A NEW KIND OF SCOPE FOR WIDEBAND TESTS/72

TI MOVES TRENCH ETCHING INTO THE FACTORY/75

MIDYEAR MARKET REPORT PAGE 44

JULY 9, 1987

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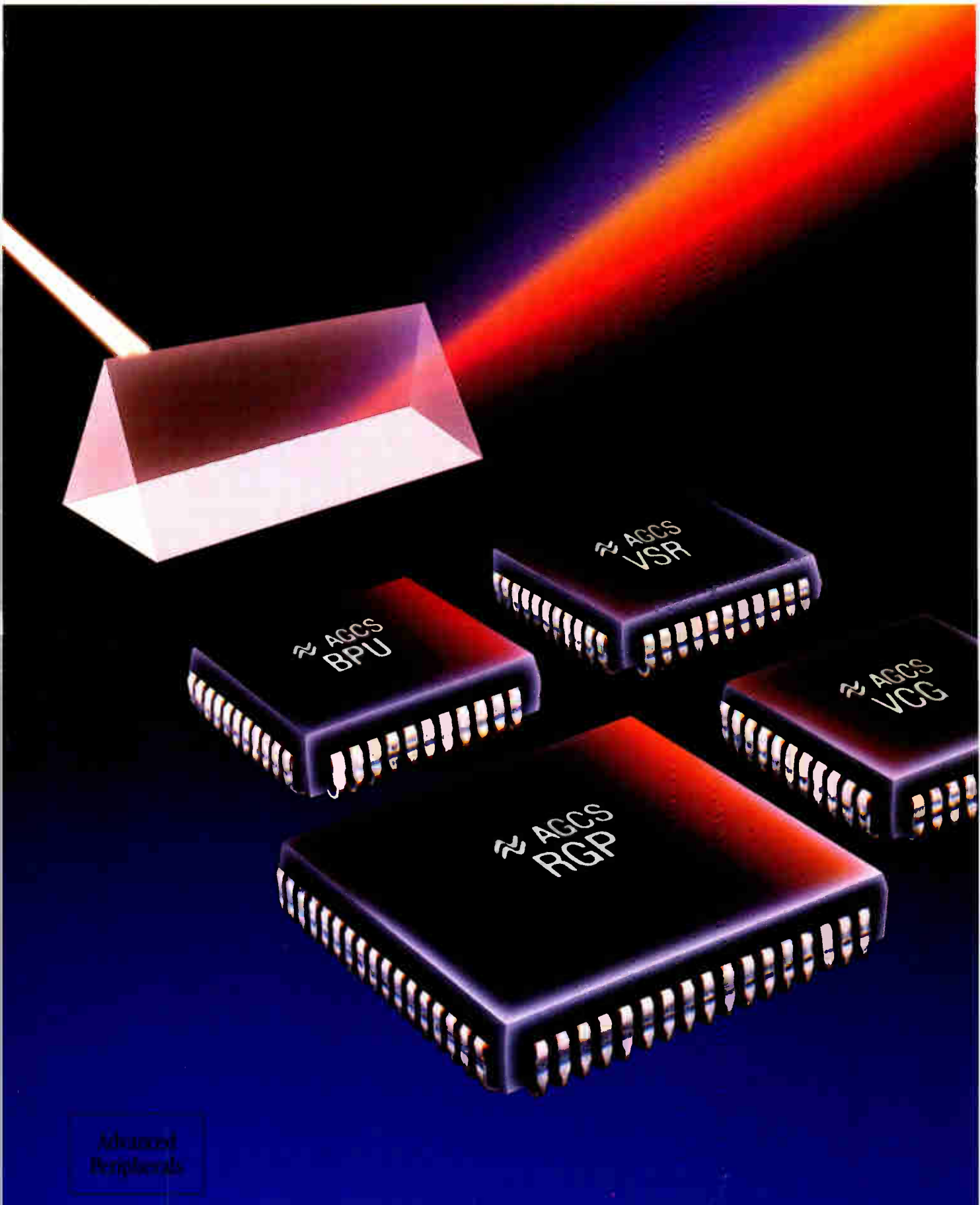
THE NEW FACES OF NONVOLATILE MEMORY

PAGE 61

- WAFERSCALE'S 256-K EPROM RUNS SUPERFAST/65
- CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS/67

National Semiconductor



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Video Clock Generator (VCG). A timing and control generator providing all of the synchronization signals needed by a graphics system, with a pin-programmable pixel frequency of up to 225 MHz. Available now.

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The secret to all this flexibility and performance is our unique multiple-chip, modular approach. Rather than trying to squeeze all the important graphics functions onto a single chip — which would require some significant design and performance compromises — we've partitioned appropriate functions onto individual building-block ICs. This allows us to optimize the design of each chip, and allows you to optimize your own design for your particular application.

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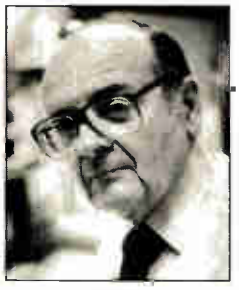
MITEL Semiconductor

Electronics

It's report-card time again. In this issue we take our annual midyear look at the state of the electronics markets, examining how the growth forecasts for 1987 that are being made now compare with those that were made for our big, first-of-the-year *Electronics* Market Report. The most recent results are on p. 44; the conclusion, in a nutshell, is that in most cases the estimates are being scaled down.



WEBER

WOLFF

Even as we make that comparison, we are using this quick July snapshot as a dry run for our full-blown 1988 U.S. market report, which we will publish in the first issue of 1988. Preparations for that survey—one of our most widely read features—are already under way under the direction of executive editor Sam Weber. Even before most of the people who will contribute to the report have looked into their crystal balls to see what kind of year they and the industry will have next year, Sam is collecting data, revising and fine-tuning the questionnaires that will go to selected companies early in the fourth quarter, and studying various methods of making the survey more valuable to our readers.

"Our basic methodology, which we have perfected over the years since we did our first report in 1958, will be unchanged," says Sam. "For the domestic report, executives of companies that make the equipment or components listed will estimate total U.S. consumption in the markets that they serve. For the overseas reports, the estimate is for consumption in each nation covered. The *Electronics* staff will then analyze the replies, and where necessary supplement the results with more research. We also check with market-research firms to see if their numbers mesh with ours."

For this issue's considerably shorter update, the technique was necessarily altered. Howard Wolff, the associate managing editor who was responsible for editing and producing it, says, "We relied on the reporting of our department and field editors. They questioned their most knowledgeable sources and boiled down the replies."

Wolff continues, "The toughest problem is not getting the information, but reducing it enough to fit in the three pages allotted for the article. For myself, the most difficult obstacles are addition and subtraction. But my family must have heard my complaints, because for Father's Day I got a printing calculator. And I truly appreciated it."

The popularity of our market reports can by judged by the number of letters and phone calls that we get suggesting changes or disagreeing with our conclusions. We don't keep count of them, but typical of the complaints was one letter from a reader who insisted that our calculations were wrong. This alarmed us, so we phoned him and asked how he had decided that. It turned out that *he* had added the figures incorrectly.

So it might be said that the first rule for reading a market forecast is to add the columns correctly. And if that proves difficult, try to borrow Wolff's new calculator.

Laurence Altman

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JULY 9, 1987

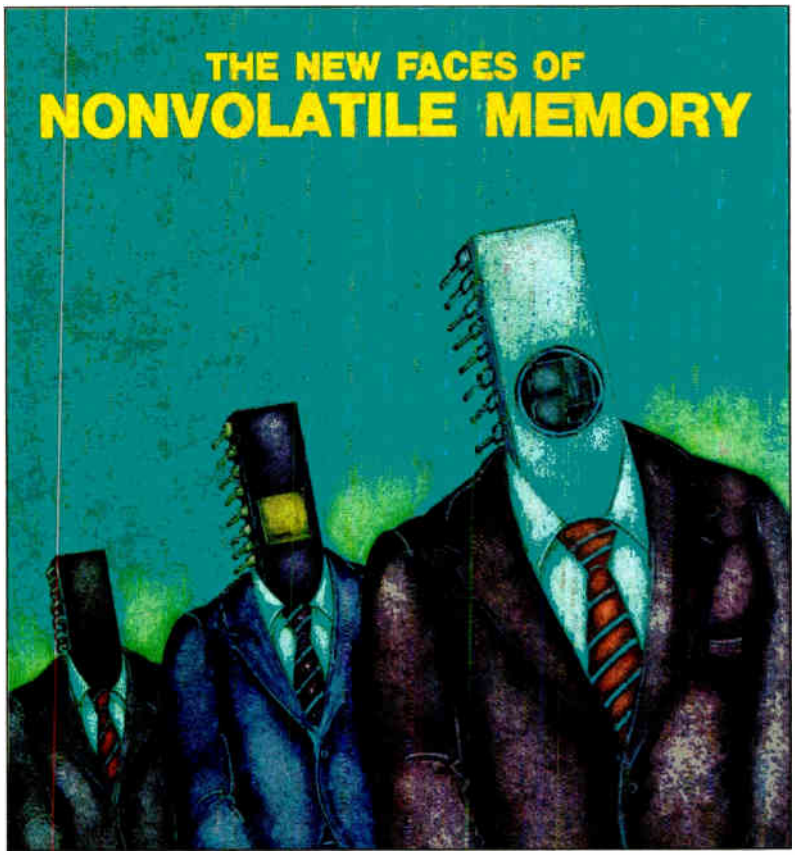
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: MICHAEL A. DONATO



PAGE 61

NEW PRODUCTS

Newsletter, 25
- RISC processor from MIPS is twice as fast as the 80386 yet costs no more
- Emulex 14.4-Mbit/s modem will cost the same as 9-Kbit/s units
- Chromatics color display has twice the speed of competitors
- Graphics board more than doubles the resolution of IBM PS/2

Design & Test, 102
- Place-and-route software from Shared Resources uses a gridless routing system to boost speed and density of pc-board designs

Computers & Peripherals, 104
- Data Translation's image-processor board offers 8-megaflops performance and bypasses the PC-bus bottleneck
- A work station from Datamedia runs MS-DOS while concurrently emulating DEC's DT240 graphics terminal

Semiconductors, 108
- Four Chips & Technologies ICs enhance the resolution and speed of PC AT clones
- Micro Linear's chips virtually eliminate the need for manual equalization of phone trunk lines

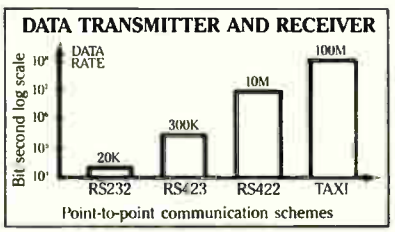
Military/Aerospace Newsletter, 97
- Why the Army canceled the RFP for its latest remotely piloted vehicle
- New Air Force unit will oversee long-term electronics R&D
- Everyone wants to study Soviet electronics technology for the U. S. Air Force
- Obtaining export licenses could get a lot easier and faster

DEPARTMENTS

Conventional wisdom is fine. For conventional designs.

Imagine a parallel-to-serial converter that lets you move data at 100 Megabits per second. Imagine it working like a register, shooting data into a latch that's stretched from point to point, letting that data race, transparently, ten times faster than conventional wisdom says it can go.

You just imagined TAXI—the Am7968 Transmitter and



the Am7969 Receiver—two of the most unconventional, incalculably useful products we've ever offered.

Our new 125MHz analog Phase-Lock-Loop receiver runs ten times faster than the popular 26LS family of RS422 devices. That makes TAXI the highest speed serial data device available. And, where you used to use ribbon cable or bundles, you can design with a single coaxial or fiber optic cable.

Its simplicity and speed don't confine you to a narrow data path, though. Twelve parallel interface pins allow you to operate with data that is 8, 9 or 10 bits wide. TAXI is cascadable, too, in multiples of 8, 9 or 10 bits. They all move through a single cable to get the message across fast.

To get your hands on TAXI, just call 1 (800) 634-TAXI. And when someone says "You can't move data that way!," you can just smile and say, "Watch."

Advanced Micro Devices

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Circle 7 on reader service card

FYI

Not everyone is getting cold feet about the near term; plenty of people are still plowing a lot of venture money into startup companies

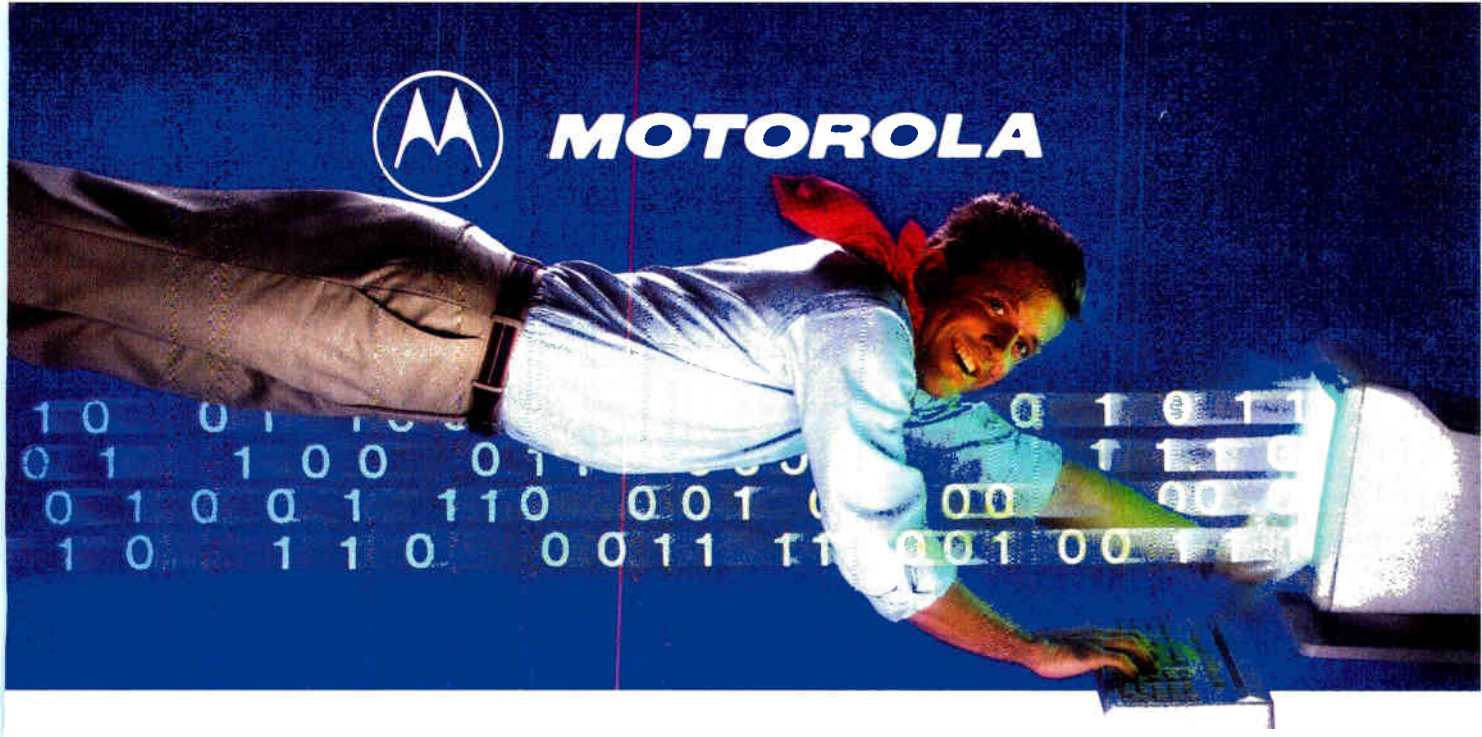
The headline on Jack Beedle's June 18 *In-Stat Electronics Report* stirred my blood: "The U.S. semiconductor order rate surges above a billion dollars in May!" Jack goes on to say it's the first time that monthly orders have broken the billion dollar barrier since August 1984! But Jack then proceeds to stomp on my enthusiasm. He does *not* believe the market can sustain itself at today's rate for the rest of 1987. And semiconductors is one of the industry's brightest spots these days.

For more on how the rest of 1987 looks, see our midyear market report beginning on page 44. For three of the five key markets surveyed, industry predictions of growth rates have declined since the beginning of the year. Maybe the question ought to be: Why are industry executives getting cold feet over the 1987 business outlook?

Not everyone is getting cold feet about the near term. Plenty of people are still plowing money into new companies. Dick Shaffer, who writes the *Technologic Computer Letter* from New York, reports in his latest survey that computer-related venture investments continue at a steady pace. Investors put $259 million into ventures in the first quarter, he says, running flat with the previous seven quarters. Not bad for something some people thought was past its prime!

Surprisingly, one kind of investment running a lot higher than normal was seed financings or first venture rounds. More than 10% of the first-quarter venture money, Dick estimates, went into 12 of these companies. Eight were chip-related: Advanced Power Technology in Bend, Ore., ASIX Systems in Fremont, Calif., Interactive Video Systems in Concord, Mass., Krysalis in Albuquerque, N. M., Prisma in Colorado Springs, Colo., SILC Technologies in Waltham, Mass., Solid State Technologies in San Jose, Calif., and Vitesse Electronics in Camarillo, Calif. Not bad for a market that's supposed to be getting far too crowded in even its fastest-growing niches.

It's been a year since we brought *Electronics* back on course as the industry's preeminent biweekly. And according to what you've told us, we've made real progress in recovering our crown. While we have continued to add new editorial features to the magazine, we certainly welcome any new ideas, or suggestions. If you've got any, please write me. I'd like hearing from you. **ROBERT W. HENKEL**



Stick to the truth at top speed.

Keep high-performance memory systems accurate, reliable with F2960/2960A control.

Fact is, today's big, fast memory arrays can separate you from reality with a single data-bit lie. Instantly, without explanation or correction.

Fortunately, there's a way to keep DRAM systems on the straight and narrow: the MC74F2960/2960A EDAC and associated LSI devices.

They do what discrete logic can't: maximize reliability, performance and economy. Without taking up usable board space.

High-speed errata eraser.

The F2960/2960A contains all logic needed to correct any single-bit error and detects all double- and some triple-bit errors. It generates 6 check bits on a 16-bit data field, 7 for 32-bits and 8 for 64 bits according to a modified Hamming code and corrects data in nanoseconds.

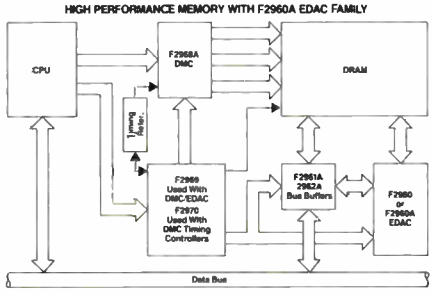
Motorola 'A' System Max Speed vs Standard System				
Mode	Path	Am2960/61	MC74F2960A/61A	% Improvement
Generate	Total Delay	57 ns	32 ns	44%
Detect	Total Delay	47 ns	29 ns	38%
Correct	Total Delay	100 ns	65 ns	35%

Featuring two diagnostic modes, the cascadable EDAC makes the error syndrome available on separate outputs for data logging.

It's pin-and-function compatible with similar units and utilizes the three-state MC74F2961A/62A inverting/non-inverting bus buffers for multiplexed bus operation.

In a 16-bit system, EDAC and buffers use about half the power of comparables.

What's more, its separate byte controls facilitate byte operations and it's fully compatible with the M68000 or comparable CPU family.



And support to make it easy.

The controller, MC74F2968A, provides complete address multiplex, refresh and drive for up to 88 DRAMs and interfaces with 16K, 64K or 256K memories.

The MC74F2969 provides all timing signals for memory control with error detection and correction, arbitrates memory cycles, handles refresh timing, memory initialization and supports error logging.

The 4-bit wide, inverting/non-inverting MC74F2961A/62A interfaces DRAMs, EDAC and data bus.

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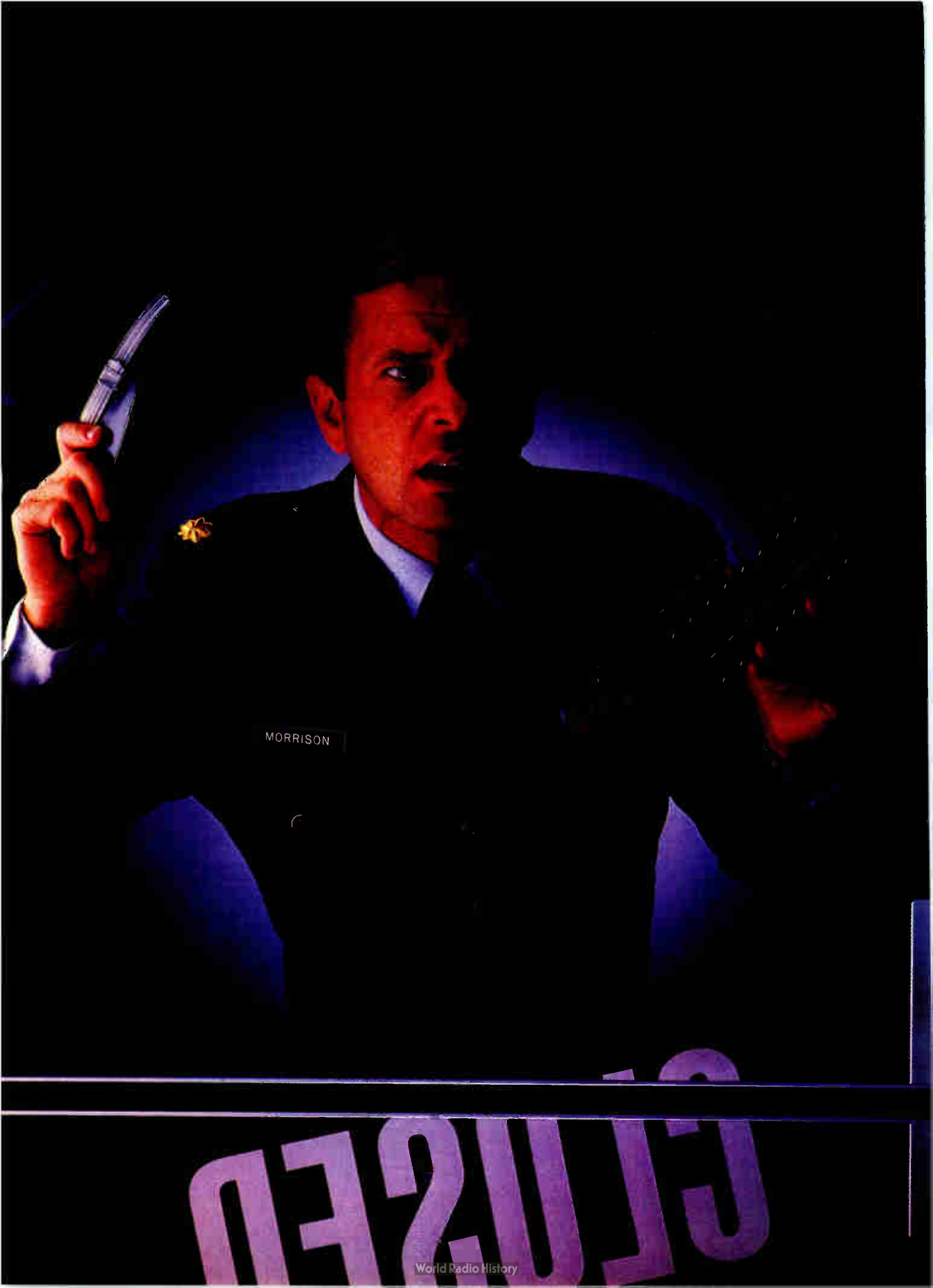

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With INMOS, you're not taking any chances. We have a seven-year history of supporting all major military defense programs with static and dynamic RAMs. Our fabrication facilities are fully compliant with MIL-STD-883C; with military burn-in, performance testing and quality assurance conducted in Colorado Springs.

We have your future in mind with our new CMOS military SRAMs (with performance to 35ns over the full military temperature range) and military low power battery backup CMOS SRAM products. And we're going to keep on producing and servicing innovative military products year after year.

For military products you can depend on, count on INMOS—the beginning of a very good memory.

16K SRAMs		
Device	Process	Access Times
IMS1400M (x1)	NMOS	45, 55, 70ns
IMS1420M (x4)	NMOS	45, 55, 70ns
IMS1403M (x1)*	CMOS	35, 45, 55ns
IMS1423M (x4)	CMOS	35, 45, 55ns

64K CMOS SRAMs	
Device	Access Times
IMS1600M (x1)*	45, 55, 70ns
IMS1620M (x4)*	45, 55, 70ns
IMS1624M (OE, x4)*	45, 55, 70ns
IMS1630M (x8)*	45, 55, 70ns

*Also available as Low Power Battery Backup CMOS SRAMs with Idr of 10µA (typical Icc at 2V at 25° centigrade)

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Circle 11 on reader service card

One for all and all for one!

To the editor: I enjoyed your article "The Drive for IC Test Bus Standards" [*Electronics*, June 11, 1987, p. 68], but would like to correct the implication that the VHSIC TM and ETM buses were developed solely by Honeywell.

These bus standards, and the other standards that ensure the interoperability of VHSIC circuits, were developed by technical teams from Honeywell, IBM, and TRW with oversight by the Department of Defense interoperability committee. It is inaccurate to imply that one or another of these companies was the principal developer of any of the standards.

G.A. Anderson
Director, VHSIC Submicron Program
Honeywell Inc.

Let me rebut...

To the editor: I was disappointed to find the cover article "GenRad's PC Board Tester Does It All" [*Electronics*, June 11, 1987, p. 59] to be full of misinformation. I have attempted to correct these inaccuracies by taking false or misleading statements and providing a rebuttal to each.

1. The article claims that the GR2750 from GenRad "... is the first board-test system that can provide concurrent analog and digital testing in real time." In 1978, Computer Automation introduced the Capable 49—a system quite adept at concurrent analog and digital testing in real time.

2. "Also, the new GenRad tester has a timing generator producing eight timing cycles to emulate any commercial or proprietary microprocessors and their buses in real time. Other board testers, with a single-cycle timing generator, must use a known-good example of the microprocessor to perform this bus emulation."

Although technically correct, the implication is that all other board testers are equipped with single-cycle timing generators. This is not true. All CA board testers provide multiple timing cycles. And our newest tester, Ironman, has a capacity eight times that of GenRad, with a full 64 timing cycles! Several other competitors also offer eight timing cycles.

3. "For the first time in the board-testing world, test engineers developing test programs and technicians running finished tests are all accessing data from one single data base." In 1983, CA coined the term "TestSharing" for this feature. Our three major board testers, the Marathon, Compact, and Ironman systems utilize TestSharing.

4. "The tester can simultaneously measure eight analog signals, each at a frequency of up to 10 MHz. Alternately, it can take on four analog high-impedance and four analog matched-impedance signals, with frequencies topping out at 50 MHz. Other testers handle up to six analog signals at frequencies between 100 and 1 MHz." CA's testers are capable of measuring up to 20 signals, each at 10 MHz with frequencies topping out at a gigahertz. I suppose there are "others" handling only up to six signals, but again the article is misleading.

5. "GenRad's system allots an unprecedented 16-Kbit-by-4-bit RAM to each pin. Its rivals back each pin with no more than 4 Kbits." CA introduced 16-Kbit-by-4-bit RAM to each pin on its Ironman tester over a year ago. And virtually all other competitors have had a minimum of 4 Kbits by 4 bits for a number of years, and several now have 16 Kbits by 4 bits.

6. "...the tester... can also accurately reproduce the complete bus cycle for any microprocessor at that microprocessor's clock rate. Until now, testers could generate only one bus cycle for each test cycle." In 1979, CA testers were reproducing the complete bus cycle for any microprocessor at its clock rate and more than a year ago provided 10-MHz real-time testing. This capability is inherent in the structure of virtually every dynamic test system produced by any manufacturer within the past four to five years.

Rick Henninger
Marketing Manager
Computer Automation

...Let me explain

To the editor: In reply to the letter from Rick Henninger, I offer the following response:

1. Concurrent analog and digital testing requires much more than the ability to take a single analog measurement in response to a high-speed digital burst of data. Concurrent operation needs both a digital and analog subsystem hardware line synchronization system and RAM memory directly behind the analog instrumentation that is employed. This means that arbitrary waveform generation of signals can be used directly in synchronism with steering signals from the digital subsystem and employed at speed because of the memory behind each instrument. Alternatively, high-speed analog samples can be taken from circuits, such as digital to analog converters, at high test rates, the results being stored in the instrument memory prior to system analysis. Unless Rick is saying that the Capable system is capable of this mode of operation, I can only believe that he was confused by the article.

2. We at GenRad do not assume that the GR2750 is the only board tester that supports multiple timing sets, and we do agree that several testers have had this facility for some time. However, the integration of these capabilities is what makes the GR2750 test techniques revolutionary and its power so significant.

3. The terms "test sharing" and "data base" are not the same, and Rick has confused them. In the GR2750's case, it means the system does not have to contain multiple circuit descriptions to handle the various test techniques employed by the test system. All of the unit-under-test data is housed in one place. All of the data for test strategy independence is housed in one data base, not many different files that can be assessed by several test systems, as is the case in TestSharing.

4. Computer Automation test systems can, as Rick says, measure up to 20 single-ended signals, but that is taking one element out of context. The GR2750 can, in addition to providing multiple analog signals to and from the unit under-test, provide full digital and analog in-circuit and functional test capabilities from a single software-controlled pin. In the case of the CA system, this same task can only be implemented via several boards within the tester and by the collection of separate testers.

5. RAM pin memory is only useful if it is sufficient to make the tester's throughput effective. The GR2750's ability to create and perform "function tests" is what makes its memory configuration notable.

6. Bus-cycle test-step generation has been available on some testers for a number of years. However, what makes the GR2750 different is that within the timing capability of the bus-cycle generation is the ability to create credible timing sets with the ability to overcome "dead zones" and "pin skew" problems that are part of many existing test systems' limitations.

In conclusion, the story of the GR2750 is not only a list of unconnected facts, but also of "integration" of a whole series of hardware and software features that make the GR2750 a test system "that does it right."

The GR2750 brings to market a new generation of test-system hardware, software, and CPU power, all tightly integrated into one system. As a result, GR2750 users can more efficiently implement true multistrategy four-quadrant testing at a higher level of performance than any competitive board-test system on the market.

David Tose
Product Marketing Manager
GenRad Inc.

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Circle 13 on reader service card

CHINA'S ZHANG: HE HAS A 'GOOD DEAL' FOR U.S. FIRMS

STAMFORD, CONN.

Zhang Zhidong, the new representative of China's electronics industry in the U.S., has one of the toughest selling jobs anywhere. The People's Republic of China wants to become a major player in world electronics markets, but it needs to meld U.S. technology with its own low-cost labor force to become a competitor in world markets. Zhang's job is to convince American manufacturers that they would not create a dangerous competitor for themselves by putting China into business.

Zhang can trot out a long list of arguments. First, China has a vast domestic market, one that is more voracious than the country's planners expected. Originally, they thought 14-in. sets would be the mainstay in color television. Now Chinese consumers are demanding 18- and 20-in. models. Planners also figured that a million color picture tubes annually would be enough for domestic consumption, but now an additional several million or more color picture tubes must be imported each year.

Though Zhang admits that with 1.4 million workers the country's electronics industry is of formidable size, he points out that exports account for only 5% of production. Also, China is less developed than neighboring countries, such as Japan or South Korea, says the 58-year-old graduate of the Radio Engineering Department of the prestigious Qinghua University in Beijing. "China is not in a position to compete with the United States or the other countries. It can only cooperate with them," he says. Also, he adds, the only electronics that China is exporting in large quantities is consumer goods, and already the U.S. spends tens of billions of dollars to buy consumer items from other Asian countries and regions each year. This state of affairs will continue for a long time to come, he maintains.

'ACW' FORMULA. Zhang hopes he can persuade U.S. firms to sign on for China's "ACW" formula—A for American technology, C for Chinese manufacturing capability, and W for world markets. If the formula works, China will be the main supplier of "low-technology" consumer electronics in the future, as Japan and other Asian countries switch to high-technology products to compensate for their rising labor costs.

Zhang, a vice president of the China National Electronics Import and Export Corp., arrived in the U.S. late last April. Along with its main selling job, the 10-member mission that he heads has two other objectives: lining up imports of American high-tech goods and exports of current Chinese products. China spends billions on imports each year, and to make sure the imports work well, service centers have been set up throughout the country. Following the lead of Hewlett-Packard Co., Palo Alto, Calif., which in 1980 established a service center in Beijing, "dozens of American companies have service centers, consultancies, liaison offices, and joint ventures in China," he says.

ZHANG. He wants to meld U.S. technology and China's low-cost labor.

Zhang's headquarters are in Stamford, Conn. He also has a three-member office in New York and one representative each in Dallas and San Francisco.

Most of the crew speak English. Zhang himself acquired his English in college and sharpened his skills while working in China shortly before he came to the U.S. "I'm ready to meet the press and talk about my business, " he says.

Comparing his work in China with his new mission in the U.S., Zhang says he feels freed from the numerous meetings and red tape he regularly faced at home. Also, "communication facilities are excellent here—people are easily reached here by phone, while in China it is much of a problem."

And Zhang intends to adapt to the automobile-oriented American way of life. Although told by his colleagues in Beijing that he was too old to learn how to drive, Zhang is taking lessons. "I need to learn the skill to be more efficient in working here," he says.

–Zhao Qinghua

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VT20C18	2K x 8	APD; 10 ns OE	20 ns
VT20C19	2K x 8	12 ns CE; 10 ns OE	20 ns
VT20C50	1K x 4	Separate I/O; FC	15 ns
VT20C68	4K x 4	APD	20 ns
VT20C69	4K x 4	12 ns CS	20 ns
VT20C71	4K x 4	Separate I/O; OT	20 ns
VT20C72	4K x 4	Separate I/O; HZ	20 ns
VT20C78	4K x 4	APD; 10 ns OE	20 ns
VT20C79	4K x 4	12 ns CS; 10 ns OE	20 ns
VT20C98*	8K x 8	APD	25 ns
VT20C99*	8K x 8	Fast CE	25 ns
VT62KS4*	16K x 4	15 ns CS	25 ns
VT63KS4*	16K x 4	15 ns CS; OE	25 ns
VT64KS4*	16K x 4	APD	25 ns
VT65KS4*	16K x 4	APD; OE	25 ns

APD = Auto Power Down, CE = Chip Enable; OE = Output Enable; CS = Chip Select; FC = Flash Clear; OT = Outputs Track Inputs During Write, HZ = High-Impedance Outputs During Write *Samples Available 4th Quarter, 1987

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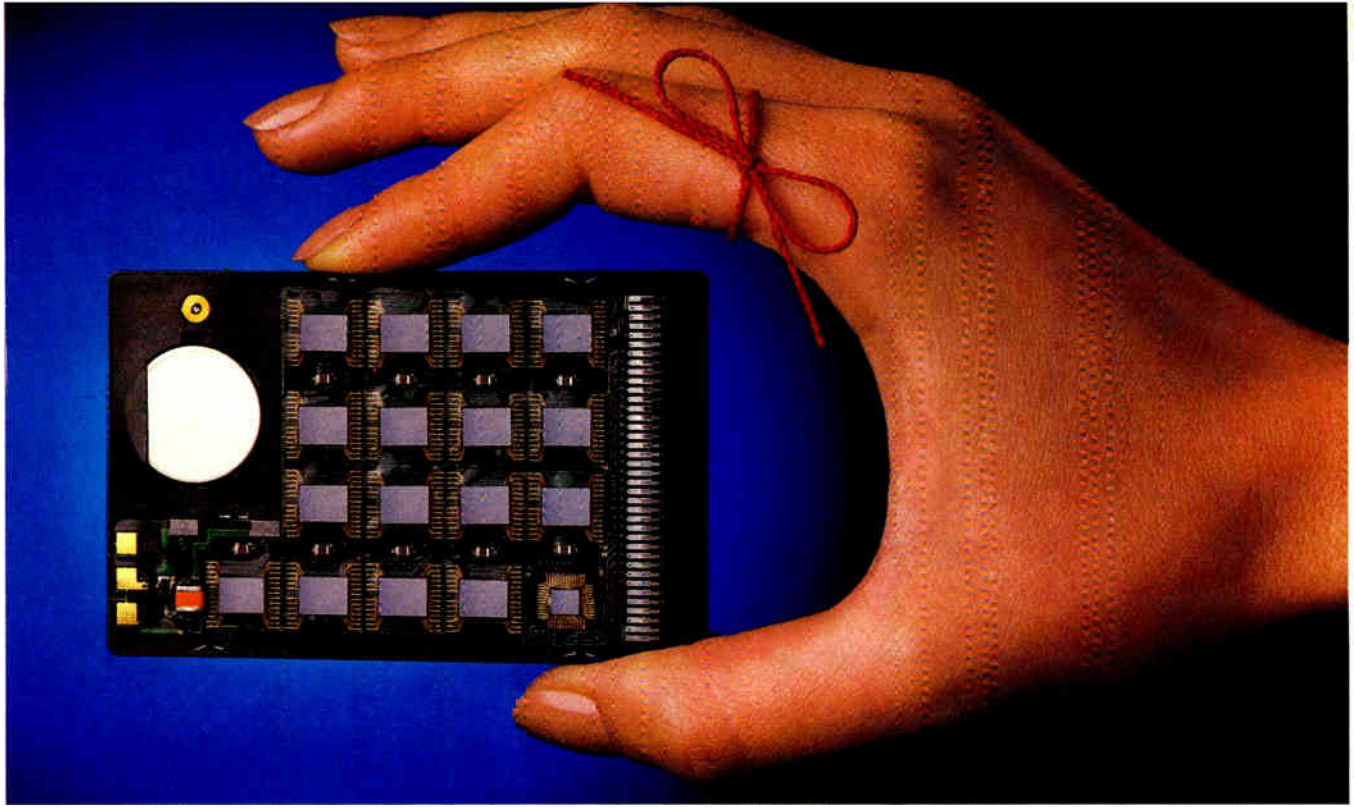

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ELECTRONICS NEWSLETTER

HITACHI'S NEW SUPERCOMPUTER LEAPFROGS CRAY...

Hitachi Ltd. has unveiled a new supercomputer that can run up to 3 billion floating-point operations/s, putting it smack in the middle of its U. S. competitors. The new S-820 model 80 will compete with several U. S.-made machines, including Cray Research's Cray 2, which runs at about 1.8 gigaflops, and ETA Systems' ETA10, which can do about 6.7 gigaflops. Based on the same chip and assembly technology used in Hitachi's two-year-old M-680H mainframe, the S-820 model 80 gets its added power partly from a 12-pipeline architecture (four more than the M680H) that lets it operate internally like a multiprocessor machine. Two chips not used in the mainframe and a new memory-extension system also aid performance. The special chips include an emitter-coupled-logic vector register—actually a 7-Kbit random-access memory integrated on a 2,500-gate array that boasts 2.5-ns access times—and Hitachi's own BiCMOS, ECL-compatible, 64-Kbit dynamic RAM, which has an access time of 13 ns, and makes possible a board access time of 20 ns (half that of the M680H). Main memory capacity for the system is 512 Mbytes, but high-speed file memory can range up to 12 gigabytes. Deliveries will start in the first quarter of 1988, with rental fees beginning at about $545,000 per month. □

...BUT THE SUPERCOMPUTER LEADER HAS THREE FASTER MODELS COMING

With Hitachi and a myriad of others nipping at its heels, supercomputer leader Cray Research Inc. is not sitting on its hands. The Minneapolis firm is pushing ahead with its plans for three new, increasingly parallel and ever faster supercomputer architectures between now and 1994. First out will be the Y-MP, an eight-processor system based on VLSI silicon technology that is expected to hit a peak speed of 3.2 billion floating-point operations per second. That machine, scheduled for delivery next spring, will be followed by the Cray 3 in 1989 or 1990. Incorporating gallium arsenide chip technology and a 16-processor design, the Cray 3 will up the performance ante to the 12-to-20-gigaflops range. Beyond that, Cray is looking toward the 1992-94 timeframe for production of a system currently code-named the MP. That machine features more processors working in parallel—perhaps as many as 64. Circuit technology for the MP has not yet been determined, but devices based on advanced GaAs high-electron-mobility transistors are a possibility. □

A WORRIED TOSHIBA MOVES FAST TO MOLLIFY U. S. AND STOP IMPORT BAN

Look for Toshiba Corp. lobbyists to swarm over Capitol Hill as the Japanese firm strives to appease the U.S. government and thus avoid heavy sanctions for illegally selling high-tech milling equipment to the Soviet Union. The Japanese firm is taking very seriously the strong signal sent out by the U.S. Senate, which on July 1 voted 92-5 to ban Toshiba and its partner in the technology diversion, Norway's Kongsberg Vapenfabrik, from importing goods to the U. S. for at least two years. The day after, Toshiba's top two officials resigned and its U.S. subsidiary hired a Washington law firm to handle its case. Chairman Shoichi Saba and president Sugiichiro Watari said they were taking personal responsibility for the sale, even though they had no knowledge or control over the deal, which was made by a 51%-owned subsidiary, Toshiba Machine Corp. Saba said he would take responsibility "for not creating an atmosphere throughout the Toshiba group that would make such activity unthinkable." Toshiba Machine sold $23 million worth of equipment for manufacturing submarine propeller blades to the Soviets in 1983 and 1984 [*Electronics*, June 11, 1987, p. 53]. The Senate action, part of a broader trade bill, is not final; although the House is considering similar legislation, the Reagan administration is opposed to the general bill. □

ELECTRONICS NEWSLETTER

NOW, A NEW FIGHT: INTEL, MOTOROLA OFFER STANDARD-CELL MICROPROCESSORS

Microprocessor leaders Intel Corp. and Motorola Inc. are ready to turn the application-specific integrated-circuit world on its ear—the first of their most popular computer chips are ready as standard cells. Intel president Andrew Grove is already claiming "the first onslaught of design wins" for the cell-based 80C51 standard microcontroller, a single-chip ASIC that also holds a choice of necessary peripheral functions (see p. 51). At Motorola, customers now have access to an ASIC version of the MC6805 single-chip microcontroller. Both offerings are making a splash, says Michael Kubiak, a San Francisco-based analyst with Kidder Peabody and Co. Both firms plan other introductions soon: Intel will release a cell version of its 16-bit 80186, and Motorola a version of its EEPROM-based 68HC11 single-chip microcontroller. □

FOUNDRY HITCH SLOWS NATIONAL'S ENTRY INTO FAST SRAM MARKET

Plans for fast 64-Kbit and 256-Kbit static random-access memories at National Semiconductor Corp. are slipping away as its Japanese production partner struggles with converting what was originally a DRAM-oriented line into a SRAM foundry. The high degree of automation in the fabrication line is also presenting hurdles, according to managers familiar with the effort. National—in step with a U. S. chip-industry trend—agreed last fall to supply its fast static designs to NMB Semiconductor Ltd., which in turn was going to produce 8-K-by-8-bit and 32-K-by-8-bit SRAMs for the Santa Clara, Calif.-based firm [*Electronics,* Oct. 16, 1986, p. 154]. "That agreement is not really dead, but [it] is somewhere between comatose and dormant," acknowledges Alan Ankerband, MOS memory marketing manager at National. □

SUN RIVER USES OPTICS TO LET USERS SHARE 80386-BASED PCs

Typical local-area networks for personal computers enable users to share and exchange data, but their bandwidth is insufficient to let them share high-resolution bit-mapped color graphics. Now Sun River Corp., Jackson, Miss., thinks it can change that, with new terminals and a 32-Mbit/s fiber-optic link that lets up to 16 users share the power of a multiuser 80386-based personal computer, such as Compaq Computer Corp.'s DeskPro 386. The Cygna 386 Fiber Optic Station looks like a terminal but for $2,000 offers the color graphics and functionality of a PC. The stations can handle true bit-mapped graphics, can run more than one DOS application package at once, and take advantage of the power of the 80386 processor at the heart of the host. □

SHORTCUT TO MARKET: TI OFFERS ITS OWN SYSTEM FOR GENERATING SOFTWARE

Texas Instruments Inc. is taking a shortcut to a new market by introducing a system that it already uses inside the company to automatically generate business software. The first two components of TI's Information Engineering Facility are for IBM Corp. computers: the Analysis Toolset for Personal Computers and the Mainframe Encyclopedia for IBM mainframes. Analysis Toolset depicts application needs in graphic form using five integrated diagramming tools; Mainframe Encyclopedia acts as a central repository for information collected by the PC Toolset. The software-design system was developed for internal use by TI's Information Systems and Service Group in Plano, Texas, and company observers say its introduction as a commercial product is a key move in TI's strategy to exploit captive technologies to enter new businesses. The Information Engineering Facility is aimed at applications in accounting, personnel programs, facilities management, and manufacturing systems. The Mainframe Encyclopedia sells for $70,000, and the Analysis Toolset costs $9,400. □

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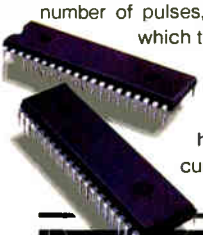

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*All execution speeds are real-world, not theoretical, and include overhead times.

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MACH Microcode Assembler And Simulator ..... for algorithm developers ($1495)
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PRODUCTS NEWSLETTER

MIPS RISC PROCESSOR IS TWICE AS FAST AS 80386 YET COSTS NO MORE

Work-station manufacturers can now buy a reduced-instruction-set processor from MIPS Computer Systems Inc. that delivers twice the performance of Intel Corp.'s 80386 microprocessor for about the same price. Available in 12.5- and 16.67-MHz versions, the R2000 chip's RISC architecture provides enough processing power to drive work stations at a pace of between 8 million and 12 million instructions/s, depending on clock speed, cache memory, and other system-design variables—compared with 4 to 5 mips for 80386-based work stations, says the Sunnyvale, Calif., company. The 12.5-MHz version will sell for $195 in 5,000-unit quantities; the 16.67-MHz version, $295. Both are available now. Systems software and third-party tools are also available for another $100 per CPU. □

EMULEX 14.4-KBIT/S MODEM TO COST THE SAME AS 9.6-KBIT/S PRODUCTS

Look for computer-products specialist Emulex Corp. to break into the communications hardware market with a 14.4-Kbit/s modem that offers a 50% performance advantage over the 9.6-Kbit/s modems now standard for leased-line transmissions. A proprietary CMOS six-chip set is the key factor bringing the Performance 1000 full-duplex modem in at just $1,795—about the same price as the 9.6-Kbit/s modems, claims the Costa Mesa, Calif., company. The chip set also delivers a 50% reduction in component count, which contributes to an 8½-by-11-in. footprint for the 2½-in.-high modem—the smallest available at 14.4 Kbits/s. The modem also features menu-driven operation monitored by a liquid-crystal display. Available now, the modem conforms to the CCITT V.33 standard. A 9.6-Kbit/s version conforming to the V.29 standard sells for $1,295. □

CHROMATICS COLOR DISPLAY HAS DOUBLE THE SPEED OF COMPETITORS

By implementing the industry-standard Graphical Kernel System software in microcode, Chromatics Inc. has come up with a color display system that draws 1 million fully transformed two-dimensional vectors per second—double the speed of competitive systems. The LeMans Colorgraphic Display can also draw 250,000 three-dimensional vectors/s and generate 25,000 smooth-shaded polygons/s with hidden-surface removal in 3-d applications. Its graphics engine is based on multiple processors arrayed in a 32-bit pipelined architecture. A standard 32-bit VMEbus interconnection provides an open architecture that interfaces easily with host computers from Sun Microsystems Inc. or Digital Equipment Corp.'s VAX series. Available in the third quarter with a 1,280-by-1,024-pixel display, the LeMans costs $25,000 each; volume discounts are available. □

GRAPHICS BOARD MORE THAN DOUBLES RESOLUTION OF IBM PS/2

A color-graphics controller board from Control Systems Inc. boosts the standard 640-by-480-pixel resolution on IBM Corp.'s Personal System/2 products by factor of more than 2.5—to a resolution of 1,024 by 768 pixels noninterlaced or 1,024 by 1,024 interlaced—while at the same time maintaining compatibility with IBM's video-graphics-array standard. Built around Hitachi Ltd.'s ACRTC graphics processor, the Artist 10/16 VGA board also offers a 16-color palette and 1 Mbyte of on-board graphics memory. A redesigned version of the company's Artist 10/16 for IBM's Personal Computer family, the new controller board plugs into a 136-connector slot in the PS/2 motherboard to work effortlessly with the machine's Micro Channel architecture. The Artist 10/16 VGA will be available in August from the St. Paul, Minn., company for $1,797 in 100-unit quantities. □

PRODUCTS NEWSLETTER

CONVERGENT SERVER OFFERS INSTANT ACCESS TO DOS AND UNIX AT 5.7 MIPS

Convergent Technologies Inc.'s departmental server for networks of personal computers combines a 20-MHz Intel Corp. 80386 microprocessor and a 64-Kbyte memory cache with zero wait states to reach 5.7 million instructions/s—and simultaneous access to MS-DOS and multitasking Unix environments. Using the San Jose, Calif., company's PC Exchange/Vines networking software, 386 Server PC can handle up to 64 personal computers or 32 terminals. Its basic configuration includes 1 Mbyte of memory, a 5¼-in. floppy-disk drive, an 80-Mbyte hard disk, and slots for three more SCSI peripherals. Memory is expandable to 64 Mbytes and disk storage to 1 gigabyte. The server runs both Microsoft Corp.'s MS-DOS 3.2 operating system and CTIX/386, Convergent's implementation of AT&T Co.'s Unix System V Release 3. Available in the third quarter, it will cost $7,500. □

QUAD DESIGN CUTS TIMING VERIFICATION FROM DAYS TO MINUTES

Accurate timing analysis is the neglected stepchild of pc-board-design software, and Quad Design Technology aims to correct that with Motive, a tool set for timing verification. Current tools use simulation and test vectors to handle problems such as clock skew, interconnect delay, and multicycle paths—a method that can take hours or even days. The Camarillo, Calif., company's Motive (for Modular Timing Verifier) runs verifications in minutes by analyzing circuits over the worst-case range of component parameters. A version for IBM Corp. Personal Computer ATs and compatibles costs $1,995. Component libraries for microprocessors, memories, and specialized components such as Fairchild Semiconductor Corp.'s FAST family cost $500 each. Versions for Sun Microsystems work stations start at $12,000. All are available now. □

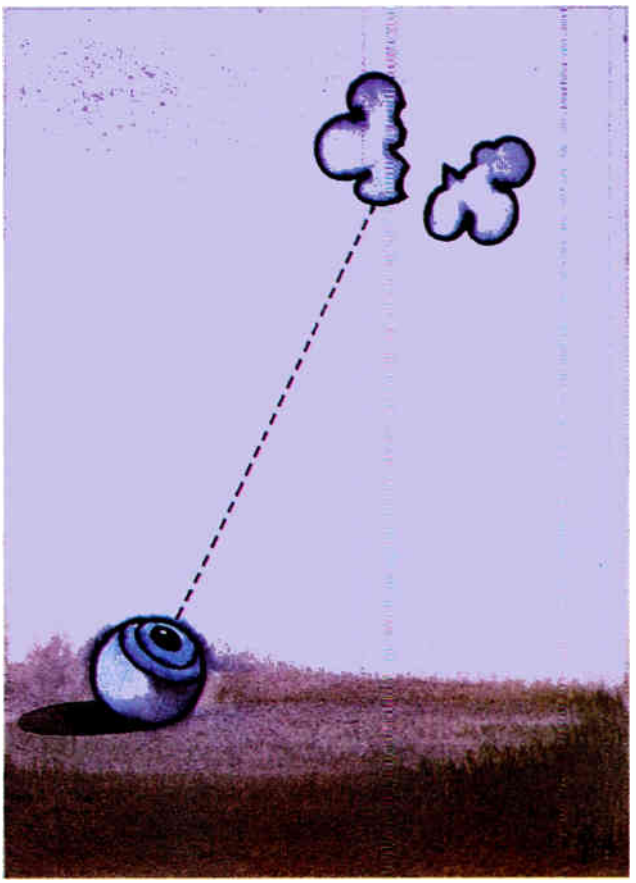
TI'S DIGITAL CROSSBAR SWITCH UNCLOGS BUS BOTTLENECKS

Bottlenecks in the buses of multiple-processor systems may soon be eliminated, now that Texas Instruments Inc. is in production with a digital crossbar switch that can transmit or read data from any combination of 16 input/output ports on the fly. The 32-bit bipolar AS8840 [*Electronics,* Feb. 5, 1987, p. 72] has 64 I/O pins grouped in 16 separate 4-bit, nibble-wide bidirectional ports. Port-to-port data transfers take 25 ns, compared with 100 ns for current MSI implementations that use two VMEbus boards. The device can be used to closely couple multiple processors to one another, to common or private memory blocks, or to system I/O, says TI. Its microprogrammability suits it to a wide range of parallel-processing architectures, such as single-instruction, multiple-data systems or in multiple-instruction, multiple-data systems. Housed in a 156-pin grid array, the AS8840 costs $93.60 each in 1,000-piece quantities. □

HARRIS CUTS DEVELOPMENT TIME FOR REAL-TIME APPLICATIONS

The operating system for two new multiprocessor superminicomputers from Harris Corp. Computer Systems Division has been especially tailored to cut development time for real-time applications. The RT-VOS/MP (real-time virtual-operating-system multiprocessor) gives developers tools to schedule tasks for up to 12 CPUs and to design and test time-critical code—features not available until now—says the Ft. Lauderdale, Fla., company. The operating system uses only 10% of CPU time for overhead. On the hardware side, the H-1600 supermini incorporates three processors based on 100K emitter-coupled-logic technology. Each processor runs at 5 million instructions/s and has its own 80-Mbyte/s memory bus to reduce shared-memory bottlenecks. Available now, the H-1600 costs $795,000. The dual-processor H-1500 costs $555,000. □

If it happens in a blink, we'll catch it.



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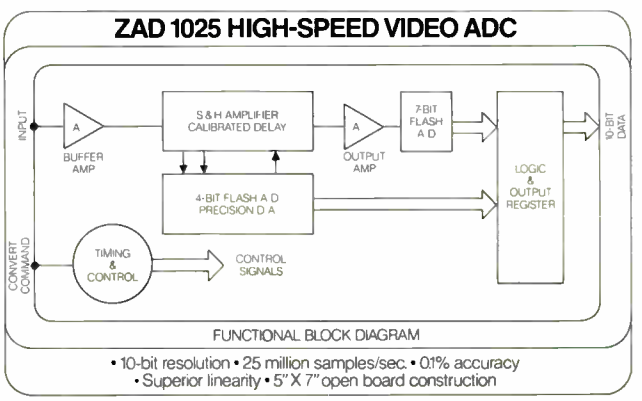

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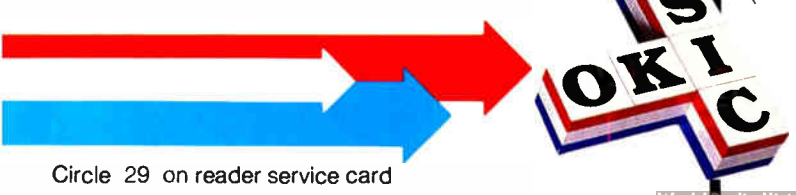

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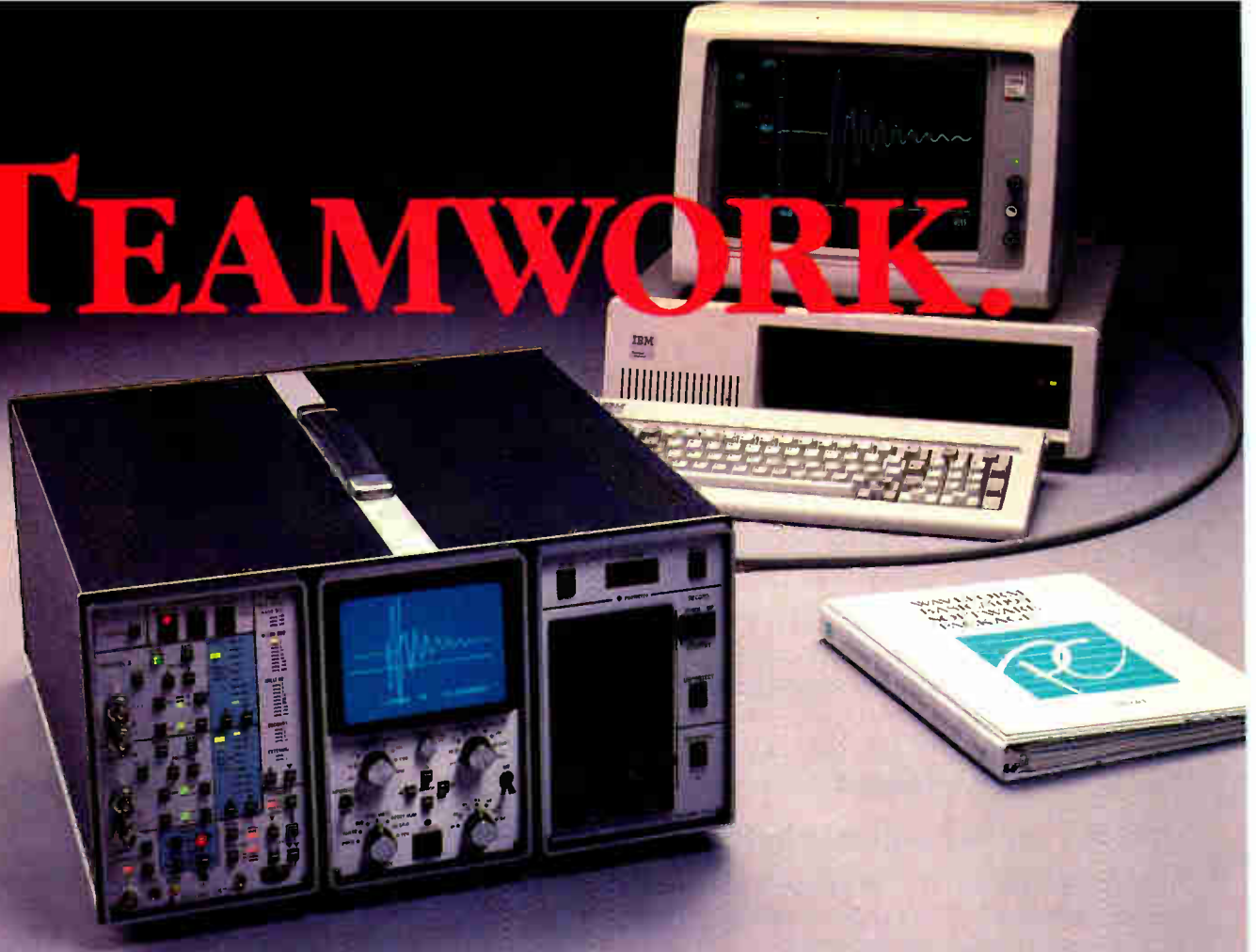

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Electronics

CAE IS FINALLY BEGINNING TO LIVE UP TO ITS PROMISE

FASTER PLATFORMS AND SIMULATION PACKAGES PROVIDE THE IMPETUS

MIAMI BEACH

In the annals of computer-assisted engineering, 1987 could well go down as the year the pieces came together. For the 107 exhibitors and some 4,000 showgoers at the Design Automation Conference in Miami Beach, the five-year-old promise of CAE—to speed product development even as it leads to better products—began to come true.

The big trends are clear. In hardware, it's faster and far less expensive workstation platforms; in software, it's more sophisticated simulation along with improved simulation models.

With the parade of work stations taking on the character of a mips war, Apollo Computer Inc. took the conference spotlight by unveiling its Domain series 4000 Personal Super Workstation (see p. 32). The machine, rated at 4 million instructions per second, can do simulation of 100,000 gates, complete system timing, and testability analysis—a run that previously required an accelerator.

The series 4000, at under $19,000, is today's price-performance leader, but the field is jammed. Digital Equipment Corp. has jumped in with its new $7,900 color VAXstation line [*Electronics*, June 25, 1987, p. 42]. Intergraph Corp. has a new under-$30,000 5-mips model, and Sun Microsystems Inc. is joining the bunch with a 10-mips machine. Hewlett-Packard Co.'s new $69,000 Model 825SRX carries 8-mips credentials.

Hand in glove with more powerful and cheaper platforms are faster simulators. For example, Cadnetix Corp. of Boulder, Colo., introduced its Configurable Analysis Engine, a network processing node that accelerates the compilation of data required for a simulation run even as it performs the digital and analog simulation process itself.

Another new class of simulators runs as fast as those requiring high-performance hardware—but without the hardware. Typical is the Verilog simulator from Gateway Design Automation Corp. of Westford, Mass. "In addition to full behavioral language, Verilog-XL simulates at the gate and even switch levels, and works faster on a work station than most hardware accelerators costing $100,000," says Prabhu Goel, president.

Simulators are being improved in other ways, too. LSI Logic Inc. of San Jose, Calif., unveiled a revamped LSIM, the first multimode simulator, which offers behavioral, logic, switch, circuit, analog, and fault simulation. The new version also has an interactive waveform viewer that lets designers pan and zoom and make voltage and timing measurement directly off the waveform. Through multiple simulation windows, the designer can view simultaneous inputs and outputs in both alphanumeric and waveform displays, says Van Lewing, director of software marketing.

While some suppliers are adding functions to their simulators, others are tailoring their products to run on lower-priced work stations. One such product is from Orcad Systems Corp. of Hillsboro, Ore. The company says its new simulator can easily handle designs with as many as 14,000 gates on a standard personal computer with an extended graphics card and 640 Kbytes of memory.

But simulators are no better than the models they run. "A simulation engine without good models is like a car without wheels," says Richard Perry, marketing vice president of FutureNet, a division of Data I/O Corp. in Chatsworth, Calif. "There aren't enough models out there, especially ones certified by the IC vendor." To address this problem, Logic Automation Inc. of Beaverton, Ore., and Quadtree of Bridgewater, N. J., have embarked on ambitious programs to have their models certified by IC vendors.

–Jonah McLeod and Stan Runyon

AUTOMATED SOFTWARE DESIGN IS TAKING OFF, TOO

Computer-aided software engineering is fast becoming a critical component in an increasing number of electronic design automation systems. Many of the EDA system vendors at the Design Automation Conference in Miami Beach are adding CASE to their product lines. Digital Equipment Corp., for example, announced a cooperative marketing program with Cadre Technologies Inc. to include its Teamwork series of CASE tools in DEC's stable of EDA applications. DEC also has a marketing agreement with Tektronix Inc. for its CASE tool set. Hewlett-Packard Co. is also offering Teamwork.

CASE products promise faster software development with fewer errors. The coupling of computer-aided documentation to CASE adds another measure of productivity and control. Vendors are working to tie both types of tools intimately into their EDA systems.

At Miami Beach, Cadre Technologies, one of the leading vendors of CASE tools, proposed a standard for interfacing CASE to existing EDA applications. Cadre has suggested an extension to the EDIF—Electronic Design Interchange Format—standard for interchanging data among CASE tools and other EDA applications.

Context Corp., a Mentor Graphics Corp. subsidiary that markets a computerized documentation system, maintains that automated documentation tools will play a critical role with CASE in integrated EDA systems. Context's system goes beyond computerized document preparation and publishing. It manages and controls all hardware and software changes to system-design documentation. Context's change-control feature can become the basic tool in an EDA system for management of a product development project.

As with the other functions in an EDA system, CASE and documentation tools must be tightly integrated to be most effective. An example of integrating CASE and computerized documentation is the system the Boeing Co. put together for itself. The Boeing Automated Software Engineering system includes a system design environment from Teledyne-Brown, a structured analysis software development environment from Cadre, and the Context documentation system, all using the same data base.

–Tom Manuel

APOLLO AND SUN HEAT UP THE MIPS WAR

BOSTON

Activity in the work-station business is getting as hot as the weather as the summer progresses. First there was Digital Equipment Corp. announcing its low-end $7,900 color VAX [*Electronics*, June 25, 1987, p. 42]. Then, last week, Apollo Computer Inc. came along with a new machine as well as a new strategy. And Sun Microsystems Inc. in a media blitz on July 7 introduced its station based on reduced-instruction-set architecture that can handle 10 million instructions per second.

TAKING THE MIDDLE. Apollo, with its Domain series 4000, is trying to establish a midrange between low- and high-priced work stations.

Apollo, in Chelmsford, Mass., calls its new desktop entry—the Domain series 4000—a "Personal Super Workstation." The series 4000 is based on a 25-MHz Motorola MC68020 microprocessor and a 25-MHz MC68881 floating-point coprocessor, which help the system achieve its 4-mips rating.

Of equal importance is the new company strategy: to create a midrange between entry-level and very-high-performance units. Prices for monochrome versions of the series 4000 begin at $13,900, and color models start at $18,900. The line fits between Apollo's series 3000 personal work stations—newly reduced in price to start at $4,990—and the DN590 Turbo, the high-performance 3-d solids-modeling graphics station introduced in May [*Electronics*, May 28, 1987, p. 46] that starts at $57,900.

OPPOSITION. A 19-in. color version of the 4000, including both 25-MHz processors, 8 Mbytes of memory, 8 planes of color, and 1,024-by-800-pixel resolution, sells for $25,900. It is equipped with an Apollo token ring or Ethernet communications software and an operating system. Cheryl Vedoe, Apollo's group manager for personal work-station marketing, compares this variation with two similarly configured machines from competitors: the Hewlett-Packard 9000 350C, priced at $32,900, and the Sun 3/260C, which sells for $44,900.

Actually, Vedoe says, neither DEC nor Sun has a high-performance personal work station, but Sun's 3/260C is the most directly comparable machine. Sun's John Hime, director of product marketing, counters that the series 4000 "is not the kind of thing our customers ask for. Apollo must be responding to some particular customer requirements they know about."

But Mark Stahlman, a research analyst with Sanford C. Bernstein & Co. in New York, who follows the work-station market closely, says flatly that the series 4000 is "hands-down the best midrange product in the industry."

Stahlman agrees with Vedoe that Sun doesn't have a product comparable to the series 4000, but suggests that Sun's new products will begin to position the firm as more than a work-station company. He expects to see the beginnings of a family of superminicomputers that will push Sun into the 30-mips performance range. Sun's Hime would not comment.

Besides dramatically cutting prices on the series 3000, Apollo has also enhanced the 16-month-old line. Analyst Stahlman sees the revamped machines as the most attractive low-end offerings in the market, including DEC's new VAXstation line. Among the improvements are reduction of the two-board Apollo token-ring network controller to one board through the use of custom CMOS gate arrays, and replacement of the "piggyback" memory-management board set with the Motorola MC68851 paged memory-management chip. The price of a 19-in. monochrome series 3000 with 4 Mbytes of memory has been cut from $11,900 to $5,990; a 15-in. color series 3000 with 4 Mbytes has dropped from $16,900 to $8,900.

Apollo also made it easier for personal-computer users to integrate with the Domain environment by introducing two software products. One is the Domain/PC Emulator, which runs MS-DOS applications on any Domain work station without the need for additional hardware. The other is Domain/PCI-Ring—a hardware-software communications package that connects a single personal computer to the Apollo token ring to allow distributed computing. The company will add a third package, Domain/PCI-Enet, later this year; it will connect a single computer to an Ethernet network. *–Larry Curran*

BELEAGUERED GCA SHOWS SIGNS OF RENEWED VIGOR

ANDOVER, MASS.

When GCA Corp. announced in early June that it had won an $8 million order from Rockwell International Corp. for several of its DSW 8500 direct-step-on-wafer cameras, it was the first good news in almost two years for the Andover, Mass., manufacturer of semiconductor-production equipment. Combined with the naming of a new chairman and chief executive officer at the end of June, the two moves are signs of renewed vigor at GCA. And that's good news as well for U.S. semiconductor manufacturers, who want to see GCA survive as an alternative to Japanese suppliers.

The new chief is David R. A. Steadman, former president of Raytheon Ventures, the venture-financing division of Raytheon Co. Steadman's move to GCA is viewed by some as prefiguring a possible sale of the company: he has been involved in several divestitures and acquisitions at Raytheon and elsewhere. GCA's president, Peter Simone, does not rule out that possibility, but he says the GCA board chose Steadman for his familiarity with the financial community.

FRAGILE. A leading maker of optical steppers, GCA was rolling along nicely in 1984 with revenues of $240 million, up 76% from 1983, and net income of $28.5 million, an increase of more than 200%. Then chip production plunged, and semiconductor makers stopped buying steppers. In 1985, GCA reported revenues of $156 million and a net loss of $145 million. The slide continued last year, although not as steeply: losses of $25 million on revenues of $123 million.

Simone hopes that the order from Rockwell indicates that the tide is beginning to turn. He quickly cautions, however, that "our recovery remains frag-

WINNER. Beleaguered GCA considers an $8 million order for DSW 8500 steppers a sign that the worst might be over.

ile, and will continue to be so until conditions in our industry improve."

GCA makes other equipment, but steppers determine its fortunes. They account for half the company's revenues and are the primary tool pitted against X-ray lithography in the battle to reach integrated-circuit line dimensions of 0.5 μm and less. The main competitor for GCA, which has a 35% market share worldwide, is Japan's Nikon Precision Inc., whose share is believed to be about 25%.

However, Rick Ruddell of Rudell & Associates, a Redding, Calif., market researcher who follows the stepper business closely, says that ASM Lithography, Tempe, Ariz., is coming on strong in the market. Ruddell also maintains that while GCA can win some short-term gains, the company's future "lies in being acquired. Potential buyers see [GCA's] installed base as an entrée into a global market."

GCA's comeback started under Richard Rifenburgh. Rifenburgh, a specialist in company turnarounds, was brought in as chairman, president, and chief executive officer in March 1986 to salvage GCA. He quickly set in motion the steps that preceded a financial-restructuring plan that was implemented this spring. The company shed three divisions, consolidated operations, and laid off 1,280 employees—cutting its payroll to 1,000.

At the same time, Simone, then a senior vice president (he succeeded Rifenburgh as president in February), and other members of senior management were laying the technology base to enable the company to benefit from its own recovery, and from any rebound in the market. "We set and achieved several goals, even though we were running out of cash. It's amazing what you can accomplish when your pants are on fire," Simone says.

GCA isn't out of the woods yet. The company's first quarter ended with revenues of $13 million and a $12 million loss, which Simone says resulted from customers' postponing orders until the restructuring plan was approved in March. He's buoyed, however, by continuing increases in semiconductor book-to-bill ratios, and by the fact that U. S. semiconductor manufacturers do not have much photolithography equipment that can produce lines finer than 1.5 μm.

GCA has developed a lens system for an excimer laser source for its steppers, to deliver the shorter wavelengths required for 0.5 μm. Simone believes that will keep optical lithography competing against X-rays. *–Larry Curran*

SOFTWARE

PLUG-IN SOFTWARE MAY SAVE BIG BUCKS

HIGHLAND HEIGHTS, OHIO

Computer hardware users take for granted the ability to tailor a system by mixing and matching boards that simply plug into a machine's backplane. Now Allen-Bradley Co. is out to match that flexibility in software.

With its eye on the factory-automation business, the company plans this summer to ship the first modules based on an ambitious new software scheme called the Software Backplane. Under development for three years, it is billed as a generic approach to factory-cell-control software: it will allow systems integrators to develop application packages as standard, portable modules that can be plugged in and played on the plant floor regardless of the host operating system employed.

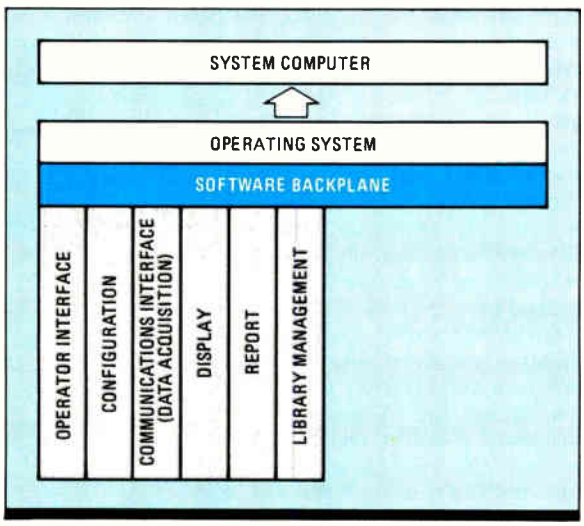
HALF THE COST. Because separate application packages won't be required for differing host systems, the approach could eventually halve the software-development costs of complex custom factory-automation systems, says Richard L. Eshleman, director of marketing at Allen-Bradley's Industrial Automation Systems Division in Highland Heights, Ohio. What's more, it could cut by 90% the cost of building systems based on a set of standard application modules, while also boosting software reliability and maintainability, he adds. The concept will be tested at "a large automotive customer site" starting this summer, and will be offered as a standard product next year, Eshleman says.

"For the high end of the cell-control business, the Software Backplane is our answer," declares J. Tracy O'Rourke, president and chief executive officer. The concept is a major piece of the firm's strategy to maintain a leading position in the cell-control business. That market is expected to grow by some 40% annually to total $1 billion worldwide by 1990.

As the name implies, the Software Backplane architecture is modeled after that of a hardware backplane. A hardware backplane combines a standard physical interconnect for the transfer of data with a protocol to manage those transfers; the Software Backplane is a software layer that provides a logical interconnect and a protocol for linking application modules to a specific computer operating system. The initial version will be for Digital Equipment Corp.'s VMS operating system.

Though yet to be proven, the concept is already drawing raves from some observers. "The potential for this is tremendous," says Daniel R. Kosmalski, division manager for Merit Systems Inc., a Troy, Mich., factory-software developer. Other vendors offer software tools designed to help isolate application software from changes and constraints in the host-system architecture, Kosmalski allows, but these tools are tied to specific hardware or operating systems.

"There are all sorts of different communication protocols like MAP [Manufacturing Automation Protocol] and Eth-



SOFTWARE BACKPLANE. With the Software Backplane, users will be able to plug in standard, portable applications packages.

ernet to transfer data between applications, but the communication between two applications isn't covered at all by the network protocols," notes Andrew Gray, supervising consultant at Coopers & Lybrand's manufacturing group in San Jose, Calif. By addressing that problem, Software Backplane could go a long way in meeting the needs of system integrators, he believes.

It contains four basic functions: a real-time distributive relational data base to meet the real-time needs of application modules; a director/arbitrator to manage and schedule resources; a conditional processor that reacts to user-configurable states within the data base to cause appropriate actions to occur; and system communications.

Allen-Bradley will initially supply six application modules for basic operation, and will then develop additional, more specialized modules. Users will also be able to develop their own application modules using C or other high-level languages. And Allen-Bradley hopes eventually to enlist systems integrators, computer vendors, and others to write standard application modules that can be plugged in. *–Wesley R. Iversen*

TEST

NEW KIND OF IN-CIRCUIT TESTER EMERGES

BOSTON

A new class of in-circuit board testers is emerging that could encroach on the low-cost market niche dominated by manufacturing-defect analyzers, which sell for $25,000 to $60,000. Three of the new testers were introduced in June at the ATE & Instrumentation Conference East in Boston.

Though they cost more money—from $50,000 to $95,000—the testers can double as manufacturing-process verification tools, offering more sophistication than the defect analyzer. The manufacturers—Hewlett-Packard, Factron/Schlumberger, and Zehntel—are heeding customers who find themselves increasingly squeezed between the need to get better control of their manufacturing processes and the escalating costs of board-test systems, which now are priced at $200,000 to $500,000 or more.

FEWER SLOTS. The HP 3065ST, at $95,000, offers similar performance at less than half the price of the first member of its 3065 family, which was introduced in 1983, says Jack Trautman, research and development manager at HP's Manufacturing Test Division in Loveland, Colo. The 3065ST has the same HP A400 multitasking central processor as the earlier family members, but has only six input/output slots, compared with 24 in its predecessors. Besides the computer, the ST also includes an 81-Mbyte hard-disk drive, a cartridge tape for back-up, an automatic-programming station and a test station, plus various system and test-oriented software. The software includes HP's Q-STATS program for data collection and statistical-reports generation.

Q-STATS, besides giving the greater sensitivity and resolution of a full in-circuit test system, makes the ST more effective than a defect analyzer in pinpointing manufacturing-process problems, says Mitch Killmon, an HP manufacturing specialist. For example, Killmon says, a conventional analyzer doesn't provide sufficient resolution to detect drift in the value of 1% metal-film resistors after a circuit board has gone through wave soldering. "An in-circuit tester like the ST will be able to pinpoint drift in those resistors that could indicate thermal shock during wave soldering which resulted from the failure of a preheating element," Killmon says.

Phillip Olson, senior sales engineer at Everett/Charles Test Equipment Inc., a supplier of defect analyzers in Rolling Meadow, Ill., doesn't directly contest Killmon's arguments about the need for greater resolution to truly diagnose component and process flaws. He stresses, however, that a defect analyzer is a niche product for cash-limited equipment manufacturers who may not do any board testing, whose board volumes are low to moderate, "and who don't want to tie up a million-dollar board tester to catch a lot of manufacturing faults."

Factron/Schlumberger's new entry is the Series 30/333V. The Latham, N. Y., company also makes defect analyzers, but Mike Esposito, director of marketing, says customers have been clamoring for more capability in a tester/analyzer that offers some of the Series 30 features at a more affordable price. The answer is the 30/333V. Esposito says it is the first of a family of process-verification tools that uses technology typical of much more expensive systems at less than half the price.

Price of the 30/333V ranges from $87,000 to $90,000, including 256 uncompromised hybrid test points, 25 Mbytes of hard-disk storage, a two-year warranty, and installation. It offers analog and digital in-circuit testing, and software that is compatible with all other Series 30 systems. The price was kept low partly by eliminating a high-speed section included in other Series 30 testers that performs complex functional testing. That move alone cut the board count from 75 in the 333E to 35 in the 333V.

BRAND NEW. Rounding out the trio are two models of Zehntel Inc.'s 1800, one of which the Walnut Creek, Calif., company is billing as the first to offer full analog and digital in-circuit testing for less than $50,000. Koorosh Nazifi, product manager, says the machines "are not stripped-down versions of our more expensive systems. They are brand-new testers designed to perform efficient identification and diagnosis of board-level construction faults."

One of them, priced at $49,750, provides 384 test points; the other covers 512 test points for $69,750. Both are based on the IBM PC/XT or AT, and all programming and test activities run under MS-DOS. The 1800 series does not include the functional digital or analog testing or VLSI microprocessor functional testing associated with board testers costing up to four times as much. However, it does provide the same in-circuit test features as larger systems.

Nazifi says the strategy behind the 1800 series reflects a split in the board-test market. Some companies are paring down products to test for process-related faults; others are adding functions to in-circuit testing, resulting in combination systems. "We decided to offer products at the low end," he says. *–Larry Curran*

TWO FOR ONE. This model from Zehntel is one of the new in-circuit testers that also does the job of a manufacturing-defect analyzer.

It's an issue that will be talked about for the entire year...

ASICs will take over 50% of the semiconductor market by 1995.

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The August 6th issue of Electronics

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- **What the traditional IC makers are up to in ASICs.**
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  New strategies and new design tools they're using to keep competitive. Is better customer service alone sufficient? Will they soon be offering their own standard parts? Must they merge to compete?
- **Profiles of the major players.**
  An examination of the tactics and strategies of both the large commodity IC manufacturers and the smaller niche companies.
- **What's new in related ASIC topics.**
  Coverage of ASIC testing, CAE tools, programmable logic devices, and users' views.

Ten *Electronics* editors from around the world will contribute their insight and worldwide perspective to this special issue.

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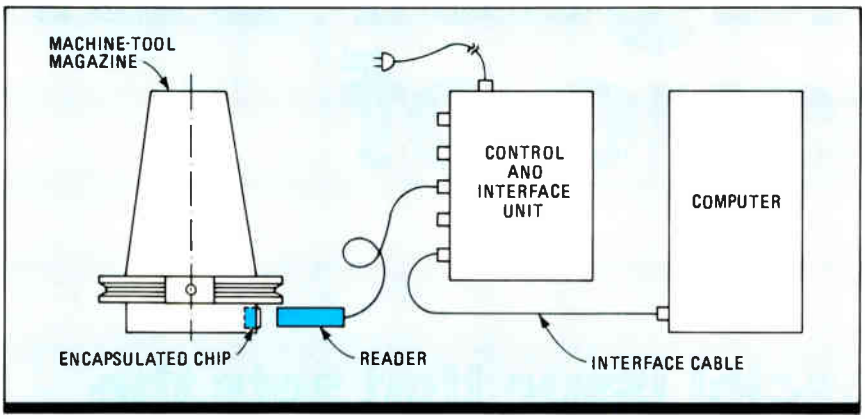
Electronics

BROOKTREE'S RF ID CHIP GOING BIGTIME



TOOL CHECKER. In this automated tool-changing system, the read head inductively picks up signals from the chip mounted on each machine tool to identify changed tools.

LOS ANGELES

A little-publicized group of programmable chips has quietly proved itself capable of filling a pivotal need in automated industrial production gear. Now the chips are on the verge of breaking into bigger markets.

The devices, dubbed radio-frequency identification chips by pioneering supplier Brooktree Corp., are now used to automate tool changing. They are a mix of on-chip logic, programmable read-only memory, and communications components whose job is to identify the right tool from among dozens in a holding magazine so the host computer can quickly direct its attachment.

They are permanently mounted on machine tools and periodically checked by an operator with an rf reading head whenever a tool change is needed. A signal transmitted to a computer identifies the tool in place. One of the biggest advantages is that no contact with the tools themselves is necessary; the chips can be pulsed at a distance by the rf head.

The devices appear to have a bright future. Topping the list of potential users is the military, says Matt Crugnale, of market researchers Crugnale and Associates, Mountain View, Calif. One idea under consideration is adapting the chips to keep up-to-date service reports attached to vehicles and weapons, he says. In civilian life, they could replace keys for security systems and could eliminate a weakness of smart cards: chips worn out from contact reading.

The chips need no on-board power source and can operate in grimy or electromagnetically noisy environments or from inside metal packages, where standard magnetic bar codes will not work. Also, their current memory size of up to 512 bits gives them better data-carrying capacity than bar codes. Crugnale adds: "They are unobtrusive [no contacts required], and you can put them into anything." The chips have been theoretically possible for some time, but only recently have design and process improvements made them practical. Prices vary, depending on application.

Two companies are making them. First into the market was Brooktree, the San Diego application-specific-IC house. It has supplied its chip for more than a year to Sensor Technologies GmbH, a company in Weinheim, West Germany, that builds a control system.

Among the machine-tool companies that build the system into their equipment are General Electric Co.'s Carboloy Systems Department and Kennametal Inc. They say that systems using the chip can change tools in as little as 12 seconds, versus the 30 minutes it takes manually.

Initially, Brooktree's n-MOS chips had fixed code. The newer ones are CMOS electrically erasable PROMs. Brooktree is willing to discuss its chip only in general terms, because it does not want to jeopardize a pending patent. The company's approach emphasizes "the effort to keep it simple and coherent," says Henry S. Katzenstein, vice president and chief scientist. A separate magnetic coil housed in the chip capsule picks up and reads the signals inductively. Katzenstein chose inductive transmission because it is both simple and most resistant to "the electromagnetic noise that pervades industrial environments."

Also in the market is Sierra Semiconductor Corp. of San Jose, Calif. It has a CMOS EEPROM-based chip that it sells to Allen-Bradley Corp., which uses it in a 1-by-3-in. circuit card. The card is used in a system that identifies large objects moving down an assembly line.

The Sierra chip, about 100 by 100 mils, contains amplifiers, oscillators, voltage regulator, high-voltage waveform shaping circuits, control logic and 512 bits of EEPROM memory. It operates on just milliwatts of power. Product engineer Joseph G. Nolan says it acts as the transceiver element on what amounts to a transponder board holding both a receive and transmit antenna, along with a number of high-frequency discrete components. Power comes from a 915-MHz microwave field in the reader. Writing the chip requires as little as 3 V; reading takes 1.5 V.

-Larry Waller

A TEST FIXTURE THAT DOES WITHOUT ALL THOSE WIRES

LATHAM, N. Y.

Under the neat face of an in-circuit tester's bed-of-nails fixture lies a massive network of wires. A fixture with 1,000 test nodes—and they can have far more—has 1,000 wires with 2,000 wire-wrapped connections linking the test probes to the tester's output connector. This massive clump of wires can slow circuit performance and cause cross-coupling; it is subject to wiring errors, and is extremely difficult and time-consuming to troubleshoot.

Now Factron/Schlumberger of Latham, N. Y., a major contender in the in-circuit testing field, has developed a simple but elegant method for eliminating the kluge of wiring under in-circuit test fixtures. In Factron's new Thinline wireless fixture, the interface board that formerly held a matrix of test probes, each with its own wire-wrap tail, has been replaced by either a printed-circuit card or a Multiwire card.

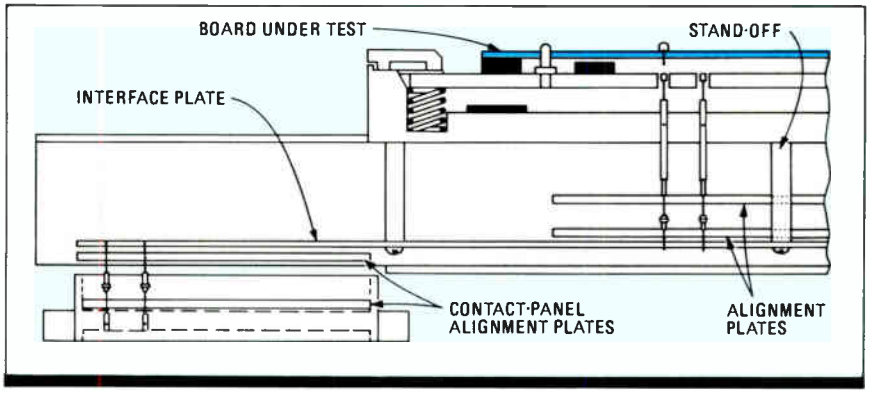
With pc boards, this kind of interface for the first time has a controlled repeatable environment, says Gary St. Onge, director of operations for Factron's Interface Products Division. Previously, pins were wired by hand with variations in length of wire, placement, and other specifications. With a board, all wiring is predetermined; the designer does not have to worry about how much

wire is used or where the wires will go. In addition, with a Multiwire interface board it is possible to have a board with a controlled or matched impedance. This will mean fewer propagation delays within the fixture as well as low cross-coupling.

There are other advantages to be gained as a result of the repeatability feature. For one thing, the printed circuit to be tested and the pc board to be used as a test fixture can be designed at the same time. For another, the use of pc techniques promises a faster process: one week rather than the three to four weeks needed to turn around conventional fixture interfaces. Finally, better control of the process means fewer wiring errors and simpler troubleshooting.

The setup is uncomplicated. On both the board types, push-on connectors soldered to the board mate with the test-contact panel posts. Printed-circuit conductors or multiwired connections run from these points across the board to a matrix of pins at the other end. The pins, in turn, are pushed onto connectors in a contact block.

Factron is evaluating pc-board versions of its wireless fixture and has multiwired versions on order. Tests to compare performance of the old and the new will start shortly. As for price, Factron figures that even though pc boards and Multiwire are more difficult to make than bed-of-nails fixtures, it can charge close to what the old ones cost because of economies of scale in manufacturing. *–Jerry Lyman*



ELIMINATING THE WIRES. Factron/Schlumberger's Thinline test fixture does without the tangle of wires that links test probes in today's fixtures to the tester's output connector.

POWER SOURCES

THIN PLASTIC BATTERY BENDS TO FIT

KELKHEIM, WEST GERMANY

If two West German companies are right, the layout and design of portable electronic equipment will start to change radically in the early 1990s. That is when these companies expect their flexible plastic battery to become a viable product.

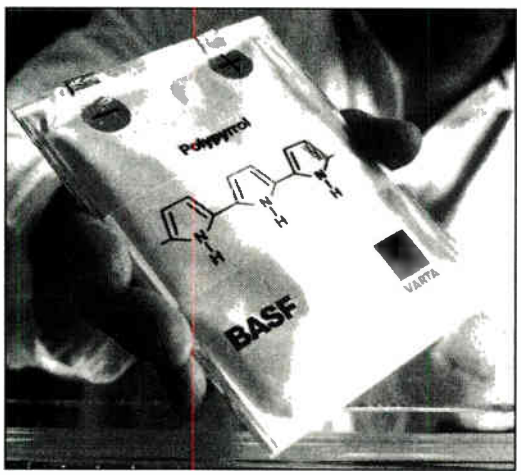
The two are developing the battery together. Varta Batterie AG is contributing its know-how in battery engineering, and BASF AG is lending its expertise in polymers. Designers will be able to gain space as well as freedom in arranging components by installing the postcard-size cells flat at the bottom of equipment. Or, since the cells can be bent just like cardboard, they can be formed to the contours of the equipment.

Varta, Europe's leading battery maker with $1 billion in sales last year, is discussing the final shapes of the polymer cells and their application with equipment makers, says Reinhard Gereth, who is responsible for research, development, and technical operations at Varta's research laboratories in Kelkheim, near Frankfurt.

The Varta-BASF cell uses polypyrrole for the positive electrode and lithium for the negative. The polypyrrole is a 50-μm-thick foil and the lithium 100 μm. In addition, an organic electrolyte, typically propylene carbonate with lithium perchlorate as the solute, is used.

The cell puts out 3.6 V under an open circuit and from 3.6 V down to 2 V under load conditions. The present laboratory versions come in two forms: with the electrode foils rolled into a tight cylinder the same size and shape as the familiar AA battery (50 mm long and 14.2 mm in diameter), or as a flat aluminum-covered sandwich 4 mm thick, about the size of a postcard and almost as flexible.

An electrical advantage is the cell's higher output compared with today's nickel-cadmium types, which put out only 1.2 V each. This means more voltage with fewer plastic cells. Also, at 20 to 30 Wh/kg, the gravimetric energy density of the Varta-BASF cell already matches that of the established NiCad type. And at its present state of development, the new cell can go through about 500 successive charge/discharge cycles, each at a 100% depth of discharge from the maximum 3.6-V value to the minimum 2-V level.



WRAPAROUND. The 4-mm-thick polymer cell puts out 3.6 V. It can be installed flat or wrapped around components.

Those values, after five years of work by Varta and BASF, lead Gereth to say: "We believe [we are] ahead of other companies working in the field," which includes Allied Corp. of the U. S., cooperating with Hitachi Ltd. of Japan, as well as Japanese car maker Toyota.

Nevertheless, he concedes that the figures are not high enough for a good commercial battery. For one thing, the energy density must be at least doubled; for another, the number of charge/discharge cycles must be raised to at least 1,000. Both can be achieved during the next few years, Gereth says.

The idea of the polymer battery dates back to 1977, when Alan G. MacDiarmid, a professor at the University of Pennsylvania, found that nonconducting plastic materials having conjugated double-bonding of carbon atoms can be made to conduct by electrochemical oxidation or reduction. The early U. S. researchers used polyacetylene as the active material, which proved to be chemically unstable.

At Varta and BASF, investigation of conducting plastics eventually led to polypyrrole, which is stable both in the air and in many organic electrolytes. This property, plus the fact that polypyrrole can be made in foil form, allows the development of an easily producible polymer cell. *–John Gosch*

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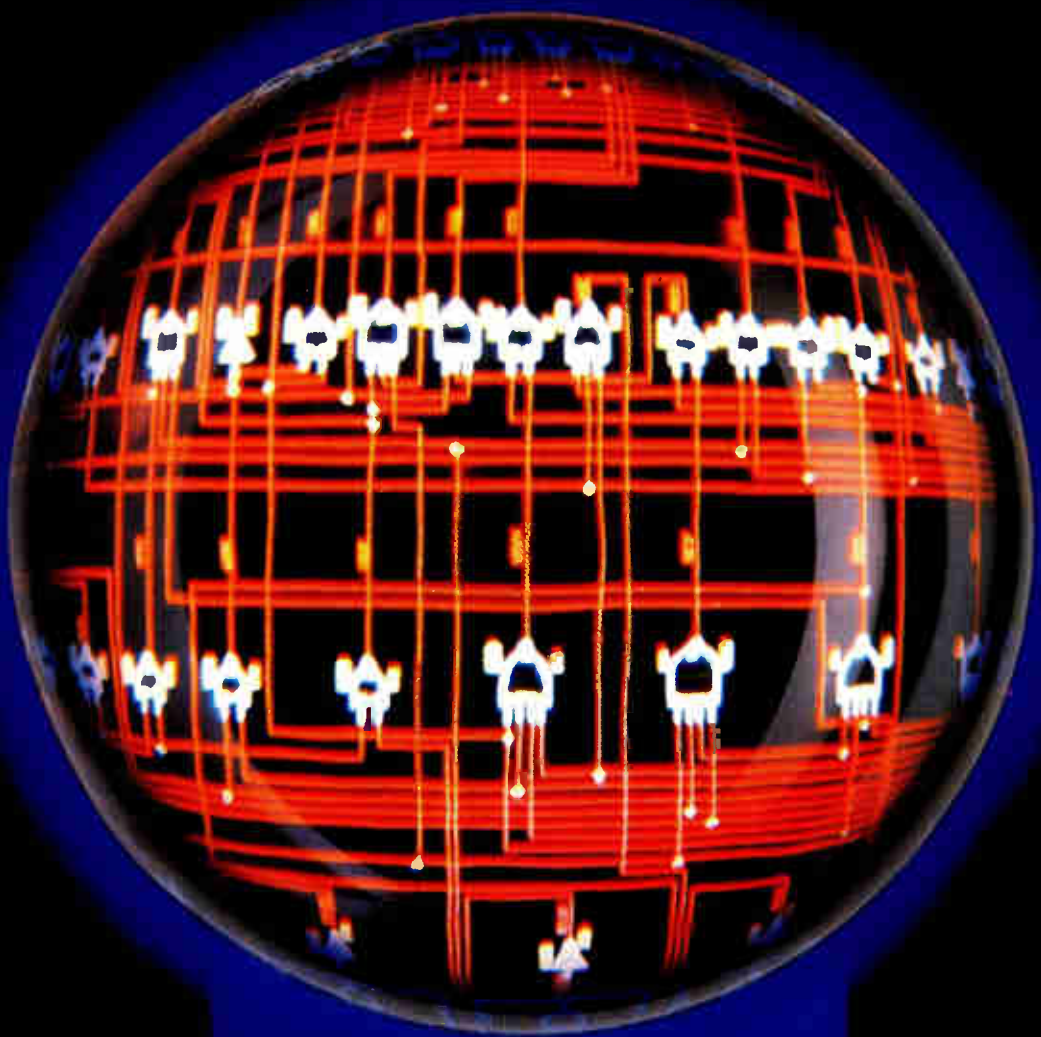

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PROBING THE NEWS

AT MIDYEAR, THE OUTLOOK SOFTENS FOR SOME MARKETS

BUT THAT SHOULDN'T STOP 1987 FROM BEING AN UP YEAR IN ALL SECTORS

Despite the rising wave of optimism coming from the semiconductor and computer businesses, the overall industry outlook for 1987 does not seem to be as strong at midyear as it was six months ago. While the semiconductor picture has brightened considerably, three other major industry sectors surveyed are not growing as fast as was forecast at the beginning of the year.

Those markets apparently weakening include computers, communications, and test and measurement instruments. The components business is holding to January expectations, but vendors worry that purchases are only for inventory. Even in semiconductors, there's a nagging worry that the rise is narrowly based, primarily on improving sales of personal computers.

SEMICONDUCTORS

Semiconductor executives are uncrossing their fingers to count up the good signs they see for the rest of 1987. Some even have that old-time optimism back and are prepared to enjoy the last half of what they see as a bona fide recovery year.

The signs are there—with a catch. Production is increasing slowly and steadily to meet three-year highs in book-to-bill ratios. And lead times are nudging longer on advanced technology components—as long as 20 weeks for Intel Corp.'s 16-bit 80286 and 32-bit 80386 microprocessors—as many personal computer makers attempt to match or top IBM Corp.'s new Personal Systems/2 line.

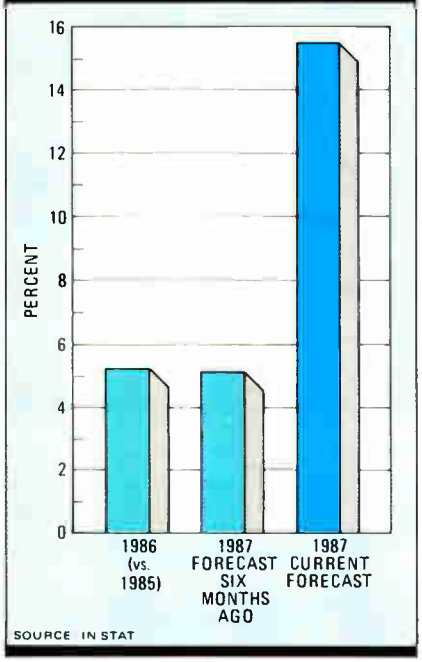
The result has been upgraded growth figures. For example, In-Stat Inc. of Scottsdale, Ariz., which in January predicted a 5.1% increase in growth for 1987, now says 15.5%. And Integrated Circuits Engineering Corp. has gone from 4% growth to 14% for the year. This brings them into line with the companies reporting forecasts for the January 1987 *Electronics* Market Report, where the consensus was 12% growth, reaching sales of $12.4 billion.

But the catch is that the growth can be traced to one market. "In the first half we've seen explosive growth fueled mostly by about 100 companies associated, in one fashion or another, with the making of [IBM] clones," says In-Stat's Jack Beedle. "If things continued to grow at the rate of the first half, it would be much, much bigger." Beedle worries that end-equipment demand will not keep pace, and he warns that the semiconductor industry could be once again fooled by the high expectations of personal computer makers.

"Déjà vu," he cautions. "We see nothing to sustain that kind of growth, except for the clone thing, which we feel could be a fizzler."

Nevertheless, optimists say, equipment makers are not just building inventory. "At computer houses, chips are going from the hand to the mouth—perhaps with just a plateful of chips in inventories instead of a cupboardful," says analyst Andrew J. Kessler of PaineWebber Inc. in New York, who notes that long lead times for 32-bit microprocessors are partly causing offshore personal-computer makers to delay expected orders on other ICs. Many hope memories and glue logic prices will come down when chip merchants begin to ramp up production, he adds.

U.S. SEMICONDUCTOR GROWTH



Because of the trade tariffs imposed on Japan, prices have risen. In the dynamic random-access memory market, 256-Kbit chips are going for $3 to $3.50 each at distributors, compared with only $1.28 to $1.50 in March, says Charles Clough, president of Wyle Laboratories. "Six months ago our largest competitor was the gray market, and that has dried up," Clough says. "I just hope Reagan hangs on to these sanctions."

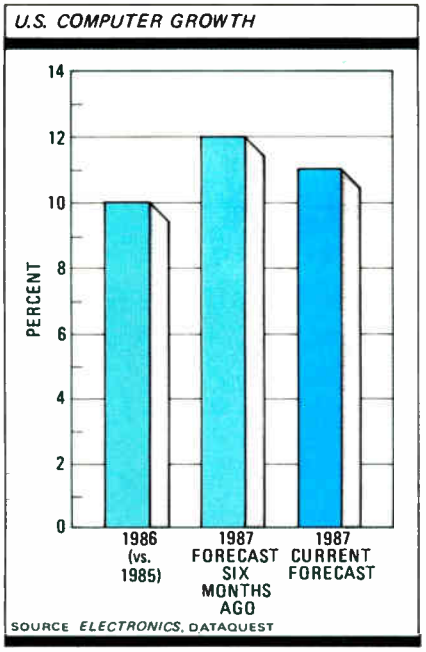
But many chip makers believe the jump in demand is real. "This is a consumption-driven recovery where we are not seeing wide speculation on the inventory side," notes Kevin McGarity, semiconductor vice president for U.S. marketing at Texas Instruments Inc. in Dallas. TI expects sales to climb, with U.S. market growth hitting 15%, assuming end-equipment shipments stay moderate.

Ben Anixter, vice president of corporate marketing at Advanced Micro Devices Inc. in Sunnyvale, Calif., says, "Are we concerned about the outlook? Yes, we are always concerned. But at least we can now see 90 to 120 days ahead of us and know what kind of business we will be doing. We think it is a real recovery, and it seems to be progressing along."

"We won't see inflated orders because we all learned a lesson from 1983 and 1984," says Larry Hootnick, senior vice president of corporate sales and marketing at Intel in Santa Clara, Calif.

COMPUTERS

At the halfway point, growth in 1987 in the computer and peripherals business looks a tad lower than it did six months ago. The outlook now is for 11% growth, down from the 12% industry consensus for the *Electronics* Market Report in January. *Electronics* and Dataquest Inc., the San Jose, Calif., market research organization, both have the computer and peripherals segment coming in at about $79 billion this year,



up from some $71 billion last year.

Most industry executives are finding more positive than negative signs amid general economic conditions that include increased capital spending, a dollar decline that should stimulate computer purchases in the manufacturing industries, and continued low inflation.

Of course, compared to the 20% growth rates of the late 1970s and early 1980s, 11% to 12% is anemic, and some executives are still more cautious than optimistic. The leading optimists are executives at companies positioned to exceed the industry's overall growth. One of those companies, Digital Equipment Corp. of Maynard, Mass., showed revenues up a rousing 25% to $2.4 billion in its most recent quarter. However, DEC's chief economist, James B. Whittaker, is holding to his original forecast for the industry: up 7% to 10% for the year.

The technical work-station and personal-computer segments appear to be coming back strongly. Apollo Computer Inc., the Chelmsford, Mass., provider of networked work stations, reported a robust first quarter. Revenues were up 50% from the same period last year, to $123.4 million.

At Compaq Computer Corp. in Houston, 1987 is shaping up as an excellent year. It's been so good to date, says Mike Swavely, vice president of sales and marketing, that Compaq has revised upward the forecast for the market segment the company serves—business computers sold through distributors and dealers—to 20% to 25% from the 15%-to-20% range.

The biggest player, IBM Corp., said at the end of June that it has shipped more than a quarter million units of the Personal System/2 line, which was introduced in April. It also expects its personal computer division to post record earnings for the year.

Joining the believers that a recovery is under way is James Bloom, executive vice president for marketing, planning, and operations at Honeywell Bull Inc., the company that emerged from the joining of the computer operations of Honeywell, NEC, and Groupe Bull. Bloom, who is located in Phoenix, says, "I have to feel that we're seeing a gradual but steady turnaround."

However, one tracker who isn't ready to subscribe to the turnaround theory yet is Gerald Kokos, executive assistant to the president and director of investor relations at Prime Computer Inc., Natick, Mass. He says his company met its first quarter plan, which resulted in a revenue increase of 13% over 1986 to $221.7 million. And while he says the second quarter is also on plan it isn't coming from market growth.

"While some prophets are saying we're in the midst of an upturn, we don't see that," he says. "We went into the year with a forecast that assumed 1987 would be similar to 1986, with no big upturn. We're saying we'll see more of the same in the second half" because of anemic capital-spending growth.

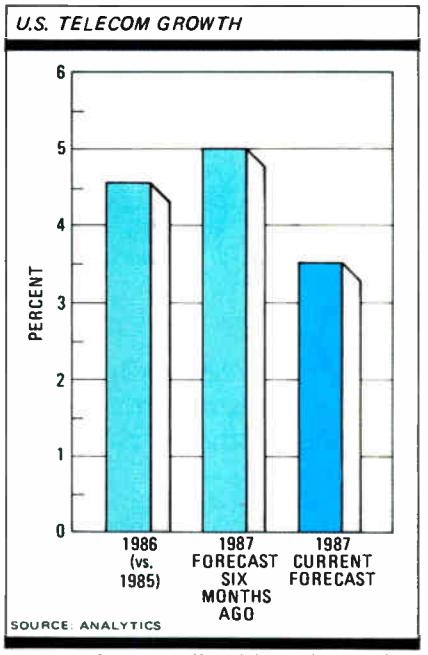
Industry standards and advanced technologies are fueling growth for the Technical Computer Operation at Hewlett-Packard Co., Cupertino, Calif. But Carl Flock, marketing manager there, isn't ready to jump on the turnaround bandwagon yet, either. "The industry has been doing a lot better, and while our situation has been good, I don't want to read too much into our experience."

COMMUNICATIONS

The picture for the U.S. telecommunications industry seems to be worsening. This year "is probably going to be the lowest-growth year for the communications industry" in the current five-year cycle, says Kent Webb, vice president of research at Analytics, a Palo Alto, Calif., market researcher.

Things were better in 1985 and '86, and they'll be better in 1988 and '89, he says. But for now, "we've reached bottom." Analytics has reduced its forecast of 1987 growth to 3.3% from the 5% it predicted in January, compared with the 7% foreseen by companies surveyed for the *Electronics* January 1987 Market Report.

The biggest damper for 1987 so far has been a disastrous first quarter, in which orders tumbled 11% to $16.837 billion, compared with the fourth quarter of 1986 when $18.943 billion in communications equipment was ordered in the U.S. That's unusual, Webb says, because orders usually pick up in the first quarter. "We pulled them [the yearly figures] down because the first quarter pulled them down," he says.



The big disappointment so far has been the lack of impact of the integrated services digital network. "ISDN certainly doesn't seem to have had any impact on total market growth yet," Webb says. That's despite AT&T Corp.'s assertion that "we continue to view 1987 as the year of ISDN."

Generally, there is a feeling of stagnation. "We are seeing a lot of indecision, and a lot of people are delaying [purchases] for various reasons," says Janet Boling, manager of strategic planning at Intecom Inc., a wholly owned subsidiary of Wang Laboratories Inc. based in Allen, Texas.

One insider in the PBX industry says times are hard and don't seem to be getting better. The PBX market, he says, has been nearly flat compared with 1986—and that figure was down from 1985. "There might be slight growth, but I think it will end up being pretty flat."

But all signs are not bad. Webb says inventories are shrinking, which is good news for equipment makers, who only recently started to really move their wares. So 1988 looks better, with growth hitting 8%. In fact, Dataquest predicts compound annual growth averaging 8.2% through 1992.

TEST & MEASUREMENT

Unless the market picks up substantially in the second half of this year, test and measurement sales in the U.S. may not even gain the low 3% growth, to $6.5 billion, now forecast for 1987. And this forecast is only half the

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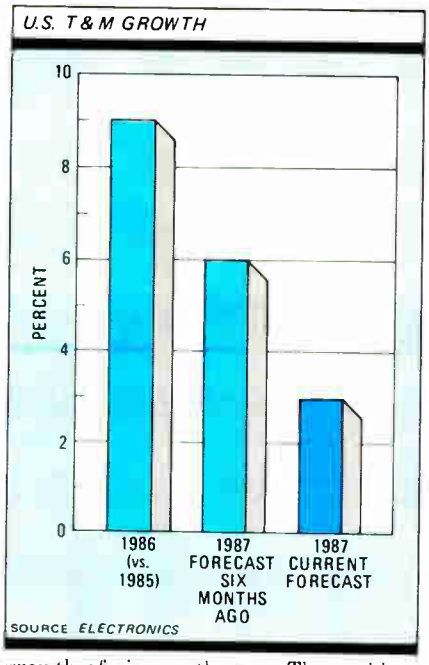


growth of six months ago. The problem has been flat capital spending and government buying. Only a continued rise in overseas sales has kept the industry from sliding into the doldrums.

In January the *Electronics* Market Report predicted that the 9% growth of 1986, which pushed total U.S. sales to $6.3 billion after a flat 1985, would spill over into 1987 and create a modest 6% growth to $6.7 billion. But leading manufacturers report the first half of 1987 almost flat compared with 1986's first half. Some market analysts say sales to semiconductor companies, computer manufacturers, and government—the biggest customers—will pick up in the last half of 1987. But these forces would all have to be unexpectedly large to push growth beyond 3%.

Hewlett-Packard, Tektronix, and John Fluke all say there has been little or no growth in the first half of 1987 for the U.S. market. In fact, an HP spokesman maintains the market has been flat since 1985. The Palo Alto, Calif., firm pegs the current level at around $7 billion.

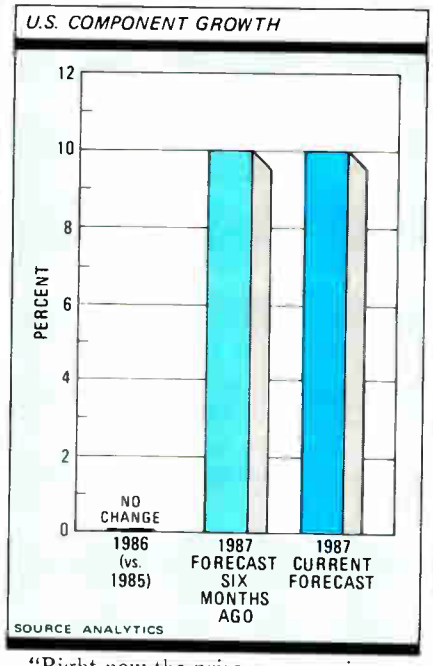
The trend looks similar at Tektronix Inc., Beaverton, Ore. New products have increased the firm's oscilloscope and logic analyzer sales, but declines in other product lines are keeping growth where it was three years ago.

At John Fluke Mfg. Co. in Everett, Wash., handheld meters and lower-cost bench instruments sold through distributors are having a good year. But this is because of new products and promotions.

Edward C. White Jr., electronics industry analyst at E. F. Hutton & Co. in New York, says the market is sluggish because semiconductor companies have cut purchases, computer companies are only just beginning a turnaround, and personal computers and instruments on cards are starting to displace standalone, benchtop instruments.

COMPONENTS

Manufacturers of components are not too cheerful at midyear. That's puzzling, considering that U.S. sales for 1987 are expected to increase about 10%, the same outlook that pervaded six months ago and up from no growth in 1986. The makers explain that the increase will largely be for inventory as customers buy now to avoid anticipated price increases. The consensus among companies surveyed for the *Electronics* Market Report was that 1987 would see a 7.7% increase, although some researchers such as Analytics in Palo Alto, Calif, were predicting then that growth would go as high as 10%.



"Right now the price pressure is enormous," says Peter B. Cherry, president of Cherry Electric Co. in Waukegan, Ill. "As many of the markets leave the U.S., the available domestic market is shrinking. That leaves more suppliers to slice up a shrinking pie, because in our industry so many companies are small or medium-sized, and for that reason have a domestic orientation."

The National Electronic Distributors Association warned in late spring that "there is no apparent fundamental rationale for any surge in component activity. What we are seeing is some order activity caused by an uncertain economic and political situation." Kent Webb, vice president of research at Analytics, agrees, crediting "inventory accumulation to avoid price increases" for the uptick. □

SILICON VALLEY PROFESSOR REDEFINES THE CRYSTAL BALL

Business forecasting and analysis in electronics sometimes seem to combine elements of science and witchcraft. But the practitioners have been working to change that; like the industry they watch, they have been devising more efficient and accurate ways to do their job. And, like the industry, some have been more successful than others.

One who seems to have found a better way, a marketing professor at Santa Clara (Calif.) University named Moshe Handelsman, has come up with a forecasting model that he says can accurately predict demand and major turning points in the semiconductor industry six months ahead. "I spent two years developing my model and tested it on 60 months of market data," he says. "It has been right 60 times, accurate within one month."


MOSHE HANDELSMAN

Handelsman, who was born in Israel 38 years ago and came to the U.S. in 1979, points to his forecasts for 1986 and early 1987 as a case in point. Countering the view of some analysts that 1986 would be a flat year, Handelsman predicted a continued decline until the end of 1986, followed by growth in the first part of 1987. That's the way it has turned out.

The major credit for that kind of forecasting, says Handelsman, is his data base. "I combine 20 to 30 written sources; I don't call up company presidents and ask them what they think. That's no way to get objective information." Each of those sources is an index in itself, says Handelsman. "I then combine them nonlinearly to get my overall index."

One commonly used indicator that Handelsman eschews is the book-to-bill ratio, which compares orders with shipments. "It's not accurate," he says. "It's more a reflection of history than a look at the future."

Apparently some people agree; Handelsman lists among his clients such companies as Advanced Micro Devices, Hewlett-Packard, and Intel, plus private investors.

Handelsman has a degree in industrial engineering from the Technion in Haifa and an MBA from Tel Aviv University. He received a doctorate in market research and econometrics from Purdue University, where he also taught.

What does he see happening next? "I predict a stagnant second quarter" is all he'll say. *–Howard Wolff*

MENTOR GRAPHICS PULLS AWAY IN ELECTRONICS CAD/CAE RACE

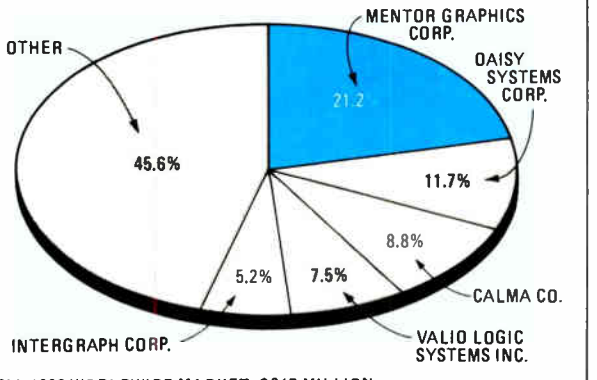
IT CLAIMS A MARKET SHARE LARGER THAN DAISY, TEK, AND VALID COMBINED

by Tom Manuel

The sweet smell of success permeates a group of buildings in a corner of Beaverton, Ore., where the people from Mentor Graphics Corp. hang out. The company is now clearly No. 1 in the new electronic design-automation industry, an industry it helped to create. Starting in 1981, the fledgling company produced an integrated system of applications for electronic design automation on a network of powerful work stations.

During the developing years of that market segment three major competitors emerged, battling for leadership—Daisy Systems, Mentor, and Valid Logic Systems. From 1983 to the end of 1985, Mentor and Daisy Systems Corp., running neck and neck, moved a length or two ahead of Valid Logic Systems Inc. However, in the first quarter of 1986, Mentor started pulling well ahead of the pack. Now it may be hard to dislodge Mentor from its strong position in the market.

MENTOR LEADS IN ELECTRONICS CAD/CAE SYSTEMS



TOTAL 1986 WORLWIOE MARKET: $817 MILLION

SOURCE: DARATECH INC., CAMBRIDGE, MASS.

Although the market for design automation in the electronics industry is large and growing, it has not been smooth sailing for all participants. Mentor's business and financial status is on solid footing, however. No matter how secure a leader's position may seem, though, its management must worry about what could go wrong—and Mentor's management is no exception. One never-ending discussion at Mentor addresses the question of what hardware platform its applications should be built on, taking into account the rapid pace of computer development.

Mentor is the only company in electronic design automation to get through the 1985-86 recession in the electronics industry without layoffs or losses, maintains Tom Bruggere, chairman and chief executive officer. Mentor's current market share exceeds that of Daisy, Valid, and Tektronix combined (whose 1986 market share were 11.7%, 7.5%, and 1%, respectively), according to Mentor. Daratech Inc., a Cambridge, Mass., research firm specializing in the areas of computer-aided design, engineering, and manufacturing, confirms that Mentor's share of the electronics segment of the market was 21.2% in 1986, with the nearest competitor, Daisy, trailing with 11.7% (see chart).

Mentor is also moving up fast to the upper ranks of the total design-automation market. By the end of 1986 Mentor had captured the No. 6 spot in the revenue rankings for the total market, which includes big segments for mapping and mechanical, architectural, and construction engineering. Based on current estimates from Daratech, Mentor should move up to the No. 4 slot by the end of 1987, passing GE Co.'s Calma Co. and McDonnell-Douglas Corp. Mentor's share of the 1987 overall market will be 4.7%, with an estimated revenue of $208 million, according to Daratech.

In its first five years Mentor rapidly grew into a $174-million company with $11 million in profits for 1986. At the end of the first 1987 quarter Mentor's revenues were running at a $202 million annual rate. Quarterly net hit a record $4,174,000, a 120% increase over 1986's first quarter. Revenues rose 36% above 1986 to $50,498,000. Mentor's success is not a domestic-only phenomenon, either: it has captured a whopping 70% share of the electronics segment of the CAE/CAD market in Japan, for example.

Among the key corporate goals that Bruggere and Jerry Langeler, president and chief operating officer, have set out for Mentor is growth of 25% each year. "I see nothing to prevent Mentor from becoming a $1 billion company," says Langeler. "We think we have the management structure in place to grow to $1 billion. We have strong organizations in each critical area. But execution is what we have to watch most critically."

In a company on an sustained upward growth spiral, management cannot avoid thinking about where things could go wrong. Right now, Langeler and Bruggere worry less about their competitors than they do about what could happen internally. "There isn't anything a competitor can do that is worse than what we could do to ourselves," says Langeler.

"If we were to stumble on the implementation of the second generation of some products," says Bruggere, "that would hurt us." He is concerned about "the possibility of hurting a software product with future releases, or not getting a new product out on time."

But the management at Mentor is not myopic, either. Bruggere and Langeler still keep an eye on competitors. And Langeler points out that there is always the possibility that a fundamental structural change in the industry could occur. For example, he says, "The perceived value of a product that Mentor is offering could change out there while the cost of delivering it doesn't—that is a real problem."

From the start, Mentor's mission has been to help electronics companies improve their product-development process. The six major application areas that the company has identified include CAE and CAD, as well as computer-aided test, electronic packaging, publishing, and software engineering. The company has many application programs in its product line in each of these areas, except for computer-aided software engineering. "We don't know what [CASE] is yet," says Langeler.

Mentor currently has no plans to enter markets other than electronics. Electronic publishing, through its subsidiary Context Inc., is as far from conventional electronics as Mentor will go. Publishing design documentation is also important. "We see more than enough business in this [electronics] segment to

grow the company to the size we anticipated," says Langeler.

Some industry observers feel that design automation companies can blame some of their difficulties on offering their software on the wrong work stations. Users, they say, want industry-standard platforms so they can use standard applications for tasks other than design work.

Vendors that started with proprietary work stations have suffered big losses, and most of them are now adapting their software for use on other work stations. But supporting multiple platforms is expensive. Langeler has two

BRUGGERE

LANGELER

empirical observations about this: "Companies that port existing applications die, and companies that support multiple platforms are not successful."

However, there is the question of what is a standard platform. Some would say that a system running under the Unix operating system and tied to an Ethernet network with a standard high-level protocol and network-wide file system, such as the systems offered by Sun Microsystems Inc., is an industry standard. Others say that Digital Equipment Corp.'s VAX series and the IBM Personal Computer architecture can claim to be industry standards, too.

Mentor has chosen and stayed with the Domain network and work-station system made by Apollo Computer Inc. Some observers call the Apollo system proprietary; they say that Mentor will eventually have to adapt its software to run on standard platforms.

Not so, says Langeler. "You have to be on the right platform or *a* right platform. Apollo is *a* right platform." A company cannot successfully be on two or more platforms at once, he says. "If you try to be on multiple platforms, you concentrate too much effort on the platforms—and your applications may be equally mediocre on all platforms."

Mentor's management agrees that the company has to be prepared for a massive move to another platform if Apollo stumbles or if a much better platform comes along. Apparently they do not think that either will happen in the near future, because Mentor has recently placed a $100 million order with Apollo for systems over the next 18 months. □

INTERNATIONAL NEWSLETTER

PHILIPS BESTS THE JAPANESE WITH ITS 1-Mbit STATIC RAM...

For the moment, the new speed and power record holder in the 1-Mbit static-RAM race is not from Japan—it's Philips of the Netherlands. The company says access time for the first working samples of its 1-Mbit CMOS static random-access memories is just 25 ns at 20 MHz. And dissipation is just 150 mW at 20 MHz during operation and less than 5 μW on standby. At this year's International Solid State Circuits Conference, Sony topped the list of 1-Mbit SRAM introductions with a chip that boasted a 35-ns access time at 100 mW. The Philips chip sports 0.7-μm minimum feature sizes and packs 128,000 8-bit memory locations onto a 94-mm^2 chip, making it the densest SRAM to date. Volume production is expected to begin in mid-1989. The Philips chip's small appetite for power should make it ideal for portable consumer equipment and battery-powered office systems. The development is part of the billion-dollar Mega Project, a joint effort by Philips and West Germany's Siemens AG to become top VLSI producers. □

...BUT SIEMENS ADMITS TO BIG PROBLEMS IN BUILDING ITS 1-Mbit DRAM

Siemens AG is having problems getting its 1-Mbit dynamic random-access memories to market. In a surprising display of candor, the Munich company admits that although deliveries were originally scheduled for the first half of 1987 [*Electronics*, Nov. 13, 1986, p. 30], it now has no firm idea when shipments will start. The 1-Mbit DRAM is one part of the Siemens-Philips joint memory effort, the Mega Project. The setback began when equipment Siemens needed for the new 1-Mbit fab line arrived late, but the situation appears to have worsened. The company now says that "still unsatisfactory yields and quality" are to blame for the delay. Company insiders say the problems may be due in part to the unproven equipment for handling the 6-in. wafers Siemens is using for the DRAMs. However, Siemens expects its integrated-circuit business to grow at more than a 10% clip this year, reaching about $440 million. □

FROM CANON AND INTEL, A CHIP THAT CONTROLS 10 FUNCTIONS AT ONCE

Canon Inc. and Intel Corp. are jointly developing an application-specific microcontroller around an Intel 80C51 core that will be capable of controlling 10 processes at once. The 80C51 will act as a supervisory unit at the center of 10 peripheral processing units, which will provide the equivalent of 10 controllers operating in parallel. Intel will fabricate the device in its CHMOS III process, and the two firms are negotiating to give the U. S. chip maker the rights to worldwide sales. Although the initial application is for an office photocopier, the chip is applicable to a wide variety of uses in office equipment and other electromechanical systems. □

SEIKO EPSON COLOR LCDs MAY REPLACE CRT DISPLAYS IN BOEING 7J7 JET

Seiko Epson Corp. is developing a color liquid-crystal display for use in the cockpit of Boeing Corp.'s next passenger jet, the 7J7, which is scheduled to make its first flight in 1990. Seiko Epson, of Suwa, Japan, is working with Rockwell International Corp., Pittsburgh, Pa., on the cockpit display systems for the jet, and they expect Boeing to adopt their design. Seiko Epson chose polysilicon thin-film-transistor technology for its color LCDs. The LCDs are better suited to the cockpit environment than conventional cathode-ray tubes, the company says, because LCDs use less power, do not wash out in bright sunlight, and take up less space than a comparable CRT. Seiko has not disclosed the dimensions of the new display, but the panel is believed to measure 7-in. square. □

INTERNATIONAL NEWSLETTER

A NEW PC FROM JAPAN IS COMPATIBLE WITH BOTH IBM PC AT AND NEC MACHINES

The first personal computer that is compatible with both IBM Corp.'s PC AT and NEC Corp.'s PC-9801—the most popular personal computers in the U. S. and Japan, respectively—is about to hit the market. Proside Corp., of Chiba, Japan, plans to sell a double-compatible model beginning next month. NEC may have something to say on the matter, however. The first company to try to clone the 9801—Seiko Epson Corp. of Suwa, Japan—met with strong opposition from NEC, which went to court to try to block sales of the computer [*Electronics*, May 14, 1987, p. 49]. NEC claimed Seiko Epson infringed on software copyrights, but Seiko ducked the controversy by bringing out a machine with a modified operating system. Proside says it is confident that its new PC will not infringe on NEC's copyrights. The company was set up earlier this month by Takayoshi Shiina, the former president of Sord Computer Corp., also of Chiba. Proside will make the double-compatible PC at its Hong Kong factory, which has been shipping a PC AT-compatible machine since June. □

JAPAN WILL BUILD A SYNCHROTRON FOR X-RAY LITHOGRAPHY

Japan will begin building an experimental synchrotron orbital ring for X-ray lithograpy in January. The synchrotron, built around a superconducting electromagnet, will be assembled in Tsukuba, Japan, at the Electrotechnical Laboratory of the Agency of Industrial Science and Technology, under the guise of the Ministry of International Trade and Industry and Sumitomo Electric Industries Ltd., of Osaka. The new synchrotron, which will have a 4-m-wide orbital ring, will use technology developed by the Electrotechnical Lab that increases the exposure area while maintaining a resolution of less than 0.25 μm [*Electronics*, March 17, 1986, p. 49]. The system should be completed by October 1988. IBM Corp. is acquiring a similar ring—becoming the first U. S. company to do so—but doesn't expect to have it operating before 1990 (see p. 112). □

THIS OPTICAL FIBER TRANSMITS A 5-GIGABIT/S SIGNAL 90 Km WITHOUT REPEATER

Using a dispersion-shifted glass fiber, researchers at West Germany's Standard Elektrik Lorenz AG have built an experimental optical communications system that can transmit data at 5 gigabits/s over 90 km—without needing a repeater to amplify the signal. The secret is in the fiber, the Stuttgart researchers say. Using a special doping profile in the glass, they found they could raise the minimum wavelength dispersion from 1,300 nm to 1,525 nm—nearly identical to the fiber's attenuation minimum wavelength of 1,550 nm. In conventional fiber, where the dispersion and attenuation minimums are vastly different, users must choose between maximum bit rate and maximum transmission distance. SEL says its new fiber eliminates the choice. The 5-gigabit/s data rate would allow the simultaneous transmission of 78,000 telephone channels or 36 high-quality TV pictures. □

WEST GERMANY FINDS A CRACK IN JAPAN'S TELECOM MARKET

Japan's telecommunications market may be tough, but it appears that at least one Western company has figured out how to play in that ballpark. In an unusual twist, West Germany's Telenorma has signed Tokyo-based Mitsubishi Corp. to market its communications equipment in Japan. Telenorma, part of the Robert Bosch Group of companies, predicts its annual Japanese sales could surpass $10 million in the next few years. The equipment involved includes automatic-call distributor systems, terminal exchanges, and dealer systems for calling up stock-market figures. What's next? The companies are now talking about marketing the equipment in other Far Eastern countries. □

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INTERNATIONAL WEEK

IC CARDS GET BIG TRYOUT IN JAPAN

A large-scale, multipurpose smart-card experiment will be started in October by 50 Japanese companies affiliated with the Sanwa Bank, Japan's fifth largest bank. The card will have numerous functions, ranging from banking, cashless shopping, auto-dialing for phone calls, and identification, to use as a substitute for hotel keys, a manual for office-automation equipment, and a data card to identify private bottles kept by customers in restaurants and bars, says a spokesman for Sanwa Bank. Cards will be fabricated by Dai Nippon Printing Co. using Hitachi chips. Meanwhile, the Federation of Bankers Associations of Japan is working on standards for smart cards so that they can be used at all banks.

SONY DELAYS SALE OF 8-MM CAMCORDER

Yield problems with a $^2/_3$-in. charge-coupled device imager have forced Sony Corp. to postpone the release of its 8-mm camcorder from June 21 until late August. The sensor has proven more difficult to manufacture than expected: Sony says tiny dust particles have kept yields too low for mass production. The high-resolution CCD imagers, which feature 330,000 pixels, are built at Sony Kokubu Semiconductor Corp., in Kokubu, Kagoshima. Sony Kokubu started shipping samples earlier this month. Sony's current line of 8-mm camcorders uses a lower resolution $^2/_3$-in. CCD imager with 250,000 pixels.

KU-BAND SATCOM TEST IN JAPAN

Japan's Ministry of Posts and Telecommunications will start a one-year satellite-communications experiment in July using the 11- to 18-GHz K_u-band, which has never been used for Japanese satellite communications. The experiment will be performed in cooperation with Kokusai Denshin Denwa Co.—Japan's overseas monopoly carrier—and two satellite-communications service firms using a satellite launched by International Telecommunications Satellite Organization. The two Tokyo firms, Japan Communications Satellite Company Inc. and Space Communications Corp., plan to start domestic data-communications operations in 1989 with satellites purchased from Hughes Aircraft of Los Angeles and Ford Aerospace and Communications of Palo Alto, Calif., respectively.

PLESSEY PULLS OUT OF ALVEY PROJECT

Plessey plc of London is pulling out of one of the most prestigious and well-funded Alvey projects—developing a computer system to understand continuous human speech—that was only an estimated two years away from completion. The project now appears in danger of being scrapped unless the other major partner, GEC Research Ltd. of London, puts in extra funding to make up for Plessey. Plessey dropped out after failing to raise £5 million of venture capital to help fund the project—even though it was announced last month that Plessey's own cash surplus has jumped from £77 million to £269 million in the last year.

YASKAWA TO SELL U. S.-BUILT COM LINK

Yaskawa Electric Manufacturing Co., of Kitakyushu, Japan, a motor and robot manufacturer, will market the bus-based link system developed by Flavors Technology Inc. of Amherst, N. H., in Japan starting July 21. The system, Bus-Link, integrates a superminicomputer and an artificial-intelligence machine for real-time numerical and AI processing. Flavors claims Bus-Link is 100 times faster than an Ethernet network. This will be Yaskawa's first stab at marketing computer-related products. The company, which owns a 20% interest in Flavors, hopes to sell 10 units of Bus-Link, at 4 million to 5 million yen each, during the first year.

PHILIPS, SIEMENS IN SWISS PHONE DEAL

Switzerland's postal authorities have placed an order with Philips and Siemens AG to install a mobile telephone network, mainly for cars, in the western part of the country. The network, part of a system which will cover the whole of Switzerland by 1990, will be ready by next June. Siemens will deliver the antennas, and Philips will provide the base stations. The full value of the order has not yet been determined.

EC-WIDE PRODUCT GUARANTEE BY SONY

Sony Corp. of Japan has become the first multinational firm to offer product guarantees that are valid throughout the 12 countries of the European Community. This means that consumers can buy Sony equipment in one country and have it serviced and repaired in any other EC country. Sony's move is the first tangible result of a Common Market campaign aimed at persuading multinational companies that operate in Europe to offer EC-wide guarantees for their products.

GERMANY EXPANDS OPTICAL-FIBER USE

The Bundespost, the agency that runs West Germany's communications lines, plans to install a total of 900,000 km, or roughly 560,000 miles, of optical fibers during the next five years. That will make the country Europe's biggest market for optical fibers. A spurt in consumption will come from the use in short-haul phone networks operating at 140 Mbits/s over monomode fibers.

TOSHIBA AND SHARP FREEZE PC EXPORTS

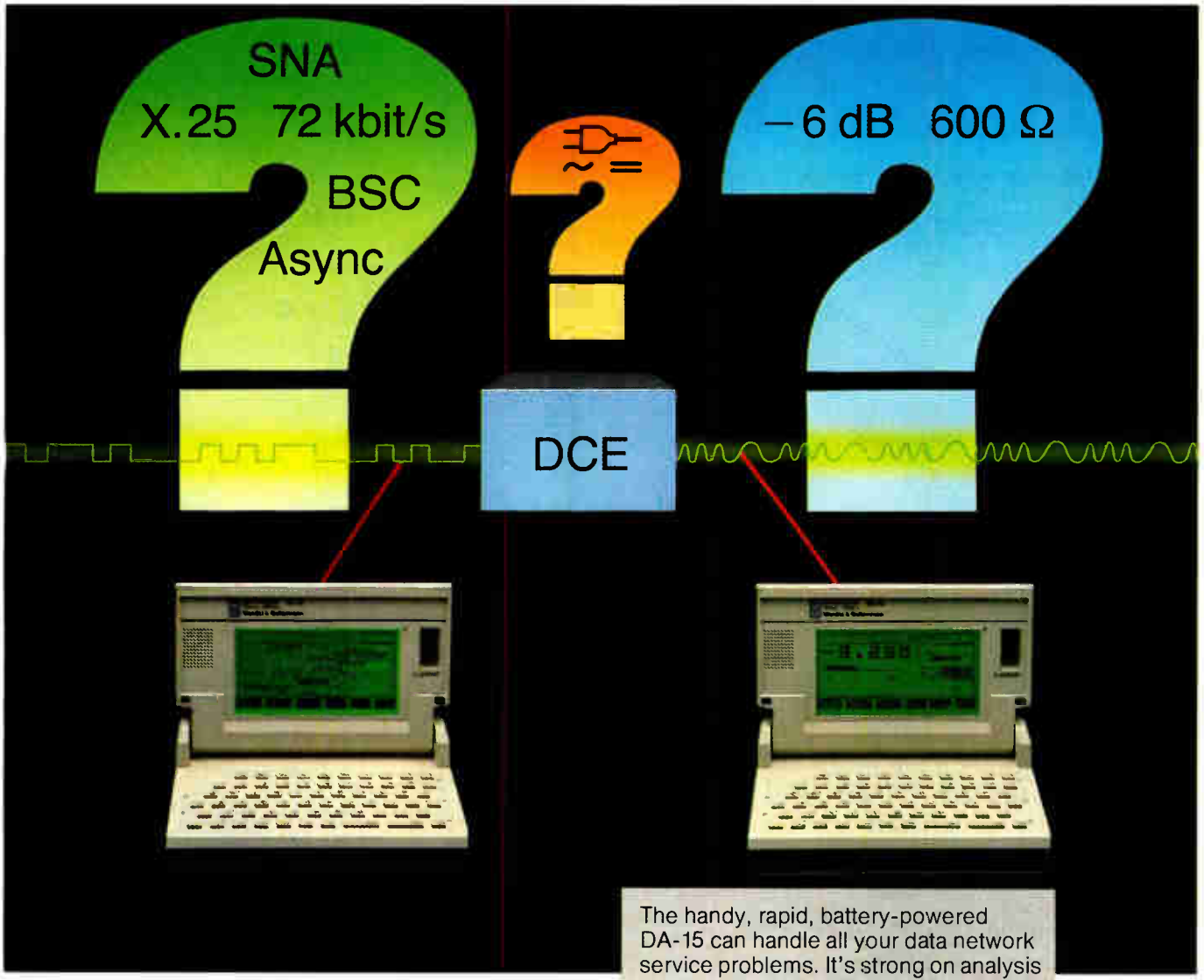
Japan's Toshiba Corp. and Sharp Corp. want to voluntarily limit personal-computer exports to the 12 European Community countries to avoid having to pay penalty duties on their products. Toshiba shipped 12,000 units and Sharp shipped 3,000 to the EC during the first three months of this year. The two want to freeze EC exports at those quarterly levels.

NIXDORF TO START SINGAPORE R&D

Nixdorf Computer AG, West Germany's No. 2 computer maker, has earmarked 30 million deutschmarks, or $16.5 million, for a research and development center in Singapore. To be staffed with about 50 engineers, mainly from Singapore, the center will concentrate on developing internationally applicable user programs for Unix-based computer systems. The Singapore facility augments Nixdorf's R&D activities in West Germany and at technology centers in the U.S. and Japan. The Paderborn company already employs about 600 people in Singapore, in sales, marketing, and production.

GERMAN FIRM TO OPEN IRISH PLANT

Stribel GmbH of Frickenhausen, West Germany, an automotive components company, will spend £2.5 million on a new manufacturing facility in Dundalk, Ireland. The factory will employ 72 people over the next three years and will produce press and injection molding tools. The number of employees will rise as the factory begins making electronic and electrical parts for the auto industry.



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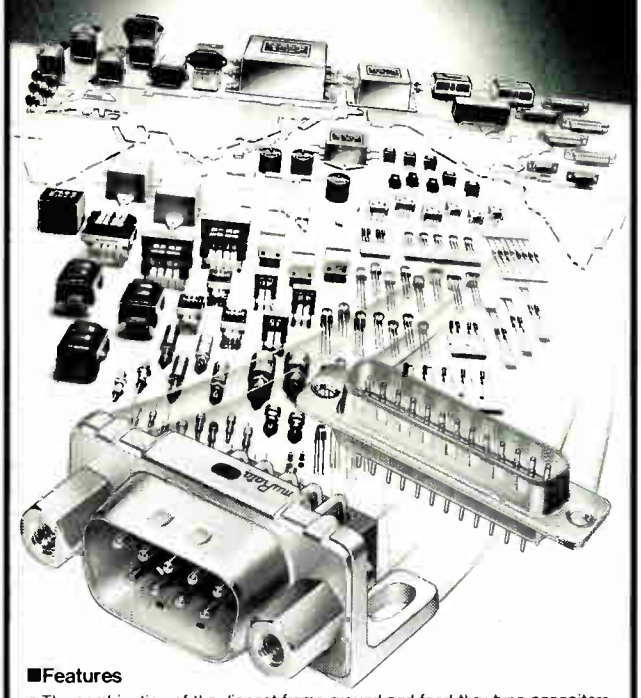

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Insulation Resistance	1000MΩ min.

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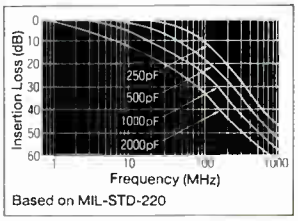

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INTERNATIONAL PRODUCTS

PHILIPS'S ADVANCED CMOS LOGIC BACKS TI'S NEW PINOUT SCHEME

1-MICRON PARTS RIVAL FAST BIPOLAR FOR SPEED AND DRIVE

By adopting a new pinout scheme in its 1-μm Advanced CMOS Logic family that rivals the speed and drive capability of the best TTL parts, Philips of the Netherlands has also achieved a threefold decrease in system noise, which reduces data-integrity problems encountered in high-speed switching.

With its ACL family, Philips has lined up with Texas Instruments Inc., Dallas, in the industry-wide pinout controversy. Philips and TI pioneered the new pinout, which moves voltage supply and ground pins from the corners to the center of dual in-line packages. It also adds a ground and supply pin for every pair of outputs, which means a 16-pin conventional DIP is replaced by a 20-pin part. TI introduced its first ACL parts in May [*Electronics*, May 14, 1987, p. 126].

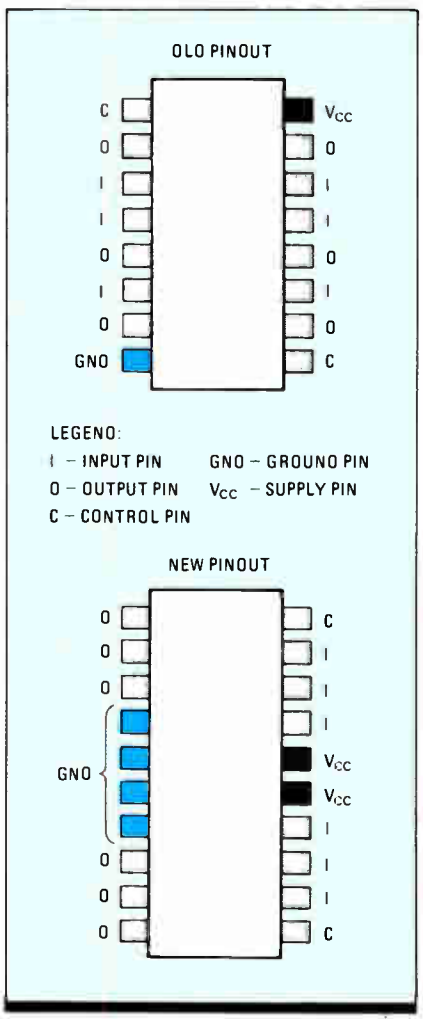
SWITCHING NOISE. Chip-to-pin lead lengths between the supply terminals play a major role in noise generation. Standard pinning maximizes lead length—and inductive noise—by placing supply and ground pins at diagonally opposite corners of the package. This creates problems in high-speed switching—lost data in internal flip-flops, extensive delays, poor noise immunity, and momentary changes of logic states.

Philips's parts, with their shorter lead lengths, avoid those problems. In a 14-pin DIP, for example, inductance drops from 10 nH for conventional pinning to 3.5 nH. Corresponding figures for a 24-pin package are 18 nH and 4 nH. Noise is cut threefold, from 2.5 V for a conventionally pinned device to around 0.8 V for an ACL center-pinned part.

The parts have an average propagation delay of 3 ns at a typical 150-MHz operating frequency and a 24 mA output—enough to drive 50- and 75-Ω terminated transmission lines, says the Dutch company.

Because the new pinout adds a ground and a supply pin for every pair of outputs, package size increases by about 10%. Better board design can compensate for this drawback.

The new pin arrangement "is the first attempt to bring the old-fashioned pinning for logic circuits in line with modern high-speed technologies," says Ad de Pagter, international product marketing manager for CMOS ICs at Philips's Electronic Components and Materials Division in Eindhoven. "With center-pinning, we know we are fighting a popular concept, but I think Jedec [the Joint Electron Device Engineering Council] will accept it as an alternate solution. In the end, the new configuration will win out."



CHANGES. Philips moved ground and supply pins to the center and added a ground and supply pin for each pair of outputs.

Many chip makers, notably in the U.S., oppose breaking away from two decades of packaging standards because doing so requires a different board layout. They argue that good design and, in the long run, greater use of surface-mount packaging will solve the problem of noise.

Philips contends that to exploit the speed potential of fast logic circuits, designers must use transmission-line techniques that require new board designs anyway. So obviously, says de Pagter, it is best to design ICs with the best pinning for high-speed ACL technology.

That technology should grab a big chunk of the logic market, Philips believes. According to market researcher Dataquest Inc., San Jose, Calif., TI and Philips together commanded one third of worldwide logic-device sales last year—$960 million of a total of $2.85 billion.

"ACL will spell an increase beyond the one-third level for the two firms," de Pagter predicts. By 1990, he thinks Philips will sell some $50 million worth of ACL parts worldwide.

CMOS PROCESS. The new family is based on a twin-well CMOS process with recessed local oxidation and a self-aligned titanium disilicide layer on the source, drain and gate areas. This reduces contact and interconnect resistance. Capacitance is reduced by oxide gate sidewall spacers.

With the effective transistor gate length just 1 μm, the on-chip propagation delay checks in at only 0.5 ns. The use of copper-doped aluminum interconnects on a tungsten layer minimizes electromigration. A p-epitaxial layer on a low-resistivity p-substrate makes the ACL family virtually latch-up free.

The typical quiescent power dissipation of an ACL gate is about 2.5 nW, roughly six orders of magnitude less than a bipolar gate. Dynamic power consumption is 0.18 mW at 100 KHz with a 50 pF load and a 5-V supply and increases to 180 mW at 100 MHz.

The parts also feature electrostatic discharge protection against positive and negative transients up to 2 kV on all inputs and outputs. The standard operating temperature range is from −40° to +85°C. A wider range, from −55° to

+125°C, is available as an option.

The first devices consist of a dozen various NOR and NAND gates as well as flip-flops. By the end of this year there will be 35 types, and by the middle of 1988 the total will grow to 103 parts. During the second half of 1988, an additional 45 types will be released. Volume production of the first parts will start at Signetics Corp., which is a Philips subsidiary situated in Sunnyvale, Calif., next year.

TWO TYPES. The devices come in two basic versions. The 74AC types have CMOS-compatible input switching levels and a 2-V to 5.5-V supply. The TTL-compatible 74ACT types have a supply of 5 V. Both versions are available in DIPs and in the Philips-pioneered small-outline packages for surface-mounting.

Philips's first twelve ACLs are the 74AC/ACT11002 quad 2-input NOR gate, the 74AC/ACT11020 dual 4-input NAND gate, the 74AC/ACT11027 triple 3-input NOR gate, the 74AC/ACT11030 8-input NAND gate, the 74AC/ACT11074 dual D-type flip-flop with set and reset, and the 74AC/ACT11240 octal-buffer line driver. Philips and Signetics developed the ACL family with TI, and the two companies' ACL families are completely pin- and function-compatible.

The Philips/Signetics prices are in line with those of the TI parts. Depending on type, the ACL family members range in price from 0.7 to 3 Dutch guilders apiece for design-in quantities.

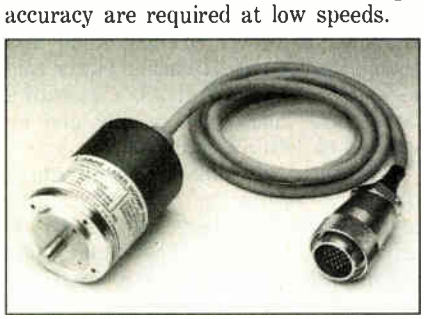
– John Gosch

Philips Elcoma, P. O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone 31-40-722091 [Circle 500]

ROTARY ENCODER USES LASER BEAM

The R-2A rotary encoder from Canon Inc. uses the interference of diffracted laser light and a fine-patterned-grating disk to produce 81,0000 signal pulses/s. Its positioning accuracy is better than 20 arc-sec.

Small enough to be used in each axis of movement in a robot arm, the encoder has an outer diameter of 36 mm and a length of 48 mm. It weighs 75 g. Other applications include scientific measuring equipment and surveying equipment where smooth shaft rotation and high accuracy are required at low speeds.



The encoder runs on ±5 V at a maximum supply current of 200 mA. Maximum permissible radial shaft load is 0.4 kg. Its light source is a semiconductor laser with 780 mm wavelength, 5 mW maximum power output, and a 200,000-hr life cycle.

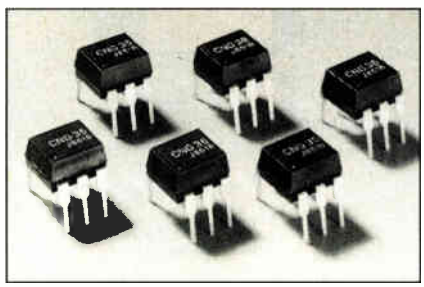
The R-2A encoder is available now. It costs 180,000 yen. Delivery takes approximately two weeks after receipt of order.

Canon Inc., 2-7-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 163, Japan.
Phone 81-3-348-2121 [Circle 702]

OPTOCOUPLERS BOOST PERFORMANCE 5-FOLD

A series of gallium aluminum arsenide infrared optocouplers from Philips boasts high current-transfer ratios at low input currents and outperform similar gallium arsenide devices by a factor of five.

The CNG35, for example, has a 0.5 current-transfer ratio when driven at 500 mA, which makes it suitable for use as a low-current CMOS driver. The Philips devices achieve their performance through single-heterojunction GaAlAs technology. The CNG35, CNG36, CNR36, 6N135, and 6N136 also offer a current-transfer ratio drop of only 5% after 10,000 hours of operation.



The CNG35 and CNG36 provide a dc isolation voltage as high as 4.4 kV. The CNR36 has a maximum propagation time of 8 μs. The 6N135 and 6N136 are fast-switching optocouplers that offer long-lifetime operation.

Samples of the devices are available from stock with production quantities scheduled for August. Depending on the device, they cost 118 to 243 Dutch guilders per 100 pieces in quantities of 10,000.

Philips Elcoma, P. O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone: 31-40-757005 [Circle 701]

CAD DRIVERS SUPPORT HIGH RESOLUTION

Robotechnic Ltd.'s computer-aided drafting and design software package features high-resolution graphics drivers that support 1,280-by-800 pixel displays.

Generic CADD 3.0 also offers functions that allow users to edit previous modifications to the drawing, to zoom into a particular area of the drawing, and to display 10 line thicknesses in any of the 256 colors available in the palette.

Drawn objects can be moved, copied, erased, subdivided, and stored in a user-created library for later use. Such stored drawings can be retrieved, rotated, and scaled as desired.

Required hardware is an IBM Corp. Personal Computer XT/AT or compatible with 360 Kbytes of RAM, two floppy disk drives, and either EGA or CGA graphics cards. Available now, the Generic CADD software costs £99.95.

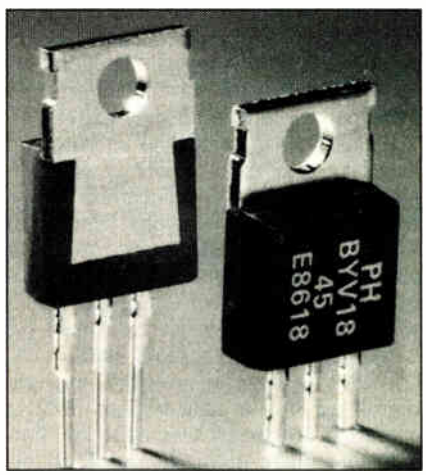
Robotechnic Ltd., 19 Queen St., Mayfair, London W1X 7PJ, UK.
Phone 44-1-499-9746 [Circle 703]

DOUBLE DIODES CUT COMPONENT COUNTS

The BYV18 series of Schottky-barrier, double-rectifier diodes from Philips reduces component count in switched-mode power supplies and high-frequency circuits by replacing individual axially leaded diodes. The series, which consists of four types (all in plastic TO220 packages), features low forward-voltage drop, low capacitance, and absence of stored charge.

The diodes target applications in which both low conduction losses and low switching losses are essential. The low forward voltage drop—less than 0.6 V—makes the diodes suitable for low-voltage output power supplies around 5 V, such as in monitors and personal computers.

The four types of diodes in the series have repetitive peak reverse voltages of 30, 35, 40, and 45 V. A 40-V type with guaranteed reverse-surge capability is also available. Prices depend on quantity and importing country; low-volume prices average about $1.10 each for 1,000 units. The devices are available from stock.



Philips Elcoma, P. O. Box 523, 5600 AM Eindhoven, the Netherlands.
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All the other features of SIEDECON are detailed in a special publication. If you would like one, please use this journal's reader service or send us the coupon.

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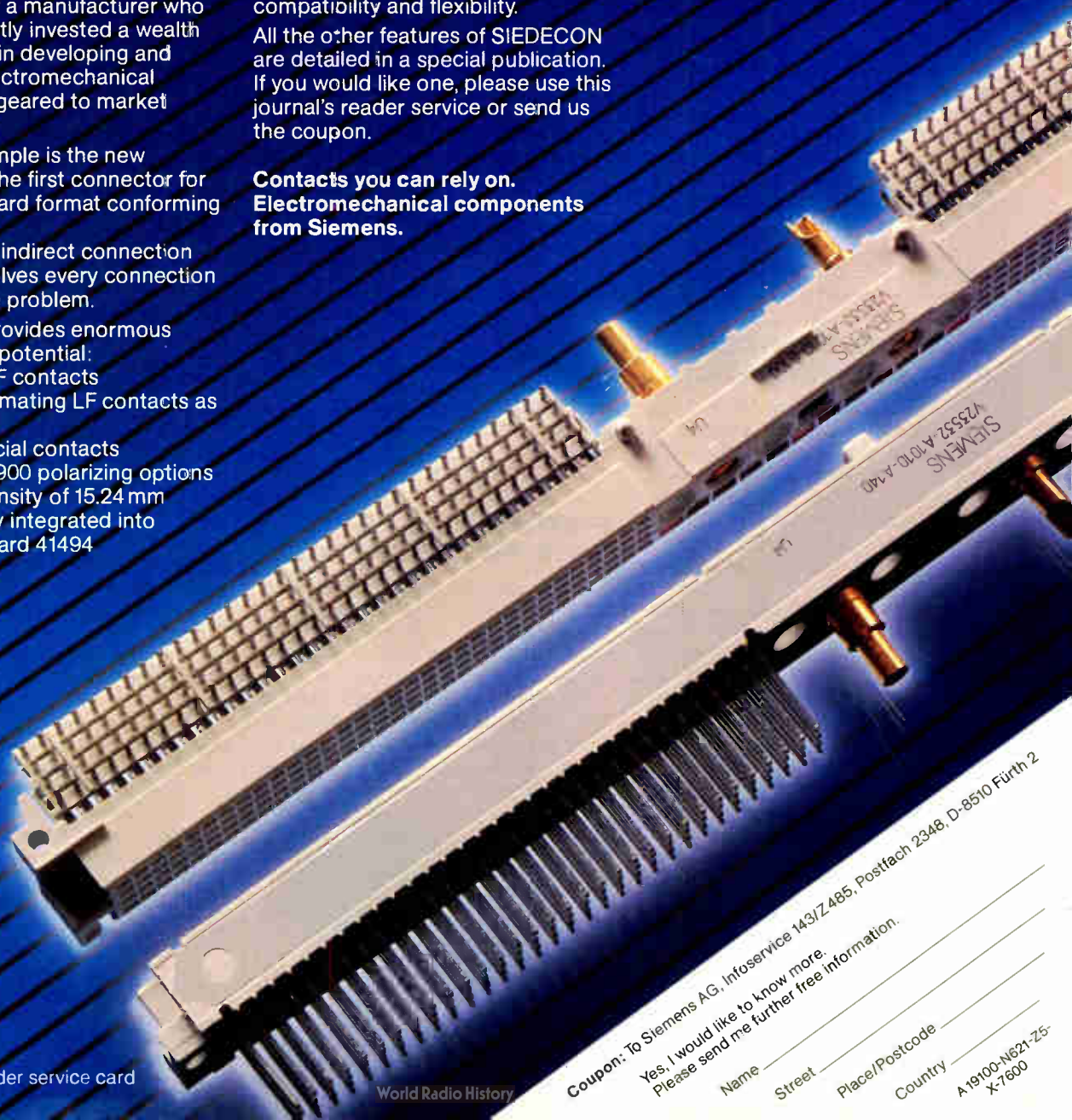

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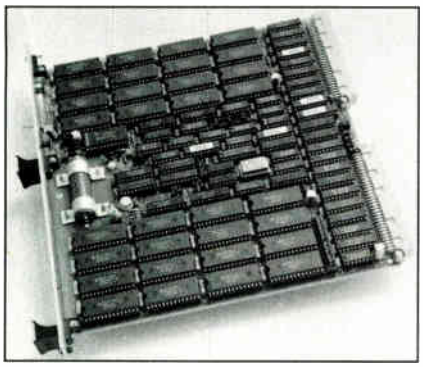
Circle 118 on reader service card

MODULE ADDS MEMORY TO VMEBUS SYSTEMS

A memory module with on-board battery backup from DY-4 Systems Inc. provides a convenient method of adding 1 Mbyte of RAM and 4 Mbytes of EPROM to VMEbus systems.

The DVME-505 can handle 8-, 16-, and 32-bit transfers over VMEbus. It occupies a maximum of 1 Mbyte of address



space in the host system. Its memory is configured from 128-Kbit-by-8-bit page-mode EPROMs and CMOS static RAMs.

The lithium battery can keep the memory active for one year. A clock/calendar is also included on the board.

Available now in commercial and military versions, the DVME-505 costs U. S. $1,327.

DY-4 Systems Inc., 21 Credit Union Way, Nepean, Ontario K2H 9G1, Canada.
Phone (613) 596-9911 [Circle 704]

AI MAKES SCANNER FAST AND VERSATILE

AI Vision Systèmes' character-recognition system uses artificial-intelligence software to read a wide variety of inputs at speeds up to 200 characters/s.

The Stirca system automatically adjusts to variations in the size of characters and can handle any font as well as handwritten numbers on stationary or moving media.

System hardware consists of a Motorola Corp. 68020 microprocessor, charge-coupled-device cameras, and various VMEbus-interface and peripheral controller boards. Software for retrieving information, computing required-light thresholds, and data processing are available as options.

Available now, the Stirca system's price varies with importing country.

AI Vision Systèmes, 29, Avenue du Roule, 92200 Neuilly/Seine, France.
Phone 33-4624-2529 [Circle 707]

FIBER-OPTIC MODEM RUNS AT 200 KBITS/S

Seiko Instruments Inc.'s fiber-optic modem offers a 200-Kbit/s transmission rate—fast enough for video transmission—over double optical fiber in communications systems conforming to the IEEE 488 standard. The SFC-1220 GP-IB modem supports transmission at distances up to 2 km when silica multimode fiber GI 50/125 is used as the medium—even in electromagnetically noisy environments, where conventional metal cable would be limited to 20 m.

The modem's light-emitting element is a diode with a wavelength of 1.3 μm. The unit is 55 mm high, 225 mm deep, and 300 mm wide. Available now, the SFC-1220 costs 350,000 yen.

Seiko Instruments Inc., Electro-Optics Systems Dept., 6-31-1 Kameido, Koto-ku, Tokyo 136, Japan.
Phone 81-3-684-2010 [Circle 706]

MOSFET BOASTS 0.6-A RATING

The ZVN4206A Mosfet from Ferranti Electronics Ltd. features a continuous current rating of 0.6 A with a 1 Ω on-resistance and 0.7 W power dissipation.

The n-channel enhancement-mode device also offers a maximum input capacitance of 100 pF that ensures switching speeds of less than 20 ns.

Developed as an interface between integrated circuits and loads, the chip is optimized for operation up to 60 V and can switch 0.5 A from a 5-V gate drive.

Housed in an E-line package, the standard ZVN4206 targets through-hole mounting to printed-circuit boards. It can also be configured for surface-mount applications.

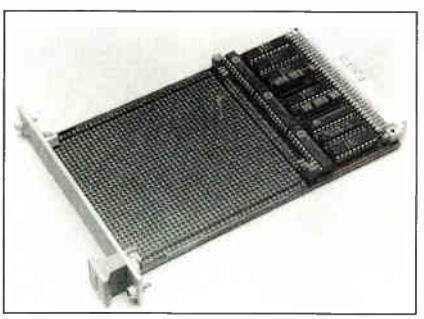
Available now, the ZVN4206A costs £0.25 in 1,000-unit purchases.

Ferranti Electronics Ltd., Fields New Road, Chadderton, Oldham, Lancashire OL9 8NP, UK.
Phone 44-61-624-0515 [Circle 708]

PROTOTYPING BOARD USES VME INTERFACE

A single-height prototyping board from PEP Modular Computers GmbH reserves two-thirds of its space for prototyping while still offering a full VMEbus slave interface.

The VPRM module makes a 40-by-34-hole grid available for prototyping circuits. Seven interrupt levels can be selected via jumpers or user devices and



two interrupt-request lines support a range of functions for sophisticated VMEbus system designs.

Applications include motor-regulator interfaces, nonstandard converter interfaces, power switching modules, timers for industrial control and high-speed input/output devices.

Available from stock, the module costs 490 DM.

PEP Modular Computers GmbH, AM Klosterwald 4, D-8950 Kaufbeuren, West Germany. Phone 49-8341-81001 [Circle 709]

OPTICAL CONNECTORS FEATURE 3-dB LOSS

The 9701 fiber-optic connector from Elco Corp. features a connection loss of 3 dB. The connectors are compatible with Matsushita Corp.'s LN125 and PN155 light-emitting diodes.

The double-pole connectors minimize light attenuation through a manufacturing process and quality control system that produces smooth fiber end faces.

Other features are a one-touch locking system and a configuration that prevents the connectors from being incorrectly joined. Cable holding force is 5 kg and the holding force on the LED is 3 kg minimum.

Available now with a solder-plated brass fixing pin, the connectors cost 800 yen for a connector with a 1-m cable attached.

Elco International Corp., 1794 Nippa-cho, Kohoku-ku, Yokohama 223, Japan.
Phone 81-45-543-7185 [Circle 710]

BOARD BOOSTS PC AT IN GRAPHICS EDITING

Optical Recording Corp.'s IB-1000 board interfaces IBM Corp. Personal Computer ATs and compatibles with the Canon Inc. NP-9030 laser printer/scanner to create an editing system that can scan and digitize fulltone and halftone images at 400 dots/in. resolution.

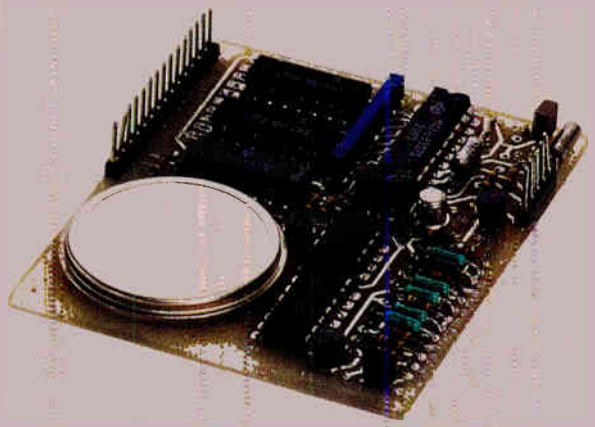
Creating a direct connection between the computer and the scanner/printer allows users to perform cut-and-paste type editing on a high-resolution PC screen.

The IB-1000 targets desktop-publishing applications with four image-processing modes: normal, fine photo (64-level pseudo halftone), positive/negative image inversion, and high contrast.

The four-layer board memory maps its image buffer addresses into the PC AT's address space for fast data manipulation. It offers a 500-ns memory-cycle time, a 4-Mbyte buffer, and 16-bit-wide words. Available now, the IB-1000 costs U. S. $3,995.

Optical Recording Corp., 141 John St., Toronto, Ontario, Canada M5V 2E4.
Phone (416) 596-6862 [Circle 711]

Remember when backup battery assembly was like putting a round peg in a square hole?



No more.

Catalyst Research's new µPowerCell™ batteries fit a rectangular footprint on your printed circuit board. That means you get more battery capacity in less space.

But that's just the beginning. µPowerCell™ batteries use Catalyst Research's patented Lithium-Iodine chemistry, the number one choice for powering implantable cardiac pacemakers. And we have over 1,000,000 Lithium-Iodine batteries in CMOS battery backup applications. We can now predict 20 years of reserve power availability, well beyond the practical life of your product, without replacement or recharging.

The B-1000 delivers one amp-hour of capacity in just 1 square inch of board space and is under 0.30" high. 600 mAhr and 400 mAhr capacity versions take even less area. And as one of the smallest backup batteries in the business, our 35 mAhr axial lead version takes less than 0.1 square inch of board space and is under 0.17" high.

This 35 mAhr battery can also be used on automatic component insertion machines just like a resistor or capacitor.

For more information call us at (301) 256-7000 or write.

™µ Power Cell is a trademark of Catalyst Research

For more information, call from your modem 1-800-332-0012 (0-1200 BAUD, 8 bit, no parity 1 stop bit) and enter the access code CAT 13A when prompted. In Va. call (703) 476-5255

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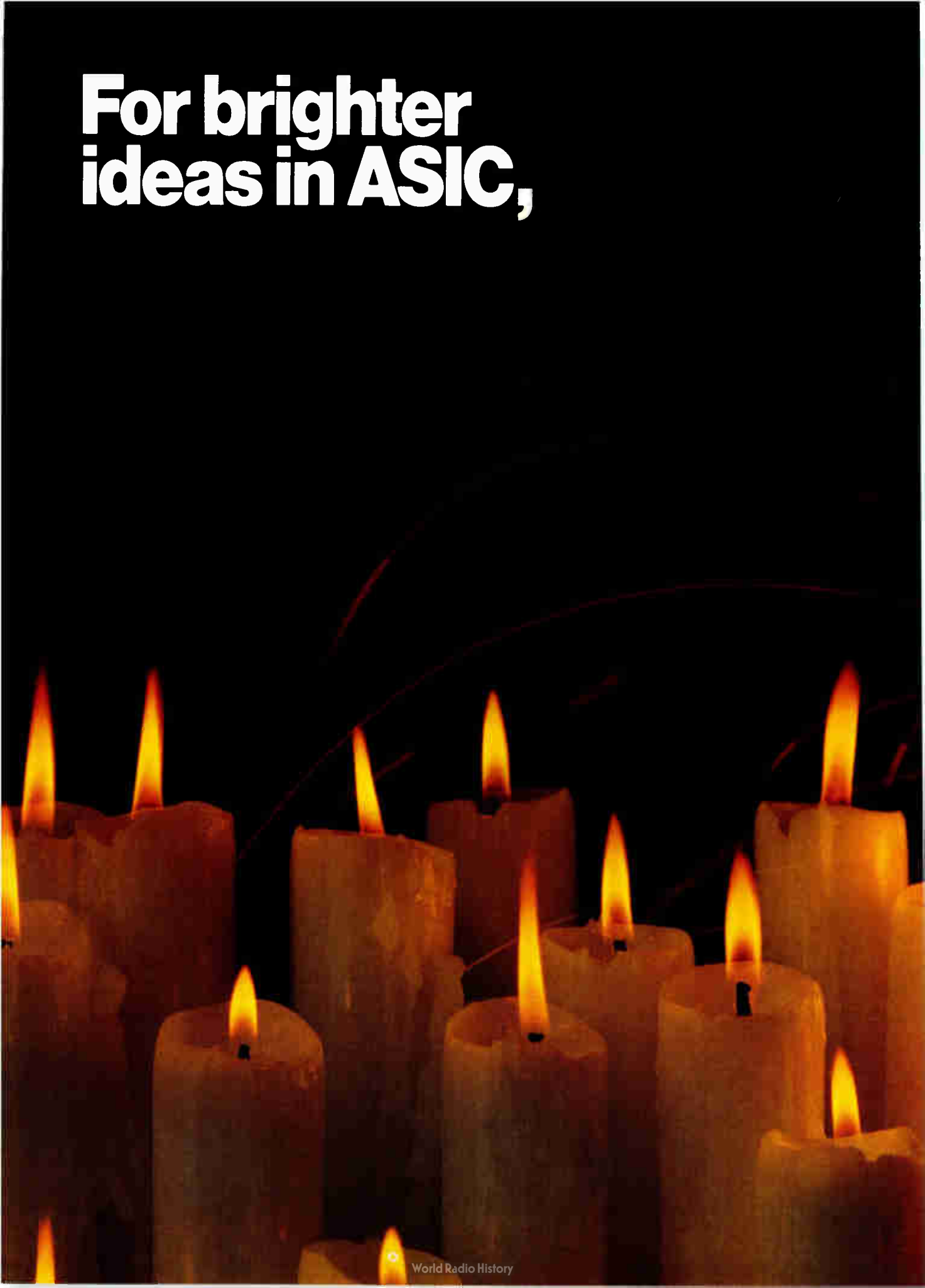
For brighter ideas in ASIC,



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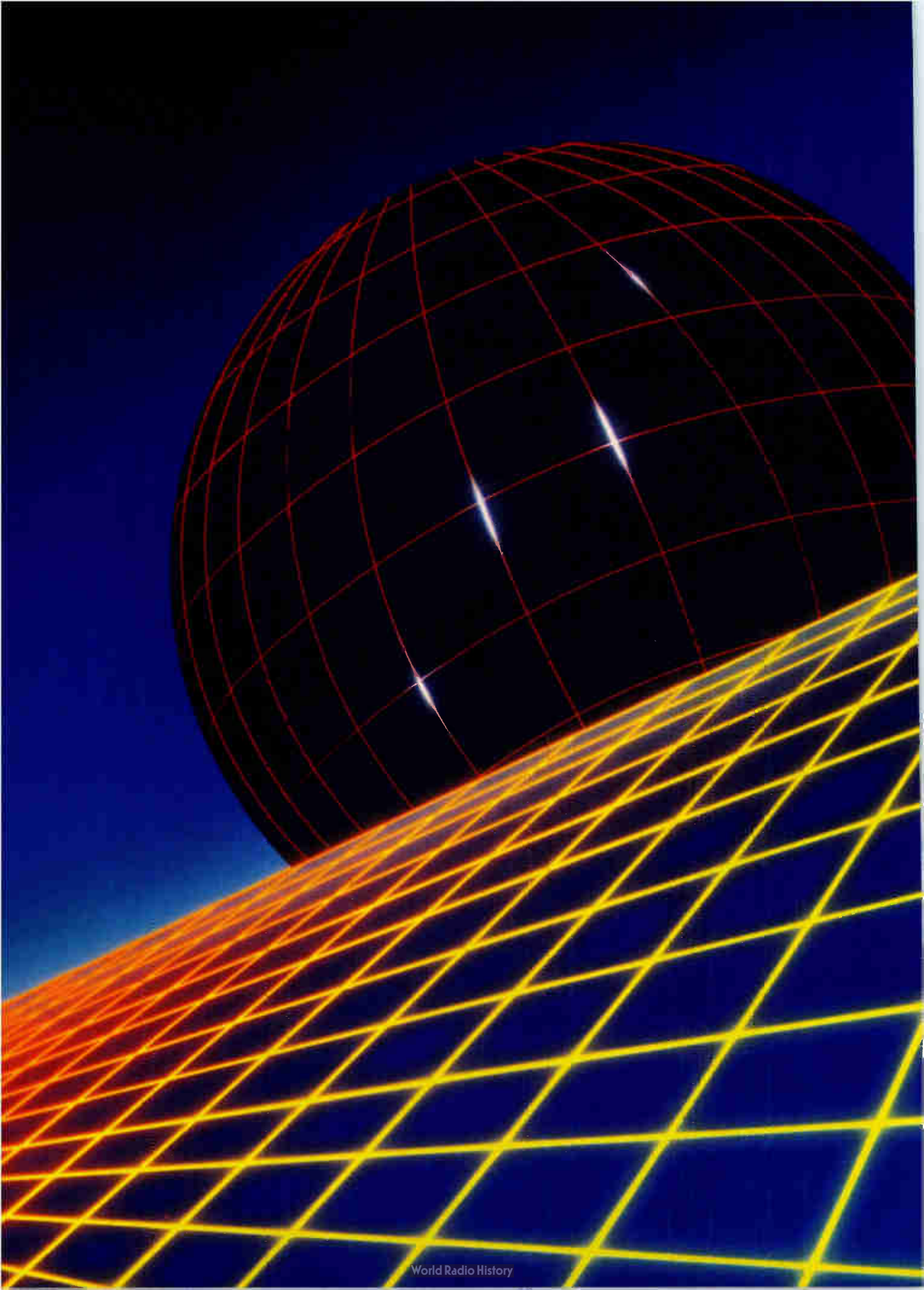

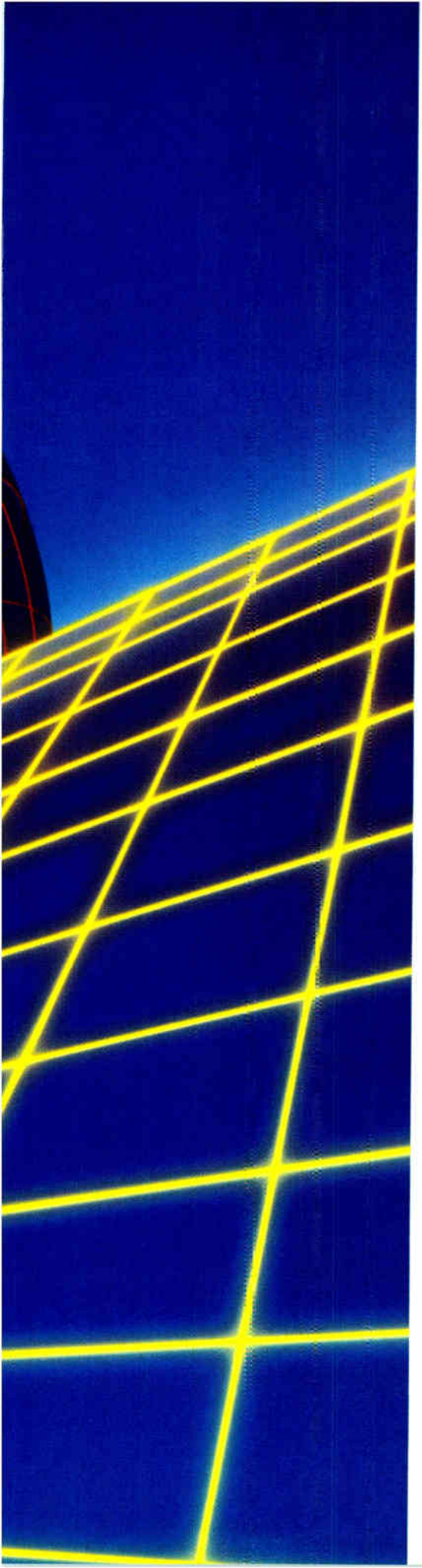

RELIABLE SUPPORT FOR ISDN

MP1601A 5GHz
Pulse Pattern Generator

Surviving in the complex and competitive world of ISDN will depend on vital problem-solving capabilities like quick response, quick recovery and preventive checking. This requires comprehensive monitoring, rigorous testing and exacting quality control of transmission systems.

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Anritsu excels in optical and digital communication test systems. We have shown our commitment to quick response to practical ISDN applications by introducing high-resolution OTDRs, 5GHz pulse pattern generators, high-performance error rate measuring equipment for digital transmissions, and many more.

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Circle 57 on reader service card

A SINGLE PACKAGE SOLUTION? IT'S ABOUT TIME.

What if there were a 16K Non-Volatile RAM that contained everything you needed in a single package? A fast and easy solution with everything from a long-life lithium battery to a real time quartz clock. Well, it's here. It's the Thomson-Mostek MK48T02 Timekeeper™ CMOS SRAM – another member in the ZEROPOWER™ family. This completely integrated device is far more efficient than real estate intensive discrete solutions. And in comparison to Dallas Semiconductor's DS1216, you'll find the 48T02 out on top every time. In every category.

For one thing, our Timekeeper RAM has 16K Bits of full CMOS memory. Theirs has none. Theirs often comes with the need for all kinds of support circuitry and discrete logic. Ours doesn't need any. And due to its software-controlled clock calibration, the Timekeeper RAM is ideal for high-accuracy applications. The Smart Watch is not. And the DS1216 requires extra time for serial-parallel software conversions and passwords. Our solution is completely parallel, so it doesn't waste your time.

The Thomson-Mostek Timekeeper RAM also features automatic power-fail chip detect and switching, write protection and read access and write times as fast as 120ns. Plus, it provides BCD format of clock and calendar data including the year, month, day, hour, minute and second. So you see, if an enhanced integrated memory solution is what you're after, don't just give it time, give it the Thomson-Mostek 48T02.

Timekeeper and ZEROPOWER are trademarks of Thomson Components-Mostek Corp.
Smart Watch is a trademark of Dallas Semiconductor.

TIMEKEEPER™ VS. SMART WATCH™

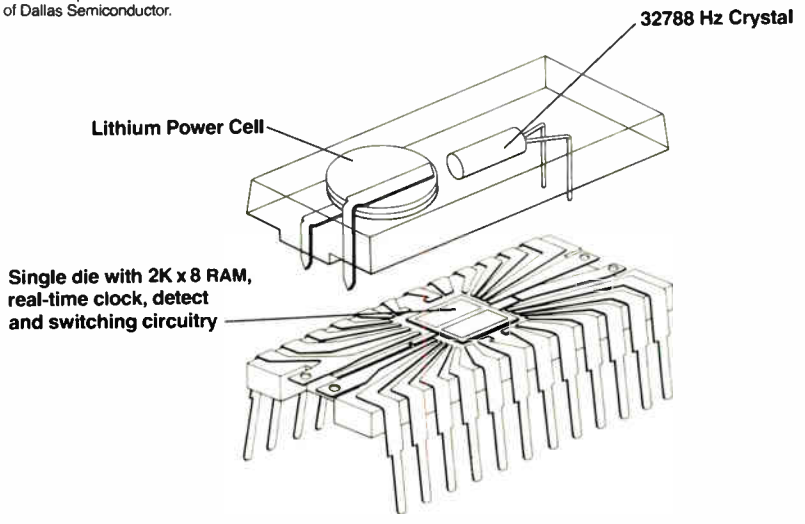
The following chart provides a comparison of the Timekeeper to the closest level of integration available, the DSC Smart Watch. You'll be able to see that when it comes to comparing apples to apples, our Timekeeper RAM is much easier to use and much more cost effective.

Parameter	MK48T02	DS1216
Memory Provided	Yes, 2K x 8 Full CMOS	No, must be provided by user
Speeds Available	120ns to 250ns	250ns only
Data Access Method	Parallel	Serial
Time to Read or Set Clock / Calendar Data	2.25µs	32.25µs
On Chip Calibrations	Yes	No
Low Battery Warning Flag	Yes	No
Pins	24	28

CURRENT ZEROPOWER DEVICES

Write Control	Write Protection Voltage 4.75V	4.5V
2 or 3 Wire	48T02 48Z02	48TI2 48ZI2
3 Wire only	48T03 48Z03	48TI3 48ZI3

Also in development, we have higher density 8K x 8 ZEROPOWER RAMs to complement the family shown in the table below – the 48Z08, 48Z09 – both are 28 pin devices. Like our ZEROPOWER RAMs, these devices will be available with a 4.5V write protection option for use in systems with ±10% power supplies.



In addition to memories, Thomson-Mostek manufactures MOS and bipolar devices for both commercial and military applications: microcomponents, telecom/datacom and linear circuits as well as Discrete, RF and microwave transistors, passive components and ASIC.

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A Leader in the Optical Age: Toshiba DFB Laser Diode

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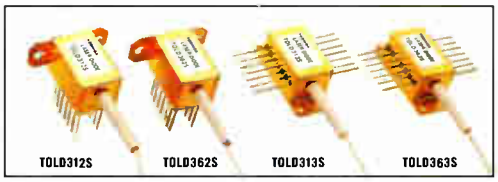
In addition, long-haul transmission of 2.0Gbps data is easily possible. And the wide variety of Toshiba systems assures that your specific needs are met.

Toshiba: the pioneer of laser diodes in the exciting world of communications, from CATV and TV conference to videotex systems.



PACKAGE	1.3μm DFB	1.55μm DFB
CHIPCARRIER	TOLD300S	TOLD350S
DIL	TOLD312S	TOLD362S
BUTTERFLY	TOLD313S	TOLD363S

TOSHIBA

TOSHIBA CORPORATION TOKYO, JAPAN

INSIDE TECHNOLOGY

THE CHANGING FACE OF NONVOLATILE MEMORIES

Faster, denser EPROMs and EEPROMs are finding new uses, displacing big ROMs and fast PROMs, for example; big chunks of them can also be added to ASICs

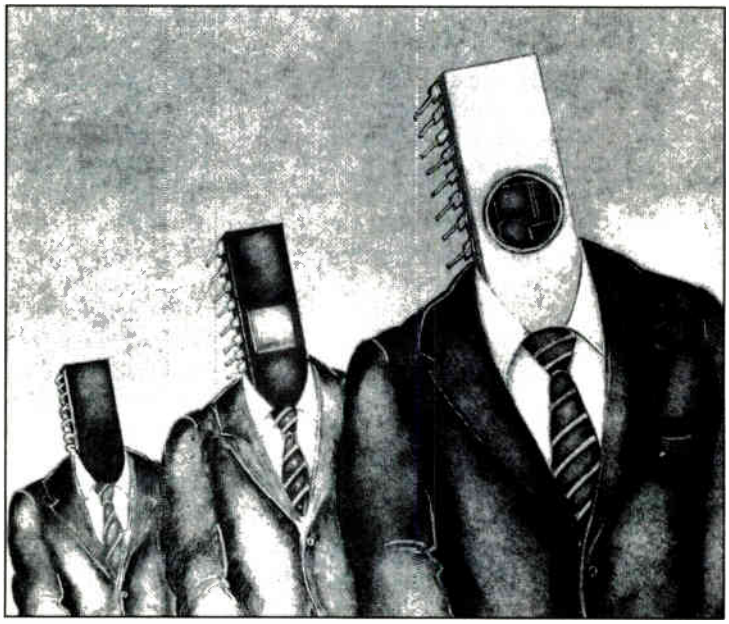
by Bernard C. Cole

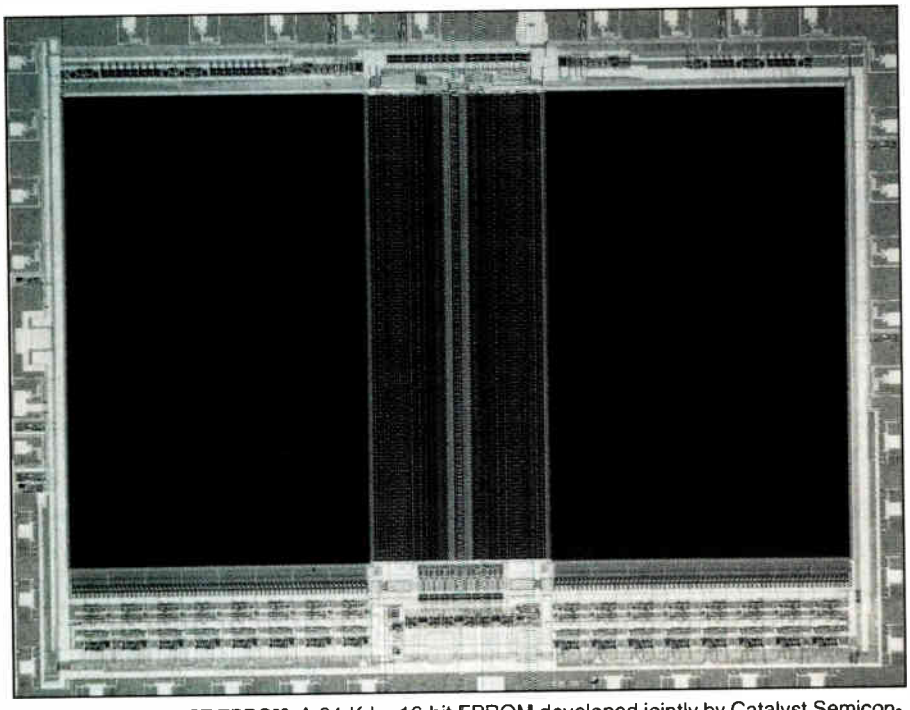
Nonvolatile memories are taking on a whole new look. As both erasable programmable read-only memories and electrically erasable PROMs get faster and denser, they are starting to displace high-density ROMs and high-speed PROMs in new applications. In current applications, nonvolatile memory will now take up significantly less board space. Higher densities also will make it easier to incorporate larger amounts of nonvolatile memory on other types of chips, opening the door to logic chips that integrate large arrays of EPROM and EEPROM.

A new generation of higher-density commodity parts is under development, while lower-density parts are being pushed to significantly faster access times. Moreover, the need for designers to choose between speed and density may disappear, as companies such as WaferScale Integration Inc. in Fremont, Calif., (see p. 65) develop parts that combine both features.

Beyond making improvements to conventional parts, a drive is under way among chip makers to develop memories tailored to specific market segments—markets where speed is paramount, or power requirements are important, for instance. An example of the latter is a 64-Kbit EEPROM that needs only 3 V, reducing backup battery requirements in lightweight portable equipment. The part was jointly developed by Catalyst Semiconductor Inc. of Santa Clara, Calif., and Oki Semiconductor Corp. of Tokyo (see p. 67). In addition, companies are looking to incorporate nonvolatile-memory technology into other non-memory chips, applying their expertise to a variety of logic circuits—including microcontrollers, digital signal processors, programmable logic, and even application-specific integrated circuits based on standard cells.

One reason for all the activity in nonvolatile-memory product development is today's healthy market. The current crop of EPROM and EEPROM products are chalking up very strong sales—so strong that cautious manufacturers are reluctant to believe the optimistic projections of future business, says Victor deDios, senior industry analyst at Dataquest Inc. of San Jose, Calif. Overall, he says, worldwide EPROM sales for 1987 can be expected to hit $1 billion, up 8% from $910 million in 1986 and up 14% from the reces-





1. FAST EPROM. A 64-K-by-16-bit EPROM developed jointly by Catalyst Semiconductor and Oki Semiconductor boasts a 150-ns access time.

sionary dip to $876 million in 1985. Next year, says deDios, with projected sales up 20% to $1.2 billion, they will again equal the sales for 1984, the industry's high point to date. Prospects are even brighter in EEPROMs. DeDios estimates that sales for 1987 will reach $231 million, up 61% from the $139 million in 1986. In 1988, he expects sales to grow by about 50% to $345 million.

And while the markets are taking off, somewhat surprisingly, Japanese makers of EPROM and EEPROM aren't keeping pace with the exploding market growth. They will slip from a market share of 15% to 20% in 1986 to less than 5% this year. To be sure, most U. S. manufacturers regard the Japanese slippage as temporary. Therefore, they're in a hurry to develop products that will put them in a strong position for both commodity parts and in high-return specialty niches when competition heats up again as the Japanese charge back into the marketplace.

For now, strong sales and the drop in Japanese competition is causing a period of price stability. And most EPROM manufacturers are using the resulting higher profits to fund more development work on CMOS processes that will take them to higher densities, higher speeds, and lower power, says deDios. The market is moving away from 64-Kbit EPROMs and toward 256-Kbit and 512-Kbit devices, says Dave Bostwick, director of strategic development for the memory group at Advanced Micro Devices Inc., Sunnyvale, Calif. Also entering the market in volume production are 1-Mbit EPROMs from AMD, Fujitsu, Hitachi, Intel, and Toshiba. One of the most recent arrivals on the 1-Mbit EPROM scene is the CAT27C210, a 64-K-by-16-bit CMOS device jointly developed by Catalyst and Oki (see fig. 1). Pin-for-pin compatible with Intel's 27210, it features 150-ns access times, an active power figure of only 150 mA, and a standby power of 500 μA.

One indicator of things to come is a 4-Mbit EPROM under development at Toshiba. Built using a 0.8-μm CMOS process, it incorporates a basic cell measuring only 9 μm^2, matching that of many single-transistor dynamic random-access memory cells. The 8-bit-wide device features a high cell current of about 10 μA, resulting in a low typical access time of 120 ns.

Access times are also being reduced in current lower-density EPROMs—from an average of 200 to 350 ns down to 150 to 200 ns, says Alan Ankerbrand, director of MOS memory marketing at National Semiconductor. And within a year, he says, speeds will edge downward even more, to about 100 to 150 ns. Dataquest's deDios agrees: "By this time next year anything under 512 Kbits in density with access times of more than 150 ns will be out of the mainstream."

In traditional full-function EEPROMs based on the Fowler-Nordheim effect, says deDios, the majority of the marketplace is moving from 64 Kbits to 256 Kbits. Most authorities agree current technology stops there, however: "Unless a radically new cell structure and architecture comes along, it will be difficult for EEPROMs to move beyond 256 Kbits," says Ian Wilson, director of product marketing at SGS Semiconductor Corp. U. S., in Phoenix, Ariz.

An alternative technology that many firms are looking at to break beyond 256 Kbits is "flash" architecture, so named because the contents of all the memory's array cells are erased simultaneously by a single field emission of electrons from the floating gate of an erase gate. Such an EEPROM combines the advantages of the ultraviolet-light-erasable PROM and floating-gate EEPROMs. It unites the high density, small size, low cost, and hot-electron-write capability of an EPROM with the easy erasability, on-board reprogrammability, high endurance, and cold-electron-tunnelling erasure of floating-gate EEPROMs.

So far, the only player in the flash EEPROM market is Seeq Technology Inc., San Jose, Calif., which introduced its first device, the 128-Kbit 48128, in August 1986. It is now following up this initial n-MOS part with two higher-density 1.5-μm CMOS parts, the 512-Kbit 48C512 and the 1-Mbit 48C1024, both with 8-bit-wide organizations. With a memory-cell size of only 20 μm^2—about one quarter the size of current EEPROM cells—these parts achieve EPROM die sizes, says

Mike Villott, vice president of marketing at Seeq, and they provide EEPROM features previously not available. Such features include on-chip address and data input latches to permit microprocessor-compatible write and erase cycles, as well as chip-erase and page-erase modes.

And whereas the 48128 required a 21-V power supply on multiple pins, the new flash EEPROMs require only a single 12-V external supply for programming and erasure. Moreover, he says, this programming voltage can be applied during read operations, which eliminates the need to switch it off when not erasing or programming. Byte write time is only 1 ms, and chip and byte erase times are no more than 5 s. Endurance—the number of times the device can be erased and written to—is 100 cycles minimum and can be screened to 1,000 cycles.

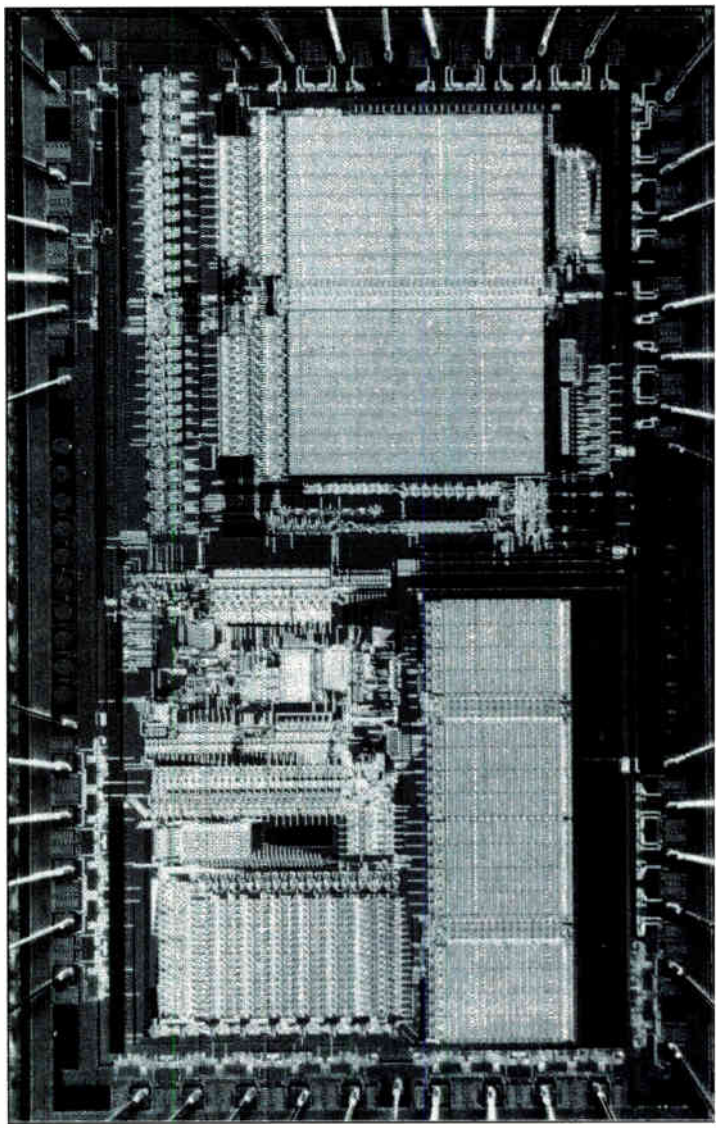
Hoping to follow Seeq into the market with a high-density flash EEPROM is Exel Microelectronics of San Jose, Calif., which is in development on a 512-Kbit device it expects to introduce early next year. Also investigating the technology as a way to achieve higher EEPROM densities are AMD, Fujitsu, Hitachi, National Semiconductor, Texas Instruments, and Toshiba.

Another recent convert appears to be Intel Corp., Santa Clara, Calif., although until recently it was enthusiastically exploring another approach to high-density EEPROMs, the thick-oxide technique pioneered by Xicor Inc. of San Jose, Calif. Intel, however, has abandoned its efforts in this area, says Don Knowlton, general manager of Intel's programmable-memory operations in Folsom, Calif., and is investigating other techniques for higher density, including the flash-EEPROM approach.

That leaves Xicor going it alone with the thick-oxide technique. The company is now in production with a 256-Kbit n-MOS device, the X28256 [*Electronics*, May 12, 1986, p. 30] and is also developing a CMOS version, the X28C256, which it expects to introduce later this year, and a 1-Mbit device tentatively scheduled for early next year.

For many manufacturers, however, the bright prospects in the mainstream EPROM and EEPROM market are essentially an opportunity to carve out new niches. The past has taught them a painful lesson: the memories may be nonvolatile, but their market is not. They want to find areas where price pressure and competition are less intense. Among the possibilities they're exploring are high-speed bipolar PROM replacements, parts tailored to specific applications such as smart cards, and other applications outside the traditional domain of EPROMs and EEPROMs.

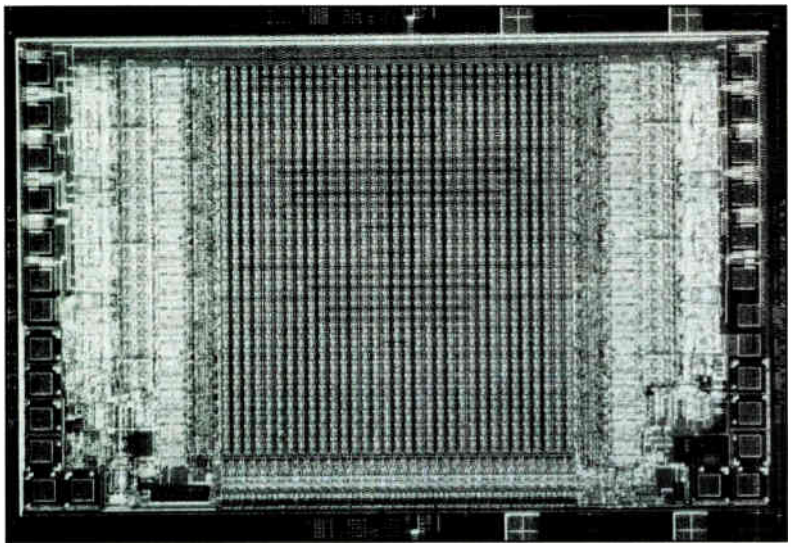
Two companies that have successfully established themselves in the bipolar PROM replacement market are Cypress Semiconductor Inc. of San Jose, Calif., and WaferScale Integration, with 16-Kbit and 64-Kbit CMOS EPROMs in the 35-to-50-ns range. Also looking to participate is Seeq, which has just introduced two byte-wide



2. REPROGRAMMABLE DSP. General Instrument has put 2.5 Kbytes of EEPROM on a digital signal processor chip.

35-ns EEPROMs, the 16-Kbit bit 36C16 and the 32-Kbit 36C32 [*Electronics*, April 30, 1987, p. 66]. Others thinking hard about entering the market include AMD, Intel, and SGS.

Another niche is being explored by Intel, which is looking at what Knowlton calls "application-oriented" EPROMs—nonvolatile memory devices with extra logic that optimizes the devices for specific applications. One of the company's first efforts in this direction was the 27916 KEPROM, or keyed-access EPROM, which combines the memory array with a pseudo-random number generator and encryption circuitry that can determine if the person accessing its contents is authorized. Taking the concept even further, the company this month introduced the first in a new series of such applications-oriented EPROMs, the 87C257 and 68C257—256-Kbit devices with on-chip latches that allow the memory's address and data pins to be tied directly to a microcontroller's multiplexed address and data



3. ERASIC. Exel's 78C800 is the first in a family of what it calls electrically reprogrammable ASICs, made with EEPROM technology.

pins. The two devices, intended for the 8051/8096 and 6800 series of microcontrollers, respectively, eliminate the need for the external logic, such as latches and inverters, that is typically required in microcontroller-based systems, says Tom Price, EPROM marketing manager.

Japanese firms seem to be carving out a niche for themselves in extremely high-density EEPROMs and EPROMs of more than 1 Mbit, for use in smart cards and memory cards. Estimated to be a billion-dollar market by the early 1990s [*Electronics*, Dec. 18, 1986, p. 55], smart cards will require high levels of built-in microcontroller intelligence, as well as memory that is both dense and nonvolatile. The only direct U. S. competitor to the Japanese in the EEPROM- and EPROM-based smart- and memory-card market is General Instrument Microelectronics, Chandler, Ariz. Besides planning to produce EPROMs and EEPROMs ranging from 256 Kbits to 1 Mbit over the next six months, the company has installed the equipment to make the smart cards themselves, as well as card readers, power supplies, and connectors. Also making efforts in this direction are Texas Instruments Inc. and Motorola Inc., but only at the chip level. The fourth contender in this arena is the team of Catalyst Semiconductor Inc. and Oki Semiconductor, which aims to produce controllers and EEPROMs.

Another strategy EPROM and EEPROM companies are following is diversification outside traditional stand-alone products. They are applying their improved nonvolatile technology to microcontrollers, DSPs, field-programmable logic, and even standard-cell ASICs.

Traditionally, small amounts of EPROM or EEPROM—usually no more than 1,024 bits—have been incorporated into microcontrollers to give users some reprogrammability. "With new advances in nonvolatile memory technology, much higher levels can be incorporated," says B. K. Marya, president of Catalyst Semiconductor. In the new generation of devices from AMD, Catalyst, Intel, SGS, and Xicor, on-chip nonvolatile memory has risen to 32 Kbits or 64 Kbits.

On-chip nonvolatile memory is also being used on DSPs. One such device is the DSP320EE12 from General Instrument, a pin-for-pin compatible version of TI's TMS320C10 DSP chip, but with 2.5 Kbytes of EEPROM added (see fig. 2). In the very near future, says Marya, it should be possible to incorporate up to 256 Kbits onto the microcontroller chip.

In programmable logic devices, two nonvolatile memory vendors—Intel and the Exel subsidiary of Exar Corp., San Jose, Calif.—have already entered the market. A third, Seeq, has just entered into a technology exchange agreement with Monolithic Memories Inc., which dominates the field-programmable array-logic market with its bipolar devices.

Just entering the market this month with a PLD product based on its EEPROM technology is Exel, with the first in a family of what it calls ERASICs, or electrically reprogrammable ASICs. Designated the 78C800 (see fig. 3), it is the first commercially available CMOS PLD offering a single-plane folded-NOR architecture, says Narayan Purohit, Exel product marketing manager. This approach makes it possible to implement multilevel logic designs and does away with the limitations of the traditional AND/OR-based designs now used. Intel's first proprietary PLD is an EPROM-based programmable bus-interface controller designated the 5CBIC. A programmable three-port transceiver with embedded programmable logic macrocells and cross-point signal routing, it allows designers to implement any of a number of different bus interfaces with a single circuit. A third company, WaferScale Integration, is working with Altera Corp. of Santa Clara, Calif., a manufacturer of EPROM-based PLDs, on a new family of user-configurable microsequencers based on its proprietary high-speed split-gate technology [*Electronics*, March 19, 1987, p. 76].

On the standard-cell side, at least two nonvolatile-memory companies—WaferScale and Exel—are in the market with cell libraries that incorporate EPROM and EEPROM cells, respectively. Similar efforts are under way at Intel and National Semiconductor, among other companies. In the Exar effort, Exel's EEPROM technology has been incorporated in standard cells ranging from a single bit to arrays of 1 Kbits. The same family of products also includes a wide range of analog megacells, including analog-to-digital and digital-to-analog converters and a variety of switched-capacitor filters. At WaferScale, engineers are upgrading an already existing EPROM-based cell library with cells that incorporate the company's newest and fastest EPROM technology. □

WAFERSCALE'S 256-K EPROM RUNS SUPERFAST

Speed or density? Density or speed? Thanks to WaferScale Integration Inc., systems designers no longer must compromise. The Fremont, Calif., company has just unleashed a pair of high-speed, 256-Kbit ultraviolet-erasable CMOS programmable read-only memories. With 50- to 55-ns access times, they are the fastest nonvolatile memories on the market at 256 Kbits and beyond—at least two to three times quicker than comparably sized PROMs, and coming within range, at twice the density, of the largest commercial bipolar PROM [*Electronics*, Feb. 10, 1986, p. 35]. And active power dissipation is a comfortable 325 milliwatts, just half that of its closest bipolar rival, sinking to 75 mW on standby.

With their combination of speed and density, the word-wide 16-K-by-16-bit WS57C257 and byte-wide 32-K-by-8-bit WS57C256F are tailored to one- and two-chip program storage for 16- and 32-bit microprocessors and digital signal processing. Conventionally, anywhere from 4 to 16 nonvolatile memories are needed. Current plans call for the byte-wide memory to hit the streets in July in standard 28-pin ceramic dual in-line packages and 32-pin ceramic leadless chip carriers. The word-wide part will follow sometime in the third quarter, in 40-pin Cerdips and 44-lead ceramic leadless chip carriers. Both are priced at $94 per unit in 100-unit sample quantities.

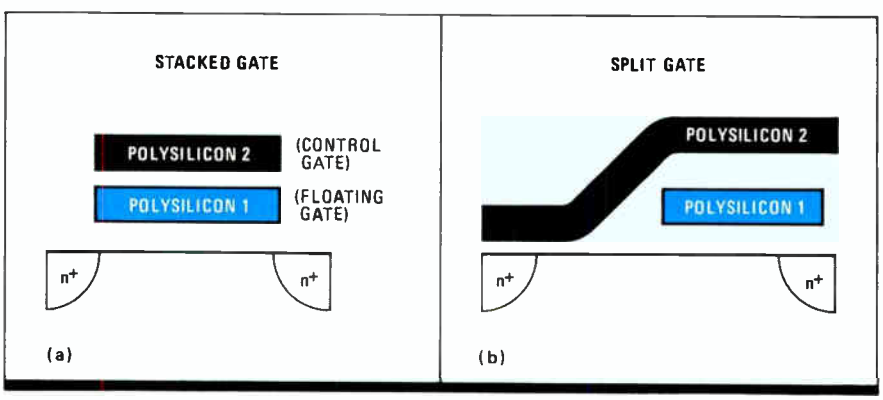
To achieve this unprecedented combination of speed and density, engineers at WaferScale Integration refined the company's process technology and fine-tuned the circuit design. On the process side, a slimmed-down, second-generation 1.2-μm CMOS process, a scaled version of the company's patented split-gate EPROM cell, and tungsten silicide word lines were the keys to success. On the circuit-design side, clocked differential sensing and a novel precharge technique, a special two-step ac signal scheme, and address-transition detection were the key developments. "These two devices disprove the traditional belief that you could have speed or size, but not both, in your microcontrol store," says Jerry Banks, marketing manager for standard products. "These large-architecture CMOS EPROMs are ideally suited for modems, real-time control, guidance systems, digital signal processing, and other real-time or complex processing applications."

WaferScale Integration first boiled down its CMOS process—from 1.5 to 1.2 μm—and then used the refined technology to whip up a scaled version of its proprietary split-gate EPROM cell. Just 6.5 μm on a side, the latest split-gate incarnation is roughly half the size of its predecessor. There's more to the new cell than just size, but the company won't go any further than saying that it adopted tungsten silicide.

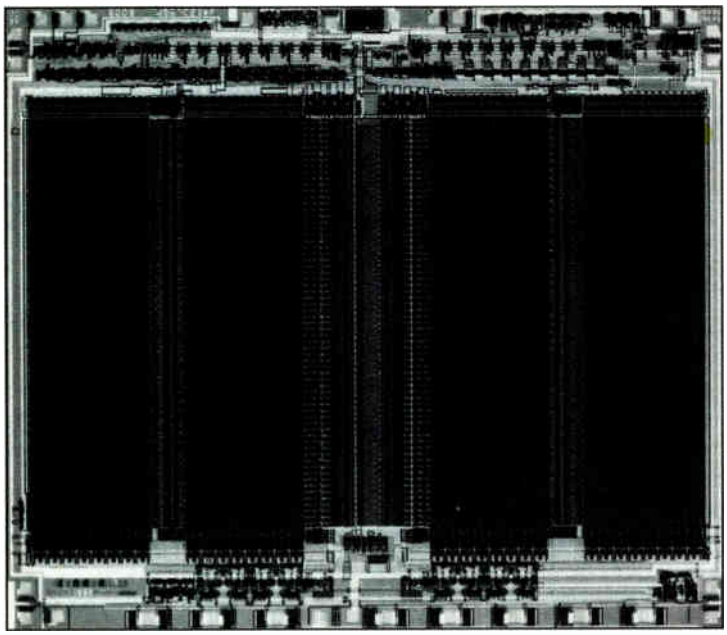
The main problem with the traditonal stacked-gate cell, notes Boaz Eitan, manager of the PROM program, is that it forces a tradeoff between the necessarily high read current and efficient programmability. "In traditional implementations, chip designers have had to make a choice," he says. "If they wanted speed, they had to implement a PROM cell with three to four transistors, separating the read, write, and select functions. If they wanted density, all three functions could be incorporated into a single-stacked PROM cell, but only at considerable sacrifice in speed."

The heart of the trouble lies in rapidly sensing the word- and bit-line voltages after address decoding. "The bit-line capacitance plays a big part in the equation," explains Syed Ali, manager of memory design. "If the capacitance remains fixed, a higher read current is needed to achieve greater speed. However, if the capacitance can be lowered, the speed can be boosted without increasing the read current."

The split-gate structure weds the best of the multiple-transistor and single-stacked cell approaches, requiring none of the compromises inherent in either. It consists of a MOS transistor linked in series with a floating-gate transistor that has been merged into a composite device (see fig. 1). In this design, says Eitan, the second polysilicon layer acts as the control gate and directly covers part of the channel area. "This eliminates drain turn-on and source-drain punchthrough, which adversely affects the stan-



1. SPLITS. Unlike the stacked-gate transistor (a), the split-gate transistor (b) has a second poly control gate that partly covers the channel, preventing drain turn-on and source-drain punchthrough.



2. DELAY KILLER. Tungsten-silicide deposition helps WaferScale's 256-Kbit EPROM achieve its 45-ns access time.

dard stacked-gate EPROM cell." As a result, bit-line read currents in excess of 150 μA can be achieved, compared with the 50 μA typical of conventional stacked-gate cells, giving the speed of the multiple-transistor EPROM cell without its attendant die size.

The memory array (see fig. 2) is divided into two planes, each consisting of two blocks separated by a mid-word-line repeater. Tungsten silicide is deposited over the second polysilicon layer to reduce word-line RC delays, further improving access time. With a resistance of only 3 Ω per square μm, tungsten silicide helps reduce the delay to 60% of that incurred with traditional aluminum metallization. The 512 columns of the array are divided into blocks of eight columns, each block with its own dedicated source lines.

The higher bit-line voltage and read current established by the split-gate structure allow the company to employ a differential-sensing scheme that does not require a separate bit line, thus eliminating bit-line capacitance. In this scheme, the sense amplifier is designed to work in conjunction with a trip inverter. During precharge, the outputs of the differential amplifier and the inverter are precharged to the inverter trip point, enabling the inverter to move rapidly in either direction after a signal has been detected. The relative difference in the rate of discharge between the bit line and a column of reference cells provides just enough differential voltage for high-speed sensing.

To ensure that signal levels are high enough for sensing—a key consideration in all memories, as density increases and interconnects get longer—a two-step ac signal-development scheme has been incorporated into the circuits. In the first step of the proprietary approach, a small ac signal is generated by using a capacitor-imbalancing technique. This 100-mV signal is rapidly read out by a differential sense amplifier. In the second step, the on-chip circuitry converts this signal to a 300-mV dc signal that is used to increase programmed cell margins by as much as 25%.

As a result, says Eitan, the design senses bit-line voltages more than five times faster than previous devices. The scheme also makes for fast programming. Typically, it takes only 0.1 ms to program a byte, compared with 1 ms for older technologies.

Address-transition detection also contributes to the improved access times. Normally associated with static random-access memories, it helps precharge the bit lines and to equalize the gain of the critical sense amplifiers. When an address transition is detected, an enable pulse is generated that precharges the bit-lines and critical sense-amplifier nodes. This eliminates the setup time normally encountered in PROMs. To further reduce the precharge time, the bit-line voltage swing is kept within narrow limits. More time is saved by performing the address decoding in parallel with the bit-line precharge, then ending them simultaneously.

To keep power dissipation down, only 25% of the cells in the array have access to the supply voltage during a read. This dramatically decreases the supply current to no more than 40 mA at 20 MHz, about half that of other designs.

WaferScale Integration is also using its high-speed process for a 64-Kbit PROM, the 8-K-by-8-bit WS57C49B, a direct pin-for-pin replacement for a bipolar PROM (called a reprogrammable ROM, or RPROM). At 35 ns it matches most high-speed CMOS SRAMs in access time. Another device for which it is using the high-speed process is a pin-for-pin CMOS relacement for the Am27C51, a 128-Kbit bipolar PROM from Advanced Micro Devices Inc., Sunnyvale, Calif. The WS57C51 is a 16-K-by-8-bit RPROM with an access time of only 55 ns and a chip area of only 32,000 mils^2, 60% smaller than the AMD device.

The company is now working on its next-generation CMOS PROM process, which at 1.0 μm will enable it to build 64-Kbit memories that access in only 25 ns and 128-Kbit and 256-Kbit devices that access in 35 ns. The same process will also allow WaferScale Integration to extend its speed challenge up into the megabit range. "There is nothing in our process that I can see that will prevent us from building 1-Mbit EPROMs with access times as low as 55 ns," Ali says. *–Bernard C. Cole*

For more information, circle 480 on the reader service card.

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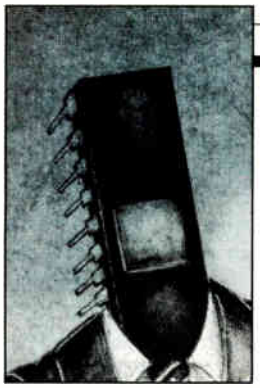


CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS

Five volts is no longer the magic number when engineers talk portable and battery-backed applications. Catalyst Semiconductor Inc. of Santa Clara, Calif., has just put the finishing touches on a 64-Kbit EEPROM that reads and writes with a supply voltage as low as 3 V. And this diminutive appetite comes at no substantial cost in speed. With an access time of 120 ns, the memory keeps pace with many existing 5-V devices. When operated at 5 V, its reads take a mere 60 ns. Also in its favor is the fact that it draws an active current of only 7.5 mA at 8 MHz, about a fifth that of its rivals.

Low voltage opens up a wide range of battery-backed applications, says B. K. Marya, Catalyst's founder and president—among them, hand-held computers, smart cards, pagers, beepers, and many telecommunications devices, which require long-term battery backup as well as small size.

The memory also will compete with nonvolatile static random-access memories that incorporate a 3-V lithium battery. "The advantage of battery-powered nonvolatile SRAMs is their ability to read and write data with access times of 120 ns or less," Marya points out. Moreover, "traditional high-density EEPROMs of 64 Kbits or more usually require at least a 5-V read and write voltage. And they are not only slow but also difficult to operate if reprogramming is necessary, requiring as they do at least four AA-type batteries or an expensive lithium power source." Because it can be operated and programmed with a 3-V supply, the device requires only two 1.5-V batteries in portable consumer settings and makes it possible to go with small lithium power sources in smart cards. Eventually, Marya says, as the power-supply requirements of EEPROMs continue to decline, it may be possible to substitute solar cells for batteries in a wide variety of applications.

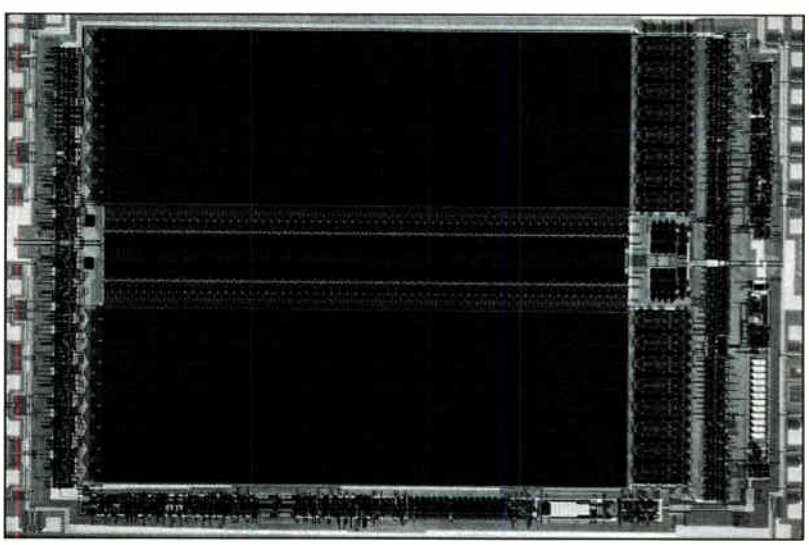
The EEPROM is the fruit of international cooperation. The cell and circuit design were contributed by Catalyst, which also created and modified the architecture. Oki Semiconductor of Tokyo furnished the process, jointly modified by the two partners, and served as the silicon foundry.

Critical to the success of the joint venture was a variety of proprietary circuit wizardry. Broadening the supply-voltage range ensured successful reads and writes despite voltage fluctuations. Bootstrapping capacitors and a clever differential sense amplifier make certain that reads are accomplished quickly in the face of low voltage and power-supply variations.

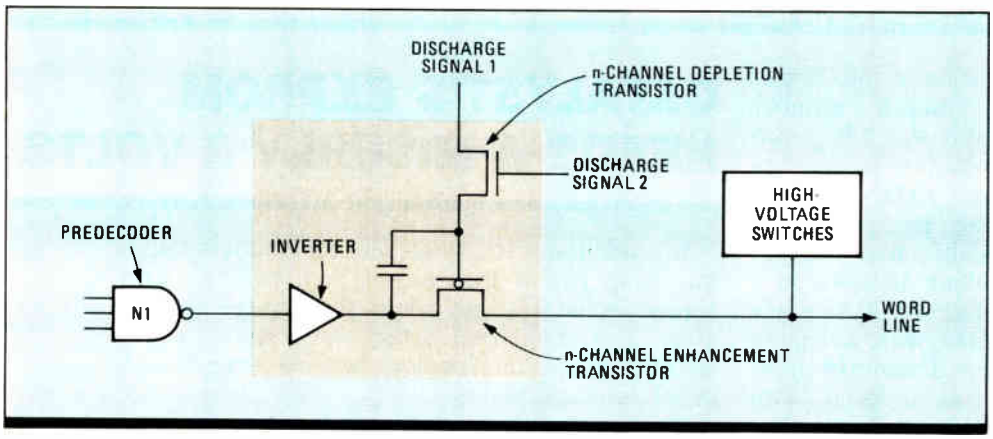
In addition, a dual-clocked, high-voltage switching circuit guarantees that switches are thrown reliably, even when the voltage fluctuates. And dynamic, rather than static, page latching keeps the memory writing even while supply voltage varies.

Measuring 4.84 by 7.06 mm and housed in a 28-pin plastic dual in-line package, the Catalyst MSM28C64A (see fig. 1) is fabricated with a slight modification of Oki's 1.5-μm n-well double-polysilicon CMOS floating-gate process. The memory incorporates five types of transistors: p-channel and n-channel enhancement-mode MOS transistors for fabricating the 3-V circuits, and enhancement, depletion, and non-ion-implanted n-type transistors for fabricating the charge-pumping circuitry that converts the 3-V supply to 18 V on-chip; in addition to these transistors, there are the floating-gate devices themselves.

The key to achieving low-voltage operation in portable applications is the ability to maintain stable reads and writes over long periods, despite the substantial variations in supply voltage associated with batteries. Relaxing the supply-voltage tolerances of the basic EEPROM cell makes that possible. With its dynamic page-mode latching scheme, the device is relatively insensitive to voltage changes and can operate even if the supply voltage varies 20% in either direction, Catalyst claims. By comparison, most competitive devices can operate only within variations of ±10 V. When operated at, for example, 5 V, the Catalyst part's supply voltage can vary from 4 to 6 V, whereas conventional EEPROMs



1. LOW VOLTAGE. Catalyst's MSM28C64A EEPROM has five types of transistors that form the charge-pump circuit needed to convert the 3-V supply to 18 V on-chip.



2. BOOTSTRAP. A decoder circuit with bootstrapping capacitor beween the two cell transistors helps keep read operations fast despite lower voltages and wider supply tolerances.

have a much narrower operating margin, from 4.5 to 5.5 V.

An additional benefit of the lower operating voltage is that power dissipation is 25% to 50% less than that of comparable devices. At 8 MHz, active power is 49.5 milliwatts and standby is only 22.5 mW. At 1 MHz, active and standby power are 15 mW and 7.5 mW, respectively.

The low operating voltage was achieved with a variety of design improvements in both the read and write circuitry. Special bootstrap decoder circuits and a differential sense amplifier made it possible to keep reads fast despite the lower voltages and wider supply tolerances. In the first instance, the key was adding bootstrapping

Catalyst uses dynamic page-mode latching, opening the door to battery operation; the usual static latching needs a highly stable supply voltage that batteries can't supply

capacitors between the two transistors in the cell and between the decoder and the output to the word line (see fig. 2). "In present designs, when the supply voltage is too low, there is insufficient voltage across the enhancement-mode read transistor to allow it to switch reliably," Marya says. "With the addition of the bootstrap capacitor, sufficient charge is accumulated to stabilize the voltage during the read operation."

To prevent latchup that might be caused by a large instantaneous discharge of current from the capacitor onto the word line, which could occur during a write, the circuit also incorporates a predecoder to step down the discharge incrementally. The differential sense amplifier also boosts the EEPROM's reliability during reads. "In other designs, when the threshold voltage of a memory cell is set to the low state during a read, a very small current flows into the bit line, on the order of about 70 to 100 μA," says Marya. "Normally, in most 5-V designs there is sufficient voltage, on the order of 0.1 to 0.2 V, to trigger the sense amplifier." In Catalyst's 3-V design, however, the voltage change is only on the order of 0.02 V. With the use of a differential sense amplifier rather than a single-ended one, this minute voltage differential is magnified about 100 times to a level sufficient to trigger operation.

To achieve low-voltage programming, Marya says, Catalyst and Oki engineers made a number of improvements to the high-voltage switches and to the page-mode latches. Usually, the high-voltage switches are controlled by a single clock, so there is only a relatively narrow range within which the switch can sense the clock edge reliably. In 5-V devices, this occurs as long as the voltage is between 4.5 and 5.5 V. Below 4.5 V, such designs fail, switching erratically. Designers from the two companies solved this, he says, by going to a fail-safe switching scheme in which a dual clock is used, allowing the switches to operate reliably over the entire range from 3 to 7 V.

In the other critical improvement to the programming circuitry, company engineers went with a dynamic page-mode latching scheme, rather than the static configuration generally used, which is highly dependent on supply voltage for correct operation. "If the supply voltage varies outside a very narrow range of a few tenths of a volt, static latching no longer works," Marya says. "With a dynamic scheme, the page-latch threshold levels vary dynamically up and down as the supply voltage varies."

As with most other high-density EEPROMs, the 16-K-by-4-bit device also incorporates two redundant rows in the event of faulty array cells. This meant that it was necessary to modify the redundant cells to operate at lower voltages. Since they are located farther out on the array, they are served by longer lines, which means more capacitance or sensing lower-voltage signals. Here, the basic changes involved modifications to the interpoly oxide to take into account the lower voltage by reducing the load capacitance. Taking advantage of the differential-sensing scheme employed in the array, a special reset circuit selects a redundant word line when a faulty bit occurs in one of the word lines. The proprietary circuit works even when the supply voltage is as low as 1 V and consumes practically no power, Marya claims. The same scheme is also employed to select or key in EEPROM-based circuit elements to trim the programming voltage and the write cycle. *–Bernard C. Cole*

For more information, circle 481 on the reader service card.

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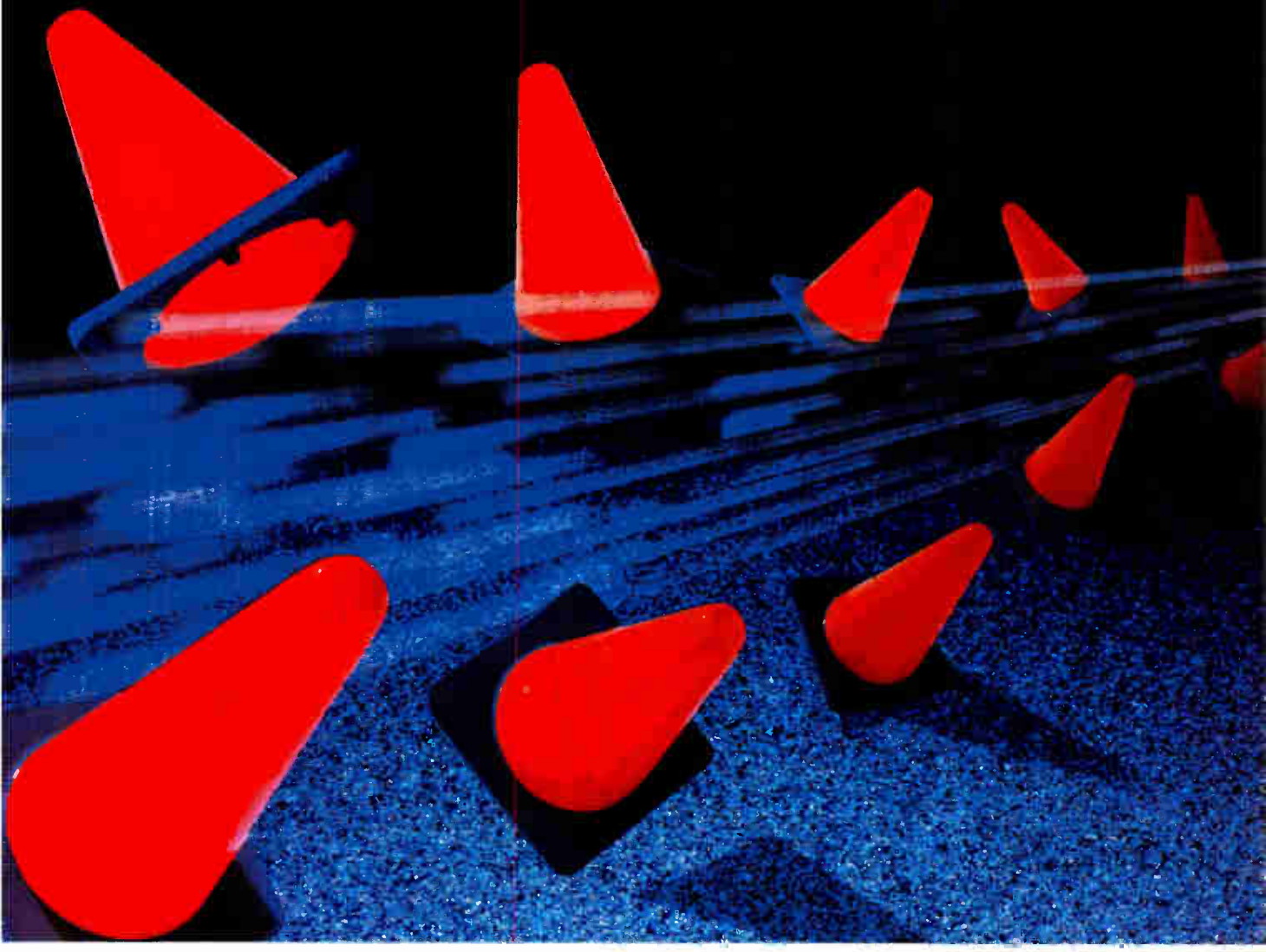

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WS57C128F	70 ns.	16k x 8 CMOS EPROM
WS57C256F	70 ns.	32k x 8 CMOS EPROM
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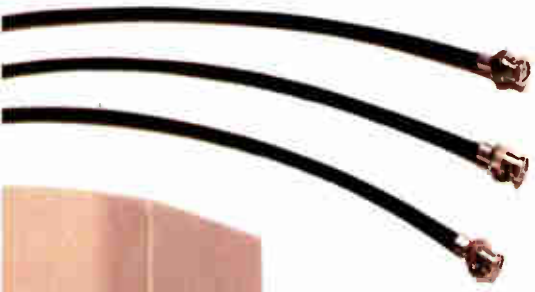

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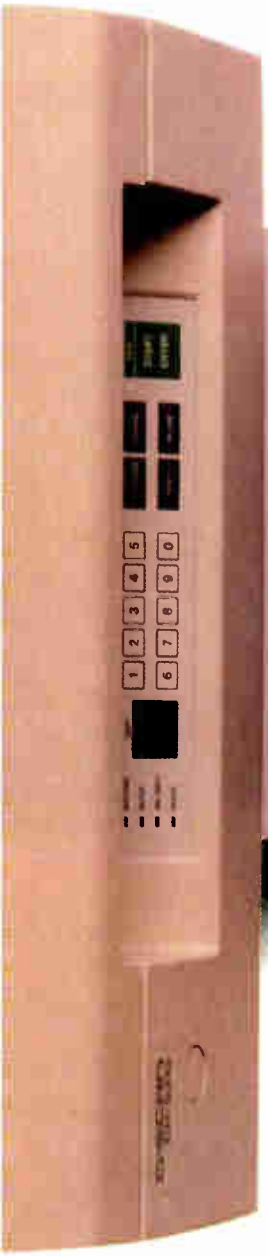

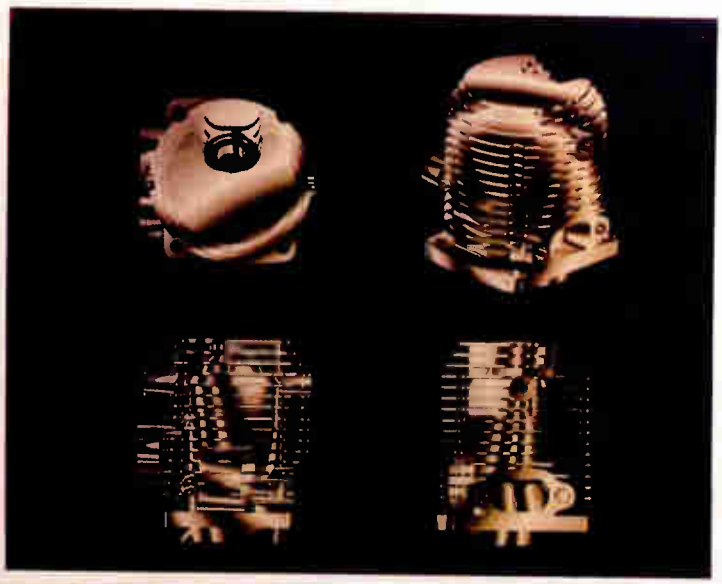

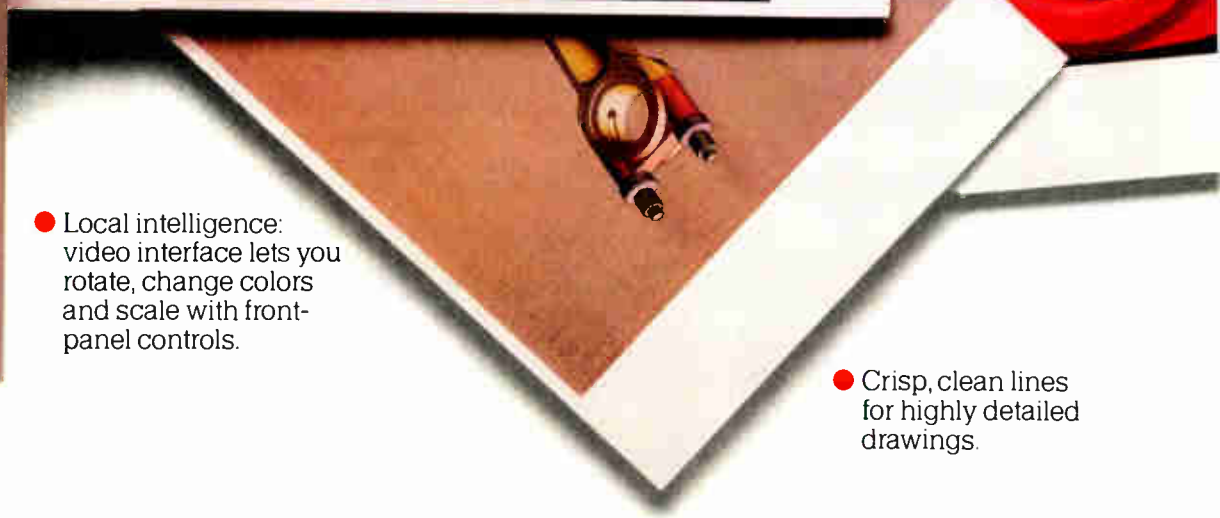

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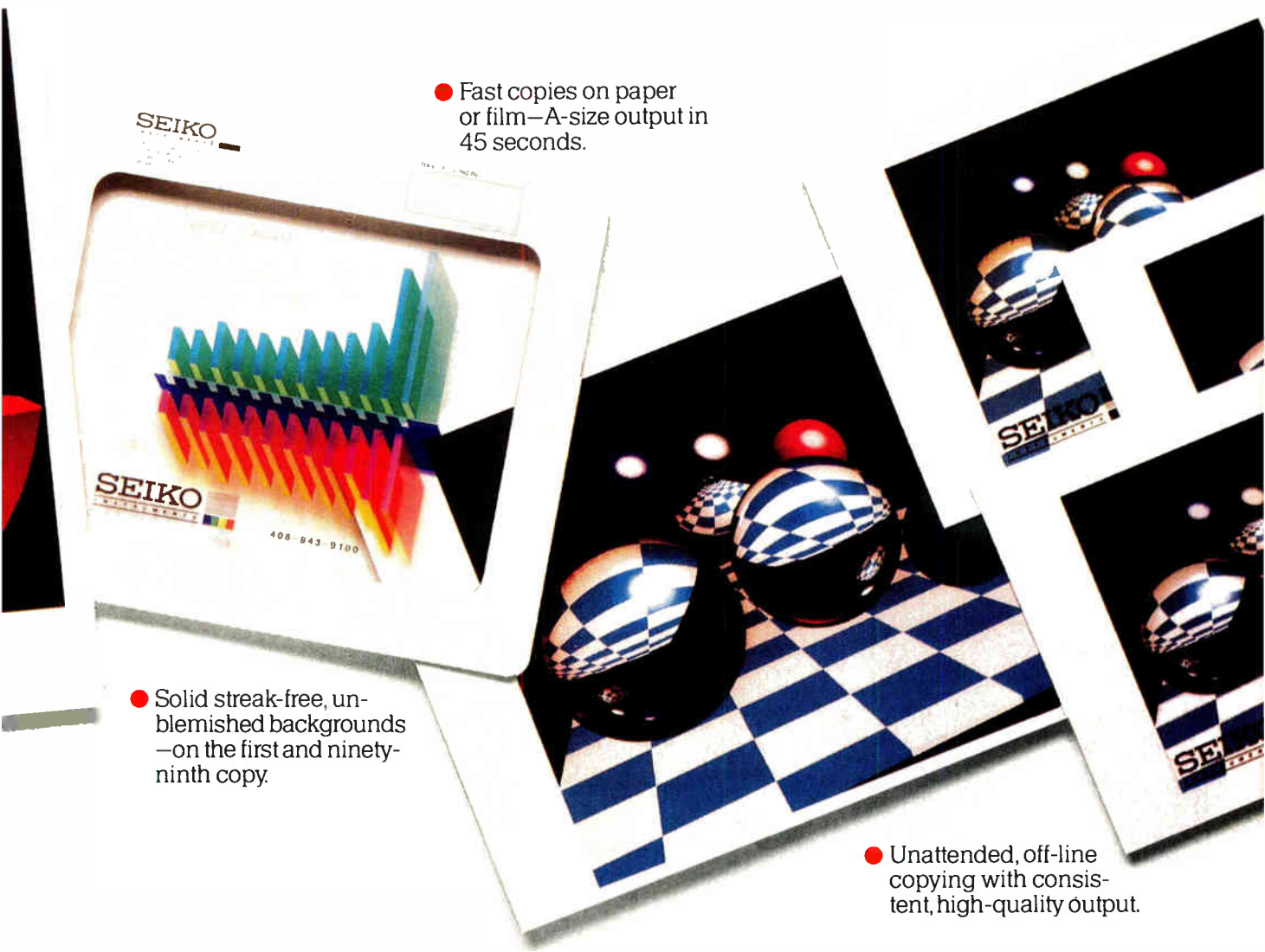

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A NEW KIND OF OSCILLOSCOPE FOR WIDEBAND SAMPLING

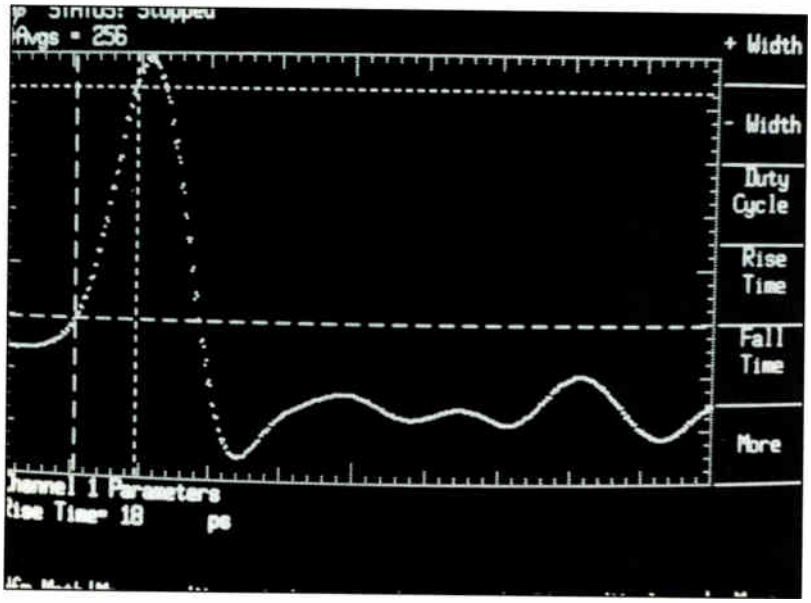
HP combines a 20-MHz digital scope and a network analyzer to sample repetitive waveforms with rise times as short as 17.5 ps, making a contribution in device modeling

by George Sideris

Designers of superfast digital and data communications systems have a new weapon to use in their struggle to capture and analyze wideband test signals. Hewlett-Packard Co. has come up with a new kind of oscilloscope for digital and pulsed-rf testing—one that combines a wideband repetitive-sampling capability with a time-domain network analyzer. The 20-GHz HP 54120T is tailored for such work as characterizing very high-speed digital circuits and nonlinear microwave devices and tuning their computer-aided-design models; developing transmission-line designs for printed-circuit boards, computer backplanes, and hybrid integrated circuits; and analyzing data communications channels.

The new sampling scope can analyze repetitive waveforms with rise times as short as 17.5 ps (see fig. 1). Just as important for precision work, it is designed for very high transient response, measurement resolutions to 0.25 ps and 32 μV, and virtually drift-free operation.

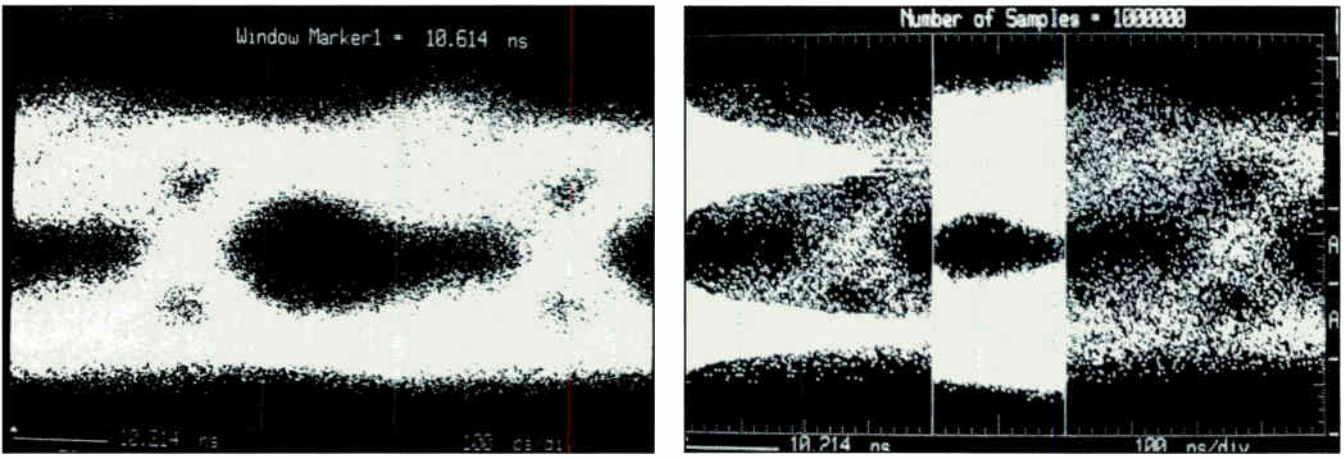
The 54120T makes it possible to characterize circuit designs with enough thoroughness and accuracy to compensate for hard-to-model parasitics, says Stanley R. Lang Jr., the scope's product marketing manager at HP's Colorado Springs (Colo.) division. One problem that needed solving, he says, is that high-speed components have parameters that conventional instruments can't measure. As a result, when prototype chips are characterized to tune computer-aided-design models, the models are still inaccurate, and chip-performance problems don't emerge until systems are tested. Gallium arsenide models in particular have suffered from such problems. "We think this machine will make significant contributions in device modeling," Lang says. Available this month, the 54120T costs $27,825.



1. FAST PULSES. In averaging mode, the HP 54120T displays waveforms with bandwidths to 20 GHz. This waveform has a rise time of 18 picoseconds.

To achieve the 20-GHz bandwidth, engineers at the Colorado Springs division redeveloped the classic sequential-sampling method, using circuitry from a microwave network analyzer to step up the performance. At the heart of this 20-GHz scope is a gallium arsenide bridge circuit adapted from one used in an HP network analyzer. Because the 54120T samples only repetitive signals, it can't capture one-shot transients.

For versatility, the 54120T has four simultaneous acquisition channels instead of the usual dual-trace inputs. This equips it for more kinds of logic and network analysis than a conventional scope. A reflectometer subsystem measures signal-path pa-



2. PATTERN ANALYSIS. The scope displays eye patterns (a) and provides histograms and statistical analyses (b) of specific areas. These statistical analyses of an eye pattern show both timing and amplitude variations for an area of the pattern.

rameters and helps the calibration subsystem null the effects of interconnections between scope inputs and measurement points. And new probes simplify measurement of high-impedance designs.

Besides automating many wideband measurements, the 54120T automates analysis. The scope has a persistence mode to hold fine details of waveforms on the display and to emulate variable-persistence analog scopes. In this mode, for instance, a user can build up a traditional eye pattern—a hole surrounded by gray shades created by the noise and jitter of multiple waveforms. But instead of estimating amplitude and timing variations, he can view histograms and statistical analyses of specific areas of the patterns (see fig. 2).

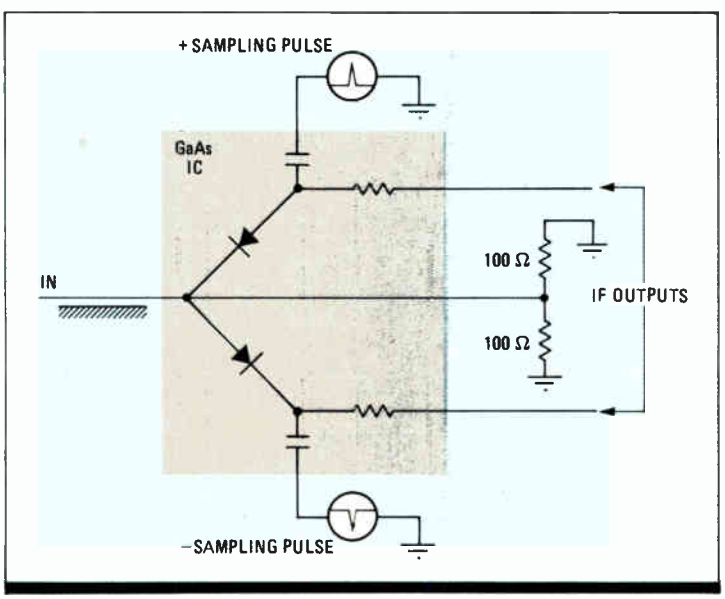
A 20-GHz digital sampling scope is not a breakthrough in speed. Earlier this year Hypres Inc., Elmsford, N. Y., introduced a 70-GHz system that samples up to four channels through liquid-helium-cooled Josephson-junction circuits [*Electronics*, Feb. 19, 1987, p. 49]. However, Hypres' system costs five or six times as much as the 54120T: $120,000 for a mainframe, plus $20,000 to $45,000 for input modules.

The 54120T costs $1,000 less than the widest-band configuration of the leading sampling scope—Tektronix Inc.'s dual-trace 7854 with 14-GHz sampling and reflectometer modules, but without accessories. However, the 7854 mainframe is also a 400-MHz real-time scope with digital waveform processing that can be used with other modules in other applications, whereas HP's 54120T reaches higher sampling bandwidth and precision by focusing sharply on its own applications range. Because the 54120T got its 20-GHz repetitive bandwidth by abandoning the single-shot mode that enables digitizers to capture a single waveform, it cannot compete with analog scopes in traditional real-time applications.

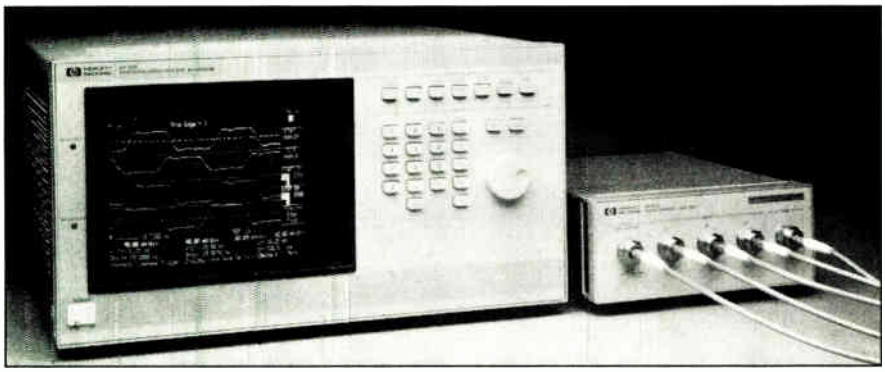
HP's goal was to be able to analyze pulse rise times, settling times, and step perturbations that in the past were too fast to measure. So it redeveloped an old, slow sequential-sampling architecture with microwave-analyzer circuitry. The circuitry lets the 54120T take a single sample at a time from repetitive waveforms and record the overall waveform as a straightforward sequence of data points at rates around 5,000 samples per second. Other HP digitizers reach single-shot bandwidths of up to 250 MHz with a billion samples/s, but they have lower resolution and don't go beyond 1 GHz in repetitive bandwidths.

Each channel in the 54120T samples up to 512 repetitive waveforms. The sampling rate is paced by the input repetition rate: an external trigger signal comes in at the start of each waveform, and the sampling time is delayed by a precision timing circuit. Sample timing is programmable, so automated measurement of mixed-waveform runs can be performed.

To remove unwanted skews from the measurements, delays between channels are adjustable in 1-ps steps. For measurements requiring precision stimuli, channel 1 contains a step-recovery-diode circuit that puts out 35-ps step pulses and offsets



3. KEY CHIP. A gallium arsenide step-recovery-diode bridge from an HP microwave network analyzer operates as a narrow-aperture sampling gate.



4. TWO BOXES. A separate unit containing the microwave circuitry, right, feeds low-frequency signals to the HP 54120T mainframe for processing.

these pulses from the sampling pulses.

Each channel's key sampling component is a gallium arsenide bridge circuit with matched step-recovery diodes, instead of the usual Schottky diodes (see fig. 3). Originally developed for the HP 8510A microwave network analyzer, which handles 26.5-GHz signals without external mixers, the bridge serves as a narrow-aperture sampling gate.

When triggered by the internal timing circuit, the bridge injects a charge proportional to the input voltage into the signal path, enabling an intermediate-frequency amplifier to sense the input level. HP says this architecture provides up to five times better transient response than other wideband designs, reliable triggering with arbitrary and other aperiodic waveforms, and almost drift-free operation. The channels have 80-dB isolation at 20 GHz. The circuitry's channel-reflection coefficient of 0.02 means a variation of only 1 Ω from the standard wideband impedance of 50 Ω.

The mainframe (see fig. 4) has a color-coordinated display, menu-driven functions, automatic scale setup, autocalibration, an independent recording memory in each channel, two display memories, and 10 setup memories. Programming conforms to the upcoming IEEE 488.2 software standard for test systems based on the IEEE-488 bus.

With four acquisition channels, a precision stimulus generator, and a time-domain reflectometer, the 54120T can perform nodal measurements on all types of binary logic and can analyze two-port networks lacking ground-referenced inputs. As a scope, for instance, the instrument can measure waveform rise times, duty cycle, and electrical parameters and can do the corresponding statistical analyses. Network measurements include signal-path reflection, impedance, gain, attenuation, and propagation delay, and the on-off envelope characteristics of such nonlinear microwave devices as step-recovery, Gunn, and tunnel diodes. Such measurements are made in the time domain with the aid of an internal fast-Fourier-transform processor that also filters at any desired bandwidth.

The bandwidth changes to suit the mode. It is 12.4 or 20 GHz in an averaging mode and 12.4 GHz in the persistence mode. With averaging, the points blend into a single waveform. At 12.4 GHz in the averaging mode, the noise floor is only 35 μV, allowing noise in the system under test to be measured with high accuracy. In the persistence mode, an extra screen memory stores and displays every sample so that the user can see fine signal details.

The basic 12-bit analog-to-digital conversion provides 250-μV vertical resolution. Averaging extends conversions to 14.4 bits and resolution to 32 μV. Timing accuracy is 10 ps, the same as with wideband analog scopes. However, the sampling method keeps the error consistent from point to point on the display, so that rise times and other signal timings between points marked with cursors can be measured with 0.25-ps resolution. □

For more information, circle 482 on the reader service card.

FROM CONCEPT TO PROTOTYPE IN TWO YEARS

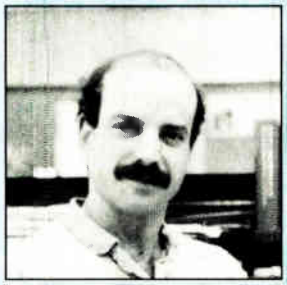
In the last days of 1984, Kenneth Rush, a Hewlett-Packard Co. development engineer, and Frederick Ramsey, research and development manager, had just completed work on the HP 54100 digital oscilloscope. Ramsey suggested to Rush that HP needed to come out with another digital scope that offered higher bandwidth and higher vertical resolution.

Ramsey went on with his job as R&D manager, but Rush carried on with the idea for the product. When he presented the concept of the proposed new digital oscilloscope to HP management, he was given three months to study the market need for the product. HP management was impressed enough with the results to fund the project with a couple of million dollars. By the end of 1986 Rush and his team had a fully functional prototype of the new HP 54120T.

About this time, Michael Karin joined the team as project manager. In the middle of 1986, John Wilson, a product marketing engineer, was brought on board to define the scope's market. The obvious users were logic designers who were building circuits with very high clock rates, but Wilson also found niches in the microwave arena, where conventional network analyzers were inadequate.

By the end of July, the group plans to have production units of the 54120T ready to ship. *–Jonah McLeod*

KEN RUSH



MIKE KARIN

JOHN WILSON

TI'S TRENCH TECHNOLOGY MOVES INTO THE FACTORY

After getting control of this tricky etch process, TI turns out 1-Mbit DRAMs with trench capacitors; researchers use it to boost PROM densities and isolate bipolar devices

When builders want to squeeze more out of a piece of real estate, they have only one way to go: up. But developers of silicon real estate have been going in the other direction. To pack more functions into a given VLSI area, device designers are working on a three-dimensional vertical-integration process called trench etching, in which holes or grooves are etched down into a chip's substrate and used for either isolation or device fabrication.

But trench etching hasn't yet moved into the factory, because it has been too tricky a process to meet the throughput demands of full production. Now, however, researchers at Texas Instruments Inc. have come up with a new technique that provides better control of the etch process, allowing them to bring trench technology to the VLSI production line for use in 1- and 4-Mbit dynamic random-access memories.

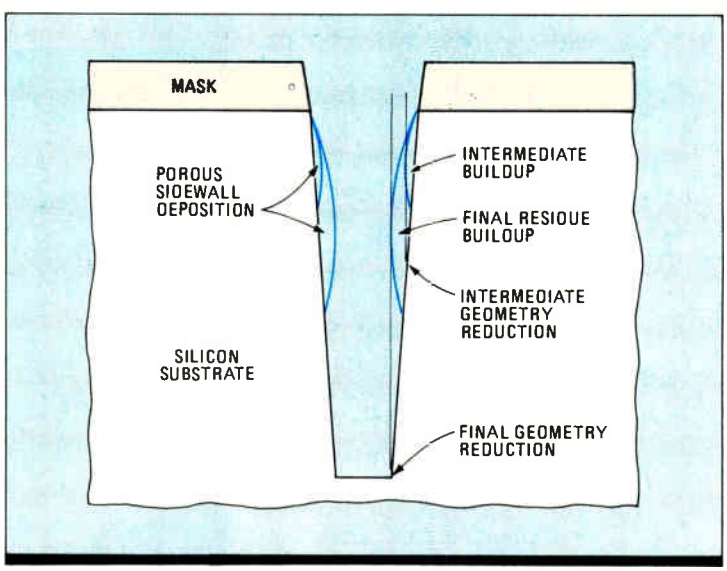
The additional chip area provided by trenching can be used to construct simple active devices or to establish area-efficient device isolation without the latchup-inducing encroachment problem inherent in conventional isolation techniques. A trench can also be used to place an insulating barrier or a conductive interconnect between a chip's surface and buried layers.

The Dallas chip maker is already turning out 1-Mbit DRAMs with trench capacitors. A forthcoming 4-Mbit DRAM will go even further, placing a storage capacitor, a transfer gate, and a contact into the same trench. What's more, TI researchers recently achieved improved programmability, better device isolation, and reduced parasitic capacitance in erasable programmable read-only memories by using a novel positioning of trench isolation between bit lines and transistors; this approach should move bit-line spacing below 1 μm. The researchers are also using trenches to isolate devices on advanced bipolar circuits.

Several problems have hampered trench technology, including undercutting of the mask and grooving at the trench bottom during the etching process. Undercutting promotes the formation of voids during subsequent refill of the trench, and contaminants can easily get into the voids and cause reliability problems. Grooving, or the formation of a V-shaped structure on each side of the trench bottom, can degrade the dielectric integrity of a trench capacitor and can promote stress-related silicon defect densities during thick thermal oxidation.

TI's selective sidewall deposition technique counters these problems by precisely controlling the profile of the trench as it is etched so as to achieve the surface texture and dimensions required to make trench technology a viable production process. TI uses a dry-etch process and produces a trench that has straight, unbowed walls and is free of defects on its floor.

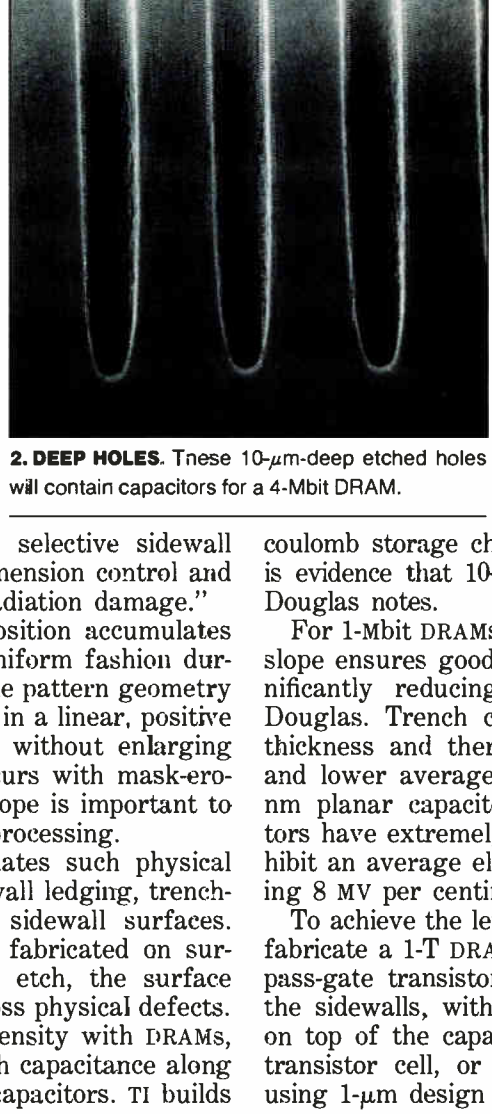
The new technique involves selective deposition of etch products on the trench's sidewall near the mask/silicon interface by two means: controlled forward sputtering of the mask material and condensation of gas-phase precipitates formed in the reactor. The deposits protect the upper sidewall from erosion (see fig. 1) and are



1. PROFILE. In Texas Instruments's trench-etch technique, etch products are selectively deposited on the trench sidewalls to protect them during deep etching.

removed in the mask wash.

Selective sidewall deposition not only eliminates many physical defects, but also yields trenches that have controllable, reproducible, straight sidewalls that are positively sloped at a steep angle. "The ideal trench profile for a 1-Mbit DRAM consists of smooth sidewalls, an 87° positive sidewall slope, and a hemispherical bottom," says Monte Douglas, senior member of the technical staff at TI's Semiconductor Process Laboratory in Dallas. "Such trenches can be successfully subjected to refill processing without sacrificing line-width control," he says. "In addition, selective sidewall deposition ensures critical dimension control and protects the sidewall from radiation damage."



2. DEEP HOLES. Tnese 10-μm-deep etched holes will contain capacitors for a 4-Mbit DRAM.

The selective sidewall deposition accumulates in a slow, continuous, and uniform fashion during trench etching, causing the pattern geometry to slowly shrink. This results in a linear, positive slope on the sidewall profile without enlarging the pattern geometry, as occurs with mask-erosion techniques. A positive slope is important to ensure reliable trench refill processing.

The TI process also eliminates such physical defects in the trench as sidewall ledging, trench-bottom cusping, and rough sidewall surfaces. Since active devices may be fabricated on surfaces created by the trench etch, the surface texture must be devoid of gross physical defects.

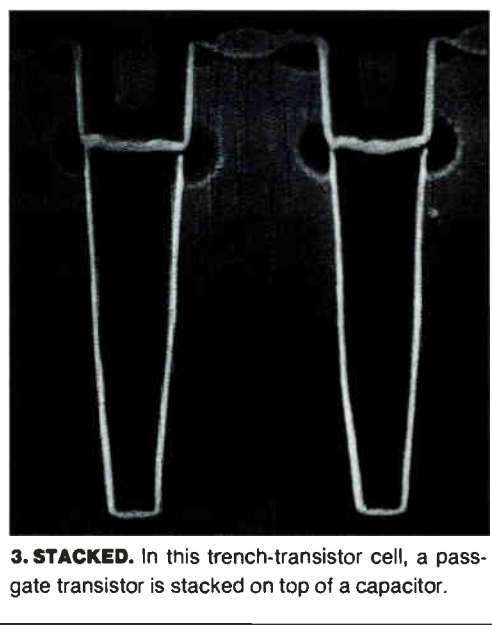
In order to achieve high density with DRAMs, it is necessary to achieve high capacitance along with minimum geometry in capacitors. TI builds high-capacitance trench capacitors by etching a deep trench (see fig. 2); the deeper the trench, the greater the capacitance for a given cell size. With the TI process, the trench can be made deep enough to reach all the way down through the lightly doped epitaxial layer, where active devices are formed, and into the heavily doped substrate. A trench that reaches this region must have a particularly well-formed bottom without grooves or any other imperfections that can cause breakdown.

Dynamic RAMs are the frontier of 3-d device fabrication and of trench technology in particular. TI's 1-Mbit DRAMs have trench capacitors with 1-T (one-transistor) cell areas that are about 20 μm^2. The 4-Mbit memory arrays will likely break through the 10-μm^2 barrier by allowing the pass-gate transistor as well as the storage capacitor to share the same trench.

For 1-Mbit DRAMs, trenches let designers achieve a chip size below 100,000 $mils^2$—a very high packing density for memory arrays. A trench capacitor is an attractive alternative to a planar capacitor, which requires a 10-nm oxide thickness to provide the 250-to-300-femtocoulomb storage charge needed in DRAMs. There is evidence that 10-nm oxides may be unreliable, Douglas notes.

For 1-Mbit DRAMs, a trench with an 87° positive slope ensures good refill processing without significantly reducing a cell's capacitance, says Douglas. Trench capacitors use a 15-nm oxide thickness and therefore exhibit higher leakage and lower average breakdown voltage than 15-nm planar capacitors. However, trench capacitors have extremely low defect densities and exhibit an average electric-field breakdown exceeding 8 MV per centimeter.

To achieve the level of integration necessary to fabricate a 1-T DRAM cell for a 4-Mbit DRAM, the pass-gate transistor and capacitor are built into the sidewalls, with the transistor being stacked on top of the capacitor (see fig. 3). This trench-transistor cell, or TTC, yields a 9-μm^2 1-T cell using 1-μm design rules.



3. STACKED. In this trench-transistor cell, a pass-gate transistor is stacked on top of a capacitor.

The profile requirements for the trench transistor are very similar to those for trench capacitors, but the fabrication techniques must be more refined. The aspect ratio, for example, is quite high, since an 8-μm-deep trench must be etched into a 1.3-by-1.5-μm aperture. Profile control is more difficult, because here the trench is a square hole, as opposed to a long trough. Sidewall angles must be tailored: the upper 2 μm that make up the transistor region have an 85° slope to prevent refill voids, whereas the lower 6-μm capacitor region requires an 89°

slope, ±0.5°, to enhance capacitance and to prevent sharp terminating points. A capacitor formed this way exhibits well-behaved electrical characteristics for gate and drain voltages above 5 V, Douglas says.

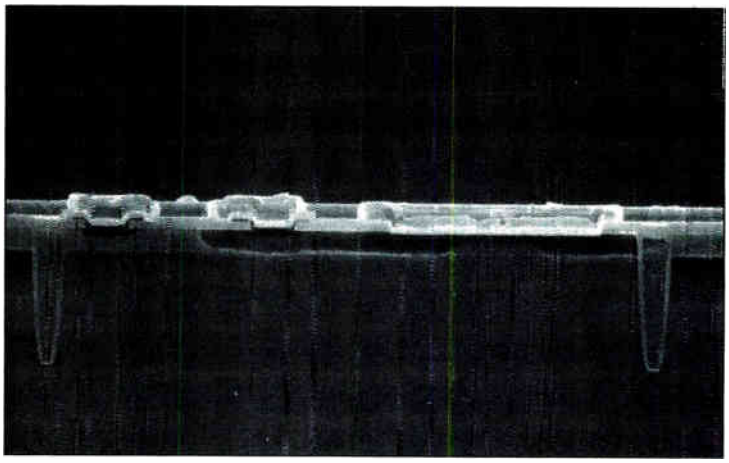
Advanced bipolar devices use trenches mainly for device isolation. As with DRAMs, the aspect ratio must be high: a 15-μm depth for a 2-μm trench width or an 8-μm depth for a submicron width. Smooth sidewall surfaces with ±1° slope control are required. Isolation trenches lay out as long slots, rather than as "postholes," and are usually easier to etch. Whereas tank-to-tank spacing of 10 μm is currently in production with oxide isolation, trench isolation allows this dimension to shrink to 2 μm and substantially increases the packing density of bipolar devices. Trench isolation also eliminates the need for a channel stop under the field oxide, significantly reducing the collector-to-DUF (diffusion-under-film) capacitance (see fig. 4).

In another isolation application, a 15-μm-deep trench-isolated SIMOX (separation by implanted oxygen) structure can replace standard dielectric isolation to achieve higher packing density and increased immunity to radiation effects.

To obtain reasonable throughput on a production line, the etch rate in the trench process must be at least twice as fast as in other processes, since the vertical depth to be etched is some 5 to 50 times greater than the thickness of films etched in conventional processes. This fact has demanding ramifications in mask selectivity, critical-dimension control, and other variables.

With trench etching, surface texture and damage considerations during production are more significant than in other dry-etch processes, because the trench-etched surface is generally destined to be an active silicon area, or at least a turned-off parasitic device in the final circuit. Newly created surfaces must be suitable for building active-device components. Because of the highly directional etch conditions, micromasking and other effects contribute to surface asperities. Without sidewall deposition, ion bombardment would result in silicon lattice damage.

When it came to choosing a means of production, the TI researchers found a single-wafer reactor to be far superior to batch reactors for trench-etch processing. "Batch reactors are more expensive than single-wafer systems; they exhibit poor selectivity to photoresist as an etch mask; and they are plagued by large etch-rate and trench-profile nonuniformities," says Douglas. "In addition, they are difficult and somewhat dangerous to clean and, as wafer size increases, it becomes more of a fiscal liability to commit a whole batch of wafers to a single run." Not only do the long run periods make it it difficult to develop a process in a batch reactor, but it is also expensive and time-consuming to requalify all wafer positions on a batch system, he adds. These require exhaustive analysis with a scanning electron microscope.



4. DENSE BIPOLAR. Tank-to-tank spacing in bipolar devices can be reduced from 10 μm with oxides to just 2 μm with trenches.

TI researchers chose to engineer their own single-wafer reactive ion etching reactor. This reactor etches silicon faster than 2.5 μm per minute and has better than 150 : 1 silicon-to-oxide and 40 : 1 silicon-to-photoresist etch-rate ratios, all with good profile control. □

THIS CHEMIST GETS DOWN INTO THE TRENCHES

It's been a life in the trenches, so to speak, for much of Monte Douglas's past five years at Texas Instruments Inc. As a senior member of the technical staff at TI's Semiconductor Process Laboratory in Dallas, he's pioneered techniques for etching deep silicon trenches for advanced device applications in dynamic random-access memories, advanced bipolar devices, erasable programmable read-only memories, and CMOS parts.

Douglas, 31, holds a BS in chemistry from Nebraska Wesleyan University and a PhD in physical chemistry from Rice University. He has more than 15 patents issued or pending. At TI, he is also involved with the development of new plasma chemistries and in designing reactor hardware for dry etching of a variety of new materials that will be required for ultra-large-scale integration. He is currently at work on dry-etch techniques for salicide local-inteconnect technology for advanced static RAMs.

MONTE DOUGLAS

Douglas's work in trench technology is an essential part of a forthcoming 4-Mbit DRAM and will play a big role in future ultra-large-scale-integration devices, says Greg Armstrong, associate director of the lab. "The problem in big DRAMs is to get sufficient capacitance in a reasonably sized chip. The only way to do that is to go vertical."

Trenches are already being used in TI's production 1-Mbit DRAMs. "For these chips, the trenches only have to be 3 to 4 μm deep," says Armstrong. "At 4 Mbit, they'll have to be 7 to 9 μm. Control of the trench profile at that depth is a real challenge." But he believes the selective-deposition technique TI is successfully using to make its 1-Mbit DRAMs gives the company an advantage when it comes to that challenge.

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WHAT'S NEW IN INTERCONNECTIONS?

THE IC SOCKET GETS NEW LIFE FROM THE VLSI CHIP

A variety of complex sockets are being developed to handle expensive VLSI chips, avoiding the risks of soldering ICs with 100 leads or more directly to a pc board

by Jerry Lyman

The integrated-circuit socket is grabbing the spotlight in interconnections, thanks to the arrival of production VLSI chips with more than 100 leads. Up until recently, IC sockets were used mainly to make it easier to repair or replace packages with few leads in systems that needed frequent field servicing or hardware updates. Now designers need a way to overcome the risks in soldering multileaded ICs directly to a printed-circuit board. So packaging designers are devising a variety of complex sockets to house expensive VLSI chips with hundreds of leads on tightly packed centers, typically 25 to 50 mils.

Packages with many leads are difficult to solder onto a fine-line pc board. And removing such a device without damaging an expensive pc board is even harder when it is soldered in place. This is where complex sockets play a leading role. Sockets allow easy modification of a board because a gate array or other type of programmable ASIC can be simply replaced with an updated device.

The special high-temperature sockets required for burn-in or high-temperature screening of ICs represent another large application. And designers are using new materials such as engineering thermoplastics and liquid-crystal polymers to overcome the temperature and mechanical stresses of surface mounting, a technique that is growing in popularity. These new sockets will take up more space than a soldered IC, but in the long run they will also result in increased board yield.

Most IC sockets are used by the computer-manufacturing industry, which in 1986 accounted for 72% of all sockets sold in the U. S. Computer manufacturers should continue to dominate socket sales (see table, right). And their growing usefulness will keep IC sockets a growing market segment. Last year, they made up 6%, or $247 million, of the nearly $4 billion worth of connectors used in the U. S., and the market for sockets is projected to grow to $300 million by 1991 at an average annual growth rate of 4% (see table, next page).

Packaging designers and socket manufacturers currently face a bewildering array of IC packaging choices, which in turn leads to a variety of socket types. Packages include the dual

COMPUTERS LEAD U.S. CONSUMPTION OF IC SOCKETS

Electronic equipment category	1986 ($ millions)	1991 ($ millions)	Average annual growth (%)
Electronic			
Computer	178	219	4.2
Communication	26	35	6.7
Government/military	18	17	−1.3
Instrumentation	6	7	1.3
Industrial	6	6	0.3
Consumer	3	5	6.1
Business/retail/education	3	3	1.3
Electrical/industrial			
Transportation	4	5	4.2
Machinery	3	3	4.3
Total consumption	**247**	**300**	**4**

Dollar figures have been rounded to the nearest whole number

SOURCE GNOSTIC CONCEPTS INC

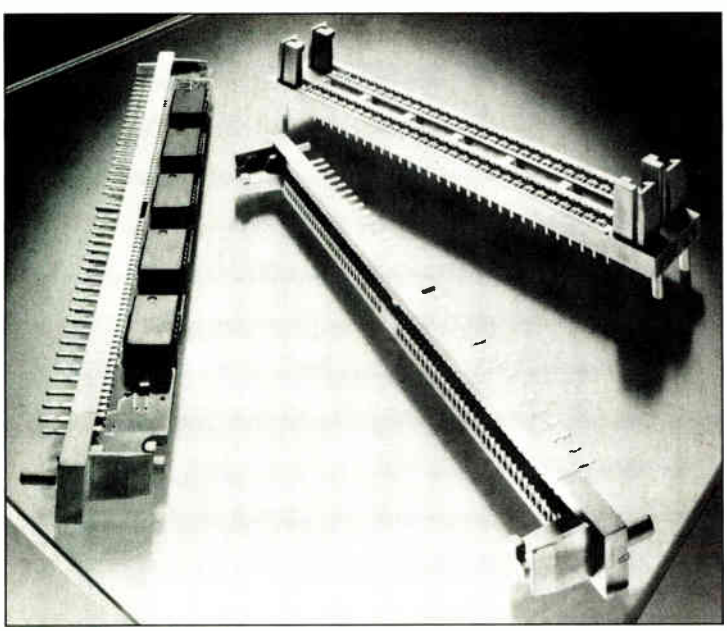
STEADY GROWTH MARKS U.S. CONSUMPTION OF CONNECTORS AND IC SOCKETS

Connector type	1986 ($ millions)	(%)	1991 ($ millions)	(%)	Average annual growth (%)
Printed-wiring	1,095	29.2	1,462	29.9	6.0
Cylindrical	814	21.7	1,064	21.7	5.5
Specialty	525	14.0	693	14.2	5.7
Rectangular	501	13.3	568	11.6	2.6
Coaxial	269	7.2	332	6.8	4.3
Planar-cable	258	6.9	327	6.7	4.9
IC-socket	247	6.6	300	6.1	4.0
Fiber-optic	45	1.2	151	3.1	27.3
Total	**3,753**	**100**	**4,897**	**100**	**5.5**

Figures have been rounded

SOURCE GNOSTIC CONCEPTS INC

in-line package, in many variations; the small outline IC, or SOIC; the single in-line package, or SIP; the zig-zag single in-line package, or ZIP; the single in-line memory module, or SIMM; a variety of leaded and unleaded chip carriers; the pin grid array, or PGA; and the plastic quad flat pack, or PQFP. And the choice of a socket is further complicated by the fact that some of the latest high-pin-count ICs, such as microprocessors or some of their support chips, are available in as many as six different package types, from the old faithful plastic DIP to the complex multilayered leadless ceramic chip carrier. Companies are also supplying sockets with integral bypasses, to increase performance, and adapters, to allow transition from one packaging format to another.



1. SIMM SOCKET. Amp's single in-line memory module socket is made from liquid-crystal polymer, assuring strong, durable ramps and latches.

There is also considerable activity on the lower end of the socket scale, in sockets with lower pin counts such as the DIP, SIP, ZIP, and SIMM. The standard plastic DIP with package widths of 900, 600, 400, and 300 mils and with leads on 100-mil centers dominates the packaging world. Thanks to the Japanese IC industry, a new variation of the standard DIP has appeared: the shrink-DIP, a space-saving package with 400-, 600-, 750-, and 900-mil widths and leads on 70-mil centers. Like the standard DIP, the shrink-DIP is limited to 68 leads.

Although a variety of sockets for the standard DIP are readily available in the U. S., sockets for the shrink-DIP are just coming on the market. So far, Advanced Interconnections, Amp, Augat, Burndy, the Garry Electronics division of Brintec, and Thomas & Betts can supply sockets for the new DIP on 70-mil centers. Many other companies are planning to come out with such a unit.

The popular gull-wing SOIC and its J-leaded version, the SOJ, are rarely socketed. Both surface-mountable units have leads on 50-mil centers. The SOIC is socketed only when it has to be burned in. This small plastic DIP-like package normally houses low-cost "jelly bean" analog and digital chips. No production sockets are available for the SOJ, used by Texas Instruments Inc. and several Japanese companies for 1-Mbit DRAMs.

However, burn-in sockets for the SOJ are available from several companies, among them Amp, in Harrisburg, Pa.; TI's Attleboro, Mass., operation; 3M's Textool Test and Interconnection Department in Grand Prairie, Texas; and Yamaichi in Japan. These special sockets are made with high-temperature thermoplastics and accept the J-leaded packages, which has leads on 50-mil centers. The socket leads, with special high-temperature contact materials, are through-hole types on 100-mil centers.

Vertical packaging of IC chips and modules has created another class of sockets for the SIP, ZIP, and SIMM. The SIP, which normally consists of a small ceramic or glass-epoxy substrate with a leadframe on one side, can hold memories in chip carriers or even passive networks. SIP sockets with leads on either 50- or 100-mil centers are available from most connector or socket companies. One interesting variation made by Garry Electronics is a 40-lead SIP socket that may be tailored by the designers themselves to whatever smaller size they need.

Sockets will soon be available from U. S. firms for the ZIP, a semiconductor memory in a single

in-line plastic package with staggered leads on 100-mil centers that several Japanese companies started delivering late last year. Advanced Interconnections, Amp, Augat, and Garry are working on these sockets. Molex Inc. of Lisle, Ill., was first to produce a SIMM connector for a vertical package, a configuration originally requested by Wang Laboratories Inc. and developed by TI. The SIMM consists of a small pc board with arrays of memory chips in plastic leaded chip carriers on both sides. The input and output leads of the module are plated-edge card fingers placed along one of its long dimensions on 50- or 100-mil centers. Now Amp Inc. (see fig. 1) and Burndy Corp. of Norwalk, Conn., are also producing these sockets, which can have up to 68 leads. Molex is already receiving requests for sockets designed to accept SIMMs with edge-card fingers on 25-mil centers.

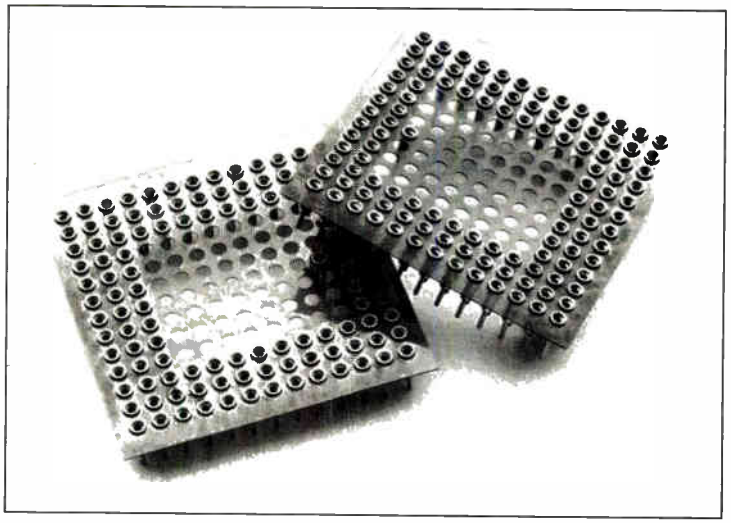
Another alternative for high-density packaging is the plastic leaded chip carrier, but its practical maximum is 84 leads. Nearly all the connector-manufacturing companies now have sockets for this package, which has J-leads on 50-mil centers. The only question for a potential user is whether to use a surface-mount or through-hole version of the socket. So far, about 80% of all plastic-leaded-chip-carrier sockets are being through-hole mounted. Nearly all the surface-mounted versions use the gull-wing configuration, usually on staggered 100-mil centers, for the socket leads.

PIN GRIDS OR FLAT PACKS?

When input/output requirements exceed 100, packaging designers must go to the pin grid array, which is often socketed, or choose from the Japanese plastic quad flat pack or the new bumpered PQFP with gull-wing leads on 25-mil centers [*Electronics*, Oct. 30, 1986, p. 36] recently approved by Jedec. The PGA, a rectangular plastic or ceramic substrate in which a grid of pins are mounted, normally has its pins on 100-mil centers. Molded and glass epoxy sockets for PGAs are readily available.

One new approach to PGA socketing, called the Peel-A-Way system, originally developed by Advanced Interconnections Corp. of West Warwick, R. I., and now used in Augat Inc.'s PKC series of sockets, is based on embedding a PGA pattern of socket terminals in a polyimide film (see fig. 2). The socket terminals are then placed into the pin-grid hole pattern on a pc board and are wave soldered. After the soldering, the polyimide film can easily be removed, resulting in a low-profile PGA socket that is easily inspected.

This technique has been extended by both Advanced Interconnections and Augat, of Mansfield, Mass., to include a large sheet of film with pin patterns of either multiple PGAs or a mix of PGAs and

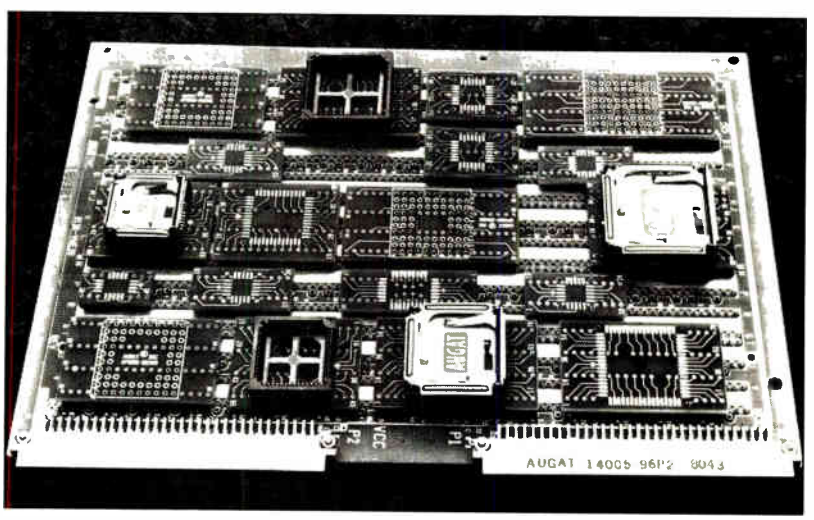


2. PIN PATTERNS. Augat's PKC series has PGA pin patterns in polyimide carriers. After soldering, the film is removed.

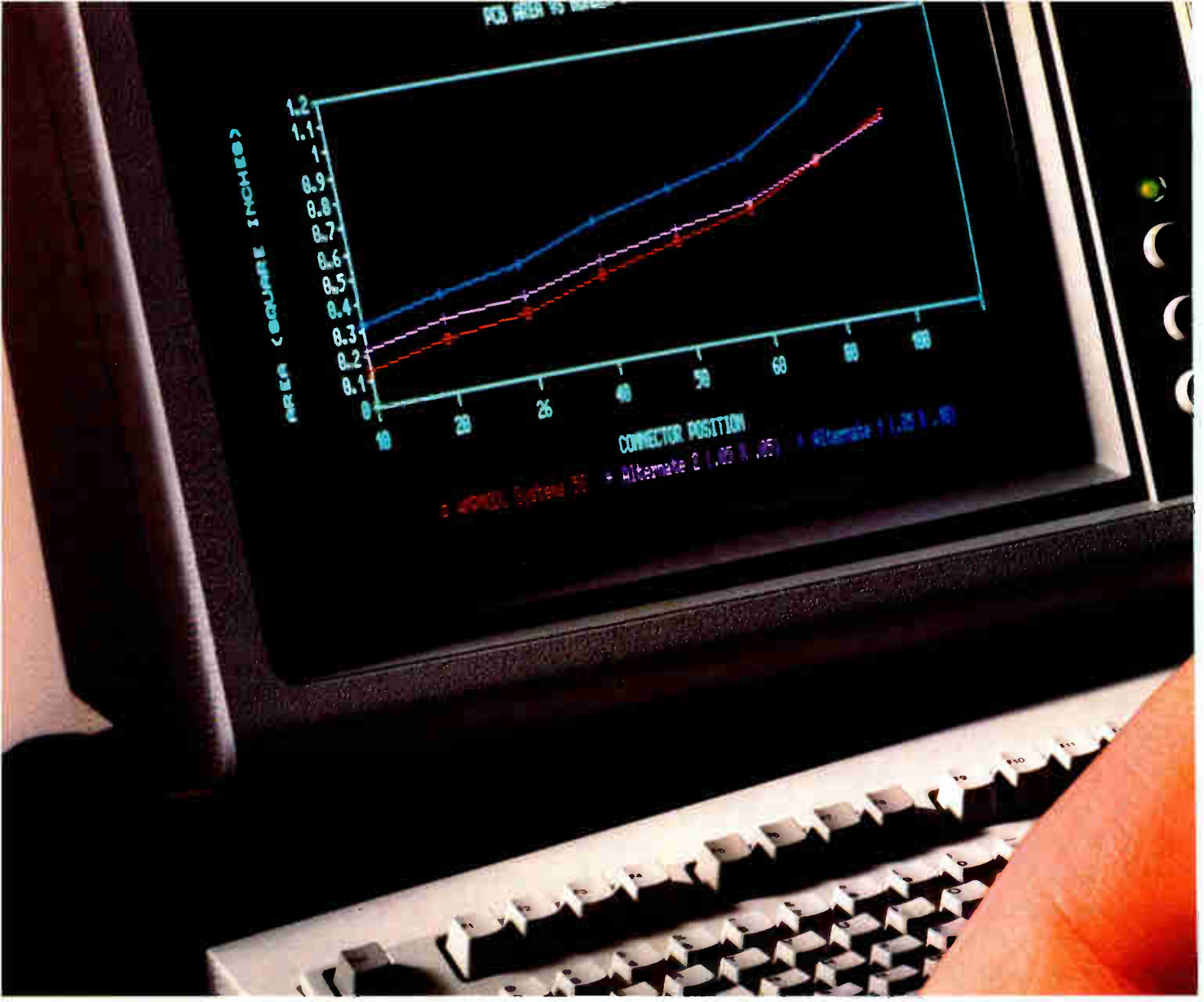
DIPs. Customers simply provide either a drawing or computer-aided-design data on their boards, and the pin-bearing film is fabricated allowing all the sockets to be inserted in one operation.

The bumpered PQFP recently approved by Jedec, which has an I/O range of 52 to 244 leads, will have the interconnection density to compete successfully with the PGA. That is why Intel, Motorola, National, and TI are all looking into producing products in this package, and why Amp, Textool, Wells, and Yamaichi are designing production and burn-in sockets for it.

Sockets with integral bypasses are part of a recent trend to take advantage of socket space to enhance performance. Because dynamic random-access memories often must be bypassed or decoupled from their power supplies, this new class of sockets with built-in ceramic bypass capacitors has been developed. The closer the bypass capacitor is to the chip's power leads, the more effective the bypass. DIP sockets with this feature are available from Amp, Augat, and

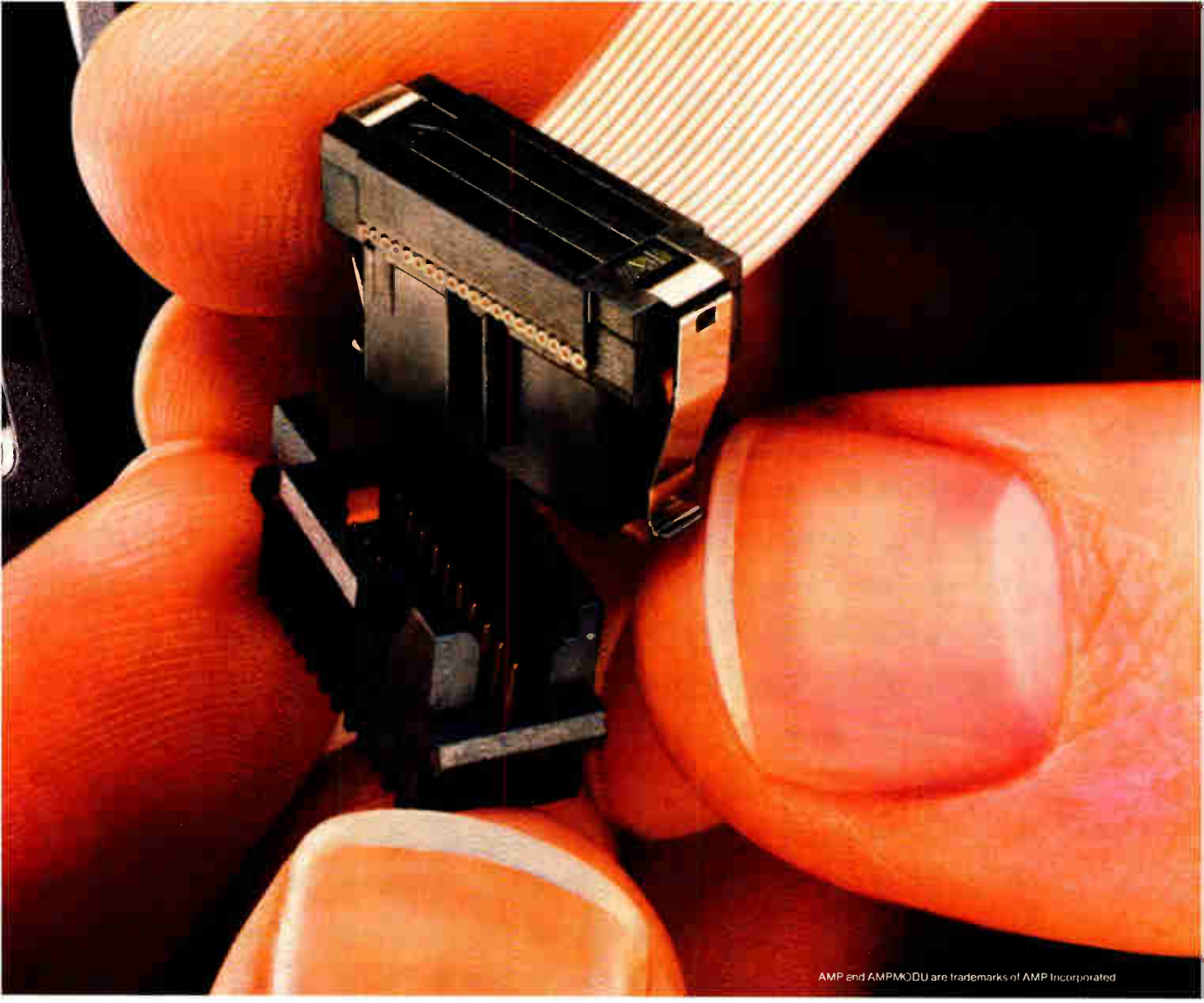


3. ADAPTERS. A small, leaded adapter board allows nonstandard components to be mounted on standard IC panels or pc boards.



An idea this small is no small idea. Especially in a system this big.

Circle 83 on reader service card



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Unique design (such as connector latch hardware on the *cable* side) occupies the least pc board space of any connectors in this class, including .050 x .050 types. For instance: 2 x 25 position shrouded headers occupy 1.5 x .284 inches² of surface; parallel boards mate with inside faces a mere .450 inches apart.

Along with selection, you also get the productivity features you expect from AMP: simple mass termination, robotic handling features, high-temp housings, selective gold plating. And, of course, outstanding quality and reliability.

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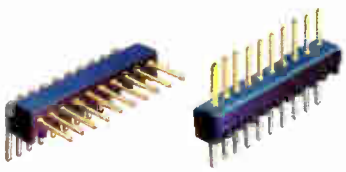
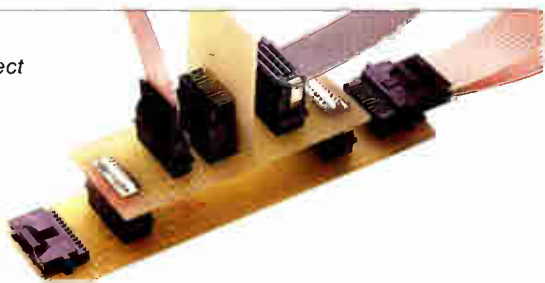
AMP Interconnecting ideas

Comprehensive high-density interconnect system: .050 x .100 connectors in a range of styles, to meet a variety of needs including board-to-board interconnect in both parallel and right-angle configurations.





Thomas & Betts, among others. This configuration is also spreading to other socket types: for example, Amp has a ZIP socket with a built-in capacitor, and Advanced Interconnections and Garry supply PGA sockets with multiple built-in bypass capacitors.

Another unusual product that some socket manufacturers are beginning to furnish is the adapter that allows a transition from one packaging format to another. For example, a designer might want to mount one or two surface-mounted devices to a board that has only through-holes. The adapters are small epoxy-glass substrates (see fig. 3) capable of handling surface-mounted parts (leadless chip carrier, plastic leaded chip carrier, or sockets for these devices) or PGA packages. They interface with standard wire-wrap panels or a pc board with plated through-holes. Using the adapter, a company can preassemble its oddball component to an adapter and then wave-solder the adapter to a conventional board. Although only Advanced Interconnections and Augat currently supply these interface adapters, the demand for them should continue to grow as the choices of IC packages increase.

The demand for adapters, which allow a transition from one packaging format to another, should continue to grow as the choices among IC packages increase

Most surface-mount boards contain a mix of surface-mountable components and some through-hole components, often made up of sockets and pc-board connectors. Mechanical designers most often select conventional board connectors for surface-mounted applications to cut costs and because they lack faith in the mechanical stability of surface-mount connectors. A surface-mounted connector is held to the board mainly by its soldered leads and a few molded pins or screw holddowns. Most designers believe that the severe mechanical loading of multipinned connectors overstresses a surface-mounted connector.

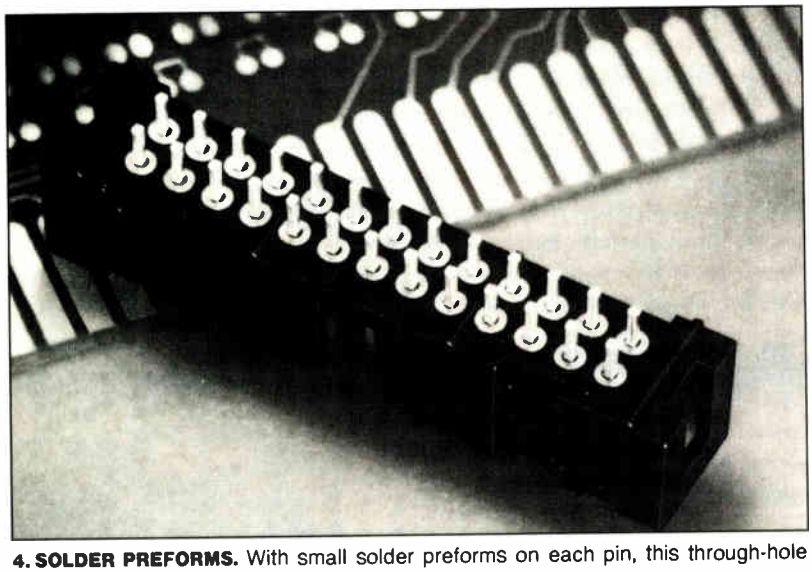
Usually, the assembly of a through-hole board would require either hand or wave soldering and some form of reflow soldering. Application of an old technique—the use of solder preforms—allows a board manufacturer to eliminate the wave-soldering step and do all his soldering by one of the two reflow methods. The result is a mechanical connection done with the speed and economy of infrared or vapor-phase reflow soldering and the bond strength of through-hole connector mounting.

For example, Advanced Interconnections has supplied DIP sockets with solder preforms on the socket's leads. In the connector field, both Du Pont and 3M have pc-board connector systems that allow through-hole components to be vapor-phase soldered. Both companies use connector bodies of high-temperature thermoplastics and have solder preforms or inlays—doughnut-like solder rings—mounted around the top of pins in the plastic housing (see fig. 4).

Along with the increasingly complex mechanical design needed with new IC sockets has come the introduction of engineered thermoplastics. Before surface mounting, most sockets and connectors were made from glass-filled polyesters. However, with the growing switch from through-hole technology based on wave soldering to surface mounting, the new sockets and connectors had to be able to take the higher temperatures of either vapor phase or IR soldering. This required a switch to engineered thermoplastics, all of which meet the temperature requirements of surface-mount attachment.

Now an entirely new material—liquid-crystal polymers—is starting to be applied to socket and connector design. This high-performance thermoplastic is approved by Underwriter Laboratories for 200°C, making it suitable for burn-in socket applications, and has the additional advantages of a high-stress modulus and a very low mold shrinkage. Electrically speaking, a liquid-crystal polymer has a low dielectric constant of 2.6 to 3.3, making it attractive for high-speed sockets.

These thermal, electrical, and mechanical advantages have led Amp, Burndy, and Molex to use Celanese's Vectra liquid-crystal polymer for the bodies of their SIMM sockets. The SIMM is a long, thin unit, and any stress in molding may cause its body to warp. In addition, tolerances on this socket can only be met by a low-mold shrinkage material such as liquid-crystal polymer, which is a good material for any long socket or connector. □



4. SOLDER PREFORMS. With small solder preforms on each pin, this through-hole board connector from 3M can be reflow soldered.

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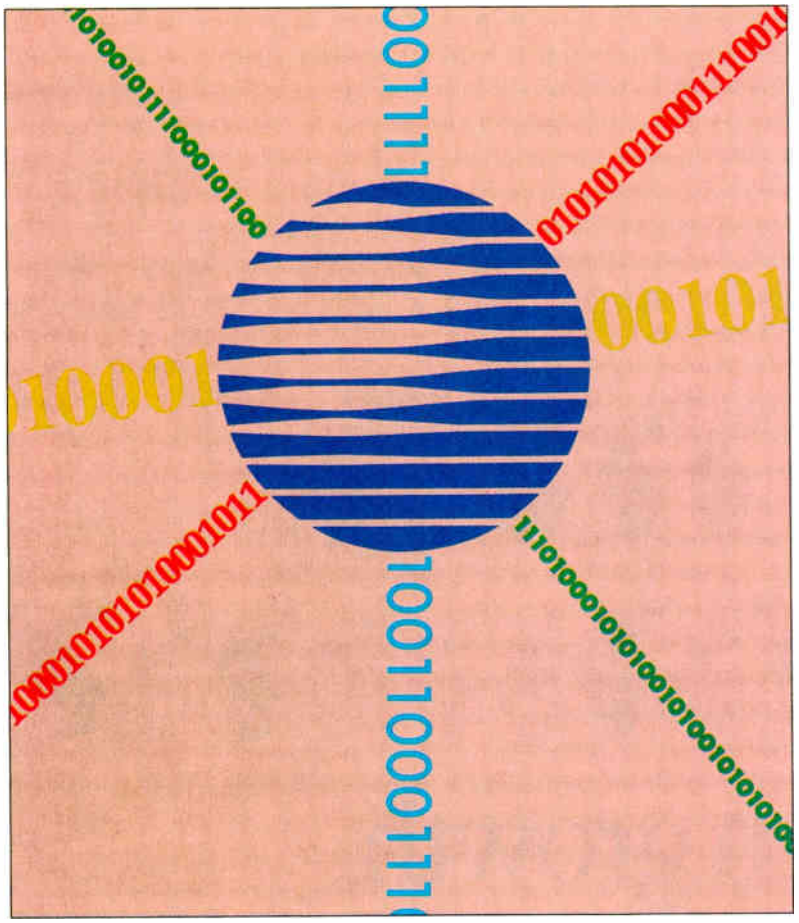


AT&T's first commercial chip squeezes 140,000 transistors onto 51 sq.mm of silicon—enough to implement a 9,600-baud modem with room left over for additional features.

AT&T Packs Performance Into Its One-Chip DSP.

"With the recent outpouring of digital signal processors from chip makers, one more DSP coming downstream now shouldn't make much of a wave. But hold on! This chip is coming from the phone company. AT&T Technology Systems, in Allentown, Pa., is about to introduce a 16-bit DSP16, AT&T's first commercial DSP. Moreover, the single-chip DSP is extremely fast in its target applications; AT&T is aiming it in particular at high-performance modem and speech-processing applications.

It is the DSP16's performance—almost a factor of two over present chips on the market—that should most interest potential customers..."

Excerpted from an exclusive article in the February 19, 1987 issue.

BIT-SLICE PROGRAMMERS GET A PC-BASED TOOL

Microprogramming the new generation of 32-bit-slice building blocks should get dramatically easier and less expensive. Step Engineering Inc. this month is introducing a $3,695 microprogramming development tool called MicroStep, equivalent in performance to systems costing five times more. What's more, Microstep runs on IBM Personal Computer XTs, ATs, and compatibles; earlier versions of the Sunnyvale, Calif., company's development tool run on dedicated systems, work stations, or minicomputers.

At the heart of the MicroStep system is a high-level microprogramming meta-assembler—called MetaStep, the name of the higher-order language the system uses—that does for bit-slice central-processing-unit development what high-level languages such as C have done for programming on fixed-instruction microprocessors such as the 8086, the 68000, and the more recent 32-bit designs. MetaStep consists of five processor modules and an assembler-to-MetaStep translator (see fig. 1). With a few user-defined high-order language statements, the system programmer using MetaStep can replace several hundred assembly or machine-level statements, says Darrell Wilburn, president of Step Engineering.

The MicroStep product consists of language diskettes, one plug-in card for IBM Corp. Personal Computer ATs or XTs, and one or more interconnection pods to a random-access or read-only memory, or to a programmable ROM. "With this package, the user can turn his IBM XT, AT, or compatible system into a fully functional microcode development system," says Wilburn. "This system is a tremendous breakthrough for the microprogram development marketplace. For years the only tools available were in the $20,000-and-up class. This can open up the market for wider use of microprogrammable components."

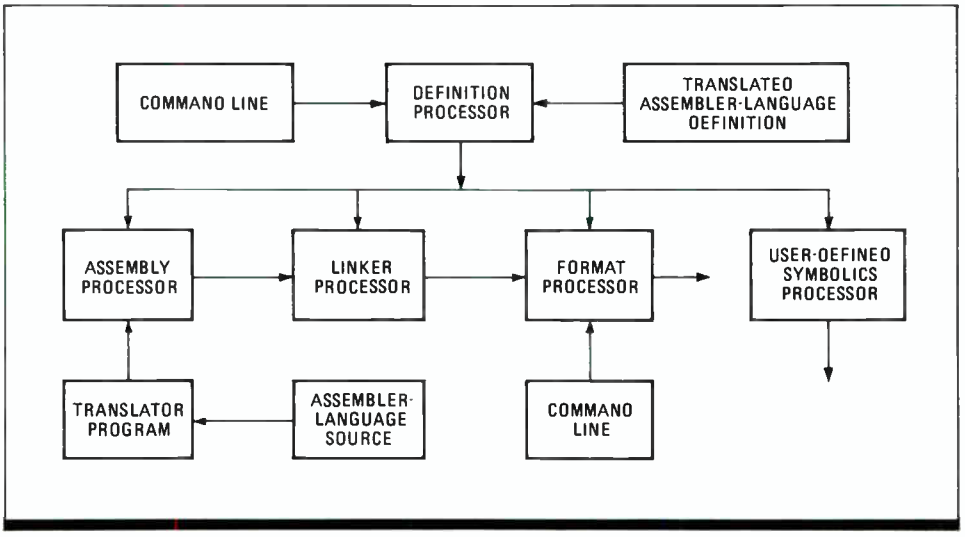
Since the introduction of the language at beta sites late last year, the company has succeeded in expanding the number of systems on which the language is available. In addition to the plug-in board for PC ATs introduced this month and its own PC-AT-based Step 40 microprogramming development system (see fig. 2), MetaStep has also been adapted for use on Digital Equipment Corp.'s VAX minicomputers and Sun Microsystems Inc. work stations.

MicroStep could be widely used in designs with the newer, more powerful microprogrammed 16- and 32-bit arithmetic logic units, and various bit-slice-based building-block digital signal processors, because it simplifies the chore of implementing and debugging large and complicated microcode programs, Wilburn says. An example is the problems a programmer has implementing a common instruction of the 29116, a 16-bit ALU from Advanced Micro Devices Inc.: the subtract with carry, which subtracts data in one location from that in another location and then places the result in a destination while setting the carry bit.

The complication, Wilburn says, arises from the fact that there are many "legal" sources both for the values to be subtracted and for the address of the destination. "Indeed, for this one instruction alone, there are hundreds of possible instruction mnemonic combinations," he says. "Not only are there 12 basic instruction mnemonics to consider, but 32 different RAM register addresses plus three additional instruction mnemonics as well as four non-RAM destinations. That is a total of 396 possible configurations for this single instruction."

To simplify and accelerate the microprogramming of such complex bit-slice architectures, Wilburn and his associates have broken away from the traditional approaches to microprogramming and created, in MetaStep, a language in which the user can create high-level-language-like instructions that are nonpositional in nature; that is, instructions are not dependent on their position in a statement for their effectiveness.

Positional languages involve creating a series of equations that define a name and link an associat-



1. META-ASSEMBLER. Designed for microcode development for 32-bit-slice building blocks, MetaStep consists of five processor modules and an assembler-to-MetaStep translator.

ed bit value to it. Format instructions define a language statement as a series of field names, and when an instruction is assembled, the source names of the fields are replaced with the bit values associated with them in the equations. "The problem is that this requires precisely placing each and every field in its proper order, a tedious and time-consuming process," Wilburn says. "And the more complex the program being written, the more likely errors are to occur."

Costing just $3,695—one fifth the price of competing systems—Step Engineering's MicroStep turns an IBM PC into a fully functional microcode development system

Of more serious concern is that no mechanism for error checking or real-value validation exists, says Wilburn. "This is because values are placed into the microword, but there is no mechanism to bind microfield values to their originating field name. Also, multiple fields often possess the same bit values, and there is usually no way to determine whether a statement is composed of proper field names and values or improper field names with accidentally correct bit values."

Although attempts have been made to create microprogramming languages that are nonpositional and that use more advanced naming capabilities, they represent only a shifting of the memorization task to a new set of mnemonics, Wilburn says. "Even though they are more understandable, there are still many mnemonics to remember. Further, there is no mechanism for performing error checking or type checking to ensure proper coding in the first place. Thus, the debugging task is not that much easier with many different mnemonics and formats to remember."

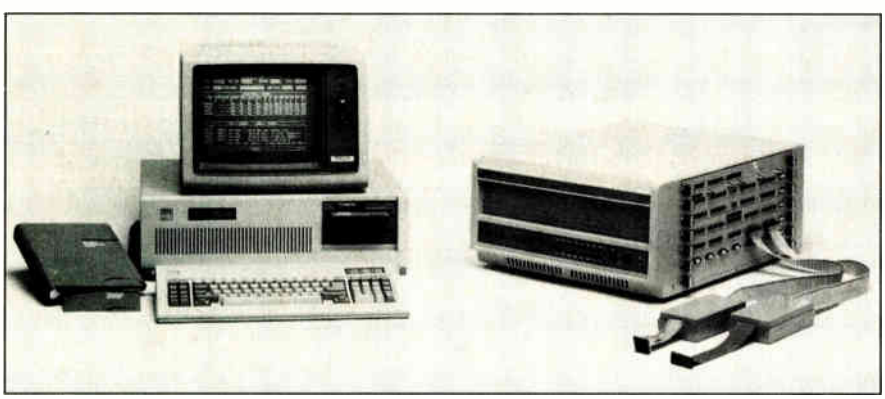
In addition to the nonpositional capability to define fields in logical order rather than simply by microcode instruction address, MetaStep provides such advanced capabilities as nested macros, case structures, and keyword parameters as well as such defensive programming techniques as check descriptors with constraint management. "What is more important is that it provides these features within the framework of a flexible, user-definable, high-order programming language that provides both high-order and bit-level control over design."

The MetaStep's five processor modules consist of a definition processor, the assembler, a format processor, a linker processor, and a user-defined symbolics processor (see fig. 1).

The programmer uses the definition processor to define a language for a given target architecture, field by field, with logical groupings where appropriate. The assembler processor is a macro-driven, relocating, and constraint-maintaining microprogram assembler. The format processor takes the absolute object file output of the linker and extracts several different types of data. The linker processor generates absolute code as well as debug, symbol, and structure tables from the definition processor and assembler processor outputs. And the user-defined symbolics processor automatically generates user-defined symbolic files.

Because of MetaStep's ability to understand the relationship between fields, field values, field names, and even the interrelationships between instructions, it relieves the programmer of the task of remembering the multitude of different instruction mnemonics and formats, Wilburn says. "It allows the programmer to think logically about the operation he wishes to perform and to write his microprogram using logical names and the logical flow of the operation." Further, says Wilburn, "there are no long lists of possible mnemonics to memorize, since the MetaStep instruction can analyze the input and determine which version of the instruction is being specified." And MetaStep automatically checks the values of the source location and destination location to ensure that no illegal values are being accidentally specified.

In addition to providing a much easier but much more powerful way of defining and using an instruction set, MetaStep allows the programmer to go beyond instruction-by-instruction or macro-instruction programming. Using its extensive macro facilities, as well as its nested macro and parameter-passing features, the programmer can define his own high-order-language constructs. And programming with these constructs will be much faster than conventional bit-level coding. "In addition, code generated will be accurate by definition," says Wilburn. "Of particular advantage is the fact that this high-order coding can be intermixed with bit-level coding techniques. The programmer can even mix bit-level and high-order constructs in the same instruction." *–Bernard C. Cole*



2. HARDWARE. MetaStep is available in a package called MicroStep that converts PC ATs to a bit-slice development system, or on the Step 40 microprogramming development system (right).

For more information, circle 484 on the reader service card.

UPDATE: HIGH COST HURTS VANZETTI LASER SOLDERER

A year ago Vanzetti Systems introduced the ILS 7000, an intelligent laser soldering system that offered real advantages over conventional open-loop laser soldering techniques [*Electronics*, July 10, 1986, p. 75]. But despite the promise of the design, the Stoughton, Mass., company has yet to sell one of its ILS 7000 systems.

The intelligent laser solder system contains an infrared monitor that checks solder-joint thermal signatures against a known good joint signature stored in memory. This feedback approach significantly reduces the product damage that often results from conventional systems, while it simultaneously cuts inspection steps and gathers soldering joint data.

The problems selling the system are unrelated to its design, says Dick Alper, director of Vanzetti's system division. The main hindrance to sales has been its cost: the $225,000 price tag on the ILS 7000 is double that of open-loop laser soldering systems. Compounding the problem is the current industry recession, which discourages manufacturers from investing in such relatively expensive equipment.

The company is attempting to reduce the system's cost without compromising its performance. For example, Vanzetti adopted the system's wide-range IR detector from an earlier product, the Laser Inspect system, which is used to inspect finished solder joints. The company now is replacing that detector with a less expensive, uncooled detector that measures the signature of the joint during the soldering process. The ILS 7000 is also being upgraded with improved software and optics. The system can now display thermal signatures in real time instead of printing out the data. Improved optics allow manual observation of laser soldering.


INTELLIGENCE COMES TO LASER SOLDERING

Two models of the Laser Inspect system have recently been converted in the field to ILS 7000s. One is being used to resolder joints on military pc boards at Texas Instruments Inc. in Dallas. A second is working at Vanzetti's West German office. A third system will reach the field later this year, when Vanzetti upgrades a Laser Inspect system at Siemens AG in Munich. *–Jerry Lyman*

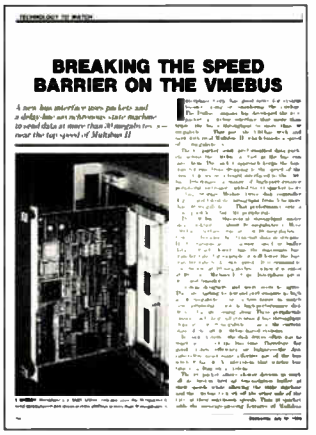
UPDATE: BUS INTERFACE SCORES FOR INTERPHASE

Interphase Corp. is in an enviable position. One year after the Dallas-based company introduced its BUSpacket, a VMEbus interface [*Electronics*, July 10, 1986, p. 58], the competition has not figured out how the design has tripled VMEbus speed to 30 Mbytes/s. Until someone does, Interphase will likely continue to enjoy its 80% share of the VMEbus disk controller market.

"We've had a phenomenal reception," says Michael Cope, Interphase president. "We're winning every benchmark in sight, and BUSpacket is the new standard for speed comparison." The numbers confirm Cope's enthusiasm. The BUSpacket has taken Interphase from $11 million in revenues last year to $15 million today, and the market is leaping ahead at a 60% growth rate. On top of that, Interphase has begun to apply the BUSpacket to other kinds of disk controllers. Meanwhile, competitors have so far only attained bus speeds of 20 Mbytes/s, still 33% slower than the packet design.

To reach its 30 Mbytes/s, the BUSpacket interface formats the data into packets, which are stacked into a 256-word, first-in, first-out buffer, then bursts the information onto the bus as fast as the bus will accommodate it. An asynchronous state machine increases the flow rate between the FIFO and the bus.

Interphase is now leveraging BUSpacket as fast as it can. Already, BUSpacket has spawned a new family of ESDI and SCSI controllers and threatens to influence other architectures, such as high-speed networks operating over Ethernet. The end benefit would be a more efficient use of available bus bandwidths.


BREAKING THE SPEED BARRIER ON THE VMEBUS

In the meantime, Interphase plans to continue refining the BUSpacket approach with further degrees of silicon integration and may eventually disseminate the BUSpacket concept through strategic partnerships. Whatever may come, Cope predicts a bright future for VMEbus, thanks to BUSpacket. "Had 10 Mbytes/s remained the top limit for the VMEbus," he says, "that would have opened the door for Multibus II to knock VME out of in-place designs. The VMEbus market share is now protected." *–Stan Runyon*

ONE PC CARD CAN SIMULATE MIL-STD-1553B SYSTEM

A new tester and simulator for the MIL-STD-1553B bus, which is now used in most military aircraft, promises to greatly reduce the cost of testing and simulation on 1553B buses. The BUS-65517 from ILC Data Device Corp. of Bohemia, N. Y., consists of a plug-in card for IBM Personal Computers and compatibles, plus appropriate software. The product costs just $8,995; with an IBM PC the total comes to around $15,000. That represents a significant savings over a competitive $45,000 dedicated system that has commonly been used for 1553B testing/simulation tasks.

Time-division-multiplexed serial data buses that meet the 1553B specification are now in place in most military aircraft and are planned for more advanced military aircraft. These buses have solved a lot of problems for aircraft designers. "The multiplexed data bus eliminates literally miles of wiring and can operate in the electrically noisy environment found in military aircraft," says Steve Muth, vice president of marketing at Data Device. The complex digital circuitry of the 1553B bus is difficult to test or simulate, though; hence the costly dedicated competitive system.

Data Device's specially designed board with its software can simulate an entire 1553B system, emulate a part or parts of a system, or be used to exercise an actual bus. In addition, the tester can inject error signals into a simulated or actual bus system. "Aside from its cost advantage, the new bus tester/emulator, due to its new user-friendly software, can be on-line in one to two hours, while a two- to three-day training course is required for the dedicated unit," says Catherine Del Casale, data-bus products engineer at Data Device. The BUS-65517, which has a six-week delivery, is currently being evaluated by several of Data Device's customers.

The main components of a 1553B data-bus system are a shielded twisted-pair cable, coupling transformers, a bus controller, a bus monitor, and remote terminal units. The bus controller initiates message transfers on the data bus. The bus monitor receives bus traffic and extracts information to be used later. Any terminal on the bus not operating as a bus controller or monitor is a remote terminal.

The keys to the BUS-65517's simulation and testing of the 1553B bus are the standard full-size printed-circuit card for the IBM PC, and the menu-driven software. These tie the 1553B bus to the PC's bus. The plug-in board and its software emulate a bus controller, monitor or multiple remote terminals. The board is capable of performing these functions simultaneously. This allows a single printed-circuit board to emulate an entire 1553B system made up of a bus controller, 31 remote terminals, and a bus monitor. In addition, error injection is also supported in both the bus-controller and remote-terminal modes. The board is transformer-coupled to the 1553B bus, allowing the board to be used as a simulator or a bus exerciser.

The purpose of the board is to provide full, intelligent interfacing between a serial dual-redundant MIL-STD-1553B bus and the IBM PC bus. The board (see fig. 1) uses a mix of surface-mounted leadless chip carriers and dual in-line packages, plus two pinned thick-film hybrids.

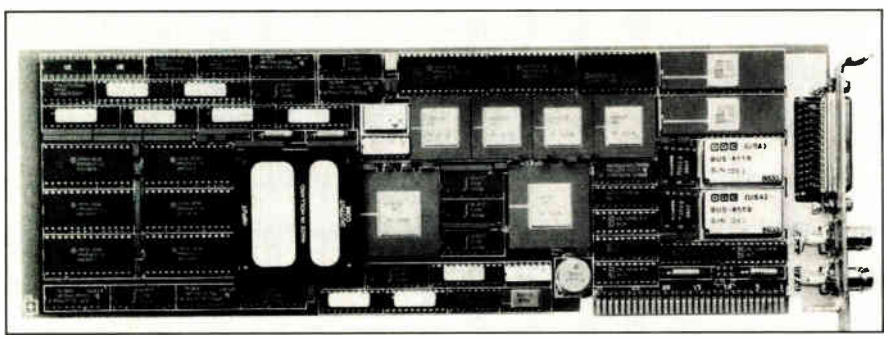
The dual-redundant 1553B bus enters the board through two transformers and two transceivers (see fig. 2). Then the circuitry is split up into two nearly identical circuit blocks, the bus controller/remote terminal unit and the the monitor unit. Each block uses a Z8002 microprocessor as its CPU.

The BUS-65517's software has three modes of operation: Setup, Run, and Monitor. The latter displays the communication stack. The Setup mode allows a user to define global parameters, bus-controller, monitor, and remote-terminal modes, and data with the assistance of a menu-driven interface.

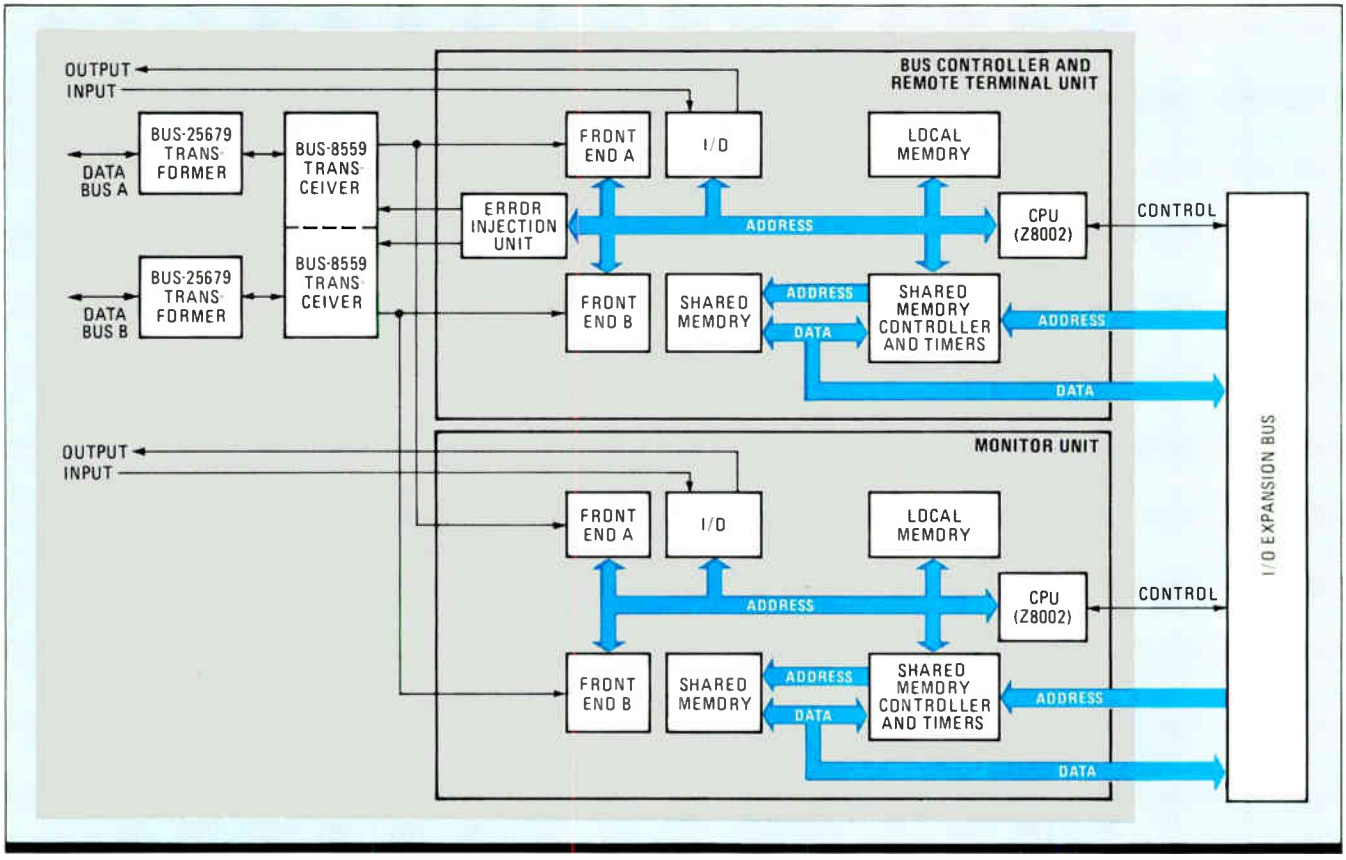
The Run mode executes the instructions defined in Setup. In Run, the bus controller and remote terminals transmit and receive 1553B message traffic, and the bus monitor stores these messages.

The Monitor mode allows a user to monitor traffic. The communication stack can be greater than 100 Kbits, so methods are provided for searching, scrolling, saving, and printing the stack.

In the bus-controller setup mode, controller activity is defined by a set of messages organized in a frame. The BUS-65517 supports up to 250 messages. A frame may contain up to 1,000 messages divided into minor frames of equal duration.



1. PLUG-IN. Data Device's BUS-65517 plug-in board and dedicated software make it possible to use an IBM PC or compatible to emulate or test the components of a MIL-STD-1553B data bus.



2. TWO BLOCKS. The dual-redundant 1553B bus enters the board through the transformers and transceivers at the left; the circuitry is then split into two blocks, the bus controller/remote terminal unit block and the monitor unit block, which interface the PC bus.

Each message is assigned a number. All message formats, including broadcast and mode commands, are supported. In addition, a user may specify the type of error to be injected into the message, if any. The error may be an encoding error, a word-length error, or a timing error. The user specifies where the data for the message is to found by indicating which data table is to be used for that message. Data tables may be used by more than one message if desired.

The user defines a frame by filling in a table indicating the order in which the stored messages are to be transmitted. The user may instruct the BUS-65517 to run the frame a specified number of times or to run it until he issues a Halt command.

In the remote-terminal setup mode, the BUS-65517 can simultaneously emulate up to 31 remote terminals. Each terminal maintains its own status and last-command words. The status bits Message Error and Broadcast Busy are determined dynamically.

Each emulated terminal can support 32 subaddresses for transmitting and receiving. Data tables may be shared between sub-addresses, as well as by multiple remote terminals.

The BUS-65517 automatically handles mode code commands for each individual sub-address. For example, remote terminal No. 4 can be instructed by the bus controller to shut down transmitter A, while the other remote terminals emulated by the board can continue to use that channel. Instructions received on channel A for RT4 will be ignored until an override shutdown-mode code command is received for that terminal.

To define the characteristics of the terminal to be emulated, the user calls up a Setup Remote Terminal menu. This permits the operator to force any bit in the status word to a logic 1 if desired. The user may also define error conditions for the remote terminal. In addition to the basic 1553B errors, the remote terminal can be instructed to respond with the wrong terminal address in its status word, or to suppress the transmission of its status word altogether.

As a Bus Monitor, the BUS-65517 records 1553B transactions. The user may indicate whether to record all messages transferred over a bus or a subset of them, and when to begin recording bus transfers. This is accomplished with a menu whose listings are: Immediate Capture; Command Template—i.e., capture only those messages corresponding to a match between the received command and a template consisting of logical 1s, 0s, and don't cares; error condition detected; and external trigger. The BUS-65517 will detect both word errors and message errors. *–Jerry Lyman*

For more information, circle 485 on the reader service card.

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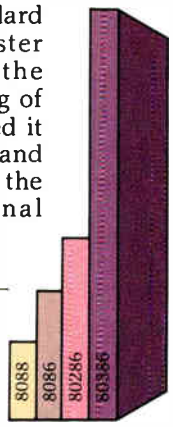

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MILITARY/AEROSPACE NEWSLETTER

WHY THE ARMY CANCELED RFP FOR ITS LATEST REMOTELY PILOTED VEHICLE

The Army Missile Command, Huntsville, Ala., has notified the two finalists competing for its Intelligence Electronics Warfare/Unmanned Aerial Vehicle contract that it has canceled the current solicitation, and will issue another request for a proposal by the end of August. The companies, California Microwave Inc., Sunnyvale, Calif., and Developmental Sciences, Santa Monica, Calif., got letters saying they didn't meet all requirements of the solicitation. However, a source at one of the firms believes the Navy is thinking about adopting the Army's IEW/UAV for its own long-range reconnaissance operations, and the extension is designed to give the Navy time to review requirements for its remotely piloted vehicle program. The Navy has lost four short-range Pioneer 1 RPVs when they crashed during test flights. The Navy, however, denies any plan to use the Army IEW/UAV. The two finalists, coming off what they thought was a successful competitive fly-off in April, were advised that they will be invited to participate in the next round. The IEW/UAV contract is valued initially at $20 million to $60 million and eventually could be worth $200 million. □

NEW AIR FORCE UNIT WILL OVERSEE LONG-TERM ELECTRONICS R&D

The Electronic Systems Division of the U.S. Air Force's Systems Command is setting up an advanced technology organization that will oversee its programs for the Strategic Defense Initiative, the Air Defense Initiative, and a new Special Projects Directorate. Under a new Deputy Commander for Advanced Techology, the outfit is charged with coming up with concepts and technologies for strategic defense. The new unit is being set up because research for all three projects overlaps to a large extent. The ADI program includes research in surveillance and command and control, with an emphasis on surveillance technologies that could be available in the near term. SDI is studying battle management, which includes command, control, and communications but is oriented toward technologies that will be developed several years from now. The new Special Projects Directorate will concentrate on technologies for advanced surveillance, battle management, and command, control, and communications that could be available in the long term—after the year 2000. The organization will also be responsible for setting up and running the SDI National Test Bed at Falcon Air Station, Colorado Springs, Colo. That facility will be used to simulate key SDI system components. A request for proposals to develop the test bed will be released by the Air Force Systems Command by Sept. 1. □

EVERYONE WANTS TO STUDY SOVIET ELECTRONICS TECHNOLOGY FOR AIR FORCE

When the Air Force Systems Command's Foreign Technology division issued a request for proposals to analyze Soviet electronics technology, it was swamped with responses. So the Wright-Patterson Air Force Base operation has postponed its original June 15 deadline for proposals and is continuing to accept responses from industry. A new deadline has not been set. More than 50 electronics and aerospace companies have already expressed an interest in the fixed-price award. It's a dual contract, meaning the Air Force plans to give the same contract to the two top bidders and presumably will use the best analyses from both studies. The three-year study calls for a review of Soviet systems designs and materials used in the development of electronic countermeasures, ground air-defense and airborne radars, and space-vehicle guidance systems. Also, in mid-July the division will request a synopsis from industry of a one-year study of foreign ballistic missiles and related space systems. The Air Force says teaming will be encouraged for this contract, which should be awarded in the second quarter of 1988. □

MILITARY/AEROSPACE NEWSLETTER

OBTAINING EXPORT LICENSES COULD GET A LOT EASIER AND FASTER

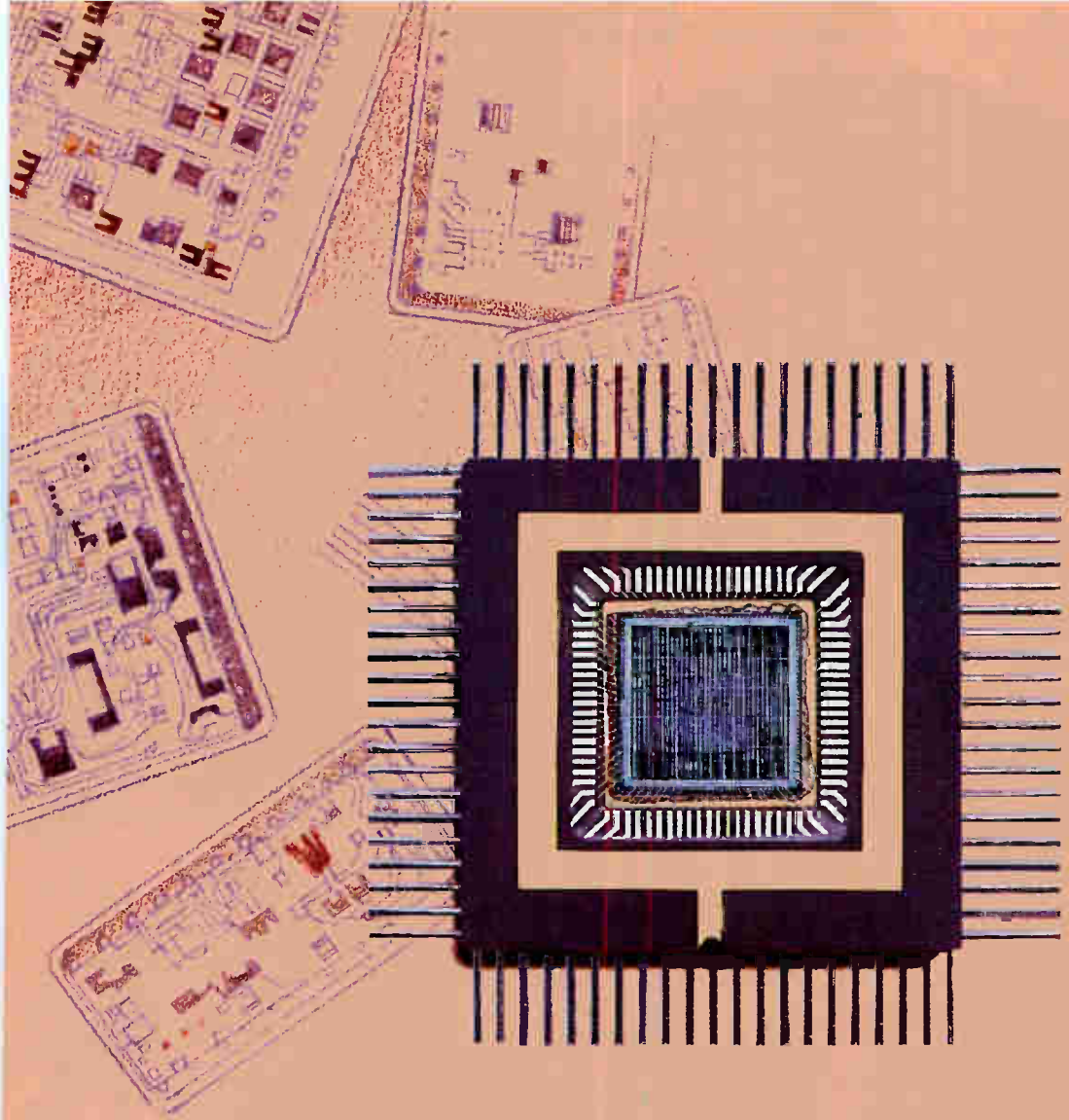
Responsibility for licensing military electronics and other products for export could shift from the State Department to the Pentagon, if Congress follows the recommendation of the Government Accounting Office. The bottom line for industry is that the shift would make it easier and faster to get an export license. The GAO will issue a report at the end of July that is expected to make several recommendations for improving the efficiency of the State Department's Office of Munitions Control, which currently licenses exports and also registers arms dealers. One of its recommendations might be to shift OMC's activities to the Pentagon, which would give the DOD more control over military and related exports. Congress called for the GAO study because the number of export licenses granted over the past 10 years has nearly doubled, but only a few people have been added to the OMC's staff. Congress has for some time thought that the OMC acts too slowly in response to export license applications and is less concerned about security issues than the DOD. The Pentagon's Defense Technology Security Administration, which monitors export licensing for the DOD, is considered by some in Congress to be better equipped for the export-licensing task and is the likely candidate to take over OMC activities. Sen. David Pryor, a Democrat from Arkansas, has asked the DOD to comment on its capabilities for handling OMC's activities but has not yet received a detailed response. □

WESTINGHOUSE INVESTS IN INOVA TO SPEED ULSI CHIP DEVELOPMENT

Westinghouse Electric Corp. has invested $5 million in Inova Microelectronics Corp., in an attempt to speed Inova's development of ultra-large-scale integrated monolithic chips. Westinghouse has been working with the Santa Clara, Calif., startup for more than a year on a now-completed classified military development program. Inova has developed a proprietary architecture for interconnecting multiple devices on a wafer's surface, named Inroute, and expects to announce its first product in several months [*Electronics,* Jan. 8, 1987, p. 91]. The infusion of funds brings the privately held company's total capitalization to nearly $10 million since it was formed in 1983. Although no exclusive technology transfer is involved in the agreement, Westinghouse's investment should accelerate Inova's work on monolithic chips for use in high-density, high-reliability avionics and space applications. "Wafer-scale technology is a strategic imperative in our advanced military programs," says Gene Strull, general manager of Westinghouse Defense and Electronics Center's Advanced Technology Division, Baltimore. Inova has produced evaluation quantities of three static random-access-memory devices, the most recent of which integrates more than 128 chips across the surface of a full silicon wafer. When brought to market, the Inroute devices will comply with the requirements of MIL-STD-883C for production of military-qualified integrated circuits, Inova says. □

AUTOMATED FACILITY HELPS TI CUT LABOR COSTS IN BUILDING HARM MISSILE

Armed with a $556 million contract to make 2,575 high-speed anti-radar missiles, or HARMs, Texas Instruments Inc. has set up an automated machining facility at its Trinity Mills plant near Dallas that is capable of turning out 9,000 different part numbers. The facility uses TI's Explorer Lisp system for the scheduling, planning, and transmitting of instructions necessary to turn out 210 missiles per month. Deliveries are scheduled to be completed in the fourth quarter of 1989. The plant's initial results indicate a 4 : 1 reduction in labor and 3 : 1 reduction in cycle time over previous production techniques. HARM, an air-to-surface missile, is designed to home in on enemy radar systems that direct anti-aircraft gunfire and surface-to-air missiles. □



A compact 1553 that carries a busload.

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The BCRT's bus controller uses a linked-list message scheme to provide the host with message "chaining." Memory space is optimized by using programmable address pointers. As an RT, the BCRT implements time tagging and message history functions. It also supports multiple-message buffering—up to 128—including variable-length messages to any subaddress.

The BCRT complies with the standard LAN used for military systems while meeting selected tests in MIL-STD-883C. It is available in 84-pin LCCs, PGAs, or Cerquads.

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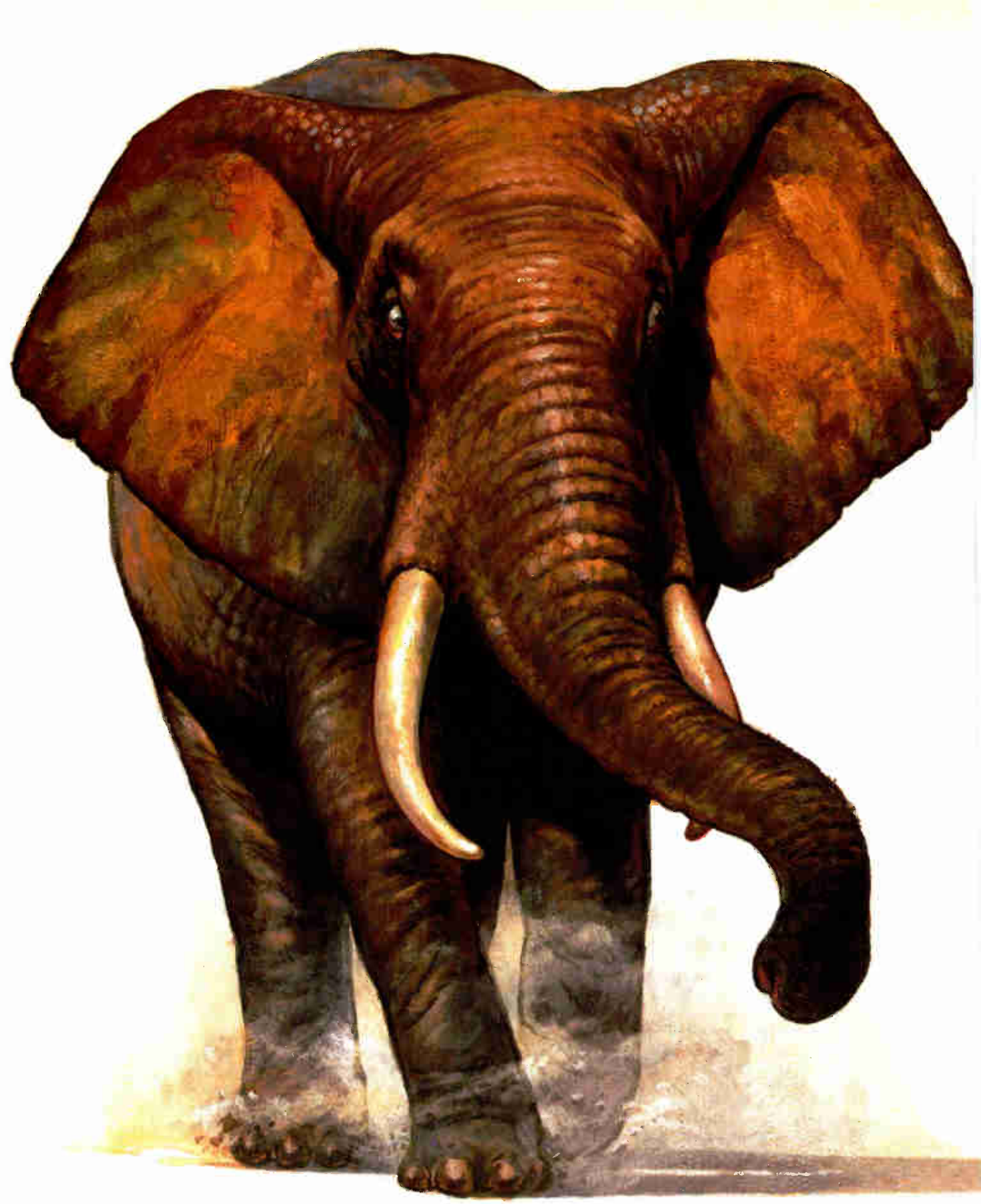

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TMM27256ADI	32KX8	NMOS
TC57256D	32KX8	CMOS
TC57256AD	32KX8	CMOS
TMM27512D	64KX8	NMOS
TMM27512DI	64KX8	NMOS
TC571000D	128KX8	CMOS
TC571001D	128KX8	CMOS
TC571024D	64KX16	CMOS
ONE TIME PROGRAMMABLE		
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TMM24128AF	16KX8	NMOS
TMM24256AP	32KX8	NMOS
TMM24256AF	32KX8	NMOS
TC54256AP	32KX8	CMOS
TC54256AF	32KX8	CMOS
TMM24512P	64KX8	NMOS
TMM24512F	64KX8	NMOS
TC541000P	128KX8	CMOS
TC541001P	128KX8	CMOS
ROM		
TC53257P	32KX8	CMOS
TC53257F	32KX8	CMOS
TC531000AP	128KX8	CMOS
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NEW PRODUCTS

SPEEDY GRIDLESS SOFTWARE DESIGNS DENSER PC BOARDS

ROUTER DOES COMPLEX DESIGNS 10 TIMES FASTER THAN COMPETITORS

By implementing a gridless routing system to solve the knotty problems presented by surface-mounted devices and pin-grid arrays, a new place-and-route software package for printed-circuit boards opens the door to complete multilayer designs with high component density. What's more, Shared Resources Inc.'s Crystal Router completes complex designs up to 10 times faster than competitive tools.

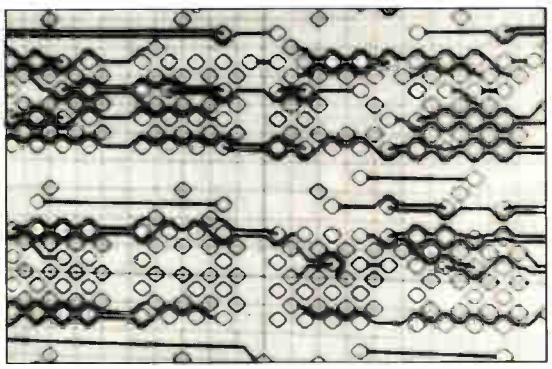
Flexibility is the key to the software's performance. Instead of routing with a conventional rectangular grid system—which must be adjusted to accommodate obstacles, such as an input/ouput pin—the San Jose, Calif., company's software simply goes around the obstacles.

With conventional routers, for example, the insertion of each via into the routing channel to connect SMDs reduces space for routing. Similarly, tight pin spacing in PGAs forces layout designers to add additional space between the arrays to accommodate the routing—effectively defeating the purpose of using high-density arrays.

MAKING ROOM. The Crystal Router, on the other hand, simply inserts the via in the routing channel and spreads the surrounding wires to accommodate the addition. Grid-based routers would have had to reduce the number of wires to insert the via. With several vias in a channel, the traces appear to be negotiating a series of S curves as they run the length of the channel. Nevertheless, even though the wires are spread apart they still maintain the same relative spacing.

In addition to the gridless router, Shared Resources uses diamond-shaped via pads that require less space than conventional pads. Combined, the two techniques can place vias for SMDs and PGAs anywhere on the board without consuming any routing resources in the process.

To handle high-pin-count PGA packages, the router places vias in between pins of the array to greatly increase the number of vias possible.



WINDING WAY. Detail of a pc-board layout shows diamond-shaped vias and characteristic S-curve paths around vias.

Dan Murphy, chairman and vice president of software development, says that in one board layout the router created 184 potential vias for a 128-pin PGA, whereas a conventional router was only able to squeeze in 41.

The Crystal Router operates much faster than its competitors. Murphy estimates that a 15-by-15-in. board containing a mix of 800 components packed as tightly as possible might have 1,500 to 2,000 nets, 5,000 to 7,000 connections, and 11,000 to 13,000 in. of wire. Crystal Router could route the board in two to six hours when running on an IBM Corp. 4341 computer. That time is an order of magnitude quicker than competitive tools.

Part of this speed comes from the tool's being a true multiple-layer router. Other routers that claim to be multilayer tools actually route two layers at a time, which reduces the probability of finding optimal routes, the company says.

The Crystal Router's gridless architecture also contributes to its speed. Shared Resources uses the term "gridless" to indicate that the router can place a component, via, or wire anywhere on the board surface. Without the grid structure, the tool has much less data to maintain and process. Other routers that claim to be gridless do in fact have a grid system with very small grid spacing and are burdened with the task of maintaining the grid structure, the San Jose, Calif., company says.

Although grid systems offered a practical option when boards were populated largely by dual in-line packages, the trend toward surface mounting and pin-grid arrays, which can squeeze more functionality on a board, has intensified the obstacle problem. These devices significantly increase the number of I/O pins the router must handle, and that often means widening the distances between grid lines. This in turn consumes space that could be used for routing.

There is an increasing need for place-and-route tools to handle high-density, multilayer printed-circuit boards. In 1986 the use of multilayer, high-density pc boards for the first time exceeded use of two-sided boards, which have inherent component density limitations, according to Dataquest Inc. figures. Dataquest also predicts that by 1989 the market share of boards having three or more layers will grow at an average annual rate of 11.6% and should reach $2.5 billion.

This contrasts with a total pc-board market of $7 billion in 1989 and an average growth rate of 7.4% through 1989. Moreover, extremely complex boards of 10 or more layers would realize an annual dollar volume increase of 18.2% in the next three years, growing to a total of $360 million.

TAKING INSTRUCTIONS. The Crystal Router lets users specify how it should proceed with its task. Electrical characteristics of the interconnections can be controlled to a large extent. Designers can specify up to four attributes out of a total of 10 to each connection point. For example, they can specify the length of the path or the number of vias to be used in making the connection.

Once a designer specifies the type of technology for each component in the layout, the router executes an internal set of rules to handle the technology. High-speed emitter-coupled-logic circuits demand very short leads and cannot tolerate a via connection, for example, and the router automatically takes these requirements into account.

Unlike other routing tools, the Crystal Router places no practical limit on de-

sign size, number of components, or number of layers. The software is available now in prices ranging from $75,000 to $125,000, depending on application and platform. —*Jonah McLeod*
Shared Resources Inc., 2902 Orchard Pkwy., San Jose, Calif. 95134.
Phone (408) 434-0444 [Circle 380]

DSP DEVELOPMENT TIME CUT BY 33%

By providing prefabricated building blocks for the most commonly used digital signal processing functions, Inmos Corp.'s B009/D703 development system for the company's A100 DSP chip cuts as much as a third off application development time.

With code for common DSP functions such as convolutions, discrete Fourier transforms, and finite impulse response filters built in, users can often specify the characteristics of a solution and let the system generate the software.

The B009-1 motherboard containing four A100 chips, 64 Kbytes of random-access memory, and the Inmos T212 transputer plugs into an IBM Corp. Personal Computer or compatible. The optional daughterboard, the B009-2, includes a T414 32-bit transputer with 1 Mbyte of RAM.

Available now, the motherboard costs $4,500. The mother and daughter boards together cost $6,000. The D703 software costs $250. A package of the mother and daughter boards, the D703 software, and the transputer development-system software costs $7,500.
Inmos Corp., P. O. Box 16000, Colorado Springs, Colo. 80935.
Phone (303) 630-4000 [Circle 385]

ANALYZER OFFERS 80 100-MHz CHANNELS

Gould Inc.'s K450B logic analyzer can be configured by keyboard commands to monitor and capture data on up to 80 channels at 100 MHz or across 40 channels at 200 MHz.

Along with a standard 4 Kbytes of memory, the system's performance allows users to analyze state and timing on 32-bit microprocessors without having to relegate some signals to lower speeds because of limitations imposed by the instrument.

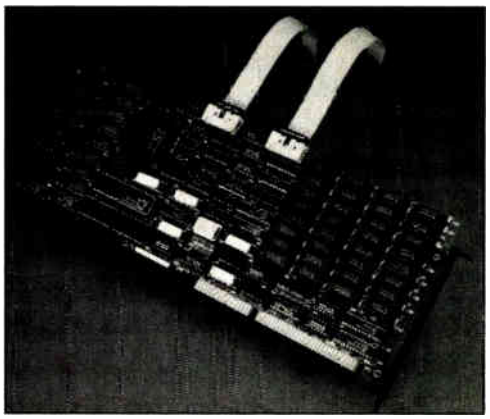
The K450B offers a single-key test set-up function for routine analysis applications and a variety of features such as six edge-sensitive and six level-sensitive clock inputs.

Available now, the 80-channel version costs $27,995. A 16-channel version costs $13,795.
Gould Inc., Design & Test Systems Div., 19050 Pruneridge Ave., Cupertino, Calif. 95014. Phone (800) 538-9320 [Circle 386]

IMAGE-PROCESSING BOARD ATTACKS PC BOTTLENECK

DATA TRANSLATION'S DT7020 RUNS AT 8 MEGAFLOPS AND BYPASSES PC BUSES FOR REAL-TIME PERFORMANCE

Data Translation Corp.'s array-processor board for the IBM Corp. Personal Computer AT can perform 8 million floating-point operations/s in image-processing and digital-signal-processing applications. But just as important as its speed is the DT7020's position as the cornerstone of the company's DT-Connect family of products. By bypassing the PC's bus and putting processors and data-acquisition boards in direct communication through external input/output ports, the DT-Connect products aim to break the processing bottleneck that microcomputer buses often create.



DIRECT LINK. The DT7020's memory maps directly into the host PC AT's extended memory space.

The $6,595 DT7020 plugs into a single slot of a PC AT. It incorporates a single-chip, general-purpose Advanced Micro Devices Inc. 29325 processor that includes a 32-bit floating-point multiplier and an arithmetic logic unit with a full 32-bit data path.

The processor performs single-precision floating-point addition, subtraction, and multiplication operations in a single clock cycle. It runs at a peak rate of 8 megaflops, using the IEEE floating-point Standard P574.

DUAL PORTS. The DT7020 has 4 Mbytes of memory, organized as 1 Mbyte by 32 bits. Mapped directly into the host PC AT's extended memory space, the memory appears to the host as two pages of 2-Mbyte memory. The data memory has dual ports, which means it can be accessed by the host over the bus or over the DT-Connect external I/O ports for high-speed transfers with devices such as an analog-to-digital board, says the Marlboro, Mass., company.

The DT-Connect concept grew out of an application in which Data Translation engineers designed two 26-pin hardware ports that linked a frame-grabber board to a processor board with hard-wired logic. By circumventing the host bus, the system lets the customer handle image-processing applications in 1 second instead of 5 minutes.

The system also triggered the interest of frustrated array-processor manufacturers, who needed 10-MHz processing, especially in imaging applications, and wanted to get off a host bus that limited them to speeds of 150 to 200 Kbits/s, says John Molinari, product marketing manager for imaging products.

DT-Connect's first products include three software packages. The Mach Vector subroutine library, which accelerates signal and image processing, is priced at $1,495. The Mach Microcode Assembler/Simulator helps users write their own microcode; it costs $1,495. The Mach DSP library, which accelerates signal and array processing, costs $1,495. In addition, a Mach DSP subroutine library facilitates direct connections between any member of the DT series and the DT7020 array processor.

In addition to the DT7020 array processor, the DT-Connect hardware family also includes the DT2841 series of six digital-to-analog boards, which range from $1,450 to $2,995 in price. The boards cover frequencies from 40 to 750 KHz. The fastest competitive boards run at 100 KHz, the company claims.

–Lawrence Curran

Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752.
Phone (617) 481-3700 [Circle 340]

COMPUTER HANDLES BOTH DOS AND DEC

Datamedia Corp. is using a CMOS gate-array custom chip set in its Colorscan/2 work station to achieve full compatibility with IBM Corp. Personal Computers running MS-DOS, and to provide an emulation mode for Digital Equipment Corp.'s VT240 graphics terminal. With a single keystroke, users can now choose either the IBM micro's

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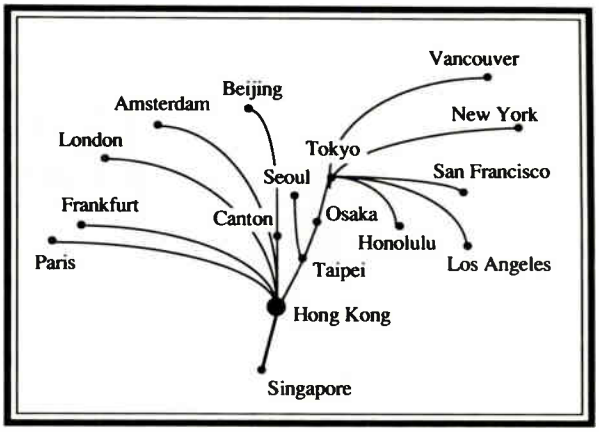

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versatility or a powerful graphics engine—all on a work station with a 10-by-15-in. footprint.

Combined with a proprietary mapping technique, the CMOS chips enable the Colorscan/2's NEC Corp. V30 8086-compatible microprocessor to switch between tasks stored in different memory partitions. That ability, plus the system's two RS-232-C ports, lets users communicate simultaneously with two host computers. A windowing feature lets users display both computer sessions at the same time or switch between them.

The Colorscan/2 offers compatibility with the IBM Personal System/2, PC/XT or PC AT, and compatibles, and

FAST. Colorscan/2 can update its screen twice as fast as IBM's EGA standard.

fully supports IBM Enhanced Graphics Adapter graphics. Enhancements permit the screen to be updated twice as fast as IBM's EGA, and provide sharper characters, says Guy Daniello, Datamedia president. The work station also fully supports DEC VT240 and Tektronix graphics.

One of the custom chips is a 2,200-gate NEC CMOS array that functions as the system controller chip. It provides all the system's input/output read-write timing, as well as memory mapping into 16 pages of memory and eight memory maps. Each map provides logical addressing so that the memory map in use appears to the microprocessor as the only application running.

CRT CONTROLLER. Another custom chip provides the timing that is required for the CRT controller, memory, and smooth-scroll functions, plus remapping from the system's different graphics modes. A third chip controls color mapping and the logic for other functions, such as color comparisons and color background fills.

Besides the two RS-232-C ports, the Nashua, N. H., company offers two IBM PC/XT expansion slots for local-area networks and external peripherals and a

parallel printer port. Datamedia offers one external peripheral—a diskfile that includes 1.4 Mbytes of floppy and 20 Mbytes of hard-disk storage, both in the 3.5-inch size. The diskfile sells for $995.

Colorscan/2 costs $2,000 and volume shipments begin this month. Other storage options include a RAMfile for $750 with 2 Mbytes of internal battery-backed storage, and a cardfile with interface for $150 that handles credit-card-sized non-volatile storage.

Storage devices are treated as MS-DOS disks, and can be used to store and share applications. MS-DOS can be booted from any of the storage options, and the system's connectivity allows users to access and store data in corporate hosts, departmental minis and LAN file servers. *–Lawrence Curran*

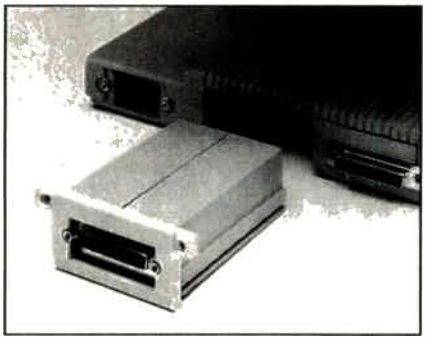
Datamedia Corp., 11 Trafalgar Sq., Nashua, N.H. 03063.
Phone (603) 886-1570 [Circle 341]

TERMINAL LETS OEMs CUSTOMIZE ADD-ONS

Interchangeable cartridges give original-equipment manufacturers wide versatility in configuring Link Technologies Inc.'s MC10 monochrome terminal into their systems.

A slot in the base of the unit accepts personality cartridges that can be programmed to accept the OEM's product, including mouses, graphics and communications packages, light pen, and bar-code readers.

A slot in the keyboard makes that module widely adaptable as well, allowing it to link to any of 14 popular terminals, including Digital Equipment Corp.'s VT 100, 220, and 52 and Wyse



Technology's models 50, TV1950, 925, and 910.

The MC10 has three position adjustments—elevation, tilt, and swivel—to accommodate almost any user. Other features are a 720-by-348-pixel display resolution and a 14-in. flat-panel CRT display in green, amber, or soft-white screen phosphors that operates on refresh rates of 60 or 70 Hz.

Available now, the MC10 costs $595.

Link Technologies Inc., 47339 Warm Springs Blvd., Fremont, Calif. 94539.
Phone (415) 651-8000 [Circle 345]

PC AT CLONE CHIPS OFFER SPEED, BETTER GRAPHICS

CHIPS AND TECHNOLOGIES' ICs BOOST CLOCK SPEEDS 56% AND INCREASE EGA GRAPHICS RESOLUTION TO 1,128×560 PIXELS

Four chips from Chips and Technologies Inc.—the leading manufacturer of integrated circuits for clones of IBM Corp.'s Personal Computer AT—deliver triple the screen resolution, boost clock speeds from 8 MHz to either 10 or 12.5 MHz in systems compatible with Intel Corp.'s 80286 microprocessor, and boost clock speeds from 16 to 20 MHz for systems compatible with the 32-bit 80386.

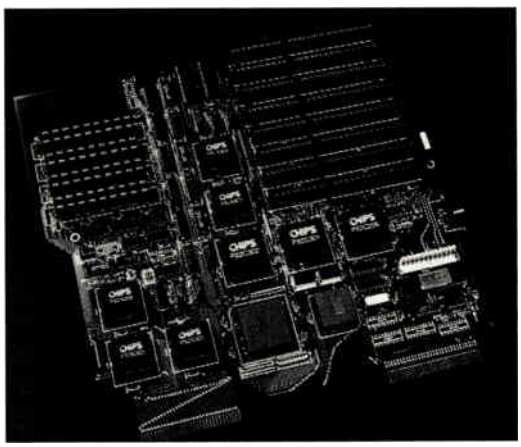
The 82C437 SharpScan delivers 1,128-by-560-pixel resolution while still retaining 100% compatibility with the 640-by-350-pixel Enhanced Graphics Adapter standard from IBM. It uses a proprietary pixel-multiplexing function that enables users to trade off the number of colors available—four instead of the normal 16—for higher resolution, says Gordon Campbell, president of Chips and Technologies.

EGA COMPATIBLE. Using the chip in an EGA chip set means that up to 300% more information can be presented on the screen than present EGA standards allow, he says. Additional software or setup changes to regular EGA monitors are not required.

Users can switch back and forth between high-resolution and normal EGA operation, depending on their application requirements. Because the new chip incorporates on-chip video drivers that were previously implemented externally with the Chips and Technologies EGA implementation, the total chip count for complete EGA implementation remains at 13—the lowest number in any configuration currently available, says Campbell.

To support clone computers that target speed-enhanced versions of the 80286, the Milpitas, Calif., company is introducing two speed-enhanced versions of its original 8-MHz CS8220 PC AT chip set: the 10-MHz CS8220-10 and the 12.5-MHz CS8220-12.

Both chips support very large memory configurations, from 1 to 4 Mbytes on the system board, making them appropriate for large memory systems and the next generation of operating systems.



TOP CHIP. The 20-MHz AT/386 chip set triples the performance of the IBM Corp.'s original PC AT.

The chip sets that complement these microprocessors have also been upgraded. A new memory-controller chip provides dynamic bus clock switching so that a system can run at full speed for on-board memory and then automatically switch to half speed for all off-board memory and input/output functions.

This capability, the company says, allows a 100% AT-compatible system to be upgraded to the higher speeds using the original add-on cards and application software with no alterations.

Chips and Technologies has targeted high-speed 386-type systems with its new CS8230-20, a 20-MHz microprocessor for the AT/386 chip set the company introduced in October 1986.

Coupled with the new chip, the enhanced AT/386 chip set delivers three times the performance of the original IBM PC AT system but uses one third the board space and one third the power. Designers achieved this by improving timing on all seven devices in the set.

The page/interleave memory controller has been enhanced to allow two-way interleave memory access for 16-MHz systems using page-mode dynamic random-access memories, as well as for 20-MHz systems that use static column DRAMs. Also, the bus controller now has an independent clock for AT bus operation, enabling the processor to run at 20 MHz while the expansion bus runs on another clock.

Available now in sample quantities, the 82C437 SharpScan EGA chips cost $6.70 each in 1,000-unit quantities. Samples of the CS8220-10/12 cost $69.10 in 100-lot quantities, and samples of the CS8230-20 cost $220 each in 100-lot quantities. A CMOS version of the CS8230 designed for low-power and portable systems will be available late in July for $184 per piece in 100-unit quantities. *–Bernard C. Cole*

Chips and Technologies Inc., 521 Cottonwood Dr., Milpitas, Calif. 95035.
Phone (408) 434-0600 [Circle 360]

ICs SIMPLIFY PHONE-LINE EQUALIZATION

Two monolithic CMOS devices from Micro Linear Corp. virtually eliminate the need for manual adjustment of the frequency response and gain in telephone trunk lines—a costly and time-consuming problem that plagues conventional hybrid-circuit solutions.

The ML202 high-performance trunk-line equalizer offers a 105-dB dynamic range, more than enough for trunk-line applications. The ML203 logarithmic gain/attenuator operates over a range of −24 to +24 dB. Its ±1-dB response at 20 KHz exceeds telecommunications requirements and suits the chip to applications in instrumentation and audio systems that use remote control of signals.

Hybrid-based trunk-line conditioning solutions are highly susceptible to performance degradation resulting from temperature drift and aging, says Charles Gopen, vice president of marketing. System noise also accumulates as trunk lines are connected in series. The ML202/203 chip set eliminates these problems with an improved biasing scheme and highly matched device geometries that are virtually unattainable in hybrid circuits.

In equalizer operation, a 14-bit shift register in the ML202 loads data from an external microcontroller into a data latch. The latch's parallel output goes to three core filters that supply appropriate capacitor values to adjust the slope, height, and bandwidth of the input signal.

The ML203 adjusts gain with a coarse-gain stage, which handles 1.0-dB steps, and a fine-gain stage for 0.1-dB steps, all within a 0-to-1.5-dB range. A 9-bit shift register, latch, and output multiplexer allow the use of parallel or serial interfaces.

Both devices will be available in the third quarter of this year. In 1,000-unit quantities the ML202 will cost $8 each, and the ML203 will be $5 each. *–Bernard C. Cole*

Micro Linear Corp., 2092 Concourse Dr., San Jose, Calif. 95131.
Phone (408) 262-5200 [Circle 361]

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ELECTRONICS WEEK

LAMBORGHINI ISN'T ENOUGH

Chrysler Corp. isn't just buying up Italian companies that build sleek red sports cars. The Highland Park, Mich., auto maker also has its eye on building a broad high-technology base: it plans to acquire Electrospace Systems Inc., a manufacturer of specialized communications and electronics gear, for about $367 million. With revenues of $191 million last year, the Richardson, Texas, firm gets more than 90% of its business from military sales.

GERMAN FIRM BUYS CONTROL OF CALAY

A controlling interest in Calay Systems Inc., an Irvine, Calif., manufacturer of computer-based equipment for printed-circuit-board design, has been acquired by AGIV, a West German holding company, along with Calay's West German parent, Calay GmbH. Calay's role will be to expand its presence in the computer-aided design market, says Peter J. Shaw, the company's president. Although Calay was a CAD pioneer, it became financially troubled before undergoing a turnaround under Shaw, who took over in August 1986.

MICROSOFT, 3COM WILL BUILD OS/2 LAN

Gunning for a front-running position in the coming generation of personal-computer networks, Microsoft Corp. and 3Com Corp. have joined forces to develop and market a local-area-network manager to go with the OS/2 operating system that the Redmond, Wash., software firm is readying for IBM Corp.'s new Personal System/2 line. 3Com's 3+open, based on the OS/2 LAN manager, can tie PC ATs, PS/2s, computers based on the 32-bit Intel 80386 chip, and Apple Corp. Macintoshes into either token-ring or Ethernet networks. The Santa Clara, Calif., firm expects 3+open to be ready by mid-1988, shortly after Microsoft's release of OS/2.

LOCUS TO LINK DOS AND UNIX FOR PS/2

Locus Computing Corp., Santa Monica, Calif., has reinforced its preferred status as a Unix software supplier to IBM. Its newest tie to the giant computer firm is a contract announced early this month to jointly develop the Advanced Interactive Executive operating system for the Personal System/2. The AIX will integrate DOS with Unix for a similar operating system currently available on the RT PC computer. Locus and IBM forged an overall joint agreement in 1983.

GTE LABS GROWS NEW TRANSISTOR

Researchers at GTE Laboratories in Waltham, Mass., are using a radically different process to grow transistors that operate in a manner similar to junction FETs. In a Czochralski furnace they combine silicon and tantalum disilicide, a conductive metal, to simultaneously grow metal connections and silicon crystals. Growing the connections as tiny rods inside a three-dimensional device is simpler and less expensive than depositing interconnect in clean rooms. Some of the devices show maximum blocking voltages as high as 300 V, indicating potential applications in power handling. Results with other devices suggest the process could also be used to produce light-sensing devices for solar cells and cameras.

THE 'PICOSECOND BARRIER' IS BROKEN

Scientists at IBM Corp. have produced electrical pulses lasting only one half of a picosecond, breaking the "picosecond barrier" for the first time. Thus, it is now possible to measure electrical pulses that are up to 20 times briefer than the switching times of the fastest present-day electronic devices. The short pulse has enabled scientists to investigate the electrical behavior of such components as transistors, chip connections, and transmission lines—an important step in designing the ultrafast electronic components of the future.

CDC BUILDING TWO SINGAPORE PLANTS

To supply rapidly growing Far Eastern markets, Control Data Corp. will begin building a disk-drive and media manufacturing base in Singapore late this year. The Minneapolis company expects to invest about $25 million in two factories there over the next five years. One will manufacture the company's Wren II half-height 5.25-in. drives and a high-capacity 3.5-in. drive that is under development. The other plant will make oxide disk media for use by Control Data and for sale to other drive makers. Both plants will be in volume operation next year, the company says.

IBM BUYS X-RAY LITHOGRAPHY GEAR

An electron storage ring will be installed at IBM Corp.'s General Technology division in East Fishkill, N.Y., in 1990. IBM will use the ring to explore the potential of X-ray lithography to fabricate semiconductor devices far denser than those possible with optical lithography. The computer giant has done X-ray lithography research for seven years at Brookhaven National Laboratory in Brookhaven, N.Y. The compact device, which will measure just 6 ft by 15 ft, is the first electron storage ring to be purchased by a U.S. semiconductor manufacturer. The IBM prototype unit will be designed and built by the Oxford Instruments Group of Oxford, England.

SEATTLE SILICON SHUFFLES STAFF

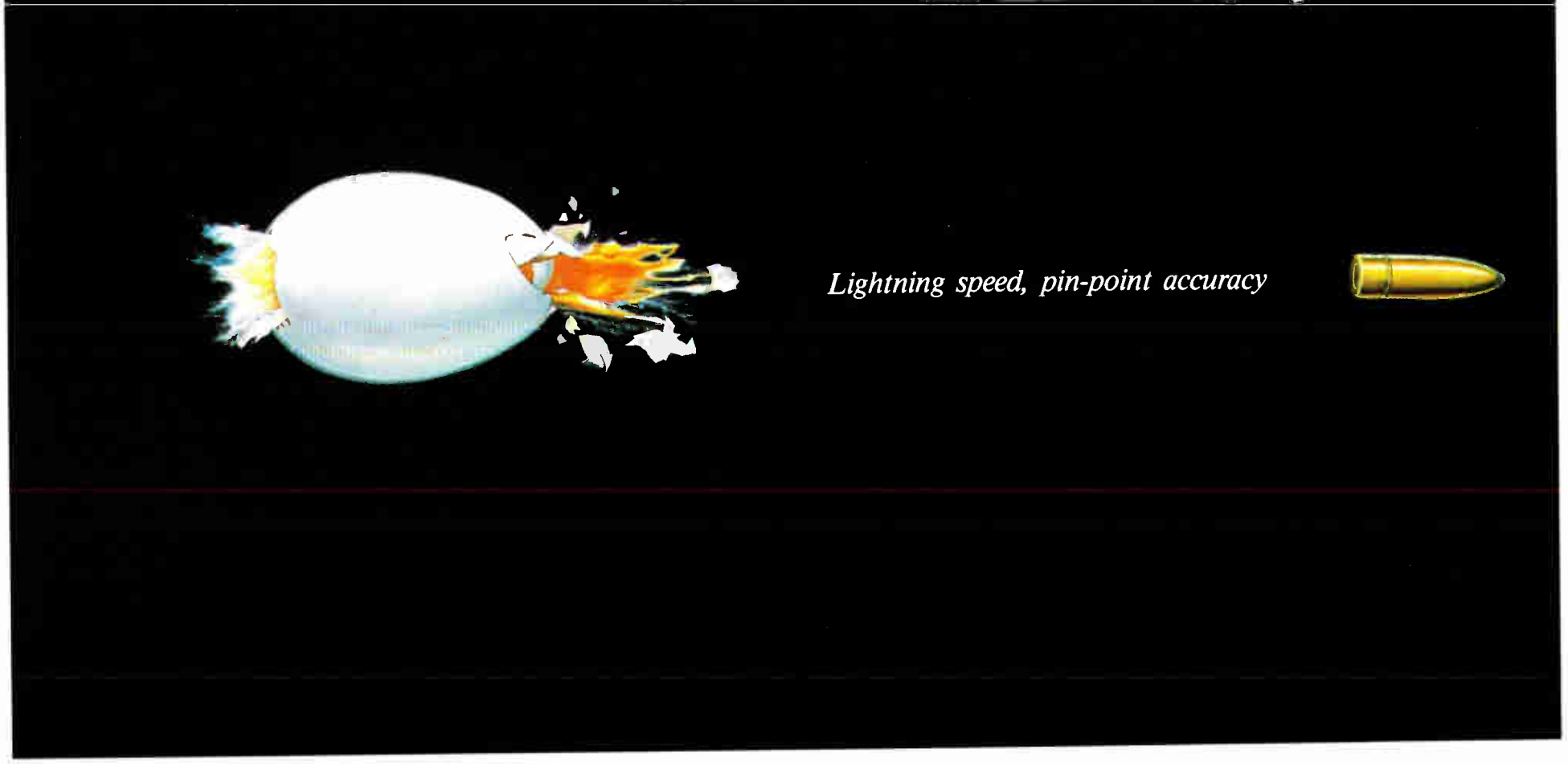
Seattle Silicon Corp. has reorganized its executive hierarchy in an attempt to recover from reportedly slow sales. The silicon compiler firm named Stewart Carrell to succeed president and founder Gordon Kuenster. It also laid off 25 employees and closed its sales offices in three major cities. The Bellevue, Wash., company plans to shift away from custom compiler tools to standardized products.

METHVIN'S BACK WITH 64-BIT MICRO

Pioneer board-computer maker David H. Methvin hopes to raise about $4 million of venture capital to start manufacturing his new 64-bit microcomputer by October. Evaluation units of the instruction-intensive machine, which is produced at Davin Computer Corp., Irvine, Calif., are already in customers' hands. The machine was conceived at Computer Automation Inc., founded by Methvin nearly two decades ago; he acquired the rights to it after leaving the company in 1984. Aimed at original-equipment manufacturers, it will sell for less than $10,000.

CAL. MICRO DEVICES BUYS GTE UNIT

GTE Communications Systems Corp. is selling its Tempe, Ariz., Microcircuits division to California Micro Devices Corp. of Milpitas, Calif. The division makes custom microprocessors, peripherals, and gate arrays for telecommunications systems. It currently meets about 50% of GTE's internal production needs, but those needs will decrease as a result of joint ventures. For CMD, the acquisition provides a reliable source of components—allowing the Milpitas, Calif., firm to concentrate on developing high-performance ASICs and custom and semi-custom chips, sources say.



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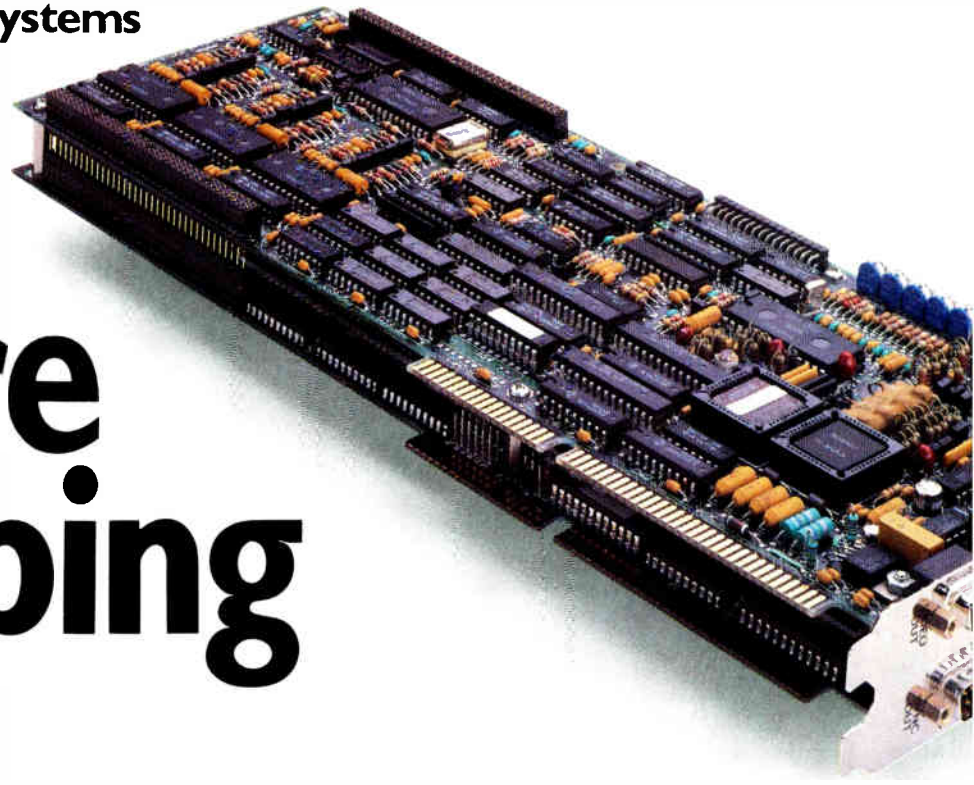

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