SOFTWARE WILL STAR AT THE DESIGN AUTOMATION SHOW/57

NOW THERE'S A STARLAN TRANSCEIVER ON A CHIP/89

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Electronics®

THE WORLDWIDE DRIVE TO TAKE OVER TTL SOCKETS/67

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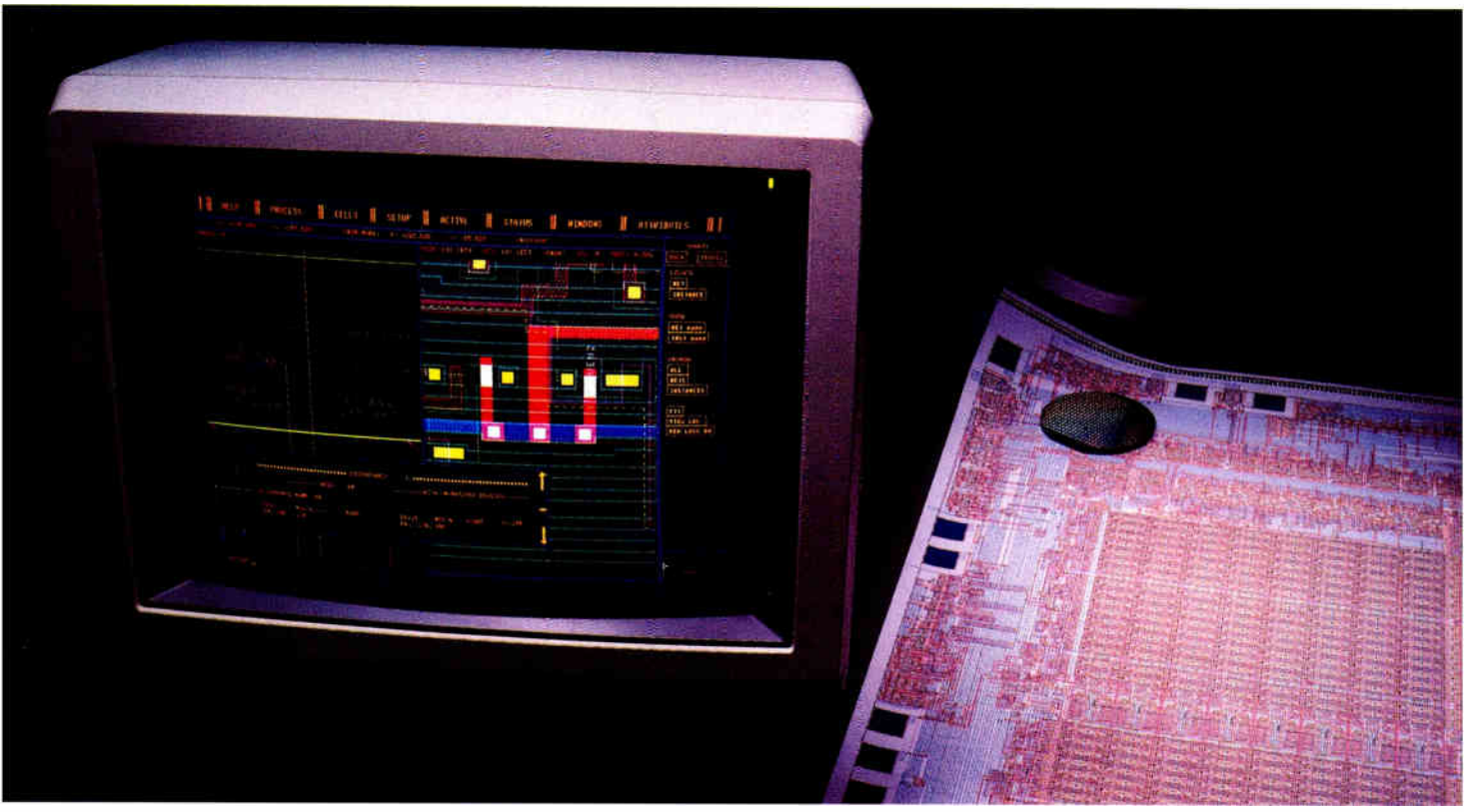
Only Mentor Graphics maps symbols to silicon.



The bigger the IC design, the bigger the problem: you're trying to locate a discrepancy between the schematic and your IC layout, but all you have is an ASCII error report. It's like driving all over a strange city to find an address — without a map.

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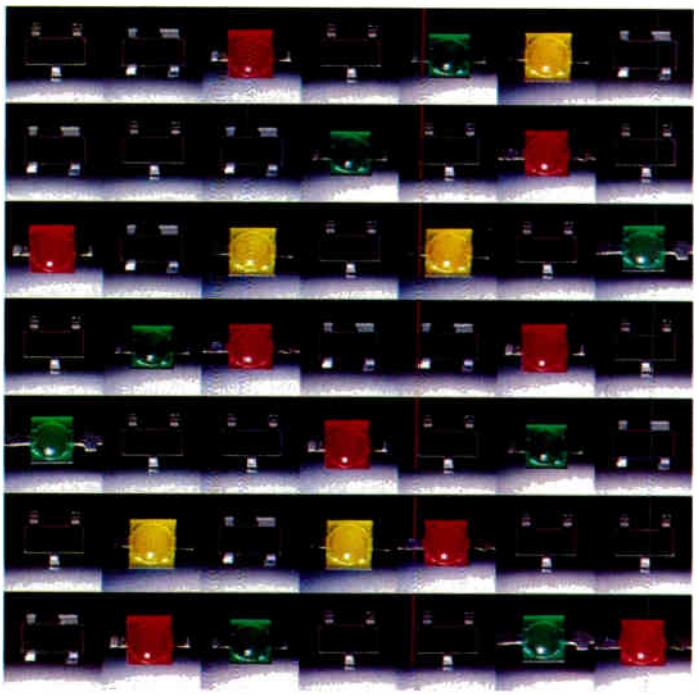

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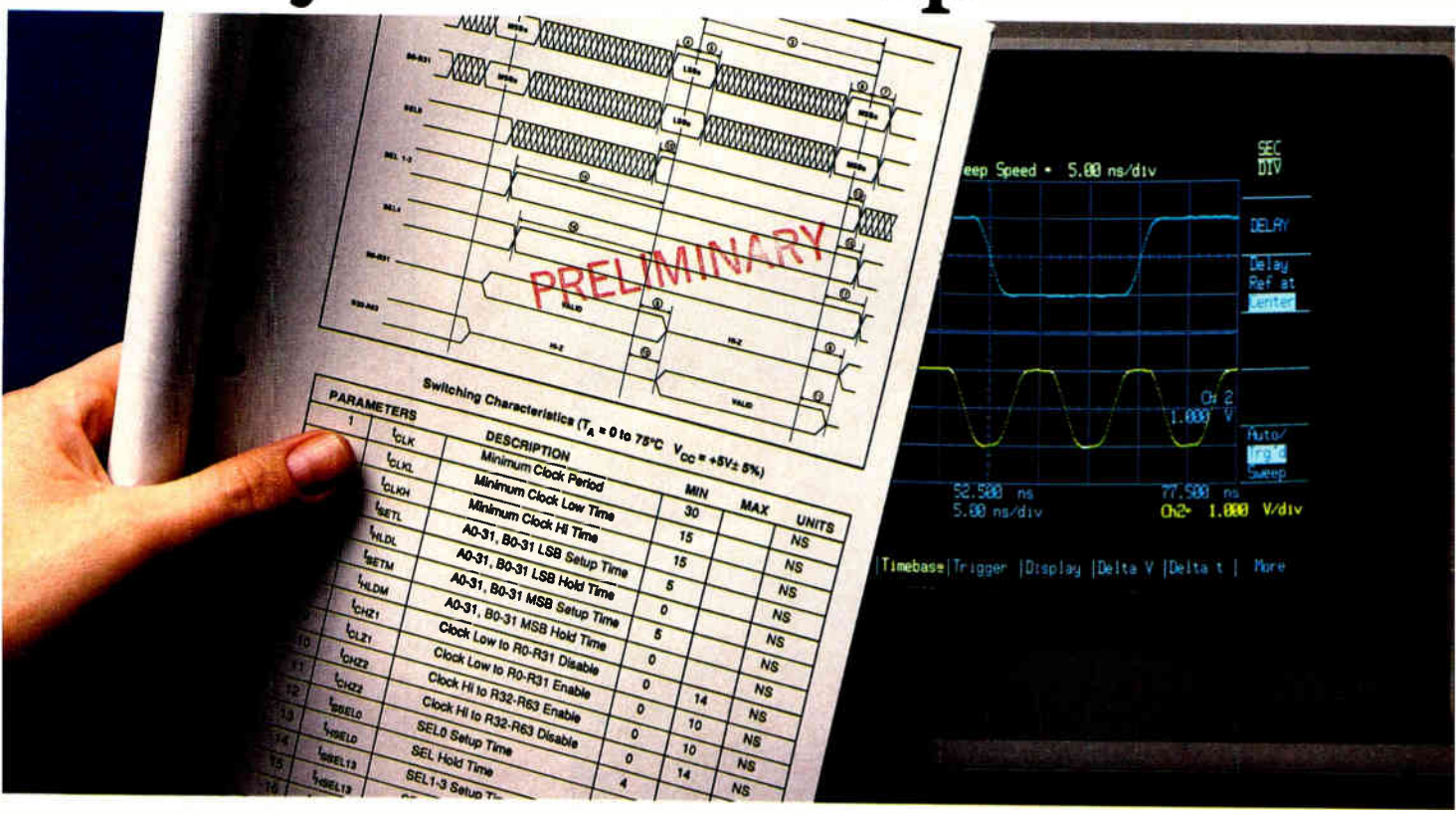

Teradyne J953 VLSI test system waveforms observed with a 1GHz digitizing oscilloscope.

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Electronics

All the talent in the world will get you nothing but a great deal of wasted energy unless it's managed properly. That's a truism in any business, but in a labor-intensive enterprise like publishing it's absolutely fundamental. That's why we consider ourselves fortunate to have added Stan Runyon to the staff.

RUNYON: Management muscle for our team approach.

Runyon arrives at *Electronics* at a particularly important time, just as we are busy fine-tuning and strengthening our team approach to coverage of technology and business news. He has spent 15 years at *Electronic Design* magazine, including a year as editor-in-chief, and just before joining us he was executive editor—the No. 2 person on the editorial staff. Stan, a BSEE graduate of City College of New York, also worked in engineering before becoming an editor. At *Electronics* he will take over the new job of associate managing editor for special projects.

What Stan represents is management experience and expertise. As *Electronics* editor-in-chief Bob Henkel puts it, "Managing a large staff like ours—which, unlike others covering the industry, is scattered around the U. S.—is one of the toughest editorial jobs around, especially when it's involved with a fast-changing industry like electronics."

That's where the team approach comes in. That type of news coverage, with value added to articles and news stories by contributions from our editors around the world, has always been an *Electronics* hallmark. But now we're going to do it even better, and in that way we're going to manage and communicate better as we stay even farther out in front of the leading edge.

What we'll be doing is borrowing a little from industry by setting up a secondary management structure, one that's transient in nature: an editorial team that focuses on putting together a particular package of related articles. It will not replace our basic editorial organization, which is set up along traditional lines—the news section with its bureaus, the technology section with its technical editors, and the support network of copy desk and art and production departments.

In Runyon's view, "It's a doubly exciting way to put together what is already the best technology-coverage package in the business. Not only will it be exciting for the reader, but it will be exciting for those of us who do the reporting, writing, and editing, because we will be using our editorial strengths to the maximum. I'm looking forward to working that way." And it won't take long: Stan is in charge of a special section on application-specific ICs that will appear in the August 6th issue.

Which brings us back to the key to making the system work: management experience. Henkel says, "Since there can be as many as a dozen people on a project, the manager must be like the conductor of a symphony orchestra: even with all the talent, so much depends on the leader. That's where people like Stan come in.

"His kind of leadership is especially crucial at *Electronics*, where we blend so many talents. It's less so for our competitors, where each article rises or falls on the skills of one person."

Laurence Altman

June 25, 1987 Volume 60, Number 13
151,065 copies of this issue printed

Electronics (ISSN 0883-4989). Published biweekly by McGraw-Hill Inc. Publication office: 1221 Avenue of the Americas, N. Y., N. Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N. Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address M C G R A W H I L L N E W Y O R K.

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JUNE 25, 1987

Electronics

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COVER: DAVID MYERS

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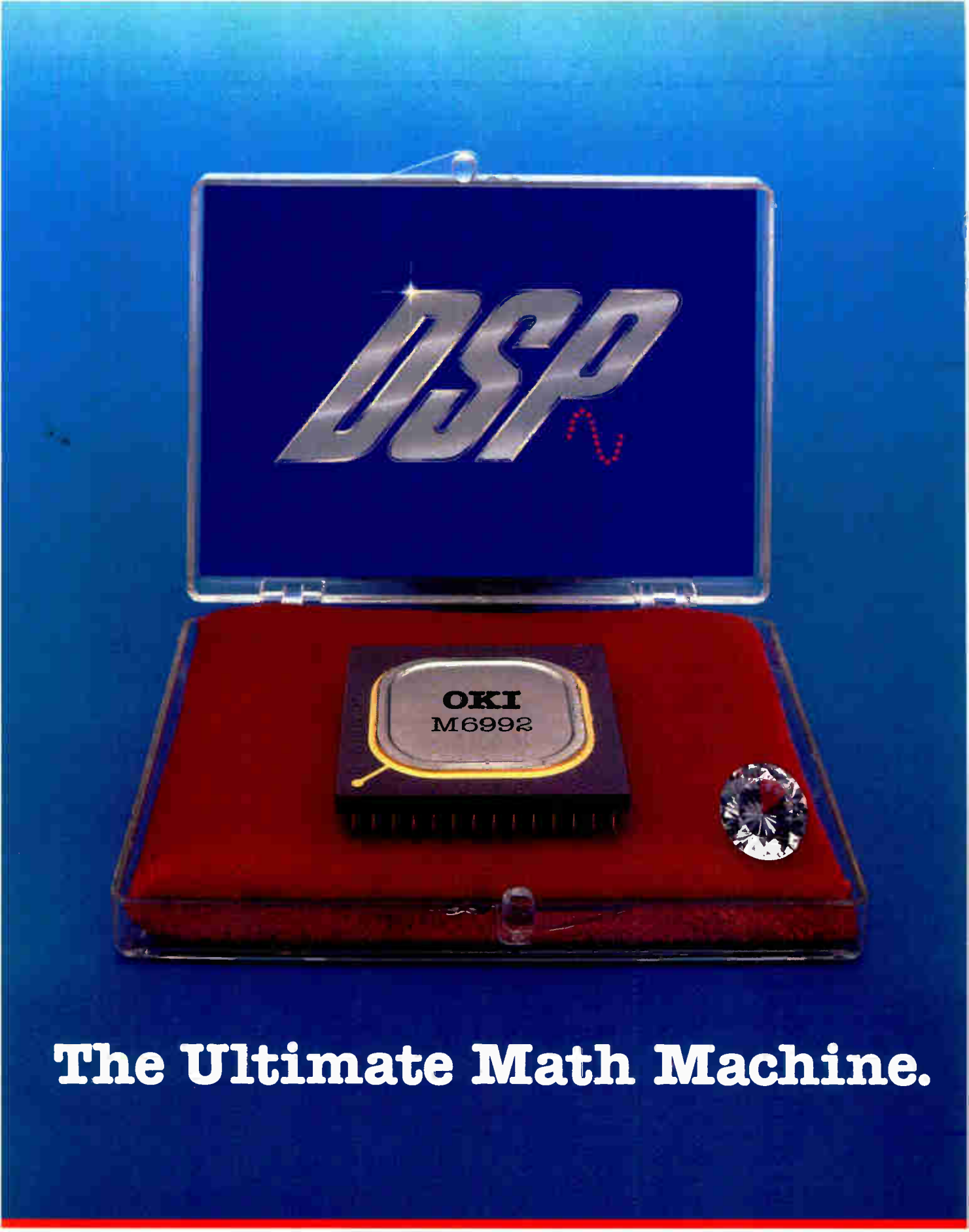

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It seems insane that chip makers would forge ahead with Sematech if it won't provide the production technology that U. S. chip makers need to stay competitive

Sematech, the proposed U. S. semiconductor manufacturing consortium that's to be funded equally by corporate assessments and tax dollars, was still painfully picking its way through the Capitol Hill maze last week in its quest for matching dollars from Uncle Sam. Getting that money now is key, since the chip makers that started the ball rolling aren't willing to put the consortium into operation until it gets a federal commitment. But even if chip makers get that support, there's now a feeling among some production experts that Sematech, as it's now planned, may be all for naught.

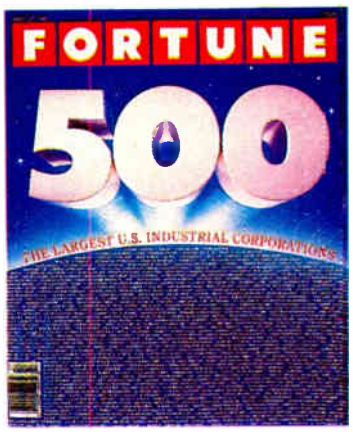
As one production expert puts it: "A compromise was made in order to present a united industry front, but it ended up bastardizing Sematech." It won't help the U. S. semiconductor industry catch up in manufacturing technology with the Japanese, he says, because it is no longer an effective demonstration program.

Two basic changes were made in the original plan: changing the demonstration product from dynamic RAMs to static RAMs and sharply cutting back production volume. The compromise was made to pull Texas Instruments Inc. and IBM Corp. into the fold, our production expert says. "Instead of the original 20,000 wafers a week, output will amount to just a few thousand a week at most," he figures. "You can't demonstrate anything with this; there's no way you can figure costs," he laments. "Anyone in manufacturing knows you have to work a production line full time to obtain maximum yields. Chip making is like paper making—one continuous process. Try turning a paper mill on and off and see what it does to your yields!"

Our expert, who happens to be a veteran manager in the semiconductor-equipment business, also wonders just how Sematech managers will pick their production-equipment suppliers, when there are 30 equipment makers chomping at the bit. "Already the big companies are maneuvering," he says. But he says that it's still not too late to persuade chip makers to agree to the original full-production Sematech. And the discussion is still going on, we understand. With so much at stake and with so much effort already put in, it seems insane that the industry would forge ahead with a version of Sematech if it won't provide the kind of production technology that U. S. chip makers figure they need to stay competitive with the Japanese.

ROBERT W. HENKEL

THINK...



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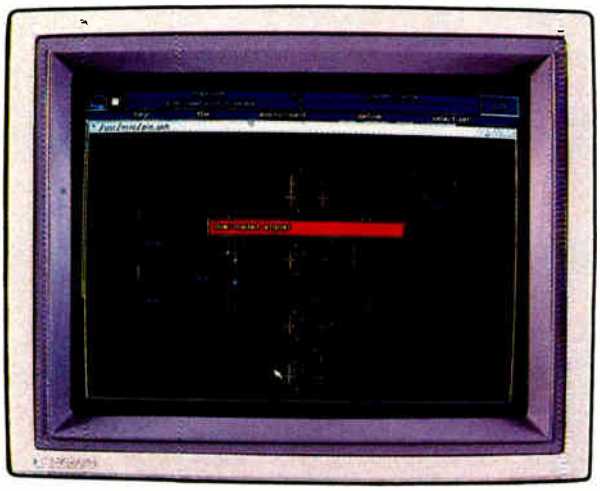

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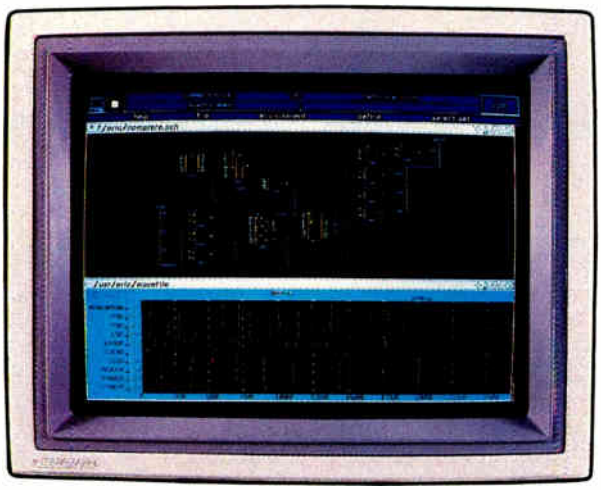
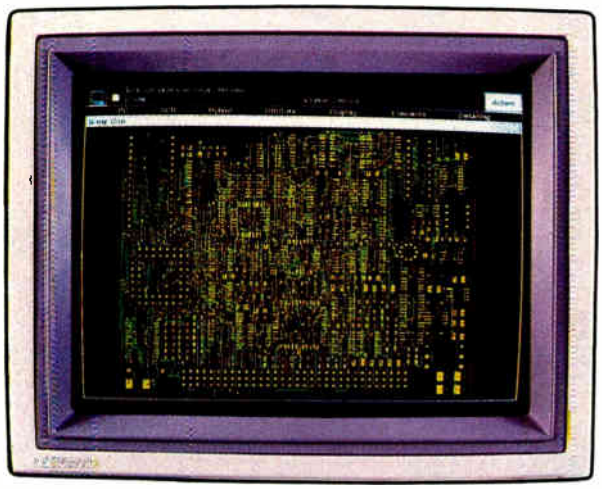


Logic analyzer type display for interactive digital analysis using HILO-3



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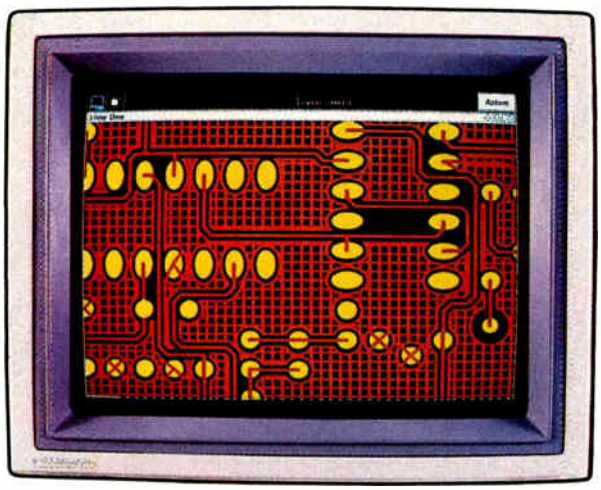

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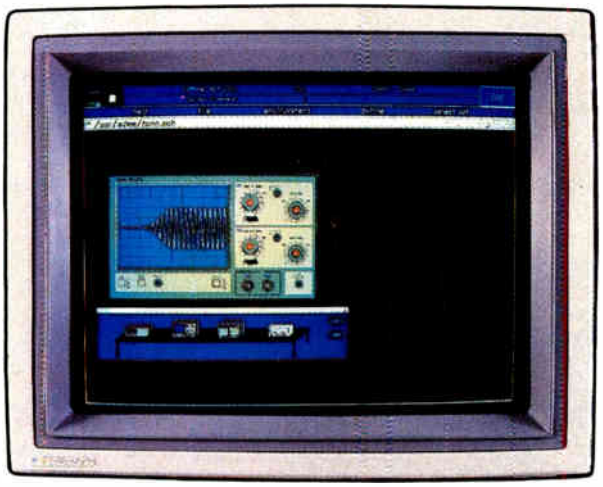

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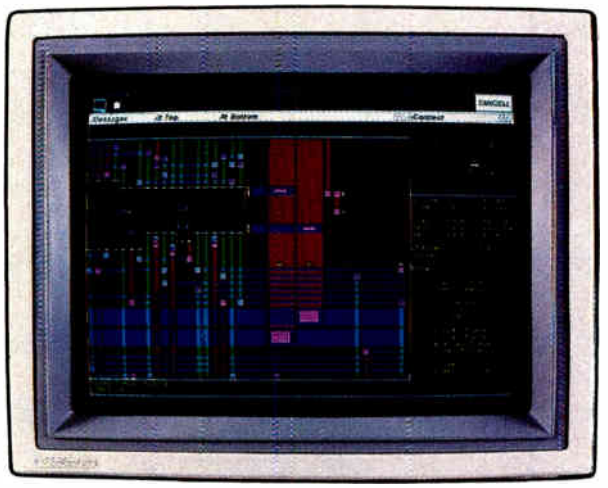

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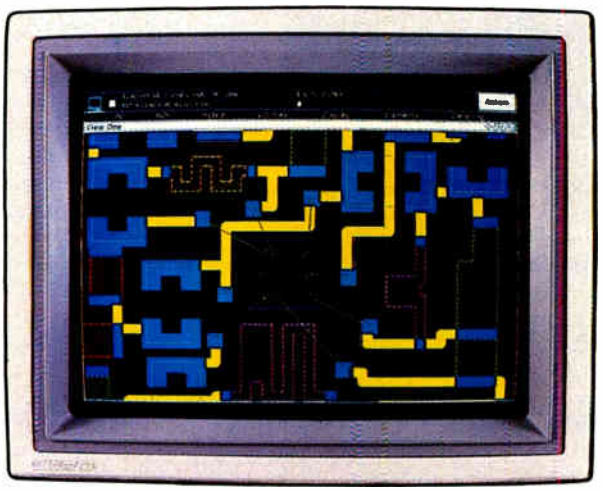

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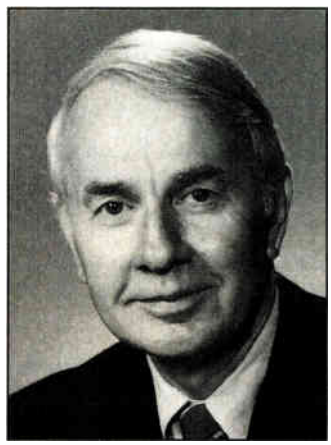
DOVE RETIRES ONE HAT AS HE TAKES OVER AT MCC

AUSTIN, TEXAS

The double life of Grant A. Dove ends July 6. On that date, the 59-year-old native of rural Virginia will no longer have to hold down two demanding jobs: one as executive vice president of Texas Instruments Inc. and the other as a consultant to industry consortium Microelectronics & Computer Technology Corp., where he will take over as chairman and chief executive officer.

The overlap occurred because he was named in March to head MCC, even though his TI retirement doesn't take effect until July. "Phew. I've got two badges, two brief cases, and feel like I've got two different hats to wear," he says. Dove—a well-liked 28-year veteran at TI—has worn the extra hat since he was named by MCC to succeed B. R. (Bobby) Inman, who had guided the co-op since it started in 1983.



DOVE: "I'm an engineer with an interest in the customer."

To MCC officials, Inman had been the strong creative force getting the consortium off the ground. Dove now hopes to bring to MCC new shareholders and a more pliable research portfolio as it enters what he believes is a critical adolescence. Dove predicts that the period will see membership turnover becoming a way of life for research consortiums as the industry continues to exist in a state of flux. In MCC's case, some companies have already resigned [*Electronics*, Jan. 22, 1987, p. 30].

Dove arrives with a perspective different from that of Inman, whose background was in the military and the government. "I'm an engineer with an interest in the customer, and I've always tried to focus on the customer and understand the needs," he says. Dove is a 1951 BSEE graduate of Virginia Polytechnic Institute who began his career at Sperry Gyroscope and later worked at radar supplier W. L. Maxson Corp. before joining TI in 1959. In 1968 he was named vice president at TI, where he headed corporate development. He is retiring as an executive vice president, most recently overseeing such areas as research and development and geophysical services.

"I had 28 years and a lot of blood, sweat, and tears with those guys at TI. Many are my very close friends. I knew the time would come when I would want to do something else," he says softly with a southern drawl. "MCC is not competitive with TI. I hope TI will one day be part of it, if I can convince them it is a good use of funds. So, I could very well wind up working for them again as well as other companies."

At MCC, Dove is hitting the ground running. He needs to deal with the recent loss of members and to restructure and sell potential members on the cooperative's research muscle. As a consultant, he encouraged MCC officials in May to host a technology-update conference for U. S. electronics companies that don't belong to the consortium yet.

That was followed by letters to chief executives of 50 prime candidates for MCC membership, says Dove. In June, he has called on several he thinks would benefit from one or more of the co-op's programs in chip packaging, software, computer-aided design, or advanced computer architecture. Dove is also pushing for a new startup program in superconductive materials (see p. 31).

In addition, the computer-architecture program is being restructured to cut minimum dues to $1.2 million, from more than $3 million a year, and thus attract more members. The reshaped program would allow participants to focus on near-term technology interests in artificial intelligence, human interfaces, or systems technology. Core technology from those three would be available. "We think we will appeal to some small developing companies, which are faced with changing their strategies as they make a transition from $250 million and $500 million size to $1 billion," he adds.

"I'm hoping that we will be able to speak the language of our customers," says Dove, referring to the challenge he and MCC face in the era ahead. "So my people are having to explain to me what they are doing in customer terms, in addition to using a scientific language. In addition, I'm encouraging our CEO members to help us describe what is being done with the technology and how they are using it," he adds (see p. 31).

–J. Robert Lineback

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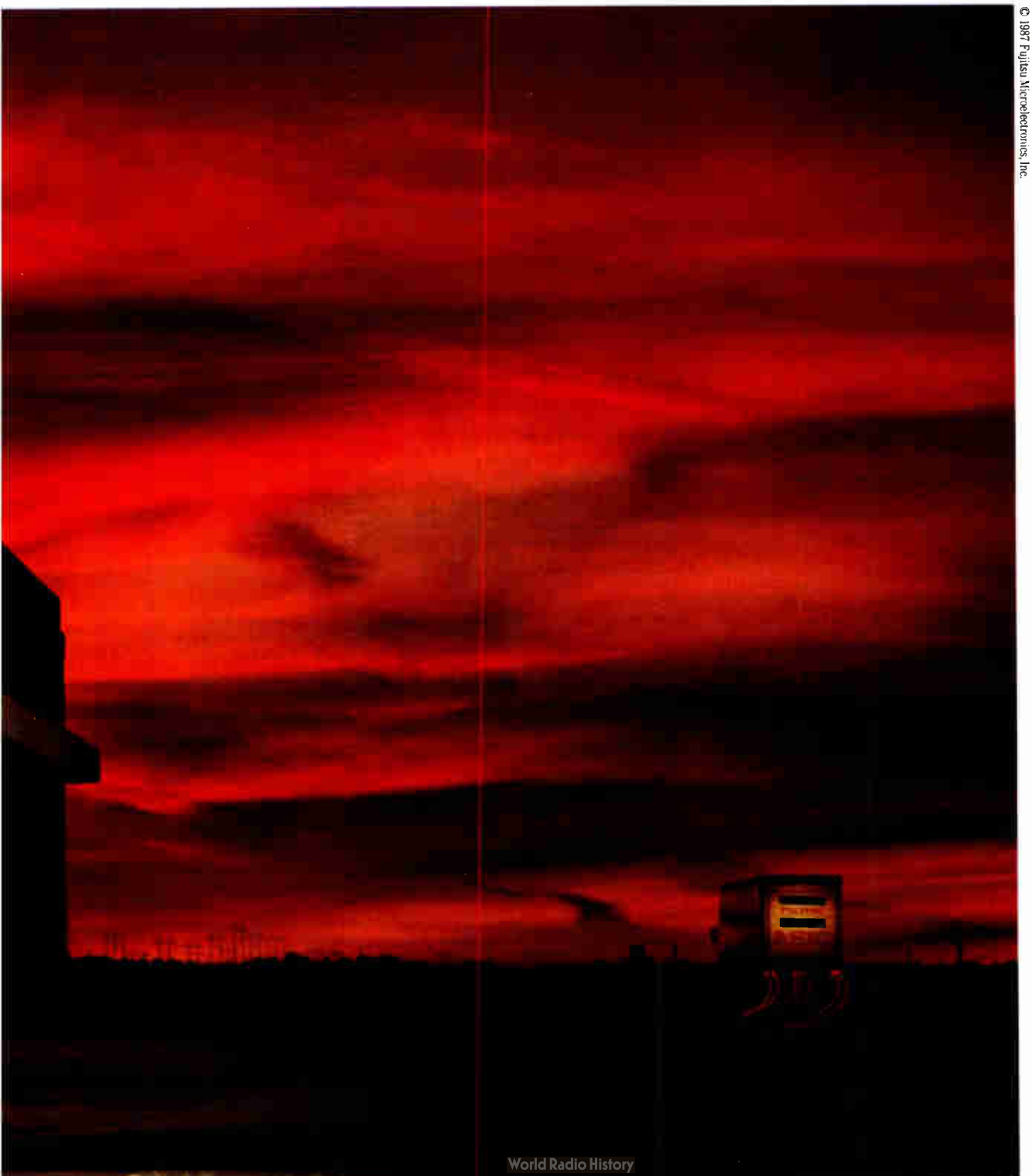

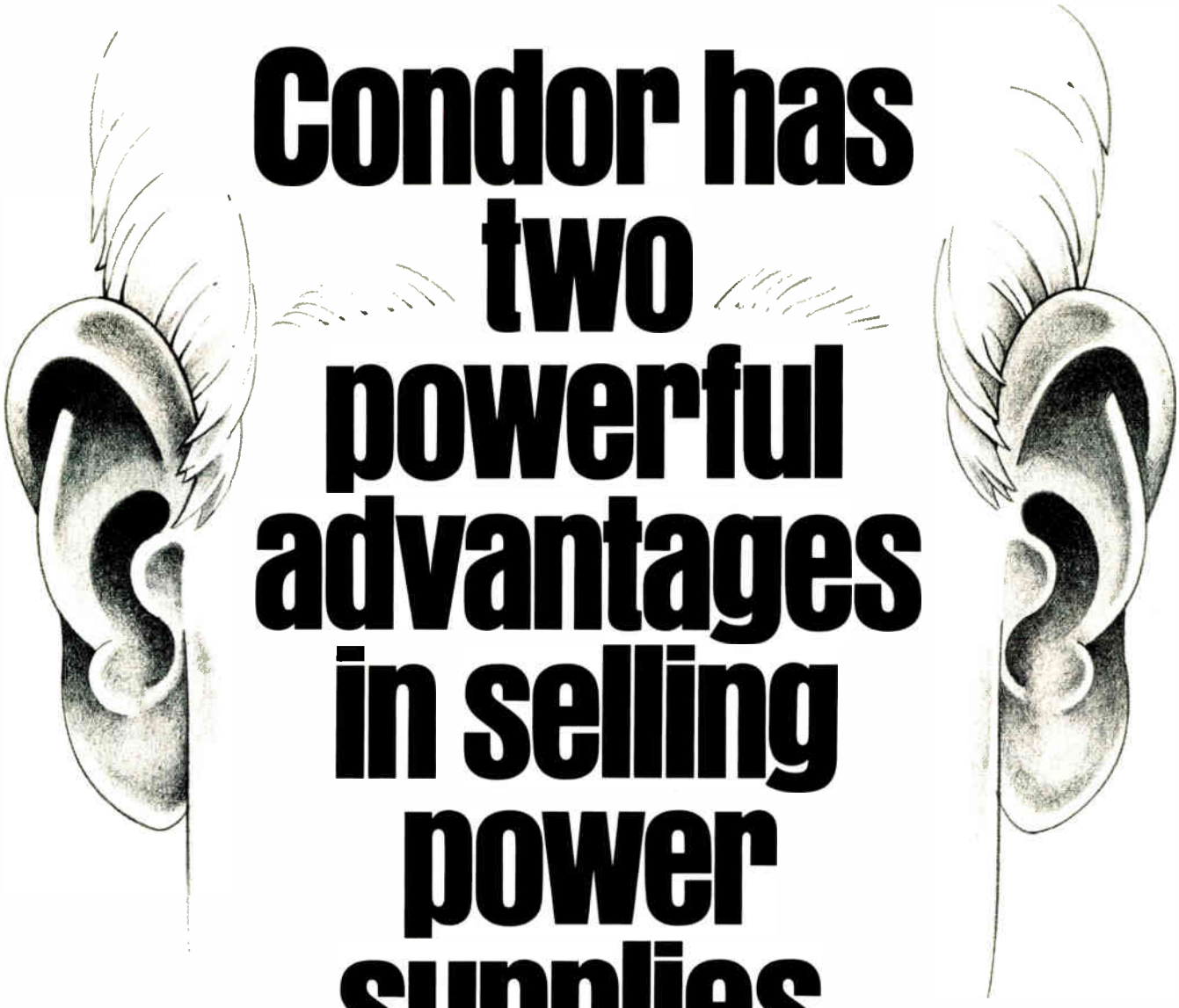

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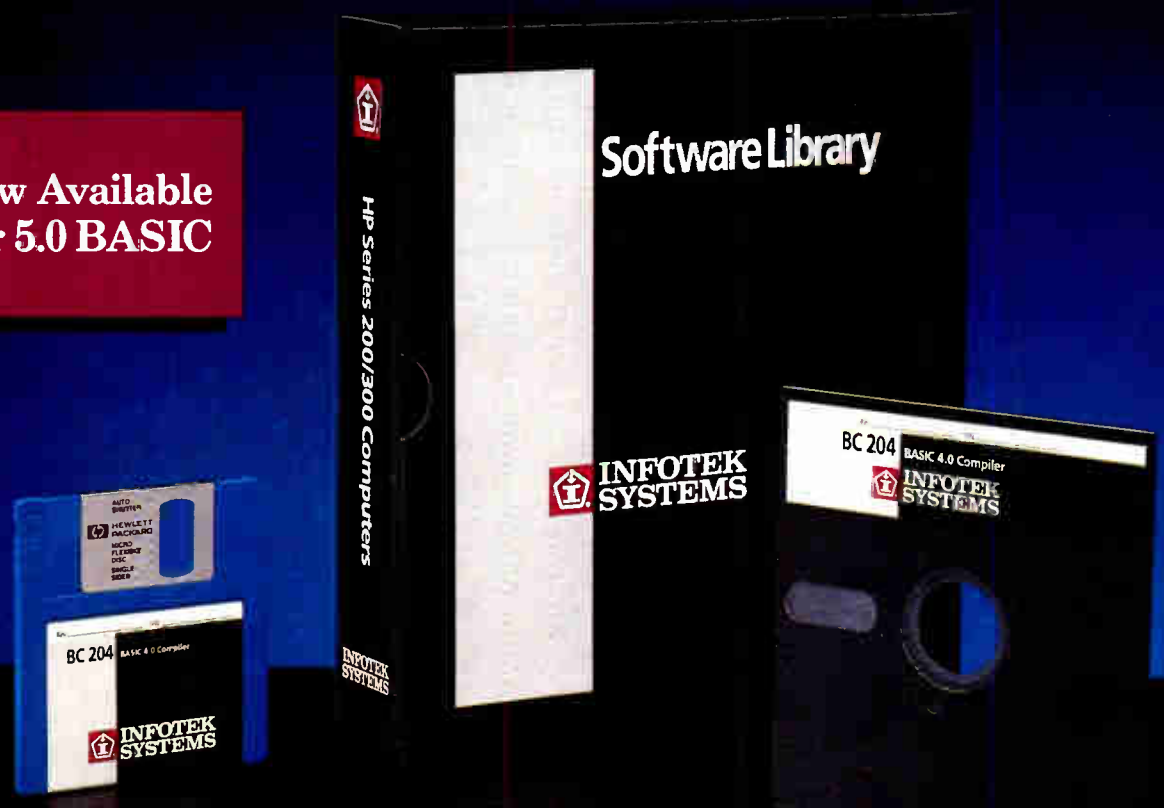

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ELECTRONICS NEWSLETTER

GE RETURNS TO COMPUTER FRAY WITH 100-MEGAFLOPS WARP MACHINE...

General Electric Co. is returning to the commercial computing business. The Fairfield, Conn., company, which sold its mainframe computer operation to Honeywell Inc. back in 1970, is now about to release a commercial version of Warp, a high-speed systolic-array-based processor that it developed under the Defense Advanced Research Projects Agency's Strategic Computing Initiative. The system, which will cost about $350,000, features peak speeds of 100 million floating-point operations/s and will hit the market "within the next few weeks," the company says. The machine is based on work done at Carnegie Mellon University in Pittsburgh, Pa. [*Electronics*, Aug. 20, 1984, p. 24]. GE has already delivered several machines to Darpa for use in high-speed image-processing tasks; they consist of 10 processor boards, each a linear systolic array capable of performing 10 megaflops. Now GE is eyeing applications such as medical image processing, finite-element analysis, and scientific computing. □

...AS INTEL BEGINS TO DEVELOP AN EVEN FASTER WARP CHIP

With General Electric Co. about to start selling its Warp processor, Intel Corp., of Santa Clara, Calif., is gearing up an effort to reduce the Warp architecture to a single chip, according to H. T. Kung, leader of the group at Pittsburgh's Carnegie Mellon University that developed the Warp system. Each chip, coupled with memory, will be the functional equivalent of one of GE's Warp boards, but will be capable of running 200 million floating point operations/s—twice that of the GE product. Kung says the Intel chips will be used in a system, called iWarp, that should reach the market around 1990. Before that, Carnegie Mellon expects to take delivery of three 72-cell systems, each capable of running 1.4 billion floating point operations/s. □

A SOLID-STATE SOLUTION FOR INDUSTRIAL GAS MONITORING

Solid-state technology based on a unique, acousto-optic crystal material from Westinghouse Electric Corp. could soon have a big impact on industrial gas monitoring. The Westinghouse Combustion Control Division, Orrville, Ohio, plans to introduce a gas-analysis system in October that uses an acoustically tunable infrared filter made from single-crystal thallium arsenic selenide. When packaged with a radio-frequency transducer, the crystal serves as a variable diffraction grating for infrared light. The crystal can be tuned to specific wavelengths by varying the sound waves applied to the material by the rf transducer. Then, because chemical compounds are identifiable by the wavelength of IR light they absorb, the device can detect whether specified compounds are present in a smokestack. Current gas-analysis techniques typically require the physical extraction of a gas sample, or the use of mechanical filter wheels, spinning gas cells, moving mirrors, or mechanical light choppers. □

AT MAXTOR, A PARTS SHORTAGE IS DEPRESSING EARNINGS

Maxtor Corp. of San Jose, Calif., the Winchester disk drive maker that has outperformed the industry while growing faster than 100% per year [*Electronics*, June 11, 1987, p. 49], has had to slow production of two products it was counting on to keep its growth rate going. Citing a shortage of critical parts from its suppliers, the company says that it is shipping its new 380-Mbyte EXT-4000T and 760-Mbyte XT-8000E 5¼-in. Winchesters "in quantities less than our customers expected." H. J. Kilsdonk, director of marketing, says the problem won't last long, however, adding that he expects "to be out of the woods in the next four to six weeks." □

ELECTRONICS NEWSLETTER

MARRYING ECL LOGIC TO RAM IN ASIC YIELDS 5-NS ACCESS TIMES

Marrying a fast dynamic random-access-memory array and emitter-coupled logic on the same chip, two new application-specific integrated circuits from Fujitsu Ltd. keep memory-access times down to 5 ns. By eliminating output buffers between logic and memory, the ASICs cut about 15 ns off access times of systems that depend on separate logic and memory chips. They also cut total energy consumption in half—down to 8 to 10 W per chip. The ET-2009M has 1,920 logic gates and 9 Kbits of RAM, and the ET-3004M offers 2,880 logic gates and 4.5 Kbits of RAM. The devices can be cooled by a 5-m/s airflow, so they are well suited for the next generation of minicomputers that target 10-million to 15-million-instruction/s performance. Fujitsu says application development takes five weeks and costs about $34,500, but the parts are initially being offered only in Japan. The chips themselves will cost between $300 and $350 each in 500-unit purchases. Fujitsu is expected to start U. S. sales in the near future. □

HOW IBM SOLVES A GaAs PROBLEM WITH JUST A LITTLE WATER AND LIGHT

Scientists at IBM Corp. have discovered a simple solution to pinning, one of the biggest problems holding back development of gallium arsenide integrated circuits. Pinning is caused by small quantities of arsenic that build up on a wafer's surface, making it a difficult base on which to implement circuitry. But by spraying a stream of purified water onto the wafer surface while at the same time exposing it to ordinary light, researchers at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y., discovered they could create a photochemical reaction that washed away the excess arsenic. In the past, designers have avoided pinning problems by putting down layers of aluminum gallium arsenide over the GaAs substrate, but that is expensive and complicated. □

HOW ONE GROUP GAINS FROM TRW'S PLAN TO QUIT COMPONENT MARKET

TRW Inc. may be selling most of its electronic-components businesses, but the company is not totally abandoning the commercial semiconductor market. It is holding onto the LSI Products Division, which will be its only semiconductor unit making outside sales. TRW is positioning the unit to be a more focused military supplier by giving it responsibility for marketing chips from Phase 1 of the Very High Speed Integrated Circuit program. The La Jolla, Calif., division currently sells about half of its data-acquisition and digital-signal-processing devices for military applications. LSI Products, one of the few organizations that has been successful in transferring military technology into the commercial arena, was started in 1977 to sell bipolar products developed for military hardware. Now, under a plan announced in June, it will become part of TRW's defense-oriented Electronic Systems Group. □

VARISTORS ON A PIN: A NEW WAY TO SAVE PC BOARD REAL ESTATE

Systems designers have long recognized the value and need to build power surge protection into most systems, but they pay a price for such suppression devices: they take up valuable board space. In designing a varistor small enough to fit like a sheath around the pins in a connector housing, however, the GE/RCA Solid State Division may have solved the problem. The company's new connector pin varistor can net board designers as much as a 15% space savings. But it will cost them—GE/RCA will charge almost 10 times as much for the new parts as for standard metal oxide varistors, which typically cost less than 50 cents. The company is aiming the new parts at military markets, where saving space is most vital. □

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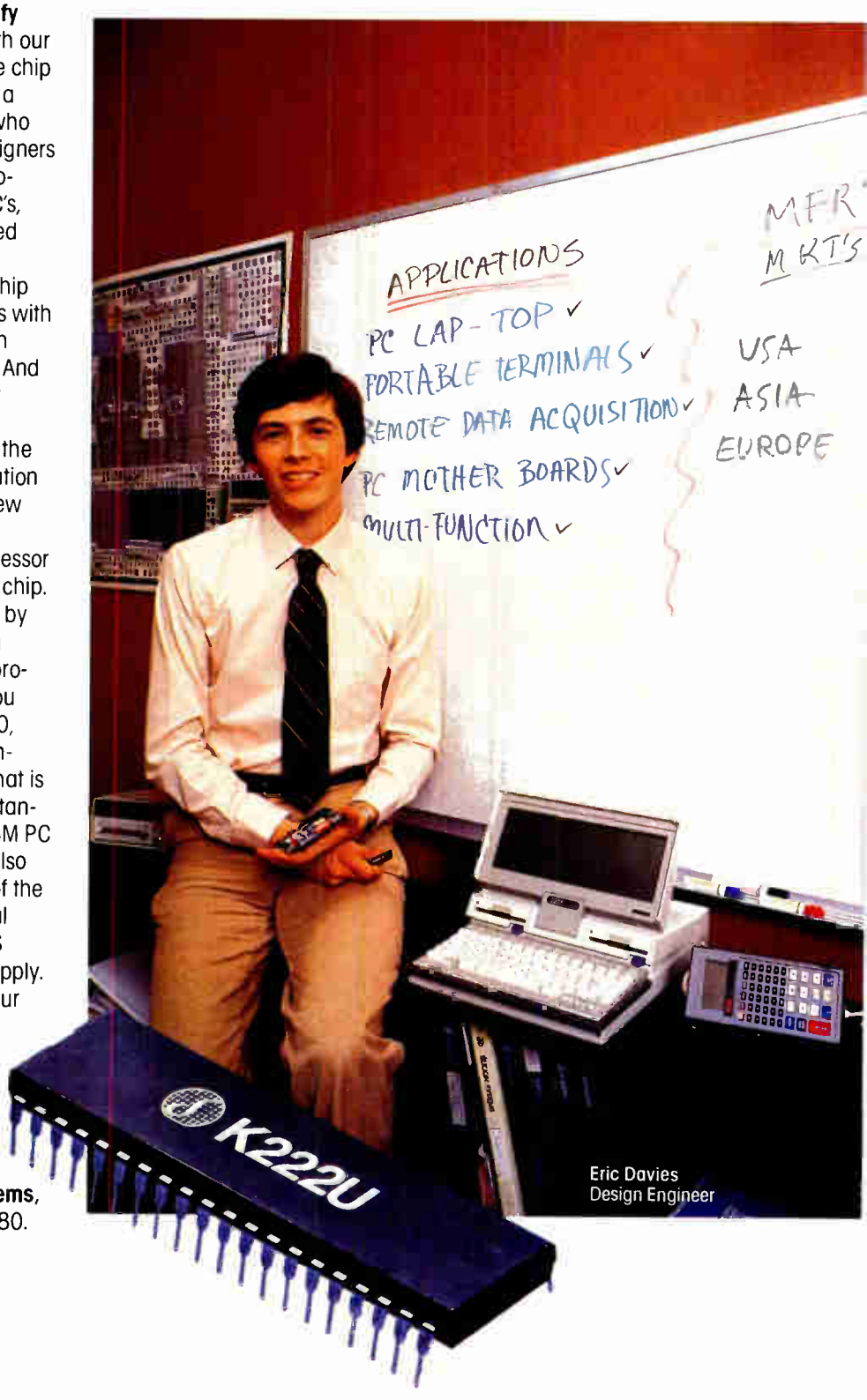

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Design Engineer

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For more information on the SSI K222U, or the complete K-Series family of compatible modem IC's, contact: **Silicon Systems**, 14351 Myford Road, Tustin, California 92680.

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DT2851 Frame Grabber	512x512x8	✓	✓	✓	$2995
DT2858 Processor					$1695
DT2853 Frame Grabber	512x512x8	✓	✓	✓	$1595
DT2803 Frame Grabber	256x256x6	✓		✓	$1495

Array Processing

Model	FFT* 1024 Point Real	FFT* 1024 Point Complex	FFT* 256x256 Image	Software	Price
DT7020 Floating-Point Array Processor	13ms	23ms	1.57s	✓	$6595
DT7010 Floating-Point Array Processor	23ms	41ms	3.9s	✓	$4995

*All execution speeds are real-world, not theoretical, and include overhead times.

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DT2841	✓	✓	✓	40–750kHz	✓	$1450–$2995
DT2811	✓	✓	12-bit	20kHz	✓	$199–$745

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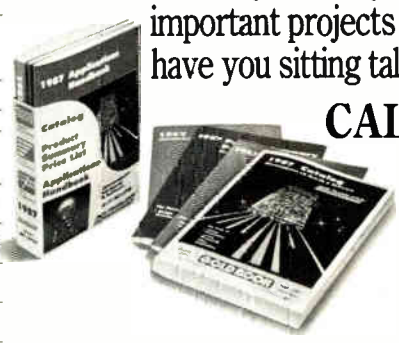

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PRODUCTS NEWSLETTER

FAIRCHILD GUARANTEES THESE PLAs WILL RUN AT 10 NS

A family of 10-ns programmable logic arrays from Fairchild Semiconductor Corp. aims to shoot holes in the theory that blazing speed and TTL programmable logic don't mix—and the company will guarantee it. The FAST-PLA family, fabricated with the company's oxide-isolated Isoplanar FAST-Z technology, is not the fastest PLA line available—some commercial emitter-coupled logic parts run at 5 ns—but it is the only family with a 100% speed guarantee. The Cupertino, Calif., company guarantees performance because instead of designing with conventional metal-link fuses, Fairchild uses vertical cells coupled with on-chip test circuitry that allows full preprogramming ac and dc testing. Instead of blowing fuses and hoping for the best, designers can test the logic pattern's speed. FASTPLA parts operate at up to 70 MHz and are functionally equivalent to standard 20-pin PLA devices. Samples are available now, with production quantities expected in the third quarter for $8 each in 100-piece quantities. □

HITACHI 16-KBIT ECL RAMs ACCESS IN ONLY 10 NS

BiCMOS 1.3-μm technology developed for Hitachi's 64-Kbit emitter-coupled-logic-compatible random-access memory [*Electronics*, March 19, 1987, p. 26] has been adapted to a new series of 16-Kbit devices that feature even faster access times: only 10 ns maximum, a 33% improvement over the 15 ns of the 64-Kbit parts. The speed is possible because word lines are shorter with the new devices. The devices come configured as either 16-K words by 1 bit or 4-K words by 4 bits in both ECL10K and ECL100K versions. All are available in Cerdip packages. Typical power dissipation for the HM100484 4-K-by-4-bit chip is 630 mW. The price for samples is $69.20 (10,000 yen). In 1,000-unit lots, the devices cost $48.44 each (7,000 yen). □

PLUG-IN CARD HANDLES LOGIC ANALYZER'S JOB FOR A TENTH THE COST

Crowcard II from Applied Physics Inc. performs like a one-shot logic analyzer in diagnosing problems in the bus of an IBM Personal Computer. But at $589—5% to 10% of the full-featured logic analyzer's price—it's a real buy for PC hardware and software developers. Like the original Crowcard from the West Lafayette, Ind., company [*Electronics*, Oct. 16, 1986, p. 138], Crowcard II plugs into an expansion slot on a PC, PC/XT, or PC AT. But it goes beyond simple bus-monitoring functions and freezes bus activity of a single cycle on a predetermined trigger. Triggers—such as the central processing unit's execution of a particular command—are preset with DIP switches. When triggered, the Crowcard II automatically latches the light-emitting diodes used to monitor the bus, providing an LED snapshot of the cycle. The Crowcard II will be available in July. □

DATA GENERAL'S MILITARY SUPERMINIS DOUBLE INDUSTRY'S BEST PERFORMANCE

Military contractors looking for secure or rugged superminis have a new range of options from Data General Corp. that delivers almost twice the performance of current military-qualified systems. Models of both the Tempest and the rugged versions of the six-month-old Eclipse MV/15000 cover a performance range from 2.9 to 6.4 million instructions/s—power the Westboro, Mass., company claims is the best on the market. The rugged MV/15000R computers meet military standards for shock, vibration, temperature, and humidity. They range in price from $117,500 to $284,000. The MV/15000T Tempest models meet the NACSIM 5100A military-security specification and cost between $177,000 and $299,000. The computers will be available in the fall. □

PRODUCTS NEWSLETTER

COPROCESSOR BOARD TRIPLES SPEED OF VAX-BASED SYSTEMS

System developers using Digital Equipment Corp.'s MicroVAX as a central processing unit can boost speed threefold by offloading number-crunching programs to a coprocessor board from Avalon Computer Systems. The AP/20 Attached Processor gets its kick from an Intel Corp. 80386 32-bit microprocessor running at 3.5 to 4 million instructions/s with a floating-point multiply time of 437 ns, says the Glendale, Calif., firm. The board needs no source-code changes, but code must be recompiled on an Avalon compiler. Compatible with any Q-Bus VAX system, multiple AP/20 boards can boost performance as much as 10 times and can run several programs concurrently. One gigabyte of protected virtual-address space and 4 Mbytes of real memory are included at the single-unit price of $10,000. Delivery is 30 days. □

CONNER'S 3½-IN. WINCHESTER COMES WITH A BUILT-IN CONTROLLER INTERFACE

Conner Peripherals Inc. is offering original-equipment manufacturers who put 3½-in. Winchester disk drives in their IBM Corp. PC-compatibles an integrated PC AT bus interface. All competing 3½-in. drives require an outboard controller, and although equipment costs of the two systems are comparable, Conner's solution saves OEMs the cost of qualifying and integrating a controller. The San Jose, Calif., company's 40-Mbyte CP342 also boasts better performance than its competitors. It offers 29-ms average access time, 6-W operating power, a noise level of less than 35 dBA, and shock resistance of 75 g. By contrast, the 3½-in. drive in a standard IBM Personal System/2 and PC AT has a 40-ms access time, 28 W operating power, a 45-dBA noise level, and a shock resistance of 25 to 40 g. Available now, the drives cost $785 each; OEM discounts are available. □

ZEHNTEL CUTS TEST-DEVELOPMENT TIME FROM MONTHS TO WEEKS

By adding functional testing to in-circuit testing, Zehntel Inc.'s 850 F/I board tester eliminates the need for traditional simulation techniques—allowing users to create a test with high fault coverage in two weeks instead of the usual six or more months, says the Walnut Creek, Calif., company. Functional testing gives the 850 F/I the ability to handle interactive or timing faults in parts of the board, such as surface-mounted devices, that are inaccessible to in-circuit test probes. In the past, that inaccessibility meant simulation was required. The system can also take advantage of self-test capabilities built into microprocessor-based boards for running an at-speed functional test. It includes a graphics work station based on the Macintosh Plus and an integral 16-channel logic analyzer. The price of an 800-node tester is $263,000, and Zehntel is scheduled to begin the first shipments in July. □

IF YOU CAN PRINT, THIS GADGET LETS YOU INPUT TO A PC

By using artificial-intelligence software to recognize hand-printed characters and numerals, Communication Intelligence Corp. has given system integrators an easy-to-use input device for personal computers. Handwriter is designed to replace unwieldy keyboards in applications such as inventory management, form-filling, and data entry. Introduced at last week's National Computer Conference in Chicago, Handwriter consists of a digitizing tablet and pen, plus an associated 68000-based processor that runs the AI package. A Japanese version of the system can recognize 3,000 ideographic characters. That version will be available in the third quarter. The Menlo Park, Calif., company is readying a U. S. version costing between $600 and $1,000 for introduction by the end of the year. □

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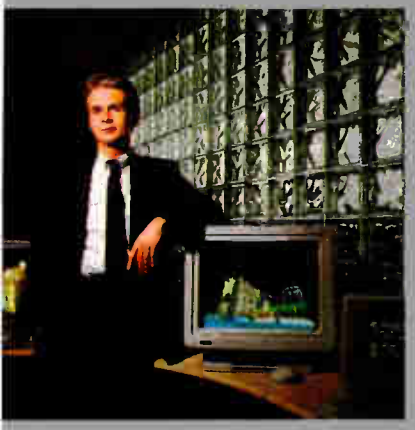
In Mr. Curry's view, Digital's ability to network, plus compatibility from individual workstations to huge processors are ideal for the architectural community. "For any building project to progress smoothly, there has to be a coordinated effort. The group working on lighting, for example, needs to share information



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with those designing heating and ventilation. In the Digital environment, that's exactly what they do."

"In our own marketing efforts," adds Mr. Curry, "Digital offers two enormous competitive advantages. Planning for the future is easier because of Digital's commitment to compatibility. And we do very little selling of Digital to our customers – engineers are already sold." To get your competitive advantage now, write: Digital Equipment Corporation, 200 Baker Avenue, West Concord, Massachusetts 01742. Or call your local Digital sales office.

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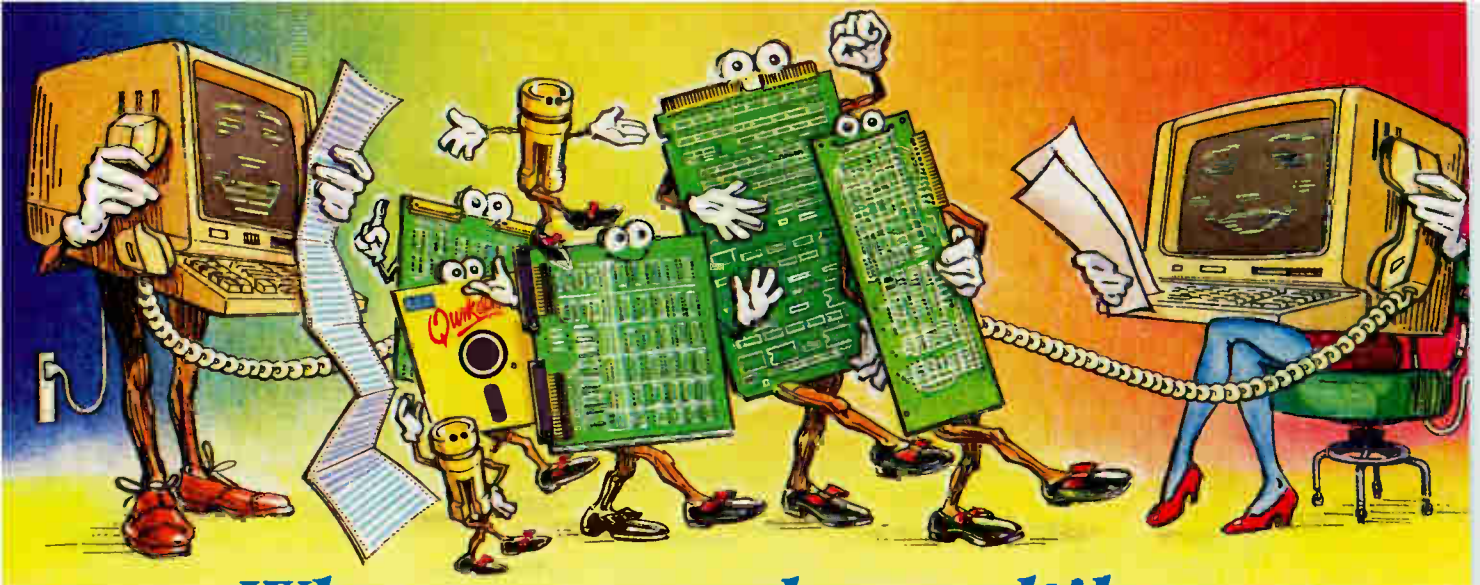

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Electronics

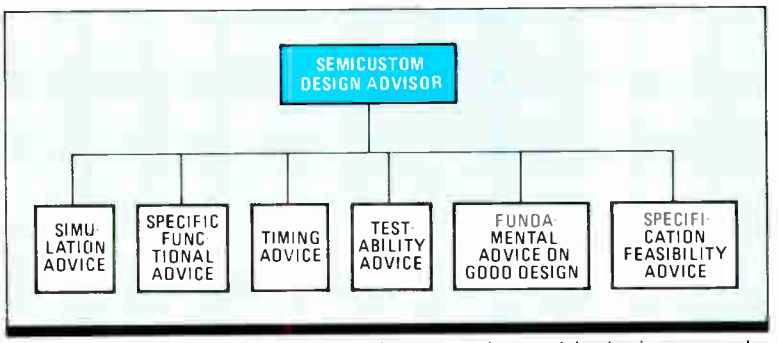
HERE'S AN AI SYSTEM THAT CHANGES ITS MIND FASTER

FIRST PRODUCT BASED ON MCC TECHNOLOGY, IT SPEEDS CHIP DESIGN

FORT COLLINS, COLO.

Getting expert systems to revise their knowledge is a slow and unwieldy process. But now NCR Corp. is preparing to go to market with one that not only gives up faulty assumptions and changes its beliefs with ease, but does it fast.

The NCR Design Advisor is to be used for designing semicustom chips and is the first commercial product based on technology developed by Microelectronics and Computer Technology Corp., the industry's research consortium. For MCC, whose critics have been saying that member companies are not getting their money's worth, the NCR product couldn't come at a better time (see p. 32).



DESIGN AID. The NCR Design Advisor gives an engineer advice in six areas as he designs semicustom CMOS chips from a library of standard cells.

The NCR system uses ground-breaking technology that integrates knowledge and rules into a single, easy-to-use data base. Built atop MCC's latest version of a hybrid expert-system shell called Proteus 2.0, it will be set up initially to give advice to customers designing their own semicustom chips from a digital CMOS standard-cell library. The tools will also be used on NCR gate arrays and eventually for analog-circuit design.

In essence, the system eliminates human engineering errors before other computer-aided-design tools begin their work. To keep the expert system from pestering human engineers, it understands and reasons about circuit design directly from the net list—the circuit description. Whenever the designer is ready, the system can be asked to look over a design and explain its inferences; the program will ask questions only when ambiguities emerge.

Working from the net list, Design Advisor can give detailed recommendations for improved performance, testability, and manufacturing yields at any point in the design routine. According to initial studies of particular designs, 66% of the problems could have been caught by the system, and 70% of the timing-related problems would have been found.

The NCR system ferrets out problems by taking full advantage of the unique truth-maintenance feature of Proteus 2.0. In operation, NCR engineers will periodically insert new knowledge gleaned from users. Proteus accepts such information because it is a logic-based nonmonotonic reasoning system, which unlike fixed-truth monotonic programs can automatically revise inferences by retracting faulty assumptions when new beliefs are entered into the program. In this area, a key contribution of Proteus to expert-system technology is the way it guides the mechanism that performs contradiction resolution, using a method known as dependency-directed backtracking.

NCR will first offer the system as a service to customers in early fall, charging $4,000 to $8,000 depending on chip complexity, says H. Gene Patterson, director of the semicustom business unit in NCR's Microelectronics Division at Fort Collins, Colo. Designs will be entered into the system via dial-up modems or by NCR engineers in Fort Collins. A typical design will be evaluated within one day, using Lisp-computing hardware from Symbolics Inc. at the NCR facility. The software is now being written to work on Apollo-work-station-based systems from Mentor Graphics Corp. (using Common Lisp). When that is done, NCR will deliver systems to customer sites early in 1988. No price has been set.

The Design Advisor's object-oriented

COMING FROM MCC: EVEN MORE POWERFUL EXPERT-SYSTEM SOFTWARE

Look for Proteus to get a sense of time and more powerful reasoning muscle. Proteus is the hybrid expert-system shell developed by Microelectronics and Computer Technology Corp. and used by NCR Corp. as the basis of its new Design Advisor. This year's 3.0 version of the expert-system development tool is expected to move Proteus into temporal reasoning as well as give it the ability to graphically display its reasoning and knowledge in its data base.

"A computer will not understand that it is not worth the time to calculate all of the primes, for example. It knows that is a determinable problem and will attempt it," explains Joseph F. Scullion, deputy director in MCC's artificial-intelligence program and the liaison for co-op member NCR Corp. "We want to add some sense of time into Proteus—how long it will take to get an answer and how time is contiguous. That is a hot topic in artificial intelligence today."

The Austin, Texas, research consortium is also working on a graphic system to display relations between rules and knowledge in Proteus 3.0. Other areas of research include isolating sections of knowledge into miniature expert systems that divide up a large problem, knowledge-acquisition tools, and enhanced explanation capabilities.

A variant of Proteus—dubbed Argo—has not yet gone to program members. Argo works by searching its knowledge base for analogous problems and solutions—much like an experienced engineer. *–J. Robert Lineback*

data base of tightly integrated knowledge frames and inference-driving rules is based on broad experience. It represents about 50 man years of collective chip-design experience from NCR engineers and customers. NCR also conducted an extensive series of taped interviews with other engineers, ranging from VLSI experts to new BSEEs, says Daniel L. Ellsworth, advanced development strategy manager at the Microelectronics Division.

One aim of the data base is to pass on NCR's experiences with semicustom-chip customers. "We think this will be a major competitiveness advantage," adds Ellsworth, referring to NCR's five years in standard-cell chip markets.

KNOWLEDGE WEB. NCR had to adapt the Proteus development system to its Design Advisor. It accomplished this by devising a proprietary web of connected knowledge frames, which are like data templates describing and recognizing common sets of features. The structure was organized by NCR's senior principal engineer on the project, Robin L. Steele, with signals and cells grouped into a lattice of cells so that values and features are inherited from like signals and cells.

The software employs these knowledge frames and integrated rules as it reviews the design with an eye toward offering advice in a half dozen areas: simulation tips; specific functional advice; timing (such as load balancing, setup and hold, and skew problems); testability; fundamental good design; and specification feasibility.

Over the past year, Steele spent much of her time at MCC in Austin, Texas, swapping information with MCC researchers, who then used the input from NCR's application development to improve the Proteus technology. MCC has delivered versions of Proteus to all of its Advanced Computer Architecture program members for use in a wide range of applications.

MCC hopes its transfer of technology to NCR is just the beginning

The result, says Charles Petrie, MCC project leader of the expert-system-technology project, is that "we and NCR both took a gamble on working closely with an application. It was a difficult application and we didn't know if we would be successful. It worked and turned out to be an excellent model for getting technology from MCC's hands to the shareholders."

For NCR, the close work with MCC enabled it to fully use Proteus' features. Says Ellsworth, "The intent of our system is to move the identification of potential problems in the design to as early a stage as possible, before they become embedded into the chips." NCR targeted the use of the belief-revision expert system at fundamental circuit-design rules and knowledge. One alternative would be to embed AI into each computer-aided design tool, such as a silicon compiler. "We are addressing it at methodology level, namely good design practices," Ellsworth says. "It is apparent to us that these good practices have remained relatively constant ever since we have been designing with discrete components."

MCC researchers have developed a way to allow the backtracking and assertion changes—the act of detecting and acting on a contradiction—to be guided by the system's own domain knowledge, explains MCC's Petrie. "The knowledge would state which assumptions should be retracked first, involving the same kind of general reasoning employed in the rest of the expert system," he says. A key achievement of the knowledge-guided mechanism is that it is generically applicable to all possible Proteus-based applications, unlike early dependency-directed backtrack systems.

"We have not yet succeeded to our standards and still have a lot of work to go," says Petrie, referring to long-term Proteus goals. The next step is getting close, however. Proteus 3.0, with enhancements—such as some ability to comprehend the notion of time and graphic display of decisions—is to be delivered this year (see p. 31).

—J. Robert Lineback

RESEARCH

IT'S TIME FOR MCC TO FISH OR CUT BAIT

AUSTIN, TEXAS

For three years now, research has gone on hot and heavy at Microelectronics and Computer Technology Corp., the industry's research consortium, but none of it has made it to market. Now the first of MCC's 20 shareholders, led by NCR Corp. (see p. 31), are starting to use MCC technology in new products, and they're hoping to see profits during the coming year. At the same time, in-house application of MCC research by its members is beginning to accelerate.

"It is a critical period. This is going to be a key year for major deliverables to shareholders," says Joseph A. Boyd, MCC's interim chairman. Boyd, whose full-time job is chairman of Harris Corp., an MCC member, will give up his MCC caretaking role in July. That's when Grant A. Dove, who intends to mold the consortium into a more flexible, market-sensitive, technology think tank, becomes permanent chairman (see p. 12).

To carry out Dove's directive, MCC is restructuring its largest program—Advanced Computer Architecture—to enable its members to focus resources on areas that promise immediate paybacks. These are spinoffs from long-term research targets, transferred in the form of prototypes and interim technology (see table). The new structure also is expected to include a cut in the minimum membership fee by more than half, to $1.2 million.

All this activity comes at a time when the honeymoon is ending between shareholders and the consortium, acknowledges Boyd. The companies supporting MCC are now looking for usable results.

MAJOR PROJECTS. "[MCC] has major deliverables in packaging, artificial intelligence, and computer-aided design," Boyd says. "Software and others are more long-term projects. The next two, three, and four years are going to be critical as to whether MCC not only can develop the technology, but assist in the transfer to shareholders, because the final payoff will be the effective use in developing products that are profitable," he continues. "We are not just in this to do research. Every member is in it to get a competitive advantage in world markets."

So several other members with their own products and services based on AI tools are coming along not far behind NCR and its Design Advisor. One, the new Honeywell Bull Inc. joint venture, is developing an expert system for personal computers that would work out the placement of text and advertising graphics using the same Proteus 2.0 shell from MCC that NCR used.

Honeywell Bull—owned by Honeywell Inc., Groupe Bull of France, and NEC Inc. of Japan—is not itself an MCC member but inherited the AI technology from what was once Honeywell Information Systems. It had been among the most aggressive users of MCC AI technology, putting the first and second versions of the Proteus shell to work in a component-placement system, called Plex, that is being used at its Boston Products Operation in Billerica, Mass., to lay out boards for Honeywell Bull's multiuser computers. Plex cuts the time it takes to place components on boards from one

week to three hours. The operation is also preparing a second Proteus-based tool for its marketing and sales people that suggests computer configurations and pricing tradeoffs for customers.

The target of the marketing system is similar to that of the existing Xsel and Xcon hardware-configuration software at Digital Equipment Corp., an MCC member. DEC wants to extend its expert systems with common-sense reasoning based on technology developed at MCC. DEC, like some other MCC shareholders, prefers to rework the co-op's technology. "Very little of those [interim technology transfers] will actually be used in the form in which we receive it," says Tom Gannon, director of technology-development programs and planning at DEC. "I could point to a number of examples in which we have found it beneficial to take what MCC has developed and explore ways those ideas could be put into products for future customers." DEC, a member of all four MCC programs (packaging, software, computer-aided design, and computer architecture), is planning to utilize tape-automated-bonding technology that has already been transferred from the co-op's packaging lab, but "perhaps not in the form it has been prototyped," adds Gannon.

DEC is also interested in the concepts in common-sense reasoning being developed under the computer architecture program. MCC's Cyc project is an attempt to give computers the ability to use what humans think of as common sense. Pieces of Cyc might end up in a front-end program to the Xsel and Xcon expert systems, helping DEC match specific user applications and office sizes to various computer configurations.

Another computer maker, Control Data Corp., is using Proteus in an in-house system for diagnostics of mainframes and assembled computer boards, says Robert M. White, vice president and chief technical officer. Control Data and Honeywell also have agreed to use MCC's computer-aided design tools in creating a new CMOS cache memory. They will start after the co-op's CAD program transfers a complete working system totaling 1 million lines of software code. "The chip will be done as a test [of the tools]," says White. Control Data is also seeking military certification of TAB technology.

Boeing Electronics Co. of Seattle became the first to announce use of MCC packaging technology last March. Now, Advanced Micro Devices Inc. is preparing to use some before the end of the year. "The results of the packaging program are substantial. We plan to utilize that technology rather extensively," says George M. Scalise, senior vice president and an MCC board member. Harris is gearing up to use packaging technology, too, according to Boyd, who says a prototyped system is based on the TAB process. *–J. Robert Lineback*

KEY INTERIM TECHNOLOGY FROM MCC

Program	Year	Technology
CAD	1985	C module editor: C language IC-layout system
		IKE: initial kernel environment for a CAD platform
	1986	Music: prototype of a batch Lisp circuit-simulation system
		Foreign-module interface: converts standard circuit-design inputs for MCC tools
		Electronic Lisp: editing tool for documenting Lisp code
		Greedy router: new routing algorithm
	fall 1987	Major release of a complete CAD system
Packaging	1986	First release of TAB process: complete set of process steps and equipment for high-lead TAB
		Test-tape handler: presents chips bonded on tape to test station
	1987	Treehouse: high-performance air cooling system
	summer 1987	Gold bump process with vertical sidewalls (100-to-50-mil centers)
	fall 1987	Second-generation TAB
Software	1986	Raddle: language for distributed software development
		Biggertalk: extended-Prolog language for object-oriented programming
	1987	Plane-Text/FIG: tool for easy linking of display windows and data-base object
		Verdi: graphic environment for designing distributed systems
	late 1987	Gibis: graphic system for tracking issues in team software design
Advanced Computer Architecture	1985	Proteus 1.0: initial expert-system demo
	1986	CSIM: simulator for multiprocessor systems
		PPL: parallel programming language
		Proteus 2.0: expert-system shell with enhanced features
		Linguist workbench: natural-language parsers and tools
		Semnet: graphical package for showing word interrelationships
		Visage: tools for building graphical interfaces
		Lucy: natural-language parser for English
	1987	Orion: object-oriented data-base system
		Proteus 3.0: expert system with a sense of time and displayable reasoning path

SUPERCONDUCTIVITY

SUPERCONDUCTOR RACE ATTRACTS MCC

AUSTIN, TEXAS

Somewhat serendipitously, Microelectronics and Computer Technology Corp. is pursuing a new research program into superconductive materials. The initiative was proposed by the Austin, Texas, research consortium's packaging researchers, many of whom had left the superconductor field a few years earlier when the prospects of the technology ever being used were dim. Now that superconductivity is hot, MCC hopes to have a major program under way in the fall. MCC's decision topped off a frenetic fortnight in early June for the rapidly expanding superconducting community. While representatives from 15 MCC member companies took part in a two-day seminar to help define and plan a superconductor project, there were other developments on the political and research fronts, among them:

- Congress was briefed by scientists from several U.S. and Japanese labs.
- White House Science Adviser William Graham said he will convene a national

conference on superconductivity July 28 and 29 in Washington.

■ Bell Communications Research claimed to have found a new and better way to produce superconductive thin films.

Superconductivity, a promising technology that over the past decade had not made much progress toward practical applications, has become in the past six months just about the hottest technology around. A rapid series of breakthroughs catapulted it into the headlines over the winter and into the spring as scientists disclosed a new class of ceramic materials that become superconductive at temperatures as high as 100 K or more, instead of below 23 K [*Electronics*, April 2, 1987, p. 49].

The emphasis will be on applications and production

Laboratories around the world are following this progress, and many have set up at least small research efforts. At this point, MCC perceives an opportunity to help provide for even its smaller members a level of research usually available only to the biggest companies. What the consortium aims to do is find new applications for superconductors and study techniques for producing the new materials.

MCC officials admit that superconductor research is now ideally suited to the consortium, since few electronics companies are likely to fund such research on their own. Indeed, they are hoping that the project will attract new members. MCC vice president Barry Whalen says the consortium will present a finished proposal in July to a group of nonmember U. S. companies that might be interested in joining the program and MCC. Outsiders note that the superconductor program came at a good time for the consortium, which had been losing members during the semiconductor industry recession.

"There is a great deal of uncertainty as to the best way to apply these materials in our areas of interest," says Whalen. "MCC will focus its efforts on the areas of fabrication and application."

MCC wants to develop analytical modeling and simulation techniques to help identify applications, says Whalen. At first, he adds, the program will have modest funding.

The government is also getting involved. The House Science, Space, and Technology Committee heard testimony from researchers at IBM Corp., the University of Houston, and the Defense Advanced Research Projects Agency as part of its effort to keep abreast of the developments. A spokesman for the committee says the information will be incorporated into a general study of technology policy that will compare the way advances in such technologies as steel and semiconductors are incorporated in the U. S. and Japan.

Meanwhile, in the research area, Bell Communications Research announced earlier in June that it had developed an approach to making superconductive thin films of an yttrium-barium-copper-oxide compound that lends itself to mass production.

IBM researchers have used two techniques to produce thin films, one using a "spray" coating system and the other using an electron-beam evaporation process. But Venky Venkatesan, manager of the materials processing science group at Bellcore's Navesink, N. J., laboratories, says he's come up with a method that provides more consistent results. IBM's electron-beam system requires separate "targets" for each element. But Venkatesan discovered that a more uniform film could be obtained by using instead a single, premixed target as well as an ion-beam sputter-coating process.

In the process, a pulsed eximer laser puts down about 2 Å to 3 Å per pulse, Venkatesan says. "The beauty of the technique is that each laser pulse produces a fixed amount of coating," he explains. "In eight minutes, 5,000 shots with the laser will give you a 2- or 3-μm film." Bellcore, the research arm of the seven regional Bell operating companies, is hoping to use superconductors in conjunction with optical transmission devices, he says. *—J. Robert Lineback and Tobias Naegele*

COMPANIES

A DOWNSIZED INMOS IS ON ITS WAY BACK

NEW YORK

Frequent flyers who pile up thousands of air miles can win free flights to almost anywhere in the world. But none can match the prize—a trip back to profitability—that Inmos International plc won for itself in part through the transatlantic shuttling of Iann Barron, one of the founders of the company and its chief strategic officer.

Sales rate tops $100 million, up 50% from 1986

In January, Barron began bouncing back and forth about once a month between Bristol, the firm's UK headquarters, and its Inmos Corp. subsidiary in Colorado Springs. At the time, the company was 18 months into a downsizing mandated by its parent company, Thorn-EMI plc, which has poured $345 million into Inmos. Barron was sent to tighten up the U. S. operation and strengthen its sales staff. Some 75% of the firm's revenues come from the U. S.

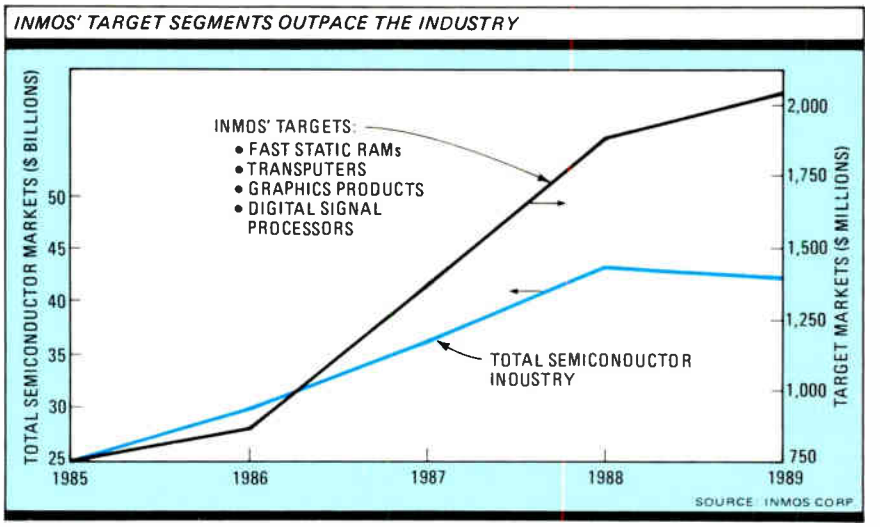
"We cut back to 1,500 people [from some 2,000 worldwide] in 1985, and then to 1,100 in 1986," Barron says. Along with the cuts in manpower, Inmos pulled its memory production lines back to Britain and converted its Colorado Springs facility to a product-development operation and pilot line.

Now the downsizing has ended and Inmos is in an uptick. "By midyear, we'll be back to 1,350 people," Barron says. By then, Inmos should have a couple of money-making months under its belt, after losing as much as $4 million to $5 million a month in the spring of 1986. "We got our head above water in March," says George Popovich, vice president for U. S. marketing and sales, "and we have some aggressive growth plans for the upcoming year."

Barron reports that sales are now running at a rate of $100 million to $120 million a year. That compares with "slightly over $70 million for 1986." Along with the rise will come a significant shift in the product mix. "Sales will be split 50% for fast SRAMs and 50% for transputers and other products. The run rate for transputers went up by a factor of two during the past year," he says.

Along with the fast SRAMs and the transputers, Inmos has targeted the markets for graphics products and digital signal processors. By the end of the decade, these four segments will grow to $2.1 billion, Inmos estimates, nearly triple the 1985 figure. They'll far outpace the growth for the total semiconductor market, forecast to rise some 75%—from $25 billion to $43 billion—during the same period (see figure).

SRAMs rank high in the company's plans. It figures their market will zoom from $150 million in 1986 to $900 million by 1990. "The 68030 and 386 [Motorola and Intel 32-bit microprocessors, respectively] are creating brand-new markets for SRAMs," Barron believes. The company's strategy is to target high-performance applications and get into market niches early, before the large merchant suppliers like Fujitsu, Mitsubishi, and



NEC in Japan and Motorola in the U.S. can move in. Inmos now is offering samples of a 35-ns 256-Kbit SRAM—so far the fastest part of its kind on the U.S. market, Barron claims—and will follow up with a 25-ns part later this year. Crucial to the performance are current sensing and a double-level metal 1.2-μm CMOS technology that Inmos calls Process '86 [*Electronics*, April 16, 1987, p. 34].

As for graphics products, Inmos has scored heavily with its color look-up table, which offers a choice of 256 colors from a palette of 256,000 hues. IBM Corp. is using the chip for its new Personal System/2. That translated into a solid boost for sales. They spurted 42%—from $19 million for the first quarter of the fiscal year that ended March 1987 to $27 million for the fourth quarter—and about one third of the increase stemmed from the color look-up table, Popovich says. The firm's cascadable DSPs debuted only last November.

Barron, a prime mover in the development of the transputer, has great expectations for the device. "Colorado Springs was aimed mostly at memories and the transputer was in the back seat. Now we're pushing harder on transputers," Barron says. Worldwide, some 2,000 companies are evaluating the transputer—a 32-bit microprocessor built with reduced-instruction-set architecture, on-board memory, and four communications links that can be used as a straightforward microprocessor or a parallel-processing element.

One of the most promising transputer markets is turbo-charger boards for personal computers, where the installed base is in the millions. The two leading suppliers of such boards are set to launch add-in boards, one for 68020 machines and one for 80287s.

Barron maintains these boards are just a beginning. "We've designed a 'VAX crusher' card that can have one or two T800s [running at 15 million operations per second] and 16 megabytes of DRAM to make a personal computer twice as powerful as a [Digital Equipment Corp.] VAX8600," he explains.

Barron says that the Occam language developed for the transputer won't be an obstacle for board designers. "It's not absolutely necessary. The trouble is that we are late with compilers for C and Fortran. But we have them now at several beta sites." *—Arthur Erikson, with bureau reports*

TELEPHONY

A NEW CHIP SIMPLIFIES PHONE-LINE TESTS

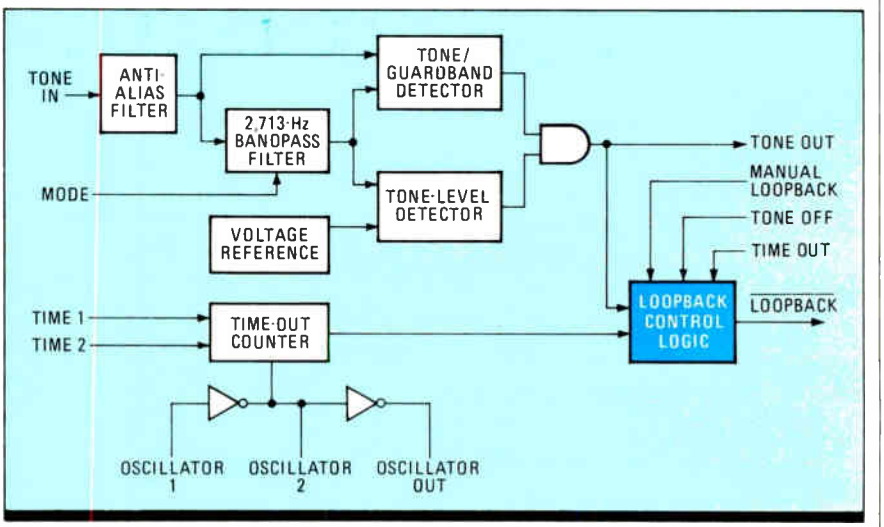
TUSTIN, CALIF.

It's not easy to find an unoccupied semiconductor niche, but Silicon Systems Inc. appears to have zeroed in on a good one with a standard chip intended to vastly simplify the task of remotely testing telephone-company lines. Placed in a maintenance unit where the company's lines join the customer's, the so-called loopback integrated circuit enables central-office personnel to remotely test transmission lines.

The CMOS chip, designated the SSI 78M400, houses all the detector and control circuitry needed to accept a 2,713-Hz command tone that activates a relay bridging the transmit and receive lines. That accomplished, the phone company can send out test-pattern signals that are looped back to be checked for errors against line-characterization data. The chip is for four-wire lines, used by customers who need reliable transmission of computer data via high-speed modems, which command premium phone rates compared with two-wire lines.

Silicon Systems expects the savings promised by its new chip to attract both phone companies and the people who supply them with test and maintenance equipment. "Much easier line maintenance tops the benefit list," says Carmelo J. Santoro, chief executive of the Tustin company. "Sending a service guy out with alligator clips to jump the lines, then call back to the office, then wait around—that's really expensive."

The chip's introduction comes at a good time, says Santoro. In the past year, as part of divestiture, customers became responsible for the lines on their premises. Santoro expects that the 78M400 might eventually be upgraded as a "meter box" at the customer's site—a sort of brain center controlling such operations as security and alarm



AROUND AND BACK. Silicon Systems' loopback chip takes a 2,713-Hz command tone through frequency, amplitude, and duration checks; it also compares minimum-level parameters.

IF YOU'RE DESIGN
YOU'RE WAST

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equipment. The loopback chip is a key to remote control, he notes.

Silicon Systems has been working on the loopback IC since early 1986. While Santoro acknowledges that there is "nothing magic about connecting lines and looping them back," integrating analog and digital logic with the required precision of tone signaling and detection posed some thorny design problems.

To be valid, for example, the 2,713-Hz command tone must be checked by circuitry that detects frequency, amplitude, and duration and compares minimum-level parameters to extraneous energy within a monitored guardband. All these conditions must be met before loopback switching takes place. The tone must be between 2,706 and 2,720 Hz in a range of 0 dBm to -32 dBm and must last for 1.6 s. Loopback bridging may be terminated by a second qualified command tone or by a timer. Power requirement is ±5 V at less than 50 mW dissipation. The chip is available in sample quantities at $11 for 100 pieces.

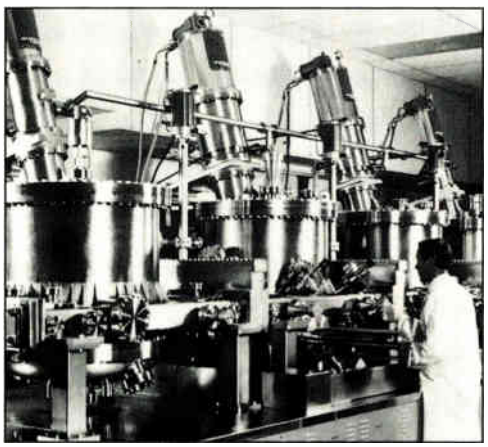
Silicon Systems believes it has a year's head start in the loopback IC market. So far there is no sign of similar chips, even from such telecommunications heavyweights as Motorola Inc. and Rockwell International Corp. The payoff will come when Bell System companies get interested, says Santoro. If that happens, "this is a million-unit-a-year market for us." *–Larry Waller*

SEMICONDUCTOR PROCESSING

HOW SILICON IS GOING TO COPY GaAs

EDEN PRAIRIE, MINN.

Advanced semiconductor devices based on epitaxially grown superlattices, quantum wells, and other exotic structures have so far been largely the stuff of gallium arsenide. But as silicon devices move toward the limits of conventional bulk structures, the same kind of epitaxial device work may soon be done in silicon.



EXOTIC. Bell Labs is using molecular-beam-epitaxy systems to research exotic silicon structures.

One major indicator comes from Perkin-Elmer Corp.'s Physical Electronics Division. In November, the Eden Prairie, Minn., manufacturer of molecular-beam-epitaxy systems plans to become the first U.S. supplier of molecular-beam-epitaxy equipment designed for silicon research. The division is building five prototype modules for delivery between November and mid-1988. The technology will be a standard option for its modular 430 MBE series.

The Perkin-Elmer entry comes at an opportune time. Silicon molecular-beam-epitaxy research is under way at a number of universities and at firms including AT&T Bell Laboratories, AEG-Telefunken, IBM, and Texas Instruments. The researchers are looking for a way to circumvent the 0.8-μm barrier expected to stop the advance of conventional silicon devices [*Electronics*, April 28, 1986, p. 37].

That interest also extends to the Defense Department. Perkin-Elmer's first module will go to California Institute of Technology as part of an extensive 430 system that includes separate modules for III-V, II-VI, and metals epitaxy, plus electron spectroscopy for chemical analysis, all linked by transfer tubes to pass wafers among modules within the system's ultrahigh-vacuum environment. The system was funded to the tune of $1.6 million by the Defense Advanced Research Projects Agency and the Office of Naval Research.

Unlike systems used for III-V compounds such as GaAs, silicon molecular-beam epitaxy requires electron-beam evaporators. Compared with resistance heaters used for flux generation at 600°C to 1,100°C in the III-Vs, the e-beam guns can hit the 1,800°C to 2,000°C needed to provide an adequate flux with silicon, a low vapor-pressure material, says Peter Chow, Perkin-Elmer staff scientist.

Perkin-Elmer isn't the only one to spot the opportunity. The Riber Division of Instruments SA in Rueil-Malmason, France, entered the silicon molecular-beam-epitaxy market two years ago, while VG Semicon Ltd. of Sussex, UK, has supplied equipment for use with silicon for several years.

In fact, next month VG Semicon will deliver to Bell Labs a silicon MBE system believed to be the first one to accommodate multiple wafers. Based on a patented AT&T design, the system can handle up to fifteen 3-in. wafers or seven 5-in. wafers.

Like others, John C. Bean, head of the Materials Science Research Department at Bell Labs in Murray Hill, N.J., sees an emerging research market for silicon systems. "I think the GaAs guys have finally scared the silicon guys. But we're gonna play a little of the compound-semiconductor game too, and see if we can find ourselves some niches," Bean says. *–Wesley R. Iversen*

COMPUTERS

IBM'S NEW BAG OF TRICKS TO CATCH UP IN NETWORKS

NEW YORK

IBM Corp. continues to go all out to try and catch up with customer demands for connectivity and networking among its diverse systems, from personal computers through midrange systems to the big mainframes. On June 16 the giant disgorged another hefty package of products in a further step toward total integration of its own and other vendors' equipment. This follows by 12 months an unprecedented blitz of some 125 new connectivity and midrange-system products [*Electronics*, June 23, 1986, p. 50], and there have been other product announcements in the interim.

Within last week's bundle of more than 40 telecommunications products, hardware was present but software dominated. The announcements covered the communications gamut from extensions of IBM's Systems Network Architecture to new work stations to T1 products, and included richer and easier-to-use network-management software. The main thrust of the package, says IBM, is to make it easier to install, run, and manage complex computer networks.

But nothing can change the fact that IBM is still basing its communications strategy on the 12-year-old SNA. The company has been building and enhancing SNA over the years to encompass more system-connectivity features as customers demand them. So it now includes features for hierarchical net-

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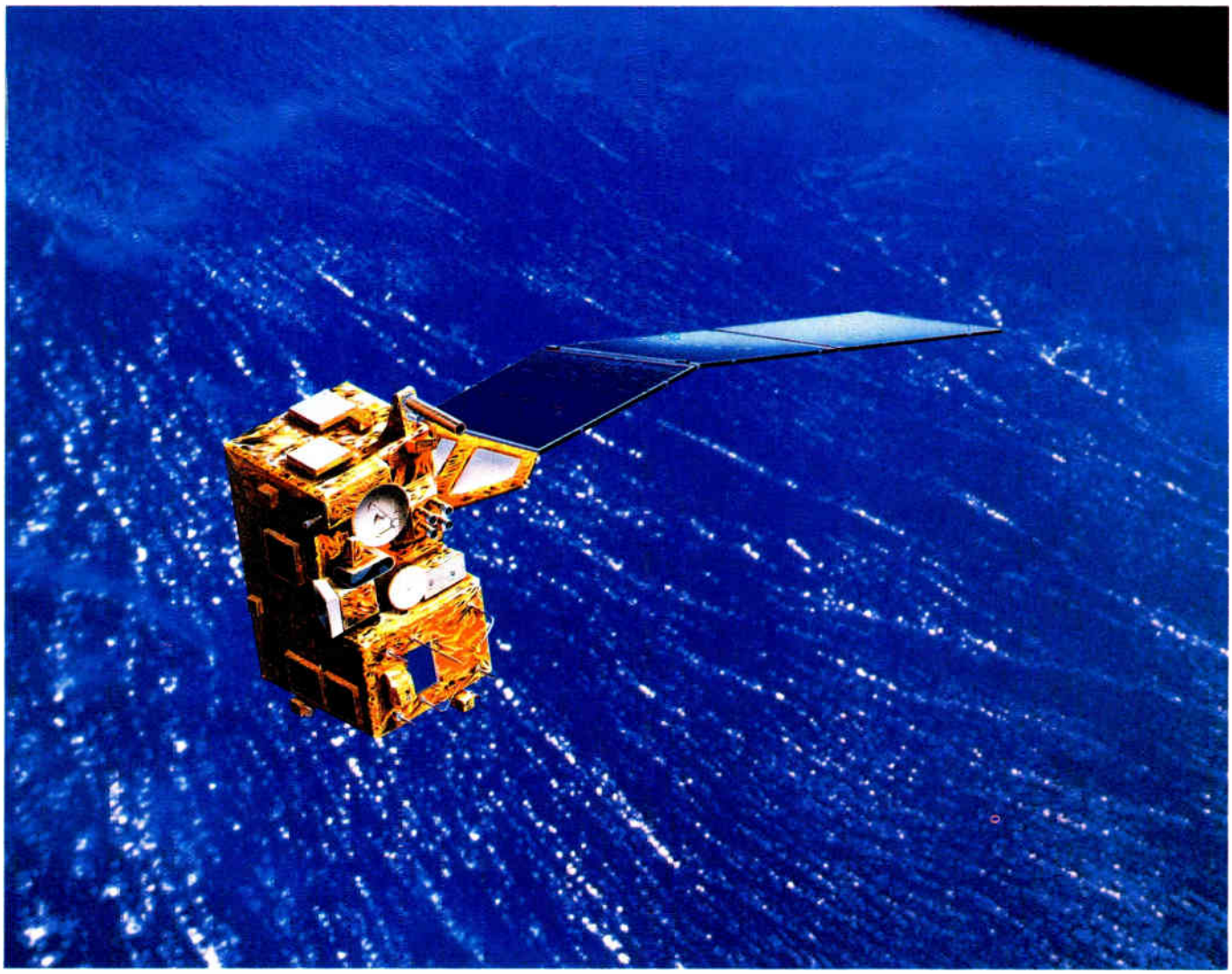

JAPAN LAUNCHES INTO A NEW ERA IN REMOTE SENSING.

Japan's first Marine Observation Satellite-1 (MOS-1) is now circling around the globe, covering its entire surface in 17 days from 909km up in space.

With three sensors aboard, the new remote sensing satellite beams back an enormous volume of data on diverse aspects of the sea, land and atmosphere. One of the sensors, MESSR (Multispectral Electronic Self-Scanning Radiometer) senses colors of the sea and land, and recognizes surface features 50m by 50m, utilizing CCD (Charge-Coupled Device) image sensing devices. The MOS-1 is expected to contribute greatly to fishery, agriculture, forestry, resources finding and environment preservation worldwide.

As the prime contractor to the National Space Development Agency of Japan (NASDA), NEC was engaged in system design, system integration and manufacture of key subsystems including major bus subsystems, the MESSR sensor, the DCS (Data Collection System) repeater, ground receiving system and image data processing system.

With more than 30 years of experience in space development, NEC has been involved, as a prime contractor or system integrator, in 23 of the 37 satellites placed in space by Japan.

NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 140M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action. As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.

The SP-3A uses 3 new CCD chips that are anti-smear and -blooming—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μPB6312 with 1,200 gates (400 Full-adders) and the μPB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

NEC

works, peer-to-peer communications, and connections to non-SNA networks. Future voice network integration will also be based upon SNA, says Larry J. Ford, an IBM vice president and assistant group executive.

The areas addressed in the latest announcement range from data communications, transmission-line bandwidth-resource management, voice communications, and network management, to information transformations such as signal and protocol conversions. With such variety, it is difficult to pinpoint any highlights among the multitude of introductions: each addresses a need in a particular area. But taken together they do point unwaveringly toward that major goal of IBM's communications strategy—to make it easier for customers to connect a variety of computer systems and voice telecommunications products.

Software dominates 40 new SNA integration products

However, among the more important data-communications announcements were new versions of the Advanced Communications Function/Virtual Telecommunications Access Method program that supports peer-to-peer communications among System 370 hosts (9370, 43XX, and 3090 systems). They work without host-application assistance and over dial-up and multipoint leased lines as well as on dedicated leased lines. Features have been added to enable customers to make network changes much faster and to be able to add new systems to a network without taking the network down.

IBM's program-to-program communications protocol, LU 6.2, has been extended to provide support to all System/370 operating systems. Now programs running on all 370 systems can communicate directly with programs running on other 370s, System/36, Series/1, System/88, RT PC, IBM Personal Computers, or another manufacturer's processor that supports LU 6.2.

SIGNED UP. To enhance transmission-line bandwidth-resource management for its customers, IBM has signed a marketing and development agreement with Network Equipment Technologies Corp. The Redwood City, Calif., firm makes a family of T1 transmission resource-management hardware products, called the Integrated Digital Network Exchange, that IBM will now sell and support. These products allow dynamic sharing and routing of a network of digital T1 lines among a number of computer systems and private-branch exchanges to construct complex, reliable, yet efficient, digital voice-and-data networks.

Also making its debut was an IBM-developed remote channel-to-channel communications box, the 3737, that allows System/370s to communicate with each other over public or private T1 lines. The 3737 can be used in conjunction with the resource managers made by Network Equipment Technologies.

–Tom Manuel

WORK STATIONS

DEC BOMBSHELL: A $7,900 COLOR WORK STATION

MAYNARD, MASS.

The ripples are still spreading after Digital Equipment Corp. splashed into the work-station pool with a series of announcements that are shaking up the pricing structure of that market, if not issuing an outright challenge to the leadership of Apollo Computer Inc. and Sun Microsystems Inc. The principal market entry from DEC is a 32-bit, $7,900 color VAXstation 2000 that the Maynard, Mass., computer giant claims is the first color work station priced at less than $8,000.

Besides the color machine, DEC also introduced other new products at the Design Automation Conference in late June in Miami (see "Software stars at the Design Automation Conference," p. 57). These include a monochrome desktop VAX work station that sells for $4,600; a VAX server system designed for work-group applications; high-capacity (159-Mbyte) Winchester mass storage for the VAXstation 2000 family; and expanded VAXcluster networking software. At the same time, DEC is cutting prices on existing models in the VAXstation 2000 line and on other work stations.

Christopher Reed, marketing manager for DEC's Worksystems Group, says the big package of announcements is the latest in a series of DEC developments dating back to last November, all aimed at establishing the company as a leader in work-group computing. Included in the earlier moves were the original Local Area VAXcluster networking software, which linked 14 nodes; the latest announcement extends that to 28 nodes.

Reed says further that the recent steps encompass "very aggressive pricing" that will make DEC more competitive in work-group computing with Ap-

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ple Computer Inc. and IBM Corp. In fact, one industry analyst sees the DEC announcements as making the company more competitive in the Apple and IBM personal-computer arena than in technical work stations. Mark Stahlman, research analyst with Sanford C. Bernstein & Co. in New York, expects the products to be "very successful in the VMS market, especially with current DEC VMS customers."

Stahlman doesn't believe the moves will push Apollo and Sun out of their work-station leadership spots, though. He maintains that DEC lacks some of the key ingredients to excel at that game, including breadth of product line and a dedicated sales force. But DEC's Sandy Friedman, strategic marketing manager in the

DEC's aggressive pricing puts the pressure on Apollo and Sun

Worksystems Group, counters that the latest announcement encompasses seven new configurations. Further, he points out that another 15 VAXstation II and VAXstation II/GPX configurations are included in the product family for which price cuts were announced.

More important, DEC executives stress that their work stations serve as desktop user interfaces to an unrivaled breadth of products scaling all the way up to the VAX 8000-series departmental mainframes. As for a dedicated sales force, Friedman maintains that work stations are the "distributed shared systems of the future, and our sales force is adept at selling whatever is appropriate for a user's desk."

In an entry-level configuration, Reed says the color VAXstation 2000 would include the MicroVAX processor, 4 Mbytes of random-access memory, 70 Mbytes of hard-disk storage, the operating system, and networking software—all for about $10,700. A comparable Apollo DN3000 system sells for $21,400.

APOLLO IS READY. Edward Zander, vice president of marketing at Apollo in Chelmsford, Mass., says his company isn't surprised by the DEC announcements, and hints that Apollo soon will drop another work-station shoe. "We haven't seen the VAXstation family as a strong competitor," he says. "The product has been relatively weak on price/performance. It looks like they've tried to correct the price part of that. They've put a little more pricing pressure on us and on Sun, but we still have a price/performance advantage in our current products, and especially in what we have coming in the near future. We'll respond with advanced technology, not just with price cuts." *–Larry Curran*

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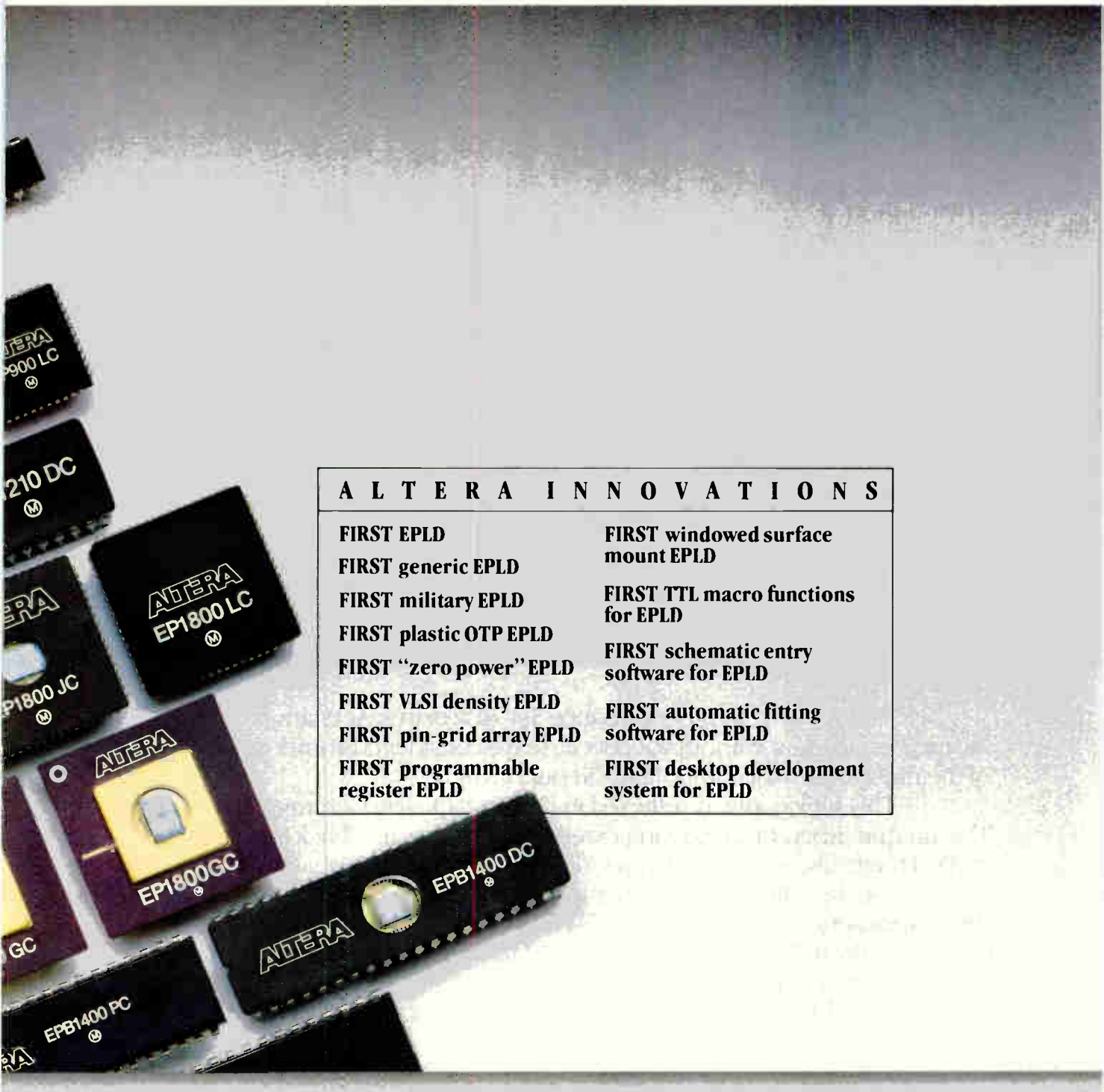

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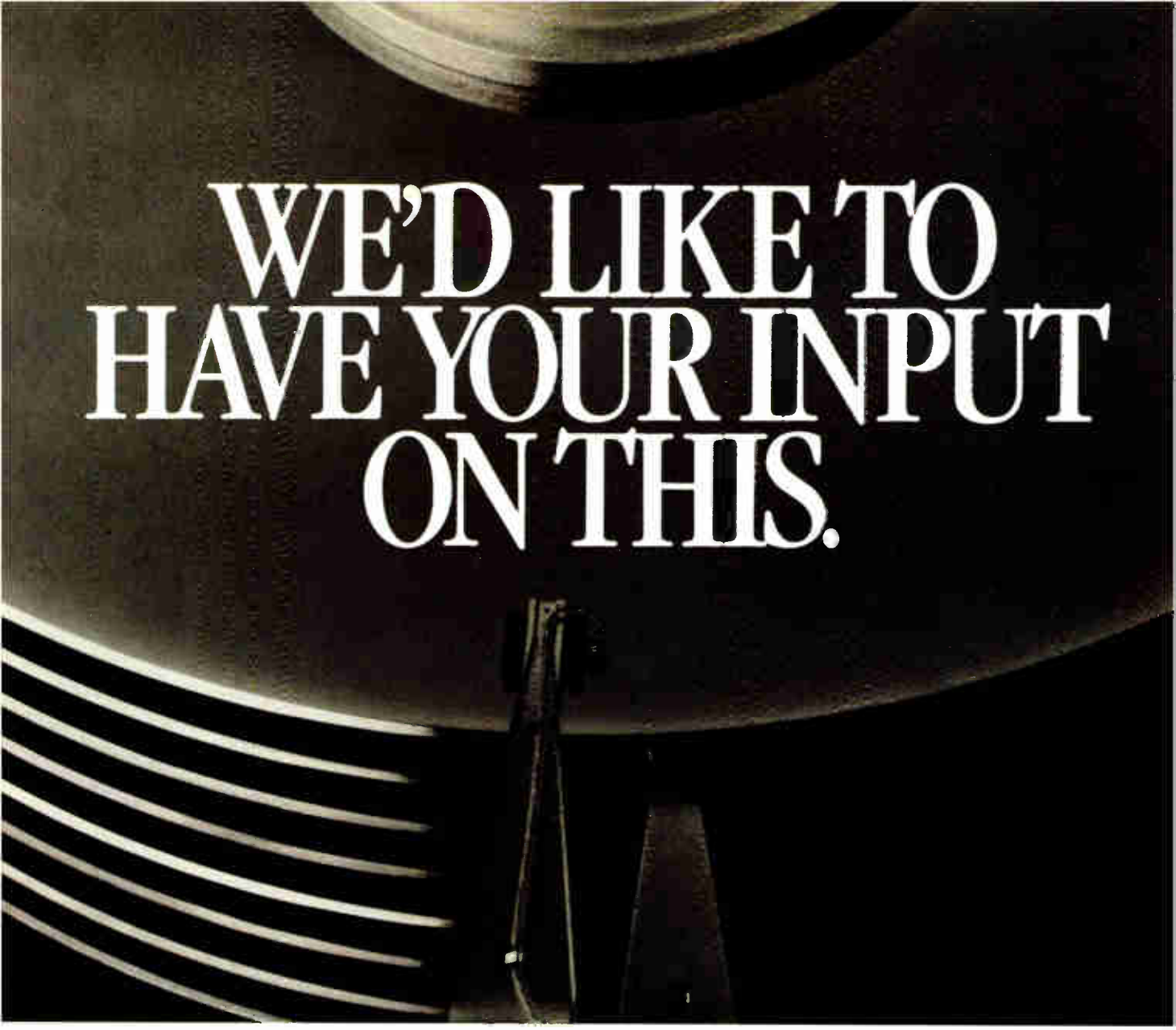

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INTERNATIONAL NEWSLETTER

PHILIPS STARTS SELLING ADVANCED CMOS LOGIC WITH NEW PIN LAYOUT

Philips of the Netherlands has started supplying customers with samples of its first advanced CMOS logic devices. The new generation of high-performance chips touched off an industry-wide controversy last year when Philips and its codeveloper, Texas Instruments Inc. of Dallas, announced that they were relocating the power and ground pins from their traditional location at the corner of the package to a new spot in the center. The companies said the switch would reduce the effects of transient voltages, which cause data errors to occur, but competitors Fairchild Semiconductor Corp. and the GE/RCA Solid State Division continue to dispute their claims [*Electronics*, May 14, 1987, p. 33]. The first 10 Philips ACL devices to feature the new pinning are various NOR and NAND gates, as well as flip-flops—all with CMOS or TTL input-level operation. □

JVC WILL BE FIRST TO MARKET S-VHS CAMCORDERS

The Victor Co. of Japan will be the first to formally introduce S-VHS camcorders to the consumer market. The company will begin selling two models in Japan this summer and hopes to market them in the U. S. by fall. S-VHS is an improved version of the VHS video format, featuring resolution of more than 400 lines [*Electronics*, April 30, 1987, p. 49]. Both machines will also be able to record and play back using the standard VHS format. The GR-55S, a 1.1-kg model that uses a compact cassette and can record up to one hour on a tape, will cost about $1,700 in Japan. The unit has an improved ½-in. charge-couple-device image sensor that delivers 330,000 effective picture elements. JVC will also offer an advanced model, the GF-S1000H, which will weigh 2.7 kg and will use a full-size VHS cassette. The $2,400 machine, which will play and record for up to 6 hrs., uses a $^2/_3$-in. image sensor with 360,000 pixels for even better resolution. Sharp Corp. is also expected to release an S-VHS camcorder this summer. □

NHK LABS BUILDS A 20-in. PLASMA COLOR DISPLAY FOR HIGH DEFINITION

A color plasma display measuring $11^1/_3$ in. by 16¼ in. has been fabricated by NHK Science and Technical Research Laboratories, the research facility of Japan's public TV station, NHK. Capable of operating as a 20-in. TV monitor that meets National Television Standards Committee requirements, the panel is actually a partial model for the high-definition TV format that NHK is pushing the world to adopt. The prototype display has more than 286 picture cells, arranged 448 vertically by 640 horizontally, with a cell pitch in both directions of 0.65 mm. The panel, which is just 6 mm thick and weighs 5.3 lb, uses a pulse memory-drive scheme to turn individual cells on and off. The pulses excite a helium-xenon gas mixture, which in turn becomes ultraviolet and turns on the color phosphors in each cell. □

HITACHI TAKES SHARPER AIM AT EUROPEAN SOFTWARE MARKET

Seeking to bring its development team closer to the markets it serves, Hitachi Ltd. is establishing a software laboratory in London to develop software products for the European market. Under Hitachi Europe, a wholly owned subsidiary, the labs will focus on software for Hitachi's work stations as well as pursue artificial-intelligence applications. Its first task will be to develop software for Hitachi's Unix-based 16-bit 2050 work station, announced in Japan in September 1985 and slated for a European launch in 1988. Hitachi also plans to develop mainframe software in London that will be sold under its own label. The Tokyo company's mainframe software is currently sold in Europe under other firms' private labels. □

INTERNATIONAL NEWSLETTER

UK's ACORN FIGHTS BACK WITH A NEW 32-BIT RISC COMPUTER

Acorn Computers Ltd. of Cambridge, UK, is back in action. Once the top name in British computing, Acorn got into trouble when financial woes almost shut it down in 1985, but Olivetti bailed it out by buying a 79% stake in the company. Now Acorn is launching a comeback, with its first computer product in 18 months. The company claims the new system, Archimedes, is the fastest microcomputer in the world. The system can perform 4 million instructions per second, making it one of the fastest machines in its class. The system, built around four custom-made chips, has at its heart a 32-bit central processing unit that uses a reduced-instruction-set computer architecture [*Electronics*, Aug. 26, 1985, p. 48]. A memory manager, a video controller, and an input/output controller round out the quartet. Production will begin in the fall for Archimedes, which will be priced from $1,300 for a basic model up to about $2,300 for a business version. □

WEST GERMAN TV MAKER SWITCHES TO AN ALL-DIGITAL LINEUP

Loewe Opta GmbH, a West German manufacturer of high-end TV sets, is the first TV maker to use digital-signal-processing circuits across the board in all its tabletop color models. The company says that digital technology improves the quality of the sets without adding to the price. Using DSP chips from Intermetall GmbH for both audio and video [*Electronics*, April 5, 1984, p. 89], Loewe's new generation of sets will go to market in time for the International Audio and Video Fair beginning Aug. 28 in West Berlin. The Kronach company says digital processing can automatically compensate for component drift, ensuring that sound and picture quality remain at peak levels. Loewe also claims that digital technology will make it easier to integrate new video services, such as videotext and Europe's upcoming direct-broadcast-satellite communications services, because no large interfaces are needed. □

FERRANTI CARRIES ON A JUNE SHOPPING SPREE

Like a shopper scrambling at a Harrod's sale, Ferranti plc spent most of June making a series of substantial purchases. The Cheadle, UK, firm acquired two U. S. companies and two British operations; it didn't reveal the financial terms. Ferranti began with the acquisition of the advanced laser-technology project group from General Electric Co., of Fairfield, Conn., and then bought Allegheny International Inc.'s majority share in Sciaky Bros. Inc., a Chicago maker of high-end welding systems based on resistance, fusion-arc, electron-beam, and laser technologies. At the same time, Ferranti was active on the home front, adding Datestore Ltd. of Watford and the military trainer and air-launcher business of Wardle Storeys plc in Godalming. Datestore makes frequency-agile and point-to-point broadband modems. □

NEW LAW WILL PROTECT WEST GERMAN CHIP MAKERS FROM PIRATES

In a move that is expected to start a pan-European trend, West Germany has passed a bill aimed at protecting the "topologies of microelectronic semiconductor products." Other member countries of the European Community are expected to follow suit with similar legislation before the year is out. Akin to the 1984 U. S. Semiconductor Chip Protection Act, the new bill will protect West Germany's semiconductor industry from unlawful copying of its products. It will become law in November. Under current law, semiconductors and their architectures are not protected in West Germany. As a result, pirates have taken advantage by illegally counterfeiting circuits, costing the industry "losses in the millions," according to Bonn's Ministry of Justice. Now offenders will face the possibility of heavy fines and even prison terms. □

SIEMENS

Why don't these new measurement instruments have any control elements?

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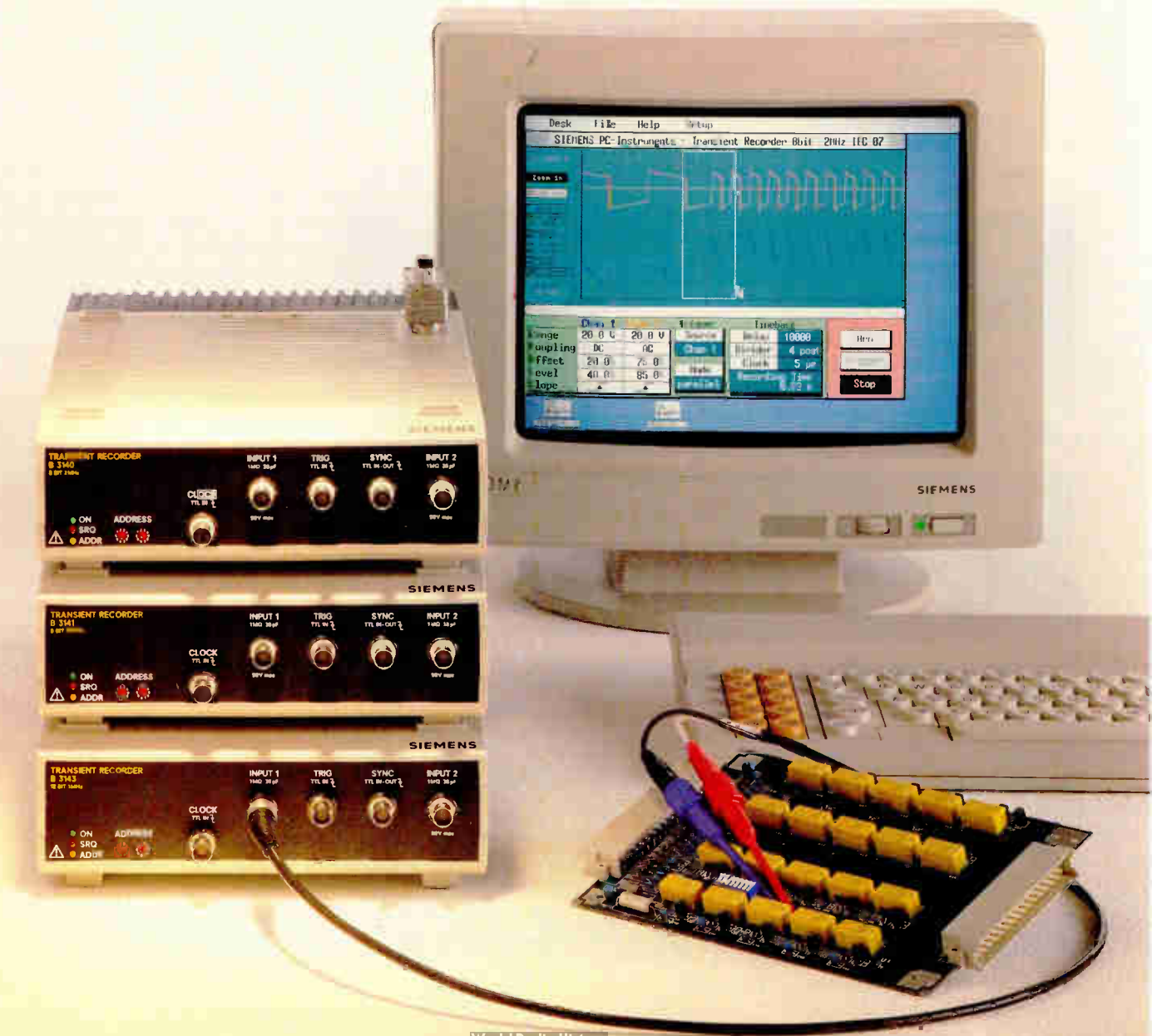

Now, you can skip unweldy operating procedures when using measurement instruments. Why? Because Siemens has developed new measurement instruments that cooperate with personal computers over an IEEE 488 bus. And that eliminates, for example, your reliance on cumbersome keys and dials when using transient recorders. Adjusting parameters, ranges, and functions is easier than ever... with the PC keyboard and mouse.

What's more, our standard software accepts only instrument-specific and logically-structured entry data. So that you get top quality results every time. And since each instrument includes pre-programmed operating instructions, there's no more flipping through time-consuming manuals to get to the point. Whenever you're uncertain about how to proceed, the instrument itself provides the plaintext answer. A click of the mouse is enough... for calling up instructions or executing commands that put you firmly in control of up to 15 measurement instruments. From function/pulse generator to digital multimeter.

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Measurement's never been easier. With PC instruments from Siemens.

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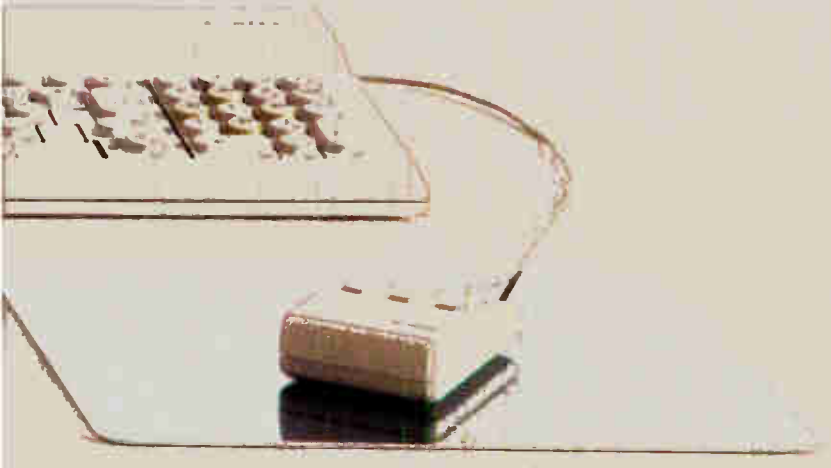

Want to know more about our PC instruments? Just contact your local Siemens office or drop a line to:

Siemens AG
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Federal Republic of Germany

A19100-E686-Z4-V1-7600

Circle 128 on reader service card

INTERNATIONAL WEEK

FUJITSU SHIFTING SOME R&D TO SPAIN

Fujitsu Ltd. will take its first step in a program to shift some of its research and development to Spain. The Tokyo company will begin by developing a Japanese-Spanish translation system using its superminicomputers. The R&D work will be done in conjunction with a joint venture in Madrid, Sociedad Española de Comunicacionese Informatica SA, which already does manufacturing for Fijitsu. Established in April 1986 as one of Fujitsu's bases in Europe, the joint venture is 60% owned by Fujitsu and 40% by Companiea Telefonica Nacional de España, a government-financed telecommunications firm. Fujitsu is already working in Japan on a translation system for English, German, French, and Korean.

USSR AND HUNGARY SET JOINT VENTURE

Hungary and the Soviet Union have established their first joint venture in medical electronics, according to Hungarian sources in West Germany. The venture, called Micromed Co. and based in the northern Hungarian town of Esztergom, will initially turn out seven types of new microprocessor-controlled medical systems, including electrocardiographs and patient monitoring equipment. Micromed will later add more systems to its lineup. The systems will eventually be sold in other countries.

KDD's SYNTHESIZER GIVES VOICE TO PCs

Kokusai Denshin Deniwa Co., Japan's international telecommunications monopoly, has developed a speech synthesizer attachment that transforms a personal computer into a talking machine. The device can be applied to any language, says a KDD spokesman, because it can give a word natural pronunciation by editing phonemes and atomic speech elements. The Tokyo company's software provides the edited words or phrases with stress and intonation so the attachment's voice can speak with a natural accent and tones. KDD has not yet decided when the device will be available. It expects the systems to be used for telephone service, for electronic mail, and to aid the handicapped.

COMPAQ OPENS SINGAPORE PLANT

Compaq Computer Corp. has opened a printed-circuit-board assembly facility in Singapore, its first outside the U.S. Assembly began last month at the Houston-based company's facility. Monthly production is expected to exceed 40,000 units by the end of this year. Shipment of the boards to Compaq's main assembly facility in Houston is expected to begin this month, and the boards also will eventually be shipped to a facility in Scotland.

OPTOELECTRONICS SALES TO SOAR

The world market for optoelectronic components and systems will rise 20% to 25% annually, reaching about $35 billion by 1990, up from $16 billion last year, according to a report from the organizers of the Laser Show, scheduled for June 22-26 in Munich. Laser-based test and measuring systems and material processing equipment built around lasers will give the market the strongest boost.

NIXDORF, AMDAHL TO DEVELOP SOFTWARE

West Germany's Nixdorf Computer AG and Amdahl Corp. of Sunnyvale, Calif., are setting up a joint engineering team at each company to develop communications functions for Unix-based systems. The team will aim to develop software that allows better integration of Unix systems into heterogeneous networks—networks with computers from different manufacturers. The initial goal, Paderborn-based Nixdorf says, will be to embed Unix systems in OSI and in IBM's SNA networks.

MITSUBISHI CLAIMS RECORD SRAM CARD

Mitsubishi Electric Corp. will market in the U.S. and Japan what the Tokyo company claims is the world's largest capacity static random-access-memory card at 512 Kbytes. In Japan, the price will be 95,000 yen. To reach that capacity, Mitsubishi mounted sixteen 256-Kbit SRAMs on a 10 mm-thick card. Also in August, the company will launch a one-time programmable 512-Kbyte read-only-memory card, a 256-Kbit SRAM for memory cards, and a 256-Kbyte version of the SRAM and ROM cards.

PLESSEY WINS DOD AUSTRALIA ORDER

Plessey Co. has won a £160 million order from the Australian Department of Defence for 6,000 advanced tactical radios. The radios are based on the London company's System 4000, which is designed to give a "user friendly" performance and to operate in harsh climates.

CASTING RESIN HAS HIGH CONDUCTIVITY

Robnorganic Systems Ltd. has developed a high-thermal-conductivity encapsulating and casting resin called PX666C. The Swindon, UK, company has spent three years developing the resin, which, by using a combination of a nonabrasive filler and a high-purity resin system, has achieved a thermal conductivity of 1.4 W/mK. Its other qualities are low viscosity, flame retardancy, and minimal sedimentation in storage. The company says that the resin's main applications will be military.

FIRMS TO COOPERATE ON COMMUNICATIONS

Two communications-equipment makers, Hasler AG of Switzerland and West Germany's Telenorma GmbH, intend to work together in their common field. The emphasis of the cooperation between Bern-headquartered Hasler and Telenorma of Frankfurt, a member of West Germany's Robert Bosch group of firms, will be on private communication systems and local-area networks.

KYOCERA WANTS TO SELL VITELIC RAMs

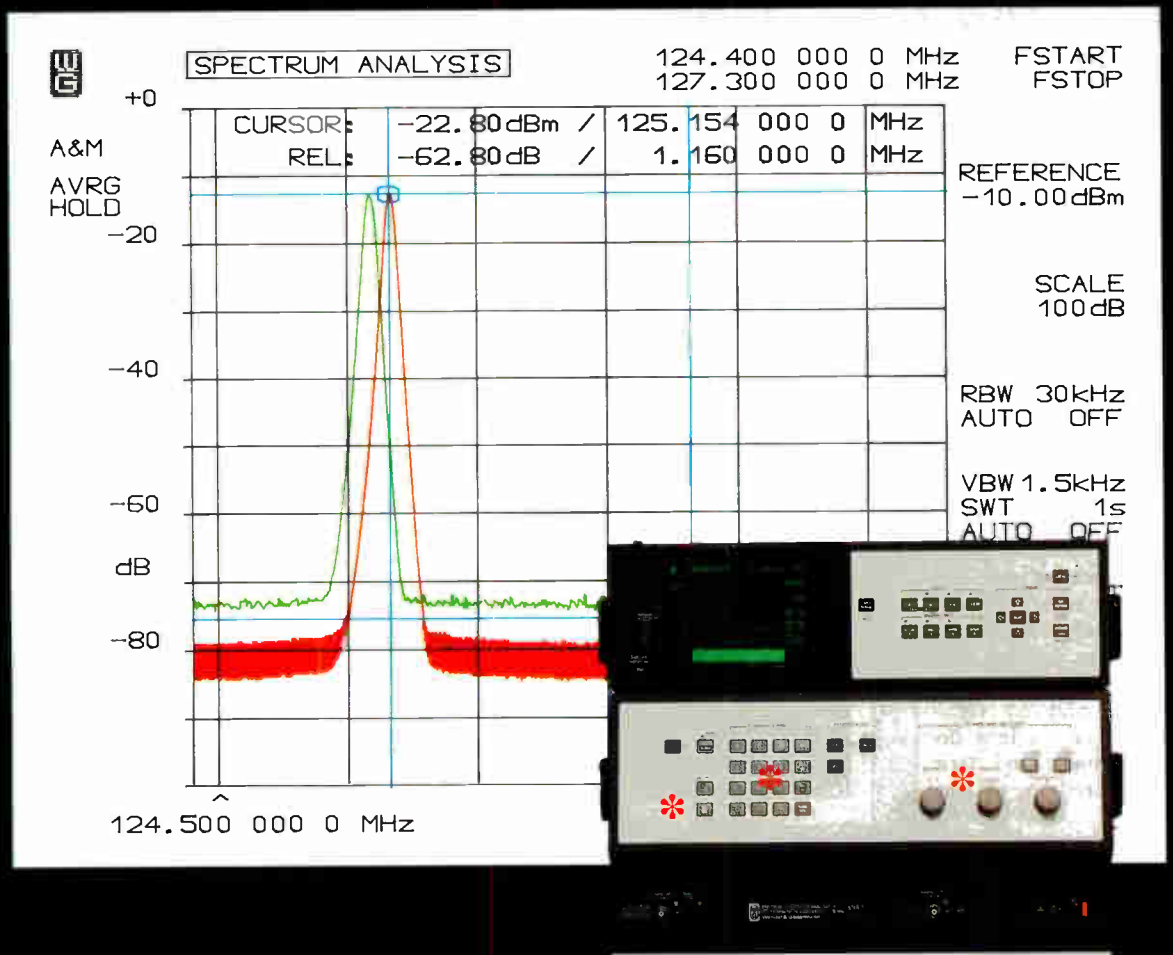
Integrated-circuit package manufacturer Kyocera Corp., Kyoto, Japan, is negotiating with Vitelic Corp., of San Jose, Calif., for rights to sell the American firm's dynamic random-access memories and static RAMs in Japan. Kyocera has an almost 10% equity position in Vitelic, which last year started selling its products through two Tokyo component traders, Internix and Microtek. Kyocera expects to sell about 200 million yen worth of ICs in the first year.

UK GROUP WARY OF BOOK-TO-BILL RISE

The UK book-to-bill ratio has managed to stay above parity for six months, but the Electronic Components Industry Federation is being only cautiously optimistic about the figures. The provisional figure of 1.34 for May follows a revised April figure of 1.17 and a March figure of 1.29, according to the federation, whose data accounts for 75% of UK semiconductor sales. "The trend is definitely upward," a spokesman says, but he warns that "the unevenness of the sales figures makes the rate of improvement difficult to quantify."

Wandel & Goltermann

Electronic Measurement Technology



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Circle 129 on reader service card

INTERNATIONAL PRODUCTS

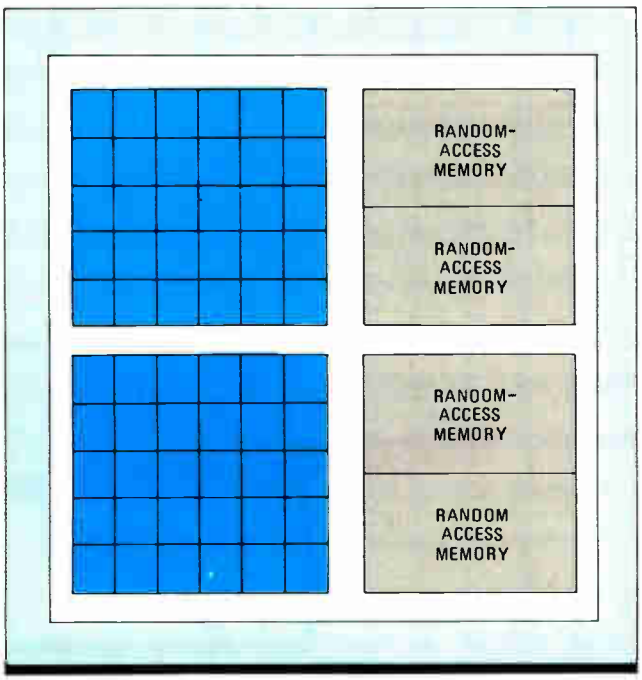
ECL GATE-ARRAY CHIP COMBINES LOGIC AND ON-BOARD RAM

FUJITSU CUTS POWER USAGE BY 50% AND SPEEDS MEMORY ACCESS 4 TIMES

Two application-specific integrated circuits from Fujitsu Ltd. combine logic and random-access memory on the same chip to cut power consumption and boost memory-access performance. By putting RAM on a chip with emitter-coupled logic and transistor-to-transistor logic, the company reduced power consumption by 50% and increased memory-access performance by a factor of four, compared with systems where logic and memory are on separate chips.

Having memory on an ASIC logic chip allows the RAM to interface directly with logic on the same chip, and that eliminates the output buffers between the memory and logic that are required in conventional systems.

The result is a maximum RAM access time of 5 ns. This compares with about 20 ns if the memory was off-chip—approximately 10 ns would be added in interconnection delay times between chips and 5 ns for input/output from the logic chip.



PLACEMENT. ECL gate arrays consisting of a 10-by-6 matrix of major logic cells, left, are complemented by four 256-word RAM arrays.

Power dissipation is 4.7 mW/gate for internal high-speed gates and 2.4 mW/gate for internal low-power gates. Because of the elimination of output buffers, the entire chip's power consumption of 8 to 10 W is about one-half that of a system with separate chips for memory and logic. The chips can be cooled with a 5-m/s airflow.

9-BIT WORDS. Two devices are available. The ET-2009M series has 1,920 gates and 9 Kbits of RAM organized into four arrays of 256 words each of 9 bits. The other option—the ET-3004M series—features more gates but at the cost of reduced memory. It has 2,880 logic gates and a 4.5-Kbit RAM organized as two arrays of 256 nine-bit words. Using 9-bit words makes system design simpler than with byte-wide memory chips because it gives designers a parity bit.

The chips are early entrants in a new breed of ECL devices intended to meet the needs of minicomputer designers pressed to deliver system performance in the range of 10 million to 15 million instructions/s while still cooling their computers with air flow instead of liquid coolants (see p. 71).

Specific applications include register files for central processing units and cache memory controllers. The chips should also find applications in communication controllers and palette controllers for graphics processing.

The prototype for the new devices is Fujitsu's 4,480-gate RT-4500 gate array. In the new devices, memory replaces some of the gates—one half of them in the case of the ET-2009M and one-fourth in the ET-3004M. A total of 96 different macros are available for configuring functional circuits.

In the 4.5-Kbit device, up to 90 major logic cells are available to the designer, each consisting of eight basic cells. A basic cell can be any of the following: dual two-input NOR, four-input OR/NOR, two-input OR-AND/NAND, or a D latch.

Internal gates have a typical propagation delay of 220 ps for fan-in and fan-out of one and no capacitive loading. A more typical value for fan-in and fan-out of three and 3 mm of aluminum wiring is 500 ps. Typical internal toggle rate is 800 MHz.

Both devices are fabricated on a 9.84-by-9.84 mm chip and sealed in ceramic pin-grid-array packages with 149 pins. To maximize heat transfer, the chips are mounted on the upper side of a downward cavity, providing the best thermal conductivity to a 6-fin heat radiator mounted atop the package.

Translation circuits at the periphery of the chip provide conversion to TTL input or output where desired.

Power supply voltage is –4.5 V for operation as ECL100K and –5.2 V for operation as ECL10KH. When operated only in TTL mode a single +5.0 V power supply suffices, but normally TTL input/output would be mixed with ECL and a +5.0 V supply would be used in addition to one of the negative ECL supplies.

ONE MICRON. The chips are fabricated with high-speed ECL technology featuring 1-μm minimum feature size. They have three layers of aluminum interconnections—two for logic and one for power supply. Three personalized masks are required for each customer design—one for each of two logic layers and one for through-holes between the logic layers.

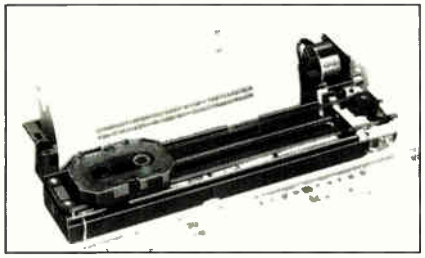
Fujitsu is taking orders now and has estimated the time from completion of logical simulation to delivery of engineering samples in Japan at five weeks. Fujitsu's development fee of 5 million yen includes five samples. Single-unit price in lots of 500 is 50,000 yen for the 1,920-gate, 9-Kbit ET2009M, and 45,000 yen for the 2,880-gate, 4.5-Kbit ET3004M. – *Charles L. Cohen*

Fujitsu Ltd., Semiconductor Marketing, Furukawa Sogo Bldg. 2-6-1 Marunouchi Chiyoda-ku, Tokyo 100, Japan.
Phone 81-3-216-3211 [Circle 500]

ALPS PRINTER USES 24-BY-24-PIN HEAD

High character resolution is achieved in Alps Electric Co.'s top-of-the-line thermal-transfer printer mechanism with the use of a 24-by-24-pin matrix print head instead of the more common 9-by-9-pin matrix.

The PTMTS42/43 prints 50 characters/s in a standard 80-column mode. Specially designed motors are used in the line and paper feed mechanisms to minimize noise and maximize paper-positioning accuracy. Up to 85 lines can be



printed on a standard letter-sized page.

Capable of battery-powered operation, the printer targets applications in laptop computers, word processors, terminal printers, and typewriters. It is available three months after receipt of order.

Alps Electric Co., 1-7 Yukigaya Otsukacho, Ota-ku, Tokyo 145, Japan.
Phone 81-3-726-1211 [Circle 701]

IBM-COMPATIBLE COMES WITH LARGER SCREEN

Lee Data International Ltd.'s model 1191 monochrome display terminal is plug-compatible with IBM Corp.'s model 3191 but offers a 14-in. screen in either green or amber, compared with IBM's green-only 12-in. screen.

Other features include support for a light pen, a station printer, or a bar-code reader, and a choice of either 87-key or 122-key keyboards.

Lee's 1192C color terminal is plug-compatible with IBM's 3192 terminal and lets users select a wide-screen mode to display a program listing or a long-screen formation to display more rows of text.

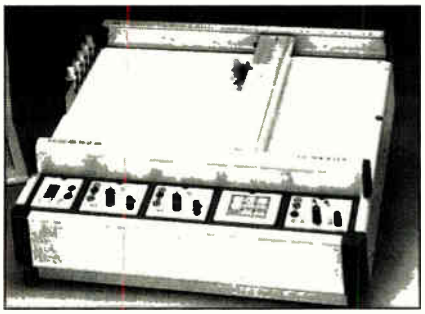
Available now, the model 1191 costs £750 and the model 1192C costs £1,200.

Lee Data International Ltd., 49 Dean St., Marlow, Bucks SL7 3BP, UK.
Phone 44-6284-76841 [Circle 702]

X-Y PLOTTER IS FAST, YET STILL IS ACCURATE

The LY1900 *x-y* recorder/plotter from Linseis GmbH features an acceleration rate of 500 cm/s^2, an end-speed of 100 cm/s, an accuracy of ±0.25%, a linearity error as low as ±0.1%, and a built-in time base with 12 selectable speeds.

The recorder can be remotely pro-



grammed—for pen up/down, color of pen, start/stop time base, and recorder-plot mode—by CCITT V.24, RS-232-C, and IEC-625/IEEE-488 interfaces. It also acts as a computer front-end in a computer-controlled measuring system. The sampling rate is 33 values per second.

Delivery time for the LY1900 is 12 weeks. It sells for 6,400 DM.

Linseis GmbH, P. O. Box 1404, D-8672 Selb, West Germany.
Phone 49-9287-79022 [Circle 703]

60-W POWER SUPPLY RANGES FROM 0 TO 30 V

Farnell International Instruments Ltd.'s power supply provides outputs over a range of 0 to 30 V, but is small enough to carry easily in one hand. Its maximum output is 60 W.

Power from the LS30-10 is adjusted by two 10-turn front-panel controls—one for voltage, the other for current. Resolution is to within 0.1 V and 10 mA. A full 10 A is available at 6 V; 6 A at 12 V;

2.5 A at 24 V; and 2 A at 30 V.

The unit measures 91 by 220 by 265 mm and weighs 2.1 kg. Available now, it costs £220.

Farnell International Instruments Ltd., Wetherby, West Yorkshire LS22 4DH, UK.
Phone 44-937-61961 [Circle 704]

SIEMENS UPGRADES DISK CONTROLLERS

Siemens AG's SAB2793/97B floppy-disk controller has improved operating characteristics over its predecessor, the 97A version, thanks to the use of a voltage-controlled oscillator with a steeper voltage rise.

The 97B controller's improved voltage characteristic means shorter capture times and improved control profiles. Its temperature-time curve is 2.5 times better than that of the 97A.

Suitable for 5¼-in. or 8-in. floppy disks, the SAB2793/97B is available from stock. Price depends on importing country.

Siemens AG, P. O. Box 103, D-8000 Munich 1, West Germany.
Phone 49-89-2343613 [Circle 706]

METER HANDLES SWR AND POWER DUTIES

Kaise Electric Works Ltd.'s SK-2300 series combines standing-wave-ratio and rf-power measurements for antenna systems in a single, compact instrument.

Two versions are available. The SK-2300 offers a frequency range of 1.8 to 150 MHz, while the SK-2310 is designed for 130 to 500 MHz. Both measure power to an accuracy of ±15% full-scale and have three selectable power ranges: 2 W, 20 W and 200 W.

Minimum power required for SWR measurements is 0.3 W for the SK-2310. For the SK-2300, minimum power varies with frequency from 75 W at 1.8 MHz to 0.1 W at 150 MHz.

Both instruments have separate meters for SWR and power measurements. The units are 180 mm wide, 68 mm high, and 110 mm deep and weigh 730 g.

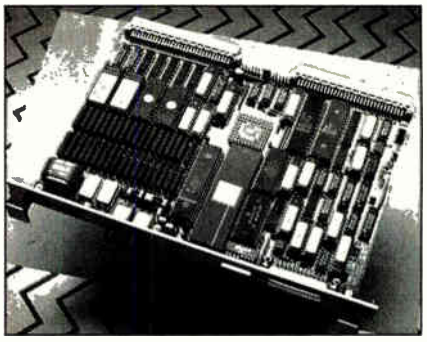
Available now, the SK-2300 costs 7,200 yen and the SK-2310 9,300 yen.

Kaise Electric Works Ltd., 422 Oaza Hayashinoso, Ueda, Nasano 386-01, Japan.
Phone 81-262-35-1600 [Circle 705]

SBC BOASTS 68010 and 1 MBYTE RAM

A single-board computer from High Technology Electronics Ltd. features a Motorola Corp. 68010 microprocessor and no-wait states on up to 1 Mbyte of dynamic RAM.

The HVME-SB68S supports the processor on both its 10- and 12.5-MHz operational modes. With the addition of a terminal and power supply, the board can run as a stand-alone processor, and units can be cascaded to create multi-



processor systems. The inclusion of a small computer systems interface, dual serial ports, and a parallel communications port make it a good candidate for such applications as work stations, multiuser systems, and development systems.

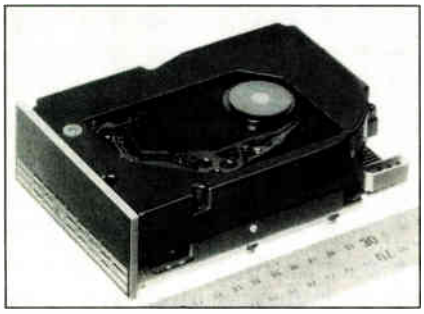
Available now, the HVME-SB68S board computer costs £1,256.

High Technology Electronics Ltd., 303 Portswood Rd., Southampton, SO2 1LD, UK.
Phone 44-703-581555 [Circle 707]

DRIVE HAS BUILT-IN SCSI INTERFACE

The DRM020D 3½-in. hard-disk drive from Alps Electric Co. features a built-in Small Computer Systems Interface controller and a balanced swing arm for enhanced resistance to vibration damage.

The 20-Mbyte drive has an average



access time of 75 ms. The drive can be delivered with an optional circuit to protect the disk in the event of a power failure or accidental shutdown.

Available three months after receipt of order, the drive is 41 mm thick, 102 mm wide, and 150 mm deep; it weighs 850 grams.

Alps Electric Co., 1-7 Yukigaya Otsuka-cho, Ota-ku, Tokyo 145, Japan.
Phone 81-3-726-1211 [Circle 708]

PRESSURE CONVERTER COVERS WIDE RANGE

The model 4283A pressure transducer from Kistler AG measures absolute pressures over a range as wide as from 0 to 400 bar. Thanks to its compact design—it is only 120 mm long—the transducer fits in tight locations. It is connected to the associated electronics system by a 4-pole DIN connector or an integrated cable.

The transducer's front end, made of high-quality steel, makes the 4283A suitable for use in harsh environments. The soldered diaphragm guarantees perfect sealing between medium and transmitter electronics. The 4283A costs 683 Swiss francs. Large orders take from four to six weeks to handle.

Kistler AG, P. O. Box 304, CH-8408 Winterthur, Switzerland.
Phone 41-52-831111 [Circle 709]

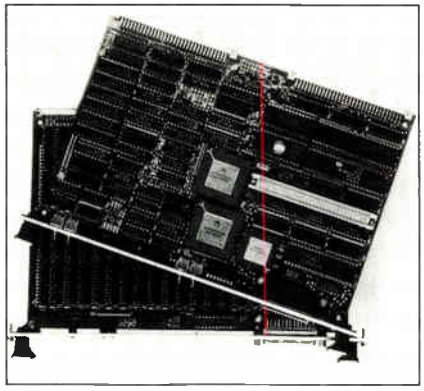
BOARD COMPUTERS MANAGE MEMORY

The latest additions to Force Computers GmbH's range of 32-bit single-board computers, based on Motorola's 68020 microprocessor, feature a page memory management unit.

The CPU-24 and CPU-25 also support an interface to the proprietary Force local memory extension (FLME) interface, which provides an extension to the local processor bus.

The two boards have 512 Kbytes of high-speed static RAM accessible through the FLME interface, allowing the processor to run with only one wait state at clock frequencies of 16.67 MHz, even with the page memory management unit.

Two serial input/output channels are provided via two multiprotocol communications controllers that support bit-oriented and character-oriented protocols. The baud rates are software-programmable up to 38.4 Kbits/s (asynchronous) or 4 Mbits/s (synchronous).



The CPU-25 has a Motorola 68851 floating-point coprocessor that runs at 16.67 MHz. Delivery time for the boards is approximately 4 weeks. The CPU-24 sells for 12,950 DM, and the CPU-25 costs 13,900 DM.

Force Computers GmbH, Daimlerstr. 9, D-8012 Ottobrunn, West Germany.
Phone 49-89-600910 [Circle 710]

LASER PRINTERS CAN EMULATE IBM UNITS

KMW Systems International's 3XLaserLink lets Hewlett-Packard Co. LaserJet printers emulate IBM Corp. 5219 printers in an IBM System 3X environment. The protocol converter supports such 5219 features as proportional spacing, right justification, and font switching.

The system consists of the company's

Matchbox Model 4 protocol converter and an application-specific software package for the System 3X. All IBM commands are supported except those that the HP printers cannot execute, such as alternative input/output trays.

Other IBM features that are supported include underlining, overstriking, superscripting, subscripting, and manual envelope feed.

The 3XLaserLink is available now with either a serial interface or a Centronics parallel interface; it costs £995.

KMW Systems International, Falcon Way, North Feltham Trading Estate, Middlesex TW14 0QX, UK.
Phone 44-844-1525 [Circle 711]

I/O BOARD LINKS EUROBUS CHANNEL

PEP Modular Computers GmbH's SIO-4N board offers a quad serial input/output interface module for the intelligent I/O channel Eurobus.

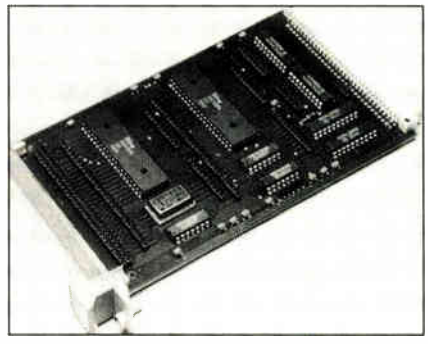
The module can be delivered with one or two serial communications controllers, resulting in two or four independent I/O channels, respectively. The multiprotocol data-communications peripheral works at 8 MHz for data rates up to 76 Kbits/s on each of the four channels.

The module can be software-configured to handle many protocols, such as synchronous and asynchronous transmission formats.

Four piggybacked modules can be mixed to configure the communications lines needed for a wide range of applications. The SIO-4N can be used with all of PEP's CPU modules.

Available from stock, the SIO-4N modules cost 470 DM each.

PEP Modular Computers GmbH, AM Klosterwald 4, D-8950 Kaufbeuren, West Germany.
Phone 49-8341-8974 [Circle 713]



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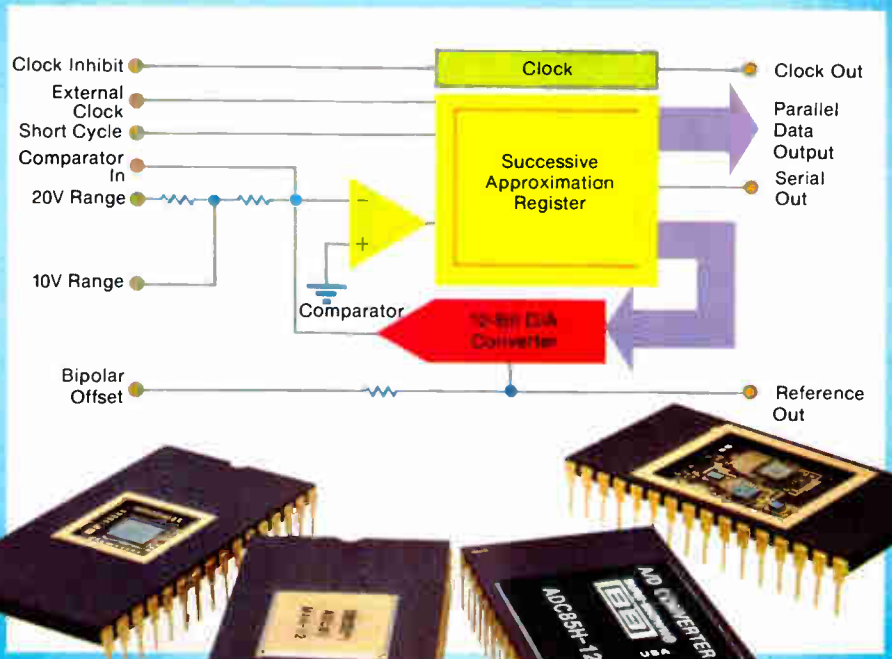

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- Lower prices.
- Complete devices, with comparators, 12-bit DACs, laser-trimmed voltage references, SARs and clocks.
- 40kHz (ADC80MAH-12) or 100kHz (ADC84, 85H, 87H) sampling rates.
- Lower power dissipation.
- Special "/QM" screening available.

KEY SPECIFICATIONS	ADC80MAH-12	ADC84, 85H, 87H
Resolution	12 bits	
Linearity error, max	0.012%FSR	
Conversion time, max	25μs	10μs
Gain tempco, max	±30ppm/°C	±15ppm/°C
Package	32-pin hermetic ceramic DIP	
No missing codes	−25/+85°C	0/+70°C, −25/+85°C, −55/+125°C
Power dissipation, max	705mW	725mW
Price*	$30	from $48

*Unit price, U.S. only, in 1000s.

For complete information on these brand new, industry-standard ADCs, contact your Burr-Brown sales representative or Applications Engineering, 602/746-1111. Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734.

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See Cadnetix Analog Design Environment at DAC booth #1149

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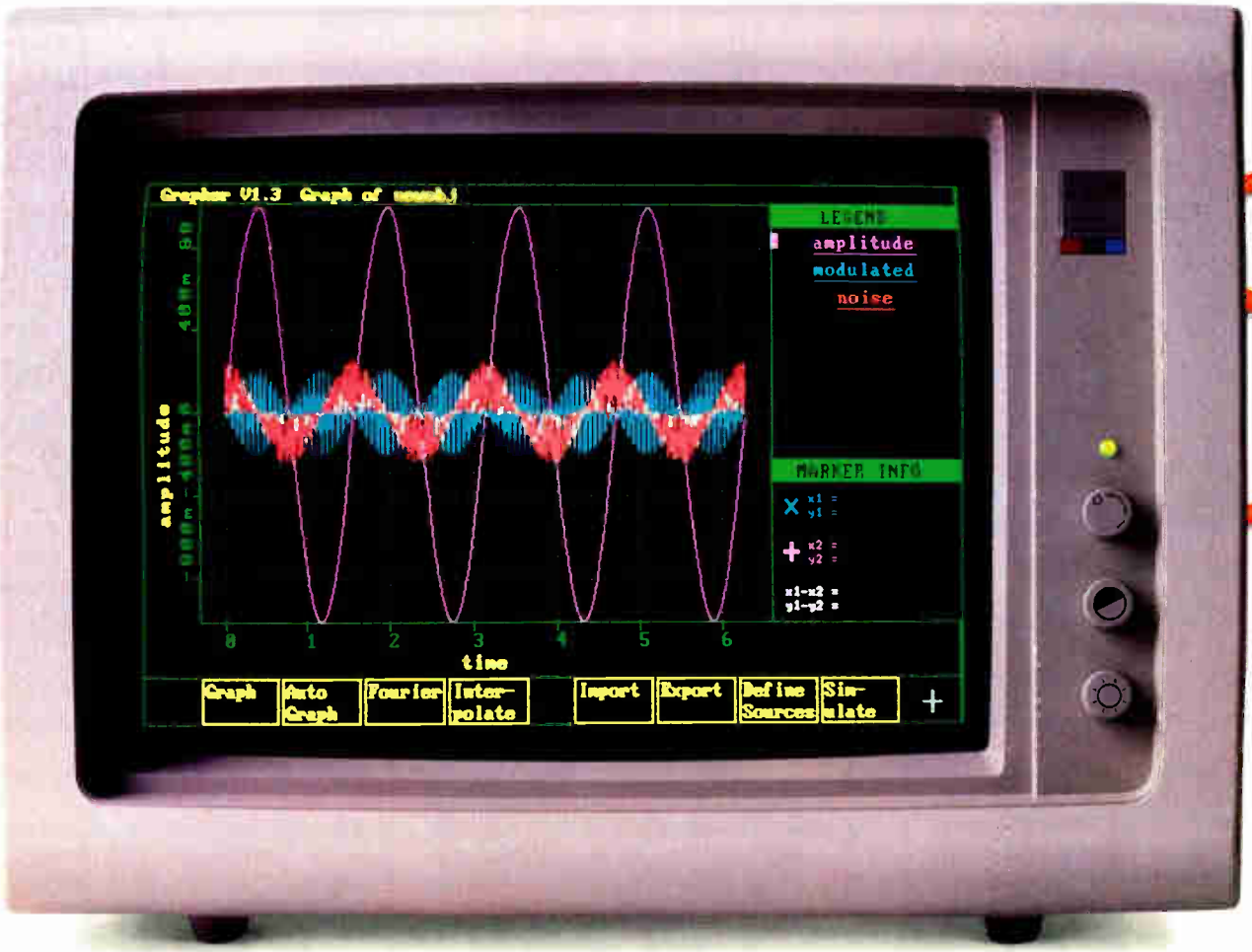
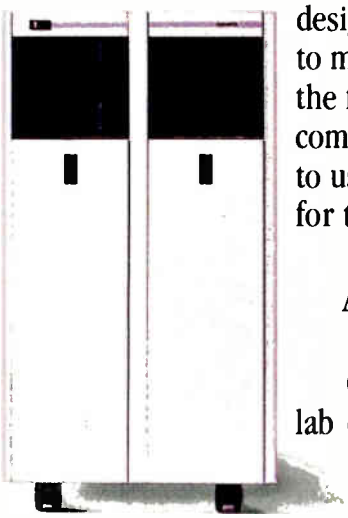


Cadnetix Analog Design Environment.

Cadnetix introduces the Analog Design Environment™ — a unique set of tools to meet the special needs of analog system designers. Cadnetix combines its system design expertise with an innovative analog simulator — Saber.™ While other analog tools are targeted to IC designers and are difficult to master, Cadnetix is at the forefront in offering a comprehensive and easy to use analog environment for the system designer.



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Cadnetix puts an analog lab on every designer's desktop with our unique Analog Data Grapher.™ Your DOS™ PC/AT performs as a multi-channel oscilloscope, a network analyzer, a frequency generator, and other instruments used in design and breadboard debugging. The Analog Data Grapher provides a wealth of features including Fourier Analysis and Linear and Spline Interpolation. And like all Cadnetix tools, it's powerful, yet exceptionally easy to use.

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Cadnetix lets you do what's never been done. Thoroughly analyze your analog design before working out a detailed implementation. Unlike other analog simulators, the Saber simulator uses a hierarchical approach which allows you to describe circuits at a functional level. No complicated macromodels, painstakingly built transistor by transistor, are required for simulation — eliminating excessive compile and computation time.

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Analog designers need substantial processing power for fast and thorough analyses of complex analog systems. Cadnetix lets you perfect your design with powerful tools that perform even the most complex analysis in record time. It's easy to make modifications then resimulate. Cadnetix Configurable Analysis Engine — a powerful network resource — significantly accelerates compilation and simulation for rapid design verification.

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Cadnetix offers all the tools you need for productive system design — from schematic capture and analysis, to layout, routing and manufacturing. Cadnetix CAE, CAD and CAM products are completely integrated. Our CAD tools support sophisticated features to layout and route analog designs, including curved traces, intricate copper fill areas, and automatic pad filleting.

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PROBING THE NEWS

SOFTWARE STARS AT THE DESIGN AUTOMATION CONFERENCE

DESIGNERS WILL FINALLY GET THE APPLICATIONS PROGRAMS THEY NEED

by Jonah McLeod

Circuit and system designers finally are starting to get the applications software they need to make computer-aided engineering a practical proposition. A vast range of these new CAE tools will star at the Design Automation Conference in Miami, June 28 through July 1. And it's about time, since CAE has long promised to make life easier for designers of both integrated circuits and printed-circuit boards. While there are plenty of applications packages out there, the current crop hasn't been designed to work together efficiently. As a result, the percentage of designers who use CAE in their everyday work is no more than 14%, according to the Technology Research Group Inc., a Boston market researcher.

Now the exhibitors at the conference are trying to boost that figure. They will display a plethora of packages that engineers have been demanding. The new products include stronger individual tools. But more important, they will offer better integration among the different front-end tools for designing ICs and pc boards and among the varied back-end layout tools. Some of the new packages also promise better integration between front- and back-end tools. Also bowing at the show are an impressive number and variety of new hardware platforms and accelerators.

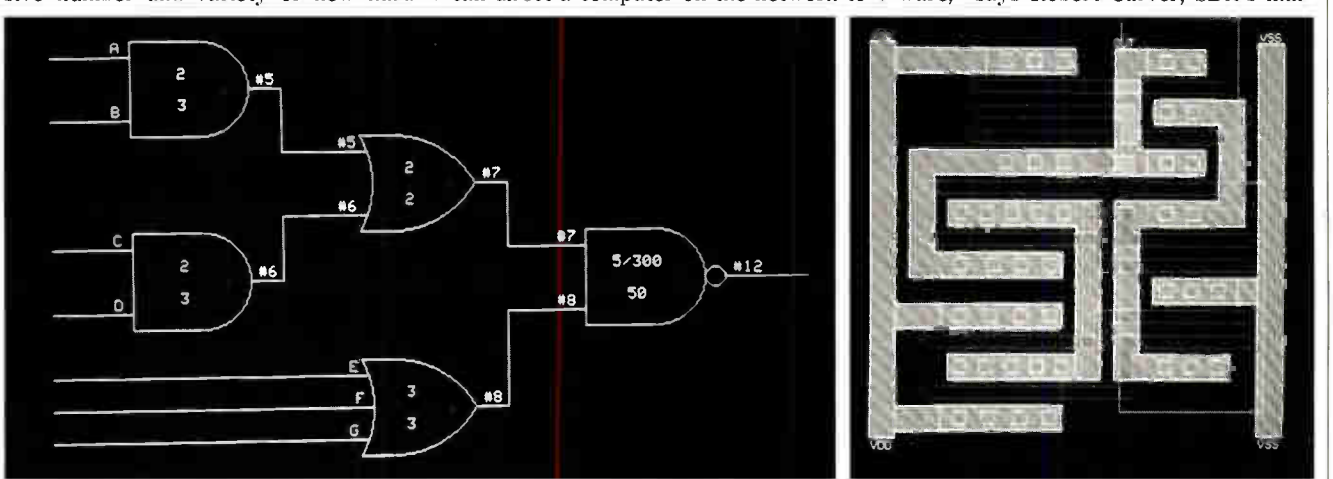
The parade of hot new software starts with front-end schematic capture and simulation software packages. For one thing, tool suppliers are beginning to recognize that it makes more sense to perform schematic capture on a personal computer rather than tying up an expensive, more capable work station. So they're turning out the kind of package exemplified by Entry!, from Daisy Systems Corp., Mountain View, Calif.

Entry! is a schematic-capture package that runs under the MS-DOS or Unix operating system on an IBM Corp. PC AT or compatible. The $5,000 package is a response to the low-end schematic-capture packages, costing about $500, coming from companies such as Visionics Inc. of Sunnyvale, Calif.

Entry! costs significantly more, but it offers a lot more, particularly in its networking capabilities. It works over Ethernet, communicating with larger work stations, minicomputers, and mainframes using Network File Service, the networking file system introduced by Sun Microsystems Inc. of Mountain View, Calif., and adopted as a *de facto* standard by most major work station vendors. A user enters his schematic design into a file on a PC; thereafter, he can direct a computer on the network to simulate the design by using the file in the PC's memory.

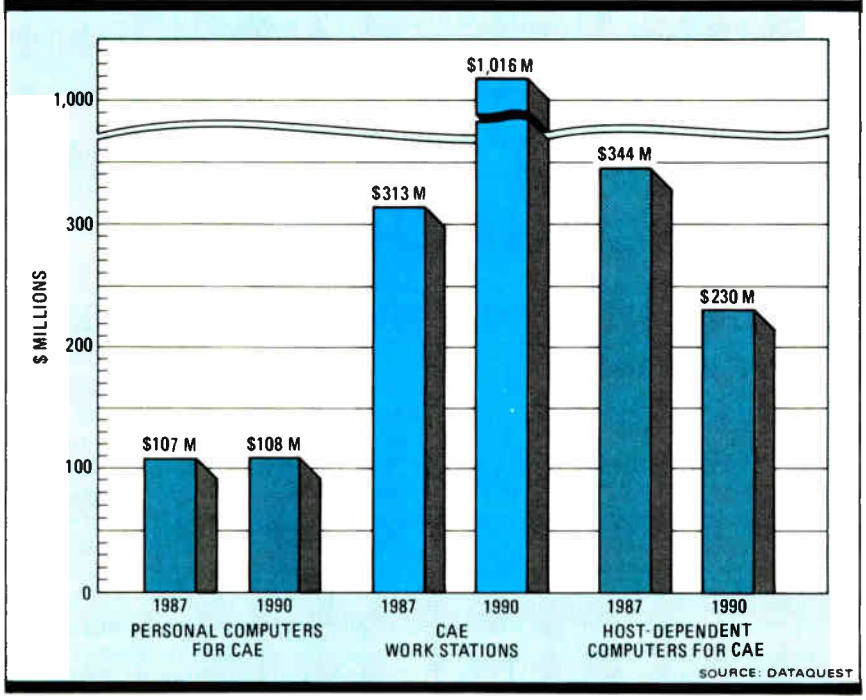
A key goal for suppliers of front-end design software is total integration—making design a computerized cradle-to-grave operation (see "HP's Young: Islands of automation aren't the answer," p. 62). The new Vanguard Stellar, for example, is a windowed operating environment for pc-board designers, inside of which are integrated a number of design tools: a schematic design system, simulators, a design rule checker, and more. Its maker, Case Technology Inc. of Mountain View, Calif., says all of the individual tools in Vanguard Stellar can be operating simultaneously. All provide the same user interface. In addition, the company has designed a common ASCII data base that all tools use in common. A schematic symbol entered during capture has associated electrical data for simulation, packaging data for layout, and so on. Being contained in ASCII form, the data can move easily from one hardware platform to another.

Integrated design environments also are showing up in IC design software. For example, Framework from SDA Systems Inc. of San Jose, Calif., is one such package. "Many design systems today are loose amalgamations of software," says Robert Carver, SDA's mar-



AUTOMATIC LAYOUT. From a schematic diagram input (left), the Layout Synthesis automatic-layout generator from Caeco Inc. produces a full custom layout (right) that comes within 10% of the density of a manual design.

WORK STATIONS WILL TAKE OVER THE CAE MARKET



keting manager. "A CAE-tool user today typically owns a collection of tools from different vendors—a schematic-capture package from one vendor, a simulator from another, and perhaps some tools of his own. Until now, each tool had its own data base. When the design data in the file had to be passed from one tool to another, a translator had to be called in to translate the data into a form the next tool could understand." Framework, by contrast, is a unified data base with a single interface to the design data, so new applications can easily be added to its tool kit.

Easy integration at designers' workbenches, sort of a software retrofit, is the goal of a simulation integration kit called SimKit. The brainchild of Analog Design Tools of Menlo Park, Calif., SimKit is aimed at designers who already have their own analog simulators and model libraries. The kit will strengthen those capabilities by adding Analog Design's icon-based, mouse-driven interface and analysis tools.

The big news in back-end CAE tools is the introduction of artificial-intelligence techniques, and exhibitors at the Design Automation Conference will be introducing AI-based packages. One example is the new Allegro pc-board design system and a knowledge-base router from Valid Logic Systems. The San Jose company claims Allegro is the first pc-board system that is driven by the engineering rules used during the front-end design process. "The CAE engineer entering the schematic can also direct the placement of the back-end layout," says Katherine Gambino, product marketing manager. "In the past, there has been little direction from the designer as to how a board should be laid out."

To work with Allegro, a designer starts with an outline of the board. Then he specifies which part of the schematic goes in what general area of the pc board. Placing related components in specific areas of the board simplifies the job of the routing tool. Consequently, a job that used to require routing accelerators can now run on standard work stations. "In one benchmark we ran, Allegro, along with a new version of our router, placed and routed 150 chips in three minutes on a Sun work station," says Gambino.

The introduction of AI techniques is the big news in back-end tools

The new Valid router, called Insight-Plus, is interesting in its own right—it incorporates a knowledge base containing rules that adjust the routing algorithms to fit a given design technology. For example, within a schematic the designer can specify that a net contains high-frequency emitter-coupled-logic components. He can specify the minimum and maximum trace widths, and he can request that a trace on the pc board be constrained to a particular layer. The netlist compiler translates these specifications into rules to be interpreted and followed by the router.

Other new routers also will use AI techniques to perform other time-consuming routing tasks. One example is the Star, for strategic automatic router, from Daisy Systems. "In the past, the circuit designer prepared a routing plan in a command file that he passed to the router," says David Barnett, marketing manager for Daisy's pc-board division. "Because Star already knows the rules for pad sizes, trace widths, spacings, etc., it can create the routing plan based on heuristics—methodologies used by designers for creating routing plans—built into the program."

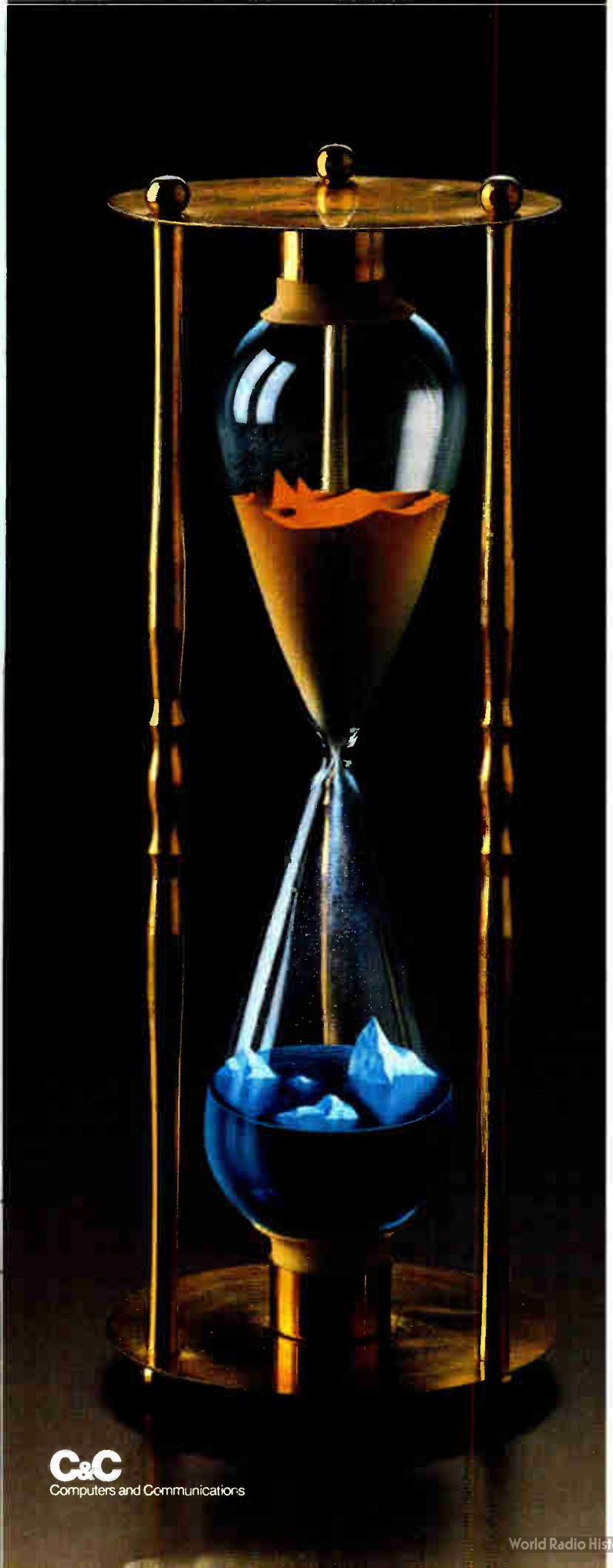
Star specifies the sequence of passes for the routing operation. In a first constructive pass, it might specify a route without vias. On designs that have connections running at 45°, the Star router can use a 45° pass that provides higher trace density and shortens the connections between devices for improved electrical performance. In still another pass, Star might initiate a rip-up and reroute router. The router can end by running a manufacturing routing pass that reduces the number of vias and optimizes interconnections of 45° routings, among other improvements.

Repeating tasks intelligently during circuit layout is the hallmark of another package, this one from Caeco Inc. Called the Layout Synthesis automatic-layout generator, it is intended for IC design. The Sunnyvale company claims the package is the first that can create a full-custom IC layout from a schematic diagram which is design-rule correct and therefore comparable to a layout done manually (see photograph, p. 57).

The package can create a layout for custom IC design with two to three times the density provided by standard cells and within 10% of the density provided by manual designs, says John Claiborne, Caeco's executive vice president. "But more important, once the system has created the layout, the IC designer can then call on a layout editor to improve the layout even more."

Initially intended for the IC designer—a later version will be aimed at system designers—the layout tool is designed to boost productivity in laying out random logic on a complex chip containing macrocells, such as programmable logic arrays, random-access and read-only memories, and a central processing unit. To ease placement and routing, the Layout Synthesis tool creates a logic block that's the equivalent of a macrocell.

It will take powerful hardware to run the new software tools, and so the market for work stations is expected to treble in the next three years. It will jump from $313 million this year to $1.02 billion by 1990, says Dataquest, a San Jose, Calif., market research firm (see chart above). Demand will heighten as work-station prices fall, thanks to the availability of chips like the Intel 80386, and as competition intensifies with the



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	France	Tel:1-3946-9617. Telex:699499 NEC EF.
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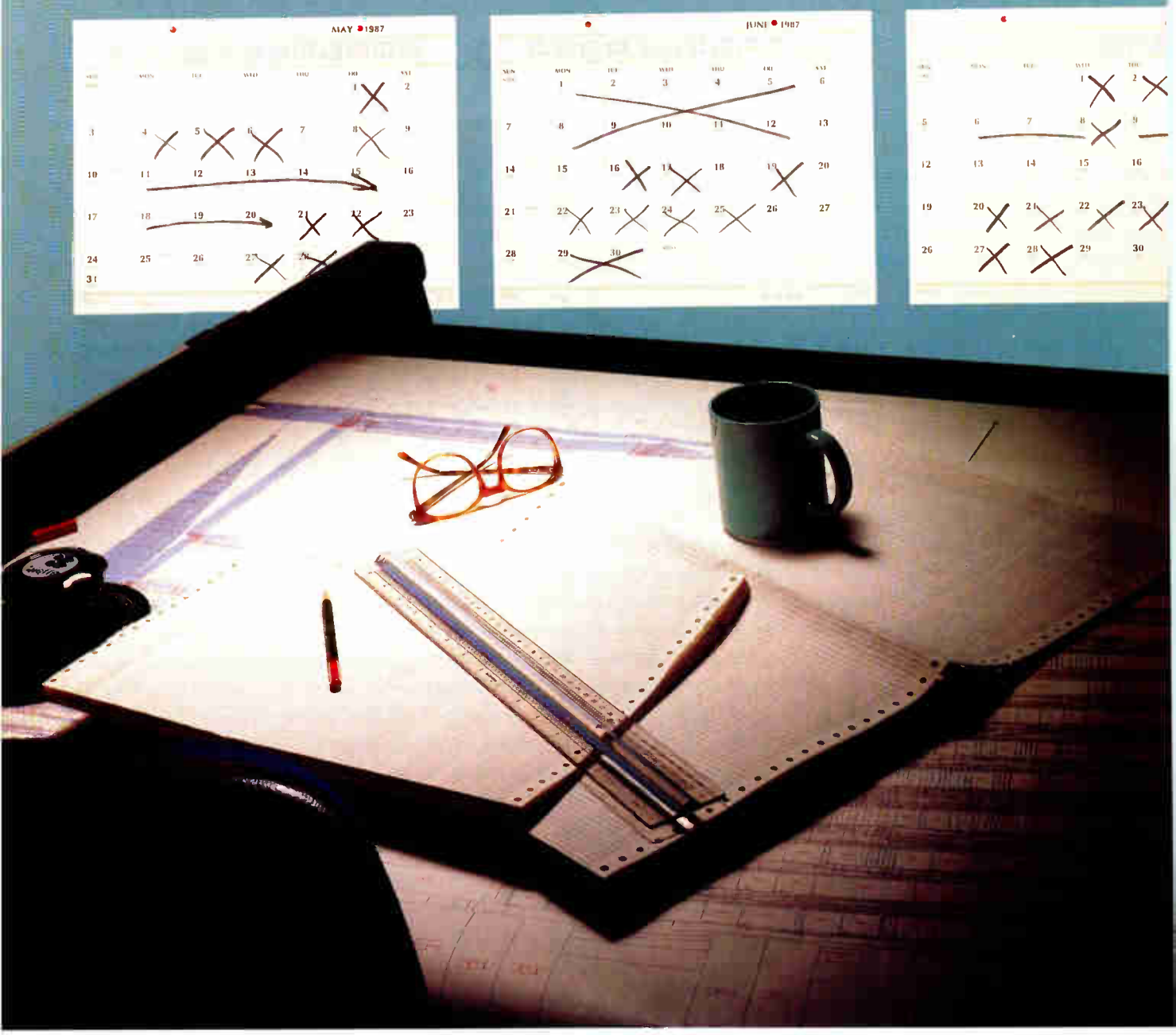
Three months



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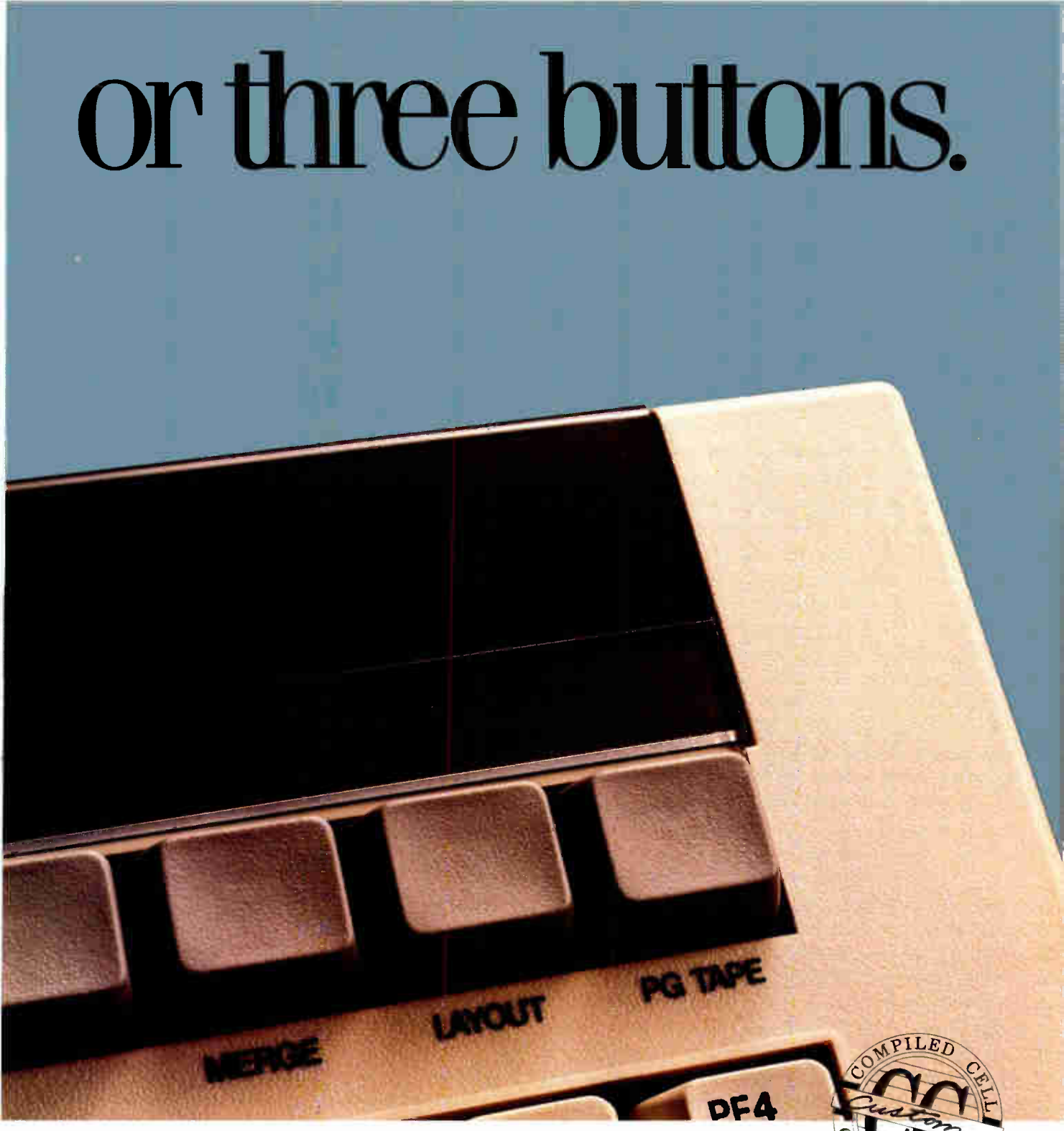

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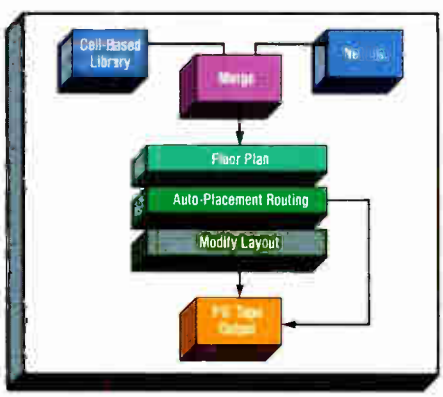

COMPILED CELL Custom CUSTOM

S-MOS SYSTEMS
A Seiko Epson Venture

Circle 61 on reader service card

appearance of the 68020-based Apple Macintosh II and other machines selling for about $5,000.

That means the latest work stations will be high-end, 80386-based machines that offer performance an order of magnitude or more better than older equipment. The performance gain will come either from the use of the 386 and its peers or through architectures or accelerators incorporating floating-point coprocessors and reduced-instruction-set-computer techniques. The high-powered work stations will eat away at the market for the IBM PCs and its compatibles that are based on earlier chips like the 80286. Dataquest expects PC sales will stay flat through 1990. Sales of minicomputers and mainframes used in CAE will decline by 1990.

Two of the new hardware platforms at the Design Automation Conference, the models 340 and 360 from Integraph Corp. in Huntsville, Ala., aptly demonstrate some of the newfound power (see p. 87). A coprocessor board containing dedicated floating-point and integer processors provides higher performance, by an order of magnitude, than that of the main CPU for the work station—the 5-million-instruction/s 32-bit Clipper chip from Fairchild Semiconductor Corp. The board accelerates any computation-intensive task—analog simulation, board layout, solids modeling, and the like—by executing the task from high-speed writable control store memory on-chip. The user determines what task to accelerate by microcoding the task and loading it into the control-store memory.

Another way to accelerate, from Mentor Graphics Corp. in Beaverton, Ore., takes less computation muscle—RISC architecture and extensive pipelining team up to achieve up to 8 million floating-point-operation/s performance. But there's a new twist: networking. Model-M, a new version of Mentor's Compute Engine global accelerator, is a networked, stand-alone version of its Model-V two-board add-in accelerator. By networking with the DN3000, DN500, or DN600 Series work stations from Apollo Computer Inc. of Billerica, Mass.—the hardware platforms for Mentor design tools—the accelerator does analog simulation six times faster; MOS analog simulation ten times faster; and gate-array and standard-cell placement four times faster than a DN 3000 work station working alone.

The work-station market will triple by 1990, thanks to 386-based machines

RISC architecture speeds up Hewlett-Packard Co.'s new platform, the HP825SRX work station. HP claims its machine outpaces the standard for comparison, Digital Equipment Corp.'s VAX 11/780. "In an integer-calculation based benchmark of CPU performance, the HP825SRX work station showed a performance of 8.5 MIPS," says Dan Vivoli, HP product manager. "That's 8.2 times faster than a DEC VAX 11/780." The HP825SRX CPU is implemented in HP's own 1.2-μm NMOS process, which helps the work station achieve its high performance.

However, DEC will have its own new work station at the Design Automation Conference, and it sets a new mark in price-performance for color work stations. The $7,900 VAXstation 2000 is only one contender in an expanded entry of CAE products from the Maynard, Mass., company.

Also bowing at the show is some of the fastest three-dimensional graphics processing around comes in a new graphics display system from Seiko Instruments U. S. A. Inc. (see p. 95). The San Jose, Calif., company's GR-4416 can display 400,000 fully transformed and clipped 3-d vectors per second—that's equivalent to high-end systems costing 20% more than the GR-4416's $32,000 price. □

HP'S YOUNG: ISLANDS OF AUTOMATION AREN'T THE ANSWER

Buyers of design automation systems are no longer satisfied with automating a single task, says John Young. They want equipment and software that tie together to automate the entire design process, says the president and chief executive officer of Hewlett-Packard Co., Palo Alto, Calif. An executive thoroughly familiar with the issues of integration, Young will be the keynote speaker at the Design Automation Conference held in Miami June 28 through July 1.

Young predicts that the integration of front-end computer-aided-engineering tools, such as simulation and schematic-capture software, with back-end computer-aided-design functions, such as chip and board layout, will be followed by the integration of additional steps in the process. Back-end CAD will link up with systems for computer-aided-manufacturing and with automatic testers. At the front end, tools for computer-aided software engineering will work with CAE functions for hardware design.

JOHN YOUNG

A number of networking issues must be faced squarely as this integration process proceeds, Young emphasizes. Industry standards for networking are crucial to the new links being formed between equipment from different vendors, for example. Young also feels that 10-Mbit/s Ethernets are not going to be up to the task as integration places more loads on the network.

One factor contributing to the recent slowdown in the design-automation industry, says Young, was that system buyers found they had anti-synergistic, isolated islands of automation within their companies. "Corporate management decided to take a hard look at the problem," Young explains. During that study period, new automation-equipment purchases were cut back. Automation in one area can improve productivity, but if productivity bogs down in an adjacent area, Young says, "you've made an investment and realized little return."

"I don't think [integrating the design process] is as much a technical problem as a management problem—of being willing to deal with the larger engineering process," he says. "Management has to start thinking of CAE as the front end of a total CIM system."

At the last two Design Automation Conferences the industry saw CAD beginning to be integrated with automatic-test and CIM equipment, Young points out. In the future, he expects to see software-engineering tools that work with CAE tools. Vendors of application-specific integrated circuits, for example, are setting up software-development systems so that programs can be run on simulated models of hardware being developed.

Changes in the networks for these tools are inevitable as well, Young believes. Networking standards are major factors in the integration of all design stages and in linking equipment from different vendors. "Five years ago, [HP] made the decision to throw out our proprietary networking approaches and go only with standard networking products," Young says. Digital Equipment Corp., on the other hand, is building systems around its proprietary DECnet. Young contends that DEC talks of embracing standards, but goes no further than a low-level physical connection.

Network bandwidth will also be a problem during the next five years as more tools start communicating, Young warns. Traffic will eventually consume all the bandwidth on an Ethernet. "There is a lot of work underway on networks capable of 100 to 200 Mbits/s," he says. *–Jonah McLeod*

OPINION

LOOK FOR ALLIES AT HOME, NOT IN ASIA

CARMELO J. SANTORO
The chairman, president, and chief executive officer at Silicon Systems Inc., Tustin, Calif., received a PhD in solid-state physics from Rensselaer Polytechnic Institute in 1968. He has served as chief scientist at Motorola Semiconductor, has run the integrated-circuit operation at RCA Solid State, and has held posts of senior vice president of standard products and senior VP for operations at American Microsystems Inc. He joined Silicon Systems in 1982.

The only way small U. S. niche semiconductor companies can survive the shakeout that is coming—and is already under way for some—is to pursue cooperative alliances with large general-purpose firms. Niche companies realize this, but something is basically wrong. So far, such alliances have been established almost exclusively with companies in Japan and Korea.

The costs of failing to set up alliances within the U. S. may be very high. It is my belief that we are risking our only certain advantage over the tough Far Eastern competitors—market leadership in ASICs. We still have the capability to conceive of these products on a more timely, competitive, and knowledgeable basis.

Through alliances with big chip houses, small niche companies can take advantage of the manufacturing economies of scale that we now lack and that are too costly for many of us to build. The large IC companies in return get superior application-specific integrated-circuit products because smaller companies have a better understanding of the niche, are closer to the major customers, and can define products that better serve the demands of the niche. The "economies of development" that exist in a niche company can be passed on to the big company, exchanged for economies of manufacturing.

The predominance of alliances between U. S. niche companies and big foreign IC vendors is the healthiest mechanism for our survival. Why can't the relationships be kept in the U. S.?

One reason is that the mutual trust that must exist before negotiations can proceed is notable by its absence. Smaller niche companies fear product piracy and what they consider to be unscrupulous tactics on the part of the larger company. They see their products as the "family jewels" and believe they must protect them.

But one could easily ask why we don't have these same fears when dealing with a foreign corporation—particularly one from Japan—but amplified. Aren't the histories of other industries or, as a matter of fact, the history of commodity products in our own, enough to convince us of where our trust should lie?

For their part, the larger U. S. companies appear to be saturated with the "not invented here" syndrome and are inclined to think of all sorts of reasons why products from smaller companies are not what they need. They also tend to be overly protective of their investment in process development and manufacturing technology—a justifiable position.

The truth is that large U. S. firms consider ties with U. S. niche companies a low priority, relative to their own efforts to get ASIC operations up and running. Their lack of success, however, in emulating the small companies' service structure and turn-on-a-dime responsiveness would seem to compel them to seek out alliances. But that isn't happening.

The apparent difficulty of teaming with a large U. S. chip company has deep implications for the industry. Both niche companies and large U. S. firms are treading a slippery path. The small companies are living without economies of scale and are essentially giving away leadership products for the privilege of using Japanese foundries. Even when these agreements start out solely as wafer-purchasing pacts, they seem inevitably to end up as an exchange of products for manufacturing capability. We cannot afford to continue in this direction.

Can we turn things around at this late date? I think we can. We need to take small steps. We need to begin with more trusting U. S. alliances. We need to explore areas where product-foundry relationships can be made to happen in the U. S. Larger U. S. companies should open their eyes to the fact that product lines from niche companies enhance their own. Second-sourcing agreements, agreements for enhancing cell libraries, and macrocell development agreements are among the plethora of possibilities that come to mind. □

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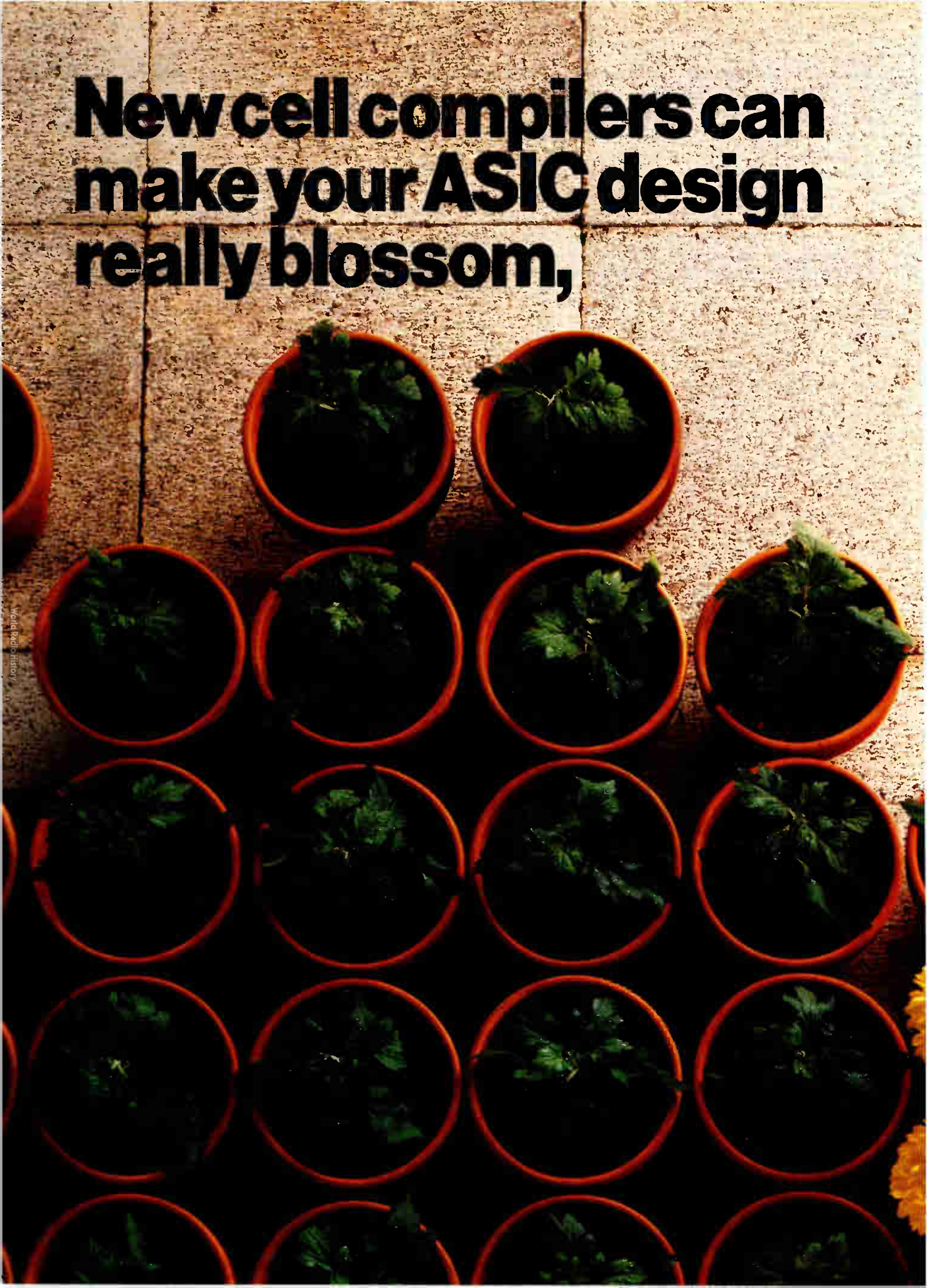

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INSIDE TECHNOLOGY

ECL'S WORLDWIDE DRIVE TO TAKE OVER TTL SOCKETS

A more flexible, denser breed of ECL that needs only simple air cooling is coming on strong to push TTL out of the high-performance arena

by Bernard C. Cole

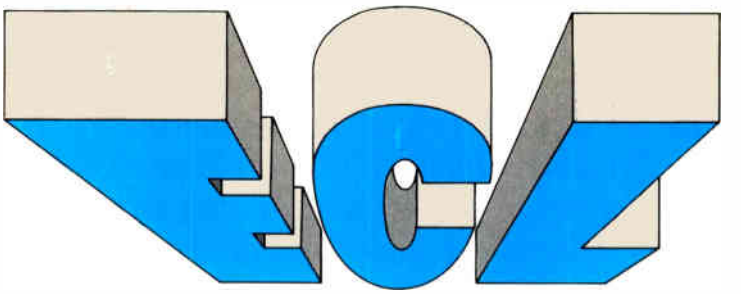
Like a giant steamroller, CMOS in recent years has slowly but steadily squeezed bipolar parts out of more and more system designs. To some people, it was only going to be a matter of time before bipolar logic lost out completely as CMOS chips got faster and faster. But a new generation of high-performance emitter-coupled logic is on the way from a growing number of chip makers around the world. And these parts should be able to fend off the CMOS push into the high-performance end of the logic market.

ECL, which has been on the fringes of mainstream markets for decades, is finally beginning to lose its image as a power-hogging, difficult design and may be starting to hit the big time. The new ECL chips will be able to make their move to the mainstream, because they are denser and faster than ever, yet they run cooler than ever before. Long considered too hot to handle, ECL is now learning how to keep its cool at high densities without the need for expensive, exotic liquid cooling. This is big news for minicomputer makers, because they need more and more speed to survive against the ever-faster, 32-bit microprocessor-based systems. And they have to get this performance with simple air-cooled designs, not with liquid-cooled kluges.

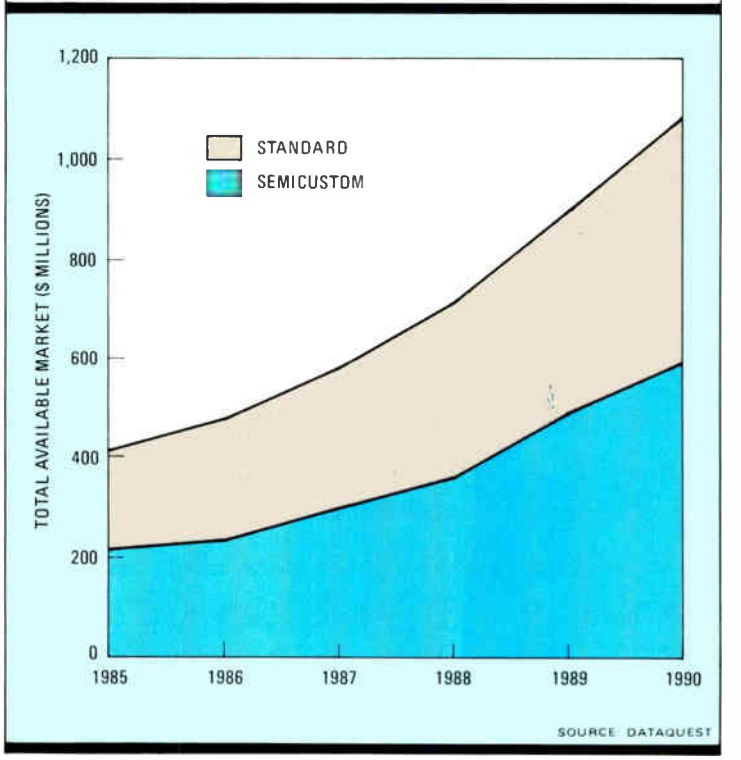
New ECL chips with 12,000 gates or more are now overcoming this problem and opening the door to a new generation of cost-effective superminicomputers—air-cooled number crunchers that can run as fast as 30 million instructions per second (see p. 71). This trend to greater ECL density promises to be a long-running one: one Honeywell array due out in mid-1988 will have a staggering 100,000 gates.

One of the companies gambling plenty on ECL hitting the big time is Fairchild Semiconductor Corp. (see p. 77). Its new high-density, standard-cell ECL line is leading the way, crowding an unprecedented 20,000 gates on a chip (see p. 74). Few ECL building-block families have been seen so far, and those that have surfaced top out at around 2,000 gates. None of them delivers the design flexibility of the coming standard ECL cells. The new ECL is far more easier for designers to work with than such logic used to be. Besides the strides being made in cooling requirements, denser packages such as Fairchild's cut interconnect needs, easing the noise problem.

The new ECL VLSI will not be able to reverse



WORLDWIDE ECL LOGIC MARKET TAKES OFF



HOW GATE-ARRAY PROCESSES STACK UP

Process technology	Price per gate (¢)	Speed (MHz)	Power (W)
CMOS	0.1 to 0.5	10 to 100	0.01 to 0.1
TTL	2 to 5	30 to 150	0.1 to 1.5
ECL	3 to 6	100 to 250	2 to 10

SOURCE DATAQUEST

the overall trend to CMOS, though. ECL still can't compete with CMOS in ease of design or cost. So CMOS, not ECL, is supplanting TTL at the low and medium levels of the logic spectrum. While CMOS logic families speed up and ECL parts get denser and faster, TTL seems to have run out of steam. There doesn't seem to be any more process or circuit tricks coming to wring out any more time delay. Also, the lower logic-level swings of ECL are inherently faster than the full-on, full-off logic levels of TTL.

Bipolar's share of the total IC market has been steadily shrinking. Bipolar shipments will slip from 44% of the market in 1985 down to 35% in 1990. Most of this loss will come from CMOS inroads into the market for standard bipolar logic families such as TTL, says Andrew Prophet, senior industry analyst at Dataquest Inc. in San Jose, Calif. "At the high end of the bipolar performance range, ECL has been holding its own, and indeed, as a result of improvements in density and power, gaining market share from the slower TTL portion of the market," he points out.

The technology behind ECL's drive for sockets comes mainly from MOS processing, and the result is the best of two worlds: higher speed, yet lower power consumption

Sales of ECL standard logic families are expected to rise from $406 million in 1988 to $461 million in 1990. But the hot action will be in ECL gate arrays, which should shoot up from $697 million in 1988 to $1.1 billion in 1990 (see graph, p. 67). "By the beginning of the 1990s, ECL standard cells should be a major factor, displacing most ECL gate arrays in market share," says Prophet. Indeed, the impressive improvement in densities that seems to be possible with standard cells should make the non-standard-logic portion of the bipolar market grow much faster than currently projected, he says.

The ECL story overseas will run along the same lines. The ECL market in Japan should hit more than $540 million annually by next year, up from about $468 million this year, predicts Toshihide Araki, an assistant manager at Hitachi Ltd.'s World Wide Marketing Operations, Semiconductor & Integrated Circuits Division.

Spurred mainly by the large computer-applications market segment, process engineers have borrowed techniques mainly from MOS technology to decrease bipolar transistor size significantly and increase density. They use such techniques as self-aligned device structures, ion implantation, polysilicon emitters, deep groove isolation, and the elimination of parasitic transistor junctions, as well as the use of multiple interconnect levels to improve routability.

"The small device areas and shallow junctions result in very fast transistor speeds," says George Wilson, president of Bipolar Integrated Technology Inc., in Beaverton, Ore. "Moreover, the speed improvement is not gained at the cost of increased current. Indeed, current is actually reduced, because of the smaller transistor size. And this, of course, translates into lower power—from hundreds of milliwatts per gate to a few tens of microwatts or milliwatts."

This means the transistor can switch very quickly with very low power requirements. For example, with Bipolar Integrated Technology's proprietary BIT1 bipolar ECL process [*Electronics*, April 7, 1986, p. 35], the cutoff frequency is greater than 5 GHz at 50 μA, and the junction capacitances are on the order of only 5 femtofarads. By comparison, Wilson says, conventional bipolar transistors would exhibit cutoff frequencies of about 3 GHz at 2,000 μA and junction capacitances 10 times greater.

The computer systems market sector is quite sensitive to power consumption. Surprisingly, on a per-gate basis, the speed-power product of ECL is very close to that of CMOS, says Neil Edmundson, ECL product planning manager at Fairchild Semiconductor Corp. in South Portland, Maine. "However, ECL is always on, always drawing power, while CMOS draws power only when it is actually switching," he says. Thus CMOS, even at VLSI densities, dissipates less than 1W per chip. By comparison, roughly comparable densities of ECL made with older bipolar processes dissipate 10 to 30 W per chip, requiring sophisticated and expensive liquid cooling at the systems level. But with the new improvements in process technology, ECL power consumption has been cut to about 5 to 15 W per package (see table, above). "Although this is still orders of magnitude greater than CMOS, it opens up the possibility of using less expensive air cooling," Edmundson says.

With a substantial portion of the power barrier removed, designers can appreciate anew the significant advantages of ECL over TTL and even CMOS. For one thing, it is much more flexible than CMOS, with five different ways of getting multiple levels of gating with essentially one level of propagation delay, says Alan Bass, ECL

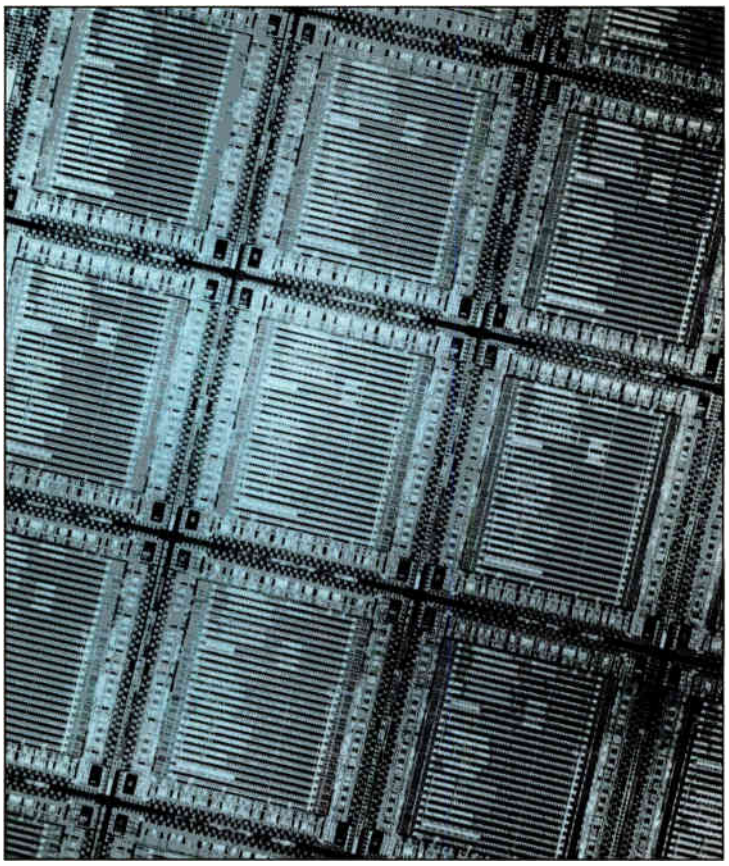
design manager at Texas Instruments Inc., Dallas. In addition to series gating, wire-ORing, and wire-ANDing, it is possible to take advantage of the differential nature of ECL and use both a signal and its complement as device outputs. By comparison, CMOS requires at least one other level of delay—an inverter—to obtain a complement. A fifth technique available to ECL circuit designers is the ability to parallel input transistors to create the OR/NOR function with very little additional delay. In CMOS, by contrast, the AND-OR-invert is the only class of structure that allows multiple levels of gating to be combined into fewer levels of delay, says Bipolar Integrated Technology's Wilson.

It should come as no surprise, then, that systems designers are taking a new look at ECL as a way to boost the performance of their systems while decreasing overall power requirements. The result has been a flowering of new offerings. Responding to the market demands, bipolar manufacturers are quickly moving into production with the first generation of high-density ECL arrays of 8,000 to 12,000 gates. In large part they are targeted for the fastest-growing portion of the systems market: mainframes, superminis, and minis. According to Prophet, superminis alone are expected to grow at about 30% per year through the early 1990s. Moving into this market segment are Motorola, Honeywell, Raytheon, Fairchild, TI, and several Japanese firms.

One of the first to market with a family of ECL gate arrays was Motorola Inc. Its 10,000-gate MCA10000ECL [*Electronics*, Feb. 19, 1987, p. 71] exhibits gate delays as low as 150 ps and dissipates a mere 1 mW per gate. Fabricated with Motorola's third-generation 2-μm Mosaic polyelectrode-transistor-based bipolar process, it features three levels of interconnect and three-level series gating. Engineers can select from a wide range of speed and power alternatives, from 10 to 30 W. At 3 mA per gate, worst-case delay is 120 ps; at 0.7 mA, delay is 150 ps. The array is available with any of three supply voltages, and each cell comes in either of two speed/power ranges. Also, designers can modify the emitter-follower and current-source structures to conform to one of two additional speed/power ranges.

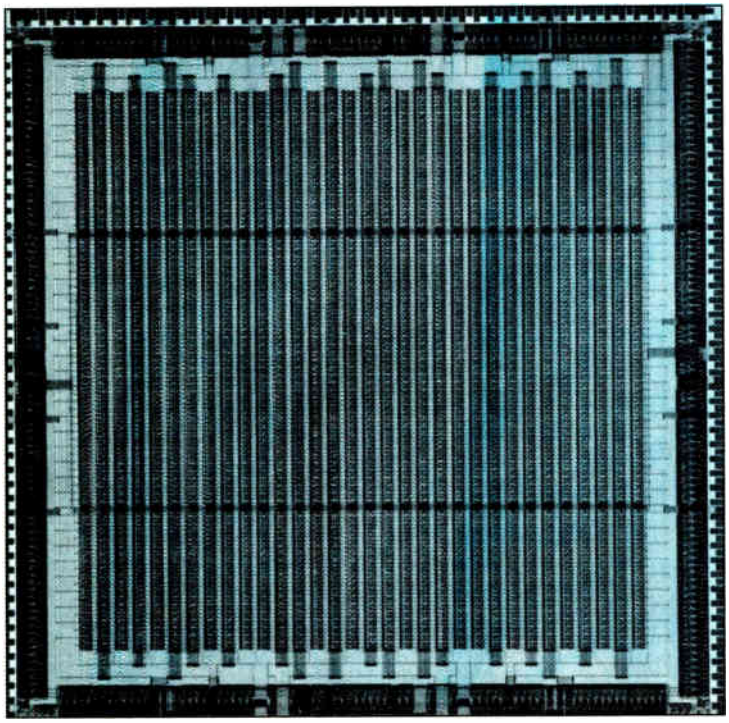
Following closely on the heels of the Motorola introduction, Honeywell's 12,000-gate array is a lower-power ECL variant called current-mode logic. Fabricated using the company's third-generation 1.25-μm advanced digital bipolar process, the HE12000 features 150 ps gate delays and power dissipation of 1.3 mW per gate.

One of the more recent newcomers to the high-performance ECL array market is Raytheon Corp.'s Semiconductor Division in Mountain View, Calif., which entered the fray on June 20th with two high-density arrays: the 12,540-gate 70E18 and the 8,000-gate 40E12. The new arrays are an outgrowth of an agreement between Raytheon and Bipolar Integrated Technology, giving the former access to the same BIT1 process used by the latter to fabricate a high-performance family of computer-system building blocks (see fig. 1). The BIT1 process yields transistors no bigger than 20 μm square, resulting in a chip size of only 336 by 364 mils for the 12,540-gate array and 270 by 290 mils for the 8,000-gate array—unusually small for arrays of such density. Typical gate delay is 300 ps, and each gate consumes only 300 μW with 90 μA of switching current. For the larger chip, the CGA70E18, this results in a total power dissipation of only 5 W with 5,000 equivalent gates and 60 outputs. To give users a range of power-dissipation choices, the arrays incorporate four programmable drive options: 90 μA, 180 μA, 360 μA, and an extremely low-power, high-drive fanout, wired-OR option in which 16 outputs share a 360-μA switching current.



1. HIGH-DENSITY ECL. Tiny transistors enable Raytheon to cram 8,000 gates into an area only 270 by 290 mils.

Fairchild Semiconductor has developed a two-pronged approach to the mini and supermini segment of the market, based on both gate arrays and standard cells. On the gate-array side, in April the company launched the Aspect 12-K [*Electronics*, Sept. 4, 1986, p. 55], a 12,269-equivalent-gate contender (see fig. 2). Fabricated with the company's 2-μm single-polysilicon emitter-coupled technology in three levels of interconnect, Aspect features two power modes. In the lower-power mode, each transistor draws a switching current of 150 μA to achieve a gate



2. MODE SELECTION. Fairchild Semiconductor's Aspect gate array features a choice of speed and power.

delay of 200 ps. In the higher-power mode, the gate delay drops to 120 ps, but current climbs to 300 μA. Here, typical chip power dissipation is 18 W with 85% gate utilization and 150 inputs and 150 outputs. To achieve even higher densities and speeds, yet hold down power dissipation, Fairchild is developing a standard-cell-based family of building blocks aimed at minis and superminis that will keep dissipation to 5 to 15 W at densities of up to 20,000 gates.

Due out soon from TI is a family of bipolar gate arrays produced with the company's new ECL process technology, ExCL [*Electronics*, March 19, 1987, p. 73]. ExCL combines polysilicon-filled trenches, to isolate transistors, with silicide polysilicon base-contact layers that reduce base resistance and polysilicon emitters that enhance the gain-bandwidth product and thus boost switching speed. The first device in the family is the TGE8000, which contains the equivalent of 8,584 gates. Starting with gate delays of 200 ps and power dissipation of 400 μW, typical dissipation at the chip level ends up between 4 and 11 W, depending on gate utilization and the speed, power, and power-supply options chosen.

The high-density market is not the only one being pursued by the makers of the new ECL generation. Most of them, including Motorola, Honeywell, Advanced Micro Circuits, and Advanced Micro Devices, also plan lower-density versions with even better speed/power tradeoffs. Motorola has developed the 7,000-gate MCA7000ECL, which it will introduce later this year, for air-cooled applications with about the same speeds as the higher-density version, but with power dissipation ranging from 10 to 15 W. Also in the works is the MCA7500RAM, a 7,500-gate array with 4 Kbits of on-chip random-access memory. Another part, the MCA1500ECL, is a 1,500-gate array characterized by 120-ps delays and chip power dissipation ranging from 3 to 6 W.

Surprisingly, Japanese firms have not been as aggressive in pushing the new generation of ECL on the open market; their densest new chips are largely for in-house needs. Most of their commercial efforts have been confined to densities below 5,000 and 10,000 gates. Fujitsu, for example, has been selling ECL gate arrays in the open market for only two years, even though it has made them for more than 10 years. So far, Fujitsu's only external sales have been to Amdahl and Cray. It has a line of four parts, with propagation delays of 0.8 ns and 1,500 to 4,000 gates. One nice feature is that the input and output gates can be either ECL or TTL, in any combination. Fujitsu also has two devices with built-in RAM: one with 1,920 gates and four 256-bit by 9-bit RAM areas, and the other with 2,880 gates and two 256-bit by 9-bit storage areas.

In Europe, Siemens AG, of Munich, West Germany, has a 9,000-gate master slice array based on current-mode logic and featuring a 150-ps gate delay and a power dissipation of 1.33 μW per gate. The array, aimed primarily at minis and superminis, uses an oxide-isolated process with self-aligned polysilicon emitter and base structures and polysilicon resistors with low capacitive loads. It also has three layers of interconnect, employing an alloy of aluminum, silicon, and tungsten that is isolated by an organic/inorganic layer with a low dielectric constant.

Another company participating in the ECL gate array market at the lower-density end of the spectrum is Plessey Semiconductor of Irvine, Calif., with a family of 1,000- to 4,500-gate arrays.

Many companies will be pushing the high frontiers of ECL density and performance, and next year will see a number of new higher-density parts. Motorola, for example, is working on a 1-μm enhancement of its Mosaic process, one with four levels of interconnect. It is expected to yield a 20,000-gate ECL array with gate delays of only 50 ps. Fairchild, TI, and Honeywell are also planning similar devices.

ECL technologists are far from finished. It appears that bipolar structures can be scaled down even further—to submicron levels—without many of the second-order and hot-electron effects that plague submicron CMOS VLSI circuits [*Electronics*, April 7, 1986, p. 24]. TI, Fairchild, and Motorola are working on gate arrays and standard-cell-based circuits in the 50,000- to 80,000-gate range. Stretching even more, Honeywell is planning an array with four levels of interconnect that pushes a staggering 100,000 gates. Due for a mid-1988 debut, this behemoth will take advantage of a fourth-generation slot-isolated process that uses half-micron design rules. □

HOW AIR-COOLED ECL VLSI MAY SAVE THE MINICOMPUTER

New ECL parts that are faster, denser, and run cooler should help minicomputers stay ahead of the 32-bit microcomputers that are pushing into their territory

by Tom Manuel and Larry Curran

Minicomputer makers are under fierce competitive pressure to push their systems to ever higher levels of performance, as new, cost-effective microcomputers based on high-performance 32-bit microprocessors close in fast on their traditional territory. New emitter-coupled logic circuits may allow minicomputers to spurt out in front of their rivals and move ahead of the micros. The minicomputer makers are now focusing their design efforts on these advanced ECL technologies—but only, they agree, so long as they can continue to be air-cooled.

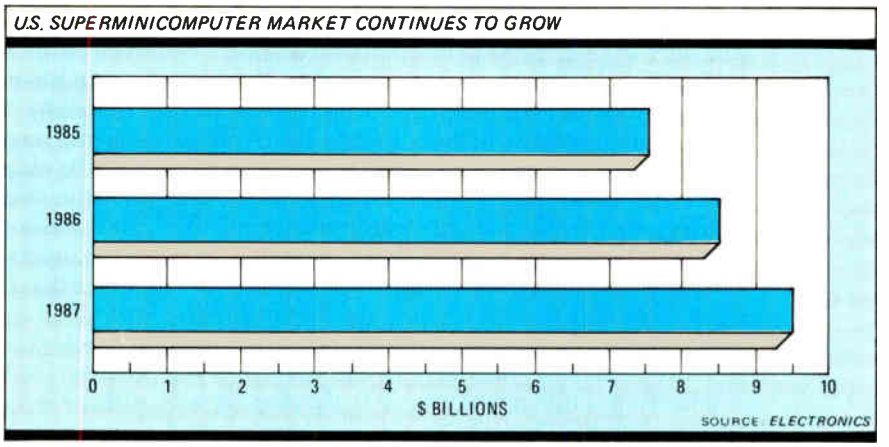
What makes the ECL circuits on the horizon (see p. 67) so important to minicomputer designers is their increasing density, their flexibility for easier design and customization, and—very critical to minicomputers—the fact that they can run cooler than today's highest-performance ECL, yet retain their speed.

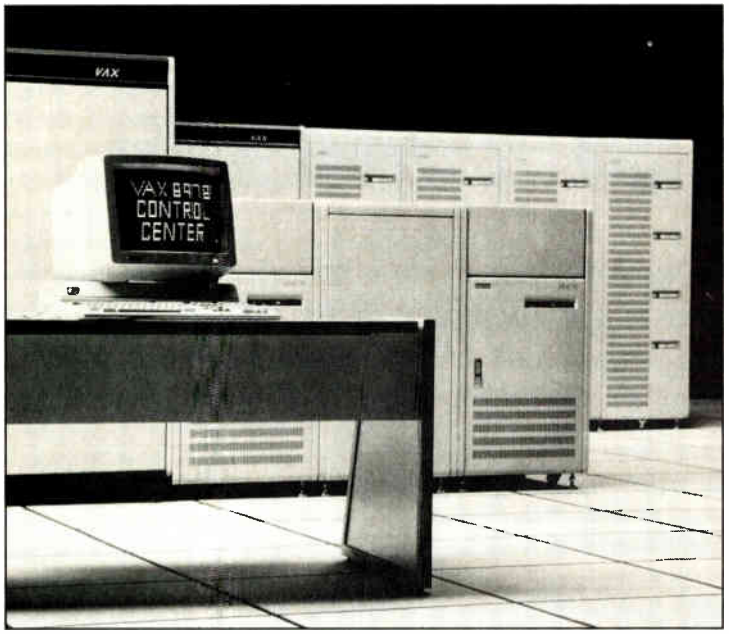
Because of the nature of the minicomputer market, two seemingly easy ways to pick up speed are ruled out. Drastic architectural changes would make the computers incompatible with the large existing software base. And the fastest state-of-the-art circuit technologies and the liquid-cooling systems that often accompany them would price minicomputers out of their market.

Just a few years ago, the minis were gaining on mainframes when they moved up in performance to 5 to 10 million instructions per second. At that time mainframe makers responded by hiking mainframe performance from a few mips to tens of mips; the top machines sprinted into the 50-to-100-mips range. Now, minicomputer designers must follow the same strategy, because microcomputers are moving into the 5-to-10-mips range. To survive, minis have to move into the 15-to-30-mips range.

Most minis now are members of 32-bit system families that span broad performance ranges. They are generally referred to as superminicomputers, and the low-end models of each family—in concert with new supermicrocomputers from a host of new competitors—have all but replaced the traditional 8-bit and 16-bit minis.

The market segment held by the superminis is big and still growing: U. S. sales should approach $10 billion this year (see graph), according to *Electronics'* 1987 Market





2. COOL RUNNING. Air-cooled ECL in DEC's VAX 8978 multiple-processor system helps this supermini run faster than 10 mips.

Forecast [*Electronics*, Jan. 8, 1987, p. 54]. The supermini sector's growth rate for 1986 was 12%, and it's projected to hit 13.5% this year.

Designers of supermini families are keenly watching developments in ECL and CMOS circuit technologies for use in the next generation of their products to push performance well ahead of the encroaching supermicros. They currently give the edge to air-cooled ECL by a wide majority. However, next-generation machines will most likely be made of a mixture of circuit technologies, using the fastest practical technology, ECL, in the highest level of a hierarchical structure. Lower levels that can run slower will probably use a lot of CMOS VLSI and some TTL to achieve the best price-performance balance.

Future machines will most likely use air-cooled ECL for the highest and fastest hierarchical levels, with CMOS VLSI and some TTL chips at the lower levels

Although ECL does require considerably more power and thus dissipates much more heat than CMOS, liquid cooling may no longer be required, except at the peak speed range. High-performance ICs made of ECL technologies with manageable power and cooling requirements are becoming available with ever higher densities; they will push TTL out of the high-performance end of the market and will give CMOS VLSI a run for the money for many years. Fairchild Semiconductor Corp., for example, makes a strong case that the standard-cell building blocks it is developing using its advanced Aspect ECL process can be used in high-performance computers that will be air-cooled (see p. 74).

Air cooling is a prime requirement for superminis to compete at their current price levels. The major minicomputer companies began switching to ECL a few years ago for their top machines, which are all air-cooled. Digital Equipment Corp., for example, the market leader with about 40% of the market, switched to ECL technology in late 1984 for launching its 8000-series VAX systems (see fig. 1). DEC declines to comment on its technology for future products.

Data General Corp. also uses ECL in its high-end systems and expects to use it in the next generation as well. Donald Lewine, a senior technical consultant at the Westboro, Mass., company, says that while CMOS may stamp out ECL in six or seven years for high-end superminis, "there will be another generation of systems in which ECL is the most cost-effective choice." He points to "very exciting" ECL developments that promise to deliver tens of thousands of gates on a chip that will operate in the low hundreds of picoseconds. "We're looking at densities in the 40,000-gate range with speeds down to 100 ps. No one has seen silicon on these kinds of parts, but we're working with vendors to help them debug their processes." He wouldn't identify the developers.

Gould Inc.'s computer division currently is staking its future on ECL gate arrays and will start looking at standard-cell arrays right away. "We believe that ECL gate arrays will be the preferred technology for the next few years—for five years, anyway, over a couple of generations of machines," says Bill Ward, vice president of development for Gould in San Diego, Calif.

All of Gould's current machines are air-cooled, and the company plans to keep designing systems that way. "With improvements in heat sinks and the speed-power product in the newer ECL circuits, we believe we can use air cooling for the foreseeable future. Although ECL still has higher power levels than MOS technologies, it's at acceptable and manageable levels," says Ward. In keeping tabs on what ECL circuit makers are doing, Gould is evaluating when it will be advantageous to switch from gate arrays to standard-cell parts, such as the new Fairchild family. Ward says standard cells could come into vogue in the next few years.

Another supermini maker, the Computer Systems Div. of Harris Corp, Fort Lauderdale, Fla., having used ECL in its H1000 and H1200 models, is planning to move its Unix-based product line to that technology. Rick Maule, director of product marketing, says "our HCX-7 and HCX-9 Unix-based systems, which now employ fast Schottky TTL in their CPUs, will soon be switched to 100-K ECL."

However, Maule expects to see some very dense CMOS gate arrays and semicustom ICs in Harris's CPUs in the next two or three years. "CMOS is moving into a new era in switching

speeds. It will rival ECL, perhaps in the next year, in getting into the low hundreds of nanoseconds in gate delays." He cautions, though, that the usual power conservation associated with CMOS "won't be there with such fast switching, because the duty cycle—the percentage of time the logic is active—will increase to the point where power consumption will rival that of fast ECL."

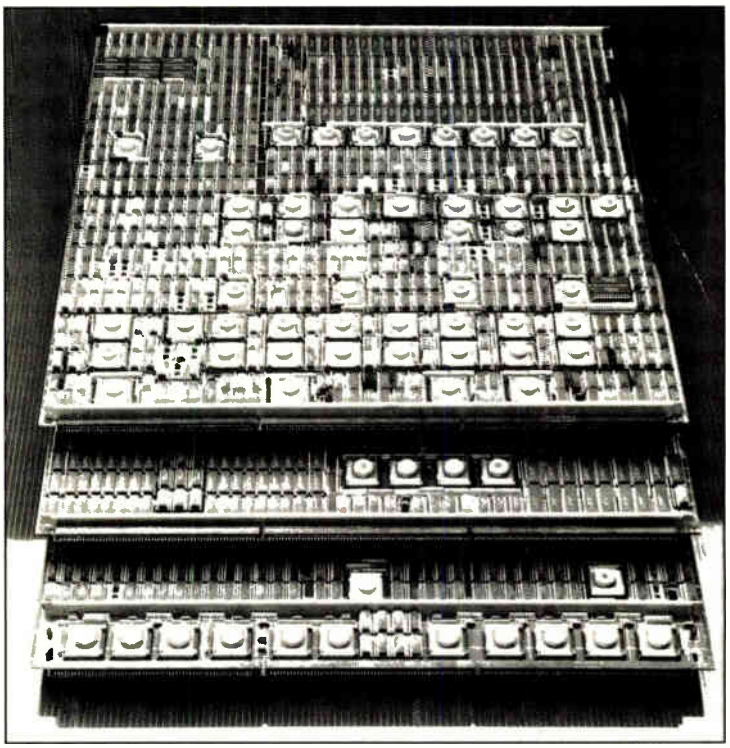
Vendors' chief designers tend to wrestle with the tradeoffs between ECL and VLSI CMOS as advances in both technologies keep them in the running. "But ECL has a real edge [in speed], even though CMOS is moving along," says Len Shar, vice president of development at Elxsi. The San Jose, Calif., maker of high-performance 64-bit multiprocessor systems uses medium-density ECL gate arrays for its CPU circuitry (see fig. 2) and plans to move gradually up to higher-density chips as they prove viable.

One relatively new but prominent player in the high-end supermini market—a segment that is often called minisupercomputers—started out in the CMOS camp but is now eyeing the new ECL parts. Convex Computer Corp., the firm that brought the industry's first 64-bit vector minisuper to market, uses high-density CMOS gate arrays in key parts of its C1 computer line. But now the Dallas firm is evaluating ECL parts, says Frank Marshall, vice president of development. "High-density ECL gate arrays are an attractive device, as long as systems using them can be air-cooled. Convex must build air-cooled systems, and I believe we can still build them with ECL circuits containing thousands of gates."

The computer designers at Hewlett-Packard Co. believe that their future low- and mid-range system designs will be based on CMOS technology. But HP will use ECL for its highest-performance systems. "CMOS technologies will continue to improve and move up, meaning that the lower- and mid-range systems will move up in performance," says Lance Mills, general manager of the entry-systems operation in HP's Information Technology Group in Cupertino, Calif. To stay ahead of these systems, the highest-performance products will have to be built with faster circuit technologies, which today and for at least the next five years probably means ECL.

Mills believes that the two dominant technologies by the 1990s will be CMOS and ECL. The trends he sees in ECL are toward the use of higher-density gate arrays, rather than full-custom designs. He sees a future in ECL standard cells too. HP is looking at both ECL gate arrays and standard cells now and expects it will make sense to use a mix of them in any given design.

One supermini maker that has not yet made the switch to ECL is Concurrent Computer Corp., Tinton Falls, N.J. All of its current parallel-processing computers are TTL-based. But Bill Hudson, director of hardware development, says "we are moving to gate arrays that are ECL internally and have TTL signals for the external interface. For the next level of performance [after that], we will have to go all the way to ECL."



3. ECL ALL THE WAY. Processor boards in the Elxsi 6400 64-bit minisupercomputer are loaded with ECL circuits.

A company not planning to hitch a ride on the ECL bandwagon is long-time minicomputer vendor Texas Instruments Inc. The Dallas-based company has chosen to move from proprietary custom processors to standard microprocessors in its multiuser midrange computers, joining the camp of microcomputer vendors nipping at the heels of the traditional minicomputer companies. "We probably will not be making another drastic change in the next five years," says Jim Hartzog, TI's Computer System Division engineering manager.

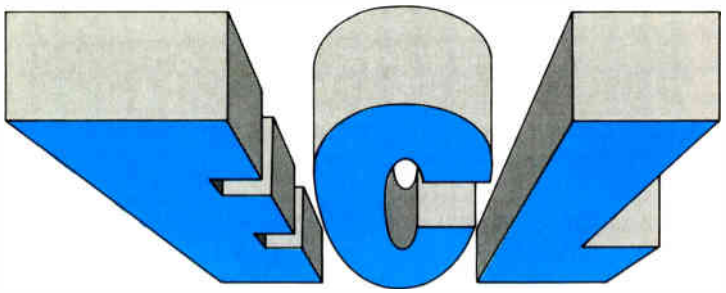
The clear trend is to mix circuit technologies in complex high-performance supermini designs, because that will yield the best cost-performance and lowest power-performance ratios. According to HP's Mills, "The CPU, cache structures, and mathematics circuitry will be ECL, while the main memories will continue to be CMOS. Most of the I/O structure will be conventional circuits. The big systems typically have a hierarchy of buses; the highest-level bus, the cache bus, will undoubtedly be ECL."

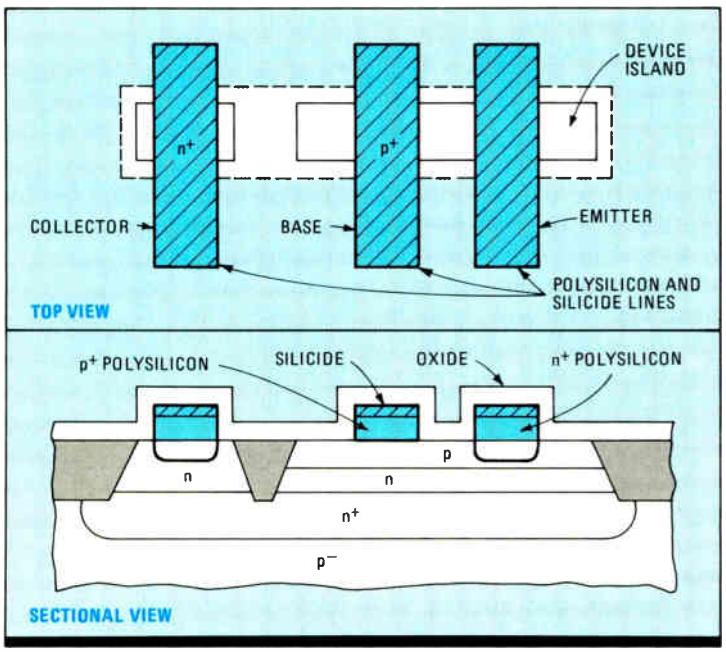
Following the trend, engineers at Gould do not build the whole machine out of ECL. They are using the latest 1-Mbit dynamic random-access memory chips and anticipate samples of 4-Mbit DRAMs later this year. They also use some MOS gate arrays and custom VLSI parts in some of the I/O areas. But for the performance-critical parts of the machines—processors, cache, and the system bus—it's ECL all the way. □

FAIRCHILD BETS ON ECL LINE BASED ON STANDARD CELLS

Targeted at superminicomputer designs, the VLSI family will be assembled from flexible building blocks that can be customized at all levels, crowding up to 20,000 gates on-chip

by Bernard C. Cole





1. ASPECT. Fairchild ECL data-path cells are built with its 2-μm advanced single polysilicon emitter-coupled logic.

Fairchild Semiconductor Corp. is taking the wraps off a flexible family of VLSI ECL standard-cell-based data-path elements that are targeted at the largest and fastest-growing portion of the bipolar marketplace—superminicomputers and high-end work stations (see p. 77).

The new family is assembled from a well-stocked library of standard cells built with the company's power-saving "contactless" single polysilicon process, which crowds an unprecedented 20,000 gates on-chip. Few ECL building-block families have been seen so far, and they top out at roughly 2,000 gates. None comes anywhere near this level of density, and none delivers the design flexibility of standard cells, which can be customized at all levels. The most important element in the library is the scannable register latch, or ratch, which can be set up to four modes, offering a greater design flexibility than gate arrays.

Fairchild plans to go public with the library in 1988. Already it has built a 16-by-16-bit multiplier designed with the standard cells. The device, called the F100610, will be available as a standard product later this year as well as being offered as a megacell in the library.

"It's clear that ECL will be the dominant bipolar logic family within the next decade," says Neil Edmundson, ECL product planning manager at the company's headquarters in Cupertino, Calif. "And it is also clear that minis and superminis will eat up much of what is produced."

Fairchild's candidate, its family of high-performance data-path building blocks, is fabricated with a modification of its 2-μm advanced single polysilicon emitter-coupled technology, or Aspect [*Electronics*, Sept. 4, 1986, p. 55]. A self-aligned bipolar process, it uses a single layer of polysilicon with proper doping to form the base, emitter, and collector contacts of the transistor (see fig. 1). The new approach boasts a power dissipation per gate of 1 mW, which is one fifth that of the company's last ECL approach, and it comes in with a power-delay product that is 1/50th of its predecessor's.

The library is a collection of high-performance ECL and current-mode-logic standard-height cells designed with an automated cell-analysis program. The mask designs, however, are laid out by hand to ensure that they are compact. Because the performance of LSI and VLSI circuits, both bipolar and CMOS, is affected more and more by the intrinsic gate delay and the capaci-

tive load of the interconnection, the cells are designed so the output drive of an ECL gate can be adjusted by changing the power in the emitter-follower. "Our methodology centers around this theme, in which the critical paths, the emitter-followers, can be extracted by higher-power versions based on the loading extracted after routing," Edmundson says.

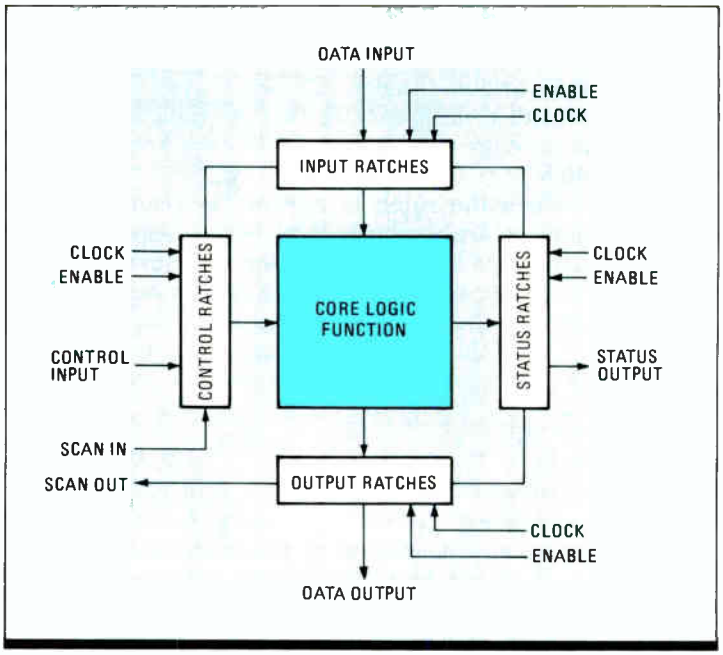
Separating the cells from the emitter-followers permits tailoring the power dissipation to the circuit requirements, he says. "For example, to drive a long line, a more powerful emitter-follower can be selected and added to the desired cells. If line driving is not a problem, lower-power emitters can be used. This way, the circuit designer has the ability to select and adjust power dissipation of each cell in the device."

The library of familiar small- and medium-scale integrated logic functions, as well as the novel register-latch combination, the ratch, combines flip flops, gates, exclusive-OR functions, adders, and such specialized functions as parity detection and generation to create a collection of megacell core functions. The library includes 32-bit arithmetic logic units, multipliers, accumulators, several multiplier-accumulators, floating-point units, and register files. These are matched up in data-path building blocks customized to a specific system.

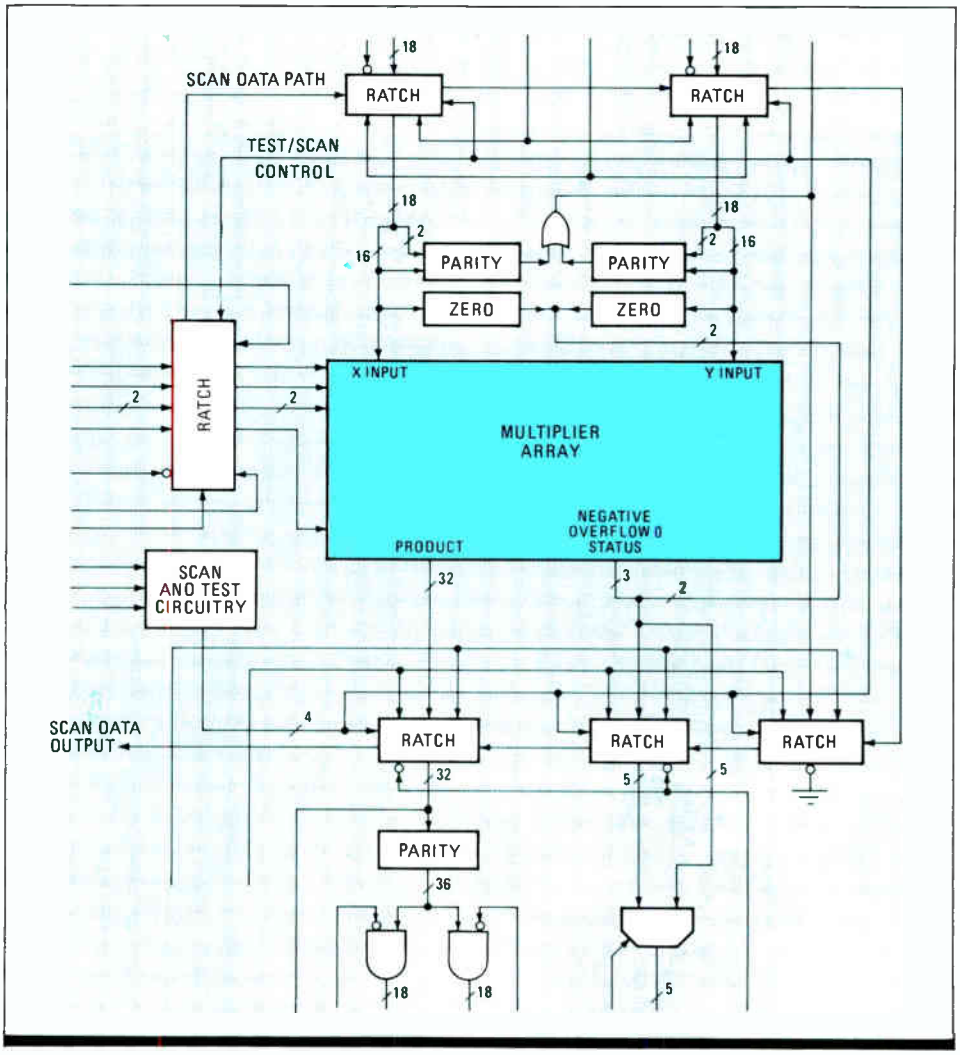
Edmundson believes designs based on VLSI building blocks of ECL-based standard-cell arrays will deliver the power and density needed to spawn the new generation of inexpensive superminis that will churn through 15 million to 30 million instructions per second (see p. 71). "At the same time, they will remain compatible with the vast body of available applications software," he says.

The cornerstone of the standard-cell library is Fairchild's scannable register latch. The building blocks owe much of their testability and flexibility to the ratch. To aid the designer, each ratch can be set with software to one of four modes: register, latch, flow-through, and scan. "The system designer has 70 different combinations he can use, delivering a degree of flexibility that no standard part or gate array can hope to offer," says Edmundson.

Adds Frank Reid, senior



2. AT THE CORE. All of the ECL standard-cell-based data-path building blocks combine a basic core function with storage elements.



3. 20,000 GATES. A multiplier is the first in a family of ECL standard-cell building blocks for superminis.

product planning engineer, "They also can be tailored to have separate control signals and separate clocks, or they can use a common clock and various enables. To boost system throughput, all a designer need do is configure a ratch as an edge-triggered register or a level-sensitive latch."

When the ratch is working in scan mode, its abilities truly shine. And when scan-path elements are added to a design, Edmundson says, "the state of every register can be detected and reset in the machine at any time."

"With this added capability, it is now possible for the designer to load in data to create a certain state within the machine that is controllable and which can be determined at any time," says Warren Snyder, architecture and logic-design manager. "Without this scan-path capability, an oscilloscope or a logic analyzer and several probes are needed to measure the same things, which is not easy in a 50-plus-MHz system."

Using the ratch in the scan mode solves two other problems facing supermini designers, Reid says. "Almost like a universal interface, the ratch can be used to isolate complex functions chip by chip, so that unneeded functions can be eliminated. Equally important, it makes it easy to do several versions of the same function to find ways to fine-tune the architecture."

As standard-cell elements, ratches may be used as interconnect buffers of various sorts—between two chips or between two core functions on the same chip. They will be optional on all standard-cell designs and will be incorporated into any megacells that Fairchild makes public. Each building block, says Edmundson, will consist of a core function (see fig. 2), which will be surrounded by ratches on all data input/output and instruction pins. Each will also include the control logic to initiate scan-path testing on the chip, board, and system level and will generate parity bits.

The first megacell from Fairchild's library is a 16-by-16-bit multiplier (see fig. 3) with a guaranteed fall-through time of 11 ns. Further, it typically takes only 4 ns for data to pass through the array. "The results have been so good that it is now being offered as an off-the-shelf multiplier," says Edmundson. Designated the F100610, the 240-by-260-mil device uses Aspect to dissipate just 6.5 W, well within the 15-W air-cooled limit that Fairchild sets for its ECL devices. And, thanks to its stock of ratches that can be set in-system with the device's control pins, the multiplier is fully testable.

Architecturally, the multiplier is unusual because it uses the Baugh-Wooley algorithm rather than the more commonly employed Booth encoding or modified Booth encoding with a Wallace tree, Edmundson says. The algorithm's principal advantage is that the signs of all partial products are positive, so no sign extension is necessary and the product can be formed using simple array addition.

In this approach, array addition is performed using a modified carry-save technique in which the array is set up as odd and even rows. The sum and carry generated by an odd row are used as the input to the next odd row. At the same time, the sum and carry of an even row are used as inputs for the next even row.

The result, according to Reid, is that two streams of numbers are processed in parallel to produce a product, "effectively halving the number of addition stages. Multiply time is further reduced by carry lookahead logic in the final summation of the partial products." □

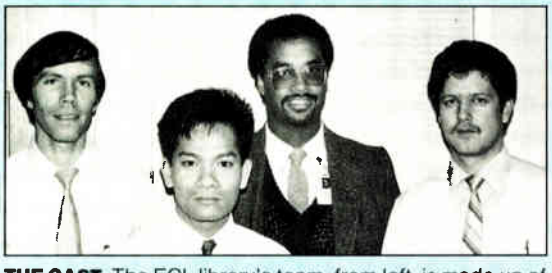
FIRST PRODUCT CAME FASTER THAN EXPECTED

To Fairchild's Warren Snyder, one of the most impressive aspects of his company's new emitter-coupled-logic VLSI standard-cell family has been the speed with which it went from concept to the introduction of the first product, the F100610 multiplier.

As manager of the architecture and logic-design group at Fairchild Semiconductor Corp.'s High Speed Logic Division in Puyallup, Wash., Snyder, 33, was also involved in earlier efforts to develop a 12,000-gate array (see p. 67). "Before very long, it became clear that to take full advantage of the high densities possible with our advanced single polysilicon emitter-coupled technology, a standard-cell methodology was the only route to go." Using comparable design rules, he says, standard-cell technology usually allows at least 50% to 100% improvements in density over gate arrays.

So in March 1986, an effort parallel to the gate-array development program was begun. The first step was the assignment of three key people to the project: 27-year-old Frank Reid as senior product-planning engineer, 30-year-old Scott Roberts as circuit-design manager, and 30-year-old Tuan Tran as senior staff design engineer. In addition to these three the standard-cell project also involved about 25 other Fairchild engineers and scientists, says Snyder.

The project also relied heavily on customer input. Potential customers in the minicomputer and superminicomputer community were inordinately enthusiastic about the project, says Reid, whose job was to seek technical input from customers about systems requirements and to ensure that the findings were reflected in the standard-cell data-path building blocks being developed. "The result was that the project moved ahead much faster than we expected," he says.



THE CAST. The ECL library's team, from left, is made up of Scott Roberts, Tuan Tran, Frank Reid, and Warren Snyder.

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FAIRCHILD'S HIGH-STAKES ECL STRATEGY

Fairchild Semiconductor Corp. is staking a lot on the future of emitter-coupled-logic technology. Ever since its founding, the company has supplied ECL circuits to makers of mainframes and supercomputers. Now, Fairchild is using a good bit of its currently limited corporate resources to bring a whole new thrust to its ECL strategy, developing and supporting a standard-cell approach that is targeted at minicomputer architectures.

Adding standard-cell parts to the standard parts and gate arrays already available means a new approach to ECL, extensive additional software support, and more engineering hand-holding. It also means the development of a broad family (see figure) of standard cells, both small cells and the larger cells that Fairchild calls building blocks (see p. 74). The family will help designers achieve the performance they need without resorting to expensive water-cooled circuitry, enabling them to stay one step ahead of the microprocessor-based systems that are nipping at their heels.

With a sharp eye on this growing ECL marketplace, Fairchild aims to carve out a substantial niche in minicomputer systems capable of 15 million to 30 million instructions per second. Such systems would outperform 32-bit microprocessors but should be considerably cheaper than mainframes.

The conventional name used for this type of high-performance system is the superminicomputer. But Fairchild's more functional description of its target market takes in all computers with 32-bit data paths and more than 1 Mbyte of main memory. Because work stations meet this definition, they too fall into the target market.

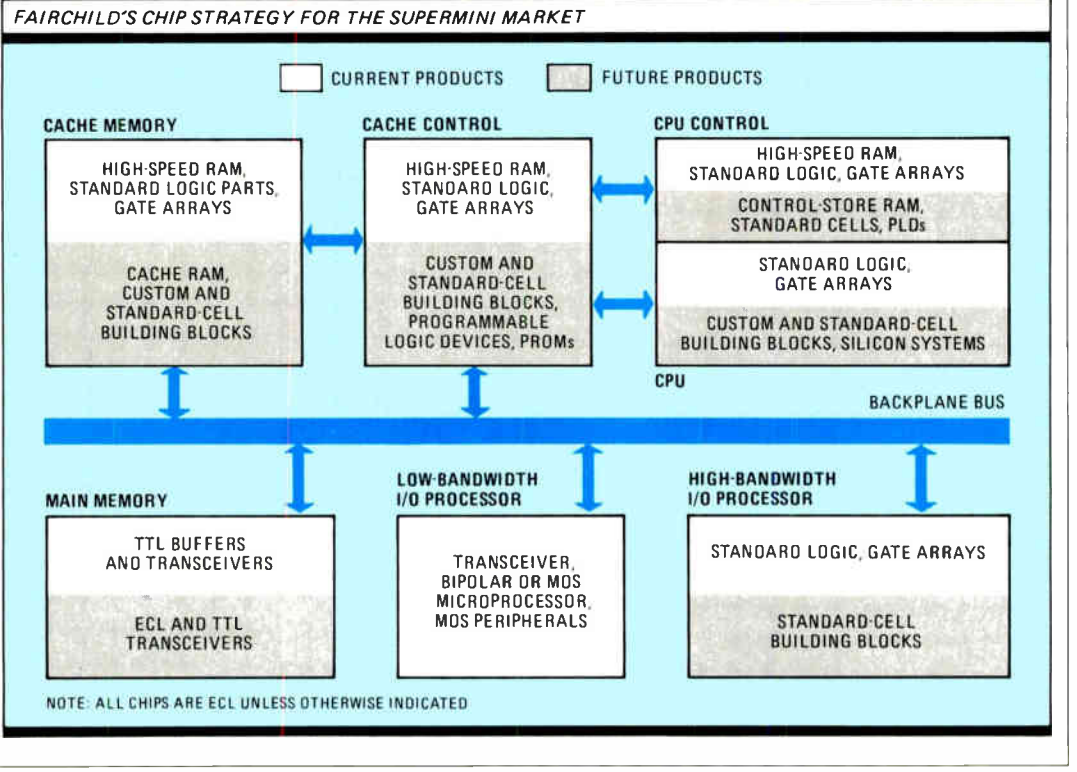
ECL offers an immediate boost in performance for systems houses—unlike parallel architectures, the other route to high performance, for which software must be developed—says Neal Edmundson, who helped shape the Fairchild strategy as product planning manager for ECL. "Virtually every supermini manufacturer either has for sale today or is preparing for sale tomorrow an ECL machine," he maintains.

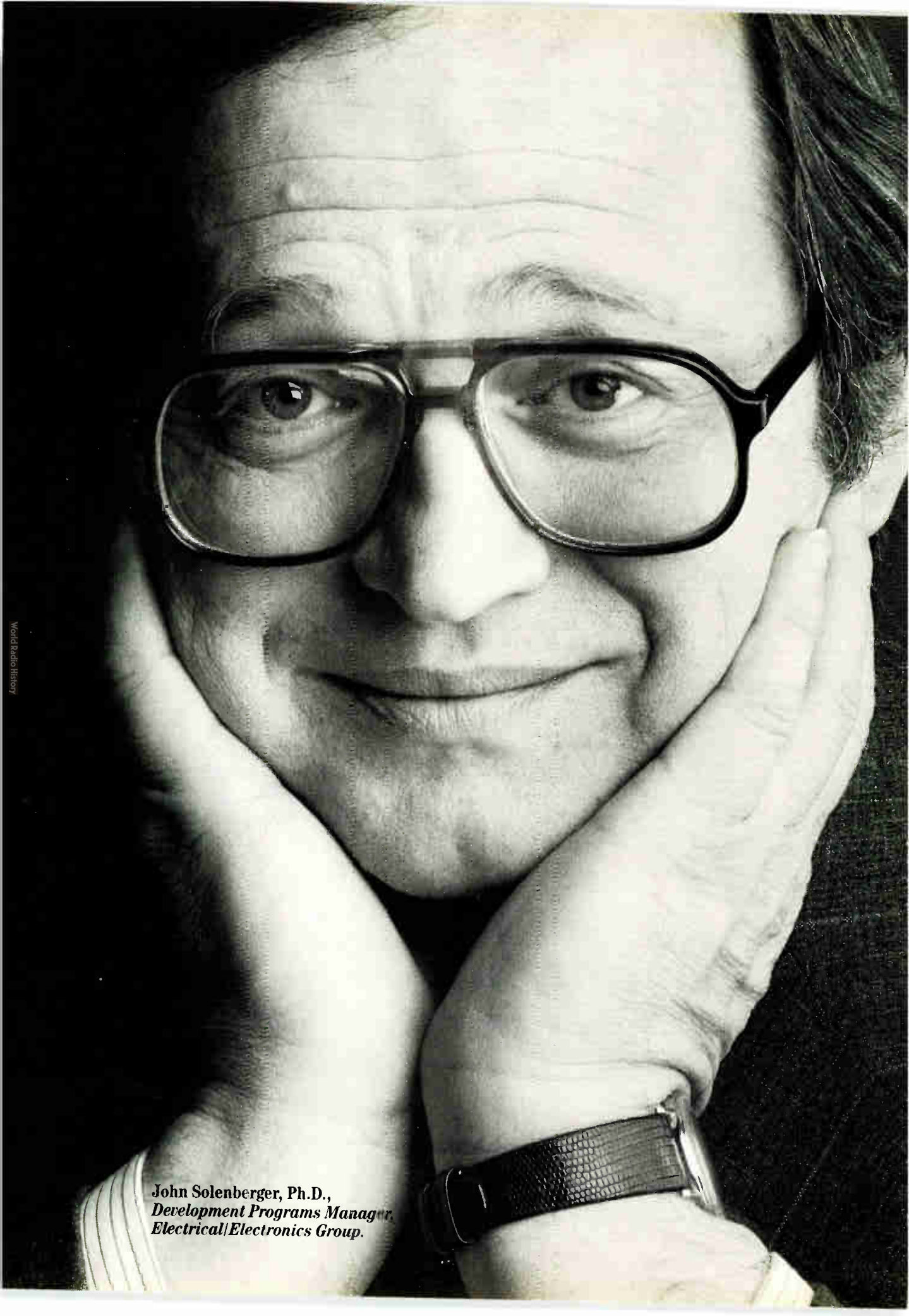
Because supermini designers are quite comfortable with the semicustom approach, Fairchild found that trying to provide them with standard products is frequently a waste of time, Edmundson says. So the company turned to standard cells.

The Fairchild cell library will include the functions of most well-known small- and medium-scale integrated circuits, as well as application-specific memories, such as caches, first-in, first-out circuits, and multiport random-access memories. Fairchild's first VLSI building block is a 16-by-16-bit multiplier; it is due out in the third quarter. To come later are a 16-bit arithmetic logic unit (cascadable to 32 and 64 bits), a 128-by-18-bit three-port register file, and a barrel shifter. These cells are designed to fit in Fairchild's model of the generic supermini, which has separate data and address paths, control circuitry, and memory management.

Standard cells deliver higher performance than the ECL gate arrays Fairchild already offers, says Edmundson. "Gate arrays do random logic well, but they do a marginal job on array logic or any logic that can be laid out in a space-efficient fashion," he says. To overcome the objections of customers who associate ECL with special water-cooling systems and difficult on-chip transmission-line characteristics, Fairchild offers assistance in air-cooling and chip design. "You really can air-cool most ECL devices, even in large, densely packed boards with up to 15- or 20-W/in.^{2} power densities," Edmundson says. *–Clifford Barney*

FAIRCHILD'S CHIP STRATEGY FOR THE SUPERMINI MARKET





John Solenberger, Ph.D.,
Development Programs Manager,
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STAYING HOME: HOW SOME U.S. PRODUCERS FIGHT BACK

Not all U.S. firms are playing dead or moving offshore; led by IBM, they are finding a vast array of new ways to battle foreign competition

by Tobias Naegele

When plant managers at IBM Corp. decided that visual wafer inspection done on their East Fishkill, N.Y., fabrication line was rapidly growing obsolete, they turned to the company's Research Division for help—a rare twist in a world where manufacturing and research people tend to steer clear of one another. The strategy worked. Today, three automated inspection units are doing the job it once took a small army of workers to do: operators peering through microscopes to make sure that solder bumps on chips were the right size.

More accurate and reliable than the people whose jobs they replaced, these machines and others like them should help IBM stay competitive. More important, the move illustrates the growing lengths that U.S. electronics manufacturers are taking these days as they strive to be more competitive with overseas producers. Rather than simply watch their rising costs push production lines off-shore, a growing number of U.S. firms are turning to a vast array of differing strategies to automate their factories.

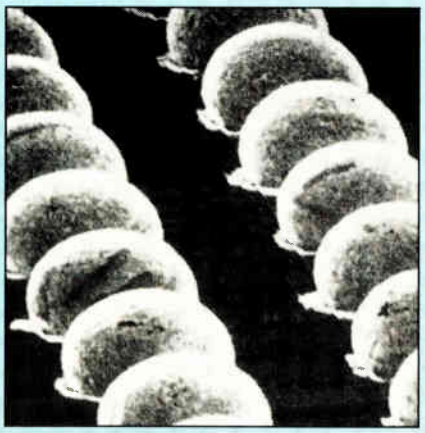
U.S. electronics manufacturers are facing more pressure than ever from low-cost overseas competition. New rivals show up almost by the hour, many from the Pacific Rim: Korea and Taiwan are taking dead aim on the U.S. market for components, computers, and other equipment, forcing some U.S. manufacturers offshore. The American Electronics Association estimates that in the past nine months alone, the U.S. has lost 60,000 electronics manufacturing jobs to off-shore operations. But, led by the likes of IBM, many companies are fighting back to make their factories more efficient, flexible, and

WHY MEASURING SHADOWS KEEPS IBM COMPETITIVE

Inspectors had no problem seeing if the tiny solder bumps on the backs of the chips were the right size when IBM Corp. first developed its controlled collapsible chip-connection (C-4) system for use in its mainframe computers. Most defects could be readily detected through a microscope. But the job kept getting harder—a single chip can now have up to 289 input/output pads rising less than 1 μm from its surface. Eventually, IBM had to move to an alternative to visual inspection—an automated inspection system developed by its Manufacturing Research Group.

Using a custom-made oblique microscope and a highly focused beam of light, the system measures the volume of each solder bump by analyzing the shadow it casts. If a shadow is too small or too large, the device fails the inspection.

The C-4 process leaves little room for error. The pads are designed to melt when heated, bonding the chip to a module that carries as many as 100 ICs. If a pad is too large, the solder can overflow into other pads, causing short circuits; if it's too small, an open can occur. In the worst case, says Charles Kelly, manager of semiconductor test and finishing at East Fishkill, the pad is just large enough to form a weak initial connection that degrades over time and eventually fails.



SOLDER BUMPS. I/O pads on IBM chips are now too small for visual inspection.

Such flaws are nearly impossible to detect visually. "The defects we're looking for are the same size and complexity as looking for a four-leaf clover on a football field," says Thomas DiStefano, manager of measurement science and technology, and a key force behind the inspection system. "You're out to do what it would take 100 or 1,000 people to do."

And even if 1,000 people could be employed for the task, Kelly says, "we're talking about a defect that's particularly difficult to specify. Visual inspection is subjective. You could get different results from person to person."

"Now we have better than 99% efficiency," says James King, the dice/pick engineering manager at East Fishkill. King is now preparing to move the technology into IBM's other chip plants. When all the wrinkles are ironed out, "carbon copies" of the inspection systems will be introduced at IBM's plants in Essones, France; Burlington, Vt.; Manassas, Va.; and Yasu, Japan.

-T.S.N.

cost-effective. They maintain that it is indeed possible to be competitive and remain a domestic manufacturer.

IBM, for example, has tapped its powerful Research Division to develop manufacturing techniques that cut labor costs and improve plant efficiency. Northern Telecom Inc. automated assembly yet shifted much of the responsibility for quality control to its component suppliers. Zenith Corp. is focusing on designing new products for simplified manufacture and servicing.

No matter how diverse the strategies and techniques may sound, all are joined by a single thread. To compete in the hotly competitive, worldwide electronics industry, U. S. producers acknowledge they must pare down labor costs—where off-shore factories enjoy their most obvious advantages—and drive quality and reliability as high as possible.

Automation is the key to both, and no company has embraced automation more fervently than IBM. Faced with pressure from Japanese competitors who used IBM technology to produce such low-cost goods as computer printers, the company set out to head the Japanese off at the pass. In the late 1970s, it pledged to become the lowest-cost producer of computer and related equipment in the world.

No one is saying that IBM has reached its goal, but the company has already surprised many with its highly automated domestic plants. Key to IBM's success thus far has been its Manufacturing Research Group, a team of 220 top-level researchers and technicians whose mandate is to develop new and better techniques for manufacturing. Based at the Thomas J. Watson Research Center in Yorktown Heights, N. Y., the group has worked its way into virtually every IBM plant. Its strategy is to apply the company's best minds to what are often described as its biggest problems—those having to do with making products quickly, cheaply, and reliably.

Although not exactly a novel idea—AT&T Co.'s Western Electric Research Center, now known as the Research and Technology Laboratories, has had a similar charter for many years—the approach has already led to a number of manufacturing breakthroughs at IBM. "We've had on the order of 10 major contributions to manufacturing and dozens of smaller ones [since] we've been doing manufacturing research," says Thomas H. DiStefano, head of measurement science and technology within the Manufacturing Research Group. The group has helped automate—and improve—the manufacture of products ranging from the electronic typewriters and printers that IBM builds in Lexington, Ky., to the thin-film heads used in the high-capacity 3370 disk drives it produces in San Jose, Calif.

Getting research and engineering teams to work together on manufacturing problems sounds easy, but in the U. S. it doesn't happen often. Although researchers now talk about understanding manufacturing better, and factory engineers emote over the wonders of automation, IBM has yet to eliminate the "us and them" attitude that can divide the two. One researcher, for example, speaks of making a process "idiot-proof" before moving it into a factory. An engineer in East Fishkill criticizes researchers for not understanding that processes cannot be controlled as closely in a plant as they can in a lab.

IBM hopes to overcome those problems by encouraging heavy and open communication between the two, says Billy T. Crowder, director of manufacturing research. Getting manufacturing to talk about its problems and research to suggest solutions helps to eliminate the old notion that researchers make inventions and manufacturers make products. More important, it enables researchers to learn what problems manufacturers will have to cope with in the future. That's essential, Crowder says, because his group isn't geared toward developing stop-gap solutions. Instead, the goal is to identify trouble spots before they develop. "The hard part is getting manufacturing people to keep an eye out for what's going to be happening in their area two to four years down the road," Crowder says.

That's precisely what made the C-4 (for controlled collapsible chip connection) inspection system at East Fishkill a success. "We saw three years ago that we had a problem," says Charles Kelly, manager of semiconductor test and finishing at East Fishkill, and formerly of Manufacturing Research. "Human visual inspection is generally only 75% efficient, and that was not acceptable. We had to be up in the 90s." The new system boosted efficiency to 99%.

IBM'S CROWDER: Communication between research and manufacturing is key.

Few companies have IBM's resources, but that hasn't kept others from finding new ways to compete on the factory floor. Northern Telecom, for example, found itself with an unusual challenge and opportunity when it was preparing for the era of the unregulated telecommunications industry a few years ago. The breakup of the Bell System set the stage for Northern Telecom, a perennial runner-up to AT&T Co., to expand its market in central office switching equipment.

To compete with AT&T and others that joined the fray, Northern Telecom set out to become the price leader in the industry, says Alan Lutz, Northern Telecom's vice president of group operations in Raleigh, N. C. Central to its strategy was a drive to completely revamp its manufac-

turing line. "Manufacturing for us is of strategic importance," he says. "We want to be—and believe we are—the cost leader in the industry."

But to get there, Northern Telecom had to rethink its entire manufacturing philosophy. Four years ago, the company used a batch process to build the line cards for its DMS-10 and DMS-100 digital switch systems. Inventories of raw materials ran high, defects could take weeks to identify, and first-pass yield, the variable by which most manufacturers measure the efficiency of their factories, stood at an anemic 65%.

To become a cost leader, Northern Telecom had to rethink its entire manufacturing philosophy, switching from a batch process to continuous control

The company realized it would have to change everything. An outside automation specialist, American Cimflex of Pittsburgh, Pa., was called in and together the companies created a modern real-time process-control system that features 48 robots and 35 computers. Every process in the Raleigh plant is monitored continously from a central control station, problems are identified and rectified almost instantly, and yield is now at a near-perfect 99.2%. The plant produces 110,000 line cards a week.

Drawing on Japanese techniques, Northern Telecom instituted a modified just-in-time delivery system and set up interdisciplinary groups to handle problems on the floor. People whose jobs were eliminated by automation were redeployed, and not a single worker was laid off during the three-month conversion from one system to the other. "Representatives of NTT [Nippon Telegraph and Telephone, the Japanese phone company] were here and they would say we're more Japanese than they are," Lutz says.

For Northern Telecom, competing came down to its ability to produce more boards than ever. "When you get to very high volumes, you have to make the transition from a batch-oriented process to a real-time process-control system," Lutz says. By constantly measuring "the state and health of the [manufacturing] system," instead of sample-testing from each batch, the company not only cut the cost of each board—direct labor costs per board are now one-third what they were three years ago—but also gained much tighter control of its factory. In the old setup, problems might not be discovered until hundreds or even thousands of faulty parts had tumbled off the line, each with identical flaws.

Better fault detection saves money and ensures that customers get products that work; rework and scrap are minimized. The payoff has been phenomenal. "An extra point of yield can be worth $200,000 over a year," Lutz says.

Automation became a useful tool for Northern Telecom when volumes reached record levels, but it has benefitted some low-volume producers, too. ETA Systems Inc., St. Paul, Minn., knew from the start that it couldn't competitively produce its ETA^{10} supercomputers without automation, says Dale A. Handy, vice president of manufacturing for the Control Data Corp. spin-off. ETA's two board-plating lines occupy about a third of its $20 million plant, but account for one-half to two-thirds of the plant's cost, he estimates.

"The key thing we've developed here is the ability to plate with lots of layers and lots of small holes," Handy says. "Automation has been geared in the past toward volume. We've done it on a much smaller volume, but we've done it to get quality and reliability." Lloyd Thorndyke, president and chief executive officer, adds: "If you don't want to [automate], you're not in the supercomputer business, because that's part of the cost today."

Automation has caught on so well throughout the electronics industry that it has begun to erode the advantage overseas manufacturers enjoy in labor costs, says Charles-Henri Mangin, president of Ceeris International Inc., an electronic-assembly consultant in Old Lyme, Conn. As recently as 1983, just 48% of the chips packaged in the U. S. were assembled automatically, he says. Now that figure has jumped to 73%. The makers of automotive electronics lead in the percentage of packages mounted automatically, according to Ceeris research (see chart, p. 84).

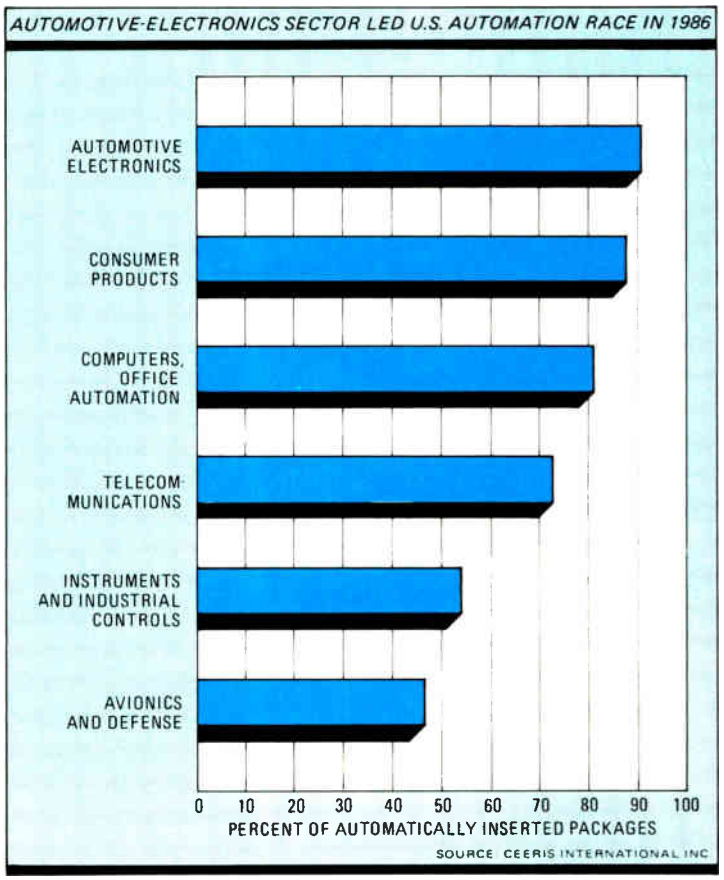
Automation, however, is not the answer for everything. Northern Telecom, for example, chose to key on quality control outside as well as inside its plants. The company insists that its vendors maintain the

FULL CONTROL. The control center in Northern Telecom's switch plant monitors key processes.

same quality standards it imposes on itself. Although it once randomly tested all incoming components for quality, Northern Telecom now inspects just 25% of the components it buys from outside suppliers, Lutz says. "Materials and components are tested and qualified by our vendors in their locations, not ours," Lutz says. That helps Northern Telecom to keep inventories low, because the company is guaranteed that every part in stock will work.

Northern Telecom has also established a series of "gates" through which a design must pass before it can reach the manufacturing stage. "You can't get a hardware design past the first design gate unless the manufacturing people sign off on it," Lutz says. A heavy investment in computer-aided-design equipment has helped Northern Telecom to employ "the design rules required for our manufacturing processes right inside the CAD software."

Just as component quality plays a key role in making Northern Telecom competitive, closer attention to the placement of components on boards has helped Zenith Electronics Corp. Within the past two years, the company has moved to eliminate product design problems that were causing trouble on the floor of its Springfield, Mo., TV factory. Chief among them were board layouts that called for small components to be placed behind larger parts on the board, making it difficult for an assembler to see what he was doing. But through a series of meetings between Zenith manufacturing and engineering people, the firm has developed a manual for designers that has become the company's Bible for optimizing product manufacturability.



Making engineers think about manufacturing is one of the greatest challenges for the U. S. as it fights to save its industrial base. The problem is simple: for years, manufacturing has been held in low regard by managers and engineers. "One place where U. S. [electronics] companies have gotten into trouble in the past is that they've made manufacturing a group in the back room that puts stuff together," says ETA's Handy. "We've tried to turn that around to make manufacturing an important, high-technology part of the company."

IBM's Crowder agrees. "The notion has been, 'If you're really good, we can use you in research. Not good enough for research? Maybe we can use you in development. Not good enough? Well, we can always find a place in manufacturing.' We reward basic innovation and not practical application."

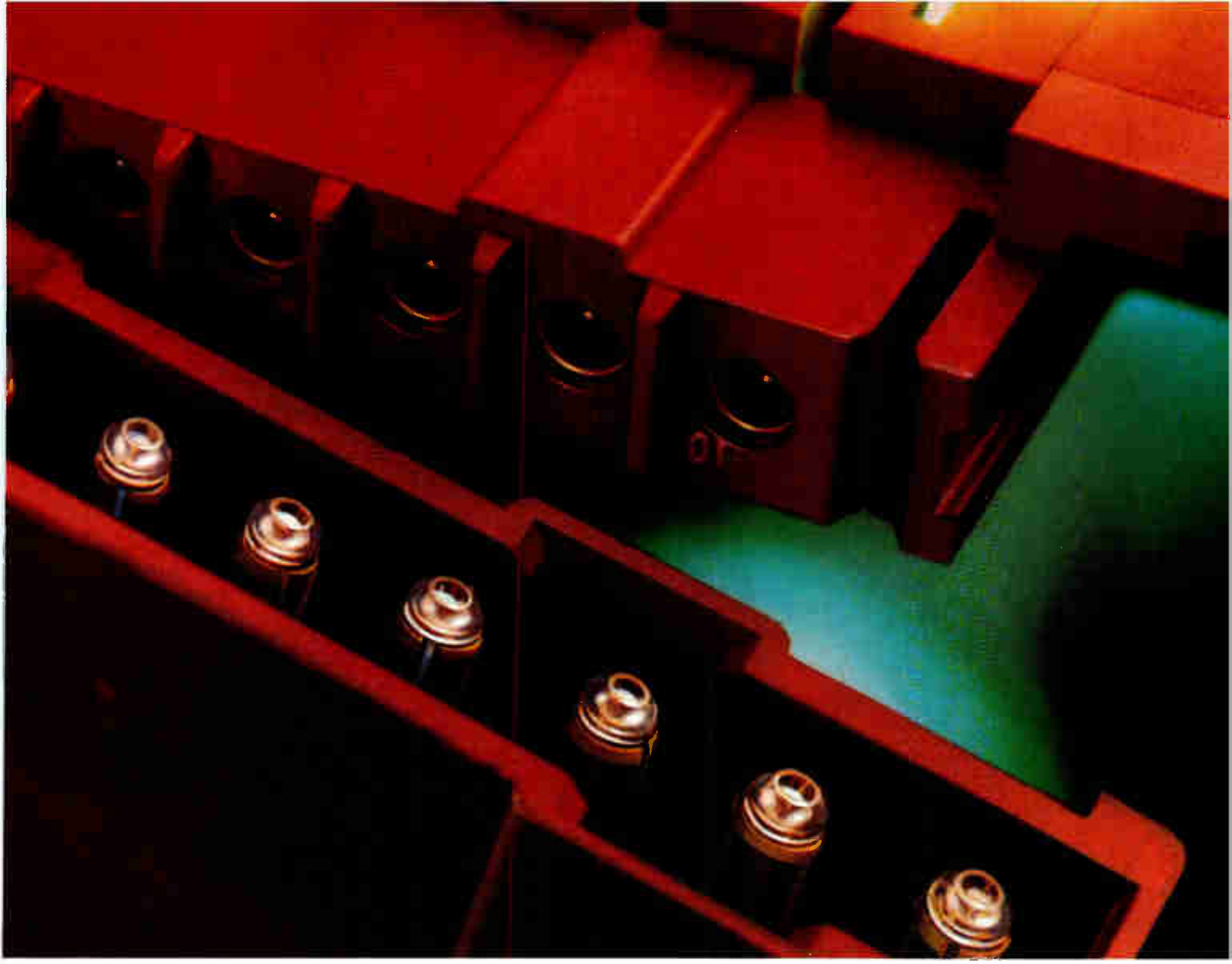
One of the best examples in IBM's drive to tie research and manufacturing together is the development of thin-film heads for magnetic disk drives. One person—Lubomayr Romankiw, a scientist in the Manufacturing Research Group—not only played a key role in developing thin-film heads, but also came up with the technology to manufacture them.

The thin-film heads are made in much the same way as integrated circuits, but were a challenge to produce, Romankiw says. "In general, the process is just as complex as any semiconductor process," he explains. "But not only do you have to worry about all the same things as you do with semiconductors, you have to worry about a whole new parameter—magnetics."

Bringing new technology such as this to a factory that doesn't have related experience is very difficult, Romankiw says. "A person has to be very familiar with the technology," he adds. "The receiver of the technology very often doesn't understand what you are trying to deliver to him, and if he doesn't learn fast, you soon will have a mess on your hands. When I'm transferring a technology, I look for it to be as foolproof as possible," he says. "If there are problems once the process is running, I just go through the plant and I smell them."

Whether drawing on research talent, trying out new inventory techniques, or automating, U. S. companies are gradually finding they can succeed where they might once have failed. Can the U. S. compete as a world-class electronics manufacturer? ETA's Handy sums it up: "U. S. manufacturing can be kept here. It just takes dedication. ETA had to focus very strongly on what its business is, and what it's trying to accomplish, and then work at it—and [now] we feel we can compete with anybody." □

–Additional reporting by Wesley Iversen



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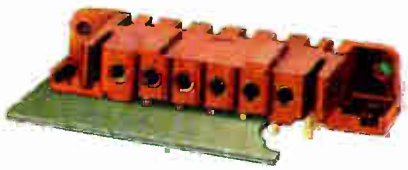

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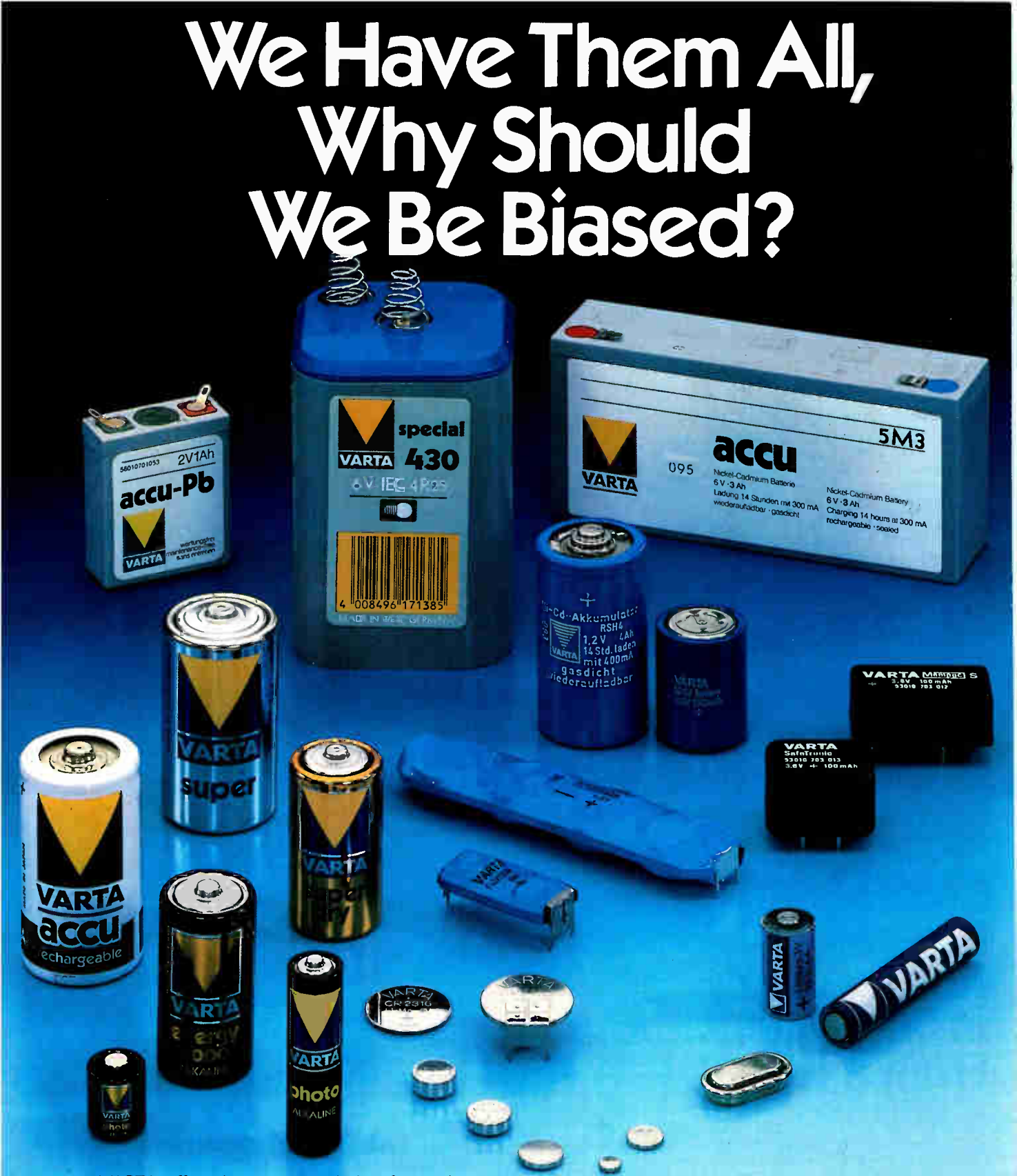

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INTERGRAPH LINE GETS ZIPPY ENGINE, GRAPHICS

Intergraph Corp. is out to save a rapidly growing list of designers a big chunk of money—those people who increasingly need both task acceleration and high-speed graphics-display capabilities in their work stations. The Huntsville, Ala., company is upgrading its work-station line by adding two boards: a floating-point engine that accelerates such tasks as analog simulation, printed-circuit-board layout, and mechanical-solids modeling; and a graphics processor for state-of-the-art graphics display.

The new line starts at less than $30,000. Up to now, designers had to pay a lot more for that combination: a dedicated accelerator would cost anywhere from $40,000 to $250,000, depending on the task, and then it would have to be hooked up to a work station with a high-speed graphics display.

The new work stations serve a broad range of markets: mechanical, electrical, and architectural computer-aided design, and scientific computation. They are expected to be available in September.

The work stations (see fig. 1) retain the names of the three existing Intergraph offerings—InterPro, InterAct, and InterView—but the three now each come in two different versions, the 340 and 360, which have varying amounts of main memory and disk space. The InterPro is for general-purpose use; the InterAct is geared toward mechanical CAD; and the InterView is aimed at mapping. The floating-point engine and graphics processor board (see fig. 2) are what set the new line apart from the previous generation.

The floating-point engine addresses the need for high-performance point acceleration of a variety of diverse tasks, including analog simulation and mechanical modeling. Electrical-engineering point accelerators cannot be used on a mechanical design problem because they are too specialized.

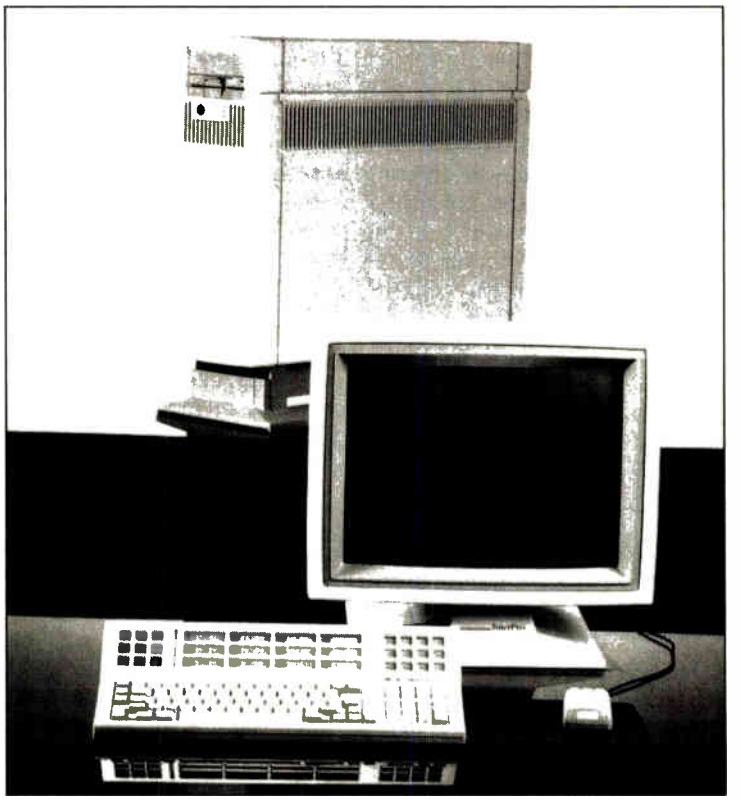
The Intergraph engine can accelerate tasks up to an order of magnitude faster than the 5-million-instruction/s Fairchild Clipper central-processing unit in the Intergraph work station. The engine has a single-instruction, multiple-data-path architecture that can execute as many as five operations concurrently. It has both a dedicated floating-point processor and an integer processor.

The graphics processor board can handle a variety of different applications simultaneously, because it comes equipped with a 1-Mbyte writable control store. Any application—analog simulation, pc-board layout, mechanical-solids modeling—can be programmed into the control store, and calculations can be accelerated at the full speed of the accelerator. The writable control store uses static column random-access memory (SCRAM), where column-address selection is made without the additional address-strobe clock that conventional static RAMs use. The result is static-RAM performance at dynamic-RAM costs.

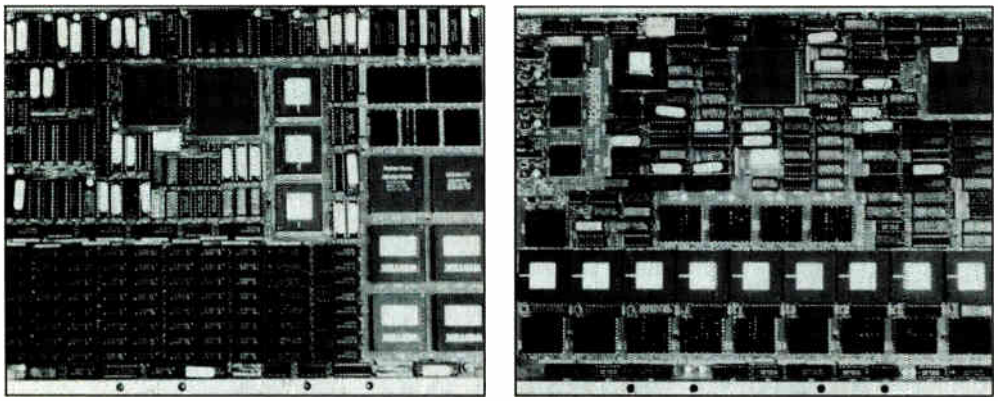
To address the problem of graphics displays, the company designed its graphics processor with the same single-instruction, multiple-data-path architecture as the floating-point engine. It placed the shading and polygon-fill operations into a 1-Mbyte writable control store on the graphics board to allow real-time wireframe manipulation and shading and polygon fills in less than a second. A special emitter-coupled-logic gate and three additional chips implement the control functions of the board's dual frame buffer, which provides fast screen update.

Both work stations have eight slots, but only four in each are required for a complete system with 16 Mbytes of memory. Two of the remaining slots can be used for additional 32-Mbyte boards of memory, for a total of 80 Mbytes. The wide-band input/output processor offers data throughput three times faster than the previous version. The board uses an 80386 I/O processor board with 2 Mbytes of its own on-board RAM.

The floating-point engine board is based on the Weitek 1066 32-by-64-bit register file and 2264 and 2265 floating-point multiplier/accumulator and multiplier chips. The engine has a peak throughput of 25 double-precision megaflops. It has a 32-bit integer processor and its own 8



1. QUICK. With its 5-mips Fairchild Clipper chip and new 25-megaflops floating-point engine, Intergraph's work station offers blazing speed.



2. POWERFUL. Both the floating-point engine (left) and the graphics processor board use a single-instruction, multiple-data-path architecture to accelerate their processing tasks.

Mbytes of data storage that is separate from other memory in the system. The processor can access any word from the memory with an 80-ns cycle time. Data and instruction transfer in the system is over a high-speed, 64-bit data path. A program sequencer, which accesses 128-bit-wide instructions from the 1-Mbyte writable control store, directs the board's operations.

Each of these operations is specified by individual fields inside the 128-bit instruction word. The operations include multiply and arithmetic logic unit—add, subtract, and compare; floating point, fixed-to-floating-point, and floating-point-to-fixed conversions; loading and storing operations from the processor board's 32-by-32-bit register file to main memory; integer operations performed in the separate 32-bit integer ALU onboard; and branch-control operations.

To speed up operations, users can determine the location of performance bottlenecks in their particular application. They can microcode the analog simulation program into the writable control store of the floating-point engine board and accelerate the operation of the program tenfold.

"We see the engine as a generally programmable supermicrocomputer that can be specialized for any floating-point-type application," says Bruce Imsand, vice president of systems development. The company will provide a standard set of applications, but if the user has an application for which no programs exist, "I have a group of programmers whose job is to convert the user's C and Fortran programs and subroutines into code for the writable control store."

With a megabyte of writable control store, more than one application (such as an analog-circuit simulator) and smaller subroutines (such as fast Fourier transforms) can use the floating-point engine concurrently. Because more than one library or applications program can be loaded into the writable control store, it is not necessary to unload one application to load another. This is in contrast to other implementations of writable control stores, where the system must overlay the previous application to run the current application.

The floating-point engine uses 1 Mbit of SCRAM, which offers nearly the speed of SRAM at the price and power consumption of DRAM. The 1-Mbit SCRAM on the floating-point engine affords the system an 80-ns total memory-cycle time for data accesses within the current page of memory. There is a 96% chance that the next memory access will be in the current page of memory. The SCRAM cycle time can be as low as 60 ns, but this application only requires 80 ns. If the memory access is in the next page, then the access requires another clock cycle to establish another row address.

The graphics processor board is also a single-instruction, multiple-path data processor. To achieve its high-performance color capability, the board contains nine 32-bit data-path processors, each with its own megabyte of control-store memory using SCRAM chips, just like the floating-point engine. All the microcode for performing graphics functions is in the control store.

Shading and polygon-fill operations tend to slow down most graphics processors. The board can handle polygons of any description, rectangular fills, patterning, vector generation of all descriptions, straight shading, or Gouraud shading—a well-defined color-interpolation technique that determines in an image what the interim colors are along a scan-line path on a surface. The board can display 512 active colors from a palette of 16 million and can redraw an image on the screen at a rate of more than 100,000 vectors/s.

Each of the nine data-path processors controls one of the nine video planes of memory to provide the 512 colors out of the palette. Each data-path processor is an enhanced 32-bit bit-slice processor with a 32-bit funnel shifter, video FIFO, and interfaces to two 32-bit buffers—one for its private memory cluster, and the other to a bus that runs throughout the board and with which all 32-bit data-path processors connect. An ECL gate array on the board contains all the logic to move the signal from the nine video planes to the digital-to-analog converters that will drive the video display. The three palette chips—red, green, and blue—that drive the video-display monitor each contain an 8-bit DAC and a 512-by-8-bit lookup table. These parts were developed jointly by Intergraph and Honeywell and are only now becoming commercially available to other graphics work-station makers.

The graphics processor board contains two sets of nine video planes. One is being displayed while the second is being updated. With simple graphics images, 10 frames/s can be produced. A more complex architectural diagram might produce only two frames/s. *–Jonah McLeod*

For more information, circle 481 on the reader service card.

NOW THERE'S A STARLAN TRANSCEIVER ON A CHIP

Designers wanting to include a transceiver for a StarLAN local-area network in a new product now can do it for one tenth the cost of the usual $500 board stuffed with standard components. Advanced Micro Devices Inc. has come up with a single-chip StarLAN transceiver employing AMD's low-power bipolar current-mode-logic technology. By combining the Am7961 with an IEEE-802.3 LAN controller, a designer can get a two-chip StarLAN transceiver that will cut his costs to no more than $50.

The Am7961 StarLAN coded-data transceiver (see fig. 1) replaces as many as 15 discrete components. It is the first bipolar device to integrate a differential transmitter and receiver, Manchester encoder/decoder, several diagnostic and signal-qualification features, and other circuitry into one 28-pin chip. It supports inexpensive multipoint-ex-tension configurations and includes a special collision-detect circuit for the MPE configurations. The 180-by-200-mil integrated circuit (see fig. 2) consumes only 620 mW of power, and the Santa Clara, Calif., company says the use of CML provides nearly jitter-free performance. It is available now.

StarLAN is a standard endorsed by the IEEE-802.3 committee of the Institute of Electrical and Electronic Engineers. The standard specifies a 1-Mbit/s baseband transmission over a 500-meter distance without the use of signal repeaters. StarLAN shares the same network-protocol specifications as its IEEE-802.3 cousin, Ethernet: a back-off algorithm scheme called CSMA/CD (carrier-sense multiple-access with collision detection). The physical medium for StarLAN is twisted-pair wire, which can be either shielded or unshielded. Since unshielded twisted pairs already exist in wiring closets for office private branch exchanges, use of StarLAN can eliminate the wiring and installation costs for a local net.

The basic topology of a StarLAN is a star consisting of a header hub and hierarchical levels of intermediate hubs and stations. However, in some cases, it is possible to avoid the expensive hub configuration by adopting the StarLAN multipoint-extension (MPE) option—and one big selling point of the Am7961 transceiver chip is its support for MPE, says Jayshree Ullal, senior strategic development engineer at AMD.

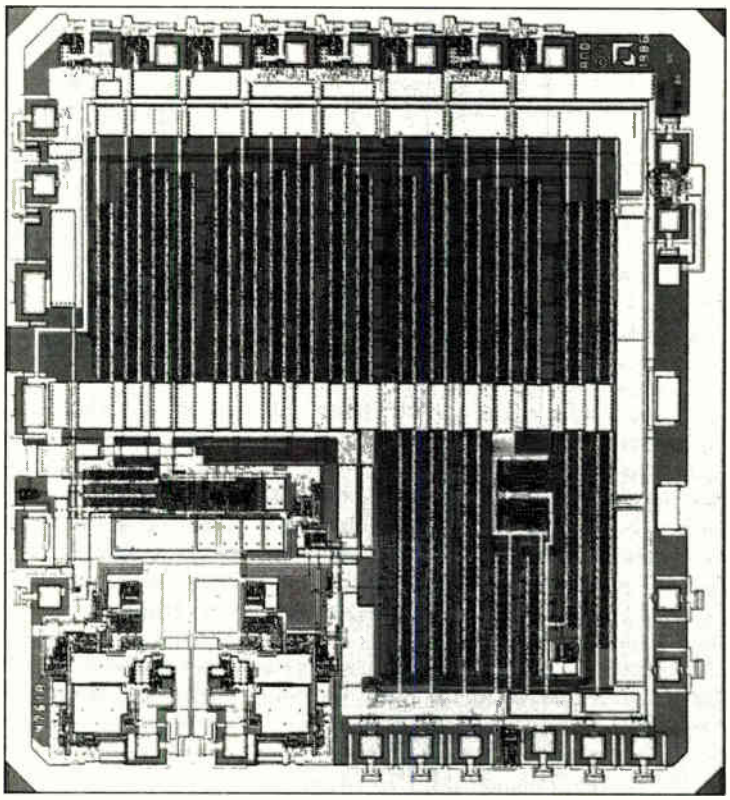
In an MPE implementation, the integrated circuit allows the connection of two to ten stations in a serial bus configuration without a hub. One of these stations also serves as a station on the StarLAN, and the other stations on the serial bus can use it to gain access to the entire network.

An MPE configuration makes it easier to build highly complex StarLAN networks with many branches. It provides a network in which Am7961 transceivers can be linked in a daisy-chaining scheme incorporating a passive serial bus configuration—one of the options now being considered by the IEEE-802.3 committee.

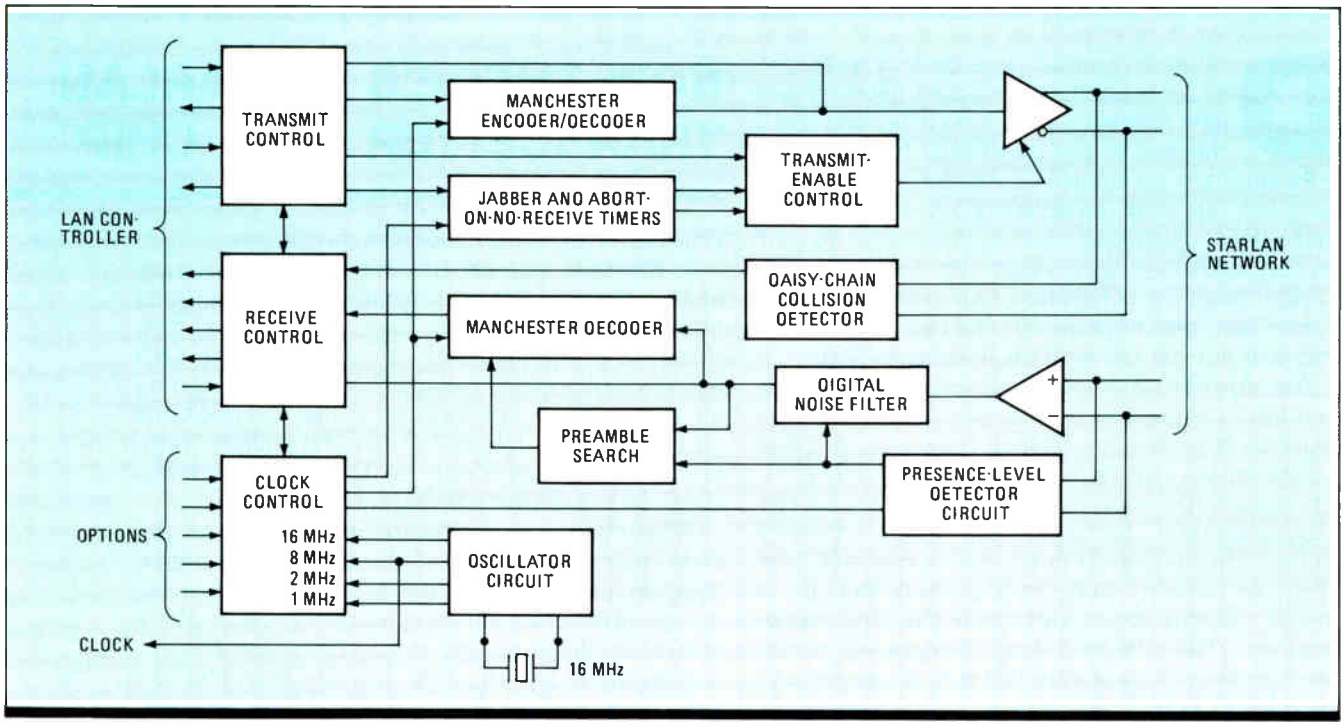
A StarLAN with an MPE scheme is a merging of two types of network configurations: hub and multiple branching. In such a complex net, there's a good chance of signal collision, so AMD has devised a collision-detection method based on an overvoltage comparator. Collision conditions on the 7961 are detected at the transmitter, rather than at the receiver, so that cable attenuations do not distort the signal.

When daisy-chained stations transmit at the same time, the quality of the transmitted signal depends on the amplitude of overvoltage noise spikes produced. The amplitude of the voltage spikes is detected by monitoring the relative phase angles of the two transmitting stations and the characteristic impedance of the network.

The comparator is designed to detect overvoltage conditions whenever two or more stations on the network are transmitting simultaneously. These signals are fed into one input of the comparator, while the other input is used to establish a transmitter voltage reference. The resulting output of the comparator flags a collision condition and disables the transmitter.



1. CURRENT MODE. The Am7961 StarLAN CML bipolar chip occupies only 180 by 200 mils and consumes only 520 mW; it replaces 10 to 15 discretes.



2. ALL IN ONE. The Am7961 StarLAN transceiver integrates a differential transmitter and receiver, Manchester encoder/decoder, several diagnostic and signal-qualification features, and a special collision-detect circuit for MPE configurations.

A peak detector, driven by a combining logic block, tracks and holds the average peak value of the transmitter outputs, which is used to generate the voltage-reference signal to the inverting input of the comparator. A phase detector, driven by a second combining logic block, adjusts and attenuates the phase of the instantaneous peaks of the transmitter output levels and feeds into the comparator's inverting input.

When there is only one active transmitter, the peak detector's output—the voltage reference—is greater than the phase circuit's output. In this condition the comparator is disabled, because the noninverting signal is greater than the inverting signal. The input bias of the comparator ensures that noise on the MPE network is ignored.

When there is more than one active transmitter, the condition changes. Voltage and phase distortions are detected, driving the inverting input of the comparator more positive than its noninverting reference input. This sets an on-chip latch, disabling the transmitter and activating the collision-detect output.

The 7961 is the only LAN chip that integrates the collision-detect circuit to provide a reliable daisy-chaining mechanism, Ulall says. What's more, the IC can be be used with existing transmitters to add MPE capability to existing StarLAN networks.

The on-chip Manchester encoder-decoder separates encoded data into non-return-to-zero data, provides an accurate clock for the decoded signal, and minimizes jitter in the received signal. It accomplishes data recovery through a special sampling technique. Data is sampled at intervals one fourth and three fourths of the way through the bit stream. If the samples are of opposing values, valid Manchester data is decoded. If the samples are identical, a violation is flagged at the collision-detect pin. Then the next ¼-bit interval is sampled. If the samples are still the same, an Idle signal is activated. The signal drives the transmitter output to a high state for 2 or 3 μs. This starts the protection timer, disables the presence-level detector, and inhibits reception of data.

Another feature on the 7961 transmitter that will make it valuable in many LAN applications is the ability to control the slew rate and thus minimize higher-order harmonics and undesirable interference, says Ullal. The chip also controls the rise and fall times of the transmitter to decrease jitter effects. And to increase network reliability, it incorporates a digital noise-filter circuit through which a differential signal—after being qualified for phase, amplitude, and duration by an internal presence-level detector—is passed to eliminate transient noise conditions. An on-chip filter also removes the need for external, discrete filter circuits, thereby increasing network reliability.

Using any IEEE-802.3 LAN controller, a 16-MHz crystal, two isolation transformers, and the Am7961, a StarLAN node is easily implemented. The 7961 is also designed to interface several LAN controllers, including the Am7990, 82586/588, and 68802. The Am7961 with a 7990 or 82586 controller IC supports bus-master configurations, such as a network of IBM Corp. Personal Computer ATs. The 7961-82588 combination supports a slave-mode interface, such as a network using the IBM PC/XT.

–Bernard C. Cole

For more information, circle 482 on the reader service card.

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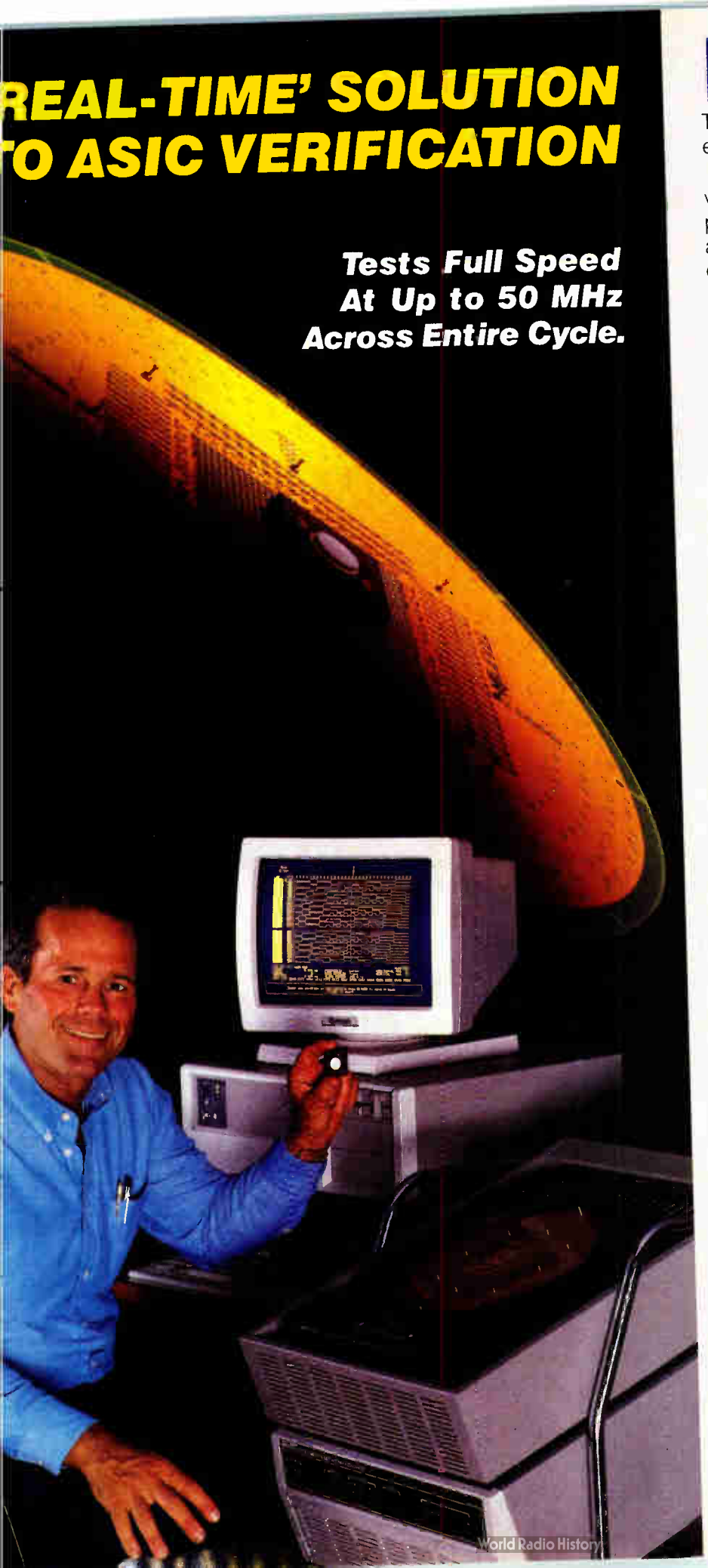

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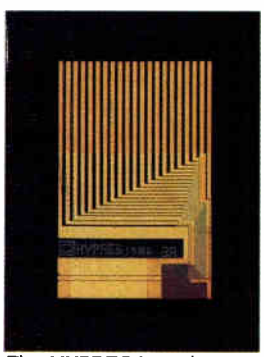

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Think of a technology with demonstrated switching speeds of 3 picoseconds.

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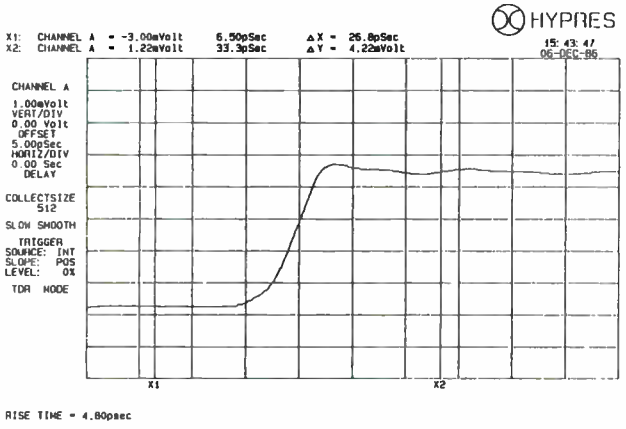

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Introducing an ultra high speed, high sensitivity measurement system with performance parameters never before achieved with superb convenience and transportability. It's...

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Time domain techniques now provide a complement, or an alternative to frequency domain approaches. Use time domain to • characterize ultra-wide bandwidth fixtures, coaxial lines, strip lines, mm IC components • millimeter-wave communications and radar • sub-nanosecond digital processing • advanced GHz packaging • pico-second device development • electro-optics • physical research.

HYPRES designed the PSP-1000 as a modular instrument. The user only changes the input module to convert from one type of operation to another. Changes take less than a minute. Using the technology, with its ultimate switching speed of 0.01 ps, future modules will be much faster than the present 5 ps.

Modules for single or dual channel oscilloscope operation, single or dual TDR use, or combined oscilloscope and TDR for simultaneous TDR and TDT tests are available. Considered as the first picosecond work station, the PSP-1000 is truly cost effective. Not only will you make measurements never before possible, you'll make them with a system that expands to meet your needs.

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We know how important ease of use is. The PSP-1000 features a 13-inch color screen and the least cluttered control and knob panel on the market. Measurement and setup aids save you time and simplify operation.

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The PSP-1000 uses Josephson junctions, interferometers and nearly dispersionless transmission lines to achieve speed and sensitivity heretofore unattainable. And this is just the beginning.

HYPRES' niobium-based Josephson junctions operate at better than 5 ps. We've already produced step generators with 3 ps rise times using 5 micron junctions. Other devices, HEMT, PBT, RTT and the like, require submicron geometries to approach 10 ps. HYPRES anticipates reaching a theoretical limit of 0.01 ps.

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The PSP-1000 Picosecond Processor

HYPRES combined revolutionary chip and cooling concepts to solve conflicting thermal, electrical and mechanical problems of these devices. HYPRES uses refractory materials such as Nb and NbN to solve the thermal cycling problem of lead and its alloys. HYPRES also perfected the technology of manufacturing highly uniform Josephson junction switching thresholds across the wafer. We're ready to take advantage of higher temperature superconducting materials right now.

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For more detailed specifications of the PSP-1000, ask for our brochure. Hypres, Inc., 500 Executive Boulevard, Elmsford, NY 10523. Please phone our toll free number, 1-800-JJ3-0522.

Circle 93 on reader service card

HYPRES, Inc.

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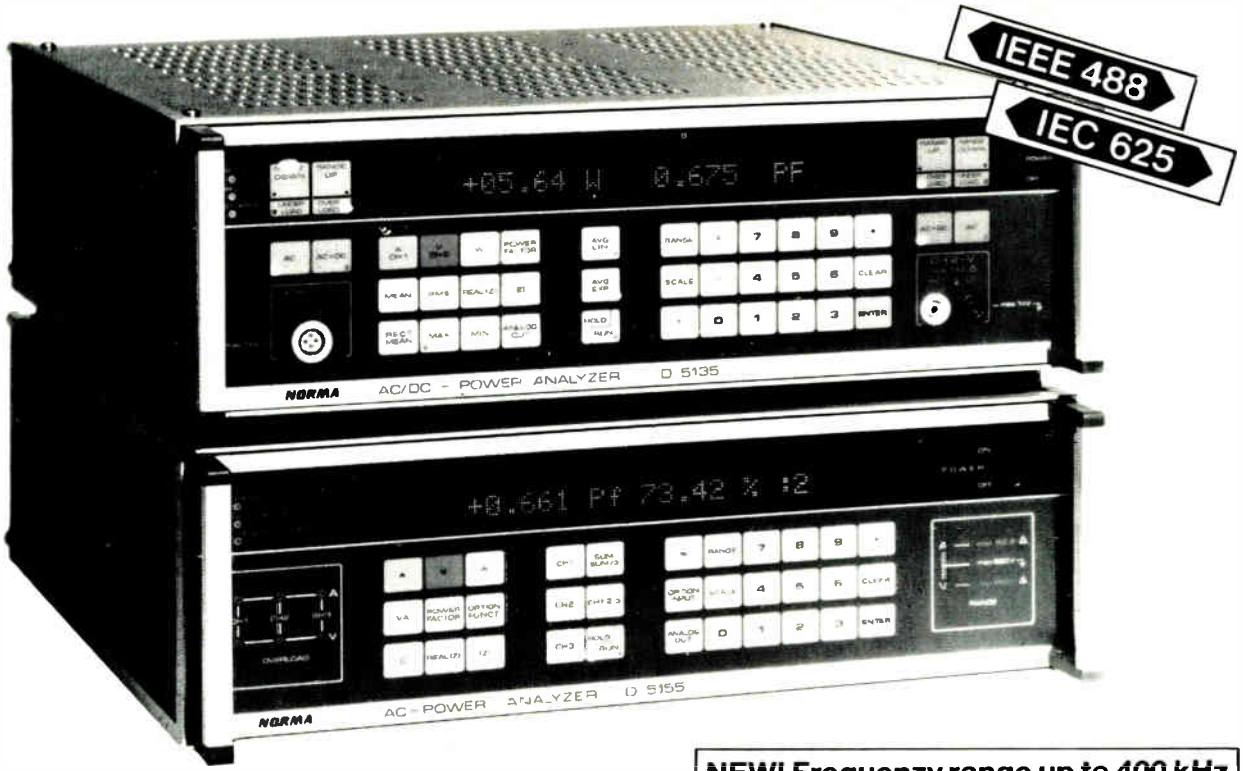

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FROM SEIKO, A 3-D GRAPHICS SYSTEM THAT'S 20% CHEAPER

It runs 400,000 vector transformations a second—speedy enough to achieve smooth real-time manipulation; fluid zooms, moves, rotations, and pans are all second nature

by Jonah McLeod

Designers no longer have to shell out up to $50,000 to buy a 3-dimensional color graphics-display system. Seiko Instruments U. S. A. Inc. is introducing its D-Scan GR-4416, which will sell for only $32,000—underselling its market rivals by 20% or more.

The San Jose, Calif., company trimmed costs by going, wherever possible, with VLSI chips rather than standard integrated circuits and discrete components. This decision paid off all along the system's graphics pipeline: a display control module was squeezed onto one board rather than three; a bit-map control module was cut down from three boards to one; and a frame buffer/video output module comes on two boards instead of three. All in all, Seiko cut five boards out of its system.

The Seiko system is fast! It whips through 400,000 vector transformations/s—speedy enough to achieve smooth real-time manipulation. Fluid zooms, moves, rotations, and pans are all second nature to the new product. Fitted with its full complement of 20 frame buffers, all of which can be double-buffered, the 4416 can paint a 1,280-by-1,024-pixel screen with 1,024 colors. At 640 by 512 pixels, it offers a palette of 16 million hues. With this kind of price-performance, Seiko engineers figure their new global product will meet the needs of designers in mechanical computer-aided design, electrical CAD and computer-aided engineering, and scientific modeling, as well as those people involved in medical imaging.

Accounting for the speed of the Seiko system is its pipeline, which has itself been streamlined. The matrix processor in the display control module, for example, is 30 times faster than its rivals. The bit-map control module is home to two data-differential-analyzer chips that share the work usually handled serially by a monolithic processor. Another two DDA chips generate 60 pixels every nanosecond. The module also houses a pair of 4-by-4-pixel buffers that write 60 million pixels/s, ensuring that images on the screen move smoothly. Finally, every module is fitted with a first-in, first-out buffer that helps move data quickly between modules.

Operation begins when a graphics image in the form of a command list ("draw line," "draw polygon," and so forth) is keyed in or sent from a minicomputer or host mainframe. The list first passes through the graphics control module (see fig. 2). A 12.5-MHz 68000 microprocessor within this module converts the command list into vectors and

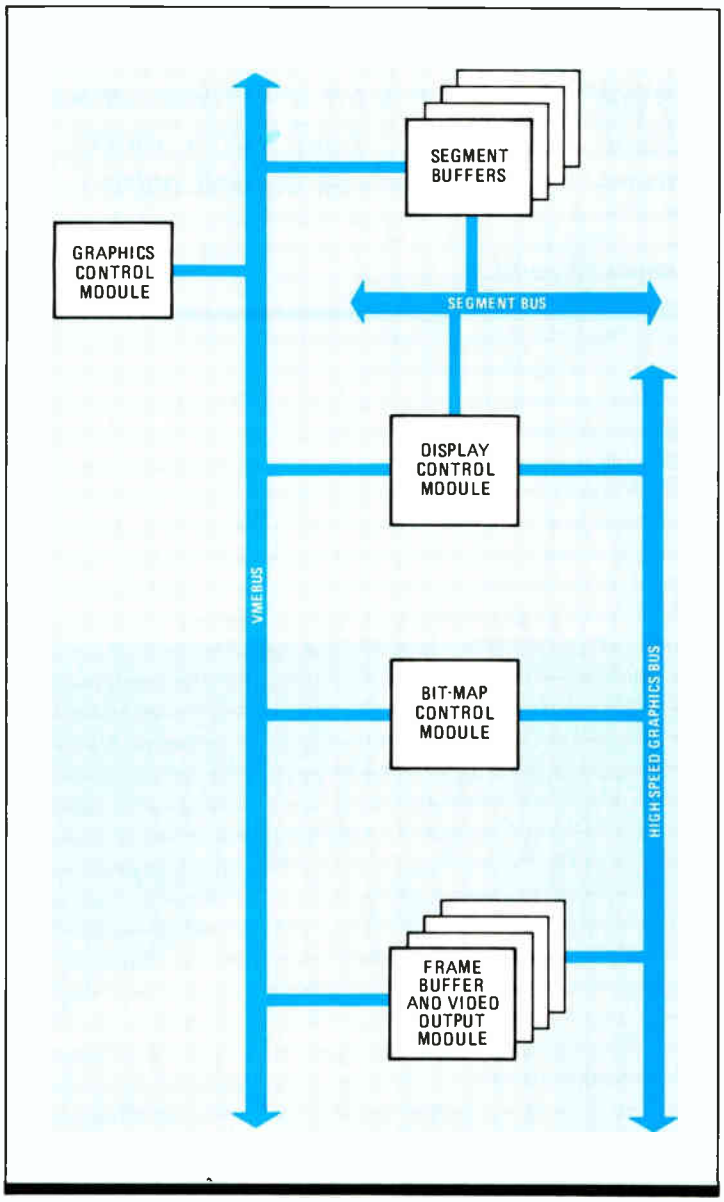
1. COMPETITIVE. Seiko's GR-4400 series graphics system offers more performance at the same price as other high-end systems.

ships them out to the segment buffers. A design of less than 10,000 vectors can fit into the 0.5-Mbyte segment memory that is standard on the system, but designs typically call for 4 to 6 Mbytes and are stored on the system's optional hard disk.

Once in segment memory, the vectors are loaded into the graphics pipeline. The three modules that make up the pipeline execute the major functions that are associated with manipulating a 3-d image on the screen.

At the head of the pipeline is the display control module. It converts the vector from the coordinate system used within the confines of the CRT screen into world coordinates, a general coordinate system that is unrelated to the display coordinates. It then makes the required calculations on every vector to relocate the image to the position specified by the operator as he moves a mouse.

Inside this module are two processors. The display processor, a 32-bit-wide AMD 29203 bit slice, grabs 400,000 vectors each second and strips them of their display coordinates, assigning world coordinates in their place. The vectors are then shunted to the matrix processor, a 4-by-4-pixel unit assembled from four CMOS 8,000-gate arrays. The matrix-processing unit performs the calculations needed to rotate, position, and scale an image.



2. STREAMLINED. The GR-4400 graphics pipeline runs without bottlenecks from display control module to bit-map control module to frame buffer.

In many graphics systems, the matrix processor is itself a bottleneck, slowing things to the point that, out of the 400,000 vectors crammed into the system each second, only 100,000 can be handled. Usually, these units work through such trigonometric functions as sine and cosine. But Seiko has chosen to sacrifice floating-point capability for raw speed, designing the processor for matrix algebra only. As a result, it rips through 28 calculations—16 multiplications and 12 additions—in one instruction cycle. Competing systems take up to 28 cycles.

To make certain that the system doesn't bog down, each module is fitted with a D-scan graphics bus controller. The 900-gate array, which acts as a fast FIFO buffer, hustles the data onto and off of the graphics bus.

MAKING THE IMAGE FIT

Once the image has been mathematically positioned within the world coordinate system, the vectors are passed along to the bit-map control module. Here, another 32-bit 29203 clips the image to fit the viewing area on a CRT screen. Then the viewing transformation processor, an 8,000-gate array, converts world coordinates back into display coordinates.

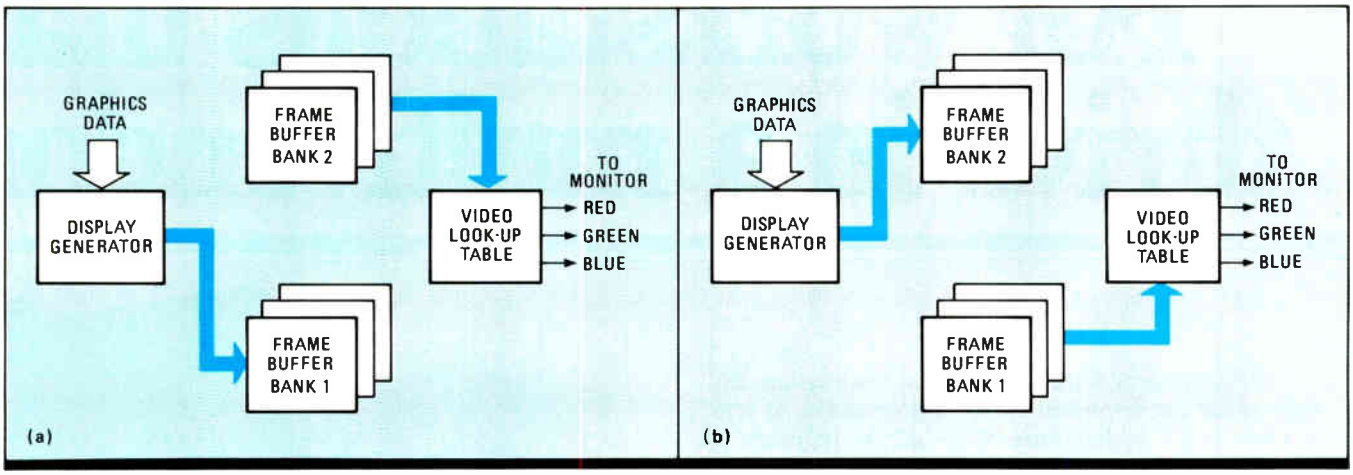
From there, the image data is sent to the first of four DDA chips. The first pair determines the slope of each image vector to be drawn on the screen. The second determines which pixel to illuminate on a bit map of the CRT screen.

On other systems, these data functions are usually handled serially by a monolithic processor. By partitioning the function, the GR-4416 handles the data rapidly and efficiently.

The first data function is fielded by two CMOS 2,600-gate arrays. Each carries an arithmetic unit that calculates such image parameters as drawing direction, transformation values, and slope determination. The second pair of LSI devices, two 3,000-gate CMOS arrays, are 16-bit-wide pixel generators that use the data from the first two DDA chips to determine which pixels to light. They spend a scant 60 ns on a pixel. These four chips together can handle data at 2 ns per vector.

The second team of DDA chips feeds the first of two 4-by-4-pixel buffers, both on one 850-gate CMOS array. Once the first buffer is filled, it dumps its load into a 4-by-4-pixel section of the frame buffer while the second pixel buffer is being topped off. Once the second pixel buffer is loaded, it drops its data into another 4-by-4-section of the frame buffer, and so forth.

By alternating in this manner, the Seiko sys-



3. DOUBLING UP. With the double buffer on the GR-4416, one frame buffer is filled while a second writes to the monitor (a), then the second buffer is filled with the next image while the first writes (b).

tem makes it is possible to write 60 million pixels/s (54 ns/pixel) to the frame buffer, a 28% improvement over the system's closest competitors, which top out at about 40 million pixels/s (74 ns/pixel). In essence, the system fills the background buffer while the foreground buffer is displayed to the screen. That means an image moves smoothly, without the jerkiness of some real-time graphics systems.

In operation, the pixel buffers pass on vectors to five write-table chips at the mouth of the frame buffer/video output module. These five chips write the actual pixels into the frame buffer and handle other operations. Inside the module are two banks of frame buffers, each of which is four planes deep. Each of the banks can be expanded to 10 planes, for a total of 20 planes, which permits users to take advantage of double buffering. The expanded memory uses the same write and address controller that is standard with the system.

Some competitive systems also offer a double-buffer function by splitting a large memory into two parts. But this approach requires additional logic to coordinate which half of memory is writing to the monitor at any one time. More logic must coordinate the timing for writing into one part of memory from the graphics display generator and reading out to the monitor. And splitting the memory in half also halves the number of colors that can be displayed.

Double buffering ensures a smooth transition between successive images in applications in which a new screen must be written into a buffer by the end of the current vertical retrace interval of the video monitor. Breaking the frame memory into two banks makes it possible to alternately send one and then the other to the monitor for display. That means the display generator can write to its buffer without having to coordinate with the video look-up table, which can read from its own buffer (see fig. 3). Also, since each frame buffer has 10 planes, every plane can maintain a palette of 1,024 colors.

With the high-performance pipeline and double-buffering capability, the GR-4416 can generate graphics images at a rate of 40 frames per second. Movie film is displayed at a rate of 16 frames per second. Such innovative circuit designs as the double buffer, fast DDA pixel buffer and data-differential analyzers, and matrix processor give the GR-4416 a price/performance edge in an increasingly competitive market. □

For more information, circle 484 on the reader service card.

HOW SEIKO GOT ITS PRICE-PERFORMANCE JUMP

In the summer of 1985 the world marketing group for Seiko Instruments Inc. got together at the company headquarters in Tokyo and concluded that the company needed a line of graphics-terminal products if it was to be a full-line supplier of graphics products worldwide. "We had to get ahead of competitors in a marketplace where price/performance was changing on a yearly basis," says Andrew Wei, division manager for the Graphics Devices and Systems Division of Seiko Instruments U.S.A. Inc.

Seiko put together a team that eventually numbered more than 100 hardware and software engineers. Working with Seiko groups in the U.S. and Europe, they developed the D-Scan GR-4416, the company's first high-end display system.

They were able to get the speed up to 400,000 transformations/s and keep the cost 20% below that of competing systems by the judicious use of custom-designed CMOS VLSI chips. "Our corporate management in Tokyo had the foresight to invest in developing 1.2-μm CMOS processing technology inside the company," says Wei.

The world marketing group's contribution was to define a product that would meet global market needs. They pinpointed a three-dimensional system that could provide smooth, fast interaction at a relatively low price. And, Wei says, "we saw a very large market for the kind of price/performance we had in mind."

ANDREW WEI

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Circle 99 on reader service card

UPDATE: ROUND TWO FOR A DESKTOP SILICON COMPILER


TURNING A PC INTO A SILICON COMPILER

FROM SCHEMATIC TO FOUNDRY IN LESS THAN AN HOUR

A year ago, Lattice Logic USA, of Santa Clara, Calif., launched its Silicon Compiler Spreadsheet [*Electronics*, June 16, 1986, p. 37], a product that would for the first time allow system designers to run a silicon compiler on an IBM PC AT or compatible personal computer. Users were eager to evaluate design alternatives at their desks before committing to silicon. But after they got the product they ran into bugs—and they also found it wasn't so easy to use.

Today, the company has a new owner, which has debugged the software and re-issued it in Release 5.4, and a new name. The new version so far has produced 45 chips—all of which worked the first time. The compiler also has been renamed, as the Solo 1000, and several features have been added, including a front-end design manager that helps designers make package and pin selections. A new release is due in August.

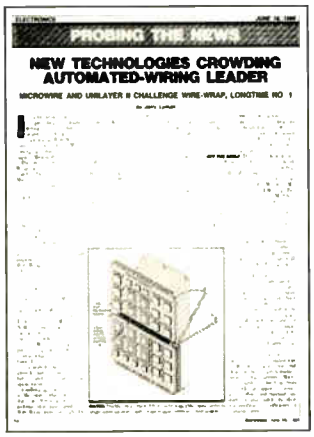
The new owner is European Silicon Structures, or ES2, which was the European distributor of the compiler. It had been interested in buying Lattice USA and its European counterpart, Lattice Logic Ltd., Edinburgh, Scotland, last year. Lattice nixed the idea because it thought that ES2—itself a startup—did not have the money to support both companies. But ES2 grew fast. Within a year, the Luxembourg-based distributor had better than $50 million in the bank. In April, it acquired both Lattice Logic USA and Lattice Logic Ltd., renaming the former US2 and merging the latter into itself.

ES2 took the feedback it got from users of the Silicon Compiler Spreadsheet and put the product back on track. The latest version, Release 5.5, will make the product even more user-friendly. In addition, the library will be expanded to include more components and analog functions, as well as ROM cells. The new release will also handle larger designs, up to 14,000 gates.

And ES2 won't be stopping there. It plans to introduce a new product in 1988 that can perform mixed-mode simulation of analog and digital components together—and again, do it all on a PC.

–Jonah McLeod

UPDATE: WIRE-WRAP HOLDS OFF THREE CHALLENGERS


PROBING THE NEWS

NEW TECHNOLOGIES CROWDING AUTOMATED-WIRING LEADER

MICROWIRE AND UNILAYER II CHALLENGE WIRE-WRAP, LONGTIME KO

The longtime leader in automated-wiring technology has managed to stay ahead of its challengers—so far. Wire-Wrap, developed in the 1950s to automate the wiring of printed-circuit boards and backplanes, has staved off the challenge from rival Multiwire and from two newcomers, Microwire and Unilayer II.

Each still occupies about the same position as it did a year ago [*Electronics*, June 16, 1986, p. 54]. The newcomers couldn't overcome Wire-Wrap's two big advantages: its huge installed base of machines, tools, boards, and software, and the fact that the technology is in the public domain. The others are all proprietary.

The competition among the four is still fierce. The companies using them are exploring new applications as they jockey for users.

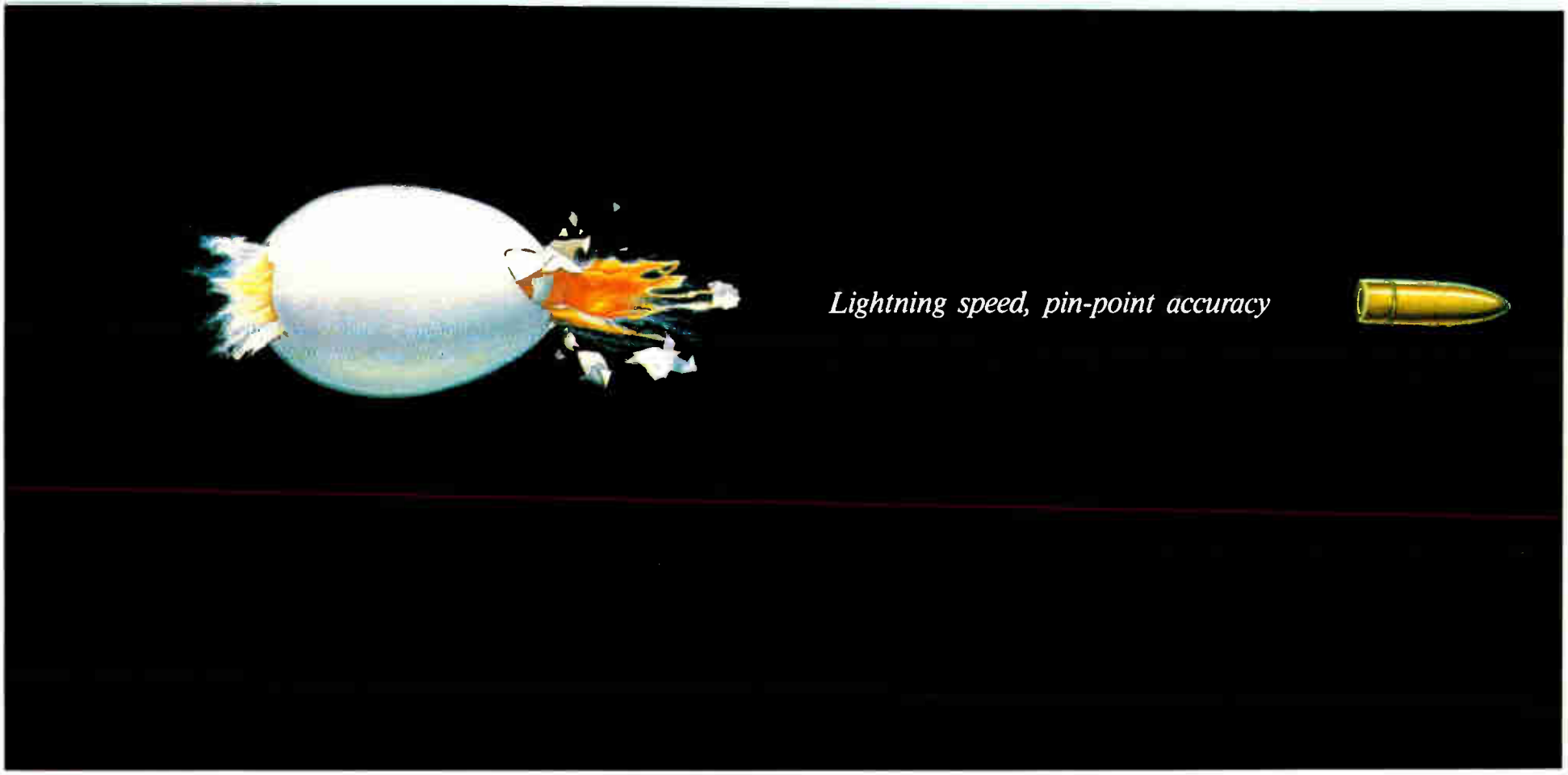
New software and hardware is moving Wire-Wrap into high-speed applications based on ECL and Schottky TTL. Data-Con Inc., a large Wire-Wrap contract service in Burlington, Mass., has a high-speed logic wiring program that minimizes propagation delays. And several Wire-Wrap manufacturers already have wrappable boards for 100-K ECL or Schottky TTL.

The Multiwire division of Kollmorgen Corp., Hicksville, N. Y., is continuing to shift from custom-board business to off-the-shelf boards with patterns that lend themselves to quick prototyping with discrete wiring. Multiwire's earlier standard boards had VMEbus, Multibus, Eurocard, and other popular formats. In early June, the company introduced Protoboard, a new panel product for general high-performance circuitry.

Unilayer II, Augat Inc.'s low-profile automated wiring technique, is picking up speed. The Mansfield, Mass., firm has a new facility that can make Unilayer prototypes from CAE data in five days.

PCK Technology's Microwire, a dense, high-speed technique based on fine-pitch leadless chip carriers, is used in several military programs. The Melville, N.Y., company's Microflex, a rigid-flex dual-Microwire-board structure, is now in production for a large contract. Microshield, a shielded version of Microwire that is also in production, still awaits large-scale applications.

–Jerry Lyman



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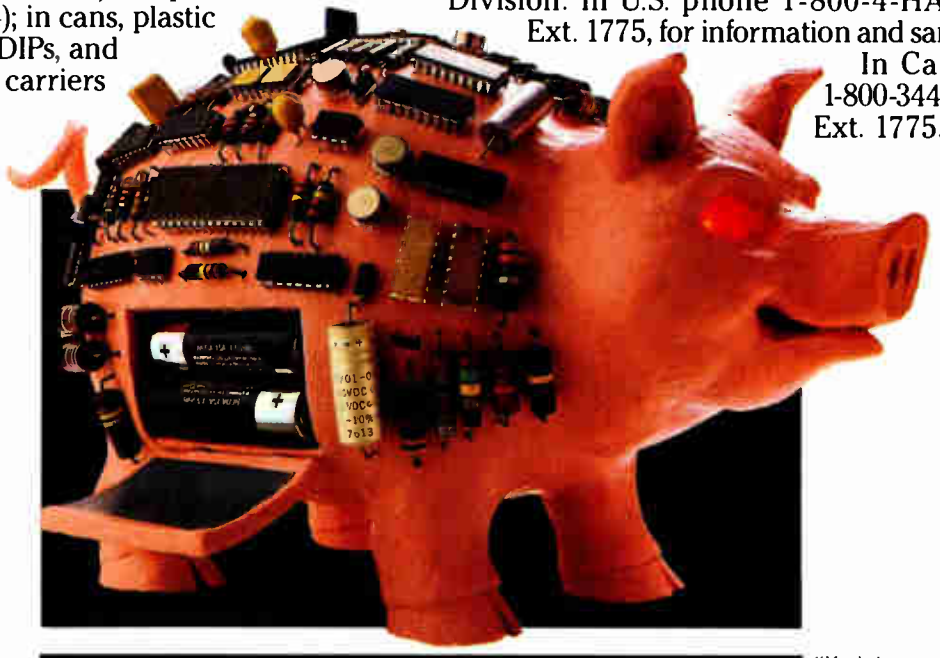

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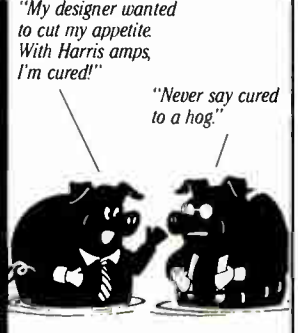


Circle 102 on reader service card

MILITARY/AEROSPACE NEWSLETTER

AIR FORCE TAPS INTEL FOR AVIONICS UPGRADE CONTRACT...

Intel Corp. is the only semiconductor company tapped to participate in a new five-year Air Force avionics upgrade program. The company's Military Operations Group will work with the Battelle Institute, Columbus, Ohio, which won a $25 million contract from the Air Force Logistics Command to come up with an engineering proposal by mid-August for retrofitting and upgrading avionics for the F-16 and other aircraft. The contract restricts Intel from actually supplying hardware for upgraded or redesigned systems or modules; rather, the company's primary role will be to recommend silicon implementations for upgraded avionics, including custom and semicustom devices. However, the contract is expandable and could eventually be worth $100 million to Battelle and bring with it a bigger role for Intel. Meanwhile, Intel is investigating several new military applications for its existing products, including the possible use of its 32-bit 80386 microprocessor as an artificial-intelligence engine. □

...AS DOD'S JOINT INTEGRATED AVIONICS PROGRAM HITS SNAG

The Defense Department is having trouble getting its Joint Integrated Avionics Program Office to agree on a definition of common modules. The DOD wants the armed services to use identical, interchangeable avionics modules that can be procured for all branches and tested with the same equipment. But the military services want more flexibility than that regulation would allow. The outcome of this internal battle has potential impact on future weapons systems, including the Air Force's Advanced Tactical Fighter—which the Navy is considering adapting for its own use—the Navy's Advanced Tactical Aircraft, and the Army's LHX helicopter. □

LITTON AND HONEYWELL TEAM UP ON ATF PROGRAM

Litton and Honeywell are teaming up to pursue contracts for the inertial navigation system that will guide the Air Force's Advanced Tactical Fighter—the only game in town for fighter-plane avionics, since it's the only fighter the Air Force will build through the 1990s. The system is scheduled this summer for demonstration and validation awards by the two prime-contractor teams competing in the ATF program—Lockheed, General Dynamics, and Boeing in one team; Northrop and McDonnell-Douglas in the other. Each of the prime teams so far has received $691 million for the initial design-validation package. Litton and Honeywell will develop the navigation system together, using their own funds, but will compete later in the production phases of the program. The work will be done by Litton's Guidance and Control Systems Division, Woodland Hills, Calif., and Honeywell's Military Electronic Division, Clearwater, Fla., as joint subcontractors. The system to be proposed will make it possible for each team member working on the navigation system to substitute its own ring-laser gyro for the inertial gyro specified for use in the system, at the Air Force's option. □

DOD TO AWARD UP TO $20 MILLION FOR ADA DEVELOPMENT TOOLS

The Defense Department has indicated that beginning in late July, it will award up to $20 million in new contracts for software-development tools for its Ada programming language. The program—under the Naval Research Laboratory's Software Systems Division and the Pentagon's Software Technology for Adaptable, Reliable Systems project—calls for production-quality tools for developing Ada application software. Prior to the release of requests for contract proposals, the DOD has identified two application areas: real-time weapons systems and information-management systems. □

MILITARY/AEROSPACE NEWSLETTER

DOD'S SWITCH TO CAD/CAM BY 1990 MAY NOT BE AS EASY AS IT THINKS

The Defense Department may find it more difficult than expected to end its reliance on paper documentation and designs and switch to CAD/CAM and similar electronic systems by 1990. That is the drift of a status report on the Pentagon's plan, called Computer-Aided Logistics Support [*Electronics*, March 19, 1987, p. 101], which is full of doubts about how the U. S. military can make the changeover to all-digital data to support logistics. The report is blunt in its apprehension about how industry and government will share CALS-based technical data: it asks whether Pentagon contractors, who will be required to adopt the plan, will share data with other contractors, including their own subcontractors. The report was mailed June 18 by the National Computer Graphics Association to industry and standards-setting organizations and key government agencies. The National Bureau of Standards, meanwhile, is scheduled to ask industry and government agencies for comments on June 25 on its proposals for handling technical documents and product definitions under the Pentagon program. A meeting of industry, government, and standards groups is planned for later this year. □

PENTAGON AGENCY CALLS FOR 'STAR WARS' RESEARCH INSTITUTE...

The Strategic Defense Initiative Organization doesn't do any research on its own, but it aims to change that. The agency that operates the "Star Wars" program wants to form a research institute to provide it with independent advice on the best way to manage SDI programs. It has apparently invited prominent scientific and technical figures—whose identities have not been disclosed—to submit proposals to operate the institute. Many of those invited are members of the SDI Advisory Committee, a nonprofit consultative group. One reason given for setting up the institute is to avoid unnecessary overlap or duplication of efforts and to facilitate the passing of information between research projects, mainly by establishing a common data base for SDI. Proposals under review by the Pentagon call for paying the director of the institute $225,000 annually and other senior staff members an average of $110,000 a year. The proposal won immediate support from the Senate Armed Services Committee, but others in Congress question whether the institute will be able to offer unbiased advice.□

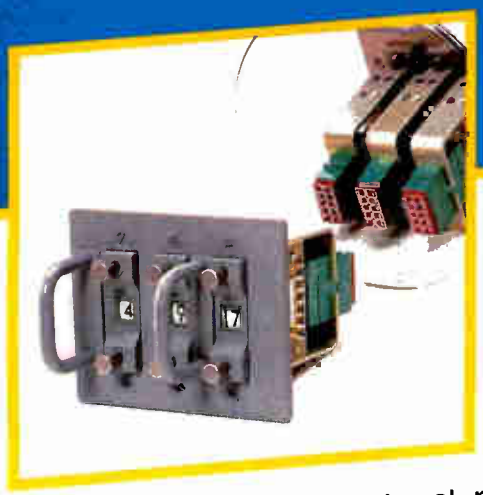
...AND AFCEA CALLS FOR NEW SDI SOFTWARE CONTRACTING METHODS

Current Defense Department software-acquisition practices are totally inadequate to support the Strategic Defense Initiative, says a study group formed by the Armed Forces Communications and Electronics Association. The Pentagon must find new contracting procedures if it hopes to develop the sources and technologies required to fulfill SDI's software requirements, said John Blakemore, the study group's software specialist and chief engineer for Texas Instruments Inc.'s New Program Development division. Speaking at the AFCEA meeting held in Washington June 16-18, Blakemore added that SDI software will have to evolve, because of "the complexity of the software problem." □

AIR FORCE LAUNCHES DEVELOPMENT OF A SURVIVABLE NETWORK

The Air Force has begun development of a survivable communications network under its Project Forecast II Advanced Technologies program. The service's Rome Air Development Center is now looking at tying multiple technologies—including fiber optics, public data networks, and cellular radio—into a real-time network-management system. RADC has initiated basic research projects with several universities to look at problems related to routing calls and messages and the handling of priority structures in an integrated voice-and-data network. An effort is also under way to develop multimedia radio gear. □

Rockwell needed a push button rotary switch for the space shuttle that would defy gravity...



JANCO DELIVERED.

When Rockwell International needed coded output switches allowing astronauts to provide critical input to the shuttle's on-board computers, they called on Janco.

But after looking through our standard catalog switches, they didn't find exactly what they needed.

We need larger numerics, they told us. There has to be greater visibility. You also have to design the switch to be actuated in a weightless environment. They asked if we could do it.

Mission accomplished. Janco engineers went to work building a switch to meet Rockwell's requirements. In addition to increasing the visibility of the numerics, a towel bar was added to the switches allowing astronauts to effect proper switching force on the button without being pushed across the shuttle's cabin in weightless outer space.

And tomorrow, you'll find 15 banks with three or more of our 10 and 12-position coded output PCB switches on each space shuttle, performing with Janco reliability on every mission.

It's challenges like the one Rockwell gave us that keep companies coming back to Janco for solutions to their aerospace and aviation switching requirements. After all, we've been doing it for the past 40 years.

Whatever your rotary selector or solenoid actuated switching requirements, Janco offers a complete line of miniature, micro-miniature, push button, printed circuit and power switch configurations to meet your needs.

For the aerospace and aircraft systems you design, call Janco for the switches to control them.

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Circle 105 on reader service card

Announcing The Winners Of The Second Annual Electronics Advertiser Audit Contest.

Earlier this year, readers of *Electronics* magazine were asked to select the ads that they thought would be best remembered by their peers. The results are in, and we are proud to present the winners of our 1987 Advertiser Audit Contest:

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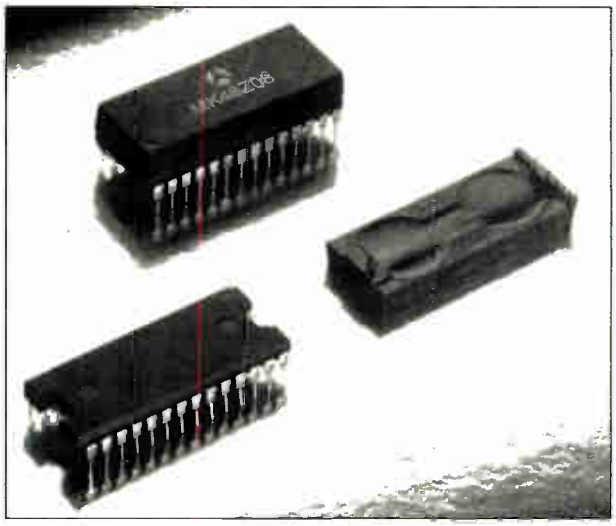
NEW PRODUCTS

BATTERY-BACKED STATIC RAMS FROM MOSTEK STORE 64 KBITS

CHIPS ADD MORE WAYS TO PROTECT DATA DURING VOLTAGE ANOMALIES

The latest additions to the battery-backed static random-access memories from Thomson Components-Mostek Corp. boost nonvolatile storage from 16 Kbits to 64 Kbits and offer a power-failure interrupt flag that alerts host processors to falling system voltages.

Two basic versions of the nonvolatile 64-Kbit Zeropower SRAMs, the MK48Z08 and 48Z18, are functionally equivalent to Mostek's four-year-old 2-Kbit-by-8-bit MK48Z02—the industry's first SRAM with an embedded lithium battery [*Electronics*, June 30, 1983, p. 147). In many applications they can replace slow, electrically erasable programmable read-only memories, which can degrade in performance after many write-erase cycles.



TWO-TIERED. A lithium battery sits atop a dual in-line package with the same pinout as industry-standard 600-mil DIPs.

The enhanced MK48Z09 and 48Z19 versions have also added features that give designers more ways to protect data during voltage anomalies. As in Mostek's 16-Kbit generation, the new 8-Kbit-by-8-bit Zeropower SRAMs integrate low-power CMOS memory cells with an analog-voltage sensor that switches on the SRAM's lithium battery cell whenever system power falls below an acceptable range.

TRIP LEVELS. Two levels of power-fail deselect trip points are available. The Z18 and enhanced Z19 SRAMs trip at levels below 4.5 V, and the Z08 and enhanced Z09 chips trigger at 4.75 V. When the trigger points trip, the chip ignores writes to memory array, preventing the loading of potentially bad data.

In battery-backup mode, data is protected for more than a decade over a zero to 70°C temperature range.

The lithium cell is contained inside a "top hat" that sits atop the dual in-line package holding the chip. The battery-in-a-DIP package has the same pinout as industry standard 600-mil DIPs for byte-wide SRAMs and EEPROMs. The Zeropower 28-pin DIP is taller, however, measuring a maximum of 0.38 in. Mostek has tested more than 50,000 16-Kbit and 64-Kbit Zeropower units and has determined a predicted worst-case battery life of 11 years at 70°C, says Dave Heacock, product marketing engineer in Carrollton, Texas.

The determining factor in battery life is not the power consumed in the protection mode but the slow evaporation of the electrolyte, says Heacock. At 25°C, the 64-Kbit Zeropower SRAM is able to retain data for more than 100 years, Mostek says.

In the enhanced 48Z09 and Z19 versions of the 64-Kbit Zeropower SRAM, the power-fail interrupt flag can be used by systems designers to prevent a processor from corrupting data when power falls below acceptable levels. The feature may also be used to initiate microprocessor startup routines whenever system power is restored. The power-fail interrupt is available through an open-drain output to the host bus. The Z09 and Z19 both have a second chip enable that can be used to address an individual chip in a bank of memory, making it easier to handle blocks of data.

The MK48Z08 and Z18 and the enhanced Z09 and Z19 chips operate on 5 V and are available in three speed grades of 150-, 200-, and 250-ns access times. Maximum active power dissipation of the 64-Kbit parts is 1 W (the average input power-supply current is 50 mA and the standby current is 3 mA). In 100-piece quantities, the 250-ns MK48Z08 is available now for $14.29 each. This 64-Kbit Zeropower SRAM will also be produced by VLSI Technology Inc., San Jose, Calif., under an alternate sourcing pact, says Heacock.

– J. Robert Lineback

Thomson Components-Mostek Corp., 1310 Electronics Dr., Carrollton, Texas 75006. Phone (214) 466-6000 [Circle 360]

DC PERFORMANCE MAKES THIS FAST OP AMP SHINE

Using an in-house linear bipolar process, Precision Monolithics Inc. has developed a fast, high-precision junction-FET input operational amplifier that matches the best dielectrically isolated parts.

Called the OP-44, it has ac characteristics similar to high-speed amplifiers such as the Harris Corp. HA-2520 but with vast improvements in dc precision, according to product marketing engineer Peter Henry. On the ac side, the OP-44 boasts a slew rate of 100 V/μs minimum and a typical gain-bandwidth product of 20 MHz. But it is on the dc side that the device shines.

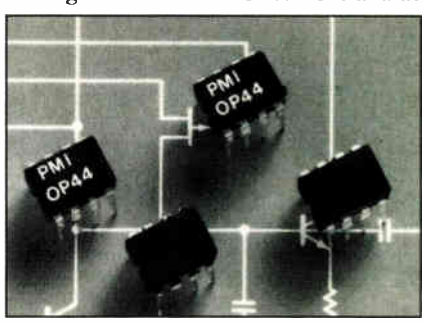
Where fast amplifiers in the past have suffered from poor offset voltages, bias current, and gain, says Henry, the OP-44 makes significant improvements in these areas. Offset voltage for the device is trimmed to below 750 μV,

compared with 8 to 10 mV for competitive devices, eliminating the need for external offset nulling in many applications.

Bias current is 250 pA at 25°C, compared with 200 to 250 nA for competitive devices. And even when the temperature increases to 125°C, the bias current is still only 25 nA.

Open-loop gain is better than 500,000 V/mV into a 10-kΩ load and is better than 200,000 V/mV into a 2-kΩ load, he says, compared with no more than 7.5 to 10 for competitive devices. Combined with an 88-dB minimum common-mode rejection, the OP-44 ensures 12-bit accuracy in both inverting and noninverting circuits, says Henry. Power-supply rejection is no more than 40 to 50 V/mV, compared with 100 to 200 V/mV for competitive devices.

The OP-44's full-power bandwidth is 1.5 MHz for a 20-V peak-to-peak signal. It has an output capable of sourcing or sinking at least 20 mA of current and at



STEEP RISE. Precision Monolithics' OP-44 boasts a slew rate of 100 V/μs minimum.

the same time is capable of surviving a continuous short to ground. Tolerant of reasonable capacitive loads, the OP-44 is guaranteed stable with 100 pF in a closed-loop gain of 3 pF, says Henry.

Applications for the OP-44 include imaging systems, ultrasound, and sonar, where its high speed and excellent precision will make it an attractive alternative, says Henry. The OP-44's high slew rate should make it the circuit of choice in pulse amplifiers, while sample-and-hold circuits and peak detectors will benefit from its low-input bias currents, Henry says.

Available now, the OP-44 comes in eight-pin metal cans and ceramic minidips and conforms to the industry-standard 741 operational amplifier pinout. It is also available in 20-contact hermetic leadless chip carriers for military applications. Available now in ceramic minidip form, the OP-44 costs $3.75 each in 100-lot quantities. An eight-pin plastic minidip version is scheduled for release in the fourth quarter of the year.

– *Bernard C. Cole*

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95051. Phone (408) 562-7206 [Circle 361]

POWER IS CUT 80% IN REGISTER FILE

Advanced Micro Devices Inc. has achieved an 80% reduction in power consumption by using its 1.6-μm CMOS process to implement a new version of the company's bipolar 64-by-18-bit register-file chip that can read and write two words in one cycle.

Like its bipolar cousin, the Am29334, the CMOS Am29C334 is a four-port, dual-access random-access-memory register file targeted at high-performance scratchpad storage.

Fabricated with AMD's CS-11 double-level CMOS technology, the 29C334 consumes a maximum of 750 MW. The second member of AMD's 29C300 building-block chip set for 32-bit processors, it has a pipelined mode supporting 40-ns cycle-time data paths—a 15% increase in overall system performance over the standard mode.

SYSTEM SPEED. Although the chip can deliver 40-ns performance, teaming it with other members of the 29C300 family results in a 73-ns pipeline-mode cycle time, says Steve Campbell, new-product marketing manager for AMD's microprogrammable processor operation.

It can be cascaded both horizontally and vertically to handle wider word widths and deeper register files. The 29C334 will write individual bytes or full words for 8-, 16-, or 32-bit systems. Its 18-bit width allows parity on each byte for error correction.

The 29C300 family's first building-block—the 29C323 32-by-32-bit parallel multiplier—was introduced in September 1986. AMD's 29C325 32-bit floating-point processor and 29C331 16-bit microprogram sequencer will be available in the third quarter, and the 29C332 32-bit arithmetic logic unit is slated for release later this year.

APPLICATIONS. AMD expects the family to be used in desktop signal-acquisition systems, factories, and military signal-processing systems. Other applications include pipelined digital-signal processing, graphics systems, telecommunications, fast-cache memory subsystems, and microprocessor interfaces.

The double-level-metal 1.6-μm technology can shrink to 1.2 μm, which will boost speeds of the register file and other 29C300 chips, says Campbell.

In 100-piece quantities, the 29C334 sells for $80 each housed in a 120-lead pin-grid-array package.

– J. Robert Lineback

Advanced Micro Devices Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, Calif. 94088.
Phone (512) 647-6274 [Circle 362]

TI'S LISP MACHINES BOOST AI PERFORMANCE FIVEFOLD

IMPROVED EXPLORER EQUIPPED WITH 32-BIT MICROPROCESSOR AND REVAMPED SOFTWARE, BUT PRICES ARE ONLY 50% MORE

Texas Instruments Inc. has designed in its recently introduced Lisp chip into the Explorer II work station to create a machine that achieves more than five times the artificial-intelligence processing performance of previous Explorer models and about 1.5 times that of Symbolics Inc.'s 3650, its major competitor.

The Dallas company claims its Explorer II is the world's most powerful Lisp work station for symbolic and artificial-intelligence processing. Yet the entry-level model of TI's new machine costs only about 50% more than the present generation of Explorer work stations, which gives it the best price/performance in the artificial-intelligence industry.

Although TI's single-chip 32-bit Lisp VLSI microprocessor, introduced early this year [*Electronics*, March 19, 1987, p. 95], played a big part in the performance boost, TI systems engineers also revamped the basic symbolic-processing software. Hardware engineers reduced the Explorer II central-processing unit architecture to a single circuit board that is implemented in surface-mount packaging.

The software designers came up with a more efficient version of TI's symbolic-processing system software. The result is a work station that is completely compatible at the software object-code level with the previous machine but is much faster.

The new software also speeds up the previous generation of systems. Existing Explorer work stations can be upgraded in the field to the new processor by swapping boards. The Nubus-based architecture—a 32-bit processor-independent bus structure—makes this upgrade flexibility possible.

STANDARD. The Explorer II work station includes 8 Mbytes of memory, a 140-Mbyte drive, and an Ethernet interface.

The Explorer II CPU consists of the TI Lisp chip, 32,000 words of writable control store, and two high-speed cache memories on the single surface-mount board. The Lisp microprocessor integrates 60% of the original two-board Explorer architecture on one 1.2-μm CMOS chip packing more than 553,000 transistors—more then 2.5 times as dense as a MC68020.

A plug-in floating-point accelerator option is available for applications requiring extensive numerical calculations. TI is also offering the LX option with the Explorer II, a MC68020 coprocessor for running standard Unix applications in conjunction with artificial-intelligence software.

Supporting more efficient development and production execution of AI applications is Release 3.0 of the AI system-software environment. Major improvements in Release 3.0 include higher performance, derived from a new dynamic memory-management scheme; new and improved application development tools; and new networking support. Networking capabilities now include interfaces to IBM Corp.'s System Network Architecture, Digital Equipment Corp.'s DECnet, the TCP/IP standard, and the Sun Microsystems Network File System.

Configurations of the Explorer II start with 8 Mbytes of memory, one 140-Mbyte disk drive, and an Ethernet interface for $49,900. They range up to the high-end configuration, the Model 73232X with 32 Mbytes, three 140-Mbyte drives, a tape drive, and the LX 68020 option for $99,900.

All 16 configurations of Explorer II, which include a high-resolution monochromatic display and a license for the system software package, will be available to customers in July. A field-installable Explorer II processor upgrade for existing Explorer and Explorer LX work stations will also be available in July for $20,000. TI is also reducing the prices of the previous Explorer systems by 9% to 19%, depending on the model.

– Tom Manuel

Texas Instruments Inc., Data Systems Group, P. O. Box 809063, DSG-141, Dallas, Texas 75380.
Phone (800) 527-3500 [Circle 340]

COLOR PRINTER HITS 200 LINES A MINUTE

By marrying a 16-bit microprocessor and customized support hardware to sophisticated graphics software, Datametrics Corp. engineers have come up with a smart color printer for military applications that runs at 200 lines/min yet produces near-photographic-quality output of 40,000 dots/in^2.

The DcM 1900 starts off on the fast track by embedding its graphics software in erasable programmable read-only memory and executing the program with an Intel Corp. 80186 microprocessor. In the past, designers have been content to use 8-bit microprocessors. Speed is further enhanced by storing output in random-access memory for transmission to the printer over a 1.5-Mbyte/s data bus.

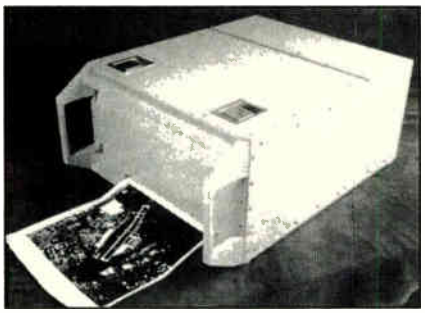
"One big advantage of using up to 4 Mbytes of RAM [output storage] is that you don't tie up your processor while the printer takes 45 seconds to print the picture," says Jerry Gaynor, marketing liaison engineer.

THREE TIMES FASTER. Using thermal-transfer technology and a standard three-color yellow, magenta, and cyan ribbon, the DcM 1900 takes just 45 seconds to print more than 4 million dots on a 10.25-by-10.5-in. page. That rate is three times faster than competitive color printers, says Gaynor. Three passes of 15 seconds each, one for each color, complete a full-color picture. The paper passes over a fixed print-head, which improves reliability by reducing the number of mechanical components. The size and weight of the overall unit are also reduced.

A black ribbon can be added to the color roll or used alone for monochrome printouts. The DcM 1900 prints 600 lines/min. in the black-and-white mode.

Proprietary software achieves near-photographic quality by a compute-intensive enhancement technique called dithering, which performs gray-scale in-

terpolations of each pixel in relation to its neighboring pixels. Dithering increases the printer's color palette to more than 4,000 shades. The software also allows users to zoom in on parts of the picture to create 4 : 1 enlargements of the area of interest. In applications



FAST. The DcM 1900 produces a full-color print of an airfield in 45 seconds.

such as the plotting of satellite data, arbitrary color assignments are possible, such as making foliage appear red. The printer also can overprint text on the graphics; it is the only military color printer that has that capability, according to Garland White, Datametrics' chief operating officer.

Applications include radar, sonar, or any system that provides a digital output of an analog signal. The DcM 1900's target market is military prime contractors such as McDonnell Douglas and Raytheon, according to White.

Because the DcM 1900 is a military product, Datametrics made it as compact as possible. "We chose the 80186 over the 80286 because it requires fewer support chips," says Gaynor. The total board space used in the printer is one-fourth that of competing products.

Because Datametrics has a target market of military prime contractors, White says, the printer's price depends on specific requirements such as interfaces, but the DcM 1900 is expected to cost anywhere from $30,000 to $35,000. The company is accepting orders now.

–Jack Shandle

Datametrics Corp., 8966 Comanche Ave., Chatsworth, Calif. 91311.
Phone (818) 341-2901 [Circle 341]

ITAC'S TRACKBALLS ARE MOUSE KILLERS

Itac Systems Inc. thinks it has a mouse killer: not a better trap, but a new trackball replacement for the computer-mouse input devices, which require most of a desktop to move a cursor around a screen.

Unlike mouses, trackballs transfer movement to the screen through movements of the ball, not the entire unit.

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Electronics Supervisor / Inspector For Quality Assurance — 2 yrs Tech. degree in Electronic Engineering. Use knowl of electronic circuit design, electromechanical devices & aspects of product performance; supv. workers who fabricate, test, analyze & adjust precision electromechanical instruments for emergency lighting equipment systems. Inspect & test components & finished systems for conformance w/specs. Recommend & oversee solutions to electronic (electrical) circuit problems. Must know electronic circuit design, electromechanical devices, product evaluation performance & test procedures. $400/wk, 35 hrs/wk; 2 yrs exp. or 2 yrs related exp. — Electronics position involving Quality control / Quality Assurance w/supervisory duties. Applicants report to: N.Y.S. Job Service, 2 Brooklyn Ave., Freeport, NY 11520 or to the Job Service closest to your home (bring 3 copies of your resume with you) J.O. #0607511 D.O.T. 726.130.010.

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RESUMES

Resumes — Complete instructions and examples; $4. Consultants, Box 567—J, Bergenfield, N.J. 07621.

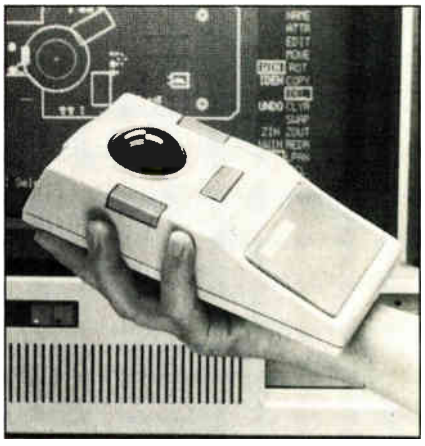
They therefore require far less room, says Peter Whitney, sales director for Itac Systems in Richardson, Texas. The company has created five Mouse-trak models using new computer interfaces and drivers that enable them to emulate popular optical mouse systems, such as those from Mouse Systems Corp., Santa Clara, Calif.

Two of the Mouse-trak models interface to personal computers compatible with IBM Corp. models, using a standard RS-232-C port and a 5-byte packed binary coding format. Three models are targeted at replacing mice for Apple, Apollo, Tektronix, Sun, and Cadnetix computers. These units use standard quadrature waveform signals indicating *x-y* directions to communicate with the host.

CONTROLS. Four of the Mouse-trak models have a speed-control button that changes the trackball's cursor-movement turning ratio. Four of the five Mouse-trak units also have a feature that will start a line with the first push of a button and end it with the second.

The units measure 8 in. by 4 in. by 1½ in. high. Unlike optical mouses, they require no special work surfaces or additional power supplies, says Whitney.

For IBM-compatible personal computers, Itac Systems is shipping the model 4, which has two input buttons and a suggested retail price of $169. Model 5 has a three-button control and is priced at $179. Both of these models have speed control.



ADAPTABLE. Mouse-trak units work with a variety of personal computers.

For engineering work stations and Apple computers, the firm is selling the model Q1, which has a two-button control but no speed-control switch and retails for $119. The model Q2 has two buttons and a speed-control switch; it costs $139.

The model Q3 device has 3-button control plus a trackball speed switch and is priced at $149. *–J. Robert Lineback*

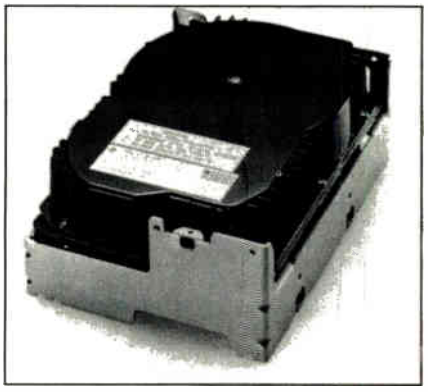
ITAC Systems Inc., 1303 Columbia, Suite 217, Richardson, Texas 75081.
Phone (214) 234-5366 [Circle 342]

DRIVE BOASTS 16-ms ACCESS

A 5¼-in. Winchester disk drive from Hitachi America Ltd. features a 16-ms average access time, 382 Mbytes of storage, and three interface options.

The DK514 achieves its speed primarily by using a voice-coil motor instead of the conventional step motor to position the read/write head. Its data transfer rate is 1.8 Mbytes/s.

Capacity has been doubled over the drive's predecessor, the DK512, thanks



to the use of oxide-coated media to increase bit density and the addition of two platters. Hitachi will manufacture three versions of the DK514, each with a different interface.

Sample units with an ESDI interface are available by the end of June; ESMD and SCSI versions will be available in the fourth quarter. Sample price for the drive is $2,700 each in 100-unit purchases.

Hitachi America Ltd., 950 Elm Ave., San Bruno, Calif. 94066.
Phone (415) 872-1902 [Circle 347]

BUBBLE MEMORY TAKES 30-g SHOCK

Magnesys Inc.'s GearDrive add-on memory storage is compatible with IBM Corp.'s new 7552 Gearbox industrial computer and can withstand up to 30 g of shock and the 0° to 70°C environment of typical factories.

The subsystem consists of removable bubble-memory cartridges that offer between 360 Kbytes and 1.4 Mbytes of storage and a 30-ms average access time.

The 3½-in., half-height units can accommodate two bubble-memory cartridges that contain either 360 Kbytes or 720 Kbytes of storage. The 720-Kbyte units sell for $1,995 each; volume discounts are available. This version is available for volume shipment immediately.

Pricing has not been set for the 1.4-Mbyte version. It will be available in August.

Magnesys Inc., 1605 Wyatt Dr., Santa Clara, Calif. 95126.
Phone (408) 988-1881 [Circle 346]

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In the July 23 issue, the editors of *Electronics* reveal the current state and future directions of 3D graphics technology.

High-performance custom and semicustom ICs. Powerful new arithmetic processors. The advent of 1 Mbit memory technology. All are driving a sudden boom in 3D graphics capability. And the editors of *Electronics* magazine will keep readers on top of important developments with an entire issue coming July 23 devoted to 3D graphics.

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What's more, we'll top off this special graphics package with an in-depth preview of SIGGRAPH, annually the premier forum for new graphics technology and products.

So don't miss this exciting issue. And if you manufacture graphics components or equipment, make sure your advertising message is there when more than 131,000 technical managers and their senior engineering partners turn to find out the latest in graphics technology—in the July 23 issue of *Electronics*.

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Electronics

ELECTRONICS WEEK

BOOK-TO-BILL KEEPS ON CLIMBING

The U. S. semiconductor business continues to look up, posting a book-to-bill ratio of 1.26 for the three-month period ending in May, reports the Semiconductor Industry Association, Cupertino, Calif. That's the eighth consecutive monthly increase, and it returns the industry close to May 1984's level of 1.27. Three-month orders for May, at $1.023 billion, were up 7.4% from April's $953 million and near August 1984's $1.027 billion. Three-month average shipments for May were $812.5 million, up 4% from $781.25 million in April.

CONTROL DATA SOUPS UP CYBERS

Control Data Corp. is moving to reaffirm its position as the leader in mainframe scientific computing, hoping to stave off competition from IBM Corp., which has made inroads in that market since its 1985 addition of a vector facility for the IBM 3090. The new 12-Mbytes/s model 887 Superspeed Disk System for Control Data's top-end Cyber 990E machines is said to be twice as fast as its predecessor and four times as fast as IBM's 3090-200. In addition, version 2 of an automatic vectorizing Fortran compiler boosts CPU performance in the 990E and the dual-processor 995E by 20% to 25%.

IBM SHRINKS ITS SHARE IN INTEL

Intel Corp. has repurchased 8.9 million shares of its common stock from IBM Corp. in a $361.5 million transaction. Armonk, N. Y.-based IBM now owns 13.7 million shares of Intel stock, or 11.5% of the Santa Clara, Calif., company's current outstanding shares—down from 22.6 million shares, or 19%, before the deal. IBM plans to use 7.8 million shares to support the exchange of IBM Eurobonds for Intel stock under a February 1986 offering of IBM exchangeable subordinated Eurobonds; it will hold the remaining 5.9 million shares as a continuing investment in Intel.

APPLE ADDS ADA TO MACINTOSH II

An agreement between Apple Computer Inc. of Cupertino, Calif., and Alsys Inc., Waltham, Mass., will enable Apple to offer the Alsys Ada language compiler with the Macintosh II computer. The U. S. Department of Defense has decreed the use of Ada for all programming related to weapons systems—and, eventually, for all DOD computer resources. Alsys, an established supplier of Ada compilers, will develop one for the Mac II by year's end. The compiler will be Apple's first offering in the Ada market, which now includes NASA, the NATO alliance, and many businesses.

EDS DROPS BID ON U. S. PHONE SYSTEM

Electronic Data Systems Corp. is pulling the plug on its bid for the $4.5 billion, 10-year contract to build the FTS 2000 federal telecommunications system. It was concerned over lawsuits that may further delay a contract award, as well as the unpredictability in telecom markets. Meanwhile, its subcontractor bidding partner, US Sprint Communications Co. of Kansas City, Mo., expects to decide soon whether to pursue the contract with another partner or pull out as well. Sources at General Motors Corp.'s EDS subsidiary in Dallas say uncertainty over the timing and final award of a contract became unacceptable to the operation. The bidding deadline has already been pushed back to July 30 in the wake of AT&T Co. protests over government requirements to guarantee prices and certify that the network is not part of a common-carrier service.

HONEYWELL BULL'S IBM COMPETITION

The first two members of a new large-scale computer family from Honeywell Bull Inc. of Billerica, Mass., are intended to compete with IBM Corp. systems. The DPS 8000/81 is a single-processor system that sells for $675,000 and vies with IBM's 4381-24 dual-processor machine for financial and other applications. The DPS 8000/82, a fully duplicated dual-processor system, sells for $1.3 million and will compete with the low end of IBM's 3090 series in on-line processing. Shipments are scheduled to begin in December.

WANG TO OFFER MICROSOFT OS/2

Wang Laboratories Inc., Lowell, Mass., and Microsoft Corp., Bellevue, Wash., have announced an agreement that allows Wang to sell Microsoft's new OS/2 operating system and Presentation Manager user interface. The software runs on Wang's new IBM PC AT-compatible PC 280 and 380 personal computers, which are based on the 80286 and 80386 microprocessors, respectively.

PASSAGE TO INDIA: 68020-BASED UNITS

As part of a relaxation of export controls on high-technology electronics [*Electronics*, Feb. 19, 1987, p. 96], the governments of the United States and India are permitting Charles River Data Systems Inc. to export to India their supermicrocomputers that include the 16.7-MHz Motorola 68020 chip. The Framingham, Mass., company will ship kits of its Universe family of 32-bit machines to Sunray Computers Pvt. of Bangalore. The Indian firm will then assemble and distribute them. The computers will be used in large-scale real-time applications, such as banking and the management of utilities.

NATIONAL BUSINESS DIRECTORY DEBUTS

About 8,700 electronics and electrical firms are listed in the first national business telephone directory for the U. S. Published by Gale Research Co. for the Nicholas Publishing Co., the *National Business Telephone Directory* contains names, addresses, and telephone numbers for more than 350,000 business and industrial establishments. The 1,903-page book is available from Gale Research Co. at Book Tower, Detroit, Mich. 48226, for $95.

WAVETEK, DATRON: TEST-GEAR MERGER?

Two makers of test and measurement equipment are talking merger. Wavetek Corp., San Diego, and Datron International plc, Norwich, UK, are discussing the possibility of Wavetek's acquiring Datron. The two publicly traded firms presently have joint marketing and research relationships that could continue and be expanded even if the merger talks are not successful. Datron, which also has plants in Florida and California, blames its current operating losses on weak worldwide market conditions.

THE SOUTHWEST COURTS HIGH TECH

The Southwest is doing its best to attract a high-tech crowd by developing links among area universities and advanced-technology industries. According to a recent study by Grant Thornton, a Chicago-based accounting and management-consulting firm, the effort is paying off: the region has been credited with having the best overall manufacturing climate for the second consecutive year.

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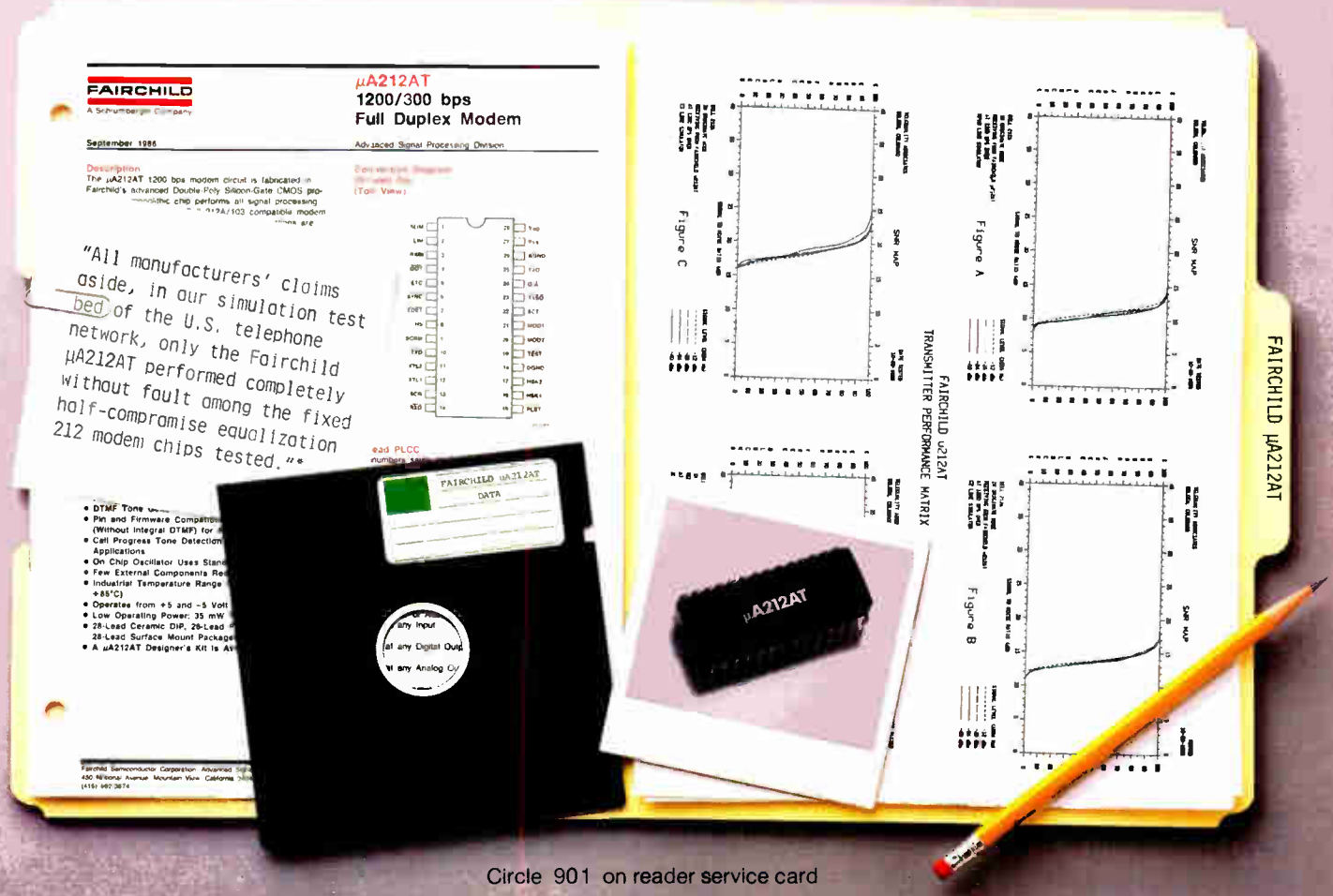

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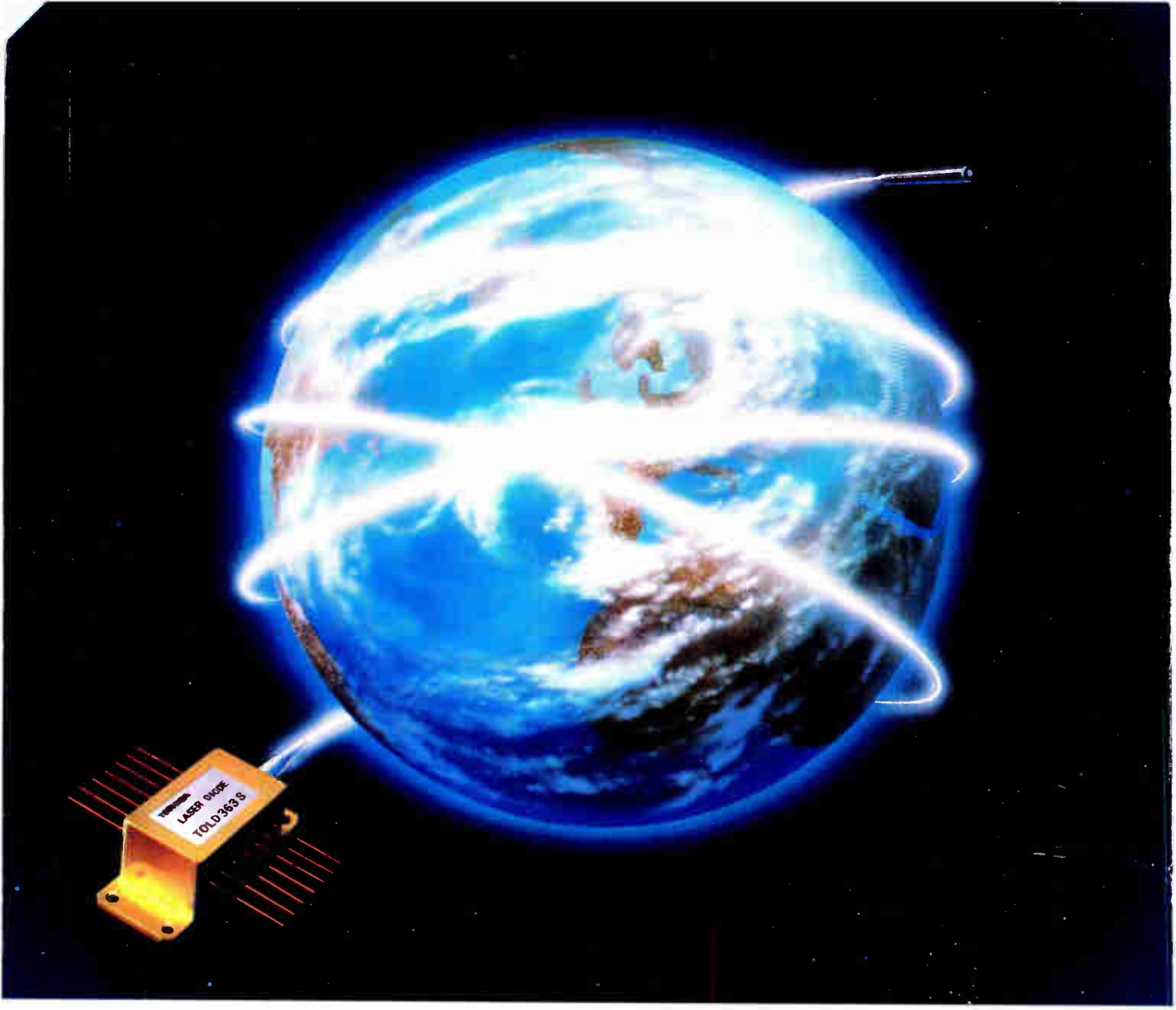

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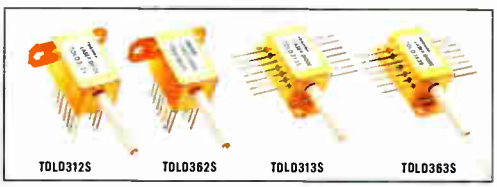

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