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Electronics

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PAGE 59

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Source: Infocorp 1987

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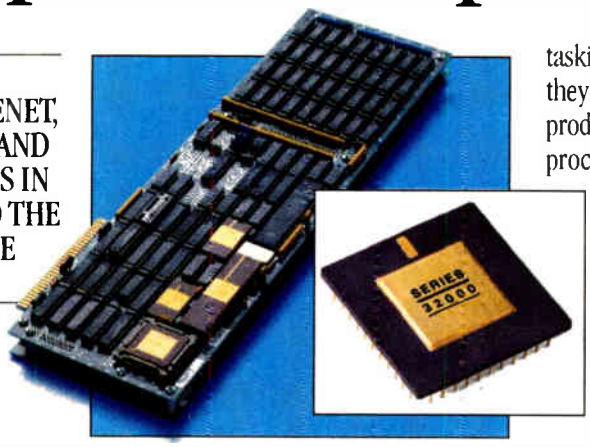

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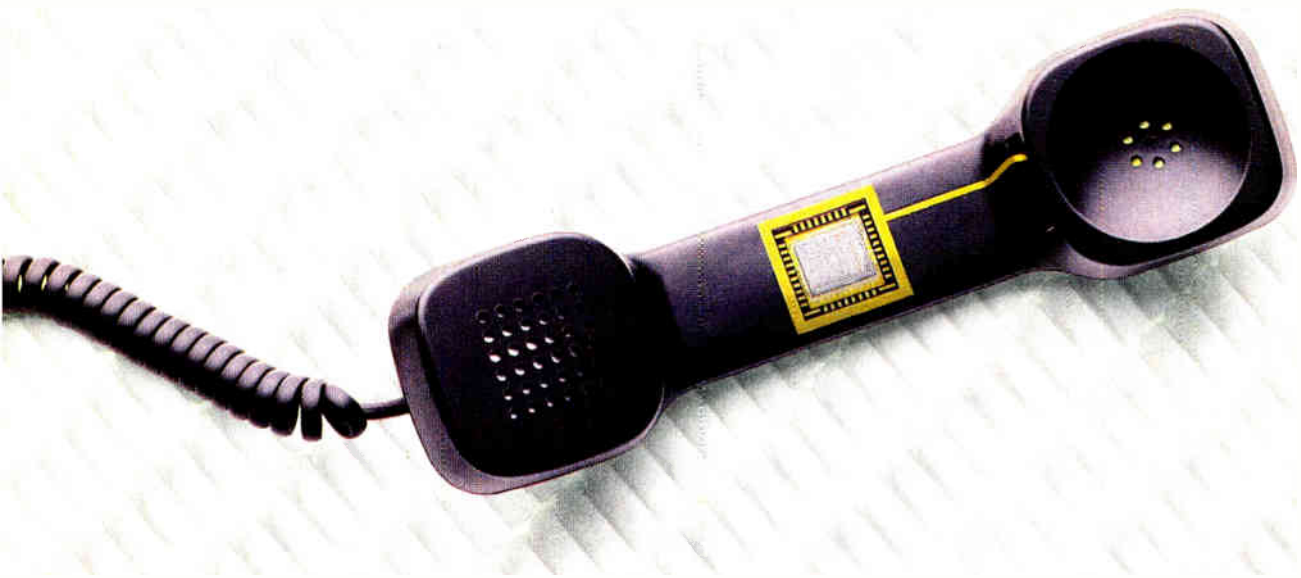

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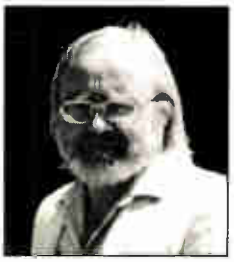

BERNARD C. COLE

Australia? Isn't that the place where all the men look like *Crocodile Dundee*'s Paul Hogan; where uncommon animals like kangaroos and koala bears are abundant, and where the America's Cup was on display temporarily until it came back to the U. S. this year?

That could be an average American's tongue-in-cheek impression of the nation down under if it were based strictly on the promotional and advertising blitz in U. S. movies, magazines, and newspapers during the last year or so. But the savvy engineering manager who reads *Electronics* knows that Australia is no joke. For example, about a year and a half ago we ran an article describing the concern of the leaders of the electronics industry there about their ability to overcome the obstacles encountered by Australia's technology leaders in their attempts to convert their strong research and development base into commercial products [*Electronics*, Sept. 30, 1985, p. 36].

Now, in this issue we present a package of articles that indicates that Australia is on the leading edge of VLSI design, at least in digital signal processors—and at least one company seems to have figured out a way to get its products into the marketplace. The company is custom integrated-circuit manufacturer Austek Microsystems Ltd., which is three years old and started out in DSP's. How it hopes to penetrate the U. S. microprocessor market, and what it will use to accomplish the job, is described in the articles beginning on p. 74.

Although we at *Electronics* pioneered the notion that electronics technology is global, and we are well known among the leaders in the electronics industry as well as in the magazine business for our worldwide coverage, we must admit that even for us, Australia is a bit off the beaten path. But as semiconductor editor Bernard C. Cole tells it, Austek's achievement comes as no surprise.

"I've been tracking the company for quite a while," he says. "The reason is that J. Craig Mudge, who founded Austek, was involved with Carver Mead at the California Institute of Technology in the design of advanced computer-assisted-design tools. Interestingly, the industry is just now beginning to use some of the systems that he worked on." Carver Mead is a pioneer in the field of CAD and the author with Lynn Conway (to tighten the Caltech-Austek relationship even more, she is a member of the company's corporate technology committee) of the seminal *Introduction to VLSI Systems*. Among the strategies that Mead foresees for the semiconductor company of the future is that they should design chips and farm them out to silicon foundries to be manufactured. And that's the way Austek operates.

But Mudge's association with Mead is not the only reason that Bernie has been following the Australian's career. "Mudge was also involved in the design of self-timed logic [*Electronics*, Dec. 9, 1985, p. 42], and since I worked on that article I noticed that Mudge had started a U. S. operation and begun doing standard products. I figured that anything he would do in that area would be worth writing about. I expect Austek to start a string of many impressive products."

Whether or not that prophecy comes true, you can be sure that Bernie will be there to report it, even if he has to fly down under to do the job.

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JUNE 11, 1987

Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

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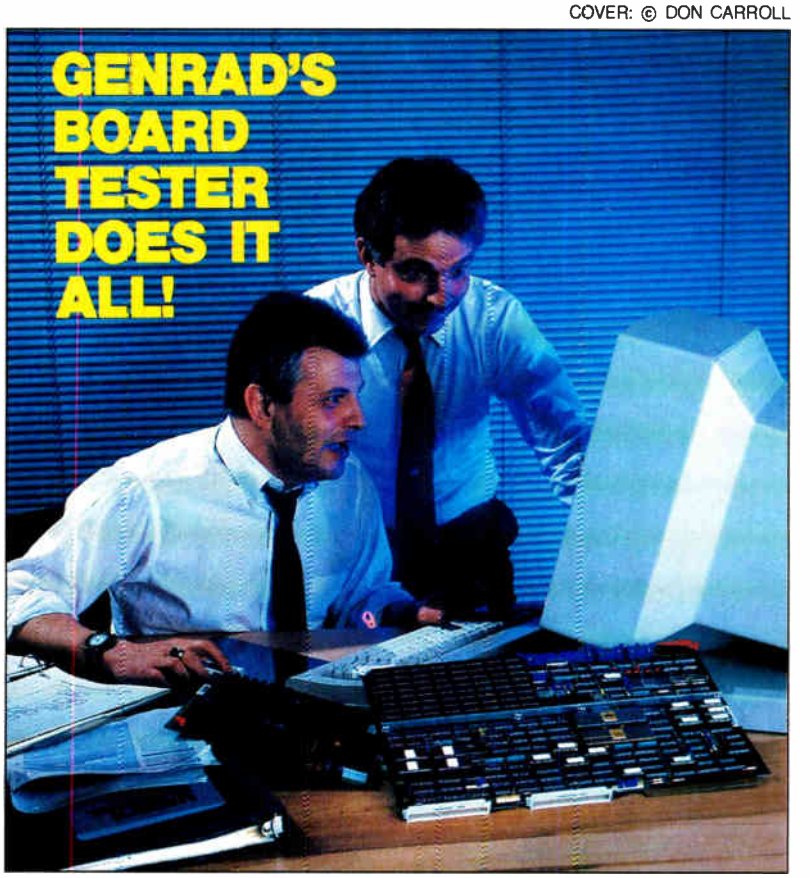

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NEW PRODUCTS

Newsletter, 27
- United Technologies' floating-point chip set suits both commercial and military products
- Artificial-intelligence software from Trimeter Technologies helps trim gate counts in ASIC designs by up to 30%
- Tektronix to cut portable-scope prices, unveil 60-MHz model
- Matsushita's pair of 2-in. floppy-disk drives boast standard 5¼-in. formatting

NCC Preview, 104
- ThumbScan's fingerprint reader restricts access to personal computers and terminals
- Low-end scanner from Kurzweil handles type or graphics

Computers & Peripherals, 107
- Datacube's DSP-1000 helps reduce the risk in developing image-processing systems

Military/Aerospace Newsletter, 99
- The DOD gives software developers more leeway in writing code by revising its software-development standard
- It's full speed ahead for the Unisys-Westinghouse team on Aegis; ITT loses its bid to be the second source
- The growth in spending for military electronics is expected to slow in 1988
- An ISDN demonstration project may lead to an Air Force-wide network; the Army and the Defense Communications Agency are interested too

DEPARTMENTS

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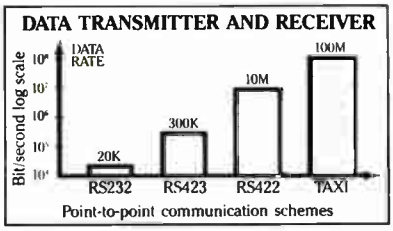

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Device	Access Times
IMS1600 (x1) IMS1620 (x4) IMS1624 (OE, x4) IMS1630 (x8)	35, 45, 55ns 35, 45, 55ns 35, 45, 55ns 45, 55, 70ns

LOW POWER DATA RETENTION CMOS SRAMs		
Device	Access Times	Idr*
IMS1403L (x1) IMS1601L (x1) IMS1620L (x4) IMS1624L (OE, x4)	25, 35, 45ns 45, 55, 70ns 45, 55, 70ns 45, 55, 70ns	0.5µA 10µA 10µA 10µA

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LETTERS

Standards on the horizon

To the editor: I read with great interest "How long will it take image processing to blast off?" [*Electronics*, Feb. 19, 1987, p. 65]. I liked your article and found useful information, such as the chart from the Frost & Sullivan Report.

But in one point, your article does not reflect some recent developments. You wrote that "most participants in the field admit no organized effort is yet under way to set standards for compatible software, image data bases, pixel formats, and digital-video compression." I am happy to inform you that due to increased efforts in standardization, there are good hopes for a successful standardization in a year or so.

I work in two international standardization bodies, ISO TC 97 and CCITT SG VIII, where such standardizations are hot items. To achieve standards in communication of natural images, CCITT SG VIII Question 18 (new image communication) is investigating this issue until 1988. In close cooperation with the CCITT efforts, the ISO TC 97/SC2 Working Group 8 is preparing a series of standards on "Coded Representation of Picture and Audio Information." Part 2 of ISO/DP 9282 will contain the "Encoding Principles for Photographic Pictures" and ISO/DP X3 the "Photographic Picture Functions."

The audience and participants of the ISO group is broader than the CCITT group; it includes the PTTs, the telecom and the newspaper industry, and the data processing world. The work of ISO is heavily concentrated on the evaluation and selection of an image compression algorithm and its coding, whereas CCITT intends to apply the ISO-selected compression method and coding within the scope of CCITT-defined Telematic Services and other applications.

ISO plans to select a compression algorithm by the end of 1987. CCITT plans to have appropriate recommendations out by the end of 1988. It is strongly believed that worldwide standards in the field of picture coding will contribute to a breakthrough in image communication and processing.

Dr. István Sebestyén
Munich, West Germany

Known but not forgotten

To the editor: Incredible! Your article "Graphics Software is on the Move" [*Electronics*, May 14, 1987, p. 81] has no mention of the Amiga, the $1,200 computer that is being used by TV stations for titling, raytrace picture creation, and animation. Please check it out.

Brian Donovan
Delta Research
Palo Alto, Calif.

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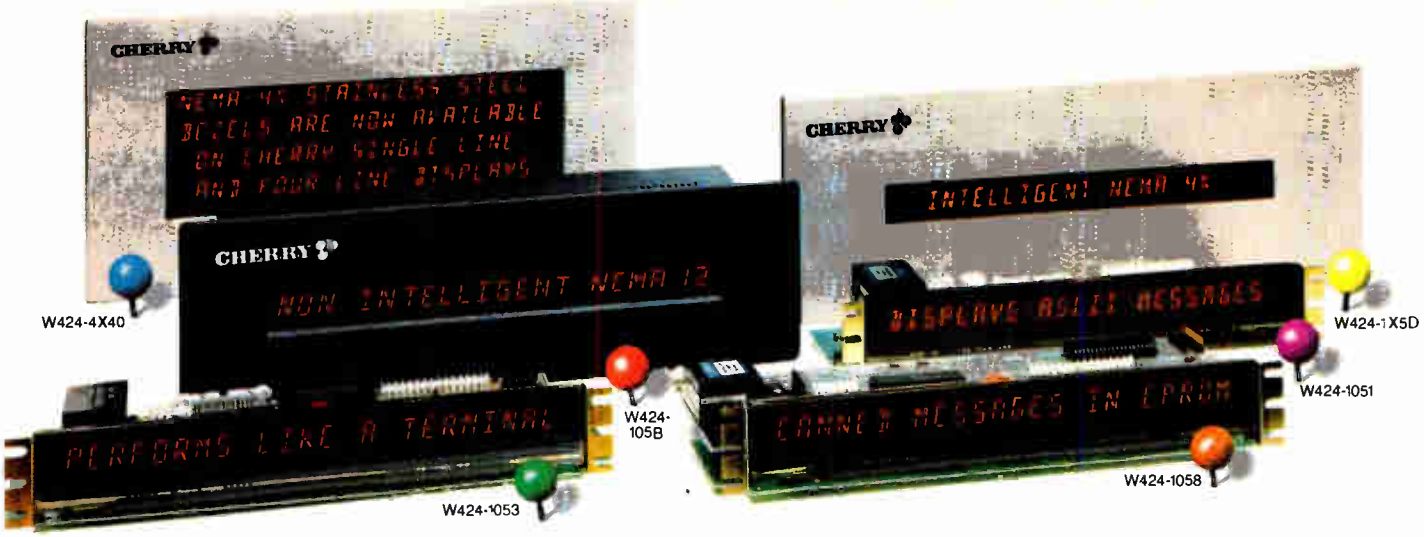

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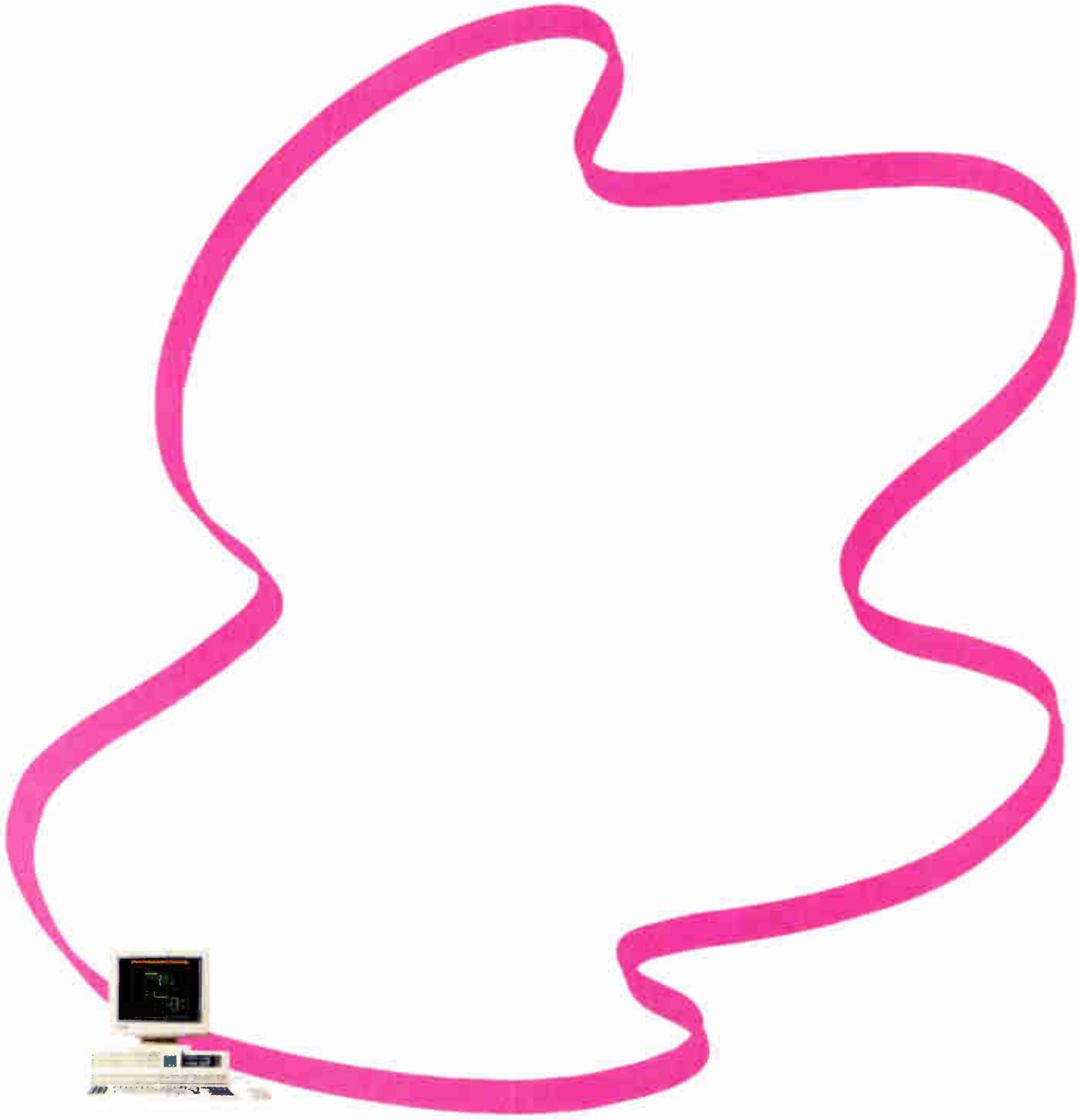

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HOW MACKENZIE'S DEC YEARS WILL HELP DG

WESTBORO, MASS.

Data General Corp. historically was highly effective in moving low-end products to the market through value-added resellers. But now the Westboro, Mass., computer manufacturer wants to reinforce its position in that market by setting up a VAR Marketing and Development Division and by hiring Ward D. MacKenzie as the vice president to head it up.

MacKenzie, 47, comes to Data General from Lisp Machine Inc. That artificial-intelligence company, in Andover and Lowell, Mass., had filed for protection under Chapter 11 bankruptcy laws and then was sold late last month to GigaMos Holdings Inc. of Montreal, Canada. The Canadians beat Data General to the punch; Data General had made an offer for Lisp Machine, planning to make it part of MacKenzie's division.

But his AI experience wasn't Data General's main reason for recruiting him. More important, he brings with him 18 years of experience at Digital Equipment Corp., 16 of which he says bear directly on his new charter. "I've had in my career a continuing interest and experience in the management of distribution through the VAR channel," MacKenzie says, adding that relationships with VARs are special. Indeed, some observers say MacKenzie's hiring is important especially because of his DEC experience, and because both DEC and IBM are neglecting resellers.

"You're dealing with companies that run their own businesses and want to form long-term relationships with vendors that are profitable to both parties," MacKenzie says. Part of the focus of the new division, therefore, will be on developing and strengthening those relationships. But equally important, the VAR Marketing and Development Division is also going to develop products for VAR channels.

The result is that five key executives now report to MacKenzie: Jim Barnes, vice president, Volume Products Division; Mike Taback, division director, Technical Systems Development Group; Art Holmes, division director, Processor Development; John McGlone, acting director, Distribution Division; and Jan Pieter Scheerder, director of systems and product management.

"We've pulled together these key resources because we wanted to make sure that we take a focused look at low-end products—products that sell for less than about $30,000," MacKenzie says. The VAR channel continues to grow rapidly, he notes. Further, powerful new computers that are relatively inexpensive are becoming available and are opening new applications, such as AI, to VARs. This new division provides a focal point to ensure that Data General incorporates advanced technology in low-end systems that will be sold corporate-wide and will be suitable as well for the VAR channel.

LOOKING TO AI. And although Lisp Machine's assets have eluded Data General because of the GigaMos purchase, it's probably safe to say that MacKenzie will continue to evaluate how to incorporate AI into Data General's picture. As Data General president Edson de Castro said in announcing the VAR division, MacKenzie has had "extensive experience in the development of AI solutions for real-time process control in industrial and commercial applications."

Before joining Lisp Machine, MacKenzie's most recent assignment was as vice president for DEC's Volume Group, responsible for managing all channels of distribution for the company's commercial and technical original-equipment-manufacturing and VAR business. His DEC experience also includes several positions in managing sales, marketing, and manufacturing in Europe.

He's excited about his new charter. "DG is a fantastic company with superior technology and resources," he says. "It's also aggressive, and that's a good fit for me." *–Larry Curran*

MACKENZIE: Working to develop VAR relationships and products at Data General.

TEXAS INSTRUMENTS REPORTS ON

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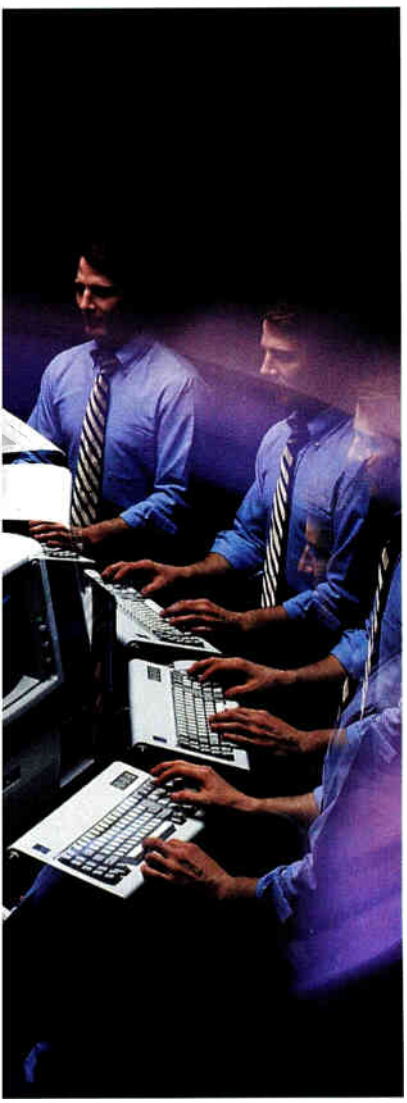

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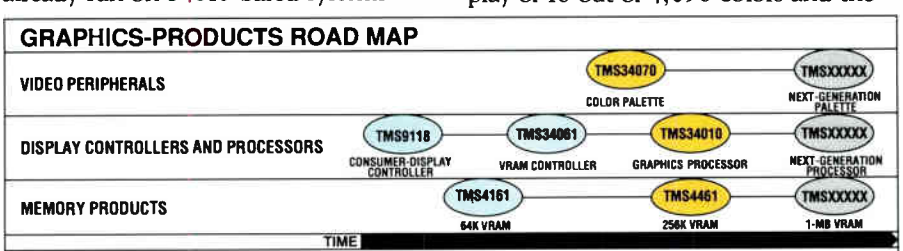
To provide the host bus interface and any other customized functions you may require, TI offers quick design and production turnaround through its Application-Specific Integrated Circuits (ASICs) capabilities.

Development tools are available now for applying the 34010. Turn the page for details. ▶



Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing,

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAFX. In Conn. dial (203) 852-9201.

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26-4537

To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit *(left rear)*, a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives*, are all readily available.

Hundreds of designers must be right. Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

Software Products	Company
AutoCad™	AutoDesk
GSS*CGI™†	GSS
Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
Graphics Development Toolkit™†	IBM
Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™, 1-2-3™	Lotus Development
P-CAD™	Personal CAD Systems

™Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

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64K	P4C187	64K x 1	12		NOW	
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64K	P4C198	16K x 4	20	W/OE	NOW	
64K	P4C198A	16K x 4	20	W/OE & CE2	NOW	
64K	P4C1982	16K x 4	20	SEPARATE I/O	NOW	
64K	P4C1981	16K x 4	20	SEPARATE I/O	NOW	
72K	P4C163	8K x 9	20	300 MIL PKG	SEPT	
16K	P4C116	2K x 8	15	300 MIL PKG	JULY	
16K	P4C168	4K x 4	12		NOW	
16K	P4C169	4K x 4	12	FAST CS	NOW	All this performance—at affordable prices.
16K	P4C170	4K x 4	12	W/OE	NOW	
16K	P4C1682	4K x 4	15	SEPARATE I/O	NOW	
16K	P4C1681	4K x 4	15	SEPARATE I/O	NOW	
4K	P4C147	4K x 1	10		SEPT	
4K	P4C148	1K x 4	10		SEPT	
4K	P4C149	1K x 4	10	FAST CS	SEPT	33% Faster than the closest contender!
4K	P4C150	1K x 4	10	SEP I/O W/RESET	SEPT	
4K	P4C151	1K x 4	10	W/COMPARATOR	SEPT	
1K	P4C422	256 x 4	8		NOW	World's fastest available CMOS SRAM.

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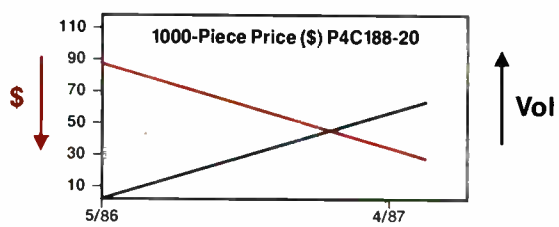

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ELECTRONICS NEWSLETTER

TI READIES ONE-CHIP DSP INTERFACE PERIPHERALS

Texas Instruments Inc. is about to sink its teeth into the potentially huge market for digital-signal-processor interface chips with a new family of monolithic peripherals that act as analog front- and back-end devices. The Dallas company is now offering samples of its first high-performance DSP peripherals, which will be formally introduced this summer. One chip, the 32040, effectively combines the tasks of two earlier interface chips, the 32050 analog input channel and 32051 analog output channel, which were announced in 1984 but dropped after TI concluded that two-chip interfaces were too expensive. The chip is built in TI's 3-μm advanced LinCMOS process and integrates filters, analog-to-digital and digital-to-analog circuitry, digital controls, and other logic. TI plans to have a series of DSP peripherals as part of its new advanced linear thrust [*Electronics*, March 19, 1987, p. 34]. Future DSP peripherals are expected to be made from a new bipolar-CMOS linear process called LinBiCMOS, which sports 20-V power capability. □

FINALLY, A NEW OFFER TO BUY FAIRCHILD: INTERGRAPH IS THE KEY

An offer to acquire a majority share of Fairchild Semiconductor is expected momentarily by its owner, Schlumberger Ltd. The team of prospective buyers—put together after an earlier deal failed—is made up of Intergraph Corp., Fujitsu America, and Fairchild's management, with Schlumberger itself retaining a share. Fujitsu Ltd. had tried to buy an 80% stake in the struggling Cupertino, Calif., chip maker but the deal fell through when two federal agencies warned they would oppose the deal on the grounds that vital chip technology and business was slipping into Japanese hands [*Electronics*, April 2, 1987, p. 31]. Fairchild president Donald Brooks has since brought together his own management team and Intergraph, a Huntsville, Ala., computer-aided-design work-station maker, to dilute Fujitsu's potential stake to a minority share. None of the parties would comment, but insiders say the deal is imminent. Intergraph is an important Fairchild customer, taking a major gamble on the chip maker's new Clipper reduced-instruction-set-computer processor by designing it into a new work station family. □

GM SIGNS SILICONIX TO DEVELOP A NEW GENERATION OF POWER ICs

Siliconix Inc., of Santa Clara, Calif., will develop a MOS power semiconductor technology aimed at automotive applications for General Motors Corp. The 18-month deal with GM's Delco Remy Division in Anderson, Ind., and the GM Research Laboratories in Warren, Mich., is aimed at netting the auto maker a family of lower-loss, lower-cost devices that go beyond current MOS FETS. Siliconix got the nod from GM in part because it is the only power semiconductor maker using 6-in. wafers and doing fabrication in a Class 1 clean room [*Electronics*, Dec. 18, 1986, p. 97]. The first working prototype devices are expected around year's end, and if all goes well, the new technology could be in GM cars by model year 1991. Neither the specific target application nor the value of the contract has been revealed. □

HERE'S A SWITCH: U.S. MAKER TAKES AWAY MARKET LEAD FROM JAPANESE FIRM

A U.S. company has taken the lead away from a Japanese manufacturer in a small but increasingly important market segment in flat-panel displays—solid-state electroluminescent screens. Planar Systems Inc. in Beaverton, Ore., has grabbed a 50% share of this market, pulling ahead of Japan's Sharp Corp., now the runner-up with a 35% share. This market is expected to grow rapidly over the next several years, jumping from about $26 million this year to $270 million by 1991, according to Stanford Resources Inc. □

ELECTRONICS NEWSLETTER

MARANTZ VOWS TO BRING DIGITAL AUDIO TAPE TO U.S. . . .

In a major break from the pack, Marantz Co. of Chatsworth, Calif., says it will go ahead with plans to market digital audio tape players in the U. S. in October—no matter what the opposition. The recording industry has opposed the introduction of the technology in the U. S. because it says DAT could be used to pirate recordings without any degradation in sound quality. It is seeking legislation that would require DAT machines to include circuitry to prevent users from copying prerecorded material [*Electronics*, Jan. 22, p. 30]. "Even if there is no prerecorded software, and even if there are legislative barriers, we will proceed with our marketing plans," says Marantz president James S. Twerdahl. "If need be, we will litigate." The decision—coming from a U. S. company with a U. S. parent, Dynascan Corp. of Chicago—was welcomed by Japanese hardware vendors, who have been reluctant to push the issue in part because of trade friction between the two countries. Japanese vendors are now expected to re-evaluate their plans, and observers predict there may even be some DAT units on U. S. shelves before Christmas. □

. . . AS HITACHI REDIRECTS ITS DAT EFFORT TO DATA STORAGE

Stalled in its efforts to introduce digital audio tape recorders in the U. S. as an audio product, one Japanese company now plans to sell a DAT machine for data storage and retrieval. Hitachi Ltd.'s New Electronic Media Division demonstrated a prototype DAT data-backup system in early June at the Comdex show in Atlanta. Although DAT is a serial medium, the worst-case access time for a 2-hr tape is only 80 s, and the tape's 1-gigabyte capacity should be attractive for applications in computer-aided design, satellite photos, and medical images. Hitachi will make samples available by year's end, and sales will begin in the fall of 1988. Pricing has not yet been set. □

HP LIGHTS UP THE LED BUSINESS WITH BRIGHT, LOW-CURRENT DIODES

Hewlett-Packard's new light-emitting diodes should brighten the future for display designers who have been looking for a high-brightness, low-current diode. HP's family of sunlight-viewable LEDs uses a double-heterostructure aluminum gallium arsenide technology that cuts current drain by 95% over conventional LEDs. The parts are the first lamp and display products specified at only 1 mA—current standard LED products typically require 20 mA to 30 mA. Initial product offerings, which are due out in July, will include discrete LEDs in industry-standard packages and four sizes of seven-segment LED displays. □

MARKET FOR SMALL GROUND STATIONS IS SET TO SWELL

The market for private data-communications networks using Ku-band VSAT (very small aperture terminal) ground stations could swell to better than $100 million by 1990, based on projections from Harris Corp.'s Communication Sector in Melbourne, Fla. The networks can cut communications costs by as much as 20% compared with leased lines. Harris has already begun a pilot program with Montgomery Ward to link point-of-sale terminals for credit verification and inventory control using Ku-band (12-14 Ghz) transmissions. A similar Harris pilot effort is under way at the American Farm Bureau to evaluate video data transmission. Meanwhile, M/A Com Inc., Burlington, Mass., has installed more than 500 such terminals, with customers including Southland, Wal-Mart, and Schlumberger. VSATs range in price from $8,000 to $15,000, and Harris officials estimate the market could reach 1,000 networks, or 80,000 earth stations, by 1990. □

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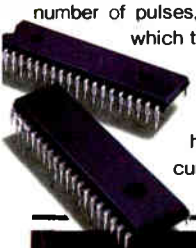
ELECTROSTATIC DISCHARGE SIMULATOR

A testing machine designed to simulate electrostatic discharge which may occur between a charged body such as human body and electronic equipment.

ELECTROSTATIC DISCHARGE SIMULATOR FOR SEMICONDUCTORS

Automatic test equipment designed to simulate the electrostatic discharge which may occur between a charged body and a semiconductor. Presetting the voltage to be applied, the number of pulses, and the pins to which the voltage will be applied allows testing to be carried out with a high degree of accuracy.



ESS-910G

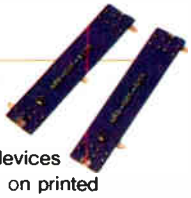
LIGHTNING SURGE SIMULATOR

Test equipment designed to simulate lightning surges which may damage low voltage control circuitry. This equipment facilitates surge testing (such as FCC Part 68, paragraph 68-310) by superimposing a transient signal directly onto the power supply line.

NOISE CANCELER TRANSFORMER

A transformer designed to protect against impulse, lightning surge, and electrostatic discharge.

NOISE CANCELER



Devices used to reduce noise on printed circuit boards. These devices can be mounted on printed circuit boards in the same manner as integrated circuits, or mounted on loaded printed circuit boards as an additional element.

POWER LINE DISTURBANCE DETECTOR

Connected to the power supply line, NDR-544 monitors supply voltage fluctuations (simultaneously on AC line and DC line), frequency variations, and impulse noise.

IMPULSE NOISE SIMULATOR

Test equipment designed to determine electronic equipment tolerance to transient signals which may superimpose on the power supply lines.

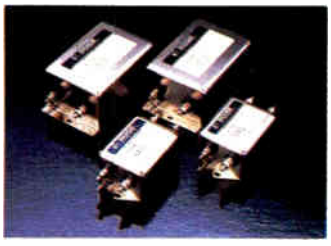
NOISE COUNTERMEASURING EQUIPMENT

This model is provided to take proper noise preventive measures for P.C.Bs loaded with CPU, I/O and RAM.
It consists of impulse noise generator, electric potential measuring unit and counter plane.

NSR-S10

VOLTAGE DIP SIMULATOR

Test equipment designed to simulate a momentary voltage drop or the momentary power failure which may occur on a commercial power supply line and adversely affect sensitive electronic equipment.



IMPULSE NOISE FILTER

A high performance filter to suppress power-line noise which may adversely affect the operation of electronic equipment. These filters also prevent noise produced by the equipment from superimposing signals on the power supply line.

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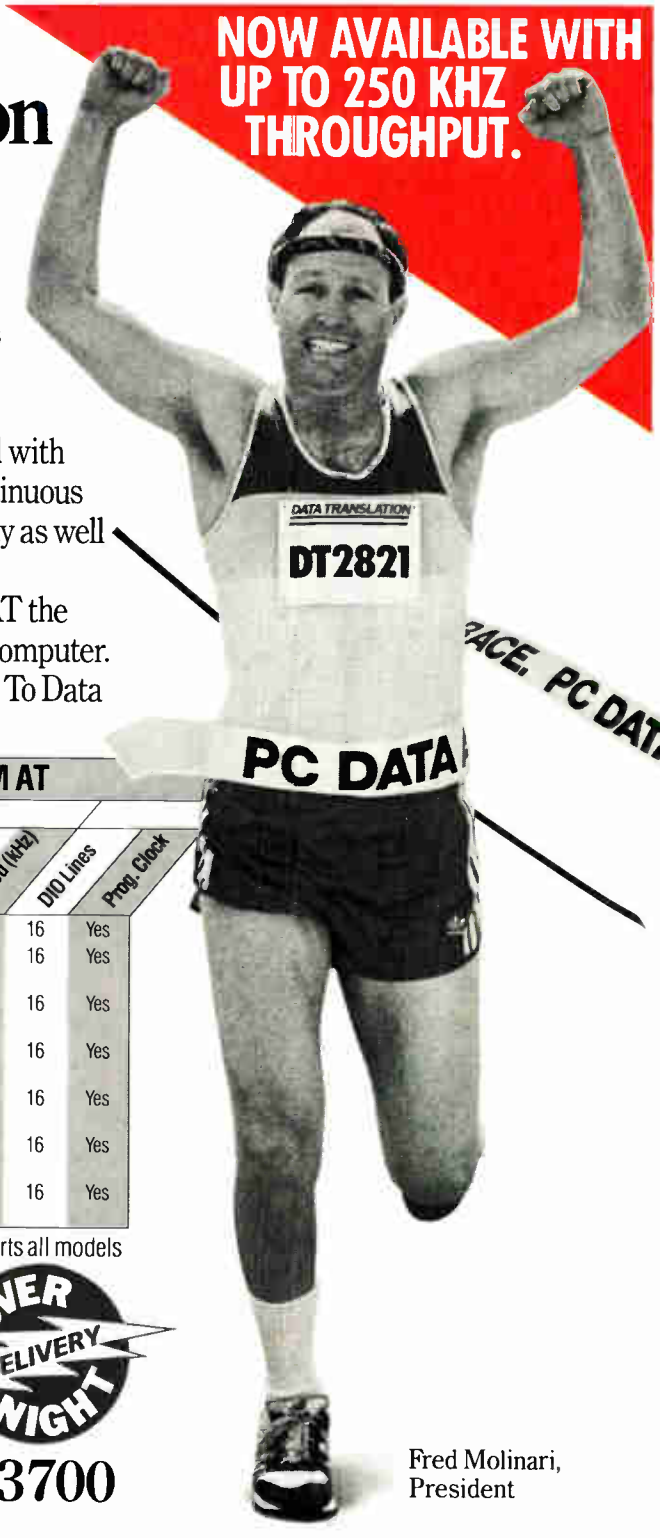

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DT2821-G Very High Speed	2995	16SE/8DI	12	250	2	12	130	16	Yes
DT2823 High Resolution	2795	4DI	16	100	2	16	100	16	Yes
DT2825 High Gain	1445	16SE/8DI	12	45	2	12	130	16	Yes
DT2827 16-Bit High Speed	2495	4DI	16	100	2	12	130	16	Yes
DT2828 Simultaneous Sample & Hold	1995	4SE	12	100	2	12	130	16	Yes

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Circle 26 on reader service card

PRODUCTS NEWSLETTER

SUPER-PURE GaAs WAFERS OPEN DOOR TO FASTER SUPERCOMPUTERS

Gallium arsenide wafers being grown by a French company boast defect densities of 100 defects/cm², five times better than previous wafers, the company claims. The wafers open the door to faster supercomputers and a new technology of 4- and 16-Kbit GaAs static random-access memories. Picogiga SA achieves a 60% yield for its high-purity wafers with a carefully refined molecular-beam-epitaxy technology and very stringent selection criteria for the substrate, says president Lihn T. Nuyen. The layers are 1-μm undoped p-type GaAs, 5-to-60-Å undoped GaAlAs, and 500-to-1,000-Å silicon-doped GaAlAs on a semi-insulating substrate [*Electronics*, March 5, 1987, p. 38]. Among the first customers were contractors on the U. S. Mimic (Millimeter/Microwave Monolithic IC) program, along with Japanese and European companies building direct-broadcast satellite antennas. Picogiga is currently shipping 50 super-pure wafers a month carrying price tags of $3,500 for a 2-in. wafer and $4,000 for a 3-in. wafer. Prices are negotiable with orders of 500 wafers or more, says Nuyen, and prices should drop by a factor of five in late 1988. Picogiga is headquarterd in Les Ulis, France, and has an Oxnard, Calif., subsidiary. □

DAISY'S ROUTER GIVES PC-BOARD DESIGNERS EXPERT HELP

Expert-systems techniques integrated into Daisy Systems Corp.'s Star printed-circuit-board router let designers sit back while the software does the routing plan, selects routing sequences, and completes virtually 100% of the routing on most boards. In one pass, for example, it might route layers without vias, followed by another pass adding vias. Still another pass might route traces diagonally to reduce trace lengths. Finally, Star's manufacturing router optimizes interconnections to make the board easier to manufacture. Available this summer, Star costs $12,000 for Daisy's Personal Logician and Logician workstations. Versions for IBM Corp.'s PC AT and Digital Equipment Corp.'s MicroVAX II cost $8,000 and $18,000, respectively. □

PC-BASED MICROCODE DEVELOPMENT SYSTEM IS 80% CHEAPER

Step Engineering Inc.'s MicroStep microcode development system provides all the tools needed for small projects such as programming bit-slice microprocessors, but costs 80% less than the $20,000 work-station systems now used. Step's $3,695 entry-level system lacks the computing power and memory of its high-end counterparts, but runs on the IBM Corp. Personal Computer XT, AT, or compatibles. It includes a control-software package and a plug-in card containing a 25-ns writable-control-store memory with a capacity of 4,096 128-bit words, program-execution control, and break-pointing hardware. An optional software package, the MetaStep microprogram language system, raises the price to $6,195. The products are available now from the Sunnyvale, Calif., firm. □

DEC/CRAY TEAM WHIPS UP A 3-MBYTE/S GATEWAY

Digital Equipment Corp.'s VAX computers and Cray Research Inc.'s supercomputers can now exchange data at 3 Mbytes/s—five times the rate of current-generation gateways—thanks to the VAX Supercomputer Gateway. Jointly developed by DEC and Cray, the device is based on the VAX 8250 processor. The gateway also simplifies access to Cray supercomputers, allowing supercomputer applications to run on DECnet local-area networks. Besides the processor, the gateway includes a 70-Mbit/s VAXcluster interconnection, a 10-Mbit/s Ethernet interconnection, licenses for VMS and DECnet, and three standard DEC interconnects: CI, NI, and BI. Slated for delivery this summer, the VAX Supercomputer Gateway costs $180,000. □

PRODUCTS NEWSLETTER

UTC'S FLOATING-POINT CHIP SET CAN GO COMMERCIAL OR MILITARY

Designers looking for a way to develop 32-bit computers that can sell in both commercial and military markets now can get a floating-point chip set that both satisfies military requirements and conforms to popular commercial math formats. The United Technologies Microelectronics Center's UT 1732 multiplier and UT 1733 ALU perform 10 million floating-point operations/s in a pipeline mode or 5 megaflops in flow-through operation over the full military temperature range of −55° to +125° C. The CMOS chips not only meet military 1750A specifications (see p. 93), they also will be the first floating-point chip set in full compliance with military 883C processing standards, say executives at the Colorado Springs subsidiary of United Technologies Corp. At the same time, the chips perform according to the IEEE-1754 format, can do 32-bit floating-point math in modes compatible with Digital Equipment Corp. VAX computers, and are compatible with Weitek Inc.'s 1232 and 1233 chip set. Available in July in 68-pin ceramic packages, each chip will cost $650 in 1- to 99-piece quantities. □

AI SOFTWARE HELPS TRIM GATE COUNTS IN ASIC DESIGNS BY UP TO 30%

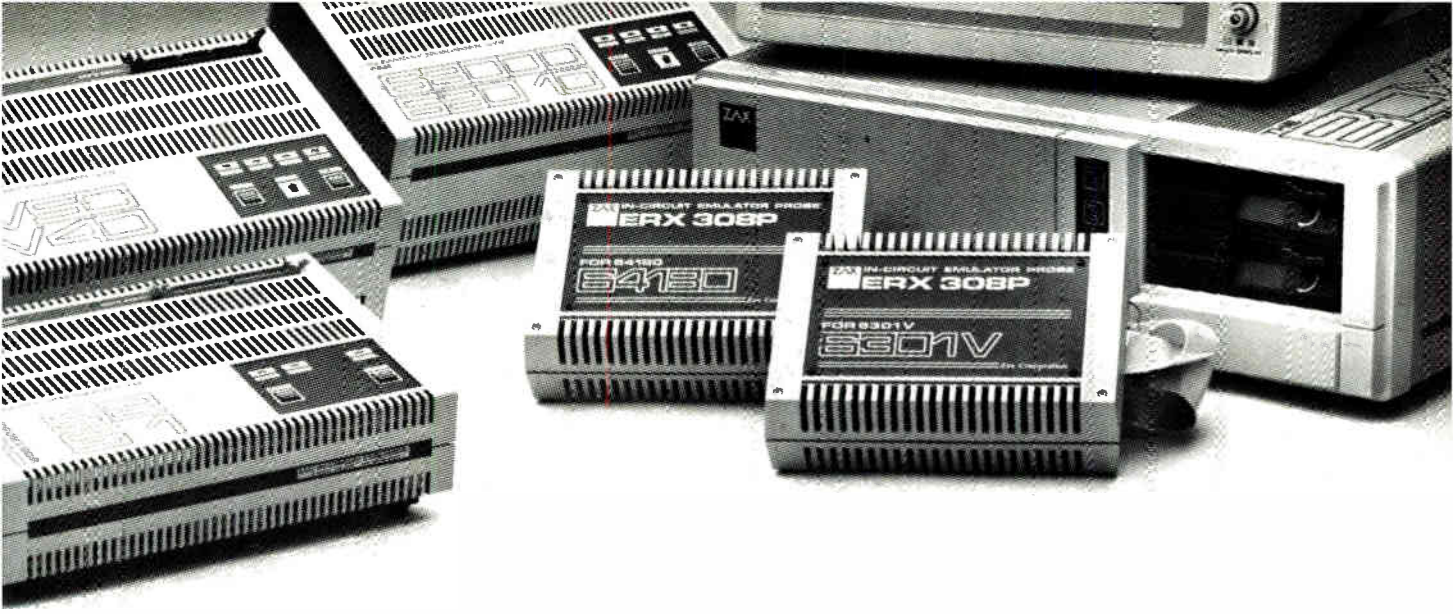
Logic designers can cut the gate counts of application-specific ICs by as much as 30% with Trimeter Technologies Corp.'s artificial-intelligence-aided software. Given a functionally correct design, the company's Logic Consultant first reduces combinational logic with Boolean algebra techniques, then applies an expert system to optimize cell selection from the user's ASIC library—all without changing circuit functionality. Running in another mode, it maximizes the circuit's propagation-delay performance. Available now, the Pittsburgh, Pa., startup's software runs on Mentor Graphics Corp. work stations and costs $30,000. □

TEKTRONIX TO CUT PORTABLE-SCOPE PRICES, UNVEIL 60-MHz MODEL

Look for Tektronix Inc. to strike back at overseas competition in the portable-oscilloscope market next month by cutting prices on its 2200 series and introducing a new family member. The Beaverton, Ore., company will drop the price of its 60-MHz 2220 digital scope from $4,150 to $2,995, and of its 100-MHz 2230 from $5,150 to $4,995—effective on orders for delivery after July 6. The new 2221, at $3,995, offers a 60-MHz bandwidth, envelope detection, cursor-controlled readout of voltage and time parameters, and other signal-processing features that the 2220 does not have. Tektronix says the price cuts derive from the economies of high-volume production on automated assembly lines, and that more price cuts are coming. □

MATSUSHITA 2-IN. FLOPPY DRIVES BOAST STANDARD 5¼-IN. FORMATTING

A pair of 2-in. floppy-disk drives from Matsushita Communication Industrial Co. follow the same read/write formats as standard 5¼-in. drives for easy integration into laptop computers and other systems where space is at a premium. But the JU-202 packs an unformatted capacity of 1 Mbyte (720 Kbytes formatted) onto 80 tracks/side, and the JU-201 offers 500 Kbytes unformatted (360 Kbytes formatted) on 40 tracks/side. Engineers at the Yokohama, Japan, company reduced the size of the disk hub to provide the same number of tracks as the 5¼-in. disks. Using a standard number of tracks sets these drives apart from Sony's 2-in. disk system, which uses 50 tracks on one side [*Electronics*, May 28, 1987, p. 100] and has a formatted capacity of 0.8 Mbytes. Matsushita's drives have a CMOS interface, consume 1.5 W from a single 5-V power supply, and can be used with currently available 5¼-in. disk controllers. Both drives will be available in Japan at a sample price of 14,500 yen in October; the company will fill offshore orders, but its prime target is the Japanese market. Matsushita expects to have disk samples available in October as well. □



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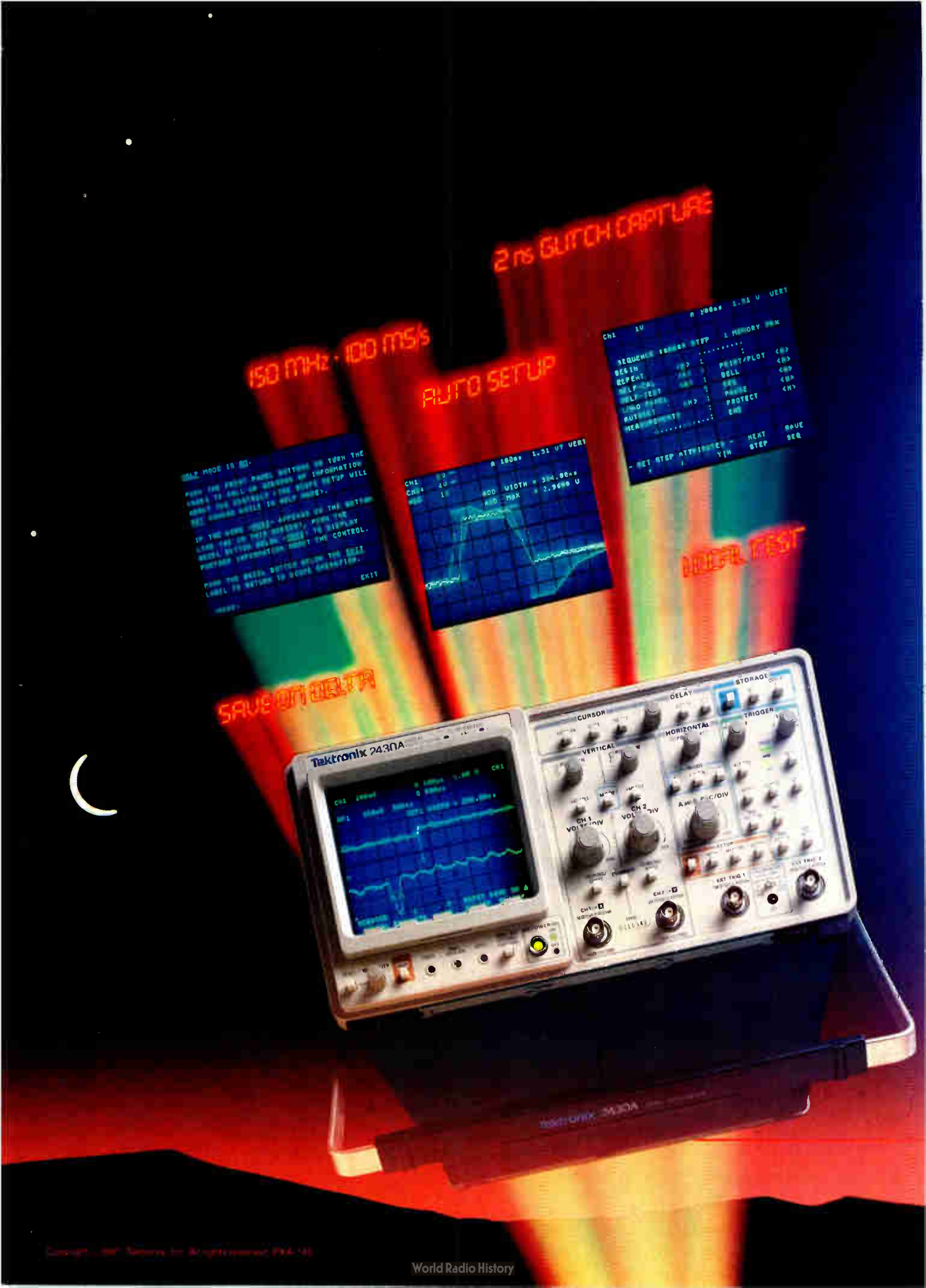
Circle 29 on reader service card

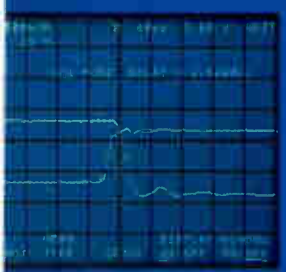


NEW TEK 2430A DIGITAL SCOPE. TODAY'S STANDARD.

(Opposite, left) The 2430A's onboard Help function ensures ease of operation for the new or infrequent operator. No more looking for that misplaced manual.

(Opposite, center) Join Save on Delta's pass/fail capability with Waveform Parameter's specific measurements.

(Opposite, right) AutoStep, a 2430A standard feature, lets you build and run automated or semi-automated test procedures from the front panel.

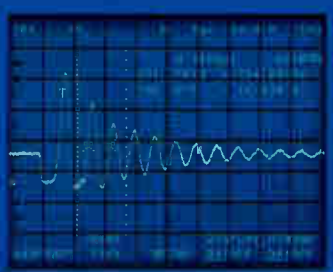


Now you can make automatic channel-to-channel propagation delay measurements with user-defined thresholds. Shown above is a propagation delay measurement from the mesial (midpoint) of the ECL rising edge on Channel 1 to the mesial point of a TTL falling edge on Channel 2. Display the waveform and read out the values on screen or over the bus.

The new, 150 MHz Tek 2430A is a superb combination of familiarity and innovation. You can digitize, view and store fast, complex signals with the proven performance of a scope built for solving tough design problems.

The 2430A with its familiar front panel and simple, one-level menus drives like the analog scopes you're used to. And powerful Local Test™ features put less time between you and results. Now you get scope setup in seconds, faster measurements and test procedures *built right from the front panel.*

The 2430A offers the highest performance for the price of any scope in its class. No other portable digital scope lets you capture elusive glitches as short as 2 ns at all sampling rates, automatically catch intermittent failures in babysitting applications using patented



Waveform Parameter Extraction allows you to make specific measurements on the windowed portion of a waveform. Here, frequency and peak-to-peak voltage measurements are made on two cycles of a damped sinewave. The cursors set the limits of the window.

Features	
Dual-Channel Bandwidth	150 MHz
Digitizing (Sampling) Rate	100 MS/s
Record Length	1K
Vertical Resolution	8 Bits
Time-Base Accuracy	0.001%
Peak Detection	10ns (2 ns)
Printer/Plotter Out	Tek HC100 Color Plotter, HP ThinkJet™, HP 7400 Series
GPIB	Standard (talk/listen)
Price	$8000

Save on Delta, and see waveform changes virtually *as they happen* thanks to the 2430A's high update rate.

New Local Test features mean fast, accurate, automatic answers. Auto Setup takes the trial and error out of scope setup. Just one button sets up the 2430A to acquire and automatically display unknown input signals as you probe multiple points on a circuit. Auto Setup also simplifies your preparations for specific measurements.

With new Waveform Parameter Extraction you can characterize waveforms instantly. Freeze 20 different waveform measurements on-screen at the touch of a button—or select four parameters for live update. Propagation delay between two signals is included.

And in just minutes with new AutoStep you can build a test routine from the scope front panel. Simply recall the sequence to debug a stack of prototypes.

It's all part of the most complete scope for product design. Features include extensive and easy-to-use triggering and direct hard copy output. Plus optional word recognizer and video triggering. On-screen operating instructions are at your fingertips—even when the manual isn't—with the 2430A's new Help Mode.

And you can take advantage of standard GPIB and off-the-shelf software to fully automate measurements and extend waveform analysis.

The 2430A's reliability is backed by a 3-year warranty. A variety of low-cost service plans can extend coverage even longer.

See the priced-right, standard-setting 2430A. Call your Tek sales engineer for a demo. For a free video demo or literature, or to find our sales office nearest you, call Tek direct:

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Circle 31 on reader service card

Tektronix

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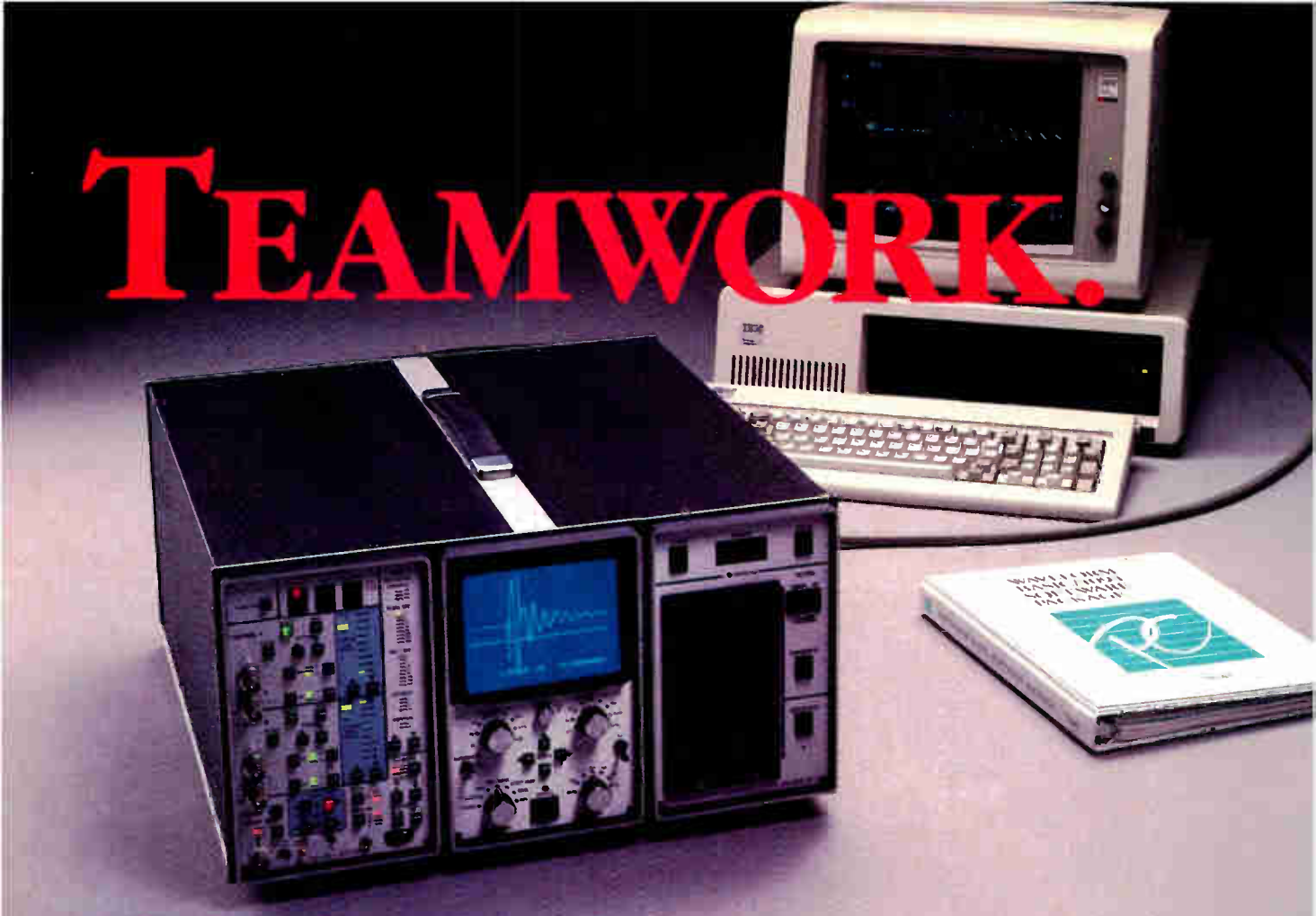

TEAMWORK.

Combine the waveform capturing abilities of a Nicolet digital oscilloscope with the computing abilities of your IBM PC.

Connected via the RS-232 or the IEEE-488 (GPIB) interface, the power of modern signal analysis can be easily realized.

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The Scopes. Nicolet digital oscilloscopes offer ten times the accuracy and as much as one hundred times the resolution of analog oscilloscopes. A wide range of digitizer speeds provide solutions for virtually every measurement problem. Our latest plug-in module, the 4570, has 12-bit resolution at the unprecedented digitizing speed of 10 MHz. Accuracy does not have to be sacrificed for speed! Neither does sweep length. Waveforms composed of up to 16k data points are available regardless of the speed. Cursor readout of measurement values, "zoom" expansion to X256, continuously variable pretrigger data capture, and built-in disk drives all contribute to Nicolet's measurement expertise.

From low cost portables to high performance laboratory systems, Nicolet digital oscilloscopes were the first and are still the best.

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The Software. Powerful, easy to use software packages are available for every Nicolet scope. Data transfers into the PC as well as mathematical data manipulation (FFT, integration, RMS, multiplication, etc.) can be accomplished without programming or computer expertise. Waveforms can be displayed on the PC screen, stored on the disk drive, and plotted on paper. The powerful new Waveform BASIC program can also operate as a waveform manipulation *language*. Using commands similar to standard BASIC, customized waveform calculations can be written quickly and easily.

Capture, analyze, store, and plot data with the convenience and ease of a Nicolet oscilloscope and Nicolet software.

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Electronics

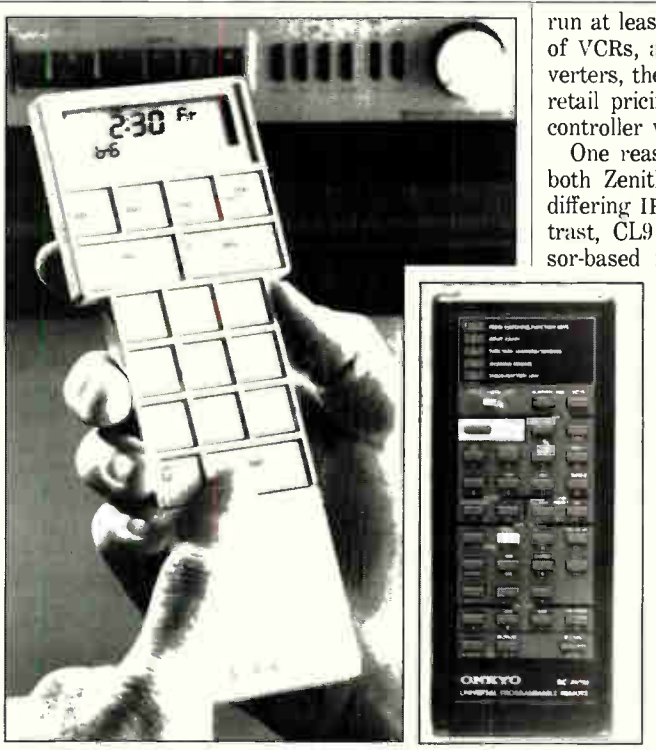
THESE REMOTE CONTROLLERS RUN ALMOST ANY CONSUMER PRODUCT

HAND-HELD IR UNITS HANDLE DOZENS OF PRODUCTS—FROM TV TO HI FI

CHICAGO

As consumers keep buying television sets, video cassette recorders, compact-disk players, and other electronic gadgets, the proliferation of incompatible, hand-held remote-control units—one for each unit—can make for clutter, confusion, and inconvenience. Now a handful of manufacturers, led by a startup, are marching into what they hope will be a profitable new market for a universal remote controller that can run all of this gear.

The startup is headed by Steve Wozniak, a cofounder of Apple Computer Inc. He spotted the problem more than two years ago and now says his new company, called CL9, will start volume deliveries in July of a product it calls CORE (for controller of remote electronics). Some two years in development, CORE is a unit that can be programmed to run any consumer video or audio electronic system equipped for infrared remote control.



UNIVERSAL TURN-ON. The universal remote controller from CL9, left, will sell for $199. The version from Onkyo carries a $119.95 price tag.

CL9's marketing target is the upscale consumer who owns $2,000 to $10,000 worth of electronics gear. The Los Gatos, Calif., company believes this consumer will be willing to shell out $199 for a controller that runs any TV or audio system.

But Wozniak is in for tough competition in his bid to save America from coffee-table clutter. At the Summer Consumer Electronics Show in Chicago in early June, several vendors unveiled their own hand-held IR remote-control units, which also are compatible with different makes of equipment. The other units don't match the sophistication of the CL9 system, which is built around two microprocessors and has only 17 function-control keys (additional programming keys are hidden when not in use). But most of its competition will be far less expensive: one, in fact, will cost less than $50.

New units from Zenith and Magnavox will handle only video components, in which IR remote is more common than with audio equipment. Others, such as Onkyo's new controller, will go after the same multibrand video and audio remote-controller market that CL9 is targeting.

At Zenith Sales Co., a division of Zenith Electronics Corp. in Glenview, Ill., Bruce A. Huber believes universal remote controllers have mass-market potential. "I don't think anybody is trying to forecast the depth of this market, but it seems like an idea whose time has come," says Huber, the marketing vice president. "We don't get interested in anything unless we think we can make tens of thousands of them. We're almost thinking of bubble packaging these things and selling them off a rack."

The Zenith Personal Control Center, a universal wireless remote-control unit introduced in May for sale to cable-TV vendors, will also be sold through retail outlets starting in the fourth quarter. It carries a custom chip that enables it to run at least 18 color TV brands, 19 kinds of VCRs, and eight brands of cable converters, the company says. And although retail pricing has not yet been set, the controller will cost "well under $50."

One reason for the low prices is that both Zenith and Magnavox program in differing IR codes at the factory. By contrast, CL9 and Onkyo use microprocessor-based intelligence that enables consumers to "teach" the unit to control a variety of video or audio systems. The teaching is done by placing the unit head to head with the remote controller of the system to be learned, and pressing appropriate buttons on each.

Onkyo will offer its unit—the Unifier model RC-AV1—as a separate accessory priced at $119.95. When bundled with two new Onkyo receiver models, the TX-82M and the TX-84M, the unit will sell for $80. At those prices, the Unifier "won't contribute significantly to the bottom line," says David Birch-Jones, national product manager at Onkyo U.S.A. Corp. But he sees the universal controller as a way to sell more Onkyo components. "I think that by the end of the year, you'll see maybe a dozen companies offering this kind of product," he adds.

Magnavox is looking to universal remote control as a way to sell its own equipment. Last year it bundled with some of its TV sets a universal remote controller that runs different makes of VCRs and cable boxes; at the Chicago show, it unveiled an upgraded version that will not only be featured with 45% of all 1987-88 Magnavox TV sets but will also now be offered as a separate accessory. It runs 32 brands of VCRs and 16 brands of cable boxes. Known as the Universal Remote control, it carries a suggested retail price of $99.95.

For its part, CL9 is counting on the sophistication of CORE to gain sales in the face of lower-priced competition. For example, CORE is billed as the only programmable master controller that incor-

porates a real-time clock for preprogramming individual components for unattended operation. It also boasts a macro-entry function that can reduce to a single keystroke a sequence of up to 259 separate commands for functions such as turning on and making adjustments to a number of electronic components.

What's more, CL9 is planning to introduce accessories, including a telephone cradle that will let users operate the controller remotely.

CL9 president Sam Bernstein—Wozniak is chief executive officer—expects industry sales of universal remotes to total perhaps a half million units over the next 12 months, with about a one-fifth share going to CL9. "There's a universe of 40 million to 50 million households that already have two or more remote controllers, and we think that number will be expanding rather dramatically," Bernstein says. "This won't be just a fad." *–Wesley R. Iversen*

NETWORKS

DATA GENERAL TAKES A BIG STEP IN NETS

WESTBORO, MASS.

These have not been the best of times for Data General Corp. The Westboro, Mass., computer maker lost $29 million last year as revenues reached $1.268 billion, less than 2.5% over totals for 1985, when profits were $24 million. And adding insult to injury, archrival Digital Equipment Corp.'s sales and earnings have soared.

But Data General has been fighting back, moving into the business of applications-driven information systems as it maintains its traditional role as supplier of equipment to OEMs. On June 2 it took a giant step along that road when it unveiled an architecture linking personal, midrange, and mainframe computers that puts it into the local-area-network business and gets it out from under DEC and IBM Corp.

Called DG/PC*I, or, for convenience, PC Integration, the networking architecture links Data General, IBM, and IBM-compatible personal computers to Data General's portables and MV family of departmental computers, and with its DS family of engineering work stations. It supports standard operating systems, such as MS-DOS, and protocols for both wide- and local-area networks. What's more, Data General will design, install, operate, and maintain systems—a new tack in customer support that IBM also is taking.

"Data General will be able to network to IBM, and while IBM and DEC say they can network to each other, they really don't encourage that," says market analyst Susie Peterson of First Boston Corp. in New York.

PC Integration fits into a corporate game plan that includes long-standing support for IBM's Systems Network Architecture, which links departmental computers and mainframes. PC Integration is also the first major move since Data General set up a Communications Systems Group under senior vice president Colin Crook a year ago.

Crook's group will emphasize support for industry standards, such as Open Systems Interconnection, MS-DOS, and Ethernet. He says that will separate Data General from DEC, with its DECnet approach, and IBM with its SNA; both of these are essentially proprietary rather than open systems (although DEC also supports Ethernet).

The PC Integration strategy includes three networking options: DG/Starlan, 802.3 Ethernet, and 802.3 Thin Ethernet. DG/Starlan is a Data General baseband LAN that uses voice-grade twisted-pair cable with 1-Mb/s bandwidth. Joseph Forgione, group manager for communications product marketing, says this option is suitable for most office applications, especially where wiring-installation economy is a consideration.

Network architecture links its portables, minis, and work stations to IBM PCs

Using DG/Starlan, work stations are connected to the network through point-to-point links to an external hub unit, which provides collision-detection and signal-repeater functions. Forgione says that hub units can be connected to other hubs, up to five deep, to create a branching-star physical topology and a logical-peer network. An MV-family processor will usually serve work stations connected through down-line hubs.

The 802.3 Ethernet network options offer 10-Mb/s bandwidth and support standard (10BASE5) or thin (10BASE2) Ethernet cable. Thin Ethernet uses a thinner, less expensive cable—but over limited distance compared with standard Ethernet. Appropriate controller boards for the type of network chosen are included in PC Integration products.

The communications software is the Workstation Transport System, which resides on the work station or personal computer to allow applications running on different nodes to make connections and exchange data. The server/departmental-computer side of the link contains previously available communications software called XTS.

Small systems encompassed by the new architecture include Data General's DG/One portables, Dasher intelligent terminals, plus the IBM PC/XT, AT, and "almost any IBM PC-compatible computer that uses MS-DOS or PC-DOS," Forgione says. The larger systems embraced under PC Integration range from the Eclipse MV/4000 all the way to the high-end MV/20000, as well as the MV/2000 DC office computer and the DS/7500 engineering work station.

Crook acknowledges that firms such as AT&T Co. (supporting the Integrated Services Digital Network), DEC with DECnet, and IBM offering SNA have been installing networks longer than Data General. But he believes his network-services team will bring more objectivity to customers' network needs. "[We] have experience in all those disciplines," he notes, "and may be able to make suggestions with less obvious commercial bias about how they can work together."

–Larry Curran

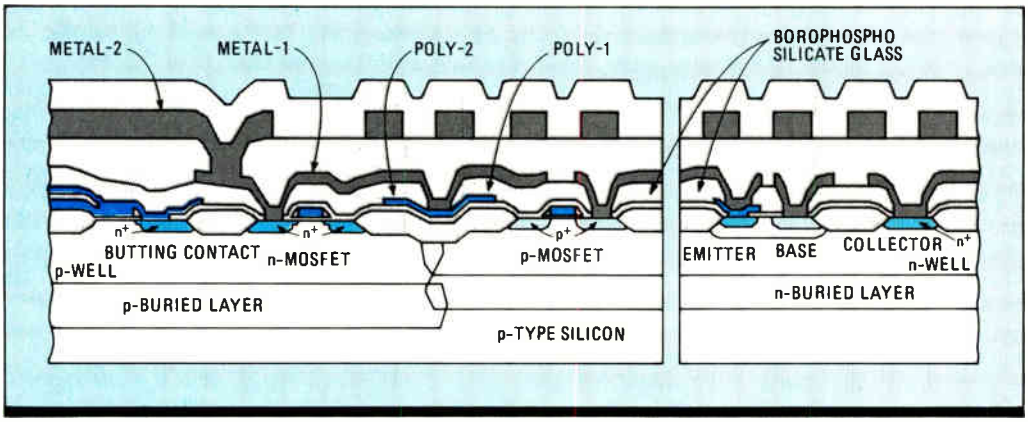
MEMORIES

HERE COMES A 256-K SRAM AND IT'S FROM FAIRCHILD

KARUIZAWA, JAPAN

Details have surfaced on what may be the first 256-Kbit static random-access memory to go on the market. The unusual thing about it is that the product is American and the platform Japanese. The company is Fairchild Semiconductor Corp., and the venue was Japan's Symposium on VLSI Technology in mid-May. Until now, the closest to market with the big SRAM appeared to be Hitachi Ltd., which showed slides of a 256-Kbit chip at a recent meeting, and Fujitsu Ltd., which says it is working on one.

Fairchild won't divulge details on the circuitry—they are expected to be disclosed at next January's International Solid State Circuits Conference. Product introduction is scheduled for the first



THE BiCMOS EDGE. Among the features of Fairchild's 1-μm BiCMOS process are the p^- buried layer, which improves isolation spacing, leads to better n^- MOS FET performance, and increases soft-error immunity.

half of next year. But it did say that the device uses BiCMOS technology, has 1-μm features, dissipates less than 1 W, and is compatible with emitter-coupled logic. The product is important for Fairchild: it plans an all-out fight to gain a leadership position in static RAMs.

Fairchild's new device will be as fast as the speediest smaller SRAMs on the market. Maximum access time will be 15 ns, with typical access time being 10 ns. Hitachi's maximum access time for its 64-Kbit BiCMOS part is 12 ns. Fujitsu achieves 15 ns for 64-Kbit ECL parts that dissipate 1.56 W, a power level that will keep this technology from extending to the 256-Kbit size.

Fujitsu, whose present high-speed devices use only bipolar technology, says it also is working on a 256-Kbit BiCMOS ECL-compatible memory chip. And another U.S. firm, Saratoga Semiconductor Corp. of Cupertino, Calif., produces a 64-Kbit SRAM in 2-μm BiCMOS technology.

Fairchild's purchase of advanced 0.8-μm steppers enabled its designers to start with a clean slate rather than work with an already operating production line, according to Bami Bastani, technology development manager for MOS R&D at Fairchild's Memory and High Speed Logic Division in Puyallup, Wash. So Fairchild designers were able to use 0.9-μm Locos (local oxidation on silicon) isolation spacing, 1.1-μm contact metallurgy, and a thin 20-nm gate-oxide layer, says Bastani.

BUSTING THROUGH. BiCMOS neatly punctures the speed/density ceiling imposed by ECL technology. ECL's speed makes it preferred for RAM designs, but its density limits are a handicap—standard packages have a power dissipation limit of about 1 W uncooled, which imposes a limit on fast ECL of either 4 Kbits or 16 Kbits. BiCMOS provides the best of both worlds: close to CMOS density and power consumption with close to bipolar speeds. And it stays within the power budget while achieving two to three times the speed of CMOS.

What's more, says Bastani, the technology group had a good head start on the bipolar portion of the device, because the Fairchild Aspect bipolar development line is in the same facility. And since the BiCMOS bipolar transistors use advanced polysilicon emitters, as do the Aspect parts, the BiCMOS designers benefitted from the expertise.

Propagation delay for the ECL gates is 150 ps in the bipolar parts, versus about 210 ps in the BiCMOS parts. But even at 210 ps, Bastani maintains, the bipolar transistors in Fairchild's BiCMOS are faster than those in competitors' ECL parts because the others have not yet mastered polysilicon emitters, which are used in the Aspect transistors.

Paradoxically, the MOS transistors are better than could be produced by a standard CMOS process. The retrograde doping of the p^- buried layer under the shallow p^- well shunts the parasitic lateral bipolar transistor that would otherwise be formed between source and drain. The effects of impact-ionization breakdown is suppressed even for very short channel lengths—here, about 0.8 μm typical, 0.6 μm worst-case.

Bastani also credits the bipolar type of configuration with two additional performance advantages. The two buried layers suppress latchup very effectively, and the device boasts better soft-error immunity.

For its part, Hitachi uses 1.3-μm technology for its BiCMOS ECL-compatible ECL100K and ECL10K 64-K SRAMs. Coming are 256-Kbit-by-1-bit and 64-Kbit-by-4-bit BiCMOS devices with TTL input/output, as well as ECL-compatible 256-Kbit BiCMOS parts with a maximum access time of 15 ns. *–Charles L. Cohen*

MICROPROCESSORS

CUSTOMERS CALM AS INTEL GETS 386 BACK ON TRACK

NEW YORK

A month-long shutdown of Intel Corp.'s 80386 production line is over: the company has corrected the mask fault that was causing multiplication errors. And it looks as though the Santa Clara, Calif., chip maker and its customers have weathered the crisis in fairly good order because the 386 is still in the startup phase.

At industry-watcher Dataquest Inc. in San Jose, Calif., the view of research analyst Patricia Galligan is that the temporary shutdown won't matter much except to Intel's bottom line. Also sanguine are executives at Compaq Computer Corp. in Houston, whose Deskpro 386 personal computer is built around the chip. "Clearly, Intel is going to take care of its largest customers, and Compaq is it for the 386," figures marketing vice president Michael Swavely. "Our relationship with Intel is such that we will not suffer inordinately. I think Intel is going to allocate [with a tilt] toward the customers with products already in the marketplace."

IBM Corp. is also getting to be a big customer, and a spokesman says delivery of the Personal System/2 model 80—its new 386-based machine—has been moved up one month, from July to June. And Texas Instruments Inc., which employs the 386 in its new multiuser System 1300, has test programs to screen out the error-prone chips.

Meanwhile, Intel executives say they can't tell just how much the 386's yield-reducing "pattern sensitivity affecting the 32-bit multiply," as it is officially labeled, will hurt. In fact, an Intel spokeswoman explains, it's difficult to tell how many chips with the glitch actually were shipped, because "there was a test hole and the 32-bit multiply operation wasn't being fully exercised." Moreover, 16-bit programs are not affected, and most users of equipment built around the chip are still working with 16-bit operating systems. "The only 32-bit programs in use are the Unix ones," she says.

Compaq won't disclose how many Deskpro 386 computers it has shipped

overall, but in February the company announced it had delivered more than 30,000. Because Compaq didn't hear about the faulty ALU until late March, some of those machines contain defective chips. Swavely says Intel offered Compaq new testing programs to screen out the bad devices, and within a matter of days, production lines were using the tests and Deskpro 386s were being shipped. "Everything we have shipped since the last week of March has been screened for the problem," he adds.

Further frustrating attempts to assess long-term effects is the fact that demand for the 386 went up substantially while Intel was fixing the faulty ALU mask. The result, says Intel, was a shortfall for the first and second quarters—though the company doesn't know whether to blame demand or the bad ALU. It won't begin to meet quotas again until the fourth quarter. At the same time, Intel is sticking with its forecast that it will ship a half-million parts during 1987, after sending some 65,000 out the door in 1986.

Swavely says this experience isn't going to start Compaq looking for a second source. "We would feel more comfortable if there was one, but we also understand Intel's needs to protect its business," he says.

Meanwhile, Intel's rival in the 32-bit market, Motorola Inc., doesn't expect its 68020 to benefit much from the 80386's problem. "By and large, the customers that are impacted by this are those that have already announced products and already are supposed to be shipping systems," says Jack W. Browne, marketing manager for the 68000 family. "This is another convolution in the startup phase they are going to have to deal with."

–Howard Wolff, with bureau reports

TEST

NOW, A WAY TO TEST FAST GaAs CHIPS

LOS ANGELES

Laser-pulsed test techniques are looking more and more like the answer to a knotty problem holding back full realization of high-speed gallium-arsenide devices. Dubbed "picosecond optoelectronics" by researchers, who have stepped up the development pace in the past year, these testing techniques—along with the equipment to perform them—are starting to travel the road from the laboratory to the real world.

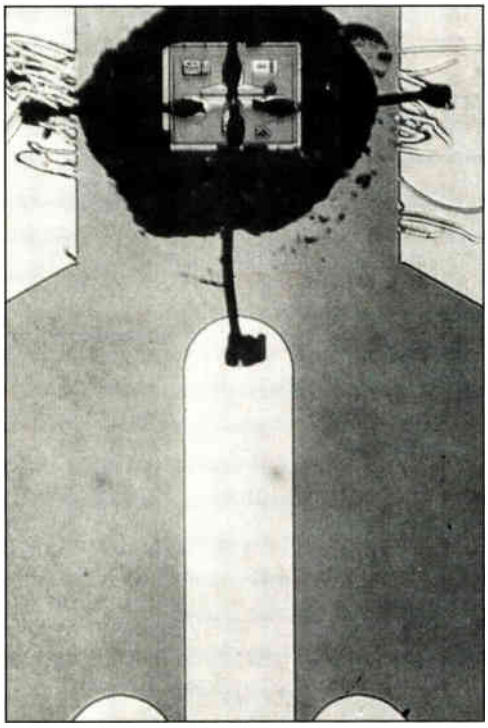
Continuing improvements are coming from AT&T Co.'s Bell Laboratories, where the initial work was done more than a decade ago, and Aerospace Corp., which has built equipment to test GaAs FETs ticketed for advanced Air Force space-communications hardware. Scientists at Stanford University also are pushing for improvements in picosecond optoelectronic testing and have expanded it to handle silicon integrated circuits. And a startup firm, Lightwave Electronics Corp., is gearing up to test devices in the Defense Department's Mimic (Microwave and Millimeter Monolithic IC) program and perhaps for commercial users as well [*Electronics*, May 28, 1987, p. 24].

GREATER BANDWIDTH. The equipment, needed by GaAs IC producers to characterize devices and by users to test them, supplies a way to accurately measure performance that exceeds the capability of conventional equipment. The objective is to have a greater bandwidth than that of the tested device. Current measurement equipment, based on frequency-domain techniques and continuous-wave signal generation, is limited to 26 GHz, researchers say. But advanced GaAs chips operate above 100 GHz. So picosecond laser pulsing is used to generate responses that can be sampled to derive time-domain-based measurements.

In addition, picosecond optoelectronics is noninvasive—there is no wire probe used to establish testing points on a chip, notes David H. Auston, of Bell Laboratories. In fact, complex GaAs chips with closely packed conductor nodes cannot be fully characterized or tested without a noninvasive approach.

Now the race is on to apply the techniques, as GaAs ICs get faster and it becomes more apparent that "the conventional measurement capability is running out of steam," says Auston. Bell Labs' latest wrinkle is a technique that probes the wafer directly with a pulsed laser beam to characterize circuits.

The underlying principle of picosecond optoelectronics is that GaAs itself is an electro-optical material that generates an electrical field when pulsed by a laser. The field changes the material's optical index of refraction and thus the polarization of any lightwave passing through it. The beam's intensity is also altered, and by measuring intensity differences, the responses can be determined, as demonstrated at Stanford and the University of Rochester [*ElectronicsWeek*, Jan. 1, 1985, p. 23].



LASER-PULSED TESTS: A GaAs FET ready to go in picosecond optoelectronic fixture.

In the Bell Labs work, an electro-optical crystal near the wafer surface is pulsed with a picosecond laser beam, altering the electrical properties of the GaAs. Response speeds of 200 femtoseconds have been measured, says Auston. Details were reported at the annual Conference on Lasers and Electro-Optics last month in Baltimore by Bell Labs' Janis Valdmanis.

David M. Bloom, an associate professor of electrical engineering at Stanford, also has demonstrated direct-beam probing. But he uses the substrate itself as a modulator rather than doing this externally, as with other reported approaches. He reports attaining bandwidths above 100 GHz and spatial resolution of the probe to several microns. He also has employed the techniques in real time with silicon ICs, using a cw laser and reaching 200-MHz bandwidths.

At Aerospace Corp. in El Segundo, Calif., a team directed by Stephen C. Moss of the technical staff has carried Bell Labs' work with FETs further by devising a test fixture to exercise them. The fixture consists of planar circuits, in which photoconductive pulse generators and samplers are fabricated in microstrip transmission lines. The GaAs device is bonded into the fixture. Sampling and triggering laser pulses then generate picosecond response times at frequencies up to 200 GHz. Aerospace is a nonprofit corporation providing systems engineering services for government customers, primarily the Air Force.

At Lightwave Electronics in Mountain View, Calif., the goal is

to have a prototype picosecond optoelectronic test system by late summer, under a contract with the Air Force. Meanwhile, ties already have strengthened between researchers and commercial GaAs device manufacturers. Aerospace is giving performance data to designers at Avantek Inc., and Stanford's Bloom has links with GMHE/Hughes Aircraft Co. and TriQuint Semiconductor Inc., among others. At Bell Labs, Auston notes, optoelectronic testing advances "are proving very valuable in guiding AT&T designers." *–Larry Waller*

POWER ICs

IN SMART POWER, ASICs ARE THE ROAD TO RICHES

PHOENIX

Players in the power integrated-circuit business know that for it to become more than just a niche market, application-specific design and production tools are needed. The cost savings and faster turnaround time that ASIC techniques routinely provide for logic parts would then attract more customers to so-called "smart power" circuits, which generally must be customized for each application. That opportunity is now at hand.

Several manufacturers have managed to master the art of blending power switching and control logic on the same chip. It's a tricky proposition, even with custom design, because of the difficulties inherent in developing the processes for isolating the two functions. Computer-aided design tools are therefore more complex than those for semicustom gate arrays, and providing cell libraries takes longer than for logic chips.

Some industry observers didn't expect the work to mature this soon. "Nobody has even been touting power ASICs," says William I. Strauss, president of Forward Concepts Inc. of Tempe, Ariz. He rates the development as an important advance for the power-chip field in general—and a real advantage for the leader, Motorola Inc.

Its Discrete and Special Technologies Group already is operating a power-ASIC program that is available at its Phoenix headquarters and in Santa Clara, Calif.; Tokyo; and Toulouse, France. Customers take their power requirements to the centers, where engineers compile them into chips.

CELL BLOCKS. The building blocks for this work, in addition to CAD software, are a library at each site of more than 50 standard cells that cover most necessary functions. They include operational amplifiers, basic references, comparators, thermal shutdown, and open-load detectors. Most of the Motorola devices have less than 100-V ratings, with current of more than 10 A. (The accepted definition of a power chip is one that operates at 25 V or above, with power of at least several watts.)

The major force behind the Motorola ASIC network is the crash program that was instituted to design and manufacture a power-chip set—motor controller and power FET—for Canon Inc.'s digitally controlled camera [*Electronics*, March 19, 1987, p. 32]. Motorola did the job in less than a year but had started ASIC design in early 1985. "The Canon program brought it to fruition," says David Cave, smart-power design manager.

Other manufacturers are nearing the ASIC goal. SGS Corp., the Phoenix subsidiary of the Italian company, has compiled a cell library and perfected CAD techniques for internal use. Executives at Siliconix Inc., Santa Clara, Calif., consider the ASIC-power IC blend "a major step," which it is taking internally. But no date is set for commercial offerings. An early leader in power ICs, General Electric Co., is also focusing on internal use.

By 1991 the market will reach $600 million, with half in ASICs

Next month, International Rectifier Corp. of El Segundo, Calif., will introduce its 28-cell ASIC library. Derek Lidow, senior vice president for marketing operations, is excited about the customer prospects for power ASICs. "The concept is the most fruitful in the power arena," he says. He predicts that ASIC types will increasingly dominate, holding half the power semiconductor market by the end of the next decade. That market, as estimated by Frost & Sullivan Inc., should increase to $600 million in 1991 from $80 million last year. This year's total is $160 million.

Motorola's Cave adds that although ASIC tools can trim some 20% off prices, the big attraction is design in as little as three weeks, compared previously with months. But he maintains that having the CAD tools at company design centers is not yet "true ASIC," which in today's logic world often resides in the customer's own work stations. "This is in the cards for key customers, but we're still nervous about proprietary technology," he says. *–L.W.*

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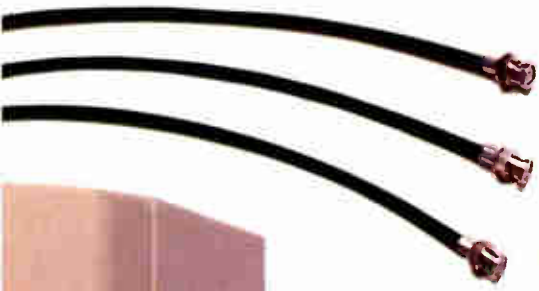

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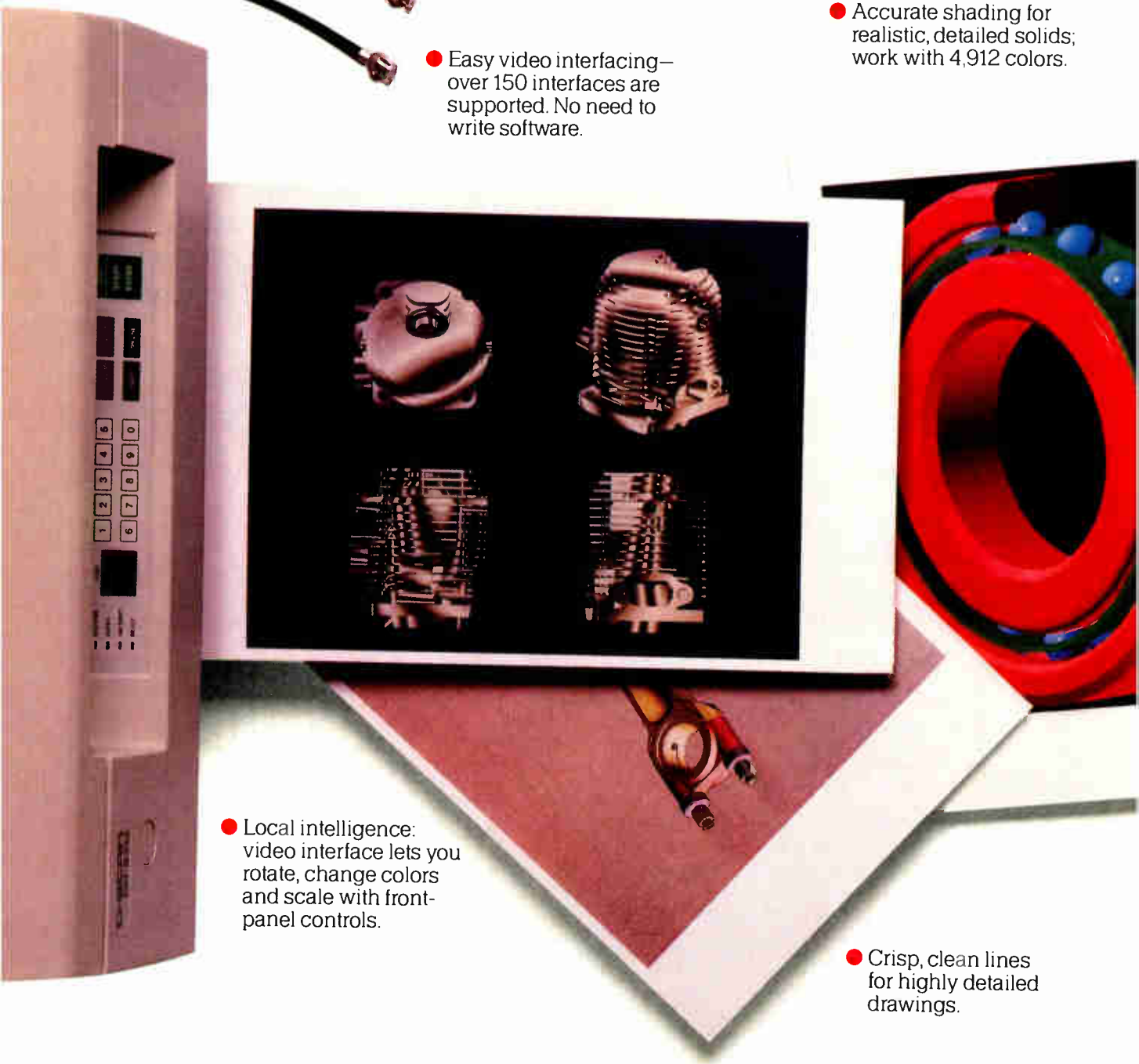

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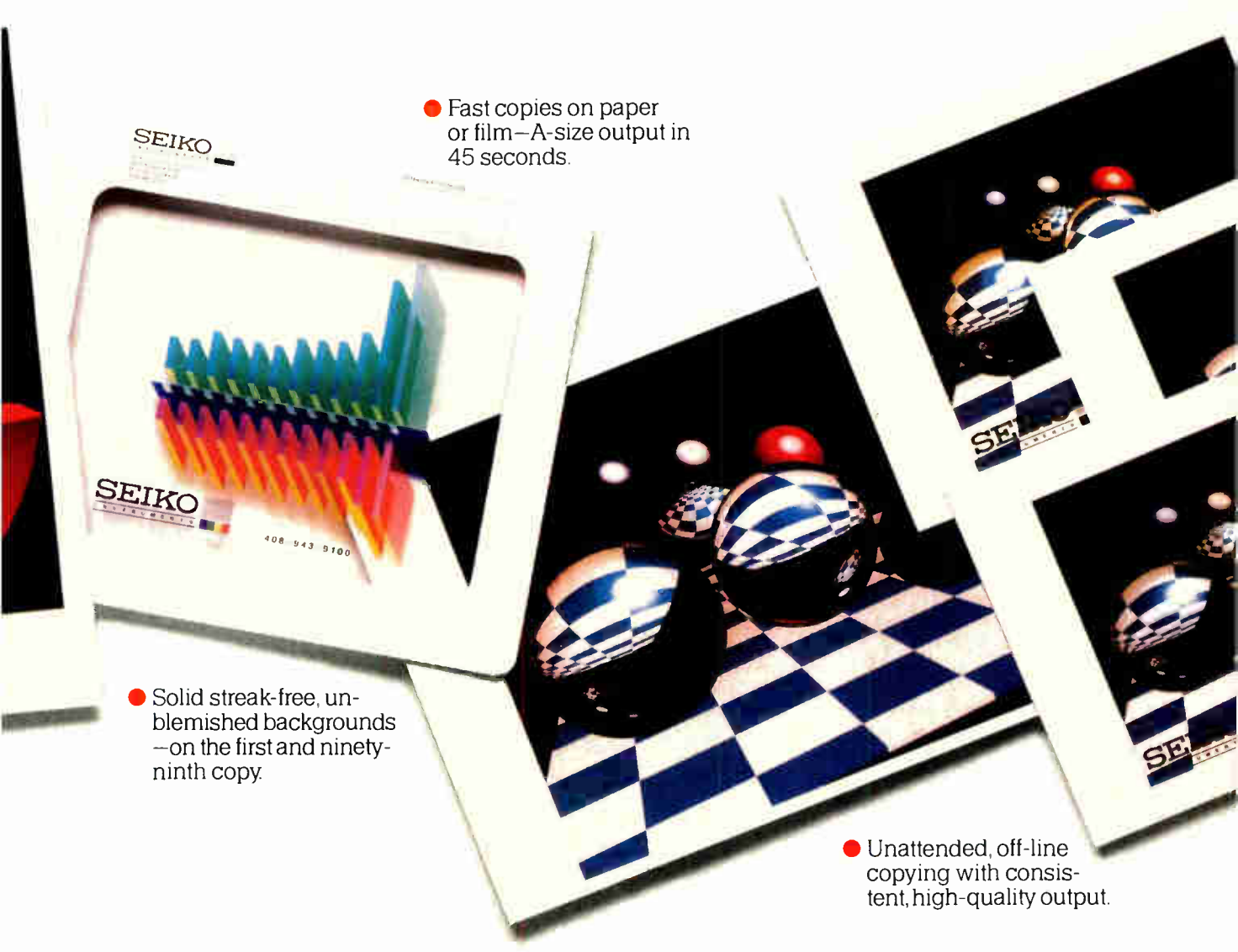

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COMMUNICATIONS

EX-AT&T ENGINEERS MAKE A NICHE OUT OF THE SPLIT

BRIDGEWATER, N. J.

Splitting AT&T Co. and the Bell Operating Companies was supposed to be be good for the country. The jury is still out on that one, but divestiture turns out to be a good thing for a Bridgewater, N. J., startup, Integrated Network Corp. Founded by 25 senior AT&T Bell Labs engineers in 1985, it has discovered a hole in the market created by that divestiture—upgrading equipment to carry data and special voice services—and has begun to plug it.

Now the company is ready with its first products. And it has signed up as customers five of the seven BOCs and is negotiating with the other two.

The engineers who founded Integrated Network designed the voice-switching and transmission equipment developed by Bell Labs for the old AT&T and its operating divisions—the equipment now in use across the country. By designing into the equipment hooks to which new gear could some day be added, they made it easy to upgrade so that it would ultimately be able to handle data as well as voice.

But the AT&T of today is concentrating on selling new telecommunications equipment and has little interest in the market for upgrades. Enter Integrated Network, which is making a business out of offering new voice services and upgrading old equipment so it can carry data along with the voice traffic.

YO-SUNG CHO: Taking advantage of an upgrade market that is growing 20% a year.

The market potential is huge. In 1986 the BOCs purchased more than $15 billion in equipment and factories. Of this total, Integrated Network estimates that more than $2 billion was for equipment for data and special services—the market niche of the company's simple but effective strategy. Yo-Sung Cho, the company's president and chief executive officer, estimates that this segment of the market is currently growing at 20% a year and will reach $3 billion by 1990.

Integrated Network is offering two categories of products, designed by a team led by Gihong Kim, vice president of engineering. One provides new services over telephone lines, the other enhances existing equipment.

VOICE, DATA SWITCH. In the first, the Universal Switched Data Capability line carries and switches data at rates of up to 56 Kbits/s through the circuits of the existing telephone network. This system also contains an integrated voice and data product family, allowing simultaneous but independent transmission of both voice and data. The data can either be circuit-switched or packet-switched and can travel at a rate of up to 19.2 Kbits/s.

The second category consists of plug-in additions to existing equipment, which allow the BOCs to provide such capability as software-controlled remote service and new data services more efficiently. This approach by Integrated Network enables the operating companies to purchase upgrade equipment on a line-by-line basis to meet customer demand in all its service areas.

The alternative—replacing entire offices with new digital equipment—is not as attractive. It produces islands of service where some areas have the new services and others still have the old. And it takes years to switch over completely to the new equipment because of the high cost and the long amortization period on the existing equipment.

–Tom Manuel

CONFERENCES

NCC REVIVAL PLAN WON'T HELP THIS YEAR

CHICAGO

Reports of the imminent death of the National Computer Conference are greatly exaggerated, at least if you believe sponsors of the 15-year-old show. They've got a plan, they say, to revitalize the event for future years. But the 1987 edition in Chicago on June 15-18 will be a sickly specimen compared with the show's heyday in 1983, when NCC drew some 97,000 visitors and nearly 700 exhibitors to Anaheim, Calif.

This year's NCC lists only about 160 vendors, down from about 400 last year in Las Vegas. And with the notable exception of IBM Corp., few are big names. The American Federation of Information Processing Societies, lead sponsor for the show, predicts about 30,000 visitors. Again, that's down from last year, when attendance plummeted to 40,000 from about 85,000 in 1985.

Conspicuous by their absence from the exhibitor list are heavyweights including Control Data, NCR, Unisys, and Honeywell. "When we looked at the dollars we'd have to spend and what's been happening to NCC in terms of dropping attendance, we decided not to go," explains a spokesman at Honeywell Buli Inc. in Minneapolis. "We're planning for another flat market this year, and we've got to spend our dollars carefully. We think we're better off going to the smaller shows that are focused at vertical and technology markets."

LACK OF FOCUS. Comments are much the same around the industry. Vendors complain of a lack of specific focus at an NCC show that has traditionally aimed to be an all-encompassing, industrywide computer conference and exhibition. Many vendors perceive a bigger bang for their buck at shows such as Comdex—which has taken over as the premier microcomputer and personal-computer showcase—and the proliferating breed of smaller exhibitions that target specialities such as computer-aided design and manufacturing, electronic publishing, networking, and other vertical segments.

Given NCC's recent downward spiral, some observers even speculate that this year's show could be the last. But Carroll Lewis says, "We've been hearing of our demise for years now." Lewis, president of Commercial Data Corp., Memphis, Tenn., serves as chairman of the NCC board. "That's a rumor that our competitors would like to promote, but it's very definitely not a consideration."

Lewis concedes problems, including an unwieldy management structure, the computer industry slump, and competition from vertically oriented shows. But

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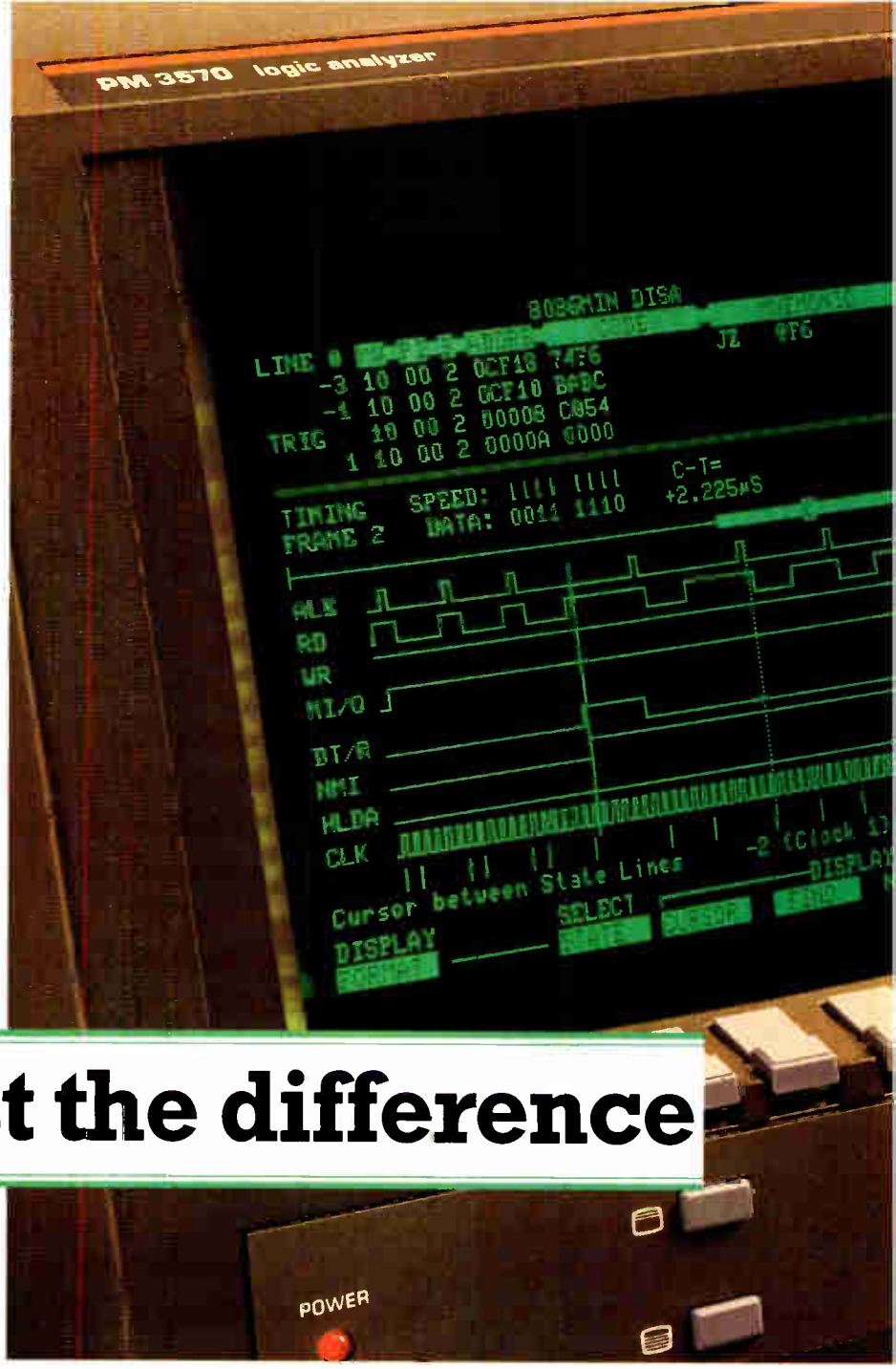

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Circle 43 on reader service card

he notes that NCC sponsors are taking a number of steps to make the event more attractive for vendors and exhibitors alike.

"The main thing as far as the future goes is that we've elected to hire an outside show-management firm," he says. That firm, which as of late May was not chosen, will take over promotion and marketing from the AFIPS staff and will also participate in technical-program planning, a task previously handled by industry volunteers.

The addition of professional management will streamline the NCC decision-making process and "will hopefully lead to more consistency" in the conference program, Lewis says. "Volunteer groups will still basically put the program together. But we want to use the outside group as a kind of stabilizer so

Will a small, more vertical show in the spring turn around the NCC?

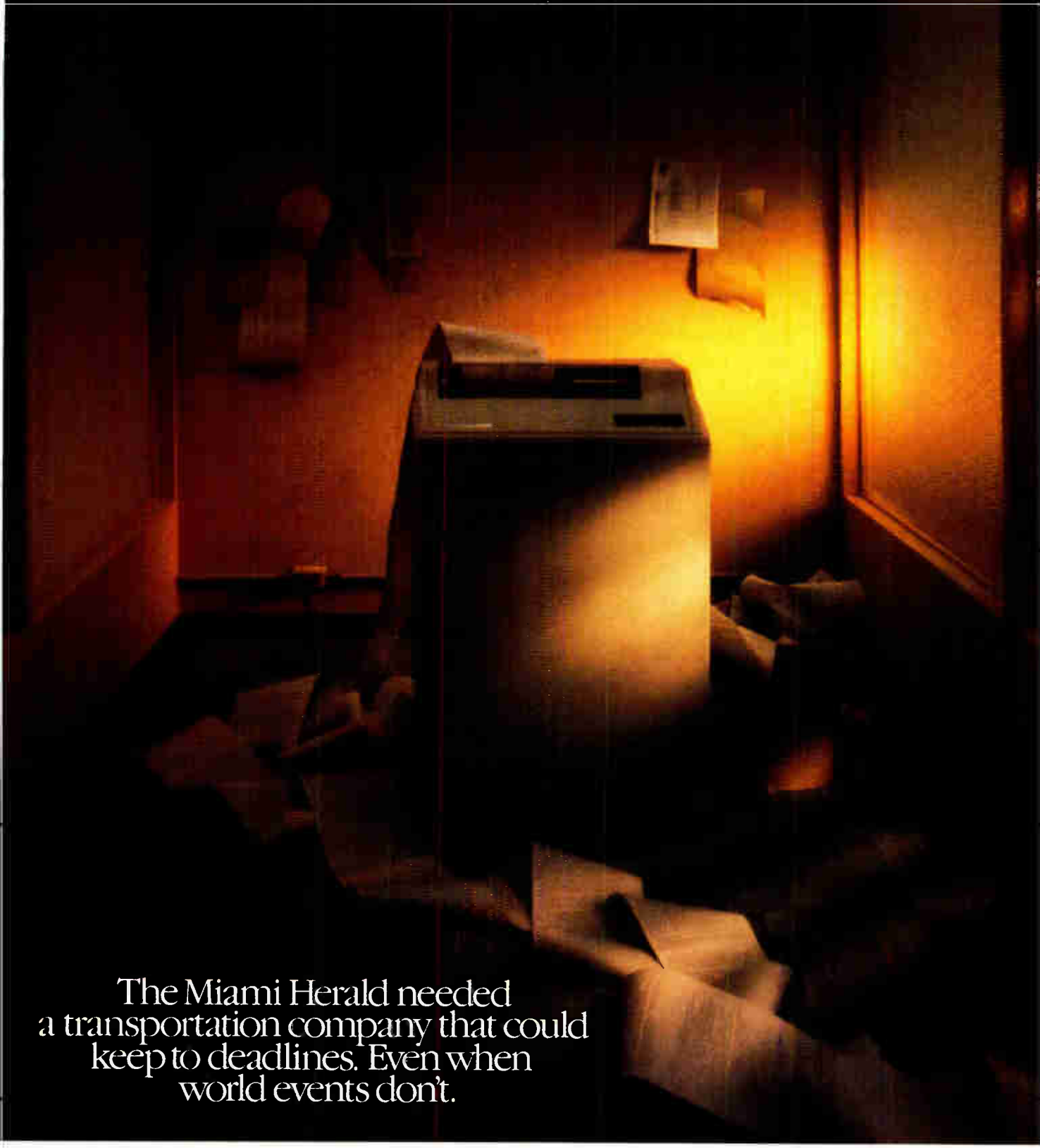
we won't be alternating between a technical conference and a management conference. Depending on who's leading the [volunteer] steering committee each year, the program has tended to be more heavily weighted toward one or the other."

NCC exhibits in future years will focus more on vertical markets, Lewis promises. "NCC still needs to remain a broad-based show, but there are things we can do to bring in some of the vertical segments. You'll see more software at NCC than you've seen in the past," he notes. "And you might even see some multiple shows within the show" that will focus on specific segments.

Likewise, the NCC's smaller size now makes possible a schedule that rotates the event among Chicago, Los Angeles, and New York, with show dates in the late spring. "When NCC grew so large in Anaheim in 1983, Chicago and Las Vegas became the only two places big enough to hold it," says Roger Halligan, NCC '87 promotion chairman. "We had no problem with Chicago, but in Las Vegas we had to take dates in July, which is not the most desirable time to be there."

What's more, "In Las Vegas, you have to import your crowd," Lewis points out. "We're now moving back to the larger regional metropolitan areas, where we can draw a large local crowd." Lewis adds that NCC show dates set for early April beginning in 1989 should help the exhibition's popularity. "Spring is when everything blossoms, and a lot of computer makers like to introduce products at that time," he says.

–Wesley R. Iversen



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gral SCSI interface—the product gives Maxtor a leading position in the technology for optical storage.

The work with Ricoh is the perfect example of the way Maxtor goes about designing, building, and marketing its products, says William Dobbin, vice president of finance and administration. "It sets the stage for the introduction of our fully erasable optical drive. When we bring the product to market [in late 1987 or early 1988], we will be the only U. S. Winchester drive company that is also selling an erasable optical product."

KITROSSER: "I was attracted by the passion in the company."

Maxtor also looks for domestic deals. It recently acquired U. S. Designs Inc. of Lanham, Md. "Our primary interest is their very-high-end controller technology, especially their adaptive-cache technology," says McCoy. "They are a leader in controller technology."

Dobbin adds, "Until recently there have been enormous strides in increasing capacity and reducing drive size. But there have not been the same strides made in the access times of the device. U. S. Designs has developed an artificial-intelligence scheme that learns where the user is going to acquire data on the disk drive. It brings that group of data onto the controller into cache and allows the user to access the data at much faster access times [from random-access memory] instead of making a disk access."

However, developing new technology is only one leg of the strategy. Another is cost-effective mass production with good yields and within the market window. "In the disk-drive industry in the 1990s, the true survivors will be broad-bandwidth companies that are both volume manufacturers and aggressive technology companies," president McCoy predicts.

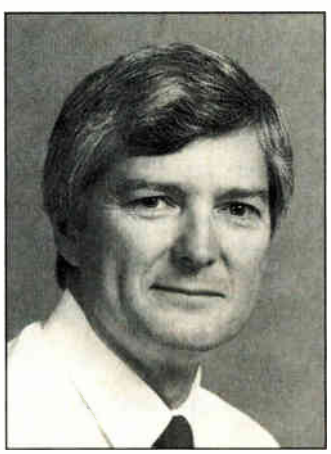
DO IT RIGHT. McCoy started Maxtor with the clear idea that he would make large numbers of a high-technology product. "I've learned from experience that trying to inject advanced technology into a lower-technology manufacturing facility is just plain unworkable," he says. And instead of robotics or sophisticated material-handling systems, the company made key investments in basic tooling. "We built and patented some tools because they are key to assembling our drive," says Kitrosser. The Maxtor drive is not easy to assemble—it uses 16 read/write heads and eight disks. Moreover, repairing the disk once it has been assembled is not cost-effective, so considerable effort goes into making sure that each drive is put together right the first time.

Another component in the manufacturing strategy was a plant in Singapore, which the company made a point of opening at the same time as its U. S. operation. "You cannot start a domestic operation and then, when production ramps up, start the offshore operation up overnight," says Kitrosser. "You have to cultivate a vendor base overseas just as you do in your U. S. operations."

Maxtor also has used its good relationships with suppliers to strengthen its manufacturing operation. Peter Tegan, vice president of marketing at Lin Data Corp. of Santa Clara, Calif., testifies to that. "When their incoming test of our thin-film media disagreed with our outgoing test, they came to us and helped correlate our testing with theirs to help us ship what they wanted in their drives," says Tegan. Maxtor also works with suppliers to solve such fundamental problems as setting up statistical quality-control methods. "The result is that we are able to catch problems before they come in the door," says Kitrosser. "[That] has increased our inventory turnover, decreased our WIP [work in process], and produced much better production yields."

'The notion of better mousetrap marketing is baloney,' says McCoy

A big contributor to improved yields and better production controls is a bar-code system that gives management instant feedback on any failures on any part of the line. "We are currently monitoring 25 to 30 points in the process on-line with the bar-code readers," says Kitrosser. "At the very least, we get a report every morning showing every operation, what the yield is at that operation, the list of failures appraised by the most critical to less critical. It also helps track our work in process."



TEAL: "We started with over $50 million in OEM contracts."

Then there is the matter of getting work out on time. "When I joined, the mindset in the company was if we got it out by the end of the quarter, it was OK," says Kitrosser. "The concept is common in the industry, but it's a bad mindset because sooner or later you have to make up [the lost time]." That means a rush during the last week of the quarter, with poor quality and waste resulting.

Kitrosser made it a goal to establish a weekly delivery schedule and then work up to a daily schedule. "I had managed to achieve the weekly schedule when we hired Robert McGrath, our current director of manufacturing," Kitrosser says. "He came from the automobile industry, where production schedules had to be met on an hourly basis." The company now makes its numbers every day—and every hour, if possible.

MARKETING SAVVY. But cost-effective production of large numbers of technically superior drives with good yields does not ensure success. Savvy marketing is needed. "The notion of better-mousetrap marketing [customers will seek out technically superior products], which was rampant in this industry in 1982, is baloney," says McCoy.

"We had over $50 million in OEM contracts before we delivered our first drive," says Robert Teal, vice president of marketing and product assurance. "Most of that we got through personal relationships with buyers who knew us from [our work at] previous companies. They knew that we had a record of delivering cost-effective and the highest-performance disk drives. We had given them a competitive edge, and they believed that we could give one to them again."

One of Maxtor's marketing tenets is based on lowest possible cost per megabyte. As Teal puts it, "When you make it low enough in price, people will use all the storage you can give them. The average selling price of our disk drives today is almost the same as it was three years ago, but the customer is getting nearly three times as much capacity."

That Maxtor's strategy is well received can be judged from its list of long-term customers. The first was Convergent Technology, a company that built its business on quickly adopting and exploiting new technology and one that's willing to take technology risks. It is still among Maxtor's top 10 customers. Others were Four-Phase, Basic Four—one of the company's top five customers—and GenRad, which has been using Maxtor drives on its automatic test equipment. □

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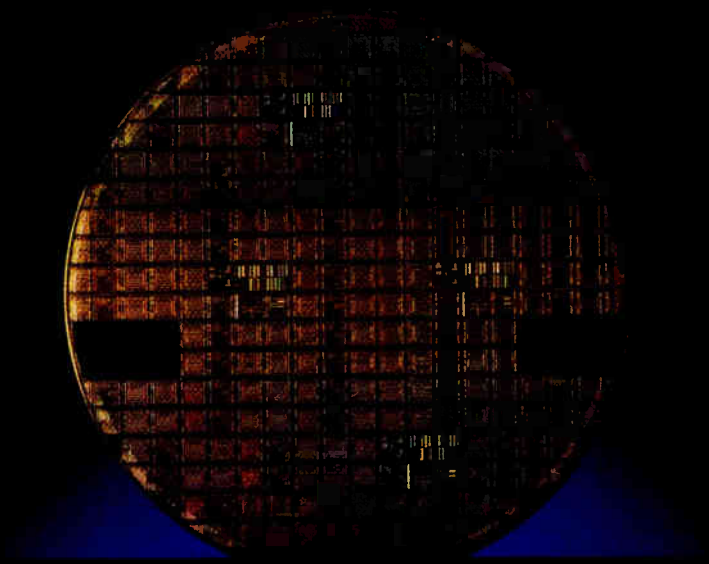

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INTERNATIONAL NEWSLETTER

TOSHIBA MAY LOSE ITS SHOT AT U.S. MILITARY CONTRACTS

Toshiba Corp. may have maneuvered itself out of the running for a number of U. S. military contracts by trying to swing a secret deal with the Soviet Union. The Pentagon has apparently delayed awarding contracts for which Toshiba was bidding pending the outcome of a Japanese government investigation into allegations that Toshiba secretly shipped equipment to the Soviets for use in manufacturing submarines. Toshiba allegedly sent the gear by way of Norway's largest weapons producer, Kongsberg Vaapenfrabrikk. Such sales are in violation of the regulations of the Paris-based Coordinating Committee, which oversees sales of advanced technology by member countries—Japan and all members of the North Atlantic Treaty Organization. If the allegations are true, Toshiba would likely lose any chance at U. S. government contracts. The Kawasaki company has been seeking contracts for a $100 million project to outfit the Air Force with laptop computers and a deal for an infrared missile-guidance system, among others. If the system were awarded, it would mark the first time that the Japanese government permitted the release of military technology to the U. S. □

NOW: PERSONAL VCRs YOU CAN TAKE ANYWHERE

Sony Corp. is seeking to do for 8-mm video what it did for audio cassettes with its Walkman. The company is hoping portability will make 8-mm video take off. Before the year is out, the Tokyo firm will market a portable 11-lb. 8-mm video cassette recorder with a built-in 5-in. high-resolution color TV. By 1988, Sony plans to release a 3.3-lb. handheld 8-mm VCR, featuring a 2.7-in. color liquid-crystal display that Sony will buy from an undisclosed manufacturer. Both machines will support video playback and have tuners for TV reception. A palm-size, 7-oz. color electronic camera, designed for use with the handheld VCR but suitable for the two 8-mm player/recorders, will be released late this year. All three were announced late in May at the Consumer Electronics Show in Chicago. □

PHILIPS AND PLESSEY: THE LATEST STRATEGIC ALLIANCE IN CHIPS

In a move that could pave the way for more far-reaching technology agreements in the future, Philips and Plessey Semiconductors Ltd. will jointly develop a circuit for digital TV tuning. In their first cooperative agreement, the Dutch and UK companies will combine the functions of a prescaler and a phase-locked loop on one chip. Each will then manufacture and market the chip on its own. Peter Haywood, marketing manager at Plessey, says the companies are talking about technical and commercial collaboration only and are not planning a corporate merger. "We are feeling our way with this venture to see how beneficial it is for us to join [our technology] together," he says. "It is looking extremely promising, and we have agreed that we will cooperate soon on future chips." □

INMOS IS FIRST UK CHIP MAKER TO START A JAPANESE SUBSIDIARY

With the startup of Inmos Japan KK, Inmos International plc is the first UK semiconductor maker to establish a wholly owned subsidiary in Japan. Douglas Stevenson, chief executive of the parent firm and also president of Inmos Japan, says he expects the new unit to have sales of $1.5 million this year, and $10 million in 1988. Sales will be handled through local Japanese distributors. As much as 75% of these sales will be special products such as transputers, color look-up tables, and digital signal processors. Stevenson says that of the 300 companies that will eventually use its transputer chips, at least 30 will be in Japan. □

INTERNATIONAL NEWSLETTER

PLESSEY-RACAL VENTURE TARGETS EUROPEAN CELLULAR RADIO NETWORK

No sooner had the governments of France, West Germany, Italy, and the UK agreed to establish a pan-European digital cellular radio network than two UK firms announced a new joint company to develop equipment and terminals for it. Plessey Co. of London and Racal Electronics plc of Bracknell are each contributing $24 million for the new concern, Orbitel Mobile Communications Ltd. They are still undecided on a site. The four nations agreed on a narrowband transmission standard in late May and hope to have an operable commercial service by 1991. Plessey and Racal expect their joint venture's sales to reach $162 million annually by then. Estimates of the total equipment market range from $900 million to more than $1 billion by 1991. □

IS INDIA THE NEXT FRONTIER FOR SOFTWARE DEVELOPMENT?

India is campaigning for a higher profile in the electronics industry, but it's doing so in an unusual way. Unlike other Asian countries that have used cheap labor to lure Western manufacturers to their shores, India's Electronics Commission is hoping to use its Western-educated engineering corps to attract foreign businesses. "We are not looking to buy technology; we are looking for partnerships," says Prabho Deodhar, the commission's chairman. "India has provided [the West with] a lot of people who have contributed to technology, and there's no reason why, given the right equipment and financing, they could not do the same in India." Of particular interest, Deodhar says, is the burgeoning software industry. Deodhar says that what happened in the Far East in the 1960s, when U. S. and European companies began producing electronic hardware there, could happen with software in India now. India has been pushing to develop its electronics industry since Rajiv Gandhi became prime minister [*Electronics*, Sept. 2, 1985, p. 26]. □

CANON GETS TECHNOLOGY FOR PHOTOSENSITIVE AMORPHOUS COATING

Canon Inc. has agreed to purchase 10% of Energy Conversion Devices Inc. and to establish a U. S.-based joint venture with ECD to develop and manufacture office-automation equipment using technologies from both companies. The deal brings Canon more than just a 10% interest in the small Troy, Mich., company. The Tokyo firm also gets an exclusive license to ECD's patented high-quality photosensitive amorphous coatings, which it plans to use in its photocopier drums. Canon says ECD has had difficulty developing new products, despite an advantage in technology, and the $7.8 million deal will provide a much-needed influx of capital. The companies have not yet selected a name and location for the new venture. □

RAYCHEM ENTERS PIEZOELECTRIC-CABLE MARKET

Raychem Ltd. of Swindon, UK, is taking on market leaders Pennwalt of Philadelphia, Pa., Solvay of Belgium, and Koreha of Japan in the market for thick-film piezoelectric polyvinylidene fluoride cable, now catching on as a sensor in a variety of applications. Raychem had previously been unable to mass produce thick-film PVDF; high-volume production was limited to thin-film cable. Raychem's new entry, Vibetek 20, is commercially available, in the form of a PVDF-clad wire with an outside diameter of 1.5 mm and an active polymer thickness of 0.5 mm, up to a mile or more long. Its flexibility is such that it can be wound around a mandrel 5 mm in diameter, allowing a wide variety of sensor shapes and sizes to be made from a continuous length. Applications include acoustic sensors for marine applications, and Raychem has already designed a prototype hydrophone using the material that is suitable for towed-array or seismic-streamer radar. □

SIEMENS

Ten BCD at a turn

with the single-deck rotary switch A1353

Siemens offers a highly extensive range of tried and tested electromechanical components, plus all the experience of a manufacturer who has consistently invested a great deal of know-how in developing and perfecting electromechanical components geared to market requirements.

The single-deck rotary switch A1353 is a typical example. One turn, and the desired termination combination is correctly aligned at each of the ten switch positions in BCD code.

This is because the A1353 employs future-oriented technology:

- Reliable contacting by means of self-wiping gold contacts
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This makes the A1353 the ideal switch for programming electronic circuits and for data encoding.

All the other features of the A1353 are detailed in a special publication. If you would like one, please use this journal's reader service or send us the coupon.

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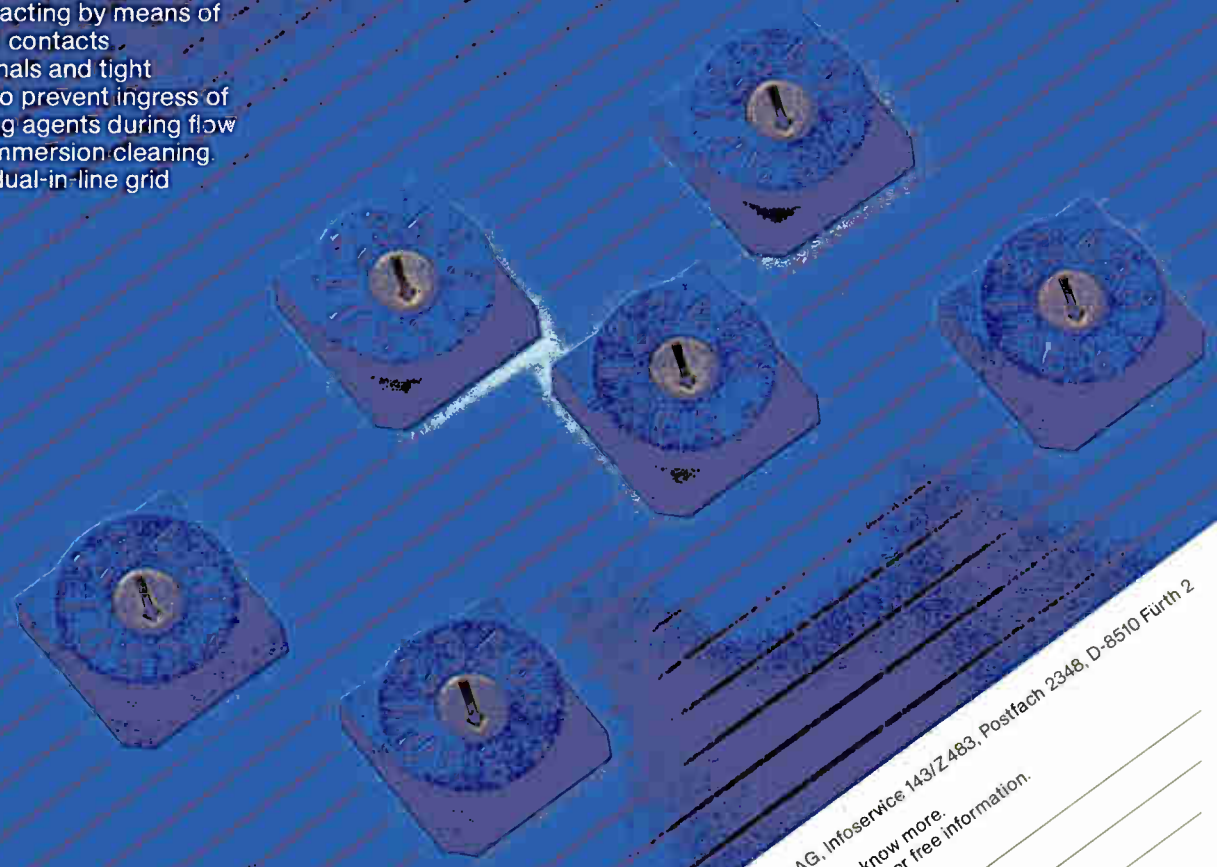

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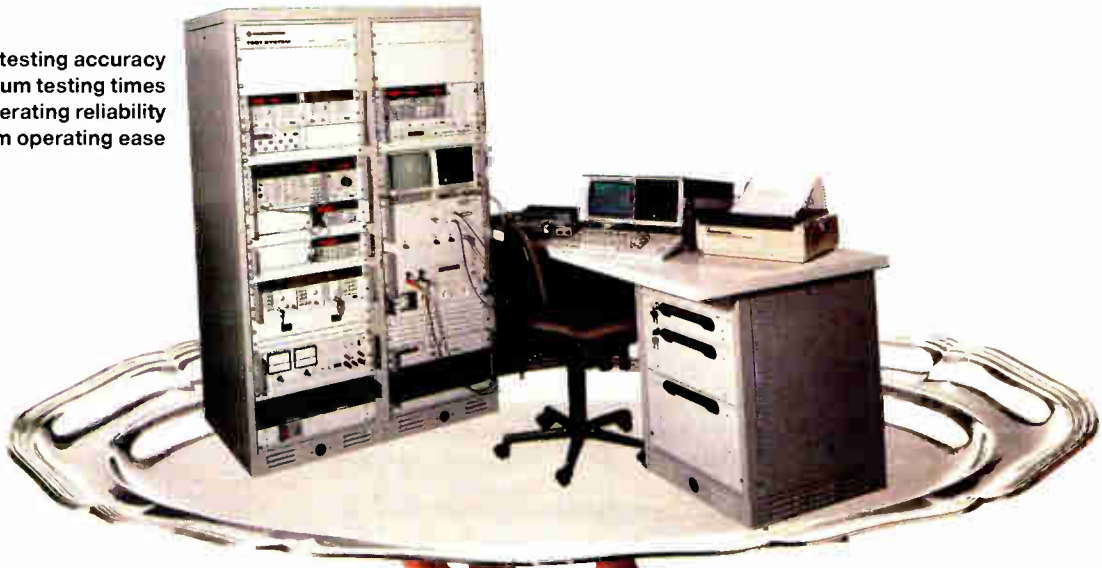

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ROHDE & SCHWARZ

Circle 124 on reader service card

INTERNATIONAL WEEK

NEC TO SELL FAX FOR CAR PHONES

NEC Corp. is set to market a 13-lb facsimile terminal that can send and receive documents over a car cellular phone. The terminal can communicate with facsimile terminals that adhere to CCITT G2 or G3 standards. Capable of making copies, the terminal can handle documents up to metric B4 size and can reduce B4 documents to A4 size for receiving machines that cannot handle the larger size. The Tokyo company plans to begin selling the units in August, at a price of 497,000 yen each. The machine can only be connected to NTT cellular phones. NEC says it has no plans to make a model for Motorola's cellular phones, scheduled to be marketed in 1989 through a new telecommunications carrier, Daini Denden Inc. of Tokyo. It also has no plans to export the terminal.

MITSUBISHI BUILDS SPACE COMPUTER

Mitsubishi Electric Corp. is developing the first Japanese computer to go up in a satellite. The satellite, ERS-1, is Japan's first earth-resources satellite; it will be used to search for mineral deposits. Mitsubishi is developing integrated circuits to keep damage from cosmic rays to a minimum, a spokesman says. It is also in the process of qualifying a method of error detection. The satellite is scheduled for launch in 1991 by the National Space Development Agency of Japan.

DAT PLAYERS FOR CARS IN JAPAN

Digital audio tape players for cars will soon be available in Japan. Kenwood Corp. will market a car player priced at 200,000 yen and a home model for 178,000 yen beginning in August. Another company, Clarion Co., plans an autumn introduction of its 198,000-yen model. The Tokyo companies claim that a car DAT player is more convenient to use than a car compact-disk player. Each firm expects to sell 300 units a month. Neither company has any plans now to export its car DAT player.

JAPAN MAY AID NTT VIDEOTEXT SYSTEM

An ailing interactive videotext system called Captain could receive 50 billion yen in aid from the Japanese government. The Ministry of Posts and Telecommunications has come up with a plan to provide 5 million households with free Captain terminals. The Captain, or character and pattern telephone access information network, service was started by Nippon Telegraph and Telephone Public Corp., now NTT, in 1984 to link terminals through switched telephone lines into a network. But only 30,000 Captain terminals are now in use, far below that anticipated, a rate of growth that has discouraged many data suppliers.

BRITISH TELECOM PLANS CABLE LINK

British Telecom will spend $65 million on optical-fiber cable links for its business telephone customers in London. The contract has been awarded to STC plc of London, with Plessey plc of London acting as subcontractor by supplying its System X service access-switch system. British Telecom plans to use transmission speeds ranging from 2 to 140 Mbit/s.

SGS BOASTS RECORD SALES...

The soon-to-be merged SGS-Thomson combine has received a double boost. SGS, of Agrate-Branza, Italy, has reached record first quarter 1987 sales of $112 million, giving it a 1.52% share of the world semiconductor market and a 5% share of the European market, both the highest the company has ever had. Sales increased by one third over the same period last year from $84 million.

...AS THOMSON SIGNS CMOS PACT

Meanwhile, Thomson Semiconducteurs of Paris has signed a deal with Catalyst Semiconductor Inc., Santa Clara, Calif., to jointly develop a CMOS electrically erasable programmable read-only-memory line. The first product is expected to be a 1-Kbit serial EEPROM. Thomson already produces CMOS EPROMs and n-MOS EEPROMs, and Catalyst has CMOS EEPROM technology. The two companies have previously worked together in developing EPROMs.

CHINA-JAPAN FIRM TO MAKE PHONES

China and Japan plan to build a joint-venture factory to produce telephones for overseas export. The Nitsuko Co. of Japan and the Beijing Number 3 radio factory are negotiating for the $1.8 million project, with the Japanese to hold 40% of the investment and the Chinese the remainder. The factory's initial annual capacity will be 50,000 phones and 2,000 internal extension sets.

UK TO FUND INMOS TRANSPUTER STUDY

The UK Department of Trade and Industry has announced a four-year $5.8 million program to fund research into applications for the Inmos transputer as a countermeasure to the Labour Party's promise to give Inmos financial backing if the party wins the UK general election on June 11. Doug Stevenson, managing director of the Bristol, UK, company, is opposed to the party's plans and says that its involvement in the company would cause it to lose U.S. orders because of the party's defense policy.

FERRANTI, TELEDYNE TO BUILD SENSORS

Ferranti plc of Cheadle, UK, has teamed up with Teledyne Industries Inc. of Los Angeles to produce and market an acoustic sensor system for the U.S. Department of Defense. The system will be based on Ferranti's Picket detection and identification technology, which uses passive sensors and advanced signal processing. Its main application will be in detecting helicopters, which often escape detection by conventional radar and infrared sensors by flying low and using infrared screening.

PLASMON GETS FUNDS TO MAKE WORM DISK

Plasmon Ltd. of Cambridge, UK, has negotiated a $4.95 million finance package that will allow it to go into volume production of its Moth Eye write-once, read-many optical disk. The money has come from a number of venture capitalists led by Rothschild Ventures Ltd. The WORM disk, named Moth Eye because the fine microstructure on its surface is similar in texture to the eye of a moth, will be second sourced by the Japanese joint venture company Kurray-Plasmon Data Systems Co.

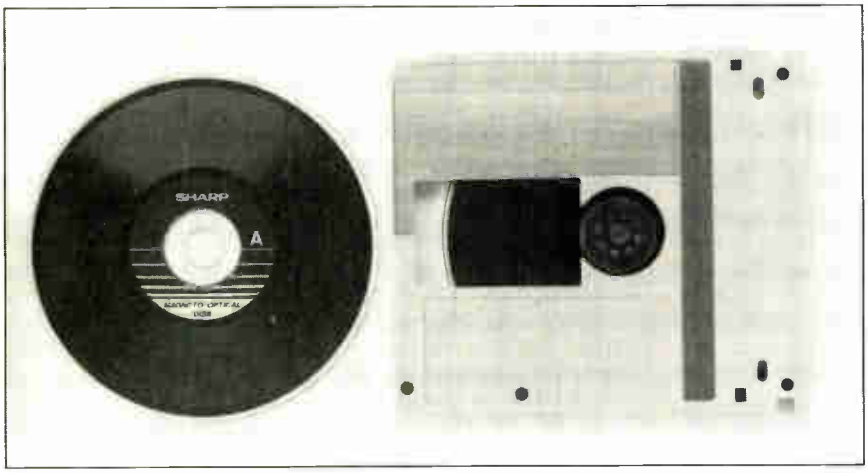
RACAL WINS ORDER FROM CANADA DOD

The Canadian Department of National Defence has ordered three communications, simulation, and electronic-warfare training packages from Racal Ltd. worth $1.4 million (Canadian). The order, which was placed through the Wokingham, UK, company's Canadian subsidiary in Ottawa, goes to training facilities at the Canadian Forces School of Communications and Electronics.

INTERNATIONAL PRODUCTS

SHARP PICKS GLASS, NOT PLASTIC, FOR ITS MAGNETO-OPTIC DISKS

IT WANTS A STRONGER DIRECT-READ-AFTER-WRITE LASER DISK



FOUR CHOICES. Sharp's magneto-optic disks come in both single- and double-sided versions and with or without cartridges, so that disk-drive designers can have maximum flexibility.

An erasable magneto-optic disk is being introduced by Sharp Corp. that is made from hardened glass instead of conventional plastics. The Japanese company picked the harder material to reduce a disk's vulnerability to scratching, warping, and birefringence, and to degradation of its magnetic film by water vapor.

Sharp engineers claim that the use of glass, besides making the disks more durable, also provides a 3-dB improvement in carrier-to-noise ratio over polycarbonate substrates regardless of the magnetic film used. However, the sample price of the hardened-glass disks is 60,000 yen, double that of a polycarbonate-based disk introduced by Sony earlier this year. Sony's disks will have 325 Mbytes on each side in 1,024-byte sectors, while four versions of the Sharp disk each provide up to 658 Mbytes of storage, 329 on a side.

TOO COSTLY? Sharp's competitors contend that glass might not be worth the additional cost and that simple, effective protection technologies are available for polycarbonate-based disks. Applying a thin-film inorganic coating similar to those used to passivate semiconductors on the magnetic film would effectively shut out water vapor, says a Hitachi Ltd. engineer. He acknowledges, however, that birefringence in polycarbonates degrades performance perhaps 1 or 2 dB. The epoxy substrates that Hitachi demonstrated almost three years ago [*Electronics Week*, October 22, 1984, p. 17] exhibit neither warping nor birefringence, he claims.

Sharp's disks are designed for use with 780-nm lasers and require 6 mW of power on the disk during write and erase operations. For reading, the laser power is 1 mW.

Since the International Standards Organization has not promulgated a standard for erasable magneto-optic disks, Sharp has followed the OSI guidelines for DRAW, or direct-read-after-write magneto-optic disks. The disks spin at a standard speed of 900 rpm and are designed to endure more than 1 million erasure cycles. For a wavelength of 1.2 μm, carrier-to-noise ratio exceeds 45 dB.

Applications will be determined by users, according to Sharp engineers. But they envision the disks being used to back up other media and to replace super-capacity floppy disks or DRAW disks in some applications. They do not expect them to replace fixed disks.

Compared with fixed disks, Sharp's products show the same speed disadvantages of other magneto-optic disks—access times 10 times poorer than the 25 to 80 ms of conventional hard disks. One reason for the poor showing is that the rotational velocity of 900 rpm is much slower than the usual 3,600 rpm of hard disks, which gives it a longer latency time. Seeks take longer both because of the heavier optical head and because the fine pitch—1.6 μm in the Sharp disk—requires a rough search followed by a more precise one. Moreover, overwrite must be preceded by an erase pass, and write must be followed by verification.

It should be possible, say design engineers, to spin the disks at higher speeds. Moreover, schemes of the type developed by Nikon [*Electronics*, April 16, 1987, p. 33] and another developed by Hitachi facilitate overwrite to provide faster operation and to enable the disks to work with standard operating systems. Hitachi's scheme uses a magnetic head whose field can be rapidly changed while flying 2 or 3 μm over magnetic film.

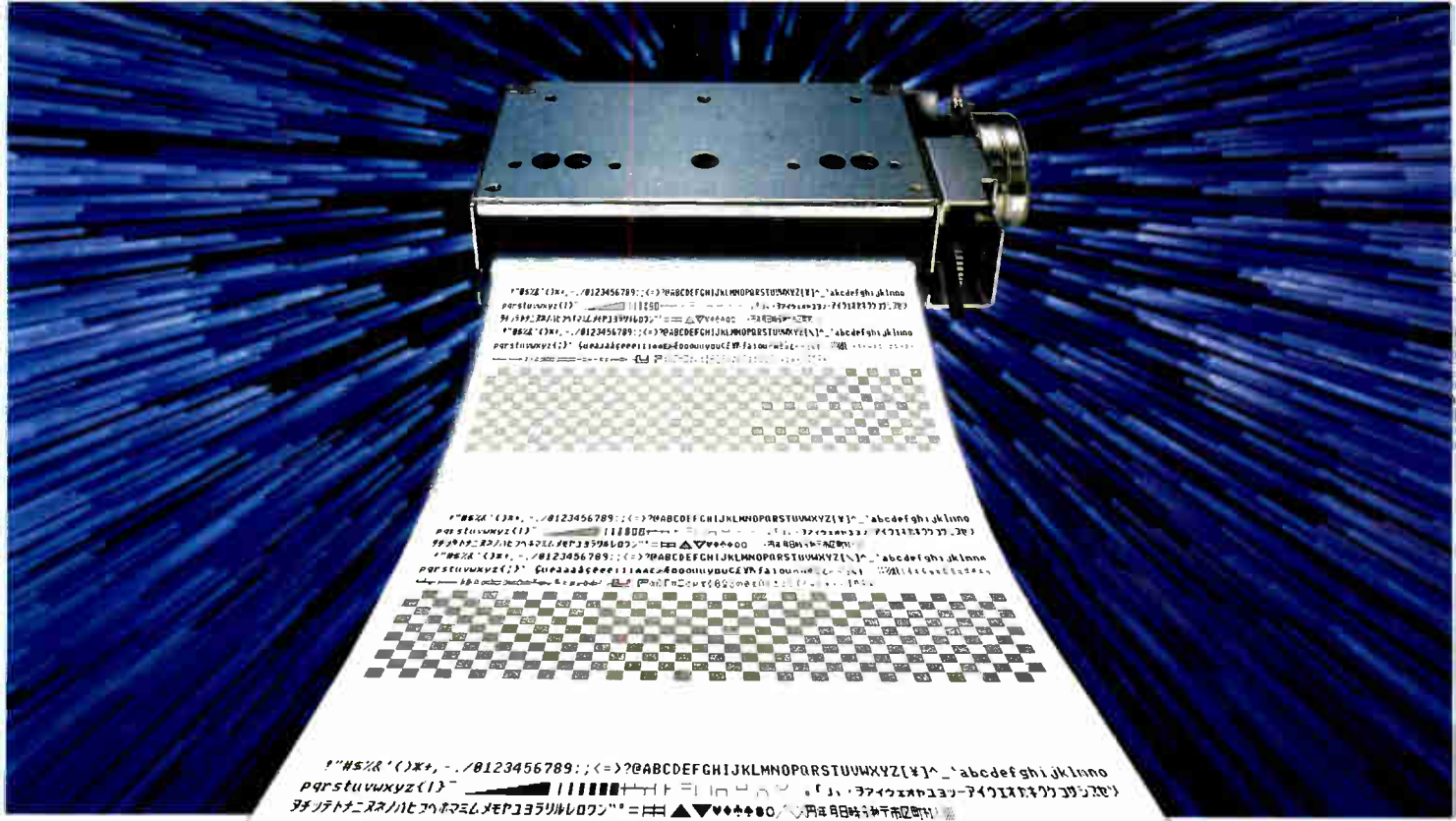
The room-temperature coercivity of the disks is 2,000 Oersteds. The magnetic field during writing is 300 Oe., and for erasing it is −300 Oe. The disks have spiral grooves on a 1.6-μm pitch, and the grooves are 0.8 μm wide and 55 nm deep. The rotation angle during read is 1.3°.

The disks' error rate is less than one in 500,000. Error correction is used in computers and other critical applications and reduces that error rate to less than one in 10^{12}.

LIGHTWEIGHTS. The bare disks measure 130 mm in diameter and weigh 80 grams. They store information in a band with a radius extending from 30 to 60 mm. The cartridges measure 135 by 153 by 11 mm and weigh 210 grams.

Sharp has also developed a prototype of a drive for the 130-mm disk. It expects to have samples of the drive ready by the end of the year. Redundancy built into the drive for error correction reduces the double-sided disks' capacity to 422 Mbytes, formatted. A Small Computer Systems Interface is built into the prototype drive.

The disks come with recording media on one side or both sides. Both the single-sided and double-sided versions can be purchased in cartridges or as hubless naked disks that drive manufacturers

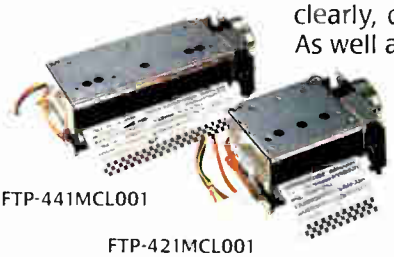


Incredible Speed! 250 dot lines/s

Ultra-high-speed High-resolution Thermal Printer FTP-441MCL001/FTP-421MCL001

Fujitsu has developed the ultra-high-speed thermal printers, the FTP-441MCL001 and the FTP-421MCL001, which can print up to 250 dot lines per second. Fujitsu's unique pressure support structure helps the head to print clearly, and the thermal head makes the printer quiet and unobtrusive.

The FTP-441MCL001 and FTP-421MCL001 print clearly, quietly, and quickly. As well as printing hard copies, they are useful for data communication, instrumentation, analysis, and medicine.



FTP-441MCL001

FTP-421MCL001

FEATURES

- High printing speed (250 dot lines/s)
- Long service life (30km: 30million pulses)
- Clear printing
- Two paper paths (One for thick paper)
- Low noise

SPECIFICATIONS

	FTP-441MCL001	FTP421MCL001
Printing method	Thermal line dot	
Dot matrix	640 dots/line	320 dots/line
Effective print width	105.6 mm	52.8 mm
Horizontal dot pitch	0.165 mm (6 dots/mm)	
Printing speed	250 dot lines/s (at 25°C and 60% RH)	
Paper width	114 mm	60 mm
Exterior dimensions (W) × (H) × (D) mm	160 × 40 × 50	107 × 40 × 60
Weight	Approx. 600 g	Approx. 300 g

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9. OG./A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
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FUJITSU

can use to design their own cartridges. The sample prices of the disks, in Japan, are as follows: ND101 (single-sided disk, no hub), 55,000 yen; ND101C (single-sided cartridge), 60,000 yen; ND201 (double-sided disk, no hub), 85,000 yen; and ND201C (double-sided cartridge), 90,000 yen. – *Charles L. Cohen*

Sharp Corp., Electronic Components Group, 8 Hachiman-cho, Ichigaya, Shinjuku-ku, Tokyo 162, Japan.
Phone 81-3-260-1161 [Circle 500]

PROTOCOL ANALYZER IS ALSO SIMULATOR

The DA-15 protocol analyzer from Wandel & Goltermann combines a data analyzer, a simulator, and a tester in a compact, easy-to-operate battery-powered instrument.

It handles data streams up to 72 Kbits/s and has 64 Kbytes of nonvolatile random-access memory for storing parameter setups and test data. Results can be sent to a printer.

Programming is primarily via soft keys. Optional interface converters are available to allow measurements on CCITT V.35 and X.21 interfaces. Other options include protocol-interpretation modules for X.25 and other interfaces.

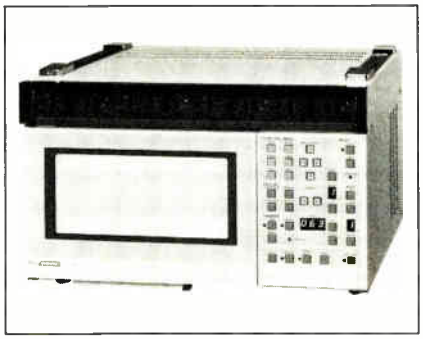
The DA-15 can also measure analog parameters such as dc and ac voltages, power level, and resistance. The instrument is available from stock, and its price depends on the importing country.

Wandel & Goltermann, P. O. Box 45, D-7412 Eningen, West Germany.
Phone 49-7121-861570 [Circle 701]

VERSATILE ANALYZER'S MEMORY IS 32 KBYTES

Graphtec Corp.'s MS5100 data analyzer is a single unit that handles input, display, calculation, recording, and data transfer generated by transducers. Based on 14-bit analog-to-digital converter technology, it can be configured with up to four input channels and offers a 32-Kbyte memory.

Analog waveforms can be measured by direct recording in the dc-to-80-Hz range and by memory recording in the dc-to-20-kHz range. A 217-by-98-mm liquid-crystal display is used to present a visual record of the waveforms, and



hard-copy records can also be generated with an internal thermal dot-matrix printer.

Cursors can be moved on the screen to select points on the waveform for the subsequent display of absolute or relative values or to zoom in on a portion of the waveform. Basic arithmetic and linear operations can be performed involving waveforms on different channels. Three trigger modes are offered.

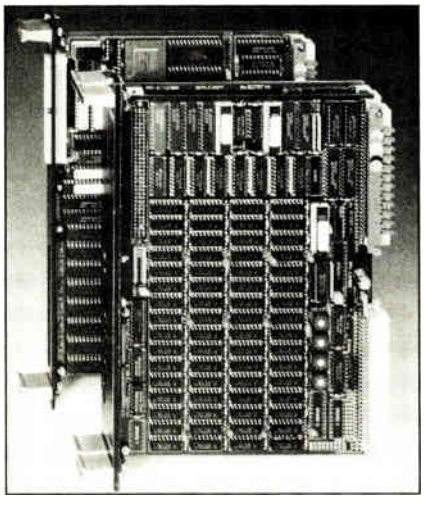
Available now, the MS5100 data analyzer costs 1.4 million yen in Japan.

Graphtec Corp., 13-16 Mita 3-chome, Minato-ku, Tokyo 108, Japan.
Phone 81-3-453-0511 [Circle 704]

IMAGER GETS FIVEFOLD BOOST IN SPEED

Eltec Elektronik GmbH's new 32-bit coprocessor board makes its PPI image-processing board set run at 15 MHz—five times faster than its previous high. The S120 does it with a high-speed video-bus interface that accepts digitized video images at pixel rates up to 15 MHz.

Several configurations of the coprocessor board are available. The highest-performance version includes a 16.67-MHz Motorola MC68020 microprocessor, an optional MC68881 coprocessor, and a local dual-port 1-Mbyte



video RAM. In all of them, video RAM is optimized to accept CPU access cycles during active image-transfer sequences, avoiding loss of processing time during acquisition.

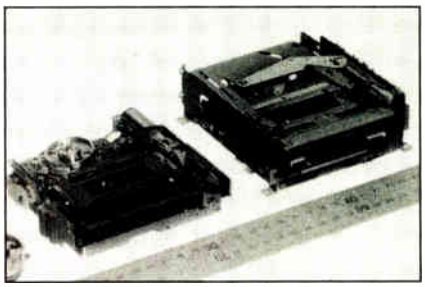
Available from stock, the S120 costs from 10,300 DM to 13,000 DM depending on configuration.

Eltec Elektronik GmbH, Galileo-Galileistr. 11, D-6500 Mainz 42, West Germany.
Phone 49-6131-50630 [Circle 705]

DAT PLAYER AIDED BY HEAD ALLOY AND PCM

Alps Electric Co.'s digital-audio-tape player/recorders use pulse-code modulation techniques and a sputtered iron-aluminum-silicon alloy in the read/write heads of the recently introduced DMRA models.

The lightweight, compact units support 8.15-mm/s tape speed and a 2,000-rpm cylinder rotation speed. They come in two configurations: a mechanism for top-loading tapes, which weighs 340 grams and measures 110 by 32 by 103 mm, and a unit for front-loading tapes, which weighs 420 g and measures 110 by



41 by 125 mm. The recording cylinders used with the devices are 19 mm high, weigh 40 g, and consume 120 mA. They are available two months after order.

Alps Electric Co. Ltd., 1-7 Yukigaya Otsuka-cho, Ota-ku, Tokyo 145, Japan.
Phone 81-3-726-1211 [Circle 707]

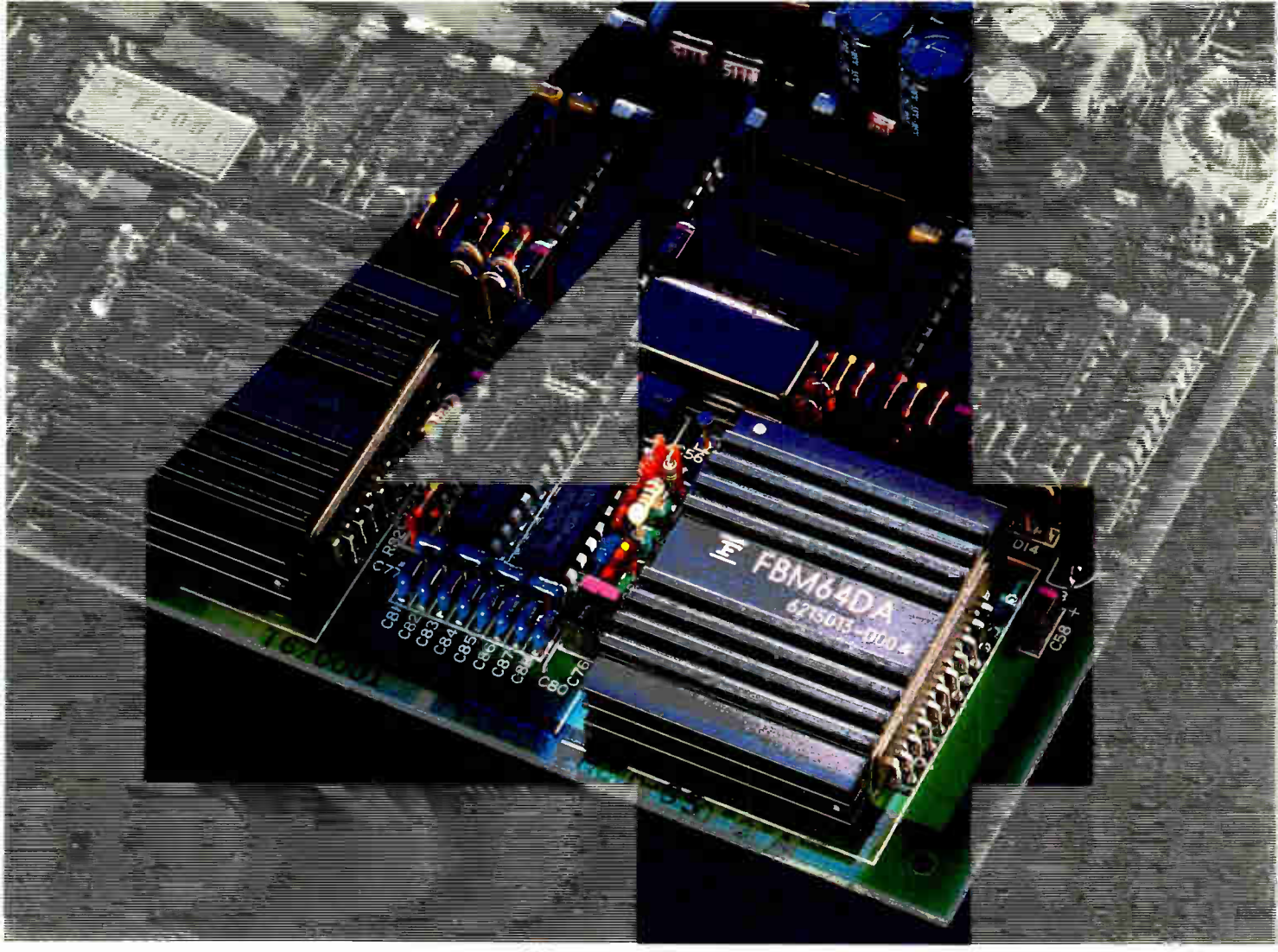
PROCESSOR SOUPS UP GRAPHICS BOARD

Tektite's graphics board for IBM Corp. Personal Computers XT, AT, and compatibles uses the Intel Corp. 82786 graphics coprocessor to achieve high-speed drawing operations and provide hardware windows.

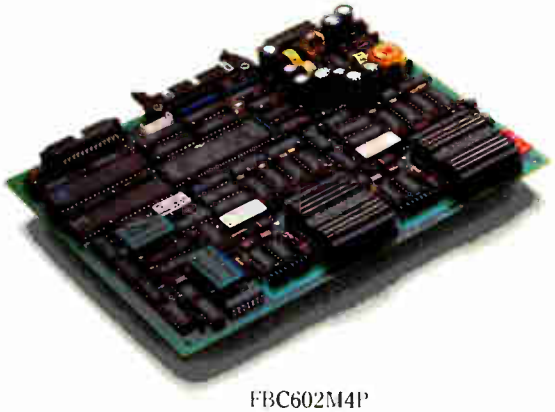
The TT786 will drive an IBM EGA monitor or CGA monitor and will share a monitor with an EGA or CGA card. When the TT786 is sharing a monitor, the CGA or EGA output appears in a dynamically resizable window on the screen.

The graphics board is equipped with 512 Kbytes of display memory. It supports a 2,000-by-1,000-pixel frame buffer and a 64-color palette.

Up to 16 windows at a time can be displayed on the screen. Bit blocks can



With 4 Mbit devices you can pack in 1Mbyte on a single bubble memory card.



FBC602M4P

Fujitsu's FBC602M4P Series of high-density bubble memory cards employ state-of-the-art 4Mbit devices that give you up to 1Mbyte memory on a single card. And up to 32MBytes using slave cards connected in series to the master card.

Coupled with easy access and selectable transfer rates of up to 800 Kb/s, you get maximum memory and optimum speed. All in one compact bubble memory card.

Specifications

Model	FBC602M4P
Device	FBM64DA (4Mbit)
Memory capacity	1Mbyte
Access time (avg.)	12.6 ms
Transfer rates	100/200/400/800 Kb/s
Interface	8-bit parallel, DMA available

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9, OG /A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
FUJITSU COMPONENT OF AMERICA, INC.:
3320 Scott Blvd., Santa Clara, California 95054-3197, U.S.A. Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355
FUJITSU LIMITED (Electronic Components International Marketing Div.)
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211
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be transferred at a maximum rate of 19 Mbits/s. Other performance features include 25-Mbit/s area fills and 2-Mbit/s line drawing.

Available now, the board costs £395.

Tektite, 9 Coolhurst Road, London N8 8EP, UK.
Phone 44-1-3412468 [Circle 706]

LOGIC ANALYZER OFFERS 48 CHANNELS

The LA48C logic analyzer from Waterloo Digital Electronics Inc. offers 48 channels, maximum clocking speeds of 20 MHz, and multiple input/output ports, all for $1,495 in Canadian currency.

The logic analyzer, which is available now, has an RS-232-C serial connection, a Centronics printer port, and a high-speed parallel interface, which allows it to be operated by an IBM Corp. Personal Computer.

Waterloo Digital Electronics Inc., P. O. Box 62, 279 Weber St. N., Waterloo, Ontario N2J 3H8.
Phone (519) 884-4330 [Circle 708]

VMEBus ADAPTER RUNS 14 SCSI PERIPHERALS

A VMEbus-host adapter card from Interphase International Corp. gives systems designers two independent Small Computer System Interfaces that can support up to 14 SCSI peripherals.

The V/SCSI 4210 Jaguar's dual-port design allows designers to dedicate one port to computer-to-computer transactions and the other to peripherals. Each SCSI port can handle up to 1.5 Mbytes/s of asynchronous data transfer or 4 Mbytes/s of synchronous data transfers.

When used with the company's Buspacket interface, which preformats data packets, the adapter card can attain VMEbus direct-memory-access rates of up to 30 Mbytes/s using its 128-Kbyte cache memory. It supports 16- and 32-bit VMEbus data transfers and 16-, 24-, and 32-bit addressing.

Both ports support the common Command Set (CCS) and virtually all vendor-specific commands. Available now, the 4210 Jaguar costs £2,200.

Interphase International Corp., 93a New St., Aylesbury, Bucks, HP20 2NY, UK.
Phone 44-296-435661 [Circle 711]

WAFER MARKER USES LASER FOR MARKING

The YL473D wafer marker from NEC Corp. eliminates contamination and cracking during inscription by using the company's YL114 YAG laser for noncontact marking in all standard fonts plus Arabic and bar-code characters.

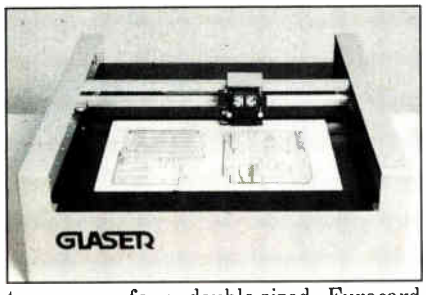
In its standard configuration, the YL473D can be adjusted to handle 4-, 5- and 6-in. wafers. Accessories are available for handling wafers up to 8 in. and as small as 2 in.

The system is controlled by a NEC PC-9801 personal computer and software that displays a variety of menu screens on a 14-in. color monitor. Available three months after order, the system costs 16.7 million yen.

NEC Corp., 1-25-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 163, Japan.
Phone 81-3-345-0781 [Circle 712]

PC-BOARD PLOTTER HANDLES 700×480 mm

Glaser AG's DP-1545 photoplotter for printed-circuit-board design artwork can handle photographic material up to 700 by 480 mm—a work area large enough



to expose four double-sized Eurocard boards.

Lines are printed with 8-μm resolution and can be placed with an accuracy of 50 μm on any point in the working area. The DP-1545 is compatible with standard graphics languages such as Gerber Scientific Inc.'s Gerber and Hewlett-Packard Co.'s HP-GL.

It can be operated directly over its RS-232-C port by most minicomputers and personal computers or by a peripheral data station using tape or floppy disk. The photoplotter is available now. The price varies with the importing country.

Glaser AG, Hölzliwisenstr., 4, CH-8604 Volktswil, Switzerland.
Phone 41-1-945-54-44 [Circle 710]

TV TUNER HAS 4 POTs, 12 SELECTOR BUTTONS

A TV tuning system from Preh Werke features 12 program-selection buttons and four potentiometers for adjusting volume, hue, brightness, and contrast. The 90004 also incorporates a memostat with an automatic frequency control switch, a video-cassette-recorder contact, and a muting contact.

Delivery time for the 90004 tuning unit is 12 weeks. It sells for 25 to 38 DM, depending on the version.

Preh Werke, P. O. Box 1740, D-8740 Bad Neustadt, West Germany.
Phone 49-9771-920 [Circle 714]

UNIT LIFTS ANALYZER SPEED TO 400 MHz

The LAS-B8 eight-channel module option from Rohde & Schwarz enhances the company's LAS logic analyzer so that it can handle measurements on high-speed logic circuits. The option's eight channels allow asynchronous data collection with an internal clock rate up

to 400 MHz and synchronous collection with an external clock signal up to 100 MHz. It provides a storage capacity of 4,000 data words.

Even at the highest sampling rate, the LAS-B8's 4,000-word memory capacity is able to hold the contents of a signal that lasts as long as 10 μs, ensuring that events both before and after the trigger event are captured. The two-level trigger facility operates without any restrictions.

Delivery time is one month, and the LAS-B8 costs 16,300 DM in Germany.

Rohde & Schwarz, Muehldorfstr. 15, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 709]

RECORDER BUFFERS DATA IN 30-KBIT RAM

Monode Ltd.'s portable Data Recorder guards against power interruptions by buffering data in a 30-Kbit random-access memory before it is written on a floppy disk and by backing up the RAM with a three-month battery supply.

The device also protects data integrity by automatically compensating for voltage fluctuations as low as 50% of rated voltage and identifying and marking defective parts of the disk. The recorder plugs into 240-V and 120-V power mains.

It accepts ASCII or 8-bit binary data from process-control units, oscilloscopes, multimeters, and other test equipment over an RS-232-C port. To reduce operator error, disk formatting is automatic. Available now, the Data Recorder costs £995 in the UK.

Monode Ltd., 12-14 Market Square, Leighton Buzzard, Bedfordshire, LU7 7EY, UK.
Phone 44-525-381899 [Circle 713]

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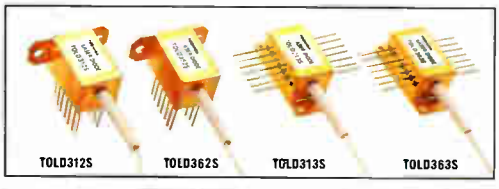

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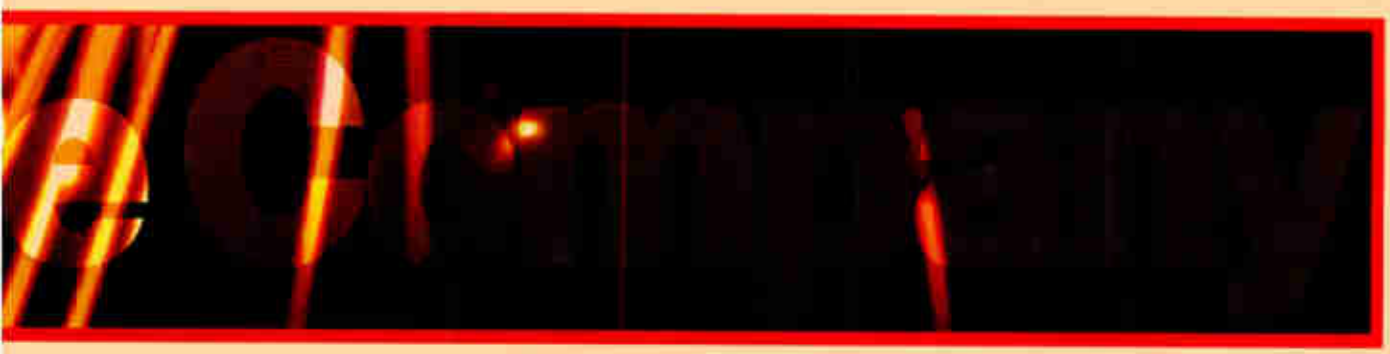

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INSIDE TECHNOLOGY

GENRAD'S PC BOARD TESTER DOES IT ALL

The company gambles on a unit that runs functional and in-circuit tests—and more—on boards stuffed with analog, digital, custom, and ASIC parts

by Jonah McLeod

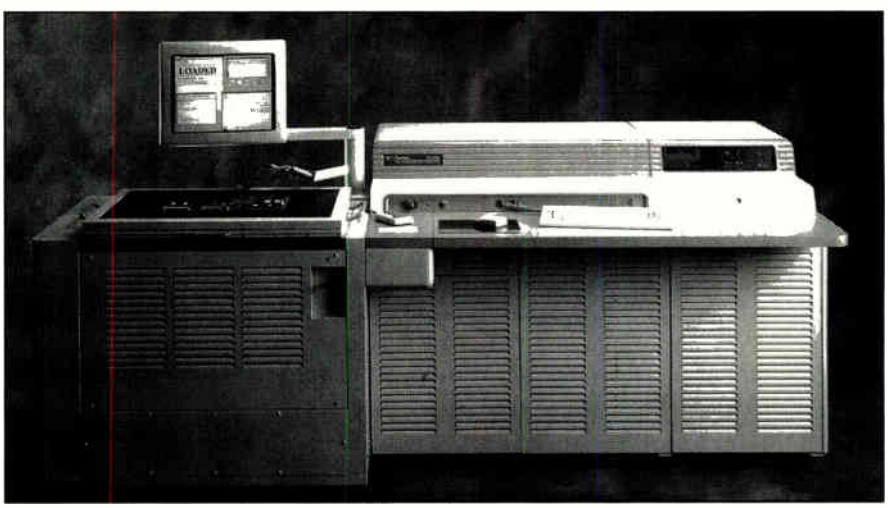
Systems makers who need to test loaded printed-circuit boards face a problem that looks as if it can only get worse. They must choose from a growing assortment of systems that each employ a different testing strategy that does only part of the job. Functional testers, for example, test boards from the edge connector, while in-circuit testers test individual components inside the board. More recently, combined testers have gone on the market that test individual components and small areas of a board by employing in-circuit isolation techniques and then doing functional tests.

And with pc boards being loaded with a growing number of increasingly complex chips, testers must provide sophisticated timing analysis, enough random-access memory to store formidable test patterns, and the power to generate those patterns. These new boards are a test engineer's nightmare: they are packed with analog and digital circuitry, semicustom and custom application-specific logic, random-access memories, and powerful microprocessors and their buses.

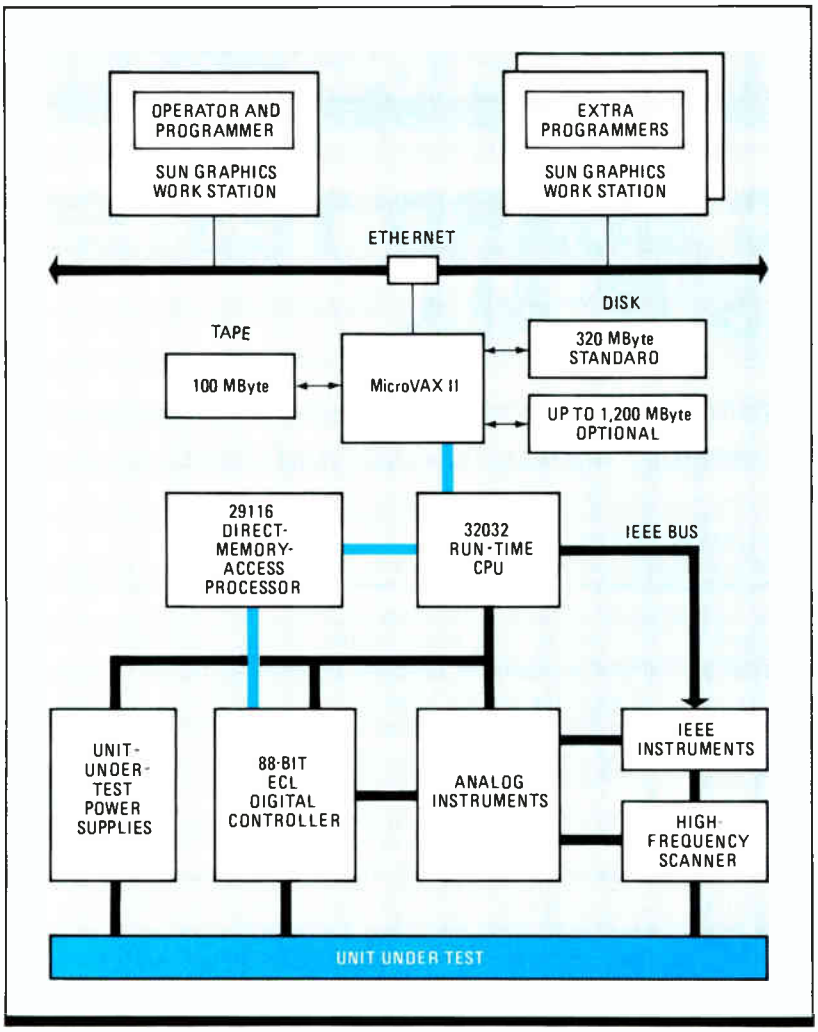
But now there is a single board tester that offers a wide variety of testing techniques to handle present and next-generation pc boards packed with every kind of the latest and most complicated chips: the GR2750 from GenRad Inc. The 2750 can do both functional and in-circuit testing, and the Concord, Mass., maker of automated test equipment claims it is the first board-test system that can provide concurrent analog and digital testing in real time. For testing the newer, more complex digital components, the tester has 64-Kbits of RAM per pin. To test large RAMs, the 2750 has a new digital control unit found on the GR160 and 180 VLSI chip testers but not on any other board tester. This unit can generate an infinite number of test patterns to test the largest memories that can be manufactured. Also, the new GenRad tester has a timing generator producing eight timing cycles to emulate any commercial or proprietary microprocessors and their buses in real time. Other board testers, with a single-cycle timing generator, must use a known-good example of the microprocessor to perform this bus emulation.

To manage the large amount of test data, there is a new test programming environment—Genesis (GenRad Extendable Strategy-Independent Software). It contains a single data-base management system built around the Frames model developed by the Massachusetts Institute of Technology. For the first time in the board-testing world, test engineers developing test programs and technicians running finished tests are all accessing data from one single data base.

The GR2750 is a key element in GenRad's bold new strategy to focus its development efforts and product offerings. In the past two years, the company has



1. COMPLEXITY MANAGER. The GR2750 tester handles printed-circuit boards with analog or digital parts, or both, and a computer subsystem quickly generates large test programs.



2. FLEXIBLE HARDWARE. The tester includes a CPU, DMA processor, and a digital controller; the computer subsystem is built around a MicroVAX II.

been fighting to regain its lead in board testers and to return to profitability (see p. 62).

At the core of the tester is a proprietary National Semiconductor Corp. 32032-based run-time CPU that executes the test program and an AMD 29116-based direct-memory-access processor that loads stimulus and response patterns into an 88-bit emitter-coupled-logic digital controller (see fig. 2). The controller actually applies the test patterns and checks the response of the device under test.

The subsystem also features the five analog instruments that measure all the analog signals found on a board. The group consists of four ac and dc source and measurement meters and a time and frequency meter. Testing beyond the capability of these five calls for IEEE-488 instrumentation, which can be added onto the GR2750. Overseeing the analog instruments is the job of the CPU, which handles the analog portion of mixed-signal testing. "The percentage of mixed-signal designs is increasing," remarks Richard J. Faubert, vice president of new product development. "In our survey of 22 ASIC companies, 18 said they plan to offer mixed-signal processing."

The GR2750 is the first to allow synchronized analog and digital testing. If a pc board is loaded with a digital-to-analog converter, the tester is able to apply a known digital stimulus to the input and synchronously measure the analog output that results. "For boards that contain both analog and digital components, conventional testers perform static mixed-signal testing," Faubert says. "They run a few test steps on the digital controller, stop, and then run a few steps on the analog controller."

The tester can simultaneously measure eight analog signals, each at a frequency of up to 10 MHz. Alternatively, it can take on four analog high-impedance and four analog matched-impedance signals, with frequencies topping out at 50 MHz. Other testers handle up to six analog signals at frequencies between 100 kHz and 1 MHz.

Now that ASICs regularly turn up on boards, testers need ample memory to store the complex patterns that put them through their paces. Genrad's system allots an unprecedented 16-Kbit-by-4-bit RAM to each pin. Its rivals back each pin with no more than 4 Kbits. The job of loading the patterns falls to the DMA processor, explains Redmond Aylward, product marketing manager. Once the patterns are loaded, the CPU executes the test program.

One hardware element that greatly eases the testing of sophisticated boards is the custom ECL digital controller. Its 88-bit instruction word enables it to handle the structured logic characteristic of memories, as well as the random logic characteristic of ASICs, microprocessors, and their associated buses.

To handle the increasing amount of RAM on pc boards, 56 of the instruction word's 88 bits produce algorithmic test patterns to read from and write to every location in memory. With 56 bits, the controller can manipulate many addressing modes and operation codes.

Within the controller are the clocks, triggers, driver/sensors, and hybrid scanners that allow the tester to apply a wide range of stimulus patterns and to check the associated responses. Three more of the 88 bits go to generating eight timing cycles.

Twenty more bits control clock generation, synchronization, and triggering. Such timing capability makes it possible for the tester to take different microprocessors and bus-structured boards in stride.

Since the tester generates up to eight timing waveforms for each test cycle (applying a stimulus, detecting a response), it can also accurately

reproduce the complete bus cycle for any microprocessor at that microprocessor's clock rate. Until now, testers could generate only one bus cycle for each test cycle. "The test system clips along with a 10-MHz test cycle in normal mode, producing a stimulus and checking a response every 100 ns," says Faubert. "It jumps to 20 MHz in an interleaved mode so it delivers the same sequencer steps every 50 ns."

Of course, all the hardware in the world doesn't help without equally powerful software. The Genesis programming environment contains an object-oriented hierarchical data-base management system that is built around the Frames data-base model developed at Massachusetts Institute of Technology.

The programming hardware is a MicroVAX II from Digital Equipment Corp., Maynard, Mass,. and one or more graphics work stations from Sun Microsystems Inc., Mountain View, Calif. The MicroVAX manages the data base, which is shared by the tester and computer subsystems.

A joint data base ensures consistent test programs. Information in the data base is represented as test objects such as circuit descriptions, strategies, and description of test fixtures. Each object is shown pictorially and described in text on the user interface. The manager retains all the information on the unit under test: simulation model, test plan, test modules, connectivity data, and the like. Schematics, simulation models, timing data, and so on are added to the data base via the ADSF (assembly data-set format) loader, allowing the tester to take advantage of data used in designing the pc board. With such information at his fingertips, a test programmer converts the design data into test vectors that translate into optimum fault coverage for the unit under test.

In addition to the data-base manager, the tester is shipped with four applications programs. ATG is an automatic test generator that handles in-circuit testing; Hilo is a logic-simulation system; Hitest is a test-generation utility; and Hichip is a universal hardware-modeling package. The ATG package generates the tests for analog and digital components or the digital function tests. Hilo and Hitest are completely integrated for real-time design and testing. □

For more information, circle 480 on the reader service card.

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LONGEVITY PAYS OFF FOR GENRAD'S GR2750 DESIGN TEAM

In an era when hardware and software designers are a highly mobile breed, it is unusual to find a group of engineers that have worked together on more than one major system. But the members of the team that built GenRad Inc.'s GR2750 are long-time co-workers. Matthew Fichtenbaum, the hardware architect for the GR2750, and Mark Swanson, the software architect, were on the design team for both GenRad's first-generation 1790 series printed-circuit-board tester and the second-generation 2270 series.

Fichtenbaum goes back more than 20 years with GenRad. As a co-op student from the Massachusetts Institute of Technology in Boston, he designed a test fixture for GenRad that would later become its first pc-board tester. He gets the credit inside GenRad as the driving force behind the new test system, although his own description of what he did is matter-of-fact: "I was the designer on some parts of the system and consultant to the designers of other parts of the system," says Fichtenbaum.

Just as the hardware bears Fichtenbaum's mark, the software architecture bears Swanson's signature. "Mark made three quarters of the system's complexity understandable to the rest of the design team," says Fichtenbaum. Swanson did the initial high-level software design and broke it into pieces that other software engineers could implement.

"Mark was the architect of the notion of one single central data base to handle all of the test data being created by test-development engineers to also be used by production engineers," says Redmond Aylward, product marketing manager for the GR2750. "He was the man responsible for the easy-to-use user interface, too."

Like Fichtenbaum and Swanson, Aylward and Chester Gapinski, the engineering project leader, and Richard Case, the engineering manager, are all long-time GenRad hands. All had worked on the second-generation GR2270.

On the GR2750, Case was the project leader in the first phases of development of the system. He had to ensure that the architecture defined by Swanson actually got implemented. He is now software project leader in the ongoing development and refinement of software, according to Fichtenbaum. Gapinski was the project leader responsible for the hardware development from the early prototype on.

Aylward, a hardware designer on the 2270 project, was one team member whose job changed over into marketing on the 2750 project. His competitive analysis of the market in the early phase of the project helped to determine what features to add to and remove from the 2750 after the initial product-definition phase.

LONG-TERM TEAM. (From left, rear) Fichtenbaum, Swanson, Aylward, and (from left, front) Gapinski and Case.

GENRAD'S TURNAROUND GATHERS STEAM

It still has a long way to go, but GenRad Inc. seems well under way now on a major turnaround effort. After losing its lead in board test systems, the Concord, Mass., manufacturer took stock in late 1985 and decided that strong measures were needed if it was ever going to regain its former market position. So it reduced its overall employment by one-third, cut the middle-management staff in half, named a new day-to-day manager, and consolidated the company into just two divisions.

Most important, though, was GenRad's major shift in product-development activities. It cut back on both the money it was spending and the number of products being developed. And in a bold shift in strategy, the company focused all of its development money on just a handful of new products, the most important of these being the new GR2750 board test system (see p. 59). Indeed, the company expects that the all-purpose tester will add as much as $20 million in new revenue this year, 10% of forecasted revenues. Next year, the tester could account for as much as $50 million.

Casual observers might question how any company that lost $1.4 million on sales of $51 million in the first quarter of 1987 could be well under way toward a recovery. But, comments Richard G. Rogers, the new chief operating officer, "when you've been losing almost $10 million per quarter for seven consecutive quarters, a loss of $1.4 million looks pretty good on the upside."

GenRad had 1986 revenues of $204.3 million and reported a net loss that year of $29.8 million. In 1985 the loss was $52.2 million on revenues of $218.3 million. A big part of the problem was the overall industry recession, which hit ATE companies especially hard. The company's most recent profitable year was 1984, when it reported net income of $10.9 million on revenues of $249.4 million.

Even if the ATE market remains flat, GenRad should move out of the red this year. Carolyn Rogers, an industry analyst who covers semiconductor capital equipment at the venture capital, investment banking, and brokerage firm of Hambrecht & Quist Inc. in San Francisco, estimates that GenRad should generate 1987 revenues "in the $230 million range." Besides the $20 million expected from sales of the GR2750, $10 million in 1987 revenues should come from another new product called the GR125,

A leaner, more focused GenRad gambles plenty on three new testers

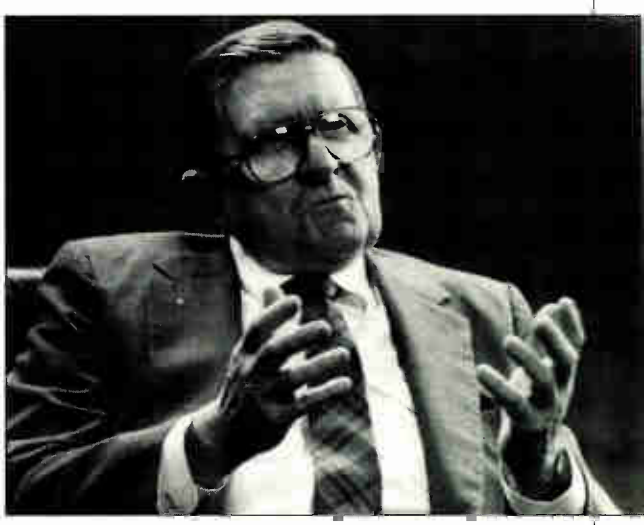
which was announced in May 1986. The low-end test system for VLSI circuits sells for $175,000 to $400,000. These products are two of the three key testers being announced this year that GenRad is gambling on to regain its market dominance. That strategy, which was conceived in September 1985, also includes the accelerated development and introduction of new products, a firmer hand in managing assets and the balance sheet, and a return to profitability as soon as possible. The 1985 plan came from an "office of the president," which was established to halt GenRad's slide in what chief financial officer Charles E. Peters Jr. calls "the darkest days in recent years."

The office of the president, which was dissolved when Rogers became chief operating officer a year later, consisted of president and chief executive officer William R. Thurston, Rogers, Peters, and Robert E. Anderson, senior vice president for the Semiconductor Test Group. Thurston worked his way to the top after joining General Radio Co., as it was called then, as a co-op employee from the Massachusetts Institute of Technology in 1941. He directed the office of the president as well, and he characterizes Rogers' appointment as "a great boon."

Rogers, a 26-year GenRad veteran, stepped in as chief operating officer last September. He had been group vice president responsible for the company's largest unit, the Electronic Manufacturing Test group, which builds test systems for circuit boards. Rogers reports to Thurston, who relinquished day-to-day operating responsibilities to focus on strategic planning. Dick Rogers was a good choice to direct GenRad's operations, declares Hambrecht & Quist's Rogers. In her opinion, he "is a nuts-and-bolts, get-things-done kind of guy." She says Thurston is better "at taking the overall view and is good as a visionary for future products and company directions."

Getting things back in order certainly hasn't been easy. Harking back to those dark days, Thurston says, "We saw early how serious the recession was, and we

AT THE HELM. GenRad chief operating officer Rogers, below, consolidated six divisions into two. Company president Thurston, right, took steps to downsize the company when he saw how bad the recession was in September 1985.



took steps to downsize the company." But it fell to Rogers a year later to enact most of the hard measures needed to bring the company's operations under better control.

Among the tasks that Rogers had to direct were the consolidation of six operating divisions into the Semiconductor Test and Electronic Manufacturing and Test divisions, trimming middle management from 22 to 11 positions, pruning the payroll from 3,300 in September 1985 to some 2,200 at the beginning of the year, cutting inventory from $85 million to $49 million since the fall of 1985, and instituting accounting procedures that include not listing any order in the backlog that won't be delivered in six months.

Such strict measures can be detrimental to employee morale, but Rogers says morale at GenRad is still good. "I'm astounded by the resilience and loyalty of the workforce here. Those who are left are here because they want to be. We've had lower than average turnover rates for the locale in all our facilities," he says.

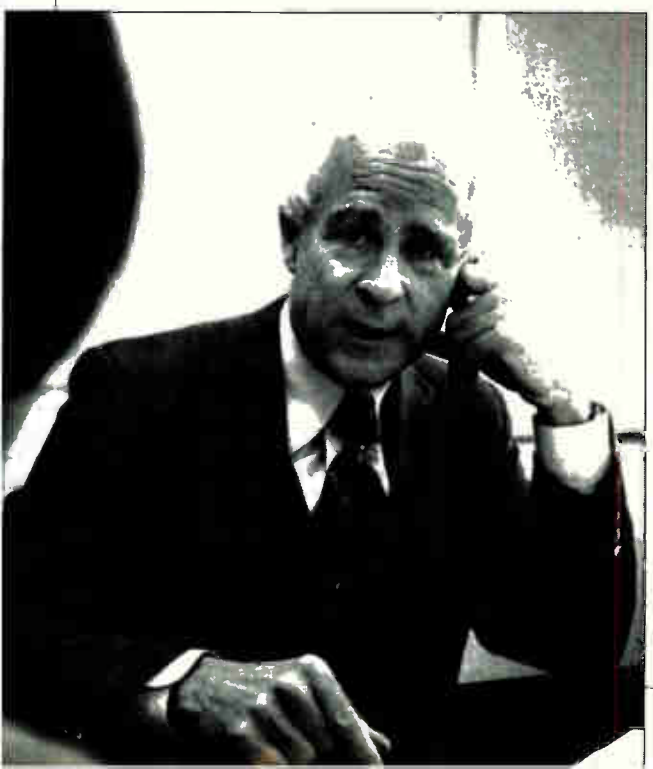
The ATE industry, in Rogers' opinion, lives or dies on new products. The trick is to make sure that the important product-development efforts are funded. Toward that end, GenRad recently installed a five-step product review stressing substantial justification in the early steps. It's intended to catch questionable projects before they become a drain.

Overall, GenRad has cut back on research and development from a level of 21% of sales two years ago ($45.5 million) to an expected 14% to 16% of sales ($30 million to $33 million) this year. Even at the lower figure, the percentage is at the high end for ATE companies, Rogers maintains.

The handful of major products being developed by GenRad have not been affected by its R&D cutback. The GR2750, for example, has received more than $25 million to date—$10 million of that last year. It was Rogers' management philosophy that caused GenRad to focus on a limited number of very important programs "so that the managers of those programs have the resources they need to get the job done," he says.

The company expects profits to flow this year even in a flat market

GenRad dominated functional board testing in the late 1970s with its GR1796, says Hambrecht & Quist's Rogers, then in effect abandoned the market by failing to follow that product up. That left Teradyne Inc. as the main contender in functional board testing, "a situation that will change with the introduction of the GR2750," Carolyn Rogers says, adding that she regards it as "a fine machine." A dozen of the new systems have already been delivered to beta sites and to selected customers.



Rogers is also high on the GR125, which should open new territory for GenRad: semiconductor test systems selling for $100,000 to $600,000. That segment should see above-average growth, she says, because the demand for these low-cost testers has been largely ignored by most vendors of high-end VLSI test systems.

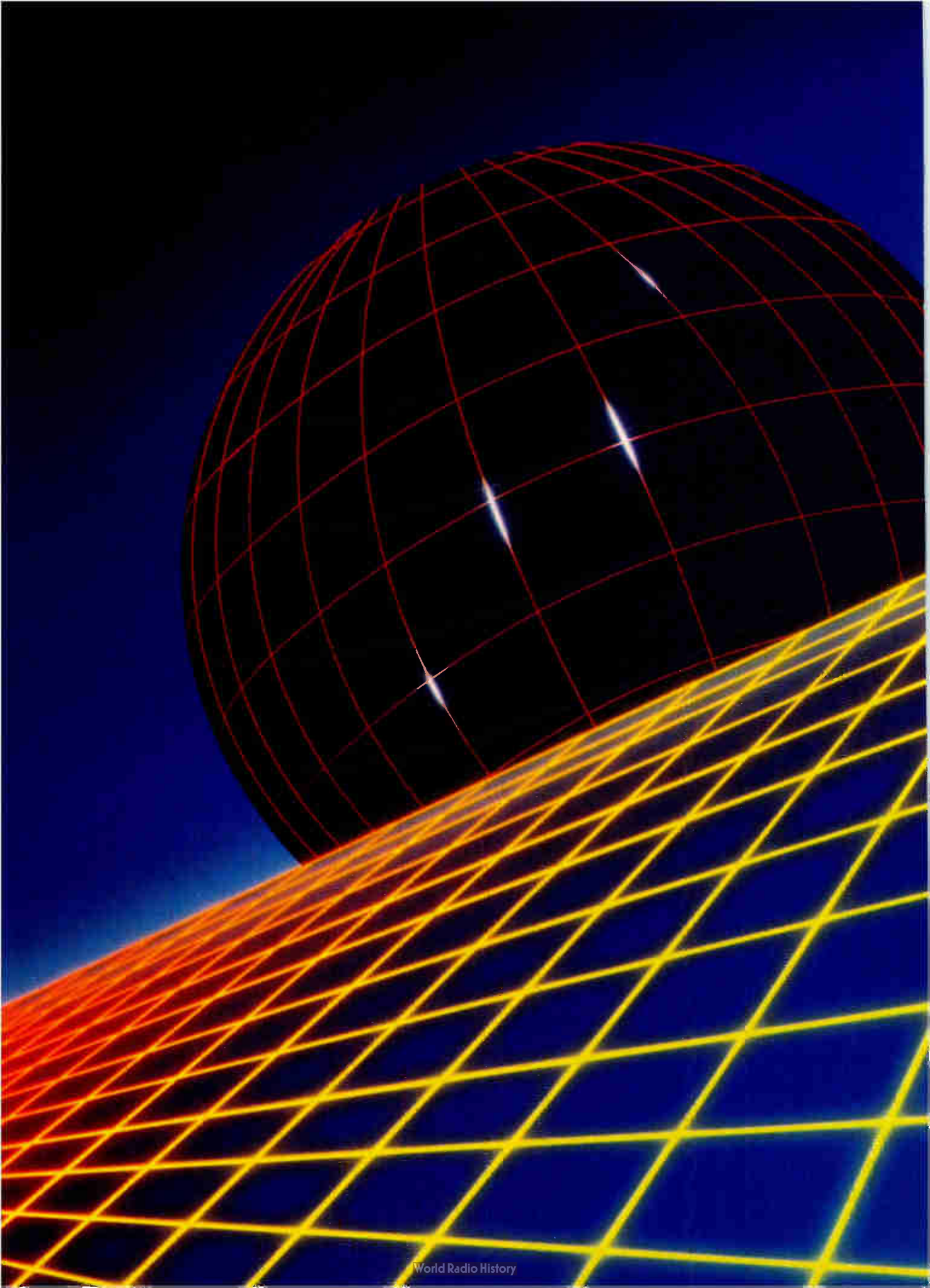
Still to come is the GR300, being announced this month. A VLSI test system intended primarily for characterizing application-specific integrated circuits, it employs a "resource per pin" architecture and will offer the accuracy and timing system performance usually associated with shared resources. The GR300 will go for $500,000 to $2 million; beta-site installations should be in operation by early next year.

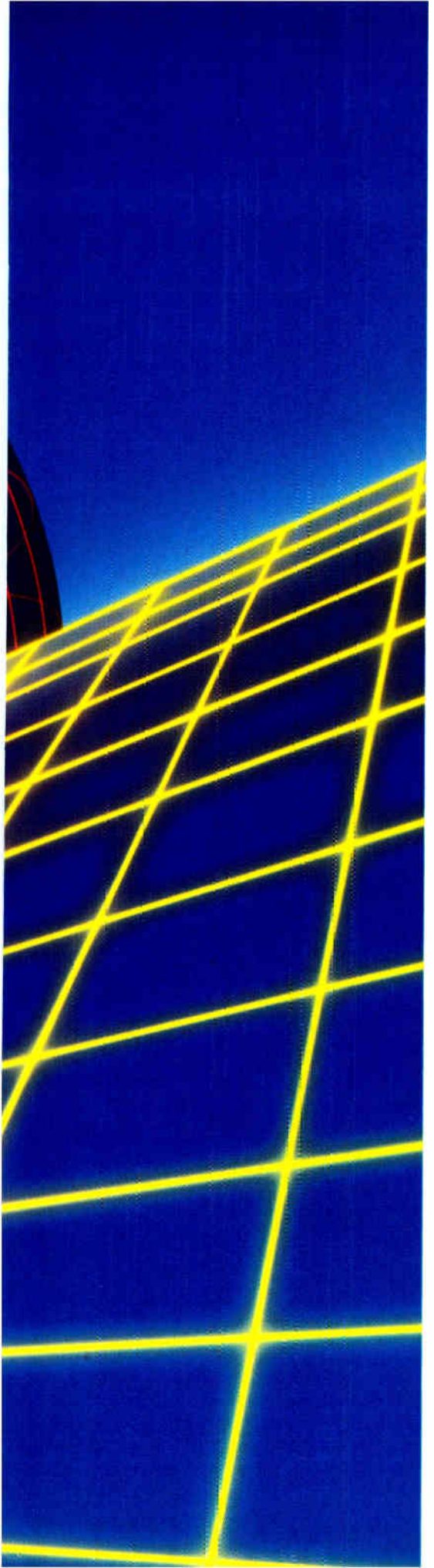
GenRad's Rogers points out that such products reflect the "important program" emphasis he favors, but they aren't the only significant fruits forthcoming from those programs. Their availability, plus a favorable ATE market outlook, should accelerate the pace of GenRad's recovery, he figures. Because the U. S. semiconductor outlook this year is getting more promising, analyst Rogers sees renewed demand for capital equipment continuing into 1988.

Those are good signs for GenRad. Dick Rogers believes the company should have no trouble showing a profit this year, even without an end to the industry's recession. But there's still a tough row to hoe before he'll feel sure that the company is sustaining the discipline that's bringing about its recovery. For example, one of the ways GenRad was so successful at reducing inventories was its switch to just-in-time controls at its Semiconductor Test Division facilities—18 months ago in Phoenix and 10 months ago in Milpitas, Calif. The board-test operations at the Electronic and Manufacturing Test facilities in Concord and Bolton, Mass., are only now beginning similar just-in-time efforts.

Taking three years for GenRad to turn around—that is, by late next year—is sensible, CEO Thurston says. "These things couldn't have been accomplished in just 18 months," he asserts. "We're in great shape internally, but once the company and industry turnarounds are well along, we have to remember the lessons of this recession and not relax the strong controls that we've established."

–Lawrence Curran





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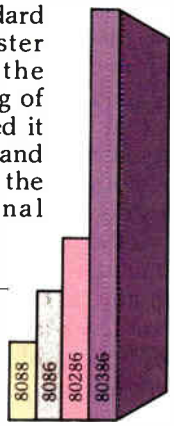

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SPECIAL REPORT: THE DRIVE FOR IC TEST-BUS STANDARDS

Two designs are picking up support—one from the military, emphasizing self-testing, and one from the civilian world, aimed at cutting board test costs

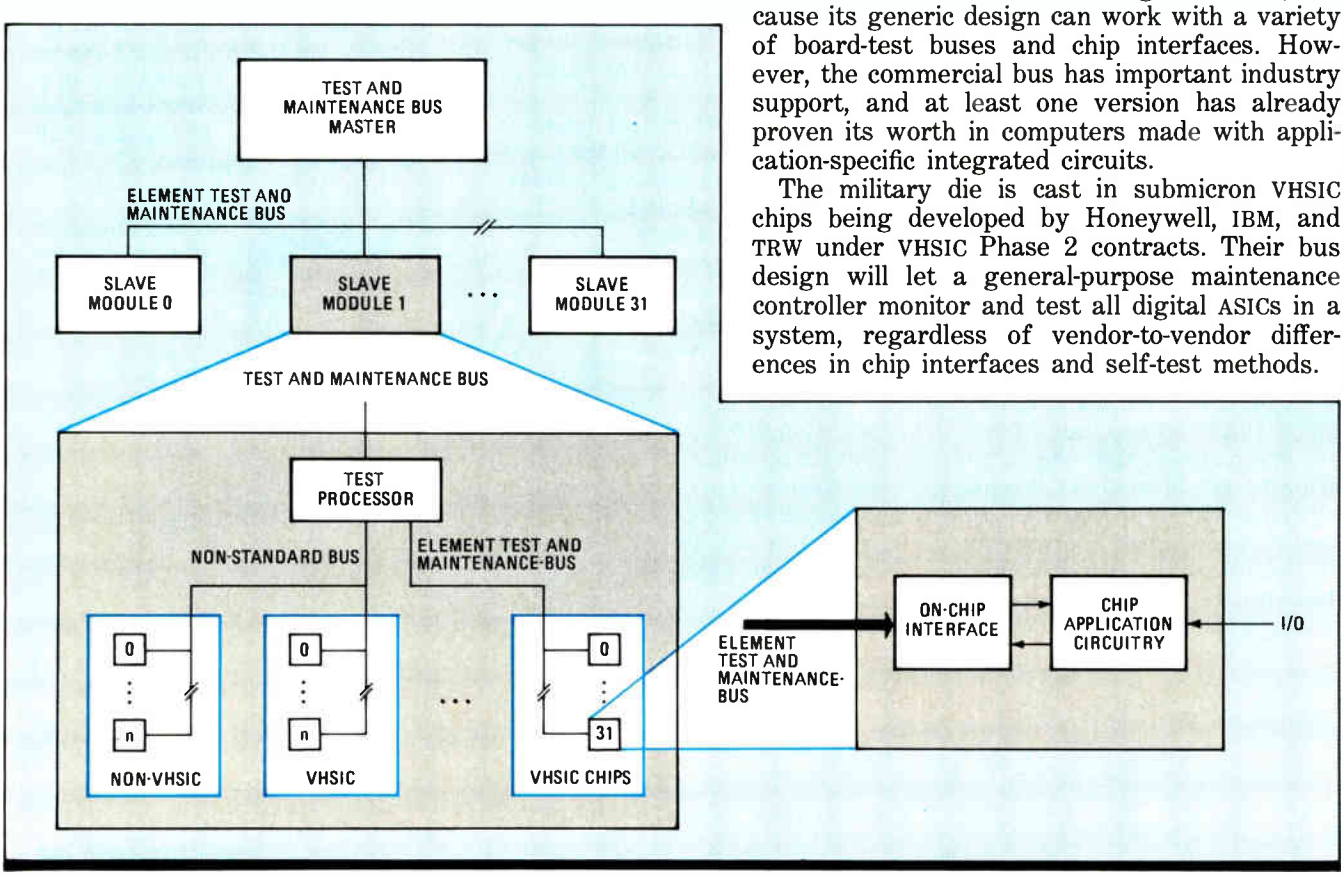
by George Sideris

Efforts to standardize test buses for integrated circuits are converging on two different buses, one military and one commercial. Both are serial buses that will employ self-test circuitry in new ICs to speed equipment testing and maintenance. They differ mostly as a result of the goals their designers had in mind as the buses were being developed.

The U. S. military wants a bus that can work in systems that will test themselves, so designers working in the Very High-Speed Integrated Circuits program developed a bus that emphasizes self-testing of systems built with chip technology developed under VHSIC. The leading contender among the commercial buses, on the other hand, initially will be targeted at cutting what one leader of the standardization effort calls the "intolerable" costs of testing boards carrying general-purpose chips linked by surface-mounted glue-logic devices. A committee affiliated with the Institute of Electrical and Electronics Engineers is working on a proposal for a test-bus standard that will try to iron out the differences.

The VHSIC bus is the leading candidate, because its generic design can work with a variety of board-test buses and chip interfaces. However, the commercial bus has important industry support, and at least one version has already proven its worth in computers made with application-specific integrated circuits.

The military die is cast in submicron VHSIC chips being developed by Honeywell, IBM, and TRW under VHSIC Phase 2 contracts. Their bus design will let a general-purpose maintenance controller monitor and test all digital ASICs in a system, regardless of vendor-to-vendor differences in chip interfaces and self-test methods.



1. MILITARY BUS. Developed mostly by Honeywell for self-testing military systems, the VHSIC test bus will make it possible for a maintenance controller to monitor and test all digital application-specific ICs on up to 32 boards carrying chips or chip sets from multiple vendors.

The leading commercial test bus is being promoted by an industry committee called the Joint Test Action Group, composed of major European and American equipment manufacturers. JTAG is backing a technique called boundary scan for testing microprocessors, ASICs, and other complex merchant-market chips. The technique's big advantage is that printed-circuit wiring and glue logic between these chips can easily be checked for faults through the test bus. Sparked by Philips of the Netherlands, the group is currently forming a U. S. chapter under the aegis of AT&T Co. (see story, p. 71).

A Testability Bus Standardization Committee is being formed to recommend an industry standard to the IEEE. Besides the VHSIC and JTAG buses, a proprietary bus design for analog and digital testing from Logical Solutions Technology Inc., Campbell, Calif., is a candidate. The committee also hopes to standardize the way chips with built-in test circuitry are production-tested. Otherwise, warns a cochairman of the committee, test-equipment costs could skyrocket.

The Department of Defense wants its systems to be capable of verifying their own operational readiness. In line with that goal, Honeywell, IBM, and TRW, who are developing the VHSIC program's Phase 2 submicron technologies, have been working through an interoperability committee. They have agreed on a design that will enable a single general-purpose maintenance controller to monitor and test all digital ASICs on up to 32 boards containing chips or chip sets from multiple vendors (see fig. 1).

Architecturally, the bus resembles a data-communications network. A bus master communicates with slave devices via a multidrop test-and-maintenance link called the TM bus. The TM bus has protocols for monitoring, testing, and maintaining modules, and four lines. One serial line carries command and data packets to slaves, another returns acknowledgement and data packets, and the other two lines distribute bus-control and clock signals.

Board-test processors interface the TM bus to VHSIC and other chip-test buses. Each VHSIC bus for element test and maintenance, or ETM, interconnects up to 32 devices. ETM buses can be configured as star networks for master-slave communications, or as rings for looped slave-to-slave communications. Besides communicating directly with masters via the two serial data lines, the devices can operate in a scan mode (scan buses move test data through a series of chips and collect responses). Self-testing chips will use an interrupt line to report faulty operation. Three other ETM-bus lines carry slave-select, mode-control, and clock signals, for a total of six lines.

Most of the bus-design work was done at Honeywell's Plymouth, Minn., space systems facility. The three contractors are now developing numerous ETM-compatible chips, according to LaNae Avra, a Honeywell engineer who represents the bus designers on the IEEE committee. Avra will soon present the design formally to the committee. She says it's more generic than JTAG's design because, "The ETM bus has simple protocols, and you can specify your own instructions. It allows you to put an interface on your chip for whatever self-test is needed."

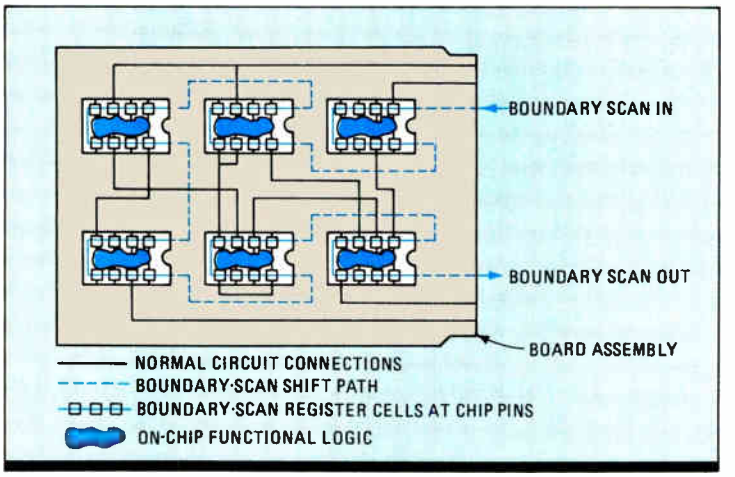
In VHSIC systems, the TM bus will go into a 32-module backplane along with a 16- or 32-bit interface and control bus designed by IBM (other buses will carry operational data). A bus simulator and other design tools have been developed at military laboratories for system designers.

Neither the TM nor the IBM bus is a military standard as yet. But both have been reviewed for tri-service suitability by a joint Army, Navy, and Air Force committee, according to the Navy member, J. P. Letellier, of the Naval Research Laboratory in Washington.

On the civilian side, a growing number of chip manufacturers already offer test-bus interfaces on self-testing ASICs. Self-test circuitry has also been going into advanced microprocessors. However, neither approach offers much relief to equipment manufacturers who must test boards built with mixed bags of components. AT&T's Rod Tulloss, who is organizing JTAG's U. S. chapter, says 80% of the cost of one new AT&T manufacturing line was for test equipment. "We cannot tolerate that. We need boundary scan to check interconnects and glue without mechanical probing. Once we have that access we can go to self-test modes for boards and systems."

Tulloss is supervisor of integrated testing at the AT&T Engineering Research Center, Princeton, N. J. So far, he reports, the new JTAG chapter has a core working group of about a dozen members, plus about 100 correspondents. He's asked them to comment on the proposed standard by July.

Boundary scan, originally developed for testing ASIC assemblies, simplifies functional testing, as a way of eliminating in-circuit testing with



2. COMMERCIAL BUS. Boundary-scan registers in major chips enable a functional tester to check out all circuitry on the board.

bed-of-nails probing fixtures. Increases in chip complexity and the swing to densely assembled, surface-mounted devices have made both alternatives costly.

"Companies using catalog parts are stuck," Tulloss says. "To write a functional test program in a reasonable time and have anything like a known fault coverage is a preposterous task today." Also, he adds, in-circuit testers can't supply enough test-pattern storage per pin to test very complex chips and need expensive fixtures to probe SMD clusters, a problem that will get worse with silicon-on-board, silicon-on-silicon, and other very high-density devices.

"To write a functional test program in a reasonable time and have anything like a known fault coverage is a preposterous task today," says JTAG's Tulloss

For boundary scan, a two-way shift register is built into each microprocessor or other major chip. The register runs around the chip periphery and has an input/output cell for each chip pin. On a board, a test bus will link these boundary-scan registers into a scan path with a serial input line for test patterns and a serial output line for test responses (see fig. 2). Besides the serial lines, a chip's test-bus interface has a control register, a bypass circuit, two mode-control inputs, and a clock input. However, a chip needs only four test-bus pins if a normal chip output can serve as the serial output.

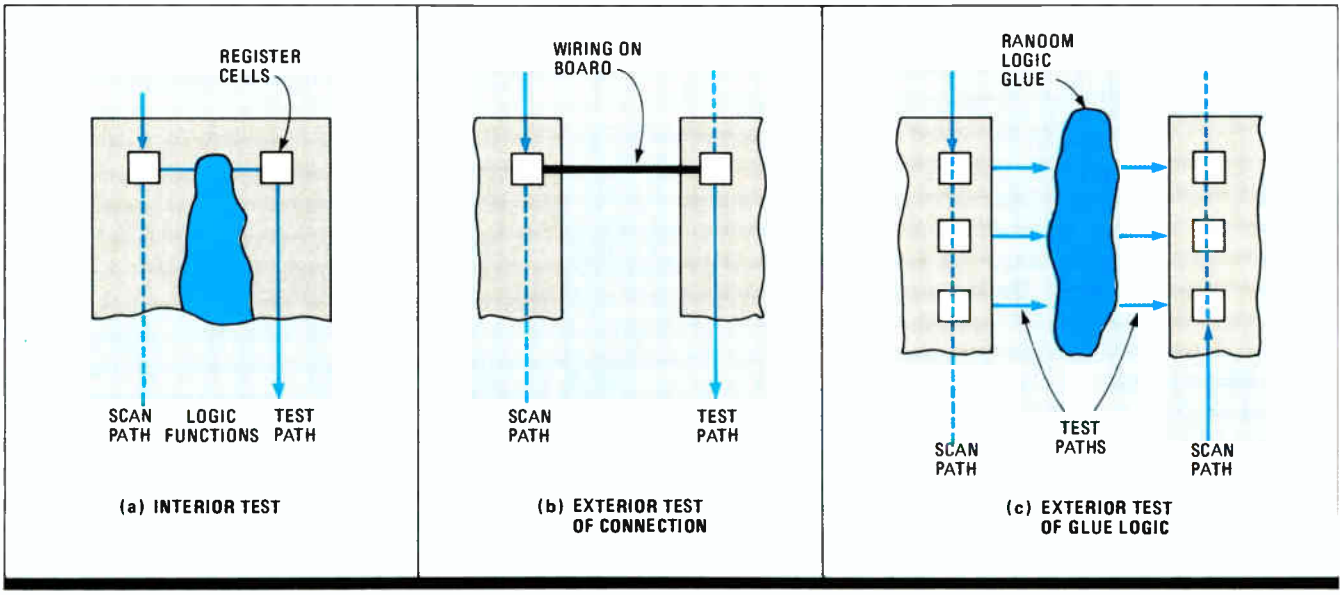
With one register cell per pin, the interface operates in an interior mode for scanning on-chip functions (or for triggering other built-in test circuitry), or in an exterior mode for testing board wiring and glue logic between the major chips (see fig. 3). In the exterior mode, functional-test patterns flow between chips through the intervening circuitry so that functional testers can easily determine whether there are faults in wiring between the chips. The division of tasks makes it easier for automatic pattern generators to churn out the functional-test programs.

Although JTAG intends to promote its interface design as a *de facto* standard, the specifications give chip designers much the same range of built-in test options as the VHSIC ETM-bus design. For example, the registers can be employed in linear-feedback modes for random-pattern generation and signature analysis.

Boundary scan has received mixed reactions from IC houses. The main bone of contention is whether the interface should be used to access built-in test circuitry. Tulloss thinks that for standardization, chip tests should not be activated, nor results read out through vendor-unique mechanisms.

Two major semiconductor companies, Intel Corp. and Texas Instruments Inc., agree with JTAG, although Anjaneya Thakar, a senior Intel engineer, argues that testing chips via boundary-scan interfaces becomes progressively more difficult with chip size. He points out that a variety of boundary-scanning chips must be developed to make test buses worthwhile and that the technique won't work unless board designers carefully position the chips for exterior testing. Nonetheless, he says, "If we have to do it, we will do it. We recognize the importance of boundary scan. It will really pay dividends when more and more chips have the interface."

Meanwhile, Tulloss notes, computers have made extensive use of test buses. As an example of what has been accomplished, he cites a supercomputer made by ETA Systems Inc., St. Paul,



3. INSIDE/OUTSIDE. In the interior mode, boundary-scan techniques are used to check the functioning of on-chip circuitry (a). An exterior mode allows the test system to send test patterns from one chip to another to check the board wiring (b) and glue logic that ties them together (c).

Minn., a Control Data Corp. spin-off. ETA's central processor is built with gate arrays containing built-in test circuitry (see fig. 4). Says Dave Resnick, the ETA fellow who designed the array, "In most cases, board troubleshooting is reduced to running the chip self-test and a chip-interconnect test. It has helped tremendously. I don't think we would have a system without it."

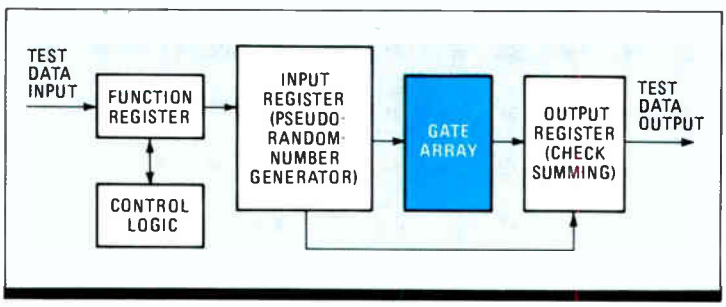
The IEEE Testability Bus Standardization Committee plans to winnow through such techniques to arrive at an overall industry standard that meets both military and industry requirements, according to cochairman Michael Stora, government business development manager, GenRad Inc., Concord, Mass. Started last fall, the committee has about 60 members in a workshop group and about 120 balloting members but is still awaiting formal authorization from the IEEE Computer Society. It was formed by Stora and cochairman Jon Turino, president of Logical Solutions Technology, which specializes in testability design.

Stora got involved because GenRad had supplied Rome Air Development Center, Griffiss Air Force Base, N. Y., with automatic test equipment for VHSIC Phase 1 chips [*Electronics*, Feb. 3, 1986, p. 42]. Each contractor came up with its own built-in-test concept, says Stora, and the lesson learned was that handling the different chip-test requirements at the new speeds and complexities would make new ATE systems very difficult to develop and could increase costs by $1 million to $2 million per tester. As a result, he says, the major ATE manufacturers want the IC industry to standardize chip-test interfaces.

Harris Corp., Melbourne, Fla., is another company that has been studying chip-test requirements. David C. Keezer, an associate principal engineer at Harris, favors the ETM and TM bus standards as a good compromise between test access and minimum bus width. "We are looking at the VHSIC design as a way to standardize component-level testing." One promising technique is to interface chips and the ETM bus through an on-chip monitor that can control different sections of a chip and activate built-in tests. The monitor is similar to an interface specified for the ETM bus and allows the chip to be tested with a scan path, boundary scan, or self-test methods.

Tulloss, though committed to the JTAG effort, calls the VHSIC bus "a nice piece of work" and adds, "We would love to see boundary scan folded into an IEEE standard, and we will interact as much as necessary to make sure that happens."

To date, Stora says, the IEEE working group has discussed only two "straw men"—the ETM bus and a more general bus developed by Logical Solutions Technology, Turino's firm—in order to define standardization issues. The latter bus, which Turino says is being used by some 17 American and European equipment makers, employs serial buses like the VHSIC and JTAG designs. It also has analog-signal test paths and a parallel mode for real-time testing. □



4. SELF-TESTER. Techniques similar to ETA Systems' gate-array self-test approach can be employed in chips on the VHSIC and JTAG test buses.

HOW JOINT TEST ACTION GROUP GOT STARTED

The Joint Test Action Group, an industry group developing and promoting an on-chip test bus for use in commercial equipment, got its start about three years ago when Philips of the Netherlands saw a need for new printed-circuit-board test methodologies to cope with increases in chip complexity.

"We were no longer able to check out boards adequately, and we felt that discussions with integrated-circuit suppliers were necessary," says Harry Bleeker, JTAG chairman and manager of computer-aided testing and computer-aided manufacturing at Philips' Telecom and Data Systems Division in Hilversum. What Philips had in mind was the boundary-scan technique that JTAG is now pushing toward standardization.

Philips realized that it could not press for common test methods on its own, so it got together with other major board producers, including British Telecom, Plessey, Marconi, and the General Electric Co., all of the UK; Thomson and Bull of France; Siemens and Nixdorf of West German ITT Europe; and AT&T in the U. S.

They formed the action group to convince IC suppliers of the need for board-level test standards. The group's first meeting was Nov. 6, 1985, in Eindhoven. Since then, seven meetings have been held to define problems, draft specifications, and streamline the organization. Colin M. Maunder, of British Telecom Research Laboratories, Ipswich, heads the technical subcommittee. Rod Tulloss, of AT&T Engineering Research Center, Princeton, N. J., is organizing an American chapter.

Bleeker is satisfied with JTAG's progress toward its goal. He reports that Texas Instruments Inc. is strongly committed to the idea; Intel Corp. has agreed to provide for boundary-scan testing in future processors; NEC Corp. of Japan has taken a positive attitude; and Motorola Inc. has shown interest. Not surprisingly, Elcoma, Philip's Electronic Components and Materials Division located in Eindhoven, also favors the standard.

JTAG is now advocating that boundary-scan cells be added to design libraries for application-specific ICs. Philips has been using boundary-scan circuitry in the ASICs and custom circuits it designs in-house and has encountered no problems, Bleeker says. *–John Gosch*

HOW A CACHE CONTROL CHIP SUPERCHARGES 386 PROCESSOR

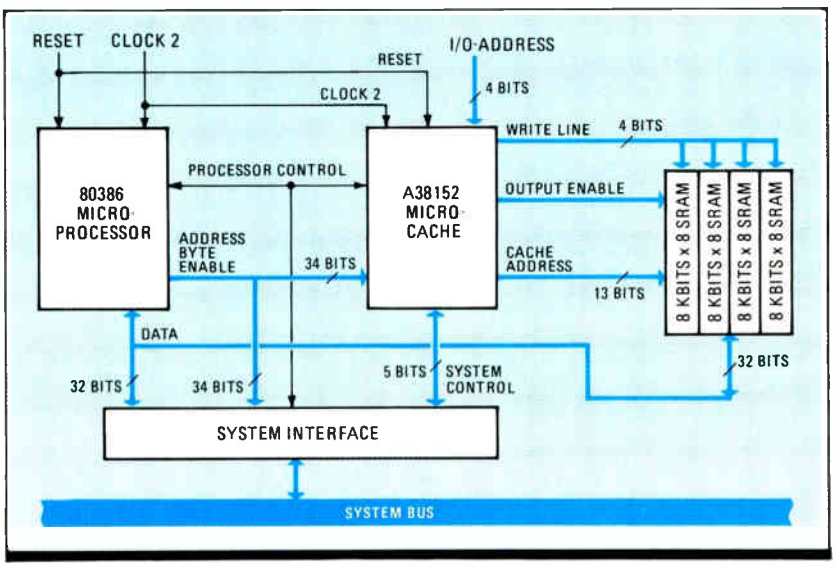
An Australian company uses a four-way set-associative cache-memory-matching algorithm to boost by 50% the speed of a 32-bit 80386 microprocessor

by Bernard C. Cole

A new cache memory controller chip can boost the speed of 32-bit designs built around Intel Corp.'s 80386 microprocessor by as much as 50%. The general-purpose device accomplishes this mainly by employing an algorithm that pushes the hit rate to as high as 99%, thus reducing the number of times that a main memory must be accessed and eliminating deliberately built-in wait states.

Tackling the 32-bit performance challenge is an Australian company, Austek Microsystems Ltd. of Adelaide. Its A38152 microcache controller, in combination with just four 8-Kbit-by-8-bit static RAMs (see fig. 1), makes up a complete 32-Kbit, four-way set-associative cache with zero-wait-state operation and high hit rates. It does this with a four-way set-associative cache-memory-matching algorithm, on-chip tag random-access memory, a modified write-through architecture with bus-watching capability, hardware and software support to improve cache coherency, and a cache-replacement algorithm that relies on random replacement rather than the more common least-recently-used method.

Fabricated in 1.5-μm CMOS, the 130,000-transistor device allows designers to build 32-bit 80386-based systems using low-cost 120-ns dynamic RAMs with zero wait states, versus the three to four wait states required with existing direct-mapped techniques, says Roger Fisher, Austek's director of marketing at the company's U. S. facility in Cupertino, Calif. (see p. 77). Moreover, while current implementations of such a system would require at least 32 Kbytes of cache data memory, four 64-word-by-52-bit cache tag SRAMs, and three or four medium-scale integrated circuits or programmable logic circuits, the A38152 can provide an equivalent system with only 32 Kbytes of data-cache RAM. Engineering samples of 16- and 20-MHz versions are available now.



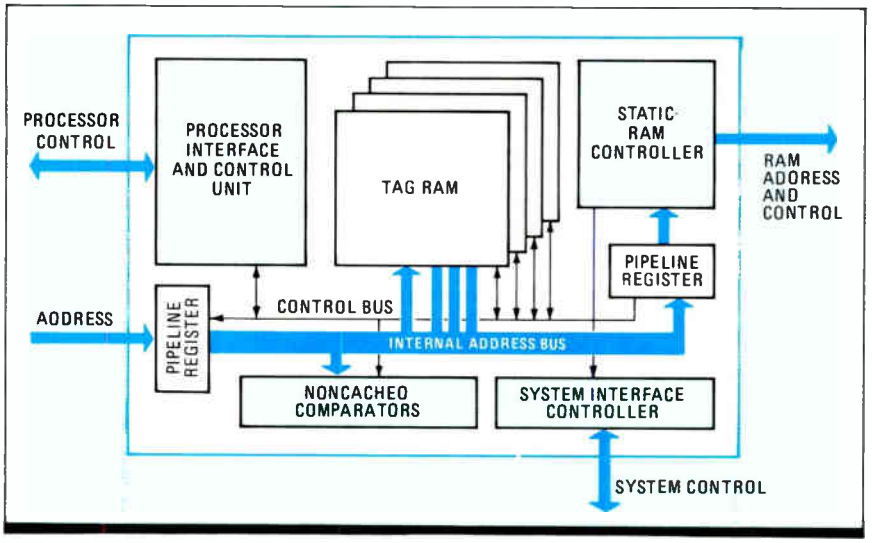
1. LOW CHIP COUNT. Austek's A38152 four-way set-associative cache controller needs only the addition of 32 Kbytes of external SRAM to achieve hit rates as high as 99%.

The most common form of cache RAM in 32-bit microprocessor systems is the direct-mapped approach, in which each memory address maps into the cache at a single memory location. Direct mapping is popular, says Glenn Farrall, the A38152 senior design engineer, because it is easy to implement, requiring only a few external field-programmable logic devices in addition to the cache tag and cache data RAMs. But, he says, "The disadvantages of direct mapping are its inefficiency and the effect on performance when a match, or hit, does not occur."

The A38152's four-way set-associative design provides four locations to which a

memory address can be mapped. A processor such as the 80386 typically generates memory requests from three sources: one for an instruction segment, another to access a data segment, and a third to perform stack operations to access local variables or to save and restore procedure context. "In a direct-mapped cache, these streams typically compete for many locations in the cache," Farrall says. "In a four-way set-associative cache, it is more likely that each stream can establish sufficent working area without conflicting with the others."

To implement the four-way scheme, the 8-by-8-mm device is partitioned into five major functional blocks: the processor interface and control unit, noncached comparators, 64 by 52 bits of cache tag SRAM, the SRAM controller, and the system interface controller (see fig. 2).



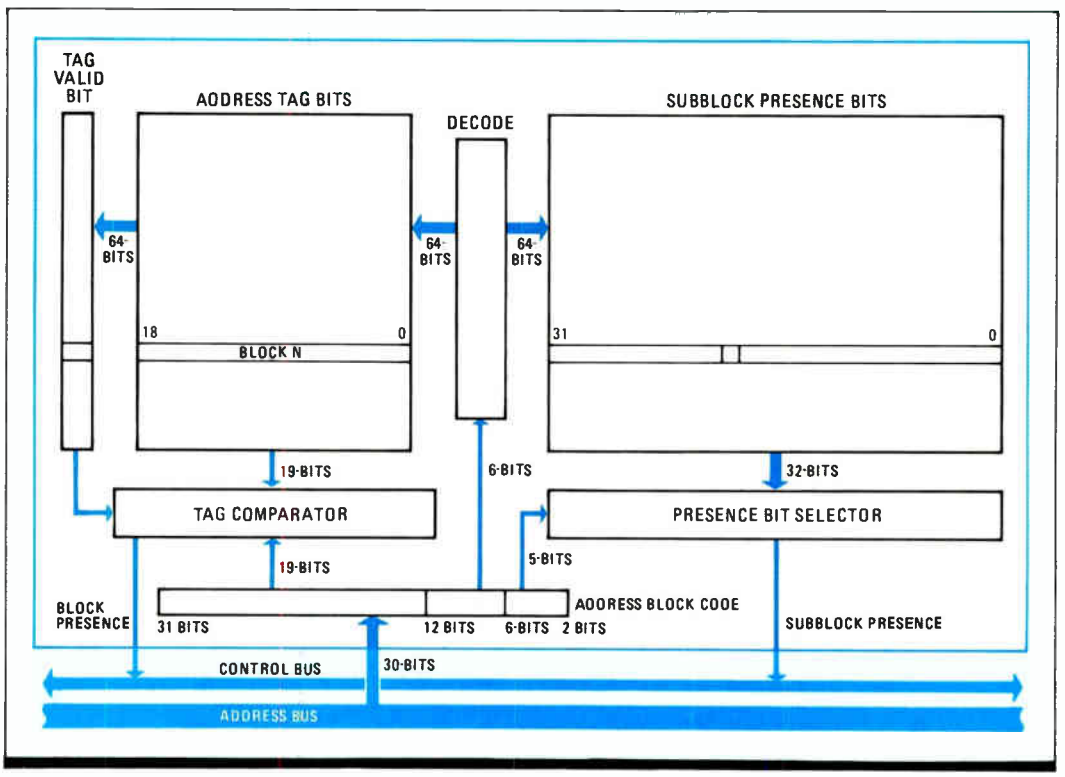
2. INTEGRATED CACHE. Austek's cache control includes 64 by 52 bits of cache tag SRAM, a data cache SRAM controller, comparators, and interface logic.

The control unit tracks the processor's operation and initiates a tag RAM access whenever the processor begins a memory cycle. It controls the operation of the two internal pipeline registers to deal with the 80386's pipelined memory cycles. It determines whether a cache hit or miss has occurred by examining the outputs of the four tag RAMs, and it initiates a system-bus access to fetch data from main memory on a cache miss.

Two high-speed comparators monitor the internal address bus to indicate when an access is to a noncached region of the address space. This information is used by the control unit to determine whether or not to cache data.

There are four tag RAMs on the chip to implement the four-way cache. Each tag RAM (see fig. 3) contains 64 entries, each consisting of a valid bit, address tag bits, and sub-block presence bits. High-speed comparators within each tag RAM indicate whether the address on the internal address bus matches the addressed entry in the tag RAM.

When the 80386 initiates a bus cycle, the control unit latches the address into the first pipeline register. At the same time, the noncache comparators check to see if the access can be cached or not. If the access is to a cachable region of memory, the tag RAMs are accessed to determine if a hit or miss has occurred. By the end of the first clock cycle, the tag RAMs indicate if there was a cache hit in one of the tag RAMs. Before the second cycle begins, the address of the current bus cycle is latched into the second pipeline register, allowing the SRAM controller to complete the bus cycle using the correct address—immediately in the case of a cache hit, or several cycles later



3. CACHE TAG. Cache tag SRAM on the A38152 is separated into two blocks: a 64-by-18-bit address-tag array and a 64-by-34-bit sub-block presence-bit array.

in the event of a miss. Then the first pipeline register allows flow-through of the next pipelined address onto the internal address bus.

If the 80386 access is a write cycle, the system interface controller is enabled during the first clock cycle of the bus cycle. This allows processor write cycles to run with no wait states when there is a write buffer in the system interface. The write buffer is used in write-through caches to avoid holding up the processor for the entire main-memory write cycle. In the event of a cache hit, the SRAM controller is enabled and the external SRAMs are cycled, and the processor continues with no wait states. In the event of a read miss, the system interface controller is enabled, and in the second clock cycle the system interface is requested to fetch the desired data. The result is one clock cycle of latency for a read miss.

The A38152 carries hardware and software to support cache coherency—the need to consistently supply the processor an up-to-date copy of data. The hardware support is special bus-watching logic that checks the contents of the tags in the tag RAMs and invalidates the data if necessary. Software logic allows the designer to designate regions of the address space as noncachable, or to invalidate either a 4-Kbyte page of the address space or the entire cache contents.

For the cache block—the amount of information transferred between main memory and the cache—Austek uses a 128-byte block, broken up into 32 four-byte sub-blocks. Typically, caches with large blocks require less storage and logic for management purposes, but they increase the latency time of the bus in responding to high-priority requests, since the entire block may have to be transmitted before the bus can be handed back to the CPU for other operations. "If the block size is larger than the bus width, multiple transfers are required, further slowing down the system," Farrall adds. Small block sizes are less likely to contain unneeded information, but they increase the overhead logic required to manage transfers, thus increasing silicon area.

Austek's approach offsets the disadvantages of using large blocks. "To keep the number of transfers to a minimum and to move only the necessary information, the cache algorithm searches through the block until it finds the information it needs," he says. "Then, rather than transferring the whole block, the A38152 transfers only those sub-blocks up to and including the one in which the needed data is located."

To offset the extra silicon required for the four-way scheme, the designers chose a random-replacement algorithm rather than the more common least-recently-used technique, which is complicated and requires a lot of silicon. "The random-replacement approach, in which the entry to be replaced is chosen at random, requires virtually no overhead circuitry," says Farrall. "Our simulations show that at the four-set level there is virtually no difference in performance." □

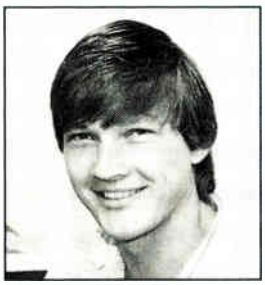
SOLVING A UNIVERSAL PROBLEM IN 32-BIT MICROPROCESSOR-BASED DESIGNS

For 26-year-old Glenn Farrall, senior design engineer at Austek Microsystems Ltd. in Adelaide, Australia, the A38152 microcache controller is the culmination of an effort that has occupied much of his adult life.

After graduating from Australia's University of Melbourne in 1981, Farrall went on to do graduate work at the school, writing a master's thesis on designing cache-memory-based computing systems. He then spent a brief stint as the Australian multiproject chip coordinator for the Commonwealth Scientific/Industrial Research Organization. In 1984, Farrall joined Austek, where he went to work developing programs for the company's proprietary in-house computer-aided design system.

He soon became involved in developing customized cache memory systems for several of the company's clients for custom and semicustom circuits. "By mid-1985 it became clear from the kinds of requests we were getting for custom circuits that the problem of cache control in 32-bit microprocessor-based designs was a universal one, and one that was amenable to a standard, rather than custom, solution," he says.

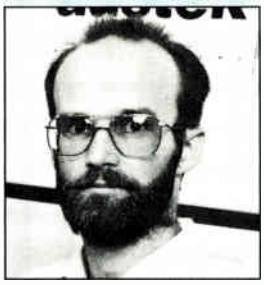
Over the past year and a half, as the chief architect on the chip, Farrall has worked to bring the cache controller to market as quickly as possible. He was part of an in-house development team that included 26-year-old Nick Foskett, who was responsible for functional simulation and logic design; 47-year-old Rob Potter, manager for Austek's microprocessor support products; and 32-year-old Geoff Smith, manager of MOS design engineering.



GLENN FARRALL

ROB POTTER

NICK FOSKETT



GEOFF SMITH

Farrall says it became clear to all of them that the design of a cache controller is in many respects even more complex than that of a microprocessor, and that it involves a great many tradeoffs. Also, the 32-bit market is still in a state of flux, with many architectural approaches being tried, from complex-instruction-set computers to the more recent reduced-instruction-set machines.

"We think that we have come up with the best solution possible," Farrall says. "But so have a number of other manufacturers. So it is up to the users out there to make the final choice. "

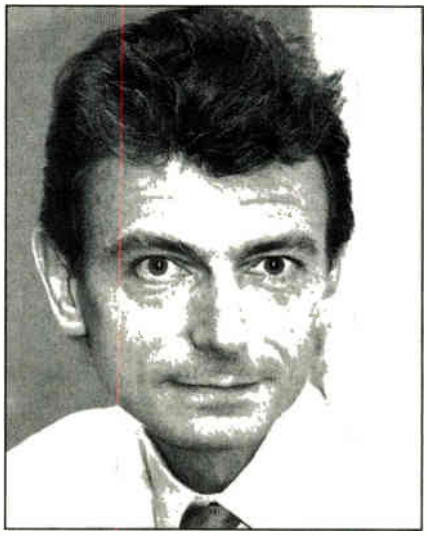
HOW AUSTEK WILL CACHE A RISING STAR

Australia isn't exactly known as a hotbed of leading-edge VLSI design. But it turns out that the country is just that, at least in digital signal processors, thanks to the government's funding a substantial amount of important work over the past decade. Now the design expertise developed from that effort is moving into U. S. markets. Austek Microsystems Ltd., an Australian custom integrated-circuit maker that cut its teeth on DSP chips, plans to hitch a ride with Intel Corp. to penetrate U. S. microprocessor markets, pinning its hopes for healthy growth to the expected bonanza in systems based on the Intel 80386.

Adelaide-based Austek (not to be confused with the Austec International Ltd. of Melbourne, whose subsidiary, Austec Inc., is in San Jose, Calif.) is part of the new generation of niche-oriented companies that provide custom VLSI solutions for computer designers. The three-year-old company's founder, J. Craig Mudge, studied with Carver Mead at the California Institute of Technology and is building a Mead-style company that specializes in design and leaves the production to silicon foundries. Lynn Conway, coauthor with Mead of the basic VLSI design text, *Introduction to VLSI Systems*, sits on Austek's corporate technology committee.

Though privately held and still small—it has 33 employees at its Adelaide headquarters—Austek has already developed a series of high-performance DSP chips to meet Australian government requirements. Examples include an autocorrelator for processing radiotelescope data, a speech-recognition chip, and a surveillance preprocessor for analysis of repetitive measurements. In the works is a high-performance fast-Fourier-transform chip suitable for use in parallel for radar and high-speed communications.

But with the introduction of a new cache controller (see p. 74), Austek is looking to accelerate its growth path. The cache controller is the first of a series of what Austek refers to as "application processors for high-performance 32-bit microprocessor systems"—in other words, peripheral chips. The company is targeting the market for systems based on the Intel 386, despite the fact that Intel entered the marketplace late, because it believes the enormous installed base of IBM Personal Computers will cause the 386 to skyrocket.



FISHER: His U. S. operation will reflect Austek Microsystems' niche-oriented strategy.

Dataquest Inc.'s figures show shipments of all 32-bit microprocessors rising from just under half a million units last year to 1.98 million units in 1987, 3.95 million next year, and 11.65 million units in 1990. In 1987 the 386 may account for 25% of all 32-bit shipments, says Roger Fisher, director of U. S. marketing for Austek in Cupertino, Calif.

Cache architecture is an Austek speciality, says Fisher, because many of its engineers have experience in minicomputers. Mudge, for example, who serves as Austek's chief scientist, founded the VLSI development group at Digital Equipment Corp. and was the designer of the DEC MicroVAX.

Austek will also develop floating-point processors for 386 systems, Fisher says. And it plans to design support chips for Motorola's 68020 and 68030 and for the National 32032 families.

The company has developed its own sophisticated computer-aided engineering tools for the MicroVAX. The tools link high-level functional simulation with low-level gate simulation so that the designer can compare outputs and be sure they are the same.

The tools also allow simulations to be exercised with applications software. The result is very fast turnaround; Austek says that making the cache controller took only 11 months from concept to silicon.

Fisher's U. S. operation will reflect the niche-oriented strategy of close connection with relatively few customers, rather than broad-based sales. "Most of our activity will be direct contact with a limited base of perhaps 100 customers," Fisher says. "They will be medium- to large-volume sales, of 5,000 to 10,000 units a year."

The cache controller may be an exception to that strategy, since it could find use in high-volume PC applications. "We estimate that with the 20-MHz 386, 50% to 75% of all PCs will use cache," Fisher says. "When the 25-MHz version is available, 100% will have cache." Fisher comes to Austek from Visic Inc., San Jose, Calif., a specialty-memory firm, where he was director of marketing. Before that, he spent 16 years at Texas Instruments.

Meanwhile, Austek will continue to pursue its DSP work. Mudge returned to his native country in 1981 at the request of the Australian government to set up the VLSI program of the Commonwealth Scientific and Industrial Research Organization.

Austek's Australian operations will focus on complex DSP chips. "Australia has a lot of strength in DSP," says Fisher. "Government researchers have done original work in image processing and satellite communications. What they have not done so far is to commercialize it." That will be Austek's job. *–Clifford Barney*

ADVANCED CACHE CHIPS MAKE THE 32-BIT MICROPROCESSORS FLY

Designers are bringing mainframe memory techniques to microprocessor systems

by Bernard C. Cole

Designers working with the powerful new general-purpose 32-bit microprocessors are finding that coming up with a high-performance system takes more than just a powerful central processor. As they gain experience with 32-bit chips, designers find they must adopt many of the architectural refinements associated with high-performance superminicomputers and mainframes in order to get full performance out of these tiny computing engines. In particular, they are moving to a hierarchical memory scheme in which high-speed cache, or buffer memory, is placed between the CPU and main memory to increase a system's throughput.

As better designs whittle away at the miss rate for accessed data—the percentage of times main memory must be read because the data required is not in the cache—they reduce the amount of time the CPUs must spend in deliberately programmed wait states until memory accesses are completed. Toward this end, a number of semiconductor companies are coming up with chips for cache-based microprocessor systems: special memory parts for building cache buffers and highly integrated cache controller chips, such as the A38152 from Australia's Austek Microsystems Ltd. (see p. 74).

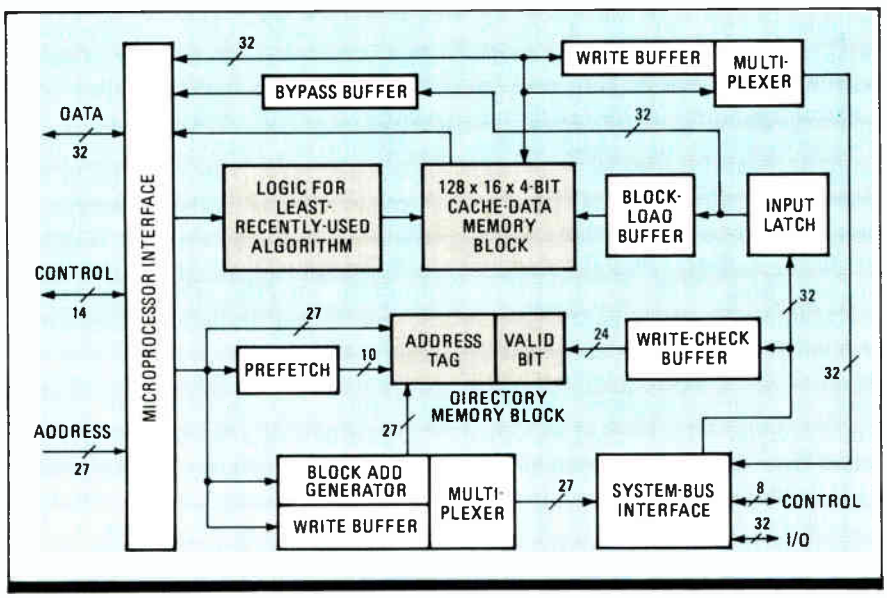
Cache is now seen as a way to take full advantage of the new 32-bit microprocessors, especially in multiple-microprocessor configurations. Without cache, designers must use either commercially available 100- to 120-ns dynamic random-access memories and introduce wait states, or shift to the use of 50- to 60-ns static RAMs, which are much more expensive and also reduce the system's circuit density.

Cache architectures offer a way out of this dilemma by storing the information most frequently accessed from the main memory. In such schemes, the buffer between the CPU and the main memory usually consists of the data cache, for storage of the data copied from main memory, and the cache tag memory, which is used to store the memory address locations.

When the CPU requests data from memory, the cache controller checks to see whether the address the CPU is issuing matches an address found in the cache tag RAM. If it does, the data in the cache data RAM corresponding to the matching cache tag address is sent to the CPU. Thus, when the CPU tries to read data from the main memory, the high-speed cache will respond first if it has a copy of the requested data. Otherwise, a normal main-memory cycle takes place. In typical systems, data will be supplied by the cache memory more than 90% of the time—that is, the system will have a better than 90% hit rate.

Although the operation of a typical cache is relatively simple in concept, implementation is a complex process involving such factors as the type of memory mapping involved, the cache size, the size of transferred blocks of data, the data-replacement algorithm, and write-request handling, says David Wyland, product-definition and application-engineering manager at Integrated Device Technology Inc., Santa Clara, Calif.

"There are as many opinions on how to design a cache memory as there are systems designers" at the microprocessor level, says Tom Goodman, director of application engineering at Vitelic Corp., San Jose, Calif. The technical issues involved in cache memory design are



1. CONTROLLER WITH CACHE. Due later this year, NEC Corp.'s μPD43608R is a four-way set-associative cache controller that integrates its own data and address-tag memory blocks.

relatively straightforward. But the environment in which the concepts were initially developed—mainframes and minicomputers—is considerably different from that in which designers using microprocessors find themselves. "A technique that might have seemed practical at the mainframe level might have to be ruled out at the microprocessor level for reasons of economics, component count, interconnect delay, or the ease of implementation," says Goodman.

Sensing an opportunity to get into a market niche for special-application memory—a niche that is still rather small but could follow in the footsteps of such previous niche products as video DRAMs and dual-port SRAMs—semiconductor companies have swept into the marketplace. "A year or so ago, cache memories were a relatively small share of the total market, dominated by bipolar solutions and aimed at mainframes and minis," says Victor DeDios, semiconductor industry analyst at Dataquest Inc., of San Jose. "In that short time, things have changed drastically with the entry of a wide variety of CMOS devices and a remarkable diversity of architectures."

Only slightly less remarkable is the speed at which the market has evolved from relatively simple designs to highly integrated solutions. For even as companies such as Advanced Micro Devices, Integrated Device Technology, Motorola, Texas Instruments, and Thomson Components/Mostek [*Electronics*, Feb. 5, 1987, p. 65] move into production with a variety of cache data and cache tag SRAMs, more highly integrated solutions—at the VLSI level—are beginning to emerge.

Whereas present circuits are combined with external logic to implement what are called direct-mapped replacement algorithms—in which each memory address maps into the cache at one memory location—the newer integrated solutions use more advanced set-associative schemes, in which each address can be mapped into many different locations. And whereas the first allows hit rates from 65% to 90%, depending on the amount of cache memory used and other factors, the advanced solutions allow hit rates in excess of 90%, using one half to one fourth the amount of memory space.

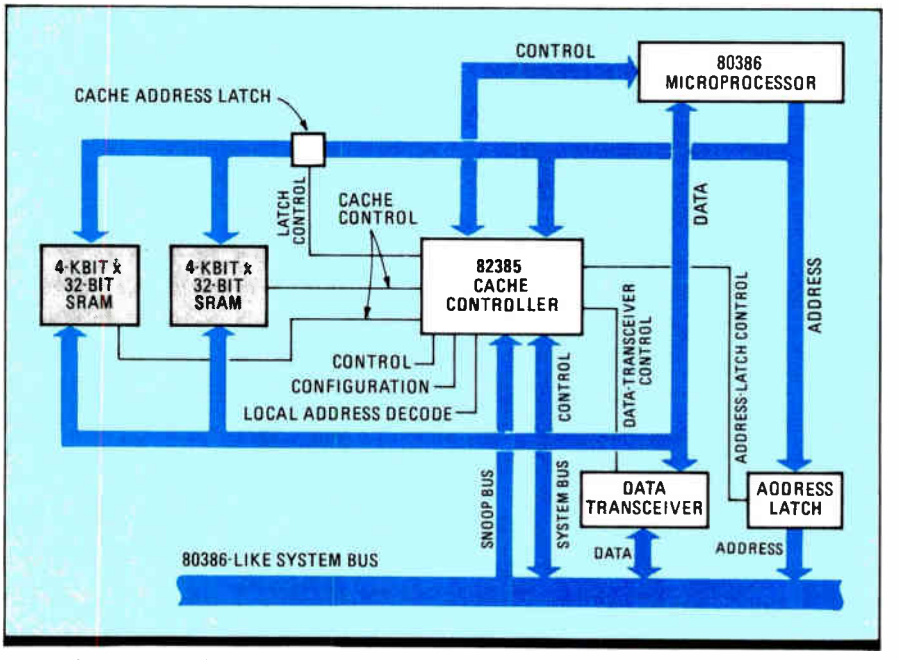
One of the first advanced designs to emerge is the A38152 cache controller from Austek Microsystems, of Adelaide, Australia, designed for use with Intel Corp.'s 80386 microprocessor. It implements a four-way set-associative algorithm and requires only 32 Kbits of external RAM to achieve a hit rate in excess of 95%. Engineering samples are available now, and the company plans to be in volume production by late August.

On its heels is another four-way set-associative controller, this one from NEC Electronics Inc. of Mountain View, Calif. Designated the μPD43608R, it incorporates not only the controller and cache tag RAM on the same die, but 8 Kbytes of cache data RAM as well (see fig. 1). The chip is designed to deliver a hit rate of up to 95% when used alone, but higher ratios can be obtained by linking up to four chips in parallel. Unlike the Austek circuit, the NEC cache controller is designed with a general-purpose microprocessor interface capable of working with either 16- or 32-bit buses. NEC intends to put the chip into production during the third quarter of this year.

Scheduled to begin production sometime during the second half of the year is a more conservative two-way set-associative cache controller for the 80386 from Intel itself. Designated the 82385, it requires 8 Kbits by 32 bits of external SRAM, two address latches, and a data-receiver circuit for bus separation (see fig. 2). It can also be used in direct-mapped cache architectures.

Also planning to jump into the fray is Inmos Corp. of Colorado Springs, Colo., with a 386-specific four-way set-associative cache controller with an 8-bit-wide cache tag function on board. Introduction is scheduled for early 1988. Inmos is also working on a cache data RAM that works with the controller, to be followed by a second-generation controller incorporating its own cache data RAM.

Other companies that are reported to be planning entry into the cache controller market include Advanced Micro Devices, Cypress Semiconductor, Chips and Technologies, and Monolithic Memories. □



2. 386 COMPANION. Intel's 82385 cache controller will work with the 80386 microprocessor in either a direct-mapped or the two-way set-associative cache configuration shown here.

UPDATE: A FAST START FOR THINKING MACHINES


65,000 PARALLEL PROCESSORS TACKLE THE BIGGEST DATA JOBS

A year ago, Thinking Machines Inc. ushered in a new type of computing with an unconventional machine [*Electronics*, June 23, 1986, p. 45]. The new style of data-level parallel computing is the forte of the 65,536-processor CM-1 Connection Machine. Now, in less time than the company had originally expected to take to introduce the speedy CM-1, it is offering its second major product, the CM-2, which is equipped with floating-point processors designed to blast through numerical calculations at upwards of 2.5 billion floating-point operations per second.

The CM-1 matched the fastest supercomputers on problems that suit the data-parallel style, such as signal processing, machine vision, numerical algorithm design, and fluid dynamics. The CM-1 with 32 Mbytes of main memory can perform 1 billion instructions/s in general computing applications and up to 7 bips for specialized tasks.

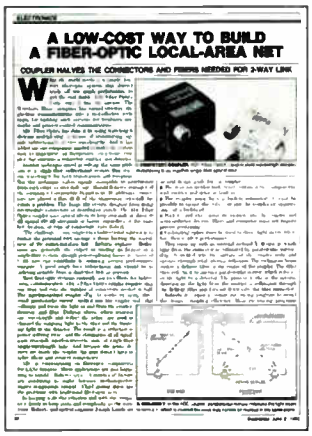
The Cambridge, Mass., company has sold at least 16 CM-1s in the first year, some of which have yet to be installed. "When we founded Thinking Machines in June 1983, I said it would take five years before we would announce out first product," says Sheryl Handler, president. "Now we've been able to introduce two new machines in the same amount of time."

The major improvement in the CM-2 over the CM-1 is the speed with which it does numerical calculations. Floating-point-accelerator processors were added to the machine to boost floating-point performance to 2.5 gigaflops and more.

There are two versions of the floating-point accelerator: double-precision and single-precision. Each accelerator consists of a custom floating-point interface chip and a floating-point execution chip. One accelerator is used with every 32 data processors; each data-processing chip contains 16 data processors. A fully configured CM-2 has 4,096 data-processing chips, 2,048 pairs of floating-point chips, and 512 Mbytes of main memory.

The double-precision accelerator pushes the Connection Machine's performance to 2.5 gigaflops when multiplying two 4,096-by-4,096 matrices together; a single-precision accelerator ups the speed to 3.5 gigaflops on the same multiplication. The blinding speed of the machine winds right off the charts on dot-product computations, running at 5 to 10 gigaflops, respectively, for double and single precision. *–Tom Manuel*

UPDATE: A ROCKY ROAD FOR ADC'S FIBER-OPTIC COUPLER


A LOW-COST WAY TO BUILD A FIBER-OPTIC LOCAL-AREA NET

COUPLER HALVES THE CONNECTORS AND FIBERS NEEDED FOR 2-WAY LINK

The plans that ADC Fiber Optics had for its single-fiber fiber-optic coupler have not worked out the way the company hoped when it introduced the product a year ago [*Electronics*, June 2, 1986, p. 36]. Sales have been sluggish, and efforts to boost them are now being affected by changes at ADC. Formerly a subsidiary of ADC Telecommunications Inc. of Minneapolis, ADC Fiber Optics was folded back into the parent company in April and was promptly moved from its offices in Westboro, Mass., to Minneapolis.

ADC still thinks the Connectorized Active Full-duplex, or CAF, coupler has good potential. It comes with a built-in emitter and detector and uses a process called wavelength-division multiplexing to transmit light bidirectionally on two different wavelengths. Its single-fiber design reduces the cost of fiber and the number of couplers required when building a fiber-optic local-area network.

The weak demand for the coupler has been due in part to a sluggish market in local-area fiber optics. "The long-distance market took off faster than anyone expected, but where speed and high capacity aren't as important, cost has been a factor," says Chip Kemppainen, an ADC product manager.

ADC also found that many potential customers were put off because they had to design their own driver and receiver circuitry to link the coupler with the digital electronics necessary to create a complete data link. "We had a lot of input from electrical engineers telling us they didn't want to do it," says Harold Roberts, chief designer of the coupler.

ADC is now packaging the coupler as part of a transceiver evaluation kit consisting of two couplers mounted on a board with driver and receiver circuitry and an edge connector. "It took us several years to design the coupler," Kemppainen says. "Now it's taking our customers time to develop products to use it." *–Paul Angiolillo*

DESPITE IBM'S PS/2, THE OUTLOOK IS BRIGHT FOR CLONE-CHIP MAKERS

Vendors work hard on chips for PS/2 clones; the PC-compatible market keeps on growing

by Bernard C. Cole

The band of chip vendors that have come up with the increasingly dense integrated circuits used to build personal computers compatible with IBM Corp.'s PC line have been the major factor in the huge success of clone-system builders. By providing higher-performance chip sets that dramatically cut the component count for such machines, these producers enabled systems houses to offer better performance at lower prices. But now that IBM has finally announced its Personal System/2 [*Electronics*, April 16, 1987, p. 46], some people believe the new line could be a double whammy for IC makers: functions in the PS/2 line will be very difficult to duplicate, and the new IBM models will kill the markets for the still-growing business for chips going into PC/XT and PC AT clones.

That isn't the case at all. The market for the older IBM PCs is not likely to slow down for the next year or two. And the same crowd of chip builders is hard at work reverse-engineering the IBM machines and gearing up to offer chips for the next generation of clones. The PS/2 machines do present some major challenges to them, however. An official at one chip maker calls the motherboard of IBM's 386-based Model 80 "supercomplicated." But none of the chip vendors in the clone-support business reveals the slightest doubt that they can do the job. ICs for PS/2-compatible systems are said to be on the way by the end of this year from at least two companies; one, Zymos Corp. of Sunnyvale, Calif., plans to announce its first part for 386-based systems at the end of June.

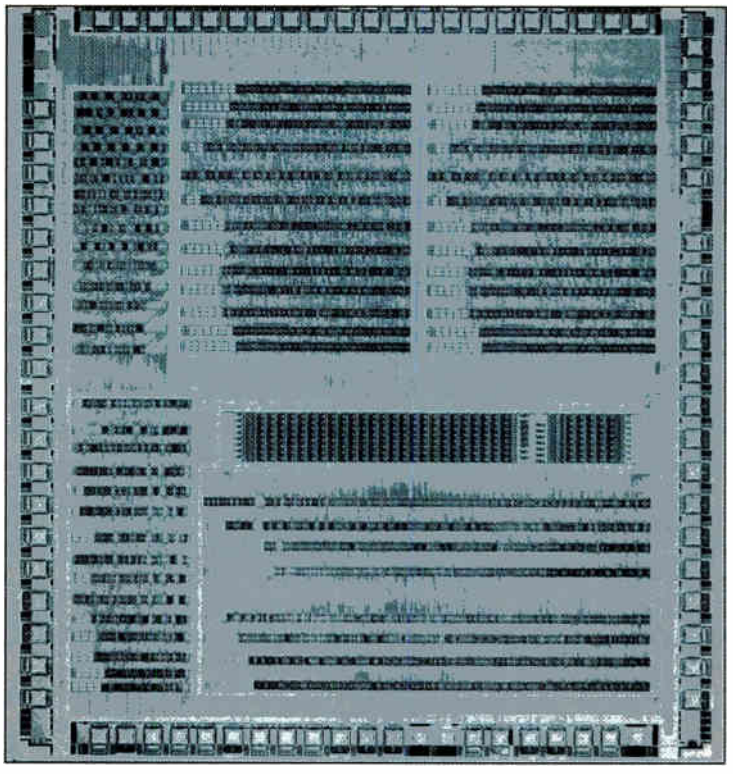
Little is known about how big the PS/2-compatible market will be, or how fast it will take off. Meanwhile, however, the market for chips that go into machines compatible with IBM's older PC/XT and PC AT models continues to boom. System sales are strong and growing, and other chip makers are trying to push their way into the business with the established companies—Zymos, Chips and Technologies, and Faraday Electronics. Among the new contenders are VLSI Technology Inc.'s Application Specific Logic Products Division in Phoenix, Ariz., and United Microelectronics Corp. of Hsinchu, Taiwan.

All of these companies are reported to be planning to build support chips for the 80386 microprocessor targeted at PS/2-compatible machines, chips that boost 386 performance and keep the system chip count to a minimum. In addition to its product introduction at the end of June, Zymos expects to unveil a part that supports a 386 running at 24 MHz this fall, and another extension to its line in the first half of 1988. Chips and Technologies Inc. of Milpitas, Calif., says it will introduce its first PS/2-compatible support chips later this year, as well.

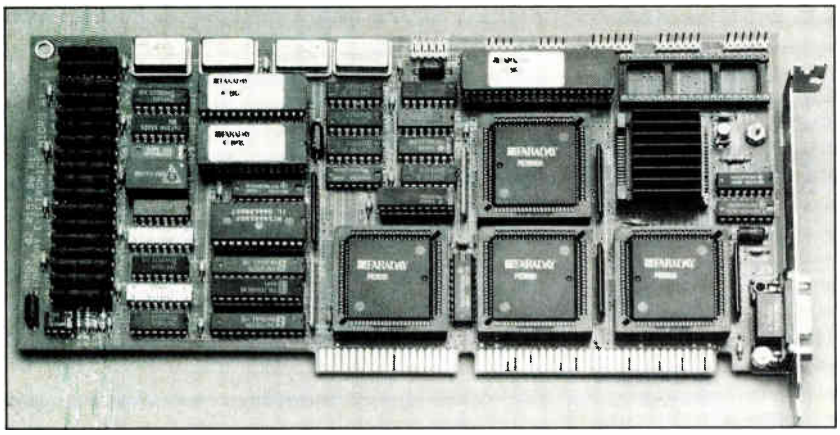
One major factor working in their favor is time. The operating-system software that will wring the full potential from the 386 processor in IBM's systems, Microsoft Inc.'s OS/2, will not be ready until the end of the year or the first quarter of 1988. This gives the clone makers and the chip makers supplying them several months to ready competition for IBM's Model 80.

"Until the introduction of the next generation of operating-system software for the PS/2, IBM is no threat competitively," says Alex Young, vice president of technology at Zymos. "Running under MS-DOS 3.3, clone makers using the chip sets becoming available will still be able to offer price/performance that IBM can't match."

It is only with the introduction of the OS/2



1. CONSOLIDATION. Poach 1 (shown) and Poach 2 from Zymos together replace about 40 chips in a computer compatible with the IBM PC AT.



2. MOTHERBOARD IN A SLOT. Four chips from Faraday Electronics fit a PC AT onto a small board.

operating system that the proprietary chips used in the high-end PS/2 series will become a factor, agrees Sinkandar Naqvi, product marketing manager at Chips and Technologies. "Overall, though, I don't see this as more than a temporary advantage for IBM," he adds.

Although they recognize the importance of the new PS/2 series, clone vendors think their XT- and AT-compatible offerings will give them solid ground to stand on for some time, and so do the chip makers who build support circuits.

PC-compatible makers last year shipped about 1 million XT and AT clones, says William Lempesis, research analyst at Dataquest Inc. in San Jose, Calif., and this year's projection is a total of 1.5 million, a 50% increase. In 1988, Dataquest estimates, the number of XT and AT clones shipped will jump by at least another 500,000 units, to nearly two million units.

With the help of chip vendors, PC clone makers have been able to cut costs while increasing performance as much as 25% over comparable IBM offerings

With the help of support-chip companies, clone makers have been able to push down system costs and increase performance as much as 25% over comparable IBM offerings. This has been achieved mainly by reducing the number of chips on the AT and XT motherboards, excluding the CPU and memory, from about 100 ICs and components to as few as three to four VLSI circuits.

Chips and Technologies has dominated the market since October 1985, accounting for 80% to 90% of the sales to PC clone makers. It has a five-component chip set consisting of two CMOS and three bipolar components that replace 63 of the 94 parts on the AT motherboard.

The two CMOS circuits provide CPU control and memory-select functions. The three bipolar circuits integrate most of the driver and buffer functions and replace a total of 30 circuits. More recently, the company has introduced a CMOS circuit, the 82C206, which integrates the functions of seven chips on the AT motherboard, including two DMA controllers, two interrupt controllers, a timer counter, a real-time clock, a memory mapper, and six miscellaneous glue-logic circuits.

Several competitors are now challenging the dominance of Chips and Technologies. The first was Zymos, which in October of last year introduced the first two devices in its Poach (PC on a chip) series. The two chips, also fabricated in CMOS on the company's standard-cell library, replaced about 40 AT motherboard circuits. Combined with two of its Poach 3 buffer chips, the parts count of the AT motherboard is cut by more than 75%, claims Zymos' Young. The company also last month introduced the Poach/XT88, aimed at 8088/86-based PC/XT systems, which replaces up to 12 chips.

Faraday Electronics Inc. also claims similar reductions in component count in AT-based systems. In April, the Sunnyvale, Calif., company unveiled a CMOS-based four-chip set: a CPU controller, a peripheral control-logic circuit, an address-buffer circuit, and a data-buffer circuit. The chips cut board area to less than 20 in.^{2}, versus 142 in.^{2} for a typical motherboard, says Ray Mazza, vice president of marketing at Faraday. Chip count is reduced from 95 to 19 and power requirements are slashed 50%, he says.

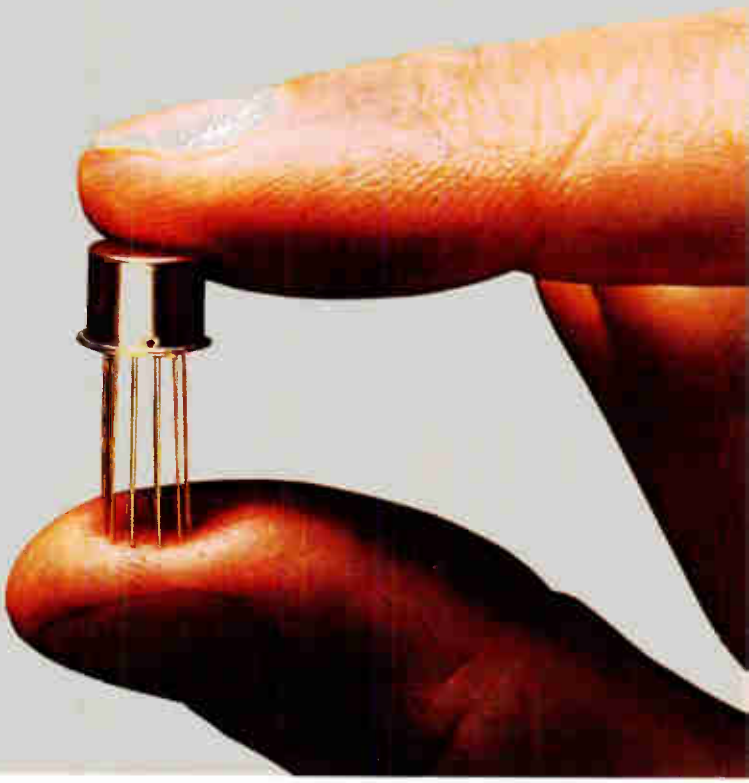
Another entry in the PC AT sweepstakes is Taiwan's United Microelectronics. Marketed through its U. S. headquarters at NMC Corp. in Santa Clara, its two chips aimed at AT applications eliminate 54 components from the motherboard. Another aimed at 8088/8086-based XT systems replaces 31 circuits.

VLSI Technology, the most recent entry, introduced last month a CMOS-based five-chip PC AT set, including a peripheral controller, system controller, memory controller, address buffer, and data buffer.

These newcomers are looking to differentiate themselves from their competitors in a number of ways. Faraday, for example, has chosen what it calls a "top-down" systems approach rather than a straightforward implementation of the PC AT and XT motherboard in VLSI. It has implemented in its chip set only functions essential to PC operation, eliminating much of the unused logic from the original motherboard design.

Zymos and VLSI Technology have chosen another route. They offer chip sets that are direct implementations of IBM motherboards. But as companies whose main business is standard-cell semicustom design, they offer customers the ability to reconfigure the basic design and generate chips that fit their requirements. □

New power TO-5 Relays handle loads up to 2 Amps



Now you can get the proven reliability of the TO-5 Relay for load levels above the traditional 1 amp rating. The new 212 Series TO-5 Relay was designed for switching applications where current surges at turn-on and turn-off run as high as 2 amps.

Teledyne Relays achieved this new higher power level for the TO-5 Relay by developing a proprietary contact system called TELESIUM™. This innovative system gives the 212 Series a resistive load rating up to 2 amperes for as many as 100,000 operations.

The 212 Series Relays are only .390 inches high and feature design and construction patterned after the classic TO-5 Relay, the relay which has become the industry benchmark for reliability. This similarity in fit and function makes the new 212 Series Relays pin-for-pin replacements for existing designs where excessive load conditions have been causing relay performance problems. The 212 Series Relays can also be screened to applicable parameters of MIL-R-39016, Level P, where required.

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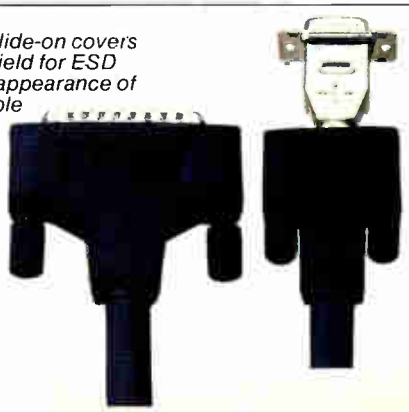

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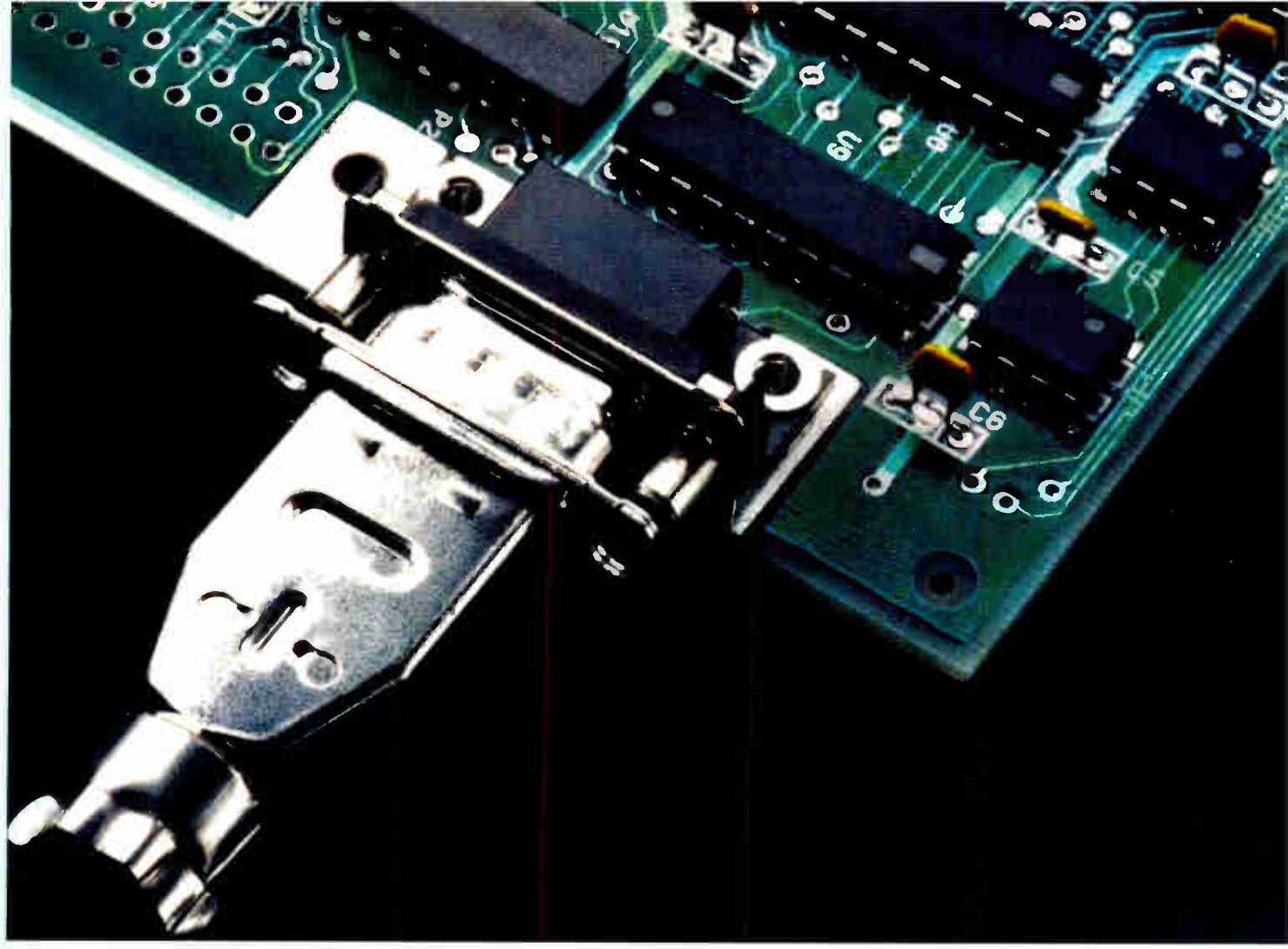

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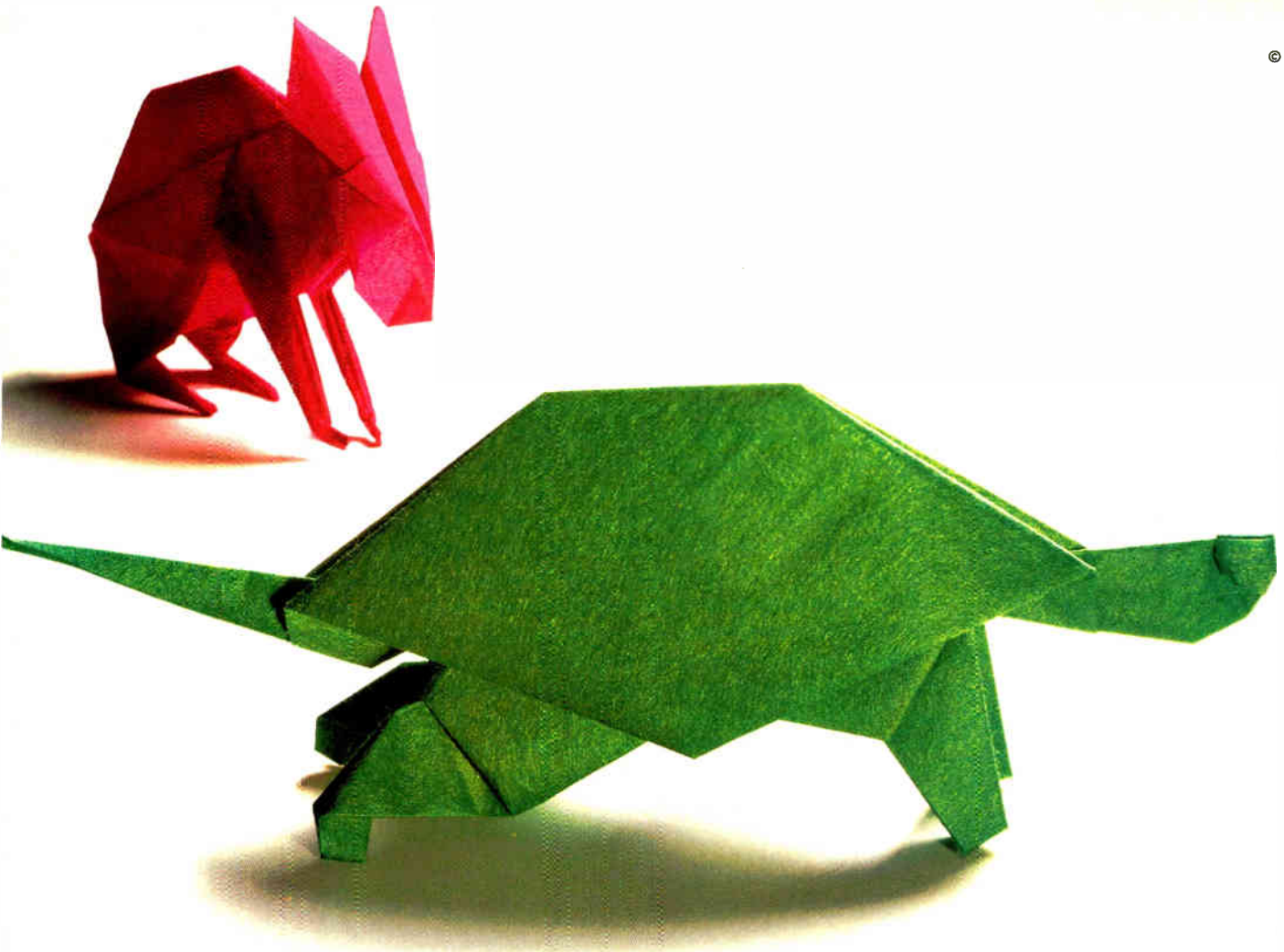

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ELIMINATING DEADLY STATIC IN IN-CIRCUIT IC TESTING

Manufacturing engineers traditionally have gone to great lengths to protect semiconductors against electrostatic discharge, which can blow out or burn out integrated circuits during printed-circuit-board assembly. They have taken painstaking precautions, using everything from grounded wrist straps and special antistatic tables and floors, to ionized air and static-free handling bags. But it turns out that the real hazards have been occurring after the boards leave the production line and move into the in-circuit testing that follows board assembly.

One company that has recognized this problem and decided to do something about it is Factron/Schlumberger, a large manufacturer of board test equipment, including in-circuit testers and fixtures. Spurred by complaints of static problems from customers involved with in-circuit testing of military boards, particularly in dry climates with low humidity such as the West and Southwest, the Latham, N. Y., company spent a year and a half developing the ATE industry's first special static-dissipative fixture, called a DISS-STAT fixture (see fig. 1).

SECRET TO SUCCESS

The secret to Factron's success is a proprietary coating that eliminates any harmful buildup of static by draining off the charge before it accumulates. The fixture also eliminates arcing from a direct discharge path to ground. The DISS-STAT fixture can be built from scratch, or the antistatic coating can be added to an existing device. The company has begun production of the fixture, and already has four of the units installed and undergoing evaluation at customers' facilities.

Static problems begin with in-circuit testing, which requires a special vacuum-actuated bed-of-nails fixture that moves a group of spring-loaded test pins on 50- to 100-mil centers against the bottom pads of the board under test. As the air is removed from the fixture during vacuum actuation, a large electrostatic charge is generated by triboelectric action—that is, by friction of the moving air against both the top plate of the fixture and the inside of the vacuum well. The same action occurs when the chamber of the fixture is refilled with air. If no means exists to bleed off the charge, a voltage level that is potentially damaging to semiconductors will develop and remain. Electrostatic voltages can reach as high as 500 V on the top plate and up to 5,000 V inside the vacuum well of the fixture.

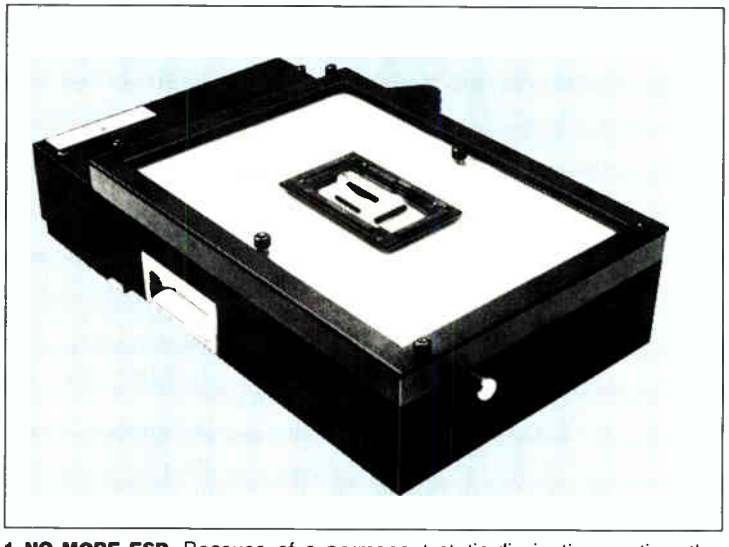
These voltages are well above the static susceptibility of all types of semiconductors. For example, the static susceptibility range of MOSFET chips is 100 to 200 V, and ECL bipolar devices can take up to 500 V. These electrostatic potentials can destroy chips on boards and can even blow out solid-state switches in the in-circuit tester interfaced to the bed-of-nails fixture.

The failure mechanism caused by the electrostatic voltage may be junction burnout in bipolar chips, dielectric breakdown (oxide punchthrough) in MOS and CMOS devices, or metalization burnout in any semiconductor type. In addition, there is the threat of electrostatic overstress, which can be caused by a charge that reaches only 25% of these values. This results in units that are apparently good and seem to have survived the static without damage, but which will eventually fail well before their specified mean time between failures. The new VLSI chips made with fine lines and even thinner oxide layers will further aggravate the danger of static.

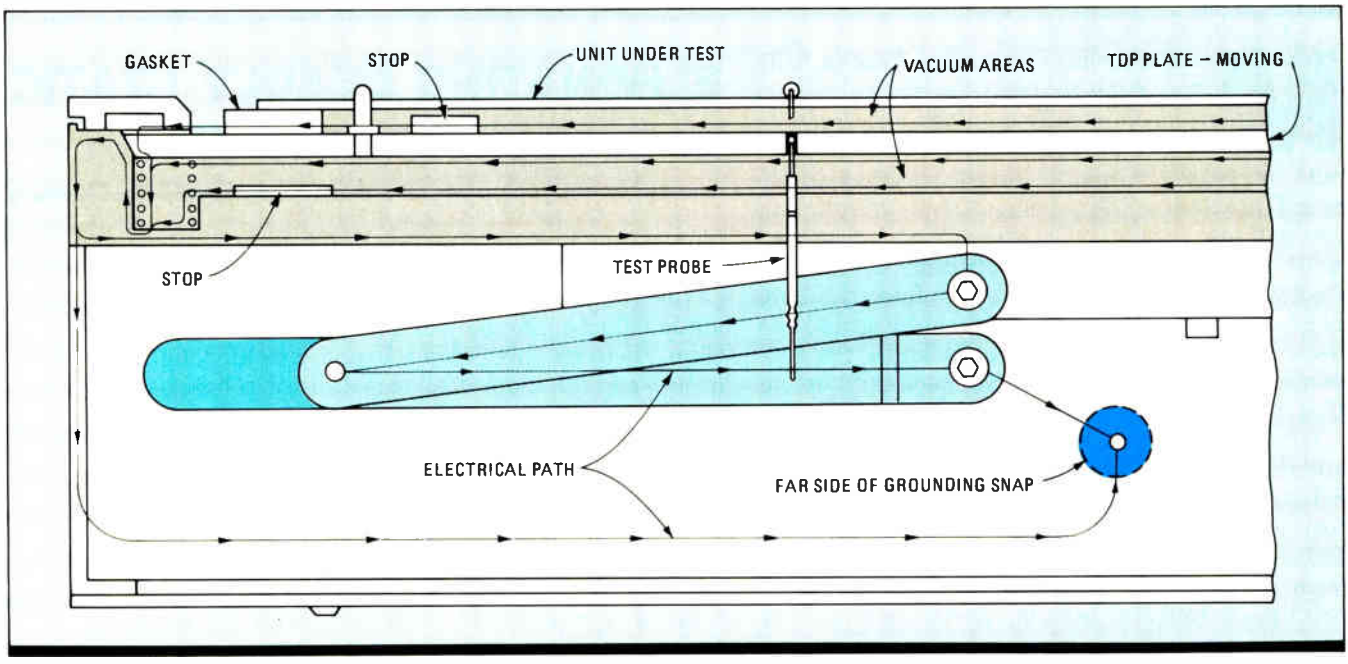
Early in 1985, Gary St. Onge, director of operations for Factron Interface Products, started hearing about static occurring in the bed-of-nails fixtures used by some of his customers. Tim Lanza, a staff engineer at Hughes Fullerton, for one, had become suspicious that some apparently random IC failures on boards that were processed through his in-circuit testers might be caused by static. Shortly thereafter, a government inspection team did find an excessive charge buildup on all the in-circuit test fixtures at this facility.

Hughes tried several solutions. First, the fixture was disassembled and sprayed with an antistatic spray. This procedure worked, but the spray had to be reapplied at one-week intervals, so another method was sought.

Next, streams of ionized air were blown



1. NO MORE ESD. Because of a permanent static-dissipative coating, the DISS-STAT fixture prevents potential IC damage.



2. CHARGE REMOVAL. The charge that is accumulated in the various static-dissipative-coated parts of Factron/Schlumberger's DISS-STAT fixture is bled off to ground.

across the fixtures, an improvement over the topical antistatic coating but still not completely satisfactory. In fact, under certain conditions, the ion blowers charged rather than protected the boards under test.

Factron became fully aware of fixture problems occurring during in-circuit testing in early 1986. In a technical paper, the company recommended the use of ionization blowers to prevent charge buildup on the fixtures. However, continued reports of fixtures taking on excessive electrostatic voltages despite the use of ionized air blowers led Factron's engineers to look for a material-oriented solution to electrostatic buildup.

Factron's aim was to make all relevant surfaces permanantly static dissipative rather than conductive. These surfaces not only included the exposed, external surface, but internal surfaces where airflow might induce a charge as well. In addition, all external surfaces likely to be encountered by a board under test fall in the static dissipative range, which mimimizes the possibility of a direct discharge between a charged object, such as the operator and the fixture.

The key element in the coating on Factron's DISS-STAT fixture is a special chemical process that molecularly bonds hydroscopic materials into the appropriate surfaces. The result is that all pertinent surfaces are permanently static dissipative. Even scratching the surfaces has no effect on their new properties.

After it is sprayed or dipped, the surface resistivity of the treated parts of the fixture is between one billion to 10 billion ohms/square. This figure falls within the EIA's specified static dissipative range of one million to one trillion square ohms. Less than 100,000 ohms/square is considered conductive by the EIA.

In the DISS-STAT fixture, the top plate that holds the board under test, the assembly that holds the spring-loaded test pins, the vacuum manifold, and the bottom frame of the fixture are all coated with the static-dissipative material. In a typical installation, any charge generated in the unit by airflow or brought to the unit by a statically charged operator or by a board that has picked up a charge in transit to the fixture is quickly dissipated through the special coating to a ground in the tester frame. Or it is dissipated to a snap-on ground point on the fixture frame, preventing any dangerous charge buildup on the unit under test (see fig. 2). Dissipating the charge rather than discharging it directly to ground prevents possible arcing to either a pc-board trace or between IC leads, either of which can cause destruction of ICs.

Factron currently has four of the new fixtures in the field for customer evaluation. One is with a large computer maker, which is considering replacing all its fixtures with the DISS-STAT to eliminate any possibility of static during in-circuit test. A DISS-STAT fixture can either be built from scratch, or an existing fixture can be modified so that it is static dissipative. The price of the new fixture is $300 more than that of an unmodified fixture.

The new coating is suitable for the most commonly used single-sided fixtures for in-circuit board testing, but the same antistatic coating is also applicable to double-sided in-circuit fixtures, sometimes called clamshell fixtures, for the testing of two-sided surface-mounted boards.

–Jerry Lyman

For more information, circle 483 on the reader service card.

A NEW WAY TO SPEED UP ARTIFICIAL-VISION SYSTEMS

Artificial-vision systems are increasingly being used in applications where human inspection is too slow or inaccurate, but until recently they could not process fast enough to be cost-effective for most applications. But now a new artificial-vision system by International Robomation Inc. called Supra (see fig. 1) may solve that problem for some of these tasks.

Supra is the Carlsbad, Calif., company's latest generation of artificial-vision systems and marks a radical departure from its predecessors. It achieves its significant increase in performance with what the company calls an iconic processor board, which uses several dedicated processors to perform with hardware a number of image-processing algorithms that previously were done much more slowly by software. One processor is a correlator that compares a learned image, or an image used for comparison that is already stored in the system, with one acquired from an object being scanned. This correlation in hardware rather than software boosts performance by a factor of 100.

A pixel statistical processor can create 16 windows for viewing an image for specific objects—pads on a printed-circuit board, for example. The previous system provided only one window. Supra also comes with two multifunction systolic-array processors: one is standard with the system and is a 10% improvement over the previous version; the second, an optional unit, improves performance fivefold.

Artificial vision is very compute-intensive. It uses a high-resolution RS-170 standard charge-injection-device video camera to scan an object—for example, printed-circuit-board components or chips on a wafer—looking for correct placement of components or reading the serial numbers of a component to trace it in a manufacturing process. The digitized image, with pixel resolutions from 64 by 64 to more than 1,024 by 1,024, is stored in a large buffer memory. Before being inspected, the acquired image may be enhanced by a variety of image-processing algorithms to remove background noise. Finally, the image is compared with a learned image.

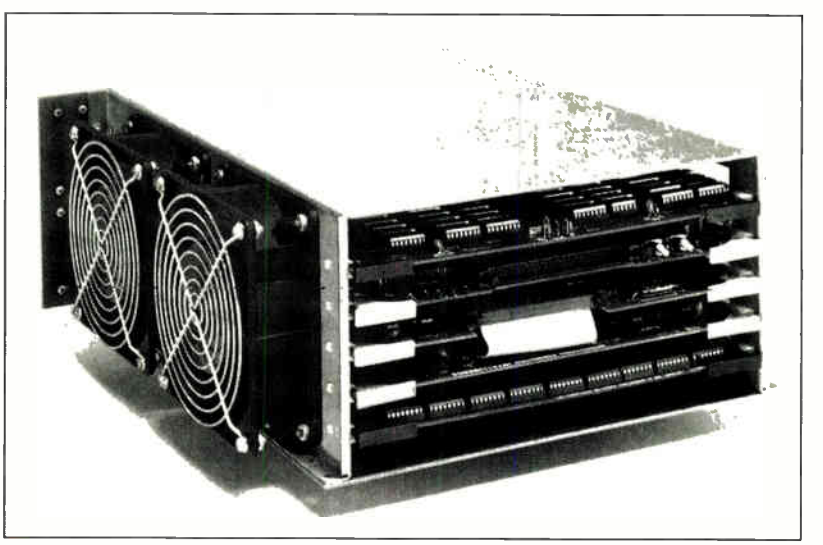
The key element in the Supra system is the iconic processor board, which contains the processors for performing hardware algorithms that were previously done in software. One new processor, the fast correlator, looks for an object and compares it with a learned object. It is unique because it provides size- and rotational-invariant optical character recognition—a character such as a "B" can be any size and can be rotated in any orientation without affecting the speed of the processor.

In wafer-probing applications, this capability would be used while the system scans a die, looking for a particular section of the die that it has learned. Prior to probing, the wafer can be positioned at the probe station and rotated two to five degrees off center. Being rotationally invariant means that the correlator can correlate and locate the desired section of the die to probe without requiring that the wafer be accurately placed under the camera.

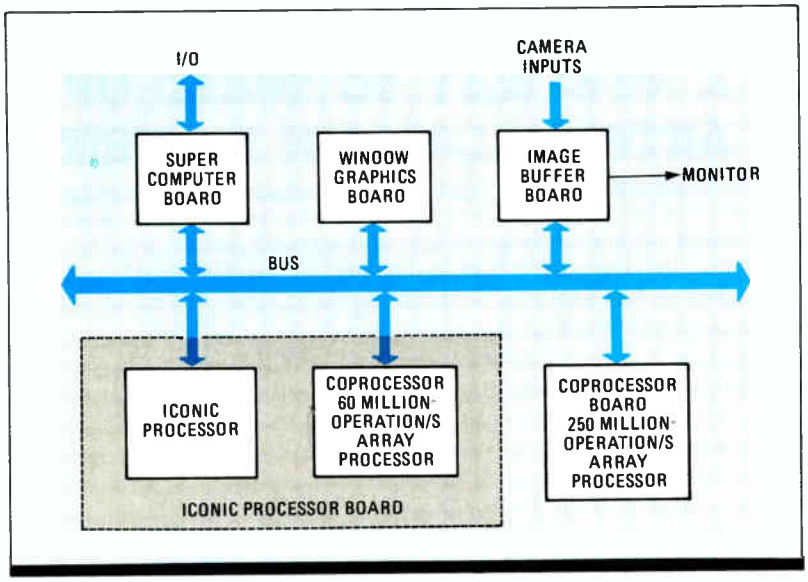
Implementing these critical algorithms with the high-speed hardware provides orders of magnitude more processing throughput than any other vision-inspection system currently available. All these critical functions entail pure mathematical processing of basic yet vigorous algorithms. For example, the fast gray-scale correlation hardware improves throughput from the standard 40 million operations/s to as many as 500 million operations/s in gray-scale correlations processing.

The fast hardware correlator on the iconic processor board accesses image data stored in the 1-Mbyte image-buffer memory. This memory holds the image detected by the camera or cameras and can accept up to four camera inputs, each into a separate memory frame. When making a comparison, the correlator holds the learned image in its own template buffer memory. In Supra, this data can be acquired from the computer-aided design system used to produce the printed-circuit board. It contains the outline and placement of every component, pad, and trace on the board.

Unique in the Supra implementaton is that both the template and acquired images are read in parallel and the comparison made as the images



1. IT'S SUPRA. Hardware in the Supra system performs image-processing algorithms many times faster than systems executing software algorithms.



2. HARDWARE EYES. On instruction from a 68020 computer, an iconic processor and two coprocessors execute image-processing algorithms.

are read. In previous generations of vision-inspection systems, the acquired image was read and the comparison made as the known good image was read from memory external to the correlator.

The 68020-based general-purpose computer consists of an MC68020 host with 1 Mbyte of on-board memory, a floating-point MC68881 coprocessor, and a VMEbus gateway. It directs the operations of the processors on the iconic processor board and the image-buffer memory (see fig. 2).

This computer contains the program that specializes the vision system for a specific application—inspecting circuit boards or reading package labels, for example. For each application, the computer would initiate different processing algorithms in the iconic processor board. For example, printed-circuit-board inspection requires very little image enhancement, but reading package labels requires a great deal of image enhancement.

The pixel statistical processor, a new piece of hardware on the Supra's iconic processor board, can concurrently process 16 windows, a considerable improvement over the previous generation of equipment's one window. This capability will be particularly useful in a printed-circuit-board application used by Chrysler Corp. The automobile manufacturer has an assembly line for producing VME printed-circuit boards with surface-mounted devices. Each device must be visually inspected to ensure that the leads are correctly placed on the pad and are not bent prior to soldering. The vision-inspection system has six seconds to inspect every component on each board.

The current system uses eight cameras, each driving eight different image-processing systems to strobe a 1-in.-wide section of the printed-circuit board into the image buffer every few tens of milliseconds as the board slowly moves in front of the cameras. Each system with its one window looks for pads inside the section of the board it has scanned.

Supra's architecture is open-ended, enabling clustering of several vision modules to simultaneously work on an inspection task. Thus, for the Chrysler applications, a cluster of four Supra subsystems, each with two cameras, could be used instead of the eight individual systems. Now, however, the cluster produces 64 windows (16 windows each) to look for pads instead of the eight windows of the company's first system.

Another addition to the Supra system that significantly boosts performance is two array processors: the CPB/60 at 60 million operations/s and an optional CPB/250 250-million-operation/s coprocessor. The CPB/60 is a high-speed multifunctional systolic-array processor on the iconic processor board used for performing other image-processing functions. The previous-generation system used coprocessors rated at 50 million operations/s. The CPB/250 coprocessor opens up new applications.

One application that will benefit from the increased processing power is vision systems that can read alphanumeric data, such as the part and serial numbers of components in a manufacturing process. The difficulty in building a system to read an eight-digit alphanumeric serial or part number is that the number of eight-digit permutations that must be maintained in memory is prohibitive.

An image-processing algorithm called blob labeling that runs on the coprocessors overcomes this problem. Blob labeling gets its name from the fact that the algorithm identifies a nebulously shaped object in an area being scanned. With blob labeling, the algorithm identifies eight blobs representing the eight digits. It then executes a second algorithm, called run-length encoding, which scans each blob and determines the outline of the image in the blob. The technique is analogous to the way a facsimile machine scans a letter.

When the alphanumeric digit in each blob has been determined, another algorithm called connectivity analysis can be run to put the letters and numbers together, and the result can be used by the Supra's 68020 computer to complete the inventory of a work-in-process task or perform some other task.

The company will offer turnkey systems that use Supra clusters and provide applications software. The systems start at $150,000, depending on the applications software, number of vision modules, development stations, and other vision equipment such as cameras and housings. IRI will also offer the vision modules as an original-equipment manufacturer's system starting at about $20,000 per module. *–Jonah McLeod*

For more information, circle 483 on the reader service card.

RCA AND ROCKWELL BUILD 'RAD-HARD' 1750A CHIP SET

Advances usually come more slowly in military technology than they do in the commercial world. Long lead times and special requirements for test and documentation restrain the rate of change for most military applications, yet no technology is as bad as radiation-hardened electronics. These chips control satellites and missiles, so there is no room for error. The slightest malfunction can have disastrous effects. So when a company sets out to build, for example, a space-borne computer, it doesn't seek out the newest technology, it looks for the most reliable.

A new rad-hard chip set implementing the 1750A military computer instruction set is a classic example. When Rockwell International Corp.'s Autonetics Strategic Systems Division in Anaheim, Calif., chose the GE/RCA Solid State Division in Somerville, N. J., as its partner in 1985, it based its decision not on what the division promised it could do in 1987, but on what it was then capable of doing. That meant a sacrifice in speed and chip density, says Bill Allen, manager of high-rel engineering at Solid State. "When you're putting a part like this into a nuclear missile, you don't want to take any chances," says Allen. "You want to be sure that it's going to work." Rockwell is using the chips for the central processing unit of the guidance and control system for its Small Intercontinental Ballistic Missile project.

Rockwell designed the chips using Solid State's standard cell library. But Rockwell didn't use any brand-new, leading-edge technology. The 1750A processor, which includes six logic chips and five read-only-memory chips, is built in 3-μm design rules—not great density considering the single-chip 1750A implementations that are available. The company wanted predictable performance and a reliable process, and that's what it got: the parts can withstand a 1-megarad dose of radiation.

Solid State is now producing samples of the CPU with its SOS technology (see fig. 1). Inherently radiation-hard, SOS offers not only a high tolerance for total-dose radiation, but also virtual immunity to single-event upset, a condition that can be caused by a sudden, overwhelming dose of gamma irradiation. In a missile application, that can mean the difference between whether an ICBM fires or fizzles.

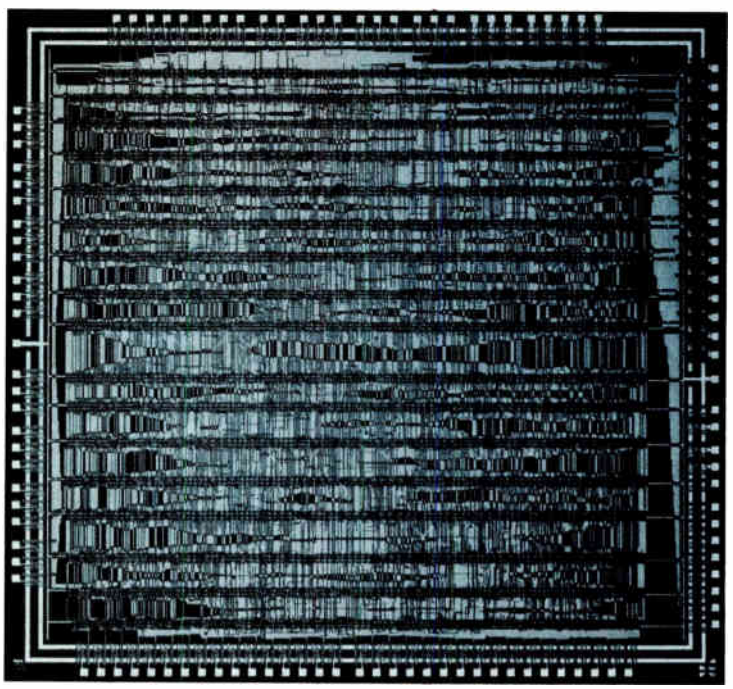
The chips are composed entirely of cells from GE/RCA's SOS library and include no full-custom sections, says Vincent DeMartino, manager of parts, material, processes, and specialties at Rockwell's Autonetics division. Moreover, they were designed as a set, and as a set only. But even though they were built specifically for the Small ICBM project, they are a true Mil 1750A implementation, featuring the complete 1750A instruction set in microcode and a facility to program in application-specific macrocode.

The chip set consists of 11 chips in all, including six large-scale integrated circuits (see fig. 2), four 16-Kbit read-only memories that contain the 1750A microprogram controls and some built-in custom macroprograms, and a fifth ROM chip that interfaces one of the logic ICs to the microprogram controller.

The six logic ICs include an instruction prefetch/direct-memory-access bus controller with two 16-bit instruction registers, a 16-bit instruction multiplexer, and other logic. It performs four functions: accessing and decoding instructions; immediate field multiplexing; determining the register tags; and controlling the direct-memory-access bus and the data-to-memory bus. Its output goes to the chip set's second device, the register file/fixed-point arithmetic logic unit.

This chip is composed of eight functional units, including a 16-word-by-16-bit register file, a 16-bit ALU, two 16-bit multiplexers, a register tag logic block, zero-test and carry/lookahead logic blocks, and a 40-bit composition register to capture results. It performs all fixed-point multiplication and division, and both loads and retrieves data from the register file. The chip also composes all 16-, 24-, 32-, and 40-bit words used in fixed- and floating-point operations.

A third chip is a status register/memory ad-



1. RAD-HARD. A floating-point ALU and barrel shifter is one of the six logic ICs in Rockwell's radiation-hardened version of the MIL STD 1750A computer.

dress chip with two loadable 16-bit counter/timers, the CPU's interrupt controller, the memory address controller, and the control-file registers. It includes a 10-μs and a 100-μs counter. These generate interrupt signals, as does the timer interrupt; the interrupts are then handed down to an interrupt controller, which also handles 13 other interrupt signals that come in from outside the CPU.

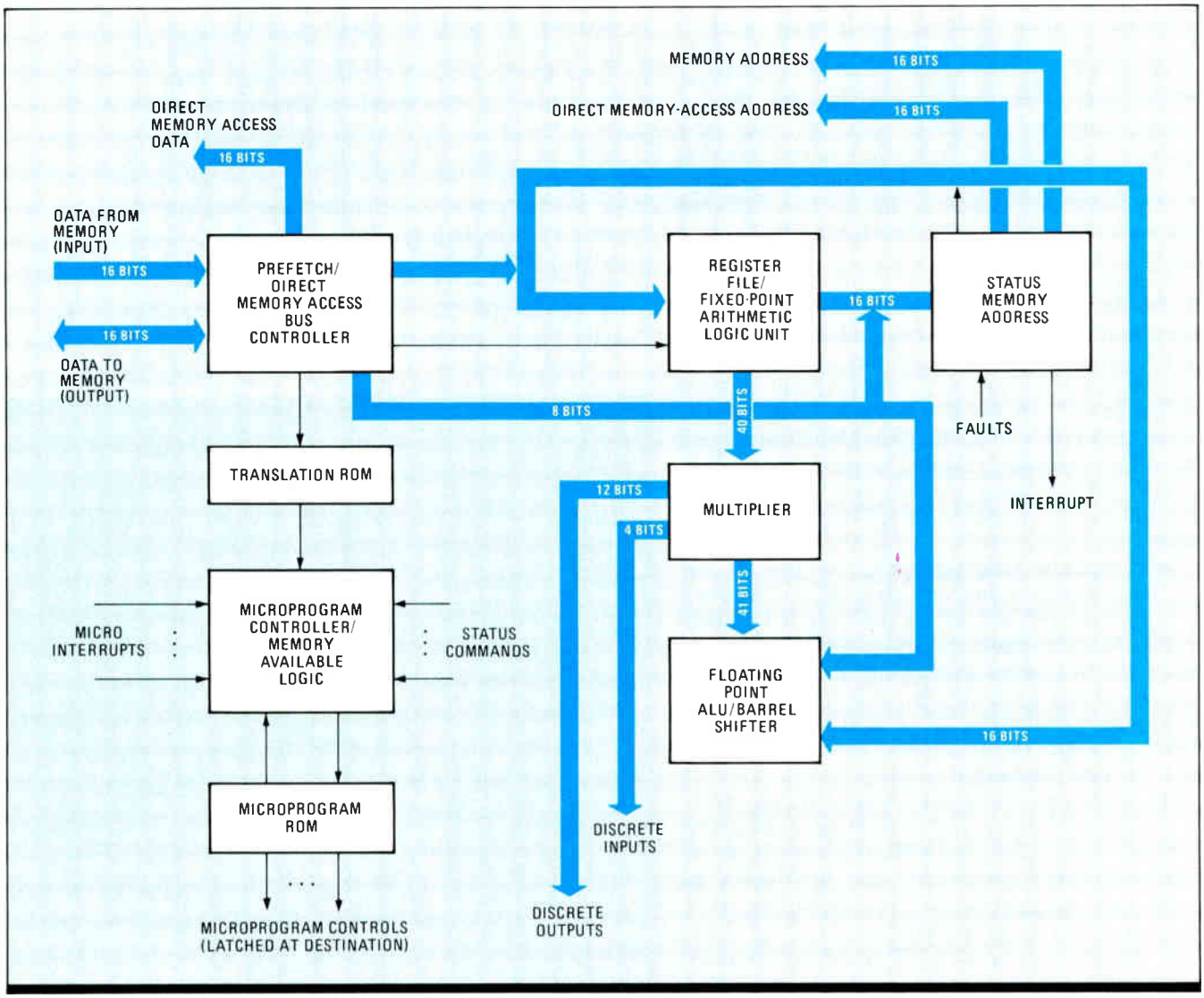
The fourth chip is a multiplier that outputs to the floating-point ALU. Besides calculating all integer and floating-point multiplications, other features are also implemented here to save room. Discrete logic-level signals—12 output signals and four inputs—can enter the CPU through the multiplier chip from elsewhere in the system. The multiplier takes output signals from the file register/fixed-point ALU chip, multiplies the results, and multiplexes the output data for the floating-point ALU/barrel-shifter chip. Corrections to and testing of the result are performed there.

The fifth chip is the ALU/barrel shifter. It has a 41-bit ALU that feeds a 41-bit accumulator/shift register. The register's output goes to the ALU, a 40-bit barrel shifter, and a demultiplexer. The floating-point ALU/barrel shifter is responsible for all floating-point operations, division operations, and shifting operations. The ALU, actually a 41-bit adder/subtracter, is partitioned into ten 4-bit ALUs and one 1-bit sign ALU. The barrel shifter is a 41-bit bidirectional multiple type one-pass shifter.

The final chip is a microprogram controller that acts as the main CPU interface to the five ROM chips that hold the 1750A microcode. Ultimately, the controller ties the CPU together. It is the main interface to the five 1-Kbit-by-32 bit read-only memory chips that contain the microcode that runs the CPU. Acting as an arbitrator, it determines the address of the next needed macroinstruction and decides what chip gets access to the memory bus and when.

–Tobias Naegele

For more information, circle 484 on the reader service card.



2. CHIP SET. The functions of Rockwell International's 1750A processor are partitioned among six SOS logic chips, which include an instruction prefetch/direct-memory-access bus controller, and are accompanied by translation and microprogram ROMs.

IS 1750A TAKING OFF? SOME THINK SO

The suppliers of the Air Force's 1750A microcomputers are ready to go—at least 17 of them at last count. Now all these chip, board, and box builders need is the big equipment market they're betting on. While it isn't here yet—this business may account for as little as $15 million this year—some observers see a recent spurt in activity as the turning point upward.

The reason for the traffic jam of suppliers—which range from the large chip makers to the major aerospace contractors—in such an embryonic market is that they see the MIL-STD-1750A processor as the basic building block, or linchpin, for the next generation in defense electronics. The architecture already has become the long-sought-after 16-bit standard for all Air Force avionics gear, and soon it will play the same role in hardware for the other services, according to industry sources. Because of this potential, some chip vendors look for a market that would be the military counterpart of the personal computer.

The 1750A, in fact, is so important to future military business that most component suppliers are spending millions of dollars to get on board with products. "We have to be [in the 1750A game]," says Dennis Snyder, product line manager for military standards at the United Technologies Corp. Microelectronics Center, Colorado Springs. Its entry is a 12-MHz 1750A processor based on a 3-μm CMOS gate array, the first designed with a reduced-instruction-set-computer architecture. It is now being upgraded to a 1.5-μm, 16-MHz model.

The list of 1750A suppliers certified by the Systems Engineering Avionics Facility at the Wright-Patterson Air Force Base in Ohio is growing fast. So far, 11 have met the latest version of the standard by satisfactorily running a mix of instructions called the Szeverenko benchmark. All suppliers of 1750A central processing units, whether they're offering chips, boards, or full computers, must be certified to qualify for Air Force use, so the roster should grow steadily longer.

This broadening range of choices delights military contracting organizations, says a Wright-Patterson official. It gives contractors a range of choices that's rare in defense electronics. Suppliers generally agree that this competition is good for the market. "The competition will make the market grow," says Ronald Burns, product manager for the 1750A chip at Fairchild Semiconductor Corp., Cupertino, Calif. "The customer has options now. He can buy a multiplicity of form factors, chips, boards, boxes, or full computers." Fairchild's F9450 chip was the first off the mark

THE INCREASING NUMBER OF SUPPLIERS DELIGHTS MILITARY CONTRACTORS

The list of players in the 1750A military computer game is long and growing. The range of their offerings is broad, from single chips to multiple-board processors, built with a variety of process technologies. Among them are:

- Allied-Bendix Flight Systems Division, Teterboro, N. J. Bendix has built a display processor for military aircraft based on Fairchild's F9450E chip.
- Control Data Corp. It received 1750A certification in September 1986 for its Spacecraft Control Processor, a multiple-board central processing unit built with 2-μm CMOS silicon-on-sapphire chips from Rockwell International Corp. [*Electronics*, July 10, 1986, p. 27].
- Fairchild Semiconductor. Its F9450E is a one-chip processor built with 3-μm bipolar Isoplanar integrated-injection-logic.
- The GE/RCA Solid State Division in Somerville, N. J., in partnership with Rockwell International's Autonetics Strategic Systems Division in Anaheim, Calif. They are developing a new radiation-hardened SOS 1750A chip set with 3-μm design rules (see p. 91).
- Harris Corp., Melbourne, Fla. It has two radiation-hard CMOS chip sets in the works, neither of which is yet certified. One is built with a 3-μm process, the other in a 1.5-μm VHSIC process.
- Honeywell Inc. The company has been awarded a $15.5 million contract to produce a 1750A chip set for the Generic VHSIC Spaceborne Computer program.
- IBM Corp.'s Federal Systems Division. The Manassas, Va., division is developing a 1750A chip set as an offshoot of its VHSIC program, in 1-μm CMOS.
- LSI Logic Corp. of Milpitas, Calif. It has two chips available, a processor and a memory-management unit. Not yet certified, the 1.5-μm parts are gate arrays built with a commercial process but benchmarked at 25 MHz over the military temperature range.
- McDonnell Douglas Corp., St. Louis. It built its MCD281 rad-hard three-chip set with a 4-μm CMOS SOS process.
- Performance Semiconductor Corp., Sunnyvale, Calif. The company has a single-chip processor, the PACE 1750A, running in both 20- and 45-MHz versions. The company says the 0.8-μm CMOS chip meets all Phase 1 VHSIC and military temperature requirements, although it is not a VHSIC chip.
- Texas Instruments Inc., Dallas. TI has the first Phase 1 VHSIC single-chip 1750A processor to be certified, built with a 1.25-μm bipolar process. It is in early production with a 10-MHz part; a 12-to-15-MHz version is due in late 1987.
- TRW Electronics & Technology Division, in partnership with the Delco Systems Operations of GM Corp. The partners have developed brassboard prototypes of a VHSIC 1750A computer built with a 1.25-μm CMOS VHSIC process.
- United Technologies Corp. Microelectronics Center, Colorado Springs. The center has come up with the UT1750AR, a single-chip 3-μm CMOS gate array. Prototypes running at 12 MHz are available; 1.5-μm arrays running at 16 MHz are being evaluated.
- Westinghouse Electric Corp.'s Defense and Electronics Center in Baltimore. It has certified a five-chip set based on 2-μm gate arrays. It is now enhancing that architecture in a 1.25-μm compiled three-chip VHSIC set to be fabricated by National Semiconductor Corp.

several years ago, establishing both the format and the pinout. Today it remains by far the volume leader; the company has sold more than 10,000 units after whipping production problems that dogged it until early 1986. Having adequate volume in hand now is another factor in spurring wider use of 1750A hardware, Burns says.

Optimism runs high among the ranks of 1750A market players. But most of them admit that they lack solid market projections to support it. "We don't have market numbers, only speculations," says Gary Craig, a senior product marketing engineer for the PACE 1750A chip at Performance Semiconductor Corp., of Sunnyvale, Calif. Integrated Circuit Engineering Corp., of Scottsdale, Ariz., for example, can only offer an estimate that 1750A products currently account for less than 10% of the $230 million value of all microprocessors used in military equipment.

Some see 1750A growing much as the PC market did

Given this void, manufacturers have been forced to fall back on their visceral knowledge of how new chip markets grow. At LSI Logic Corp., Hans Schwarz's "gut-level feel" tells him all hands will sell some 10,000 1750A processors this year, at an average price of about $1,300 each. Peripheral chips that tie them into systems will account for the remainder of the estimated $15 million market, predicts Schwarz, marketing manager for the LSI Logic 1750A. The Milpitas, Calif., company's entry, a processor and companion memory-management chip, are 1.5-μm gate arrays.

Schwarz predicts the steep takeoff will not occur until the second half of next year, when the suppliers get into volume production and the contractors for the major new military systems are picked. Those systems include the Air Force's Advanced Tactical Fighter, a possible Navy version called Advanced Tactical Aircraft, the Army's LHX advanced helicopter, and a host of integrated avionic systems. By 1989, annual volume should be at $35 million, Schwarz believes, and it should reach $45 million in 1990.

While companies such as Fairchild, LSI Logic, and Performance Semiconductor are doing well with the 1750A, they concede that a major impetus is now coming from the products offered by contractors in Phase 1 of the Defense Department's Very High Speed Integrated Circuits program. These devices, which are based on a 1.25-μm process, in effect set standards against which all 1750A suppliers must compete. Phase 1 contractors IBM Corp. and Texas Instruments Inc. each have their own 1750A chips certified; and TRW Inc. and Westinghouse Corp. are now in the last stages of developing a 1750A computer under a Phase 1 insertion award.

Within this field, TI is setting a fast early pace with its bipolar SLC1750 chip, says Randy Preskitt, VHSIC marketing manager in the Military Products Department of the Dallas company's Semiconductor Group. TI already has locked up the 1750A contract with Lockheed Corp., leader of one of the two major teams bidding on the ATF award. Industry chatter notes that TI is trying hard to line up the other team, led by Northrop Corp., as well. TI intends to have a 1-μm CMOS version ready by late 1988.

But some industry observers worry about a shakeout in 1750A players as competitive pressures build. What companies survive will be determined by the usual factors, they say: the capability to turn out products in ever-bigger volumes at lower prices. A shakeout could start as soon as late 1988. Average selling prices for chip sets should fall below $1,300 by then, Schwarz feels, and TI foresees even more drastic cuts. By 1990, TI says its high-volume customers will pay less than $500, compared with a single-unit sample price now of $3,200. Snyder predicts: "Some who are dabbling in the semiconductor market will drop out when the head-butting on price starts next year."

–Larry Waller

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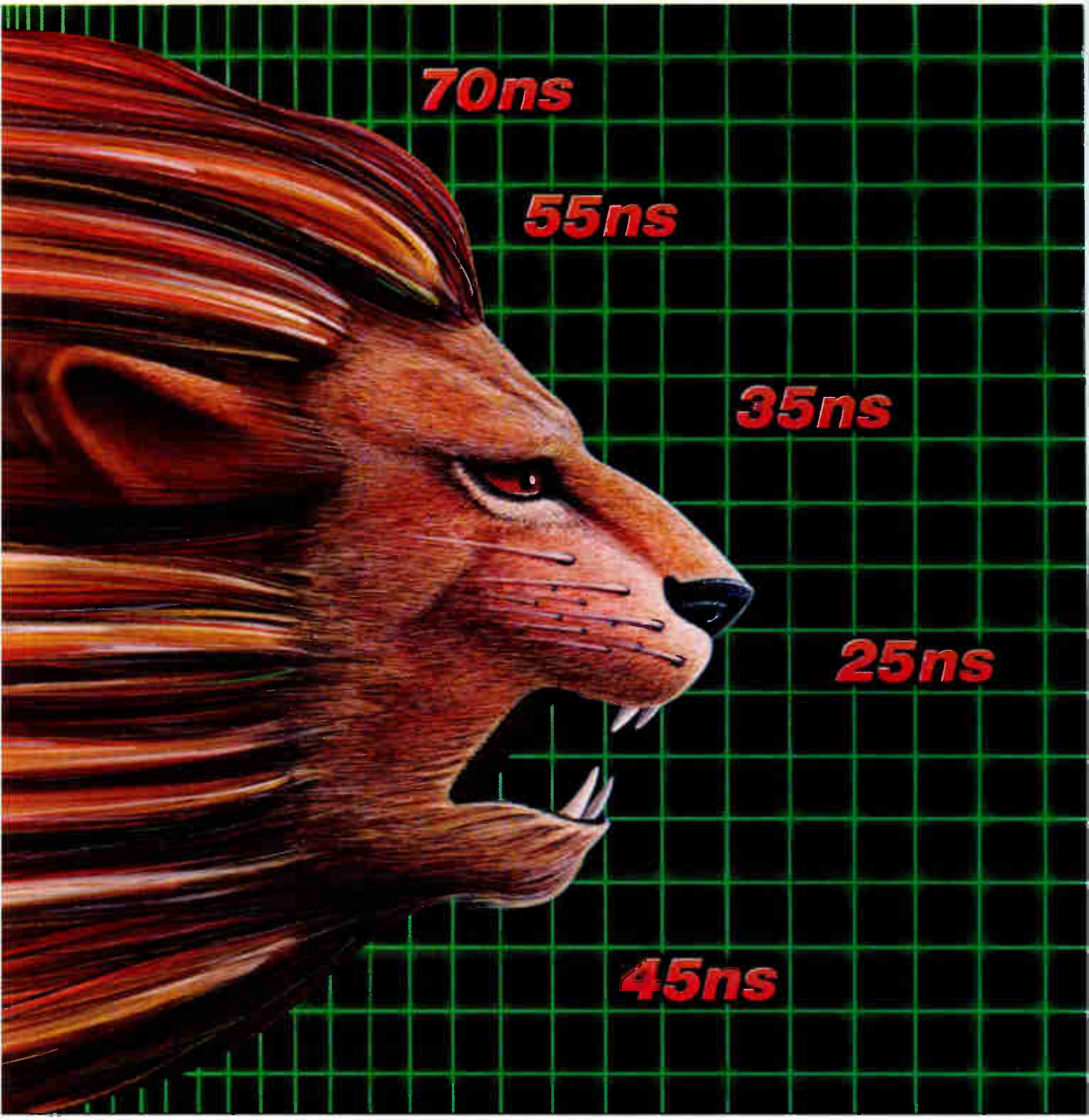

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TMM2068D	4KX4	35	20P	CDIP	NOW	NOW
TMM2068AD	4KX4	25	20P	CDIP	9/86	11/86
TMM2078D	4KX4	55	22P	CDIP	NOW	NOW
TMM2078D	4KX4	45	22P	CDIP	NOW	NOW
TMM2078D	4KX4	35	22P	CDIP	NOW	NOW
TMM2078AD	4KX4	25	22P	CDIP	9/86	11/86
TMM2018D	2KX8	55	24P	CDIP	NOW	NOW
TMM2018D	2KX8	45	24P	CDIP	NOW	NOW
TMM2018D	2KX8	35	24P	CDIP	NOW	NOW
TMM2018AD	2KX8	25	24P	CDIP	12/86	12/86
TMM2089C	8KX9	45	28P	SBDIP	NOW	10/86
TMM2089C	8KX9	35	28P	SBDIP	NOW	10/86
TMM2088P	8KX8	45	28P	DIP	9/86	12/86
TMM2088P	8KX8	35	28P	DIP	9/86	12/86
TC55416P	16KX4	45	22P	DIP	11/86	2/87
TC55416P	16KX4	35	22P	DIP	11/86	2/87
TC55416P	16KX4	25	22P	DIP	UNDER DEVELOPMENT	
TC55417P	16KX4	45	24P	DIP	11/86	2/87
TC55417P	16KX4	35	24P	DIP	11/86	2/87
TC55417P	16KX4	25	24P	DIP	UNDER DEVELOPMENT	
TC5561P	64KX1	70	22P	DIP	NOW	NOW
TC5561P	64KX1	55	22P	DIP	NOW	NOW
TC5562P	64KX1	55	22P	DIP	NOW	NOW
TC5562P	64KX1	45	22P	DIP	NOW	NOW
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MILITARY/AEROSPACE NEWSLETTER

DOD GIVES SOFTWARE DEVELOPERS MORE LEEWAY IN WRITING CODE

Military contractors no longer will be forced to use top-down methodology—in which design and coding of computer programs use a hierarchical structure—when developing software for the Department of Defense. The Pentagon has revised its two-year-old Defense System Software Development Standard, designated 2167, and will issue the new version, 2167/A, on June 30. The document spells out what the DOD expects from software contractors and gives them more leeway in writing code than the original standard. Although the DOD revised 2167 in response to industry dissatisfaction with the standard, some software suppliers are calling for further changes, such as provisions for rapid prototyping. Howard L. Yudkin, president of the Software Productivity Consortium, a Reston, Va., group representing 14 aerospace companies, is pushing for an industry position on where and how to use and not use 2167. The DOD, he says, should "recognize Standard 2167 as good for the engineering development phase for which it was intended, but not for advanced development." The Pentagon's Computer Software Management Subgroup, the joint-services committee responsible for 2167 revisions and compliance, believes that 2167 coverage of rapid prototyping is premature, according to Air Force Capt. Rick Schmidt, committee chairman. □

IT'S FULL SPEED AHEAD FOR UNISYS-WESTINGHOUSE ON AEGIS; ITT LOSES BID

Unisys Corp.'s Shipboard and Ground Systems Group, Great Neck, N. Y., and Westinghouse Defense Systems, Baltimore, will begin negotiations with the Navy in the next two to three weeks as the second-source team for the Aegis AN/SPY-1 shipboard radar system, for which RCA Corp. is prime contractor. ITT Corp.'s Gilfillan Division had filed a protest with the General Accounting Office to stop the award of the contract to the Unisys/Westinghouse team but was turned down in late May. In its protest, ITT claimed the Navy had restructured the second-source bid to require a full radar-development team, ruling out ITT, which only makes antennas, as a bidder. Unisys, Westinghouse, and ITT had all bid separately on the transmitter and phased-array antenna portions of the second-source contract when the Navy canceled the procurements and called for a combined rebid for the entire Aegis system. So far, RCA has received more than $1 billion as the sole contractor for Aegis, which is scheduled to be placed on 27 Ticonderoga-class cruisers and 29 Burke-class destroyers. A source involved in the negotiations has indicated that the Navy would prefer to work solely with RCA, because adding a second team now would add to the cost of the program. □

GROWTH IN SPENDING EXPECTED TO SLOW IN 1988 FOR MILITARY ELECTRONICS

Military electronics production in the U. S. will grow by only 4.4% this year and by only 3.6% in 1988, according to the Henderson Electronic Market Forecast. "Gramm-Rudman legislation and the president's opposition to tax increases leave little room for increased defense spending," says Edward Henderson, president of Henderson Ventures, a Los Altos, Calif., market research firm. President Reagan's budget request calls for a 2.1% decline in procurement but a 19.1% increase in research, development, test, and evaluation. Although the procurement budget contains the largest dollar figure for electronics, the RDT&E segment is much more electronics-intensive. On the average, Henderson says, procurement outlays contain 35% electronics, and RDT&E contains 49%. So the decline in the procurement budget is somewhat offset by the large RDT&E increase. Command, control, communications, and intelligence continues to be a strong growth area, with an 8% increase forecast for 1987 and a 5.8% increase in 1988. Radar systems, a weak spot, are expected to decline by 1.2% in 1987 and 4% in 1988. □

MILITARY/AEROSPACE NEWSLETTER

ISDN DEMO MAY LEAD TO AIR FORCE-WIDE NETWORK; ARMY AND DCA INTERESTED

The Air Force intends to build a demonstration integrated-services digital network at Mather Air Force Base, Sacramento, Calif., the center for evaluating computer hardware, software, and telephone-switching systems for the Air Force model-base program. A potential forerunner for an Air Force-wide ISDN, the Mather installation would allow access to all types of communications through a single system. The project has caught the eye of both the Army and the Defense Communications Agency as well. The Air Force Communications Command, Scott Air Force Base, Belleville, Ill., will meet with Army Information Systems Command officials to discuss the Mather project and may invite the Army to participate in future development meetings. The Defense Communications Agency is also interested in the Air Force test. The agency is considering tying its Defense Data Network into an ISDN. □

SIA GOES TO CAPITOL HILL TO LOBBY HARDER FOR SEMATECH

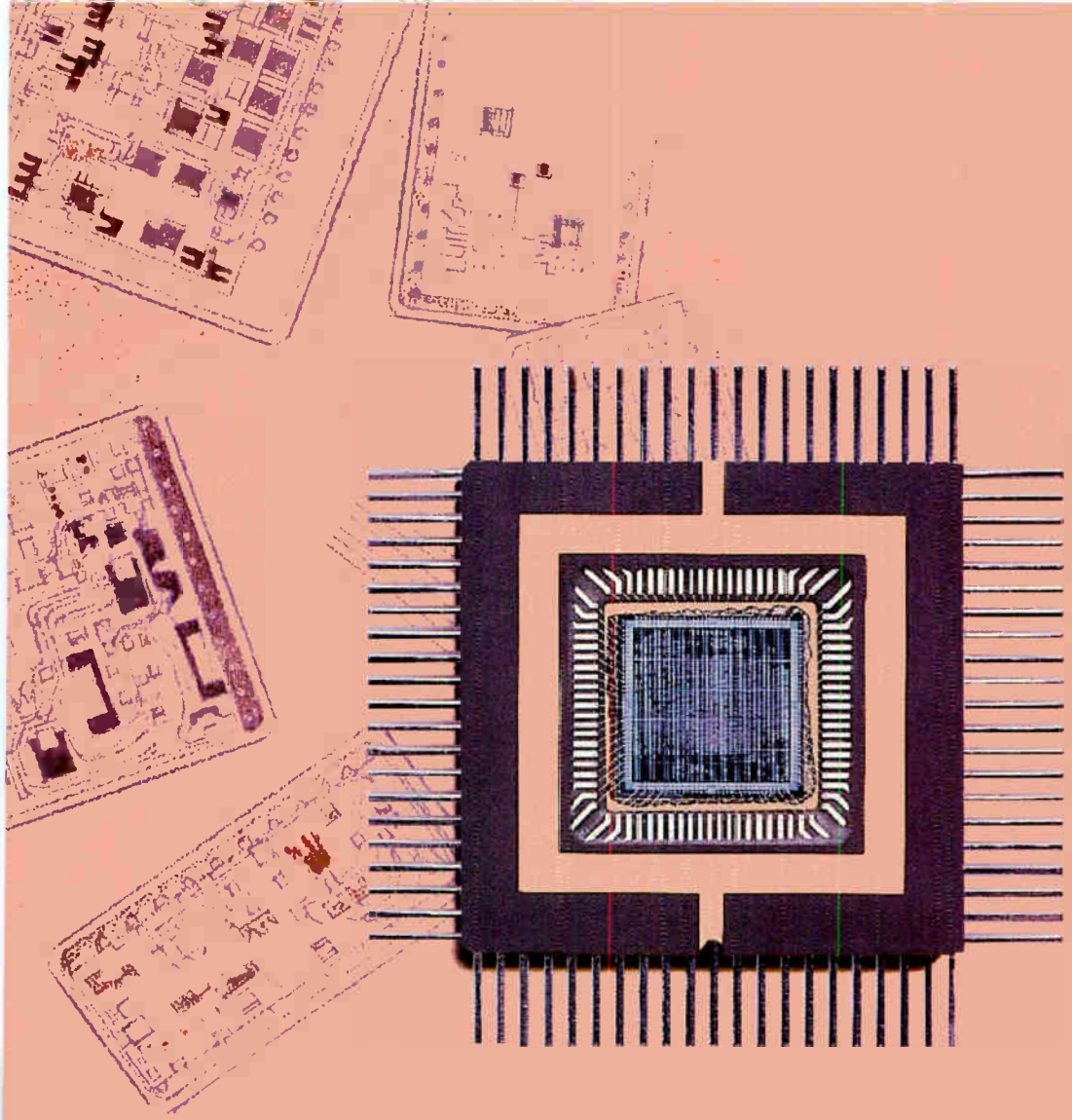
With several pieces of Sematech-related legislation—notably defense authorization budgets—still very much in limbo in Washington, the Semiconductor Industry Association has invited key legislative aides of both houses of Congress to a briefing on June 10. "Some people would call it lobbying," says an SIA spokesman. "We just want to get some of the more influential legislative aides together and bring them up to date on our plans and progress." Two sessions have been scheduled to ensure attendance at the briefings, which will be conducted by Robert N. Noyce, vice chairman of Intel Corp., and William N. Sick, executive vice president of Texas Instruments Inc. □

VERDIX TRIES TO SPEED NSA ENDORSEMENT OF SECURE LOCAL-AREA NET

Verdix Corp. isn't scheduled to deliver its multilevel secure local-area network to the DOD's National Security Agency until the end of this year, but it has already shipped at least two of the systems to defense contractors with an immediate need for high-security LANs. Also, evaluation of the system by the contractors is expected to speed NSA endorsement of the secure LANs, which the Chantilly, Va., firm is developing under an NSA contract. Meanwhile, the NSA's National Computer Security Center is reportedly ahead of schedule in the development of a security processor that removes the security function from a host computer. The center hopes to demonstrate prototypes of the processor sometime next year. NCSC is working with Honeywell Secure Computing Technology Center, St. Anthony, Minn., to develop products under the secure processor program, which is expected to satisfy or exceed all DOD Trusted Computer Systems Evaluation Criteria A1 requirements. □

EMBEDDED COMPUTERS YET TO MAKE THE TEMPEST LIST

The number of computers and communications systems shielded against electronic eavesdropping that qualified under the Pentagon's Tempest program jumped from 177 in January 1984 to 386 in January 1987. But so far, no hardware embodying the 1750A instruction-set architecture for 16-bit computers and none of the military's AN/UYK series computers has qualified, limiting protection for embedded systems, says International Resource Development Inc., a Norwalk, Conn., research firm, in a study of the Tempest market. IRD points out that embedded systems like flight computers are not normally within eavesdropping range when in use. But programs for them are developed on secure computers—shielded against electromagnetic radiation—and later put at risk by testing in unshielded areas. "This lack will have to be addressed soon," IRD says. □



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NEW PRODUCTS

FINGERPRINT READER RESTRICTS ACCESS TO TERMINALS AND PCs

$995 UNIT MATCHES STORED THUMBPRINT WITH THAT OF PROSPECTIVE USER

An electronic fingerprint verification system similar to those that control access to restricted areas has been developed to protect sensitive information from unauthorized access via personal computers and data terminals. Consisting of a software package and a peripheral about the size of a modem, the ThumbScan system from ThumbScan Inc. costs less than a third the price of conventional fingerprint readers.

The ThumbScan system operates by using software to match a template of a stored thumbprint to an image created by a user pressing a thumb or finger into the peripheral device. If the images match, access is granted within 3 to 5 seconds, says Peter Dignan, the president of ThumbScan, an Oakbrook Terrace, Ill., startup. For additional security, ThumbScan incorporates data-encryption techniques to foil anyone trying to break the system.

CODED. ThumbScan can add data encryption for another level of security.

OEM PRICE. The system is believed to be the first fingerprint security package aimed at the personal-computer and terminal market. "We are definitely the first with a fingerprint system priced under $3,000," says Dignan. ThumbScan will sell for $995 in single-unit quantities and for less than $500 each for volume orders over 100.

Besides its low price, the 5.5-by-10.5-by-1.8-in. ThumbScan unit is considerably smaller than earlier fingerprint systems used for physical-access control, Dignan says. Those systems typically measure a cubic foot and weigh 25 to 30 lbs, he says. The ThumbScan unit weighs just 2.8 lbs.

The key factors in achieving the ThumbScan's low price and small size are the use of an advanced optical technique for image acquisition, as well as increased integration at the electronics level. Dignan declines to provide details, but he notes that unlike earlier systems that acquire images via a Xerographic technique, ThumbScan's optical system contains no moving parts.

The ThumbScan comes in three versions. The TSI 101 handles asynchronous terminals. The TSI 201 hooks up to bisynchronous terminals, such as IBM Corp.'s 3270 line. The TSI 301 runs on the IBM Personal Computer family and compatibles.

In networked terminal applications, the software that runs the system resides in the host mainframe or the minicomputer. For use with PCs, ThumbScan Inc. offers either floppy-disk-based software or an auxiliary board that plugs into the PC and contains the system software. "If you've got a PC and you don't even want it to boot up [for an unauthorized user], that's what the board will stop," says Dignan.

The software version can't stop boot-up, but it does require fingerprint authentication before allowing access to secondary hard-disk storage.

For added security, the ThumbScan's system software comes with the National Bureau of Standards' Data Encryption Standard algorithm built in. "When you store on secondary storage, we scramble the data," Dignan says. "If somebody breaks through the [fingerprint] system and he gets access to your data, the data is unusable, because he doesn't have the encryption key." For PC users who are particularly security-conscious, the company offers a board version with a chip that incorporates the DES algorithm in hardware. It costs $200 extra.

SHIPPING. The ThumbScan is set for introduction at the National Computer Conference. Dignan says 52 units will be shipped in mid-July to a half-dozen networked-terminal beta sites and 14 PC-user beta sites. The company plans to hit production levels by November.

Until an adequate number of units have been field-tested, Dignan is reluctant to predict the reliability of the ThumbScan. But design goals call for the system to permit access to an unauthorized user only 1 in 20,000 times, he says. The design goal is 1 in 200 for authorized users not being allowed access to data.

The ThumbScan is aimed at large users with sensitive data, such as government agencies, oil companies, and companies with large customer mailing lists.

–Wesley R. Iversen

ThumbScan Inc., Two Mid-America Plaza, Suite 800, Oak Brook Terrace, Ill. 60181. Phone (312) 954-2336 [Circle 460]

NCC 1987

With just 160 exhibitors and an expected crowd of 30,000 this year, the National Computer Conference has certainly seen better days. But organizers say the show (see p. 42) at Chicago's McCormick Place June 15-18 will host the introduction of no fewer than 100 products aimed primarily at the computer-peripheral market, some of which are previewed on the following pages.

KURZWEIL'S ENTRY IN LOW-END SCANNERS

A scanning system that can read 60 characters/s, scan high-contrast and half-tone graphics, and handle multiple type styles on the same page is coming from Kurzweil Computer Products Inc. The company linked proprietary character-recognition software to a coprocessor board based on a 32-bit microprocessor to create the Discover 7320.

The system targets low-volume users in small companies and work groups in such applications as desktop publishing. It costs less than $10,000 and plugs into an IBM Personal Computer AT or compatible, which is not included in the price. Since the coprocessor board handles image-recognition and -manipulation chores, other applications can run on the PC AT during scanning.

HIGH TO LOW. Kurzweil, an established vendor of high-end scanning systems that cost $40,000 and up, has basically scaled down its Kurzweil 4000 system, which uses the Motorola 32-bit 68020 microprocessor, to make the new system. Unlike high-end scanners, the Discover 7320 does not store both text and graphics at the same time. Nor does it store text in two-column format. And so far, it can recognize only characters used in English.

Several other companies also offer low-end scanners, among them Compu-Scan Inc. of Fairfield, N. J., and Dest Corp. of Milipitas, Calif., according to Marty Gruhn, executive vice president of the Sierra Group, a Tempe, Ariz., market research company. But, she says, Kurzweil's reputation as a seller of high-end systems should help it enter the relatively low-end markets of desktop publishing and office automation.

At the heart of Kurzweil's scanner technology is the Xerox-owned company's artificial-intelligence software, called Intelligent Character Recognition. ICR analyzes the geometric and topological properties of text, stores the information it gathers, and then makes decisions about characters according to rules of character formation. This makes it more versatile than the traditional optical-character-recognition systems commonly used for reading highly standardized documents such as tests, vouchers, questionnaires, and retail labels. Those systems match strictly defined sizes and spacings of text to preprogrammed character templates.

ICR also analyzes the format and layout of a page, separates text and graphics, resolves ambiguities between similar characters such as "l" and "1," decides where to split touching characters, and ignores noise or dirt, such as staple marks or scribblings, according to the Cambridge, Mass., company. Information acquired about a page is then used to "teach" the system about succeeding pages, which speeds up the scanning process.

The Discover 7320 scans areas up to 8½ by 14 in. and handles type sizes from 8 to 24 points. It has a 10-page automatic feeder and built-in user-definable lexicons of either 10,000 or 40,000 words. Its software is menu-driven.

The system that will become available July 1 will include a desktop scanner, software, and a coprocessor board that contains either 2 or 4 Mbytes of random-access memory. A 2-Mbyte system costs $9,950, and the 4-Mbyte system is $11,950. *–Paul Angiolillo*

Kurzweil Computer Products Inc., 185 Albany St., Cambridge, Mass. 02139.
Phone (617) 864-4700 [Circle 461]

PCs SHARE PRINTER FOR ONLY $200 EACH

Printer sharing and data transfer between personal computers with the NetCommander from Digital Products Inc. costs about $200 per port instead of the $1,000 per port of a typical local-area network.

Based on an asynchronous RS-232-C communications interface, Zilog Inc.'s Z-

80 microprocessor, and a variety of memory-buffering options, the 6- and 10-port NetCommanders target work groups of three to eight personal computers.

Both products support transmission rates up to 19.2 Kbits/s. Compatible with all personal-computer operating systems, NetCommanders can also interface with full-scale LANs over standard network interfaces.

Model NC/6S and NC/10S are available with 6 or 10 serial ports and have a 250-Kbit buffer that is expandable to 1 Mbit. Model NC/10SP offers six serial and four parallel ports and a 250-Kbit buffer that is expandable to 2 Mbit.

Available now, the 6-port products cost $1,095, and the 10-port products are $1,995.

Digital Products Inc., 108 Water St., Watertown, Mass. 02172.
Phone (617) 924-1680 [Circle 465]

WRITE-ONCE OPTICAL DISK IS IBM-COMPATIBLE

Data/Ware Development Inc.'s Mainframe Optical Storage Transport (MOST) family of write-once data-storage systems offers 2-gigabyte capacity and is plug-compatible with IBM Corp. System/370 magnetic-tape units.

The DW34800 offers a transparent interface with IBM's MVS and VM operating systems, as well as with Microsoft Corp.'s DOS operating systems.

Units consist of a MOST controller, one or more disk drives, and an automatic cartridge handler. Software modifications are not required, because drives are added to the basic unit.

The Model DW34800-P basic system accommodates up to two drives and costs $54,795 with a single disk drive. Adding the second drive costs $16,340.

The top-of-the-line Model DW34800-J2 is a jukebox version that takes up to four drives and stores 95 cartridges. It features a robotic cartridge-handling system and costs $187,145. These and other intermediate models are available now.

Data/Ware Development Inc., 4201 Sorrento Valley Blvd., San Diego, Calif. 92121.
Phone (619) 453-7660 [Circle 466]

DIGITIZER EMULATES INDUSTRY STANDARD

A digitizing tablet from Pentel of America Ltd. features four operating modes and emulation of an industry-standard digitizer. Any software that accepts input from Summagraphics Corp.'s Bit Pad One will also run on Pentel's DST-4AN digitizer.

In the streaming mode, data flows continuously as long as the stylus pen is within 3 mm of the tablet. The point mode reads single data points by pressing the pen to the tablet.

Switch Stream Mode 1 provides a continuous data stream when the pen is pressed on the tablet, and Switch Stream Mode 2 permits continuous data reading of single points.

The active digitizing area is 11.8 by 8.3 in. Data is transmitted via an RS-232-C port at a set rate of 1,200, 2,400, 4,800, or 9,600 bits/s.

The digitizer supports both English and metric scaling and is accurate to 0.025 in. Available now, the DST-4AN costs $419.

Pentel of America Ltd., 2805 Columbia St., Torrance, Calif. 90503.
Phone (213) 320-3831 [Circle 467]

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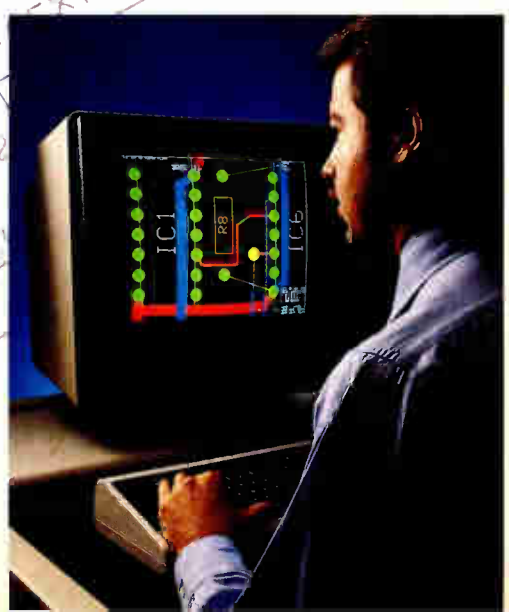


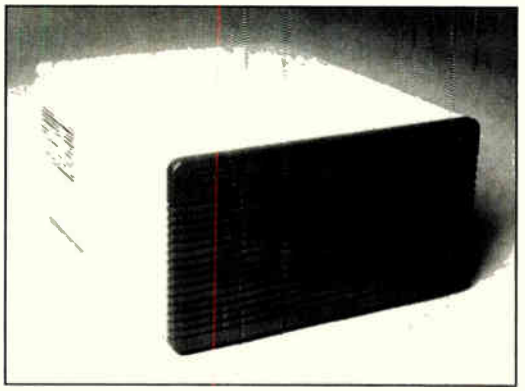
Circle 106 on reader service card.

THIS SYSTEM INTEGRATES DSP AND IMAGE PROCESSOR

DATACUBE'S DSP 1000 SYSTEM IS SAID TO ELIMINATE THE COST AND RISK OF DEVELOPING CUSTOM SYSTEMS

A fully assembled digital-signal-processing and image-processing package saves DSP designers the time and risk involved in specifying customized, board-level hardware for every new development application. Datacube Inc.'s DSP 1000 is the first such package, the company claims.

The system reduces recurring development costs in two ways. Its seven boards emulate any functional module in the company's MaxVideo 17-board family. But it is also expandable, so users who want the maximum performance furnished by a board designed for a particular function can add that board to the seven. By furnishing a package that provides a variety of functions, the DSP 1000 resolves the dilemma of video designers who have to choose between spending thousands of dollars on boards they might not need or finding midway through the design that they must purchase one or more additional boards.



POWERFUL. The 20-slot, VMEbus-compatible DSP 1000 can be easily expanded to enhance performance.

The Peabody, Mass., company created DSP 1000 by integrating seven of its VMEbus-compatible MaxVideo boards. Those boards capture, enhance, and display video, acoustic, X-ray, infrared, and other high-bandwidth analog signals.

Euclid, a programmable DSP module [*Electronics*, June 16, 1986, p. 74], is the system's backbone. Based on Analog Devices Inc.'s ADSP 2100 chip, it runs at up to 8 million instructions/s and can be programmed in C or assembly language. A von Neumann processor optimized for DSP applications, Euclid has a library of image-processing and numerical routines, a C compiler, and strong VMEbus compatibility.

Digimax, an analog-to-digital and digital-to-analog converter, converts standard video signals in real time. The module includes eight camera inputs, three output digital-to-analog channels, and graphics-overlay hardware. The other signal acquisition module, Max-Scan, locks into most video cameras, including fast- and slow-scan units, high- and low-image resolutions, and line-scan sensors. It also digitizes nonvideo signals such as those from seismic, radar, sonar, ultrasound, X-ray, and infrared sources.

For performing real-time image and signal-convolution algorithms, DSP 1000 contains the VFIR Mk II module. The module works on 8-by-8 or 64-by-1 convolution kernels with a 10-Mbyte/s digital signal stream.

Two region-of-interest frame-store modules, ROI-Stores, can be used simultaneously, one processing while the other maintains a steady visual display. Or they can be cascaded to provide two 16-bit-deep signal-output pipelines. The modules include hardware support for pan, scroll, and zoom programming.

256 COLORS. The Max-Graph module controls graphic displays, user interfaces such as menus, and overlays. It can overlay graphics with real-time digital video signals and supports the simultaneous display of 256 colors.

A digital cross-point switch, Max-Mux, governs all the DSP 1000 modules via Maxbus. With Max-Mux, programmers can use software to dynamically reconfigure the data stream between modules without having to switch internal connectors manually.

The DSP 1000 comes in configurations for Sun Microsystems Inc.'s Sun-3 work stations and for Motorola Corp.'s 68020-based systems running on Microware Inc.'s OS-9 operating system. Available now in a chassis that includes a 750-W power supply and forced-air fan cooling, the system costs $46,000.

– *Paul Angiolillo*

Datacube Inc., 4 Dearborn Rd., Peabody, Mass. 01960.
Phone (617) 535-6644 [Circle 340]

SYSTEM LETS FOUR PCs SHARE PERIPHERALS

Fifth Generation Systems' Logical Connection peripheral-sharing system allows as many as four personal computers to share access to printers, plotters, and modems as well as to communicate with each other.

The system reduces costs by eliminating the need for dedicated interfaces, such as local-area-network boards for each personal computer.

Parallel-to-serial and serial-to-parallel conversions are performed automatically to match dissimilar devices. Configurations of computers and peripherals are controlled through a switching menu called PopLC.

When more than one computer has a task for the peripheral, the Logical Connection spools the computer transmissions into a random-access-memory buffer and processes each according to the order in which they were received.

A 256-Kbyte buffer is standard with the system, and a 512-Kbyte buffer is available as an option.

The system can be altered to allow the computers to share data files by adding any of a number of personal-computer communications programs.

Logical Connection also has a reset switch that eliminates the need to unplug and reconnect the device when diagnosing problems. Light-emitting-diode displays aid in identifying problems with printers or other peripherals.

As many as 45 Logical Connections can be daisy-chained for peripheral sharing at remote sites up to 0.7 miles away. Available now, Version 3.0 of the Logical Connection costs $495 with a 256-Kbyte buffer and $595 with a 512-Kbyte buffer.

Fifth Generation Systems, 11200 Industriplex Blvd., Baton Rouge, La. 70809.
Phone (213) 493-4483 [Circle 348]

BACKUP POWER UNIT GROWS AS NEEDED

Modular Power Corp.'s Upstar power supplies for backing up mainframe computer systems present an innovative modular approach to uninterruptible-power-supply technology that allows users to add 12-kVA modules up to a maximum of 360 kVA.

A microprocessor-based controller monitors power output from each module to maximize system efficiency. It also diagnoses potential problems, such as battery depletion, and minimizes distortion by automatically correcting phase differences between input and output.

The unit is controlled through graphic displays that present each module's operating status, and programming is simplified by built-in operator prompts.

A typical system for a mid-sized computer installation occupies 9 sq. ft and

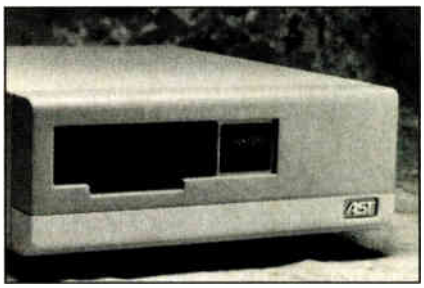
weighs 2,000 lbs, compared with 30 sq. ft and 6,500 lbs for competing units. This means the system can be installed right in the computer room, which reduces cabling costs.

A basic Upstar module costs $30,200. Delivery takes 90 days.

Modular Power Corp., 1150 Ringwood Ct., San Jose, Calif. 95131.
Phone (408) 432-3060 [Circle 349]

MAC II DRIVE BOASTS 5-MBYTE/S I/O RATE

AST Research Inc.'s Small Computer System Interface-compatable FAST 20 Winchester hard-disk drive offers users of Apple Computer Inc.'s Macintosh II and SE models a data-transfer rate of 5 Mbytes/s, 20 Mbytes of storage, and an average access time of 68 ms.



The 5-Mbyte/s input/output speed is achieved by reading each sector of the disk during each revolution, instead of the more conventional method of reading every other sector or every third sector.

Dual SCSI ports built into the 3½-in. drive let it accommodate up to seven SCSI devices, such as additional disk and tape systems.

Available now, the drive costs $1,195, including several software utilities such as data-backup and restore programs and disk-optimization software.

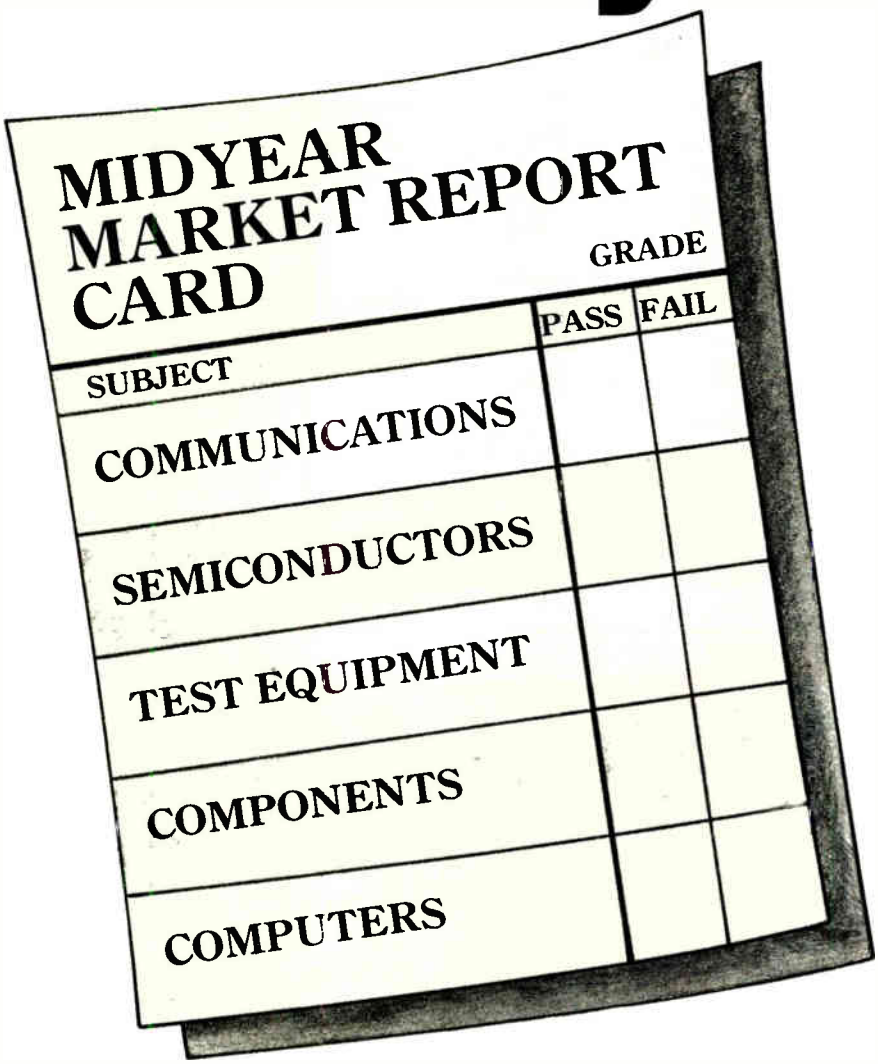
AST Research Inc., 2121 Alton Ave., Irvine, Calif. 92714.
Phone (714) 863-1333 [Circle 347]

FLAT-SCREEN CRT IS 50% BRIGHTER

A 14-in., high-resolution color monitor from Zenith Data Systems uses innovative shadow-mask technology to fabricate flat viewing screens that minimize glare and allow 50% more brightness and 70% greater contrast than current cathode-ray-tube screens.

Zenith's shadow mask—a thin metal sheet perforated with thousands of holes that help direct electrons to the screen—differs from current technology in two fundamental ways: conventional shadow masks are curved, and they are suspended inside the tube by springs. These shadow masks limit screen brightness, because intense electron bombardment heats up and distorts the mask. As the mask deforms, the loca-

Report Cards go out July 9th.



In the July 9th issue, the editors of *Electronics* will provide a special midyear report on the electronics and computer marketplace.

Though there were different schools of thought earlier in the year, the facts at midyear are encouraging—the industry is definitely on an upward trend. This report details the long-awaited turnaround.

And because we've done our homework, the July 9th issue will also feature a timely report on nonvolatile memory technology, as well as a special marketing section on interconnections.

So be smart. Put the July 9th issue on the top of your reading list. And if you're an advertiser, put your advertising message in the issue that will be required reading for more than 131,000 technical managers and their senior engineering partners.

The July 9th issue of *Electronics*. It's summa cum laude.

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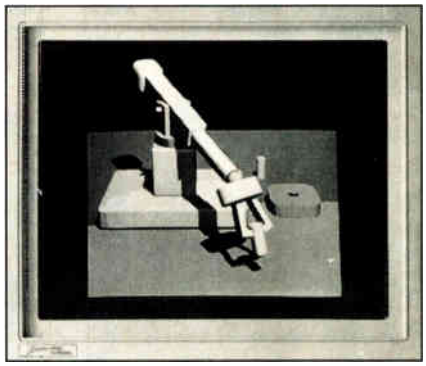
Electronics

tions of the holes move relative to the electron gun, thus degrading resolution.

Zenith's shadow mask is held flat under tension, making it virtually impervious to distortion. Brightness can be increased significantly, which in turn means that a dark-glass faceplate can be used to enhance contrast.

Although the ZCM-1490 monitor has adopted the 640-by-480-pixel resolution



standard in IBM Corp.'s Personal System/2 computers, it is capable of resolutions as high as 1,400 by 1,200 pixels.

The monitor and a companion Z-449 controller card that supports CGA, EGA, MDA, and Hercules software will be available in July. The monitor will cost $999, and the controller card will sell for $599.

Zenith Data Systems, 1000 Milwaukee Ave., Glenview, Ill. 60025.
Phone (800) 824-9000 [Circle 345]

HAND-HELD COMPUTER CAN PLUG INTO PCs

A hand-held computer from Psion Inc. offers 32 Kbytes of RAM and a communications module that links it via an RS-232-C port to most personal computers, peripherals, and modems.

To provide off-line memory similar to disk drives, the 5½-by-3-by-1-in. Organiser II Model XP has two slots for 128-Kbyte Datapaks implemented in EPROM that can be erased and reused.

Other components include an 8-bit Hitachi Ltd. 6303 CMOS processor running at 1 MHz, a 36-key keyboard, and an LCD screen that displays two lines of 16 characters each.

Applications programs written in Psion's Opel programming language are accessed through a scrollable menu screen. Optional 128-Kbyte memory modules fit in the Datapak slots for finance, math, and spreadsheet applications.

The Model XP costs $230. Datapaks with 16-Kbyte to 128-Kbyte memories cost from $30 to $180. The communications module costs $100, and the special applications programs cost $50 each. All are available now.

Psion Inc., 320 Sylvan Lake Rd., Watertown, Conn. 06795.
Phone 203-274-7521 [Circle 346]

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ELECTRONICS WEEK

TWO SOFTWARE GIANTS MERGE

Computer Associates International Inc. is acquiring Uccel Corp. in the biggest merger ever in the software industry. Both companies are leading independent software vendors of system and application software packages, primarily for the IBM Corp. mainframe world, but also for the minicomputers and microcomputers that connect with those mainframes. Computer Associates will pay some $800 million in stock for all outstanding Uccel common shares. Computer Associates of Garden City, N. Y., a $309-million-a-year company, will be the surviving firm. Dallas-based Uccel reported $142 million in revenue in 1986.

STANDARD OIL IS BIG ON SUBSTRATES

Standard Oil Engineered Materials Co. has rolled its three electronic-products business groups into a single unit: the Electronic Ceramics Division, with headquarters in Niagara Falls, N. Y. The division is investing $8.5 million in facilities that will produce surface-mount substrates and planar-diffusion sources for the microelectronics industry. The substrates, made of silicon carbide and aluminum nitride, dissipate heat better than the commonly used aluminum oxide, allowing integrated circuits to be mounted closer together.

APOLLO JOINS THE WALL ST. CROWD...

Now Apollo Computer Inc. will be competing with rival Sun Microsystems Inc. in a new arena: financial services. Like Sun [*Electronics*, May 28, 1987, p. 110], the Chelmsford, Mass., company will be selling its work stations on Wall Street. To attract customers, Apollo opened a New York office and has signed marketing agreements with several financial-services software vendors. The latest pact is with Prophecy Development Corp. of Boston, creators of Contessa, a program for managing financial resources.

...BUT KEEPS ITS OLD FRIENDS

Apollo has just closed its largest deal ever—an 18-month, $100 million contract to supply work stations to Mentor Graphics Co., a leading maker of computer-aided-design and technical-publishing systems. Mentor had revenues of $174 million last year, and analysts see better than $200 million coming in 1987. That explains the upping of the order, from $50 million worth of work stations over the last 12-month period, ended in May. Apollo supplies all of the work stations incorporated in the 6-year-old Beaverton, Ore., company's products.

ZENITH MS-DOS PC IS EASY TO USE

Zenith Data Systems has a new computer called the Eazy PC, and Robert Dilworth, the president of Zenith Electronics Corp.'s computer subsidiary, bills it as "the first MS-DOS personal computer with the ease of operation generally attributed to Apple's Macintosh." Introduced June 1 at the Spring Comdex show in Atlanta, the PC/XT-compatible machine comes in three configurations: model 1, with one 720-Kbyte 3½-in. disk drive, at $999; model 2, with two drives, at $1,199; and model 20, with a 20-Mbyte hard disk and one 3½-in. floppy drive, at $1,699. The machines have 512 Kbytes of random-access memory.

SUPER VHS LOOKS LIKE A WINNER...

One of the stars at the Summer Consumer Electronics Show in Chicago was the high-resolution ½-in. Super VHS video cassette format. Several companies, including JVC Co. of America and Toshiba America Inc., showed Super VHS machines, which will be selling in U.S. stores by August for around $1,200. Super VHS, with 400-line horizontal resolution, provides a better picture than standard VHS's 240 lines and has separate chrominance and luminance signals. Not to be outdone, Sony Corp. displayed its 500-line Enhanced-Definition Beta format, due in the U.S. by 1988. Video cassette cartridge maker 3M Co. of St. Paul, Minn., expects Super VHS to grab 90% of the VCR market by 1990.

...BUT WILL COSTLY CD/Vs SELL WELL?

Compact Disk Video players [*Electronics*, May 28, 1987, p. 34] can't fail to impress onlookers with their 5 minutes of digital video plus 20 minutes of audio. But despite lots of hoopla and a $2 million CD/V booth at the Consumer Electronics show, there remains doubt among industry observers that the $600-and-up players will sell well in the youth market, which seems to be their main target.

SONY, AMD TEAM UP ON CMOS SRAMs

Look for a standard 1.2-μm CMOS process from Sony Corp. and Advanced Micro Devices Inc. by early next year. The two have signed a three-year pact to jointly develop SRAM products, including high-performance 64-K and 256-K CMOS devices. The immediate goal after that is 1-μm parts, says W. J. Sanders III, chairman and chief executive officer of AMD in Sunnyvale, Calif. Akio Morita, chairman and CEO of Sony, calls the move a response to a "globalized" industry.

RODIME RESPONDS TO IBM ACTION

Rodime plc of Glenrothes, Scotland, is fighting to protect the validity of two patents it holds on 3½-in. hard-disk drives. IBM Corp. has asked a U.S. district court in Washington, D. C., for a declaratory judgment invalidating the Rodime patents on the grounds that they are vague, covering the 3½-in. form but no specific technology. Rodime responded by filing a counterclaim for damages. It contends that IBM is infringing on the patents with a 3½-in. drive it builds for its small systems, including the Personal System/2. Margaret Pfeiffer, of Sullivan & Cromwell, the Washington law firm representing Rodime, says the counterclaim is "just the beginning of a long lawsuit." No court date has been set.

TI SUFFERS BLOW IN DRAM SUIT

Texas Instruments Inc. has hit a snag in its battle with NEC Corp. over alleged infringements of patents covering dynamic RAMs. Janet Saxon, a U.S. administrative law judge in Dallas, ruled that NEC holds implied licenses on some key patents from an expired pact, and that TI had not bargained in good faith on renewing the licenses. TI is appealing to the International Trade Commission, which will make a final ruling by mid-September. Just prior to the decision, TI settled similar patent differences with Hitachi Ltd. out of court, but details were not disclosed.

RICOH ENTERS U.S. ASIC MARKET

Add Ricoh Ltd. to the list of Japanese companies seeking a foothold in the burgeoning U.S. market for application-specific ICs. Ricoh is setting up a semiconductor design center in San Jose, Calif., in which it will invest $14.3 million during the next three years. The center, to be called the Ricoh Electronic Devices Division, will start with a staff of 30 and grow to 150 people during that time.

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3 18 33 48	63 78 93 108	123 138 153 168	183 198 213 228	243 258 273 350	365 380 395 410	425 440 455 470	485 500 705 720
4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
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7 22 37 52	67 82 97 112	127 142 157 172	187 202 217 232	247 262 339 354	369 384 399 414	429 444 459 474	489 504 709 951
8 23 38 53	68 83 98 113	128 143 158 173	188 203 218 233	248 263 340 355	370 385 400 415	430 445 460 475	490 505 710 952
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10 25 40 55	70 85 100 115	130 145 160 175	190 205 220 235	250 265 342 357	372 387 402 417	432 447 462 477	492 507 712 954
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12 27 42 57	72 87 102 117	132 147 162 177	192 207 222 237	252 267 344 359	374 389 404 419	434 449 464 479	494 509 714 957
13 28 43 58	73 88 103 118	133 148 163 178	193 208 223 238	253 268 345 360	375 390 405 420	435 450 465 480	495 510 715 958
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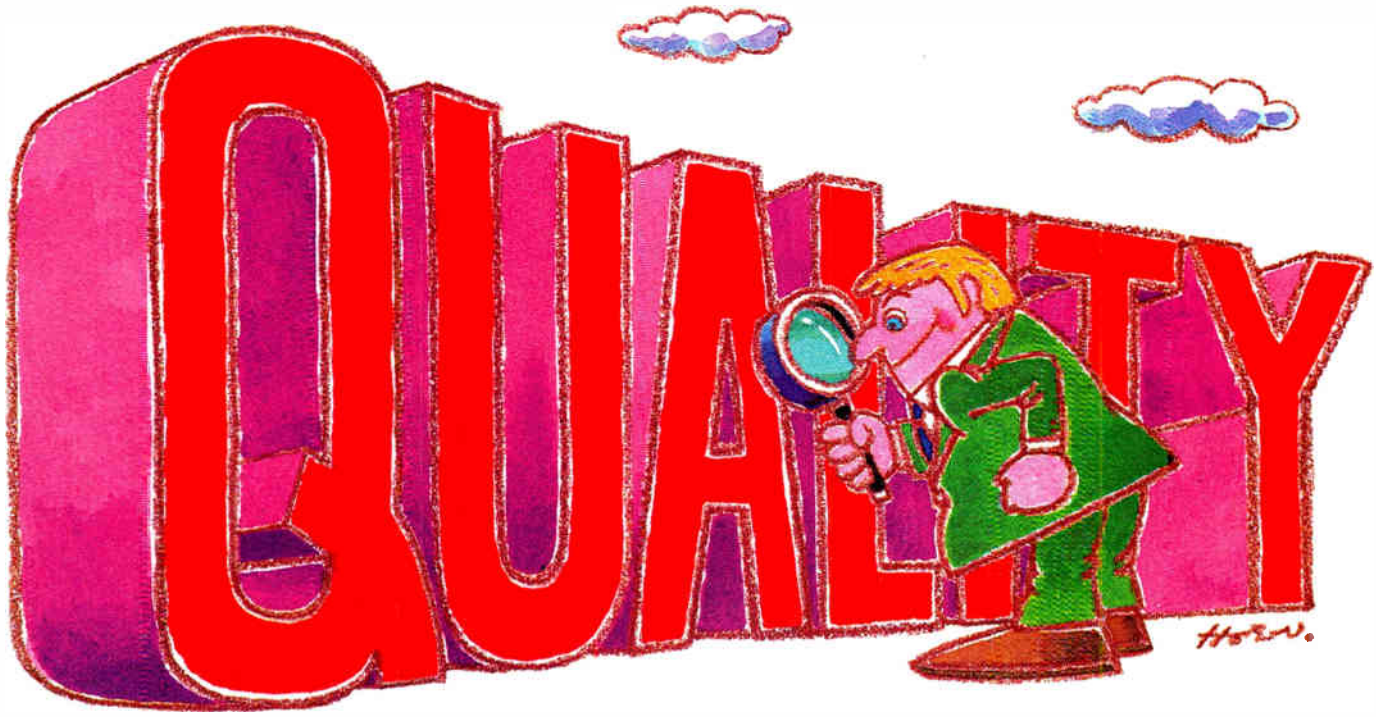

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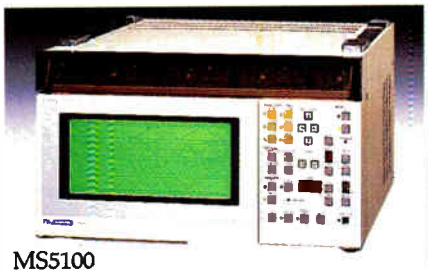
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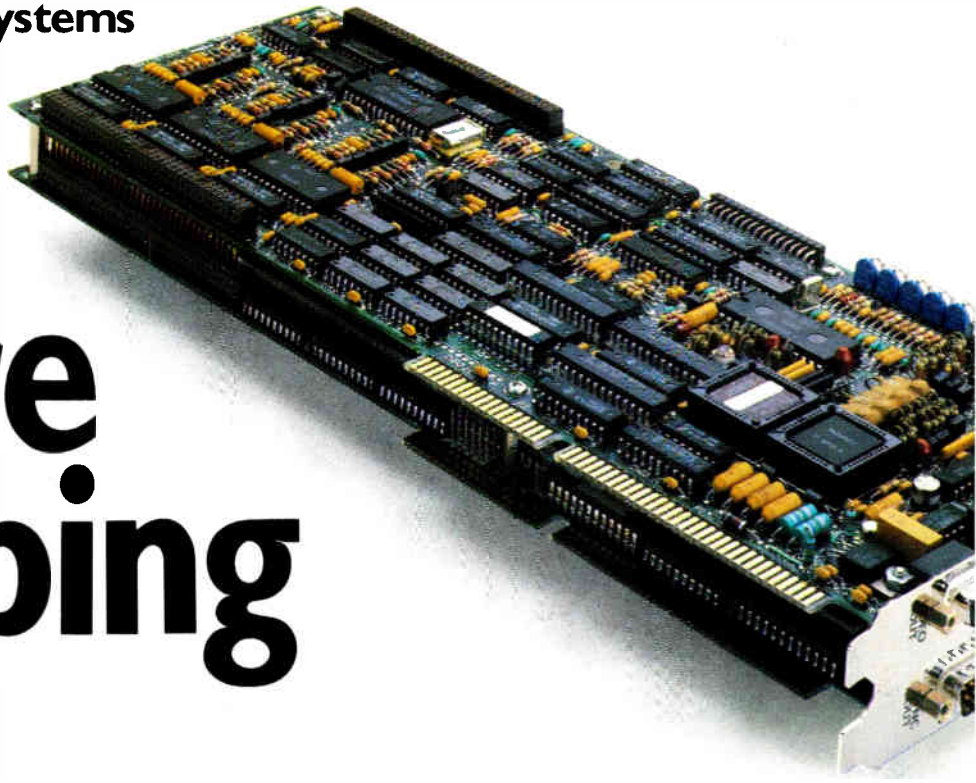

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