HOW LINEAR IC DESIGNERS ARE BUILDING DENSER CHIPS/67

EXECUTIVE OUTLOOK: NO SLOWDOWN IN TECHNOLOGY/86

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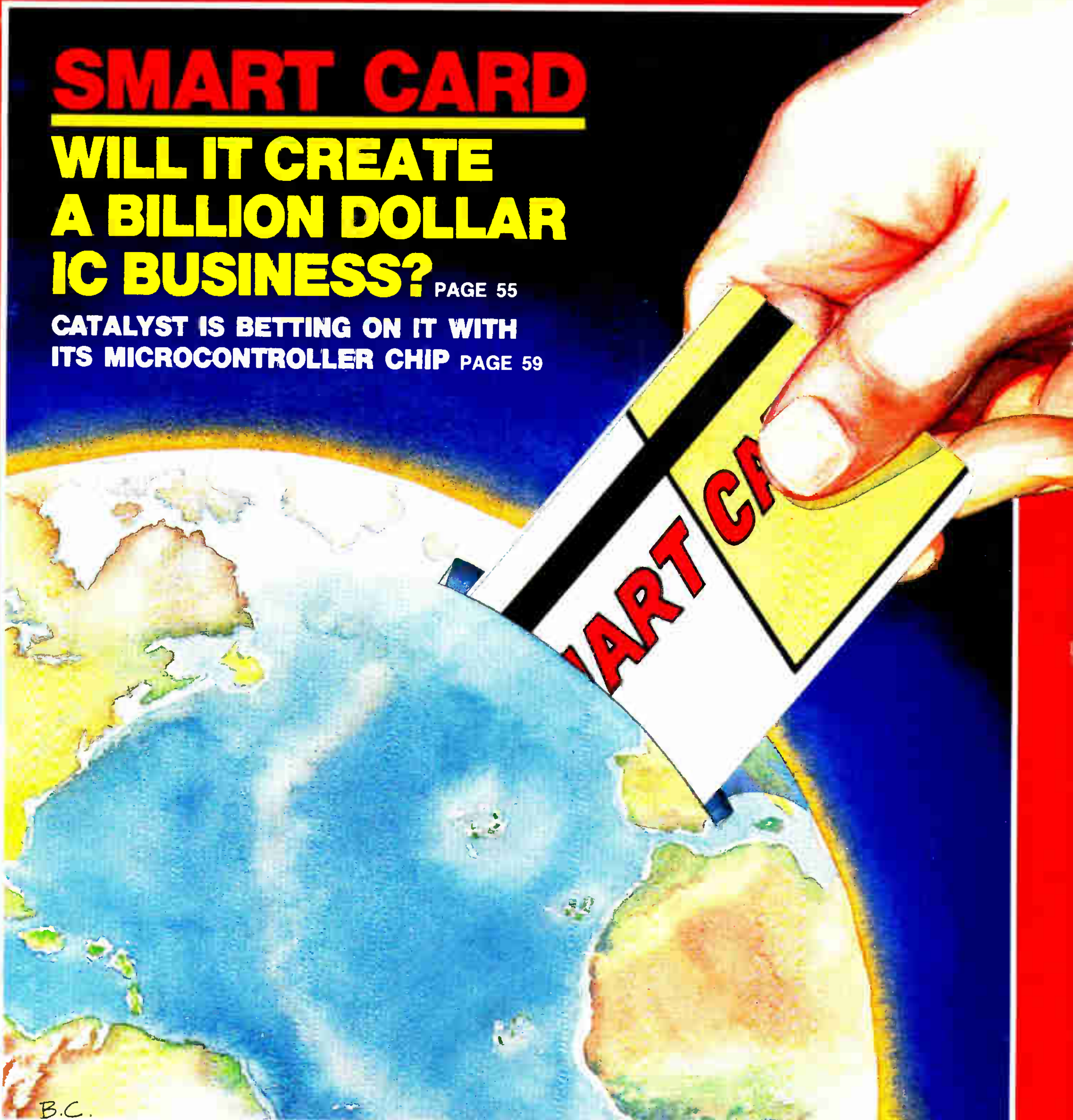

SMART CARD

WILL IT CREATE A BILLION DOLLAR IC BUSINESS? PAGE 55

CATALYST IS BETTING ON IT WITH ITS MICROCONTROLLER CHIP PAGE 59

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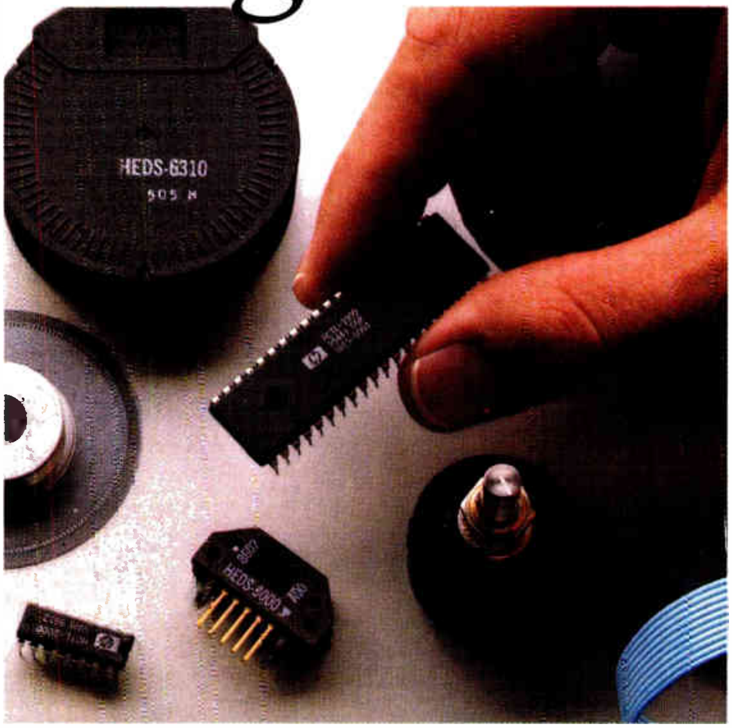

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Electronics

For the January 3, 1972, issue, *Electronics* editors decided to ask industry leaders to list their business concerns for the coming year. The idea was to give our readers what we called an Executive Outlook, a preview of the rough spots and the bright spots just down the road.

YOUNG. The leader of the team that took the industry's pulse.

The idea was a good one, and the result has been an outstanding series that can serve as a prototype of the kind of innovative and authoritative coverage that is our hallmark. The 15th Executive Outlook starts on p. 86, and there are several major contrasts between it and the first edition. For one, the story that appeared on Jan. 3, 1972, was five pages long; the one in this issue spans 10 pages. Also, the first Executive Outlook concerned U. S. companies only; now this roundup encompasses business around the world.

"But perhaps the most significant difference this year is the organization of the story," says assistant managing editor Jeremy Young, who directed the coverage. "We have divided it into two parts: one for the executives and the other for the research and engineering managers. With that format, we have been able to get more specific with our questions. For example, one of the chief concerns for the executives is the new tax law and how it affects their companies. On the other hand, the technologists are more concerned about bottlenecks in the lab-to-market process."

The one thing that hasn't changed is that it takes many people to produce the story. All the editors in our domestic and overseas bureaus interviewed the leaders whose views we present. In New York, those interviews were compiled by Young along with New York bureau manager Tobias Naegele and chief copy editor Larry King. "We quote about 60 people in the story," says Young. "Keeping all the names and reporting straight is a complicated business."

Some universal worries have persisted over the years. In 1972 the article said, "Three major problems emerged: an inability to compete with Japan on an equal footing, loss of momentum of the country's technological leadership; and doubt about the Nixon administration's game plan.

"On the plus side, conditions seem ripe for recovery—perhaps slow at first, but building to a substantial pace by the second half." One executive is quoted as saying, "By the second half we'll be running to catch up, which is a pleasant predicament compared to the last two years." That's a predicament that would be doubly welcome in 1987.

Overall, the mood of the executives was described as "cautiously optimistic." Sound familiar?

Laurence Altman

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Electronics

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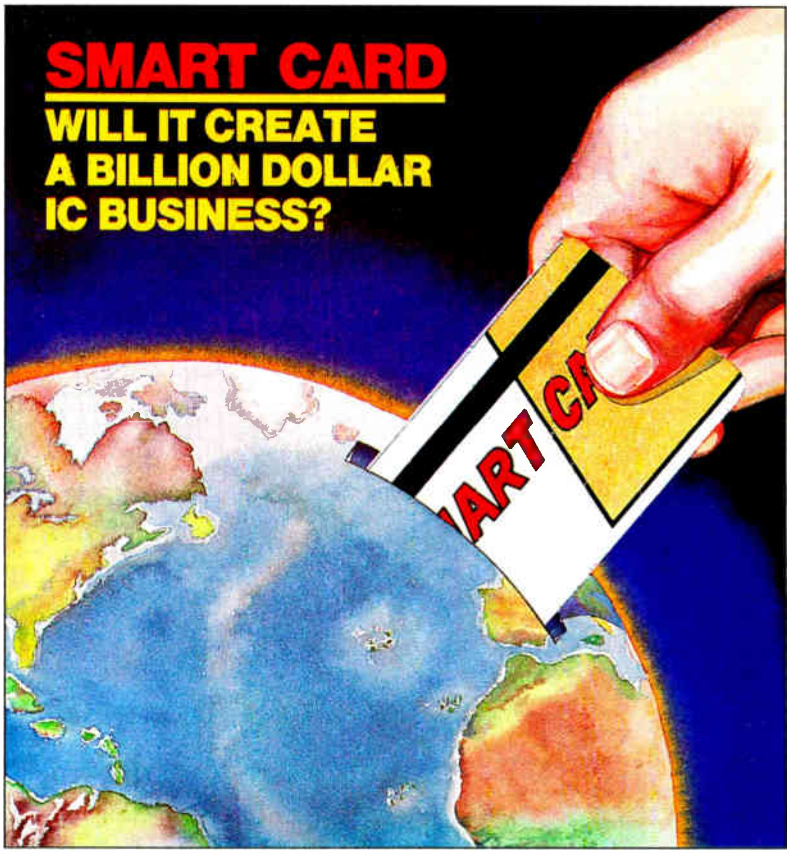

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IMS1423M (x4)	CMOS	35, 45, 55ns

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IMS1630M (x8)*	45, 55, 70ns

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Circle 7 on reader service card

One good reason why we're the only magazine doing our own market forecast: It's hard to do. Next month will mark 30 years of running this authoritative feature

Here's a question: What is it that industry managers criticize or make sport of, yet can never get enough of when they're on the hook to develop a budget or product plan? Hint: Only one magazine is smart (dumb?) enough to tackle this impossible job for the electronics industry.

If you still can't guess the answer, grab the next issue of *Electronics*, which will hit the streets on Jan. 8, 1987. You'll see the latest installment of an innovation by this magazine that has become an unequaled classic: our annual market report. Our first 1987 issue will feature 24 jam-packed pages of data on U. S. markets, which as nearly as we can figure out will mark 30 years of running this authoritative feature.

There's a mighty good reason why we're the only magazine turning out our own forecast: It's darn hard to do. The data this year came from more than 500 companies as well as from several market researchers. We came up with the forecasts with the help of a computerized data-analysis system linked to our own electronic publishing system.

But we still have problems. Two of the biggest are getting little or no market data on a product category and the wide disparity in some estimates that companies give us. Major cause for these wide swings are misconceptions of what a category covers, says Art Erikson, executive news editor. Art, who spent November reporting in Europe for our Jan. 22 overseas market report, says: "I was once asked by a market statistician of a major British trade association whether we listed phonograph records as hardware or software." Needless to say, his association's data came in for extra scrutiny.

There always seems to be too many figures in one area and not enough in another, laments Howard Wolff, associate managing editor. Judging from the questionnaires, everyone in Japan has an insight into the pot and trimmer market, but not too many are willing or able to estimate the 1987 sales of satellite earth stations. Also, unfortunately for us, for every respondent like the Japanese marketer who completed his five-page questionnaire with every line on every page filled in, there are another half dozen others who toss our questionnaire in the round file. But we are quick to press on when we realize that our calculations are going to be read and probably used by more than a half million people.

ROBERT W. HENKEL

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NEW 32-BIT CMOS MICROPROCESSORS.

The two new members of NEC's CMOS microprocessor V-Series bring unprecedented density and performance in the 32-bit realm. The V60 and V70 supermicros are the first to integrate a Memory Management Unit and basic floating-point processing functions on a single chip.

The V60 has a 16-bit external data bus for an easy, affordable path into 32-bit products while the V70 is a full 32-bit engine designed to power leading-edge systems.

The super-fast V60 and V70 offer a clock speed of 16MHz, and execute 3.5 MIPS and 6 MIPS respectively. A six-stage pipelined CPU enables concurrent execution of up to 4 instructions. With 32 on-board 32-bit general-purpose registers, there is no need to access slow off-chip memory.

The V60/V70 feature an on-chip memory management unit with 4 gigabytes of demand-paged virtual memory space, and 4 levels of memory protection for multi-tasking and multi-user environments.

The V60/V70 instruction set is ideal for high-level languages and OS support (UNIX™ V and proprietary realtime OS). There are 21 addressing modes, 273 instructions, and an emulation mode for 16-bit V20/V30 software.

UNIX: trademark of AT&T Bell Laboratories.

C&C
Computers and Communications

NUMBER 136

COMING SOON: 1.3/1.55μ DFB LASER DIODES.

Dispersion has always been a major obstacle in long-distance, high-speed lightwave communications. With conventional laser diodes emitting multiple spectrums, pulses deteriorate by dispersion after long travel through the fiber. This in turn limits repeater span to 20–30km and capacity to 400–560Mbps for the prevalent 1.3μ fiber optic systems.

NEC has overcome this obstacle with newly-developed distributed feedback (DFB) laser diodes for 1.3μ and 1.55μ fiber optic transmission systems. They feature a stable single longitudinal mode operation, high efficiency and high output power. The new DFB laser diodes are expected to expand repeater span to 80–100km for 1.3μ system or 100–200km for 1.55μ system.

NEC's new DFB laser diodes inherit the renowned double channel planar-buried heterostructure (DC-PBH) and have a diffraction grating in the optical guide region to produce a single wavelength. Output powers are rated 8mw for the 1.3μ NDL5600 and 5mw for the 1.55μ NDL5650. They come in the TO-5 package with an integral monitor photo diode or chip-on-carrier configurations.

As matching light-receiving devices, NEC has planar type InGaAs avalanche photo diodes. They have a selective guard ring construction to achieve high sensitivity and excellent reliability.

NEW INTELLIGENT BUILDING COMPLEX AT VANCOUVER.

The intelligent building is an idea whose time has come. As the perfect nestling for office workers in the Information Age, it centers on an advanced information management system which provides simultaneous voice, data and image services to tenants at less cost while it controls the entire building environment efficiently.

The World Trade Centre/Pan-Pacific Vancouver Hotel recently opened is just such an installation. NEC's NEAX 2400 Information Management System (IMS) allows tenants to utilize enhanced telephone/facsimile services including least-cost routing, message center and voice mail services, and computer terminal connection via a multifunction digital telephone set. The NEAX 2400 IMS also offers sophisticated services to hotel guests.

NEC's Intelligent Building Systems, based on our unique C&C (integrated computer and communications) technology, are the most advanced and comprehensive available today. As the core of this system, the modular NEAX 2400 IMS can expand to 255 tenant partitions. It supports more than a hundred advanced features including a protocol converter to allow communication with most popular host computers.

NEC also supplies comprehensive component equipment including multifunction digital telephones, information display pagers, high-speed facsimiles, business and personal computers, teleconferencing and CATV equipment and local distribution microwave links.

NEC's comprehensive systems breathe new life into the smart building concept, bringing costly services like teleconferencing within the reach of every business.

NEW HIGH-CAPACITY 64QAM DMR SERIES.

NEC's newest 800 Series high-capacity digital microwave radio (DMR) systems transmit two or three DS3 signals per RF carrier, utilizing 64-state quadrature amplitude modulation (64QAM) for effective use of radio spectrum.

Three systems meeting FCC standards are available: a 4GHz 90M-bit system providing 1,344 voice channels, and 6GHz and 11GHz 135M-bit systems for 2,016 voice channels.

The new systems incorporate the latest LSIs, hybrid and microwave ICs throughout to achieve compact design, lower power consumption and improved system reliability. Housed in a standard 19-inch rack, they require minimal cabling work for installation.

The advanced 800 Series is fully compatible with Bell's facility maintenance and administration system.

NEC

LETTERS

Age discrimination?

To the Editor: The comment that Wayne Ponik "declines to state his age" in "Ostertag gets his kicks dealing with picoseconds" [*Electronics*, Nov. 13, 1986, p. 74] makes Wayne come off a bit heavy, when in fact his age is no more relevant than his hat size or his religion. It is suprising, especially in light of recent heightened sensitivity to age, sex, and race discrimination, that *Electronics* still finds it necessary to pin an age on everybody, or to call attention to him when he refuses to give it.

Frederick Van Veen
Vice President
Teradyne Inc.
Boston, Mass.

Just in time for a bargain

To the editor: The recent article on a very accurate $20,000 West German clock [*Electronics*, Oct. 30, 1986, p. 38] was interesting and informative. Your readers might be interested in an American-made clock with similar accuracy, more utility, and a $450 price tag. Precision Standard Time's OEM-10 radio-controlled clock provides accurate, reliable, and National Bureau of Standards-traceable time by receiving and decoding the transmissions from the NBS radio stations WWV in Colorado and WWVH in Hawaii. The clock can be controlled by a computer system over an RS-232-C port and hooked up to an optional digital display.

Rex A. Brown
Vice President, Marketing
Precision Standard Time Inc.
Santa Clara, Calif.

Ottawa was our Waterloo

To the Editor: As a faithful reader of *Electronics* since my years at the University of Waterloo, I was shocked to find in "How Jacob got into analog simulation" [*Electronics*, Oct. 30, 1986, p. 82] that the University of Waterloo is in Ottawa! I reckon I was a bit angered because I am a Waterloo graduate. For your information, the University of Waterloo is in Waterloo, Ontario.

Calvin Chang
Computing Facilities Associate
Facilities Provisioning
Toronto, Ont.

That's Schottky!

Correction: The detector portion of the Honeywell Inc. GaAs optoelectronic receiver chip discussed in "GaAs Opto IC gets up to 200 gates" [*Electronics*, Nov. 13, p. 31] was built by fabricating interdigitated Schottky contacts—not by using ion implantation, as was reported. The MES FETs on the device were built using ion implantation.

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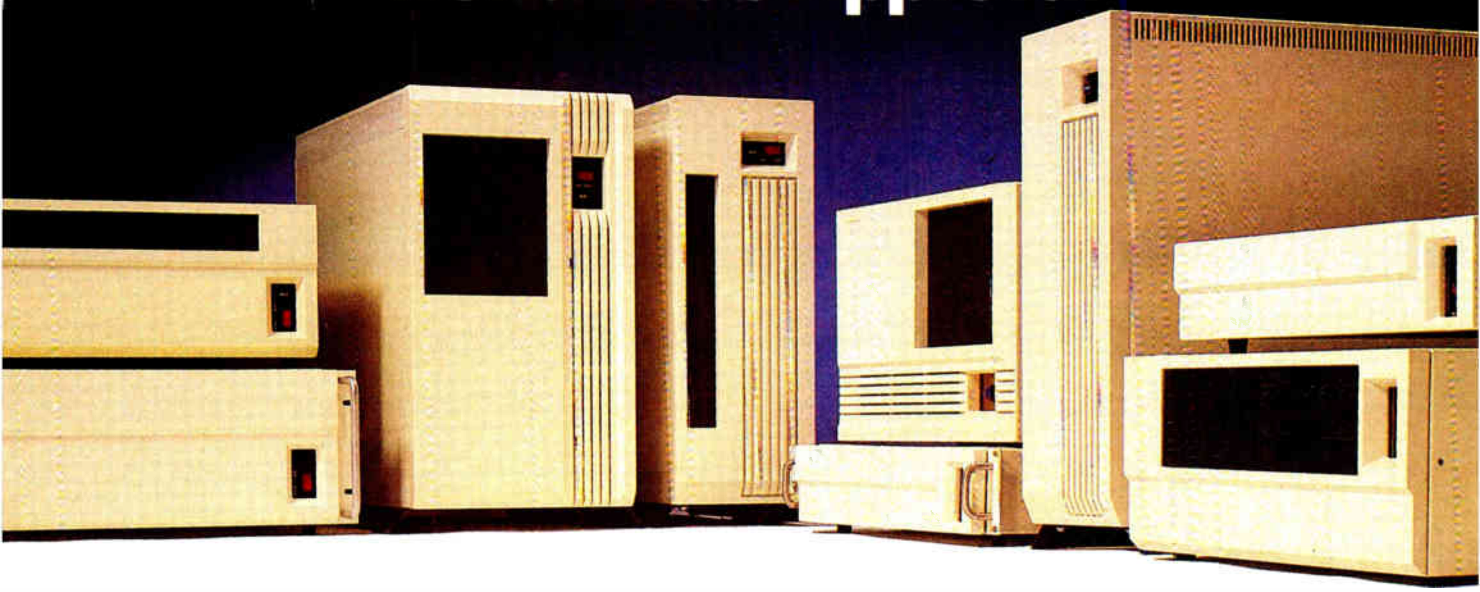

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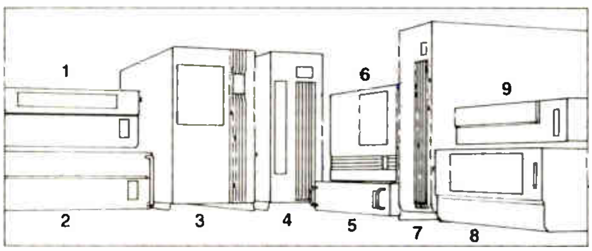

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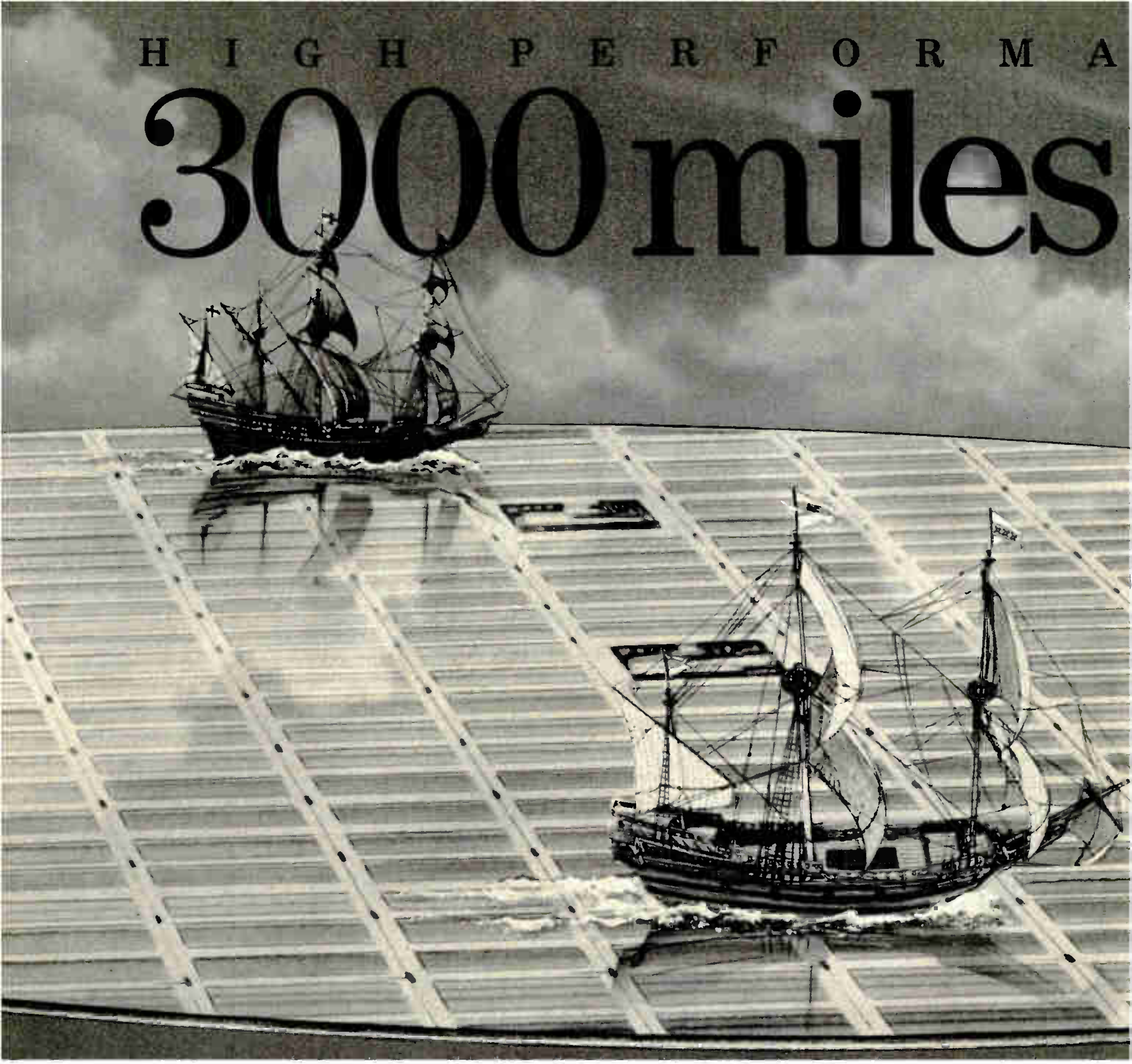

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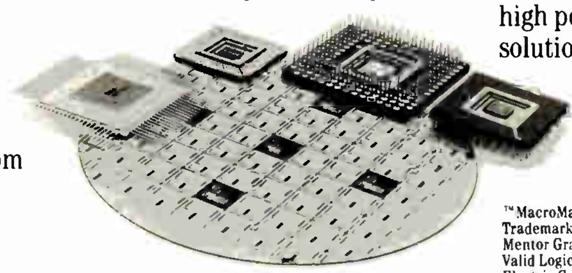

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PEOPLE

HOW THE LASER DISK IS RESHAPING ONE CAREER

As the producer, writer, and host of 65 half-hour television shows on consumer health for Westinghouse Broadcasting, and a communications consultant for Twentieth Century Fox and Viacom, Jim Mason seemed destined for a career in television. But with a degree in public health from the Yale School of Medicine and teaching experience at Boston University Medical School, Mason also had the qualifications for a future in academia.

So he went into electronics.

It started three years ago, says the 38-year-old Boston native, when he became interested in interactive laser-disk technology and was struck by its potential, especially with its promise as a cost-effective educational tool. After spending a year of what he calls "tracking the technology," Mason believed he had found a way to improve what he saw as a longstanding problem—the inability of industry to effectively communicate health-care information, especially in training employees about hazards on the job.

MASON: Marrying TV's qualities and the computer's power.

The result: Interactive Medical Communications, a company Mason founded in 1984 to meet the training needs of American industry. Earlier this year, the Boston-based company completed a contract with General Motors Corp. to train more than 400,000 employees in 147 locations across the country.

The medium will be interactive laser-disk systems, or ILDS, which are fast becoming a hot educational item. Comparing the ILDS with the much-heralded but ill-fated computer-aided instruction, Mason sees interactive laser disks as a revolutionary advance, because the systems are like television sets rather than computers.

"CAI provides a rather impersonal approach to learning—it's you and your computer. [With ILDS] we use live-action footage and create a highly engaging and entertaining TV program. We're drawing upon the emotional and visual power of TV and marrying it to the speed and power of the computer."

In the General Motors program, workers are trained to understand the hazards in the workplace by using a touchscreen to answer questions as they watch slickly produced training videos. The system keeps track of each worker's progress, recording the information that gives an employee trouble and generating a review program. Since employees are trained individually, they work at their own pace and are not intimidated when they don't understand course material.

Such versatility has not been lost on IBM Corp. This fall it threw its hat into the ILDS ring, introducing a system designed to help reduce adult illiteracy and claiming very positive test results.

Mason maintains that ILDS effectively trains employees in an average of one third less time than the conventional training methods, such as classroom audio-visual presentations. "Interactive laser-disk training has become the only practical way to make sure employees understand and retain vital information, which in turn they can apply in the workplace."

A system from Interactive Medical Communications consists of a color touchscreen monitor, a microcomputer with 640-K of random-access memory and a 20-Mb hard disk, and a laser-disk player. Branching software is used to create programs that adapt to an individual's progress. In a typical 30-minute disk, a worker will make 40 to 80 decisions that can result in a tremendous number of paths—there are on the order of 10^6.

Producing an effective laser-disk program is a team effort, says Mason. In addition to content and software expertise, good production values are essential to the program's credibility. "People aren't going to believe a visual image that is not similar to TV," says Mason. A single disk for the General Motors training program took eight months to develop.

Although working with health-oriented material is his company's strong point, Mason says IMC has now developed proprietary tools that will enable it to branch out in areas such as engineering management and other industry-specific applications. Eventually, Mason sees ILDS as reaching even the home market. Claims Mason: "Because it is responsive and identifies the unique needs of each learner, ILDS can be used for virtually any kind of instructional program." *–Rick Elliot*

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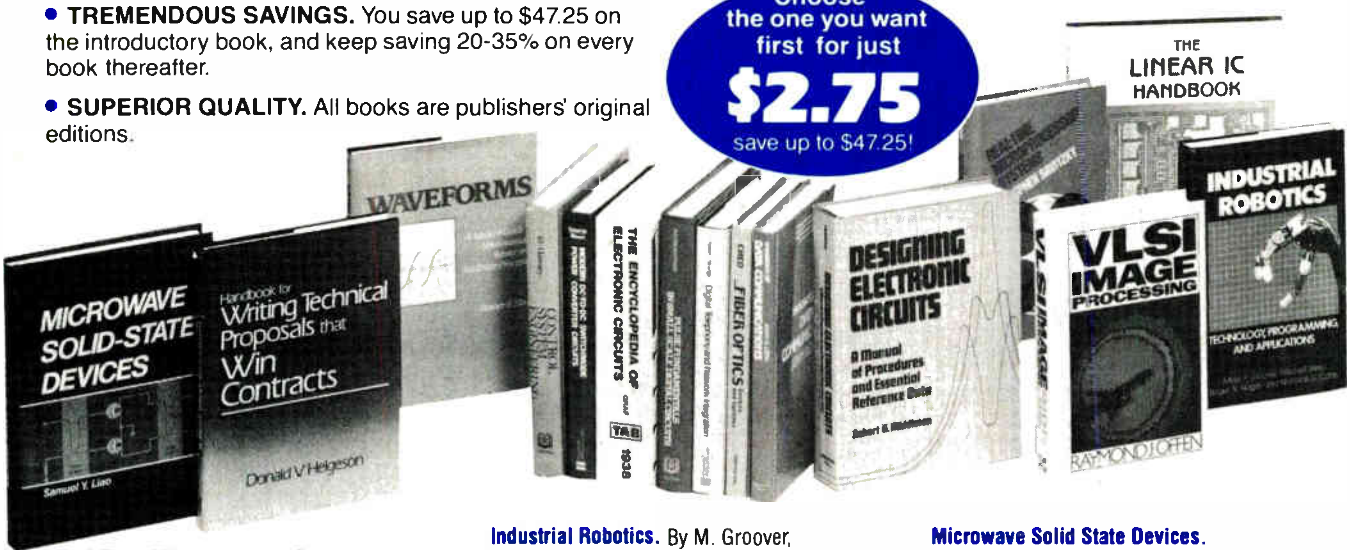

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ELECTRONICS NEWSLETTER

HONEYWELL DROPS PRODUCT EFFORTS IN COMMERCIAL DIGITAL GaAs

Honeywell Inc. is phasing out commercial-product efforts in the slowly developing market for digital gallium arsenide ICs. The GaAs-IC product line fell victim to corporate cost-cutting measures announced by Honeywell in September—in fact, company officials confirm that they are reviewing efforts in the merchant silicon market as well. With the GaAs move, Honeywell's new GaAs production facility in Richardson, Texas, will be converted to support an expanding thrust into silicon solid-state sensors, after existing contracts for Honeywell's GaAs gate arrays and custom ICs are completed. Honeywell officials add that GaAs research and government work will be consolidated at the company's Physical Sciences Center in Bloomington, Minn. ☐

IBM STEPS UP ITS COMMITMENT TO SUPERCOMPUTERS

IBM Corp. appears to be punching up its drive to develop supercomputers. That's how industry watchers interpret the creation last week of a new post in IBM's Data Systems Division—the White Plains, N. Y., division that manufactures IBM's 3090 series of large processors. The job, which carries the title of vice president for engineering and scientific computing, will be filled by Irving Wladawsky-Berger, now the division's vice president of development; he earlier served as vice president of systems and director of computer sciences in IBM's Research Division. He will have worldwide responsibility for the strategy, development, and technical support of IBM's supercomputer. Another indication of the stronger commitment to supercomputers is a realignment of operations in what IBM calls "numerically intensive computing" and everyone else calls "supercomputing." As part of the realignment, the Information Systems Group, which is the marketing and service arm of the company, will establish new centers at IBM's facility in Kingston, N. Y., and at its Palo Alto, Calif., Scientific Center to explore advanced technology, develop applications, offer customer support, and sponsor research at colleges. ☐

U. S. TO PROBE JAPAN'S SUPERCOMPUTER BARRIERS

Determined not to lose America's leadership position in supercomputer technology, the federal government is launching a three-month investigation into Japanese trade practices that have excluded U. S. makers from the Japanese market. "If Japan is targeting the supercomputer industry for dominance—as it has other industries—we have to study how that will affect the U. S. economy and national security," says a spokesman from the U. S. Trade Representative's office, which will conduct the investigation. The U. S. dominates the worldwide market, with 86% of the 168 supercomputers in operation. But in Japan, only 6 of 26 supercomputers are U. S.-made. ☐

GE TECHNIQUE FOR VERTICAL VIA HOLES PROMISES DENSER VLSI

An enhanced chemical-vapor-deposition technique for metallizing vias promises denser very large-scale integrated circuits. The selective CVD tungsten technique developed by General Electric Co. permits the use of vertical via holes, which require two to five times less real estate than the tapered vias used in conventional circuitry. GE has licensed Genus Inc., Mountain View, Calif., to build equipment for the double-layer-metal process. The GE Research and Development Center in Schenectady, N. Y., already has prototypes of the CVD machine and has used them in tests for a new family of 1.2-μm gate arrays. GE says yields are better than 95%—high enough to make the company consider adapting its current 1.2-μm VLSI technology to the new approach. If it does, production chips would emerge in late 1987. ☐

ELECTRONICS NEWSLETTER

THE PENTAGON PUSHES AN INDUSTRY TECHNOLOGY CONSORTIUM...

The Defense Department, worried about being cut off from leading-edge memory technology, has taken the initiative from industry with a plan to improve commercial semiconductor-manufacturing technology through a federally supported consortium. A Defense Science Board task force is finishing a report, to be submitted next month, that is said to recommend $1.25 billion in funding, which will be spent over a five-year period, for an industry consortium to develop the technology and the equipment to build advanced dynamic random-access memories. The proposed consortium is considered a good bet for Pentagon approval, and could begin operation next year if the Defense Department can find the funds. □

...AND THE SIA SEEKS TO FORM A MANUFACTURING CO-OP

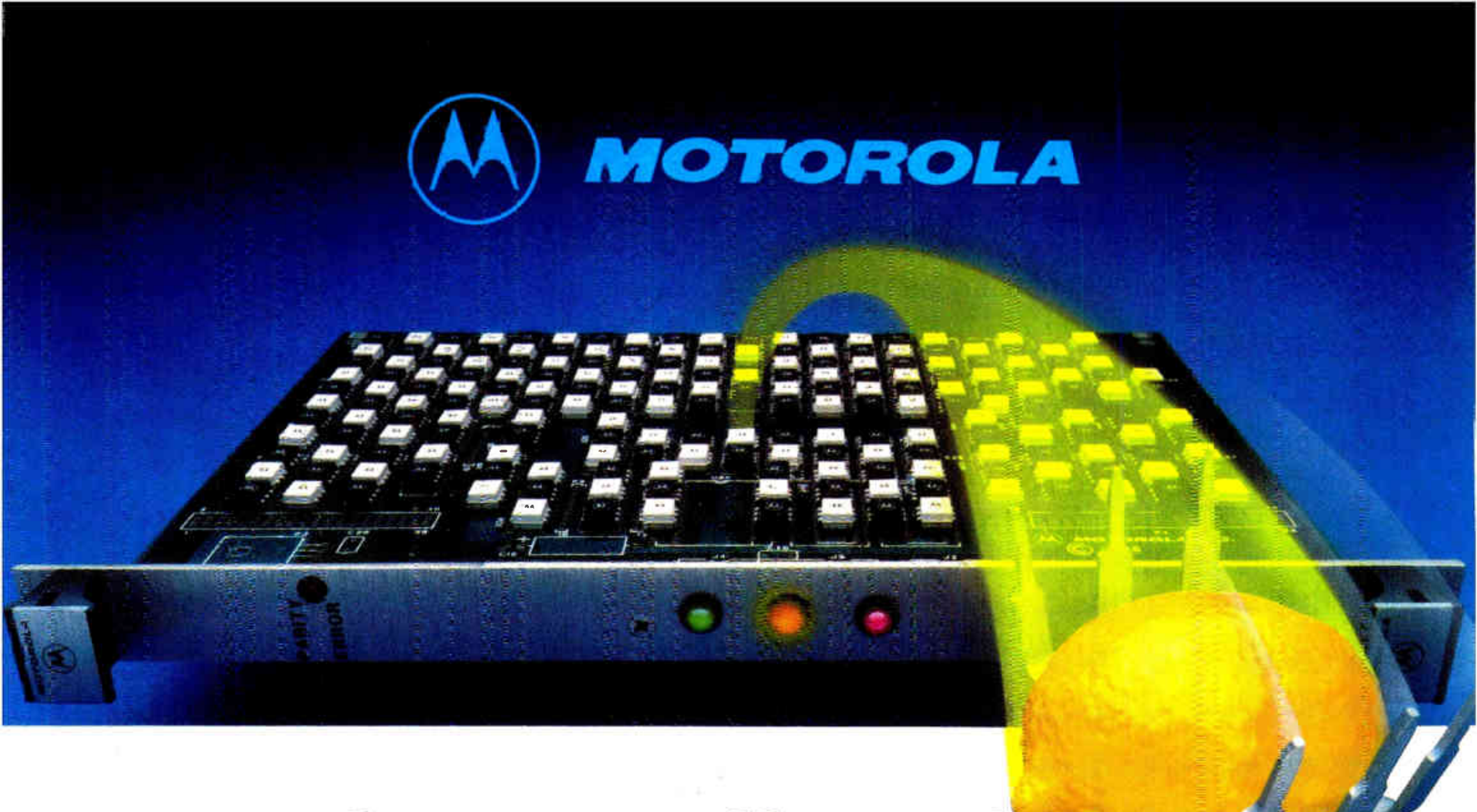
Apparently lagging behind the Pentagon task force is a Semiconductor Industry Association steering committee that's exploring ways to get federal money for a manufacturing cooperative. Nicknamed Sematech, the co-op would develop dynamic random-access memories as a manufacturing and technology driver. The SIA panel will not report until March. Fears that the DOD plan would swallow up the Sematech effort were discounted by Charles E. Sporck, president of National Semiconductor Corp. and head of the Sematech committee. "Sematech is still under development, and is not linked to the Defense Department." Adds Larry Sumney, president of the industry cooperative, Semiconductor Research Corp., "Everyone feels that something significant will have to be done, on a cooperative basis; I don't think everyone agrees on what that something should be." He says the science board's plan and Sematech were conceptually similar, "but details on each side will be different because the different interests involved aren't identified yet." □

INTEL AND AT&T SIGN A DEAL TO COOPERATE ON ISDN

Intel Corp. and AT&T Co. have signed a cooperative agreement to verify the interoperability of their integrated services digital network (ISDN) chip sets, beginning with the companies' 4-wire transceivers. AT&T is embracing an open-systems strategy for ISDN in an attempt to speed ISDN to commercial reality, and the company is betting that signing with the Santa Clara, Calif., chip maker will help cement it in a leadership role. For its part, Intel hopes the deal can strengthen its position as an ISDN chip supplier. The accord holds great promise for future developments between the two companies—the two are discussing more such deals—and AT&T says it has not ruled out similar agreements with other companies. □

SIA CHANGES SAMPLE TO GET MORE ACCURATE BOOK/BILL FIGURES

The Semiconductor Industry Association is revising the sample from which it calculates the preliminary book/bill figures released at about the middle of each month because its findings were revised upward eight times during 1986. CMOS and semicustom sales, which have accounted for a greater share of market and have caused swings of as much as 5% in estimated and actual bookings, were added to the sample, the SIA says. Using the new sample, which is supposed to include at least 40% of the U. S. market, the SIA estimates three-month average bookings for November at $720.1 million and average billings at $723.8 million, for a book/bill ratio of 0.99. It is the second month in a row that the closely watched index has risen. SIA statistician Douglas Andrey attributes the increase to continued slow growth in end-user markets and the long-awaited withering of inflated inventories at original-equipment manufacturers. □



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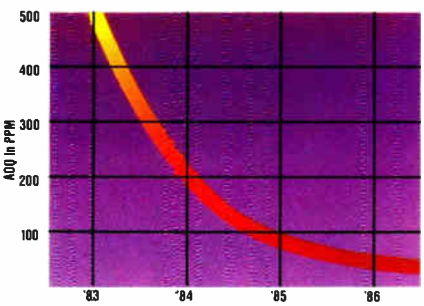

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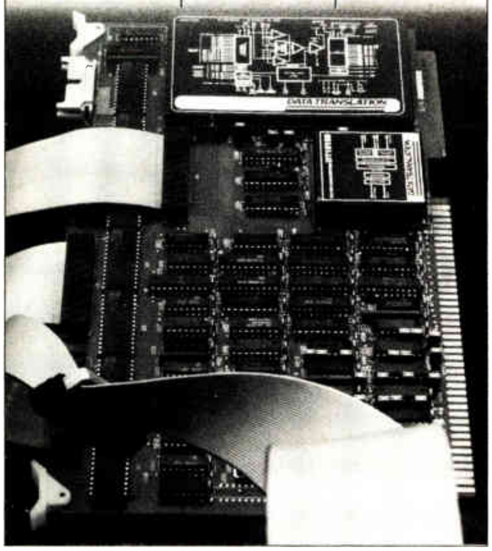
DT714	Low Level A/D	64DI
DT714 + DT715	Low Level A/D Expanded	256DI



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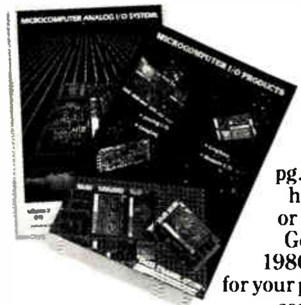

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PRODUCTS NEWSLETTER

LCD-CONTROLLER CHIP COULD CUT COST AND SIZE OF LAPTOP COMPUTERS

Portable and laptop computer manufacturers looking to cut costs and the size of their products will want to take a look at Hitachi America Ltd.'s new liquid-crystal-display controller chip. The company says that its new CMOS chip, which replaces 30 separate n-MOS devices, will reduce controller-board space by 40% to 50% and costs by 40%. The monolithic device will enhance system reliability and reduce controller power requirements, the San Jose, Calif., company says. Compatible with industry-standard software, it can control screen sizes up to 1,024 by 2,048 dots—high resolution for laptops. The HD63645 is for Motorola Corp. microprocessors; the HD64645 version interfaces Intel Corp. products. Samples will be available early in January, and production will start later in the first quarter of 1987. In 10,000-piece quantities, the chips will cost $7.10 each. □

DAISY CAD TOOL TACKLES MIXED ANALOG-DIGITAL SIMULATION

Daisy Systems Corp. is tackling a nagging shortcoming of computer-aided design: simulating the behavior of combination analog-digital circuits. The Mountain View, Calif., company's A-D Lab tool combines Daisy's D-Spice analog simulator and DLS digital simulator through a common interface and data base. Users interactively simulate combination circuits by driving the simulation of each stage with the previous stage. The tool takes into account component technologies, loading, and drives to achieve an exact translation between analog and digital signals. The software will be available later this month on the company's Logician work station and in February on the IBM Personal Computer AT and compatible work stations. The software for the Logician sells for $5,000. □

IBM MAINFRAMES TO GET AI-BASED PERFORMANCE MANAGEMENT

DASD Advisor, the first in a series of artificial-intelligence products that will help manage the performance of IBM Corp. mainframes, is due next spring from Boole & Babbage Inc. of Sunnyvale, Calif. DASD Advisor interprets data from B&B's DASD (for Direct-Access Storage-Device) Response Manager, a set of programs for gathering and monitoring data on storage-device workloads, and then makes suggestions for load balancing to optimize the use of large systems. Based on AI tools developed at the Aion Corp., Palo Alto, Calif., the Advisor series will consist of extensions to B&B's current products and will be implemented across the entire product line. The DASD Advisor came first because IBM studies show that input/output operations on large disk-drive systems account for 70% of response-time problems and 50% of system costs. Prices for the packages are expected to range between $10,000 and $30,000. □

MOTOROLA CUTS PRICES OF ITS FAST CMOS SRAMs BY UP TO 39%

Motorola Inc. is slashing prices on its fast, 1.5-μm double-metal, double-polysilicon CMOS static random-access memories by as much as 39%. According to Motorola memory executives in Austin, Texas, intense competition among makers of fast SRAMs [*Electronics*, Aug. 7, 1986, p. 121] was a factor, but the higher yields the company is getting keep the line profitable at the lower prices. The deepest percentage cut is in the price of the 25-ns, 4-K-by-4-bit MCM6268P25 SRAM, which now sells for $8.40 each in plastic DIPs—down from $13.65—in 500-piece quantities. Prices for a half dozen types of 64-K SRAMs with access speeds of 25 and 35 ns are being trimmed by 10% to 17%. For instance, the 64-K-by-1-bit MCM6287L25 in a ceramic package is now $42.90 each, down from $50.70. □

PRODUCTS NEWSLETTER

ETA SYSTEMS' FIRST SUPERCOMPUTER RUNS AT 3.5 GIGAFLOPS

ETA Systems Inc. will start shipping its first product, the E-Series ETA^{10} supercomputer, this month or in January. The multiprocessor system will run 20% to 25% below expectations, at 0.8 billion to 3.5 billion floating-point operations/s, but that still tops the fastest Cray supercomputer, which runs at 1.2 gigaflops. Moreover, later in 1987, the St. Paul, Minn., company plans to field another series it says will perform up to expectations. The E Series comes with from one to four central processing units, each equipped with 32 megabytes of local memory and from 256 megabytes to 2 gigabytes of shared memory. Prices range from about $6 million to $12 million. Higher performance will arrive late next year with the G Series, incorporating faster versions of the 20,000-gate CMOS arrays that are the heart of both systems. The G Series will cost about $25 million for an eight-processor system that should hit the 10-gigaflops peak speed for which the ETA^{10} was named. ETA split the project into two series when it encountered problems with the gate arrays [*Electronics*, July 24, 1986, p. 21]. □

DATA TRANSLATION'S BOARD BOOSTS A-D THROUGHPUT ON PCs

Data Translation Inc.'s latest data-acquisition board doubles the analog-to-digital conversion rate of its industry-leading boards for the Compaq 386 PC and offers similar improved performance for many other personal computers. The Marlboro, Mass., company claims its DT 2821-G will support throughput at 250 KHz on the Compaq and rates in the 180-to-235-KHz range for the IBM Personal Computer AT and compatibles, depending on clock speed. The single-board system has 12-bit resolution for 16 single-ended or 8 differential analog inputs. It uses a proprietary direct-memory-access technique for uninterrupted data acquisition. On-board hardware includes two 12-bit analog-to-digital converters and a channel-gain inventory list stored in RAM for a-d sampling control. Targeted for use in high-speed data-acquisition and analytical applications, the 2821-G is available now for $2,995. □

APPLITEK SIMPLIFIES LAN FOR SPERRY OR BURROUGHS COMPUTERS

Applitek Corp. is making Burroughs and Sperry local-area networks from Unisys Corp. more flexible. One version of its NI10/G gateway allows Burroughs host computers to communicate with asynchronous terminals such as Digital Equipment Corp. VT100s as well as with Burroughs MT983 terminals. A similar gateway will link Sperry hosts using Univac VTS20 terminals and asynchronous terminals. The Wakefield, Mass., company's LAN gateways, priced at $11,700, allow hundreds of terminals to communicate at distances of up to 20 miles. The gateways accommodate baseband, broadband, or fiber-optic cable. □

QRONOS SOFTWARE TAKES BIG STEP TOWARD OPEN ARCHITECTURE FOR CIM

A big step toward an open architecture for computer-integrated manufacturing is coming from Qronos Technology Inc. Developed with IBM Corp., Production Master runs on the IBM System/88 computer but lets other CIM systems access its decision-support programs. The Cupertino, Calif., company's software also is truly generic, because it works for any industry using batch and continuous-process manufacturing techniques. Production Master's programs include those for inventory, engineering data, and resource management. The product also handles security and on-line help, and it has a structure system for defining physical plant, operations, and other production-oriented variables. Prices will start at $300,000 when the software becomes available in March. □

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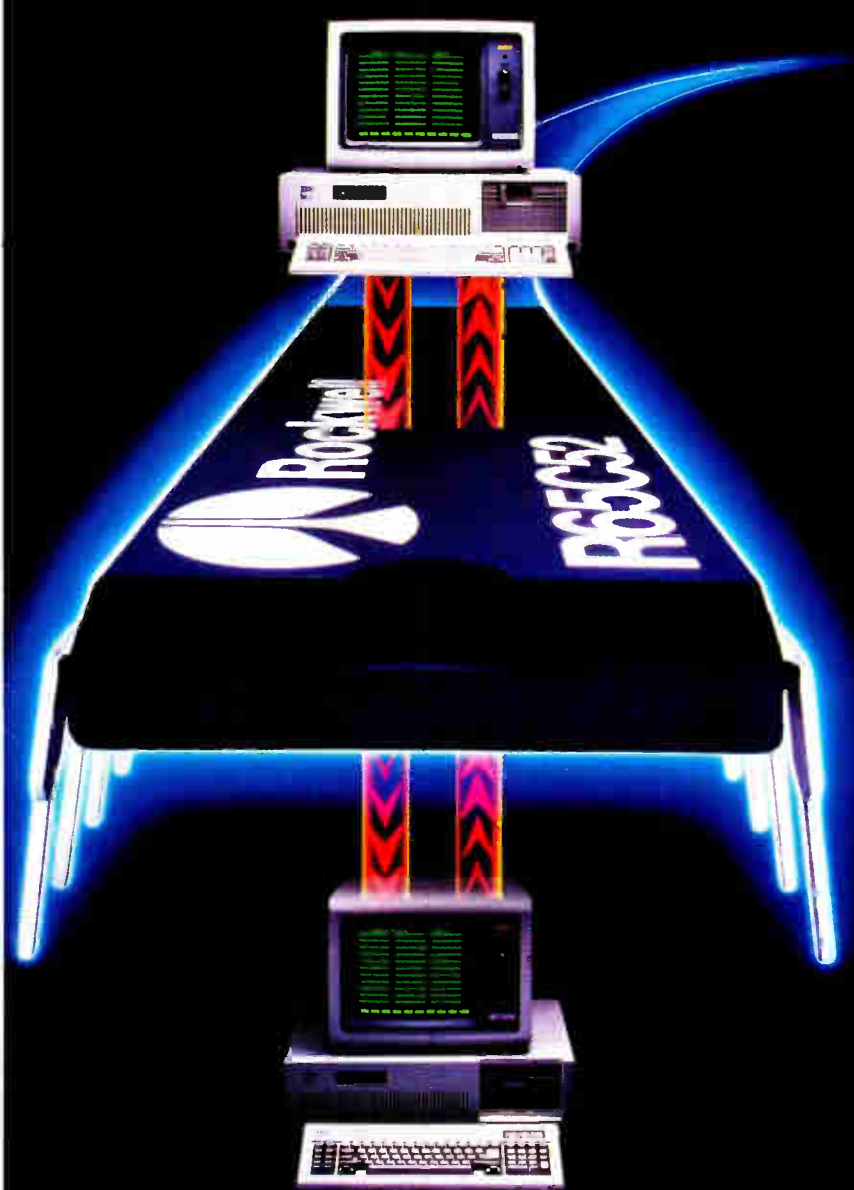

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Electronics

HUGHES BREAKS SPEED RECORD FOR DIGITAL GALLIUM ARSENIDE

CHIP ACHIEVES 18-GHz CLOCK RATE WITHOUT BEING COOLED

LOS ANGELES

Researchers working with gallium arsenide have a new clock-speed record to aim at: slightly more than 18 GHz for digital GaAs integrated circuits. Scientists at GMHE/Hughes Aircraft Co. reported last week that they have demonstrated a divide-by-two frequency-counter chip that runs in the laboratory at a clock rate of 18.05 GHz—without being cryogenically cooled.

The fastest clock rate previously reported for an experimental digital GaAs device was 13 GHz, according to the team at Hughes's Research Laboratories in Malibu, Calif. That chip, built at AT&T Bell Laboratories in 1984, was also a divider circuit. D-type flip-flops operating as binary frequency dividers are normally used to demonstrate the speed-power characteristics of new digital IC technology, the researchers say.

The Hughes GaAs chip gets its high speed by combining a number of advances in both logic design and fabrication techniques. But the most significant aspect of the achievement, the company says, is that Hughes built the high-speed chip using a conventional structure, the metal-semiconductor field-effect transistor. "The MES FET allows operation at room temperature, not the 77 K [–200°C] required for high-electron-mobility transistors [to run at top speed]," says Joseph F. Jensen, staff scientist at the labs. Much high-speed GaAs development work, including the Bell Labs chip, involves the use of HEMTs, which are regarded as having the best performance specifications. But equipping systems with cryogenic cooling causes complications not faced with MES FETs—cryogenic systems are bulky, heavy, and expensive.

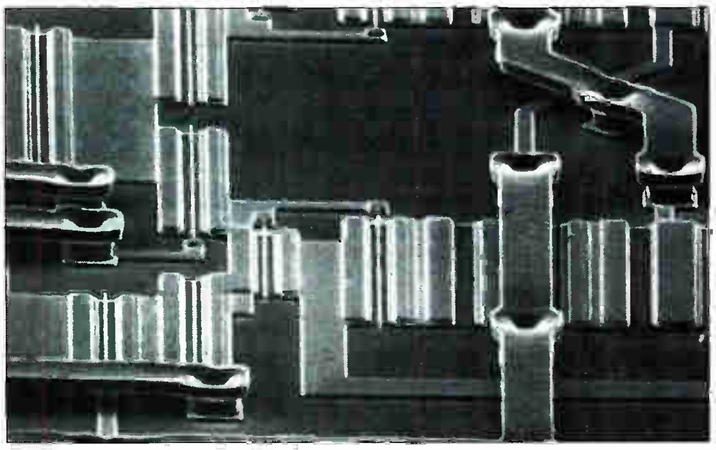
Hughes disclosed details about the new circuit last week at the International Electron Devices Meeting in Los Angeles, so manufacturers of GaAs ICs have just begun to mull over its meaning. Even so, one of them is already calling it a potential advance.

"What it shows is how much further MES FET technology can go," says Ira Deyhimy, vice president of engineering for the IC Division of Vitesse Electronics Corp., Camarillo, Calif. "It's proof of the potential of an intrinsically simple structure." His company uses MES FETs for its commercial GaAs circuits, so he welcomes experimental advances that extend the approach's perceived promise. At 18.05 GHz, the new Hughes device runs about five times faster than the fastest commercially available GaAs ICs—and about 10 times faster than silicon parts.

Hughes uses two different types of logic, both based on depletion-mode technologies, to build the ultrafast circuit, fabricating them side by side on the chip for demonstration purposes. Buffered-FET logic provides the fastest gates—it was clocked at 18.05 GHz—and high fan-out, meaning its output can drive a relatively high number of other gates. Its drawback, however, is the need for level-shifting circuitry, which contributes to excessively high power dissipation—657 mW total for the divider circuit at the top clock rate.

By contrast, capacitively enhanced logic, whose top speed is a slightly slower 17.8 GHz and whose fan-out performance is lower because the output is not buffered, achieves nearly a fivefold reduction in power dissipation, to 150 mW. CEL, also known as capacitor-diode logic, uses diode level shifting to establish the dc operating points of the circuit, which minimizes operating current and helps attain low power dissipation, according to the Hughes team. Even lower dissipation is attained at lower frequencies—98 mW at 14.5 GHz, for example.

The basic difference between the two logic types is buffering, Deyhimy says. By demonstrating both on the same chip, Hughes is smoothing the way for integrated designs that select logic types for functions where the advantages of the chosen type suit the objective, in Deyhimy's opinion. The two families "are compatible and could be mixed," Jensen confirms.



RAPID. Experimental Hughes GaAs chip proves that MES FET structures can run about five times faster than commercially available digital ICs.

Direct-write electron-beam lithography gives the chip minimum dimensions of 0.2 μm. Geometries this small demand scaling channel thickness in the device's active regions down to less than 700 Å. This requirement is met by forming the semiconductor layers by molecular-beam epitaxy.

Since molecular-beam epitaxy itself is still young, its use is another noteworthy part of the Hughes project, says process and market consultant William I. Strauss of Forward Concepts Inc., Tempe, Ariz. Molecular-beam epitaxy "is clearly the way to go when literally laying on a few molecules at a time. It gives much more precise control," he says. The epitaxy technique, which Hughes is developing at Malibu under a U. S. Navy contract, has not yet seen any commercial applications.

Work on the Hughes GaAs chip is continuing, to reduce the 2-V logic swing and further lower the power dissipation. The work is supported in part by a contract from the U. S. Air Force Wright Aeronautical Laboratories, Dayton, Ohio. *–Larry Waller*

SILICON-ON-INSULATOR GETS EASIER

LOS ANGELES

A silicon-on-insulator technique that could change industry thinking about how SOI circuits are fabricated is under development at Matsushita Electric Industrial Co. Matsushita's technique uses standard CMOS processing, avoiding the use of largely unproven chip-fabrication technology required by other SOI approaches, so it may prove far more practical for near-term commercial exploitation.

Experimental devices built with the technique developed by the Kadoma, Japan, company perform about as well as devices built on bulk silicon, according to a paper delivered by the company last week at the International Electronic Devices Meeting in Los Angeles. SOI experts at the meeting were impressed with the work, but noted that Matsushita's SOI technology can build only relatively small isolated islands of bulk silicon. They pointed out that several earlier SOI techniques are more mature.

As silicon fabrication technology approaches submicron geometries, where a plethora of second-order effects disrupts the operation of circuits, interest is growing in SOI because of its higher packing density, improved speed, lower dynamic power consumption, reduction in the number of fabrication steps, and freedom from latchup. Until now, these benefits have required techniques still largely unproven in the production environment, such as using recrystallized silicon and zone melting with lasers and electron beams.

NITRIDE'S THE KEY. Matsushita's alternative requires none of these. It uses conventional bulk CMOS processing to fabricate the insulating layer and to form tightly packed isolated islands onto which active transistors are placed. The key to the process lies in the use of several silicon nitride steps.

With a double layer of Si_3N_4 acting as a mask, trenches are formed to define silicon islands. Another layer of Si_3N_4 is deposited and etched using reactive-ion techniques to cover the sides of the silicon islands, and the silicon substrate underlying the islands is etched away. This is followed by selective oxidation using the two Si_3N_4 layers as masks until the silicon islands are electrically isolated from the substrate. The trenches are filled with polysilicon and SiO_2.

Matsushita has built islands 1.1 to 1.7 μm wide with a minimum separation of 1.5 μm. The company has fabricated both 25-stage ring oscillators and frequency-halving circuits with delay times of about 360 ps per stage.

Matsushita's technique represents a workable alternative to the more firmly entrenched SOI techniques, according to David Spratt, engineering manager of special product development at Texas Instruments Inc., Dallas. "However, the latter processes have much more momentum going for them," he says.

For example, silicon-implanted oxide techniques have been used to build 4-K static random-access memories, says Susan Partridge, an SOI researcher from GEC Research Ltd., Middlesex, UK. Silicon-on-sapphire is used in a variety of commercial products, she adds.

The major limitation of the Matsushita process, says TI's Spratt, is the size of the islands, about 1 to 2 μm wide and 10 μm long, versus at least 10 by 50 μm for one method used by TI. "It looks as if the applicability of [Matsushita's] process is limited to very high-density applications," he says.

Matsushita's work may, however, help manufacturers to squeeze the last ounce of density and speed out of bulk silicon. "It [also] appears to be a good way of combining bulk-silicon and SOI-type transistors on the same substrate, a difficult proposition for current SOI techniques," Spratt says.

–Bernard C. Cole

PROGRESS COMES, TOO, IN CONVENTIONAL SOI

Not to be upstaged by Matsushita's silicon-on-insulator development, researchers from Texas Instruments Inc. and Sharp Corp. described at IEDM last week advances in SOI technology that build on established techniques.

Starting with a common SOI technique called full isolation by oxidized porous silicon, or FIPOS, researchers from TI have attempted to surmount the process's inherent limitations. The result is a technique the Dallas company calls Islands, for isolation by self-limiting electrolytic anodization of an n^+ epitaxially defined sublayer.

Previous FIPOS efforts, based on electromechanical anodization and oxidation of p-type silicon or p^+ silicon on a p-type substrate, met with limited success because of the difficulty in isolating sufficiently wide islands without forming excessively thick porous oxide layers. There were also problems with slice warpage and stress-related defects caused by the formation of anodization "tails" at the silicon/oxide interfaces.

In the Islands process, epitaxial-quality silicon is dielectrically isolated using specially formed anodizable structures of n, n^+, and n^- silicon; computer-controlled processing to decouple vertical and horizontal anodization; and trench etching. The result is the ability to isolate layers of any desired thickness and to anodize either from a top surface or from the side walls of a trench. TI researchers were able to fabricate transistors on 0.5-μm-wide islands isolated by 1.2 μm of porous oxide.

From Sharp in Osaka, Japan, comes a recrystallization technique that allows the first layers in a three-dimensional, layered circuit to be formed as conventional ICs are. An isolating silicon dioxide layer is deposited atop the first layer, then etched to form depressions, where polysilicon film is deposited. The polysilicon/oxide layers are recrystallized by a scanning laser or electron beam. Sharp has fabricated image sensors in which one layer contains the select logic, a second holds the digitizing logic, and a third contains the photodetectors. *–B. C. C.*

COMPANIES

IS GM'S HIGH-TECH FUTURE CLOUDY WITH PEROT GONE?

DETROIT

General Motors Corp. may have rid itself of a nettlesome in-house critic, but the automaker still faces rough seas ahead after this month's messy breakup with the charismatic and outspoken H. Ross Perot, former GM director and chairman and chief executive officer of GM's Electronic Data Systems unit. Perot's departure, coupled with the indifferent success of GM's highly publicized automation efforts, leave the future cloudy for high tech at GM.

A GM management realignment gives overall EDS responsibility to Donald G. Atwood, the executive vice president in charge of the GM/Hughes Electronics Corp. subsidiary, which includes Delco Electronics Corp. The EDS president and newly elected chief executive officer, Lester M. Alberthal Jr., will now head the data services company, reporting to Atwood.

By combining all its high-technology businesses, including EDS, under one executive, GM says it will promote "even greater synergy" among the operations. But both Atwood and Alberthal are quick to point out that EDS will remain a distinct and autonomous organization within GM. "My responsibility is to work with Les on overall strategy but not to get into day-to-day operations," Atwood says.

IN CHARGE. GM's Atwood has taken EDS under his wing.

Atwood is a well-regarded manager, but some industry watchers doubt that the $742.8 million buyout pact with Perot will soon lead to improvements at GM, which reported a $338 million operating loss in this year's third quarter. And it may make things worse. "I know GM created more problems for itself with this than it solved," says Maryann Keller, an automotive analyst at Furman Selz Mager Dietz & Birney Inc. in New York.

If Keller is right, the new problems will be piled on top of old ones. Despite the $2.5 billion EDS acquisition in 1984 and a $5.1 billion buyout of aerospace and defense electronics contractor Hughes Aircraft Co. last year, GM's highly vaunted efforts to inject high technology into the company's operations have so far fallen short of the mark. GM manufacturing costs, in fact, are now higher than its domestic competitors', critics point out, and it has been forced to slow down its automation spending programs.

'IT WILL PASS.' However, Perot's departure might have little effect on GM, some observers say, although they agree the automaker faces serious problems in its core business and in its efforts to integrate high technology into the operation. "GM's major challenge is to maintain competitiveness in the automotive industry. I doubt if this will be much distraction. These kinds of things pass within a couple of months," says Edward H. Bowman, a professor of management at the University of Pennsylvania's Wharton School.

Much of the controversy centers on GM Chairman Roger B. Smith's decision, with board approval, to pay nearly double the market price to buy out 11.3 million shares of GM's Class E common stock controlled by Perot. The value of the Class E stock held by Perot and some 200 EDS executives is tied to the performance of EDS, not GM as a whole. Perot became GM's largest individual shareholder when the automaker acquired EDS, and in recent months the Texas entrepreneur had become increasingly strident in his criticism of GM's management style and its slow pace of change.

Some observers predict that GM's willingness to spend so much in an apparent effort to silence a critic—as a part of the deal, Perot agreed to stop criticizing GM—will lead to tougher 1987 labor negotiations for the automaker. Union officials are already smarting over GM plans to close all or part of 11 plants over the next three years.

And with Perot's departure, EDS employees have lost a champion at the top, GM watchers say. Some fear that lingering concerns over GM's plans for the computer-services unit could take its toll on EDS employee morale. But in the aftermath of the Perot deal, Atwood says that GM's first order of business must be to deal with the effect on EDS employees.

The Perot affair also created a furor on Wall Street and among some large GM investors, who regarded the EDS chief as a positive force within GM and are concerned over the cost of the buyout. At least two shareholder lawsuits have already been filed aimed at blocking the deal.

Whatever else happens, EDS now must solicit more business outside GM, Alberthal and Atwood agree. EDS revenues have grown from about $950 million at the time of the GM acquisition to a projected $4 billion this year. But most of that growth came from new GM business; EDS has fallen behind its historical 20%-plus compounded annual growth rate in noncaptive outside revenues. "This year we'll be in the 15% to 16% range," says Alberthal. "We're shooting to bring it back to the 20% level next year." *–Wesley R. Iversen*

TRADE

MOTOROLA AND TOSHIBA: THEY'VE ONLY JUST BEGUN

TOKYO

The sweeping semiconductor accord between Motorola Corp. and Toshiba Corp.—a trailblazing deal linking two of the world's top chip manufacturers—could eventually grow to include a joint Motorola-Toshiba presence in the U. S. market, Toshiba officials say. Industry observers think it could also be the first in a series of major alliances struck by other Japanese and U. S. companies.

The agreement signed late last month improves Motorola's access to the Japanese market, a provision that includes a new plant to be jointly owned by the two companies. It also sets technology-exchange agreements between them and gives Toshiba rights to Motorola's microprocessor line.

Toshiba executives in Tokyo say a similar agreement covering the U. S market is likely—the two companies are not likely to stand pat with what they have now. "The probability is high for a similar joint venture in the U. S.," says Toru Shima, senior manager of the Semiconductor Group's Business Planning Office. But he cautions that "there is no schedule and no program at present." In fact, some details of the current agreement are still being negotiated, Shima says, even though discussions started about 18 months ago.

For Motorola, the key to cracking the Japanese market will be the new plant, which will start producing advanced memories and microprocessors in early 1988. For its part, Toshiba will run the plant and will "actively support" Motorola's Japanese marketing effort and its worldwide activities in dynamic and static random-access-memory products.

The plant will be at Izumi City near Sendai, Japan. Building and equipping the first section will cost about $216 million; a second fabrication module will cost another $185 million. The name of the enterprise and its president are not yet settled, but the companies have agreed that, besides the microprocessors and DRAMs, the plant will also turn out 64-K and 256-K SRAMs.

MORE TO COME. The Motorola-Toshiba agreement could be a harbinger of other deals between U. S. and Japanese companies. "The semiconductor business can be roughly divided into architecture-design technology and wafer-processing and device-structure" know-how, says Hajime Sasaki, vice president of the Electron Device group at NEC Corp. "The U. S. strengths lie in the architecture, while Japanese strengths are in wafer design and processing."

Equally important, Japanese semiconductor firms are known to believe that an alliance with a U. S. counterpart may be the best way to ensure access to the U. S. market. Such alliances could help shield them against U. S. protectionist legislation that could be passed in coming years. Similarly, U. S. companies will continue to seek a door to the Japanese market.

Such factors almost certainly played a part in the Motorola-Toshiba deal, according to semiconductor-industry analysts, who note that Toshiba's longer-range objective is an enhanced U. S. presence. "It's part of the political equation," says Adam Cuhney, a San Francisco-based analyst for Kidder, Peabody & Co. "A solid relationship with Motorola could eventually be the best avenue for Toshiba into the U. S. market."

In general, industry sources believe the pact will work out, mostly because, as one consultant puts it, "each firm gets something it doesn't have now." The payoff will probably come more quickly for Motorola, they say, because the infusion of Toshiba's mass memory expertise, particularly in process and manufacturing technology, can be used to improve many of its product lines immediately. Motorola already buys 256-K RAMs from Toshiba, then does its own assembly. It will expand this operation to include larger RAMs when they come on stream.

For Toshiba, the major payoff is farther off. The plum provision in the initial agreement gives Toshiba the license to produce Motorola's 32-bit 68020 family. The 68020 is the world's best-selling 32-bit microprocessor, and its design has been sought after by Hitachi Corp. and others, but previously licensed to no one. "This shows the value Motorola placed on Toshiba's process, production, and memory technology," says Hideo Ito, manager of international planning and operations in Toshiba's Semiconductor Group and its chief negotiator for the agreement.

Shima says the Motorola-Toshiba pact is significant "because there were no similar arrangements in the past." Other deals were different, since they often involved one strong and one weak partner. "This time the strengths of both Motorola and Toshiba will be combined. It heralds a new era."

–Larry Waller and Charles Cohen

ASIAN BOOM ENTICES U. S. CHIP HOUSES

DALLAS

A sudden, dramatic boom in semiconductor sales across the Asian-Pacific basin is sending two leading U. S. chip makers in very different directions as they try to stake out regional market shares. As the strong yen cuts into the profit margins of Japanese companies, the Americans see a golden opportunity to pick up business elsewhere in Asia.

Motorola Inc. aims to boost its Asian sales by teaming up with Toshiba of Japan (see p. 33). But its American archrival Texas Instruments Inc. is searching for strength within, shuffling executives to form a new, high-level semiconductor post partly aimed at making the most of TI's installed production base in Japan and southeast Asia.

"Japanese chip sales were up 40% this past year in dollar volumes, but the strong yen has given them profitless prosperity," notes electronics analyst Michael A. Gumport of Drexel Burnham Lambert Inc., in New York. "The Japanese cannot currently afford to be too aggressive" in neighboring Asian countries.

Enter the Americans, says William McClean, semiconductor industry analyst at Integrated Circuit Engineering Corp., a Scottsdale, Ariz., market-research concern. McClean says that U. S. companies are rushing to capitalize on the 1986 Asian boom, which has rocketed sales to nearly double their 1985 level.

In 1985, semiconductor sales in Asian countries—outside of Japan—were running along at about $300 million per quarter. Sales during the third and fourth quarters were $296 million and $313 million, for example, according to ICE figures. Then sales jumped to $396 million in the first quarter of 1986 and $509 million in the second quarter. The research company believes that fourth-quarter sales will hit $600 million. N-MOS memories alone jumped from $7 million in January to $29 million in September after the U. S. imposed "foreign market value" pricing protections in a trade accord with the Japanese.

McClean says the sales explosion is a combined result of U. S. systems-assembly operations migrating to Asia, the growth of new businesses in the region, and increased chip purchases aimed at skirting the U. S. pricing regulations on Japanese ICs. "Some of these chips are getting back to the U. S. on the gray market," he says.

OPEN WINDOW. Regardless of the reasons, Dallas-based TI believes that for the coming year it has a wide-open market window to exploit. William N. Sick, leaving his post as president of TI's Semiconductor Group, has been named to a new position in charge of realizing the company's full potential in the Asian-Pacific region. TI has been manufacturing semiconductors in Japan for 15 years and now operates three wafer plants in there. In addition, it runs four other chip plants elsewhere in Asia.


LOOKING EAST. TI's Sick says sales growth in the Asian-Pacific region is now twice that of the U. S.

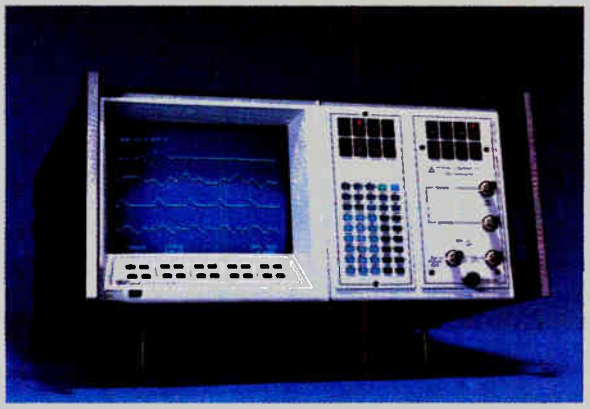
Sick says the growth rate in the Asian-Pacific region, excluding Japan, has reached twice that of U. S. markets. To capture a significant portion of the new growth, TI believes, top management must get directly involved in pursuing sales.

But the president of TI's large Semiconductor Group does not have enough time while running the day-to-day operations, explains Sick. As a consequence, TI has named executive vice president William P. (Pat) Weber president of the group and has spun off the top-level efforts in Asia to Sick, who remains an executive vice president with new duties aimed at creating worldwide business alliances with chip customers and other IC makers. Partnerships with other chip companies in Japan are not initially part of TI's new Asian thrust, Sick maintains, rebutting industry speculation.

But while executives in Dallas were attempting to distinguish between Sick's Asian marketing thrust and new efforts to create business alliances in the West, word leaked from Japan of an inventory-swapping pact between Mitsubishi and TI. TI's Japan subsidiary has agreed to exchange its advanced low-power Schottky bipolar logic parts for Mitsubishi high-speed CMOS logic.

A corporate spokesman for TI in Dallas maintains the Mitsubishi pact is aimed at filling spot shortages in the Japanese market and does not represent a major business alliance. A company source in Japan indicates that TI, which has made similar deals in the past, is using inventory-swapping agreements to avoid bringing up additional fab capacity during uncertain times in the chip market.

–J. Robert Lineback



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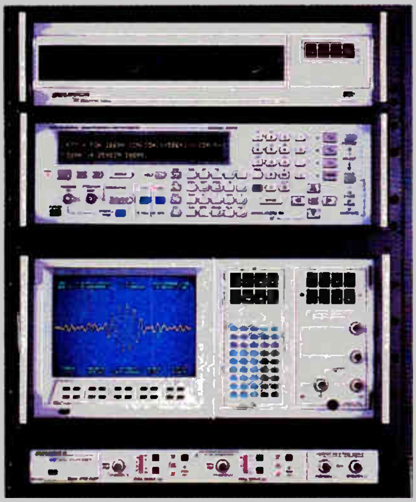

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FAIRCHILD SLASHES DIP BURN-IN REJECTS

PORTLAND, MAINE

A nasty rejection rate in solderability tests for the leads of military chips housed in dual in-line packages has been cut from 25% or 30% to zero at Fairchild Semiconductor Corp., thanks to a new approach to finishing the leads. The technique solves problems with device-lead coatings that result from the burn-in process.

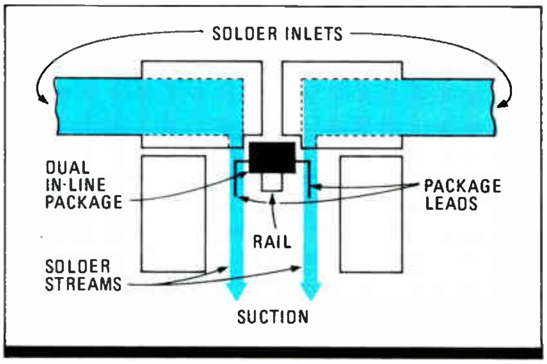
The new approach involves doing burn-in with tin-plated leads and a new wave-soldering technique that is applied after burn-in. It replaces older wave-soldering techniques, which are tricky to adjust and control, with a simpler and cleaner process, and results in a solder coat that exceeds the requirements of military standards.

WAY OF LIFE. Burn-in—operation at 125°C for 160 hours or at 150°C for 80 hours—is a way of life for manufacturers of military integrated circuits. The object of the mandated burn-in is to ensure higher reliability of the chip, but the process causes a major problem for ICs in ceramic DIPs with solder-coated leads—which are required by the Joint Army-Navy specifications.

During burn-in, solder-plated leads are subject to the formation of intermetallic compounds and surface oxides. These degraded leads then often fail the MIL-STD-883 method 2002 solderability test after the burn-in, leading either to expensive rework or to scrap. Such was the case at Fairchild's Digital Aerospace and Defense Division in Portland before the new method was developed.

In 1984, Fairchild started an engineering effort to address the solderability problem and to reduce lead-finishing costs, says Rich Wood, the senior process engineer at Fairchild who developed the concept of the new wave-soldering machine. What it came up with is a method that begins by using tin plating on the leads to absorb the rigors of burn-in. Then, just prior to shipping, the tin plate is replaced with solder in a fluxless process that is both clean and simple. The clean lead substrate beneath the tin plate together with a redesigned solder wave allows the flux to be eliminated from the soldering operation.

NO WASH. Eliminating the flux also eliminates the need to wash and dry the devices after soldering. The removal of this cycle shortens the process; it also means there is no need for a drain, allowing the equipment to be installed anywhere in a manufacturing facility. In addition, the elimination of flammable and corrosive flux makes the operation safer.



SOLDER COLUMNS. A Fairchild process for coating DIP leads with solder has eliminated solderability-test failures.

The first step in the Fairchild process consists of cleaning the Alloy 42 leads with acid. Then the leads are tin-plated, and the IC is burned-in.

Ordinarily, the next step would be to go to a conventional wave-soldering machine. But for this application, the machines have several drawbacks. Wave heights fluctuate, for example; environmental changes can cause solder "icicles;" and there is a tendency for solder to go places it's not wanted.

Fairchild's wave solderer isolates the solder that goes to the leads. The wave consists of two vertically flowing solder columns through which the DIP travels, sliding along a supporting rail (see figure). The two solder columns, one on each side of the DIP, flow down over the leads as the package travels horizontally. The tin plate is dissolved in the molten solder, allowing solder to adhere to the clean substrate that was beneath it. As the package leaves the solder, it enters a stream of hot nitrogen gas, which prevents the formation of icicles on the ends of the leads.

The resulting solder finish is smooth and uniform, and the part has no difficulty passing the MIL-STD-883 test. The Fairchild process produces a solder layer with a thickness that exceeds military requirements. The average thickness achieved by the process is 750 μin.; the standard specifies a minimum solder thickness of 200 μin. *–Jerry Lyman*

COMPONENTS

A SIMPLER FRONT END FOR DATA-ACQUISTION SYSTEMS

AUSTIN, TEXAS

Setting up data-acquisition systems to handle multiple high-speed analog signals is a burden that systems designers have had to bear for many years. Discrete-circuit solutions have been plagued by poorly understood error sources and low temperature ceilings, and bipolar-based hybrids are power-hungry and carry high price tags. But by drawing on recent advances in digital CMOS logic, Crystal Semiconductor Corp. is aiming to unburden the systems designer with a single-chip solution containing four simultaneously operating amplifiers.

The Austin, Texas, company has built a CMOS track-and-hold analog integrated circuit—a single chip that, besides the four amplifiers, contains its own microcontroller, signal-storage capacitors, output multiplexer, and output buffers. Crystal says the 18-pin IC could streamline data-acquisition architectures and greatly boost performance.

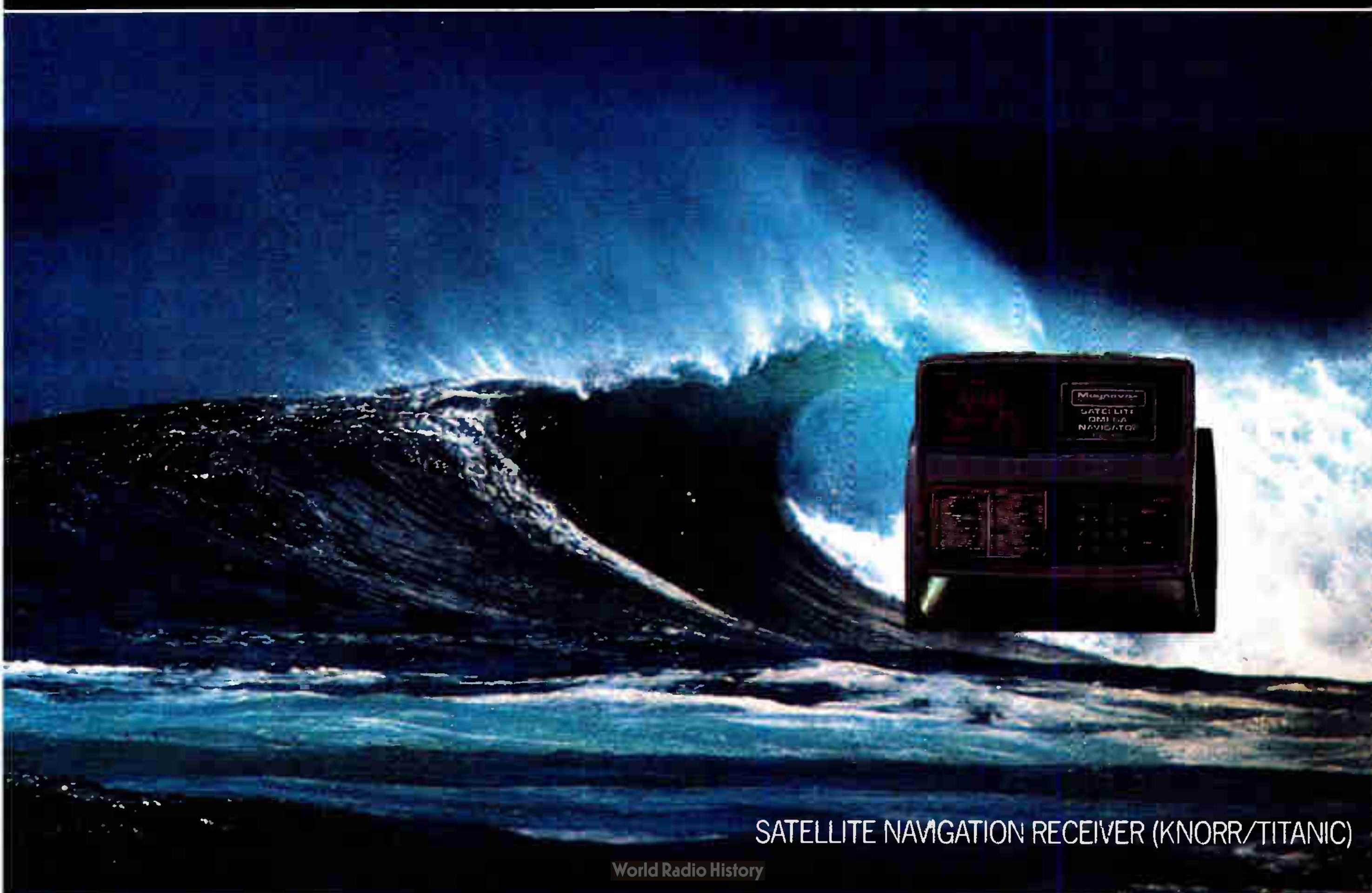
The cool-running 3-μm design has the digital power to calibrate itself with control logic, and it will maintain steady 12-bit accuracy even if the operating temperature climbs above the Mil-Spec range, says Crystal.

The track-and-hold market is a small one, worth about $46 million last year, says Edward D'Entremont, vice president of marketing at Hybrid Systems Corp., an established supplier of track-and-hold and other data-acquisition products in Billerica, Mass. But he adds that the market is growing by about 20% to 25% per year, and Crystal's John Croteau, product manager for data-conversion ICs, believes it could grow even faster with the emergence of low-cost monolithic parts. Track-and-hold devices are generally used in combination with analog-to-digital converters to slow down high-speed signals long enough for the highly accurate (but often slow) ADCs to do their job.

Twelve-bit converters today are relatively slow, able to deal with only 2-Hz signals when unaided by a track-and-hold circuit. D'Entremont says track-and-hold devices enable 12-bit converters to reach about 28 kHz, opening up military radar and avionics applications.


STAR TRACKER (IPS/SPACELAB)

The secret of finding...


SATELLITE NAVIGATION RECEIVER (KNORR/TITANIC)

At 11:40 p.m. on April 14th 1912, the *RMS Titanic* struck an iceberg some 400 miles off the coast of Newfoundland. In less than three hours, the 'unsinkable' luxury liner had sunk to the sea bottom in one of the worst maritime disasters of the century. Finding her became a commitment by oceanologists and technologists alike.

Several tried. All failed. For the problems, like the tragedy, were on a grand scale. The North Atlantic is not known for its hospitality. And the freezing waters are nearly 2.5 miles deep. To add to these difficulties, not only was *Titanic's* last radio position known to be inaccurate, but fierce currents had also swept her away in a south-easterly direction.

Last year, however, after the French ship *le Suroît* had covered 80% of the target zone, the French-American expedition team embarked on the high-technology research ship *Knorr*.

This high-technology included a pair of MAGNAVOX* satellite navigation receivers - one providing highly accurate position information by tracking satellites of the new global positioning system, the other providing periodic position updates from transit satellites. With these two receivers onboard, the *Knorr* was equipped with the most precise and sophisticated marine navigation system available.

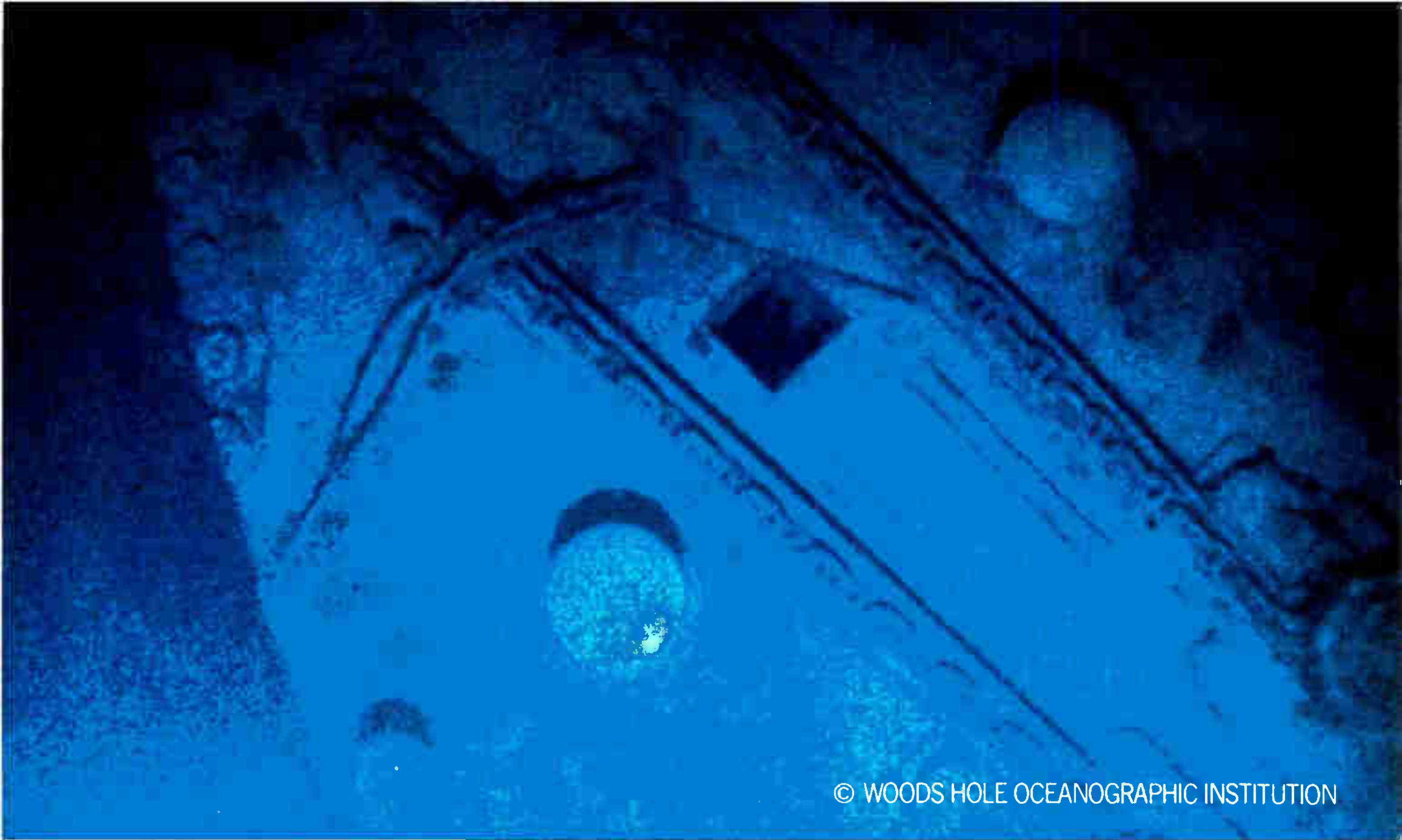
The MAGNAVOX receivers were used to criss-cross the remaining 20% of the search area, working to a position accuracy of just 35 meters. Even in heavy seas. Then, starting from the most likely spot, the underwater search vehicle *Argo* was lowered to begin close-up investigation.

At 1:05 a.m. on September 1st, 1985, her video cameras recorded the eerie outline of one of *Titanic's* mighty boilers. The seventy-three year search was over.

Little wonder that our satellite navigators are used aboard thousands of offshore platforms, rigs and ships - including *Queen Elizabeth II* - and that our global positioning system receivers are leading the way in precise navigation, on land, at sea and in the air.

Because no matter where you look, you won't find anything better.

...is knowing where



to look... Philips.

From the depths of the ocean to the depths of space. One of the most demanding endeavours is the scientific exploration of the sun - a research programme conducted by NASA in collaboration with the European Space Agency, ESA.

Key to this research is SPACELAB 2; fifteen tons of advanced space technology launched in August 1985. The problem was how to ensure that, once in orbit, SPACELAB 2's platform, with the powerful telescope, could be manoeuvred under remote control without any sensitivity to the shuttle motions.

The solution was provided by three SODERN** SED 04 star trackers integrated by Dornier in the Instrument Pointing System responsible for positioning the platform. Each of these electronic sensors operates to an accuracy of 0.75 seconds of arc - which is roughly equivalent to a golf ball seen from 10,000 meters. Distance, however, is no problem, for the platform responds perfectly to every command from mission control some 300 km below. Which is hardly surprising, for similar SED trackers have been operating on EXOSAT for over 3 years.

In fact, SODERN, as world leader in attitude measurement and star tracking, has been involved in major European and U.S. space programmes, providing over 90 opto-electronic systems with more than 200 years of operation without a single failure.

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*** SODERN - a high tech French Philips research company specializing in e.g. attitude sensors for satellites and spacecraft; positioning and alignment of inertial platforms; rendezvous and docking; remote sensing of Earth resources, etc.*

PHILIPS

Circle 41 on reader service card

Philips Corporate Marketing Communications, Eindhoven, the Netherlands.

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SEIKO INSTRUMENTS

Circle 44 on reader service card

fringence-effect displays. SBE displays achieve higher contrast and are easier to read than conventional twisted-nematic models. With twisted-nematic displays, contrast is critically dependent on the viewing angle, but SBE displays, in which the molecules of the liquid crystal are twisted by 270°, maintain high contrast even at small voltage variations. SBE displays can achieve four to five times higher contrast than their twisted-nematic cousins. Moreover, dependence on the viewing angle is reduced by a factor of 10 in the vertical and 4 in the horizontal direction.

Besides the opening of the Heerlen center, another significant component in Philips's LCD strategy is an assist from Sharp Corp., Osaka. Under an 18-month-old cooperative agreement, Sharp is sharing its technical know-how on LCD fabrication and also furnishing production equipment. Also, the partners have granted each other licenses to some of their LCD patents, and they are logical candidates to become second sources for each other's products.

The Japanese ally could be a key factor for Philips—its fiercest competition in the LCD market will come from Sharp, Hitachi, and other Japanese companies that are already entrenched there. Philips thinks that taking on the Japanese will be worth the effort. Conrads says the company is convinced that LCDs—now found mostly in low-cost products such as watches, clocks, and pocket calculators—are going to be used more and more in complex applications, ranging from consumer electronics to automobiles, and telecommunications. "We regard LCDs as key components for future information and communication concepts," he says. Not only will LCDs affect system design—in such areas as personal computers—but they will also find new applications, such as pocket personal computers, and information and navigation systems for automobiles. *–John Gosch*

INDUSTRIAL

DIAGNOSTIC BOX CATCHES CONTROL FAULTS FAST

BURLINGTON, MASS.

By going against the grain of current design practice, a new on-line diagnostic unit for process-control systems used in manufacturing achieves dramatically higher input-scanning speed at a lower cost. The diagnostic unit proper is distinguished by the absence of microprocessors and software, at a time when the instinctive reaction to many engineering problems is to reach for a microprocessor. Relying instead on firmware and custom logic, the unit promises to simplify diagnostics and provide scan times that are far faster than other approaches.

Called the Detective, the unit will be field-tested by Ford Motor Co. this month. It is essentially a state machine that requires processes to be modeled in stages, using a flow chart. Developed by Transimatics Inc., Burlington, the system stores, in an electrically programmable read-only memory, data that defines the progression of process-control stages and the inputs required to proceed with a control sequence.

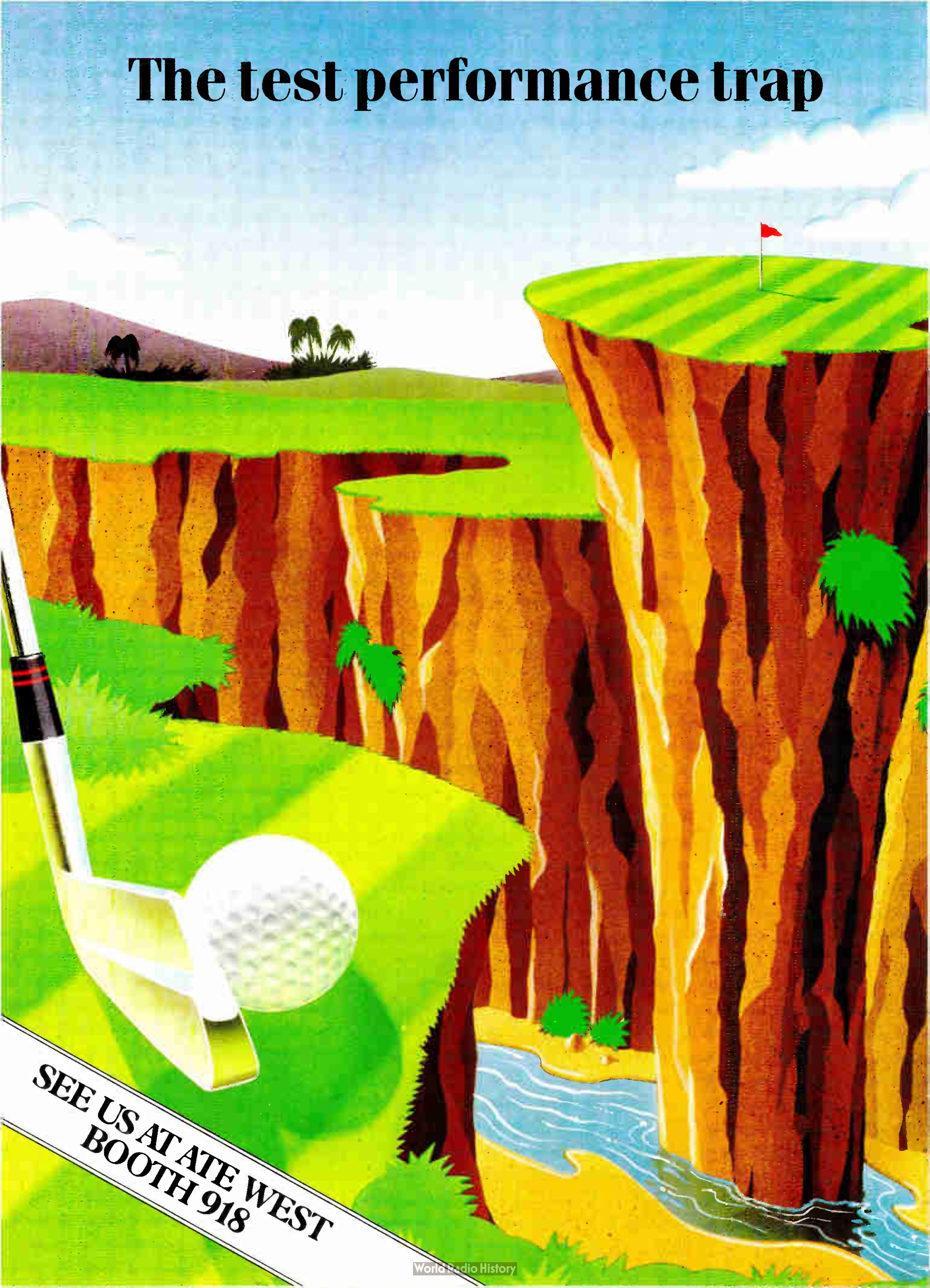
The Detective is based on an approach that Transimatics calls firmware transitional logic. It monitors processes by high-speed detection of input transitions. Its users see current process-control stages or preset alarm stages identified on the screen of a personal computer. The approach cuts the time needed to detect a transition associated with a malfunction to about 32 µs. The unit can interface with any programmable logic controller.

The heart of the Detective is a printed-circuit board called the Transimate, which carries a pair of custom integrated circuits that scan 29 external channels, plus three used for internal purposes, at a rate of one µs per input, looking for transitions. The transitions may originate directly from the process machinery or from on-board timers on another custom IC.

In either case, when a transition on a channel is detected by the Detective's central logic unit—a chip consisting of gates and registers—the logic unit consults an on-board EPROM about the detected change. The 8-K EPROM has a 13-bit address word. Five of the bits are defined by the particular input channel, out of 32 possible, being scanned. Eight bits are assigned to stage definition, for a capacity of 256 process-con-trol stages.

DERSIN: Defining a system in firmware speeds diagnostics.

The scanning ICs send 5 bits to the EPROM that tell it on what channel the


The test performance trap
SEE US AT ATE WEST
BOOTH 918

transition was detected. At any given stage, the EPROM's data output tells the logic unit whether a transition is expected on that channel. If none is expected, the logic unit signals a malfunction. The EPROM may also store control outputs for an emergency shutdown, corresponding to alarm stages.

RECALL. The only microprocessor used in the system is employed as an interface between a first-in, first-out stack board and the supervisory personal computer. This board can recall the transitions detected for the last 29 stages, so that a sequence of events leading up to system failure can be traced.

Pierre Dersin, president of Transimatics, a subsidiary of Fabricom SA in Belgium, emphasizes that a microprocessor-based solution to the problem of real-time process diagnosis would be handicapped by software and operating systems, most likely resulting in substantially lower performance. "We use no operating software," says Dersin. "Everything is in firmware."

Attempts to use programmable logic controllers themselves for diagnostics often run into significant obstacles. Adding diagnostic functions can de-

EPROM and logic chip detect malfunctions in 32 microseconds

grade performance to unacceptable levels. The only way to maintain performance is to add costly memory.

In either case, the ladder diagrams used to program the controllers are cumbersome and require special skills. Their complexity increases engineering costs, particularly when changes in a process require modification of the diagnostic system. Finally, controllers have relatively slow scan rates, from 1 to 10 ms per input, often making it impossible for them to capture the first in a rapid series of malfunctions.

The Transimate board was itself initially marketed as a controller. Feedback from customers led Transimatics to reconfigure the product with an intelligent interface as a diagnostic system.

Ford will begin field trials of the device this month in a manufacturing environment, after successful lab tests at its Robotics and Automation Application Consulting Center in Dearborn, Mich. Bill Ford, a computer-applications engineer at the center, says the automaker developed—and later rejected—an in-house computer-based system for the diagnostic application for which the Detective is slated. "The problem is that if the computer goes down, there's no diagnostics for the system . . . and it's not as fast," he says. *–Craig D. Rose*

Cadnetix the standard C

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- Physical Modeling Engine: This engine simulates

introduces AE workstation.

VLSI chips at vector rates of up to 16 MHz and accommodates devices with up to 364 inputs and 384 outputs. Vector storage of 512K x 91 bits provides for longer simulations and simultaneous analysis of up to 30 devices.

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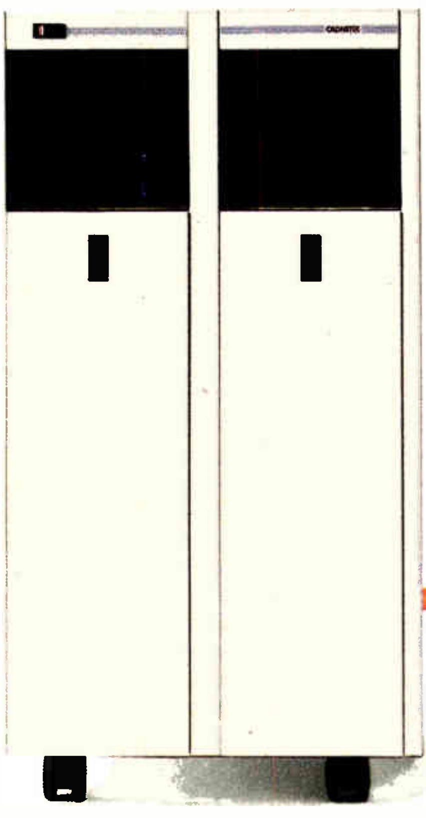

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Circle 49 on reader service card

INTERNATIONAL NEWSLETTER

BRITISH SAY THEY HAVE A WAY TO SHARPEN LARGE LCD ARRAYS

A British government-backed research project, led by STC Technology Ltd., has come up with a way to get high-quality large-screen displays with ferroelectric smectic liquid crystals. LCDs now in use cannot handle large arrays without seriously degrading the picture quality. The Japanese build a thin-film transistor behind each picture element; that's fine for small displays but gets extremely complex in larger screens. STC, however, says that by using the memory properties of the ferroelectric smectic crystals, it has built a lab device with 4,000 picture elements and has simulated the crystals' behavior on a million-element screen. The researchers report switching arrays of picture elements greater than 1,000 rows at 64 μs. □

JAPAN SETS UP COPYRIGHT PROTECTION FOR SOFTWARE

To encourage greater enterprise within Japan's software industry, two government agencies are moving to make software eligible for Japanese copyright next spring. Copyrights help programmers to protect their work—presumably encouraging them to write more and better software. Software copyrighted in the U. S. will be protected automatically in Japan. The Software Information Center, established last week by the Ministry of International Trade and Industry in cooperation with the Ministry of Education, will administer the program. The center will store printouts of programs in microfiche for 50 years, the period for which protection will be provided. □

PHILIPS' LOW-POWER SRAM COULD CLICK WITH BATTERY-POWERED GEAR

A 256-K static random-access memory under development at Philips Research Laboratories is shaping up as a natural for battery-operated equipment. Using less than 1 μW of power in standby and 75 mW at 10 MHz, the SRAM has a cell area as small as 200 μm^2, achieved by a relatively simple CMOS process. The six-transistor memory cell, in which both the npn and pnp transistors are cross-coupled, gets its small size from a 1.3-μm double-metal technology with a single polysilicon layer on an epitaxial substrate. It's also fast: the 32-K-by-8-bit memory accesses in 40 ns. □

HITACHI ADDS MEMORY-MANAGEMENT FUNCTION TO C COMPILER

Closing a performance gap in C-language compilers, Hitachi Ltd. has developed a compiler for its Z80-compatible 64180R1 microprocessor that can implement the memory-management function that translates the 64-K byte logical-address space into the 1-megabyte physical-address space. The new compiler will be sold initially as a VAX compiler; a version for the IBM PC is coming. The VAX version will ship in Japan on Jan. 21, at a price of $3,400, and overseas on Feb. 20, with the price to be determined. In Japan, the PC version will cost about $1,575; overseas prices are not set. □

PRIVATE FIBER LINK TO CROSS THE ATLANTIC BY 1989

The first privately financed transatlantic fiber-optic link, PTAT-1, is scheduled to enter service in June 1989, hot on the heels of the first publicly funded system, TAT-8, which will be ready in 1988. STC Submarine Systems Ltd. of Greenwich, England, has been awarded a $350 million order as prime contractor for PTAT-1 from Cable & Wireless and Tel-Optik. The line will span more than 7,000 km underwater, from Weston-super-Mare in England to Long Island, N. Y., with a spur to Suewood Bay in Bermuda. The system will include three working pairs and a spare pair that can be used as a backup; each pair will carry 5,760 channels at 420 Mb/s and have 114 repeaters. □

INTERPHASE PULLS A FAST ONE

30 MBytes/s on VMEbus

INTERPHASE® shatters the old speed limits of the VMEbus with its second generation of VME disk controllers boasting 30 megabytes per second bus speeds and above. Using a new INTERPHASE technology breakthrough called the BUSpacket Interface℠ ... the new V/SMD 4200 Cheetah and V/ESDI 4201 Panther triple existing VMEbus speeds and approach the VMEbus theoretical bandwidth of 40 megabytes per second!

SIMPLY THE FASTEST

The combination of the BUSpacket Interface and a large (128 KBytes) cache memory provide the V/SMD 4200 and V/ESDI 4201 with unequalled speed, and make them the fastest SMD and ESDI controllers by a factor of three. No one even comes close!

In simple terms, the new INTERPHASE technology preformats packets of data to go across the bus before acquiring it. The INTERPHASE BUSpacket approach unharnesses the VMEbus from slow devices through deep, high-speed bus FIFOs and an asynchronous delay line-based state machine, which controls bus transfers. Data is emptied onto the bus in packets at speeds 30 megabytes per second and above.

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The V/SMD 4200 and V/ESDI 4201 also incorporate the proven INTERPHASE features of the multitasking Virtual Buffer Architecture℠, Intelligent Caching, and zero latency operation found on other popular INTERPHASE products. The four drive V/ESDI 4201 Panther even adds an integral SCSI port for easy addition of back up devices.

Both products complement INTERPHASE's high-performance V/Tape 3209 1/2" tape controller, and are **PLUG & PLAY** software compatible with the industry's most successful SMD and ESDI controllers, our V/SMD 3200 and V/ESDI 3201.

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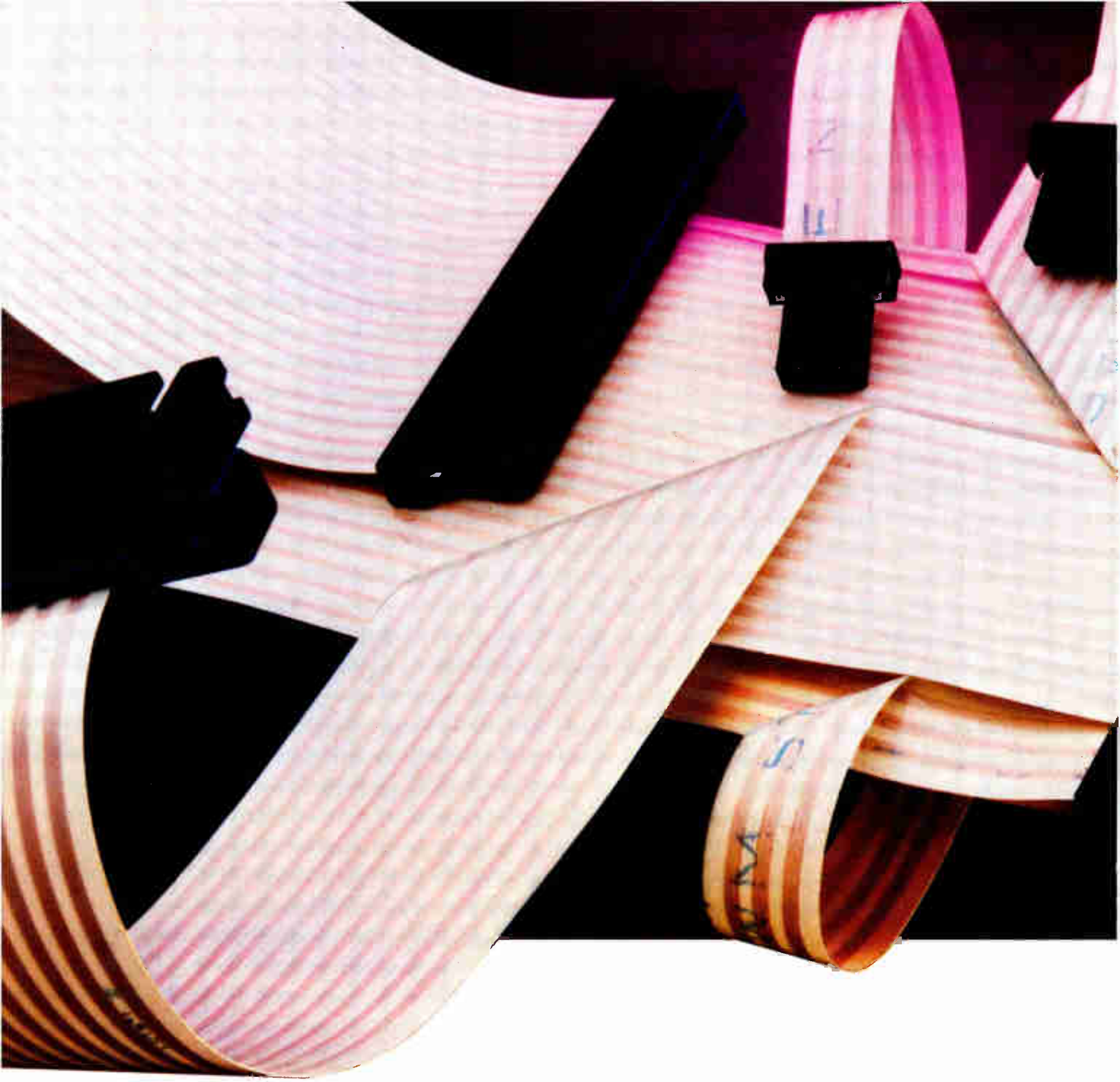
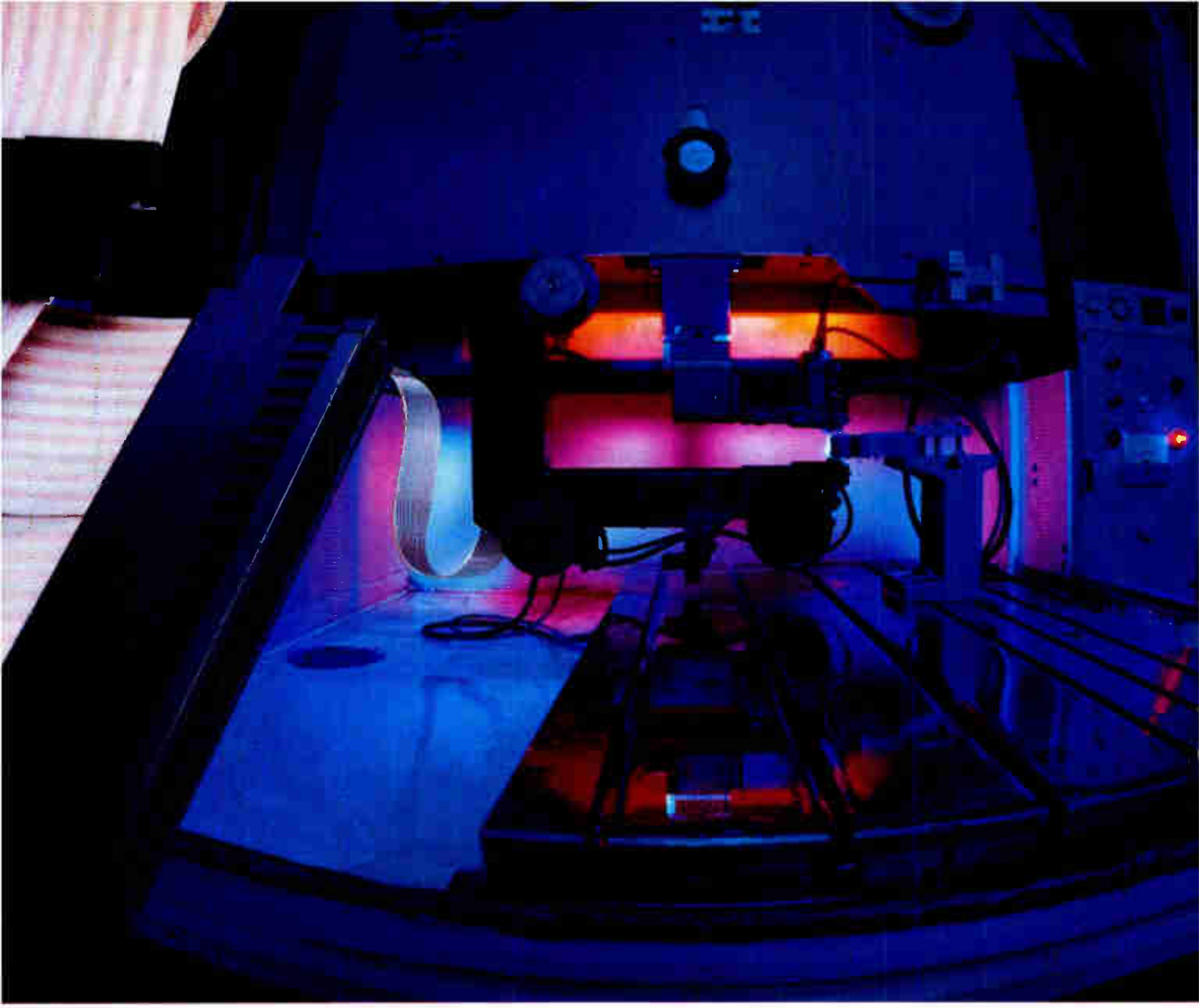


This flat conductor cabling system from AMP lets you flex your imagination, too.



Flexible flat cable offers today's designers an attractive alternative to discrete wire—higher-density packaging and uniform conductor-to-conductor relationships. And, of course, it's flexible. To the tune of tens of millions of cycles.

Now, picture this. Our flex flat cable harnesses come complete and ready to install, and they intermate with a wide variety of standard headers on .050″ or .100″ centers. And our cable and components are designed for high-productivity machine termination in your plant. Either way offers big savings for you.

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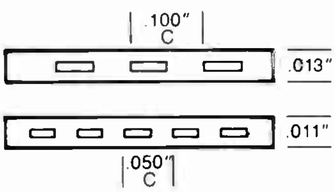
Circle 53 on reader service card

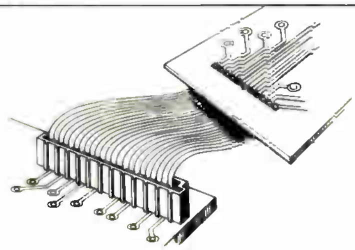
AMP Interconnecting ideas

Pressed for space? .100″ center cable is just .013″ thick, max, rated to 3A/conductor; .050″ center cable is .011″ thick, rated to 1.5A/conductor.

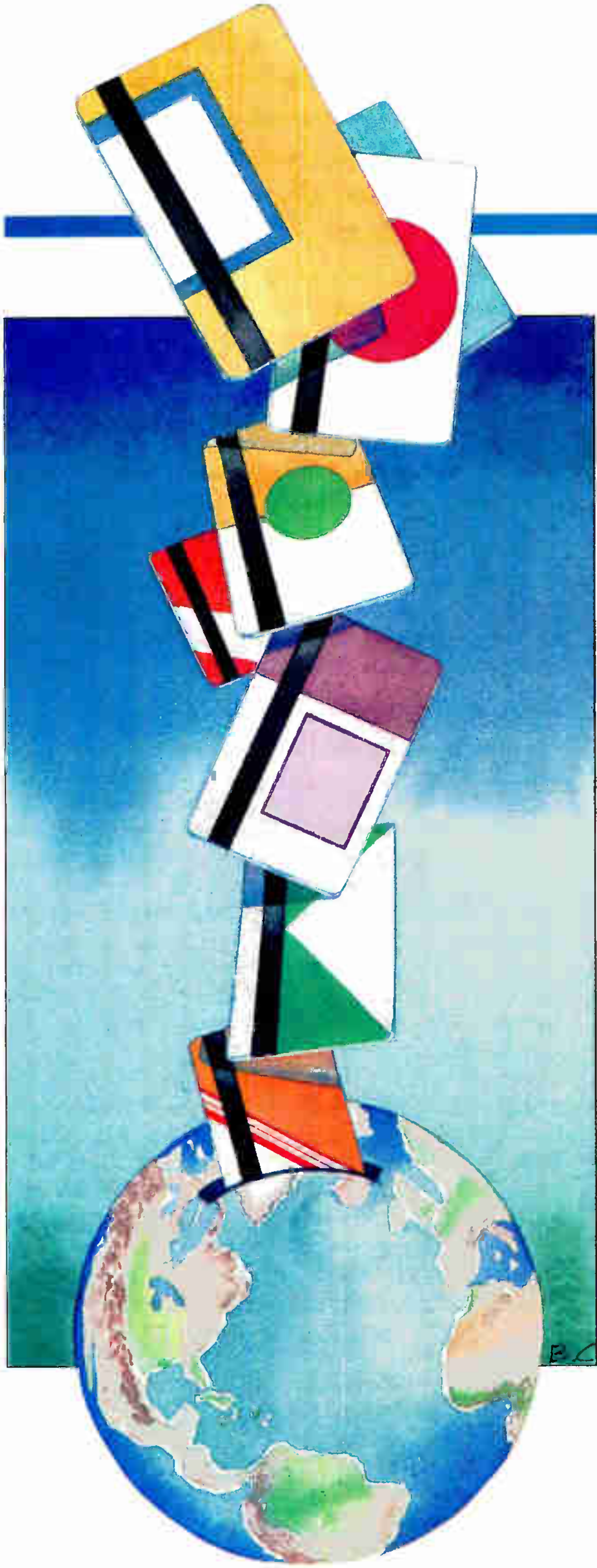
Flat conductors dissipate heat more efficiently. Ideal idea for connecting things in motion, from print heads to robotics.



AMP Trio-Mate connectors for flat flex cable .004″ to .015″ thick. Staggered contacts reduce insertion force, wiping action assures reliable contact. Horizontal and vertical styles, 2-22 positions.



INSIDE TECHNOLOGY



SMART CARD

WILL IT CREATE A BILLION DOLLAR IC BUSINESS?

by Clifford Barney

Smart cards—wallet-sized plastic with embedded microprocessor and memory chips—are beginning to emerge as a marketplace, one that many see as the next semiconductor bonanza. Painting visions of potential applications almost anywhere digital information is processed, smart card enthusiasts predict multimillion-unit markets, all delightfully free of the need to surround chips with boards, computer iron, and cables. A lightweight card and a few contacts are all that is needed to

SMART-CARD TESTS PLANNED OR UNDER WAY	
Sponsor	**Application**
JAPAN	
Dai-Ichi Kangyo	Banking
Daiwa Bank	Shopping
Fuji Bank	Corporate banking
Mitsui Bank and Toshiba Credit	Banking and shopping
Sanwa Bank	Shopping
Seibu Bank	Medical
Sumitomo Bank	Shopping
Toshiba	Point-of-sale systems
Toyo Trust Bank	Financial management
EUROPE	
Credito Valtellinese, Italy	Savings
French PTT	Point-of-sale systems
French PTT	Public phones
French PTT	Telepayment
University of Paris	Student transcripts
UNITED STATES	
Bank of Virginia	MasterCard trial
Department of Agriculture	Food-stamp card
Department of Health, Education, and Welfare	National health insurance cards
J.C. Penney	Home banking
MasterCard	Point-of-sale systems
Visa	Supersmart card
Navy	Medical records

SOURCE: DATAQUEST INC

put a smart-card chip to work. But the ability to put intelligence on a card has outstripped the imagination to use it. Without unique applications, smart cards have remained a technical curiosity, some sort of bonsai computer. Now those new applications are beginning to appear, as chip and card makers develop more flexible ways of packaging control and memory.

Progress is most evident in France, where some 8 million cards are being used. Japan is closing in, with dozens of smart-card tests planned or under way. So far, however, the U. S. companies have lagged behind in developing both technology and applications.

One reason for the delay is that the market is hard to pinpoint. Because many of the products and chips are still undefined, most analysts estimate unit sales, rather than dollar volumes. For example, Sheridan Tatsuno of Dataquest Inc., a San Jose, Calif., market-research firm, pegs the U. S. market by orders of magnitude. This year, he says, hundreds of thousands of smart-card chips will be made. By 1988, the volume will be in the millions; by 1989, in the tens of millions; and by the 1990s, in the hundreds of millions. One explicit prediction comes from B. K. Marya, president of Catalyst Semiconductor Inc., a Santa Clara, Calif., company that has developed a smart card with 2-K bytes of memory (see p. 59). He says the market for microcontrollers has the potential to grow to $2 billion by 1992.

One problem with forecasts is that smart cards themselves are somewhat vaguely defined. Generally, most industry observers draw a distinction between "chip cards," which have on-board intelligence, and cards that only have memory capacity. Some people lump pure memory cards in with smart cards; others consider these "dumb cards" (see p. 58). Most people use the labels "smart card" and "chip card" interchangeably, but the former is a general term and the latter implies the presence of an integrated circuit, usually a microcontroller.

Regardless of the definition, the smart card is expected to generate a lot of business, with credit-card transactions bringing the most. So far, that market is developing very slowly, as bankers feel their way along unfamiliar ground.

While the financial community tries to decide how to use smart cards, niche markets are beginning in cards for what Tatsuno calls "3-M applications:" military, medical, and manufacturing uses, including process control, maintenance, security and access, and medical records.

In Japan alone, Tatsuno counts 40 tests scheduled or in progress, nine of them major (see table), involving 81 vendors of chips, cards, readers, and services. Besides Japanese printing companies, which make credit cards, Tatsuno reports that IC makers, materials manufacturers, and watch and calculator makers are all jumping in.

SINGLE CHIPS FOR JAPAN

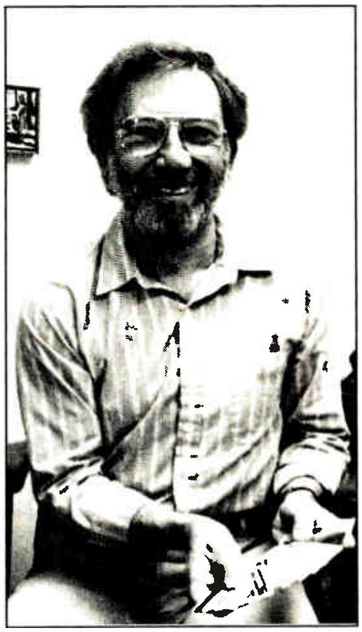
Japan has already gone through a generation of multichip cards and is gradually switching to single-chip versions except where large amounts of memory are required. The major application is off-line shopping, in which banks "charge up" a card and merchants subtract, at the point of sale, the purchase price from the balance recorded on the card.

Dai Nippon Printing Co. is engaged in an experiment with banks and merchants in 10 cities for cashless shopping. Toppan Printing Co., Kyodo Printing Co., Hitachi Maxell, and Fujitsu also have off-line shopping tests. Dai Nippon has a medical-records experiment in which 50 hospitals use its cards to record visits to doctors. Toppan is using cards to charge employees for meals in the firm's cafeteria, and reportedly has a multi-application card in the works. Kyodo has a data card for use in personnel management and inventory control.

In France, a government-mandated smart-card effort is starting to generate some significant numbers. Last month, Thomson Semiconducteur's MOS division marked the fabrication of its 15 millionth smart-card chip in a single year. The French have 7 million telephone chip cards and a million bank credit cards already in circulation, estimates Jerome Svigals, publisher of the newsletter *Smart Cards and Comments*. And the big wave of French cards has yet to hit: under government directive, all French retailers must have smart-card readers by 1990, providing support for millions of cards.

Applications are already proliferating. Marc Lassus, general manager of Thomson's MOS division, says that his firm is developing new products for manufacturing-inventory control and for the trucking industry, to monitor vehicle performance. Smart cards are being used to record the transcripts of some 8,000 students at the University of Paris; the French national health-insurance program will draw on the results of that operation for its own smart card.

"We are confident that the market is going to explode very soon," Lassus says. "The problem is going to be to help the customer with a complete system, rather than just a piece of plastic with a chip on it. That, we have already mastered. Now it is just a question of new products fitting to an exact application."



SEIDMAN: If MasterCard goes ahead, Visa will have to go along.

In the U. S., however, only three field trials of smart cards are now going on; four more are planned. Tatsuno and Svigals say the Japanese and French are leaving the U. S. behind.

"Every major Japanese bank, retailer, equipment vendor, card supplier, or government agency involved with postal telegraph, health and welfare, or transportation is involved in tests," Svigals says. "There are industrial applications, taxi-meter cards, music-synthesizer cards. I have never seen anything in Japan that matches the scope and intensity of this technology."

By contrast, says Tatsuno, "The U. S. has been slow on its feet. The American firms say, 'There is no market here; why waste our time?' The Japanese say, 'There will be no market for five years, there is time to do the groundwork.'"

Tatsuno warns that smart-card customers are institutions, rather than individuals, so startup time includes two to three years of testing. "Volumes may not pick up until 1991," Tatsuno says, "but by then the technical game will be over. Unless you are in now, it's too late."

The U. S. market is not totally quiescent. Motorola Semiconductor, the sole major U. S. chip firm with a serious smart-card program, says it has more activity than it can handle. And a handful of smaller firms, like Catalyst, Seeq Technology, Exel Microelectronics, and Xicor, are exploiting electrically erasable memory technology to build "soft chips" that can multiply smart-card applications.

General Instrument Corp.'s Microelectronics Division in Chandler, Ariz., says that it is looking into smart-card chips with on-board EEPROM. Another division of General Instrument provided prototypes for a "supersmart" card, with a keyboard and display, that Visa is investigating.

But in general, the big U. S. chip firms are not convinced that smart-card applications warrant a major effort at this time. Neither Texas Instruments Inc. nor Advanced Micro Devices offers a smart-card chip. (Seeq, however, has a chip with on-board EEPROM built around the TMS 7000 microprocessor from TI.) Intel Corp. indicates a keen awareness of smart-card potential but little inclination to pursue it now.

The biggest U. S. player so far is MasterCard, which is aggressively promoting smart cards in two tests and has already distributed specifications for its next-generation bank cards to nearly 150 potential suppliers. But financial smart cards in the U. S. are being held up while MasterCard and archrival Visa come to terms.

The gap between them is wide. MasterCard is going full-bore. It expects to have pilot quantities of terminals and cards available by next October or November, and to be in full-scale production by 1988. "We will have a minimum of six to eight major vendors," says John C. Elliott, MasterCard's executive vice president for electronic services. Further, Elliott adds, the cards will not be limited to financial transactions but will also be capable of keeping medical records and performing other functions. Siemens in West Germany, Bull SA, Motorola, and Omron in Japan are likely contenders. Cards for one of MasterCard's field trials are being made by MicroCard Technologies Inc. of Dallas, a Bull SA subsidiary, and contain a Motorola chip.

Tatsuno: "Americans say, 'There's no market here; why waste our time?' The Japanese say, 'There will be no market for five years, there's time to do the groundwork'"

Visa general manager J. Pino Francini argues that cards that require a special reader are not cost-effective in the decentralized U. S. banking system. "We are not against chip cards; on the contrary, we fully believe it will come," Francini says. "But we are not for rushing ahead and turning banking upside down purely in the name of technology. Let's figure it out first, and then there are a hell of a lot of technologies out there we can use."

Stephen Seidman, publisher of the newsletter *Smart Card Reports*, thinks Visa may have no choice, however, because "If MasterCard goes ahead, it's hard to imagine that Visa would let it have the single say over how smart cards are used." Seidman adds that individual banks may force the issue by giving customers cards that carry a form of electronic Green Stamps, giving extra credit for use of a client's airline, hotel, or auto-rental service.

MasterCard has suggested a meeting next month to thrash out the future of smart cards in the U. S., but no date has been set.

Not everyone thinks smart cards are ready to fly. John Fisher, executive vice president of Banc One in Columbus, Ohio, compares them to the Concorde, as an example of a "fine but misplaced technology."

Fisher agrees with Francini that the U. S. banking industry is moving toward on-line storage of data, not storage distributed on cards. He claims that only 10% of the public has accepted the use of automatic-teller cards to obtain cash, leading him to think that smart cards will not win easy acceptance. "Nothing important will happen with chips for a decade," he says.

In any case, the embryonic market faces problems of cost, reliability, security, and standardization, even as it tries to develop new applications. One-chip cards go a long way toward solving the first three, but standards are such a thorny issue that the earliest markets are in smaller applications where interoperability is not necessary. Japanese cards do not conform to the standards worked out by the International Standards Organization. Eventually, however, widespread use of smart credit cards will depend on adherence to standards.

'A POTENTIAL TO EAT SILICON'

The smart-card believers are not dismayed. "The smart-card market could be the next personal computer for chipmakers," says Michael Zillott, marketing manager of Seeq. "It has that potential to eat silicon." Zillott himself, however, does not expect the market to develop until the 1990s, despite the example of the European and Japanese firms that are already doing a lively business.

"A lot of people in the United States are too far from the market," says Marya. "They don't see why you need intelligence on a card. But the French see, and the Japanese aren't far behind. The smart card is just as intelligent as you want it to be. It can be a bank card, a security card, an inventory card—anything." □

DREXLER KEEPS PLUGGING AWAY WITH 'DUMB' OPTICAL STORAGE CARD

While many companies wrestle with the development of the smart card, Drexler Technology Inc. is ready to start production of a "dumb" card—a storage medium that holds up to 4 megabytes of laser-written optical storage. Drexler's brand-new Mountain View, Calif., plant can churn out 30,000 cards a day and will be able to make 100,000 a day by next April. That kind of production would create quite a bottleneck, however, because at the moment there are only a hundred machines in the world capable of reading the cards, according to the company's president and founder, Jerome Drexler.

Help is on the way. Drexler has licensed two dozen firms to make readers since announcing the card in 1981, and a number of those companies, mostly Japanese, have started to introduce products. This year, the Sumitomo Bank began testing a cashless banking system using the LaserCard and a reader made by Olympus Optical Co.; Toshiba Corp. has announced both read-only and read/write equipment; and both Computer Services Corp. (CSK) and Nipponcoinco of Japan have announced $100 readers.

DREXLER: "Our card is the floppy of optical storage."

Drexler needs not only readers but also a second source for the cards before its new factory will be able to ramp up. Blue Cross of Maryland, which gave the LaserCard its first big push in May 1985 by agreeing to use it for medical records, told Drexler last July that it would not go into production until a second source had been signed.

Meanwhile, Maryland Blue Cross's LifeCard International subsidiary has also licensed technology rights to another laser card whose designers, Optical Recording Corp. of Toronto, say it can store 50 to 200 megabytes. The company says it will manufacture neither the card nor the readers, but is negotiating with 50 potential manufacturers of both, 25 of them in Japan. LifeCard will act as a distributor and will have first rights to any product arising from the technology.

For its part, Drexler, though it has energetically marketed licenses to make card readers, has retained rights to its cards, while nailing down the technology with a dozen patents. "Eventually, we will have half a dozen second sources," says Drexler—but the first one will have to make a commitment to build a $25 million plant, before the market has been established. To be willing to do that, Drexler concedes, "They will have to see a market." Drexler has no doubt that there is one; for two years, he has stuck to his prediction that 160 million cards a year will be sold by 1991.

Skeptics suggest that these are heady projections for a card that has never been field-tested (except by Sumitomo, whose test includes only 100 users and has just begun). But Drexler is already looking far beyond medical and financial applications, to using the cards in publishing and as an input/output device for personal computers and optical disks. A recent technical advance enabled the firm to double the amount of storage on the card, to 4 megabytes—meaning, Drexler points out, that the card can now store as many as 125 pages of graphic information as well as 800 pages of text.

"For the optical storage world, our card is the floppy disk," Drexler says. "Our biggest problem is shaking out of people's minds the idea that it looks like a credit card." *–Clifford Barney*

DOES CATALYST HAVE THE KEY TO SMART CARDS?

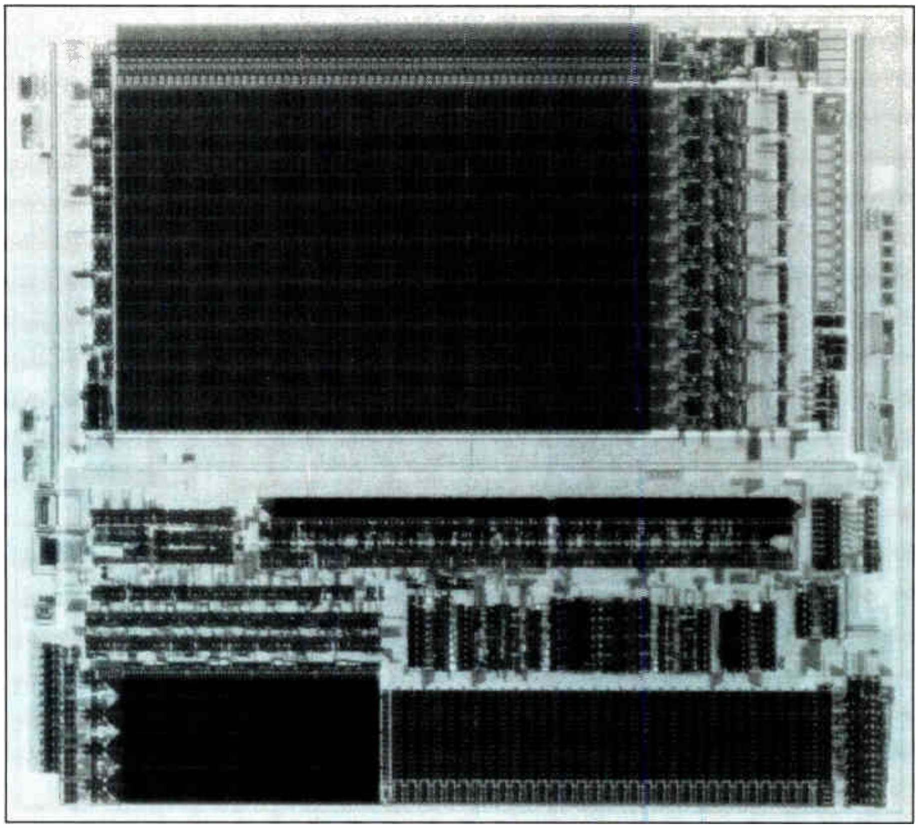
Catalyst Semiconductor thinks that its new chip, which meets ISO smart-card standards and has 2-K bytes of EEPROM, could finally open up the market

A tiny but powerful microcontroller from Catalyst Semiconductor Inc. may be the key that will unlock a worldwide billion-dollar business in smart-card chips. Measuring 4.5 by 5 mils by only 200 μm thick, the CAT61C580 chip is small enough to meet size requirements set by the International Organization for Standardization for smart-card applications, yet it packs 2-K bytes of electrically erasable, programmable read-only memory. That's at least four times the EEPROM of any other ISO-compliant smart-card chip now available using the same 2-μm CMOS design rules.

The Santa Clara, Calif., company achieved this density by stripping away the peripheral logic around the EEPROM and writing these functions into microcode. That left plenty of room for the 2-K bytes of EEPROM, and the chip is still about 30% smaller than competing devices that have only a fourth or less memory. What's more, Catalyst is working on an 8-K-byte chip, which will be made by shrinking the current 220-μm^2 EEPROM cell size to 80 μm^2 with a combination of proprietary design refinements and 1.5-μm geometries. The CAT61C580 is just being released; the 8-K-byte chip should be available next year.

Working in conjunction with joint developer Oki Electric Co., Tokyo, Catalyst designers modified an Oki microcontroller by adding a programmable logic array and 2-K bytes of EEPROM. (Fig. 1). They also managed to squeeze in 3-K bytes of ROM, 128 bytes of random-access memory, and enough electrostatic-discharge-protection circuitry to protect the chip from up to 15,000 kV, enough to protect against the static electricity generated by removing a credit card from a pocket or a billfold.

In addition, the CAT61C580 op-



1. LITTLE GIANT. Catalyst's 8-bit microcontroller is tiny enough for use in smart cards, yet it has an elephant's memory.

erates at the ISO-recommended frequency of 4.9 MHz with a high-speed instruction-cycle time of 813.8 ns, allowing it to run at the ISO's recommended 9,600 baud through a single serial input/output pin. Power dissipation of the 8-bit chip is only 20 mW.

The architecture of the chip allows asynchronous, two-way communications through a single serial I/O pin. This eliminates the need for a universal asynchronous receiver/transmitter and an interrupt, reducing the number of pins to only five—one third to one half of what's required in other approaches.

A TANTALIZING IDEA

The idea of EEPROM-based microcontrollers has long captured designers' imaginations because of the wide range of applications—not only for smart cards, but also for robotics, artificial intelligence, industrial controls, consumer products, and more. But so far, applications have been limited to a small number of niche markets for controllers, because of the small amount of EEPROM that could economically share the same chip as the microcontroller. Smart cards are one application that promises to allow EEPROM-based microcontrollers to break out of their niche; now that such a powerful chip that meets ISO smart-card standards exists, that breakout could be imminent. And with the increased memory that is promised, the chips will have a crack at the full range of potential microcontroller markets.

Catalyst president and founder B. K. Marya claims his is the only chip that meets, and in some cases exceeds, all of the ISO requirements for smart-card applications, including area, thickness, electrostatic discharge, power dissipation, and speed. Of these, the first three are the most critical, he says.

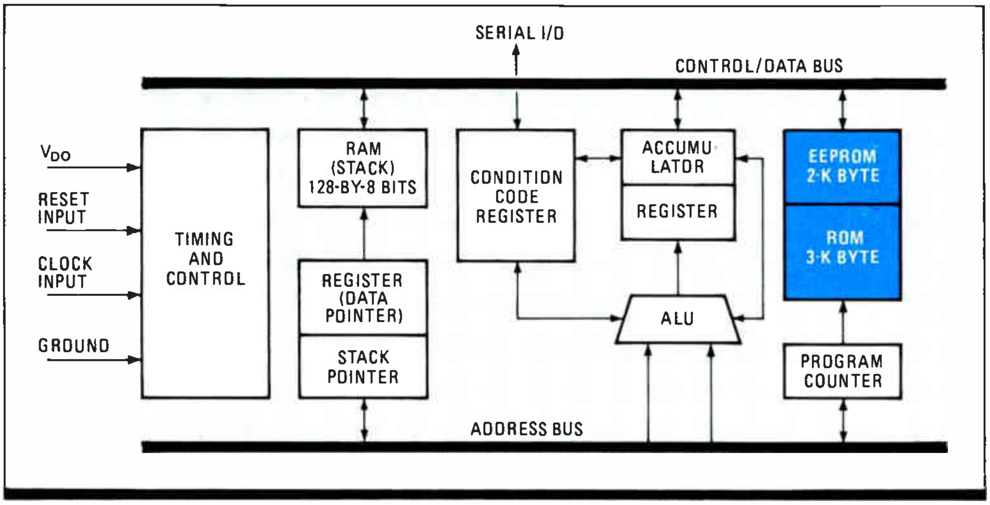
"The thickness must be no more than that of a standard credit card, 200 μm. And the area must not only be 5 by 5 mils or less, but [the chip must] be as square as possible, to prevent the possibility of breakage when the card is bent. In addition, the chip must be capable of withstanding the electrostatic discharge that builds up taking credit cards in and out of pockets and wallets." This buildup has been measured in excess of 10 kV, he says.

The 2-K-byte chip is aimed at a projected near-term market for smart cards that some estimate to be worth hundreds of millions of dollars (see p. 55). In a typical smart-card transaction, a card holder puts the card in a point-of-sale terminal. The terminal supplies the card with electric power and communicates to the card's microcontroller through pin contacts on the card's surface. The user is asked to enter a password. When the sale is rung up, the amount of the transaction is stored in the card's EEPROM, credited to the retailer's account, and debited from the card holder's credit balance, which is also stored in the card's memory. The card holder can replenish the credit balance at an automatic-banking machine.

What has held back the development of the EEPROM-based microcontroller market, Marya says, is the fact that, although stand-alone EEPROM parts of 16-K, 64-K, and 256-K densities are becoming commonplace, EEPROM-based microcontroller densities have trailed the stand-alone densities by at least four generations.

One way to achieve more on-board EEPROM is to advance the processing state of the art: scaling down the lateral dimensions from geometries between 2 and 3 μm to between 1.25 and 1.5 μm, and the vertical dimensions on the EEPROM from 150 to 250 Å down to 80 to 90 Å, which comes close to the limits at which EEPROMs operate reliably. The problem with this, says Marya, is that it requires manufacturers to push the process technology for microcontrollers beyond what is currently available even for stand-alone EEPROMs. And although such an advance is technically feasible for the high-volume applications that could use such large EEPROM/microcontroller combinations, the high cost of manufacturing such devices rules out their use. Marya says there is also the problem of reliability, which is critical for smart cards, where data integrity and security are important. So to make room for more EEPROM, Catalyst replaced the peripheral-function circuitry with microcode.

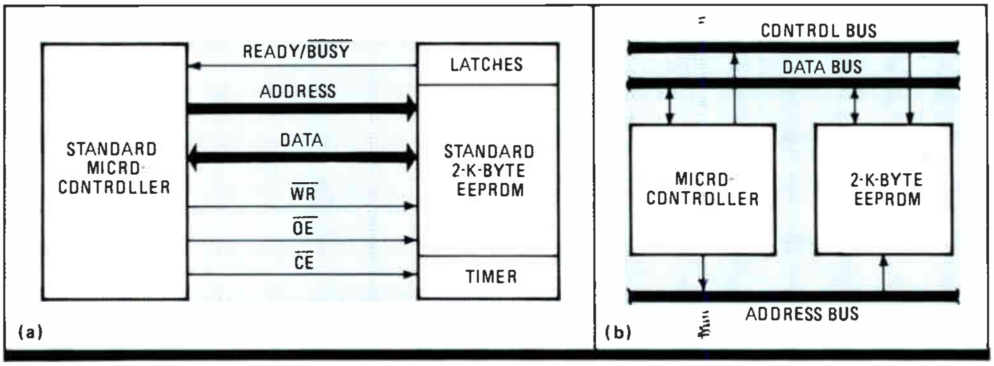
To get 2-K bytes of EEPROM into an ISO-standard smart-card chip, says Marya, "what is required is a fundamental rethinking of the architecture of EEPROM-based microcon-



2. ATTRACTIVE SWAP. By writing the latch, timer, and test logic functions into microcode, Catalyst designers were able to free up more than enough room on the chip for 2-K bytes of EEPROM.

trollers. Basically, most current implementations are 'brute-force' affairs combining the functions of an EEPROM and a microcontroller on the same chip, without any modification whatsoever."

By writing the functions of the EEPROM's peripheral logic into microcode, Catalyst has freed up real estate for more EEPROM. "Essentially, we have taken a standard EEPROM device, stripped off such peripheral circuitry as the latches, timers, and self-test logic, and incorporated these functions into the microcode of the on-board 8-bit microcontroller (Fig. 2), resulting in a 5-by-4.5-mm die size," says Marya. To achieve these breakthroughs, Catalyst designers came up with an architecture that differs from standard single-chip EEPROM/CPU implementations in five fundamental ways.



3. SIMPLIFIED BUS. By eliminating latches, timers, and test logic, the complex bus structure of a standard EEPROM-based chip (a) is replaced with a simpler three-bus arrangement (b).

First, even though it uses the same 200- to 250-μm^2 cell structure as the CPU, the 2-K-byte EEPROM takes up only half the area of the microcontroller. Second, the microcontroller's microcode has been expanded to include the latch, timing, and test functions usually associated with the operation of the EEPROM. Although this increases the area occupied by the microcode by 5%, eliminating the peripherals from the EEPROM circuitry saves 20% of the EEPROM's space.

Third, the bus architecture has been simplified. In the traditional one- and two-chip approach (Fig. 3a), at least six separate data, address, and control lines link the EEPROM and the CPU. Moreover, Marya says, the user has to provide necessary waveforms on control pins WE, OE, and CE, along with the valid data and address. The completion of programming is signaled via the RDY/BUSY pin, which has to be monitored by the microcontroller. In the CAT61C580, the interface between the CPU and the EEPROM is reduced to a three-bus structure (Fig. 3b), because the EEPROM's hard-wired latches and timer are eliminated. In addition, testing of the EEPROM is done internally, eliminating the need for test pads.

Fourth, the addressing scheme has been modified, says Marya, in that the EEPROM is above the ROM address space but, unlike the ROM, it is addressed through RAM. The addressing scheme is made efficient by eliminating page boundaries and providing both direct and indirect addressing of the RAM.

Finally, two additional registers have been added to the basic architecture: a B register to enhance the arithmetic logic unit's computation-intensive tasks, and a D register, which can be auto-incremented or -decremented to enhance the speed of the RAM's read and write operations. The 128-by-8-bit RAM provides 32 levels of nesting, and it can be used as a stack for pop and push operations.

WHAT'S IN THE MICROCODE

Most of the read, write, and erase functions are performed using two simple move commands incorporated into the CPU's microcode, MOV_1 and MOV_2. The first command transfers data from the internal RAM to the EEPROM, erasing previous data after receiving the appropriate 24-bit security code. The second command reads data out of the EEPROM locations and into the RAM. With these commands, EEPROM programming is made totally transparent to the user. "This transparency adds an additional level of security and reliability, since, unlike other implementations, the actual mechanism of writing into EEPROM is never revealed to the user," says Marya.

In addition to these special instructions, there are the 95 other housekeeping commands usually incorporated into a microcontroller: 55 one-byte instructions, 35 two-byte instructions, and 5 three-byte instructions. However, the instructions have been modified to reflect the chip's use in smart-card applications. The large number and smaller width of instructions provide more programming power to the user, and that's important in smart cards, where programming space is limited to on-board ROM, says Marya.

Security is also essential for smart-card applications, because the user stores important financial and personal information in the card's EEPROM. So Catalyst designers incorporated a set of special instructions into the microcode and a program into the on-board ROM that allows a three-level security scheme. "In a credit card application, this would make it possible not only for the primary user, say the financial institution, such as MasterCard or Visa, to have an access code, but the issuing bank and the individual card user as well—the first incorporated into the nonerasable ROM when the chip is sold to the issuing institution, and the other two inserted into the EEPROM when the card is issued to a customer," says Marya. "In any transaction, all three codes must be matched before any information is revealed to the user or any data is changed on the card—the first two between the card and the machine automatically, and the third by the user on request."

The high voltage for erasing and programming the EEPROM cell is generated on the CAT61C580, so the chip needs only a single power supply of 5 V. Fabricated with a 2-μm EEPROM process, which combines a 2-μm CMOS logic process with a conventional high-voltage two-transistor, floating-gate tunnel-oxide EEPROM process, the chip's EEPROM is specified for 10,000 program-erase cycles and 10 years of data retention. The process uses dual oxides—a thin oxide to obtain high-speed EEPROM read capability and a thicker oxide to withstand the 21 V required for erasing and programming the cell.

In this scheme, Marya says, the user can change his code at regular intervals, as can the issuing institution via the automatic teller machine. Also, the card-reading machine can be programmed to disqualify the card after a certain number of unsuccessful attempts to enter the code. In addition, he says, further levels of security can be incorporated into the EEPROM, such as specifying several individuals who are authorized to use the card, and their credit limits.

Catalyst is evaluating a number of strategies to take advantage of planned second-generation improvements. First, implementing the 2-K-byte architecture in 1.5-μm CMOS and using the 80-μm^2 cell that is now under development will reduce the die size of 2-K-byte devices by as much as 50%, while increasing the number of dice per wafer and lowering the cost of the finished devices. Alternatively, the same process improvements will allow an increase in EEPROM array capacity from 2-K bytes to 8-K bytes without substantially increasing the present die size. Finally, Marya says, the enhancements will allow fabrication of 16-bit microcontrollers with as much as 32-K bytes of EEPROM, opening a host of application areas that require real-time response, such as artificial intelligence, robotics, and high-performance industrial and military controllers. □

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

MARYA: THE MICROCONTROLLER COULD BE THE NEXT GREAT 'GIZMO'

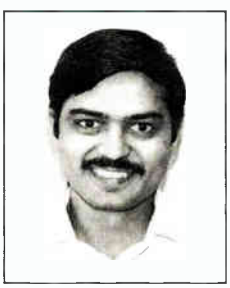
"For years the semiconductor industry has been looking for the electronic gizmo that would approach the dollar and unit volumes that digital watches, calculators, and video games generated," says Bharat Kumar Marya—"B. K." to his friends and associates. The president and founder of Catalyst Semiconductor Inc., Santa Clara, Calif., believes that smart cards are just the tip of the iceberg in a market for nonvolatile memory-based microcontrollers that he thinks may reach $2 billion a year by the mid-1990s.

Marya, 38, thinks that many observers expect growth to come from the wrong places. "Almost everyone has turned their eyes toward personal computers and work stations, which have quickly moved from 8 to 16 to 32 bits," he says. But as explosive as that market was at its beginning, it has begun to level off in terms of growth and penetration. Moreover, he says, the largest share of the profits went to original-equipment manufacturers and system integrators, not to chip manufacturers.

"The only market that has a good chance of recreating the bonanza of dollars and unit volumes of the past is the market for smart integrated-circuit cards built around EEPROM-based, 8-bit microcontrollers," says Marya, who points out that there are some 200 million banking and credit cards in circulation. He projects that by 1990 about 25% of these cards will be integrated-circuit-based. Beyond this, he says, there are other potentially huge replacement markets, such as telephone credit cards, as well as new applications, such as health-history cards, warranty cards, security cards, military dog tags, welfare cards, and passport cards.

B. K. MARYA

Although many of these potential IC-card applications are already being test-marketed in Europe and Japan, Marya says, the major market will ultimately be the U. S. "Ironically, virtually no U. S. semiconductor company, with the exception of some tentative efforts on the part of Motorola, is taking steps to participate in this market," he says. "U. S. companies must act fast, or we'll lose another major market."



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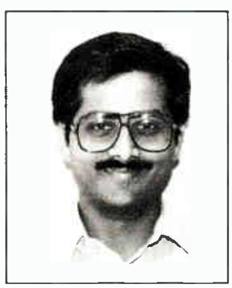


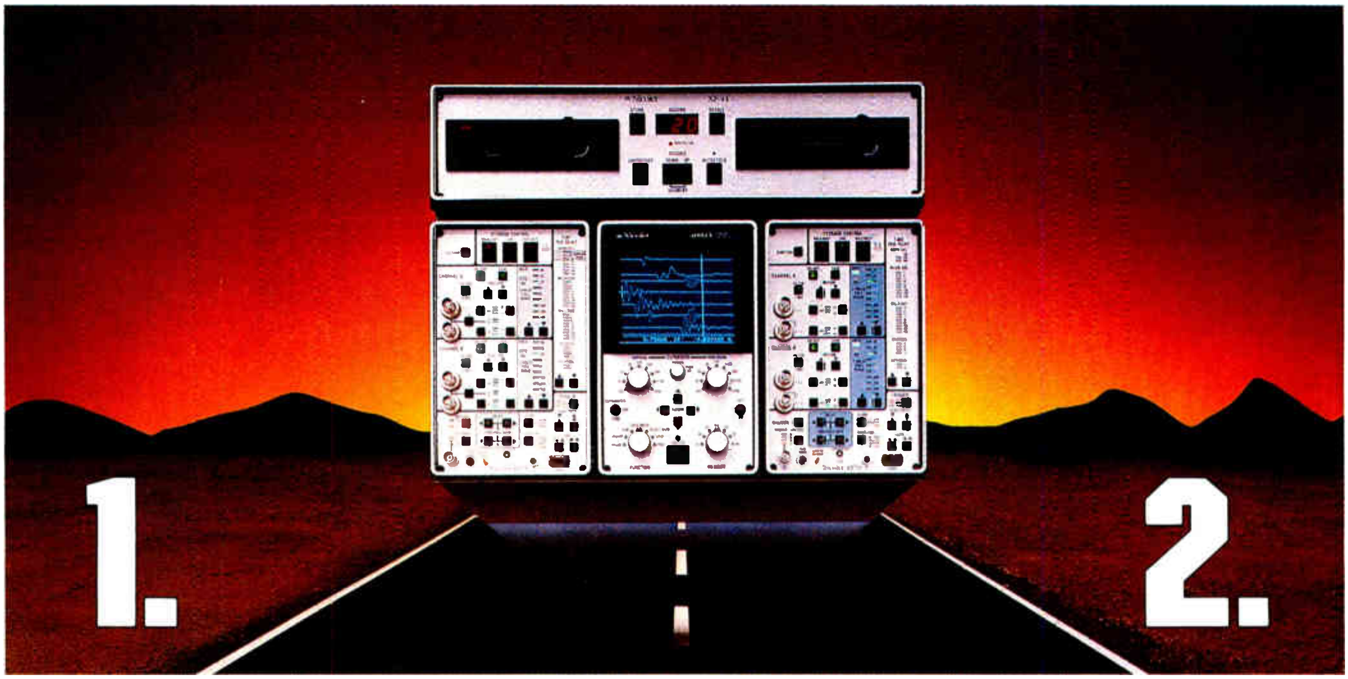
NAGESH CHALLA

To enter Catalyst in this market sweepstakes, Barya set up a joint development agreement with Oki Electric Co., Tokyo, 18 months ago. "We provided the basic architecture modifications, the circuit design, and the EEPROM expertise," he says. "They provided the process and fabrication capability."

Maintaining communications and schedules for the joint project required many transoceanic flights by Marya, design manager Nagesh Challa, Catalyst senior design manager Samir Patel, and Tomoaki Yoshida, an Oki section manager in Japan.

Catalyst is Marya's second startup. His first, Exel Semiconductor, an EEPROM and EPROM manufacturer, was acquired this year by Exar Inc. Marya earned a BSEE from Punjab University, India, and an MSEE from the University of New Mexico. He has since directed the design, construction, and operation of fabrication lines at several companies, including Hewlett-Packard, National Semiconductor, Synertek, and Seeq Technology.

THE FIRST NAME IN DIGITAL SCOPES



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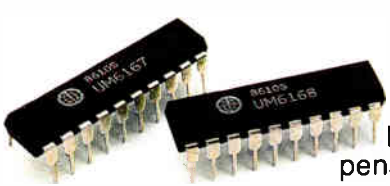

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HOW LINEAR IC DESIGNERS ARE BUILDING DENSER CHIPS

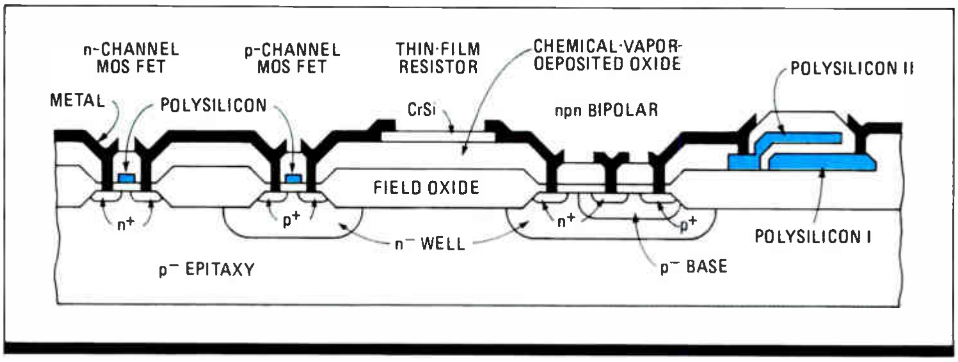
Linear functions do not scale down as well as digital functions. Nevertheless, systems designers have issued a density challenge—and it is being met

by Bernard Conrad Cole

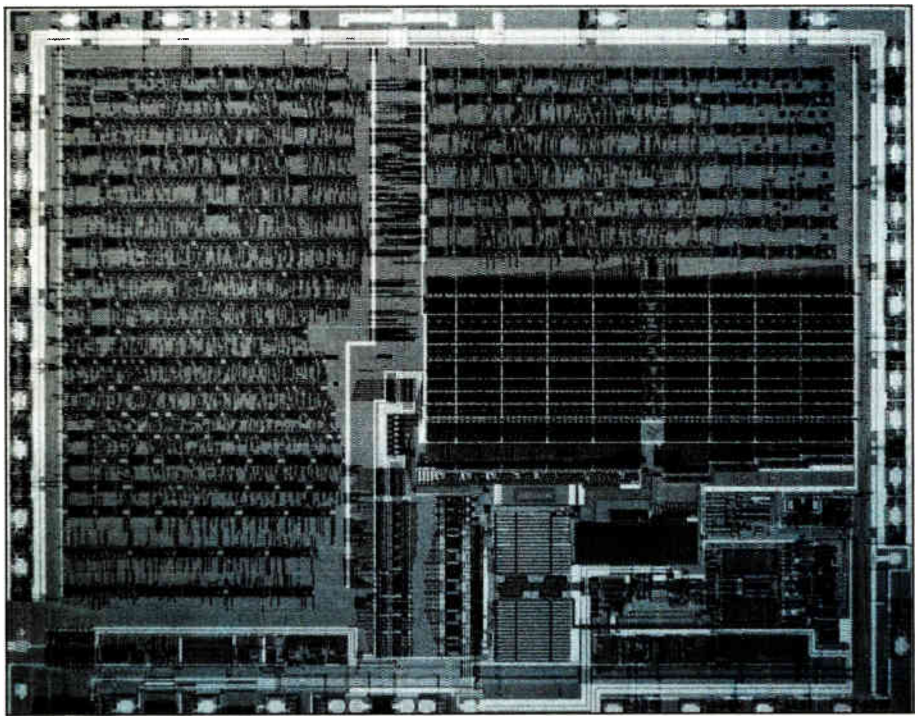
Like it or not, linear-circuit designers are being pushed into the VLSI era. Doing the shoving are system developers who keep demanding higher functional densities, higher speed, better accuracy and resolution, and easier-to-use devices. It's not an easy move for the IC designers; the characteristics that make a good digital process do not necessarily allow the design of good linear functions. Linear circuits are much more sensitive than digital circuits to second-order effects, such as those that come with scaling down transistors to smaller dimensions.

Despite those difficulties, linear-circuit designers are rising to the challenge with two approaches: scaling down existing 3- and 5-μm processes to 2 and 3 μm, and optimizing 1- and 1.5-μm VLSI processes for the fabrication of linear functions. Their solutions cover a wide range. Some designers are trying to optimize linear CMOS processes for high-density digital functions; others are taking high-density CMOS processes and trying to improve their linear characteristics; and still others are betting on a higher-performance mix of bipolar and CMOS. In terms of architecture, some are implementing linear subsystems on a chip, allowing digital designers to program a linear device as if it were a microprocessor peripheral. Where calibration is needed, designers are using digital calibration schemes based on nonvolatile memory, or devising sophisticated self-calibration schemes that allow devices to adjust and compensate automatically for errors.

The problem of implementing linear circuits at LSI and VLSI densities is particularly critical in CMOS, which is approaching 1-μm dimensions on the digital side. "As currently implemented, sub-2-μm digital CMOS, let alone 1-μm, does not allow the design of good linear functions," says Dave Fullagar, vice president of research and development at Maxim Integrated Products Inc., Sunnyvale, Calif. Whereas digital circuits are running into problems at 1 μm, linear



1. LINEAR VLSI. Aiming at densities approaching digital VLSI, General Electric has developed a 1.25-μm linear CMOS process using molybdenum-based resistors and isolated metal-to-metal capacitors.



2. LINEAR SUBSYSTEMS. Crystal Semiconductor's linear VLSI-based data acquisition system on a chip eliminates many external linear and digital functions.

circuits run into the same problems much sooner, at around 2 μm or so. As a result, says Fullagar, "most linear designers are happy enough with 3- and 4-μm CMOS processes, which are well understood and allow fabrication of good, reproducible, and reliable linear functions."

But, having achieved such high levels of integration on the digital side, systems designers are pressing to integrate high levels of linear functionality on the same chip, says Wayne Foletta, strategic marketing manager at Fairchild Semiconductor Corp.'s linear division in Mountain View, Calif. "And if that is not possible, at the very least they are asking that the stand-alone linear ICs move to a higher level of integration, incorporating the functions of several small- and medium-scale-integration devices in a single linear LSI or VLSI circuit."

SCALING DOWN CMOS

To meet these demands, several companies, including Texas Instruments, National Semiconductor, Fairchild, and General Electric, are scaling down their linear CMOS processes. At TI in Dallas, process engineers have developed a second-generation 3-μm LinCMOS process to meet the needs of complex data-acquisition and telecommunications applications requiring a high degree of analog and digital functional density on the same chip (see p. 71). Fabricated in a p^- epitaxial layer grown on a p^+ substrate to improve density and speed while at the same time reducing latchup, the Advanced LinCMOS process will be used to manufacture a new family of 8-bit analog-to-digital converters, plus a host of other standard and custom ICs.

Similarly, National Semiconductor, Sunnyvale, Calif., is moving into production with its new 2-μm LMCMOS process featuring the use of channel stops and lightly doped drain extensions to increase breakdown voltage to more than 60 V while retaining high-speed operation. It is used to fabricate quad analog switches that can handle rail-to-rail signals on supply voltages up to 20 V; a new series of switched-capacitor filters; and an 8-bit ADC with 19 multiplexed inputs and a serial data interface.

At Fairchild Semiconductor Corp., Mountain View, Calif., engineers in the Linear Division are moving into production the company's second-generation 2-μm linear CMOS process. LCMOS II features two-layer metal interconnections using a titanium/tungsten metallization scheme; differential oxidation of polysilicon gate, source, and drain regions; and self-aligned siliciding of the source and drain regions and polysilicon interconnect regions. The process is aimed at fabricating complex linear and digital functions, such as modems and other communications circuits.

Taking a step past the current 2- to 4-μm processes being considered in the industry, GE is proposing to push the state of the art in linear CMOS to 1.25 μm by taking a digital VLSI process and optimizing it for linear functions. At GE's Corporate Research and Development Center in Schenectady, N.Y., researchers have developed a two-layer metal process (Fig. 1) that incorporates molybdenum-based resistors and isolated metal-to-metal capacitors—both of which are critical elements in many linear circuits.

So far, GE is going it alone with a pure CMOS approach to a sub-2-μm linear VLSI process. Even its Silicon Valley subsidiary, Intersil Inc., is ramping up a mixed bipolar-CMOS production line alongside its traditional CMOS facility. Also following this route are Analog Devices, Fairchild, Honeywell, and Micropower Systems [*Electronics*, Dec. 28, 1985, p. 35].

Neither CMOS nor bipolar will yield higher levels of integration alone, says Robert Albertson, product manager for data-acquisition ICs at Intersil, Cupertino, Calif. "In many respects, linear bipolar scales better than linear CMOS," he says. "But, important for combined linear-digital designs, CMOS gives you high density, while bipolar gives you high performance." So many traditional linear houses, such as Burr-Brown Inc. of Tucson, Ariz., are preparing for an eventual merging of bipolar and CMOS by developing traditional linear CMOS product lines in addition to their linear bipolar products. Others are looking at mixed CMOS-bipolar processes to get a good balance of high functional density and good linear characteristics in the near-1-μm range. Included in this category are Analog Devices, Fairchild Semiconductor, Honeywell, and Micropower Systems [*Electronics*, Dec. 28, 1985, p. 35].

These new linear VLSI processes are most dramatically impacting the design of mixed linear and digital circuits, such as telecommunications ICs and data-conversion devices. On the one hand, the higher functional density is making possible the fabrication of what Michael J. Callahan Jr., vice president of engineering at Crystal Semiconductor Corp. of Austin, Texas, calls "smart analog," but which might more accurately be described as linear VLSI subsystems on a chip (Fig. 2). On the other hand, the higher functional density is opening up new horizons for linear circuit designers in coming up with new and innovative ways to ensure greater accuracy and resolution, using techniques such as on-chip EPROM and self-calibration using weighted capacitor arrays.

Linear subsystems on a chip, which are under development by companies such as Crystal Semiconductor, Linear Technology, and Micro Linear, are being approached from two directions. In one approach, data conversion is being simplified by the incorporation of additional linear functions, such as the track-and-hold circuitry, the analog multiplexers, trimming circuitry, and potentiometer functions. In the other approach, the interface to the digital world—especially to microprocessors—is being simplified through the inclusion on board of not only the digital timing circuitry, but a full digital interface.

More than just a set of input and output lines modified to reflect the protocols of various microprocessor buses, this digital interface block on an analog-subsystem chip may include registers and microsequencer control logic. "What this allows the system designer to do is to program and select specific converter features in a manner similar to that on any microprocessor peripheral," says John R. Croteau, data-acquisition product manager at Crystal Semiconductor.

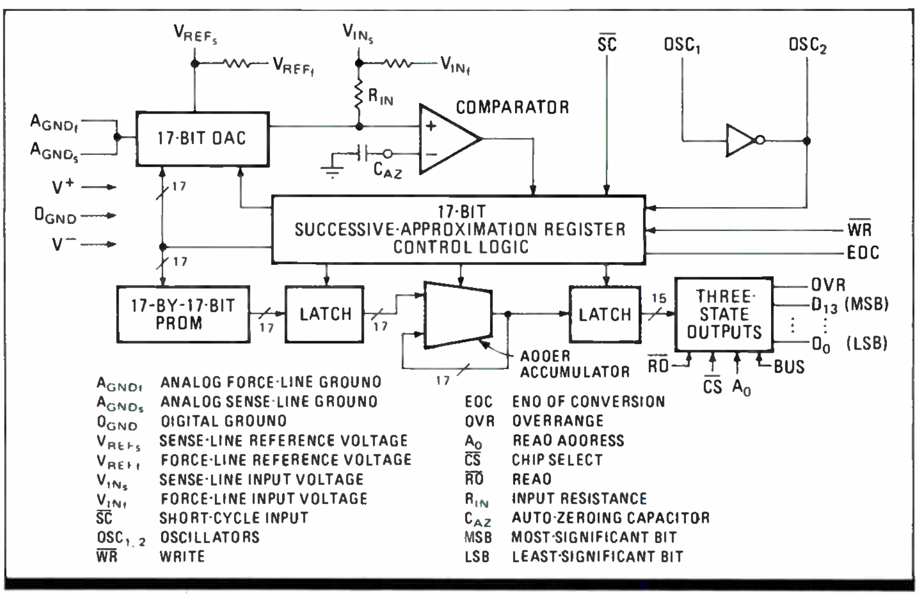
The other effect of such linear VLSI CMOS processes on mixed linear and digital applications such as data conversion is that it has given designers the freedom to consider other alternatives to zener zapping and laser trimming. Zener zapping and laser trimming are currently used to trim circuits and bring them within specified parameters after fabrication. The problem with these techniques is that they also introduce stresses and modifications to the silicon which affect offset, gain, and linearity. Moreover, the packaging and potting introduce additional errors, requiring manual calibration using external passive components to compensate for offset, gain, and linearity errors, says Charles Gopen, marketing vice president at Micro Linear Corp., San Jose, Calif.

These alternatives to zener zapping and laser trimming have resulted in the emergence of 12- to 16-bit accuracy in monolithic data converters, a level previously available only from hybrids. To get these accuracies, two approaches are being considered: open-loop systems similar to present configurations, but with a digitally based electrically erasable read-only memory used for calibration purposes; and closed-loop, self-calibration schemes that cancel out the inherent errors of data-acquisition devices.

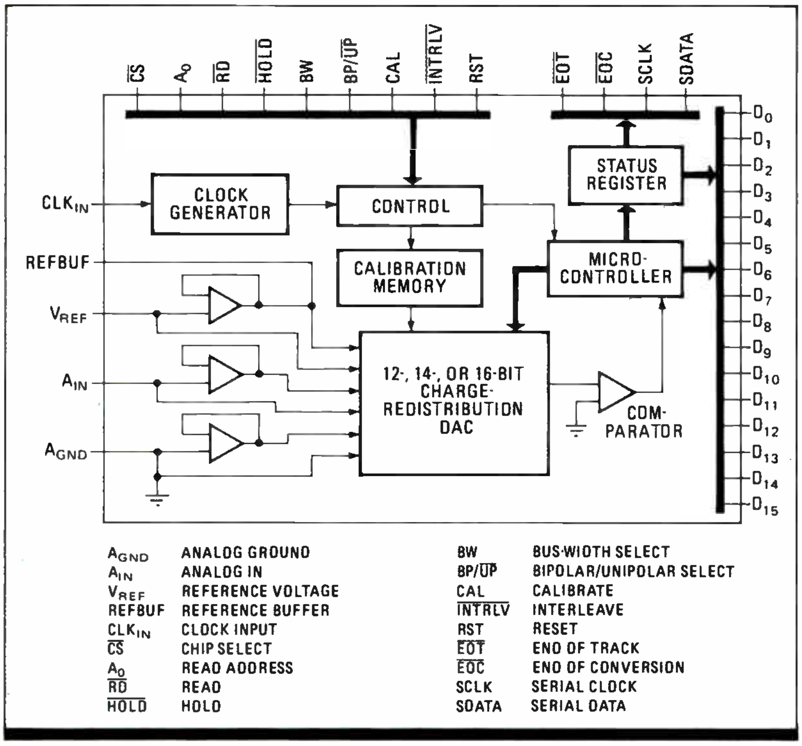
EPROM-BASED CALIBRATION

Intersil, a pioneer in EPROM-based calibration in data converters, is using the technique in two 14-bit products: the ICL7115 ADC (Fig. 3) and the ICL7134 digital-to-analog converter.

In the ICL7114, combining a 17-by-17-bit EPROM with a thin-film, 17-bit, low-accuracy DAC implemented with a modified R-2R resistor ladder scheme produces redundant DAC codes that cover the analog output range, without any missing codes. Each bit value of the DAC is compared internally with an accurately calibrated input voltage, which is entered as a 17-bit word into the on-chip EPROM. A comparator decision to keep what it has determined to be a "good" bit causes the corresponding bit value to be accessed from the EPROM and added into the accumulator's register, while a decision to drop a "bad" bit leaves the accumulator's contents un-



3. CALIBRATION EPROM. By replacing laser-trimmable resistors with EPROM, Intersil's converter gets 14-bit accuracy.



4. SMART ANALOG. Crystal Semiconductor combines self-calibration and on-chip controller and registers to achieve 16-bit accuracy.

changed. At the end of the conversion, the accumulator contains the sum of the values of the bits that were kept, representing the true input voltage. The 17-bit result is rounded off to 14 bits at the end of the conversion.

In Intersil's ICL7134 DAC, the on-board EPROM controls two error-correction DACs, the outputs of which are summed with that of the primary DAC. The accuracy of the first DAC can be as low as 9 bits. The EPROM contains 31 correction codes, one of which is selected for each combination of the most significant 5 input bits of the primary DAC. Not only is the linearity of the device calculated to less than ±½ least-significant bit, but also the superimposition errors and the nonlinearities inherent in the internal feedback networks are all corrected by the same memory-coding scheme, says Intersil's Albertson.

In both devices, calibration programming of the memory space can be done after packaging and burn-in, which means that unlike in present laser-trimming, zener-zapping, and link-busting schemes, errors induced by potting pressures and thermal stresses can also be corrected. Moreover, Albertson says, none of the on-chip bit-setting resistors is disturbed in the memory-programming processes.

As an alternative, many companies are taking advantage of the density improvements possible with their second-generation linear CMOS processes to move from resistor-based architectures to more self-calibrated methods that use switching-capacitor charge redistribution for bit-weighting. These methods require more area than EEPROM-based calibration.

Self-calibrated ADCs and DACs employ calibration cycles in which each bit is analyzed and checked for systematic errors generated by the random discharges of capacitors during periods when the device is not in use. These errors are then converted to a digital representation and stored for use in later conversions. In subsequent normal conversion cycles, an analog error signal is subtracted from the input signal. This error signal is generated by an error-correction DAC whose input is the sum of all the stored error signals corresponding to bits with the value of "1." The result is an input accuracy equivalent to a perfect capacitor array, one that produces no randomly generated or systematic error signals. The advantage of this approach, says Crystal Semiconductor's Croteau, is that calibration cycles need to be executed only infrequently, requiring only about 5 or 10 times the time of a normal conversion, and can thus be executed in a transparent manner between normal, sparsely timed conversions.

The self-calibration scheme that TI plans to use in its soon-to-be introduced family of 8-bit ADCs, for example, contains a calibration DAC based on such a bit-weighted capacitor approach. The calibration DAC compares the value of the charge on the most-significant-bit capacitor to the sum of the lesser capacitors. If their values are not equal, the difference is measured on the comparator and the comparator DAC, and the result stored in an on-chip 120-bit static random-access memory. Each capacitor in the array is tested similarly, in sequence. During signal conversion, the calibration DAC injects the error voltage stored in RAM into the comparator to cancel the capacitor error. As successive capacitors in the primary DAC are switched in, their error is retrieved from RAM and accumulated with the error of the other capacitors. The calibration DAC uses a digital accumulator to generate the total analog error correction, which is then injected into the comparator.

COMBINATIONS FOR CALIBRATION

A taste of things to come is Crystal Semiconductor's CS5016 (Fig. 4), a self-calibrating ADC subsystem on a chip that automatically provides true 16-bit accuracy over the full commercial temperature range. It achieves this by combining the switching-capacitor charge-redistribution technique with a track-and-hold amplifier, a microsequencer, and associated program registers. The microsequencer manipulates the capacitive DACs to trim the offset, gain, and linearity errors. Calibration can be directly controlled by the user by programming the program registers, or the chip can be placed in a mode where calibration occurs automatically and continuously. □

TI PROCESS BOOSTS LINEAR CMOS ICs TO LSI DENSITIES

The Advanced LinCMOS process gives the densities needed for high-performance data converters and other complex chips that combine analog and digital circuitry

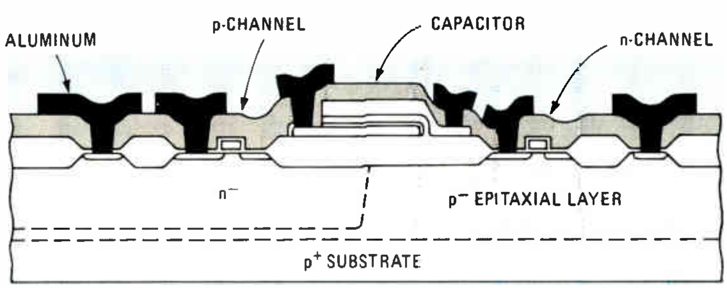
Linear CMOS is blasting off for the realm of large-scale integration at Texas Instruments Inc. The Dallas company has scaled down minimum feature size to 3 μm in its Advanced LinCMOS process, from 5 μm in the first-generation LinCMOS. Now it can achieve the density levels needed for complex data-acquisition and telecommunications chips and other high-performance integrated circuits requiring the use of combined analog and digital circuitry.

Besides shrinking the LinCMOS process, TI technologists went to a low-resistance epitaxial layer instead of bulky guard rings between n- and p-channel devices. They also reworked the capacitor and resistor structures so that these devices occupy only a fourth of the area of equivalent devices in the older LinCMOS technology [*Electronics*, April 5, 1984, p. 145]. These improvements will make possible such new chips as high-resolution data converters that are not significantly larger than current converter ICs with lower resolution.

The TI engineers also developed process improvements that give IC designers a choice of two high voltages—10 and 15 V—in addition to the 5-V digital level. LinCMOS offered only 10 and 5 V, and designers had to choose between them. With Advanced LinCMOS, designers can use any two of the three voltage levels on the same chip, dramatically increasing their design options.

Advanced LinCMOS will also permit chip designers to make better use of switched-capacitor technology, opening the door to the implementation of highly advanced switched-capacitor filters with more poles on chip. For example, when applied to the fabrication of the TCM29C13 codec-filter combination, the scaled-down Advanced LinCMOS reduces chip size 42%, compared with versions fabricated using the original process. The performance of the new codec-filter IC also is significantly improved. Active power use is 6 mA compared with 8 mA in the older part, and standby power use is 0.8 mA versus 1.2 mA. Idle channel noise on the receive side is 5 dBrnc0 compared with 7 dBrnc0 in the earlier device, and on the receive side 11 dBrnc0 versus 12 dBrnc0.

The new linear process will also allow the cost-effective fabrication of high-speed single-chip products, such as



1. NEW LOOK. In Advanced LinCMOS, use of an epitaxial layer reduces latchup and eliminates need for guard rings between n- and p-channel devices.

modems that combine digital and linear circuitry. Such a chip should provide a wider dynamic range than current combos—opening up new applications such as high-speed modems based on digital-signal-processing techniques and devices that can encrypt telecommunications signals.

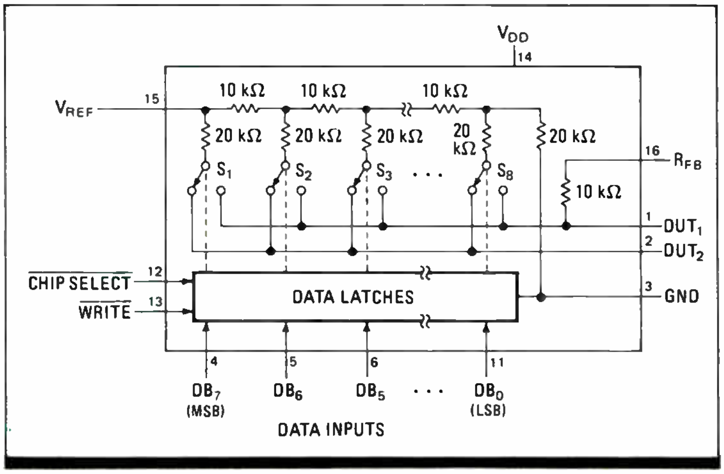
Most significantly, Advanced LinCMOS will open the way to the cost-effective manufacture of high-performance data-acquisition products using self-calibration techniques. With the increased packing density, there will be room on chip for circuitry that allows automatic calibration of some or all of the bits. Self-calibration will make it possible to produce 12- to 16-bit chips providing the sub-30-μs performance required for instrumentation applications without resorting to the expensive thin-film-resistor and

The packing density of Advanced LinCMOS will make room for on-chip self-calibrating circuitry in place of expensive thin-film resistors and laser-trimming techniques

laser-trimming techniques that must be used today to produce such high-resolution parts.

Reducing feature sizes is a straightforward approach to improving speed and to increasing packing densities, thereby increasing functionality while maintaining a cost-effective die size. The Advanced LinCMOS team identified 3 μm as the minimum size capable of meeting its requirements. At smaller dimensions, the analog performance of the scaled transistors is inadequate, TI says. So 3 μm is the appropriate size, even though advanced digital-only processes have moved into the 1-μm region.

Like its predecessor, Advanced LinCMOS is a silicon-gate, double-level-polysilicon process (Fig. 1). However, where the n-well of LinCMOS is fabricated in a p-substrate, the n-well of the twin-well Advanced LinCMOS is fabricated in a p^- epitaxial layer grown atop a p^+ substrate. It reduces the critical spacing of n^+ to n^- and p^+ to n^- regions.



2. NO FILM. An Advanced LinCMOS 8-bit DAC can use a well-matched polysilicon resistance ladder, eliminating costly thin films.

The use of the low-resistance epitaxial layer reduces latchup susceptibility and eliminates the need for guard rings between n- and p-channel devices. Because an LSI part contains many more individual transistors than a small- or medium-scale IC, single or multiple guard rings for each transistor would occupy a considerable portion of the total chip real estate.

Even though epitaxial material is more expensive than conventional material, its cost is less than the additional silicon required to incorporate guard rings on LSI devices. As a rule of thumb, the cost of an IC increases linearly with chip area up to 35,000 mils^2. But above 35,000 mils^2, the cost rises exponentially. So low-resistance epitaxy allows chip makers to hold down the chip size for both high yield and low cost while guarding against latchup.

Reducing feature size and substituting low-resistance epitaxial material for guard rings are important steps, but they are not enough to increase packing densities and maintain economical die sizes in components containing extensive analog circuitry. Both data-acquisition and telecommunications chips rely heavily on resistors and capacitors, so the capabilities of these components must be extended to keep die sizes within bounds.

One of the principal virtues of the original LinCMOS process is the control it gives chip designers over the capacitance of each of the two polysilicon layers. Designers also can modify the thickness of the second gate oxide without affecting the capacitors in the two poly layers. This independent control offers more versatility for implementation of complex ICs.

However, adding just a single bit of resolution to an analog-to-digital converter requires twice the capacitor area when the process technology uses binary-weighted switched capacitors, as does LinCMOS. Moving from 8 to 10 bits of resolution would require four times more capacitor space, which could make an ADC too expensive to be used in many applications.

So the TI technologists who developed the advanced LinCMOS process worked out a new capacitor structure consisting of an oxide-nitride sandwich. Thinning the capacitor's oxide layer is key to increasing its unit capacitance, since capacitance is inversely proportional to the thickness of the capacitor oxide. The result is an effective oxide thickness that is just a fourth that of the straight-oxide capacitors in LinCMOS and a fourfold increase in capacitance per unit area—all without significantly increased chip size.

Changes in the resistor implant dosage of Advanced LinCMOS have quadrupled sheet resistance, or resistance per unit area. With this improvement, a resistor of a given value can be made in just a quarter of the area required by LinCMOS technology. This improvement is the result of a design tradeoff made to increase sheet resistance while maintaining the temperature coefficient of expansion and retaining matching values comparable to the desirable performance of LinCMOS resistors.

While scaling down Advanced LinCMOS thinned the gate and made possible the 3-μm minimum channel length, it also required the development of proprietary process enhancements to provide the required breakdown voltage and the targeted speed improvements. Moreover, operating voltages of linear ICs typically are higher than the 5 V common to digital circuits, and thicker gate oxides are commonly used to increase breakdown and operating voltages. TI has taken its process a step further by developing techniques for Advanced LinCMOS that make it possible to employ both thick and thin oxides on the same chip. Such an IC can handle a relatively high voltage and a lower voltage without requiring excessive silicon real estate.

With the Advanced LinCMOS process, chip designers can use either the first or second polysilicon level to provide the thick or thin oxide. The use of two oxides and selectively scaled transistors on the same die allows TI's chip designers to tailor the breakdown voltages of n-channel transistors. (P-channel transistors generally are not the limiting factor in CMOS technology.) Thin gate oxides and transistors with short channel lengths can be used for high-speed, low-voltage logic circuitry on one part of an Advanced LinCMOS chip, and devices with thick gate oxides and longer channel lengths can handle higher voltages elsewhere on the chip.

In this way, transistors with three recommended operating voltages can be produced: 5 V, using thin oxide in a transistor with a 3-μm channel length; 10 V, using thin oxide in a transistor with a 4-μm channel length; and 15 V, using thick oxide in a transistor with a 7-μm channel length. The older LinCMOS process has two operating-voltage options: 5 or 10 V. The breakdown voltage is 30 V for Advanced LinCMOS, versus 20 V for the earlier process. TI says speeds improve by about 30%.

An example of what TI's Advanced LinCMOS brings to the game is an 8-bit digital-to-analog converter under development at the company. An enhanced, second-source version of an industry-standard device, the Advanced LinCMOS product is 25% smaller than the original and has a settling time 40% faster. The DAC uses an R-2R resistance ladder (Fig. 2) fabricated in polysilicon. The high sheet resistance and good matching characteristics of Advanced LinCMOS resistors enable TI to use this approach, rather than a costly thin-film technology.

In the new DAC, TI process engineers needed to build a chip with control logic that could be interfaced to the relatively high voltages in the outside world, while providing elsewhere on the same chip the scaled-down transistors necessary for efficient, low on-resistance switches. Thanks to the flexibility inherent in the Advanced LinCMOS process, they could tailor the chip's transistors to the different roles.

The engineers also decided to trade off the digital performance of the device's control logic for higher voltage capabilities. Scaling up the digital transistors is accomplished in Advanced LinCMOS by increasing the oxide thickness and channel length of the transistor. This trade-off still allows the new DAC to be 40% to 50% faster than competing devices. □

THE PATH TO A BETTER LINEAR CMOS PROCESS

A new family of innovative telecommunications chips: that was the goal at Texas Instruments Inc. But to build those circuits, TI engineers needed a revised linear CMOS process that could produce single chips to handle the complexity of telecom functions.

TI's existing LinCMOS technology is the company's linear process workhorse, used in more than 200 standard and custom integrated circuits. But with a 5-μm minimum feature size, it could only produce medium-scale ICs. So TI's process-development branch, working with the telecom design engineering group, decided to develop Advanced LinCMOS with 3-μm minimum features.

"We achieved a more streamlined process that lays out 30% to 40% tighter than our current LinCMOS process and applies itself well to virtually every linear and telecom part we have looked at," notes Lou Izzi, senior designer on the project. Harry Davoody, system-engineering branch manager, agrees. "Before Advanced LinCMOS, we were unable to integrate the kinds of complex products that we can now. Advanced LinCMOS technology has given us the capability to offer our customers cost-effective systems solutions with catalog parts and custom circuits, telecom and a-to-d—you name it."

The process development took about 18 months, but the payoff has been big. With the high-end telecom chips and custom parts, "we are utilizing the process in product areas we never imagined before. It has really proved to be a winner," says Davoody.

Izzi, a senior member of TI's technical staff, is manager of the data-acquisition design section. A graduate of New York Institute of Technology in 1977 with a BSEE, he has served as senior designer for the development of many telecommunications and custom ICs.

Davoody is responsible for the definition of new telecom and data-acquisition products and technical support for linear customers. A graduate of the University of Texas at Arlington with a BSEE, he is working on an MBA at the University of Dallas.

THE GENESIS. Izzi (left) and Davoody needed LSI density.

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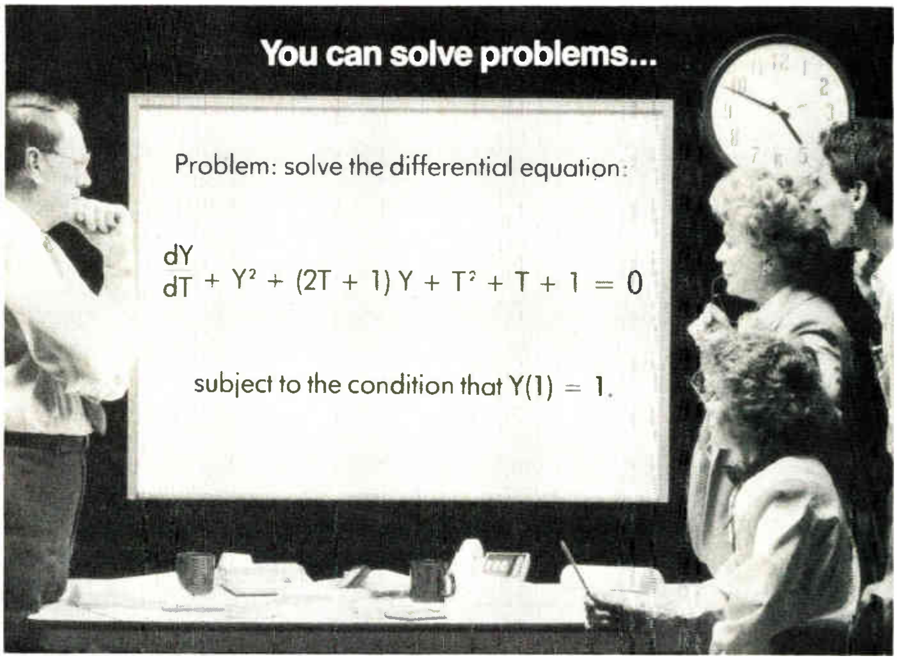

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(C1) DEPENDS(Y,T)$

(C2) DIFF (Y,T)+Y^2+(2*T+1)*Y+T^2+T+1;

(D2) $\frac{dY}{dT} + Y^2 + (2T + 1)Y + T^2 + T + 1$

(C3) SOLN:ODE(D2,Y,T);

(D3) $Y = -\frac{\%C\,T\,\%E^T - T - 1}{\%C\,\%E^T - 1}$

(C4) SOLVE(SUBST([Y=1,T=1],D3),%C),NUMER;

(D4) [%C = 0.5518192]

(C5) SPECIFIC_SOLN:SUBST(D4,SOLN);

(D5) $Y = -\frac{0.5518192\,T\,\%E^T - T - 1}{0.5518192\,\%E^T - 1}$

and Numerically.

```
(C6) FORTRAN(D5)$
        Y = -(0.5518192*T*EXP(T) - T - 1)
     1      /(0.5518192*EXP(T) - 1)
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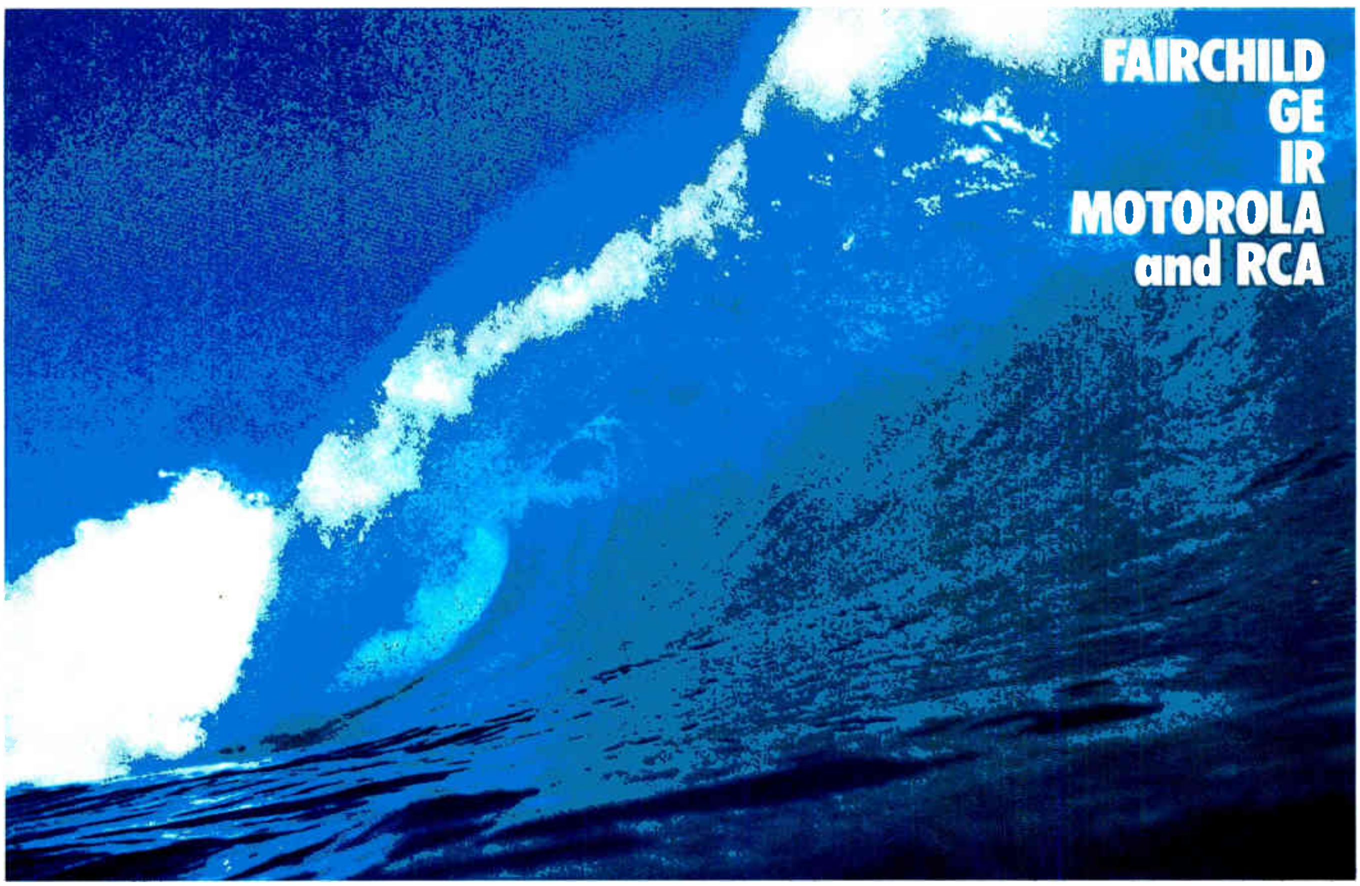

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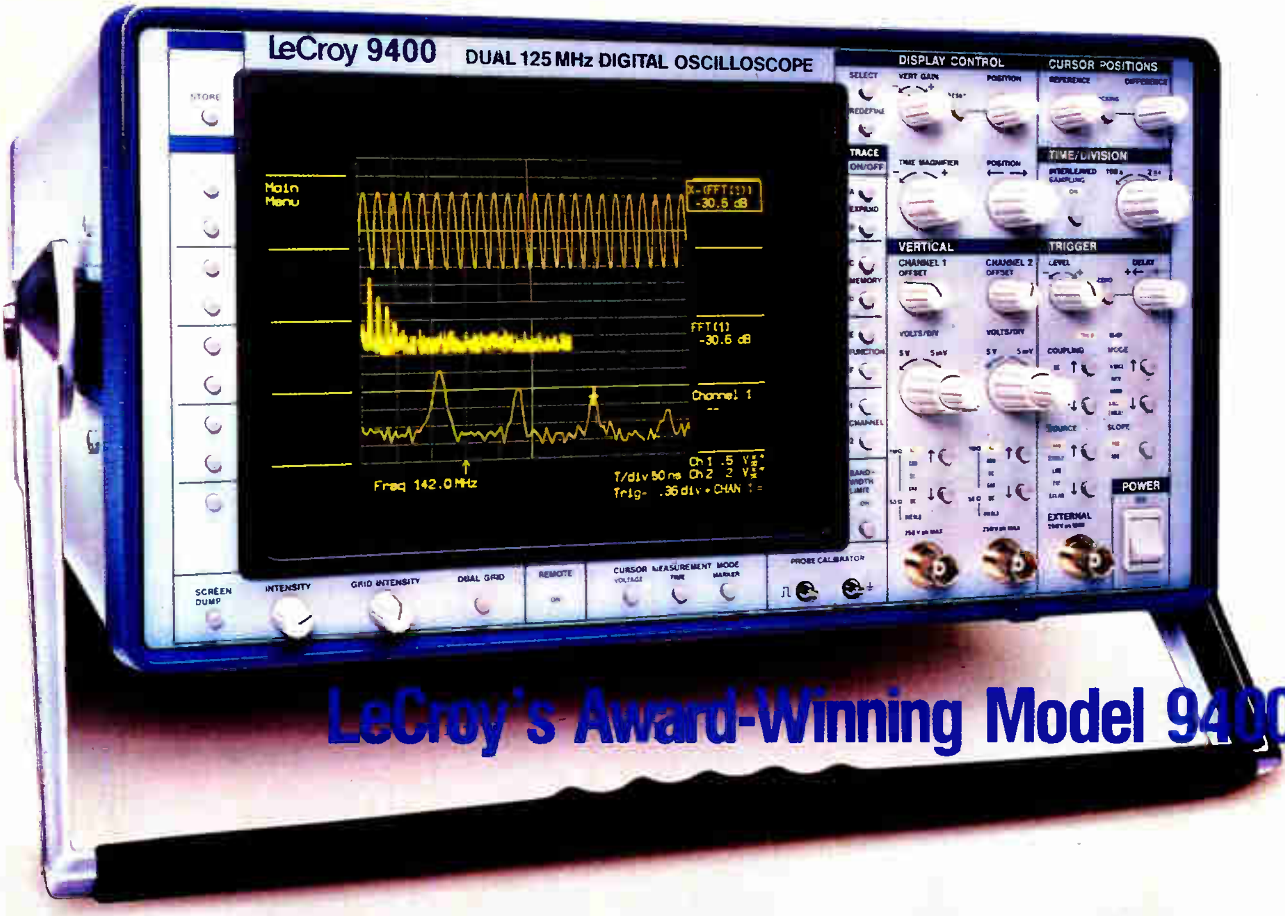

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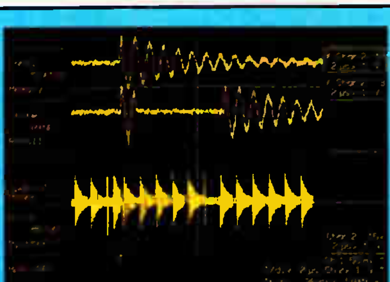
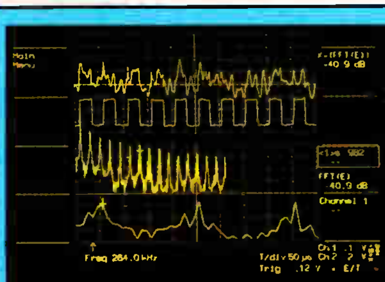
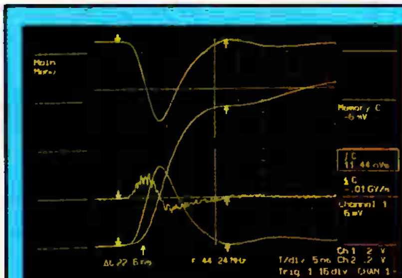


Switching transients recorded in segmented memories show contact bounce in segment number 3. Cursors measure bounce-time-interval precisely.



Noisy H.F. Transmission Signal is averaged in time domain. Spectral content of cleaned-up signal is analyzed by FFT.



Inverted photo-diode signal is normalized then integrated for energy measurement (area under curve >11.44 nVs). Differential dC/dt is shown as well.

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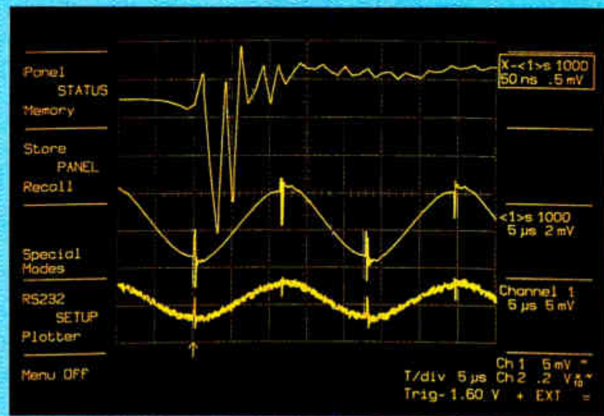
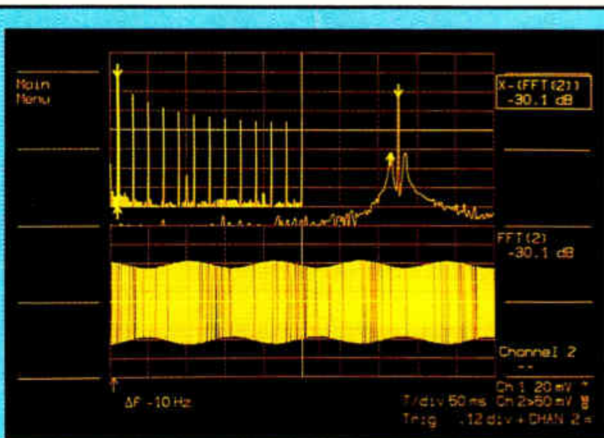


Signal averaging improves dynamic range and sensitivity. Perturbation on a function generator sine wave is expanded to 500 μV/div vertically (10x) and 50 ns/div horizontally (100x) showing fine details, helpful to find cause of distortion.



Long records give wide frequency span. Modulated audio signal, recorded over 25,000 points, shows harmonics up to 25 kHz. Expansion shows siebands at 10 Hz and −30.1 dB. Frequency resolution is 2 Hz.

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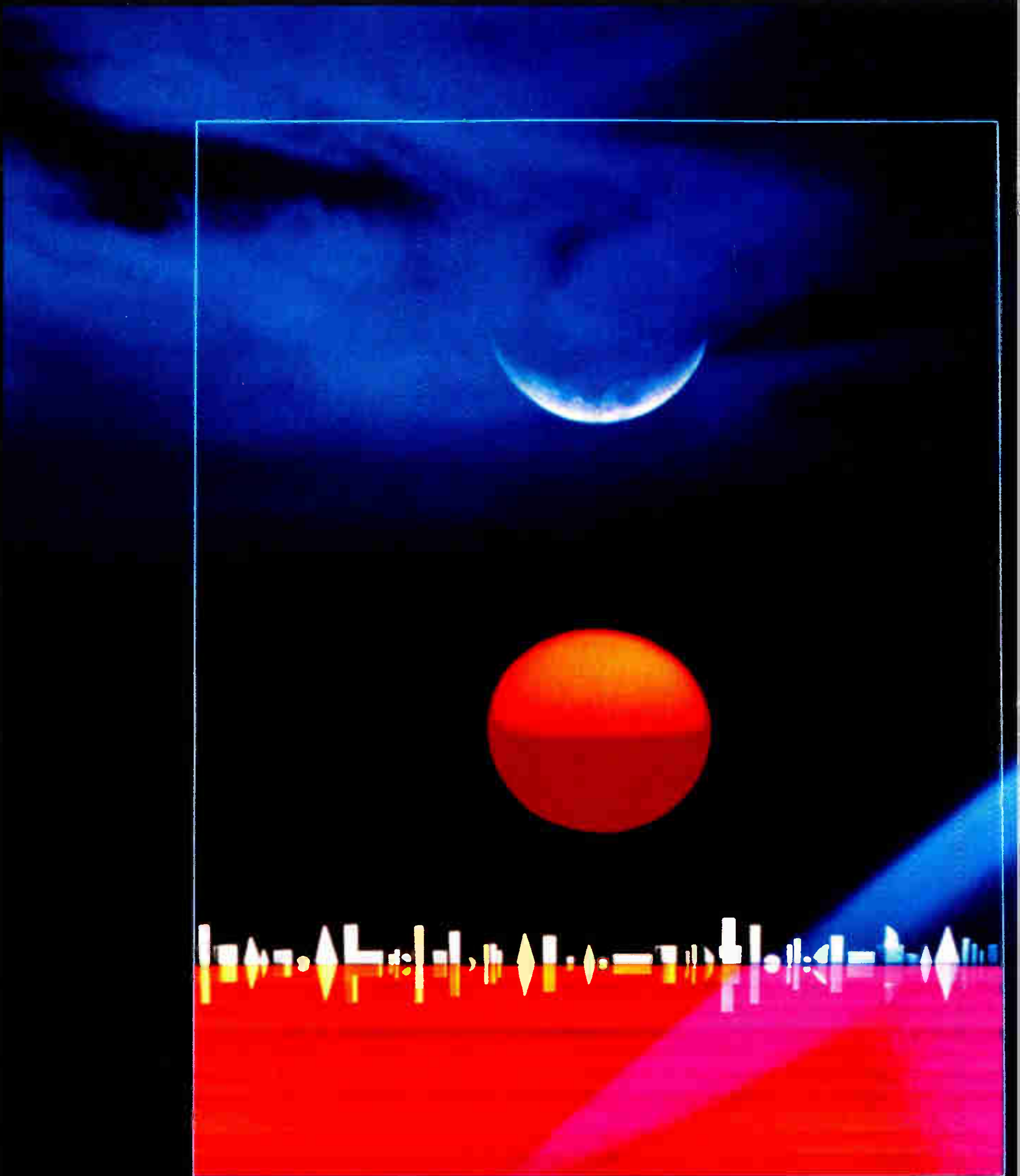

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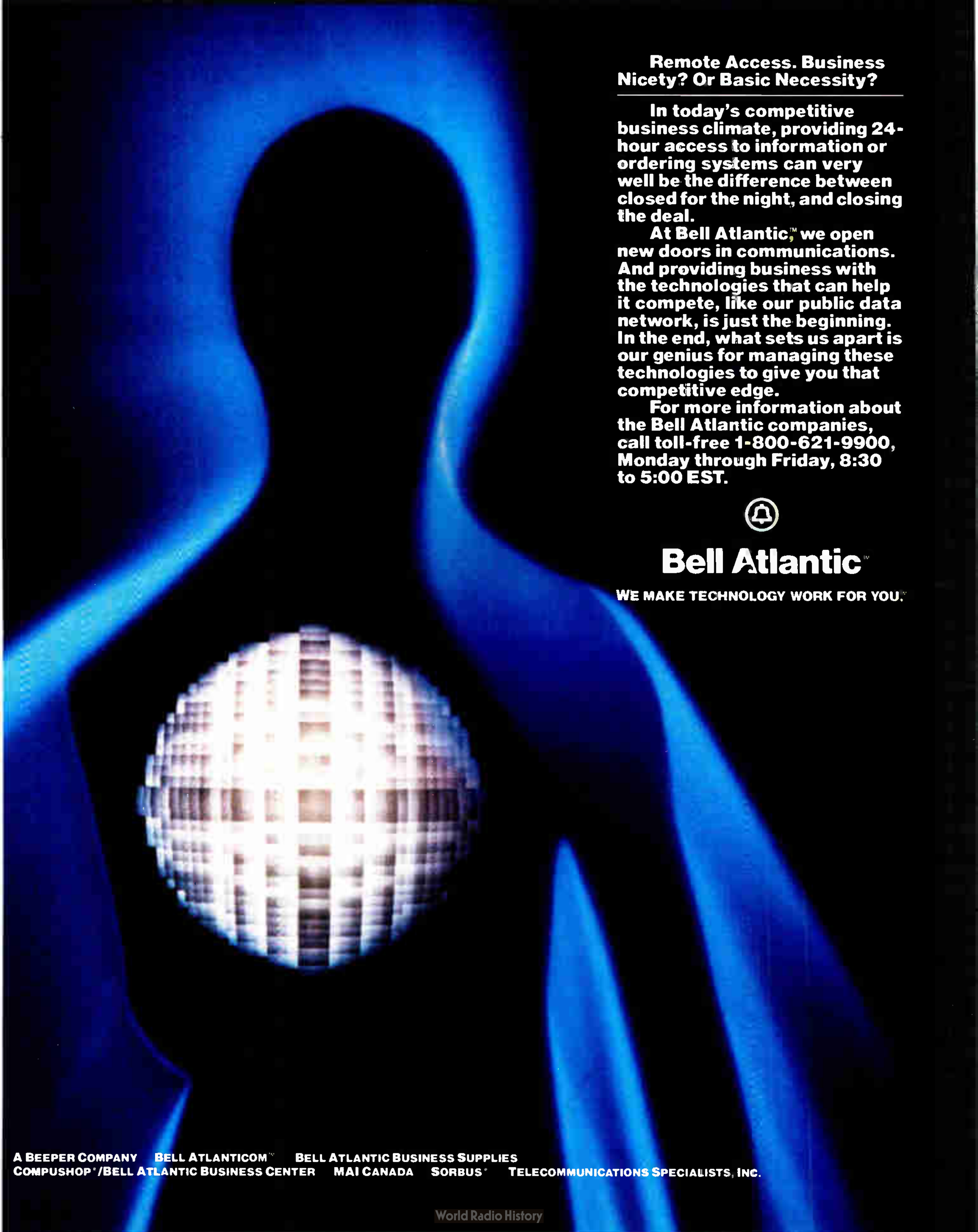
BELL ATLANTIC MOBILE SYSTEMS BELL ATLANTIC PROPERTIES BELL ATLANTIC SYSTEMS LEASING BELL ATLANTIC TRICON

IN TECHNOLOGY ALONE, BUT IN THE ABILITY TO MANAGE IT.



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LAYOUT TOOL STREAMLINES FULL-CUSTOM IC DESIGN

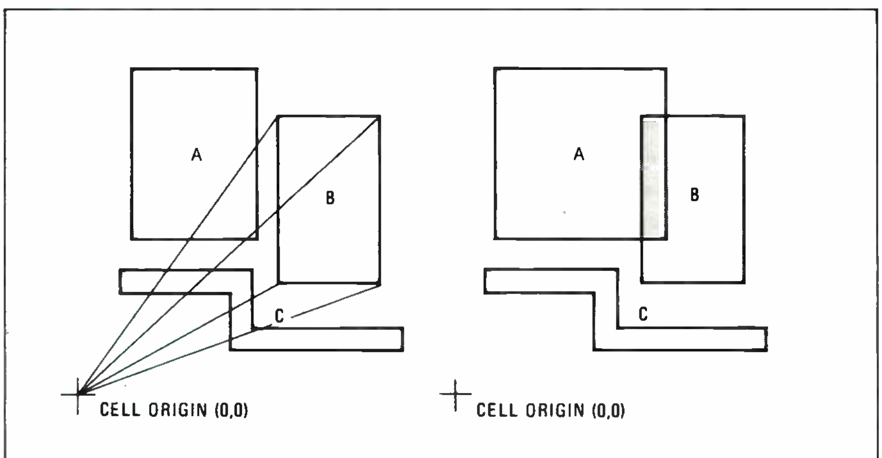
Caeco's R-Cells system provides reusable macros, automatic changes when one transistor is altered, and a facility for matching layouts to processes

Laying out full-custom, very-large-scale integrated circuits usually means working through a design one transistor at a time on a computer-aided-design system. But now a new software package from Caeco Inc. in Sunnyvale, Calif., promises to streamline VLSI layouts. Called the R-Cells VLSI Design System, the software features three specific capabilities that solve crucial layout problems.

First of all, an intelligent graphics interface enables the designer to create a macro design for an individual cell and then replicate the macro anywhere in a layout. In addition, each segment of the design is laid out in a relative-coordinate system, so that when the designer later reduces or enlarges a transistor, the layout automatically expands or contracts around the cell to accommodate the change. And for flexibility, a separate process-definition file can be configured to any process environment. A designer who wants to change processes changes the file, and the entire layout is altered to conform to the new design rules.

The first version of the R-Cells system, which is set for introduction next month at a price of $30,000, will allow designers to create only the individual cells, which can be a single transistor or a more complex gate or flip-flop. Any changes to those cells will automatically change only the portion of the layout immediately adjacent to them. However, Caeco says a future extension of the system will expand the R-Cells concept beyond the cell to the entire layout, so that each cell will be related to its neighbor. With the extended version, designers would be able to alter whole sections of a layout as easily as they will be able to change individual cells with the initial version.

The R-Cells capabilities represent major changes in the way full-custom VLSI circuits are designed, the company claims. Today, these ICs, which contain upwards of 500,000 transistors, are laid out by hand, one transistor at a time, on CAD



1. FIXED. Older, absolute-coordinate systems use fixed cell origins, so changing a polygon block can mean moving all adjacent blocks.

systems. Caeco says the new software will help make existing design tools more efficient by automating procedures that now must be done individually.

The package runs on work stations from Sun Microsystems Inc. of Mountain View, Calif., and Apollo Computer Inc. of Billerica, Mass. The system produces and can read the GDS-II Streams data-file format developed by Calma Co. of Milpitas, Calif., a de facto standard for CAD files.

Caeco's approach begins with the first step in a layout. Today, a designer begins a layout with a blank screen, on which he laboriously builds individual transistors by arranging polygons that represent metal and polysilicon over one another to form the transistor's base, emitter, and collector, a process called "polygon pushing." The methodology is at least 10 years old, says Caeco's Marlow Draney, director of software. Using this method, it takes up to four hand operations to build elementary transistors. Creating the same transistor with contacts for connecting to other devices can take eight operations. And building a bent gate—one that fits into a right-angle space—can take as many as 12 operations.

By contrast, the Caeco system allows a designer to define a transistor or cell and then replicate it where it is required in the rest of the layout. More important, he can define more complex cells—for example, a 4-bit counter—and reuse them elsewhere in the layout. Once the cell has been placed in the circuit, it can be edited to fit into the area surrounding it. The designer no longer has to push polygons to create a circuit element each time it is used; nor does he have to place each element separately in a layout. Other layout systems allow the designer to reuse portions of existing layouts, but they do not allow the replicated circuit to be edited.

With R-Cells, the designer can also capture each stage of the editing process as he uses the graphics-screen editor, and thereby create a new macro from any of those stages. To create a piece of reusable layout, he asks the editor to record the indicated piece of layout as a cell. "As the designer creates the macro, every operation he performs, every edit he makes, is encoded as part of the R-Cells description," says Mark Miller, Caeco's director of marketing.

The data is automatically written in the form of a macro description file. In addition, the designer can use the editor to place parametric references or prompting messages in the macro description file. Thus, when the macro is called later, the system can ask the designer invoking the macro for the size of the device-level primitive, its aspect ratio, and any other programmable attributes of the macro. The macro cell resembles a subroutine call, in which the designer supplies the appropriate arguments or parameters.

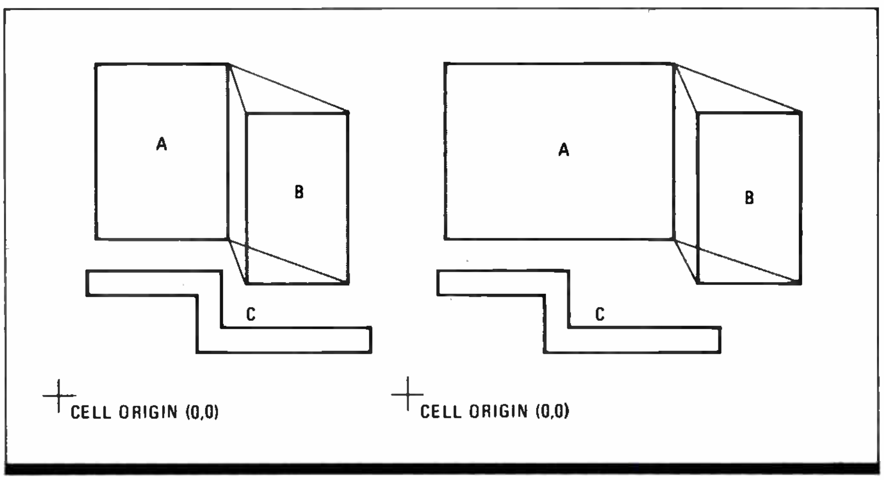
Besides working faster, the designer will be able to get layout structures equivalent in density to those created by hand, and he can make changes to the layout after it has been automatically generated. For example, if a designer wants to place a straight gate in most areas but convert it into a bent gate that can fit into a specific area of a layout, he can edit the macro description file of the straight gate to add the new vertices for the bent gate, and he can vary the length and width of either leg of the right angle. Once that gate has been created, it too becomes a macro cell that can be reused.

REUSING EXISTING LAYOUT

The capability for editing and reusing an existing layout provides designers much more flexibility. This feature is made possible by a relative-coordinate system that describes the position of every polygon in a design. Other layout systems have used an absolute-coordinate system (Fig. 1), in which every polygon block in a cell is referenced to a fixed origin. If three blocks make up a cell, the location of the corners of block A is established by x-y coordinates with respect to cell origin 0,0. The same is true for blocks B and C. If the width of block A increases, the designer must move block B the required amount of space to prevent A from overlapping B, thereby violating design rules.

In a relative-coordinate system (Fig. 2), every polygon block in a cell is referenced to a fixed cell origin, but each is also referenced to every adjoining block. In a three-block cell, for example, the corners of block A are referenced to adjacent blocks B and C. If the width of block A increases, the Caeco software automatically moves block B the appropriate distance to maintain the relation it had with block A before the latter was enlarged.

The relative-coordinate system determines



2. FLEXIBLE. Caeco's relative-coordinate system relates a block to cell origin and its adjacent blocks; changes automatically shift the adjacent blocks.

such design-rule requirements as polygon-to-polygon spacing, overlaps, and minimum and maximum device sizes. Devices can then be defined as complete entities, and as they are entered into the data base they can be intelligently edited as to their size, shape, placement, and orientation without disturbing the integrity of the design rules being used.

CHANGE THE DESIGN OR THE PROCESS

The designer therefore can adjust the finished layout if, for example, he discovers a gate in the middle of the design has to be changed because it affects the timing of the entire circuit. Being able to edit an existing layout is especially helpful when a layout is altered to improve electrical performance of a design. "If the designer does a simulation of a cell in a larger design that has been laid out and finds that one gate in the middle of the cell is a little too slow, he may need to fatten up the gate a bit so its speed will increase," says Miller. "The designer can use the R-Cells capability to expand that one gate without affecting the remainder of the layout and without creating a design-rule violation."

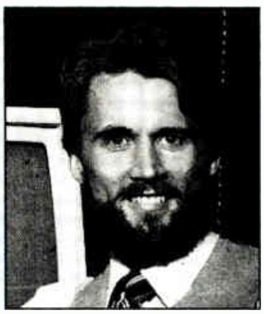
The relative-coordinate system accommodates changes that the designer wants to make in the design itself. To accommodate changes that occur in process technology, the R-Cells system keeps process data in a separate process-definition file. This allows the designer to change the file without having to change the layout data.

The process-definition file contains design rules and device characteristics. It can be configured to the particular process technology: CMOS, n-MOS, p-MOS, or bipolar. With the file, the designer establishes basic relationships between structures: for example, the distance between a polysilicon gate and a polysilicon wire that is not off the same node must be a minimum of 4 μm. The R-Cells capability uses the file to inform the system of the design rules. "It enables layout designers to design at the component level using transistors and wires, without having to concern themselves with the limitations of the process," says Draney. "Every time the designer lays out a gate, it instantly appears in a form that meets all the required design rules, ready for editing by the designer."

Caeco's overall goal is to make designers more efficient, by using the current generation of CAD systems as a foundation for the R-Cells system. "As a company," Miller says, "we are trying to build a software environment in which the productivity of existing layout tools can be increased." □

MAKING A CAREER OF IMPROVING LAYOUT TOOLS

Marlow Draney, Caeco Inc.'s director of software, started trying to improve software layout tools for integrated-circuit CAD systems soon after he graduated from Brigham Young University. As a designer of ICs at National Semiconductor Corp., he began tinkering with the layout software running on National's minicomputers.



MARLOW DRANEY

MARK MILLER

"One problem I was keenly interested in was the limitations of macros in these layout systems," says Draney. "A designer could build a device and then replicate it at other points in the layout. But if the macro needed to be changed, he had to edit the macro by hand to ensure the changes met the design rules of the process."

"Marlow understood the IC-layout software problem," says Caeco's director of marketing, Mark Miller. "He struck on the idea of allowing the designer to define a macro in a relative-coordinate system, so that as the macro was changed, the cell itself would automatically adjust its component parts to conform to the design rules."

That concept eventually found its way into Caeco's new layout software, the R-Cells VLSI Design System. Miller saw a preview of some of the R-Cells tools while he was working for a Caeco competitor, Daisy Systems Inc. of Mountain View, Calif. The demonstration convinced him to leave Daisy and join Caeco.

By the time Miller came to work at the Sunnyvale, Calif., company, Draney was completing the first full version of R-Cells. "Caeco already had unique features that put them ahead of others in the field of IC-layout software," Miller says. Among those was a transistor that can be defined by parameters as opposed to simple polygons. Another was a real-time design-rule checker, one that detected rule violations as layout occurs, rather than one that could be invoked periodically to check the layout after some number of entries had been made. A third was connectivity in the design-rule database. Rule checkers lacking connectivity data cannot distinguish between an error and the connection of two poly layers at a node. The designer has to examine each connection to determine which are errors.

"When I came on board and saw the R-Cells product, I knew the company had four features not found anywhere else in the market," says Miller. What the system still lacked at that point was a user interface that would allow easy use of the relative-coordinate system, a key feature. Miller's contribution to the project was to help define what that interface should be.

One of the features incorporated into the interface was the ability to allow the user to graphically specify relationships between elements of a cell. "One could relate the edge of one polygon to an adjacent polygon simply by pointing to the two on the screen and indicating that some specified spacing should be maintained," says Draney.

Now Caeco is setting its sights on more powerful layout tools. Draney thinks a future product will take the next logical step: it will extend the capabilities that R-Cells provide for individual cell design to the entire chip layout.

COMBINING THE BEST OF STEP AND DC MOTORS

Seiberco Inc. is launching a controllable-drive motor that fills the cost-performance gap between a step motor and a brushless dc motor. It is marrying a sensor, driver, and controller to a specially designed two-phase motor (Fig. 1) for a system with the easy controllability of an inexpensive step motor and the performance of a costly brushless dc motor system (Fig. 2). The Braintree, Mass., company says its new AIM 2300 is suitable for many applications, such as microscope-focusing equipment, *x-y* tables, and antenna and telescope drives.

For applications requiring variable torque, relatively low speeds, and maximum position retention, the step motor fills the bill. For those applications with very high-speed requirements coupled with constant torque and where high cost is not an issue, the brushless dc motor is the answer. However, the characteristics of Seiberco's sensorimotor—the "i" is for integral position sensing—are sufficiently different from step motors and brushless dc systems to fill a need not covered by either.

The AIM 2300 exceeds 3,000 rpm, has torque characteristics of a brushless dc motor without needing an external sensor, and can handle applications that are cost-sensitive but need the dynamic performance of a brushless motor. Sensorimotor-based systems cost about 20% more than a step-motor system and half the price of a comparable brushless dc motor-based system.

Step motors are relatively easy to control because their commutation does not depend on position-feedback information. Steppers have many poles and are incrementally advanced, or stepped, from one equilibrium position to the next by a single pulse and a direction-control voltage. Stepper speed is proportional to pulse rate. However, useful rotation of step motors rarely exceeds 500 rpm.

Step motors are typically used for their good static performance and simple open-loop control applications. When high rotation speed and high peak torque are required, users turn to brushless dc motors. These types of motors have fewer poles, typically 4 to 12. And to close the position servo loop, shaft-position information needs to be monitored by the position sensors attached to the shaft.

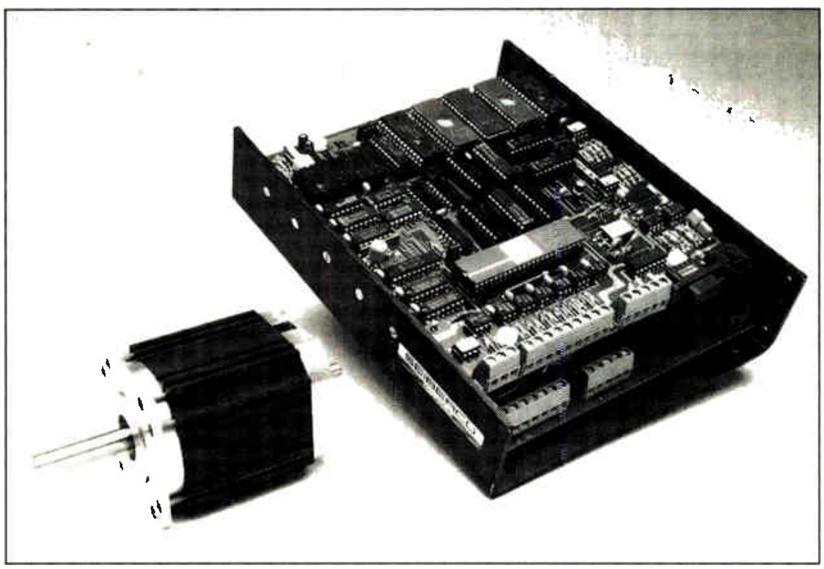
Brushless motors can operate at 10,000 rpm but typically operate well below this limit. At low speeds, however, these motors perform poorly and have difficulty maintaining static rest positions. Moreover, the cost of a brushless dc motor system plus external sensor and closed-loop controller is far higher than a step motor and its open-loop control interface.

But Seiberco offers the best of both worlds in terms of speed and cost. The AIM 2300 system is intended for automated positioning systems in a variety of industries. For example, the system has replaced a step motor in a wafer-test platform where the stepper lacked sufficient speed and needed an external sensor for position feedback. The comparable cost of outfitting the stepper with a resolver was greater than the cost of the AIM 2300 system.

BUILT-IN SENSOR

In a prototype integrated-circuit lead trimmer, the AIM 2300 system replaced a brushless dc system for positioning a cutting head. A slow speed specification required gearing down the brushless motor. Added to the cost of a sensor, the added gearing drove up overall machine costs. The AIM 2300 was able to provide sufficient torque at low speeds without gearing, and its built-in sensor provided more than enough position resolution to allow the machine designer to meet system and cost requirements.

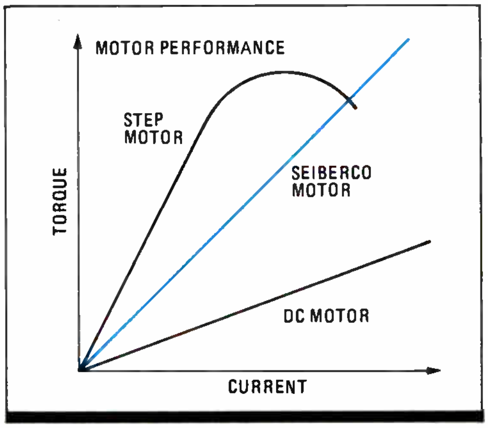
Seiberco's motor is a two-phase, 18-pole unit that produces a pair of signals in quadrature. These signals indicate the shaft's position in relation to the stator. Properly processed, the sig-



1. HIGH PERFORMANCE. The AIM 2300 motion-control system features a new motor design with internal position sensing and a microprocessor-based controller.

nals provide position-feedback information like that of an external sensor such as a resolver, but they add no shaft loading. Since the built-in sensor is an integral part of the motor, there is no added cost as in the case of an external sensor.

Dual H-bridge driver circuits supply power to each of the motor's phases. Each driver uses power MOS FETs switching at a chopping rate of 50 KHz with relatively low conduction loss and heat dissipation. The drivers can deliver 40 W to 250 W of continuous power.



2. BLENDED MOTOR. Seiberco's motor combines the high torque-to-current ratio of the stepper with the linear torque-to-current ratio of the dc motor.

An Intel 8096 16-bit microcontroller provides the processing power to handle the real-time motor control within a 500-μs cycle and has more than enough time to handle user-interface tasks in the background.

Real-time tasks include closed loop and proportional integral-derivative motor control. Pulse and direction signals, whether input directly or as pulse-train profiles computed by the 8096, are summed with position decoder signals and used by the PID algorithms to compute final gain values. This process is repeated every 500 μs and ensures that the system will hold its static position or execute a motion profile well within the stated accuracy limits of displacement, velocity, and acceleration.

The motor's high performance is attributed to its novel design and the newer, high-energy, samarium magnets in its magnetic structure, according to Ralph Horber, vice president of engineering.

Seiberco is offering three motor sizes with peak torques ranging from 90 to 270 oz-in. and continuous torques of 36 to 108 oz-in. Position resolution is 2,304 parts per revolution with position accuracy rated at ±20 min of arc. Test results have been closer to ±10 min of arc. □

TECHNOLOGY TO WATCH

CAPACITIVE COUPLING SIMPLIFIES ISOLATION

Capacitive coupling is the key to Burr-Brown Corp.'s radical new way of providing signal isolation. The Tucson, Ariz., company's technique could simplify the design and packaging of isolation amplifiers and other circuits that require a buffer against harsh signal environments.

This three-chip hybrid technique can be widely applied in systems in which analog signals must be isolated from noise interference or very high voltage potentials that could occur because of an electrical fault. Typical applications are industrial process-control systems with multiple remote transducers, biomedical measurement systems, military equipment, power monitoring, and motor control.

Conventional hybrid isolation amplifiers typically use magnetic or optical coupling to reject high-voltage spikes and noise interference while transferring signals between various parts of a system or circuit. However, such amplifiers are complex and expensive to manufacture, often require assembly techniques in which alignment of the isolation barrier's parts is critical, and are difficult to automate. Breakdown-voltage ratings for typical isolation amplifiers are no higher than 1,500 V_{rms}. Even though the devices usually operate below this value, however, undesirable interaction between input and output often occurs.

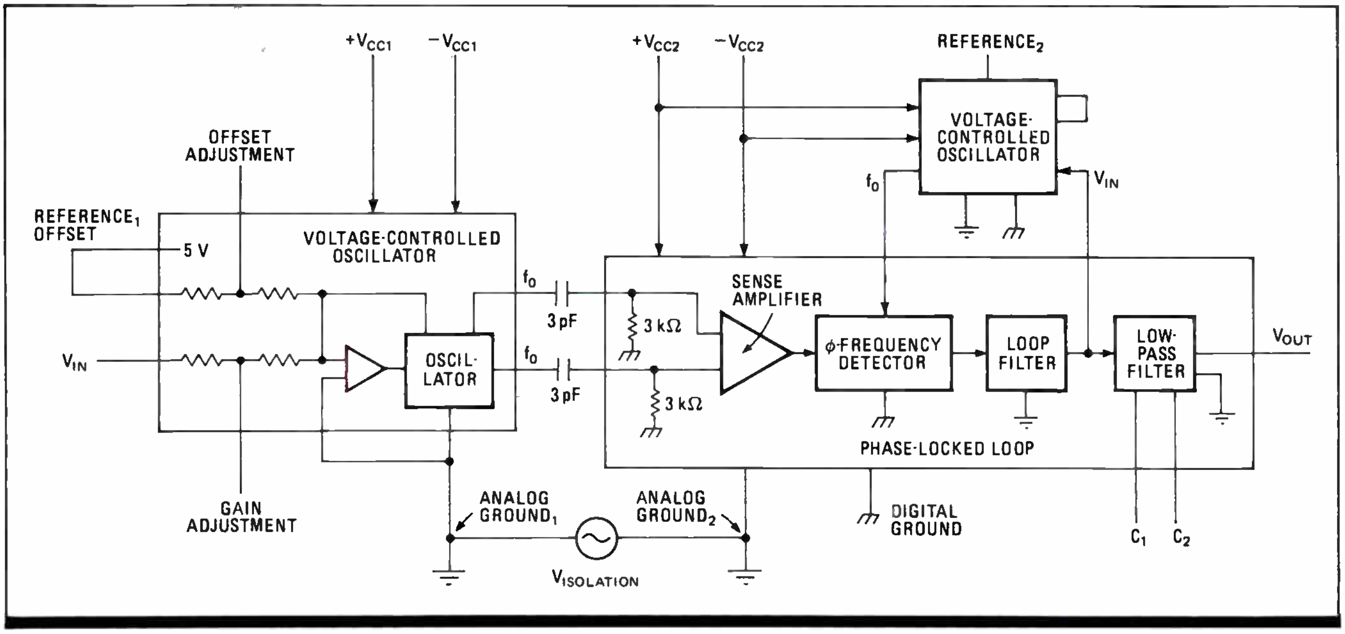
Using its new capacitive-coupling technique, Burr-Brown has developed a pair of unity-gain isolation-buffer amplifiers that ameliorate, if not eliminate, most of these limitations. The ISO102 operates at 1,500 V_{rms}, and the ISO106 operates at 3,500 V_{rms}. These amplifiers are supplied in 24-pin and 40-pin packages, respectively. Both packages are 600 mils wide.

A CAPACITIVE BARRIER

To achieve such high isolation-voltage ratings, the I/O elements of the isolation amplifier are separated by a capacitively coupled barrier in which a pair of 3-pF thin-film capacitors are formed on a standard single-layer substrate within the fired ceramic of the package. Rather than using standard plate-type capacitors, the ISO102 uses capacitance that results from the fringing electric fields surrounding adjacent lines of tungsten.

These lines are deposited in a spiral pattern whose lines are 0.63 mm apart on a 0.6-in.-wide ceramic substrate. Atop this pattern is fired a thicker ceramic layer, embedding the spiral capacitor in solid ceramic. With a dielectric strength of 15,000 V/mm, this ceramic-enclosed capacitor has a breakdown voltage of more than 9,000 V_{rms} and a barrier resistance in excess of 100 terohms.

In the top ceramic layer, windows are fabricat-



1. GETTING THE MESSAGE. Burr-Brown's ISO102/106 amplifiers couple signals across an isolation barrier by using digital signal modulation, a voltage-to-frequency conversion scheme, and carefully matched voltage-controlled oscillators.

ed, forming the cavities into which the I/O circuitry of the isolation amplifier is placed. On the input side is a proprietary voltage-to-frequency converter chip that is a voltage-controlled oscillator that transforms a ±10-V input signal into pulses ranging in frequency from 0.5 to 1.5 MHz. The pulses are generated in complementary form.

A two-chip decoder that senses the pulsed signal and reconstructs the input-level signal is on the output side of the isolation barrier. One chip contains a sense amplifier, a phase-locked loop, and an output filter, and the other contains a second VCO carefully matched to the input VCO by selecting adjacent dice on a single wafer and by careful laser trimming.

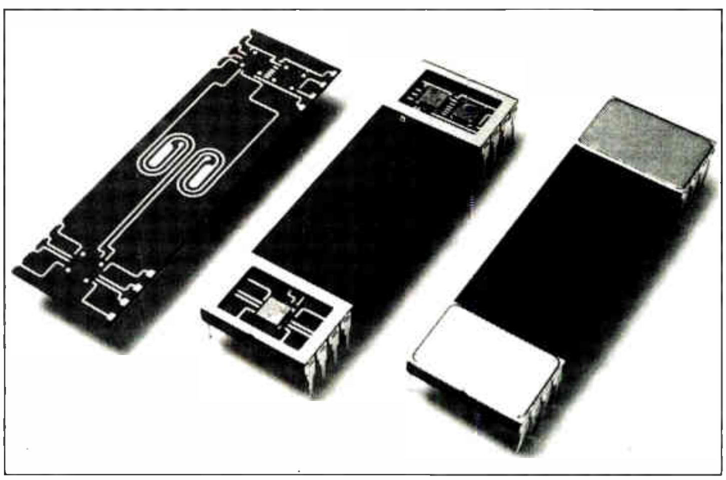
Rather than use the analog coupling methods in previous devices, Burr-Brown engineers have opted for a new digital signal-modulation technique to pass information across the barrier with a minimum of noise. In this technique, the ±10-V input-signal frequency modulates the 1-MHz output of the first VCO. The modulated signal is differentially coupled through the barrier capacitors to the demodulation circuit, which rejects any common-mode signals, including the isolation voltage.

Unlike analog methods, in which the isolation-mode rejection ratio—a change in the output signal divided by any change in the isolation voltage—degrades continuously with increasing isolation-voltage frequency, the differential signal in this approach is not affected by the barrier voltage, except if it exceeds the noise immunity of the signal.

As a result, the ISO102 and ISO106 have IMRR ratings more than two orders of magnitude better than previous optical and magnetic isolation-coupling techniques. Indeed, the only significant IMRR effects in the devices are minute, capacitively coupled currents in the analog ground connections. Typical IMRR for the ISO106 is −150 dB at 60 Hz, and for the ISO102, −120 dB at 60 Hz, independent of ambient temperature.

HOW THE CHIPS PERFORM

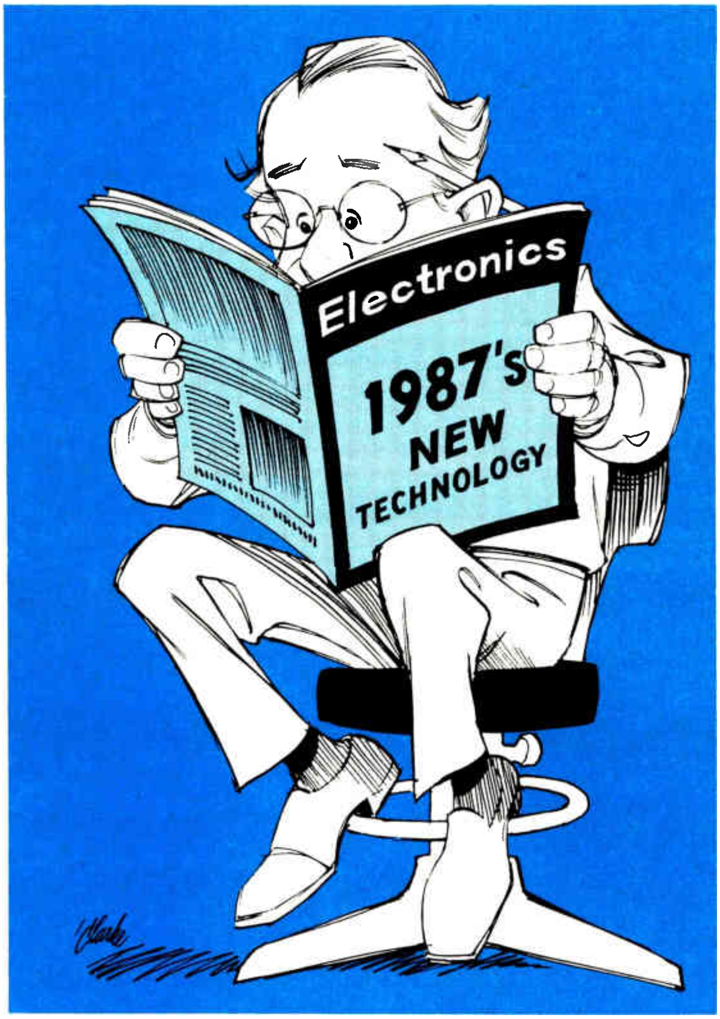
Settling time and overload recovery time for a −10-V to +10-V step is 100 μs to reach 0.25% accuracy. Wideband noise of the output signal is flat to below 0.1 Hz. At 70-KHz bandwidth, the dynamic range is 12 bits, doubling whenever the signal bandwidth is quartered, reaching 16 bits for a 280-Hz bandwidth. At full bandwidth, the 1-MHz carrier appears at the output as a 1-mV peak-to-peak ripple voltage. Frequency-response rolloff is −40 dB per decade. □



2. IN SHAPE. The ISO102/106 amplifier forms signal-coupling capacitors by embedding metallic spirals in ceramic substrate.

EXECUTIVE OUTLOOK: NO TECHNOLOGY SLOWDOWN

In the annual worldwide survey, executives and technologists see headlines on biMOS technology, practical GaAs products, real-world AI, optical disks, and networking



Without a doubt, next year will be an exciting one for executives in the worldwide electronics industry. That's what they expect; their only question now is, what kind of excitement?

On the positive side, managers look for rapidly changing technologies, which should continue to create new markets, obsolete present products, and shift company market shares. But *Electronics'* annual survey of industry executives on the outlook for the coming year is also laced with plenty of adversity. This feeling comes mostly from executives worrying about the health of their 1987 markets, something that will be the subject of in-depth forecasts to be published in the next two issues of *Electronics.*

Foreign managers expect to have their own set of problems next year. Japanese managers say they will have their hands full with the growing problems caused by the stronger yen (p. 89), while their European counterparts try to figure out what strategies they will need to keep from being run over by Japanese and American manufacturers (p. 90).

The same technologies kept popping up when executives around the world were asked what technologies would make the product headlines next year. Many managers expect to see major improvements in complementary-MOS chips and a speed-up in the march of CMOS toward greater market share. They also see news coming from those researchers working on relatively new processes that combine bipolar and MOS devices on the same die. Others anticipate that 1987 will be a big year for gallium-arsenide product breakthroughs, although some think that GaAs may be headed off at the pass by the faster speeds being achieved by bipolar silicon devices.

In computing, executives are sure they will be hearing about rapid progress in the optical-disk storage field, as well as the coming wave of systems based on 32-bit microprocessors, especially the Intel 80386. Developments in networking will come much faster next year, as will significant announcements in the areas of parallel processing and artificial intelligence.

Still others expect 1987 headlines to be made in the fields of computer-aided design, surface-mount technology, self-testing chips, smart power, and semicustom integrated circuits.

One executive expecting to see news of advances in CMOS technology is James R. Fiebiger, president of Thomson Components-Mostek Corp., Carrollton, Texas. He thinks high-density, high-speed CMOS with design rules of 1.5 μm or less and two layers of metal will garner attention. Daniel Queyssac, president and chief executive officer of SGS Semiconductor Corp., Phoenix, is another who predicts a "continuing move to CMOS throughout the year."

"We will see a further shift away from n-MOS to CMOS because of the speed and lower power dissipation the latter offers," chimes in Klaus Ziegler, vice president of marketing and sales in the Components Group of Siemens AG, Munich.

But there is an upstart challenger with some special capabilities of its own. BiMOS, a combination of bipolar and MOS, will prove significant because of the high performance it offers, as well as its ability to combine analog and digital functions on one chip, says Gollapudi R. Mohan Rao, Semiconductor Group vice president at Texas Instruments Inc., Dallas.

"BiMOS will make headlines next year because it is really starting to offer much higher performance in semicustom and mixed analog-and-digital systems," agrees Bob Hunt, general manager of the semiconductor division of STC Components Ltd, Foots Cray, UK. "There are a lot of people requiring precision analog in combination with high-density logic functions, and biMOS can provide this." Data acquisition is one area ripe for a biMOS invasion, points out Charles R. Thurber, a staff engineer at General Electric Co.'s Intersil Inc. subsidiary, Cupertino, Calif. He thinks biMOS will fuel big improvements in high-performance data converters.

Years of work on GaAs devices will yield marketable products next year, executives hope. "I think that next year will be the year when GaAs becomes recognized as a real technology," says Peter van Cuylenburg, managing director of Texas Instruments Ltd. in the UK and vice president of TI's worldwide semiconductor group. "I think there will be a range of large- and very-large-scale integrated random-logic products, such as arrays and processors. There are enough products under development that some will surface next year." Hans Weinerth, director at Philips GmbH, Hamburg, West Germany, also thinks GaAs will capture attention next year, "although economically it will still play a negligible role."

"The dark horse is the heterojunction bipolar GaAs circuit technology, which may surprise us," says Denos Gazis, assistant director of logic, memory, and packaging at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N. Y. This has been an area of interest for a while, but "suddenly it's beginning to show signs of life," he says.

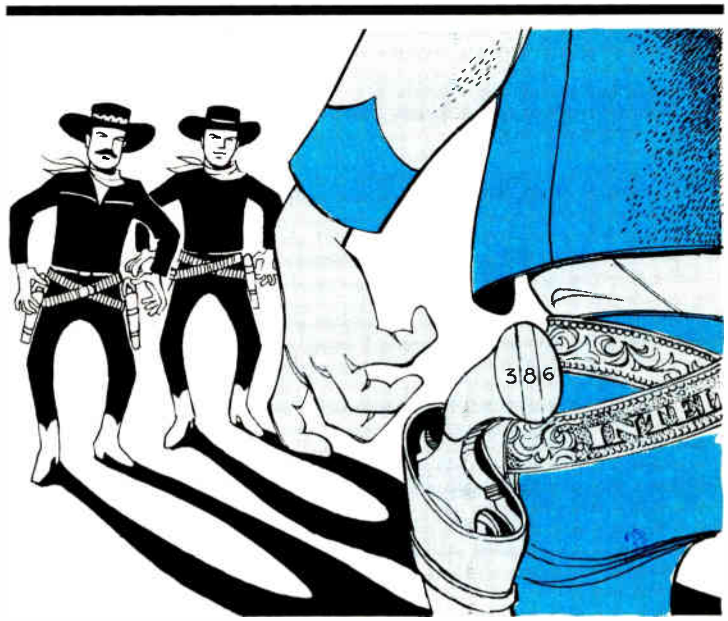
"We're trying to bring GaAs out of research and development into the real-world environment," says R. Ronald Duncan, general manager, Microelectronics Research & Development Center, Defense Electronics Operations, Rockwell International Corp., Anaheim, Calif. But the wild promises made in the past continue to hurt the realistic development of GaAs technology. "GaAs will have to show its mettle very soon, or people will get disenchanted."

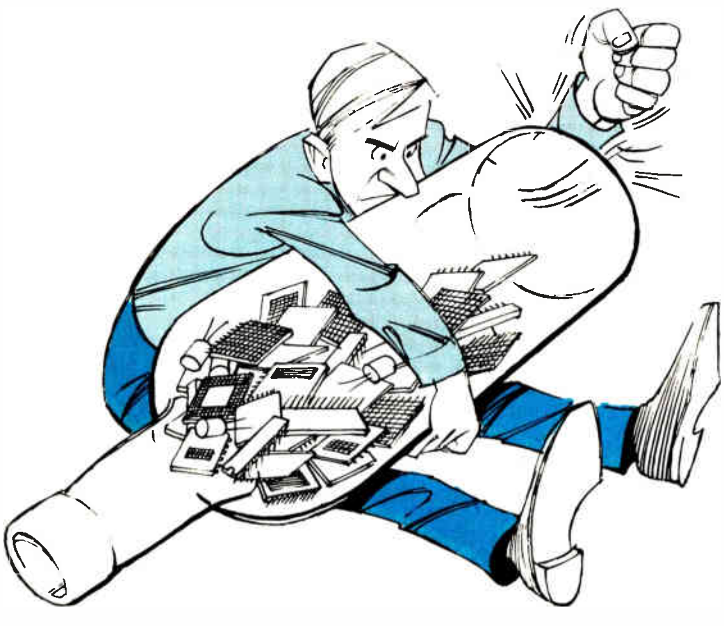
GaAs may well be squeezed out of the picture by fast CMOS on the one hand and improvements in bipolar technology on the other, says John Brothers, development executive for MOS at Plessey Semiconductors Ltd., Plymouth, UK. Doug Dunn, Plessey's managing director, agrees. "I think bipolar will be the biggest headline next year," he says. "If you look at the past five or six years, CMOS has made the headlines because it is a new technology with good performance. Meanwhile, bipolar has always had its strength in speed. It has seen pressure from CMOS on power and from GaAs on speed. But it has been making its own progress and is re-emerging."

In the computer industry, the hot story for 1987 looks to be optical-disk technology. Peter Giles, vice president and general manager of Eastman Kodak Co.'s Mass Memory Division, Rochester, N. Y., sees write-once optical disks and the first erasable-optical-disk systems getting started in 1987 and having real impact in 1988 and beyond in image- and information-management systems.

"Optical will be news," concurs James M. McCoy, president of Maxtor Corp., San Jose, Calif. Although optical storage "will continue to get a lot of 'share of mind,'" he says, "it will become

Intel's 30386 is a favorite in the 32-bit microprocessor shootout, but no winner is expected in 1987—the issue will be 'hotly contested for years'





Companies trying to push new products to market face many frustrating bottlenecks, among them the need to teach customers how to use them

clearer through 1987 that it won't happen overnight and won't displace major areas of the magnetic recording business—certainly not quickly, and not nearly to the extent that was believed a couple of years ago."

McCoy is one of many executives who say they expect much news of the new generation of microprocessors. Like most others, he singles out the Intel 80386 as one to watch, noting that it "will bring improvements in small-system cost and performance at a continuing rapid rate."

But the Motorola 68020 should not be discounted, says James Norling, executive vice president and general manager of Motorola's Semiconductor Products Sector, Phoenix. "The 32-bit shootout will be hotly contested for years," he says. "The Japanese are finding the way in, too."

One important benefit from 32-bit processors is lower system costs. "On the 386, you'll have Lisp and AI on a more cost-effective platform," says Robert Miller, senior vice president at Data General Corp., Westboro, Mass. "Before, [customers] have had to buy a $50,000 machine. Now, they'll spend less than $10,000."

AI in general is expected to make waves. AI-based man-machine interfaces, for example, will become common not only for computers but also for word processors, cash registers, and work stations, says Yutaka Iuchi, Division General Manager of the Information Systems Laboratories of Sharp Corp, Osaka, Japan. Hajime Sasaki, vice president of the Electron Device group at NEC Corp., Tokyo, says "LSI design methodology will be greatly transformed by migration to AI technology. Expert systems will advance from tools to intelligent systems with the inclusion of sufficient knowledge to perform actual designs. Gate-array and semicustom design will rely heavily on AI as the designer population increases, with a shift from design-by-vendor to design-by-customer."

Although less likely to produce breakthrough news, computer networking will make steady progress, executives say. For example, a wave of products based on the network model developed by the International Organization for Standardization is expected in Japan, says NEC's Hiroshi Hatta, an assistant general manager for the company's Information Processing Group.

Evolutionary developments will be made in networking technologies—digital signal processing, fiber optics, and software—says Timothy P. Sullivan, vice president for small systems and networks in the BNR labs of Northern Telecom Inc., Richardson, Texas. "The greatest breakthroughs will be in combining all of those things."

Ken Olsen agrees. Regardless of the magnitude of any one development, the president of Digital Equipment Corp. says flatly, "Technologies never make headlines. The important things come from good engineering." Development of networking capability and transparency will have the greatest effect on his company's business next year, he says, although convincing companies to open up their organizations to make productive use of networks is an ongoing struggle. The customers themselves are the big bottleneck in selling networks, Olsen maintains.

Asking executives about the bottlenecks encountered in bringing other types of new products to market elicits a wide variety of responses, ranging from insufficient funds, engineers, and work stations to testing problems, setting standards, and passing the baton from lab to design team to production people to marketing. There are many hurdles to clear, and which ones are encountered depends on the product.

One hurdle that stands out as being on the minds of many executives is the difficulty of making sure a product is mature, reliable, and compatible with existing systems. Another is training and supporting users in the use of a truly new product. Executives also harp on the problems of bringing products to market when the market itself is sluggish.

Apollo Computer Inc., for one, has instituted "exhaustive product-maturity testing"—something it didn't do two years ago—says David L. Nelson, vice president and chief technical officer. "[We] set up a large number of machines and test them for long periods of time under different conditions," delaying the introduction of a new product, but ensuring a more solid product.

The time required for "analysis, development tests, environmental tests, field tests, and validation of our product, to make sure that we introduce something starting off that has high reliability and durability" is also cited by Donald J. Atwood, president of GM/Hughes Electronics Corp., Detroit. He sees some relief in sight in the form of improved simulation systems and modeling techniques. "There's no substitute for building and testing," he says, "but [with modeling] we can short-circuit some of the need for building and testing every iteration."

When a wafer-etching product was brought out a few years ago by Applied Materials Inc., Santa Clara, Calif., it was enough to demonstrate the technology to get a share of market,

CAN THE JAPANESE COPE WITH THE SOARING YEN?

The Japanese electronics industry is painfully coming to grips with the rising value of the national currency. Industry leaders expect the impact of a strong yen—and the search for ways to maintain the flow of exports that provides a large part of their revenue—to remain a major challenge in the coming year.

They have their work cut out for them. The value of the yen has climbed more than 50% in about a year, driving prices up and sales down. At the same time, the Japanese are getting more competition from Asian countries that continue to enjoy a more favorable exchange rate with the U. S. dollar.

As a result, many export-oriented Japanese companies are being forced into defensive strategies that are ironically similar to those adopted by American and European businesses when they were threatened with a flood of Japanese imports. The parallels are pronounced enough for one Japanese executive to predict gloomily that his country, like the Western industrialized nations, is about to begin an inevitable decline as a manufacturing power.

Few share that extreme view. Indeed, some companies—those that import equipment necessary to their businesses—welcome the stronger yen. Most are not that lucky.

The dilemma posed by endaka, as the high yen is called in Japan, is simple, says Toshio Miamoto, managing director at Sony Corp. Compared with the dollar, the yen is now worth 50% more than it was in September 1985. All other things being equal, a company would have to raise its prices by 50% to maintain its profit margins. But to remain competitive, Sony has had to limit its price hikes to no more than 20%, and that applied to only a few products, Miamoto says. The difference has to be made up elsewhere.

The obvious solution is to cut costs, which all Japanese companies are trying to do. Hindering such efforts is the long-established policy of lifetime employment at large companies. Layoffs come only when "you've lost your last trump card," says Miamoto. "In Japan, the labor wage is a fixed cost," he adds.

The alternative, of course, is to find cheaper labor elsewhere. "Japanese companies... will have to move some of their production overseas," says Tsuneo Uraki, general manager of the Marketing and Product-Planning Division for Hitachi Ltd.'s Computer, Telecommunication, and Office Systems Group. "Hitachi is building its 5-gigabit drives for large computers in Oklahoma. Consumer and components manufacturers may have to step up their purchases from NICs [newly industrialized countries], where good components are available. Hitachi may buy terminals from NICs."

Complicating the move offshore is the fact that the offshore countries are now competing with the Japanese. Partly in response, the Japanese are trying to promote their products as high-quality items, unlike the low-cost merchandise sold by the up-and-coming Asian countries. "Competition with Korea is very severe, but to a large extent only in standard products," says Sutezo Hata, senior executive managing director of Hitachi. "The development capabilities of the Koreans is not great. We can compete by stressing sophisticated products and newly developed products." Again, the effort is ironically similar to the claims of American companies a few years ago that the Japanese excelled at producing cheap, imitative commodities but couldn't really compete at the top of the line.

Most companies are combining a number of approaches. "There are two strategies to cope with the high yen," says Hajime Sasaki, vice president of the Electron Device Group of NEC Corp. "We must sell high-value, advanced products, and we must move more production to lower-cost regions. The U. S. probably has cheaper labor costs than Japan. The NICs have even lower labor costs."

And some companies don't need to take any approach; the high yen works in their favor. For example, Sachio Senmoto, senior vice president of Daini-Denden Inc., one of four new common carriers challenging Nippon Telegraph and Telephone Corp., says that the rising currency helps his company because the U. S. and European equipment it uses is now cheaper.

But most electronics companies are net exporters, not importers. "Something like 50% of Japanese electronics products are exported overall," says Hata of Hitachi. "Many of our customers have export ratios of 60% to 70%."

The situation has left some Japanese managers uncharacteristically pessimistic. "There are no measures that are truly adequate. Neither cost reductions nor price increases are sufficient," says Yutaka Iuchi, division general manager of Information Systems Laboratories and group deputy general manager of the Information Systems Group at Sharp Corp. "Sourcing overseas is not a complete answer, because we don't want to weaken Japanese industry. If a manufacturer merely handles products from low-cost producers and loses the characteristics of a manufacturer, it will soon come to an unhappy end."

Sony's Miamoto takes an even bleaker view. He thinks Japan is slowly going the way of the U. S. and Europe, toward a declining manufacturing base. "It's inevitable." he says. "I'm always telling my U. S. and European friends, 'Don't worry. We are following you.' "

EUROPEANS WORRY ABOUT BEING RUN OVER BY THE U. S. AND JAPAN

The most important single issue confronting the European electronics industry is the growing threat of domination by the far larger U. S. and Japanese industries. For both executives and technologists, the question more than ever next year will be whether their businesses are in danger of being overrun by the competition from the West and the East, and if so, what they can do about it.

European executives agree that the overseas competitors represent a serious threat, although they disagree on the extent of that threat and what should or can be done about it. Most, however, do not favor wide-ranging intervention by their governments, generally on the grounds that nobody can win an all-out trade war.

One obvious alternative—cooperative efforts in research and development—gets mixed reviews. Many question the effectiveness of such existing projects as Alvey, the British fifth-generation computer program, and Esprit, the pan-European effort to develop information technology. Overall, though, European industry figures support such projects in principle, believing that if nothing else, they teach their members valuable lessons working together.

Whatever the possible countermeasures, the overseas competition is very much on their minds. "The U. S. and Japan are overrunning us to a major extent," says Bob Hunt, general manager of the Semiconductor Division at STC Components Ltd. in the UK. "The thing to be done is to improve our own capability. The problem in improving our own capability is the smallness in scale of our industry compared with Japan's."

Others take a more measured view. "There is real competition from Japan and the U. S., but I don't think they are overrunning Europe," says Doug Dunn, managing director of Plessey Semiconductors Ltd. in the UK. "There is a high use of U. S. and Japanese components in European systems. The European component industry should redouble its efforts to strengthen itself in its own market segments."

The idea that the threat from the U. S. and Japan is very real, but that European companies can and do compete in selected market segments, is widespread. "The semiconductor market is dominated by the U. S. and Japan," says Peter van Cuylenburg, managing director of Texas Instruments Ltd. in the UK and vice president of TI's worldwide semiconductor group. "But in equipment, the European companies are much stronger. In the consumer market, the Japanese are predominant, but high-definition television could change this. Automotive is a big growth area. There is not an area of car electronics in this country in which there isn't world-class activity taking place."

In some cases, recognition of the U. S. and Japanese position amounts to acceptance of it. "If some of their products are better, why not accept it, the same way women accept French perfume as apparently superior?" asks Lubo Micic, managing director of the ITT Semiconductor Group in West Germany.

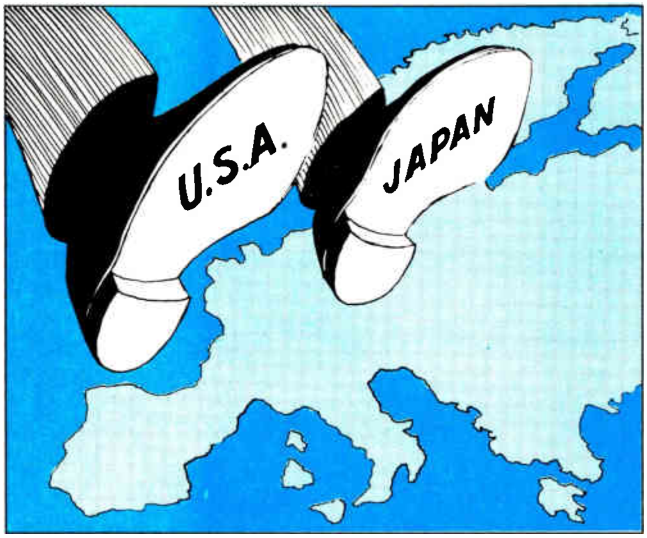
Regardless of how its members view the competition, the European electronics industry generally does not believe governments should protect them. Most industry figures argue for fair competiton, not less competition. "We strongly support free trade," says Hans Weinerth, a director at Philips GmbH in Hamburg in West Germany. "But it must be fair." As long as conditions are not equal, "we cannot afford to do without the customs levied against semiconductor imports."

Full-scale protectionist measures against all overseas competition would not work, most observers agree. Aside from whatever value they assign to free markets as such, they fear retaliation. Micic, of ITT, points out that his company exports 60% to 70% of certain components.

At least one executive believes the answer lies neither with competition nor with protection, but with cooperation. "I think major equipment manufacturers in Europe should form technical alliances with powerful component suppliers and set up a mechanism where U. S. suppliers assist European manufacturers in getting access to leading-edge technologies," says van Cuylenburg of TI Ltd. "In return, they give U. S. suppliers a large share of business."

As for the potential for cooperation among European companies themselves, opinions vary widely. STC's Hunt says, "Alvey has done us an awful lot of good. It has got us to a position of advanced technology very quickly." But Paul Wynter of Advanced Text Systems declares, "Alvey and Esprit are a load of rubbish. Alvey is no benefit to anybody. You have to go through too much to get into it. It is all government PR. It can't effect marketing changes."

The general view is somewhere in between. John Brothers, a MOS development executive at Plessey, finds the projects valuable because they lessen risk. "You are just not as worried in putting 50% of the money into a project as you would be if you were putting 100% in," he says. He does have reservations: "The problem with these projects is that they are too long-term, say three to five years, and things change quickly. It is not easy to redirect the programs as things change in general."



Regardless of the obstacles, though, European companies eventually are going to have to cooperate at least in the pre-competitive stages of research and development, says Richard Epple, director for European research programs at AEG Research Center in West Germany. The value of the current programs may lie in their helping to make such cooperation easier, he says. The director of AEG Research Center, Stefan Maslowski, agrees: "Joint projects are teaching us to get along with each other."

says Dan Maydan, vice president for the firm's Applied Deposition Technology Division. "Today, that's not enough. We have to demonstrate that the system is very reliable, that it is fully automatic, and that it is particulate-free."

"The thing that's most troublesome is making sure a system is [fully compatible], that it has all the interconnection capabilities you need," says Blaine Davis, corporate vice president for strategic and market planning at AT&T Co., New York. "In a closed [computer or network] architecture, bringing out new products is easier, because you don't have to worry about being able to accommodate other companies' products. But AT&T doesn't believe that the world is waiting for another proprietary architecture."

The very newness of new products can create education bottlenecks. Two types of efforts are aimed at this problem: supporting the user with tools and training, and making the product easier to use in the first place. In the field of semicustom ICs, for instance, "it is becoming necessary to interface closely with customers and provide more support," says Sutezo Hata, senior executive managing director of Hitachi Ltd.

With completely new products, "the major problems are not in development," says Tsuneo Uraki, general manager of the Marketing and Product Planning Division of Hitachi's Computer, Telecommunication, and Office Systems Group. "Perhaps the major problem is that products are not designed to be sufficiently easy to use," he goes on. "The end user in general doesn't have time for new things because of a backlog of old work."

Users of semiconductors need training too. "Coming from semiconductor producers is a heavy innovative pressure, and it is especially the small and medium-sized firms that are having difficulty adapting to this pressure," says Philips' Weinerth. Although chip makers are introducing new devices rapidly, he says, many users take too long to make them work in new products, so Philips and others are lending a hand in applying new circuits.

Power MOS FETs and power ICs, for example, "require engineers to relearn how to design their products," points out Alex Lidow, executive vice president of manufacturing and technology at International Rectifier Corp., El Segundo, Calif. He says it has taken seven years to establish enough knowledge of power MOS FETs such that rapid market growth can now take place.

New products may be needed to stimulate renewed market growth, but a slow market makes it difficult to introduce products. "The biggest bottleneck we have right now is paying the bills," says Charles Minihan, senior vice president and general manager for Perkin-Elmer's Semiconductor Equipment Group. "You can't fund R&D if sales are just too low and you don't have any money coming in."

Even after a product is ready, it stops in its

Although most electronics executives don't see direct harm to their companies in the new tax law, they agree it will make economic recovery slower in coming

tracks if market demand is too depressed. "There is lots of interest, but delays in buying," says SGS's Queyssac of some new products.

"The biggest bottleneck in 1986 has been the flatness of the market, which we think will change next year," agrees Nicholas Matelan, president of Flexible Computer Corp., Dallas. However, one of the biggest roadblocks to increasing business, he feels, is the tax bill.

When asked about the new U. S. tax code's effects upon their businesses in general and with respect to capital and R&D spending in particular, executives in the electronics industry are on the whole negative. A very small minority of those surveyed say their companies will be paying less taxes; outside that group, the best thing they can say for the new law is that its passage has relieved the uncertainty that prevailed while Congress worked on new tax legislation.

Many of those surveyed think the new code will have relatively little direct effect on their companies. Few think it will cut noticeably into R&D spending. Most, however, cite its dampening effect on capital spending and on business in general. And some representatives of the semiconductor industry say their companies are being materially hurt by the new law.

"Two things were left out of the tax code: help for small companies and tax-loss carry-forwards," says Matelan. "I think this is stupid, because 80% of all new jobs are created by small startup companies." Not only does the law offer no special aid to startups, but it will contribute to a general slowdown that will depress startup activity, according to Data General's Miller.

"I agree with the school that says it will have a negative impact on the economy for some time to come," says Gordon R. England, vice president, research and engineering, at General Dynamics Corp.'s Land System Division in Warren, Mich. By removing investment incentives, he says, the tax code will slow capital spending.

"The dilution of the tax credit [on capital goods] has made our customers much more cautious with their capital," according to Richard J. Boyle, vice president and group executive at Honeywell Inc.'s Industrial Systems Group in Minneapolis. As a result, "many of our marketplaces will be characterized by more cautious spending." The new code could lead to continued sluggishness in the computer business, he continues. "I think it will be a damper on many of the capital-goods markets."

Although Fiebiger of Mostek, Queyssac of SGS, and others do not think their companies will be harmed, many semiconductor executives are not so sanguine. Lidow from International Rectifier calls the tax reform "one of the most foolish policies of the last decade," largely because it eliminates the provisions for fast depreciation.

"The new tax code is going to cause an overall reduction in capital spending and will have a negative effect on the industry in general," says Richard Funk, manager of standard IC applications at GE/RCA Solid State Division, Somerville, N. J. "The semiconductor industry is very capital-intensive. This is going to put very severe limitations on our ability to compete, and I think the government is going to have to take a second look at this. They'll have to modify it."

Not surprisingly, suppliers of capital equipment to semiconductor houses stand to lose. "I'm worried about the [loss of rapid] depreciation and the investment-tax credit," says Perkin-Elmer's Minihan. U. S. chipmakers will be less able to buy new equipment, and he thinks they need to do just that. "They need to revise their whole approach to manufacturing, and [the tax code] is going to slow things down."

TECHNOLOGISTS: TOOLS TO DRIVE CHANGE

Next year will bring major advances in software tools: among them should be better silicon compilers, tools for writing programs, and expert systems for fab lines

Managers heading up research and engineering efforts in the worldwide electronics industry see the prospects for 1987 brightened considerably by the growing availability of better engineering tools to carry out their work. In *Electronics'* annual survey of industry executives on the outlook for the coming year, the research and engineering managers are quick to agree with industry leaders that the pace of technology change will continue at a good clip. They expect to achieve this progress with improved tools, such as silicon compilers, computer-aided software generators, and expert systems, which they see coming on stream next year.

These tools are badly needed, too, because of the shortage of first-rate systems designers and manufacturing engineers. Some schools are moving to fill those needs, technologists say. The technologists don't expect manpower shortages to slow progress in the semiconductor sector in 1987, but the pace there is so furious that the rest of the electronics industry will be hard pressed to keep up.

Despite the hoopla and size of major military research and development programs, they will not be the technology drivers next year. Many technology leaders doubt whether the Strategic Defense Initiative will have any commercial impact in the near term, and they give the Very High-Speed Integrated Circuits program mixed notices at best.

Hanging most tantalizingly on the horizon now, according to technologists, are workable silicon compilers. Also not too far off, they say, are tools that will make it easier to write complex software. Artificial-intelligence techniques are expected to be brought to bear on the program-writing task. Expert systems could become important tools in the manufacture of ICs, aiding the operators of complex fabrication equipment. And software may also soon be available that helps engineers and researchers to pool their knowledge more efficiently.

. Some silicon compilers are available now, but they are still regarded by many development engineers as embryonic. Major improvements are expected soon, so that engineers unfamiliar with IC design will be able to implement their systems in silicon without bringing in specialists to handcraft chip designs. One big deficiency of the current compilers is their inability to combine analog and digital circuits on a chip.

Overall, the level of dissatisfaction with the compilers remains high. They "far from satisfy our needs, as they lack complexity and flexibility," says Lubo Micic, managing director of the ITT Semiconductor Group, based in Freiburg, West Germany. With present systems insufficiently automated, the user must do too much work himself to make the best use of chip area, trying out different layouts. "We are dreaming of a fast and high-performance product that requires little human intervention," says Micic.

Others would forgo some automation in favor of broader capabilities, especially the ability to design analog chips and mixed analog-and-digital chips. Intersil's Charles Thurber is one of those waiting for "a really good, efficient layout tool, like a silicon compiler, for both analog and digital systems. I would be very happy to do all the layout if the tools were available," he says.

Takao Matsui, group executive in charge of technology at Toshiba Corp.'s semiconductor group, Tokyo, is another who wants a good set of analog-chip CAD tools, even if they aren't as automatic as a compiler. "Chips for consumer products account for about half of Toshiba's production," he says. "In this field we need many kinds of linear ICs." He especially wants a good test-pattern generator for analog circuits.

"In power ICs, we need CAD equipment and software to close the loop between testing, design, and simulation," agrees International Rectifier's Alex Lidow. "Progress in digital is well along, but not even started on the analog side."

"The industry needs better linkages between different CAD software packages, which are themselves okay if they could communicate," says SGS Semiconductor's Daniel Queyssac. And Apple Computer Inc.'s Lawrence G. Tesla, vice president of advanced technology, wants "a vendor-independent set of chip-design tools that let us do designs and go to more than one vendor. Typically, design tools fit only one vendor. But there are times when we understand fully what we want to do, low cost is critical, and we need to be able to get bids and go with lowest cost."

Others are looking for CAD tools that help with design not only at the chip and board level, but also at the systems level. Hitachi's Tsuneo Uraki says that a work station for systems design is under development at his company. "Such a work station is hard to buy, because its design is closely tied in with development methods." Systems are also needed for simulating and documenting systems-level designs, he says.

Systems engineers doing chip designs find themselves trying to work with IC design tools, says TI's Gollapudi Mohan Rao. He says the industry needs a way to translate silicon knowledge to printed-circuit-board design. "You could call it a true silicon compiler, true pc-board compiler, or true computer compiler. We need it and I think it is going to come," he predicts. David Topham, business manager, Cambridge Interconnection Technology Ltd., Cambridge, UK, wants "a system compiler so it can be a total package."

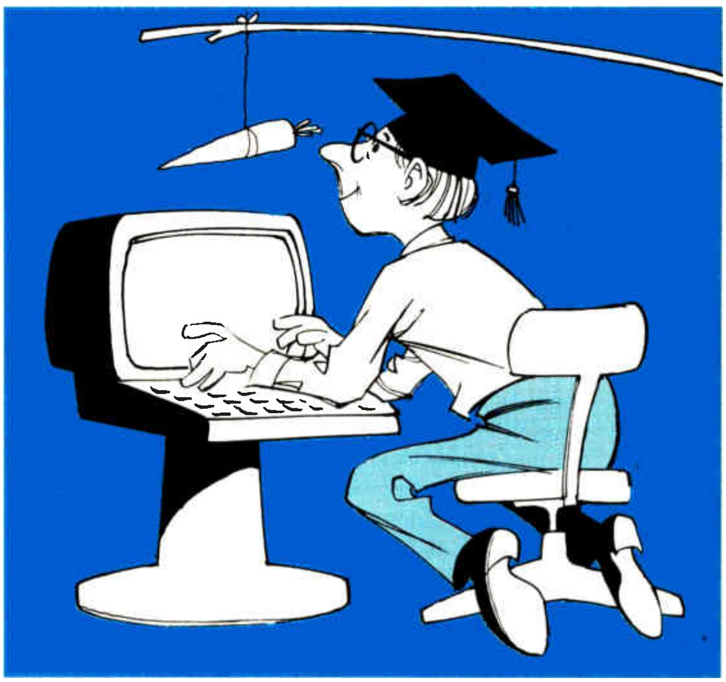
CAD software may come more and more to the aid of software writing itself. "Some type of software CAD is needed," says Sharp's Yutaka Iuchi. "Writing software requires the majority of personnel." "We must step up the use of AI to increase the quality of software," opines Kunio Ohkuwa, manager of the business, marketing, and product planning department of NEC Corp.'s Information Processing Group. "We must also use AI to increase software productivity."

"Internally, I see tools on the brink of a breakthrough for software productivity," says Northern Telecom's Timothy Sullivan. "I also see new tools that will help us better integrate and test the many options as we bring our products together. That is on the fringes of AI."

TI's Mohan Rao thinks AI will also soon come to the aid of process engineers. "Complex equipment must be built with expert systems that will automatically—99% of the time—perform diagnostics, synthesize the analysis, and take corrective actions," he says. "If you have a very expensive direct-step-on-wafer system which does not have effective throughput, you want an expert system to take care of the problem."

Tools may also soon become widely available

Electronics companies are competing for students who master manufacturing skills; they also want graduates who can combine technologies on a systems level



In the semiconductor sector, the pace of change is quickening—and systems makers say they are finding they can't keep step with the technology advances

that, instead of adding AI, serve to amplify human intelligence. Lynn Conway, professor of electrical engineering and computer science and an associate dean of the College of Engineering at the University of Michigan, Ann Arbor, points to a developing discipline known as collaboration technology or "group computing." It goes beyond distributed processing and computer networking to deal with tools "to aid with group processes," Conway says. "It's the development of software tools and protocols for interacting so people can have more productive meetings."

One narrow example is software tools used at Xerox Parc (Palo Alto Research Center) that help people keep track of an evolving argument or process involving multiple individuals participating at their own screens. These tools allow an individual to come back to his screen after an absence and more easily pick up on the process at the point where he left off. Conway says there is "a groundswell of research activity" in the field right now.

Many of the automated tools will help electronics manufacturers overcome their biggest staffing problems, for industry leaders agree that there is a worldwide shortage of top-notch manufacturing and systems engineers. These disciplines are becoming increasingly important as companies seek to cut manufacturing costs and increase the functionality of their products.

"Manufacturing skills are golden," says International Rectifier's Lidow. "Good manufacturing engineers are extremely important, [but] the supply is always short," adds Maxtor's James McCoy. Help is on the way: a few universities have begun to offer manufacturing engineering programs, says Donald Atwood of GM/Hughes Electronics.

Manufacturing skills are not the only ones in demand. U. S. executives say that more than any particular specialty, they want engineers with broad backgrounds, capable of tying together technologies on a systems level. "The toughest ones to find are engineers who can apply technologies such as integrating fiber with signal-processing components and software," says Northern Telecom's Sullivan. That's why technologists praise the programs at the top engineering schools, Ivy League universities, and some of the better land-grant institutions, which have broad engineering programs.

Most industry leaders say that most of all they want bright, flexible engineers who are not too specialized. "We need multidisciplinary people," says Dan Maydan of Applied Materials.

The British also say they are short on practical, multidisciplinary engineers, while Japan faces a shortage of software engineers. "We are trying to hire [software] engineers," says Toshio Miamoto, managing director at Sony Corp., Tokyo. "But we cannot hire all that we want."

The British problem is altogether different, says Topham of Cambridge Interconnection Technology. "Practical engineers are needed," he says, "people who know which end of a soldering iron is hot. There are a lot of software engineers, but not enough real engineers."

GE/RCA's Richard Funk agrees. "Too many engineers are coming out of school oriented toward software and computer architecture," he says. "Hardware and laboratory experience are not getting as much attention as they used to."

Meanwhile, industry presses on. Managers of engineering and research see the pace of technological change as quickening in the semiconductor sector, but lagging in the rest of the electronics industry. Top engineering managers say that new tools and acute competition are holding chip makers to a feverish pace as they race to scale down geometries. The pace is so fast, in fact, that systems makers can't pack these new devices into functional equipment before the next-generation products are hitting the street.

"While integrated circuits get denser, faster, and more complex, systems makers find it hard to put these advances to use in their products," says ITT Semiconductor's Micic. "Hardware just cannot keep step with technology."

Fueling the competitive race are several factors, including economic considerations and advanced design tools. "The pace of technological development is speeding up," says Plessey's John Brothers. "I don't think silicon technology will slow down for 10 years, [because] the capability to design things has improved."

Not everyone is convinced that the technological growth curve will continue to rocket, however. "It's flattening out," says RCA's Funk. "The worldwide capacity for making chips is out-stripping the available sockets, and the markets for computers, automobiles, and other equipment that use semiconductors is limiting the pace of technological growth."

Others say that as the technology matures, economic factors play an increasingly significant role. "If in the past the rate of technological change was determined by physics and engineering, in the future economic considerations will become an increasingly important factor influencing change," says Philips' Hans Weinerth.

Mohan Rao says chip technology will maintain its current growth rate for the next decade. He says memories are becoming more complex at a rate of about 35% to 40% per year, and random logic is increasing in complexity at about a 20% to 25% rate. That pace will remain steady until the next boom market begins to accelerate the semiconductor industry, he thinks.

As to what will push technology—at whatever pace—most technology leaders think SDI will be a major driver in the years to come, but debate lingers over how well SDI-derived advances will be integrated into commercial products. Many also worry that the VHSIC program, a Department of Defense project that is aimed at producing high-speed military ICs, may be too narrowly focused for its technology to make its mark in commercial products

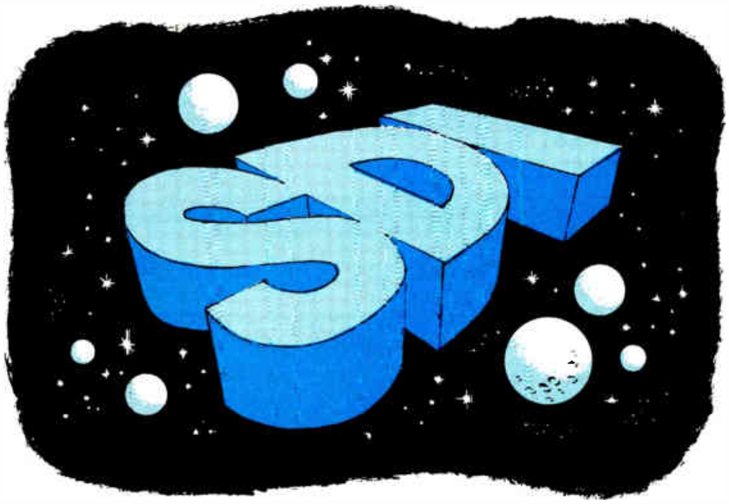
"I have no doubt that simply attempting to do [what SDI calls for] is going to open up new frontiers in materials, information systems, sensors, and so on," says University of Michigan's Conway. But, she adds, "there's a question of whether we'll be able to exploit the stuff we get out of SDI for other than military purposes."

It seems clear that SDI will significantly effect development in some areas—particularly software and computing, for example—but other technologies, such as semiconductors, will be virtually unaffected by the program. "You are not likely to take the leading edge of [chip] technology and put it into a space application," explains Fiebiger of Thomson Components-Mostek.

SDI supporters point to the credit the space program was given for advancing technology in the 1960s and 1970s, but others—including those who dispute whether the space program played a major role in driving technology—say that SDI is different from past government programs because of the politics involved.

"I don't put it in the context of either a technology driver or a waste of money," says Honeywell's Richard Boyle. "I believe it's serving many purposes, both defense-wise and as a negotiating tool."

Boyle and others, such as Atwood of GM/Hughes Electronics, agree that only time will tell whether SDI technology really filters down into mainstream commercial products. "The big quarrel is that so little is known," says Atwood. "People say we shouldn't spend so much money when we don't know what's going to be produced, but at the same time, the benefits to be gained are such that I support going ahead."



The Strategic Defense Initiative may be a technology driver in the years to come, but a strong debate is raging over its likely impact on commercial products

Others can see explicit payoffs. "I came from Bell Labs and was involved with SDI," says Maydan of Applied Materials. He thinks SDI will spur "the development of really big computers that will push new technologies."

The VHSIC program also has strong backing from executives and engineers. "VHSIC has been very successful," says Gordon England of General Dynamics. "It's influenced a lot of programs and products." He says the VHSIC program has been "directly beneficial for military signal and image processing, and it's been a driver in the commercial market."

But the program does have its critics. "VHSIC is in the wrong hands and is having limited impact," says Lidow of International Rectifier. VHSIC is "giving some drive to develop higher-density chips," says Maydan, "[but] it hasn't been organized to get the most out of the program." He says the program sought to step too far ahead of the current state of the art in semiconductor technology, and that in doing so it may have missed developments that could have come from the intermediate stages. "Usually, technology cannot jump," he says. "You have to go step by step."

VHSIC may already have affected commercial semiconductors by pressuring suppliers to squeeze chip geometries below 1 μm, but those new parts will take time to make it into military systems, let alone commercial products. "I don't see VHSIC as an art now being applied to future military systems," says Charles Minihan of Perkin-Elmer. "And it is not a technology driver—yet, at least—for commercial products." □

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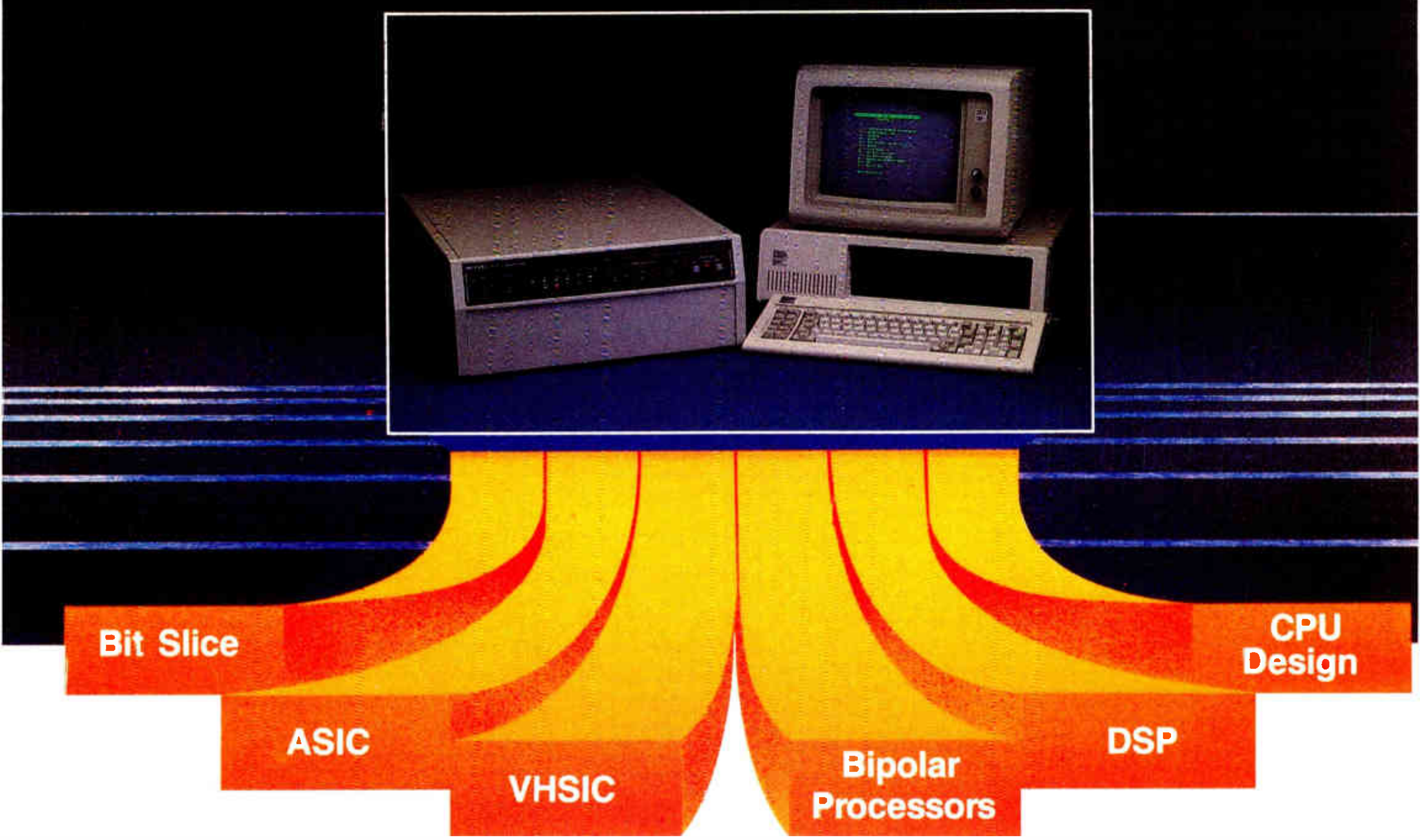

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PROBING THE NEWS

THE COMPETITION EXPLODES IN POWER MOS FETS

OUTLOOK IS FOR 40% ANNUAL GROWTH, BUT A SHAKEOUT MAY BE COMING

by Larry Waller

LOS ANGELES

The competition has turned scorching hot in power MOS FETs. The reason is simple. In a semiconductor business that currently is growing slowly at best, power is one of the fastest-growing segments, and more chip makers are trying to grab a piece of the action. A business where U. S. companies still dominate, power is shooting ahead for solid reasons—MOS FET drive circuitry is simpler and operating frequencies are higher than those of bipolar power transistors. Because of these advantages, MOS FETs are displacing their bipolar cousins at a rapid pace and are opening up a wealth of new applications—including some highly attractive ones in the auto market.

The prospect of a worldwide business growing at what some participants think could run at a 40% annual clip over the next five years from a 1986 base of $210 million has competitors investing heavily. The top three players in particular—in order, International Rectifier, Motorola, and Siliconix—have anted up impressive amounts for product and technology development and manufacturing capacity. They aren't alone. As the battle for customers intensified in 1986, other big competitors from the U.S., Japan, and Europe have spent more money to develop MOS FET products and expand their activities.

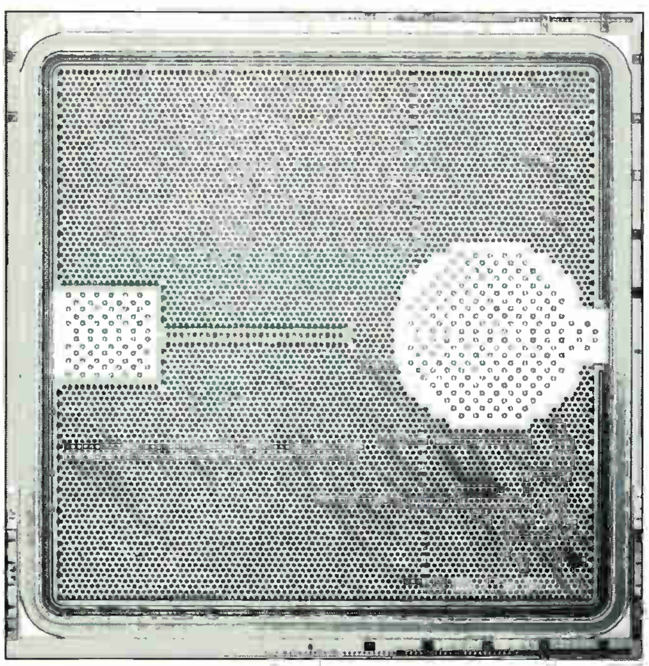
While each player predictably insists that it has its own proprietary edge in technology or quality with its MOS FET parts, all of the competitors acknowledge that the current fight hinges on one factor. As one industry consultant puts it, "The MOS FET battle will be fought on that most basic of all sales issues—price." Agreeing is Paul V. White, vice president of marketing for Motorola's Discrete Semiconductor Group. "There's product, reliability, and price. We're all pretty much even on the first two. So what does that leave?"

Consider what happened this year to two typical parts. The high-end IRF440, a 400-V model, slid from $12.35 to $8. And the commodity IRF520, rated at 100 V, dropped from $1.11 to 90¢. MOS FETs had traditionally cost more than bipolar equivalents; now there is virtual parity for some parts.

Market leader IR, which had the field to itself for several years after the introduction of its Hexfet in 1979, sees the issue similarly, though it still claims a technology advantage stemming from its basic MOS FET patents and its longer experience in building the devices. "There's less and less product differentiation," concedes Alex Lidow, executive vice president for manufacturing and technology. "With time, MOS FETs become more and more of a commodity."

So the contenders have honed strategies, put their facilities in place, and sent marketers out on a blitz for more customers. Seven companies are fighting for market share (see table, p. 98), maneuvering to capture the high ground, especially in the U. S. market.

■ **International Rectifier Corp.** The El Segundo, Calif., company is moving at flank speed in its effort to hold onto its No. 1 ranking. It hopes to gain a price advantage through manufacturing efficiencies gained from a new $80-million plant designed to build MOS FETs. The plant will triple IR's capacity when it reaches full-scale production next year. Derek Lidow, executive vice president for marketing, says the goals are a "50% reduction in costs, which will permit us to take the price leadership." Furthermore, he says, the production cycle has been cut from weeks to only four days, which he says will enable IR to deliver product 10 days after receiving an order. But the cloud in the bright outlook is what one industry observer calls "IR's financial pressures from the cost of building such an expensive plant for a $145 million company."



DENSE. Motorola's TMOS IV chip houses more than 1 million cells/in.² and is designed to withstand high energy in the avalanche mode.

■ **Motorola Inc.** The largest U. S. entry in MOS FETs, and the world's leading discrete component supplier, finally got its act together in 1986. Among other moves, it dedicated a Phoenix fabrication line to making power devices; previously, they had been built in shared facilities. The Phoenix-based Discrete Semiconductor Group has made major commitments across the board to MOS FETs, beefing up design and marketing efforts, and earmarking even more of Motorola's massive MOS production capacity for them. Manufacturing is under way at Austin, Texas, and Japan, and work is scheduled to start next in Scotland. In pricing, Motorola played the major role in forcing levels down faster than the normal learning curve would call for, by up to 40% in the highest-volume, low-power lines. Nevertheless, some analysts believe the strong Motorola move, long expected by competitors who fear the firm's manufacturing and financial muscle, comes several years late. They say it was delayed by conflicting priorities with the company's profitable bipolar transistor business, which amounts to more than $300 million yearly.

■ **Siliconix Inc.** The company is building its MOSpower line in the industry's only facility that employs 6-in. wafers and does fabrication in Class 1 clean rooms. Siliconix executives say the plant, costing more than $30 million, gives the company the highest device yields in the business—some 11 times better than the common 4-in.-wafer-based production—meaning Siliconix is as well-armed as anyone to handle cost-cutting strategies. The only caveat from market watchers is whether it will stay the course in a commodity business, as its usual strategy is to target profitable niches. David Cooper, director of MOSpower for the Sunnyvale, Calif. company, says Siliconix is committed "to be one of the top two or three in MOS FETs."

■ **Hitachi Ltd.** The Japanese chipmaker ships only a moderate volume of power MOS FETs to the U. S., where they are used largely in personal computers and minicomputers for switching power supplies where frequencies exceed 100 KHz. Hitachi's S Series, employed instead of bipolar versions in audio amplifiers, fills a need that U. S. firms cannot meet, the company says. These devices provide 10 W to 125 W output at audio frequencies and 120 W at 100 MHz. Hitachi says it still plans to address mainly its home market, which has needs somewhat different from those in the U. S.

■ **Toshiba Corp.** The company is building a presence in the U. S. market with devices in the upper MOS FET power ranges—25 A, 500 V—and higher. It is avoiding the product areas of 150 V and lower, where competition has been most heated, says David Lanthier, product market manager at Toshiba's Electronic Component Business Sector in Tustin, Calif. The company has a substantial automotive effort in Japan and is planning to pursue this segment in the U. S., too. In the overall MOS FET picture, however, Toshiba would hold back its plans if price-cutting goes too far, he says.

■ **Siemens AG.** The Munich, West Germany, company earlier this year sold its Broomfield, Colo., plant, so it does not produce its SipMOS devices in the U. S. But it has plans to start building them again early next year in Santa Clara, Calif., where a new

IN SMART POWER, U.S. FIRMS LEAD

International Rectifier	50*
Motorola	35
Siliconix	30
Hitachi	24
Toshiba	21
Siemens	20
GE/RCA	18
Other	12
Total	210

*Worldwide sales, millions of dollars

SOURCE *ELECTRONICS*

power semiconductor division is now being set up. Responding to industry speculation that drastic price decreases earlier this year spurred Siemens to drop U. S. production, George Fodor, marketing director at the firm's U. S. division, says that Siemens, the European leader—with some 30% of the business—will continue to serve the U. S. market.

■ **RCA/GE.** The major question at the RCA Solid State Division in Somerville, N. J., a pioneer in power devices, concerns who will own the operation. Parent General Electric Co. is reported to be shopping around its entire merchant semiconductor operation, although there has been no official confirmation. One report names Siemens as a potential buyer, along with several Japanese companies. However, RCA, showing no apparent effects of the uncertainty, continues to hustle for business: it has brought out its MegaFET high-density device, which has 2 million cells per square inch. It also has won a $1 million development contract for radiation-hardened MOS FETs from the government.

If the marketing battle is hard on participants, it will certainly make things easier for customers, who can expect lower prices and better service. This has not been the case all along, because power MOS FETS have been used principally by the military in switching power supplies, where higher switching frequencies pay off with better overall efficiencies and cheaper transformer costs. With such limited market potential, prices stayed up.

Now, as prices continue to decline, the devices look like the power answer for new designs of industrial controls, power conversion, and perhaps ultimately the biggest market of all, variable speed control of electric motors. Modules designed for that task are moving toward the market from most companies and should surface next year. Siliconix, for example, has a module for variable control of air conditioners that uses six MOS FETs, and IR's Sixpak module powers Winchester disk drives.

Marketing executives aren't just looking at 1987 for solid growth. In fact, they are counting the days until 1988, when they expect to see the advent of a market many feel will be the best yet for MOS FETs. Says Siliconix's Cooper, "Automotive—that's the next real acceleration for MOS FETs."

Because automakers are even more secretive than military contractors, the MOS FET firms cannot discuss specific plans, but all of them have development links with the car companies. The potential is there for the power devices to replace the numerous relays on today's autos, and for switching via common buses that will replace miles of wiring in new models. Other potential applications are for motor control in "smart power" packages, which combine logic and MOS FETs, and for solenoid drivers.

While the next year should be an exciting time for MOS FET suppliers, the extreme pricing pressures likely to prevail will leave no room for inefficient producers. There could be a shakeout, and those close to the industry say that it would be no surprise in a high-stakes market segment such as MOS FETs to see an eventual lineup of no more than three major contenders. One would be Motorola, leaving IR and the others to fight it out for the remaining slots. As Ron Bohm, industry analyst at market-watcher Dataquest Inc., diplomatically says, "there will be a smaller supplier base after a year or so." □

IS THIS THE LAST ROUND OF MOS FET DENSITY DERBY?

MOS FET suppliers have traditionally showcased their technology by pushing densities ever higher, shoehorning more power cells onto the die. Not only does higher density help reduce the key on-resistance specification—which cuts power dissipation—but it also spotlights manufacturing skills.

The latest round of MOS FETs is an example. All of them have substantially more cells than the previous industry standard of 1 million/in.^{2}. RCA Corp.'s MegaFET even boasts double that, with on-resistance lowered to 1.5 mΩ/square.

But this is the last round of the MOS FET density derby, predict technologists at International Rectifier Corp. and Motorola Inc. The cost of building chips denser than 2 million cells/in.^{2} is not worth the benefits.

Instead, IR and others are recommending that customers choose a specific device for applications based on the optimum cell density in relation to desired voltage. Since this measurement is heavily cost-weighted, the standard is likely to become one that some buyers already employ: pennies per ampere at a given breakdown voltage. Now, the lower industry pricing level is 2¢ to 3¢ per ampere; IR says it expects to push this toward 1¢ at its new plant. *–Larry Waller*

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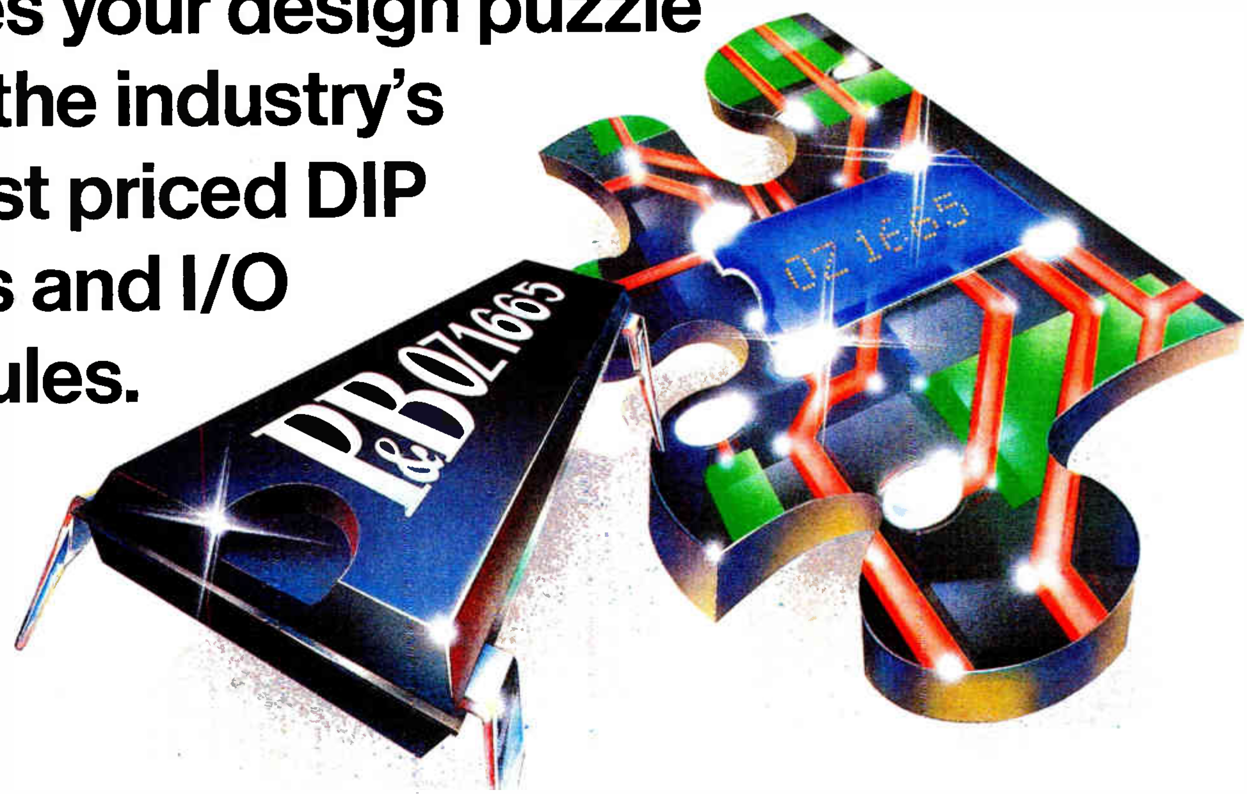

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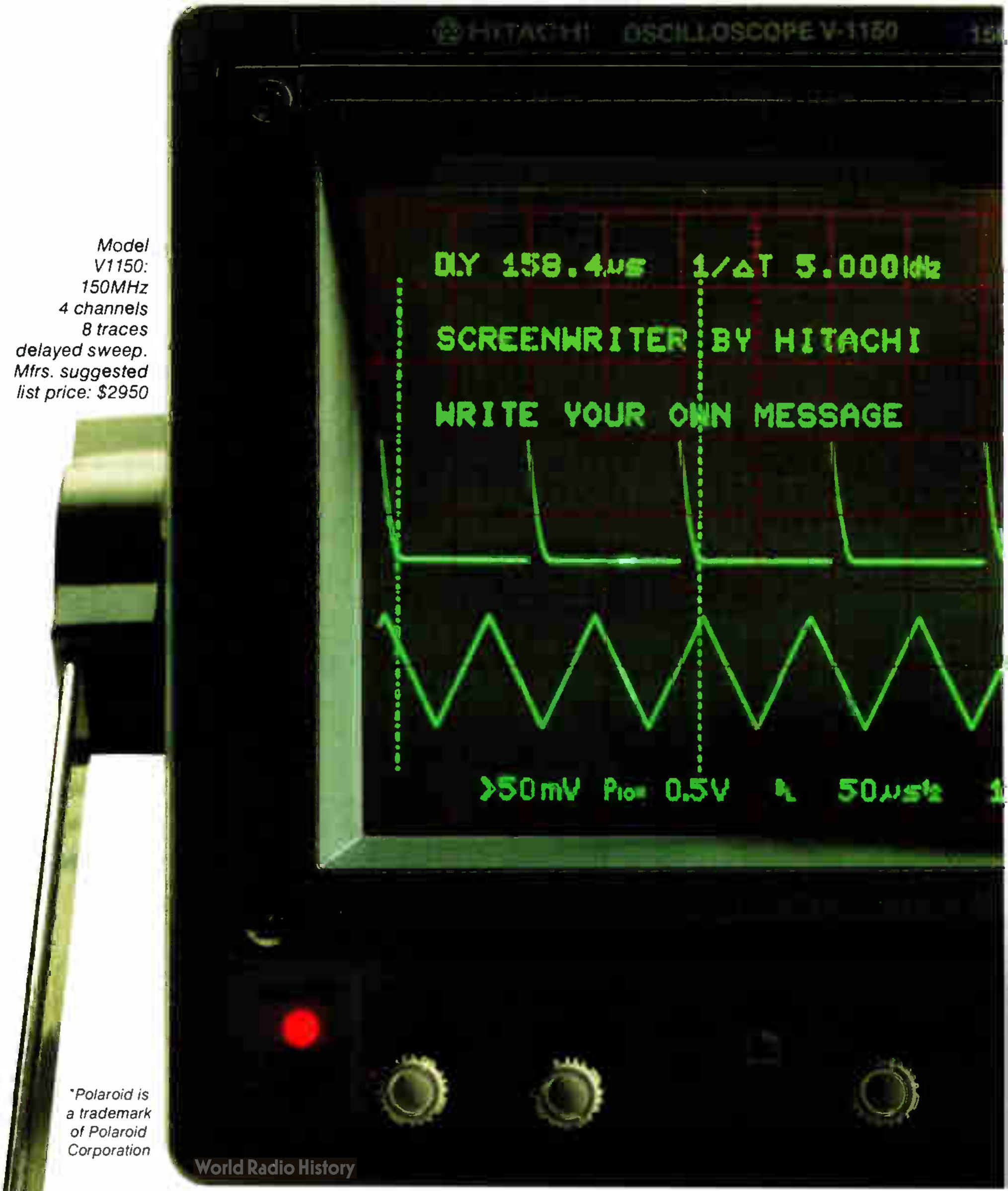

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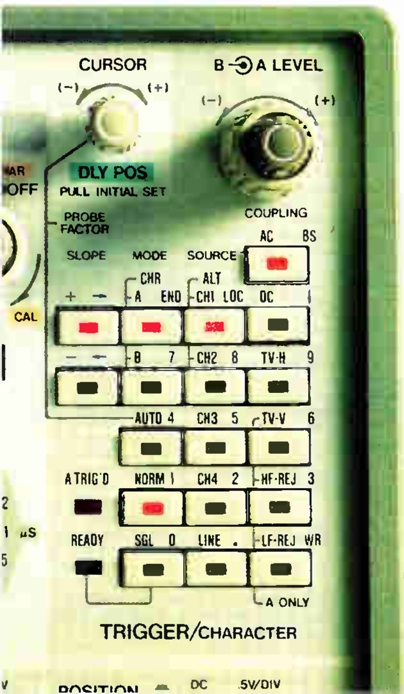

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THE DOOR IS OPENING FOR CHIP-ON-BOARD ASSEMBLY

LOW COST AND HIGH DENSITY MAKE IT IDEAL FOR SMART CARDS

by Jerry Lyman

NEW YORK

Chip-on-board assembly—still a niche market in the U. S., but one with tremendous potential—is finally solving the various technical problems that have held it down. COB is now catching on in a growing variety of applications because it can provide high density and good performance at a low cost. And what could give the assembly technique a boost into the big time is the smart card, with its embedded chips, which may be on the verge of becoming a major mass market (see p. 55).

Because it is just about the ideal application, the smart card could propel COB into the heady position as one of the leading assembly techniques for U. S. manufacturers. COB, basically a method of wire-bonding integrated-circuit chips directly to printed-circuit boards, has only one real competitor in smart cards, a closely related technique called bare tape-automated bonding, or TAB. Both enable card designers to squeeze smart-card circuitry and components inside a 40-mil-thick package, but COB backers maintain that their technique has the advantage of greater design flexibilty.

COB is already making inroads into solid-state memory packaging, telecommunications designs such as mobile cellular phones and pocket pagers, floppy-disk and Winchester-disk drives, and circuitry for miniaturized sensors. And it is being used increasingly in the production of both pin-grid arrays and leadless chip carriers that are based on small printed-circuit-board substrates with single chips wire-bonded on.

COB is able to do this because it is an inexpensive way to get all the advantages of a thick-film hybrid—such as dense component packaging and high performance [*Electronics*, May 26, 1986, p. 33]—by cutting out one of the hybrid's most costly components, its ceramic substrate. COB substitutes a pc board for a substrate, which can cost 40 times as much as the board. The tiny chip itself replaces packaged chips. Using the bare chip saves not only the cost of the package but 80% to 90% of the space the same chip in a packaged version would occupy.

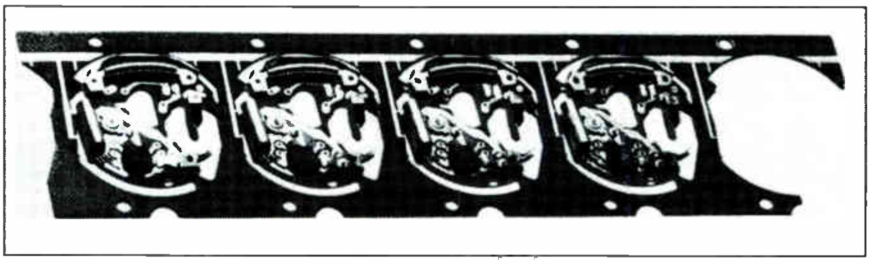
If COB is so good, why hasn't it caught on yet in the world's biggest electronics market? It did enjoy a brief boom when it was used in simple plug-in read-only-memory modules for video games and low-end personal computers, but it sank along with those markets. Yet it has caught on overseas. COB is now used extensively in Japan and Europe in consumer electronics—watches, cameras, calculators, audio and TV sets. But U. S. engineers have generally shunned COB, not only because they have been worried about the technical problems but also because of sheer inertia.

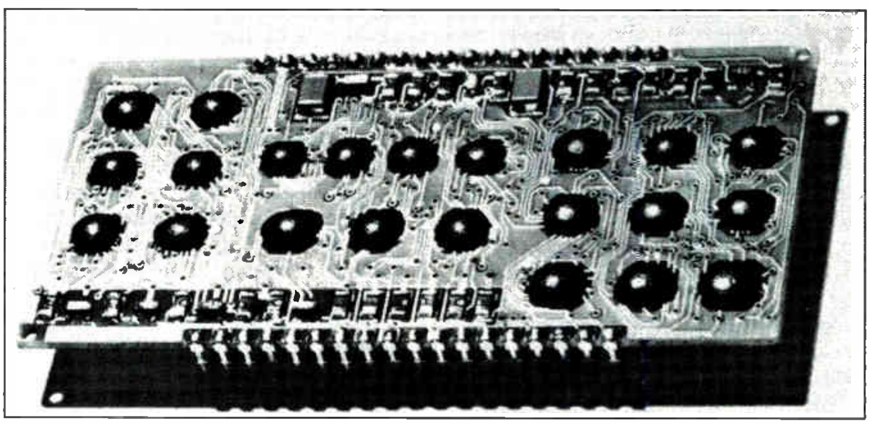
SOLDER IS KING. This inertia can be traced to the fact that the U. S. pc-board industry is based on soldered connections, and it is not about to switch overnight to wire bonding. For the same kind of reason, the switch to surface mounting and tape-automated bonding has been agonizingly slow in the U. S., even though both technologies flourish in Japan.

The technological barriers that have tended to stymie COB in the U. S. are getting rid of heat, providing sufficient protection to the chip, and getting good chip yields. Most American packaging engineers have centered their reservations on the heat-dissipating potential of the bare chips on a COB board, not to mention how well they are protected from the environment. Normally, these problems are taken care of to a certain extent in the package, whether it's a dual in-line, single in-line, chip carrier, or any other.

However, Alan Bertaux, president of Valtronic Inc. in Columbia, Md., one of the few U. S. companies exclusively devoted to COB, notes that his engineers have come up with epoxy-glass COB boards capable of dissipating 5 W. Packaged chips, depending on the package, can dissipate 0.25 to 1 W; bare chips with no special packaging can dissipate only 0.1 to 0.25 W.

Bertaux says that increased COB heat dissipation can be accomplished through the use of thicker copper cladding and wider pc conductors, metallizing the underside of a board, and even sandwiching an aluminum sheet between two thin glass-epoxy substrates. In that case, the overall package is no thicker





ALL ABOARD. Original chip-on-board—wire-bonding bare chips to pc boards—was used for wristwatches, top. More modern version has many more chips on a small board, bottom.

than a normal double-sided board, yet it provides excellent heat-transfer characteristics.

The environmental-protection issue is somewhat more complicated. One method that can be used to protect chips in the COB technique is to encapsulate them with a glob of epoxy or silicone. This method, also used in TAB, still has to prove itself as humidity-resistant and able to handle the possible mechanical stresses on the chip due to thermal expansions.

Valtronic is currently running tests based on MIL-STD-883, method 202, on encapsulated chips and says it will have results soon. In addition, the work being done by an Institute of Electrical and Electronics Engineers task force, which is seeking a silicone gel to protect chips in premolded plastic chip carriers, will also yield useful data on protecting bare chips bonded to pc boards. At the same time, within the IC industry itself there are many efforts under way to come up with even better passivation coatings for the surface of the chip than are currently in use, and this may be the eventual solution to a truly waterproof chip.

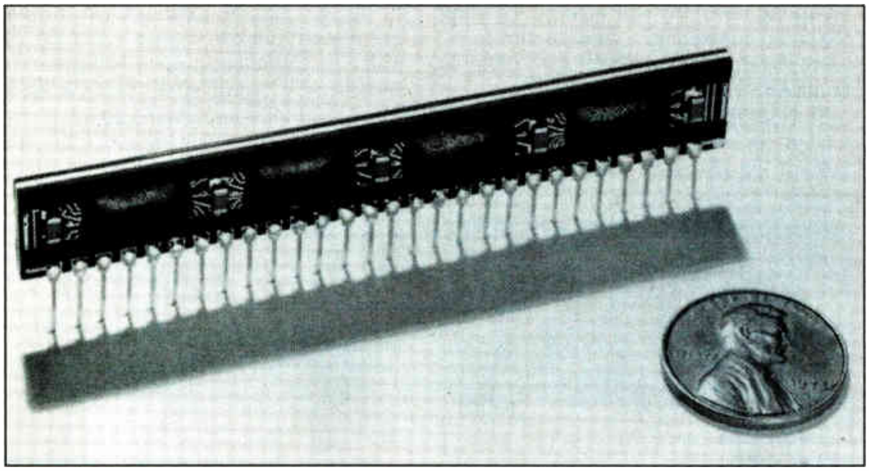
SOME OVERKILL. Such work could be overkill. True hermeticity even with non-COB techniques is possible only in expensive ceramic packages that are aimed at military applications. In most applications the chip actually needs only to be mechanically protected. For example, one of Valtronic's customers requested a module, for a pocket-pager, with fully conformal coating. A year later, the customer realized that this protection was really not needed and eliminated the requirement.

Finally, low chip yields worry some board assemblers. One of the acknowledged experts in surface-mounting technology, Phil Marcoux, manager of advanced technology of SCI Inc. of Santa Clara, Calif., says that his company, formerly known as AWI Inc., has occasionally mixed COB with a predominantly surface-mounted board when no packaged device was available, but he notes a potential deficiency in high-chip-count COB. Marcoux points out that the yield of complete COB assemblies suffers from the same dependency on individual chip yield as in the other bare-chip technology—thick-film hybrids.

It is an established fact that on a hybrid, as the number of chips goes up, overall circuit yield goes down, unless the individual chip yield is kept high. For instance, a chip yield of 0.8 in a 4-chip hybrid theoretically results in a hybrid yield of 0.4, although a chip yield of 0.95 will result in a hybrid yield of 0.8.

For smart cards, tape-automated bonding will rival COB

However, Valtronic's Bertaux notes that most COB circuits use only one to five chips, which doesn't require an excessively high chip yield for acceptable circuit yield. In addition, he says, most COB companies are paying for chip inspection at the chip vendor. Valtronic itself doesn't shun multichip boards. It has made many and, in fact, recently landed a production order for a nine-chip COB array that is to be used in a cellular phone.



COB SANDWICH. Substrates sandwich aluminum strip for better heat transfer.

Still, the flurry of COB activity so far accounts for only a small part of the total number of pc-board assembly techniques used in the U. S. COB still takes a back seat to surface mounting of small discrete components, or, in the great majority of cases, the tried-and-proven standard through-the-board technique.

So more than anything else, COB needs the smart card to hit the big time, and for that to happen, smart cards themselves have to do as well as many industry observers are expecting. Jerome Drexler, for example, the president of card maker Drexler Technology Inc., is particularly optimistic; he predicts that 160 million cards a year will be sold by 1991.

At least one U. S. company, MicroCard Technology Inc. of Dallas, is already using COB on a pilot line for smart cards being used in a MasterCard test. The card's circuitry consists of a single custom chip—a microprocessor with electrically erasable programmable read-only memory—wire-bonded to a thin epoxy-glass substrate that is sealed within the card.

Byron Claghorn, vice president of engineering of MicroCard, says, "Smart cards have the potential to be one of the largest semiconductor applications in the world. Most adults in the United States already have two to three cards, and these surely will be converted to smart cards eventually."

To win a major share of the smart-card market, though, COB must beat out the competition coming from the backers of TAB. Smart Card Systems Inc. of Cherry Hill, N. J., for one, is already making a two-chip smart card based on multilayer TAB. It may not be simply coincidence that Smart Card Systems is a subsidiary of IMI Inc. of Cherry Hill, N. J., a producer of TAB tapes and assembly equipment.

TAB-bonded chips are excised from their tape and bonded or soldered to a pc board. The technique is used in Japan for consumer applications, and in both Japan and Europe by computer makers for large multilayer ceramic-circuit-board hybrids. In the U. S., TAB is still used mainly as an assembly method for bonding LSI and VLSI chips into packages or leadframes.

SUPPORTERS. Both COB and TAB have their advocates. Courtney Miller, packaging strategy manager at Texas Instruments Inc.'s Semiconductor Group in Dallas, says that chips on tape are both testable and also can be burned-in on the tape. This ensures that only those chips known to be good are being put down on a substrate. Although the chips put down for COB may be tested at a probe station at extra cost, he says, they cannot be burned-in at either the chip or wafer level. In addition, says Miller, the "bumping" or buildup of the extra metallization of the I/O pads of a chip serves to increase its resistance to humidity.

However, MicroCard's Claghorn says his company considered using TAB for its cards housing 8-lead chips, but decided that the technique was more suitable for a high-count pinout application. COB turned out to be more cost-effective. COB is also simpler: TAB requires special bumped chips, special bonding equipment, and a new tape pattern for each new card design. □

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TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
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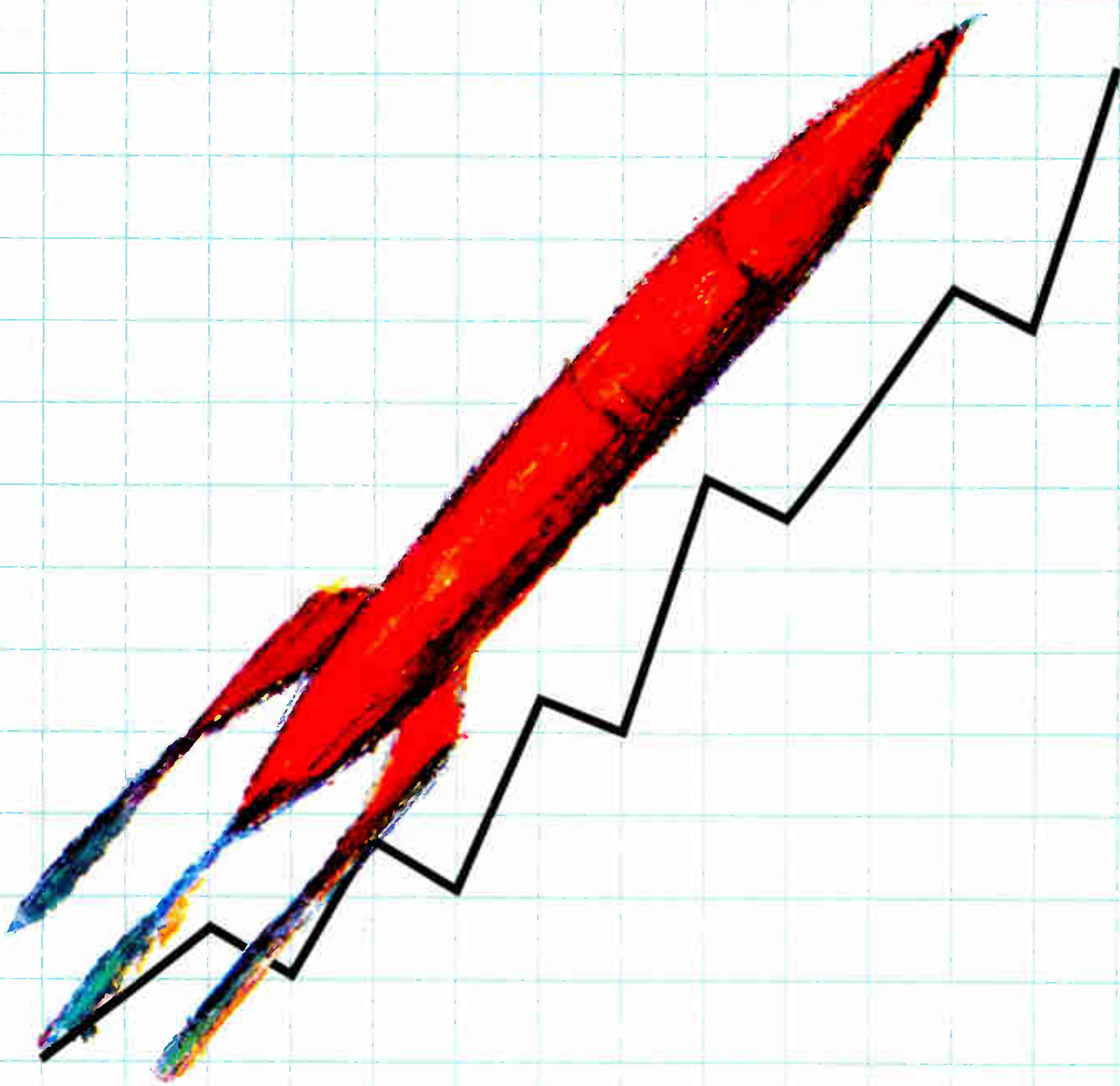
MILITARY ELECTRONICS OUTLOOK



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MILITARY ELECTRONICS OUTLOOK

SPECIAL ADVERTISING SECTION

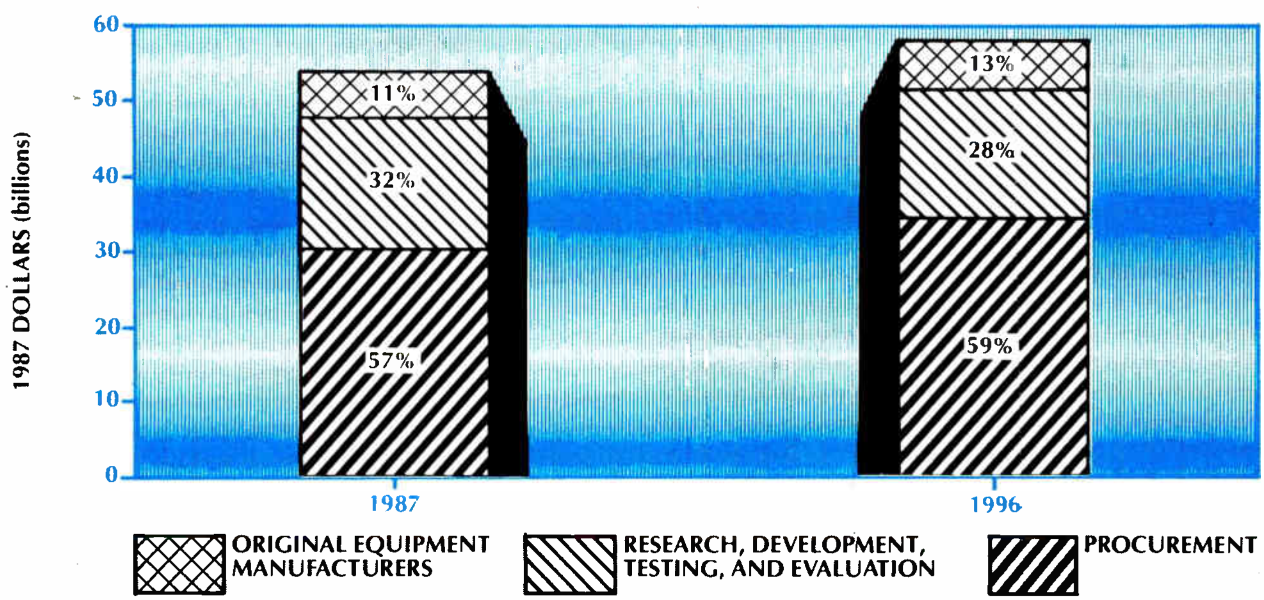
Defense-electronics spending to stay on flat trajectory for next few years

Defense-electronics companies may have a tough time finding new business during the next several years. The outlook for the industry is essentially flat until at least 1995, according to a forecast in this year's annual update from the Electronic Industries Association's Government Division. The only suppliers that can expect to continue to do well are those currently involved in major defense programs and smaller firms seeking second-source contracts.

To most industry watchers, many of whom expected the defense buildup of the early 1980s to start slowing, the EIA's projection is no surprise. It already has garnered a lot of support. For example, a study by the International Institute of Strategic Studies, which reports annually on world military trends, states, "The Reagan Administration's defense buildup is over." And a recent forecast of the industry's near-term prospects from Henderson Ventures, the Los Altos, Calif., market researcher, says that budget-balancing legislation inspired by Gramm-Rudman will be instrumental in forcing a sharp decrease in military-electronics spending next year.

According to the EIA, the Department of Defense's fiscal 1986 budget will contain $55.6 billion for procurement, research and development, and

DEFENSE ELECTRONICS: MODEST INCREASES OVERALL



Source: Electronic Industries Association maintenance of electronics. That's barely more than the $55.5 billion allotted in 1985. It then will drop to a low of $52.6 billion in 1989 before rebounding, reaching $58 billion in 1996.

Meanwhile, the total defense budget authority, which represents the enabling legislation that authorizes the DOD to spend money, will drop steadily—by 2.8% in 1987 and 0.5% in 1990. Electronic content should drop 3.7% in 1987, 0.9% the following year, and 1.1% in 1989, but it should gain a modest 0.1% in 1990.

The breakdown for defense electronics in fiscal 1987 goes like this, says the EIA: $33.3 billion for procurement, $16.1 billion for R&D, and $6.1 billion for operations and maintenance, for a total of $55.5 billion. Up to and including fiscal 1996, the EIA says that spending on R&D and operations and maintenance will remain fairly constant. Procurement, however, will be unsteady, dropping to $30.2 billion in fiscal year 1987 and to $29.6 billion in 1989 when it begins to rebound, climbing to $34.3 billion in 1996.

Major procurements identified

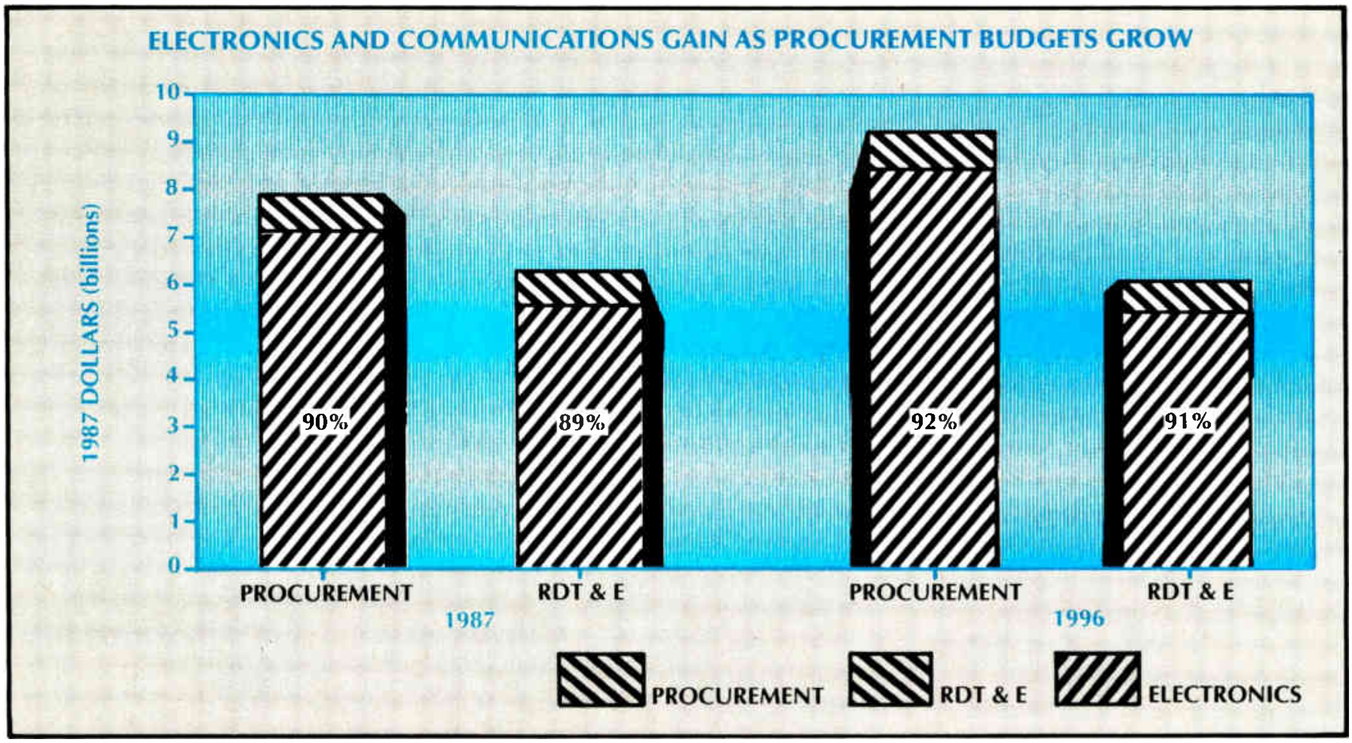
In other major procurement areas, the EIA forecasts the following for the next 10 years:

Aircraft—During the next five years, budgets should decline; gradual increases will start in 1992. The period is characterized by programs that take longer to complete than expected initially, some reduction of current programs, and modernization of existing systems, in lieu of new procurements. The electronics content for aircraft, however, will gain, from more than $8 billion in 1987 to about $10 billion in 1996.

Missiles—Budgets at first should decline sharply as such current strategic programs as M-X and Trident reach completion. Tactical missile production programs should retain strong support, however, and these budgets will decline more slowly through 1996. Although electronic content will gain slightly, the impact of a big drop in spending on missiles will cut electronics spending from just over $6 billion in 1987 to about $5.5 billion in 1996.

Space—The increase in budgets is based on procurement of communication and reconnaissance satellites, military acquisition of expendable launch vehicles, and the Military Strategic Tactical & Relay program. No deployment of Strategic Defense Initiative hardware is expected. The projected electronic content in DOD space programs is already high—65%, or approximately $2.7 billion in 1987. That should climb to 70% of defense space programs, or about $4.7 billion, by 1996.

Ships—The 600-ship Navy either is completed or under contract. Modernization of this equipment and replacement of the fleet's older vessels should be the major expense during



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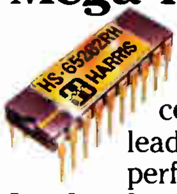

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this period. Electronic content remains stable through 1996 at about $3.2 billion annually.

Ordnance and weapons—Budgets should remain level. Expenditures will cover the procurement of existing equipment programs as well as the building and replenishing of war reserves. Emphasis on the acquisition of smart weapons should continue. Electronic content will inch up from $1.2 billion in 1987 to $1.3 billion in 1996.

Vehicles—The flat outlook is based on expectations that the DOD will emphasize maintaining current program production levels. Although electronics spending should increase about five percentage points by 1996, total annual spending will remain fairly stable at $0.8 billion.

Requirements seen growing

Despite the sector's less than explosive gains, a recently published report from Prudential-Bache Securities, New York, argues that the need for military electronics is growing. Byron K. Callan, Prudential-Bache's defense-electronics analyst and author of the report, sees promising markets in command, control, and communications programs (particularly strategic ones), intelligence gathering, and upgrades to electronic-warfare systems.

He states that companies involved in upgrading strategic forces, naval electronic warfare, radar, and communications should see higher growth than other defense-electronics segments. He also believes that small to midsize firms will continue to hold their own in a market dominated by large electronics conglomerates. For one thing, second sourcing has greatly eased market entry, particularly for smaller firms. At the same time, Congress's push for increased competition among defense contractors has forced them to watch program performance more closely.

Callan also expects more takeovers within the industry, similar to the acquisition by Lockheed Corp. of Sanders Associates, and possibly at a more rapid pace.

In November, for example, Honeywell Inc., the Minneapolis computer and controls company, announced that it had agreed to purchase the Sperry aerospace group of Unisys Corp., Detroit, for $1.03 billion in cash. The Sperry unit, best known for flight controls and instrumentation, will complement Honeywell's production of guidance and navigational equipment.

Also last month, Goodyear Tire & Rubber Co., Akron, Ohio, said it already was talking with several companies interested in buying its aerospace subsidiary only a week after putting it up for sale.

Among other merger activity, Boeing Co., Seattle, recently tried to expand its holdings in defense electronics with the acquisition of Hughes Aircraft Co., Newport Beach, Calif., but lost out to General Motors Corp. Rockwell International Corp., Newport Beach, which Honeywell beat in the Sperry sale, reportedly continues to search for a major acquisition.

Military-industry analysts cite a variety of reasons for all these mergers and acquisitions, including the stable cash flows of established defense contractors and expected benefits from the new tax laws. In addition, analysts report that the stock of many defense suppliers is undervalued, a result of the slim defense-budget increases and new Pentagon policies that call for contractors to assume more risk and upfront investment.

Furthermore, merging with the right company could make it easier to win the fewer large contracts now available. For example, the merger of General Electric Co., the Navy's fourth largest contractor, with seventh-ranked RCA Corp. should yield a tougher competitor for Navy electronics contracts. Since the merger, GE has created two divisions in its defense and aerospace operations by combining several of its existing businesses with RCA units.

Another reason for the spate of merger activity is expected advancements in design concepts and technology, says Prudential-Bache's Callan. Citing a recent Air Force report that sensors will be embedded in the skins of aircraft to make the planes more difficult to detect, Callan says that electronics will gain in importance and that in the future aircraft will be designed around their avionics rather than the other way around.

Star Wars tops R&D budgets

Nowhere is leading-edge technology sought more avidly than in SDI. As far as R&D is concerned, SDI will dominate the DOD's budget at least through the mid-1990s. The result: strong growth in R&D spending by the military for space programs over the EIA forecast's 10-year period.

SDI's budget should grow from $3.1 billion in 1987 to $5.1 billion in 1991. Though it will slow after that, it should approach $6 billion a year by 1996, the EIA says, with 60% to 70% going for electronics.

But contractors could have a tough time figuring out exactly where the DOD wants to spend its money, mainly because some parts of SDI's allocation are buried in other programs. For instance, the EIA estimates that two thirds of SDI's budget is built into space program R&D, and one third of SDI's R&D budget is included in Pentagon missile programs. These programs cover such areas as radiation-hardened, warning-equipped, anti-jam platforms designed to survive a nuclear exchange.

In fact, the equipment's ability to survive a nuclear attack is getting more emphasis. Program managers are looking closely at laser shielding, neutral-particle-beam and microwave hardening, and kinetic shielding, as well as at such active schemes as warning sensors and jammers. In a separate report on the military laser

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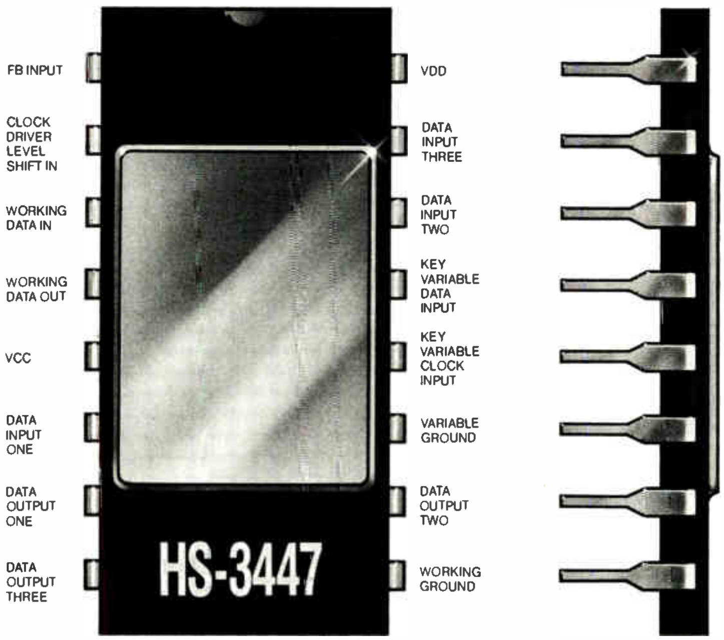

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FOR YOUR INFORMATION, OUR NAME IS HARRIS market, Frost & Sullivan states that SDI accounts for more than $3.2 billion in laser funding for fiscal 1986, a share it will maintain at least through 1991. Developing concepts in directed-energy weapons now account for nearly 83% of the dollars in the space-armament sector, says Frost & Sullivan.

The New York market researcher points out that the ability to withstand nuclear bombardment is critical to satellite systems as well. In a recent study, it says, "If there is one common theme that underlies most defense agency efforts on military satellite communications systems, it is the endeavor to make them more survivable and capable of functioning in an environment of protracted nuclear attack." The concern over survivability is a byproduct of the widening role that satellites play. The Milstar program alone uses more than one third of all military satellite dollars and could rise to half the market by fiscal 1991. Part of that effort is bound up in the

JUMP EXPECTED IN THE MILITARY SECURITY MARKET

Military security is gaining as a market opportunity for companies in the industry.

According to Honeywell Information Systems, which conducted a study of the market, the number of secure computer systems submitted for evaluation to the National Security Agency's National Computer Security Center (NCSC), Fort Meade, Md., will more than double in the next year.

NCSC requirements calling for the Defense Department to purchase only secure computer systems beginning in 1987 are expected to be a major factor in the market's expansion. Moreover, the NCSC, which has central responsibility for computer security within the federal government, will require all federal government agencies to purchase secure computer systems beginning in 1988.

The actions are part of a series of directives affecting the Pentagon and defense contractors. Last month, for example, the Reagan administration issued new guidelines restricting the release of a broad range of government data that is unclassified but nonetheless considered sensitive. Federal agencies are not getting additional authority to restrict release, however.

The directive is the result of a federal study aimed at limiting access to unclassified information through public and government data bases. Initially focused on two government agencies—the Defense Technical Information Center and the National Technical Information Service—the study has been expanded to include private electronic data banks that hold potentially sensitive information. In fact, federal officials already have visited commercial on-line data-base concerns to determine whether their data (technical, economic, and so forth) ought to be secured.

More recently, the administration has ordered all federal agencies to identify sensitive data held in government computers so it can be protected with strict computer-security methods. Although the Pentagon always has made information security a high priority, the DOD is expected to reevaluate its own data bases under this new directive.

Diane Fountaine, director for information systems in the Office of the Assistant Secretary of Defense, recently told an audience at an industry meeting: "The question is not will there be restrictions or controls on the use of commercially available on-line data bases. The question is how will such restrictions or controls be applied." Her office has been formulating recommendations on restricting access to commercial data bases. These recommendations could be announced at any time.

Although several solutions have been discussed, the general impact of this apparent change in national policy is likely to generate an even larger market for both information systems software and hardware.

Another growing sector in the military security market is that for Tempest-qualified computer systems. This equipment eliminates the unauthorized detection of electromagnetic emissions.

Some vendors in the field estimate the current Tempest market at $0.5 billion. International Data Corp., a market researcher in Framingham, Mass., projects the market for this type of equipment at 500,000 unit sales annually by 1990.

So far, most developers of Tempest-approved equipment sell directly to the military. However, some specialists in the field are increasingly aligning themselves with major systems manufacturers, both to market their products to the military services as well as to develop products jointly.

The number of products, mostly computer systems and computer peripherals, developed under the DOD's Tempest security standard guidelines has grown to 200.

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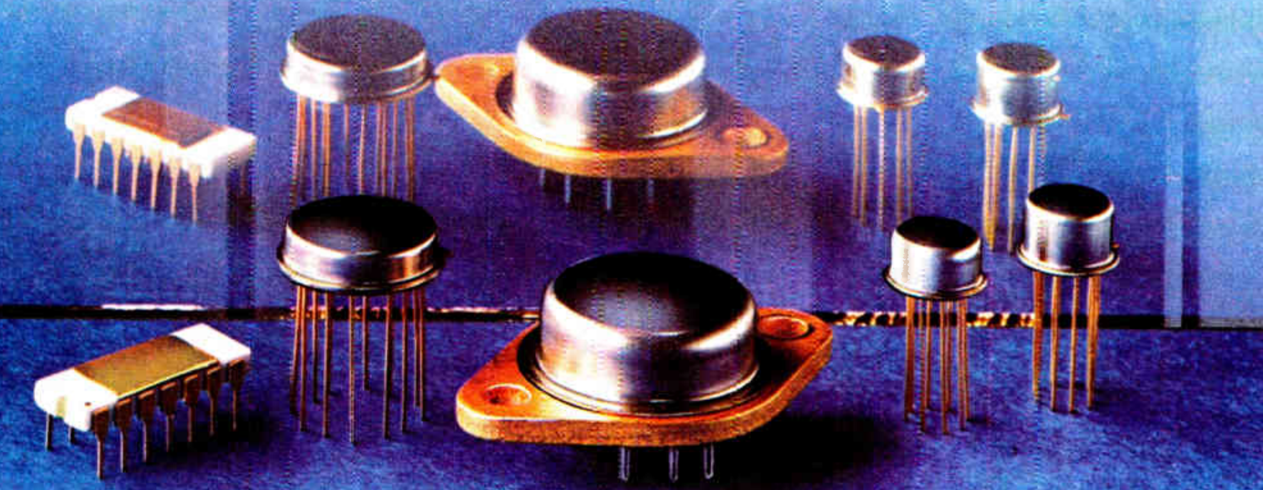

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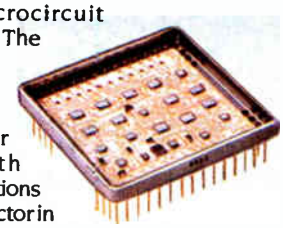
Advanced Air Force Communications System uses CTS Military Hybrid

The prime contractor for the Air Force SEEK TALK anti-jam voice communication system selected a CTS Hi-Rel unit as a primary microcircuit component. The need for high reliability in this system linking fighter aircraft with command stations was a major factor in the selection of CTS.



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DOD's gallium arsenide program. GaAs circuits will play a vital role in transmitter and receiver modules in new phased-array radar systems, satellites, and avionic packages, not only in SDI and Milstar but also in other programs. More than a dozen contractors have submitted proposals to run a major new development program that could rapidly accelerate the technology.

Called Mimic, for microwave and millimeter-wave monolithic integrated circuits, the program's aim is to produce a reliable, affordable supply of complex GaAs chips for next-generation communications and weapons sensor hardware. Among the teams bidding on Mimic are GM-Hughes Electronics and GE, Texas Instruments and Raytheon, Westinghouse Electric and Rockwell International, and TRW and Honeywell. Because of expected budget cuts, other elements of SDI won't fare as well near term. For example, a surveillance tracking system experiment and a long-wave infrared radar probe will likely be delayed, according to the EIA. A space-based radar project has been dropped and space-based experiments will be reduced.

Darpa changes seen

Budget cuts also have hit the Defense Advanced Research Projects Agency, established to advance the military's knowhow in information processing and expert systems. In some Darpa projects, funding is roughly 25% lower than requested. Darpa's budget came to approximately $104 million for fiscal 1986.

Darpa continues to award contracts, however. One, for $10.7 million, recently went to Encore Computer Corp., Marlborough, Mass., for a prototype system that can execute 1 billion instructions per second. The Naval Warfare Systems Command awarded the three-year Darpa contract to produce the system. In addition, AT&T Bell Laboratories last month picked up a Darpa contract valued at $7.7 million to build a prototype computer for speech and image recognition.

Meanwhile, Darpa continues work on three of its current major programs: the development of an autonomous land vehicle, a battle-management system, and a system for feeding critical information to pilots in combat.

The agency reported that an autonomous land vehicle, or smart truck, lived up to most of its design goals during a private demonstration in October. A public demonstration is scheduled for 1987. Martin Marietta Corp., Bethesda, Md., is the program's prime contractor, although other companies, as well as the University of Maryland and Carnegie-Mellon University, are involved.

The battle-management program's goal is to develop a threat-warning system for the Navy. A prototype system is being developed for the aircraft carrier USS Carl Vinson; the Pacific Fleet Command Center is managing the work. Extending the project, Darpa added an air-land battle management system for the Army in 1985. The Army's Ballistic Research Laboratory at the Los Alamos National Laboratory in New Mexico is managing the program.

The aim of the combat-pilot project, referred to as the pilot's associate, is a system to channel information from the plane's instruments and sensors through an expert system that prioritizes it and feeds the pilot only the information required at the moment. Two teams—one led by Lockheed, the other by McDonnell Douglas Corp., St. Louis, Mo.—are working on the program's first phase under contracts that were awarded last February.

Darpa's top management is scheduled to meet this month to review and update its goals and programs.

The NATO co-op

Plenty of opportunities also exist outside the Pentagon. The North Atlantic Treaty Alliance, always a major market for military-electronics vendors, has suddenly become an even bigger one. As a result of recent U. S. legislation intended to encourage domestic and European defense contractors to jointly build weapons for their respective armed services, NATO has earmarked a total of $345 million in military funds this year and next to finance the U. S.'s share of cooperative research into new weaponry.

NATO has proposed seven projects:

- A 155-mm guided artillery shell that tracks its target.
- A family of bombs and missiles that are fired from planes and home in on targets up to 70 miles away.
- An airborne radar system that spots

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It took Gould computers to train two generations on the same simulators.

Eight hard-working flight simulators that trained a whole generation of C-141 pilots had become obsolete. The Air Force studied the feasibility of refurbishing the 20-year-old simulators with the technology of the 1980's.

Burtek was selected to refurbish. And Gould computers were selected because first generation computers from the same company had successfully driven these simulators for 20 years.

Results? A new generation of pilots, copilots and flight engineers now receive greatly expanded training. They can practice the full range of C-141B flight capabilities in modern state-of-the-art simulators. Over 900 types of aircraft malfunctions can be simulated. Plus, these are the first DoD simulators to have computer automated performance certification.

The project was also cost effective. "We have saved the taxpayers several million dollars without skimping on performance", reports Burtek.

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enemy targets and directs NATO forces to attack them.

- A multifunctional system for information distribution, whose task will be to move data between headquarters and airfields.
- A NATO friend-or-foe identification system for aircraft.
- A data-distribution system with global range and low frequencies.
- A computer language for use by NATO weapons and command and control systems.

NATO commanders are expected to decide which programs will get the go-ahead in February. ■

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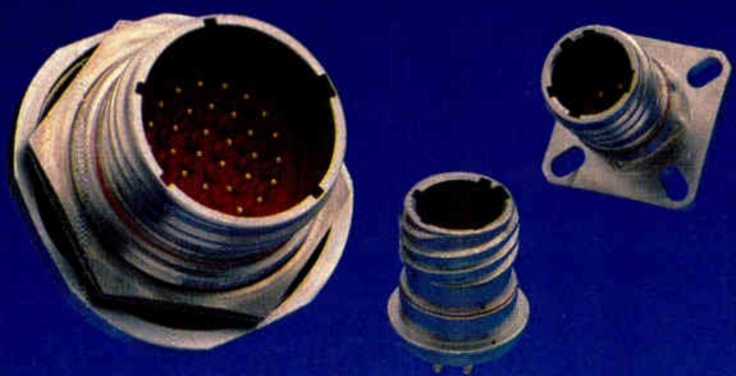

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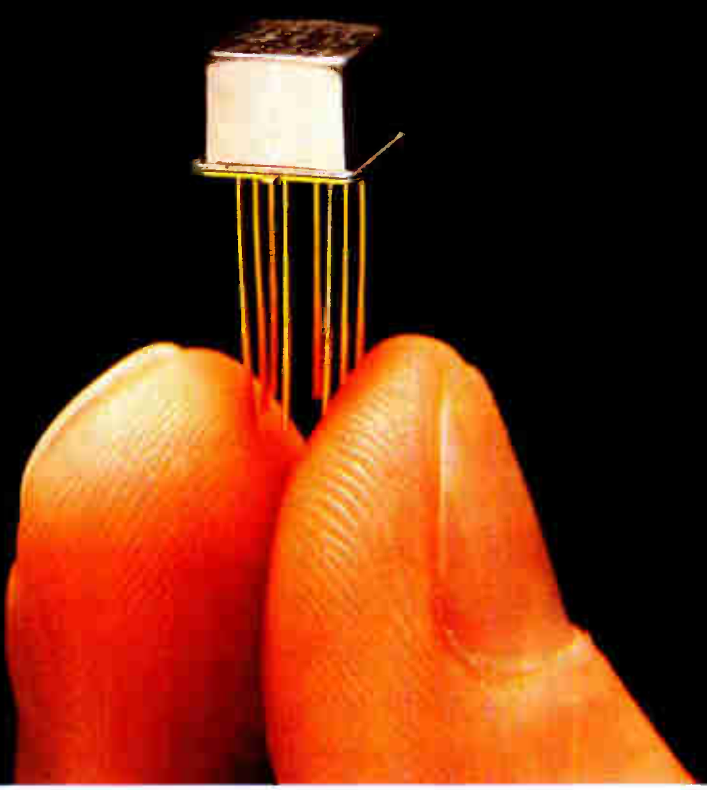

Our Centigrid relay is the vanguard of a new EMR generation. After all, it is the natural outgrowth of all those years of proven Teledyne TO-5 technology.

It is rugged. The uniframe-housed motor assembly is stabilized by the header at four points, making it very tolerant of mishandling during warehousing and assembly.

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2. Does your distributor offer immediate access to a broad range of high reliability products with fully certified, separate military warehousing capabilities?
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5. Can your distributor give a rapid response to your military questions?
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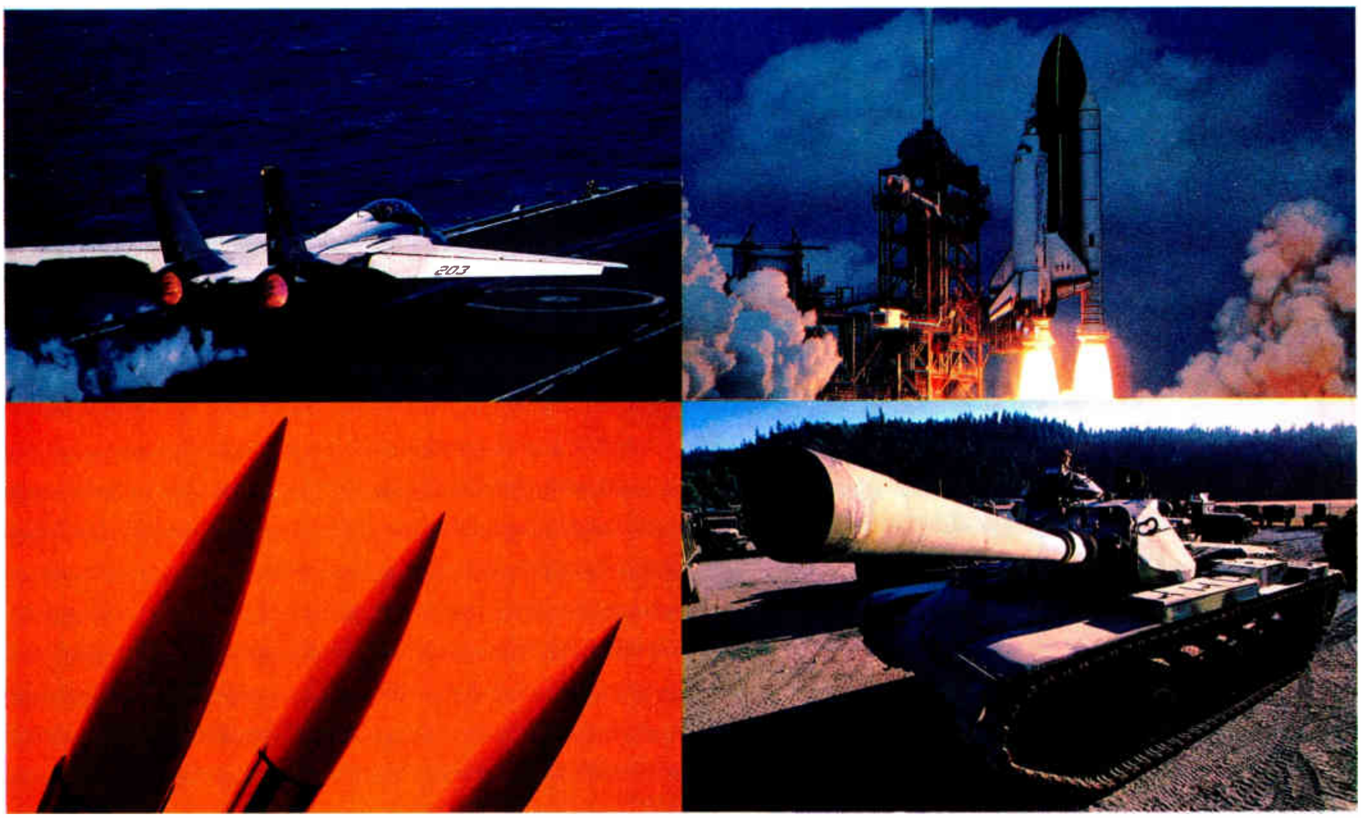
THE MILITARY PROFESSIONALS



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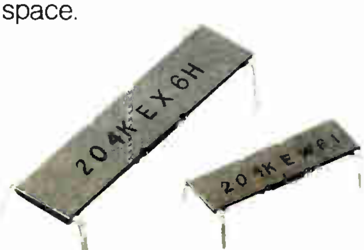

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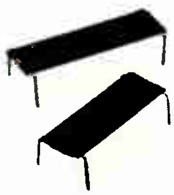
Improve existing board performance



MICRO/Q capacitors can be retrofitted to solve noise problems on existing boards. Because MICRO/Q caps share mounting holes with existing IC pins, no board redesign is required. Effective decoupling becomes a matter of adding one insertion step.

Circle 177 on reader service card

Simplify board layout and get a choice

MICRO/Q ceramic decoupling capacitors share board mounting holes with IC pins. You don't have to waste space on additional holes, as you do for standard caps. Simplifying board design opens up two very attractive options. Add more active devices with increased packaging density in the same space, or design the same package on a smaller board. Either way, you win with MICRO/Q.

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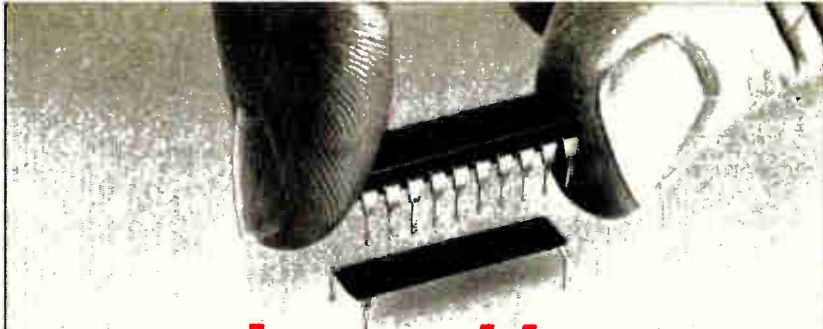

noise problems... space problems...

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Rogers MICRO/Q® decoupling capacitors reduce voltage noise spikes in IC's, often by as much as a factor of ten. And since they're easily mounted *underneath* the IC, MICRO/Q capacitors conserve valuable board real estate, too. A range of configurations makes MICRO/Q flat capacitors especially effective at reducing noise on:

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- Microprocessors
- Bus drivers/buffers
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- Telecommunications
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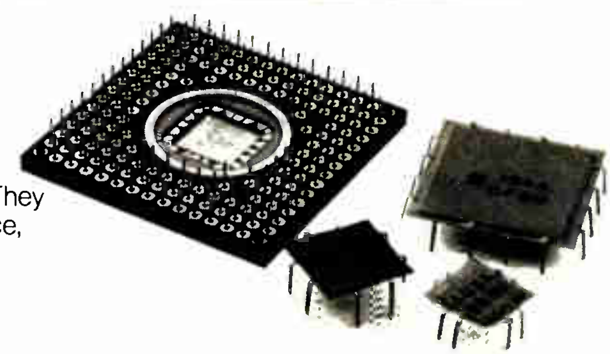
Design noise out of PGA and LCC packages



PGA MICRO/Q capacitors provide effective solutions to noise problems with VLSI PGA packages and LCC sockets. Design effective decoupling on complex multi-layer board layouts by fitting PGA MICRO/Q capacitors under PGA or LCC sockets. They occupy no additional board space and provide the low-inductance, high-frequency decoupling required by today's VLSI packages. Available in a range of pinout configurations.

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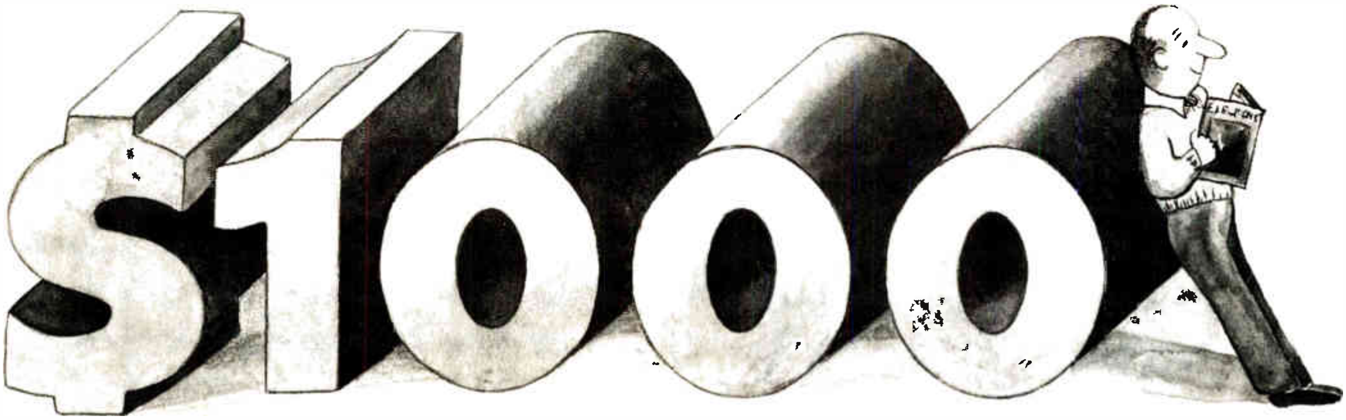

Watch for more details and complete contest rules in the January 8, 1987 issue.

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Electronics

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The new ADC600 gives Nicolet's 4094 DSO System 12-bit resolution with 8-bit speed

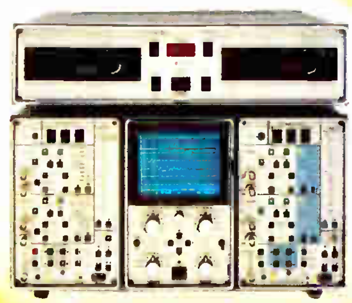
When Nicolet wanted both high resolution and ultra-high speed for its new DSO digitizer module, they brought their specs to Burr-Brown, the leader in high performance analog-to-digital conversion technology. They left with a handshake commitment to solve their problem. They got the ADC600 12-bit, 10MHz sampling A/D converter.

"... more than we asked for."

"We subjected the Burr-Brown ADC600 to a series of tests including noise, distortion, linearity (differential and integral), and bandwidth at frequencies from DC to above 10MHz. The results of these tests, plus the straightforward interface to our system, convinced us to select the ADC600 for our application. They gave us more than we asked for."

Jim Hyatt
Product Design Manager
Nicolet Test Instruments Division

ADC600 is the first high resolution, ultra-high-speed sampling converter to combine small size, low power dissipation, and straightforward interfacing in a reliable, low cost design. It's complete with sample/hold, encoders, reference DAC, and timing circuits on a space-saving, 17-square-inch printed-circuit card. And it's easy to use, requiring only external power supplies and CONVERT command for operation.



Key ADC600 Specifications

Resolution	12 bits
Sampling rate	10MHz min
Linearity error (200Hz)	±1.25LSB max
Harmonic distortion (F_{IN} = 1MHz to 5MHz)	65dB
Input range	±1.25V
Signal-to-Noise Ratio	70dB
Power dissipation	8.5W
No missing codes	0 to +70°C

With ADC600, Burr-Brown continues a thirty-year tradition of solving customer problems through innovative designs, high quality manufacturing, and dedicated customer service and assistance.

"Customer response has been excellent."

"The ADC600 provides state-of-the-art high-resolution digitizer performance in our already powerful 4094 digital scope. Many applications require 12-bit precision but also 8-bit speed; the Burr-Brown modules do both. Customer response has been excellent."

Dale Baldwin
Marketing Manager
Nicolet Test Instruments Division

If you have a data conversion problem, we invite you to contact Burr-Brown. You may be only a handshake away from the solution.

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768 X 512/480		✓	✓	✓	✓
640 X 512/480		✓	✓	✓	✓
512 X 512/480		✓	✓	✓	✓

Optional 100% CGA emulation available

Each family member utilizes the latest VLSI ACRTC Graphic Chip (Hitachi HD-63484), 256K Video RAMs, and high speed Video DACs, allowing a performance spec that is 5 to 10 times faster than NEC 7220 based controllers and 2 to 3 times faster than Hitachi HD-63484 based designs not using Video RAM technology. Most boards available in both interlaced and non-interlaced format.

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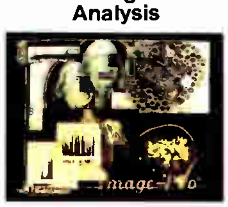
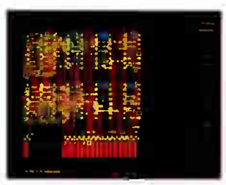


IMAGEPRO 1000

Electronic CAD



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NEW PRODUCTS

HP CLAIMS ITS IC TESTER RUNS FASTER THAN ANY OTHER

IT OPERATES AT 128 MHz TO TEST MIXED-SIGNAL CHIPS WITH 182 PINS

Hewlett-Packard Co. has started shipping a mixed-signal integrated-circuit tester that it calls the fastest tester of any type now on the market. The system attains speeds of up to 128 MHz for testing analog-digital devices with as many as 182 pins, surpassing even high-speed digital very-large-scale-integration testers that operate at 40 MHz but can be multiplexed to attain a 80-MHz test rate.

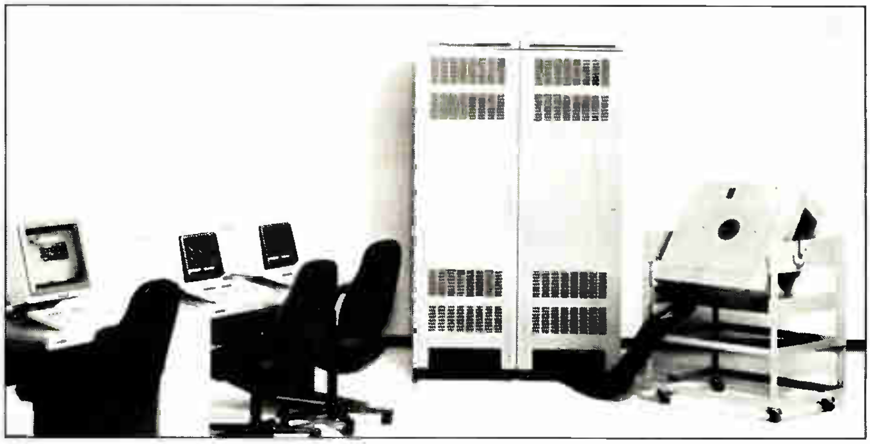
Its faster performance over other mixed-signal IC test systems is even more impressive, since they offer maximum frequencies of 25 MHz. They also contained a maximum of 96 pins—one for each test channel.

In addition to enhanced speed and capacity, the HP9480 runs with low signal distortion—a total harmonic distortion of –60 dB compared with an industry performance standard of –50 dB. It offers a 50-Ω test environment through the device under test. Previous test systems could guarantee such an environment only to the test head. The 9480 carries a base price of $650,000.

PRESSING NEED. The need for such a high-speed tester has become more pressing as applications for digital-to-analog converters and analog-to-digital converters that operate between 20 MHz and 100 MHz have increased. DACs used at the output of graphics-controller boards for driving high-resolution color monitors, for example, operate up to 100 MHz. This sector of the IC market will grow, according to VLSI Research Inc. of San Jose, Calif. In 1986, 1.2 billion DACs and 905 million ADC chips will be shipped, and the markets are expected to grow at a rate of 24% and 27%, respectively, through 1988.

To achieve its high speeds, the tester uses an eight-plane matrix of high-speed emitter-coupled-logic random-access memories. Each plane contains 2 K of emitter-coupled-logic RAM that can be from 16 bits to 128 bits wide.

Conventional test systems have one plane of memory. Digital stimulus patterns are applied by sequentially unloading one address after another. As a result, the tester is limited to the access speed of the ECL-RAM read cycle—



VALUE. HP's tester starts at $650,000 but costs $1.3 million fully equipped.

about 40 ns—hence the 40-MHz test rate. By contrast, HP's tester takes digital test patterns from plane to plane, allowing the instrument to overlap the ECL-RAM chip's read-cycle overhead. This overcomes the 40-MHz limitation to achieve the 128-MHz test rate.

In gathering response data, the test system strobes each word received from the device under test into the eight memory planes in the same way that stimulus is moved out of memory. It can generate and receive stimulus and response, respectively, every 8 ns.

To provide analog stimulus at a 128-MHz analog test rate while maintaining low distortion, HP has applied a technique called Fractional N Divider developed for its microwave signal sources. The 9480's analog stimulus source uses a 200-MHz crystal oscillator as its signal, then uses the Fractional N Divider to achieve a lower frequency. A benefit of the technique is its very low total harmonic distortion. At certain frequencies—1, 2, 5, 10, 20, 50, and 100 MHz—the divider produces an almost pure sine wave with a total harmonic distortion of –80 dB. At the 128-MHz frequency, total harmonic distortion is –60 dB.

For gathering analog responses, HP uses a technique developed for the company's 1-GHz oscilloscope, which uses a 40-MHz sampling rate to digitize its input waveform with 6 bits of resolution. Instead of using the 40-MHz sample rate, the test system samples at 1-MHz rate and thus achieves a 12-bit resolution required to test high-resolution DACs currently being produced. The tester can use a lower sampling rate because—unlike a scope—it precisely controls the stimulus source.

A fully equipped system with all 128 channels installed costs about $1.3 million. The system is ready three months after ordering, and HP has begun shipments. *–Jonah McLeod*

Hewlett-Packard Co., 3000 Hanover St., Palo Alto, Calif. 94304.
Phone (415) 857-1501 [Circle 380]

UNIVERSAL COUNTER HAS BUILT-IN CRT

A microprocessor-based instrument from Enertec Instruments is the first universal counter with a built-in CRT display, the company claims.

Model 2721 measures frequencies up to 200 MHz with voltage sensitivity of 15 mV. An optional channel extends the instrument's frequency range to 1.25 GHz. It attains high sensitivity and noise immunity by utilizing two precisely set trigger levels that can be set at 30% of the signal amplitude. This also allows resolutions of 500 ps when the instrument operates in single-shot mode.

The counter comes with 17 measurement functions, including signal fre-

quency, period, phase and duty factor, rise and fall times, and peak-to-peak signal values. It includes a feature for totaling measurements.

Mathematical processes such as scaling, averaging, smoothing, and limiting may be applied to the result. In addition to its analog output, the 2721 records and displays on its CRT screen how the measured parameter changes with time. Three types of time bases are available, depending on desired stability. The instrument may be programmed to create hard copies of screen displays.

Available now with an IEEE-488 interface, the 2721 base unit costs $4,600.

Enertec Instruments Export Department, 5 rue Daguerre, 42030, St. Etienne Cedex 2, France.
Phone 77 25 22 64 [Circle 385]

MULTILAYER BOARDS GET CAD SOFTWARE

Visionics Corp.'s EE Designer II computer-aided-design software targets pc-board applications where surface-mounting design and multilayer capabilities are required. The software retains the functions of the company's products for schematic design, circuit simulation and board layout, but adds a graphics kernel that provides flexibility in creating components and pad shapes.

Designers can use EE Designer II to create ground planes on both sides of a pc board and to specify trace widths, pad sizes, and several other options, including 5- and 12-mil grid spacings, and the ability to save design macros. The software also facilitates the production of fabrication drawings with related text through its automatic board-dimensioning and text-editor features.

Available now, the package costs $1,875. A companion product, the AutoRouter II package for routing, costs $1,475. Together, they cost $2,975.

Visionics Corp., 1284 Geneva Dr., Sunnyvale, Calif. 94089.
Phone (800) 225-5669 [Circle 388]

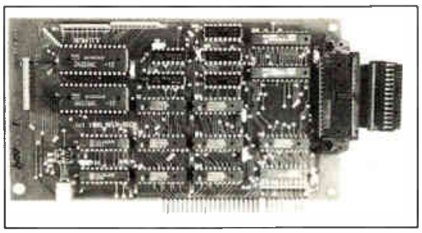
IN-CIRCUIT EMULATOR COSTS LESS THAN $600

Beck-Tech's Romice in-circuit emulator for testing and developing embedded microprocessing systems in personal computers uses a single plug-in slot and costs $595.

Romice emulates ROM or EPROM on IBM Personal Computer ATs, XTs, or compatibles. Processor-independent, it operates in 4- to 32-bit systems. It clocks in at 64-K bytes in 15 s, has a standard access time of 200 ns, and offers an optional speed upgrade to meet 150- or 100-ns access times.

The emulation package includes a 24-in. cable and connector for 28-pin memory-device sockets.

Up to two of the cards can be plugged into a PC to provide 128 K of



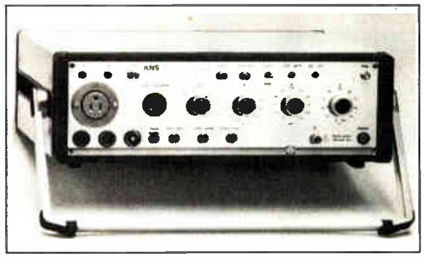
emulation memory. Disk-operating-system software is included to support a screen editor of the memory contents as well as other commands. Romice's flexibility permits the PC to perform other functions while the emulator is in emulation mode.

Beck-Tech, 41 Tunnel Road, Berkeley, Calif. 94705.
Phone (415) 548-4054 [Circle 386]

INTERFERENCE TESTER OPERATES IN 3 MODES

A bench instrument from MWB Messwandler-BAU AG of West Germany lets IC designers test for electrostatic discharge and power-line-interference susceptibility in three different simulation modes.

Model KNS is specifically intended for verifying product immunity to electrostatic discharge from people and to the power-line disturbances that can affect



high-density ICs in production areas.

Its electrostatic-discharge component is based on a human reactive-capacitance model of 150 Ω and 150 pF. Simulation voltage is variable to 6 kV at a repetition frequency of 1 Hz. An optional high-voltage test gun can be used to direct the discharge to the point of contact.

The three interference modes vary with impulse voltage, wave shape,

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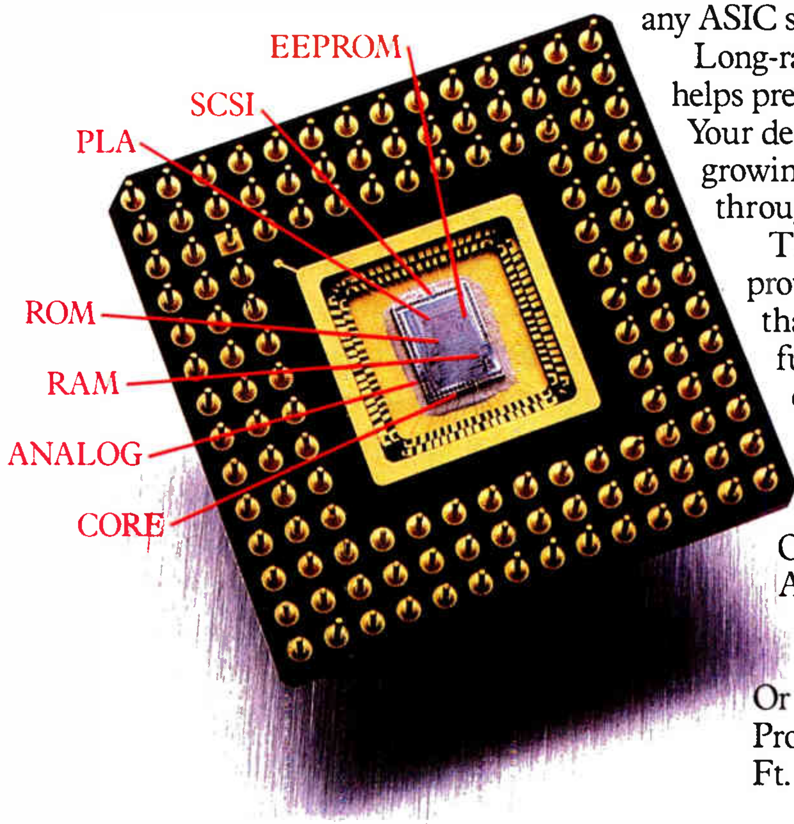

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Circle 131 on reader service card

source impedance, and polarity. The line-interference coupling network accommodates products with power ratings as high as 220 V and 10 A.

The instrument has been modified for use in the U. S. It will be distributed by Slaughter Corp. in the first quarter of 1987 at a base price of $4,800.

Slaughter Corp., P.O. Box 1805, Ardmore, Okla. 73402.
Phone (405) 223-4773 [Circle 387]

PORTABLE HAS SCOPE, AVERAGER, METER

A microprocessor-controlled; multipurpose measuring instrument from the Yugoslavian company Iskra Electronics Corp. combines the functions of a digital oscilloscope, an averager, and a digital multimeter in a single, portable instrument.

At a $1,500 base price, the Iskrascope LCD can be used for measuring and recording as well as for inspection and

testing of components and equipment. The instrument features a membrane keyboard with voice indication of manipulation commands and a tiltable LCD data display. The eight-pound unit folds into its own carrying case and can operate on rechargeable NiCd batteries, making it ideal for field work. It is available now from the company's U. S. distributor.

Iskra Electronics Corp., 222 Sherwood Ave., Farmingdale, N. Y., 11735.
Phone (800) 862-2101 [Circle 390].

WAVEFORM DIGITIZER HAS 10-BIT ACCURACY

Sequence Inc.'s Model 3000 waveform digitizer attains 10-bit amplitude resolution at a 1-ns sample interval and offers a 1,024-word acquisition memory with pre- and post-triggering capability.

The instrument also features a single-shot input bandwidth of dc to 350 MHz and a multifunction software package designed to allow up to eight Model 3000s to use a single personal computer for display and signal analysis.

Available now, the Model 3000, including the multifunction software package, costs $28,500. Delivery is within 60 days of order.

Sequence Inc., 1650 Zanker Rd., San Jose, Calif. 95112.
Phone (408) 436-6065 [Circle 389]

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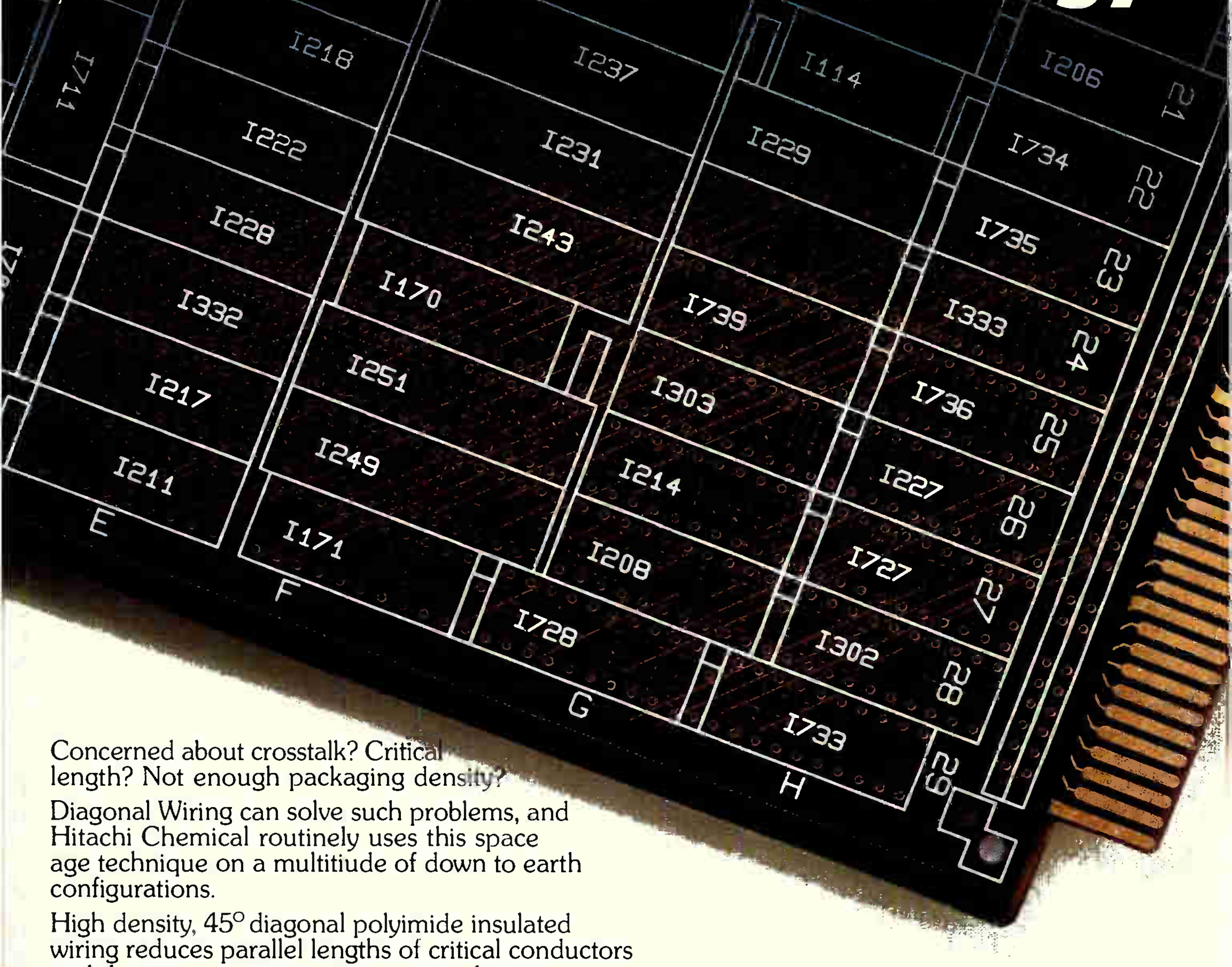

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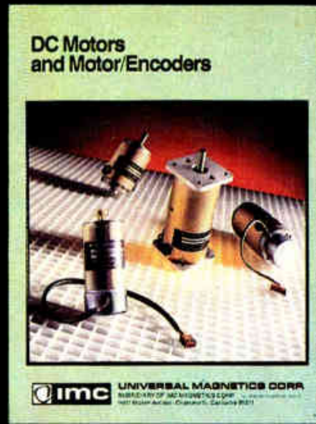
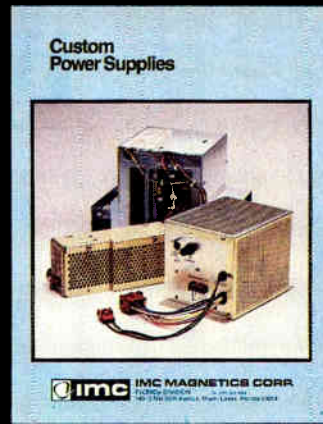
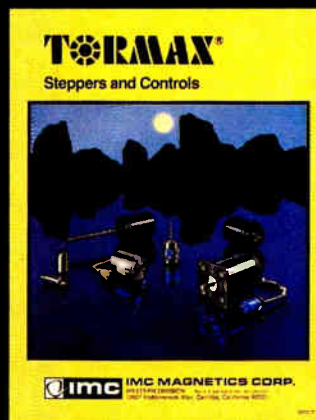


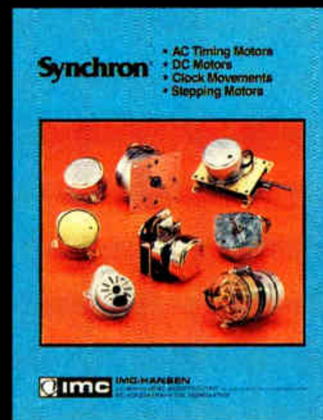
Circle Reader Service No. 165
Catalog features DC motors and motor/encoders along with performance data and specifications.



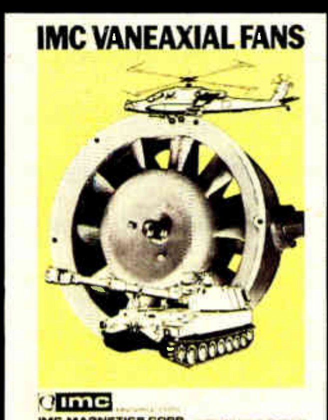
Circle Reader Service No. 166
Catalog shows how you can benefit from IMC's consolidation of resources as well as other information pertaining to their custom built power supplies.



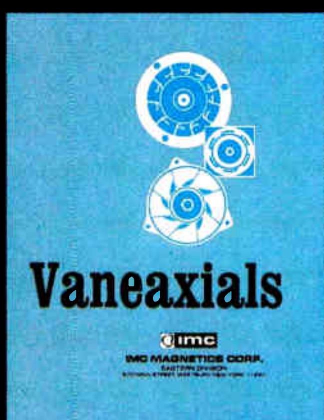
Circle Reader Service No. 168
Catalog features specialty stepping motors and listing of controllers to drive them. Also chapters on theory of operation, excitation modes and applications.



Circle Reader Service No. 167
Catalog gives general specifications on Synchron® AC timing motors as well as Magna-Torc DC motors. Products include clock movements, chart drives and slip ring assemblies.

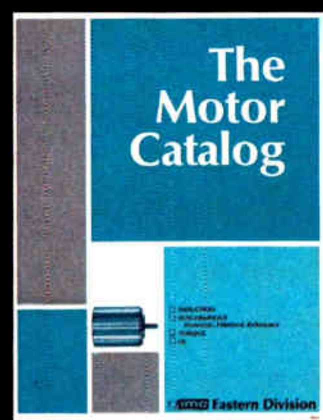


Circle Reader Service No. 169
Portfolio contains spec. sheets on IMC's complete line of large vaneaxial units. Fans are ideally suited for cooling applications requiring a large volume of air.



Circle Reader Service No. 170
Catalog contains information on air-movers rated for highest efficiencies. Included are charts as well as data on aerospace applications.

Circle Reader Service No. 171
Catalog contains an extensive range of centrifugal blowers to meet a variety of cooling requirements.



Circle Reader Service No. 172
Catalog is divided into sections for induction, torque and DC motors with sections devoted to technical information.

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QUAD-GATED DRIVER LETS BIPOLAR DO HARSH DUTY

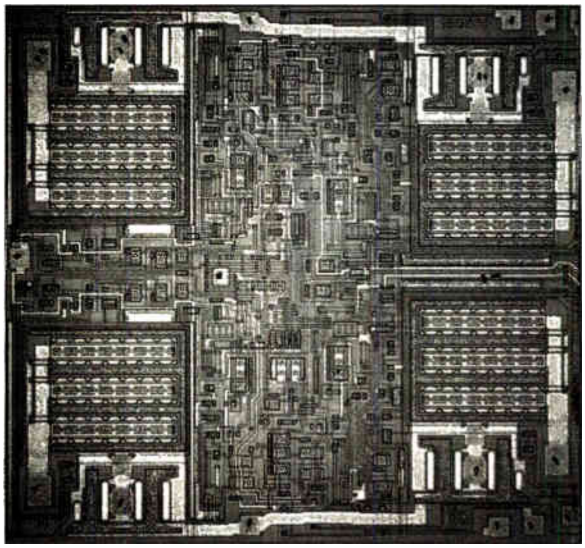
RCA DEVICE INDEPENDENTLY LIMITS TEMPERATURE AND CURRENT ON FOUR OUTPUTS FOR PROTECTION IN TOUGH ENVIRONMENTS

GE/RCA Solid State Division has targeted automotive and industrial applications for its quad-gated inverting power driver by incorporating into a bipolar device the protective features needed in harsh environments.

Previous implementations in these applications were almost entirely CMOS. No bipolar entrants offered the same degree of protection. Samples in dual in-line packages and surface-mounted versions of the device are available.

Containing four-gate switches, the CA3262 is a 16-lead circuit that interfaces low-level logic to inductive loads such as ac and dc motors, heaters, and vacuum-fluorescent displays. A key feature is its independent over-current and over-temperature limiting provisions on each of the outputs. Outputs are capable of switching 600-mA load currents without introducing spurious changes in the output state.

To maintain maximum heat transfer from the chip—an important factor in the constantly varying environment of automotive applications—the two center leads are directly connected to the die substrate and ground bond pads. This reduces the junction-to-air thermal resistance in free air to no more than 50°C/W, on the average. Without the precautions taken to ensure high-performance heat transfer, a comparable device would typically have a junction-to-air resistance in free air of about 150°C/W.



INTERFACE. RCA's quad driver connects low-level logic to inductive loads such as motors and fluorescent lamps.

If one output load is short-circuited, the remaining three outputs on the CA3262 function normally unless the 155°C maximum junction temperature of those outputs is exceeded. Also, the output stage does not change its logic state when in the current-limiting and thermal-limiting modes.

The CA3262 can drive as many as four incandescent lamp loads without modulating their brilliance. The devices can be cascaded to drive large loads.

Although its inputs are compatible with TTL logic or 5-V CMOS logic, the CA3262 can tolerate unusually high maximum input voltages. It can operate at a logic-supply voltage as high as 7 V and a logic-input voltage as high as 15 V. Output voltage is 50 V, and output sustaining voltage is 35 V. Featuring an output current of 1 A dc, the CA3262 has a power dissipation of 1.5 W.

In 1,000-unit quantities, the 16-pin device costs \$2.87 each in a plastic DIP and \$3.37 each when surface-mounted. They are available in production quantities.

–Bernard Conrad Cole

GE/RCA Solid State Div., Box 3200, Somerville, N.J. 08876. [Circle 360]

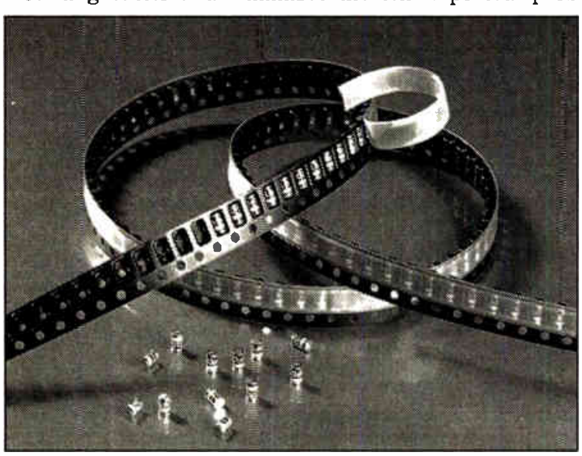
RECTIFIERS CAN BE SURFACE-MOUNTED

Philips International NV is fielding a family of rectifiers that offer performance and assembly advantages over conventional diodes. The company produced the new surface-mounted implosion diodes by adapting its existing implosion-diode technology to allow surface mounting on printed-circuit boards.

The SMIDs are fabricated by imploding a glass sleeve around the diode to form a high-integrity, cavity-free capsule. The encapsulating glass maintains excellent contact between the end studs and the diode crystal, resulting in low forward-voltage characteristics—about 10% to 15% lower than glass-bead diodes [*Electronics*, Aug. 21, 1986, p. 37]. Moreover, for the same size crystal, the cylindrical IDs are 20% to 30% smaller than ball-like glass-bead diodes.

Philips' 3.5-mm-long devices are 1.5 mm shorter than conventional diodes. The devices come in an SOD-87 package that can be packed on 8-mm tape instead of 12-mm tape, and they fit on a wider variety of surface-mounting machines, according to the company.

SMIDs save board space and weigh half as much as glass-bead diodes with crystals the same size, which makes mounting easier and minimizes the tendency of the diodes to roll during mounting. Their smaller diameter also requires less solder.



SMALLER. Philips' rectifiers can be packed on 8-mm surface-mounting tape instead of 12-mm tape.

Philips decided to adapt its IDs to surface mounting because customers reported problems with existing 5-mm-long surface-mounted-devices, says Graham Hine, international marketing manager for diodes at Philips' Electronic Components and Materials Division (Elcoma). The new devices handle up to 1 A at 1,000 V.

The new rectifier family includes the general-purpose BYD17 series; the BYD37 series, for fast-recovery applications such as TV; the BYD77 series epitaxial-avalanche rectifiers, for switched-mode power-supply and high-frequency applications;

and the BZD27 series of voltage regulators, for medium-power circuits.

Both the general-purpose BYD17 and fast-recovery BYD37 types feature a voltage range from 200 V to 1,000 V and an average 1.5 A of forward current. The corresponding values for the BYD77 versions are from 50 V to 400 V and 2 A.

The BZD27 series of voltage regulators have a nominal working voltage range of 7.5 V to 270 V. Certain types are available in the 300-to-510-V range on request, and the series will be extended to 3.9-V types in the future. The total power dissipation for this series is 2.3 W maximum. The nonrepetitive peak reverse power dissipation is rated at 300 W maximum.

Prices worldwide depend on importing country, but savings in mounting costs will more than offset the initially higher price, Hine says. In the U.S., Philips' distributor, Amperex Electronic Corp., says the rectifiers will be available in the first quarter of 1987. In volume quantities, BYD17 parts will cost 6¢ to 8¢ each; the BYD37, 7¢ to 10¢; and the BYD77, 11¢ to 22¢. The BYX27 regulators will be available in the second or third quarter of 1987. Prices for the BYX27 are not yet available.

–John Gosch

Amperex Electronic Corp., George Washington Highway, Smithfield, R.I. 02917. Phone (401) 232-0500.

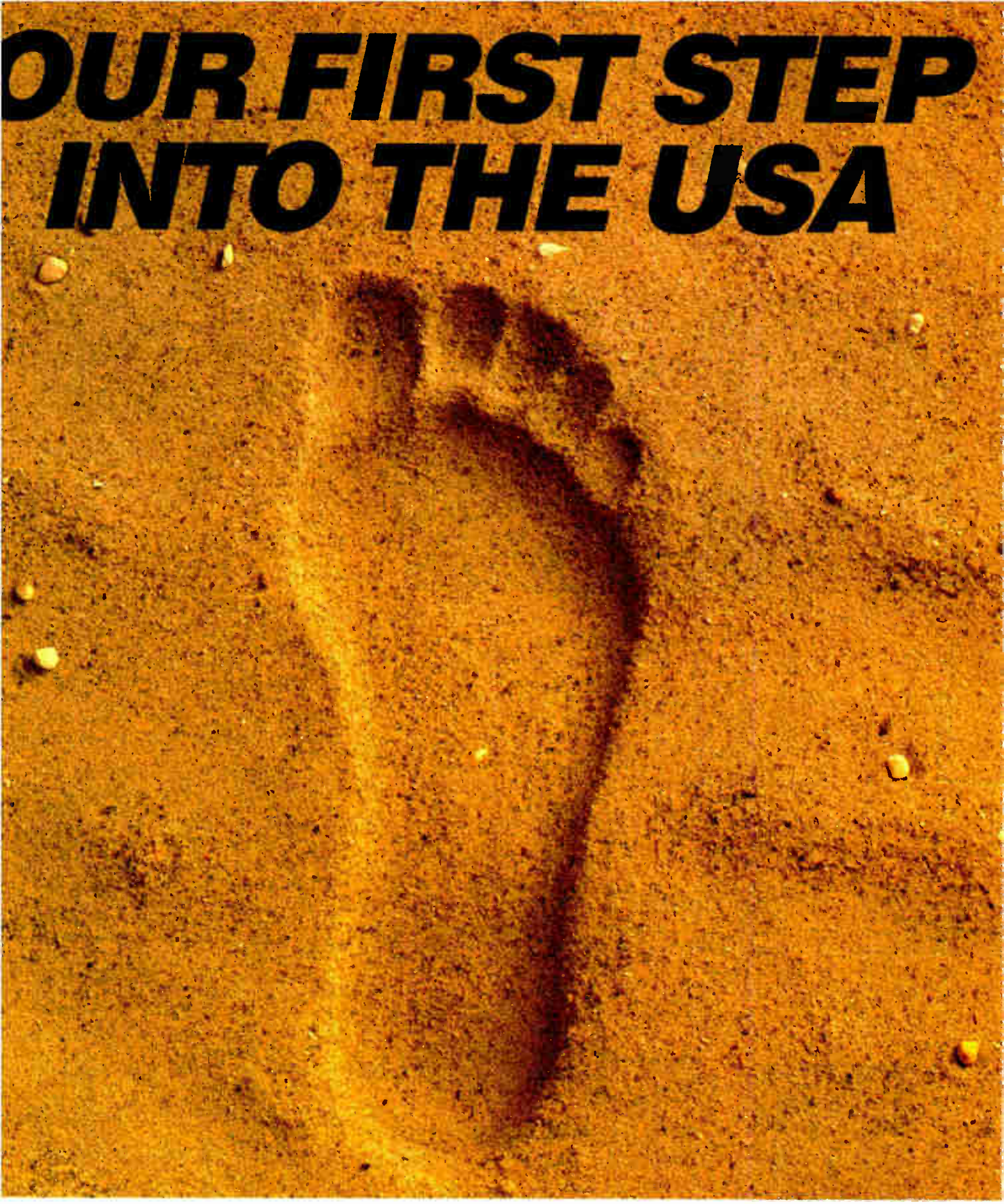
Philips Elcoma, P.O. Box 523, 5600 AM Eindhoven, The Netherlands. [Circle 361]

AT&T'S 32-BIT CHIPS WILL RUN AT 24 MHz

AT&T Technology Systems has rounded out its 32-bit product line with a microprocessor that targets high-performance, multiuser, multitasking Unix computing systems. The company's fastest 32-bit microprocessor—its predecessors ran at 10, 14, and 18 MHz—is one of three integrated circuits in the WE 32200 microprocessor and peripherals chip set.

Fabricated using 1-μm CMOS technology, the WE 32200 chip set supports clock speeds from 24 MHz to 30 MHz; the chips will initially be offered in 24-MHz versions only. The set consists of the WE 32200 central-processing unit, WE 32201 integrated memory-management unit and data cache, and WE 32206 math-acceleration unit. They are compatible with AT&T's existing WE 32100 chips.

The WE 32200 CPU features a 256-byte instruction cache, 32 registers, additional kernel and user registers, ad-



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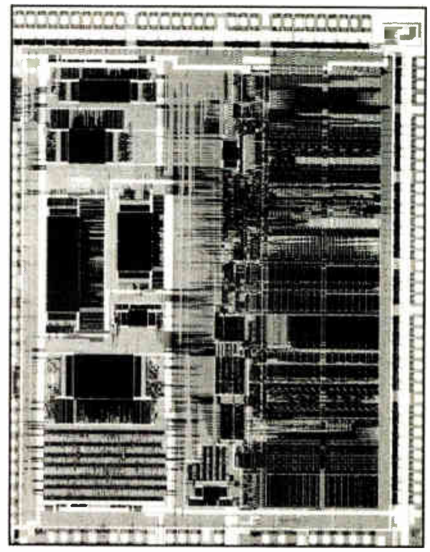

SPEEDY. AT&T's 32-bit WE 32206 floating-point coprocessor chip can execute 2.8 million Whetstones/s at 24 MHz.

dressing modes to support array access, enhanced quick interrupt, and binary-coded decimal arithmetic instructions.

The WE 32201 memory-management-unit chip provides logical-to-physical address translation and access protection for the WE 32200 CPU. It features a 4-K-byte on-chip integrated data cache. This cache speeds system performance by supporting zero-wait-state virtual-memory accesses. Four of the caches can be linked for up to 16-K of cache memory.

For math-intensive applications, the WE 32206 math-acceleration unit relieves CPU overhead and improves performance by transferring math functions from software to hardware. AT&T claims that the chip is faster than any floating-point coprocessor on the market. To cite a standard performance benchmark, it can execute 2.8 million Whetstones/s at 24 MHz and 3.5 million Whetstones/s at 30 MHz. Although an Inmos Corp. chip has benchmarked at 4 million Whetstones/s, it will not be available until next year. Typically, competitors benchmark between 0.3 and 1 million Whetstones/s.

Some 1,500 Unix applications packages are available to take advantage of that speed. "As developer of Unix, we offer depth in support that's unmatched in the industry," says Al Hofmann, manager of microprocessor marketing. For programming in-house WE 32200 applications, AT&T offers a complete line of software development tools, including Fortran, C, Pascal, and Ada compilers. Also available are math and input/output libraries, a symbolic debugger, assemblers, and a firmware tool for encoding EPROM software.

Engineering samples of the WE 32200 chip set will be available in the second

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Circle 139 on reader service card

quarter of 1987. Production quantities will be ready later in the year. In quantities over 100, the CPU chip will sell for $500 per unit, the memory unit/cache for $550, and the math acceleration unit for $425. *–Alexander Wolfe*

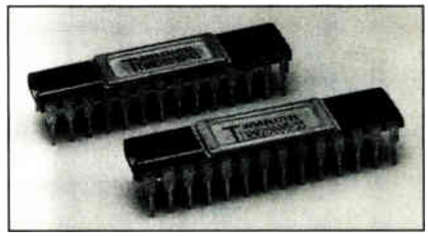
AT&T Technology Systems, 555 Union Blvd., Dept. KB, Allentown, Pa. 18103. Phone (800) 372-2447 [Circle 362]

TOSHIBA SRAM HAS 35-ns ACCESS TIME

Toshiba America Inc.'s n-MOS static RAM features access times as low as 35 ns. It is organized as 8,192 nine-bit words to provide an extra bit for parity checking.

The TMM2089C targets applications in control-store memories, cache memories, graphics, and telecommunications.

A power-down feature results in a maximum operating current of 120 mA,



and 10 mA in standby mode.

Packaged in a 300-mil-wide, 28-pin ceramic DIP, the chip is available with access times of 55 ns, 45 ns, and 35 ns. The devices cost $36.80 in 1,000-piece quantities, and delivery takes 8 to 12 weeks.

Toshiba America Inc., 2692 Dow Ave., Tustin, Calif. 92680. Phone (714) 832-6300 [Circle 365]

256-K CMOS EPROM USES ONLY 65 mA

A 256-K ultraviolet-erasable PROM from WaferScale Integration Inc. offers access times of 70 ns and is organized as a 32-K-by-8-bit array.

Fabricated with the company's 1.2-μm CMOS technology, the WS27C56F consumes 65 mA while cycling at full speed—less than one-fourth the power consumption of comparable n-MOS devices—while operating at twice the speed of n-MOS, the company claims.

It targets high-speed applications such as digital signal processing, and is available in a leadless, surface-mount package that reduces pc-board area requirements. It is also available in a conventional 28-pin ceramic DIP. Available in mid-January, the DIP version will cost $82 per 100 pieces; the surface-mount version, $110 per 100 pieces.

WaferScale Integration Inc., 47280 Kato Rd., Fremont, Calif. 94538. Phone (415) 656-5400 [Circle 366]

AMD GLUE-LOGIC PALs FEATURE 15-ns DELAYS

Programmable-array-logic chips with delay times as low as 15 ns from Advanced Micro Devices Inc. are program-compatible with the company's previous PAL devices.

The AmPAL16XXB series features a 15-ns delay time and a 40-MHz frequency with maximum power-supply current of 180 mA. The AmPAL16XXAL series has a 25-ns delay time, and a 90-mA supply current. For even lower power consumption, the AmPAL16XXQ series operates at 35 ns and 45 mA.

The chips are software-compatible with AMD's current AmPAL16XX, AmPAL16XXA, and AmPAL16XXL series of PAL devices.

The family is used in a variety of glue-logic and state-machine applications, such as computers and add-on cards. In 100-unit quantities of plastic DIPs, the AmPAL16XXB chips cost $5.85 each, and the AmPALXXAL $3.70 each. Both are in production. The AmPAL16XXQ costs $5 each in 100-unit lots and will be available in January.

Advanced Micro Devices Inc., 901 Thompson Pl., P.O. Box 3435, Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 368]

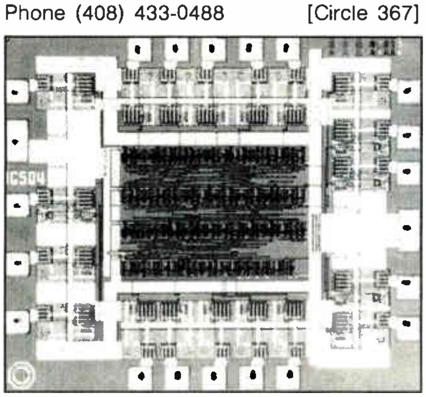
LOW-POWER REGISTER SUPPORTS 25 MHz

Zyrel Inc.'s 12-bit successive-approximation register runs at a guaranteed maximum speed of 25 MHz on less than 4 mA of current.

For use primarily in analog-to-digital converters, the Zy25HCT04 can also be used in ring counters and serial-to-parallel converters. Analog-to-digital converters capable of 5 million conversions/s can use the device. It is a 1.5-μm CMOS replacement for Advanced Micro Devices Inc.'s bipolar chips, the 2504 and 25L04, according to Zyrel officials.

The 25HCT04 is available now in chip form and in plastic DIPs. Its 100-piece price is $4.80 for the chip alone and $5.50 in the plastic DIP.

Zyrel Inc., 1900 McCarthy Blvd., Suite 201, Milpitas, Calif. 95035.
Phone (408) 433-0488 [Circle 367]



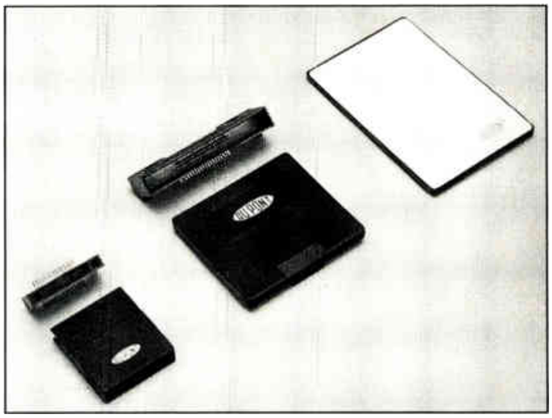
DUPONT'S MEMORY CARDS HOLD 1 Mb OF ROM OR RAM

COMPACT PACKAGES COMBINE SURFACE-MOUNT, CHIP-ON-BOARD, AND CONNECTION TECHNOLOGIES

Du Pont Co.'s Connector Systems Division has branched into a new field—chip-based memory cassettes that are capable of high-speed digital information retrieval. Three styles of the cassettes provide substantial memory capacity in handy packages that blend surface mounting, chip-on-board, interconnection, and materials technologies.

The memory cassette comes in three compact sizes in random-access-memory and read-only-memory versions, from 32 K through 1 Mb. The smallest, style M, for miniature, is 37 mm by 32 mm; the next, style S for standard, is 58 mm by 53 mm; and the largest, style CC, for credit-card size, is 58 mm by 85 mm. Style CC is the first 1-Mb credit-card-size RAM memory cassette, the company claims.

Each device has two parts: a cassette with an integral connector, and a mating header. A special pin-and-socket connector has been developed that can withstand a minimum of 10,000 mating cycles. Connector contacts are palladium-nickel-plated with gold flash for durability. The miniature connector has its pins on 50-mil centers.



HANDY. DuPont's memory cards come in three convenient sizes and have a variety of applications.

The 1-Mb CMOS static-RAM cassette consists of 16-by-64-K chips tape-bonded to a thin epoxy-glass printed-circuit substrate assembled inside a 120-mil-thick plastic card case.

The nylon connector and header housings have 38 mechanically shielded male/female contacts. Polarized to prevent misapplication, the device provides electromagnetic-interference and static-discharge protection and includes a write-protection switch. Read/write cycle time is 350 ns. A 3-V lithium battery provides 2.5 years of data retention.

The S cassette can be used for either RAM or ROM packaging with 40 I/O contacts on 50-mil centers. It can accommodate 4-, 8-, or 16-K bytes of RAM or two or three times 128-, 256-, or 512-K byte ROM, depending on the number of memory chips desired. The M cassette has 30 I/O contacts and provides one or two times 128-K, 256-K, or 512-K ROM capacity.

Applications include text memory and type fonts of printers, electronic typewriters, and word processors; video/image memory for videotex, teletex, or CAD/CAM; language-instruction display for copiers; and software backup to floppy disks.

–Jerry Lyman

Dupont Co. Connector Systems Division, 30 Hunter Lane, Camp Hill, Pa. 17011. Phone (717) 975-2000 [Circle 400]

LIGHT MONITORS, CONTROLS OWN OUTPUT

A lighting system from Lightgate monitors its own output and adjusts power to maintain the desired light-output level to within 1%. The system, called the LightSource 2010, also monitors incoming power to sense when a light source is about to fail. An optional programmable control cell, programmed by an IBM Personal Computer, allows the modulation of polarity, color, and intensity while maintaining the same output light level.

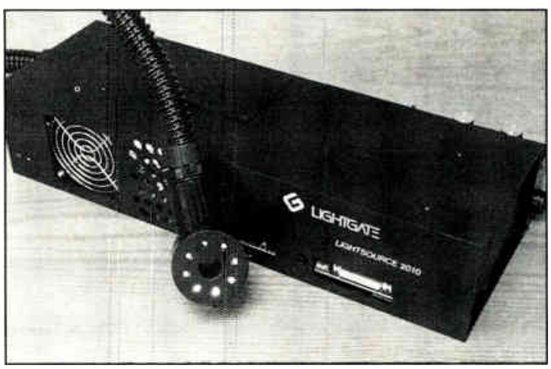
Lightgate, an Oakland, Calif., specialist in light-modulating products, developed LightSource 2010 for robot vision systems. However, Lightgate President Victor B. Kley expects it to be used as a component in a wide variety of applications in still photography and motion pictures and generally in the measurement and planning of lighting requirements. The system plays a key control role in a robotic wire and tape bonder built by Shinkawa of Japan and displayed this month at Semicon in Tokyo.

The programmable control cell utilizes liquid-crystal elements to modulate light output for maximum contrast. In a wire bonder such as the one displayed at Semicon, the robot sensor must distinguish between leads and lead spacings, Kley explains. If the light has high reflectivity, the robot will not always be able to distinguish between leads and spacings on the basis of contrast. Consequently, it will fail to make a certain percentage of the bonds.

Lightgate adapted a technique it developed for enhancing contrast in microscopes to eliminate glare in bonding applications. Only a few combinations of polarity, color and intensity will work for any given situation. "We build a histogram of the problem and select the best set of solutions," Kley says. "With this kind of structured lighting, we can guarantee to deliver the contrast required 100% of the time."

The system can be controlled manually or remotely, or by a PC over an RS-232-C interface link. It responds in less than 15 ms to changes in light output, as detected by a photodiode. Under computer control, the system can link up to 16 light sources and control a total of 32 kW. Current versions use tungsten/halogen lamps; a discharge-lamp version is planned.

For applications where a continuous light source is required, such as an inspection line where a bulb failure will shut down the line, the 2010 can warn of impending problems. It monitors how much power is required to operate the bulb at its peak; when this value exceeds a certain boundary, the system signals that the bulb is about to fail.



VERSATILE. Lightgate's programmable light source can be used in robot vision, photography, and motion pictures.

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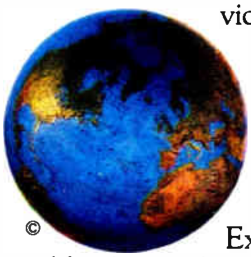

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The 2010 operates at 90 to 130 V and from 40 to 80 Hz. The light source alone costs $2,000 for a single unit, and "under $1,000" in quantity, Kley says. With the light-control module, the single-unit price is $5,000. The systems are available now.

Lightgate, 6300 Telegraph Ave., Oakland, Calif. 94609.
Phone (415) 653-8500 [Circle 401]

VME BOARD HOLDS 32-BIT COMPUTER

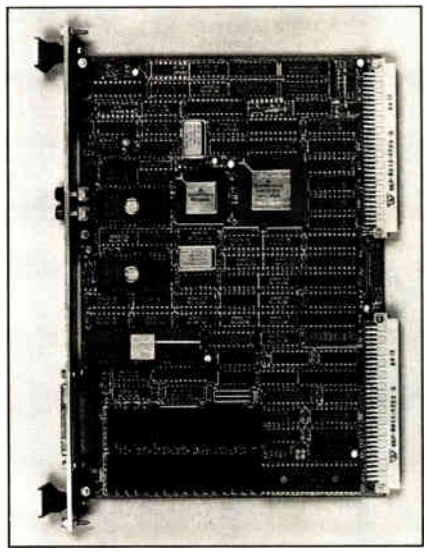
Motorola Inc. is combining its 32-bit 20-MHz MC68020 central processing unit and MC68881 floating-point math coprocessor with 1 megabyte of dynamic random-access memory, putting all on a single VMEbus-compatible printed-circuit board.

The MVME133A-20 is a $4,250 computing engine for real-time operations such as robotics, machine and numerical control, and image processing, say executives at the company's Phoenix, Ariz., microcomputer division.

A key feature of Motorola's new board computer is its software compatibility with the company's predecessor products. Designers can often integrate the 68020's high clock rates and other features into existing systems without undue compatibility problems, the company says.

The 68020 microprocessor features external 32-bit address-and-data-paths capability, enhanced addressing modes, and on-chip instruction cache.

The 68881 floating-point coprocessor fully implements the IEEE standard for binary floating-point arithmetic. It will



OPTIONS. Motorola's board computer can be fitted with software offering 32 debugging, up/downline load, and disk boot commands.

substantially improve speed in applications that require arithmetic computations over nonfloating-point processors, the company says.

The 68881 uses three standard types of operations: byte, word, and long-word integers; single-, double-, and extended-precision real numbers; and packed, binary-coded-decimal real numbers. Each operation supports seven data formats as well as a full set of trigonometric and transcendental functions.

Included in the MVME133A-20 board is one serial debugging port, one RS-232-C multiprotocol serial port, one RS-485/RS-422 multiprotocol serial port, three 8-bit timers, a real-time clock, and an A32/D32 VMEbus master interface.

The four 28-pin memory sockets are organized as two banks with two sockets per bank for ROM, programmable-ROM, erasable PROM, and electrically erasable PROM. This wide array of features provides the required functions for a large number of applications.

Options include a debugging package that offers 32 upload, download, and disk-bootstrap-load commands, as well as a full set of on-board diagnostics and an on-line assembler/disassembler.

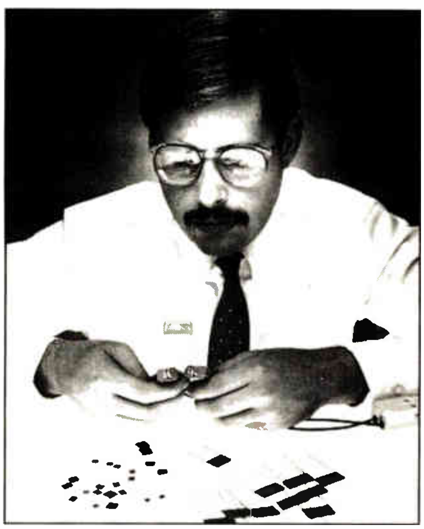
The MVME133A-20 and the $500 debug software package are available now. *–Ellie Aguilar*

Motorola Inc., Microcomputer Division, P.O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 438-3501 [Circle 402]

DIELECTRIC HIKES CAPACITANCE VALUES

Marcon America Corp.'s multilayer ceramic capacitors use a niobium-oxide-based dielectric material to achieve double the dielectric constants of conventional capacitor materials.

The TCD series offers a capacitance range of 0.1 to 47 mF and voltages of 50, 100, and 250 V dc from stock; 400-V devices are available on request. Special



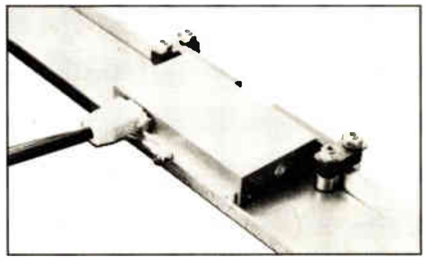
orders are also accepted for customized, surface-mounted multilayer capacitors.

Applications include surge protection for ICs, filtering for switching power supplies, and bypass decoupling.

Marcon America Corp., 310 Era Dr., Northbrook, Ill. 60062.
Phone (312) 564-2820 [Circle 405]

LINEAR MOTORS GIVE PRECISE POSITIONING

A family of linear motors from Stock Drive Products Inc. uses an electromagnetic system to hold friction to a minimum and to achieve microstep accuracies of 0.001 in. The Series 7302 and 7304 motors—for two- and four-phase operation, respectively—are designed for accurate positioning of *x-y* plotters; wafer processing; pc-board assembly; and automated-inspection systems.



The motors replace conventional leadscrews or cable-pulley systems with a moving part controlled by electromagnets. It moves over a 0.005-in. air gap created by the electromagnetic field. The electromagnet's coils also move it linearly in microsteps of 0.001 in.

The company offers versions that operate over 36-in. or 72-in. magnetic platens. A two-phase device costs $1,463. All models are available now.

Stock Drive Products Inc., 2101 Jericho Tpke., New Hyde Park, N.Y. 11040. Phone (516) 328-3330 [Circle 406]

CONNECTORS OFFERED FOR FLAT CABLES

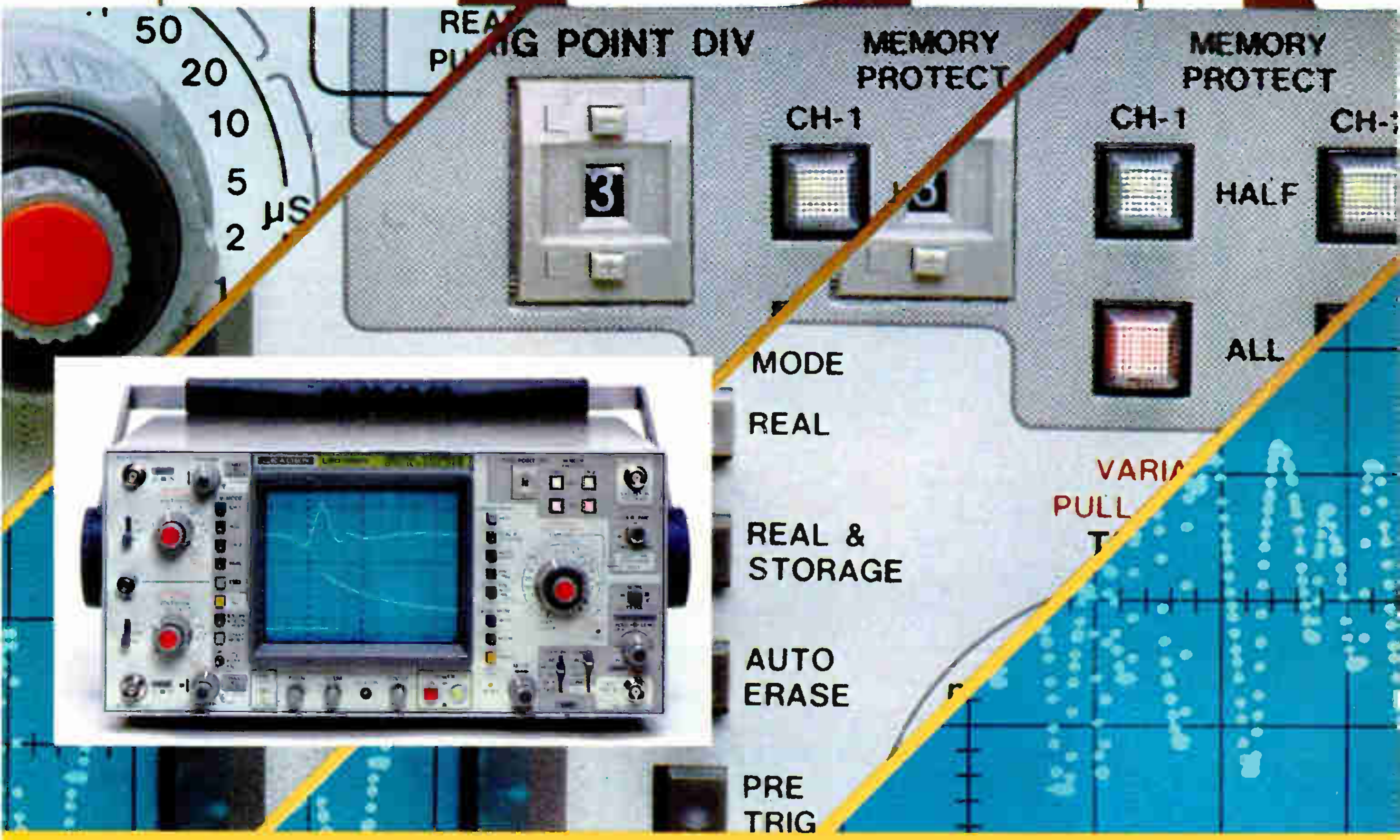
A family of connectors developed by the Ansley Electronics Division of Thomas & Betts Corp. allows the simultaneous mass termination of as many as 64 conductors in flat cables.

Space savings and reduced costs associated with flat cables compared with wiring harnesses are best realized when the multiple connectors in the cable are terminated simultaneously rather than one at a time, says the company.

The units include transition connectors, DIP socket connectors, and low-profile DIP plugs. The family includes 600 different units. All are fabricated in Pocan polyester resin reinforced with 30% glass fiber.

The connectors' electrical qualities include a dielectric strength of 492 V/mil and an arc resistance of 10 s. Their ten-

LEADER



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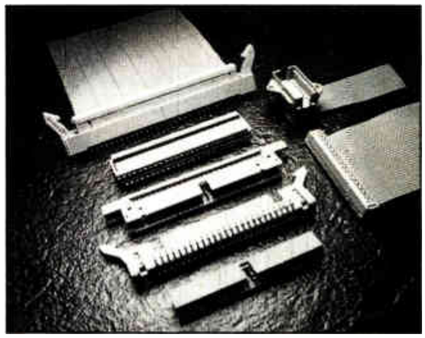

sile strength of 19,900 lb/in.^{2} and flexural stress at break is 27,600 lbs/in.^{2}. All the connectors are available through distributors. Price depends on configuration and size.

Thomas & Betts Corp., Electronics Division, 920 Rt. 202, Raritan, N.J. 08869.
Phone (201) 469-4000 [Circle 407]

FINLUX EL DISPLAY CUTS POWER NEEDS

Finlux Inc. has reduced power requirement in its newest flat electroluminescent display by 30% by utilizing a proprietary energy-recovery circuit, says the company.

Power consumption of the MD512.256-40, including its power unit, is 11 W in typical use and 16 W maximum. Another benefit of the new drive scheme is an average 10°C decrease in the display-driver temperature, which results in longer life than previous models.

Graphics are displayed in a flicker-free yellow produced by an electroluminescent phosphor. The 4-by-8-in. display offers 67-line/in. resolution.

The display is available in preproduction quantities. The single-unit sample price for the display and power converter is $1,115. In 100-unit quantities, the price is $590.

Finlux Inc., 20395 Pacifica Dr., Suite 109, Cupertino, Calif. 95014.
Phone (408) 725-1972 [Circle 408]

RESISTORS SUIT DENSE PC BOARDS

The CR series of 1/8-W and 1/16-W chip resistors from International Components Corp. are designed for high-density use on pc boards and for small-to-large hybrid integrated circuits.

Innovative electrode construction and thick-film elements with glass coatings endow the resistors with high mechanical strength and electrical stability, the company says, and they operate between –55°C and 125°C.

Available from stock, they are priced as low as $9.50 per 1,000 and come packaged on tape or reel.

International Components Corp., 105 Maxess Rd., Melville, N.Y. 11747.
Phone (516) 293-1500 [Circle 409]

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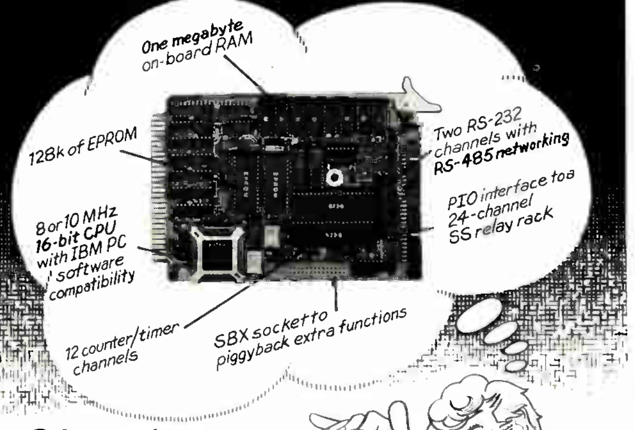

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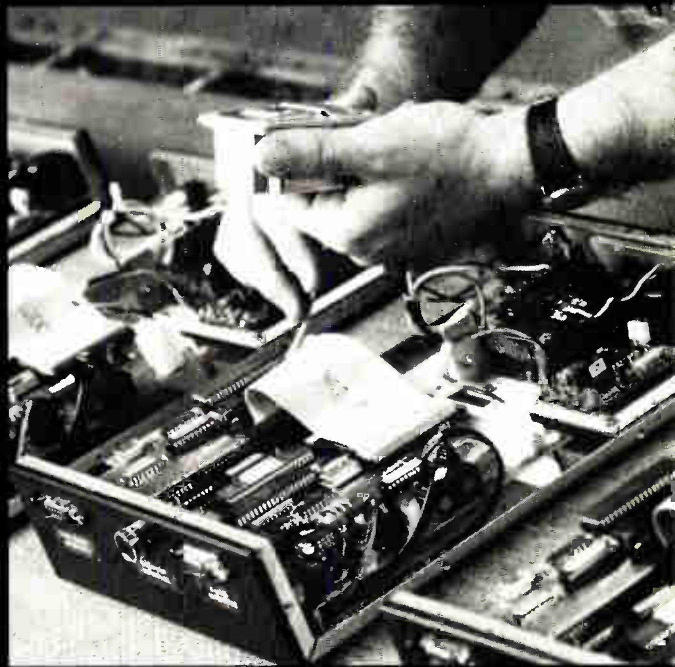

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MEETINGS

SMART III: Surface Mounting and Reflow Technology, EIA, *et al.* (2001 Eye St., N.W., Washington, D.C. 20006), New Orleans Hyatt Regency, New Orleans, La., Jan. 12-15.

Computer Graphics '87, Frost & Sullivan Inc. (106 Fulton St., New York, N.Y. 10038), Wesgate Hotel, San Diego, Jan. 14-16.

OFC/IOOC '87: Optical Fiber Communication Conference/International Conference on Integrated Optics and Optical Fiber Communication, IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Pl., N.W., Washington, D.C. 20036), Reno-Sparks Convention Center, Reno, Nev., Jan. 19-22.

Hybrid Microtech '87: Conference and exhibition for electronic interconnection technology, International Society for Hybrid Microelectronics (Hybrid Microtech Secretariat, 13 Firlands, Bracknell, Berkshire RG12 3SB, England), Heathrow Penta Hotel, Heathrow, UK, Jan. 19-21.

International Symposium on Modeling and Simulation Methodology, University of Arizona, *et al.* (Special Professional Education, Harvill Building/Box 9, Tucson, Ariz. 85721), Hotel Park Tucson, Tucson, Ariz., Jan. 19-23.

SYSCON: OEM Computer Peripherals Subsystems Conference & Exposition, Multidynamics Inc. (17100 Norwalk Blvd., Suite 116, Cerritos, Calif. 90701), Los Angeles Airport Hilton Hotel, Los Angeles, Jan. 20-21.

Uniforum Conference and Trade Show, USR/group (4655 Old Ironsides Dr., Suite 200, Santa Clara, Calif. 95054), Washington Convention Center, Washington, D. C., Jan. 20-23.

Winter 1987 Usenix Technical Conference, Usenix Association (P.O. Box 385, Sunset Beach, Calif. 90742), Omni Shoreham, Washington, D. C., Jan. 21-23.

Southern Manufacturing Technology Show, National Machine Tool Builders Association (7901 Westpark Dr., McLean, Va. 22102), The Charlotte Convention Center, Charlotte, N.C., Jan. 26-29.

Advanced Semiconductor Equipment Exposition & Conference, Cartlidge & Associates Inc. (1101 S. Winchester Blvd., Suite M259, San Jose, Calif. 95128), Santa Clara Convention Center, Santa Clara, Calif., Jan. 27-29.

Wincon '87, Aerospace and Electronic Systems Society (P.O. Box 6876, Burbank, Calif. 91510), South Coast Plaza Hotel, Costa Mesa, Calif., Jan. 27-29.

1987 Annual Reliability and Maintainability Symposium, IEEE, *et al.*, (Gen Pettee, Lockheed Missiles and Space Co., P.O. Box 1269, Cocoa Beach, Fla. 32931), Dunfey City Line Hotel, Philadelphia, Jan. 27-29.

Computer Graphics New York '87, Exhibition Marketing & Management Inc. (8300 Greensboro Drive, Suite 690, McLean, Va. 22102), The Jacob Javits Convention Center, New York, N. Y., Jan. 28-30.

Measurement Science Conference, MSC (John Van de Houten, program chairman, TRW S/937, One Space Park, Redondo Beach, Calif. 90278), Irvine Marriott, Irvine, Calif., Jan. 29-30.

International Symposium on Pattern Recognition and Acoustical Imaging, International Society for Optical Engineering (P.O. Box 10, Bellingham, Wash. 98227), Newport Beach, Calif., Feb. 1-6.

International Conference on Data Engineering, IEEE Computer Society (1730 Massachusetts Ave., N.W., Washington, D.C. 20036), Pacifica Hotel, Los Angeles, Feb. 2-6.

Manufacturing Productivity Conference & Exposition, Society of Manufacturing Engineers (One SME Dr., P.O. Box 930, Dearborn, Mich. 48121), Expo Centre, Orlando, Fla., Feb. 2-5.

Aerospace Applications Conference, IEEE South Bay Harbor Section (Fausto Pasqualucci, Hughes Aircraft, 3100 Fujita St., Torrance, Calif. 90509), Vail, Colo., Feb. 8-13.

Communication Networks '87, CW/Conference Management Group (375 Cochituate Rd., Box 9171, Framingham, Mass. 01701), Washington Convention Center, Washington, D.C., Feb. 9-12.

Systems Design & Integration Conference, IEEE, *et al.* (Electronic Convention Management, 8110 Airport Boulevard, Los Angeles, Calif. 90045), Santa Clara Convention Center, Santa Clara, Calif., Feb. 10-12.

Southwest Optics '87, IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Place, N.W., Washington, D.C. 20036), Albuquerque Convention Center, Albuquerque, N.M., Feb. 9-13.

Electronics

1987 Recruitment Editorial Calendar

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February 19	Computer-Aided Engineering Hannover Fair Preview	February 2
March 5	Online Transaction Systems ISSCC Wrap-Up	February 16
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November 26	Military Electronics Parallel Processing ISDN IEDM Preview	November 9
December 17	Year-End Double Issue Executive Outlook ISSCC Preview GaAs Technology	November 30

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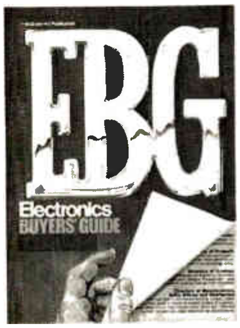

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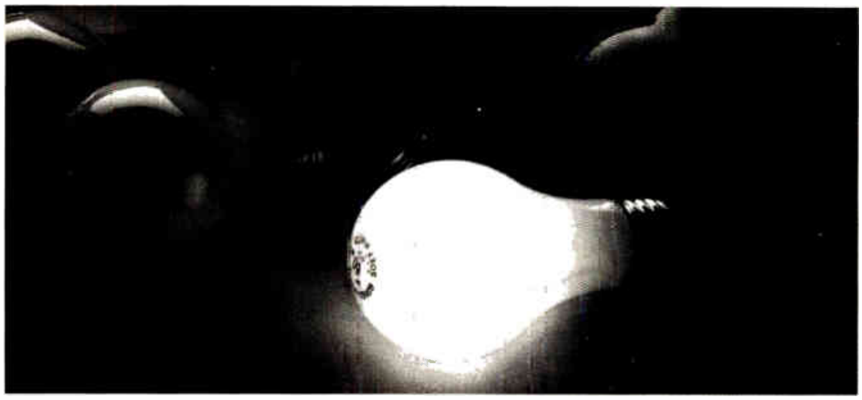

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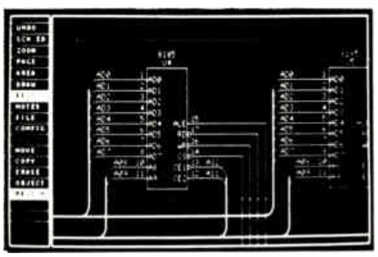

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ELECTRONICS WEEK

HONEYWELL EXITS COMPUTER FIELD...

Honeywell Inc. is easing out of the computer business. The Minneapolis firm is splitting off Honeywell Information Systems into a new, separate company that will be managed by Compagnie des Machines Bull, Paris, which is buying a 42.5% share in the new company. Honeywell will also maintain a 42.5% stake in the business, and NEC Corp., Tokyo, will own the remaining 15%. Honeywell plans to take in about $522 million on the deal. That includes about $350 million to be paid by the new company for return of capital and repayment of debt, and about $172 million from NEC and Bull. Honeywell says the sale will allow it to better concentrate its resources on its defense, aerospace, automation, and controls businesses.

...AND FORECASTS RARE LOSS FOR '86

For the first time in 95 years, Honeywell Inc. expects to see red ink on its year-end financial disclosure. The price at which the 101-year-old company is selling the majority interest in its computer business is based in part on a $250 million discount off the unit's book value, which Honeywell claims to be $900 million. Combined with other write-offs, the discount will force Honeywell to show substantial losses for its fourth quarter and year-end reports.

PANASONIC TO SELL CHIPS IN U. S.

Panasonic Industrial Co. has formed a new division to market semiconductors in the U. S. The Semiconductor Sales Division will start out with a line of power MOS FETs and a variety of memory and logic products, including a pair of 1-Mb random-access memories and families of gate arrays and standard cells. The devices will be made by Panasonic's sister company, Matsushita Electronics Corp., of Kyoto, Japan.

AT&T, BOEING JOIN IN TELECOM BID

AT&T Co. and Boeing Co. say they will enter a joint bid for the Federal Telecommunications System 2000 program, a 10-year contract that could be worth as much as $4.5 billion. Ironically, AT&T will be squaring off with a team that includes the seven regional Bell operating companies, which just two years ago were still part of AT&T. The BOC team includes some competition that should be more familiar to AT&T—Martin Marietta, the prime contractor; Northern Telecom; and MCI. The contract is being administered by the federal General Services Administration, which is expected to issue a formal request for proposals this month. The winner should be determined within a year.

W. GERMANY, CHINA TEST TV MEETINGS

West Germany and the People's Republic of China have started two-month trials in video teleconferencing among the 13 public video-conference studios run by the West German post office and a similar studio in China's capital of Beijing. West German and Chinese government officials and business managers will be able to use the 6,000-mile video link, which will carry both voice and full-motion color TV pictures, free of charge until the trials end Jan. 31.

FLEXIBLE COMPUTER SHORT OF CASH

Flexible Computer Corp., the Dallas maker of parallel-processing computers, postponed its annual stockholders meeting last week after disclosing that it was experiencing a "severe working-capital shortage" and was in default on some of its obligations. The computer maker is revising its net income and sales figures for 1985 and the first three quarters of this year, when it had been reporting sales income before the deals had been completed. Flexible had reported a net loss in 1985 of $7.6 million on sales of $2.5 million, and through third quarter 1986, the company was $3.2 million in the red on sales of $4.2 million. Now Flexible's auditor, Arthur Andersen & Co., has withdrawn certification of the company's 1985 financial statement, and no date has been set for release of the revised figures. Flexible is seeking additional financing, but a spokesman warns there is "no assurance that [the search] will be successful."

PHILIPS SETS DEAL WITH MATSUSHITA

Philips International NV of the Netherlands and Matsushita Electronics Corp. of Japan are joining forces to launch a new family of 8-bit CMOS microcontrollers. Under the new agreement, Matsushita will manufacture and market the PCF84CXX family designed and developed by Philips. The pact is aimed at ensuring customers of two sources of supply as soon as the family hits the market.

TANDON WILL BUY MAKER OF BIG DISK

The Tandon Corp., Chatsworth, Calif., which has been repositioning itself as a supplier of IBM-compatible personal computers, is again paying attention to the disk drive market. Tandon is attempting to flesh out its line of disk drives, which reaches only 40 megabytes at the high end, by acquiring struggling Atasi Corp., San Jose, Calif. Atasi offers a 170-megabyte drive but barely survived Chapter 11 bankruptcy proceedings earlier this year. Terms of the deal, which is not yet final, were not disclosed. Although Tandon will move volume production of Atasi drives to Singapore, the company says it has no plans for wholesale layoffs in the U. S.

AEL GETS 6% SHARE IN ISRAEL'S TADIRAN

Philadelphia-based American Electronic Laboratories Inc. is trading its 59% share in Elissra Electronic Systems Ltd., an Israeli defense-electronics maker, to Israel's largest electronics company, Tadiran Ltd., which already owns 41% of Elissra. In exchange, AEL will get a 6% stake in Tadiran, in an agreement that should be signed by the end of the year. Elissra, which makes equipment for electronic warfare and civilian and military telecommunications, had sales of $60 million this year but is expected to report a $4 million loss—its first in 19 years. Elissra blames the loss on increasingly high labor costs in Israel.

TEXET ADDS WANG TO CUSTOMER BASE

Texet Corp. continues to sign up major hardware vendors for its electronic-publishing software, and Wang Laboratories Inc. of Lowell, Mass., is its latest partner. The agreement calls for Texet to integrate its software with the Wang VS line of minicomputers, which will then be distributed through Wang's regular channels. Earlier this year, Texet signed similar agreements with Sun Microsystems Inc. of Mountain View, Calif., Compugraphic Corp. in Wilmington, Mass. and I3D/Framatome in Paris. The Arlington, Mass., company says that it will continue to market its dedicated electronic-publishing systems independently, while continuing to pursue more cooperative arrangements.

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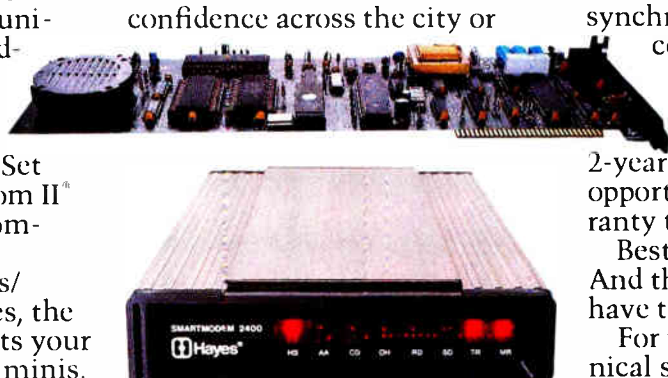

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TLC-363

TLC-402

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	VDD	7 V	7 V
	VDD – VEE	20 V	20 V
Input Voltage		0≦VIN≦VDD	VSS≦VIN≦VDD
Recommended Operating Conditions			
Supply Voltage	VDD	5±0.25V	5±0.25V
	VEE	−11±3V Var.	−11±3V Var.
Input Voltage	High	VDD – 0.5V min.	VDD – 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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