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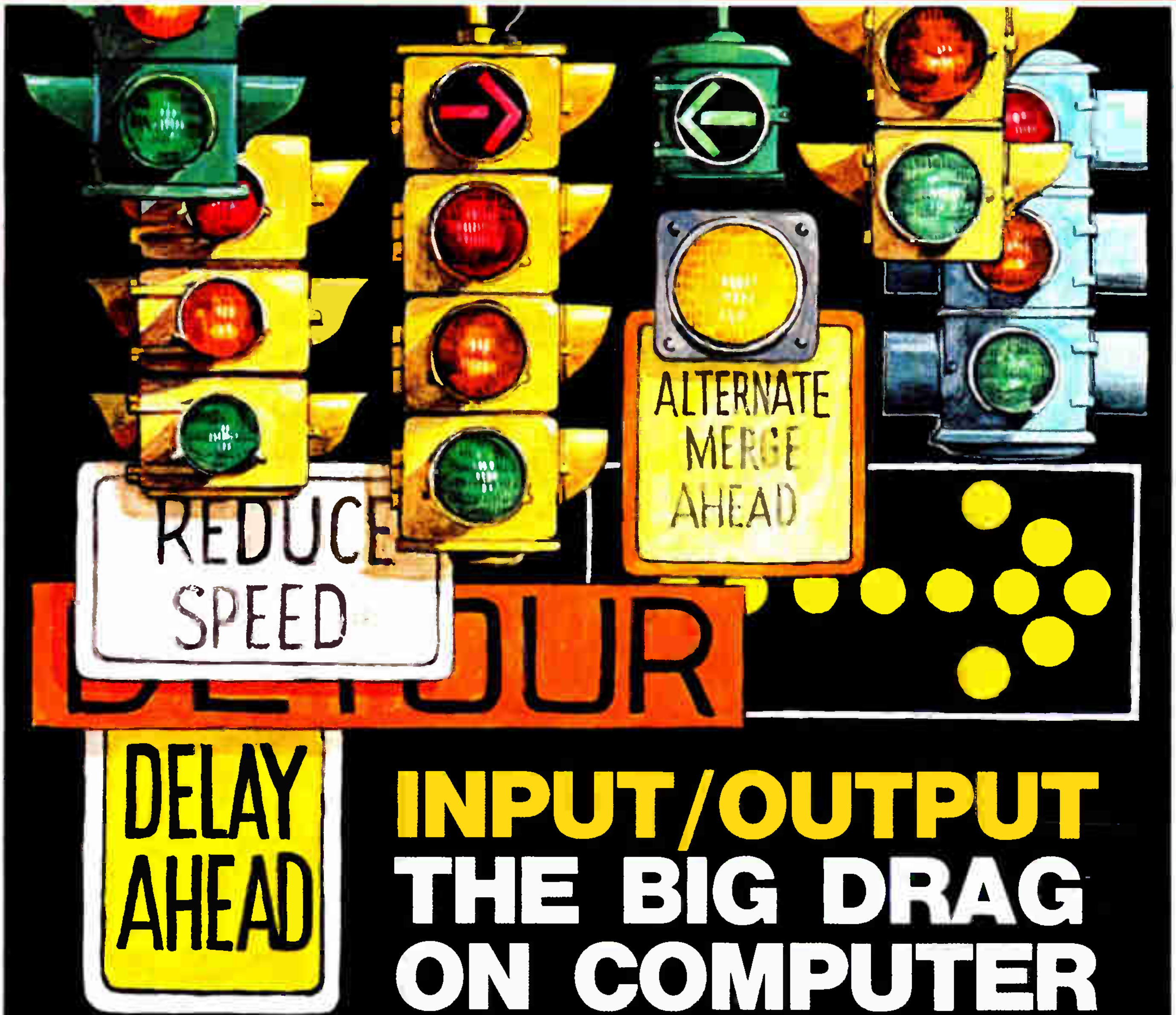

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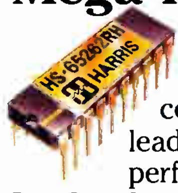

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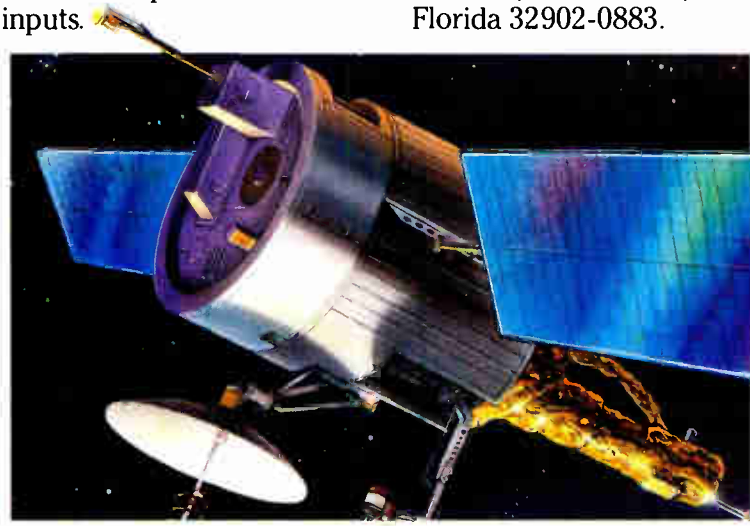

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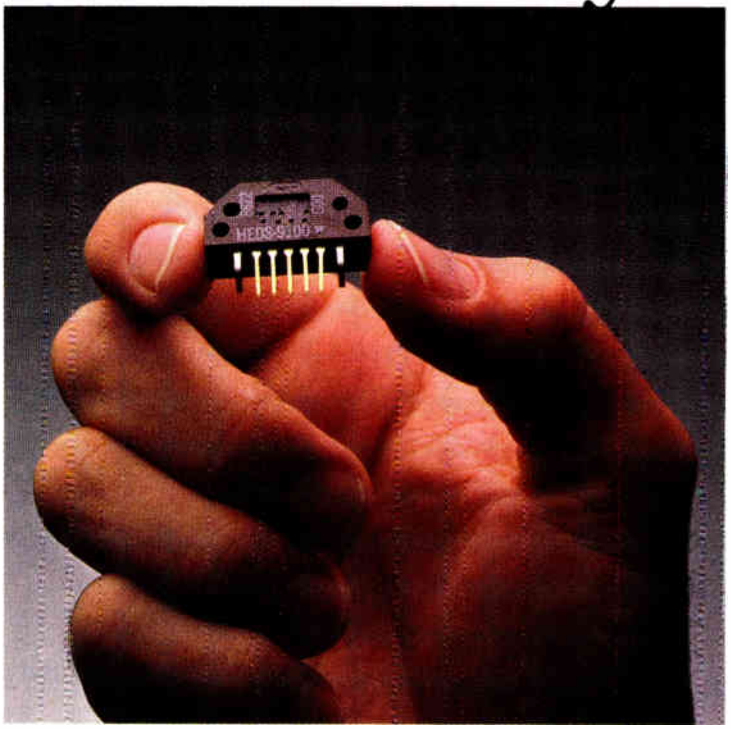

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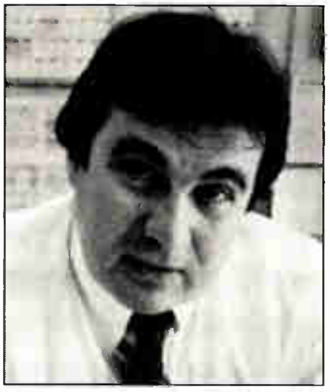

SHANDLE: *Electronics'* editing means "a higher-grade product."

Comparing the way we do things at *Electronics* with the way they were done at his newspaper, Jack says he is impressed by the exhaustive fact-checking and editing process at the magazine. "When I wrote a story for the newspaper, it went in the paper without much editing. Here, no fewer than four people scrutinize it, and while that can be a frustrating experience sometimes for the writer, it certainly makes for a much higher-grade product than dailies or weeklies," he says.

Jack can testify about quality control from an unusual dual perspective, that of a man who has been educated as an electronics engineer and journalist. Jack has a background that is ideally suited for any *Electronics* editor: he earned a bachelor's degree in EE from the University of Pennsylvania and then, 10 years later, a master's in journalism from Temple University. Both schools are in Philadelphia. In the interval, he worked as an electronics engineer for the Philadelphia Electric Co. and wrote an as yet unpublished novel.

"But the bulk of my experience as a writer and editor came at the *Bucks County Courier Times*, the largest suburban newspaper in Pennsylvania," says Jack. Most recently, he was the chief political writer and columnist.

While working for the *Courier Times*, Jack won numerous awards, including a first place for investigative reporting in 1981, from the Greater Philadelphia chapter of Sigma Delta Chi, the Society of Professional Journalists. In 1985 he won a first prize for feature writing from the Pennsylvania Associated Press Managing Editors Association.

Although Jack has moved his career to *Electronics*, his home is still in peaceful Bucks County, in the southeastern corner of Pennsylvania. That means a daily one-way commute of about 60 miles, which totals about 3 hours, including two hours on a train. "I don't mind," he says. "It's good to get back to the slower-moving suburban life after the frenetic pace of New York."

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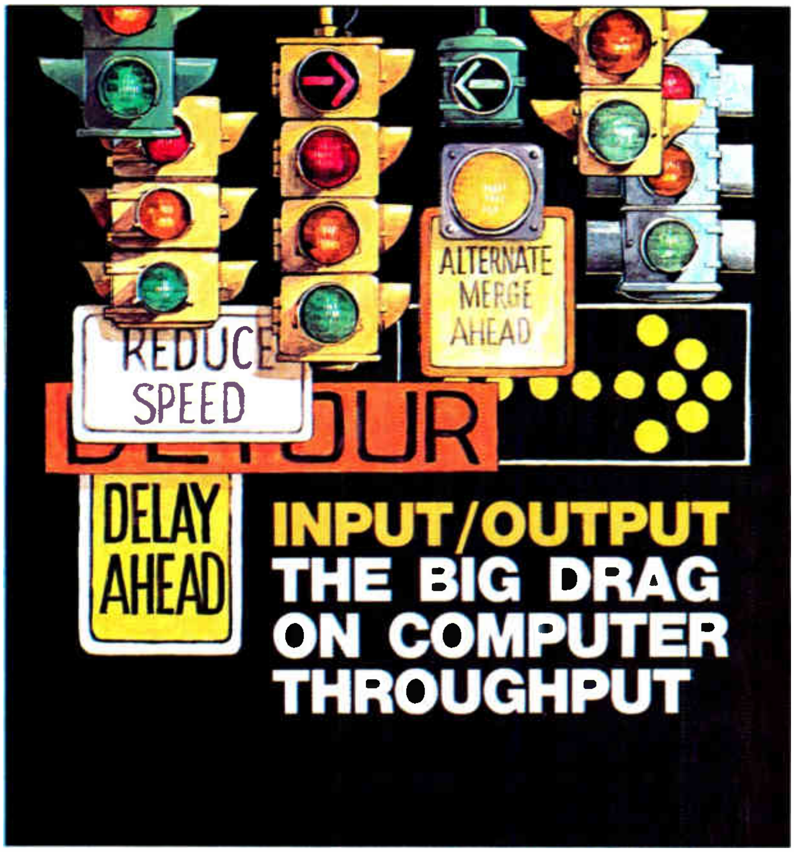

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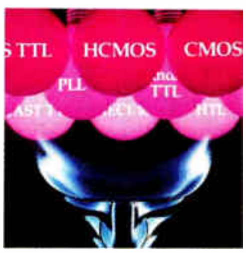

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Skinner's gloomy prediction: In 10 years, only two of the top 10 chip producers will be American— IBM and Texas Instruments

It's handwringing time around the U. S. semiconductor industry. Japan's mighty Fujitsu is buying Fairchild Semiconductor, the grand old lady of the U. S. semiconductor industry. To hear Fairchild managers tell it, it's a good move. But for many industry observers, it's the beginning of the end for a U. S. industry that had grown accustomed to being the world leader.

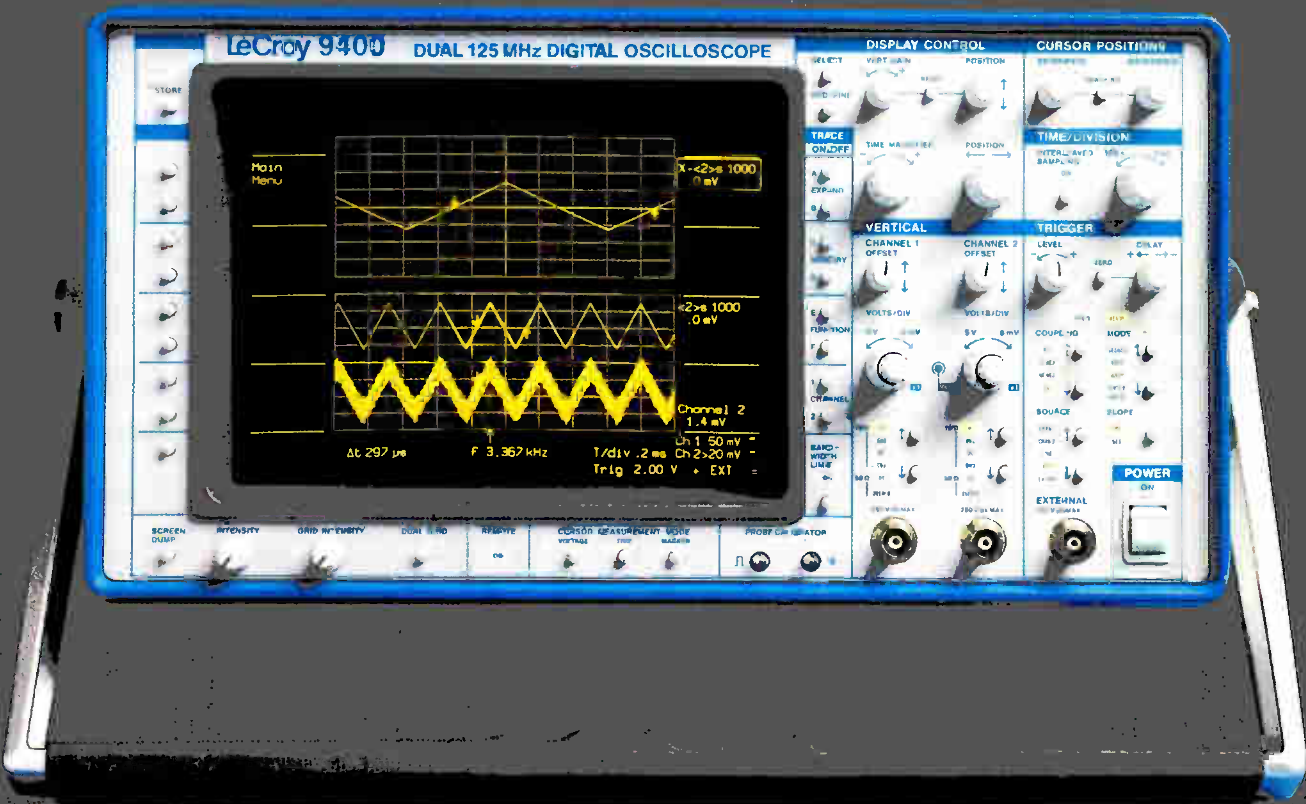
Can the Americans still avoid such a showdown? Maybe, but it would take an all-out effort by America's top companies, one they have shown little inclination to mount. Most of the U. S. equipment giants are not on board a major industry shift that's well under way. "By the year 2000, you won't even recognize the world semiconductor industry," predicts veteran industry-watcher Jack Beedle. "It will be made up of gigantic conglomerates."

Few observers expect these vertically integrated giants to be American. In 10 years, only two of the top 10 chip producers will be American—IBM and Texas Instruments— predicts Richard Skinner, president of Integrated Circuit Engineering. He expects six of the top 10 to be Japanese companies, one to be Korean, and one West German.

The real question is, why aren't the giant U. S. equipment makers staking out a long-term position in an industry that is so vital to their future product development? Where has General Electric Co. been? And why aren't Ford or Boeing investing in chip making? Amazingly, U. S. giants may be moving in just the opposite direction. Although GE isn't talking, observers say it is trying hard to get out of the chip business. Says ICE's Skinner: "I can't understand why GE would want to sell; they're going in the wrong direction."

To Skinner and others, the big U. S. equipment makers could have matched the semiconductor moves of their Japanese counterparts. "Either GE or RCA could have done the same thing by themselves," he says. "They could have followed a more highly integrated merchant semiconductor activity by tying in the development of semiconductors with the development of new products in other areas. Both of them have large enough requirements that could have supported rather large captive semiconductor operations," he adds. But they followed the typical American strategy of trying to keep the semiconductor units responsible for their own P&Ls, he says, a habit most U. S. companies will find difficult to break.

ROBERT W. HENKEL



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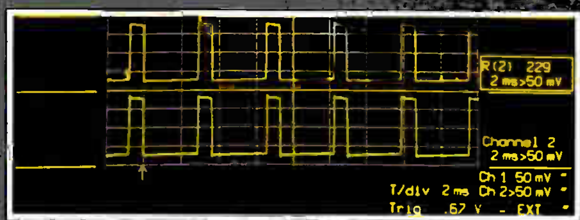

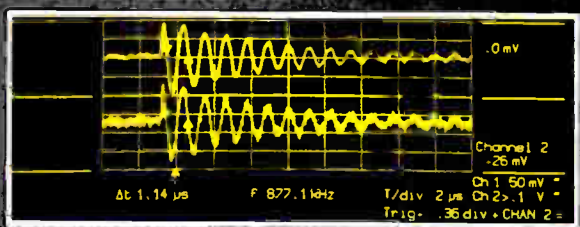

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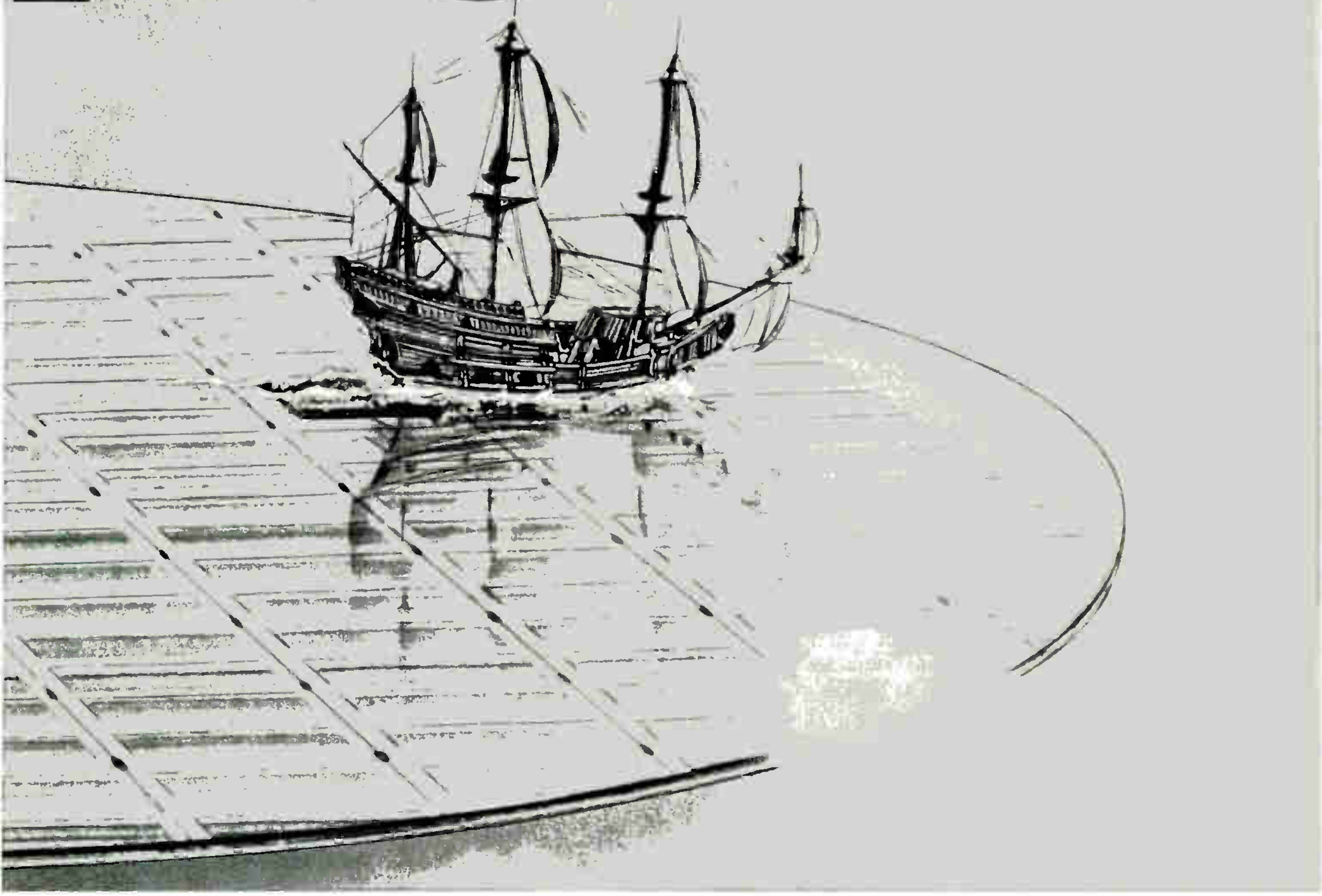

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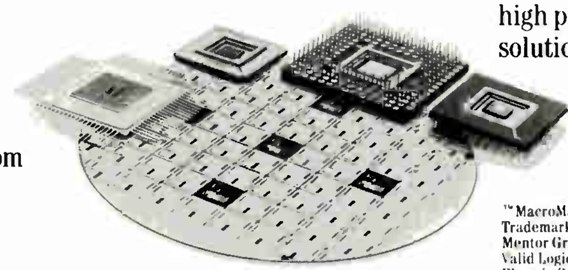

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Circle 11 on reader service card

More on ACL pinouts

To the editor: I have read with interest the articles debating the virtues of changing pin configurations on advanced CMOS logic packages. Another solution exists. Why not develop a new DIP that includes a chip capacitor under the die? Manufacturers could determine the appropriate value for each type of chip and mount it to allow standard bonding to the die during assembly. This would favor the use of end pins for power rather than fast-moving signals (since the lead inductance still exists, even with the new pinout).

Costs might rise somewhat, but they would be cancelled by the fact that fewer—if any—board-mounted decoupling caps would be needed. It also seems that only DIPs need this kind of treatment and are the only packages crying out to maintain the older pinout. Small-outline packages and surface-mount devices exhibit much less of a problem with end-lead inductance and in general represent a far smaller population in existing designs.

Lee Hardesty
Scott Instruments
Denton, Texas

Who's on top?

Correction: In the profile that accompanied our story "This smart power chip breaks the 100-V barrier," [*Electronics*, Oct. 2, 1986, p. 89], Ixys Corp.'s Nathan Zommer was incorrectly identified as the company's president. He is executive vice president and chief technical officer; Howard Hofstein is president.

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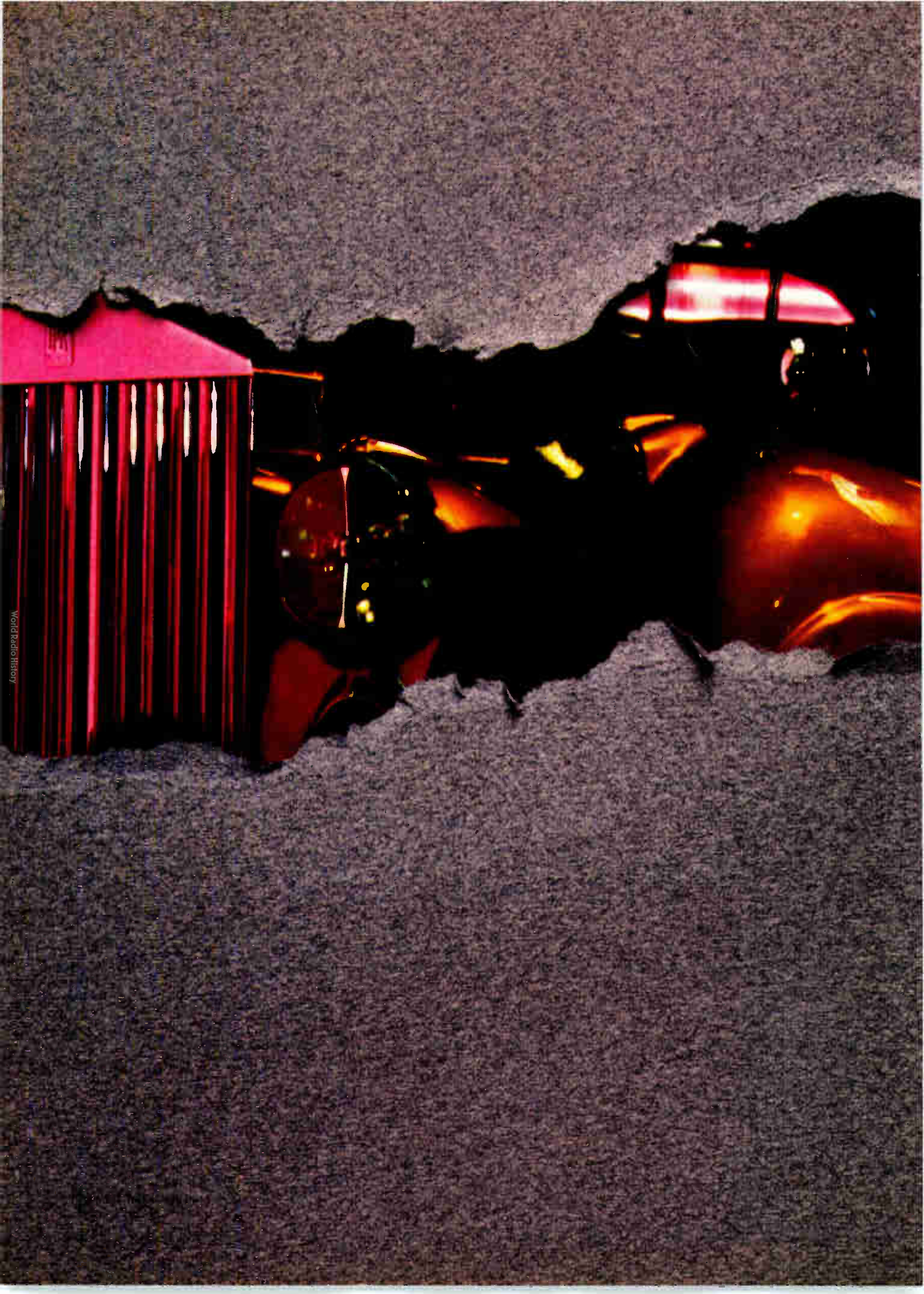

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PEOPLE

POPOVICH STEERS 'BIGGEST PILOT LINE IN THE U.S.'

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Life for George J. Popovich Jr. has been anything but slow-moving since he went to work at Inmos Corp. last April. Only two months after joining the chip maker as vice president of sales, Popovich took over the marketing operation and was named senior U.S. officer of the Colorado Springs operation by Inmos's British parent, Thorn EMI Ltd.

But that wasn't all. One month later, in July, Inmos consolidated its manufacturing, moving volume memory production across the Atlantic to its plant in Newport, Wales. This left Popovich's Cheyenne Mountain fabrication facility—with its total workforce cut from 800 to 450—to fill a new role as a kind of super pilot line for future products and 1-μm CMOS technologies. The plan calls for new products to be transferred to Wales from Colorado after processes are fine-tuned.

The changes mean that the biggest challenge is still ahead for Inmos. The company had served as the U.S. production arm of the Thorn EMI subsidary, Inmos International plc; now, says Popovich, "You could say we've become the nation's largest pilot line."

Popovich is used to challenges. The 36-year-old native of Pennsylvania started his career in 1974 as a marketing engineer at Texas Instruments Inc. in Dallas after receiving a BSEE from the University of Nebraska. He later moved to New York as a TI sales representative calling on IBM Corp. In early 1977, Intel recruited Popovich away from TI and made him territorial sales manager—for the express purpose of getting more of IBM's business, says Popovich.

Intel promoted him to memory marketing manager in Hillsboro, Ore., and then last year Popovich decided to join Lattice Semiconductor Corp. in nearby Beaverton. His stint as marketing director lasted only two months. He is philosophical about the experience. "Sometimes you can find out only so much about another company on the outside, and it's not until you are inside that you realize you are heading one way and the company is going another," he says.

Now, Popovich is directing the U.S. Inmos operation in its new role, which calls for it to help lead Inmos' research and product development. This means that, although overall employment is down from a year ago, R&D staffing in Colorado Springs will eventually increase by up to 15%, Popovich says.

In addition, he still has responsibility for U.S. marketing—a high priority, since 75% of Inmos' sales are in the U.S. Marketing personnel will also be added, as Inmos adds new products.

Beside adding staff in key areas, Inmos will be enhancing its facilities, too. "We are installing several millions of dollars of equipment between now and year's end. We are adding class 10 clean-room space, as well as bringing in new photolithographic equipment," Popovich says.

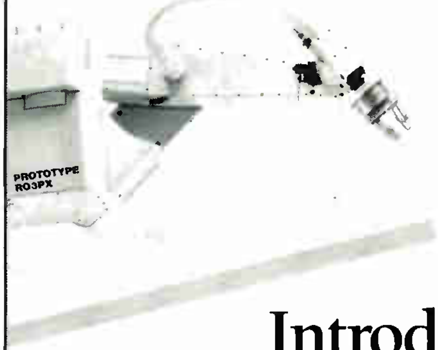
One of the first tasks for the additional staff and the new equipment will be to bring up Process 86, Inmos' 1-μm CMOS technology aimed initially at making very fast static random-access memories. The double-level-metal process is

POPOVICH: His latest challenge is converting Inmos's Colorado facility into a super pilot line.

now being applied to a new line of 256-K and 64-K SRAMs with access speeds of 25 ns. Process 86 will also be applied to transputer products slated for introduction next year. Already on the drawing boards is what Inmos calls Process 88, a submicron CMOS technology aimed at fast 1-Mb SRAMs.

Popovich emphasizes that the Colorado facility will not only research the new process, it will also produce the SRAMs in volume. "We are seeing more aggressive production schedules here," he says. "Our plant is not a pilot line in the sense that its only charter is dealing with a cerebral mode of R&D. We actually will ramp up production of new products here.

"The issues of doing technology development and product design here and then transferring it to the UK will present a set of challenges. If we are diligent and thorough, we will pull it off without a lot of problems," Popovich says. *–J. Robert Lineback*



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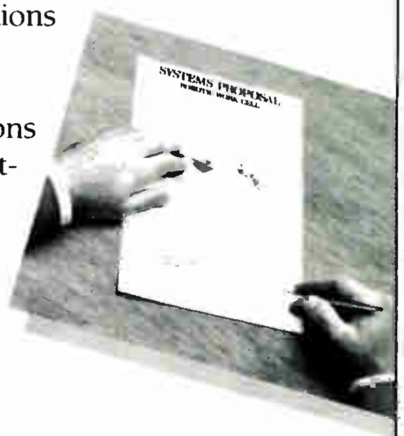

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PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED SORTS AVAILABLE (ns)				PACKAGE OPTIONS
DYNAMIC RAMS									
TMM4164AP	64KX1	NMOS	YES	YES	150	200			P
TMM41256P	256KX1	NMOS	YES	YES	120	150			P/T
TMM41257P	256KX1	NMOS	YES	YES	120	150			P/T
TMM41464P	64KX4	NMOS	YES	YES	120	150			P
TC511000P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC511001P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC511002P/J	1MbX1	CMOS	YES	2Q'86	100	120			P/J
TC514256P/J	256KX4	CMOS	YES	2Q'86	100	120			P/J
TC514258P/J	256KX4	CMOS	YES	2Q'86	100	120			P/J
STATIC RAMS									
TMM2114AP	1KX4	NMOS	YES	YES	120	150			P
TMM2016AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2016BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2064P	8KX8	NMOS	YES	YES	100	120	150		P
TMM2063P	8KX8	NMOS	YES	YES	100	120	150		P
TC5504AP	4KX1	CMOS	YES	YES	200	300			P
TC5514AP	1KX4	CMOS	YES	YES	200	300			P
TC5516/17AP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18BP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18CP	2KX8	CMOS	YES	YES	150	200			PFY
TC5565P	8KX8	*CMOS	YES	YES	120	150			PFY
TC5565AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5563AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5564P	8KX8	CMOS	YES	YES	150	200			PY
TC55257P	32KX8	*CMOS	YES	YES	100	120	150		P
HIGH SPEED STATIC RAMS									
TMM2018D	2KX8	NMOS	YES	YES	35	45	55		D
TMM2068D	4KX4	NMOS	YES	YES	35	45	55		D
TMM2078D	4KX4	NMOS	YES	YES	35	45	55		D
TC5561P	64KX1	*CMOS	YES	YES	70				P
TC5562P	64KX1	*CMOS	YES	YES	45	55			P
EPROMS									
TMM2764D	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764DI	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764AD	8KX8	NMOS	YES	YES	150	200			D
TMM27128D	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128DI	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128AD	16KX8	NMOS	YES	YES	150	200			D
TMM27256D	32KX8	NMOS	YES	YES	150	200			D
TMM27256DI	32KX8	NMOS	YES	YES	150	200			D
TMM27256AD	32KX8	NMOS	YES	YES	150	200			D
TC57256D	32KX8	CMOS	YES	YES		200	250		D
TMM27512D	64KX8	NMOS	YES	YES		200	250		D
ONE TIME PROGRAMMABLES									
TMM2464AP	8KX8	NMOS	YES	YES	200				PF
TMM24128AP	16KX8	NMOS	YES	YES	200				PF
TMM24256AP	32KX8	NMOS	YES	YES	200				PF
TMM24512P	64KX8	NMOS	2Q'86	2Q'86	250				PF
MASK ROMS									
TC5364/5/6P	8KX8	CMOS	YES	YES	250				P28
TMM23256P	32KX8	NMOS	YES	YES	150				P28
TC53257P	32KX8	CMOS	YES	YES	200				FP28
TC53512P	64KX8	CMOS	YES	2Q'86	200				P28
TC531000P	128KX8	CMOS	YES	YES	200				P28
TC532000P	256KX8	CMOS	YES	2Q'86	200				P32

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ELECTRONICS NEWSLETTER

RESEARCHERS COME UP WITH FASTER MAGNETO-OPTIC RECORDING

Magneto-optic recording systems provide density and read-write capability. But they have been partly stymied because, unlike conventional magnetic recording, they require separate passes to erase and write. Now the process may be speeded significantly by researchers at Carnegie-Mellon University in Pittsburgh who have developed a method to directly write over previous data while it is being erased. The key is to use magneto-optic thin films with a compensation temperature that is a few tens of degrees higher than the ambient temperature—allowing the demagnetizing field to also be used as a bias field for writing. □

MOSTEK STEPS UP ITS EFFORTS IN THE MILITARY DRAM MARKET

One of the companies hit hardest by the 1984-85 price collapse of commercial 64-K dynamic random-access memories is serving notice that it is still alive and kicking in the DRAM market. Mostek—now Thomson Components-Mostek Corp.—is readying a new military-grade fast 256-K DRAM. Once a top world supplier of 16-K chips, Mostek dropped commercial DRAMs after being sold to Thomson-CSF of France by United Technologies Corp. a year ago. However, the Carrollton, Texas, MOS maker quietly stayed in the military DRAM business, shipping its Joint Army-Navy-qualified MKB4564 64-K and 4116 16-K chips. Now, Mostek is preparing to introduce a new 1.5-μm n-channel 256-K-by-1-bit DRAM, the MKB/J45F56, which will have access speeds as low as 100 ns. □

PARALLEL-PROCESSING STARTUP WILL TAKE ON THE BIG PLAYERS

A tiny Manhattan startup, hoping to enter the big leagues of parallel computing alongside the likes of Intel, Thinking Machines Inc., and BBN Advanced Computers, is racing to complete its first product by the end of the year and deliver it in the first quarter. The Fifth Generation Computer Corp. plans a computer based on the massively parallel-processing architecture, called Dado, developed at Columbia University. The computer, also called Dado, will use Motorola 32-bit 68020 microprocessors connected in a binary-tree configuration. That configuration means that Dado is well-suited for applications such as speech recognition, acoustic signal identification, relational data-base operations, general pattern matching, and two- and three-dimensional graphics, the company says. Unlike other parallel computers that run as stand-alone units, Dado is designed as an accelerator. It attaches to a general-purpose computer or work station that acts as controller, allowing Dado to devote itself to parallel computing. A typical Dado, with 16, 32, or 64 processors, attachable to a Sun work station, will cost $90,000 for about 1.8 mips per processor. □

SURPRISE! CHIEF EXECS ARE HEAVY PERSONAL COMPUTER USERS

A study of how 113 senior executives and middle managers of U. S. corporations use personal computers concludes that, contrary to conventional wisdom, senior and chief executives actually use their machines quite heavily—on the average of seven hours a week in one-hour sessions. The study, conducted by the Stanford University Graduate School of Business and sponsored by Epson America Inc., also contradicts the academic precept that senior executives should use computers for decision-making and planning, and middle management should use them primarily for management-control information. Instead, top management's most frequent use is for information on how the company is doing—while middle management, in fact, uses the computers most frequently for decision analysis and planning. □

ELECTRONICS NEWSLETTER

CONVEX AIMS NEW 64-BIT PROCESSOR AT EMBEDDED SUPERCOMPUTING

Not all of the new minisupercomputers from Convex Computer Corp. were announced last month when the firm introduced its second-generation C1 XP and low-cost C1 XL models [*Electronics*, Oct. 30, 1986, p. 56]. A third, smaller minisuper is for system integrators who want to embed 64-bit processing power into their own equipment. Convex will announce this model, the XE, in the first quarter of next year. The XE contains the core of the $350,000 XL and costs $19,000 in quantities. It repacks the CMOS system so it can slip into a 19-in. rack with its own power supplies, boot-up disk, Multibus card cage, and up to 64 megabytes of system memory. A key application for the XE could be computer-aided design and manufacturing systems, which can use the 64-bit processor as a powerful engine for graphics. Convex believes the XE's price and size could make it the first supercomputer to see action aboard ships and in seismic-search vehicles. □

ENTRY-LEVEL VERSION OF 7-GIGAFLOPS SUPERCOMPUTER IS COMING . . .

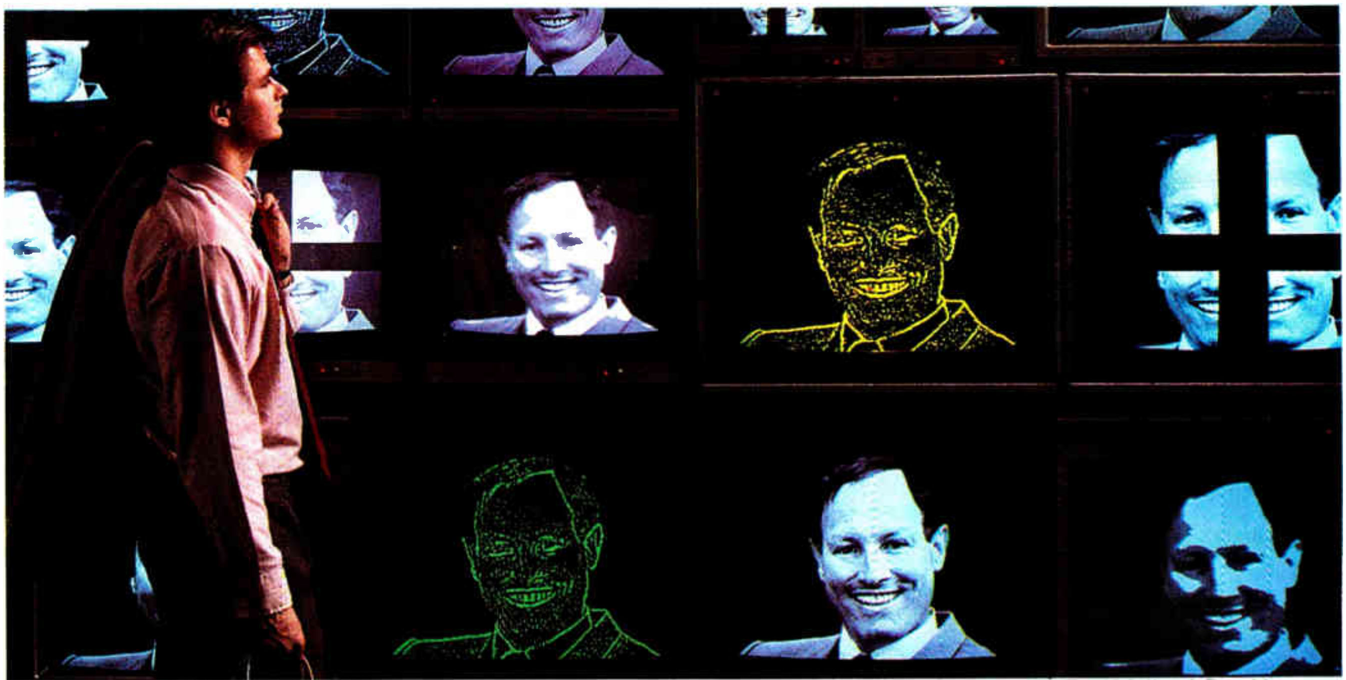
Potential users who want to get into supercomputing, but don't think they need to pay for the full 7-gigaflops power of ETA Systems Inc.'s forthcoming ETA^{10} supercomputer, may soon have a way to do it. The St. Paul, Minn., company is working on an entry-level model known internally as the Piper, which reportedly will use slower, air-cooled single- and dual-processor versions of the full model's liquid-nitrogen-cooled, CMOS-based single-board processors. ETA officials say they haven't yet fully defined the Piper product strategy, but the machine could be introduced as soon as next year's first half. The Piper could still pack a lot of wallop: each processor board is about equal in power to a Cyber 205 supercomputer. Its price also would start at $1 million, versus the $6 million to $25 million of the full ETA^{10}. □

. . . AS ETA SIGNS PERFORMANCE SYSTEMS AS SECOND SOURCE FOR GATES

ETA Systems Inc.'s future customers can take comfort in the fact that the firm has finally nailed down an alternate source for the 20,000-gate CMOS array chips, supplied by Honeywell Inc., that will be the heart of the ETA^{10} supercomputer [*Electronics*, May 26, 1986, p. 33]. ETA is preparing to deliver tapes for mask generation before year end to Performance Semiconductor Corp. in Sunnyvale, Calif., which will take on the second-source task. ETA officials expect Performance to make its first deliveries late in next year's first quarter and to begin small-volume production by the third quarter. But Performance will need until mid-1988 to develop and produce all 92 options of the array to be used in the ETA^{10}. In the meantime, the supply of high-quality, working packaged chips from Honeywell improved dramatically in October, when "we received more devices alone than we did during the first nine months of the year," says an ETA source. □

DEC SPREADS CLUSTERING DOWN TO MICROVAX II AND VAXSTATION II

Digital Equipment Corp. is extending its VAXcluster multiprocessing capability down to its low-end MicroVAX II and VAXstation II. To be available next month, the software, Local Area VAXcluster, will allow work stations to function in a tight computer environment with centralized system management and transparent file sharing. In such an environment, what is called dynamic load balancing lets individual work stations draw upon the computing power of other stations in the system for processing tasks. The Maynard, Mass., company also announced several new VAXstation II and MicroVAX II configurations—including diskless models—to run the Local Area VAXcluster software. □



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DT2803 Low Cost Frame Grabber	IBM PC, PC XT, PC AT	256x256	64	Yes	Yes		8*	Yes	Yes	1 buffer 256x256x8 (64 Kbytes)					VIDEOLAB PC SEMPER	$1495
DT2851 + DT2858 High Resolution Frame Grabber and Auxiliary Frame Processor	IBM PC AT	512x512	256			Yes	8*			2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2851 $2995 DT2858 $1695
DT2603 Low Cost Frame Grabber	MicroVAX II	256x256	64				4			1 buffer 256x256x8 (64 Kbytes)					DT-IRIS	$1895
DT2651 + DT2658 High Resolution Frame Grabber and Auxiliary Frame Processor	MicroVAX II	512x512	256	↓	↓	Yes	4	↓	↓	2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2651 $2995 DT2658 $1895

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PRODUCTS NEWSLETTER

TI CHIP SET PROMISES A 1,200-BAUD PRICE FOR 2,400-BAUD MODEMS

Texas Instruments Inc. is teaming its powerful 32-bit digital signal processor and 8-bit TMS7042 microcontroller to lower the cost of 2,400-bit/s modems to the level of today's 1,200-b/s modems. TI's ROM-coded TMS32011 signal processor contains a dual-channel serial port that attaches directly to codecs. TI's Houston operation says customers will be able to build 2,400-b/s modems for $50 each, including the chip set, a codec, interface, and glue logic. The chip set will cost about $25 in quantities of 25,000. A prototyping kit is being introduced at this week's Comdex/Fall show for $995. ☐

SOLID-INK PRINTER RIVALS LASER JETS, DAISYWHEELS IN OUTPUT QUALITY

An innovative solid-ink process will make possible a printer that Dataproducts Corp. claims will produce better-quality output than laser and daisywheel machines. The SI 480 also runs at speeds four times faster than the daisywheels, says the Woodland Hills, Calif., company. In the printer, a solid pellet is melted, and the molten ink is fired through tiny nozzles to the media, where it then hardens. The SI 480 prints on any media. Its speed of 200 characters per second at 480-dots/in. horizontal resolution puts it into the midrange of letter-quality office printers. Dataproducts will start quantity deliveries to original-equipment manufacturers in the first quarter of 1987. Price for the basic unit is $2,795 and includes an automatic sheet feeder, tractors, two character fonts, and two interfaces. ☐

FERRANTI ASIC DESIGN TOOLS HANDLE ANALOG-DIGITAL COMBOS

Software tools for layout and design of combined analog and digital application-specific integrated circuits from West Germany's Ferranti GmbH run on IBM Personal Computer ATs and XTs using FutureNet Corp. schematic-capture software and MicroSim Corp. PSpice. Ferranti's Digilin library of uncommitted logic arrays includes more than 30 linear macrocells, and users can design custom macrocells having as many as 140 transistors. The company estimates four to six weeks from verified design to supply of samples. The Digilin software library, a design manual, a CAD support manual, and a two-day training course will be available in the U. S. in January from Ferranti subsidiary Interdesign Inc., Scotts Valley, Calif., for about $1,500. ☐

SIEMENS ARRAYS PROMISE FASTER, SMALLER MAINFRAMES

A new family of gate arrays from Siemens AG will make central processing units of large mainframes smaller and faster. The West German company's SH100E is a bipolar device that packs 9,000 gate functions—60,000 elements—on 145-mm^2 chips. The emitter-coupled-logic array features a gate delay of 200 ps. It comes in a tape-automated-bonding package with 320 pins. The arrays are being introduced at this week's Electronica show in Munich. Prices have not been announced yet. ☐

LOW-COST CAMERA CONVERTS PHOTOS TO PC IMAGES

Users of CAD and PC-based graphics systems can convert photographs into high-resolution computer images with a $1,200 camera from Julie Research Laboratories Inc., New York. The C850 uses an external color wheel to capture images in a three-step red-blue-green procedure. The camera provides high contrast and color resolution of 512 lines. Software running on an IBM Personal Computer XT, AT, or compatible machine synthesizes color components into an accurate image with hues matching the original. The camera is compatible with a wide variety of video-frame-grabber boards. ☐

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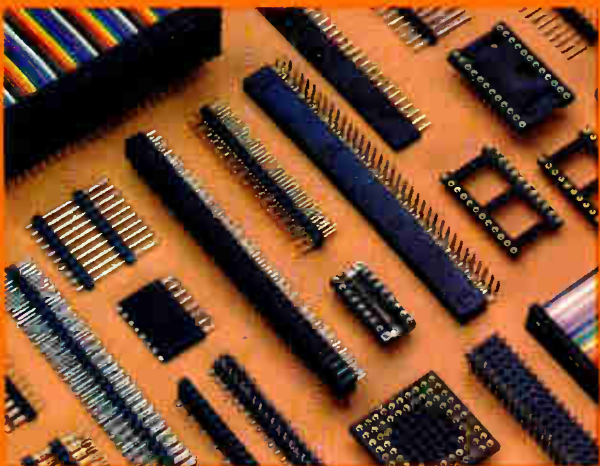

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Company "E"	Medical Instrumentation	100%
Company "F"	Computers	Zero Defects
Company "G"	Telecommunications	100%
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Company "J"	Medical Instrumentation	100%
Company "K"	Heart Pacemakers	Excellent

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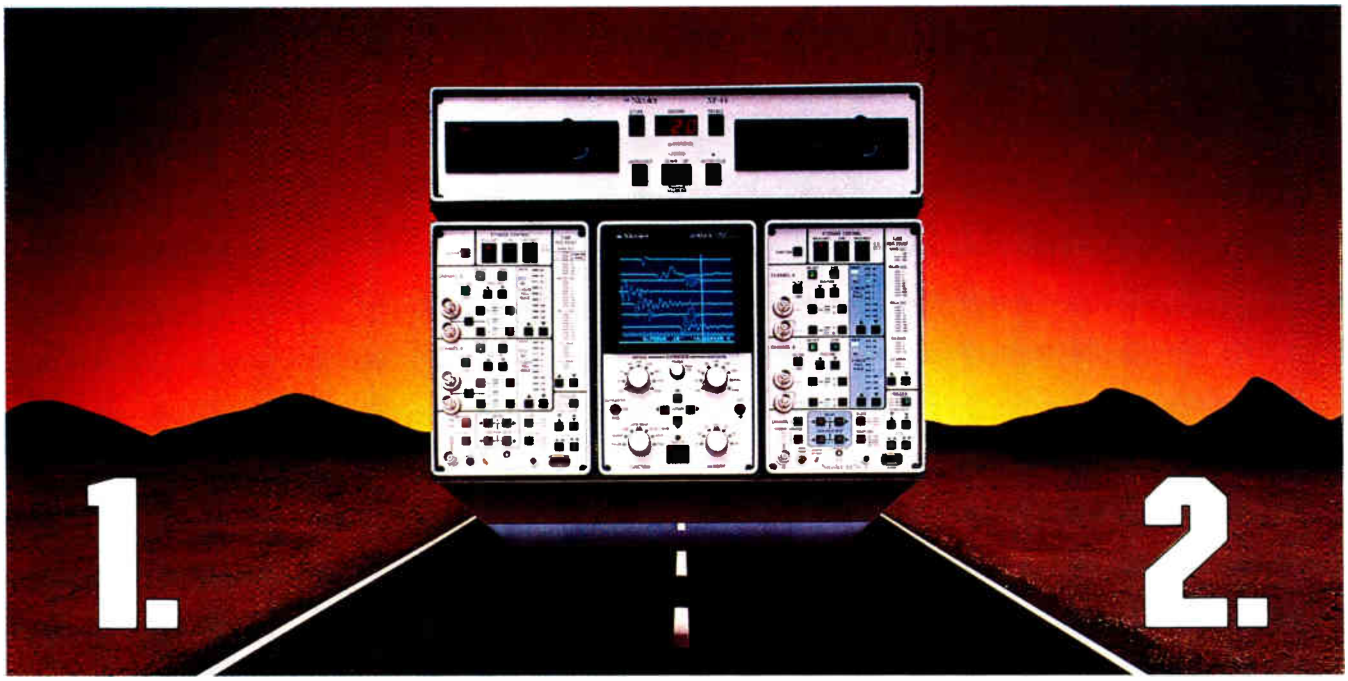
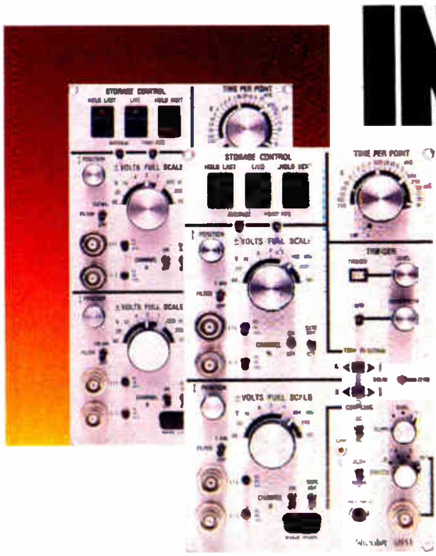


TWO DIGITAL SCOPES IN ONE.



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Electronics

IS THE FAIRCHILD-FUJITSU DEAL A VISION OF THE FUTURE?

VERTICALLY INTEGRATED GIANTS COULD DOMINATE WORLD MARKETS

NEW YORK

It's been 18 months since Silicon Valley was first struck by an economic earthquake that left the U. S. chip business in a shambles, and the aftershocks aren't over yet. The latest jolt came late last month when Fujitsu Ltd. agreed to buy an 80% stake in Fairchild Semiconductor Corp. from Schlumberger Ltd., thereby leaping into the elite class of the world's five biggest chip makers.

The deal—hailed by analysts as a match made in heaven, even as the military, leading chip makers, and the Semiconductor Industry Association howled with discontent—could mark the start of a whole new era in the U. S. semiconductor industry: the age of the giant chip makers. The prospect of those giants being overseas is particularly disturbing to the Pentagon.

Further fueling the uproar are reports that General Electric Co. is ready to sell off its merchant semiconductor businesses (see p. 30). And analysts say others may also be seeking financially strong buyers who can help with expensive capital investments. Together, these factors indicate that the Fujitsu-Fairchild deal is not an isolated incident.

CHEAP DOLLARS. Behind the changes in the industry are such related causes as the recent semiconductor trade agreement with Japan, depressed market conditions, overcapacity, and an evolving global market for semiconductors, analysts say. The driving force, however, may well be the sliding U. S. dollar.

The dollar was weakened to make U. S. goods more attractive overseas. But the cheap dollar has also made the companies that produce those goods highly attractive for foreign takeover. That worries U. S. chip makers, especially Texas Instruments Inc. "While some consolidation in the industry is inevitable," the Dallas-based company said in a statement on the Fairchild sale, "it is disturbing that Japanese companies with cheap capital can buy U. S. market position and products at low prices."

The semiconductor trade agreement may also have played a part in Fujitsu's purchase of Fairchild. Fujitsu now joins NEC Corp. as the only Japanese powerhouses with firm U. S. beachheads, meaning they can make chips here as domestic suppliers, whose prices are not regulated by the agreement. That and the possibility that other Japanese companies may follow worries the SIA, says vice president Warren Davis. "We have to study the matter very carefully," he says.

Not everyone is panicking, however. Some observers regard the Fairchild acquisition as a repeat of events in the 1970s, when, encouraged by the cheap dollar, Schlumberger acquired Fairchild, Philips bought Signetics, and Siemens

HARBINGER. Brooks says there will be more deals like the one he cut with Fujitsu.

picked up some specialty houses and a stake in AMD. But even these observers admit this may well turn out to be a more sizable trend. For their parts, the Japanese chip makers don't seem to think there are that many worthy potential partners in the U. S. A spokesman at Fujitsu headquarters in Tokyo says the company moved quickly because "there are only a limited number of brides available." Toshiba, meanwhile, described Fujitsu's move as "very brave."

One of the major attractions of U. S. chip makers for foreign companies is their well-defined distribution channels. One of the reasons for all the interest in GE/RCA Solid State is its distribution network, says former division vice president Bob Pepper, who now runs a startup called Level One Communications Inc. in Folsom, Calif. A company that could latch onto Solid State's distribution agreements could get instant market opportunities for its own products, he says.

Just who might be interested in buying GE's merchant chip operations, which are worth an estimated $400 million in annual sales, is the topic of much debate. The companies most often mentioned are Toshiba, whose business in discrete components might be compatible with GE/RCA's; Sharp, which had sought to enter the U. S. chip business through a joint venture with RCA Solid State only to see the deal quashed by RCA's merger with GE last winter; and Siemens, the West German giant that has been seeking ways to boost its production capacity on this side of the Atlantic [*Electronics*, June 2, 1986, p. 38].

What these firms all have in common is that they are large, cash-rich, vertically integrated companies with sizable sales in the merchant chip market. That's just the kind of company that will be dominant in the semiconductor business into the next decade, says Richard Skinner, president of Integrated Circuit Engineering, a Scottsdale, Ariz., market research firm. ICE predicts that by 1996 the top 10 chip producers will include only one U. S. merchant firm—TI—plus IBM and six Japanese companies. Siemens will be the lone European entry.

Skinner says the reason for Japanese success is that the parent firms buy chips in-house. Tying chip development to product development in other areas holds costs down, he says, and either GE or RCA could easily have done the same.

Instead, they followed the more typical American strategy of trying to keep the semiconductor units responsible for their own profit margins. "RCA Solid State and GE Semiconductor were both equal in stature with TI or Motorola when it came to doing business with RCA's Commercial Electronics Division," he says. "But if they bought only from within, GE and RCA both would have large enough requirements that they could have supported rather large captive semiconductor operations."

That's what IBM does, and now the company's semiconductor operations are the largest in the world. Rumors persist in Japan that IBM could may make a push into the merchant market with its 1-Mb dynamic random-access memories, but Big Blue dismisses the talk as "pure speculation."

Fairchild president Don Brooks says there will be a lot more deals like the one he pushed for with Fujitsu. Japan and Korea, he says, have built semiconductor capacity around well-defined commodity products that are manufactured in high volume. But after two years of over-investment, they're finding themselves with excess capacity—even as the industry is beginning to change from commodity products to application- and user-specific ICs.

The results have been trade friction, price deterioration, and unprofitablity in the U.S., Japan, and Korea. Now the Japanese are trying to get closer to the customers they serve. There are two ways to enter the U.S. markets: build a U.S. facility, as NEC has done in Roseville, Calif.; or invest in equity, as Daewoo of Korea did in Zymos Corp. Fairchild says 50 U.S.-Japanese alliances were made in 1985, up from 20 in 1984.

Meanwhile, in Washington, the departments of Justice, Commerce, and—most important—Defense are studying the Fujitsu-Fairchild deal very closely. Defense Secretary Caspar Weinberger is especially concerned with "foreign dependency," says Arney Stensrud, a member of the Defense Science Board and director of strategic marketing and government relations for Motorola Inc.'s Semiconductor Products Sector. This concern does not address manufacturing issues or the availability of devices themselves, he says, but rather the transfer of technology offshore into unsafe hands. When U.S. firms cooperate with foreign outfits, he says, "the know-how slowly leaks away." A top source at a leading defense electronics firm points out, however, that the supply of ICs is not in jeopardy. U.S. defense suppliers are already buying critical parts from foreign sources.

According to figures supplied by ICE, Fairchild is the No. 2 military chip supplier with $150 million in sales—right on the tail of TI and a step ahead of No. 3 Harris Corp. Fujitsu and Fairchild are not about to let their military business shrink away. Shortly after the agreement was announced, Brooks went to Washington to assure government officials of his and Fujitsu's good intentions. He says the discussions were held at his request, and disputes reports that he was summoned to Washington. "I wanted to make sure they were clear on what we wanted to do," says Brooks, who won't say exactly whom he talked with in Washington. "Military sales are a big part of our business. After the merger, we will bring more, not less to that market."

Motorola's Stensrud says Fujitsu will push hard to maintain and even expand Fairchild's military business. He calls the acquisition "bad news for the military IC industry. It says the Japanese are capable of participating in the market."

From Fairchild's point of view, though, it will now have more, not less U.S. control. Neither the company's present owner, Schlumberger Ltd., nor any of its top management hails from the U.S. After the purchase, Fairchild will be a public U.S. company with two major shareholders: Fujitsu and Schlumberger. *–Tobias Naegele, Clifford Barney, and Larry Waller*

GE LIKELY TO SELL ALL CHIP LINES BUT ASICs AND SOS

Neither General Electric Co. nor officials at the GE/RCA Solid State Division is willing to comment, but talk is swirling about the industry that GE is unloading its merchant semiconductor operations. Industry observers agree that there is little question that the businesses are up for sale.

GE reportedly is seeking about $400 million for the package, which is made up of GE/RCA Solid State and the Intersil subsidiary, plus GE's power business. GE is keeping several product lines that it considers strategically essential—its application-specific chips and some military lines such as RCA's silicon-on-sapphire CMOS technology.

In 1985, RCA Solid State had $341 million in sales, while GE's Semiconductor Business Division accounted for about $295 million, according to figures supplied by Dan Hutcheson of VLSI Research Inc., a San Jose, Calif., market-research firm. About $140 million of RCA's sales were in its highly regarded CMOS, a technology in which the company was a pioneer. Discretes accounted for about $101 million, and linear devices brought in about $92 million.

Most of GE's commercial operations are nestled in Intersil's line of discrete components and MOS chips. In 1985, GE sold about $125 million in MOS parts and about $112 million in discretes. Linear devices accounted for about $41 million.

High-reliability military devices account for about 23% of the division's sales, says Carl Turner, who ran Solid State before the merger and is now responsible for the operations that GE is selling.

He adds that about one quarter of his military business is in radiation-hardened SOS devices. But GE almost certainly won't let that technology go; SOS is ideal for space applications, a business in which GE is heavily involved. *–T. N.*

SEMICONDUCTORS

SIEMENS JOINS THE 1-Mb DRAM CLUB

MUNICH

Siemens AG is about to take its first big step in an all-out drive to propel itself into what the West German giant calls the "mega era" of the semiconductor industry. Lagging only major Japanese suppliers, Siemens next March will start sampling a 1-Mb dynamic random-access memory to its customers.

The big chip is just the beginning. New facilities that will come on line next year, such as a new mask center, a process line for high-speed bipolar devices, and a design center for application- and customer-specific CMOS circuits, will contribute greatly to Siemens' drive. Coupling these facilities to the West German company's experience as a systems manufacturer will add greatly to Siemens' clout in the European semiconductor markets, predicts Peter Savage, associate director and a components market watcher at Dataquest UK Ltd. in London. "They should also give the company a good chance to become a major player on world markets."

The Munich company's efforts in 1- and 4-Mb DRAMs are part of the Mega project, which Siemens and Philips International NV jointly launched in 1984. This $2 billion endeavor, partly financed by the Dutch and West German governments, envisions 4-Mb Siemens DRAMs by 1989 and 1-Mb Philips static random-access memories also by 1989. The company is one of three European manufacturers that, under the Joint European Silicon Submicron Initiative [*Electronics*, Oct. 30, 1986, p. 48], want to set up a common research institute for developing a 0.3-μm technology. Philips of the Netherlands and the Thomson Group in France are also Jessi partners.

By sampling the 1-Mb DRAMs next spring, "Siemens is right on schedule, although the $270 million project is an unusual *tour de force* even for a company our size," says Hermann Franz, member of the Siemens board of management and president of the $1.15 billion Components Group. The $270 million represents the company's investment in the 1-Mb DRAM facility.

Being on schedule would not have been possible for Siemens, however, without help from Toshiba Corp. Under a technology-exchange agreement with the Japanese company [*Electronics*, July 22, 1985, p. 12], the West German company acquired the mask-fabrication technology necessary for making the devices. That, Franz says, has enabled Siemens to cut the time it had lagged other firms in getting memories to market. In the past, its lag time had been running 2½ years, but with boost from the Japanese, it now is only about half that. And with its 4-Mb devices—which Siemens will make entirely on its own—the company thinks it will pull even with its Far Eastern and U. S. competitors.

To that end, engineers at Siemens's Central Research Laboratories in Munich have tested parts of their 4-Mb DRAMs, which will be made with 0.8-μm lines. Thanks to Jessi, Siemens is even eyeing 0.3-μm, 64-Mb devices.

Produced at Siemens' Regensburg plant, the 1-Mb DRAM uses 1.2-μm CMOS technology. The 1-Mb-by-1-bit DRAM will come with maximum access times of 100 and 120 ns and will draw either 330 or 275 mW. The 54-mm² chip comes in a standard 18-pin dual in-line plastic package, which is the same size used for 16-, 64-, and 256-K memories. Around mid-1987, the 1-Mb DRAM will be available in a surface-mountable package.

Volume production of the 1-Mb DRAMs will be gradually stepped up during 1987. The production line is geared for 6-in. wafers, in contrast to most of the competition, which still works with 5-in. wafers.

About the same time that volume production of 1-Mb DRAMs gets under way, Siemens's mask center and process line for high-speed bipolar logic circuits will come on stream. This facility, in Munich, will concentrate on emitter-coupled-logic arrays with gate delays initially around 200 ps. Another project due to come on line next year is a design center for CMOS ASICs and customer-specific circuits. So by the end of 1987, Siemens should be in a strong position to run with the Japanese and U. S. chip makers in the mega area. *–John Gosch*

OPTOELECTRONICS

GaAs OPTO IC GETS UP TO 200 GATES

BLOOMINGTON, MINN.

Honeywell Inc. has moved optoelectronic computing a step closer to the product stage by demonstrating a gallium arsenide receiver. The circuit integrates a photodetector, preamplifier circuitry, and a digital 1 : 4 demultiplexer, all on the same 2-by-2-mm device. The chip decodes a 1-Gb/s optical input into four parallel 250-Mb/s electrical outputs. The circuit carries about 200 gates and exhibits "a density-speed product about 10 times better than any other [optoelectronic] circuit known to date," Honeywell says.

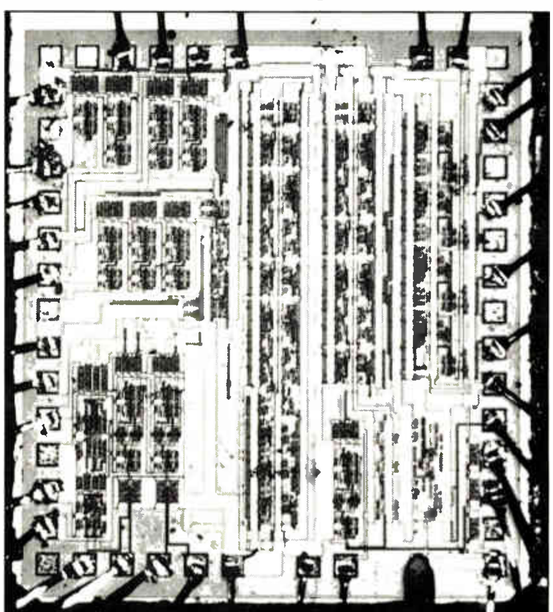
Developed under funding from the Defense Department's Strategic Defense Initiative, the chip is part of a larger DOD effort to push technology for building full-blown monolithic optical transceiver circuits. The idea is to make devices to facilitate direct chip-to-chip communication over high-speed optical fibers. The DOD sees the technique as a way to break the input/output bottleneck that could slow down future systems built with complex, high-speed, I/O-intensive integrated circuits. As part of the push, the Defense Advanced Research Projects Agency has been funding work on optoelectronic interconnection since 1981 at Honeywell and since 1984 at the Rockwell Sciences Center of Rockwell International Corp., in Thousand Oaks, Calif.

Parallel programs at the two companies are aimed at developing true monolithic optoelectronic devices. Funding responsibility for Honeywell's chip effort was transferred to SDI in 1984, but both programs are being managed by Darpa.

The 200-gate Honeywell device breaks new ground in optoelectronic circuit density, says Sankar Ray, a principal research scientist at Honeywell's Physical Sciences Center here. "People have built chips like this before, but only at small-scale-integration levels, like a detector with maybe 10 or 15 gates on the chip." The digital circuits on Honeywell's chip are built with 1-μm ion-implanted metal-semiconductor FET technology.

Rockwell's optoelectronics manager Kevin Kilcoyne says his firm expects to demonstrate a similar GaAs receiver chip in about a month. It will push complexity even further, by integrating an 1 : 8 demultiplexer—about 250 gates.

The receiver technology is only part of the problem. The tougher task is the integration of a laser diode on chip with digital multiplexing circuitry to handle the transmission end of the optical link. Under the DOD program, Honeywell and Rockwell are charged with eventually putting both the photodetector and the laser diode on the same chip. The goal, says John Neff, a program manager in Darpa's defense sciences office, is to get working monolithic GaAs transceiver circuits by late 1988, integrating the laser and the photodetector with their associated multiplexing circuitry. As an interim step, both firms plan to build a monolithic transmit-only chip.



GIGABIT. Honeywell's optoelectronic receiver chip demultiplexes four data streams from a 1-Gb/s optical input.

"The receiver chip is the simpler of the two tasks, because we fabricated the detector right on the GaAs substrate using ion-implantation techniques," Ray says. The transmitter will require use of a more exacting process involving metal-organic chemical-vapor deposition of the epitaxial layers necessary to form the laser diode.

For its part, Honeywell is working with a transverse-junction-strip laser technology. The firm has fabricated a discrete gallium-aluminum-arsenide laser diode on a 3-in. wafer that operates down to a threshold of 32 mA. By contrast, Rockwell is pursuing a multiple-quantum-well laser approach that Darpa's Neff believes holds more potential for reaching the 5-to-10-mA minimum threshold levels that the agency ultimately desires. Rockwell has already demonstrated 22-mA thresholds with its technology, Kilcoyne says.

After a mask modification, Rockwell expects to demonstrate within six months a transmitter chip integrating 8 : 1 multiplexing circuitry, Kilcoyne says. But Ray says that Honeywell will leapfrog to a 16 : 1 multiplexer on its first transmitter chip. What's more, the firm plans to build the transmitter device with enhancement/depletion-mode GaAs technology, which the DOD wants for the final transceivers in late 1988. Although built with a more difficult process, the enhancement/depletion-mode parts will save power.

Ray says Honeywell expects to have its transmitter with a 16 : 1 multiplexer ready in about 12 to 18 months. For the transceiver chip, the firm will integrate 16 : 1/1 : 16 multiplexer/demultiplexer circuitry, Ray says. Rockwell is planning to integrate 8 : 1/1 : 8 circuitry on its first transceiver. *–Wesley R. Iversen*

TECHNOLOGY TRANSFER

MEITEC TO OPEN A WINDOW ON JAPANESE TECHNOLOGY

NAGOYA, JAPAN

A Japanese company, Meitec Corp., is setting up a service that will help U. S. companies gain access to Japanese technology. With the opening next week of its office in Santa Clara, Calif., Meitec will begin providing a number of services for U. S. companies that want to put Japanese know-how to work on the American side of the Pacific; it will also help U. S. companies that want to start operations on the Japanese side.

The services offered by the office will be modest at first: largely translation of Japanese technology papers and some assistance in gaining rights to that technology. From that beginning, Meitec hopes to expand its role as a middleman, making it easier for U. S. companies both to do business in Japan and to make products based on Japanese technology in the U. S.

Meitec's initial services will include translations of information stored by Technomart, a year-old on-line Japanese technology-marketplace service. And Meitec can assist in the negotiations for licensing of technology described in Technomart documents, says Fusaro Sekiguchi, president of Meitec.

Technomart not only stores data on technology but evaluates that technology and attempts to act as a clearinghouse for anyone interested in purchasing rights to it. Technomart's largest data categories cover technology and products for sale. Other items include requests for participants in joint R&D projects and personnel notices.

Data-base access and translations also will be offered for the Patent On-line Information Service, or Patolis, which covers all patents registered in Japan; and a science and technology reference service called JOIS, for JICST (Japan Information Center of Science and Technology) On-line Information System.

Meitec will provide translations from these data bases within 24 hours. It will also translate and format items submitted by U. S. firms for registration in Technomart. The company will be able to provide fast translation services because translators in Japan can work while the U. S. sleeps.

Initially, the U. S. office of Meitec will have two Japanese employees and an American secretary, who will take care of Technomart and data-base input/output and survey the market. Within three years, Sekiguchi expects to have 40 to 50 U. S. employees available for assignments outside the company, an arrangement similar to its operation in Japan, where Meitec provides technically trained staff to both Japanese companies and Japanese branches of American companies. Unlike most agencies that hire out temporary help, Meitec permanently employs the people it loans out. Their assignments last anywhere from six months to several years. Between assignments, they continue to work for Meitec.

In the future, Meitec plans to supply staff members to U. S. companies that want to start subsidiaries in Japan. In return, Meitec expects to get equity interest in the local branch. The arrangement is similar to the deals struck by venture capitalists, except that Meitec's investment consists of personnel instead of cash.

KNOW-HOW. The arrangement will work for both Meitec and its clients, Sekiguchi says, because small and medium-size U. S. companies need people and know-how, not money, when they set out to do business in Japan. Generally, such companies have no idea of how to get started. Nevertheless, he says, it is to their advantage to open an office, rather than relying on trading companies. One reason, he says, is that the prices of products from many U. S. companies represented by traders have not fallen as they should in Japan in response to the much stronger yen.


SEKIGUCHI: His company helps move technology between the U. S. and Japan.

Meitec has about 330 clients in Japan, and almost 3,000 employees, who generated more than $110 million in billings in the latest fiscal year. *–Charles Cohen*

COMPUTER-AIDED DESIGN

SCAN HEAD LETS PLOTTER SERVE AS AN INPUT DEVICE

AUSTIN, TEXAS

The traditional role of pen plotters is being turned the other way around. Plotters, which normally produce line-drawing output under computer control, become image-input peripherals with a new optical-scanner attachment from the Houston Instrument division of Ametek Inc. The scan head, which snaps into the pen holder of Houston Instrument's DMP-50 series of drafting plotters, could open up a new market for low-cost, large-document scanners.

Instead of making marks with pens, the plotter will sweep over paper drawings with the solid-state scanner, digitizing documents up to 36 by 48 in. in size.

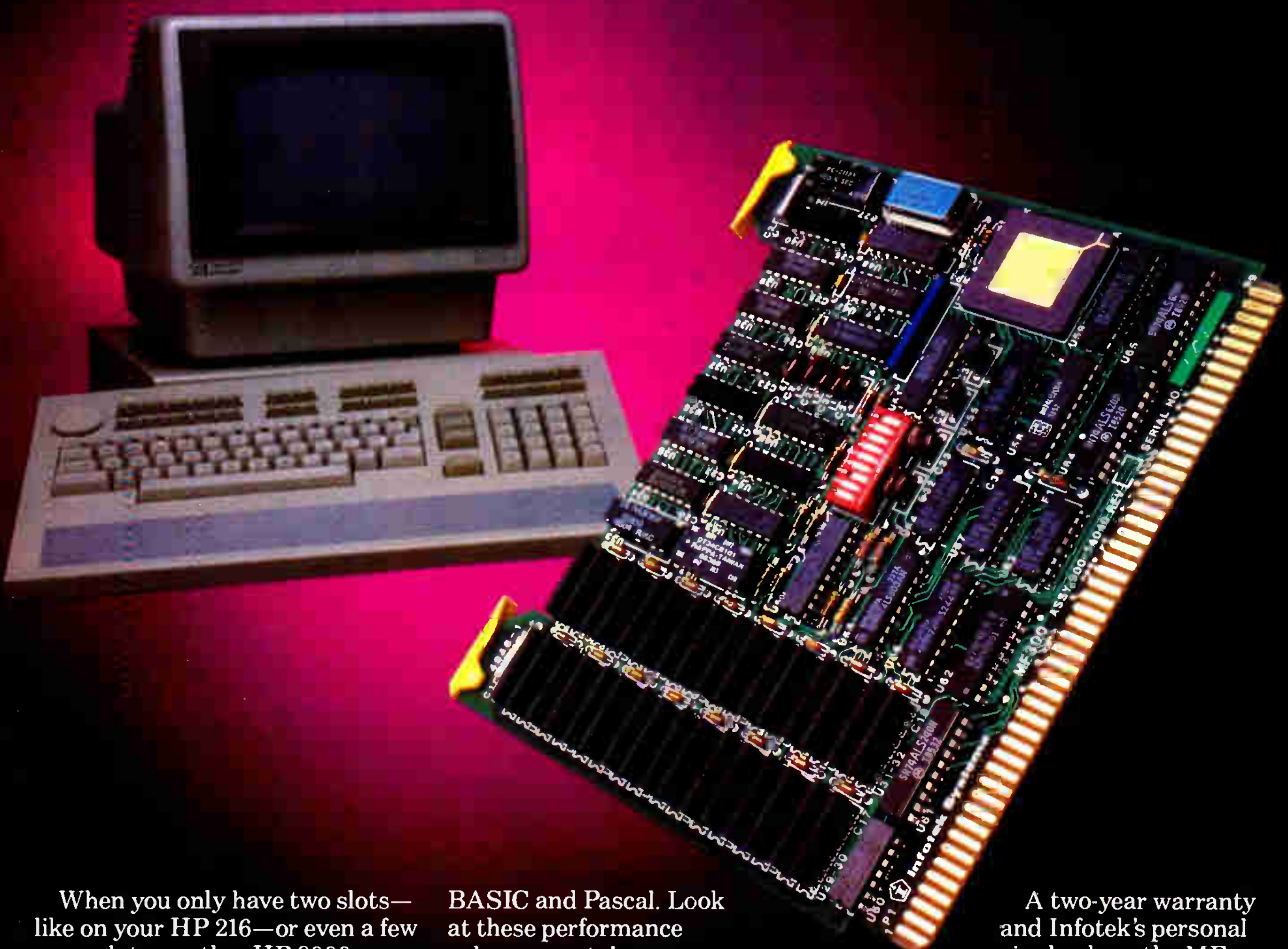
Slated to debut at this week's Comdex/Fall show in Las Vegas, Scan-CAD is being offered as an add-on accessory to the DMP-50 plotter series with a suggested retail price of $2,995. At that price, a fully operational plotter/scanner system will sell for less than $10,000, about a sixth the cost of dedicated large-document scanners.

Sharing mechanical and control components between the plotter and the add-on scanner helps to keep costs low. Movement of the paper and control of the scan head are driven by the same commands used in normal plotting operations.

"Instead of having a plotter and a scanner, you can have one mechanism that serves both functions—using pens

HP LIFE INSURANCE

Now, put up to 4 MBytes memory plus a floating point processor in a single slot of your HP 200/300 computer.



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	310	161	37	4.2
X=SQRT(Y)	216	2,117	38	56
	310	1,333	30	44
X=SIN(Y)	216	4,326	64	68
	310	2,746	50	55

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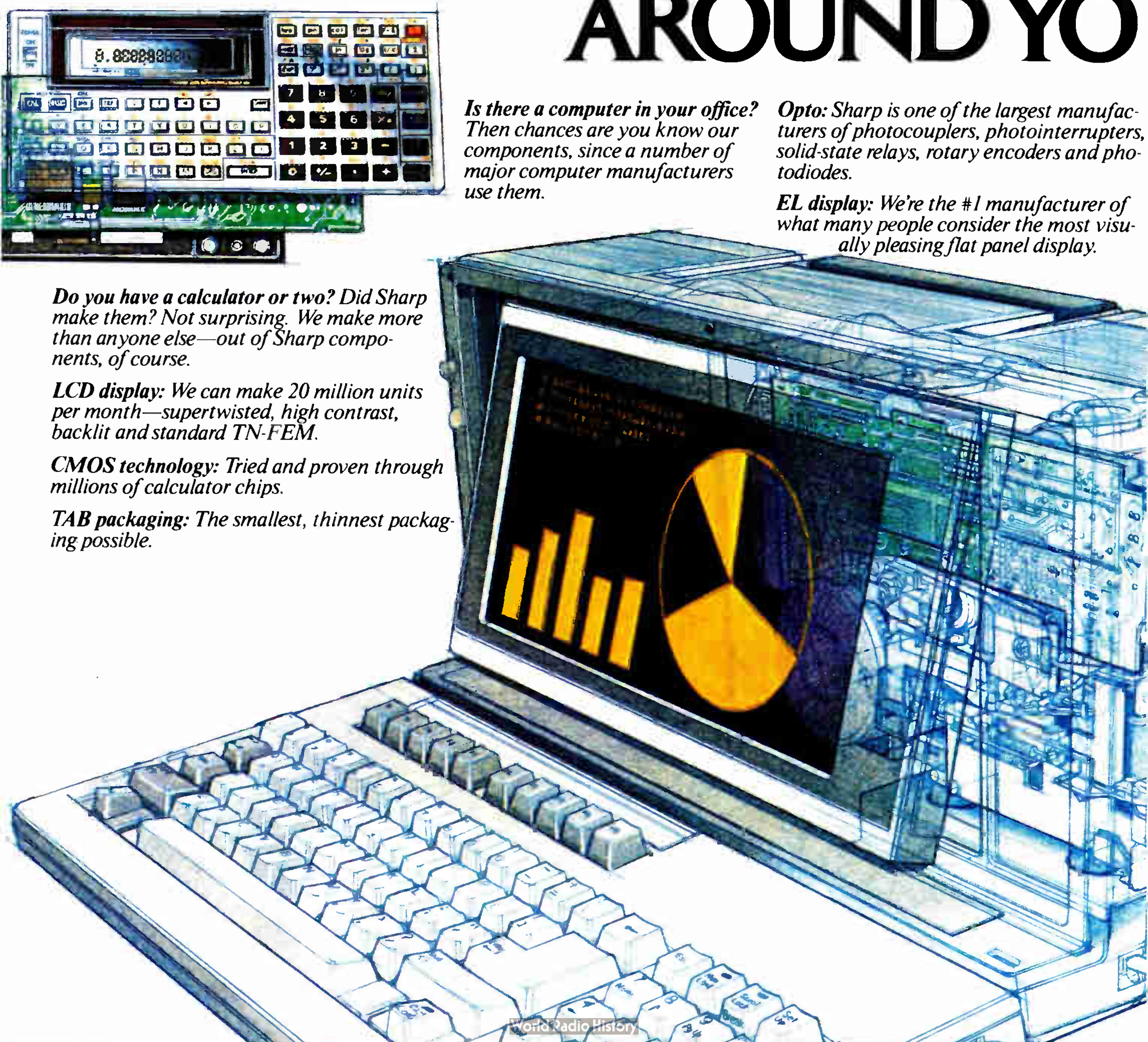

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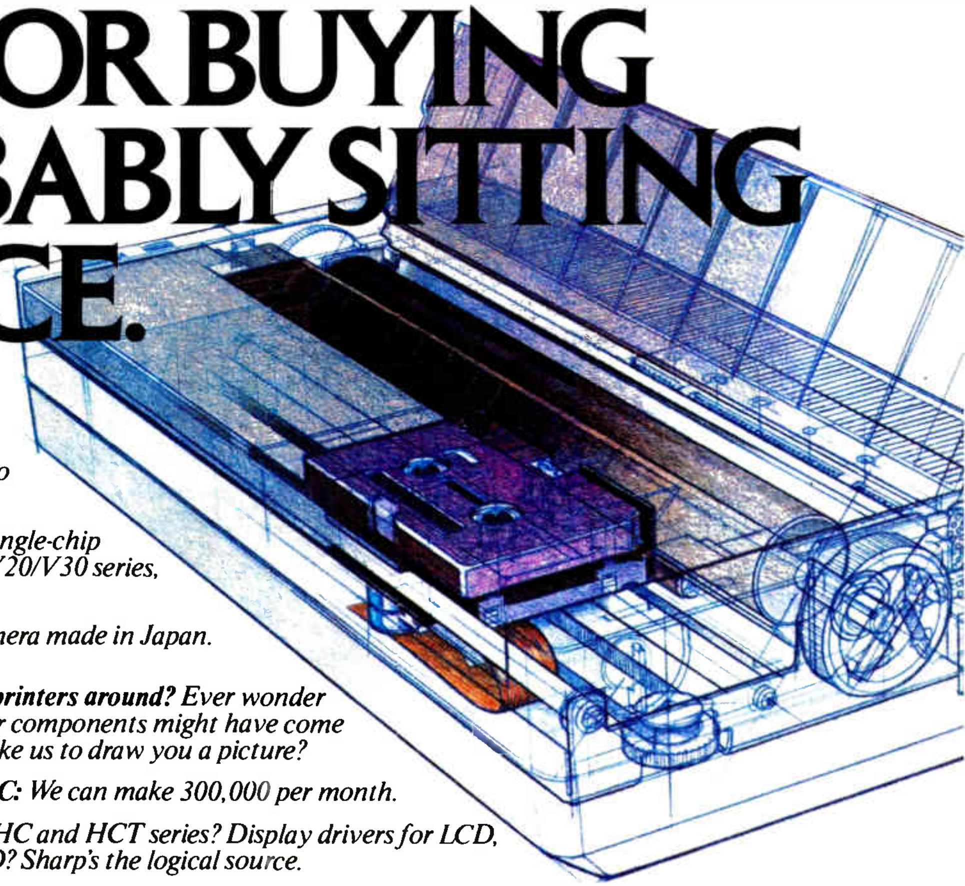

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Circle 35 on reader service card

to draw some of the time, and the scan head the other times," says Brian Plunkett, engineering project leader at Houston Instrument. He notes that some 20,000 DMP-50 plotters have been sold.

Already, the package is drawing the support of computer-aided-design software vendor Autodesk Inc., Sausalito, Calif., which hopes the low-cost system will help propel a price-bound market for large-document scanners. "Normally, the $60,000 price [for dedicated large-document scanners] ends it for the average company. It's even a tough sell to larger companies," says Kevin O'Lone, the product manager for Autodesk's CAD/Camera software. "The price is a major breakthrough. Houston Instrument is the first on the block to do it, and I'm sure once the competition has seen what was done, they will copy it."

Houston Instrument has been trying to gauge the potential size of the market for low-cost large-document scanners, "but no one knows. There have not been any before now," says Eileen Jones, product marketing manager at Houston Instrument.

The company is working with CAD vendors to match raster files to design packages. For example, one version of the Scan-CAD system will generate files in the format used by Autodesk's CAD/Camera program. CAD/Camera converts the raster-image files generated by scanning into the vector format required by Autodesk's AutoCAD software.

EXCLUSIVE. The scan head has been designed to fit only in the pen-holding collar of Houston Instrument's plotters. The scanner also uses Houston Instrument's own control software, preventing Scan-CAD from being used on plotters from rival plotter makers.

The Scan-CAD system requires an IBM-compatible personal-computer host with a minimum of 10 megabytes of hard-disk capacity and 640-K bytes of main memory. The plotter-turned-scanner feeds images back to the PC host, where data is converted from an analog stream to digital raster files at a rate of 1 Mb/s using a plug-in PC card included in the package. Once images are stored in memory, raster files can either be automatically converted to vector form by software or manually traced, using a graphics editor, to ready data for manipulation by CAD packages.

Many high-speed large-document readers scan drawings in a single pass with a long band of imagers. Scan-CAD uses an 8-oz scan head containing a 1-by-128 charge-coupled-device array. Scanning resolution is 200 dots/in., so the system can detect lines as thin as 0.007 in. The plotter's paper-motion and head controllers run the scan head at a speed of 1.2-in.^{2}/s. Each pass of the CCD array captures a 0.6-in. swath. An E-size (36-by-48-in.) drawing can be scanned in 24 min.

The CCD scanner detects images with a 16-level gray scale. A section of memory and logic on the PC card compensates for optical variations in CCD output or imperfections in the scan head's lens or incandescent light source. Digital calibration performed on the fly during scanning enables Houston Instrument to use low-cost components while maintaining acceptable imaging resolution, says Plunkett. *–J. Robert Lineback*

AUTOMATED TEST EQUIPMENT

AUTOMATING OPTICAL-DISK TESTING

TORRANCE, CALIF.

The introduction of an automated tester for optical-disk media opens one of the last doors standing between that technology and its widespread use: mass production of the disks cannot begin without test systems that can detect media flaws reliably and economically. The new system from California Peripherals Corp. may also provide crucial help in setting testing standards for media suppliers, disk-drive makers, and system builders.

Introduced this week at Comdex in Las Vegas, the OMS-500 is an automated system that integrates into a single package all testing elements needed to qualify write-once or magneto-optic erasable disks. It is the first of its kind, say optical-drive experts.

If the reaction of a manager at optical-media supplier 3M Corp. is typical, then the new tester should make quick inroads. "The need is great," observes Roger Hildy, market operations manager for 3M's St. Paul-based optical recording project. He terms the automated testing job "unbelievably important," since each disk must be inspected when his production lines get into full swing next year. Any automated unit must be flexible enough, however, so that original-equipment manufacturers can dial in their own test parameters.

The OMS-500-based system is said to be able to handle this task. It sells for $125,000 for the basic package—more, with options.

California Peripherals has U. S. marketing rights to optical-disk testers manufactured by Nakamichi Corp. of Kodaira, Japan, some 60 of which have been sold since 1984. The Torrance company has raced to develop a system built around Nakamichi's latest, the OMS-500. The full system incorporates the OMS-500, custom software, a personal computer, and such other gear as a spectrum analyzer and a digital-signal generator. It can be used for development work and in the early ramp-up stages of manufacturing; it is not intended for high-volume production lines.

PATHFINDER. Optical-disk test system from California Peripherals could help set testing standards.

Up until now, users of Nakamichi's testers had put together their own test setup with analyzers and signal generators. They had to operate the tester manually and then laboriously compile the results. These installations have all been custom setups with no standard way of going about the job.

California Peripherals has put together a complete computerized test system and has written software for computer-controlled test functions. Among them are tests that determine the carrier-to-noise ratio; media reflectivity; optimum write, read, and erase power; and jitter and dropout characteristics. The system generates charts and graphs of bit-error distributions and other characteristics that the company thinks can be used as standards for test comparisons.

"We feel there's an opportunity to establish standards," both in test procedures and test-data presentation formats, contends Howard Wing, vice president of marketing and sales. Disks now are checked out at several stages: by the disk manufacturer, drive makers, system integrators, and finally by the disk users themselves—all with no

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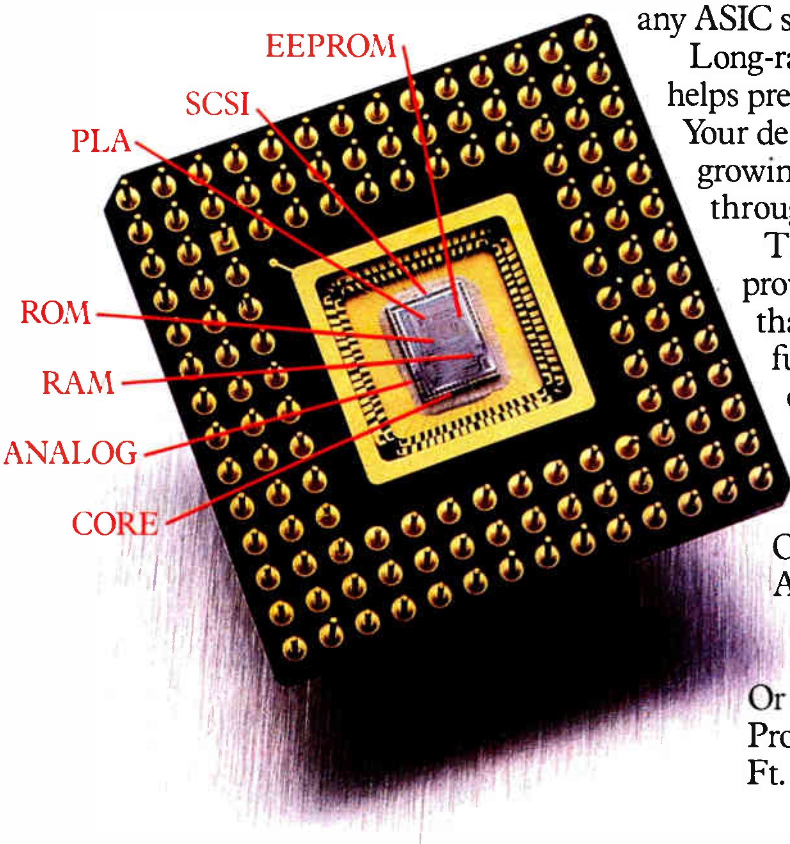

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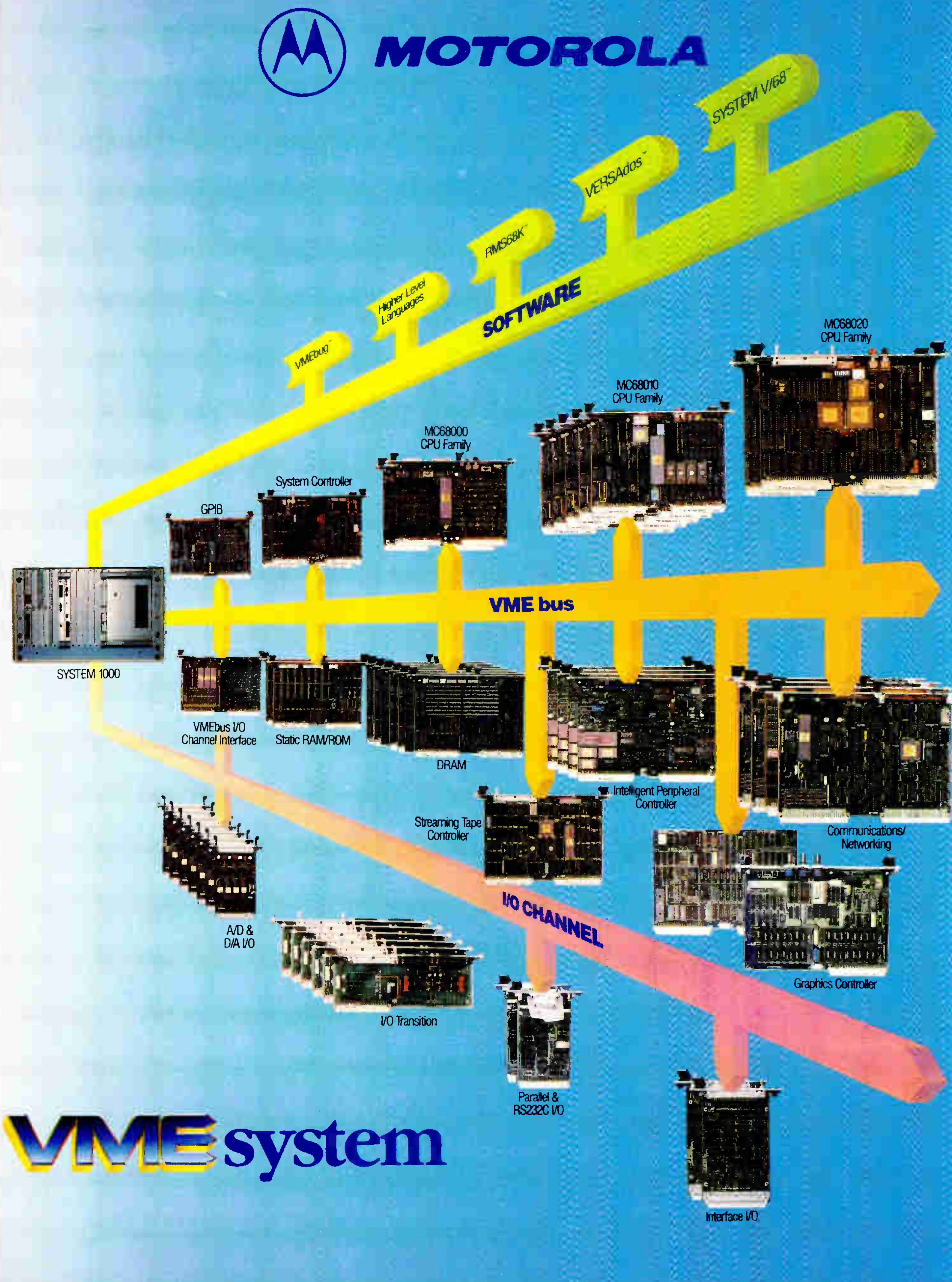
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VMEbus CPU Modules

Model	CPU	Clock Speed (Mhz)	Cap/Sup(Kb) RAM	Cap/Sup(Kb) ROM	CACHE (Kb)	Parallel Ports (Bits)	Serial Ports
MVME 101	MC68000	8.0	64/NS	2048/NS	—	20	2
MVME 104	MC68010	10.0	512/512	256/NS	—	16	2
MVME 105	MC68010	10.0	512/512	256/NS	—	16	2
MVME 106	MC68010	10.0	512/512	256/NS	—	16	2
MVME 107	MC68010	10.0	512/512	256/NS	—	16	2
MVME 110-1	MC68000	8.0	64/NS	2048/NS	—	16	1
MVME 117-3	MC68010	10	512/512	256	—	16	2
MVME 117-3FP*	MC68010	10	512/512	256	—	16	2
MVME 121**	MC68010	10	512/512	512/NS	4	16	1
MVME 123	MC68010	12.5	512/512	512/NS	4	16	1
MVME 130†	MC68020	12.5	64/NS	512/NS	—	—	2
MVME 130COF*†	MC68020	12.5	64/NS	512/NS	—	—	2
MVME 130DON†	MC68020	16.67	64/NS	512/NS	—	—	2
MVME 130DOF*†	MC68020	16.67	64/NS	512/NS	—	—	2
MVME 130XT*	MC68020	16.67	64/NS	256/NS	16	—	2
MVME 131**	MC68020	12.5	64/NS	512/NS	—	—	2
MVME 131COF*•	MC68020	12.5	64/NS	512/NS	—	—	2
MVME 131DON**	MC68020	16.67	64/NS	512/NS	—	—	2
MVME 131DOF*•	MC68020	16.67	64/NS	512/NS	—	—	2
MVME 131XT*	MC68020	16.67	64/NS	256/NS	16	—	2
MVME 133*	MC68020	12.5	1024/1024	256/NS	—	—	3
MVME 133-1*	MC68020	16.67	1024/1024	256/NS	—	—	3
MVME 135*†	MC68020	16.67	1024/1024	128/NS	—	—	2

*MC68881 FPCP NS = Not supplied **MMU †PMMU Socket

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coordination. Testing standards could eliminate the need for much of the costly multiple testing, and a turnkey system reduces the effort required to put a testing operation in place.

The system tests 5¼- and 3.5-in. disks, as well as 4.9-in. Compact-Disc-sized media. The semiconductor laser employed for optical power in Nakamichi's latest tester has been boosted from 20 to 30 mW to improve the reading of data at higher densities and disk-rotation speeds. Rotation speed, laser power, and even the direction of disk rotation can be changed to verify optimum read/write and erase performance.

Write-once optical disks cannot, of course, be bit-mapped over their entire surface without rendering them useless. The system derives its bit-error and other data by tests performed on the narrow strips at the extreme inside and outside edges of the disk, outside the regions reserved for user writing.

For the optical-disk business itself, the new test system, and its potential of helping the move toward standardizing parameters, is coming along at the right time, notes Lee H. Elizer of Freeman Associates Inc., a consulting company in Santa Barbara, Calif. "It's not something that happens in a business going nowhere," he adds. He is coauthor, along with Raymond C. Freeman, of a recent report that predicts $2 billion annual sales of optical drives and media to OEMs by 1991. *–Larry Waller*

PERSONAL COMPUTERS

OLIVETTI AND AT&T'S DEAL MEANS BUSINESS AS USUAL

BASKING RIDGE, N. J.

AT&T Co. may have appeared last week to be throwing in the towel in the personal-computer business, but the new agreement it announced with its European partner Ing. C. Olivetti & C. SpA in reality changed very little. AT&T, which owns about 23.5% of the Italian office-automation company, is placing the fate of its 6300 line of PCs completely in Olivetti's hands. But AT&T was already reselling Olivetti's M24 personal computer in U. S. markets as the 6300 and had relied on Olivetti to manufacture the 6300 Plus.

NEW TERMS. Under the terms of the new agreement, Olivetti will be the exclusive developer and producer of all future AT&T PCs. The agreement extends only to PCs and will last for 10 years. It does not cover the 3B1, a slow-selling desktop Unix work station manufactured by Convergent Technologies Inc., San Jose, Calif., nor AT&T's 32-bit 3B2 work station or the line of 3B minicomputers, which have scored some large sales to Federal agencies.

"This is a move on paper. It really makes no big difference to either company, since both will keep on doing what they had been doing right along," says Francis McInerney, who follows the computer industry for Northern Business Information, New York.

But Olivetti chairman Carlo De Benedetti is jubilant about the decision and says that it positions his company right behind IBM as a global player in PC markets. Of the half-million PCs built at Olivetti's plant in Scarmago, Italy, more than one third went to the U. S. and AT&T, although AT&T has been able to capture only about 6% of U. S. PC sales.

To cement the agreement, Olivetti's Vittorio Cassoni, currently chief of North American operations, will be replacing James E. Edwards as the senior vice president of AT&T's new Data Systems Divison, which includes the former Computer Systems Divison. Edwards, who has moved to a strategic planning slot, says "Olivetti is a creative, low-cost partner who has the ability to get to market quickly. We've been working for two years, driving toward the kind of relationship we announced last week. This new relationship gives each of us a clear assignment: AT&T is responsible for 3Bs, while Olivetti has the PCs." *–Robert Rosenberg*

MEMORIES

3-LOGIC-STATE IC SPEEDS DATA BASE

CAMBRIDGE, MASS.

An extremely flexible form of content-addressable memory developed at the Massachusetts Institute of Technology promises to do for data-base operations what floating-point accelerators have done for number crunching. Called the MIT Database Accelerator, the hardware heart of the system is a content-addressable memory cell that stores three states of logic, yet occupies no more silicon real estate than a typical cell of static random-access memory.

Moving processor functions into memory through the use of content-addressable cells is one way of reducing the bottlenecks that can occur in conventional machine architectures. Content-addressable memory allows for the rapid filtering of large data bases by performing a large number of individual functions simultaneously in the memory cells. Previous approaches to such memories have been effective but rigidly application-specific.

ZIPPEL: "Don't cares" add to the flexibility of content-addressable-memory ICs.

MIT's 32-bit system, however, which will be reported on in detail at Wescon in Anaheim, Calif., on Nov. 18, can perform a variety of operations with words from 1 to 32 bits in size (or larger, when built in 32-bit increments). Key to this flexibility was the injection of significantly more logic into the memory than earlier approaches did, and the ability of that logic to deal in "don't care" states as well as 1s and 0s. The don't-care states are vital to efficient use of CAM in some major applications.

The MIT Database Accelerator is best described as a single-instruction, multiple-data processing system. The system is organized as a large number of lines, each line consisting of a 32-bit word of CAM, four 1-bit registers, a latch to hold the result of match operations, a 1-bit function generator, a selector that controls participation in different operations, and a priority encoder used to serialize output when more than one line finds a match.

COMBINATIONS. The function generator can perform any Boolean function with data from the match latch, the set of four 1-bit registers associated with each line, or from the registers of preceding and succeeding lines of the array. So, for example, two 32-bit lines can be combined to build a 64-bit word.

The use of three logic states provides for finer line-enablement control than that found in earlier CAM arrays. Specifically, the use of don't-care states in the line-enablement mechanism allows the use of binary patterns of lines. Thus even or odd lines exclusively could be enabled for a given operation.

The Database Accelerator performs as a fine-grained parallel processor. After initial concurrent processing, function generators on each line can combine the results of the matches on con-

tiguous lines, if appropriate. In all cases, a priority encoder then scans at high speed and provides the addresses of relevant lines at a speed of one cycle per line. A cycle is about 100 ns.

The 1-bit dynamic CAM cells on each line include four transistors and a diode, as contrasted with other CAM cells approaches, which use up to 10 transistors. Implemented in CMOS because of the circuit complexity and the need to minimize static power consumption, the MIT chip employs buried n-contacts to reduce size. Another space saver is the use of titanium silicide/polycide for the bit lines and match lines in the cell. These require fewer contacts than lines made with two-level metal technology and have lower resistance and capacitance.

Concurrent processing is the key to speed

These technologies together reduce the size of the cells by about 40%, says Charles Sodini, an assistant professor of electrical engineering who oversaw the circuit design. He reports that cells sized 25 by 22 μm have been fabricated, using 2-μm design rules. The team has also built working chips with 64 cells, with future plans to fabricate chips with 1,000 lines at MIT's new in-house fabrication site by the end of 1987.

The data-base work at MIT is part of the Smart Memory Project involving close collaboration between circuit designers, systems architects, and fabrication technologists. It was as a direct result of that collaboration, says Sodini, that don't-care states were added.

"If I designed a CAM [in isolation], I never would have thought to store a don't care," says Sodini. Pressure to include don't cares came from Richard Zippel, an associate professor of computer science and engineering, who is now on leave and working as a technical director at Symbolics Inc., a maker of artificial-intelligence systems. Zippel argued that the inclusion of this third state added greatly to the system's flexibility.

"Two applications couldn't be done without it—logic simulation and constraint networks for AI applications," he says. With logic simulation, the don't cares allow the system to ignore variables that don't exist in product terms. The team anticipates that the Database Accelerator will find applications in text retrieval, logic simulation, and speech or vision processing. *–Craig D. Rose*

MANUFACTURING

SENSOR LETS ROBOTS DO TOP-QUALITY ARC WELDING

TOKYO

A breakthrough in robot technology that could give Japanese shipbuilders an important competitive advantage has emerged from an unlikely source—Nippon Telegraph and Telephone Corp. A new visual sensor that allows robots to perform continuous-bead arc welding, a type of welding vital to shipbuilding, has been developed by NTT.

The combination of shipbuilding and telecommunications is not as unlikely as it seems. Hisashi Shintoh, president of NTT since 1981, had previously been president of Ishikawajima-Harima Heavy Industries Co., one of Japan's largest shipbuilders. It was his idea to use communications technology to widen the use of robots in shipyards.

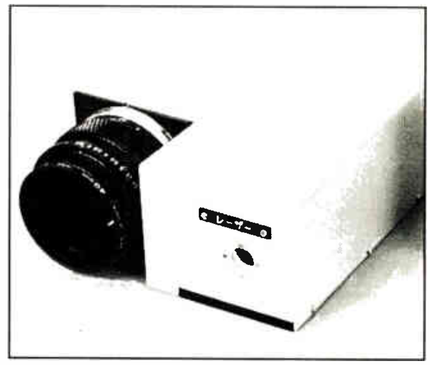
What Shintoh sought was a sensor that could guide a robotic arc-welding head. Although robots routinely do welding jobs in a variety of industries, notably automobile manufacturing, sensor shortcomings have limited the use of robots for continuous-bead arc welding. Now, a small Tokyo subsidiary of NTT, NTT Technology Transfer Corp., whose main function is licensing NTT technology to outside users, has built a sensor that is up to the task. And it has given Ishikawajima Harima Heavy Industries a nonexclusive license to build arc-welding gear for in-house use and for sale to others. Test-equipment manufacturer Ando Electric Co., Tokyo, is also designing a system, and NTT Technology Transfer president Giichi Ito says that his firm is actively seeking additional licensees at home and abroad.

PRECISE. NTT's new sensor tracks the x-y position coordinates of the cross section of the parts to be welded along the path traveled by the welding torch. This enables the weld to be made precisely at the joint between the two workpieces, resulting in a strong weld.

It has been their inability to follow the joint precisely that has made robots poor arc welders. Tolerances are much coarser in the spot welders commonly used in automobile production, because welds can be anywhere within the width of the lips provided for spot welding. However, even in autos, spot welding may be replaced by arc welding, because elimination of the lips would reduce weight in the finished cars.

NTT's sensor can make its measurements immediately adjacent to the

The Healthiest Companies . . .



WELDING EYE. NTT's new sensor makes accurate robot arc welding possible.

bright welding arc, so it can guide the welder accurately. Moreover, it can do so while mounted 200 to 400 mm away from the work, keeping it away from splashing molten metal and fumes. Other sensors must work much closer. As a result, the filter glass protecting the sensor lens must be changed every 30 minutes. The NTT sensor can operate for half a day or more before a filter change is necessary.

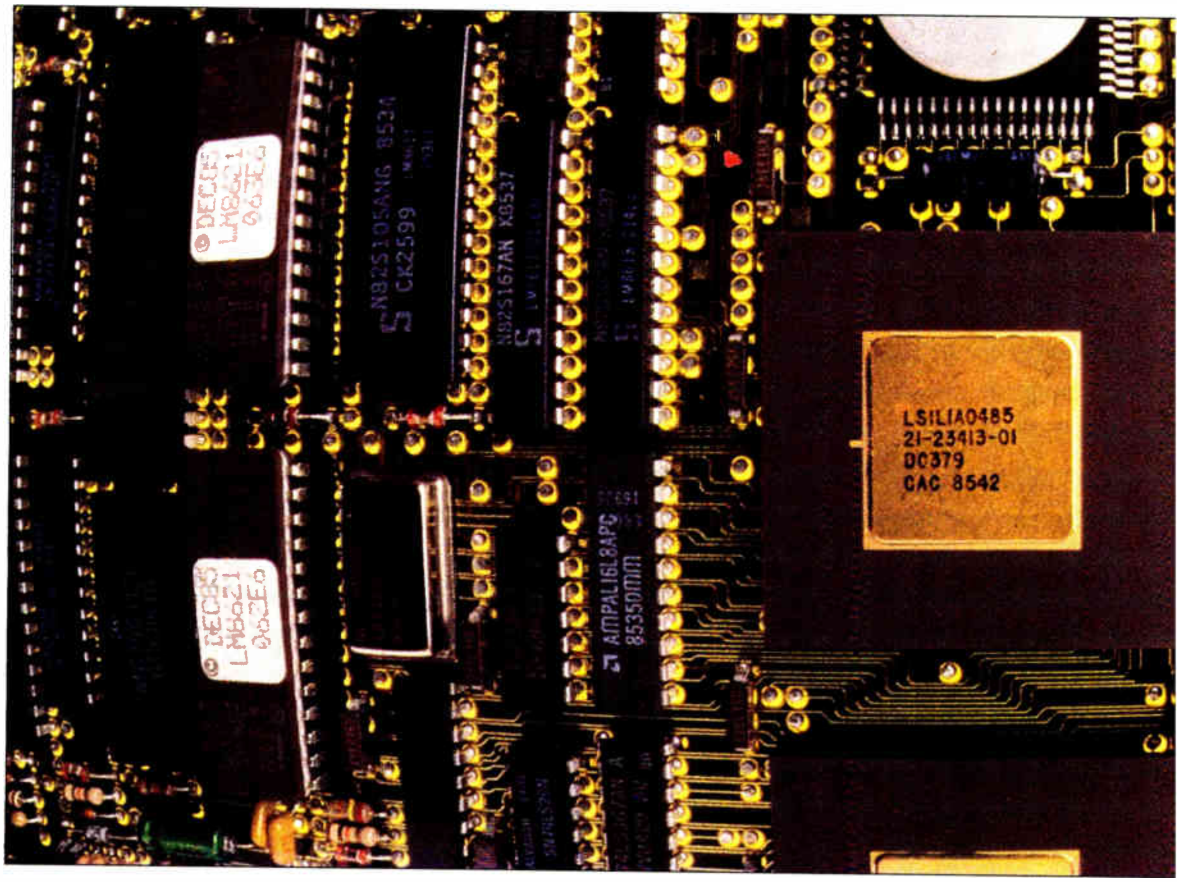
BRIGHT LIGHTS. The mechanically scanned laser beam is diffusely reflected by the work and returns to strike one of the 64 photodiodes in a linear array. Signals from the array are converted from parallel to serial format by scanning the diodes at 160 kHz. Triangulation is used to determine the height profile of the work.

A sensor used for arc welding must cope with interference from light radiated by arcs with currents of up to 1,000 A, and random sparks. Fortunately, the luminous energy from the arc reflected from a unit area of the work is slightly smaller than the laser-beam energy reflected from the same area, and most of the reflected arc energy is concentrated in the frequency range below 100 kHz.

Carrier-frequency techniques, including modulation of the laser-diode beam at 1.6 MHz, make it possible to filter out noise from the arc's reflected luminance. Each photodiode is selected by the 160-kHz scan for a period during which 10 pulses are emitted by the laser. Ten cycles from each diode pass through bandpass filters in the sensor's amplifier circuits, which reject the noise.

It takes 75 ms for the laser beam to make one scan across the work, so three of these pulse trains are produced while the reflected beam passes over each of the array's 64 diodes. This lets the system pinpoint the position of the reflection at that time. During each scan, 64 height measurements are made. Ito says that using television-type image sensors—which other companies have tried—is a losing proposition, because they integrate incident light, preventing the use of modulation techniques. *–Charles Cohen*

If you're not finding Gate Array, Advanced Schottky, and SMT faults, maybe the fault lies with your tester.



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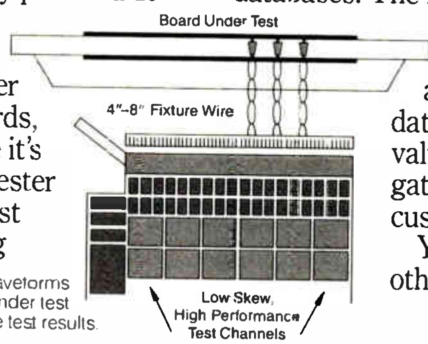

The L210i delivers waveforms accurately at the board under test for repeatable test results.

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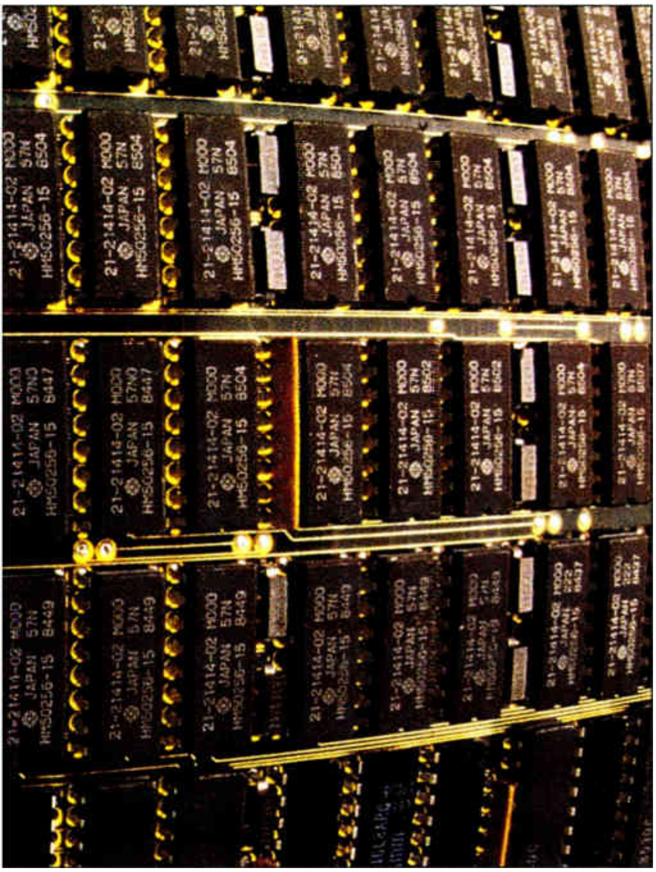

clusters. Memory arrays. Or hard-to-isolate devices.

With its MultiMode capability, you can easily partition the board into functional clusters, making the most of the L210i's functional test and diagnostic techniques.

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Circle 47 on reader service card

INTERNATIONAL NEWSLETTER

HITACHI, FUJITSU BELATEDLY TEAM TO DEVELOP TRON MICROPROCESSORS

With time running out on Japanese efforts to catch up in the 32-bit microprocessor market, the TRON operating-system kernel is attracting more attention [*Electronics,* May 12, 1986, p. 41]. Four of the five leading Japanese semiconductor companies are working on 32-bit CMOS chips for TRON (The Real-time Operating-system Nucleus), and now two of them, Hitachi Ltd. and Fujitsu Ltd., will jointly develop a family of 32-bit TRON microprocessors, under the terms of an agreement that includes exchange of pattern-generation tapes for fabricating masks but excludes process details. The first chip will have the same specifications as Hitachi's H32 [*Electronics,* Oct. 16, 1986, p. 39] and is scheduled to be delivered in late 1987. Fujitsu has been working on an even more powerful TRON chip, with more than 1 million transistors, that is due to reach the market in 1988. □

INTERMETALL TWEAKS OLD PROCESS TO GET 1-MHz LOGIC

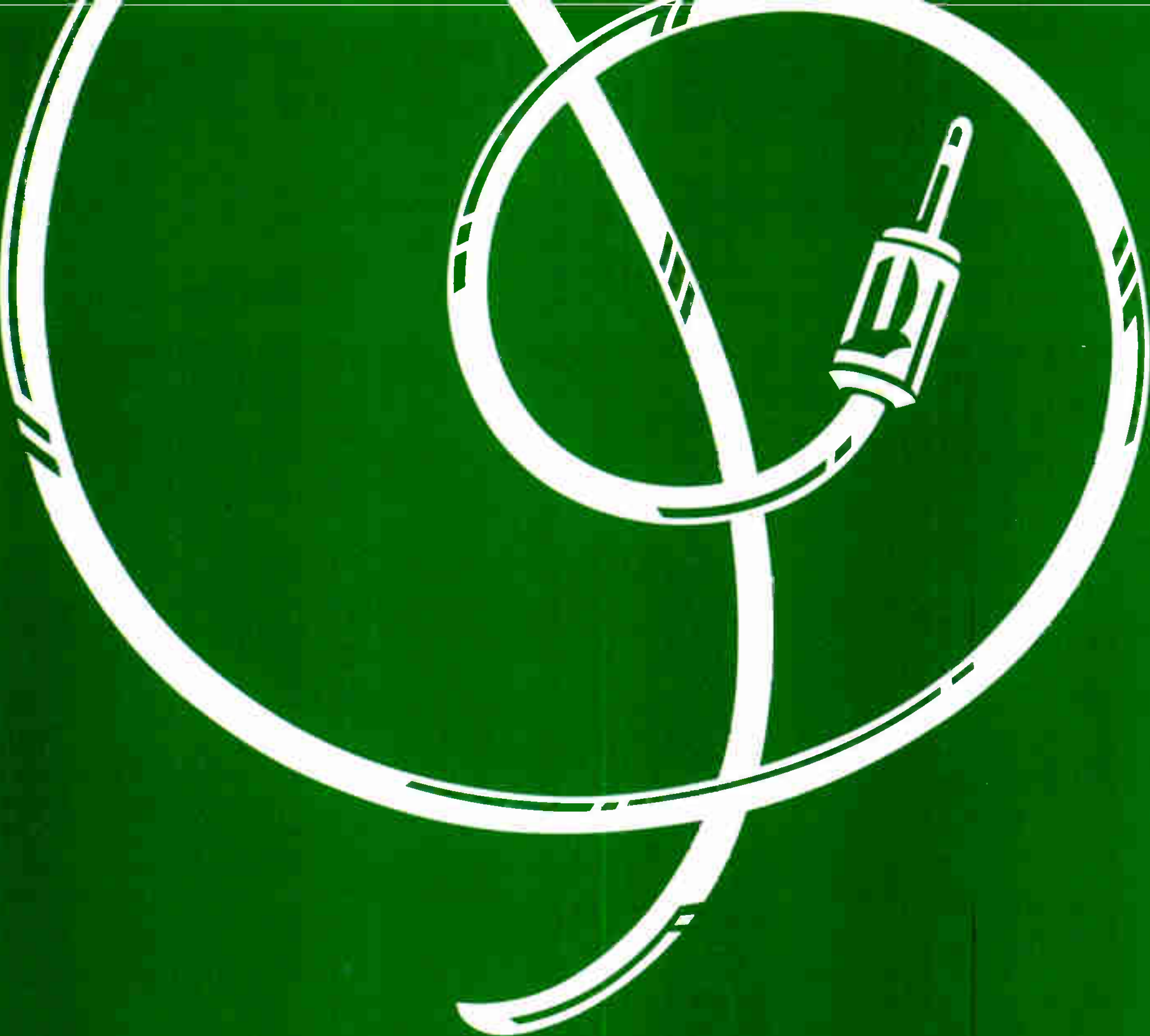
Engineers at Intermetall GmbH, the Freiburg, West Germany, lead house of the ITT Semiconductor Group, have taken the fast route to fast logic. Instead of coming up with new technology, they've simply modified their own collector implantation technology [*Electronics,* July 24, 1986, p. 29] to build emitter-coupled-logic integrated circuits with transit frequencies as high as 5 GHz. This value, which they believe is the best for any nonepitaxial bipolar device, will let them design logic circuits that run at up to 1 GHz; that's more than three times better than the original collector implantation process. The Intermetall team achieved the high speed by using arsenic-doped polysilicon for the emitter and a completely silicided transistor surface, which reduces the collector, emitter, and base resistances. The ECL gate delay checks in at 200 ps and the external base resistance at 20 Ω. Matching of a transistor pair is better than ±0.25 mV over a temperature range of 0°C to 150°C. □

PIONEER JOINS THE RUSH TO 5¼-IN. OPTICAL DISKS FOR THE OFFICE

The 5¼-in. format is rapidly becoming the standard for office optical data disks, opening the floodgates to Japanese manufacturers rushing into the office-automation business. The latest is Pioneer Electric Co., which has developed a subsystem with a double-sided read-write disk storing 600 megabytes that it expects to market next year in the U. S. and Japan. The system is to be shown at Comdex this week. Also coming next year is Sharp Corp.'s 600-megabyte filing system. These optical-disk systems will join Toshiba's 800-megabyte product, which is already available in sample quantities. □

FRANCE'S CGE BUYS CABLE AND FIBER-OPTIC OPERATIONS FROM ITT

France's Compagnie Générale d'Electricité last week picked up ITT Corp.'s cable and fiber-optic operations, worth $427 million, adding them to the billion-dollar package it has purchased from ITT. The deal [*Electronics,* July 24, 1986, p. 113] has made CGA's Alcatel SA subsidiary the world's No. 2 producer of telecommunications equipment after AT&T. Meanwhile, CGE and its partners filed papers in late October to set up a Dutch holding company, Teleglobal Communications NV, that will become the parent company of the German, Belgian, and Spanish telecommunications-equipment subsidiaries of ITT. But despite rumblings that the potential Spanish partner, Telefónica SA, might pull out of the deal, CGE president Pierre Suard insists that his firm, plus the Société Générale de Belgique and other European partners, can raise the $1.152 billion cash payment that ITT will get in addition to a minority share in the new company. It will start up with assets of $4.6 billion and annual sales of $12.5 billion. □



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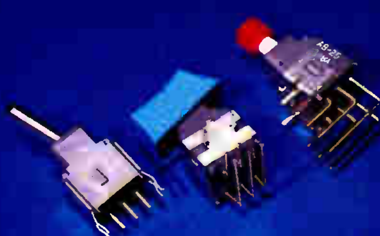

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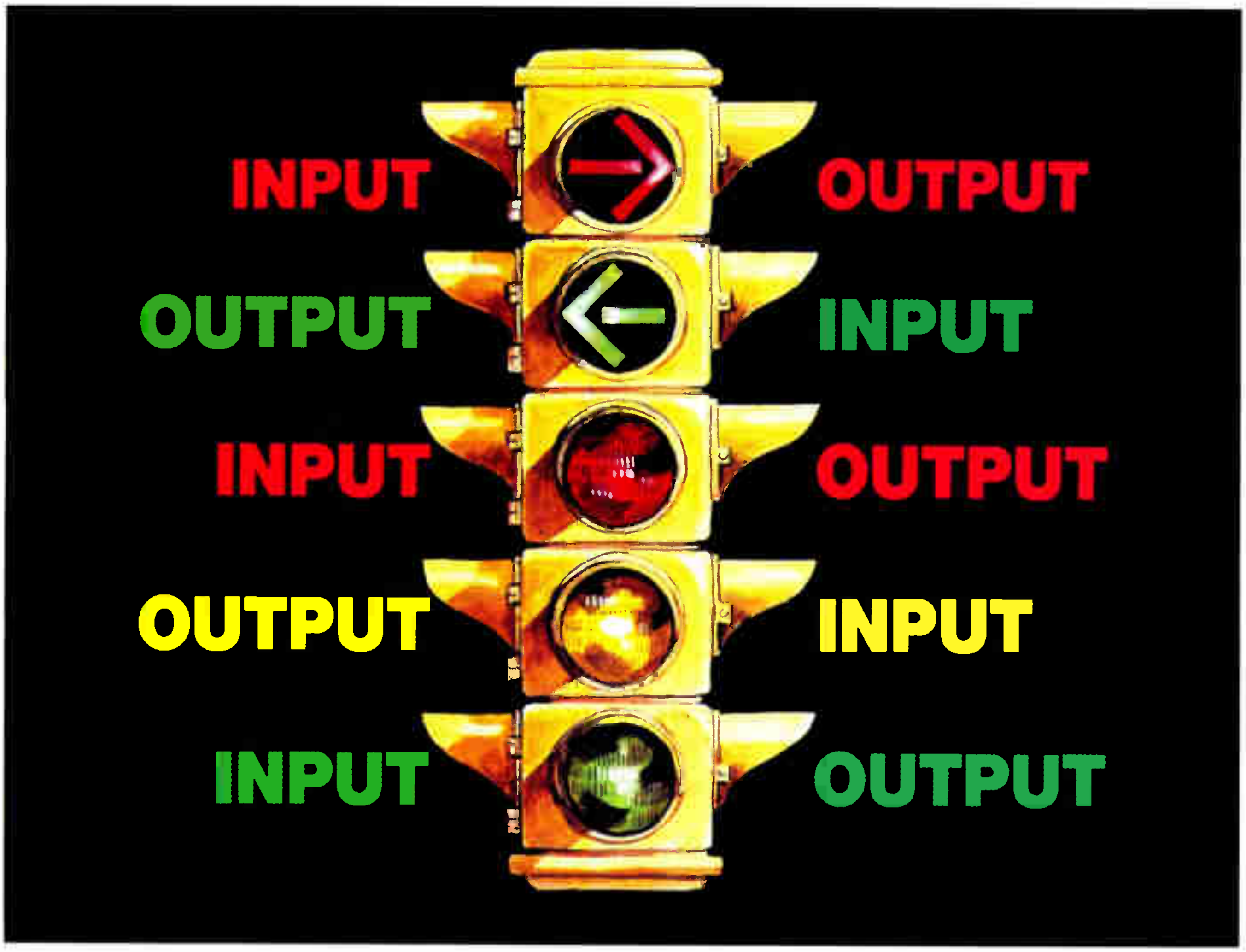


THE BIG DRAG ON COMPUTER THROUGHPUT

by Tom Manuel and Clifford Barney

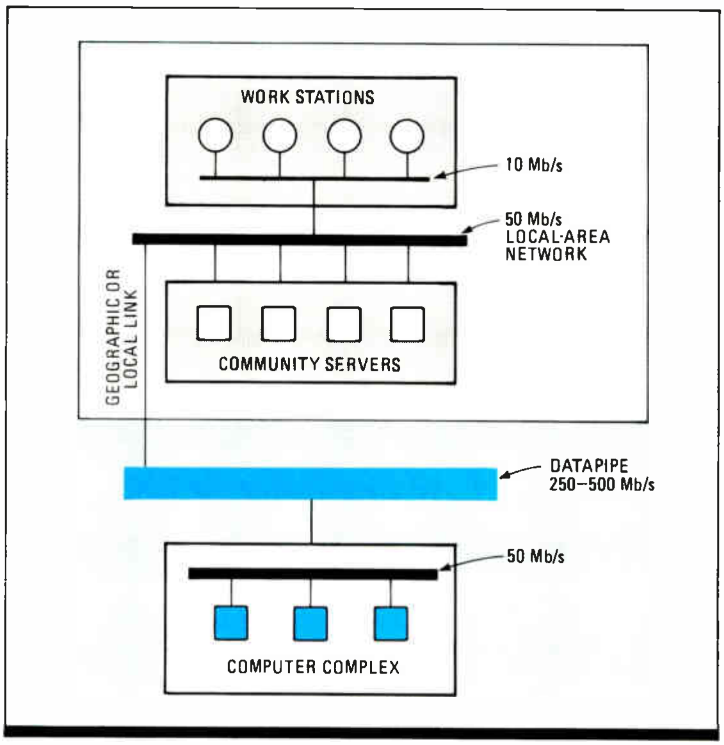
Input/output is the neglected stepchild of computer systems. Little has been done to make I/O pathways fast enough to keep up with central processors and memories. But now, I/O bottlenecks are getting more attention from specialized vendors as well as some designers of high-performance computer systems. They have begun to realize that no matter how much time and money a design team spends building a fast central processing unit, its effort will be wasted if the processor sits idle because it can't get or send data fast enough.

The I/O bottleneck has become glaringly obvious with the newest systems coming onto the market—supercomputers, minisupercomputers, parallel computers, and high-performance graphics processors—systems that have very fast CPUs, multiple processors, and specialized I/O devices. "There is too much focus on macho-flops and not enough on throughput," says Jeffrey Canin, supercomputer analyst at Hambrecht & Quist Inc. in San Francisco. At least one minisupercomputer vendor agrees: Most systems have "the wrong kind of plumbing; they're trying to feed a six-inch pipe with a garden hose," says Carl Haberlund, marketing vice president at Scientific Computer Systems Inc.

The trickle of data through the I/O hose will turn into a torrent if the growing number of companies working on the problem have their way. A wide range of new I/O techniques are hitting the market—faster buses, intelligent high-performance I/O channels, and multiple I/O processors.

New technologies are being implemented, such as the fiber-optic-based Datapipe from Network Systems Corp. (Fig. 1). Most important, and most encouraging to those spreading the gospel of faster I/O, is the fact that some of these products come from new companies that are building specialized products to speed up I/O.

One such product is a 100- to 200-megabyte/s I/O computer from Aptec Computer Systems Inc. (see p. 54), the system 200, which uses a 25-MHz bus to clear a high-speed path for data. Wayne H. Matterson, director of engineering at Aptec, says that an I/O computer can be the hub of a high-performance computer—a tool that takes care of all the traffic among processors and peripherals.



1. I/O FOR THE FUTURE. Datapipe, now in beta test, is designed to run at 275 Mb/s, a speed that Network Systems Corp. believes will be needed soon.

Other companies are taking different approaches, but all of them are betting that a market for specialized I/O tools is emerging. "Is I/O a problem? You bet it is. We're building a company based on the premise that there is a big problem," says Newton Purdue, vice president of product development at Ultra Corp., a Santa Clara, Calif., company that was incorporated in January.

Ultra is working on a new method of high-speed data transfer, about which it will reveal very little. Purdue says only that he sees interfacing as the key: "There are not as many high-performance peripherals as users would like to see, because there is no place to connect them." In general terms, Ultra's interface will be adaptable to each supercomputer and minisupercomputer that comes out. Every specific host and peripheral will have a unique interface on one side and a standard on the other. That way, the host can be accessed by every new peripheral that comes out, and the new peripherals can access every host.

HIGH-SPEED INTERFACING

ZeroOne Systems Inc., the Santa Clara, Calif., supercomputer system integrator, is taking another tack. It is adding a high-speed I/O subsystem to a Convex Computer Corp. C1 supercomputer by using the Convex high-speed parallel interface, an Aptec System 24 I/O computer, and high-speed Ibis Systems Inc. disk drives. This combination is then connected to a Cray supercomputer through a Network Systems Corp. 6-megabyte/s Hyperchannel.

Convex is one of the few computer vendors that can attach high-speed peripherals to its own products. Its interface, called HSP, is a channel control unit that manages a tap into the Convex C1 minisupercomputer's internal bus, which is 64 bits wide and speeds along at 80 megabytes/s.

"HSP taps the C1's 80-megabyte/s bandwidth for burst transfers of data in or out for certain applications, such as capturing large amounts of data in short periods of time—for example, from a satellite as it passes overhead," says Jeff Wilson, product manager for hardware at the Richardson, Texas, company.

A potential problem with high-speed I/O pipes is latency, the time it takes to get them going. A long latency time can reduce throughput on burst transfers. The HSP reduces latency by doing the lgoical and physical memory mapping completely in hardware. Also, the HSP preempts the I/O subsystem of the C1 while it is in operation, so that little else in the way of I/O can occur. However, it is a boon to certain users who have unusual requirements for fast data transfers—those who have systems configured with the ZeroOne Convex-Aptek-Ibis high-speed subsytem and the Cray-Hyperchannel connection, for example.

Another minisupercomputer vendor that is now concentrating on I/O is Ncube Corp. in Beaverton, Ore. Its N-Cube family is built around the hypercube architecture, with systems ranging from 16 to 1,024 processor nodes. All I/O is built into the processor chips, which are custom 2-μm NMOS parts from VLSI Technology Inc. Each chip has 11 2-megabyte I/O channels—10 to communicate with other nodes, one for system I/O. "We're actually using a processor chip for I/O," says Robert C. Hausman, vice president of marketing for the N-Cube system.

One reason for the company's emphasis on efficient I/O is the growing realization that customers have to have it. "Finally, people are starting to recognize that you can't have a supercomputer without putting something next to it to move stuff into it," says John Gustafson, staff scientist. "People need good graphics capability. They need to be able to compile quickly, to get things off and on the disk. Not providing these features is irresponsible."

GRAPHICS TAKE A FAST BUS

Besides supercomputers and minisupercomputers, the systems that put the highest demands on I/O are probably specialized graphics processors and their output devices. They feature very high-resolution color displays that must be changed rapidly—and therefore need very high data-transfer rates. For example, Ultra's Purdue says, "a lot of customers we talk to have graphics problems that require data-transfer rates in the range of a gigabit per second or greater. A typical 1-K-by-1-K screen size, refreshed at 24 bits/pixel, requires close to 3 megabytes of data per screen. Users want to animate that by pushing a button and see it change immediately. That requires a 24-Mbit/s I/O rate."

Among the specialized solutions to this problem is the Pixar Image Computer from Pixar in San Rafael, Calif. (Fig. 2.) It has a system-bus bandwidth of 240 megabytes/s and an 80-megabyte/s bus called the Yapbus for updating pixels on the screen [*Electronics Week*, April 29, 1985, p. 18].

Other approaches are being explored for conventional data processing, including one by Ibis, a maker of high-performance disk drives. The Westlake Village, Calif., company is more or less forced to work on its own approach, because the I/O problem "is only recognized by a handful of people," says Taroon Kamdar, director of business management. "Designers of fast CPUs have ignored or given lower priority to the problem of passing data back and forth to peripherals. They are concentrating on MIPS and megaflops. Some minisupers have buses that can handle only 2 to 3 megabytes/s."

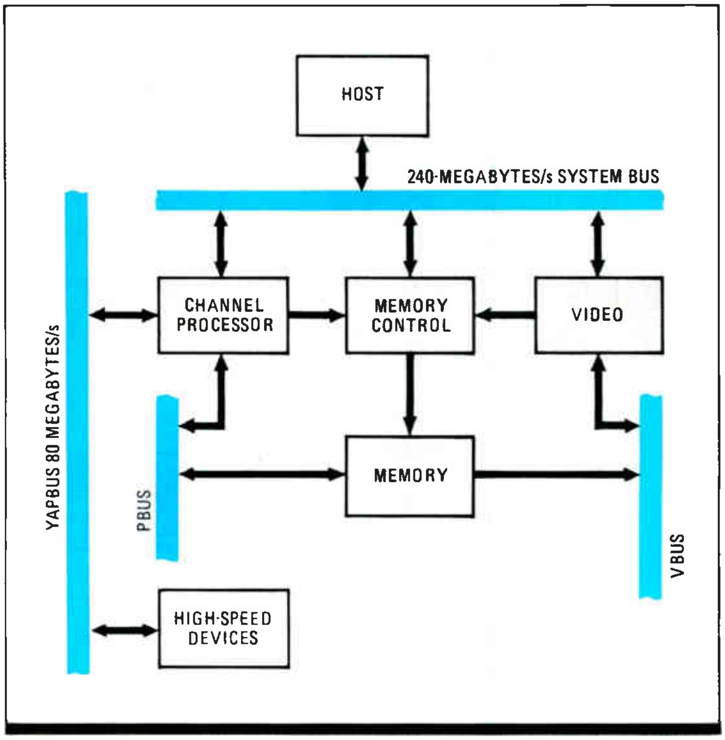
The speed of the Ibis drive—12 megabytes/s—is obtained by driving four 3-megabyte/s channels in parallel. Ibis now has 6-megabyte/s channels running in its laboratory and will ship a product within 90 days that will perform at 24 megabytes/s. Even 48 megabytes/s is possible with this technology, Kamdar says.

An I/O tool adapted from communications technology is being promoted by Network Systems, the Minneapolis maker of the Hyperchannel. There, Gary Christensen, vice president of development, echoes Kamdar's feelings about the fixation on high-speed central processors. The idea that computer designers pay too much attention to making faster CPUs and not enough attention to the I/O "has been my song and dance since [Seymour] Cray built his first machine," he says. "Although the Hyperchannel is primarily a computer-networking solution, it does help bust the I/O bottleneck in cases where it is used to allow computers to share peripherals."

Network Systems' answer for the future is Datapipe, a fiber-optic network product that is targeted to run at 275 Mb/s (about 35 megabytes/s). Datapipe [*Electronics Week*, July 22, 1985, p. 36] is in beta tests at one customer site, where it is running at about 250 Mb/s.

Christensen concedes that his company has seen only limited demand so far. "A lot of people don't understand why they would need 275 Mb/s," he says. "It's only the very sophisticated users who are starting to get enough traffic on their networks that they're starting to wonder, 'Hey, what am I going to do?' We hope we're coming out with a product at about the time the demand gets there." □

Additional reporting by Wesley R. Iversen



2. READY. Pixar's Image Computer, with its 240-megabyte/s system bus, is designed for quick responses in high-resolution graphics work stations.

HOW APTEC PLANS TO BREAK THE I/O BOTTLENECK

A system with independent processors and a 25-MHz bus, capable of moving 200 megabytes/s, takes over data-transfer chores from central processing units

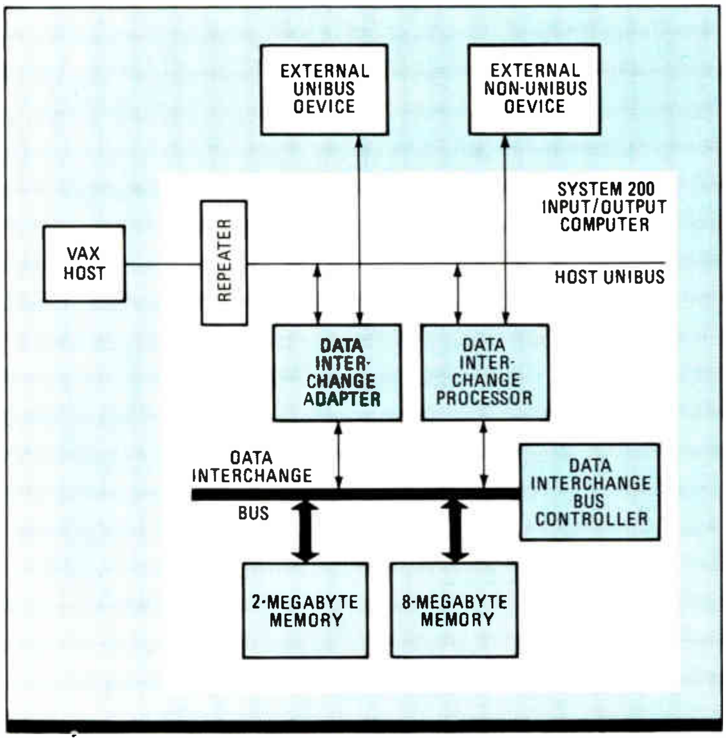
One way of cracking the input/ouput bottleneck is by giving all of a system's I/O tasks to a separate computer equipped with its own high-speed processing units and wide-bandwidth data bus. Following this approach, Aptec Computer Systems Inc. has come up with an I/O computer that can keep pace with the fastest central processing units and peripherals available today—reaching peak data rates of 200 megabytes/s.

Aptec's system 200 (Fig. 1) speeds up I/O two ways. It moves data across a high-bandwidth bus at typical speeds of 150 megabytes/s. It can also perform input and output functions in parallel, using a multiword addressing scheme, which boosts the rate to 200 megabytes/s. And, besides speeding I/O for hosts, the system 200 can grow with them—as more external devices are added to the host system, more processors can be added to the system 200.

The configuration resembles that of Aptec's first product, the system 24. The difference lies mainly in enhancements to the data bus, chiefly going from one 32-bit-wide bus to two independent 32-bit-wide buses. Overall, the enhancements dramatically increase the data rate—from 24 megabytes/s for the older system to the 200 megabytes/s possible with the new one.

Aptec's systems are built around two types of processing units, equipped with banks of first-in, first-out buffer logic, that direct the flow of data; a 25-MHz data bus and its controller; and two banks of mass memory. A unit called a repeater isolates the system 200 from other devices on the host system's bus, so that it can perform I/O functions without involving the host. The system 200 makes extensive use of state-of-the-art CMOS gate arrays, organized in a bit-slice architecture, from LSI Logic.

All bus-interrupt requests from attached devices are handled by the controller managing the system 200's bus. For example, data coming from a data-acquisition device is shipped across the high-speed bus to mass memory. When an attached processor, such as a graphics processor, needs that data, it sends a request to a specific location in the memory, and the data is shipped back across the bus. Once the graphics processor has completed its operations, the data is sent back to memory. From memory, the data then



1. LIFTING THE LOAD. Two kinds of processors and a high-bandwidth bus combine in the system 200 to relieve host processors of I/O functions.

can be sent across the bus again, to a display, disk drive, or applications processor.

The two kinds of system 200 processors can operate in parallel, transferring data to or from external devices for use in the same application. The parallelism is maintained when additional data-interchange-adapter or data-interchange-processor cards are loaded into the system.

"There is really nothing fancy about it. We are using a mailbox method to communicate between the independent processors attached to the bus," says Wayne H. Matterson, director of engineering at Aptec. "When one of our independent I/O processors completes its job, it ships the data to memory, where the next processor looks for its address. People are scared when it comes to writing applications with any degree of parallelism. This mailbox approach greatly simplifies the programming task."

Both of Aptec's systems are designed to work with a Digital Equipment Corp. VAX, although they can be adapted to run with systems from other computer makers. New versions are now being adapted for other systems, the company says. The basic system 200 is currently undergoing beta testing. Shipments are scheduled to begin in March 1987.

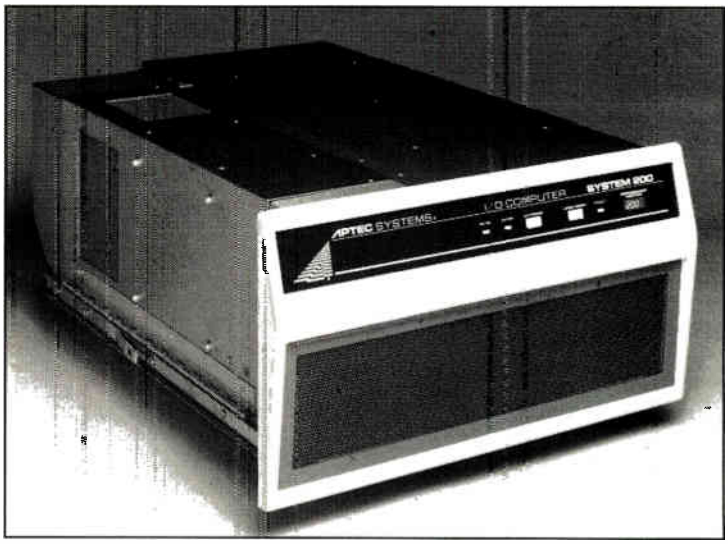
If the executives of Aptec are right, the computer industry needs as many versions of its I/O computer as the Beaverton, Ore., company can turn out. "With so much of the industry's attention focused on CPU speeds, most computers simply are not designed with enough I/O bandwidth to strike a balance between processor speeds and the input-out demands of high-speed peripherals," says Thomas Moir, Aptec's president. "The U.S. computer industry is myopic about CPU speeds. They have become speed freaks."

Aptec's cofounders, Gary McAlpine and Woodrow Wittmayer, realized that cranking up CPU speeds does not address the problem of the bus bottleneck at all. They saw a solution in lifting the burden of I/O control from the host computer and giving it to independent processors—the system 200—which can keep pace with the demands of high-performance peripherals.

TWO PROCESSORS

The processors at the heart of the system 200 are called the data-interchange adapter and the data-interchange processor. They control the I/O functions of such high-speed peripherals as data-acquisition devices, graphics processors, and high-performance disk drives. Instead of hogging host CPU cycles, the high-speed peripherals or specialized applications processors share access to the system 200's mass memory.

The data-interchange adapter provides a transparent, 3.125-megabyte/s interface between peripherals attached to VAX systems through a Unibus and the system 200's data-interchange bus. The VAX can execute operations through the data-interchange adapter, or the adapter can



2. EXPANDABLE. The basic box contains one of each type of processor; more can be added as system I/O demands grow.

command data transfers between the attached device and the host's main memory without involving the host CPU. The adapter can also transfer data between devices on the VAX's Unibus and the system 200's mass memory, another adapter, or the second type of processor, the data-interchange processor.

The data-interchange processor controls I/O for non-Unibus devices. It can manage up to three devices, overseeing 12.5-megabyte/s data transfers between the device and System 200 mass memory or between VAX memory and other data-interchange adapters or processors.

Building the system 200 "required liberal use of high-performance gate-array technology in the processors as well as the first-in, first-out memory buffers," says Matterson. The FIFO electronics make up the bus interface logic on all the boards in the system that perform interface functions in the system 200.

The two processors and their attendant FIFO buffers are built with 144-pin gate-array technology from LSI Logic. "We have the equivalent of four 2901 bit-slice processors implemented in one of our gate arrays," Matterson says. "We chose LSI Logic because it was the only vendor with CMOS parts in the range we needed. Others announced, but they could not deliver. The 9000 series that we used in the design has 8,600 effective gates, and we used every one."

Both types of processors send data across a data-interchange bus built around 32-bit-wide address, write, and read paths that are synchronized to a 25-MHz clock under control of a single processor called the data-interchange bus controller. The bus accommodates simultaneous bidirectional transmission of 8-, 16-, 32-, 64-, or 128-bit words to any combination of processors. Matterson refuses to be very specific about the arbitration scheme that manages the transfers, saying, "It is the one thing that we hold near and dear to our heart. It is our trade secret."

The data-interchange bus controller contains the arbitration logic and controls the data interchange bus: it takes care of requests for acccess and issues grants from other processors, typically within 40 ns.

The system 200's mass memory—configured using 55-ns static random-access memory—is implemented on either 2- or 8-megabyte boards. Both configurations use single in-line packaging to conserve board real estate: the 2-megabyte version is implemented with 64-K-by-1 chips while the 8-megabyte version is packaged as 256-K-by-1 chips. Matterson says the current boards hold more logic, to direct the flow of data into and out of memory, than memory itself, and that next year, a new generation of logic could push the transfer rate still higher.

FOUR MEMORY BANKS

Each board, regardless of its storage capacity, has four distinct memory banks with a total board bandwidth of 50 megabytes/s. Writes to memory can be 8, 16, 32, 64, or 128 bits long. Reads use 32-, 64-, or 128-bit accesses.

A multiword addressing scheme eases the burden on the address bus. In a simple addressing scheme, each data element transferred across the read or write bus is preceded by an address—which means address-bus throughput can limit overall performance. Aptec's multiword addressing automatically computes the second and possibly up to three additional address words from the first word, rather than sending sequential addresses across the bus.

An important feature of the system 200's configuration is the Unibus repeater. It reduces the Unibus's load by isolating the system 200. Acting as a Unibus extension, in effect it provides room on the bus for the system 200 to operate without drawing on the VAX's resources.

Aptec chose to design its original system 24 and the new system 200 to work with DEC systems mostly because the VAX seemed to be the computer that most needed help with I/O, says Larry Wade, Aptec's vice president of marketing. "Its processors are continually tied down servicing I/O requests on the low-bandwidth bus, which simply can't accommodate today's high-speed I/O traffic."

The company doesn't intend to stop with the VAX. Work is already under way on a VME-bus interface adapter. And connections for the Flex/32 from Flexible Computer Corp. and Butterfly computers from Bolt, Beranek & Newman are also being considered, Moir says.

Aptec's system 200 overcomes the constricted bus bandwidth that plagues a variety of host computers in complex systems. By concentrating on I/O requirements, it could also help rearrange some computing priorities—turning attention away from the drive to build faster and faster CPUs, and toward an effort to improve overall system performance. □

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HOW APTEC'S McALPINE TOOK ADVANTAGE OF A CONSERVATIVE DESIGN

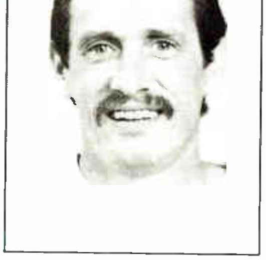
Road maps are hard to come by in the world of advanced computing, but that has never bothered Gary McAlpine, the cofounder of Aptec Computer Systems Inc. and the chief designer of its latest input/output computer, the system 200. "My education has always come from experience," says McAlpine, who is vice president of research and development for the Beaverton, Ore., company.

The 38-year-old McAlpine joined the Navy right after high school. He spent the first two years of his hitch training as a data systems technician. Then he saw the world for four years aboard an aircraft carrier, where he helped run a large computer system used for intelligence gathering.

McAlpine used his Navy training to get a job with Floating Point Systems Inc. There he gained a new perspective on the problems faced by system integrators trying to build complex systems, and the shortcomings that inevitably resulted. "Those array processors weren't giving customers everything that they needed," he says. McAlpine began working as a consultant to Floating Point Systems users who had I/O problems.

In January 1981, McAlpine and a former Floating Point coworker, Woodrow R. Wittmayer, launched Aptec. Wittmayer is now vice president of marketing. The company's first product, the system 24, was introduced in August 1982. It was based on a very simple principle: it would take over the I/O functions from a host computer, the functions that "divert the host processor from its primary function, which further slows overall system performance," says Aptec's director of engineering, Wayne H. Matterson.

"We were very conservative. We over-engineered the machine," McAlpine recalls. "When we saw the clean signals we were getting across the backplane, we decided we could have squeezed four times the throughput from it." He began considering how to improve the system 24 before it hit the street, but had to wait. "We just didn't have customers who were ready with applications yet. They were talking about higher speeds, but they didn't need them yet." Now Aptec thinks they're ready.



GARY McALPINE

WAYNE MATTERSON

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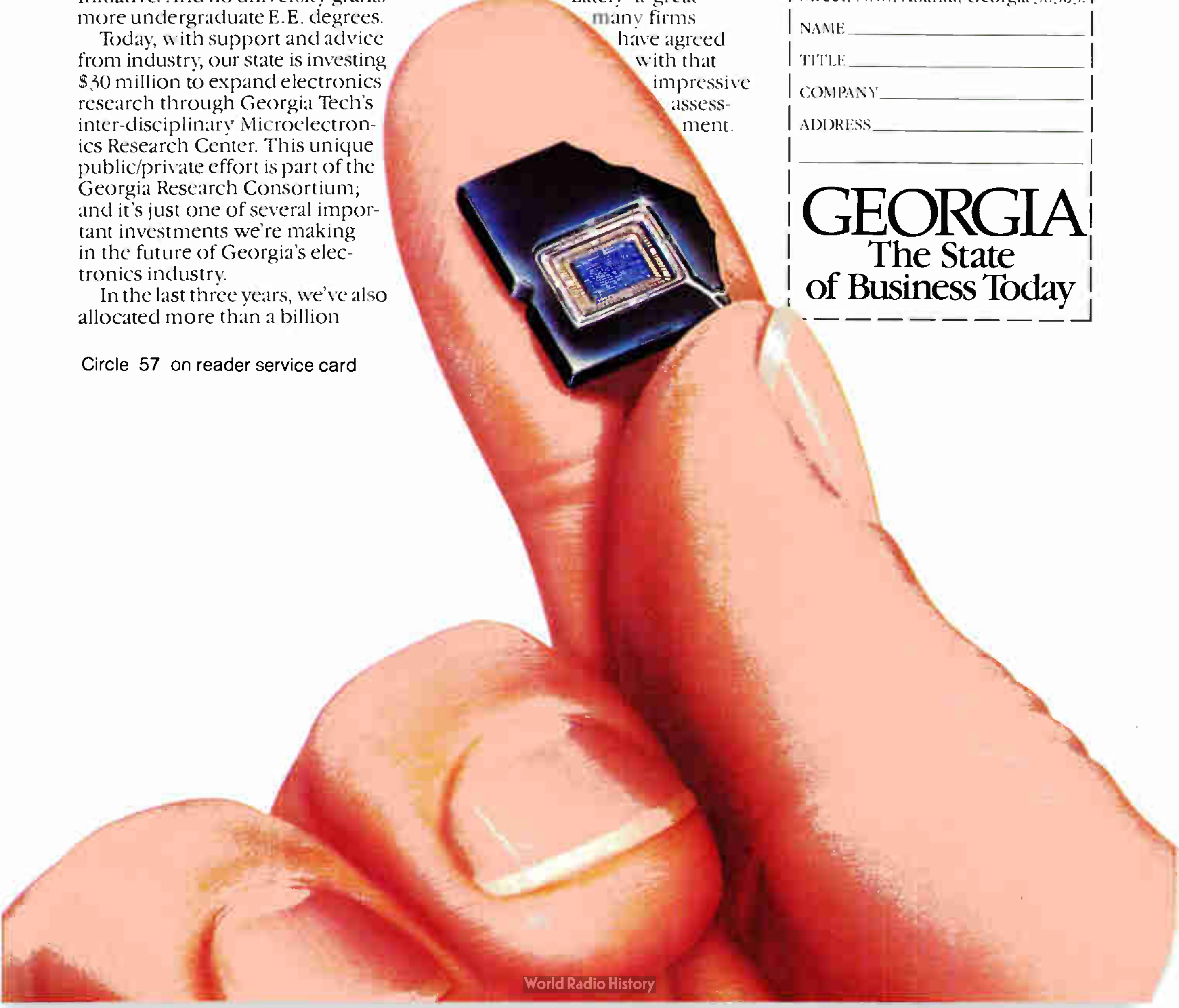
The State of Business Today

Circle 57 on reader service card



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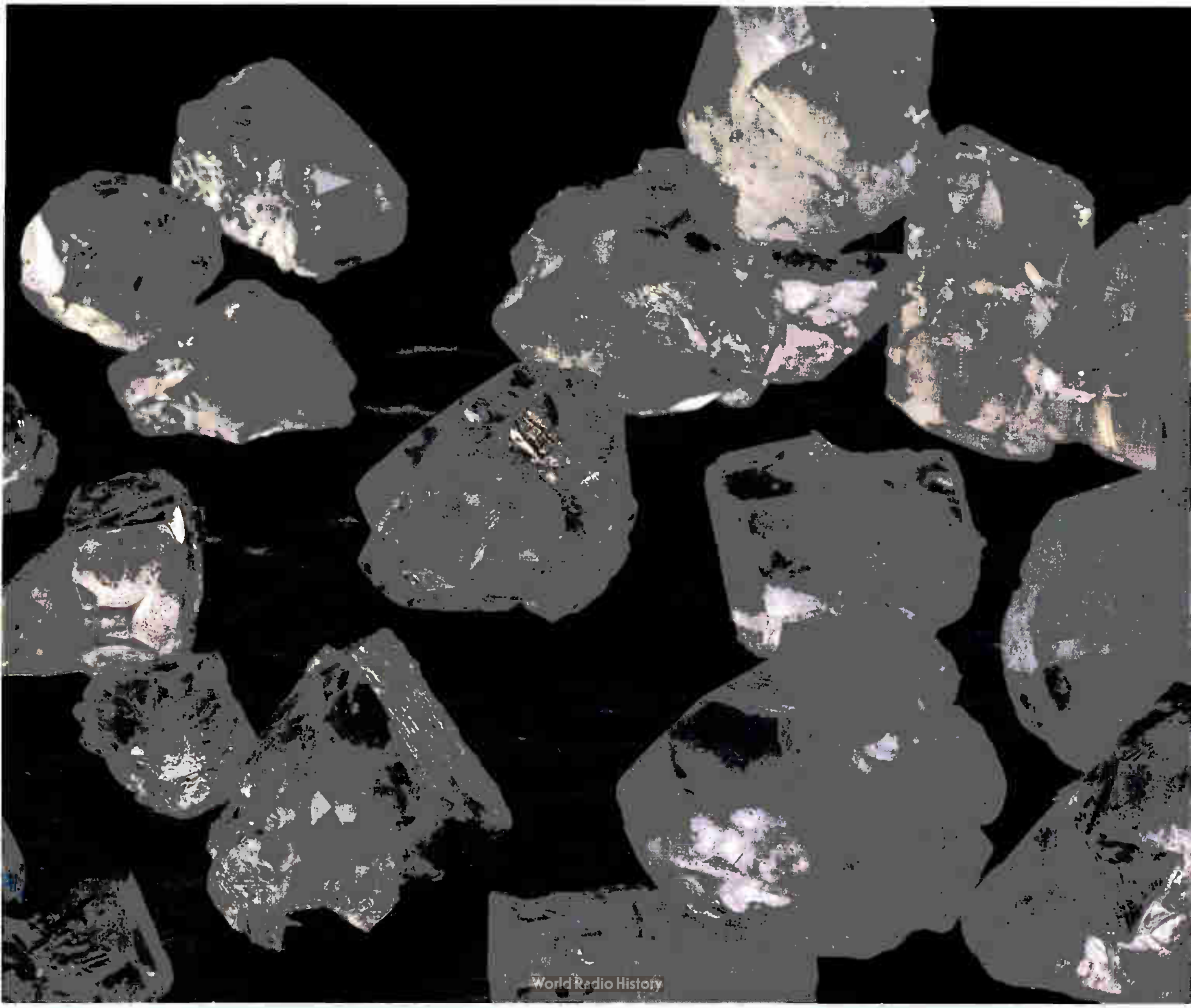

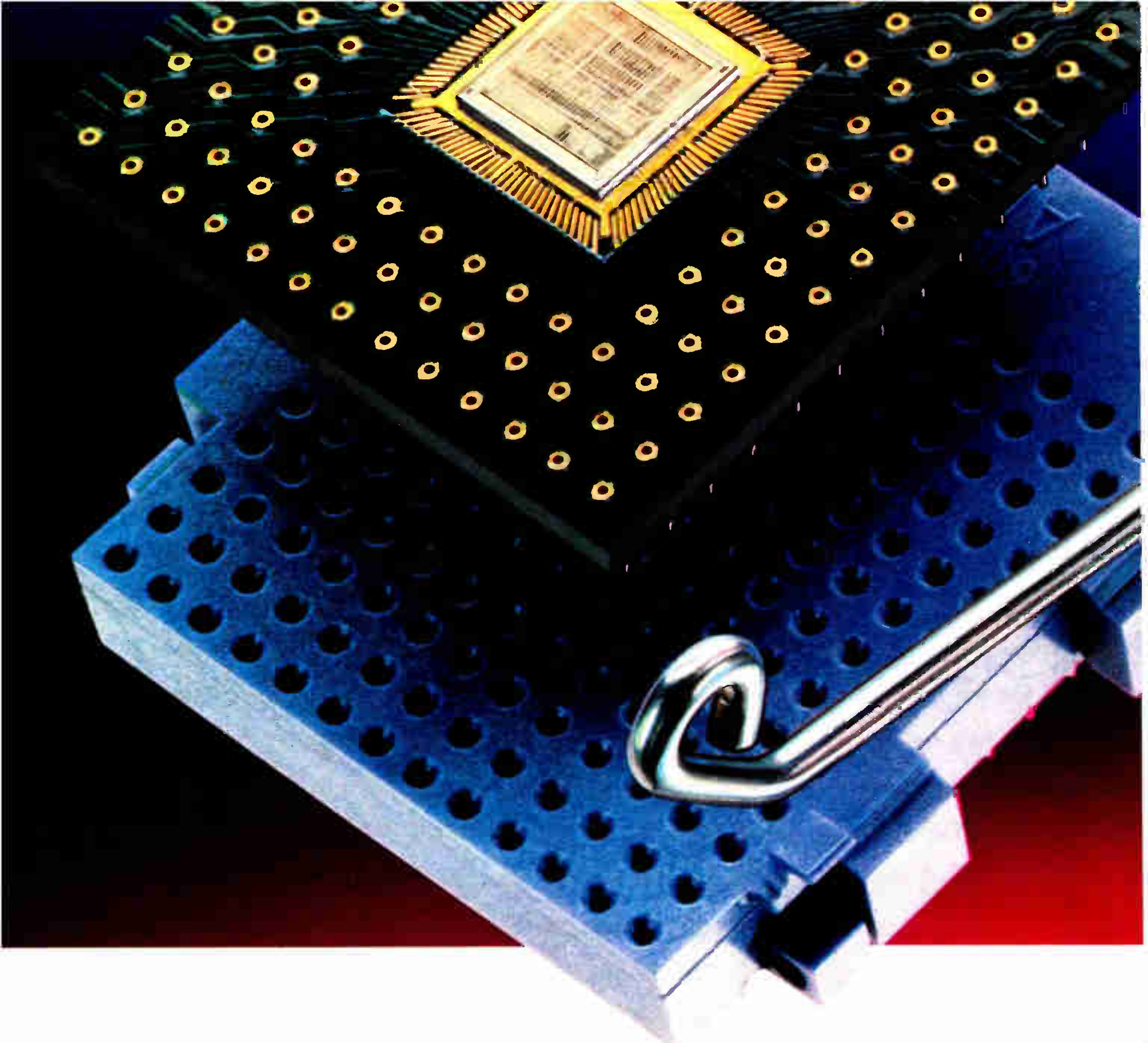

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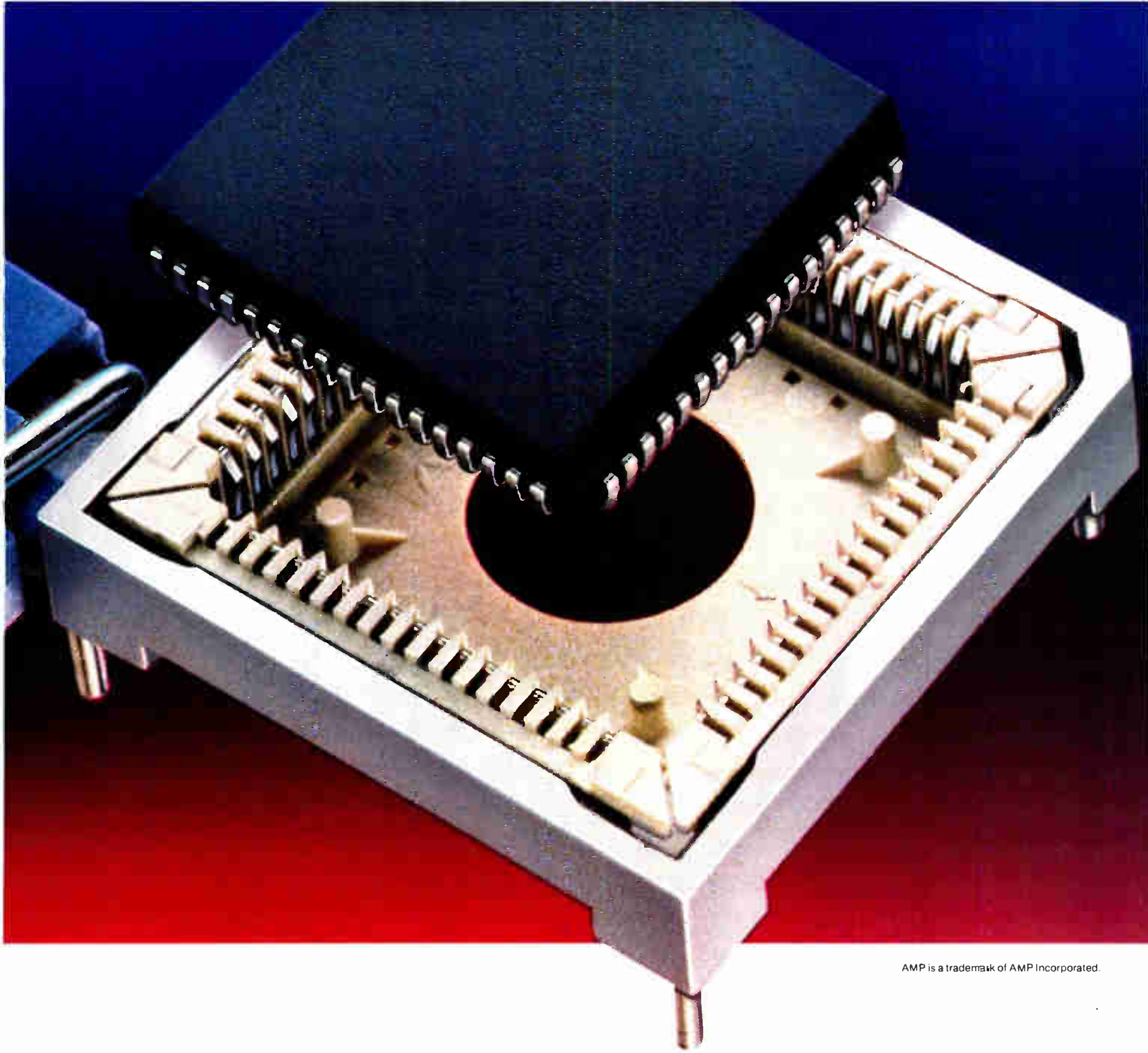

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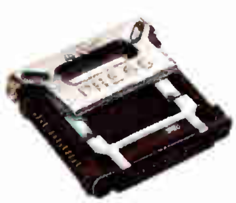

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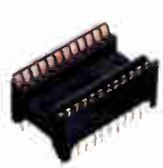


A WORK STATION THAT RUNS UNIX AND MS-DOS SIDE BY SIDE

Convergent Technology's new Ngen 386 work station teams Intel's 32-bit 80386 processor with a fast cache memory to switch operating systems in microseconds

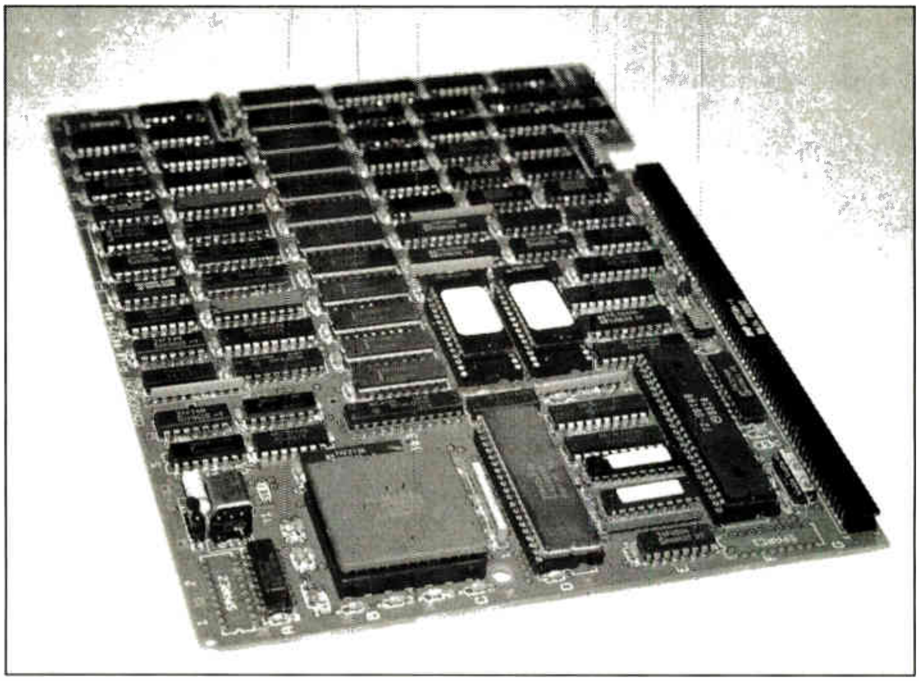
A work station that can shoulder both engineering and office tasks, running programs from two different operating systems side by side, is on the way from Convergent Technologies Inc. Users of systems based on the new Ngen 386 will soon be able to switch back and forth between, say, a UNIX-based design-automation program and an MS-DOS spreadsheet.

The series 386 is the first work station announced that will take advantage of the multiple-execution mode of Intel Corp.'s 32-bit 80386 microprocessor. It represents a significant increase in horsepower for the company's Ngen family of work-station products, all of which are based on Intel microprocessors.

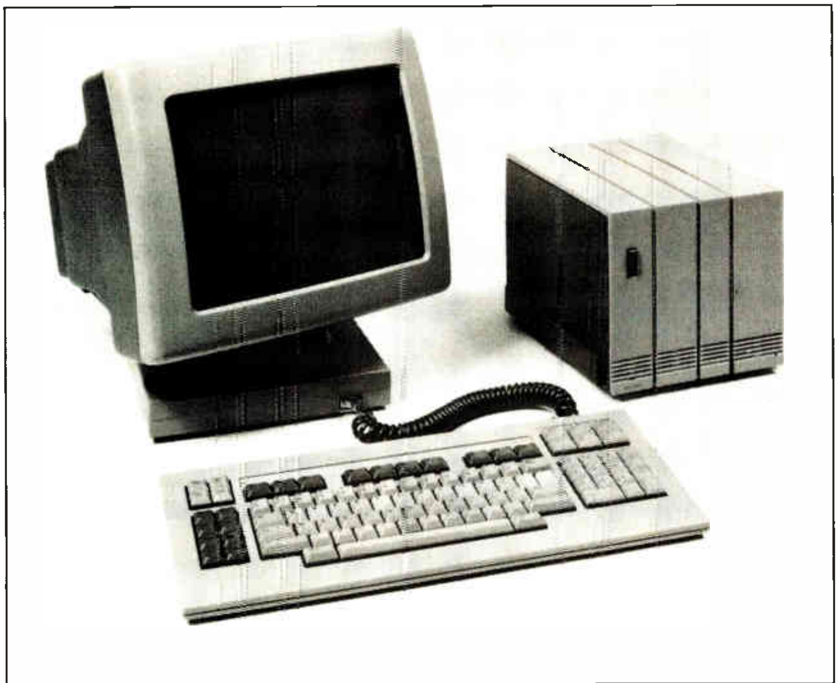
The new model will run Unix System V.3, MS-DOS 3.1, and Convergent's CTOS, a proprietary system for network applications. Initially, UNIX programs have to run independently, but the other two systems can operate together in the multiple-execution mode. "We know we can put together CTOS, MS-DOS, and Unix, but so far no customer has asked for that combination," says Eric Carlson, vice president and general manager of Convergent's Cluster Systems division.

For now, CTOS will act as the host, or base, system, employing MS-DOS as what Convergent calls a transparent assistant to run personal computer programs. "We'll probably have a Unix base with an MS-DOS assistant early next year," Carlson predicts. Although that is just months away, Convergent has plenty of competition that could beat it out as the first to offer this powerful combination. Many software houses are working overtime now on such a multiple-execution operating system because of Unix's widespread use in engineering applications and MS-DOS's popularity in business.

Nevertheless, Convergent expects to be among the leaders into this market, says Kathryn Hanson, the Cluster Systems division's director of marketing. She sees the early hosting of Unix on a fast, 80386-based work station that can also execute MS-DOS programs as Convergent's opportunity to break into such



1. FAST WORKER. Convergent's 386 CPU board includes the 16-MHz 80386 and a 32-K-byte cache built of 35-ns CMOS SRAMs.



2. WORKING TOGETHER. An Ngen 386 can serve as master in a network that includes other family members. Various connection schemes may be used.

markets as computer-aided engineering. "We are talking with manufacturers in the technical-work-station market," Hanson says. Already, a single Ngen machine can do design and cost computations, and in the near future two different kinds of programs will be able to run in adjoining display windows.

Convergent's Ngen work-station family is now used mainly by original-equipment manufacturers as a platform for building office-automation networks. The family includes the series 186 and 286, which have central processing units based on Intel's 16-bit 80186 and 80286 microprocessors, respectively. Now the San Jose, Calif., company hopes to break into new markets, notably engineering applications, with the far more powerful series 386. "We're using the 80386 not for its raw speed as an MS-DOS machine, as personal-computer manufacturers have, but to build new applications bases," says Carlson.

Convergent's search for new application areas goes beyond the Ngen 386 and its target of engineering-system OEMs. The company is scrambling to expand its customer base to make up for a sharp falloff in revenues as OEM sales to office-system makers have plummeted. It plans to build a federation of captive OEMs that can serve as customers for its work stations (see p. 66).

Convergent plans to charge only "a few hundred dollars" more for the series 386 CPU board in high volume than for the series 286 board, says Carlson, so OEMs can offer a 386-based system for only about $1,000 more than a 286-based machine. That will be about $500 less than Convergent's 16-bit coprocessor called the PC Emulator, which is used with Ngen 186 and 286 work stations to serve as an MS-DOS host.

If the Series 386 does as well as expected, the new board (Fig. 1) should take the credit, because nothing else has changed in the Ngen family's modular architecture. Series 286 and 386 models are so alike, in fact, that one can be converted to another in the field by swapping CPU boards. And, the company promises, that upgrade will transform the 16-bit systems into supermicrocomputers more powerful than the speediest PCs and capable of leaping from one operating system to another in microseconds.

Carlson expects MS-DOS users who are thinking of buying new 80386-based PCs to think twice when work stations based on the multiple-execution Ngen come on the market. Putting himself in a user's shoes, he says, "I wouldn't buy a new machine to run my Lotus spreadsheet program faster. I wouldn't pay $1,000 for that. On the other hand, I can now switch between my electronic mail and word processor, or between my mail and my voice processor, in one second instead of five seconds. I do that a hundred times a day and I'll pay $1,000 more to do it faster, you bet." The voice processor, a recently announced Ngen option, turns a work station into a telephone answering machine.

Convergent rates Series 386 throughput at 3 million to 4 million instructions per second, or about as fast as the 16-MHz 80386 can go. Instead of directly accessing dynamic RAM, the new CPU employs virtual memory in an on-board cache built with 35-ns static RAMs and Fast (Fairchild Advanced Schottky TTL) logic clocked at 32 MHz. The cache stores 32-K bytes and reconfigures on the fly to accommodate 16- or 32-bit code. It allows the 80386 to access memory with no wait states 85% to 90% of the time, reports Ngen hardware manager Robert Schopmeyer, who designed the CPU. Unix V.3 has a slightly lower hit rate, because it performs multiuser as well as multitasking operations, he adds.

Schopmeyer says the large, fast cache gives the Series 386 "horsepower to spare." With existing 16-bit software, its performance is about twice Series 286 and four times Series 186 performance, and also four times IBM Personal Computer AT performance, he says. Some programs run even faster than that, he adds. For instance, in a comparison test using Burroughs Corp. CTOS-based office-automation software, the Series 386 scored 2.4 times better than the Series 286 in performance. Also, it runs graphics programs three times as fast. And, Schopmeyer estimates, OEMs can redouble overall performance by recompiling 16-bit programs to improve cache utilization and take full advantage of the 80386's 32-bit capabilities.

To OEMs, Carlson points out, a more important performance measure is how much network growth a master work station can support. A Series 186 master, which handles about 4 to 6 work stations, can be upgraded to a Series 286 model supporting 6 to 12 work stations. In contrast, a Series 386 model can take care of 16 to 24 work stations.

In cluster networks (Fig. 2), masters are work stations that also act as network controllers and servers, as well as gateways to such communications facilities as Ethernet backbone networks and X.25 or IBM SNA (Systems Network Architecture) long-haul networks. Ngen work stations usually communicate within clusters via Convergent's RS-422 and HDLC (high-level data-link control) interfaces, or with such third-party interfaces as IBM token-ring cards. However, a new Telecluster interface allows private branch exchanges to interconnect work stations at lower cost via telephone wiring. New wiring need not be installed, because existing wiring can be shared by voice telephone signals and data transmitted at rates up to 1.8 million bit/s.

Convergent was able to get the Series 386 to market quickly because in 1982 the company's engineers designed the Ngen architecture to accommodate a 32-bit processor, and they developed the new CPU in parallel with the 80386. "Intel designed the chip; we got the first in-circuit emulator and found the bugs," Carlson says. He says the last major problem was fixed this summer after Convergent's implementation of Unix V.3 revealed bugs in the chip's virtual-memory manager. "Intel ran our software, probed the chip, and solved the problem," he says.

The CTOS/MS-DOS combination has also been in the cards for a long time. CTOS was designed for context switching as part of its support for network applications development. A context-switching system can host other operating systems, which allows users to select additional programs through a keyboard instead of rebooting the system to start up a different operating system. A year ago, Convergent employed this function when it added the PC Emulator. When the module is installed, CTOS traps input/output data calling for MS-DOS programs and controls the coprocessing operation.

CTOS employs the same trapping method with the new CPU. However, CTOS and its MS-DOS assistant both run on the same microprocessor now—the 80386. The chip stores program contexts in register banks so that contexts can be switched with a single instruction [*Electronics*, Oct. 21, 1985, p. 50]. With previous microprocessors, register contents had to be shuttled back and forth between memory by time-consuming software routines. But single instructions now execute instead of the routines and, as a result, operations that previously added up to seconds with coprocessors are now performed in microseconds. OEMs can use existing 16-bit software, because all code shipped by Convergent in the past two years was designed to run on the 80386 without change.

Next year, Carlson adds, Convergent will add multiple-execution systems to all its networking product lines, starting in January with a server being developed as a joint project of the Cluster Systems and Network Systems divisions. Dubbed the 386 Server PC, it has a 64-K-byte cache memory and up to 16 megabytes of dynamic RAM—four times Ngen main-memory capacity. In addition to Unix, MS-DOS, and CTOS, the server will host IBM-compatible minicomputer and networking packages. As a server, the system will handle 50 or more PCs and terminals. Although it can also be configured as a multiuser computer or a minicomputer-performance engineering work station, Hanson says the server is primarily intended to be an OEM platform for building PC networks. □

HOW SCHOPMEYER HIT THE 125-NS MARK

"If you had talked about virtual-address space and caches three years ago in the microcomputer world, people would have thought you crazy," remarks Robert Schopmeyer, Ngen hardware manager at Convergent Technologies. "And now here we are with a machine that runs at an overall cycle time of 125 ns. Again, if you had said you could do that in a microcomputer three years ago, people would have thought you crazy."

Schopmeyer, 43, is comfortable with speeds like that. A BSEE from the University of Minnesota, he worked on large computers at what was then Univac Corp. for several years and then designed some 15 minicomputer caches at other companies before he decided to enter the microcomputer world at Convergent four years ago.

Schopmeyer, who designed all three central processing units in the Ngen family, arrived at 125 ns by making sure his designs took advantage of increases in microprocessor speeds. The first, containing the 80186, cycles in 500 ns while accessing main memory built with 150-ns dynamic RAMs; the second, with the 80286, uses 120-ns DRAMs to cycle in 250. The 80386 does it in 125 ns by accessing virtual memory in a cache built with 35-ns static RAMs.

What's more impressive, he thinks, is that all three processors operate in the same system architecture with no problems. When Schopmeyer joined Convergent, the company was planning a new generation of products—the Ngen family—around the 80186. He recalls, "We needed a new system bus, and we had to make sure we would not cripple the bus with some unique 80186 feature and then discover that we couldn't use it in future products." Because Schopmeyer and his fellow "Ngeneers" did their homework, the Series 386 central processing unit runs with astounding performance on that same 16-bit bus and with the same main memory as the Series 286 CPU.

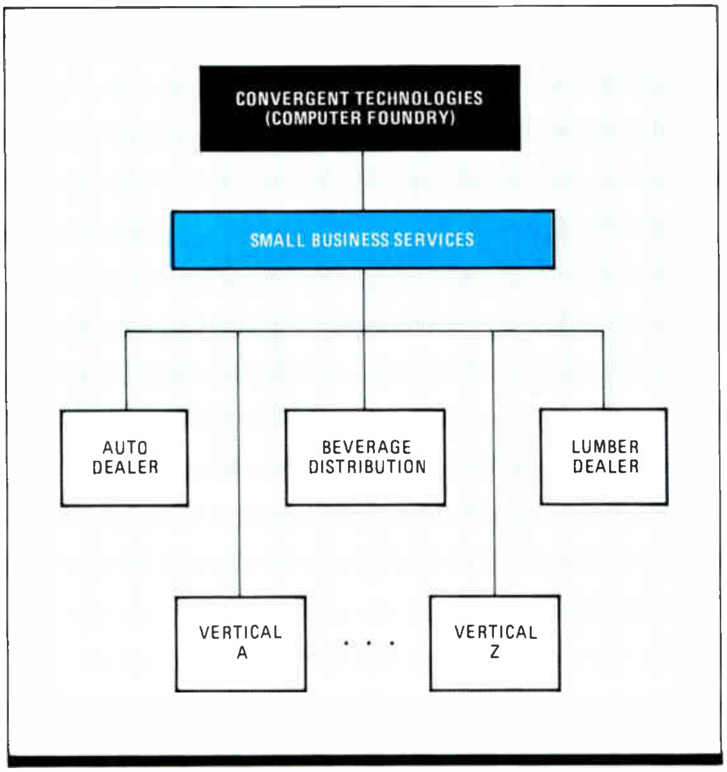
ROBERT SCHOPMEYER

CONVERGENT HUSTLES TO TURN AROUND

For a company that has fallen off a cliff, Convergent Technologies Inc. is showing a surprising amount of bounce. After watching the bottom fall out of its sales and earnings sheets, the San Jose, Calif., company has moved quickly to embark on an ambitious program of acquisitions while simultaneously restructuring itself so as to try to avoid repeating the agonies of the past year.

Company assets now include a war chest of $78 million and a top management team composed mostly of former Hewlett-Packard Co. executives recruited over the past two years. The product lines have been expanded with a series of new machines, most recently with a new model of the Ngen, which is one of the first work stations to employ the Intel Corp. 80386 (see p. 63). And its acquisition program seems to be back on track after last March's embarrassing cancellation of a merger with the network vendor 3Com Corp. The deal was on the verge of being made final when it was torpedoed by 3Com's investment bankers.

The work-station maker is fighting to stem its losses with a new strategy: it is buying small companies offering turnkey systems in vertical markets



NEW LOOK. Convergent Technologies will be a computer foundry; Small Business Systems will manage companies serving vertical markets.

If the bankers believed Convergent had a lot of problems, they were right. The company's sales and earnings were about to take a precipitous slide: in the third quarter of 1986 alone, it lost $25.6 million on sales of $64.7 million—down from a profit of $3.8 million on sales of $117.4 million in the same period the year before (see table, p. 67).

Most of Convergent's problems can serve as a worst-case example of what can happen when most of the corporate eggs are packed in a few baskets. Started in 1979, the company hit more than $360 million in sales in 1984, largely on the strength of contracts to supply work stations to AT&T, Burroughs, NCR, and a few other large original-equipment manufacturers. When Burroughs and then AT&T sharply reduced their purchases, Convergent was in deep trouble.

But the company was already attempting to diversify by means of the 3Com deal. President Paul C. Ely, 53, lured from HP to help wean Convergent from its dependence on large OEMs, wanted access to 3Com's strong dealer base. For its part, 3Com saw in Convergent a convenient anchor against the day when networking companies would need strong connections to computer makers.

Ely didn't get what he wanted, but Convergent did end up with one new asset—John Celii, 44, 3Com's chief financial officer, who had already begun working with Convergent in anticipation of the merger. Celii, a 20-year HP veteran before joining 3Com, has now become the point man in Ely's plan to rebuild the company: he is the vice president and general manager of the new Small Business Services Division, which is, in effect, buying its customers. The aim of the novel approach is a federation of companies that deliver business-automation packages—built around Convergent computers, the company hopes.

The recruting of Celii was only part of an effort by Ely to bolster Convergent's management. The most recent addition was Cyril Yansouni, also 44 and another HP veteran, who was brought in last month to head the company's manufacturing arm. He worked closely with Ely for 17 of his 19 years at HP, most recently as president of the Personal Computer Group. With Yansouni's appointment, Ely has the elements in place for a new Convergent.

"We are in the middle of a substantial transition," Ely says. "We have our original business as a computer supplier, with 1,400 employees mostly in California; and meanwhile, in the past two months we have added new businesses with more than $100 million in revenue, involving thousands of customers and another thousand employees. I felt very strongly that there was enough activity in this company to keep two of us very busy."

To emphasize the structure of the new company, Ely wants to form a new unit, called simply Convergent, that will have Convergent Technologies and the Small Business Services unit as subsidiaries. Convergent Technologies, under Yansouni, will build and service computers for a growing stable of OEMs and value-added resellers; Small Business Services will manage a federation of companies that provide turnkey solutions in vertical markets. A formal change will require stockholder approval, but that is how Convergent is supposed to be running today.

Despite those ambitious plans, Convergent must still contend with a sluggish computer market and increased parts costs. The company recently had to lay off 500 employees. In such an environment, Convergent must rebuild and diversify its stricken OEM program and simultaneously develop a new growth path in a novel form, the federation of subsidiaries.

To shore up the OEM business, Convergent will add 30 to 100 salesmen in the next 18 months. The company is embarking on an ambitious program of adding 10 new VARs and one small OEM each quarter, and one major OEM a year. Yansouni will run the manufacturing operation—what the company calls its "computer foundry"—that fuels this effort.

The foundry will still provide the bulk of Convergent's sales until well into the 1990s, Ely says. During that period, Small Business Services is to grow carefully, looking for core members that are in well-protected markets, profitable, and in need of advanced technology. It is to have revenues of $300 million by 1990.

A typical Small Business Services core company will have a good grip on a market that requires special expertise and is too small to attract IBM Corp. or Digital Equipment Corp., says Michael M. Murray, vice president of business development for the unit. Each core company will have experienced management and its own sales, service, and support. However, it will still need technology, Murray says.

Convergent has already acquired three companies: Display Data Corp. of Hunt Valley, Md., which supports auto dealers, lumberyard wholesalers, and beverage distributors; Open Systems Inc. of Minneapolis, an accounting specialist; and Digital Systems Inc., a Pensacola, Fla., vendor of systems for accountants and contractors. These initial federation members are not even Convergent users; Display Data, for instance, is presently committed to DEC. It may

CONVERGENT'S DRAMATIC DROP

Quarter ending	March 31	June 30	September 30
Sales ($ thousands)			
1985	$ 92,616	101,119	117,398
1986	73,469	50,090	64,740
Earnings ($ thousands)			
1985	$ 206	2,454	3,851
1986	1,893	(5,101)	(25,693)

SOURCE: CONVERGENT TECHNOLOGIES INC.

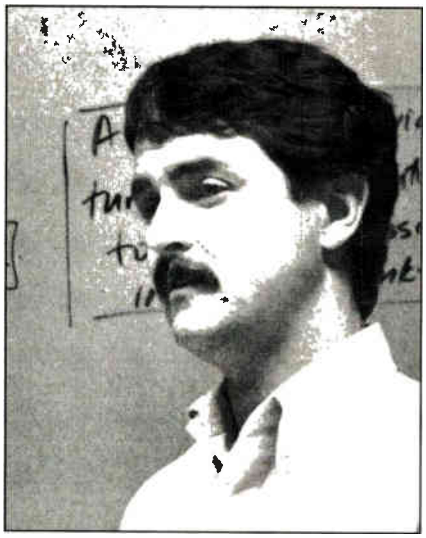
take several years, Murray concedes, to start selling Convergent equipment to Display Data customers.

To convert the customers, Small Business Services will talk margins. Typically, Meyer says, VARs get a 30% to 35% discount, give it all to their customer, and take a profit on their application alone. As a volume supplier, Convergent can up the discount to as much as 50%.

And while waiting for hardware sales to materialize, Small Business Services will derive income from hardware and software support, leasing, and supplies and services. In fact, Murray says, only 30% of the unit's income will come from hardware.

Some analysts question the new strategy. Bruce Lupatkin of Hambrecht & Quist Inc., San Francisco, cautions that by taking an equity position Convergent may cause its federation members to lose credibility with their customers. "VARs are supposed to have a free hand in selecting hardware and software," he points out.

But Ely is committed to 100% ownership of federation companies, and with Yansouni on board, he is ready to start pushing that strategy harder. "I am going to spend most of my time making sure that Small Business Services succeeds," Ely says. "Cyril will make the money, and I will spend it." *–Clifford Barney*



MURRAY. His business-development job is to help build a federation of vertically oriented turnkey business-automation firms.

YANSOUNI. A new arrival from Hewlett-Packard, he will be in charge of the manufacturing operations of Convergent Technologies.

THE SKY IS NOT FALLING IN THE ATE WORLD

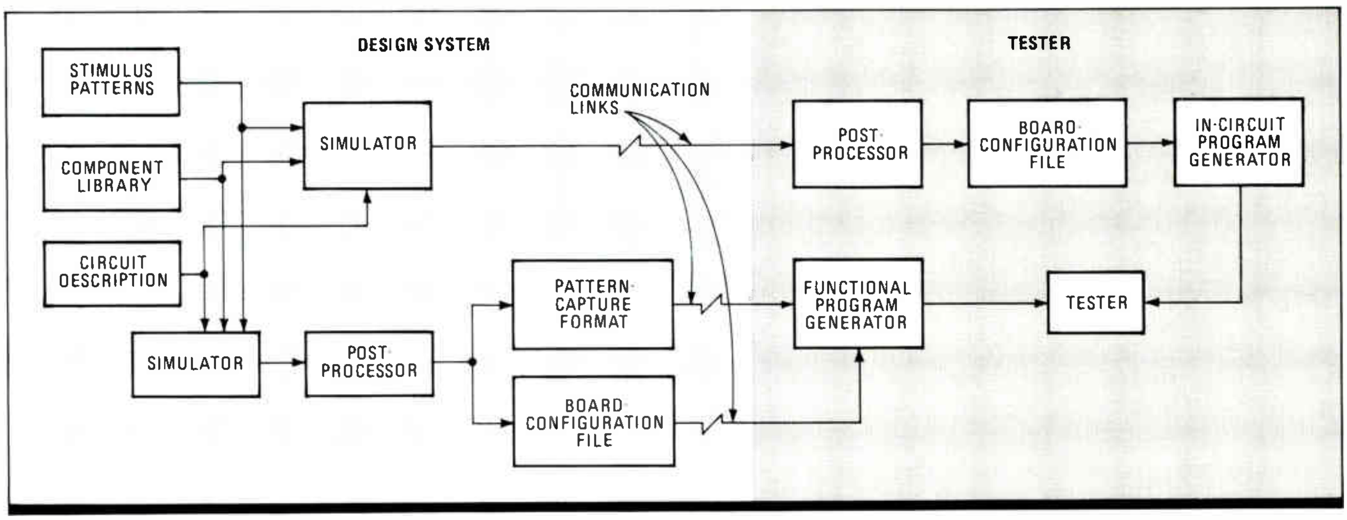
Test-equipment makers are showing they can deal with what doubters said would be insurmountable problems in testing ultracomplex VLSI chips

by Jonah McLeod

The Chicken Littles of the tester world have long warned that the sophistication of complex new integrated circuits would outstrip the abilities of automatic test equipment. But ATE makers are moving fast to deal with the problems presented by printed-circuit boards laden with complex application-specific integrated circuits, 32-bit microprocessors, and highly sophisticated components.

The doomsayers have been warning that ATE makers face three nearly insurmountable problems in testing these large, complex boards: how to create the millions of test vectors needed; how to apply the test vectors to the board under test without having to break down large disk files into smaller segments that must be loaded into the tester's pattern random-access memory one at a time; and how to apply these patterns to the board fast enough to keep pace with the increasingly faster IC components used on these boards.

But ATE manufacturers are wrestling successfully with these three roadblocks. To address the first problem, they are beefing up fault simulators to handle the larger test patterns now needed to test boards. In addition, they are linking board testers and computer-aided-engineering systems (Fig. 1). Another important source of added muscle is software postprocessors used to access vectors generated by the simulators at the design stage and to convert them into test patterns. Also, some test systems are using the



1. CONVERSION. The test patterns created during the design of a pc board laden with complex ICs can be a source of test vectors for production-line ATE.

microprocessor and associated self-test programs found on most new boards to generate the patterns needed to test the rest of the board.

To tackle the second problem of applying the flood of test vectors, some new board testers use large RAMs to hold the larger test patterns. Others contain microprocessors or sophisticated memory-switching circuitry directly at each pin to generate some of the large patterns needed to test complex very large-scale ICs on the fly.

To solve the third problem of speed, manufacturers are building higher-speed test systems capable of applying patterns at up to 80 MHz. These systems can keep pace with the faster high-speed microprocessors and VLSI components on these boards.

To perform these tests, users are leaning toward functional and combinational testers, says Raj Rajaratnam, a market analyst at Needham & Co. in New York who follows the ATE industry. These customers need functional testers and combinational testers, which contain both functional and in-circuit test capability. Only functional and combinational testers can ensure with almost 100% certainty that the board is operating properly. As a general rule, in-circuit testers find more than 80% of the faults found on most pc boards. Functional testers find most of the remaining faults.

Rajaratnam says that functional and combinational tester sales of $250 million worldwide in 1985 are expected to grow at a 20% to 25% rate over the next five years. By contrast, in-circuit testers accounted for a larger $315 million in sales in 1985, but he says they will grow at a more modest 8% to 10% in the next five years.

SAVING ON SOFTWARE

Of the three problems confronting functional and combinational testers handling large pc boards, the time required to generate test programs for large pc boards is the most acute. "Over the next five years the cost of generating software will be 20 times higher than the cost of hardware in the overall ownership cost of a tester," says Marshall Bates, the national sales manager for GenRad Inc. in Concord, Mass.

One solution to the test-generation problem is concurrent simulators. Conventional simulators create a fault in a pc-board model and then generate a test pattern aimed at finding that fault. Concurrent simulators go an important step further: they evaluate the test pattern to determine how many other faults the test pattern can find.

"The ability of simulators to create test patterns for more complex pc boards results partly from the development of concurrent simulators, which can efficiently generate large numbers of test patterns," says Joseph B. Lassiter, who is the vice president and general manager at Teradyne's Manufacturing Systems Division in Boston. Version 6 of the company's Lasar simulator has turned this machine into a concurrent tester.

Computer Automation Inc. of Irvine, Calif., is another company with a new concurrent version of its fault simulator. Computer Automation estimates that fault-simultation time can improve fourfold by using concurrent simulators along with other aids to test-program generation, such as algorithmic pattern generation using the microprocessor behind each pin and the use of existing patterns from the design system.

To turn out software that can handle the hard-to-model new chips, ATE makers are developing concurrent simulation and are adding hardware models of the new ICs

Others selling software to aid test-equipment manufacturers, such as HHB Systems Inc. of Mahwah, N. J., are beefing up their simulators by adding models of new, complex, hard-to-model VLSI components to libraries used for simulating boards. During board simulation, the company's Computer Aided Test Systems modeler is plugged into the work station or simulation engine that applies a set of inputs to the hardware model during a simulation run. It then responds correctly to the software simulation.

Teradyne has developed its own set of hardware models to accompany chips that do not now have software models. The D300, a set of hardware models of microprocessors and other complex chips, has a software shell around the device that allows the part to be used for fault simulation. The shell takes patterns of 1s and 0s applied to the input pins of the hardware models and determines which input signals are meaningful for the test and which are don't care signals. "By eliminating the unused signals, the pattern can be applied to the hardware model and a meaningful response sent back to the fault simulator so it can proceed with its job," says Lassiter.

GENRAD'S BATES: The cost of creating test programs can be 20 times the cost of the system's hardware.

The vectors created during the design of a pc board are another source of test patterns for functional and combinational testers. GenRad claims to be the only ATE vendor with a complete solution for getting data from CAE systems into the ATE in usable form. Its HILO high- and low-logic-level design simulator provides a software data base for the HiPoste software postprocessor, which converts the patterns for use in fault analysis. "With the ability to make immediate use of the simulator output, test generation is three to five times faster than generating test patterns from scratch," says GenRad's Bates.

TERADYNE'S LASSITER: Super-big vector memories let testers handle extremely long test patterns in one pass.

In accessing test patterns from a design system, the net list, parts list, and simulator test vectors are entered into the test system in a number of different ways, most commonly by magnetic tape or an RS-232-C communications link, with the faster GPIB bus and Ethernet less commonly used. A postprocessor on the tester or a work station tied to the tester converts simulator data into appropriate test vectors in what Hewlett-Packard Co. calls a board-configuration file for an in-circuit portion of a combinational tester.

Depending on the sophistication of the system, the postprocessor can also produce what HP calls the pattern-capture format file for simulator data used by the functional portion of a combinational tester. This is a format in which the data can be converted into a form usable by a variety of different manufacturers' testers.

HP is lobbying other test-system vendors and trying to drum up support among test-system customers for a standard pattern-capture format for the data coming from the design system. A standard format will ease the task for the postprocessor.

While some manufacturers have addressed the problem of test-pattern generation at the simulator, others are using the microprocessors found on most new boards coming onto the market to solve the problem more economically. "Of all the boards currently on the market, 60% contain a microprocessor with an associated bus on board," says Craig Pynm, who is the vice president of marketing at Zehntel Inc., a Walnut Creek, Calif., company. "What's more, nearly all pc boards currently being built are bus-based boards with one or more on-board microprocessors."

One popular solution to test generation is a technique called bus-cycle emulation that capitalizes on the self-test programs built into on-board microprocessors

Besides having a microprocessor, most of these boards come with a built-in self-test routine that runs on board power-up. A technique called bus-cycle emulation that takes advantage of these on-board test programs is found on the 3200 functional test system from Zehntel.

With the 3200, the test system clips over the microprocessor and in most cases holds the reset line of the microprocessor at a constant reset level. This puts every pin of the microprocessor into a three-state, or high-impedance, condition. With the microprocessor in a permanent three-state condition, the tester also replaces the self-test routines in read-only memory or programmable ROM on the board with its own program code, consisting of either the board's self-test program or test patterns created to test the board.

"In this way, the stimulus test vectors are applied from inside the card and propagate out to the edge connectors," says Don Cassis, director of marketing at Support Technologies Inc. of Beaverton, Ore., which uses bus-cycle emulation in its model 2000 board tester.

"What the 2000 offers is a low-volume board tester for about a tenth the cost of a larger high volume system," says Cassis. A bed-of-nails test head can be added to probe at critical nodes in order to verify correct operation.

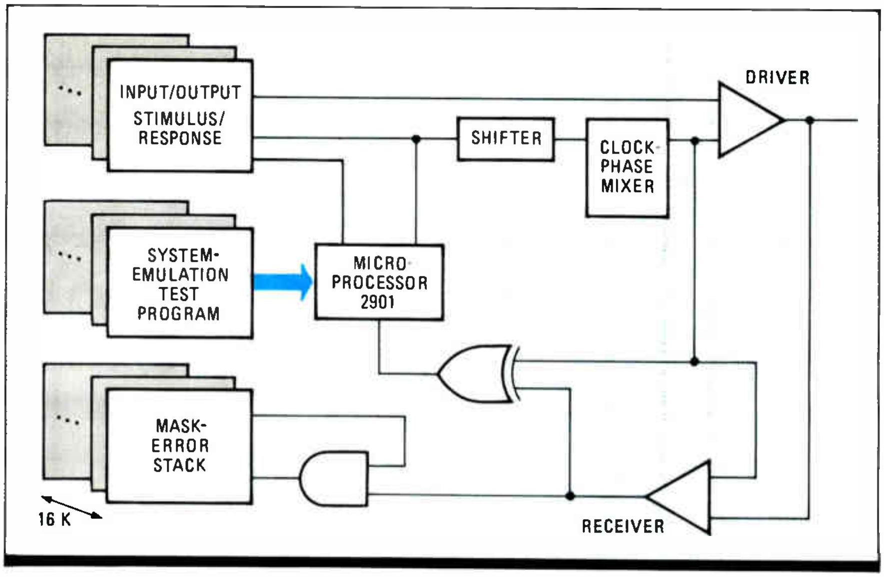
Critics of the bus-emulation technique complain that the patterns used for testing are designed only to ascertain if a board is operating, not to find faults. They claim that the lower cost is achieved at the expense of longer troubleshooting times. Bus emulation proponents say that, because the technique makes use of test patterns generated during the design of the board, it is more cost-effective than patterns generated by fault simulators.

A functional and combinational board tester must confront the problem of how to apply large test programs to the board without repeatedly reloading the disk memory to accommodate the entire set of patterns. "Good ASIC designs typically have built-in level-sensitive scan-design circuits to improve testability," says Lassiter. "These devices require a large vector memory to contain megabytes of test vectors."

Teradyne has solved the problem on its L290 combinational tester by backing each test channel with up to 32-K by 4 bits of pattern RAM. "The tester's large channel-memory capacity enables it to execute the extremely long test patterns required in testing complex VLSI boards," Lassiter says. Also, the tester uses a digital command processor to access test patterns from the memory of the test system computer, a Digital

Equipment Corp. MicroVAX II. The patterns are moved into the channel memory at a fast 500,000 vectors p/s, using a direct-memory-access technique.

Another memory solution is offered by the HP 3065 AT combinational tester from HP's Manufacturing Test Division in Loveland, Colo. It boasts the ability to provide 67 million vectors to the device under test because it has three different memories. The system has a vector memory 256 bits wide by 2-K deep. Each address contains a unique vector. An 11-bit-by-64-K sequence RAM behind the vector memory defines the order in which each address in vector memory is to be applied to the device under test. Behind the sequence RAM is yet another memory called the directory RAM.



2. ON THE FLY. Microprocessors in Computer Automation's Ironman tester generate patterns on the fly as specified by the simulation emulation test program.

The sequence RAM can be divided into several sequences. The directory RAM then can specify a sequence of sequences to be applied to the vector RAM. The multiplier effect results from the sequence RAM being able to use the same vector many times during a test run. A similar capability is found on the model 750 combinational tester from Factron Schlumberger of Latham, N. Y.

To handle the large numbers of patterns required, other functional and combinational testers are adding intelligence to each pin to create patterns on the fly. In addition, these systems are using the memory more wisely.

An example of adding more intelligence to the pin is found in Computer Automation's Ironman functional tester (Fig. 2). "We use a technique called system emulation test," says David Brock, marketing analyst at the company. "Behind each tester pin there is a 2901 bit-slice microprocessor." In addition to executing the test patterns stored in memory, the microprocessor on each pin can generate a pattern by executing an algorithm. This capability is especially useful in testing ROM and RAM on a board.

The microprocessor can also monitor the response from the board under test on the fly and detect any error conditions as they occur at a 10-MHz rate. This means that a test that might require several stimulus patterns to finish can be halted immediately after an error is detected, rather than waiting until the sequence is completed.

Being able to produce enough test patterns to test the new generations of ICs means that testers must apply stimuli and receive responses at speeds at which the board normally operates. To handle the high speeds of the coming generation of ASICs and commercial VLSI components on pc boards, the new functional and combinational testers are much faster than earlier models. For example, the 750 tester from Factron Schlumberger can apply a clock signal to a board at a 50-MHz rate and can send a stimulus signal to and receive a response from the board at a 30-MHz rate.

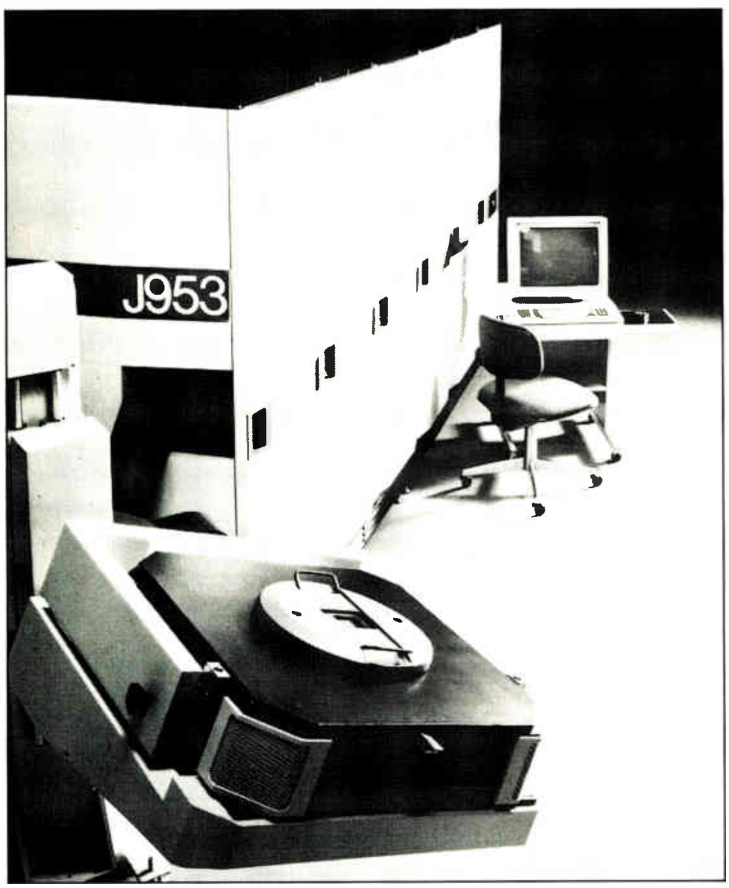
Teradyne's L290 board tester accommodates 1,152 channels each operating at 40 MHz. For even faster operation, two channels can be multiplexed together to provide an 80-MHz channel. To ensure proper line terminations for bidirectional signals at data rates up to 80 MHz, the tester's three-state driver switches a programmable terminating voltage to the driver's output when in a three-state condition. The three-state driver also contains a 50-Ω resistance that can be selectively switched in or out of the driver's line as needed.

To handle the high speeds of the coming generation of ASICs and VLSI parts, the new board testers are pushing their data rates to as high as 80 MHz

With the trend toward functional and combination testers expected to continue for at least the next five years, there will be a continued effort to address the three major problems confronting these systems. ASICs and standard ICs are growing in size, so even larger test patterns will have to be created to test pc boards containing these components. The patterns must somehow be contained in the tester and applied to the board without requiring long test times. And finally, faster microprocessors and other VLSI components will continue to push testers' data rates even higher than the 80-MHz maximum found on most testers today. □

TERADYNE'S TESTER FOR TOMORROW'S VLSI

With a 50-MHz data rate, system accuracy within 250 ps, and a huge memory capacity, the J953 provides up to 4 million vectors per pin to test complex VLSI chips in one pass



1. GENTLE GIANT. Teradyne's new J953 VLSI test system is huge and runs at test rates to 100 MHz, yet its very high accuracy is extremely repeatable.

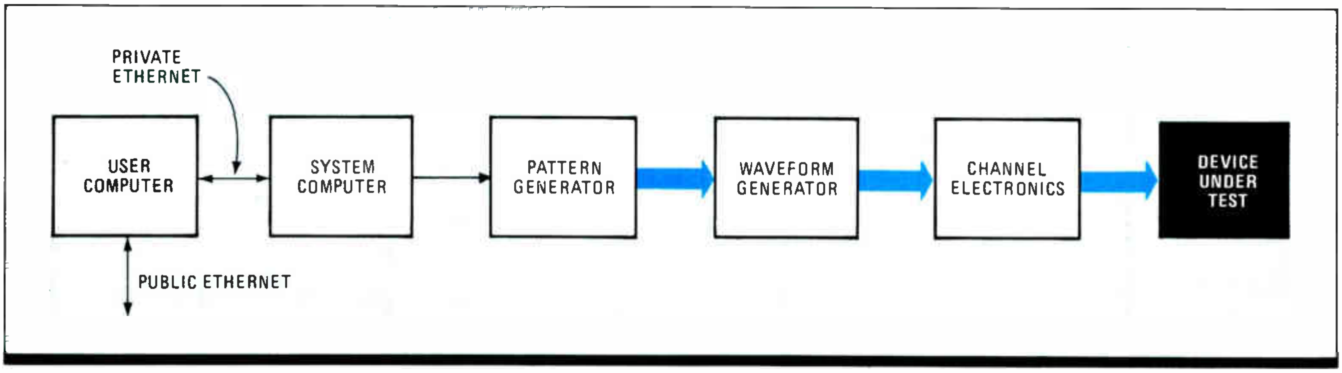
Teradyne Inc.'s new J953 test system, armed with exceptional accuracy, high speed, and large test-pattern capacity, is ready to tackle the toughest challenge facing integrated-circuit testers. It can check out the next generation of superfast, complex very large-scale ICs built in 1.25- to 1.5-μm technologies, and it can do it without slowing down production cycles.

To tackle this job, the J953 boasts 256 channels with an unrestricted data rate of 50 MHz on all channels, or 100 MHz with channel multiplexing. That speed, coupled with system accuracy within 250 ps, gives it sufficient performance to handle the next VLSI generation, where, for example, 32-bit microprocessors will end up as cells in application-specific ICs. The J953's huge pattern-memory capacity enables it to provide as many as 4 million vectors per pin to test complex VLSI chips—in one pass, without reloading.

Teradyne reports that signal edges arrive at the input/output pins of a device under test with a system accuracy of ±250 ps from any pin to any other pin, even when changes in vector timings and formats cause edge positions to shift rapidly. "It's not too difficult to hold 250 ps from cycle to cycle when test patterns stay the same, but the J953 does it everywhere, every time, with the signal edges shifting from cycle to cycle," says Wayne Ponik, VLSI product manager at Teradyne's Semiconductor Test Division in Woodland Hills, Calif.

Other high-performance testers take an hour or more to calibrate themselves, says Ponik. But the J953 (Fig. 1) takes about five minutes to calibrate all channels all the way out to the device pins, he claims. Accuracy is high because the designers built the timing generators with emitter-coupled logic gate arrays and fought to remove picoseconds of error in circuitry, Ponik says. Calibration is fast because the timing circuits are so linear that all programmable timing points can be calibrated with a single adjustment controlled by an algorithm.

Test vectors stored in a pattern memory flow through a waveform generator and then into the channel electronics that drive the device under test (Fig. 2). A pin-sliced architecture, with independently programmable timing generators and a measurement unit in each channel, allows



2. TWO COMPUTERS. The J953 has the same basic two-computer architecture as its predecessor, the J967, but now each channel has independent, rather than shared, electronics. Channel data rates can be as high as 50 MHz, or twice that with multiplexing.

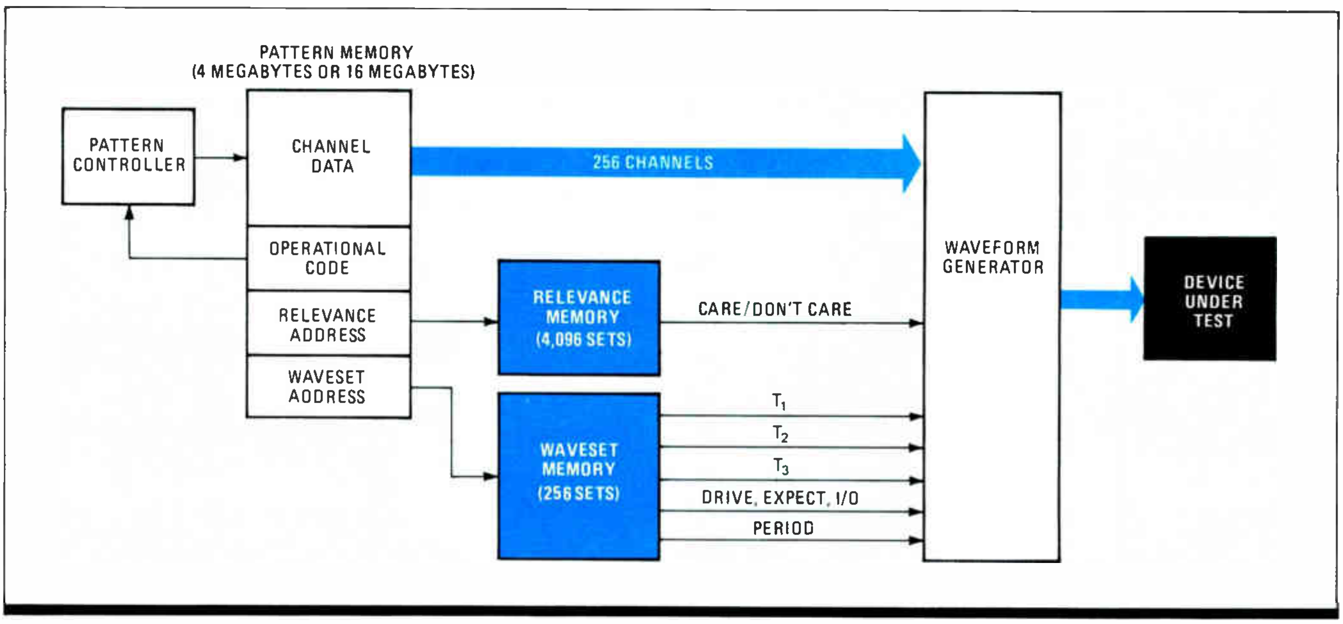
channels to be grouped in any way desired. The measurement units provide the voltage and current levels needed to test not only bipolar and CMOS circuits with conventional I/O signal levels, but also chips with analog-signal inputs and outputs, mixed-technology devices with bipolar and MOS segments, and digital circuits with such odd I/O levels as pseudo-ECL.

Edward Ostertag, J953 hardware engineering manager, designed the tester's timing generators with 100-ps resolution so that test vectors could be programmed at that resolution to emulate sloppy, skewed signals and wavering, asymmetrical clocks. A T_1 timing point marks the beginning of a cycle, and a T_2 point marks the end. A third point, T_3, switches signals from input to output. These edges can be moved around and through the signal period in 100-ps increments to aggravate the device under test. Ostertag says this makes the J953 ideal for such tasks as determining the sensitivity of embedded microprocessors to timing variations and ensuring that reduced-instruction-set microprocessors can execute an instruction every clock cycle.

Few ICs need million-vector test patterns now, but, Ponik points out, longer and longer streams are being used for sequential scan-path testing of standard devices with serial I/O functions, such as microprocessor peripheral chips. To produce such streams, the pattern generator works with a memory that stores up to 4 million vectors per pin, compared with at most 1 million for previous VLSI test systems. The pattern memory, built with 256-K-bit dynamic RAMs, is expandable to 16 million vectors per pin with 1-megabit DRAMs.

The J953 can be programmed to repeat test patterns and sequences more than 64,000 times. Also, an ECL memory that reloads on the fly stores 256 wavesets. Each waveset provides vector timing and formatting information for 256 channels, and any of the wavesets can be used in a test cycle. Moreover, test engineers can program microprocessor operation codes, build nested loops, and pass parameters from one subroutine to another during tests. The system uses masks (programmable data patterns) to deter-

3. PATTERNS PLUS. With a 4-megabyte pattern memory, expandable to 16 megabytes, plus separate relevance and waveset memories, the J953 can easily rerun design simulation tests.



mine whether devices pass or fail tests. Up to 4,096 mask sets can be stored in a relevance memory and accessed randomly during tests.

"You could argue that this is more capability than you need to test a 10,000-gate array, and I would not fight that argument," Ponik concedes. "On the other hand, the ASIC market is moving quickly toward cell-structured, high-density devices. People are already talking about using the 80386 [Intel Corp.'s new 32-bit microprocessor] as a cell, and it contains more than 250,000 transistors."

Besides, Ponik adds, circuit designers are developing longer sequences to simulate more-complex designs on computers. With big pattern, waveset, and relevance memories available, engineers can simply download simulation test patterns to the J953 to test the actual chip (Fig. 3). With a small pattern memory, patterns would have to be reformatted and run in pieces loaded from a disk drive, so the tests would take longer and would not exactly duplicate the simulations. The J953's three memories are partitioned to cater to scan-path testing and simulator organizations. Also, its system software runs on a Unix operating system compatible with that of many ASIC-design systems. So, Ponik says, "You can get a test program on the air very quickly."

For interactive testing of new designs by circuit engineers, the J953 features a logic-analyzer-like mode. With a mouse, the engineer points to test and parameter selections in screen windows to set up a test run. The system can trigger upon a programmed event or upon a test pass or failure, and then display test data or timing and voltage waveforms.

Ponik doesn't expect the J953 to be everyone's cup of tea. He recommends it for production testing of ASICs with feature sizes in the 1.25-to-1.5-μm range and for such difficult-to-test standard products as microprocessor peripherals. He recommends the 192-channel, 40-MHz J967 VLSI Test System for microprocessors and for ASICs in the 1.5-to-2.0-μm range. In price, performance, and architecture, the J953 takes up where the J967 leaves off. It costs from $1.1 million to $2.5 million, depending on the number of channels and test stations.

Like the J967, the J953 is a dual-computer system with a private Ethernet for communications between the two computers and a public Ethernet for communications with other systems. One computer controls testing; the other serves as a test-programming work station, logs data, communicates with other systems, and such. Both are 32-bit Sun Microsystems Inc. work stations, but the J953 uses the newer and more powerful Sun 3 model.

However, everything else in the system architecture has changed radically. With the J953's new pin-sliced architecture, channels no longer share timing generators and measurement units, so that each channel's timings, driver levels, comparator levels, and dynamic load levels are individually controllable. To serve ECL and other high-speed devices, pin capacitance was cut from 80 pF on the J967 to 30 pF on the J953 without increasing impedance, which remains at 50 Ω.

The J953 also has two system timing generators that distribute up to 16 clocks at frequencies to 125 MHz, two system measurement units that deliver high voltages and currents to the channels through relay and field-effect-transistor switching matrices, and facilities for ganging channels to test such large analog cells as 12-bit analog-to-digital and digital-to-analog converters. Without this flexibility, many ASICs would need two different testers or test heads, and accuracy might be compromised, Ponik notes. □

OSTERTAG GETS HIS KICKS 'DEALING WITH PICOSECONDS'

Big as they are, VLSI test systems are still instruments, and so the instrument designer's traditional goal, of making each new design more accurate than the last one, still applies. Teradyne Inc.'s J967 tester, which preceded the company's new J953, was one of the industry's most accurate, with a skew error of only ±375 ps from one pin of the device under test to any other pin.

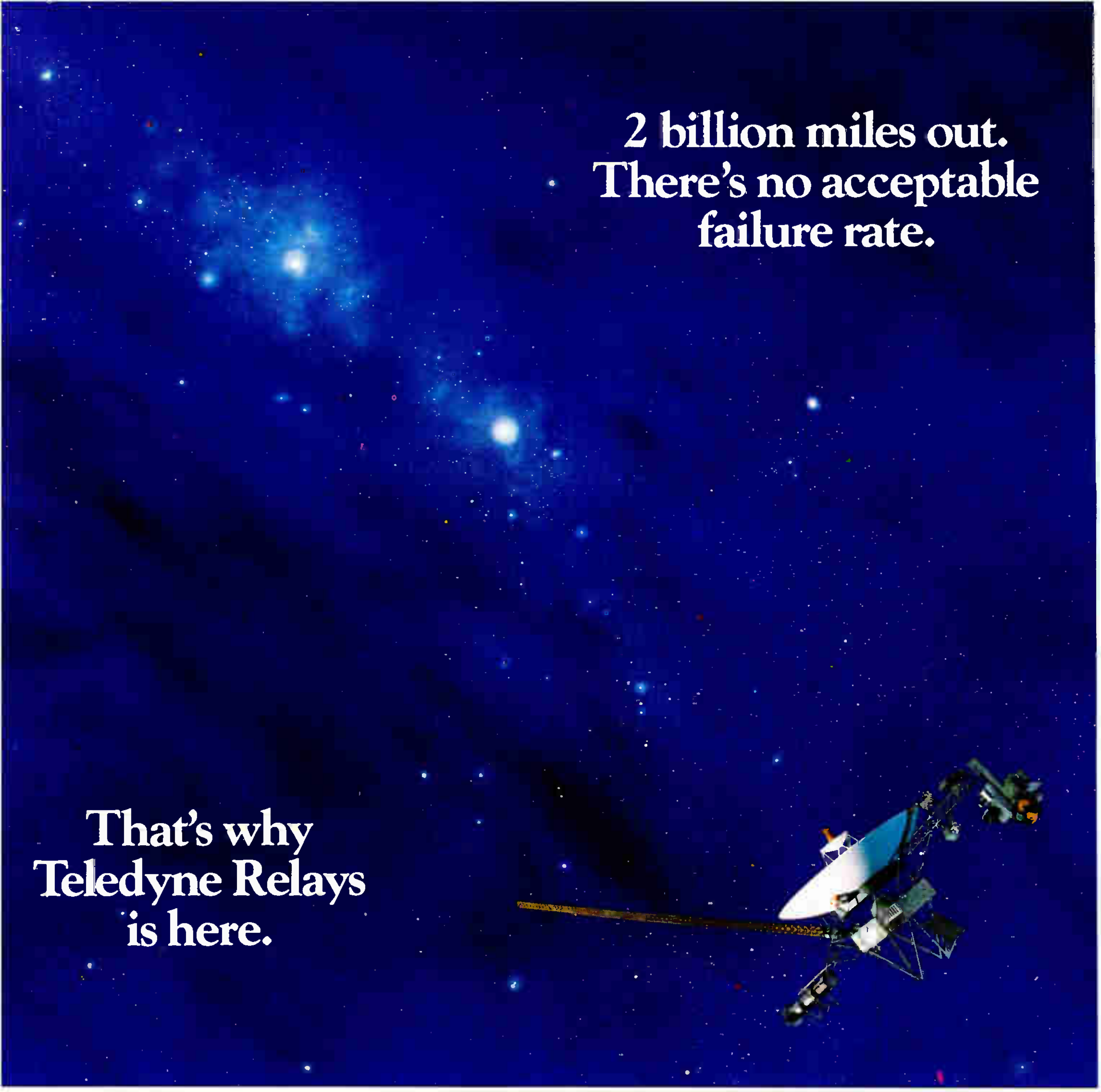
But the J953 cuts another 125 ps from that error, says Edward Ostertag, J953 hardware engineering manager. And this new level was reached, he adds, because "we pulled out all the stops, considered every possible way that errors could be introduced, and then designed every part to save picoseconds."

Ostertag, 37, designed the 100-ps-resolution timing generators that make this accuracy possible. "Dealing with picoseconds has always been my area of interest," he explains. "To me, designing the most accurate system is the biggest challenge and the most fun. Then, when the system is being debugged, the part that I enjoy the most and put the most personal effort into is getting the system running and then measuring the accuracy."

ALL THE STOPS. Ostertag (l.) and Ponik tightened circuitry to shave error to a minimum.

Teradyne has paid Ostertag to have fun since 1976, when he joined the company to work on logic testers with 10-ps resolution. He has been designing VLSI test systems since 1979, and he started the J953 project in 1983. Ostertag earned his BSEE degree at the University of California at Northridge.

The business side of the J953 project was the responsibility of Wayne Ponik, VLSI product manager for Teradyne's Semiconductor Test Division. Ponik, who declines to state his age, has worked at Teradyne in marketing and product-management positions for 15 years. He received his BSEE from Worcester Polytechnic Institute, Worcester, Mass., and his MBA from Santa Clara University, Santa Clara, Calif.



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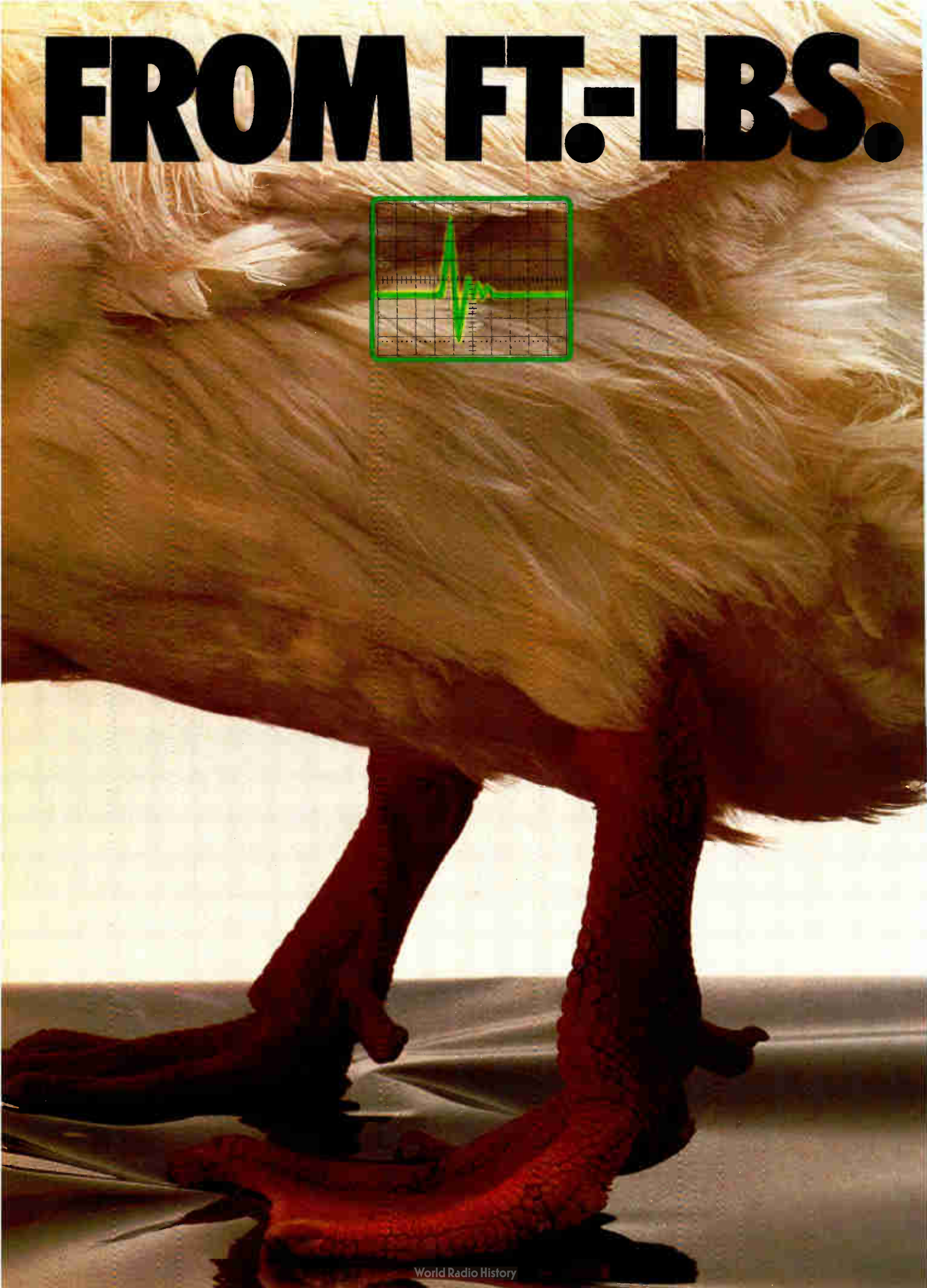
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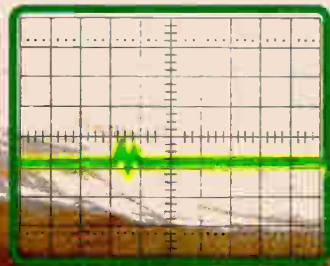

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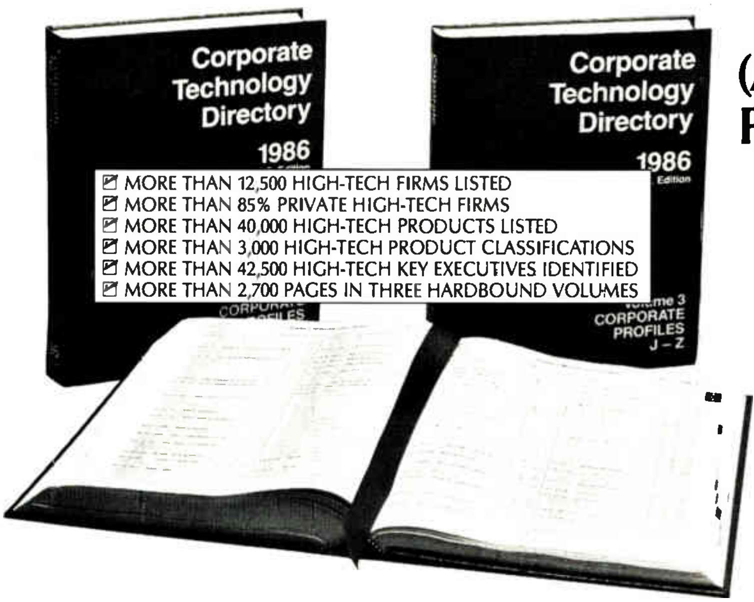

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HOW TO BOOST FLOPPY-DISK CAPACITY TO 11 MEGABYTES

Konica's advanced head-positioning system gets a ninefold capacity increase in standard 5¼-inch floppy disks with embedded servo data added to them

Floppy-disk drive technology is making a bold leap ahead in the KT-510 drive from Konica Inc. The new drive from the Sunnyvale, Calif., company boosts capacity a dramatic ninefold over standard floppy-disk units by overcoming three problems that dog any attempt to boost track density: the inability to position a read/write head accurately over tightly spaced tracks, disk-centering misalignment, and disk deformation. And the KT-510 uses the standard floppy disks that have been restricted to 96 tracks per in. and 1.2 megabytes of storage.

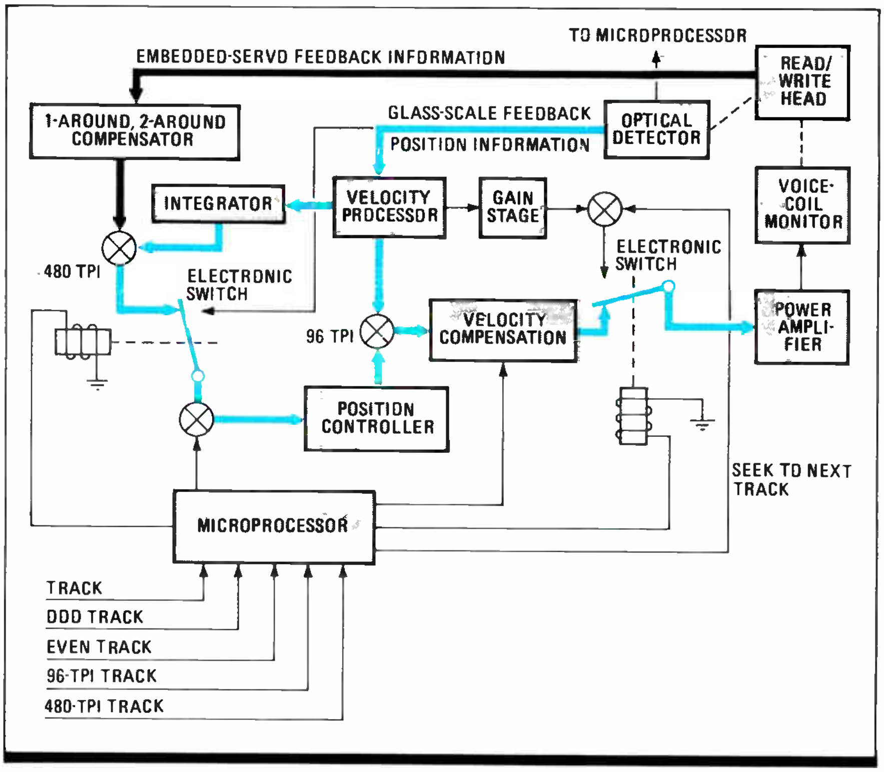
"The drive can store 10.9 megabytes (formatted) on a standard 96-tpi 5¼-in. floppy similar to the one used on an IBM PC AT or compatible computer," says Richard Freedland, director of business and marketing for Konica. The KT-510 [*Electronics*, Oct. 16, 1986, p. 137] only requires that the PC floppy be written with embedded servo data. This adds only 5¢ or 10¢ to the cost of each floppy. The KT-510 will cost less than $400 in volume.

With this low-cost means of storing 10.9 megabytes, floppies can now be used for backing up as much as 40 megabytes of Winchester storage and for distributing large software packages, such as AT&T Bell Laboratories' Unix operating system, large application programs, and data bases. Konica hopes to make the floppy as a medium of exchange of programs and data for the IBM PC AT and for advanced systems such as those based on the 80386 microprocessor.

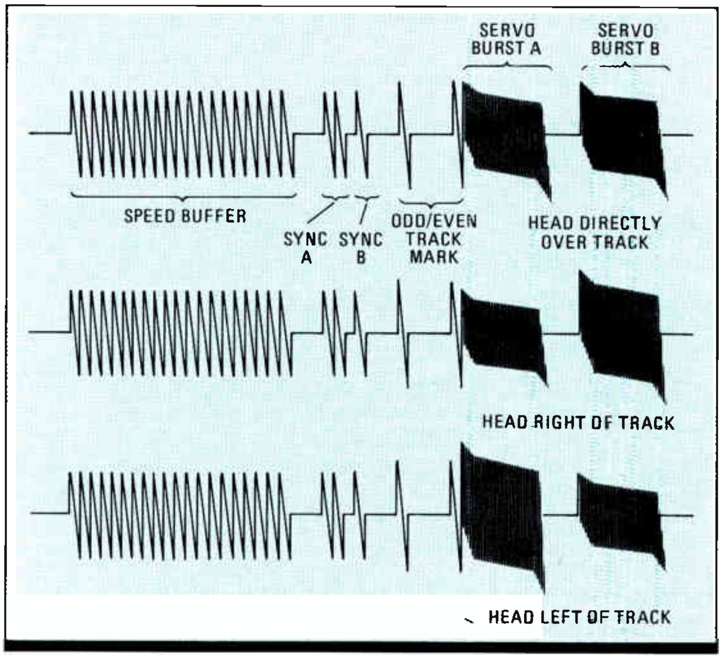
The new floppy writes five 2.083-mil tracks at a density of 480 tpi. They take up the same space as one 10.415-mil-wide track in a 96-tpi floppy. To achieve this, the drive is required to keep its head, with its narrow 20-μin. gap, centered precisely over the thin 2.083-mil-wide track. The result is a head that can write and read at 480 tpi and also can read 96-tpi floppies.

Three design elements give the drive its critical technical edge. Two closed-loop servo systems position the head precisely over the track. A special circuit compensates for disk-centering misalignment and disk deformation.

One of the servo systems is an



1. TWO LOOPS. The KT-510's optical loop positions the head over the desired track, and an embedded servo loop keeps it at track center.



2. TRACKING DATA. The embedded servo uses the amplitude of the two servo bursts to control the position of the head.

optical loop that provides coarse continuous feedback to the actuator controlling the read/write head's position. It locks the head in a circular path over the disk surface and prevents vibration from moving the head.

But this system has no way of determining how accurately it is positioned over the narrow track center. So a second servo system corrects the coarse position to keep the head directly over the track center. Embedded servo data prerecorded between every sector of each track on the disk surface provides fine-positioning feedback 61 times with every revolution of the disk.

LOCKING ON A TRACK

The coarse servo (Fig. 1) uses an optical detector assembly consisting of a single light source on one side of the drive frame and three optical sensors on the other. Between the light source and the sensors is a glass scale affixed to the actuator arm that moves the read/write head. Two of the sensors detect the intensity of the light as it passes through the scale's divisions, and the servo's electronics use that information to adjust the head's position.

On each side of the glass scale is an alternating pattern of opaque and transparent squares, with the opaque squares on one side of the glass covering the transparent squares on the opposite side. The overlap is not exact, so the light from the source can pass through to the detectors at the edges of the opaque/transparent overlap. The scale is designed so that an edge occurs only where a track can be written on the disk surface.

As the actuator arm travels in a given direction, the amount of light passing through the glass goes from zero to a peak, and then back to zero, forming a triangular wave signal. "If there were only a single sensor, it would not be possible to determine if the read/write head were moving inward to the disk center or outward," says Alex Moraru, senior staff engineer at Konica. "So we use two sensors separated by 90° of the triangular wave." The sensors produce two identical triangular waveforms with a 90° phase difference. They ascertain the direction of the head by examining which waveform is leading and which is lagging.

A third sensor is mounted on the same side of the drive frame as the position sensors, but it does not receive light though the opaque-transparent pattern. Rather, it monitors a separate, clear part of the scale for variations in the light source's output. In this way, it detects degradation in the light's intensity due to aging of the source or dust buildup on the glass scale. This data can be used to adjust the reading from the other two sensors.

When a drive is seeking a track, the microprocessor controlling the drive will switch a drive signal to the power amplifier and the voice-coil motor in order to move the head. Because the continuous-feedback optical loop provides a constant indication of the head's location on the disk surface, the microprocessor can apply a large drive signal to move the head quickly to the desired track.

Once the head reaches its target, the optical loop locks the head on track with a feedback signal from the optical detector through the velocity processor and velocity compensator to the power amplifier. Head movement to either side of the track is immediately detected as a positive or negative velocity change, and the velocity processor and velocity compensator apply a correction signal to the power amplifier, which moves the head back on track.

Once the two optical sensors have indicated that the drive has reached the desired track, the second servo loop controlling fine positioning becomes active as the read/write head begins reading servo data between the track sectors. The embedded servo data is sent through the 1-around, 2-around compensator position controller and power amplifier to the motor to adjust the head position.

When the embedded servo data is not present, continuous-velocity data detected by the optical detector moves through the velocity processor to an integrator and into the embedded servo loop at the position controller. This continuous feedback locks the head in place until the next burst of data arrives from the embedded servo loop. In addition, the locking action allows the drive to be tilted at an angle not possible with other floppy-disk drives: ±30°, according to Freedland, as opposed to the ±5° specified for most other high-capacity disk drives.

The embedded servo data appears 61 times a revolution and is what the read/write head detects first as it comes up on a data sector. The servo data (Fig. 2) begins with a speed buffer zone alerting the system that the positioning data is coming up under the head. Next appears a pattern of sync pulses, followed by a signal that tells the head whether the track is odd or even. Then comes the actual positioning information: servo bursts A and B for the left and right sides of the track, respectively. The first synchronization pattern, sync A, is 4 bits long (four alternations) and synchronizes the capture of servo burst A. Sync B, the second pattern, is 2 bits long and does the same for servo burst B.

Any misalignment of the head increases or decreases the amplitude of one servo burst relative to one another. Any amplitude difference is applied to the voice-coil motor to move the head back on track.

IN ALL KINDS OF WEATHER

There is one other control circuit inside the servo system that ensures the system's ability to recover data written at the 480-tpi track density. It is the 1-around, 2-around compensator, a special circuit to compensate for disk-centering misalignment and disk deformation. This circuit continually compensates for deformation due to temperature and humidity and for misalignment due to improper disk centering.

The drive is specified to operate between 0°C and 50°C and between 5% and 90% relative humidity. Temperature and humidity can turn a round track into one that is elliptical in shape. The ellipse causes a track misalignment twice per revolution. To the servo system, the deformation appears as a sine wave oscillating at a 20-Hz rate. Disk-centering inaccuracy can produce a head that moves on and off the track center at a 10-Hz rate with the disk turning at 600 rpm.

To compensate for the elliptical deformation of the disk, the 1-around, 2-around compensator increases the servo loop gain at a 20-Hz rate. To compensate for disk-centering inaccuracy, it makes a separate gain adjustment at a 10-Hz rate.

Such extreme measures to ensure proper track positioning accuracy and to adjust the drive to accommodate a flexible media that can stretch and deform with each revolution give Konica a drive that can store 10 megabytes on an inexpensive 5¼-in. floppy disk. "We see a 20-megabyte, 5¼-in. floppy a couple years in the future," says Freedland. "But it will have to use special high-coercivity media, which by then should be more readily available." □

KONICA SWITCHED PLANS ON THE WAY TO ITS 11-MEGABYTE DRIVE

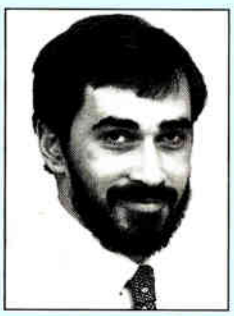
Developing the KT-510 10.9-megabyte floppy-disk drive took Konica Technology Inc. down a different path than originally planned. "Our parent company, Konishiroku Photo Industries Ltd., has been involved in magnetic-media development for over 10 years," says Richard Freedland, director of business and marketing for the Sunnyvale, Calif., company. "Two and a half years ago, it decided to develop a disk-drive product that would use its advanced magnetic storage media." But instead, Konica wound up using standard media coupled with an advanced head-positioning system.

The Japanese company formed its wholly owned U.S.-based subsidiary in December 1984 and hired Akihiro Nishimura, who came to the U.S. from Japan 26 years ago as a Fulbright scholar and has remained ever since. When Konica hired him, he was director of research and development with Ampex, where he had helped set up a joint venture between the two companies to make consumer video and audio tape.

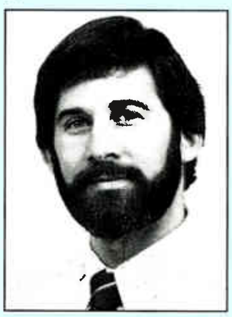
Nishimura decided it was possible to build a high-capacity floppy drive that could use off-the-shelf media—commonly found on IBM PC ATs and all 3½-in. microfloppies. The key would be a head-positioning system so precise that it could read and write tracks only a fifth the size of the typical track. And that would give a ninefold density increase on the standard media.

"The company had already developed a prototype by the time I joined them in April 1985," says Freedland. "When I came on board, Aki asked me to do a business plan on the new floppy product that assumed we could store more than 10 megabytes of formatted data on a conventional 5¼-in. floppy disk."

AKIHIRO NISHIMURA



ALEX MORARU



RICHARD FREEDLAND

Alex Moraru, the company's senior staff engineer, joined Konica in June 1985. Like Freedland, he had been at Epelo, the disk-drive subsidiary that Xebec Corp. had just finished absorbing.

"I had been designing the servo writer for the Epelo drive before I left," Moraru explains. "I had been offered a job with Xebec building other servo writers, but when the Konica project came along, the thought of building a servo that would enable a floppy to store over 10 megabytes sounded more interesting and challenging."

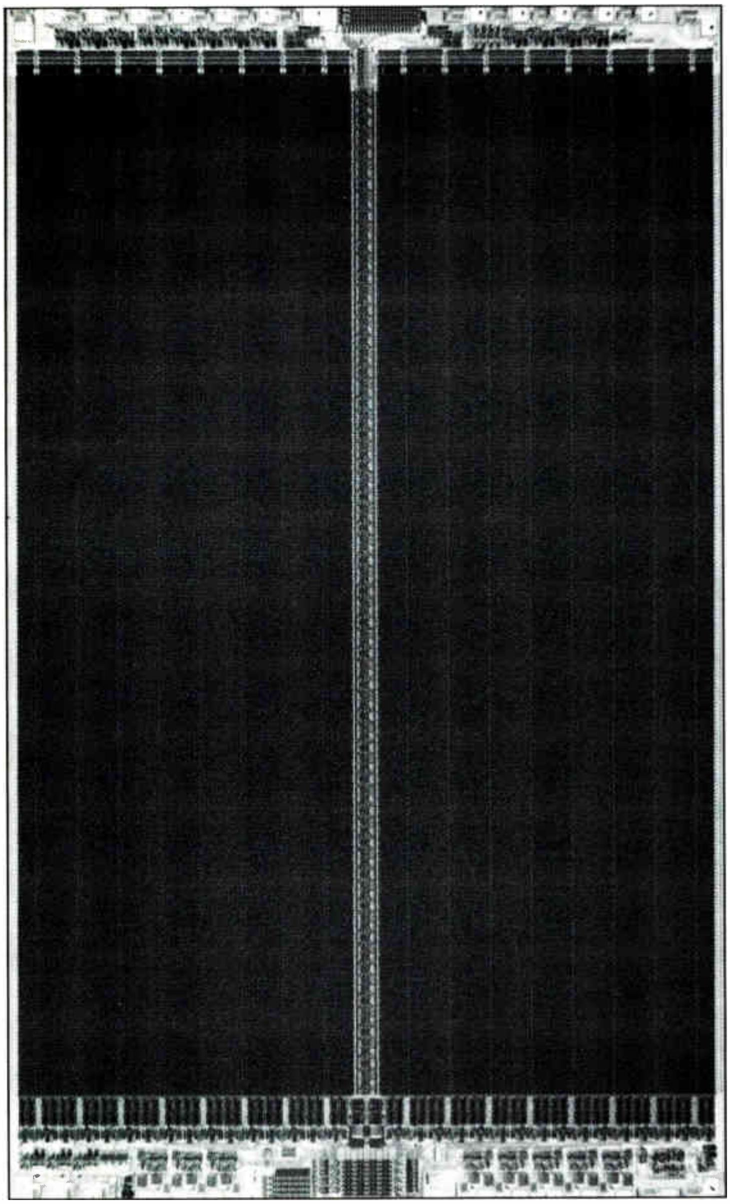
Moraru's group made several changes to the prototype Konica drive. "We improved the design to remove restrictions on data throughput," Moraru says. "We also changed the positioning system to increase the data integrity of the unit and at the same time made the drive much more manufacturable."

With the drive ready to roll off the production line in the first part of next year, Freedland and Moraru are busy with support projects. Freedland is drumming up support for the 10-megabyte floppy disk as the next industry standard, and Moraru is putting the finishing touches on a $30,000 servo writer with which floppy manufacturers can write the servo pattern on each floppy.

AMD 256-K CMOS SRAM REACHES BIPOLAR SPEEDS

Makers of 256-K static random-access memories are going all out to boost their parts to the 35- to 45-ns access times of 64-K bipolar SRAMs. Advanced Micro Devices Inc., for one, is pushing its CMOS expertise to downscale its chips. The Am99C328 SRAM also incorporates aggressive transistor design.

AMD uses such advanced processing techniques as double polysilicon gates, lightly doped drains, dual metal interconnections, and surface planarization. At the architectural level, innovations in the Am99C328 include twin wells, a novel redundancy scheme, the use of precharging by address transition detection, and a two-stage differential amplifier technique. Now available in sample quantities, the 32-K-by-8-bit Am99C328 has an active power dissipation of 400 mW (125 mW standby).



The Am99C328's die size is 114,000 mils^2. The chip boasts a 1.2-μm critical dimension for the n- and p-channel polysilcon gates, equivalent to 1.0- and 0.9-μm effective channel lengths, respectively. At such small geometries, however, designers at the Santa Clara, Calif., company found such second-order effects as hot-electron injection and associated breakdown phenomena. Hot-electron injection occurs when some electrons gain enough large-energy potential from the channel electric field to be injected into the oxide, creating traps and defects in the oxide and at the silicon-dioxide-silicon interface. These traps and defects change the electrical characteristics of the CMOS devices, shortening their lifetime.

To ameliorate such problems, AMD process engineers added a lightly doped n-type region between the heavily doped source and drain and the channel regions. As a result, some of the drain voltage is applied across the lightly doped region, reducing the channel electrical-field strength and the number of hot electrons. The lifetime of the transistor structures is then greatly extended; in fact, it takes more than 100 years for hot electrons to reduce the saturation current by 2%.

REDUCING RESISTANCE

An important factor in the Am99C328's speed is an aluminum/molybdenum silicide double-metal interconnection system that reduces the resistance of the interconnection line and the RC time delay. However, achieving the fine line patterns for the interconnection required that the AMD designers also incorporate a surface planarization step. For this, they opted for a simple etch-back technique that provides good interlayer dielectrics for isolation, good metal-step coverage and reliable device characteristics, all important in a dual-metal interconnection system.

Another problem was electromigration, the transport of metal ions through the aluminum conductor, resulting from the passage of direct current. So AMD designers opted for a layered structure in which molybdenum silicide acts as a barrier to the migration of electrons, extending the lifetime of the interconnection 10 times over that of the aluminum/polysilicon structures used in current devices.

At the architectural level, basic memory-cell size is a major factor in achieving high densities in memory designs. In SRAMs, the critical factors

SPEEDY SRAM AMD downscaled its CMOS process to produce the 256-K Am99C328 SRAM with a 35-ns minimum access time.

in cell size are contact and pitch. In the Am99C328, contact size has been reduced from 2 μm to 1.4 μm, and pitch size has been relaxed from 4 μm to 3 μm. To make up for the possible increase in cell size, the number of contacts has been reduced, for example, by sharing common-source and collector-supply voltage contacts among four adjacent memory cells, resulting in a cell size of no more than 173 μm^2.

To improve reliability, AMD designers incorporated twin-well structures to increase alpha-particle immunity and reduce latchup. To improve yield, they incorporated a unique SRAM redundancy scheme similar to that in dynamic RAMs. In the Am99C328, the spare elements are incorporated so any point defect at any transistor location can be repaired by any spare row or column. And further, a defective spare row or column can be replaced with another spare row or column.

Two polysilicon fuses are used in each spare element. When a spare element (row or column) is not used, both fuses are conducting, which disables the spare element. If the enable fuse is blown, the spare element is then activated. When this spare is selected, a control signal will be sent by the redundancy circuit to quickly disable the regular word line so there is no significant signal contamination between the spare and the regular cells. If the enabled spare is defective, the disable fuse can be zapped, and the particular spare element is deactivated. □

TECHNOLOGY TO WATCH

LATTICE OPTS FOR CIRCUIT INNOVATION IN FAST SRAM

Lattice Semiconductor Corp. is charting its own course to achieve the same 35- to 45-ns access times that AMD is targeting for 256-K static random-access memories. The Portland, Ore., company emphasizes architectural innovation in a new family of 256-K SRAMs that also features state-of-the-art MOS processing.

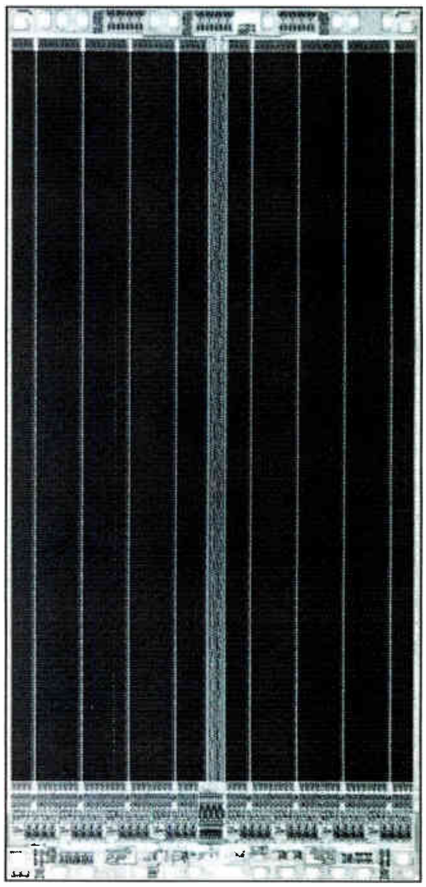
Lattice is scheduling the 256-K-by-1-bit SR256K1 (Fig. 1) for sampling early next year; the 64-K-by-4-bit SR256K4 and the 32-K-by-8-bit SR256K8 will be available later. It says its recent financing woes [*Electronics*, Oct. 30, p. 19] won't affect the schedule. The family is fabricated using a double-level aluminum, single-polysilicon 1-μm n-well n-MOS/CMOS process in which an extra n-type diffusion well is produced with a smaller p+ diffusion well within it. Active power dissipation is 450 mW; on standby, it is reduced to 100 mW.

To achieve 256-K densities in a 100,000-μm^2 die, the Lattice device combines an n-MOS array of six transistor SRAM cells measuring 180.6 μm^2 (8.6 by 21 μm) with peripheral circuitry that is 80% CMOS and 20% n-MOS. To achieve the 35-ns access times, Lattice engineers have employed an array of circuit-design techniques that include a divided word-line architecture, a modified-address-transition detection scheme, use of a bootstrapped column-decoder select signal, and a distributed chip-enable technique.

The basic architecture of the internal n-MOS array is organized into eight sections (Fig. 2), only one of which is activated at any one time, using a divided word-line technique. Each row has a common second-metal word line connected to eight NOR gates which can activate a local polysilicon word line. The NOR gate selected is determined by the column decoding, resulting in short word lines with minimum delay times. To further reduce delay, the sense amplifiers are duplicated in each section, reducing parasitic loading on data lines from the array decoding logic.

Further speed improvement is achieved by using a modification of the standard approach to address-transition detection in which two parallel time-delayed paths and a wired-OR gate are used to compare address signals. The standard approach introduces additional time delays into the speed path. To overcome these delays, Lattice incorporates a steered latch, using the race conditions of the latch to provide the inputs to the NOR gate that generates the address-transition-detection signal. In addition, the n-MOS input transistor has been replaced with a CMOS TTL structure with built-in hysteresis, allowing the standby current to be kept low while specifying TTL input levels.

Also contributing to the enhanced performance of the Lattice device is the use of a column-decoding circuit that bootstraps the output of the decoder signal above the collector supply voltage, eliminating the voltage drop across the enhancement MOS



1. ANOTHER WAY. In building its 256-K SR256K1 SRAM, Lattice emphasizes architectural innovation over scaling.

FET structure used to pass the signal from the decoded column to the sense amplifier. The result is a more highly biased input signal that allows the sense amp to operate 10% to 15% faster without significantly increasing signal levels.

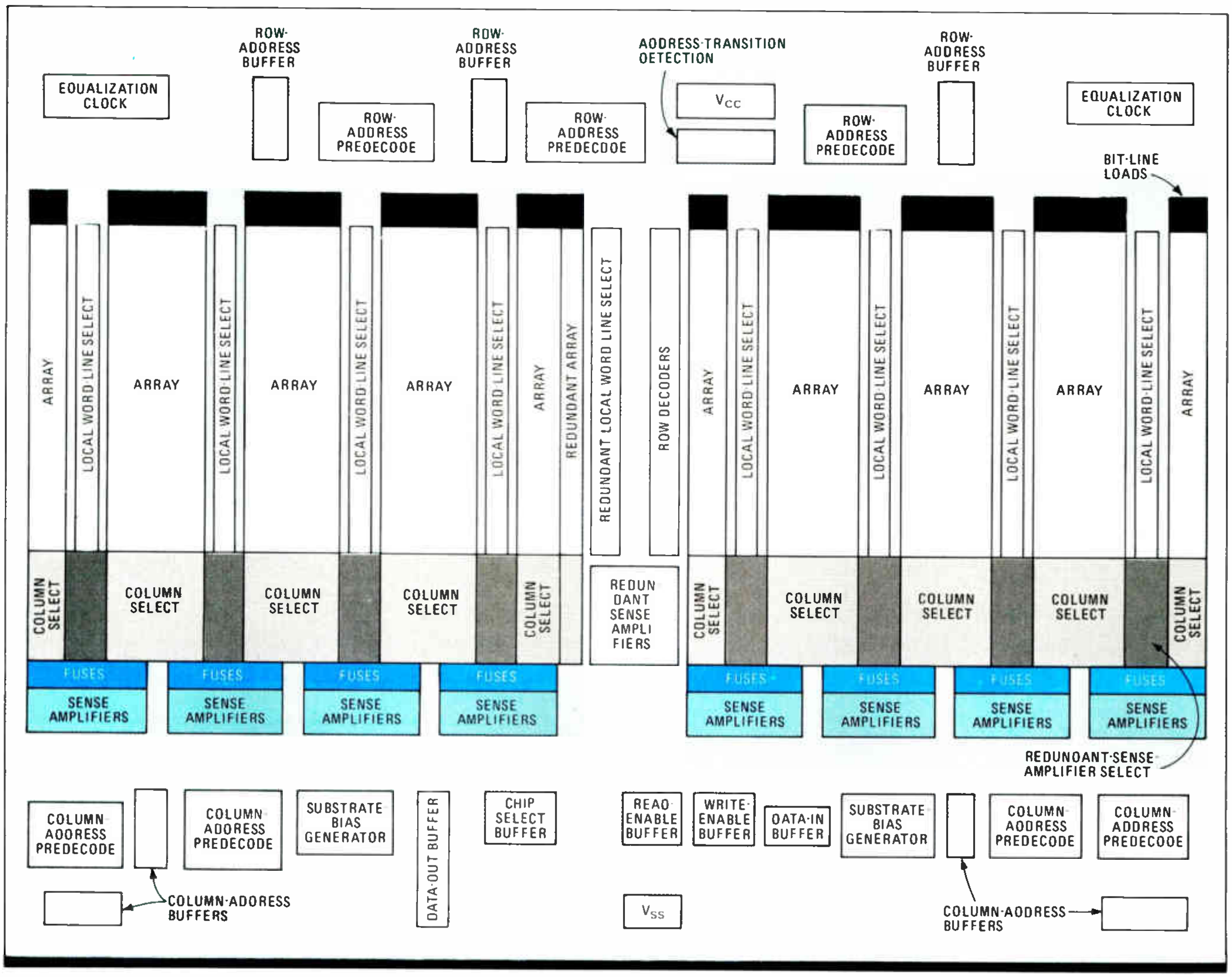
Finally, the 256-K SRAM uses a modified version of a distributed chip-enable scheme employed on the firm's 64-K SRAMs. In this earlier generation, one chip-enable signal goes to address buffers and equalization circuitry at the top of the array, and another to the bottom of the array, where the data output buffers and sense amplifiers are situated. For even greater flexibility in setting independent timing parameters referenced from the chip enable, the distributed scheme in the 256-K device uses four signals applied independently to the column decoders, the sense amplifers, the output buffers and the equalization and address-buffer circuitry.

One of the innovations Lattice uses to get a 35-ns access time in its 256-K SRAM is a distributed chip-enable scheme for flexible setting of independent timing parameters

On the process side, the contribution to speed improvement includes the use of depletion transistors to fabricate high-gain n-MOS sense amplifiers in the periphery. These sense amps are also efficient in both layout area and power.

Unlike the twin-well CMOS process used by AMD, Lattice's n-well n-MOS/CMOS does not have the same degree of latchup immunity, however. So Lattice uses a substrate biasing scheme in which the substrate is pumped to about a −2-V level. This scheme prevents biasing of the parasitic bipolar transistor structures that would impede current flow. A side benefit is reduced parasitic junction capacitances, which also increase speed.

As in the AMD SRAM, the Lattice 256-K SRAM uses lightly doped drains to mitigate the hot-electron injection and other second-order effects. To further enhance reliability and yield, the Lattice SRAM also uses a laser redundancy scheme in which any failed column detected during testing at the factory is replaced by one of four extra columns. □



2. EIGHT BLOCKS. The n-MOS array of Lattice's 256-K SRAM is organized into eight blocks to improve speed and reduce power levels.

PROBING THE NEWS

WHERE THE ACTION IS IN SOUTHERN CALIFORNIA

FIVE HOT SPOTS KEEP THE INDUSTRY BOILING IN THE L.A. METRO AREA

by Larry Waller

LOS ANGELES

Like comedian Rodney Dangerfield, Southern California's sprawling electronics industry often gets no respect. If they aren't the butt of unending wisecracks over their laid-back qualities or conducting business around the pool, local companies usually are ignored in favor of Northern California's more glamorous Silicon Valley. But the situation may be changing.

What's happening in Lotusland is rare in these slump-ridden days. With almost no fanfare, electronics-industry growth in the seven-county crescent from Santa Barbara south to the Mexican border is continuing slowly and steadily. In fact, company startups have broken out in five hot spots throughout the region.

The number of Southern California electronics companies has soared in the past half-dozen years. On the eve of the opening of the 1986 edition of Wescon, which will be held in Anaheim (see "Wescon is still the place to check out California Business," p. 90), the number of electronics companies based in Southern California has zoomed to more than 4,000, double the 2,000 that were doing business in 1980, according to the Southern California Technology Executives Network, which calls itself So/Cal/Ten.

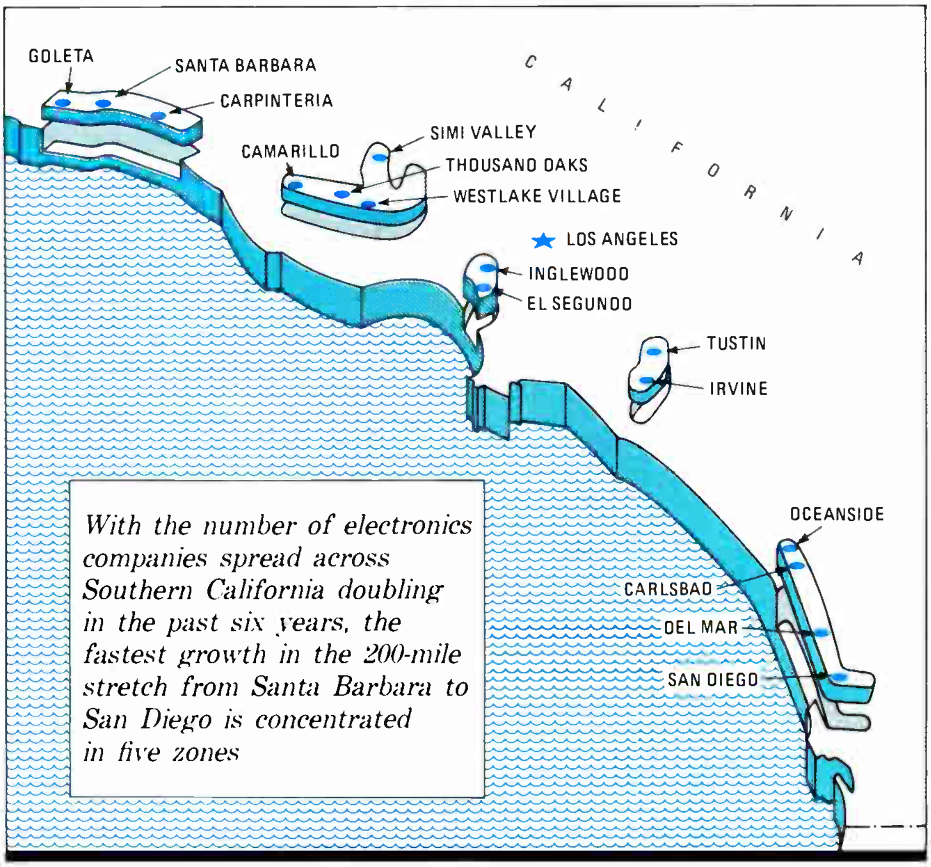
The number of companies will continue to show a strong and steady upward trend, with the possible exception of those manufacturing personal computers and peripherals, according to observers of the local business scene. Several factors are propelling this growth, from the attractions of the Southern California lifestyle to a highly regarded university system. But most important is the concentration of the defense industry in the region.

Whatever the reasons, the overall growth is impressive. The American Electronics Association reports that its membership has soared throughout the Los Angeles metro area. The total reached 2,792 companies this year, with 1,389 in Los Angeles County and 839 in Orange County. In 1982, when the AEA began keeping its data base, there was a total of 1,815. San Diego County also grew, from 299 companies to 422, in the same period. Northern California currently has 2,379 AEA members, with about 1,800 actually based in the Silicon Valley.

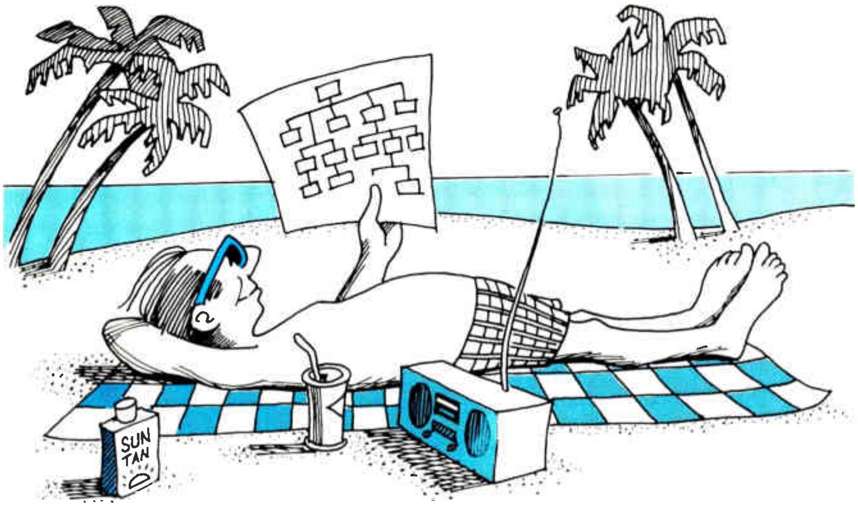
Southern California employment also has skyrocketed during the 1980s. There were some 212,000 electronics-industry workers, both commercial and military, in the Los Angeles region in 1980. Now there are more than that in the commercial sector in Los Angeles and Orange counties alone, estimates California's Employment Development Department. Military electronics jobs and other Southern California counties are included, the total could well approach the 500,000 mark. By comparison, Santa Clara County, which encompasses Silicon Valley but is a far smaller area than the southern crescent, had about 200,000 workers engaged in commercial manufacturing in June 1986.

Though industry growth is widespread throughout Southern California, five hot spots have emerged:

- In the northwest sector, along Highway 101 running west from Los Angeles, growth that started in the late 1970s continues unabated in Calabasas, Agoura, Westlake Village, Thousand Oaks, Newbury Park, and Camarillo.
- Recently, a wave of startups and expansions have reached Oxnard and Ventura on the coast, along with a cluster



With the number of electronics companies spread across Southern California doubling in the past six years, the fastest growth in the 200-mile stretch from Santa Barbara to San Diego is concentrated in five zones



in Santa Barbara.

■ The International Airport section of Los Angeles has kept its core of defense electronics firms relatively intact, while dozens of startups and expanded operations of major companies have moved in. The attractions are proximity to the airport, reasonable rents, and a central location. Also, growth begets growth: Jack E. Shemer, chairman of computer maker Teradata Corp., says he located there in 1981 because of "the broadest pool of technical talent anywhere within a one-hour radius."

■ The heart of Orange County, from Irvine east into the Tustin-Santa Ana area, has come back strongly after troubles in the microcomputer business in the early 1980s caused a brief downturn. There are miles of new industrial parks inviting more expansion.

■ San Diego is reaping the fruits of an aggressive program to attract technology firms. The northern coast of the county from Oceanside-Carlsbad down to the Kearney Mesa region of San Diego city have the bulk of activity.

The growth has been overlooked, says E. E. Ferrey, who retired last year as president of the American Electronics Association, because "it's been overshadowed by Silicon Valley. The Valley enjoyed spectacular growth and is the high-technology capital of the U. S." Ferrey, who is now a consultant, has been involved with the California electronics scene for 34 years, capping his career with the presidency of the AEA. He sees a northern-hare, southern-tortoise relationship between the two areas. "It didn't happen overnight. Southern California's industry always was larger, with more dollar volume, so it had a bigger and broader base to grow from. 'Steady growth' describes it better than anything. With things slowing [in northern California], the growth [in the south] only makes it look like a resurgence."

"Steady growth" also decribes the arrival of U. S. branches of Japanese companies. That influx promises to become even more important as manufacturing expands. In San Diego, for example, Sony Corp. arrived in the 1970s to build television sets and soon was joined by Kyocera International Inc., the world leader in ceramic packages for integrated circuits. Toshiba Corp. has its chip, printer, and computer operations in Tustin, and Epson Corp.'s printer and computer divisions are part of an expansion by Japanese companies into the Torrance area south of the Los Angeles airport. It is estimated that eight of every 10 new Japanese operations in the state now locate in the south.

Overall, different reasons for the crescent's growth are advanced by those who have contributed to it. But one is mentioned by virtually everyone: the lifestyle of Southern California still attracts those who seek a mild climate and a less pressured pace. Engineers are plentiful; many continue to move in, while those already there do not leave. Also, top engineering schools—for example, California Institute of Technology in Pasadena—turn out graduates who also tend to stay around.

Military and aerospace business continues to be the driving force

The biggest source of engineering talent is the state-supported university and college system. The region has five of the eight campuses of the top-rated University of California, anchored by UCLA, along with the same number of state colleges.

However, probably the biggest single force driving expansion has been the presence of a strong defense and aerospace business since the days of World War II. Expansion of those companies alone would cause the region to grow. Take, for example, GM/Hughes Aircraft Co. The region's leading employer, it saw its work force grow from 56,000 employees in 1980 to 82,000 this year. Other aerospace firms have grown apace.

Equally important is the way employees of those giant companies start their own businesses. "Most people underestimate the value of the infrastructure of military electronics and aerospace," notes Robert P. Kelley Jr., president of So/Cal/Ten. That group, founded in 1983 and based in Irvine, is a case in point. Its members are 150 area firms whose top officials meet regularly to exchange information and counsel on common issues and problems. Kelley observes that a majority of these executives have worked at some point at the big military electronics houses, an experience that is also common for engineers and scientists throughout the region.

TWO EDGES. But the miltary electronics business has been a double-edged sword—when it went sour, so did Southern California. The last time there were such problems was in the mid-1970s. Defense spending cuts after the end of the Vietnam War hit hard. A lot of engineers were out of work, and a bitter joke circulated widely: the best background for a real-estate license was a BSEE.

However, significant cuts in military spending in the near future are considered unlikely. And even if the Pentagon's budget does get cut, the industrial base of Southern California has broadened so much since the last military bust that any shock could be absorbed much more easily. Unlike regions that are closely tied to one segment of the business, as with Silicon Valley's heavy semiconductor orientation, the area does not depend on any single commercial product. "We don't get devastated if any one of them gets in trouble," says Steven M. Panzer, cofounder of So/Cal/Ten.

The diversity of the Southern California technology thrust provides another advantage. The broad spectrum of companies serves to attract other companies. The mix of those involved in semiconductors, computers, computer peripherals, software, and instruments, added to the massive military electronics base, means that subcontractors and ancillary services are usually just a freeway ride away.

Panzer has sought to strengthen the links by founding Rimtech (The Research Institute for the Management of Technology) in Los Angeles in 1985. Rimtech's charter is to "develop entrepreneurial ventures to support American technology companies in a highly competitive international marketplace." The first effort, launched earlier this year, provides the framework to transfer technology generated at Pasadena's Jet Propulsion Laboratory to area firms that want to use that technology commercially [*Electronics*, July 10, 1986, p. 28].

The healthy growth being experienced in Southern California, during a period when Silicon Valley is mired in its deepest slump ever, highlights another basic difference between the two regions. "We're a different mentality down here," says Carmelo J. Santoro, chief executive officer of Silicon Systems Inc., a Tustin producer of custom and standard integrated circuits. Santoro, who has spent years in both places, says there is a components orientation in the north in contrast to a system-level outlook in the south. That holds true even for Southern California companies that are in the chip business, adds Santoro. He also sees that systems-oriented position as an advantage in times like these, when overcapacity plagues components companies around the world, and believes that companies offering system solutions are poised for further gains.

But thoughtful officials still look at the Silicon Valley experience and find at least one of the north's advantages missing in the south. That is the opportunity to get together and "network." There is no central gathering spot where executives meet informally to exchange ideas, gossip, and philosophies—and, almost as often, jobs. "The main reason is geography," observes Ferrey. "Southern California is so diffuse, while Silicon Valley is a compact, focused place." Santoro adds, "We don't have anything like Rickey's Hyatt House or Dinah's down here."

IDEA SESSIONS. So a number of programs to fill that need have sprung up. So/Cal/Ten itself came into being for this purpose; in fact, the hunger of entrepreneurs for a place to try out ideas on each other and seek advice is shown in how fast the roundtables provided by So/Cal/Ten have taken off. At present, Kelley says, some 140 companies are participating in 12 such events per month, not to mention three major conferences and additional workshops. Topics covered deal with such problems as computer security and finding financing. "Where else can a CEO find experts on many topics without hiring very expensive consultants?" Panzer asks.

In addition, 27 Orange County companies participate in a CEO Roundtable with the University of California at Irvine. They frankly admit that they envision a role for the university like the one played decades ago by Stanford University in the development of Silicon Valley. Santoro thinks that building a better social atmosphere and strong ties to a university will help "correct our negatives."

Prospects look even rosier for the years ahead, as trade with Pacific Rim nations continues to build from its center in the Los Angeles metropolitan area. "We now have a critical mass of technology and entrepreneurship in Southern California," Rimtech's Panzer predicts confidently. Walter J. Zable, chief executive at Cubic Corp., which was established in San Diego in 1951 and is the industry pioneer in that city, agrees. "The high-tech engineering business in Southern California is just beginning to really show its stuff," he says. And there is nothing laid-back about that. □

WESCON IS STILL THE PLACE TO CHECK OUT CALIFORNIA ELECTRONICS

Wescon has been many things down through the years, but the big show has always been an accurate reflection of the electronics industry's fortunes in California. This year, Wescon will be held in Anaheim—it alternates between there and San Francisco—and it has two striking aspects. One is the strength of the military electronics presence, and the other is the remarkable diversity of Southern California's electronics community.

The military content of Wescon is continuing the growth trend of the last few shows—in both exhibits and technical sessions. And the many companies showing a wide range of products are indicative of the balance that is preventing the slump in semiconductors and computers from seriously damaging the area's economy as well as Wescon's attendance and number of exhibitors.

Show officials expect about 60,000 persons to pass through the doors of the Anaheim Convention Center from Nov. 18 to 20, less than the record 75,404 in 1984 because of a drop in attendance from outside the region. The total number of booths, more than 1,800, and companies, about 900, are nearly the same as in the past several years.

Dating in its current form from 1952, Wescon is the largest and the oldest continuous electronics trade show. It has continued to thrive mainly by managing to change along with the changing needs of its supporters, says Bruce S. Angwin. As president and general manager of Electronic Conventions Management, he directs the nonprofit organization that runs Wescon, Electro, and a host of regional shows. Angwin has deep roots in Wescon, working in the first show and being involved with it continually in some capacity.

"It's always been an innovative show, and we are never afraid to make changes," says Angwin. Innovations credited to Wescon include a comprehensive statistical breakdown of who attends, advance tutorial sessions to help exhibitors get the best results, and organization of its professional sessions around invited experts in particular technology fields, rather than around the conventional call for papers. These innovations have been widely copied, but Wescon implemented them first. The show also mobilizes a larger volunteer staff from industry than other shows.

In a new wrinkle this year, Wescon will use an advanced bar-coding system for registering and tracking attendees. This system will allow management to find out immediately the exact number of people attending the different parts of the show.

The 34-year-old show continues to thrive

The technical sessions have a decided military-aerospace orientation, with Donald R. Beall, president of Rockwell International Corp., giving the keynote speech. And one of the featured panels, which the organizers expect will draw a capacity audience, will offer an update on the Strategic Defense Initiative and include a question-and-answer period.

Historically, the presentation of military-related technical sessions and products has been a hallmark since 1944, when Los Angeles area manufacturers organized Wescon's predecessor to help sell products after World War II. They displayed their wares on card tables at the Los Angeles Elks Club. They must have had the right idea, because the defense business has flourished. But Angwin recalls it also triggered the "biggest trouble Wescon ever had," beginning in 1971.

A Department of Defense edict that year removed financial support from promotional activities of its contractors by requiring strict separation of military and commercial work. This caused exhibitors already signed up for the San Francisco show "to back out en masse overnight," recalls Angwin, and booth totals dropped from 1,200 to 569. The order changed Wescon into a showcase for commercial products, and it took nearly a decade to get back to the pre-1971 numbers. Only in recent years has Wescon "been relatively successful in re-establishing the defense side," says Angwin. *–Larry Waller*

NEW PRODUCTS

NAND GATES BOOST FLEXIBILITY IN FIELD-PROGRAMMABLE LOGIC

NEW DEVICE'S INTERCONNECT STRUCTURE CAN LINK ANY TWO NODES

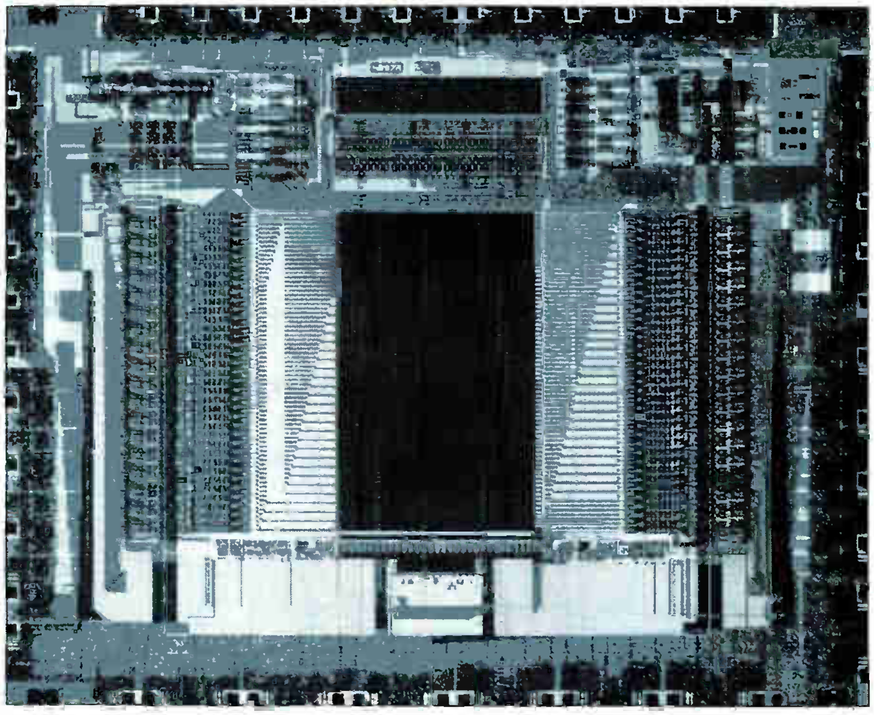
A new generation of field-programmable logic devices based on NAND gates is coming from Signetics Corp., which claims that the products are more flexible than traditional programmable-logic structures.

Scheduled for formal unveiling at Wescon '86 next week in Anaheim, Calif., the first member of Signetics' programmable macro logic (PML) family is the PLHS501, a 52-pin device incorporating 72 NAND terms, 24 dedicated inputs, eight bidirectional input/output lines, eight exclusive-OR (XOR) outputs, and eight dedicated outputs.

Unlike traditional programmable-array-logic and programmable-logic-array structures, PML devices rely on a single NAND array to implement the standard sum-of-products logic. The central programmable interconnection structure supports a periphery of logic macros. Moreover, the interconnection matrix is virtually unrestricted, allowing any node in the device to be connected to any other logic node. As a result, says the company, the NAND-based PML structure is more forgiving than the fixed-OR, programmable-AND structure of PALs, as well as being more flexible than the programmable AND/OR structure of PLAs.

MACROS. PML-based devices can support any number of multilevel logic functions, which are constructed by looping back through the central NAND array matrix. The on-chip macros that surround the core can be connected into the feedback path, thus eliminating the need to exit and re-enter the device via the I/O buffers. Besides leaving I/O pins free for external communications paths, this technique allows internal logic functions to be performed without incorporating I/O-buffer delays.

Primarily a combinatorial device incorporating only primitive macros, the PLHS501 is a gate-bucket-type device that can implement virtually all logic functions now provided by all existing PLA and PAL devices. It is also the first to incorporate true XOR output functions and output-polarity inversion, as well as multigate constructs and cross-coupled latches on-chip without involving output pins.



VANGUARD. The PLHS501, incorporating 72 NAND terms, leads off Signetics' PML family.

Built with Signetics' proprietary ZA Oxide isolated bipolar process and its vertical-avalanche-migration fuse technology, the device incorporates a NAND matrix about the size of a 16-K PROM. With a typical common-collector current of 250 mA, it features a maximum input-to-output delay of 18 ns for a single-level, single-pass implementation and 26 ns for a two-level device. Unlike AND/OR-based FPLDs, each additional level in this NAND-based device incurs only one NAND feedback delay—8 ns maximum—per level.

In addition to its flexibility, the PML approach allows the fabrication of field-programmable logic devices of much higher density than equivalently sized AND/OR-based bipolar or CMOS electrically programmable logic devices. The bipolar PLHS501, for example, even assuming a relatively conservative interconnect factor of only 20%, has a density roughly equivalent to 3,000 two-input NAND gates, some 30% to 50% higher than the density of the CMOS EPROM-based PLDs now available.

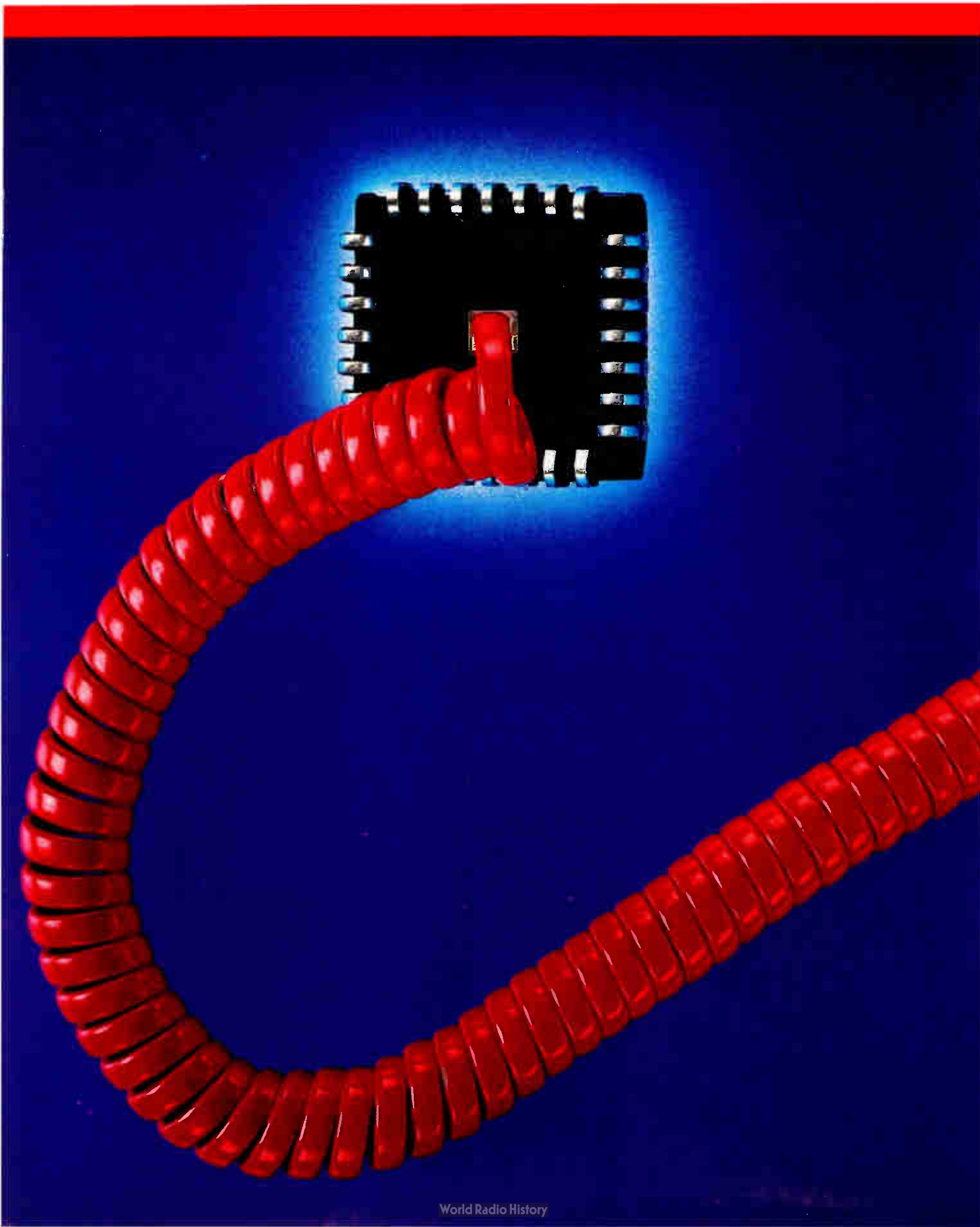
The PLHS501 costs $36.99 each in 100-lot quantities and is available now in sample quantities in a 52-pin square plastic leaded-chip-carrier package.

Scheduled for introduction sometime

Wescon/86

Few electronics trade shows can boast the diversity of products traditionally shown at Wescon, and the 1986 edition is no exception. Included on this and following pages, for example, are a new generation of programmable logic, power transistors, software, and push buttons. All will be introduced from Nov. 18 to Nov. 20 in a show expected to attract 60,000 people and 900 exhibitors.

Communications condensed:



the single-chip CMOS modem.

Introducing the K212, a complete Bell 212A compatible, full duplex modem on a single chip. It provides all the functions on one chip that used to require up to five separate chips.

Developed by Silicon Systems Inc., this 1200/300 bps modem is alternate sourced by RCA.

Peripheral-on-a-chip.

To the system designer, the K212 looks like a peripheral. It includes full Bell 103 and 212A operating modes, a call progress monitor and a DTMF dialer.

Interface with popular micros.

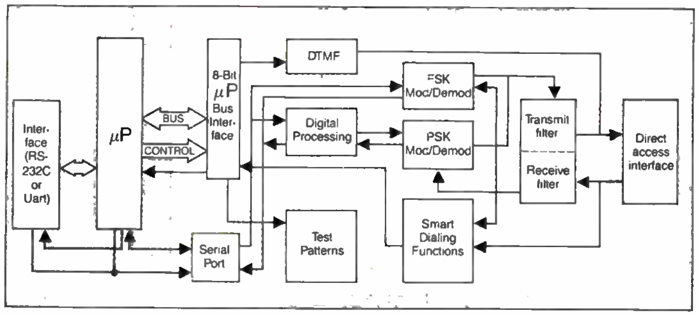
The K212 interfaces directly with the 8048/8051 family of low-cost micros. Modem operation is controlled through the on-chip, 8-bit multiplexed address and data bus, or through an optional serial-command bus. The address-latch-enable control line simplifies address demultiplexing. Data communications go only through a separate serial port.

The on-chip DTMF enables the K212 to dial its own calls. And a call-progress detection feature allows it to change calling action in response to dial tones, busy signals or ring back. The dial-up phone line is connected through an external direct access arrangement interface (FCC approved).

And because it's CMOS, the K212 consumes very little power (less than 10mW in the idle mode and only 120mW in operation).

It makes talk even cheaper.

Now a complete modem requires only the K212, a phone line interface, an RS-232-C level converter and a control microprocessor. Perfect for personal computer modems,



voice/data terminals, portables or battery operated systems. Ideal for free-standing products or systems; synchronous or asynchronous communications.

By eliminating multi-chip sets, you save board space, testing and time in bringing your product to market.

Futurespeak: the V.22 modem.

The K221 modem is coming soon, to support CCITT V.22 and V.21 communications protocol standards for Europe.

Availability: lines are open now.

You can get the K212 in 22-pin and 28-pin DIPs, or in quad packages. Samples are available for evaluation right now.

To order samples, write: RCA Solid State, Box 2900, Somerville, NJ 08876, or Silicon Systems, 14351 Myford Road, Tustin, CA 92680.

*8048 and 8051 are trademarks of Intel Corporation.

silicon systems™

RCA

Circle 95 on reader service card

next year is another bipolar device in the series, the PLHS502, which incorporates all functions of the first product but includes higher-level macros. It will be roughly twice the density of the PLHS501.

Future devices in the family will include CMOS EPLD versions with densities in the 5,000-gate range, incorporating even higher-level macros, such as buffers, counters, multiplexers, decoders, arithmetic logic units, and memory.

According to the company, the PML product line will be supported by a Signetics design software package, available in versions for IBM Personal Computer and Digital Equipment Corp. VAX 11/780 users. The package will encompass all aspects of design, partitioning, simulation, device programming, and documentation. A macro library of functions, ranging from a simple string of gates to complex ALUs, will be included.

–Bernard Conrad Cole

Signetics Corp., 811 East Argues Ave., P.O. Box 3409, Sunnyvale, Calif. 94088. Phone (408) 991-2000 [Circle 510]

DATA-FLOW IC SAMPLES AT 320-MILLION/S RATE

A new data-flow architecture by Inmos Ltd. applies the power of 32 separate 16-by-16 multipliers and 32-bit accumulators to signal-processing applications inside a cascadable, programmable, digital-transversal filter to achieve sampling speeds as high as 320 million operations/s.

Each node in the IMS A100 signal processor's data-flow architecture consists of a multiplier-accumulator and local storage. The device achieves its speed by processing input signals in parallel to its 32 on-chip multipliers. Delay and accumulation are performed in a distributed manner.

The 1.5-μm CMOS integrated circuit [*Electronics*, Oct. 30, 1986, p. 25] can be programmed to handle coefficient words of 4, 8, 12, or 16 bits. Data words are 16 bits. The 84-pin A100 achieves processing rates up to 10 MHz, or 320 million operations/s, when operating with 4-bit coefficients and 16-bit data words. The A100 runs at 2.5 MHz, or 80 million operations/s, when using 16-bit data and 16-bit coefficients.

Inmos designed the A100 as a highly flexible building block for a wide range of signal-processing applications, such as high-speed communications, radar, sonar, and speech and image processing, company representatives say.

The precision of the chip's chain of multiply-accumulator blocks is maintained by means of a 36-bit result inside the IC. A programmable barrel shifter, on the output of the multiply-add chain, lets users select one of four 24-bit fields from the 36-bit result. The 24-bit word is rounded by the circuit.

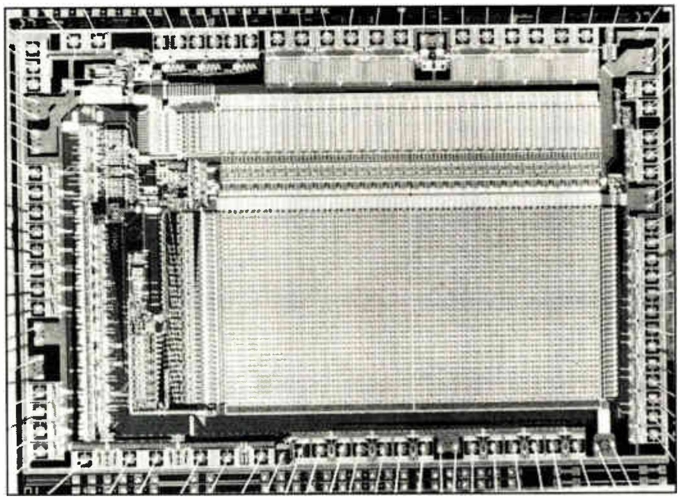
I/O ACCESS. Inmos' A100 contains a non-multiplexed memory interface that can be used to link the chip to microprocessors or standard memory buses. Coefficients and status registers can be accessed through this interface. Data input and output to the multiply-accumulator array can also be accessed through the interface, but in most high-performance applications the A100's dedicated I/O ports will be used to handle 16-bit data.

The A100 operates from a 5-V power supply, ±10%. Maximum power dissipation of the fully static CMOS circuit is 2 W. The processor, which has an operating temperature range of -40°C to +85°C, is housed in a ceramic 84-pin-grid array.

Inmos will demonstrate the A100 at Wescon '86, five months after initially announcing development of the chip during last summer's National Computer Conference. The company says the signal processor is now available at a price of $406 each in 100-piece quantities.

–J. Robert Lineback

Inmos Corp., P.O. Box 16000, Colorado Springs, Colo. 80935. Phone (303) 630-4000. Inmos Ltd., Whitefriars, Bristol BSI-2NP, England. Phone 44 272 290 861 [Circle 502]



FLEXIBLE BUILDING BLOCK. The 84-pin AL100 signal processor from Inmos can handle words of 4, 8, 12, or 16 bits.

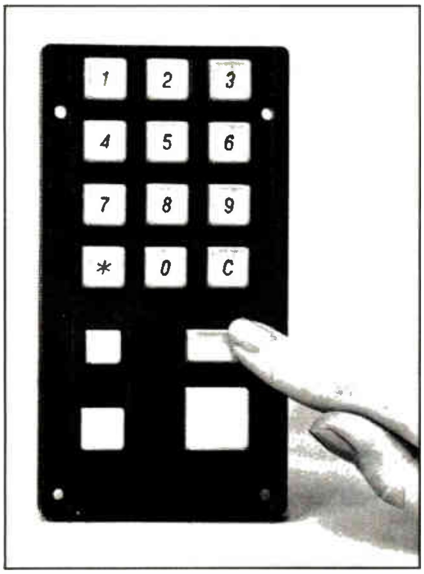
LOW-COST PUSH BUTTONS 'FEEL' RIGHT

The SLP series of push-button switches from Honeywell Inc.'s Micro Switch Division provides original-equipment manufacturers with a selection of low-cost, yet reliable switches that offer the tactile "feel" many end users want.

The SLP—second-level push button—is offered in two versions. One employs an assembly that includes a basic membrane touch panel, but adds a conventional push button and actuator mounted on top. The other uses push buttons assembled atop a conductive elastomer boot that contacts a printed-circuit-board trace to make a connection.

In the membrane-based SLP version, key travel is 0.02 in., and 14 oz of pressure is required for actuation. This provides a tactile feedback not present on standard membrane touch panels. And since the key allows for precise control of the manner and amount of pressure applied in actuating the membrane switch, the SLP promises five times the operating life of a finger-actuated touch panel. Compared with a typical life of 2 million operations for a touch panel, the membrane-based SLP will be specified at 10 million operations, says product manager Gary L. Turner. Useful life is extended because feedback provided by the top-mounted push button moderates deformation caused by operators who apply more pressure than necessary to be sure a membrane switch is activated.

The conductive elastomer-based SLP is designed to last even longer. Micro Switch has not completed testing, but expects to specify lifetime at 30 million operations, Turner says. The SLP built with conductive elastomer will offer a longer key travel, at 0.05 in., with 7 oz of pressure required for actuation. Also, the elastomer-based button will be available in a version that lights when actuated, a feature that will be attractive to engineers configuring systems where specific keys are important enough to



SMART PUSH. Micro Switch push-button module can come with a microprocessor.

be highlighted. Push buttons in any part of an array can be lit by red, yellow, or green light-emitting diodes. Unlike products that rely of a light-piping scheme and light only elements on the periphery of the array, internal keys on an SLP module can be illuminated.

Micro Switch will sell the SLP buttons assembled into strips or arrays, with or without built-in electronics and other features. In general, says Turner, the SLP is priced about 30% to 40% lower than conventional discrete buttons that rely on electronic control or mechanical contact.

Prices will range from about 50¢ per push button for a strip or array with no options when purchased in quantities of 5,000 to about $6.50 per button for 2,500 units when they are assembled in an array housed in an enclosure and equipped with a microprocessor, associated electronics, and communications circuitry for control by an outside host.

SLP push buttons are suitable for use in equipment such as office copiers, cellular telephones, and medical equipment. When equipped with a special sealed enclosure offered by Micro Switch, the SLP can be applied to industrial equipment or to outdoor operations such as automated teller machines. Both versions conform to shock, vibration, temperature, and humidity criteria specified by MIL STD 202, Turner says.

The membrane-based SLP is currently available; the version based on conductive elastomer will be available in prototype form in December, with full production scheduled for March 1987.

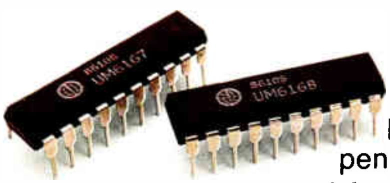
–Wesley R. Iversen

Micro Switch, 11 West Spring St., Freeport, Ill. 61032.
Phone (815) 235-5731 [Circle 550]

Circle 124 on reader service card

Score A Winning Touchdown with UMC

With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.



UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

If you want to be on a winning team, go with a proven winner......UMC.

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U.S.A. HEADQUARTERS: NMC CORPORATION 3054 SCOTT BLVD. SANTA CLARA, CA 95054 U.S.A. TEL: 408-7279239 TLX: 172730 NMC SNTA FAX: 408-9700548

POWER TRANSISTOR DOES QUICK SWITCH

Insulated-gate bipolar power transistors from Toshiba America Inc. combine high-speed switching characteristics of MOS FETs with the high-voltage resistance and low saturation voltage of bipolar devices to operate virtually noise-free at high voltage.

Conventional power transistors generate control-system carrier noise, because the switching carrier frequency is between 1 and 2 KHz. The high switching speed of insulated-gate bipolar transistors allows carrier frequencies above the audio band (15 Hz to 15 KHz) for noise-free operation.

Toshiba's GTR Giant Transistor Modules feature switching speeds comparable to conventional MOS FETs and considerably faster than the 10 to 15 μs typical of bipolar transistors. Maximum turn-off time at 500 V is 1.5 μs; at 1,000 V it is 2 μs. Maximum turn-on time is 1 μs at 500 V. Since the slope of the falling current is smoother than that of conventional MOS FETs, surge voltage is lower. Target applications will be low-noise inverters, high-speed inverters, and uninterruptible power supplies, according to the company.

QUICK. Power transistors from Toshiba feature switching speeds of 2 μs and less.

GTR modules offer minimum gate-emitter turn-on voltages of 2 or 3 V with a collector current of 25 or 50 mA. Collector-emitter voltages are 500 to 1,000 V, and maximum collector current is 25 to 50 A.

Insulated-gate transistors differ from other bipolar devices in that their drive goes to a MOS gate, resulting in high input impedance and low drive power—3 V minimum, 6 V maximum. They have attracted much attention recently and are likely to find a niche in products with blocking voltage of 1,000 V or more.

GTR prices range from $40 to $80 in 25-piece quantities. The modules are available from stock. *–Ellie Aguilar*

Toshiba America Inc. ECBS, Semiconductor Products Division, 2692 Dow Ave., Tustin, Calif. 92680.
Phone (714) 832-6300 [Circle 505]

TELPAR PUTS COLOR IN TANDEM DISPLAY

Telpar Inc. is adding color to the normally monochrome environment of Tandem Computers Inc.'s 653X data terminals. Implemented through firmware code, eight colors are available at any character location in either foreground or background. The 14-in. cathode-ray tube offers 640-by-240-pixel resolution and sits in a tilt-and-swivel enclosure atop a base that houses a monitor controller and the power supply.

All functions of the 653X terminals are duplicated by Telpar's system. The terminal contains asynchronous communications for either RS-232-C or 20-mA loop connections to host computers. Display memory will support up to 192 lines of text in a continuous-scrolling mode, or eight pages in block mode.

COLORFUL CLONE. Telpar duplicates all functions of the Tandem 653X terminals.

To configure terminal communications and screen settings, users select from a menu on the display, eliminating the need to set switches for baud rates, bit parity, and other variables.

A display timeout feature turns off the display to protect the CRT if it is not being used after a preset interval. In quanitites of 100 units, the Telpar terminal costs $1,985. Deliveries are scheduled to begin in the first quarter of 1987. *–J. Robert Lineback*

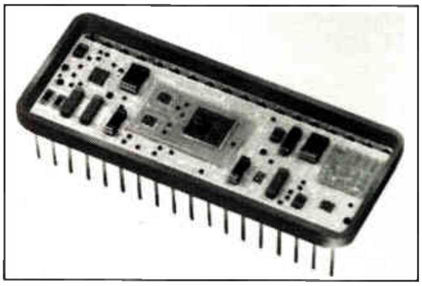
Telpar Inc., 4137 Billy Mitchell Rd., P.O. Box 796, Addison, Texas 75001.
Phone (214) 233-6631 [Circle 501]

CUSTOM IC BOOSTS TRACKING ABILITY

A new synchro-to-digital tracking converter from Natel Engineering Inc. uses a custom integrated circuit to achieve twice the accuracy of previous models and to automatically compensate for large phase-angle differences between reference and input signals.

Compatible with 8- and 16-bit microprocessors, the Model HSD/HRD1026 offers dynamic accuracy of 1.3 arc-min at a maximum tracking rate of 1,800°/s. By using a reference synthesizer to compensate for large phase differences, the company has reduced the effect of speed-induced voltages at high rotational speeds, according to Ed Berman, vice president of marketing and sales. This improves the converter's dynamic accuracy, which is maintained for signal-to-reference phase shifts up to ±45°.

The 1026 features zero velocity-lag error; a built-in test feature that signals the user when tracking error exceeds 1°; and an anti-false-lockup circuit that ensures the converter does not lock into an angle 180° from the true angle when a 180° step function is applied to it.



PRECISE POSITIONER. Natel's converter can be used in a wide range of servo systems.

Packaged in a hermetic 36-pin double DIP, the 1026 is designed for a wide range of servo-system monitors. Prices begin at $495 and depend on temperature-range selection and other options. The 1026 is available now. *–Ellie Aguilar*

Natel Engineering Co., 4550 Runway St., Simi Valley, Calif. 93063.
Phone (805) 581-3950 [Circle 500]

LINEAR INTRODUCES PRECISON OP AMPS

Linear Technology Corp. is unveiling a line of linear building-block circuits, including the LTC1057/1058 dual and quad JFET input precision operational amplifiers and the LTC1042 window comparator.

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applications such as high-speed instrumentation and logarithmic, D/A output, and photodiode amplifiers.

Available in a standard 8-pin DIP, the LTC1057 is designed to replace all popular bipolar and JFET input dual operational amplifiers. Available now, the LTC1057 costs $3.40 each in lots of 100 in plastic DIPs and $4.65 each in ceramic DIPs or metal-can packages. In similar quantities, the LTC1058 is $6.50 and $8.40 each in plastic or ceramic DIPs.

The LTC1042 is a monolithic window comparator designed for use in such applications as fault detectors, limit-cycle controllers, and as a monitor in microprocessor power-supply circuits. Its sampling and comparison cycle is 80 μs, and it consumes 1.5 μW of power when operating at one sample/s. Available now in an eight-pin mini-DIP, the LTC1042 is $1.90 each in 100-piece lots.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, Calif. 95035.
Phone (408) 942-0810 [Circle 511]

SOFTWARE TARGETS IEEE-488 DATA BUS

Lotus Development Corp. is aiming to push its Lotus 1-2-3 spreadsheet into the scientific and technical market by introducing Lotus Measure, a software package that allows direct entry of test-and-measurement data into personal computers over the IEEE-488 bus.

The software's IEEE-488 bus code was developed jointly with National Instruments Corp., which will market its GPIB-PC2 and PC2A boards as the interface hardware, besides selling the Lotus software. Lotus Measure supports simultaneous operation of up to 15 devices over the parallel bus.

The package enhances 1-2-3 operations in several ways. For example, users can configure the software to function as several particular instruments on the IEEE-488 bus. An interactive test mode can be used to give data-collection programs a dry run.

The software stores complete IEEE-488 bus configurations and individual instrument settings. Data can be read from the parallel bus in three modes. Those modes are numeric, ASCII files, or binary data.

Lotus Measure costs $495, and will be available by year's end. National Instruments' GPIB-PC2 and PC2A interface boards sell for $395 each and are available from the Austin, Texas, company now. *–J. Robert Lineback*

National Instruments Corp., 12109 Technology Blvd., Austin, Texas 78727-6204. Phone (512) 250-9119 [Circle 504]

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EL 11/13/86

AT&T FIBER-OPTIC MODEM CRACKS RS-232 STANDARD

DEVICE OPERATES AT 19.2-Kb/S, FULL DUPLEX BY MULTIPLEXING DATA AND CONTROL CHANNELS

A fiber-optic modem from AT&T Technology Systems Co. multiplexes data and control channels onto a single strand of optical fiber to attain full-duplex communication at the 19.2-Kb/s data rate of the RS-232-C standard. In addition to this fiber-optic breakthrough, the ODL RS232-2 eliminates radio-frequency noise and gives local-area-network designers the opportunity to extend LANs beyond the bounds of standard modems.

Previous attempts at implementing fiber-optic modems required two fiber lines for two-way communication, an expensive alternative to copper wire. But AT&T found that by multiplexing two data channels—plus a control line for each—onto a single fiber, the price of a fiber system could be reduced. Moreover, in applications where there is little or no need for control functions on the network, the control channels can be used as extra data channels instead.

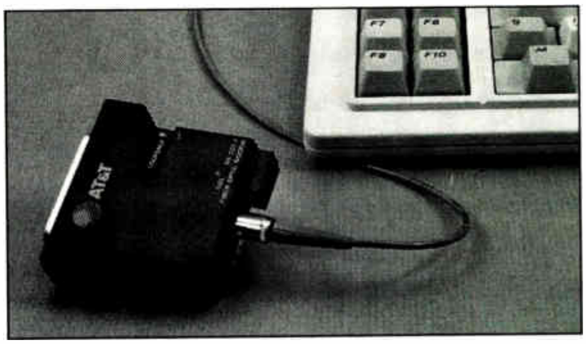
MULTIPLE CHANNELS. The high bandwidth of fiber makes it easy to squeeze multiple channels onto a single strand, says Reinhard Knerr, supervisor of the Lightwave Local Area Network Technology Group at AT&T's Bell Laboratories. "The user sees full duplex, but in reality we are doing extremely fast half-duplex," Knerr says. "We use a proprietary time-compression scheme—a ping-pong type of protocol" in which the receiver reads each channel alternately.

Since fiber transmits light rather than electricity, it is immune to electromagnetic and radio-frequency interference and therefore is ideal for networking in places where interference is a problem.

Another advantage, says product manager Mitch Bloom, is that the fiber-optic modem can be used to extend the RS-232-C network. While the standard specifies links up to 15.5 m, the fiber version works to 1 km—extra distance that can help in configuring a LAN over a factory floor or through a multiple-story building.

The modem's heart is a custom CMOS lightwave transceiver, the Model 02X, which AT&T will make available to original equipment manufacturers as a separate unit. Housed in a rugged 16-pin DIP with an integral lens-coupled optical connector, it is designed for use with 62.5-μm/125-μm optical fiber, but AT&T says it can be used with other fiber as well.

A light-emitting diode that accompanies the custom IC produces and interprets the light pulses that drive the system. AT&T believes it is the only company using an LED as both transmitter and receiver on a commercial device. Besides overcoming the distance and radio-frequency interference problems, fiber eliminates the need for a ground wire—a problem in factories or office buildings, because different locations may have different dielectric values.



PROBLEM SOLVER. High RF-noise environments and long-distance communications are easy for fiber-optic modems.

Priced at about $105 in 100-unit quantities (about $85 in 1,000-piece orders), the RS232-2 modem is not cheap. The modem is substantially more expensive than a standard RS-232-C port connector, but AT&T believes it will sell into a niche market where other solutions, such as shielded wire, are just as expensive or infeasible.

The 02X lightwave transceiver costs $57 in 100-piece quantities and about $50 each in 1,000-unit orders.

–Tobias Naegele

AT&T Technologies, Dept. 50AL203140, 555 Union Blvd., Allentown, Pa. 18103. Phone (800) 372-2447 [Circle 340]

SERVER LINKS 15 PCs TO MULTIPLE PRINTERS

One of the first PC-network shared-printer applications to emerge is an easy-to-use product for 2 to 15 PCs that is inexpensive and easy to install. EasyPrint, offered by Server Technology

Inc., consists of PC software and cables with RS-232-C modular connectors. One PC is designated the hub and can have up to four shareable printers or plotters connected to it. Printer sharing using EasyPrint is transparent to the PC users and the PC application programs—users are able to rely on standard print commands.

A starter kit consisting of two copies of the software and a 30-ft. cable is priced at $159.50. When more PCs need to be connected, a two-port or six-port serial-port expansion board is purchased for the server PC. Prepackaged kits including cables and serial-port expansion boards for three-PC and seven-PC systems are available at $349.95 and $899.95, respectively.

The serial-port expansion boards are available separately for $219.95 and $489.95 for two and six ports, respectively. EasyPrint can be ordered now, and the company will begin shipping on Nov. 25.

Server Technology Inc., 1095 East Duane Ave. #103, Sunnyvale, Calif. 94086.
Phone (800) 835-1515 [Circle 346]

HITACHI TO OFFER 600 Mb OPTICAL DRIVE

Hitachi America Ltd.'s forthcoming 5¼-in. optical disk drive will offer a capacity of 300 Mb per side in a write-once/read-many (WORM) configuration. The OD101 drive uses a single-beam laser, spins at 1,800 rpm, and features an average access time of less than 100 ms. Hitachi, which plans to introduce the drive at the Las Vegas Comdex show this week, says the OD101 will be available in the second quarter of 1987 for $4,380 in OEM quantities. Following on the heels of a 5¼-in. optical drive announced by Fujitsu America Inc., San Jose, Calif., last month, Hitachi's drive adds pressure to establish an international 5¼-in. optical disk standard. Companies already manufacturing 5¼-in. optical drives include Optotech Inc. and Information Storage Inc., both of Colorado Springs, and industry experts expect Toshiba to follow suit sometime next year.

Media to support the new drive will come from Hitachi's Maxell Corp. of America subsidiary, which has announced a new 5¼-in. optical direct-read-after-write (DRAW) disk. The new 600-megabyte double-sided disk is capable of storing 13,000 letter-size pages of information per side, and is available in both blank and pre-grooved formats. Maxell, which already manufactures a 12-in. optical disk, prices its new 5¼-in. product at about $200, with sample distribution this month.

Hitachi America Ltd., 950 Elm Ave., San Bruno, Calif. 94066.
Phone (415) 872-1902 [Circle 345]

MEETINGS

MIL-STD-1553B: Applications, Developments, and Components, ERA Technology Ltd. (Laura Christie, seminar organizer, ERA Technology Ltd., Cleeve Road, Leatherhead, Surrey KT22 7SA, UK), Regent Crest Hotel, London, Nov. 25-26.

Power Electronics and Variable-Speed Drives '86, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL, UK), National Exhibition Centre, Birmingham, England, Nov. 25-27.

Electronicom '86, IEEE (Richard Brostrom, Berger & Associates Canada Inc., 133 Richmond St. W., Suite 203, Toronto, Ontario M5H 2L5), Toronto Convention Centre, Toronto, Canada, Dec. 1-3.

GLOBECOM '86: Global Telecommunications Conference 1986, IEEE (Ross Anderson, Southwestern Bell, Room 706, 3100 Main St., Houston, Texas 77002), Westin Galleria Hotel, Houston, Texas, Dec. 1-4.

National Database and 4th Generation Language Symposium, Digital Consulting Associates Inc. (6 Windsor St., Andover, Mass. 01810), Ritz Carlton Hotel, Boston, Dec. 2-5.

2nd International Conference on Artificial Intelligence, Institut International de Robotique et d'Intelligence Artificielle de Marseille (Viviane Bernadac, IIRIAM, 2 Rue H. Barbuss, 13241 Marseille Cedex 1, France), Marseilles, France, Dec. 2-5.

Controls West '86, Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Long Beach Convention Center, Long Beach, Calif., Dec. 3-5.

IEDM '86: International Electron Devices Meeting, IEEE (Melissa Widerkehr, Courtesy Associates Inc., 655 15th St., N.W., Washington, D.C. 20005), Westin Bonaventure Hotel, Los Angeles, Calif., Dec. 7-10.

International OEM, Penton Exhibitions (Bill Little, Penton Expositions, 122 E. 42nd St., New York, N.Y. 10168), Jacob Javits Convention Center, New York, Dec. 9-11.

Microcomputer Graphics Show and Conference, Expoconsul International Inc. (3 Independence Way, Princeton, N.J. 08540), Jacob Javits Convention Center, New York, Dec. 17-19.

International Winter Consumer Electronics Show, EIA Consumer Electronics Group (2001 Eye St., N.W., Washington, D.C. 20006), Las Vegas Convention Center, Las Vegas, Nev., Jan. 8-11.

Macworld Exposition, Mitch Hall Associates (P.O. Box 155, Westwood, Mass. 02090), Moscone Center, San Francisco, Calif., Jan. 8-10.

O-E/LASE '87: Second Annual Symposium on Optoelectronics and Laser Applications, The International Society for Optical Engineering (P.O. Box 10, Bellingham, Wash. 98227), Marriot Hotel and Airport Hilton Hotel, Los Angeles, Calif., Jan. 11-16.

SMART III: Surface Mounting and Reflow Technology, EIA, *et al.* (2001 Eye St., N.W., Washington, D.C. 20006), New Orleans Hyatt Regency, New Orleans, La., Jan. 12-15.

Picosecond Electronics and Optoelectronics, Lasers and Electro-Optics Society of the IEEE, *et al.* (Optical Society of America, 1816 Jefferson Place, N.W., Washington, D.C. 20036), Hyatt Lake Tahoe Hotel, Incline Village, Nev., Jan. 14-16.

Instrument Asia '87, Instrument and Control Society (Kallman Associates, Five Maple Court, Ridgewood, N.J. 07450-4431), Singapore, Jan. 14-17.

OFC/IOOC '87: Optical Fiber Communication Conference/International Conference on Integrated Optics and Optical Fiber Communication, Lasers and Electro-Optics Society of the IEEE, *et al.* (Optical Society of America, 1816 Jefferson Place, N.W., Washington, D.C. 20036), Reno-Sparks Convention Center, Reno, Nev., Jan. 19-22.

SYSCON: OEM Computer Peripherals Subsystems Conference & Exposition, Multidynamics Inc. (17100 Norwalk Blvd., Suite 116, Cerritos, Calif. 90701), Los Angeles Airport Hilton Hotel, Los Angeles, Calif., Jan. 20-21.

Uniforum Conference and Trade Show, USR/group (4655 Old Ironsides Dr., Suite 200, Santa Clara, Calif. 95054). Washington Convention Center, Washington, D.C., Jan. 20-23.

Winter 1987 Usenix Technical Conference, Usenix Association (P.O. Box 385, Sunset Beach, Calif. 90742), Omni Shoreham, Washington, D.C., Jan. 21-23.

Southern Manufacturing Technology Show, National Machine Tool Builders Association (7901 Westpark Dr., McLean, Va. 22102), Charlotte Convention Center, Charlotte, N.C., Jan. 26-29.

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ELECTRONICS WEEK

NEC WANTS NEW TRIAL JUDGE

Final disposition of the legal battle between Intel Corp., Santa Clara, Calif., and Japan's NEC Corp. will be delayed for several weeks pending a ruling on NEC's request that the judge in the case be disqualified. U. S. District Judge William A. Ingram, who ruled in September that Intel's microprocessor microcode is covered by copyright law [*Electronics*, Oct. 2, 1986, p. 24], was at the time a member of an investment club that held 60 shares of Intel stock. Ingram, whose share was worth about $80, said he was not aware of the investment. Still to be decided is whether NEC violated the Intel copyright.

COUNTERPOINT GETS A NEW DEAL

Its deal to supply AT&T stymied for the moment, Counterpoint Computers has signed an OEM and technical exchange agreement with Multitech Industrial Corp. of Taiwan. Under a three-year, $20 million agreement, the San Jose, Calif., startup will turn its 68020-based System 19K platform into a server for Multitech's IBM Personal Computer clones. Counterpoint will also have rights to market Multitech's PCs. AT&T has reportedly delayed its plans to market a machine based on the 19K while it coordinates its computer operations more closely with Ing. C. Olivetti of Italy (see p. 40).

U. S. STARTUP GOES INTO SRAM MARKET

Just when everyone thought the U. S. had virtually abandoned the commodity memory-chip market to offshore producers, a Sunnyvale, Calif., startup comes along to buck the trend—and the odds. MOS Electronics Corp. is introducing a 64-K CMOS static random-access memory for as low as $10 in 100-unit orders. The company believes it can compete in that cutthroat market because its submicron technology results in smaller chips and lower production costs.

VLSI TECHNOLOGY TO SELL MEMORIES

VLSI Technology Inc., a market leader in application-specific integrated circuits, is using an old trick to prove out its fledgling 1.2-μm process. The San Jose, Calif., company says it will phase in its new technology by pushing 16-K static random-access memory chips beginning late in the third quarter of 1987. Within a year, however, as its 1.2-μm ASIC designs enter production, VLSI says it will already be preparing its exit from the memory market—before the SRAMs become commodity parts.

ROBOT SALES SOAR, BUT ORDERS LAG

Shipments by U. S. robot manufacturers rebounded strongly during the second quarter after a slowdown early this year, but that growth may be short-lived. The dollar value of robot shipments was up 44% from $83 million in the first quarter to $119 million, and new orders rose 74%, from $73.1 million to $127 million, during April, May, and June, according to the Robotics Industry Association, Ann Arbor, Mich. The industry's order backlog, however, is not bouncing back as strongly. By June 30, the backlog stood at about $217 million, up from $210 million in the first quarter, but nowhere near the $381 million of a year ago.

COMPAQ PLANS ASSEMBLY IN ASIA

Compaq Computer Corp. is making its first move toward overseas assembly. The Houston, Texas, company will assemble printed-circuit boards at a subsidiary in Singapore beginning in the third quarter of 1987, and will return the boards to Texas for system assembly and shipment. Compaq will maintain its board assembly line in Houston for new products, especially those that require fast turnaround to meet market demands. The company says higher costs for memory chips, in part a result of the recent U. S.-Japan semiconductor trade pact, were a factor in the decision.

TI BACK IN BLACK, BUT LOSES IN CHIPS

Sales rose 5% at Dallas-based Texas Instruments Inc. in the third quarter as the company declared a net gain of $14 million, compared with an operating loss of $44.1 million for the same period a year ago. TI says its semiconductor business is recovering from last year's slide, but the chip division still operated "slightly below break-even for the quarter."

DATA GENERAL LOSES $29 MILLION

Data General Corp. reported a $29 million net loss for its fiscal year 1986, which ended Sept. 27, on sales of $1.27 billion. Partly responsible for the red ink was a one-time payment of more than $30 million to Fairchild Semiconductor Corp., the result of a suit in which DG was charged with unfairly bundling software with hardware. The 1986 results compare with a net profit of $24.3 million on $1.24 billion in sales in 1985.

DANA PULLS IN MORE CAPITAL

Less than a year after winning $11 million in initial funding from venture capitalists, Dana Computer Inc., Sunnyvale, Calif., has secured $20 million more from Kubota Ltd., a Japanese industrial-equipment maker that was seeking a route into high technology. In exchange, Kubota gets an equity position in Dana, but not control of the company, says founder Allen H. Michels. Dana is developing a desktop supercomputer that will ship in late 1987.

EQUATORIAL MAKES MORE STAFF CUTS

Equatorial Communications Co. says it laid off 127 employees because of sluggish sales of its interactive satellite earth stations. The largest of three layoffs this year, the latest move reduced employment at the Mountain View, Calif., company to 428 from January's high of 700. Earlier this month, founder Dean T. Mack resigned as president and chief executive officer and was replaced by cofounder Edwin B. Parker.

FEW GO TO FALL COMPUTER SHOW

The Fall Joint Computer Conference had plenty of technology papers during its first run at the Informat in Dallas last week, but attendance fell far short of original estimates. Preliminary figures showed only 2,500 people attended the conference, far fewer than the expected crowd of 6,000 to 10,000. Exhibiting companies were left to wonder if the light turnout was a sign of tough times in the industry or lack of interest in the fall conference.

PHILLIPS WILL BACK THOMSON PACKAGE

Philips International NV of the Netherlands and France's Thomson Semiconducteurs are pushing to make the French company's ISO-TOP package for power semiconductors a worldwide standard. Philips will manufacture the package, which is suited for compact high-power industrial applications, under a Thomson license.

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- **K.** ☐ Educational 2 4 Year College University
- **L.** ☐ Other ______________ Please specify

Your principal job responsibility (check one)

- **A.** ☐ Corporate Operating and General Management
- **B.** ☐ Design & Development Engineering
- **C.** ☐ Engineering Services
- **D.** ☐ Basic Research
- **E.** ☐ Manufacturing & Production
- **F.** ☐ Other ______________

Estimate number of employees (at this location): **1.** ☐ under 20 **2.** ☐ 20-99 **3.** ☐ 100-999 **4.** ☐ over 1000

1 16 31 46	61 76 91 106	121 136 151 166	181 196 211 226	241 256 271 348	363 378 393 408	423 438 453 468	483 498 703 718
2 17 32 47	62 77 92 107	122 137 152 167	182 197 212 227	242 257 272 349	364 379 394 409	424 439 454 469	484 499 704 719
3 18 33 48	63 78 93 108	123 138 153 168	183 198 213 228	243 258 273 350	365 380 395 410	425 440 455 470	485 500 705 720
4 19 34 49	64 79 94 109	124 139 154 169	184 199 214 229	244 259 274 351	366 381 396 411	426 441 456 471	486 501 706 900
5 20 35 50	65 80 95 110	125 140 155 170	185 200 215 230	245 260 275 352	367 382 397 412	427 442 457 472	487 502 707 901
6 21 36 51	66 81 96 111	126 141 156 171	186 201 216 231	246 261 338 353	368 383 398 413	428 443 458 473	488 503 708 902
7 22 37 52	67 82 97 112	127 142 157 172	187 202 217 232	247 262 339 354	369 384 399 414	429 444 459 474	489 504 709 951
8 23 38 53	68 83 98 113	128 143 158 173	188 203 218 233	248 263 340 355	370 385 400 415	430 445 460 475	490 505 710 952
9 24 39 54	69 84 99 114	129 144 159 174	189 204 219 234	249 264 341 356	371 386 401 416	431 446 461 476	491 506 711 953
10 25 40 55	70 85 100 115	130 145 160 175	190 205 220 235	250 265 342 357	372 387 402 417	432 447 462 477	492 507 712 954
11 26 41 56	71 86 101 116	131 146 161 176	191 206 221 236	251 266 343 358	373 388 403 418	433 448 463 478	493 508 713 956
12 27 42 57	72 87 102 117	132 147 162 177	192 207 222 237	252 267 344 359	374 389 404 419	434 449 464 479	494 509 714 957
13 28 43 58	73 88 103 118	133 148 163 178	193 208 223 238	253 268 345 360	375 390 405 420	435 450 465 480	495 510 715 958
14 29 44 59	74 89 104 119	134 149 164 179	194 209 224 239	254 269 346 361	376 391 406 421	436 451 466 481	496 701 716 959
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- **D.** Test and measurement equipment
- **E.** Consumer products (TV, radio, hi-fi, recorders, home computers, appliances)
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- **I.** Other manufacturers using electronics equipment as part of their product (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
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- **K.** Independent research and development laboratory or consultant
- **L.** Research and development organizations which are part of an educational institution
- **M.** Independent software developers
- **N.** Operators of communications equipment (utilities, railroads, police and airlines, broadcasting, etc.)
- **O.** Educational 2-4 year college, university
- **P.** Other ______________

☐ **Indicate your principal job function, occupation and/or title (place applicable letter in box. If letters O, P, or Q are used, fill in name of college or university).**

- **A.** Corporate Management (Owners, Partners, Presidents, V.P.'s, etc.)
- **B.** Operating Management (General Managers, Group Managers, Division Heads, etc.)
- **C.** Engineering Management (Project Manager, Chief Engineer, Section Heads, V.P. Engineering, V.P. Research and Development, V.P. Quality Control, etc.)
- **D.** Software Engineering
- **E.** Systems Engineering/Integration
- **F.** Quality Control Engineering (Reliability and Standards)
- **G.** Design Engineering
- **H.** Engineering Support (Lab Assistants, etc.)
- **I.** Test Engineering (Materials, Test, Evaluation)
- **J.** Field Service Engineering
- **K.** Research and Development (Scientists, Chemists, Physicists)
- **L.** Manufacturing and Production
- **M.** Purchasing and Procurement
- **N.** Marketing and Sales
- **O.** Professor/Instructor at ______________
- **P.** Senior Student at ______________
- **Q.** Graduate Student at ______________

☐ **Indicate your principal job responsibility. (place the appropriate number in box)**
1. Management 2. Engineering Management 3. Engineering

Estimated number of employees at this location. (check one)
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Product name		Type	Shape	Dimensions L (mm)	W (mm)	T (mm)	Electrical Characteristics
Multilayer Ceramic Chip Capacitor		C1508		1.5	0.8	1.0	C: 0.5 ~ 470pF, 100 ~ 22,000pF
		C2012		2.0	1.25	0.6 / 0.85 / 1.25	C: 0.5 ~ 1,800pF; C: 470 ~ 100,000pF
		C3216		3.2	1.6	0.6 / 0.85 / 1.1	C: 0.5 ~ 270pF; C: 470 ~ 220,000pF
		C3225		3.2	2.5	<1.9	C: 750 ~ 8,200pF, 56,000 ~ 470,000pF
		C4532		4.5	3.2	<1.9	C: 2,400 ~ 18,000pF, 180,000pF ~ 1μF
		C5650		5.6	5.0	<1.9	C: 5,100 ~ 33,000pF, 270,000pF ~ 1.5μF
Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)		FC1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
		FC2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
		FR1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
		FR2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
Wound Chip Inductor		NL322522		3.2	2.5	2.2	L: 0.01 ~ 220μH
		NL453232		4.5	3.2	3.2	L: 1.0 ~ 1,000μH
		NLF453232		4.5	3.2	3.2	L: 1.0 ~ 1,000μH
Multilayer Chip Inductor		MLF321606		3.2	1.6	0.6	L:0.047 ~ 220μH
		MLF321611		3.2	1.6	1.1	
		MLF322511		3.2	2.5	1.1	
		MLF322518		3.2	2.5	1.8	
		MLF322525		3.2	2.5	2.5	
Multilayer Chip Transformer		MTT4532		4.5	3.2	2.8 max.	L: 10 ~ 200μH
Multilayer Chip IFT		MIA4532		4.5	3.2	2.8	F: 455, 459, 464kHz
		MIF4532		4.5	3.2	2.2	F: 10.7MHz
Multilayer Chip LC Trap		MXT4532		4.5	3.2	2.8 max.	F: fo ±2%
Multilayer Chip LC Filter	HPF (Tuner)	MXF4532H		4.5	3.2	2.8 max.	Electrical characteristics are representative, please specify value when ordering.
	BPF (FM radio)	MXF4532B		4.5	3.2	2.8 max.	
	BPF (VCR)	MXB5050B		5.0	5.0	2.8 max.	
	LPF (VCR)	MXB5050L		5.0	5.0	2.8 max.	
	Equalizer (VCR)	MXB5050E		5.0	5.0	2.8 max.	
	Delay Line (VCR)	MXB50500		5.0	5.0	2.8 max.	
Multilayer Chip Capacitor Network		MCN7575		7.5	7.5	0.9	C: 1 ~ 1,000pF (TC:CH) (10 capacitors); C: 10 ~ 1,000pF (TC:SL) (10 capacitors)
Ferrite Chip Beads		CB201209		2.0	1.25	0.9	Zo: 7, 10, 11Ω
		CB321611		3.2	1.6	1.1	Zo: 19, 26, 31Ω
		CB322513		3.2	2.5	1.3	Zo: 31, 52, 60Ω
		CB453215		4.5	3.2	1.5	Zo: 70, 120, 125Ω
SM Active Delay Line		FDL		12.0	9.5	5.6	Delay time: 20 ~ 250 nsec.
SM Transformer/ Inductor		EE5		7.4	5.3	4.75	Electrical characteristics are representative, please specify value when ordering.
		ER9.5		11.5	9.5	6.3	
		ER11		12.5	11.0	6.3	
		T2		7.0	5.0	2.2	
Step-up Inductor (Piezo Buzzer)		OL3.3×1.6		5.6	5.3	1.6	Inductance values are representative, please specify value when ordering.
		OL3.3×2.1		5.6	3.3	2.1	

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TLC-363

TLC-402

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W×H×D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	VDD	7 V	7 V
	VDD – VEE	20 V	20 V
Input Voltage		0≤VIN≤VDD	VSS≤VIN≤VDD
Recommended Operating Conditions			
Supply Voltage	VDD	5±0.25V	5±0.25V
	VEE	−11±3V Var	−11±3V Var.
Input Voltage	High	VDD – 0.5V min.	VDD – 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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