THIS MINISUPER IS AIMED AT PARALLEL PROCESSING/56

HOW AI WILL ADD BRAINS TO OFFICE AUTOMATION/63

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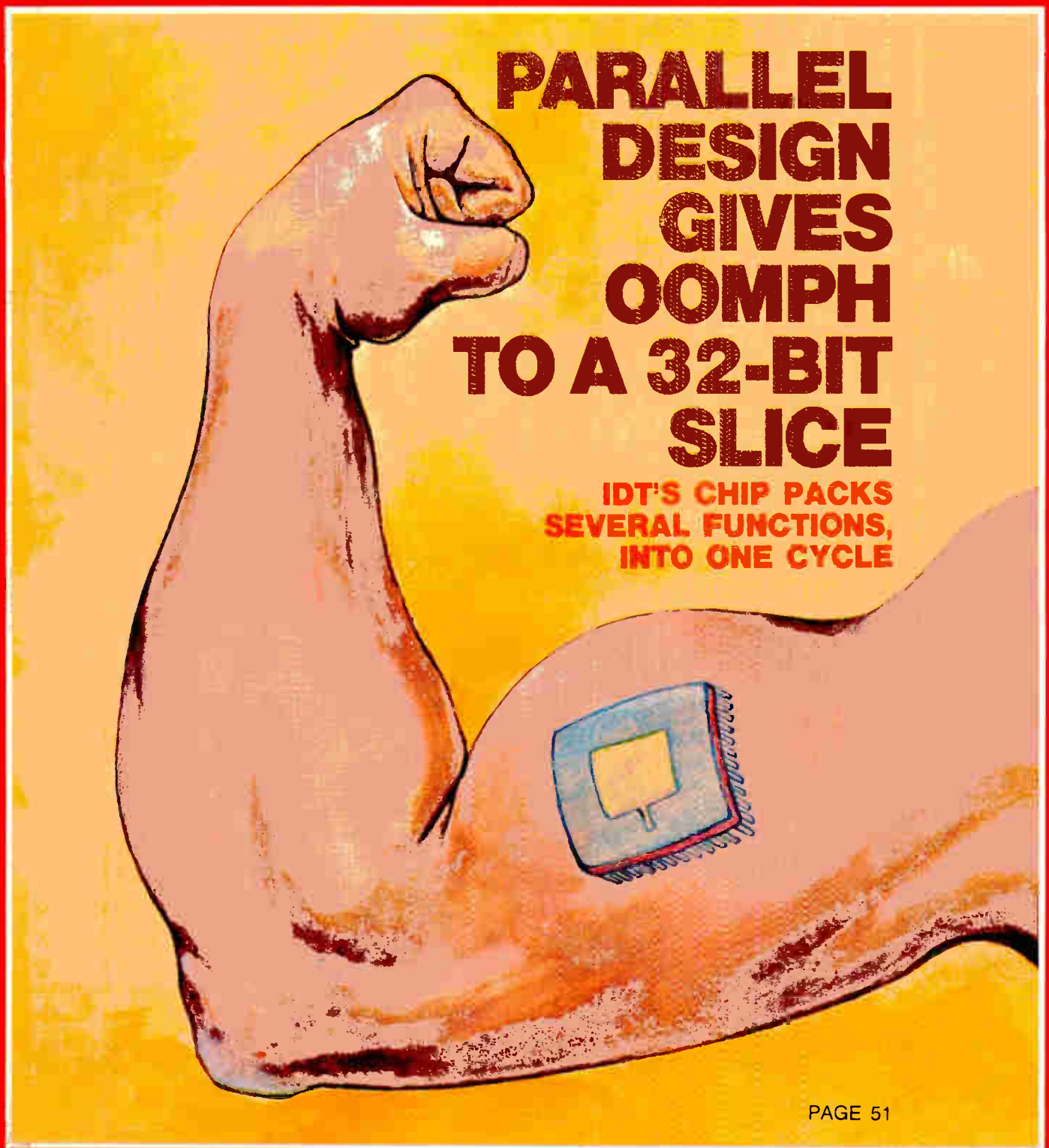
Electronics



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PAGE 51

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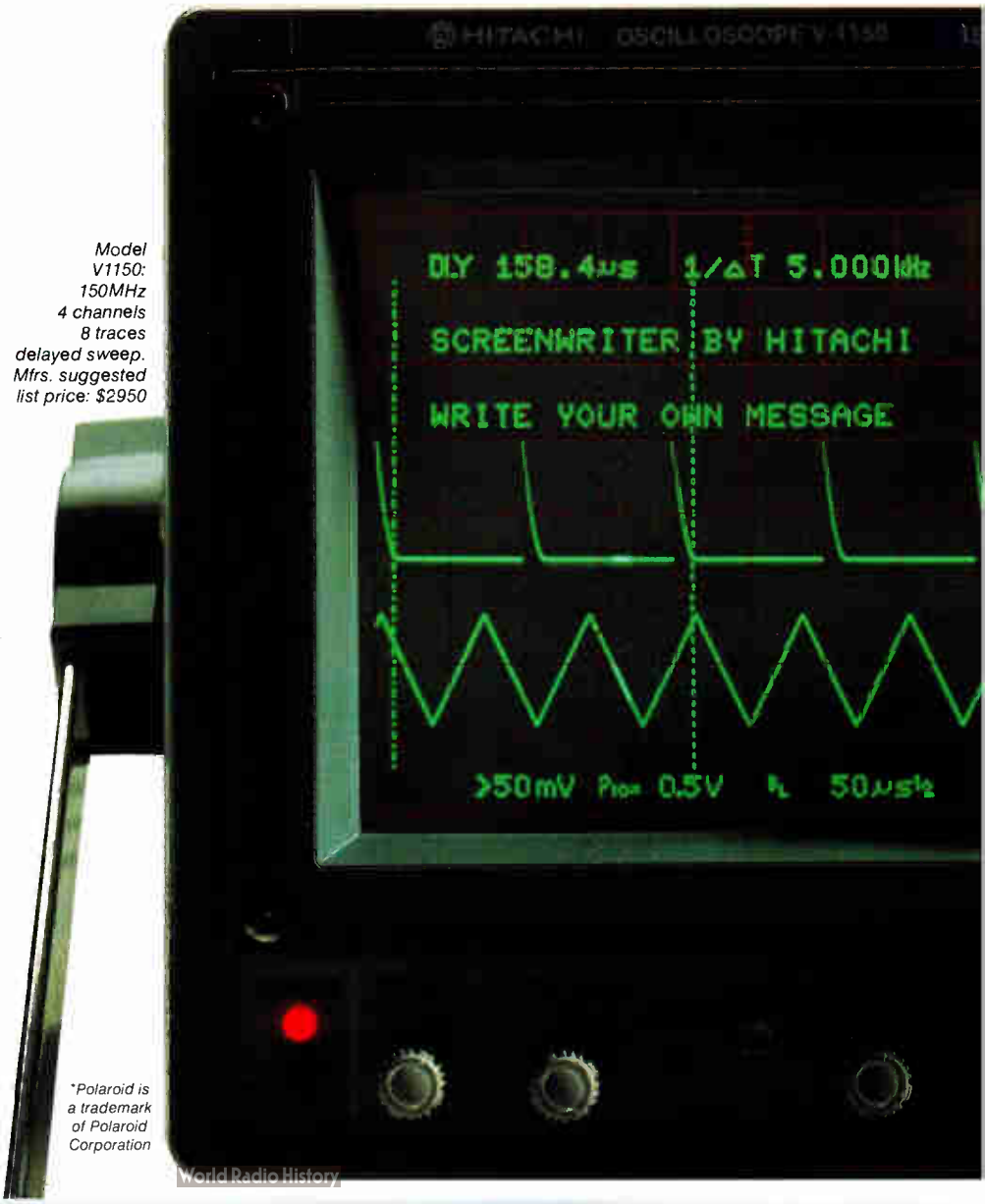

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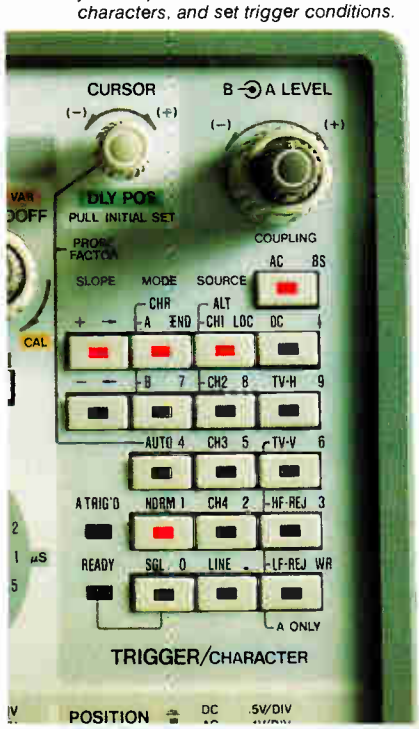

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Circle 2 on reader service card

There have been 11 Electronica shows, and John Gosch, our man in West Germany, has covered all but the first one, in 1964. So when he writes about the 12th edition of the big international components exposition in Munich, as he does in this issue on page 83, John brings to the table the depth of background that only two decades on the job can provide—and that only *Electronics* can share with you.

GOSCH: Recalling the early days and Miss Electronica.

Electronica, which is held in even-numbered years, has always been a good indicator of the industry's direction. At his first one, John says, "I reported, 'The trend toward solid-state applications is gaining momentum in Europe despite grumblings by some old-time designers who still cling to engineering practices of the past.' And, quoting a German engineer, I cabled New York, 'By and large, European integrated-circuit manufacturing methods are at best what can be termed large-scale laboratory production. And that will be the case for some time to come.' The big issue in those days was Europe's growing technology gap vis-à-vis the U. S.—no word of a Japanese threat back then. How things have changed."

Probably the most interesting thing about Electronica is how the show got started and how fast it has grown, says John. It began in the early 1960s, when American electronics companies operating in Germany were looking for a forum where they could display their wares. They were turned down by the Hanover Industrial Fair, so they approached a number of cities, among them West Berlin, Munich, and Frankfurt, to organize an exhibition devoted solely to components. Munich was the first to say yes.

"The first show," says John, "was a regional affair, and it was given little chance of being repeated. There were around 100 companies (not only American, but many small German outfits that also couldn't get into Hanover), and they didn't even fill three exhibition halls. On their stands they displayed products from an additional 300 companies. Total attendance was 13,400." This year, there will be 2,284 exhibiting companies from 36 countries, with 125,000 visitors expected.

John finds Electronica an exciting event, but he misses the good old days when it was like a club where the competitors were also friends. "In fact, in 1968 it was decided to name a Miss Electronica—a woman working at the stand of a UK company won. But at the next show, when the big German companies came aboard, it became a no-nonsense, strictly professional and businesslike affair. No more Miss Electronica contests after that."

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OCTOBER 30, 1986

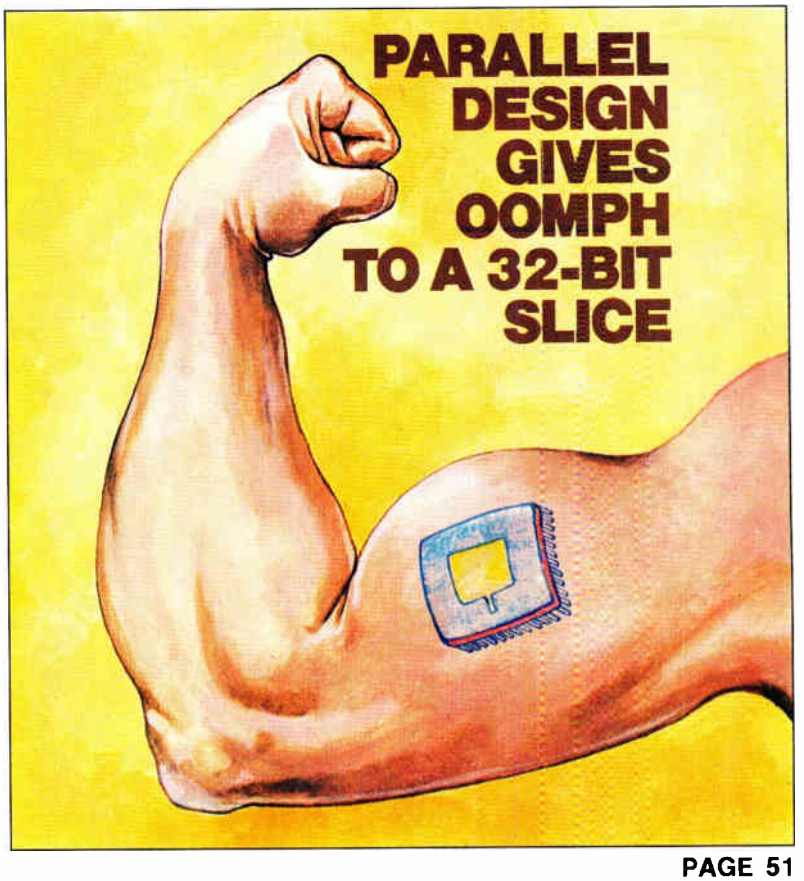
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: ART DIRECTOR FRED SKLENAR



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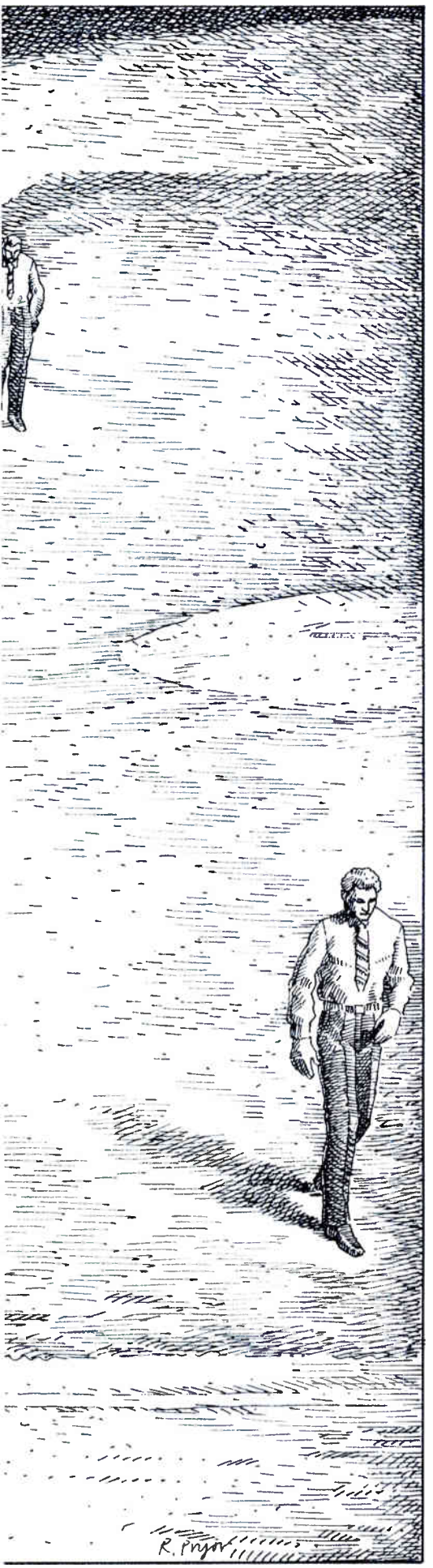
NEW PRODUCTS

DEPARTMENTS



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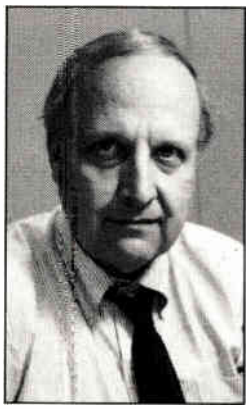
Wyle's Clough is also an optimist: 'If my assumptions are right, we're looking at a good, strong, up year in 1987 for the U.S. semiconductor business



One more optimist has checked in to support our Sept. 4 column. We had stuck out our neck to declare that every time we heard grim forecasts for the semiconductor industry, it would end up bouncing back higher than ever. And that this was going to happen once again. "In every past cycle, the gloom and doom is at its deepest level just before the upturn," reminds Charlie Clough, president of Wyle Laboratories, the El Segundo, Calif.-based semiconductor distributor.

A long-time industry watcher, Charlie makes a strong case for a big 1987 for the U.S. semiconductor industry. "If my assumptions are right," he maintains, "we're looking at a good, strong, up year in 1987 for the U.S. semiconductor business—on the order of 30% to 35% industry growth." Here is how Charlie dopes it out:

The primary reason for his bullishness is the extremely low level of semiconductor inventories at U.S. equipment makers. As these companies burned chip inventory in 1985 and again in 1986, they caused the deepest decline in semiconductor history. Inventories fell more than $3 billion, and they are still dropping. They had doubled from $3 billion in 1983 to $6 billion in 1984, the single largest factor driving the chip market to a record high that year.

"We are now at the same point in the semiconductor cycle that we were in early 1982," Charlie figures. The industry then had just gone through the first wave in a cycle that was later called the "false blip." The error signal had come from the small-to-medium equipment builders who had finally balanced their semiconductor inventories after a long and deep recession. When distributor orders started soaring as a result, in April of that year, chip makers turned euphoric and believed their recession was over. But an eight-month period of discouraging decline followed, Charlie reminds us, because the large mainframe makers didn't return to the market until the end of 1982.

"Now I believe we are approaching a point where the large electronics manufacturers will have their inventories below their end-equipment run-rate requirements, just as happened at the small-to-medium size electronics company in the first quarter of 1986," Charlie says. And when that happens, "their return to the marketplace after a two-year absence will cause a very sudden and high demand on the semiconductor industry."

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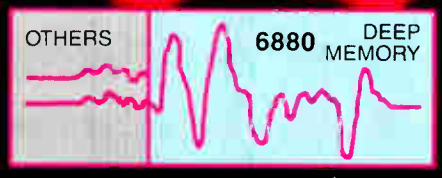

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MEETINGS

Sensors '86 and Autofact '86, Society of Manufacturing Engineers (One SME Drive, P.O. Box 930, Dearborn, Mich. 48121), Westin Hotel, Dearborn, Mich., Nov. 11-13.

Electronica '86 and 12th International Microelectronics Conference, Munich Fair and Expositions GmbH, *et al.* (Postfach 12 1009, D-8000 München 12, West Germany), Munich Trade Fair Center, Munich, Nov. 11-15.

International Workshop on Moisture, Measurement, and Control for Microelectronics, National Bureau of Standards, *et al.* (Dr. Didier Kane, Rome Air Development Ctr., Griffiss AFB, N.Y. 13441), NBS, Gaithersburg, Md., Nov. 12-14.

International Electronics Packaging Conference, International Electronics Packaging Society (114 N. Hale St., Suite 2B, Wheaton, Ill. 60187), Sheraton on Harbor Island–East, San Diego, Calif., Nov. 17-19.

Conference on Magnetism and Magnetic Materials, American Institute of Physics, *et al.* (Diane S. Suiters, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, D.C. 20005), Hyatt Regency, Baltimore, Md., Nov. 17-20.

Scientific Software for Supercomputing, National Bureau of Standards (Francis Sullivan, A151 Technology Building, NBS, Gaithersburg, Md. 20899), NBS, Gaithersburg, Md., Nov. 17-20.

Plastics in Electronics, Business Communications Inc. (9 Viaduct Rd., Stamford, Conn. 06907), Crowne Plaza Holiday Inn, Stamford, Conn., Nov. 18-19.

Wescon '86, IEEE (Electronics Conventions Inc., 8110 Airport Blvd., Los Angeles, Calif. 94303), Convention Center, Anaheim, Calif., Nov. 18-21.

PRONIC '86: International Exhibition of Equipment and Products for Electronics, Société de Diffusion des Sciences et des Arts (20, rue Hamelin, F 75116 Paris, France), Porte de Versailles Exhibition, Paris, Nov. 18-21.

Microcontamination Conference and Exposition, Microcontamination Magazine (Expocon Management Associates Inc., 3695 Post Rd., Southport, Conn. 06490), Santa Clara, Calif., Nov. 18-21.

MIL-STD-1553B: Applications, Developments, and Components, ERA Technology, Ltd. (Laura Christie, Seminar Organiser, ERA Technology Ltd., Cleeve Road, Leatherhead, Surrey KT22 7SA, UK), Regent Crest Hotel, London, Nov. 25-26.

Power Electronics and Variable-Speed Drives '86, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL, U.K.), National Exhibition Centre, Birmingham, England, Nov. 25-27.

Electronicom '86, IEEE (Richard Brostrom, Berger & Associates Canada Inc., 133 Richmond Street W., Suite 203, Toronto, Ontario M5H 2L5), Toronto Convention Centre, Toronto, Canada, Dec. 1-3.

GLOBECOM '86: Global Telecommunications Conference 1986, IEEE (Ross Anderson, Southwestern Bell, Room 706, 3100 Main Street, Houston, Tex. 77002), Westin Galleria Hotel, Houston, Tex., Dec. 1-4.

National Database and 4th Generation Language Symposium, Digital Consulting Associates, Inc. (6 Windsor St., Andover, Mass. 01810), Ritz Carlton Hotel, Boston, Dec. 2-5.

2nd International Conference on Artificial Intelligence, Institut International de Robotique Et d'Intelligence Artificielle de Marseille (Viviane Bernadac, IIRIAM, 2 Rue H. Barbuss, 13241 Marseille Cedex 1, France), Marseilles, France, Dec. 2-5.

Controls West '86, Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Long Beach Convention Center, Long Beach, Calif., Dec. 3-5.

IEDM '86: International Electron Devices Meeting, IEEE (Melissa Widerkehr, Courtesy Associates, Inc., 655 15th St., N.W., Washington, D.C. 20005), Westin Bonaventure Hotel, Los Angeles, Calif., Dec. 7-10.

International OEM, Penton Exhibitions (Bill Little, Penton Expositions, 122 E. 42nd St., New York, N.Y. 10168), Jacob Javits Convention Center, New York, Dec. 9-11.

Microcomputer Graphics Show and Conference, Expoconsul International Inc. (3 Independence Way, Princeton, N.J. 08540) Jacob Javits Convention Center, New York, Dec. 17-19.

International Winter Consumer Electronics Show, EIA Consumer Electronics Group (2001 Eye St., N.W., Washington, D.C. 20006), Las Vegas Convention Center, Las Vegas, Nev., Jan. 8-11.

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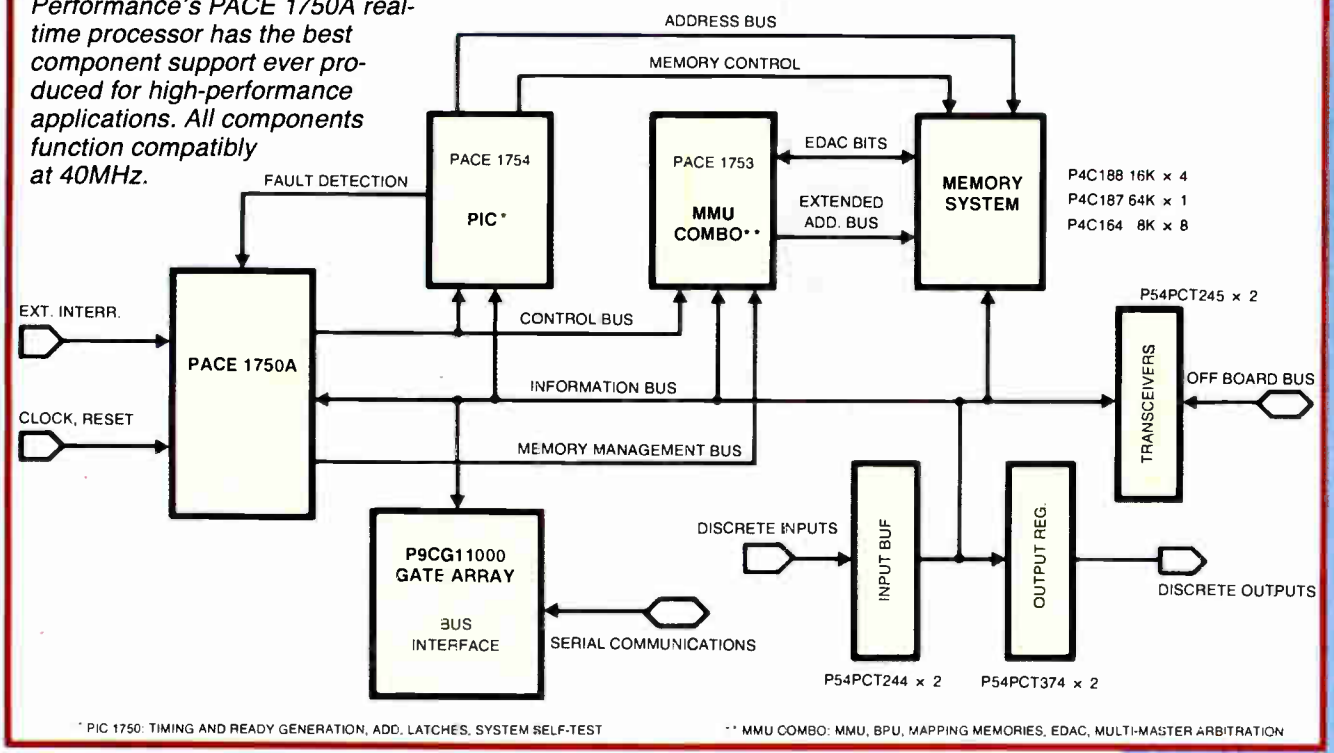

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Electronics 10/30/86

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'CRAZY IDEA' WINS NOBEL FOR BINNIG AND ROHRER

NEW YORK

When Gerd Binnig and Heinrich Rohrer set out eight years ago to build a device that could see individual atoms, their colleagues told them they were "completely crazy." On the other hand, Rohrer recalls, "they also said that if we succeeded we would win the Nobel Prize."

Now the prophecy has come true. The researchers, both career staff members at IBM Corp.'s Research Laboratory in Zurich, will share the 1986 Nobel Prize in Physics with 79-year-old Ernst Ruska, who developed the scanning electron microscope in 1931. Binnig and Rohrer are credited with developing the scanning tunneling microscope, which allows scientists to study the surface of materials in atomic detail. Their invention has already found wide application in materials research at IBM and other electronics companies, and the scientists believe it is also well-suited for biological studies on viruses, cancer, and DNA.

Rohrer sees some important applications for the technology, especially in next-generation computing, which will require submicron geometries and ultrahigh levels of integration on complex silicon and gallium arsenide substrates. "There is already talk of doing lithography with this technique," he says. The technology may eventually be used to make physical changes to a material, he says.

Binnig, a native of West Germany, and Rohrer, a Swiss, will share their half of the $290,000 cash prize; Ruska will collect the rest. But Binnig, 39, and Rohrer, 53, say they have not thought much about what they will do with their cash award. Rohrer says that he might build a new house.

When news came earlier this month that they had won, the two were swamped with congratulations from their 120 colleagues at the Zurich labs, and by phone calls from news organizations and friends. "I never experienced anything in my life like this," says Binnig, who joined IBM in 1978 after earning his PhD in physics from Johann Wolfgang Goethe University in Frankfurt, West Germany. "It was really something, all this excitement and all these people coming to shake hands."

The research project was not the result of years of academic contemplation, but rather the fruit of a short discussion on the physical phenomenon of tunneling, in which electrons will jump from one surface to another when the two surfaces are held close together and a current is applied. Still, it took 30 months before Binnig and Rohrer saw their first pictures.

"When we started, I was personally convinced that it would work, but when it did, it really surprised me," says Rohrer, who joined IBM in 1963 after earning his PhD at the Federal Institute of Technology in Switzerland. "It's so amazing that such a primitive instrument could work. Really—it's like a rusty nail you drag across a surface."

LAUREATES. IBM's Heinrich Rohrer, left, and Gerd Binnig share the 1986 Nobel Prize in Physics.

The microscope is not that simple. The primary components are a tiny tungsten probe, so fine that its tip is a single atom, and a small clamp to hold the material under study. A small current is applied, creating an electric field between the probe and the material surface, and the probe slowly scans the surface, following its contours atom by atom.

The result is a TV-like image that maps the landscape on the material's surface; each hill is an atom. The technique allows researchers to actually see how atoms bond. Moreover, Rohrer says that the design has been refined so that now resolution is between 0.7Å and 0.8Å. "Now you can actually see the shape of individual atoms," he says.

The most difficult development challenge may have been finding a way to keep the material and probe completely free of vibration. The probe and the material must stay within 5Å to 6Å of each other for the phenomenon to work, so scanning tunneling microscopes consist primarily of shock-absorbing equipment. The systems, which can be about as small as a grapefruit, must be operated in a vacuum. *–Tobias Naegele*

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SEIKO INSTRUMENTS

Circle 17 on reader service card

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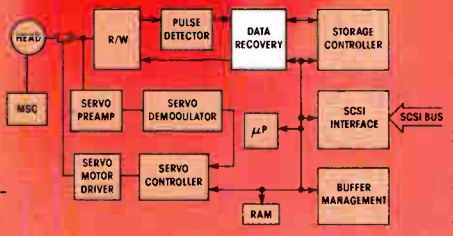

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ELECTRONICS NEWSLETTER

TI ENLISTS VIDEO-7 TO HELP DEVELOP GRAPHICS INTERFACE

There's a war raging in the 32-bit graphics-processor market between Texas Instruments Inc. and Intel Corp. as each tries to get makers of graphics products to use its chip. In the latest round, TI has signed up Video-7 Inc. to help it develop a standard interface, based on the TI TMS34010 Graphics System Processor chip, for the IBM PC and PC AT. The work will include both silicon and software that will be made available as part of the TMS 340 family. Video-7, Milpitas, Calif., is already a major player in the market for Enhanced Graphics Adapter cards; it says that it will be the first to incorporate the new Microsoft Windows driver of the TMS34010 into a high-resolution graphics product. TI's chip was announced last January [*Electronics,* Jan. 27, 1986, p. 67]. Intel's, the 82786, came out in the spring [*Electronics,* May 19, 1986, p. 57]. □

AMD AND SIEMENS SCHEDULE A PIXEL-CONTROL CHIP

TI and Intel are pushing complete graphics coprocessor ICs, but others play on a lower level of integration by developing chips to be used as parts of coprocessors. One of those players, Advanced Micro Devices Inc. of Sunnyvale, Calif., says it will begin shipping samples of its own graphics chip, the Am95C60 quad pixel dataflow manager, in the first quarter of next year. Siemens AG of Munich will second-source the chip in Europe. AMD, now in beta test, promises full production by the second quarter of 1987. □

WITH INVESTORS FRIGHTENED OFF BY SUIT, LATTICE SKIPS PAYDAY

The patent infringement suit brought against Lattice Semiconductor Corp. by Monolithic Memories Inc. apparently has indirectly dealt a powerful blow to the 3½-year-old Portland, Ore., firm. Lattice said last week that because of the suit, several current investors had refused to take part in its $10 million fifth round of financing. In order to keep afloat, Lattice stopped paying its professional employees, offering them stock and bonuses instead if they stayed on. Nevertheless, 33 of the 176 people in the company's total workforce quit their jobs rather than wait, the company says. The salary holdup may last as long as three months, an internal memo said. Secretaries and employees covered by minimum-wage laws are being paid. The company also persuaded its suppliers to accept deferred payments. "We haven't run out of money," a spokesman says. "However, we are paying essential bills only." Meanwhile, the investment house of Drexel Burnham Lambert is trying to recruit more investors to complete the financing. In its suit, Monolithic Memories, of Santa Clara, Calif., charged that the programmable logic circuits made by Lattice and Altera Corp. were infringing on its programmable array logic patents [*Electronics,* Sept. 18, p. 23]. Lattice has since filed a $100 million countersuit. A Lattice spokesman says that bookings remain high, with the largest single-day bookings, $1.8 million, occurring this month. □

MOTOROLA TO STAGE SRAM SPEED RACE AT WESCON

Motorola Inc. is reacting to the fierce competition in fast static random-access memories with a whimsical marketing gimmick. The Austin, Texas, operation, which offers 64-K parts with speeds of 25 ns, will challenge its SRAM competitors to an access-time race on the floor of next month's Wescon '86 in Anaheim, Calif. Motorola managers in Austin, Texas, plan to have a high-speed tester installed in their booth to measure the speed of parts submitted by customers and competitors. The stunt will be called "The Motorola Shmoo-out at the Wescon Corral." Test programs will record each chip's access time on a Shmoo plot. □

ELECTRONICS NEWSLETTER

UNIVERSITY OF ILLINOIS FINALLY GETS PLATO'S PRICE DOWN...

Plato, the computer-based instruction system that has always been too expensive to fulfill its once-heralded potential, is about to get significantly cheaper. Researchers at the University of Illinois, where Plato was developed 26 years ago, have come up with an approach that relies on new, inexpensive computer hardware as well as satellite transmission to deliver instructional materials more cost-effectively from a central mainframe to remote terminals. Conventional Plato systems rely on older computer hardware and land-based phone lines, and can cost a user around $60 per month per terminal in long-distance charges. The so-called NovaNET system can run for one-tenth that price, says an official. Control Data Corp. of Minneapolis, which has rights to market Plato, has chosen not to license the satellite-based technology. So NovaNET will will be marketed by a university spin-off company, University Communcations Inc., in Urbana, Ill. □

...BUT CONTROL DATA SAYS IT HAS A BETTER IDEA

Now that it has decided not to license the NovaNET technology for Plato, Control Data Corp. says it plans to pursue an even less-expensive approach for low- to medium-volume users, one that does away with mainframe communications costs—which can be as much as 50% of delivery cost. The first example is at an American Airlines training facility, where CDC is installing a Plato system that uses IBM PC AT-compatible work stations teamed with central file servers. CDC has offered work-station-based Plato before, but never on such a powerful machine and always for stand-alone use. The installation is the first Plato from CDC to rely on a local-area network. □

BUILT-IN SELF-TEST EASES CHECK OF ASIC-EMBEDDED MEMORY

Testing the memories embedded in application-specific integrated circuits may be one of the most time-consuming and expensive tasks an ASIC user encounters while building custom parts into a system. AT&T Co. is taking aim at that problem with built-in self-test circuitry, which makes testing embedded random-access memories almost automatic. At a cost of about 3% of the chip's total area for each on-chip memory block, it can track memory faults to a single pin or gate and can study bridging faults and pattern sensitivities, says David Aadsen, the Bell Laboratories staffer who incorporated this approach into AT&T's ASIC compiler. Aadsen estimates that this self-testing can cut development costs by 10% or more, but he points out that there may be a more significant advantage to the added circuitry: system designers can use it in system-level testing. □

GaAs MARKET ESTIMATES ARE CALLED OVERLY OPTIMISTIC

Those market studies that several years ago predicted gallium arsenide chip sales would soon amount to billions of dollars missed the mark badly, says a new report by The Information Network. The San Francisco market researcher says the main reason is that the low levels of integration of initial GaAs chips did not provide enough functionality to be cost-effective to customers. "Suppliers are wasting their time trying to establish an MSI and SSI [medium- and small-scale-integration] standard," says Robert N. Castellano, who wrote the report. Also, the suppliers underestimated the lead times from design to chip insertion for military equipment, which drives the GaAs market (see p. 29). As a result, the worldwide market for GaAs devices will not reach the billion-dollar level until 1991, when sales will be $1.184 billion, he says. Analog integrated circuits will have the lion's share, some $667 million, compared with $85 million in 1986. □

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Circle 21 on reader service card

At 11:40 p.m. on April 14th 1912, the *RMS Titanic* struck an iceberg some 400 miles off the coast of Newfoundland. In less than three hours, the 'unsinkable' luxury liner had sunk to the sea bottom in one of the worst maritime disasters of the century. Finding her became a commitment by oceanologists and technologists alike.

Several tried. All failed. For the problems, like the tragedy, were on a grand scale. The North Atlantic is not known for its hospitality. And the freezing waters are nearly 2.5 miles deep. To add to these difficulties, not only was *Titanic's* last radio position known to be inaccurate, but fierce currents had also swept her away in a south-easterly direction.

Last year, however, after the French ship *le Suroît* had covered 80% of the target zone, the French-American expedition team embarked on the high-technology research ship *Knorr*.

This high-technology included a pair of MAGNAVOX* satellite navigation receivers - one providing highly accurate position information by tracking satellites of the new global positioning system, the other providing periodic position updates from transit satellites. With these two receivers onboard, the *Knorr* was equipped with the most precise and sophisticated marine navigation system available.

The MAGNAVOX receivers were used to criss-cross the remaining 20% of the search area, working to a position accuracy of just 35 meters. Even in heavy seas. Then, starting from the most likely spot, the underwater search vehicle *Argo* was lowered to begin close-up investigation.

At 1:05 a.m. on September 1st, 1985, her video cameras recorded the eerie outline of one of *Titanic's* mighty boilers. The seventy-three year search was over.

Little wonder that our satellite navigators are used aboard thousands of offshore platforms, rigs and ships - including *Queen Elizabeth II* - and that our global positioning system receivers are leading the way in precise navigation, on land, at sea and in the air.

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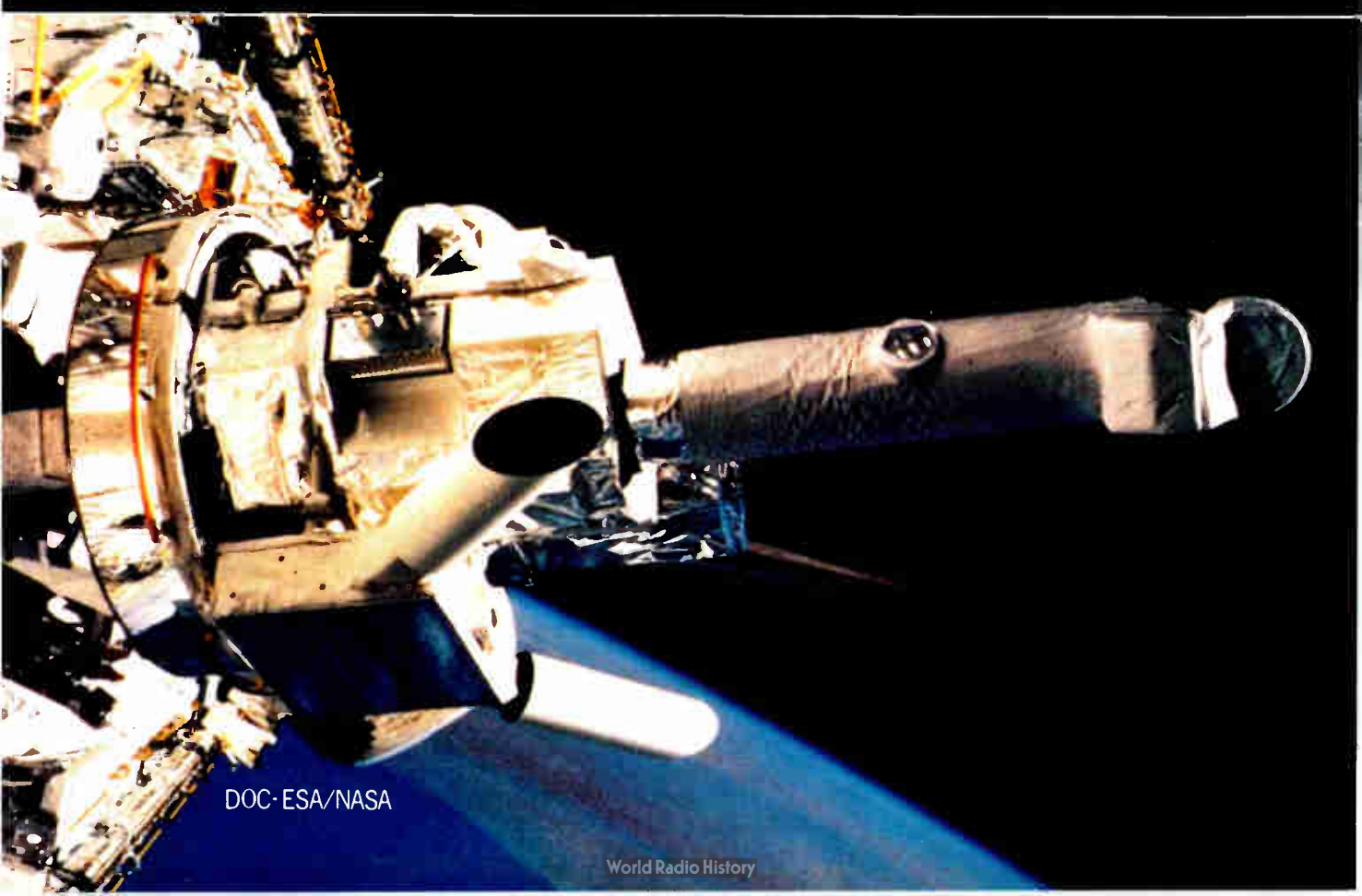

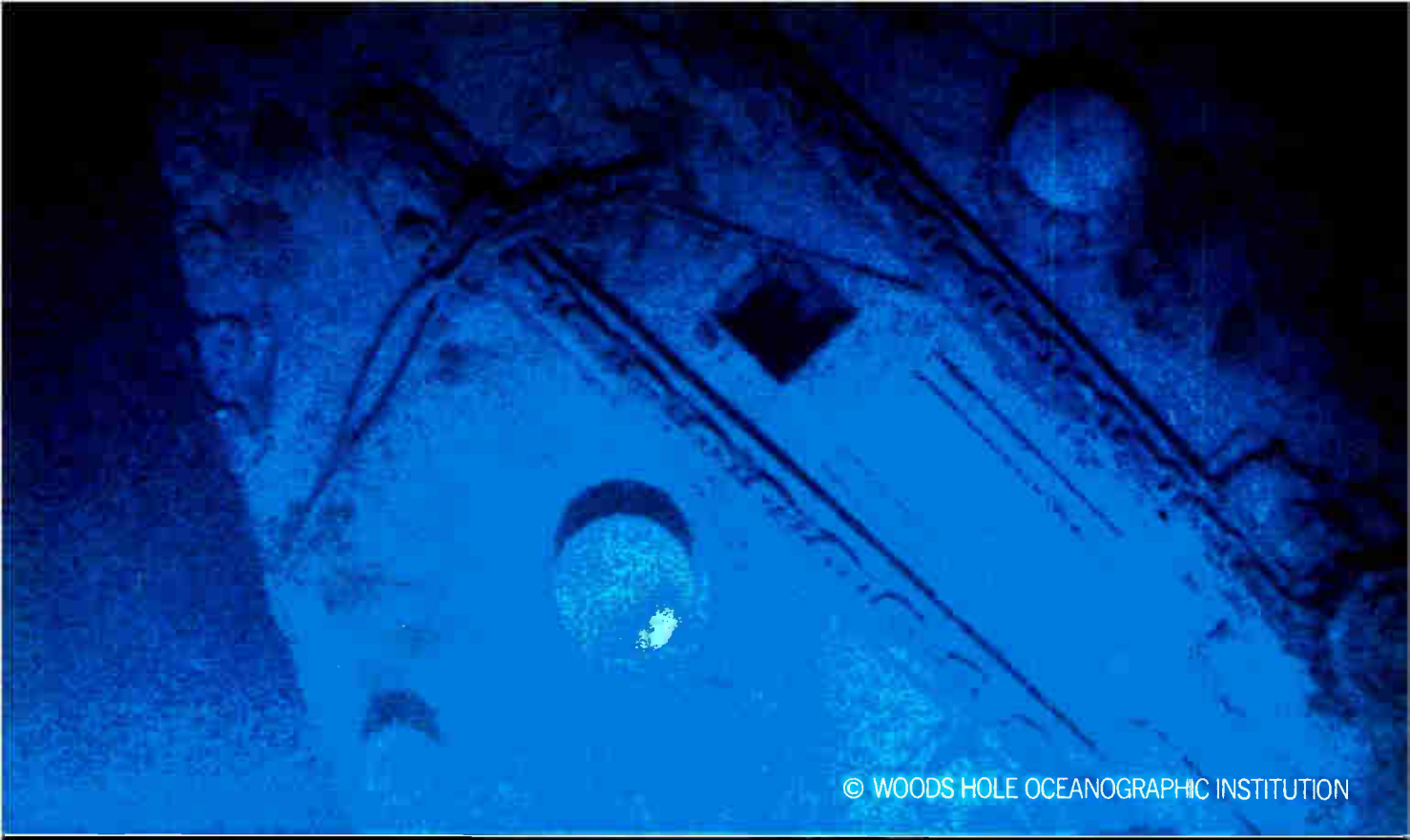

wing where to look. Philips.

From the depths of the ocean to the depths of space. One of the most demanding endeavours is the scientific exploration of the sun - a research programme conducted by NASA in collaboration with the European Space Agency, ESA.

Key to this research is SPACELAB 2; fifteen tons of advanced space technology launched in August 1985. The problem was how to ensure that, once in orbit, SPACELAB 2's platform, with the powerful telescope, could be manoeuvred under remote control without any sensitivity to the shuttle motions.

The solution was provided by three SODERN** SED 04 star trackers integrated by Dornier in the Instrument Pointing System responsible for positioning the platform. Each of these electronic sensors operates to an accuracy of 0.75 seconds of arc - which is roughly equivalent to a golf ball seen from 10,000 meters. Distance, however, is no problem, for the platform responds perfectly to every command from mission control some 300 km below. Which is hardly surprising, for similar SED trackers have been operating on EXOSAT for over 3 years.

In fact, SODERN, as world leader in attitude measurement and star tracking, has been involved in major European and U.S. space programmes, providing over 90 opto-electronic systems with more than 200 years of operation without a single failure.

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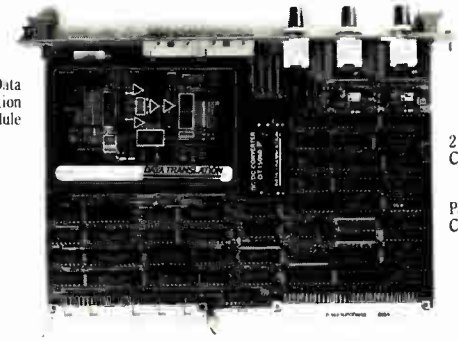

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PRODUCTS NEWSLETTER

TWO CMOS VERSIONS OF 1750A MICROPROCESSOR INTRODUCED

Squaring off in toe-to-toe competition for the military digital avionics microprocessor market, Performance Semiconductor Corp. and LSI Logic Corp. have each announced CMOS chips functionally equivalent to Performance's 1750 bipolar device. Performance, of Sunnyvale, Calif., calls its 1750A the world's fastest single-chip implementation of the MIL-STD-1750A instruction set. Available in 20-, 30-, and 40-MHz versions, the fastest version executes the complete Digital Avionics Information System benchmark at 2.6 mips and consumes less than 1 W. LSI Logic's 1750A implementation is rated at 25 MHz and is available as a single device or as a cell in a larger chip. The Milpitas, Calif., company will introduce it at the 1750 users conference next week in New Orleans. □

DESIGN TOOLS FOR LOW-DENSITY GATE ARRAYS RUN ON IBM PC AT

Monolithic Memories Inc. is pegging its move into the low-density gate-array market to a set of menu-driven design tools that execute all design functions, including simulation, on IBM Corp. PC AT and compatible computers. Monolithic Memory's gate-array family, built in a sub-2-μm twin-well, double-layer CMOS process, has eight members ranging from 720 to 6,000 gates. The Santa Clara, Calif., company offers an integrator module that converts PAL designs to gate arrays, and a library of 200 TTL macros. The complete system, with the PC AT, costs $30,000. □

REACTOR PROMISES $75 EPITAXY COST FOR GaAs WAFERS

Crystal Specialties Inc. should draw a lot of attention at Semicon in Tokyo this December. Its Model 411 metal-organic chemical-vapor-deposition reactor offers the promise of a seven-fold cut in the cost of growing epitaxial layers on 3-in. wafers in production volumes compared with molecular-beam epitaxy. Claiming a yield of 1,000 wafers a month in continuous operation, the Portland, Ore., company estimates an average epitaxy cost of about $75 per wafer, compared with $500 per wafer using MBE. A producer of laboratory epitaxy equipment for 12 years, Crystal claims its $350,000 Model 411 yields research-grade results in high-volume production—specifically, high uniformity and precise junction lines for gallium arsenide and other III-V and II-VI materials. □

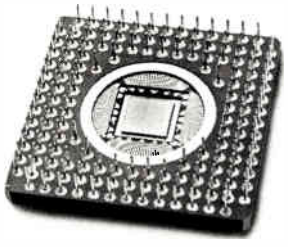
FIBER-OPTIC MODEM MULTIPLEXES TO GET 19.2-K-BYTE/S DATA TRANSFER

A new fiber-optic modem from AT&T Technology Systems Inc. transmits data in full duplex over a single strand of fiber, multiplexing fast enough to be fully transparent to the user while maintaining the 19.2-kilobyte/s rate called for by the RS-232-C standard. Designed to replace the standard RS-232-C connector, the asynchronous RS-232-2 has two control lines and two data lines. It costs $105 in 100-unit quantities; $85 in orders of 1,000. □

INMOS CASCADABLE DSP RUNS AT 320 MILLION OPERATIONS/S

By combining thirty-two 16-by-16 multipliers and thirty-two 36-bit adders on a single CMOS chip, Inmos Corp. has attained processing speeds of 320 mips in its IMS A100 cascadable digital signal processor. The Colorado Springs subsidiary of the Bristol, England, company is aiming the device toward high-speed communications, radar, speech processing, and image processing. The chip will be shown at Wescon in Anaheim, Calif., Nov. 18-22 and at Electronica in Munich Nov. 11-15. The IMS A100 costs $406 each in 100-unit lots. □

This is a Motorola semi-custom chip.



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MIMIC COULD DO FOR GaAs WHAT VHSIC IS DOING FOR SILICON

WASHINGTON

A dozen or more contractors submitted proposals last week to run a major new military development program that could do for gallium arsenide what VHSIC is doing for silicon technology—vastly accelerate the technological learning process. Called MIMIC, for microwave and millimeter-wave monolithic integrated circuits, the effort should give the U.S. a big boost in an area where experts say Japan currently leads.

While VHSIC (for very high-speed integrated circuits) aims primarily at logic circuitry such as microprocessors and other computational elements, MIMIC aims at producing a reliable and affordable supply of complex GaAs chips for the next generation of communications and weapons-sensor hardware. As Kenneth Entwistle, contract officer for the MIMIC effort, says, "VHSIC is the brains, while MIMIC is the eyes and ears."

Such GaAs devices are not being produced commercially because of excessive costs and technology limitations. DOD planners concluded last year that these parts might never surface without a program to encourage their development.

Procedurally, MIMIC resembles the VHSIC effort, which was launched for similar reasons more than five years ago and is now starting to turn out silicon ICs for military customers. And as MIMIC picks up momentum, the tie between the two will become closer, since they will be run by the same officials, according to a spokeswoman in the VHSIC office. Lead agency for MIMIC is the U.S. Army's Electronics Technology and Devices Laboratory in Ft. Monmouth, N.J., which received last week's industry bids for the initial Phase 0 stage.

The reliability goals of MIMIC are much more stringent than for previous GaAs chips. Failure rates for packaged chips cannot exceed 0.006% per 1,000 hours, at a 60% statistical confidence level, operating over the full military temperature range of −55° to +125°C.

The Army document that seeks Phase 0 proposals is called a Broad Agency Announcement and is considered by military contractors to be a way of streamlining initial procurement. About 300 announcements went out, and—based on the DOD's experience—up to 15 contractors, most of them working in teams, are likely to respond. The VHSIC office plans to issue a formal request of its own for proposals later this year, but contractor sources say that the same companies will likely take part, and the Army and VHSIC-office MIMIC programs would essentially merge.

Among the teams bidding on MIMIC are GM-Hughes Electronics and General Electric, Texas Instruments with Raytheon, Westinghouse Electric and Rockwell International, and TRW with Honeywell.

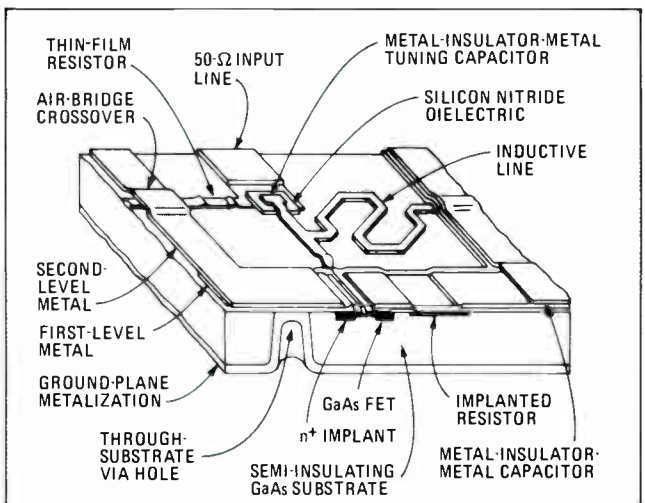
The word among contractors is that perhaps nine will be chosen around late January for the 12-month Phase 0. Follow-on Phases 1 and 2 will likely run 36 months each, and Phase 3 will be carried out in parallel with them. DOD is asking for upwards of $135 million to fund MIMIC for the 1987 fiscal year.

Although the Phase 0 announcement asks prospective suppliers only for a "technology road-map/plan" leading to building devices in Phases 1 and 2, the outlines of the entire program are clearly visible. Besides calling for the expected requirements for computer-aided design techniques, circuit layout, and testing, MIMIC also emphasizes the need to improve materials and manufacturing processes in order to achieve higher-volume production and reasonable yields, both of which are major problems for GaAs chip makers. Phase 3 sets up research programs at industry and university labs at the same time as the Phase 1 and 2 devices are developed.

Volume "is the key issue for the kinds of very complex circuits MIMIC needs," says Robert N. Castellano, a San Francisco-based market analyst. "Not enough experience has been gained so far in turning out large-scale GaAs ICs. Everybody is still at the SSI and/or MSI level." Castellano, president of The Information Network, recently completed an extensive study of the GaAs business. He says that only the U.S. military has the buying clout to spur GaAs development.

The small circle of GaAs chip makers is enthusiastic about MIMIC, which can foot the bills for expensive, and heretofore largely neglected, research. "There's a tremendous need for improving the technology across the board," says Hughes Aircraft Co.'s Eugene H. Gregory, in a typical view. He agrees that yields and volume have high priority, but he says the basic materials step—growing better GaAs crystals—is a key job. Gregory heads Hughes' MIMIC effort for the Radar Systems Group, El Segundo, Calif., where he also is chief scientist of the Rf System Laboratory.

The types of circuits sought by MIMIC typically operate above 2 GHz, combine digital and analog functions, and integrate a number of passive and active components (see figure). Castellano points out that their complexity makes



TRICKY. The Pentagon is moving to spur development of microwave GaAs chips, whose many features make their fabrication complex.

them very difficult to build—they require up to 11 mask levels, including a metal-semiconductor FET structure.

But the GaAs performance is indispensable for transmitter and receiver modules in new phased-array radar systems, satellites, and avionics packages. Such top-priority programs as the Milstar satellite program and radar for the Strategic Defense Initiative are among many potential applications.

Because speed is inherent in GaAs devices, MIMIC does not emphasize performance, as does VHSIC, but it does require substantial radiation hardening. The MIMIC circuits must operate in a radiation environment of at least 10^6 rads, compared to the total-dose requirement of 5×10^4 rads for VHSIC Phase 2 devices. *–Larry Waller*

MILITARY

IBM HITS 1-MICRON LEVEL ON PHASE 2 VHSIC CHIPS

NEW YORK

The race to produce 0.5-μm chips for Phase 2 of the Defense Department's Very High Speed Integrated Circuits program is tightening up. IBM Corp. revealed last week that it has produced functional prototypes of two 1-μm chips for Phase 2. It says it will have first silicon of 0.5-μm parts by mid-1987.

The other two competitors in the hard-fought race, TRW and Honeywell, also have recently delivered test chips to the DOD. All three companies are proving out their technology.

To meet the requirements of the four-year Phase 2, the contractors must produce working chips with 0.5-μm design rules by 1988. The three are following different strategies—IBM, for example, is using CMOS for its five-chip set, and Honeywell is using bipolar technology to produce its five devices. TRW plans a set of six "superchips," which will incorporate features such as self-configuration, a triple-redundant bus, and automatic repair using on-chip spare components. Four of them will be built in CMOS, and the other two will use triple-diffusion bipolar technology [*Electronics*, July 10, 1986, p. 49].

IBM's Federal Systems Division, Manassas, Va., appears to have a slight edge over TRW and Honeywell with its new 1-μm prototypes. Shrinking the designs to the required 0.5 μm is still a major challenge, but the company has processed some test devices at 0.5 μm.

GOING FOR BROKE. Honeywell, however, is the surprise contender. It is pushing directly from the 1.25-μm technology of Phase 1 to the 0.5-μm requirements of Phase 2. George A. Anderson, VHSIC submicron program director for Honeywell's Solid State Electronics Division in Plymouth, Minn., says the company expects to send its first 0.5-μm circuit design, a bus interface unit, to the foundry before the year's end.

The bus-interface chip, which is scheduled for September 1987 delivery, will be joined on the line by an array processor unit, the largest of the set with about 30,000 gates, and an 18,000-gate array processor controller. The final ICs in Honeywell's set are two 50-MHz memories built with Phase 1 technology: an 18-K random-access memory and a 144-K read-only memory.

The Honeywell bus-interface chip will integrate about 16,000 gates. It will eventually be enlarged to encompass about 28,000 gates for use in a brassboard demonstration of an electro-optic signal processor scheduled for October 1988. Honeywell, which is using electron-beam technology for 12 of the 14 production steps, will get first-pass parts on the other two logic circuits late in the third quarter of 1987, according to Anderson.

TRW Inc., meanwhile, is developing and testing its technology piecemeal, producing devices that incorporate only elements of the circuits it hopes to produce. This approach tests the macrocell architecture of TRW's superchips. TRW says it has a 750-K memory now in fabrication using both the 1.25-μm CMOS design rules developed under Phase 1 and some 1-μm features.

One reason for IBM's two-tiered approach of first proving designs at 1 μm and then shrinking them by half may be a switch in tactics—though Big Blue isn't offering an explanation. In Phase 1, it used n-MOS technology to produce its 1.25-μm parts. Now it is switching to CMOS, essentially starting over. Bob Estrada, VHSIC program manager at the Federal Systems Division, says IBM shifted because "we believe CMOS is really a preferred technology for DOD systems."

CMOS technology's small appetite for power makes it ideal for military systems that often rely on battery or generator power, Estrada says. Moreover, "the real benefit of CMOS is that it is also attractive from a radiation-hardening point-of-view," an important consideration since such hardening is mandated in the VHSIC contract. CMOS also offers very good performance and density profiles when contrasted with competing technologies, he says.

GROUNDWORK. In proving its 1-μm CMOS process, IBM is laying the groundwork for what it hopes will be an easy migration to smaller line widths. The 1-μm technology supports between 20,000 and 50,000 equivalent gates on each chip. So far, it has produced functional 1-μm devices for its bus interface unit and an 18-K configurable static RAM chip, which carries some logic in addition to memory. IBM's other three parts are on the 1-μm pilot line now.

One of the three chips is a signal processor for which IBM is building elements—memory modules, switching modules, and processor modules—that can be tailored for service in a number of military programs, including the Generic Space-Borne Computer being developed for the Strategic Defense Initiative. *–Tobias Naegele*

INTERNATIONAL TRADE

EQUIPMENT MAKERS BID TO MODIFY IC TRADE PACT

SAN MATEO, CALIF.

Increasingly worried that high prices being set for Japanese memory chips by the Commerce Department will drive their manufacturing offshore, U. S. equipment makers are trying hard to meet as soon as possible with U. S. chip makers. Their goal simply is to gain the support of semiconductor manufacturers in modifying the U. S.-Japan semiconductor trade agreement. "An alliance between users and semiconductor management is one way to get a lot of political leverage in Washington," says Andrew J. Kessler, industry analyst at PaineWebber Inc., in New York.

THOMPSON: U. S. chip makers and users need to set up dialogue, says AEA vice president.

The American Electronics Association is the prime mover in setting up the talks, which will not include either Commerce or the Office of the U. S. Trade Representative. "There is a very clear need for a producer-user dialogue," says AEA vice president Ralph Thomp-

son. For three months, chip users have waited for relief from the high "foreign market values" set under the terms of the trade agreement—and they found the prices released in mid-October not much more satisfying than the initial figures, which came under heavy fire from users when they were set in August [*Electronics*, Sept. 18, 1986, p. 32].

"While the new FMVs are lower than the first round, they are still too high," says users' group chairman Stephen C. Schmidt, chief operating officer of Tandem Computers Inc., Cupertino, Calif. "There is a real risk that the electronics industry is going to continue to seek alternative methods—specifically offshore purchasing and manufacturing—rather than buy at these prices."

But the users leave no doubt that they would rather talk than flee offshore. "We want to meet with the semiconductor makers to find a more viable, proactive way to revitalize the semiconductor industry," Schmidt says. "Putting higher prices on parts not made here anyway won't help them."

It is the pricing assigned to dynamic random-access memories, for which there are few U. S. suppliers, that is the burr under the users' saddles. Accustomed to stuffing boards with cheap Japanese DRAMs, chip users balk at paying a premium that they claim handicaps them against foreign competition. There is much less controversy over erasable programmable read-only memories, for which there are many U. S. suppliers and no big price differentials.

Chip makers say the FMV structure is based on true costs and that the users are trying to perpetuate an unfair market practice in which they can buy below cost.

The AEA, whose membership includes both producers and users of semiconductors, took the lead in arranging a meeting between them, and last week Thompson began contacting each side. The initial response from the semiconductor faction was cautious but positive. "Any extent to which we can develop further understanding of the trade agreement is worthwhile," said George Scalise, vice president of chip maker Advanced Micro Devices of Santa Clara, Calif., and government affairs representative of the Semiconductor Industry Association.

The plan for negotiations is one of the first suggestions from the AEA semiconductor users' group, which was formed last month to make a belated response to the chip agreement. The systems houses did not take part in the long negotiations leading to the agreement, an omission they are beginning to see as a serious mistake.

"The semiconductor group has been working on this problem for a year and a half," says Edwin Lee of Prolog Corp., Monterey, Calif. "The process went on without adequate involvement of the downstream people. There was an honest attempt to protect us, but it wasn't good enough."

Having missed the chance to influence the agreement itself, the AEA group wants a say in how it is implemented. It would like to eliminate the setting of FMVs, for instance, on chips that are not offered by any U. S. supplier, such as certain high-performance 1-Mb DRAMs. The AEA will promote such goals in further meetings with Commerce Secretary Malcolm Baldrige and Under Secretary Bruce Smart.

System builders want a say in how the trade pact is implemented

The users agree that they can not live with the new FMVs, Tandem's Schmidt says. Even the lower 256-K DRAM prices of $2.50 to $4 are too high, they say, because the parts are available in Japan for $1.75. With that kind of differential, says Lee, "there will be a migration of jobs to Japan to do board- and system-level manufacturing."

Users trying to buy U. S.-made DRAMs have few choices. Micron Technology Inc. of Boise, Idaho, is about the only game in town. Texas Instruments Inc. is just beginning to ramp up production in its new Dallas DMOS IV line.

LINE FIXED. While TI says "a significant share" of its fourth-quarter DRAM production will come from Dallas, the new plant lags far behind its twin in Miho, Japan. The Dallas plant, which was opened a year ago, has been modified since coming under the control of the Miho management last spring [*Electronics*, June 2, 1986, p. 11].

NEC America Inc., Mountain View, Calif., the subsidiary of Japan's NEC Corp. that is the other U. S. DRAM source, says it is not accelerating production at its Roseville, Calif., plant beyond normal rates. In fact, most Japanese DRAM makers are reportedly cutting production in the face of a glut that is overflowing into the gray market.

Schmidt says the lure of Japanese parts and offshore production could change purchasing habits in ways that would be hard to reverse. "There are other parts on those boards besides memories," he says. "There will be a tendency to buy those overseas, too."

Moving offshore, however, is not a panacea. Michael Boman, purchasing di-

THE TRADE PACT SPARKS A THRIVING GRAY MARKET

At least one form of Japanese export business has taken off since the U. S.-Japan semiconductor trade pact was signed: the gray market.

Small trading houses shipping 256-K dynamic random-access memories to customers in Taiwan and Southeast Asia at unit prices close to $1.85 are apparently getting all the business they can handle. But the major Japanese chip makers' exports generally are as flat as a wafer, although the products of each had different "foreign market values" (FMVs) assigned to them by the U. S. Commerce Department in mid-October, and at least two Japanese companies are fairly well pleased with the FMVs they were assigned.

The Japanese Ministry of International Trade and Industry is demanding full production information from the major makers before it will grant export licenses, but it hasn't cracked down on the small exporters, perhaps because they're shipping to Asian markets, not the U. S.

Chip users in the U. S. say there's no shortage of cheap memory in Asia. "Both governments have been optimistic about their ability to police these markets, but they haven't been able to do it," says one user, who declines to be identified. "Even within the context of the agreement, there are lots of ways to get cheap parts. They are available in Japan: a broker who buys parts from a Japanese company will have to agree not to ship them out of the country, but that buyer can resell to another party without that provision."

The major chip makers depend heavily on the U. S. market, and they are reporting mixed effects from the trade pact. NEC Corp. appears to be in the best position to sell in the U. S. Its FMV price is about $3 for 256-K DRAMs, and it has a U. S. plant that makes DRAMs, which it can sell for any price it chooses.

Toshiba Corp., the leading 1-Mb DRAM maker, is said to be delighted with the $19.31 value assigned to it for those chips. Industry sources say the company is selling 1-Mb products for as little as $15 in the Japanese market, where the average price is close to $22.

At Hitachi Ltd., third-quarter U. S. sales are down from the second quarter, and its FMV of $4.01 for 256-K parts is not helping. Fujitsu Ltd., which didn't provide enough data for FMV evaluation, reportedly has been tagged with an even higher $4.50 figure, and industry sources say the company, more dependent on memory-chip sales than the other DRAM makers, is in deep trouble.

–Michael Berger

rector of the Kaypro Corp., San Diego, says the rush of systems houses to establish offshore facilities has clogged up the channels to the point at which it may take three to six months to set up a reliable manufacturing site. "By the time the bugs are out of it, we could be past the DRAM problem," he says.

Many users pin their hopes on achieving some sort of détente with semiconductor suppliers. There's no clear idea of how to do that, though, because the chip makers, still mired in the worst slump in industry history, see the trade pact as an important barrier to further encroachment by Japanese firms. "We need to work in an interdependent way to recapture semiconductor manufacturing in the U.S.," the AEA's Thompson says. *-Clifford Barney*

DATA PROCESSING

A NEW WAY TO TIGHTEN SECURITY IN PC NETWORKS

RICHARDSON, TEXAS

User-friendliness is something everybody wants in a personal computer—except security-conscious managers who are worried about the vulnerability of PC networks to unauthorized access. Now, however, a Texas microsystems-engineering company says it can resolve the conflict between easy operation and secure operation with a protection mechanism that can lock out unwanted access to hardware or software.

Triad, which Micronyx Inc. plans to introduce next month at Comdex in Las Vegas, is one of the latest personal-computer-security products aimed at assuaging fears over the unbridled use of desktop computers in large networks—fears that executives at Micronyx, in the Dallas suburb of Richardson, say are far from unfounded. Information leaks cost U.S. businesses between $100 million and $500 million worth of data every year, the company says. Personal computers in large networks can aggravate the problem—they function as a giant, unlocked file cabinet, connected to a lot of built-in, high-speed copiers. Micronyx and others in the business want to reconcile the inherent lack of security of single-user personal computers with network environments, says Micronyx president W. Mark Goode.

NEW TWISTS. As its name implies, Triad takes a three-pronged approach to security. Like some existing security products, it puts proprietary software and expansion boards to work behind the scenes while application programs run on IBM-compatible personal computers. But to better prevent unauthorized access to personal computers, peripheral ports, and encrypted files stored on disk, Triad adds a couple of new twists. First, the system double-checks users after they turn on the machine. It uses an electronic "key" inserted into a socket in a half-sized expansion card. Second, a file-labeling technique limits access to files to authorized users.

The card, which contains memory and both semicustom and standard logic, performs background processing to prevent the security tasks from bogging down the computer's central processing unit. The key, made by Dallas Semiconductor Corp., is a small cartridge containing user-verification data in memory kept alive by a lithium battery. The key cartridge has built-in mechanisms that prevent its data from being copied.

Micronyx's file-labeling technique allows computer users exclusive access to designated software and data. The labels, which consist of 24 bytes of ownership information, tell Micronyx's hardware who created the data object, when it was created, and what can be done with it. The data or software is encrypted by Triad, which intercepts the files and inserts the label before they are stored on disk. The label itself is also encrypted.

"When a file is called up by a PC user, the system takes out just enough of the encrypted label to see who owns it. If the user is not authorized to access the file, the system will put the label back and leave the file safely on the disk," explains Goode.

The label does not interfere with the operating system or application programs. It provides what is called access control to data objects, such as spreadsheet and word-processing files. This opens up the possibility of adding utilities and operating-system services for access control similar to those used in large multiuser environments.

Goode says the system has hooks in it to incorporate the security features into other software packages. Micronyx is negotiating with several large software houses in Europe and personal-computer program vendors in the U.S. to modify their software so it will support Triad.

"We don't claim that this is hacker-proof," Goode says. But he adds that his engineers have cracked all competing products on the market in about 30 minutes.

HARD TO COME BY. Triad's kind of security doesn't come easy. Goode says he talked with seven U.S. federal agencies, the armed services, the White House, three British government branches, and nearly 50 companies as part of the research and development work on Triad. He came up with 25 principles aimed at securing personal computers without disturbing their operation. "We have erected a very sophisticated technical gateway that forces a user to expend an enormous amount of time and money before he can steal anything," he says.

The National Computer Security Center, a division of the Defense Department, has begun an initial evaluation of Triad and Micronyx's underlying personal-computer-security system, which is known as the Workstation Management Architecture. Micronyx hopes the two-stage evaluation and development process—which can take up to three years to complete—will result in a DOD-approved high-security personal-computer system for the military.

One way the Triad technology could be tailored for government use is in a file-backup system that would allow a mainframe to copy all the hard disks in the attached PCs and then erase the original data at the end of a work day. "This happens every day in the government environment, where sensitive files are collected at the end of the day

LOCK IT UP. Micronyx's personal-computer-security system uses an electronic key and encrypts files.

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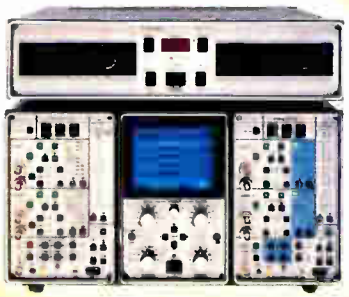

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and put under lock and key," Goode notes.

Micronyx is not alone in its pursuit of government and corporate personal-computer-security business. For example, Fischer-Innis Systems Corp., Naples, Fla., has been marketing Watchdog, a software-based product, since 1983. While Triad's end-user cost will be $795 in single-piece quantities, Fisher's all-software approach keeps the retail price down to $295 and avoids the use of expansion slots. Some competitors, however, say protection packages that rely solely on software are vulnerable to hackers. *–J. Robert Lineback*

PACKAGING

HIGH PIN-COUNT ASICs MAY GET NEW JEDEC PACKAGE

NEW YORK

A new family of high-pin-count chip carriers for application-specific integrated circuits has a good chance of becoming a Jedec standard before the year is out. The new package is the result of the efforts of Indy Electronics Inc., a Manteca, Calif., company that assembles chips in packages, and a group of chip vendors that agreed that far too many package types are being used for high-pin-count ASICs.

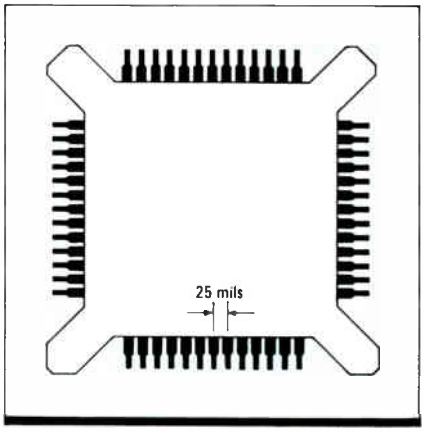
The seven plastic carriers, with pin counts ranging from 52 to 244 pins, use gull-wing leads set on 25-mil centers. Small bumpers protruding from the flat packages' corners protect the delicate leads during board assembly and allow chips to be mounted for maximum board density. The technique was pioneered by AT&T Co.

Indy Electronics set out to organize a committee of industry experts to develop a standard when orders for packages with more than 100 pins started coming in last winter. Indy sold the idea to several major chipmakers, among them Intel, Motorola, National Semiconductor, IBM, and AT&T. After several months of wrangling over competing designs and methodologies, the Ad Hoc Committee on High-Pin-Count Plastic Chip Carrier Standardization emerged from a meeting in August with a proposal for Jedec's JC-11 packaging committee. Late last month, the Jedec committee overwhelmingly approved the measure. It is now before the general membership on a special ballot, and the vote should be in by mid-November.

100 PINS. "We received numerous calls in the last year from customers who were going to require packages that had more than 100 pins," says Jeffrey Braden, vice president for advanced technology at Indy. "So we perceived a need, especially for ASIC and systems-house guys, to develop a standard."

The first meeting, held at Semicon West in May and scheduled to last only half a day, drew 13 companies and about 20 engineers, Braden says. Support grew. Forty-eight people from about 20 companies attended the second meeting, and at the third meeting, in August, more than 50 people from 33 companies were on hand. It was at that gathering that the issue of whether or not the packages should include the protective bumpers came to a head.

"When you're dealing with fine-pitch packages, the leads are very difficult," Braden says, explaining why bumpers are useful. "At the second meeting, the committee almost overwhelmingly voted down the bumpers. It wasn't until the third meeting that we began to see a strong sentiment to keep them."



BUMPERS. AT&T's chip carrier with lead-protecting bumpers may soon be a standard.

The bumpered package was developed at AT&T Co.'s Bell Laboratories and has been in use for certain AT&T parts for several years. Harry Scholz, the IC packaging expert at Bell Labs in Allentown, Pa., who led AT&T's delegation to the meetings, was surprised that competitors were unwilling to go along. "We thought using bumpers was the best way to go about protecting the leads, but we really got shouted down," he says. "We kind of went away with our tail between our legs."

Unwilling to take defeat so easily, Scholz began calling colleagues around the industry to find out what caused the resistance. He discovered that much of the problem was tied to AT&T's patent on the technology—the other companies were afraid AT&T would demand royalties—and he persuaded his company that opening up the patent would be in everyone's best interest. "That swayed a lot of our competitors," Scholz recalls.

It didn't sway everyone. Signetics, the Sunnyvale, Calif., subsidiary of Philips NV, for example, opposed the proposal at the August meeting. "The addition of a new package family will only increase confusion, because we already have so many different packages for surface-mounting," says Francisco Osegueda, a Signetics packaging engineer.

COMPROMISE. Signetics has softened its stand, however, adopting a wait-and-see position. The design has merit, Osegueda says, adding that using bumpers is "a very good concept." Scholz says AT&T was willing to compromise on some of the finer issues to get its basic package accepted as a standard.

The job is not finished yet. Indy and Intel Corp. are still working on a standard for the lead frames the packages will need, and Jedec approval is likely. Braden believes "there is about a 50% chance it will become a standard at the December Jedec meeting." Failing that, he puts odds at 99.9% that it will be a standard by March.

Indy is already gearing up to make the packages. "We will have the 100-lead version tooled and ready for samples by Nov. 1," Braden says. "The 132-lead part will be ready by Feb. 1."

–Tobias Naegele

NETWORKING

SOFTWARE MAKES NETS TRANSPARENT TO USERS

NEW YORK

A communications software package could go a long way toward rendering moot the competition among supporters of Ethernet, token-ring, and other local-area-network technologies. Touch Communications Inc. says its product allows different LAN implementations to work so well together that users won't care what kind of network it is to which they're connected. The LANs themselves will become invisible.

The software, called Touch OSI, is now being tested at the Boeing Computer Services Group, a Seattle-based subsidiary of The Boeing Co. Boeing is using it to connect computers that use different operating systems—IBM Corp.

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*Samples available 4 Qtr. 1986

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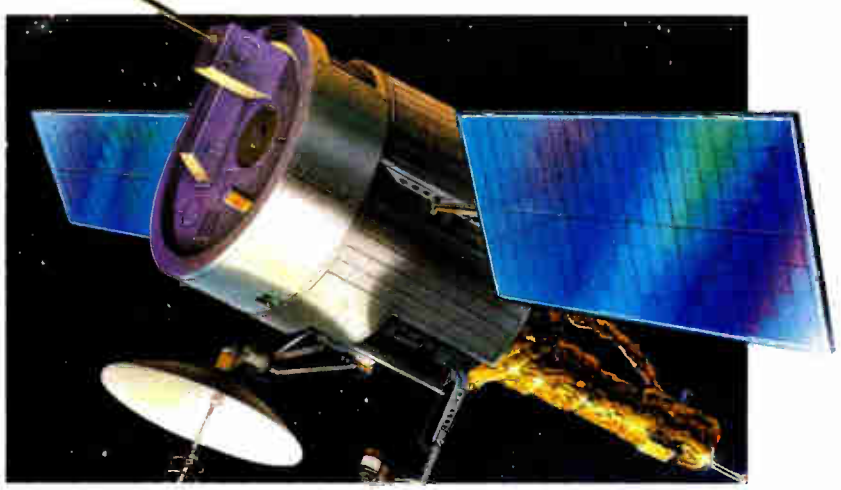

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Circle 37 on reader service card

NETWORK ERASERS. Touch Communications' Bass and McGann are working to make networks transparent to users.

Personal Computers running under PC-DOS and Digital Equipment Corp. machines running under VMS.

Touch Communications, Scotts Valley, Calif., is the newest venture of networking veteran Charlie C. Bass, cofounder of the well-known LAN vendor Ungermann-Bass Inc. The company has already demonstrated that its new software can act as an internetwork router, connecting Manufacturing Automation Protocol and Technical Office Protocol (MAP and TOP) networks.

NO INTERVENTION. If the Boeing tests go well, applications running on DEC equipment situated at Ethernet nodes will be drawing data from IBM gear at token-ring nodes, and vice versa, without user intervention. Although a similar product, from Retix, a Santa Monica, Calif., software house, can also connect dissimilar equipment, it requires the user to integrate the LAN package with the various local operating systems.

Touch OSI is based on the higher levels—layers 3 through 7—of the Open Systems Interconnection reference model, which provides a framework for communications between dissimilar processors. Developed by the International Organization for Standardization, OSI is a seven-layer partitioning of logical entities that provide different classes of network services: the lower layers provide transmission services and the upper layers support applications processes.

Touch OSI intercepts input/output requests and maps them to basic file-transfer access management (FTAM) operations described in the OSI model. By doing so, it makes all networks and services appear as extensions of the user's computer. "The significant value [Touch Communications] is adding is transparency" between the two operating systems, says Laurie Bride, manager of networking technology in Boeing's Network Services Group.

To implement that transparency, the Touch software acts as an interface that appears as a set of modules for applications programmers writing I/O routines for file-based operations. The modules match the various models and libraries that accompany the programming languages the developer is already familiar with. They make it as easy to write an I/O operation for a remote printer or disk drive as it is to write one for a local device.

"The common [programming] model for integrating Touch OSI is to intercept local I/O requests," says L. Brian McGann, Touch's vice president of engineering. "We work with any local file access, turning it into an elemental file-system request and determining if there is a network request. If it is a network request, we map the I/O request to a sequence of FTAM operations. Any remote machine that is FTAM-compliant reacts, and then we map the data back into the local environment. This is at such a low level that the user and application don't know that they are not operating in the local environment."

Similar software from Retix provides implementation of layers 2 through 7 of the OSI model; it has been available for about a year. But Retix leaves it up to the buyer to integrate the OSI protocols into the local operating system, unless the buyer signs a contract to have Retix do the work, says M. Charles Fog, vice president of marketing for the Santa Monica company.

Like Retix, Touch Communications claims its products conform to MAP and to TOP, MAP's counterpart for office-automation communication, as well. The product does not have formal MAP certification, concedes Dennis Morrison, general manager of Touch OSI products. But he points out that it has been used for linking MAP and TOP networks. He cites the successful May demonstration of a layer-3 network router between IEEE 802.3 Ethernet networks and 802.5 token-ring networks at the first combined meeting of MAP and TOP users' groups, which was held in Seattle last May.

'CULTURALLY CONSISTENT.' However, Touch Communications executives insist that Touch OSI is more than a gateway between two dissimilar networks. What makes it important is its potential for ease of communication among different kinds of computers, Morrison says, since it provides a "culturally consistent" interface for users: as they create, copy, or move files between dissimilar machines, they use the command syntax of their own machine. Users do not have to learn operating-system command structures they don't already know, Morrison says, because "all network resources appear in a syntax the user is familiar with." *–Robert Rosenberg*

CONSUMER

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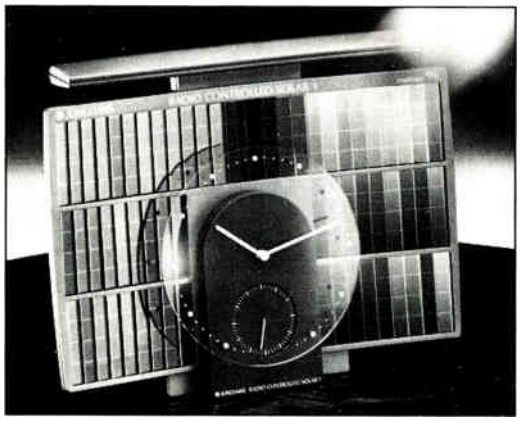
SCHRAMBERG, WEST GERMANY

One of technological man's oldest dreams is a device that measures time with the utmost accuracy and that runs indefinitely without human intervention. Such a perfect timepiece has become reality at Junghans Uhren GmbH, a 125-year-old Schramberg company.

The RCS 1—for radio-controlled solar—keeps track of time so precisely that it will take 150,000 years for it to deviate 1 second from astronomical time. This precision derives from a cesium atomic clock, the most exact time standard today.



ULTRAPRECISE. The RCS 1 clock picks up radio signals controlled by a cesium clock and adjusts itself.

There are no plans to enter the mass market with the RCS 1 as it is built now. Rather, now that a prototype has been made, plans call for building another 156 by the year 2000—that is, one per month till the end of this century—at a prestige price of more than $20,000.

Junghans expects competition, however, and to stay a step ahead, it is working to miniaturize the design and to get the cost down to a level that consumers will accept. Wolfgang Ganter, director of development

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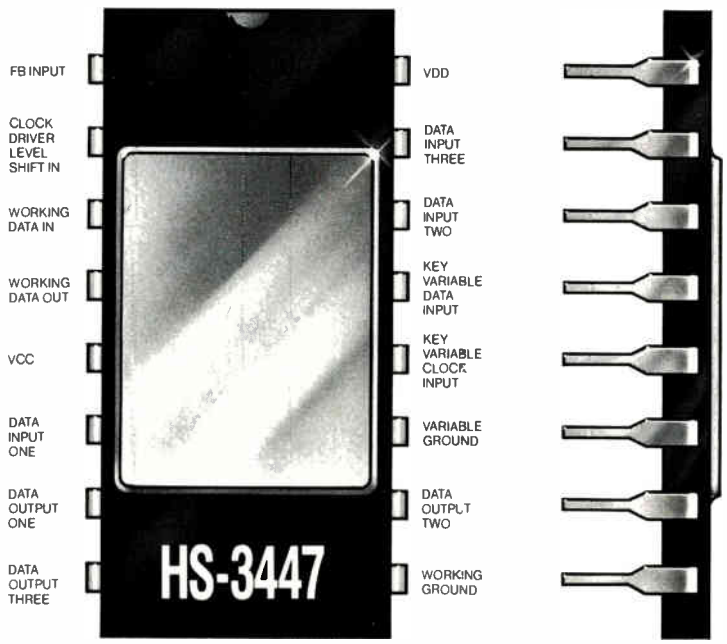

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TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
TC514256 - 12	256K x 4	CMOS	120 ns	Fast Page	20 pin
TC514258 - 10	256K x 4	CMOS	100 ns	Static Column	20 pin
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TC55257L - 10	32K x 8	CMOS	100 ns	100μA MAX	28 pin
TC55257L - 12	32K x 8	CMOS	120 ns	100μA MAX	28 pin

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at Junghans, says wristwatches based on the same principles are conceivable.

The RCS 1 picks up radio signals that carry time-data messages. Controlling this signal is the cesium clock at West Germany's Physical-Technical Institute in Braunschweig, an agency akin to the U.S. National Bureau of Standards, which keeps a similar clock and transmitter in operation in Boulder and Ft. Collins, Colo., respectively.

The West German agency continuously transmits the time messages from Mainflingen, near Frankfurt, as part of its service to research laboratories and other scientific organizations. The transmitter's range is about 1,200 miles, which covers most of Europe. The message contains signals that automatically switch the RCS 1 clock to show daylight-savings or standard time, so the user never need set the clock himself.

Before a truly worldwide market can develop, time-data signals must be transmitted over more regions than Europe and the U.S. Ganter expects that some day they will be broadcast from satellites.

The clock picks up radio signals from a cesium time standard

The RCS 1 uses a ferrite antenna to pick up the time data, which is amplitude-modulated on a 77.5-kHz signal. A bipolar integrated circuit from West Germany's Telefunken electronic GmbH makes up most of the receiver. The time data is passed to a 4-bit single-chip CMOS microprocessor from Eurosil GmbH, a Telefunken subsidiary.

SELF-ADJUSTING. The microprocessor switches the receiver on and off and decodes the message. It compares the information with the time shown by the clock. If necessary, it delivers pulses to the drive mechanism to adjust the clock hands.

The RCS 1 gets its power from 58 amorphous-silicon solar cells arranged on a panel behind the clock. Together, these cells put out about 1 W when exposed to sunlight. Of that power, however, only 1/6,000 is needed to drive the quartz-controlled clockwork, according to Ganter.

The surplus energy is stored in a capacitor network and is tapped when there is no ambient light. When the panel is not exposed to light, the clock can run in the dark for as long as two weeks. Also, it will operate at light levels as low as 20 lux. If the clock is placed in a dark area, the panel can be detached and put where light will reach it.

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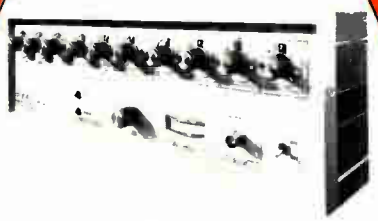

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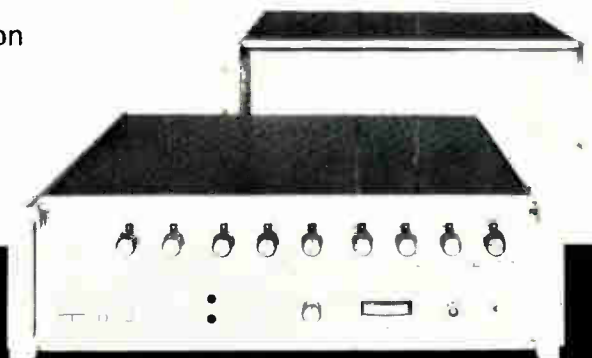

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the RCS 1 takes 50 centuries of clock-technology development work back to the sun, where it began when the Egyptians invented the sundial. "With our new clock we have come full circle," says a Junghans spokesman. "It all started with solar power, and we are now back to solar power." *-John Gosch*

ARTIFICIAL INTELLIGENCE

NTT BUILDS A LISP MACHINE FOR JAPAN

YOKOSUKA, JAPAN

When researchers at Tokyo's Institute for New Generation Computer Technology established directions for Japan's government-backed fifth-generation computer project six years ago, they placed their bets on what was then a relatively obscure artificial-intelligence language: Prolog. Despite the considerable influence of the fifth-generation project, however, Lisp—the AI language most popular in the U.S.—continues to gain popularity in Japan. Recognizing this, Nippon Telegraph & Telephone Corp. has unveiled Elis, a work-station designed to run Lisp programs.

A number of U.S.-made Lisp engines are available in Japan, but none have facilities for use in the Japanese language, as does NTT's Elis. The work station's 64-bit microcoded central processing unit and stack-based memory architecture give it a high level of performance, too. It is said to be several times faster than 3600-series machines from Symbolics Inc. of Cambridge, Mass.

"We chose Lisp because our research showed there is more demand for it [in Japan], but we're not rejecting Prolog," maintains Takashi Sakai, who heads the Data Entry Equipment Section at NTT's Integrated Communications Laboratories in Yokosuka. Elis can also run Prolog programs, but not with the performance it brings to Lisp processing.

The reason for Lisp's continuing popularity, Sakai says, is that Lisp's greater flexibility makes it easier to use in compiling complex data for specific tasks. "The fifth-generation project chose Prolog," says an industry executive, "because it wanted to try something new, and be less dependent on Lisp, which is dominant in the U.S."

Most expert-system programs marketed in Japan are in Lisp, but a lack of data-base material, especially in the medical field, and a lack of AI specialists (industry sources say there are only a few hundred at present) are restricting market growth. Nonetheless, analysts predict the market for AI systems in Japan will grow from its current modest 20 billion yen ($130 million at

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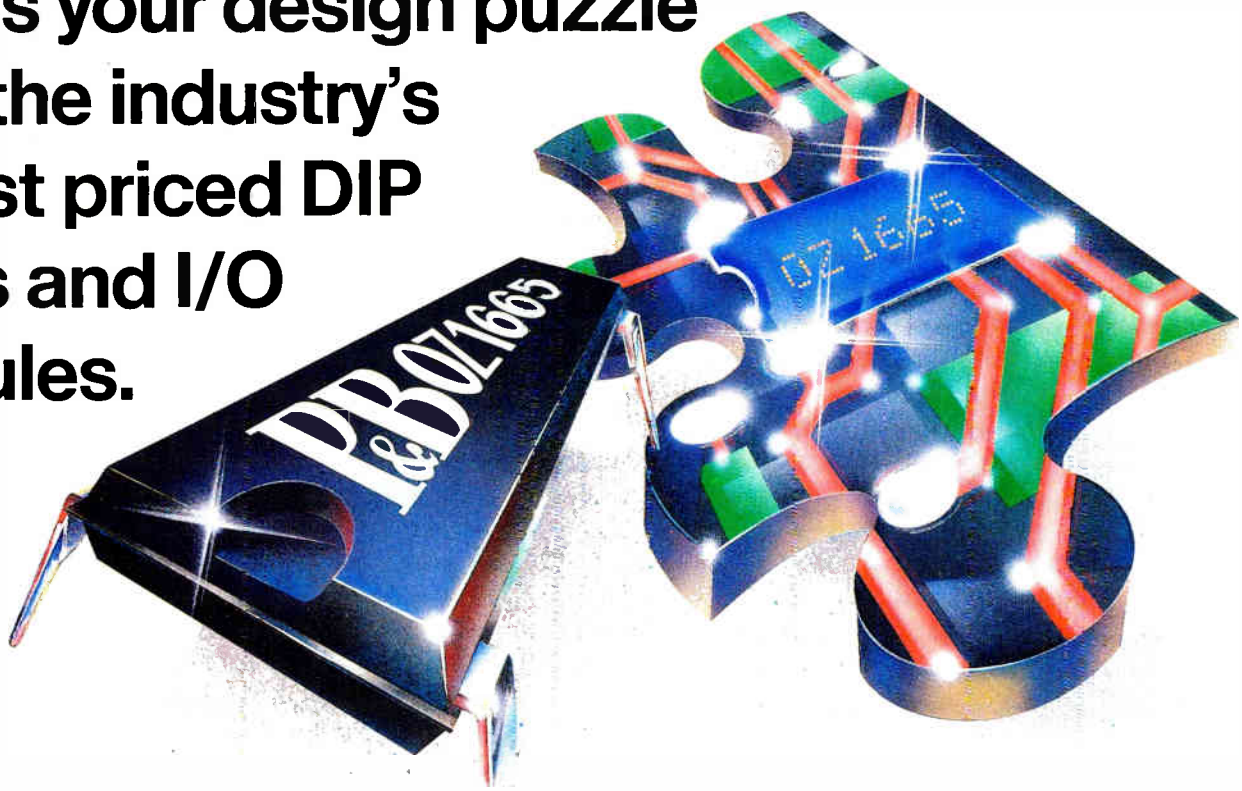

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current rates) per year to 1 trillion yen ($6.45 billion) by 1990.

Lisp engines from Symbolics are among the U.S. AI machines marketed in Japan. They are sold by Nippon Symbolics Ltd., a joint venture of Symbolics and the Nichimen trading house. IBM, Digital Equipment Corp., and Symbolics hardware is also available as platforms for Intellicorp.'s Knowledge Engineering Environment through CSK Research Institute Ltd.

None of the U.S. machines, however, has Japanese-language support. For Elis, NTT has developed Japanese-language data-input facilities for use with English-language programs.

The result of a four-year project, Elis will be on the Japanese market by late next summer, say NTT engineers. Production in the first year will be small, only 20 to 50 units, manufactured by Oki Electric Industrial Co.'s plant at Takasaki. NTT says it hasn't set a price yet for Elis, but NTT feels the product will eventually be a money-earner.

The first Elis prototype had about half the logic of its 64-bit CPU implemented in 2900-family bit-slice chips from Advanced Micro Devices Inc. and

Despite fifth-generation project's use of Prolog, Japanese prefer Lisp

the remainder in Schottky TTL [*Electronics*, Nov. 3, 1983, p. 134]. Much of that logic has now been replaced by one 20,000-gate array chip. This makes it a more compact unit that can sit beside a desk and accommodate four terminals.

A Motorola 68010 microprocessor serves the work station as a front-end processor handling all input/output tasks. It controls a 16-bit bus to which disks, terminals, and other peripherals are connected. A direct-memory-access controller ties this bus to the 64-bit CPU bus. A floating-point accelerator and main memory are tied to the CPU bus.

Among the notable features of the CPU are a very large writable control store—64-K words of 64 bits each—for microinstructions, which support a Tao interpreter. Tao is a dialect of Lisp.

To run programs written in Common Lisp, some functions not found in Tao—about 10% of the functions of Common Lisp—are added in a separate software package. Tao also has functions that support Prolog and Smalltalk.

Fast memory access is a major performance factor, Sakai says. In addition to main memory, which can be as large as 128 megabytes, there is a 32-K-by-32-bit bank of fast static random-access memory configured as a first-in, last-out stack. *–Michael Berger*

INTERNATIONAL NEWSLETTER

EUROPEAN CO-OP TO SPEND BILLIONS ON SUBMICRON TECHNOLOGY

Agreement is near on a $2.5 billion European research effort to develop 0.3-μm chip technology by the middle of the next decade. Three government-industry committees, from France, West Germany, and the Netherlands, are now organizing the Joint European Silicon Submicron Initiative; they are also determining whether to make it part of Eureka [*Electronics*, Dec. 2, 1985, p. 53], Europe's alternative to the U. S. Strategic Defense Initiative. The aim is a research institute set up by West Germany's Siemens AG, France's Thomson Group, and the Netherlands' Philips International NV, with Italy's SGS-ATES likely to join soon. Details on organization, financing, intermediate targets, and government support of the Silicon Submicron Initiative may come by the end of this year. □

BRITISH AIM TO DOUBLE ION-IMPLANTER THROUGHPUT

Researchers in a $5.5 million project funded mostly by the British government have developed an oxygen ion implanter they say can eventually make up to 2,000 silicon-on-silicon-dioxide wafers per week, though they won't say when. The fastest equipment now on the market can produce 500 wafers. The implanter, called Oxis 100, generates a 200-kV, 100-mA beam. That strength is key to the high throughput. The wafers are produced in a vacuum between 400°C and 750°C, a range that maintains the crystallinity of the top silicon surface layer. VG Semicon Ltd. developed the machine with two Atomic Energy Authority facilities, Harwell Laboratory and Culham Laboratory, and semiconductor manufacturers Plessey, British Telecom, and General Electric Ltd. Chips from the wafers have already been sold into the radiation-hardened market, and telecommunications chips have been sold to users in Britain, the U. S., and Japan, says Steve Moffatt, project manager at VG Semicon, which will make and market both the equipment and the wafers. He would not name the customers. Moffatt also refuses to discuss yield and production numbers and won't say when VG Semicon might reach output of 2,000 wafers a week. □

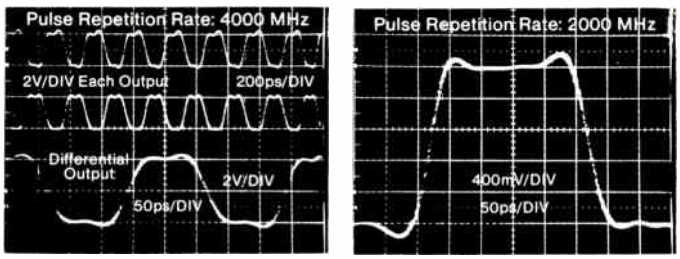
JAPANESE CUT BACK ON CHIP PRODUCTION

Bedeviled by continued soft demand and frustrated by the new Japan-U. S. semiconductor trade agreement regulating prices of dynamic random-access memories exported to the U. S., Hitachi Ltd. has cut production of all chips by 20%, including a virtual shutdown of all production of DRAMS. It is also switching from memory- to logic-chip assembly at its U. S. plants. Industry sources in Tokyo say that Fujitsu Ltd. has made similar cutbacks because of sluggish memory sales in the U. S., which may have dropped drastically in recent months. Prices in Japan for typical 256-K DRAM products have dropped to $1.83 from $1.96. □

STC DEVELOPS LOW-NOISE BIMOS PROCESS

A bipolar-CMOS process from STC Semiconductors Ltd. will yield chips with a noise level of 1 dB at 150 MHz, which "pushes the noise performance of GaAs," says Roger Baker, advanced technology manager. The technology, developed at STC's facility at Foots Cray in South London, uses a 2-μm CMOS process that is a version of STC's planned 1.25-μm process. The first product from the technology, a one-chip telephone containing all functions except a ringing circuit, is expected about mid-1987. The company is also about to start shipping samples of a 45-ns byte-wide 64-K static random-access memory using just the 2-μm CMOS process and plans to have a 1.25-μm version out next with speeds of 25 to 35 ns. □

5000 MHz PULSE GENERATOR WITH 30 ps RISETIME



Above Photos **Include** the 30ps Risetime of the Sampling Head.

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Circle 87 on reader service card

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Electronics
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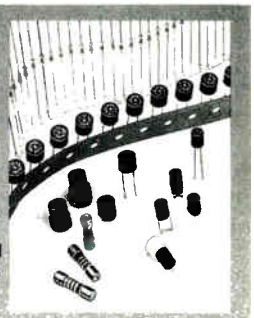

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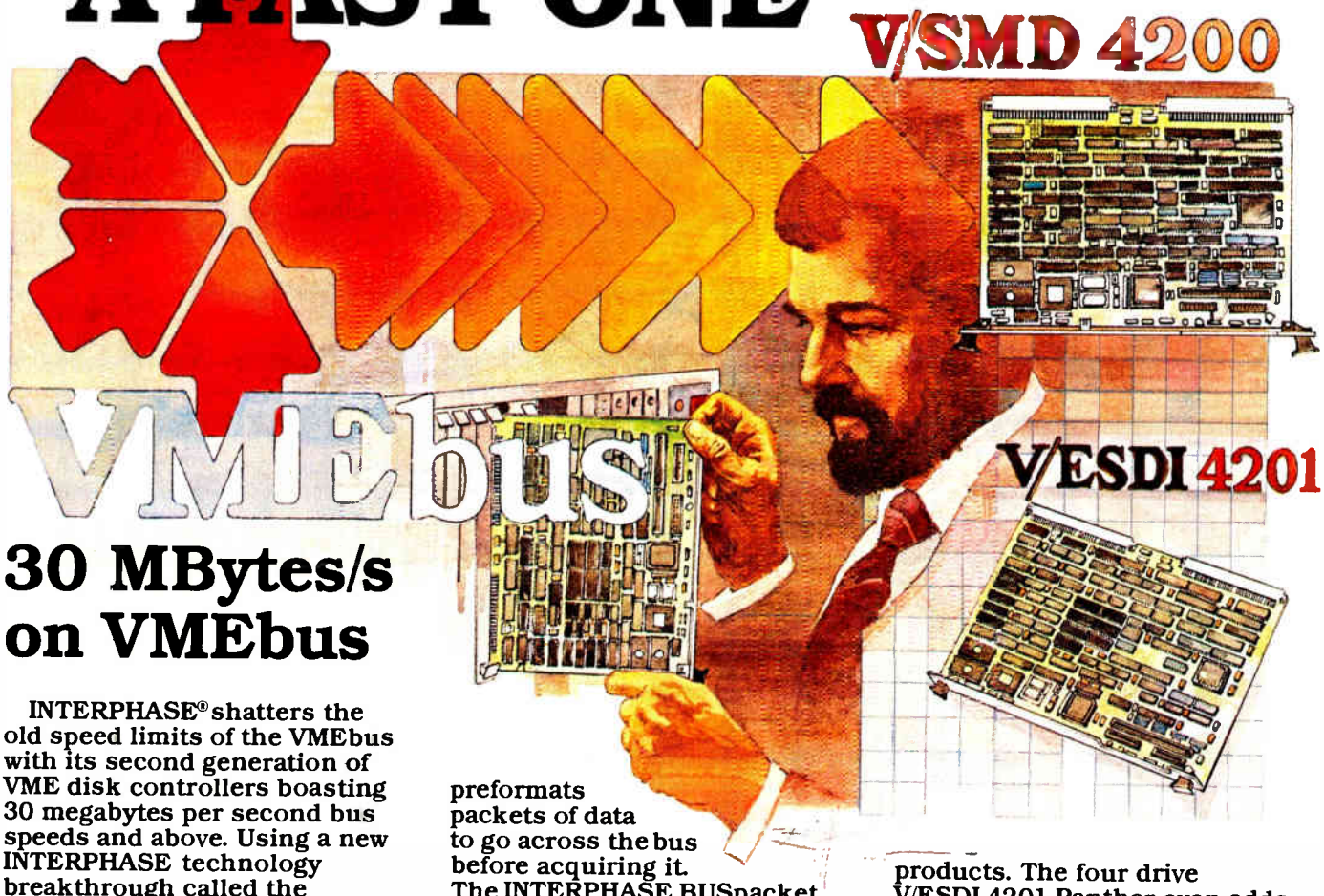

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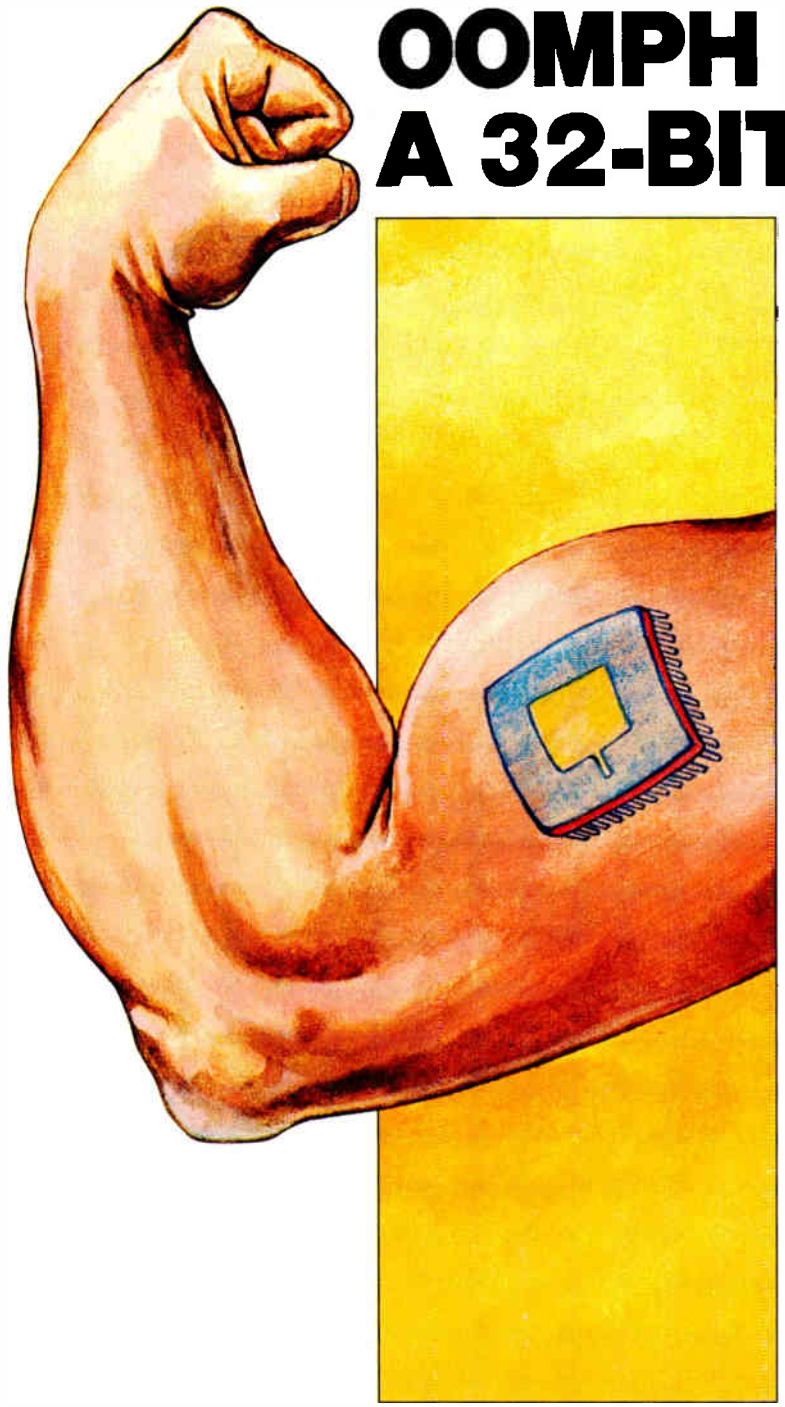
INSIDE TECHNOLOGY

PARALLEL DESIGN GIVES OOMPH TO A 32-BIT SLICE



A powerful 32-bit slice processor, able to perform several operations on data simultaneously in a single clock cycle, can yield highly parallel system designs that boost throughput 4 to 20 times over other available 32-bit slice chips. Integrated Device Technology Inc.'s IDT49C404 is optimized for parallel operations and bit-field manipulation, and it can be expanded into 64-bit word configurations. This new candidate in the 32-bit slice sweepstakes

[*Electronics*, Sept. 4, 1986, p. 64] is a 1.2-μm bipolar-enhanced CMOS design that features an 80- to 100-ns system cycle time—comparable to many bipolar implementations.

More important than raw cycle time, the architectural innovations incorporated into the IDT49C404 make possible the design of highly parallel system architectures that boost throughput dramatically over other 32-bit designs, says John Mick, director of product definition and applications engineering at IDT.

These innovations include a register file with four output ports and three input ports, plus an on-board funnel shifter that is linked sequentially to an eight-function, 32-bit arithmetic logic unit and a 32-bit-wide merge-logic block. This combination allows shift, rotate, mask, and merge operations in a single 80- to 100-ns clock cycle (Fig. 1), says Michael Miller, IDT's manager of product definition and applications engineering. Another innovation is a three-bus architecture designed for bidirectional operations.

Also contained on chip is a powerful 32-bit mask generator, 32-bit counting for matrix operations, and various other features such as byte, word, and double-word operations. The IDT49C404 also incorporates a powerful internal diagnostic capability for detecting and pinpointing hardware failures in a system at any point in the engineering or manufacturing cycles, or at the customer facility after delivery, Miller says. The processor uses a serial diagnostic scheme that requires the use of only four pins; devices with diagnostic capability are cascaded, output to input, into one long serial shift register.

For the 32-bit slice, IDT has developed a CMOS process that combines the low power, high noise immunity, and wide operating-temperature range of traditional CMOS with speed and output-drive capability equal or superior to those of bipolar Schottky TTL. Called Cemos-IIC, it's a 1.2-μm double-layer-metal, twin-well process (Fig. 2) that incorporates both a deep underlying p-well and a shallower n-well formed by altering the doping profile near the surface of the p-channel transistor regions. That makes possible the fabrication of high-performance transistors in both polarities. In addition, to enhance performance and output drive, bipolar devices are used as needed; they are formed from the parasitic structures inherent in the CMOS process.

OPENING UP THE I/O BOTTLENECK

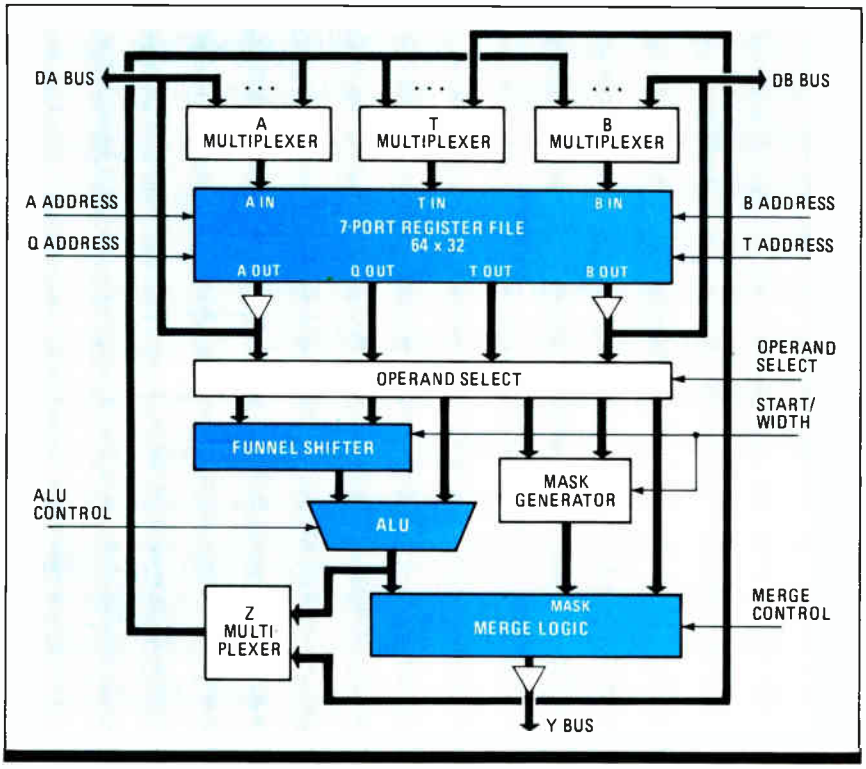
In many advanced applications, the gating factor—the key element or node in a design that determines overall system throughput—is the ability of the system's register-file static random-access memory to transfer data in and out of memory, says Mick. "No matter how much we improved the ability of the IDT49C404 to manipulate data internally, it would have all come to naught if there were no way to get data in and out without compromising performance."

In systems using the IDT design, this will not be a problem, he adds, because company designers have incorporated an on-board register file (Fig. 3) that is unusual in two respects. First of all, at 2 K, it is two to four times the size of that available on any other bit-slice design. Second, it has a seven-port configuration.

"We considered designs with two, three, and four independent on-board register files, and single-memory designs with two, three, and four ports," Mick recalls. "After analyzing the tradeoffs, we decided that the seven-port approach was the optimal design for the kinds of applications we are targeting. When we examined typical high-end applications, such as digital signal processing, image processing, and graphics manipulation, we found they were often I/O-bound. In other words, the applications were often limited by the rates at which they could transfer data in and out of memory."

Organized into an array of 64-word-by-32-bit registers, the seven-port SRAM has three dedicated input ports—A-in, B-in, and T-in—and four dedicated output ports—A-out, B-out, T-out, and Q-out. There is a latch at each of the outputs.

Any four RAM locations can be addressed at the address ports by us-



1. SPEED SECRETS. IDT's 32-bit slice achieves its speed with a highly parallel three-bus architecture, a seven-port SRAM, and an on-chip funnel shifter, ALU, and merge-logic combo.

ing the A, B, T, and Q address fields, and data can be read simultaneously from all four ports. Identical data will appear at the four output ports when the same addresses are applied at the three address inputs. When the clock is high, the internal latches are transparent on the output ports; when it is low, data is held at the latches. Each data input path has a multiplexer that allows selection of data from any of the chip's three bidirectional data and address buses.

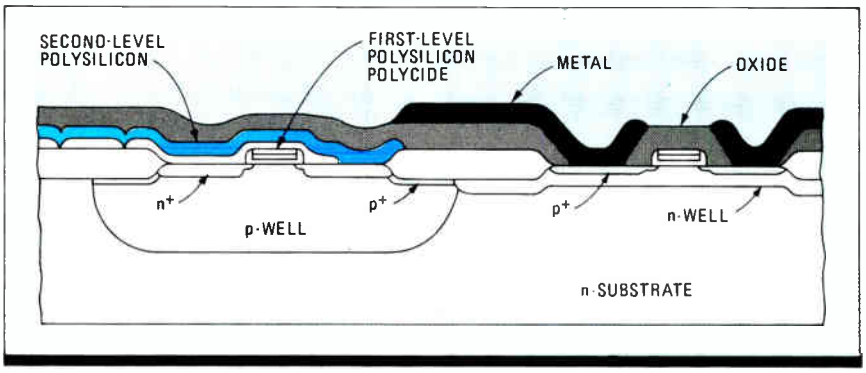
A key element in the IDT49C404 architecture is the 32-bit funnel shifter, which operates on two 32-bit inputs and generates a 32-bit output. It can perform all basic barrel-shift functions such as shift up, shift down, rotate up, or rotate down any number of positions. This high-speed shifting is very useful in operations such as the normalization of mantissas for floating-point arithmetic and in applications in which the packing and unpacking of data are frequent operations. In addition, the funnel shifter can be used to extract a 32-bit output from a sliding window applied to a 64-bit input.

The processor also contains a 32-bit merge-logic-block capability that is under the control of a 32-bit mask generator, as well as a priority encoder for use in floating-point operations and various types of polled interrupt systems.

The ALU can operate in eight functional modes: three arithmetic, four logic, and one special-instruction mode. The three arithmetic functions are to add registers R and S, subtract S from R, and subtract R from S. The four logic functions include OR, AND, exclusive-OR, and exclusive-NOR. In the eighth mode, the programmer can make use of a variety of special high-level instructions, including unsigned and 2's complement, multiply, divide, prioritize, load immediate, load the internal counters, exchange words, test bit field, clear bit field, and sign magnitude to 2's complement conversion.

IDT's contribution to the state of the art in bit-slice design lies in the way the company has combined these three elements—the cascadable funnel shifter, the merge logic, and the ALU—with the seven-port register file to increase system throughput dramatically.

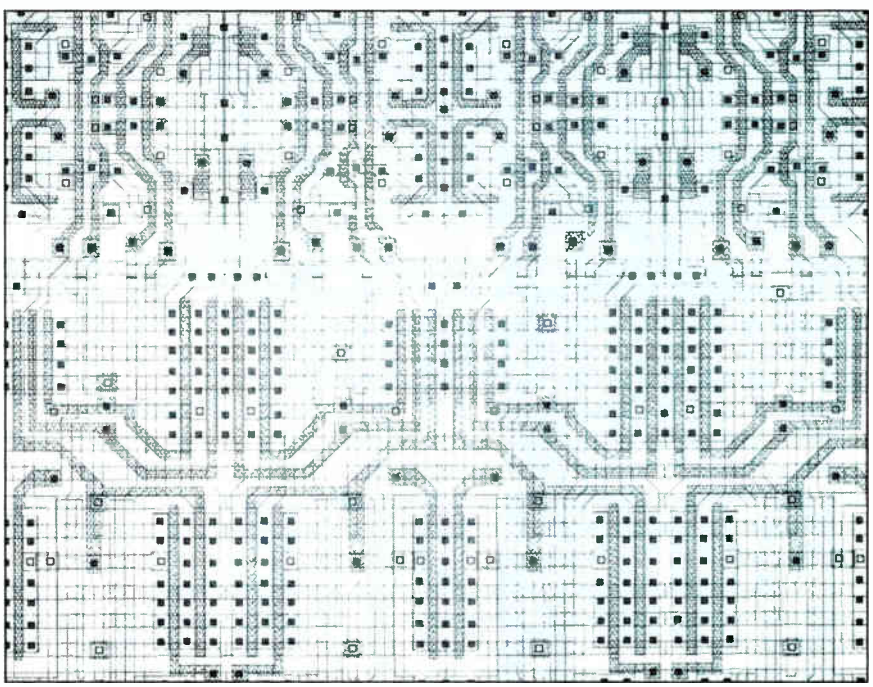
In simplified form, Mick says, the IDT49C404 can be viewed as a seven-port register file feeding into a funnel shifter, then into an ALU, and finally ending in merge logic. "The importance of this particular sequence of operations is that it allows the user to select data from the registers, shift it, operate on it with the ALU, and then merge it in one 80- to 100-ns cycle," he says. "In most other 32-bit slice designs, it requires multiple cycles, anywhere from 4 to 20, to extract a field, operate on it, and return it back to the register file and shift it to an output."



2. SPECIAL PROCESS. The key to the short cycle time of the IDT49C404 is a bipolar-optimized 1.2-μm twin-well CMOS process.

In addition, with this design the user can bypass the funnel shifter, the ALU, or both. He then avoids the performance penalty that would be incurred when the algorithm being implemented requires only one of the two, or neither of them, in combination with the merge function. "With the IDT49C404, the cycle time can be tailored to match the specific processing requirements of the system being implemented," Mick says.

To perform comparable operations using competing 32-bit slices requires at least two to four external components, which further degrade system throughput, says Miller. In addition, he



3. INSIDE THE REGISTER. In IDT's 32-bit slice, the seven-port register contains proprietary SRAM cells organized into a 32-by-64-bit array—much larger than other bit-slice designs.

says, it is much harder to configure these processors to the specific requirements of a system.

For example, although Advanced Micro Devices Inc.'s 32-bit 29332 has an on-board funnel shifter similar to the IDT design, it can be used only in conjunction with the merge logic. According to Mick, the 29332's ALU cannot be used in series with the funnel shifter, making it impossible to shift and merge in one cycle and do arithmetic operations during alternate cycles.

The IDT49C404 also stacks up well against Texas Instruments Inc.'s 74AS8832 central processing unit, says Miller. While the TI part also has an on-chip register file, it has only three ports and is one fourth the size of the CPU on the IDT chip. Moreover, it does not include an internal funnel shifter.

The final ingredient that enables the IDT49C404 to operate at such high system speeds is the use of three bidirectional data buses to enhance the concurrent operation of the seven-port register file and the ALU. In this design, the register file's A and B outputs go onto the DA and DB buses, which go directly on and off the chip. "The advantage of this configuration over competing designs is that data can be read out of the register file on either DA and DB, or both; or data can be brought in independently on either bus," says Miller.

The third bidirectional data bus is the Y bus, which links the output of the merge-logic block to the input of the register file, via the T input port and the Z multiplexer. When the output of the ALU is selected, the results of the ALU operations can be stored back into the register file while data is brought out through the merge path onto the Y bus, allowing ALU operations to be performed in parallel with the extraction of data out of the register file. Alternatively, the Y bus can be linked directly to the T multiplexer, enabling data to be written from the ALU back into the register file while data is being sent over the Y bus to the register file.

With the processor, IDT is looking to stake out a position in such high-end applications as robotics, superminis, image processing, telecommunications, digital signal processing, and CAD/CAM graphics controllers and accelerators. The IDT49C404 is scheduled to come to market in the first quarter of 1987 in sample quantities. □

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THEY'RE BETTING ON CMOS FOR ADVANCED BIT-SLICE COMPONENTS

The development of high-performance, high-density processes—such as Integrated Device Technology Inc.'s Cemos-IIC—is making complex parallel designs feasible, says John Mick, director of product definition and applications engineering at the Santa Clara, Calif., company. "Bit-slice designers have been thinking about advanced architectures for a long time. But as long as bit-slice components were built with bipolar technology, most of these ideas were just wishful thinking, because of the density, packaging, and power limitations of bipolar technology."

Except for the extreme leading edge, where raw speed is imperative, CMOS is the wave of the future in bit-slice design, Mick says. And even there, he believes, the combination of submicron CMOS and advanced parallel architectures will give bipolar implementations a run for their money.

Although it's a latecomer as a manufacturer of bit-slice microprocessors, IDT has wasted no time catching up. Within the past year the company has introduced almost 50 CMOS-based bipolar 4- and 16-bit slice components, including the IDT39C300 family of low-power drop-in replacements for AMD's 2900 family, and the more recent IDT49C400 series, which are high-integration versions of the 2900s. Capping the effort is the high-throughput, 32-bit slice processor, the IDT49C404.

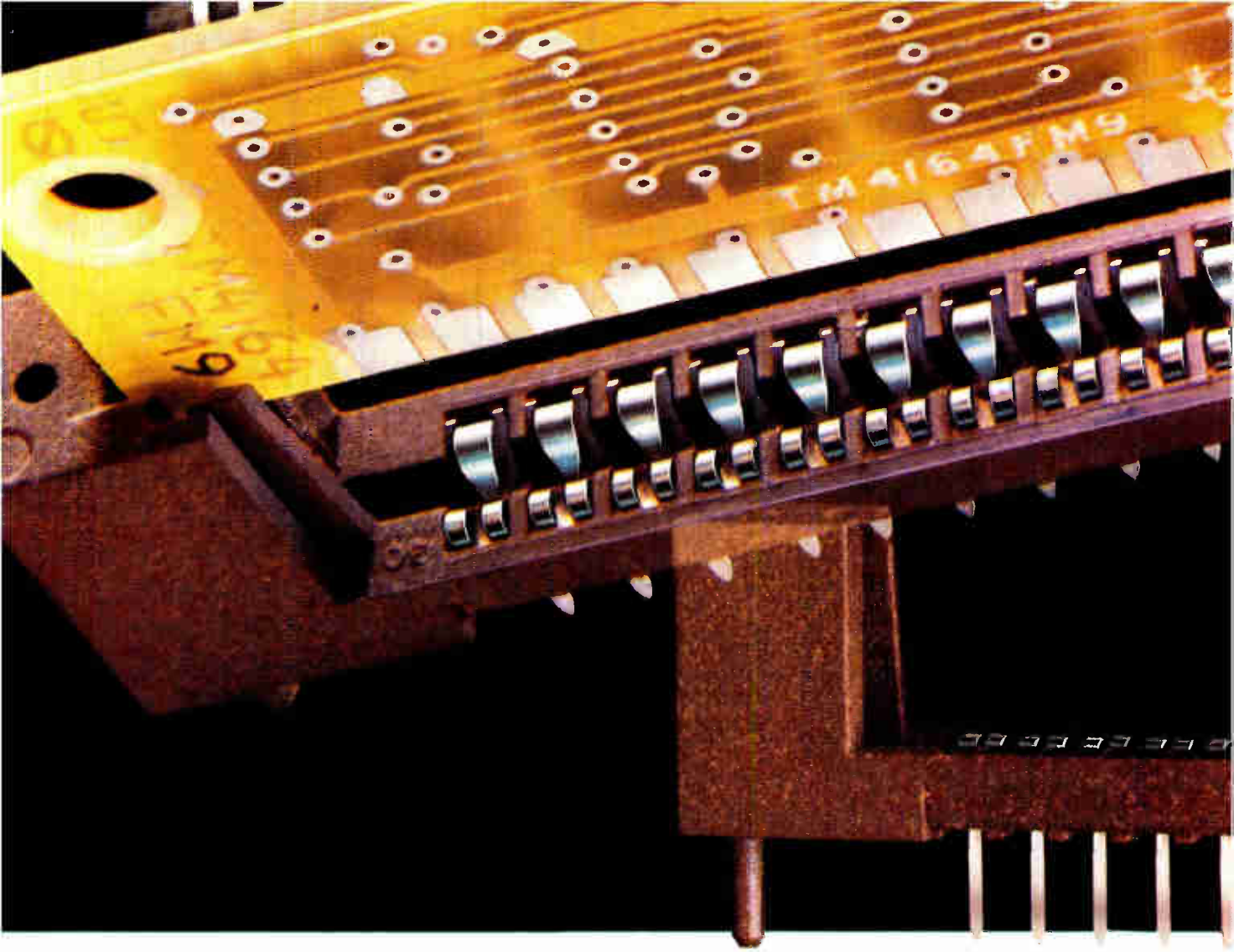
A key element in IDT's quick sprint to market prominence has been the accumulated experience of the bit-slice design team, headed by Mick and by Michael Miller, manager of product definition and applications engineering.

SLICE TEAM. The IDT49C404 design team includes (standing, l. to r.) Au, Tsui, Wang, Le Ngoc, and (seated, l. to r.) Miller, Hickox, and Mick.

Mick, 45, previously worked at Advanced Micro Devices. In 1973, he came up with the concept of AMD's original 4-bit 2901 and proceeded to direct the development of all devices in the family. In addition, as director of bipolar product planning, he was responsible for the development of 150 AMD circuits, including 4-, 16-, and 32-bit slice components, as well as bipolar memory, interface logic, gate arrays, and programmable logic arrays. He is coauthor of *Bit-Slice Microprocessor Design* (McGraw-Hill, New York).

Miller worked with Mick at AMD and was a contributing author to the book. At AMD, Miller was responsible for product planning, applications, and logic design for the 2901C, 2903A, 2910A, and 29818.

Other key members of the design team include Ying Long Tsui, design engineering manager; senior design engineer Fu Lam Au; design engineer Shyun Wang; applications manager Danh Le Ngoc; and Keith Hickox, who developed the software tools.



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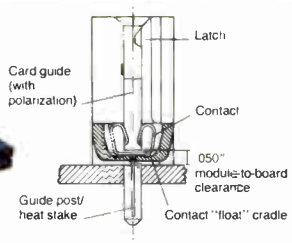

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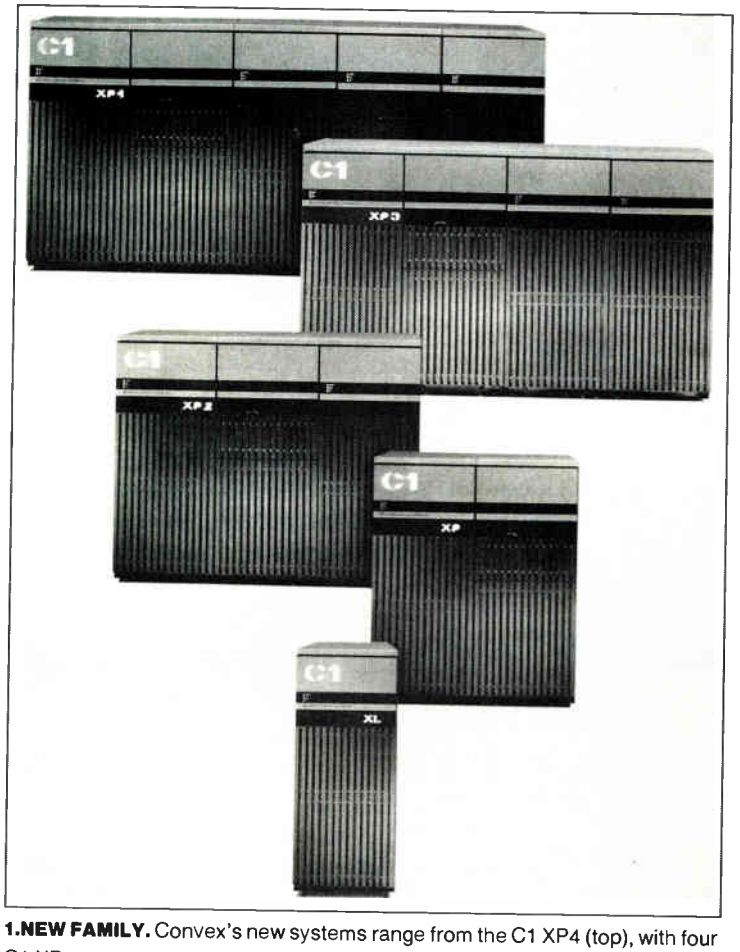
THIS MINISUPER IS AIMED AT PARALLEL PROCESSING

Convex Corp.'s C1 family features upgraded processors and memory with a high-speed fiber-optic interconnection for under $1 million



1.NEW FAMILY. Convex's new systems range from the C1 XP4 (top), with four C1 XP processors, to the C1 XL, a lower-priced version of the original C1

Convex Computer Corp., the company that invented the minisupercomputer, is about to introduce a second-generation product line. The Richardson, Texas company revamped the architecture of its current product and developed a new interconnection scheme to come up with a line that's aimed at the multiple computer market and a move into parallel processing. According to Convex, the new computers will also provide better price-performance than its original C1 machine, offering an upgraded memory and greater speed at a lower cost.

The minisupercomputer market has turned into a hot spot in what overall has been a rather temperate computer business. Convex alone has sold more than 80 of its C1 supercomputers in less than two years. Now it is using this machine as the basis for a family of compatible, expandable low-cost supercomputers (Fig. 1).

The new C1 product line includes the C1 XP, a new processor, the C1 XL, a repackaged and repriced version of the old processor, and a fiber-optic-based system for connecting the processors called the Convex Extended Supercomputing Interconnect (CXSI). An architectural extension called CXS allows the interconnection of multiple C1 XP, C1 XL, and original C1 processors in a cooperating supercomputer environment with transparent file sharing.

The C1 XP is implemented with 20,000-gate CMOS arrays to provide up to 1½ times the performance of the original C1 processor. Memory has been upgraded too, by as much as one gigabyte per central processing unit, using 1-Mb chips. The 80-Mb/s fiber-optic interconnection can link up to 32 C1 supercomputers—in any mixture of new C1 XP, C1 XL, or C1 machines—for transparent load management and file sharing. The CXSI link is designed as a foundation for multiple supercomputer configurations.

To take full advantage of the multiple computers in the CSX architecture, Convex has also implemented distributed system-wide batch-management software. The features of CXS are designed to run more multiple-user jobs faster and run any given job in a shorter period of time, as well as to provide incremental upgrades.

The CXS system is very flexible in the number of processors used and in the different ways they can be connected. Although it can be expanded as necessary, the company is offering a family of four preconfigured systems with one to four of the new XP processors providing graduated levels of performance (Table). Customers can add additional CPUs, I/O processors, memory,

and peripherals to any of the preconfigured systems. The base price of the C1 XL is $350,000. A typical preconfigured system XP1 costs $475,000; a typical XP2 costs $775,000.

Convex plans to focus on the commercial needs of scientific-computer users, rather than the research-oriented requirements of computer-science theorists. These plans led it to emphasize practical capabilities in the new computer family: improving throughput of a variety of jobs with multicomputer systems, making individual jobs run faster by offering a basic processor with higher performance, continuing software developments, and reducing the price of C1 systems.

TWO PATHS TO FASTER COMPUTING

The two basic ways to speed computation are to build faster processors or to add more processors. Convex has done both. The C1 XP is a faster processor; the C1 CXS multicomputer system puts more of the processors to work.

To upgrade the C1, Convex went to new Fujitsu gate arrays. The original C1 processor was implemented with many Fujitsu 8,000-gate CMOS arrays. All the scalar floating-point calculations used the vector floating-point arithmetic and logic-unit pipeline to save on hardware.

The new C1 XP processor uses 20,000-gate CMOS arrays to provide the scalar part of the CPU with its own very fast scalar floating-point calculation unit. Therefore, the C1 XP delivers the greatest power boost to scalar-dominant programs—acceptable because the vector part of the machine is already very fast and the offloading of the scalar calculations leaves more time for vector calculations.

Several other speed benefits result from this upgrade. First, the new scalar ALU unit is optimized for scalar floating-point work and therefore does a better job than the vector ALU. And since the scalar floating-point calculation unit is now on board with the scalar registers, the time to exchange data between the scalar and vector units is saved. Because the greater number of gates on the new logic chips mean more pins—220 out of 256 for logic versus 160 out of 179 available on the 8-K arrays—data can be moved on and off the chip faster.

Although getting the data on and off the logic chips is desirable, the data also has to go somewhere—the main memory. The basic architecture of the original C1 already provided a large main memory and a wideband path between it and the processing units. Convex now is increasing the maximum main memory of the C1 XP processor up to 1 gigabyte—eight times the old maximum of 128 megabytes. Using 1-Mb chips and surface mounting, the engineers have developed 128-megabyte memory boards.

Convex customers want to run programs that need physical memory beyond 128 megabytes. "All the installed base can be field-upgraded with these new memory boards," says Steve Wallach, Convex's vice president of technology. This is one of the major advantages of an extendable architecture like the C1 CXS. Large, memory-hungry applications such as structural analysis will reap an immediate performance benefit from the large gigabyte physical memory, he says. And a C1 CXS system can go beyond 1 gigabyte of main memory when multiple processors are interconnected, because each C1 XP can have a gigabyte.

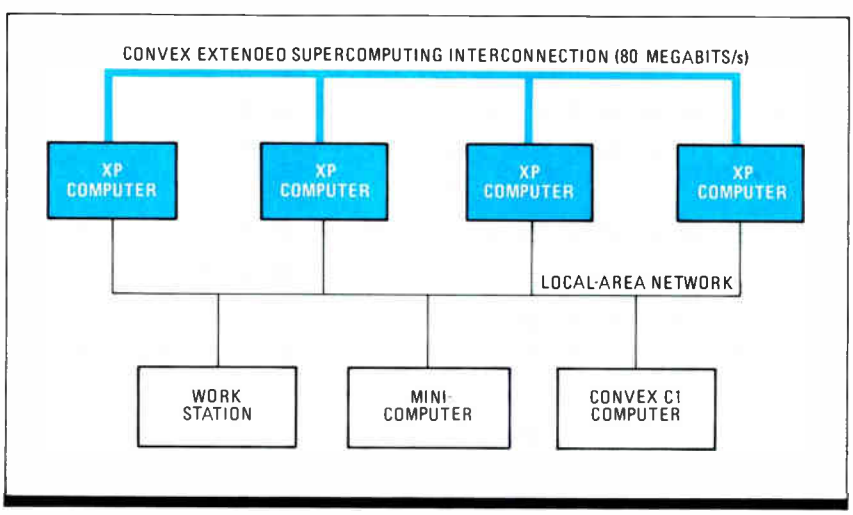
The backbone that interconnects multiple C1 XP processors, CXSI, is an 80-Mb/s token-passing ring implemented with noise-immune fiber-optic cable; a more economical coaxial-cable version is also available. Processors on the ring can be up to 2.5 km apart. Redundant links can be configured.

With the flexibility and speed of CXSI and the fast C1 XP, Convex has created a foundation for building a variety of multicomputing and multiprocessing systems. The C1 CXS systems introduced now are loosely coupled multicomputers with their own large local memory that can be easily used to run a mix of existing applications concurrently. The computers can be tied in a variety of ways, depending on the computational needs of the customer. An example of a C1 CXS system is one with four C1 XP computers linked

CONVEX XP SYSTEM CONFIGURATIONS

Feature	XP1	XP2	XP3	XP4
Number of processing units	1	2	3	4
Maximum memory (gigabytes)	1	2	3	4
I/O speed (Mbytes/s)	80	160	240	320
Floating-point operations (Mflops)	40	80	120	160
Maximum mips	6.4	12.8	19.2	25.6
Number of Ansys jobs per hour	24	48	72	98

SOURCE: CONVEX COMPUTER CORP



2. TEAMWORK. A four-processor C1 XP4, one configuration of C1 CXS multicomputer systems, can also be teamed with Convex's original C1, a minicomputer, and a work station.

through CXSI and tied to an original C1 computer, a minicomputer, and a work station with a local-area network (Fig. 2).

Another interconnection scheme for loosely coupled multicomputers is the cosmic cube or hypercube architecture, in which each computer is directly connected to all other processors in the cube. The C1 XP processors also can be configured as a hypercube using CXSI links.

Convex's next step, although the company won't say when, is to provide tightly coupled parallel processors that share a large memory and can quickly solve one problem. Then multicomputer configurations will be able to have some of these parallel processors as nodes in the CXSI network, mixing both loosely and tightly coupled processors in one system.

The parallel processors and the mixed systems will require some special software for efficient use. Convex is working on parallelization software and already has a set of vectorizing compilers and software development tools for the C1. For the C1 CXS system, the company is introducing a distributed system-wide batch-management software package.

Convex software engineers learned from C1 users that the machines typically run large job mixes. The majority of individual jobs in the mix are large, taking up to an hour to complete. The long jobs typically run in batch mode rather than in an interactive user mode—the user starts a job and goes on to something else. The new batch-management software manages the many jobs in a sophisticated way. The package works closely with the operating system to dispatch jobs transparently among all the processors in the system, based on the estimated job length and computer resources needed.

The batch-management system, combined with other features of the C1 CXS architecture, are designed to run more jobs for more users and run the whole mix faster. In addition, individual users' single jobs will be completed in less time because the individual C1 XP processors run faster than the original C1 processor. Thus the new features announced by Convex for its second generation of supercomputers address two of the most important user aspects of multiprocessor system design—greater throughput and faster job completion. □

CONVEX STICKS WITH A WINNING MINISUPERCOMPUTER TEAM

It does not pay to tamper with a winning team, and Convex Corp. doesn't intend to. Essentially the same team of hardware and software engineers that designed its original C1 computer also worked on the CXS multicomputer system and XP processor designs. CXS and XP join the C1 computer to make up the building blocks of the C1 series, the name given to the Convex architecture.

The development projects that resulted in the current announcements advance Convex into the ranks of multiproduct companies. The C1 computer development team, which in 1984 launched the affordable supercomputer, has extended the technology into a family of compatible and modularly expandable supercomputers.

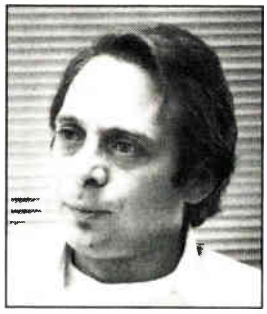
Co-founders Robert J. Paluck, president, and Steven J. Wallach, vice president for technology, originators of the minisupercomputer concept, are still active in directing new-product development. Paluck and his startup team were confident they would bridge a market gap between superminicomputers and supercomputers with their new class of computer. They still were excited, though, when the machine started to sell—proof that the need was real.

But the development team, which also included Frank Marshall, vice president of development; Harold Dozier, manager of very large-scale integration; and John Clark, manager of system engineering, recognized along with Convex's customers that they must move beyond a single-CPU system to meet the growing need for better performance and throughput.

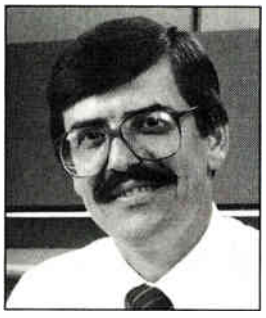
The Convex design team decided that the company's first approach to multiple processors should be the loosely coupled multicomputer architecture that became CXS. According to Wallach, "We heard from many users that the way they would most often use multiple processors would be to run more jobs simultaneously—they were not so interested in applying multiple processors to the same job."

Parallel processing requires that the application be broken down into parts that can be executed simultaneously. But running many jobs on multiple processors—multicomputing—usually does not involve any program changes. "The [multicomputing] solution solves 95% of the user's problems," says Wallach. For example, Convex learned that about 90% to 95% of the work done on the four-processor X-MP/48 supercomputer from Cray Research Inc. uses the machine as four separate computers.

BOB PALUCK



STEVE WALLACH



FRANK MARSHALL

HAROLD DOZIER

Those findings heavily influenced the design team. "A key factor in what Convex is announcing this month is that these developments are a foundation for [future systems] that address two aspects of multiprocessor systems—running multiuser jobs faster and speeding up single jobs—with either a multicomputer or multiprocessor configurations," Wallach says.

CONVEX HAS A MASTER PLAN TO BE KING OF THE HILL

The minisuper maker will use its new computer to separate itself from a growing crowd of competitors and also as a wedge into the parallel-processing field

by J. Robert Lineback

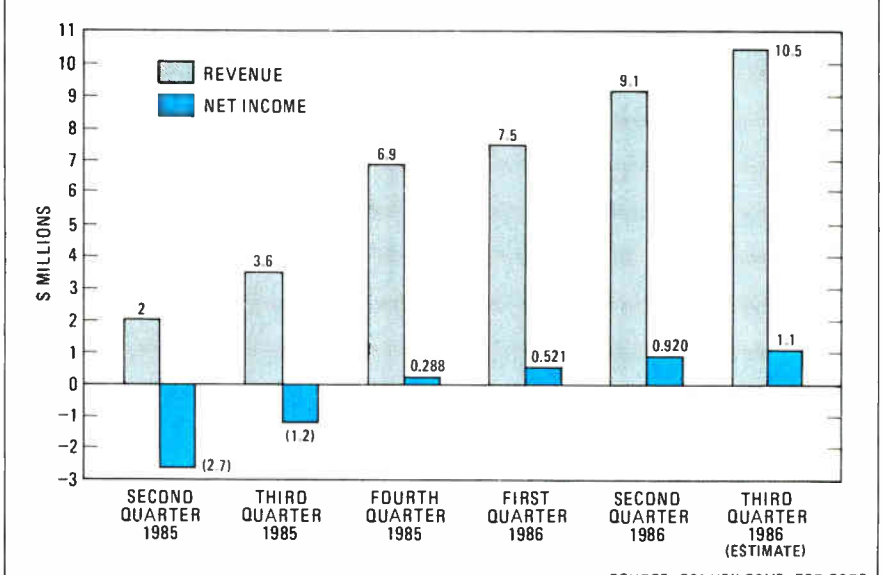
Convex Computer Corp. is so determined to dominate the market for scientific computers costing less than $1 million—the minisupercomputer market—that its engineers are willing to learn Japanese to give themselves an edge. Hardware designers at the Richardson, Texas, company have taught themselves enough kanji to read Japanese new-product specifications before they are translated for the American market. Their enterprise helped make Convex the first company in the U. S. to use new 20,000-gate CMOS logic arrays from Fujitsu Ltd. in its latest and most powerful C1 family.

Another secret of Convex's success is its blend of semiconductor and system talents. "This company probably has more VLSI expertise than most of its largest competitors. That's a remarkable quality. Many of the Convex engineers are ex-designers right out of the chip industry," says Convex chairman L. J. Sevin, a semiconductor executive turned venture capitalist who introduced the two company founders, Robert J. Paluck and Steven J. Wallach, in 1982.

That expertise played a key role in getting Fujitsu interested in Convex's original C1, the first CMOS-based 64-bit computer that integrated vector and scalar processing in a small, air-cooled cabinet, says Sevin, a founder of Mostek Corp. and its chairman before he left in 1981. "I knew the Fujitsu folks from the Mostek days. I just called them up and we went over to see them. Lo and behold, Fujitsu agreed to develop 8,000-gate CMOS array chips for a startup. That was a little surprising, but I think they've concluded startups can be a good market now."

The initiative Convex showed then has led some industry analysts to suggest that the company's development strategy will be a model for other U. S. computer makers. Hal Feeney, director of the technical computer systems industry service at Dataquest Inc., says, "The Japanese companies seem to be very good at exporting the raw

CONVEX'S REVENUE AND INCOME CLIMB



SOURCE: CONVEX COMPUTER CORP

TURNING 'EM OUT. Convex Corp. factory-floor workers assemble C1 computers at the Richardson, Texas, plant.

resources—nuts and bolts of computer technology, if you will—but they have had difficulties bridging the gap to implement systems in the systems market."

Four-year-old Convex's design strategy combines CMOS chip integration from Japan with American know-how in hardware architectures and software technology. The latest results of that strategy, announced this week, pair the powerful C1 XP processor with a new, lower-cost C1 XL model, a repackaged C1 selling for about $100,000 less. They represent aggressive moves by Convex on two fronts: one warding off a growing number of competitors peddling new scientific and parallel-processing systems, the second making the XP the baseline for Convex's eventual entry into parallel processing.

The American-Japanese combination was the approach the company successfully used with the two-year-old C1. The original C1 in turn helped create the scientific computer market, bridging the gap between 32-bit minis and larger 64-bit supercomputers from the likes of Cray Research Inc.

With the new 20,000-gate arrays, Convex designers made the new C1 XP an average of 25% faster than the original C1 system (which executes up to 60 million operations per second). Besides running faster, the C1 XP can contain up to four 64-bit central-processing units, each capable of performing vector and scalar computations simultaneously. Initially, Convex officials expect most multi-CPU C1 XP systems to be used as multiple computers, with each processing unit performing separate tasks. Eventually, though, software and high-speed interconnections are likely to turn the equipment into a full-fledged parallel-processing system. It is Convex's "baseline to move forward," says Wallach, who is vice president of technology and chief systems architect at Convex.

AN ALL-FRONTS STRATEGY

"To be the leader in supercomputers, you must be the leader in supercomputer software. You must also be the leader in tightly coupled parallel approaches; you must be the leader in loosely coupled parallel approaches; you must be the leader in hooking multiple machines together; and you must do it in a way that users can make their applications work on your machine," says Wallach.

"There is a need for [parallel-processing] software, where users have to do a minimal amount of restructuring because compilers do all the work. They want the operating systems to be as transparent as possible, because users don't want to be computer scientists. We know how to do it and are doing it," he says, hinting that some of Convex's customers have been given a peek at prototypes. For the moment, however, Convex bases its marketing of the C1 XP and C1 XL on the virtues of single-CPU computing and the company's compiler, which automatically vectorizes and optimizes code for execution on its 64-bit hardware.

The market Convex pioneered keeps growing. Dataquest estimates it was worth $395 million in 1985, and the market-research firm expects sales to reach $1.8 billion by 1990. Convex intends to be the leader in those sales. "Our goal is to offer the highest-performing supercomputers for under $1 million, and we want to dominate the market," says Paluck, the company president. "You won't see us doing a low-end work station or high-end luxury supercomputers."

So far, the highly focused strategy has paid off. Convex has been profitable since the final three months of 1985 (see chart). It is shipping an average of 20 systems each quarter; more than 80 of the original C1 computers have been installed.

The company also went public this month in a second pass at an initial stock offering. The first offering was postponed last July when the investment market soured on the news of sudden losses and layoffs at rival Floating Point Systems Inc. in Beaverton, Ore. After waiting for the stock market to firm up, Convex made an offering of 3.135 million shares at $7.50 apiece, worth a total of $23.5 million. □

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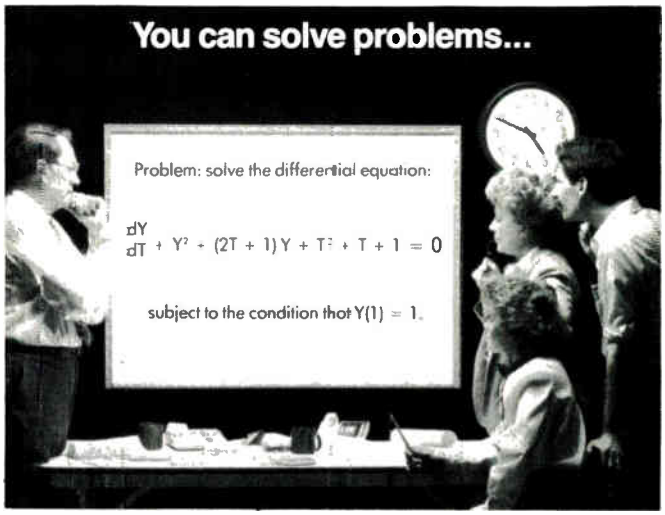

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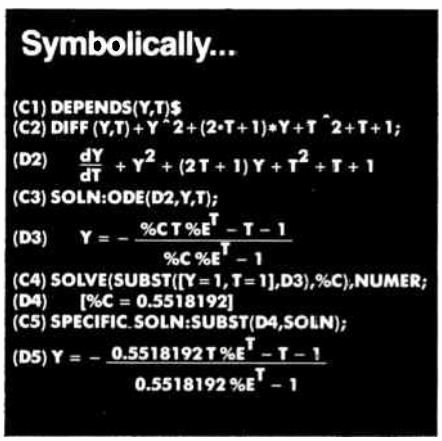

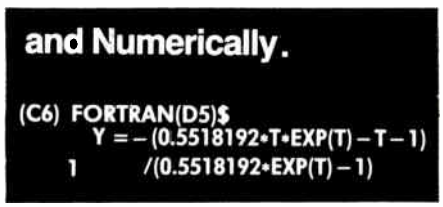

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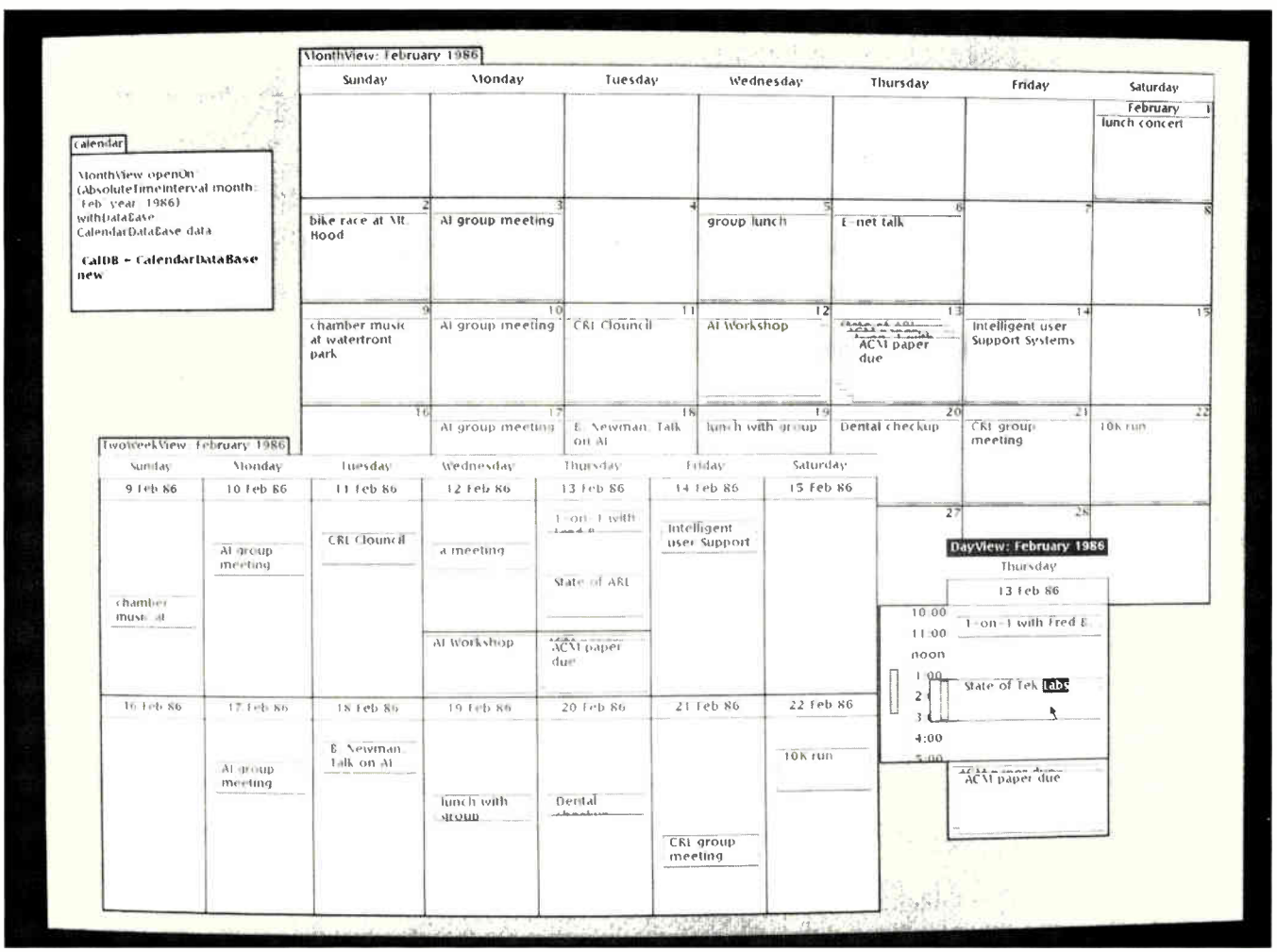
HOW AI WILL ADD BRAINS TO OFFICE AUTOMATION

Artificial-intelligence techniques will manage the flow of information; one goal is automatic updating of a pool of information for the engineers working on a project

by Alexander Wolfe

Artificial intelligence, which cut its teeth on specialized applications such as expert systems, is about to move into the mainstream in a big way. The ambitious goal of developers is nothing less than taking over the job of managing information in the workplace. Breakthroughs are starting to come from a tiny band of researchers who are applying AI techniques to office automation.

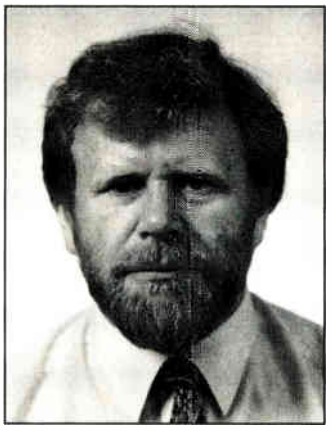
Finding a way to knit together AI and office automation has not been an easy task. But early systems now being developed in the laboratory will create a central pool of knowledge about engineering projects, clue in users on any elec-



1. DAYS OF OUR LIVES. IPSE's intelligent electronic calendar will use AI to coordinate scheduling of people, office space, and equipment.

tronic mail messages that fit their interests, and automatically juggle an entire work group's schedules to resolve any conflicts. Results should begin to emerge from the lab within the next 18 to 24 months, offering vast productivity improvements to end users of the roughly $250 billion of office-automation hardware and software that is expected to be sold over the next five years.

Most ambitious are the separate efforts under way by researchers at Tektronix Laboratories, Beaverton, Ore., and at the Massachusetts Institute of Technology. The two groups have already demonstrated prototypes of new office-automation systems incorporating some AI features. Tektronix Inc. is enhancing its Intelligent Project Support Environment (IPSE). And a version of the MIT Information Lens will soon be up and running at Xerox Corp.'s Palo Alto Research Center, a sponsor of the effort. Office-automation giants Data General Corp. and Wang Laboratories Inc. also say they're pursuing research, but they decline to discuss specifics.



2. PHILLIPS. "A lot of difficulties on projects arise because people fail to mesh correctly."

"The potential to use artificial intelligence in office automation is tremendous," says Jit Saxena, president of Applix Inc., a Westboro, Mass., office-automation software house. AI-enhanced office automation will take the form of integrated software packages running on networks of high-powered desktop work stations or personal computers. That software will typically provide each user with access to individual word processing and spreadsheet applications. On a system level, features will include an electronic calendar or scheduler for keeping track of meetings and appointments, electronic mail for communicating with other system users, and perhaps a document-management and -tracking feature. All these functions will be tied together via a huge data base. AI will help manage that data base, controlling the flow of information.

Controlling the flow for engineers working on large-scale technical projects is the idea behind Tektronix's IPSE system. "A lot of difficulties on projects arise because people fail to mesh correctly," says Brian Phillips, a principal scientist in the Computer Research Laboratory portion of Tektronix Laboratories and head of the IPSE effort. Indeed, problems often arise because programmers and engineers become isolated from key "outsiders" such as management and support personnel. "We need to increase the access to information beyond the project team. This is not a trivial task," says Phillips.

To provide that access, IPSE brings together three main parts: a project encyclopedia, or data base; an intelligent electronic calendar; and an electronic mail system. The IPSE will use AI as a key ingredient in each of those features, as well as for tying together the information they contain. AI will allow the system to act as a filter that makes decisions about efficiently routing information to the system's users.

3. MALONE: His Information Lens acts as a filter in electronic-mail systems to control and manage the flow of information.

FACING UP TO AI

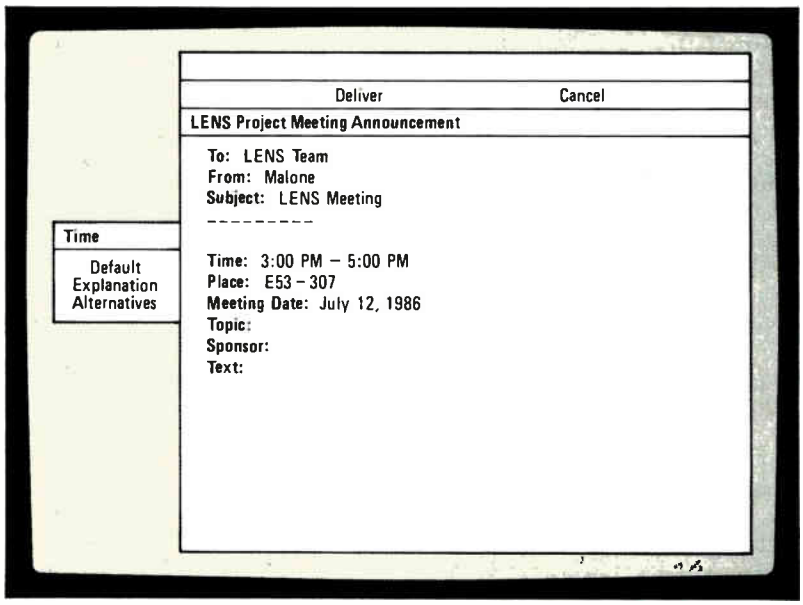
Phillips and colleagues Jeff Staley and Eric Gold are integrating the calendar, encyclopedia, and electronic-mail components. Prototypes of some of the system's AI components also exist; more AI power will be added during the next year. Although the toughest obstacle to fully realizing IPSE's proposed capacities will be development of the natural-language software—programs that can "understand" written text—"we strongly believe we can get some subset of that to work fairly quickly," says Staley.

The completeness of the project encyclopedia is crucial to IPSE's success, says Phillips. As a data base containing the complete history and state of the engineering project that IPSE users are working on, the project encyclopedia is the ultimate source of all information that the system's AI-enhanced software processes.

Internally, the project encyclopedia is modeled as a semantic network, a knowledge-representation form used in AI. In many ways, this model is like a filing system that features extensive cross-referencing. Roughly, "primitives," or nodes containing abstract concepts, are linked to more detailed explanations. At the same time, groups of primitives, as well as groups of detailed explanations, can also be linked together.

In this way, the complete volume of project data can be accessed by dipping into the system through a relatively small number of primitives.

The intelligent electronic calendar (Fig. 1) is much like a desk diary in electronic form. IPSE users can note their appointments and schedules on their calendar; their input automatically becomes part of the project encyclopedia. Using that input, the system will assist in coordinating the use of all time-restricted resources—people, office and lab space, and equipment. A goal is to be able to use the calendar to help automatically schedule an engineer's or programmer's day. "To do this, it [the calendar] has to know something about the idiosyncratic preferences of the user. For example, they [the user] may want to keep Wednesdays free of meetings so they can get some work done," says Phillips (Fig 2). Much more complex constraints would also have to be handled: the calendar provides facilities to access the project encyclopedia, view multiple schedules, summarize a schedule, automatically schedule repetitive meetings (such as weekly staff meetings), and automatically negotiate a meeting time.



4. TELE-GRAPHIC. Templates, or blank forms containing category headings, are the basis of the Information Lens.

The communications system consists of an electronic-mail system combined with an AI component that will analyze the messages. The electronic-mail system will feed its information into the IPSE via the project encyclopedia. Because of its file-linkage model, the project encyclopedia is adept at processing information input from the electronic-mail system.

AI software in the form of a local reasoning system will make decisions on message routing based on knowledge about that message, knowledge about the project, and information gleaned from previous messages. In addition, a user may instruct the system on how to make message-routing decisions by entering rules. For example, a user might enter a rule commanding IPSE to route a copy of all messages to the project's department secretary. A more complex set of rules might detail the steps to take if a member of the IPSE team is out of town. IPSE might sort the absent member's arriving messages by content and resend messages covering different topics to different group members.

At times, the local reasoning software will need information on the status of other IPSE users to make its routing decisions. For that reason, the communications system will also contain a remote reasoning system to automatically send the necessary data to other local reasoning points in IPSE.

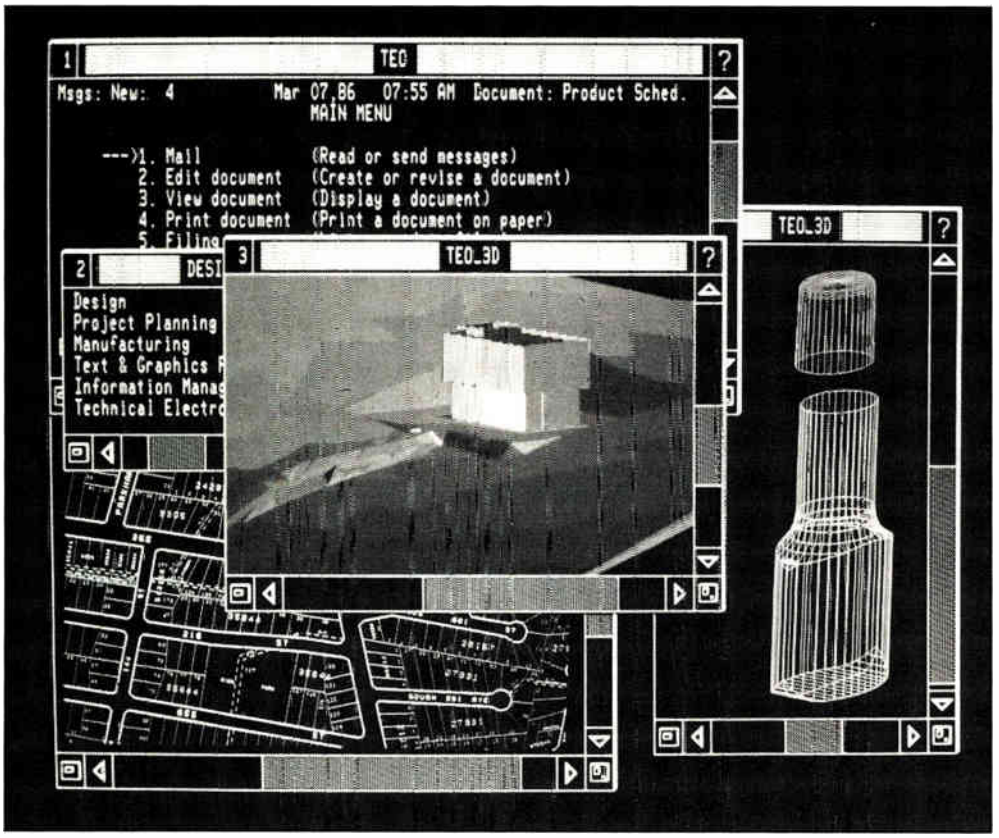
IPSE is being implemented on the Tektronix 4404 AI work station in the AI programming language Smalltalk. To operate IPSE, users select system functions using pop-up menus and a mouse. The menus allow users to call up screens to enter information in the encyclopedia, update the calendar, or send electronic mail. Windowing lets several tasks be processed simultaneously.

Future work on IPSE will also seek to extend the breadth of information stored in the project encyclopedia, so the system will have more project data to share among users. But this will be no easy task. "The burden of entering information must be minimized. We are seeking as many ways as possible to reduce the manual effort involved. We are exploring optical character-recognition techniques. Another idea is to automatically capture information from the communication channels and place it in the encyclopedia," Phillips, Staley and Gold wrote in a recent paper describing the project. "Nevertheless, relevant information will [also] be generated in informal, off-line situations: 'at the coffee machine.' Collecting this information is a future challenge. "

WILL THE SOFTWARE UNDERSTAND?

Ultimately, IPSE's future will ride on the success of its natural-language-understanding software. Writing software that can understand free-form unstructured paragraphs and pages is an immensely complex process. Indeed, the comprehension capacity of current natural-language systems is severely limited. In the commercial arena, natural-language front ends have scored some successes; they convert English-language input into programming-language queries intended for data-base-management systems. The natural-language front ends can do this because they can handle limited, single-sentence messages quite handily. Long multisentence passages, on the other hand, press AI researchers to the limit.

Thomas W. Malone (Fig. 3) took a detour around that natural-language roadblock in developing the Information Lens. It uses templates—



5. A TOOL FOR ENGINEERS. Data General Corp.'s TEO helps engineers work with CAD applications that include AI software, but does not itself use AI-based analysis.

blank forms containing category headings (Fig. 4)—instead of software that understands natural language. "What our system does is allow you to communicate a much wider range of information that may be beyond the power of current natural-language-understanding systems," says Malone, who is an associate professor of information and technology at MIT's Sloan School of Management in Cambridge.

A GIANT FILTER

Billed as "an intelligent system for information sharing in organizations," the Information Lens handles the electronic-mail component of office automation. "One of the ideas behind the system is that, by giving people tools for selecting what is important to them, they gain access to information without being overloaded," says Malone. The system, running on 25 Xerox 1100 work stations scattered throughout the Sloan School, is the most sophisticated electronic-mail network ever implemented, Malone claims.

The Information Lens acts as a giant filter operating on all the electronic-mail messages that travel throughout the network of work stations. It monitors the information content of all of those messages; its 'filtering' function determines the significance of the information to each of the many users logged on to system.

To this end, a detailed representation of each user's interests is programmed into the Information Lens. When message content matches that stored representation, the system picks off the information and routes it to the user. In this manner, the Information Lens can sort and prioritize messages that are already addressed to a user. But more important, it can deliver messages to users who otherwise would not have received them.

Users enter their outgoing-message text into a template. For example, a template announcing a meeting might include fields for 'time,' 'place,' 'organizer,' and 'topic.'

The templates lock the messages into a structure the Information Lens's software can easily decompose into informational components. The template concept is also used to help users program in rules to capture and categorize incoming information. Customized templates could be added to extend the range of the system. By using templates to structure information, Malone avoided one of the toughest AI-development problems. "One of the things that's unusual about our system is that our combination of AI techniques and user-interface techniques avoided the need to do natural-language understanding," he says. The templates make the Information Lens user do work that would otherwise be left to a natural-language system.

Another office-automation giant, Data General Corp., recently released TEO, a state-of-the-art office-automation package for engineers (Fig. 5). While the package allows users to work with AI-based computer-aided-design applications programs, it does not contain any "global" AI information-analysis tools. "We see [AI] as an important area, but nothing that can be integrated into office automation quite yet," says a company spokesman. "You can't hand people technology before it's ready." Nevertheless, Data General is investigating AI and says future systems are likely to contain some of the information-sorting and -sifting tools that appear to be an increasing focus of AI researchers.

A Wang spokesman says that the Lowell, Mass., company is also pursuing office-automation research in the AI areas of natural language, knowledge-based systems, and voice applications. But the company would not discuss specific projects. □

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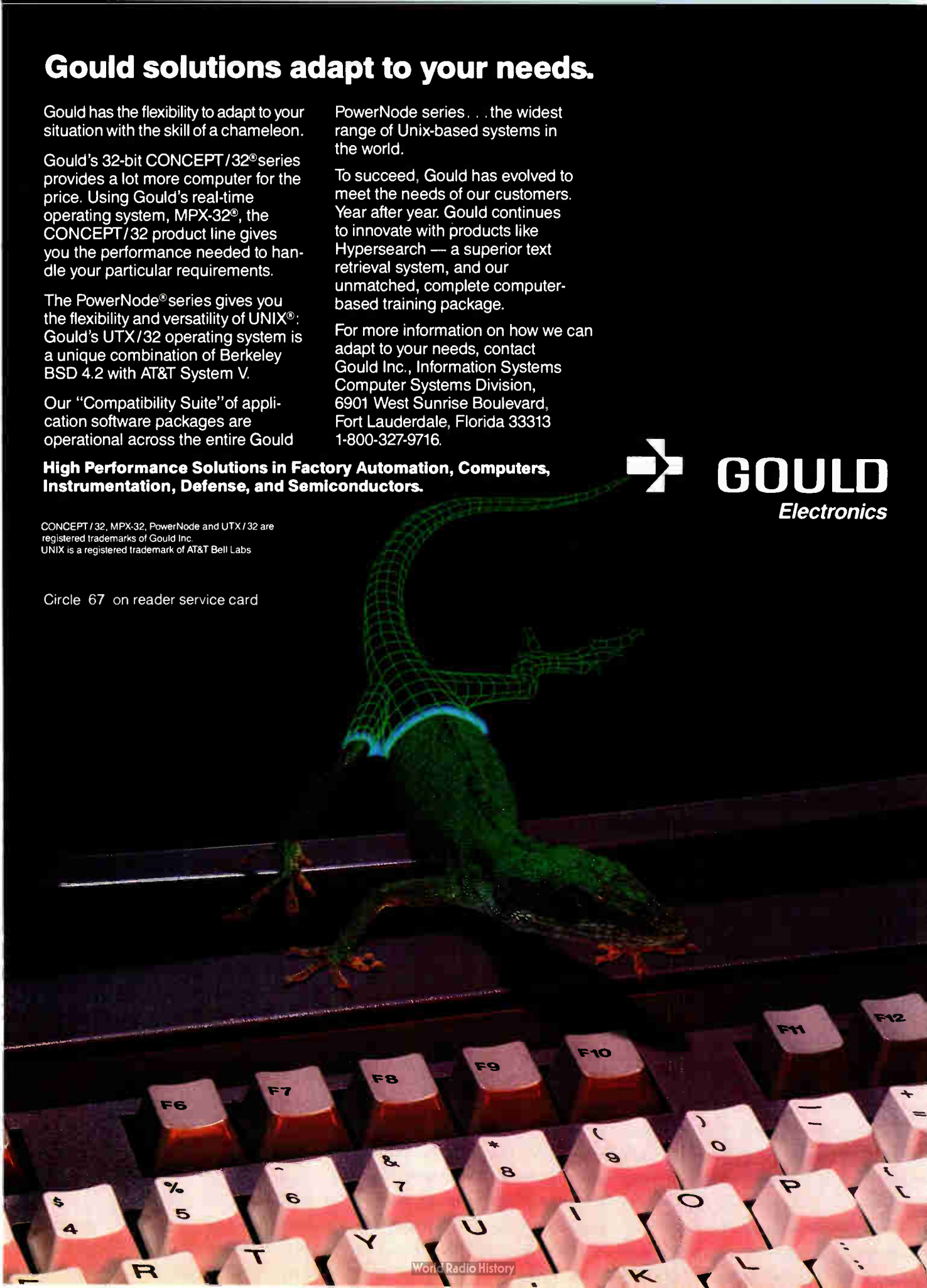

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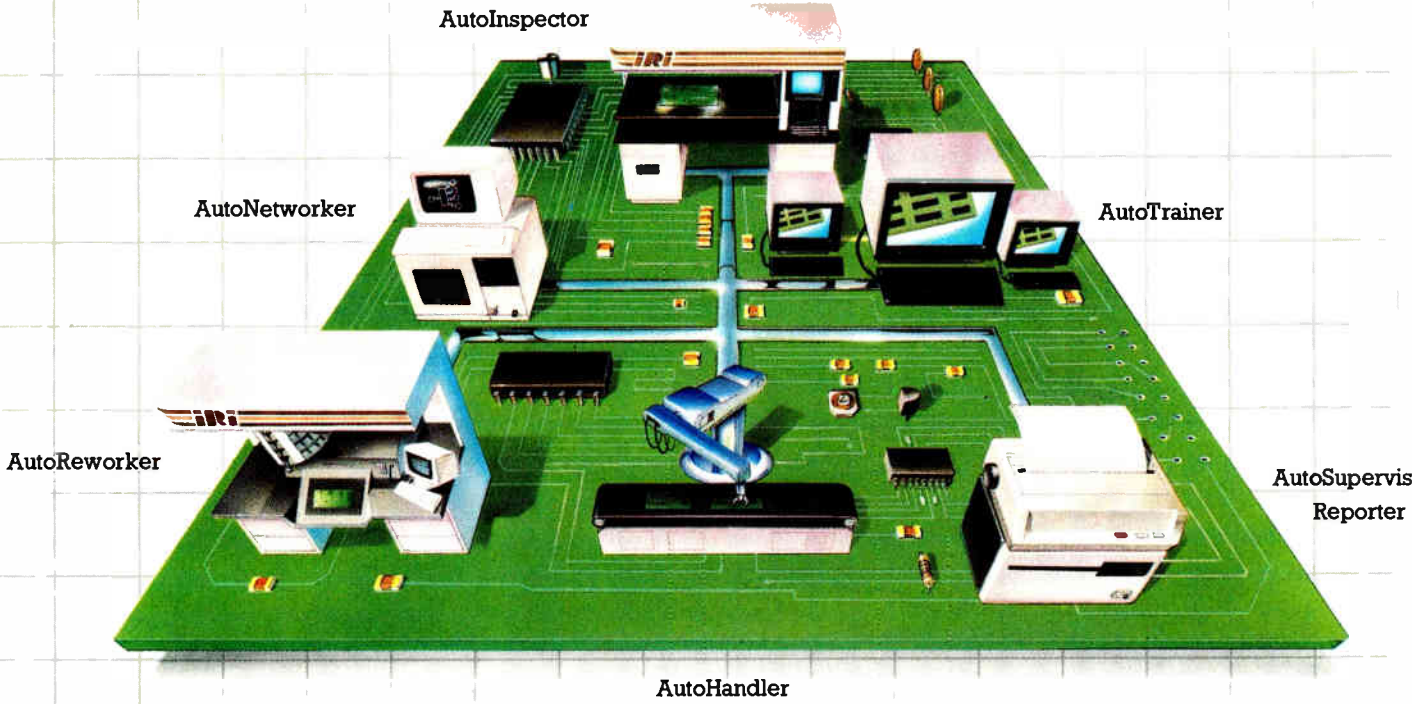

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HOW WEITEK'S CHIPS RUN FORTRAN AT 25 MEGAFLOPS

Three new processor chip sets combine optimizing compilers for high-level languages with a hardware architecture that uses the best features of RISC

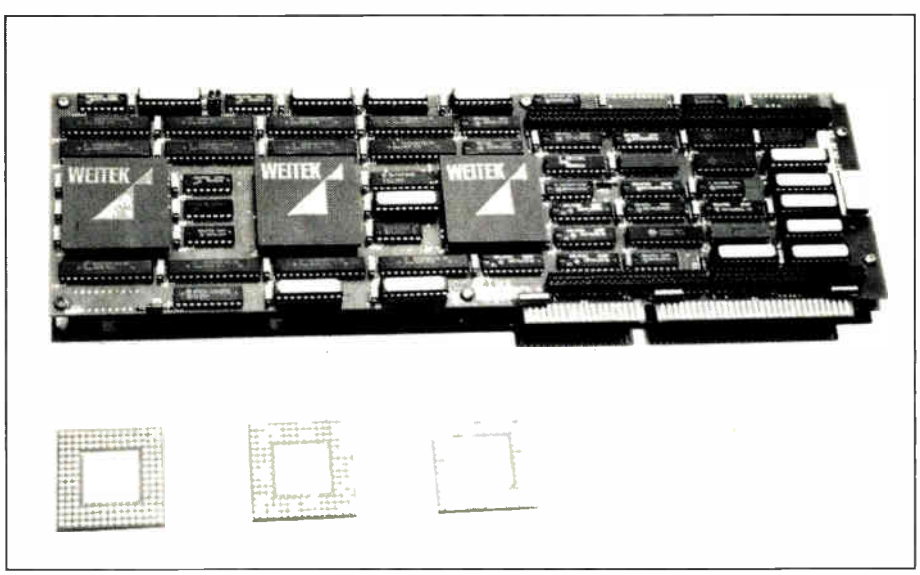
A major advance aimed at easing the task of designing high-performance numerical processing systems comes in the form of three new processor chip sets from Weitek Corp. The Accel processors couple a rich software-development environment with a powerful hardware architecture using some features of reduced-instruction-set computers to yield peak performance of 25 million floating-point operations per second (Fig. 1).

That combination should spell relief—in time and costs—for developers of supercomputers, work stations, two- and three-dimensional graphics systems, digital signal processors, and other power-hungry number-crunching applications. "We offer the ease of software development of microprocessors with the performance that you find in bit-slice building-block products," says Julie Cates, Accel product marketing manager for the Sunnyvale, Calif., company.

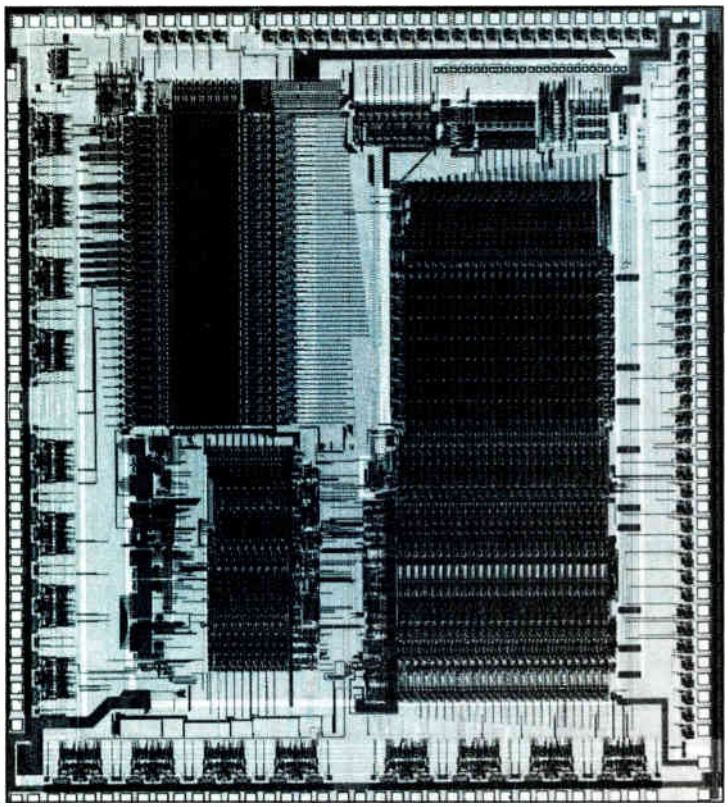
Key to the Accel family's software arsenal is a set of optimizing C, Fortran, and Pascal compilers that allow users to code directly in high-level languages, eliminating the reliance on the cumbersome microcoded approach of bit-slice building blocks. An instruction set utilizing the best of both the RISC and non-RISC worlds allows the compilers to generate the most efficient code possible. A parallelizing instruction scheduler further optimizes that compiled code. And an optional development system attaches to an IBM Corp. Personal Computer AT to allow rapid prototyping and debugging of Accel applications.

Those tools have helped the Accel processors, which are available in sample quantities, get off the dime quickly. The Jet Propulsion Laboratory, Pasadena, Calif., is using Accel processors in a new version of its Hypercube parallel processing computer. Pixar Inc., a high-end graphics systems manufacturer, and Evans & Sutherland Inc., a maker of graphics terminals, are also using Accel chips.

The Accel 8000, 8032, and 8064,



1. ACCEL-ERATOR. The Accel-DS design system helps ease software development for the three-chip Accel 8064 processor, aimed at numeric processing applications.



2. NUMBER-CRUNCHER. The floating-point processor in the Accel 8032 and 8064 offers 25-megaflops peak performance.

all fabricated using 1.5-μm CMOS technology, make up the new line. At the low end of the family, the Accel 8000 32-bit integer processor is ideal for 2-d graphics and simulation applications. Execution speed is 5 million instructions per second sustained and 12.5 mips peak. In graphics applications, such performance equates to line-drawing rates of 5 million pixels/s, polygon shading at 3 million pixels/s, and two-dimensional image transformation and clipping at 2 million vectors/s.

The Accel 8000 processor is composed of two very large-scale integrated circuits, an integer processing unit and a program sequencing unit. The IPU performs all integer-based computation, such as data address generation and integer control operations. The PSU controls program flow, ensuring that instructions execute in the proper sequence. It also manages branching, subroutine jumps, and interrupt response.

The additional power of the next processor in the Accel lineup, the 8032, is aimed at digital signal processing and 3-d graphics applications. While the 8032 maintains the 5-mips processing capacity of the 8000, it adds 10 million floating-point operations/s of 32-bit single-precision calculations. In DSP applications, this allows calculation of a 1,024-point fast Fourier transform in 2.8 ms. With 3-d graphics, the transformation and clipping speed of 500,000 points/s is at the level of real-time computer graphics animation. The 8032 consists of three VLSI chips: an IPU, a PSU, and the single-precision floating-point unit.

At the top of the line is the Accel 8064, featuring 64-bit double-precision floating-point power for high-end Fortran, scientific, and graphics applications. Using a full 64-bit design, including 64-bit instructions and a 64-bit-wide data path, and a 200-megabyte/s memory bandwidth, the 8064 executes 5 mips and 5 megaflops (single or double precision). Running Spice, a standard simulation program, the 8064 can perform up to 48 times faster than a VAX 11/780, Weitek says. Using a standard floating-point benchmark, the 8064 has a single-precision Linpack rating of 2 megaflops. The three-chip 8064 set consists of an IPU, PSU, and a double-precision FPU (Fig. 2). The Accel 8000, 8032, and 8064 will sell for $600, $1,000, and $1,500, respectively, in hundreds.

A CRUCIAL GOAL

In constructing the Accel processors' instruction set, a crucial goal was to make it work well with high-level-language compilers. Designing a compiler that converts programs written in Pascal, Fortran, or C into optimized code targeted at a numeric processor is itself no easy task—but a properly chosen instruction set allows for a more efficient compiler to generate more compact code. To that end, Accel combines the best characteristics of both RISC and non-RISC instruction sets.

As in RISC processors, all instruction-set operations are register-based; the only memory operations are data loads and data stores. As a result of this streamlining, a single three-address, register-to-register operation takes a cycle time of only 80 ns.

Yet the Accel processors execute arithmetic operations, such as integer multiply and divide and floating-point add, multiply, and divide, as single instructions. In traditional RISC processors, such operations are executed as a lengthy stream of instructions. The Accel processors also treat a floating-point multiply-accumulate as a single instruction. As a result, floating-point operations may be initiated every clock cycle, allowing a peak throughput of up to 25 megaflops.

The instruction set further boosts performance by supporting more parallelism than traditional RISC processors. It performs data-address generation—including powerful indexing modes—in parallel with computation. Memory load and store operations also parallel the computational processing.

Instruction-set features also help tighten the loops, which can take up 90% of the execution time in a numerical processing program. Available are loop control, endloop, subtract, and branch instructions. An instruction-neutralization feature helps optimize program paths containing conditional branch instructions. And instructions that can generate an address and load data into a register every clock cycle speedily handle arrays, which are critical to

many numerical processing applications.

Accel's software lineup includes a range of optimizing compilers to generate efficient code, the parallelizing instruction scheduler to further speed execution of that code as it runs on the processor hardware, and a variety of development tools such as assemblers and debuggers.

The C, Fortran 77, and Pascal optimizing compilers were developed by Weitek in conjunction with Green Hills Software Inc., Glendale, Calif. To develop efficient target code, the compilers apply standard optimization techniques, including elimination of common subexpressions and elimination of redundant load and store instructions.

The parallelizing instruction scheduler significantly enhances the performance of the compiled code by examining the instruction stream and rearranging the instruction flow where possible. Integer, floating-point, and address-generation actions can occur simultaneously within the Accel processor: the scheduler attempts to maximize the parallel execution of these functions. It also resequences instructions to make the most efficient use of the inherent latencies, pipelines, and branch delays of the Accel processors. It achieves this by overlapping single-cycle instructions, such as integer ALU or address generation instructions, with multicycle instructions, such as floating-point operations. Using these methods, the scheduler can reduce program cycle times up to 50%.

The difficulties of software development are the biggest barrier to the development of applications heavily dependent upon floating-point operations. Development tools offered for the Accel processors include an assembler, disassembler, linker, and simulator. The assembler uses syntax and directives similar to that of a Unix BSD 4.2 assembler. It generates relocatable object code and supports multiple sections, expression evaluation, and symbol table generation for symbolic debugging. The disassembler converts native-code instructions back to their assembly syntax, a useful aid in testing new assembly-language applications. The linker converts object modules created by the assembler into executable modules that can run on the Accel processors. The simulator provides an architectural simulation of an Accel processor. Its user interface includes a debugger that features register and memory status display, breakpointing, macros, and limited symbolic debugging.

Also, to help prepare programs for the Accel processors, a powerful software development environment is available separately. The environment, the Accel-DS design system, is a set of two boards containing one of the three Accel processors, 4 megabytes of random-access memory, 4 kilobytes of program code, and data cache memory. Plugged into an IBM PC AT, the boards provide a platform on which to develop Accel software. C, Fortran, or Pascal programs can be tested and debugged. The $10,000 Accel-DS will be available in the first quarter of 1987. For users developing software on a VAX machine, Weitek will offer a simulator that models the behavior of the Accel processors. □

DEVELOPING THE ACCEL CHIPS STRETCHED THE PROJECT MANAGERS

With the Accel processor project, Weitek managers Fred Ware and Greg Lee tackled new challenges. Ware, 34, took on his first project-manager role. "This is the first time I've directed an effort of this magnitude," he says. Lee, 38, manager of the Accel software team, faced a different kind of challenge. Until now, Weitek has been largely known for its chips. But with Accel, "Weitek has to establish itself as a credible vendor of software," says Lee.

Ware had been a chip designer since graduating with honors in applied physics from the California Institute of Technology and adding a computer science MS at the University of California at Berkeley. At Hewlett-Packard Co., where he worked starting in 1975 through 1982, Ware designed custom integrated circuits for minicomputers, including, in 1979, a floating-point chip set for Hewlett-Packard's HP1000 mincomputer.

After joining Weitek in 1982 as R&D manager, Ware immediately racked up designs as chief architect of the 1032 series of floating-point chips. In 1984, he added design of the 1064 series of floating-point chips to his resume.

But when Ware put on his management cap for Accel, he found there were some adjustments to make. "It's not always real easy to do—you have to figure out what each person's strengths and weaknesses are," he says. Nevertheless, "so far though I find it a fairly rewarding thing."

FRED WARE

GREG LEE

Lee shifted to programming after years as an academic. After he graduated from Reed College in 1970, he went on to earn a PhD in mathematics at the Massachusetts Institute of Technology. He taught for three years at New York's Fordham University and then spent a year as a Congressional Science Fellow.

But in 1979, Lee made his move and joined Oregon-based Floating Point Systems, a maker of array processors. In 1981, he moved to Applicon, a graphics house. After joining Weitek in 1984, Lee participated in microcode development on custom graphics projects. And although he managed a team of six on the Accel project, he hasn't abandoned design entirely. "Let's say I'm a technical manager in the sense that I'm very much involved every day with technical details," he says.

LOGIC TIMING ANALYZER HAS 100-ps RESOLUTION

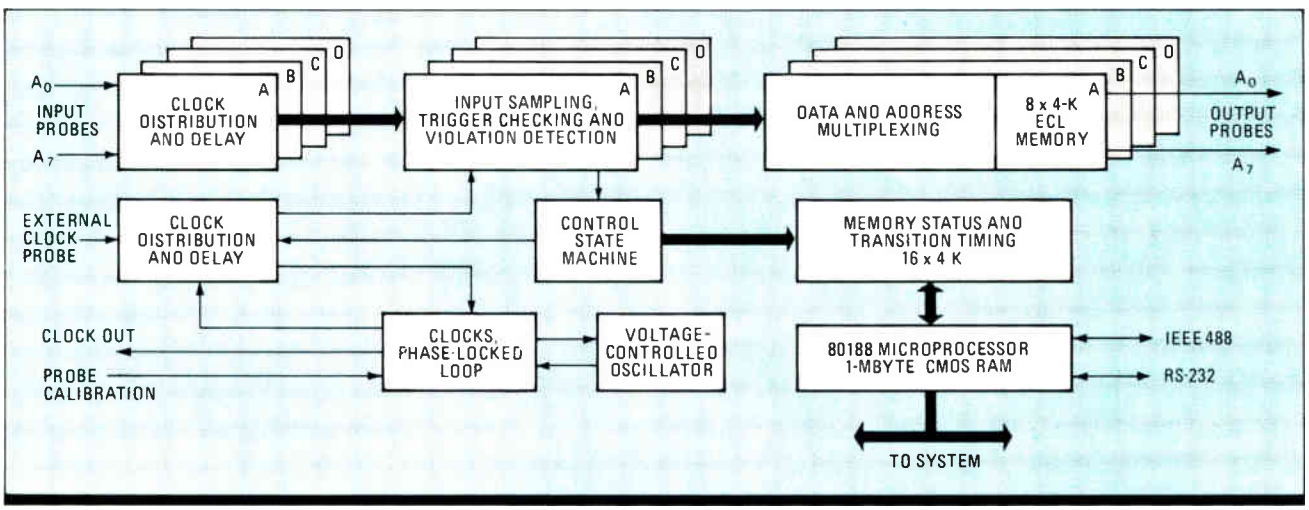
With new equivalent time recording and synchronous harmonic sampling modes, Outlook's instrument speeds debugging of systems with clocks to 200 MHz

Coming early next year from the team that sired the first generation of logic timing analyzers is a new instrument that will kick off the second generation. Outlook Technology Inc.'s T-100 analyzer will combine the system-debugging capabilities of timing analyzers with the precision of sampling oscilloscopes—and will introduce several brand-new operating modes.

Basic operating modes haven't changed much since Outlook's president, B. J. Moore, and its chief scientist, Curtis Blanding, designed the first timing analyzers at Biomation Inc. Moreover, only a few modes can be synchronized to system clocks. The new analyzer corrects these shortcomings, the Campbell, Calif., startup company says, so it will save much of the time designers must now spend debugging system hardware built with very high-speed integrated circuits and other advanced silicon and gallium-arsenide ICs. The T-100's new architecture also contributes to the higher resolution.

At its maximum sampling rate of 2 GHz, the Outlook T-100 will be as fast as any logic timing analyzer made today. And with prices starting at $27,500, it will be at least as expensive. However, the T-100 offers the resolution of a 10-GHz instrument—100 ps instead of 500 ps. This alone will be a boon to system designers, notes James Sheldon, marketing and sales vice president. With system clock rates rising into the 200-MHz range, the small timing variations that could cause mysterious intermittent failures in the field are hard to find, he explains. "Logic analyzer users have been plagued by the need to know what to look for before they can find it."

To boost resolution, Outlook partitioned all the



1. PLUG-IN ARRAYS. All clock and input subsystems of the T-100 analyzer are ECL gate arrays plugged into a single circuit board.

high-speed logic circuits into the five emitter-coupled-logic gate arrays, three of which are replicated to build up a 32-channel analyzer (Fig. 1). The arrays' major functions are clock distribution and delay; input sampling, trigger checking, and timing-violation detection; data and address multiplexing; clocks and phased-locked loop; and a control state machine. As usual, input channels are multiplexed into small, high-speed memories so that recording-memory depth ranges from 4-K bytes with 32 channels to 32-K bytes with 4 channels. When this ECL memory is filled, the recording is transferred to a 1-megabyte CMOS memory.

Sheldon expects deliveries to begin in January or February, depending on when Outlook receives the set of five ECL gate arrays. The T-100 was designed around 2,000- and 2,500-gate ECL arrays now in the production queue at Fairchild Semiconductor Corp.

THE NEW MODES

To perform the classic analyzer debugging functions, the T-100 will operate synchronously with the system under test at rates to 2 GHz—10 times as high as other timing analyzers' synchronous operation—as well as asynchronously at sampling rates ranging from 250 MHz with 32 channels to 2 GHz with 4 channels. Then, to zoom in on problem areas, it will operate in a new equivalent time recording mode that's similar to equivalent time sampling with a digital oscilloscope. In this mode, the analyzer will record repetitive inputs as though it were a bank of synchronized sampling scopes.

Recordings of samples will be offset by 100 ps, stored in a 1-megabyte random-access memory and used to build a composite recording with 100-ps resolution. The technique will help designers to focus more rapidly on marginal components, mismatches in propagation delays, and other design errors. For instance, Sheldon explains, synchronous equivalent time recordings will help designers see exactly how far logic transitions move back and forth with respect to system clock edges during variations in operating environments and supply voltages.

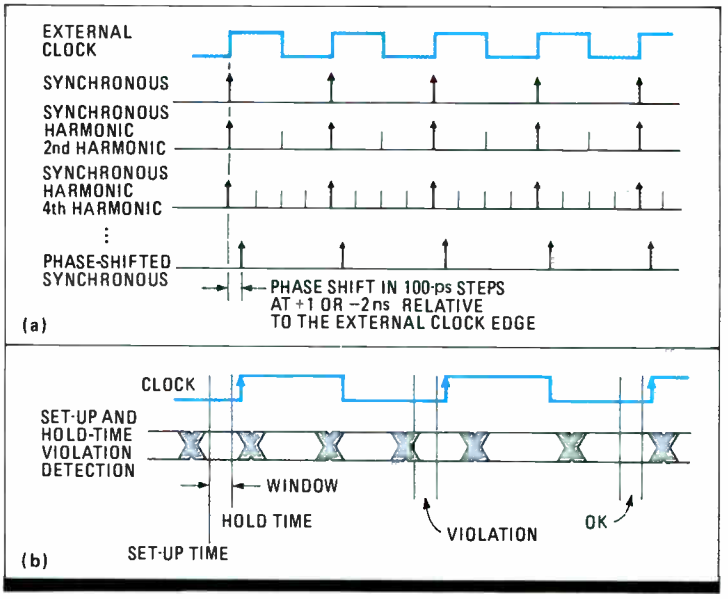
Without equivalent time recording, designers would still need to make primary measurements with other instruments to find out whether the analyzer was triggered at one end of the sampling interval or another, or in between. In contrast, equivalent time recording will provide 100-ps resolution on as many as 16 channels at a rate of 250 MHz. With every other input probe attached to the system under test, the analyzer will split each sample point into a reference channel and an offset channel. The first recording is made with the offset channel at 0. Then, the second sample is recorded with a 100-ps offset, the third with a 200-ps offset, and so forth. The system tested must put out repetitive signals, but that's no problem in a lab.

Another new mode, synchronous harmonic sampling, samples at harmonics of the system clock frequencies. Outlook invented it for such applications as debugging systems with multiphase clocks and for determining whether signals from parallel processors are aligned. The T-100 will sample inputs within the system clock period at intervals as short as the 16th harmonic of the clock rate (Fig. 2). For a still closer look, it will use a new synchronous phase-shifted mode to step through input samples at 100-ps increments.

In synchronous harmonic sampling, the T-100 will generate a higher-frequency harmonic—up to the 16th—of the system under test's clock and phase-lock it to the clock. For example, if the system clock rate is 50 MHz and the eighth harmonic is programmed, the analyzer will operate on 16 channels at 400 MHz and sample data twice during each quadrant of the clock of the device under test. Synchronous phase shifting samples inputs at 100-ps increments over a range of ±4 ns relative to the clock edge. Here, the analyzer operates at 250 MHz on 32 channels.

Since violations of the specifications for setup and hold times are a common cause of intermittent data errors, the T-100 can be preset to monitor every input in every configuration all the time and to trigger whenever a sample violates a set-up and hold time. For example, a designer can start with a wide window, then narrow it in 100-ps increments until inputs trigger the T-100 now and then—a warning that the system will fail intermittently in the field. Then he can decide how to adjust system margins by widening the window bit by bit while varying supply voltage and operating enviroment to determine what margins will prevent intermittents.

To ice the cake, sample rates will come from an on-board frequency synthesizer. Users will be able to crank through thousands of programmable sample rates in the various modes to opti-



2. SYNCHRONIZED. New modes key sampling to a system clock, expediting detection of high-speed faults and intermittent problems.

3. PARTNERS. The T100 analyzer can work with an IBM PC in a timing-analysis mode. Windows give user four views of recorded data.

mize analyzer setups. Rates from less than 100 Hz to 1 GHz can be programmed in 1% increments. With the conventional crystal-controlled 1, 2, 5 sequence, the choices were 10, 20, and 50 MHz, followed by 100, 200, and 500 MHz, and 1 and 2 GHz.

In its pattern-generation mode, the T-100 will generate 250-MHz output patterns up to 32 bits wide. It also will operate in mixed input/output modes and separately record glitches and data. These modes locate logic transitions and glitches in real time within apertures as small as 500 ps, which is state of the art.

Computer simulations indicate that the arrays will operate with the performance matches needed to reach 100-ps resolution, according to Curtis Blanding, vice president and chief scientist. But just in case the first model needs a little tuning to reach 100-ps resolution, he says he "mixed a little art with the science" and designed the printed-circuit boards with "trombones"—sets of wiring traces for adjusting propagation delays.

Also nearing completion is the system software, which is written in the C high-level language and has a layered architecture for easier upgrading. The software runs on an IBM Corp. Personal Computer XT or compatible machine with a high-resolution color display. Acting as a host, the PC/XT provides menu-driven setup displays, trace displays, and other interfaces. It can also collect large numbers of recordings on disk drives for additional reviews or analyses.

Programs that run the analyzer in real time are downloaded to an 80188 microprocessor in the T-100. The instrument can also be programmed to operate as a black box in host systems. For example, it could be embedded in a mainframe to monitor critical paths and to determine when preventive maintenance is needed. □

CHANGE THE RULES TO GET AHEAD, SAYS OUTLOOK'S CURT BLANDING

"I hope we've changed the rules," says Curtis Blanding, the engineer who started Outlook Technology and headed the team that designed the firm's 100-ps logic analyzer. "One of the rules was 'To get more resolution you have to go faster.' We're not under that constraint anymore. Everybody else still is—but they won't be in the future, because equivalent time recording is a concept, not something you can patent. We'll get 100-ps resolution or better, not because the chips run faster but because the T-100's architecture allowed us to do things that could not be done before."

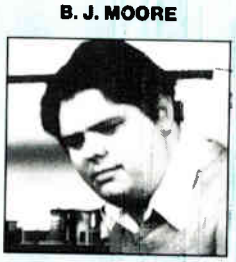
Computer-aided design systems are changing the rules, too, Blanding adds. "That's a dream come true. We can design circuit boards that provide clean edges, design chips that match each other very well and cut down noise and jitter. This has changed the rule from 'How fast can you run?' to 'How precisely can you put your feet down on a line?' " as you run.

What hasn't changed, he says, is the need to make instruments simple to operate. "The hardest job in the world is to make something simple, but it has to be done because computer designers work on complex systems. They don't need complex tools, too."

During his 10 years at Biomation and Gould Inc. (Biomation became part of Gould in 1978), Blanding led the development of some of the industry's most widely used logic analyzers. They were popular, he believes, because each was easier to use than the previous model.

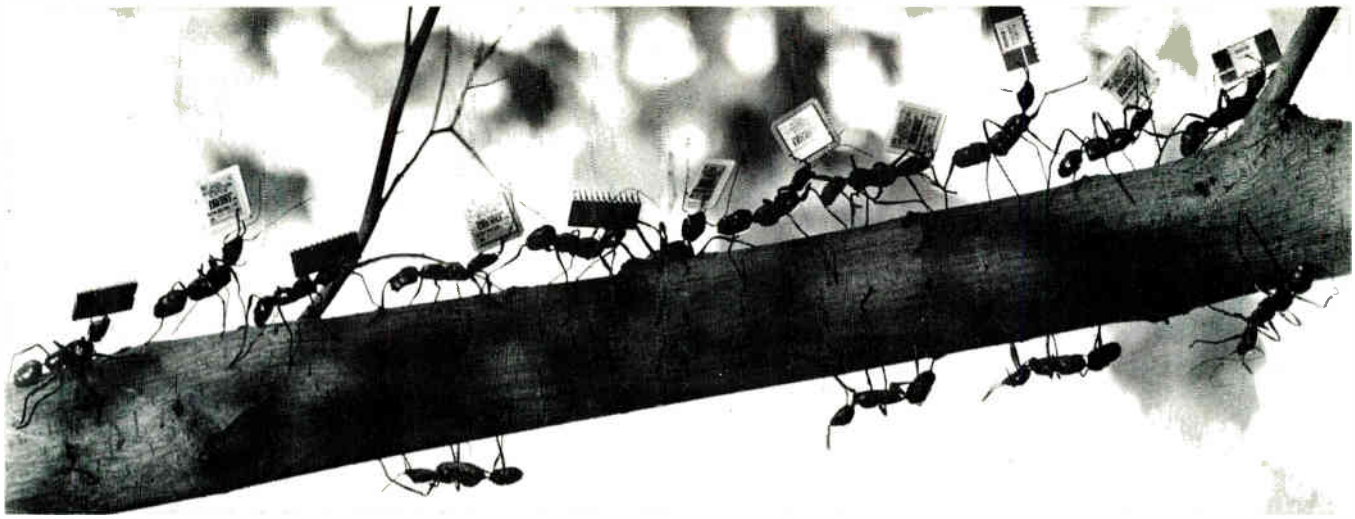
Blanding, now vice president and chief scientist, founded Outlook in March 1984 with two other men from Gould: James Sheldon, vice present of marketing and sales; and William Shoemaker, vice president of engineering. B. J. Moore, who developed the first logic analyzer and headed Biomation, joined as president last year. Mark van Hook was the software architect for the T-100.

B. J. MOORE



MARK VAN HOOK

FOUNDERS. The three founders of Outlook Technology are, from left, James Sheldon, Curtis Blanding, and William Shoemaker.



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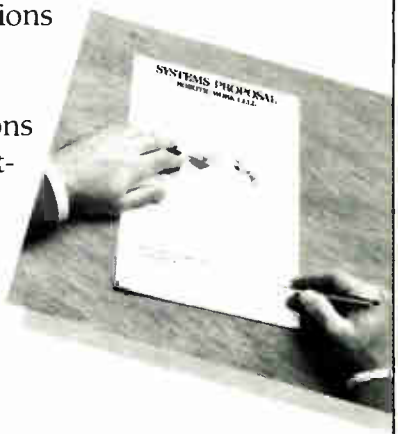

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HOW DESIGNERS CAN SAVE TIME IN LAYING OUT A SEA OF GATES

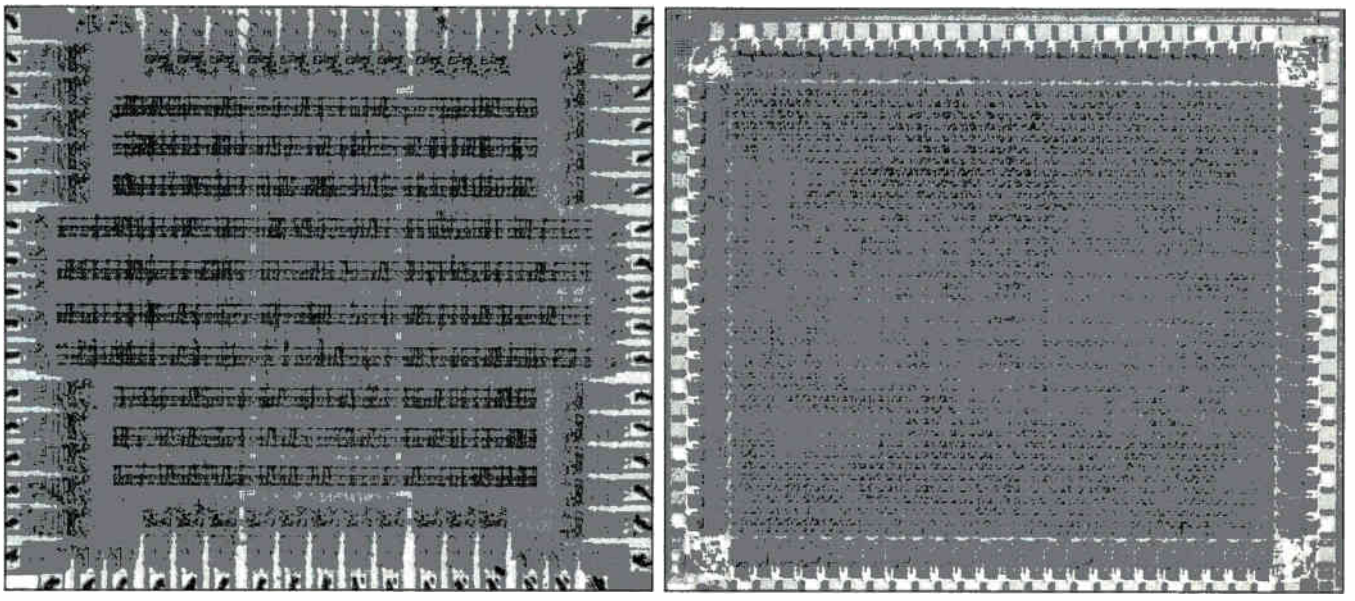
California Devices' software slashes turnaround time by using a work station instead of a mainframe computer to place and route 10,000-gate arrays

Designers can now create large sea-of-gates arrays on an engineering work station, rather than having to farm them out to a foundry for layout on a mainframe, thanks to California Devices' new Wise II place-and-route tool. The San Jose, Calif., company says that although some channeled-architecture tools can do a limited amount of sea-of-gates routing, Wise II is the first based on channelless architecture.

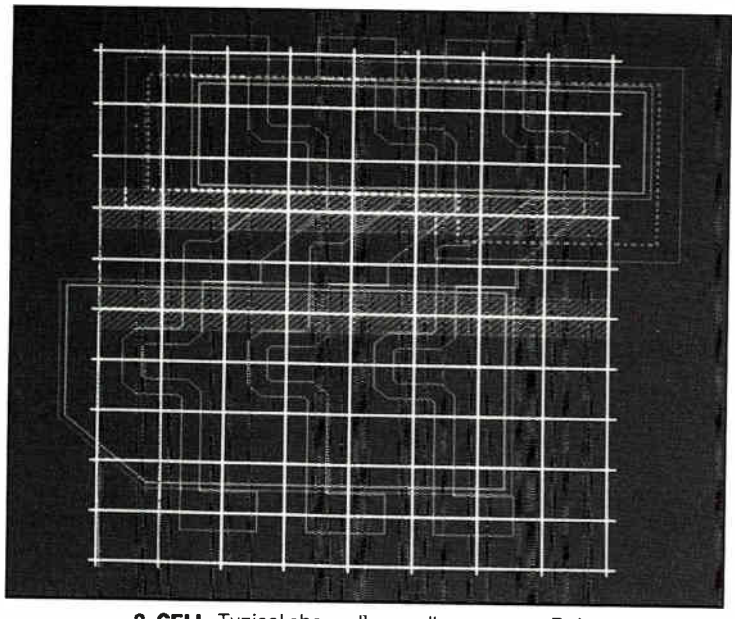
California Devices' place-and-route software [*Electronics*, Oct. 16, 1986, p. 28] is able to handle large arrays of up to 10,000 gates. Until now, automatic place-and-route tools have not been able to lay out arrays larger than about 4,000 gates, because vendors' device architectures and place-and-route tools have been developed to handle channeled arrays, as opposed to the sea-of-gates arrays. These channelless arrays, as California Devices calls them, are becoming popular because they allow much more efficient use of chip real estate (Fig. 1).

With Wise II, a designer can save the week or two of turnaround time spent waiting for a run on the foundry's mainframe, as well as saving the cost of that run. Since there may be several iterations for a given design, the savings in both time and money can be dramatic.

Wise II was developed in conjunction with Daisy Systems Inc., Mountain View, Calif., and runs on Daisy's Megalogician work station. "We provide the work station with a data base, gate array foundations, and the physical macro library," says John Burchfield, CAE work-station



1. EFFICIENCY. Channeled array (left) on 40,000-mil² chip can yield only 1,200 gates; channelless array (right) can reach 2,800.



2. CELL. Typical channelless cell, as seen on Daisy workstation, contains three p-channel and three n-channel transistors.

tools manager at California Devices. Daisy provided the place-and-route algorithms, which were modified for the channelless architecture.

California Devices' library contains symbols of functions, such as flip-flops and gates, and specifies how to implement them in silicon. It specifies the input and outputs of a flip-flop, for example; on silicon, the library's gate array foundation consists of six-transistor cells.

CHANNELED VS CHANNELLESS

When software vendors began automating the place-and-route function for gate arrays, they borrowed the channel-routing algorithm already implemented on layout tools for printed-circuit boards. In the usual pc-board routing process, chips are laid out in a row, and routing channels are reserved on either side of the row. In similar fashion, channeled gate-array routers set aside channels between rows of cells and use them to interconnect gates in different rows or in the same row.

"Suppliers of this type of tool approach the problem of getting more functions on a given array by shrinking the process," says Martin Harding, director of strategic development at California Devices. But at a certain point it is no longer cost-effective to shrink the process to get more gates on a chip.

So vendors will have to rely on compaction to get the 50,000- to 100,000-gate densities needed in the next generation of arrays. But channeled architecture, even with 1-μm process technology, will be unable to achieve this kind of density. And as vendors seek to support gate arrays implemented with a channelless architecture, they will have to build a new set of place-and-route tools, since the routing algorithms for the two array architectures are different.

"The advantage of channelless arrays would not have been realized without dual-layer metal," says Douglas Ritchie, president of California Devices. The advent of dual layers allows metal channels to be laid down over active areas in two directions (along the x and y axes). Channeled gate arrays can use dual-layer metal too, but the advantage of channelless arrays can be best understood by comparing the way the two architectures are routed.

In both a conventional channeled array and a channelless one, the two metal layers form a grid, with layer 1 below layer 2. The lines of the two layers are perpendicular to each other, and the resulting grid can be used to interconnect gates. The lengths of metal required to make these connections can be several thousand microns, crossing over severals cells, or a few hundred microns, connecting nodes within a cell.

Where a layer 1 line crosses a layer 2 line, a connection, or via, can be made between the two layers. Layer 1 routing is parallel to the routing channels (on the x axis), and layer 2 routes perpendicular to the routing channels (the y axis). Sea-of-gates routing uses the same rules, but without the routing channels.

Routing channels are real-estate hogs. "Conventional gate arrays require a larger die size to contain a given number of gates than a channelless array, because silicon area is being devoted to the routing channels," says Burchfield.

The sea-of-gates approach can yield much higher gate densities. But laying out compact channelless gate arrays in dual-layer metal requires a design tool that understands unstructured placement and routing. The Wise II software for performing unstructured placement is based on an algorithm called simulated annealing. The routing is done by a maze router, which finds the tightest three-dimensional "weave" that will interconnect the gates to build the desired function for the chip.

PLACING CELLS IN A SEA-OF-GATES

Simulated annealing is an algorithm developed by IBM Corp. to simulate the way metals cool. As any metal cools, it reaches impasses in molecular compaction in which intermolecular friction causes the metal to heat up briefly, expanding it slightly and allowing the molecules to become realigned so that they may then become more closely compacted. The same mathematical model is used for channelless gate-array placement.

To reduce wire lengths to a minimum, the algorithm measures overall wire lengths between gates in an array. The software performs an initial placement and then calculates the total point-to-point distances of all these connections. Then it performs another placement to minimize the distances and computes the total point-to-point distances of all these connections again. The iterative process continues until the software can reduce the distance no further.

Then, mimicking the temporary expansion model of cooling metal, the algorithm will make a placement that results in greater distances if it can see that subsequent placements will result in further reductions in overall distances. Furthermore, to optimize the performance of a circuit, the designer can direct the placement tool to give greater weight to placing a group of gates with critical timing requirements closer together than other gates. He may choose to assign much less weight to global connections, such as resets and clock lines, where placing these connections close together is not critical.

After placement, the designer invokes the maze router. As with the placement algorithm, the designer can control the approach the router takes in laying out a circuit: starting with the shortest connections, or nets, and moving to the longest nets; or longest nets first, then shortest nets; or some other approach he wishes to set. If the router must choose between making a 100-μm-long connection between two adjacent cells and a 2,000-μm-long connection between two separated cells, it will choose the shorter with the shorter-to-longer-nets approach. Typically, all cells must connect to voltage supplies V_{dd} and V_{ss} via shorter local connections, and therefore these are routed first.

In a typical channelless array, there are three transistor pairs (six transistors) in a cell (Fig. 2). They form one three-input NAND gate. If only a two-input NAND gate is needed, there remains an extra transistor pair. The metal that would have been used to connect the extra transistor pair can now be used for routing. "In a conventional gate array, the router never routes through a cell [in layer 1]; it routes over a cell [in layer 2]," says Burchfield. With a channelless array, the metal that would have been used to connect the unused transistor pair can now be used to route through a cell (in layer 1).

The software comes in two versions. One supports arrays of up to 4,000 gates. The other, for arrays up to 10,000 gates, requires a Daisy MegaGatemaster accelerator for both placement and routing. A disadvantage of a placement algorithm based on simulated annealing is that it requires large amounts of computing power; the accelerator provides sufficient power to make it practical to run Wise II on a work station.

California Devices is not resting on its laurels. The company believes that its competitive edge will erode as other vendors bring their sea-of-gates products to market. So just as the competition gets their first products on the market, California Devices plans to jump ahead again. "We're going to announce early next year a new product that is going to be the biggest gate array in the world," says Harding. How big? "Better than 70,000 gates," he grins. □

WHAT DREW THREE SEASONED PROS TO A STRUGGLING STARTUP

The gate-array technology developed by California Devices Inc. was a powerful attraction for Douglas Ritchie, Martin Harding, and John Burchfield. All three recognized the advantages of its channelless architecture and signed on even though the San Jose, Calif., company was going through some tough times.

In April 1985, California Devices' founders and investors were in search of a chief executive officer who could help get financing and who could exploit the technical advantages they believed the company had. They chose Ritchie, who had previously headed National Semiconductor Corp.'s custom and semicustom chip division, because the rest of his 17 years of experience—six at Burroughs Corp. and nine at Tektronix—had involved semicustom work.

"I came to the company because I was intrigued by the channelless architecture CDI had developed," Ritchie says. "The technology was a couple of years ahead of anyone else in the gate array business when I joined. The only thing missing was the design tools needed to automate the process."

Burchfield, who worked for Ritchie at National Semiconductor, went to California Devices in 1984. He is now manager of CAE work-station tools at California Devices and is responsible for getting the Wise II automatic place-and-route tool developed. Burchfield early on recognized the trend toward work stations and the desire on the part of customers to do the place-and-route themselves. "It gives them faster feedback on what needs to be changed in their design to get it to work in silicon," he says.

Harding joined California Devices in 1984 after developing gate arrays at Fairchild. "I came to the company during the bleak period in its history, but I could see they had a technology that was well ahead of every other gate-array company at the time," he says. Harding is director of strategic marketing.

The three men's assessment has proven correct. Competitors LSI Logic Inc. and VLSI Technology Inc., both of San Jose, now offer their own sea-of-gates products. With new funding and a complete tool set, California Devices seems well positioned to fulfill the potential all three men saw when they joined.

BELIEVERS. Channeless arrays attracted (from left) Burchfield, Ritchie, and Harding.

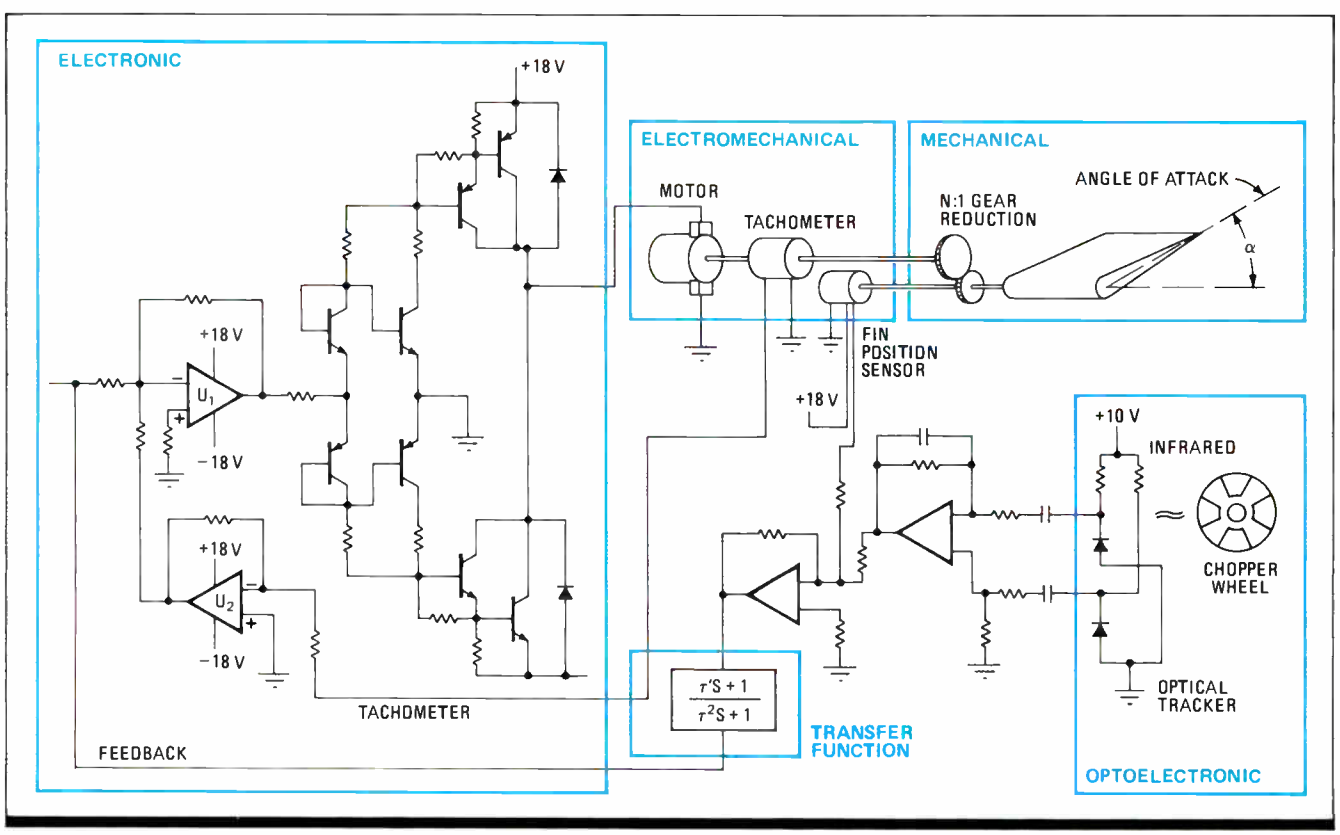
SABER CUTS SPICE OUT OF ANALOG SIMULATION

Based on a library of behavioral models, Analogy's new software tool can simulate any physical system and is faster, more flexible, and much easier to use

A new analog simulation software tool is far faster, more flexible, and much easier to use than Spice, currently the most popular analog simulation program. Called Saber, the package was developed by Analogy Inc., which says it can simulate any physical system that can be described using mathematical equations—electronic, electromechanical, mechanical, or optoelectronic.

Saber resembles the analog-digital circuit simulator recently introduced by Sierra Semiconductor [*Electronics*, Oct. 16, p. 60] for its standard cell library in that both use behavioral models to describe circuit or system action. This approach is fundamentally different from Spice, which mathematically models each individual device in the circuit. While Sierra's software is aimed primarily at ASIC designs with mixed analog and digital circuitry, Analogy's software is suitable also for systems containing a mix of electronic, electromechanical, or optoelectronic devices.

Saber will run on work stations or minicomputers, and it is more than an order of magnitude faster than Spice, which was developed 14 years ago at the University of California at



1. VERSATILE TOOL. Saber can be used to design any physical system that is capable of being described in mathematical terms—including this wing-flap controller, for which a combination of several electronic, optical, and electromechanical functions must be simulated.

Berkeley. Spice has been improved since then [*Electronics*, Aug. 26, 1985, p. 50]. Initially, it ran on a mainframe and permitted no designer interaction during processing; now it operates interactively on work stations—but it is still inflexible, slow, difficult to use, and sometimes incapable of producing a useful simulation.

The major advantage Saber has over Spice is its flexible modeling. Like Spice, it works by creating models based on mathematical equations that represent various characteristics of whatever is being simulated. However, Analogy, a startup in Beaverton, Ore., designed Saber so that it could work with the mathematically based models for a vast array of components, or with models created by the user.

By contrast, Spice was designed to work with a limited number of models, all of which originally were created to represent transistors used in designing integrated circuits. A designer who wanted to create, for example, a radio circuit, would have to find a way to use those models to represent the different radio-circuit components, instead of the IC transistors they were intended to represent. Doing so was usually tedious and time-consuming—and sometimes impossible.

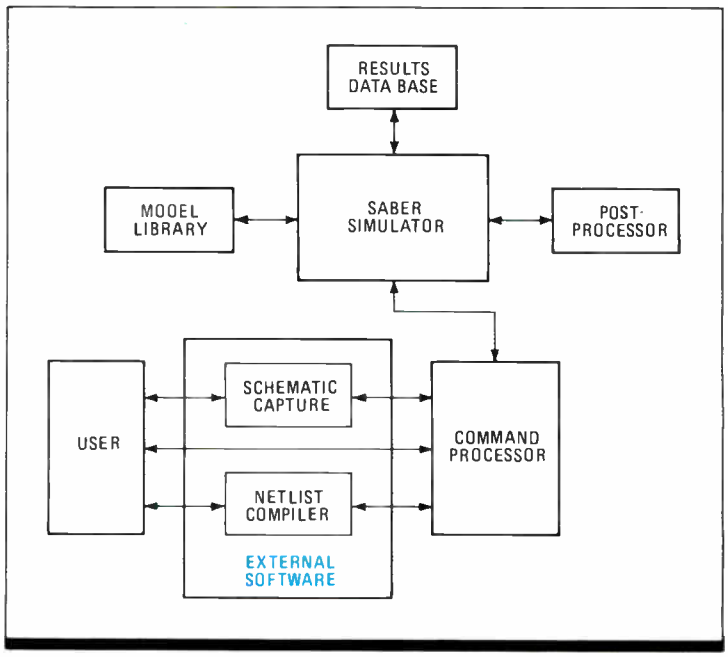
Saber allows engineers to use models that were designed to represent the components they are working with, not modified models that once represented something else. For example, an engineer who is designing the control system for a mechanical flap on an airplane wing would begin with a high-level block diagram of the design. The mechanism has a motor, a tachometer for measuring rate feedback, a power amplifier for driving the motor, and an encoder with a potentiometer or optoelectronic encoder for sensing motor position (Fig. 1).

Using Saber, the engineer can begin entering transfer functions of every major block in the design into a high-level, top-down block-diagram model. Transfer functions are the characteristic equations of a system, subsystem, or device. The motor, for example, has a transfer function that describes inertia characteristics and its mechanical and electrical time constants. These variables are all available in the data book on each motor.

PLAYING THE "WHAT-IF" GAME

"By entering transfer functions, the designer can evaluate various options in a 'what-if' type analysis to determine, for example, the amount of amplifier gain needed to position the motor in a given time," says Larry Jacob, president and chief executive officer of Analogy. "He can try several different motors to see which positions the fastest and which will be the most cost-effective." The simulator allows the designer to create a simulated breadboard for each of the design blocks, and evaluate each as if he had built the circuit with real components.

Simulating all the functions of this design with Spice would be difficult. The optoelectronic and electromechanical components would have to be reduced to an electrical-equivalent circuit, using components already defined in Spice. Saber is far more flexibile. The designer can define the operating parameters of each model in its own measurement units—the motor, for example, is defined in terms of torque, inertia, and so on, depending on the function being simulated.



2. MALLEABLE MODELS. Templates in the model library can be modified without affecting the performance of Saber itself.

This flexibility arises from Saber's design, which takes advantage of the mathematical nature of simulation. The model of a component in any simulator is the mathematical expression of its parameters. It has two parts: the template, which is the generic component model, and the parameters, which define a specific component.

With any Spice variation, "the model templates are an integral part of the program, and cannot be changed or added to," says Douglas Johnson, Analogy vice president. "Adding new templates requires changing the algorithm portion of the simulator. In these simulators, therefore, system components must be modeled from combinations of existing model templates, which places restrictions on what can be simulated."

In Saber, models are created from templates that are modular, not integral to the software; they can be modified by the designer. For frequently used models, such as transistors, the operating parameters are included as part of the template. For other models, such as motors and tachometers, the parameters are added later by the designer, who takes them from measurements or from data sheets.

Once a model is created by generating a template, it is entered into the simulation library (Fig. 2). The library is separate from the Saber simulator, so it can be constantly changed with-

out affecting the simulator itself. In addition, users who need to create models for which no template exists can do so using a modeling language supplied with the software.

During operation, the simulator draws models from the library; which models to use is determined by components described in the circuit netlist or a schematic supplied through a schematic-cap-ture package. From these, Saber computes how the circuit will behave. It calculates the voltage and currents at each circuit node, either at one point in time or in time increments. The intermediate and final results of the calculations are stored in a results data base. Postprocessing software uses the final results to produce waveform graphs that the designer can analyze.

SPEEDING THE SIMULATION PROCESS

Saber gets much of its speed advantage by eliminating Spice's initial step of flattening the design. Flattening means reducing a circuit design to its elementary devices, resistors, capacitors, and transistors. Then, to simulate an input signal, the waveform is divided into a series of time steps. At each time step, the resulting electrical values for each node in the path of the signal are calculated.

Saber gains additional speed by recalculating for each time step only at the nodes where values have changed. Optimizing the code for vector and parallel processing makes Saber even faster when it is run on dedicated simulation accelerators. Also, it can halt simulation, change values and parameters inside the simulated circuit, and resume operation from an arbitrary point. With Spice, any change requires recompiling the netlist, then rerunning the simulation.

The flexibility and speed of Saber enable it to simulate large circuits all at once; Spice must break circuits down into smaller sections and simulate them individually. "Saber has already been used on a mainframe to simulate an 8,000-device circuit in 15 minutes," says Johnson.

Analogy has further refinements in mind. A series of enhancements to the basic simulator package is scheduled for introduction by the third quarter of next year. They will allow designers to do "sensitivity analysis in which the value of each part—capacitance, resistance, etc.—is varied over its tolerance range to determine the sensitivity of the performance of the circuit," Jacobs says. Other features will allow designers to do optimization analyses, to find the ideal values for circuit components to achieve at given performance levels, and to evaluate the circuit's long-term reliability.

In addition, designers will be able to perform a worst-case analysis that checks every component at its tolerance limits, which helps ensure that if the tolerance builds up in the worst case, the circuit will still perform within specification. The simulator also will be able to provide an evaluation of the circuit's average performance over its lifetime. Finally, the company plans to add a digital functional simulator to allow mixed simultaneous analog-circuit and digital-logic simulation.

Thus, with one tool a designer sitting at a work station can complete his design all the way from a high-level block-diagram description to test program generation without ever building a single piece of hardware. Moreover, once the design has been developed on the work station, it should be sufficiently characterized that it will need little debugging. □

HOW JACOB GOT INTO ANALOG SIMULATION

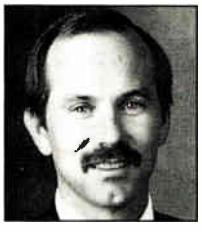
Larry Jacob spent a big chunk of 1983 looking for the right opportunity for a new business. He found it in design simulation for analog circuitry. "The one simulation tool available to do analog design was Spice," he says, "but it had and continues to have many limitations."

Seeking a new challenge, Jacob had just left Flight Dynamics Inc., a Portland, Ore., company that makes aircraft instrumentation. He had founded the company and taken it public, which gave him the cash he would eventually use to start Analogy Inc. in Beaverton, Ore.

JACOB

Designers' dissatisfaction with Spice had convinced Jacob that he had found the motherlode. Next, he had to find people to help him mine it.

He went to the library, to find out who was writing on simulation tools, and found Jiri Vlach and Kishore Singhal, both professors at the University of Waterloo in Ottawa. Jacob met them at the 1984 Design Automation Conference in Albuquerque, N. M. They were interested in his ideas; both eventually became technical consultants to Analogy.



JOHNSON

They also led him to Martin Vlach, Jiri Vlach's son. Martin had recently gotten his PhD from the University of Waterloo and, in the process, had written a new simulator that matched what Jacob had in mind. He also had just applied for a professorship at the University of Waterloo, but in January 1985, the school—and the Canadian winter—helped him change his mind about his career plans. "The university turned down my request for the position. It was 20 degrees below zero outside in Ottawa," he says. "I decided to take Larry up on his offer to move to Oregon and join the company."

VLACH

Jacob, meanwhile, had met Douglas Johnson, then at Metheus-CV in Hillsboro, Ore., who became interested in Jacob's ideas about analog simulation. By the time Analogy opened for business early in 1985, Johnson had joined up: he saw the new company was in the right place at the right time. CAE hardware vendors are going after the printed-circuit-board design and layout market. Printed-circuit boards have much larger analog content than integrated circuits. "Spice is something they can offer immediately, but eventually they are going to need something better. We expect to be that something."

PROBING THE NEWS

MUNICH'S MICROELECTRONICS CONFERENCE TAKES A NEW TACK

ELECTRONICA MEETING BECOMES A TECHNICAL EXECUTIVES' GATHERING

by John Gosch

MUNICH

As international conferences go, it's a small meeting—23 papers and an anticipated attendance of 400 to 500—and it only lasts a day and a half. But Munich's biennial Microelectronics Conference is a good-sized and ambitious show—nine of the papers are invited from the big names in Europe, Japan, and the U. S. Their common thread is competition.

The 12th edition of the conference, to be held Nov. 10 and 11 concurrently with the giant Electronica show (see "Electronica is bursting at the seams and still growing," p. 84), is trying a new tack this year by appealing to the technical executive and the beginning engineer rather than the designer—in effect, the present and the future buyers of microelectronic parts. The result is that the main subjects cover technology and economics in broad terms. Discussions are scheduled on the renaissance of bipolar technology, the emerging market for gallium arsenide devices, and the direction that standard integrated circuits will take.

SHARP DEPARTURE. The new focus, says conference chairman Leo Steipe, president of Munich-based Stenocord Electronic GmbH, is a sharp departure from past practices. "In former years we tried to cover as much ground in integrated circuits as possible," he says. The result: many sessions became so mired in details that they appealed only to a select few.

Not this year. Following the new format and theme, most of the main subjects concern some form of competition—between bipolar and MOS technologies, between silicon and gallium arsenide materials, and between standard parts and application-specific integrated circuits. Though none of these conflicts is new, the conference organizers hope the speakers and their papers will illuminate them from different angles, and in the process provide those attending the show with the latest perspectives.

Typical is the bipolar-MOS matchup.

SHOW SITE. Congress Hall will house the Electronica conference, as it did in 1984.

Kenji Taniguchi of the Hitachi Device Development Center in Tokyo will discuss the latest changes in both technologies, and what those changes mean for those who are applying CMOS and bipolar techniques to very large-scale integrated circuits.

Taniguchi will confirm that constant improvements in speed and density have made bipolar the leading technology for ultrafast computer logic, while CMOS will become dominant in medium-speed logic and memory, where the emphasis is on cost, and also play a principal role in gate arrays and polycell-type VLSI circuits. But there is a third element in the equation: BiCMOS, which merges bipolar with CMOS devices and is about twice as fast as CMOS. Its place will be in applications where high speed—typically above 100 MHz—and low power dissipation are required, or where bipolar interfaces are needed. Further, BiCMOS may play a big role in static random-access memories, providing 25-ns access times—twice as fast as CMOS.

Picking up the cudgel for bipolar in his invited paper, Armin Wieder of the Siemens Research Laboratories in Munich will single out the revival of bipolar techniques in the submicron range. After 15 years of competing with MOS, bipolar is still going strong because of its analog characteristics, very high intrinsic speed (gate delays less than 50 ps), and excellent device performance because of high transconductance. Those are exactly the properties that designers of the upcoming integrated services digital networks will look for.

ON THE MOVE. And with silicided contacts and very shallow doping profiles, bipolar transistors will open new fields of performance, with room-temperature gate delays of less than 5 ps, Wieder says. Applications ranging from analog circuits and real-time signal-processing devices to advanced communication circuits will, with bipolar's reliabilty and low cost, keep it on the move.

But what is coming after silicon? Bernard T. Murphy, a researcher at AT&T Bell Laboratories in Reading, Pa., believes the market is developing in compound semiconductors such as gallium arsenide.

In an invited paper, Murphy will cite several reasons. For one, although sili-

con still has a lot going for it, the rate of innovation in MOS is slowing. For another, there are high-performance jobs (as in monolithic microwave circuits) that silicon cannot do. What's more, owing to work on materials for laser and light-emitting diodes as well as on microwave field-effect transistor technology, a GaAs IC capability has already emerged.

But silicon is far from dead. Disputing Murphy about what is to come after silicon is Joseph Borel of Thomson Semiconducteurs in Grenoble, France. He will predict that a new silicon era is in the offing. Silicon, he says, has been gaining market share in many fields, particularly in memories, because it has provided an increasing number of functions per square millimeter at a constant price. This follows the rule that says the number of elements per chip doubles every two years but the price stays about the same.

At the same time, smaller and smaller dimensions, extending into the submicron range, allow a performance increase both with MOS and silicon bipolar technology, which should make them more competitive with gallium arsenide in the digital field. Further, advances in device structures, such as permeable-base transistors, will provide still higher performance, as will be the case with ballistic transistors.

Technologies aside, an invited paper by Peter Verhofstadt of Fairchild Semiconductor Corp. in Mountain View, Calif., will discuss standard chips versus ASICs. He will make the point that standard chips' growth potential—as well as that of the nonstandards—will still be significant for a while. However, standard circuits' slice of the total worldwide IC pie will continue to shrink.

The ASICs will make their greatest gains in VLSI logic, Verhofstadt predicts. Despite continued growth in memories, the worldwide sales of standard VLSI circuits should drop to 60% of the total market by the end of this decade. The figure in 1983 was more than 70%.

GETTING SPECIAL. Verhofstadt will predict that in memories, the number of bits per chip will continue to grow, but more and more special-purpose chips (such as video random-access memories) will appear. In microprocessors, performance of central-processor units (in terms of mips) will keep increasing. But there seems to be little need to go beyond 32-bit word lengths, the Fairchild expert says.

Although standard logic circuits will remain important well into the 1990s, a shift from TTL to CMOS will take place. The circuits will also move up in complexity to the level of large-scale ICs, in an effort to minimize the impact of off-chip delays on system speed.

What should also attract much attention is an invited paper from Bernd Höfflinger, head of the Institute for Microelectronics in Stuttgart, West Germany. Höfflinger will discuss application-specific VLSI and its effect on customer-vendor relations. He will point out that the customer, using work stations and hierarchically organized design tools, will have an increasing role in chip design. The role of the vendor, on the other hand, will be to teach the customer how to use the tools.

Also of note are invited papers from Peter Draheim of the Philips components-producing subsidiary, Valvo GmbH in Hamburg, and Paul Lin of the Motorola Microprocessor Products Group in Austin, Texas.

Draheim, discussing new approaches in digital signal processing through VLSI, will point to new uses of such devices in, for example, speech and video processing. Among these will be fast speech codecs for digital mobile phones, and memories to enhance TV displays.

Lin, discussing trends in VLSI high pin-count packaging, will predict that the fine-pitch plastic-leaded chip carrier, or FPPLC, with 25-mil pitch will be a major package in the near future. Lin also foresees hermetic chip approaches such as bumped-die, capped-die, or flip-chip technologies emerging in the pursuit of high reliability. □

ELECTRONICA IS BURSTING AT THE SEAMS AND STILL GROWING

The components industry it serves may have its ups and downs, but for the biennial Electronica exhibition in Munich, things are always up, in good times and bad. True to form, this year's biennial show, Nov. 11-15, will again be bigger than the one before. "We are bursting at the seams," says an official.

There will be some 2,300 companies—about 120 more than in 1984—exhibiting components and electronic assemblies on nearly 1 million ft² of floor space. They'll come from 36 countries in both East and West, on five continents—even from the tiny principality of Monaco.

The U. S. will check in as the biggest foreign exhibitor, with a total of 293 companies represented. Flocking to the Bavarian capital will be an estimated 120,000 visitors.

But it is not only the exhibits that make Electronica so popular. Held concurrently are symposiums and congresses, the most notable of which is the International Conference on Microelectronics. It will meet on Nov. 10 and 11 in the fairground's congress hall, a short walk from the exhibition area (see accompanying story). Then there is the Macroelectronics Conference on Nov. 13 (smart power devices, thyristors, and power supplies). Also of note are a symposium on quality assurance on Nov. 12 and a technical session on sensors on Nov. 14.

And Electronica is always a good place for spotting trends and recognizing what's hot in the industry. If in former years it was the microprocessor that captured the most attention, this year the digital signal processor will move into the limelight.

Visitors will no doubt hear of the exploding DSP market. In West Germany alone, consumption will rise from a meager $4 million last year to at least $40 million by the end of this decade. The impetus is the widening use of DSPs: today 75% are used in communications, but the big growth will be in the automotive market. The auto industry worldwide now uses 7% of total DSP consumption. But by 1996 its share should double, to roughly $150 million—with total DSP sales reaching $1.14 billion.

Another hot item at Electronica will be gallium arsenide devices, where the experts also see tremendous growth ahead. Europe, they say, will consume some $1 billion worth of GaAs devices by the end of this decade, which would translate into a 20% annual growth rate.

This year, GaAs parts will account for some 8% to 9% of the European semiconductor market, a share that should rise to 11% by 1996. At present, West Germany is the leader in consumption, followed by France, England, and the Benelux countries. About half of all GaAs parts are used in the civilian sector, with telecommunications accounting for about 75% of that total. *–John Gosch*

AISLE TIME. Some 120,000 visitors, like these at the 1984 show, are expected to attend next month's twelfth edition of Electronica.

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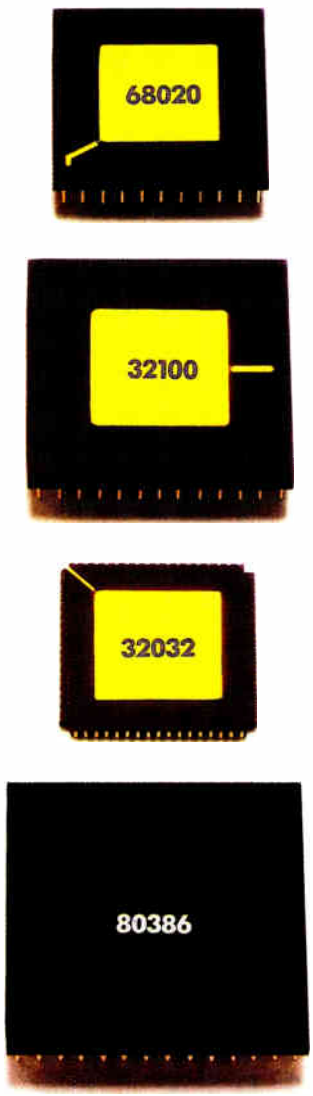
COMPUTERVISION

Circle 85 on reader service card

State-of-the-past.



State-of-the-art.

CLIPPER™ from Fairchild. The most significant advance in microprocessors since microprocessors themselves.

Unlike the others, its performance isn't limited by an architecture designed back at the dawn of the microprocessor era. It's built from the ground up with a brand *new* architecture, for today's high-performance applications. And it's the only microprocessor that can bridge the architectural gap to true supercomputer performance.

CLIPPER. The new definition of state-of-the-art.

How the competition wishes they'd done it.

In a highly integrated three-chip set, you get an architecturally advanced, very high performance, CMOS 32-bit compute engine, optimized for scientific and professional computing applications in the UNIX® operating system environment. In fact, you get everything in the three CLIPPER chips that it takes the competition's entire CPU board to give you.

Designed for high bandwidth and true concurrent execution of instructions, CLIPPER runs at 33 MHz. Which, until we proved otherwise, was considered impossible. CLIPPER achieves a peak execution rate of 33 MIPS, with average performance greater than a VAX™ 8600 – twice as fast as any other microprocessor in existence, five *times* as fast as a VAX 11/780. And floating-point performance exceeds 2 MFLOPS, while simple instructions execute in a scant 30 ns.

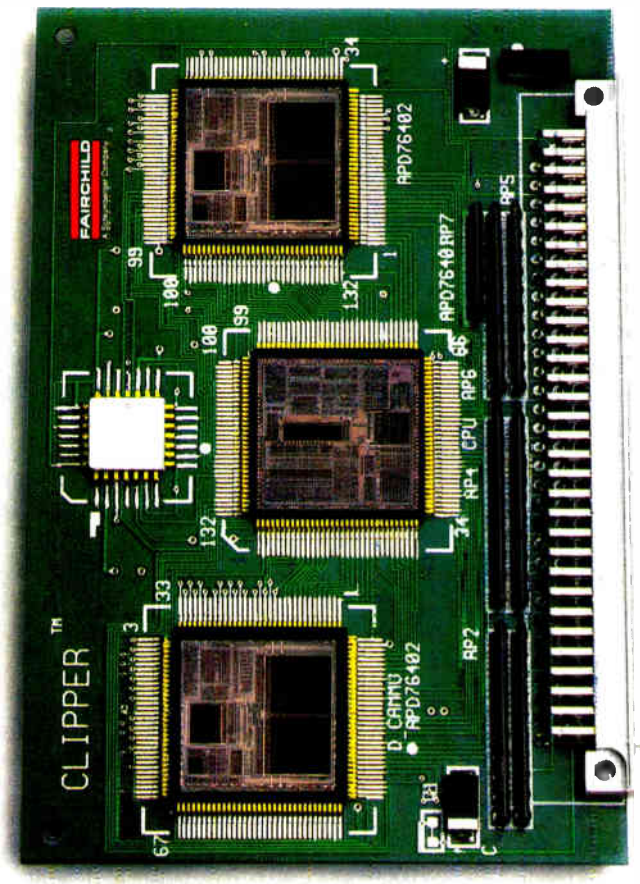
Supercomputer technology on a chip.

Unlike any other microprocessor architecture, CLIPPER uses proven supercomputer and mainframe architectural concepts.

Such as extensive pipelining. An on-chip floating point unit processing in parallel to a three-stage, pipelined integer execution unit. Two 32-bit buses, one for instructions, one for data, delivering up to 133M bytes per second to the CPU, eliminating bandwidth as a performance bottleneck.

Two large 4K-byte cache/memory management units (CAMMUs) provide mainframe-style, copyback caching concurrent with virtual address translation.

Then there's our Streamlined Instruction Set. With 101 instructions hardwired instead of microcoded for performance. There's also a macro-instruction unit, providing 67 high-level instructions and system functions. For all the advantages of RISC and the robustness of a CISC.



Actual die size approximately 140mil. x 440 mil.

What got into CLIPPER.

Residing on a 3.0 x 4.5-inch printed circuit card, the CLIPPER three-chip module includes a pipelined CPU with an on-chip, IEEE-standard FPU, and two 4K-byte cache/memory-management units. A clock generator completes the package, adding up to a staggering total of 846,000 transistors.

How CLIPPER backs you up.

CLIPPER is supported by a powerful software environment. Including a port based on the UNIX System V operating system. Optimized FORTRAN, C and Pascal compilers. Plus numerous utilities.

Or you can choose a complete VAX cross-support package.

And you're further supported by our application engineers and system designers. Each of them experts on CLIPPER.

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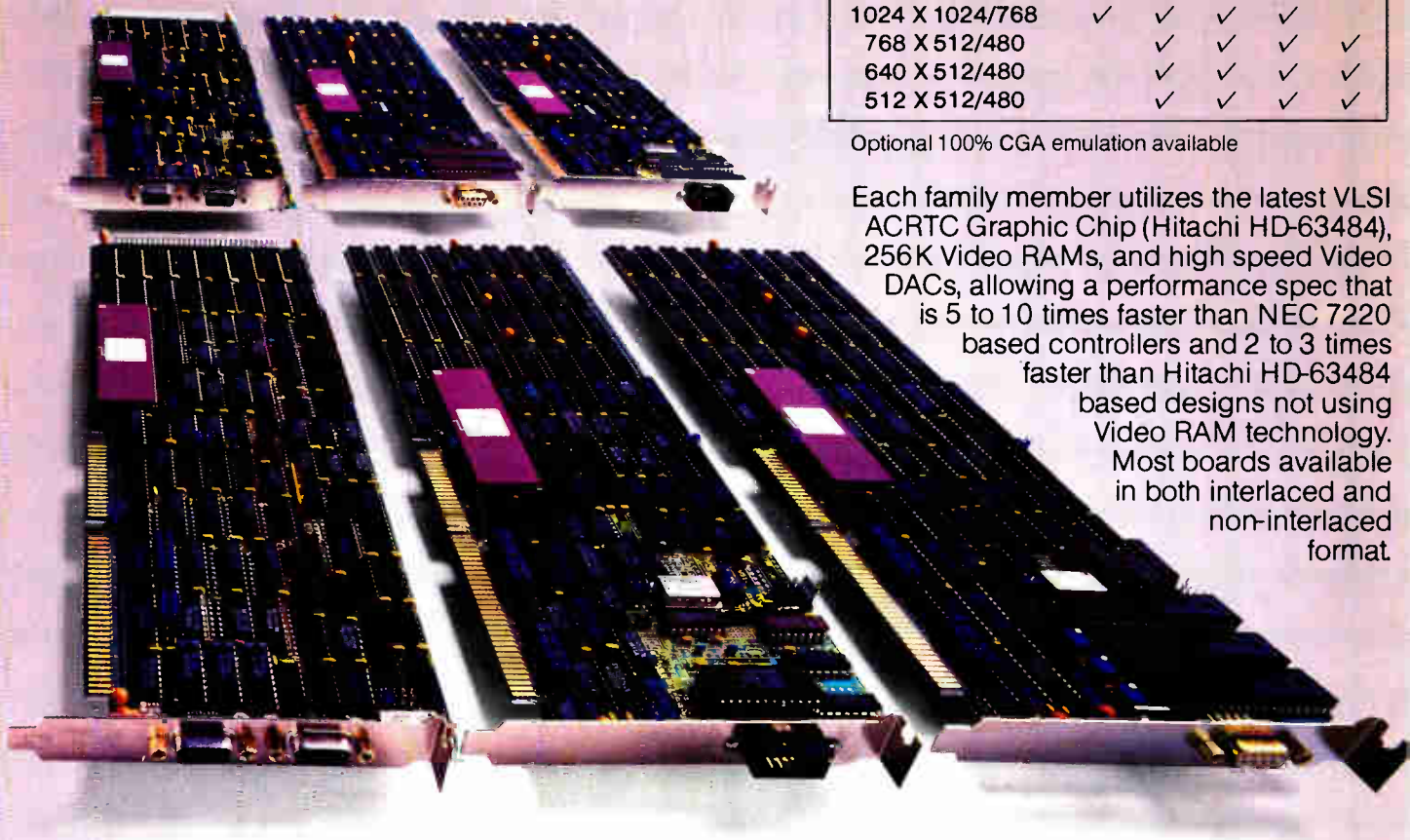
Display Resolution	Bits / Pixel 4	8	16	24	32
1280 X 1024/960	✓	✓		✓	
1024 X 1024/768	✓	✓	✓	✓	
768 X 512/480		✓	✓	✓	✓
640 X 512/480		✓	✓	✓	✓
512 X 512/480		✓	✓	✓	✓

Optional 100% CGA emulation available



Each family member utilizes the latest VLSI ACRTC Graphic Chip (Hitachi HD-63484), 256K Video RAMs, and high speed Video DACs, allowing a performance spec that is 5 to 10 times faster than NEC 7220 based controllers and 2 to 3 times faster than Hitachi HD-63484 based designs not using Video RAM technology. Most boards available in both interlaced and non-interlaced format.

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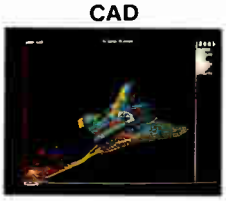
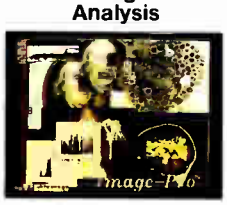


AUTOCAD

Image Analysis



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Circle 90 on reader service card

NEW PRODUCTS

FLASH CHIPS CONVERT A TO D AT 125 MEGASAMPLES/S RATE

HONEYWELL CLIPS DRIVE REQUIREMENT, KICKBACK CURRENT

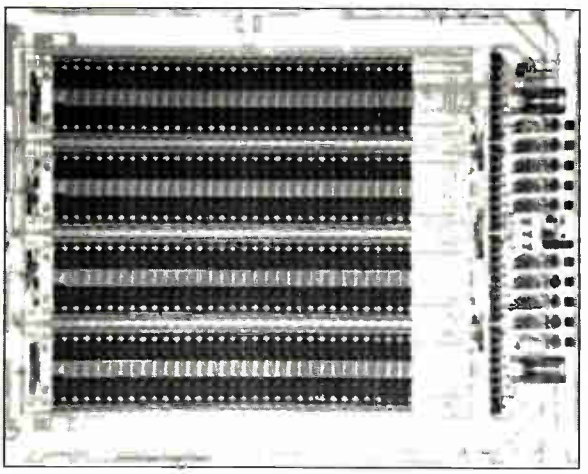
By minimizing drive requirements and damping kickback transients, Honeywell Inc. has designed a pair of analog-to-digital flash converters that convert a 2-V analog input signal with full-scale Nyquist frequency components into 8-bit digital words at a rate of 125 megasamples/s.

Fabricated in Honeywell's 2.4-μm Advanced Bipolar Digital II process, the new 8-bit, single-chip devices integrate 256 input preamplifiers between the circuit's reference ladder and its input comparators. Competitive flash-converter architecture is subject to variable input capacitance—a condition that leads to unstable input frequency and voltage. By buffering each of the circuit's 256 input comparators with preamplifiers, Honeywell makes its HADC77100 and 77200 chips easier to drive by holding capacitance at 60 pF. Moreover, comparator-preamplifier pairings increase input-signal gain sixfold, which gives each comparator a wider threshold range. This, in turn, reduces output errors caused by metastable states within the circuit.

LESS KICKBACK. Situating the preamplifiers between the circuit's reference ladder and its comparators reduces kickback in the analog circuit to 40 μA, the company says. Typical kickback for 8-bit converters is μA.

Honeywell's Signal Processing Technologies operation in Colorado Springs, Colo., has targeted a number of high-performance A-D applications for the new chips, including high-definition video equipment, digital oscilloscopes, transient-capture systems, radar, medical electronics, instrumentation, and direct radio-frequency downconversion systems. Steven J. Sockolov, marketing manager for high-speed data acquisition, believes the converters are the fastest flash A-D parts commercially available.

Housed in a 42-pin ceramic dual in-line package, the 77100 is compatible with Sony Corp.'s CX20116. The 48-pin 77200 has additional features, including five external reference-ladder taps—compared with three on the Sony-compatible part—and a data-ready pin for clocking outputs to high-speed memory chips or latches. The 77200 also has reference-force pins and an overrange bit for systems demanding higher resolution.



SYSTEM ENHANCERS. Integrating preamplifiers on-chip enhances system performance.

In most applications, external sample-and-hold circuitry is not required for accurate conversions because of the part's bandwidth. On board the chip are a tapped reference resistor and encoding logic and output register.

The 77100 and 77200 feature emitter-coupled-logic compatibility, with output drive of 50 Ω compared with 100 Ω for other flash converters. Operated from a single −5.2 V power supply, the devices dissipate a maximum of 2.2 W. They are available with operating ranges of −25° C to +85° C.

In quantities of 100, the 77100 costs $593.75 each; samples are available at a single-unit price of $350. Honeywell plans to offer 77200 samples in December at an introductory price of $350. When available in production quantities during the first quarter of 1987, the 77200 will cost $653 each in 100-piece lots.

–J. Robert Lineback

Honeywell Inc., Signal Processing Technologies, 1150 E. Cheyenne Mountain Blvd., Colorado Springs, Colo. 80906. Phone (303) 577-3705 [Circle 360]

CIRRUS CAN CUSTOMIZE DISK-CONTROLLER CHIPS

Using a proprietary, compiled-design methodology that yields circuits as dense and as fast as full-custom chips, Cirrus Logic Inc. has built an enhanced version of the industry-standard hard-disk-controller chip set. In addition, the new chips can be customized to include special functions.

In off-the-shelf versions that are software- and hardware-compatible with Adaptec Inc.'s AIC 300 and AIC 010 industry-standard chip set, the CL-SH120 buffer-storage manager and the CL-SH130 Winchester controller offer power savings of more than 50%. Specifically, the CL-SH130 consumes 400 mW at 20 MHz compared with 1,050 mW at 15 MHz for the AIC 010, and the CL-SH120 consumes 130 mW at 5 MHz compared with the AIC 300's 450 mW at 3 MHz.

But adaptability is the key advantage the Cirrus chip-set combination has over other Winchester disk-controller sets. Because they are fabricated using Cirrus' semistandard "redefinable" IC design methodology, "you can buy these chips as they are, or have them customized by us to your exact system requirements," says Cirrus President Michael Hackworth.

MADE TO ORDER. The CL-SH130 can be quickly customized to add I/O ports, add to or modify the writable control-store memory, expand or change the error-correction code polynomial, and add encode/decode to modify the microproces-

sor interface. Examples of customization on the buffer storage manager include additions such as logic for advanced Small Computer Standard Interface functions, on-chip buffer random-access memory, IEEE-488 bus interface logic, a dynamic RAM interface, processor address/data bus interfaces, logic for sector counting, and an on-chip formatter/controller function. Although software compatibility with the Adaptec chips is not preserved in customized chips, the user can request further customization, such as modifying the register set and the direct-memory-access management scheme.

Fabricated with a 2-μm CMOS process, the off-the-shelf versions are hardware- and software-compatible with the Adaptec chips, which are fabricated in 4-μm n-MOS. Although the chips target the high-performance disk-drive market, they can also be used to upgrade existing drives, says Hackworth. The set will be second-sourced by Silicon Systems Inc., of Tustin, Calif.

TESTS BETTER. Compared with earlier devices, the CL-SH130 Winchester controller offers important performance improvements, including additions to on-chip registers that improve testability. Besides offering speed and power enhancements, the CL-SH120 is designed to maximize throughput and simplify buffering of block-oriented peripheral controllers, the company says. Key performance improvements include a host-bus data-transfer rate of 2.5 megabytes/s.—twice the speed of previous devices.

The CL-SH120 can address up to 16-K bytes without multiplexing, and any buffer size greater than 16-K bytes in the extended-memory multiplexed mode, compared with a 1-K-byte limitation on previous devices.

The chip set supports most drive interfaces without modification, including Enhanced Small Disk Interface, Storage Module Drive, ST506/412, QIC-36 tape, and a variety of custom drive interfaces. Users can fully reprogram the CL-SH130's 32-bit error-correction-code polynomial and RAM-based sequencer to operate with a variety of drive interfaces and to define unique track formats. The CL-SH120 is designed to work with the CL-SH130.

Available now in a 44-pin plastic leaded chip-carrier package, the CL-SH120 costs $17.50 each in 100-lot quantities. The CL-SH130 10-MHz version costs $48 each and the 15-MHz version $52 each, in 100-lot quantities. The 20-MHz version's price depends on quantity.

–Bernard Conrad Cole

Cirrus Logic Inc., 1463 Centre Pointe Dr., Milpitas, Calif. 95035. Phone (408) 945-8300 [Circle 361]

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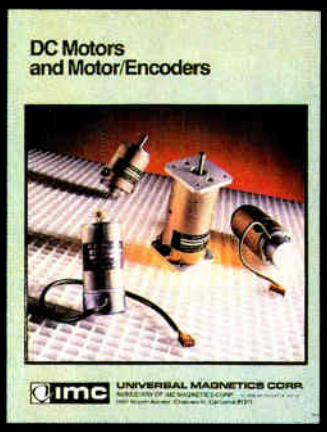
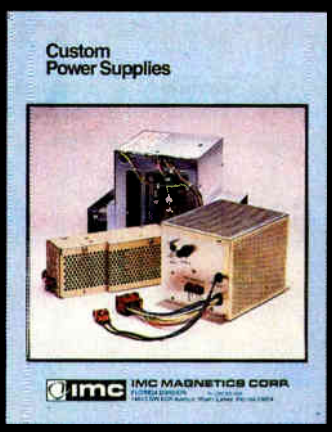


Circle Reader Service No.118
Catalog features DC motors and motor/encoders along with performance data and specifications.



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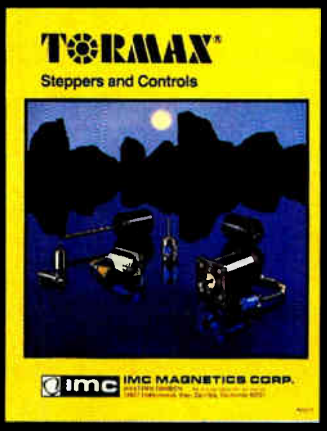
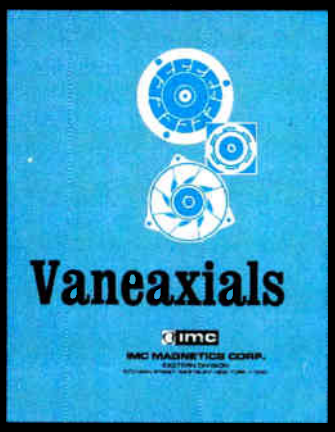
Catalog shows how you can benefit from IMC's consolidation of resources as well as other information pertaining to their custom built power supplies.



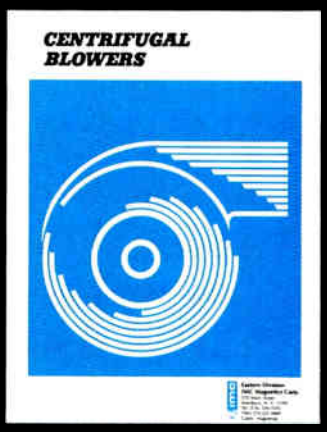
Circle Reader Service No.120
Catalog features specialty stepping motors and listing of controllers to drive them. Also chapters on theory of operation, excitation modes and applications.

Circle Reader Service No.121
Catalog gives general specifications on Synchron® AC timing motors as well as Magna-Torc DC motors. Products include clock movements, chart drives and slip ring assemblies.

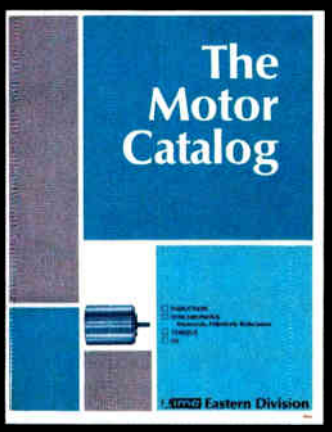
Circle Reader Service No.122
Portfolio contains spec. sheets on IMC's complete line of large vaneaxial units. Fans are ideally suited for cooling applications requiring a large volume of air.



Circle Reader Service No.123
Catalog contains information on air-movers rated for highest efficiencies. Included are charts as well as data on aerospace applications.



Circle Reader Service No.124
Catalog contains an extensive range of centrifugal blowers to meet a variety of cooling requirements.



Circle Reader Service No.125
Catalog is divided into sections for induction, torque and DC motors with sections devoted to technical information.

Keep Your Eye on IMC

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BLACK-ON-WHITE SCREEN RIVALS LETTER-QUALITY

MICRO-TERM DOUBLES THE NUMBER OF DOTS PER CHARACTER AND REDUCES FLICKER ON DEC VT-COMPATIBLE TERMINALS

A family of computer terminals from Micro-Term Inc. solves the problems inherent in displaying black characters on an all-white screen and gives a crisp appearance rivaling the look of high-quality printing on paper. The Foresight Edition 4500 series is compatible with Digital Equipment Corp.'s VT terminals.

Although other attempts to implement reverse-video—black on white—displays have fallen short of simulating a printed page, there was always reason to keep trying: experts believe that they would reduce eyestrain for operators who constantly look back and forth from printed page to video screen. Early attempts to do reverse video failed primarily because the large, brightly lit white area flickered too noticeably. Moreover, the small, black characters were hard to read because they were not as well-formed as those on letter-quality printers.

CRISP DISPLAY. Better phosphors and scanning techniques give Micro-Term's display a sharper image.

The 4500 series uses new monitor technology with better phosphors and innovative scan techniques to provide clean, crisp characters with twice as many black dots as usual against a soft-white, flickerless screen. The dots are so close together the user cannot see them; instead, fully formed, letter-quality characters appear on the screen, which has been overscanned—that is, scanned from top to bottom, edge to edge—to make it completely white.

HALF-DOT SHIFT. To eliminate spacing between the dots on the vertical axis, the designers raised the number of scan lines from 240 to 500. Closing the spaces between dots on the horizontal axis while maintaining character-cell compatibility with DEC's VT series terminals was more of a challenge. The engineers developed a timing technique called half-dot shift to combine a 20-by-20-dot character cell with 15-by-18-dot characters. DEC and other makers of VT-compatible terminals use a 10-by-16-dot character cell.

The half-dot shift is a timing maneuver performed during the horizontal scan. Successive dots are turned on or off a half-clock-cycle apart. To maintain compatibility with the 10-cell-wide character cell of DEC VT terminals while using new cells that are 20 dots wide, 10 cycles must be used to scan 20 dots. One-half cycle after the first dot is switched on or off, the second dot is switched—but the first one is not changed. At the beginning of the second cycle, the first dot is turned off or on, and the third dot is switched to its correct state. The process continues across all 20 dots in a cell. The first and third dots are equivalent to the first and second in a DEC VT terminal.

By doubling the scan rate to 34.2 MHz, Micro-Term designers reduced the flicker of the white background to the point where it is unnoticeable. This reduces eye strain for operators using the terminal for prolonged periods.

The Foresight Edition family's three models come with a 14-in. tilt-and-swivel monitor and three pages of display memory, each with space for 4,000 by 4,000 pixels. Terminals are controlled by a Zilog Corp. Z80 microprocessor and two gate arrays.

One array, which replaces about 100 discrete components and ICs, has everything required to run the display, such as the CRT controller, which handles scrolling, the memory interface, cursor generation, and horizontal and vertical timing. The other array takes care of video shifting, display blanking, and signal mixing.

GRAPHICS. The 4520 is an alphanumeric terminal with no graphics capability and is compatible with the DEC VT220, VT100, and VT52 terminals. The model 4525 is the same as the 4520 but with graphics capability. A plug-in monochrome graphics card with two kinds of graphics—DEC's Regis-compatible graphics and Tektronix Plot-10 compatibility—is available for the 4525.

A top-of-the-line fast graphics terminal, the model 4560, draws monochromatic graphics at the rate of 2 million pixels per second—comparable to the best midrange graphics on work stations and high-end graphics boards for personal computers. The 4560 provides DEC VT alphanumeric terminal emulation along with Tektronix 4010/4014 graphics compatibility to run Plot-10 applications software. The high-speed graphics on the 4560 are delivered by a team of processors—a Motorola 68000 microprocessor and a Hitachi Inc. ACRTC 63484 graphics processor.

The Foresight Edition 4500-series products, to be unveiled at the Comdex/Fall '86 show in Las Vegas next month, have a two-year warranty. The 4560 is priced at $1,296, the 4525 at $795, and the 4520 at $695. All three models will be available in December.–*Tom Manuel*

Micro-Term Inc., 512 Rudder Rd., St. Louis, Mo. 63026.
Phone (314) 343-6515 [Circle 340]

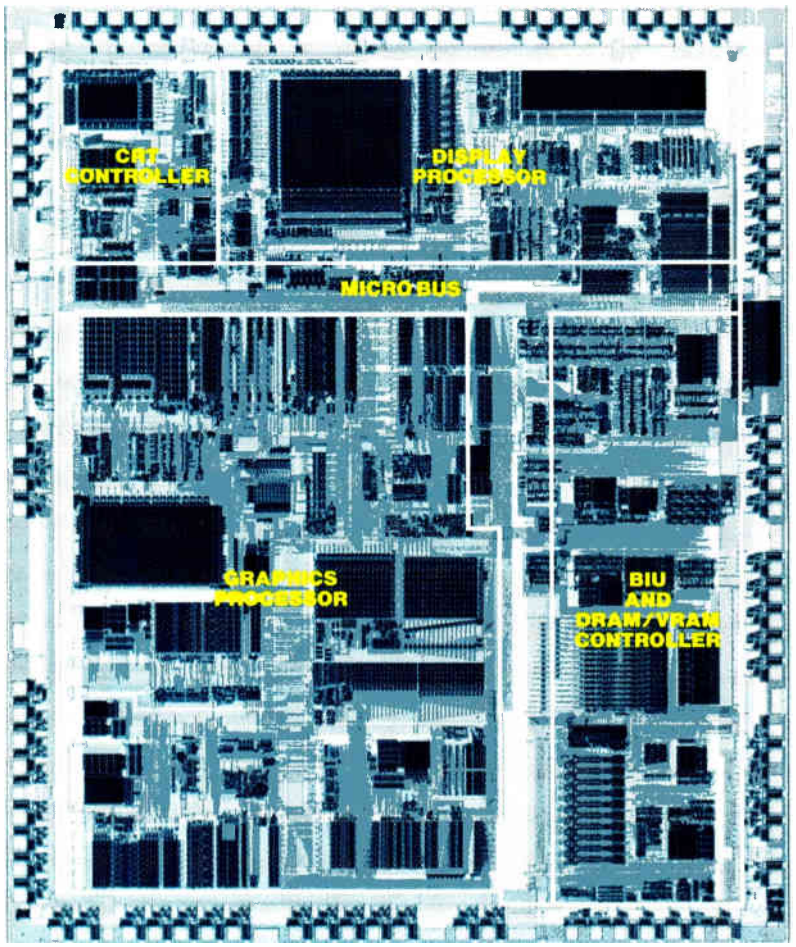
PLUG-IN CARD ACQUIRES ANALOG DATA IN REAL-TIME

Hitching an IBM PC, PC/XT, or AT directly to an incoming analog signal holds the promise of instant signal analysis and high-powered data manipulation, but, like many shortcuts, this one can end in frustration for users whose data-acquisition processor cannot keep pace with the incoming signal.

A plug-in card from Ariel Corp. offers a solution to that problem. The card provides 16-bit resolution and real-time data acquisition on two input and two output channels at a maximum 50-KHz sample rate.

High resolution and high speed tend to be mutually exclusive, and using multiple channels can further degrade system performance. But chiefly because Ariel's DSP-16 utilizes Texas Instrument's TMS32020 digital signal processor—one of the most recent and most powerful single-chip DSPs available—it

DOES WINDOWS.



Intel's 82786 graphics coprocessor supports its family of 16- and 32-bit central processing units.

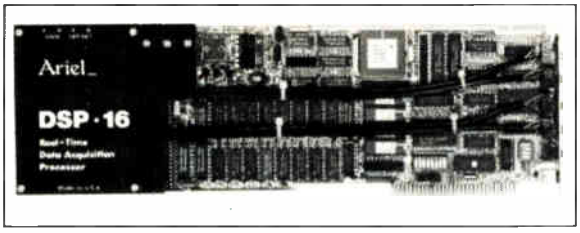
"Two completely different kinds of end customers seem to be fueling the embryonic graphics chip market: the personal computer user in business, and the designer on a work station. Intel Corp., long reported to be developing a graphics-oriented microprocessor, is finally announcing its 82786 graphics coprocessor for both applications.

Demand for multiple-windowing capability is on the rise, especially for multitasking chores in the office environment. The 82786 implements this capability in hardware. Each application can have its text and graphics drawn into separate regions of memory, which are then combined within windows of the same display. Large amounts of overhead associated with graphics tasks can be offloaded from the main system CPU by storing more text and graphics information in memory than is shown in the display..."

Excerpted from an exclusive article in the May 19, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE



NO-COST SOFTWARE. The DSP-16 comes bundled with six application software packages at no extra cost.

can operate on both channels of input and output with 16-bit precision at its maximum sample rate, with horsepower left over for real-time processing, says Mark Clayton, president of the New York company.

The card is both compact and affordable, using a single expansion slot of the computer's backplane and costing $2,495. Configuring an equivalent system with components would require no fewer than four devices: a high-performance data-acquisition board; a processing card; an analog-to-digital converter; and extensive PC-accessible memory, Clayton says.

The 32020's 5-million-instruction/s throughput makes possible complex processing and analysis of the acquired signal in real time. "We can guarantee throughput because our board doesn't involve the central-processing unit at all," Clayton says. In fact, the PC is left to do what it does best: set up and control the DSP-16 applications programs, and display, store, or retrieve the processed signal, Clayton says.

Another key to the DSP-16's performance is the combination of on-board sample-and-hold filters with memory capability. The standard memory buffer of 512-K bytes can capture and hold 5.25 s of data flow at the 50-MHz maximum sampling rate—plenty for most applications. Upgrades to 2 megabytes stretch retention to 21 s of data flow at a 50-MHz sampling rate. "Although other boards may claim higher sampling rates, their performance in real-life situations is limited by their data-buffering capacity," Clayton says.

Applications programs are loaded from the PC to 16-K words of high-speed, zero-wait-state random-access memory. A separate DSP-to-host interface permits program modification and data transfer even while the 32020 processes the incoming signal.

APPLICATIONS. To demonstrate the DSP-16's flexibility, Ariel has bundled six application programs with it, at no extra cost. Written in Microsoft Corp.'s C and 32020 assembly language, the software transforms the board into several devices, including a digital storage oscilloscope; a dual-channel, digital audio-delay line; a waveform synthesizer; an audio-loop editor that captures and edits sound; and a general-purpose program developer. Ariel invites further software development by original equipment manufacturers, Clayton says; he expects them to respond, since OEMs should find many uses for the card.

Ariel plans to introduce the DSP-16 at the Scientific Computing and Automation Show in Atlantic City, N.J., on Nov. 5. The board will be available later in the month. OEM discounts will be offered. *–Jack Shandle*

Ariel Corp., 110 Greene St., Suite 404, New York, N. Y. 10012.
Phone (212) 925-4155 [Circle 341]

CARTRIDGE PACKS 630 MBYTES ON TAPE

A half-inch cartridge streamer with a formatted capacity of 630 megabytes and an industry-standard Pertek interface marketed by MegaTape Corp. targets a growing data-backup market for increased-capacity hard-disk drives.

The cartridge's companion MT-750 drive is compatible with Digital Equipment Corp., Data General Corp., and Apollo Computer Inc. systems. The move to higher tape-storage capacity permits one-cartridge-per-disk backup and reflects the increasing number of Fujitsu Corp. Eagle XP and other high-capacity disk drives on the market.

MDC-750 tape cartridges have a data-density of 16,000 bits/in. and a 240-K-byte/s data-transfer rate. Backing up a 630-megabyte hard disk usually takes less than an hour, the company says. A 128-K-byte error-correction cache is standard on all models, and some models are compatible with the company's 500-megabyte products.

Available now, a system consisting of an MT-750 drive, 10 MDC-750 data cartridges, and accessories costs $15,500. Discounts are available for OEM-quantity purchases.

MegaTape Corp., 1041 Hamilton Rd., Duarte, Calif. 91010.
Phone (818) 357-9921 [Circle 345]

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Gate Arrays

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1000	66	4290	104	720	62
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*Customer-Specific Integrated Circuit

For RFQ or technical data, complete form below and return to: CSIC Marketing, OKI Semiconductor, 650 N. Mary Ave., Sunnyvale, CA 94086. (408) 720-1900.

RFQ

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OKI CMOS Gate Arrays

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2. Pin count: _____
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   - ( ) 2 micron
   - ( ) 3 micron
4. **Packaging preferred:**
   Surface-mount
   - ( ) PLCC
   - ( ) Flatpack

   Through-hole
   - ( ) Pin Grid Array
   - ( ) DIP
5. **Anticipated volume:**
   _____ pieces/month

☐ Please call me for immediate consultation.

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☐ Please rush complete technical input on:

- ( ) CMOS Gate Arrays
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- ( ) CMOS Custom VLSI Logic

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Address _____ City _____ State _____ Zip _____

EL 10/30/86

Circle 97 on reader service card

SIMULATION MODEL MIMICS ALL 68000 FUNCTIONS

QUADTREE'S CHIP MODEL SIMULATES MOTOROLA'S FULL INSTRUCTION SET, REGISTER STATES, AND PIN TIMING

Quadtree Software Corp., a two-year-old company specializing in modeling very large-scale integrated circuits, has reached new heights of simulation sophistication with full-function models of Motorola Inc.'s 68000 and 68010 microprocessors, along with a family of microprocessor peripheral chips.

In contrast to competing models that simulate only bus functions, Quadtree claims its Designers' Choice models handle all functions, including execution of the full instruction set, the state of internal registers, and the timing at the pins according to data-book specifications. Bus-level models do not permit the full simulation of a board design, and so they do not fully replace the breadboard prototyping stage, according to William Billowitch, executive vice president of Quadtree.

"Only full-function microprocessor models simulate the complex interactions between instruction execution, bus timing, and asynchronous interrupt handling," he says. "Timing information can be analyzed that would be unobtainable in a partial or bus-function model."

DEVELOPMENT SOFTWARE. To complement its Motorola chip models, Quadtree offers development-system software that allows a designer to proceed as if a hardware prototype were available and connected to a conventional development system. With this interactive, graphic environment, designers can set breakpoints, step through instructions, and observe and modify the contents of internal registers—including the program counter—to debug hardware and assembly-language software at the same time.

The models mimic the detailed timing characteristics of all instructions executed by the microprocessors. Instruction prefetching and pipelining occur as they do in the actual devices, and interrupt handling is performed with the proper clock-edge timing and protocols.

The models therefore can simulate detailed bus-protocol timing, which is intimately dependent on instruction flow. Interrupts are serviced at the precise moment in the simulation that the prefetch and execution sequences of the actual processor dictate.

Included in the package are Quadtree's X-Handling routines that deal intelligently with unknown conditions on the processor's pins. The routines report these conditions to the user when appropriate, but do not necessarily halt the simulation because of them, as other models generally do. For example, unknown data from failed components or sensors can be allowed to ripple through the system to study its effects. X-Handling software avoids burdening the designer with a flood of error messages. He is warned of unknowns on control lines that can affect the performance of the processor, but unknowns in the data stream of a block-move instruction, which might be data from bad sensors, can pass through without delaying simulation.

PERIPHERALS. Quadtree has many models for 68000-family peripherals, including the 68121 intelligent peripheral controller, the 68153 bus-interrupt controller, the 68230 parallel interface/timer, the 68440 two-channel direct-memory-access controller, the 68450 four-channel DMA controller, the 68451 memory-management unit, the 68488 IEEE-488-bus interface, and the 68681 dual universal asynchronous receiver/transmitter.

The company also plans to build models for Intel Corp.'s microprocessors, Advanced Micro Devices Inc.'s 2900-family bit-slice processors, and other manufacturers' memory ICs, says Billowitch. Quadtree already markets a model for Weitek floating-point math chips.

The models run on work stations from Sun Microsystems Inc. and Apollo Computer Corp. The single-host license fee for either the 68000 or the 68010 model is $3,500. Prices for the peripheral-chip models range from $500 to $3,000 when licensed individually, or $7,878 for the entire peripheral library ($6,500 if licensed in conjunction with one of the microprocessor models). The optional development-environment package costs $3,500. All are available 30 days after receipt of order. *–Jeremy Young*

Quadtree Software Corp., 1170 Route 22 East, Bridgewater, N. J. 08807.
Phone (201) 725-2272 [Circle 380]

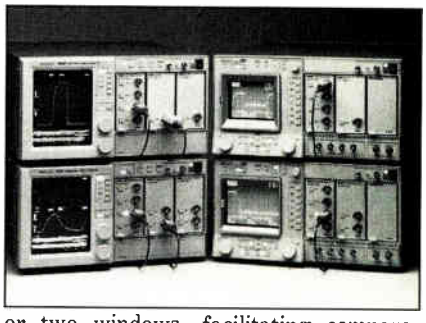
OSCILLOSCOPES HANDLE 1 GHz

Bandwidths of 1 GHz, 10- to 14-bit resolution, and up to 12 input channels highlight Tektronix Inc.'s 11000 series of oscilloscopes. Two digitizing and two analog versions are offered, all incorporating touch-screen control, interactive menus, and intelligent functions into the user interface.

Both digitizing models offer 10,240 sample-point waveform records and a 9-in. screen. The top-of-the-line 11402 has a 1-GHz bandwidth; the 11401, 500 MHz. The 11402 combines its high bandwidth with 10-ps horizontal resolution and 10-bit vertical resolution. Using signal averaging, it can achieve 14-bit vertical resolution.

The 11401 and 11402 accommodate 12 input channels, as many as eight of which may be displayed in any combination. With three optional vertical amplifiers, for example, the 11402 can display eight traces at 300 MHz, six traces at 600 MHz, and three at 1 GHz. Both oscilloscopes are accurate to within 1% of full scale and adjustable in 0.1% increments.

Major user-interface menus for the 11400 series include waveform, trigger, measure, store/recall, and utility. Controls are grouped on or near the infrared touch screen so users can focus on the display. To enhance measurement accuracy, the 11400 series includes 100-K bytes of data-point memory. It can display waveforms on the screen in one



or two windows, facilitating comparative measurements.

Tektronix's 11300 series of programmable analog oscilloscopes feature built-in, full-function counter-timers. The 11302 offers a 500-MHz bandwidth; the 11301, 400 MHz. Both can display a counter-view trace that allows the user to see the exact portion of the waveform being measured by the counter-timer.

Equipped with two vertical amplifiers, the 11300 series oscilloscopes can display eight traces at 250 MHz, and two at 500 MHz. Traces from other signals can be added or subtracted. Time intervals can be measured to ± 0.5% full-scale and ± 0.3% if dual delayed sweeps are employed.

The 11300-series user-interface menus add adjust/focus and numeric entry to the 11400-series menus. All four instruments are available now. The 11401 costs $13,000; the 11402, $15,500; the 11301, $8,550; and, the 11302, $12,950.

Tektronix Inc., P.O. Box 1700, Beaverton, Ore. 97077.
Phone (800) 547-1512 [Circle 385]

DEPOSITION SYSTEM AIMED AT WAFER RESEARCH LABS

SMALL-SCALE SYSTEM OFFERS HIGH REPRODUCIBILITY AND EPITAXIAL LAYER GROWTH AT ATMOSPHERIC PRESSURE

Building on six years of experience growing epitaxial layers in multi-wafer production applications for the IC industry, Spire Corp. has targeted the research-laboratory market for its newest metal-organic chemical vapor deposition system.

The SPI-MO CVD 240 was designed by the Bedford, Mass., company to grow high-quality epitaxial layers of III-V and II-VI compounds. Although the system's capacity is only two two-inch wafers, its reduced throughput allows a high level of uniformity in creating epitaxial layers and flexibility.

"It's a small system designed to do high-electron-mobility transistor (HEMT) devices at atmospheric pressure," says Spire sales manager Thomas C. Dearmin. This is the first instance of a small system working reliably at atmospheric pressure, according to the company.

The 240 offers fully automated process control through an IBM Personal Computer. It utilizes a vertically oriented radio-frequency-heated susceptor for uniformity of layer growth.

Operating temperature, which typically ranges between 400° and 1,100° C, is controlled to one degree by a feedback loop. Models are available for both atmospheric and low-pressure operation.

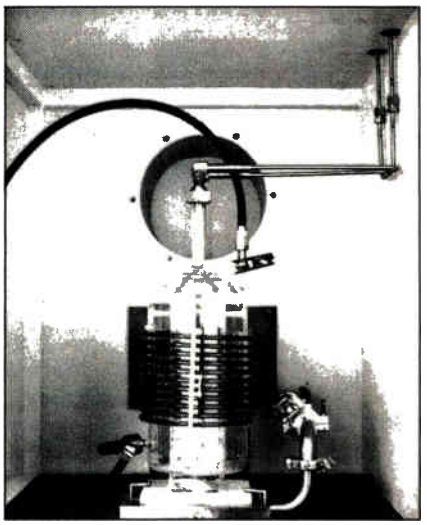
Type III-V and II-VI compounds grown in Spire vapor-deposition reactors include gallium arsenide, aluminum gallium arsenide, gallium phosphide, gallium arsenide phosphide, and gallium indium arsenide. According to Dearmin, one of the system's strongest features is its compatibility with other Spire vapor-deposition reactors, some of which have been marketed for six years. The 240 provides the same proven performance as Spire's other models, he says, and Spire has parts in stock.

As many as six metal-organic sources can be used in large-volume cooling baths. An upstream liquid trap is included for each metal-organic source to prevent accidental back-diffusion. Also available is a hydrogen-dilution system on either the metal-organic or the gas lines.

Process gases are switched using an injection manifold composed of four-port and three-port pneumatic bellows valves. Options allow a maximum of 15 gas lines to be introduced into the system.

A typical growth rate for the 240 is 0.06 μm/min, with an eight-hour day yielding between one and three two-wafer sets. Sheet-resistance uniformity exceeds 5%. The 240 system costs between $225,000 and $300,000, depending on selected options, and delivery takes about five months.

–Rick Elliot



EXACT. Spire's research deposition system reproduces epitaxial layers uniformly.

Spire Corp., Patriots Park, Bedford, Mass. 01730. Phone (617) 275-6000 [Circle 420]

SOLDER REPAIR UNIT FEATURES LOW HEAT

A pc-board repair/rework unit employs a recirculating molten wave of solder to avoid exposing the board to possible damage associated with the high temperatures of hot iron or iron/air vacuum techniques.

Virtually any size pc board can be reworked by operators with minimum skill with the Soldapak repair station from Electrovert USA Corp., the company claims. The solder wave is controlled by interchangeable nozzles that match the size and configuration of most components. A hand-held tool that is activated by downward pressure on the pc board uses low-pressure compressed air to clear lead holes. Soldapak will operate at temperatures as high as 650° F. Available now, the Soldapak costs $6,000.

Electrovert USA Corp., 4330 Beltway Place, Arlington, Texas 76018. Phone (817) 468-5171 [Circle 426]

QUICK-CHANGE HEADS SPEED PRODUCTION

Production of pc boards that require several different pin and terminal types or a specific angle for insertable components can be speeded up with a pin/terminal insertion system from Autosplice Inc. that features quick-change heads.

Head changes take only 15 minutes, the company claims. The system includes a microcomputer that can be programmed by keyboard, microcassette, or joystick. The insertable pins, terminal jumpers, and sockets are supplied to the machine on a continuous-reel tape. The complete system includes a rotary table that processes the pc boards and presents them to an operator. Available now, it costs $45,000 to $53,000, depending on table size.

Autosplice Division of General Staple Inc., 59-12 37th Ave., Woodside, N.Y. 11377. Phone (718) 429-0500 Circle [427]

DETECTOR CAN SPOT 0.2-MICRON PARTICLES

A laser-light surface-contamination analyzer that can detect particles as small as 0.2 μm also features haze contamination sensitivity as low as 0.6 parts per million and extended upper-range particle detection.

Upgraded front-end electronics enables the Surfscan 4500 from Tencor Instruments Inc. to detect and analyze particles from 0.4 to 1,024 μm^2 and particle haze as high as 102,400 ppm. The increased particle-haze range is useful for inspecting surfaces with high background-light scatter, such as polysilicon, the company says.

The Surfscan 4500 includes one direct-access sending cassette and one receiving cassette. Pass/fail sorting can be done with two cassettes.

After each laser scan is complete, five color displays are available on the user's control monitor, including particle maps, haze maps, and a histogram showing particle-analysis data. Available now, the instrument costs $115,550.

Tencor Instruments Inc., 2400 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 969-6767 [Circle 425]

Electronics CAREER OPPORTUNITIES

Fall 1986 Planning Guide

Issue		Closing
November 13	**Wescon Preview** Bonus Distribution at Wescon **Instruments Technology** Automatic Test Equipment	October 27
November 27	**Communications Technology** Fiber Optics Special Communication Career Section	November 10
December 11	**Year-End Double Issue** Executive Outlook **Semiconductor Technology** Linear ICs ISSCC **Military Technology** Special Section: Military Electronics	November 24

For more information, contact Susan Barnes-Ronga, National Recruitment Sales Representative, at (212) 512-2787

Project Engineer. Responsible for the design of custom switchmode power supplies; takes the project from its inception thru to final production; utilizes a variety of switchmode power supply circuit topologies that must include feedback control systems and off-line topologies of flyback, forward converter, full and half-bridge types; analog circuit design; power digital circuit design; heat transfer techniques; high voltage switching transistors; high frequency magnetics, and advanced mathematical/analytical skills; utilizes design and measurement techniques to assure product compliance to the FCC and VDE requirements of line conducted EMI (electromagnetic interference). Requirements: M.S. in Electronics Engineering and four years experience in the offered position or four years experience as Senior Electronics Engineer/ Power Supply Systems. Experience must include working on the design and development of switchmode power supply units; this additional experience may be part of the experience required above. 40 hours per week. 8:00 A.M. to 4:30 P.M. $42, 000 per year. Send resume to: Illinois Job Service, 910 South Michigan Avenue, Room 333, Chicago, Illinois 60605. Attention: L. Donegan. Reference No. 6223-L. An employer paid ad.

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We are a major producer of Navy Tactical Weapons and Systems, including Standard Missile, SPARROW, and the PHALANX CIWS. Exciting new projects have created openings for individuals to perform mission operation requirements studies, weapons systems requirements analyses, systems level trade-off analyses and performance requirements studies with emphasis on Naval Anti-Air Warfare and Anti-Submarine Warfare. Positions require a B.S. degree and experience in Navy AAW or ASW.

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‡ Advertisers in Electronics domestic edition

ELECTRONICS WEEK

IBM PULLS OUT OF SOUTH AFRICA

IBM Corp. said last week it would sell its South African subsidiary to a holding company set up for the employees of IBM South Africa Ltd. The deal, which followed a similar announcement by General Motors Corp., will allow the new company to represent other vendors. The sale should go through by March. Other U.S. firms are expected to follow IBM and GM's lead.

SIEMENS PRODUCES FIRST 1-MB DRAMs

Siemens AG's new chip factory in Regensburg, West Germany, has turned out its first 1-Mb dynamic random-access memories. Samples of the CMOS chips, which use 1.2-μm geometries, will be available in early 1987; volume production will start later next year. Meanwhile, at the Siemens Central Research Laboratories in Munich, parts from a next-generation 4-Mb DRAM, which will use 0.8-μm design rules, have already been tested successfully.

SIEMENS, BASF JOIN IN MAINFRAME DEAL

A new alliance looming in West Germany could spell trouble for IBM Corp. Siemens and BASF AG are setting up a joint venture to market IBM-compatible mainframe computers built in Japan. The new company will pool Siemens's sales of the Fujitsu 7800 computer line and BASF's sales of Hitachi's Series 7/XX mainframes.

BRAZIL OPENS DOOR A CRACK

Foreign firms that want a piece of Brazil's growing computer services market—worth $1 billion this year and growing 20% annually—can take a leaf from IBM Corp.'s book. The computer giant has become a 30% partner in a new teleprocessing service, Gerdau Servicos de Informática (GSI) SA, with the Gerdau Group, the country's largest native steel producer. But tough protectionist laws still block foreign investment in hardware manufacture and sale.

RCA ASTRO SIGNS $200 MILLION DEAL

RCA Astro-Electronics Division has signed a $200 million contract to design and build two 16-channel, high-power, direct-broadcast satellites for Advanced Communications Corp., a new company setting up headquarters in Washington. The satellites, which will be delivered by early 1990, will be powered by 125-w travelling-wave tube amplifiers and will transmit a variety of programming.

UNISON APPEALING COPYRIGHT RULING

A landmark decision that could establish copyright protection for the displays created by software programs as well as the code used to generate them is being appealed. The decision found that Unison World, Berkeley, Calif., had infringed on the copyright of a graphics program from Broderbund Software Inc. because of a similarity in screen appearance, not in computer code. Unison World plans to appeal the decision of a U.S. District Court in San Francisco. Unison says its program was independently designed and is written in a different language from the Broderbund package.

NATIONAL FIGHTS COURT BATTLE

National Semiconductor Corp. has filed in California Superior Court to block United Microelectronics Corp., a Taiwanese company, from selling in the U.S. a part that the San Jose, Calif., company claims is based on its design. United Micro wants to market a universal receiver/transmitter here, but National claims the circuit is based on documentation it supplied as part of an earlier foundry agreement.

COMSAT LENGTHENS SATELLITE LIFE

Comsat Corp., the U.S. arm of Intelsat, says a slight change in satellite operation can make geosynchronous satellites about 10 times more fuel-efficient—significantly lengthening their seven-year life-spans. By shifting the angle at which the satellite orbits relative to Earth, Washington-based Comsat says, the north-south drift (correction of which accounts for as much as 90% of a satellite's total fuel consumption) is reduced—without affecting the way the satellite appears to earth stations.

TURNER QUITS AT FLOATING POINT

Lloyd D. Turner has stepped down as president of Floating Point Systems Inc. His replacement is George P. O'Leary, who left the Beaverton, Ore., company in 1983, after 11 years as vice president, for an independent venture. Floating Point lost nearly $4 million on sharply reduced sales in the third quarter of 1986 and expects an even worse fourth quarter.

DEC IS DOING WELL IN GERMANY, TOO

Munich-based Digital Equipment GmbH topped $500 million in sales in fiscal 1986, which ended June 30. The West German subsidiary of Digital Equipment Corp., Maynard, Mass., scored a 20% sales gain for the year—more than double that of Europe's data-processing industry as a whole and one-third better than its parent's fiscal 1986 growth rate of 14%.

NEC IS BOOSTING V SERIES OUTPUT

NEC Corp. is increasing production of its V Series microprocessors from 250,000 to 300,000 per month by the end of the year, industry sources say. NEC claims that close to 100 companies are working on applications for the parts and that 30 firms have expressed interest in the 32-bit V60, samples of which are being shipped this month. NEC reportedly has a 1990 target date for producing a microprocessor based on 1-μm design rules capable of performing 10 million operations/s.

CARROLL TOUCH BUYS TOUCH TECH

Carroll Touch Inc., a leading maker of infrared touch-screen systems [*Electronics*, May 5, 1986, p. 42], has acquired Touch Technology Inc., an Annapolis, Md., maker of resistive overlay-touch input systems. Carroll Touch, a Round Rock, Texas, subsidiary of Amp Inc., claims the combined company now controls 40% of the nearly $32 million touch-screen market.

LOTUS LINKS 1-2-3 TO INSTRUMENT BUS

Lotus Development Corp. is trying to crack the market for scientific data-acquisition software with Measure, a new package that plugs instrument data directly into the Lotus' 1-2-3 spreadsheet program. At the same time, it introduced Manuscript, a word-processing program designed for technical professionals that also handles 1-2-3 inputs. Measure, which is the Cambridge, Mass., company's first product for engineers and scientists, can handle up to 15 devices simultaneously on the IEEE-488 bus. It runs on the IBM Corp. line of Personal Computers, Hewlett-Packard's Vectra, and Compaq's Portable. Both programs cost $495.

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1	16	31	46	61	76	91	106	121	136	151	166	181	196	211	226	241	256	271	348	363	378	393	408	423	438	453	468	483	498	703	718
2	17	32	47	62	77	92	107	122	137	152	167	182	197	212	227	242	257	272	349	364	379	394	409	424	439	454	469	484	499	704	719
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4	19	34	49	64	79	94	109	124	139	154	169	184	199	214	229	244	259	274	351	366	381	396	411	426	441	456	471	486	501	706	900
5	20	35	50	65	80	95	110	125	140	155	170	185	200	215	230	245	260	275	352	367	382	397	412	427	442	457	472	487	502	707	901
6	21	36	51	66	81	96	111	126	141	156	171	186	201	216	231	246	261	338	353	368	383	398	413	428	443	458	473	488	503	708	902
7	22	37	52	67	82	97	112	127	142	157	172	187	202	217	232	247	262	339	354	369	384	399	414	429	444	459	474	489	504	709	951
8	23	38	53	68	83	98	113	128	143	158	173	188	203	218	233	248	263	340	355	370	385	400	415	430	445	460	475	490	505	710	952
9	24	39	54	69	84	99	114	129	144	159	174	189	204	219	234	249	264	341	356	371	386	401	416	431	446	461	476	491	506	711	953
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11	26	41	56	71	86	101	116	131	146	161	176	191	206	221	236	251	266	343	358	373	388	403	418	433	448	463	478	493	508	713	956
12	27	42	57	72	87	102	117	132	147	162	177	192	207	222	237	252	267	344	359	374	389	404	419	434	449	464	479	494	509	714	957
13	28	43	58	73	88	103	118	133	148	163	178	193	208	223	238	253	268	345	360	375	390	405	420	435	450	465	480	495	510	715	958
14	29	44	59	74	89	104	119	134	149	164	179	194	209	224	239	254	269	346	361	376	391	406	421	436	451	466	481	496	701	716	959
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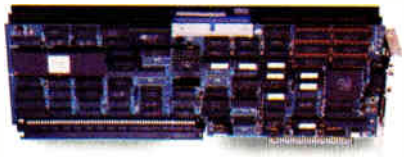

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