THIS SUPERCOMPUTER ALSO RUNS VAX/VMS PROGRAMS/74

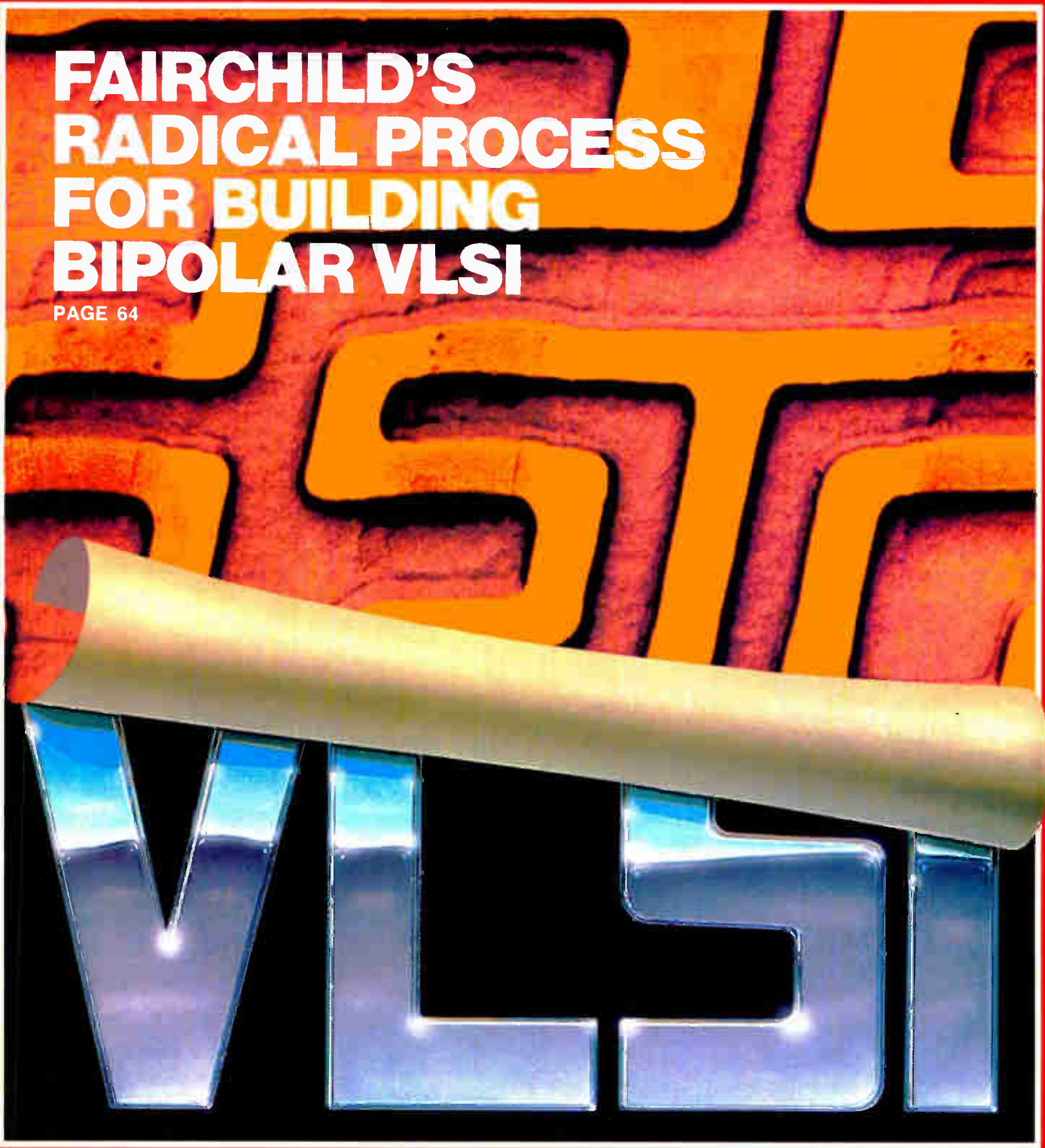
AN ATE SYSTEM THAT CUTS THE COST OF ASIC TESTING/81

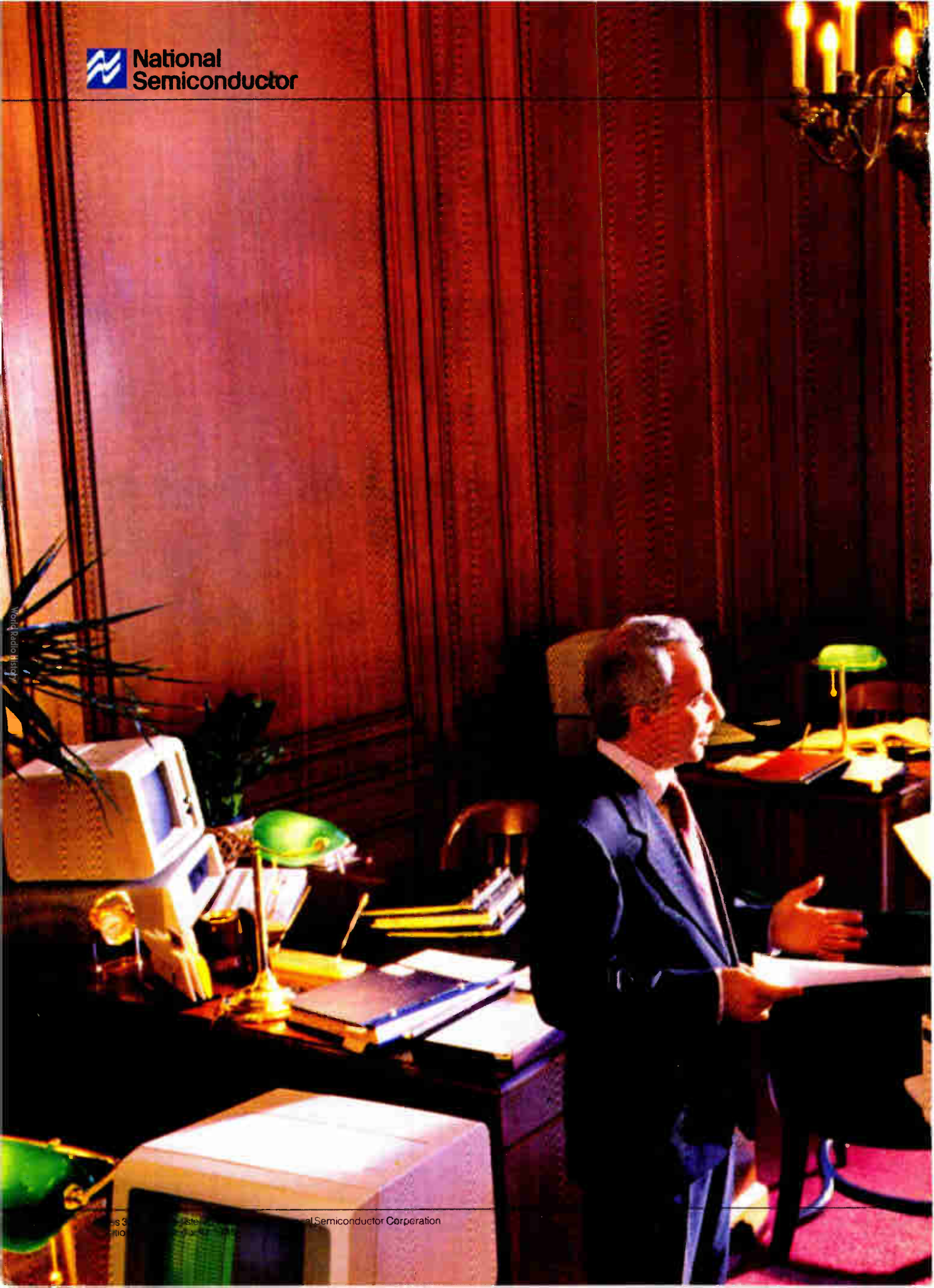
A McGRAW-HILL PUBLICATION SIX DOLLARS SEPTEMBER 4, 1986

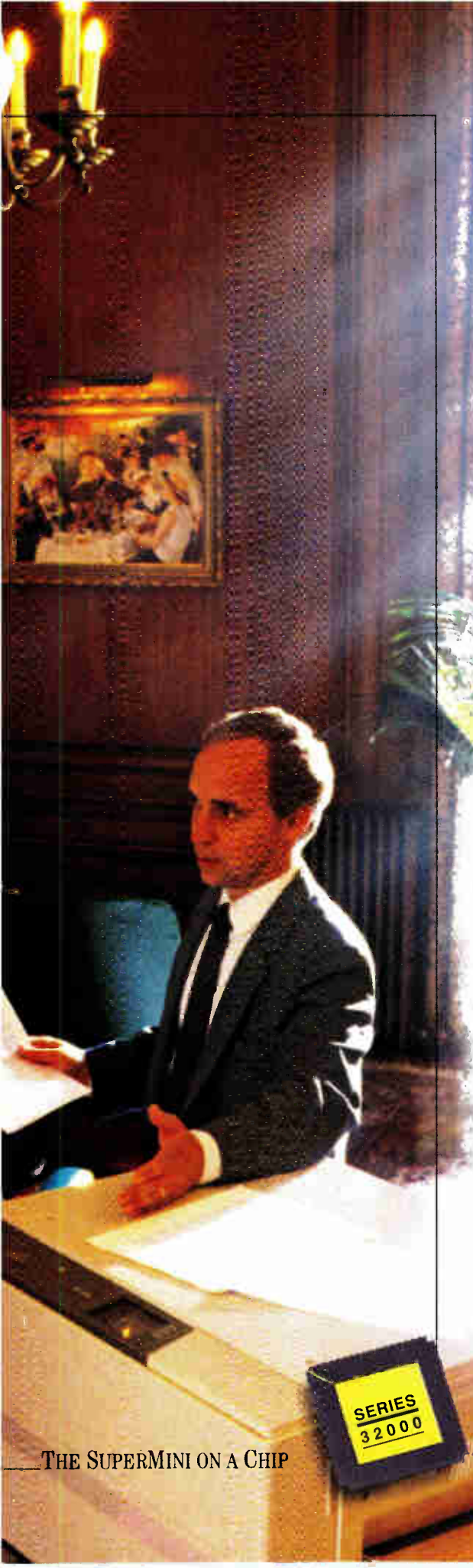
Electronics

FAIRCHILD'S RADICAL PROCESS FOR BUILDING BIPOLAR VLSI

PAGE 64







"This is great, it's supporting their entire office."

"And do it with the same wordprocessing software they've already installed."

"And that we would still be there... if it hadn't been for the Series 32000."

"Like we said, our one printer would replace four of their old daisywheels."

"Funny to think where we were just a year ago, isn't it?"

Only one 32-bit microprocessor could deliver the performance Dataproducts needed for their new laser printer. National's Series 32000 family.

Dataproducts needed a powerful product to fill an important market.

They wanted to introduce laser-printer speeds into daisywheel environments. So they developed the LZR-2630. It prints up to 26 pages a minute, a full page at a time, on demand. Yet it's fully compatible with the enormous installed base of wordprocessing software.

The secret of such speed and flexibility is National's Series 32000® family.

The Series 32000 performs *three times faster* than its nearest competitor in this application. So Dataproducts got the throughput they needed for their ultra-fast printer's engine.

They also got a powerful set of development tools, comprehensive diagnostic systems, full applications support, and the corporate-wide commitment of National Semiconductor.

So Dataproducts met the market demand for a high-performance cost-efficient solution.

Which means the Series 32000 is not only the right *engineering* decision for today, it's also the right *business* decision for tomorrow.

Find out how you can build the future into your own 32-bit design. Contact National Semiconductor today.

National Series 32000, MS 23-200
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Circle 1 on reader service card

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Help Wanted

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- Works unsupervised after hours.
- Able to travel.

MITEL CMOS MODEM ICs FIT THE JOB!

Today's modems must be more durable, smaller and, of course, more cost-effective than before. Mitel fills these requirements with 300 or 1200 bps CMOS modems that meet Bell 103/113 and 212A standards for North American products and also CCITT V.21 and V.22 standards for international markets.

The MT3530 Monolithic 300 bps Modem
The MT3530 is an ISO²-CMOS ™ single-chip, full duplex, asynchronous, FSK modem. For complete applications flexibility, this IC operates in many modes:

- Auto-Answer/Originate modes for smart modem applications.
- Manual mode for stand-alone RS-232C modem applications.
- Pass-through mode for protocol independence.
- Test mode for analog and digital loopback.

This IC has on-chip transmit and receive filters, a 4.8 KHz UART clock output, and is TTL compatible.

The MT35213/212A 1200 bps Modem Set
The MT35213 is a single-chip, full duplex 1200 bps, PSK modem with a 300 bps FSK fallback mode for operating in adverse signal conditions. This IC has a 48 dB dynamic range and has loopback capability in both analog and digital.

The MT35212A Modem Filter uses switched capacitor techniques to implement both the filtering and equalization requirements of Bell 212A and CCITT V.22 modems. For CCITT V.22 applications, this device supplies a notch filter that provides selectable 1800 or 550 Hz rejection. This IC offers on-chip answer/originate mode selection and includes half-channel compromise amplitude and group delay equalizers; two uncommitted op amps can be used for anti-alias filtering.

These parts are available in plastic or ceramic dual-in-line packages. Contact your local Mitel sales office for further information.

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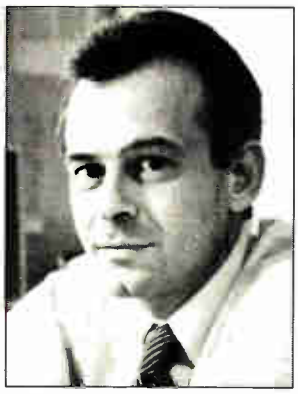
Electronics

PUBLISHER'S LETTER

There's a new name on our masthead, that of the person who's filling one of the most important slots in New York: Larry King, our copy chief. Larry is the editor responsible for seeing that every word in every article in the magazine says unambiguously what it's supposed to say, and that all the words flow smoothly through the editing process.



KING: In charge of seeing that the words mean what they say.

And that's no simple task, particularly on *Electronics*. Telling our readers what they have to know about a technology as complex and a business as competitive as electronics is a process that requires hours of work behind the scenes by a small army of talented people. Reporting and writing a story are only the first steps in that process.

No publication in the electronics press works so hard and so thoroughly on its copy as *Electronics*. To understand how the system works, take a typical news story—such as the one in the Aug. 21 issue from our Tokyo bureau chief, Charlie Cohen, headlined "Master slice has bipolar functions, CMOS logic."

The story was transmitted to New York, to the queue of news editor Jeremy Young, via the McGraw-Hill Pubnet network. Jeremy copied it electronically and sent it to our Silicon Valley bureau, in San Mateo, Calif., to semiconductor editor Bernie Cole, who helped evaluate the story in light of what's happening in the U.S. IC industry. At the same time, Jeremy edited the story and executive news editor Art Erikson looked it over, after which it went to the copy desk queue, where King swung into action by reading it and assigning it to a copy editor.

After the copy editor polished the story, it went back to Young, who sent any questions from the desk—as well as those from Cole—to Cohen. His replies were incorporated in the piece, which was then read again by *another* copy editor and sent into production. But that's not the end, for the next day a typeset copy of the story was read by the editor-in-chief and the two executive editors.

King is a kind of quarterback, handing off stories and articles to editors and also taking part in the planning process that decides the direction and depth of our coverage. His background has prepared him well for this exacting work, which requires expertise in both the language and the technology, as well as the ability to organize well and react quickly under pressure.

King, 34, grew up in Virginia. He has a BS in journalism from Virginia Commonwealth University and has worked on newspapers in Virginia and upstate New York. Before coming to *Electronics* he was assistant managing editor/features of *InformationWEEK*.

Laurence Altman

September 4, 1986 Volume 59, Number 30
108,590 copies of this issue printed

Electronics (ISSN 0883-4989) Published biweekly by McGraw-Hill Inc. Founder: James H. McGraw 1860-1948. Publication office: 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P.Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879 Cable address: M C G R A W H I L L N E W Y O R K.

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Editorial department phones: Administration (212) 512-2645, News and New Products (212) 512-2685, Technology (212) 512-2666. Bureaus: Boston (617) 262-1160, Chicago (312) 751-3811, Dallas (214) 458-2400, Los Angeles (213) 480-5234, New York (212) 512-3322, San Francisco/San Mateo (415) 349-4100, Washington (202) 463-1650, Frankfurt 72-5566, London 493-1451, Paris 42-89-03-80, Tokyo 581-9816. **Business departments:** (212) 512-6435 (Business departments follow the Advertisers' Index).

SEPTEMBER 4, 1986

Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: PHOTO BY FAIRCHILD, ART BY JEFFREY LYNCH

PAGE 64

NEW PRODUCTS

DEPARTMENTS

WEEK 46

Sick of working in half the space you need? Heartbroken at having to leave out those exquisite little bits of code? AMD has the cure. The 8053 Single-Chip Microcomputer.

8053

4K ROM free. No green stamps.

The 8053 is just like our high-spirited 8051 except you get 4K bytes of extra ROM. Free. Just like the 8051, it has two 16-bit timers, four 8-bit I/O ports and 128K x 8 RAM. But where the 8051 has a 4K x 8 ROM, the 8053 has an 8K x 8 ROM.

And all this doesn't cost any more than the 8051.

For prototyping and development work, we have the EPROM version: The 8753.

We think giving 4K ROM free is a very generous offer. You'll never miss the stamps.

WEEK 47

Just remember AMD's new 4K x 4 CMOS SRAMs: The Am99C58 and the Am99C59. They have the fastest 16K CMOS SRAM access time around: 20ns. But even at speeds like that, they don't forget what they're made of: An advanced CMOS. So they don't use much power.

Am99C58/59

The fastest way to improve your memory.

What else could you ask for in an SRAM?

You could ask for separate I/O. Okay. Both chips have separate I/O ports to eliminate bus contention snarls and give you faster throughput. Being able to fly through like that increases performance by 20%.

The Am99C58 also has a chip enable function which automatically powers down the chip when deselected. And that decreases power consumption by over 70%.

The Am99C59 has a scorching 10ns chip select access time which will increase memory system throughput. It's just the thing for cache memory applications.

With the fastest access times around and separate I/O, AMD's Am99C58 or Am99C59 CMOS SRAMs give you the options you need to improve your memory. Fast. And that's worth remembering.

WEEK 48

It's about time someone met the needs of the stingy. And AMD did it. With our new Am29C841 High-Performance CMOS 10-Bit Latch. Another member of AMD's Bus Interface Family.

The Am29C841 gives you speed comparable to a bipolar latch—with a propagation delay of only 11ns. But it only uses 80 microAmps at stand-by. That should warm any power-pincher's heart.

Am29C841

A latch for the stingy.

In addition to saving power, the Am29C841 is 10-bits wide. That extra data width is just what you need for wider address/data paths or buses carrying parity.

Use the Am29C841 instead of a bipolar latch when you need only moderate drive capability. The CMOS Am29C841 provides 24mA drive. Its MOS/TTL compatible inputs and outputs mean you can use it with both bipolar and MOS systems.

You don't necessarily have to be stingy to want a low-powered, high-performance latch like the Am29C841. You just have to be wise, far-sighted and exceptionally bright.

Circle 151 on reader service card

Circle 152 on reader service card

Circle 153 on reader service card

WEEK 49

Nothing travels faster than a good rumor except the data in AMD's new Am9580A Hard Disk Controller. A single chip that can make data approach the Speed of Gossip.

Am9580A

Only rumors travel faster.

To achieve this feat, we designed the Am9580A with on-board sector buffers. These make data easier to find so it's easier to pull up when it's needed. We also designed in Direct Memory Access (DMA). DMA retrieves data and transfers it directly to the main memory. And that takes a burden off the CPU.

But what really makes us a challenger to the coffee room is our Zero Sector Interleave. A user can pull up random data as much as six times faster than other hard disk controllers.

The Am9580A supports the ST 506 ANSI standard interface and the ESDI interface (which the coffee machine doesn't). And it's flexible. Handle any combination of up to four hard or floppy disk drives.

Get in and out of storage faster than ever with the Am9580A Hard Disk Controller. And, in case you were wondering, we got all this information from a very reliable source: AMD. Pass it on.

Advanced Micro Devices has broken the game wide open.

After building a comfortable lead with a new product a week, every week—on the shelf, in volume—we called in the heavy hitters:

ISDN. CMOS. 32-bit microprocessor chip set. High-speed RAMs. Modems.

No one who follows the game closely is the least bit surprised. This team puts more dollars into R&D, as a percent of sales, than anyone else in the business.

If you like the sound of extra bases, call Advanced Micro Devices.

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Circle 154 on reader service card

FYI

Almost every time we've ever heard that kind of doom-and-gloom forecast, the market has ended up bouncing back higher than ever

One big advantage that comes from covering the electronics industry for as long as we have is knowing that history can and usually does repeat itself. That certainly holds true for product demand. Granted, the past year has been a tough time for U.S. chip makers. And computer sales may be in the dumps because there is too much capacity in place. But we don't go along with those people who now paint an uncertain future for these markets. Almost every time we've heard that kind of doom-and-gloom forecast, the market has ended up bouncing back higher than ever.

Stick around. The same magic is going to happen once again. The first thing we need is innovative new products, and on a late-August trip to California's Silicon Valley, we were struck by the huge number of products in development and by the many classy new products that have recently been introduced or soon will be. National Semiconductor Corp., for example, introduced 154 new chips in the past 12 months, 80% of them proprietary designs, reports Jim Smaha, who heads the semiconductor group.

Much of the talk around the Valley centered on another flood of new products—those being designed around Intel Corp.'s 80386 microprocessor. As many as thirty 386-based products will be announced this year, predicts George Alexy, Intel's microprocessor marketing manager. He's now about to ship the first lots of thousands of the 386.

There were other rumblings in the Valley that made us feel a lot better about the state of the industry. Executives at Hewlett-Packard Co. see more blue sky ahead as their overall order backlog grows in the U.S. as well as overseas. HP wrote $1.86 billion in orders during the quarter ended July 31, up a tidy 25% from the year-ago period.

And an ebullient T.J. Rogers was claiming bragging rights at Cypress Semiconductor. He is logging a book-to-bill ratio of more than 1.3 for his lines of SRAM, PROM, and PLD products. But the icing on the cake was the San Jose company's second-quarter profits of $3.27 million: up from a year-ago loss and 66% over the previous quarter. And sales hit $12.26 million, an awesome 330% over the year-ago quarter. "I'm still production-limited," Rogers claims, but a second wafer fab line should help solve that problem next year.

Those are just a few of the reasons why we're convinced history once again will repeat itself. **ROBERT W. HENKEL**

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125 MHz BW; 100 MS/s ADCs; 5 GS/s Interleaved Sampling; 128 k Waveform Memory; ± 1% Accuracy; Summation and Continuous Averaging; Arithmetic Processing; Fully Programmable.

PROGRAMMABILITY. All settings of the 9400 Digital Oscilloscope are programmable; you can operate the instrument in unattended areas or as a computer-aided testing station. You can redefine the softkeys and send messages to the display, in order to step inexperienced operators through complex test procedures. And even without a computer you can store and quickly reproduce up to *eight front-panel setups*, for your most common measurements.

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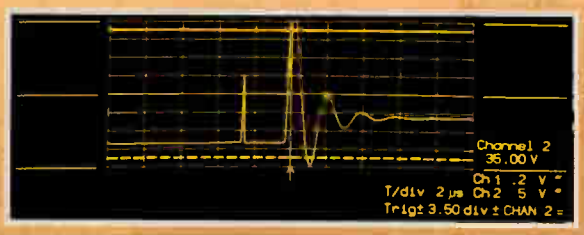
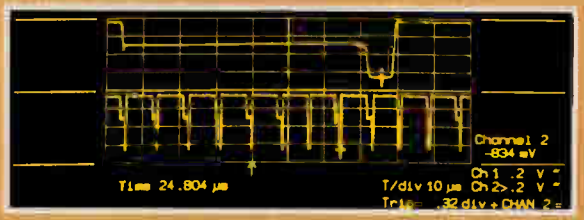
ARCHIVING. *On-board firmware* makes archiving of measurement results by a digital plotter fast and easy. The entire display may be dumped in any size to a wide range of high-resolution multicolor plotters—ready for publication or immediate presentation.

★And there is much more to say about this versatile and cost effective ($9900 base*) DSO. **Call us now...for details and a demonstration!!** *USA price list only





Top: Acquisition Parameters listing enables the 9400 user to precisely set and check front panel settings, all of which can be remotely controlled.

Middle: Window mode trigger set at ± 3,5 divs from center grid captures switching transient. 50% pre-trigger shows contact bounce prior to trigger moment.

Below: Crosshair marker, acting as a precise timer and DVM, gives times from trigger (arrow) and absolute voltage.

LeCroy

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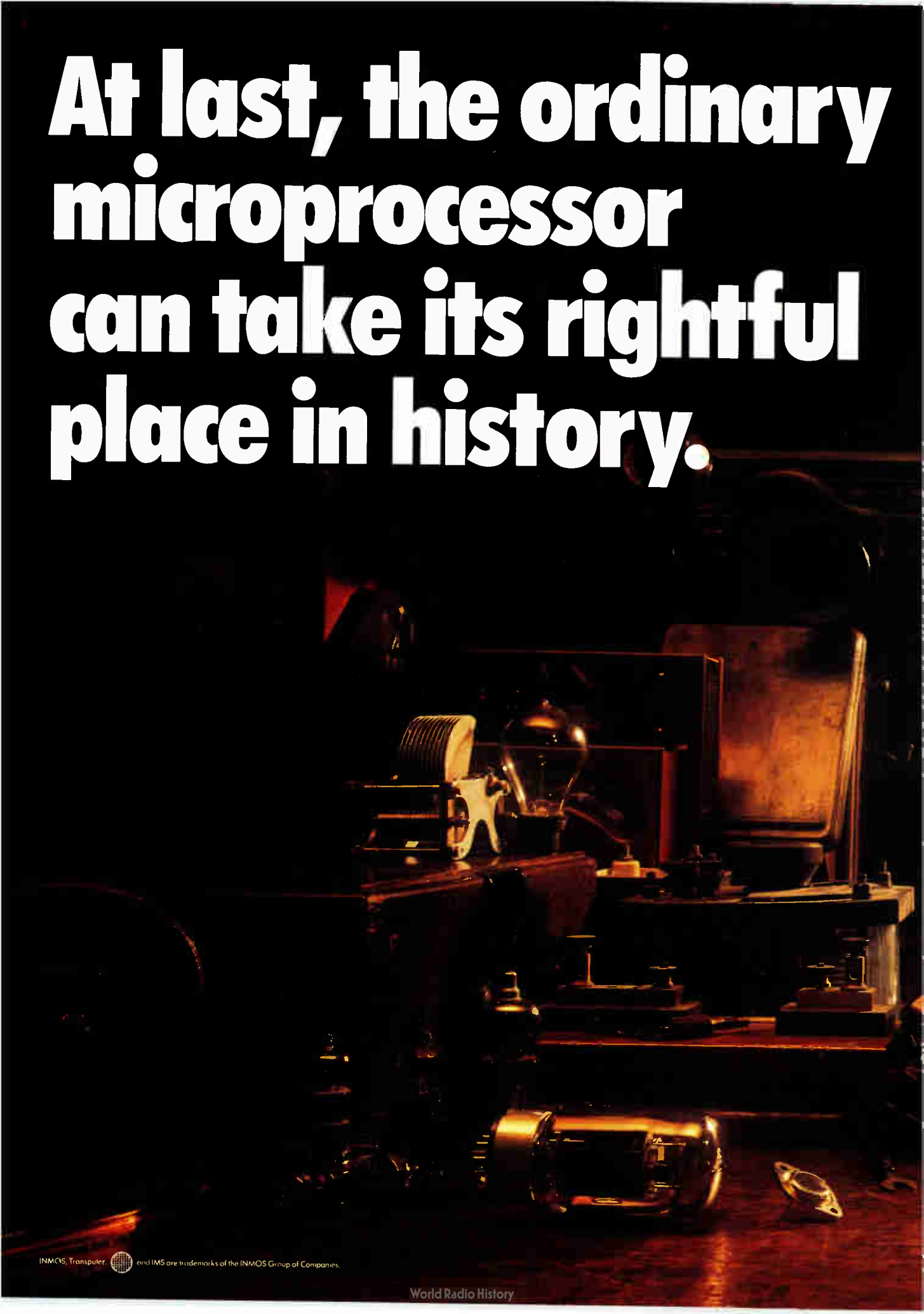
Circle 168 for Demonstration

Circle 9 for Information

At last, the ordinary microprocessor can take its rightful place in history.



It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

The IMS T414 transputer is a fast, easy-to-use VLSI component, integrating a 32-bit processor, four inter-transputer communication links, 2K bytes Static RAM, 32-bit memory interface and DRAM controller. All on a single CMOS chip—offering execution rates up to 10 MIPs.

While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

And there's more. Programming multiprocessor systems has never been easier. The Transputer Development System (TDS) supports C, Fortran, Pascal and OCCAM, providing a complete software development environment, and is available for a number of popular hosts. Software developed on the TDS can be executed on one or more transputers, enabling cost-performance tradeoffs to be made.

INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

TRANSPUTER PRODUCTS	
IMS T414	32 bit Transputer–2Kbyte —4 links
IMS T212	16 bit Transputer–2Kbyte —4 links
IMS M212	16 bit Disc Processor–1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
IMS B002-2	Double Eurocord + IMS T414 + 2Mbyte DRAM + 2 x RS232.
IMS B003-1	Double Eurocord + 4 x IMS T414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Formot + IMS T414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocord + 9 x IMS T212 + 128Kbyte SRAM.
IMS B007-1	Double Eurocord + IMS T414 + 0.5Mbyte DRAM + 0.5Mbyte VideoRAM.
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Circle 11 on reader service card


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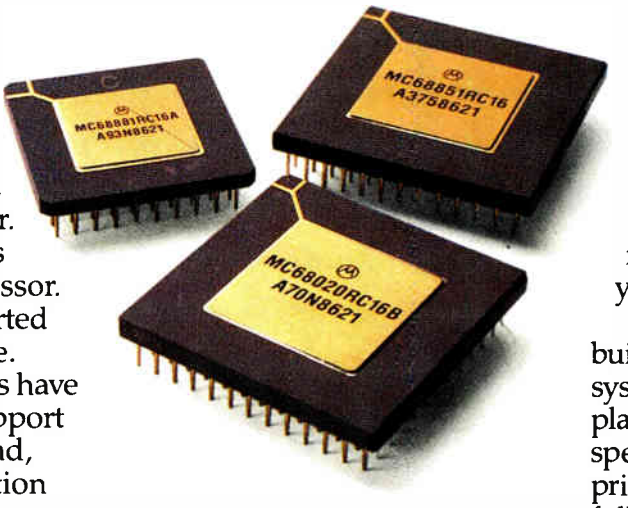
Put your chips on the software.



The best bet.

If you're betting your future on a 32-bit microprocessor-based system, you'd rather bet a winner. Today, the clear winner is the MC68020 microprocessor. It's faster. It's fully supported in hardware and software. It's backed by what others have called, "The strongest support team in the business." And, we're delivering production quantities. Now.

In fact, last year Motorola shipped over 50,000 units and this year we expect to ship more than a quarter of a million MC68020s.

Software support. Now.

When you choose the MC68020, you get the largest body of software available for 32-bit microprocessor-based machines. Operating systems. Languages. Tools and utilities. Host independent development systems. And, of course, applications. In fact, 80% of the microprocessor-based system designs running UNIX® OSs are based on M68000 Family chips.

The fastest just got faster.

At 25 MHz, the latest version of the MC68020 and its earlier 20 MHz version remain

The MC68020

the fastest general-purpose processors on the market today. And fully compatible. But speed alone isn't the answer. And for the generation beyond the MC68020, we're committed to higher performance devices while maintaining the M68000 Family software base.

Chips, boards or boxes.

Motorola is with you at every level. As the world's leader in VMEbus products, supplying MC68020-based VMEmodule™ and VMEsystem™ products, we can work with your development team at virtually every level, including technical training.

Betting the winner.

There's a lot of 32-bit talk in the press. Sampling quantities, blue sky and vaporware are fine, but maybe you'd rather not bet your company on them.

When you're planning to build the kind of leading-edge systems that win in the marketplace, Motorola offers you speed to market, aggressive pricing and the strength of a fully-realized 32-bit environment.

If you're an executive evaluating microprocessors, software and support, call us at 1-800-521-6274. We'll arrange a one-on-one management-level meeting. Fast. And we'll show you why a better microprocessor, coupled with here-and-now volume production, software and support, adds up to a winning combination.

MOTOROLA

WHY SCHWENGER LIKES HIS NEW JOB AT SIEMENS

MUNICH

There is a certain fascination for Rudolf Schwenger in his new job as worldwide sales and marketing manager for integrated circuits at Siemens AG's Components Group. "The fascination is the chance it offers to push the company from an underdog status to a world-class position—in certain segments," he says. At the same time, he does not have to worry about where the Munich company ranks overall among the world's IC suppliers.

In his strategy for Siemens's $400 million IC business, not only is world rank immaterial—Siemens is not even in the top 10—but Schwenger doesn't particularly want Siemens to build up strength in commodity parts. "What we must become is a specialist in specific fields and then excel in them," he declares.

By that he means communications and automotive and entertainment electronics. And with the ICs developed or envisioned for these industries, "we want to go worldwide, including the U. S. and Japan, and play a leading role," Schwenger says. "That's the goal for the next five years."

For all his efforts in the special-circuits field, the Siemens executive will not let the microprocessor and dynamic random-access memory areas slide. "We must have such devices to keep our factories busy and to serve as a base load for our sales organization," he says.

If Schwenger does not want Siemens to be known as a full-range commodity supplier, neither does he want it to become known as a niche-filler. The entire industries he wants to serve are more than just niches. Eventually, they will turn out to be substantial businesses.

Schwenger exudes the can-do spirit typical of Siemens executives during these days of confidence in their firm's technological prowess. He is certain the company will become a world competitor in specialty markets. Underlying his optimism is the expertise his company has gained with certain products. For example, Siemens already has sold tens of thousands of the chips recently introduced for integrated services digital networks [*Electronics*, Sept. 30, 1985, p. 46].

PUSHING ISDN. Siemens is now making a strong push with its ISDN chips in the U. S. Schwenger concedes that competing with such innovative companies as Intel Corp. and Advanced Micro Devices Inc. won't be easy. "And the moment of truth will come in two or three years, when the Japanese enter the scene with low-cost ISDN devices," he says. But by then, he thinks, his company will at least have its foot in the door and could be well established.

Schwenger also sees good chances in world markets for automotive ICs, a sector in which Siemens has acquired much know-how as a components supplier to German car-accessory makers. The company wants to put to use in devices for world markets the expertise it has gained with chips for such subsystems as antiskid systems and airbag safety equipment. It also plans a push with engine-management chips.

SCHWENGER: Aiming Siemens ICs at the communications, auto, and entertainment fields.

Also prominent in Schwenger's "noncommodity" IC strategy are chips for entertainment electronics. Here, Siemens plans a big effort in ICs that sharpen the picture of digital TV sets and add new features, such as teletext, to them. With such chips, Schwenger thinks Siemens can catch up with, and perhaps overtake within a few years, other semiconductor producers already active in digital TV.

The 46-year-old Schwenger brings just the right credentials to his new job. A graduate of Munich's Technical University with a master's degree in communications engineering, he joined Siemens in 1968 and has been active in ICs

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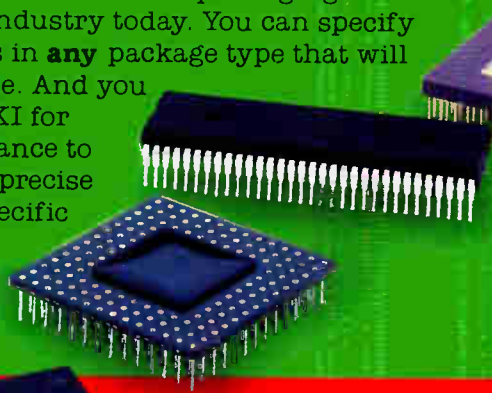

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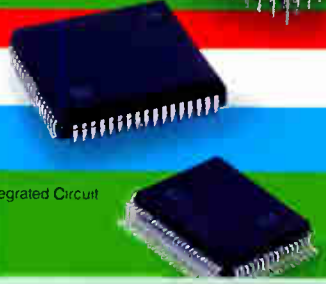

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ever since—in production, project management, development, and sales. He also spent five years in Singapore, building up and running a Siemens IC plant, before moving into his present post last spring.

Among Schwenger's hobbies is mountain climbing. "That makes you tough," he says. It also gives you a chance to think undisturbed, he adds, especially when you're waiting in a hut for the weather to clear.

One of Schwenger's thoughts is that Siemens has no choice but to keep making ICs. "That business is a technology engine enabling us to stay in Europe's league of successful semiconductor suppliers," he says. "We are determined to stand up to world competition and to make good in the market."–*John Gosch*

HOW TERADA IS PUSHING TELECOM R&D IN JAPAN

TOKYO

When Hiroaki Terada was an electronics engineering student more than 30 years ago, he recalls, "the only telecommunications switches we Japanese were building were on paper." Japan's switching technology still lags behind that of the U. S., but Terada says the gap is narrowing, and it could be closed a lot sooner than anyone thinks.

The 53-year-old Osaka University professor has specialized in switching-control-system design for more than 15 years. He recently led a government-backed joint project in which the university and four leading Japanese technology companies developed a new type of dual-pipeline microprocessor with telecommunications applications. The basic reason for the rapid advances Terada foresees in Japan's telecommunications switching technology is the liberalization of the country's telecommunications industry last year.

TERADA: NTT will still be strong, but now other manufacturers will develop more products faster.

"NTT [Nippon Telegraph & Telephone Corp.] is still a giant," he says, "but there is a new kind of dynamism in research." When NTT was a monopoly and controlled all telecommunications markets, its group of private suppliers, the so-called "NTT Family," had to follow its dictates in technical standards and product design. Now, with all the major Japanese makers competing not only in products but also in services ranging from value-added networks to satellite communications, they are freer to go their own way in the laboratories, too. Terada thinks that within 10 years, the Japanese will be building switches to rival those of Western leaders such as AT&T Co. and Northern Telecom.

NTT's laboratories will remain important in research, Terada predicts, acting as a stimulus to the major manufacturers. But he also believes that the biggest changes will be seen among those manufacturers. He says they will come up with new products and technologies more rapidly now that they're competing head-on with the former monopoly. And Terada believes NTT will continue to prosper as well, "because the major makers still will compete strongly to win NTT contracts, which means NTT can play them off against each other and keep production prices down."

A graduate of Ehime University in western Japan, with a doctorate in electronics engineering from Osaka University, Terada first worked under Prof. Zenichi Kitamura, who designed and built Japan's first transistorized switching system in 1957. In the mid-1970s, Terada worked on the design of control software for switching systems at Essex University in England, then moved on to the Centre National d'Etudes des Télécommunications in France, to work on distributed control architecture for use in French digital telecommunications systems.

At Osaka University, he has been working for more than a decade on what he calls an "elastic storage" concept. In the recent joint project, the concept was used to develop a so-called Q-p (queue-prototype) single-chip microprocessor. The Q-p splits processing functions into several autonomous subfunction units that are realized by an elastic queue structure. Terada also designed a data flow-through architecture to create an easily programmable one-chip microprocessor unit.

Terada spends a great deal of his time in offices and laboratories, but he has managed to get one of the best suntans in Japanese academia. "You can tell my hobby by looking at me," he says, smiling. "I love golf, even though I am only a duffer." He carries an 18 handicap.

–*Michael Berger*

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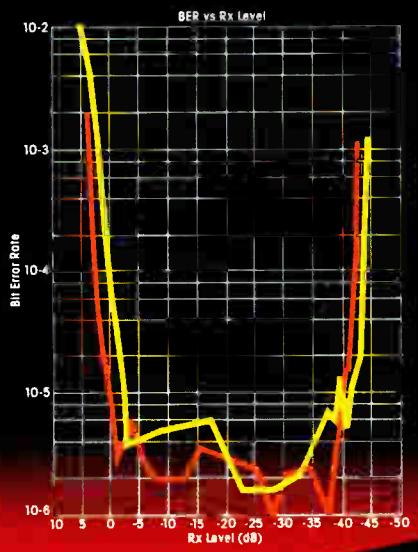

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ELECTRONICS NEWSLETTER

COMPAQ WILL INTRODUCE AN 80386-BASED MICROCOMPUTER THIS WEEK

In the race to get on the market first with a microcomputer using Intel Corp.'s powerful new 32-bit microprocessor, the 80386, Compaq Computer Corp. of Houston will announce its version this week in New York. Compaq's entry will be one of 20 to 30 80386-based machines introduced this year. It will run at 16 MHz, twice the speed of the IBM Corp. Personal Computer AT. It will likely run an enhanced version of Microsoft Corp.'s MS-DOS operating system and Xenix, Microsoft's Unix-like operating system. Microsoft is readying its next generation of MS-DOS, Version 5.0, which will support machines equipped with more than 640-K of random-access memory—including Compaq's 80386-based computer. Intel says MS-DOS 5.0 should be available late this year or early next. Though executives at both Microsoft and Compaq remain mum on the machine and its software, industry sources say the computer should retail for $6,000 to $9,000. □

GTE DOUBLES CAPACITY OF FIBER-OPTIC LINES

GTE Laboratories has taken a hatchet to the $50,000-per-20-km cost of fiber-optic lines by developing a division multiplexer that doubles each line's capacity. The device can simultaneously send two distinct light signals through a single cable and is usable with "virtually any terminal equipment," says Leslie Riseberg, director of GTE's electronics and phototonics lab in Waltham, Mass. What's more, he says, the technology could be applied to more than two channels. The multiplexer can distinguish between signals as close together as 14 nm; the channels it creates are independently tunable and can be retuned to adapt to laser fluctuations in the field. A field test is scheduled to begin later this year on the U. S. Sprint system. □

MITSUI WILL SPEND CHEAP DOLLARS TO BUY U. S. FIRMS—AND TECHNOLOGY

The Japanese are taking increasing advantage of the cheap dollar by buying into U. S. companies and thereby gaining access to new technology. No one is practicing that strategy more aggressively than Mitsui & Co., one of Tokyo's giant trading companies. It has formed a Los Angeles-based concern, Mitsui Comtek Corp., that will acquire companies marketing computers, semiconductors, and telecommunications equipment. It intends to obtain products or development data, manufacture offshore, and sell everywhere, including Japan. The new company, actually a subsidiary of Mitsui USA, which exports high-technology goods to Japan, expects $50 million in revenue its first year and $200 million within five years. □

AT LAST, A PRODUCT WILL INCORPORATE TI's VOICE-VERIFICATION ALGORITHM

It took 10 years to get the right price, and now a voice-verification system based on an algorithm that Texas Instruments Inc. developed for the Air Force will hit the commercial market this month when Voxtron Systems Inc. introduces its Veritron 1000 Voice Verification System. The New Braunfels, Texas, division of Detex Corp. says the security system analyzes a voice's spectral components and timing and matches them to a prerecorded template. If the voice does not match the template, Veritron denies entry. With its processing engine, a TI Business Pro computer with a 20-megabyte hard disk, it can control access at up to 16 doors or gates. Ten years ago, a system would have been powered by a VAX computer and cost $200,000; today's price is $40,000 to $50,000. Would-be entrants access the computer by telephone and respond to synthesized voice prompts. Five levels of security are possible. In field tests in which the system was used more than 10,000 times, Voxtron claims, it let not a single impostor in. □

ELECTRONICS NEWSLETTER

HUGHES DESIGNS ITS VHSIC CHIPS INTO ELECTRO-OPTICAL SIGNAL PROCESSOR

Add Hughes Aircraft Co. to the growing list of companies designing military systems with chips developed under Phase 1 of the Defense Department's Very High Speed Integrated Circuits program. Hughes's Electro-Optical and Data Systems Group in El Segundo, Calif., has inserted its VHSIC chips into a prototype programmable electro-optical signal processor. The unit is aimed at a variety of image-processing tasks that require different performance levels, so it uses a parallel-computing architecture that allows the easy addition of modules to increase speed. The new VHSIC chips boost throughput while cutting power, weight, and size—which keeps the processor small enough for airborne tasks, says the GM Hughes Electronics Corp. subsidiary. VHSICs from Honeywell, IBM, RCA, Texas Instruments, TRW, and others have already been used in equipment [*Electronics,* Dec. 16, 1985, p. 33]. □

WILL A NEW DATA-COMPRESSION SCHEME SPARK THE SLOW CD-ROM MARKET?

Some optical-memory makers are hoping that a new data-compression technique will spark an expansion of their slow-moving market for compact-disk read-only memories. The latest to toss its compression scheme into the ring is Reference Technology Inc. At this week's Federal Computer Conference in Washington, the Boulder, Colo., company will introduce a CD-ROM work station that is compatible with the IBM Corp. Personal Computer. The DocuStation, which includes a laser printer, has a special engine that builds up full images and text from disks containing compressed data that conforms to the International Telegraph and Telephone Consultative Committee's Group III and IV standards. DocuStation sells for less than $11,000, and DocuTrieve, the software controlling the CD-ROM access and information display, will cost $95 in single quantities. Reference Technology also provides a service, DocuCapture, that writes the data on the disks. □

NEC WINS 'GRAY-MARKET' CHIPS SUIT, STOPPING IMPORTS

Unlicensed third-party U. S. distributors of semiconductors purchased abroad have something new to worry about now that a U. S. district court has found that at least one such distributor infringed trademark laws. NEC Electronics Inc., a wholly owned U. S. subsidiary of the Japanese electronics giant, won a ruling late last month preventing Cal Circuit Abco of Woodland Hills, Calif., from importing and selling NEC parts purchased in Japan. The court ruled that NEC Electronics has exclusive ownership of the NEC trademark in the U. S. Cal Abco, which has been selling Japanese and U. S. parts for years, says it will appeal. It is also banking on an overhaul of the 50-year-old trademark law under a bill (S. 2614) now in the U. S. Senate. □

A COLOR COCKPIT DISPLAY THAT DOESN'T WASH OUT

Putting color displays in airplane and helicopter cockpits has befuddled designers, because they haven't been able to get their hands on tubes bright enough to shine through the glare at high altitudes. The problem is that when display makers try to boost brightness, the excessive heat from the brighter light source causes the image to distort. Now Bendix Flight Systems, the Teterboro, N. J., division of Allied Aerospace, and Tektronix Inc., the Beaverton, Ore., instrument maker, have designed a high-resolution CRT that uses a tension mask rather than the usual metal shadow mask; the metal mask bends when used with bright, hot light sources, distorting the image and muddying the color. By stretching a thin metal foil over a frame, like a drum skin, Tektronix built a taut mask that holds its shape—and therefore its focus. The result: tubes five times brighter than conventional displays. □

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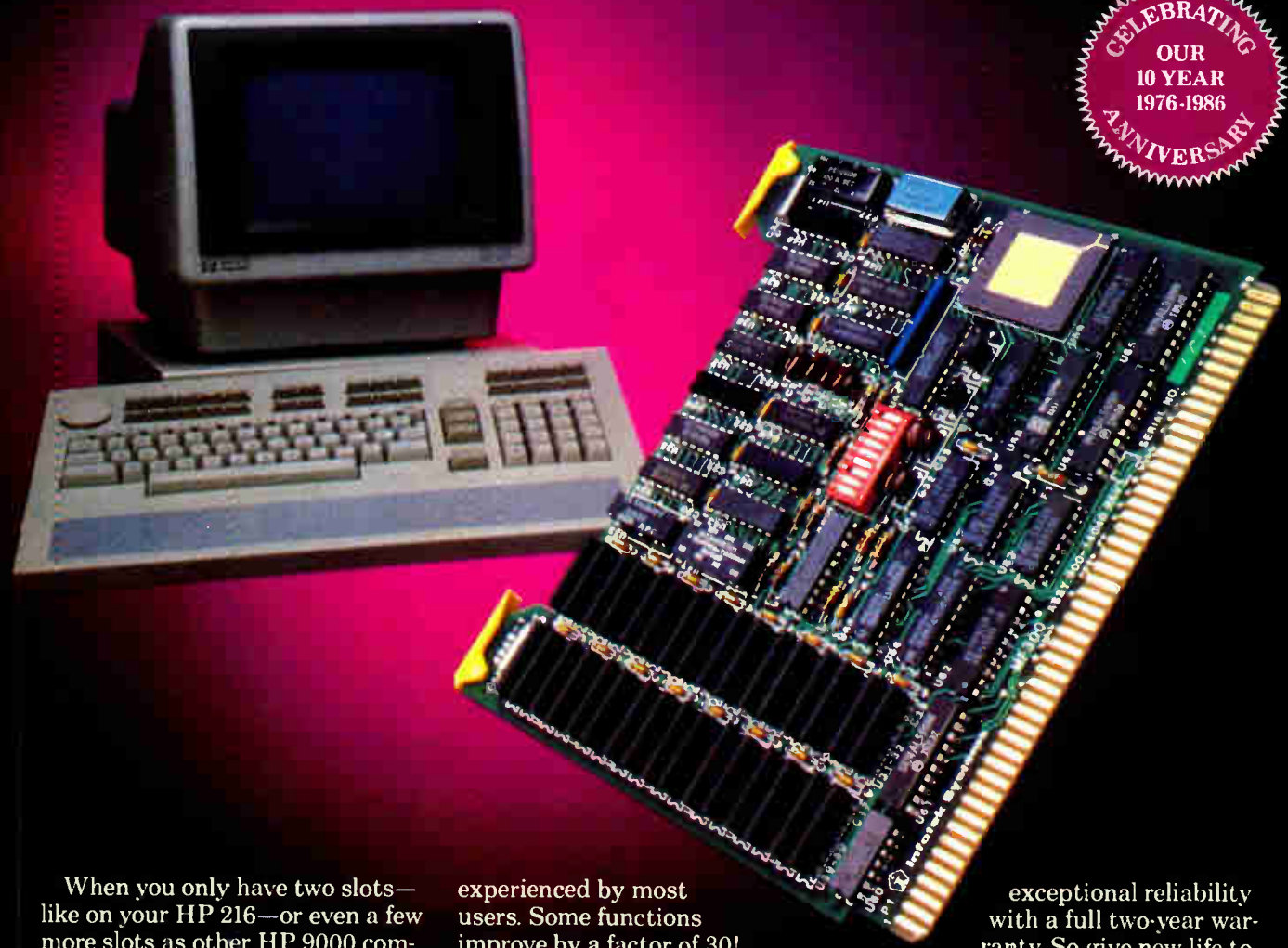

When you only have two slots—like on your HP 216—or even a few more slots as other HP 9000 computers do, you want the most capability in the least possible space. Now, you can have a full megabyte of memory plus an advanced floating point processor on a single card—the MF 300 from Infotek.

The MF 300 incorporates a powerful floating point processor (based on the Motorola 68881 processor) which significantly increases the speed of transcendental functions as well as arithmetic operations for both BASIC and Pascal. For math intensive applications such as CAD, improvements in speed of three to five times are experienced by most users. Some functions improve by a factor of 30!

The same performance (without the memory) is available in the new FP 881 floating point processor. Or you can choose the Infotek FP 210 floating point processor for BASIC and Pascal. The FP 210 employs the National 32081 processor to increase real arithmetic speed as well as transcendentals. And all floating point boards further enhance real math functions when used with Infotek's BASIC compilers.

As with all Infotek HP enhancement products, the floating point processors demonstrate their exceptional reliability with a full two-year warranty. So give new life to your HP 216 or other 9000 computer! Put maximum performance in a single slot. Call Infotek Systems at (800) 227-0218, in California (800) 523-1682, or (714) 956-9300, 1400 North Baxter Street, Anaheim, California 92806-1201, TELEX 182283.

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PRODUCTS NEWSLETTER

RAM-BASED STORAGE SYSTEM SPEEDS NETWORK-ACCESS PERFORMANCE

Santa Clara Systems is delivering a storage system for the IBM Corp. Personal Computer line that's based on battery-backed RAMs, has a capacity of 4 to 20 megabytes, and boasts processing speeds as much as 700% faster than conventional PC storage. According to the Santa Clara, Calif., maker of networking products, the Batram system is designed to be used as a file server and will greatly improve network performance: it can transfer data at 3.7 megabytes/s, compared with the 5-megabit/s transfer rate of a hard-disk drive. The 4-megabyte-storage version sells for $1,895. □

SUPERTEX COMBINES THE BEST OF BIPOLAR AND POWER MOS FETS

Supertex is bringing to market a power transistor that combines the best features of power MOS FETs and bipolar power FETs. Called the bipolar enhanced FET, or Benfet, the monolithic chip is an array of eight FETs on a 36-by-93-mil-wide die. Each FET has an input capacitance of only 5 pF and an output drive capability of 200 mA and 300 V. The lateral structure retains bipolar's low on-resistance rating—eight times lower than that of MOS FETs—but with the high voltage and fast switching speeds of MOS FETs. The Sunnyvale, Calif., company is completing plans for a January 1987 introduction of a family of n- and p-channel Benfet arrays; prices have not yet been set, but they will be about 40% less than those of comparable MOS FETs. □

PC/XT COMPATIBLE BOWS FOR JUST $699

Another IBM PC/XT-compatible has hit the market, and it's priced at only $699. Blue Chip Electronics Inc.'s new machine is equipped with one floppy-disk drive, where the $2,000 PC/XT has one floppy- and one hard-disk drive. The 8088-based Blue Chip Computer comes with 512-K bytes of RAM, a parallel port, and a 12-in. monochrome monitor. Memory can be expanded to 640-K bytes, and a 14-in. color monitor and a second floppy-disk drive are available as options. Deliveries from the Chandler, Ariz., subsidiary of Korea's Hyundai will begin this month. □

LANCORE UNVEILS FAULT-TOLERANT NETWORK SERVER

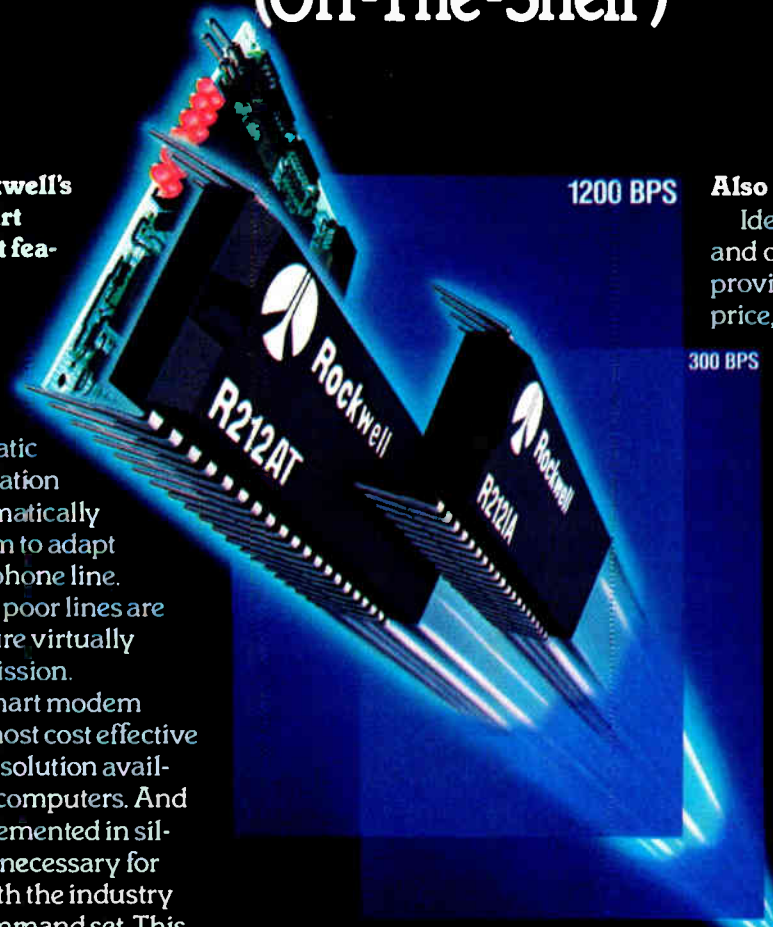
Fault tolerance is coming to local-area networks. The Core 75 FT server from Lancore Technologies Inc. features system firmware that improves data security and provides fault tolerance by mirroring the disk—duplicating the data on a secondary drive. One of the dual 75-megabyte disk drives is mounted in the main system unit along with its power supply, and the slave disk drive is enclosed in a cabinet with its own power supply. In addition, the server has a 60-megabyte streaming-tape drive or an optional 400-megabyte optical-storage device. Priced at $12,235, the server is available immediately from the Westlake Village, Calif., company. It works with most popular network operating systems. □

TEXET GOES TO SUN WORK STATION FOR ELECTRONIC-PUBLISHING SYSTEM

Texet Corp. will shift away from proprietary hardware in its electronic-publishing product line by introducing a new system based on a popular work station from Sun Microsystems Inc. The Arlington, Mass., company's LP 3300 system has a controller with an attached production work station, 4 megabytes of main memory, and a 330- or 660-megabyte hard disk. Each base system can support three additional diskless production work stations. Base systems are priced at around $100,000, with additional work-station nodes starting at $30,000. Texet is shipping systems now. □

ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 1200 BPS AT 300 BPS PRICES.

(Off-The-Shelf)



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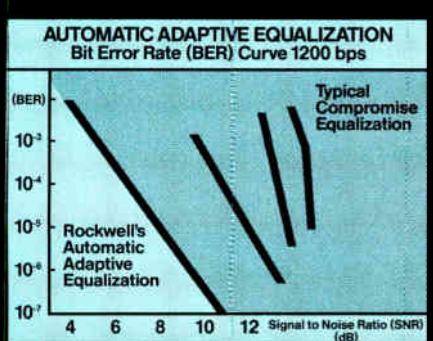
The R212AT smart modem offers lower system cost because it incorporates the controller and analog filter circuitry required for modem communications in the device set itself. This reduces parts count, enhances total system reliability and meets low power requirements for portable applications.

As well as operating asynchronously, the R212AT has synchronous mode operation for higher transmission throughput.



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The R212DP, like the R212AT, has automatic fall back to slower speeds and an RS232C interface. Both these Bell 212A and 103 compatible device sets are available at any level of integration from devices to boards or customized private label systems.

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Electronics

DOD SPURS VHSIC EFFORTS WITH 'ADVANCE AGREEMENTS'

NONCOMPETITIVE PACTS WILL PUMP MILLIONS INTO IC PRODUCTION

MELBOURNE, FLA.

The managers of the Defense Department's Very High Speed Integrated Circuits program are taking an unusual step to speed up production of devices designed according to VHSIC criteria. They have signed "advance agreements" with a number of the VHSIC suppliers—agreements that will pump many millions of dollars into chip production efforts.

The advantage of the agreements, from the government's point of view, is that they are not considered contracts. Therefore, they do not have to be opened up to competitive bidding. The agreements are signed after detailed negotiations, during which both sides agree, for example, on how much a contractor will be reimbursed for his overhead during device development. Essentially, the agreements are an accounting device. Besides avoiding the bidding process, they are said to help control costs for the work they cover.

Details about the agreements—which suppliers they are being offered to, and how those companies were chosen—are not clear.

Most VHSIC contractors say for the record they have not been informed about the agreements and are puzzled as to what they mean. For example, Dallas Burns, director of the Honeywell Inc. VHSIC program, says: "We are not yet familiar enough with details and prefer not to comment at this time."

But several contractor officials say, not for attribution, that the only interpretation is that the directors of the VHSIC program are trying to beef up a device production capability that is perceived to be lagging. "We would be in better shape with more money like that, too," adds one executive.

One of the two companies known to have signed an advance agreement is Harris Corp., Melbourne, Fla. Its Government Systems Sector has a contract to supply devices under VHSIC Phase 1, but lost out in the competition for Phase 2 contracts. Oddly enough, though, the $46.5 million that the Harris operation will get through 1990 under the advance agreement will be used to help it develop a Phase 2 chip production line.

Harris last month announced the signing of its agreement, making its case all the more unusual—again unlike contracts, the agreements are seldom made public. Harris, in fact, was the first company to reveal that it had one for VHSIC work. The other advance agreement that has come to light is with IBM Corp.'s Federal Systems Division, Manassas, Va. The company is a contractor for VHSIC Phases 1 and 2, and was the only Phase 1 contractor to deliver chips on schedule.

So far, the VHSIC program office has nothing to say about the Harris agreement, other than that E. D. (Sonny) Maynard Jr., the office's director, took an active part in the process of qualifying the company for it. Maynard was away on a personal emergency leave last week and not available for comment.

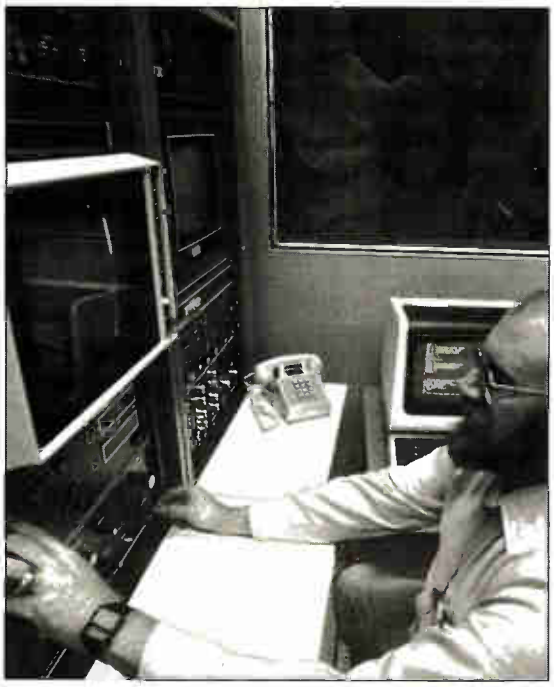
A VHSIC program spokeswoman noted, however, that financial support for this agreement will not be charged to VHSIC, since funds for such agreements come from a DOD-wide pool, rather than specific programs. She also confirmed industry reports that IBM's Federal Systems Division holds an advance agreement as well. The agreement covers engineering support to bring out the VHSIC line, according to an IBM spokesman who declined to elaborate further.

MORE COMING. Similar pacts with other companies doing VHSIC work are either signed or in the works, according to industry reports. The VHSIC office offers no comment on these.

The Harris agreement comes as something of a surprise to VHSIC contractors and observers of the research program for advanced military devices, who generally have regarded the Phase 2 lineup as frozen since it was chosen two years ago [*Electronics Week*, Nov. 12, 1984, p. 20]. Nevertheless, Harris says it will use the money from the agreement to help support its development of a 0.5-μm, 100-MHz, Phase 2 fabrication line for radiation-hardened CMOS devices.

"This definitely is a new wrinkle for VHSIC," says Robert N. Castellano, a San Francisco-based integrated circuit consultant and analyst who recently wrote a report that presents a comprehensive look at the program. But a DOD effort to bring in additional production muscle for VHSIC from a proven semiconductor house appears logical to him, since it addresses a weakness that Castellano says is growing ever more apparent.

"The problem is a shortage of actual chips," says Castellano. Although Phase 1 of VHSIC, which officially ran from 1981 to 1984, stayed fairly close to schedule in designing the 1.25-μm chips, contractors have fallen much further behind in producing working prototype devices so designers of military systems can experiment with them. Castellano says delivery from



BENEFICIARY. DOD is encouraging Harris's VHSIC program, which aims to produce 0.5-μm ICs in this facility.

all contractors was due in 1984 and estimates the lag averages about 18 months and is widening. Texas Instruments Inc., for example, late last month said it has delivered the first operational set of its Phase 1 chips.

The next step in Phase 1, which is to extend over several years, aims to make chips available in quantity, and this looks increasingly shaky, according to contractor sources involved in the program. Potential users especially are "worrying about betting on something they don't have in hand," observes an executive at a Phase 1 contractor who declines to be identified.

For its part, Harris regards the agreement as an important stepping stone that "allows us to design our own line of Phase 2 ASIC devices," according to Lee R. Allain, vice president of VHSIC operations. The significance of the agreement, in his opinion, is that "it brings more capacity and more components to VHSIC."

Harris, a member of the Westinghouse Corp. Phase 1 team that lost out in its bid for a Phase 2 contract, is highly regarded in the industry for its expertise in building militarized rad-hard chips. It presently is entering the prototype phase with its own VHSIC chip intended for high-performance space computers. *–Larry Waller*

SEMICONDUCTORS

NEW MEMORY-CELL DESIGN MAY LOWER EPLD COSTS

KAWASAKI, JAPAN

A new memory-cell configuration from Toshiba Corp. shows promise of driving down the cost of ultraviolet-erasable programmable logic devices. Based on a single-polysilicon-layer gate design, it will be used in the erasable programmable read-only-memory cells. It will replace on the EPLDs the dual-poly cell configuration used in EPROMs.

The cell should make it easier to produce inexpensively the user-programmable and reprogrammable logic devices needed for turning out systems quickly or in quantities too low to justify semicustom production, says Kuniyoshi Yoshikawa, senior researcher at the company's Semiconductor Device Engineering Laboratory in Kawasaki.

ADVANTAGES. The single-poly technique holds a number of advantages over the dual-poly-gate configuration used in several generations of commodity n-MOS and CMOS EPROMs, although it does exact a substantial real-estate penalty. The cell is compatible with the processing used in CMOS logic devices, says Yoshikawa. And it's faster, cheaper, more reliable, and easier to fabricate than the dual-poly structures.

Despite its complexity, the dual-poly method is practical for commodity production of dedicated EPROM chips, which come in limited varieties. Design costs are amortized over the large numbers of chips built, and economies of scale prevail during production.

But that same complexity makes dual-poly gates impractical in most types of logic circuits, which come in innumerable varieties and in much smaller quantities. Moreover, rapid turnaround time for new types of logic or processor designs is extremely important.

Toshiba has no firm production schedule set for the new cell type. But chances are that when the company does go into production, competitors will not be far behind. Roger Cuppens of Philips International NV proposed a similar structure for EEPROMs in 1984. And researchers at WaferScale Integration Inc., Fremont, Calif., set forth such a design for EPROMs independently of Toshiba at the Custom Integrated Circuits Conference in Rochester, N. Y., last May.

Toshiba's memory cell bears some design similarities to the standard stacked-gate EPROM. To store data, for example, it utilizes stored charge in a floating gate embedded in silicon dioxide overlying a transistor channel. As in the stacked-gate EPROM, the floating gate is programmed by voltage capacitively coupled from a control gate. Hot electrons generated near the drain by impact ionization tunnel into the floating gate of cells to which programming voltage is applied.

But unlike the usual stacked-gate EPROM, the control gate in the new cell is an n^+ diffused layer in the substrate rather than an insulated gate. Moreover, it is laterally isolated from the channel of the cell transistor both physically and electrically (see diagram). The floating gate extends over the control gate to obtain capacitive coupling.

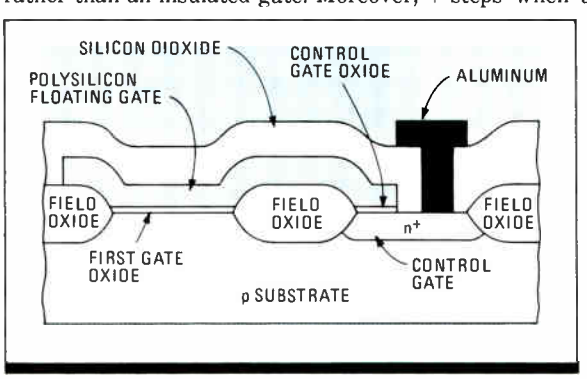
The new cell type makes for better reliability and a better match with logic-fabrication processes than the standard design. But the tradeoff is a larger cell, because of the need for an additional field-oxide isolation area and the control gate. For cells designed with 1.2-μm design rules and 20-nm-thick gate oxide, cell size is about 50 μm^2, compared with 20 μm^2 for the stacked design.

LESSER PENALTY. Yoshikawa points out, however, that this real-estate penalty is much less damaging than it might appear. A logic array will usually have 10,000 to 20,000 gates rather than the 256-K bits or more of a memory device, and only a small portion of the gates need be reconfigurable. In microprocessors and similar systems, only a tiny portion of the total number of transistors will require the reprogramming capability.

The oxide between the control gate and the floating gate is thermally grown bulk silicon oxide, which makes for better data retention. In the stacked-gate cell, the oxide between the gates must be thermally grown polysilicon oxide, which is more prone to leakage. In the new cell, there is no leakage at voltages below the breakdown voltage of the control gate, which is designed to provide a healthy margin above programming voltage of 12.5 V. Erasing is about 2.8 times faster than it is for the stacked-gate design, because the floating-gate peripheral length in proximity with the n^+ layer is longer.

Starting with a conventional n-well CMOS process, Toshiba required only one additional mask to define the control-gate region and one extra ion implantation for fabrication of the prototype erasable programmable device. The floating-gate oxide and control-gate oxide are grown simultaneously. In actual production, it may be possible to fabricate the control gate during the process steps when a depletion transistor gate implant or n-well implant are formed, eliminating the need for the extra mask and process steps.

After completing reliability tests, the company will allocate resources for production of chips using the cell. The next task for Yoshikawa, and researchers Seiichi Mori and Norihisa Arai is to convince company executives the process is ready for production. *–Charles L. Cohen*



SINGLE POLY. Toshiba's EPROM cell laterally isolates the control gate from the cell transistor physically and electrically.

CAN DOD COEXIST WITH OPEN SYSTEMS?

MONTEREY, CALIF.

The Defense Department has been wrestling for years with merging open systems interconnection protocols with its widely used Transmission Control Protocol/Internet Protocol [*Electronics*, May 13, 1985, p. 34]. The individual services want OSI as soon as possible, but the DOD says it could take seven years to replace TCP/IP.

To make the transition gracefully, the DOD is forging a coexistence plan, the first step of which is applications-translation software. Later, the National Bureau of Standards, under a contract from the Defense Communications Agency, will develop internet gateways that will "unwrap" datagrams to see whether they belong to DOD or OSI systems. It will also develop terminal access devices that will log on to either kind of system. Meanwhile, the NBS has set up a group to develop OSI specifications for use by federal agencies.

PRIORITY FOR MAIL. A series of OSI/DOD gateways will begin to take shape next month when the NBS network-applications group obtains a processor to support both protocol sets and on which it can run translations of network-applications software. The first translation will be for electronic mail, enabling transmissions between X.400 OSI networks and DOD networks that use the Simple Mail Transmission Protocol.

X.400 will be first for two reasons, says group manager Jerry Mulvenna: it's the most widely implemented OSI application, and the translation will be the easiest. The X.400/SMTP software will probably be available by late next year, Mulvenna said last week at a TCP/IP seminar in Monterey. Next will come a translation between DOD's File Transfer Protocol (FTP) and the OSI File Transfer Access Method (FTAM); and following that a link between DOD's Telnet and OSI's Virtual Terminal Protocol.

FTAM to FTP translation, which would give users access to each other's network files, may be ready six months after the mail software is finished, says Martin A. Thompson, assistant director for interoperability and standards for the Defense Communications Agency.

However, virtual-terminal software, which would let users log on to each other's networks, is probably a long way off. The International Organization for Standardization has not yet fully specified the OSI protocol.

And when it is specified, the protocols will still have to be turned into products. The newly formed Corporation for Open Systems, a consortium of computer and networking companies who want to speed development of OSI and the integrated services digital network, is only beginning to staff up.

GATEMAN. An electronic-mail link between OSI and DOD nets will be first, says the NBS's Mulvenna.

In contrast, TCP/IP, which was first implemented on the Arpanet [*Electronics*, May 5, 1983, p. 61], has been finding increasing use in industry. The DOD will support further development of the TCP/IP and invariably specifies it in procurements. Also written into the popular Berkeley 4.2bsd Unix operating system, TCP/IP is becoming the communications protocol of choice in the absence of OSI products.

It was precisely because TCP/IP is finding its way into so many commercial systems—while OSI struggles to be born—that last week's seminar was held. Sponsored by the Defense Advanced Research Projects Agency, it brought together representatives of more than 100 commercial developers of TCP/IP with DOD users and the old Arpanet hands who have been writing the protocols for over a decade.

Vendors who turn to TCP/IP find that its roots in the research community have produced a protocol set that is as much a philosophy as it is a protocol. "Vendors are in the dark," says Daniel I. Lynch, who is the president of Advanced Computing Environments, Cupertino, Calif. "They're faced with a de facto standard that exists only as a collection of papers on the Arpanet."

At Monterey, attendees debated whether methods of testing and certifying TCP/IP equipment should be developed—and if so, who should do it. They also learned of new Internet protocols being investigated by the Internet Activities Board, an informal research group with private-sector and government members. Its task forces are working on applications, end-to-end services, architecture, engineering, privacy,

WAYS OF CUTTING AM SKYWAVE SIGNALS TO BE TESTED

An experimental AM antenna project organized by the National Association of Broadcasters could lead to the first major improvements in the technology in more than 50 years.

The project, which will be discussed at the NAB's Radio '86 conference in New Orleans next week, will focus on new broadcast antenna designs that aim to boost signal strength by pumping more radiated energy into the groundwave signal while reducing the amount of energy radiated into a skywave.

Current AM antennas rely on vertical towers, which generally focus only about 15% of radiated energy into a groundwave signal that AM receivers can pick up. The remaining 85% travels outward and upward into a skywave. These skywave signals cause particular problems at night, when they can bounce off the ionosphere and produce interference hundreds or even thousands of miles away from the source.

To attack the problem, the NAB will construct towers based on two experimental designs at leased sites in Leesburg, Va., and in Beltsville, Md.

At the Leesburg site, the NAB will try out a design developed by Richard Biby of Communications Engineering Services, Arlington, Va. It's based on a round electric screen and a number of short, vertical radiators deployed around the base of a conventional vertical, monopole antenna.

When properly tuned, these elements are expected to increase the strength of the monopole groundwave signal. They will also radiate skywaves that can cancel out much of the monopole's skyward radiation.

In Beltsville, the association will set up an antenna designed by Ogden Prestholdt of A. D. Ring & Associates, Washington. That design relies on a combination of vertical, horizontal, and diagonal antenna elements that should improve separate control over groundwave and skywave radiation.

Before building the towers, the NAB must obtain approval from the Federal Communications Commission, the Federal Aviation Administration, and local zoning boards, says Michael C. Rau, the NAB engineer in charge of the project. Then will come a one-year construction period, followed by one year of field tests. *–Wesley R. Iversen*

scientific computing, and testing.

The NBS has also set up the interagency Government OSI Users Committee, to develop a federal specification for product procurement. The group was formed in anticipation of a policy recently developed, but as yet unissued, by the Office of Management and Budget, which would mandate use of OSI products on a government-wide basis, says John Heafner, chief of the NBS Systems and Network Architecture division.

The committee will attack the problem in two phases, says Heafner. In the first, the group will define and adopt OSI protocols that have already been defined for the commercial world by the NBS/OSI Implementers Workshop. This group is made up of vendors and users of commercial OSI equipment.

In phase two, the committee will identify protocols needed by the government that are not yet part of OSI, and will work with the ISO and the International Telegraph and Telephone Consultative Committee to get them developed.

The Government OSI Users Committee will hold its first meeting only this month, however, and does not have a target date for completing the job. In the meantime, DOD expects entire user communities to stick with either TCP/IP or OSI protocols, and to communicate via the gateways. *–Clifford Barney*

INDUSTRIAL

WITH CARRIER-BAND CHIPS, MAP WILL SOON COST LESS

CHICAGO

A major step toward making the Manufacturing Automation Protocol cost-competitive with proprietary networking schemes may be taken before the end of the year. The first single-chip carrier-band modems designed to implement the MAP specification are about to appear, promising a new thrust for those hoping to make MAP the standard in multivendor factory networking.

Motorola Inc. is poised to enter the market first, with its MAP-compatible MC68194 carrier-band modem chip. It fabricated initial working versions about two weeks ago. Sample devices will be ready by December, says James F. Vittera, a strategic marketing manager for the company's Semiconductor Products Sector in Phoenix, Ariz.

But it looks as if other chip makers won't be far behind. West Germany's Siemens AG, for example, is developing a single-chip carrier-band modem device to be known as the SAB82511. The Munich company declines to say when the chip will be available, but some industry sources believe samples could be ready by the second quarter of next year.

Intel Corp. plans a similar chip for its MAP product line. No date has been set for introduction, says Adi Golbert, senior applications engineer for Intel's Data Communications Component Operation in Folsom, Calif.

The early availability of carrier-band chips—which are designed to replace the board-level circuit implementations now being used in carrier-band modems—is of vital interest to General Motors Corp. and other major backers of MAP. Though testing has focused on broadband implementations so far, the carrier-band portion of the proposed MAP architectures will do the most to hold down costs, according to MAP proponents. "We're expecting multiple vendors [of carrier-band products], and we'd like to see the chips get out there and knock the price down," says Michael F. Bukowski, an Advanced Engineering Staff project engineer at the GM Technical Center, Warren, Mich.

MAP is based on the seven-layer open-systems interconnection reference model developed by the International Organization for Standardization. GM and others assume that factory networks based on MAP will use a broadband-network backbone for factory-wide communication, but will rely on attached carrier-band subnets for cell-level control [*Electronics*, Nov. 11, 1985, p. 16]. The less expensive carrier-band technology is crucial to this scheme; without it, additional broadband network hardware must be used, and costs climb.

SIMPLER APPROACH. The carrier-band subnets use phase-coherent frequency-shift-keyed modulation for sending messages with only a single pair of frequencies. This approach is much simpler and thus potentially less expensive than the broadband technique, which requires radio-frequency components and other complex circuitry for sending modulated signals over numerous channels.

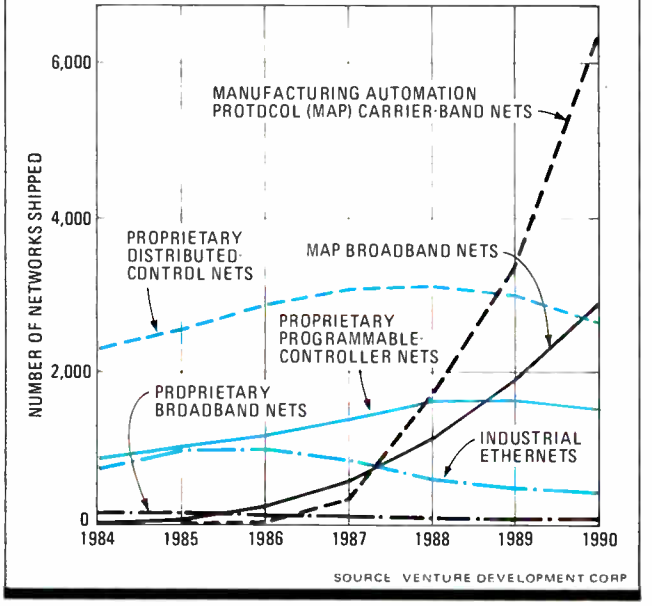
Besides being cheaper, carrier-band subnets are more flexible than broadband, says GM's Bukowski. "With carrier-band, plant maintenance personnel will be able to set up an application, modify it, take it down, and move it around," something that's not feasible with broadband, he says. What's more, some observers believe that for MAP to be practical in the process industries a carrier-band approach may be necessary to achieve performance adequate for time-critical process-control jobs.

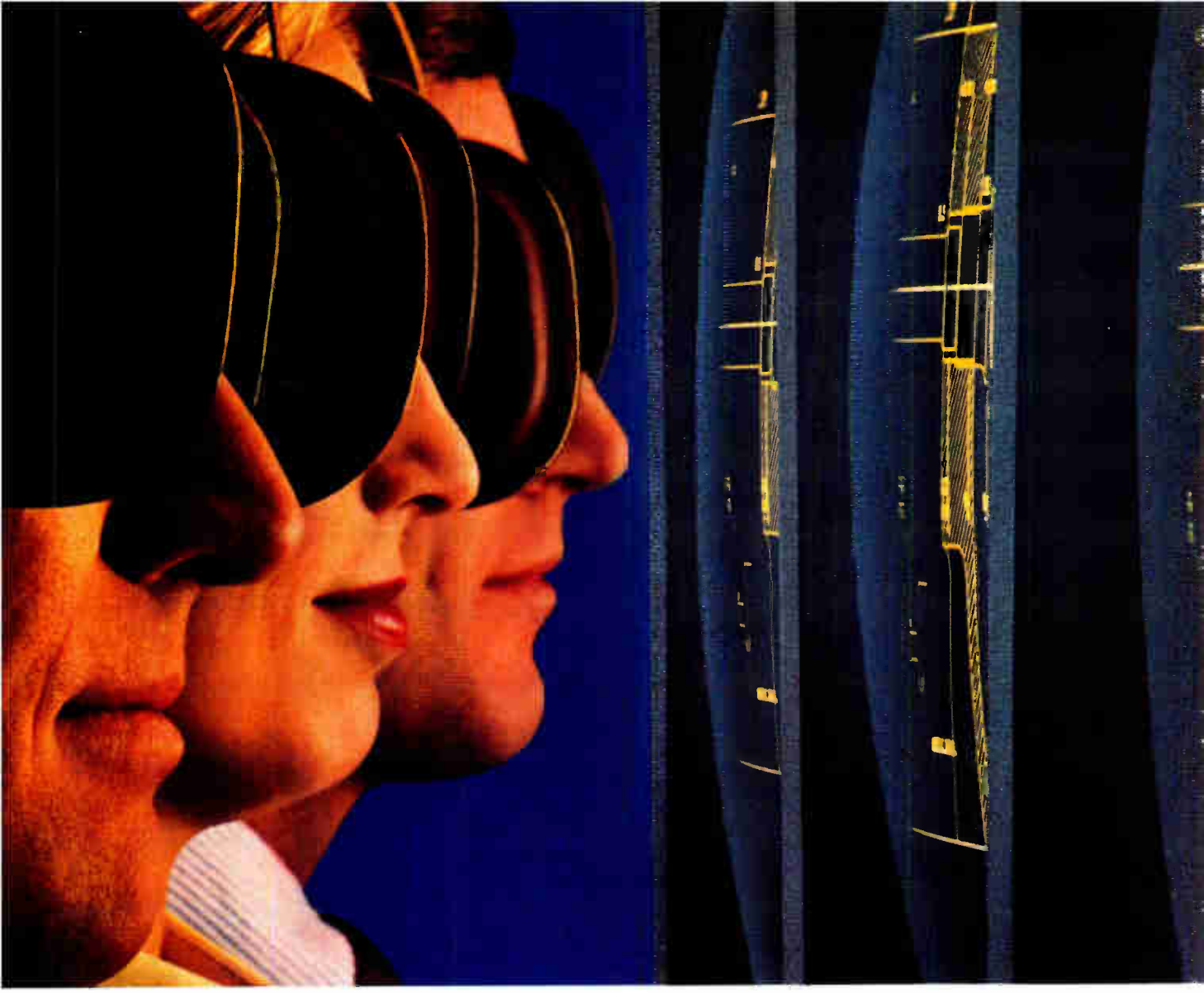
Besides about 10 pilot broadband MAP networks that GM is testing at various factory sites, the automaker early this year began limited carrier-band MAP tests in its Oshawa, Ont., plant, says Michael A. Kaminski, MAP program manager. He adds that GM is planning to install its first pilot production carrier-band MAP subnets in another plant next spring, with two more plants set to come on line next summer.

Tests are also planned by the Industrial Technology Institute, Ann Arbor, Mich. By the end of the year, the nonprofit corporation will begin a conformance-testing service for MAP carrier-band products, similar to the broadband MAP testing service it already offers, says Andrew McMillan, manager of the ITI Network Evaluation and Test Center.

Given the cost, flexibility, and real-time control advantages, most observers expect the number of carrier-band nets sold for MAP applications will eventually outstrip the number of broadband nets. Venture Development Corp., a Natick, Mass., market research firm, projects that sales will ramp up quickly beginning next year (see chart) and pass the 6,000 mark by 1990. That figure compares to fewer than 3,000 broadband nets.

CARRIER-BAND NETS TO OUTSTRIP BROADBAND TYPES





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Although carrier-band networks may come to represent the largest unit-volume market for MAP chip and equipment vendors, the business will fall short of broadband in terms of dollar volume. Venture Development, for one, projects the average MAP selling price per node by 1990 at $1,860 for broadband and $1,375 for carrier-band.

Many industry watchers believe the difference could be even greater. In fact, some say, if MAP is to predominate in the factory, carrier-band connection costs must approach parity with the price of today's proprietary nets. "Users are looking for Ethernet-type connect costs, in the $300-to-$600 [per node] range," observes Motorola's Vittera. "Because the silicon in carrier-band MAP is very similar to [that in] Ethernet, there's no reason why the price couldn't be about the same."

The big question: will carrier-band nodes drop to $600 or less?

So far, with no single-chip devices available, MAP carrier-band modems have been based on board-level circuit implementations. Modems made this way are available for about $700 from such companies as Concord Data Systems, Waltham, Mass., and the Ridgefield, Conn., Computrol division of Kidde Automated Systems Inc. Both can replace a broadband modem in working with a separate MAP controller board, which handles layers 2 through 7 of the MAP token-passing protocol drawn from the IEEE-802.4 standard.

The arrival of single-chip carrier-band modems will allow makers to cut modem prices significantly. At Motorola, Vittera says the 68194 large-scale-integrated chip, which is fabricated in a 3-μm emitter-coupled-logic process, will be packaged in a 44-pin plastic-leaded chip carrier and will be priced initially at around $30 to $35 apiece. But within a couple of years, he says, volume pricing should bring that figure down to between $10 and $15.

Besides selling the chip for use by original-equipment manufacturers, Motorola is also planning a carrier-band product as part of its systems-level MAP line. This unit will integrate the carrier-band modem chip and associated devices on a single board with the MAP token-bus control circuitry. Planned for introduction late next year, it is expected to sell initially at about $1,000 to $1,200, Vittera says. But with volume, the price could eventually drop to around $500, with the modem accounting for $100 to $150 of the total, Vittera predicts. *–Wesley R. Iversen*

IC TESTING

ATE MAKERS EYE ISDN AS NEW MARKET

BOSTON

Battered by the overall industry slump, vendors of automatic test equipment are taking increased notice of the market for ISDN hardware as a growth area. Though complete standards are still two years off and the integrated services digital network business is far from booming now, ATE vendors see a large and growing market coming within reach.

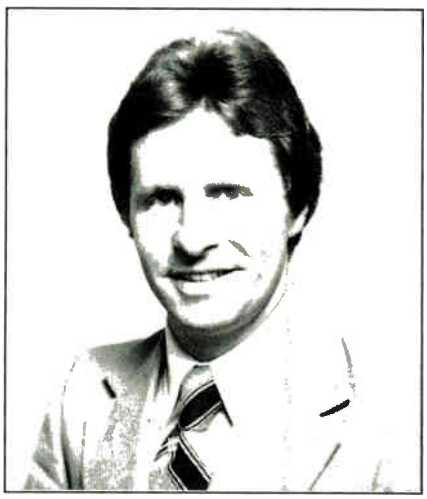
The optimism arises from the production of ISDN chips, the scheduling of field trials, and the generation of specifications by Bell Communications Research [*Electronics*, Aug. 21, 1986, p. 57]. A panel discussion scheduled for the Sept. 8-12 International Test Conference in Washington will examine what this activity means for the test industry.

LTX Corp. of Westwood, Mass., was among the first test-equipment builders to aggressively target the telecommunications market and now it holds a leading share. Now LTX is among those pressing hard to capture ISDN device-test business. Paul Scrivens, vice president of the linear business unit at LTX, describes the market as "embryonic," pegging it at about $100 million for last year. Business for the current year, he adds, will probably be down. "I don't expect it to come back until 1988, when the [additional] standards are set," says Scrivens. But within five years, he believes, the ISDN test market will double.

In the past, telecommunications had been mostly an industry closed to test-equipment vendors. AT&T Co. and other major telecommunications companies developed most test equipment themselves. For example, Northern Telecom Ltd.'s Bell-Northern Research unit, Ottawa, Canada, recently announced a system for testing ISDN products and analyzing protocols. Such companies have considered the ATE firms' testers inferior.

But ATE manufacturers have caught up with and surpassed the communications industry in test-equipment technology, Scrivens claims. For example, ATE vendors introduced computer buses into test equipment, replacing IEEE buses, and initiated the use of digital signal processing. Now, Scrivens says, "every time there's a technical change, we get a little more of the market." With the technical gap closing and AT&T broken up, there is "very little possibility of test-equipment companies getting locked out of the market," he says.

Mixed-signal ISDN devices present problems of overall synchronization between the analog and digital aspects of the devices and the test system, as well as event control—the synchronization of inputs with outputs, ATE makers say. An additional demand comes from chip makers, who are struggling to shorten time-to-market cycles. "Semiconductor makers have told us it's taking two to three years" to get devices to market, says Randy Kramer, communications applications manager at Teradyne Inc. of Boston.



SCRIVENS: ISDN test-system market will not take off until 1988, says LTX executive.

Responding to the semiconductor makers, ATE makers say life with ISDN could be easier if chip makers provided for bit-error-rate testing in the receiver circuit, says Kramer. Test channels or pins and loop-back modes for receivers and transmitters internal to the devices would also be helpful, he adds.

Because ISDN devices have both digital and linear characteristics, the question of single-socket versus multiple-socket testing also arises. "You can't afford to buy a very large-scale-integration tester and a linear tester," says Richard Mullen, Teradyne's product marketing manager for the communications market. So "the problem is how you maintain a high level of quality and [adherence] to specifications at the test head with both analog and digital" capabilities. Mullen predicts ATE vendors will provide integrated testers to satisfy this need by 1988. *–Craig D. Rose*

IMAGING

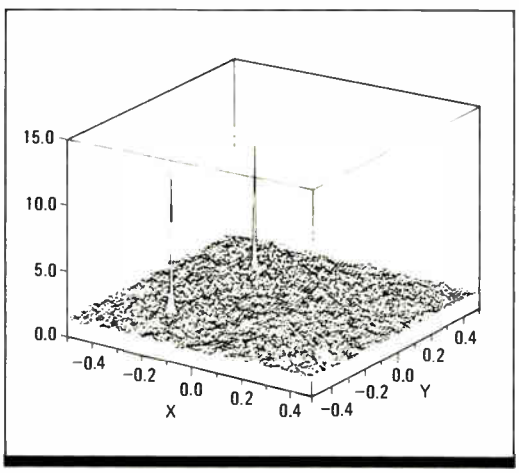
HOLOGRAPHIC FILTER SPOTS IMAGES FROM ANY ANGLE

LIVERMORE, CALIF.

Researchers at Sandia National Laboratories have developed a pattern-recognition method that could be used to improve machine-vision systems. Using a holographic filter, the new system can detect two-dimensional images regardless of position, rotation, or intensity. When rotated, the holographic filter reveals target images as points of constant amplitude in a Fourier image while points corresponding to all other images are fluctuating in value.

Existing optical methods of pattern recognition employ correlation filters that produce maximum response when the input image closely matches the stored pattern. However, such filters do not take into account parametric distortions such as rotation, intensity, or perspective. They recognize only the information that is invariant under these distortions, and such invariant information frequently matches images other than the target.

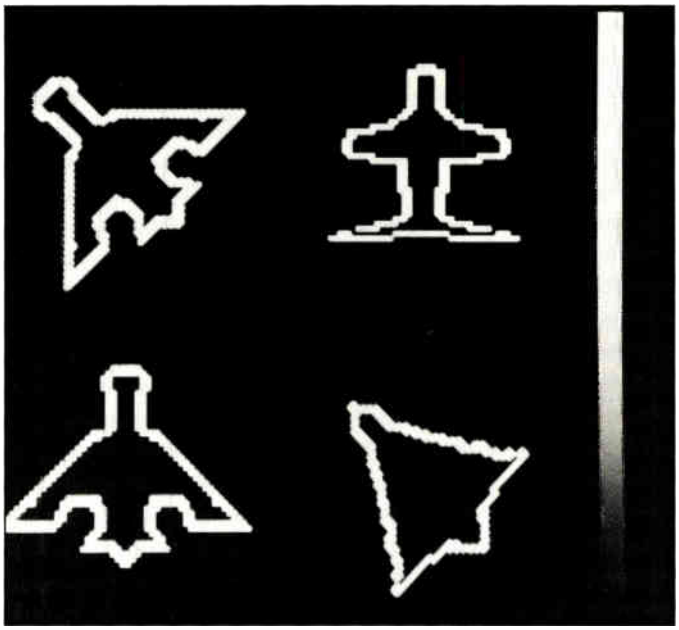
The new system was developed by two researchers at Sandia's Livermore laboratory, mathematician George F. Schils and optical scientist Donald W. Sweeney. They call it a "lock-and-tumbler" process because only the target image can "unlock" a filter that has been keyed to it. Schils and Sweeney performed their work as part of



SPOTTED. Two spikes in Sandia system's plot correspond to images matching a stored target image.

Sandia's basic research program, but they note that it has applications in all aspects of machine vision, from smart weapons to robotics.

The discrimination of the holographic filter is demonstrated in the illustrations. The two spikes in the chart (p. 37) were produced from the two images of the four shown (this page) that match the target image, by plotting the ratio of the mean value of each point in successive displays of the Fourier image to its root-mean-square value. The rms deviation at the invariant points, corresponding to the target images, is zero, and thus the ratio approaches infinity. All other points are smoothed out by variations.



WHICH PLANE? Sandia system picks out the two images on the left as matching the target image, despite their rotations; the others are rejected.

The constant points are displayed in a Fourier image that has been processed by the holographic filter, which is the central component of a hybrid digital and optical system. The system first digitally enhances real-world images, then converts them into coherent light and passes them through a Fourier lens to obtain a spatial transform. The resulting image is called a Fourier image.

SPINNING HOLOGRAM. The hologram is placed in the focal plane of the Fourier lens. When it is rotated, it produces the Fourier summation of all angular harmonics of the input image. Only the images of the same target will have the same amplitude and phase in their angular harmonic terms. And because the holographic filter is designed so as to exhibit constant amplitude, the target images will show up as constant spots on a detector after the beam has been passed through a second Fourier lens.

Creating a hologram that will produce constant-amplitude harmonics at any rotation requires computing the complete rotational response of the target image. The method used entails calculating values for each degree of rotation and finding the commonality of these values by multiplying them together and integrating the result. This obtains new values, called inner products, that are used to determine the basic elements of the image. These can be combined in different ways to reconstruct all possible rotations of the image.

The basic elements are used to design the holographic filter, which in effect performs this reconstruction optically. A calculation that would take 10 hours on a Digital Equipment Corp. VAX computer is performed by the optics in less than a hundredth of a second, according to Sweeney.

However, not all combinations of the inner products will produce a filter that exhibits the constant response. The technique of finding one that does, called spectral iteration, is similar to those used in enhancing telescopic images of stars, Sweeney says. It begins with a random guess and converges by repeated iterations of an algorithm to a solution for which the amplitude harmonics are equal.

Interestingly, a different initial guess will produce a different solution and a different hologram. Schils says he does not know how many solutions are possible.

The hologram designed through these calculations is written by an electron beam on a glass substrate about 3 mm in diameter. The substrate is rotated so that all values of the output Fourier sum will vary except those held constant by the filter, which will only be those of the matching image.

To identify these constant points in a field where most values are constantly changing as the filter is rotated, successive output images are put in a frame buffer and the ratio of the mean value to the rms value calculated.

Development of the lock-and-tumbler process took the Sandia research team, which also included laboratory optical scientist Ellen Ochoa, two years. They now plan to adapt it for three-dimensional images. *–Clifford Barney*

BUSINESS

HALF-HEARTED CHEERS FOR THE TAX BILL

WASHINGTON

Electronics executives aren't exactly jumping for joy over the compromise tax bill Congress will vote on early this month, but they aren't spilling tears over it, either. They say the overhauled tax plan could have been a whole lot worse.

The drop in the maximum corporate tax rate from 46% to 34% is a boon for electronics companies, many of which got little help from the tax cuts of the early 1980s. "We're glad and very supportive of the base-broadening aspects of the bill," says Vico Henriques, president of Cbema, the Computer and Business Equipment Manufacturers Association in Washington. "The drop in the maximum corporate tax rate brings some instant tax relief."

The new bill, however, has its drawbacks, too. The repeal of the investment tax credit will hurt capital-intensive businesses, especially semiconductor manufacturers, and could also discourage computer sales.

R&D CREDIT CUT. Moreover, although the tax credit for increases in research and development spending will be extended—they were scheduled to end this year—the credit will be reduced from 25% to 20%. Also, capital gains, now taxed at a maximum rate of 28%, will be taxed at corporate levels up to the top rate of 34%, which could eliminate some incentive for investment. Tax credits for taxes paid overseas will be reduced, and the new tax code is designed to encourage increased R&D expenditures within the U. S., as opposed to overseas.

Henriques says Cbema had hoped to make the R&D tax credit permanent, but he is encouraged that Congress recognized the importance of the credit enough to extend it for at least three more years. "After all, they could have deleted it all together," he says. Cbema also was disappointed that the R&D tax credit dropped to 20%, but "that may be fixable two or three years down the road." Henriques says.

Ralph Thomson, senior vice president at the American Electronics Association, said his organization would

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Circle 41 on reader service card

work toward getting a permanent R&D tax credit. "With the present competitive environment, to be moving backwards on incentives for commercial R&D is counterproductive," he says. "Raising the percentage and extending that timespan is a major goal." The Semiconductor Industry Association also plans to lobby for permanent tax credits.

Some companies will be hurt more than others. Chip makers are really feeling the brunt of the bill, says Daryl Hatano, government affairs manager for the SIA. "The loss of the investment tax credit puts us in a bit of a hole," he says. "Even with the lower rates, we are still overall worse off than with current law."

Industry groups want to save the R&D tax credit

Also painful for semiconductor companies, he says, is the loss of the 100% investment tax credit carry-over, a provision which allowed a company that lost money (and therefore owed no taxes) to save investment tax credits until it started making money and paying taxes. Now only 65% of investment tax credits can be carried over. "That hurts industries like ours that were caught in a recession during 1985 and '86," Hatano explains.

Successful, non-capital-intensive companies, however, such as Apple Computer Inc. or Tandy Corp., will benefit greatly from the legislation, according to Eugene Glazer, an analyst at Dean Witter Reynolds Inc., New York. "Apple and Tandy, they pay real taxes, high rates," he says. "Overall, their rates will go down." Systems integrators, such as Eastman Kodak Co. or Xerox Corp., however, will not be greatly affected, in Glazer's view.

Peter McCloskey, president of the Electronic Industry Association, is among those who are not fully convinced of the bill's merits. "We had to make certain concessions, and the partial loss of the R&D tax credit was a price we had to pay" to gain a better tax law.

"Generally, we were treated favorably," he says. But balancing the budget is still the most important economic issue facing the country, McCloskey says, and the bill does little or nothing about it. *–Tobias Naegele*

INSTRUMENTATION

SOFTWARE TURNS PC INTO IEEE-488 BUS MONITOR

AUSTIN, TEXAS

Personal computer owners who have recently installed an IEEE-488-bus interface board from National Instruments Corp. got a better bargain than they knew. The Austin-based company is about to ship a software package that brings a dormant section of the board to life as a 488-bus monitor.

The software and special interface logic depict the bus's line-signal conditions in a pop-up screen display that replicates the front control panel of a dedicated analyzer box. The software is scheduled to debut next week at Midcon '86 in Dallas, and the company plans to give a copy—which it says is worth about $100—to anyone who already owns a GPIB-PCIII board or who buys one by the end of this year. The board, which can transfer data at 1 megabit/s, has been on the market for nine months.

National Instruments executives liken the pop-up engineering tool to the growing number of memory-resident office-automation aids for personal computers, such as on-line spelling checkers and pop-up calculators. They say it puts a 488-bus analyzer at the fingertips of those using IBM Corp. Personal Computers and compatibles. The monitor software resides in about 9-K bytes of main memory.

To see what's happening on the instrumentation bus, users strike two keys simultaneously. The command interrupts the bus's operation and causes a horizontal display to pop up across the top of the screen. Icons show the condition of each data, bus-management, and handshake line on the IEEE-488 bus at the split second the monitor program was activated. A single keystroke releases the monitor, and the GPIB-PCIII goes back to its main task, transferring data to and from the bus.

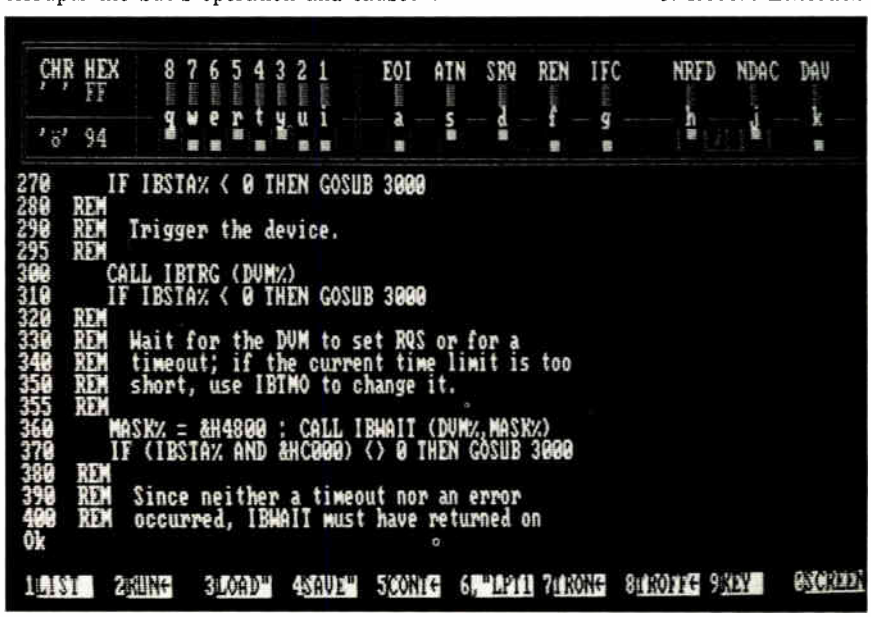
"The boards have had the special logic, but we have been keeping this feature under wraps" until the software that makes use of it was ready, says Donald Nadon, vice president of sales.

The monitoring program is a subset of more powerful software used on National Instruments' 410 analyzer board, which can be set to selectively capture conditions on the 488 bus as well as search for specific patterns. The monitoring program of the GPIB-PCIII only presents a freeze-frame image of bus-line signals at the time it is manually invoked; it has no self-triggering facility built in.

Lab engineers and technicians often need to determine the signaling conditions of the 488 parallel bus when they are debugging control programs for test and measurement applications. They have to find out why buses hang up and which 488-attached device is not reading or writing correctly, notes Larry Anglin, applications engineer for the product. "Usually, they will have to use dedicated analyzers to evaluate the problem," Anglin says.

Stand-alone analyzer boxes do offer more sophisticated capabilities, but they're also much more expensive than the resident monitoring software, says Donald Nadon. He estimates dedicated analysis hardware can cost as much as $5,000, compared with $795 for the GPIB-PCIII board.

–J. Robert Lineback



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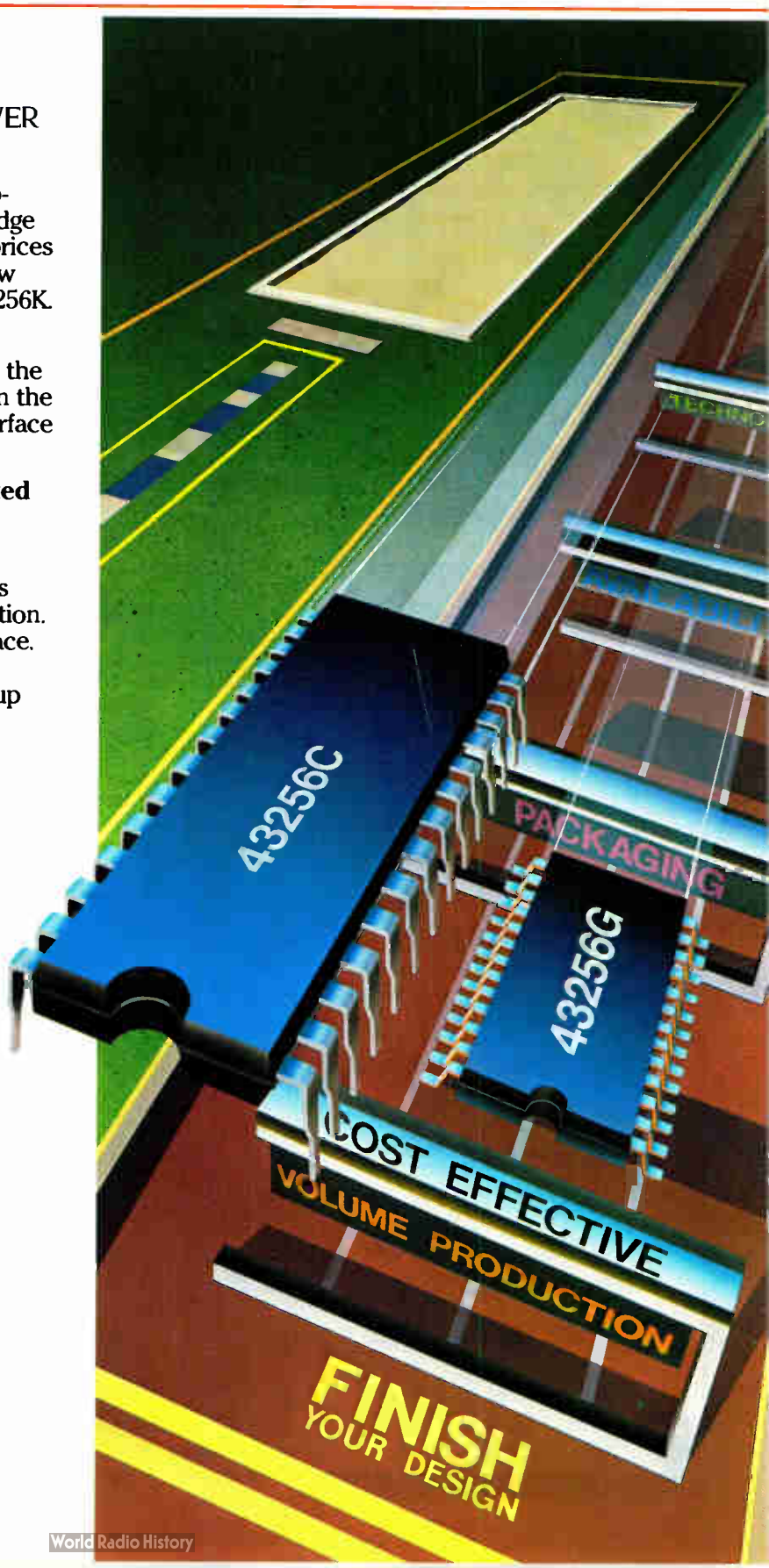


MODULE ADDS SMARTS TO MINITEL TERMINAL

PARIS

The French Minitel videotex terminal already has proved to be a fountain of francs for banks, retailers, airlines, service industries, and a growing band of entrepreneurs who use it to offer everything from legal advice to dating services. Now a six-person Paris firm, C&D Informatique SA, is cashing in on the fast-growing Minitel network with hardware—a $200 microprocessor-based interface module that lets users work with their terminals off line.

Intended mainly for business users, C&D's Mistral 1 module got off to a fast start last month after it was featured in a TV newscast. Vacations make August a poor month for business in France, but 4,000 viewers phoned to ask about the module the same week, reports Christian Dollet, a cofounder of the two-year-old company. "We had a thousand in stock and they're almost gone."

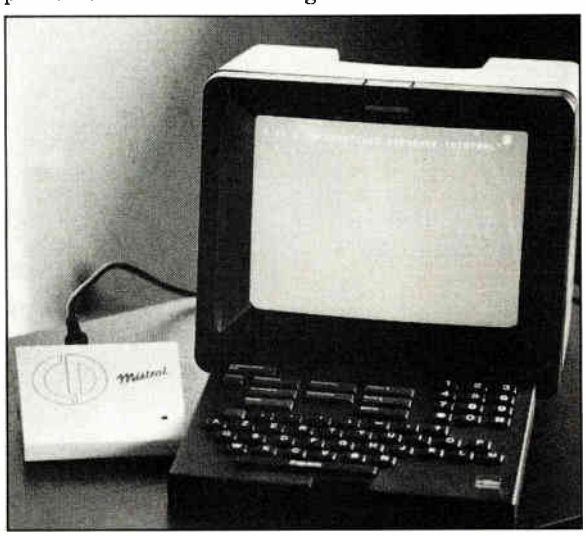
C&D has an arrangement with a small factory in Limoges to produce the module, but it is lining up other contractors to turn out as many as 100,000 a month if they are needed to meet demand. "Mistral targets a large percentage of people using Minitel," Dollet says. "There are 1,800,000 Minitels in France and we know that the Direction Générale des Télécommunications [the government agency that runs the phone system] wants a Minitel for each telephone in the future, because the system was created to replace telephone books [*Electronics Week*, June 10, 1985, p. 17]."

In effect, the Mistral module converts a "dumb" Minitel tethered to the telephone network into an intelligent terminal. The basic idea isn't new; a handful of boxes already exist that hook the Minitel up to a limited range of computers and printers or generate cyclical advertising displays, but they sell for $300 to $700. One small company, Télématique Videotex Française SA, for example, markets an advertising-message module for $500.

OFF-LINE SAVINGS. Mistral does that and more. It helps cut costs for those using Minitel's data bank, the most common uses of which are looking up the numbers of service people and reviewing bank statements. Mistral users can call up information, store it, then turn off the telecommunications link and work with the information off line. Companies that make heavy use of Minitel to send internal messages can slash line charges by preparing texts in advance, then using the line only to transmit.

The module has no controls; all functions are performed from the terminal's keyboard, which includes a function key to disconnect it from the telephone line. The module is built around an 8-bit 6802 microprocessor supplied by Thomson-CSF (which has a license for the device from Motorola Inc.) and has 8-K bytes of static random-access memory and 32-K bytes of erasable programmable read-only memory in its basic version. An additional 32-K bytes of SRAM runs the price up another $130. Dollet originally considered using semicustom circuits for the module but ruled them out because they cost too much.

Even using standard components, Dollet was able to package Mistral 1 in a box that measures 4.4 by 1 by 3.7 in., small enough to fit into the carrying-handle indentation at the top rear of the Minitel cabinet.



INTELLIGENCE. Mistral module fits into the handle space of a Minitel and turns it into a reasonably smart terminal.

For Dollet and cofounder Gérard Cappagli, Mistral 1 is just the first of a family. "All the products will be the same shape and price" and fit into the Minitel handle space, says Dollet. But unlike the Mistral 1, "the next project will directly attack the home-computer market. Minitel in the future will be in all homes, so we will need to develop family uses, such as cassettes with applications software," he suggests.

–Jennifer L. Schenker

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SEIKO INSTRUMENTS

Circle 45 on reader service card

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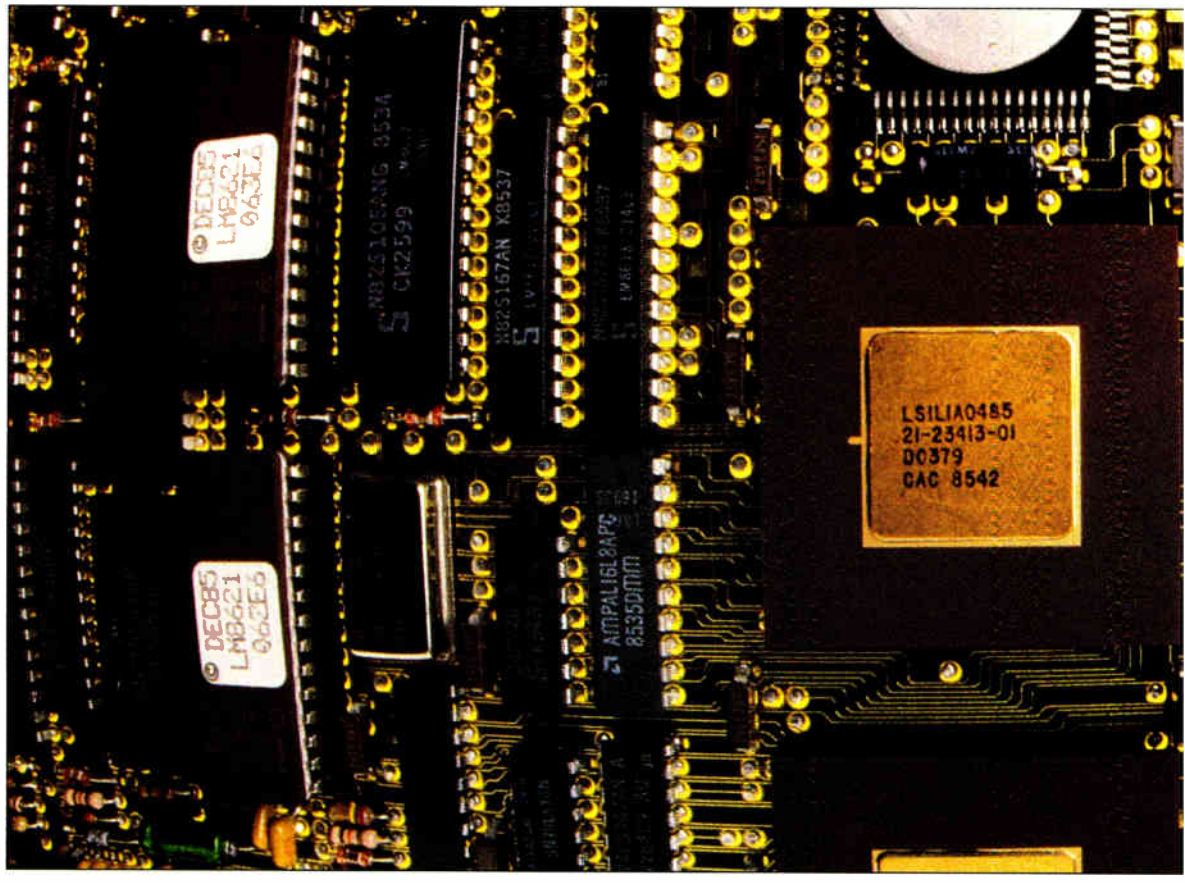

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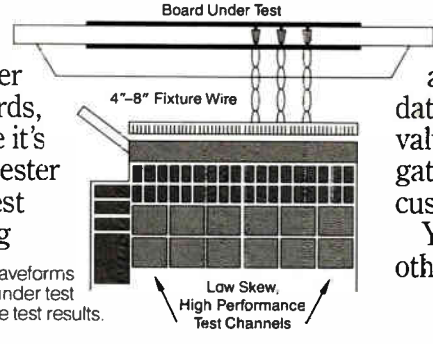

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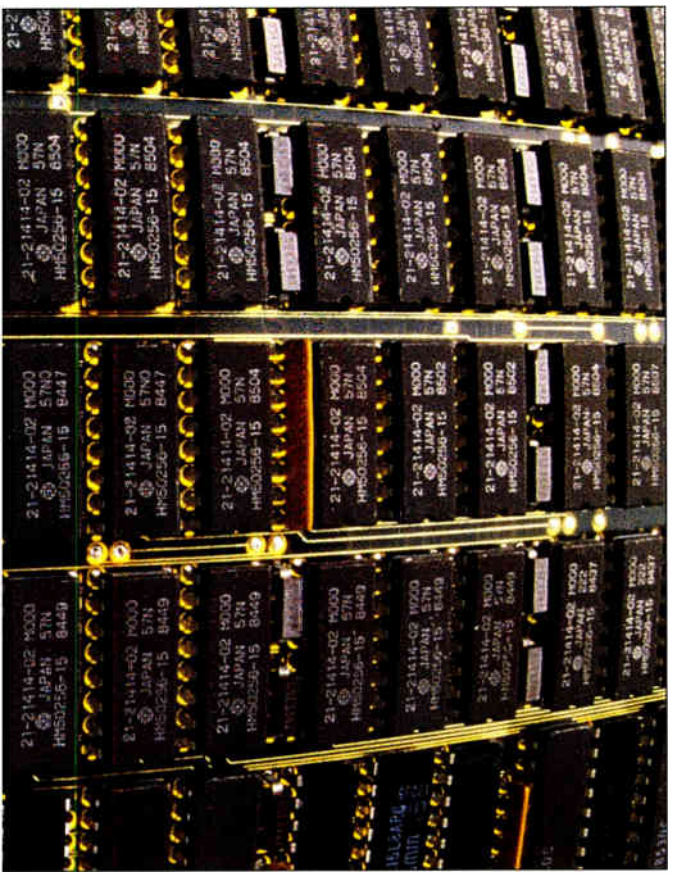

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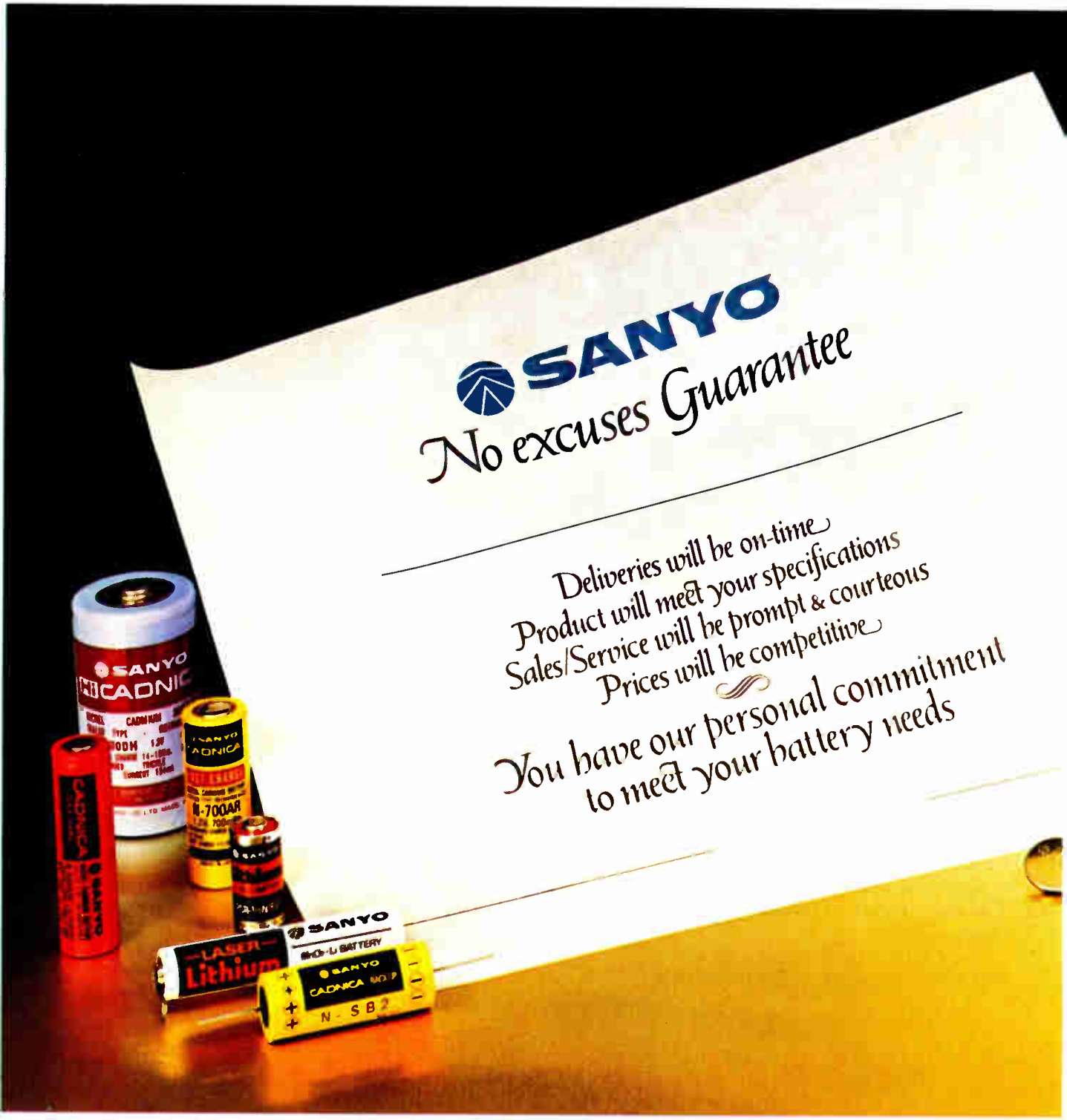

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INTERNATIONAL NEWSLETTER

U. S.-JAPANESE COMBINE PLANS A JOINT VENTURE IN CHIPS

Executives of a U. S. maker of chip sets for IBM PC clones were scheduled to head for Japan on Labor Day to nail down details of a partnership with one of Japan's largest software companies. The two firms, Chips & Technologies Inc. of Milpitas, Calif., and Ascii Corp. of Tokyo, are putting together a company to enter new worldwide markets, particularly in communications protocols such as those for the integrated services digital network. Plans are still tentative—the new firm does not even have a name yet—but the idea is to use Chips & Technologies' computer-aided-engineering system for design work and have the products manufactured by major Japanese chip makers working as silicon foundries. The two companies will each hold an equal share of the majority interest in the new venture. Minority investors will include general trading company Mitsui Bussan, component and equipment manufacturer Kyocera, and perhaps others, including diversified manufacturer Nippon Gakki. Tentative arrangements call for Kazuhiko Nishi, vice president of Ascii, to be president of the new company and for Gordon A. Campbell, president and chief executive officer of Chips & Technologies, to be chairman. □

SIEMENS MIXES LITHOGRAPHY METHODS FOR GaAS ICs

Siemens AG is joining the likes of Raytheon, Tri Quint Semiconductor, and Westinghouse in combining optical and electron-beam lithography to build gallium-arsenide ICs. Researchers at the Munich company are producing prototype GaAs field-effect transistors for use in broadband communications systems that handle data at rates up to 10 gigabits/s. Like the other companies, Siemens uses the electron beam to make the gates, whose length—0.5 μm and less—is crucial to high-speed device operation. It uses the speedier optical methods for the less critical structures between 0.5 and 2 μm. □

SONY INTRODUCES NEW 8-MM PRODUCTS AND PROMISES MORE

Striving for advantage in the battle over 8mm-format video-cassette equipment, Sony Corp. is coming out with a feature-loaded camcorder as well as a new recorder, and promises more products before the end of the year. At $1,795, the camcorder is $182 more than Sony's recently introduced model [*Electronics,* June 2, 1986, p. 11]. It boasts a wiper/fader, titling in seven colors, continuous color balance, variable zoom speed, and both single-frame and interval recording (at 8 frames every 10 seconds). The new VCR sports a price tag of $1,149, some $464 less than the existing top-of-the line model. Meanwhile, Hitachi Ltd. has lined up with Victor Co. of Japan and against Sony in the format imbroglio. Hitachi, which sells camcorders under its own name in JVC's VHS-C format, says it will stay in that camp and will supply a 3-lb unit to camera makers Kyocera (Yashica), Asahi Pentax, and Minolta [*Electronics,* July 10, p. 42]. Kyocera will also continue to sell private-label Sony models. □

EAST GERMANS EMPHASIZE ELECTRONICS IN THEIR LATEST 5-YEAR PLAN

The East German government is placing most of its eggs in an electronic basket, with particular emphasis on automated production. In the newest version of the government's five-year plan, running through 1990, the electrical and electronics industry has been assigned a growth rate of 8.3% to 8.6% a year, a goal higher than those assigned to any other industrial sector. The number of industrial robots is to triple, from about 4,500 last year, and the number of flexible automated-production centers is to quadruple, from the present 20 to 80. All in all, East Germany's GNP is slated to rise to 4.7% a year, which compares with an annual 4.4% during the previous five years. □

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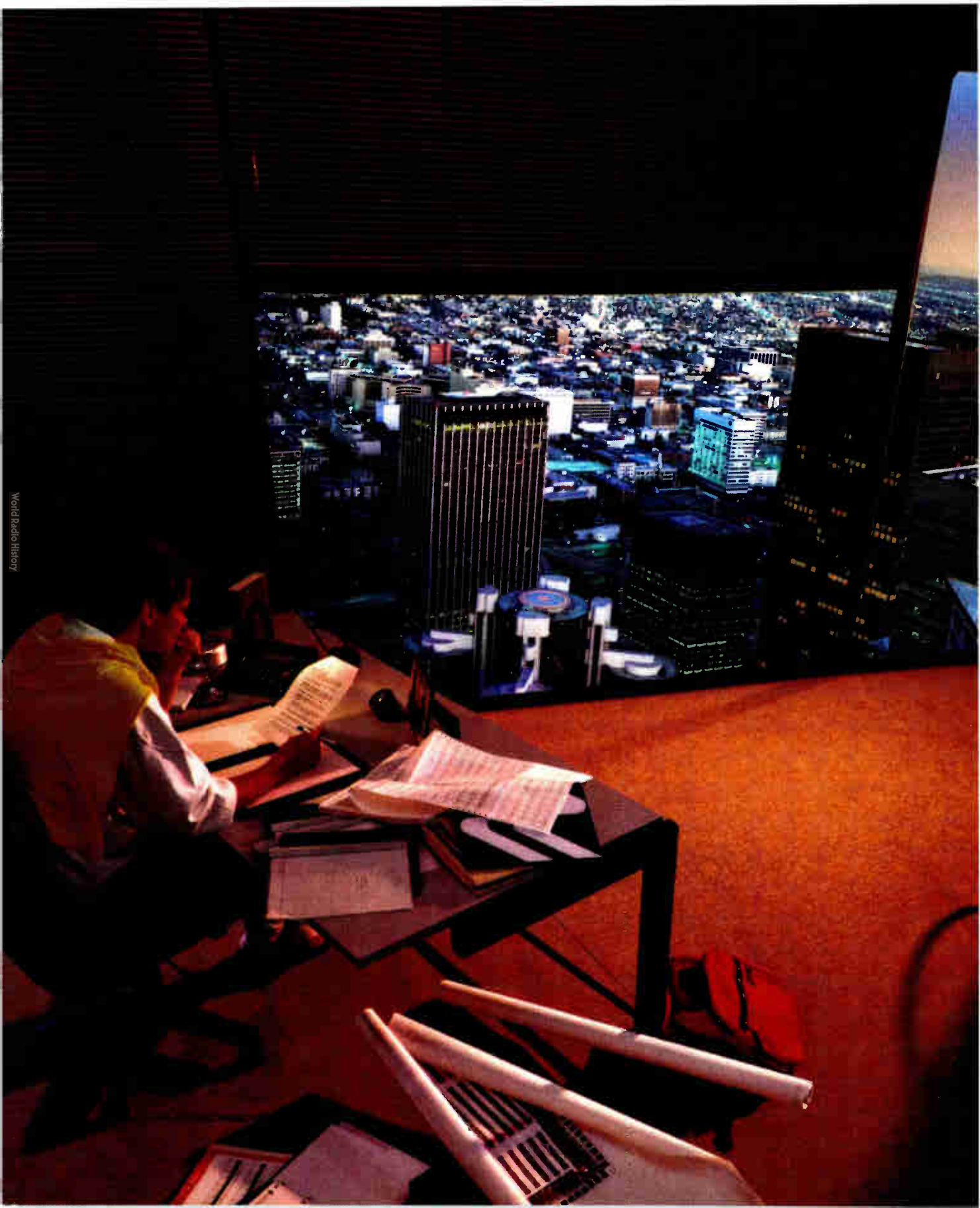

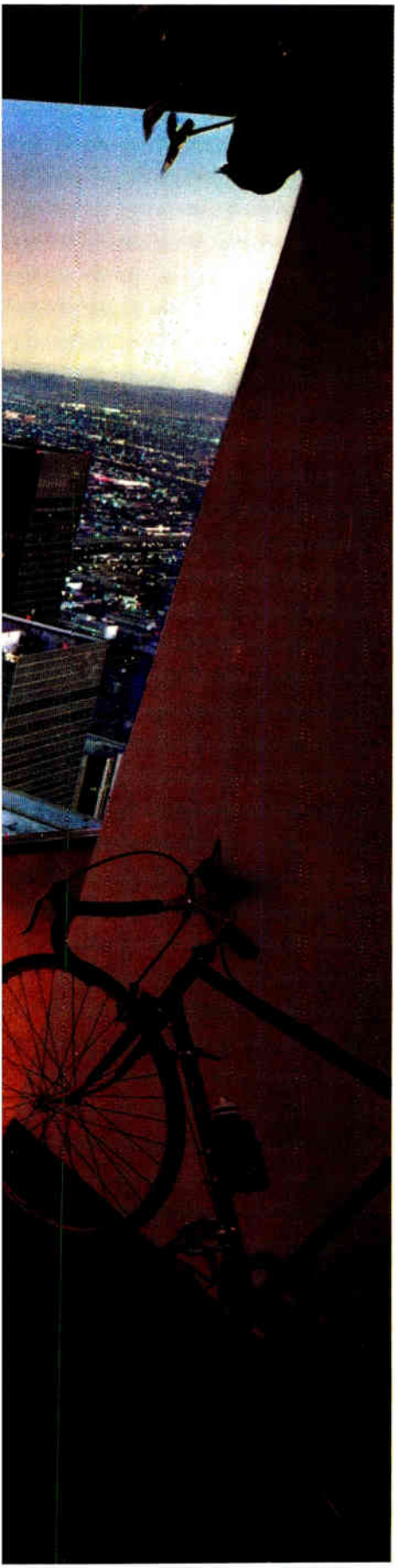

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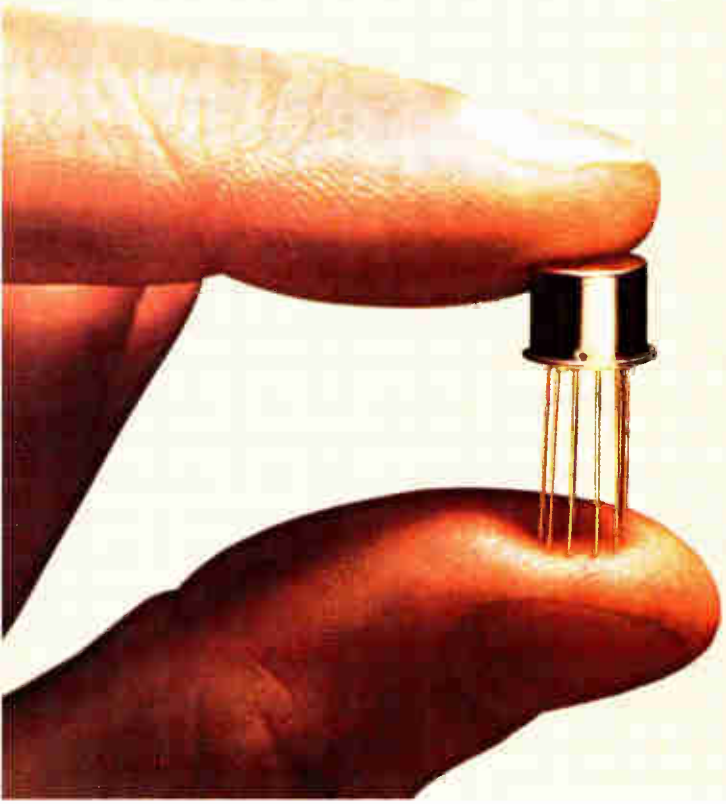

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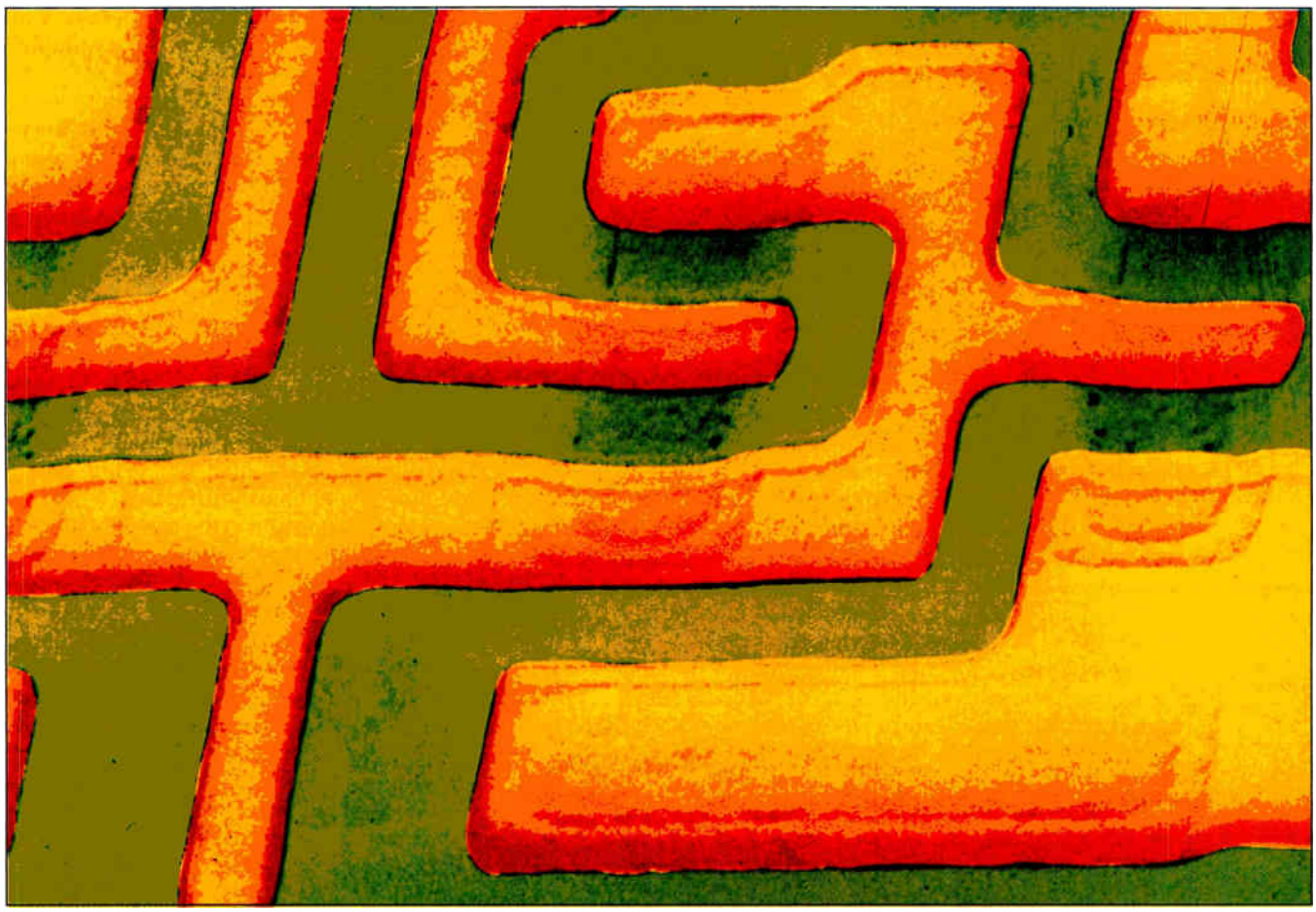
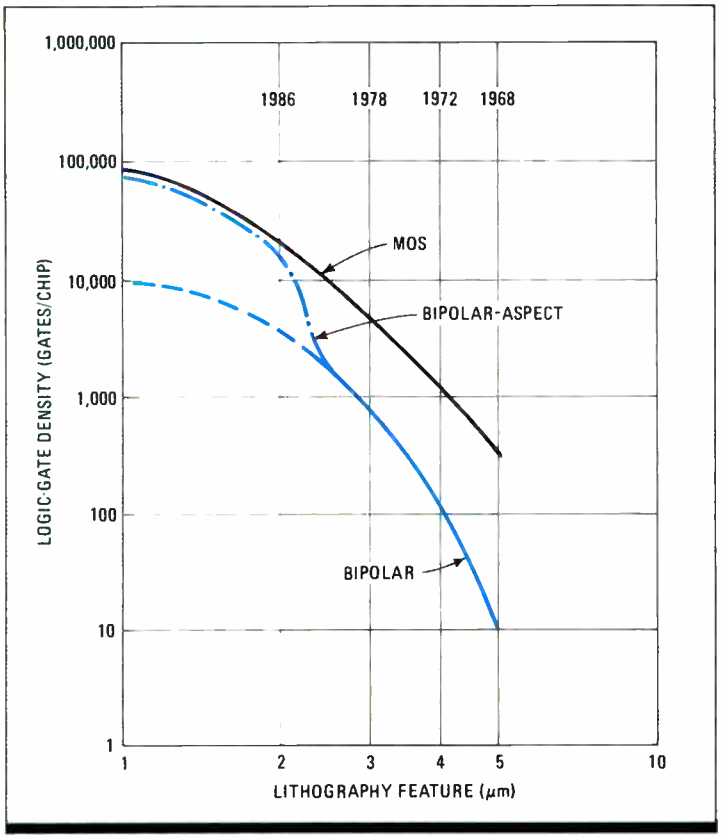
INSIDE TECHNOLOGY

FAIRCHILD'S RADICAL PROCESS FOR BUILDING BIPOLAR VLSI



Bipolar technology, always faster than CMOS, is about to break through into CMOS-level density. For years, that achievement has eluded the makers of bipolar chips, although they have managed to reach the feature size necessary for very large-scale integration. Attempts to fabricate dense bipolar



1. ONE BETTER. Bipolar ICs fabricated in the Aspect process will match the density of MOS devices and surpass them in speed.

devices have run up against oversize transistors, excessive power dissipation, and low yields. Now a new process based on the concept of contactless transistors has reduced the size of these devices and virtually eliminated the problems of interconnecting them on a chip. It will make it possible to create the chips needed for further development of such products as mainframe supercomputers and advanced engineering work stations. The contactless process also cuts power consumption and increases yield.

Developed by Fairchild Semiconductor Corp.'s Research Laboratory, the Aspect process uses conservative 2-μm design rules to bring CMOS-like VLSI density and 500-MHz clock rates to an enhanced class of emitter-coupled-logic integrated circuits. Not only will Aspect allow fabrication of gate arrays ranging in density from 20,000 to 80,000 gates; it will also allow the design of memories of very high density and speed. With the present 2-μm process, 64-K SRAMs approaching 1-ns speeds are possible. The next-generation 1-μm process will bring 256-K SRAMs of comparable speed.

KEY PROCESS PARAMETERS

	Aspect	Isoplanar ECL
Effective gate size (mil^2)	4	15
Power per gate (mW)	1	5
Loaded-gate delay (ps)	350	500
Unloaded-gate delay (ps)	200	250
Power-delay product (pJ)	0.2	1.25

Within the next six to nine months, Fairchild expects to begin shipping samples of a variety of Aspect products, including a 10,000-gate ECL array, a 400-MHz digital-to-analog converter, and a video shift register for graphics processing. The Aspect process will reach its full potential in full-custom and standard random-logic designs, at least doubling the density of such implementations as gate arrays. And density will be increased even more by stacking logic levels.

One of the most exciting prospective applications of the Aspect process is in the fabrication of high-performance 16- and 32-bit microprocessors. Fairchild's designers can integrate 20,000 gates in 2-μm geometry on a 0.4-by-0.4-in. chip, assuming that power consumption does not exceed 20 W. Using 1.5-μm design rules, a chip of the same size can hold another 10,000 gates. And when 1-μm Aspect technology becomes available, 70,000 gates will fit.

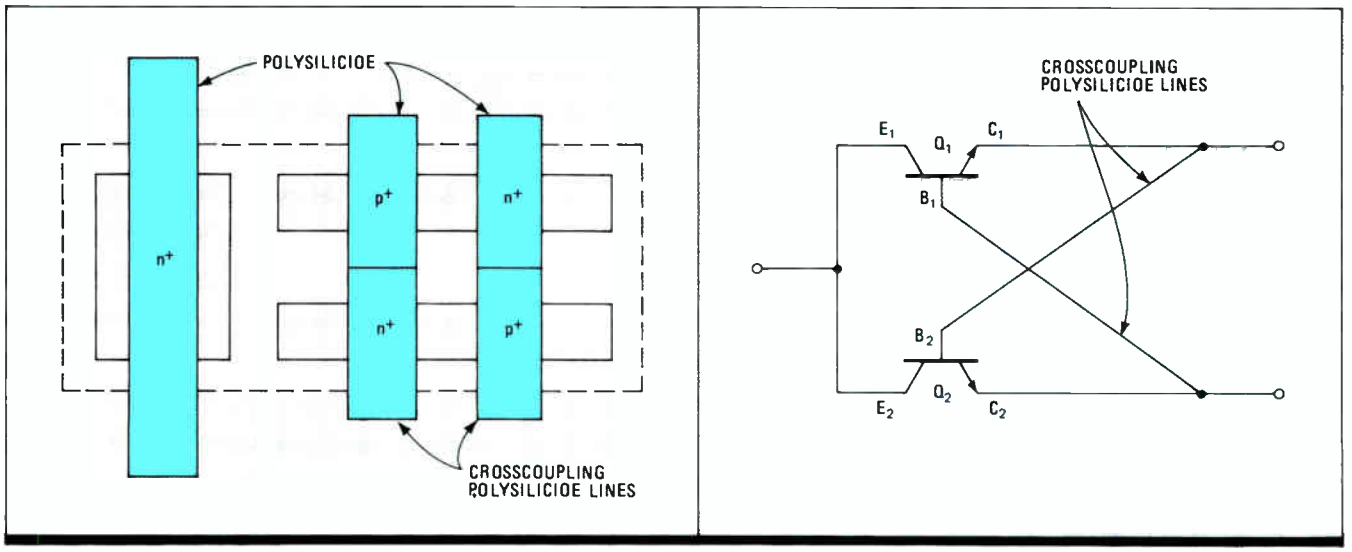
Aspect is one of a number of developments marking the resurgence of bipolar technology. One sign of that resurgence is the resurrection of the Bipolar Circuits and Technology Meeting (see p. 100). Before Aspect, bipolar technology trailed MOS processes in the number of gates that could be packed on a chip. At current 2-μm geometries, MOS has a significant lead over ECL. Moreover, while MOS continues to improve in density, conventional ECL hits a plateau even as feature sizes fall to the 1-μm dimension.

Aspect processing, however, allows bipolar technology to challenge the dominance of MOS (Fig. 1). The density of bipolar will soon equal that of MOS. Moreover, chips fabricated with the Aspect process will continue to provide faster switching speeds than their MOS counterparts.

REDUCING THE GATE

To fabricate dense ECL digital ICs, chip designers must optimize three parameters: density, power, and speed. The first step is to reduce the size of a basic gate. With Fairchild's current 3-μm Isoplanar ECL technology, each gate occupies about 15 mil^2. A standard 0.4-by-0.4-in. chip can theoretically hold about 5,000 gates, including interconnecting wiring. Each gate, however, consumes about 5 mW in order to keep propagation delays in the range of 500 ps under loaded conditions. But if each gate dissipates 5 mW, a 5,000-gate chip would consume 23 W, far too much power for current IC packages. Conservative design in Isoplanar ECL dictates a total of about 200 gates for a device that consumes 5 mW/gate—hardly VLSI.

An Isoplanar ECL gate's power-delay product is 1.25 pJ, based on a dissipation of 5 mW and an unloaded-gate delay of 250 ps. Aspect's designers, aiming for true VLSI densities of around 20,000 gates per device, sought to lower the power-delay



2. DUAL-PURPOSE. Fairchild Semiconductor's Aspect process is based on the concept of contactless transistors. The polysilicide lines that interconnect common transistor nodes also serve as part of the transistor's base, collector, and emitter.

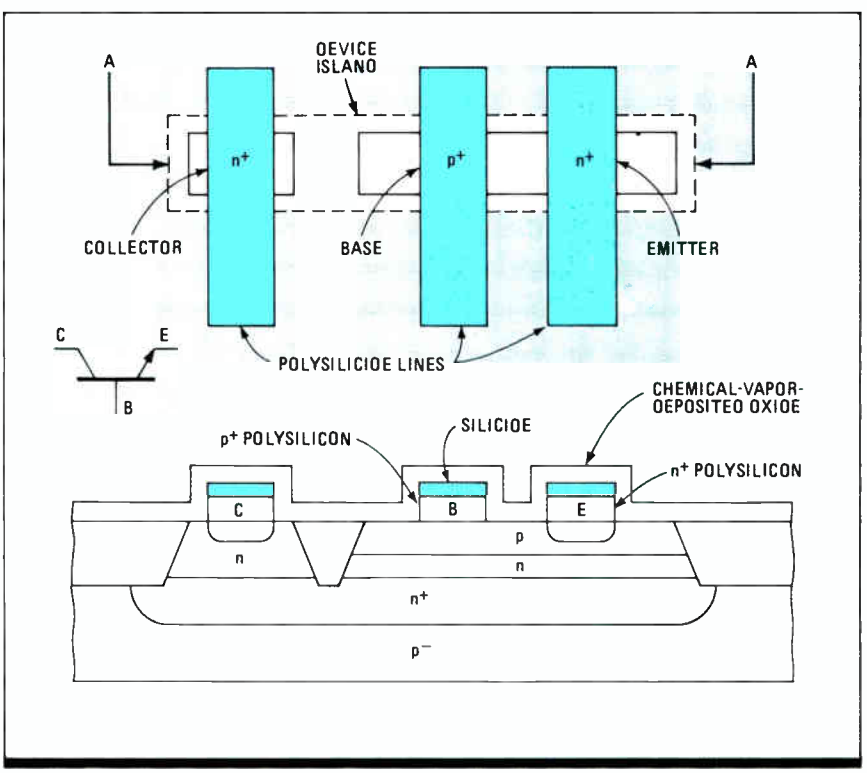
product to less than 0.2 pJ per gate (table). This meant a dissipation of about 1 mW/gate and an unloaded propagation delay of 200 ps. And it required transistors small enough—less than 4 mil²—to fit these operating parameters.

Fairchild designers decided against modifying Isoplanar ECL technology. For one thing, Isoplanar ECL consumes too much power. For another, scaling down from 3-μm to 2-μm geometry does not appreciably increase packing density, because lateral diffusions and encroachments are too large. In addition, designers would have had to deal with exacting ECL processes such as diffusions, contact holes, and inside islands, plus the technology's inability to align mask levels—all formidable barriers.

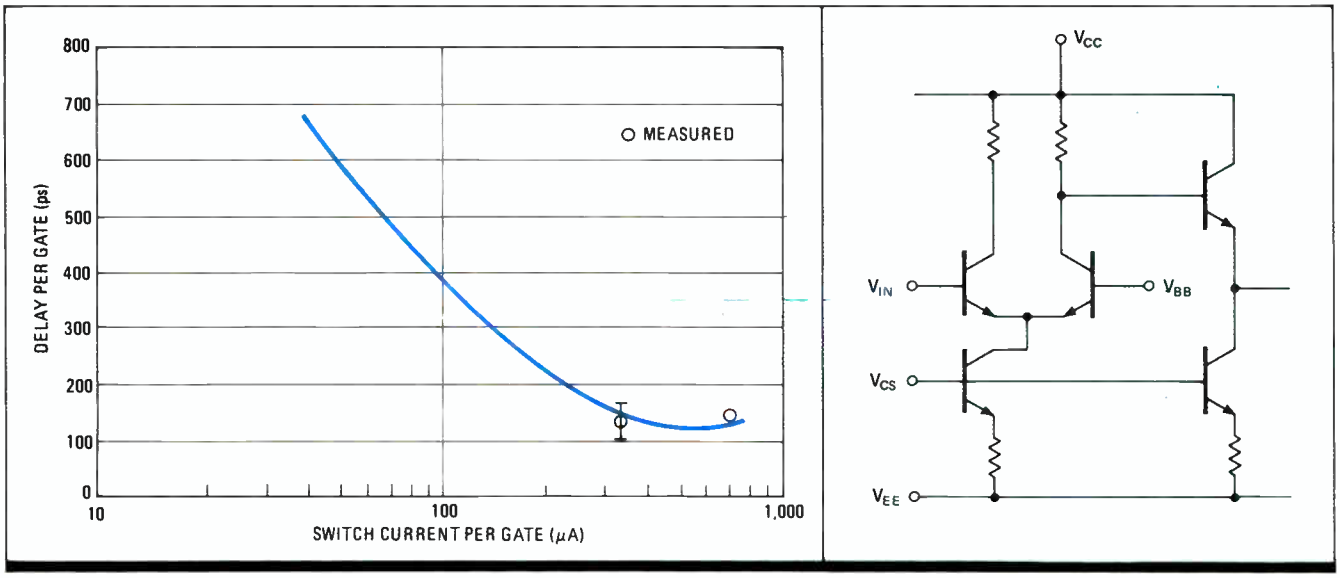
Yields also would be problematic. VLSI devices must be manufactured at yields at least an order of magnitude better than those of low-density ECL chips. Typical failure rates for ECL transistors in manufacturing are on the order of 100 parts per million. Aspect, however, has a manufacturing failure rate of 10 ppm. Such low rates are mandatory for devices that will contain 100,000 or more transistors. In fact, recent yield figures on the Aspect process indicate that 3 ppm could be possible once the process is refined.

An npn transistor fabricated in Aspect's contactless process has polysilicide running above the base and collector regions, which serves two purposes. First, it connects the base and collector electrodes; second, it eliminates the need to connect the two electrodes on a common metal contact point. Because the polysilicide can be extended in any direction throughout the substrate, any number of transistors or logic elements having common points can be connected (Fig. 2). Moreover, the metal contact that connected the emitter to other elements kept an emitter from coming close to the surface. With the development of polysilicide as an interconnect, Fairchild designers had an opportunity to not only bring emitters closer to the surface but also to fabricate shallower bases.

Because polysilicide can short two doped lay-



3. BUFFER. A chemically deposited oxide covers an Aspect-fabricated npn transistor's polysilicide interconnection material and isolates the emitter, base, and collector from the metal layer that will be formed over the oxide.



4. FAST SWITCH. An Aspect gate (right) will still switch at subnanosecond speeds, even though power varies.

ers—one p and one n—fewer contact windows need to be opened on the chip. This makes more area available for active devices, which permits increased packing density.

These contactless connections are the result of a number of bipolar processing enhancements to planar technology. For example, Fairchild's planarization process eliminates the well-known bird's beak phenomenon, in which residual polysilicon, called stringers, cause the shorting of transistor bases to emitters. This improved planarization opens the way for polysilicide to be used as an interconnection medium.

One reason that polysilicide can be used as an interconnection medium is that it is buried beneath a layer of oxide formed by chemical vapor deposition. A metal layer can be formed over the oxide without concern for its shorting to the polysilicide.

Because Aspect is relatively insensitive to misalignment, it will be able to move to smaller geometries much more easily than can conventional bipolar processes

Instead of using conventional copper-doped aluminum for emitter connections, Aspect uses polysilicide because it is a more reliable current carrier. Metal lines must be made extremely thin—3/4 to 1-μm wide—to fabricate a small transistor whose base and emitter are close together. The already thin lines narrow even further as they pass through the bird's beak area in other ECL transistors, creating a localized weak spot. Current flow on the order of 5 mA can burn through the metal at the weak spot, especially if the transistor operates at high temperature. Polysilicide emitter connections can be up to 4 μm wide, and so they pose no current-handling difficulties and no excessive dissipation that could melt the lines.

In the Aspect process, a typical npn transistor is fabricated by composed masking, which means that critical spacings between the base and emitter are defined at the same mask level (Fig. 3). Alignment becomes less important, because any movement of the polysilicon mask either to the left or to the right equally shifts the base and emitter electrodes. If the base and emitter were defined at different mask levels, as in conventional bipolar processing, even the slightest misalignment between two masks could result in open or shorted connections.

Because alignment tolerances are not expected to improve significantly as transistor geometries are scaled to 0.5-μm spacings, Aspect's relative insensitivity to misalignment will enable it to move to smaller geometries with less difficulty than conventional bipolar processes. For example, the best available steppers can hold a tolerance of about 0.1 μm, more than adequate for building transistors with 2-μm spacing. Though designers would like greater tolerances for 0.5-μm spacing, it is unlikely that the necessary machinery will materialize.

An important feature of Aspect is that it is almost entirely self-aligning. The polysilicide covering the base, emitter, and collector regions can align itself to the polysilicon layer, and the n^+ polysilicon layer can align itself to the emitter. Aspect also uses polysilicon resistors, which are formed over the field oxide. Such resistors exhibit very low junction capacitance, making them ideal passive components for high-speed logic circuits.

Aspect is the first bipolar process to use polysilicon for the emitter structure. Polysilicon acts as a source of impurities that enter the device's crystal structure. This permits the fabrication of

extremely shallow emitters—about 500 Å below the surface. Before Aspect, the shallowest emitters in bipolar technology were at least 1,000 Å below the surface—it was impossible to make them shallower. The metal-over-single-crystal emitter structure in conventional bipolar technology acts as a sink for the hole current coming from the base, thereby lowering the transistor's current gain.

As in the emitter, polysilicide serves as a source of impurities for the base. This allows both shallow and narrow base regions to be fabricated with significant amounts of base doping. The combination of shallow emitters and bases leads to transistors with a very high gain-bandwidth product. And the higher the gain-bandwidth product, the faster the transistor operates in switching applications.

BUFFERING THE STRUCTURE

In addition to eliminating conventional metal contacts, polysilicide acts as a buffer between the polysilicon base and emitter regions below it and the metallization layer above it. Although the layer is only about 0.2 μm, it plays an important role in the vertical scaling of bipolar transistors. Before Aspect, transistors could be scaled only in the horizontal plane, in part because extremely shallow junctions could not be fabricated. No matter how small a transistor's horizontal dimensions, its performance seldom reached designers' expectations. By scaling both horizontally and vertically, bipolar transistors can be reduced in size and upgraded in performance.

The power-delay product remains the most useful and universal specification for defining the performance of a logic gate. Besides reducing a gate's power consumption to 1 mW or less to achieve device densities of about 20,000 gates, bipolar chip designers must develop gates that operate at 1 ns or less to meet the requirements of supercomputers and other sophisticated, high-end computing equipment.

An Aspect gate's power consumption can vary over a wide range (Fig. 4); yet the device maintains subnanosecond switching performance. For example, at a current of 55 μA, the gate delay is 550 ps; at 350 μA, the delay improves to 170 ps.

This is an important factor in application-specific IC fabrication. It means that a designer can program slower logic paths for lower current (hence lower power consumption) while maintaining high performance in terms of switching speed. And when power consumption is reduced, packing density can be increased, since a chip's consumption is the limiting factor in IC design. With more gates on a chip, a greater number of logic functions can be incorporated within a single IC. □

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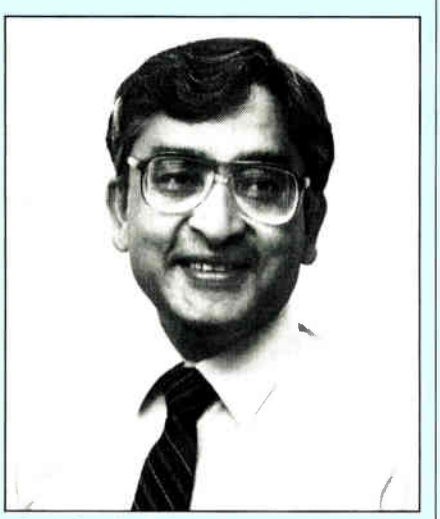
HOW VORA TURNED ECL INTO A TECHNOLOGY DRIVER

One measure of the importance that Fairchild Semiconductor Corp. places on bipolar technology is that 50 to 60 designers and engineers are on the bipolar research team—more than the entire technical staff at many companies. Heading that effort is 48-year-old Madhu Vora, principal architect of Fairchild's Aspect, a bipolar process based on the use of contactless transistors.

By the early 1980s, it became clear to Vora and his fellow workers at the Fairchild Research Laboratory in Palo Alto that the design and fabrication of bipolar circuits would have to be changed radically to achieve very large-scale integration. "The situation is very much different from the late '70s when bipolar designers looked to MOS and CMOS for the techniques and processes that would allow them to achieve LSI levels," he says.

"Bipolar VLSI is pushing into areas that even CMOS VLSI has not gone. Reversing the situation of the '70s, CMOS designers are looking to bipolar VLSI as their technology driver, borrowing such techniques as multilevel interconnections, the use of alternatives to aluminum for interconnect, and silicided interconnects and gates."

Fairchild's Aspect process goes several steps further. "I think it is safe to say that Aspect is a revolutionary step forward, not only in bipolar, but also in MOS/CMOS VLSI as well," Vora says.



VORA: Pushing bipolar into new areas.

Ultimately, he believes, almost every technique that the Aspect process uses for the fabrication of bipolar circuits can also solve certain problems in MOS design. "In particular, advanced CMOS VLSI processes are running into the same problems with diffusions and contact holes that ECL designs are having. Applying the contactless-transistor approach to MOS designs would result in similar improvements in density, speed, and reliability."

Born in Amreli, India, Vora earned his BSEE degree at the Government Engineering College in Jabalpur and his MSEE at the Worcester Polytechnic Institute in Worcester, Mass. Before joining Fairchild as its director of bipolar research, he spent 14 years at IBM Corp. in Poughkeepsie, N. Y., leaving in 1976 as a senior engineering manager.

His first effort at Fairchild was managing the development of Isoplanar ECL and its transfer to production. He also worked on the company's 9450 bipolar microprocessor.

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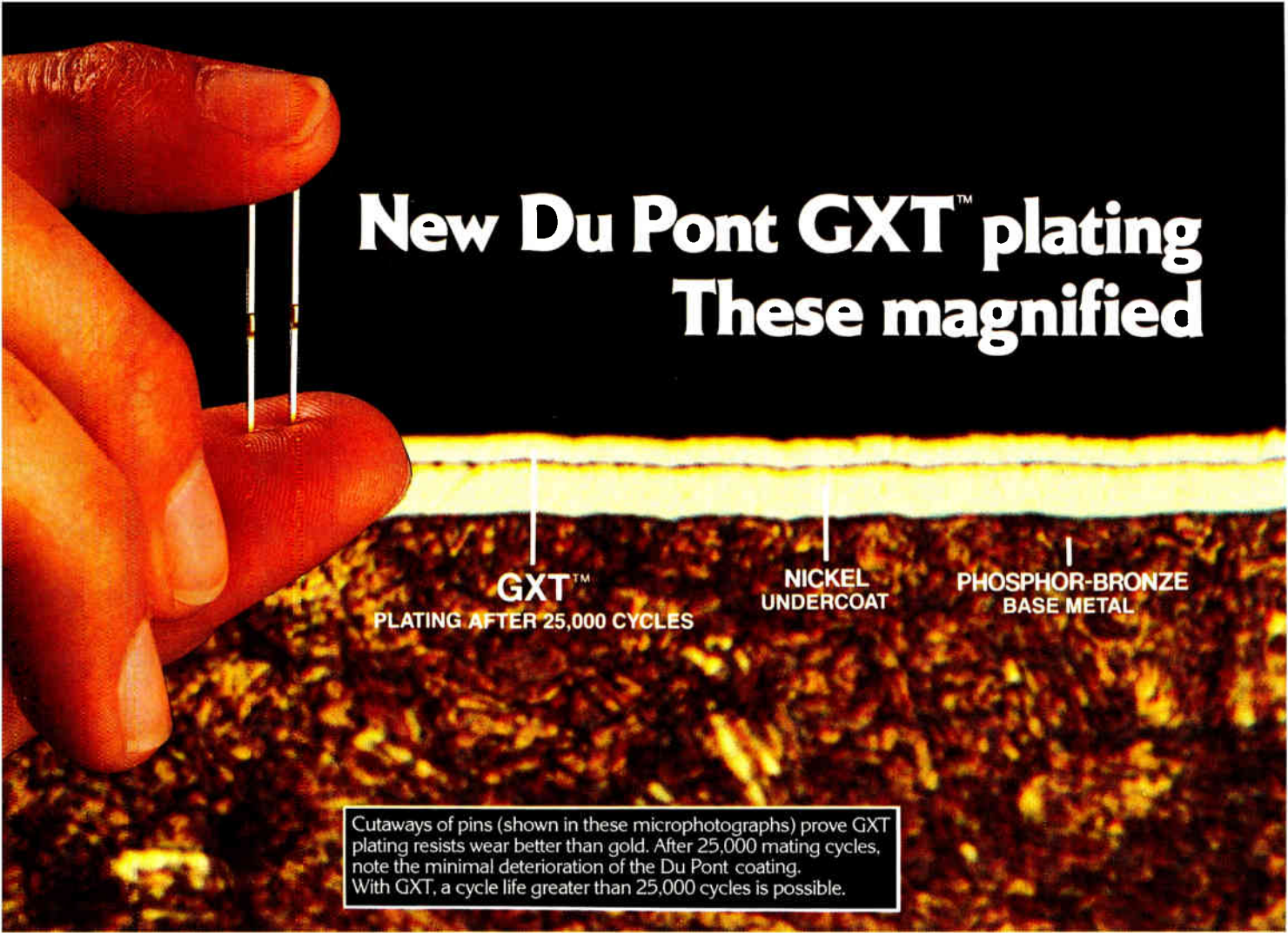

Tests also show the GXT plating system is better than gold in solderability, porosity, bend ductility, and corrosion resistance. Yet GXT can reduce costs as much as 20%.

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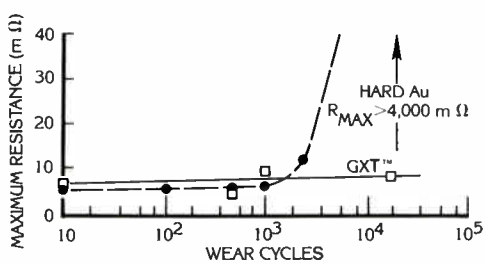

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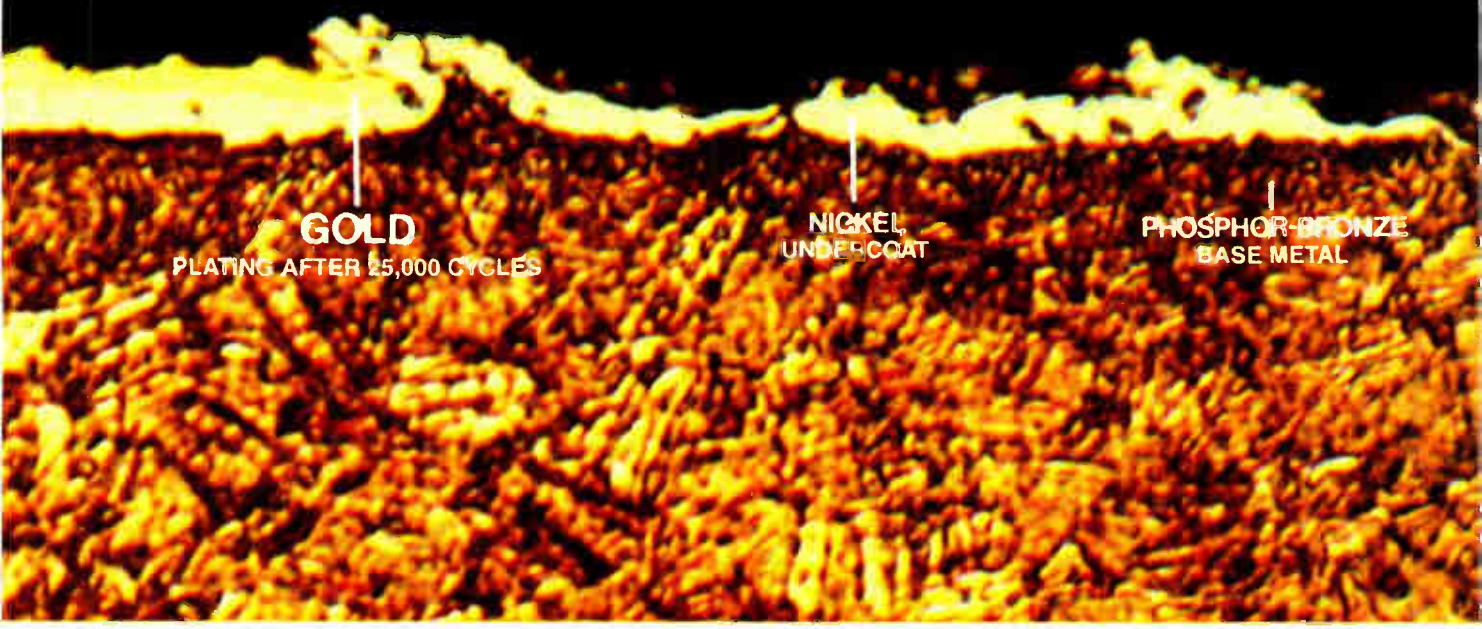

In these tests, other gold substitutes didn't measure up to GXT, either. In porosity, solderability, intermetallic growth, bend ductility, internal stress, and manufacturing process stability, the GXT plating system clearly outperformed all other gold alternatives including other palladium-nickel and pure palladium coatings.

In fact, in no test did any gold substitute—or gold itself—outperform GXT.

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BIT-SLICE ARCHITECTURE TACKLES THE 32-BIT WORLD

A raft of microprogrammable 32-bit-slice components is heating up the competition, but microprocessor makers are fighting back with faster parts and enhancements

by Bernard Conrad Cole and Alexander Wolfe

An upstart product is capturing a lot of attention in the 32-bit processor world, a market that's already generating plenty of excitement. In the past year or so, the action has shifted to the 32-bit-slice microprogrammable building block.

Many semiconductor companies are jumping into this new market and are introducing products at a quickening pace. By the end of the year, 32-bit-slice components will be available from at least four companies, and other product families are slated for early introductions.

Not that advances in the traditional 32-bit microprocessor market have peaked. Faster clock speeds, along with architectural and software enhancements for existing products, have either been announced or are expected soon. And chip makers are beginning to drop some hints of what's in store for the next generation of 32-bit microprocessors.

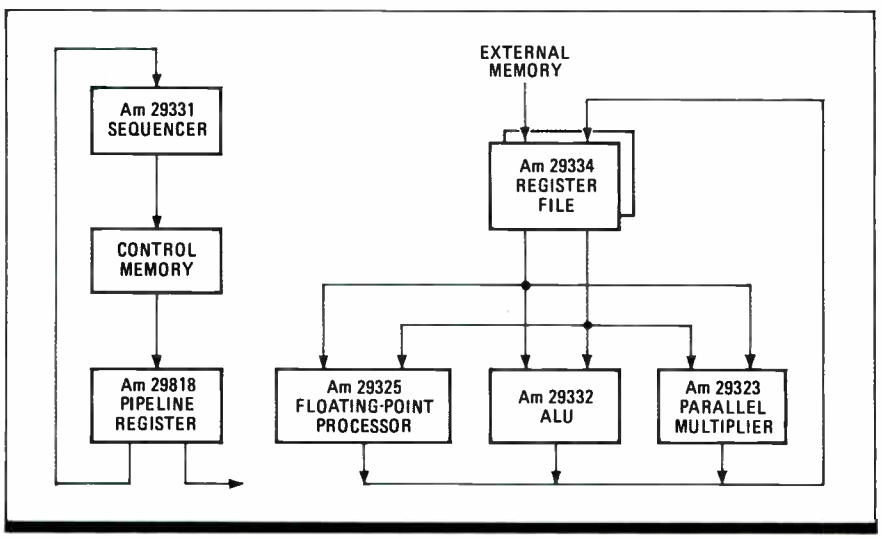
Part one of this special report, on 32-bit-slice developments, was written by Bernard Conrad Cole in San Mateo. New York-based Alexander Wolfe wrote the second part, on 32-bit microprocessor advances, beginning on page 67.

PART 1

Barely making the scene a year ago, the 32-bit microprogrammable building block, the high-end successor to the 4-, 8-, and 16-bit 2901-type bit slice, is now one of the fastest-growing portions of the 32-bit processor marketplace. Last year about this time, only one manufacturer, Advanced Micro Devices Inc., had announced such a product: its 29300 TTL-compatible family of general-purpose building blocks.

The Santa Clara, Calif., company expects to be in production by the end of this year not only with the 29300, but also an F10K emitter-coupled-logic version, the 29400. Both will be fabricated with the company's 1.5-μm IMOX-S bipolar process. Also due by year-end is a 1.6-μm CMOS version, the 29C300.

Others are joining the fray, however—for example, Texas Instruments Inc. with its 32-bit 74AS88XX family of bipolar and



1. THREE BUSES. AMD's 32-bit Am29300 family uses external registers and is linked by three 32-bit buses using a flow-through architecture.

CMOS building blocks. The Dallas company also expects to be in production by year's end.

Another player is WaferScale Integration Inc., of Fremont, Calif., with its CMOS WS59032, a 32-bit general-purpose building block available both as a standard product and as a cell in WaferScale's standard-cell library. Also staking a claim is Weitek Corp. of Sunnyvale, Calif., with its CMOS TTL 7000 series, aimed at use in computationally intensive numerical processing and intelligent controller applications. WaferScale's part is in production now; Weitek has just announced its chips.

This rush to production is all the more remarkable considering that the 32-bit microprogrammable building blocks currently have a virtually nonexistent share of a bit-slice market that Gnostic Concepts Inc. of San Mateo, Calif., estimates at $217 million this year. "Barely above the noise level," as John Rizzo, Weitek's vice president of marketing, measures it. But Weitek and the other chip makers expect the 32-bit-slice market to grow rapidly, to $300 million to $500 million by 1990, approximately half of all bit-slice sales they expect for that year.

One reason for this remarkable growth is a move toward more sophisticated architectures in high-performance superminicomputers and supercomputers, which are a traditional centerpiece in the bit-slice market, observes Christopher King, AMD's 29300/2901 product marketing manager.

Also, as much as 20% of the high-performance digital signal-processing applications—long a main source of sales for general-purpose bit-slice components—will remain the domain of these microprogrammable building blocks, King adds. That's despite the fact that a majority of such applications are moving to single-chip DSPs such as TI's 32020.

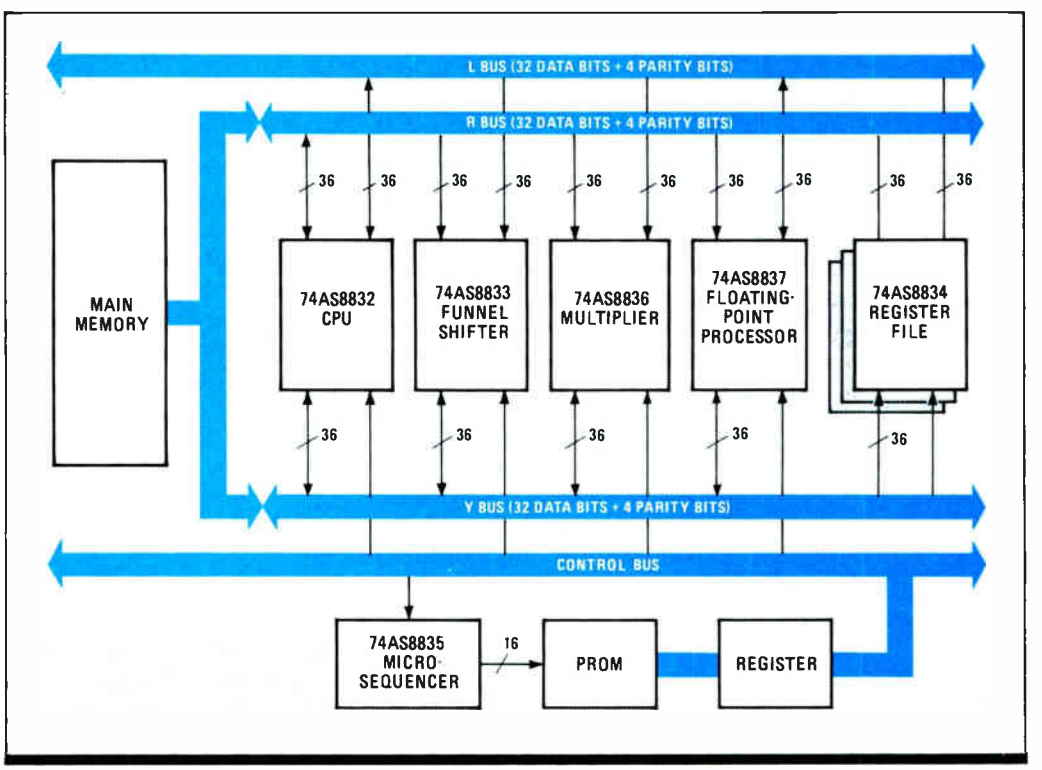
But fueling most of the growth, says Weitek's Rizzo, are such applications as industrial automation, communications, graphics, robotics, peripheral controllers, avionics, and military and other sophisticated controllers. These applications need such features as 32-bit word lengths, fixed-instruction words, high speed and low power, multiply and divide capabilities, internal data storage, bit/byte/word data types, multiple interrupts with fast response and powerful bit shift, mask/merge, and other bit-manipulation capabilities.

Scarcely out of the starting gate, the participants are jockeying for position, attempting to divine the needs of the diverse users and evolving architectures that diverge in a number of fundamental ways from that of AMD's pioneering 2900 4-bit-slice family. That line has vertical partitioning, in which the register file memory and arithmetic logic unit are combined in a single package; the ability to cascade and on-chip carry-lookahead logic; and the use of a bidirectional bus structure for increased flexibility in design.

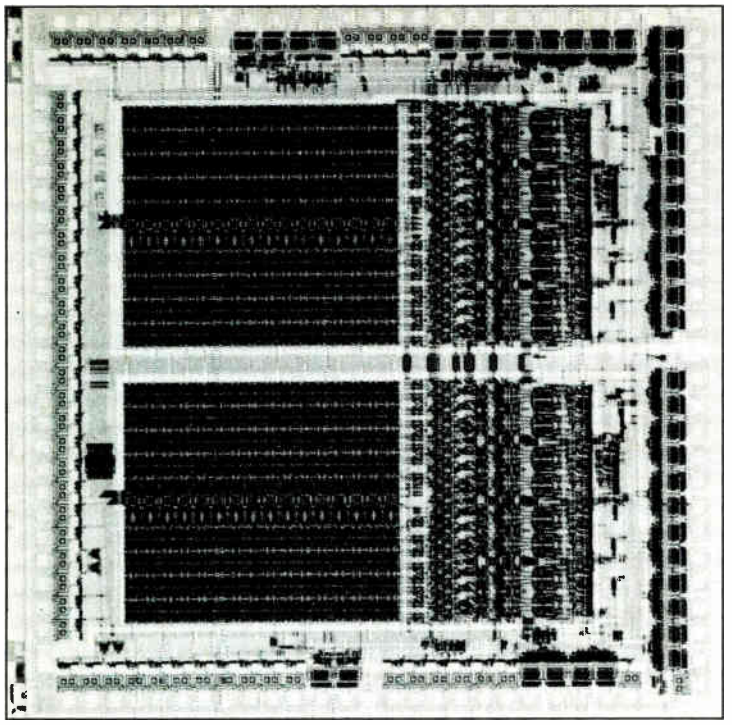
AMD CHANGES COURSE

Suprisingly, one of the companies to diverge most radically from this original architecture is AMD itself, with its 29300 family (Fig. 1). The line includes the Am29331 microprogram sequencer, the Am29332 integer-processor ALU, the Am29323 parallel multiplier, the Am29334 register file, the Am29325 floating-point processor, and the Am29818 pipeline register. AMD is betting that the 32-bit-slice market won't overlap with the 4-bit-slice market, and so cascadability and code-compatibility with the 2900 family won't hobble the 29300 and 29400 families.

The main divergence from the 2900 family is the use of horizontal partitioning, with the register file separated from the rest of the datapath elements. King says that separation has two advantages: it offers an easily expandable register file space, and it enables arithmetic



2. FOUR BUSES. TI's 74AS88XX 32-bit-slice family incorporates registers onto the ALU chip and communicates over four buses.



3. 2901-COMPATIBLE. WaferScale's WS59032 contains 32 registers, eight 4-bit 2901-type ALUs, and carry-lookahead logic. It is microcode-compatible with the 2900 family.

accelerators to be added to the data path.

A major disadvantage of the original 4-bit-slice architecture is that much time is lost in transmitting carries from one chip to another. To avoid this, the Am29300 family has full 32-bit data paths. That not only speeds up data transfers, but allows inclusion of functions that are not easily sliced. For example, multipliers and shift arrays require an unacceptable amount of data to be transferred between slices.

AMD is alone in switching to a new horizontal-slice architecture for 32-bit building blocks; other makers are keeping the AM2900's vertical-slice configuration

To take full advantage of the 32-bit internal data paths, AMD has eliminated the bidirectional or shared input/output approach and opted for a three-bus flow-through architecture, with two input buses and one output bus. "The advantage of this approach lies in its simplicity," says King. "It allows the designer to tailor the system's register file to the specific application, rather than forcing the use of a fixed, more general memory organization."

But the horizontal architecture AMD uses in its 29300 family presents a major problem, argues Christopher Demonico, bit-slice strategic marketing manager at TI. It forces the user who has been designing with smaller, word-sized bit slices to throw out microcode that's been years in the writing and develop totally new code.

TI has retained the vertical-slice architecture by combining a 64-by-36-bit register file and a 32-bit ALU into the same part, the 74AS8832 microprogrammable central processing unit. The new chip retains microcode compatibility with TI's 74AS888 8-bit-slice family. Moreover, unlike the AMD CPU, whose word length is fixed at 32 bits, TI's device can be configured as four 8-bit ALUs, two 16-bit ALUs, or a single 32-bit ALU.

The two companies also differ on such functions as funnel and barrel shifting. The Am29332 incorporates them on the same chip as the ALU. But in the TI approach, the two functions are separate ICs—the 74AS8833 and 74AS8838, respectively. Other family members include the 74AS8834 register file, the 74AS8835 microsequencer, the 74AS8836 32-bit multiplier, and the 74AS8837 floating-point processor.

For overall bus architecture, Demonico says, TI has attempted to combine the best of the vertical- and horizontal-slice worlds (Fig. 2), with three bidirectional I/O buses, each accommodating 32 bits of data and 4 parity bits, and a fourth control bus that transfers the microword from the microsequencer block to the other processing elements for execution. This gives the designer the option of setting up either multiport memory communication or time sharing of the buses to system-wide single-port memory, Demonico says.

AMD has opted for separate processes for its different bit-slice families, but TI mixes process technologies. It fabricates the 32-bit multiplier and floating-point processor in 1-μm CMOS and the other devices with its 1.5-μm Impact-X bipolar process [*Electronics*, Dec. 23, 1985, p. 56].

While TI considers the horizontal approach to be a problem in AMD's products, WaferScale Integration pegs the lack of cascadability and of microcode compatibility with its 4- and 16-bit predecessors as weak links in the 29300 family. So WaferScale has taken aim with its 1.2-μm CMOS WS59032 (Fig. 3)—the equivalent of eight 2901 4-bit-slice ALUs and three 2902-equivalent carry-lookahead units. The part also contains 32 registers to enhance throughput by eliminating many external memory fetches. Designed to be 100% microcode-compatible with the 2900 family, the WS59032 can also be cascaded, allowing it to emulate almost any 4- or 16-bit computing system based on a 2900-type bit slice, says director of marketing Dale Prull.

In contrast to other vendors' presentation of their 32-bit building blocks, WaferScale also offers the WS59032 as part of its Probe cell library, which includes cells that are functionally equivalent to AMD's 2904 status and control unit, 2909 microprogram sequencer, and 2913 priority interrupt expander. In addition, the Probe library has such support cells as expandable random-access memory and erasable programmable read-only memory, as well as a variety of medi-

um- and small-scale macrocell functions such as inverters, buffers, NANDs, flip-flops, and latches.

In developing its 32-bit-slice family, Weitek's approach is to offer specific architectural and algorithmic solutions to particular applications problems. For example, the WTL7137 integer processor (Fig. 4) is targeted at numeric and controller applications, and so it combines a 32-bit ALU with a four-port register file, a field merge unit, and independent multiply and divide units.

The WTL7136 sequencer-controller incorporates such features as a 32-bit code address space, instruction neutralization logic, code- and data-breakpoint registers, timer and status registers, and stall and abort circuitry to allow connection to variable-latency memory systems such as caches and static-column-mode dynamic RAMs.

Weitek also offers the 64-bit double-precision WTL2264 floating-point multiplier/divider and the 32-bit WTL2265 floating-point ALU. All four parts are fabricated in 1.5-μm CMOS.

FLEXIBLE BUSES

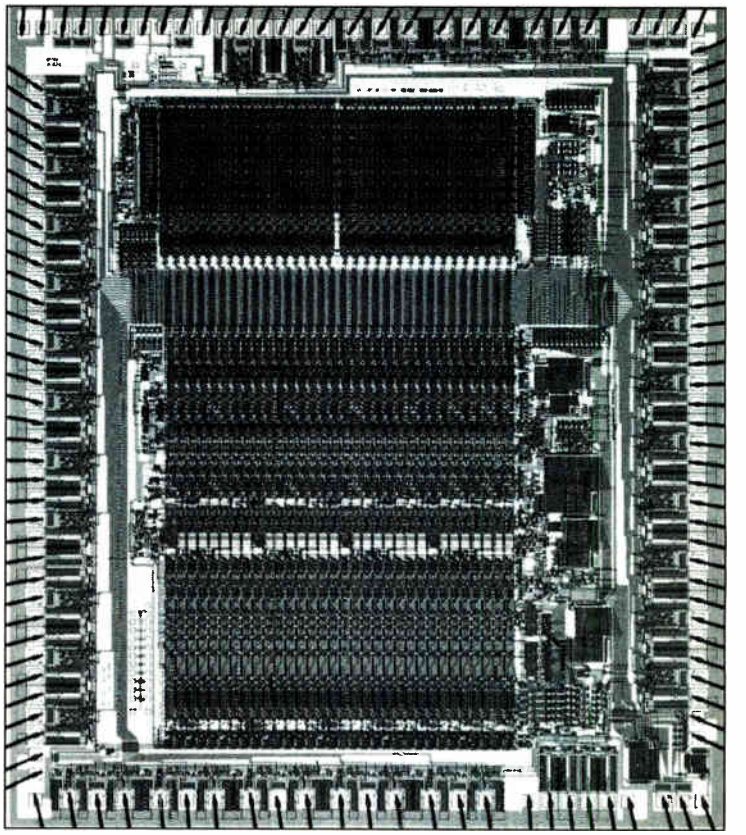
Weitek's approach to bus implementation has to be as flexible as possible, with one bus for code transfers between the sequencer, the integer processor, and the floating-point processor. A data-bus arrangement allows the parts to be linked via two bidirectional buses, a single bidirectional bus, or one input and one output bus.

Though these chips offer users a broad choice, several more players are targeting particular market sectors. One is Analog Devices Inc. of Norwood, Mass. In January, it introduced a 32-bit microprogrammable floating-point ALU, the ADSP-3220, aimed at numerical, or array, processing and digital signal processing. It also introduced the ADSP-3210, a 32-by-32-bit floating-point multiplier.

Scheduled for introduction later this year from Integrated Device Technology is the IDT49C404, a 32-bit bit slice containing a 32-bit ALU, a 64-by-32-bit register file, a cascadable funnel shifter, priority encoder, merge logic, and a mask generator. The part will be built in the Santa Clara company's bipolar-optimized CMOS process.

Also planning to enter the market with families of 32-bit microprogrammable building blocks are Fairchild Semiconductor Corp. of Cupertino, Calif., and Integrated Device Technology Inc., of Santa Clara. Fairchild will offer a microprogrammable DSP building-block family, probably built around Aspect, its new 2-μm contactless process (see p. 55), or with a BiMOS process still under development [*Electronics*, March 3, 1986, p. 27].

Four other companies also likely to be seriously considering participation in the 32-bit microprogrammable building-block market are Logic Devices Inc., of Sunnyvale, Calif., and Cypress Semiconductor Corp., of San Jose, Calif., both of which have just introduced 16-bit slice products; LSI Logic Corp., Milpitas, Calif., a gate-array manufacturer that has just introduced its first standard product, the L64032, a 32-bit multiplier accumulator; and VLSI Technology Inc., another Milpitas semicustom-circuit manufacturer.



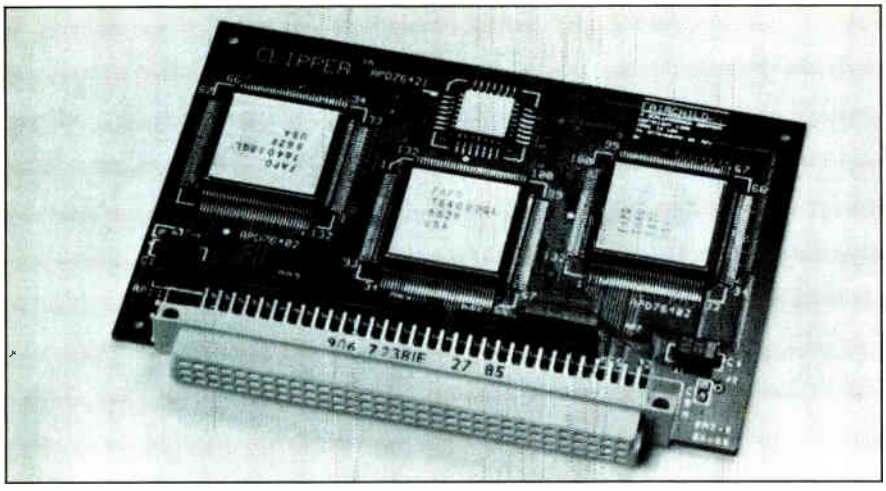
4. NUMBER CRUNCHER. Weitek's entry in the 32-bit building-block race is the WTL7137, a 32-bit integer processor with the on-chip functions needed in numeric and controller applications.

Many of these newcomers are expected to focus on the lucrative DSP market in their initial offerings. In doing so, they will have to take into account the fact that AMD is protecting its flank. Not only has it included a floating-point processor, the 29325/29C325, as part of its 29300 32-bit-slice family, but it also has introduced the 29500 family of microprogrammable DSP building blocks, including the 32-bit 29501 multiport pipelined processor.

PART 2

Although 32-bit microprocessors are now readily available, semiconductor manufacturers are not letting the technology sit still. They're increasing the chips' clock frequencies, offering improved software tools and emulators, and supporting the Unix operating system. In a highly competitive marketplace, such attention to technical features that make the chips easier to use is seen as the way to win the hearts and minds of potential customers.

Of all specifications, the one most closely followed in the 32-bit world is clock frequency. And Fairchild Semiconductor Corp., Cupertino, is



1. CLIPPER CHIPS. Fairchild's three-chip Clipper 32-bit microprocessor module is being introduced in a 40-MHz version featuring a top execution speed of 6.5 mips.

readying a 40-MHz version of its Clipper 32-bit microprocessor chip set. With the new frequency, the Clipper's top execution speed rises from the 5.0 million instructions/s of the initial 33-MHz chip set to 6.5 mips. The three-chip set is mounted on a printed-circuit board; the package is called the Clipper module (Fig. 1).

The Clipper features a streamlined instruction set that offers the execution speed of a reduced-instruction-set computer without sacrificing floating-point number-crunching power. Dual pipelining—an ALU pipeline can operate concurrently with the CPU pipeline—is another key speed-enhancing architectural feature. The 40-MHz Clipper will be available in the second quarter of 1987.

Motorola Inc. also recently topped its highest 32-bit frequency, 20 MHz, with the introduction of a 25-MHz MC68020 (Fig 2). The higher clock speed

Clock speeds are climbing above 20 MHz, and enhancements such as pipelining are also boosting instruction execution in the newest 32-bit microprocessors

was attained with a 1.5-μm HCMOS manufacturing process and a single metal layer with polysilicide. The 25-MHz MC68020 can execute 5 mips of sustained throughput and 12.5 mips in burst mode. That performance comes from the increased clock frequency, added on-chip instruction caching, and three-stage instruction pipelining. A completely new 32-bit microprocessor, dubbed the 68030, is rumored to be in the works.

Motorola is also introducing a 25-MHz MC68881 floating-point coprocessor. The chip is typically incorporated into 68020-based systems to boost number-crunching performance. While the 16-MHz MC68881 was benchmarked at 1.2 megawhetstones (whetstones are a standard floating-point yardstick), the new chip should top out at approximately 1.7 megawhetstones, Motorola estimates. Motorola representatives say there will be introductions in the 32-bit area in the fourth quarter of this year.

National Semiconductor Corp. offers 15-MHz versions of its full Series 32000 family. The NS32332, the top of that line, offers full 32-bit external-address and data-bus widths. The Santa Clara, Calif., company has not yet announced plans for faster versions, but "certainly 20 MHz is not beyond the realm of possibility," says marketing manager Anil Uberoi. If National announces a faster speed, it will release upgrades for the entire Series 32000 line, says Uberoi.

In addition, the chip maker will add technical enhancements to the current 32-bit architecture. Improved microcode and additional on-chip pipelining to increase chip throughput by 30% to 40% at the same clock frequency are on tap. At the same time, the company plans to introduce a new 32-bit microprocessor, which will become the top of the line in the Series 32000. Designated the NS32532, it will operate initially at 20 MHz and will become available by mid-1987.

But National argues that clock speed cannot be the sole standard by which 32-bit microprocessors are judged. "Beyond clock speed, the thing that leverages a microprocessor's performance most strongly is compiler performance," says Uberoi.

For the Series 32000, National now offers an optimizing compiler available with both C language and Fortran 77 front ends. These front ends generate a semantic-tree representation of the input code. The compiler's optimizer, using a technique called "coloring," then replaces complex semantic structures with simple semantic structures that perform the same function. From this simplified tree, the optimized output code is generated.

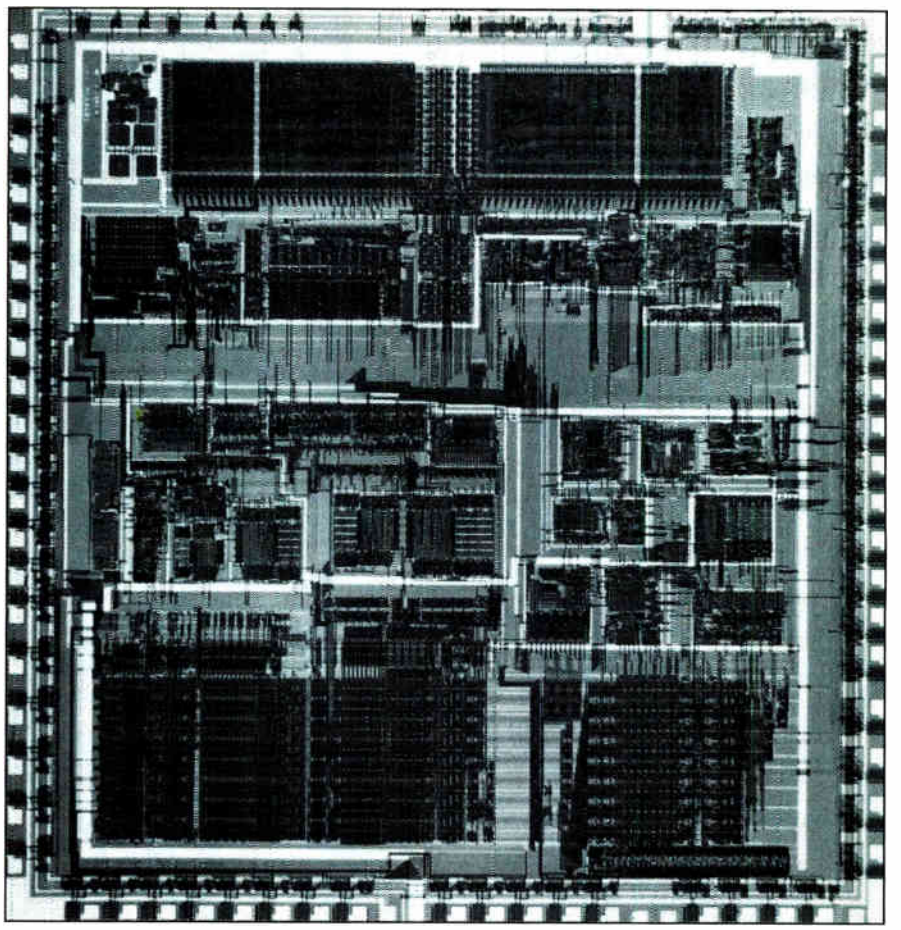
Increasingly, such software tools are playing an important role in the 32-bit market. "People buy these microprocessors for just one reason—to get software," says Bob Freund, National Semiconductor's Series 32000 development systems and software group director. Where hardware performance among competitive chips is roughly equal, users will go where the accompanying software environment and development tools allow the greatest productivity in terms of getting their design to market quickly.

Another important attribute for 32-bit microprocessors, National believes, is the ability to run AT&T Bell Laboratories' Unix operating system. National now supports the new Unix System V Release 3.0 [*Electronics*, June 16, 1986, p. 15] for the Series 32000 chips. And compatibil-

ity with Unix's file-format standard allows users to take files developed on one system and execute them on another. "Instead of coming up with our own file-format standard, we adopted AT&T's common-object file format," explains Freund. Motorola also says it has internally demonstrated a chip that runs Unix System V Release 3.0.

For 32-bit microprocessor users looking to get right down to developing software, the single-board computer may be the way to go. That approach bypasses the four to six months it typically takes to design a system from scratch. Intel Corp.'s 80386-based single-board computer is likely to find a home in high-end work stations, predicts Gordon Reid, marketing manager for the Santa Clara, Calif., company. "That's where the pressure for performance has been the highest," he says.

Going with a ready-made board allows work-station manufacturers to concentrate on developing the software for their new machines. "One of the things to understand in a make-versus-buy decision is that it's hard to differentiate the hardware [from other manufacturers' designs]—the differentiation is in the applications software," Reid explains.



2. SPEEDUP. Motorola boosted the speed of its MC68020 to 25 MHz using a 1.5-μm HCMOS manufacturing process and a single metal layer with polysilicide.

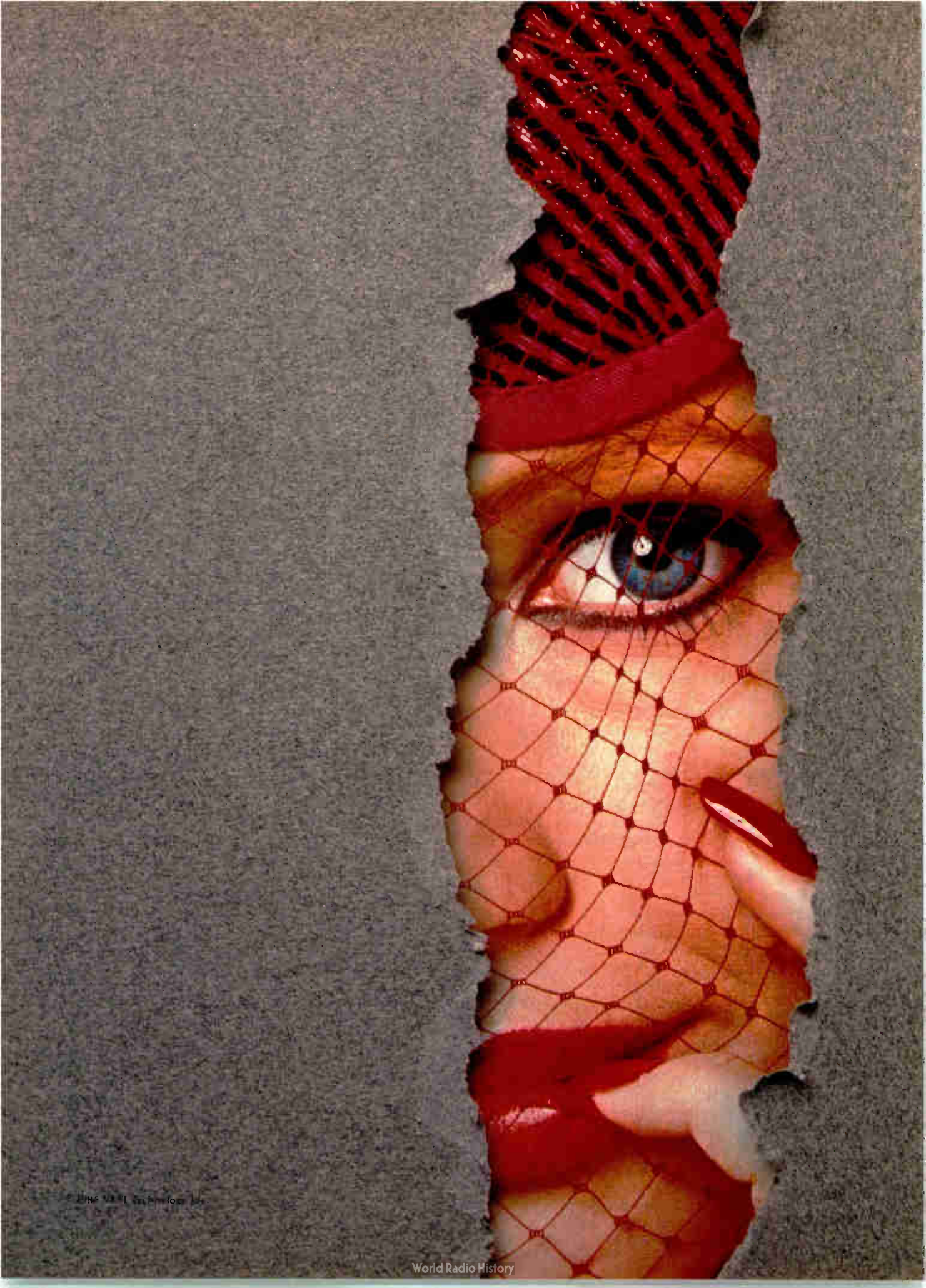
To help develop that software, Intel offers a range of development tools, such as compilers, linkers, and debuggers. But these tools work in an environment that has changed dramatically over the past several years. "The old 'blue box' [Intel's Series II and Series III software-development systems] started out as an individual-user work station. But the applications have become so large that an individual user on a work station is no longer effective," Reid says.

So Intel is using a local-area network to link together 80386 software developers working on a wide variety of both large and small machines. Software development tools for the 80386 can now reside on Digital Equipment Corp. VAX superminicomputers; Intel's microcomputers running the Xenix 286/310 and iRMX 86 operating systems; PC-DOS-based personal computers and work stations; and Intel's Series II, III, and IV and Model 800 software-development systems. The disparate machines are linked together with Intel's OpenNet LAN. Such high-powered computing hardware lets engineers develop software at their desks. And in the laboratory, the debugging and testing can proceed on the software-development systems.

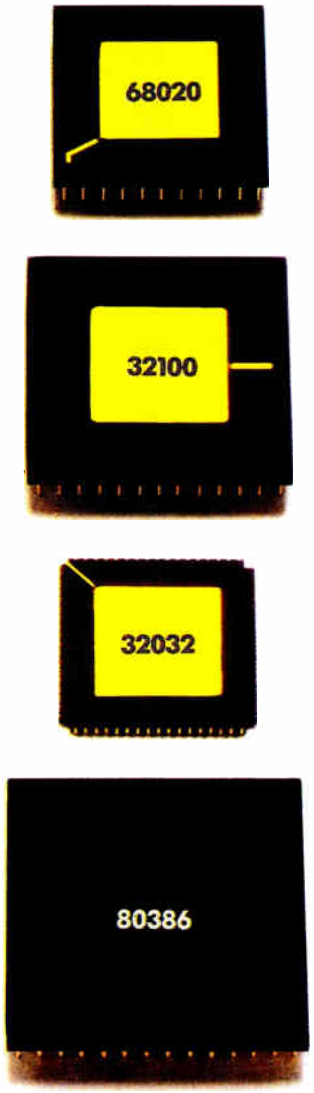
On the military front, National Semiconductor makes much of its work with Sandia National Laboratories to develop radiation-hardened versions of the NS32332. Because the chip is available in CMOS, it dissipates a small amount of power—roughly 300 mW on average. This makes it desirable for military applications where low heat translates into low cooling requirements. That's important because equipment on aircraft and ships is specified to run at all temperatures from -55°C to +125°C. "This will be the only 32-bit microprocessor to be radiation-hardened, so it will be the only chip for Strategic Defense Initiative applications," claims Uberoi.

As fabrication technology advances, higher levels of device integration will be possible. In the future, the Series 32000 will become part of a standard-cell library. System designers will be able to incorporate a Series 32000 microprocessor into a larger VLSI design, thus creating complete, individualized systems on a chip.

Other U. S.-based manufacturers of note in the 32-bit microprocessor field include Zilog Inc., Campbell, Calif., and AT&T Co. Zilog's Z80,000 chip is expected to go into production in the fourth quarter of this year; sampling quantities are currently available. AT&T's WE32100, aimed strongly at Unix applications, is already in production. □



State-of-the-past.



State-of-the-art.

CLIPPER™ from Fairchild. The most significant advance in microprocessors since microprocessors themselves.

Unlike the others, its performance isn't limited by an architecture designed back at the dawn of the microprocessor era. It's built from the ground up with a brand *new* architecture, for today's high-performance applications. And it's the only microprocessor that can bridge the architectural gap to true supercomputer performance.

CLIPPER. The new definition of state-of-the-art.

How the competition wishes they'd done it.

In a highly integrated three-chip set, you get an architecturally advanced, very high performance, CMOS 32-bit compute engine, optimized for scientific and professional computing applications in the UNIX® operating system environment. In fact, you get everything in the three CLIPPER chips that it takes the competition's entire CPU board to give you.

Designed for high bandwidth and true concurrent execution of instructions, CLIPPER runs at 33 MHz. Which, until we proved otherwise, was considered impossible. CLIPPER achieves a peak execution rate of 33 MIPS, with average performance greater than a VAX™ 8600 – twice as fast as any other microprocessor in existence, five *times* as fast as a VAX 11/780. And floating-point performance exceeds 2 MFLOPS, while simple instructions execute in a scant 30 ns.

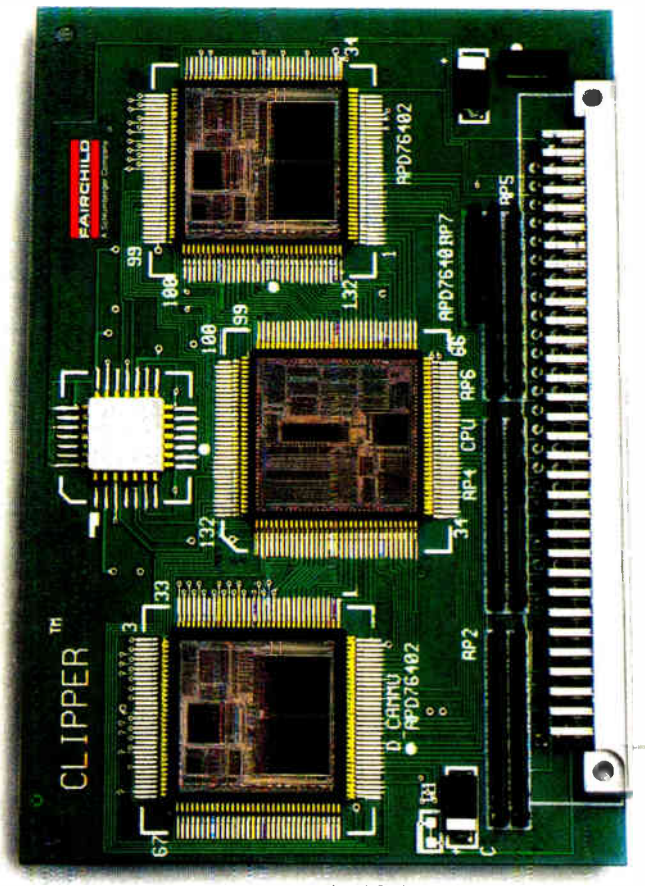
Supercomputer technology on a chip.

Unlike any other microprocessor architecture, CLIPPER uses proven supercomputer and mainframe architectural concepts.

Such as extensive pipelining. An on-chip floating point unit processing in parallel to a three-stage, pipelined integer execution unit. Two 32-bit buses, one for instructions, one for data, delivering up to 133M bytes per second to the CPU, eliminating bandwidth as a performance bottleneck.

Two large 4K-byte cache/memory management units (CAMMUs) provide mainframe-style, copyback caching concurrent with virtual address translation.

Then there's our Streamlined Instruction Set. With 101 instructions hardwired instead of microcoded for performance. There's also a macro-instruction unit, providing 67 high-level instructions and system functions. For all the advantages of RISC and the robustness of a CISC.



Actual die size approximately 440mil. x 440 mil.

What got into CLIPPER.

Residing on a 3.0 x 4.5-inch printed circuit card, the CLIPPER three-chip module includes a pipelined CPU with an on-chip, IEEE-standard FPU, and two 4K-byte cache/memory-management units. A clock generator completes the package, adding up to a staggering total of 846,000 transistors.

How CLIPPER backs you up.

CLIPPER is supported by a powerful software environment. Including a port based on the UNIX System V operating system. Optimized FORTRAN, C and Pascal compilers. Plus numerous utilities.

Or you can choose a complete VAX cross-support package.

And you're further supported by our application engineers and system designers. Each of them experts on CLIPPER.

For more information on the most advanced microprocessor since the advent of microprocessors themselves, just give us a call. You'll find us at The Fairchild Customer Information Center, 1-800-554-4443.

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THIS SUPERCOMPUTER ALSO RUNS VAX/VMS PROGRAMS

With its new software, the Elxsi 6400 minisupercomputer runs applications from the most popular computing environment for engineering and scientific installations

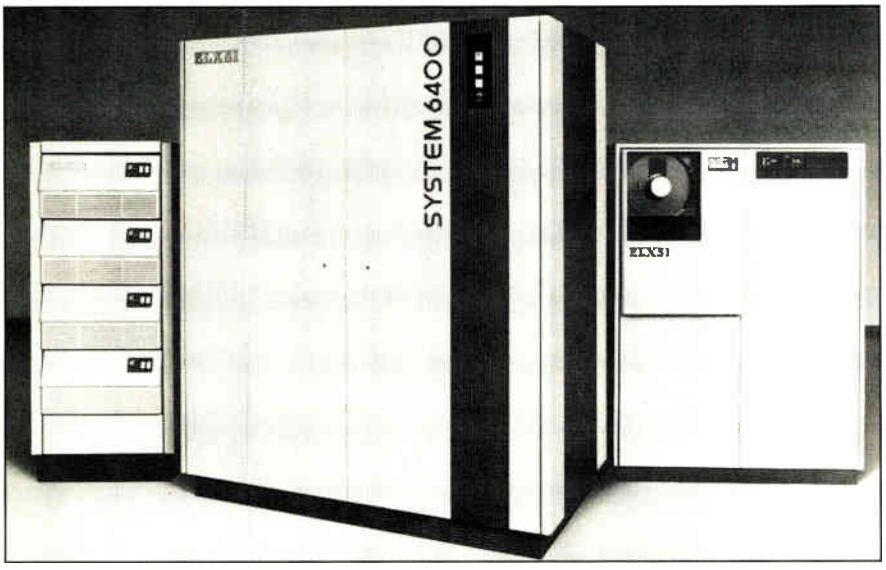
A supercomputer can bring superheadaches to users unfamiliar with such an exotic machine—but not if it looks like the most popular system in engineering and scientific computing. That's why Elxsi is blazing a new trail with its System 6400 64-bit multiprocessor minisupercomputer (Fig. 1). It is announcing a four-package bundle of software, called EMS, that, along with a few operating system enhancements, is designed to make the System 6400 compatible with the popular VMS operating system used on Digital Equipment Corp. VAX superminicomputers.

The new Elxsi software for the 6400 gives VMS users a way to easily increase the capacity of their computing installations. With its fast new processor [*Electronics*, July 24, 1986, p. 22], the 6400's throughput is expandable way beyond the top machine in the VAX line—up to about 80 million instructions per second, or roughly six times the top-of-the-line VAX 8800, according to Elxsi.

The VMS-compatible EMS software represents a major strategic thrust for Elxsi. The San Jose, Calif., subsidiary of Trilogy Ltd. thinks that EMS will propel its machines into the many VAX/VMS shops, either as a computation and device server for VAX-based networks or as a VAX replacement for users accustomed to VMS. VMS compatibility will also make the Elxsi system a more attractive target for third-party software and will make it much easier for software vendors with VMS applications to produce Elxsi 6400 versions of their products.

In almost every significant engineering discipline, the major computer application programs run on VMS. This has resulted in most large engineering organizations building their computing environments around the VAX/VMS environment and training many programmers and users how to use it.

Elxsi does not intend to provide a VAX plug-compatible processor. In-



1. VERSATILE MACHINE. The System 6400 minisupercomputer from Elxsi now can run software designed for VAX/VMS computers.

stead, it is extending its proprietary Embos operating system and adding new software to provide VAX/VMS compatibility without losing any of the features of the 6400 system architecture. "We gain our technological advantage over the VAX through fundamental architectural differences all through the software and hardware," says Robert Olson, director of software development. "For example, we can allow EMS, Embos, and both flavors of Unix [AT&T System 5 and Berkeley 4.2] to run simultaneously through what is in essence a virtual machine approach."

Besides the changes to Embos, EMS includes four software products to emulate a VAX computer more closely than does any other computer, according to Elxsi. The first three packages, to be available in September, are ECL, which emulates the Digital Command Language (DCL) interpreter; ERT, which provides the VMS system services and run-time library; and an editor that is compatible with the VMS EDT editor. The Elxsi 6400 already has VMS-compatible Fortran.

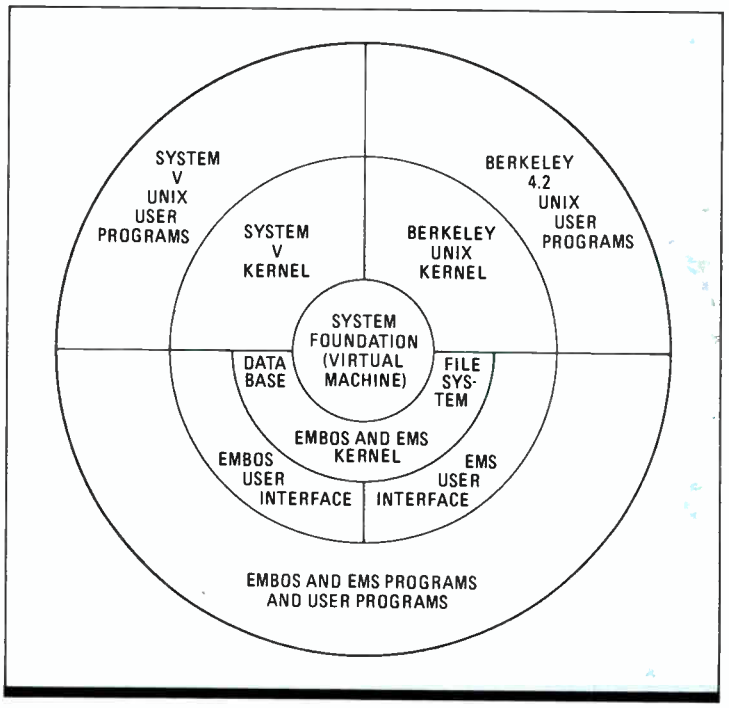
Elxsi will add the fourth new support package by the first quarter of 1987. It will be a package called Community that emulates the DECnet Phase IV end node. With it, the System 6400 can communicate with VAX machines over an Ethernet-DECnet lashup. Many customer sites use DECnet as their primary communications technology, and those users will be familiar with the DECnet commands.

Experienced computer users know how difficult it is to switch back and forth between different user interfaces that have different names for the same function. In reality, many users will simply refuse to use two different operating systems. With the VMS environment provided by Elxsi's EMS, users familiar with VMS will not have to learn another operating environment to use the System 6400.

THE STARTING POINT

To develop EMS, the Elxsi engineers decided to keep everything they had. They modified and extended Embos rather than create a whole new operating system. The organization of Embos made the task simple, for it is a message-oriented operating system built out of multiple processes. These processes automatically load-balance themselves over the available central processing units, so that the operating system does not become a bottleneck causing the other CPUs to sit idle. The Embos processes are networked, with well-defined interfaces among them.

In designing the Embos processes, Elxsi closely adhered to the abstract-object model, in which service objects, such as tables and control structures, are completely encapsulated inside operating-system processes. The effect of this encapsulation is to make service objects and the applications using them independent of one another. Changes can be made to either the objects or the application software without affecting the other.



2. EASY ADDITION. The compartmentalized structure of the System 6400 lets Elxsi add EMS functions at all levels while leaving existing Embos and Unix functions virtually intact.

This highly structured organizational model made it easy to add functions at each of the levels without significantly altering existing Embos and Unix functions (Fig. 2).

The Embos command interface is very similar to the Unix shell, with its pipe and filter facilities for interprocess communication. In particular, these strong interprocess communication features in Embos provide for multiple command interpreters, even within the same job. For much of its work, the command interface simply makes requests on other operating system processes. So the EMS designers found it easy to integrate an optional command language interpreter that executes the VMS DCL instead of Embos's command language.

The interface most used by the least sophisticated VMS users is the DCL intepreter. It was here that EMS had to be most faithful to VMS. The Elxsi engineers working on ECL—their version of DCL—set a goal that all commands used on a daily basis, either interactively or in a command file, would be available with the first release. By the second release, all non-operator commands would be implemented exactly as DEC's DCL manual specified.

DCL provides a number of programming language-like features and a modest-sized command set. The first design challenge for Elxsi was to build a command interpreter that would handle the syntax and semantics of individual VMS commands. The resulting program supports VMS-style parameter specification and handling, including prompting and defaults. The program also allows command names, qualifiers, and key

words to be truncated according to the DCL rules.

ECL handles all of the complex VMS-style file names, such as version IDs, wild-card characters, and default-device, default-directory, and foreign-file specifications. It supports logical names, including the creation, deletion, and display of names and the process, job, group, and system scoping of them. Much of this support was integrated into the Embos file system in order to achieve the highest possible performance for these features. As a consequence, EMS files are accessible from Embos and vice versa.

Many builders of the most significant VMS application packages have put DCL commands in command files as an integral part of the application. This practice was an important incentive for Elxsi to provide the DCL command-file functions in ECL. These functions include batch execution, use of defined parameters and qualifiers, and the nesting of command procedures to an arbitrary depth. ECL also handles the typical programming uses of command files.

However, command files and programs written for VMS will not run on another system unless that system also supports the same run-time routines. Moreover, many, and perhaps even most, of the thousands of application programs written for the VMS operating system make use of its system services and run-time library. These run-time procedures support a wide variety of services, from asynchronous input and output and interprocess communication to simple time- and date-string manipulations.

The ERT run-time interface for programs evolved from the beginning on the VMS model—hundreds of run-time routines specialized for their tasks. Modifying the Embos file system to match VMS and to handle its run-time library was not difficult because of Elxsi's very flexible file system architecture, which is built in a layered fashion. So most of the EMS run-time library—routines to do the same things as the VMS run-time library—could be merged into Embos. The EMS run-time library either calls an Embos run-time routine if an appropriate one is available or else directly accesses the same lower-level system facilities that Embos run-time routines use.

For text editing, DEC supplies EDT, an interactive text editor very rich in functions, as part of the VMS operating system. The EMS version, called CLXCI, is a complete implementation of EDT.

Also, extensions were made to EDMS, the Embos implementation of the Ingres relational data-base manager from Relational Technology Inc., to bring it into full conformance with the VAX/VMS version. Since EDMS also runs under Elxsi's Unix, users can run data-base-management applications on the Elxsi 6400 under any of the three operating systems—Unix, EMS, and VAX/VMS—with a single user interface.

Finally, to make the System 6400 a compatible contributor to VAX networks, Elxsi engineers are busy adapting Community, a software package from Technology Concepts Inc., to Embos and EMS. This package will allow a 6400 to act as a DECnet Phase IV end node on an Ethernet. As long as that Ethernet is part of a DECnet through a gateway interconnection, the 6400 can be a fully functional member of a DECnet-based network.

With Community in place, EMS provides System 6400 users all the advantages of both VMS and the Elxsi system technology and architecture. And EMS is a response to the fact that VMS is the most successful operating system in the engineering world and therefore a de facto standard. In an era when the computer industry is entering a period of intense new interest in standardization and compatibility, that's an important plus for the System 6400. □

'NO WINDOW DRESSING,' VOWED THE EMS TEAM

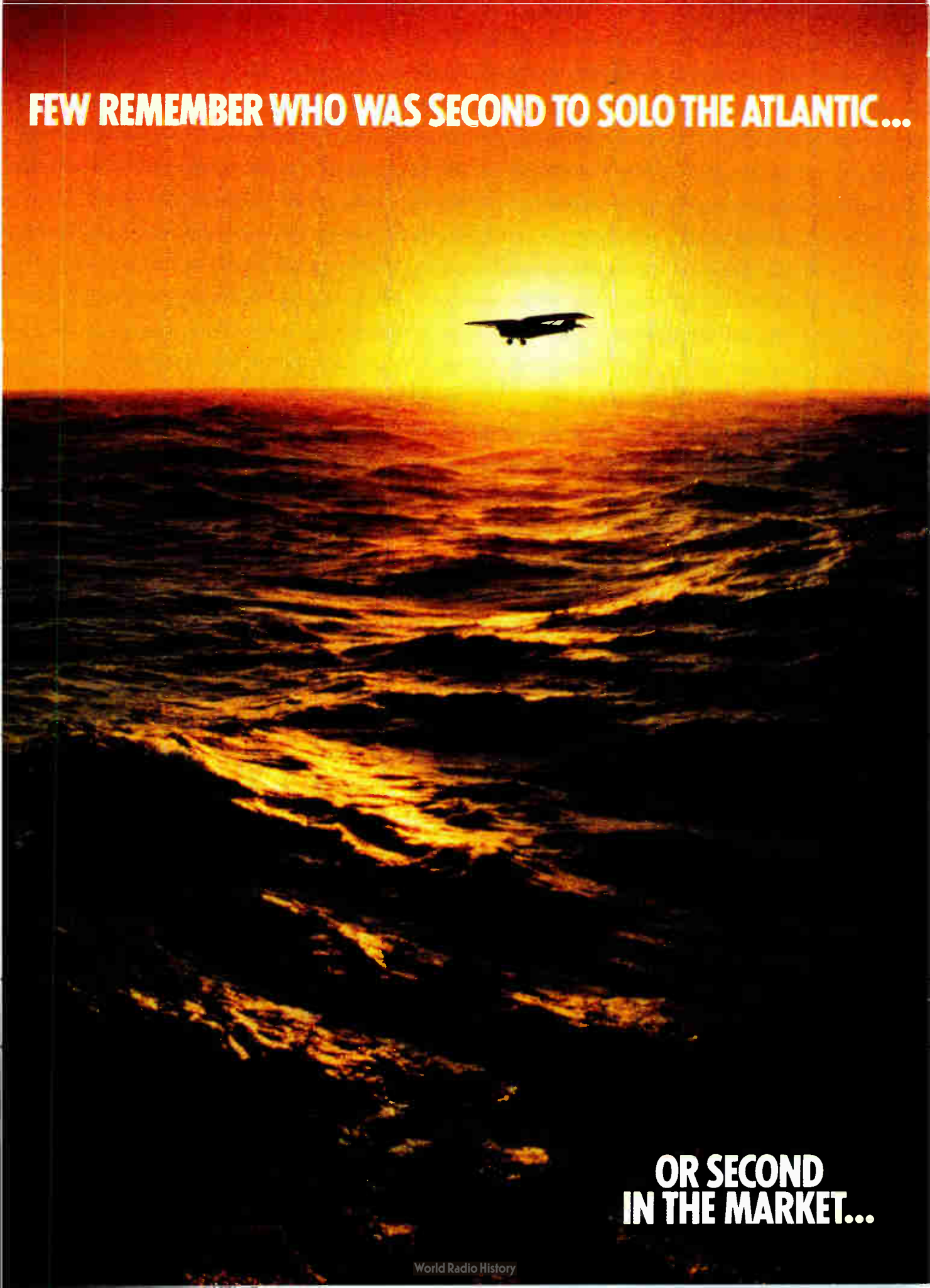
Deciding to emulate a VAX/VMS software environment on the Elxsi 6400 parallel processor was the easy part. "It was pretty clear that our customers wanted the System 6400 for its performance, easy expansion, and real-time responsiveness. But they wanted to use it in a VMS environment," says Robert Olson, Elxsi's director of software development. At first, "I thought that might be difficult, so I had the idea to make the first release just a shell with window dressing."

But his development team talked him into a set of products deeply integrated with Elxsi's native operating system, Embos. "After looking at the problems and goals for the products, the team committed itself to a better-performing and much more complete set of products in almost the same amount of time. In retrospect, they were absolutely right," says the 36-year-old graduate of Stanford University.

Olson spent nearly seven years at Hewlett-Packard before joining Elxsi in 1980 as one of the System 6400 architects. His involvement has ranged from the instruction-set architecture through compilers to his current position, where he manages the EMS and various Embos file-system and data-communications projects.

The key members of the project team were Claude Teeter, Nick Whyte, Jeff Norton and Peter Thiesen, with a number of other staff members making important contributions. Teeter is the project manager in addition to his design and implementation tasks. Whyte was responsible for adapting the Ebmos file system to VMS. Norton performed much of the other operating-system work "and kept encouraging us to get it right, not just close," says Olson. Thiesen applied his compiler background to quickly produce ECL, the command interpreter.

EMS TEAM. The Elxsi project team for the EMS software package included (l. to r.) Claude Teeter, Jeff Norton, Robert Olson, Peter Thiesen, Nick Whyte.



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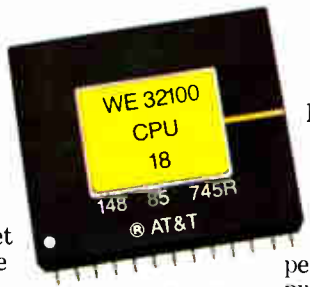

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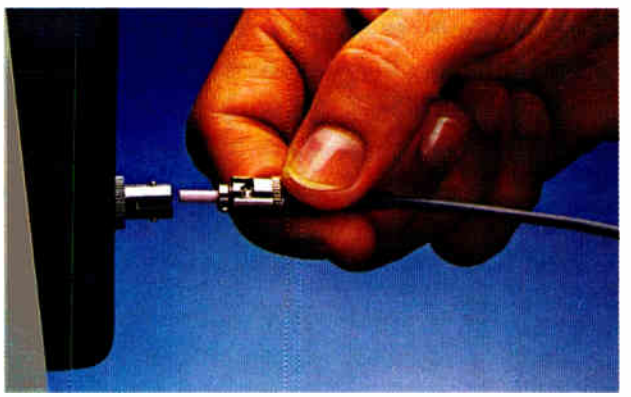

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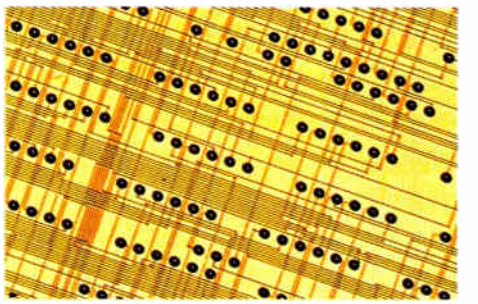

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AN ATE SYSTEM THAT CUTS THE COST OF ASIC TESTING

A new architecture yields a $700,000 system with 256-pin capability and overall ±2-ns timing accuracy in an easily reconfigured, compact package

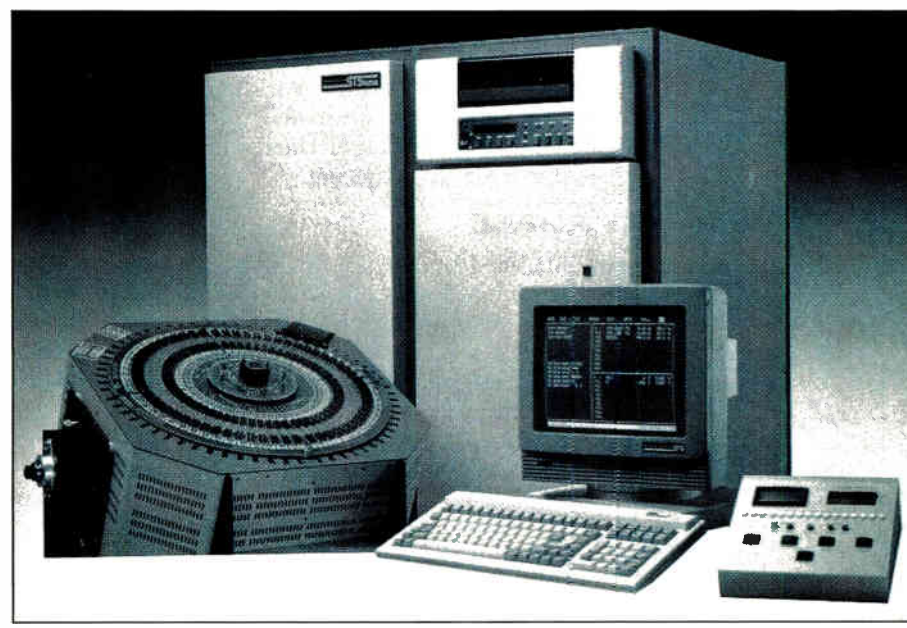
Today's high-pin-count application-specific integrated circuits are usually tested on a system designed to handle just a few types of high-volume commodity chips and costing as much as $2 million. The hefty price tag comes less from the automatic test equipment's ability to handle large numbers of pins than from its testing accuracy—but ASIC manufacturers still have had to pay for both.

But not anymore. The STS 8256 system (Fig. 1) from Semiconductor Test Solutions aims to serve those who need to test a wide variety of chips with as many as 256 pins apiece, but with a bit less accuracy. By reworking the conventional ATE architecture from the ground up, the Santa Clara, Calif., company has engineered a $700,000 system with a flexible timing-pattern generator and programmable functions that let the user easily reconfigure it to switch from testing one type of integrated circuit to another.

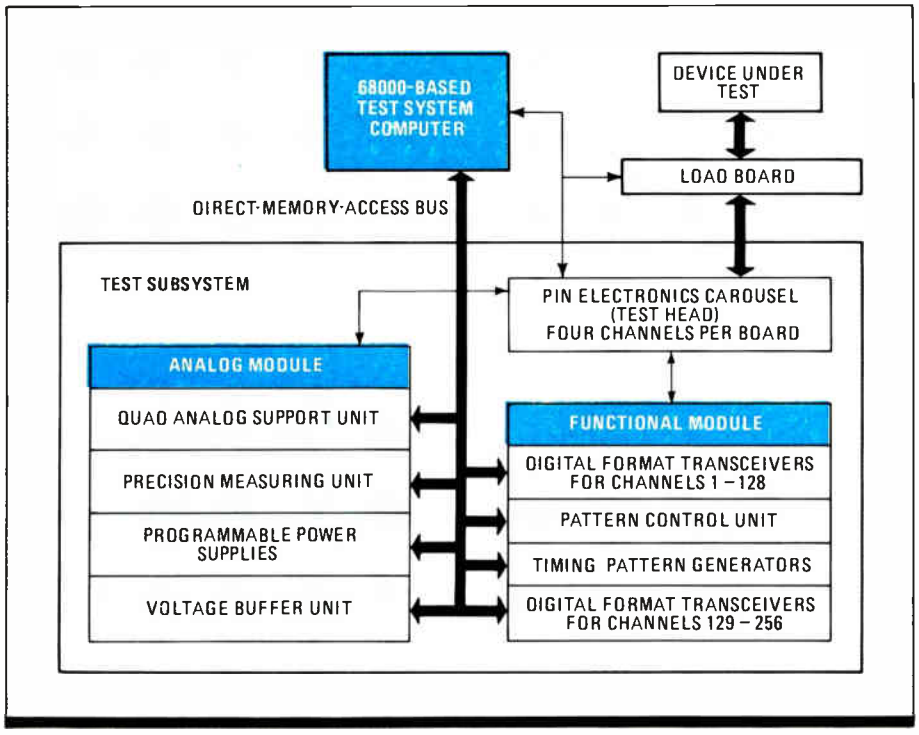
"There is a market for a product in between the high-pin-count, high-accuracy, million-dollar testers and the low-end, 120-pin commodity testers selling for around $500,000," says Al Perry, vice president of marketing and sales. "Currently, there are few if any testers that can offer 256 pins, an overall system accuracy of ±2 ns, and a 20-MHz test rate, all for about $700,000." By comparison, Genrad Semiconductor Test Inc.'s top-of-the-line GR180 offers 750-ps accuracy and a 120-MHz rate for a base price of about $1 million [*Electronics*, May 19, 1986, p. 49].

"What was required was a whole new modular architecture aimed at providing a high pin count with reasonable performance in a system that does not fill an entire room with 10 to 15 racks of printed-circuit boards," says project manager Gregory Illes. The STS 8256 is completely contained in two 19-in. racks.

The 8256's architecture (Fig. 2) consists of a computer system, a functional module with test-pattern and timing-generation elements, an analog module with dc parametric test components, and the test head itself. The functional and analog modules are partitioned differently than in conventional ATE. The Semiconductor Test Solutions designers evaluated each element in the modules to determine whether it could be shared or whether separate ele-



1. COMPACT TESTER. Though it includes all the circuitry needed to test 256-pin ASICs, the STS 8256 system is completely contained in two 19-in. racks.



2. FAST LINKS. A DMA bus links the system computer to the analog and functional test modules. High-speed cables connect the two modules to the test head.

ments had to be provided for each test pin. They then aimed to share as many resources as possible to keep the cost low. This modularity also makes it easy to expand the system.

The computer, for example, serves all other system elements. Built around the Motorola MC68020 32-bit microprocessor, it is used to develop a test program, compile the program into test vectors, or patterns, and then load the vectors into the high-speed test components.

To compile test vectors, the computer first needs a program. As one option, users can write these in Factor, a well-known vector-generation language. The 8256 also accepts test programs created by many chip-design systems. Work stations that use the Transmission Control Protocol/Internet Protocol can send files of these vector sets to the tester over an Ethernet.

FUNCTIONAL MODULE

After compilation, the test electronics control inside the computer ships stimulus vectors and control words over a direct-memory-access bus to the functional module. Vectors arrive at the digital format transceivers, and control words at the pattern control unit. Also part of the functional module is a set of four timing pattern generators. After the functional module applies test vectors to the device under test, the pattern control unit looks for responses on the DMA bus.

In order to apply test patterns and receive response data directly from each pin of the device under test, the 8256 provides one digital format transceiver per chip lead. Each of the 32 transceiver boards in the 256-pin tester contains drive and sense circuits for eight tester pins. Adding the capability to test more pins is simply a matter of adding transceivers.

Each test pin is backed by 4-K of random-access memory that holds either the test vectors or the device's response, if the pin is configured to sense the chip output. The more memory behind each pin, the faster the tester can run, because storing a large number of test vectors reduces requests for more patterns from the central processing unit. Each pin's RAM can be expanded with an extended vector memory board. Initially, an additional 500-K of RAM per pin will be available. Later, SMS will expand add-on memory to 2 Mb per pin.

The 4-K of test data in the digital format transceivers are applied to the chip's pins under direct control of the high-speed pattern control unit. At the heart of the test system, the pattern control unit controls the generation of timing, clock, and control signals to all the pin electronics. Only one pattern control unit is needed to service all the transceivers, however, because it supplies relatively few instructions at high speed to each.

The timing pattern generators are also shared resources. They deliver the test patterns with correct timing to the chip's input pins at up to 20 MHz. Each timing pattern generator can produce four dual-edge timing waves, for a total of 16 different waveforms.

FLEXIBILITY FEATURES

The timing pattern generators make it possible for the 8256 to stimulate and test a wide variety of ICs. First, it lets the engineer specify waveforms across the boundaries of a cycle, the time required to apply one stimulus pattern to all input pins of a device under test, and to receive a response from all output pins. To do this, the engineer programs the position of a waveform's rising and falling edge within a test cycle. He can specify that the rising edge begin in one cycle and the falling edge in the next.

Second, the timing pattern generators let the engineer program up to 16 different sets of 16 dual-edge timing waveforms in high-speed RAM before the start of a test. Having multiple sets of waveforms means that the engineer can program the timing pattern generators to switch timing to any pin on the fly. In one cycle, he can use the waveform in set 1, set 2 in the next cycle, set 14 in a later cycle, and so on.

The analog module performs all dc current and voltage measurements as well as providing

reference and dc power supplies, automatic de-skew adjustment, and programmable loads. The analog module comprises a quad analog support unit, programmable power supplies, a voltage buffer unit, and a precision measurement unit. All are shared resources.

The automatic de-skew and programmable load functions are new to testers in the 8256's price range. Skew is the amount of time separating the first and last tester pin to rise when a pulse is simultaneously applied to all pins. On lower-priced testers, de-skewing is usually a manual operation that takes one to two hours a month. It is always subject to technician error. The automatic compensation keeps the skew of all pins in the pin electronics to less than 500 ps.

The 8256's programmable-load feature replaces the switching relays found in most existing test systems. The loads for each pin are located in the test head's pin electronics.

"The quad analog support unit can change the loads to each test pin dynamically as a test is occurring," says Illes. "Not only does this reduce test time, it also reduces the number of different tooling setups required to test a variety of different ASICs by a factor of 10. In addition, the programmable-load feature allows many more types of devices to be tested than can be done with relays alone."

Finally, the programmable loads can be used to perform short- and open-circuit testing. Testing all pins for opens and shorts can be speeded up by a factor of two.

Power supplies are also programmable and serve the precision measurement unit as well as the test head's pin electronics. There are reference supplies for both the analog drivers and receivers. Users can program supplies to produce a voltage swing between –2 to 16 V with a 4.0-mV resolution and accuracy of ±0.1% +1 least significant bit. Most other testers produce a swing of only –2 to 8 V. The larger swing means that high-voltage CMOS and military parts can be tested at the high end of their operating voltage range.

A 12-bit analog-to-digital converter with 1 bit of positive or negative sign converts the supply output to a digital value that is read by the tester CPU. A programmable current comparator is also provided as an overcurrent shutdown mechanism.

The precision measurement unit provides voltage and current force and measurement capability. To do so, it uses the programmable power supplies and the high-current supplies in the voltage buffer unit. It can force or measure up to 131 V with a resolution of 32 mV and an accuracy of ±0.1% +1 LSB. In addition, it can force or measure from ±4.096 μA to ±131.072 mA of current with a resolution of 32.0 μA and an accuracy within ±0.1% +1 LSB. Fast ADCs perform analog voltage and current measurements.

Unlike the analog module, the test head's pin electronics are replicated for each pin to be tested. To cut costs, the designers doubled the number of pin electronics circuits on each board in the test head from two on an earlier system to four.

One function in the test head that is replicated for every pin is the comparator circuit. The 8256 tester compares expected response with actual response right at the test head. An error is detected as it occurs. On other test systems, the comparator is in the test system mainframe. "Having the comparator at the test head greatly reduces the tester's error budget," says Illes. "It makes the system much more accurate."

With the 8256, Semiconductor Test Solutions has set a new price-performance mark that others will now have to match or better, Illes maintains. "Test-system manufacturers cannot simply take their $2 million system and strip it down to achieve a system such as ours," he says. □

THE CONSULTANTS WHO BECAME ATE MAKERS

Semiconductor Test Solutions Inc. began life as a consulting firm, says Gregory Illes, its fourth employee and manager of the STS 8256 project. "We started in 1979 and survived by creating programs for test system buyers who didn't have the manpower to do it themselves."

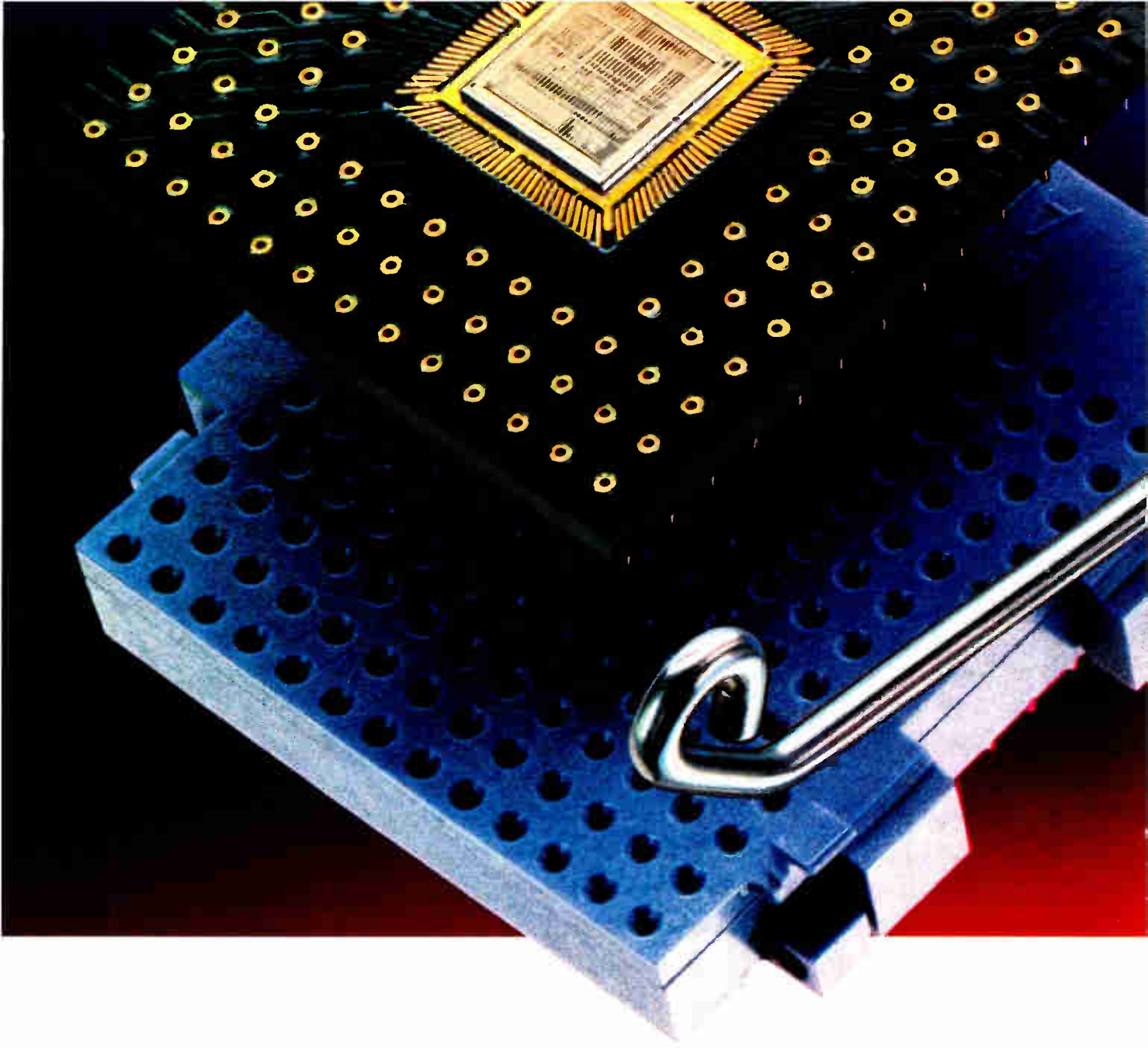
The company quickly found that automatic-test-equipment makers were building low-cost benchtop testers and $1 million-plus systems for high-volume commodity parts—and little in between. "Knowing that no manufacturer was producing a midrange system that could test smaller batches of components, we decided to build one," says David Mees, president and chief officer.

PUTTING IT TOGETHER. The STS team included (from left) Gregory Illes, president David Mees, and David O'Brian.

When STS decided that an entirely new architecture was required, Illes led the design effort. An ATE veteran, he received his BS and MS in engineering at California Coast University in Anaheim, Calif. His master's specialty was in ATE.

A team directed by software engineering manager David O'Brian wrote the all-important software to run the system. After graduating from Harvard in 1979 with a BA in physics, O'Brian journeyed west to Stanford, where he got a master's in applied physics. He came to STS as a contract programmer in 1981 and joined full time in 1983. One of his first contributions was to convert all its software to the C language.

As with any good project, putting together the right design team produces the best results. "The best sign that we're making the right products is that we are prospering in the worst recession to hit this industry since it began," says Mees.



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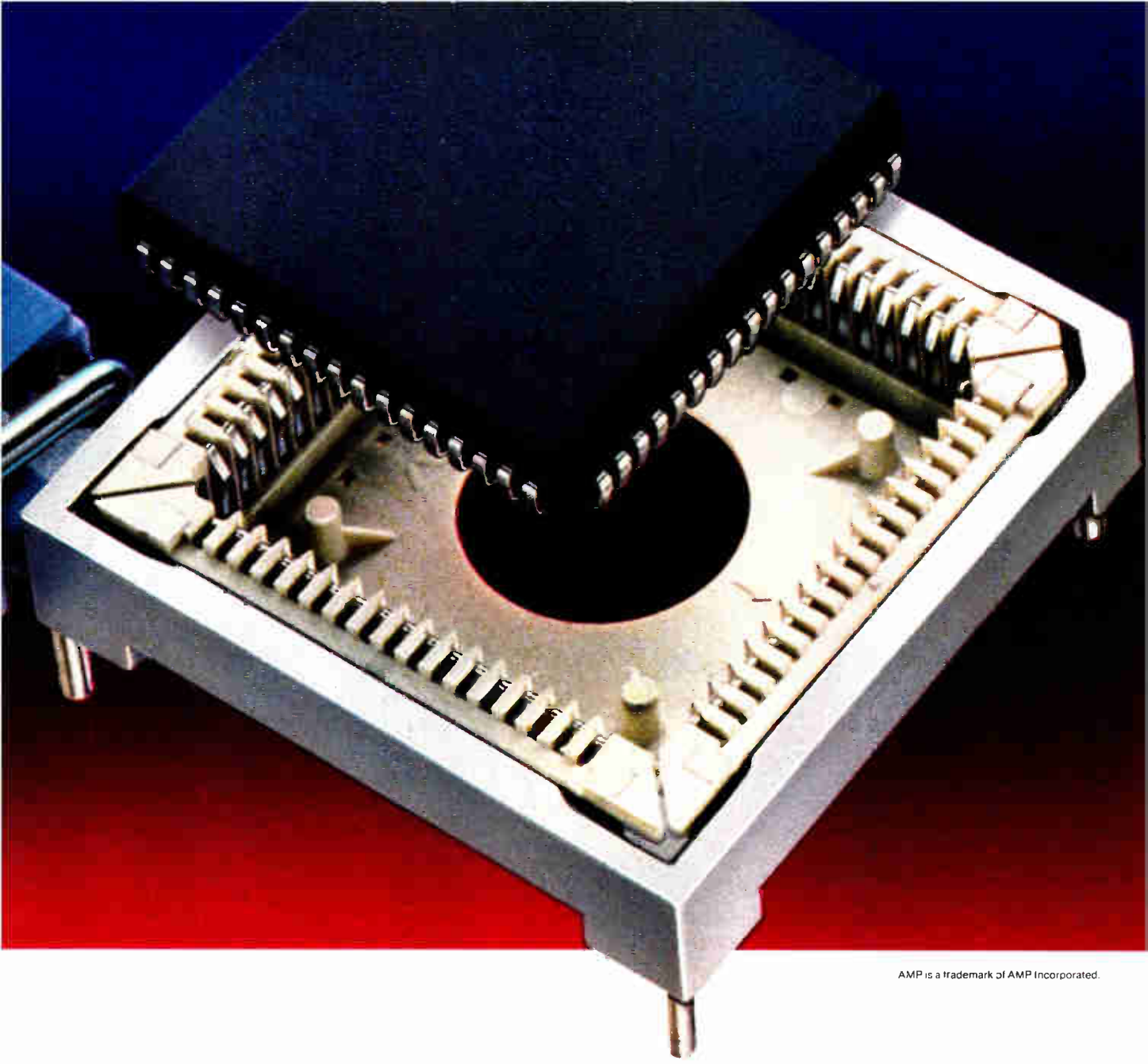

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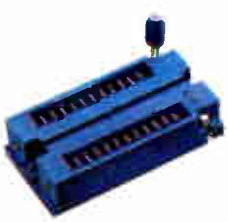
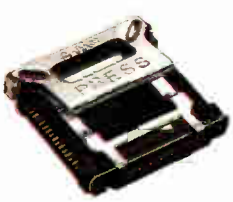


Press-to-release hinged cover on low height burn-in socket eliminates tools, eliminates loose parts. Low profile gets more on the board.



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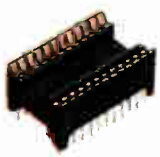

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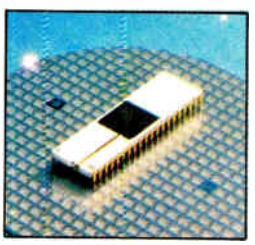

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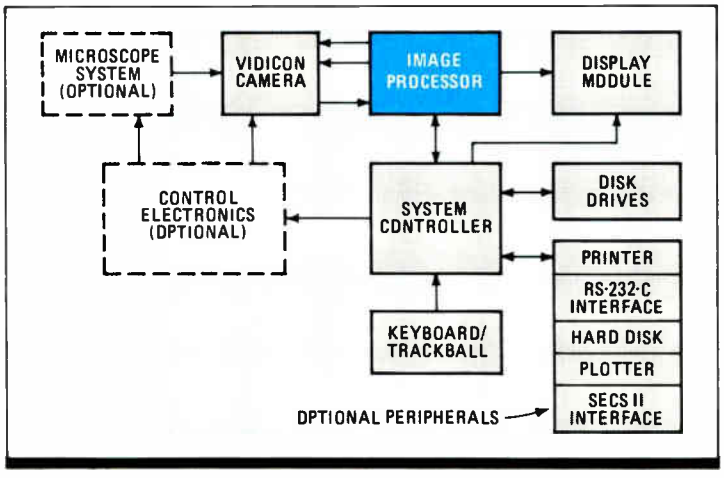
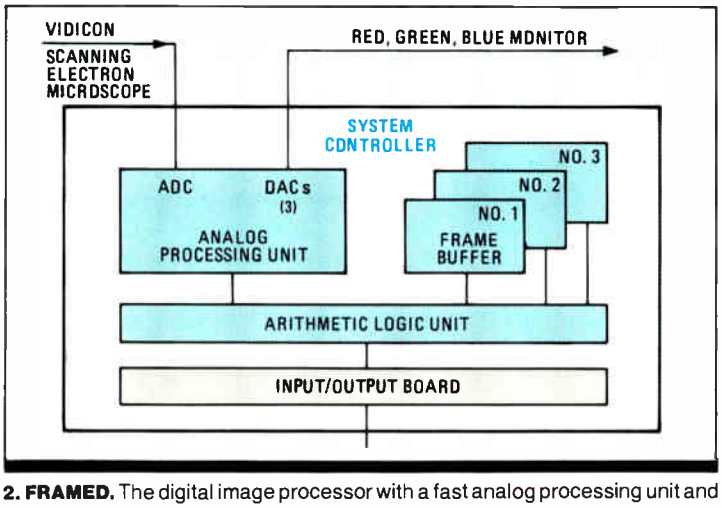
A NEW WAY TO PROBE SUBMICRON DETAILS

Adding image processing overcomes the limitations of optical microscopes in measuring and inspecting wafers with feature sizes under 1 micron



1. DIGITAL MICROSCOPY. Digital signal processing and software let an Accuvision system make submicron measurements with an optical microscope.



2. FRAMED. The digital image processor with a fast analog processing unit and up to three frame buffers digitizes, stores, and averages object images.

As circuit features drop to 1.5 μm and below, the demands of wafer processing are fast outstripping the capabilities of scanning-electron and high-power optical microscopes. Now IVS Inc., a Concord, Mass., maker of video-processing equipment, has added image processing to an optical-scope system, making it accurate enough to measure and inspect semiconductors with features under 1 μm.

The Accuvision system incorporates digital image processing and proprietary application software for repeatable line-width measurements and rapid image enhancement. Users can measure and inspect on the same system, so there's no need to handle the wafers more than once.

Today wafer processing depends on critical-dimension measurement and detection and timely analysis of both random and repetitive defects. When design rules call for 2- to 4-μm features, scanning-electron and optical microscopes suffice. But chip makers are making a transition to 1.5-μm features and will soon attack 1-μm features—too fine for these microscopes.

The optical microscope's limitations stem from the wavelength of visible light. Its resolution and clarity begin to deteriorate at 1.5 μm and are extremely poor in the 0.3-μm range. The scanning-electron microscope can reach the 1-μm range, but has clarity and resolution problems similar to those of the unaided optical microscope when examining lines with extremely fine widths. Furthermore, the energy levels of the electron beam make it destructive and slow.

The Accuvision digital microscope, which includes a display module, converts regular optical microscopy to digital microscopy. Various digital enhancement techniques are used to remove the random noise that plagues optics and electronics. They dramatically improve the signal-to-noise ratio, enabling the system to dependably take repeated measurements in the submicron range. Typical repeatability is 0.008 μm on a 0.5-μm line on a wafer. This is accomplished by using digital image enhancement to improve the S/N ratio before the measurement is taken.

Automatic focus is another important Accuvision feature. The small dimensions of today's ICs make it difficult, if not impossible, for human operators to focus a microscope to a consistent level. This is why autofocus hardware and soft-

ware are standard on all but the low-end model—and optional for that one. To determine the point of best focus, the digital image processor calculates the slope of the edge of the light-intensity profile, which will be steepest at that point.

The Accuvision family consists of four models, ranging from the manual ACV through the highly automated ACV3 (Fig. 1). All are built around three basic subsystems, which can be used in a manual or automatic mode. The optical subsystem consists of a high-quality stable microscope and a high-resolution video camera. The system controller serves as the interface between the user and the system. The digital image processor digitizes and stores the signal from the video camera at a rate of 30 frames per second.

The digital image processor (Fig. 2) has four major elements. The analog processing unit (APU) contains a flash analog-to-digital converter and three digital-to-analog converters. Next are the frame buffers: one or two for storing data and one for transferring it. The arithmetic logic unit performs fast processing and transformation of digital data. The input/output board communicates with the system controller.

After the video data is digitized by the APU, it is stored in one of the frame buffers. The buffers have a resolution of 512 by 480 pixels, each 8 bits wide. Each pixel has 256 levels of gray.

With the frame buffers, the ALU can perform mathematical and logic operations on the data. These operations can improve the S/N ratio, make measurements on the digital representation of the subject under test, or enhance the digital representation of the object under test.

IMPROVING THE S/N RATIO

To improve the S/N ratio of the digitized image, Accuvision uses background subtraction, averaging, and summation. Background subtraction accounts for the optical imperfections that dirt, scratched lenses, and nonlinearities of the optics can cause on the microscope and video camera. It eliminates these distortions by acquiring a blank or defocused image containing only the imperfections caused by the optics. This image is stored in a frame buffer and subtracted from the image to be measured. Afterwards, the image to be measured will contain only the information relevant to the object.

Averaging reduces the random noise introduced by such sources as the environment and system electronics. This noise will be part of the digitized image and, because of its random nature, can unpredictably influence the actual measurement of a chip feature.

Accuvision's high-speed digital image processor allows for 30 frames, or images, per second to be acquired, digitized, and averaged—a process in which successive versions of the same digitized image are stored, then added and divided by the number of samples in the ALU. Because the noise is random, averaging eliminates most of it, leaving a nearly perfect stored digital image of the object under test.

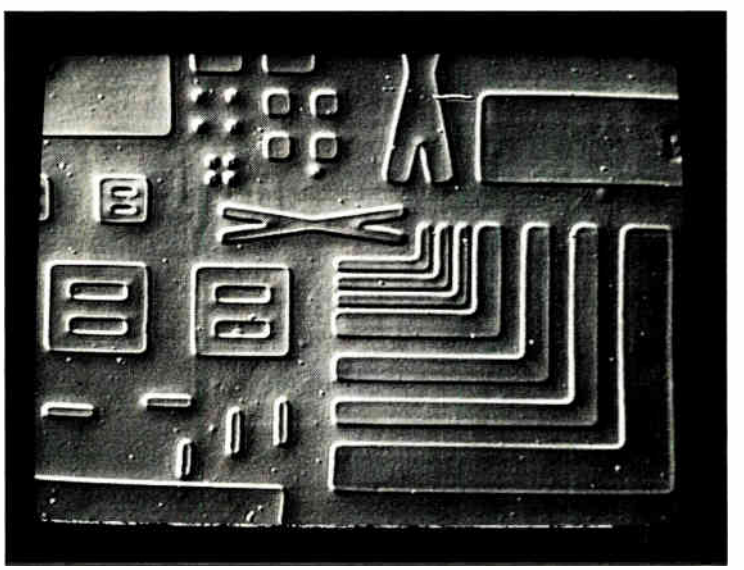
At times, because of the properties of the material or device under inspection, the image's contrast level can be very low, and the usual resolution of 256 gray levels might not be enough to make a meaningful measurement. Then the digital image processor's high speed permits rapid summation of the incoming digitized images. Using two frame buffers gives a range of 16 bits, or about 65,000 levels of gray.

After these procedures, measurement algorithms can be applied. In a measurement, the number of pixels between two selected points on the feature's intensity profile is counted.

FOUR WAYS TO MEASURE

Accuvision allows for selection of four measurement algorithms—dual-threshold, maximum-gradient, and two proprietary IVS algorithms: edge-contrast and autothreshold. The dual-threshold and maximum-gradient algorithms take into account only the information contained in one data point of the image's edge. The edge-contrast and autothreshold algorithms deal with the information contained in the complete edge, so they have many more data points to use in determining the measurement points with the highest degree of repeatability. Edge contrast enables a user to determine a portion of the line edge to be included in the measurement, whereas autothreshold automatically selects the point of the edge of highest repeatability.

The number of pixels to be counted depends on the degree of magnification. When measuring submicron features, it is necessary to get the greatest magnification possible, trading off resolution and contrast. To do this, the user selects the parameters of the rectangular gate—position, width, and height. The digital



3. SHEARED EFFECT. In shearing, two identical images are displaced by several pixels, producing a 3-d-like image.

image processor then interpolates between pixels, resulting in more repeatable measurements. For example, if an optical magnification set for an 8-pixel count represents a 0.5-μm line, then the resolution of each pixel would be 0.0625 μm. Without interpolation, this figure would be the measurement's repeatability and accuracy. Accuvision's interpolation capability raises the repeatability and accuracy.

Even with repeatability between pixel measurements, it is still important to average the measurements for highest repeatability. The rectangular gate, with its variable position and dimensions, plays a role here. Measurements are taken over each video line within the gate and averaged to give the final measurement result for highest repeatability.

The Accuvision system can do more than measure critical dimensions in a single plane: it also can check the alignment between structures located on different layers of a wafer. A standard optical microscope cannot do this adequately in the submicron region: the magnification needed for fine-line measurements reduces the depth of focus, making it impossible to get both layers in the field of view.

Multiple frame buffers and Accufocus hardware and software make it possible to store images located in two focal planes. These images, both perfectly in focus, can be superimposed to form one perfectly focused image, and the alignment of structures in different layers can be measured.

Many of the image-enhancement techniques used to improve measurement in the Accuvision also play a role in the inspection of semiconductor wafers and masks. The digital image processor plays a major role in wafer and mask inspection by implementing such features as shearing and digital comparison.

In shearing, an image of the object to be inspected is averaged, digitized, and sent into two frame buffers. The inspection program then calls for one stored image to be shifted with respect to the other in X, Y, or both directions. The degree of shift is specified in number of pixels. The algorithm automatically subtracts one image from the other, eliminating everything that is equal but highlighting the differences and the edges in a three-dimensional fashion (Fig. 3).

An operater viewing a sheared image can detect common failures such as protrusions and spots. He can also inspect edge roughness, which is extremely difficult to examine on a wafer that has submicron features.

Another important feature of the Accuvision system is digital comparison. Here, a digitized image known to be good is stored in a buffer and compared on screen with the digitized image of the object under test, which is stored in a second buffer. This feature allows detection of process variations and defects. Differences can be highlighted in color. Other measurement features—such as summation, dual-level imaging, contrast enhancement, and zoom—also can be applied to the inspection operation.

IVS is currently engaged in hardware and development work to automate Accuvision completely and to integrate advanced signal-processing capabilities into the instrument to further enhance its inspection capabilities. □

IT ALL BEGAN WITH DIGITIZING IR IMAGES

IVS Inc. was founded in 1980 by Don Yansen and Thorlief Knutrud, graduates of Massachusetts Institute of Technology, and Eutimio Saporetti, a graduate of Rensselaer Polytechnic Institute. Yansen, vice president of manufacturing, specializes in electro-optics; Knutrud, vice president of engineering, specializes in analog-digital design. Saporetti worked on development programs in electro-optics and image analysis for the Mariner Mars Canopus Star Tracker as a systems engineer at Honeywell Inc.

The company's first product was a system that facilitated the conversion of infrared images into digital information, which then could be enhanced and analyzed by computer techniques. In spring 1984, IVS introduced a second line of image-processing equipment that is designed for the study of living cells.

It was about this time that the three founders realized their image-enhancement technology could be applied to the expanding field of wafer and mask inspection, where need was arising for systems that could cope with 1.5-μm features. The result is an optical system that can do critical dimension measurements in the submicron region.

"IVS is now well-positioned in the marketplace and is participating in one of the high-growth segments of the wafer-inspection market," says Rene Verhaegen, the company's director of sales and marketing. Five Accuvision systems have been built: three are in the field at beta sites and two are at IVS. The company expects to sell eight machines in the next two years.

DIGITIZERS. Yansen, Knutrud, and Saporetti added image processing to the microscope.

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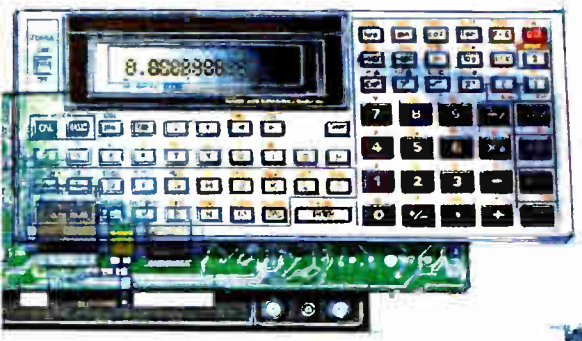

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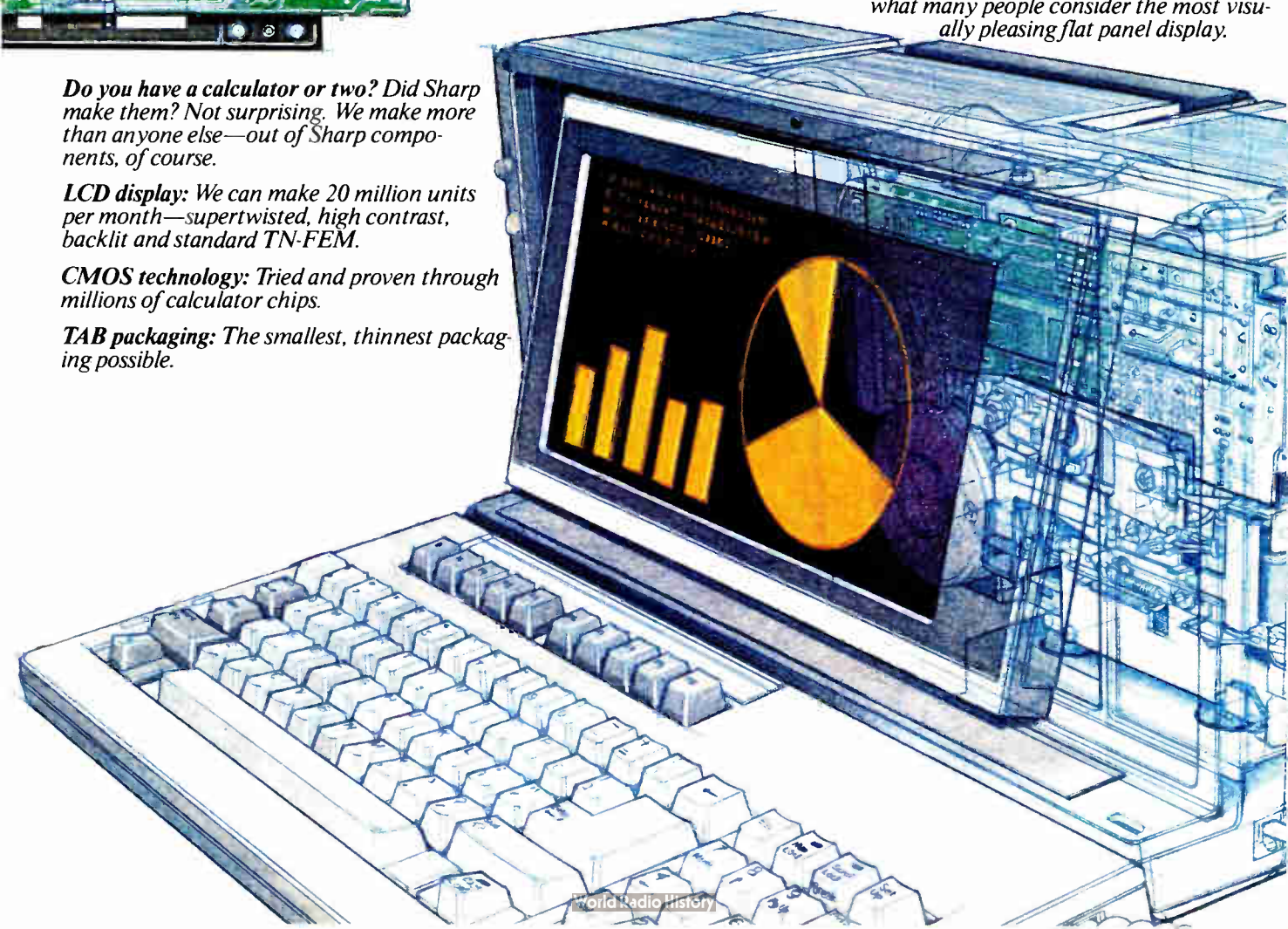

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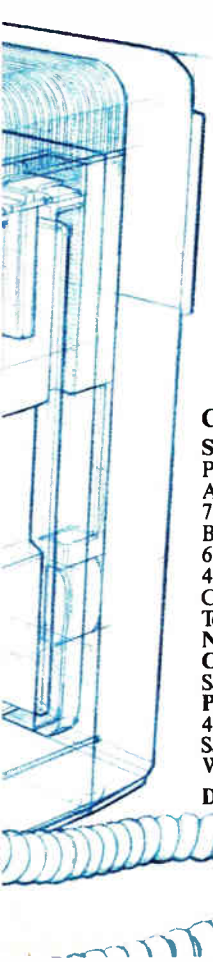

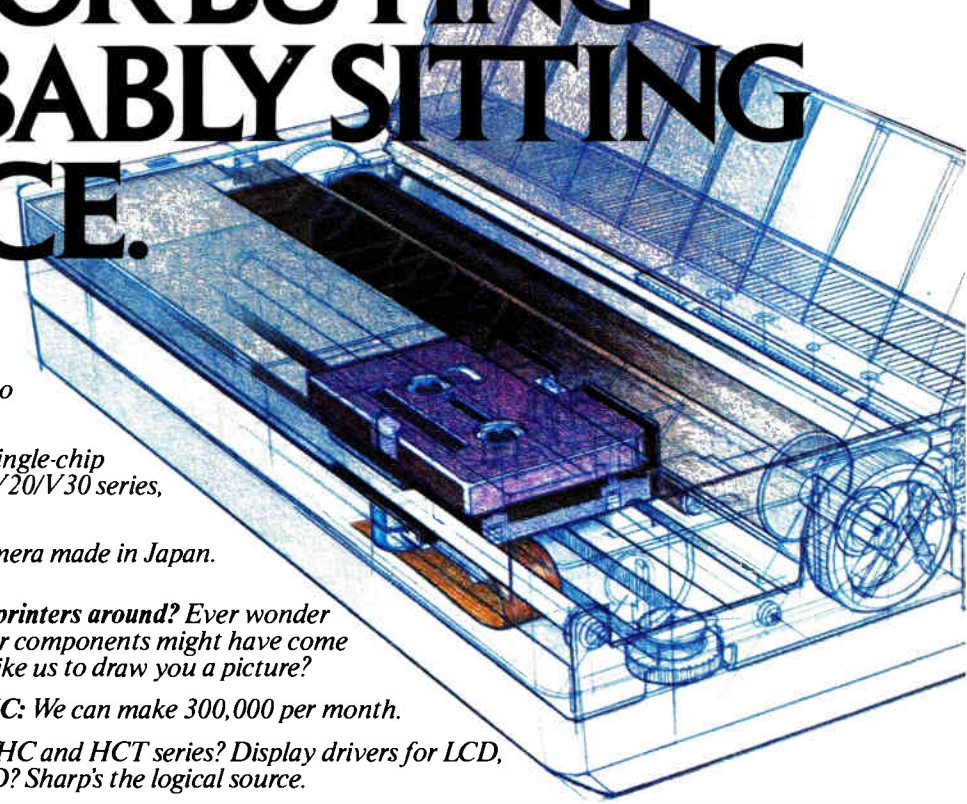

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SOFTWARE IS THE CHALLENGE NOW IN BETTER GRAPHICS

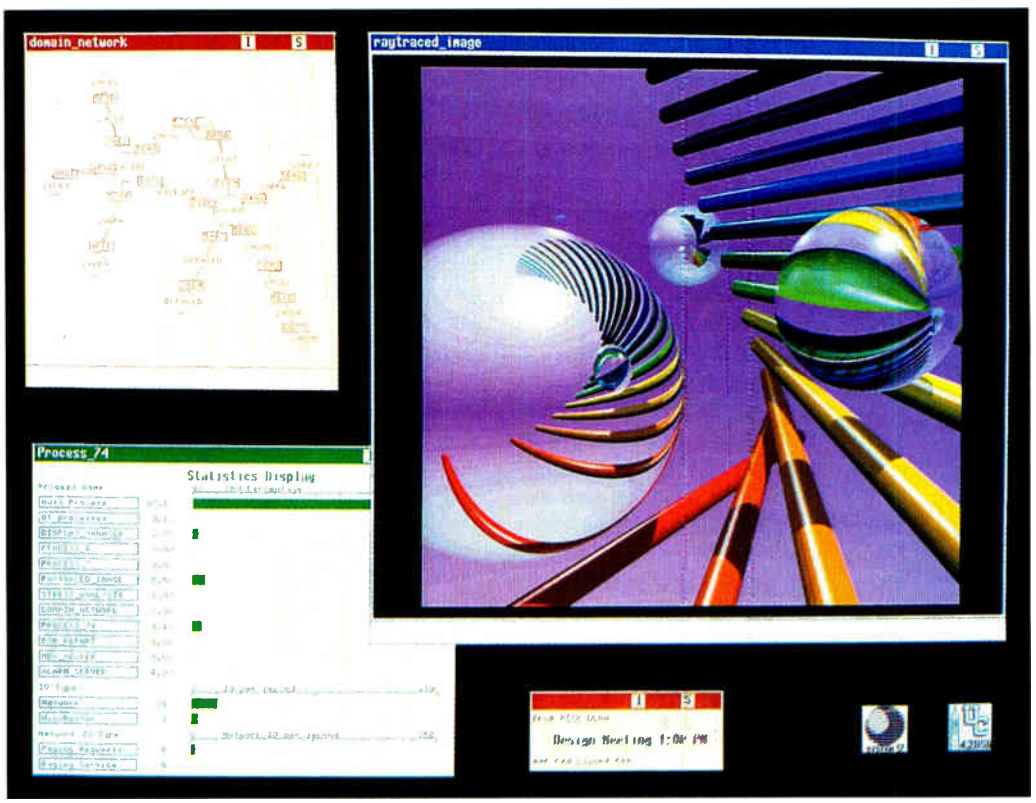
Advances in hardware and firmware are making high-end graphics possible on low-end machines; now all that is needed is the right application software

by Tom Manuel

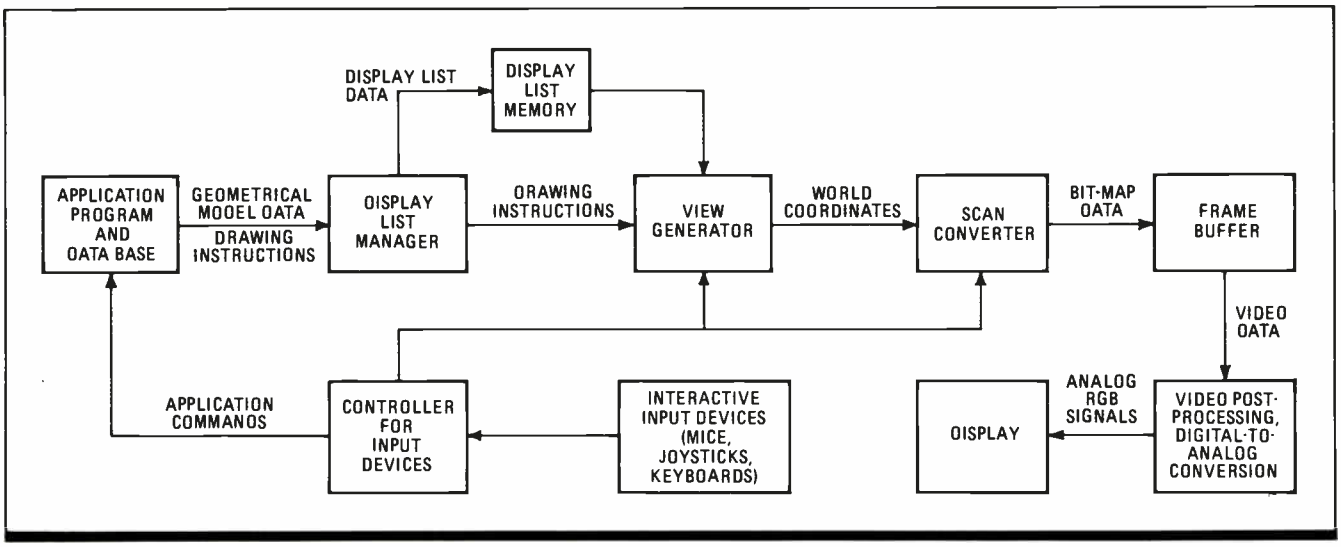
Computer-graphics technology is advancing to the point where even personal computers will soon be producing graphical images with resolution, rendering, and speed that were barely conceivable just five years ago. The hardware is ready, available, and affordable. The firmware and system software for basic graphics operations are pretty much in place. But one thing is still lacking: the body of application software that can use the latest technology effectively.

Developing such applications will be the final, and greatest, challenge for graphics engineers and a new challenge for application programmers. The hardware and firmware for graphics were simple, in one respect: they are quite similar in all computers. But there are many ways to partition the systems—a great variety of architectures—and hence there is a wide variety of choices that a programmer must make in writing application software that uses graphics .

Since graphics require considerable data manipulation and plenty of memory, the technology that has done the most to make them feasible on a wide range of computers is high-performance, general-purpose and special-purpose VLSI processors and fast, very dense memory chips. For example, general-purpose 32-bit microprocessors are commonly available at speeds between 10 and 20 MHz, with a few models in the 20-to-40-MHz range beginning to show up [see story on p. 67]. Now readily available are 256-K DRAMs with access speeds of 150 ns, and 1-Mb chips are beginning to come on stream. Special-purpose ICs useful in graphics systems include several kinds of graphics processors, bit slices, digi-



INTERFACE. Apollo's Domain/Dialogue user-interface management system makes it easy to develop graphics interfaces with a variety of icons, menus, and display windows such as those shown. The graphic at upper right is a ray-trace image.



1. ASSEMBLY LINE. A typical graphics subsystem has several processing steps, beginning at an application program and ending with the display, that act like an assembly line to produce a picture. The user closes the loop between the display and input devices.

tal signal-processing chips, fast static RAMs [*Electronics*, August 7, 1986, p. 121], video RAMS, digital-to-analog converters, new integrations of triple DACs on single chips, and RAMs for video lookup tables on the same chips with DACs.

A simplified model of the graphics assembly line in a raster graphics system shows a series of steps (Fig. 1). Building a display list and converting it into a bit map, which is stored in a frame buffer, leads to postprocessing of the data into video information. At that point, the digital information is converted into analog signals. From there it goes to the final stage, the output device, which usually is a display screen but sometimes a plotter or laser printer.

THE FIRST STEP

The assembly line, however, must begin with an application. Software tools are now being developed that will allow application program developers easy access to graphics technology, enabling them to build enhanced user interfaces and rich graphical output into their programs. Graphics libraries, window managers, and user-interface management systems are about to bring state-of-the-art graphics interfaces to most programs.

Graphics library packages include DI-3000 and GK-2000 from Precision Visuals Inc., Boulder, Colo.; the line of graphics packages from Integrated Software Systems Corp., San Diego; Visual:GKS from Visual Engineering, San Jose, Calif.; and the GSS*CGI (Computer Graphics Interface) Graphics Development Toolkit offered by Graphics Software Systems Inc., Beaverton, Ore. Such packages contain subroutines that applications programs can call to draw common shapes and pieces of pictures, called graphics primitives.

At the other end, the user interface with the computer, software to manage graphical user interfaces is becoming much more common. The earliest such software was often called a window manager; one example is Microsoft Windows, from Microsoft Corp. As user-interface software packages expand in scope, they are increasingly being referred to as user-interface management systems (UIMSs). A typical UIMS is the Apollo Computer Inc. Domain/Dialogue system shown in the opening photograph. The UIMS makes it easier for application software developers to employ in a series of programs the same windows, icons, menus, pop-ups, scroll bars, help facilities, and other such graphical interface features.

The next step in the production of graphics is display list generation. The display list manager, a graphics-utility software package, takes information from an application program or data base and uses it to form a display list: a group of graphics primitives such as vectors, polygons, circles, and text in a number of fonts. The list fits a format designed for rapid drawing and modification of views of a modeled object. Current 32-bit microprocessors and the densest RAMs available are the technologies of choice for the processing power that manages the display list and the memory in which to store it.

The next step in graphics production, view generation, occurs when a particular view of the model or portion of the model is ordered by the application program. The view generator uses drawing instructions from the application program and coordinates for the primitives from the display list to produce the desired view, showing the object from a particular vantage point. It clips that drawing to the volume containing the portion of the model it was drawn from. Then it takes the point in space representing the location of the observer for this particular view and creates the viewplane—a two-dimensional projection of the image as it would appear to the observer. The

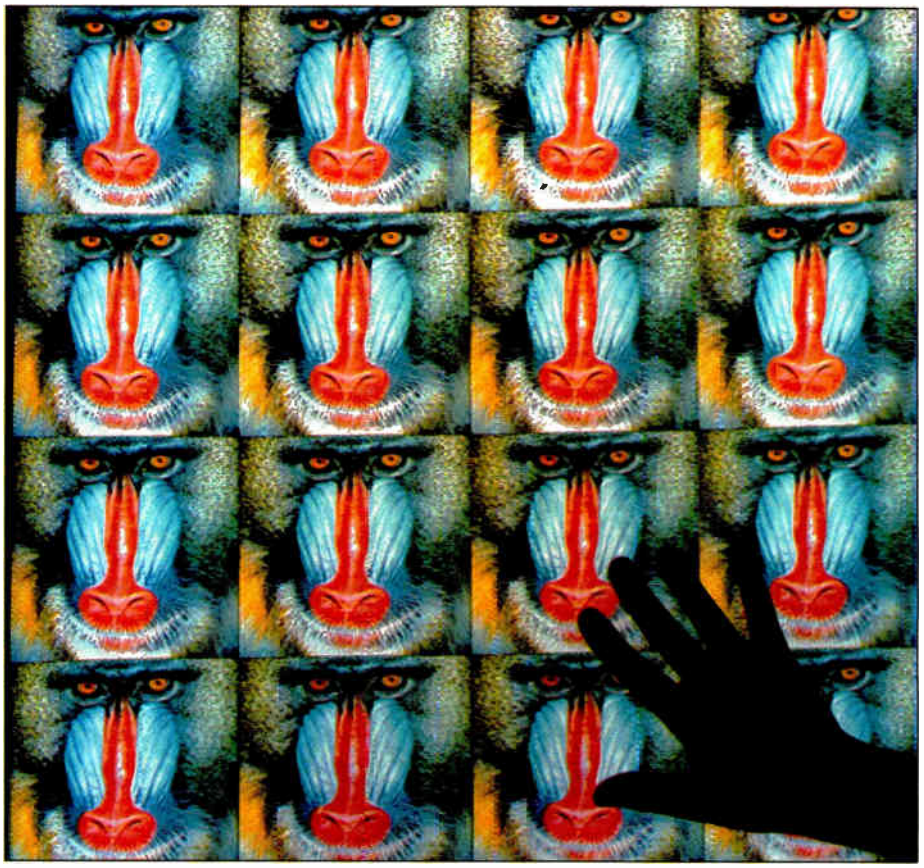
viewplane is cropped and mapped to the part of the screen selected for this picture (the viewport). The object coordinates are converted to device-independent world coordinates, which are passed on to the rasterizer to be turned into a bit map for drawing the view.

In most interactive graphics systems, views change frequently, if not constantly, placing a heavy computational burden on the view generator. Standard microprocessors can handle view generation, but the demands are so heavy that they are confined to the least expensive systems. They do an acceptable job with two-dimensional, 16-bit integer data, when a mathematics coprocessor is also used. For more complex images, special-purpose processors, often implemented with bipolar bit-slice processors, are being used.

Among these processors are the Advanced Micro Devices Am29116, digital signal-processing chips such as the Texas Instruments TMS320 family, Motorola's DSP56000 [*Electronics*, March 10, 1986, p. 30], and the ZR34161 from Zoran Corp. [*Electronics*, July 24, 1986, p. 59]. In the future, floating-point processor chips from vendors such as Weitek may be coupled with the emerging 32-bit families of bit-slice building blocks such as the Am29300 from AMD (see story on p. 64).

However, a few makers of graphics systems prefer to design their own chips and graphics engines. A couple of older examples are Silicon Graphics Inc.'s Geometry Engine and the graphics processors Raster Technologies Inc. and Megatek made for their systems. However, Silicon Graphics has just announced a faster Geometry Engine at 10 MHz, which can manipulate 3-d at 110,000 floating-point coordinates/s. Other new custom processors include the chip set Hewlett-Packard Co. introduced for its HP320SRX work station [*Electronics*, August 7, 1986, p. 97] and a graphics subsystem from General Electric Co., the Graphicon 700. Masscomp Computers Inc. is the first company to offer the Graphicon 700 in a computer system and GE's CAD systems company, Calma, will soon follow suit.

Both the Graphicon and the HP work station bring nearly real-time drawing speed to three-dimensional shaded solid images at the 1,280-by 1,024-pixel resolution level. Metheus Corp., in Hillsboro, Ore., however, is pushing resolution to a new high of 2,048 by 2,048 pixels. Using multiple bit-slice and floating-point processor chips, including some custom gallium arsenide ICs, the Omega 3720 and 3710 are the first commercially available graphics subsystems to generate a full-color 2,048-by-2,048-pixel picture (Fig. 2). Shown for the first time at the Siggraph '86 conference in Dallas the week of August 18, the controllers not only heighten resolution but deliver the graphics at high speed—pixel writing rates range from 6 million to 160 million pixels/s—over 350 MHz.



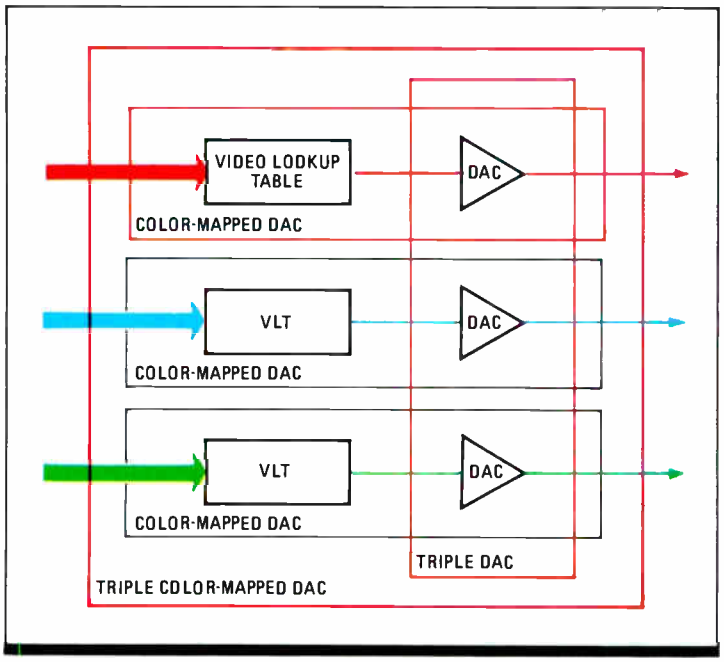
2. PIXELS GALORE. It takes lots of pixels (2,048 by 2,048) to produce 16 images at 512-by-512 resolution each. The Metheus Omega 3720 controller does it.

RASTERIZE IT

Following view generation from a display list, the next step is transforming the graphics primitives into information that describes exactly how every pixel on the display device is to be shown. This step has many names—rasterization, display processing, and scan conversion, among others. The pixel information is stored in a large memory, several planes deep, that is known by several names—the frame buffer, refresh memory, or bit map.

The bit-map and display-processor stages may use some of the same processor chips and memories as the earlier display list and view generation stages, but they also have their own processor and video DRAM chips. Among the first generation of standard large-scale integrated graphics processor chips is the NEC Corp. 7220 GDC.

The second generation of graphics controller



3. CHIP OPTIONS. There are at least three methods for integrating video lookup tables and DACs in the post processing stage of graphics processing.

chips [*Electronics*, May 19, 1986, p. 64] is now coming on stream. They can handle higher-level commands, address multiple color planes, and convert more primitives. Among these second-generation chips are the Hitachi 63484 ARCTC, the Intel 72786 [*Electronics*, May 19, 1986, p. 57], the NCR graphics chip set [*Electronics*, May 19, 1986, p. 61], National Semiconductor's 8500 family, AMD's Am95C60 Quad Pixel Data Manager, and TI's 34010 [*Electronics*, Jan. 27, 1986, p. 15].

Widespread demand for greater graphics capability is pulling the technology at the same time that development of high-performance components is pushing it

To support these new chips with graphics system software, Graphics Software Systems in June introduced new firmware packages for both the TI and Intel chips. The DGIS*34010 and DGIS*82786 ROM kits implement the Direct Graphics Interface Specification. DGIS is an emerging board-level standard that provides a high-level programmer interface for writing graphics-device driver software. The result is high-speed graphics—10 times faster than host-resident software, the company claims.

Many graphics boards or built-in graphics subsystems for personal computers can be implemented using the new graphics controller chips and firmware products. A few graphics board vendors, however, are turning to bit-slice and application-specific ICs to bring high-end workstation graphics to personal computers. Launching this trend are products such as the Pepe board from Vectrix Corp., Greensboro, N. C.; the T4 board from Microfield Graphics Inc., Beaverton, Ore.; and the Clipper graphics subsystem offered by Pixelworks, Hudson, N. H. [*Electronics*, July 24, 1986, p. 38]. All of these offer 1,280-by-1,024-pixel resolution and high line-drawing speeds—from 7.5 million to 20 million pixels/s.

Once a view is generated and rasterized and stored in the frame buffer, it has to be processed and converted for the display device. Video postprocessing is supported by fast ECL RAMs for the video lookup tables (color tables) and digital-to-analog converters. But the trend is toward higher integration. For example, there are several integration paths (Fig. 3): integrating a VLT with a DAC and using three of them, one for each color of the RGB signal; combining three DACs into one IC and using three VLT RAMs; or putting the entire VLT/DAC subsystem on one chip (three VLTs and three DACs). Perhaps the most successful at this is Brooktree Corp., San Diego, with its family of Videodacs, Ramdacs, and graphics support devices. Graphics back-end (postprocessing) products are also available from Analog Devices Inc., Norwood, Mass.; Intech Inc., Santa Clara; and AMD.

Display monitors and plotters are seeing their share of rapid developments. The most recent advances include the Sony DD2800 2,048-by-2,048-pixel color monitor; the 1,600-by-1,280-pixel 19-in. MX-4190 color monitor from Monitronix Corp., Columbus, Ohio; and the 4,096-by-3,278 300-dot/in. 19-in. monochrome CRT just introduced by Megascan Technology Inc., Gibsonia, Pa. And a display the size of a D engineering drawing (22 by 34 in.), the Softplot 2122 "paperless plotter," is offered by Greyhawk Systems Inc., Milpitas, Calif.

Finally, the user-interaction loop is closed with input devices, through which users call for modifications to a picture, request a new picture, or tell a graphical user interface to perform the next task. Input devices range from mice, joysticks, and track balls, to tablets to digitizers. Even the more exotic methods are almost invariably accompanied by a keyboard, though. At some point, the user is going to need it to enter words and numbers.

The transformation of graphics from a highly specialized function into a standard feature is a push-pull phenomenon. The demand for graphics in many more applications pulls the technology; the development of components with continually increasing performance at continually decreasing prices pushes it. At the high end, the transformation is making it possible to manipulate solid, shaded 3-d images in almost real time. At the personal computer level, it soon will bring graphics capability with the resolution, speed, and richness of color that used to be available only at the high end—just yesterday, it seems. □

PROBING THE NEWS

BIPOLAR COMES ALIVE AGAIN AS DEVELOPMENT SPEEDS UP

CIRCUITS AND TECHNOLOGY MEETING RETURNS AFTER 20-YEAR ABSENCE

by Bernard Conrad Cole

MINNEAPOLIS

Bipolar technology is on the move again, advancing rapidly into VLSI now that it has overcome many of the scaling problems that continue to bedevil MOS. One good indicator of the increasing momentum is the number of new processes being moved to production, such as Fairchild Semiconductor Corp.'s contactless Aspect process (see story, p. 55).

Another measure of this resurgence is the resurrection of the Bipolar Circuits and Technology Meeting, a gathering of bipolar technical specialists that had been missing from the calendar since the mid-1960s. Sponsored by the Institute of Electrical and Electronics Engineers, it will be held in Minneapolis next week.

The innovations and solutions that researchers will describe are the new guideposts for the technology, which is increasingly finding its greatest number of applications in the high-density, high-performance end of the market: precision analog and very high-speed digital circuits. And this strength is building even as bipolar's share of the total integrated circuit market diminishes.

According to conference chairman John Shier, device engineering manager at VTC Inc., Bloomington, Minn., "Overall, bipolar is a shrinking fraction of all IC shipments, dropping from 44% of the IC total in 1985 to about 35% in 1990. But viewed by itself, bipolar is an industry with $8.4 billion in revenue and a compound annual growth rate of 12.7%." This growth would be impressive, he says, by almost any standard except that of the MOS market, which is increasing by 22% a year.

Nevertheless, says Shier, in its own segments of the IC spectrum, bipolar will continue to hold its own against MOS technology, which is running into problems as it moves slowly, by tenths of microns, toward submicron geometries. By comparison, he says, bipolar very large-scale integration has overcome many of its scaling problems and, requiring only finer lithography, is moving rapidly from 2 to 1 and even 0.5 μm. "Bipolar devices readily scale to submicron horizontal dimensions," says Shier. "By comparison, MOS devices have to contend with short-channel effects and hot-electron trapping as scaling increases the electric field."

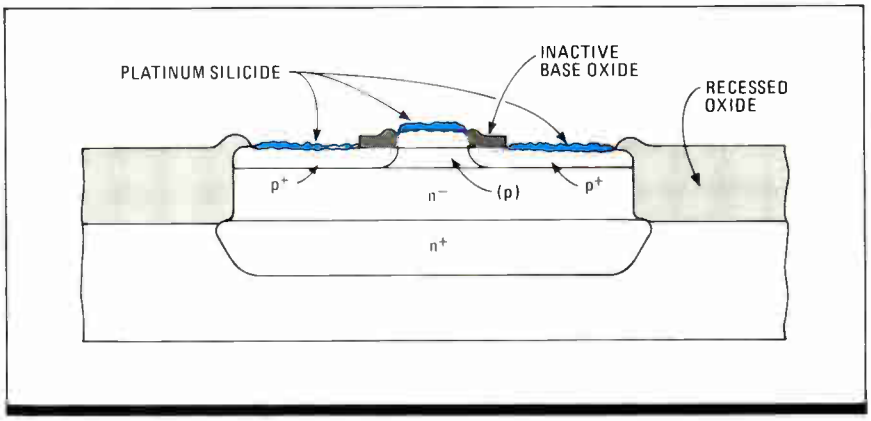
Take, for example, a paper the Honeywell Inc. Solid State Electronics Division in Plymouth, Minn., will present at the conference, describing that company's fourth-generation current-mode-logic process, called ADP-IV (for automatic design process). It can be used for circuits as dense as 100,000 gates, gate speeds of about 500 ps or better, and a power dissipation of only 50 μW per gate. Key to the high density are shorter channel lengths, thinner gate dielectrics, groove isolation, triple implantation, four layers of metalization, and electron-beam lithographic techniques. The advantage, the researchers say, is that the scaled-down bipolar gates maintain their speed at a lower current, allowing more devices to be placed on a die for a given amount of power.

'Bipolar devices readily scale to submicron horizontal dimensions'

Also for use in CML-based circuits is a process that will be described in a paper from TRW Electronic Systems Group in Redondo Beach, Calif. The technology features an oxide-walled self-aligned emitter. In addition to buried layers, recessed oxides, diffused isolation regions, diffused n+ contacts, and platinum silicides for interconnection (see figure, below), it incorporates an emitter-base structure designed to minimize problems with boron channeling that occur in many VLSI designs, both bipolar and MOS.

STRESS BUSTER. Involving the formation of a thin thermal oxide on the arsenic-doped polysilicon, the process prevents unacceptable levels of stress between the silicon nitride and the poly, accommodating the undercut of the polysilicon gate emitter without significantly etching the implanted base region. Used in the fabrication of a simple divide-by-2 prescaler, it can operate at 3.9 GHz with internal logic swings of only 200 mV.

Also being described at the meeting is a complementary bipolar process for high-speed precision analog circuits from Analog Devices Inc. of Wilmington, Mass., used for the fabrication of junction-isolated vertical npn and pnp transistors with toggle frequencies in excess of 0.5 GHz and breakdown voltages above 36 V. Both the npn and pnp

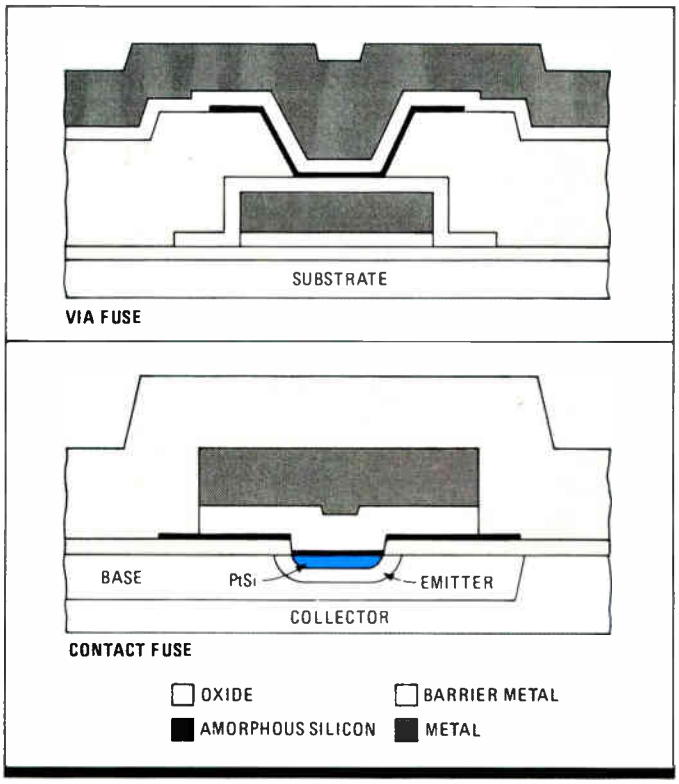


NOT TO WORRY. TRW's process for CML-based circuits has an emitter-base structure that is designed to minimize the boron-channeling problems that occur in both bipolar and MOS VLSI.

transistors use standard double-diffused emitters and base junctions. The pnp has a standard epitaxial buried-collector structure, but requires a p-type epitaxial layer, whereas the npn transistor is a triple-diffused structure with a buried collector isolated by a p well.

Researchers at Tektronix Inc. of Beaverton, Ore., who are trying to design devices that can withstand the 400°C to 500°C anneals necessary in the fabrication of high-performance bipolar circuits, will describe a metalization scheme to replace the palladium-silicide-titanium/tungsten-palladium-gold process.

Circuit yield suffers at high temperatures, the researchers say, because of gold-silicon interdiffusion and penetration of the titanium into the thin oxide around the gate contacts. To prevent this, rhodium is added to the mix and vanadium silicide replaces the palladium silicide, allowing anneals as high as 600°C without degradation.



NO TRENCH. TI turns to scalable antifuse technology using amorphous silicon for high-density bipolar PROMs without trench isolation.

And from Fairchild Semiconductor in Mountain View, Calif., comes a single-polysilicon process optimized for fabrication of circuits requiring both analog and digital functions. With 2-μm design rules, emitter-coupled-logic gate delays of 162 ps have been achieved that dissipate no more than 2.5 mW per gate. With 1-μm design rules, the designers expect to reduce the gate delay to as little as 100 ps. The process has been used for a 900-MHz 8-bit shift register and a video digital-to-analog converter with a conversion rate of 400 MHz.

As for circuit design, several papers describe the use of advanced bipolar techniques for a variety of semicustom circuits. From Texas Instruments Inc. of Dallas, there is a 16-input, 8-output ECL fuse-programmable-array logic device that is made using TI's Impact-X process; it features delays of only 4.5 ns.

Another high-speed FPAL of the same design comes from the company that originated the concept, Monolithic Memories Inc. of Santa Clara, Calif., with a 7.8-ns device fabricated using its new oxide-walled-base bipolar technology. Engineers from Signetics Corp., in Sunnyvale, Calif., who are aiming at more complex programmable logic devices will describe the application of the company's vertical fuse technology to a 20-input, 24-output field-programmable logic array that can operate at 14 ns.

In gate arrays, engineers from Motorola Inc.'s Government Electronics Group in Scottsdale, Ariz., have developed a radiation-hardened 2,500-gate macrocell-based device that can be fabricated with either of two bipolar technologies: Motorola's 6-GHz polyimide-isolated Mosaic II for ground applications or its 4-GHz Mosaic I, using silicon-dioxide isolation between metal layers. Not to be outdone, Honeywell Inc.'s Solid State Electronics Division will describe a 1.6-GHz bipolar array that combines nine tiles containing a variety of analog structures with a 96-gate integrated Schottky logic array. Another analog/digital offering comes from VTC: a bipolar standard-cell library that includes 40 fully characterized analog and 101 digital functions.

Innovations abound in semicustom, gate arrays, and memory

In memory, Bipolar Integrated Technology Inc. of Beaverton, Ore., will describe a 6-ns, five-port, 1-K register file that it has fabricated with its 2-μm BIT1 process, which offers high performance and high density [*Electronics*, April 7, 1986, p. 24]. Including one read/write, two read-only, and two write-only ports—all of which may be used on the same 6-ns cycle—the random-access memory contains 43,000 active devices on a 290-mil² die and dissipates 6 W, including the 54 ECL output drivers.

Resulting from a collaboration between Honeywell and Sperry Corp.'s Minneapolis operation is a 64-by-12-bit ECL dual-port RAM with 2.1-ns read-access and 1.75-ns write times. The memory is fabricated with a self-aligned bipolar process that has a 2-μm single-polysilicon layer.

And researchers from TI's process-development facility in Houston will describe what they did when they were looking for a way to achieve high-density 64-K to 256-K bipolar programmable read-only memories without using trench isolation. Their solution was a scalable antifuse technology (see figure, left) using undoped amorphous silicon, which requires a significantly reduced programming current when compared to conventional fuse-blowing technology.

A variety of standard and full-custom circuits made with analog and digital bipolar processes will also be described, including a programmable correlator with redundancy from the Institute for Theoretical Electronics in Aachen, West Germany, which can do 656 million operations/s; a 150-MHz video DAC with six-color palette from Motorola's Tempe, Ariz., operation that dissipates only 750 mW; a 175-MHz video-display driver featuring 2-ns rise times, from Tektronix; a 10-GHz, 17-dB microwave self-oscillating mixer functioning as a frequency converter from Avantek Inc., of Santa Clara, Calif.; and a precision high-speed sample-and-hold amplifier from Harris Semiconductor Corp. of Melbourne, Fla., with a slew rate of 100 V/μs, an open-loop gain greater than 140 dB, a droop rate of 10 V/μs, and an acquisition time of 500 ns per 10-V step.

Considerable attention will also be focused on the device modeling, simulation, and design tools that will be key to bipolar's move into the VLSI level. Included will be a number of new Spice models from companies such as Tektronix Inc.'s Integrated Circuits Operation; TI's Semiconductor Process and Design Center; and the University of Florida Department of Electrical Engineering; as well as a three-dimensional model for bipolar transistor simulation from the Department of Electrical and Computer Engineering at Arizona State University. And from Carnegie-Mellon University's Department of Electrical and Computer Engineering comes Fabrics II, a CAD bipolar layout tool. □

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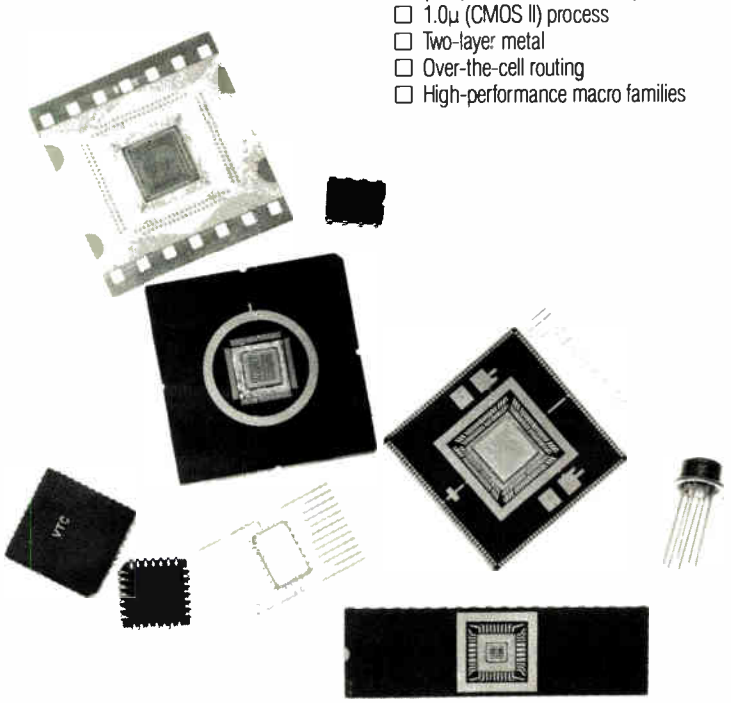

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THE ATE-AI PARTNERSHIP IS HITTING ITS STRIDE

PRACTICAL SYSTEMS ARE STARTING TO APPEAR ALREADY

by Jonah McLeod

WASHINGTON, D. C.

Artificial intelligence is widening its role in the world of testing. Manufacturers of automatic test equipment are moving beyond such first steps as as the establishment of knowledge bases, and they're now fashioning practical ATE expert systems.

AI functions such as designing and building testability into very large-scale integrated circuits, establishing expert systems and using them to pinpoint faults, and creating diagnostic routines to sniff out failures in test equipment are being expanded and refined far beyond their first incarnations in testing equipment [*Electronics*, Nov. 25, 1985, p. 56]. New applications, among them automatically configuring test systems to perform specific tasks, are being developed. And some of the new approaches are getting set to move out of the lab and into the marketplace.

At the International Test Conference in Washington next week, two sessions on AI in testing will outline developments that hold great promise not only for those who build and use test systems but also for those who design the circuits to be tested. Some of the systems automatically incorporate the trial-and-error knowledge fed them by test engineers, continually upgrading themselves in a partnership with their users.

Among the more elusive aims is built-in testability. Most VLSI designers don't have the knowledge of sophisticated design methodologies needed to build self-testing into their chips. This blind spot is felt quite sharply right now in application-specific ICs, so GEC Research Ltd. will describe a knowledge-based setup that it says provides the ASIC designer with built-in self-test expertise as part of the VLSI design system.

Based at GEC's Hirst Research Centre in Wembley, England, the researchers call their tool Loops, for Lisp object-oriented programming system. In examining a circuit design, the tool proposes individual test circuits that can be built into the IC (see figure, right). Once the user has entered the circuit design, Loops generates individual test circuits a user can incorporate into the ASIC design. The user then enters time and area constraints, enabling Loops to further refine the test circuits it has added to the ASIC.

Some 4,000 miles from Wembley, at Purdue University's School of Electrical Engineering in West Lafayette, Ind., a similar knowledge-based design has been built into an expert system. Called DEFT, for design for testability, it works in conjunction with a design-automation system from IBM Corp. called MVISA (Manassas VLSI interactive system for automation) and uses IBM's Basic Design Language for Structure to describe the circuit being designed.

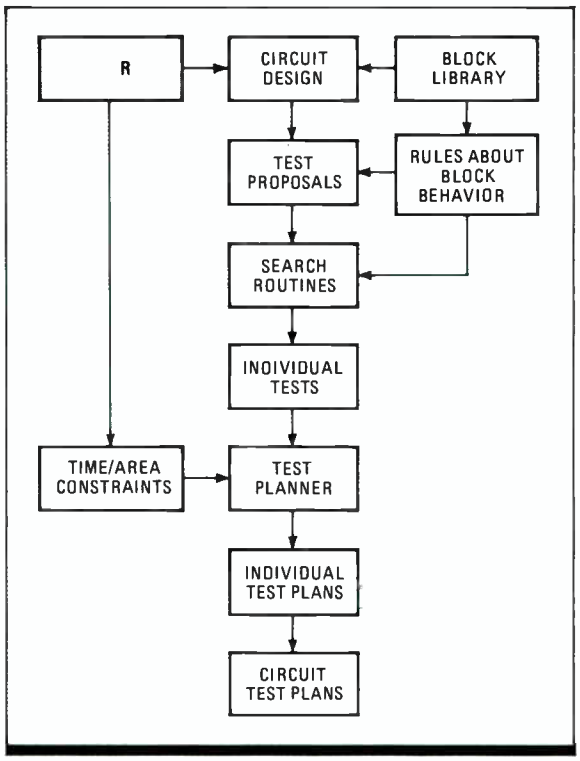
But DEFT, which is a research tool, modifies the description of the circuit to improve testability. It adds criteria such as fault coverage and hardware overhead to determine an optimum design that takes testability into account. After determining what modifications to make, DEFT then feeds back a new description to MVISA. In this way, design for testability is built in without much intervention from the designer.

The goal of yet another new system is to offload the drudgery—as well as to improve efficiency—in the process of finding faults in circuits during manufacture or during repair in the field. Westinghouse Electric Corp.'s Integrated Logistics Support Division in Hunt Valley, Md., draws on the trial-and-error knowledge of test engineers and a detailed knowledge of basic electronics to find circuit faults in a device under test.

TWO DATA BASES. Called In-House Use and Knowledge-Based Diagnostic System, it contains two data bases (see top figure, p. 105). The design data base houses a description of the schematic and behavior of the circuit, and is used by the system's causal reasoning inference engine to justify symptoms and identify faulty components. The rule data base contains information acquired or predicted about the relationships among test stimuli, symptoms, and faults.

That information comes from both the causal reasoning inference engine and the experience and analysis of test engineers. The rule-based inference engine uses the rule data base to help the test engineer isolate a fault in the unit under test. During the course of the debugging process, the system learns from the test engineer and stores the knowledge in the rule data base. Westinghouse says the system is now in development and it hopes to demonstrate it by the end of the year.

Teradyne Inc. of Boston will describe a similar AI system, one that aids in diagnosing analog component failures on a board under test in an in-circuit tester. In-circuit testers isolate each component on a printed-circuit board, classifying analog components such as resistors and transistors and testing their operating characteristics. The system operator then deciphers failure indications to find out



BRITISH BUNDLE. From England's GEC Research, Loops suggests circuits to be built in to provide self-test.

why a component failed the test and how to correct the problem.

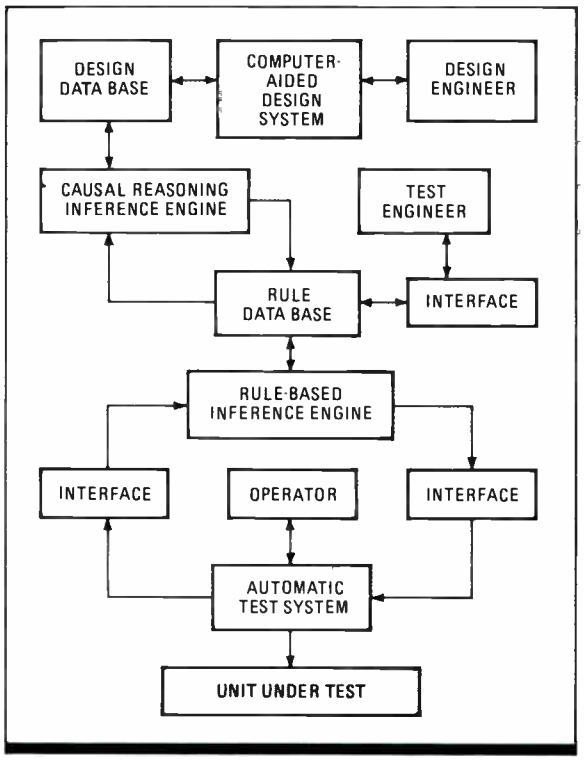
The system, called In-Circuit Diagnostics, is part of the software for the L-200 VLSI board testers and has three parts: a knowledge base developed during test generation that contains information about the board under test and every component on it; a failed-test analyzer; and a diagnostic inference engine. The engine uses data about each component in the knowledge base along with rules for analog circuits to determine why a component failed. Teradyne says its product could reduce the need for defect analysis in the manufacturing rework process, and that the failure data can also be used to help test-management systems provide manufacturing-quality feedback via defect reports

SMART SYSTEM. Sentry/Schlumberger in San Jose, Calif., takes the notion of improving manufacturing process management with AI to perhaps its ultimate conclusion. Its AI system is marketed under the name Smart, for semiconductor manufacturing analysis and reduction tools. The new version of a factory-automation system called Test Area Manager, Smart contains knowledge provided by semiconductor manufacture and test engineers, including facts and relationships of device physics, product definitions, fabrication properties, and test definitions.

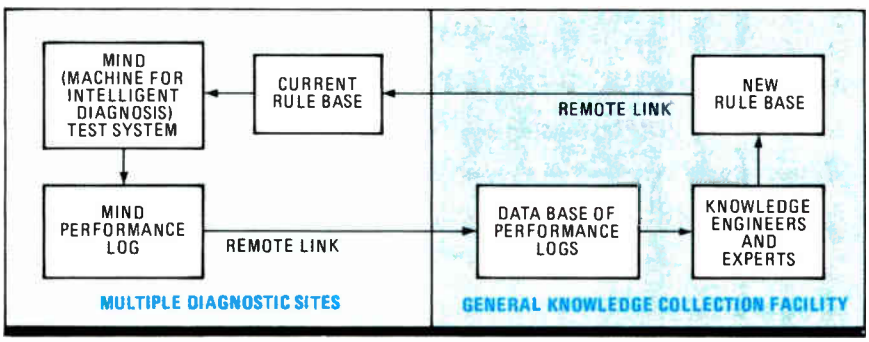
Smart is part of Sentry's factory-automation system, which controls and defines the semiconductor manufacturing process. It contains an AI system called PIES (parametric interpretation expert system) that diagnoses process failures by analyzing parametric test data measured in semiconductor fabrication lines. In turn, Smart uses the diagnosis in conjunction with other information in its knowledge base to suggest an action or change in the manufacturing process to correct a problem. The problems and solutions thus encountered are then added to the knowledge base.

An improved version of a system that finds and repairs failures in test systems themselves will be described in two papers from Teradyne's Woodland Hills, Calif., facility. The system, called MIND (machine for intelligent diagnosis), reduces by half the mean time it takes to repair a complex VLSI test system. MIND, which will be an integral part of the J937 memory-tester system software, is built into a work station from Sun Microsystems Inc. and is connected by communications lines to Teradyne VLSI test systems in the field. The company says the system provides a 2:1 improvement over a human doing the repair alone.

The system combines algorithmic fault analysis—following an error condition back to its source by tracing the logic—with knowledge acquired from experienced field-service technicians who have figured out when to swap a particular board that's probably causing an error. A program called Check, housed in each field test system, interacts with MIND to carry out the system fault isolation.



TWO BASES. Westinghouse system contains two data bases, one for design, the other for faults.



KNOWLEDGE COLLECTOR. Teradyne's central facility collects data from all its MIND VLSI test systems in the field. The information then is used to update the field installations.

CENTRAL BRAIN. In addition, Teradyne has set up a central knowledge-collection facility that gathers data from field sites, each of which has its own MIND system. Each system in the field contains a performance log that is periodically sent to a data base of performance logs at Teradyne (see figure at bottom). By analyzing the data from these sites, the company can update MIND rule bases in the field to reflect new information. This trial-and-error technique duplicates human experience.

What MIND does for fault isolation, a product called Arnold does for automatically configuring a test system to work on a VLSI component. Developed by Tektronix Inc., Beaverton, Ore., Arnold does not generate test vectors but rather uses test vectors and parametric data entered by the test engineer.

Arnold knows the hardware of the tester and the best way to test VLSI components. The test engineer defines the pinout of the chip in a knowledge base of parts being tested; Arnold does the rest. The system knows which elements of the parametric measurement unit to connect to which pins, and it knows how long to wait for relay switches to settle before starting a test. In effect, Arnold carries out all the connections and tester configurations that previously the test engineer had to do himself.

Besides the papers that will deal with specific aspects of applying AI to automatic test, the conference will hear a trio of papers exploring some general solutions to the problem of test generation. One, from AT&T Bell Laboratories in Murray Hill, N.J., describes the application to test generation of a mathematical technique called the Interactive Theorem Prover, developed by the Argonne National Laboratories. Briefly, the technique develops the intermediate steps needed to arrive at some mathematical conclusion—for example, the Boolean expression at the output of a logical circuit.

Also from AT&T, in this case the Engineering Research Center in Princeton, N.J., is a paper detailing a test-generation algorithm that creates a test vector to detect the greatest number of possible faults, as opposed to one that finds a single fault. The technique affords tests that are 50% more compact than those arrived at with conventional test-generation algorithms. □

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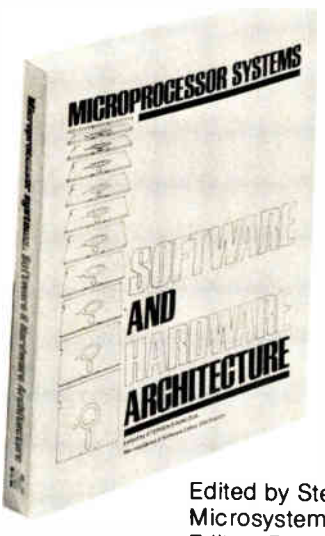

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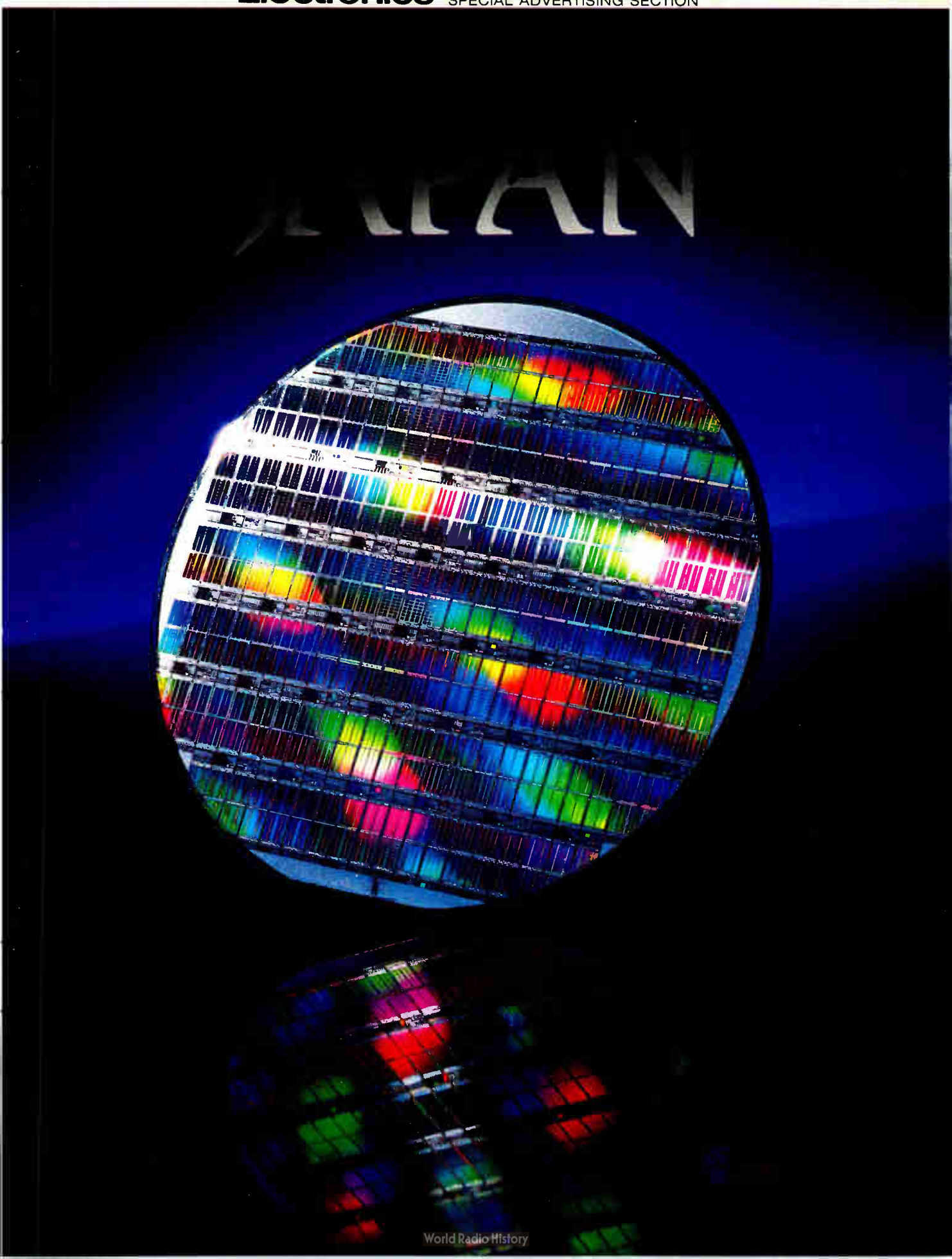

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JAPAN

SPECIAL ADVERTISING SECTION

Japanese electronics industry rises to meet ever-changing conditions

The Land of the Rising Sun has always been the shining star in the world of electronics. Energy shortages, market saturation, and a tougher competitive climate caused by the soaring value of the yen are challenging the Japanese mettle. In telecommunications, the liberalization of Japan's laws are creating new market opportunities for a number of companies. Personal-computer network services, for example, are thriving; one such service already has more than 16,000 subscribers, a considerably longer list than the national service has lined up.

Both worldwide and domestic conditions have made virtually all Japanese companies loook into automating their factories. The two oil crises have had an especially strong effect on the industrial economy, given that the island nation that has always been short of energy resources.

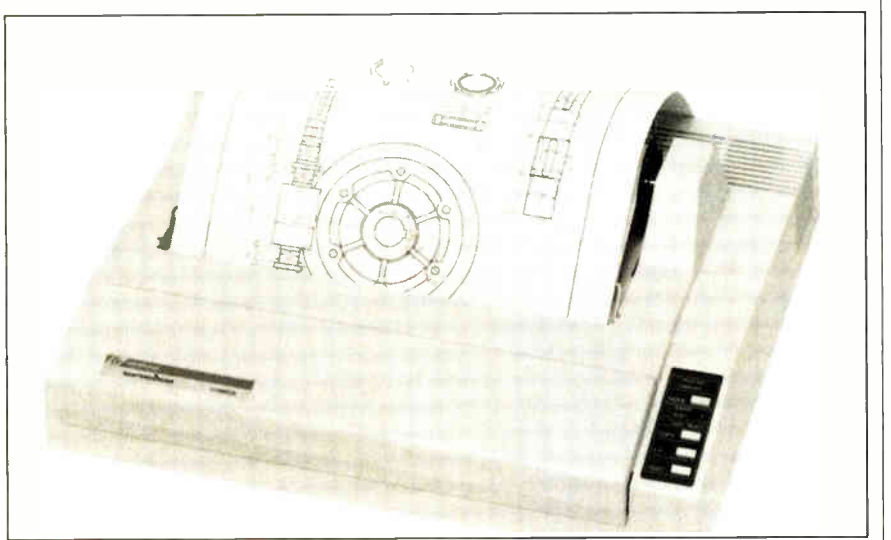
The great effort put out in developing fifth-generation computers has also spawned a boom in artificial intelligence. One area that is showing great promise for AI applications is in data-base computers.

In semiconductors, last year brought a double dose of bad medicine. Not only did the market contract but the rising value of the yen eroded prices overseas. This hurt industry in particular because Japan exports 37% of its production. In the components arena, companies are finding new markets in hybrid-ICs and flat-panel display makers.

This year's report was written by the industry analysts at the Nomura Research Institute in Kamakura. Shigeaki Kaneyori spearheaded the project and wrote the Telecommunications section. The Factory Automation section was prepared by Kensuke Shima, the Memory Card chapter by Shinji Yamane, and the Artificial Intelligence section was written by Ken Miura. Shin Kusunoki, Junichi Inoue, and Masakazu Kimura wrote the Magnetic Media, Semiconductor, and Components sections, respectively.

TABLE OF CONTENTS

Cover photo: Semiconductor wafer compliments of Toshiba Corp.



Graphtec's MS8603 Rastercorder thermal plotter prints with a resolution of 8 dots/mm.

2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.

TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} – 0.5V min.	V_{DD} – 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

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TELECOMMUNICATIONS

Liberalized telecom laws create opportunities for savvy companies

The liberalization of Japan's telecommunications regulations in 1985 has opened new opportunities in both information communications and voice communications for savvy and energetic companies.

In the area of information communications, vendors of both terrestrial and satellite communications services have begun domestic service in competition with Nippon Telegraph & Telephone. The number of companies registered as value-added-network service vendors now totals almost 300. International communications services are also expected to have new entries to compete with Kokusai Kenshin Denwa Co., Japan's international communication carrier.

Compared with the vitality of information-communication services, such newer services as videotex and community access television, at first targeted mainly at consumers, have been dragging. Now the personal computer network service could be set to give them a push.

Personal computer network services have emerged as grass-roots information-communication services—an alternative to Captain, the national videotex service, which has been received poorly despite the vigorous promotional efforts since its start in November 1984.

Captain has 16,000 terminals installed, of which less than 1,000 are in homes. In contrast, the total number of subscribers to ASCII's ASCII Net, the largest personal computer network service in Japan, exceeded 10,000 subscribers within a year after its start in May 1985. The number of subscribers to ASCII Net currently stands at 16,000.

Computer networks

Other vendors include NTT PC Communications (a joint venture of NTT and Logic Systems International), Japan Air Line, NEC, Nikkei, and Nippon Telenet (which is supported by Matsushita). Moreover, almost 100 private bulletin-board services are available.

U. S.-based personal computer network services such as Compuserve, the Source, and Dow Jones News Service have also captured about 500 to 1,000 subscribers, who get access to the U. S. services through KDD's international public packet-switching network, Venus-P. Compuserve is

Focus on Toshiba Corp.

Kinichi Kadono, senior managing director

In the fiscal year ended March 31, 1986, Toshiba Corp. registered net sales of $18.7 billion, of which 31% was generated outside Japan, and net income of $330.2 million. Its business encompasses four main segments: industrial electronics and electronic components; consumer products; heavy electrical apparatus; and materials and machinery. It also produces such parts as color picture tubes, pc boards, and charge-coupled devices.

Toshiba is a major supplier of MOS memory devices, MOS logic ICs, bipolar ICs, and discrete devices. As Japan's third-largest manufacturer of semiconductors, it is positioning itself for growth in electronics, office networking, and telecommunications through alliances with major U. S. and European companies. For example, Toshiba is teaming up with LSI Logic Corp. to jointly develop high-performance gate arrays.

Although its semiconductor business fell 17% from the 1985 fiscal year, the company is not cutting back R&D. It already has developed a prototype 4-Mb DRAM.

To meet increasing customer demand for applications-specific ICs, Toshiba is constructing an Electronic Engineering Center in Kawasaki. Already the company operates design centers for large-scale integration in Japan, the U. S., and Europe—all linked to host computers through satellites.

scheduled to be on Fenics, Fujitsu's VAN service.

Joint system

Also planned is Famicon Net, which is designed to capitalize on the more than 7.5 million Nintendo Family Computers that have been sold. And NTT and Japan Radio Co. intend to build a joint network system for personal communications using satellite communications—19.2-kb/s lines over CS-2B communications satellites and ground stations, digital termination equipment, and satellite data multiplexers.

As personal computer communications becomes a hot topic, deregulation has made a variety of acoustic couplers, telephones with built-in modems, and separate modems available at a very attractive price. Communication speed is shifting from 300 to 1,200 b/s, and will reach 2,400 and 4,800 b/s. The Ministry of Post and Telecommunications has already standardized a 4,800-b/s protocol for personal computers.

Changes in CATV are coming as well, which will open its use in business for video teleconferencing as well as link it with information-processing systems. A major innovation will be program distribution of satellite-communication carriers such as Japan Communications Satellite and Space Communications. CATV services in Tokyo, Yokohama, Kawasaki, Nagoya, and Sapporo are scheduled for 1988.

Telecommunication equipment also is linked increasingly with information-processing systems. And one of the vital telecom-equipment businesses is digital private branch exchanges. The market for digital PBXs in Japan grew from 38 billion yen in 1984 to 45 billion yen in 1985, according to the Nomura Research Institute.

In Japan, various traditional communications regulations has kept the market for digital PBXs on hold. Fujitsu, Hitachi, NEC, and Oki, the market's front-runners, initially focused on U. S. markets.

The next stage, following central processing and distributed processing, is integrated processing. And at its heart lies the digital PBX. Also of importance are local-area networks and micro-to-mainframe links.

The final stage of system integration will be the multimedia integration; early multimedia setups have been developed as intracompany versions of the integrated services digital network. Among these are Fujitsu's Corporate Information Network System and NEC's Vision for large corporations. The components of multimedia networks include multiplexers, leased lines, public networks, LANs, digital PBXs, and terminals for facsimile, telephone, image-data communication, traditional data-communication gear, and mobile phones.

Still to come

Nevertheless, it will be a number of years before full-scale multimedia integration prevails among large companies. First the price of leased lines will have to decrease, which should happen as competition builds among class-one carriers, those communication service vendors that possess communication facilities. The next step is the integrated digitalization of public-network subscriber lines during the 1990s. Among small and midsized companies, however, only tenants of smart buildings with shared services will find setups of this scope economical.

FACTORY AUTOMATION

Global and domestic forces encourage companies to automate

Efforts to improve Japanese production systems have been in response to a host of global and domestic changes, the major ones being the two oil crises, advances in microelectronics technology, and the soaring yen.

The oil crises triggered energy-conservation programs while motivating companies to automate production facilities. Factory automation would have been impossible without the advances in microelectronics technology, which has led to the development of such needed equipment as industrial robots.

Just when it appeared that Japan had weathered the oil crises, however, it was hit by the soaring yen and its affects on the price of exports. In one year, the yen has risen by over 30%, sparking two movements.

First, Japan's major manufacturing industries are reassessing their production facilities and are stepping up the move to overseas production. Since the 1985 Geneva Conference to discuss economic conditions, the number of companies making investments has soared, from 38 in November to 55 in December, 90 in January 1986, 77 in February, and 132 in March.

Second, corporations are reviewing their domestic productive functions and are trying to make production systems even more sophisticated.

Thus far, efforts to streamline production have focused mainly on individual processes, such as

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robotization of spot welding, arc welding, painting or coating, and assembly. Now the accent is also on increasing the use of computers in monitoring and managing production. Japan's computer manufacturers have launched vigorous campaigns to market two types of factory automation systems. One type is a 32-bit minicomputer-based system, such as Hitachi's Shopcon, Mitsubishi Electric's Factoryland, and Toshiba's Fapscon.

Data collection

These products, which sell for 5 to 10 million yen each, enable the construction of a fairly comprehensive system. They perform such tasks as transmitting work instructions to the production site, collecting data on the work performed, and managing a battery of automated equipment, including industrial robots.

The other type is based on a 16-bit computer. NEC's FC9801 has commanded the greatest following. Based on the company's popular PC9801, it is immune to the temperature and humidity changes, voltage fluctuation, contamination, and other conditions found in the plant.

Also in the 16-bit factory-automation market are Anritsu's Packet, Fuji Electric's Fasmic G500 and L-300, Fujitsu's FA work station, Hitachi's B 16/FX, Mitsubishi's FactoryMate and Meliac, Omron's FC 983, Seiko's TechnoPro models 700 and 9100 II, and Yokogawa Hokushin's Yewmac.

In addition to production-control computers, a great deal of increasingly sophisticated automated gear is being developed and deployed, including automatic guided vehicles, laser-application equipment, pattern-recognition equipment, and diagnostic systems. The functions this equipment performs will become critical to production within the next few years.

Another trend is the optimization of work cells by combining manufacturing processes and by designing modular production lines. Such increasingly sophisticated production equipment is indispensable for the survival of Japan's manufacturing industries.

MEMORY CARDS

Memory cards find wide acceptance in business

Cards containing embedded ICs are prompting a good deal of interest in Japan today. Of the two types—memory cards and smart cards that contain embedded microprocessors—memory cards are finding a greater degree of acceptance in business and are spearheading the expansion of the technology (Fig. 1); smart cards, meanwhile, have yet to progress beyond the testing stage.

The companies in this field include big semiconductor manufacturers such as Mitsubishi, Hitachi, Toshiba, and Oki, as well as printing firms and manufacturers of floppy disks, plastics, and connectors. The result is fierce competition.

The ICs embedded in the memory cards are mainly masked ROMs, which

1: IC CARDS AND MANUFACTURERS

	SMART CARDS		MEMORY CARDS	OTHER TYPES
	INTERNATIONAL ORGANIZATION FOR STANDARDS	NON-ISO		
MITSUBISHI ELECTRIC		yes	yes	
MITSUBISHI PLASTIC		yes	yes	
ARIMURA GIKEN		yes	yes	yes
ASTOR INTERNATIONAL			yes	yes
JAPAN LSI CARD			yes	yes
FUJISOKU			yes	yes
HITACHI-MAXELL	yes		yes	yes
TOPPAN PRINTING			yes	
MATSUSHITA ELECTRONIC			yes	
DAI NIPPON PRINTING	yes			
KYODO PRINTING	yes			
SHOEI PRINTING	yes			
TOPPAN-MOORE	yes			
DU PONT JAPAN			yes	
CASIO COMPUTER		yes	yes	
TOSHIBA	yes	yes	yes	
TDK			yes	
HITACHI	yes		yes	
OKI ELECTRIC	yes		yes	yes
NEC	yes		yes	
FUJITSU			yes	

Source: Nomura Research Institute

2: RECORDING MEDIA PRODUCT MAP

		TECHNOLOGY		
		MAGNETIC	SILICON	OPTICAL
CAPACITY	LOW	BUBBLE MEMORY	MASKED ROM EPROM EEPROM SRAM DRAM	OPTICODI-STABLE ELEMENT
	MEDIUM	MAGNETIC CARD	MEMORY CARD ROM CARTRIDGE	LASER CARD OPTOELECTRONIC IC CARD OPTICAL IC CARD
	HIGH	MAGNETIC TAPE FLOPPY DISK BUBBLE-MEMORY CASSETTE HARD DISK	RAM DISK	OPTICAL DISK CDROM DIRECT-READ-AND-WRITE DISK ERASABLE-DIRECT-READ-AND-WRITE DISK OPTICAL TAPE

account for the overwhelming majority of cards in use, followed by static RAM, EPROM, and EEPROM technology.

Masked-ROM cards currently make up 90% of the market. In 1985, the market for memory cards totaled an estimated 90 million cards, or 16.5 billion yen. The main use of the ROM models is in electronic games; RAM models are designed to replace floppy-disk drives.

Fast access

As an erasable recording medium, memory cards offer high-speed access and convenience; they do not require an actuator, as do floppy-disk drives, and they are right in tune with the trend toward smaller, more personal, energy-saving equipment. These pluses have fueled expectations that memory cards will replace floppy-disk drives and find use as external memories for information equipment. In the long term, such improvements as increased capacity and intelligence could lead to an even broader range of applications. Nomura Research Institute expects floppy-disk drives, memory cards, optical cards, and optical disks to dominate tomorrow's recording-media market (Fig. 2). The memory card will be the technology of choice in applications requiring less than 1 megabyte of capacity. Floppy disks will cover the 1- to 10-megabyte range, and hard disks will cover the territory

Focus on NMB Semiconductor

NMB Semiconductor, founded in 1984 as a subsidiary of Mineaba Co., is dedicated to the development of sophisticated CMOS memories. Its CMOS 256-K dynamic RAMs and 64-K static RAMs have exceptionally low power consumption and high speed. To design these highly reliable devices, the company licensed advanced design technology from Inmos Corp. and combined it with advanced processing capabilities developed in-house.

Takumi Tamura, president

Wafers are fabricated in ultraclean rooms having no foreign particles larger than 0.1 μm. The company's fully automated microfabrication lines are controlled by advanced computer systems, and remote-controlled robots perform all operations. The microfabrication lines feature a 5 : 1 projection and exposure system, a high-performance, fully automatic photolithography system, single-wafer plasma-etching equipment, a complete range of chemical-vapor-deposition equipment, and high-performance measuring equipment.

NMB Semiconductor also has established an ultramodern R&D center for circuit design and process development at its Tateyama plant. The company is doing all pilot runs of its products here. Among the projects that it has under way are the development of 1- and 4-Mb DRAMs, high-performance SRAMs, EEPROMs, 1-μm processing techniques, and submicron processes. The 1-Mb DRAMs are already in the testing stage, and samples will be shipped soon.

between 10 and 500 megabytes per spindle. Optical-disk drives will have the large-capacity segment. Although the memory card has the lowest capacity, its advantages—small size, high-speed access in the order of several nanoseconds, and low energy consumption compared with floppy-disk drives— suit it for a wide range of applications in all types of portable equipment. Nomura Research Institute projections show a five- to tenfold increase in the size of the domestic Japanese market for memory cards in the next five years.

ARTIFICIAL INTELLIGENCE

Systems and software emerge from the laboratories

Japan's information industry is shifting its emphasis from traditional hardware technology to software and new-generation architecture development. And one of the most important new fields for Japanese computer manufacturers is artificial intelligence. For a time, Japan was swept by a kind of AI boom ignited by the fervor of the Fifth Generation Computer Project and the great response that project evoked overseas. Though the boom has since subsided, AI has progressed to the point that prospective suppliers and users are searching for a means to

generate workable AI systems and applications, as well as a market.
Basic AI research into cognitive science and pattern recognition is being conducted by major corporations and universities. The areas of greatest activity are knowledge engineering and related computer technology. The Institute for New Generation Computer Technology in Tokyo (ICOT), which is the scene of work on the Fifth Generation Computer project, is also doing research in these areas. Its membership consists mainly of researchers dispatched from domestic computer manufacturers.
The project's first phase, which started in 1982 and lasted three years, resulted in two systems. The first is the personal sequential-inference machine, a logic-language work station that performs 30,000 logical inferences per second (lips). It is being manufactured and marketed by Mitsubishi Electric Corp., Tokyo, and is selling for 20 million yen. The second is a relational data-base machine called Delta, still in development.
The systems are linked by a local-area network with a backend inference machine that performs over 100,000 lips. This forms the basis of the project's middle phase, which is under way. The machines' operating systems are written in a Prolog-based logic language; Mitsubishi Electric has also developed knowledge-acquisition support systems and knowledge-representation systems.

Guarded horn

The four-year middle phase is concentrating on development of a parallel inference machine. Guarded Horn Clause was adopted as the description form of the logic language for parallel programming. Plans call for the manufacture of a prototype of computer with a data-flow architecture with eight processing modules. Testing and evaluation of parallel-processing formats will be followed by development of a parallel processor with approximately 100 modules. Target completion: 1988. Plans also call for the construction of a knowledge subsystem, an intelligent interface that accepts common English statements, and a programming tool.
The goal for 1991, the year of the project's third and final phase, is a system containing several applied expert systems. These will include a natural-language inference machine that performs 100 million to 1 billion lips and has 1,000 processing modules, a 100- to 1,000-gigabyte knowledge base, an advanced programming environment, a specification-description system, and automatic programming.
Other research organizations are also working on parallel processors with an eye on AI applications. Tests are under way on Prolog machines at Nippon Telegraph & Telephone, the University

Focus on Oki Electronic Devices Group

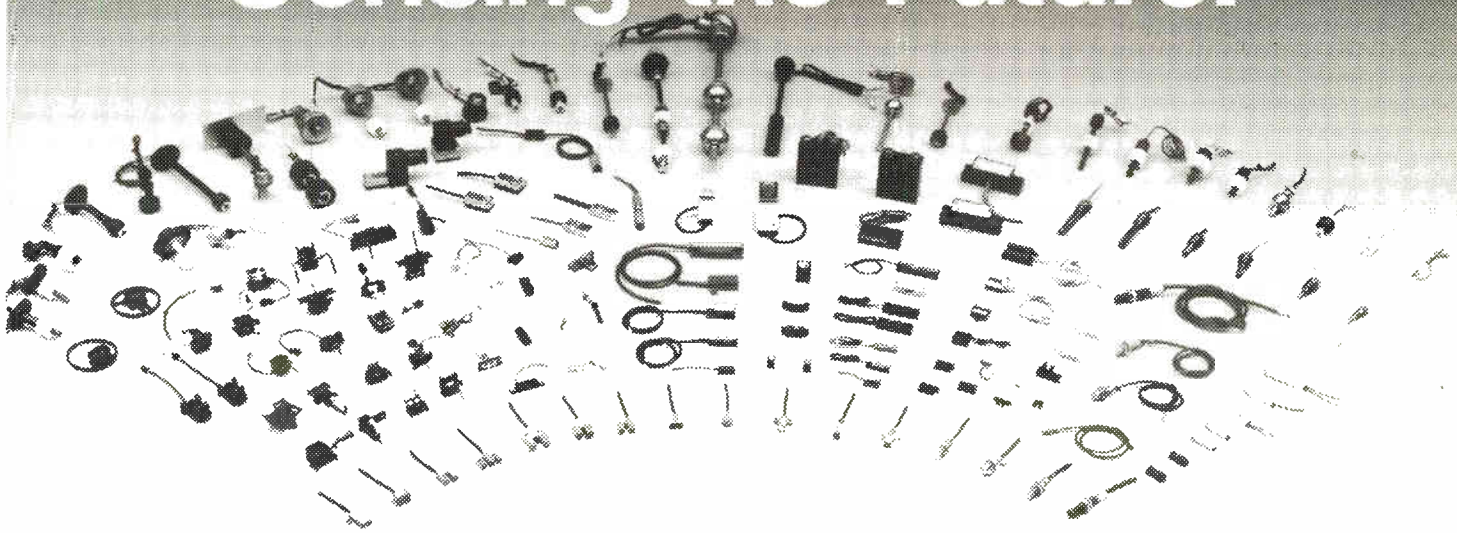
Oki Electronic Devices Group's plan is to continue to automate its world-class production facilities to guarantee customers faster and more consistent delivery of products. A second full-scale wafer-fabrication plant at Miyazaki has just been completed, with a third under construction; a new R&D production line in Hachioji is up and running; and a plant near Sendai will have submicron capability. Oki also has expanded its capacity for surface mounting and for the manufacture of hybrid ICs.

Masao Nogami, managing director

The company's focus is not limited to production of leading-edge technology, however. It is reinvesting a large percentage of profits into technology-focused R&D. High on the list of priorities is expansion of its gallium arsenide capability; Oki has been using GaAs ICs in its mobile cellular telephones.

Moreover, Oki is producing 3-, 2-, and 1.5-μm application-specific ICs with a variety of gate counts as well as a number of packaging options. And it is continuing to broaden its design capabilities.

Sensing the Future.



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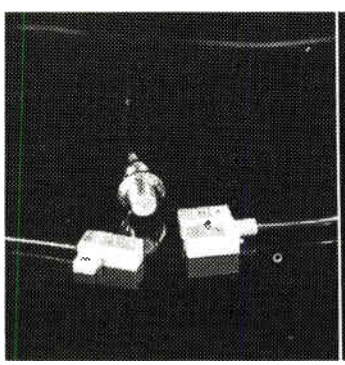

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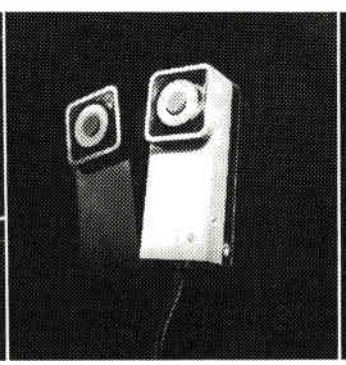
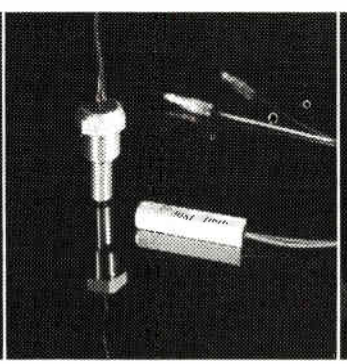
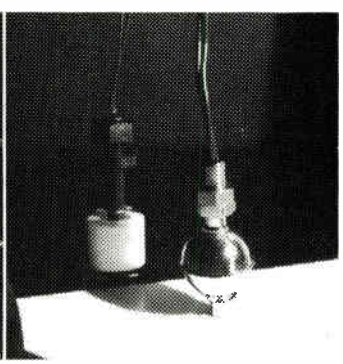
The ME Series, our latest proximity sensors, are limited to use with magnets or ferrous metals, but are high in precision and performance and extremely low in cost.



■**USS-101A Photoelectric Sensors**
Unlike conventional ultrasonic sensors, our USS-101A has a detection range of 5 to 30 centimeters. It is suitable for transparent and translucent targets at short ranges.



■**RC Series Thermal Sensors**
The RC Series thermal sensors are available in thermosensitive ferrite, permanent magnet and reed switch varieties. In contrast with bi-metal types, the RC Series has an constant detection point and snap action.



■**FS Series Level Sensors**
The FS Series provides a wide variety of sensors in every shape and size for different liquids and switching applications.

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- Computer Link Function
  Personal computer link software is available for writing, editing, transferring and printing out programs. Applicable personal computers: IBM PC5150, PC5160XT and PC5170AT
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  * Ladder diagram writing
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◀ Printer control unit is available for ladder diagram printout

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of Tokyo, Kobe University, and the University of Tokushima. Lisp machines are being tested at NTT, Ministry of International Trade and Industry's Electro Technical Laboratory, and Tohoku University. Similarly, Smalltalk work stations are under development at Oki Electric Industry, and research on software and systems is being done by numerous universities and manufacturers.

Market blooms

And now the market is beginning to bloom; rising sales have been reported for AI work stations made by such U. S. companies as Symbolics, Sun, and Xerox, as well as for Fujitsu's Lisp processor, Facom. Likewise, the market for expert-system development tools, which started with Toyo Information Systems' Brains in 1983, now has more than 10 entries, including U. S.-made models. Two of the more notable entrants are NEC's Excore and Fujitsu's Eshell. In addition to computer manufacturers, a number of software houses have also come up with products for this market.

Another notable development is the sales of Lisp and Prolog interpreters, particularly those for use with personal computers. All these products are contributing to the emergence of AI in the marketplace.

Virtually all the expert systems that have been developed to date have been prototypes, but instances of actual use in the field are increasing. NEC, for example, coded the software for its gate-array computer-aided design system through the use of expert systems. The inference portion is written in Prolog and can call conventional Fortran subroutines. The circuit-wiring rules number 230, and in some cases the system has halved the usual time required for circuit development.

At Mitsubishi Electric's Central Laboratory, researchers used Prolog to prepare an electrically powered analytical support system. The rules number 100, with as many as 1,000 data inputs, called facts, of varying types. Hitachi used a rule-based language for part of a manufacturing-control system ordered by a steel company, reducing developmental costs and making the system easier for the user to work with. The inference program is written in C, and the control system operates in real time.

Some prospective end users of expert systems are also trying their hand at development. These efforts include:

Focus on Fujitsu Ltd.

Fujitsu Ltd. started as a maker of telephone switching systems about 50 years ago and has since become an all-around supplier of telecommunications equipment, computers, and semiconductors.

The company designed equipment for several test runs of the integrated services digital network.

Ryoichi Sugioka, board director

The D70 private branch exchange, which the company developed with Nippon Telegraph & Telephone Corp., has been used as the service nodes in NTT's Information Network Systems trial, an ISDN experiment that started in 1984. A number of the voice-data systems are being introduced throughout Japan. Fujitsu's Fetex-150 system, another PBX, also integrates voice and data. This ISDN node machine was put into field test in 1985 using an actual network in cooperation with Singapore Telecom.

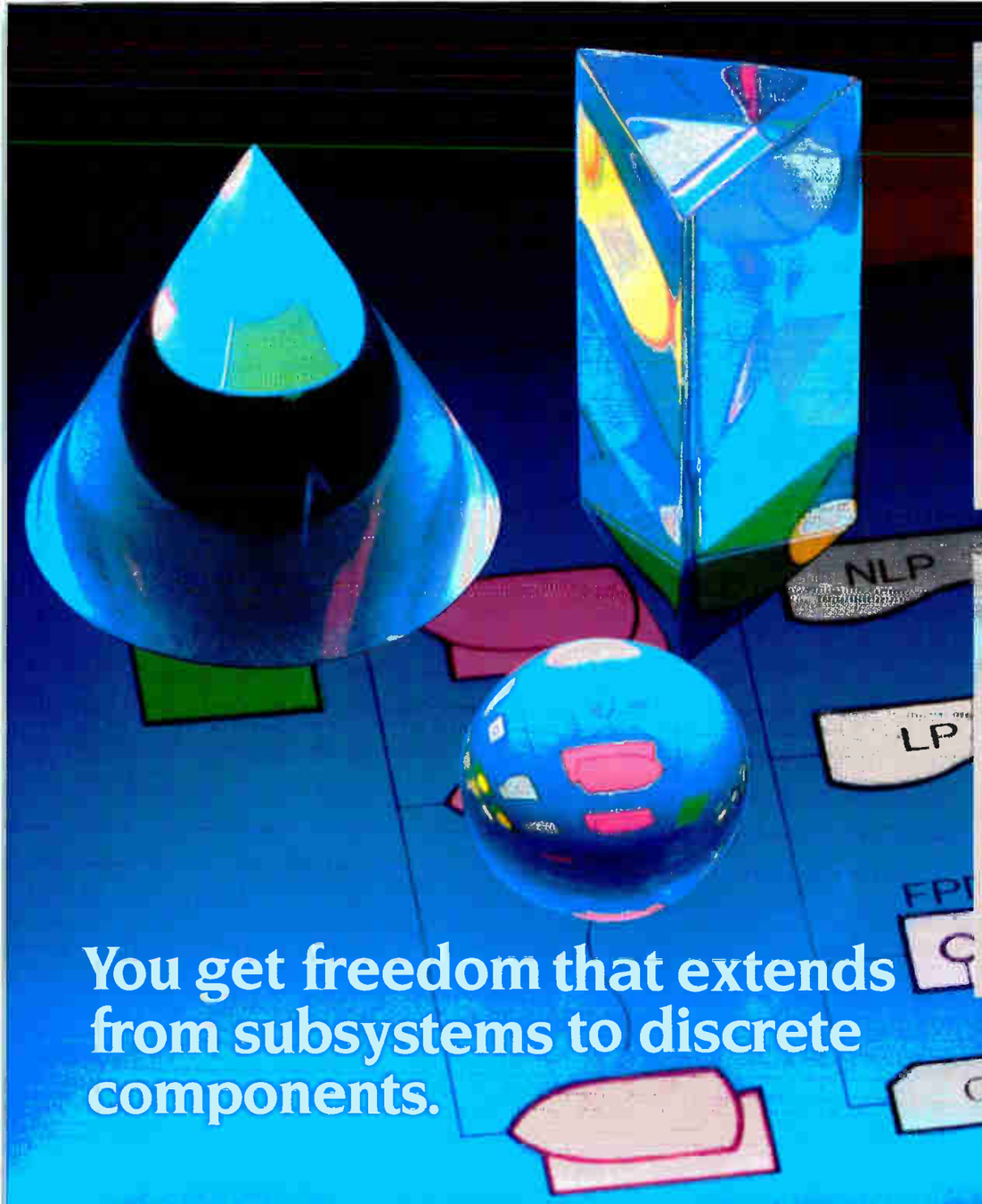
Fujitsu's next target for ISDN development is the building of operation and maintenance facilities and implementation of broadband ISDN, which would allow any kinds of communication without limits or restrictions. It uses very high-speed packet-switching technologies.

Since the deregulation of the Japanese communications field in 1985, the need for advanced, multipurpose corporate communications systems have been increasing. To meet the demand, Fujitsu is providing new communication systems that integrate private branch exchanges, multiplexers, and other gear under the Corporate Information Network System (Coins).

Fujitsu's Coins contributes to office automation in two ways: with network components, such as digital PBXs that include integrated voice and data terminals, as well as with communication-processing systems such as multimedia main system for voice, facsimile, and text and with packet-switching systems.

The company has promoted technology transfers to overseas cooperating companies as well as to a subsidiary company in the U. S. And it has encouraged the establishment of local product development, manufacturing, and sales, and customer support.

Fujitsu's switching systems play a key role in any kind of communication networks including both public and private ones. They are still advancing steadily towards coming ISDN era with integration of computer and transmission systems.



You get freedom that extends from subsystems to discrete components.

Fujitsu gives you the widest possible selection of electronic components. In the subsystem category, we offer ergonomically designed keyboards and space-saving plasma display panels which enhance the interface between man and machine. Among discrete components, we manufacture connectors and hybrid ICs that provide the user with the latest in high density technology. We even offer custom designed components in addition to our formal lineup of products.

Every component we manufacture is subject to an exhaustive series of strict quality assurance tests. It's our way of guaranteeing products of the highest quality and reliability. This kind of commitment to perfection is what made us Japan's No. 1 computer maker and a world leader in telecommunications.

It's also the kind of commitment that is helping us to make perfect electronic components.

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PLASMA DISPLAY PANELS

Fujitsu's thin, flat plasma display panels provide a bright, flicker-free, space-saving alternative to conventional displays. Fujitsu also offers a CRT-compatible interface that makes these graphic plasma displays compatible with personal computers on the market today.

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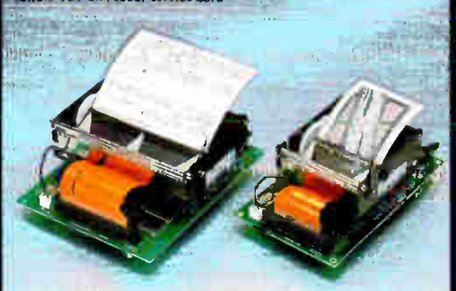

THERMAL PRINTERS

Fujitsu's 20- and 40-column-wide line-dot thermal printers, recognized by UL, feature quiet, maintenance-free operation and are finding increased application in POS terminals, medical and measurement equipment.

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RELAYS

Fujitsu continues to develop durable relays that are both compact and low in power consumption. These lightweight relays are widely used in electronic switching systems, car electronics and portable equipment.

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KEYBOARDS

Fujitsu's low-profile keyboards are ergonomically designed to provide the most efficient link between man and machine. In addition, these keyboards are fully compatible with major brands of personal computers on the market today.

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BUBBLE MEMORIES

Fujitsu's newly developed 4 Megabit bubble memory device means greater nonvolatile solid-state file memory for equipment subject to rough operating conditions, ranging from NC machines to industrial robots.

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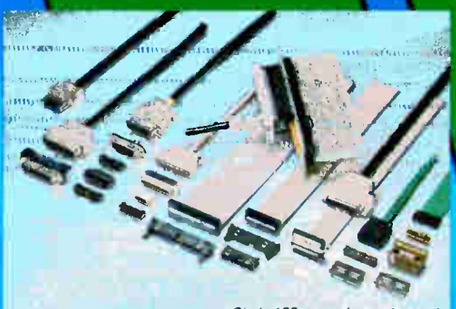
HYBRID ICS

Utilizing the latest in thick-thin film combination technology, double-sided packaging technology and LSI mounting technology, Fujitsu's high quality hybrid ICs provide the system designer with unlimited custom applications.



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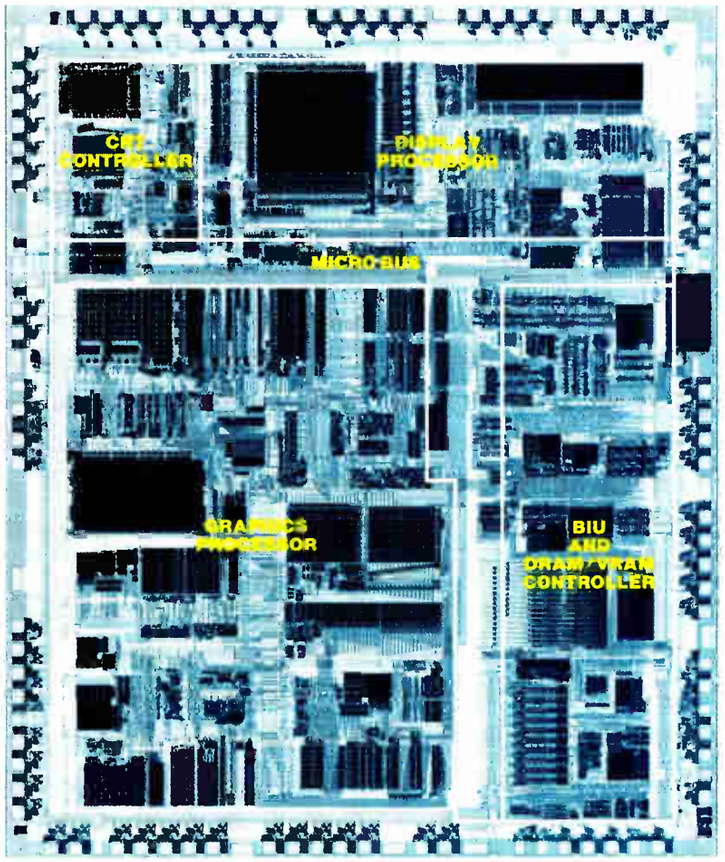
CONNECTORS

In keeping with the latest trends in high density product development, Fujitsu has made a number of valuable contributions to connector technology. These include half-pitch, surface-mounting, press fit, EMI shielding and double IDC for a more efficient link between peripherals.

FUJITSU ELECTRONIC COMPONENTS

DOES WINDOWS.



Intel's 82786 graphics coprocessor supports its family of 16- and 32-bit central processing units.

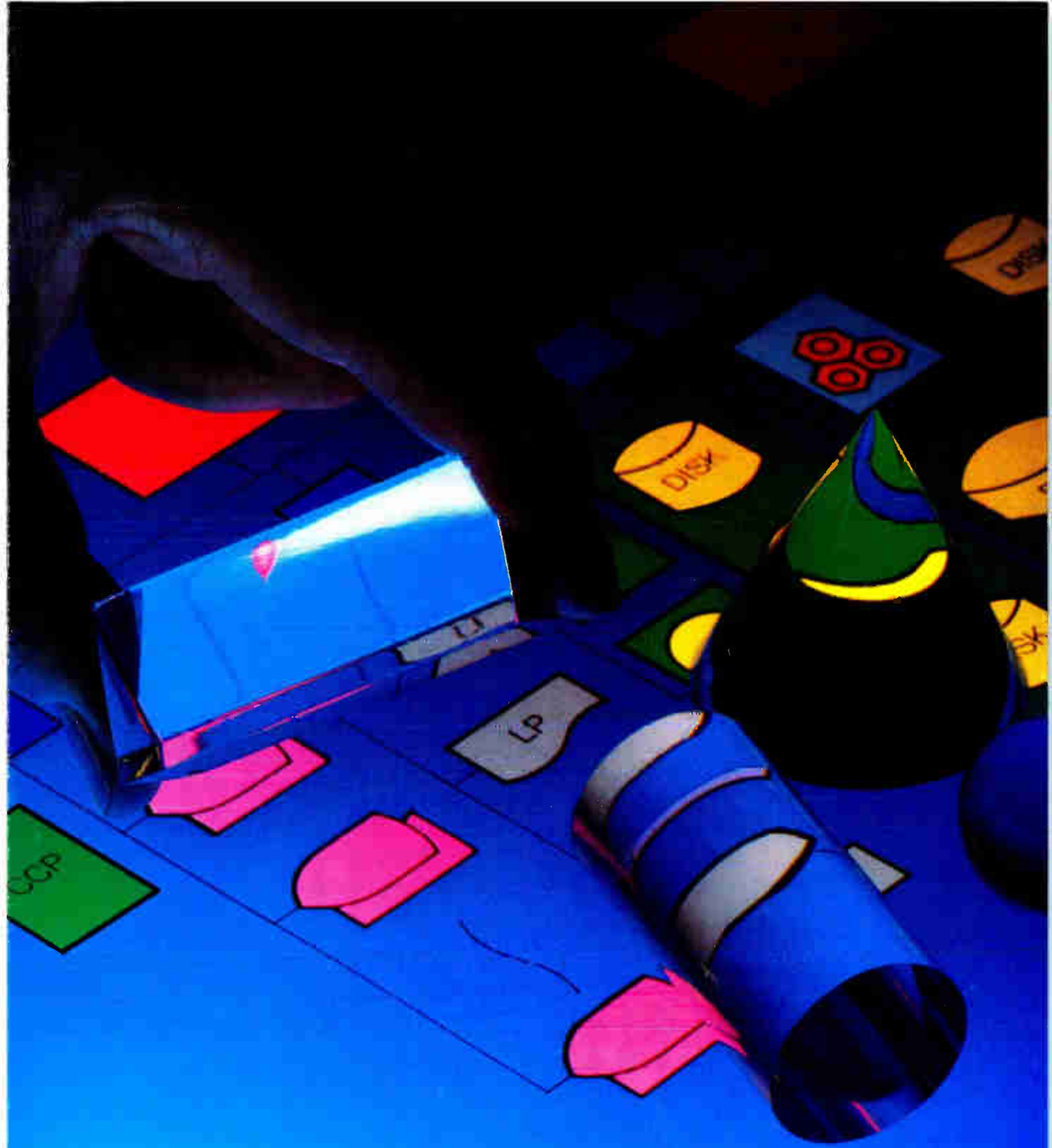
"Two completely different kinds of end customers seem to be fueling the embryonic graphics chip market: the personal computer user in business, and the designer on a work station. Intel Corp., long reported to be developing a graphics-oriented microprocessor, is finally announcing its 82786 graphics coprocessor for both applications.

Demand for multiple-windowing capability is on the rise, especially for multitasking chores in the office environment. The 82786 implements this capability in hardware. Each application can have its text and graphics drawn into separate regions of memory, which are then combined within windows of the same display. Large amounts of overhead associated with graphics tasks can be offloaded from the main system CPU by storing more text and graphics information in memory than is shown in the display..."

Excerpted from an exclusive article in the May 19, 1986 issue.

McGraw-Hill Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE



Most dream systems are just that. Dreams.

Fujitsu gives system designers the freedom to make those dreams real.

System designers need freedom. Freedom to pull ideas out of the air and turn them into reality. The kind of freedom that you get with Fujitsu electronic components.

You get this freedom because our components come in such a broad range. From keyboards to hybrid ICs. Because they're flexible enough to adapt to any system. Large or small. Complex or simple. And because we can alter our own product design to conform with your unique specifications.

With Fujitsu there are no limitations. Only possibilities.

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• Consultation systems to keep track of construction-material regulations and technology by construction companies.
• Failure and trouble diagnostic systems and system operation planning systems by electric power companies.
• Automotive diagnostic systems.
• Management and diagnostic systems for chemical and steel plants.
• Railroad diagramming systems.

In most cases, these are small-scale systems, with rules numbering only in the hundreds, for use in research on developmental methods and system appraisal.

Translation machines

Also in development are machines to translate Japanese to English. Major computer manufacturers and office-equipment manufacturers along with the big translation companies are active here; still needed are improvements in precision and cost. For now, the major translation systems are Fujitsu's Atlas, NEC's Pivot, Hitachi's Athene, and Bravice International's (a translation company) Micropak, for use with personal computers.

In sum, it remains difficult to construct a practical system for solving the ill-structured problems that had been the original goal of AI. Present systems address particular problems of a highly logical nature.

Development in this direction is likely to be pursued mainly in engineering divisions and result in preparation of electronic manuals for in-house use and in systems to boost the value-added content of the existing ones, with an emphasis on increased practicality. General use, particularly in offices, will likely take the form of low-priced user-friendly work stations that utilize 32-bit personal computers for user-specific intelligent data bases and how-to bases.

The emergence of AI will bring more programming languages into general use and will improve in man-to-machine interfaces throughout the information-processing industry. End-users have traditionally worked with Fortran and Cobol, but such languages as Lisp and Prolog would come to the fore. Conversely, AI systems will have to be able to work with existing Fortran and Cobol systems. A more immediate development, however, will be the integration of AI programming techniques and graphic interfaces into conventional equipment. Improvement of the graphic interface will probably become a critical item on the agenda

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for research and development. The primary tasks in the short run are developing a methodology for the construction of large-scale systems and building the hardware to execute them. The methodology could be realized around 1990 if the Fifth Generation project proceeds on schedule. Sophisticated systems arising through the integration of pattern recognition and robotics for use in engineering could be the main AI topics in the 1990s, at which time construction of personalized bottom-up AI systems are also likely to expand.

RECORDING MEDIA

Makers of audio and video tapes look at ways to boost sagging sales

Japan's recording media industry has expanded greatly in the past few years, boosted mainly by the burgeoning market for video cassette recorders. Today, however, domestic VCR tape production is down, tripped up by slumping exports as a result of the strong yen (see chart), the saturation of the market in Japan, and the emergence of such technologies as 8-mm video tape. Now a number of companies are taking measures to regain their once-healthy positions.

Video tapes have felt the brunt of the effect of the strengthening yen—the dollar, which stood at 255 yen in January 1985, fell to 165 yen as of May 1986—because approximately 80% of total production is exported. To cope with the situation, companies are both boosting their wholesale prices in the U. S. market and studying the prospects for a complete shift to overseas production. TDK Electronics sparked these wholesale price hikes when it announced 2% to 7% increases effective May 1, 1986. The other suppliers followed, and the hikes should settle at 10%.

At present, the only Japanese supplier whose overseas facilities carry out the coating process—the part of tape making that requires the most advanced manufacturing know-how—is Sony. Its Georgia plant produces 1 million tapes monthly. The overseas production operations of the other Japanese suppliers merely amount to the exporting of pancakes from Japan for cassette assembly. With the drop in export feasibility due the strong yen, however, all of the suppliers have begun to consider boosting their ratios of overseas production.

JVC, for example, has announced plans for construction of a video tape plant in Alabama in the U. S., and Hitachi-Maxell Ltd. is reportedly increasing the output of its overseas plants. It remains to be seen whether this boost in overseas production will

Focus on Nippon Automation Co.

Michio Sakamoto, president

In its 18 years of existence, Nippon Automation Co. has developed reed switches, Hall-effect elements, magnetoresistors, and other sensors, receiving a large number of patents and registered applications. The company's focus is on the development of applied laser, piezoelectric-effect, microwave, ultrasonic, and photoelectric technology employing a variety of sensors, including proximity, thermal, and level.

In 1985, Nippon Automation developed a high-frequency oscillating proximity sensor. It also offers the ME series—low-cost high-performance magnetoresistor element proximity sensors for sensing steel plates and magnets. Its other lines include ultrasonic and photoelectric sensors.

Nippon Automation believes that, as computers continue to evolve, sensor technology will become increasingly critical. In some personal computer applications, sensors are expected to play a major role as they are used to replace the five basic human senses. In resource conservation, energy conservation, environmental protection, and medical technology, the demand for sensors has come to govern the design of systems.

JAPAN

SPECIAL ADVERTISING SECTION

MAGNETIC TAPE AND VCR PRODUCTION					
	1981	1982	1983	1984	1985
VIDEO TAPE					
UNITS (METERS² IN MILLIONS)	320	560	716	932	1,308
YEN (IN MILLIONS)	173	286	314	314	347
AUDIO TAPE					
UNITS (METERS² IN MILLIONS)	300	307	363	383	358
YEN (IN MILLIONS)	130	131	144	149	137
VCR					
UNITS (MILLIONS OF SETS)	9.498	13.134	18.217	27.124	28.538
YEN (IN MILLIONS)	1,087	1,285	1,514	2,020	1,812

Source: Ministry of International Trade and Industry

also entail coating processes.

Some 21.9 video tapes were purchased for every VCR in the Tokyo area in 1985, according to the "Survey of Audio and Video Tape Consumption" released by the Magnetic Tape Industrial Association last February. This represents just a slight increase from the 19.8 video tapes purchased in 1984.

Because the number of video tapes purchased per VCR has begun to level off, further growth in the tape market depends on further sales of VCRs. Though on a unit basis 1985 VCR production increased by 5.2% over 1984, on a monetary basis it fell by 10.3%—the first time production value fell from the previous year.

Unfortunately, for the near term, the coming years should bring more of the

same. The development of new recording media technology continues at a rapid pace. The main focuses are improving recording density of the tape and developing new media such as video disks and still-video disks like those from Sony and Canon.

Barium ferrite

One development drawing a great deal of attention is recording materials for magnetic tapes. Three types of materials are the subject of intensive efforts: metal powder made of high-purity ferrite, barium ferrite magnetic powder, and a vaporized cobalt-nickel alloy. Development is furthest along in magnetic metal powder, which not only is used for 8-mm tapes, seen as the next generation, but also is the prime candidate for digital audio tapes, which will come to market this autumn. Initially, because the crystals in this powder are finer than ferrite crystal, they were prone to clump during coating, making the magnetic metal powder difficult to work with in mass production. Nevertheless, all the tape suppliers have already developed the production technology needed to supply themselves with tapes for 8-mm VCRs, and it appears that the major problems have been overcome.

The industry is looking at barium ferrite for use in vertical magnetic recording because it could dramatically boost the recording density of floppy disks. It already is being used in audio tapes and is used in the high-grade VHS-C tape that was unveiled by JVC in June. Furthermore, it is one of the constituents of the magnetic powder used in digital audio tapes. With a saturation point midway between metal and gamma-ferrite, it is a fine candidate for use as magnetic powder.

Vaporized tape

The development of vaporized tape is moving ahead at Matsushita Electric, where it has resulted in commercial audio products. The process involves vaporizing iron, cobalt, nickel, and other highly magnetized materials and depositing them on a base film in a vacuum. Tape so produced delivers excellent performance at high frequencies. But it has several critical drawbacks: The tape still lacks durability, and the method is not conducive to mass production. Developments are also coming quickly in the market for other recording

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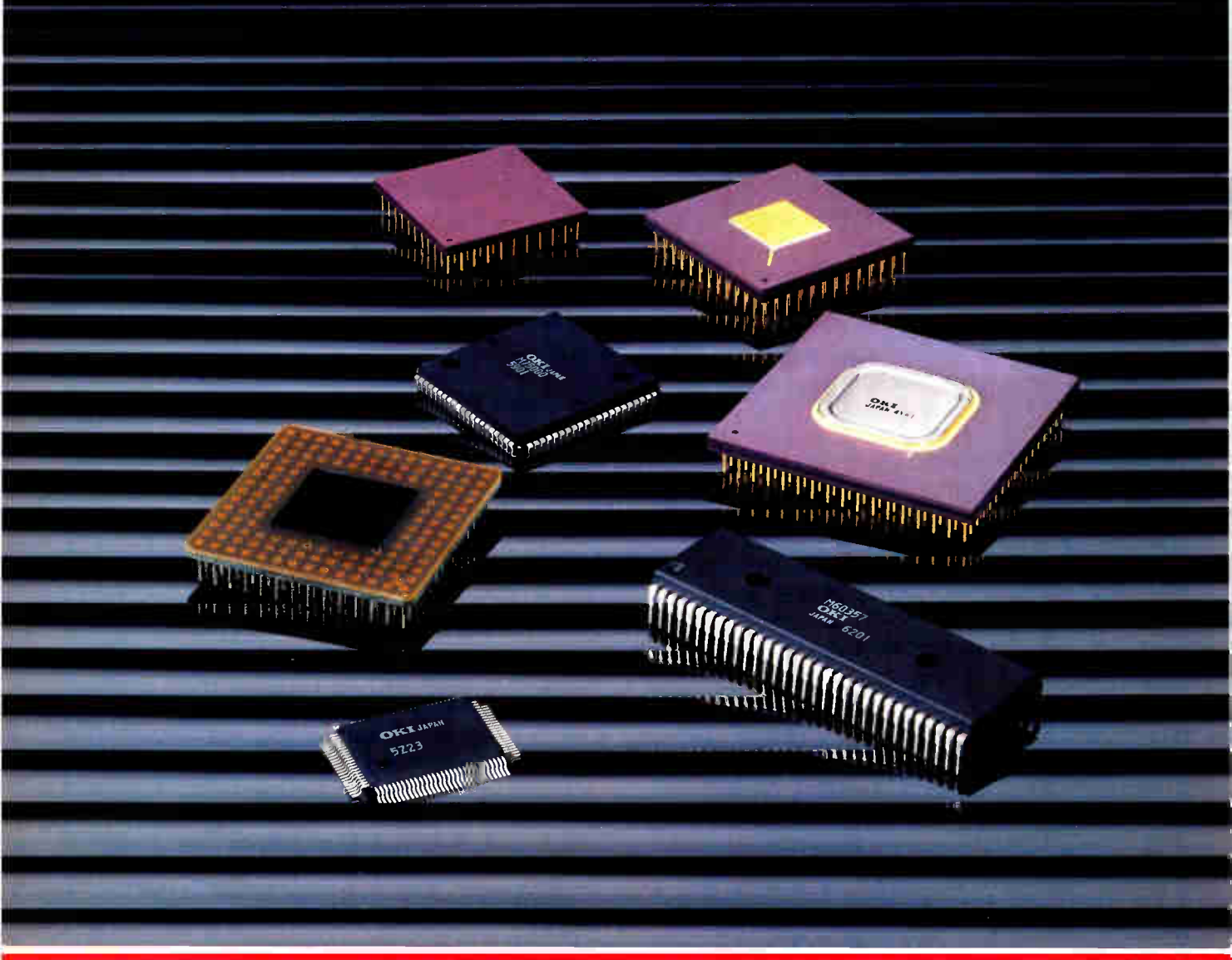

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70V000 Series VERY HIGH SPEED		*70H000 Series HIGH SPEED*		*70000 Series*	
# Gates	# I/Os	# Gates	# I/Os	# Gates	# I/Os
700	66	3289	86	387	44
1000	66	4290	104	720	62
1500	66	6000	130	1445	88
2000	80	8024	148	2000	106
2500	80	10008	172	4205	120

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OKI offers the system designer maximum ease in low-power Customer-Specific logic integration by minimizing customer time/cost/expertise requirements.

To our broad range of CMOS CSIC product options, OKI adds total development support—from chip design to fabrication and testing—based on longterm experience: Gate Array designs since 1977; Standard Cells since 1979; with on-going Custom chip solutions.
Enhanced by OKI's design/process leadership: with 3-micron CMOS in 1981; 2-micron in 1983; 1-micron CMOS in late 1985.

Application of these advances can help designers meet all gate-count, chip-size and schedule criteria.

OKI CMOS GATE ARRAYS are used for fast turnarounds and extra development ease—quickly built from OKI's predesigned dual-layer metal chips.

OKI CMOS STANDARD CELLS are selected as the production volumes rise, for single-chip integration in about 25% less chip space—designed from OKI cell libraries of logic, RAM and ROM functions.

Transparent software is OKI's key to instant conversion. With totally compatible cell libraries, OKI can configure the standard cell directly from the gate array design—no need for a new data base.

OKI CMOS CUSTOM CSICs can reduce chip size to the absolute minimum for very high volume runs. OKI's very small geometries permit major silicon/cost savings while complementing the logic with special functions such as analog and high voltage, high current cells.

Flexible options in CAD and packaging

CSIC designs can be captured on either a Mentor or Daisy Work-station. Yours or ours. You can work alone or work with an OKI Design Center—we can take over implementation at any development stage. OKI's software was created to simplify logic, timing and fault simulation; auto place and route; plus PG and test tape generation.

To package the design, OKI versatility satisfies the most demanding specifications for compactness, configuration and pin count. OKI CMOS CSICs are being produced in plastic DIP, PLCCs and flat packs, as well as plastic and ceramic Pin Grid Arrays. OKI application engineers will assist in the selection of optimized packaging for your application.

Total system integration in OKI CMOS VLSI

With complete CMOS CSIC capabilities on call, OKI's commitment to full-service and broad product-line support extends low-power VLSI across the board: CMOS MCU/MPUs, VLSI memory, telecomm, voice chips, display drivers and peripherals.

All from a single market-responsive source. And all are volume-produced in one of the world's most highly automated manufacturing plants. OKI has invested over $360-million to expand and robotize our masking, prototyping, wafer fab, assembly and test facilities, to assure our customers both quality and cost control.

"CSIC" vs. "ASIC".

Industry has long used the term "ASIC" (Application-Specific Integrated Circuit) to refer to any combination of Gate Array, Standard Cell, or Custom products.

We at OKI feel that these products would be better described by the term "CSIC" (Customer-Specific Integrated Circuit) since they are truly unique to an individual customer rather than to an application.

We believe that "CSIC" will evolve as the preferred acronym.

OKI

Circle 135 on reader service card

Oki Electric Industry Co., Ltd.: 10-3 Shibaura 4-chome, Minato-ku, Tokyo 108, Japan Tel: Tokyo 454-2111 Telex: J22627 Fax: Tokyo 452-5912 (GIII)
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Heat-Conductive and Flame-Retardant Insulating Silicone Rubber

Shock-absorbing silicone rubber replaces fragile mica spacers. High elasticity and low thermal-contact resistance eliminate grease, for easy assembly and long-term durability. Lower tightening torques reduce semiconductor breakage. Wide −60~+200°C temperature range with excellent resistance to weather, corona and arc discharge and corrosive chemicals. Can be punched from sheets, press moldec or extruded in a variety of sizes and shapes.

Applications:

- Heat-conductive insulators for power transistors, ICs and other semiconductor devices.
- Heat-conductive insulators for thermistors in heated containers, electric heaters, etc.
- Insulator and low- or high-temperature heat-transfer media for temperature fuses and temperature sensors, in microwave ovens, electric heaters, etc.
- Replacement for molded silicone-rubber parts in applications where a heat gradient is present, such as insulation for magnetron tubes in microwave ovens, motor and transformer mounts, etc.

Typical Properties:

Color	Gray-green
Hardness	75 (Shore A)
Tensile strength	50kg/cm^2
Elongation	100%
Tear strength	12.0kg/cm
Bulk resistivity	$1.2\times10^{15}\Omega$cm (at 1kVDC)
Dielectric constant:	4.6 (at 60Hz)
	4.5 (at 1kHz)
	4.5 (at 1MHz)
Dielectric dissipation factor:	0.0028 (at 60Hz)
	0.0017 (at 1kHz)
	0.0026 (at 1MHz)
Dielectric strength:	24kV/mm (AC)
Thermal conductivity:	2.9×10^{-3} Cal/cm. sec. C
Flame retardance	94-VO (UL-94)
(UL File Number	E58126)
Minimum Thickness	0.10 mm

* Glass-fiber reinforced SARCON GRT (94-V0) & Adhesive coated SARCON (94-V0) are also available.

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Circle 136 on reader service card

media, the most notable of which is the jump in demand for video disks. Although some potential equipment buyers are waiting for one of the two formats—very high-density or laser disks—to emerge as dominant, sales have already topped those of video tape in Japan.

Development is proceeding on such optical-disk formats as direct read and write and erasable DRAW. Numerous materials manufacturers are active here. Programs also are under way to develop still-video tape using floppy-disk technology.

SEMICONDUCTORS

Companies keep rolling out products though the market remains slack

Compared with its steady growth in the past, Japan's semiconductor industry has been on a rocky road these past few years. For an industry that grew 25% annually in the early 1980s—production totaled 2 trillion yen in 1984—the slowdown in 1985 was a shock. Though demand has shown strong signs of building this year, trade friction and the strong yen have put a damper on exportation, which accounts for about 37% of total production.

Despite these so-so circumstances, new products keep coming to market. At the beginning of this year, for example, the big semiconductor manufacturers started marketing 1-Mb dynamic RAMs and 256-K static RAMs.

Notable in the memory field is the evolving market for EPROMs and EEPROMs. Because of its limited scale, this market has been occupied mainly by products from midsized manufacturers, such as Seiko Epson and Ricoh, and by imports. These chips are key devices in IC and memory cards, however, and demand for them will jump along with production of the cards. This has led such major players as Toshiba, NEC, and Fujitsu to increase their presence in the field and Mitsubishi Electric to enter it.

Each participant is aiming for high-speed access times throughout its 256-K, 512-K, and 1-Mb EPROM families. This is supplemented by research on single-chip microcomputers that have on-chip EEPROM circuitry. Likewise, the variety of product types offered is gradually growing, with an emphasis on lower prices and parts with special-purpose features, such as a 256-K EEPROM that can batch erase all bits.

The slump in the semiconductor industry has also had a great effect on the semiconductor-equipment manufacturers, because it has led to a decline in capital investment by

semiconductor manufacturers. Capital-equipment investment by the nine big semiconductor manufacturers—NEC, Hitachi, Toshiba, Mitsubishi, Fujitsu, Oki, Matsushita, Sharp, and Sanyo—had grown at an average of over 20% annually and even recorded an increase of 105% in 1984. However, the 780 billion yen that they spent on capital equipment in 1984 dwindled to just 606 billion yen in 1985, a 22% decrease.

Moving the market

Hoping to get the market moving up again, equipment manufacturers are stepping up development of X-ray lithography, which has been coming to the forefront in recent years. One such example is the unveiling of X-ray step-and-repeat equipment by the aligner manufacturers Nippon Kogaku and Canon.

In the same vein, Micronics, a forerunner in X-ray lithography, has switched from batch exposure to the step-and-repeat method for new products. Although this equipment is designed for use in R&D, all this activity indicates that manufacturers are on the path to next-generation manufacturing equipment.

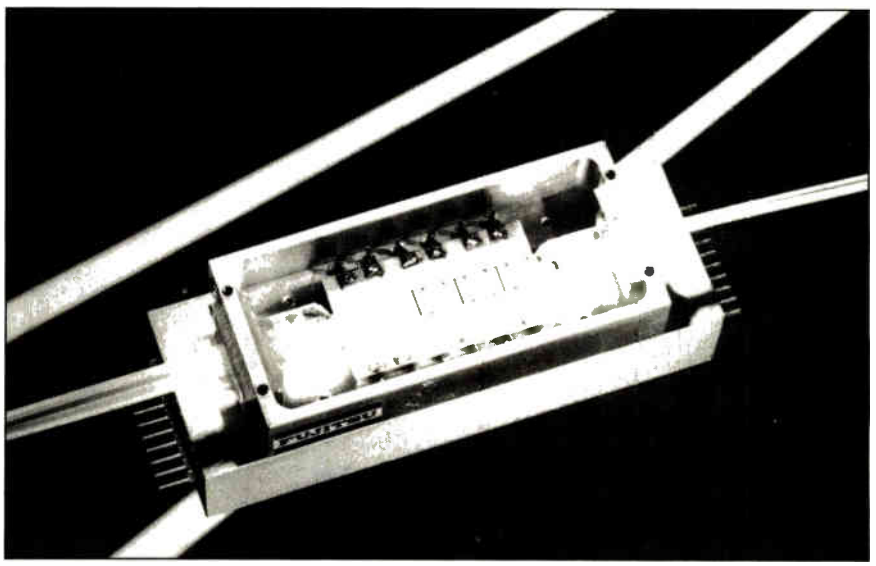
R&D efforts in synchrotron radiation have also been gaining momentum. Besides NTT's current construction of an in-house synchrotron-radiation facility, which is being watched closely by manufacturers, the High Energy Physics Laboratory has completed its synchrotron-radiation facility, which contains the biggest accelerator in Japan. The major semiconductor manufacturers have set up their own beam lines at this facility and have begun testing.

Mask manufacturers Dai Nippon Printing and Toppan Printing are already providing samples of masks to support research in X-ray lithography, and resist samples have been shipped by such manufacturers as Toyo Soda, Daikin, and Kureha Kagaku.

The domestic market for semiconductor materials—masks, semiconductor gas, resist, wafers, lead frames, and package materials—equals roughly 30% of the IC production value and totaled more than 950 billion yen in 1984. This market also felt the effects of the recent slip in production, falling by 26%, to roughly 700, billion yen in 1985.

Still, it may not be down for long,

thanks to the emergence of compound semiconductor materials such as gallium arsenide, gallium phosphide, indium phosphide, and indium antimonide. Compared with current silicon wafers, the quality and price of these materials could keep them from the semiconductor mainstream for some time. Nevertheless, their rate of growth now outstrips that of silicon. Thus far, compound semiconductors have found use in radiant elements such as light-emitting and laser diodes, magnetic devices (hole elements, which are devices used for the motion sensor in such rotating equipment as floppy-disk drives and audio record players), and discrete devices such as high-frequency transistors. The manufacturers supplying this equipment are gradually shifting



Fujitsu is bringing out a waveguide three-channel optical matrix switch.

JAPAN

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toward liquid-encapsulated-Czochralski wafers for GaAs ICs. The traditional silicon wafer manufacturers in this field—such as Japan Silicon, Osaka Titanium, Shin-Etsu Handouta, and Komatsu Electronic Metals—have been joined by such big companies as Furukawa Electric, Mitsubishi Metal Mining, Nippon Metal Industry, Showa Denko, Sumitomo Electric Industries, and Sumitomo Metal Industries, most of which entered the business to lay the groundwork for moves into the electronics field.

On a trial basis, the big manufacturers already have manufactured prescaler ICs—chips having a smaller scale of integration than standard ICs and intended for use in such equipment as TV tuners—and are shipping samples. This is also true of ICs on the 1-K level. As the degree of integration increases, these products could compete with bipolar emitter-coupled logic in both price and speed.

So despite the adverse conditions, the emphasis on development continues in the semiconductor industry and its peripheral industries—motivated not so much by immediate gain but by the industry's potential over the medium and long terms. According to Numura Research Institute, production in Japan's semiconductor and peripheral industries should reach about 5 trillion yen in 1990. Such healthy growth is likely to encourage even further activity.

COMPONENTS

Overseas holds promise for component firms

If the electronic-components industry has a centerpiece, it is large-scale integrated-circuit technology. This is because of the other electronic-component technologies are virtually devoid of color when it comes to significant trends. Now the industry is looking at means to inject more resources into high-value-added products and to diversify product portfolios by forward integration.

For components manufacturers, forward integration means production of hybrids, modules, subsystems, and even end-user systems built around the components they manufacture. And in a effort to increase their market penetration, they are looking at offshore production. Part of this is in response to the Japanese makers of consumer electronics equipment that are already producing offshore and are asking for a nearby source of components.

Two vehicles that the components industry has singled out as potentially lucrative market niches for its components

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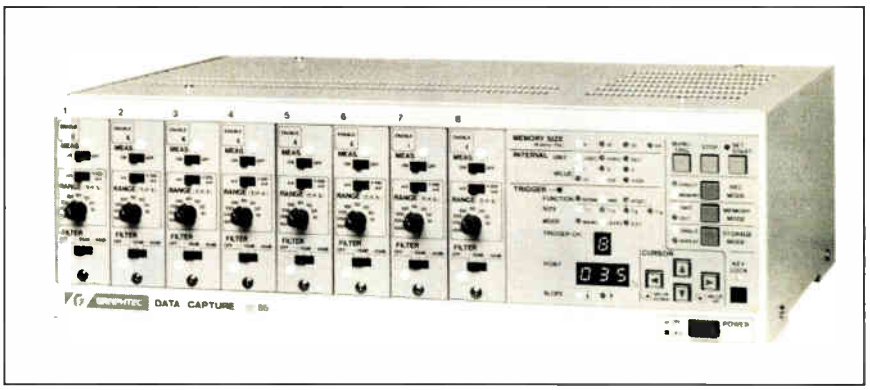


Graphtec makes use of 14-bit data converters in its IF-85 data-acquisition system.

are hybrid ICs and the many types of flat-panel displays.

The hybrid-IC industry had annual sales of approximately 160 billion yen in 1985. It is an industry that has continued to show strong growth, on a par with that of the semiconductor industry when it is considered over the long term. The last few years in particular have seen a stream of companies entering the field.

The hybrid market

Use of hybrid ICs is undergoing a transformation in step with burgeoning demand. Thus far, hybrid ICs generally have been perceived as components for high-density high-reliability packaging. The sector's latest developments expand these characteristics with:

- An increase in product size from squares of a few centimeters to 10 cm and more. The implication is that hybrid ICs will define the nature of electronic equipment.
- Products requiring a customized shape utilizing flexible printed circuits and other new technology. In most cases, these products are for use in mechatronics equipment.
- Products that do not necessarily have a great number of integrated elements per unit of area and are not highly reliable but whose prices are low because they use low-end substrates and other such technology.

The evolution of these hybrid-IC concepts is expected to accelerate in the coming years. Further developments should result in products that integrate:

- Functional components such as charge-coupled devices and other solid-image sensors, liquid-crystal displays and other flat-panel displays, and related peripheral circuits.
- Mechanical components such as switches, connectors, and cables with general-purpose peripheral circuits.
- Software and hardware.
- Optical and electronic components.
- Multivalue-logic ICs, fuzzy-logic ICs, and other post-binary devices with the conventional binary devices.

LCDs and other flat-panel displays are entering a phase of rapid growth and are expected to soon make up a large portion of the market. The foundation of this growth is the steady advances that have been made in all types of flat-panel-display technology.

New markets

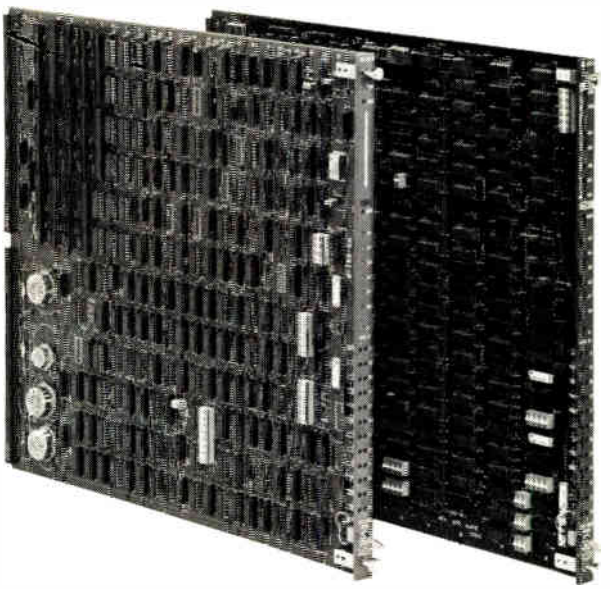
When it comes to generating new markets, the most fertile force in the display field is the LCD, from which has come such practical products as a large-screen display with a 100,000-pixel dot-matrix display, a full-color product for pocket TVs, and a high-contrast high-resolution display using an active matrix.

Electroluminescent displays, perhaps the most pleasing to use of the luminescent displays, are moving from the lab into actual use. Expected to follow thin-film EL in widespread use

FASTBUS

FASTBUS is an IEEE standard, modular, high-speed data acquisition and control system. It has more advanced features than CAMAC and NIM systems which have been widely used. The super high data transfer speed makes the FASTBUS quite suitable for computer graphics as well as high-volume data processing.

We, Maruei-Shoji Co., have been working with the National Laboratory for High Energy Physics, JAPAN (KEK) and have developed over 10 FASTBUS modules. A new master module, MC68020, and FASTBUS kluge card are under development. For more details on the FASTBUS please contact us. (Information on the FASTBUS is also available from U.S. NIM committee.)

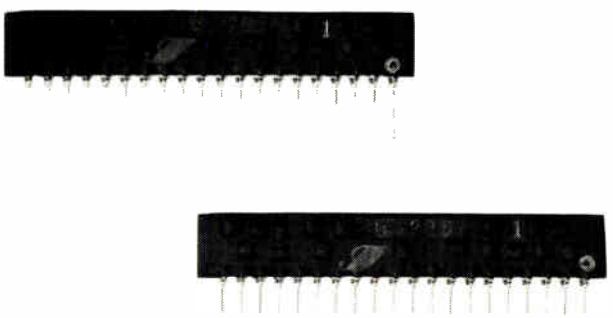


Modules

A NEW FASTBUS CABLE SERGMENT DRIVER HYBRID IC: MS-CSD-TT

Featuring:

- Very long power consumption (360 mW max.)
- Low profile (10 mm high when vertically mounted on a PC board)



Segment Drivers

Specification:

Ta = 20°C to 60°C

Size: 17 mm H (incl. lead length) x 55 mm W x 6 mm L (max.)

On-state current: 4.0 mA ±0.2 mA

On-state current matching: 1% max. over full common mode voltage range

Off-state leakage: 40 μA max. over full common mode voltage range

Common mode voltage range: ±3V min. (Ta = 25°C); ±2.5V min. (Ta = 60°C)

Rise time: 4 ns typ. (10%–90%)

Propagation delay: less than 10 ns

Designed by: T. Taniguchi KEK

Manufactured by: Iwatsu Electric Co., Ltd.

MARUEI SHOJI CO., LTD.

6-7, 1-chome, Nakamachi, Musashino-shi, Tokyo 180, Japan
Tel. 0422-54-6800

Rep.: RAINIER INTERNATIONAL TRADING CO.
Rainier Bank Tower, P.O. Box 3966, T23-4 Seattle, WA98124, U.S.A.
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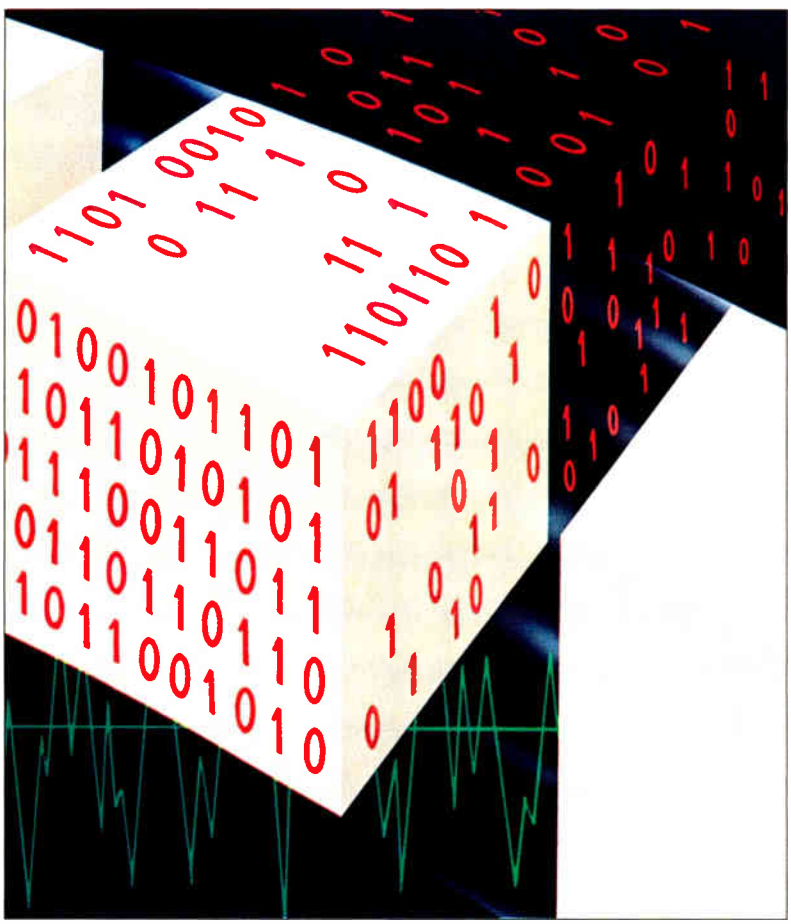
DATA GRABBER.



Zoran's vector digital-signal-processing chip with 70,000 transistors requires only three instructions to do a 1,024-point fast Fourier transform in 2.4 ms.

"A speedy new single-chip contender is getting set to make a splash in digital signal processing. Zoran Corp.'s ZR34161 uses vector-handling techniques to gulp down blocks of data, rather than picking off a single data input at a time as scalar processors do. Vector processing alone is a big speed booster, and Zoran enhances it with embedded signal-processing algorithms that radically pare down system overhead.

The Santa Clara, Calif., company's 16-bit CMOS VSP is the first monolithic signal processor to utilize the powerful vector-handling techniques employed for scientific data processing in large vector computers and minicomputer array processors..."

Excerpted from an exclusive article in the July 24, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

for information displays is dispersed EL, which is attractive to designers because it is very flexible. Sharp, previously the only manufacturer engaged in electroluminescent-display development, now has numerous competitors in the field, including NEC and Matsushita.

Striking advances in plasma display panels are bringing this technology out of its recent slump. These developments have included a reduction in drive voltage through the use of trigger electrodes. In addition, use of thick-film technology has ushered in improved quality and lower prices.

Spearheading growth

The vacuum-fluorescent display continues to stand behind the expansion of the entire market for flat-panel displays and has also begun to evolve in a new direction—super-small products that use an active matrix.

Electronic-equipment manufacturers and even materials manufacturers are starting to see flat-panel displays as a key area, as shown by the burst of new entrants into the field. The electronic-equipment manufacturers want to produce flat-panel displays to preserve the value they add to OEM products; the materials manufacturers see flat-panel displays as a gateway to the electronics industry.

Recent trade conflicts, which have been making headlines, along with the falling value of the yen are causing the export-oriented component companies to look at overseas manufacturing. Japan's electronics manufacturers have production facilities already in place not only in southeast Asia but also in the U. S. and Western Europe. But it should be noted that the products made in the western countries have been either consumer electronics equipment or integrated circuits. Overseas production of components has been limited mainly to southeast Asian countries thus far.

Japan's component industry is changing its policy, however, and starting local production in the developed countries. In addition to the

trade conflicts and falling yen, another force driving the change is the need of overseas equipment makers to be supplied with components.

Parts for VCRs

Production of video cassette recorders in West European countries is an example. After negotiations between European Communities Commission and the Ministry of International Trade and Industry concerning restrictions on exports of VCRs to EC members, Japanese VCR manufacturers chose to establish plants in those countries. Subsequently, establishing a local supply line of Japanese components became critical for these Japanese VCR makers, and so they were eager to see Japanese components manufacturers establish production facilities in Europe.

Traditionally, Japanese components manufacturers have been reluctant to set up overseas production facilities. This is changing: Alps Electric Co. and Matsushita Electronics Components both have started to produce tuners and radio-frequency converters for VCRs. Mitsumi Electric Co. also was licensed by a local manufacturer to provide it with rf converters.

Offshore production of video cassette recorders is regarded as a trigger for overseas production, because the Japanese VCR makers operating in Europe can create a big market for Japanese component manufacturers. That demand is spilling over into other areas, enticing Japanese manufacturers of the components not used in VCRs—such as connectors—to move production overseas to serve European as well as Japanese companies.

The typical lineup of components (excluding integrated circuits) that are produced in the developed countries currently include:

- Capacitors
- Resistors
- Transformers
- Coils
- Tuners
- Rf converters
- Magnetic media (VCR tapes, audio tapes, and floppy disks)
- Connectors
- Keyboards
- Cathode-ray tubes
- Photomultiplexer tubes
- Audio speakers
- Microphones
- Photosensitive drums for photocopiers
- Ceramic packages for ICs
- Leadframes for ICs

Greater involvement

Japanese components manufacturers are looking to do even more production overseas, especially in the developed countries. In doing so, they hope to expand their market beyond Japanese equipment manufacturers to include U. S. and European equipment manufacturers as well.

The companies will be producing components for industrial electronics equipment in addition to components for electronics equipment. The impetus behind their broader focus: the expected shift of emphasis on the part of Japanese electronics equipment manufacturers from consumer electronics to industrial electronics in the coming years. ■

Focus on Graphtec Corp.

Mitsuo Yamaguchi, president

Since its founding in 1949, Graphtec Corp. has captured a large share of the markets for measuring instruments, pen-writing recorders, and such computer peripherals as plotters and digitizers—not only in Japan but throughout the world. It bases its success on such products as the WR3101 and WR3500 multichannel thermal-pen oscillographic chart recorders; the MP1000 and MP2000, intelligent digital plotters with an attractive price/performance ratio; and the KD4030A, a compact, low-priced digitizer for computer-aided design systems. The G-CAD6 and G-CAD7 are among the company's personal CAD systems.

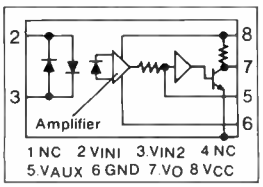
Graphtec put its experience in analog and digital technology to work in the development of hybrid products that combine analog and digital functions. These hybrids are essential now that digital technology has revolutionized the measuring-instruments market and measurement applications have become more complicated. Among its offerings are the MH9010 hybrid recorder; the IF-85 data-collection unit; the MS8603 Rastercorder, which uses a thermal recording method; and measurement software.

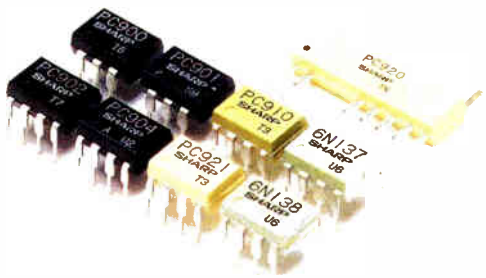
In addition, it is bringing out products to meet the increasing demand for peripheral equipment such as low-cost high-speed plotters and high-resolution digitizers.

In its role as an international manufacturer of measuring instruments and graphics and information processing devices, Graphtec will continue to develop products that meet user requirements.

For application-specific, specify Sharp OPIC.

Sharp's unique opto-electronics technology and IC technology have been integrated to create the OPIC photocoupler with its own built-in circuitry.
Sharp developed this application-specific OPIC to better respond to rapidly diversifying needs.
The applications are ample and diverse, including high-speed digital transmission, programmable controllers, inverter air conditioners, switching power supplies, etc.
This leading-edge technology gives you enhanced performance, reduced product cost and compact/light-weight design.
Now you have an ally to help you to beat the competition.





Choose your photocoupler as wisely as you choose your club.

●OPIC photocouplers/general purpose photocouplers

Series	Model	Features	Applications
PC900 series	PC900	Digital switching, Normal-off operation	Computers, Programmable controllers, Measuring equipment, Numerical control machines
	PC901	Digital switching, Normal-on operation	Computers, Programmable controllers, Measuring equipment, Numerical control machines
	PC902	AC input, Built-in integration circuit	Programmable controllers, Telephones, Copiers
	PC904	Built-in voltage deviation detection circuit	Switching power supplies
	PC910	Ultra high speed(10Mb/s)	Computers, Programmable controllers, Copiers
	PC920	For inverter control, Single-in-line package	Inverter air conditioners
	PC921	For inverter control, Dual-in-line package	Inverter air conditioners
6N series	6N135	High speed(1Mb/s)	Computers, Telephones, Measuring equipment, Numerical control machines
	6N136	High speed(1Mb/s)	Computers, Telephones, Measuring equipment, Numerical control machines
	6N137	Ultra high speed(10Mb/s)	Computers, Telephones
	6N138	Low input current, High sensitivity(CTR:300 % min.)	Computers, Telephones
	6N139	High sensitivity (CTR:500 % min.)	Computers, Telephones, Measuring equipment, Numerical control machines

OPIC PHOTOCOUPLERS

▶OPIC is a registered trademark of Sharp and stands for Optical IC.

SHARP

SHARP CORPORATION, JAPAN

SHARP CORPORATION Electronic Components Group International Sales Dept
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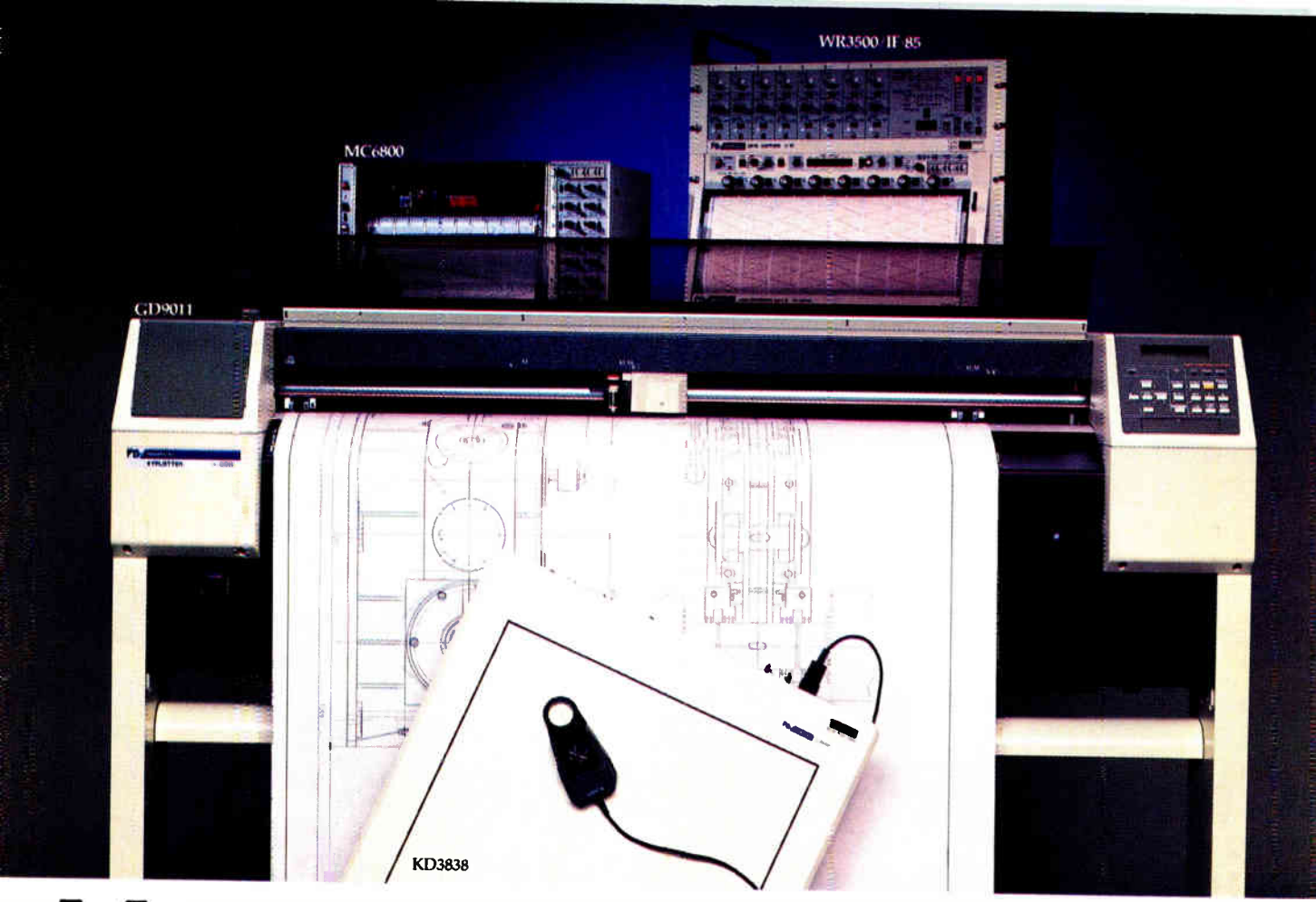
Circle 147 on reader service card



Meet the Graphtec Professionals

Not so long ago, if you bought professional-level graphics and recording equipment you had to make a major financial investment. Then spend hours wondering how to set it up. Then go home worrying about breakdowns.

No longer.

Graphtec are pleased to announce the availability of the Professionals. A range of affordable, easy to use, reliable graphics devices and recorders that put real meaning back into the word "Quality".

Below we've mentioned the highlights of just a few of the extensive Graphtec range. Contact your nearest dealer today, there will be a model to suit your application.

MS8603

MS8603 Rastercorder: Graphics and character capable plotter/printer, 8 dots/mm resolution fixed thermal head.

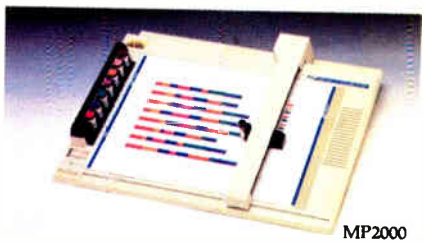
KD3838 Digitizer: ±0.5mm point reading accuracy, high-sensitivity electromagnetic detection, 4-button cursor, and robust, lightweight construction.

MH9010

MH9010 Hybrid Recorder: 18-channel recorder, 6-color recording and printout, RAM storage.

WR3500/IF-85 Data Capture Recorder: Eight channels, 64kword memory capacity, 18-step sampling rate from 10us to 5s, and choice of GPIB or RS-232C interface.

MC6800 Multicorder: Up to eight channels, ASCII annotation, zero between-channel time delay, and 1600mm/s pen speed.



MP2000

MP2000 X-Y Plotter: Eight self-capping pens, three built-in command sets, and choice of GPIB interface or dual port Centronics/RS-232C interfaces.

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Circle 148 on reader service card

NEW PRODUCTS

HIGH-RESOLUTION BOARD BOWS FOR VMEBUS SYSTEMS

IMAGRAPH'S CARD SETS UP A WINDOW OF 1,280 BY 1-K BY 4 BITS

Imagraph Corp. has developed a high-resolution VMEbus graphics board for work stations by extending the capabilities of an industry-standard controller chip beyond its typical range. Called the VME-1280-4, the color graphics board provides a display window of 1,280 by 1-K by 4 bits per pixel, with an addressable window area of 2-K by 1-K by 4 bits.

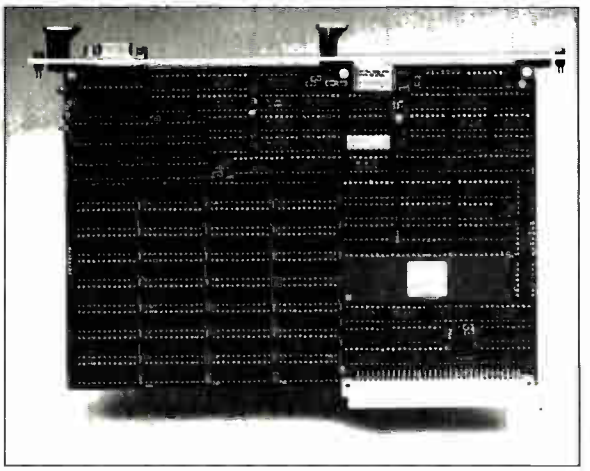
The dual-port memory-mapped card allows the simultaneous display of 16 colors or gray shades from a programmable palette of 4,096. Flicker-free display is possible on most CRTs because the board's video refresh rate is 60 Hz noninterlaced. The double-width Eurocard measures 233 by 160 mm and fits in a single VMEbus slot. It has 1 megabyte of on-board display memory and a 106-MHz pixel clock, required to achieve the high resolution.

PRIMITIVES APLENTY. The heart of the VME-1280-4 is Hitachi Ltd.'s HD-63484 advanced CRT controller. Imagraph selected the chip because it has the fullest set of graphics primitives, explains president Robert Wang. It also has an intelligent processor that can accept graphic commands directly from the VMEbus processor through memory-mapped I/O registers and boasts a drawing speed of 1.3 million pixels/s. The Hitachi controller will support up to 8-MHz clock speed.

To get the performance it wanted, however, Imagraph had to overcome some limitations inherent in the Hitachi chip. A major obstacle in designing the VME-1280-4, says Wang, was the instability of the Hitachi chip's video synchronization generation circuits. "We just bypass that by creating our own stable video-tuning signal."

Users of the new board will experience no waiting time for horizontal or vertical retrace when drawing pixels. And Imagraph says no pixel-update flash or flicker will show up, even when a 1,280-by-1,024-pixel screen is refreshed at 60 Hz using the 106-MHz pixel clock rate.

The VME-1280-4 memory supports independent access by the Hitachi chip or the host processor. Display memory can be mapped in 8 pages of 128-K bytes or as 1 megabyte of continuous memory in the 16-megabyte address range.



MEMORY RICH. Imagraph's double-wide VMEbus color graphics controller holds 1 megabyte of memory on board.

Data transfer to and from the board is done with 16-bit words—equivalent to four horizontal pixels four bits deep—at 600 ns per word or 6 million pixels per second. The VME-1280-4 also supports external direct memory access to and from its display memory. Burst-mode DMA can run at a 1.6 million words/s rate.

Imagraph had to design its own video RAM control circuits because the new board uses dual-port 256-K video RAMs. The year-old company decided to use video RAMs from NEC Corp. rather than conventional dynamic RAMs for the board for higher speed, according to Wang.

The color graphics controller has three 16-by-4-bit wide high-speed RAMs for its lookup tables. Each RAM drives one gun of the color CRT.

Designed for applications such as computer-aided design and engineering and graphic-arts work stations, the VME-1280-4 is base priced at $3,495, with discounts available to original-equipment manufacturers. It is also available in a lower-resolution 1-K-by-768-by-4-bit model for $2,495. Both graphics controllers are available in 30 days. *–Craig D. Rose*

Imagraph Corp., 400 W. Cummings Park, Woburn, Mass. 01801 Phone (617) 938-5480 [Circle reader service number 341]

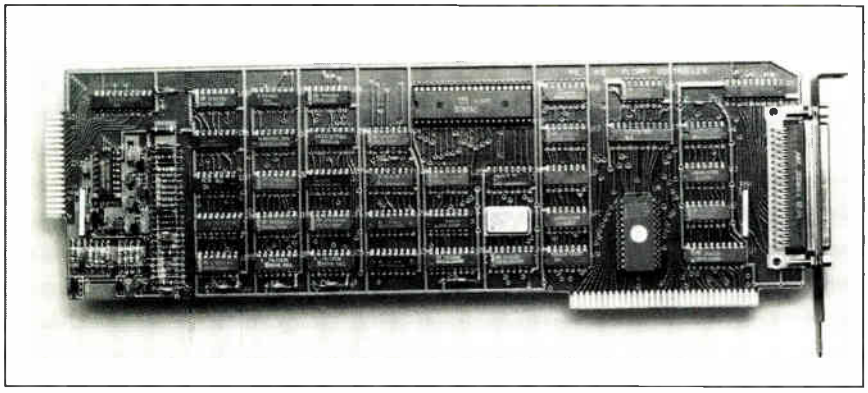
CONTROLLER QUADRUPLES PC STORAGE CAPACITY

A floppy-disk-drive controller board for IBM Corp. Personal Computers, PC/XTs, and PC ATs supports both 360-K-byte and 1.2-megabyte floppy-disk drives at the same time. Because PCs and PC/XTs have 360-K-byte drives, a user can nearly quadruple the storage capacity of the basic PC by using the board to add one higher-capacity drive. Capacity increases even more when more than one drive is added.

Computer Peripherals Inc.'s Drivemaster can also streamline operations in offices where standard PCs and PC/XTs work alongside PC ATs, which use 1.2-megabyte drives. Adding the boards and 1.2-megabyte drives to the PCs and PC/XTs makes it possible to pass data or programs stored on AT disks to those machines without first converting to the 360-K-byte disk format.

The board controls any combination of up to four internal or external 5¼- or 3½-in. floppy-disk drives. It can support 48-, 96-, and 160-track/in. formats; its built-in buffer stores data temporarily when media of different storage capacities are used at the same time.

Most PC application programs can take advantage of the extra storage of



MIXING. With Drivemaster, 360-K-byte and 1.2-megabyte drives can be mixed in systems.

1.2-megabyte disks provided by Drivemaster, as long as they use standard MS-DOS (or PC-DOS) calls to access the disk. All operating-system commands and calls will operate as described in the MS-DOS documentation. This means the user does not have to learn any new commands or any modifications to commands.

Furthermore, the user need not configure and install any software drivers or modify the system's operation in any way. ROM-based firmware on the board supports all commands.

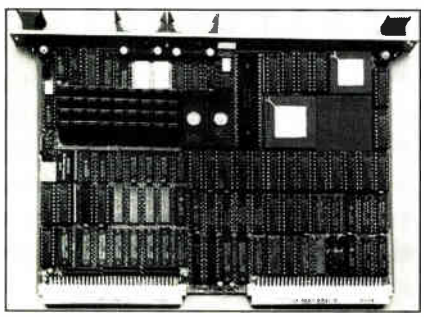
The Drivemaster uses multilayer printed-circuit-board construction, which makes possible wider signal traces, greater heat dissipation, and a ground plane that reduces noise. The board is compatible with the Compaq Computer Corp. header connector, which is different from that of other IBM-compatible computers. It is also compatible with Irwin Magnetic Systems Inc. tape-backup drives.

The Drivemaster is priced at $249 and is available now. *-Ellie Aguilar*

Computer Peripherals Inc., 2635 Lavery Court, Newbury Park, Calif. 91320.
Phone (805) 499-5751 [Circle 340]

VMEBUS COMPUTER USES 25-MHz 68020

The HK68/V2F single-board VMEbus computer brings the power of the 32-bit 68020 microprocessor to real-time applications in robotics and high-speed communications control. The board includes a 25-MHz 68020 chip and has up to 4 megabytes of dual-access RAM with parity, up to 128-K bytes of EPROM, 128-K bytes of static RAM for user functions, and a single RS-232-C serial port.



Available as options are an RS-422 port, a 68881 floating-point coprocessor, and a time-of-day clock with battery backup. Software support for real-time applications is provided by Hunter & Ready's VRTX real-time executive and Microware's OS-9 operating system. Unix-to-VRTX development systems are also available for developing and testing applications. In lots of 100 pieces, the HK68/V2F is priced at $1,195 each.

Heurikon Corp., 3201 Latham Dr., Madison, Wis. 53713.
Phone (608) 271-8700 [Circle 345]

LATEST iRMX 86 SUPPORTS MULTIBUS II

Release 7.0 of the iRMX 86 real-time multitasking operating system is available now for a $6,000 license fee. The operating system, which is used in industrial control, real-time data acquisition, and process control, has a number of new features.

With Release 7.0, it now supports the Multibus II architecture. Interactive configuration utility screens are available for incorporating device drivers for new Multibus I peripheral-controller boards. Terminal-support code enables a block-mode terminal to transmit an entire block of data with a single keystroke. In addition, system-callable external-declaration files give users easy access to iRMX 86 services directly from Pascal or Fortran programs.

Intel Corp., Literature Dept. #W313, 3065 Bowers Ave., P. O. Box 58065, Santa Clara, Calif. 95052. [Circle 349]

PACKAGE FINDS BUGS IN C PROGRAMS

A diagnostic facility for the C programming language, PC-Lint runs under MS-DOS and analyzes C programs, providing reports on bugs, glitches, and inconsistencies. PC-Lint looks across multiple modules and gets a perspective that compilers do not.

Among the errors that PC-Lint finds are type inconsistencies across modules, parameter-argument mismatches, library-usage irregularities, and variables declared but not used.

PC-Lint includes support for such American National Standards Institute C-language extensions as enum, structure assignment, prototypes, and void, and such Microsoft Corp. keywords as far, near, and pascal. PC-Lint is delivered with user-modifiable standard library descriptions for most major compilers.

PC-Lint, which requires 128-K bytes of memory, sells for $139. It is available now.

Gimpel Software, 3207 Hogarth Lane, Collegeville, Pa. 19426.
Phone (215) 584-4261 [Circle 346]

ADAPTOR LETS PCs WORK ON VMEBUSES

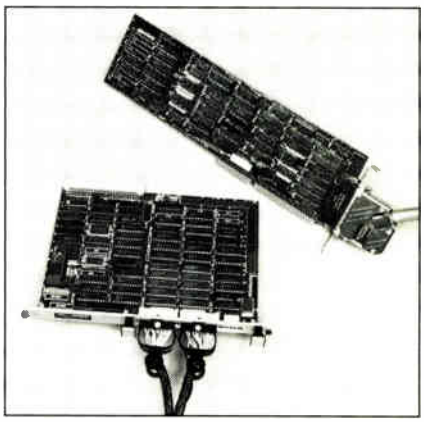
A two-card adaptor enables IBM Corp.'s Personal Computer AT to become a VMEbus processor. As such the 403 PC AT VME adaptor can be used as a bus slave, a bus master, or one of several bus masters in a multiprocessor system to control I/O devices.

Address mapping permits the PC AT to directly address VMEbus memory as if it were PC AT memory. Communication between the AT and the VMEbus is accomplished through AT RAM read and write operations; there is no need to pass the data through intermediate software drivers.

An optional dual-port RAM piggyback module provides additional memory that both the PC AT and the VME system can share. It can conserve VMEbus bandwidth, because the PC AT does not use the VMEbus when it reads from and writes to the dual-port RAM.

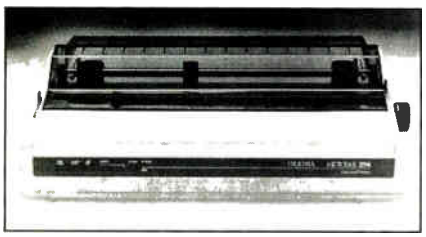
The 403 adaptor is priced at $1,280 and is available two weeks after ordering.

Bit 3 Computer Corp., 8120 Penn Ave. S., Minneapolis, Minn. 55431.
Phone (612) 881-6955 [Circle 347]



PRINTER PERFORMS AT 400 CHARACTERS/S

With its 400-character/s print speed, the Microline 294 is targeted mainly at data-processing and draft-copy applications. But the printer also has a near-letter-quality mode that prints at 100 characters/s in two passes.



The high speed is possible because the unit uses a dual 9-pin printhead rather than a single 24-pin head. The printhead moves two 9-pin columns across the page, each printing alternate, adjacent columns within a character. With this setup, the Microline 294 can print bit-image graphics at up to 288-dot/in. resolution.

The printer accepts single sheets or continuous-roll paper up to 16 in. wide. Optional color ribbons provide yellow, cyan, magenta, and black, which can be mixed to create as many as 14 colors.

Available now, the 294 is priced at $1,499.

Okidata Corp., 532 Fellowship Rd., Mt. Laurel, N. J. 08054.
Phone (609) 235-2600 [Circle 348]

SYMBOLICS' SYSTEMS TOP OLDER MODELS

Two new symbolic processing systems, the 3620 and 3650, are one-fourth the size but offer 20% to 40% higher performance and greater expansion potential than the company's present entry-level and midrange development systems. The new computers are intended primarily for software development, but can also be used for delivering end-user applications.

The minimum configuration of the 3620 contains a 36-bit proprietary processor with 4 megabytes of memory, I/O controllers, a 190-megabyte disk drive, Ethernet interface, expansion slots for three additional memory boards, and monochrome display. The basic 3650 is similarly configured but has a 368-megabyte disk drive.

The 3620 sells for $49,900 and the 3650 for $65,900. Both are available now.

Symbolics Inc., 555 Virginia Rd., Concord, Mass. 01742.
Phone (617) 259-3600 [Circle 350]

ESDI DISK CONTROLLER SERVES MICROVAX II

An enhanced small-device-interface disk controller for Q-bus and MicroVAX II computers has a maximum data-transfer rate of 2.45 megabytes/s. This allows it to be used with existing disk drives that operate at 5- or 10-megabit/s transfer rates.

The ESDI disk controller supports a maximum of four logical drives. Disk-drive sizes can be from 67 megabytes to over 4 gigabytes formatted, and with different data-transfer rates. The controller also includes a direct-memory-access autothrottle and multilevel interrupts among its features.

The single-quantity price of the Q-bus model is $1,671, and the MicroVAX II model is $1,707, which includes a driver for MicroVMS. Both are being shipped this month.

MDB Systems Inc., 1995 N. Batavia St., Orange, Calif. 92665.
Phone (714) 998-6900 [Circle 351]

SOFTWARE AIDS IN STD BUS WORK

STD Multi-DOS combines PC-DOS with a multitasking executive to create an STD-8088-based operating system. The multitasking operating system's kernel, VRTX (Virtual Real-Time Executive), runs in real time independently from the PC-DOS utilities, with an interrupt response time of just 100 ms. The user determines the priority of task execution.

The development configuration consists of an IBM Corp. PC-compatible personal computer connected through a serial link to the STD bus system. The Multi-DOS development package includes PC-DOS, Multi-DOS BIOS, VRTX, and Tracer, a real-time debugger. Hardware consists of the ZT 8806 or 8807 single-board computer, the 256-K-byte ZT 8824 Megaram board, card cage and power supply, cables, and documentation. The base price for hardware and software is $6,000.

Ziatech Corp., 3433 Roberto Court, San Luis Obispo, Calif. 93401.
Phone (805) 541-0488 [Circle 352]

8-MHz 80186 DRIVES STD BUS COMPUTER

The Thunder Plus 80186 single-board S100 bus computer includes an 8-MHz 80186 microprocessor, 1 megabyte of zero-wait-state RAM, and a floppy-disk controller that can run either 8-, 5¼-, or 3½-in. drives. In addition, the card has two RS-232-C serial ports, a parallel port, and room for an 80287 math coprocessor.

The card, which is suited for applications requiring high-speed data handling, comes with the Concurrent DOS operating system. Concurrent DOS allows concurrent execution of MS-DOS and CP/M-86 applications.

Priced at $1,195, the Thunder Plus is available now.

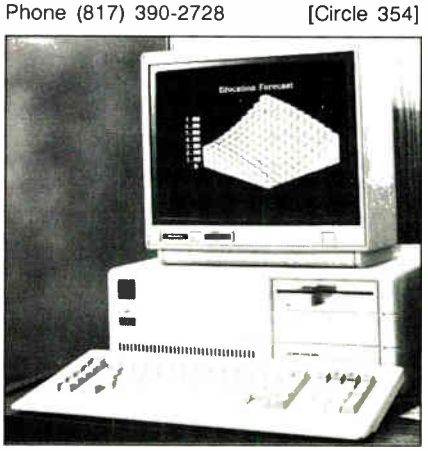
Lomas Data Products Inc., 182 Cedar Hill St., Marlboro, Mass. 01752.
Phone (617) 460-0333 [Circle 353]

PC/XT COMPATIBLE GOES FOR $1,699

An IBM Corp. Personal Computer/XT-compatible with two floppy disk drives instead of a floppy and a hard disk drive is priced at just $1,699. The 3000 HL system, which can be fitted with a hard-disk drive, is built around an 80286 microprocessor that runs at switch-selectable speeds of 4 and 8 MHz.

The standard configuration comes with 512-K bytes of RAM, expandable to 640-K bytes. It also has a parallel port, a real-time clock with battery backup, and a socket for the 80287 math coprocessor. The system has seven expansion slots for adding peripherals. It is available now.

Tandy Corp./Radio Shack, 1800 One Tandy Center, Fort Worth, Texas 76102.
Phone (817) 390-2728 [Circle 354]



ROBOT AIMS AT NICHE BETWEEN INDUSTRY, HOME

$8,000 SIX-AXIS ARM HAS 8-LB PAYLOAD, 27-IN. REACH, AND 1.1-METER/S VELOCITY; FITS IN 30-FT³ OPERATING ENVELOPE

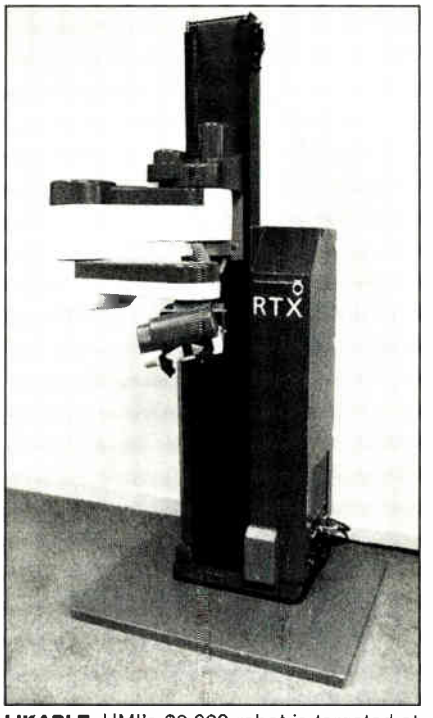
Despite an already crowded market in robotics, a startup known as Universal Machine Intelligence Inc. says its RTX robot arm has something unique to offer. For an $8,000 base price, the six-axis RTX splits the ground between today's high-priced industrial robots and low-end personal or teaching arms, says Geoffrey C. Henny, the company's cofounder and chief executive officer.

"What we're offering is basically a high-performance machine at a very low cost, and it's extremely easy to use," Henny says. "It's an arm that upgrades to a mobile [robot], which can be run by somebody who need not have even a high school education. But it can also be used for things like artificial intelligence research."

The four-foot-high RTX features a SCARA architecture (for selective compliance automated robot arm) that is particularly suitable for applications in education, health care, light industry, laboratories, and research, where human interaction is important, Henny notes. The arm's 30-ft³ operating envelope allows the RTX to work from floor level to typical tabletop height, while a programmable force-control feature, among other things, will contribute to safety by automatically limiting driving forces on the arm.

TRADEOFFS. With a maximum 8-lb payload capacity, a 27-in. reach, a top velocity of 1.1 meters/s, and repeatability to ±0.018 in., the RTX is not as powerful, fast, or accurate as most conventional industrial arms. The AdeptOne, a light-industrial-class SCARA arm from Adept Technology Inc., Sunnyvale, Calif., for example, can handle a 20-lb payload and features a 31.5-in. reach and 9 meters/s maximum speed, with repeatability specified at ±0.002 in. But the AdeptOne sells for about $46,000, and other industrial robots range in price up to $100,000 or more. By contrast, the $8,000 RTX—when equipped with an optional plug-in controller card for stand-alone operation—will go for $12,000.

The RTX's price is higher than that of home and basic teaching robots, which sell in the $4,000 to $5,000 range with a built-in controller. But those arms generally fall short of the RTX performance, Henny says. The XR-3, a popular teaching robot from Rhino Robots Inc., Champaign, Ill., for example, sells for about $5,000. But the maximum XR-3 payload is specified at only 1 lb.



LIKABLE. UMI's $8,000 robot is targeted at tasks that require human interaction.

Universal Machine Intelligence is aiming at "a new niche between industrial and home robots," says Lynn Conway, an associate dean of engineering and professor of electrical and computer science at the University of Michigan, Ann Arbor, who serves on the company's board of directors. The University of Michigan, in fact, has ordered 10 of the RTX arms for use in its robotics instructional laboratory program, Conway says. "There's a real need for this sort of medium-scale, medium-priced robot in the higher-education arena," she notes.

Henny expects initial sales will be to universities and other educational and training institutions, with a long-term eye on a potentially much larger business in health care applications. Henny also sees potential for the RTX in electronics assembly. The RTX is not fast or accurate enough for component insertion, but RTX arms could work as servers to board-stuffing robots, he says.

The RTX comes equipped with a serial RS-232-C port and software designed to run on the IBM Corp. Personal Computer family and compatibles. Written in Forth, the software is designed to let the inexperienced user begin operating the robot quickly using a library of simple English commands, Henny says. Users can also write their own programs in any high-level language, including Lisp, Prolog, and C, he adds.

CONTROL CHOICES. A pair of 8031 microprocessors in the RTX control the arm under program control from a PC host. But for an additional $4,000, UMI offers a control board, the RTX-MSP, which plugs into the RTX backplane. Equipped with an 8088 processor and 8087 math coprocessor, the RTX-MSP board enables the RTX to operate in a stand-alone mode once a program has been loaded from a PC host or a dumb terminal. The RTX-MSP includes 14 I/O ports for connecting peripherals such as a vision or speech-recognition system, and up to four RTX arms can be controlled using a single RTX-MSP card.

The RTX and associated RTX-MSP card are available now, and the firm plans soon to offer more options through third-party agreements that are now being negotiated. These include a machine-vision system, a speech-recognition system, tactile sensing systems, and a variety of interchangeable grippers. By next April, the company also plans to offer a mobile robot with either one or two RTX arms.

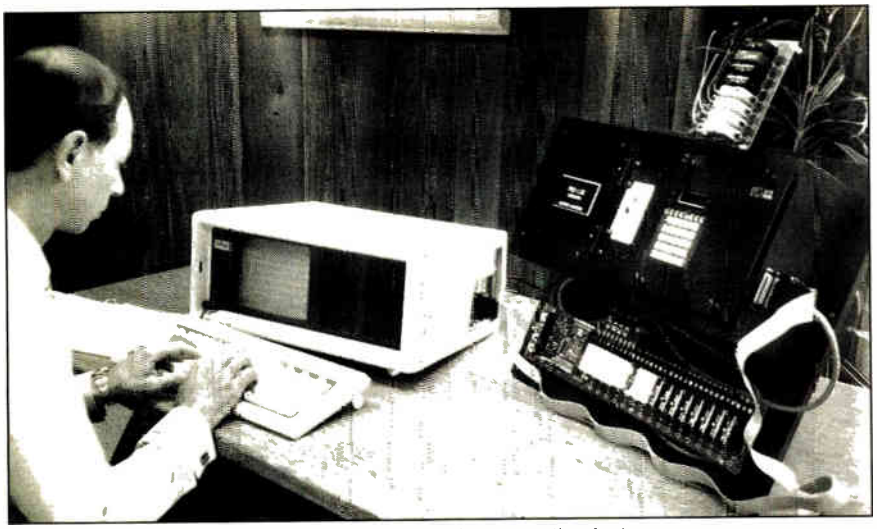
–Wesley R. Iversen

Universal Machine Intelligence Inc., 3135 State St., Suite 209, Ann Arbor, Mich. 48104. Phone (313) 995-5115 [Circle 460]

CARDS ENABLE IBM PC TO PROGRAM IN LADDER LOGIC

Engineers in factory automation can program control modules in ladder logic on an IBM Corp. Personal Computer with an STD-bus card set and accompanying software from Pro-Log Corp. Ladder logic—gate-level logic used to program relay controls—is so named because its electrical representation resembles the side rails and rungs of a ladder, with each rung signifying a sequence of instructions.

Pro-Log has put what amounts to a diskless PC on two STD cards, and packaged it with software developed by one of its oldest customers, Control Process Corp. of Davenport, Iowa. The software includes a programmable controller and accompanying development system.



FACTORY HELP. Pro-Log's cards aid engineers in automating factory processes.

One of the Pro-Log TLC 1.0 cards contains an 8088 microprocessor (plus a socket for an 8087 math coprocessor) and an executive programmable read-only memory that interprets symbolic ladder-logic commands. The second card has 64-K bytes of battery-backed CMOS RAM, 32-K bytes of which can be used for applications programs.

With the cards comes a disk containing the Control Process RD 1000 logic editor. Users unfamiliar with high-level languages can program in the logic they have traditionally used for process control, and download the sequences to the STD cards.

The TLC processor exercises controls locally or remotely (up to a mile) over an RS-232-C or RS-422 link. An optical multiplexer interface can address up to 992 I/O points over a single link. Inputs to the processor can come from other STD boards, such as analog-to-digital and digital-to-analog converters, drivers, or relays. A proprietary programmable-array logic chip on the TLC CPU card performs bus arbitration logic for up to 16 other CPUs on the bus.

The CPU card can multiplex commands to 512 devices over 32 16-module boards. In drum mode, for use with specific sequences tied together, the system operates like an electronic cam, programmed by 16 rows of 16 switches.

Pro-Log developed the controller cards for the in-house engineers responsible for automating factory processes, for original-equipment manufacturers who build factory-control equipment, and for systems integrators such as Control Process, a specialist in food processing.

End users will be able to program and reprogram factory systems using the editing software. The target system will accept up to 16 programs, which can call one another and jump to each other's subroutines.

The RD 1000 will also monitor actual operation sequences so that programs can be debugged. As each control operates, the monitor highlights the corresponding ladder-logic symbol on the screen.

The price of the TLC 1.0 is $995 in quantities of 25 to 49. The RD 1000 software is priced at $1,750. Delivery takes two to four weeks.

Pro-Log Corp., 2411 Garden Rd., Monterey, Calif. 93940.
Phone (408) 372-4593 [Circle 461]

ULTRASONIC UNIT WORKS 1 MILE AWAY

The Sonologic Multi-Point ultrasonic system can monitor the level of liquid or solid material in up to 16 vessels from as far away as a mile. A complete system includes a model 5510 level indicator, 1 to 16 intelligent transceiver units, and the company's Sonocell sensors (one ITU and one Sonocell for each vessel).

Time values derived from pulsed signals from the Sonocell and reflected off the material determine the level in each bin. Advanced electronics in each ITU measure this time and analyze all echoes, filter out extraneous noise, and convert the time values to material-level information.

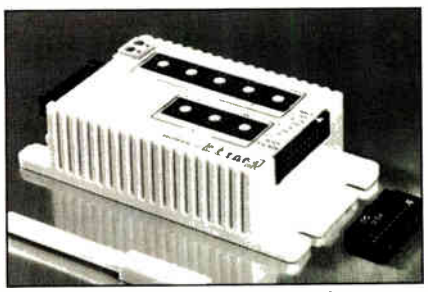
That data is then transmitted over an RS-422 interface to the 5510 level indicator. It is displayed on a digital readout, which automatically sequences from one bin to the next. A single-vessel system is priced at $3,500; discounts are available for multi-vessel systems.

Kistler-Morse, 10201 Willows Rd. N. E., P. O. Box 3009, Redmond, Wash. 98073.
Phone (206) 881-8000 [Circle 465]

MODULE CONTROLS STEPPER DRIVER

The RC-201, a compact control module, governs the company's RD-1 stepper motor's movements by monitoring and counting the pulses put out by the motor. The RC-201 process controller will count up to 15,000 pulses/s, sufficient for most industrial applications.

The device allows input signals from three limit switches or photosensors. Its low step setting will accommodate up to 9,990 pulses. For high step counts, its binary-coded decimal rotary switches



can be set for up to 99,999 pulses.

Designed for input from limit switches or photosensors, the RC-201 can determine the upper and lower limits to the motor's trajectory as well as home position. A simple signal changes direction from clockwise to counterclockwise and initiates manual starting, emergency stopping, and repeating.

Priced at $270, the RC-201 is available now.

Semix Inc., 4160 Technology Dr., Fremont, Calif. 94538.
Phone (415) 659-8800 [Circle 466]

SOFTWARE SERVES PROCESS CONTROL

The Loopworks software series provides a variety of process-monitoring and control functions, including real-time trend displays, sequence control, and signal processing. It works with equipment from such industrial equipment vendors as Action Instruments, Analog Devices, Burr-Brown, Data Translation, Intel, Metrabyte, and Opto 22.

The digital signal-processing functions

This is Motorola's new super-microcomputer.

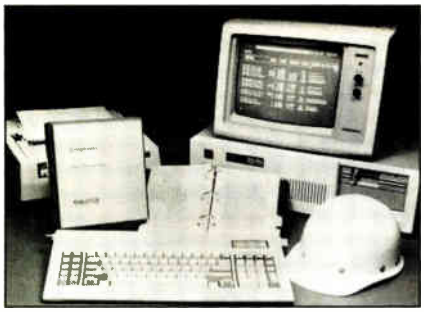
System 8000 is a midrange computer built around Motorola's own MC 68020 32-bit microprocessor, and is ideal for departmental computing. For information call 800-262-4488 ext. 730. In California call 800-252-4488 ext. 730.

It's expandable. It's upgradeable. It's fast. And its future is just like its remarkable architecture. Wide open.

MOTOROLA

Advanced Electronics for
a More Productive World.

Circle 155 on reader service card



provide transition alarms, signal inversion, override capability, and selectable labels. The analog signal processing provides limit alarms, scaling, ranging, filtering, and selectable linearization for thermocouples and other sensors.

Sequencing and ramp/soak packages perform up to five steps per sequence, chainable sequences; they have manual or automatic start, stop, and resume capabilities. Another package for real-time trend displays lets users set up to 10 displays, with three pens per display, continuous scrolling and averaging, and a selectable time base of 12 minutes to 24 hours.

Packages are priced starting at $995 and are available now.

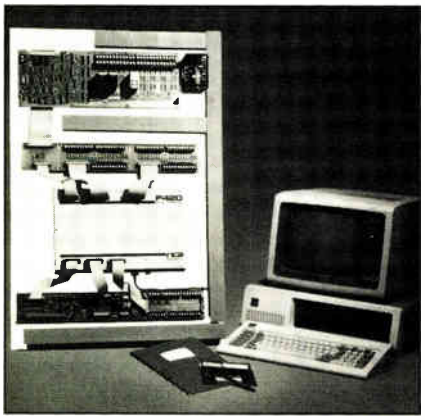
Equinox Data Corp., 150 Nickerson St., Seattle, Wash. 98109.
Phone (206) 281-7327 [Circle 467]

UTILITY LINKS PC AND CONTROLLER

Machine designers and programmers can now use the full capability of the IBM Corp. Personal Computer to prepare and edit motion programs and to troubleshoot any North Coast Automation P420 motion controller, thanks to the PC/P420 communications link package.

The utilities permit the P420 programmable motion controller to communicate directly with the PC. The package includes software to communicate over an RS-232-C or RS-422 interface. Hardware is available for converting the PC serial port from one interface to the other.

Software support includes utility programs on floppy disks to download and upload motion-control programs, start and stop programs, display axis positions, check I/O status, check program status, and perform various additional functions.

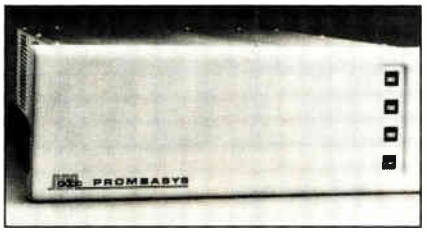


Priced at $50, the communications link is available immediately.

North Coast Automation Inc., 71 Alpha Park, Cleveland, Ohio, 44143.
Phone (216) 473-3800 [Circle 468]

RAM DISK WORKS IN HARSH ENVIRONMENTS

Data-acquisition systems that must work in harsh locations can be equipped with a high-capacity data-storage system that holds up to four megabytes. The Prombasys system works in less than ideal conditions because it uses PROMs and RAMs set up like disk drives.



The storage system also can be set up for multitasking data acquisition and control with no reduction in performance or capability.

The company's proprietary programming language, I/OBasic, plus Digital Equipment Corp.'s RS-11 operating system and the applications software, are all resident in PROM. The system supports full utility handling and comes equipped with a real-time clock and dual serial ports. Prombasys can accommodate more than 1,000 analog inputs, 2,000 discrete I/O points, 128 analog outputs, and up to eight serial lines.

Priced at $7,000 for a 19-in. rackmount version equipped with 128-K bytes of RAM and 256-K bytes of PROM, the system is available now.

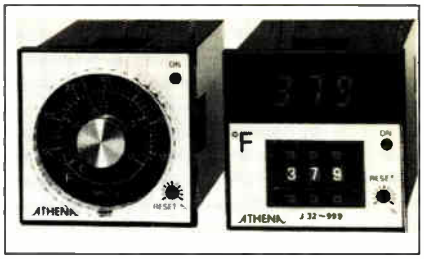
Adac Corp., 70 Tower Office Park, Woburn, Mass. 01801.
Phone (617) 935-6668 [Circle 469]

COMPACT SYSTEM CHECKS TEMPERATURE

The Series 1600 temperature controllers come in the 1/16 DIN size, the industry's smallest size standard at 1.890 by 1.890 in. Series 1600 consists of analog and digital models that supply proportional or on-off control of heating and cooling processes.

They accept either J or K thermocouple, or platinum resistance temperature detector inputs, and can be supplied with either relay or voltage outputs.

The 1620 analog models have front-panel, full-scale dial for set point, offset



adjustment, and power-on indication. The digital units, the 1640 models, feature front-panel digital switches for temperature setting, digital LED display of process temperature, and offset adjustment. The 1620 analog unit sells for $95 and the 1640 digital version is $195. Both are available now.

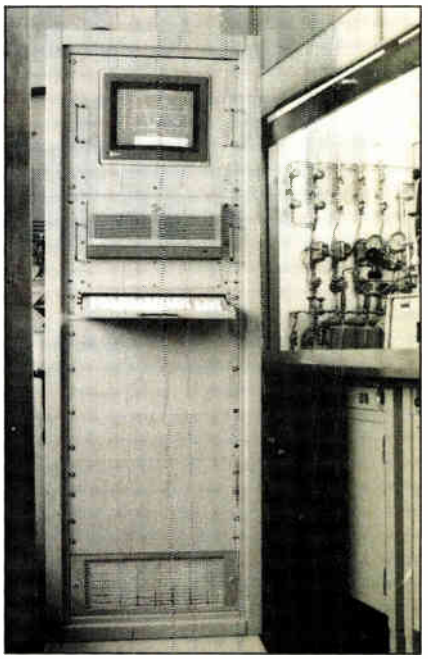
Athena Controls Inc., 5145 Campus Dr., Plymouth Meeting, Pa. 19462.
Phone (215) 828-2490 [Circle 470]

AT&T UNVEILS FACTORY COMPUTERS

AT&T is moving into the industrial market with a line of computer and networking products. The AT&T Industrial Workstations are modifications of the AT&T PC 6300 and the PC 6300 Plus, the company's personal computers, which run both MS-DOS and Unix. The modifications include special fans, filters, and housings to protect them from dust, dirt, and other conditions found in industrial settings.

The basic configurations include an 80186-based CPU, a monochrome monitor, and keyboard. The system based on the PC 6300 is priced at $4,200 and the version based on the PC 6300 Plus is $5,090. Delivery begins in October.

AT&T Information Systems, 1 Speedwell Ave., Morristown, N. J. 07960.
Phone (800) 247-1212 [Circle 373]



Burr-Brown came to Livingston for the workforce.

For Burr-Brown, the requirements for their European location were relatively straightforward.

A clean environment, modern facilities and direct transport and communication links with continental Europe.

They found all this in Livingston, Scotland.

A town purpose-built for new industries situated at the heart of one of the greatest concentrations of electronic companies in Europe.

And they found much more.

They found investment grants of up to 35%, rent-free periods plus European Community assistance. They found Kirkton Campus, a high-technology park ready-made to receive them.

And they found us.

A Development Corporation that could help them develop at every turn and a workforce that was both skilful and conscientious.

In Burr-Brown's words, one whose productivity was 'second to none in the world'.

A 20 minute drive down the M8 motorway and they're in Edinburgh. Scotland's capital city and a distinguished I.T. community that's home to no less than four Technology Transfer units.

Including the Wolfson Micro-electronics Institute and the Centre for Applications Software Technology.

Today, Burr-Brown is one of a long list of blue chip Livingston residents with firm plans for expansion.

A list that we can offer you every incentive to join.

To: C. Anne Robins, PO Box 345, Old Greenwich, CT 06870. Tel: (203) 629-3496.
Prove that Livingston is Europe's most logical location for my company. BLOCK LETTERS PLEASE.

Name _____

Position _____

Company _____

Address _____

_____

_____

Zip Code _____

Telephone _____

E9

MAKE IT IN LIVINGSTON

Europe's most logical location.

FAST ERROR-CORRECTION CODE FITS INTO 24-PIN DIP

ALGORITHM IMPLEMENTED IN SILICON BUNDLES PARITY AND DATA BITS FOR QUICK TRIPLE-BIT ERROR FIXES

A new CMOS IC packs a powerful short-block, forward error-correcting code into a 24-pin DIP. The component from Space Research Technology Inc. of Houston implements a 24-12-03 extended Golay algorithm in silicon, bundling 12 parity bits with 12 data bits.

The half-and-half, parity-data bit combination enables the Hyper-FEC III chip to quickly fix triple-bit errors in each 12-bit block of information. Silicon integration of the random bit-error-fixing Golay code is expected to open up its use in a broad range of data-communication applications, including the embryonic market for very-small-aperture terminals receiving one-way satellite transmissions. The extended, short-block Golay code normally requires a pc board full of logic components and software.

In addition to so-called micro earth stations, the new IC is also expected to be applicable in terrestrial data-communication links such as twisted-pair networks, fiber-optic networks, and microwave transmissions. Space Research president Ben Midulla says the Golay code can also be used in correcting burst bit errors, if the glitches are scattered throughout the data, using interleaving circuits ahead of the Hyper-FEC III chip. Interleaving the incoming data will enable system integrators to use the IC to correct block-bit errors typically coming from high-density optical disks, Midulla suggests.

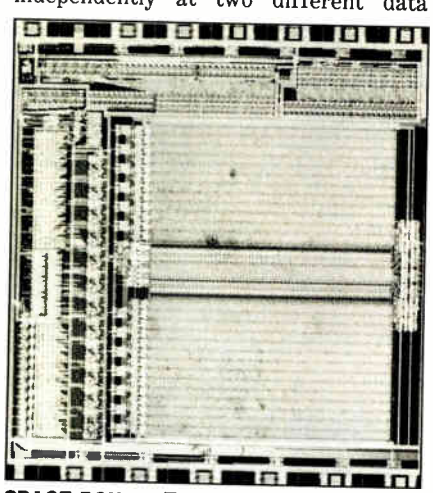
Made in 3-μm CMOS, the Hyper-FEC III error-correction chip contains an encoder and a decoder that can operate independently at two different data rates with two clock signals. The device will operate at bit rates of up to 5 Mb/s, counting parity bits (the maximum data rate is 2.5 Mb/s). The chip uses what is known as a hard-decision decoding process, which is performed after the data has been converted from analog to digital form. The channel error rate is 1 in 10^4 bits transmitted.

The chip's decoder block contains a self-checking autosynchronization circuit that synchronizes transmissions with the reception of two complete error-free code words. "The autosync circuit and the short-block Golay code enable the device to achieve synchronization very quickly, which is important in satellite and optical disk applications," notes Lawrence J. Rennie, vice president of engineering.

The Hyper-FEC III chip's total encoder-decoder delay period is the time it takes 40 bits to pass through the IC. The chip, which is being fabricated by VLSI Technology Inc. for Space Research, is available with both TTL and CMOS logic outputs. Each output will drive two standard TTL loads. The chip operates over a commercial temperature range of 0°C to 70°C.

In quantities of up to 100, the Hyper-FEC III sells for $195 each. Samples are available now. Look for Space Research to introduce soon a 16-pin Hyper-FEC chip, which will be fabricated from 2-μm CMOS and with a new pipelined architecture. It will offer a data rate of 20 Mb/s. *–J. Robert Lineback*

Space Research Technology Inc., 507 Three Corners, Houston, Texas 77024. Phone (713) 461-5849 [Circle 440]



SPACE BOUND. The chip works in satellite transmissions as well as in terrestrial ones.

DIALER CHIPS NEED ONLY 1.7 V TO HOLD NUMBERS

Motorola Inc. executives say there's been a sudden resurgence of design activities at American phone-set makers. And their company is trying to grab a bigger share of that growing market by launching a new series of telecommunications dialer chips. Four CMOS chips—three with on-board memory—are the first dialer ICs that Motorola's MOS telecommunications operation in Austin, Texas, has introduced since the late 1970s [*Electronics*, Aug. 21, 1986, p. 21].

"The dialer business has gone absolutely crazy!" exclaims Al Mouton, Motorola's MOS telecom marketing manager. "A lot of people thought the dialer business was going away and many semiconductor firms pulled the cork. We find ourselves in a position to take over with a new line of parts and a new market wanting more features over low-cost phone sets."

To answer the phone makers' call for features and for chips that consume less power, Motorola is unveiling the MC145412 and MC145413 repertory pulse/tone dialers, as well as the MC145410 pulse/tone dialer with last-number redial capability. A fourth chip, the MC145409 pulse dialer (with no automatic redial), is also being fabricated in low-power silicon-gate CMOS.

The repertory pulse/tone dialers, 145412 and 145413, contain memory storage for nine 18-digit telephone numbers, plus last-number redial. The 145410 dialer stores 21 digits.

All three may be used with 3.579545 MHz color-burst crystals and standard 2-of-7, 2-of-8, and Form A keypads. A 500-Hz tone-signal output in the pulse mode is fed back to the phone-set user to indicate that dialing is in progress. The MC145412 is pin-compatible with Sharp Electronics Corp.'s LR4803, while the MC145413 has the added ability to change dialing modes through a keypad-selectable switch.

"A key feature of these chips is the low-voltage memory retention. The memory will hold numbers with voltages as low as 1.7 V," notes Mouton. Current supply for the dialers when active is typically 75 μA in the pulse mode and 1 mA in the tone mode.

In quantities of 10,000 pieces or more, the MC145410 dialer is priced at $1.34 each. The MC145412 and MC145413 repertory dialer chips sell for $4.07 each. The MC145409 dialer sells for $1.09 each. *–J. Robert Lineback*

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78762. Phone (512) 928-6880 [Circle 441]

TEST SET WORKS ON VOICE-GRADE CIRCUITS

A transmission-impairment measuring set brings troubleshooting to data-communications operators on a tight budget. The $7,900 HP 4947A diagnoses impairments on voice-grade data circuits

either in a stand-alone configuration or as part of an automatic test system.

The system features a full measurement set and can obtain data on signal level and frequency, message-circuit noise, noise with tone, signal-to-noise ratio, and other variables. It also has a print-and-plot output and an IEEE-488 interface. The 4947A also performs automatic sequence measurements. Delivery takes about eight weeks.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 449]

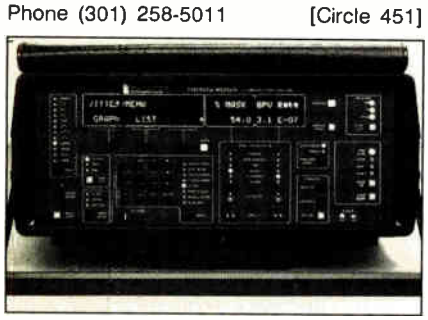
TOOL ANALYZES MANY FUNCTIONS

The Fireberd 6000 communications analyzer tackles signal, timing, and performance analysis. The unit has a clock-slip detector, frequency counter, and inverted-clock detector and uses a frequency synthesizer to operate at programmable rates for synchronous, asynchronous, and recovered clock applications.

With an optional T-carrier interface, the 6000 can perform bipolar, logic, framing, and error analysis on extended superframe and D4 framing formats. Jitter-generation and -measurement capabilities, including spectral analysis with multiple jitter masks, are standard.

The Fireberd 6000 costs $7,995. Delivery takes 90 days.

Telecommunications Techniques Corp., 444 N. Frederick Ave., P. O. Box 6027, Gaithersburg, Md. 20877.
Phone (301) 258-5011 [Circle 451]



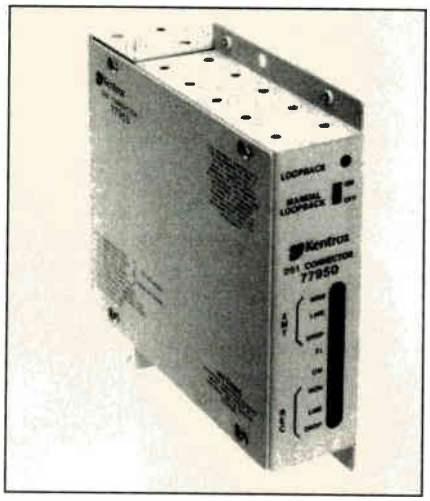
LINK STANDARDIZES T1 CONNECTIONS

The DS1 connector for providers of T1 data-communications services provides an RJ-48C modular jack to standardize the connection to all customer-premises equipment while performing a number of other tasks. These functions include dc isolation, simplex power looping, remote DS1 signal loop-back, line build-out, and loss-of-signal detection.

The DS1 digital service interface is installed at the network interface—the point of demarcation between the network and the customer's wiring. With the DS1, problems can be isolated and diagnosed by the central office, reducing costly service calls.

Pricing and delivery information for the DS1 was unavailable at press time.

Kentrox Industries Inc., P. O. Box 10704, Portland, Ore, 97210.
Phone (503) 643-1681 [Circle 453]

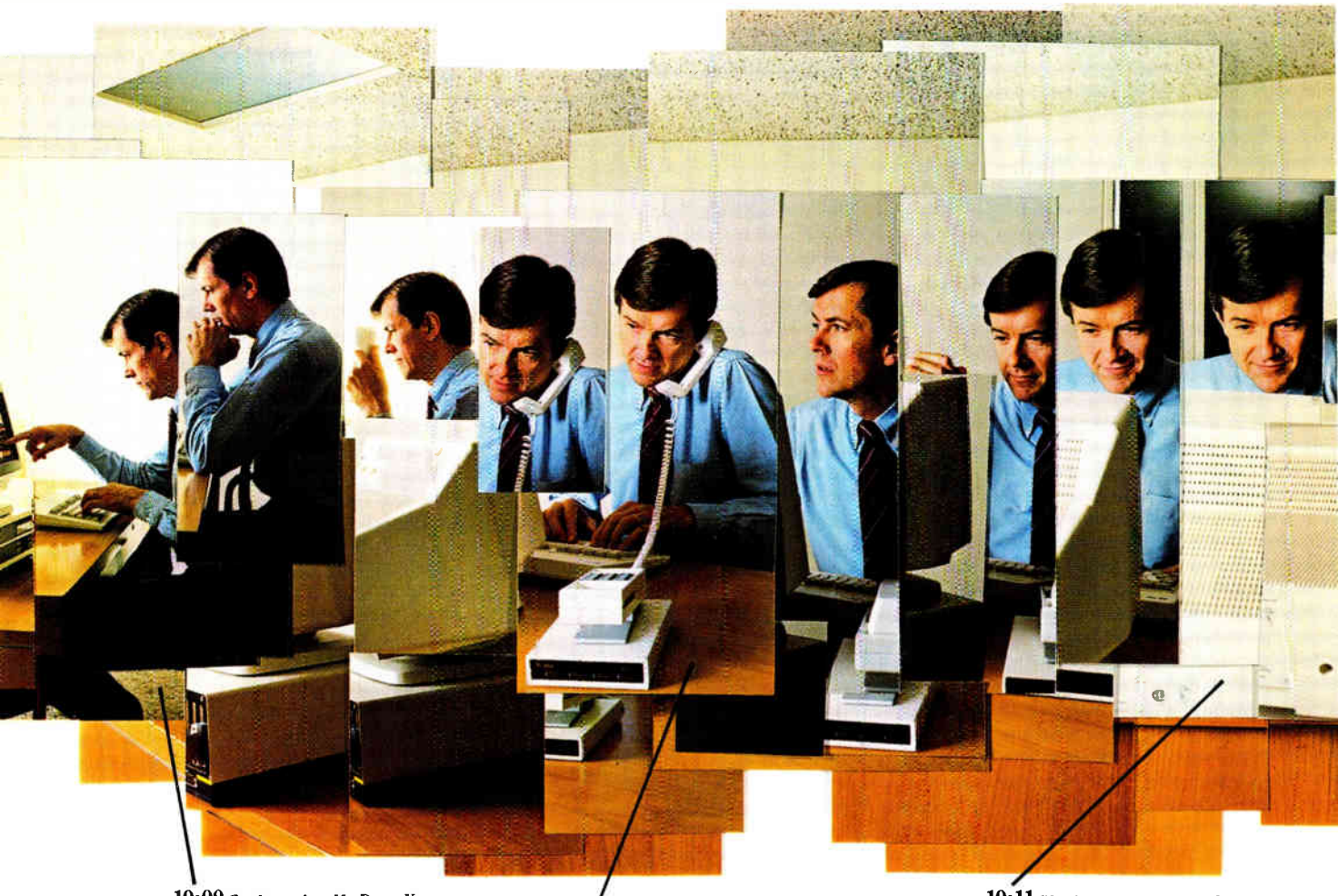


MODEM FLIES ALONG AT 18 KB/S

The Trailblazer modem has been upgraded to run at 18 kb/s, up from a previous high of 10 kb/s. GTE Supply, which markets the product for Telebit Corp., Cupertino, Calif., claims Trailblazer is now the industry's fastest dial-up microcomputer modem.

The modem automatically adjusts to line conditions by altering its speed. Internal error correction guarantees 100% error-free transmission. Trailblazer is available now. Add-in boards for microcomputers are priced at $1,995; stand-alone versions,at $2,395. Existing Trailblazers can be upgraded in the field for $99 or in the factory for $250.

GTE Supply, 5225 Wiley Post Way, Lakeside Plaza 2, Salt Lake City, Utah 84116 [Circle 450]



10:00 *Good morning, Mr. Drew. Your mission: revise monthly market forecast and update client roster. Fast. Your secret weapon: an AT&T PC 6300 PLUS with Simul-Task.*

10:05 *As you enter new names in client database, this remarkable PC is already tapping a Denver mainframe for the market figures you will need.*

10:11 *Obeying pre-set commands, your new AT&T PC enters market data in spreadsheet. It will simultaneously run your spreadsheet and print from the database. So why not get some coffee?*

26 MINUTES IN THE LIFE OF

The machine is AT&T's PC 6300 PLUS. At its heart, a bit of technological lightning that permits the computer to do several tasks at once.

This AT&T breakthrough is called Simul-Task. It mightily expands the usefulness of the PC experts already place in the first rank of today's more powerful "80286" machines.

One manager likens Simul-Task to having an assistant handle one chore while you get on with another. With Simul-Task aboard, the AT&T PC 6300 PLUS can comb through a database for the figures you need while *you* update a memo...or print out a report while *you* set up a spreadsheet.

SIMUL-TASK: THE SOUL OF A BETTER PC

There exist few machines that can match the power of AT&T's PC 6300 PLUS. The speed is intoxicating, the graphics razor sharp. Look hard enough, and you may find a similar machine. But you will find none that can *apply* its power to one of your existing PC programs—and to other jobs at the same time.

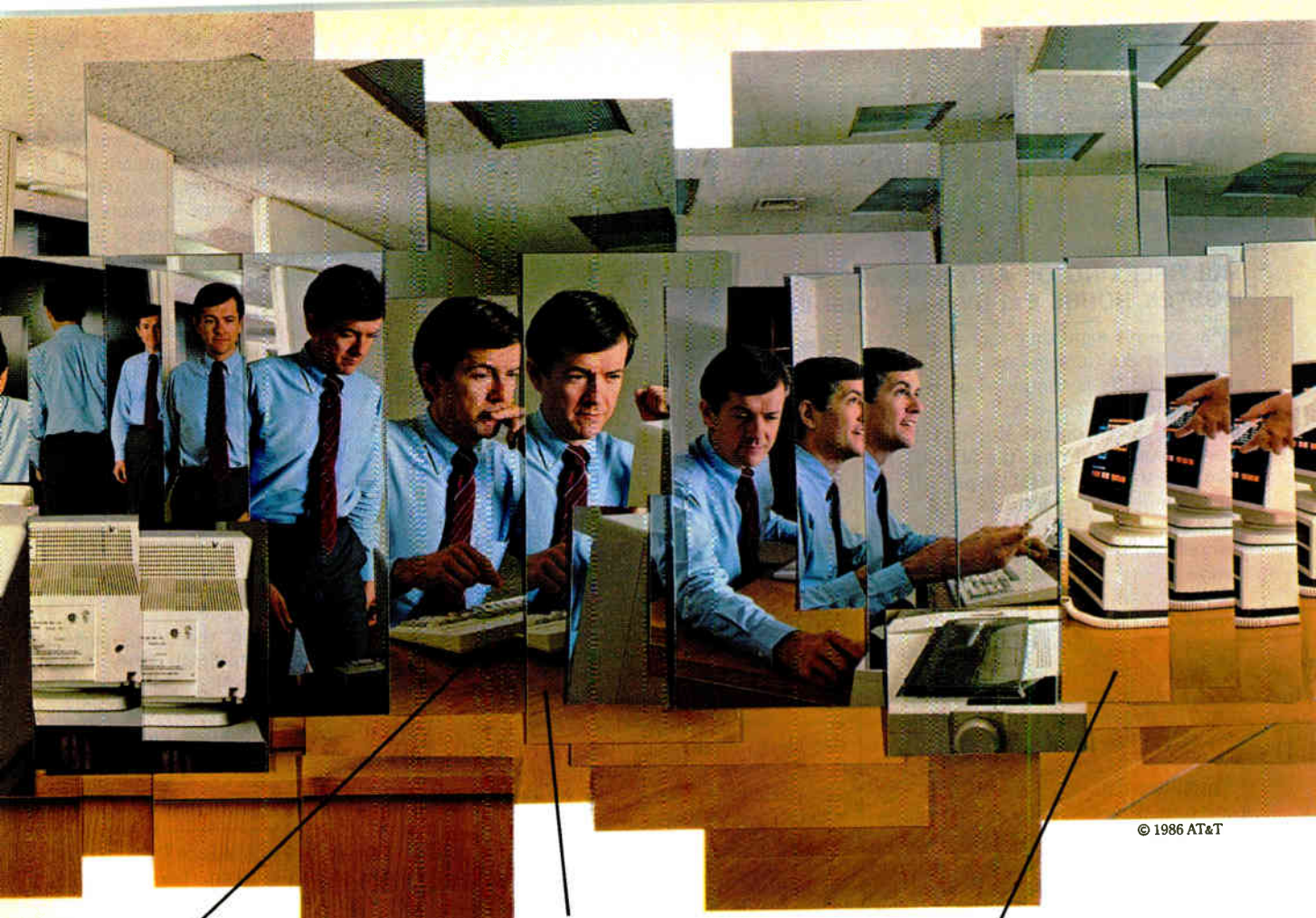
Caveat emptor: You can pay plenty for software that lets you *look* at several programs at once. AT&T's Simul-Task *runs* several programs at once. It's the difference between window shopping—and getting things done.

The secret: Simul-Task unlocks the full potential of the "80286" processor chip. So you have all the benefits of today's PC software, without the limitations of today's PCs.

Simul-Task gives anyone who sits down at an AT&T PC 6300 PLUS the ability to do more—and do it faster—than users of other PCs. But there is more to the Simul-Task story.

Item: Simul-Task opens the door to better data communications. Two keystrokes can tap you in to a mainframe 1,500 miles away, or the PC down the hall.

Item: Even as you run one, two, or three business



10:16 *The spreadsheet is almost done, but you needn't wait for it to finish. AT&T's Simul-Task lets you update your cover letter while other programs run.*

10:20 *Send FYI report to branch managers via electronic mail. One command reminds the PC to back up files during lunch hour.*

10:26 *Boss stops by. Hard copy just happens to be ready. Well done, Mr. Drew! And welcome to the world of Simul-Task.*

TODAY'S MOST PRODUCTIVE PC.

programs, the PC 6300 PLUS is open to receive and store electronic mail or data someone else is sending to *you*. No matter what programs you are running, your "mail" is just three keystrokes away.

Item: You put your computer on "automatic pilot," running time-consuming jobs like database sorts after hours. Rather like setting a VCR to tape tomorrow night's movie.

COMPUTERS WITH THE FUTURE BUILT IN

Most of today's 19 million PCs are islands unto themselves. But tomorrow is coming up fast. For some companies, the next step is tapping a remote database. For others, it is networking one PC to another. Or uniting all their computers in a larger constellation.

Here Simul-Task shines. For many companies, AT&T's PC 6300 PLUS with Simul-Task can be the bridge between today's *personal* computer applications...and tomorrow's *company-wide* applications.

When the time comes to take the next step, you'll be ready. AT&T makes the pieces fit.

How much will all this cost? The exact figure depends on how you equip your system, but most companies have been pleasantly surprised. And right now (for a limited time) you can get even more for your money.

To learn more, and to arrange for a Simul-Task demonstration, please contact your AT&T Account Executive, stop by any authorized AT&T supplier, or telephone 1 800 247-1212.

AT&T
The right choice.

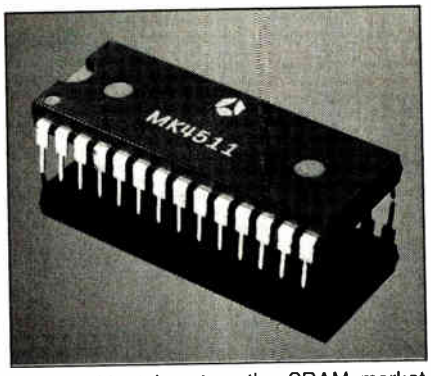
DUAL-PORT SRAM HAS ON-CHIP ACCESS LOGIC

MULTIPLEXING OF ADDRESS AND DATA LINES LETS MOSTEK HOUSE 512-BY-9-BIT CHIP IN A 28-PIN DIP

The control logic that coordinates access by multiprocessors to dual-ported static RAMs is contained on board a new CMOS 512-by-9-bit RAM from Thomson Components-Mostek Corp. Mostek was able to put the MK4511 BiPort SRAM in a low-cost 28-pin DIP by using multiplexed address and data pins. The 48-pin DIP currently on the market houses some nonmultiplexed parts.

Data stored at each addressable location of the 4511 can be simultaneously accessed from both the input/output ports because the memory array is made up of 8-transistor BiPort memory cells. The dual-ported SRAM is available with access speeds of 120, 150, and 200 ns.

To assure data integrity, Mostek has incorporated software-controlled interrupt outputs and addressable status-control flags into the chip's design. The interrupt-control registers are made up of two blocks of flip-flops. The control logic represents a departure from other dual-ported memory architectures, which use arbitration techniques to resolve memory-array contention.



SMART. Mostek enters the SRAM market with a chip that has on-board control circuitry.

"An arbitrator will give you either the old byte or the new byte of data, but often you are not sure, and that can be a problem for many multiprocessor applications," says David Chapman, who manages new product definition and applications for the Memory Products division at Mostek. Other dual-ported memories require off-chip logic to implement the multiprocessor control.

The new 4511 is targeted at a broad range of multiprocessor environments and real-time personal-computer applications, such as process control. In many multihost applications, the 4511 will act as a "message box" between processors.

Fabricated in a 3-μm CMOS process, the 4511 has a typical power dissipation of 275 mW in the active state and 11 mW in the standby mode. The BiPort SRAM is available for commercial operating temperature ranges (0°C to +70°C) or full military conditions (−55°C to +125°C).

In quantities of 100, the 120-ns parts sell for $26.40 each in plastic DIPs. The 150-ns parts are priced at $22.86 each and the 200-ns chips at $21.43 each, also in lots of 100. Mostek plans to offer the device in a surface-mountable plastic-leaded chip carrier during the first quarter 1987. *–J. Robert Lineback*

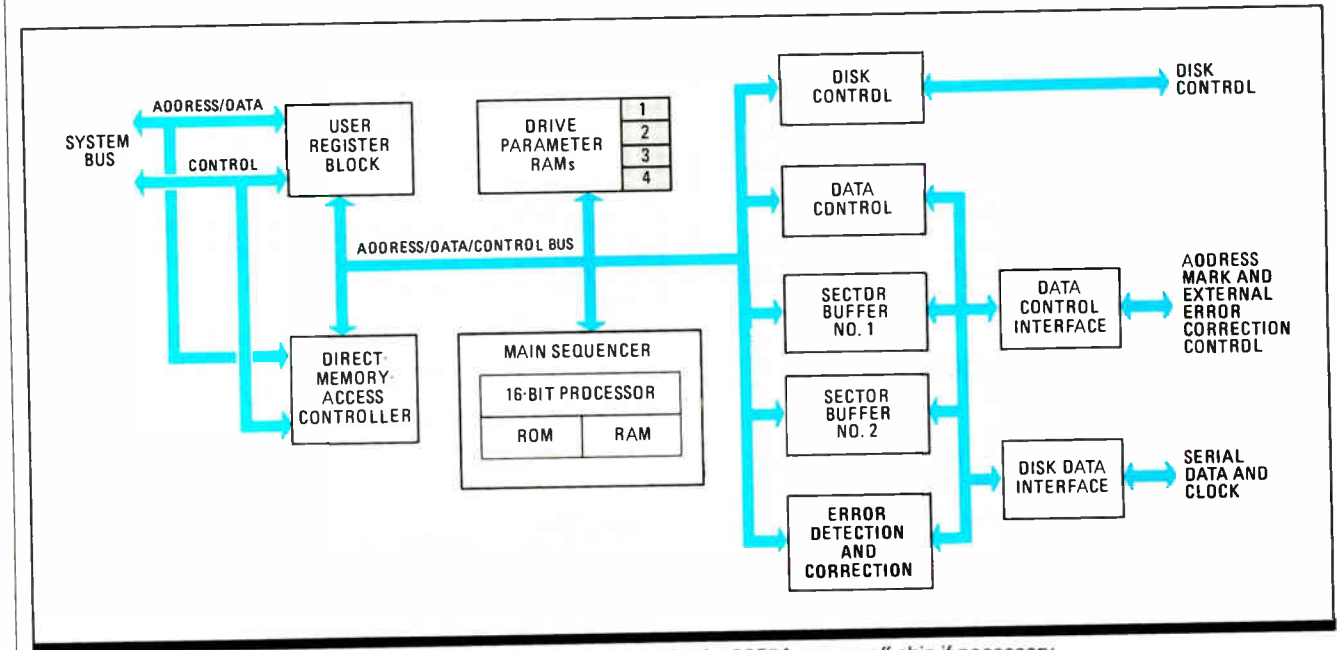
Thomson Components-Mostek Corp., 1310 Electronics Dr., Carrollton, Texas 75006. Phone (214) 466-6000 [Circle 360]

DISK-CONTROLLER IC RUNS 4 DRIVES

The latest board-level computer subsystem to disappear inside silicon is the disk controller. The Am9850A, this week's Liberty Chip from Advanced Micro Devices, is a disk-drive controller that boasts on-chip direct memory access and dual buffers, so it can talk to the host and the disk drive at the same time. In addition, the chip has a trio of error-correcting routines.

The controller can run from one to four hard- or floppy-disk drives. The characteristics of each can be programmed by the user.

With the companion 9851 modified FM



OUTSIDE HELP. In addition to its three error-correcting procedures, the Am9850A can go off chip if necessary.

data separator, the 9850A supports both the 5-Mb/s ST506 and the 10-Mb/s ST412 interface standards. Replacing the 9852 with three 22V10 programmable-array-logic chips to perform run-length-limited data separation allows the new controller to support the Enhanced Small Disk Interface at up to 15 Mb/s.

HANDSHAKING. The 9850A performs three kinds of on-chip error checking: a simple 16-bit cyclic redundancy check and both single- and double-burst Reed-Solomon error detection and correction. In addition, the controller chip will provide the handshake signals required to implement an error-checking and -correcting algorithm through external ECC circuitry.

The double buffer improves system throughput, because it allows the on-board 16-bit processor to read or write an entire track in a single disk revolution. Without the extra buffer, the controller would have to skip sectors while communicating with the host. Users can program sector sizes of 128, 256, or 512 bytes.

The basic unit of the command structure, the I/O parameter block (IOPB), is stored in system memory by the host processor. Each IOPB specifies one disk command and contains the parameters needed to execute it. The chip fetches these IOPBs through a DMA controller.

The chip's DMA controller fetches the commands, writes status information, fetches data to be written on disk, and writes data read from disk. It is programmable to adjust for bus occupancy.

A linked-list data structure allows IOPBs that reside in system memory to be executed by the on-board processor without host intervention. A list of commands can thus be set up by the host and executed by the controller chip without further aid from the host. The on-chip processor can overlap seeks by scanning ahead in the command chain.

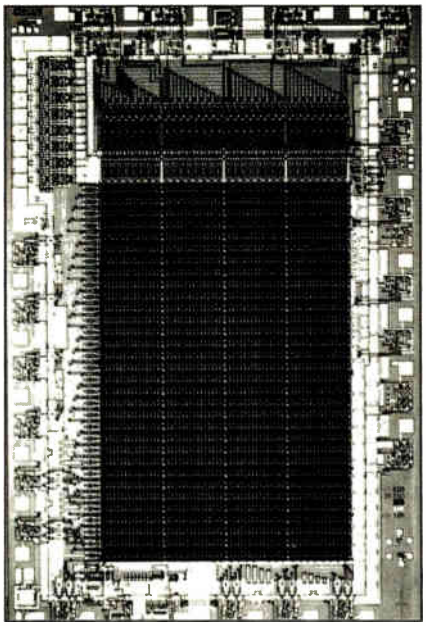
The 9580A is built in 1.6-μm n-channel MOS technology. Priced at $53 in 100-unit lots, it is available immediately. The 9851 data separator will be available later this year.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 361]

FAST CMOS SRAM IS ECL-COMPATIBLE

Saratoga Semiconductor now has available a four-member family of 4-K ECL-compatible static RAMs with access times of 15 ns. The four devices, the SSM10470, -10474, -100470 and -100474, are fabricated in the company's proprietary self-aligned bipolar CMOS technology, Sabic II.

Two of the SRAMs are organized as 4-



K-by-1-bit, one for 10K or 10KH ECL levels and one for 100K ECL levels. The remaining two are organized as 1-K-by-4-bits, one for 10K or 10KH ECL levels and one for 100K ECL levels.

Unlike ECL RAMs on the market, Saratoga's use the full six-transistor cell architecture found on CMOS SRAMs, which allows them to offer lower power consumption than ECL RAMs, improved radiation tolerance, and a lower soft-error failure rate during exposure to alpha particles.

The RAMs are priced from $14.55 to $19.55 each in lots of 100 pieces.

Saratoga Semiconductor, 10500 Ridgeview Ct., Cupertino, Calif. 95014.
Phone (408) 973-0945 [Circle 373]

16-BIT DSP CHIP BLAZES AT 25 MHz

A 25-MHz single-chip CMOS digital signal processor, the DSP320C10-25, is pin-for-pin compatible with the industry-standard n-MOS version from Texas Instruments that it equals in speed. Fabricated in a 2-μm n-well CMOS process, the 16-bit chip executes 6.25 million instructions/s, faster than other similar CMOS parts, the manufacturer claims.

The chip operates at between 15 and 25 MHz, with a typical current drain of 40 mA from a 5-V supply. It is available in commercial, industrial, and military temperature-range grades.

The commercial and industrial versions come in a 40-pin plastic DIP or a 44-pin plastic leaded chip carrier; the military part is packaged in ceramic. Prices start at $55 each in lots of 100. All versions are available now.

General Instrument Corp., Microelectronics Division, 2355 W. Chandler Blvd., Chandler, Ariz. 85224.
Phone (602) 963-7373 [Circle 366]

70-NS MULTIPLIER DISSIPATES ½ W

By using the Am29C509 12-by-12-bit CMOS multiplier instead of the TRW bipolar TDE1009J, engineers can cut power consumption by 83% while boosting speed 50%. The 70-ns part dissipates less than 0.5 W.

The Am29C509 features a 27-bit product-accumulation result that provides 24-bit product plus 3-bit extended product. This allows for the accumulation of values larger than the normal accumulator width.

The chip's instruction set allows the loading of the accumulator, and either adding or subtracting the product from the accumulator value. The Am29C509 is suited for digital signal processing, video processing, medical image processing, telecommunications, and radar and sonar.

Available now, the chip sells for $65 each in lots of 100. It comes in a 64-pin ceramic DIP.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 367]

2-MICRON ARRAYS BOAST 16 mA DRIVE

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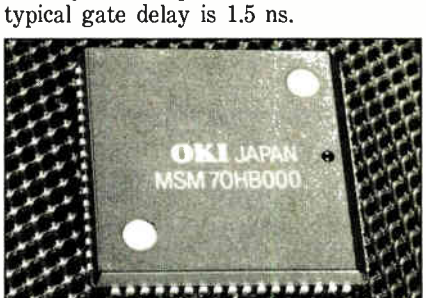

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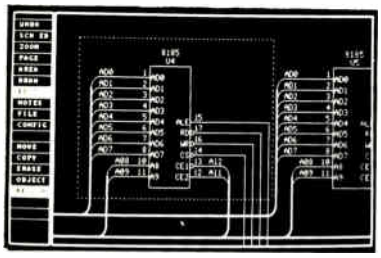

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MEETINGS

1986 IEEE International Electronic Manufacturing Technology Symposium, Components, Hybrids, & Manufacturing Technology Society of the IEEE (IEEE Council Office, 701 Welch Rd., Suite 2205, Palo Alto, Calif. 94304), Hilton and Tower, San Francisco, Sept. 15-17.

Networld '86, Novell Inc. (748 North 1340 West, Orem, Utah 84057), Infomart, Dallas, Sept. 16-18.

Expanded Voice Input/Output Conference, American Voice Input/Output Society (P. O. Box 60940, Palo Alto, Calif. 94306), Radisson Mark Plaza Hotel, Alexandria, Va., Sept. 16-18.

FORMAT '86, *Computer Products Magazine, et al.* (Tower Conference Management Co., 331 W. Wesley St., Wheaton, Ill. 60187), Chicago Hilton and Towers, Chicago, Ill., Sept. 16-18.

Independent Power Generation Conference and Exhibition, Fuel and Metallurgical Journals Ltd. (2 Queensway, Redhill, Surrey RH1 1QS, UK), Excelsior Hotel, London, Sept. 16-17.

CAD and CAM on the Shop Floor, Society for Computer-Aided Engineering, *et al.* (7811 N. Alpine Rd., Rockford, Ill. 61111), Adams Mark Hotel, Philadelphia, Sept. 17-18.

PC FAB EXPO, PMS Industries (1790 Hembree Rd., Alpharetta, Ga. 30201), Meadowlands Hilton, Secaucus, N. J., Sept. 17-18.

Sensors Expo Conference and Exposition, *Sensors Magazine* (Expocon Management Associates Inc., 3695 Post Rd., Southport, Conn. 06490), O'Hare Exposition Center, Chicago, Ill., Sept. 17-19.

IEEE Symposium on Logic Programming, IEEE Computer Society (1730 Massachusetts Ave. N. W., Washington, D. C. 20036), Westin Hotel Utah, Salt Lake City, Sept. 21-25.

Electronics and Aerospace Systems Conference '86, IEEE (Dr. Arvid G. Larson, Vice President, Analytic Disciplines Inc., Suite 400, 2070 Chain Bridge Rd., Vienna, Va. 22180), Shoreham Hotel, Washington, D.C., Sept. 22-24.

Ultratech Conferences and Expositions, Society of Manufacturing Engineers *et al.* (P. O. Box 930, Dearborn, Mich. 48121), Convention Center, Long Beach, Calif., Sept. 22-25.

Buscon/East-86, Multidynamics Inc. (17100 Norwalk Blvd., No. 116, Cerritos, Calif. 90701), World Trade Center, Boston, Sept. 23-24.

Nepcon Southwest, Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), Infomart, Dallas, Sept. 23-24.

Artificial Intelligence & Advanced Computer Technology Conference and Exhibition/Europa '86, Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Rhein-Main Halle, Wiesbaden, West Germany, Sept. 23-25.

Engineering and Manufacturing Software Conference/Exhibition, Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Chicago Hilton and Towers, Chicago, Sept. 23-25.

International Test & Measurement Exhibition, Gambica (Network Events Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK), Grand Hall Olympia, London, Sept. 23-25.

1986 International Symposium on Gallium Arsenide and Related Compounds, (W. T. Lindley, Room E118E, Massachussetts Institute of Technology, 244 Wood St., Lexington, Mass. 02173), Caesar's Palace, Las Vegas, Sept. 28-Oct. 1.

IECON '86, IEEE (Richard C. Born, Rexnord Inc., 5101 W. Beloit Rd., Milwaukee, Wis. 53214), Hyatt Regency Hotel, Milwaukee, Sept. 28-Oct. 3.

1986 Applied Superconductivity Conference, IEEE (Lahni Blohm, Code 6630C, Naval Research Laboratory, Washington, D. C. 20375), Hyatt Regency on the Harbor, Baltimore, Sept. 28-Oct. 3.

1986 National Communications Forum, National Engineering Consortium (505 N. Lake Shore Dr., Suite 4808, Chicago, Ill. 60611), Ramada Hotel O'Hare, Rosemont, Ill., Sept. 29-Oct. 1.

Satech '86, Intertec Communications Inc. (Sam Davis, 2472 Eastman Ave., Bldg. 34, Ventura, Calif. 93003), Indiana Convention Center & Hoosier Dome, Indianapolis, Sept. 29-Oct. 3.

Automated Design and Engineering for Electronics East, Cahners Exposition Group (1350 E. Touhy Ave., P. O. Box 5060, Des Plaines, Ill. 60017), World Trade Center, Boston, Sept. 30-Oct. 2.

Conference on Electromagnetic Compatibility, Institution of Electronic and Radio Engineers (99 Gower St., London WC1E 6AZ, UK), University of York, York, UK, Sept. 30-Oct. 3.

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ELECTRONICS WEEK

GOULD WILL SELL DEFENSE BUSINESS

Gould Inc., Rolling Meadows, Ill., is putting its defense systems business up for sale. The unit accounted for about 28% of the firm's $1.4 billion in sales last year, but has recently become a source of problems—such as a $130 million writedown in this year's first quarter due to cost overruns on fixed-price defense contracts. Gould says divestiture of the defense business will allow it to concentrate on commercial electronics, including minicomputers, factory-automation systems, and semiconductors. But the move has fueled speculation that Gould is grooming itself for acquisition by a foreign company. West Germany's electronics giant, Siemens AG, reportedly held talks with Gould last year.

PETRITZ SEEKS STARTUP FUNDS

Richard L. Petritz, founder and former chairman of the board of Inmos Corp., is raising capital for his startup, Simtek Corp. The company, which will be based in Colorado Springs, will develop electrically erasable programmable read-only memories using metal-nitride-oxide-semiconductor technology.

ASHTON-TATE ENDS COPY PROTECTION

Bowing to customer pressure, microcomputer software house Ashton-Tate is removing copy protection from all its products sold in the U.S. Large corporate customers have been complaining that copy protection slows the operation of their personal computers. The latest move covers the Torrance, Calif., company's dBase III Plus, dBase III Plus LAN Pack, and Framework II. The Multimate line of word-processing programs is already unprotected. At the same time, Ashton-Tate announced that its newly established Systems, Service, and Information Division will offer support plans to individual and corporate users.

MOTOROLA TO SELL TOSHIBA'S DRAMS

Motorola Inc. is ending its brief absence from the turbulent market for 64-K and 256-K dynamic random-access memories. The company's MOS memories operation in Austin, Texas, says it is now offering n-channel DRAM chips fabricated by Toshiba Ltd. in Kawasaki, Japan. Toshiba dice for the parts are assembled and tested by Motorola in Malaysia. Motorola bailed out of the DRAM business last fall when prices fell too low to make a decent profit. The company says it is now working on new submicron CMOS technologies that could be applied in the future to 1-megabit DRAMs as well as to static RAMs and erasable programmable read-only memories.

ELECTRONICS SALES SLOW IN EARLY '86

Shipments of electronic equipment and components slipped 1.8% for the first half of 1986, according to the Electronic Industries Association. Total shipments were $99.5 billion for the first six months, down from $101.3 billion a year ago. Consumer electronics and electronic-related goods and services were up 10.8% and 9% respectively, says the Washington-based organization. But that wasn't enough to make up for a 12.8% decline in computer and industrial electronics shipments, according to the industry group.

CORNELL TO HOST IC CARRIER STUDY

Semiconductor Research Corp., a consortium of U.S. electronics, computer, and communications companies, is sponsoring a program aimed at improving integrated circuit packaging. The Electronics Packaging Sciences Research Program at Cornell University in Ithaca, N.Y., will begin with $250,000 in funding from SRC and corporate sponsors including IBM Corp. and General Electric Co. It will focus on the size and reliability of packages and the heat retention and expansion properties of their materials.

SOFTWARE SALES DOWN IN STORES

Unit sales of microcomputer software through retail channels dropped 16% from May to June, and dollar sales slipped 17%, according to Infocorp. The slide was across the board, with software sales down 26% for the Apple II, 13% for the Macintosh, and 12% for the IBM Personal Computer and compatibles. These sales were at their lowest level since the Cupertino, Calif., market watcher began tracking retail outlets 20 months ago. Infocorp says other sales channels, such as mail-order, are eating into the retail outlets' share of the high-end ($500 or more) software market.

TANDON SPLITS INTO TWO DIVISIONS

Tandon Corp. is splitting its operations into two independent business units—one devoted to personal computer systems and the other concentrating on disk drives and subsystems. Each will be a separate entity with its own management, manufacturing, marketing, engineering, and research organizations. The company says the restructuring will help cut its payroll by about 10%.

U.S. FLOPPY-DISK REVENUE DECLINING

Unit sales for the U.S. floppy-disk industry jumped 15.3% in 1985, but that wasn't enough to make it a good year. Actual revenue from floppy-disk sales dropped 16.8%, according to the International Tape/Disc Association. Total unit sales of all sizes of floppy disks reached 386.1 million, up from 334.8 million in 1984. Dollar volume, however, dropped by nearly $100 million, to $476.76 million. Sales of 3½-in. microfloppy disks led the growth curve with 18.1 million units in 1985, an increase of 123%. But even these were not immune to price erosion, as dollar volume grew by only 69.6% for the same period.

CONCORD SPINS OFF ITS LAN DIVISION

Concord Data Systems Inc. is spinning off its local-area-network division as an independent company. The Marlboro, Mass., company will retain its modem business, however. The new company, Concord Communications Inc., with initial capitalization of $9.5 million, will concentrate on LAN products for the factory environment. It is headed by president Tony Helies, who joined Concord last December from Analog Devices Inc.

$7,000 CD PLAYER CAN RECORD TOO

The ultimate in consumer audio may be here. CompuSonics Corp., of Palo Alto, is planning to offer by Christmas a $7,000 editable audio-optical disk recorder—the first such machine to make use of the write-once, read-many (WORM) optical disk technology. The DSP-1000 uses a 5¼-in. WORM drive built by Optotech Inc., Colorado Springs. Thanks to CompuSonics' proprietary data-sampling and reduction algorithm, the recording time per side can be varied from 37 to 256 min. The stored data can be edited using a serial interface to Apple Computer Inc. and IBM Corp. personal computers.

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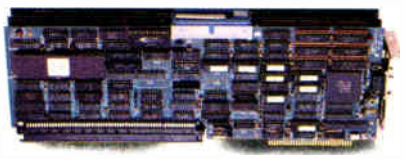
PROFESSIONAL

1280 x 1024

Only the Matrox PG-1280 graphics card satisfies the workstation display needs of technical professionals.



Plug
Select any PC AT compatible machine. The PG-1280 plugs directly into IBM's PC AT and RT PC, the Hewlett Packard Vectra, Olivetti M28, Tandy 3000, PC's Limited AT and more. The board requires two full size slots and a modest 32 watts of power.

Play
Run virtually any PC-based software package or utility imaginable. The PG-1280 is 100% compatible with both VDI and IBM's CGA and PGA standards. We support most popular applications packages including the following:

Autocad (Autodesk Inc)
Anvil 1000MD (MCS)
p-cad (Personal Cad Systems Inc)
VERSACAD (T & W Systems Inc)
Personal Designer Software (Computervision Inc)
TGRAF-07 (Grafpoint)
GKS (Prior Data Sciences)
HALO (Media Cybernetics Inc)
dBASE III Plus (Ashton Tate)
Lotus 1-2-3 (Lotus Development Corp)

Precision
See the details you have been missing. Our 1280 x 1024 bit mapped display eliminates jagged lines and fuzzy characters. The PG-1280 ensures a clear detailed display of complex drawings and schematics. The 60HZ non-interlaced refresh rate provides a crisp flicker-free display that is easy on your eyes.

Palette
Choose the colors you want. The high-res 2 Megabyte frame buffer comprises 8 memory planes, yielding 256 colors from a palette of 16.7 million shades. A separate low-res buffer with its own color palette provides CGA emulation. Both buffers are displayed on a single high resolution RGB color monitor.

Performance
Get the job done quickly. Fast response is guaranteed by a powerful new 32-bit graphics engine. Eight custom gate arrays deliver raster op (BitBlt) performance in excess of 13 million pixels per second. And, a VLSI drawing processor blasts images onto the screen at a rate of 20,000 vectors per second.

Now, if you want more information, talk with your local dealer or call us toll-free. Ask for department 16.

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Tel.: (514) 685-2630 Telex: 05-822798
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