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ISDN FINALLY STARTS TAKING OFF/57

A McGRAW-HILL PUBLICATION

# Electronics

AUGUST 21, 1986

## THE EXPLODING ROLE OF NONVOLATILE MEMORY

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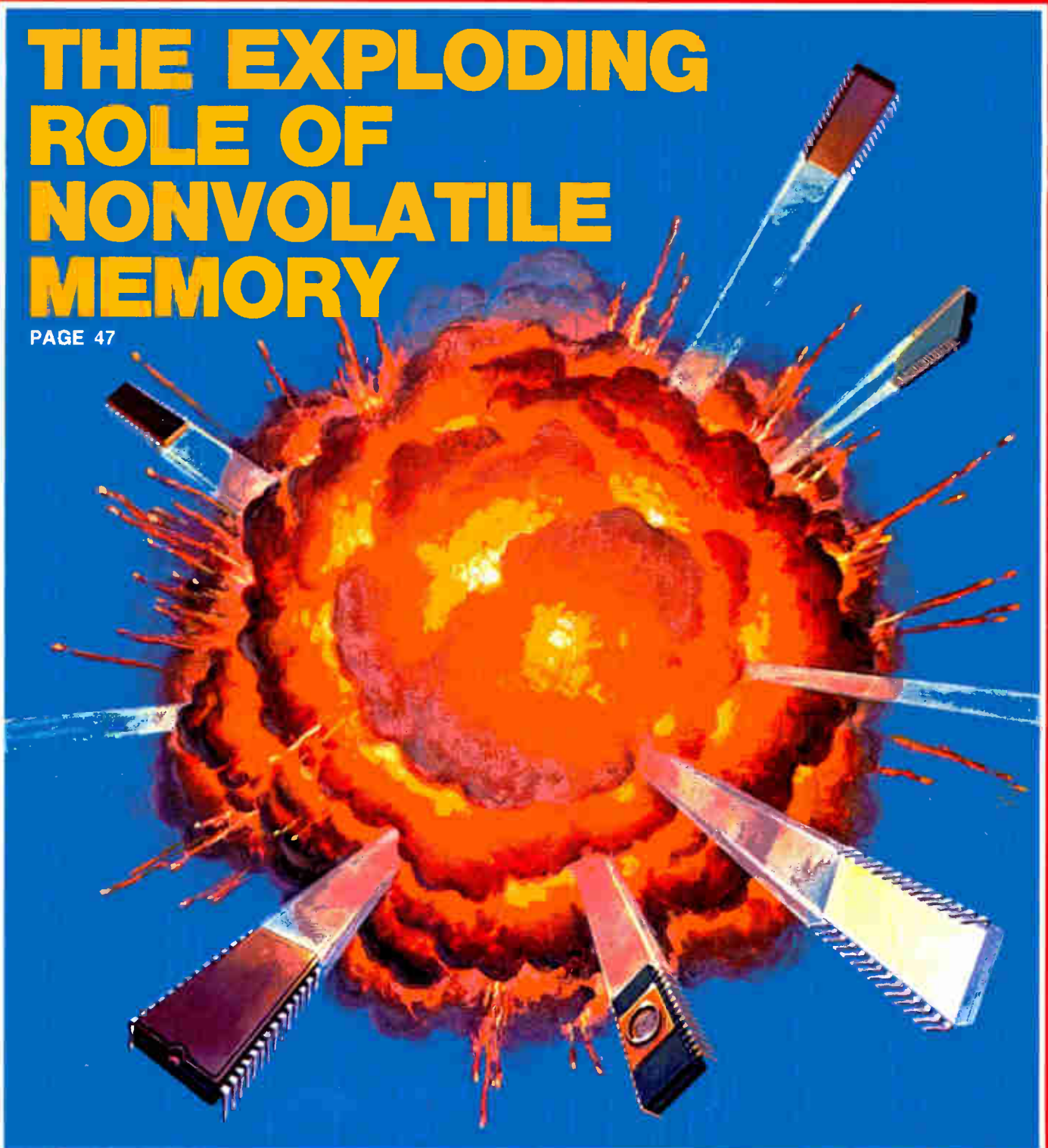

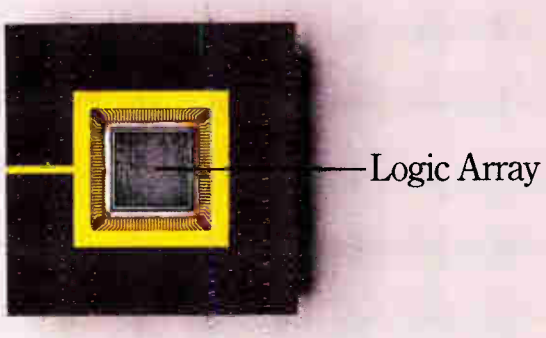


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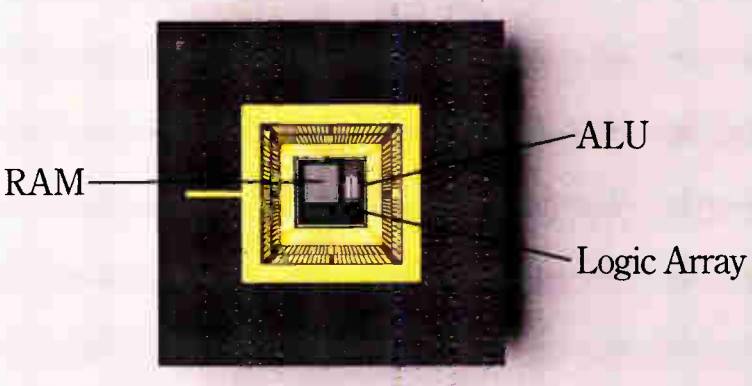


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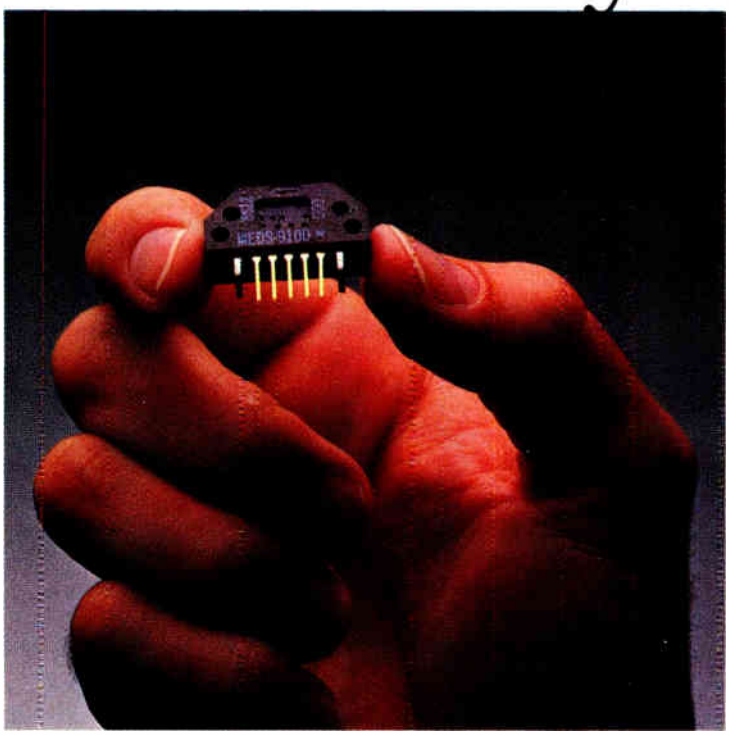


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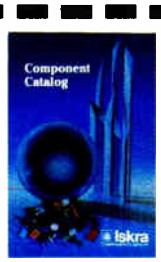


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It's been five months since Kathy O'Neill brought her unflappable efficiency to *Electronics*. And as any visitor to our production department will testify, anyone who can stay unruffled in an environment in which stories and pages at various stages of the editing and production cycle are simultaneously being put together, sent to the printer, and corrected must indeed be a special person.

**KATHY O'NEILL:** Staying calm despite production pressure.

Kathy, at 25 a veteran of both the book and magazine publishing businesses, says, "I've always been a calm person. I can't see any sense in getting excited and waving your arms and shouting. That way, nothing gets accomplished."

The New York City native started out to make a career in the fashion industry and enrolled at the Fashion Institute of Technology. After two years there and an associate's degree, she went on to Manhattan College for a BA in English. Kathy went to work for a small monthly magazine, then came to the McGraw-Hill Book Co.'s College Division as a text processor, using a Wang system to enter text corrections.

"But using the *Electronics* Atex editing and production system is a different world," Kathy says. "It's so powerful—I feel as if all I have to do is punch the keys and a magazine comes out the other end. And the system can turn around so fast: a story can be written and closed all in one day."

That's a pretty apt description of how the system works. Articles are composed on the terminals and sent along to the pertinent editors and the copy desk. Then the production department—Kathy and production manager Charlie Ciatto—lay out pages electronically from the art department's designs. The finished pages are sent to New Jersey, where film of each is made, and the film is shipped to Virginia for printing.

Kathy describes herself as a "winter person." When she isn't working—and that sometimes involves 12-hour days—she skis in the winter and travels whenever she can the rest of the year.

"The travel bug bit when I went on a 19-country student tour of Europe," she says. "That was some experience; on some days we visited two countries. But at least it gave me an idea of which countries I would like to go back to see again. Since then, I've revisited Spain, England, and Ireland."

As for the future, Kathy says she hasn't quite gotten the fashion business out of her system. "Someday I would like to own a fashion magazine," she says. But since—so far as we know—neither *Vogue* nor *Harper's Bazaar* is for sale, we expect to benefit from Kathy's talent and grace under pressure for some time to come.

Laurence Altman


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AUGUST 21, 1986

# Electronics

## NEWS



## INSIDE TECHNOLOGY



## PROBING THE NEWS

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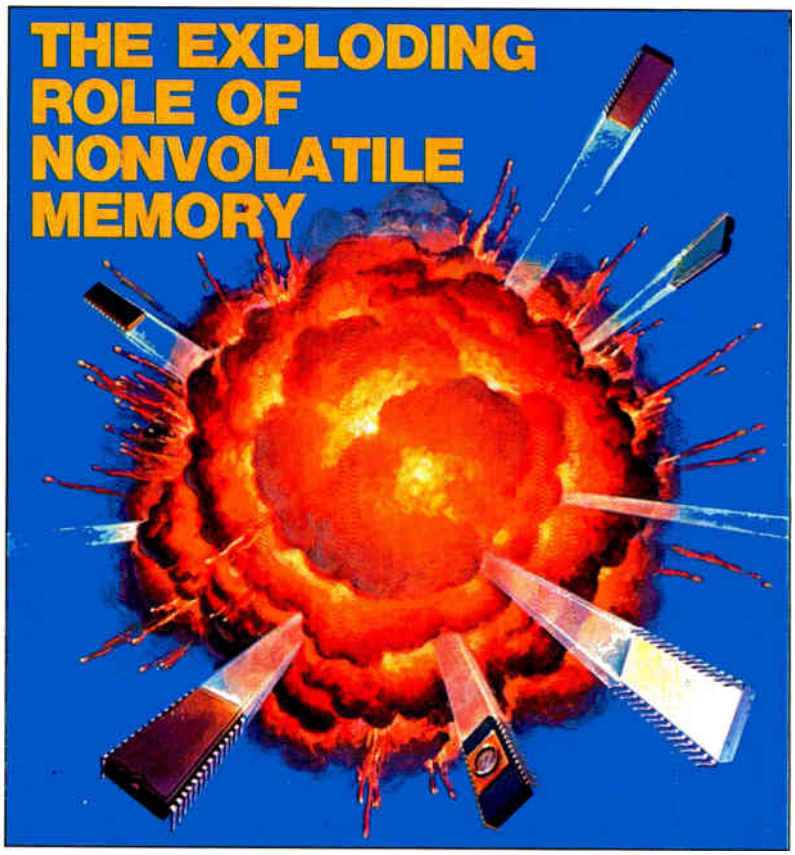


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## NEW PRODUCTS



## DEPARTMENTS

# WEEK 44

Our new Am8159 Three-Gun Graphics Color Palette is all you need to turn a dull lifeless system into one with exciting color graphics. Out of a total of 4096 colors, you can create a graphics palette of 64 colors.

**Am8159**

## Help for the colorless.

The Am8159 puts three 4-bit video DACs and a 64 x 13 RAM color map all on a single chip. That means better, more efficient performance. There's an on-chip Address Multiplexer which supports Video Address pins for the graphics mode. And System Address pins for the look-up table.

Whether you're working with a 16-bit or 8-bit system, the Am8159 delivers greater flexibility in your system performance. And with an 83 MHz pixel data rate, you'll get high resolution.

The Am8159 is just part of our complete system solution of bit-mapped graphics. So whatever system you're designing, turn to us for the solutions you need to put a lot of color in your life.

# WEEK 45

Presenting the I-only-have-a-few-milliwatts-to-spare microprocessor. The 80C31 8-Bit CMOS Single-Chip microprocessor from AMD.

If you need a low-power device, how does this sound? 120 milliwatts of operating power and 100 microwatts of standby power. With an operating speed of 12 MHz.

**80C31**

## Less is plenty.

The 80C31 is a second source for Intel's 80C31. It's a plug-in replacement. And just like Intel's, you can use our 80C31 right off the shelf because there's no ROM.

If you like the 80C31 you'll also like the rest of our single-chip microcomputer family: The 8051 single-chip microcomputer, the 8053 with twice the ROM and the forthcoming CMOS 80C51. And the EPROM versions: The 8751 and the 8753.

The 80C31: When you need a low-power device, it's good to know AMD has one designed to make the most out of the least.

# WEEK 46

Sick of working in half the space you need? Heartbroken at having to leave out those exquisite little bits of code? AMD has the cure. The 8053 Single-Chip Microcomputer.

**8053**

## 4K ROM free. No green stamps.

The 8053 is just like our high-spirited 8051 except you get 4K bytes of extra ROM. Free. Just like the 8051, it has two 16-bit timers, four 8-bit I/O ports and 128K x 8 RAM. But where the 8051 has a 4K x 8 ROM, the 8053 has an 8K x 8 ROM.

And all this doesn't cost any more than the 8051.

For prototyping and development work, we have the EPROM version: The 8753.

We think giving 4K ROM free is a very generous offer. You'll never miss the stamps.

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Circle 153 on reader service card

# WEEK 47

Just remember AMD's new 4K x 4 CMOS SRAMs: The Am99C58 and the Am99C59. They have the fastest 16K CMOS SRAM access time around: 20ns. But even at speeds like that, they don't forget what they're made of: An advanced CMOS. So they don't use much power.

**Am99C58/59**

## The fastest way to improve your memory.

What else could you ask for in an SRAM?

You could ask for separate I/O. Okay. Both chips have separate I/O ports to eliminate bus contention snarls and give you faster throughput. Being able to fly through like that increases performance by 20%.

The Am99C58 also has a chip enable function which automatically powers down the chip when deselected. And that decreases power consumption by over 70%.

The Am99C59 has a scorching 10ns chip select access time which will increase memory system throughput. It's just the thing for cache memory applications.

With the fastest access times around and separate I/O, AMD's Am99C58 or Am99C59 CMOS SRAMs give you the options you need to improve your memory. Fast. And that's worth remembering.

Advanced Micro Devices has broken the game wide open.

After building a comfortable lead with a new product a week, every week—on the shelf, in volume—we called in the heavy hitters:

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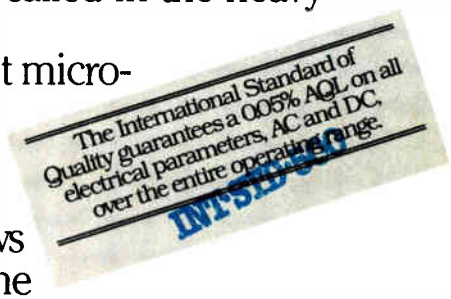


No one who follows the game closely is the least bit surprised. This team puts more dollars into R&D, as a percent of sales, than anyone else in the business.

If you like the sound of extra bases, call Advanced Micro Devices.

**Advanced Micro Devices**

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FYI

*The message is clear; if the U. S. does not act quickly, major production sources for the submicron VLSI chips of the 1990s may all be overseas*

At a time of rising national concern over the sputtering performance of the U. S. semiconductor industry and the outpouring of media attention questioning whether the recent market-regulating agreement with Japan will provide much help to American chip makers (see p. 80), an even more threatening development is emerging that's getting little or no attention. And unless something is done quickly, it could end up badly hurting U. S. chip makers by the mid-1990s.

The U. S. is quickly falling behind the rest of the world in X-ray lithography research. If America is to remain competitive in the production of high-density chips, a coordinated government, university, and industry program must be mounted immediately in X-ray lithography. There's a critical national need for such a program to begin as soon as possible, declares Henry Guckel, director of the University of Wisconsin's Center for X-Ray Lithography. A national program, he points out, must include the construction of a compact storage-ring source, a masking technology, and the necessary exposure systems.

"The window of opportunity for these developments is so narrow as to force an exceedingly tight timetable in order to have practical systems in place by 1991," Guckel says. This is necessary because America's overseas competitors are moving far faster than it is. Unfortunately, any cooperative U. S. effort in X-ray lithography is still in the procrastinating stages. The Americans have held meetings, but they have not yet made any real headway.

By contrast, the West Germans are already deeply involved in an X-ray lithography program, while the Japanese have just made a major commitment to a similar effort. The West German semiconductor industry is now rapidly approaching the hardware stage for all phases of a cooperative X-ray lithography program based on a storage-ring source. In Japan, America's major rival in very large-scale integration technology, a government-sponsored joint-venture company has been set up to build a synchrotron center for use by 13 Japanese electronics companies.

The message is clear. If the U. S. government does not act quickly with both the direction and funding for advanced X-ray lithography, the major production sources for the submicron VLSI chips of the 1990s may all be overseas.

**ROBERT W. HENKEL**

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Our two key ISDN chips are specifically designed to allow complete realization of a full CCITT compatible S-Bus Interface:

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Modularity is designed-in by using IOM (ISDN oriented modular interface) which controls the data flow between the ICC and SBC allowing flexibility to adapt to different transmission configurations in the future.

Just look at these important performance features:

**PEB 2070 ICC:**

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- Serial IOM interface to Level I devices
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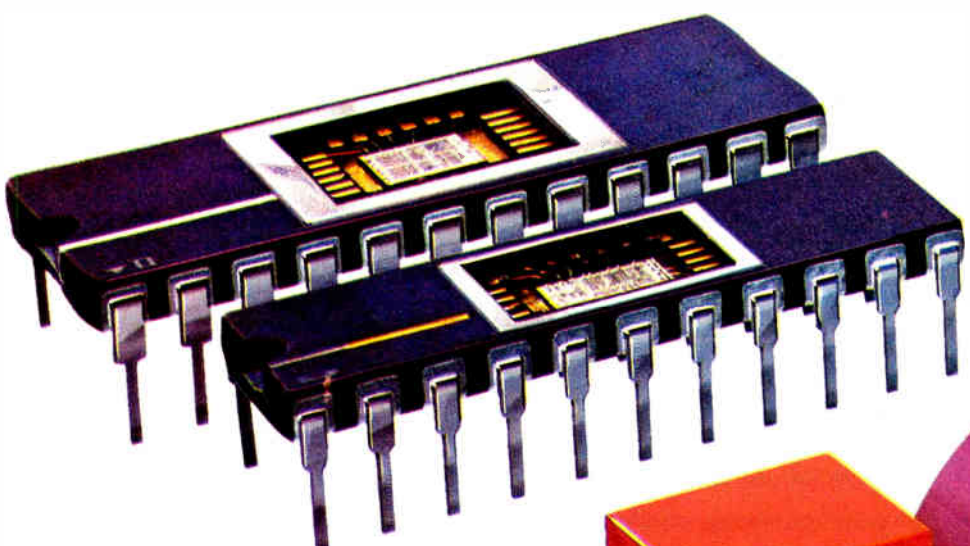

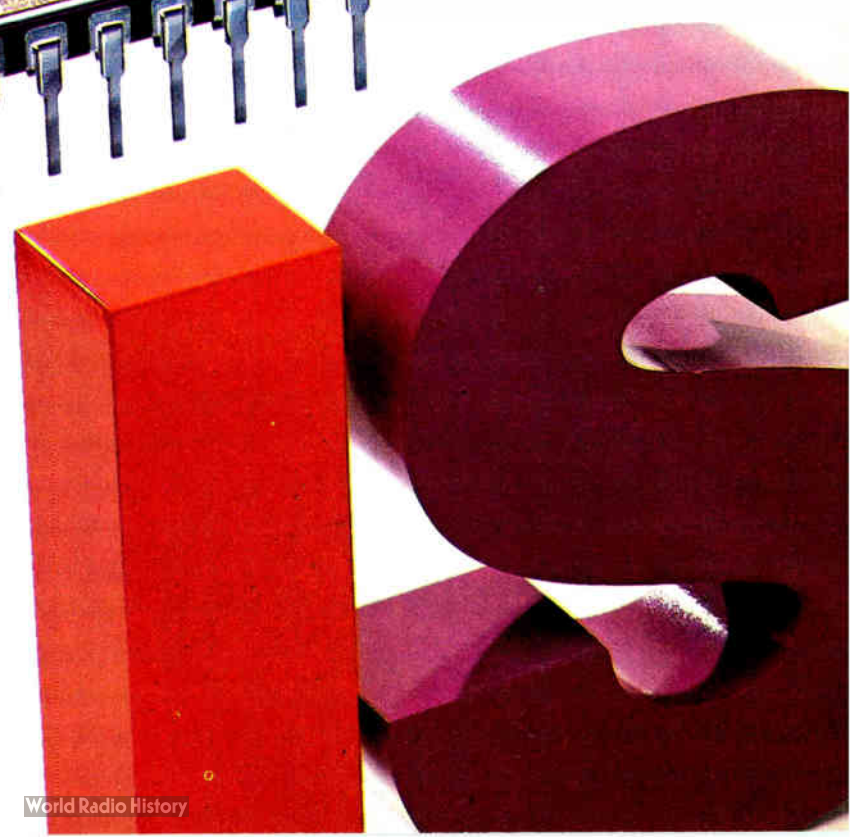

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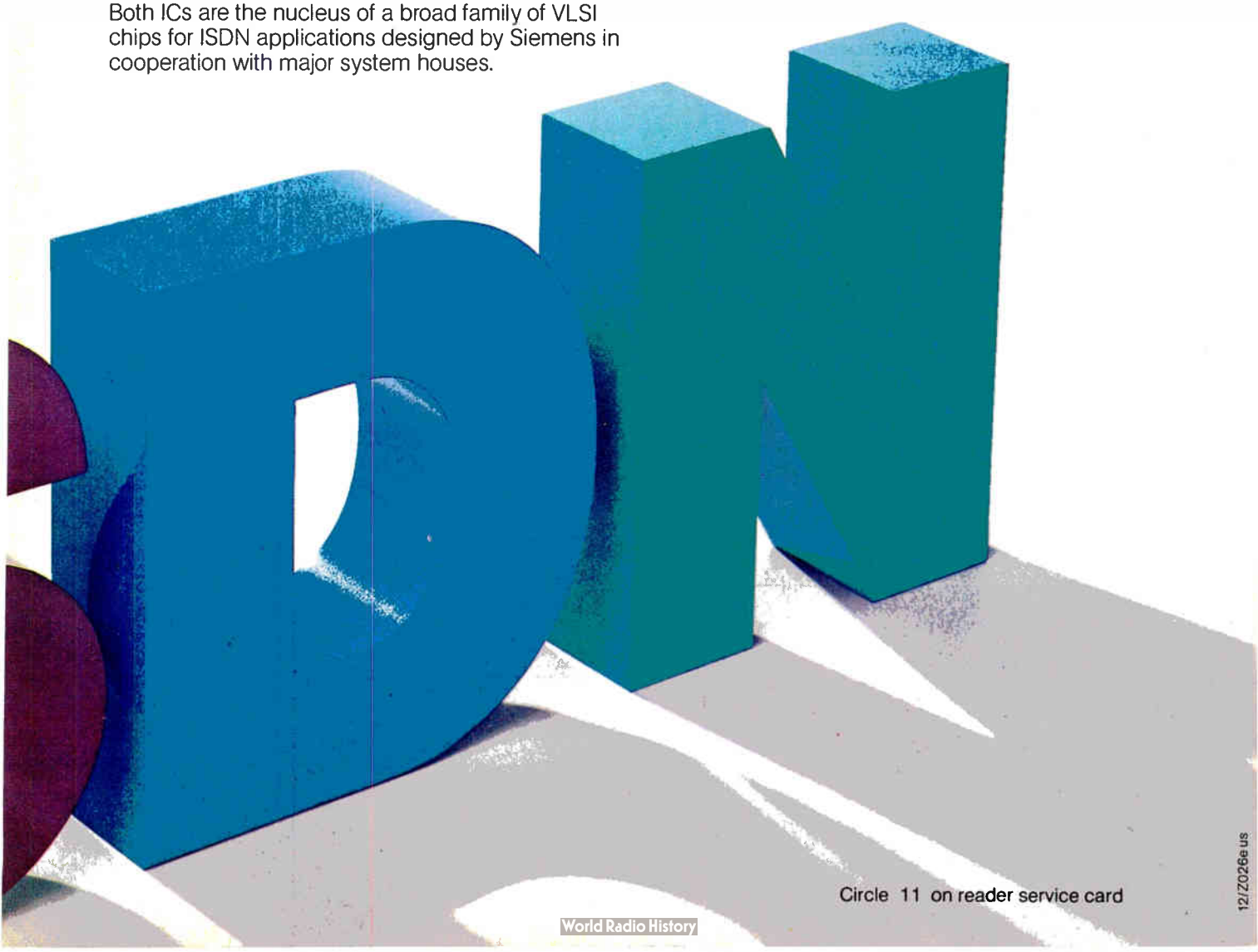



Circle 11 on reader service card

12/Z026e us

## LETTERS

### Don't forget Ciprico

**To the editor:** "Breaking the Speed Barrier on the VMEbus" [*Electronics*, July 10, 1986, p. 58] deals with "breakthrough technology" in the design of a new disk controller from Interphase Corp. It says Interphase's breakthrough was [based in part] in placing a short, high-speed FIFO between controller memory and the VMEbus. Ciprico Inc. has incorporated this [technique] into four products—the Tapemaster 3000 VMEbus tape controller, the Ramfire 3200 VMEbus disk controller, and two similar controllers for Multibus II.

The article makes several references to throughput that seem to equate this term with bus speed. To begin with, over time disk throughput cannot exceed about 85% of the maximum serial data rate if formatted in a typical manner. A 512-byte sector of data requires about 80 to 90 bytes of overhead. For a typical high-speed Storage Module Drive and disk drive, this is about 1.6 megabytes/s for a Fujitsu Eagle, running at 1.89 MHz in a Unix file system. No amount of coaching or increase in bus speed can cause the average throughput to exceed this.

I must also comment on "Multibus II Heads for the Fast Track," on p. 116. Interphase is mentioned as a future Multibus II supplier, while no mention is made of Ciprico. We introduced a disk and a tape controller for Multibus II at this year's National Computer Conference.

*Michael Quealy*
*Vice President, R&D*
*Ciprico Inc.*
*Plymouth, Minn.*

### The fastest in the land?

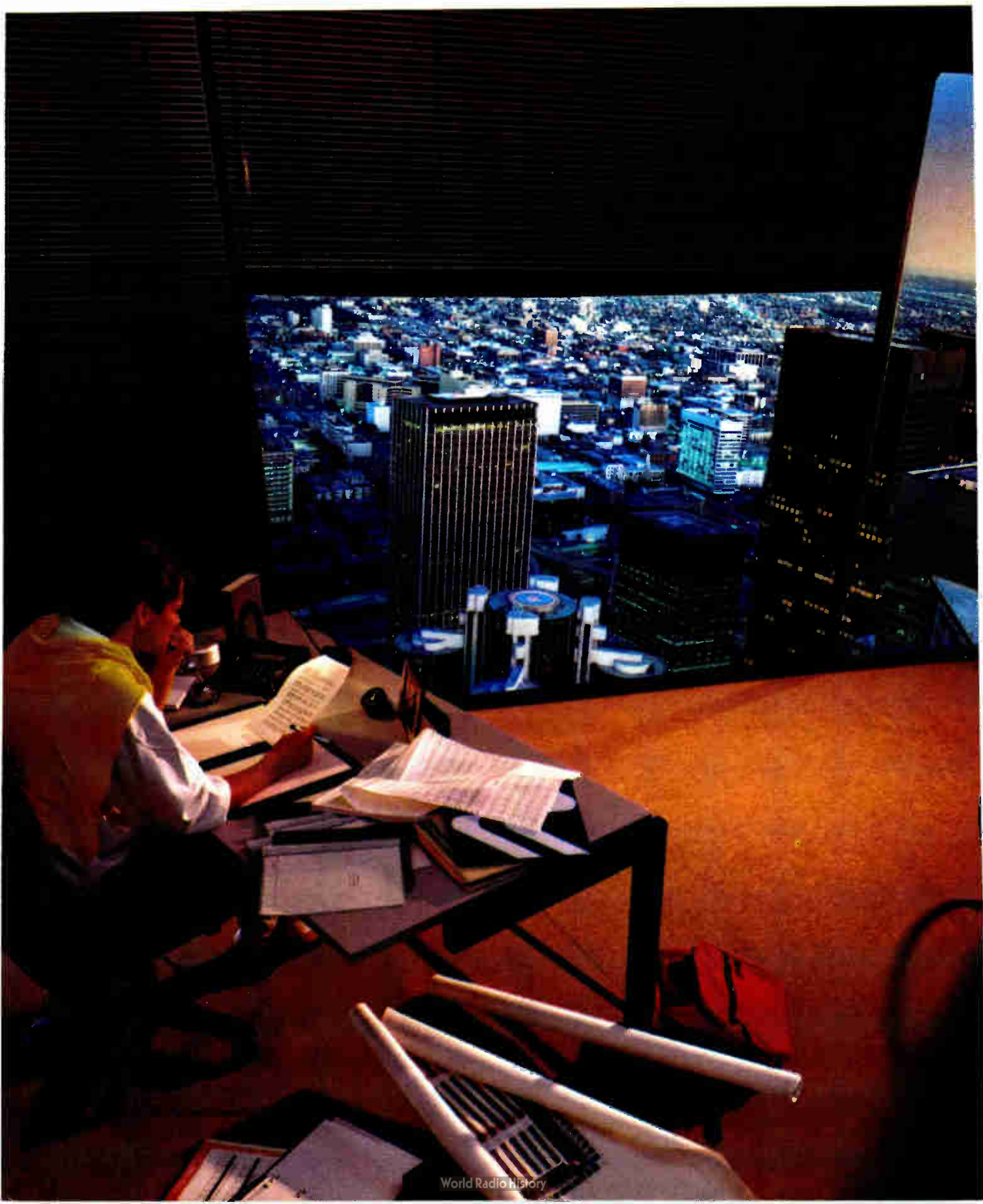
**To the editor:** Vectrix Corp. takes strong exception to statements by Gerald Dwyer of Pixelworks, Hudson, N. H., in "PC-based Graphics Take on Work Stations" [*Electronics*, July 24, 1986, p. 38]. Our complaints are with statements regarding our products. Dwyer is quoted as saying that Vectrix and Number Nine Computer Corp. use "slow, predesigned chips. Their display speed cannot match ours." In fact, the Vectrix PEPE graphics board has two processors designed by Vectrix from discrete components, and while Pixelworks states that the Clipper Graphics Card set draws vectors at 10 million pixels/s, the Vectrix PEPE board draws vectors at almost 20 million pixels/s. And Vectrix has been delivering PEPE since August 1985 at a list price of $2,495—the Clipper set costs $4,500.

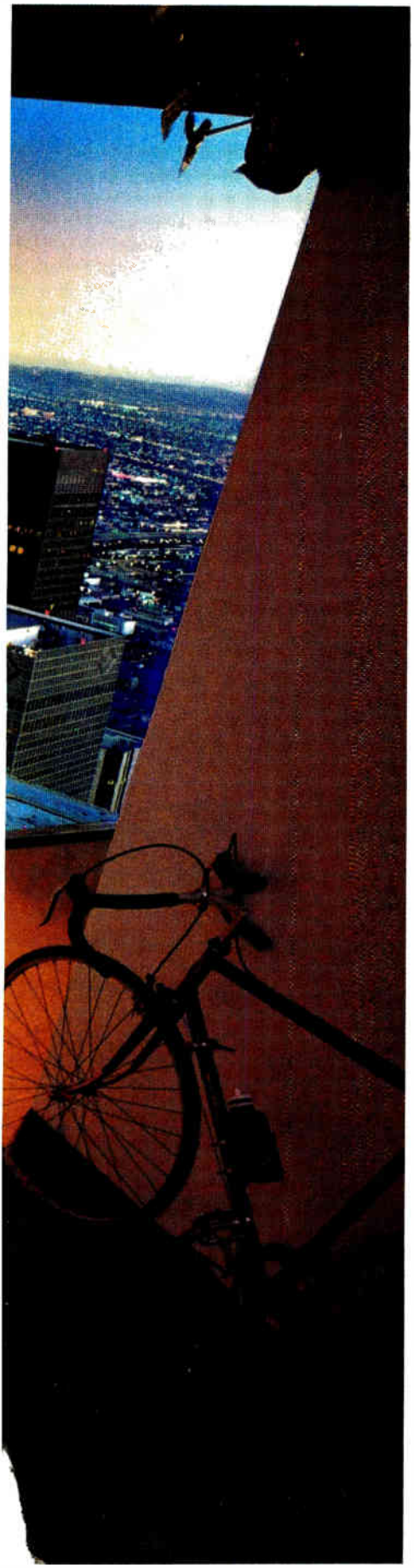
*William D. Waller*
*President*
*Vectrix Corp.*
*Greensboro, N. C.*

# Long hours.
# Late nights.
# Lost weekends.

# Nobody said choosing an ASIC company was going to be easy.

National Semiconductor





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# DIGIDYNE'S MURRAY CAN FINALLY BREATHE EASY

**TUSTIN, CALIF.**

During almost two decades of managing computer operations at a half-dozen companies, Ronald N. Murray has seen his share of the ups and downs of that mercurial business. Now the cycle is turning up again for Murray, who for four years has been president and chief executive officer of tiny Digidyne Corp.

Those have been the toughest years of all for Murray. His job was to hold the Tustin company together while a make-or-break antitrust suit, filed in 1977 against Data General Corp. by Digidyne, Fairchild Semiconductor Corp., and others, slowly worked its way through the federal courts. "I had a tiger by the tail and couldn't let go or we were dead," Murray says.

He can loosen up a bit now, because on July 30 the U.S. District Court in San Francisco granted a permanent injunction favoring Digidyne and Fairchild. (The other companies involved in the suit dropped out in the interim.) The injunction prohibits Data General from bundling its RDOS operating system with its line of small Nova computers. Data General has 60 days to reply to the ruling, and a spokesman at its Westboro, Mass., headquarters says it is studying the details.

Digidyne and Fairchild, which manufactured Nova-compatible machines built around a Fairchild chip set, claimed in their suits that Data General's bundling practice and its refusal to license the RDOS software for Digidyne and Fairchild products violated antitrust laws. Murray maintains that the impact on Digidyne and its customers was devastating, in effect preventing the sale and use of its computers. "We were getting killed every day by this illegal practice," he says.

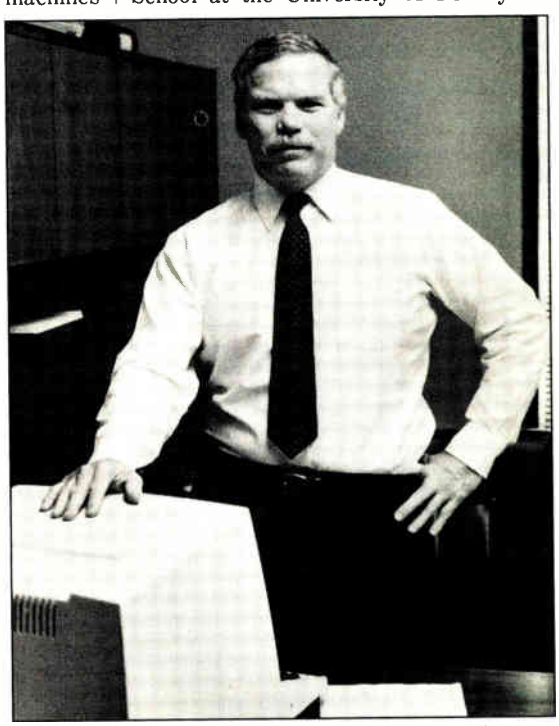
Murray, 43, who is known in the California computer community for his decisiveness and high energy, took on Digidyne's top post in 1982, when the outlook was especially bleak. The company had won the first jury trial on the antitrust issue, but the verdict was set aside by the judge and the much larger Data General began an appeal process that promised to stretch out for years. As a result, sales of Digidyne computers were stopped in their tracks; 1982 marked the company's last year of significant sales, at $3 million.

The owners of the privately held company turned to Murray. "[They] said, 'Here's the problem, tell us what to do,' " the executive recalls. After studying the situation, Murray concluded he could build a company, even one in such deep trouble.

**CHAPTER 11.** But his solutions were drastic. They included curtailing production and, from 1983 to 1985, putting the company under Chapter 11 protection to stave off its creditors while it reorganized. Concurrently, he spearheaded the legal battles. These led all the way to the U.S. Supreme Court, which refused to hear the case and returned it to the lower court.

But, Murray says, "I never considered giving up." Through his efforts, new refinancing was found, creditors satisfied, and design of a new computer line started in expectation of a legal victory. In coming months Digidyne will bring out these models.

Murray has experience in all parts of the computer business. He holds a BSEE from California Polytechnic State University at San Luis Obispo and an MBA in finance from the Wharton School at the University of Pennsylva-



**MURRAY:** His drastic solutions—production cuts, Chapter 11—to Digidyne's critical problems could be working.

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nia. Before joining Digidyne he was director of minicomputer operations for Sperry Systems, Irvine, Calif. Before that he served as director of commercial systems for Zilog, vice president for direct sales at Microdata, and director of sales for General Automation.

But Murray says that nothing in his background could have prepared him for the unrelenting legal and business problems of the last four years. "Maybe only fighting muggers in the alley could do that," he remarks.

Still, Murray sees the court decision as a landmark for the industry, as well as for his company, in that "it permanently separates hardware and software." Digidyne and Fairchild are now preparing for a trial, which is to start early next year, to set damages for the antitrust violation. The companies will ask for a total of $100 million, a sum that if affirmed by a jury would triple under antitrust law. *–Larry Waller*

# NARGI DELEGATES SO HE CAN GET HIS HANDS DIRTY

**WAYNESBORO, VA.**

Michael L. Nargi Jr. has found that he who manages least manages best. His aim as the new senior vice president for operations at Genicom Corp. is to "delegate authority to the lowest possible level" and make sure everyone does his or her job. Nargi, 43, joins the Waynesboro maker of printers and electromechanical relays for aerospace, defense, and transportation determined to "let people implement their own ideas without my intervention—it's their job and their responsibility."

The immediate challenge will be to apply that philosophy to more employees—1,100 people—than at his last job. As executive vice president and chief operating officer of Tecmar Inc., a manufacturer of personal computer add-ons and software in Cleveland, he commanded 400 people. "But it really is no problem going from 400 to 1,100," he maintains, "if the organizational structure below you is very strong." The goal, he says, is to "try and identify who I see as having potential to move up in the company."

**NIGHT SCHOOL GRAD.** That attitude would seem to fit Nargi, a native of Stamford, Conn., and a man who chose to work while he learned. He holds a BS in electrical engineering from Bridgeport (Conn.) Engineering Institute, which offers its programs after working hours, and a master's in business policy from Columbia University's Master's Degree Program for Executives.

He attended the institute while working at his first job, as an assistant engineer for Raytheon Co., where he eventually became a production engineer. Nargi moved on to the Norden Division of United Technologies Inc. in Norwalk, Conn., where he became lead engineer of the division.

In 1981 he went to a maker of office systems, Pitney Bowes Inc. of Stamford, where he became director of manufacturing for business systems. It was while he was at Pitney Bowes that he

**NARGI:** "I like to get down into the designing nitty-gritty and get my hands dirty."

was chosen for the one-year Columbia program, which consists of classes one day a week plus 20 hours of work to take home.

Nargi became Pitney Bowes's director of manufacturing for business systems, in charge of five divisions of the company. "The technology we use [at Genicom] working with printers and putting them together is quite similar to the kind of technology that I saw at Pitney Bowes," he says.

**NITTY-GRITTY.** That's fine with Nargi, who sees himself as more than just a delegator of authority. "I like to get down into the designing nitty-gritty and get my hands dirty," he says. So he anticipates using his engineering experience at Genicom by helping with production design.

He also looks forward to the upcoming Autofact '86 show in November in Detroit. It is a return to the scene of one of the highlights of Nargi's career, the presentation of a paper in 1983, "Computer Technology: Backbone of Electronic Assembly." *–David Rubinger*


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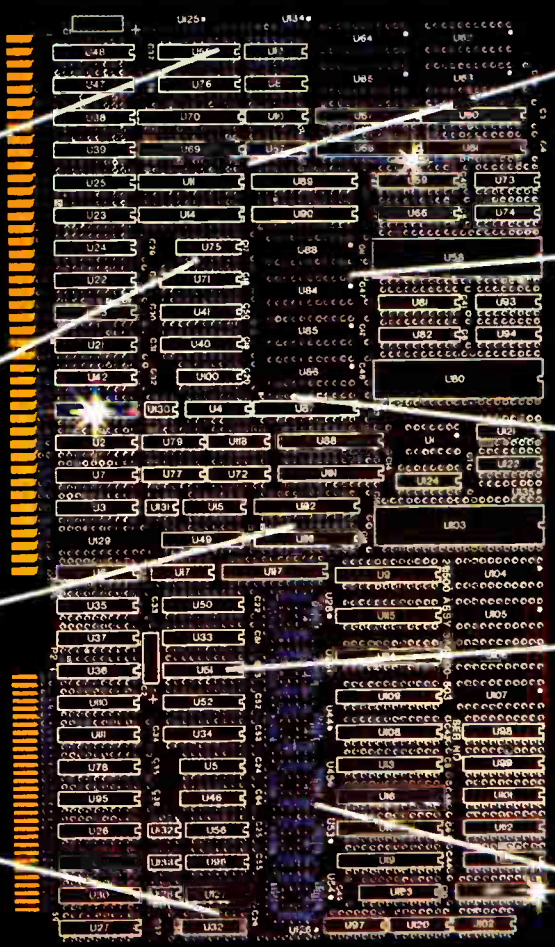

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# ELECTRONICS NEWSLETTER

## TRANSPUTER COMPUTER SYSTEM BLAZES AT 3,000 MIPS

Add Meiko Ltd. to the list of makers of world-class computers. The Bristol, England, company turned up at this week's Siggraph '86 conference in Dallas with a 311-transputer version of its Computing Surface that can carry out upward of 3,000 million instructions per second. Meiko believes the $850,000 machine is the most powerful multiprocessor now on the market, and to impress the graphics experts at Dallas the company set up the system for ray tracing—at a rate of 8.5 million ray intersections in 47 seconds. Meiko builds its multiprocessors [*Electronics*, Oct. 7, 1985, p. 43] around 32-bit transputers from Inmos Corp. A Digital Equipment Corp. MicroVAX host computer acts as a file server for the 311 transputer machine. □

## CONVERGENT CUTS WORK FORCE AND REGROUPS

Troubled computer maker Convergent Technologies is hoping that a sharply reduced work force and a new corporate structure can help end the sales slide caused by loss of business from its biggest customer, AT&T. The Santa Clara, Calif., company last week laid off 500 of its 1,900 employees, although it will triple its sales force to over 100. It also spun off several newly acquired vertical businesses into a subsidiary, Convergent Small Business Services, which will build turnkey systems in selected markets. The initial components of the subsidiary are Baron Data Systems, Display Data Corp., and two business units it plans to acquire from the Uccel Corp. of Dallas. Convergent itself will continue to sell to OEMs and value-added resellers. It plans to offer this year several new products based on the Intel Corp. 32-bit 80386 microprocessor. After a barely profitable 1985, in which $157 million of its $395 million sales were to AT&T, Convergent has suffered two dismal quarters as AT&T severely restricted its purchases of the company's Unix-based work station. □

## IBM BACKS THREE-YEAR AI STUDY AT CARNEGIE-MELLON

In a move that could have far-reaching influence in the marriage of artificial intelligence and manufacturing automation, IBM Corp. last week launched a three-year AI study with Carnegie-Mellon University in Pittsburgh. The university will receive 225 IBM RT Personal Computers valued at $5.5 million, a machine particularly well suited for both AI and factory automation because it has the PC bus and thus can accommodate the many controller boards available for this market. Under the project, announced at the National Conference on Artificial Intelligence in Philadelphia, CMU will port its system-development tools to the RT PCs and then explore ways to make computers more productive in a wide range of areas, from insurance to manufacturing. □

## MOTOROLA TO MOUNT NEW ASSAULT ON DIALER-CHIP MARKET

Can telephone dialer chips still ring up profits for U. S. silicon houses? Executives at Motorola Inc. think so, and they are planning to introduce the company's first new dialer chips since the late 1970s, when aggressive pricing competition from Asia weakened profits for domestic suppliers. Motorola's MOS telecommunications operation in Austin, Texas, will unveil next month a family of four silicon-gate CMOS dialers, including chips with last-number redial and onboard memory for nine 18-digit phone numbers. Many of Motorola's renewed efforts in high-volume dialers are aimed at grabbing market share from cross-state rival Thomson Components-Mostek Corp. Motorola executives privately suggest that the Carrollton company—still a U. S. powerhouse in dialers—has become vulnerable to new domestic competition. □

# ELECTRONICS NEWSLETTER

## TI TRIES TO HEAD OFF FAIRCHILD WITH FAST-EQUIVALENT BIPOLAR LOGIC

If you can't beat 'em with existing system designs, join 'em and grab market share. That's what Texas Instruments Inc. hopes to do with a new F series of bipolar logic that's equivalent to FAST—Fairchild Advanced Schottky TTL—from arch rival Fairchild Semiconductor Corp. For nearly five years, TI has competed against FAST with two series of its own: the faster Advanced Schottky and the slightly slower advanced low-power Schottky. But, say TI executives in Sherman, Texas, Fairchild came to market with FAST 18 months before TI did with AS in 1982-83. As a result, Fairchild chips became firmly fixed in many customer's systems. So, to catch up, TI now plans to offer 70 SSI and MSI parts in the F series by year's end. Eight are available now, ranging from dual flip-flops to an octal bus transceiver priced between 36¢ and $4.50 each in 100-piece quantities. TI says it will continue to promote AS and ALS for new equipment designs and for complex functions. The F series brings TI's bipolar logic offerings to six, including TTL, Schottky, low-power Schottky, AS, and ALS. □

## WHITE HOUSE NAMES NEW CZAR FOR PENTAGON ACQUISITION

One of the Packard Commission's key recommendations on defense management, the creation of a top-level Pentagon position for supervision of military procurement, has been quietly set in motion. The White House has picked Richard P. Godwin, 64, a longtime executive with San Francisco's Bechtel Corp., for under secretary of defense for acquisition. If confirmed, he will set policy for procurement and research and development, supervise the performance of the entire acquisition process, and establish policy for administrative oversight and auditing of defense contractors. The Senate Armed Services Committee plans confirmation hearings Sept. 11. □

## ASIC DESIGN CENTERS WILL WORK WITH MOTOROLA'S SMALLER CUSTOMERS

In an attempt to gain a step on its competitors in the application-specific IC business, Motorola Semiconductor Products Sector's ASIC Division has signed up four outside design firms. Motorola believes that the four, using Motorola's cell libraries and computer-aided-design tools and working directly with customers, can serve smaller ASIC buyers better than Motorola itself. The centers—Custom Silicon Inc. in Boston; Electronic Technology Corp., Cedar Rapids, Iowa; Integrated Silicon System Inc., Raleigh, N. C.; and Texas Arrays Inc. in Dallas—will be under contract to the Phoenix-based division, which will also operate its own center, Pico Design in Santa Clara, Calif. Motorola also has signed distribution agreements with Hall-Mark, Hamilton/Avnet, and Schweber to complement the design centers. □

## ELECTRONICS TRADE DEFICIT CONTINUES TO CLIMB

The U. S. electronics trade deficit is continuing to soar, and last year it increased more than 40% from 1984 levels, says the American Electronics Association. The AEA, using Census Bureau data, says the $20.7 billion worth of electronics products and services that Japan alone exported to the U. S. in 1985 was more than the combined total U. S. sales to the top seven countries importing products from America. And the U. S. had significant electronics trade surpluses with only five of these countries: Australia, Canada, France, the Netherlands, and the UK. Those surpluses totaled $7.8 billion; but the deficit with Japan was $17.6 billion. U. S. electronics-industry exports totaled $35.6 billion, and imports were $44.4 billion. Canada was the biggest importer of U. S. electronics at $4.9 billion, and the biggest U. S. trade surplus was $2.4 billion with the UK. □

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| IMS2801-80 | | 43ns | 13ns | 46ns |
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| DT2821-F 12-bit, High Speed | 1995 | 16SE/8DI | 12 | 130 | 2 | 12 | 130 | 16 | Yes |
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# PRODUCTS NEWSLETTER

## DEC WORK STATION CAN COMBINE AI AND CONVENTIONAL PROGRAMS...

Digital Equipment Corp.'s new high-end artificial-intelligence color work station lets users develop applications that combine AI with conventional programs. Based on the company's general-purpose MicroVAX II computer, the AI VAXstation/GPX (for graphics extension) was introduced at the National Conference on Artificial Intelligence in Philadelphia last week. It comes in two versions, one supporting the Ultrix-32 operating system, the second supporting the MicroVMS operating system. Both are priced at $63,395. Each consists of a MicroVAX II central processor with 16 megabytes of memory, a 5¼-in. Winchester disk drive, and a 95-megabyte streaming-tape cartridge system. The VAXstation/GPX also has an Ethernet interface, a 19-in. color monitor, the VAX version of the Lisp language, and graphics software. The Ultrix-32 version comes with a window manager and the MicroVMS version offers user-interface services. Both will be available in late September. □

## ...AS TI's EXPLORER IS BEEFED UP TO HANDLE SIMILAR JOBS

Texas Instruments Inc. will make available a Unix processor board that expands the scope of the Dallas company's Explorer artificial-intelligence work station. Introduced last week at the Philadelphia AI conference, the card links 68020 and Lisp processors in the same computing environment to create the Explorer LX. The board is designed for applications that require both knowledge-based programs written in Lisp and numeric-computation programs written in C, Fortran, or Pascal—a type of integrated programming that's growing in popularity. The basic LX configuration, priced at $73,900, comes with 4 megabytes of memory, two 182-megabyte disk drives, and a cartridge tape drive; as an upgrade for existing Explorer systems, the card alone is $18,500. Delivery will begin in December. □

## IRWIN UNVEILS COMPACT TAPE DRIVE TO BACK UP WINCHESTER DRIVES

Next month, Irwin Magnetic Systems Inc. will introduce a peripheral tape drive only one fifth the size of its current external backup drives. The Ann Arbor, Mich., company's 400 series is intended for backing up personal-computer Winchester disk drives. The 400 series measures 4¾ in. high by 2 in. wide by 7½ in. deep and is based on technology developed for Irwin's internal tape drives, which fit the form factor for a 3½-in.-drive. The new unit will be sold to original equipment manufacturers as well as to retailers. OEM pricing is unavailable, but suggested retail prices will range from $799 to $1,095 for 10- and 40-megabyte systems respectively. □

## 50-MHZ TESTER CHECKS OUT ASICS ON THE FLY

Most test systems used to characterize application-specific, very large-scale ICs at 50-MHz test rates are combinations of a logic analyzer and a pattern generator. The drawback to such setups is that they can't perform real-time comparison of expected versus actual response from a device under test. Now comes the Topaz 50 from HiLevel Technology Inc. The Irvine, Calif., company's system provides such comparisons on the fly at 50 MHz. It requires no cabling to the device under test and can employ up to 512 pins to test an ASIC. The system is equipped with programmable drivers and receivers on each pin, so it controls the placement of a waveform and its rising and falling edges with a resolution of 500 ps. Pin drivers allow programming of both output high and output low over a range of –3 to +7 V, with a maximum swing of 7 V. The drivers provide 30 mA of drive current on each pin and may be operated with ECL or CMOS impedance values. Available now, the Topaz 50 is priced starting at $25,000. □

# PRODUCTS NEWSLETTER

## AN INTEGRATED PROGRAM FOR MACINTOSH IS COMING FROM MICROSOFT...

Taking advantage of the graphics features of the Apple Computer Inc. Macintosh, Microsoft Corp.'s integrated program Microsoft Works lets users draw lines, boxes, and circles around or on top of text. The Redmond, Wash., company's package, which sells for $295 and will be available next month, includes a 256-column by 9,999-row spreadsheet, a modem-communications package, a word processor, and a data base that supports 60 fields per form. The word processor has form-letter capability, automatic pagination, and a copy-format option that allows paragraph formatting to be repeated from one paragraph to another. □

## ...WHILE ASHTON-TATE ADAPTS dBASE FOR THE MACINTOSH

Ashton-Tate has adapted its dBASE relational data-base system to the Apple Macintosh in dBASE Mac, which uses the machine's mouse-based point-and-click interface and its pull-down menus. The Torrance, Calif., company's system enables users to link as many as 36 data files by using the mouse to drag a key field from one file to another. dBASE Mac can access IBM-compatible dBASE data files directly through ASCII text files. It works on a Macintosh with 512-K bytes of memory or a Macintosh Plus with at least one 800-K-byte disk drive. It is priced at $495 and will be available in the fourth quarter. □

## MOTOROLA ADDS DEVELOPMENT SUPPORT FOR ITS SIGNAL PROCESSOR

Motorola Inc. is adding versions of its development software for the 56000 digital signal processor for two multiuser computers: the 68020-based work stations from Sun Microsystems Inc. and the VAX computer line from Digital Equipment Corp. On both computers, the $3,000 DSP package runs under AT&T Co.'s Unix operating system with the University of California at Berkeley's 4.2 extensions. It also runs under DEC's VMS operating system. A new 1.1 version of the original development system is being offered for IBM Corp. Personal Computers at $295. All are available now. □

## A LOWER-COST PACKAGE FOR THE HEXFET LINE OF POWER MOS FETs

International Rectifier is providing a less-expensive plastic package for all voltage ranges of its Hexfet line of power MOS FETs. The plastic package, which replaces the metal TO-3 cans, can work in nonhermetic environments and makes for easier installation in printed-circuit boards. It accommodates the El Segundo, Calif., company's large HEX-4 (5.77 by 4.32 mm) and HEX-5 (6.53 by 6.53 mm) die sizes for high-current handling. Rated reverse voltages are 60, 100, 150, 200, 350, 400, 450, and 500 V. Price per 1,000 pieces ranges from $4.90 for the IRFP143 to $13.43 for the IRFP450. The prices are 15% to 20% lower than those of the metal TO-3 cans the plastic parts replace. □

## ITT CANNON ADAPTS D-SUBMINIATURE CONNECTOR TO SURFACE MOUNTING

ITT Cannon is offering a new version of its standard D-Subminiature connector incorporating several changes to accommodate surface-mounting applications. The connector provides flexible contacts to compensate for circuit-board and solder-pad irregularities and warpage. A 90° front metal shell can be mated with all existing D-Subminiature connectors with 9, 15, 19, or 25 pins. The connector is made of high-temperature plastic insulator material that can withstand vapor-phase soldering (215°C for 45 seconds). Prices range from $2.08 for the 9-pin version to $3.70 for the 25-pin connector. □

# Digitization Enhances Oscilloscope Capabilities.

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Electronics

# AUTOMATION INDUSTRY FACES A SHRINKING MARKET

## TOUGH TIMES FORESEEN AS GENERAL MOTORS CUTS BACK ORDERS

**BOSTON**

General Motors Corp. has sneezed—and the fledgling manufacturing automation industry is feeling the blast. The automaker is pulling back from its previously aggressive automation program, and this is rocking an industry that at best was only staggering toward profitability.

The retrenching at GM is expected to affect virtually all the players in the industry. Companies that are closely tied to automakers will be hit hardest, but those whose main business comes from other industries will be affected in the long term.

The most prominent victim to date is GMFanuc Robotics Corp., Troy, Mich. After losing $88 million in GM business it had expected to ship in 1986 and 1987, the company announced this month that it intends to cut back its work force by one third by the end of the year. GMFanuc is a joint venture of GM and Fanuc Ltd. of Japan.

Smaller companies are also being pinched. Order cancellations at Automatix Inc. in Billerica, Mass., recently forced it to lay off 20% of its workers. Itran Corp. in Manchester, N. H., reports its orders are softening. Robotic Vision Systems Inc. in Hauppauge, N. Y., says it lost a major contract with GM, and Diffracto Ltd., Windsor, Ont., and Applied Intelligent Systems in Ann Arbor, Mich., both report order cancellations.

Subsystem companies have also taken blows. "We've certainly seen our customers who build systems for other people impacted," says Stephen Silver, president of Imaging Technology Inc., Woburn, Mass.

Some companies report no impact from GM's pullback yet, but many are concerned nonetheless. "I'm not gleeful when I hear competitors are losing significant orders," says Robert Shilman, president of Cognex Corp., Needham, Mass. "When the orders are disappearing, it's not good for anyone."

Eric Mittelstadt, president and chief executive officer of GMFanuc, believes the shakeout has begun and says "it's perfectly natural" for an infant industry. Laura Conigliaro, who watches the industry for Prudential Bache Securities Inc., New York, adds "You're not dealing with companies in resoundingly strong shape.... Near-term and intermediate, it will probably be very rough going."

**ROCKY FUTURE.** A number of companies almost certainly will go out of business. In the machine-vision segment of the industry, for example, some 100 companies are chasing business that will be worth about $180 million this year, says Walter Pastorious, vice president of marketing at Diffracto. Steve Marco, executive vice president and chief operating officer at Itran, goes further: "By Jan. 1, 1987, there will be only four or five pure vision companies that are in any position to do business for 1987."

The loss of big auto-industry orders will also retard the development of technology. "What we need are projects and innovation and dollars for product development," says Tom Reynolds, director of product marketing at Automatix.

The need for technological progress is underscored by the reasons for GM's pullback: apparently, automation turned out to be a lot more difficult than the automaker expected. Though GM will say only that "our plans on the rate of implementation are not as aggressive as they once were," other sources say the company took on too much, too soon. "GM greatly underestimated the amount of red ink, time, and persistence required to make automation systems work," says one executive whose company has worked closely with GM.

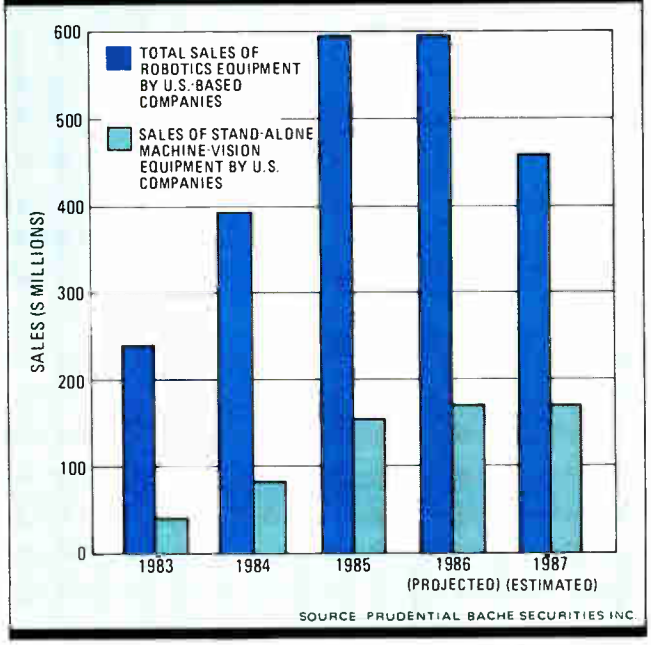
"Clearly, projects have not come up as fast as anyone would have liked," says Pat Costa, president of Robotic Vision Systems and chairman of the Automated Vision Association, an industry trade group. The result has been a technology backlash. "Two years ago, technology was the answer to all problems," says Costa. "Now people are saying the problem is too much technology. What we're seeing now is a learning period—and the tuition can be high."

Moreover, those systems that have been implemented have not paid off as well expected. The cost differential between U. S. and Japanese manufacturers does not appear to be reduced by automation, according to Conigliaro.

Disappointment with the systems themselves is not the only factor in GM's pullback. Sluggish markets and a general cutback in capital spending also played a part. The bulk of these cutbacks are in the area of $1-million-plus contracts for new ventures. Less-expensive projects have not been hit as hard—the market for retrofitting production lines with equipment costing $150,000 to $400,000 has remained fairly steady, reports Michael Schuh, vice president of marketing at Automatix.

Some companies may stave off the brunt of the automotive cutback because of their

GROWTH STALLS IN U.S. ROBOTICS INDUSTRY



concentration on other markets. One industry study projects that the electronics industry, for example, will become the dominant buyer of machine-vision equipment by 1990.

The electronics industry typically requires less system integration than automobile manufacture. It also holds greater potential for general-purpose, transferrable applications, says Donald Vuchetich, director of marketing at Applied Intelligent Systems. Still, the electronics industry is far from healthy.

Increased original-equipment-manufacturer sales could help automation vendors. Pastorious, at Diffracto, says an OEM strategy "allows you to pursue a broader variety of applications without ending up with an unwieldy applications engineering staff." But Mittelstadt says the OEM business, which accounts for about 50% of GMF Robotics' sales, may surprise newcomers. "We've spent a heck of a lot of resources supporting [customers] even when it was OEM business."

Guesses vary as to how long GM will hold back on its automation programs. Robotic Vision's Costa thinks the dry spell could end by next summer and shouldn't last longer than 18 months in any case. Mittelstadt talks about a two- to three-year slowdown. Others say it's impossible to tell. They think the business will boom only when the technology becomes transparent to the end user—and reaching that point, says Costa, will require far greater cooperation between vendors and customers. *–Craig D. Rose and Wesley R. Iversen*

*ARTIFICIAL INTELLIGENCE*

# IBM FINALLY JUMPS INTO AI WITH BOTH FEET

**NEW YORK**

IBM Corp. is suddenly making it clear that artificial-intelligence technology is high on its list of development activities, after years of showing little interest in the subject. "We are going into the commercial arena [with AI technology] in full force with a lot of investment," says Herbert Schorr, group director of products and technology for the Armonk, N. Y., company's Information Systems and Storage Group.

Schorr outlined IBM's four-pronged strategy for AI. It involves applications for internal use, product development, the establishment of marketing-support centers for AI products—the first one opens next month—and joint research projects with academic partners such as Carnegie Mellon University in Pittsburgh (see story, p.21). He also covered the strategy in the keynote address to the American Association for Artificial Intelligence's fifth annual conference in Philadelphia last week.

"We have seen too many people try to implement too many difficult applications with standard technology and have to give up; we need [knowledge-system] technology now," says Schorr. That technology is ready to be applied, he says. It should soon begin to yield a whole new class of applications for a new class of users.

Old hands in AI research applauded loudly at the news. "To see the world's major computer manufacturer take this position is a great victory," beamed Edward Feigenbaum, an expert-systems pioneer who is now a professor at Stanford University. Nils Nilsson, chairman of the computer science department at Stanford, agreed. "Most of us know that IBM Corp. has not been in the forefront of artificial intelligence. They haven't even used the term much. It's a significant event to see a large corporation say the technology is ready."

Schorr, who says he has been called the AI champion at IBM, heads a corporate project office that oversees the development, marketing, and internal use of AI products and applications. "We didn't want to make [the project office] into an independent business unit like the one that developed the PC, because our efforts permeate the organization," he says. "However, my role is to get the effect of an IBU in coordinating strategies and cutting all the red tape."

**SCHORR:** IBM is commercializing AI "with a lot of investment," says the head of its AI project office.

Applications for internal use represent the first leg of IBM's strategy. Work on more than 70 such applications is now under way, by Schorr's count. They encompass all areas of IBM's business. "We see knowledge systems helping us become more efficient," he says.

"We are systematically and thoroughly searching all facets of our business for the high-payoff applications and to choose those to do immediately that produce a quick return on investment. Since we want to be the low-cost producer, we are searching for all opportunities where knowledge systems will help us do this," he adds.

The second element of the strategy is IBM's AI product-development program. Besides its own versions of Lisp and Prolog languages and an expert-system development environment for the System 370 mainframe computers, IBM has encouraged third-party software houses to provide versions of their expert-system development tools on its Personal Computer and RT PC.

**MORE COMING.** Furthermore, Schorr indicates that much more AI product development is under way inside the company. Teams in Santa Theresa and Menlo Park, Calif., and in Gaithersburg, Md., are developing both tools and applications, he says. "We will have a bigger set of products and we will integrate them with mainframe data-processing systems—in fact, we are working on a family of products compatible across our PC, RT, System 36, and System 38, through the 370 products; that's our goal," he says.

Schorr emphasizes that integration of AI technology into conventional applications is the key to making AI commercially valuable. For example, both software vendors and computer companies need to develop ways to combine knowledge systems with data bases and communications software, he says.

"The key problem will be systems integration, more key perhaps than the AI stuff. A little AI goes a long way," he says. "New tools to make the link between knowledge systems and conventional programs are needed. And they must be seamless. They are really not here yet."

The third segment of IBM's strategy is marketing. Schorr's project office has been working on internal applications and products for a year. On Sept. 15, the company will open its first facility to help customers deploy AI applications, an AI marketing-support center in Cambridge, Mass. A second center will open on the West Coast, but the company is not ready to say when.

The fourth part of IBM's strategy carries forward a series of joint AI research projects with universities. The biggest such project yet was announced at the AAAI conference—a broad program of porting tools to the RT PC and other research at Carnegie Mellon University.

*–Tom Manuel and Alexander Wolfe*

# AMD TRIMS SAILS AS SLUMP HITS HOME

**SUNNYVALE, CALIF.**

The semiconductor slump just will not go away. Last week the published book-to-bill ratio slipped below 1, and at Advanced Micro Devices Inc., the no-layoff policy that made it unique among chip makers became as extinct as the four-layer diode.

Faced with a prospect of flat sales after a disastrous first quarter in which it lost $27.9 million on revenue of $153.9 million, AMD laid off 200 recently hired workers and said that more layoffs will probably follow in October, once second-quarter results have been analyzed.

In addition, AMD decided to cut back sharply on research and development spending, which had amounted to a whopping 32% of sales. The Sunnyvale company abandoned its tiny but process-driving dynamic random-access-memory work and indicated it will eliminate selected other R&D projects. Savings will probably amount to about $10 million per quarter, although the timing for the cutback has not been settled.

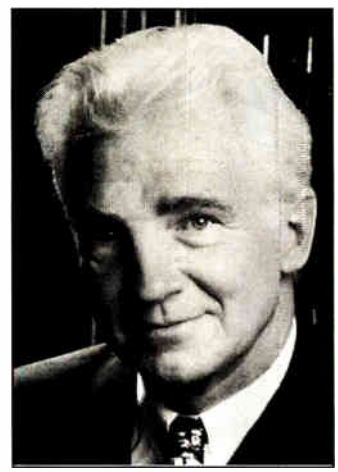
AMD president W. J. Sanders III had clung to the no-layoff policy through several semiconductor recessions, making employees the envy of an industry where employment generally tracks profit margins. Few analysts, however, thought Sanders could continue to hold out in the face of the current decline, the worst in industry history, and many had criticized him for failing to take the step earlier.

**FIRST, ATTRITION.** Before last week's layoffs, AMD had 13,800 employees—down, due to attrition, from a peak of 15,299 in June 1985. The initial cutbacks are not considered a break in the no-layoff policy, because the employees affected had been with the company less than a year and are not covered by it. AMD would not estimate how many employees it will lay off in October, but outside analysts estimated that layoffs might total 500 to 1,000.

Sanders had been among the first to predict the semiconductor slump, in the fall of 1984, even as AMD was on its way to a record-breaking year in fiscal 1985, when it had profits of $135.4 million on sales of $931.1 million. But he couldn't prevent the slide to $576.1 million in sales in fiscal 1986, when the company lost $36.6 million.

AMD tried a variety of cost-cutting maneuvers last year, including a pair of two-week shutdowns, a period of four-day work weeks, and 10% pay cuts for all employees. However, it put a stop to these moves in January, even as it was attempting to produce its way out of the recession by introducing a product a week.

Sanders blamed fierce Far Eastern competition for forcing his company to go to layoffs. "The onslaught of Asian competitors, their massive over-investment and attendant excess capacity, has irrevocably changed the semiconductor industry," he says. "Our world has changed and to survive we too must change."



**SANDERS:** Due to Asian competition, "our world has changed and we too must change."

Much of AMD's losses were due to price erosion in erasable programmable read-only memories, which account for 15% to 20% of the company's business. Ironically, the layoff announcement came only a week after the U. S. and Japan agreed to a price structure for imported EPROMs (see p. 79). That was too late for AMD, though, because it was already committed to long-range EPROM contracts with some major customers.

The layoff announcement also came on the same day that the Semiconductor Industry Association announced that the book-to-bill ratio for the U. S. market had dipped to 0.97, the first time it had gone below 1 since last December.

The SIA has given up predicting any significant upturn this year. And In-Stat Inc., the Scottsdale, Ariz., research firm, has cut its already pessimistic estimate of industry growth from 3.7% to 2.9% for 1986. "There is no new business out there to get excited about," says In-Stat's William Groves.

Most analysts agree that AMD had to act. "You can't continue to take $25 million quarterly losses and survive," says Adam Cuhney of Kidder Peabody & Co., San Francisco.

"Sanders made a big bet and lost," says Michael Murphy, publisher of the *California Technology Stock Letter*. "He tried to run the company Japanese-style and not cut back at the first sign of trouble. He built a hell of a reputation in the Valley."

AMD was able to introduce one new product a week since last September, "and the market turned up," says Murphy. "But it didn't keep going. They were hemorrhaging too much to continue with no layoffs."

Cuhney, however, argues that AMD's R&D policy was not paying off. "They were spending more than their in-house capacity could absorb in production," he says. "Their R&D efficiency was low. Intel Corp. spent $195 million on R&D in 1985 for 80 new products; AMD will spend an equal amount through September of this year and come out with 63 new products." *–Clifford Barney*



# STANDARD IS SPARKING NEW GRAPHICS PRODUCTS

**DALLAS**

A world where computers pass images to each other freely—regardless of boundaries between nations, hardware, and software environments—may soon be possible, thanks to the Computer Graphics Metafile. A barely visible but nonetheless weighty industry specification, CGM is sparking a number of new products, and it is said to be an important sign of the direction being taken by the slowly developing but more comprehensive graphics standards.

A metafile is a file meant to be translated before it is used. In the case of CGM, the metafile is a standard-format picture description that cannot be displayed as an image until it has been translated into a graphics file in a format with which a specific system can work.

The completed technical specifications are the industry's clearest picture of what the more inclusive and elusive standards being pursued for the Computer Graphics Virtual Drive Interface (or just CGI) will look like, says Peter R. Bono, chairman of the American National Standards Institute's X3H3 Technical Committee on Computer Graphics and the U. S. delegate to the International Organization for Standardization. Although nearly 80% done, the broader CGI hardware interface standard is not expected to see final form

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## NEW GRAPHICS STANDARD IS ALREADY BEING EXTENDED

**Toil is everlasting** for standards makers. Although work on the document for Computer Graphics Metafiles is about to end, the International Organization for Standardization is expected to consider, at its meeting in England next month, new formal efforts to extend CGM.

Extended CGM—which has been in the works informally in ISO—would broaden the functionality of the image-describing metafiles. The extension would include an "audit trail" of the graphics transactions used to create a picture, and the capability for separating textual descriptions from the image itself.

"Some people feel it would be desirable to capture not only the final, static image, or snapshot, of pictures, but also the transactions that got you there," says Peter R. Bono, chairman of the American National Standards Institute's computer graphics committee and U. S. delegate to ISO. Some ISO members have expressed interest in creating segmented primitive groups, which can be used to create a hierarchical picture library of graphics objects and can be referenced by other graphics objects. In addition, the current metafiles cannot directly store three-dimensional images, Bono notes.

"I think everyone feels ECGM is worthy of standardization," he says. But "with all the other standards we are developing, will our parent committees give us permission to work on one more project? They might want us to complete some of these other projects first." *–J. R. L.*

until 1988 or 1989, he says.

"The elements of CGM that are used to describe a picture are carried directly in the current CGI draft," notes Bono. "So people who are looking for a standard device driver for primitives and attributes can look to CGM as an important subset of functions that will allow them to migrate toward the future CGI standard."

**TWO-WAY METAFILES.** The product bandwagon for CGM is also growing larger this week as both the ANSI and ISO prepare to give the specification final seals of approval. At Siggraph '86 in Dallas this week, Nova Graphics International Corp. of Austin, Texas, is introducing Nova*CGM. Like several other CGM-based programs, the package transmits image metafiles rather than data stored in a display-frame buffer. The receiving graphics system uses metafiles to construct its own picture.

Nova*CGM, available for delivery in the fourth quarter, will cost $3,500 for versions that run on Digital Equipment Corp. VAX superminicomputers. Lower-priced CGM packages will also be available for personal computers and work stations.

"I see CGM taking off in two areas today," says Christopher Nelson, vice president of research and development at Nova Graphics. "One is what I would call a computer graphics 'photo shop' for production of presentation graphics. The other would be for distributed editing of combined text and graphics."

X3H3 chairman Bono, chief consultant to CGM-software supplier Graphic Software Systems Inc. in Beaverton, Ore., admits CGM has had a relatively low profile in graphics standards, compared with CGI, GKS (Graphics Kernel Standard), or Phigs (Programmer's Hierarchical Interactive Graphics System). "CGM is low-profile because it is not a programming standard, but rather a data-exchange standard. The concept of graphical picture files has also been around for a long time. Some people wonder why they need a standard metafile," he notes.

The answer is that, in addition to opening up the transmission of pictures to different environments, CGM allows great flexibility in hardware design and usage, he says. For example, "you can archive your picture and bring it back two years later when there are new and better output devices," says Bono.

**TOOL KIT.** Graphic Software Systems offers two versions of CGM based on the completed ANSI specifications: a graphics development tool kit for the IBM Corp. Personal Computer and compatible systems, which contains a metafile generator; and a CGM interpreter that reads the metafiles.

Still another entrant, The Advanced Technology Center, began shipments of its CGM option to GrafPack-GKS software for the DEC MicroVAX three months ago, says Sahib Dudani, president of the Culver City, Calif., company. For one year, the company will update CGM software free of charge to ensure conformance with refinements of the ANSI and ISO standards.

And CGM will soon be getting the full attention of the Manufacturing Automation Protocol/Technical Office Protocol users group. Earlier this month, a computer graphics committee of the MAP/TOP group drafted a proposed CGM "application profile" defining a specific implementation of the standard.

Frank Dawson, CGM project manager for McDonnell Douglas Corp. in St. Louis and chairman of the TOP document-architecture technical subcommittee, expects to publish a document in March 1987. The MAP/TOP application profile takes the CGM standards and resolves some of the more loosely defined features of metafiles, such as the types of floating-point and integer coordinates and default conditions.

"I believe that between now and the end of the century, CGM is going to have the most important impact of any [of the] graphics standards, because it is going to allow the opening of existing closed systems," says Dawson. "But before you see a lot of CGM implementations, a user group like MAP/TOP has to sit down and specify the implementation constraints." *–J. Robert Lineback*

*SEMICUSTOM ICs*

# MASTER SLICE HAS BIPOLAR FUNCTIONS, CMOS LOGIC

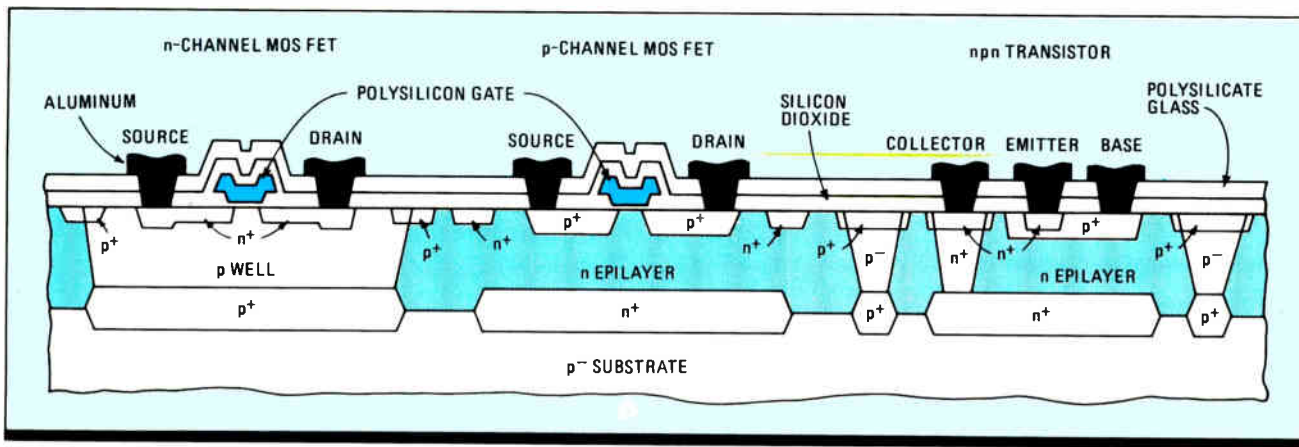
**KAWASAKI, JAPAN**

Fujitsu Ltd.'s in-house need for servomechanism control circuits has spawned an unusual addition to the company's line of semicustom chip offerings. The part is a master-slice chip that carries both bipolar analog and CMOS digital functions.

Fujitsu needed a number of different chips with both analog and digital circuits for its upcoming fixed-disk drives for mainframe computers, and these varying requirements precluded using a single custom circuit. Fujitsu engineers instead hit upon the idea of designing the mixed-process master-slice array, which can be wired in different ways to suit different purposes. A large part of the effort went into developing a library of macrocells, predefined circuit blocks that users can specify to simplify the design of new parts based on the master slice.

**OUTSTANDING MIX.** Among semicustom arrays combining analog and digital functions, Fujitsu's part stands out in its combination of bipolar and CMOS technology. Such arrays from other semiconductor manufacturers generally are either fully bipolar, such as the Quickchip arrays from Tektronix Inc., or fully CMOS, such as the TMG6000 arrays from Telmos Inc.

Furthermore, the Fujitsu master slice fills an application niche unmet by most such parts. Because of the context in




**BiMOS.** To combine bipolar analog and CMOS digital functions on a master slice, Fujitsu added thin oxide and poly layers to a bipolar process.

which it was developed, it's well suited for magnetic peripherals and other motor servo-control uses. Previous chips accommodate different ranges of applications. For example, the Telmos arrays are aimed at analog-to-digital and digital-to-analog conversion tasks.

The 3.4-by-5.5-mm master slices are fabricated with a fairly standard p-well process implemented in an n-epitaxial layer grown on a p-type substrate. The process was originally a bipolar one, with process steps and masks added to fabricate structures needed for CMOS circuits.

**HAND WIRED.** The first layer of the two-layer aluminum wiring is mainly used inside the macros. The second layer serves for power-supply distribution. Both wiring levels are used for making connections between macros. No channels are reserved for wiring; instead, it is run over the top of unused devices. Wiring design is a manual process that must be performed at Fujitsu.

The Kawasaki company's engineers say developing the semiconductor process was less difficult than designing a complete library of macrocells. But for users, the task of circuit design is fairly simple. Customers specify macrocells by circuit symbol—operational amplifier, comparator, and the like—rather than doing so at the transistor level.

The chip carries eight general-purpose analog macros, eight CMOS analog switch macros, four resistor macros, 60 CMOS gate macros, and four CMOS output macros. Also available are a total of 234 discrete npn and pnp transistors and 370 resistors. Input circuits, among others, are designed using the discrete devices rather than the macros.

Users must supply a complete circuit diagram, including macros. The company offers devices for breadboarding and also will supply parameters for simulation using the popular Spice program. Fujitsu does not provide any special support, though, for the relatively small 60-gate logic portion of the chip.

The company plans to start taking orders in October. Fabrication of new circuits will take about three months. Development costs are $32,000, and sample price per device is almost $8.00. A variety of dual in-line and small-outline packages with 16 to 28 pins are available.

The general-purpose analog macros are fabricated around bipolar transistors and typically will be used to implement op amps, comparators, two-input multiplexers, or voltage references. Users may specify standard op amps with a gain-bandwidth product of 1 MHz and a slew rate of 0.4 V/$\mu$s or a gain-bandwidth product of 2.2 MHz and a slew rate of 1 V/$\mu$s. Comparators are available with delay times of 1 or 0.2 $\mu$s.

Each resistor macro includes 36 separate 10-k$\Omega$ resistors with center taps that allow them to be used as 5-k$\Omega$ resistors. Their absolute tolerance is $\pm$20%, but the ratio between the values of a pair of resistors is specified as $\pm$2%.

The CMOS output macros are for interfacing off-chip circuits with the CMOS on-chip digital gates, which have insufficient driving power. Buffers enable the output macros to source or sink 0.44 mA. The propagation delay time of the logic-gate macro is 13 ns/gate. The discrete bipolar transistors have a common-emitter cutoff frequency ($f_T$) of 400 MHz for the npn devices, 6 MHz for the pnp devices. *–Charles L. Cohen*

*INDUSTRIAL*

# FACTORY DATA GATHERING THAT RUNS ON A PC

**IRVINE, CALIF.**

A company with unlimited assets could easily build the ideal plant with the help of the Manufacturing Automation Protocol, integrating host mainframe, programmable terminals, and robotics with MAP chips and software. But because cost constraints rule in the real world, most manufacturers would settle for an affordable hardware-and-software package that could gather critical data from products moving through the manufacturing line.

That's why True Data Corp. of Irvine is launching a simple but highly flexible system designed around an IBM Corp. Personal Computer or compatible. The company is moving to fill what observers agree could grow into an important market niche.

The TDC Perform system's principal hardware development is the SDT-100, an optical-scanning terminal that greatly simplifies data reporting by operators who lack high-level training. As many as 128 scanning terminals can tie into a production network with a memory-resident software package, also called Perform, that serves as a bridge between the data-collection terminals and the time-shared personal computer.

**$25,000 SYSTEM.** The SDT-100 terminals cost about $2,000 each and the software package $10,000, with communications hardware and battery backup for memory adding about $2,000 more. A general-purpose layout with five terminals would therefore go for less than $25,000. Custom-designed data-collection systems generally carry tabs many times that figure, notes True Data chairman James W. McKee.

His company is a natural source for factory-automation improvements that depend on reliable optical-scanning equipment, contends McKee. The privately held company is an established, though little-known, supplier of a major share of the optical card readers for on-line data terminals operated by

17 state lotteries across the U. S.

The key to any effective low-cost approach "is to make it simple for the worker on the floor to operate," says McKee. But another major factor is flexibility—the ability to read all common factory-floor data formats. The SDT-100 unit not only scans the company's proprietary document cards, but also can be set up to read the bar codes increasingly used on tagged manufacturing units. In addition, it reads magnetic strips and measurement data from instruments through a converter module that ties a machine with an RS-232-C port to an RS-422 link. An optional keyboard is available, too, to cover all the standard data-input approaches.

For most manufacturing operations, says McKee, the immediate problem is upgrading the way workers keep track of goods—typically by filling out forms manually. The forms take up too much time—both when they are being filled out and when data is compiled from them later—and they are the source of too many mistakes.

**TRAVELING DOCUMENTS.** Instead, True Data's system uses a "traveler" document, a card that carries optically coded information created by the system software. Information on the card conforms to a general format, but it describes a specific part and any instructions that a worker might need.

The worker inserts the card into a terminal at the beginning of a production step and reads the instructions that appear on the liquid-crystal display. When the task is completed, the worker marks boxes on the card for record-keeping and reinserts it. The terminal reads the marks and stores the acquired data in an 8-K-byte buffer until the personal computer polls it.

The records of all terminal transactions can be sent to a host computer.

*One terminal can read all common factory formats for data input*

"TDC Perform not only gives manufacturers a solid start at the factory-floor level as a stand-alone system but can work as a front-end processor for most mainframe hosts," says McKee.

True Data has been working on the system for more than a year, smoothing out rough spots at its beta-test sites, a textile company in New England and a machine shop in Southern California. With a polished product ready, McKee says, the company now faces "our biggest task—getting it to market."

The solution seems to be hooking up with distributors of software for general manufacturing applications, who regularly call on True Data's potential customers. The company is planning to set up a network of these distributors, and already has signed up several who serve prime manufacturing areas. So far, True Data reports a good deal of interest in the product and several initial sales.

The timing is right for such a system, believes Jeffrey Jilk, a vice president at DBSI, Laguna Hills, Calif. Many companies either are ready for a data-collection system now, he says, "or have plans for installing one." His distribution company has been evaluating these systems for some time, and it hasn't found another that incorporates as many approaches to data input as Perform.

For his part, McKee believes having a system in hand puts True Data "two years ahead of any competitors." To protect its lead, the company has applied for patents on the terminal and on the method of reading the documents.

As for MAP-based systems, whose complexity and cost now clouds the factory-automation picture, McKee says his company's system can be an important first automation step. "We're not fighting MAP. It's just that the world's not ready for it yet." *-Larry Waller*

*COMPUTER GRAPHICS*

# SMART BUFFER SPEEDS 3-D GRAPHICS

**CHAPEL HILL, N. C.**

Researchers at the University of North Carolina at Chapel Hill are pushing speed limits for interactive 3-d graphics on raster displays with a new system employing a smart frame buffer. Called Pixel-Planes, the raster-display system programs the buffer's custom logic-enhanced memory chips to execute time-consuming operations in parallel for each pixel.

The Chapel Hill team will report at Siggraph '86 in Dallas this week that the system is able to process 25,000 smooth shaded, z-buffered full-screen triangles per second. It can also form 13,000 smooth-shaded interpenetrating spheres per second (see photograph).

Some conventional systems might be able to match Pixel-Planes in triangles, but only when processing small figures that involve relatively few pixels, says Henry Fuchs, a professor of computer science and principal investigator for the five-year-old project. Such systems can do only a few hundred spheres per second, he says.

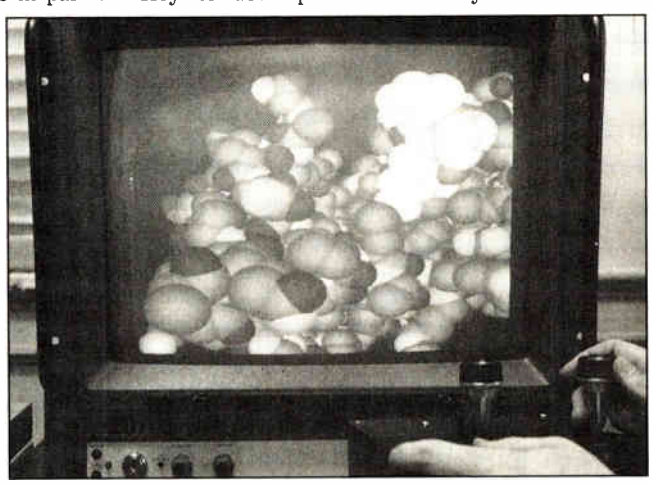
The prototype Pixel-Planes stores 512 by 512 pixels with 72 bits per pixel. The buffer contains 2,048 custom 3-$\mu$m n-MOS chips operating at 10 million microinstructions per second. The National Science Foundation and the Defense Advanced Research Projects Agency are financing the research.

Key to development of the system was overcoming the input/output bottleneck at the memory chips, says Fuchs. To do that, the team at Chapel Hill developed a translator module that shortens graphics algorithms to linear coefficients and associated operational codes.

"We found that a lot of [conventional graphics descriptions] drop out into linear expressions," says Fuchs. "We found that a particularly simple way to do algorithms." This design shifts the burden of calculating new values for each of the pixels onto the smart frame buffer.

Each of the buffer's 2,048 custom chips has a dynamic memory array that stores pixel data for a 128-pixel column, an array of 128 1-bit arithmetic logic units, and a multiplier/accumulator tree that evaluates linear expressions simultaneously for all pixels. The logic units within the memory chips execute the same microinstruction simultaneously. All memories also receive the same address at the same time.

Each chip is assigned a rect-



**MOLECULAR VIEW.** The Pixel-Planes system's logic-enhanced pixel memory gives it the performance needed for molecular modeling.

angular grid of continuous pixels, and its multiplier/accumulator—a tree of 1-bit adders—evaluates the linear coefficients to see if they apply to that grid.

"This is a binary tree at whose leaves are the pixels," says Fuchs. "Coefficients are poured into the tree at the top and what comes out at each leaf is the proper value for each pixel."

While the addition of logic to the memory increases the cost of the chips, Fuchs emphasizes that the logic takes up less than one third of the total silicon. "So it's not that expensive if you have a memory maker who wants to add it on," he says. Several chip makers have approached him for licensing, he says, but he would not name them.

In addition to Fuchs, the design team currently includes John Poulton, a co-investigator, and John Eyles, John Austin, and Trey Greer, research associates. Fred Brooks, also a computer-science professor at Chapel Hill, suggested the algorithm that produces the spheres .

The university has one patent for the basic design and another pending for the latest version. The Pixel-Planes machine is already in use in the university's graphics lab for molecular modeling. Another application is for a lung-tumor study at the university medical school. "These are applications that are very demanding of 3-d graphics and for which no current system was satisfactory," says Fuchs. *–Craig D. Rose*

***COMPONENTS***

# IMPLOSION PACKAGING SPEEDS DIODE PRODUCTION

**EINDHOVEN, THE NETHERLANDS**

A simple but ingenious trick is being used to fabricate glass-encapsulated diodes that perform better and are much easier to make than conventional glass-bead diodes. A vacuum-filling step used at Philips in encapsulating a diode in a glass sleeve causes the sleeve to implode and the glass to tightly grip the diode crystal.

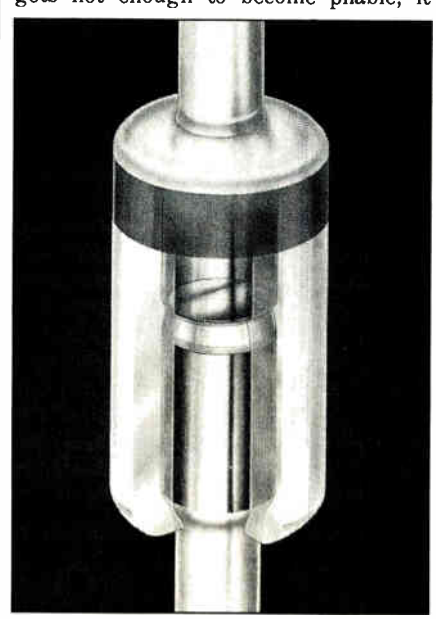
The implosion diode (ID) technology "greatly speeds up device fabrication compared to its glass-bead counterpart with a crystal of the same size," says British-born Graham Hine, international marketing manager for diodes at the firm's Electronic Components and Materials Division (Elcoma) in Eindhoven. An important electrical advantage, Hine adds, is a lower forward voltage. This makes for a more efficient device.

There are mechanical advantages, as well. As robust and reliable as a glass-bead diode, the ID is smaller in volume for the same crystal size. Furthermore, its cylindrical construction makes it better suited for automated handling than the glass-bead type with its ball-like package. The ID's size and shape together provide for a higher packing density on printed-circuit boards.

The ID technology is not a Philips invention. The basic idea for it came from Unitrode Corp., but the Lexington, Mass., company never went into full production with it, Hine says. After starting work on the technique in 1982, Philips refined it, introduced new features, and has moved it into volume production. The Dutch firm will also make the technique available to Japan's Matsushita Electric Industrial Co., in which it has a 35% interest.

Glass-bead diodes are made in four steps. First, the copper leads are soldered to molybdenum studs. Then, using aluminum, the studs are alloyed to the diode crystal. Next, the diode is coated with powdered glass suspended in a liquid slurry. Finally, the glass is sintered. This step forms the bead, which hardens as it cools.

The ID technique does away with the last three steps, replacing them with the implosion process. After the leads are soldered to the studs, the diode crystal and the studs are assembled in the glass sleeve. The sleeve is heated at atmospheric pressure and the assembly is wetted in the vacuum to oxidize the surface of the studs. As the glass sleeve gets hot enough to become pliable, it sticks firmly to the oxidized studs.



**IMPLODED.** Philips is in production with a new technique for encapsulating diodes in sturdy, cavity-free cylindrical glass packages.

Then comes the crucial implosion process. In this controlled operation, which takes place at 715°C, the vacuum is suddenly filled. As atmospheric pressure returns, the sleeve implodes—that is, the space between the round bevelled crystal and the hot glass collapses, causing the glass to firmly grip the studs and crystal. As it cools, the glass forms a cavity-free cylinder, which provides a sturdy structure, tight encapsulation, and excellent passivation for the crystal.

Assembling the crystal to the studs in the sleeve, heating the sleeve, wetting the assembly, and implosion are all one automated operation.

Both diode types, implosion and glass-bead, use round, beveled crystals to enhance the reverse blocking stability and to cut the field strength at the crystal surface. Both types of glass packaging are rugged and offer an excellent hermetic seal. Unlike plastic packages, glass packages are nonflammable.

But for the same crystal size, the ID with its cylindrical body is 20% to 30% smaller in volume than its ball-like glass-bead counterpart, Hine says. In addition to providing circuit-density advantages, the ID's small size improves a circuit's high-frequency performance. And the 715°C temperature used in ID fabrication is much lower than that employed in glass-bead-diode production, which lowers stresses in the ID.

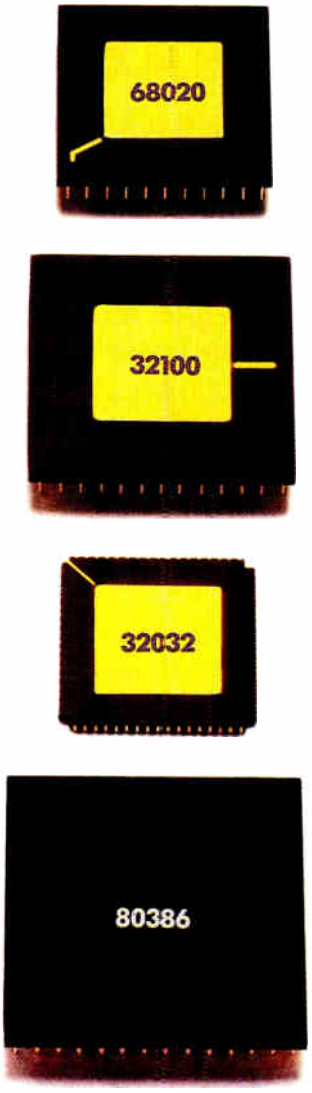
The pressure that the hardened glass exerts on studs and crystal is the prime reason for the ID's low contact resistance and, consequently, for its low forward voltage—10% to 15% lower than that of a glass-bead diode using a crystal of the same size and diode technology (double diffusion). This contact-by-pressure feature eliminates the need to alloy the studs and crystal together, a process that raises the forward voltage in a glass-bead diode.

ID technology makes it possible to build devices with a wider range of crystal sizes than is possible with glass-bead types. Because the ID is put together inside the sleeve, the stud-to-crystal joint is not subject to mechanical strain during assembly, so smaller crystals may be used. Crystal diameter can be as little as 0.7 mm. In glass-bead diodes, crystals must be at least 1 mm across.

The upper diameter limit for an ID crystal may be as high as 3 mm—in the future perhaps up to 4 mm. For glass-bead diodes, the crystal-fabrication process becomes difficult to control for diameters greater than about 2 mm.

Because there is no alloying phase in IDs, such devices can also accommodate a wider range of diode technologies—for example, high-speed Schottky and break-over diodes, both of which use shallow junctions. In glass-bead devices,

# State-of-the-past.



# State-of-the-art.

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Unlike the others, its performance isn't limited by an architecture designed back at the dawn of the microprocessor era. It's built from the ground up with a brand *new* architecture, for today's high-performance applications. And it's the only microprocessor that can bridge the architectural gap to true supercomputer performance.

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Designed for high bandwidth and true concurrent execution of instructions, CLIPPER runs at 33 MHz. Which, until we proved otherwise, was considered impossible. CLIPPER achieves a peak execution rate of 33 MIPS, with average performance greater than a VAX™ 8600 – twice as fast as any other microprocessor in existence, five *times* as fast as a VAX 11/780. And floating-point performance exceeds 2 MFLOPS, while simple instructions execute in a scant 30 ns.

## Supercomputer technology on a chip.

Unlike any other microprocessor architecture, CLIPPER uses proven supercomputer and mainframe architectural concepts.

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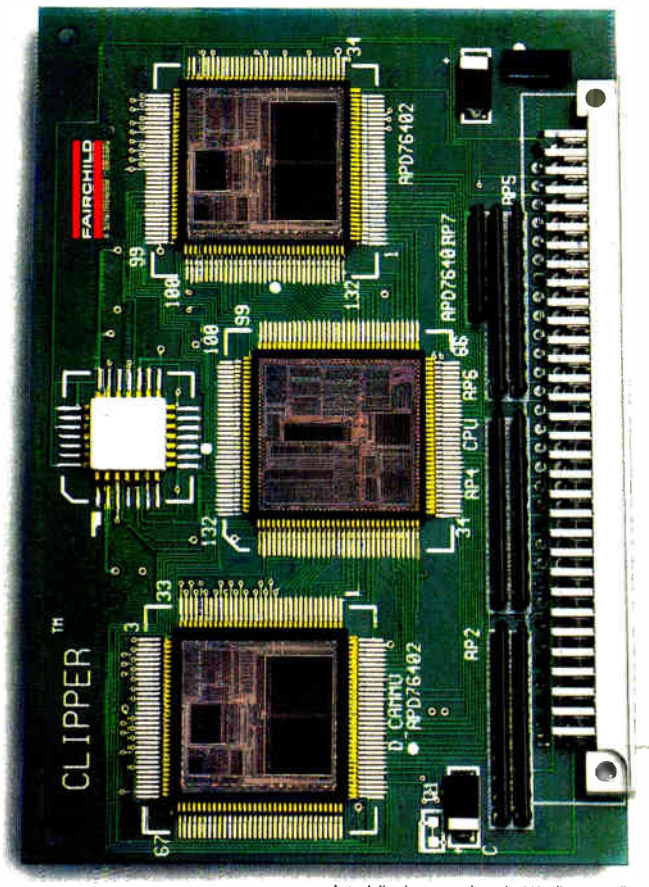
Two large 4K-byte cache/memory management units (CAMMUs) provide mainframe-style, copyback caching concurrent with virtual address translation.

Then there's our Streamlined Instruction Set. With 101 instructions hardwired instead of microcoded for performance. There's also a macro-instruction unit, providing 67 high-level instructions and system functions. For all the advantages of RISC and the robustness of a CISC.



Actual die size approximately 440mil. x 440 mil.

## What got into CLIPPER.

Residing on a 3.0 x 4.5-inch printed circuit card, the CLIPPER three-chip module includes a pipelined CPU with an on-chip, IEEE-standard FPU, and two 4K-byte cache/memory-management units. A clock generator completes the package, adding up to a staggering total of 845,000 transistors.

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the deep aluminum diffusion region precludes the use of shallow-junction technology. In IDs, the junction can be less than 5 μm deep.

The ID, Hine emphasizes, will come in especially handy in automated surface-mount assembly, to which Philips is firmly committed. By contrast, the ball-like construction of glass-bead diodes makes them hard for machines to grab.

Given the ID's many advantages, industry acceptance of glass-encapsulated diodes should accelerate, Hine says. At present, diodes that come in glass or glass-and-plastic packages account for about 40% of the world's diode market. Fully plastic-encapsulated types claim a 60% share. "It may not be long before that ratio is reversed," the Elcoma executive says. *–John Gosch*

*CONSUMER ELECTRONICS*

# ZENITH TV SOUNDS BETTER WITH FOLDED WAVEGUIDE

**NEW YORK**

Zenith Electronics Corp. thinks it has found a way to rise above the crowd of TV set makers offering digital models. The Glenview, Ill., company intends to woo customers by appealing to their ears as well as their eyes. Its new top-of-the line $1,400 to $1,700 models, introduced last week, come fitted out with a high-fidelity sound system designed by acoustic wizard Amar G. Bose, chairman of loudspeaker manufacturer Bose Corp., Framingham, Mass. To further differentiate itself, Zenith has tucked in a teletext decoder developed jointly with ITT Corp.

Set manufacturers can easily demonstrate the many wonders that digital processing of signals can bring to viewers: ghost-free images, pictures within pictures, zoom focusing, and the like. But convincing customers that a particular digital TV set stands out from the competition is another matter. Practically all the sets now on the market are built around the same chip set, making them all essentially equals as far as video goes.

Like most of these other set makers, Zenith has built its digital receiver around a chip set developed by West Germany's Intermetall GmbH, the lead house of the ITT Semiconductors Group [*Electronics*, July 15, 1985, p. 27]. "We are all using the Digit 2000 TV circuits," says Norm Watters, director of color-TV electrical engineering for Zenith.

No TV-set maker, though, has anything like the sound system from Bose—the Massachusetts Institute of Technology professor and entrepreneur who successfully launched a stereo speaker company and followed up with a line of stereo sound systems for General Motors Corp. cars. Bose came up with a low-frequency waveguide that improves the bass response of digital TV audio signals without a large enclosure or a particularly powerful amplifier. The Zenith models represent the sound system's first use in TV sets.

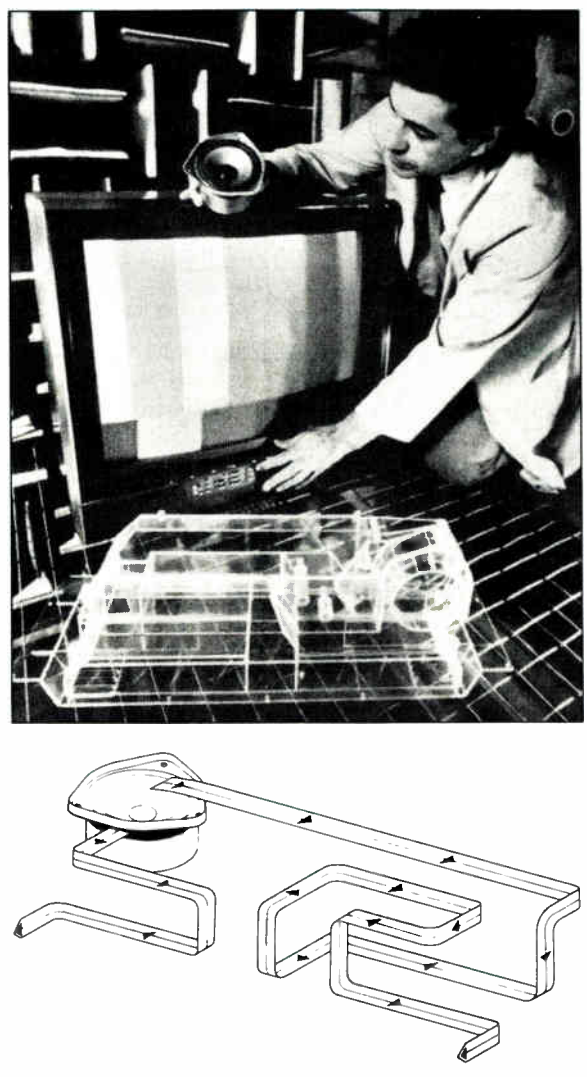
Magnetically shielding midrange and treble components assures good sound for the higher frequencies, but creating sound in the bass range involves moving large amounts of air in a large enclosure with a large speaker cone. Folded horns, bass reflex systems, and acoustic suspension systems improve bass response and decrease speaker size, but degrade efficiency or performance, says Zenith. And using oversize stereo speakers like outriggers on a TV set has never caught on.

**BASS OUT THE BACK.** Bose has hit on a speaker enclosure design that creates standing acoustic waves, which build to deliver high-quality bass response within the confines of the standard TV cabinet. The enclosure is mounted high at the rear of the cabinet and beams sound out the back (see photograph). For improved separation, a combination tweeter and midrange driver is mounted low in each of the two corners at the front of the cabinet. Each has its own amplifier. "The sound quality is excellent," notes David Lachenbruch, editorial director of *Television Digest*, a New York-based industry newsletter.

The standing waves in the Bose enclosure are formed by two elongated waveguides folded back onto themselves. A single low-frequency driver with a helical voice coil is precisely positioned so that one of the two waveguides is three times the length of the its complement. With the electromagnetic characteristics of the drivers and the dimensions of the waveguides precisely tuned, standing waves develop.

The waves reflect down the opening and travel back toward the speaker cone without dampening. Thus they produce a velocity gain in the air movement and a concomitant reduction in cone motion that improves speaker efficiency. The folded waveguides also function as low-pass filters that suppress distortions produced by the bass driver. The crossover frequency is 400 Hz.

Zenith maintains the set will be the first hardware with a built-in decoder for World System Teletext. The firm claims that 40% of U.S. television households are within range of World System broadcasts, but the protocols are not expected to find widespread support for some time. *–Robert Rosenberg*



**FINE TUNING.** Bose's split waveguide fortifies the bass component of TV stereo sound and beams it out of the cabinet's rear on both sides.

# INTERNATIONAL NEWSLETTER

## EC THREATENS ACTION AGAINST U.S.-JAPAN IC PACT

Reaction among U. S. electronics executives to the new U. S.-Japanese accord on semiconductor trade may be mixed (p. 79), but the Commission of the European Communities has stated in no uncertain terms that it doesn't like the agreement at all. In fact, fearing that the pact will also boost chip prices in Europe, the commission is threatening to take action under the General Agreement on Tariffs and Trade. The EC agrees that Japanese dumping must be halted, but objects to having the prices of chips sold in Europe determined, in effect, by a bilateral deal that has been made between countries outside the Continent. Meanwhile, the European Electronic Components Manufacturers' Association in Brussels is pursuing an antidumping case against the Japanese. West Germany's Siemens AG and others are alleging unfair pricing in dynamic random-access memories and in electrically programmable read-only memories. Speaking for the DRAM sector, an executive at Siemens in Munich says the company can prove the Japanese are engaged in dumping. □

## 3-D VIDEO DISKS GO ON SALE IN JAPAN NEXT MONTH

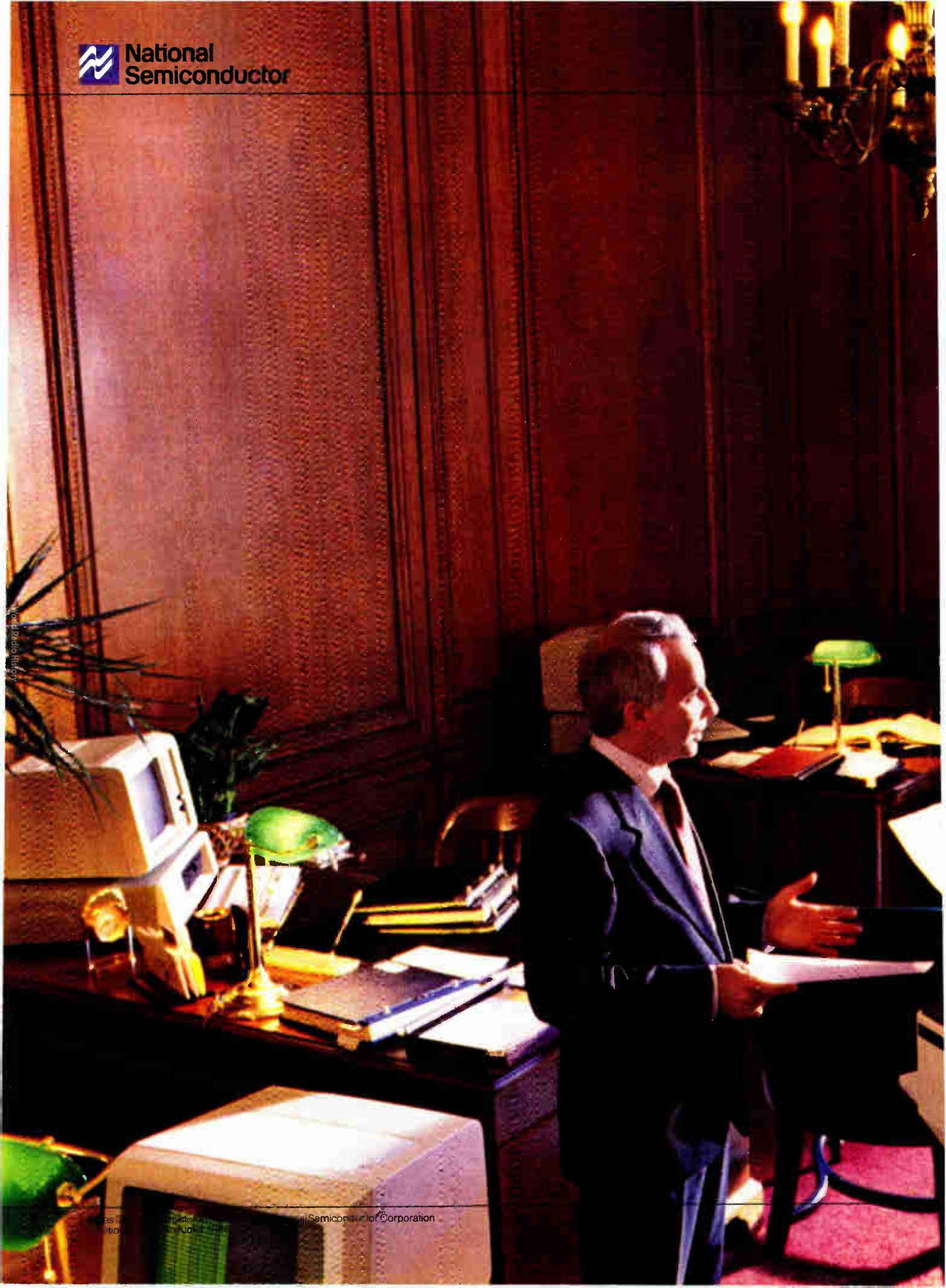
Disks that play three-dimensional video are about to hit the home-entertainment market. Victor Co. of Japan (JVC) will be first out with disks in Japan next month. The disks will be available only in Japan because Video Home Disk-format players for the consumer market are not available anywhere else. Adapters, priced at about $130, will be needed to play the new disks on conventional players; in addition, each viewer must wear an $85 pair of liquid-crystal-shutter eyeglasses, just as in the prototype system that Sharp Corp. displayed at the last Summer Consumer Electronics Show [*Electronics,* June 9, 1986, p. 11]. Matsushita, Sharp, and Toshiba will join JVC next month in selling adapters. Only Sharp has announced that it will begin sales of glasses, but other manufacturers are expected to do the same, even if initially they are private-label products supplied by Sharp or another vendor. JVC and the other manufacturers plan to sell players in the future with the 3-d function built in. JVC is committed to a total of 10 disk titles by year's end and many more next year. Disks only partly 3-d in content will sell at about the same price as ordinary disks; all-3-d disks will cost $33 more. □

## WEAKER DOLLAR STARTS TO HIT WEST GERMAN INDUSTRY

The declining U. S. dollar is beginning to hurt West Germany's electronics industry. One of the first companies to be hit is Hell GmbH, a Siemens AG subsidiary in Kiel that produces computerized typesetting equipment for publishing houses. It has put about 1,000 of its 2,660-person work force on shorter work weeks. It plans to lay off several hundred others. Company executives blame the deutschemark's strength against the dollar. □

## HUNGARY FORCED TO UPGRADE WAFER-FAB LINES

A fire that destroyed both the MOS and bipolar wafer-processing lines at Hungary's MEV Microelectronics Co. has been a blessing in disguise for the nation's nascent semiconductor industry. It has forced the government to accelerate plans to upgrade the lines, and Budapest has turned to Western companies to design a new plant. The old lines could do 3-$\mu$m features and the Hungarians want to get down to 1.5- to 2-$\mu$m geometries. Negotiations are going on mainly with West German companies, says the government, though it won't specify which ones. The Hungarians say they will give preference to companies willing to make a capital investment or at least to participate in a turnkey arrangement. □


National
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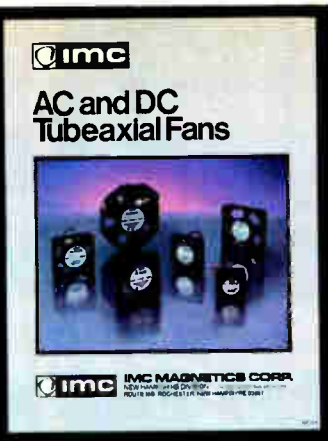


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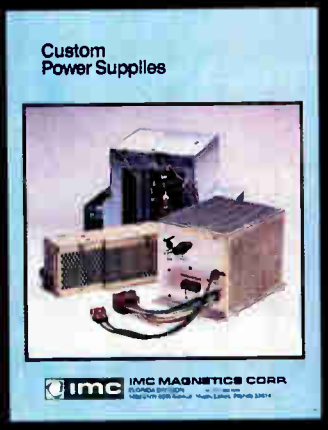


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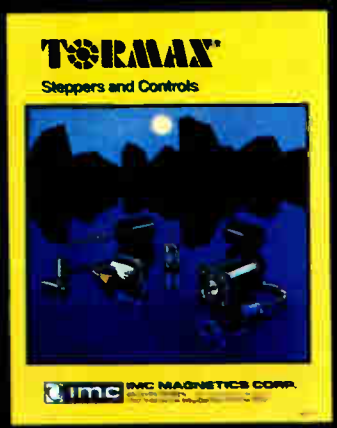


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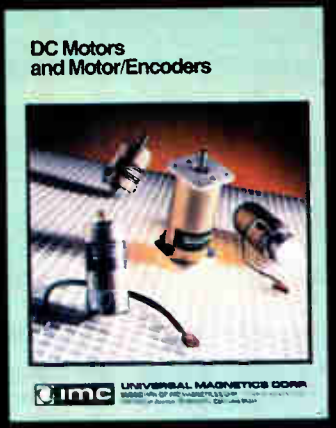


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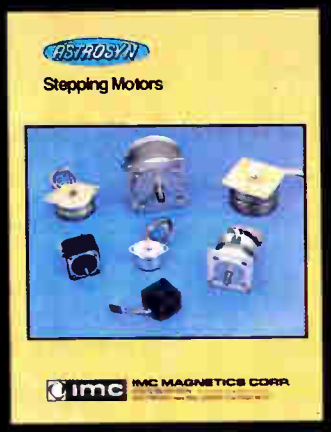


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Catalog features Mini Angle type stepping motors. Also contains engineering information and application examples.


Circle Reader Service No 118

Brochure features stepping-motor drive IC chip which is intended for a wide variety of applications. Contains diagrams & tables on excitation, modes & applications.

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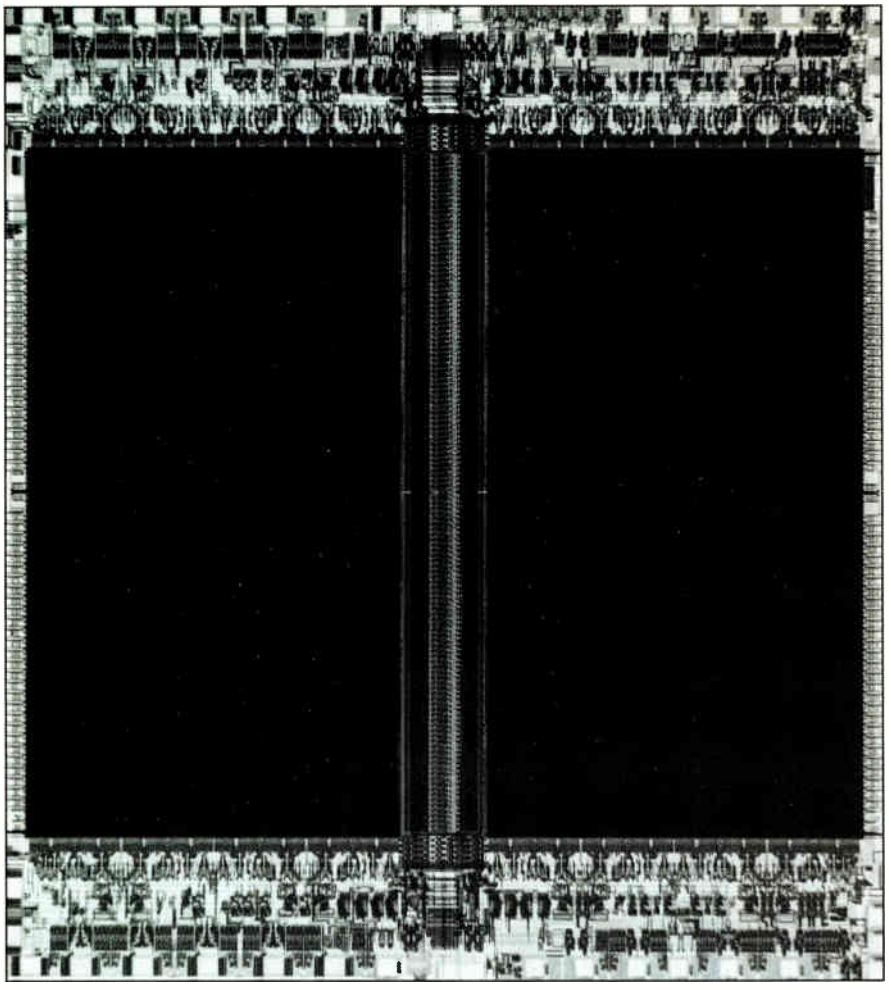
INSIDE TECHNOLOGY

# THE EXPLODING ROLE OF NONVOLATILE MEMORY

by Bernard Conrad Cole

*Hustling to stimulate a stagnant market, producers of EEPROMs and EPROMs are pushing the limits of nonvolatile memory technology. Companies are not only exploring new uses for existing technology, they are launching major efforts aimed at boosting densities and speeds and developing new design approaches. This effort is fueling a chain reaction that is already driving nonvolatile memory beyond its traditional role of simple data retention. The memory makers are*



**3. COMPACTED.** With its 1.4-μm compacted HMOS II-E, Intel Corp. achieves 150 ns in its 64-K-by-16-bit 27210, one of the company's three 1-Mb EPROMs.

the single-transistor EPROM cell is inherently slower than the fuse element in PROMs. In addition, EPROMs have usually been optimized for programmability and density, often at the cost of speed.

Cypress achieved its high speed by combining a 1.5-μm n-well CMOS process with a new four-transistor differential EPROM cell. The latter separates the read and write transistor functions with a true differential sensing technique rather than the traditional differential dummy-cell approach. Also employed for the first time in an EPROM is a substrate bias generator to improve performance and boost immunity to latchup.

Aiming ultimately at much higher speeds and densities than Cypress, WaferScale has developed a proprietary split-gate structure with which it can build single-transistor EPROM cells comparable in performance to four-transistor designs. According to manager Ali, the split-gate structure results in high bit-line voltage and read current, allowing the company to employ a differential sensing scheme that does not require a separate bit line. This allows bit-line voltages to be sensed more than five times as fast as previous approaches, he says.

"The heart of the EPROM speed problem lies in rapidly sensing the voltage on the bit lines following address decoding," Ali says. "The bit-line capacitance plays a big part in the equation. If the capacitance remains fixed, higher read current is needed to achieve greater speed. If the capacitance can be lowered, speed improvements can be achieved without increasing read current." Scaling the 1.6-μm double-poly CMOS process used in its 64-K EPROMs down to 1.2 μm and combining it with an even higher read current will allow the company to fabricate 128- and 256-K EPROMs that will go head-to-head with bipolar PROMs in speed, according to Ali.

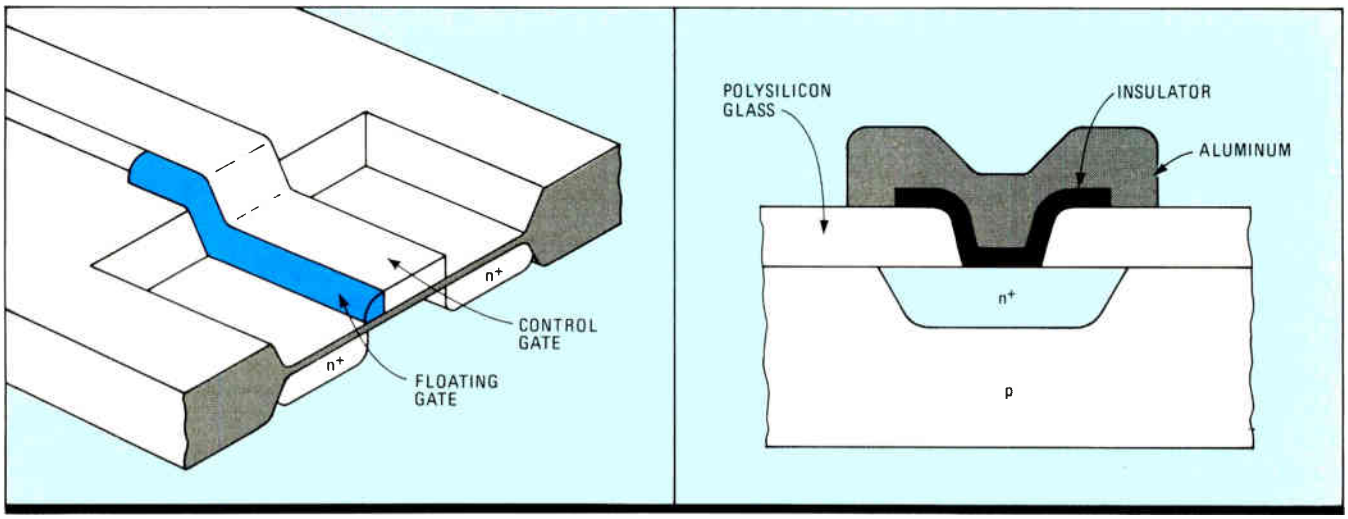
Because EPROMs are so easy to scale, they are on a fast track toward higher densities. According to Dataquest's Mason, at least six companies should have 1-Mb EPROMs in production by mid-1987, including AMD, Hitachi, Intel, Motorola, Texas Instruments, and Toshiba.

First out is Advanced Micro Devices Inc., Sunnyvale, Calif., with its 200-ns Am27C1024, organized as 64-K words by 16 bits and fabricated using a 1.5-μm CMOS process with two layers of poly and one of metal. Although the memory cell retains many of the basic characteristics of n-MOS, AMD completely redesigned the peripheral circuitry for CMOS. The use of stepper-based lithography and aggressive scaling yields a cell about 20 $\mu m^2$, about the size of a masked-ROM cell, says product marketing manager Ajay Shah.

Following AMD into the market is Intel Corp. The Santa Clara company has not one, but three 1-Mb EPROMs. The 150-ns 27210 (Fig. 3) is organized as 64-K words by 16 bits. The 128-K-by-8-bit 27010 and the page-addressed 27011, organized as 8 pages by 16-K bytes by 8 bits, are both byte-wide, 200-ns devices. All are fabricated using a 1.4-μm compacted n-MOS process the company calls HMOS II-E.

Hitachi Ltd. is using a 1.3-μm CMOS process to achieve 1-Mb EPROM densities. The Tokyo company combines the traditional stacked floating-gate structure with deeply doped channel and double-step drain structures to hike programming speeds, maintain high breakdown voltages, and improve immunity to soft errors.

In its 1.2-μm CMOS 256-K and 1-Mb designs, Motorola supplements the traditional stacked double-poly floating gate with a third thin-oxide,




**4. BEYOND 1 MEGABIT.** Two designs that promise EPROMs above 1 Mb are Toshiba Corp.'s sidewall floating-gate structure (a) and Fujitsu Ltd.'s BIC cell (b), which stands for breakdown of insulator for conduction.

nitride-oxide layer. All told, the three layers produce a 17-$\mu m^2$ cell.

Getting EPROMs to the 2-Mb level will require scaling down to about 1.0 $\mu$m as well as incorporating alternative isolation structures, such as the deep trenches being considered in 4-Mb CMOS DRAMs. Even higher densities will require a shift to alternative EPROM cell structures. Two designs that promise EPROM densities up to 4 Mb come from Japan. One is a sidewall floating-gate structure (Fig. 4a) from Toshiba Corp. The other is the BIC cell (Fig. 4b) from Fujitsu Ltd., a new programmable structure that uses breakdown of insulator for conduction.

Toshiba strays from traditional EPROM design in using a floating gate on one side of a poly gate, which reduces cell area by 60%. For data programming, the n+ region on the floating-gate side acts as the drain and the n+ region on the other side of the control gate acts as the source.

Fujitsu's BIC cell uses the electrical breakdown of a proprietary thin insulation layer for programming. The advantage of this design is that an EPROM can be formed by simply adding the BIC structure to a MOS FET.

## MERGING TECHNOLOGIES

The most frenzied activity has been in EEPROMs, with manufacturers studying a variety of techniques to match EPROM density. The problem with traditional EEPROM cells is that they need at least two transistors, one a floating-gate structure for programming and erasing and a separate select transistor for reading. The result is that two-transistor-cell EEPROMs are at least one generation behind single-transistor EPROMs in terms of density.

One of the most promising techniques for achieving EPROM-like densities involves merging the hot-electron avalanche-injection programming mechanism of EPROMs with the cold-electron Fowler-Nordheim erase mechanism of standard EEPROMs. This achieves what is known as the flash EEPROM, a single-transistor cell.

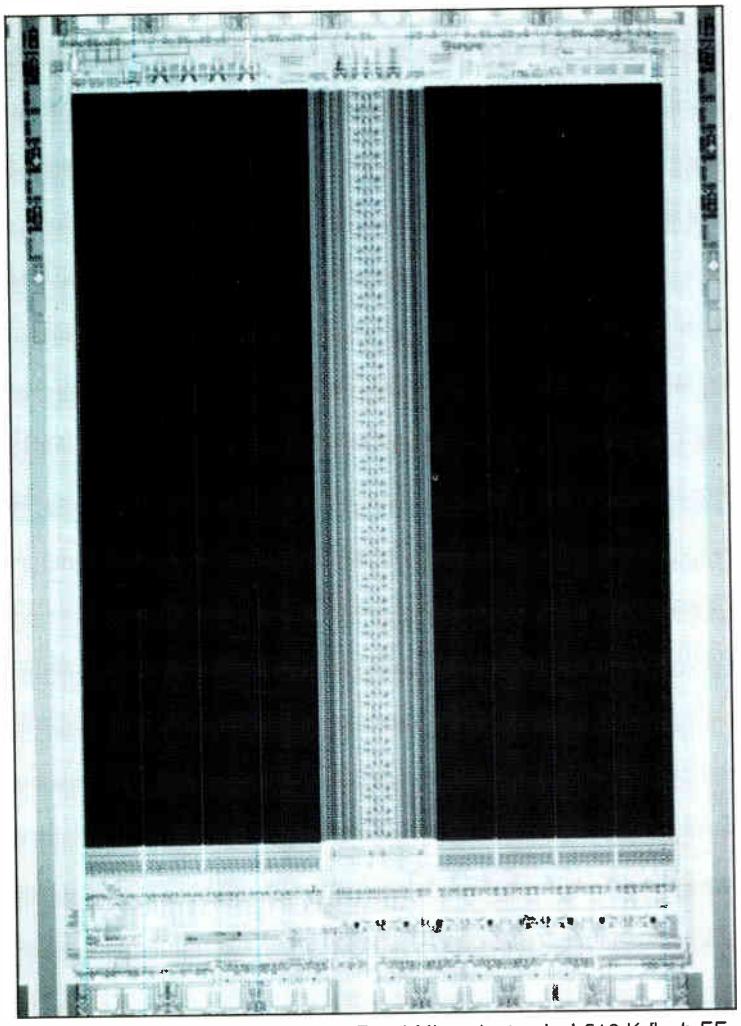
Flash-EEPROM technology has important implications for chips other than memories, says Michael Villott, marketing director for Seeq Technology Inc., whose 128-K QPROM was one of the first flash EEPROMs into production. "One obvious extension we have under study is to use it in single-chip microcontrollers for program memory storage," he says.

The San Jose company has modified the basic floating-gate structure to create a "phantom" select gate, eliminating the need for an external read transistor (see story, p. 53). Using a relatively conservative 2.5-$\mu$m n-MOS process, this

*Flash-EEPROM technology has important implications beyond memories. Among other uses, it could store the program in single-chip microcontrollers*

1½-transistor design yields a cell around 40 $\mu m^2$, about twice the size of a standard EPROM cell and one half to one fourth that of an EEPROM cell with similar geometries. Scaling could further pare down cell size, pushing densities to the 512-K and 1-Mb levels.

This technology will allow the design of self-adaptive microcontrollers with internal memory capacities equal to that of the largest ROM-based units, says Gheorghe Samachisa, Seeq's flash-EEPROM project manager. Another possible extension is the integration of a low-endurance 100- to 1,000-cycle flash EEPROM with smaller amounts of high-endurance 10,000- to 1-million-cycle standard EEPROM onto a microcontroller chip, allowing even greater flexibility. "Programmable logic arrays are also likely to benefit from



**5. ONE TRANSISTOR.** Excel Microelectronics' 512-K flash EEPROM has a double-poly, single-transistor CMOS cell. Like an EPROM, it uses the control gate as the select transistor.

the high densities possible with flash EEPROM cells," Samachisa says.

A slightly different design for a 512-K flash EEPROM (Fig. 5) will be in production by year's end at Excel Microelectronics. Using a traditional double-poly stacked cell, Excel engineers found a way to eliminate altogether the need for an external select transistor for reading, allowing them to design a true single-transistor flash-EEPROM cell. Like an EPROM, the cell uses the control gate as the select transistor. The result is a cell of only 25 $\mu m^2$, compared with the 44 $\mu m^2$ for Seeq's 1.5-transistor cell, the 20 $\mu m^2$ of standard EPROM cells, and the 80 to 160 $\mu m^2$ of traditional two-transistor EEPROMs.

A third flash-EEPROM approach, from Toshiba, achieves a single-transistor cell by using three levels of poly instead of two. The first layer serves as the erase gate, using Fowler-Nordheim tunneling; the second handles programming, using EPROM-like hot-electron avalanche injection; and the third acts as the control and select gate for reading.

Toshiba fabricated a 256-K device with a 64-$\mu m^2$ cell in the laboratory, using 2-$\mu m$ design rules. Under development is a 1-Mb flash EEPROM with a 29-$\mu m^2$ cell using 1.2-$\mu m$ design rules. However, the company is closemouthed about when—or if—it expects to come to market with the device.

But no matter what structure is used, one problem with the flash EEPROM is that it still requires a thin-oxide approach, says Xicor's Owen. "And as you scale the cell to get to higher densities, it is necessary to do so in all three dimensions. Scaling the geometries horizontally is hard enough. But in thin-oxide designs, it is also necessary to scale an already intolerably thin 90- to 100-Å oxide down to 70 to 80 Å, introducing serious reliability problems."

For this reason, he says, Xicor has opted for a thick-oxide triple-poly cell as its vehicle for high-density EEPROMs [*Electronics*, May 12, 1986, p. 30]. Achieving 256-K densities with this approach required only scaling down from 3 to 2 $\mu m$ horizontally and from 600 to 400 Å vertically, he says. At 68 $\mu m^2$, the resulting cell is only slightly larger than Seeq's thin-oxide flash-EEPROM cell.

Intel gave Xicor's approach its seal of approval by switching its allegiance away from the thin-oxide floating-gate (Flotox) cell approach it pioneered and made the de facto industry standard for EPROMs and EEPROMs. "Even though Flotox has proven to be a highly reliable technology for lower densities, we are shifting to the triple-poly thick-oxide approach because it allows the cell to be scaled to a greater degree," says Bruce McCormick, EEPROM marketing manager at Intel.

The move to higher densities in EPROM and EEPROM designs can be expected to upset the status quo in the Novram marketplace. At present, there is a standoff between SRAMs backed up by lithium batteries, supplied by vendors such as Dallas Semiconductor, Mostek, and Thomson Components, and EEPROM-SRAM combinations supplied by Catalyst Semiconductor, Intel, Xicor, and others.

## SHAKING UP NOVRAMS

Battery-backed SRAMs now appear to be taking the lead because they combine nonvolatility with the high speed and high density of SRAMs, says Michael Bolan, vice president of marketing at Dallas Semiconductor Corp. Battery-backed SRAMs as high as 64-K are available, he says, versus about 4-K for Novrams.

This will likely change when high-density EEPROMs begin to capitalize on the fact that their single-transistor memory cells are one fourth to one sixth the size of SRAMs', believes Catalyst president B. K. Marya. Not only will this tip the balance back to EEPROM-based Novrams, says Dataquest's Mason, but it will considerably expand their market, which has hovered between $20 million and $25 million annually since 1984.□

# HOW SEEQ IS PUSHING EEPROMs TO 1-Mb DENSITIES

*Combining the fast programming techniques of EPROMs with the erasure mechanism of EEPROMs results in a high-density device with the best of each*

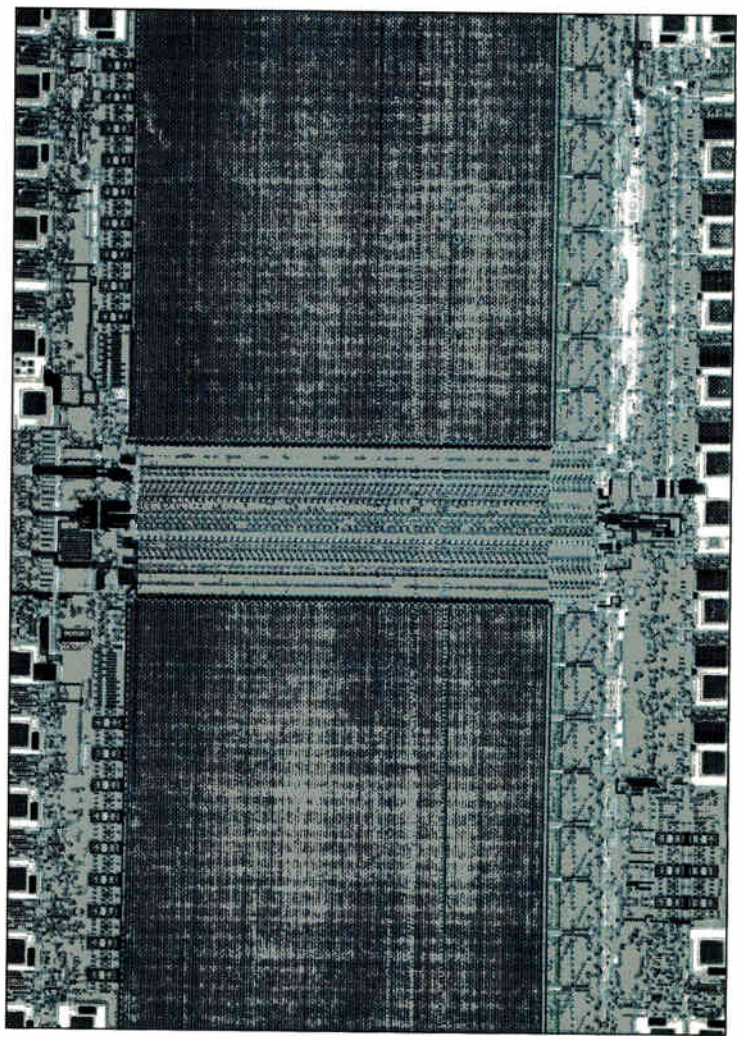
The 1-Mb electrically erasable read-only memory has come a step closer, now that Seeq Technology Inc. is going into production with its version of a flash EEPROM. This device, so named because the contents of all the array's memory cells are erased simultaneously by a single field emission of electrons from the floating gate to an erase gate, combines the advantages of ultraviolet-erasable EPROMs and floating-gate EEPROMs. It unites the high density, small cell size, low cost, and hot-electron write capability of an EPROM and the easy erasability, on-board reprogrammability, high endurance, and cold-electron tunneling erasure of floating-gate EEPROMs. In doing so, Seeq's single-transistor 16-K-by-8-bit memory paves the way for high-density EEPROMs.

"No longer will EEPROMs trail EPROMs in density," says director of marketing Michael Villot. EPROM arrays have a 4:1 density advantage over the EEPROM, whose array densities still hover at the 256-K level. And even though EEPROM cells are now as small as 57 $\mu m^2$, the EPROM cell remains one third its size with attendant cost advantages. But because flash EEPROMs are made with the same processes as EPROMs, says Gheorghe Samachisa, project manager, their prices will be competitive—and considerably lower than comparable two-transistor EEPROMs.

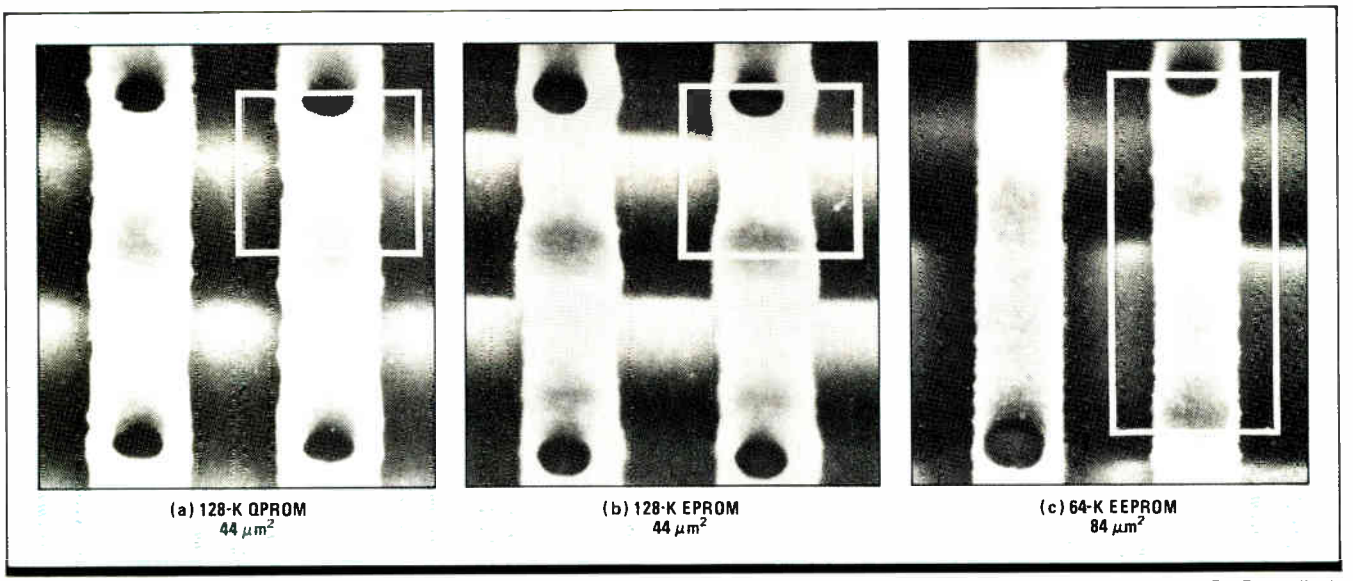
"In addition, because the flash EEPROM can track the density path of the EPROM very closely, it resolves a dilemma for those users who required the high density of EPROMs but also wanted the ease of erasability of EEPROMs," Samachisa says. The San Jose, Calif., company's first commercially available flash EEPROM (Fig. 1) is the 2½-$\mu$m n-MOS 42128 QPROM, for quick EEPROM. It is based on a proprietary 44-$\mu m^2$ single-transistor cell half the size of standard EEPROMs (Fig. 2). It will be followed soon by versions in the 512-K to 1-Mb range, says Villott.

Flash EEPROMs have two functional advantages over EPROMs—fast erasure and in-circuit reprogrammability. "Flash EEPROMs erase in about 1/60th of the time—no more than 20 seconds," says Samachisa. It takes a design engineer about 1 minute to erase and reprogram a flash EEPROM, compared with 20 minutes or more for an equivalent EPROM. These advantages cut the time needed to design a system and upgrade it in the field.

Even if in-circuit reprogrammability is not



**1. FLASHY.** Seeq's n-MOS 128-K 48128 QPROM is a flash EEPROM whose cells are erased simultaneously by a single field emission of electrons from a floating gate to an erase gate.




**2. SMALL CELL.** At 44 $\mu m^2$, the cell size of Seeq's QPROM (a) equals that of an EPROM cell (b) and is half that of an EEPROM cell (c).

used, Samachisa says, the flash EEPROM still comes out ahead of the EPROM because it can be upgraded in the field. This eliminates the need for an inventory of EPROM spares; it also ends the waste when replaced memories are discarded rather than returned for reprogramming. Further, as with less-dense traditional EEPROMs, the high-density flash chips can be soldered into the equipment. Erasing and reprogramming in the field are done either by removing cards and placing them in a special programmer or by programming them without removal from the system when the required high-voltage programming and erasure voltages are available.

## EPROMs vs. EEPROMs

An EPROM cell is relatively simple in structure. It is a true single-transistor cell, usually consisting of two polysilicon gates. The upper one, connected to row decoders, is the control gate, and the bottom one is a floating gate between the control gate and the substrate, isolated in the surrounding silicon dioxide. Programming, or writing, is done by avalanche injection of hot electrons from the substrate through the isolating oxide under the influence of a high applied drain voltage. This causes an electrical charge to be collected on the floating gate. The electrons must gain enough energy to jump over, rather than through, the potential energy barrier between the silicon substrate and the silicon dioxide. When the high programming voltage is removed, the charge is trapped on the floating gate by the surrounding oxide insulator.

To pull the electrons toward the floating gate requires application of a high positive select voltage. As the gate becomes more charged, the electrons in the oxide field are repelled from the floating gate and move back to the substrate.

An EPROM cell is erased through internal photoemission of hot electrons from the floating gate to the control gate and the substrate. Incoming UV light increases the energy of the floating-gate electrons to a level at which they jump the potential energy barrier between the floating gate and the $SiO_2$. This avalanche injection can occur with oxides as thick as 1,000 Å, which makes the devices relatively easy to fabricate. However, they can be used only to write and have no deprogramming mechanism. This necessitates the use of an alternative method, such as UV light, to discharge the gate. In addition, says Samachisa, there's a tradeoff for the EPROM's small size (about 20 $\mu m^2$ at the 1-Mb level) and low cost. Designers have had to settle for low endurance—no more than 100 to 1,000 erase/program cycles.

EEPROMs' chief advantages are significant system flexibility, thanks to on-board programming capabilities, and an endurance of 10,000 to 1 million cycles. To achieve this, most manufacturers use a two- to three-element cell with two transistors and one tunneling dielectric element per cell. One transistor is used for reading, the other for programming and erasure. Standard EEPROMs are erased by means of the Fowler-Nordheim effect, in which cold electrons are tunneled through, rather than over, the energy barrier at the silicon-$S_2O$ interface and into the oxide conduction band.

The advantage of the Fowler-Nordheim approach is that it can be reversed and used for programming. Its disadvantage is that it depends on the manufacturer's ability to process thin-oxide layers (100 Å or less, depending on the technology) that have high reliability. Processing gets more difficult as device geometries shrink.

The program-erase operation of the EEPROM cell depends on the ability to apply a large reversible electric field to the thin oxide separating the floating gate from the substrate. This field must be strong enough to produce a measurable

current through the thin oxide by indirect tunneling. At the same time, the field in the interpolysilicon oxide has to be maintained at a relatively low value to prevent unwanted transport of electrons between the floating gate and the control gate.

During programming and erasure, the thin-oxide field is controlled by the relative voltage applied to the control gate and the drain overlap region, resulting in much lower programming voltages than EPROMs. Erasure is performed by charging the floating gate, resulting in a logical-1 state in the cell. It occurs when the source, drain, and substrate are grounded and the control gate is raised to a high voltage. Programming is done by tunneling electrons from the floating gate to the n+ drain diffusion by grounding the control gate and applying the programming voltage to the drain diffusion. This produces a logical-0 state in the cell.

Unlike an EPROM cell, in which the control gate also acts as the select transistor, an EEPROM cell requires a separate select transistor linked in series with the floating-gate transistor to read the device. During a read operation, the cell's state is determined by current sensing by means of the select transistor.

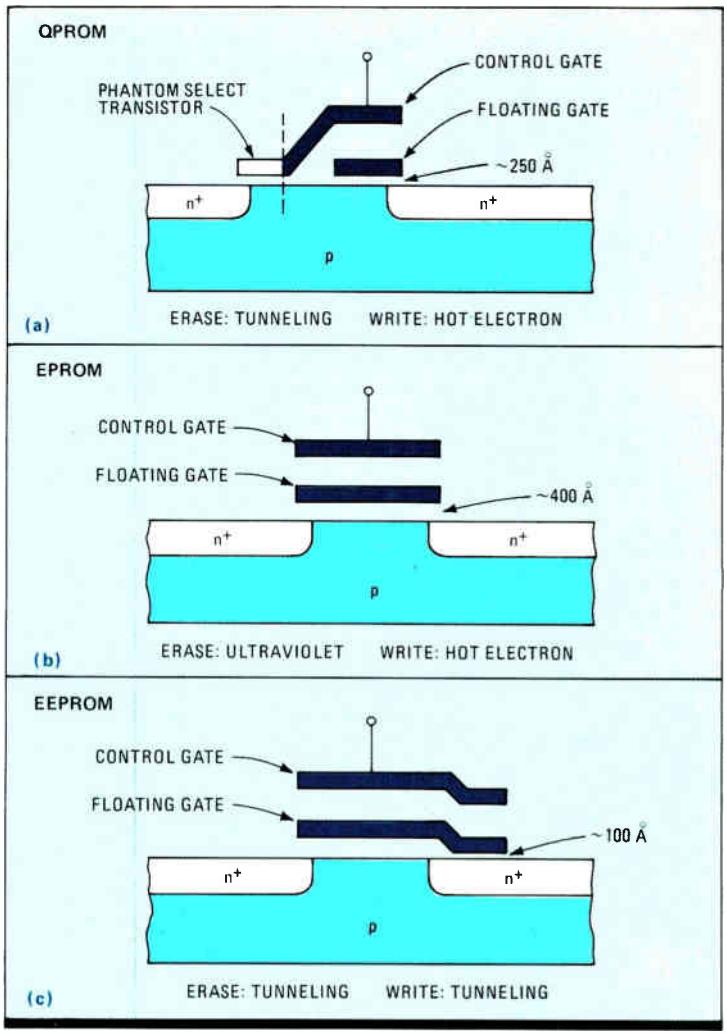
## ENTER THE FLASH EEPROM

In contrast, the flash EEPROM combines the programming, write and erase, and read-select functions in a single-transistor structure (Fig. 3). Frustrated by the high cost and low density of traditional EEPROMs, a number of companies recently have investigated single-transistor structures for flash EEPROMs (see story, p. 47). In other companies' approaches, though, an important functional problem remains, says Samachisa. "In the erased state, the cell's floating gate is depleted of electrons and behaves like a depletion-mode transistor. What this means is that a nonaddressed cell in the erased state leaks current. This leakage can cause false data reads and/or a failure to program."

Seeq's design, however, modifies the basic EPROM so that the poly gate controlling the channel between it and the floating gate extends beyond the floating-gate edge, creating a "phantom" select transistor. This eliminates the need for another transistor.

The cell is self-aligned at both the drain and source sides. The section of the channel under the influence of the control gate forms an n-channel select transistor that operates in the enhancement mode, in effect linked to the floating-gate transistor in series. This prevents leakage during read and programming through an erased cell that has not been addressed.

The QPROM cell programs like an EPROM cell, using hot-electron injection in the channel between the control gate and the floating gate. During programming, the phantom select transistor is on only in the addressed cell. In all




**3. EPROM/EEPROM.** The QPROM cell (a) merges the EPROM write mechanism (b) and EEPROM erase mechanism (c) with the read-select transistor into a single structure.

nonaddressed cells, the select transistors are off.

The QPROM is erased by Fowler-Nordheim tunneling of electrons from the floating gate to the drain diffusion, during which the control gate is grounded and the drain raised to a high voltage. The erase speed depends on the oxide thickness and the potential voltage difference between the floating gate and the drain. It can be improved by decreasing the oxide thickness or increasing the drain voltage, but both approaches have disadvantages. Scaling the oxide requires similar scaling in the horizontal direction, increasing the complexity of the process and increasing cost. Increasing the drain voltage adds the risk of breakdown and reduces reliability. In the Seeq approach, thin oxides are used only at the drain electrode in the overlapping area between the drain diffusion and the floating gate, which makes it easier to manufacture than devices using thin oxides throughout.

Built with a relatively conservative 2.5-$\mu$m process, a 128-K QPROM cell measures about 44 $\mu m^2$, the same as a cell in the company's 27128

EPROM. The device can be erased and reprogrammed in less than 1 minute, versus 20 minutes or so for an equivalent EPROM: 20 seconds to raise the program voltage pin to 21 V in order to reset all memory locations to logic-1 states, and 32 seconds for programming. A 90-μs programming pulse is then applied on a byte-by-byte basis after data is validated; the pulse is repeated for all addresses to be written.

### BEYOND 128-K

Moving from 2.5 to 2 μm, Samachisa says, will allow densities in the 512-K range. And scaling to about 1.5 μm will push flash EEPROM densities beyond 1 Mb.

More importantly, if the flash EEPROM cell is scaled, the 21-V programming and erasure voltages can also be scaled to the 5- and 12-V levels typical of standard EEPROMs. "This will extend the applicability of flash-erase EEPROMs to systems that might have used standard EEPROMs if they were more cost-effective," Samachisa says. "With scaling, additional EEPROM-like features can be added, such as page-mode erase and programming, latches, and on-chip timers."

Currently, the endurance of the company's first flash EEPROM is about 100 erase/program cycles, approximately equivalent to that of an EPROM. However, says Samachisa, it should be possible to improve endurance considerably with a combination of process enhancements and circuit-design improvements. And because the double-poly process used to fabricate the QPROMs is similar to that used in high-endurance EEPROMs, nonvolatile memory combinations merging the low cost and high density of the former with the high endurance and byte erasability of the latter are also possible, he says. □

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## THE QUEST FOR A HIGH-DENSITY EEPROM BEGAN OVER A CUP OF COFFEE

**The QPROM grew** out of a conversation that Gheorghe Samachisa, project manager, held in late 1984 over coffee with several members of Seeq Technology Inc.'s research and development group.

"We were talking about the technical papers that had been appearing describing various approaches to building high-density megabit EEPROMs," he says. "A number of them were highly imaginative designs. But all had critical flaws." One had small enough cells, but the process and transistor structure were too complex. Another had a simple structure but still was prohibitive to make. A third had the right balance of all these factors, but it was not reliable.

Samachisa remembers that at one point he groaned in frustration and burst out: "There has just got to be a simple way to design an easily erasable, nonvolatile memory cell that is as cost-effective as an EPROM but has all the features of an EEPROM." At that point, he began scribbling ideas on pieces of napkin and passing them to coworkers George Smarandoiu, Chien Su, and Ting Wong. It was several weeks before he came up with a scheme he thought might work, and several months working with staff process engineer Su to determine if the device could be fabricated.

Samachisa, 50, is a 1977 graduate of the Polytechnical Institute in Bucharest, Romania, with a doctorate in semiconductor physics. He was a professor of semiconductor devices there until joining Seeq three years ago to work on standard EEPROMs.

Smarandoiu, 41, is an engineering department manager for EPROM development. Before joining Seeq five years ago, he headed the semiconductor R&D Institute in Bucharest. From 1975 to 1977, he worked at Siliconix Inc., where he developed the first monolithic MOS codec. A 1969 graduate of the Polytechnical Institute, he received a master's degree in engineering from the University of California at Berkeley in 1978.

**RIGHT MIX:** Su, Wong, Smarandoiu, and Samachisa (from left) took Seeq's flash EEPROM from development to production.

Su, 37 and a graduate of the University of New Mexico in 1982 with a doctorate in electrical engineering, spent two years in the EPROM department at Intel Corp. before joining Seeq in 1984. The 36-year-old Wong, director of engineering in charge of special projects, has been with the company for four years. A 1977 graduate of the University of Pennsylvania with a doctorate in electrical engineering, he worked for six years in nonvolatile memory and static RAM development at Fairchild Semiconductor Corp. and Intel.

"The idea for the QPROM would not have occurred if we had only had experience in EEPROMs or just in EPROMs," Samachisa says. "What it required was an understanding of both, as well as a number of other memory technologies. It also required a company willing to take a risk on a new approach to nonvolatile memory."

Also contributing to the development of the flash EEPROM was Chenning Hu, professor of electrical engineering and computer science at UC/Berkeley, who served as project consultant.

For good ideas to come to fruition, says Samachisa, it "takes the right mix of expertise, within the company and within the design group. And that is what we had."

# THE DIGITAL PHONE NET FINALLY STARTS TAKING OFF

*Chip makers are beginning to turn out ICs, operating companies are coming up with detailed network specifications, and worldwide trials are beginning*

**by Robert Rosenberg**

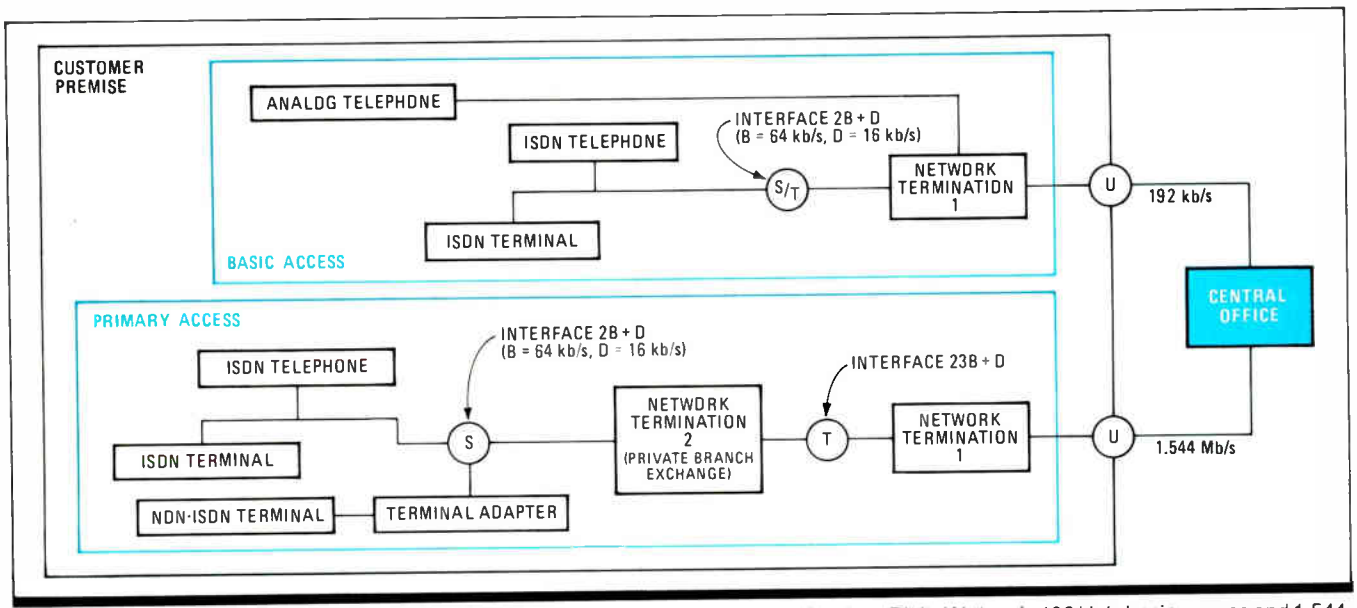
Just a few months ago, skeptics were muttering that ISDN, the brave new world of voice and data integration, stood for "I Still Don't Know." Details of the plan to substitute the integrated services digital network for the worldwide analog telephone system were fuzzy, and standards were being set too slowly. Now, however, the quickening tempo of developments is forcing the naysayers to change their tune.

Chip makers are starting to churn out integrated circuits to support the new terminal devices. In the U. S., Bell Communications Research is finally reshaping the International Telegraph and Telephone Consultative Committee's ISDN recommendations into hard and fast specifications.

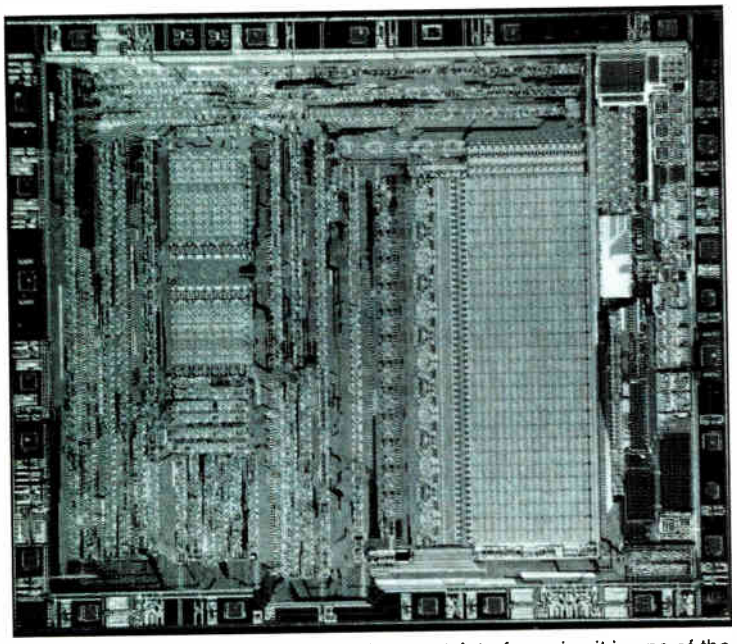
Around the world, local telephone authorities are scheduling ISDN field trials, though the U. S. is moving more slowly than Europe and Japan. In the meantime, the Bell operating companies are trying out ISDN-like telephone services that may be offered to customers eager for stopgap integrated voice and data channels.

But it takes more than the chip makers and the service providers to launch ISDN. The equipment makers have got to weigh in, too, and so far they have been very quiet about their plans. In fact, most of the naysayers on ISDN are equipment manufacturers—notably, terminal makers. They have been particularly critical about the lack of detailed network specifications, which must be set by the service providers.

For example, at the June International Com-




**1. ISDN PLAN.** The CCITT is setting standards for two types of service in the Integrated Services Digital Network: 192 kb/s basic-access and 1.544-Mb/s primary-access for large installations such as PBXs.



**2. RARITY.** Mitel's digital network interface circuit is one of the few U interface chips available. It is one of 30 ISDN chips that the company will be offering by year end.

munications Conference in Ottawa, one Bell Canada official remarked, "We wanted to evaluate the terminal market, so we issued a request for proposals and got back 350 responses." He said roughly a third of those answering said they were interested in supplying terminals to be used in an ISDN field trial, a third were not interested, and a third said, "What is ISDN?"

Why have terminal manufacturers been slow to embrace the ISDN concept? Part of the reason is the trauma resulting from the breakup of AT&T Co.'s local services into the seven regional operating companies. It has slowed the consolidation and implementation of the new standards.

## ISDN DEFINED

The ISDN's purpose, says the CCITT, is to put a worldwide all-digital network in place of the analog one. In the process, the ISDN will give users access to a broad range of new services in circuit-switched, nonswitched, or packet-switched modes available in 64-kb/s increments on a clear channel [*Electronics*, Sept. 30, 1985, p. 46].

The CCITT has already defined two types of communications channels from the ISDN central office to the user (Fig. 1). What is called the basic-access 192-kb/s channel will serve small installations. The primary-access channel will have a total overall data rate of 1.544 Mb/s in North America and 2.048 Mb/s in Europe and will serve installations with large data rates, such as those with PBXs.

In basic-access service, the interface between the customer premises and the central office, designated U by the CCITT, is the point where the 192-kb/s channel is divided in two 64-kb/s data- or voice-carrying channels, designated B channels, and a 16-kb/s signaling channel, designated the D channel. This allocation is commonly referred to as 2B+D and gives an effective channel capacity of 144 kb/s. The remainder is used for framing and other overhead signals.

In the CCITT formulation, the network termination point 1 converts the channels from the two-wire local-loop format to the four-wire format used on customer premises. The S and T interfaces provide the link to the customer's telephones and terminals. The S and T interfaces are identical for most practical purposes and are combined in the basic-access format.

In the CCITT's primary-access format, the North American 1.544-Mb/s channel is converted to 23 64-kb/s B channels plus a 64-kb/s D channel (23B+D). Europe will use a 30B+D format in its 2.048-Mb/s channel. In this format, the S interface provides the interface to the loop at NT1, the first network termination point, and the T interface provides the interface to the PBX.

With those specifications firmly set, the seven regional operating companies in the U.S. are starting to move. Their common research arm, Bell Communications Research, in Livingston, N.J., is beginning to give terminal-equipment vendors the answers to their interface questions. Bellcore promises that it will soon release a set of technical references for the ISDN basic-access format. With it, terminal vendors will have a clean interface to set up and release connections to the network.

Bellcore is advising the operating companies to support five basic-access services: speech, 3.1-kHz audio, 64-kb/s unrestricted data, a 56-kb/s service adapted to 64-kb/s unrestricted data, and packet-switched data. The Bellcore advisory also provides interface requirements between ISDN and non-ISDN lines in the same switch, an ISDN line and an interoffice facility, and an ISDN line and a public packet network. The next stage will be to specify primary-access service to PBXs and to calls between ISDN lines on different switches.

Bellcore's efforts are aimed at removing any ambiguity from ISDN interface specifications. This is important to terminal vendors because they have to design products around dozens of new chips. Advanced Micro Devices, AT&T Technology Systems, Harris Semiconductor, Mitel, Mostek, Motorola, National Semiconductor, Siemens, and SGS Semiconductor have already introduced or started shipping a number of ISDN products, and Intel is expected to announce its entries soon.

Advanced Micro Devices Inc. introduced its bipolar 7936 subscriber power controller in mid-June. It is touted as the only available chip that fulfills the CCITT power requirements for a line-supplied, regulated, 5-V-dc controller for the S interface. By year end, two new ICs will be in production: the 7938 quad-exchange power controller to take PBX line-card power and deliver it to as many as four subscriber lines; and the 79C31 controller to provide an interface between the PBX line card and the S reference point. Next

quarter, the Sunnyvale, Calif., company is promising full production of its 79C30 subscriber controller. The 79C30 and 79C31 are pin-compatible CMOS controller circuits for voice-data and data-only terminals, respectively.

In late July, AT&T Technology Systems, Berkeley Heights, N.J., announced availability of its S/T terminal interface, the first in a family of ISDN chip products. The T7250 Unite is a CMOS device, using 1.75-μm design rules, that will be up to full production later this year. It uses an on-chip High-Level Data-Link-Control (HDLC) formatter to manage the 2B+D channels. It is equipped with a general-purpose microprocessor bus interface and a simple interface to an external codec.

Harris Semiconductor Corp. is making its ISDN bow with the HC5590, a 160-kb/s two-wire transceiver for the U interface. The Melbourne, Fla., company developed the 5590 to accommodate alternate-mark-inversion coding of the ISDN signals. But with certain circles in the CCITT expressing growing interest in block coding, it is making provisions to handle either coding scheme.

Also planned for the U interface is the HC5532, a wide-band subscriber-line interface circuit for central-office line cards. A comparable SLIC for the S interface is the HC5530 power-feed. For both S and U interfaces, Harris is planning the HC5533, an intelligent power converter.

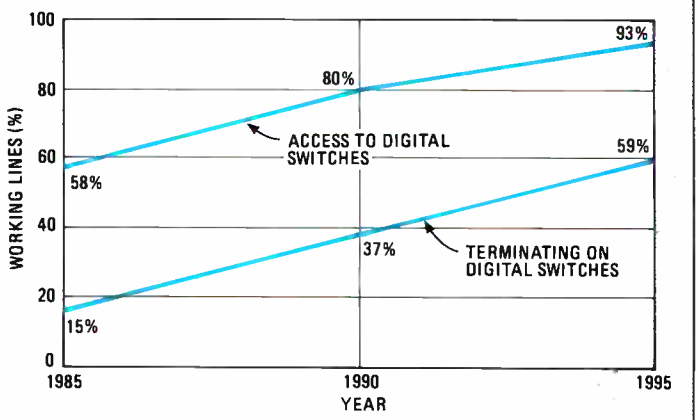
National Semiconductor Corp., Santa Clara, Calif., is coming out with a digital adapter for subscriber loops, designated the TP3400 DASL—a transceiver/echo canceler for PBX short-loop applications up to 6,000 ft. It will be available early in 1987. Also planned is the TP3410, a version for applications beyond this distance—up to several miles, in the case of some connections between the subscriber and the central office.

Another National IC, the TP3420 S interface, will be in full production in early 1987. This four-wire transceiver will meet the basic electrical specifications forming layer 1 of the open-systems-interconnection reference model of the International Organization for Standardization. Layers 2 and 3 of the seven-layer OSI model will be handled by the HPC16400, a 16-bit microcontroller for D-channel control, also to be available early in 1987.

Thomson Components-Mostek Corp. will soon introduce the MK5025, a packet-switching controller for LAPD (Link Access Protocol, Version D) applications for customer premises and the MK5027 for the central-office switch. In development are two chips for the S interface: an OSI layer-1 device, the TSG7610; and a layer-2 part, the TSG7620. The Carrollton, Texas, company also plans to develop chips for the U interface.

Motorola Inc.'s Semiconductor Products Sector, Phoenix, Ariz., has upgraded its line of universal digital-loop transceiver chips that link analog phones to digital line cards. The second-generation CMOS chips, the MC145421 and MC125425 demonstrated in early June, double the speed of the

**CANADIAN TELEPHONES GO DIGITAL**




devices, to 160 kb/s over 2 km. They provide two D and two B channels over a twisted-wire pair.

And in a move that is sure to worry other chip makers, Motorola announced in late May that it was joining with Northern Telecom Inc. to develop S, T, and U interface transceivers and a generic digital interface providing high-speed input/output for the transceivers. The S/T interfaces will be available in sample quantities later this year; samples of the U interface won't be ready till 1988.

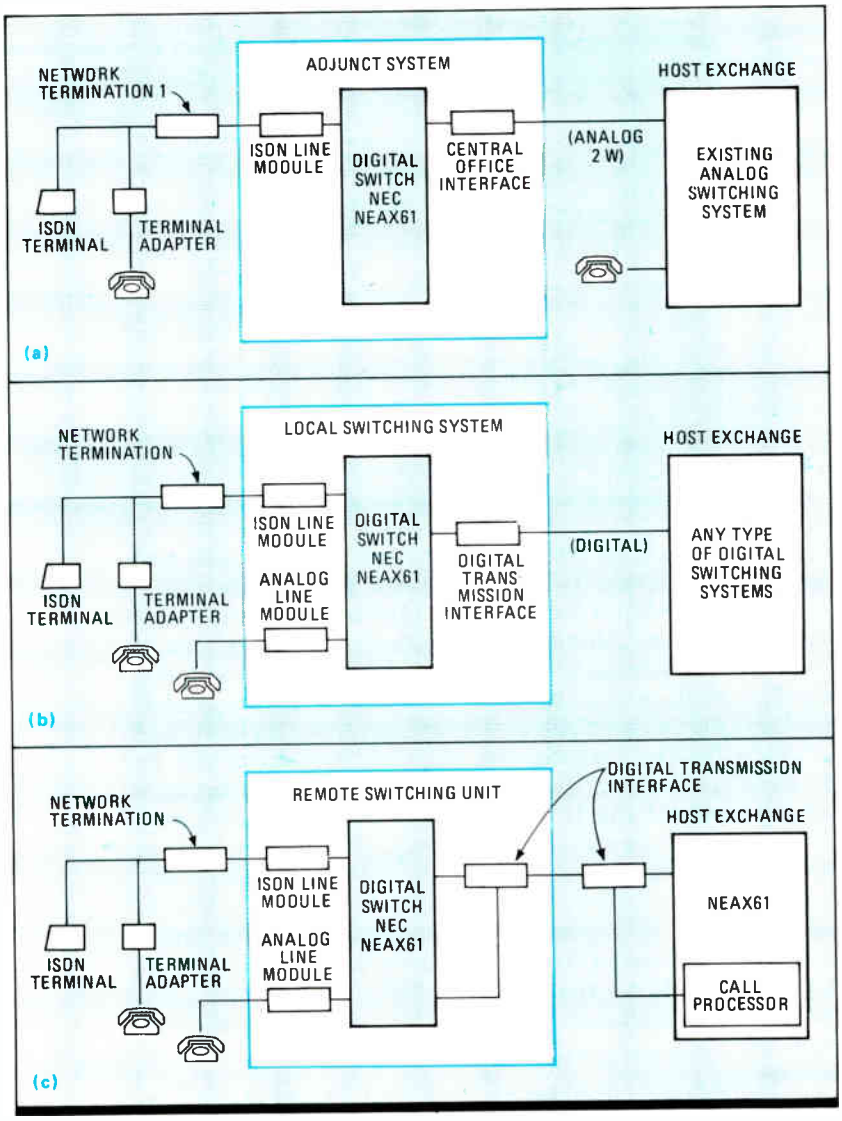
SGS Semiconductor Corp., Phoenix, is still in the early prototype stages of its S/T interface, and a finished chip should be available late in 1987. A U interface is further along. The prototype uses three gate arrays, and a final version should be ready by mid-1987.

Siemens AG is pushing into the U.S. and Cana-

*Most chip makers are starting slowly with just two or three ISDN products, but Mitel offers 17 ICs now and will introduce another 13 introduced by October*

dian markets with several very large-scale ICs designed for ISDN applications. An S interface, the SBC2080, has been available in sample quantities since the end of last year. Samples of the IBC2095 burst-transceiver circuit will be available early next year. And the IEC2090 echo-canceler circuit will be available in sample quantities in March 1988. All perform OSI layer-1 data transmission at the S and U interfaces. The ICC2070 ISDN communication controller—for layer-2 link-access protocol control—has been available in sample quantities since last year.

The Munich company is combining the 2070 and 2080 functions onto a single chip called the ISDN subscriber-access controller for the S interface. Samples will be shipped in September. A combined 2070 and 2095 ISDN subscriber-access controller for PBX applications will be available




**3. FLEXIBIITY.** The NEC NEAX 61E ISDN adjunct system changes its role to suit the needs of the central office. It can be adapted to an analog switch (a), a digital switch (b), or can serve as remote switch (c).

at the end of 1987. Samples of the 2160 codec will ship in mid-1987. The 2160, 2070, and 2080 will be combined into a digital telephone circuit; samples will be ready by mid-1988.

Samples of two high-voltage power controllers—the ISDN remote power controller for terminals and network terminations and a 40-V controller for the S interface—will be available in 1987. A high-voltage power controller for the exchange side of the local loop is also planned, but availability has not been set. These ICs use CMOS technology.

Mitel Inc., Kanata, Ont., Canada, has 17 products supporting ISDN and promises to deliver an additional 13 by October. The MT8972 U interface chip (Fig. 2), introduced a little more than a year ago, is already in volume production and being tested in undisclosed field trials in the U. S.

More recently, the 1.544-Mb/s T1 communications channel has been getting Mitel attention. The MT8974 digital trunk interface circuit permits mixing of T1 and high-speed serial data on the same link. Samples are available of a D-channel signaling controller, the MT8952B HDLC protocol controller, and samples of the MT8930 S interface will begin shipping in September.

With ISDN circuitry coming available, network providers are ramping up their efforts. The U. S. operating companies may be slow to start, but other countries' phone companies have jumped right in.

At Bell Canada, for example, Kim Markvorsen, ISDN service manager, says, "We think its [ISDN's] success is about 80% assured at this time." At this point, about 20% of Canada's phone customers are on digital exchanges, while 60% have access to digital switches, and those percentages are scheduled to rise dramatically (see graph).

Markvorsen says Bell Canada has completed testing the local loop and is testing ISDN hardware on captive central-office switches. By mid-1987, it will offer customer trials of an ISDN version of Centrex, the enhanced-services package provided from central-office switches. Centrex III will be available in the Ottawa area and will provide customers simultaneous access to the public phone network, the Canadian circuit- and packet-switched data networks, and Centrex lines specially conditioned for data. By early 1988, plans call for expanding Centrex III service to additional nodes in Toronto and Montreal as well as introducing ISDN basic-access service to non-Centrex customers in those cities.

In West Germany, the Bundespost will begin to test ISDN components and terminals later this year in Mannheim and Stuttgart. Testing will last for about 15 months, to be followed by first commercial implementations in the second half of 1988, says Joachim Claus, project manager of 64-kb/s implementations at the Fernmelddetechnisches Zentralamt in Darmstadt. "By 1990, we hope to have 70% of our commercial customers covered by ISDN," he says. Set for early commercial service are enhanced telephony, high-speed high-resolution facsimile, teletex, and 64-kb/s speech, data, image, and text transmissions.

In Japan, a homegrown version of ISDN, the Information Network System, is reaching 2,000 users in the Mitaka area and in part of central Tokyo. However, the INS is not fully compatible with the CCITT standards for ISDN. This year, Nippon Telegraph & Telephone Corp. promises to enhance its telephone offerings with such services as voice storage and credit-card calls. Nonvoice traffic such as facsimile is growing 50%

per year. NTT plans to launch commercial 64-kb/s circuit-switching later this year; by 1988, it plans to have a full system in place and make the cutover to the 2B+D signaling scheme defined by the CCITT.

In the UK, British Telecommunications plc launched its London ISDN trials last year and is extending them to Manchester, Birmingham, and a second exchange in London, says John Griffiths, head of the Digital Network Division, British Telecom Research Centre, Martlesham Heath, Ipswich. The present offerings are a single 64-kb/s B channel for the basic-access service and an 8-kb/s D channel, as well as 30 64-kb/s B channels for primary-access service, and they will be upgraded to the full CCITT specifications as new exchanges are cut over. By the end of 1987, over 180 exchanges will be providing ISDN services.

In the U. S., at least one operating company associated with each of the seven regional holding companies is scheduling trials. Among the holding companies, U. S. West seems to be leading with six ISDN field trials—the most ambitious being implemented by Mountain Bell in the greater Phoenix area. It will coincide with the 1987 International Switching Symposium, which is expected to draw upward of 2,000 attendees.

Beginning in November, Northern Telecom's DMS-100 central-office switch will provide 200 2B+D channels to the Arizona state government offices, Honeywell Inc., and Telegroup, a videotext information provider. Customers will receive voice calls on the B channels with access to non-ISDN voice channels. Circuit-switched data connections on the B channels will have a 64-kb/s clear channel to other ISDN links, and the 16-kb/s D channel will support signaling and packet switching. Later, full B-channel packet switching will be made available. By late 1987, service will be increased to more than 1,000 lines.

GTE Corp., Stamford, Conn., will become part of the Phoenix trial in December, when Mountain Bell will test a GTD-5 EAX digital switch for basic- and primary-access ISDN performance. The 23B+D primary channel will link a GTE Omni PBX at GTE corporate offices in Phoenix to the EAX switch in a central office.

An AT&T Technologies 5ESS digital switch will be added to the trial network in February 1987 and linked to an optical remote switching module using fiber optics. Users will have access to about 50 2B+D lines for voice and circuit- and packet-switched data.

Local operating companies have an alternative to investing a bundle to upgrade to full ISDN capabilites: they can can test the market for ISDN-like services. NEC America Inc., Melville, N. Y., and Lear Siegler Inc.'s Electronic Instrumentation Division, Anaheim, Calif., are offering digital upgrades to existing central-office technology.

The NEAX 61E adjunct system from NEC is a reworked version of the company's NEAX 61 central-office switch. It can provide both basic- and primary-access services for both circuit- and packet-switched data networks.

The adjunct resides between existing central-office hardware and the local loop and handles anywhere from a few hundred to several thousand lines. The design is modular and can be upgraded by replacing the type of interface between the adjunct and the host central-office switch (Fig. 3). NEC is providing its 61E adjunct to Mountain Bell for field trials in Denver and to Pacific Bell as part of the three-city ISDN demonstration planned for San Francisco, San Jose, and San Ramon.

Lear Siegler also has an eye on local operating companies eager to cash in on the market for enhanced services. It is pushing its VAD 9600 simultaneous digital voice and data system, a multiplexer aimed to provide enhanced service over existing voice-grade lines. Within a single 64-kb/s digital time slot, the VAD 9600 provides a 19.2-kb/s data channel, a 1.2-kb/s low-speed data channel, and a 32-kb/s pulse-code-modulated voice channel. The company plans an upgrade that will adapt the VAD 9600 to ISDN.

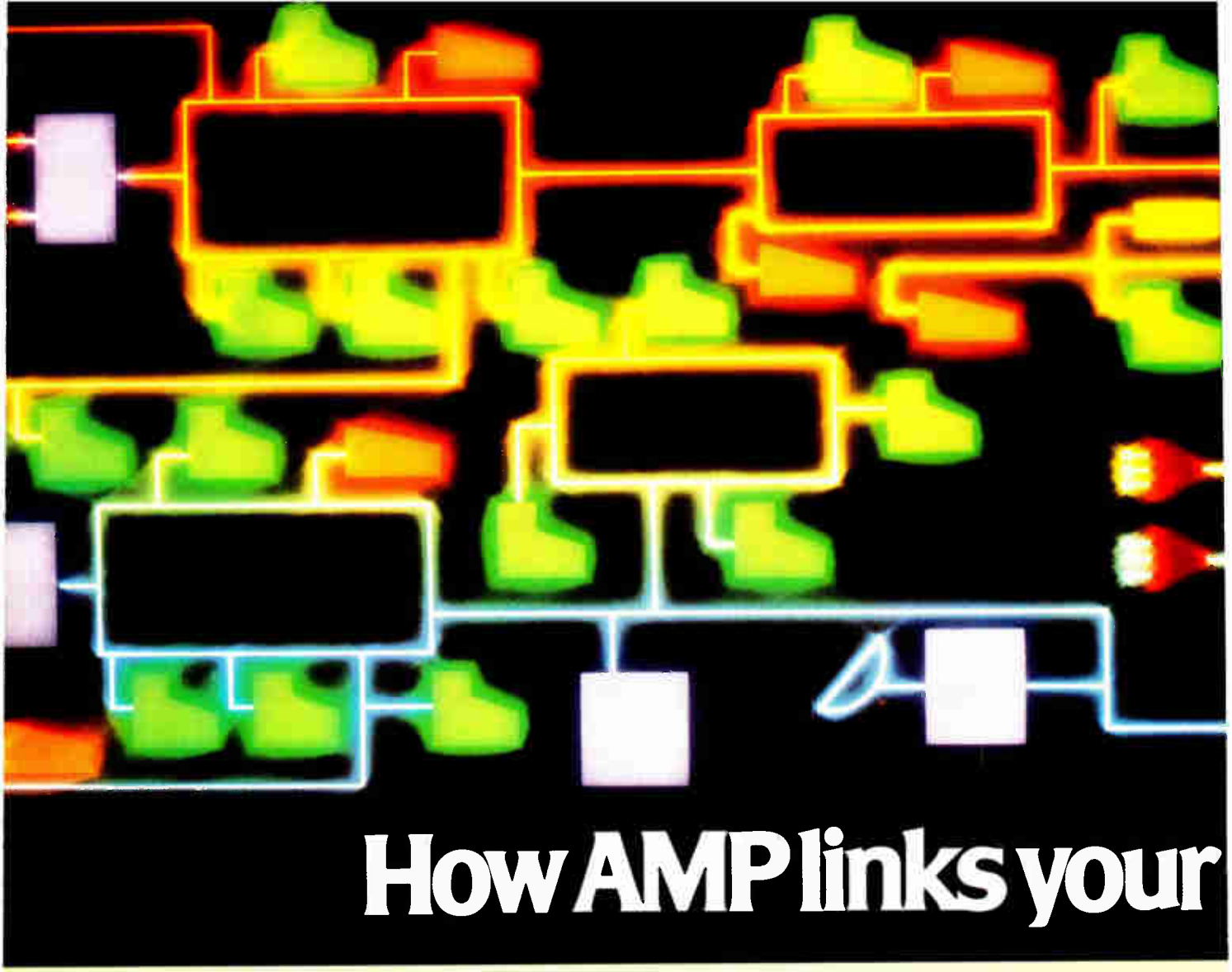
Pacific Bell's Project Victoria is another ISDN-like service that converts an existing line into seven simultaneous communications channels.

*Local operating companies may not wait for the all-digital network; they're investigating ISDN-like services that upgrade existing central-office switches*

The system consists of digitizing and multiplexing transceivers at either end of the local loop.

During the initial field trials, the customer side is being supplied with a remote multiplexer. It provides subscriber access to multiple, logically independent digital channels. Initially each device will support two voice channels, one medium-speed (up to 9.6 kb/s) asynchronous data channels and four low-speed (up to 1.2 kb/s) asynchronous channels. Pacific Bell's Project Victoria design team is readying a smaller unit with integrated power and battery that will support four terminals. At the central office, the Victoria hardware is compatible with existing analog and digital hardware and routes data between local loops and the gateways supporting RS-232-C and X.25 ports.

Project Victoria—like the ISDN field trials—will be watched carefully by U. S. terminal vendors who will be looking for confirmation of their belief that ISDN is pie in the sky. To semiconductor manufacturers and network suppliers who have already made the leap of faith toward ISDN, the trials will be crucial tests of both network performance and the marketability of enhanced services. □



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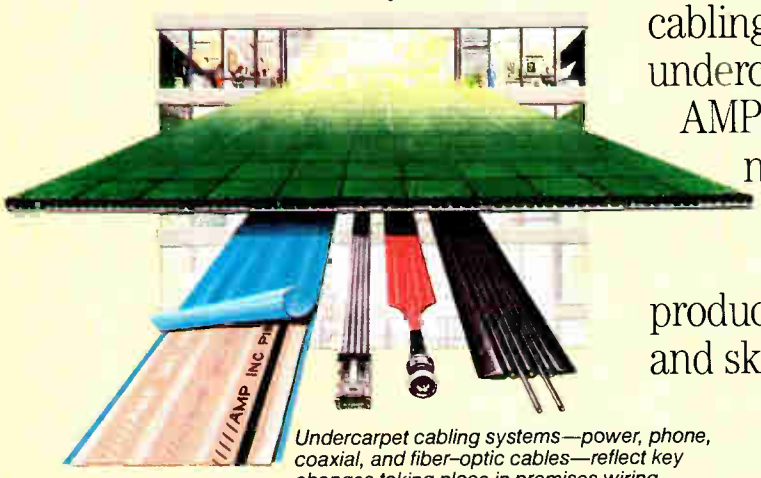


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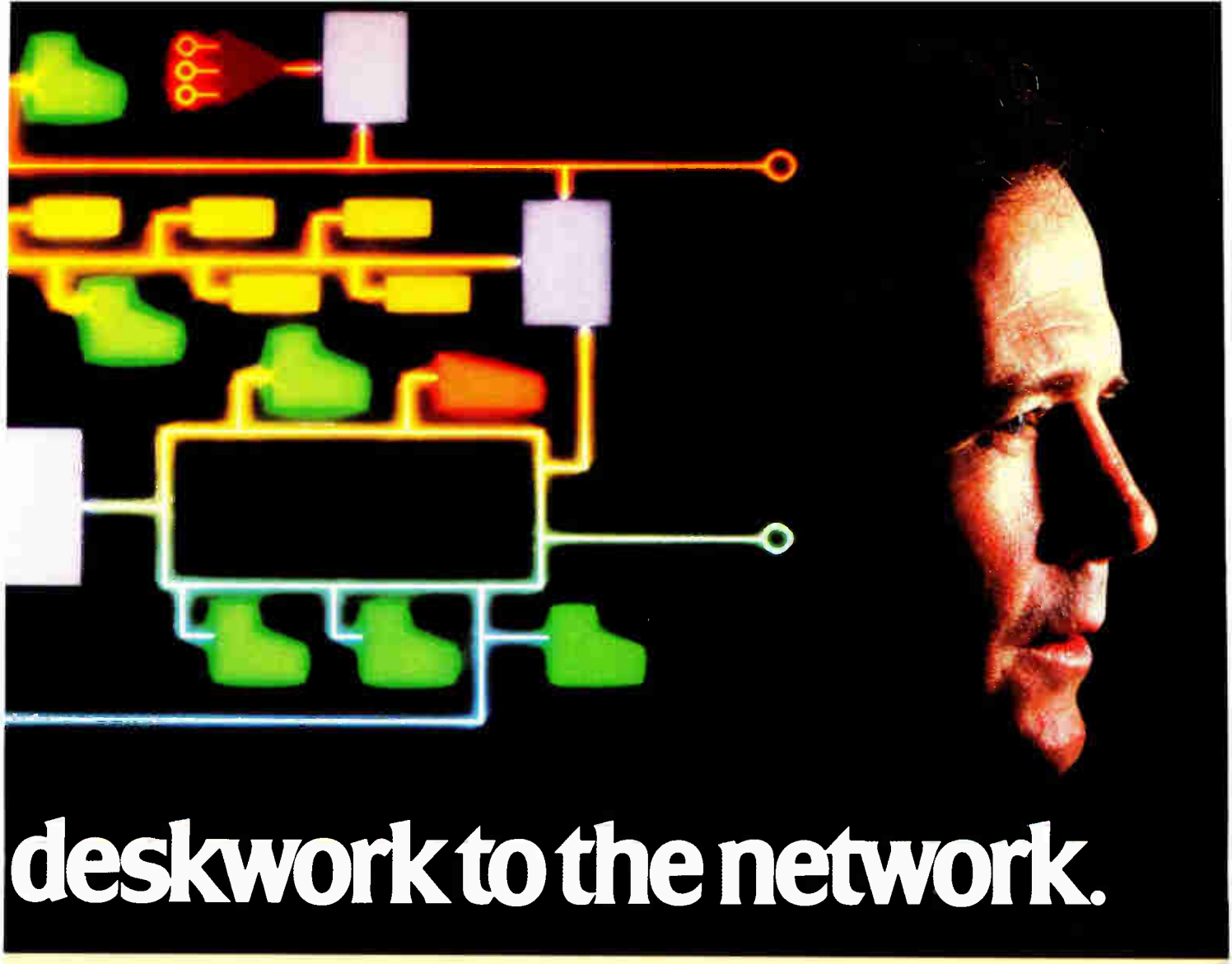

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# DSP BOARDS HELP TACKLE A TOUGH CLASS OF AI TASKS

*Multiple digital signal-processing ICs running at up to 320 mips join with a Lisp work station to meet demands of jobs such as speech recognition and synthesis*

Work stations are a hot item in the world of artificial intelligence, as AI moves from the research laboratory into the realm of practical technology. Likewise, new digital signal-processing chips are hitting the market with increasing frequency. But until a current project at Texas Instruments Inc. got under way, no one had attempted to combine the two fast-moving technologies.

TI has combined them in Odyssey, a prototype digital signal-processing board that runs under the control of TI's Explorer AI work station. Users can pack as many as 16 Odyssey boards into a system, thanks to a flexible interface bus, and can execute 320 million instructions/s written in Lisp, Forth, or assembly language. That kind of power and flexibility can tackle a whole new class of AI tasks, says Richard H. Wiggins, director of the Speech and Image Understanding Laboratory at TI's Computer Science Center, Dallas.

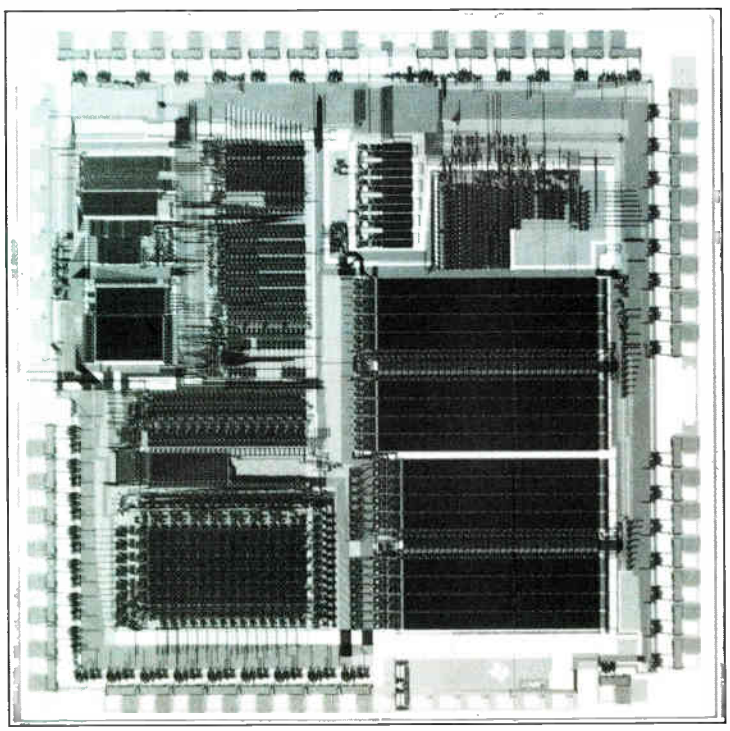
At the head of that class are tasks that require real-time processing in an AI environment, such as speech recognition and synthesis. Handling the challenge of real time is well within the capabilities of the powerful TMS32020 DSP chips (Fig. 1) at the heart of the Odyssey board.

Introduced in early 1985, the TMS32020 boasts a cycle time of 200 ns. It can execute a 16-bit pipelined multiply-and-accumulate operation in 200 ns; a 32-bit floating-point multiplication in 7.8 μs; and a 256-point complex fast Fourier transform in 6.9 ms. Internally, the 32020 features a 32-bit Harvard architecture, with a 16-bit external interface.

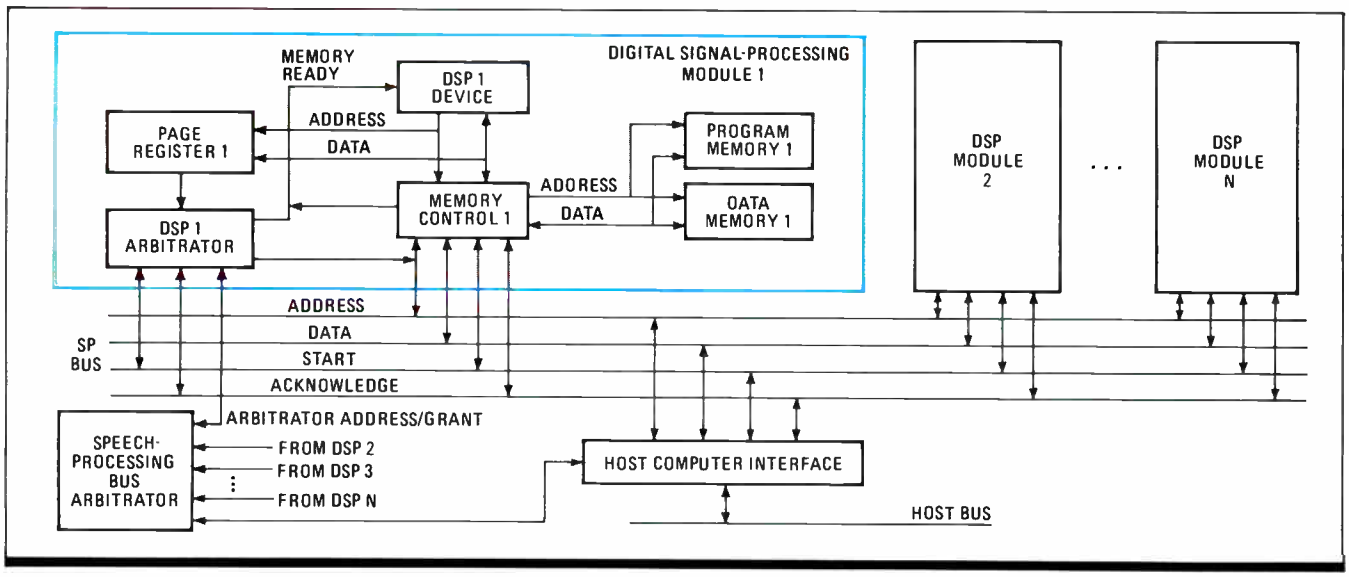
With four 32020s per board, Odyssey is a powerful, dedicated signal-processing computer that performs parallel processing. When operating in the local-memory mode, each Odyssey processor can execute separate algorithms.

On each Odyssey board (Fig. 2), three 32020s run user applications software. Each processor carries 8-K by 16 bits of high-speed static random-access memory, which holds the program memory. Data memory resides in 64-K by 16 bits of dynamic RAM.

The fourth 32020 has 16-K by 16 bits of pro-



**1. SIGNALS.** The TMS32020 digital signal-processing chip at the heart of TI's Odyssey board features a 200-ns instruction cycle.




**2. QUARTET.** The Odyssey architecture uses four TMS32020s, three to run applications software and the fourth for I/O processing.

gram memory and functions as an input/output processor, incorporating two I/O ports. The first is an 8-bit codec port. The second is a standard external port for data acquisition that has a capacity of 10 megabytes/s. A signal-processing bus links the four 32020s together, allowing the high-speed transfer of 16-bit data words.

The Odyssey board connects to the Explorer through a host-computer interface. In contrast to conventional work stations designed for numerical data processing, the Explorer's architecture is optimized for the execution of Lisp, an AI programming language.

The Explorer supports up to 16 megabytes of RAM and up to eight 140-megabyte (unformatted) Winchester disk drives for on-line mass data storage. A data-communications package implementing the Transmission Control Protocol/Internet Protocol allows the Explorer to connect to other computers through a local-area network.

## INTERFACING ODYSSEY

The Odyssey interfaces with the Explorer through TI's proprietary NuBus architecture. NuBus provides expandability, an important factor in the Odyssey-Explorer marriage. It is the key to Odyssey's utility as a parallel signal-processing computer. The NuBus lets the Explorer host up to 15 additional Odyssey boards, for a total of 64 TMS32020 chips.

The expandable NuBus "is a true extension of the system in that one processor on one board can talk directly to the memory of a processor on another board, just as it can to the processors that are on its own board," says Richard T. Tarrant, senior member of the Computer Science Center's technical staff. "In effect, all memory—both program and data memory—of the 32020 becomes global memory to another processor, such that it can read and write to it."

Because all memory, command, and interrupt functions are memory-mapped across boards, a single 32020 on one Odyssey board can access the data memory of any other 32020 on any of up to 16 Odyssey boards. It can use that memory as an extension of its own.

This bus structure allows considerable flexibility in design applications for the system. "Because the multiple boards can communicate independently of the host machine, you can modularize your algorithm and distribute it among the processors to run autonomously, but to pass data in a very efficient manner—all independent of the host. And you can program these processors independently to do different functions," explains Tarrant. Data can be transferred between processors at more than 2 megabytes/s.

Taking Odyssey's expandability to its 16-board limit results in an extremely powerful machine. The 320-mips muscle from a fully configured system is precisely what scientists in areas such as speech processing need to advance their research.

To develop the speech-recognition systems of the future, researchers must have machines that can run in the 100- to 1,000-mips range, Wiggins says. "Each TMS32020 is capable of doing 5 million multiplications and 5 million adds/s," he says. "That's a total of 10 million arithmetic operations/s if you count the multiplications and additions separately, each one of those being a 16-by-16-bit multiply, and each add being a 32-bit add of the result per processor. With four of these systems on a board, you can get 40 million arithmetic operations/s. So with 16 of these, you can provide 640 million arithmetic operations/s.

"You can see what the future is going to hold when you have devices that have a 100-ns cycle time, instead of 200 ns [of the 32020]. You'll be able to provide potentially something over 1,000 mips."

Wiggins sees three types of applications

where high-powered Odyssey systems will likely see service: dedicated DSP applications, research, and systems development. One example of a dedicated DSP application would be speech recognition and synthesis. Here, an Explorer might act as an expert system while the Odyssey board functions as a dedicated voice I/O system, performing the required speech recognition and analysis to communicate with the user.

## SPECTRAL APPLICATIONS

Spectral analysis would be another dedicated DSP application. Odyssey would collect and analyze signals of some kind—for example, audio, video, or radar-return signals—and pass along the results to the host AI machine.

Most research applications also involve collecting and analyzing signals of one kind or another. Good candidates include speech processing, underwater acoustics, image processing, and many medical applications, such as interpretation of electrocardiogram signals.

To develop software for those applications and more, users will have four basic software-development strategies at their disposal. They are: writing Lisp programs to control Odyssey from the host Explorer; programming the Odyssey in Forth; using an assembler and linker to write assembly-language programs for Odyssey; and using a multiprocessor debugger to verify 32020 programs.

Lisp-callable routines running on the Explorer allow the host to control Odyssey. The available routines are device-service routines that initiate both board- and processor-level functions. Board functions include reset, open and close I/O channels, and execute self-test. Processor functions include reset, allocate/deallocate, download program/data, upload program/data, execute self-test, and get status.

TI developed a Forth interpreter to allow Odyssey users to write programs in that high-level language. The user can download the interpreter directly into any of the four 32020s on the Odyssey board and use it to execute standard Forth 79 programs. The user can also define extensions to the Forth 79 instruction set. In addition, Forth programs can run in conjunction with 32020 assembly-language programs—Forth programs may contain calls to 32020 assembly-language routines.

An assembler and linker are also available for developing programs in the 32020 assembly language. The programs may be developed on a Digital Equipment Corp. VAX minicomputer or an IBM Corp. Personal Computer and then transferred to Odyssey.

TI has designed a special Lisp-based debugger for use with Odyssey. Running on the Explorer, the debugger features four windows to simultaneously display the software status of all four 32020 processors on the Odyssey board.

The debugger can display the contents of data and program memory, internal data and registers, and provide a reverse assembly of program memory. With it, the user can modify the contents of all registers and memory locations before resuming program execution. The debugger can also be used to set breakpoints. A reverse assembler displays program memory address and machine code as well as assembler mnemonics. A trace mode is also available. □

## SPEECH APPLICATIONS DRIVE ODYSSEY DEVELOPERS

**Powerful digital** signal-processing systems such as Odyssey may well be the answer to the prayers of speech scientists. "We can do processing today that years ago required much, much larger systems," says Richard H. Wiggins, director of the Speech and Image Understanding Laboratory at Texas Instruments' Computer Science Center.

Wiggins' involvement in speech processing dates back to 1966, when large racks of equipment were needed to perform even pedestrian tasks. He joined Mitre Corp. to design voice-communications systems. That led to work on digital signal processing and the mathematics of analyzing speech. Wiggins, 43, joined TI in 1976, working on speech-processing projects as a member of the Speech Research Group, including the design of the speech system for TI's ground-breaking Speak & Spell [*Electronics*, June 22, 1978, p. 22]. He managed the Odyssey research project from September 1984 until last February.

WIGGINS

McMAHAN

Mike McMahan, head of the Computer Science Center's Systems and Applications branch, now manages Odyssey research. He joined TI in 1968 as a speech-systems engineer and in 1980 moved to TI's Semiconductor Group, where he worked as technical liaison between the corporate speech-research and chip-development organizations. Since 1982, he has worked in the corporate speech-research organization.

Richard T. Tarrant designed Odyssey's host interface. A digital systems designer by training, he once worked on the hardware design for TI's 99/4 home computer. He joined the Odyssey project direct from his involvement with TI's Speechboard Processor.

Wanda Gass developed the multiple-processor end of the hardware design. She joined TI in 1980, armed with an MSE from Duke University and a BSEE from Rice University. At TI, she set to work in the Semiconductor Group. Her first assignment was as design engineer for the TMS32010, the first chip in TI's TMS320 DSP family.

TARRANT

GASS

# HERE COMES A BETTER WAY TO WIRE UP AN AUTO

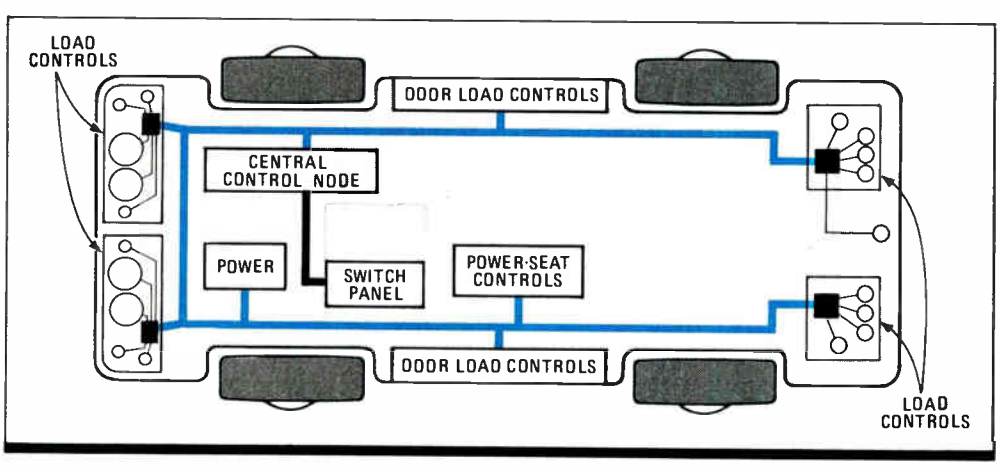
*Motorola couples multiplexing with microprocessors for greater flexibility and control and to save weight and space over conventional auto wiring harnesses*

Conventional automotive wiring systems are going the way of the dinosaur, now that falling semiconductor prices have made digital control systems economical enough for standard vehicular use. Motorola Inc.'s Semiconductor Products Division thinks a likely replacement will be a multiplexed system built around single-chip microcomputers. It has designed such a setup, using an optical link between the driver's controls and a central microcontroller and a twisted-pair global bus between that microcontroller and remote control nodes.

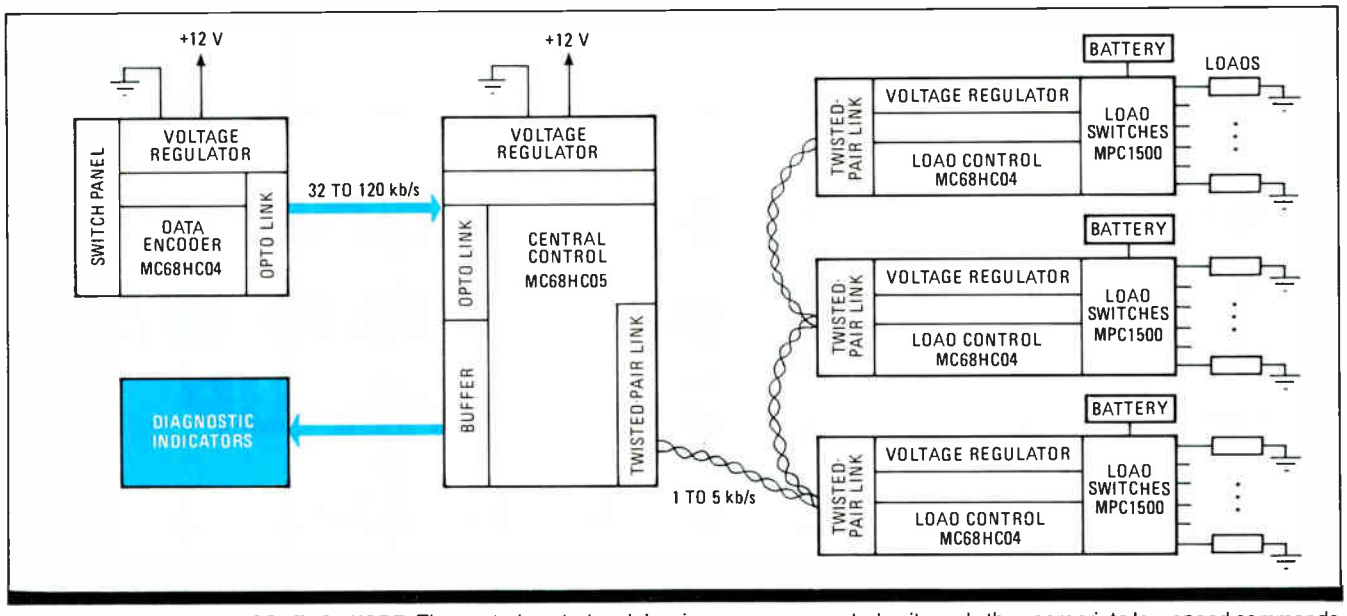
Almost every car on the road uses a complex point-to-point system in which high-current wiring is strung throughout the vehicle, from the battery to the dashboard and steering column switches and then through a fuse box to the loads—lights, wipers, and so on. The Motorola system replaces this with a low-voltage control network and direct high-current wiring from the battery to the loads. It offers critical advantages: lower weight, reduced bulk, easier addition of accessories, and simplified troubleshooting. In addition, fiber-optic components make it possible to build a reliable electrical power system with increased bandwidth and immunity to electromagnetic interference.

Motorola calls its setup a "generic mux system" because it is not intended for a particular make of automobile and because automakers are already using the term "mux" for such wiring schemes. In fact, carmakers are already implementing the concepts of the generic mux system (see story, p. 81).

Motorola's setup (Fig. 1) has three basic subsystems: the driver's switch panel, probably in the steering wheel hub; a central control node; and remote intelligent load-control nodes. A one-way optical link runs from the switch panel to the control node, and a twisted-pair multiplexed bus links the central node and the remote nodes. Such a system needs a microcontroller in the central control node. Motorola's Richard J. Valentine says the intelligence needed at each remote node can be either less-power-




**1. TWO BUSES.** Motorola's generic mux bus uses a fiber link between the switch panel and the central control node plus a global twisted-pair bus serving the control and remote control nodes.




**2. CENTRAL CONTROL NODE.** The central control node's microprocessor control unit sends the appropriate low-speed commands out over the system's twisted-pair global bus, from which they are routed to the remote nodes, which include some sort of intelligence.

ful microcontrollers or else hard-wired logic.

A multiplexed bus promises significant improvements in reliability, installation, and servicing, thanks to a greatly simplified wiring harness and built-in diagnostics. "An owner of a mux-wired vehicle is going to have a more reliable electrical system because the system is going to have fewer wires," says Valentine, a systems design engineer working on advanced automotive system designs at the Phoenix, Ariz., division. "And the manufacturer is going to have an easier system to install with sophisticated diagnostics built in."

One level of system diagnostics is aimed at the driver, displaying information indicating whether there's a fault on the sensor that monitors the circuit. A second level is aimed at the mechanic.

## SIMPLER DIAGNOSTICS

"In present wiring systems, the wire harness usually has to be cut open in order to locate the source of a wiring fault, and a bad wire may run throughout a vehicle," explains Valentine. Because the mux-wiring concept uses a direct-to-load-center electrical-power distribution system, a fault can be pinpointed to a quadrant of the vehicle. "With enough intelligence in the load-control nodes or central control node, it is possible to give the technician a single simple diagnostic procedure," Valentine says.

To keep the system affordable, Motorola uses twisted-pair wires for the global bus, but future systems could use an optical bus with passive splitters or tees with bidirectional optical emitter and detectors, Valentine says. This type of optical communications network offers enough bandwidth to handle high-speed requirements, such as digitized audio for voice recognition, or low-data-rate information, such as engine-control sensor data.

The central control node manages much of the automobile's electrical system (Fig. 2). Data transmitted from the switch panel is received either on a periodic basis or per switch hit. The microcontroller interrogates this data and sends out the appropriate low-speed commands over the twisted-pair bus. The remote nodes receive these commands and take whatever action is required.

For example, when the driver switches on the headlights, a message goes immediately to the central control node by means of the optical link. The node's microcontroller verifies that the headlight switch is on and checks for other interactive switch commands, such as a high-beam request. In this case, global messages such as "Headlamps on" and "High beams off" are transmitted at a low data rate to all nodes.

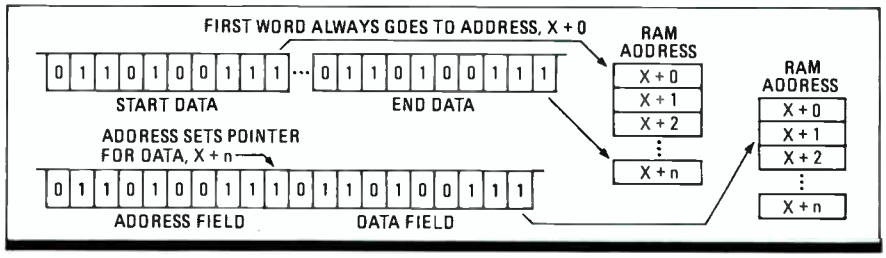
A global system bus can be built with zero data collisions, but such buses are significantly slower because the central-control-node unit must poll each remote node separately before proceeding to the next. Instead, Motorola's mux system uses a software bus-arbitration scheme.

For example, if the central control node sends out a diagnostic request to all the remote nodes, then each node responds with a minimum 1-byte message. Because the first node can respond with a lengthy reply if several faults are detected, the remaining nodes will have to wait before accessing the bus. A bus-idle detector routinely strobes the bus every 6 to 24 $\mu$s, depending on the microcontroller crystal frequency. If a zero level is detected (bus busy), the detector resets itself for another 4- to 10-ms idle. A bus collision can occur when a remote node is just starting to transmit a diagnostic message back to the central control node and that node has just processed a user switch-update request.

Motorola uses a twisted-pair bus and differen-

tial transmitters and receivers to minimize EMI pickup. The central control node's serial communications interface (SCI), in the "twisted-pair link" block of Fig. 2, uses an advanced error-detection method to minimize bit errors.

The data protocol that is implemented on the communications link depends on the system's size and the total number of components to be controlled. Because Motorola's system is generic, two protocols are possible.




**3. SERIAL FORMATS.** The top protocol uses minimal program overhead but ties up the bus. The bottom format uses more overhead but less serial bus time.

One protocol is a serial data format with minimal program overhead, in which the SCI program stores all incoming data in sequential locations in random-access memory (Fig 3a). It takes anywhere from 1.3 to over 5 ms to transmit 16 bytes, depending on the SCI bit rate (120 to 32 kHz) and whether 10- or 11-bit data words are used. This protocol is useful for relatively simple systems with uncomplicated messages.

The other protocol, which Motorola uses in its generic mux design, requires that the program test each incoming word for a specific address and then store the bits at that address (Fig 3b). The program decodes the address and updates the correct RAM location. Only a minimum message is required to update one entity. This protocol has more overhead but less serial bus time. To implement this protocol, the microcontroller must be fast enough to process and set up the address pointer before the next word fills the SCI data register. Using a bit rate of 2.4 kHz, this implementation leaves only about 4.2 ms for the microcontroller to determine the address and store the data to that address.

The generic mux network uses an 8-bit data word with 5 address bits, 2 data bits, and 1 bus-priority bit. The SCI controller adds the start and stop bits plus an optional ninth data bit. The 5 address bits allow 32 unique codes, which can include up to 4 subsets per the 2 data bits. The bus-priority bit arbitrates bus transmission collisions between the central control node and the remote nodes. This 8-bit data format allows 128 central commands plus 128 remote diagnostic responses.

As the microcontroller for the central control node, Motorola chose the MC68HC805C4, which has a 4-K electrically erasable programmable read-only memory. "In our application, an EEPROM provides a space for storing diagnostic data even if the battery is disconnected," Valentine explains. "The EEPROM also provides a convenient way to add field updates or options." If a dealer adds an accessory, the command library could be updated easily.

The Motorola generic system uses MC68HC04 microcontrollers in each remote node. Like the central microcontrollers, these chips have 8-bit data buses, but their program memory is limited to 1-K of ROM. Another key semiconductor device is the load switch. Each remote load-control node will have a number of these, one for each load. Motorola and other semiconductor manufacturers have been developing power devices with built-in fault protection for automotive load switching. For example, Motorola's MPC1500 offers high side switching plus short-circuit protection and a diagnostic status line. It is connected between the battery and the load and can be used to control loads such as tungsten lamps, which need high inrush currents. Not only is there no need to run the high current wires through the dashboard switches, but there is no need to run them through a fuse box.

A setup like the generic mux system can be realized today. What will make it commonplace is more affordable optical components and a new generation of semiconductor and multifunction power devices with improved self-testing. □

## TEENAGE TINKERING LED TO WIRING CONCEPT

**It may have been** skinned knuckles or getting grease past the elbows that gave Richard J. Valentine his mission: help Detroit build an automobile that's easier to service. The 41-year-old systems design engineer who developed the automotive multiplexed wiring system at Motorola Inc.'s Semiconductor Products Division says his memories of working under, around, and through the engine compartments of jalopies as a teenager remain vivid.

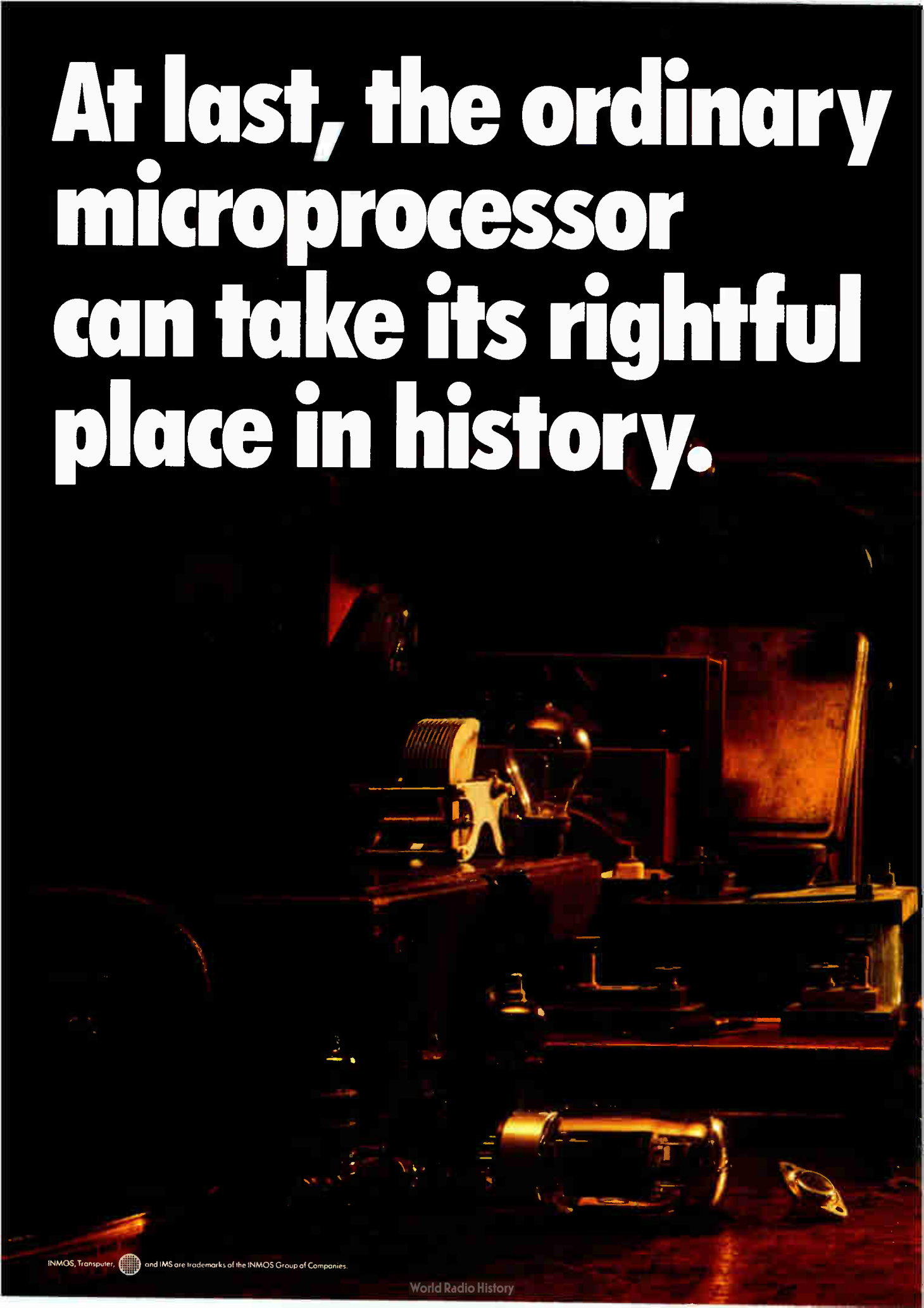
Nowadays, though, he says it is impossible for the owner to work on any car with electronic ignition—and that's a problem. "I keep trying to get the automobile manufacturers to design a car that can be fixed by you and me," says Valentine.

**VALENTINE**

But because electronics suppliers wield as much clout with the auto industry as makers of nuts and bolts, it may be a while before a full diagnostic checkout will be within reach of the backyard mechanic. "Some day, you may be able to plug your personal computer into the serial port of the diagnostics module to do all your own maintenance," Valentine says. "Take the engine-control module. If you have a data network, you should be able to tap into it and poll each system and check its health."

Valentine says that about half the automotive electronics modules recently returned for repair were fully operable. He says that when automakers discover that self-test and full diagnostics in electrical modules are cost effective, the concept will become reality.

# At last, the ordinary microprocessor can take its rightful place in history.



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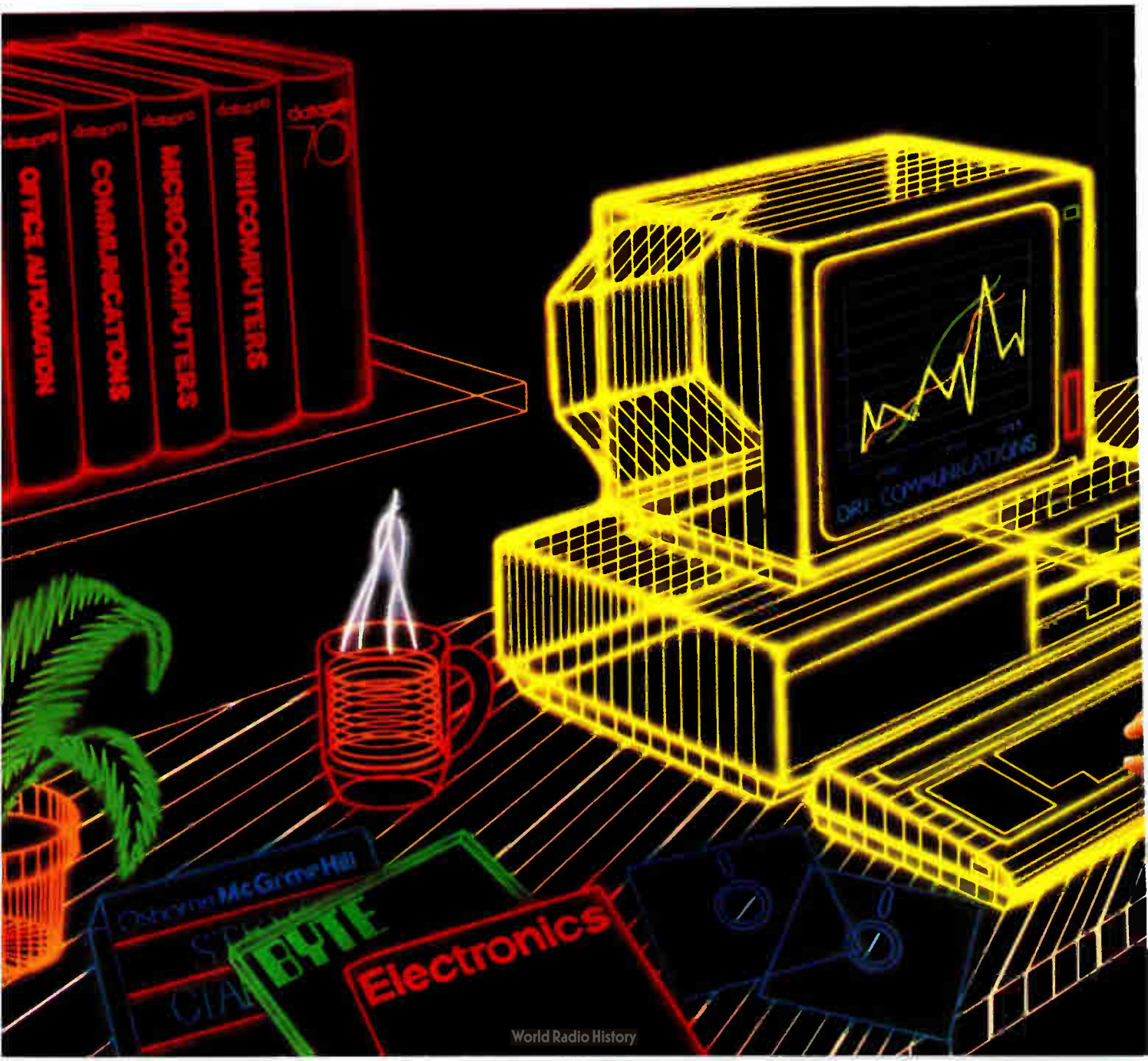

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# NATIONAL'S BIG GAMBLE IN AUTOMATED PACKAGING

*The Odyssey flexible assembly line will go into full operation by mid-1987; it can reconfigure itself to handle different chips and a variety of assembly methods*

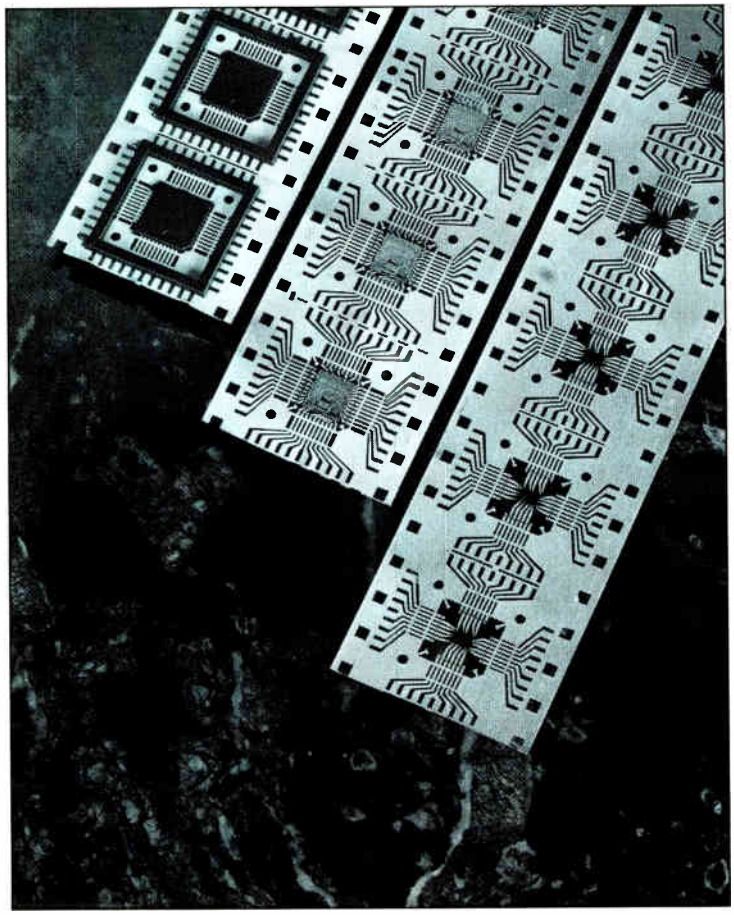
**by Jerry Lyman**

At least one major U. S. semiconductor maker is getting set to gamble on a fully automated, flexible packaging line as a way of radically reducing production costs. National Semiconductor Corp.'s Odyssey assembly line is scheduled to go on stream in mid-1987 and start turning sorted wafers automatically into packaged chips. If it works as planned, Odyssey will fulfill chip makers' dreams of a truly flexible assembly line, for it is designed to reconfigure itself to handle different chips and varying package types.

Among the package types it will accommodate is a new product that National believes is the next step forward in tape-automated bonding: Tape Pak. A miniaturized plastic leaded package, Tape Pak (Fig. 1) grows out of the Santa Clara, Calif., company's continued drive for high reliability and low cost in package designs. Now it is gearing up Odyssey to handle Tape Pak and other package types.

National calls Odyssey one of the first automated flexible manufacturing systems for integrated-circuit assembly, transforming what are usually individual batch processes into a generalized manufacturing line. Sorted silicon wafers fed into the system will emerge as fully assembled and tested chips. The system will use a variety of assembly techniques to produce a plethora of package styles: plastic, ceramic, and CerDip dual-in-line packages; plastic leaded chip carriers; ceramic leadless chip carriers; and small-outline IC packages. "Odyssey's virtually automatic assembly represents the future of flexible manufacturing for the entire chip-making industry," says Martin Petraitis, director of automation and tape products.

One market analyst also sees it as a possible response in the near term to what he calls confusion in the market. "The market today is in the middle of nowhere, where it is difficult to see clearly in any direction," says Charles-Henri Mangin, president of Ceeris International Inc., Old Lyme, Conn. "Everyone's predictions have been so wrong—in computers, defense, test—that it is difficult to tell what equipment to buy. A flexible line such as Odyssey, which can turn



**1. NO HANDS.** In Tape Pak assembly, a copper-bumped tape is the lead frame for a testable IC package suited to automated assembly.

out short runs on short notice, could remove many uncertainties," in Mangin's view.

It also will help hold down inventories, he says, meaning that producers and users alike will not have to "eat parts that become obsolete quickly." Mangin says that flexible automation should prove particularly valuable when small lots of expensive parts have to be handled—for example, a $50 microprocessor. But in that regard, flexibility has a price, he cautions. "For shorter runs, you usually need excess capacity in terms of equipment, because there are more setups and idle equipment," Mangin points out.

Essentially, Odyssey consists of an automated handling system paired with intelligent processing machines (Fig. 2). To make the system self-configuring, these two functions are tied together through a computer hierarchy run by a Digital Equipment Corp. VAX superminicomputer. The setup is designed to work with minimum inventory, since many materials are common for different package styles.

Once a wafer is sawed into chips, the system-control computer makes priority decisions about where to send them, first taking into account which processing machines are free. The processing machines carry out their operations on the chips or packaging materials fed them under computer instruction. Then they pass the instruction back to the handling system. It, too, has intelligence to control its looped conveyor belts and the elevators that receive and deliver materials.

To keep the hierarchy flexible, DEC and National are developing a variety of software modules. Some will control materials schedules and handle the priority instructions for the processing machines. Others will oversee the overall work flow and the movement of materials. Software will also allow the factory to reconfigure the system to take advantage of available resources in light of current needs.

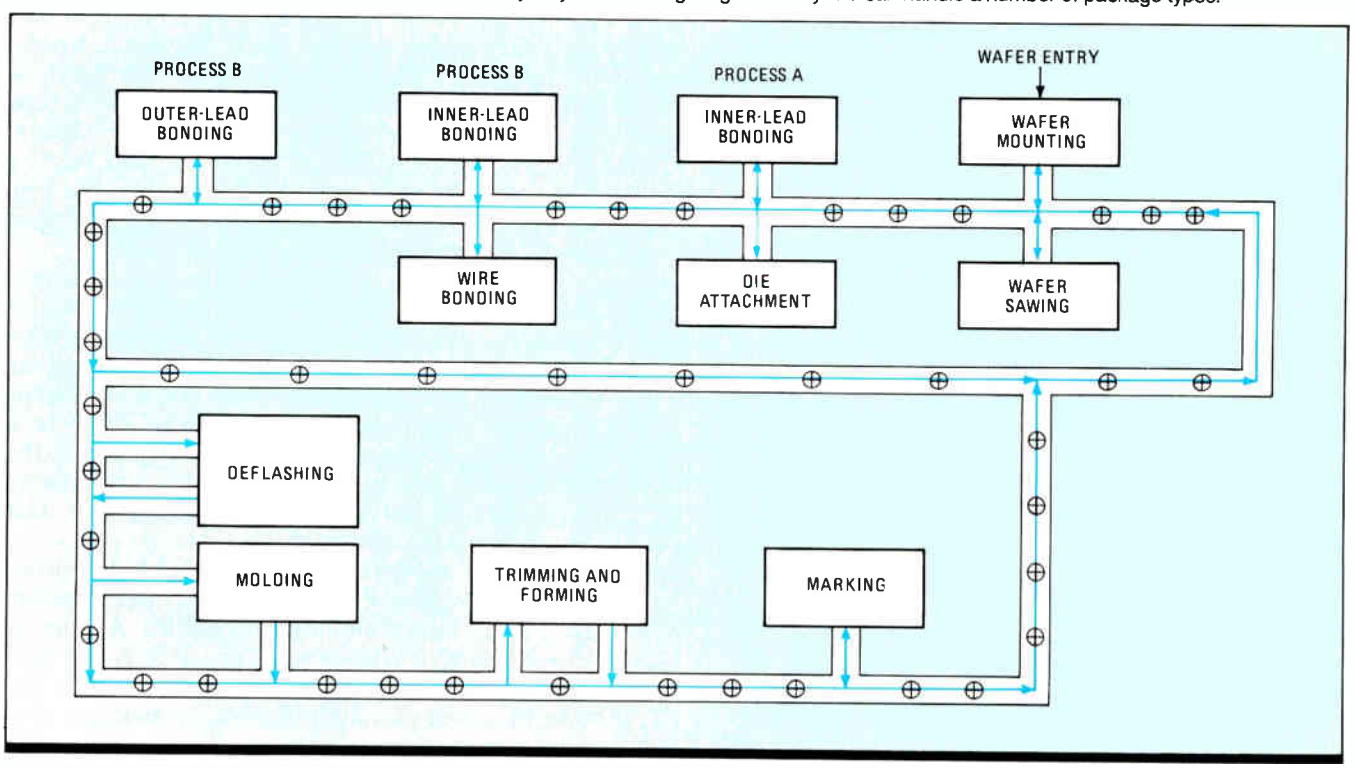
## RELYING MORE ON TAB

The pilot Odyssey line will share two processes, wire bonding and TAB, with the chips on lead frames ending up in molded DIPs. At the end of 1986, National promises to demonstrate assembly from wafer mounting and sawing to trim-and-form. By July 1987, the company plans to have up and running a complete assembly line encompassing all the steps and equipment, from wafer mounting and sawing to test. The line will have a maximum output equivalent to 3.5 million molded DIPs per month, working around the clock.

As it moves toward wafer-to-test automated packaging, National will continue to rely heavily on TAB. The company, which spends upward of $10 million yearly on packaging, has shipped more than 10 billion chips assembled with TAB since its first experiments with the method in the 1970s, and has been constantly developing the technique.

Today, the TAB effort has spilled over into newer package styles. TAB assembly based on two-layer polyimide tape is now being integrated into high lead-count molded-plastic leaded chip carriers. An all-copper single-layer bumped tape is being used for high-volume production of commodity items, and an entirely new miniaturized, high-density molded package based on the

**2. FLEXIBLE ASSEMBLY.** National Semiconductor's Odyssey self-reconfiguring assembly line can handle a number of package types.



bumped copper tape is at the prototype stage.

One of National's newest TAB developments is its Flow 60 process, based on a bumped single-layer copper tape. The company can apply bump-free dice directly to this tape, which cuts costs in two ways: it is not necessary to build up bumps on the chip, and the single-layer tape is less expensive than the double. To form this special tape, both the conductor pattern and the bumps of the inner leads are subtractively etched from a flexible copper tape. Development of this bumpless single-layer tape led directly to the creation of Tape Pak, actually a molded TAB. Basically, Tape Pak is a small square plastic package with leads on 20-mil centers that uses a copper TAB tape as its lead frame.

The executives in National's package-engineering group saw the need for a package for very large-scale integrated circuits that would be smaller than present plastic chip carriers and pin-grid arrays. The new package also needed to be testable and suited to automated assembly. It had to offer improved performance, high reliability, compatibility with a wide range of substrates, low thermal resistance, and low cost per lead.

*Tape Pak packages contain as many as 300 leads, yet still measure less than an inch on a side; they are one third the size of other surface-mountable packages*

Among the potential competitors for this packaging segment were the plastic chip carrier, the small-outline IC package, chip on board, the plastic quad flatpack, and the pin-grid array with a plastic substrate—but all had drawbacks. The chip carrier and SOIC are simply too big at large lead counts. Chip on board is space effective but difficult to test and automate. The plastic quad flatpack has handling and test problems. The plastic pin-grid array is large and cannot be surface mounted.

Only the Tape Pak meets all requirements for a small, testable unit capable of automated handling, National maintains. To emphasize its commitment to Tape Pak, the company has submitted its specifications to the Joint Electron Device Engineering Council as a proposed standard.

In Tape Pak assembly, a chip is first bonded to the special bumped copper tape. This tape has the package leads on 20-mil centers, and these leads fan out to test points on 50-mil centers. Next, the package and an outer test ring are molded onto each frame of the copper tape. This ring is discarded along with the tape once the package has been removed by the automatic pick-and-place machine at the point of assembly.

The test ring provides expanded contact test points and allows burn-in of single devices. In addition, it keeps test probes away from the actual package leads while physically protecting the assembly leads.

The result is a high-lead-count, surface-mountable package one tenth the size of a comparable DIP and one third the size of surface-mount packages (see table). With Tape Pak, packages can contain from 28 to 300 leads, yet still measure less than 1 in. on a side. Tape Pak also has much better electrical characteristics than competitive packages. For example, parasitic capacitance and inductance typically can be reduced by a factor of 10 from other packages.

National assumes that its new package will be mixed with small-outline and plastic-leaded chip carriers in surface-mount board assembly. This means that the Tape Pak must work with all forms of reflow soldering. The plastic package requires a 13-by-35-mil pad and 6-mil traces spaced 8 mils apart. The Tape Pak's compliant gull-wing leads allow it to be surface mounted to alumina or epoxy-glass boards.

## A PENNY A LEAD

Pick-and-place equipment already exists to handle the new package in a modified Model 4621 Omniplace system from Universal Instruments Corp., Binghamton, N. Y. This machine will accept plastic chip carriers and SOICs on tape and reel and uses a special "coin stack" magazine for the Tape Pak. A special handler takes a Tape Pak from its coin stack, removes the protective ring, cuts and shapes the leads, and then feeds it to the Omniplace placement head.

At this time, a square package 300 mils on a side with 20 to 40 leads is in production, and a 700-mil square unit with 80 to 124 leads is moving from the prototype stage to pilot production. A second 700-mil package with 124 to 172 leads is in the prototype stage. National projects a production quantity price of 1¢ a lead for the Tape Pak, which is competitive with conventional DIP packages. In time, the company says, this figure could be cut in half.

National reports that several large manufacturers are already evaluating the new package for future high-volume applications. As far as the company is concerned, Tape Pak is the optimum implementation of TAB and indicates the way to the dense, high-lead-count packages that future generations of chips will require. □

*PACKAGE CHARACTERISTICS*

| | Dual in-line package | | Plastic chip carrier* | | Tape Pak | |
|---|---|---|---|---|---|---|
| Body size (in.) | 2 by 0.55 in. | | 0.650 in.² | | 0.286 in.² | |
| | Long | Short | Long | Short | Long | Short |
| Lead length (in.) | 1.0 | 0.3 | 0.35 | 0.25 | 0.1 | 0.1 |
| Resistance (mΩ) | 7 | 4 | 4 | 3 | 2.4 | 2.4 |
| Inductance (nH) | 22 | 6.0 | 6.5 | 5 | 1.2 | 1.2 |
| Capacitance (pF) (lead to lead) | 0.5 | 0.2 | 0.3 | 0.2 | 0.2 | 0.1 |

*44 pins; the other two have 40 pins

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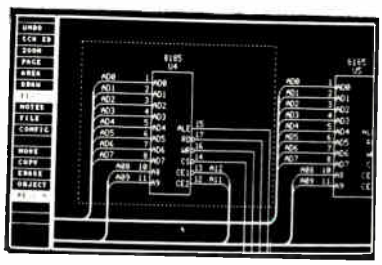

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PROBING THE NEWS

# TRADE PACT HITS FAST AS PRICES SOAR ON SOME JAPANESE ICs

## BUT MANY CALL THE MARKET-REGULATING AGREEMENT UNWORKABLE

*by Clifford Barney and Michael Berger*

**TOKYO**

Japanese exporters have given the first sign that the U.S.-Japan agreement on semiconductor trade may have real muscle behind it. Only days after the July 31 signing, the exporters began notifying distributors and customers of sharp price hikes for erasable programmable read-only memories and dynamic random-access memories.

Based on "foreign market values" set by the U.S. Commerce Department that differed from company to company, the increases were as much as 250% (see "How the prices of Japanese imports are calculated," p. 80).

But all else is confusion. U.S. manufacturers don't agree on how fast and far chip prices will climb. And some observers are flatly calling the agreement unworkable.

Intel Corp., the leading U.S. EPROM producer, says that after a couple of weeks of chaos, it expects prices to go up 20%, and will raise its own accordingly. National Semiconductor Corp. says it has no plans for an immediate price hike. Advanced Micro Devices Inc., second to Intel in EPROM sales, hedged and said it would follow the market, though it assured its long-term customers that they would not be hit with a rise.

On the DRAM front, Commerce's foreign market values were just as varied as those for EPROMs. Industry sources put Tokyo's NEC Corp. as apparently the most efficient producer, at $2.50 to $3 for 256-K parts. Mitsubishi and Toshiba came in at $4, Texas Instruments Japan and Hitachi at $5, and Oki at $5.50. Fujitsu Ltd. was on top at around $7, having reportedly been penalized for supplying insufficient data.

Yet the price fluctuations were only the immediate result of the agreement, and most companies expect them to dampen soon. The real significance lies not so much in the numbers, but in the fact that the Commerce Department had set prices for Japanese companies, and Japan's Ministry of International Trade and Industry had agreed to help police them.

So tight is the agreement that it may even restrict Japanese chip makers' ability to quote prices for delivery at a later date. "Regardless of the shipping date, the contract must be made at the foreign-market-value price," says economist Melissa Skinner of Commerce's Office of Import Administration.

U.S. Trade Representative Clayton Yeutter, who helped negotiate the pact, calls it "one of the most important bilateral agreements that has ever been negotiated by the United States." Commerce Secretary Malcolm Baldrige says the agreement has "far-reaching consequences for U.S. jobs and technology." And although there was widespread skepticism as to whether it could be enforced, or what long-range impact it will have, Yeutter's words are being echoed in some unexpected quarters.

**YEUTTER:** "One of the most important bilateral agreements negotiated by the U.S."

"This is a monumental agreement," says Jerry Crowley, the president of Oki Semiconductor, the U.S. affiliate of Tokyo giant Oki Electric Industry Co. Crowley is no fan of price floors for Japanese chips. "The U.S. has forced the Japanese to acknowledge that they have been dumping [selling below cost], and to accept being policed for the next five years."

Key to the agreement, Crowley says, is that MITI had agreed to monitor costs and to allow or disallow exports to the U.S. on a company-by-company basis. Only DRAMs and EPROMs are subject to immediate price control, because they were covered in the dumping cases. But MITI will monitor a variety of other circuits, among them emitter-coupled logic and memory, static RAMs, telecommunications chips, 8- and 16-bit microprocessors, 8-bit microcontrollers, and application-specific integrated circuits. Under the agreement, MITI will provide cost data on these chips within 14 days after being asked by Commerce in order to expedite a dumping investigation.

**MORE COMING?** "That sets a precedent," Crowley says. "If it can be done for semiconductors, what about printers, personal computers, or modems? What about textiles or pharmaceuticals? This is a breakthrough for the U.S. government, which has never been able to get that kind of agreement from Japan."

U.S. companies and the Semiconductor Industry Association lined up behind the government negotiators in hailing the agreement as a landmark. But in Tokyo, some Japanese and U.S. executives, after a look at the early numbers, say the agreement won't work.

"There hasn't been a market-regulating agreement in history that hasn't been circumvented, and this one is no exception," says one U.S. executive. And analyst David Keller of James Capel & Co.'s Tokyo office goes even further: "The Americans have shot themselves in the foot. This agreement will benefit more Japanese firms, and hurt more American firms, than anyone yet realizes."

They and other industry sources in Japan see three major results of the price-monitoring system:

■ What could be an enormous gray market will grow. "Akihabara [a Tokyo district where electronic goods of all de-

scriptions are traded] is going to become a mecca for U.S. chip buyers," says an import-export manager. "What everyone forgets is that there are more American chip buyers than there are makers. And they're going to look for bargains wherever they can find them. They're not going to pay a 'fair market value' $5 for a Hitachi chip when they can pick it up in Akihabara for $2.25."

■ Use of the board-stuffing ploy will explode, say sources. Because systems aren't covered by the pact, they predict both Japanese and U.S. producers in Asia will import chips embedded in phantom systems.

■ Third-country exports to the U.S. will increase dramatically. The agreement sets prices for chips made by Japanese subsidiaries in third countries, but at least one major Japanese chip maker already is studying a way to get around that. The tactic is simple: make the subsidiary an independent company.

There were two parts to the trade agreement. But if the antidumping portion had some immediate effects, there was much skepticism concerning the other—giving the U.S. access to Japanese markets. At present, according to Yeutter, U.S. firms account for only 8.5% of semiconductor sales in Japan, about $600 million last year. Within five years, he said, sales could jump to $1.5 billion to $2 billion.

Information on the agreement released by the White House said only that it requires MITI to establish an organization to promote U.S. sales in Japan. Several industry sources said, however, that a side agreement, which would not be made public, set a specific target of 20% of the market for U.S. companies.

**BALDRIGE:** The agreement has "far-reaching consequences for jobs and technology."

"I don't see how you can enforce the access commitments," says Michael Borrus of the Berkeley (Calif.) Roundtable on the International Economy, an organization that has studied the Japanese market extensively. "There is no incentive for Japan to enforce them. On the contrary, control of the domestic market is an important part of Japan's marketing strategy. They have economies of scale, so they can test new products and perfect manufacturing strategies without worrying about a foreign presence. If you double the U.S. market share, you begin to make important inroads into their ability to control the market."

Nevertheless, a number of U.S. chip makers are taking significant steps to position themselves in Japan [*Electronics*, April 14, 1986, p. 44] to tap a market Dataquest Inc. predicts will grow to more than $25 billion within five years. Texas Instruments Inc. and Motorola Inc. have significant operations in Japan, and Fairchild Semiconductor Corp. will start fabricating there in 1987. But other chip makers, now plagued with overcapacity, show no immediate signs of rushing to build in Japan. (LSI Logic Corp., however, has a joint venture to build a plant with Kawasaki Steel Co.)

**SYSTEMS FEARS.** While U.S. and Japanese semiconductor executives debate the merits of the agreement, two side issues emerge immediately. Some U.S. systems houses voice fears that the immediate rise in chip prices would make them less competitive. And all sides began wondering how Korean semiconductor houses would react to what could be a competitive bonanza.

SIA spokesman George Scalise replies that a healthy U.S. semiconductor industry would benefit systems houses in the long run. He points out that Korean firms could also be subject to dumping actions. In fact, one industry source says, a dumping charge against Korea will be instituted within 60 days.

"We will hammer on Uncle Sam to take action on other dumpers," says Ralph Thompson, vice president of the American Electronics Association. "That might be hard to do. But the agreement with the Japanese is a good 'Don't tread on me' reminder that people cannot continue dumping." □

## HOW THE PRICES OF JAPANESE IMPORTS ARE CALCULATED

**The U.S.** Commerce Department calculates minimum prices for Japanese imports of dynamic random-access memories and electrically programmable read-only memories from cost data provided by the Japanese themselves during last year's dumping investigation. These prices are called foreign market values (FMVs).

From the cost data, Commerce's Office of Import Administration builds a "constructed value" by adding overhead, 10% of material and labor costs, and a profit of 8% of all expenses, unless the company submits actual figures. This formula is unfair to producers who don't operate at full capacity, says Mark Giudici, pricing analyst at Dataquest Inc., the San Jose, Calif., research firm.

"It never gets better because each quarter the FMVs are recalculated using higher costs because of unused capacity," Giudici says. A fairer method, he suggests, would be to use the least-cost manufacturer as a floor, or to calculate an average.

Cost information comes from questionnaires sent by the Commerce Department. EPROM data originally reflected costs from April through September; DRAM data, July through September. Under the agreement, the data was updated to include the first six months of 1986.

EPROM data comes from seven companies: Fujitsu, Hitachi, Mitsubishi, NEC, Oki, Texas Instruments of Japan, and Toshiba. These plus one other, Matsushita, also provided data for DRAMs.

Because their cost data differs, each company now finds itself selling at a different set price in the U.S. Japanese firms must use these values when quoting on sales in the U.S., even on contracts for later delivery.

The new FMVs are effective immediately, except that DRAM orders made prior to Aug. 1 for later delivery may be shipped at the old prices until Sept. 15. For EPROMs, the subject of renewed dumping allegations during July, the agreement is retroactive to June 30. Sales made prior to that date will be reviewed case by case and Commerce will allow only those that are essentially firm in terms of price and delivery dates.

New FMVs will be released no later than Oct. 11 for use from Oct. 16 through Dec. 31, and new values will be set every quarter thereafter for the five-year term of the agreement. The Commerce Department may go to Japan and look through the actual records to verify data.

Meanwhile, the Japanese Ministry of International Trade and Industry will monitor costs in other categories of chips: emitter-coupled logic and memory, static RAMs, 8- and 16-bit microprocessors, 8-bit microcontrollers, and application-specific integrated circuits. If dumping is suspected in any of these categories, MITI has promised to turn the data over to the U.S. within 14 days. *–C.B.*

# THE NEXT BIG AUTO MARKET: THE MULTIPLEXED DATA BUS

## A $50,000 CADILLAC ROADSTER WILL KICK IT OFF THIS FALL

*by Tobias Naegele*

**DETROIT**

This is the year of the bus for the U. S. automobile industry—not a diesel bus or minibus, but a multiplexed data bus that can replace the tangle of wires behind the dashboard with a single wire. Its debut this fall in an American production car indicates that a revolution in automotive electronics could be just around the corner.

Cadillac's 1987 Allanté, a hybrid $50,000 Euro-American roadster, will be the world's first production automobile to implement an interactive multiplexed bus system to control multiple functions along a single copper wire, says General Motors Corp. And GM and Cadillac are not alone. Virtually every major automobile maker in the U. S., Europe, and Japan is at least researching multiplexed buses, and several plan to use such systems in production models before the end of the decade. Moreover, the Society for Automotive Engineers may recommend a list of standards for automotive multiplexing as early as February 1987.

Driving all this activity is the technology's potential: such systems eventually could replace the bulky wiring harnesses that now crowd the cramped space between a car's firewall and dashboard with a cheaper and more reliable single-wire or fiber-optic solution. At the same time, multiplexing can also provide more information to the driver and the mechanic and perform diagnostic operations to determine what problems exist and how to fix them.

The idea is exciting more than just auto makers. The semiconductor houses view the multiplexed bus as their next big auto market. Such bus systems need semiconductor switches to interpret the multiplexed signals, directing input commands to drive an automobile's electrical loads, such as lights, power windows and locks, motor controls, displays, and stereo equipment. Motorola Inc., for one, is promoting a generic mulitplexed system (p. 67). So is Hitachi Ltd., but the Japanese company says its entry is 3 to 5 years away.

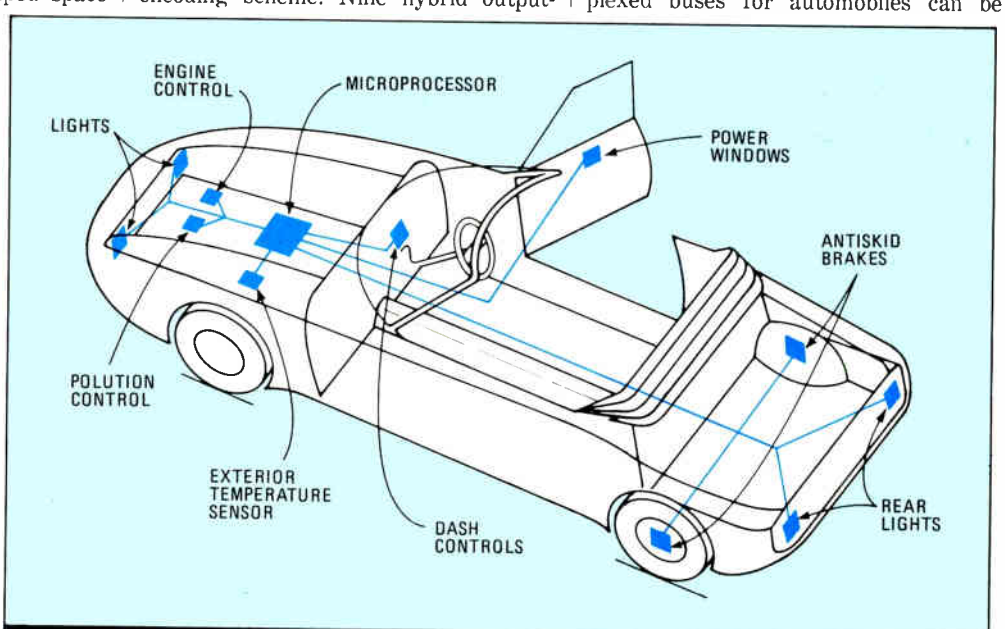
The attraction of this approach for components manufacturers is easily explained by the numbers behind it: the average car carries about 40 electrical loads, and top-of-the-line luxury models can carry 80 or more. At one integrated circuit per load, the market begins to look like a chip maker's paradise—and that's not counting the scores of other components that could be incorporated into cars' subsystems as the automotive environment becomes more electronic.

GM is filling the Allanté with electronic components from the U. S., West Germany, and Japan that run virtually every gadget imaginable (the car's only option is a cellular mobile phone that has its own retractable antenna). But it is the elaborate light system's bus—designed by GM's Delco Electronics Corp. and itself featuring about a dozen custom ICs—that really is the Allanté's star electronic attraction.

The bus carries information back and forth between a custom-designed central processor and virtually every filament in the car, using a pulse-width-modulation encoding scheme. Nine hybrid output-switch modules, each with four outputs, control more than 40 lights. A tenth hybrid circuit—called the input-switch module—acts as the user interface, providing eight different input signals, such as headlights on and off, turn signals, and hazard lights. The system warns the driver when bulbs burn out, turns on alternative lights when the appropriate bulbs do not respond, and enables headlights to turn on and off automatically when it gets dark or light. Only the transmission shift-position indicator and the glove-box light do not fall within the bus system's network.

**SECOND BUS.** Like the 1986 Cadillac Eldorado and other 1986 GM-30 models that share the same basic platform, the Allanté also has a secondary bus for sharing data between the engine-control computer—which regulates fuel delivery, idle speed, and the like—and the body-computer module, which controls displays, operates the climate-control system, and handles most of the internal features, such as driver controls. Unlike the bus that runs the lights, the second bus is not multiplexed.

Frederick Miesterfeld, chairman of the SAE subcommittee for multiplexing and data communications, says multiplexed buses for automobiles can be




**LINES OF COMMAND.** This multiplexed bus concept uses one central computer to control access to the bus.

broken down into three categories. Class A buses include basic controls, he says, such as headlights, power locks, and windows; Class B covers instrument clusters, engine controllers, trip computers, and other areas where data communications comes into play. Class C buses, which are the furthest from implementation, include real-time control of antilock brakes, active suspension systems, and other engine controls. Miesterfeld says most of his subcommittee's work is on Class A and B buses, and that any implementation of a Class C bus "will be beyond the 1993 model year."

Class A and B buses will come first primarily because they do not require the extra-high data rates that the other class demands. Cadillac's systems, for example, can run at 10 kb/s, but in practice are running at only 5 kb/s. Faster data rates are possible, but they present a problem with radio-frequency and electromagnetic interference.

Miesterfeld, an engineering supervisor at Chrysler Corp.'s Advanced Electronic Development Lab in Highland Park, Mich., says his subcommittee will likely choose 10 kb/s as the standard rate when it recommends a standard to the SAE. Other key issues facing the standards committee are whether or not fault-tolerance should be required, whether the input/output structure should be regulated by voltage or current, and what sort of encoding method should be used. Miesterfeld says a final document could be issued by the time of the SAE annual meeting in February.

Meanwhile, European car makers are also busy with buses. Many observers believe the first manufacturer to market a car in which the entire electrical system is based on a bus will be French. That nation's two giants—Régi Renault and Peugeot SA, which also owns Citroën—have joined forces to define a common system on which they are putting the finishing touches.

In West Germany, Robert Bosch GmbH, the automotive components giant, is working on a high-speed data bus for communications between such loads as the sensors in antiskid brake systems and engine and transmission controllers, where a sacrifice in speed translates into an impractical—and often impossible—sacrifice in vehicle safety. In a fast-acting antiskid braking system, for example, 200 $\mu$s is all the time available for data transmission under worst-case conditions. Bosch is working on a master-slave concept whereby access to the bus is controlled not centrally, as in the Cadillac bus, but locally by the individual control units.

*Intel is designing ICs for a high-speed bus to come from Bosch*

Bosch is cooperating on chip designs with Intel Corp., Santa Clara, Calif., to make sure it has the kind of chips that can cope with the high-speed transmissions that next-generation systems will require. The U.S. company is developing ICs that meet the interface specifications Bosch has supplied, but the Stuttgart company cannot say when carmakers will begin to integrate such systems into their designs.

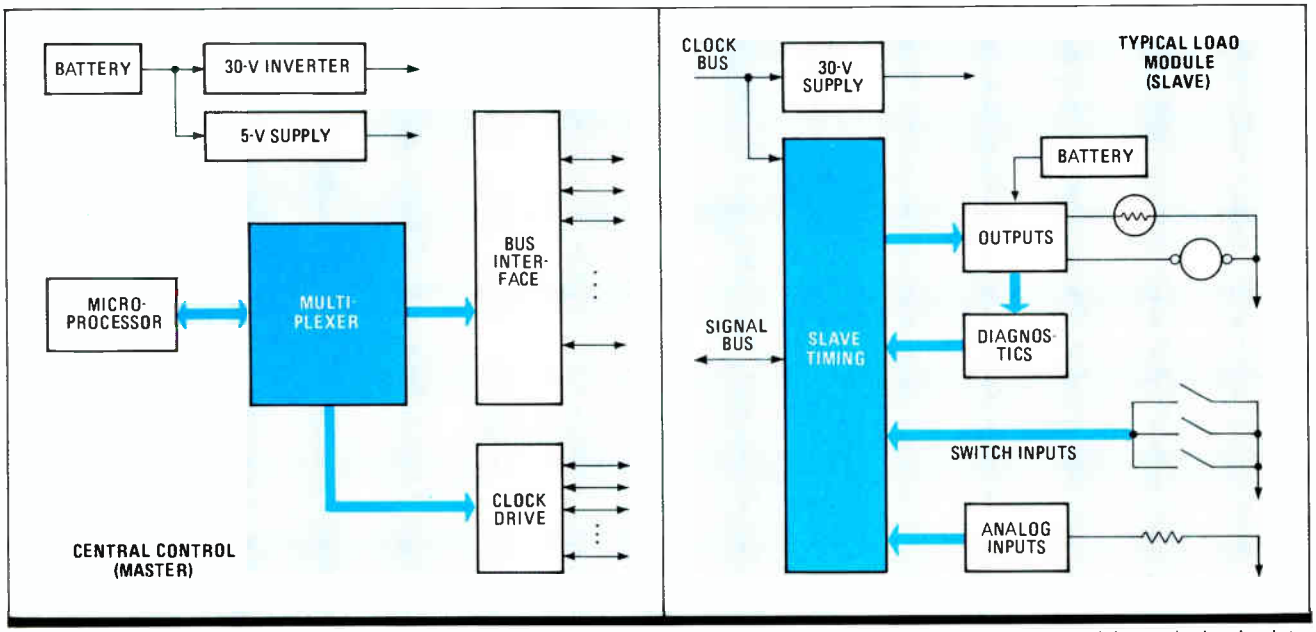
In Japan, there appears to be no hurry to multiplex, although fiber-optic systems are in limited use. As early as 1982, Toyota introduced its Century, a high-end luxury car with door-mounted microcomputers linked by optical fiber to a central computer. The system handles nine functions, including power windows. And some Nissan models feature sound controls mounted in the center of the steering wheel.

Multiplexed systems may be invisible to the owner, but they could influence design. Nigel Gardner, automotive product marketing engineer with National Semiconductor Corp. in Swindon, England, says multiplexing could change the way manufacturers look at an auto when they are designing it. "Automotive designers are forced to design cars around the electrical harness," he says. "With the multiplexed bus they'll be able to complete their design and add the electronic system afterward."

Still, both Renault and Peugeot warn that multiplexing will not be an overnight sensation. "When you talk about multiplexing a car you're talking about a true revolution," says Michel Durin, technical director of Peugeot. "The problem is that multiplexing is not something you can sell to the customer, so it has to present a tangible advantage to the manufacturer."

The reasoning here is that a car's electrical system, whether multiplexed or not, is transparent to the car's owner. And to the owner, the only palpable advantage of multiplexing might be functions like a global diagnostic scheme, which becomes fairly easy to do when the car's electronic systems are networked. But manufacturers also know that customers aren't willing to pay a heavy premium for such a system. Price, in the end, will dictate when multiplexed buses become a universal feature. □

*Reporting also by Robert T. Gallagher, John Gosch, and Charles L. Cohen.*




**CONTROL FAMILY.** In this example, the central control computer would be mounted under the hood and the slave modules at the load points.

# NEW PRODUCTS

## CASCADABLE GaAs MICROWAVE IC OFFERED AS UNPACKAGED DIE

### HARRIS 6- TO 18-GHz CHIP IS FIRST IN A FAMILY

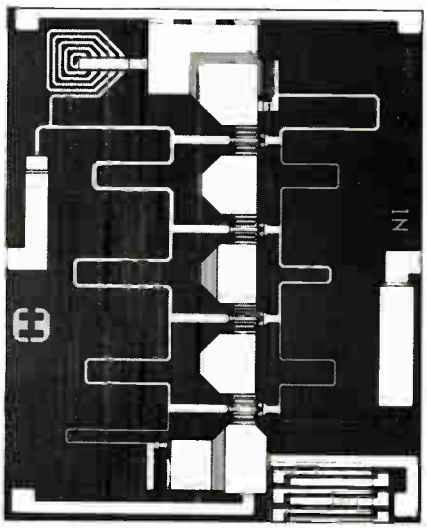
The first chip in a family of fully integrated standard 0.5-μm gallium arsenide monolithic microwave integrated circuits (MMICs), is now available in die form from Harris Corp.'s Microwave Semiconductor operation.

Designated the HMM-11810-0, the 6- to 18-GHz MMIC is being offered as an alternative to fully packaged devices, which are limited in the way they can be implemented on a pc board. According to Harris, the HMM-11810-0 is the first fully cascadable GaAs MMIC in the industry to be offered in die form.

"What this means is that systems designers are no longer limited by packaging requirements," says Bruce Hoffman, marketing manager. The part "allows designers to place gain anywhere in the system in small gain blocks."

Compared to the packaged alternative, says Hoffman, MMICs in die form offer such additional advantages as reduced die-attachment and wire-bond counts and increased reliability. Also, the decreased size and weight of the die make MMICs far more useful to system designers as more manufacturers develop in-house hybrid chip-fabrication capabilities.

The HMM-11810-0 has a small signal gain of 5 dB and a gain flatness of ±0.75 dB across its 6- to 18-GHz range. Maximum input and output voltage standing-wave ratio is 2:1, while the typical noise figure at 50 mA is 6 dB at 18 MHz. It includes on-chip dc blocking and bypass functions, allowing users to cascade it without turning to the blocking capacitors or additional components that are required by traditional packaged MMICs to achieve their specified performance.



**GAIN.** With the Harris MMIC, designers can put gain anywhere in their systems.

The HMM-11810-0 measures 5,600 mils² and is fabricated with 0.5-μm gate lengths, using the company's through-the-substrate via-hole process. This method is designed to reduce unwanted inductance in the overall circuit, to simplify bonding requirements associated with incorporating the device into a system design, and to ensure greater device uniformity.

**TAILORABLE.** The chip also features silicon nitride dielectric scratch and short-circuit protection, large gold bonding pads, and titanium/platinum/gold metallization. It incorporates a variable bias capability that allows it to be optimized for the specific power, gain, or noise level required by the application, Hoffman says.

The HMM-11810-0 is designed for gain-stage applications, where broadband high-frequency performance with excellent gain, high-power, and low-noise characteristics are critical, he says. Applications for the device include wideband receivers used in electronic warfare devices and transmitters used for radar warning and jamming.

Available six weeks after ordering, the HMM-11810-0 is priced at $200 each in 100-piece lots. *–Bernard C. Cole*

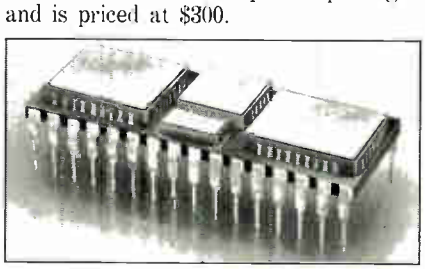
Harris Corp., Microwave Semiconductor, 1530 McCarthy Blvd., Milpitas, Calif., 95035. Phone (408) 747-1000 [Circle reader service number 360]

## HIGH-SPEED SRAM MODULES SAVE SPACE

Electronic Designs Inc., a manufacturer of high-speed, high-capacity memory modules, is bringing out two new parts: a 1-Mb (128-K-by-8-bit) static RAM module that offers a 4:1 saving in pc-board space; and a monolithic 8-K-by-8-bit SRAM. Both have the high speeds needed for military applications.

The Hopkinton, Mass., company's 128-K-by-8-bit module contains four RAMs surface-mounted on both sides of the ceramic substrate of a 32-pin DIP, allowing for development of smaller devices or additional functionality on the same device, says an EDI spokesman.

The module comes in two versions. The 88128C uses RAMs packaged in leadless chip carriers and sells for $610 in quantities of 100. The 88128PC has RAMs in small-outline plastic packages and is priced at $300.



**SPACE SAVER.** EDI's 128-K-byte SRAM module provides 4-to-1 space saving.

Both versions can be used for commercial or military-screened applications, and have access times of 120, 150, and 200 ns. They are fully static and have a decoupling capacitor mounted on the substrate for bus control. The products offer Jedec compatibility and are compatible as well with 8-K-by-8-bit monolithic parts. They will be available in October.

**CHIP OPTIONS.** EDI's monolithic 8-K-by-8-bit SRAMs are available in two packaging options for six-transistor- and four-transistor-cell devices. Both are Jedec compatible, with the four-transistor 8808AC J/K MHR version offering 70-ns

access times, one of the fastest speeds around for military applications.

The four-transistor version, which is fabricated in a mixed-MOS technology, also has rates of 100 and 120 ns. In a 32-pin ceramic leadless chip carrier, the part costs $74 in quantities of 100, or $45 for a 28-pin side-brazed DIP.

The six-transistor versions—the 8808-ACL-20 JMHR and KMHR—feature a stable low-voltage data-retention rate of 10 mA with internal cell stability. Built in CMOS technology, they boast speeds of 150 and 200 ns.

The 8808ACL-20 JMHR comes in a 32-pin leadless chip carrier and is priced at $105 apiece in quantities of 100. The 8808ACL-20 KMHR, in a 28-pin side-brazed DIP, sells for $72. All versions of the monolithic SRAMs are available now. *–Debra Michals*

Electronic Designs Inc., 35 South St., Hopkinton, Mass. 01748.
Phone (617) 435-9077 [Circle 361]

## AMD SHIPS FAST 16-K STATIC RAMS

Advanced Micro Devices Inc. has moved into volume production with a pair of CMOS static RAMs featuring access times in the 20- to 25-ns range, making them among the fastest now available.

Designated the Am99C58 and Am99C59, the SRAMs are high-performance CMOS circuits organized as 4-K by 4 bits and featuring separate data inputs and outputs. Both operate from a single 5-V supply, and all inputs and outputs are fully TTL-compatible.

Available in either a 24-pin, 300-mil DIP or a 28-pin ceramic leadless chip carrier, the 28,000-mil$^2$ parts have a maximum active power dissipation of only 770 mW. Standby power (Am99C58 only) ranges from 200 mW at TTL input levels to 50 mW for CMOS input levels.

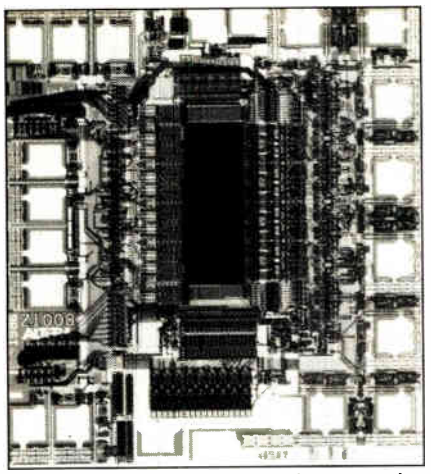
Available now over a speed selection from 20 to 45 ns, the devices are priced at $24.75 each (20 ns) and $19.95 each (25 ns) in lots of 1,000.

Advanced Micro Devices Inc., 901 Thompson Place, P. O. Box 3453, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 362]

## ERASABLE PLD DRAWS ONLY 10 mA

The EP320, billed as Altera's third-generation of erasable programmable logic devices, has a standby current of just 10 mA. Built with advanced CMOS EPROM technology, the part can be used as a generic building block to replace any of 46 different programmable-array-logic devices.

When operating at 1 MHz, the EP320 draws a maximum of 10 mA, and at



higher clock rates, current increases by 0.5 mA/MHz. Like its predecessors, the chip has a fully programmable output architecture, so it can be used as a user-configurable building block in place of such logic devices as those from Monolithic Memories Inc., including the industry-standard 16L8 and 16R8.

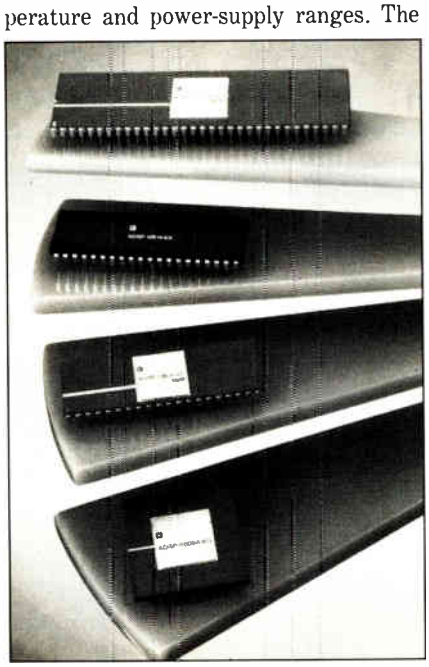
The EP320 is available now with a 35-ns I/O delay speed; 25-ns versions are to follow later in the year. Prices start at $4.50 each in lots of 100.

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051.
Phone (408) 984-2800 [Circle 365]

## 12-BIT MULTIPLIER RUNS AT 20 MHz

Two 8-bit and two 12-bit multipliers and multiplier/accumulators from Analog Devices are faster than the bipolar parts they replace because they are fabricated in a 1.5-μm CMOS process.

The ADSP-1080A and ADSP-1081A 8-by-8-bit multipliers guarantee multiplication rates of 30 MHz over the full temperature and power-supply ranges. The



ADSP-1080A operates on 2's complement data and is a pin-compatible replacement for TRW's MPY008HJ5. The ADSP-1081A runs on unsigned-magnitude data; this part replaces TRW's MPY08HUJ5.

The 12-bit parts are the ADSP-1012A and ADSP-1009A. The ADSP-1012A guarantees operation at 20 MHz (50 ns) at 300-mW power consumption. The ADSP-1009A has a 70-ns execution time and consumes 350 mW.

In lots of 100 pieces, the parts range in price from $27 to $55.30. Delivery is from stock.

Analog Devices Inc., 1 Technology Way, Norwood, Mass. 02062.
Phone (617) 461-3881 [Circle 369]

## 25-MHz VERSIONS OF 68020, 68881 BOW

The 25-MHz version of the 68020 32-bit microprocessor and the 20-MHz version of the 68881 floating-point coprocessor are now available in sample quantities. Together, the two easily surpass the 1 million Whetstone performance mark.

The 25-MHz 68020 operates in burst mode at 12.5 million instructions/s, with a sustained throughput of 5 mips. This is seven times the performance of the 68000, an improvement that comes from the new part's high-speed operation, on-chip instruction cache, three-stage instruction pipeline, powerful instruction set, and addressing modes.

The 68881, which adheres to the IEEE floating-point specification, offers more than 40 floating-point functions. It handles trigonometrics, hyperbolics, exponentials, logarithms, absolute values, and square roots, among others. All of these functions are implemented in hardware.

Samples of the 68020 are available now for $849; production will begin in the fourth quarter. The 68881 is available in sample quantities for $699.

Motorola Inc., Microprocessor Products Group, P. O. Box 3600, Austin, Texas 78764. Phone (512) 440-2839 [Circle 371]

## 16-K STATIC RAM ACCESSES IN 25 NS

Built in 1.3-μm CMOS, the 16-K HM6268P static RAM is available in versions with access times of either 25 or 35 ns. The SRAM is organized as 4-K by 4 bits and housed in a 20-pin package.

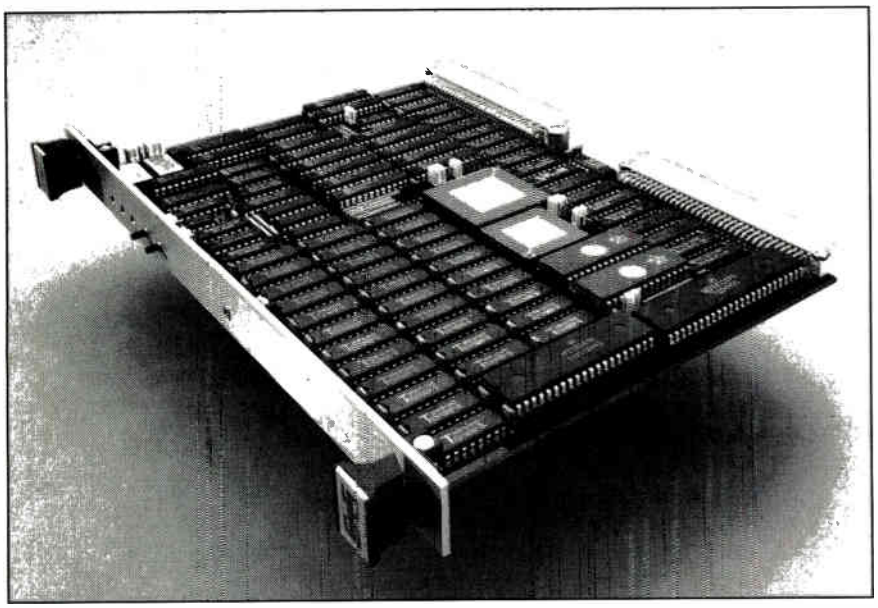
Power requirements are 250 mW in the operating mode and 20 mA in standby. It is suitable for use in cache memories, microcomputers and mainframes, and high-speed graphics systems.

Samples are available now. In lots of 100, the 25-ns part sells for $15.45.

Hitachi America Ltd., 2210 O'Toole Ave., San Jose, Calif. 95131.
Phone (408) 435-8300 [Circle 373]

# BOARDS CUT WAIT STATES IN REAL-TIME PROCESSING

## TWO 32-BIT CARDS HAVE 64 BYTES OF 'MAILBOX' RAM TO STORE INTERRUPT SIGNALS DURING CRITICAL TASKS



**CHOICE.** CPU-4 VMEbus boards offer three serial ports or one parallel and two serial ports.

Two 32-bit VMEbus computer boards from Electronic Modular Systems Inc. combine fast dynamic RAMs, a 68020 microprocessor, and a look-ahead addressing scheme to cut out wait states in industrial processing applications. The fastest version uses a 20-MHz 68020 with 60-ns 256-K DRAMs.

The CPU-4RT and -4SC VMEbus computers fit on standard 233-by-160-mm double-height Eurocards and hold Motorola 68020 chips running at 12.5, 16.7, or 20 MHz. DRAM storage ranges from 256-K bytes to 4 megabytes. They also contain a built-in mailbox, 64 bytes of dual-ported RAM that holds interrupt signals while the host is completing a critical task. The CPU-4RT features two serial ports and one parallel port, while the CPU-4SC has three serial ports.

**35 FLAVORS.** "With all the different variations of speed, memory density, and wait states or no wait states, the boards are available in about 35 different configurations," says Jerry Slaughter, director of sales. Besides uses in factory automation, he says, the CPU-4 modules are suited for image processing, avionics flight-test and -simulation equipment, and other real-time-processing applications.

To keep the 16.7- and 20-MHz 68020 microprocessors humming along with no memory-access wait states, Electronic Modular Systems uses 256-K DRAMs from Inmos Corp. that operate at speeds of 60 ns. The Inmos memories have a modified static-column decoding scheme that uses a 2-ns early setup time at the start of a row-address capture period to complete the task in 4 ns [*Electronics*, May 3, 1984, p. 56]. The early setup time is 15 ns using other static-column decoding schemes.

In addition to employing the speedup feature built into the Inmos chip, the CPU-4 boards have an automatic look-ahead register that anticipates the next address from the CPU. The firmware for the look-ahead access is contained in programmable-array-logic chips. To eliminate wait states, the look-ahead access feature must be combined with the 60-ns DRAMs and the 16.7- and 20-MHz 68020s or with 100-ns DRAMs and the 12.5-MHz 68020.

An optional 68881 floating-point coprocessor and a 16-bit timer for the 68881 are also available for both the CPU-4RT and -4SC. The boards have a pair of 28-pin sockets for up to 128-K bytes of ROM. Zero-wait-state operation is available in all 256-K-byte and 1-megabyte DRAM configurations.

In versions that pack 4 megabytes onto the small processor boards, the company uses 100-ns 1-Mb DRAM chips. All boards can be upgraded in the field with new processor and memory chips; to handle the resultant timing differences, the firmware in logic arrays can also be upgraded.

The boards have an operating temperature range of 0°C to 55°C with 0% to 95% relative humidity (noncondensing). In single quantities, the 12.5-MHz CPU-4 boards sell for $2,000 with 1 megabyte of storage.

The 16.7-MHz version with 1 megabyte of RAM sells for $3,485 each; the 20-MHz model with 1 megabyte is $3,930. —*J. Robert Lineback*

Electronic Modular Systems Inc., 4546 Beltway Dr., Dallas, Texas 75244.
Phone (214) 392-3473 [Circle 460]

## CONTROLLER HANDLES 25,000 STEPS/S

A programmable single-axis stepper motor controller interfaces with any dumb terminal or computer through an RS-232-C serial or 8-bit parallel interface. The DCI-4000-1, which comes with 16-K bytes of battery-backed RAM, supports programmable parabolic velocity profiles at up to 25,000 steps/s.

With up to 4,000 W of power at 1 to 5 A/phase, the controller drives any stepper motor with a 23-, 24-, 34-, or 42-frame size. It supports conditional and unconditional jumps, three levels of program nesting, and absoute or incremental position commands.

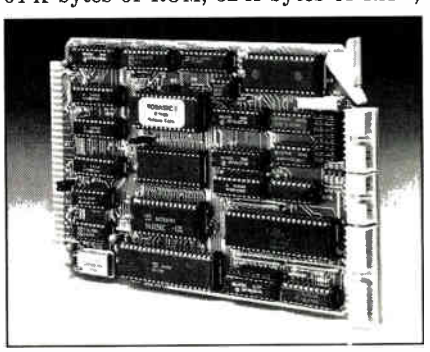
The controller costs $2,000. A joystick and a run-only keypad are optional.

Design Components Inc., 1 Kenwood Circle, Kenwood Industrial Park, Franklin, Mass. 02038.
Phone (617) 528-7300 [Circle 465]

## DATA COLLECTOR COMES WITH COMPILER

The 886 data-acquisition CPU card comes with an integrated operating system and Robasic, an advanced language developed for industrial programming. Built into the 886, the Robasic multitasking language uses familiar Basic commands.

The 886 card is built around the 16-bit 8088 microprocessor. It has 16 parallel I/O lines for linking with relays, lamps, and and timers, and its memory includes 64-K bytes of ROM, 32-K bytes of RAM,



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Toshiba technology leads the way again with the development of Ultra Large Scale memory devices that feature high speed access times.

## 1 MB CMOS DRAMS

TOSHIBA is delivering now ... all the 1Mb product you can use. In three different access modes. With speeds of 100 and 120 ns. You have a choice of fast page mode, static column or nibble mode. And you can get production quantities now.

| TOSHIBA 1 Mb DRAMs | | | | | |
|---|---|---|---|---|---|
| Part Number | Organization | Process | Speed | Mode | Package |
| TC511000 - 10 | 1 Mb x 1 | CMOS | 100 ns | Fast Page | 18 pin |
| TC511000 - 12 | 1 Mb x 1 | CMOS | 120 ns | Fast Page | 18 pin |
| TC511001 - 10 | 1 Mb x 1 | CMOS | 100 ns | Nibble | 18 pin |
| TC511001 - 12 | 1 Mb x 1 | CMOS | 120 ns | Nibble | 18 pin |
| TC511002 - 10 | 1 Mb x 1 | CMOS | 100 ns | Static Column | 18 pin |
| TC511002 - 12 | 1 Mb x 1 | CMOS | 120 ns | Static Column | 18 pin |
| TC514256 - 10 | 256K x 4 | CMOS | 100 ns | Fast Page | 20 pin |
| TC514256 - 12 | 256K x 4 | CMOS | 120 ns | Fast Page | 20 pin |
| TC514258 - 10 | 256K x 4 | CMOS | 100 ns | Static Column | 20 pin |
| TC514258 - 12 | 256K x 4 | CMOS | 120 ns | Static Column | 20 pin |

## 256K CMOS STATIC RAM

Toshiba's product development leadership continues. We were first with 16K CMOS RAMs. First with 64K CMOS RAMs. And now first again—with 256K CMOS static RAMs. This 32K x 8 device features the lowest power consumption available today—only 5mA/MHz. Lower than any competitive product. And we offer speeds to 100 ns.

| TOSHIBA 256K CRAMs | | | | | |
|---|---|---|---|---|---|
| Part Number | Organization | Process | Speed | Standby Power | Package |
| TC55257 - 10 | 32K x 8 | CMOS | 100 ns | 1mA MAX | 28 pin |
| TC55257 - 12 | 32K x 8 | CMOS | 120 ns | 1mA MAX | 28 pin |
| TC55257L - 10 | 32K x 8 | CMOS | 100 ns | 100μA MAX | 28 pin |
| TC55257L - 12 | 32K x 8 | CMOS | 120 ns | 100μA MAX | 28 pin |

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and jumper-selectable EPROM of up to 64-K bytes for user programs. Total addressable memory is 1 megabyte.

The card's 8-channel analog-to-digital conversion circuitry is built around a 10-bit CMOS ADC that uses the successive-approximation register technique. The 886 incorporates an eight-channel multiplexed analog input through a resistor network that allows for both bipolar (±5 V) and unipolar (0- to 5-V and 0- to 10-V) inputs.

The device supports nine prioritized interrupts. The eight-level interrupt priority controller causes execution to branch directly to Robasic line numbers. An additional ninth interrupt is nonmaskable. Interrupts can be handled directly from Robasic.

Priced at $695 each, the 886 is available from stock.

Octagon Systems Corp., 6510 W. 91st Ave., Westminster, Colo. 80030.
Phone (303) 426-8540 [Circle 466]

## MOTOR CONTROLLER RUNS THREE AXES

The Automove 201 stepper-motor controller handles three axes of motion for X-Y positioning tables and stepper-motor systems. The unit controls and drives each of the three axes sequentially or it can move the X and Y axes simultaneously, providing precise positioning through linear and circular interpolation.

The computer-programmed system supports incremental and absolute motion, angle-independent speed in X and Y axes, and an independent full- or half-stepped third-axis driver. Microstepping increases resolution and takes advantage of the accuracy and reliability of stepper motors. The controller achieves velocities up to 65,000 microsteps/s, with resolution programmable up to 6,400 microsteps/revolution.

The Automove Control Language, a two-letter mnemonic command language in firmware, simplifies host-computer software and reduces computation and communication time. Easymove, a menu-driven application-software package for IBM Corp. Personal Computers, further simplifies programming the Automove 201 controller.

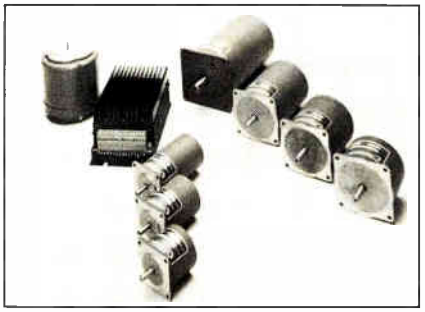
The Automove comes as a complete package with a power supply, motor drivers, an RS-232-C serial interface for linking with computers, an indexer, firmware, outputs, and optional inputs in a single package. The Automove 201, including two motors, is priced at $3,995 each.

Asymtek, 2142-C Industrial Ct., Vista, Calif. 92083.
Phone (619) 727-7422 [Circle 467]

## MOTOR DRIVER HAS BUILT-IN INDEXER

The CX motor driver includes a built-in indexer that will operate with almost any standard hybrid stepper motor. The driver, which measures 6 by 4 by 2½ in, supports 12,800 steps/revolution.

The driver's built-in indexer features an RS-232-C interface, 60 commands, a daisy-chain capacity for up to eight motors, user-selectable microstepping waveform for optimal smoothness with



all motors, and 2-K bytes of nonvolatile memory for storing up to seven multiple-move sequences.

Priced at $640, the CX will be available in 30 days.

Compumotor Corp., 1179 N. McDowell Blvd., Petaluma, Calif. 94952.
Phone (707) 778-1244 [Circle 470]

## LIMIT SWITCH CAN BE SET ON LINE

A programmable limit switch called AstroSet features a teach capability that permits users to program it right at the machine site. As the machine is walked through its process, precise limit settings for each operation are entered by simply pressing a button for storage into a program.

A jog button lets the user fine-tune limits as physical parameters change during the operation. Off-line programming is done through a keyboard or by down-loading programs from a host computer over an RS-322-C, RS-422A, or RS-423A interface.

The switch features digital filtering that makes the unit impervious to shop-generated electrical noise. A single AstroSet switch can control two axes, or two separate machines. Seven programs can be stored in memory, each holding up to 32 cam profiles or relay channels, with 1,000 set points per channel.

Pricing and availability information for the AstroSet was unavailable.

Astrosystems Inc., 6 Nevada Dr., Lake Success, N. Y. 11042.
Phone (516) 328-1600 [Circle 471]

## WORK-CELL ROBOT STARTS AT $15,300

A pair of four-axis work-cell robots and their controller, targeted for use as the base building block for an assembly cell, are now available at $15,300 to $26,000. Because they're not isolated robots but rather building blocks, the Ar-i 350 and 550 robots and their controller—the HAC-05—require no complex interfacing to the work cell.

The Ar-i 350 robot has a maximum payload of 8.8 lb and can move at 141.7 in./s. Repeatability is to within 0.002 in. The Ar-i 550 has an 11-lb payload with the same velocity and resolution.

The HAC-05 controller can execute 15 interrelated jobs concurrently, with the operating system automatically processing I/O instructions with maximum cycle times of 4 ms when it is configured at its maximum, 256 inputs and 256 outputs. The controller can be linked to an IBM Corp. Personal Computer for off-line programming and storage of programs. Software support is Harl-II, a Basic-like compiler.

The controller and work-cell robots are available now.

Hirata Corp. of America, 3901 Industrial Blvd., Indianapolis, Ind. 46254.
Phone (317) 299-8800 [Circle 468]

## MOTOR DRIVER CUTS LOW-RPM RESONANCE

The MD10, a high-performance bipolar stepping-motor drive, microsteps a 200-step hybrid motor at 2,000 steps/revolution, resulting in a tenfold improvement in resolution and the elimination of low-speed resonance and vibration, which is characteristic of stepper motors when used in the full- or half-step mode. The driver will operate a wide range of two-phase stepper motors, from a single-stack 23-frame size to a multistack 42-frame size, with current ratings from 2.5 to 7.2 A/phase.

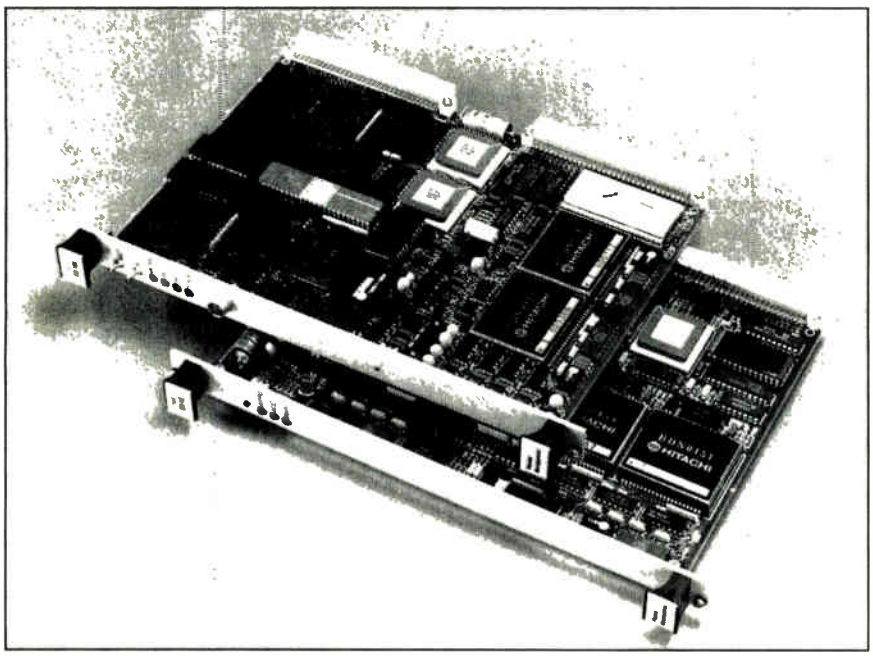
The user can control output current with an external resistor in a pulse-width modulator using power MOS FETs. The MD10 has a wide power-supply range, from 24 to 60 V, allowing the control to be tailored to the application with a minimum of wasted energy.

The MD10, which is packaged in a 4-by-4-by-1-in. case, is priced at $350.

Oregon Micro Systems Inc., 15075 N. W. Pioneer Rd., Beaverton, Ore. 97006.
Phone (503) 644-4999 [Circle 469]

# BUBBLE-MEMORY SYSTEM STORES 17 MEGABYTES

## PLESSEY'S BOARD SET IS A FAST AND RUGGED ALTERNATIVE TO HARD DISKS FOR VMEBUS SYSTEMS



**SPEEDY.** Plessey's VMEbus bubble memory transfers data at 3.6 megabytes/s.

Plessey Microsystems Inc.'s bubble-memory board set for VMEbus computers is laying claim to the highest-capacity board-based mass-storage subsystem yet. The PME BB-1 master card holds 1 megabyte; when eight 2-megabyte BB-1S slave cards are attached, total system capacity hits 17 megabytes.

The master and slave boards connect through row A on the J2 backplane and allow access through the Small Computer Systems Interface command set. Both board types feature typical access times of 11 ms and 16 ms maximum, compared with the 33-ms typical access times of hard-disk drives. The bubble-memory subsystem is also suitable for harsh environments, where contamination may render disk drives impractical.

The BB-1M master board uses an 8-MHz Z80H microprocessor to perform subsystem control functions. The system's CPU coordinates command-block and data transfers using 256 bytes of dual-port RAM, which consists of 2-K-by-8-bit static RAM chips.

The dual-port RAM acts as the interface between the VMEbus and the bubble memory. Data can be transferred across the VMEbus at up to 3.6 megabytes per second.

The Z80H sets up a 16-bit, single-channel direct-memory-access controller to handle data transfers between the dual-port RAM and the VMEbus. The DMA controller reads and acts upon subsystem status information and programs the gate arrays to access the bubble memory. Two custom gate arrays generate all the timing and control signals necessary to govern the operation of the bubble memories and the passing of data between bubble and dual-port RAM.

The controller, which has 24 address lines, gains control of the VMEbus with an on-board requester, then uses block-transfer mode to pass paged data in either 16- or 8-bit transfers, as specified in the command parameter block. An 8-bit upper-address latch gives the DMA controller the ability to handle 32-bit addresses.

**ERROR CORRECTION.** Error-correction facilities are provided under control of the CPU. Using the status information generated by the gate arrays, single-bit errors are corrected by inverting the error bit in the dual-port RAM.

The BB-1M master card is fitted with 1 megabyte of bubble memory using two of Hitachi's new 4-Mb bubble-memory devices, arranged as 4,096 logical pages of 256 bytes. Each slave board has 2 megabytes of memory, using four 4-Mb chips. The slave boards are arranged as 8,192 pages of 256 bytes.

VMEbus devices, such as a computer's CPU, can set up a task for the BB-1M by reading from and writing to the command parameter block in dual-port memory. The block is structured around the SCSI command-block format and comprises the SCSI command registers, data-address pointer, data-length bytes, control words, SCSI status register, interrupt completion, and error vectors.

An RS-232-C serial I/O port is included on the master card. If the board is switched to local mode using the front-panel switch, the CPU enters an EPROM-based control monitor program, and independent access to the bubble memory (master and slaves) is available over a front-panel connector. With this method, data transfers occur at 9,600 bits/s.

Available 30 days after ordering, the master cards cost $3,523. The slave cards are $4,205 each. *–Steve Zollo*

Plessey Microsystems Inc., 1 Blue Hill Plaza, Pearl River, N. Y. 10965.
Phone (914) 735-4661 [Circle 340]

# BOARDS ELIMINATE NEED FOR GRAPHICS TERMINALS

Two board-level products that control graphics displays over a system bus are based on a proprietary application-specific IC. The Colorware cards, which Advanced Electronics Design Inc. is unveiling at Siggraph this week in Dallas, offload graphics control from the central processor.

"Engineering work stations need a closely coupled graphics environment," says AED product marketing manager Robert Deisher. "Some of the newer stations are providing graphics control at the board level. We are taking this [idea] a step further and providing the capability of a graphics *terminal* at the board level."

In other words, the need for a complete external graphics terminal is eliminated. All of the terminal's electronics, save that which powers and drives the cathode-ray tube in the external monitor, are pulled inside the host system. Thus the architecture becomes similar to that used for IBM Personal Computer graphics systems, although at a higher level of functionality and resolution.

AED's Colorware boards are tailored

for the Q- and VMEbus. The two-board 1280Q-GDS can be integrated into the MicroVAX II environment. A Motorola 68020 microprocessor gives the user the ability to invoke multiple concurrent text and graphics windows. Each window can emulate a terminal, such as those in the Tektronix 4100 series or Digital Equipment Corp.'s VT-100.

The 1280V-GDS, also equipped with a 68020, runs under the Unix operating system. Here, the windows are managed as virtual devices, so they're easily integrated into a system, Deisher says.

**LIST TASKS.** Both boards do digital list processing, a method of providing local manipulation of graphic segments. The onboard memory can download lists, such as macro commands, to define segments that may be combined to make a graphic object. An optional Graphics Kernel System interface is available.

AED also offers the board sets as the Graphics Display Processor, a lower-level product without the 68020 and hence lacking window management. These sets contain the ASIC processor for drawing, vectors, and raster operations.

Both pairs of systems support screen resolution of 1,280 by 1,024 pixels, a 60-Hz noninterlaced refresh rate, eight color planes, and vector drawing of 375 ns per pixel (50,000 vectors/s).

The Q-bus 1280Q-GDS costs $6,495 apiece and the VMEbus 1280V-GDS is $7,995. The 1280Q-GDP is $4,495 and the 1280V-GDP is $5,295. All will be beta-tested in the third quarter and available by year's end, Deisher says.

Advanced Electronics Design Inc., 440 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 733-3555 or (800) 538-1730 outside California [Circle 343]

# GRAPHICS BIOS GIVES PC CLONES 10% SPEED BOOST

To improve the graphics-handling capability of its Personal Computer family, IBM Corp. created the Enhanced Graphics Adapter basic I/O software. So if rivals making PC-compatible products are to remain competitive, they must have a BIOS of their own along with the EGA hardware to implement it.

Joining the onrush of EGA hardware are some new software offerings, including a proprietary version of IBM's BIOS from North Star Computers Inc. The company's BIOS runs an average of 10% faster than the comparable IBM BIOS, and it supports full graphics compatibility and functionality of the standard IBM EGA. In addition, the package is priced 20% lower than competitive products from other software suppliers offering an IBM PC BIOS. North Star charges a one-time licensing fee of $20,000 for unlimited use.

"The new BIOS can run most applications programs written for the IBM PC and its compatibles," says Charles Grant, North Star's founder and chief executive officer. "The BIOS can be implemented with industry-standard chip sets, such as those from Chips & Technologies, as well as the IBM EGA." Further, he says, the package works with any of the current adapters, monitors, and software that run on IBM's EGA BIOS. Among them are monochrome and color graphics adapters and associated software.

North Star's BIOS supports 640-by-350-pixel resolution, displaying 16 colors from a 64-color palette. Other standard features include support for a light-pen interface, bit-mapped graphics in four planes for flicker- and flash-free display, loadable fonts, user-programmable advanced character sets, palette manipulation for color changes and animation, split-screen capability, and a powerful write-string command.

The company says the BIOS has been tested on an IBM EGA card and on Chips & Technologies Inc.'s EGA chip set. It has also been extensively tested with such software programs as Digital Research's GEM, Lotus's 1-2-3, Microsoft's Windows, and others.

North Star offers its BIOS as either a loadable driver or as a ROM adapter module. Both versions use approximately 13-K bytes for executable code and tables. This leaves about 3-K bytes in a 16-K-by-8-bit PROM for additional customer-supplied test-coding extensions.

The EGA BIOS does not support any hardware testing, North Star says. It is available now. *–Jonah McLeod*

North Star Computers Inc., 14440 Catalina St., San Leandro, Calif. 94577. Phone (415) 357-8500 [Circle 342]

# MULTIUSER LINE TEAMS 80286 AND XENIX

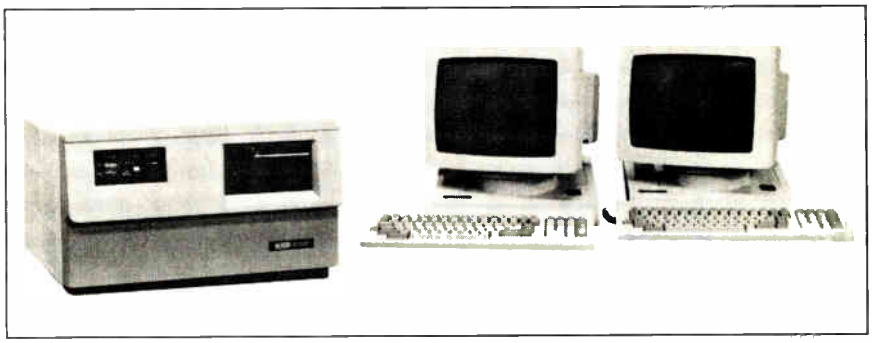
Four computers with 10-MHz 80286 microprocessors and a selection of larger, faster disk drives bring added performance to the Rexon Business Machines line. All run under Microsoft's Xenix version of AT&T's Unix operating system and are compatible with software developed for the IBM Corp. Personal Computer AT.

"Xenix System V is standard now in the multiuser business, and we wanted to make sure we had a product with fast-access disks. They are critical in the Unix world," says Robert H. Love, executive vice president. All hard-disk drives used in the new TX series have average access times of 30 ms or less.

**DESK MODELS.** Of the four machines, three are desktop models capable of handling 16 users each. They include the RX105-TX, with 51 megabytes of unformatted disk capacity and a base price of $13,270; the RX205-TX, with 85 megabytes, $15,290; and the RX305-TX, 191 megabytes, $22,290. The freestanding RX405-TX can serve up to 32 users. Its unformatted disk capacity is 227 megabytes, and base price is $26,490. All four can accommodate a second hard-disk drive to double storage capacity.

Standard equipment in the TX series includes a 1.2-megabyte 5¼-in. floppy-disk drive, a 60-megabyte ¼-in. cartridge tape drive for hard-disk backup, and 1 megabyte of main memory. An extended card cage, eight serial ports, and four parallel ports are also standard features.

Among the options available are a 80287 numeric coprocesser, a 1,600-b/in. ½-in. magnetic tape drive, additional se-



**COMBO.** Rexon's machines put the 82086 and Unix to work for business applications.

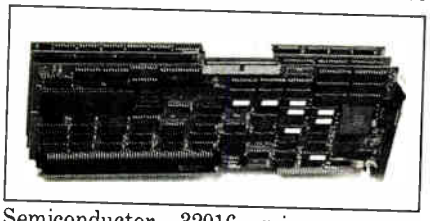
rial and parallel ports, and up to 4 megabytes of main memory. The company is also offering field upgrades for its existing systems to bring a faster 80286 to bear. *–Ellie Aguilar*

Rexon Business Machines, 5800 Uplander Way, Culver City, Calif. 90230.
Phone (213) 641-7110 [Circle 341]

## GRAPHICS SET DRAWS 20,000 VECTORS/S

The PG-1280 color-graphics board set, which supports a sceen resolution of 1,280 by 1,024 pixels, is compatible with IBM Corp.'s Professional Graphics Adapter and Color Graphics Adapter, as well as the Virtual Device Interface. The PG-1280 draws 20,000 vectors/s, 15,000 characters/s, and does bit-block transfers at 13 million pixels/s.

The heart of the PG-1280 is a National



Semiconductor 32016 microprocessor pipelined with a Hitachi 63484 graphics controller. The 32016, running at 10 MHz with 128-K bytes of EPROM firmware and 128-K bytes of RAM and using its own 32-bit internal bus, keeps the graphics load off the motherboard's CPU and minimizes traffic on the bus. The board set has a direct-memory-access port for easy transfer of complete images to the system.

The card set, which is priced at $3,995, supports 256 colors from a palette of 16.7 million. It is available now.

Matrox Electronic Systems, 1055 St. Regis Blvd., Dorval, Quebec H9P 2T4.
Phone (514) 685-2630 [Circle 345]

## CARD CRANKS OUT 18 MEGAFLOPS

The Zip 3232-20, which executes 18 million floating-point operations/s, is available now in board-level versions for Q-bus, Multibus, and VMEbus systems. A chassis version system works with the IBM Corp. Personal Computers.

For signal-processing applications, the 3232-20 does a 1,024-point complex fast Fourier transform in just 2.2 ms. For image processing, the unit can do a convolution of a 3-by-3 kernel on a 512-by-512 bit image in 221 ms.

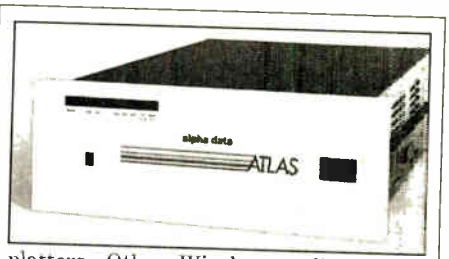
The 18-megaflops version is priced at $18,000. A 20-megaflops version will be available early next year.

Mercury Computer Systems Inc., 600 Suffolk St., Lowell, Mass. 01854.
Phone (617) 458-3100 [Circle 346]

## 76 HEADS GIVE DRIVE 18-NS ACCESS TIME

The Atlas stores 520 megabytes, yet claims to have one of the fastest access times among hard-disk drives at less than 18 ms. The drive responds to computer requests with far fewer seeks because its 76 recording heads have access to a 2.5-megabyte cylinder with no movement. Cylinder size is the number of megabytes that can be read without head movement.

The Atlas uses four 14-in. hard-disk




platters. Other Winchester disk drives offer 200-K-byte cylinders and may have to perform up to 10 new-cylinder seeks to cover the same amount of data that the Atlas can access instantly, the com-

# Score A Winning Touchdown with UMC


With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.

UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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**U.S.A. HEADQUARTERS:** NMC CORPORATION 3054 SCOTT BLVD. SANTA CLARA, CA95054 U.S.A. TEL: 408-7279239 TLX: 172730 NMC SNTA FAX: 408-9700548

pany claims. For those drives, typical access time is in the 30- to 40-ms range.

The Atlas's platters are in a sealed disk chamber that eliminates atmospheric contaminants and lets users operate the drive in harsh environments. A patented retractable-head design means heads never slide on the disk surface, even during start and stop operations.

Priced at $10,850, the Atlas 520 is available now.

Alpha Data Inc., 20750 Marilla St., Chatsworth, Calif. 91311.
Phone (818) 882-6500 [Circle 348]

## TANDEM ADDS DISTRIBUTED SYSTEMS

Tandem Computers is targeting a pair of systems at users who distribute their transaction-processing tasks at local or regional levels. The NonStop EXT10, an entry-level fault-tolerant transaction-processing system priced at $82,500, can process 4.3 transactions/s. The EXT25 is a midrange system that is 2½ times as fast; it is priced at $325,000 and can process 11 transaction/s.

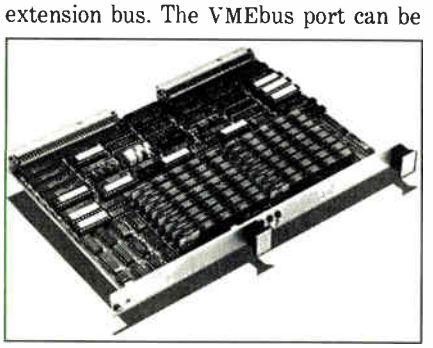
Both systems can be expanded: the EXT10 to 8.6 transactions/s, and the EXT25 to 22 transactions/s. The basic system cabinet houses two processors, two 128-megabyte 8-in. Winchester disk drives, two cartridge tape drives, a communications controller, two power supplies, and an operations and service processor. The EXT10 has 8 megabytes of RAM and the EXT25 has 16 megabytes. Both systems will be available later this quarter.

Tandem Computers Inc., 19191 Vallco Pkwy., Location 4-40, Cupertino, Calif. 95014. Phone (408) 725-6000 [Circle 349]

## RAM CARD WORKS ON VME AND VMX BUSES

The MM-6400D provides VMEbus systems with up to 4 megabytes of dual-ported dynamic RAM. The memory card makes use of DRAM chips in single in-line packages and also comes in 1-, 2-, and 3-megabyte versions, transferring data at rates up to 12 megabytes/s.

The MM-6400D boosts system performance because it can transfer data over either the main VMEbus or the VMX extension bus. The VMEbus port can be disabled by a lock signal from the VMX bus that transforms the memory module into a single-port memory accessible only by the VMX bus. The MM-6400D is available in four weeks; a 4-megabyte version sells for $2,395.

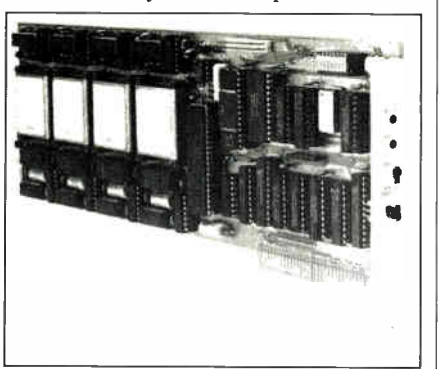


Micro Memory Inc., 9540 Vassar Ave., Chatsworth, Calif. 91311.
Phone (818) 998-0070 [Circle 347]

## BUBBLE MEMORY WORKS IN IBM PCs

Bubble-memory mass-storage systems are now available for the IBM Corp. Personal Computer, PC/XT, and PC AT. The PCI-1 provides 512-K bytes of memory on a single PC expansion card.

The memory card incorporates intelligent control firmware and circuitry that handles bubble-device formatting and control, interfaces the bubble-memory system to the PC's bus structure, and provides for both soft- and hard-error detection and correction. The PCI-1 can be operated as either a floppy- or a hard-disk drive and is compatible with both PC-DOS and MS-DOS.



Available in 30 days, a 512-K-byte version sells for $1,111.

Bubbl-Tec, 6805 Sierra Court, Dublin, Calif. 94568. Phone (415) 829-8700 [Circle 351]

## CARD EMULATES MAINFRAME PRINTERS

Instead of purchasing an expensive 3287 printer for use with IBM Corp. mainframe computers, customers can employ personal computer printers, thanks to a card that emulates the 3287. Typical personal computer printers are in the $1,000 price range, compared with the $8,000 cost of printers for mainframes.

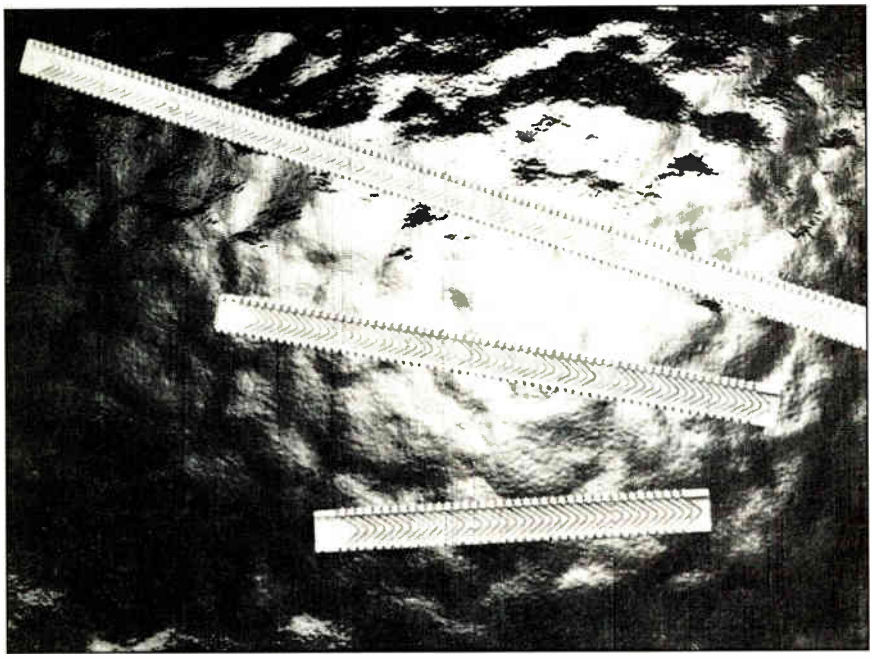
The IDEAcomm 3287 software-driven printer control panel duplicates all the features of the 3287 printer.

Available now, the card is priced at $795.

IDE Associates Inc., 29 Dunham Rd., Billerica, Mass. 01821.
Phone (617) 663-6878 [Circle 350]

# A NEW ASSEMBLY METHOD FOR FLAT-PANEL DISPLAY

## ITT-CANNON'S PARALLEL INTERCONNECT, A THIN CONTACT WITH ALIGNMENT POSTS, USES NO SOLDER OR CLIPS



**SECOND USE.** The Parallel Interconnect can also be used to stack pc boards closely together.

One of the major challenges facing flat-panel display designers is assembling the board, the glass, and front- and back-mounting bezels in a damage-free and reliable way. Coming to their aid is the Parallel Interconnect, a solderless, high-density pin-and-post device from the Cannon Division of ITT Corp.

The Parallel Interconnect's thermal coefficient of linear expansion closely matches that of the glass and the pc board, providing long-term reliability. "In display applications, an optional frame can be provided that sandwiches the glass, connector, and pc board together," says William J. Clark, director of new product development for ITT Cannon's Commercial Interconnect Division. "The result is a gas-tight, reliable interconnect."

**STAMPED CONTACTS.** The PI features a copper-alloy blanked contact in an array of housing cavities. Contacts, which are stamped by flat-pattern blanking, are retained in the housing by a slip-in plastic cover. The contact alloy and thickness can be readily altered to meet various electrical requirements.

The solderless approach creates a number of benefits for users, Clark says. For starters, not soldering each contact increases the yield (number of good connections) and reduces the need for testing and reworking joints. Also, soldering requires a great deal of skill, and boards or components can easily be damaged by operator slipups.

Besides its flat-panel display applications, the Parallel Interconnect is also useful in closely stacking pc boards in parallel, reducing the space needed for board-to-board interconnections in computers or telecommunications gear to as little as 0.275 in. Boards stacked in parallel are typically spaced from ½ to 2 in. apart, depending on the types of components they carry. "This makes the connector ideal for surface-mounting applications," Clark says.

Though made to order, the PI is also available in standard configurations that can be delivered in six to eight weeks after ordering. A low-profile product, the PI features 0.275-in. board-to-glass or board-to-board separation with contacts available on a 0.030-in. grid in the standard configuration. Average contact resistance is 30 mΩ, very low for this type of interconnect. The PI is environmentally tested against vibration, corrosive atmosphere, and thermal and mechanical shock.

In flat-panel display design, the PI system replaces a variety of less reliable and more troublesome interconnection and assembly methods. Among them are flat flexible circuitry, which must be soldered in place; mechanical clips, which are tricky to position; and elastomeric connectors, which have high resistance and can't be repaired.

The PI ensures accurate placement by means of aligning posts, which are pressed into position in the interconnect body. Pins that fit into accurately drilled holes in the board guarantee quick and positive alignment. The glass is aligned with three posts pressed into the pc board to correspond to the same alignment posts used to position the glass during manufacturing.

The company has also designed an assembly press incorporating jigs and fixtures to hold the components of the assembly. First the bottom aluminum bezel is placed, then a board is put in the jig, the connector is placed on the alignment pins, the glass is positioned, and finally the top bezel and rivets are affixed. The machine compresses the assembly and rivets it together in less than 1 min per unit. The device is sold separately for $15,000, but customers may use the PI interconnect system without it.

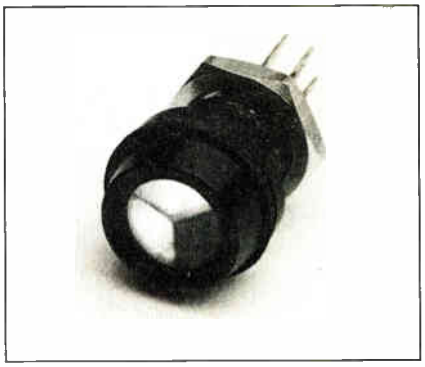
PI connectors are priced at 0.035c to 0.065c per connection line, depending on size of the connector and quantity ordered. *–Steve Zollo*

ITT Corp., Cannon Division, P. O. Box 8040, Fountain Valley, Calif. 92728. Phone (714) 964-7400 [Circle 400]

## TRICOLOR LEDs PROVIDE 8 SIGNALS

Special optics in the Oxley three-in-one LED indicators provide a three-color display that can be used to show up to eight different visual signals in combinations of red, green, and yellow.

The LED is ruggedly housed in a black anodized aluminum case that is sealed to withstand 65 ft of seawater; the thermal flash-proof lens and O-ring sealing provide full environmental protection. The lamps are therefore suited for equipment designed to withstand a salt-laden atmosphere, in accordance with MIL-STD-810.



Applications include battery-condition indicators, process controllers, and mimic diagrams. Available from stock, the LEDs are priced at $25 each in small quantities. They can also be ordered in two-color versions—red and green, for example.

Oxley Inc., 25 Business Park Dr., P. O. Box 814, Branford, Conn. 06405.
Phone (203) 488-1033 [Circle 406]

## 500-V MOS FETs SAVE MOUNTING COSTS

The combination of SGS Semiconductor Corp.'s packaging talent and Siliconix Inc.'s power MOS FET expertise is producing a line of high-power n-channel MOS devices featuring an easy-to-mount, electrically isolated package. The initial products are the 2N7056 and 2N7059. Both are available now.

The 2N7059 is a 500-V device with 9-A continuous current rating and a maximum on-resistance of 0.45 Ω. It's suited for off-line power supplies operating at 100-kHz or more and providing 200 W to 2 kW of power. The 200-V 2N7056 has an on-resistance of 100 mΩ and 19-A continuous current rating.

Housing the devices is the Isowatt218 package, which incorporates a proprietary over-mold technique to provide 4,000-V peak isolation (with a 70-W power dissipation) between the internal package electrical points and the heat sink or mounting surface. This feature means easier assembly and reduced costs for the user, since it eliminates all insulation layers and mechanical standoffs. Yet it maintains safety and complies with UL and VDE isolation standards.

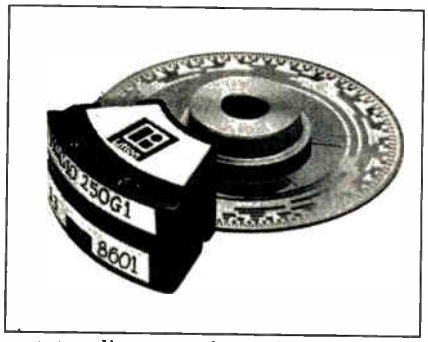
Siliconix prices the MOS FETs starting at $3.95 in lots of 10,000. SGS pricing was unavailable.

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, Ariz. 85022.
Phone (602) 867-6100 [Circle 405]
Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, Calif. 95054.
Phone (408) 988-8000 [Circle 415]

## OPTICAL ENCODER TAKES UP LITTLE ROOM

The model MGC modular absolute encoder is a compact device that suits factory-automation gear, machine tools, medical equipment, and sonar scanning systems. The low-profile encoder uses LED light sources and phototransistors to generate a 10-bit parallel gray code output.

The phototransistor outputs can be buffered by the user to interface with TTL, CMOS, and other logic families. Three hub sizes are available: ¼-in., ⅜-in., and ½-in. The encoder has a maximum 1.16-in. radius for reading a code wheel, a height of 0.57 in., and a commutator diameter of 1.78 in.

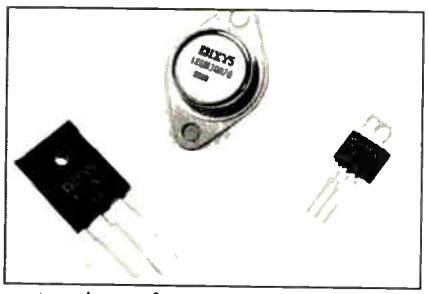


The MGC is mounted by the user onto an existing shaft-and-bearing assembly. Pricing and delivery information for the encoder was unavailable.

Litton Systems Inc., Litton Encoder, 20745 Nordhoff St., Chatsworth, Calif. 91311.
Phone (818) 341-6161 [Circle 408]

## 30-A TRANSISTOR CHALLENGES SCRs

At 30 A, the MOS insulated-gate transistor can challenge such bipolar devices as silicon controlled rectifiers and darlington transistors. The Mosigt monolithic power transistors combine polysilicon-gate MOS technology—for simplified drive circuitry—with bipolar power-handling capability to give 10 times the current ratings of MOS FETs.



Turn-off times have been reduced by a factor of four, down to typical fall times of 500 to 800 ns. The IXGH30N80 800-V, 30-A Mosigt, a 67,000-mil² single chip, can withstand surges of 100 A at 150°C without latching. The gate capacitance of the IXGH30N60, a 600-V, 30-A chip, is just 2,800 pF; and for the IXGH20N60, a 600-V, 20-A device, it is 1,800 pF. The 30-A parts are priced at $27.36 in lots of 100, and the 20-A model is $15.96 in like quantites. They are available now.

Ixys Corp., 142 Charcot Ave., San Jose, Calif. 95131.
Phone (408) 435-1033 [Circle 412]

## SOCKETS BOW FOR J-LEADED PACKAGES

Sockets are now available for the 26-pin small-outline J-leaded package that is currently pending Jedec approval. The socket's contact system prevents damage to the device leads and loss of lead coplanarity, with its subsequent mounting problems.

The SOJ socket, which is compatible with existing sockets, offers dead-bud device loading. Its body is polyetherimide and the contacts are beryllium copper with gold plating. The maximum temperature capability is 170°C.

Priced at $9.90 each in lots of 1,000, the sockets are available in eight weeks.

Nepenthe, 2471 E. Bayshore Rd., Palo Alto, Calif. 94303.
Phone (415) 856-9332 [Circle 410]

## TOSHIBA RED LEDs EMIT 3,000 mcd

The TLRA line of red LEDs boasts a luminous intensity of up to 3,000 millicandelas. The diodes are made from gallium arsenide and emit light at a wavelength of 660 nm.

The LEDs achieve a high emission efficiency thanks to a double heterostructure, with an active layer sandwiched between a p layer and a high-aluminum-mixture n layer.

With an input current of 20 mA, the TLRA120 series delivers up to 900 mcd, typically with a ±20° half-viewing angle; the TLRA135 series delivers up to 1,500 mcd with a ±8° half-viewing angle; and the TLRA150, up to 3,000 mcd with a ±4° half-viewing angle. Lighting linearity allows operation from dc or pulse sources.

Prices range from $1.30 to $3.00 each in lots of 100. Delivery takes six weeks.

Toshiba America Inc., 2692 Dow Ave., Tustin, Calif. 92680.
Phone (714) 832-6300 [Circle 409]

## CERAMIC CAPACITORS CAN BE TRIMMED

The Cera-trim line of surface-mountable ceramic dielectric capacitors can be trimmed in capacitance ranges from 0.6 to 2.5 pF through 5.0 to 25 pF. The high-Q ceramic dielectric enables Cera-trim to operate from dc to microwave frequencies at temperature ranges of −55°C to +125°C.

In addition, because Cera-trim is sealed, it is impervious to solder fluxes, cleaning solvents, and most other manufacturing, atmospheric, and environmental conditions. Cera-trim withstands 275°C soldering for 20 s.

Cera-trim was configured for automated index and placement and is compatible with existing tape-and-reel and cartridge-installation techniques. The capacitors measure 0.165 by 0.180 by 0.090 in. Priced at 80¢ each in lots of 1,000, they will be available in four to eight weeks.

Johanson Manufacturing Corp., Rockaway Valley Rd., Boonton, N. J. 07005.
Phone (201) 334-2676 [Circle 407]

# LOW-COST PLOTTER BOWS FOR PC-BASED CAD

## HP'S DRAFTPRO USES THE SAME TECHNOLOGY AS ITS 7580 LINE, BUT COSTS ONLY $5,400

Hewlett-Packard Co. is adding the missing piece of equipment to the low-cost, personal-computer-based computer-aided design market: an inexpensive plotter that handles C- and D-size media. The HP 7570 DraftPro, which employs the same technology as HP's tried-and-true but more costly 7580 family of plotters, is priced at $5,400.

"HP designed the low-price DraftPro to go along with the low price tag of personal computer-based CAD systems," says Richard A. Mayes, marketing manager for the San Diego Division. The target is work stations that range in price from $10,000 to $30,000 per seat. Though personal computer-based work stations are less expensive, they are no less professional than the top-tier CAD systems, he says.

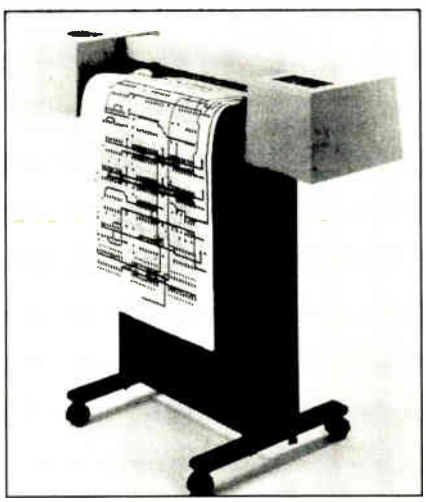
Compatible with most personal computers—including the Apple Macintosh, HP's own Vectra, and the IBM Corp. Personal Computer—the DraftPro plotter is supported by such widely used CAD packages as Anvil-1000, AutoCad, and VersaCAD. It features a 2-g pen acceleration and a 15-in./s pen speed. With a 0.001-in. addressable resolution and linear accuracy to within 0.2%, the device plots 1,000 dots/in.

**MULTIMEDIA.** The plotter works on paper, vellum, and double-matte polyester film at widths of 550 to 640 mm and lengths of 400 to 1,000 mm. These measurements include C- and D-size media as well as the A2/C A1/D architectural media sizes. The plotter uses disposable fiber-tip pens or refillable liquid-ink drafting pens.

An eight-pen carousel features automatic pen changing and pen capping. The pen sorting is independent of software, so the plotter can draw a full buffer of vectors for one color before proceeding to another. This reduces plot time by minimizing the number of pen changes.

"Reliability at a low price is the key feature of the new eight-pen DraftPro," says Mayes. Both goals were achieved through design simplicity and rigorous environmental testing, he says.

The plotter's design incorporates plastic-injection molding and very large-scale integration, both of which reduce the overall parts count and therefore the number of potential failure points resulting from continual daily use. Mayes says there has been a 10-to-1 parts reduction compared with the 7580 machines, which are targeted at CAD systems in the $100,000-per-seat price range. And the use of injection molding—a way to integrate functions mechanically into single parts—enabled HP to reduce manufacturing costs.



**FEWER PARTS.** HP hiked plotter reliability by lowering parts count as much as 10:1.

Environmental testing included operating the plotter at temperatures from 0°C to 55°C, subjecting it to a 25,000-V shock, exposing it to a blowtorch, and jolting it with 50 times the acceleration of gravity.

The plotter features a simple paper-loading procedure, front-panel controls that can be learned quickly, and the HP-GL graphics language for user programming. An RS-232-C interface is standard; an IEEE-488 interface and the Japanese Kanji character set are available as plug-in accessories.

The plotter is mounted on casters so it can easily be moved from department to department. Delivery takes two weeks after ordering. *–Steve Zollo*

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 380]

## PACKAGE CHECKS FOR FAULTS IN NET LISTS

A software product called Qwikcheck allows users of the FutureNet's IBM Personal Computer-based Dash work stations to check netlists for design-rule wiring errors. For example, engineers can use Qwikcheck to analyze their netlists for single wires, shorted nets, and duplicated wires.

Users can then eliminate those errors before the design goes into production, when it becomes more costly to weed them out. Also included is a communications utility that transmits the data to the Qwikcheck manufacturer's VAX computer, where it is converted to the data bases needed for automated manufacturing of the pc board.

The $95 package is available now on 5¼-in. floppy disks.

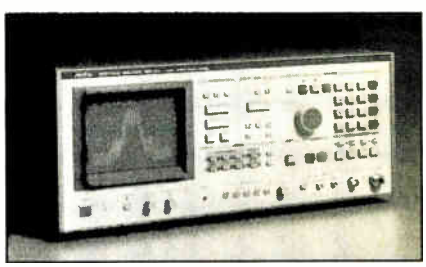
Augat Inc., Interconnections Systems Division, 40 Perry Ave., P. O. Box 1037, Attleboro, Mass., 02703.
Phone (617) 222-2202 [Circle 388]

## SPECTRUM ANALYZER REACHES 140 GHz

A new series of microwave spectrum analyzers can measure over a range of 10 kHz to 140 GHz. The MS710C, MS710D, MS710E, and MS710F have both 300- and 100-Hz resolution bandwidths and a dynamic range of 100 dB.

Up to nine measurement setups can be stored in the analyzers' memory. The analyzers have an IEEE-488 interface to support plotters.

The base frequency range of the MS710 is 100 kHz to 23 GHz. A low-band option permits measurements from 10 to 30 kHz. The MS710C and 710D reach the



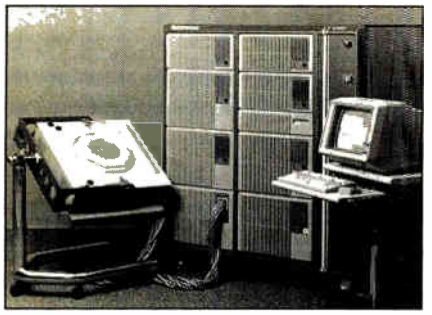
140-GHz mark through the use of external mixers. Pricing ranges from $25,050 to $32,000. Delivery takes up to 12 weeks.

Anritsu America Inc., 15 Thornton Rd., Oakland, N. J. 07436.
Phone (201) 337-1111 [Circle 387]

## 256-PIN TESTER TARGETS CMOS ASICs

The LT-1000 50-MHz test system is targeted at the production testing and incoming inspection of CMOS application-specific ICs. With 256 pins, the system accommodates a wide variety of wafer probers and automated device handlers to permit use with gate arrays, custom, semicustom, and standard CMOS ICs.

To keep operational costs of ASIC testing low, the LT-1000 provides a highly interactive test-development environment that features automatic program generation and links to computer-aided-design data bases.



Key to the system's performance is its integrated pin electronics. Most of the circuitry that connects directly to the device under test to provide timing and drive voltages and to acquire response measurements is condensed into two custom monolithic ICs per test channel.

A typical configuration of the LT-1000 test station is priced at $650,000. Delivery will begin in early 1987.

Tektronix Inc., P. O. Box 4600, Beaverton, Ore., 97075.
Phone (503) 629-1035 [Circle 385]

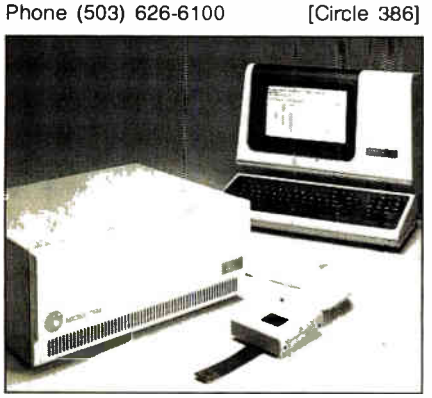
## EMULATORS WORK WITH 24-MHz 68010s

While most in-circuit emulators can go up to only 12.5 MHz, the ECU series of in-circuit emulators for the 68000 and 68010 microprocessors features a zero-wait-state operation up to 16.6 MHz and one-wait-state operation up to 24 MHz.

The emulator can have up to 2 megabytes of overlay memory, which can be mapped as read and write access, read only, or no-access. The overlay memory mapped as RAM will allow read or write access, and ROM-mapped overlay memory will ignore write cycles. Any access to those areas protected with a no-access qualifier will cause emulation to break.

The ECU series has 32 hardware triggers, each with its own counter, a 4-K trace buffer accessible during full-speed emulation, and sophisticated macros that support C-like language structures. The emulator is priced at $10,490. Delivery will begin in September.

Microcosm, 15275 S. W. Koll Pkwy., Suite E, Beaverton, Ore. 97006.
Phone (503) 626-6100 [Circle 386]

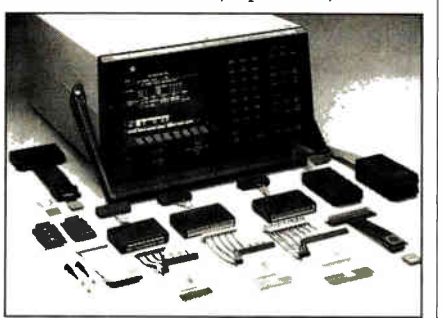


## ANALYZER LINE ADDS 80286 DISASSEMBLER

A line of logic analyzers now includes software and hardware disassembler suport for the 16-bit 80286 microprocessor. The disassembler can be used with the Philips' entire line of logic analyzers, including the PM 3551A, PM 3565, and the PM 3570.

Disassembly involves the translation of 80286 states into mnemonics closely related to the programmer's assembly source code. Hardware support consists of an easy-to-install front-end unit that assures proper connection of the logic analyzer channels to the 68-pin-grid array package of the 80286.

Software support comes in a PROM-based package fitted on the option board of the analyzer. Up to four different packages can reside inside the instrument. Addresses, operands, and ad-



dressing mode are clearly displayed in addition to the mnemonics.

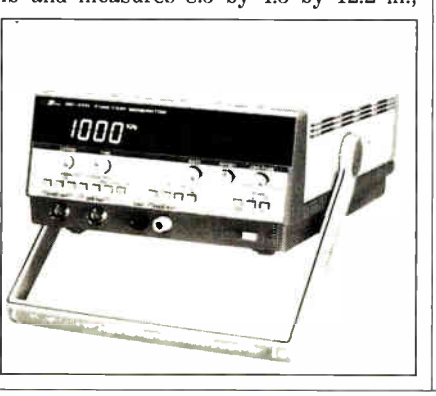
Pricing and delivery information was unavailable.

Philips Test & Measurement Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430.
Phone (201) 529-3800 [Circle 390]

## FUNCTION GENERATOR IS ACCURATE TO ±2%

Accuracy to within ±2% is the boast of Iwatsu's model SG-4101 function generator. The instrument has a frequency range from 0.1 Hz to 1 MHz in seven ranges with 3½-digit resolution.

It features 20-V peak-to-peak outputs, TTL synchronization-pulse output, and dual outputs with 50- and 600-Ω impedance. The generator, which weighs 5.7 lb and measures 8.3 by 4.3 by 12.2 in., has a large LED display for easy reading. Available now, the SG-4101 sells for $395.




Iwatsu Instruments, 430 Commerce Blvd., Carlstadt, N. J. 07072.
Phone (201) 935-5220 [Circle 392]

## 8086 EMULATOR OPERATES AT 10 MHz

An in-circuit emulator for the Intel 16-bit 8086 microprocessor runs at 10 MHz, the full rated speed of the processor. The emulator can run as a stand-alone system or it can operate with a variety of computers, including those from Apollo Computer, Digital Equipment, IBM and Sun Microsystems.

The emulator provides a look at all bus and control signals, as well as full 16-bit address and data widths, using trace modes. A wide and deep trace memory allows capture of 2,046 words, each 72 bits wide, to reveal the actual sequence of execution.

The unit includes the company's event monitor system, which allows an engineer to control emulation by breaking on any combination of address, data, status, pass counter, and logic state fields.

Priced at $10,495, the emulator is available now.

Applied Microsystems Corp., 5020 148th Ave., N. E., P. O. Box 97002, Redmond, Wash. 98073.
Phone (206) 882-2000 [Circle 393]

## CAD SOFTWARE DOES ALL METAL ROUTING

A computer-aided-design layout tool provides interactive logic placement and 100% of an IC's metal routing. The company says Blocks accelerates the design of application-specific ICs because it allows designers to cost-effectively examine any number of layout configurations and evaluate the results.

Blocks includes such features as gridless routing for increasing density, compatibility with standard-cell libraries, ports on all block sides, irregular block shapes, hierarchical layout, multilayer interconnects, and on-screen menus. All information required by Blocks is in a transparent central data base, including definitions, circuit descriptions, user information, and a standard-cell library.

An average circuit of 400 blocks and 400 signals takes two to five days to lay out, the company says. During successive cycles, initial placement will be completed in 10 minutes, and rerouting will take about 2 minutes.

The single-copy price of Blocks is $50,000. It is available now.

DeNies Resources Inc., 4320 Stevens Creek Blvd., Suite 120, San Jose, Calif. 95129. Phone (408) 247-6200 [Circle 391]

## MEETINGS

**Satellite Communications Users Conference,** Satellite Communications Magazine (Kathy Kriner, 6530 S. Yosemite St., Englewood, Colo. 80111), Bally's Grand Hotel, Las Vegas, Sept. 9-11.

**European Simulation Congress,** Society for Computer Simulation, *et al.* (Ghislain C. Vansteenkiste, University of Ghent, Coupure Links 653, B-9000 Ghent, Belgium), Antwerp, Belgium, Sept. 9-12.

**Electronic Materials Management Conference,** Electronic Materials Report (111 Main St., Los Altos, Calif. 94022), Hyatt Regency Hotel, Palo Alto, Sept. 10-12.

**1986 Bipolar Circuits and Technology Meeting,** IEEE (John Shier, VTC Inc., 2800 E. Old Shakopee Rd., Bloomington, Minn. 55420), Hyatt Regency Hotel, Minneapolis, Sept. 11-12.

**Intelevent '86,** E. F. Hutton & Co. *et al.* (Marianne Berrigan, Executive Director, 1120 Connecticut Ave. N. W., Suite 1144, Washington, D. C. 20036), Hotel Bayerischer Hof, Munich, Sept. 14-17.

**Fiber LASE '86,** Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227), Hyatt Regency Hotel, Cambridge, Mass., Sept. 14-26.

**1986 IEEE International Electronic Manufacturing Technology Symposium,** Components, Hybrids, & Manufacturing Technology Society of the IEEE (IEEE Council Office, 701 Welch Rd., Suite 2205, Palo Alto, Calif. 94304), Hilton & Tower, San Francisco, Sept. 15-17.

**Independent Power Generation Conference and Exhibition,** Fuel and Metallurgical Journals Ltd. (2 Queensway, Redhill, Surrey RH1 1QS, UK), Excelsior Hotel, London, Sept. 16-17.

**IEEE Symposium on Logic Programming,** IEEE Computer Society (1730 Massachusetts Ave. N. W., Washington, D. C. 20036), Westin Hotel Utah, Salt Lake City, Sept. 21-25.

**Electronics and Aerospace Systems Conference '86,** IEEE (Dr. Arvid G. Larson, Vice President, Analytic Disciplines Inc., Suite 400, 2070 Chain Bridge Rd., Vienna, Va. 22180), Shoreham Hotel, Washington, Sept. 22-24.

**Ultratech Conferences and Expositions,** Society of Manufacturing Engineers *et al.* (P. O. Box 930, Dearborn, Mich. 48121), Convention Center, Long Beach, Calif., Sept. 22-25.

**Buscon/East-86,** Multidynamics Inc. (17100 Norwalk Blvd., No. 116, Cerritos, Calif. 90701), World Trade Center, Boston, Sept. 23-24.

**Nepcon Southwest,** Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), Infomart, Dallas, Sept. 23-24.

**Artificial Intelligence & Advanced Computer Technology Conference and Exhibition/Europa '86,** Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Rhein-Main Halle, Wiesbaden, West Germany, Sept. 23-25.

**Engineering and Manufacturing Software Conference/Exhibition,** Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Chicago Hilton and Towers, Chicago, Sept. 23-25.

**International Test & Measurement Exhibition,** Gambica (Network Events Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK), Grand Hall Olympia, London, Sept. 23-25.

**1986 International Symposium on Gallium Arsenide and Related Compounds,** (W. T. Lindley, Room E118E, Massachussetts Institute of Technology-Lincoln Laboratory, 244 Wood St., Lexington, Mass. 02173), Caesar's Palace, Las Vegas, Sept. 28-Oct. 1.

**IECON '86,** International Industrial Electronics Conference, IEEE (Richard C. Born, Rexnord Inc., 5101 W. Beloit Rd., Milwaukee, Wis. 53214), Hyatt Regency Hotel, Milwaukee, Sept. 28-Oct. 3.

**1986 Applied Superconductivity Conference,** IEEE (Lahni Blohm, ASC86, Code 6630C, Naval Research Laboratory, Washington, D. C. 20375), Hyatt Regency on the Harbor, Baltimore, Sept. 28-Oct. 3.

**1986 National Communications Forum,** National Engineering Consortium (505 N. Lake Shore Dr., Suite 4808, Chicago, Ill. 60611), Ramada Hotel O'Hare, Rosemont, Ill., Sept. 29-Oct. 1.

**Satech '86,** Intertec Communications Inc. (Sam Davis, Conference Director, 2472 Eastman Ave., Bldg. 34, Ventura, Calif. 93003), Indiana Convention Center & Hoosier Dome, Indianapolis, Sept. 29-Oct. 3.

**Automated Design and Engineering for Electronics East,** Cahners Exposition Group (1350 E. Touhy Ave., P. O. Box 5060, Des Plaines, Ill. 60017), World Trade Center, Boston, Sept. 30-Oct. 2.

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# ELECTRONICS WEEK

## THREE GIANTS SIGN CUSTOM CHIP DEAL

General Electric, Siemens, and Toshiba are developing a common standard-cell library for their semicustom chip businesses. The multinational companies will base the library on 1.5-μm CMOS technology, and initial development will include 160 macrocells and memory blocks. The library will be available this year, and a more complex set of high-performance macrocells utilizing 1.2-μm technology will be ready by 1988.

## GI BUYS M/A-COM's CABLE-TV DIVISION

New York's General Instrument Corp., expanding its presence in the cable-TV business, has agreed to acquire M/A-Com Inc.'s Cable/Home Communications Division for $220 million. The division includes M/A-Com's Comm/Scope coaxial cable business, its VideoCipher encryption equipment, and Prodelin & Converter, a maker of C- and $K_u$-band satellite receiving antennas and baseband and radio-frequency cable-television equipment. GI will retain Frank Drendel, an M/A-Com executive vice president and vice chairman, as the Hickory, N. C., division's manager.

## HARRIS MOVES INTO CAD SOFTWARE

Harris Corp. is buying out Scientific Calculations Inc., a computer-aided-design software house based in Fishers, N. Y. Harris, of Melbourne, Fla., says the deal makes it the only computer manufacturer that also develops and supports its own software for CAD applications in both mechanical and electronic design. Scientific Calculations' products include Scicards, a popular program for laying out printed-circuit boards and thick-film hybrid microcircuits [*Electronics*, Oct. 7, 1985, p. 62]. Scientific Calculations will operate within the Harris Computer Systems Division. Harris says the takeover will not affect the software house's relationship with IBM Corp. and DEC, who are two of Harris's biggest competitors.

## NTT SEEKS HELP IN VIDEO PHONES

Nippon Telegraph & Telephone Corp. is soliciting Japanese and foreign components makers to participate in the research on and development of Track III, a 64-kb/s video encoding and decoding system for use in video telephone systems. The Tokyo telecommunications company says the goal of Track III is to create a line of equipment that can encode 4-MHz-band NTSC color TV signals of subjects with limited motion into 64-kb/s digital signals that can be decoded after transmission.

## CRAY SPEEDS UP ITS X-MP LINE

Cray Research Inc. is boosting performance on its X-MP series of supercomputers 12% by using an 8.5-ns clock rate instead of the earlier 9.5-ns standard. The Minneapolis company says it is also cutting prices on its one- and two-processor systems by up to 20%, and is making two new models available. The $12 million X-MP/44 has four central processing units sharing a 4-million-word emitter-coupled-logic memory, and the $7 million X-MP/22 has two CPUs sharing a 2-million-word CMOS memory.

## IC DEMAND KEEPS PACE WITH MARKET

Demand for integrated circuits is growing, but it isn't outpacing overall demand for electronic components, Ceeris International Inc. contends. The Old Lyme, Conn., marketing consultant disputes other analysts' projections that ICs will capture a major share of the component business at the expense of discrete and passive parts. Consumption of ICs, in relation to total component consumption between 1980 and 1984, is stable, the company's report says. Demand for discrete components is growing at a 26% annual clip, compared with the 21% growth rate for ICs and the 18% rate for all electronic components.

## NBS ESTABLISHES OPEN SYSTEMS NET

The National Bureau of Standards is setting up Osinet, an experimental computer network based on open-systems-interconnection standards. The network is intended to encourage industry and government to use the International Organization for Standardization's OSI reference model, which allows different manufacturers' computers to communicate with each other. The NBS plan allows for 25 cooperating organizations to build, verify, and demonstrate OSI test systems and to conduct related research. Participants include General Motors, IBM, and the U. S. Navy.

## DOD LASER WORK MAY PEAK BY 1989

U. S. research funding for military laser technology—worth about $3.2 billion this year—will peak at $3.9 billion by 1989, according to a study by Frost & Sullivan Inc. Spearheaded by the Strategic Defense Initiative, space armament research accounts for 26.3%, the largest chunk of those funds, the New York market researcher says, with more conventional missile programs taking 24.7% of the research money.

## GTE BUYS AIR PHONE SERVICE

GTE Corp., Stamford, Conn., is purchasing Airfone Inc., an airline-passenger telephone service based in Oak Brook, Ill. Airfone has been operating under an experimental license from the Federal Communications Commission since 1984 [*Electronics*, Dec. 9, 1985, p. 22]. It will become part of the business services unit of GTE's Telephone Operating Group. The service is now available on more than 300 domestic airliners, and a new version, Railfone, is being offered on Amtrak's Metroliner service between Washington and New York.

## GERMANY TO GET FIRST FIBER PLANT

Responding to the exploding demand for optical fibers, Siecor Corp., a joint venture of Munich-based Siemens AG and Corning Glass Works in Corning, N. Y., is putting up a glass-fiber manufacturing plant in Neustadt, Bavaria. It will be West Germany's first such facility for volume fiber production. The $50 million plant will initially have an annual capacity of 60,000 miles of fiber.

## SERVICE INDUSTRY MERGERS RISE

Mergers and acquisitions among computer software and services companies rose in the first half of the year, continuing a 15-year trend. According to the Adapso/Broadview Index, 130 transactions were reported in the first six months of 1986, compared with 82 for the same period of 1985.

## AT&T TO BUILD AIR TRAFFIC LINK

The Federal Aviation Administration has picked AT&T Corp. to design, test, and manufacture a new voice and signaling system to control communications between air-traffic controllers and pilots. It will be installed at 2,035 locations over the next six years. The initial contract award is worth $66 million with a total value of over $120 million.

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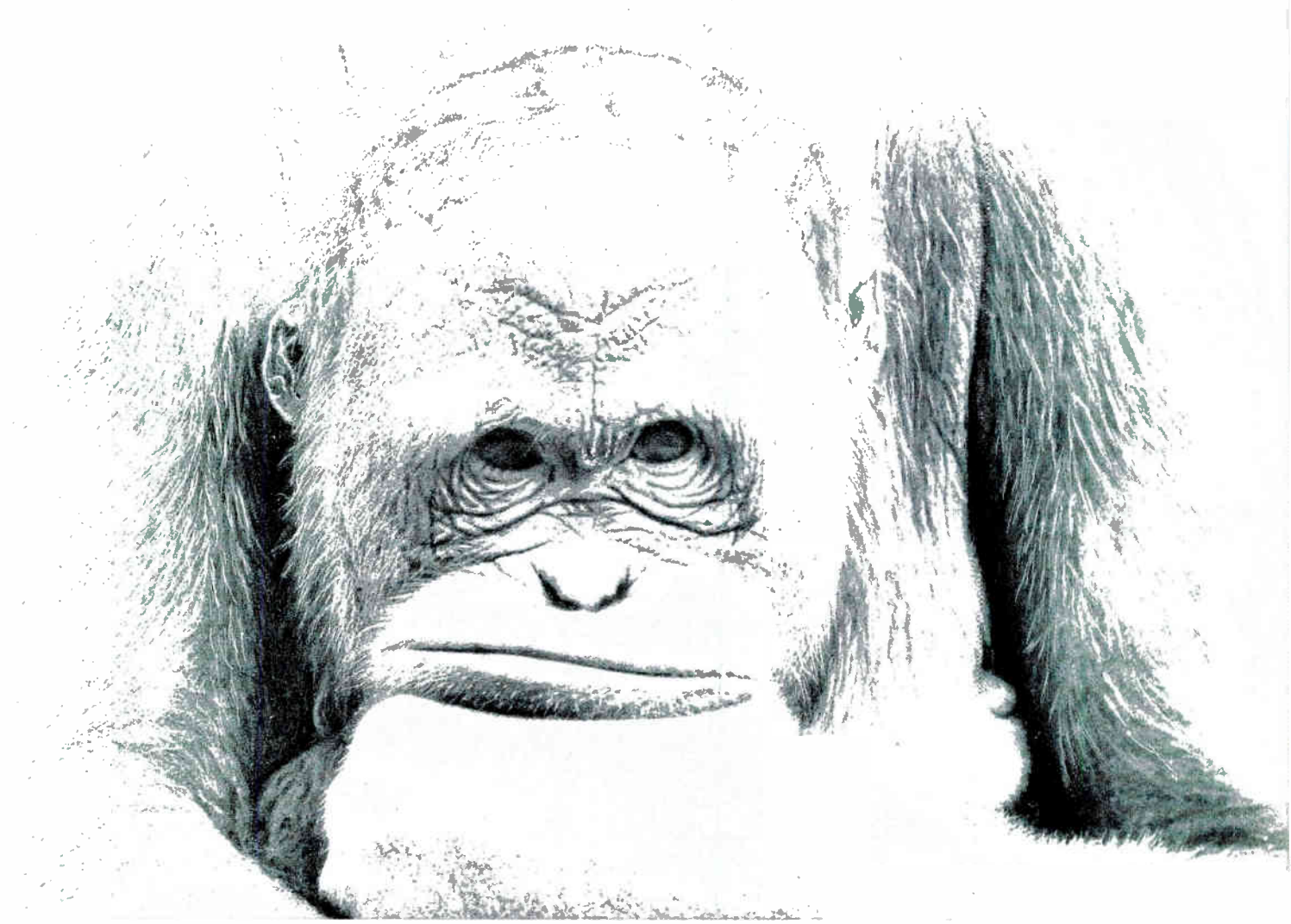

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Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

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*TLC-363* *TLC-402*

## Specifications

| | | TLC-402 | TLC-363B |
|---|---|---|---|
| **Display** | | | |
| Number of Characters | | 80×25 (2,000 characters) | 80×25 (2,000 characters) |
| Dot Format | | 8×8, alpha-numeric | 8×8, alpha-numeric |
| Overall Dimensions (W × H × D) | | 274.8×240.6×17.0 mm | 275.0×126.0×15.0 mm |
| **Maximum Ratings** | | | |
| Storage Temperature | | −20° – 70° C | −20° – 70° C |
| Operating Temperature | | 0° – 50° C | 0° – 50° C |
| Supply Voltage | $V_{DD}$ | 7 V | 7 V |
| | $V_{DD} - V_{EE}$ | 20 V | 20 V |
| Input Voltage | | $0 \leq V_{IN} \leq V_{DD}$ | $V_{SS} \leq V_{IN} \leq V_{DD}$ |
| **Recommended Operating Conditions** | | | |
| Supply Voltage | $V_{DD}$ | 5±0.25V | 5±0.25V |
| | $V_{EE}$ | −11±3V Var. | −11±3V Var. |
| Input Voltage | High | $V_{DD}$ − 0.5V min. | $V_{DD}$ − 0.5V min. |
| | Low | 0.5V max. | 0.5V max. |
| **Typical Characteristics (25°C)** | | | |
| Response Time | Turn ON | 300 ms | 300 ms |
| | Turn OFF | 300 ms | 300 ms |
| Contrast Ratio | | 3 | 3 |
| Viewing Angle | | 15 – 35 degrees | 15 – 35 degrees |

Design and specifications are subject to change without notice.

# TOSHIBA

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