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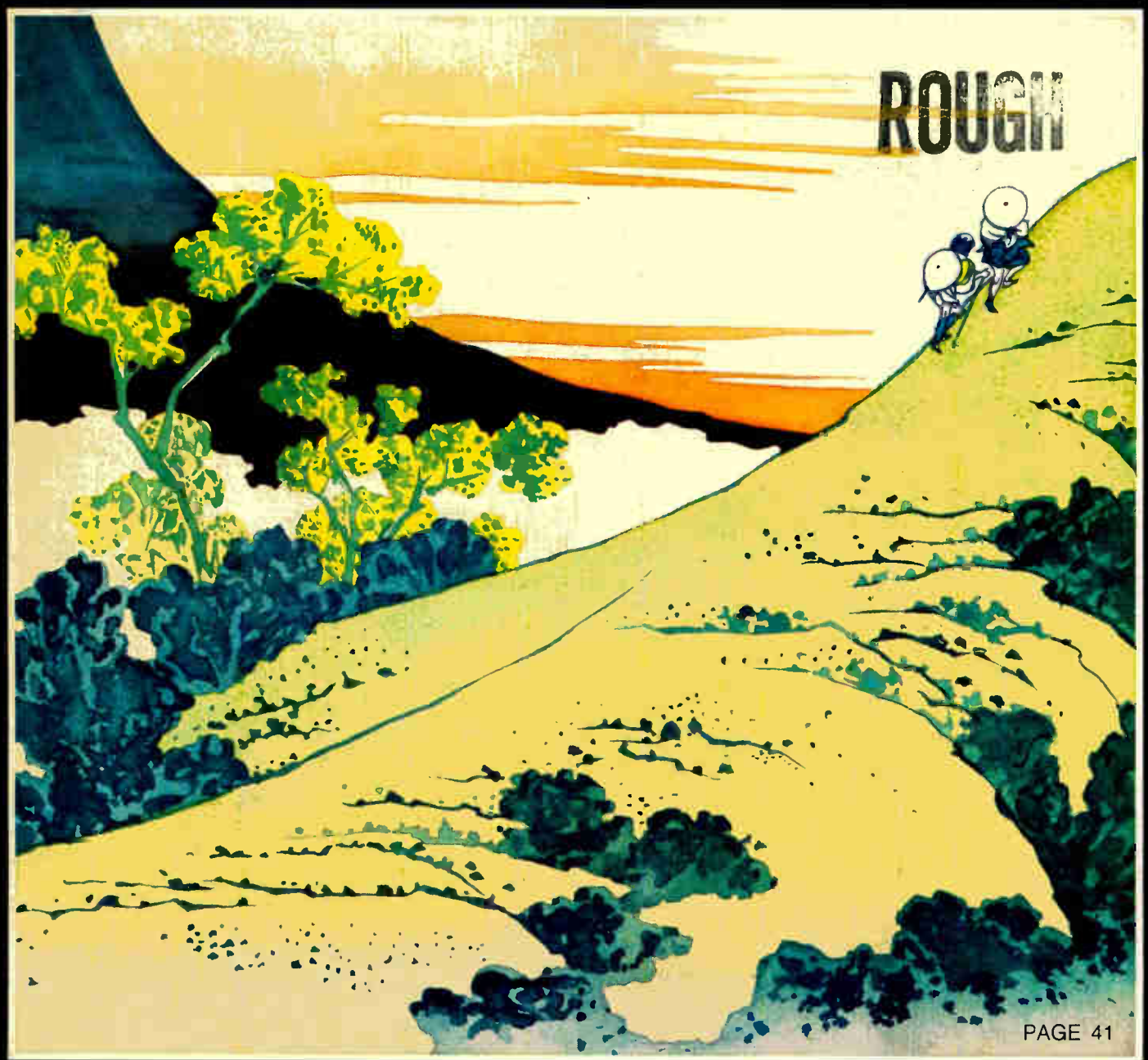
Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

MAY 12, 1986

CAN JAPAN CATCH UP IN 32-BIT PROCESSORS?



PAGE 41

The only thing small about it is its size!

The RTP-650A is the only portable data recorder that gives you bigger performance than a reel-to-reel.

- **DC to 40kHz frequency response on 14 (or 21) channels** — at a 76.2cm/sec (30 ips) on Beta format video cassette tape. Covers twice the IRIG WBG1 bandwidth on any of the other six tape speeds. WBG1 is selectable for an even better SN ratio.
- **Superior vibration resistance (tested in conformity with MIL-STD-810C)** plus a compact and lightweight design give you a wholly new latitude of applications.
- **FM, DR and PCM recording — three modes in all** A first for a desktop data recorder.
- **Optionally available GP-IB port** lets you easily configure a computer-controlled data acquisition and processing system.

And it's easier to use than any other data recorder.....

- **Bright easy-to-read menu style EL display** provides the window for easy access to the multi-microprocessor intelligence.
- **Programmable settings for simpler operation** Even an unskilled operator can use it on site.

Learn more about the RTP-650A and its many other exciting features. Write or call:

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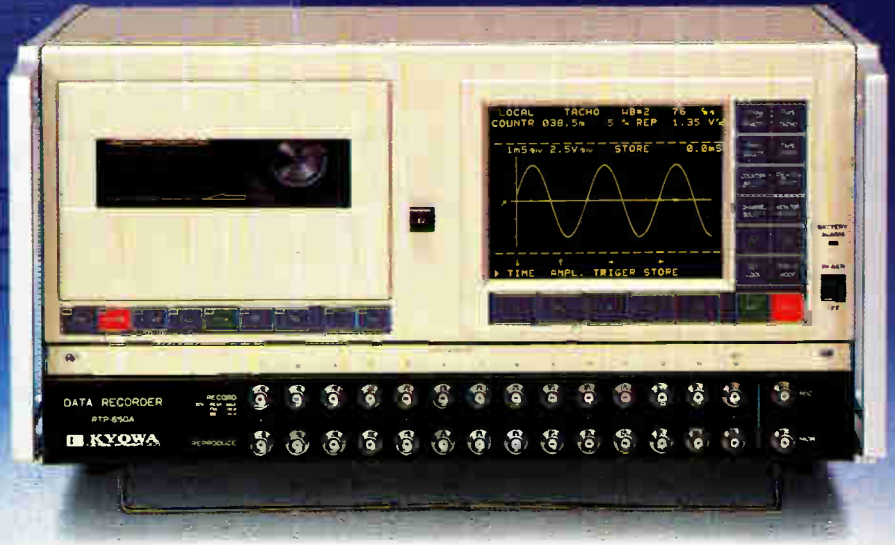
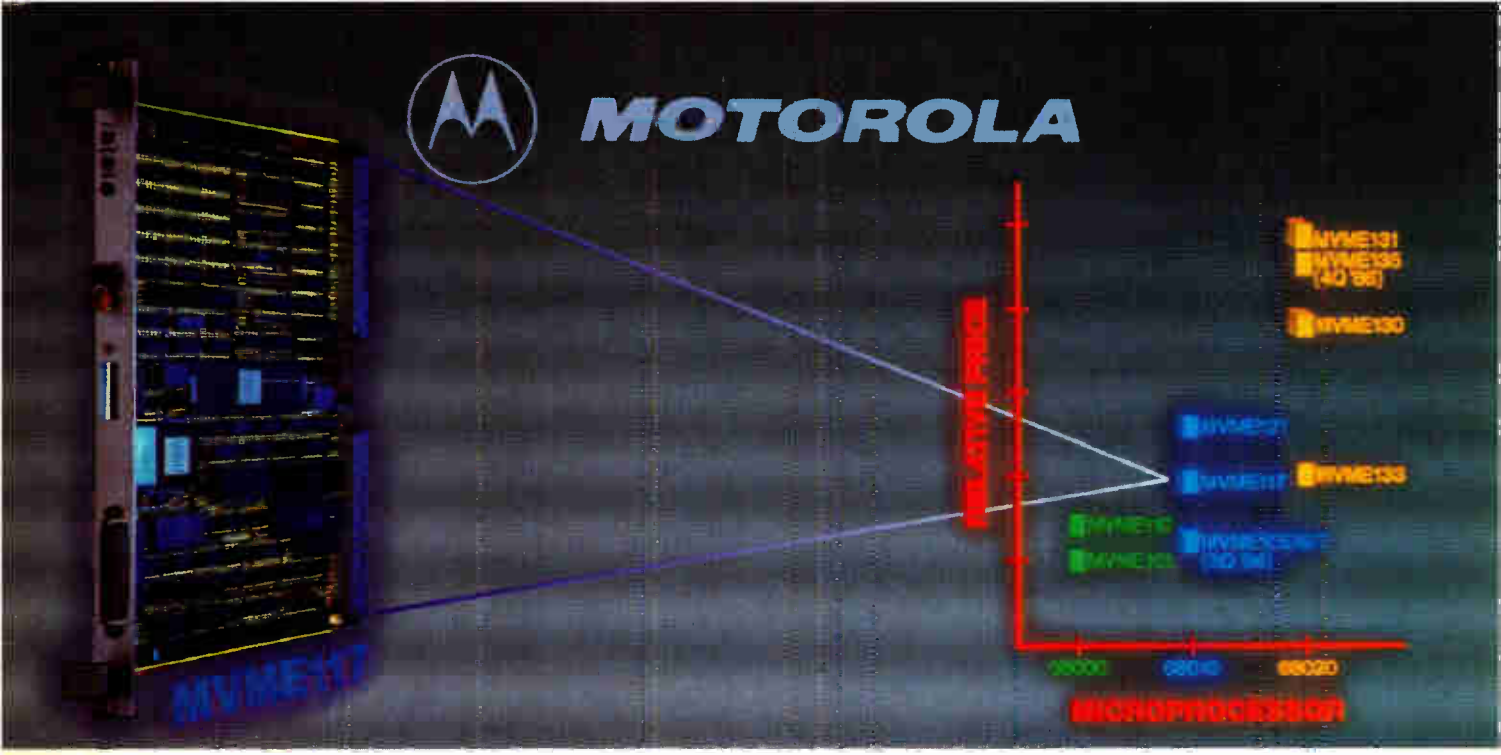


RTP-650A

VIDEO CASSETTE DATA RECORDER

Circle 900 on reader service card



More Choices in VME. For Less.

Select this full-featured 16/32-bit VMEbus SBC board for less than $1,400* in OEM quantities of 100 or more.

True design freedom comes down to choice. Yours. That's why Motorola offers more than 15 different VMEmodule™ processor boards based upon our proven M68000 Family of microprocessors. And that's also why we've established breakthrough OEM quantity pricing that lets you add outstanding price/performance to your list of VMEbus selection criteria.

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Far More Than Raw Hardware

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If the MVME117 is the logical choice for your cost-conscious design, we'd like to mention that the powerful VRTX,® PDOS,™ pSOS™ and Hemenway BASIC™ software packages are all available from their respective third-party sources. They're ported and ready to run.

One-on-one design-in help

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If a phone call can't answer your needs, one of our local VME specialists will contact you. We'll get you to market faster. And Motorola's heralded technical training is available for VME products if desired.

For VME processor-module data sheets, write Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036, or use the coupon below.

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Call Martin Nelson at (408) 943-9100 today.

SEIKO INSTRUMENTS

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MAY 12, 1986 VOLUME 59, NO. 19

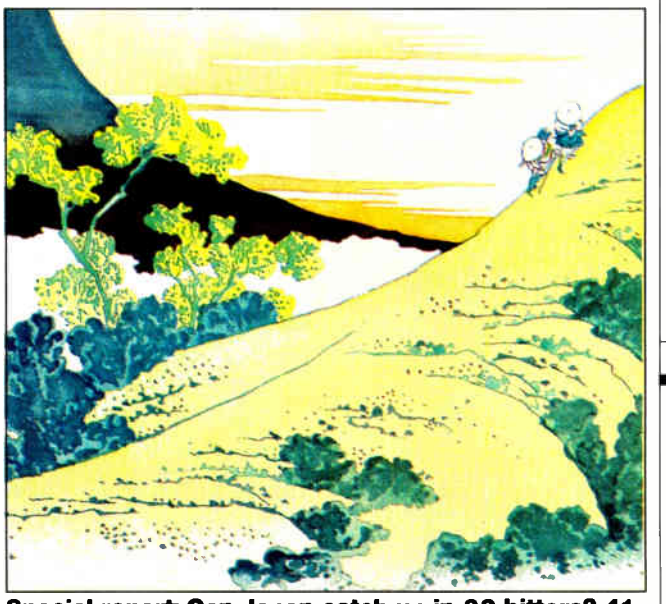
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER



Cover illustration by Cynthia Watts Clark, from Hokusai's "Inume Pass in the Province of Kai"

NEW PRODUCTS

DEPARTMENTS

UPGRADE CACHE, TAG, BUFFER MEMORY

NEC TIPS THE BALANCE IN YOUR FAVOR WITH THE 4-TO-1 DENSITY ADVANTAGE.

Put the scales in your favor. Design-in the μPD4362 fast static RAM. You'll reduce memory space, and upgrade your system at the same time.

4-to-1 Advantage

The 16K x 4 organization is ideal for upgrading your cache, tag, and buffer memories. You can virtually replace four devices with a single 4362. You also get CMOS performance, at NMOS prices with NEC's new MIX-MOS process.

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A Full Line-up

Choose from three speeds: 45, 55, or 70 ns. That's just the beginning. In fast static RAMs we offer a family of **four** devices and **five** access speeds, for a total of 15 variations of speed, power, and package.

Fast SRAM Selection Guide

Device	Access Time (ns)	Org.	Availability
μPD4362	45/55/70	16K x 4	Now
μPD4361	40/45/55/70	64K x 1	Now
μPD4314	35/45/55	4K x 4	Early '86
μPD4311	35/45/55	16K x 1	Now

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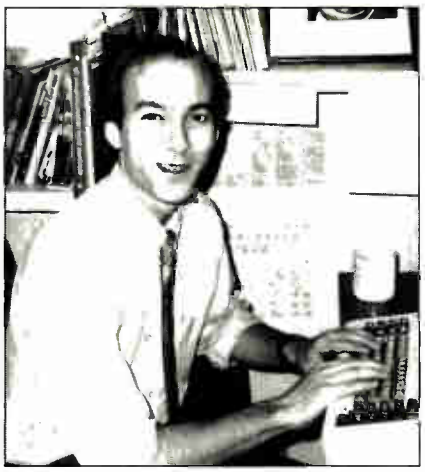

WOLFE: Covering technology in a hurry.

Writing a Technology to Watch requires a smooth blending of a number of talents and skills. The editor must be technologically literate, able to identify the latest developments, a discerning interviewer, and a skillful writer. On top of that, he or she must be able to turn the stories around fast, because at *Electronics* we strive to combine the speed and timeliness of a newspaper with the interpretation and attention to detail of a magazine—and that takes considerable planning and foresight.

That means that we are geared up to move fast. Take this week's Technology to Watch, "How Data General Improved Its Laptop Display," on p. 35. It is a detailed examination of the new technology in the new Data General/One Model 2 by software and microsystems editor Alexander Wolfe. "When we heard that the new machine was coming, we went to work fast. The result was that though it was announced only last Tuesday, we have an in-depth story just a couple of days later," says Alex.

The first Technology to Watch Alex wrote was only the second to appear in the magazine. "I was assigned to do the next one, for the July 8, 1985, issue. I had to travel from New York to California for one day so that I would be able to write about the software-development system from Rational [*Electronics*, July 8, 1985, p. 36]. Going to Boston for the Data General article was easier, but I don't get to watch a movie on the flight."

But there is a good side to any Boston trip, says Alex, a native of New York. "I lived there when I was in engineering—at GTE in Needham and at Signetron Inc. in Lexington—so in a sense it's like a trip home." And a trip anywhere gives him the opportunity to collect material for his leisure-time pursuit: writing humorous pieces. One has been published on the op-ed page of the *New York Times* and another has been printed in *Newsday*, a Long Island daily.

"I enjoy doing Technologies to Watch," says Alex. "It gives you a chance to examine a product or technology up close before anyone else. Also, as an ex-engineer, I like to get behind the technology and explain it. I also get a kick out of the way companies are pleasantly surprised when we discuss their products from an angle that even they hadn't thought of."

That's fortunate, because even as this page goes to press, Alex is on a plane to Boston to do another one in a hurry.

Laurence Altman

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Unlike other 8- and 16-bit processors being extended upward, the Series 32000 has no programmer-visible changes in architecture—throughout the entire family. So Siemens could develop any application the market demanded, now or in the future, without depreciating its existing software investment.

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These are supported by our family of CMOS Octals for bus interfacing, which are faster than advanced Schottky TTL!! And now, for the first time ever, you can get CMOS with this speed and bipolar driving capability to 64ma for buffers and transceivers.

Our Sunnyvale plant has the world's only Class Two facility for Six-inch wafers. It is 100% dedicated to the manufacture of our products using PACE TECHNOLOGY, and we have already shipped the first parts for revenue in 1985.

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The 4-bit μP slice cell is functionally identical to the bipolar 2901 4-bit slice, yet runs 25% faster. You can replace the bipolar part directly for instant improvement in system performance and power consumption.

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CMOS EPROMs.

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STEP UP TO E SIZE

Houston Instrument's new E size DMP-56 delivers the precision, throughput, and reliability you require from a drafting-intensive plotter. The DMP-56 also gives you the flexibility to handle 18 different drawing format sizes ranging from 8½ × 11 inches to 36 × 48 inches.

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In terms of throughput, performance, price, and quality the DMP-56 is the professional graphics tool you need. For more information, call 1-800-531-5205 (512-835-0900 if in Texas), or write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. In Europe, contact Houston Instrument, Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel.: 32-(0)59-277445. Tlx.: 846-81399.

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TECHNOLOGY NEWSLETTER

MOTOROLA WANTS FCC OKAY ON RADIO BAND FOR LAN USE

The latest twist in linking office computers isn't based on coaxial cable or optical fiber. Instead, a Motorola Inc. proposal now before the Federal Communications Commission is for a radio local-area network sharing the 10-MHz frequency band now used by weather satellites. Motorola officials are tight-lipped about the proposal, but the FCC has initiated a rule-making proceeding to consider technical standards necessary to control interference. Ronald Netro, deputy chief of the Private Radio Bureau Rules Branch, says the FCC proposes to license radio LANs that are at least 2,000 ft from others on the same frequency. In addition, operators of systems within 100 km of the 29 weather-satellite receiving stations in the country would have to submit detailed signal-level information. □

OSI SOFTWARE RUNS ON BOTH ETHERNET AND TOKEN-RING NETS

The first complete open-systems-interconnection software linking equipment on Ethernet and token-ring local-area networks will be demonstrated this week at the MAP/TOP users group meeting in Seattle. A new software house, Touch Communications Inc., Scotts Valley, Calif., developed the software for layers 3 through 7 of the International Organization for Standardization's OSI reference model and has provided what it calls a router that allows it to integrate the IEEE-802.3 (Ethernet) and 802.5 (token-ring) implementations of layers 1 and 2. The demonstration will link work stations from Sun Microsystems Inc. with several IBM Corp. Personal Computer ATs. Touch says it will be a first for OSI software running on a token-ring network. The demonstration will also mark the first use of token-ring architecture on the Manufacturing Automation Protocol and Technical Office Protocol networks, the factory- and office-automation networks backed by General Motors Corp. and Boeing Co., respectively. □

CIRCUIT MODELS SIMULATE IC FUNCTIONS AT BOARD AND SYSTEM LEVELS

Systems designers working with Advanced Micro Devices Inc.'s integrated circuits will soon be able to save much design time and money by simulating designs at the board and system levels. Logic Automation Inc., Beaverton, Ore., and AMD will collaborate on a library of SmartModel software for a number of the Sunnyvale, Calif., company's ICs. The software provides fully functional models of large- and very large-scale ICs and makes possible behavior-level logic simulation. It includes a design troubleshooting feature that checks for timing and other sources of errors, then generates error messages pinpointing cause, location, and time of an error if one occurs. Logic Automation has also offered SmartModel support for Intel Corp.'s 80386 32-bit microprocessor since late April. □

MANAGEMENT SOFTWARE KEEPS TABS ON LARGE CAE PROJECTS

Help is in sight for managers of complex computer-aided-engineering projects running on Digital Equipment Corp. VAX computers. Sherpa Corp. (formerly Cadtec Corp.), of San Jose, Calif., now offers a data-management system that sets up a series of attribute files to keep tabs on the origin, status, and history of each working data file. When a system user requests data, the Sherpa software verifies the authorization levels established by the project managers and checks project milestones before fulfilling the request. When design changes are made, they are rippled through all the working files. "There is no magic here, just five years of work in understanding what companies need in terms of automated project management," says D. Stuart Harrison, vice president of marketing. □

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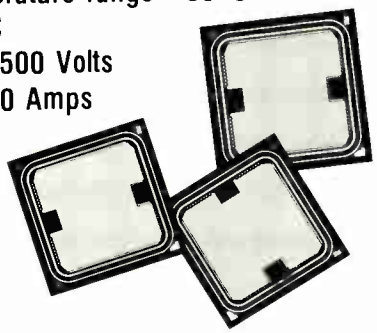

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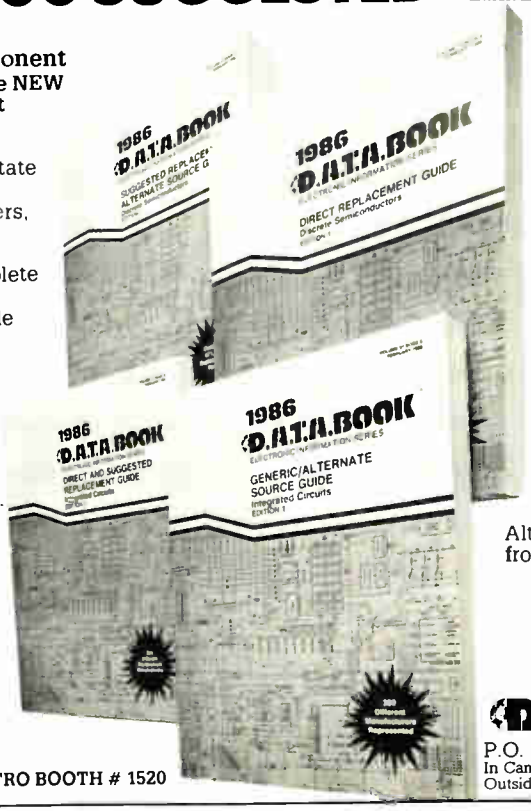

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ELECTRONICS NEWSLETTER

DUMPING PENALTIES NO CURE, SAYS OKI'S CROWLEY

Even if the tough dumping penalties levied by U. S. regulators against Japanese semiconductor companies actually survive the appeal process—as most now predict—they will provide only "temporary relief" to U. S. manufacturers, says Jerry R. Crowley, president and chief executive officer of Oki America Inc. At market consultant In-Stat Inc.'s Semiconductor Forum held last week in Phoenix, Ariz., Crowley said two likely actions will blunt the effect of the fines. Japanese companies will simply step up U. S. manufacturing to avoid import curbs, Crowley maintains, and systems customers in America increasingly will move purchasing and assembly offshore to buy more cheaply. Both events will further hurt the U. S.-Japan trade imbalance, in the opinion of the Sunnyvale, Calif., executive. □

DENATIONALIZATION PLAN ACCELERATES IN FRANCE

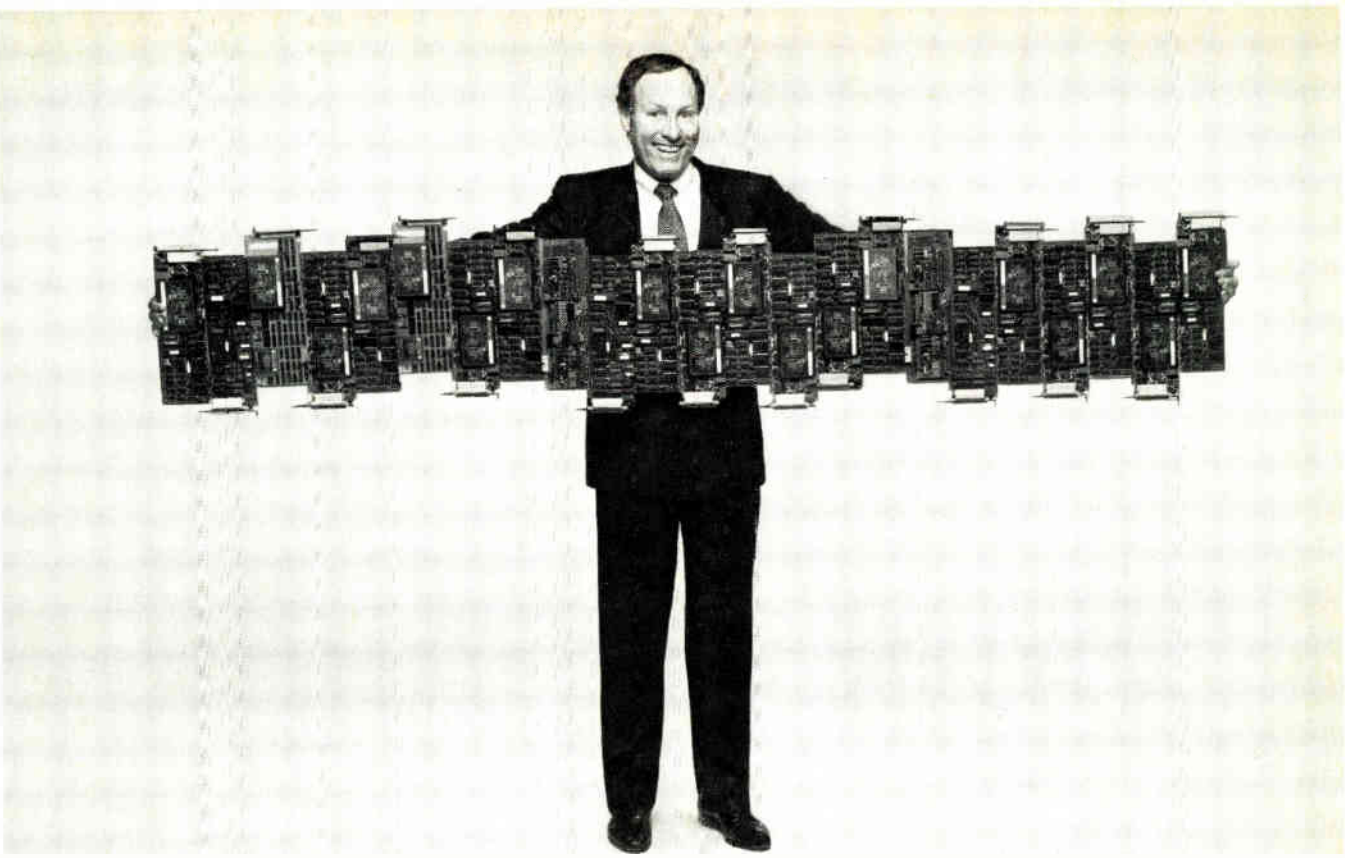
Encouraged by a spectacular rise in the domestic stock market, France's conservative government is gaining confidence that it can pull off its denationalization plan [*Electronics,* Feb. 24, 1986, p. 79] within the next two years. Most observers felt at first that the total amount of the planned privatizations, generally estimated at more than $20 billion, would swamp the French equity markets. But the Bourse, as the French stock market is called, has logged a rise of more than 50% since the beginning of the year and that has led some conservatives to believe they should try to accomplish as much of the program as possible before May 1988, when the country's next presidential elections are scheduled. A bill enabling the government to denationalize electronics companies Thomson SA, Group Bull, and Compagnie Générale d'Electricité as well as a group of other industrial companies, banks, and insurance companies is currently before the National Assembly. □

KOREAN CHIP MAKERS FORM DRAM R&D ALLIANCE

South Korean semiconductor makers, ever optimistic, are banding together to invest close to $80 million to develop 4-Mb dynamic random-access memories for mass production within three years. The chip makers plunged into the 256-K DRAM market last year only to lose tens of millions of dollars in a massive, worldwide semiconductor slump. The organization, called the Association of Major Korean Semiconductor Manufacturers, includes 13 chip makers and will receive government subsidies for research and development. At present only Samsung Electric Co. and Gold Star Semiconductor Co. claim to have developed 1-Mb prototypes, but neither has shipped products. □

DATAPOINT BUYOUT DROPPED, PROFIT SEEN

Datapoint Corp. is apparently on the road to recovery after a stormy two-year period. A leveraged buyout proposed last fall by chairman Asher Edelman and other board members of the troubled San Antonio, Texas, computer maker was dropped last week and the company now says it will hold the stockholders meeting that has been postponed since January [*Electronics*, March 3, 1986, p. 72]. Edelman changed his stance after it became likely that Datapoint would show a "modest profit" in the fiscal quarter ended April 30. "While the terms of the buyout were found to be fair at the time they were proposed, and although the investment bankers to the buyout group have advised me of their ability to raise the financing for the transaction, the recent improvements in Datapoint's results and prospects have caused me to conclude that the proposal should be terminated," Edelman says. If Datapoint reports a net income for the period in the next two weeks, it will be the first in a half dozen operating quarters. □



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General Purpose	DT2806	295	to 80	12	20	to 24	12	to 72	Yes	DT757
	DT2808	495	16	10	3 3	2	8	16	Yes	DT707
	DT2814	299	16	12	25	–	–	–	Yes	DT757
Low Cost	DT2815	399	–	–	–	8	12	–	–	DT757
	DT2817	199	–	–	–	–	–	32	–	DT758
High Speed	DT2821	1195-2495	4-16	12-16	50-130	2	12	16	Yes	DT707

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PRODUCTS NEWSLETTER

AT&T TO ANNOUNCE ENCRYPTION PROCESSOR

Look for AT&T Technology Systems to display a digital encryption processor at Electro Mini/Micro this week. The T7000A processor will protect sensitive data by means of multiple encryption, including custom programming. It executes all four Data Encryption Standard modes established by the National Bureau of Standards. Samples of the T7000A are available now for about $45 each in quantities of 1,000 from the Allentown, Pa., division of AT&T Co. □

KLA SOFTWARE WILL SAVE PHOTOMASKS FROM SCRAP HEAP

Severely damaged photomasks, including those with incomplete geometries and feature boundaries, can be fixed with Clone-it from KLA Instruments Corp. The Santa Clara, Calif., company says this is the first software to electronically create a repair template from defect-free geometries and patterns found elsewhere on the same mask. Clone-it uses an extremely precise ion beam to copy and repair areas up to 40 by 40 μm in size. Bundled with the KLA/Micrion 808 photomask-repair system [*Electronics*, Jan. 6, 1986, p. 65], Clone-it meets the 0.1-μm repair requirements of photomasks for very large-scale integration. Current owners of 808 systems will be offered Clone-it as a field upgrade. □

DATAPOINT OPENS ARC NETWORK TO OUTSIDE STANDARDS

Datapoint Corp. is stepping up efforts to tap its local-area network and computer equipment into a number of leading markets for communications protocols with the introduction of a 68000-based server called Stargate. The communications server is the home for a family of gateway software packages intended to allow users of Datapoint's Attached Resource Computer network to connect with other system protocols. The San Antonio, Texas, company is targeting protocols supported by IBM Corp. and specified by the International Organization for Standardization. Stargate, which provides high-speed synchronous data transmissions, will initially run SNA/SDLC gateway software. The hardware costs $3,500; the SNA/SDLC gateway software is priced at $2,750. □

SOPHIA'S UDS GOES WHERE THE MICROPROCESSORS ARE

A portable universal development system and in-circuit emulator with interchangeable pods for 8-bit microprocessors has been introduced by Sophia Systems of Santa Clara, Calif. The Sophia SA2000 includes two built-in 5¼-in. floppy disks and an EPROM programmer. Available now are pods for the Intel 80C85 and the Zilog Z80H and Z80C. The development system and programmer package, with software, is priced at $7,995; each pod, which supports one or two microprocessors, is priced at $3,245. Sophia is a subsidiary of Sophia Systems Ltd. of Japan. □

NEC WILL MARKET BICMOS GATE ARRAYS

NEC plans to begin marketing BiCMOS gate arrays next month. The Tokyo company says its mixed bipolar-CMOS chip, which has an internal-gate time delay of 0.8 ns, offers the high speed of emitter-coupled logic circuits. NEC is making four types of BiCMOS gate arrays. At the low end, the 624-gate PD67001 will sell for $4.24 in lots of 5,000; the high-end PD67030 has 3,140 gates and will sell for $21.21. The company will announce details of its BiCMOS technology at the Custom Integrated Circuits Conference in Rochester, N. Y., this week (see story, p. 48). □

Electronics

WHY GIANTS ARE GOING AFTER AN OBSCURE AVIONICS PRODUCT

DIGITAL RF MEMORIES FOR ECM COULD BECOME A BEST SELLER

LOS ANGELES

Ask most electronics engineers what a digital radio-frequency memory is, and you're likely to get a blank look. But engineers working in electronic warfare know that a DRFM is a critical subsystem in electronic countermeasures receivers that must be speedily improved for next-generation avionics gear.

Two defense heavyweights, GM-Hughes Electronics Corp. and Raytheon Co., now aim to cut in on the business of the principal DRFM supplier, Whittaker Corp.'s Tasker Systems Division. Major product development programs are under way at both companies to shrink the size of such systems, speed up their operation, and increase their resolution.

The DRFM plays a key role in ECM receivers by serving as a coherent medium for storing incoming signals from hostile radars, likely to be of the sophisticated pulsed-Doppler type. The DRFM must accurately convert these radar's distinctive analog waveforms to digital form for processing. Furthermore, the conversion must be so fast that the ECM system can return these signals either in their original shape to mask the identity of the plane or missile carrying the ECM gear, or transformed into false information.

The DRFM thus includes an analog-to-digital converter, a digital-to-analog converter, a multiplexer and demultiplexer forming interfaces between the converters and a bank of random-access memories, and control circuitry (diagram).

To achieve the necessary performance, present ECM systems can weigh hundreds of pounds and dissipate 2,000 W. Advanced DRFMs using new technologies offer the opportunity to shrink these down to compact packages suitable for airborne applications, both in existing craft and the next round of fighters.

Leading the charge to come up with what could become a best-selling avionics product, GM-Hughes's Radar Systems Group, El Segundo, Calif., has loosed a substantial DRFM research and development effort that's already paying dividends. The Electronic Warfare Programs office of the group's Advanced Program Division has snagged what many sources consider the most important DRFM development contract yet.

The Air Force's Avionics Laboratory at Wright-Patterson Air Force Base, Dayton, Ohio, has chosen Hughes to deliver by May 1988 a spectrally pure DRFM prototype that employs gallium arsenide converters and advanced silicon devices. The term stems from the required signal-to-noise ratio.

A DRFM digitizes hostile radar signals and then stores them

Developing the device "depends heavily on the high-speed sampling rates of both GaAs and silicon parts," says a lab spokesman. "Multiple-bit performance is equally important," adds Stanley R. Hall, Hughes's EW programs manager. Hughes already has demonstrated a DRFM with 6-bit, 750-MHz analog-to-digital conversion and expects by 1989 to have a 10-bit model that operates at 1.2 GHz by teaming four 300-MHz converters. For now, researchers are using a commercial RAM; they plan to upgrade to faster versions as they become available.

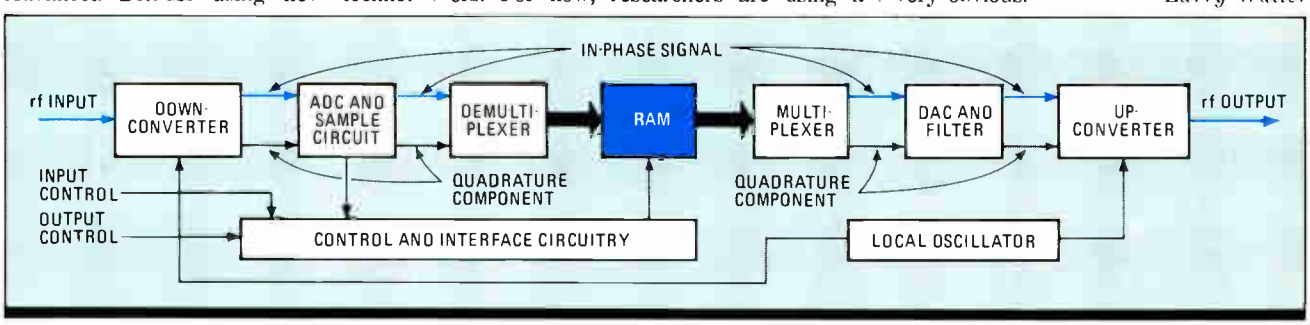
The product development efforts of both Hughes and Raytheon threaten the position of the company that pioneered DRFM technology and remains virtually the sole source of these parts today—Tasker Systems of Simi Valley, Calif.

"Suddenly, very competent companies are breathing down our neck," concedes John R. Marlowe, Tasker's product line marketing manager. Though Tasker as a policy does not discuss its R&D, Marlowe is emphatic that the company isn't standing still on advanced DRFMs. "You'd better believe it," he says.

Tasker's DRFM patents date back to the early 1970s, he says, and its MIPS products are the only DRFMs in volume production. Most advanced is its MIPS 130, which uses emitter-coupled logic and operates at a 500-MHz sampling rate. It is used in ECM equipment on the B-1B bomber, among other craft.

DRFMs pack a number of circuit boards in a microcomputer-size package and hit $45,000 each in quantity for the highest-performance products. These tabs undoubtedly would drop steeply for future hybrid packages.

But information on the progress of DRFM may soon dry up; a nervous Pentagon could remove them from public view. Officials of a Defense Department subcommittee that tracks DRFM development reportedly told industry and government representatives that the work might henceforth be classified. Says Marlowe, "It's highly sensitive, since it deals with threats. The applications have become very obvious." *–Larry Waller*



MEASURES. Hughes has a digital rf memory with 6-bit resolution and a 750-MHz sampling rate. It hopes to hit 10 bits and 1.2 GHz by 1989.

THE MOVE TO PC-BASED IMAGE STORAGE

BOSTON

A new breed of document-storage systems is emerging as vendors tie together write-once optical disk subsystems with personal computers. Such low-cost systems are most likely to find applications, their makers say, in organizations that have a lot of paper to file but not enough to justify the cost and inconvenience of a microfilm system.

Optical-disk-based systems have been available for some time, but they cost hundreds of thousands of dollars. The trend to less expensive systems will be evident this week in San Francisco at the Association of Information and Image Management's AIIM '86 Show.

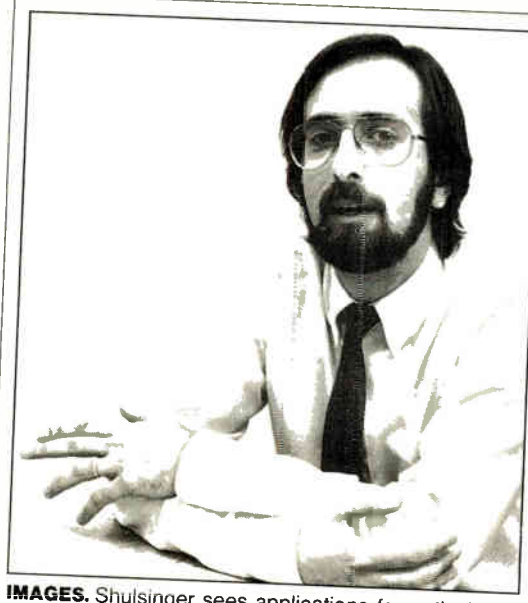
The new wave of products, which will account for nearly half of those on display this week in San Francisco, will be turnkey products priced at less than $50,000. These document-filing systems typically consist of a scanner for document entry, a personal computer, hardware for digital compression and decompression, high-resolution monitors, a laser printer, and write-once optical disks for storing pages.

MOVING FAST. The conference illustrates how fast this technology is moving. The number of turnkey document systems demonstrated at AIIM '86 will be twice the size of any previous show, says Ed Rothchild, publisher of *Optical Memory News*. The climate is also different at this year's show. "Systems were shown last year to get end-user input," he says. "This year it's to sell systems."

Industry observers don't think the bulk of early uses for the optical-disk systems will come from the replacement of microfilm systems, although their function is similar. "Only a portion of [the microfilm] market is susceptible to replacement," says Linda O'Keefe, director of office system industry services at Dataquest Inc., a San Jose, Calif., market researcher. Microfilm users will stay with that medium because of its perceived permanence, observers say.

"You will mostly see the image-management systems in new applications," O'Keefe predicts. But that presents another problem. "The difficulty with this market is that there must be a lot of user education," she says. "It's going to take a breakthrough application to ignite this technology."

But with the advent of low-cost optical storage systems, microfilm could lose out when new customers start looking for document storage. "The major application is with the 97% of the people who don't have microfilm but still have lots of paper," says Don Shulsinger, vice president of marketing at Laserdata Inc. The Lowell, Mass., company will introduce at the show its LaserView system. LaserView has several interesting features: It can handle halftones, a user can view documents while other pages are being printed, and its speed—decompression of a standard document takes less than one second.



IMAGES. Shulsinger sees applications for optical-disk document storage where microfilm has not penetrated.

New York-based AGA Inc., which markets a system based on IBM Corp.'s Personal Computer AT, considers its selling point to be commitment to what executive vice president Stanley Marder calls "pure MS-DOS compatibility." AGA has been marketing its 12-in. optical-disk document-storage system, dubbed Discus 1000, for six months.

The Image and Document Management System from Aquidneck Data Corp., Middletown, R. I., can be integrated with computer-aided-design software, allowing for the generation of documents electronically and their subsequent storage on optical disk. George Steele, program manager for digital optical systems, says the system is positioned so end users can give optical storage a relatively inexpensive trial run.

As the market for the new low-cost systems develops, hardware generally will become fairly standard, with key system features depending on their software, Rothchild believes. And because it is a low-end market, pricing will grow increasingly important as the market grows, he predicts.

Although the optical-disk document-storage market is still embryonic, forecasts of its growth are highly optimistic. Rothchild projects that 350,000 small-capacity optical-disk image-and-document-storage systems will be shipped in 1990, generating revenue in excess of $4 billion. A more conservative view comes from Dataquest, which pegs total 1990 revenue for image-management systems at $1.6 billion. *–Craig D. Rose*

DISPUTES MAY STALL HDTV STANDARD FOR TWO YEARS

WASHINGTON

As broadcasting groups from around the world gather in Dubrovnik, Yugoslavia, this week for the 26th plenary assembly of the International Consultative Committee on Radio (CCIR), it's becoming increasingly unclear whether a worldwide studio-production standard for high-definition TV will be adopted. The CCIR is scheduled to resume the ongoing debate over HDTV on Wednesday.

The U. S. and European broadcasting industries appear to be moving closer to agreeing on a studio-production standard proposed by the CCIR's HDTV study group—a standard that has largely Japanese origins. But there's still plenty of controversy over the signal format.

Unconfirmed reports last week had the 12 countries of the European Community signing a statement calling for a two-year postponement on the HDTV recommendations at the Dubrovnik meeting. An EC representative did say, however, that such a move is in keeping with current sentiment among member nations.

Meanwhile, the French and Dutch governments reportedly want to retain the European 50-Hz studio standard rather than the 60-Hz system recommended by the CCIR's study group. In addition, European TV-set manufacturers, fearing further Japanese inroads into the European consumer electronics market, are also known to oppose

HITACHI MAY MAKE IBM JUMP AGAIN

At least once before, experts say, Hitachi Ltd. helped to prod IBM Corp. into hurrying up introduction and delivery of its high-end 3090 mainframe line. And last week, the Japanese giant may have done it again.

Following Hitachi's announcement of its M-680 series last year [*Electronics Week*, March 18, 1985, p. 16], IBM moved to deliver its 3090/200 and 3090/400 systems earlier than originally scheduled. Now the Tokyo company is promising machines with nearly twice the processing performance of IBM's top-of-the-line model 400 by the third quarter of 1987.

The announcement "may again force IBM to accelerate the introduction and shipment of products in its 3090 series," says Bob Djurdjevic, computer industry analyst and president of Annex Research, Phoenix, Ariz.

Delivery schedules were announced last week in Tokyo and in the U.S. by National Advanced Systems, the mainframe importer owned by National Semiconductor Corp. Hitachi's machines are based on the central processing unit used in the two-CPU M-682H, which is being delivered this month and offers performance roughly equal to the four-CPU IBM 3090/400. But the new Hitachi high-end systems will have either three or four CPUs.

The third new entry is a new low end for the series at about 60% to 80% the performance of the single-CPU M-680H (known as the AS/XL 60 in the U.S. and about equal in power to an IBM 3090/200). *–Jeremy Young*

the CCIR recommendation.

The proposed recommendation that the study group adopted last October would set the standard at 1,125 scanning lines per frame interlaced as well as at a 60-Hz field rate. It is based primarily on the Japan Broadcasting Co. system, which uses bandwidth-compression techniques that allow picture elements to be transmitted in four packets, stored in memory, and reassembled to produce an image. Predictably, Hitachi, Mitsubishi Electric, Sanyo Electric, Sony, and Toshiba are all behind the proposed system. All of them displayed HDTV systems at the Japanese Electronics Show last fall.

The U.S. government, representing five industry groups including the Advanced Television System Committee, endorsed the study group's proposed recommendation in January. "We think it's timely and appropriate," says Richard E. Shrum, director of the State Department's Office of International Radio Communications and head of the U.S. delegation to the conference. Because the U.S. produces a vast amount of program material, Shrum estimates that an HDTV studio standard could reduce costs 70% by ensuring equipment compatibility.

EUROPE, TOO. Similar support has been voiced by the European Broadcasting Union, which agreed on May 1 to seek "the establishment of a single worldwide production standard and supports the [CCIR] parameters . . . as a possible way of achieving this aim." The union did, however, temper its endorsement of the HDTV parameters by identifying two remaining areas of concern.

The first is that choosing a studio-production standard before the CCIR selects a transmission medium could make the broadcasting union's goal of a homogeneous European transmission standard difficult. George T. Waters, director of the union's technical center in Brussels, says a worldwide transmission standard is possible, but he stops short of calling it probable.

The other issue raised by the broadcasting union relates to the production standard itself. An interlace standard would be required to achieve the 1,000 active lines generally seen as the minimum for HDTV. Waters says that could cause future problems with editing and special effects. The union will back the interlace standard but will seek to update it later to a serial standard.

The U.S. industry agrees that these issues still need to be resolved, says the State Department's Shrum. "Our people have the same kinds of concerns and questions." An interlace standard may eventually create the need for subordinate standards or techniques to produce computer-generated images, he says. "That particular point is really what our own U.S. broadcasters are saying," Shrum notes.

Although he concedes there are also many transmission questions to be resolved, Shrum argues that "nobody seems at all concerned about the fact that the production standard for today is not that closely related to the transmission standard. To a very large extent, HDTV is an alternative to film. Who knows whether it will ever be broadcast?"

What happens if the HDTV standard is again stalled at the Dubrovnik meeting? "I don't think the world will end," Shrum responds. If a two-year postponement is adopted, he says, multiple transmission standards are possible. Meanwhile, Japan Broadcasting plans to start broadcasting HDTV signals by satellite in 1989, but probably on just one channel. *–George Leopold and Robert Gallagher*

SEMICUSTOM ICs

USING LASERS TO CUT CHIP TURNAROUND TO HOURS

LIVINGSTON, N. J.

Systems designers typically have to wait 6 to 12 weeks for semicustom integrated circuits. But Bell Communications Research has come up with a new process that, once perfected, could cut turnaround time to a matter of hours.

Laser etching and deposition techniques enabled researchers at Bellcore, the Livingston-based research arm of the seven Bell operating companies, to develop a CMOS random-logic array that offers the flexibility they need for high-speed production of limited chip quantities. The array features rows of isolated transistors with local interconnections that act like small country roads, alternating with high-speed routing channels for global interconnections, which mirror interstate highways. The etching process is further along and better understood than deposition methods, according to Joshua Alspector, principal investigator for the project in Bellcore's VLSI Design Methodology Group.

Using maskless fuse-link and antifuse-link techniques—in which lines linking transistors can be either opened or closed with a pulsed laser beam—the researchers need only alter the chip's top metal layer to achieve a fully customized silicon chip. Because such routing schemes can sometimes cause contention between transistors, researchers implemented an interdigitated channel to ease vertical contention and guarantee routing at maximum density.

The motivation behind development of the technique was quicker turnaround on research prototypes, explains Alspector. With productivity hampered by slow turnaround on custom ICs, Bellcore looked for a faster alternative, one that Alspector calls "the ultimate goal—to be able to create a few prototype chips in a matter of hours."

Alspector realized it was necessary to keep the customizing work to a minimum, to get a nearly complete chip out of the foundry, and to modify the chip

with minimum effort. For the best possible performance, predefined standard metal is used for long-distance interconnections, Alspector says; laser-deposited metal—which tends to have higher resistance—is used only for short links. "The fundamental point in the project is to have the foundry do as much as possible," says Charles Lee, manager of the VLSI Design Methodology Group.

That's why available semicustom techniques were deemed inadequate for the project's purposes, Alspector says. Programmable logic arrays, for example, were considered "a very inefficient way to do things," because the format requires too much silicon to accommodate its truth-table architecture; devices such as adders of more than 4 bits require huge amounts of real estate, he says. Gate arrays, on the other hand, were deemed too difficult and time-consuming to make, because they require the design and construction of up to five masks for each chip design. Moreover, says Lee, both PLAs and gate arrays limit the user to static-CMOS technologies, and Bellcore is interested in the speed advantages of dynamic-CMOS structures such as Zipper CMOS [*Electronics*, April 28, 1986, p. 20].

Instead, the Bellcore researchers decided to try a technique in which only one layer of metal needs to be fussed with. A laser expert, Robert Contolini of the Photonic Device Research Group, was brought in to help devise a method in which metal could either be deposited on the chip to link transistors or etched to break a link between transistors. "Using fuse-link technology for programmable logic arrays has been done before," Alspector says, but this is the first use of the technology for random-logic arrays.

Bellcore process needs only to alter top layer to complete custom IC

Etching was relatively easy, Contolini says. Ignoring conventional wisdom by choosing not to use a continuous-wave laser to etch aluminum, Contolini opted instead to use a pulsed laser-enhanced chemical etching technique. "What that allows you to do is vaporize a small area to cut a link without damaging the rest of the circuit," he explains. To etch away the links, the chip is immersed in a chemical bath and the laser is focused on the given spot. Once exposed to the laser, the spot heats up, activating the chemistry to burn away the link.

"Etching will work," says Alspector, but points out that it "hasn't been tried on a large scale," and there is "a lot of development to do."

Using the laser for deposition is an even trickier game. We're trying to do with the laser what the foundry does lithographically," Contolini says of the process he calls "laser writing." "We're trying to do what the foundry does with photoresist, without it."

The process, devised by Alspector, Harold Craighead, Lawrence Schiavone, and Donald Eilenberger, uses a modified commercially available gold ink. A laser is shined on the ink, and then post processing "not dissimilar to photoresist" takes place. Alspector says the goal is to achieve the ease of use of the photoresist process, but there are still some problems with deposition, including reliability of the contact made. But he claims that this combination of processes will provide faster turnaround and higher-quality circuits. *–Tobias Naegele*

MICROPROCESSORS

NEC'S CHANGING 32-BIT STRATEGY

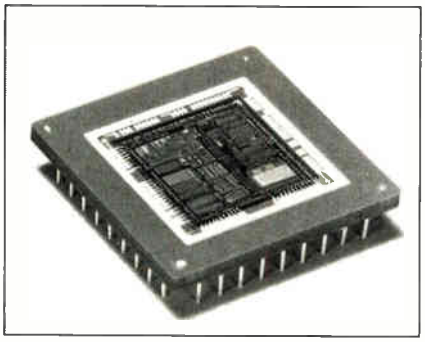
TOKYO

The latest microprocessor in NEC Corp.'s V series CMOS family signals a bold departure in the Tokyo company's game plan. Unlike earlier family members, the V60, a 16-/32-bit microprocessor, is not operationally compatible with Intel Corp. microprocessors.

Some industry observers believe that the turnaround in chip architecture may reflect the legal battle between the two companies that threatens to cloud the future of the entire V series. NEC denies the new chip design is due to the lawsuit, saying that development of the V60 started four years ago.

If NEC wins its fight with Intel, it is likely to become the one Japanese chip maker to win a significant share of the worldwide 32-bit processor market (see p. 41). NEC is betting on AT&T Bell Laboratories' Unix as the operating system of the future for microprocessors and is steering the V series in that direction, says Kenji Kani, manager of the System Design Deptartment of NEC's Microcomputer Products Division. NEC will begin offering the V60 in sample quantities at about $550 this month and will start volume shipments in August.

To design a high-performance processor, the company had to work out a tradeoff, says Kani. NEC engineers saw two possible directions: continuing to parallel the Intel 8086 line and increase instruction-decode speed or moving toward the Motorola 68000 family and high-level-language support.



INSIDE STORY. The V60, which runs at 3.5 mips, has a 32-bit floating point calculating function written into the microcode.

NEC chose the latter, but denies trading an Intel for a Motorola model. "We aren't making a Motorola-style chip. We're making a NEC-style chip," Kani says. Company executives hope to have a 10-million-instructions/s 32-bit Unix-based microprocessor out by 1990.

LEGAL BATTLE. Mips rates may be less important to the future of the V series than is the court battle between NEC and Intel, now under way in California. The V series has been enmeshed in legal skirmishes ever since the introduction of the first family members, the 16-bit V20 and V30, in late 1984. Intel is charging that the microcode used on those processors violates its copyright on the 8086 and 8088 microcode [*ElectronicsWeek*, March 4, 1985, p. 14]. A trial may begin this week in U. S. District Court, San Jose, Calif., but the case will probably take two years to wind its way through the courts. An Intel spokesman claims the trial itself should take just four to six weeks.

Whatever the merits of the case, it has clearly dampened V series sales. In 1984, NEC held about 6% of the world market in 16-bit chips, says Kani, and the share didn't grow at all in 1985 "because of the court case." He refused to comment further.

The suit also casts a pall over the future of the entire V series, say market watchers. "NEC can't get anyone to design-in the V series," maintains Carole A. Ryavec, a Merrill Lynch Securities Co. analyst in Tokyo. And equipment manufacturers that don't design-in the low end of the series are apt to stay away from the high end, says Manny Fernandez, president of San Jose market researcher Dataquest Inc. and former head of Zilog Corp., Campbell, Calif.

Undaunted by such predictions, NEC is forging ahead with its plans for the V

series. As a team of 30 engineers works full time to port Unix to the chip, the company sees a panorama of existing Unix-based applications opening up. Chief among them are office systems, work stations, high-end personal computers, and control applications.

The V60 runs at 3.5 mips with a 16-MHz clock. Kani claims that overall throughput "is 10 times better than the [Motorola] 68020 or the [Intel] 80386." Unlike these microprocessors, the V60 has a 32-bit floating-point calculating function written into the microcode. It needs only a third as many commands to implement high-level languages like C while doubling the symmetry of its data-type and addressing-mode functions, he claims. When three or more V60s are linked, they have automatic redundancy capabilities, essential for switching systems like private branch exchanges.

The next chip in the V series will be a full 32-bitter

NEC still is out on a limb because the new chip had to be designed with an emulation mode to make it downwardly compatible with its V series brethren. And Intel has every intention of pushing NEC even farther. The Intel strategy is to "take a very aggressive position in protecting our intellectual property rights," says Eugene J. Flath, executive vice president of Intel Japan K.K., Tsukuba. "We intend to continue that."

Though the storm continues to swirl around the V series, NEC executives are digging in for the long haul. The V60 will probably be limited to the Japanese market for now, and NEC hopes to sell about 10,000 units a month by the end of the year. Kani predicts sales rising to 30,000 units in 1987, and sometime next year NEC will come out with the V70, which is fully 32-bit, with a 32-bit external bus.—*Jonathan Joseph*

IC PRODUCTION

ION-BEAM LITHOGRAPHY: A WAY TO PRODUCE ULSI?

VIENNA

An ion-beam machine now in development at a small, 15-month-old Austrian company may make it possible to mass produce ultradense integrated circuits with sub-0.2-μm structures—the ultralarge-scale ICs of the next decade.

The ion-projection lithography machine from IMS-Micro-Fabrication Systems GmbH is based on the same principles as an optical wafer stepper, but it uses ions instead of light to image patterns of an open-stencil mask onto a wafer, and does so at a 1:10 or 1:5 reduction.

Experimentally, the machine has produced lines with an even finer resolution than what's planned for production: below 0.1 μm, in a self-developing organic resist on a silicon wafer. Given a line periodicity (or center-to-center distance) of 0.25 μm, the wafer thus crams about 4,000 lines into the space of 1 mm.

At the May 19-22 Semicon/West exhibition in San Mateo, Calif., IMS will show off what it has accomplished with the machine, dubbed the IPLM-01, and will present details on how it works at the concurrent technical sessions. Its design is based largely on the ideas of Gerhard Stengl, the company's president.

Qualifying the machine as a candidate for future high-volume production of sub-0.2-μm circuits are two factors, says Hans Löschner, executive vice president of IMS. One is its use of step-and-repeat exposure. In contrast to focused, or scanning, ion- or electron-beam systems, the source of illumination of a projection machine exposes the circuit patterns in one flash.

The exposure time checks in at about one tenth of a second, which is as fast as that obtained with optical wafer steppers. That makes ion-projection lithography four to six orders of magnitude faster than, say, focused ion-beam techniques, Löschner points out.

NO MOVING PARTS. In addition, electronic fine-alignment of the mask to the chip eliminates moving parts that could slow down production. Electronic devices produce electric fields that deflect the ion image in the X and Y directions, while magnetic fields rotate the image. An unusual feature of the system is that intrafield distortion may also be corrected electronically.

These factors, Löschner says, should result in a wafer throughput for a perfected ion-projection machine "as high as that achieved with optical wafer steppers." Today, the latter get up to sixty 4-in. wafers/h, depending on circuit complexity, alignment schemes, and other variables.

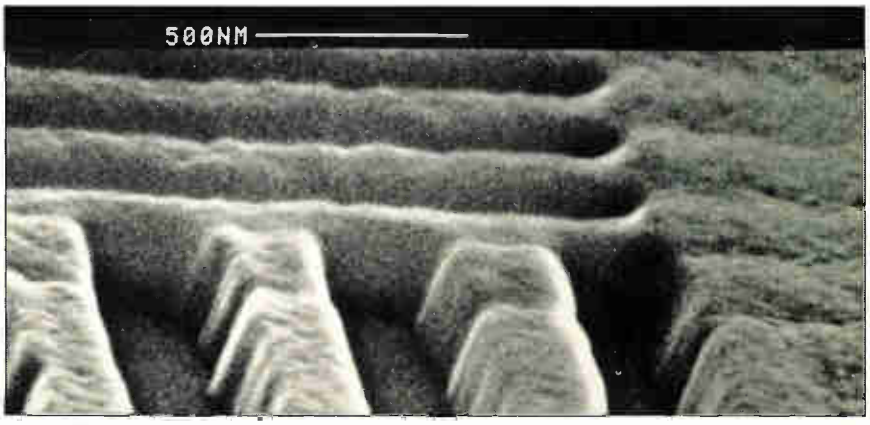
IMS is at work developing its wafer-alignment system. It expects soon to be able to demonstrate 0.02-μm alignment accuracy with the system, which it says will do its job in 0.1 second for volume production. Crucial to obtaining sub-0.2-μm features is the ion source. Its configuration allows a laminar flow of ions—at more than 200 μA—to be extracted within an angle of 4°. Thus the ions seem to come from a virtual point source: its diameter is just 10 μm.

Also contributing to small feature size is a sophisticated ion-optical lens system using electrostatic lenses that project mask patterns onto to wafer after a 1:10 or 1:5 reduction of the image.

IMS has other goals besides obtaining sub-0.2-μm lines in volume device fabrication. It plans to combine ion lithography with ion-implantation applications to cut costs. Further, the high power density—up to 50 W/cm^2 at the wafer—that is possible with ion lithography extends the technique to projection processes involving resistless wafers.

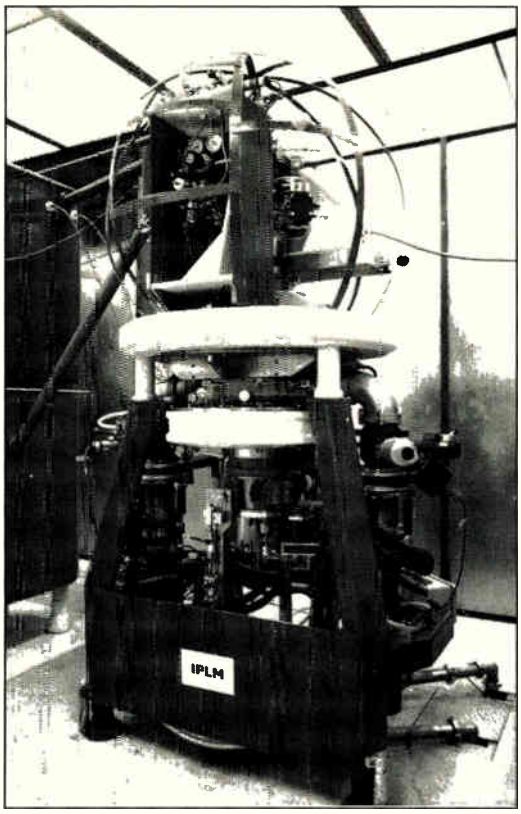
Also, ions can be used to alter the electrical properties of certain semiconductor materials such as gallium arsenide. What's more, using oxygen or nitrogen ions, chemical reactions in silicon wafers can be triggered to produce silicon dioxide or silicon nitride.

Löschner doesn't think ion projection will completely replace optical methods: "For production-standard devices with features of around 1 μm, optical lithography cannot be undercut in price." However, he believes they will start becoming standard pilot production tools by 1988, being used for fabricating, say, surface-acoustic-wave devices, GaAs parts, integrated-optic components, and a host of other devices. In the early 1990s,



PATTERN. IPLM obtains 0.2-μm pattern in silicon dioxide atop silicon by exposing and etching.

IONIZED. IMS's ion-beam machine is based on the same principles as an optical wafer stepper but images patterns with ions instead of light.



he says, ion-optical wafer steppers will be applied in volume production. By 1995, they will account for between 10% and 20% of all lithography systems made.

IMS claims to be the world's only company so far actively engaged in ion-projection lithography. Companies in the U. S. and Japan, to be sure, have built single-focused as well as masked ion-beam systems, but these are limited in their applications. Löschner says ion-projection techniques have been given little or no attention until now because production equipment manufacturers have poured most of their research money into electron-beam or X-ray methods as well as into stretching the limits of optical methods.

If IMS is convinced that there is a future in ion projection, so, apparently, are some capital venture companies and government authorities. Since its founding in February of last year, IMS has been allocated more than $2 million to carry through its project. Among the money givers are Munich-based Techno Venture Management GmbH and Vienna's Horizonte Venture Management GmbH. Together with another venture capital company, Vienna-based Friesca GmbH, they have contributed $1.5 million so far. Another $600,000 is coming from the Austrian government. *–John Gosch*

MATERIALS

FRENCH TAKE BIG STEP FORWARD IN OPTICS

BAGNEUX, FRANCE

A team of French engineers has taken a big step toward providing the tools necessary to build the all-optical systems that could be the building blocks of tomorrow's data-processing and telecommunications systems.

A new nonlinear organic material and an optical source made with it that are completely tunable in the wavelength range most common for telecommunications have been developed at the laboratories of the Centre National d'Etudes des Télécommunications (CNET) in Bagneux. The CNET has already used the optical source in a new time-resolved spectroscopy scheme boasting resolution better than 1 ps.

The CNET's patented material is called NPP, short for N-(4-nitrophenyl)-(L)-prolinol. NPP is an organic molecular crystal transparent between wavelengths of 0.5 and 2.0 μm, a range covering all three windows used for telecommunications applications as well as those targeted for potential consumer systems such as video disks. Using NPP, CNET has realized a coherent parametric source continuously tunable (by varying the angle at which stimulating laser light hits the NPP) between 0.75 and 1.6 μm.

The fact that nonlinear organic materials will be one of the most promising avenues for the future of integrated optoelectronics has been recognized for some time. They are seen as a means of eliminating the conversion between optical and electrical signals, which is unavoidable in all present optical systems.

KEY APPLICATIONS. They are particularly tantalizing for use in three kinds of devices. One is in systems based on the linear electro-optical (Pockels) effect. Examples are in beam steering, deflecting directional couplers, gates and switches for integrated optics, and amplitude and phase modulators for optical communications systems. A second type of device is based on second-order frequency-mixing effects such as emission, regeneration, and detection of information-carrying optical signals. The third is third-order-effect devices such as bistable optical elements and switches, which are essential to the implementation of optical logic operations and optical signal-processing or computing systems.

Nearly all nonlinear optical and electro-optical devices are now produced using inorganic materials. The most common examples are lithium compounds such as lithium niobate and III/V semiconductor materials. But Joseph Zyss, who is coordinating the CNET's effort in this area, reckons that organic materials could offer a number of substantial benefits over their inorganic counterparts.

One of the most fundamental advantages is that they are likely to open broad horizons for optical signal processing because they can be tuned by organic synthesis—during the manufacturing process—to vary optical properties over a wide range. And because at optical frequencies the nonlinear optical effects of organic materials are electrical in origin, their nonlinearities are more pronounced. Confirmation of this can be seen in the fact that the nonlinearity of benzene derivatives, the group of organic materials on which a number of laboratories are working, is six times that of LiNb. That difference translates into a nonlinear efficiency a full two orders of magnitude greater than that of LiNb.

Organic materials also boast a high optical-damage threshold. The optical-damage threshold for benzene compounds works out to about 2 GW/cm^2 at a wavelength of 1.06 μm and 50 MW/cm^2 at 0.53 μm. At 0.53 μm, LiNb can tolerate only 15 MW/cm^2. This parameter will be critical in withstanding high power densities caused by beam confinement in thin-film waveguides.

Yet another advantage of organic materials is their extremely fast response time—about 200 fs for NPP. The CNET's first application for NPP takes advantage of that. Tagged ETAP, a French acronym for parametric amplification and time sampling, the scheme makes use of a collision pulse laser emitting high-power pulses 100 fs long at a wavelength of 0.62 μm. Above a threshold of 3 GW/cm^2, these pulses provoke parametric emission at 1.24 μm in a cleaved crystal of NPP. At this wavelength, the nonsaturated gain is between 10^4 and 10^5 for a pump power of 1 GW/cm^2.

The CNET has capitalized on this effect to put together a time-resolved spectroscopy scheme with the aid of the Applied Optics Laboratory at the Ecole Nationale Supérieure de Techniques Avancées, Palaiseau, France. A pumped laser's pulses are divided with a beam splitter; half of the beam is used to excite a sample of a material to be ana-

lyzed while the other half follows a path that is longer by a distance corresponding to a delay of 100 fs. The two beams are brought together to excite a crystal of NPP. Detection of the filtered output of the crystal permits spectral analysis of the infrared luminescence of the sample in question with a resolution significantly better than 1 ps.

This system, Zyss points out, opens the way to fundamental physical research previously inaccessible. The CNET itself has begun by studying the infrared continuum emitted by water, organic dyes, and quantum wells in III/V materials. *–Robert T. Gallagher*

PERSONAL COMPUTERS

APPLE FINALLY GIVES UP; ADDS MS-DOS TO MAC

CUPERTINO, CALIF.

That old devil, standardization, has finally caught up with the only major alternative remaining to IBM Corp.'s Personal Computer. Apple Computer Inc. decided to join the pack and offer the MS-DOS operating system used by the IBM PC. It will be offered as an add-on board to the Macintosh. Not only that, the No. 2 microcomputer maker will add AT&T Co.'s Unix operating system in a renewed bid to penetrate the business and technical markets.

The announcement, made by Apple chairman and chief executive officer John Sculley at a closed meeting of financial analysts at the company's Cupertino headquarters, represents a radical departure for the company. Until now, Sculley's references to "open architecture for the Macintosh" have referred only to allowing development of hardware and firmware products. In software, Apple has encouraged third parties to develop business software for the 68000-based machine's closed box and proprietary operating system.

But now Apple has promised to offer as options for a new open-architecture Macintosh two operating systems that are perceived as industry standards in their respective worlds of office automation and high-end scientific and technical computing, according to Apple.

FOLLOWING THE STANDARD. Officials at Compaq Computer Corp., the successful Houston manufacturer of IBM PC compatibles, refused to say whether they perceived Apple as a threat to the company's strong position in the market. "No products are out yet, and we won't comment on a speculative product from a company," says company representative Bob Beach. "If any company such as Apple would provide an MS-DOS product, however, we would feel they're [just] recognizing the industry standard."

Development of Unix for the Macintosh is taking place inside Apple, the company says. It is using proprietary software bought from Unix hardware manufacturer Cadmus Computer Systems Inc., Lowell, Mass.

Apple is not giving specifics on development of the MS-DOS implementation for the Mac. And Apple denies that Sculley in the closed meeting promised the products in 12 months.

On the other hand, Michael Murphy, publisher of the *California Technology Stock Letter* in San Francisco, who was at the meeting, says that "Sculley specifically said they are going to announce, during the next 12 months, more products than Apple has announced in its entire corporate history to date." After the announcement, Sculley was asked how the MS-DOS system would be implemented. "All he would say is that MS-DOS would be an add-on board, not a clone," says Murphy.

Apple reportedly has already signed a third-party developer to handle the tricky MS-DOS implementation. The company won't say who, but speculators think the project has gone either to AST Research Inc. of Irvine, Calif., which builds Apple enhancement products such as hard disks and tape backups for the Macintosh, or Dayna Communications Inc., Salt Lake City, which pioneered MS-DOS compatibility for the Macintosh with its product, MacCharlie.

An official of AST Research, who would not comment on the contract rumors, questioned the timing of Apple's move. "I don't see anyone wanting to use MS-DOS on an Apple computer. I think the need for MS-DOS compatibility is long gone," says Ash Jain, director of the compsny's Apple Enhancement Products Group. "People wanted it two years ago when Apple first introduced the computer. But today the Macintosh is perceived on its own merits."

Of more importance to users will be the level of compatibility, Jain says. "Will you be able to exchange data, or will it be just operating-system compatibility?" he asks. "Data exchange is most important. The ability to take a Lotus 1-2-3 file from an IBM PC and load it into a Macintosh would be useful to people who want to use both computers."

The large quantities of high-end design software, which could conceivably run on the Macintosh in its Unix implementation, haven't yet caused much worry for Challenger Software Corp. The Homewood, Ill., company sells a three-dimensional graphics package for the Macintosh, called Mac3D.

"We're concerned, but we're not afraid of any communication compatibility between Unix, a VAX, and a Macintosh," says Andrew Sirota, Challenger's director of marketing. "We're interested in the possibilities that the open channel can create." *–Denise Caruso*

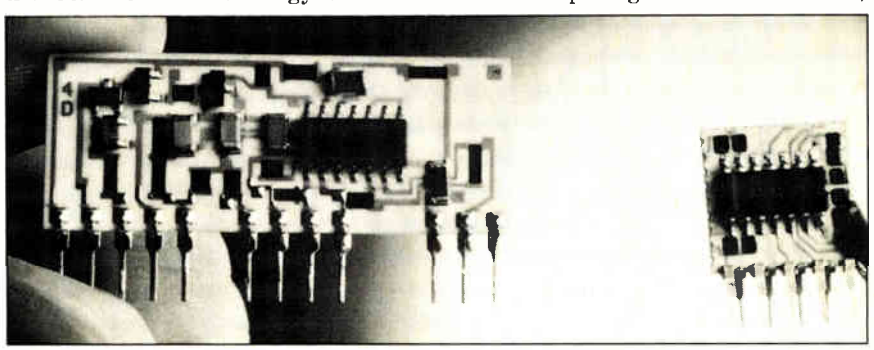
PACKAGING

EMBEDDING CAPACITORS SAVES CHIP REAL ESTATE

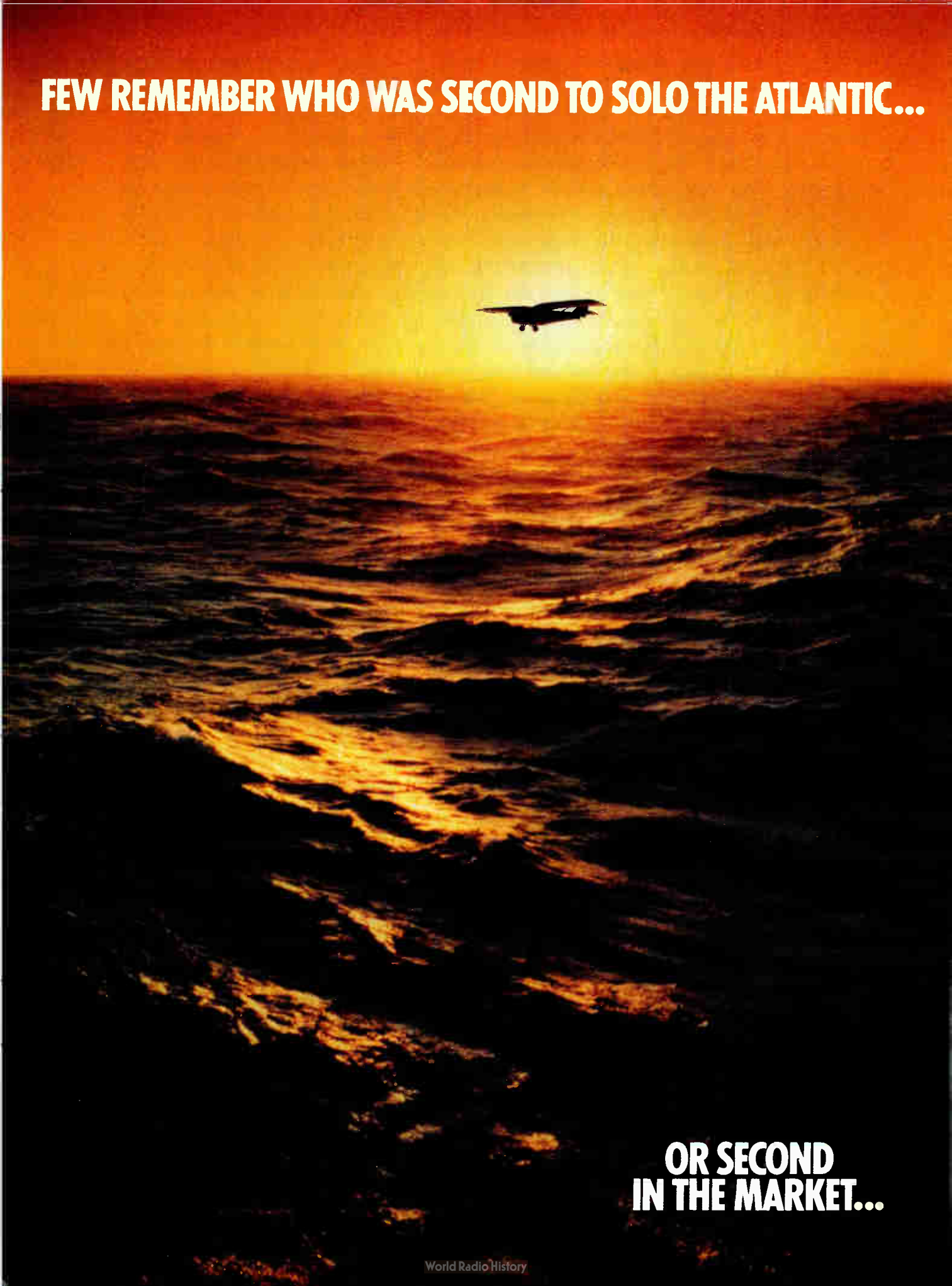
LEXINGTON, MASS.

Hybrid-circuit designers will be able to save a lot of real estate by integrating passive components into the ceramic substrate, thanks to developments in materials processing at Sprague Electric Co. The new technology combines the versatility of thick-film materials with the complexity of multilayer cofired ceramic-substrate manufacture.

Sprague, a Lexington-based unit of Penn Central Corp., calls the technology Multilythics, for multifunction arrays in monolithic packages. For the moment,



SHRINK. Multilythics will have capacitors in the substrate, thick-film resistors on the surface.



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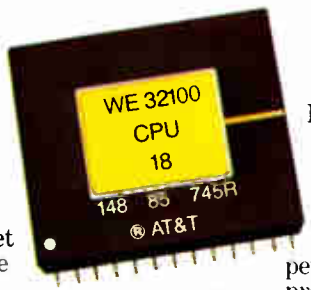

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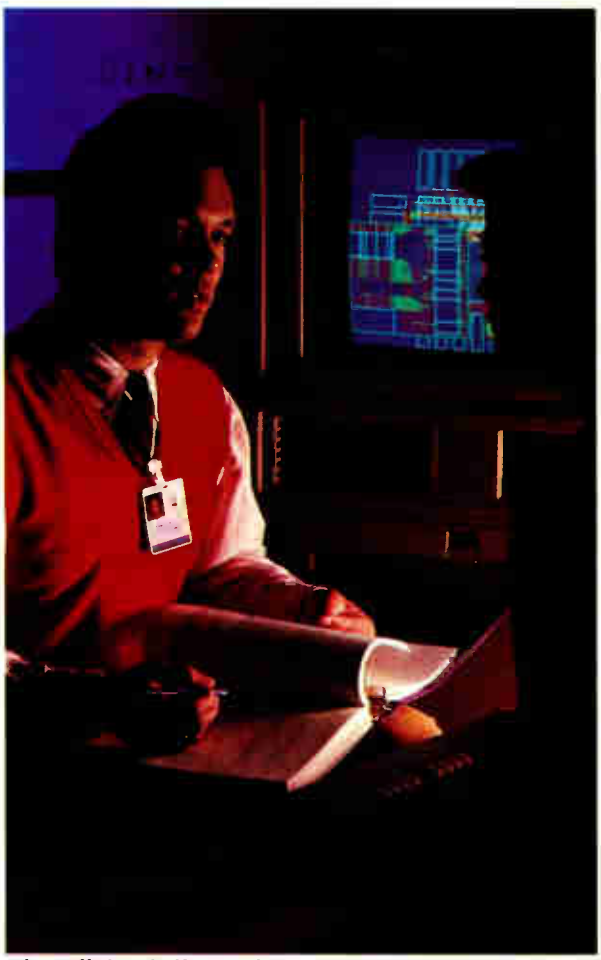

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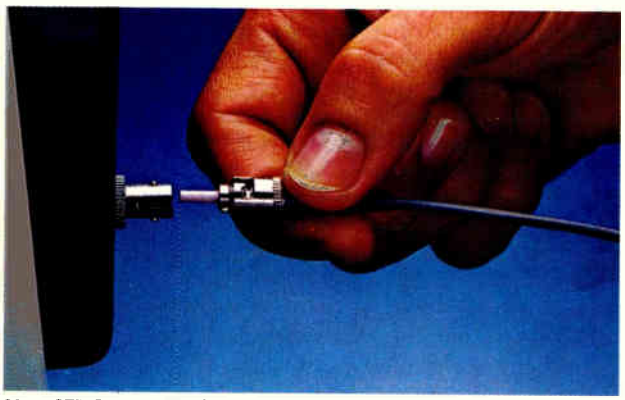

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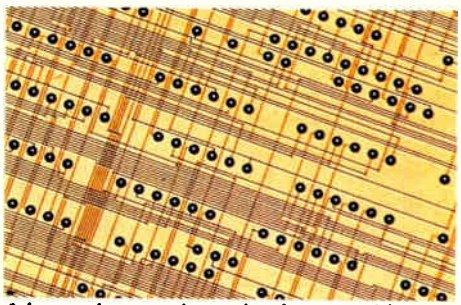

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development has focused on integrating capacitors within the substrate, says Peter Loconto, vice president and general manager of Sprague's Advanced Ceramics Division. The technology's ability to combine several dielectric layers makes it possible to embed capacitors with a wide range of characteristics.

SHRINK CONTROL. Key to the development was materials control. "It's all in the ability to control shrink factors during cofiring," says Loconto. More specifically, Sprague uses a so-called wet-stack or paint-processing technique to build its new chips. This process involves casting a slip onto an inert carrier, drying it, printing patterns using standard thick-film processing, and then casting subsequent layers in situ.

Capacitors are built between ceramic layers

Parlaying its experience in organic chemistry and mechanical engineering, Sprague says, it has optimized the basic process for printing location accuracy and for high uniformity, essential in achieving high manufacturing productivity for both large and small runs. A typical device might incorporate cover layers with low dielectric constants, high-dielectric-constant capacitor layers, low-constant capacitor-electrode and conductor layers, thick-film conductor and resistance layers, and finally, chips in surface-mount packages on top.

The flexibility of assembly obviates the need for standard or catalog parts. Instead, Sprague will allow customers to design their own devices with computer-assisted facilities integrated with its manufacturing area. The company also says it has cut the traditionally high cost of hybrid thick-film manufacturing by setting up process equipment in smaller modules. These modules are more efficient for short production runs.

In the future, Loconto expects that inductors, varistors, voltage-variable capacitors, and other passive parts may also be integrated into substrates. "There's no reason most passive components could not be integrated," he says.

For now, however, Sprague has chosen to keep resistors on the surface of the substrate to make trimming possible. "It's an application-specific technology, so we don't know the ratio of resistors to capacitors," says Loconto. "We don't know if there's a requirement for embedded precision resistors."

Sprague's pilot assembly line for Multilythics is to be replaced by a 30,000-ft² manufacturing plant in Hudson, N. H. The facility is scheduled to begin production in August and will employ 90 people initially. *–Craig D. Rose*

TINY CHANNELS TAKE HEAT FROM MULTICHIP MODULES

SEATTLE

Multichip ceramic modules are good for packaging the arrays of very large-scale integrated circuits needed for mainframes and supercomputers. But designers have not been able to stack these modules to get even higher density because they can't get rid of the heat. These modules dissipate hundreds of watts and they need heat sinks or other cooling schemes that are bulky and take long cabling to interconnect modules in a stack.

Now an innovative method for removing this heat has been developed that makes the stacking of these multichip modules possible. Two researchers from Japan's Nippon Telegraph & Telephone Corp. are using standard, cofired ceramic technology to fabricate microchannels in a multilayer substrate. These tiny tubes carry liquid coolant throughout the alumina substrate. Tohru Kishimoto and Takaaki Ohsaki, who work at NTT's Electrical Communications Laboratories, described their system in a paper at the Electronic Components Conference last week in Seattle [*Electronics*, May 5, 1986, p. 9].

After using computer simulation to investigate an optimal structure for the cooling section, they designed the channel cross section to be 800 μm wide by 400 μm high to achieve an appropriate thermal resistance. Based on the simulation, the researchers fabricated a package with a 5-by-5 array of 8-mm-square VLSI chips on an 85-by-105-mm alumina substrate. The substrate has 29 coolant microchannels, 6 conductive layers, and 900 input/output pins.

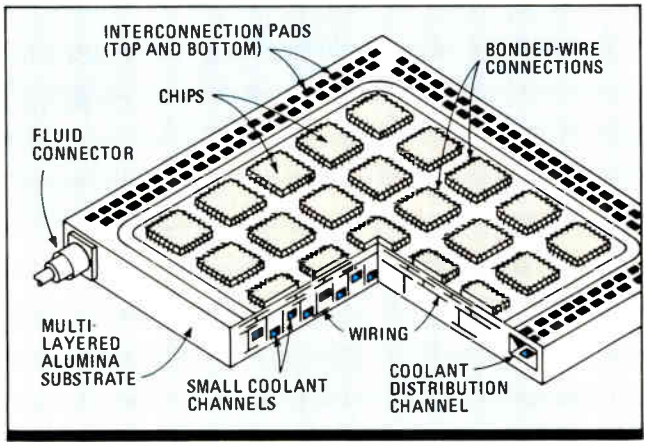
With a flow rate of 1 liter/m, the package can dissipate more than 400 W. Furthermore, because the cooling section is less than 1 mm thick, the volume power density increases to 17 kW/liter or more, a value 10 times greater than that obtained by conventional indirect water cooling, and equal to that of immersion cooling.

Very fine coolant channels are formed in the lower portion and between the vias of a multilayered alumina substrate. Multiple substrates are stacked horizontally into a card cage composed of three vertical printed-circuit boards arranged as an open rectangle. Interconnection pads fabricated on the vertical front and back surfaces of the substrate permit connection of the substrate to the pc boards.

COOLING. The coolant is supplied from an inlet port and sent to the channels by a distributor. The heat generated in the chips is conducted to the channels through the alumina substrate and transferred to the liquid. The warmed coolant is subsequently collected, then flows out through an outlet port.

There are four principal advantages to this new cooling method. First, the cooling and conductor layers can be formed into a single substrate by the same punching process used in via-hole formation. Second, a high cooling capability is realized by fabricating channels just inside the multilayer substrate. This structure has a lower thermal resistance because of the very short thermal passage and the high heat-transfer coefficient possible with the miniature channels. Third, high-density stacking is possible because of the minimal thickness of the cooling channels. And last, when replacement or inspection of VLSI chips is needed, performance tests can be carried out under the same conditions as those of an actual operating system, because the cooling section is formed within its own substrate.

The two Japanese researchers found that initial tests, based on epoxy die-bonded 8-mm-square chips, resulted in a dissipation of 12 W per chip and 300 W per package. Changing the die-bonding material to tin/lead solder increased allowable heat dissipation to 14.5 W per chip, or 360 W per package. *–Jerry Lyman*



CHANNELING. Tiny coolant channels were formed into the lower portion and between the vias of a multilayered alumina substrate.

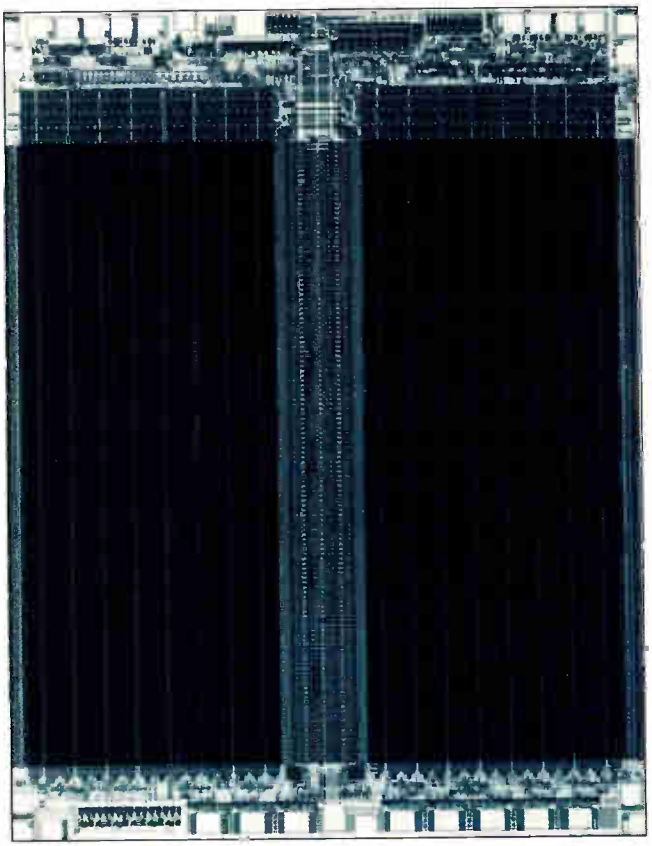
INSIDE TECHNOLOGY

THICK OXIDE BEATS THIN FILM IN BUILDING BIG EEPROMS

XICOR USES IT TO SOLVE 3-D SCALING PROBLEMS IN 256-K CHIPS

By abandoning the conventional thin-film route to fabricating high-density electrically erasable programmable read-only memories, Xicor Inc. may have overcome the problems that have kept the parts from climbing above the 64-K density level. The Milpitas, Calif., company employed a conservative 2-μm process and standard off-the-shelf 5× stepper lithographic equipment to build a 256-K EEPROM.

The key to doing this was the use of a thick oxide and a unique triple-polysilicon floating-gate cell, says William Owen, Xicor's vice president of research and development. The process is inherently more reliable and easier to scale to submicron dimensions, he claims, although it was more difficult for the Xicor engineers to master. They were less familiar with it than with the thin-oxide double-poly technology derived from EPROM manufacture.



1. SMALL DIE. Equivalent in size to many thin-oxide 64-K parts, Xicor's 256-K EEPROM die measures about 64,000 mils².

Conventionally used thin-oxide floating gates are relatively easy to manufacture, but cannot be scaled down easily without introducing significant reliability problems. This unpleasant consequence of the laws of physics is one reason many EEPROM houses are having difficulty moving to densities beyond 64-K to the 256-K level. To do so requires pushing minimum line widths on the oxides down to 1 μm using advanced photolithography.

"The problem with scaling EEPROMs lies in the fact that it is necessary to scale in three dimensions—in the vertical as well as horizontal directions," says Owen. "To achieve 256-K densities, not only must thin-oxide EEPROMs be scaled from 2 or 3 μm down to 1 to 1.5 μm in the horizontal direction, but from 90 to 100 Å down to about 70 to 80 Å in the vertical direction." To achieve similar densities in its 256-K EEPROM, Xicor found it necessary only to scale down from 3 to 2 μm horizontally and from 600 to 800 Å down to 400 Å vertically.

The thick oxide enabled Xicor's designers to form a basic EEPROM cell with a triple-poly structure that puts the programming portion atop the erase mechanism. This resulted in horizontal cell dimensions smaller than the thin-oxide structure.

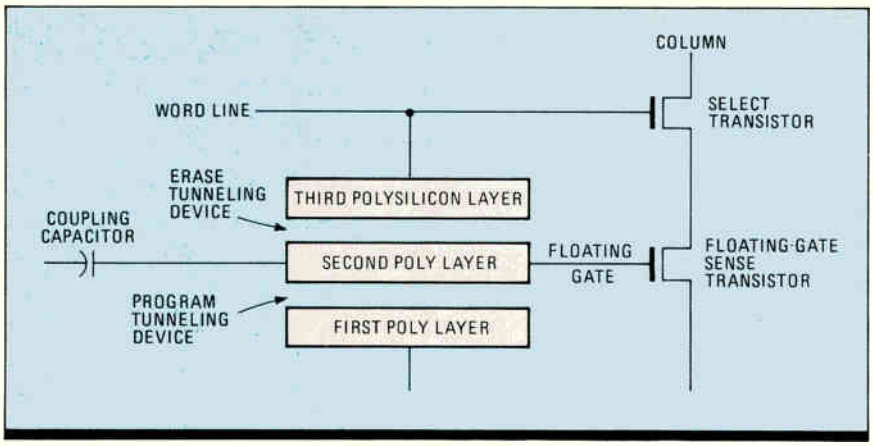
Another factor in the smaller size was the use of a proprietary textured thick-oxide surface on the programming elements. The textured surface's electrical potential per unit area is greater than conventionally used smooth surfaces, producing cells that are inherently smaller than comparable thin-oxide cells, but with the same effect. The oxide can be shaved off without affecting cell reliability, making vertical scaling relatively easy.

The first 256-K EEPROM fabricated with the 2-μm process is the 32-K-by-8-bit n-MOS X28256. It features a chip area of about 64,000 mils² (Fig. 1), equal in size to many thin-oxide 64-K parts fabricated using 1.5-μm design rules, and half the size of thin-oxide 256-K EEPROMs designed with 1- to 1.2-μm geometries. Soon to follow will be a CMOS version, the X28C256. Both parts feature 150-ns access times and support 64-byte page-write operations. A write cycle takes 31 μs per byte, enabling the entire memory to be written in less than 1 second.

In Xicor's triple-poly cell (Fig. 2), the floating gate sits between the upper and lower poly layers, forming the thick-oxide tunnel structures for erasure and programming. Compared with the 80- to 120-μm² cells of conventional 1-μm thin-oxide designs, the electrically erasable cell in Xicor's 2-μm 256-K parts measure only 68 μm².

The programming tunnel mechanism occurs between the first and second floating-gate poly layers; the erase tunneling action occurs between the second and third (Fig. 3, left). As in the thin-oxide approach, a selection transistor isolates the selected cell on a column while a capacitor develops, through capacitive coupling, enough voltage across a tunneling device to make electrons tunnel on and off the floating gate. This voltage is sensed by a MOS transistor, whose gate is formed by the second poly layer.

TECHNOLOGY TO WATCH is a regular feature of Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*



2. TRIPLE POLY. Key to the small die area is a unique triple-poly floating-gate cell. The gate, between the upper and lower poly layers, performs erasure and programming.

Because capacitance increases linearly as oxide thickness decreases, tunnel devices made with very thin oxides—80 to 100 Å thick—rate 5 to 10 times higher than tunnel devices made with 500- to 800-Å-thick oxides. Consequently, cells using thin oxide have to push photolithography requirements to the limit of available equipment and processes in order to make the thin-oxide tunneling devices as small as possible. The coupling capacitor, which must be made from a thicker, nontunneling oxide, ends up relatively large to obtain efficient coupling.

In contrast, thick-oxide tunnel devices inherently have very low capacitance. Therefore they can be made with reasonable feature sizes and still produce a small cell with good coupling-capacitor efficiency. Since the feature sizes used in the tunnel devices are compatible with the lithography requirements of the rest of the cell, they can be readily scaled down as advances in lithography technologies become available for manufacturing.

What makes this structure work is its surface, which Xicor describes as textured with hillocks (Fig. 3, right). Also called asperities, these odd-looking features were at first considered an undesirable side effect of MOS processing, and occur because oxidation progresses faster along some crystal directions than others. Because crystal orientation is random in deposited poly, there are points on the surface of an integrated circuit where oxide growth is enforced. The temperature of the oxide controls the size and shape of the hillocks.

Through the use of carefully designed and controlled fabrication techniques, Xicor exploits this phenomenon to build EEPROM transistors using thicker silicon dioxide layers that can still discharge the floating gate. Because the oxidation is a well controlled step, the properties of the emitters are exceptionally regular. They are shaped so that the electric field increases at the crest of the hills, substantially enhancing the emission of electrons.

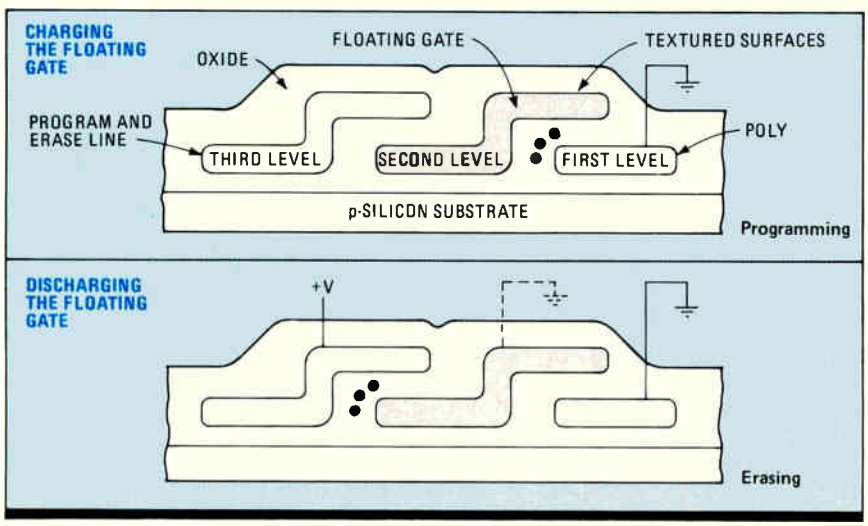
The poly electrodes are separated by oxide layers about 500 to 800 Å thick. Without the hillocks, Xicor says, 100 V would need to be applied to produce effective tunnel current. With the textured surfaces, the voltage required for tunneling is only 10 to 20 V, low enough to be generated easily on chip with an internal charge-pump circuit.

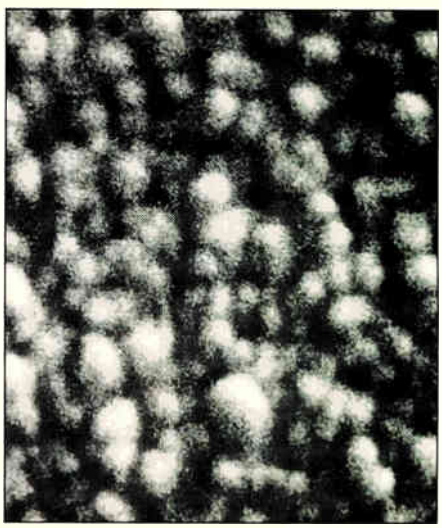
The coupling capacitor's size also contributes to the smaller cell area. To induce tunneling, the floating-gate voltage is raised or lowered through capacitive coupling to a bias-voltage supply. To avoid excessively high bias voltages, efficient coupling to the floating gate must be achieved by making the coupling capacitance much higher than all other floating-gate capacitances combined. These other capacitances include that of the MOS sense transistor, and especially that of the tunnel devices.

To electrically program a cell, electrons must tunnel onto the floating gate. In Xicor's triple-poly enhanced-emission cell, this is accomplished by applying a bias voltage to the coupling capacitor to capacitively pull the floating gate high and develop a voltage across the program tunneling device. When this voltage reaches the tunnel voltage, electrons tunnel from the first poly level's surface through the programming device to the second-level floating gate. When the applied voltages are brought back to normal reading levels, the programmed floating gate carries a negative voltage because of the extra electrons on it. When read, the MOS floating-gate sense transistor is turned off by the negative voltage and a 0 is produced at the EEPROM's output.

To electrically erase a cell, electrons must tunnel off the floating gate. In Xicor's triple-poly cell, this is done by capacitively coupling the second poly level's floating gate low while the third poly level's word line, which forms the other end of the erase tunneling device, is brought high. When the voltage across the erase tunneling device reaches the tunnel voltage,

3. TUNNELS AND TEXTURE. In Xicor's cell design, programming by tunneling action occurs between layers 1 and 2 and erasure between layers 2 and 3 (left). The thick-oxide cell approach uses a "textured" floating gate surface to enhance electron emission.





electrons tunnel from the second poly floating gate to the third poly word line. When the applied voltages are brought back to normal reading levels, this erased floating gate has a net positive voltage because of the lack of electrons on its surface. When read, the MOS floating-gate sense transistor is turned on by this positive voltage and a 1 is produced at the EEPROM's output.

Other advantages of the thick-oxide approach, says Owen, include improved data retention and endurance, or the number of data changes a nonvolatile memory can sustain before the first bit fails. Because the floating gates in the Xicor design are completely surrounded by thick thermal oxides, similar to an EPROM, data retention is excellent even at very high temperatures. "In fact, the only way retention can be measured on the thick-oxide devices is by subjecting them to temperatures over 300°C for several weeks," Owen says. "If these measurements are extrapolated, the typical retention for a Xicor EEPROM is more than 2 million years at 125°C." But for the record, the company is much more conservative, guaranteeing data retention of only 100 years at 125°C.

The data-retention advantages of the textured thick-oxide approach are retained—or even improved—as devices are scaled, he says. This is due to the fact that lower programming voltages are needed in order to scale the memory properly, so isolation widths and device channel lengths can be reduced in both the memory array and in the peripheral circuitry. However, for a typical part, which stores data in 3 ms and must retain it for 10 years, the tunneling current under storage and reading conditions must be reduced by at least 10^{11} than under programming conditions because the retention time is 10^{11} times longer than the storage time.

For planar nontextured tunneling structures, this is a difficult design constraint because the slope of the current voltage curve—that is, the relationship between the current and voltage of the tunneling device—is fixed. This means that the maximum allowable read voltage drops with the programming voltage on a volt-for-volt basis, not proportionately.

On the other hand, a textured-surface tunneling structure has a much steeper current-voltage curve; that is, for each increment of change in one voltage, there is an amplified increment of change in the other. In addition, the curve is not fixed, which means the relationship between the current and voltage can be tailored to yield steeper curves if necessary. This means that for a given maximum read voltage, a textured surface requires a lower programming voltage than a planar thin-oxide structure, leading to better scaling.

With regard to endurance, recent data on Xicor's EEPROMs indicates an expected failure-in-time rate of 0.015% per 1,000 hours, or 150 FIT, in systems requiring 10,000 data changes per byte over a 10-year period, says Owen. "Thus for many applications, the endurance-related fallout is actually similar to or lower than other semiconductor-related failure rates."

To achieve 1-Mb densities, Owen believes that although it will require moving to 1-μm geometries horizontally, only a few "tens of angstroms" reduction will be necessary in the vertical direction. "In thin-oxide EEPROMs, this is a reduction of 10% to 15% down to the operational limits of the floating-gate mechanism," he says. By comparison, Xicor's thick-oxide approach requires a reduction on the order of a few percentage points. "Moreover, the scaling is well within the limits of the Xicor cell design," he says. "As a matter of fact, we think we can continue to scale for several generations before we run into any of the problems our competitors are running into with thin-oxide EEPROMs." □

XICOR: FROM LONG SHOT TO LEADER

Life is sweet these days for Raphael Klein, Julius Blank, William Owen III, and Wallace E. Tchon, who all helped found Xicor Inc. in 1978. But they can recall the time when the Milpitas, Calif., company's chance of survival was considered a long shot.

"The problem was that few in the industry thought we had a technological edge except us," says Owen, vice president of research and development. "There was Intel Corp., with its thin-oxide approach to fabricating electrically erasable programmable read-only memories, and there was Xicor, with the thick-oxide approach. Everybody seemed to be going the thin-oxide route." All that is changing now.

First of all, it is becoming clear that the company is at least a generation ahead of its competition with its thick-oxide approach. While everyone else is pushing to 1-μm geometries to achieve 256-K products, Xicor is coasting along with a relatively conservative 2 μm to achieve the same density.

Second, thin-oxide advocate Intel has entered into a long-term agreement with Xicor for joint development of advanced EEPROMs. The deal also calls for mutual second-sourcing of EEPROMs and related products. Xicor has already received $6.5 million from Intel and will get $3.5 million more pending achievement of certain milestones, as well as a $10 million lease guarantee.

COMING UP ROSES. The commitment to thick-oxide EEPROMs finally starts paying off for Xicor Inc.'s Tchon (left), Blank, Klein, and Owen.

Third, the company continues to dominate the market it created, 5-V-only EEPROMs. Sales have grown from $2.8 million in 1982 to $39 million in 1984. Estimates for 1986 range as high as $55 million.

Finally, Xicor is now entering its third straight year of profitable operation after losing money the previous four. It owns about 50% of the market for 5-V EEPROMs and Novrams, static random-access memories backed by nonvolatile EEPROM cells.

Klein, now chief financial officer and chairman of the board, is a graduate physicist from the Israeli Institute of Technology and performed in a variety of technical management positions at Fairchild, Intel, Monolithic Memories, and National Semiconductor before starting Xicor as its first president. He holds two patents.

Owen, who joined the company to direct its development of advanced memories in 1978, holds an MS in electrical engineering and previously worked at Intel. As a process engineer and senior design manager, he was involved in the development and design of Intel's HMOS memory products.

Strategic planning vice president Tchon, who joined Xicor to aid in the development of its initial memories, is now principally involved in business planning, patent activity, and investor relations. With an MS in physics, Tchon holds 10 patents. Before Xicor, he held engineering positions at Honeywell Information Systems and Intel.

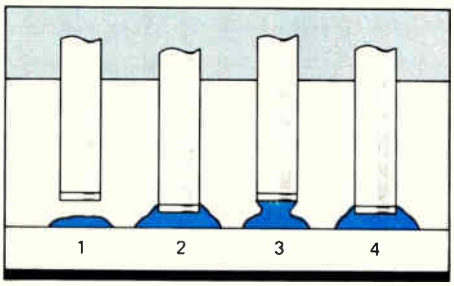
Blank, one of the original eight founders of Fairchild Semiconductor Corp. in 1957, has been a member of the Xicor board of directors since its founding.

WIRE-BONDING CHIPS TO BOARDS MAY SPEED SURFACE MOUNTING

SWISS SCHEME GETS HIGHER COMPONENT DENSITY BY USING BARE CHIPS

Surface mounting of components on printed-circuit boards is not catching on as fast as backers had expected in the U. S., but a Swiss company, Valtronic SA, has come up with a technique that could speed it up. In some cases, it may even be able to replace standard surface mounting. Called LSIS, for large-scale-integration shrinking, it is based on the smallest integrated-circuit package possible—the bare chip.

With LSIS, unpackaged LSI chips are wire-bonded to tiny pc boards that plug into larger motherboards. This is an extension of a technique called chip on board, a type of surface mounting that was developed for miniaturized digital watches and calculators. But unlike chip on board, which uses only small- or medium-scale-integration chips, LSIS bonds LSI chips—usually three or four—on pc boards that in general are even smaller than those used in chip on board. In some cases, a small number of surface-mounted discrete active and passive components can also be mounted on the same board, or on both sides of the board. The result is a packaging scheme that permits a higher component density than that of standard surface mounting because replacing IC packages with the bare chip saves huge chunks of board space.



1. COPLANARITY. In surface mounting, poor lead coplanarity in many components leads to nonexistent (1) or poor (3) solder joints.

LSIS has other advantages over traditional through-the-board mounting and standard surface-mounting technology, according to Alan Bertaux, president of Valtronic Inc., the company's U. S. subsidiary in Lombard, Ill. With the LSIS modular approach, the entire system does not need to be mounted on a single board, as they are in surface mounting. This allows for local miniaturization, and in turn minimizes repair problems.

The entire technique requires no technological breakthroughs or investment in special equipment or production processes. LSIS is based on established wire-bonding and pc-board-assembly technologies and does not require the special soldering and pick-and-place machines used in standard surface mounting.

There are three reasons for the use of only LSI chips in the LSIS approach. The first is that LSI chips use a lot of board real estate. Wire-bonding such dice directly to a board saves 80% to 90% of the space occupied by a similar packaged chip, even one in such miniaturized surface-mount packages as chip carriers, small-outline ICs, or flatpacks.

Packaged LSI chips are also expensive, often costing several dollars each. The corresponding die can cost as little as half that of an IC in a dual-in-line-package and 20% to 30% less than the same chip in a flatpack or SOIC package.

Finally, LSI dice are much more readily available than they were a few years ago, when IC makers were reluctant to furnish bare LSI dice because packaged ICs brought higher prices. Now, the availability of LSI dice is often better than that of packaged equivalents.

Without wire bonding, however, the use of bare chips of any size wouldn't be practical in LSIS or the older chip-on-board technique. In wire bonding, a gold or aluminum wire is welded directly from a chip's input/output pads to pads on a pc board, bypassing the extra operations of die-to-carrier bonding and carrier-to-board soldering used in conventional component mounting and surface-mounting assembly. A weld is more reliable than a solder joint and eliminates the coplanarity problems that affect flatpacks and SOICs, which often result in opens or poor solder joints (Fig. 1). Such tight packaging in LSIS greatly reduces electromagnetic interference.

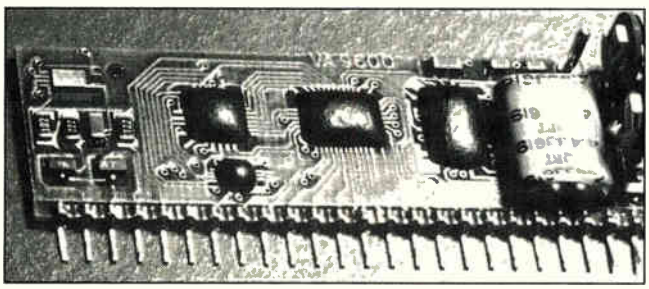
A striking advantage of LSIS is its ability to mount several LSI chips onto a DIP or a single-in-line package module. This is because in most applications, the chips share interconnections—that is, they "talk to each other." For example, a SIP module carrying four 40-pad dice can have as few as 25 pins. Though most applications require only three to eight dice, Valtronic has mounted up to 22 on one board.

The minimum board size for LSIS is about 0.25 by 0.25 in., bearing an LSI die on each side. Maximum board size can be 12 by 12 in. In most applications, board size will not exceed 1 by 4 in. Boards can be made of ceramic, epoxy-glass, or even flexible materials such as polyimide. LSIS boards, because they use bare chips, can also be much thinner and lighter than standard boards.

Using four unpackaged chips in an LSIS configuration on a SIP saves not only considerable board area but also money, compared with mounting the same four ICs packaged conventionally in DIPs on a standard pc board. In standard IC packaging, according to Valtronic, the four DIPs take up 5.6 in.^{2}. In LSIS, the total board area used is 0.375 in.^{2}. Total cost of the standard package is $9.34 versus the LSIS board's cost of $6.05.

The modular approach also allows the LSIS boards to be tested during assembly. Valtronic says the small boards with their limited number of chips can be functionally tested without the special fixtures usually required for surface-mount boards. In addition, use of LSIS modules reduces the number of components that have to be inserted on the motherboard.

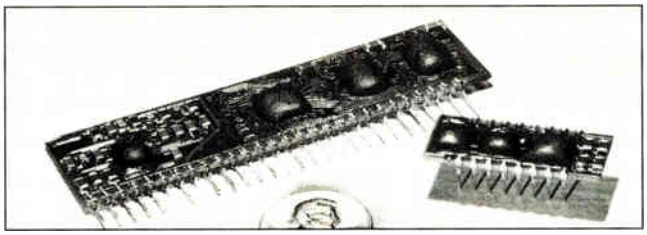
The assembly of an LSIS board requires no special equipment or technological advances. Board layout and manufacturing are standard, with one exception: for wire-bonding, 4-mil printed-circuit traces must be plated on the board



2. MINI MODEM. Direct wire bonding of LSI chips to a small printed-circuit board makes possible a modem half the size of a credit card.

for connecting the board to the chip's I/O pads. A wire-bond board also requires more care in its metallization than a board designed for soldering.

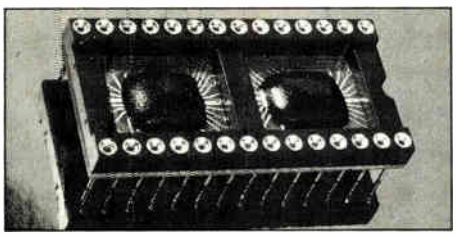
After the board is fabricated, dice are wire-bonded to the board and the chips thermosonically ball- or wedge-bonded to the pad patterns on the pc board. After bonding, the wires are pull tested to ensure good mechanical connection to the board before the chip is encapsulated. Valtronic typically looks for a pull resistance of over 10 grams per bond—about twice the resistance required in military chip bonding.



3. LSI SHRINKING. Using LSIS, a single-in-line package (left) can hold a video controller. A sensor's circuitry can fit in a small DIP.

The bonded dice are then covered with a protective epoxy encapsulation. A conformal coating can also be applied to the entire board.

Following this step, the encapsulated dice are tested electrically. Next, if the design requires, surface-mounted components such as resistors, capacitors, and discrete semiconductors can be applied by reflow soldering. The finished board can then be subjected to burn-in if desired, and then dynamically tested.



4. RAM MODULE. LSIS assembly permits four 32-K-by-8-bit CMOS RAM chips to be packaged in the space of a standard IC socket.

An objection often raised to LSIS is the problem of repairing bonded dice. The extremely thin wires used in bonding make such dice generally hard to replace, and replacement also risks damaging the fine-line pc-board traces. Bertaux argues, however, that the necessity for repair is a function of manufacturing yield. "Control your manufacturing to a point where you get 97% or 99.5% bond yield and you won't have to worry so much about repairs in the field," he says. Valtronic claims to have achieved rejection rates for finished and tested LSIS boards of a fraction of 1%.

"Our experience has also shown that LSIS typically involves the bonding of only three to four LSI chips on a module," Bertaux adds. "With standard epoxy blob protection, such dice are not repairable. But the risk is only a few dollars higher than for individual ICs. Besides, the LSIS modules are 100% tested by the assembler, and if a module should fail later in use, it is certainly easier and less costly to troubleshoot one LSIS with four chips than four individual ICs."

For boards involving more chips, it is possible to use plastic caps or a layer of silicone on top of the dice, so that they can be more easily repaired. Such caps can be removed without destroying the wire bonds.

The environmental reliability of LSIS is essentially the same as its standard IC-based counterparts, such as MIL STD 883. Packaging reliability depends more on the die's specifications than on the assembly method. Therefore, commercial-grade chips will produce commercial-grade LSIS specifications and military dice will meet military specifications.

Valtronic uses LSIS to produce boards to customer designs. With the technique, the company mounted four LSI chips plus several conventional surface-mounted devices in a modem board less than one fourth the area of a credit card—about 2 by ¾ in. (Fig. 2). Such a reduction in board size is particularly important where modem chip sets are concerned, and for laptop computer applications where space for a built-in modem is at a premium.

For a video controller, four LSI chips and a few surface-mount devices were packed on a 3-by-¾-in. SIP (Fig. 3). Valtronic also has built a sensor board that holds three LSI chips and several passive chips on one side of a module and more dice and passive chips on the other side of a 1.2-by-0.5-in. DIP, increasing packing density further.

Most recently, the company has applied LSIS to packaging both static and dynamic random-access memories. It has packed up to 32-K bytes of SRAM in the space of a standard IC socket by mounting dice on both sides of the module (Fig. 4). Some versions of this package include the decoder die and even a lithium battery for memory retention.

A new version of this SRAM module that will be introduced soon has an even greater memory density based on higher-density CMOS SRAMs. This module packs 1 Mb of SRAM (configured as four 32-K-by-8-bit chips) in a package of the same size. □

HOW THE SWISS GOT STARTED IN LSI SHRINKING

Alan Bertaux, president of Valtronic Inc., the Lombard, Ill., subsidiary of Valtronic SA, sees LSIS as a gradual approach to full surface-mounting technology in the U.S. The recession in the U.S. electronics industry and the reluctance of standard-board assemblers to take on new methods of assembly, soldering, and testing are holding surface mounting back, he says.

LSIS is a variation of the chip-on-board technique developed by Japanese and Swiss companies in the early 1970s for low-cost miniaturized digital watches and calculators. Chip on board was widely used in the U.S. during the heyday of video games and low-end home computers. But the decline of those two businesses nearly put a stop to chip-on-board production.

In 1978, Valtronic, Les Charbonnières, Switzerland, began producing microelectronic watch modules using what are now known as surface-mounted devices. It bonded microprocessor and memory dice directly to printed-circuit boards.

ALAN BERTAUX

"Valtronic was using these technologies long before there were names coined for them," says Bertaux. Building on this experience, Valtronic extended the technique into the more complex LSIS method.

Bertaux was born and raised in Paris. He left France for the U.S. at the age of 20 after completing the equivalent of an associate's degree in engineering at the University of Paris.

After three years in the U.S. Army, he earned a BA in political science at the University of Maryland, and also studied business management. He gained his engineering experience at two connector companies—Amp Inc., Harrisburg, Pa., and Molex Inc., Lisle, Ill. He then started an electronic-component import/export business before helping Valtronic set up a joint venture to promote U.S. sales of the Swiss company's products.

Valtronic now does all of its assembly work in Switzerland, but it plans to open an assembly facility in the U.S. to be run by Valtronic Inc.

HOW DATA GENERAL IMPROVED ITS LAPTOP DISPLAY

MODEL 2 COMES WITH CRT-QUALITY EL OR 2ND-GENERATION LCD SCREEN

Microcomputer users liked most of what they saw when they got their first look at the Data General/One laptop model back in September 1984. But there was one major exception: the machine's liquid-crystal display suffered from poor contrast—a problem common to all first-generation full-screen LCDs.

Last week, the Westboro, Mass., company sought to eliminate that problem by introducing its Data General/One Model 2. It has produced a pair of machines with high-contrast second-generation displays designed for enhanced readability. One version has a liquid-crystal display that is "tuned" to the center of the visible light spectrum for maximum contrast; the second incorporates a light-emitting electroluminescent display that inherently is high contrast. Both models will start shipping in July.

"There's no question that this is the best LCD available today in a commercial product," declares Robert Miller, senior vice president of Data General Corp.'s business group. The new LCD has a contrast four times better than competing LCDs, he claims; the contrast on the EL display is comparable to that of standard cathode-ray tubes. Both screens display 25 lines of text at 80 characters per line.

Data General calls its new laptop a 'portable XT'

Each model weighs less than 12 lb and comes with a multitude of ports for user-installable memory and communications options. "It's really a portable [IBM PC] XT," says engineering manager Ronald W. Pipe. "Fully loaded, this machine can have up to 640-K of main memory, internal 1,200-baud modem, floating-point option, 3½-in. double-density disk, and a 10-megabyte hard disk."

A set of internal rechargeable batteries and a built-in recharger make the LCD model completely portable. The LCD draws approximately 1 W of power and can run for up to 7 hours on a single charge. The EL version, which typically consumes 15 to 18 W, should be able to run for up to 3 hours from an external battery pack the company is developing for August delivery. Both units run on ac by means of a small external adapter.

Data General's Japanese subsidiary, Nippon Data General, did most of the design and development of the new laptops. It acquired the Model 2's LCD from a Japanese manufacturer, whose name Data General is keeping a closely guarded secret. The company's main research and development facility in Research Triangle Park, N. C., developed the unit's software. The project's far-flung components were coordinated at the company's headquarters.

In a typical configuration, the Data General/One Model 2 comes with 256-K bytes of internal random-access memory and twin 720-K-byte double-sided 3½-in. disk drives. With the LCD screen, the laptop will retail for $1,995. The EL version in the same configuration will cost $2,995. In place of the rear 3½-in. drive, a 10-megabyte internal hard disk is available for an additional $1,300.

The Model 2's four expansion slots make it easy to add features. Two general-purpose rear-panel slots accept a series of 4-by-4-in. option cards developed for the Model 2. They include a color adapter to support a standard red-green-blue color monitor; a second asynchronous controller (the basic unit comes with one); an IBM-compatible communications controller with modem; a "transceiver module" interface card that supports an external 5¼-in. drive; another transceiver module, which extends the 62-pin bus for attachment to external devices such as the previously available expansion chassis; and a 128-K-byte memory card.

The rear-panel memory-expansion slot can be fitted with a credit-card-sized printed-circuit board containing an additional 256-K bytes of RAM. All told, the unit can be expanded to 640-K bytes of internal RAM when both the 256-K-byte memory-expansion card and the 128-K-byte memory card that fits into the input/output slot are attached. The rear panel also contains a parallel printer port (the original Data General/One came with a serial port) and an RS-232-C communications port. There is a slot on the machine's side for adding an internal 1,200-baud modem card. A floating-point math option, added to the main pc board, is also available.

The displays use 640 pixels vertically and 200 horizontally, forming each character in an 8-by-8-pixel area. (The LCD actually has 256 pixels horizontally, but to maintain compatibility with standard software it uses only 200 of them.) Both screens have a 2:1 aspect ratio. "We have maintained the form factor and aspect ratios of a CRT so all the graphics software that's already out there runs unmodified," says Pipe. "So circles are circles and not ellipses."

To prevent burn-in of screen images, both displays feature automatic shut-off. If no keys have been depressed for 8 minutes, the screen goes dark. And the screens can be tilted out of the way, without having to remove them from the machine, so that the Model 2 can be used with a color monitor.

The most innovative technology in the twin laptops is here, at eye level. Birefringence, the splitting of a light beam into two components that travel at different speeds, is behind the second-generation technology

PORTA-READABILITY. The Data General/One Model 2 brings high-contrast LCDs (shown) and electroluminescent displays to laptops.

of the Model 2's LCD. It is used to tune the display's optical properties "very precisely to the center zone of the white-light spectrum. That allows for very sharp contrast between light that is going through and light that is not going through, which gives you the rapid difference"—that is, contrast—"between on pixels and off pixels," Pipe explains.

LCDs use reflected light to create characters. To turn a pixel on in any LCD, the orientation of the crystal associated with a given pixel must be changed. Once reoriented, the crystal will block the light entering the display and keep it from being reflected from the rear of the screen back to the viewer. The on pixel thus appears as a dark green spot against the lighter green of the screen's background.

"The conventional, first-generation LCD is simply a twisted-nematic-type display—the crystals in the media are twisted but allow all wavelengths to go through," says Pipe. Those displays work with the entire visible-light spectrum, and the problem is that "you might have some intermediate state where, around the fringes of the pixel, some of the light is going through and some of it isn't, so you don't get the sharp contrast between on and off."

The birefringence display, which is tuned to a much narrower wavelength, has the easier task of having to block a smaller chunk of the spectrum.

Strictly speaking, the new display uses both the birefringence effect and twisted-nematic crystal orientation. "You still have to rotate the crystals to switch on a pixel," says Pipe, "but the birefringence component of the system gives you the tuning and the narrower wavelength and gives more precise differentiation between things that are on and things that are off. The visual result is much sharper contrast."

The heart of the LCD is fabricated as a sandwich, with two layers of glass enclosing the liquid-crystal layer. This sandwich is much thinner than that on the Data General/One's display. The liquid-crystal layer is a mere 4 μm across, compared with 8 to 10 μm in the earlier display. Thin layers are needed to exploit the birefringence effect—the thinner the layers, the easier it is to tune to a particular wavelength.

EL technology, which graces the second version of the Data General/One Model 2, has inherently high contrast. A thin film is at the display's center, acting as a strong light emitter when subjected to an electric field. Whereas the LCD offers viewers a green screen, the EL panel displays dark orange characters. The EL display consists of a series of thin-film layers—also with thicknesses measured in microns—laid down by a thin-film vapor-deposition process.

The EL display's indium tin oxide outer layer holds the vertical bars, or Y-axis electrodes. Next a bright yellow emitting-phosphor layer is sandwiched between two dielectric insulating layers. This is followed by the aluminum row, or X-axis electrode layer. Typically, some 200 V must be applied to the EL display's phosphor to get it to glow. When an individual pixel is addressed, a charge is applied across the emitting-phosphor layer, causing that point to glow. When the charge is removed, the pixel shuts off.

Owners of the original Data General/One, which is being discontinued, can buy a second-generation LCD screen for their units for $600. □

HOW DATA GENERAL IS KEEPING UP IN LAPTOP TECHNOLOGY

Data General Corp. learned a lot about laptops from its original Data General/One, acknowledges senior vice president Robert Miller. He says that users "cited screen contrast as one of the major issues."

So the company concentrated on display technology in coming up with a new laptop. As a result, the Model 2 displays outperform those used on IBM Corp.'s new Convertible laptop [*Electronics*, April 7, 1986, p. 44]. It claims the two new displays—liquid-crystal and electroluminescent—have the highest contrast in any general-purpose computer.

According to Ronald W. Pipe, the Westboro, Mass.-based manager of the Model 2 project, "Now all the LCD vendors in the world have plans in place to develop products using this technology. Through our subsidiary in Japan, we have what we believe to be the inside track with a number of those people."

The EL panel in the other Model 2 version features a display acquired from Planar Systems Inc.

Another new technology incorporated into the Model 2 is the 3½-in. floppy disk. Data General helped pioneer the medium in the original Data General/One. But users have resisted the move from 5¼-in. floppy disks to the higher-capacity 3½-in. drives. Nonetheless, not only does the Model 2 feature the smaller drives but so does IBM's PC Convertible.

"We pioneered it, and IBM's decision ratifies it," says Agnes Imregh, Data General's director of product marketing. "So for once we don't have arrows in our back. It would have been tragic for us and, I believe, a mistake for IBM to have chosen a different format. The fact is they didn't, so we lucked out."

Although 3½-in. floppy disks are typically twice as expensive as the larger format, they hold twice as much data. So on a capacity basis, says Imregh, they are not more costly. And hundreds of major software titles currently are available in the smaller format.

Now that IBM has climbed aboard, she says, "a lot of customer fears will be allayed and they can now make their decision on the basis of product merit. That's an obstacle that we ran into in the past that we're very happy to see finally go away."

Whether easy-to-read displays and 3½-in. disks can get the sagging laptop market on its feet remains to be seen. For this year, though, forecasters predict industry sales will double to between 120,000 and 135,000 units. Data General won't say how many of those units it expects to sell. But according to Miller, "We expect to be one of the top two or three players in that market."

Clearly, Data General is betting that the small machines are here to stay. Adds Miller, "If anything epitomizes high technology, it's what's going on in these machines, and I think there are only a few companies that can effectively develop laptops competitively. This is really where the world is heading."

ROBERT MILLER

AGNES IMREGH

RONALD W. PIPE

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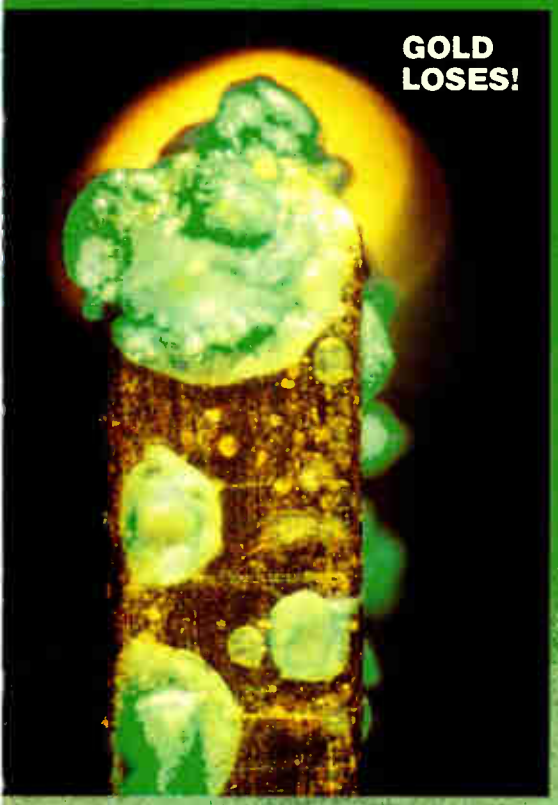

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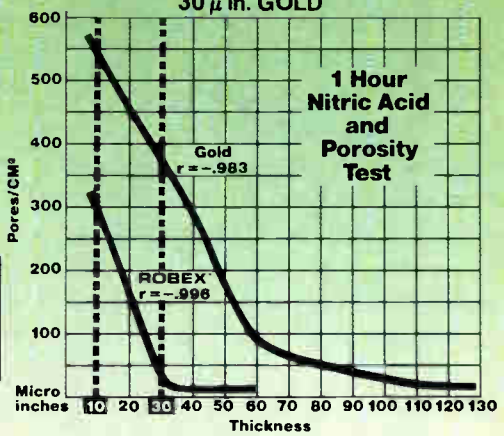

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PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED	SORTS AVAILABLE (ns)			PACKAGE OPTIONS
DYNAMIC RAMS									
TMM4164AP	64KX1	NMOS	YES	YES	150	200			P
TMM41256P	256KX1	NMOS	YES	YES	120	150			PT
TMM41257P	256KX1	NMOS	YES	YES	120	150			PT
TMM41464P	64KX4	NMOS	YES	YES	120	150			P
TC511000C	1MbX1	CMOS	YES	YES	100	120			C
TC511000P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC511001C	1MbX1	CMOS	YES	YES	100	120			C
TC511001P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC511002P/J	1MbX1	CMOS	YES	2Q'86	100	120			PJ
TC514256P	256KX4	CMOS	YES	2Q'86	100	120			P
TC514257P	256KX4	CMOS	YES	2Q'86	100	120			P
STATIC RAMS									
TMM2114AP	1KX4	NMOS	YES	YES	120	150			P
TMM2016AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2016BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015AP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2015BP	2KX8	NMOS	YES	YES	90	100	120	150	P
TMM2064P	8KX8	NMOS	YES	YES	100	120	150		P
TMM2063P	8KX8	NMOS	YES	YES	100	120	150		P
TC5504AP	4KX1	CMOS	YES	YES	200	300			P
TC5514AP	1KX4	CMOS	YES	YES	200	300			P
TC5516/17AP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18BP	2KX8	CMOS	YES	YES	200	250			PFY
TC5517/18CP	2KX8	CMOS	YES	YES	150	200			PFY
TC5565P	8KX8	*CMOS	YES	YES	120	150			PFY
TC5565AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5563AP	8KX8	*CMOS	2Q'86	2Q'86	100	120			PFY
TC5564P	8KX8	CMOS	YES	YES	150	200			PY
TC55257P	32KX8	*CMOS	YES	YES	100	120	150		P
HIGH SPEED STATIC RAMS									
TMM2018D	2KX8	NMOS	YES	YES	35	45	55		D
TMM2068D	4KX4	NMOS	YES	YES	35	45	55		D
TMM2078D	4KX4	NMOS	YES	YES	35	45	55		D
TC5561P	64KX1	*CMOS	YES	YES	70				P
TC5562P	64KX1	*CMOS	YES	YES	45	55			P
EPROMS									
TMM2764D	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764DI	8KX8	NMOS	YES	YES	150	200	250		D
TMM2764AD	8KX8	NMOS	YES	YES	150	200			D
TMM27128D	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128DI	16KX8	NMOS	YES	YES	150	200	250		D
TMM27128AD	16KX8	NMOS	YES	YES	150	200			D
TMM27256D	32KX8	NMOS	YES	YES	150	200			D
TMM27256DI	32KX8	NMOS	YES	YES	150	200			D
TMM27256AD	32KX8	NMOS	YES	YES	150	200			D
TC57256D	32KX8	CMOS	YES	YES		200	250		D
TMM27512D	64KX8	NMOS	YES	YES		200	250		D
ONE TIME PROGRAMMABLES									
TMM2464AP	8KX8	NMOS	YES	YES	200				PF
TMM24128AP	16KX8	NMOS	YES	YES	200				PF
TMM24256AP	32KX8	NMOS	YES	YES	200				PF
TMM24512P	64KX8	NMOS	2Q'86	2Q'86	250				PF
MASK ROMS									
TC5364/5/6P	8KX8	CMOS	YES	YES	250				P28
TMM23256P	32KX8	NMOS	YES	YES	150				P28
TC53257P	32KX8	CMOS	YES	YES	200				FP28
TC53512P	64KX8	CMOS	YES	2Q'86	200				P28
TC531000P	128KX8	CMOS	YES	YES	200				P28
TC532000P	256KX8	CMOS	YES	2Q'86	200				P32

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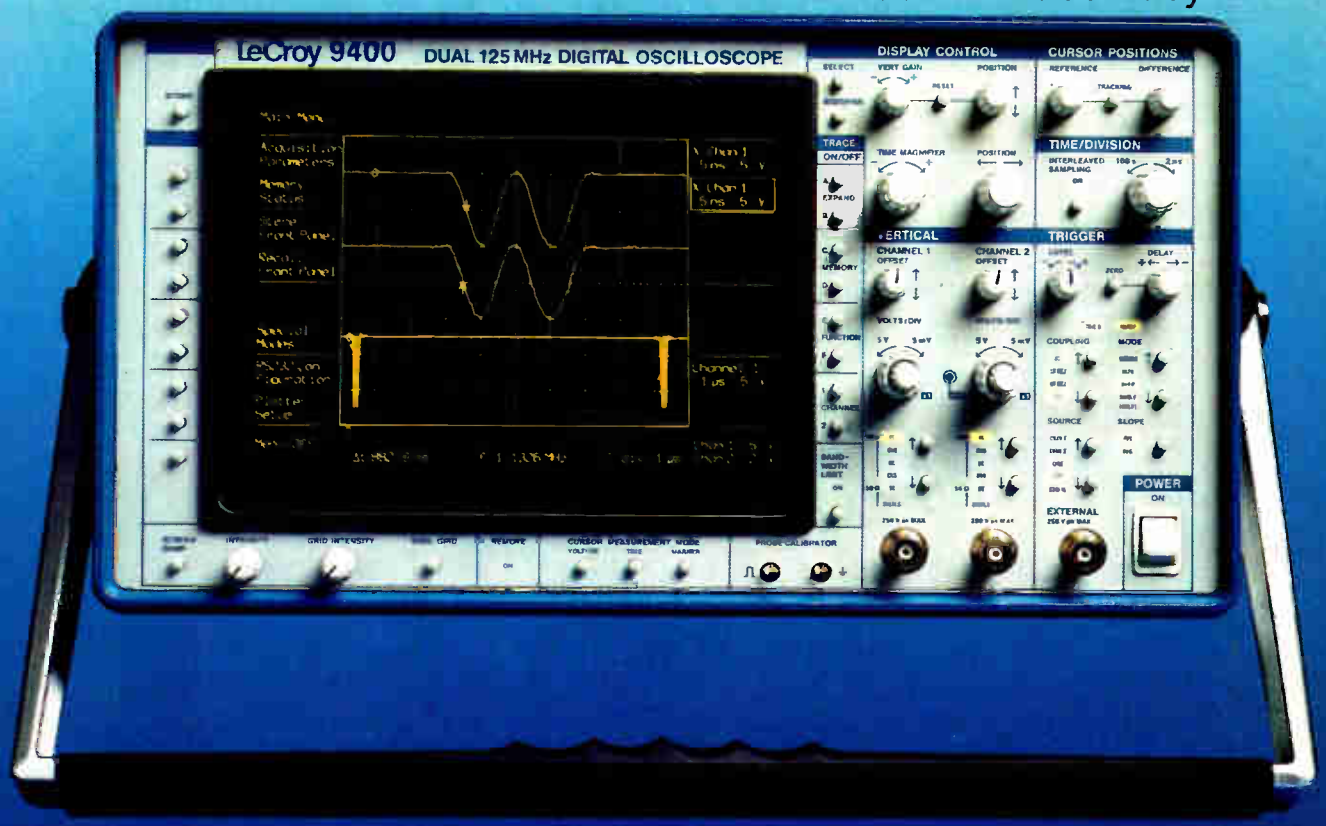

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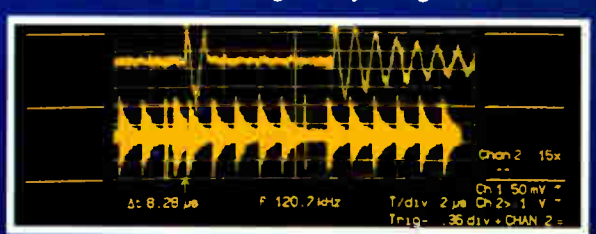

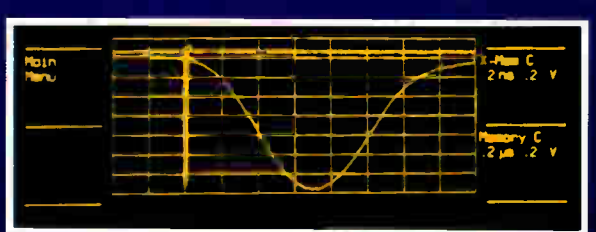

Top: Dual zoom and time cursors are applied to measure delay between double pulses with 100 ps resolution and 0.002% precision.

Middle: Channel 2 is segmented in 15 partitions of 2,000 words each. Expansion of event #3 appears on top.

Below: A 10 ns wide pulse is digitized with 5 Gs/s interleaved sampling speed. Expansion to 2 ns/div shows outstanding time and screen resolution.

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CAN JAPAN CATCH UP IN 32-BIT MICROPROCESSORS?

PROBABLY NOT IN THE NEXT DECADE, DESPITE A RUSH OF PRODUCT R & D

by Bernard Conrad Cole and Charles L. Cohen

Time is running out on the Japanese chances to play much of a role in the upcoming billion-dollar annual market for 32-bit general-purpose microprocessors. Current trends indicate that Japanese participation will be virtually nonexistent through at least the mid-1990s.

"It's hard to believe," comments John Payne, director of advanced product development and planning at National Semiconductor Corp., "but it does not appear that the Japanese will be a significant factor in the 32-bit market—at least in the first round of applications—despite all our assumptions to the contrary."

The market numbers are rapidly turning against the Japanese, confirms M. L. Bader, president of Bader Associates, Mountain View, Calif., and author of a study on the impact of 32-bit microprocessors on the computer-systems market. Although Japanese companies are not talking much about their plans, various industry sources indicate that Fujitsu, Matsushita, Mitsubishi, Oki, and Toshiba, among others, have proprietary central processing units under development. What is not certain is when, and if, these circuits will see the light of day.

"Whatever they are planning, they had better hurry up," says George Alexy, microprocessor marketing manager at Intel Corp. in Santa Clara, Calif. "The window of opportunity—that is, the time frame within which they have to introduce the device and obtain design commitments—is narrowing rapidly." Predicts National's Payne: "At most,the Japanese companies have a year or less to establish any sort of presence in the 32-bit market."

Key figures in the Japanese semiconductor industry tend to echo this gloomy assessment. Next year is the deadline for announcing any new CPU for the present market, acknowledges Kenji Kani, manager of the System Design Department of NEC Corp.'s Microcomputer Products Division. Agreeing is Hiroshi Kadota, senior engineer at Matsushita Electric Industrial Co.'s Advanced Devices Laboratory of the Semiconductor Research Center, estimates that the window for introduction of a new 32-bit CPU is extremely short—about a year and a half at most.

But many of the Japanese designers won't be pinned down. Joe Nakajima, manager of Hitachi Ltd.'s Technical Marketing Department, thinks the appropriate product can be announced anytime and still participate in the market. NEC's Kani agrees, adding that a revolutionary design can be announced at any time.

Though there will probably always be a place in the market for an innovative architecture, acknowledges Keiji Namimoto, senior manager of the Integrated Logic and System Department at Toshiba Corp.'s Semiconductor Group, he warns that it will gradually become difficult to participate in the standard 32-bit microprocessor market because of the lead time that existing architectures have in gaining market share.

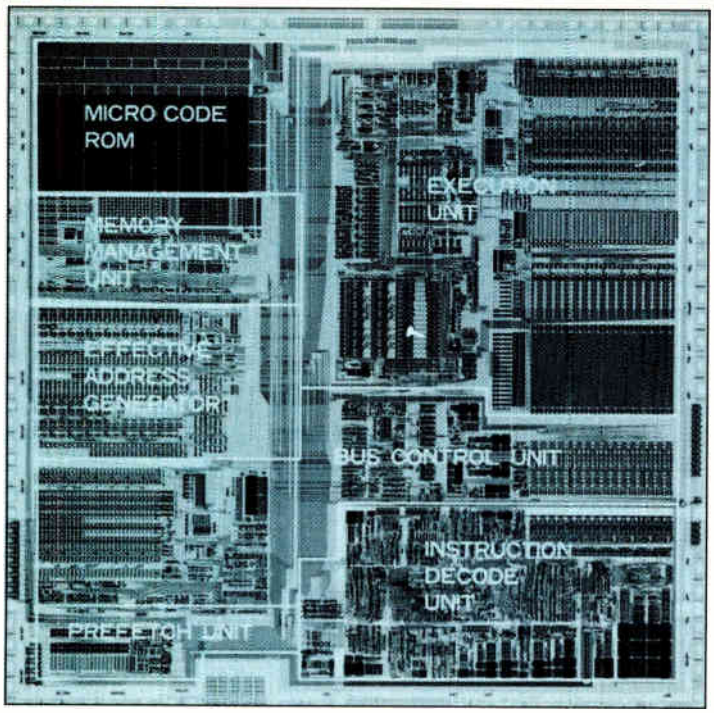
If current trends continue, says Bader, the Japanese will have little or no market share by 1990. Motorola Inc. will probably be in the No. 1 spot by then, he predicts, with 27% of the world market, including sales of CPUs by second-source suppliers. Intel would grab second place with 25% of the market, while he expects National Semiconductor to be No. 3, with about 18% of the market, including sales from its second sources—Texas Instruments Inc. and possibly one of the major Japanese manufacturers. Bader says that AT&T Co. will most likely be No. 4, with 11% of the market, and Zilog Inc. will probably take the fifth place, with 9% [*Electronics*, May 5, 1986, p. 40].

That would leave about 10% of the market for the other players, which Bader says currently include such vendors as Fairchild Semiconductor Corp., Inmos International plc, and a half dozen or so other manufacturers that Japanese companies will have to battle if they choose to develop proprietary architectures.

There are only two other routes the Japanese can pursue to gain market share: either adapt their proprietary architectures to make them also operate in an emulation mode or go a strictly second-source route. However, says Bader, "new, more strict U. S. copyright laws governing designs are making it virtually impossible for the Japanese to become unlicensed second-source suppliers of U. S. designs." Furthermore, there is increasing reluctance on the part of U. S. manufacturers to license new technology to the Japanese.

"It's not like the late 1960s and early 1970s, when U. S. companies naively licensed products and designs left and right to the Japanese, only to find the market pulled out from under their feet," says Intel's Alexy. "U. S. manufacturers have learned their lessons and are really playing hard to get."

So far, only one Japanese company, NEC, has announced its intention to



1. JAPANESE HOPE. Introduction of the V60 gives NEC a head start over other Japanese companies in the world market for 32-bit microprocessors.

manufacture a 32-bit CPU family in direct competition with the likes of AT&T, Intel, Motorola, and National Semiconductor. However, says Bader, it does not appear that its CPUs—the V60 and V70—will be in production much before mid-1987. One other company, Hitachi, is sitting on the fence with a proprietary CPU, the Micro 32, hoping that its protracted negotiations with Motorola's Semiconductor Products Sector will pay off and that it will be able to enter into production with a second-sourced version of the U. S. company's 32-bit 68020 CPU.

Japanese and U. S. industry observers agree that NEC is probably the only Japanese company that can expect to garner a share of the 32-bit market worldwide, thanks to its recent introduction of the V60 (Fig. 1) and V70 series, executed in 1.5-μm CMOS geometries and incorporating 375,000 transistors on a single die.

Scheduled to be in volume production in early 1987, the V60 uses a 32-bit architecture internally with a 16-bit external data bus and a 24-bit external address bus. The V70, by contrast, is a full 32-bit device. According to Richard Naro, V series microprocessor manager, both devices feature on-chip virtual-memory management, an arithmetic floating-point processor, and a six-stage pipelined architecture. Consuming only 1.5 W, the V60 can execute 3.5 million instructions per second at a clock speed of 16 MHz.

PIPELINE ARCHITECTURE

Internally, the processors are divided into six independently operational units organized into a pipeline structure (Fig. 2). The prefetch unit prefetches instructions into a 16-byte prefetch queue, and the instruction-decode unit decodes the instructions and sets commands into a 2-word-by-53-bit decoded-instruction queue. The effective address generator calculates the operand addresses, and the virtual-memory-management unit translates virtual addresses into real addresses. The bus-control unit initiates memory access for instruction and data fetching, and the execution unit carries out the instruction-set functions. According to Naro, the execution unit is a microprogrammed 32-bit data-path processor with thirty-two 32-bit general-purpose registers, sixteen 32-bit scratchpad registers, a 64-bit barrel shifter, and a 32-bit arithmetic logic unit. In addition to its normal arithmetic operations, the ALU implements a second-order Booth's algorithm, allowing multiplication of either 32- or 64-bit-long floating-point data according to the IEEE-754 standard.

Featuring a typical instruction-execution cycle time of 62.5 ns, the V60 incorporates 273 instructions of 119 types, as well as 21 addressing modes and up to 4 gigabytes of demand-paged virtual-memory space.

NEC has also developed a 32-bit CPU, the IDP1, which is designed for use in its family of office computers. The device has 87,000 gates on a 12-by-12-mm chip. Design of this microprocessor was started five years ago, long before commercial 32-bit microprocessors became available and even before it was evident what they would look like. But NEC engineers knew they needed a high-speed, highly integrated engine for their office computers, and they set out to build the IDP1, which operates at a 10-MHz clock speed. The first computers using this chip were shipped in May 1984. Even today, NEC does not have a general-purpose chip that surpasses this special-purpose one for its office computers because its 32-bit V60, which is just coming out, has only a 16-bit external bus.

Depending on whether it can work out a mutually satisfactory second-source agreement with Motorola, the only other company with a chance of grabbing a share of the 32-bit market is Hitachi, with its Micro 32, which was unveiled in late 1984. The performance characteristics of the Micro 32 have been proven only in the laboratory, says Bader. If Hitachi cannot work out an agreement with Motorola, the part will probably be ready by mid to late 1987, estimate such industry observers as Gene Finkler, author of the four-volume *32-bit Microprocessors*.

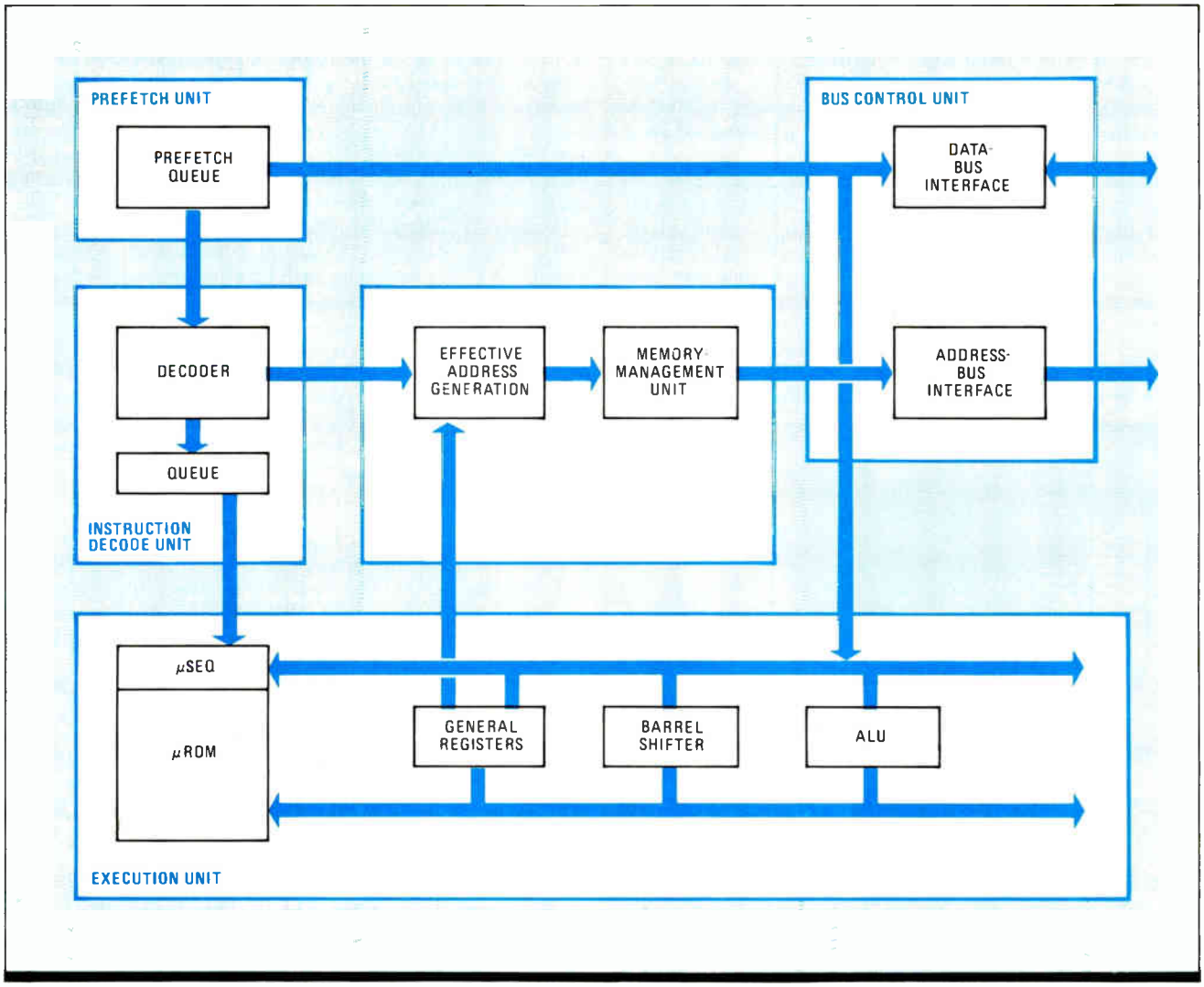
Said to be upwardly compatible with the Motorola 68000 family, the Micro 32 (also known as the HD63020) is fabricated using a 1.3-μm CMOS process. Containing about 400,000 transistors, the Micro 32 features a heavily pipelined architecture with on-chip 256-bit cache memory and 256-K of read-only memory and incorporates an extended instruction set of which the 68020 is a subset. The 32-bit CPU, which features an internal clock rate of 20 MHz (40 MHz, external), is designed to operate at about 4 to 5 mips, with a typical power dissipation of 0.5 W. Typical instruction-execution cycle times are in the 60-ns range.

More questionable in terms of their future in the marketplace are some later entries, such as the MB32 from Fujitsu, the 32-bit designs from Matsushita and Mitsubishi, and the Toshiba TMB, all of which Finkler expects to be introduced before the end of 1987. According to Finkler, the MB32 is a sub-2-μm CMOS general-purpose CPU that incorporates many digital signal-processing functions, and the Matsushita CMOS design uses a more traditional design with 32-bit internal and external data buses, on-chip direct memory access and cache memory, and a 4-Gb virtual-address range. The Mitsubishi 32-bit CPU is a sub-2-μm design that supports image and graphics processing. The Toshiba design uses a highly parallel architecture with on-chip barrel-shifter logic, special multiplication hardware, an instruction-prefetch queue, and special floating-point instructions, according to Finkler.

DIFFERENT ROUTES

Alternatives to a new microprocessor could be special-purpose processors that would be attached to any host through the general bus interface, says Kadota of Matsushita. Toshiba's Namimoto says his company is considering alternatives to the 32-bit microprocessor, including proprietary peripherals, coprocessors, digital signal processors, and special-purpose application-specific memories.

At least three of the five leading Japanese semiconductor



2. FULL PIPELINE. NEC's V60 microprocessor has a heavily pipelined, six-stage, 32-bit internal architecture with a 16-bit external data bus and a 24-bit external address bus. It executes 3.5 million instructions per second at 16 MHz.

companies appear to be hard at work developing 32-bit CMOS chips for TRON (The Real-time Operating-system Nucleus), an operating-system kernel developed by Ken Sakamura of Tokyo University [*Electronics*, July 22, 1985, p. 46]. Hitachi, Matsushita, and Mitsubishi are working on chips that adhere to Sakamura's design but are implemented in different ways. Two other companies, NEC and Fujitsu, are part of the same group that is working to promote TRON. There are rumors that Fujitsu cannot get a license for the Intel 80386, and so it is also actively working on TRON hardware.

TRON has been implemented for a variety of popular microprocessors, including Intel's 8086 and 80286, Motorola's M68000, and NEC's 16-bit V series and 32-bit V60. Moreover, engineers at Mitsubishi have considered an implementation for National's NS32032. However, the full benefit of TRON can be expected only on chips designed with TRON architecture, which is needed to take full advantage of its high-speed real-time task switching.

It is not obvious where the project will lead, and the companies involved are not talking. Matsushita could reap maximum benefits because it is not yet participating in 32-bit chips or systems. TRON would provide the company with a high-performance proprietary chip that is operating-system-compatible with available software and yet should not infringe on the intellectual-property rights of other companies. It would enable Matsushita to compete in the 32-bit microprocessor arena much more favorably than it does in the 16-bit market, where it has a high-performance CMOS processor used only by the company, its subsidiaries, and a Matsushita-Fujitsu joint venture.

TRON'S CLOUDY FUTURE

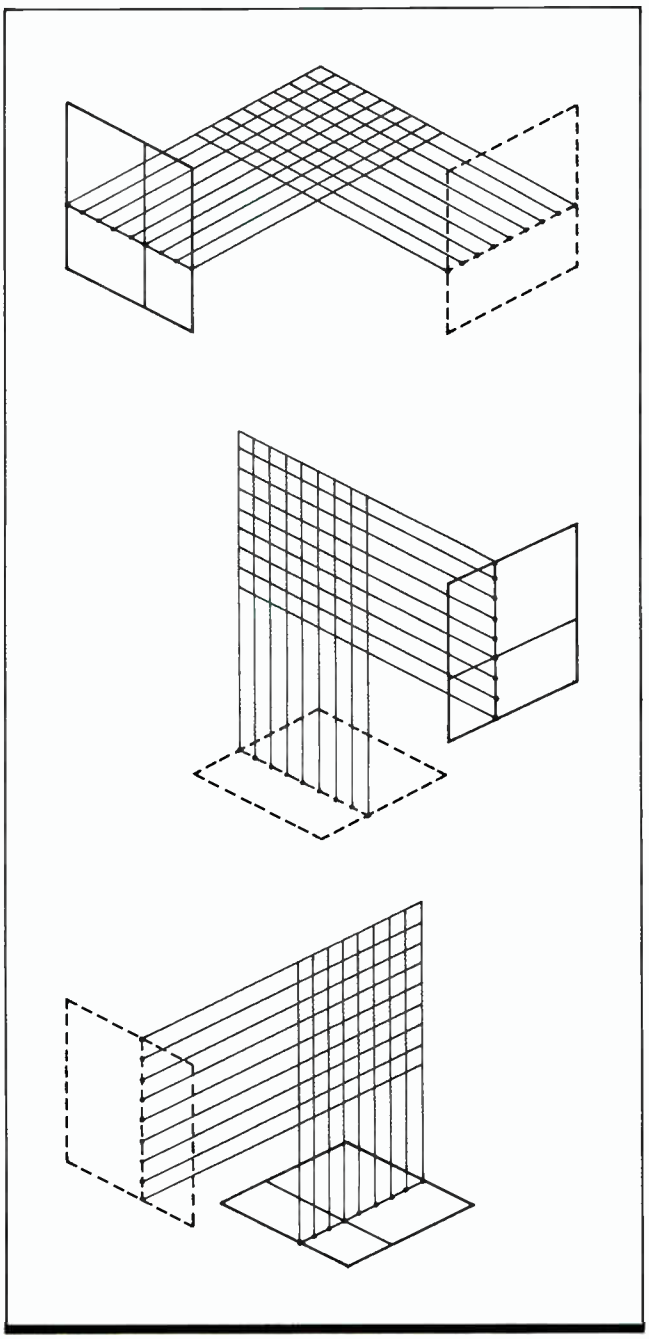
But there is a dilemma with the TRON chip: from an engineering viewpoint, TRON shines most brightly in its I-TRON implementation, which is for industrial applications; but only business applications (which would use the B-TRON version) such as work stations and personal computers seem likely to generate enough sales volume to make the chip commercially successful in the immediate future. So, like other manufacturers in the TRON group, Hitachi is searching for new high-volume applications. NEC could elect to stand pat with its proprietary V60 and its software implementation of TRON rather than marketing a TRON chip as well. But this, too, is a gamble, especially because the lower-end members of its V series are the subject of litigation between NEC and Intel. By contrast, no one has accused the higher-end V60 of being unoriginal, but industry sources say that U. S. customer reluctance to buy the other members of the series could extend to the V60.

Hitachi is also working with Sakamura of Tokyo University on development of a TRON processor chip. TRON is most needed for the industrial I-TRON operating system, but there

probably isn't enough demand for such a chip to make it attractive. Demand for the B-TRON business version could be sufficient to go into production, but Hitachi claims that it still has no firm plans for commercial production of such a chip.

In addition to its general-purpose 32-bit design, Matsushita is developing both a 32-bit TRON chip and a specialized 32-bit microprocessor for parallel computing.

Matsushita will use a 16-by-16-microprocessor array to build a parallel computer that differs significantly from the vector pipeline processors that have become standard for supercomputing. It is most suitable for numerical solutions of the three-dimensional partial differential equations common in science and engineering. The parallel-architecture supercomputer is based on the work of Tatsuo Nogi, associate professor of applied mathematics and engineering at Kyoto University. Nogi's prototype version of this computer uses Fairchild F-8 microprocessors connected in a 16-processor, one-dimensional (linear) array.



3. ADENA. A parallel-architecture supercomputer scheme alternately switches the planes in a cubic memory array.

Nogi's scheme starts with a 1-d array of processors for 2-d parallel processing. In the future, it will be enhanced to a 2-d array of processors for 3-d processing. To process along three coordinate axes, the computer will have a 3-d array of buffer-memory units. The computer array will be alternately (sequentially) connected by data buses to perpendicular planes in the cubic memory array for each processor to access a 1-d subarray of memory buffers (Fig. 3).

Designated Adena, for alternating direction edition nexus array, Nogi's design is based on a method of alternating direction for 1-d processing, with data for processors of different states implemented as a 16-by-16 array of 32- or possibly 64-bit microprocessors. Four very large-scale-integration chips will be developed for the commercial version. Slated for completion by the end of 1988 are the microprocessor, DMA controller, I/O buffer, and a custom memory chip for use as data or instruction memory. Budget for development includes direct costs of $4.4 million, according to Hiroyuki Mizuno, managing director of the Semiconductor Research Center.

32-BIT VLSI

One of the most active Japanese organizations in the 32-bit field has been the research laboratories of Nippon Telegraph & Telephone Public Corp. and its successor, NTT Corp. Researchers there have successfully integrated mainframe-architecture computers and central office switches in CMOS VLSI.

The first attempt to build a 32-bit VLSI processor was a bipolar-VLSI feasibility study. Its goal was to build a CPU for a telephone central office switch that was functionally compatible with NTT's D70, which is implemented with ECL circuits. Super self-aligned subnanosecond bipolar technology was selected for the 12,000-gate array to achieve the speed needed for the required throughput. Design of this processor was considered significant, and a paper was given at the 1981 Custom Integrated Circuits Conference. However, the project was abandoned before the chip was made fully operational because it became obvious that this single chip was insufficient. High-speed memory and other chips would be needed to make the processor chip useful and complete.

Since then, NTT researchers have used a 2-μm CMOS process to develop an integrated chip that incorporates the arithmetic and control functions of the large computer architecture used in NTT's DIPS on-line computing systems. This 20,000-gate device with a cycle time of 200 ns first operated in 1981 and was announced at the 1982 International Solid State Circuits Conference. Because it is not a complete CPU, other chips are needed to round it out to a single-board processor. Also developed for this system are an I/O processor and an integrated communications adapter. Master-slice chips with 5,000 to 10,000 gates are used for the logic portions of the CPU, the I/O processor, and the integrated communications adapter.

These chips are incorporated in the DIPS-V20 system that could be used in a banking system as a network node processing system, a distributed processing system, or a small on-line processing system (Fig. 4). Throughput of the DIPS-V20 for a banking mix (an instruction set optimized for banking applications) is 0.2 to 0.3 mips. This is fully one third that of the DIPS-11/5 mainframe. Two CPUs are used in systems that require higher performance. Performance appears to be low compared with that of other computers because banking applications are I/O intensive and consequently slower than other applications.

Like the DIPS-11/5 that it replaces in low-end systems, the V20 CPU is manufactured by Hitachi. NTT will not reveal who makes the two peripheral chips, but it is highly possible that they are divided between NEC and Fujitsu, which make the midrange and top-end mainframes in the DIPS series. NTT engineers say that their V20 and V30 chips are downsized

mainframe-architecture chips, much like the IBM 370 chip described at this year's ISSCC.

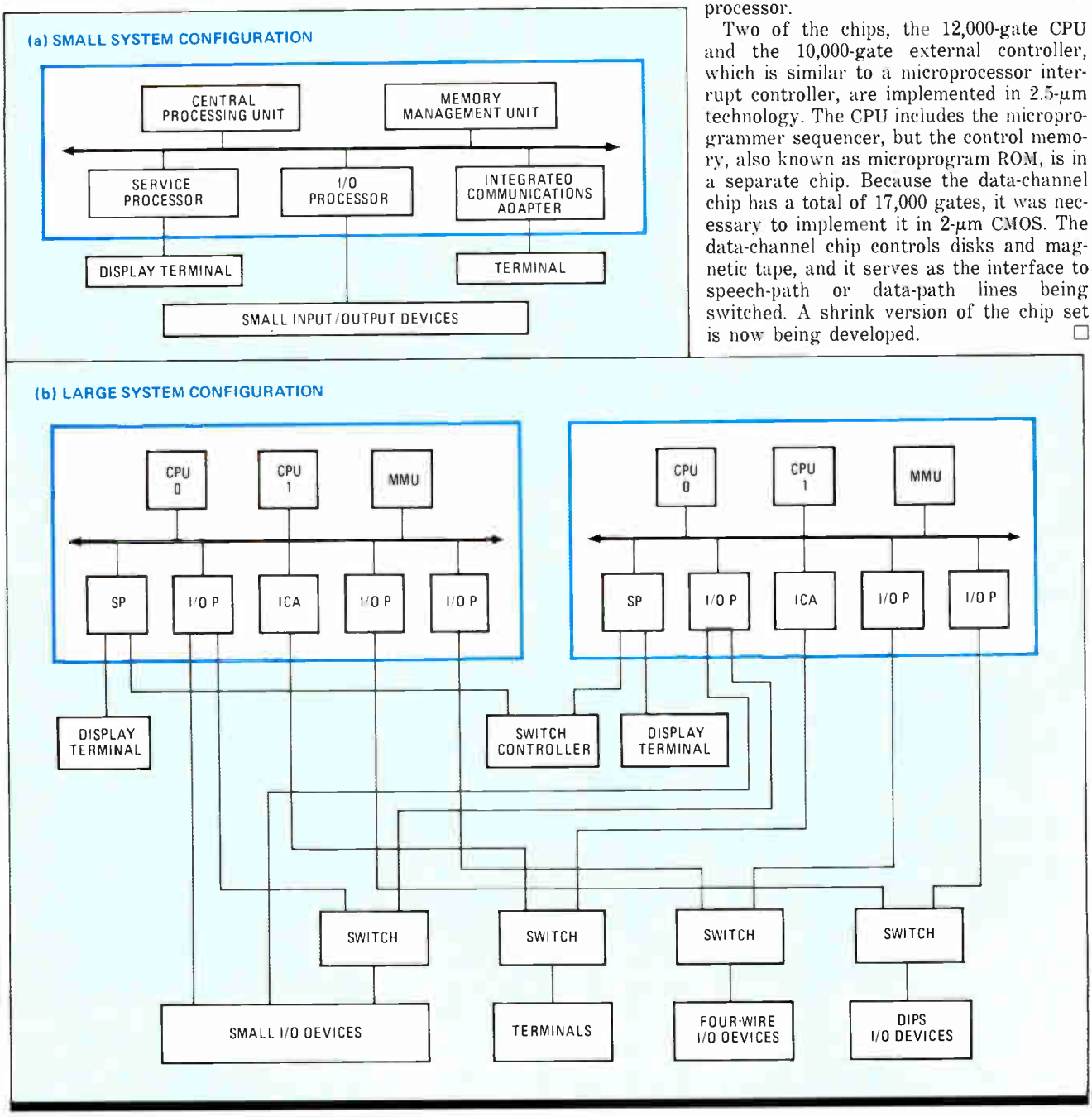
Since this year's conference, the V30, a new chip with 70,000 gates, has been developed for improved performance. It will be used commercially later this fiscal year, which started April 1. DIPS-V30 will be the smallest system in the enhanced DIPS-11/5E series announced in October 1985. The V30 chip uses a near n-well version of twin-tub CMOS technology with 1.3-μm design rules, Hitachi's mainstream lithography process, to enable it to fit on a 13.9-by-13.9-μm chip. Tungsten polycide is used for gates to decrease the delay of the polysilicon interconnect layer. Cycle time has been reduced from the V20's 200-ns figure to only 120 ns to provide almost double the processing power.

The one-chip V30 has been benchmarked at 0.6 mips in the same banking mix used for the V20. Throughput is more than doubled, even though cycle time is not quite halved, because the single-chip design reduces CPU size from a single board to a single chip for better performance. System size is relatively small: about one cubic meter.

Despite the higher chip density and much higher throughput, the V30's maximum power requirements are only 1 W, compared with 750 mW for the V20. Actually, both chips typically operate at half their maximum power. The V30's I/O processor is a 10-by-10-mm chip with 15,000 gates. The integrated communications adapter measures 9.3 by 9.5 mm and integrates 13,000 gates. Further details of the V30 system are not available.

NTT's DEX D70 digital switch was originally implemented in ECL 10K master-slice chips but is now produced in a three-chip CMOS family. Because CMOS could not match bipolar performance and throughput could not be reduced, a multiprocessor configuration has been adopted for function sharing. Load sharing is provided by a supervisory processor.

Two of the chips, the 12,000-gate CPU and the 10,000-gate external controller, which is similar to a microprocessor interrupt controller, are implemented in 2.5-μm technology. The CPU includes the microprogrammer sequencer, but the control memory, also known as microprogram ROM, is in a separate chip. Because the data-channel chip has a total of 17,000 gates, it was necessary to implement it in 2-μm CMOS. The data-channel chip controls disks and magnetic tape, and it serves as the interface to speech-path or data-path lines being switched. A shrink version of the chip set is now being developed. □



4. TWO SIZES. NTT Corp.'s 32-bit DIPS processor chip provides arithmetic and control functions for a small on-line system (a) or a larger distributed configuration (b) that might be used in a banking network system.

PROBING THE NEWS

LARGE-SCREEN DISPLAYS GET BIGGER AND BRIGHTER

LOOK FOR MODULAR MODELS, BETTER PROJECTION TV, ELECTROCHROMICS

by Jesse J. Leaf

SAN DIEGO

The common thread in most display research and development is the drive to make screens bigger and brighter. And that trend was certainly demonstrated last week at the Society for Information Display Symposium in San Diego. Getting big play were late developments in large-screen display technology ranging from giant modular displays to brighter projection TV and higher-visibility electrochromics.

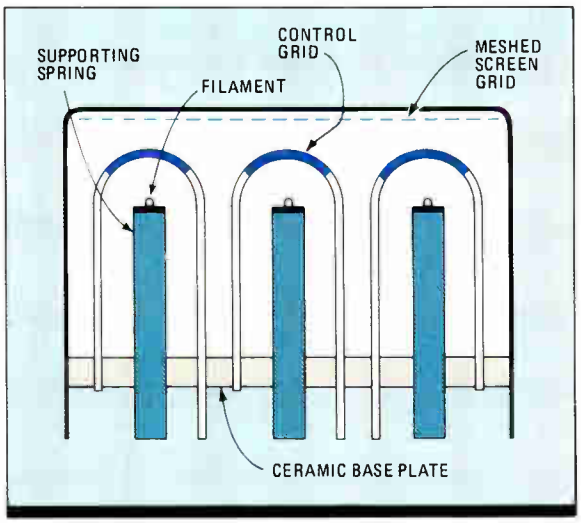
Large-screen usually defines those displays that measure 40 in. or more diagonally, and most commercial applications have been for such uses as projection TV in the home. But based on the development work now going on in such places as the U. S., Japan, and China, it appears that a bunch of exotic new uses are coming—giant electronic billboards and conformable liquid-crystal signs, for example.

Perhaps the most exciting big-screen development at SID was modular displays. An entire session was devoted to them and their potential to bring moving displays to the billboard market. "This is recognition that modules solve many of the problems commonly associated with large-size displays," particularly poor resolution and low brightness levels, says session chairman Milo Johnson. A planner at Texas Instruments Inc.'s Dallas Research Laboratories, Johnson says that by putting together display building blocks in rows and columns, it is possible to build, within practical limitations, arbitrarily large panels using any display technology. In most cases, he adds, overall costs would be lower than for a monolithic approach.

Sony researchers are developing a commercial version of what many called the most striking modular display ever built. That was the company's experimental Jumbotron, an outdoor video display measuring almost 160 ft diagonally. The commercial version will measure up to 20 meters wide. Composed of 151,200 color cells with three rectangular phosphor pads, the original giant screen was built for the 1985 Tsukuba science and technology exposition [*Electronics Week*, Sept. 3, 1984, p. 30] and could be seen in daylight from as far as 1 km.

As they scaled down the Jumbotron, Sony researchers found the original pixel pitch—100 mm—wouldn't give them adequate resolution for screens about 20 m wide. So they set about to design a new lighting device capable of high resolution on "small" screens and came up with the TL-8, which is composed of 8 pixels with a pitch of 22 mm.

The smaller pitch made it impractical to build all of the low-voltage electrodes on lead frames as was done on the Tsukuba unit, however, so a low-voltage electrode block corresponding to respective triplets was designed (figure). Filaments and control grids are mounted on a ceramic base and covered with a box-shaped second grid. The control grids are bent into concentric semicircles to cover the wire filaments, and a meshed screen forms the aperture for the electron beam. This grid curvature enables the electron beam from the wire filament to be distributed uniformly.



SMALL BROTHER. Sony's 20-m version of its Jumbotron uses bent control grids covering wire filaments.

The color-pad arrangement, chosen by computer simulation, is blue, red, and green from left to right—the red had to be bracketed in the triplet or a halo would have formed around images. The eight pixels are arranged in two rows of four, and the rows are lit alternately by driving their filaments of the rows at 120 Hz. Each control grid is operated independently to select the colors and brightness. The display screen is built up of modules consisting of 32 of the lighting devices, four in a row and eight in a column.

Chinese display makers also have modules in mind for big, relatively inexpensive big-screen displays. At SID, researchers from the Changchun Institute of Physics in Jilin, China, described two similar EL devices—one using ac, the other dc. The displays are identical—30 modules arranged into five rows of six columns—measuring 3 by 2.5 m. Each unit is a 24-by-24-dot matrix, the pixels measuring 5 by 5 mm.

What is different about the two is the phosphor composition. The luminescent layer of the ac EL display, or ACEL, is composed of zinc sulphide, copper, and bromine. The phosphors of the dc version, or DCEL, are made with zinc, magnesium, and copper. The Chinese researchers developed a capacitor-forming technique to decrease capacitance and therefore improve brightness and contrast of the DCEL matrix panels. They found that thickness of the phosphor layer had no effect on capacitance, but it decreased when they increased the forming voltage and time, as well as the temperature.

GREEN DISPLAY. One interesting aspect of the ACEL was the choice of color display. Using a color theory developed in China, they chose a green color as the optimal chromaticity coordinate for the lighting conditions under which the pan-

el will be viewed—in this case, the Great Hall of the People in Beijing.

SID showed that interest is still high in one of the oldest technologies, TV projection. "Manufacturers believe it is an important part of future business," says William P. Bleha, assistant program manager for projection displays at Hughes Aircraft Co., Carlsbad, Calif. "One reason is high-definition TV. It will be some time before hi-res gets to the home, but manufacturers expect an earlier payoff. The other reason for the continuing interest in projection TV is that it looks like it has the potential of revolutionizing the movie industry—both in production and viewing."

Tektronix Inc. has addressed itself to the problem of projecting high-resolution pictures while maintaining high brightness levels—what the researchers call "disjoint requirements." They maintain that the most common and successful method is to converge three light valves in the manner of projection CRTs, and they have constructed a color projector that houses three converged liquid-crystal light valves that use transmissive refractive optics without schlieren stops or polarizing beam splitters.

THREE VALVES. The projection optics harnesses three liquid-crystal light valves in an in-line configuration. A 400-W metal halide lamp provides illumination. The light is separated into red-green-blue components by crossed dichroic beam splitters, which then pass through various lenses to condense the image and provide uniform field coverage. It is then polarized, modulated by the liquid-crystal cell, and then passed through a crossed Polaroid Corp. HN 38 analyzer (polarizer) and projected to the screen.

Seiko Epson Corp. has taken a different approach to solving the major drawbacks of conventional CRT projectors—expense, lack of brightness, and need for precise adjustment—with an inexpensive projection LCD that uses three small thin-film transistor LCDs and simple optics. The researchers claim the projector can be made to be no larger than a portable 35-mm slide projector.

The main components of Seiko's projector (figure) are a halogen lamp with a color temperature of 5,000 K, two dichroic mirrors, three liquid-crystal light valves, one dichroic prism, and one projection lens. The light from the lamp is separated into red, green, and blue beams by the dichroic mirrors, and each passes through the corresponding liquid crystal cell. The cells act as light valves to control the transmittance of each beam; the prism synthesizes the beams to form an image on one optical axis through a single projection lens.

MAIN FACTOR. The most important element in this system is the light valve: it is the main factor that determines image quality. All the driver circuits for X and Y are integrated by the polysilicon thin-film transistors on the same substrate where the matrix elements are fabricated, accounting for the projector's compact size and low cost.

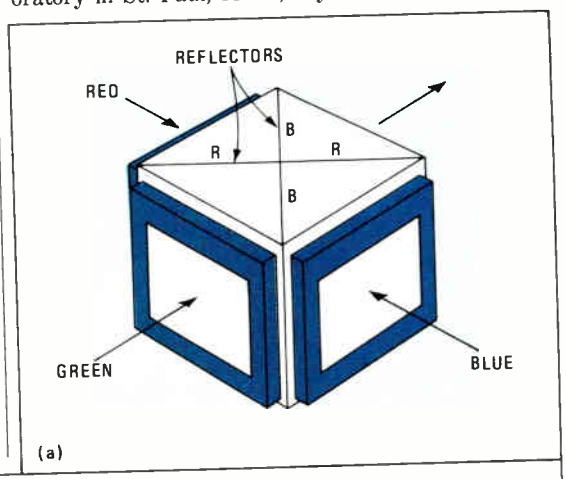
William A. Huffman, research manager of 3M Co.'s Corporate Research Laboratory in St. Paul, Minn., says he sees a huge appetite for conformable electronic special-purpose signs; he sees this appetite as the engine for developing new technologies in the field, especially in liquid crystals.

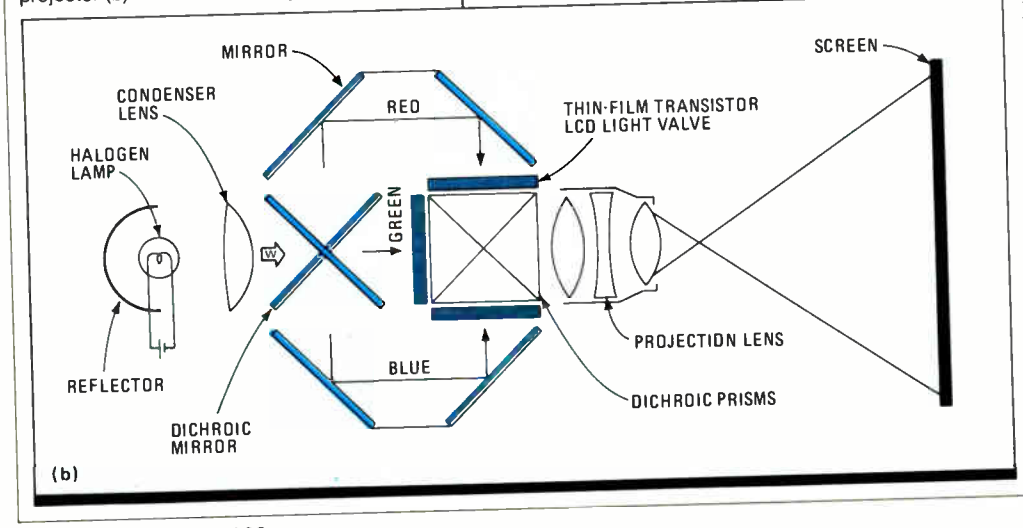
"People in the LC science are beginning to understand the materials, the physics, and their surface characteristics as they work toward high-performance systems," he says. As an example, he cites Hitachi's work in highly twisted birefringent devices with applications in high-resolution, larger-area CRT displays. Another exciting advance, says Huffman, is a method of microencapsulating nematic liquid crystals in an index-matching binder and sandwiching them between conductivity-coated Mylar films. This is a big step toward cheap, large-scale signs, says Huffman.

Research has also been going on since the late 1960s on electrochromics, a technology that has had little commercial success. Despite the disappointment with electrochromics, which once were considered a potential replacement for LCDs [*Electronics*, April 21, 1982, p. 76], work is continuing, and there has been progress in materials and fabrication. At the SID Symposium, researchers from the Asahi Glass Electronic Products R&D Center Co., Yokohama, Japan, reported on an electrochromic display that they said has several advantages over LCDs, such as excellent visibility in sunlight and long-term open-circuit memory. The major drawback in these displays is that the response time gets slower as the operating area gets larger.

Asahi is working on a large-area dot-matrix electrochromic display that it says has a sufficiently short response time to allow commercial application in large-area public-information displays. Its engineers accomplished this by replacing the indium tin oxide lead electrode with a more conductive material.

To those who question which of the many developing technologies will gain prominence, 3M Co.'s Huffman says "I think people have begun to realize that there is not one universal technology. There is a wide range of applications—from outdoor public information displays that can have a screen diameter of several meters down to anything larger than desk top CRTs. There's a lot of room for discovery." □





LIGHT SPLITTER. A dichroic prism (a), which eliminates the seam of quad dichroic mirrors, is the major component of Seiko's liquid-crystal projector (b). LC cells act as light valves.

CUSTOM IC MEETING IS TURNING INTO NEW PRODUCT SHOWCASE

GOULD/AMI, NATIONAL, AND TEKTRONIX TO MAKE MAJOR ANNOUNCEMENTS

by Bernard Conrad Cole

ROCHESTER, N. Y.

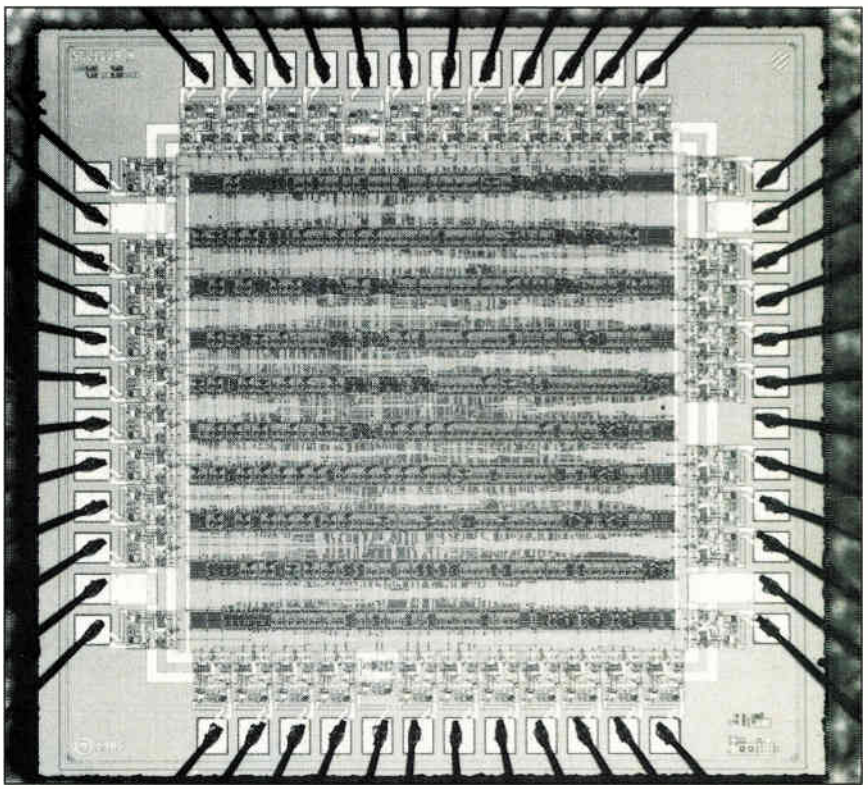
As the premier conference for gate-array and standard-cell designers, the annual Custom Integrated Circuits Conference is fast becoming the stage for companies wishing to showcase their new custom and semicustom products and technologies. This year's conference will be the scene of major announcements from such companies as Gould/AMI, National Semiconductor, and Tektronix. During a three-day run this week in Rochester, advances in process technologies—particularly gallium arsenide—and in paring design turnaround times will be discussed.

Gould/AMI, Santa Clara, Calif., will introduce an expert system that for each design compiles cells and generates complete circuit layouts, documentation, and data-base descriptions. Called Score, it allows designers to automatically generate data for new cells based on the customer's performance requirements, eliminating the customer's dependence on an IC vendor's library of standard cells. According to the company, Score can create custom cells because the cell-simulation model and mask layout are not prestored in a data-base library, as is done conventionally for standard-cell circuits and gate arrays.

The Score cell-library development system was created using artificial-intelligence techniques, says Gould/AMI vice president Bruce Bourbon. In constructing a circuit with Score, a designer uses spatial-relationship reasoning to achieve the most space-efficient layout. The Lisp-based software tools retain the steps of human reasoning of spatial relationships and use them to create other designs.

Separate papers at the conference describe three of the Score AI-based software tools: an expert silicon compiler called Descart; a cell-generator system based on spatial reasoning; and a software tool set for manipulating circuit designs that uses precedent-based reasoning.

While Gould/AMI's Score moves the customer away from a standard-cell library, National Semiconductor Corp., Santa Clara, Calif., will announce its formal entry into the standard-cell business. It has completed work on a library of fixed-height cells and functional blocks, advanced development software, and design-center support for customers. Fabricated using the company's 2-μm microCMOS process (figure), the SCL (for standard-cell library) includes 150 cells in the initial offering. This will be expanded by an additional 100 standard cells by the end of this year.



NEW FAMILY. National Semiconductor Corp. is announcing its entry into the standard-cell business with its SCL family, which includes an advanced logic simulator.

Included in the package's development tools is a key piece of software called Newton. This advanced logic simulator has a predicted accuracy of 95% to 99%, versus the typical 20% to 50% accuracy of conventional techniques, according to National. The simulator's key elements are its ability to model multiple paths within a gate and the delays associated with the input signals, a parameter not included in current offerings.

The significance of this technique is that the Newton package does not have to perform a further device-level simulation to achieve higher accuracy, as other products must. This means that timing problems can be detected at the simulation stage rather than at the silicon stage, says National, thus eliminating discrepancies in testing and logic simulation results.

BEYOND SOFTWARE. Gate arrays will also be unveiled at the conference. Tektronix Inc. will announce the availability of the QuickChip 4 bipolar array (figure, p. 50), a predesigned array that mixes analog and digital functions on the same IC using a high-frequency gigahertz-range bipolar process. The array combines high-speed, medium-voltage capabilities with typical npn transistor cutoff frequencies approaching 6.5 GHz for the analog portion and up to 0.5 GHz for the digital. The digital portion of the array consists of an emitter-coupled-logic gate array with 300 equivalent gates incorpo-

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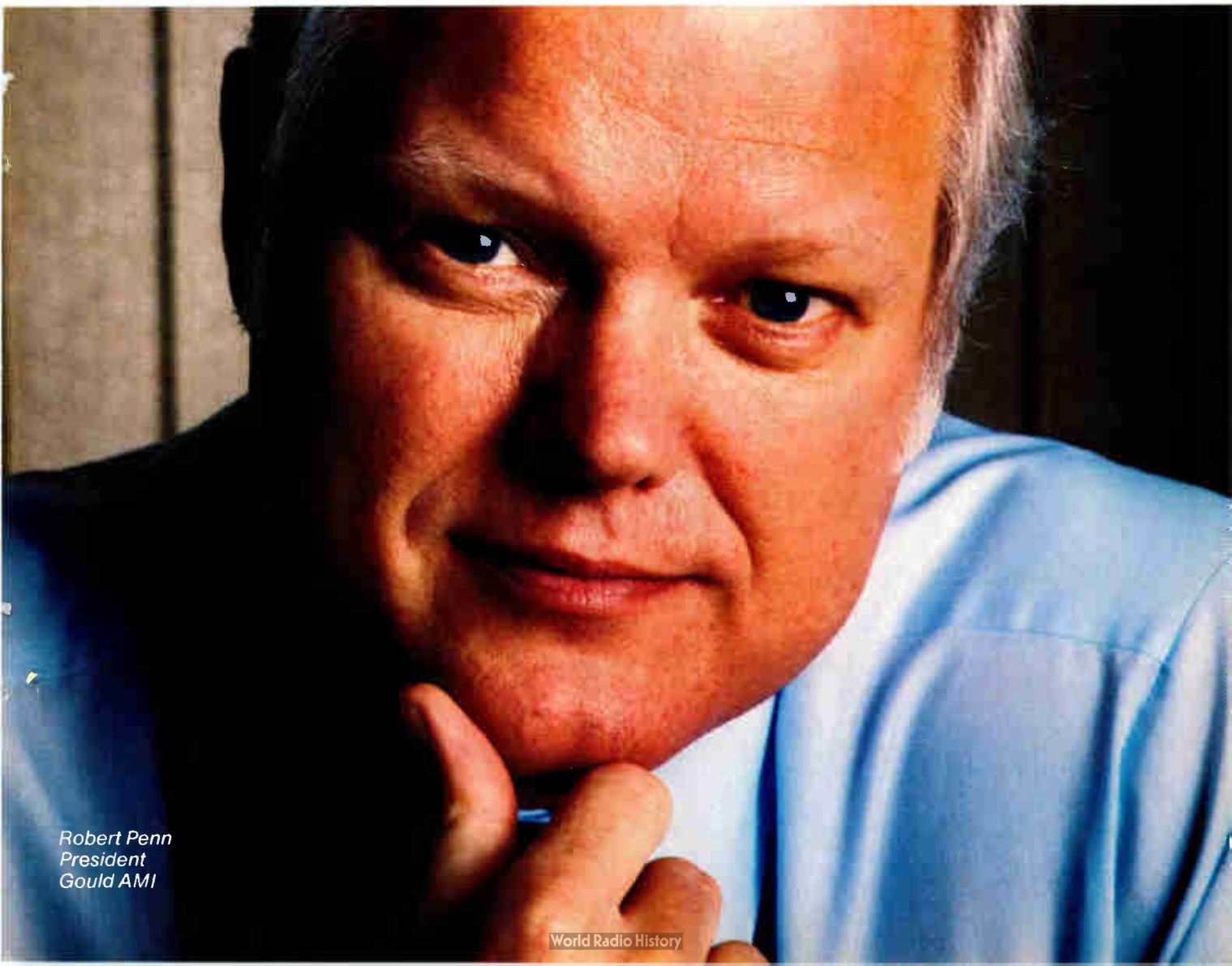
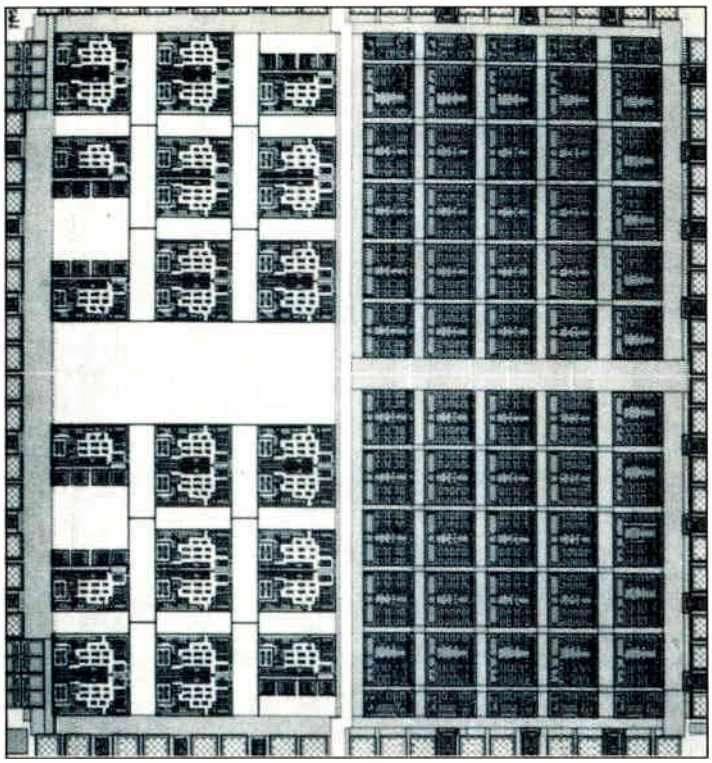


Robert Penn
President
Gould AMI

rating functions such as AND, OR, NOR, and NAND, multiplexers and decoders, buffers, latches, inverters, and TTL interfaces. The analog portion consists of a total of 360 transistors and passive components.

Process technology at this year's conference will focus on achieving high-performance arrays using silicon bipolar ECL, mixed-process biMOS and biCMOS, and gallium arsenide.

Many of the conference papers will come from GaAs circuit designers. Ford Inc. Microelectronics, Colorado Springs, has developed an array of 500 four-input NOR gates, fabricated with a process-tolerant, high-noise-margin, depletion-mode metal-semiconductor FET GaAs design compatible with silicon bipolar ECL levels and supplies. It features loaded gate delays of 250 ps and dissipates only 2 mW/gate.



COMBINATION. Tektronix' QuickChip 4 IC is a high-speed, high-performance bipolar array for integration of analog and digital functions on one die.

Pushing performance even further, engineers from Gigabit Logic Corp., Newbury Park, Calif., will describe a prototype GaAs array designed using capacitor-diode FET logic. The company used it to fabricate a 19-state ring oscillator with gate delays as low as 76 ps and a power dissipation of 1.8 mW/gate.

Aiming to reduce power dissipation, designers from Honeywell Inc.'s Systems and Research Center, Minneapolis, have fabricated a 2,000-gate GaAs array using Schottky diode FET logic (SDFL) with power dissipation as low as 73 mW/gate at a gate delay of 1.3 ns. Using a variation they call bootstrapped SDFL, they report a capacitive drive capability of 1.6 ps/fF at 240 mW/gate.

Looking for ways to reduce GaAs design-to-prototype time, engineers at Triquint Semiconductor Inc., Beaverton, Ore., have developed a standard-cell library using buffered FET logic. The cell library includes gate-level cells as well as ECL, TTL, and CMOS interface cells, with a range of performance and power configurations. Using the family, the designers have fabricated a line of GaAs counters with frequencies ranging from 1 to 3 GHz.

In silicon bipolar ECL, designers from NEC Corp., Kawasaki, Japan, have fabricated a 540-gate array with 100-ps unloaded gate delays and a power dissipation of only 5.78 mW/gate, eliminating the need for forced-air cooling systems used in present bipolar ECL designs.

From NTT Electrical Communications Laboratory, Kanagawa, Japan, comes a novel 7,000-gate master slice that combines high-speed nonthreshold logic gates and low-power current-mode logic using a 1-μm design-rule superself-aligned process technology. Typical gate delays are 50 ps at 2.3 mW/gate for the nonthreshold logic gates with toggle frequencies of 2.6 GHz at 5.2 mW/cell for the circuit's current-mode logic.

MIL-SPEC. And from VTC Inc., Bloomington, Minn., comes a 350-ps/gate ECL standard-cell library based on an oxide-isolated walled-emitter process with internal CML gates and three levels of series gating. The library, which has a channelless architecture for high densities, is designed for military and aerospace applications and can withstand total radiation doses as high as 10 millirads.

In the mixed-process area, Motorola Inc., Mesa, Ariz., chose the conference for the formal introduction of its 2-μm 6,000-gate biMOS array with an average gate delay of 900 ps and a fan-out of one. Active power dissipation ranges from 460 mW to 1.7 W in the all-TTL mode, with only 0.5 W on standby. And engineers at NEC, using 1.5-μm emitter npn transistors and a 1.6-μm CMOS process, have developed a biCMOS array family with densities up to 3,100 gates.

All the activity in GaAs doesn't mean the conference will ignore CMOS designs, however. Among the many offerings to be detailed are a high-performance 3-μm CMOS analog standard-cell library from Microlinear; a 1.2-μm radiation-hardened CMOS standard-cell library for very high-speed IC applications from VTC; a 700-ps/gate, 100,000-gate CMOS array from LSI Logic; and a configurable 2-μm CMOS megacell/gate-array hybrid that combines a 6845 cathode-ray-tube controller megacell on the same chip as 2,000 uncommitted logic gates from VLSI Technology Inc.

Looking to improve the gate efficiency of their arrays, designers at Mitsubishi Electric Corp.'s LSI Research & Development Laboratory, Itami, Japan, have developed a 1.3-μm, double-metal, CMOS variable-track master slice to eliminate wasted silicon from unused transistors in the macrocells and unused interconnections. Used in the fabrication of a 540,000-transistor device, this technique makes use of chains of pnn channel transistors rather than the pn channel transistor pairs that would be used in a sea-of-gates design [*Electronics*, Sept. 23, 1985, p. 48]. In this approach, small in-channel transistors are used as transfer gates in memory cells as well as in implementing intracell functions.

Regardless of the process technology used, gate-array makers have a continuing interest in reducing the turnaround time on their designs, as reflected in a number of papers at this year's conference. For example, a research team from Bell Communications Research, Morristown, N. J., makes use of a laser-programming technique and a maskless metal-link technology (see story, p. 20).

In a second approach, Hughes Research Laboratories, Malibu, Calif., uses focused ion-beam microsurgical techniques to customize circuits. Usable with both bipolar and CMOS devices, the technique involves breaking an interconnection by simply milling a trench through the conductors.

Looking for ways to increase the reliability and the yield on its CMOS master-slice arrays, designers at Fujitsu Laboratories Ltd., Atsugi, Japan, have developed a 30,000-gate device with built-in self-test circuitry. In the self-test circuits, a pseudorandom pattern generator and a pattern compressor operate in one of three modes: 32-bit pattern manipulators, 16-bit pattern manipulators, and 32-bit shift registers. An on-chip counter is used as an address controller for those portions of the master slice devoted to memory. □

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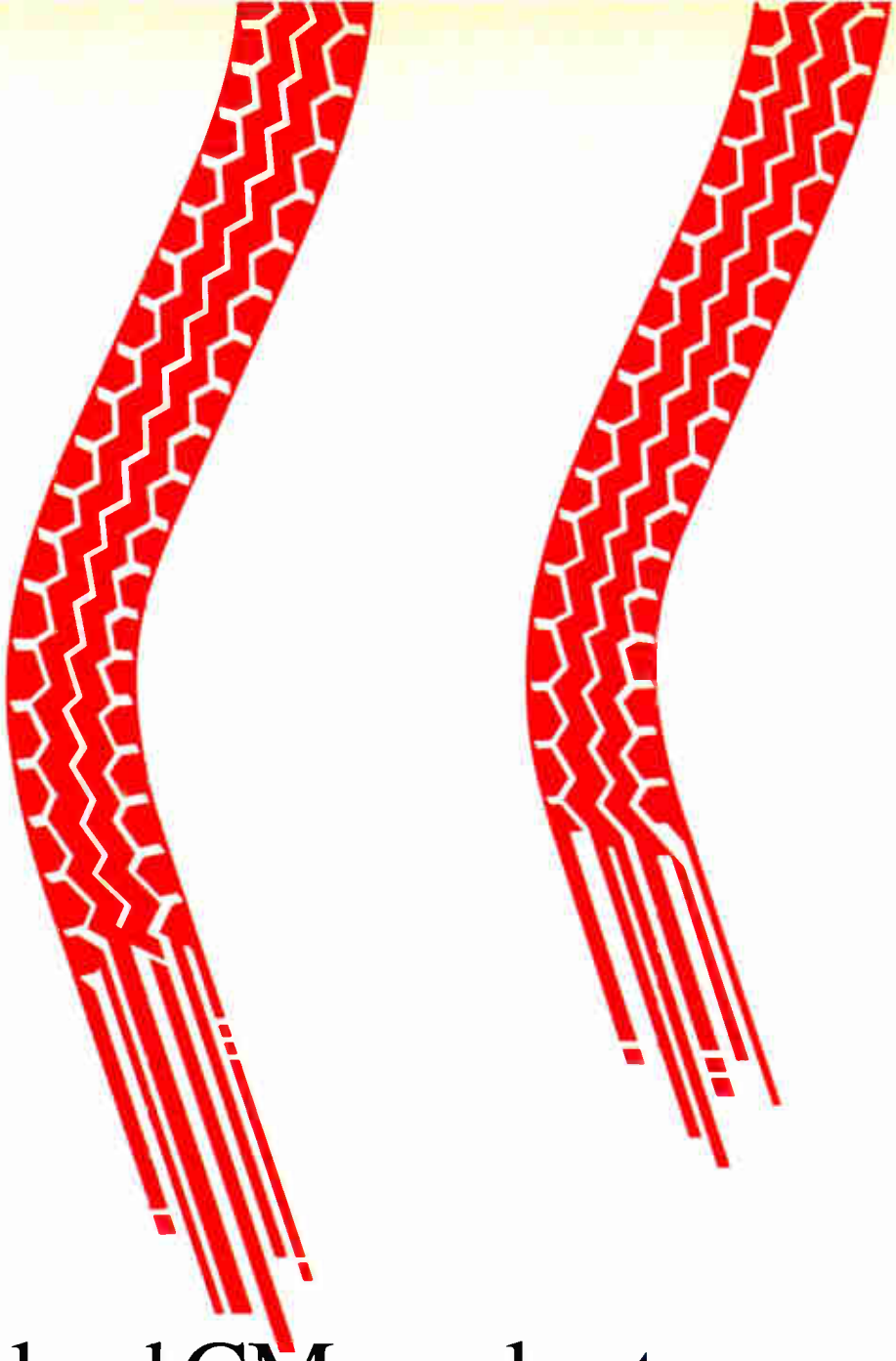

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IN THE U.S., ELECTRONICS CAN PREVENT A CHERNOBYL

NUCLEAR PLANT OPERATORS HAVE LEARNED THEIR LESSON

by Howard Wolff

NEW YORK

The big question in the wake of last week's nuclear reactor diasaster at the Chernobyl plant in the Soviet Union was: "Could the same thing happen in the U.S.?" Anything is possible, but a comparable catastrophe is not as likely and would be controlled faster because the U.S. plants have far better electronic systems.

Comparisons are still difficult because Soviet officials veiled the Chernobyl accident in secrecy. "We don't know what was the initiating event [at Chernobyl], so it's hard to speculate whether or not it would have been sensed or terminated," says John McAdoo Jr., assistant manager of nuclear safety for the Nuclear Technology Systems Division, the section of Westinghouse Electric Corp.'s Power Systems business unit in Pittsburgh that manufactures reactors.

Electronic control at Chernobyl, or lack of it, is emerging, however, as a key ingredient as the Soviets continue to struggle to bring the reaction under control. Experts from industry and government say that Soviet nuclear plants have neither the redundant electronic safeguards nor the degree of electronic sophistication found in U.S. plants.

McAdoo points out that Americans learned the value of electronic controls, complete with redundancy and backup systems, from two accidents—the one at Three Mile Island (the Metropolitan Edison Co. plant) in Middletown, Pa., and the other in 1980 at the Browns Ferry Nuclear Power Station in Decatur, Ala. Since then, he says, a good deal of work has gone into nuclear plant electronic controls and control-room technology.

REVOLUTION. The display and analysis of data is one area in which there has been what McAdoo calls a "revolution." This involves new microprocessor-based systems that can analyze data and provide graphics with more detail to plant operators when a problem occurs. Such an improvement could have gone a long way toward preventing the accident at Three Mile Island.

There, McAdoo says, the shutdown system worked well, but the problem was human error. The operators shut down some things that actually should have been left running, he says, because they had more data than they could cope with. "The operators were faced with a surplus of data that was beyond their ability to assess."

When a nuclear plant problem occurs, "you can get literally hundreds of systems alarming," explains McAdoo, which results in reams of data being spewed out. Under the old approach, the philosophy was to highlight information from the first system that sounded an alarm. But Three Mile Island showed that speedier and more thorough analysis was needed together with systems that can better present the pertinent data to plant operators.

Since 1979, McAdoo says, "a lot of progress" has been made in development of such analysis capabilities for plant computers and processors. These systems provide information to operators in graphical form on a cathode-ray tube "to give the operator a predigested view of things," instead of just providing data. This technology has gone into most of the newer nuclear plants, though it has not been extensively retrofitted, McAdoo says (see "Where shutdown is automatic," p. 54).

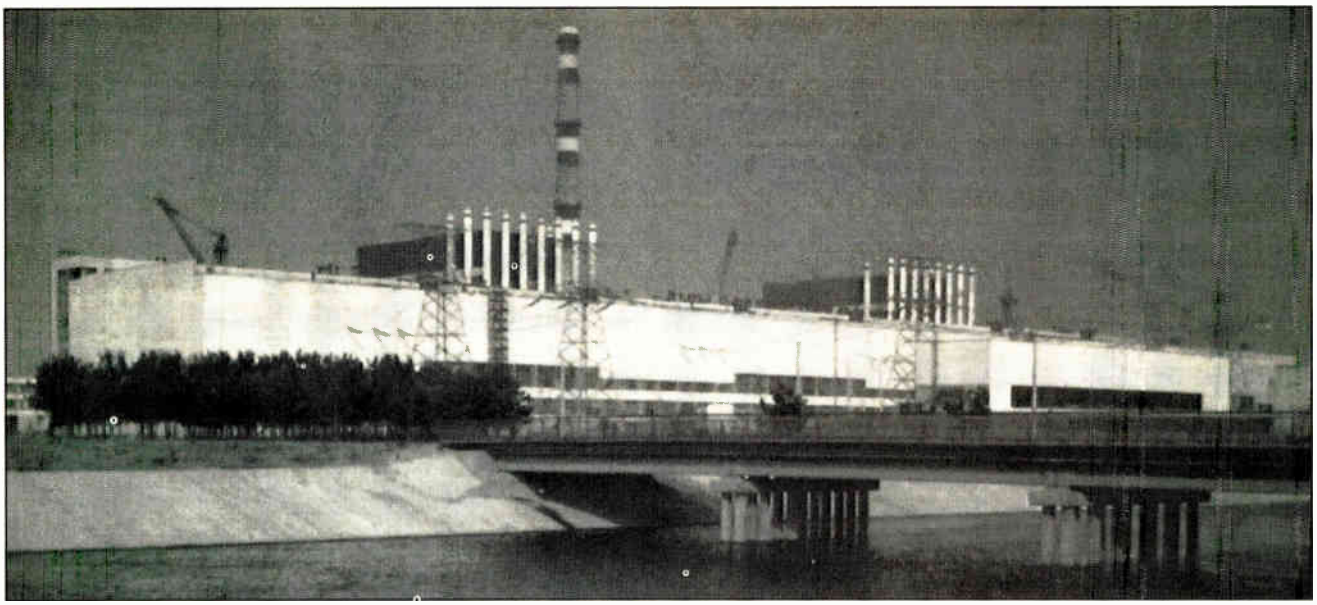
From Browns Ferry, the lesson was a little different. There, the problem was a fire in a cable area that knocked out both channels of a two-channel redundant system that typically carry electronic signals as well as power signals for a nuclear plant, says McAdoo. But with both cable systems knocked out, operators had to take action manually.

Since then, separate channels in redundant systems have become the rule, says McAdoo. Channels A and B must now go through separate traces in which they are physically separated. These new standards are being implemented in new plants and have been backfitted into some existing plants.

Another apparent Soviet weakness is in redundancy. Roger Houston of the Atomic Industrial Forum Inc., an industry lobbying group, says plants there probably lack adequate backups, like emergency cooling systems, for contingencies. "The level of redundancy in the Soviet plants is less than it is here," Houston says. For example, he explains, a Soviet plant may have only one emergency pump or power supply; U.S. plants contain multiple backup systems.

In fact, Houston says, U.S. reactor designers use a "single-failure criterion" required by the Nuclear Regulatory Commission. This means that an emergency system must accomplish its task despite the failure of any single compo-

INSIDE CHERNOBYL. Workers at the Soviet nuclear plant, in the Ukraine, are carrying out maintenance on a reactor.



IN QUIETER DAYS. This view of the Chernobyl nuclear plant was published in a Soviet magazine just three months before the accident there.

nent within that system.

But there is still some disagreement about how well the U. S. systems work. Says Robert D. Pollard, a former staff member of the U. S. Nuclear Regulatory Commission who was in charge of plant safety review from 1970 to 1976, the agency's basic safety philosophy is that the role of plant operators should be oversight and that they should not have to act during the first 10 minutes of an accident—automation should do the job. Pollard is now a nuclear safety engineer with the Union of Concerned Scientists, an antinuclear group.

Pollard maintains that despite that goal, automation is not always all it should be. He says current U. S. plant designs do have automated control systems to, say, withdraw fuel rods. But he says there has not been a very high level of reliability in such systems: the control systems respond to too many false alarms. "Automation is good if its accompanied by reliability," he notes.

Furthermore, Pollard claims, no new automated control-system technology has been added to U. S. reactors since Three Mile Island in 1979. Some plants now have training systems such as plant-specific simulators, but he sees nothing new to actually help operators cope with an accident. "The level of automation in terms of safety varies considerably depending on the manufacturer," he concludes.

John Kemeny, professor of mathematics and computer science at Dartmouth College and chairman of the presidential commission that investigated the accident at Three Mile Island, believes that the recent upgrading of display and analysis equipment should have been done sooner. He maintains that the automation technology at Three Mile Island was inadequate and says that obsolete computer equipment played a key role in the accident because it reacted too slowly.

Kemeny, quoting the U. S. Nuclear Regulatory Commission, says the reactor's computer technology was 20 years old at the time of the accident. "Today, a personal computer could handle what we [the presidential commission] recommended"—systems that process more data faster.

Displays available to U. S. plant operators are still inadequate, Kemeny says. At Three Mile Island, he says, a computer that could handle thousands of alarm signals simultaneously could have easily analyzed the hundreds of signals generated during the accident and could have displayed them in order of priority to operators.

The Chernobyl disaster promises to spur development of more reliable and quicker-acting safeguards. In the case of Westinghouse plants, says McAdoo, much of the research and development is done cooperatively with funding by nuclear plant users' groups—each of the major vendors has one. McAdoo estimates that funding from Westinghouse users—71 Westinghouse-built plants are in operation, 40 of them in the U. S.—for the new data display and analysis work totaled about $2 million to $4 million, which includes some other projects.

Those numbers can be expected to increase because, as one industry insider puts it, "This thing will have us under the microscope for quite a while." □

Reporting was provided by Wesley R. Iversen and George Leopold

WHERE SHUTDOWN IS AUTOMATIC

Throughout the U. S. nuclear power industry, redundancy of sensing, instrumentation, and control is the requirement. Typical of U. S. plants is San Onofre, just south of San Clemente, Calif., about halfway between Los Angeles and San Diego. There are three units—a 48 MW opened in 1968 and two 1,180 MWs that went on line in the early 1980s.

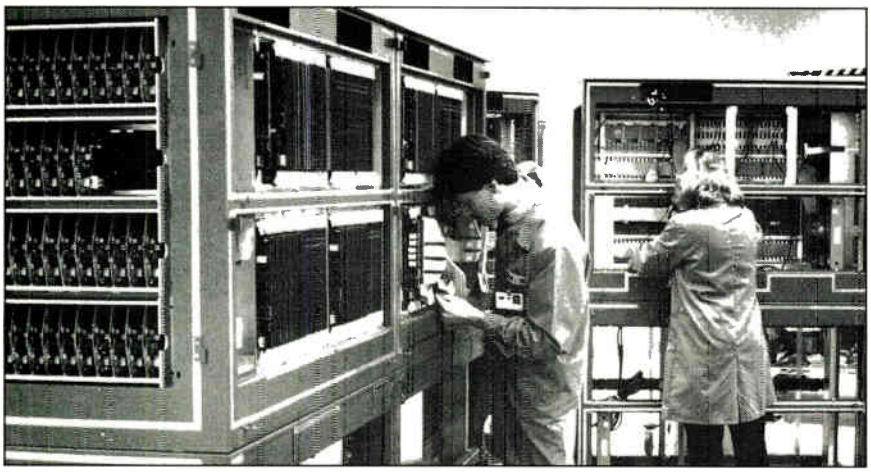
The key reactor protection system has four independent channels for sensing and shutting down. It is under 32-bit minicomputer direction, also with redundant backups; if any two of the channels register a problem, the reactor shuts down at once. Richard M. Rosenblum, manager of nuclear safety, says the sensing and actuation speed is about 300 ms for automatic shutdown of the reactor or any parts of the facility, such as pumps, valves, or coolers. Some of these mechanical functions take as long as 10 seconds to complete, however.

To shut down the reactor, control rods are dropped into it, a process that gravity takes about 3 seconds to complete. By contrast, the Soviets at Chernobyl depended on electric motors that pulled up control rods. "Big difference," as Rosenblum succinctly puts it.

He says he has read descriptions of the process that have been published by the Soviets and emphasizes that their control hardware, sensors, and instrumentation components and computers themselves are of proven reliability, and are tested over and over. Some are still based on mid-1970s designs but are updated constantly, he says. *–Larry Waller*

VMX GIRDS FOR A FIGHT IN MARKET IT PIONEERED

MANUFACTURER OF VOICE-MAIL EQUIPMENT HOPES TO KEEP ITS LEAD AS BIG COMPANIES MOVE IN



FIGHTING. VMX thinks new products will help it in the voice store-and-forward market.

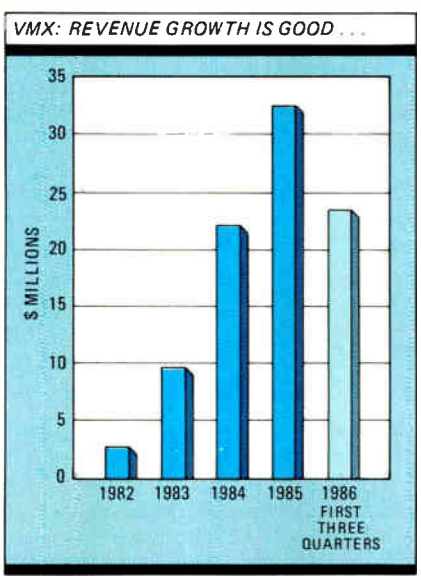
RICHARDSON, TEXAS

Survival for many a startup company in the electronics industry has often meant carving out a market for its new products, then trying to avoid being trampled as larger companies move in to take control of a growing business. Life has been that way for VMX Inc. The company, which pioneered digital voice-mail technology, now must fight off the likes of AT&T, IBM, Northern Telecom, and Wang Labs to hold on to the market lead.

Even though VMX still claims half the market, it is fighting a year of disappointing results. Because the growth rate has slowed in this market, the company's current fiscal year is shaping up as an unprofitable one. But VMX has launched a strategy that management hopes will enable the company to hang on to its share in 1987, when the market moves into a brisk annual growth rate of 50%, says president W. Dal Berry. His strategy includes building on the company's market leadership, developing new distribution channels, and pushing research and development to turn out next-generation products. Berry also has up his sleeve a bundle of patents filed years before the market existed.

Competitors in the business for voice store-and-forward equipment are chasing what they still claim could be a $1 billion-plus market by the mid-1990s. The battle is now being fought in the private-branch-exchange arena as PBX suppliers enhance their systems with the ability to store and forward verbal messages. Voice messages, which are digitized and compressed for storage, usually can be forwarded to any telephone exchange.

The market-share race is dead even between VMX and Rolm Corp., the IBM Corp. telecommunications subsidiary, says Probe Research Inc. The Morristown, N.J., market watcher estimates each company had about 20% of 1985's total $145 million in equipment sales. VMX officials, though, note that Probe includes dictation machines that digitize and store voice inputs but cannot forward them by telephone. If that category is removed, they say, VMX and IBM are in a dead heat but with only 40% of the business. Probe says the market it watches will double in 1986.



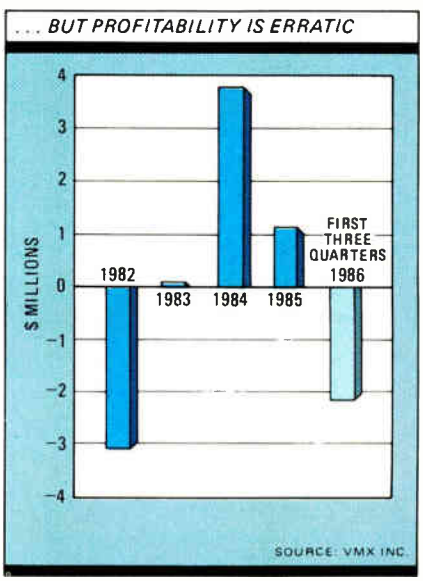
"VMX was the first real company in this industry," says Bill Spain, director of voice-technology analysis at Probe Research. "They knew how to market the concept and had the most advanced system. Therefore, they dominated the market early on, particularly in doing business with Fortune 1,000 companies. But two things have happened since those early days," he adds. "Other companies have come out with smaller, cost-effective systems and some, perhaps, might have improved the user interface. And while the market has been growing at a healthy rate, VMX has been a bit stagnant."

VMX, which began life in 1978 as ESC Communications Inc., still believes it has an inherent advantage of being first in the market. A number of top U.S. executives are hooked on their own use of VMX's system. Worldwide, VMX claims to have over 300 systems installed, serving 600,000 users.

"Our basic premise is that if we are the market leader and we continue to grow as fast as the market—even when all these other companies come into the race—we won't lose," says Berry, who was recruited from Xerox Corp. in 1982 by VMX founder and chairman Gordon H. Matthews. But after three profitable years, VMX is trying to battle its way out of a loss-ridden fiscal 1986.

In the first three quarters of fiscal 1986, which ends June 30, VMX lost $2.2 million on revenue of $23.6 million. In the same period last year, it earned $801,000 on revenue of $22.9 million. Berry expects a slight profit in the fourth quarter and that VMX will be profitable in fiscal 1987.

Company officials blame the stalled growth on a general slowdown in corporate capital spending during an uncertain economic period. The voice-mail market, now closely tied to PBX sales, also suffered from a slump in deregulated U.S. telecommunication markets,



adds Berry. But he expects industry growth to return to 50% in 1987.

"We have decided that we are not going to force a profitable short-term quarter. The investments we are making in research and development and our efforts to establish distribution channels are the right long-term investments," he adds. VMX has signed Ameritech, Nynex, Southwestern Bell, U. S. West, and Xerox as distributors. VMX voice-mail systems are also being integrated into PBXs from GTE, InteCom, Northern Telecom, and Siemens.

Those are powerful allies. But competition for voice-mail revenues is building fast. Northern Telecom is expected to begin selling its own voice-mail products embedded in its digital Meridian PBX product line this summer. Rolm is also stepping up its voice-mail marketing efforts. Rolm is adding to its PBX some user-interface features previously designed into IBM's original Audio Distribution System, which was introduced in 1981 when Big Blue first stepped into the embryonic voice-messaging business. And AT&T Co. is putting its Audix integrated voice-messaging features into its System 85 PBX.

VMX chairman Matthews believes the competition will have difficulty knocking his company out of its installed base. "The thought is to install systems at the headquarters and get the president, chairman, and staff using the system," Matthews says. "They are seed accounts. The companies will see it is working and then buy more machines. That is really starting to happen."

PATENT CLAIMS. Also in VMX's corner are a fistful of basic U. S. patents covering many of the fundamentals of computer-based voice messaging that Matthews developed in the late 1970s. The patents have such a tight grip on some of the principles of digital voice mail that VMX has signed licensing pacts with 14 companies, including IBM. The agreements do not transfer technology but let other companies develop systems without infringing on VMX's patents. VMX gets an initial fee of $250,000 and 6% of the ongoing revenue.

"At one time we tried to decide whether or not we wanted to license companies for royalties or whether we wanted to use patents as a defensive weapon to keep people out," recalls Berry. "We made the decision to license the technology because we needed the big guys in the industry if we really wanted it to grow. Outside of those 14 [licensees], we are now aggressively pursuing anyone else who might be infringing on our patents." – *J. Robert Lineback*

BOTTOM LINES

MINICOMPUTER SALES TO GROW 11% IN 1986

The U. S. market for minicomputers and superminicomputers should take a turn for the better in 1986, growing 11% to $2.9 billion from last year's $2.6 billion, predicts Dataquest Inc., the San Jose, Calif., market researcher. These computers, which Dataquest describes as machines that support 21 to 64 users in large corporate departments, generally cost from $75,000 to $250,000. A major factor in the projected 1986 demand is "a growing acceptance of departmental computing in the business environment," according to the Dataquest study. Yet this acceptance is gradual and will mean a lower growth rate in the future. Dataquest sees this market growing at a compound annual rate of 7.4% through 1990.

SILVAR-LISCO ENTERS R&D PARTNERSHIP

Silvar-Lisco, a developer of computer-aided-engineering software, has formed a limited research and development partnership with R&D Funding, a unit of Prudential-Bache Securities Inc., New York. Silvar-Lisco, of Menlo Park, Calif., says the partnership will fund development of an advanced set of software for the front end of the CAE design cycle, including design-capture and logic-verification products. R&D Funding will provide up to $6.2 million in two stages: $2.7 million in the first and $3.5 million in the second.

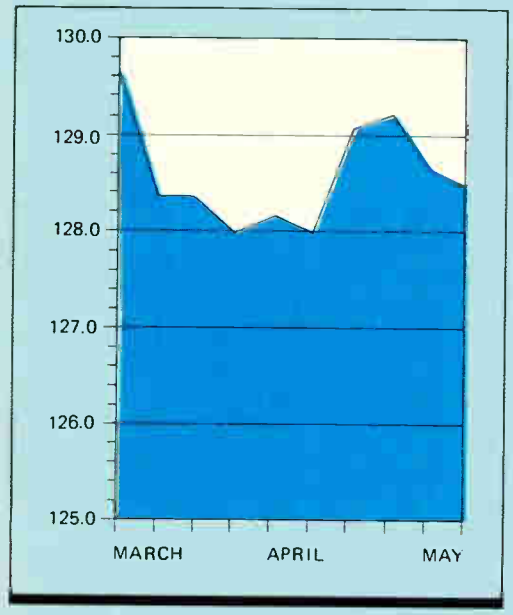
TEKELEC PLANS TO GO PUBLIC

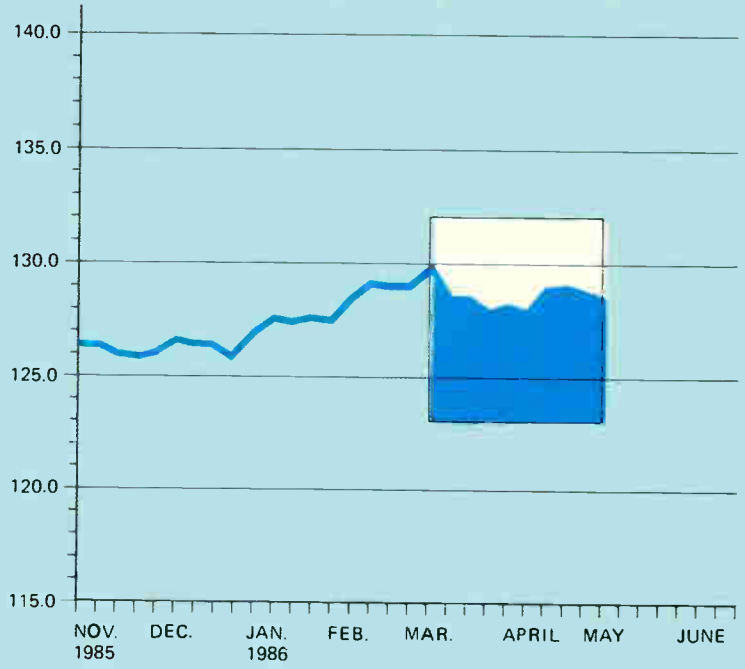
Tekelec Inc. plans to go public by selling 1 million shares of stock priced from $11 to $13 a share. The Calabasas, Calif., maker of test equipment for digital telecommunications devices and networks, says it will offer 900,000 shares of stock; shareholders will sell the rest.

MATSUSHITA BLAMES DOLLAR FOR DECLINE

The falling value of the U. S. dollar took its toll on Matsushita Electric Industrial Co., which is attributing its decline in profits to the sharp appreciation of the yen versus the dollar. The Osaka, Japan, company says its profits in the first fiscal quarter dropped 19%, to $219 million from $271 million, from the same period in 1984. Overall sales fell 8%, to $4.85 billion from $5.3 billion, with overseas sales down 16%, it says. Domestic sales were off just 1%.

ELECTRONICS INDEX





THIS WEEK	= 128.5
LAST WEEK	= 128.7
YEAR AGO	= 127.4
1982	= 100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. ELECTRONICS INDUSTRY EMPLOYMENT

Production workers (thousands)	February 1986	January 1986	February 1985
Office and computing machines	166.5	170.1	197.9
Communications equipment	278.5	282.6	295.8
Radio and TV receiving equipment	56.3	56.4	58.5
Components	344.9	345.0	400.3

February's drop in the production of electronic goods sparked another round of work-force cutbacks as U. S. manufacturers tried to compensate for the still-uncertain demand for their products. The ranks of production workers in the U. S. electronics industry dropped a hefty 0.9% in February, according to the latest government statistics.

The decline made February the 16th consecutive month in which overall industry employment declined. From November 1984 to February 1986, total employment in the U. S. electronics industry has dropped by 13.2%. The drop in employment pushed the *Electronics* Index down 0.2 of a percentage point last week.

The downturn in employment in February comes on the heels of a 1.9% slide in output by U. S. electronics equipment manufacturers [*Electronics*, May 5, 1986, p. 53]. That was the first decline in output in four months. The bad news in the production statistics in February was that for the first time in over a year production output in all industry segments—office and data-processing equipment, communications equipment, radio and television equipment, and components—was down.

The employment report did contain one positive note. February was the first month since last November that reductions in electronics worker ranks did not pervade every sector of the industry. Components manufacturers managed to keep their payrolls just about equal with those of January, with a 0.02% slip in the number of workers. And February was the first month in nearly two years that component producers were not forced to make significant cutbacks in their employment levels. Still, worker ranks in the component sector are down 13.8% from their levels in February 1985.

As large as that drop is, it isn't the largest by far. The number of workers in the office and data-processing equipment sector fell a whopping 2.1% in February. This lowered employment levels in this sector by a huge 15.9% from the February 1985 level.

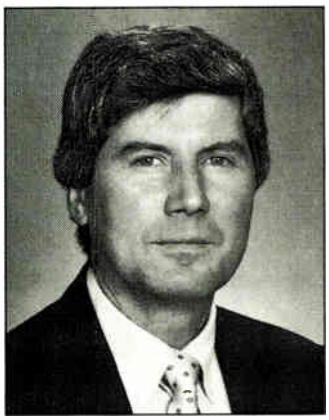
Employment in the industry's communications-equipment sector fared almost as badly as it did in the office-equipment arena. Here, payrolls in February were chopped by a strong 1.5%, pushing employment down 5.8% from what it had been in February 1985. The drop in employment at U. S. consumer electronics companies amounted to just 0.2%, however. And employment among producers of radio and television equipment is still down 3.8% from its levels of a year ago.

TO BALES, TRAINING IS THE WAY TO BEAT JAPANESE

SCHAUMBURG, ILL.

U.S. electronics manufacturers must adopt Japan's training philosophy if they want to beat—or even meet—its low-cost high-quality production levels, says Edward W. Bales. As director of operations for the Motorola Training and Education Center, he is moving swiftly to emulate the successful Japanese formula.

When it comes to continuing employee education, says Bales, "we're still nowhere near the Japanese. They train everybody from the janitor on up to the top managers." The continual updating of employee skills is ingrained in the Japanese culture, he says. U.S. companies are moving in that direction, but need to do more, he believes.



BALES: Inaugurating a new era in training at Motorola.

Bales, 47, has been instrumental in inaugurating a bold new training era at Motorola Inc. that has yielded impressive productivity gains. "In several cases, we've seen a 30:1 return on our training investment," he says. He says that the goal of Motorola's employee training is to better match the company's corporate culture to that of the Japanese. For example, Motorola teaches manufacturing personnel to think more in terms of building quality into a product than throwing out bad parts.

One training program brings together employees from design, manufacturing, quality, marketing, and finance at the start of a product-development cycle. By taking a Japanese-style team approach to product development, Motorola aims to save money and time.

In one case, a team that went through the three-day training session cut the development time on a mobile-radio to only 18 months, Bales says. That compares with 36 to 48 months previously, he notes, and costs came in well below target. Another course teaches managers the coaching skills needed to pass on their knowledge, because "one key role of Japanese managers is to train subordinates."

Much of Motorola's curriculum aims at updating the knowledge and skills of its technical personnel; half of what an engineer learns in school is obsolete only two to three years after he graduates, Bales points out. Beyond engineering, the curriculum also includes programs in management, manufacturing, marketing, and sales.

A 23-year Motorola veteran, Bales has experience in several disciplines—a necessity for the far-ranging Motorola curriculum. The holder of a BS in electrical engineering from the Illinois Institute of Technology and an MBA from the University of Chicago, Bales started out as a design engineer for Motorola's Communications Sector in 1963. He held subsequent jobs in sales and marketing, including management positions, before being named one of three employees assigned to the training center when it was formed in 1980. He was named director of operations last August.

CONCRETE EVIDENCE. Bales can point to concrete and brick as the latest evidence of Motorola's commitment to employee training. Last week, the training operation moved into the Galvin Center for Continuing Education, a new $10 million building in Schaumburg.

The new center is a giant step in the right direction. Named after Motorola's late founder Paul V. Galvin and current chief executive officer Robert W. Galvin, the 88,000-ft² facility contains 12 fully equipped classrooms and a 180-seat auditorium. By next year, robotics and computer-aided-design and manufacturing laboratories will join the half dozen or so labs already in place.

Much more needs to be done, says Bales. Not counting new buildings, Motorola spent about $40 million last year on training. That's less than 1% of the company's $5.4 billion sales, Bales notes. But, he says, most U.S. electronics and computer companies spend much less proportionately on training than does Motorola. *–Wesley R. Iversen*

PEOPLE ON THE MOVE

DAVID L. STONE

☐ Digital Equipment Corp. has promoted David L. Stone from manager to vice president of international engineering and strategic resources. Stone, 44, joined the Maynard, Mass., company in 1970 and has held a succession of management positions, including membership in the corporate engineering staff.

FRANCO SAVOIA

☐ The new chief executive officer for the Arcotronics units of Emhart Corp.'s Electronic/Electrical Group is Franco Savoia, who moves up from vice president and managing director. Arcotronics makes capacitors and capacitor-making equipment for parent company Emhart, a diversified U.S. multinational manufacturer based in Farmington, Conn. Savoia, 48, joined Arcotronics in 1982 after 25 years in engineering and management positions in several European electronics companies.

KUNIO KAKIGI

☐ Victor Company of Japan Ltd. has named a new president, Kunio Kakigi. An engineer who championed research and development of new products rather than refinement of old ones as a basic strategy for survival, the 61-year-old Kakigi will replace Ichiro Shinji, who will become JVC's chairman of the board. Kakigi, a graduate of Tokyo University, joined the company in 1948, rising to general manager of the Color Television Division in 1974 before becoming senior managing director in 1980.

WENDELL C. KILPATRICK

☐ Tracor MBA, San Ramon, Calif., has named Wendell C. Kilpatrick its vice president. The company, a subsidiary of Tracor Inc. operating within the Tracor Aerospace Group, makes countermeasures systems. Kilpatrick joins Tracor MBA from his post as general manager of Wilbur-Ellis Co., Fresno, Calif.

RICHARD P. DONNELLY

☐ Promoted to director of product management for Concurrent Computer Corp., Richard P. Donnelly will be responsible for the planning and management of all computer hardware and software products. He joined the Holmdel, N.J., company (then the Interdata Division of Perkin-Elmer Corp.) in 1974 as a design engineer. Donnelly's most recent position at Concurrent was product line manager for large computer systems.

RICHARD D. PASHLEY

☐ Intel Corp. has appointed Richard D. Pashley general manager of the recently formed EEPROM memory operation, Folsom, Calif. Pashley, 38, moves from his previous position as director of Intel's Technology Development group in Santa Clara, Calif., a post he held for five years.

NEW PRODUCTS

FINDING FAULTS FAST WITH A PC-BASED PACKAGE

SOFTWARE ELIMINATES THE NEED FOR SPECIALIZED TEST GEAR

Automated fault isolation of digital circuit boards can now be done without specialized testing gear. An automated functional simulation and troubleshooting package called Fast simply turns a logic analyzer and an IBM Corp. Personal Computer, PC/XT, or PC AT into a test system.

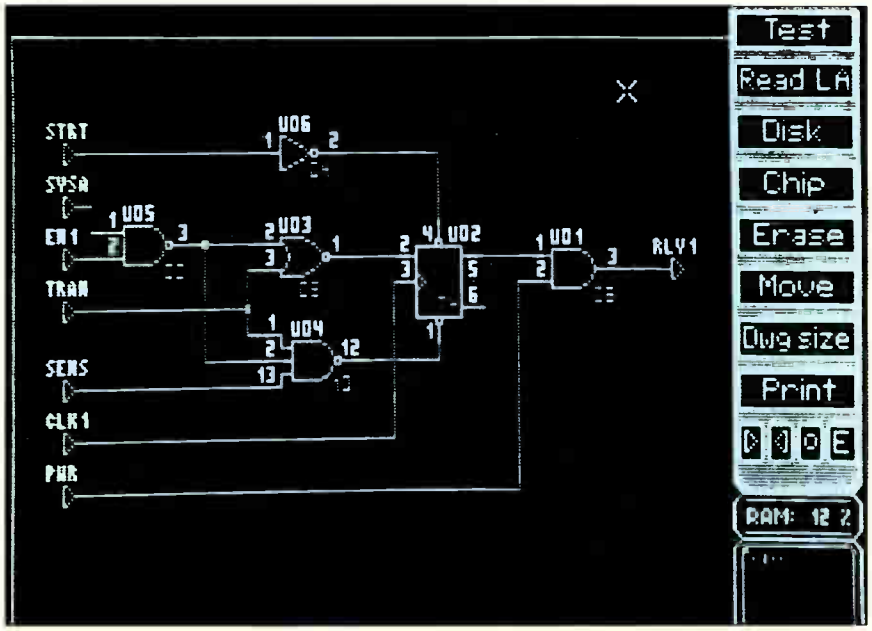
The portable system, which resides in the PC, was developed by Automated Logic Design. The analyzer is connected over an RS-232-C link or IEEE-488 bus to a PC equipped with at least 512-K bytes of RAM and a hard disk.

The analyzer probes attached to the pc board under test capture signals that the Fast software compares to a set of references derived from a schematic of the circuit under test stored in the computer. Discrepancies between expected and measured signals are indicated on the computer screen.

Other test systems usually require the generation of unique test patterns and a comparison with the outputs of known-good hardware. This approach requires special test fixtures. It isn't economically practical to produce such fixtures in many applications, including engineering breadboard debugging, in-system hardware tests, field hardware troubleshooting, and small production runs. So engineers have had to rely instead on tedious and time-consuming manual troubleshooting.

LIVE SIGNALS. The Fast system can replace those manual operations. What's more, it detects design and wiring errors on boards in their actual system environments. All other testers require that the devices be transferred to a specialized test environment, which is a burden on field service, particularly in military applications and in remote areas. But the Fast system works with live signals, so doing a test means simply bringing the logic analyzer and computer to wherever the board is.

Another difference between the Fast system and most other test systems is that it does not require special board conditioning—presetting, resetting, grounding, or waveform generation—and analysis can start from any unknown initial condition or from any operational cycle. In addition, feedback loops need not be disconnected.



PC CONTROLLED. A PC-based fault-isolation package does away with test fixtures.

Furthermore, the system can isolate faults on partially assembled or modified boards. The basic Fast package works on boards containing gate arrays and other programmable logic arrays; RAMs and ROMs; and the logic families 54/7400, CMOS 4000, emitter-coupled logic 100K, and Motorola ECL 10K.

To operate the system, the user connects the logic-analyzer probes to points on the circuit board; the resulting timing signals are displayed on a monochrome monitor. The Fast software compares these signals with those generated by Aldec's schematic logic analyzer and verifier (SLAV) software.

The logic analyzer stores the board's test-point signals and sends them to the computer, which performs the logic operations dictated by the stored functional schematic reference. When it has determined what the outputs should be, the computer compares them with the signals from the analyzer. Discrepancies are indicated in reversed video.

Bad ICs, shorted or open lines, or points stuck in the high or low state are highlighted on a color monitor that displays the schematic of the logic circuit under test. If desired, a single color monitor can be used to alternately display either the timing signals or the logic schematic.

The company will soon introduce three new software options that can be added to the basic package. The first is for test-point evaluation, to analyze all signals and indicate whether the provided waveforms are adequate for a complete test of the circuit board. A second

Electro/86

Judging by product introductions slated for this week's Electro '86, the electronics industry is showing some signs of vitality. Products featured in these six pages run the entire gamut from components to systems. When the show opens on May 13 for three days at Boston's Haynes Auditorium, some 50,000 electronics professionals are expected to visit its 1,200 exhibitors.

option is spike-analysis software that automatically checks spikes and determines their effect on system behavior. Finally, a propagation-delay analysis program will display the propagation characteristics of an IC under its actual operating conditions.

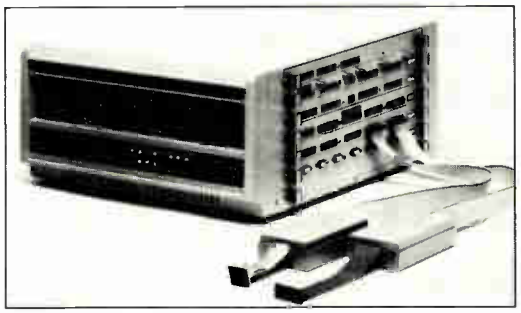
Delivery of the basic Fast software package will begin this month, with a price of $2,500 for users who already own SLAV software; the combined price for the Fast package and SLAV will be $3,000 to $7,500, depending on the logic analyzer chosen. Those prices do not reflect the cost of the computer.

The company says the test-point evaluation software will be available later in the second quarter, the spike-analysis program in the third quarter, and the propagation-delay software in the fourth quarter. *–Jonah McLeod*

Automated Logic Design Co., 3525 Old Conejo Rd., Suite 111, Newbury Park, Calif. 91320. Phone (805) 499-6867
[Circle reader service number 357]

512-CHANNEL ANALYZER DEBUGS 50-MHz LOGIC

Step Engineering is adding an all-purpose analysis tool that combines both speed and a high channel capacity. The Digital Analysis System, which works on a range of digital circuitry, including both logic and memory, will be offered as a standalone unit or with an IBM Corp. RT Personal Computer. It is designed to perform design verification, debugging, and testing on digital circuitry ranging from ICs to complete systems and bit-slice processors, pc boards, and subsystems.



REPLACEMENT. Step's Digital Analysis System can replace logic analyzers and pattern generators.

A fully configured system provides up to 512 channels of simultaneous stimulus generation and response analysis for circuits operating at speeds up to 50 MHz. The system can supply a pattern of stimulus data and control signals to the target device, analyze data both at the target's output and within the target, and change the stimulus-data pattern and its timing according to the target's response. Timing resolution on stimulus channels is to within 200 ps; on response-data channels, it's 100 ps.

The system, which is priced starting at $25,000, is offered as a lower-cost solution for engineers who now use logic analyzers teamed with power supplies and pattern generators. A sophisticated logic analyzer alone is priced in the $20,000 range and doesn't support as many channels. What's more, a logic analyzer and generator lack features that are on the DAS, such as data analysis.

The system comes with a 32-K-word buffer memory for storing response data; the system can check the data in the buffer against a file of expected responses. Data held in the response buffer can be learned—that is, stored in a file—and used as the expected response data for future comparisons.

A DAS consists of three main sections: the controller, the pattern stimulus section, and the response measurement section. At the heart of the system is the controller, which provides the necessary real-time control for running the patterns, collecting response data, and controlling the interaction with a target. The controller section operates the rest of the DAS under the direction of the CPU controlling the system bus.

Simple commands issued by the user cause all the necessary signals to appear and data to be sent and collected at the programmed timers. Keyboard commands instruct the controller to run a pattern and strobe data into the response buffer, to halt at a previously programmed breakpoint, and to resume after an examination of the target conditions has been completed. For state-by-state examination, single-step instructions can be issued after a halt.

The stimulus section contains memory to hold the stimulus data, circuitry to send the stimulus-data pattern at the right times, and circuitry to load a pattern of stimulus data from the CPU bus into the stimulus memory. The response section acquires data from an external target and holds it in its memory for analysis by such software as the comparison routine.

In most applications, connection of the target to the DAS is accomplished—at CMOS, TTL, or ECL levels—with Step's pods and appropriate cables. In-circuit emulators for certain bit-slice parts are available, including the 2918 and 29116 from Advanced Micro Devices Inc. and the 74AS888 and 74AS898 from Texas Instruments Inc. ROM, RAM, and PROM can be emulated by Writable Control Store arrays in the system.

While an analysis is being run, the keyboard remains live, enabling the user to change operating parameters on the fly without halting the target. Also, help menus may be left on the CRT screen or called up at any time, even during a run. The system is available 45 days after ordering. *–Steve Zollo*

Step Engineering, 661 E. Arques Ave., Sunnyvale, Calif. 94086.
Phone (408) 733-7837 [Circle 350]

8-BIT CONVERTER DRIVES 2-K-BY-2-K-PIXEL CRT

An 8-bit digital-to-analog converter from Honeywell Inc. has the blazing conversion rates and the on-chip features needed to support CRTs with resolutions of 2,000 by 2,000 pixels. The 24-pin HDAC51400 offers a guaranteed conversion rate of 385 million words/s with a 10% to 90% rise time of output signals of less than 1 ns.

"To get up to these speeds before, people had to resort to tricks like using standard nonvideo-ready DACs or using several video DACs and switching between them to get the speeds up," says Steve Sockolov, marketing manager for high-speed data-acquisition products at Honeywell's Signal Processing Technologies Venture in Colorado Springs.

The new generation of CRTs, with resolutions of 2-K by 2-K pixels, must be driven at a minimum of 325 MHz, says Sockolov. "Depending upon such things as CRT refresh rates and the application, that number could be higher—up to 380 MHz," he adds. The HDAC51400 has a nominal update rate of 400 megawords/s. The 8-bit raster DAC is aimed at such applications as medical electronics displays, computer-aided-design work stations, and test equipment.

To achieve such speeds, Honeywell is fabricating the 51400 in its 2.5-μm bipo-

lar technology. The 0.103-by-0.122-in. chip contains an on-board bandgap voltage reference and a dozen latches to hold video, data, and video-control bits—such as synchronization, blanking, bright, and forced-high signals.

It is housed in a 24-pin ceramic DIP and sells for $74.38 each in 100-piece quantities. Samples will be available in May, with volume deliveries expected in a couple of months.

The 51400 operates with a single −5.2-V power supply and dissipates 1.04 W over its temperature range of −25°C to +85°C. The DAC will drive a doubly terminated 50- or 75-Ω load directly, and it does not have to be buffered in the video system. All data lines that come from the part are compatible with emitter-coupled logic. *–J. Robert Lineback*

Honeywell Inc., Signal Processing Technologies Venture, 1150 E. Cheyenne Mountain Blvd., Colorado Springs, Colo. 80906. Phone (303) 577-1000 [Circle 356]

BOARD SET BUILDS VMEBUS SYSTEMS

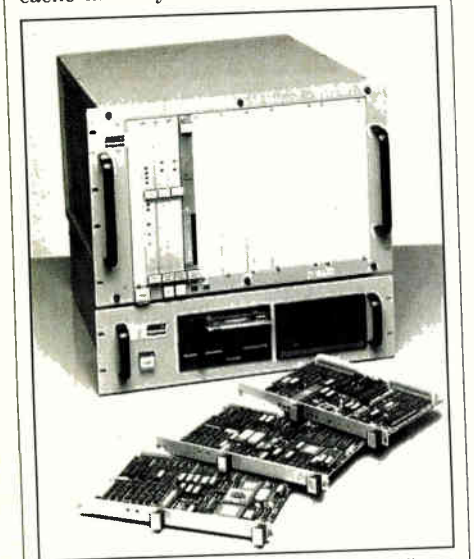
Ironics' Performer 32/D board set lets original-equipment manufacturers build high-performance multiuser systems around the latest emerging industry standards: the VMEbus, Unix V.2, and the 68020 processor. At its core are two high-performance VMEbus boards—the IV-3201 CPU and the IV-3273 system control and console I/O interface.

The IV-3201 is built around a Motorola 68020 processor running at 16 MHz with no wait states. The board needs no cache memory. The card uses the 68851 memory-management unit and can accept a 68881 floating-point coprocessor. On-board RAM totals 1 megabyte, which is dual-ported with the VMEbus. This feature, in combination with the bus-interrupter and interrupt-handler modules, provides the interprocessor synchronization and communications capability needed for a multiple-CPU system.

With the Ironics system, users can take advantage of the VMEbus extension bus, the VMXbus. The IV-3201 has two independent 32-bit bus interfaces, which allow the expansion of tightly coupled resources over the VMXbus. The VMEbus controls interprocessor communications and use of resources.

The IV-3273 serves the system in two ways. It is a VMEbus system controller handling all I/O functions over the bus and it serves as a mass-storage and I/O interface to the user. With it and any of the Ironics line of CPU boards, a complete disk-based computer system can be configured with as few as two cards.

In addition to its system-controller functions, the IV-3273 includes two asynchronous serial ports; two buffered,



EXPANDABLE. The Ironics system allows use of the VMX expansion bus.

general-purpose parallel ports; a battery-backed clock-calendar chip; a Small Computer Systems Interface for integrating disk drives; two programmable timers; and an interrupt structure that can operate as either a round-robin or parallel priority arbiter.

SCSI SUPPORT. The board supports a full SCSI implementation, including host-to-host communications. It handles data-transfer rates of more than 8 Mb/s. Because the IV-3273 uses 32-bit direct-memory-access transfers over the VMEbus, disk data transfers use less than 25% of the VMEbus's bandwidth. This minimizes the degradation of coexistent real-time processes due to disk-drive transfers, Ironics says. The card supports a wide range of mass-storage peripherals, including floppy- and hard-disk drives, removable-cartridge tape drives, and nine-track tape drives.

Ironics offers a variety of operating systems and programming languages. The Unix V.2 operating system, which is compatible with AT&T Bell Laboratories software, comes from Unisoft with enhancements by Unisoft and the University of California at Berkeley. A C-language compiler and 68000 assembler are provided with the Unix operating system. Ironics also provides Ada, Cobol, Fortran, and Pascal compilers.

In addition, flexible and easy-to-use facilities are provided so that systems integrators can install third-party device drivers for serial I/O functions, Storage Module Drive interface boards, and Ethernet interfaces.

The Performer 32/D systems, which support two users in their basic configurations, are priced starting at under $18,000 and will be available in the second quarter. *–Steve Zollo*

Ironics Inc., 798 Cascadilla St., Ithaca, N. Y. 14850.
Phone (607) 277-4060 [Circle 354]

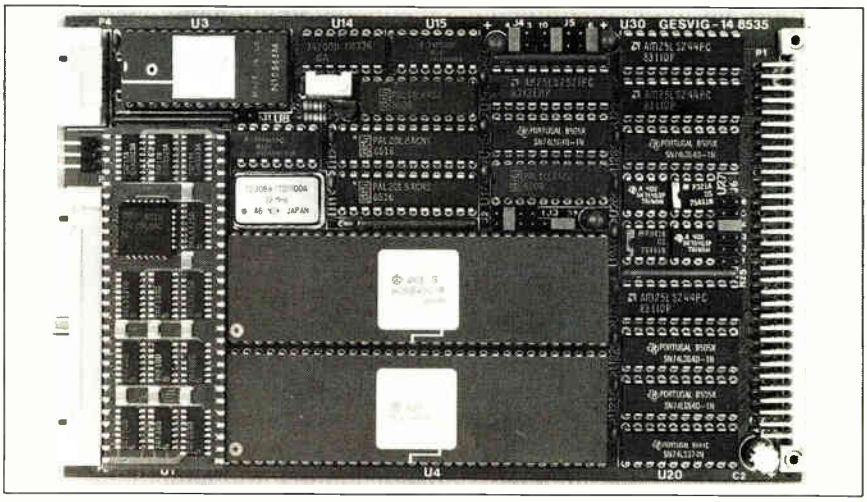
GESPAC BUS ADDS GRAPHICS, MEMORY CARDS

Gespac is making its proprietary bus more attractive to systems integrators by adding a graphics controller and memory board to its stable of offerings. The boards target designers of computer-aided-design work stations, industrial data terminals, and displays for navigation computers.

The Gesvig-14 controller supports noninterlaced displays of up to 800-by-600-pixel resolution in up to 16 simultaneous colors. The board uses Hitachi Ltd.'s advanced CRT controller, the HD63484, to draw more than 2 million pixels/s. It also contains a direct-memory-access controller that allows the user to exchange large blocks of display memory with system memory over the bus. With this feature, the user can create screen updates at speeds greater than 4 megabytes/s.

However, more cost-sensitive or less performance-sensitive applications do not require DMA operations. The interface to the controller can be handled completely under software control. The Gesvig-14 performs an interleaved access for display and drawing operations. Because there is no contention between display and drawing accesses, a flicker-free display is obtained while maintaining full drawing speed.

Most other controllers require additional hardware for windowing, but the



SQUEEZE. Surface-mount technology lets Gespac squeeze many features on the Eurocard.

HD63484 supports on-board windowing on the Gesvig-14. The chip divides the physical frame memory space into four logical screens; for each logical screen, the host specifies a starting address in the physical memory, the number of memory words per raster, and the number of bits per pixel.

The Gesvie-14 memory board is useful for CAD and other applications that demand fast pan and scroll throughout the display memory. Its 2 megabytes of dynamic RAM store four times the maximum display data of the Gesvig-14 controller board. This excess memory can be used to store the different windows supported by the controller or several different pictures, which can be recalled instantaneously to generate animation displays.

To pack such extensive features into the single-height Eurocards that serve as Gespac's form factor, the company went to surface-mount technology. Gespac's G-64 and double-wide G-96 buses are easy-to-use midrange 8- and 16-bit vehicles for industrial applications.

Gespac supports this subsystem with software drivers developed for the 68000-based OS-9 multitasking, real-time operating system. The boards are available now at $3,950 each. *–Ann Jacobs*

Gespac Inc., 100 W. Hoover Ave., Suite 11, Mesa, Ariz. 85202.
Phone (602) 962-5559 [Circle 351]

LAB APPLICATIONS RUN ON MACINTOSH

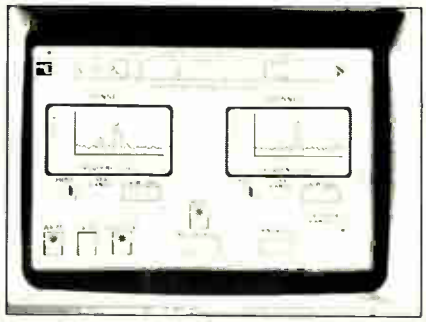
Programmers of test and measurement systems will get a new view of computer controls with LabView, a graphical programming product that runs on an Apple Computer Inc. Macintosh. National Instruments Corp.'s package applies the popular desktop system's icon interface to the development of such laboratory applications as instrument control, data acquisition and analysis, and report generation.

LabView's graphical programming language depicts an instrumentation configuration with images of front panels and functional block diagrams displayed on the Macintosh's screen. National Instruments also sells interface systems that attach the Macintosh to instruments over standard interfaces such as the IEEE-488 bus.

VIRTUAL. The heart of the new programming system is what National Instruments calls a virtual instrument, which the user sees as an image of a front panel. The panel is actually an icon that has "hot spots" representing a system's inputs and outputs. The company plans to build a library of icons representing commonly used lab instruments.

At Electro, National Instruments will demonstrate LabView with the icon of a voltmeter from John Fluke Mfg. Co. and a Wavetek Corp. arbitrary-waveform generator. The panels provide a window for interactive operation. Beneath the icon, a series of modular block diagrams is used to program functionality.

LabView is self-documenting because the front-panel icon and block diagrams construct a complete drawing of the op-



GRAPHICAL. National gives users a graphical view of hooking up their instruments.

POSITIONS VACANT

U.S. DSP Program Manager with MSEE or Electronic (DSP concentration) and 7 years experience in DSP including hardware and software design. PhD in same with 5 years experience acceptable. Knowledge of programmable semi-conductor products, development systems and TMS320DSP or equivalent required. Background in speech, telecommunications and data communications, control and developing/instructing DSP courses. Travel minimum 30% in U.S. Salary to: $47,000. Send resume to: P-6365, Electronics.

POSITIONS VACANT

South? Technical/Professional Placement Network-Fee paid. Murkett Associates, Box 527, Montgomery, AL 36101.

Design Engineer responsible for design, analysis & support of state-of-the-art low-to-medium switching power supplies for consumer, commercial & industrial applications; engage in modeling, analysis & measurement techniques & closed loop stability, analog power, circuit design & development; engage in magnetic design, component specification, thermal analysis, EMI/EMC & reliability analysis as well as computer aided engineering. Masters degree in Electrical Engineering required & must have completed one course in either Power Electronics, Theory of Semiconductor & Semiconductor devices & semiconductor electronics. 40 hrs. M/F, 8:30 to 5:00, $33,000/yr. Send resumes & SSN to: Illinois Job Service, 910 S. Michigan, Rm. 333, Chicago, Ill. 60605, Attn: Dennis Doligala, Ref. #5491D, An Employer Paid Ad.

POSITIONS WANTED

Electronic Expert For Hire. I do Microprocessor hardware/software, assembly language. Analog, digital design in my N.Y. lab or worldwide. Project rates. Mr. Barry Masel (718) 476-1516.

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We Buy and Sell all kinds of surplus inventory — electronics, computers, OEM, etc. (718) 639-2872.

ELECTRO ROUNDUP

eration and system configuration. The package sells for $1,995. National Instruments expects to begin deliveries in August. *–J. Robert Lineback*

National Instruments Corp., 12109 Technology Blvd., Austin, Texas, 78727.
Phone (800) 531-4742 [Circle 355]

ON-CHIP DIODES CUT DRIVER COSTS

Sprague Electric's dual full-bridge motor-driver chip comes with eight power diodes on chip so that original-equipment manufacturers need not assemble external diodes at additional cost. Though the diodes are essential for motor-driver applications, competitors SGS Semiconductor and Unitrode Corp., which both make the industry-standard L298 driver, do not include them on chip. Adding discrete diodes can cost an additional 50¢ to 80¢ per driver.

The UDN-2998W is not a direct replacement for the L298, but an enhanced version with a different pinout, Sprague says. The part serves as an interface between low-level logic and solenoids, high-current stepper motors, and brushless dc motors.

The UDN-2998W handles load-input voltages of up to 50 V, compared with the 46-V maximum of competing systems. It is rated for continuous currents of up to 2 A, with peak or startup currents of 3 A per bridge. Logic-control inputs are compatible with TTL, diode-transistor logic, and 5-V CMOS logic.

The part's 12-pin single-in-line power-tab package provides 50% better allowable power dissipation than competing products, says a company spokesman. "Heat is the big killer of ICs," he says, so extensive circuit protection is provided on chip. A thermal-shutdown circuit disables the load drive if temperature exceeds the chip's rating. Because the chip runs cooler, it can last up to three times longer than other versions. At +25°C, the package can dissipate 5.2 W, compared with competitors' 3.5 W.

An internal regulator lets the UDN-2998W operate from a single voltage supply. Other chips require two power supplies. Sprague's motor driver also features an internally generated turn-on delay to prevent crossover currents when switching current direction.

The UDN-2998W is available now for $4.16 each. *–Debra Michals*

Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606.
Phone (617) 853-5000 [Circle 353]

NEW PICOLOGIC™ MUX/DEMUX LETS YOU TRANSMIT 5 YEARS OF *ELECTRONIC NEWS* IN 1 SECOND.

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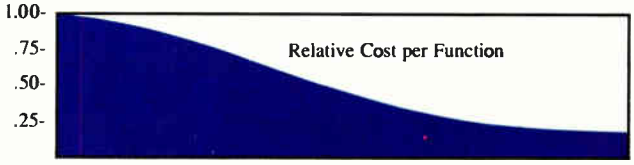

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THE NEXT GENERATION

Circle 65 on reader service card

In Surface Mountable Chip Components. TDK Quality Is More Than Skin Deep.

As boards are getting thinner, TDK is helping that diet succeed by providing a variety of extra-slim surface mountable components. Nourished by TDK's expertise in ferrite and ceramic materials, these miniaturized components feed on TDK-developed multi-layerization and multi-functionalism.

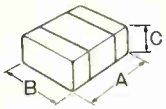
How we know the exact needs of high-quality automated board production? Well, a fair share of the world's automatic mounting equipment—the Avimount series—comes from TDK.

Multi-layer Ceramic Chip Capacitors

A wide range of capacitances and high dimensional accuracy are instrumental in the production of slim, high-density, quality boards.

Dimensions A x B x C (mm)	Class I (50V)						
	CH	PH	RH	SH	TH	UJ	SL
3.2 x 1.6 x 0.6~1.1	0.5~680pF	0.5~820pF	0.5~1,000pF	0.5~1,200pF	0.5~1,520pF	0.5~1,500pF	0.5~2,700pF
2.0 x 1.25 x 0.6~1.1	0.5~430pF	0.5~560pF	0.5~680pF	0.5~750pF	0.5~820pF	0.5~1,000pF	0.5~1,800pF

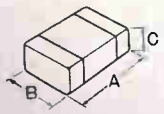
Dimensions A x B x C (mm)	Class II	
	50V	25V
3.2 x 1.6 x 0.6~1.1	1,000~100,000pF	12,000~220,000pF
2.0 x 1.25 x 0.6~1.1	470~47,000pF	6,800~100,000pF



Multi-layer Chip Inductors (MLF Series)

Coilless chip inductors utilizing TDK's multi-layer ferrite technology. Closed magnetic paths for perfect shielding.

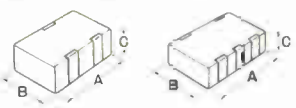
Dimensions: A x B x C (mm)	Inductance (μH)
3.2 x 1.6 x 0.6	0.1~1.2
3.2 x 1.6 x 1.1	0.39~27
3.2 x 2.5 x 1.1	33~56
3.2 x 2.5 x 2.5	68~220



Multi-layer Chip Transformers, IFT, LC Traps

With the world's smallest transformers, IFT and LC traps (series 4532), TDK advances automated surface mounting by another significant step. Monolithic IFT and LC traps incorporating non-adjustable transformers and capacitors in a single, sintered, multi-layer block. Another world's first from TDK.

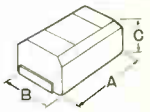
Series designation Dimensions: A x B x C (mm)	Applicable frequency range	Characteristics
MTT (transformers) 4.5 x 3.2 x 2.8	300kHz~1MHz	L 10~200μH
MIA (AM IFT) 4.5 x 3.2 x 2.5	455kHz, 459kHz 464kHz	Q above 40
MIF (FM IFT) 4.5 x 3.2 x 2.0	10.7MHz	Q above 40
MXT (LC traps) 4.5 x 3.2 x 2.2	in-series type parallel type	F~2% Attenuation over 20dB



Leadless Inductors (NL & NLF Series)

Especially suitable for automatic high-density mounting. Epoxy sealed, excellent dimensional accuracy, large inductance, steep Q. High temperature and humidity resistance.

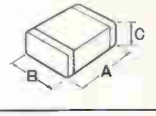
Series designation, Dimensions: A x B x C (mm)	Inductance range (μH)	Q
NL 3.2 x 2.5 x 2.2	0.12~100	20~30
NL 4.5 x 3.2 x 3.2	1.0~1,000	30~50
NLF (shielded) 4.5 x 3.2 x 3.2	1.0~1,000	30~50



Ferrite-chip Type Microbeads (CB Series)

Effectively eliminate EMI/RFI and parasitic oscillation vibrations. Suitable for easy, automated surface mounting. Your new, reliable anti-noise (EMI/RFI) weapon. Mounted on circuit board, no need for lead wires.

Dimensions: A x B x C (mm)	Impedance (Ω) at 100MHz	DC resistance Rdc (Ω)
2.0 x 1.25 x 0.9	5~9	0.030~0.033
3.2 x 1.6 x 1.1	14~26	0.048~0.055
3.2 x 2.5 x 1.3	37~77	0.105~0.121
4.5 x 3.2 x 1.5	55~130	0.193~0.212



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Circle 66 on reader service card

SPUTTERING SYSTEM BOASTS HIGH THROUGHPUT ON 8-IN. WAFERS

MATERIALS RESEARCH CLAIMS HIGH UNIFORMITY AT 60 WAFERS AN HOUR

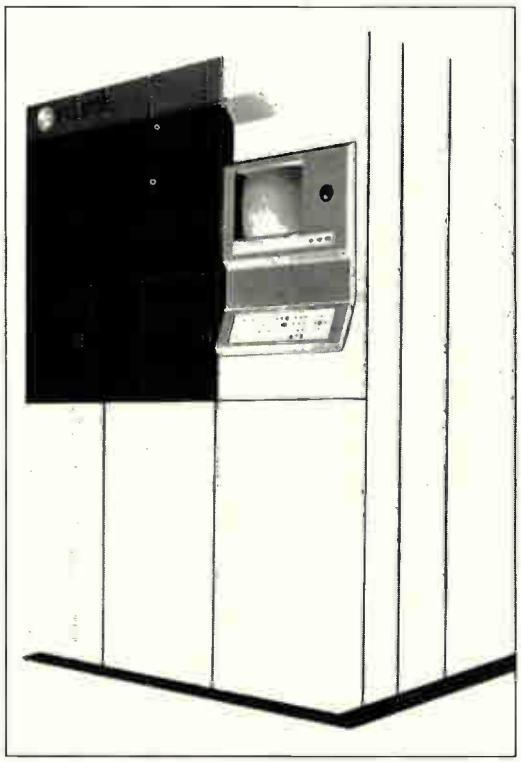
Materials Research is expanding its line of semiconductor-processing equipment with an automated cassette-to-cassette sputtering system targeted at production runs of 8-in. wafers. The Eclipse, like its sister product, the Aries etcher [*Electronics*, March 10, 1986, p. 69], is aimed at the chip maker that is looking for high quality in high-volume production.

For a 1%-aluminum silicon film, for example, the Eclipse achieves deposition rates up to 13,000 Å/min (or 1.3 μm/min). This translates into a throughput for aluminum and aluminum-alloy processes of about 60 wafers per hour, according to Howard Siegerman, director of marketing for sputtering equipment at Materials Research. He admits that figure is not the fastest in the industry, but maintains that "wafer throughput becomes less important as wafer size goes up." Film uniformity is high, at ±5% over the life of the target, and in a typical 1-by-2-μm geometry, step coverage is at least 50%.

"High volume is the key to success in very large-scale-integration technology," says Donald Messina, sputtering equipment product manager. He says that in order to be competitive in the fast-paced world of VLSI technology, semiconductor companies need to boost their yield and throughput figures, and to do that they need sputtering systems that can provide even coatings and high step coverage on the biggest wafers available—6 and 8 in.

Looking to support growing interest in larger wafer sizes, Eclipse was designed first for 8-in. wafers and then modified to accommodate 6-in. wafer technology as well. "We decided it would be more important to develop the 8-in. technology and scale it down to 6-in. than to do it the other way round," Messina says. He adds that the machine can be adapted from one size to the other in a day's time.

FIVE-CHAMBER OPTION. Two versions of the system are available. The first is a four-chamber system with a load-lock station, a sputter-etch cleaning station, and two deposition chambers for double-metal processes. The second offers a fifth chamber for a third metal layer. Messina says chip makers can choose to eliminate the sputter-etch stage, which cleanses the wafer of debris prior to deposition, and use that chamber for sputtering as well.



STILL LIFE. No wafer movement occurs during processing with Eclipse, cutting particulate contamination.

Because good step coverage is a function of a machine's ability to maintain a low-pressure vacuum, each process chamber has its own dedicated cryogenic pump capable of maintaining a vacuum level of 6×10^{-8} Torr. In addition, the load-lock and transport chamber share a fourth cryogenic pump that maintains an already-low vacuum of 10^{-7} Torr, which helps to hasten pump-down in the process chambers. Thanks to separate heating units in each process chamber, temperature levels can be individually tailored to each process for optimum results.

Automation is also important to chip makers, who want systems that help eliminate the human factor from the manufacturing process. This requires multiple process chambers to isolate wafers from one another in order to avoid process contamination. Wafers travel through the system on a rotating platter that carries the wafers from chamber to chamber.

A robotic arm takes the wafers from the cassettes to the load-lock chamber, where it places them on the wafer-transport mechanism. Like the process stations, the load-lock chamber can preheat the wafer to speed the manufacturing process. Although four wafers share the transport chamber, or plenum, at any one time, that area is maintained as a controlled environment and is constantly purged with dry nitrogen to eliminate water vapor, which can damage the wafer during processing.

The Eclipse sputtering system is priced from $900,000 and delivery takes 180 days. *–Tobias Naegele*

Materials Research Corp., Route 303, Orangeburg, N. Y. 10962. Phone (914) 359-4200 [Circle reader service number 338]

SEIKO TAKES ON TEKTRONIX IN GRAPHICS TERMINALS

Seiko Instruments is taking Tektronix head on with a graphics terminal it claims is twice as fast and priced 15% less than the market leader's. The GR-1105 offers an addressable coordinate space of 32-K by 32-K points of virtual resolution and meets the demands of computerized pc-board design systems for close tolerances.

The GR-1105 relies on a mainframe or minicomputer for the most taxing work of data storage but has sufficient self-contained display-list memory to execute 4,500 short (¼-in.) vectors/s. The 14-in. screen's displayable resolution is 1,024 by 780 pixels, usually found only on 19-in. screens.

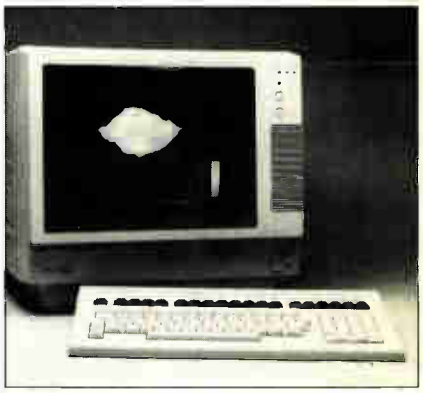
Senior product manager Michael

COMPUTER GRAPHICS

Warner sees the GR-1105 competing successfully with Tektronix' 4106A and 4107A terminals, which have 640-by-480-pixel resolutions and speeds of 2,000 vectors/s. The Seiko product is priced at $4,995, compared with $5,995 for the 4106A and $6,995 for the 4107A.

SPEEDY. The GR-1105's speed comes from its three parallel very large-scale-integration graphics display controllers, which drive independent memory planes. A combined 8086/8087 processor pipelines instructions to these controllers at 8 MHz. A custom gate array handles color mapping, also helping to boost drawing speed and display time.

In the mechanical-design, electrical, and civil-engineering markets, Warner says that the GR-1105's higher resolution and faster pixel update give it a strong advantage as blueprints and circuit designs become more and more complex in these fields. In other engineering tasks, the GR-1105 can display complex blueprints locally without first reducing them into 4-K-by-4-K sections.



FASTER. Seiko takes on Tektronix with a faster graphics terminal.

Individual levels of a multilayer pc board can be treated as separate logical elements with independently selectable attributes for color, screen assignment, and display priority. Because the complete drawing is stored locally in segment memory, pan and zoom are fast, even for large layouts.

Color graphics and text are combined into a single image at a 60-Hz noninterlaced refresh rate. Standard interactive drawing functions include rubberbanding, dragging, inking, zooming, positioning, rotation, and scrolling. Interactive devices for the GR-1105 include landscape and portrait digitizers and a mouse.

The standard system supports 512 colors, compared with 64 for the Tektronix models. A contrast-enhancement filter eliminates screen glare and improves image visibility. Peripheral and hard-copier interfaces are also standard on the GR-1105, which supports both color hard copy and transparency creation.

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Circle 69 on reader service card

COMPUTERS

The user can design applications with Seiko's Graphical Control Subroutine software, or use third-party applications packages from a number of vendors of business, scientific, and engineering software, including PDA Engineering, Issco, and Swanson Analysis. Delivery takes 60 days. *–Ann Jacobs*

Seiko Instruments U.S.A. Inc., Graphic Devices and Systems, 1623 Buckeye Dr., Milpitas, Calif. 95035.
Phone (408) 943-9100 [Circle 339]

HARRIS SUPERMICRO OUTGUNS MICROVAX

Harris's Computer Systems Division has long been known for playing a good game of hardball in the price/performance stadium. Now it has entered the race for the markets where Digital Equipment Corp.'s MicroVAX II holds the pennant with a series of machines that team multiple copies of Motorola's 68020 microprocessor with the 68881 floating-point coprocessor in a three-bus environment. In particular, Harris hopes to maintain a strong position with its traditional customers in the engineering field.

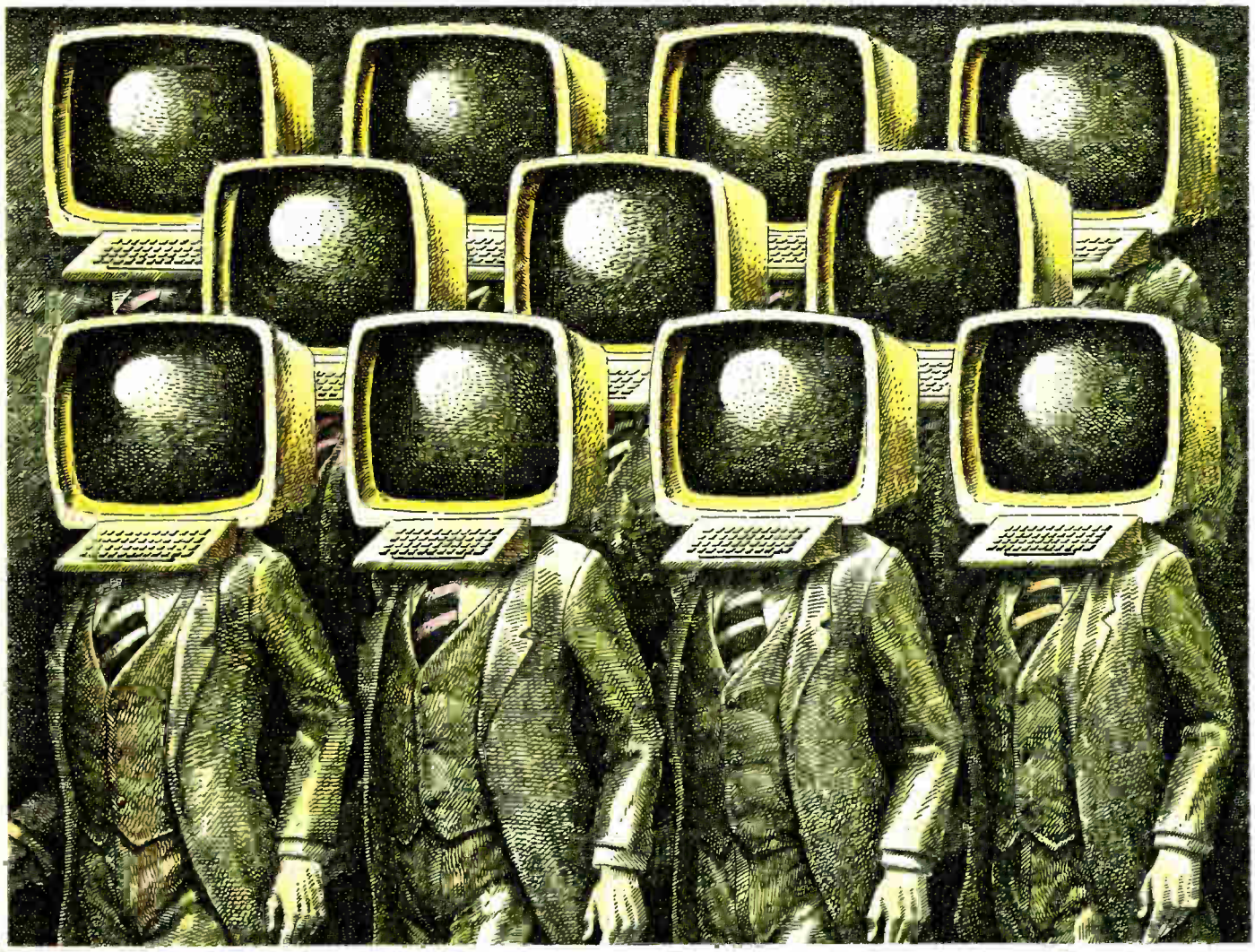
Harris's first MCX supermicrocomputers have from one to four CPU cards, each of which carries a 16.7-MHz 68020 and a companion 68881. Each of these cards is said to bat out 1.5 million single-precision or 1.0 double-precision Whetstone instructions per second.

A single-CPU system, the MCX-3 model 40, offers this level of performance for a starting price of $18,700. That is slightly less expensive than a MicroVAX II, which achieves well under 1 million single-precision Whetstone instructions/s, or about 1 million instructions/s when equipped with a floating-point accelerator. But Harris also offers an optional floating-point accelerator card, which boosts performance to 3.6 million single-precision and 2.8 million double-precision Whetstone instructions/s.

The 32-bit MCX machines, which run under Harris's HS/UX Unix-based operating system, are designed for high-performance real-time applications such as simulation, analysis, modeling, process control, and communications. The present top of the line is the MCX-5 model 70, which is priced at $73,000 and has four CPU cards. The MCX-3 model 60 and MCX-5 model 60 are midrange systems that support two CPUs each.

Each system includes an 8-K-byte cache memory; separate buses for memory, I/O operations, and real-time data

All too often, you can become just another face in the crowd simply by following it.



Following the crowd is no way for any hi-tech company to select a new location. You'd overlook more than you can imagine.

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BALTIMORE GAS AND ELECTRIC

Circle 84 on reader service card

acquisition; and virtual memory management hardware. In addition, the systems come with a Small Computer Systems Interface for disk drives. The family supports up to 32 megabytes of main memory, 256 megabytes of physical address space, and 4 gigabytes of virtual address space.

Harris's operating system, HS/UX, is based on both AT&T Co.'s System V and the Berkeley 4.2bsd Unix versions. HS/UX enables users to alternate between the two Unix systems and offers access to an abundance of software-development tools and application packages. Harris provides compilers for C, Fortran, and Ada.

Rather than going to Multibus II, which has few peripherals available for it, Harris's MCX design is based on an enhanced Multibus I I/O system, which offers access to a wide variety of available peripherals. The MCX Multibus implementation allows a pair of 16-bit words to be transferred to or from memory in a single bus transaction, which in effect doubles the Multibus I/O bandwidth to up to 6 megabytes/s.

The memory bus and Multibus are separate and communicate through a hardware adapter designed for efficient direct memory access. Harris offers an Ethernet implementation to link the MCX computers to its work stations and superminicomputers.

The entry-level single-processor MCX-3 model 40 supports up to 12 users and has four expansion slots available; the double-processor model 60 has 12 available slots. The MCX-5 model 70 accommodates up to 64 users and 26 expansion slots. *–Steve Zollo*

Harris Corp., Computer Systems Division, 2101 W. Cypress Creek Rd., Ft. Lauderdale, Fla. 33309.
Phone (305) 973-5125 [Circle 340]

FIRST FAMILY. Harris hits the supermicro market with the 68020-based MCX series.

MEETINGS

NCC SHIFTS FOCUS TOWARD MANAGEMENT

The National Computer Conference is moving away from technical presentations and toward management issues. "We want to appeal to a broader audience," says program chair Addie Mattox of NCC, which will be held in Las Vegas June 16-19. "Last year's was more academic and research oriented than ours will be," adds Mattox, president of Mattox Group, a Laguna Hills, Calif., management-consulting firm that specializes in automated office systems.

About half of NCC's 95 sessions will be technical, and there are only 40 technical papers scheduled. Software issues and an in-depth look at artificial intelligence will dominate these presentations. Thirteen sessions will cover such software topics as fourth-generation languages, user-friendliness, and reusability, or "getting the most from programming efforts," she says. In response to the keen interest in AI, another seven sessions will explore that subject.

Besides software and AI, 12 technical sessions will be devoted to hardware and four to engineering issues. Networking will be the focus of a dozen sessions, half of which are technical. The others will offer nontechnical executives overviews on integrated-services digital networks, local-area networks, and microcomputer-to-mainframe links.

A set of seven sessions will debate controversial issues in the computer field, such as video display terminals and health problems, whether application programming is becoming obsolete, and "Should the data-processing department control personal computer use?"

CLEO/IQEC '86: Conference on Lasers and Electro-Optics/International Quantum Electronics Conference, IEEE and Optical Society of America (OSA, 1816 Jefferson Pl., N. W., Washington, D. C. 20036), Moscone Convention Center, San Francisco, June 9-13.

Comdex International in Europe, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Acropolis Conference Center, Nice, France, June 10-12.

Nepcon East '86, Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), Bayside Exposition Center, Boston, June 10-12.

Rochester Forth Conference, University of Rochester (Maria Gress, Institute for Applied Forth Research, 478 Thurston Rd., Rochester, N. Y. 14619), University of Rochester, Rochester, N. Y., June 10-14.

Distributed Information Systems: Emerging Uses and Technology, National Bureau of Standards and Association for Computing Machinery (Wilma M. Osborne, B266 Technology Building, National Bureau of Standards, Gaithersburg, Md. 20899), NBS Building, Gaithersburg, June 12-13.

NCC '86: National Computer Conference, IEEE *et al.* (NCC '86, American Federation of Information Processing Societies, 1899 Preston White Dr., Reston, Va. 22091), Convention Center, Las Vegas, June 16-19.

Compeuro '86, IEEE Computer Society, (1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Congress Center, Hamburg, West Germany, June 16-20.

ICC '86: International Conference on Communications, IEEE (Hugh J. Swain, Andrew Antenna Ltd., 606 Beech St., Whitby, Ont., Canada L1N 5S2), Dunfey's Hyannis, Hyannis, Mass., June 17-20.

Computer Vision and Pattern Recognition, IEEE Computer Society (1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Fontainebleau Hilton Hotel, Miami Beach, Fla., June 22-26.

94th American Society for Engineering Education Conference, ASEE (11 Dupont Circle, Suite 200, Washington, D. C. 20036), Clarion Hotel, Cincinnati, June 22-26.

Designing for Surge and Transient Immunity in Electronic and Computer Systems, University of Wisconsin-Madison (Francis P. Drake, University of Wisconsin-Madison, 432 N. Lake St., Madison, Wis. 53706), Howard Johnson Executive Hotel, Madison, Wis., June 23-26.

ATE East '86: Automatic Test Equipment Conference, Morgan-Grampian Expositions Group (1050 Commonwealth Ave., Boston, Mass. 02215), World Trade Center, Boston, June 23-26.

CPEM '86: Conference on Precision Electromagnetic Measurements, National Bureau of Standards, IEEE, and Union Radio Scientifique Internationale (Norman B. Belecki, National Bureau of Standards, NBS Building, Gaithersburg, Md. 20899), NBS Building, Gaithersburg, June 23-27.

EFOC/LAN 86: European Fiber Optics Communications & Local Area Networks Exhibition and Conference, Information Gatekeepers Inc. (Joan Barry, Information Gatekeepers, 214 Harvard Ave., Boston, Mass., 02134), International Congrescentrum Rai, Amsterdam, June 23-27.

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ELECTRONICS WEEK

PENTAGON TO BUY UK WORK STATIONS

Watch for Britain's Rank Cintel to announce that it has won a contract from the U. S. Defense Department to supply its Rank Cintel Retriever document-storage system [*Electronics*, March 22, 1984, p. 76] for an installation that the company says will ultimately be the largest in the world. Initially, the order is for five work stations at a cost of $3.8 million, but the company, in Ware, says the number will rise to 72 when the defense budget is passed.

JAPAN INCREASES R&D SPENDING 9.9%

Japan's spending for electronics research and development reached almost $44 billion in fiscal 1985, pushing the industry to first place in the country's R&D expenditures, according to Eurogestion KK, a Tokyo market researcher. The sum, which topped 1 trillion yen for the first time, was a 9.9% increase over the previous year. Representing 2.6% of Japan's gross national product, it places the country in third place behind the U. S. and West Germany.

BURROUGHS IN NEW BID TO BUY SPERRY

Burroughs Corp. last week renewed its attempt to acquire fellow computer maker Sperry Corp., despite being rebuffed last summer in a similar bid. Burroughs says the merged company resulting from the merger would maintain both partners' computer architectures yet realize savings through joint manufacturing, research and development, and procurement. Industry observers see little sense to the merger, since the two vendors have incompatible product lines and Burroughs's plan to support both could prove too expensive. Late last week, Burroughs started a hostile takeover because, says the Detroit company, Sperry, Blue Bell, Pa., was slow to respond to its originally friendly bid.

ZENITH UNVEILS FLAT-MASK CRT

Zenith Electronics Corp. says it has developed a new cathode-ray-tube technology that obtains nearly 70% better contrast ratios and 80% improved brightness over conventional units by flattening the shadow mask. The flat tube uses a shadow mask that is stretched and held under tension so that it is unable to distort during use the way conventional shadow masks do. The Glenview, Ill., company initially will supply a 14-in. version to original-equipment manufacturers of computer displays.

GCA HITS BLACK INK

Troubled GCA Corp., which has suffered losses in its three previous quarters, jumped into the black for the quarter ending March 31. The Bedford, Mass., builder of semiconductor-manufacturing equipment showed net income of $251,000 for the quarter on revenue of $37 million. GCA also announced that it had secured an additional $15 million in funds from its creditors.

XEROX TO SELL TANDON STATIONS

Tandon Corp., Chatsworth, Calif., and Xerox Corp., El Segundo, Calif., have entered into a joint agreement under which Tandon will manufacture a family of its work stations to be sold under the Xerox name. The work stations will augment Xerox keyboard products that are designed, developed, and manufactured by Xerox and by a number of outside vendors. Volume shipments are scheduled to begin later in the year. Under the terms of the multi-year agreement, the total dollar value can't be disclosed, the companies say.

MARIETTA, ALPHA IN CHIP VENTURE

Martin Marietta Corp., Bethesda, Md., and Alpha Industries, Woburn, Mass., will form a joint venture to develop gallium arsenide integrated circuits for millimeter-wave radar applications. Alpha will contribute expertise in the design and production of advanced microchips, and Martin Marietta will provide know-how in developing processes for materials production, circuit design and analysis, and chip testing.

GTE, FUJITSU FORM JOINT PBX VENTURE

GTE Corp. and Fujitsu Ltd. have agreed to form a joint venture that would develop and market private branch exchanges and other business communications systems for North America. The majority owner would be Fujitsu America Inc., San Jose, Calif. The final agreement is expected to be signed by the end of the year. The venture will market GTE's Omni family of PBXs as well as its Starlog voice/data communication system plus new products.

SIEMENS ADDS JOBS AND INVESTMENTS

Banking on continuing growth in the world's electronics and electrical markets, Siemens AG is adding 9,000 jobs at home and abroad. The hiring boom will bring the employee level to 357,000 worldwide. The Munich company has also raised its investments by 69%, to more than $1 billion, during the first six months of the fiscal year ending Sept. 30. Siemens—which is active in components, computers, and communications—expects to have investments of around $2.7 billion for the full 1985-86 fiscal year.

NORTHERN WINS IN JAPAN AGAIN

Northern Telecom Inc. has won another contract from Japan's Nippon Telegraph & Telephone Corp., this one for $260 million worth of digital telephone switching systems to be delivered over a five-year period starting in fiscal 1989. NTT says the Nashville, Tenn., company's systems, which will replace existing local exchanges in urban phone offices, will cost 30% less than competing Japanese brands because the stronger yen has made dollar prices more competitive.

DEC TO HELP SELL APTEC GEAR

Aptec Computer Systems Inc., Portland, Ore., which provides a boost for Digital Equipment Corp.'s VAX minicomputers with its special-purpose input/output processor, got a boost of its own last week from DEC. The Maynard, Mass., computer maker agreed in a joint marketing pact to distribute literature and make sales calls with Aptec. The Aptec 2400 computer is instrumental in solving a variety of I/O problems for the VAX by directing data transfers between the central processing unit and high-speed peripherals along a 24-megabyte bus.

ERICSSON WINS SWISS CONTRACT

LM Ericsson has beaten several international competitors in a bid to supply Switzerland with equipment to expand its cellular radio-telephone communications services, which are now operating at capacity. The Swedish company's Nordic Mobile Telephone system—already chosen by several countries in and outside Europe—beat out systems by companies in France, Germany, and the U. S. Switzerland chose the NMT system because it allows easy network extension.

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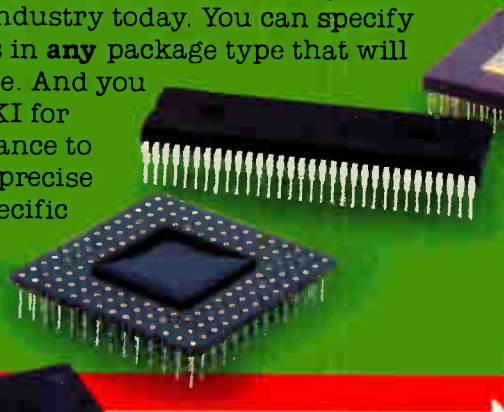

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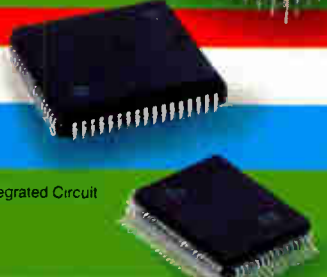

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# Gates	# I/Os	# Gates	# I/Os	# Gates	# I/Os
700	66	3289	86	387	44
1000	66	4290	104	720	62
1500	66	6000	130	1445	88
2000	80	8024	148	2000	106
2500	80	10008	172	4205	120

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