A McGRAW-HILL PUBLICATION THREE DOLLARS

Electronics®

THE WORLDWIDE TECHNOLOGY WEEKLY MARCH 3, 1986

A SIMPLE DESIGN MAY PAY OFF BIG FOR HP

BIPOLAR-MOS CHIPS ARE ABOUT TO HIT THE BIG TIME/27

HOW MOSIS WILL SLASH THE COST OF IC PROTOTYPING/48

Open one up.

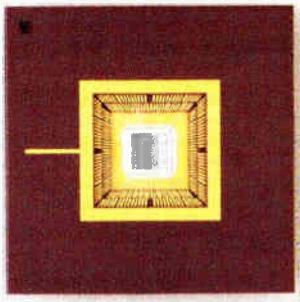
And feel your pulse accelerate. 50,000 logic gates on a single chip. Room enough to implement large macro-functions and build an entire digital system.

All with our new LCA 10000 Compacted Array™ Series.

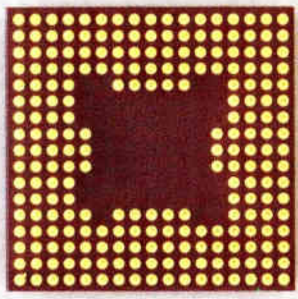
In theory, somewhere between a gate array and a cell-based custom IC.

In practice, it's a flat-out acceleration of our ASIC technology. With advanced 1.5 micron, dual-layer HCMOS technology. And our innovative variable routing tracks.

For performance no mere gate array can touch. 0.7 nanosecond propagation delay for a 2-input NAND gate. ECL-like speeds. Random Routing. VHSIC performance compatibility. And more.



Our new 50,000-gate LCA 10000 Compacted Array Series makes "System Scale Integration" a reality. Now, you can fit an entire system on a chip.



Even the packaging is advanced, with up to 256 I/O signal pins.

You'll get there fast, too, using our proprietary LDS™ Design System. Working at any of our 12 worldwide design centers.

And you'll get there safely. Thanks to our proven 97% first-time hit rate.

With manufacturing in our facilities. The best equipped in the country. Geared to pump out all you need. From hundreds. To hundreds of thousands. All thoroughly tested on our 256-pin system.

Start yours today. Call one of our sales offices listed below.

Because with our new Compacted Array Series driving your next design there's no telling how far you'll go.

Or how fast.

LSI LOGIC CORPORATION

San Jose, CA 408/248-5100, Irvine, CA 714/261-0124, Sherman Oaks, CA 818/906-0333, Denver, CO 303/756-8800, Westport, CT 203/222-9336, Altamonte Springs, FL 305/339-2242, Boca Raton, FL 305/395-6200, Schaumburg, IL 312/397-0155, Waltham, MA 617/890-0161, Ann Arbor, MI 313/769-0175, Minneapolis, MN 612/835-6161, Raleigh, NC 919/872-8400, Trevose, PA 215/638-3010, Austin, TX 512/343-4513, Dallas, TX 214/788-2966, Bellevue, WA 206/455-5055, Nepean, Ontario 613/726-1585, England 44-344-426544, Israel 972-3-421146/7, Japan 81-3-589-2711, West Germany 49-89-926903-0 LCA 10000 Compacted Array Series is a registered trademark of LSI Logic Corporation.

Circle 900 on reader service card

INTRODUCING OUR 1986 COMPACTS.

0-50,000 IN 0.7 NSEC.

ELECTRONICS WEEK

JAPAN'S IC SURPLUS WITH U.S. FELL 55%

Japan's trade surplus with the U.S. in integrated circuits totaled just over $400 million last year, down 55% from the record 1984 surplus of $887.6 million, according to Ministry of Finance statistics. Japanese IC exports to the U.S. dropped 41% to $934 million, while imports of U.S. ICs fell 23% to $534 million.

NTT's FOREIGN BUYS UP 5% IN 1985

Nippon Telegraph & Telephone Corp. bought $157.4 million worth of foreign-made equipment in fiscal 1985, an increase of only 5% over the previous year. The Tokyo giant's purchases of U.S. equipment were $136.1 million, an increase of about $1 million. Those figures do not include an estimated $225 million, five-year deal with Northern Telecom Inc., Nashville, Tenn., for telephone switching systems, which will take effect in 1989.

SHARP, RCA DELAY JOINT CHIP PLANT

The joint chip-making venture between RCA Corp. and Sharp Corp., called RCA/Sharp Microelectronics, is delaying construction of its $250 million plant in Camas, Wash., for several months while the partners review the implications of RCA's acquisition by General Electric Co. Neither side expects the project to be canceled, however.

MOVE TO GET ANSI OK FOR ESDI STALLS

A move to promote the 10-Mb/s Enhanced Small Disk Interface as an industry standard seems stalled. The reason: the standard still requires timing improvements to support tape and optical drives as well as Winchesters, says H. Dal Allen, vice chairman of the American National Standards Institute's committee X3T9.3 on floppy and hard disks. While Allen terms ESDI a brilliant solution to high-speed data transfer for small Winchesters, he says the standard is still so loose that ANSI consideration now would be more likely to slow than to speed its acceptance.

DAISY SYSTEMS SEES SLOW SALES

Daisy Systems Corp., the Mountain View, Calif., workstation manufacturer, is curtailing its product line and laying off 100 workers because of declining orders. Daisy says sales in its first fiscal quarter, ended Dec. 31, leveled off at $36.6 million, and second-quarter sales are expected to be even lower. Daisy has restricted its product focus to three-dimensional computer-aided engineering systems, abandoning its Vulcan line of mechanical CAE products.

COMPANIES OFFER CD-ROM FORMAT

Sony Corp. and Philips of the Netherlands, joint developers of Compact Discs, have developed tentative specifications that define a format for the use of compact-disk read-only memories in handling speech, high-fidelity audio, still and animated pictures, graphics, and computer data. The proposed CD Interactive Media Standard calls for a total data capacity of 650 megabytes per CD. Philips and Sony expect to complete final details of the specification in the next few months.

SEARS TO MARKET FRANKLIN PRODUCT

Franklin Computer Corp., Philadelphia, just one year out of its reorganization under Chapter 11 bankruptcy laws, says Sears Roebuck & Co., Chicago, has agreed to test-market Franklin's enhanced ACE 2100 computer. Franklin says the Apple II-compatible machine, with standard 384-K bytes of random-access memory (expandable up to 576-K bytes), will be sold in Sears stores in New York, New Orleans, and the Pacific Northwest.

IBM TAKES 30% IN BRAZIL VENTURE

In an unprecedented move for IBM Corp., its IBM Brazil subsidiary plans to take a minority position in a new teleprocessing services company. IBM will own 30% of Gerdau Servicos de Informatica SA, with the rest owned by the Gerdau group, Brazil's largest private steel maker. Observers see IBM's move as a way to gain a favorable position in the Brazilian market when an eight-year ban on importing computer-related equipment expires in 1992.

DECWORLD DRAWS 20,000 VISITORS

Digital Equipment Corp. kicked off its Decworld '86 extravaganza in Boston with news of a new four-cable wiring strategy for data, voice, and video transmission. An enhanced software package for integrating IBM Corp. Personal Computers into DEC's networks was also announced, along with other networking products. More than 20,000 people attended the one-company show, which filled 75,000 ft^2 with 200 computers and other equipment, according to DEC estimates.

UCCEL TO SELL EUROPE OPERATION

Continuing its plan to concentrate exclusively on the software business, Uccel Corp., Dallas, expects to complete the sale of its European computing services operations to Inspectorate International SA by the first of April. Included in the proposed sale are Uccel's Automation Center International subsidiary in Zurich, Switzerland, and University Computing Co. in England. Inspectorate, of Neuchâtel, Switzerland, will pay an undisclosed amount for the operations, which contributed about $38 million to Uccel's 1985 revenue of $205 million. Uccel will continue to operate its International Software Division in London.

DATAPOINT ANNUAL MEETING DELAYED

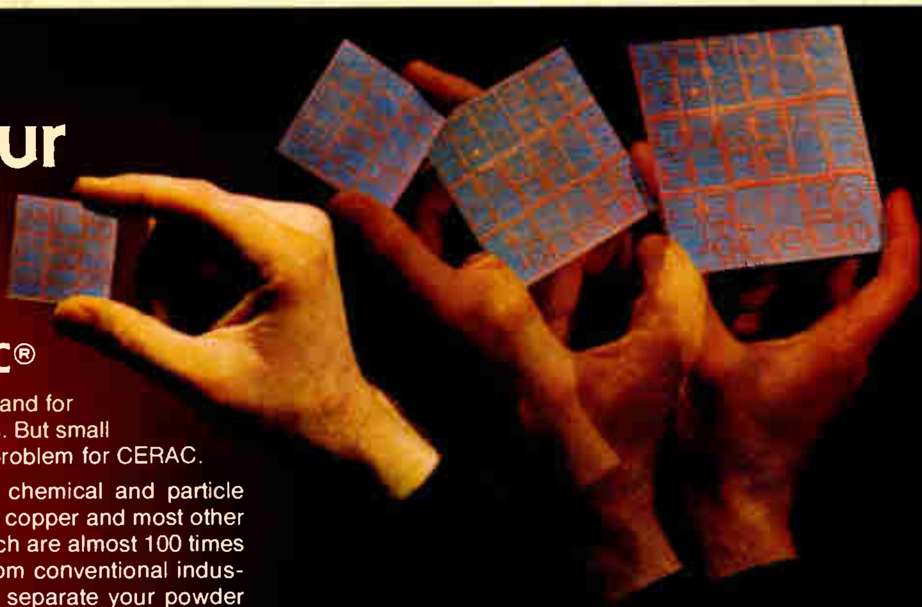
No timetable has been set for Datapoint Corp.'s postponed stockholders' meeting, which had been set for early this month. The meeting was delayed to allow an investor group, led by chairman Asher B. Edelman, time to negotiate financing for a proposed leveraged buyout of the troubled San Antonio, Texas, computer maker. Datapoint reported a net loss of $8.4 million in the quarter that ended Jan. 25, compared with a $15.9 million loss a year ago.

CIRCUIT PIONEER LAMB DIES AT 85

James J. Lamb, an electronics pioneer who invented a basic noise-silencing circuit, died last month in Cupertino, Calif., at 85. Lamb worked for both Remington Rand and Sperry Univac and was at one time chief scientist for the U.S. Army Electronics Command at Fort Huachuca, Ariz. In 1980, *Electronics*, in its 50th anniversary issue, named Lamb's silencing circuit one of the dozen great circuits basic to the commercialization of radio, TV, and computers.

HONEYWELL SELLS CABLE UNITS

Honeywell Inc. has agreed to sell its computer cable and subassembly manufacturing operations to Southwest General Industries, Vista, Calif. Under the deal, Honeywell will buy about $100 million worth of products from SGI over the next five years.



Re-fine your circuitry

with Low-Micron Powders from CERAC®

As printed circuits shrink, the demand for sub-micron copper powder grows. But small particle size powders are no big problem for CERAC.

Through a variety of proprietary chemical and particle sizing techniques, we can reduce copper and most other materials to low micron sizes which are almost 100 times smaller than typically available from conventional industrial manufacturers. We can also separate your powder into various size categories and provide you with a complete particle size distribution curve.

What's more, our Certificate of Analysis, detailing the results of our X-ray diffraction, spectroscopy, and wet chemical analyses, guarantees a purity you can count on.

Ask for our "Low-Micron Powder Sheet". Then try our powder for size. We think you'll find it measures up.

When small particles make the big difference.

CERAC® incorporated

P.O. Box 1178 • Milwaukee, Wisconsin 53201 • Phone: 414-289-9800 • Telex: 269452 (CERMIL)

Circle 71 on reader service card

20th BIAS International Automation Instrumentation Conference and Exhibition

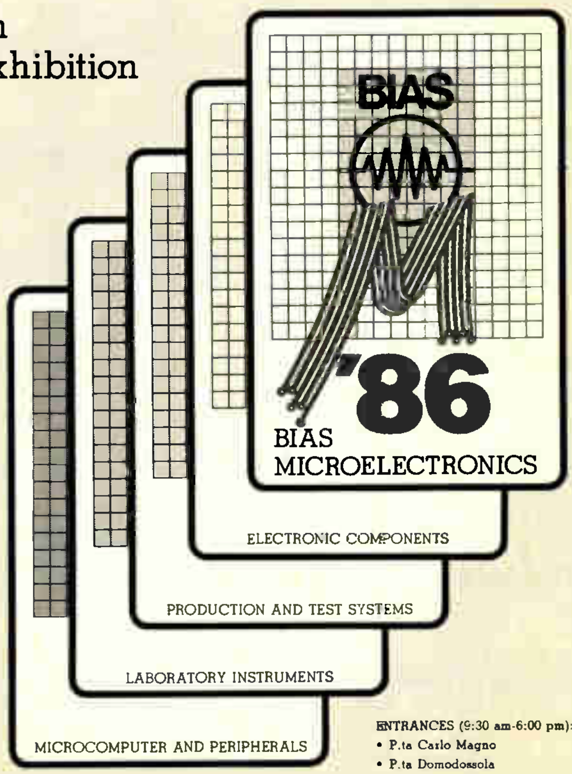
1986 devoted to edition MICROELECTRONICS

18th-22nd March 1986

Milan Fair - Italy

More than 1200 exhibitors
75.000 visitors expected

E.I.O.M. Ente Italiano Organizzazione Mostre
Segreteria della Mostra
Viale Premuda, 2 - 20129 Milano (Italy)
Tel. (02) 54.00.196-135-471 - Telex 334022 CONSEL I



ENTRANCES (9:30 am-6:00 pm):
- P.ta Carlo Magno
- P.ta Domodossola

Circle 82 on reader service card

AI TO DOMINATE OPTICS SYMPOSIUM

Booming interest in optical applications of artificial intelligence will double the size of last year's most popular conference at the Society of Photo-Optical Instrumentation Engineers' Symposium Southeast on Optics and Optoelectronics. Applications of Artificial Intelligence III will have 96 papers—far more than any of the other 10 conferences and double 1985's total, according to conference chairman John F. Gilmore. Gilmore expects a corresponding doubling of attendance at the conference, the largest draw at 1985's symposium.

Gilmore, who heads the AI branch of the Georgia Institute of Technology's Research Institute, says that the large number of applications to be discussed gives this meeting an edge over other AI conferences. Papers will describe products and systems that are "either being used or going to be used."

Predictably, many of the papers describe expert systems or knowledge-base systems, many of which focus on image understanding and processing. But within that focus is an area that took the organizers by surprise in the amount of interest it generated. An entire session will be devoted to papers that discuss the topic of "evidencing" as it applies to image reconstruction.

Evidencing tries to come up with an image based on incomplete data, explains Gilmore. For example, he says, evidencing would try to ascertain the presence of an airplane if it detected only wings and a tail.

Many of the technologies can have military applications—radar, expert-system control of a tank, or combat systems. But Gilmore also sees industry uses such as vision systems and pattern recognition for robotics. The conference will draw "a real mix of industry, military, and academia," he says.

OAC '86, Federation of Information Processing Societies Inc. (1899 Preston White Dr., Reston, Va. 22091), Astrohall, Houston, March 24-26.

Systems I, Computer and Business Equipment Manufacturers Association *et al.* (Society of Manufacturing Engineers, 1 SME Dr., Dearborn, Mich. 48121), Chicago Hilton and Towers, Chicago, March 24-26.

Washington Ada Symposium, IEEE Computer Society *et al.* (Connie Finley, Johns Hopkins University Applied Physics Laboratory, Johns Hopkins Rd., Laurel, Md. 20707), Johns Hopkins University, March 24-26.

Spring National Design Engineering Show & Conference, American Society of Mechanical Engineers (Show Manager, Spring National Design Engineering Show, 999 Summer St., Stamford, Conn. 06905), McCormick Place, Chicago, March 24-27.

Artificial Intelligence '86, Singapore Science Council (John Tagler, 52 Vanderbilt Ave., New York, N. Y. 10017), Hyatt Regency Hotel, Singapore, March 24-27.

IMTC/86: IEEE Instrumentation and Measurement Technology Conference, IEEE (Robert Myers, Conference Coordinator, 1700 Westwood Blvd., Suite 101, Los Angeles, Calif. 90024), Hilton Harvest House, Boulder, Colo., March 25-27.

Symposium Southeast on Optics and Optoelectronics, Society of Photo-Optical Instrumentation Engineers (SPIE, P. O. Box 10, Bellingham, Wash. 98227-0010), Sheraton Twin Towers, Orlando, Fla., March 31-April 4.

1986 International Reliability Physics Symposium, IEEE (Lucian A. Kasprzak, IBM Corp., 44 S. Broadway, White Plains, N. Y. 10601), Anaheim Marriott Hotel, Anaheim, Calif., March 31-April 4.

Comdex/Winter, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Convention Center, Los Angeles, April 1-3.

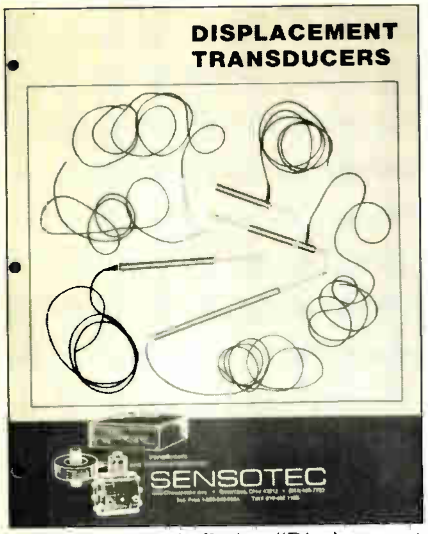
1st International Conference on Expert Database Systems, IEEE (Gio Wiederhold, Stanford University, Dept. of Computer Science, Stanford, Calif. 94305), Charleston Sheraton, Charleston, S. C., April 1-4.

Management and Information Technologies, Data Processing Management Association and Association for Computing Machinery (Doris Dodge, Conference Manager, DPMA, 505 Busse Hwy., Park Ridge, Ill. 60068), Expo Center, Chicago, April 2-4.

Communications Tokyo '86, Communication Industries Association (Sankei Bldg. Annex, 1-7-2 Otemachi, Chiyoda-ku, Tokyo 100, Japan), Tokyo International Fairgrounds, April 2-5.

Future of Software Protection Symposium, Software Engineering Institute and University of Pittsburgh Law Review (Carol Biesecker, Software Engineering Institute, Carnegie-Mellon University, Pittsburgh, Pa. 15213), Software Engineering Institute, Pittsburgh, April 4-5.

29th IPC Semi-Annual Meeting, Institute for Interconnecting and Packaging Electronic Circuits (IPC, 3451 Church St., Evanston, Ill. 60203), Sheraton Hotel, Boston, April 6-10.



LVDTs. A free bulletin, "Displacement Transducers," describes two series of linear variable-differential transducers. The PLV and S5 series are designed for single and multipoint industrial gauging applications; they also measure microdisplacement in scientific instrumentation. Copies are available from Sensotec Inc., 1200 Chesapeake Ave., Columbus, Ohio 43212; phone (614) 486-7723. [Circle reader service number 421]

CMOS INTERFACES. This 416-page data book, the first to be published by VTC Inc., features CMOS A. C. T. (Advanced low-power Schottky speed, CMOS power, TTL drive) interfaces; linear signal-processing circuits; and bipolar semicustom cell libraries. The applications sections include product characterization, test and correlation procedures, and tips for good system design and layout. To order the free publication, call (800) 882-2667 or write the Marketing Department at 2401 E. 86th St., Bloomington, Minn. 55420. [Circle 422]

ETCHING SAFETY. A free two-page application bulletin discusses the detection and measurement of process-gas leaks in a dry-etching operation. Employee safety, alarm levels, and recommended monitoring points are among the subjects covered. For a copy of bulletin no. 970712, contact MDA Scientific Inc., 405 Barclay Blvd., Lincolnshire, Ill. 60069, or call (800) 323-2000; in Illinois, (312) 634-2800. [Circle 423]

PARALLEL PROCESSING. *Parallelogram*, a quarterly newsletter on parallel processing and multiprocessing, has just debuted. The first issue, January 1986, includes an interview with David Kuck of the University of Illinois, Urbana, on software for parallel computing, and an article on a computer-aided engineering application from Shiva Multisystems Corp. *Parallelogram* is free from Sequent Computer Systems Inc., 15450 S. W. Koll Pkwy., Beaverton, Ore. 97006; phone (800) 854-0428. [Circle 426]

TANTALUM CAPACITORS. A 128-page handbook discusses tantalum capacitors with working voltages of 1.5 to 900 V dc. The components range in size from less than 3.6 mm^3 to more than 70 cm^3. The handbook, which contains tables, charts, graphs, and diagrams, comes free from the Steatite Group, Hagley House, Hagley Rd., Birmingham, England B16 8QW; phone (021) 454-6961. [Circle 424]

JEDEC STANDARD. The Electronic Industries Association has released Jedec Standard No. 12-2, "Standard for Cell-Based Integrated Circuit Benchmark Set." The JC-44-2 Committee on Cell-Based Integrated Circuits, which developed the standard, was chaired by William Huber of General Electric Co. Copies are available from the EIA Standard Sales Office, 2001 Eye St. N. W., Washington, D. C. 20006, for $14. Phone (202) 457-4981. [Circle 425]

CATALOGS. The following companies are making available product catalogs, which are free unless otherwise noted:
Aremco Products Inc., 23 Snowden Ave., P. O. Box 429, Ossining, N. Y. 10562. Phone (914) 762-0685. Production equipment. [Circle 450]
Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752. Phone (617) 481-3700. Microcomputer I/O products. [Circle 451]
Hitachi America Ltd., Semiconductor and IC Division, 2210 O'Toole Ave., San Jose, Calif. 95131. Phone (800) 842-9000, ext. 6809. Designer's Selection Guide, Literature No. R15. [Circle 452]
ILC Data Device Corp., 105 Wilbur Pl., Bohemia, N. Y. 11716. Phone (516) 567-5600. Short-form catalog of data converters and MIL-STD-1553 products. [Circle 453]
Kulicke and Soffa Industries Inc., 507 Prudential Rd., Horsham, Pa. 19044. Phone (215) 674-2800. Semiconductor assembly systems. [Circle 454]
Kyocera International Inc., Electronic Components Group, 11425 Sorrento Valley Rd., San Diego, Calif. 92121. Phone (619) 454-1800. Oscillators. [Circle 455]
Leecraft Manufacturing Co., 21-02 44th Rd., New York, N. Y. 11101. Phone (718) 392-8800. LED optoelectronic products. [Circle 456]
Magnetics, Components Division, 900 E. Butler Rd., P. O. Box 391, Butler, Pa. 16003. Phone (412) 282-8282. Catalog FC-405SFP, ferrite cores for power and filter applications. [Circle 456]

Advertisers Index

▪ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
• Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition

Electronics

THE ADVERTISERS AUDIT STUDY CONTEST

Enter a drawing for $1,000 cash by selecting your favorite ads in the March issue of *Electronics.*

Reader Contest Rules

1. After you have examined this issue of *Electronics*, pick your three favorite ads and enter your selections on the entry blank bound in this issue or on a 3" x 5" index card. Your entry should include: 1) the name of the advertiser; 2) the advertiser's Reader Service Number; 3) the page number the advertisement appears on; and, 4) if you would like, your comments explaining what you like most about the ads you selected. Ads placed by McGraw-Hill, Inc. should not be considered in this contest.

2. Check the box on the entry blank marked "Reader Contest." No more than one entry *per issue* may be submitted by any one individual. All entries must be postmarked no later than midnight, April 18, 1986. The winner will be notified in May, 1986.

3. The winner of the $1,000 cash prize will be selected in a random drawing from among all eligible entries. Winner will be notified by mail. Odds of winning depend on the number of entries received.

4. No purchase necessary. Contest void where prohibited or restricted by law. Liability for any taxes on the $1,000 cash prize is the sole responsibility of the winner. Employees of McGraw-Hill, Inc., its advertising agencies, and their families are not eligible to participate.

Advertiser Contest Rules

1. All advertising and marketing personnel in companies and agencies (other than McGraw-Hill, Inc. and its advertising agencies) are invited to participate in a separate contest for advertisers. All rules for the Reader Contest will similarly apply for this contest, with two exceptions: 1) the winner of the Advertiser Contest will *not* be selected in a random drawing from among all eligible entries; and 2) the box on the entry blank marked "Advertiser Contest" must be checked.

2. Examine the March issues of *Electronics* with extra care. Choose the three ads in each issue that you think readers of *Electronics* will pick as their favorites and enter your selections on the entry blanks bound in each issue or on a 3" x 5" index card. No more than one entry *per issue* may be submitted by any one individual.

3. All entries must be postmarked no later than midnight, April 18, 1986. Each individual's qualifying entries will be matched against the winning ads as determined in the Reader Contest. Whichever individual in this Special Advertiser Contest comes closest to picking the 15 winning ads for the month of March, 1986 will receive: 1) $1,000 cash; 2) one free full-page ad in *Electronics* for their company or client; and 3) a plaque acknowledging their skill in evaluating advertising. McGraw-Hill, Inc. reserves the right to schedule the free ad at its discretion.

4. This special Advertisers Contest is open to all advertising and marketing personnel in companies and agencies (other than McGraw-Hill, Inc. and its advertising agencies), whether or not their companies or agencies have an advertisement in the March, 1986 contest issues.

5. No purchase necessary. Contest void where prohibited or restricted by law. Liability for any taxes on the $1,000 cash prize is the sole responsibility of the winner. Employees of McGraw-Hill, Inc., its advertising agencies, and their families are not eligible to participate.

Winning Advertisers Earn Free Ad Reruns

The three advertisers receiving the most votes in each March 1986 issue of *Electronics* will receive a free rerun of their winning ads and a plaque commemorating their achievement. Since there are five issues of *Electronics* in March, there will be a total of 15 winning ads.

After all the March Reader Contest ballots are received, the three ads that scored the highest over the course of the entire contest will be determined and announced in May, 1986. These three Grand Prize Winners will receive a special plaque, plus a free rerun in *Electronics* of *all* the ads they ran in *Electronics* during the entire month of March.

All reruns will be made from existing plates or negatives. If the advertisement qualifying for a free rerun is an insert, the winner may run up to a four-color, two-page spread on R.O.P. stock from existing plates or negatives. McGraw-Hill, Inc. reserves the right to schedule reruns at its discretion.

WIN $1,000 CASH ADVERTISER AUDIT

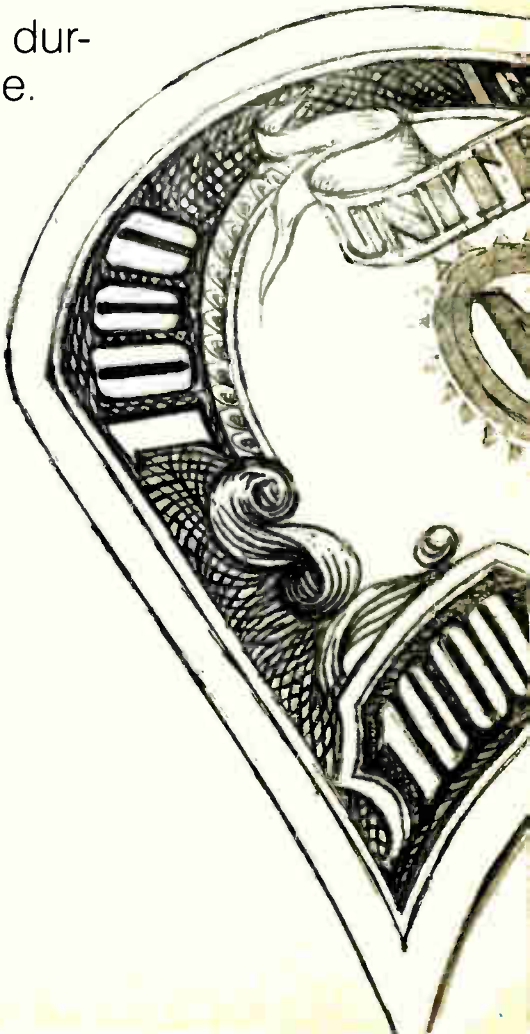
Electronics' unique new contest makes it easy to win big.

The rules are simple. Each issue this month contains a ballot asking you to select your three favorite ads in the issue. All you do is fill in your choices and drop it in the mail. Your returned ballot or reasonable facsimile is automatically entered in the prize drawing at the end of the month. If your name is drawn at random, you win one thousand easy dollars.

Ads receiving the most votes each week and during the course of the contest will be rerun for free.

You can win money *and* let advertisers know what you think of their selling messages. Advertisers can win extra insertions.

So watch for contest ballots and rules in each March issue. And get ready to win big this month.



ADVERTISERS: YOU CAN WIN $1,000, TOO!

All advertising and marketing personnel in companies and agencies are invited to participate along with our readers by filling out a special Advertisers Ballot included in each March issue. Whoever comes closest to picking the 15 winning ads for the month (3 from each issue) in this special Advertisers Contest will receive an award for skill in evaluating advertising, plus a free ad insertion for his or her company, and $1,000 cash!

The Contrast Tells the Story.

Brand New LCD From Sharp

With contrast up to 7.0 and viewing angle from −10° to +45°, it's twice as easy to see why LCD readability can now be twice as good for your portable computers and OA equipment. The demand for this LCD is expanding rapidly — due to Sharp's success in improving LCD performance in direct response to market demand.

IBM PC® Compatible LCD Monitor

This new LCD monitor comes with an RGB video signal interface cable, completely eliminating the cost and time needed to design and develop an interface to IBM PC® or PC clones. This monitor enables you to instantly display your PC software on our 640×200 LCD by just plugging the RGB interface cable into an IBM PC® or PC clone.

Type No.	LM64014W	LM64016W
Dot pitch ratio	1:1.4	1:2
Type	Reflective Type	Reflective Type
Contrast	7.0(TYP.)	7.0(TYP.)
Viewing angle	−10～+45°(Co≥2,TYP.)	−10～+45°(Co≥2,TYP.)
Unit outline dimensions W×H×D(mm)	256×128×13.3	256×164×13.3
Display format(W×H)	640×200	640×200

* Compared with earlier Sharp models.

SUPER TWISTED HIGH CONTRAST LCD

NOW AVAILABLE

※ LM64014W

LM64016W

● IBM PC is a trademark of International Business Machines Corporation.

※ Screen image printed with permission of Micropro International Corporation

SHARP

SHARP CORPORATION, JAPAN

SHARP CORPORATION International Sales Dept. Electronic Components Group.
22-22, Nagaike-cho, Abeno-ku, Osaka 545, JAPAN Tel: (06)621-1221 Cable: LABOMET OSAKA Telex: J63428 Attn: OSKPA(LABOMET A-B)
U.S.A.:SHARP ELECTRONICS CORPORATION Electronic Components Division.
Sharp Plaza, Mahwah, New Jersey 07430 Tel: 201-529-8200 Telex: 426903(SHARPAM PARA)
EUROPE:SHARP ELECTRONICS(EUROPE)GMBH Electronic Components Dept.
Sonninstrasse 3,2000 Hamburg 1, F.R. Germany Tel: (040)23775-0 Telex: 2161867(HEEG D)

Circle 65 on reader service card

resolution of 640 horizontal by 350 vertical pixels and builds characters in an 8-by-14-dot matrix. It also includes a parallel port. Both are available now.

Paradise Systems Inc., 217 E. Grand Ave., South San Francisco, Calif. 94080.
Phone (415) 588-6000 [Circle 366]

CONTROLLER LINKS FOUR DRIVES TO PC/XT

A disk-controller board, model SMC4012-PC, is plug-compatible with the IBM Corp. Personal Computer XT's bus and controls two Winchester disk drives through the ST506 interface. At the same time, the board can control two floppy-disk drives through the SA-450 floppy interface.

This combination of drives on a single board frees one board slot and reduces power requirements in the PC/XT. The SMC4012-PC handles error detection and correction as well as on-board data separation. Prices were unavailable.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 273-3100 [Circle 365]

FAST ADCs MEET MIL-STD-883 SPECS

A 12-bit analog-to-digital converter guarantees a maximum conversion time of 4.5 μs over the entire military temperature range; a second, less expensive model that also meets MIL-STD-883

specifications converts in 6 μs.

The AD578TD and AD578SD are complete successive-approximation ADCs requiring no external components. The parts differ in their gain, unipolar, and bipolar offset drift. A buried zener reference specified at +10 V, ±100 mV, can be used to drive maximum loads of ±1 mA. Power dissipation is 775 mW.

The ADCs have both parallel and serial data outputs. Packaged in hermetic 32-pin ceramic DIPs and processed to MIL-STD-883 level B, method 5008, the AD578TD sells for $205 and the AD578SD for $165.

Analog Devices Inc., Literature Center, 70 Shawmut Rd., Canton, Mass. 02021
[Circle 362]

PROCESSOR IC CYCLES IN 150 NS

Signetics' new 150-ns 8X401 microcontroller is the centerpiece of a new family that is a successor to the company's 8X305 family. The ECL 8X401 is 35% faster than the earlier model, thanks in part to an expanded instruction set: the 8X401 has 32 fixed instructions, compared with 16 for the 8X305.

The chip employs the Harvard parallel-path architecture. In one 150-ns cycle it can fetch, execute, and generate the next instruction address for a 20-bit instruction. Then, within one instruction cycle, the 8X401 can be programmed to enter, merge, rotate, and mask single- or multiple-bit subfields, in addition to performing an arithmetic or logic operation.

An 8-bit bidirectional data-address bus and a signal-I/O control and timing bus gain access to peripheral devices. Three independent I/O banks can address up to 256 locations each. The 8X401 is available from stock, in a 64-pin Cerdip, for $99.95 in lots of 1 to 10. It will be offered in a 64-pin plastic DIP and a 68-pin plastic leaded chip carrier by midyear.

Signetics Corp., 811 E. Arques Ave., P. O. Box 3409, Sunnyvale, Calif. 94088.
Phone (408) 991-2000 [Circle 350]

ECL ARRAY HITS 5,000-GATE COUNT

Two ECL gate arrays offer densities of 5,000 gates—the model μPB6350—and 4,000 gates—the model μPB6340. The high densities are possible because the designers have solved the heat-dissipation and power-consumption problems encountered in high-density ECL, the company says.

Both arrays feature a delay time of just 0.7 ns per gate. The devices will find applications in minicomputers, parallel processors, IC testers, and high-speed communications equipment. They are offered in 132- and 208-pin ceramic pin-grid arrays with heat sinks.

Unit prices are $206 for the μPC6350 and $167 for the μPC6340, in quantities of 5,000.

NEC Electronics Inc., 401 Ellis St., P. O. Box 7241, Mountain View, Calif. 94039.
Phone (415) 960-6000 [Circle 352]

SCOPE CONTAINS THERMAL PRINTER

The model SE 571 Digitalscope has a built-in thermal printer that delivers a hard copy of all the information from its CRT in 10 seconds, including the measurement protocol. The scope itself is an autoranging instrument with two chan-

nels, each displaying signals of up to 10 MHz. For digital-circuitry analysis, the SE 571 provides up to eight logic channels; the user can program eight signal-parameter settings.

With a maximum sweep frequency of 25 MHz, the scope's display is fast enough to capture changing waveforms, creating the effect of an analog oscilloscope. The SE 571 sells for $6,500 and will be available next month.

BBC-Metrawatt/Goerz, 2150 W. Sixth Ave., Broomfield, Colo. 80020. Phone (800) 821-6327; in Colorado, (303) 469-5231
[Circle 356]

DIGITAL THERMOMETER WORKS IN FIELD

Fluke is entering the handheld digital thermometer market with a family that is built to withstand rough treatment in the field. Typical battery life for the 50 series is 1,200 hours. An offset potentiometer for each J- or K-type thermocouple input allows field calibration to a given temperature.

Accuracy is within ±0.1% over an ambient operating range of 18°C to 28°C, with a resolution to within 0.1°C.

The model 51 sells for $119. The model 52, which provides differential information, goes for $189. Both are available now.

John Fluke Mfg. Co., P. O. Box C9090, Everett, Wash. 98206.
Phone (206) 347-6100 [Circle 367]

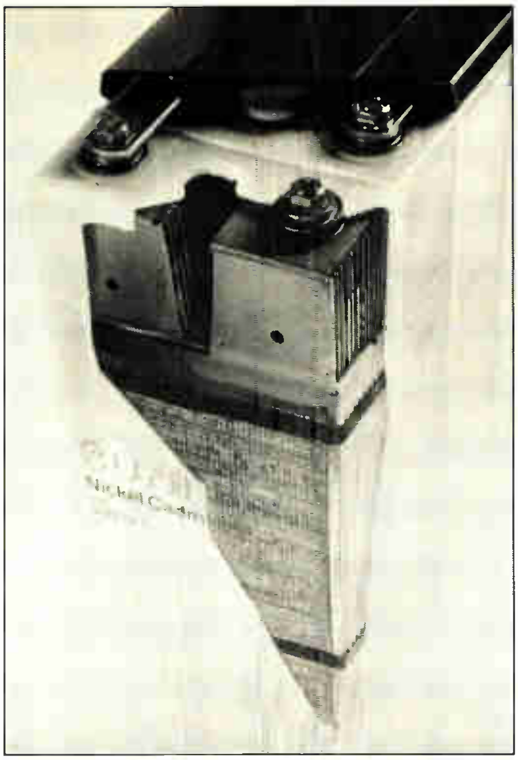
EPROM ACCESSES DATA IN 110 NS

With an access time of 110 ns, a 128-K EPROM clips 40 ns off the record of its predecessors. The 27128B-110V05 is built in Intel's HMOS II-E process. A smaller die reduces data-access time, the company says, while the size of the active area of the EPROM cell remains unchanged because HMOS II-E eliminates unused areas of the EPROM array. The EPROM, housed in a windowed 28-pin ceramic DIP, is priced at $13.30 in lots of 1,000.

Intel Corp., Literature Dept. W-278, 3065 Bowers Ave., Santa Clara, Calif. 95051
[Circle 361]

plates and connectors do not react with the alkaline electrolyte and do not corrode, causing "sudden death." The battery also is immune to acid stratification—the active chemicals do not precipitate out.

And although a comparably rated lead-acid battery is about two to five times cheaper than the Sunica, a photovoltaic system using the nicad battery will cost less initially and remain less costly to maintain, says Arne O. Nilsson, director of international projects. This is because a voltage regulator is not needed, and in many applications a lower-capacity nicad battery can replace a higher-rated lead-acid one. The Sunica costs about $300 per kWh.



IN THE POCKET. SAB Nife's nicad battery uses pocket-plate technology to end the memory-effect problem.

Specified for –50°C to +55°C, the battery survives undercharging in cold locations and overcharging in heat. A potassium hydroxide electrolyte survives temperature extremes and, unlike lead-acid batteries, presents no sulfation—progressively reduced capacity—when continually discharged to below 70%. Thus where lead-acid batteries must be oversized by as much as 50% to compensate, the Sunica does not.

The overall charge-discharge efficiency of most lead-acid batteries is from 80% to 85%. The Sunica battery, by contrast, returns 89% to 99% of the energy put into it.

SAB Nife also claims the Sunica beats the lead-acid battery in maintenance. Its electrolyte must be topped off once every 10 years. This is particularly important for remote sites, where servicing a lead-acid battery every two or three years can cost more than the battery itself, Nilsson says. Sunica batteries can be stacked safely because there are no live parts on top. Another safety feature is a spill- and explosion-proof venting system.

MEMORY EFFECT. The Sunica's pocket-plate technology eliminates the memory effect that plagues sinter-plate nicad batteries—that is, after numerous well-defined charge-discharge cycles, the batteries "remember" their former state when used at another cycle. When tested in satellites, sinter-plate batteries were run at full capacity after repeated cycling at the 25% discharge level, and it was found that they produced voltage plateaus—a much higher level for the first 25% of the time.

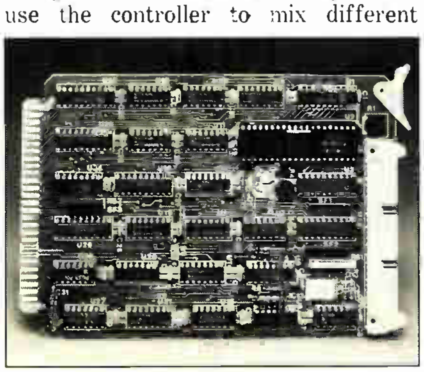
Thanks to an iron-based active material in the Sunica cadmium electrode, the pocket-plate batteries do not suffer from this effect under any conditions, the company says. And because pocket plates cannot be destroyed by over- or undercharging, voltage regulators are not necessary.

Capacities range from 11 to 1,100 Ah, and the company will quote prices. The Sunica battery can be delivered in about eight weeks. *–Ann Jacobs*

SAB Nife Inc., George Washington Hwy., P. O. Box 100, Lincoln, R. I. 02865.
Phone (401) 333-1170 [Circle 340]

CONTROLLER MIXES DRIVE SIZES, FORMATS

Designed for the STD bus, the FLP-380 provides an interface for up to four 5¼-, 3½-, or 8-in. floppy-disk drives. Because all read, write, and format functions are configured in software, the designer can use the controller to mix different drives and formats in the same system.



Complete development systems and tools for the FLP-380 are available, and software support includes the CP/M 2.2 and MP/M operating systems. The controller costs $232 in original-equipment-manufacturer quantities, with a CMOS version going for $252. Delivery is from stock but can take up to 30 days.

Computer Dynamics Inc., 105 S. Main St., Greer, S. C. 29651.
Phone (803) 877-7471 [Circle 364]

8-MHz BOARD RUNS UNIX ON VMEbus

The 68010-based CPU-3 runs the AT&T Co. Unix operating system on the VMEbus for Unix development or production systems or in multiuser engineering work stations. For memory-management tasks, the CPU-3 uses a 68451 chip, which can be bypassed for more efficient CPU throughput. Also accelerating process execution is a no-wait-state static RAM. Local functions are under software control, and programmers can reconfigure system-design parameters on the fly.

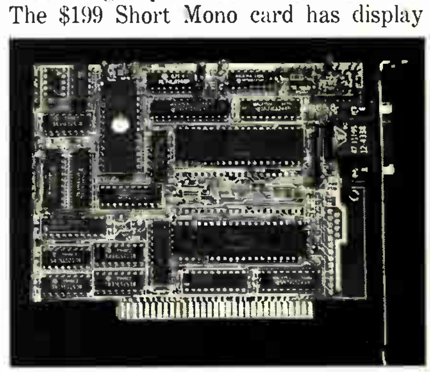
The 8-MHz CPU-3A, with 32-K bytes of RAM, sells for $2,195 each. The CPU-3B—running at 10 MHz and with 128-K bytes of RAM—is $2,845. Delivery takes 30 days after ordering.

Force Computers Inc., 727 University Ave., Los Gatos, Calif. 95030.
Phone (408) 354-3410 [Circle 363]

GRAPHICS CARDS FIT IN IBM PC'S SHORT SLOT

Two graphics products, the Short Color Card and the Short Mono Card, are short-slot replacements for the IBM Corp. color and monochrome graphics display adapters in the Personal Computer, PC/XT, and PC AT. These replacement cards will run all the PC software that IBM supports.

The short color card, which sells for $179, provides flicker-free scrolling and supports both red-green-blue and composite monitors. It has connectors for both a light pen and an rf modulator. The $199 Short Mono card has display



NEW PRODUCTS

TRIQUINT BUILDS A FAMILY OF DIGITAL GaAs PRODUCTS

OFFERINGS INCLUDE STANDARD ICs AND ASICs, PLUS CELL LIBRARY

TriQuint Semiconductor is racing to become a full-line supplier of digital gallium arsenide products. The Tektronix Inc. subsidiary has a line of 3-GHz GaAs medium-scale-integration components based on its Q-Logic depletion-mode standard-cell library. In addition, the company can provide application-specific ICs produced from customers' electrical specifications. And by the third quarter of the year, TriQuint will provide customers with a standard-cell software library so engineers can design circuits on their own work stations.

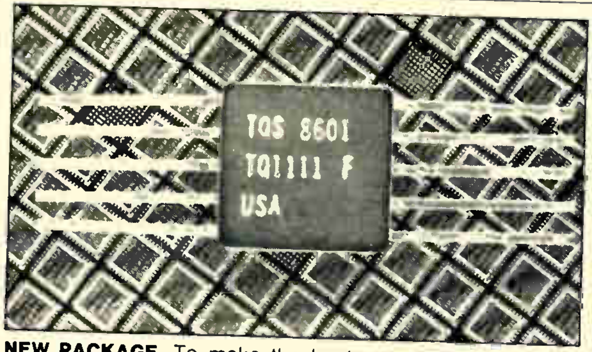
The Q-Logic digital GaAs series, which operates at up to 15 times the speed of silicon CMOS and five times the speed of silicon ECL, is TriQuint's first family of standard MSI components. TriQuint joins a list of about 50 companies offering some type of GaAs products, including GigaBit Logic, which also has GaAs MSI chips; GigaBit Logic's frequency counters and dividers are specified at 2.5 GHz, compared with TriQuint's 3-GHz devices.

Previously, TriQuint offered a semicustom gate array called the Q-Chip, which enabled potential GaAs users to try the high-speed technology. But "a standard product line will encourage more people to try out the logic," says Tom Reeder, marketing manager.

Reeder sees a big market for GaAs as a replacement for ECL in fiber-optic communications systems. "Designers want to go up to 1-Mb/s data rates, double the current speed," Reeder says. "This would allow them to double the number of channels and reduce per-channel costs."

Q-Logic works with an improved GaAs IC-device data base that allows design for a wide range of power-supply voltage and temperature fluctuations. Q-Logic will operate with little change in performance with a power supply that ranges from ±4 to ±5.2 V. Initially, parts will be able to operate from 0°C to +85°C, but will be extended for the military range of –55°C to +125°C. The series is compatible with ECL 10K and 100K over the full range of power-supply and temperature variations.

As with any new technology, reliability is a critical issue. The company says reliability testing of GaAs depletion-mode ICs demonstrates a mean time to failure of more than 10 million hours at 125°C. Because there are no standard testing practices for GaAs circuits yet, TriQuint can't ensure speed, but using silicon testing practices (up to 10 MHz), the company can functionally test the devices. "The parts will reach customers functionally tested and packaged," Reeder says.



NEW PACKAGE. To make the best use of GaAs's speed, TriQuint developed a new multilayer ceramic package.

RIPPLE COUNTER SERIES. The first component available in the Q-Logic series is the TQ1111 4-bit ripple counter series. Designed for use in prescaler and high-speed counting applications, the TQ1111 is available in three models. The TQ1111-20 covers the frequency range up to 2 GHz, the TQ1111-25 extends operation to 2.5 GHz, and the TQ1111-30 handles frequencies up to 3 GHz. The counters consume 1.6 W. The divide-by-2, -4, -8, and -16 outputs are 10K and 100K ECL-compatible and the divide-by-2 stage includes a complementary output to facilitate high-speed circuit interfacing.

Also available now are the TQ1112, a 4-bit synchronous up-down counter that operates at 1 GHz, and the TQ1121, a divide-by-4/5 dual-modulus counter operating at 2 GHz. Soon to be available are a programmable dual-modulus divider, multiplexers, and demultiplexers.

Q-Logic devices can be packaged in commercially available IC flatpacks or in a new, high-performance multilayer ceramic package, designed by TriQuint for extremely high-speed applications. The new package can easily attach to high-speed circuit boards with current manufacturing technology.

The TQ1111 counter series is available 45 days after ordering. In lots of 100 pieces, the TQ1111-20 sells for $89, the TQ1111-25 for $119, and the TQ1111-30 for $199. An evaluation board for the 3-GHz chips will be available for $275.

–Steve Zollo

TriQuint Semiconductor, Tektronix Industrial Park, Group 700, P. O. Box 4935, Beaverton, Ore. 97075. Phone (503) 627-6348
[Circle reader service number 339]

NICAD BATTERY FOR SOLAR CELLS LASTS 20 YEARS

SAB Nife AB is bringing to market Sunica, a nickel-cadmium battery for photovoltaic systems that boasts a longer life, smaller size, and more reliability than its lead-acid counterparts. And with its pocket-plate technology, the Sunica is more reliable than other nicad batteries.

The company notes that developments in photovoltaics technology have made it possible to set up navigational aids, radio repeater systems, and satellite telecommunications systems in a host of harsh and inaccessible places. But the weak link in such systems until now has been the battery used to store the energy captured by solar panels.

The Sunica's lifespan is 20 years, about five times that of a lead-acid battery. Unlike lead-acid batteries, the ting edge of semiconductor manufacturing for telephony applications, he is instead involved with typefaces, fonts, and the paraphernalia of electronic printing. The Corel system includes a personal computer, software in compact-disk read-only memory, and a Ricoh Co. laser printer.

UP AND OUT. The move began with a shove. Soon after British Telecommunications plc, London, announced its intention to acquire 51% of Mitel's stock last May, Cowpland was shuffled upward and out of an active role in the management of the Kanata, Ont., company that he founded in 1973 with partner Terry Matthews. But there were other considerations. "I still have a strong interest in Mitel and I'm still on the board, but I had to get as far as I could from telecommunications," he concedes.

Corel Systems gives the 42-year-old Cowpland, who holds a doctorate in electrical engineering from Carleton University in Ottawa, plenty of room to exercise his entrepreneurial bent. Among Canadians, Cowpland has long had a reputation as a zealous investor in technology, though his successes are less notable than his failures. "He had the reputation of someone who would throw money at anything that moved," says one observer of Cowpland's venture capital career.

Cowpland, for instance, was the organizing force behind Bytec Management Corp., the Ottawa venture capital outfit that developed the Hyperion personal computer and played a big role in seeding and funding many Canadian high-technology startups. Hyperion, an early look-alike to the IBM Corp. Personal Computer, was sunk by problems with its disk drives. Cowpland also took a bath when he poured millions into System House Inc., the Canadian systems-integration company, although it recently received an infusion of new capital.


MICHAEL COWPLAND: A recognized authority in telecommunications, he now heads a startup in electronic publishing.

This time it's different, says Cowpland, adding that the electronic publishing venture was launched only after careful study. First, he surveyed the technological landscape for emerging growth areas and focused on optical-disk manufacturing and electronic publishing. But on closer inspection, he concluded the optical-disk market was too risky and the window of opportunity was closing fast. "We would have needed to start 12 months ago," he says.

However, he found it easier to get an electronic publishing venture off the ground. Cowpland launched Corel Systems for a modest $5 million, and after five months in operation, it has more than 20 beta-test-site units in the field. Plans call for volume shipments to begin this year.

Cowpland is entering an already crowded field, but he is convinced the opportunites are there. "Typesetting with personal computer architecture, CD ROMs, and laser printers will be fertile ground for the next 10 years," he predicts. *–Robert Rosenberg*

PEOPLE

FOR COMPAQ'S CANION, LAPTOP'S TIME IS NOT HERE

HOUSTON

The way the cofounder and president of Compaq Computer Corp., Joseph (Rod) Canion, sees it, the world is not yet ready for the laptop computer. He says laptops have a most difficult hurdle to clear before they can be more widely accepted: the important functional tradeoff between battery operation and screen readability. And other technology advances are necessary, in Canion's view: better flat-panel displays, small mass-storage units, and longer-life battery packs.

ROD CANION: The laptop still must hurdle technological obstacles.

Canion, a 42-year-old Houston native who once worked at Texas Instruments Inc., says that Compaq did dabble for two years with plans to introduce a battery-powered laptop, showing a working prototype to its retail dealers and potential large corporate customers. But Canion, who was the catalyst behind the laptop, pulled the plug because there was little demand.

He insists that today's technology still isn't able to integrate a full-function computer into the profile of a battery-powered laptop unit. "The marketplace is not changing, and people in the business world still want increased functionality from new computers." That philosophy has propelled the company, cofounded by Canion in February 1982, into the rank of second-largest manufacturer of business personal computers behind IBM Corp.

Rather than go the laptop route, Canion decided that the way to stay successful was to make the Compaq Portable, the company's original product, smaller and lighter. That was accomplished last month when the Portable II, which retains full compatibility with IBM's Personal Computer, was unveiled [*Electronics*, Feb. 24, 1986, p. 64].

But the weeks leading up to that carefully orchestrated introduction turned out to be more nerve-wracking than usual for such an event. That's because rumors were circulating throughout the computer industry that IBM was about to introduce its own long-awaited and closely guarded laptop computer, nicknamed Clamshell. An introduction by Big Blue would have upstaged the Portable II and certainly taken some of the thunder away from Compaq's new machine.

"This is going to be a very important product for us, and it comes at an interesting time when many of our larger competitors are talking laptop," notes Canion.

Fortunately for the people in Houston, however, IBM never did take the wraps off Clamshell and the Compaq introduction came off without a hitch.

But Canion, with his MSEE from the University of Houston, remains the restless engineer-businessman. He says that if the giant computer maker introduces a laptop, he intends to have his engineers take a close look for technological surprises. If they find that a full-function laptop computer has been made possible, Canion believes, his company can top IBM's product with a crash design effort in as little as six months.

That statement is more than bravado. Canion has never allowed Compaq to veer off the research track that leads to still-smaller portable computers. "The [laptop] prototype is long gone, but we have also said we are continuing development work. Sooner or later, we will have a portable small enough to call a laptop," says Canion. "But we will begin with what goes in it, rather than drawing a box and filling it with whatever we can." *–J. Robert Lineback*

NOW COWPLAND IS MOVING INTO PRINT

OTTAWA, CANADA

It's not often that a major industry figure breaks completely with his original field and stakes out virgin territory, as Michael Cowpland has done. Cowpland, an innovator in telecommunications equipment and a cofounder, former president, and chairman of Mitel Corp., has forsaken telecommunications to try his hand at electronic publishing.

His new venture, Corel Systems Corp., is a radical change of direction for Cowpland. After 13 years at the cut-

PEOPLE ON THE MOVE

ALFRED C. SIKES

☐ The Reagan administration has nominated Alfred C. Sikes to be Assistant Secretary of Commerce and administrator of the National Telecommunications and Information Administration. If confirmed by Congress, Sikes, 46, will succeed David J. Markey, who left the post last November [*Electronics*, Nov. 4, 1985, p. 64]. The Cape Girardeau, Mo., native is president of Sikes & Associates Inc., a seven-year-old media consulting company in Springfield, Mo. During the mid-1970s, Sikes served as director of Missouri's Department of Consumer Affairs, Regulation, and Licensing and its Department of Community Affairs.

LEONARD S. SHEINGOLD

☐ GCA Corp.'s choice to succeed former chief executive officer Milton Greenberg is Leonard S. Sheingold. Sheingold, who has been a director of the Bedford, Mass., company since 1983, is a former chief scientist for the U.S. Air Force. He also served as vice president of advanced technology for GTE Corp., Stamford, Conn. In addition to taking over as CEO, he will serve as GCA's president, succeeding Richard D. Stewart, who has been appointed vice chairman of the board. Greenberg, who cofounded the company in 1958, will continue to serve as chairman of the board.

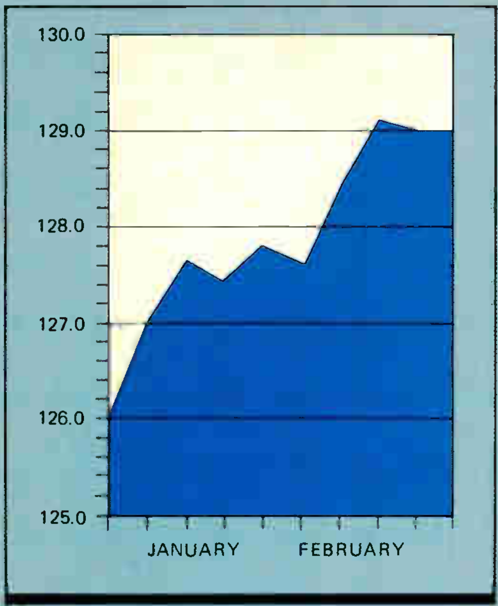
ROBERT E. CALDWELL

☐ Siemens Components Inc. has appointed Robert E. (Ed) Caldwell as senior vice president and general manager of its new Semiconductor Group. Caldwell, 48, comes to the Iselin, N.J., company from Mostek Inc., Carrollton, Texas, where he was senior vice president, engineering and technology. He has also served with Fairchild Semiconductor Corp. and Motorola Inc. in various management positions.

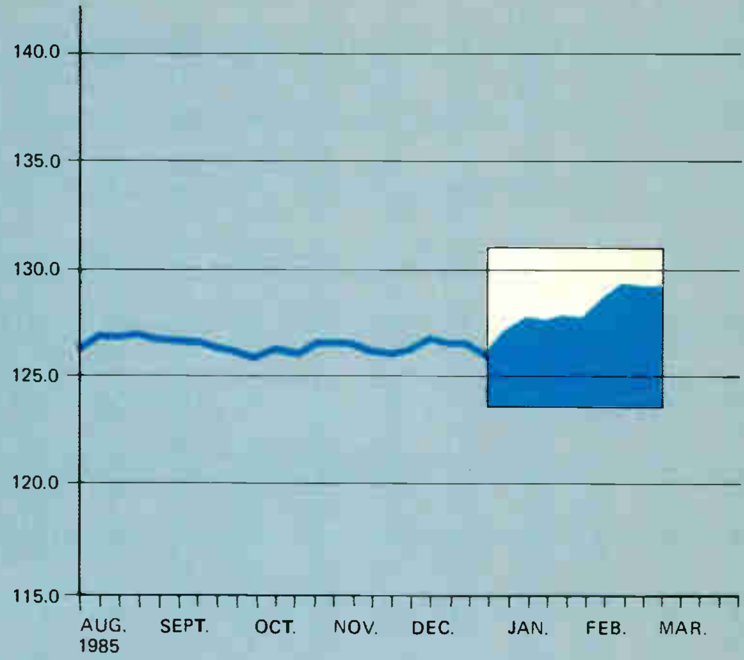
HUGO P. CANNIZZARO

☐ As part of its expansion strategy, Caddex Corp. not only has completed a third round of financing but also has appointed Hugo P. Cannizzaro president and chief executive officer. He replaces founder and former president Alan Higginson, who will serve as chairman of the board for the Woodinville, Wash., manufacturer of electronic technical publishing systems [*Electronics*, Feb. 24, 1986, p. 76]. Cannizzaro was vice president of Western operations for Prime Computer Corp. Before that, he spent 30 years with IBM Corp. in sales, planning, and senior management.

ELECTRONICS INDEX



THIS WEEK = 129.0
LAST WEEK = 129.0
YEAR AGO = 130.9
1982 = 100.0



The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS COMPONENT-PRODUCER PRICE INDEX (1967 = 100)

	January 1986	December 1985	January 1985
Digital bipolar integrated circuits	61.6	60.7	61.1
Digital MOS ICs	30.8	30.9	42.8
Linear ICs	57.1	59.0	61.7
Capacitors	185.8	185.6	192.8
Resistors	189.6	189.4	187.7
Relays	313.1	313.2	319.3
Connectors	237.0	236.6	231.9

U. S. GENERAL ECONOMIC INDICATORS

	January 1986	December 1985	January 1985
Average prime rate (%)	9.50	9.50	10.61
Retail sales ($ billions)	117.501	117.405	110.972
Unemployment rate (%)	6.6	6.8	7.2

Prices of electronic components appear to be firming, according to the latest government figures. Producer prices for components dropped slightly in some categories and increased in others from December to January, translating to no movement in this week's *Electronics* Index.

Prices of bipolar integrated circuits increased 1.5% for the month, bringing them 0.8% higher than levels of a year ago. Capacitors and resistors were also up slightly—0.1%—in January over December. Capacitor prices are still down 3.6% from last January. However, resistor prices are 1% ahead of year-ago levels.

MOS IC prices, still 28% below last year, slipped 0.3% in January. And prices of linear ICs, off 7.5% from their January 1985 level, fell 3.2% in January from December. Relay prices are about the same as the final month of 1985, though they have fallen almost 2% from January 1985, and connector prices are up 0.2% in the month and 2.2% from a year ago.

KONING. His strategy to turn around the consumer electronics giant is working.

around 24,000 by early 1984, just over half that of its heyday in 1979. The cuts instituted under Koning brought the labor force down to the present level of 19,000, and the president says the number "will stabilize at about 18,000 by the end of this year."

Having pruned its work force, Grundig is now going over its product line. A management-worker committee is drawing up proposals for new equipment lines, and the existing product range is being thinned. For example, the number of different color TV models is being slashed by more than half from the 500-odd models two years ago.

ON THE VHS BANDWAGON. Meanwhile, Grundig's inventory of 225,000 Video 2000 recorders has been sold, and the company has suspended production. Like many other European consumer electronic makers, Grundig has jumped on the VHS bandwagon and now turns out VHS models at a rate of 600,000 units a year.

Koning does not exclude the possibility of Grundig someday developing a VCR machine that, using inexpensive components from the Far East, will sell for less than 1,000 Deutschmarks, or about $400 at the present exchange rate. That sum would be 30% to 40% lower than the retail price of VCRs, both foreign and domestic, on the West German market.

Despite its ties to Philips, Grundig remains an independent firm, Koning emphasizes. In product design and development, the two organizations go their own ways and compete in important areas on European markets.

As for himself, Koning leaves no doubt about his allegiance. "I wear a Grundig hat. No one at the company will quarrel with that." *–John Gosch*

Another diversification move now under way is the establishment of a nationwide franchising chain to sell personal computers, a big, untapped market in West Germany. With headquarters in Munich, the chain will comprise about 50 House of Computers stores throughout West Germany within three years and sell personal computers made by such companies as Hewlett-Packard, IBM, Nixdorf, and Philips. "These outlets will give us know-how in the data processing business, know-how that may come in handy in future diversification efforts," Koning says.

EARLY SUCCESSES. Through this diversification, Koning hopes to get the company back on its feet. Founded by Max Grundig in this North Bavarian town in 1946, the company and the man behind it once stood for successful entrepreneurship. During West Germany's "economic miracle" years of the 1960s, Grundig rose to become one of Europe's major and most innovative producers of radios and TVs, ranking No. 2 behind Philips and, in 1979, employing some 40,000 people in dozens of manufacturing plants throughout Europe.

But the Japanese offensive in consumer electronics that began in the 1970s hurt Grundig badly, as it did most U. S. and other European producers. On top of the new competition came harder economic times, with consumers reining in their spending.

As a result, Grundig suffered sluggish sales, fierce price wars, and excess capacity. It also had one major marketing failure, the Video 2000, a video cassette recorder developed jointly with Philips. Though technically on a par with, if not superior to, Japanese-made VCRs, the Video 2000 did not score well in the market. It was incompatible with the Japanese VCRs, and a lack of cassettes prompted consumers to turn to the Japanese products.

Grundig continued its slide until Philips, which bought 24% of Grundig in the 1970s, raised its stake to 31.5% on April 1, 1984, and sent in Koning. The Max Grundig Foundation holds 49.5% of the stock and a group of banks the rest.

Koning has held a number of executive positions at Philips affiliates around the world, the latest as top man in West Germany. There he helped lift the Germany-based group of Philips companies back into profitability. It was this expertise he brought to Grundig.

One of the first measures taken, Koning reports, was to reduce the overhead. With capacity too high and per-worker output too low, the new management team started streamlining operations and cutting the number of workers to achieve higher productivity.

Even before the management change Grundig had slashed its work force to

COMPANIES

GRUNDIG SEES AN END TO ITS RED INK

THE CONSUMER ELECTRONICS GIANT IS DIVERSIFYING EVEN AS IT MOVES TO STRENGTHEN ITS TRADITIONAL BUSINESSES

FÜRTH, WEST GERMANY

Financially troubled Grundig AG still has a way to go before it's out of the red, but president Hermanus Koning is confident he's steering it in the right direction. The 61-year-old Koning is a veteran manager with the Dutch giant Philips, a part owner of the company. Under his leadership, Grundig is shifting more of its focus from consumer electronics into new product areas.

West Germany's largest producer of consumer electronics equipment is forging new alliances and adding product muscle in such new markets as office and factory automation, while continuing to reduce payrolls and streamline operations. It's even starting a chain of stores to sell personal computers.

In the process, the 40-year-old company is trimming its mammoth losses and heading for renewed profitability. "By the end of 1986, we hope to be out of the red," says Koning. To date, he has cut year-to-year losses by about $80 million—from $115 million in April 1984 to an estimated $32 million by April of this year, on sales of roughly $1.2 billion (charts).

STILL THE MAINSTAY. Koning, who took over as Grundig president in April 1984, wants to make the company less dependent on consumer electronics, which he thinks probably won't grow at more than 2% annually for the next few years. However, audio and video equipment "will continue to be our main pillar of business.".

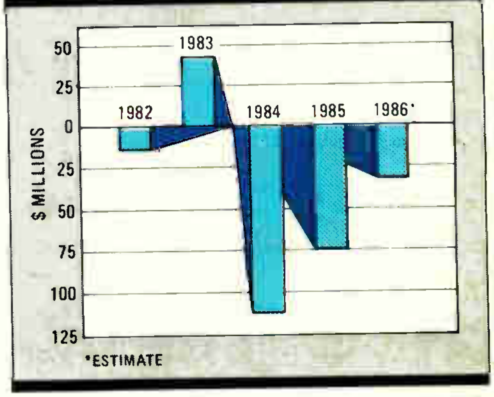
Even here, though, Koning is finding ways to lessen Grundig's exposure. For example, he has set up a production swap with Blaupunkt Werke GmbH, a consumer electronics equipment maker in the Robert Bosch group of companies. Blaupunkt will phase out production of TV sets, instead buying them from Grundig. For its part, Grundig will stop making car radios and purchase them from Blaupunkt. Industry observers view the agreement, signed late last year, as a measure to cut down overhead and to help reduce excess capacity for both companies.

The deal will also help Grundig to manufacture more efficiently. Grundig makes about 1.5 million color-TV sets a year, as well as several hundred thousand TV kits for assembly in developing countries. Add in the 600,000 sets that Grundig expects to produce for Blaupunkt, and the annual output will come to nearly 3 million sets and kits. "That will give us an economy of scale approaching that of the Japanese and allow us to stay competitive on foreign and domestic markets," Koning says.

Nonconsumer products contribute between 8% and 10% of Grundig's sales, and this business is growing by about 25% a year. Grundig will push even harder in office systems equipment, such as dictating machines, telephone answering sets, and videotex equipment. Another promising field is industrial electronics, where Grundig will add to its products, offering numerical control systems, closed-circuit TV systems, and measuring instruments for TV service and repair shops.

Grundig is also seeking outside partners for new product pushes. For example, under a 1984 agreement it recently teamed up with United Technologies Corp., Hartford, Conn., to make electrical cables and other components for the automobile industry at a Grundig plant in North Bavaria. "We are ready to enter further cooperative deals if they help maintain jobs and improve our financial standing," Koning says.

GRUNDIG: LOSSES HAVE BEEN TRIMMED . . .



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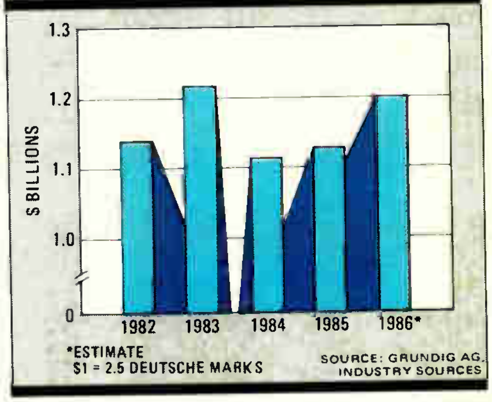

BOTTOM LINES

TANDEM BUYS 19.5% OF TELECOM FIRM

The ever-growing telephone-company demand for computers is luring Tandem Computers Inc. The Cupertino, Calif., maker of fault-tolerant computer systems has acquired a 19.5% interest in Integrated Technology Inc., a privately held telecommunications company in Plano, Texas. Tandem says the investment—for an undisclosed amount—is part of a strategic alliance between the two companies. They will jointly develop telecommunications products for Tandem's NonStop computer systems, and they will be "among the first to provide integrated services digital network capabilities." ISDN is a concept for an all-digital network based on international standards, Tandem notes.

SOFTWARE RESEARCH RAISES $4.2 MILLION

Software Research Corp., a privately held company in Natick, Mass., has raised $4.2 million in new venture financing. The company, which makes software products that allow users to exchange information between dissimilar computers, says this new funding brings to $9.7 million the amount it has raised since its start in 1978. It will use the new money to fund development work and marketing activities.

MONOLITHIC MEMORIES PLANS STOCK OFFER

Monolithic Memories Inc., Santa Clara, Calif., plans a public offering of 2 million common shares. The manufacturer of semicustom logic and memory circuits will use the proceeds for working capital.

CHIPCOM COMPLETES SECOND FINANCING

Chipcom Corp. has raised $4.25 million through a second round of venture financing. Founded in 1983, the Needham, Mass., company makes radio-frequency data-communication products for broadband local-area networks.

TOSHIBA. NOW, 1 MB DRAMS

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The executive notes that the stimulative nature of the IBM price cuts will help Burroughs's business as well as IBM's. But that hasn't started happening yet. "The first reaction is that everybody sits down and analyzes what the hell happened, and then you start to see the beneficial effect," says Ingham. "I would say there is usually about a quarter lag on that."

STRONG UPPER END. Sales in the upper end of Burroughs's equipment, Ingham notes, "are very strong. I expect a very strong billing quarter for our A-15 class of equipment," which is comparable to IBM's Sierra class. "That's going certainly at expectation, and, in fact, I think it's gone slightly above that."

Burroughs's midrange systems, such as the V series, the A-9, and the A-10, "are running just about where we thought they would be. It's pretty similar to last year and not dramatically different." For the low-end A-3 mainframes, "we're seeing some growth there compared to the same quarter last year. We're seeing quite a significant billing growth."

Honeywell Information Systems, Minneapolis, enjoyed a strong year in 1985 in its high-end mainframes despite the industry slowdown, according to vice president William N. Wray. Worldwide order rates in 1985 rose 10% from 1984, with the U.S. up 19%. "And the major portion of the increase in activity was in our large-systems business, rather than in our minicomputer or small end," he says.

But now Wray sees "a substantial improvement in activity." This doesn't mean an improvement in orders, but rather a rise in the number of prospects it sees. "The order activity has not turned up yet. But I've been waiting all through the last half of last year to see the first signs that precede an order activity improvement, and I'm feeling encouraged," he says.

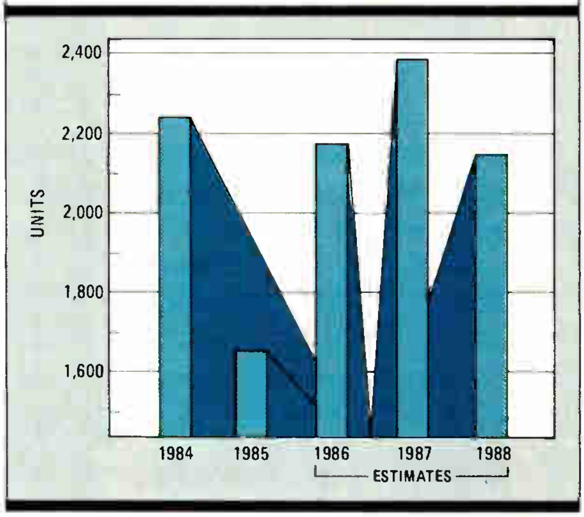
"Six months ago, we had hoped the upturn in the minicomputer business would be evident earlier," Wray notes. "So at the middle of 1985, we were expecting to see a stronger 1986 than the way we've actually now planned 1986. Right now, we're really saying 1986 in total is going to look about like 1985.

"If I compare it to the way we saw it at the middle of last year, probably the increases in revenue are going to tend to occur later in 1986 than we had contemplated or believed. And the longer it takes for order levels to really turn up, the less that will be felt in terms of shipments and revenue in 1986."

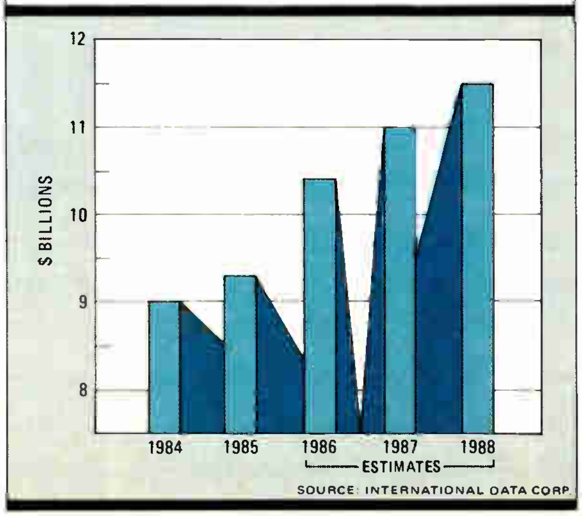
Although Honeywell is encouraged by what it sees in new prospects and activity, "until the orders actually come in at a significantly improved rate, you can't really expect there to be much of a change in shipments and revenue," Wray says. □

Additional reporting was supplied by Wesley R. Iversen in Chicago, Eve Bennett and Clifford Barney in Palo Alto, and Craig D. Rose in Boston.

U.S. SHIPMENTS OF MAINFRAMES TUMBLED IN 1985 . . .



. . . AS REVENUE INCHED AHEAD



SOURCE: INTERNATIONAL DATA CORP.

IBM PRICE-CUTTING CASTS DOUBT ON MAINFRAME UPTURN IN 1986

BUT SOME STILL SEE STRONG ORDER RATES IN THE SECOND HALF

by Robert J. Kozma

NEW YORK

While IBM Corp. would never publicly admit to it, the company's early price-cutting on its new Sierra line has got many people thinking that the computer giant is turning bearish on a turnaround this year in sales of mainframe computers. That would be particularly bad for Big Blue, which relies on mainframes for as much as 50% of its profits.

Industry watchers may see it that way, but other computer makers say they remain optimistic. They say that customer demand for mainframes is coming around according to their schedules and insist that IBM's move was a logical action dictated by manufacturing economies and lower component costs. Those very factors, they hold, will ultimately stimulate sales later this year for all suppliers.

IBM cautioned the Wall Street investment community earlier this year that it didn't see any signs of a big increase in demand, and it decided to slash prices of its high-end and medium-scale computer systems. The computer giant also boosted rental prices by 8% as a result of "normal business reviews." The mainframe price cuts range from 9% on the new top-end Sierra machine, the 3090 model 400, to 13% for its new midsize 4381 group 12, to 19% for two of its 308X models (table).

REAL CONCERN. Among those who believe the move was prompted by worry is Ulric Weil of Weil & Associates, Washington, who says, "Demand is clearly not as strong as IBM thought it would be at this time. They're cutting prices out of real concern." Mainframe sales are "critically important for IBM," and the company believes cutting prices will stimulate sales.

"When IBM lowers its prices, they have a very good idea of what they're doing," notes David Moschella, director of systems research at International Data Corp., the Framingham, Mass., market research company. "A price cut generally indicates that 3090 demand is not as good as they'd hoped."

Sales of mainframe computer products remain slow, Weil says, because the budgets of information-systems departments continue to be scrutinized by corporate managers who think they might not be getting enough return on their investments. On the other hand, he says, some orders that might have been placed in 1986 were actually placed in the fourth quarter of 1985 for tax reasons, thus skewing the 1986 figures.

David Turner, general manager of National Advanced Systems, the Mountain View, Calif., computer subsidiary of National Semiconductor Corp., argues that the mainframe-computer market needs—and will get—stimulation from IBM's action. "IBM has to put people in decision-making modes. When people start making decisions, they start buying."

One forecast is for a 3% drop in sales this year

Although "the first half is going to be tough for the industry, with some users still trying to figure out which way they want to head," it's still too early to tell what kind of year 1986 will be overall, says a spokesman for Amdahl Corp., which sells IBM-compatible systems. But the Sunnyvale, Calif., company is optimistic. "The second half shows a lot of promise," the spokesman says.

According to International Data forecasts, the mainframe market will be in for less-than-historical growth this year. The company, which has been tracking mainframe sales for 20 years, sees sales of mainframe computer systems—including peripherals and bundled software—increasing just under 12% this year to an estimated $10.4 billion, with the number of processors installed rising 32% to 2,180 (charts). That's a refreshing difference from 1985, when the number of installed units fell 26% to 1,650, increasing total industry sales a scant 3% to $9 billion. Still, if International Data's forecasts are correct, industry shipments in 1986 will be almost 3% below 1984's 2,240 units.

IBM accounts for about 60% of the large-scale computer market, by International Data's estimate, so it's easy to see why the leader wants to step up these sales. "Cutting prices was a very constructive move—not done out of panic, but to solidify their customer base," argues Fred Cohen, of L. F. Rothschild Unterberg Towbin, New York. Cohen notes that IBM's orders were soft in December, but says its mainframe backlog reaches to September of this year.

More important, Cohen believes, IBM is trying to reduce the price differential between its processors and those offered by competitors. This is especially true of IBM's decision to introduce the 3090 models 150 and 180. Cohen thinks IBM is trying to beat back any competitive thrust by Digital Equipment Corp., which is reaching upward in processing power with its top-of-the-line machines. "DEC is not a threat to IBM at the high end," Cohen says. "But where there is an overlap, the price difference is substantial. IBM is starting now to reduce that difference."

Clive W. Ingham, program general manager for systems at Burroughs Corp. in Detroit, disagrees with the notion that IBM cut prices because it is concerned about a slump in the market. "The Sierra announcements were pretty

IBM CORP. MAKES BIG CUTS IN PURCHASE PRICES OF HIGH-END SYSTEMS

Machine	Model	New price ($ thousands)	Old price ($ thousands)	Price cut (%)
3090	200	4,100	4,600	11
3090	400	7,944	8,744	9
3090	400 Upgrade	3,844	4,144	7
3081	GX1	1,805	2,190	18
3083	BX0	930	1,155	19
3084	QX3	3,885	4,820	19
4381	Group 12	330	380	13
4381	Group 13	440	500	12
4381	Group 14	735	855	14

SOURCE: IBM CORP.

a Mega-chase in space.

have been specially designed to withstand the demands of space travel.

What science hopes to learn:

Scientists will use this data to learn about the origin of Halley's and other comets. They hope to determine the location and nature of the comet's nucleus. On-board instruments will detect particles as small as one-trillionth of a gram. Many scientists believe these particles are samples of matter from the formation of the solar system.

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Halley's Comet will appear late in November, 1985, and will be fully visible in late March, 1986, particularly in the southern hemisphere. Don't miss the opportunity to see the splendor...your next chance will be in the year 2060.

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Pursuing Halley's Comet:

All five satellites on the trail of Halley's Comet rely on RCA High-Rel components.

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A worldwide effort.

Years ago, governments all over the world agreed to set up a tracking force of five satellites: the European Giotto, Japanese MS-75 and Planet A, and Soviet Vega I and Vega II. Launched into coordinated orbits, they will monitor the path of the comet precisely.

RCA helps make it possible.

All five of these satellites will use High-Rel CMOS devices made by RCA. Devices which

Darpa's Arpanet telecommunications network, without which, says Lewicki, "Mosis would not go."

Getting customers proved to be the easiest job—there's no other service like Mosis anywhere in the world. The first Mosis chip run took place in August 1980, for the National Aeronautics and Space Administration.

Mosis filled a need for a VLSI program, apparent since the mid-1970s to university and military/aerospace engineers who found themselves unable to take part in this emerging technology. Spearheading its formation was Robert Kahn, who then managed the Information Processing Technology Office at Darpa. "It was crucial to create an affordable methodology for computer science departments and nonsemiconductor people to get hands-on experience with VLSI," says Kahn. The alternative was conventional custom device prototyping through commercial houses, but the cost is prohibitive for many—in today's market, the price could reach $50,000.

Beginning in late 1977, Darpa funded researchers, mainly at top colleges, to work on key parts of what became Mosis. Involved were the California Institute of Technology, Stanford University, Hewlett-Packard Co., Xerox Corp., and others that worked on such aspects as language, interfaces, and structured chip design. The first results of this work were coordinated at Caltech, in Pasadena, where students of Mead were doing early devices. Help also came from companies that lent design and fabrication facilities.

But the service didn't click until Kahn chose USC's Information Sciences Institute to run Mosis. ISI, which oversees consultant and technology programs for the university's engineering school, had little semiconductor background at the time. Still, says Kahn, with its "extensive computer and networking experience," it seemed "a natural" choice. From Caltech came faculty member Danny Cohen as the first manager. And by 1982, says Kahn, Cohen had "turned [Mosis] into a service with user interaction."

Lewicki, who replaced Cohen as the service's director that year, came to the project from the user side, as head of the Silicon Structures Program at Caltech, which brought companies onto the campus for cooperative VLSI work. According to Kahn, Lewicki has shaped Mosis into "a real success story."

The locus of Mosis is the middleman role played by the staff, which numbers about 15. The staff members go to the foundries that do the fabrication for Mosis's customers and say, as Lewicki puts it, "Let us handle all the stupid questions for you—transfer to us all the information burden" such as scheduling, distributing completed parts, and transmitting data to the foundry. For their part, circuit and system designers get a proven step-by-step way to realize packaged devices some 10 weeks after their data arrives at the office with completed circuit geometries conforming to process specifications and design rules. Besides CMOS 3 and 1.2 μm, Mosis supports n-MOS in 3 and 4 μm, and less-used CMOS silicon-on-sapphire semiconductor processes.

Mosis processed 2,000 chip designs last year

To preserve confidentiality, Mosis staff members do not check details, or even know the general purposes, of the devices for which they're creating ICs—the designer has sole functional responsibility. The economies of Mosis derive from fabrication runs, in each technology, in which the wafer carries up to 40 designs. This arrangement enables costs to be shared so that prices for prototypes are very cheap, compared with commercial rates: from about $4,000 to $9,000 for 12 to 24 packaged parts, depending on die size. The commercial price would be $25,000 to $50,000. Foundry runs take place almost weekly, but not for all processes.

There is a great deal of opinion, pro and con, about Mosis's practice of grouping totally different chip designs with different die sizes on the same wafer. "Nobody else mixed sizes, they're not that crazy," admits Cohen. But he and Lewicki say such mixing becomes a problem only when fabricating mass memories. Cohen also observes that Mosis goes against the grain of semiconductor technology evolution itself. "We tried to throttle back high-volume mass production of similar parts to small volumes of dissimilar parts," he says.

This iconoclastic approach has not prevented Mosis from building a small coterie of enthusiastic supporters. It reports that more than 100 organizations used Mosis last year for some 2,000 chip designs. Typical of the reaction is that of Caltech's Mead, who says, "Those guys [at Mosis] have done a tremendous service to the community." Having access to Mosis has made his researchers "10 times more effective than before" in obtaining chips, Mead says.

Adds Paul Losleban, a senior research associate at Stanford who earlier served as a Mosis manager, "It has produced a crop of new ideas across the research community far beyond the original expectation."

CONSTANT BATTLE. Of course, all is not trouble-free at Mosis, as Lewicki is quick to admit, confessing to "bad runs sometimes." And, he says, there's the constant problem of vendor turnover, because foundries often "don't want to mess with small runs, even in a recession." This attitude makes it difficult to maintain three fabricators for each process technology. Still, he says, there's always the chance that a small Mosis run could ultimately result in a big order, and this is the carrot Lewicki dangles in front of his vendors.

The big question for Mosis's future revolves around its coming plunge into the commercial world and what that will do to its character as a haven for research. Proponents of the new direction point out that if commercial volumes grow as planned, Mosis can expand its staff and process technology even further. Such expansion, they believe, can only help its research-minded users. ☐

HUNTING FOR BUSINESS. George Lewicki, Mosis's project leader, says a turnkey VLSI design kit from Mentor Graphics lets Mosis look for commercial volume in its prototype runs.

HOW MOSIS WILL SLASH THE COST OF IC PROTOTYPING

NEW SOFTWARE ENABLES IT TO EXPAND BEYOND UNIVERSITY BORDERS

by Larry Waller

MARINA DEL REY, CALIF.

One of the best-kept secrets in the semiconductor business is stepping out of the shadows. Called Mosis, an acronym for MOS Implementation System, it is a service at the Information Sciences Institute of the University of Southern California that turns out prototype runs of very large-scale integrated circuits for a great deal less than it would cost at a commercial house. Its customers so far have been noncommercial, mostly university researchers and a smattering of aerospace companies.

But now Mosis officials are reaching out for a broader market and an even more ambitious service, one that moves yet a step closer to what Carver Mead, the Caltech pioneer in structured VLSI design, calls silicon publishing, where the creative and manufacturing processes are separated.

What this means, says Mead, is that the chip or system designer would take the design to a foundry, much as a writer takes a manuscript to a publisher or printer. "It separates the creative side from the manufacturing side. [Mosis has] taken all the pain out of things of this sort. We've only seen the beginnings of a whole new era" where people with new ideas won't have to start their own manufacturing companies to realize them. Expansion of Mosis would thus afford greater opportunity for innovation without incurring the burden of fabrication.

"We've purposely kept quiet before, but now we would like to see lots of commercial volume," says George Lewicki, the Mosis project leader.

Lewicki and his fellow managers think they finally have the missing link to expanding the Mosis client base: a turnkey VLSI design kit that makes using Mosis much simpler. The package, for Mosis's 3-μm CMOS process, integrates the CMOS 3 standard-cell library and design rules with a work station from Mentor Graphics Corp. that offers front-end processing and automatic layout capabilities. Mentor claims that the $400 software kit is the industry's first for standard cells and, when coupled with its work station, can in the company's words, "provide a scrupulous integration between the [VLSI] schematic and physical layout."

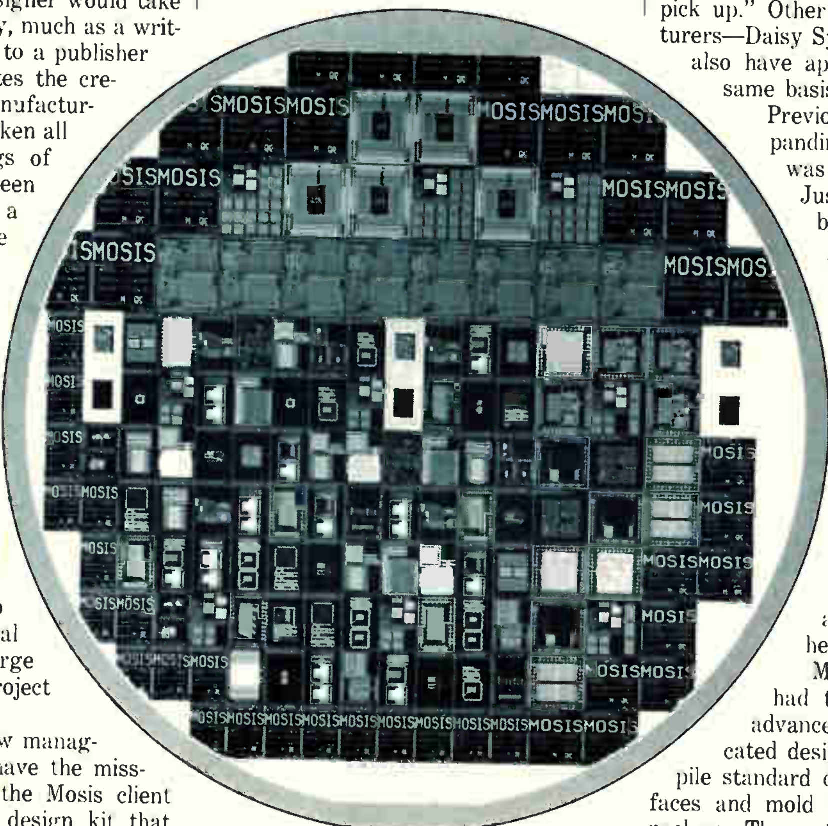
TROUBLESOME GAP. The purpose of the kit is to fill what has been a troublesome gap for Mosis: a way to ensure the compatibility of circuit design rules. In the past, Mosis's customers have managed to work their way around this problem by the seat of their pants—in Lewicki's words, "They were very bright students who found a way to do things."

The kit—developed jointly in less than a year by Mentor, Aerospace Corp., and the Boeing Military Airplane Co., a Wichita, Kan., subsidiary of Boeing Co.—allows a system designer with little VLSI expertise to configure a standard-cell chip for schematic entry, simulation, and physical layout. Correct design is ensured by logic and physical models that describe CMOS 3's technology characteristics and rules. In addition, embedded work station software supplies IC analysis and delay calculations for the CMOS technology. A designer works out chip geometries using the kit, then sends them to Mosis by electronic mail for production.

Lewicki says he began receiving inquiries about the process right after it was announced last month [*Electronics*, Feb. 10, 1986, p. 13]. He predicts that "Mentor will sell more hardware, and we expect the commercial business to pick up." Other work station manufacturers—Daisy Systems Corp., for one—also have approached Mosis on the same basis as Mentor, he notes.

Previously, says Lewicki, expanding Mosis's client base was out of the question. Just launching the trailblazing operation and getting it to run smoothly were daunting enough, even with financial backing from the Defense Advanced Research Projects Agency beginning in the late 1970s. Historically, the most formidable task has been to find chip vendors willing to do small-quantity work, and that's still a major headache.

Mosis's founders also had to build a cell library advanced enough for sophisticated designers, as well as compile standard design rules and interfaces and mold them into a workable package. The system is held together by



SMORGASBORD. Typical wafer done for Mosis by a foundry has a wide variety of circuits that can be processed in a single run.

er technologies, HP says. It rates the TTL series 930 at 4.5 mips, about the same as the ECL Digital Equipment Corp. VAX 8600.

Analyst Cuhney challenges these performance figures, however, noting that HP rates the 930 as having only twice the throughput of the Series 68, a 1.1-mips machine. He suggests that there may be a difference in "RISC mips" and mips on complex-instruction-set machines.

The aging 3000 family, limping along on a 16-bit data path (Spectrum is a 32-bit architecture), was chosen as the vehicle for Spectrum's introduction because it is in dire need of an upgrade. Later this year, HP will introduce a machine in its 9000 family with about twice the performance of the present top-of-the-line series 500, and a 1000-line real-time system for computer-integrated manufacturing (CIM). An artificial-intelligence computer, supporting Lisp, will be announced at midyear.

HP will not disclose a date for introduction of the first member of the 1000 family. However, Dataquest believes that the company could have a surprise up its sleeve here. A 1000 machine could hit the market as soon as the 930, or late in 1986, Peterson says.

In any case, Young says, for three or four years beginning in 1987, HP will be releasing Spectrum products every quarter or so. Those products may cover areas of the market where HP does not now compete. "There are no technical limits to the capability of the architecture," says Young. However, he adds, for now HP has no plans to enter the mainframe or supercomputer markets.

"We may be able to build faster machines than we want to build," he says. "We're not constrained by the technology but by the markets of interest to us. Spectrum will allow us to compete in areas where we haven't really had entries before." One is the high end of computer-assisted engineering, Young says, where HP has had a platform but no servers or big number crunchers. Another is CIM, where the company lacks network management for larger machines.

Once Spectrum begins to pervade the HP product line, it will influence the way HP operates. Instead of separate product divisions, each with its own manufacturing operation, HP will have a single information technology group for development and manufacturing, and separate divisions that map Spectrum's capabilities into their own markets.

MARKET SUPPORT. The Information Technology Group will supply components and boards, Young explains; at the systems level, the divisions will package the boards into their own products. In addition, Young hopes, the single technology will ease housekeeping pressures on HP engineering, freeing it for market support.

During the past year, in preparation for Spectrum, HP merged its integrated-circuit and printed-circuit-board fabrication activities and formed market-oriented divisions in office automation and technical work stations. Meanwhile, with Spectrum's full impact still a year or more away, HP is proceeding cautiously.

Hurt by the drop in orders last year, it cut back on capital expenditures and reduced work periods by a day every two weeks. Now, Young says "the trough is behind us." But he questions the robustness of the recovery. Some of the employees are back on full time, but HP has restricted hiring to the point where every new employee must be approved by HP's top-level executive committee.

First-quarter results from 1986, released only last week, showed profits off 6% from a year ago, but orders slightly up. Whatever happens to shipments this year, HP is depending on Spectrum to get the orders flowing even faster for next. □

***DESPITE THE SLUMP, HP PRESENTS A SOLID PICTURE** (\$ millions except per share figures)*

	1981	1982	1983	1984	1985
Domestic orders	1,918	2,283	2,901	3,629	3,662
International orders	1,739	1,897	2,021	2,721	2,733
Total orders	3,657	4,180	4,922	6,350	6,395
Net revenue	3,528	4,189	4,710	6,044	6,505
Pretax earnings	567	676	728	860	758
Net earnings	305	383	432	665*	489
Per share					
Net earnings	\$1.24	\$1.53	\$1.69	\$2.59*	\$1.91
Cash dividend	11¢	12¢	16¢	19¢	22¢
At year end					
Assets	2,782	3,470	4,161	5,153	5,680
Employees (thousands)	64	68	72	82	84

*Includes one-time increase in net earnings of \$118 million (46¢ per share) resulting from tax law change.

SOURCE: HEWLETT-PACKARD CO.

FIRST RISC MACHINE WILL APPEAR LATE THIS YEAR

Of the three new members of the 3000 family announced last week by Hewlett-Packard Co., only the conventional series 70—with its complex instruction set that can use several machine cycles for a function—is available now. The TTL-based series 930 will appear late in 1986 and the n-MOS 950 in the second half of 1987.

The 930, HP says, is built around a 4.5-million-instruction/s TTL processor with reduced-instruction-set computer architecture. It supports up to 24 megabytes of main memory and has about twice the throughput of a series 68, now the top of the 3000 line. A base system for the 930, including 16 megabytes of memory, two input/output channels, a local-network channel, and fundamental operating software, sells for \$225,000. With a 404-megabyte disk drive, tape backup, and a system console, the cost is \$284,500. A discrete TTL floating-point coprocessor option costs \$10,000.

Douglas C. Spreng, general manager of HP's Computer Systems Division, Cupertino, Calif., claims performance for the 930 equal to that of a Digital Equipment Corp. VAX 8600, at half the VAX's \$450,000 price tag. The 930 also outperforms the 2.7-mips IBM 4381 model 2, which costs more than \$600,000, he says.

The series 950 will have a 6.7-mips n-MOS processor, support up to 64 megabytes of main memory, and deliver three times the throughput of the series 68. The 950 will cost \$300,000 to \$350,000.

HP claims a better than 20% performance increase for the series 70 over the series 68, at a 20% drop in price, ranging from \$150,000 to \$210,750. Upgrading the 68 with a series 70 processor and improved operating system software costs \$30,000.

The series 930 and 950 are both object- and source-code compatible with earlier 3000s. Current applications will run without modification, recompilation, or data conversion on the new machines. The user need only perform a store/restore operation on the programs, which will then be able to access data on both the new computers and other 3000s. But to take full advantage of the Spectrum performance, source code must be recompiled into a native-mode environment. So HP has developed optimizing compilers for Cobol, Fortran/77, and Pascal. *–C. B.*

accident. The photos released show three indistinguishable boxes that look like nothing so much as large air-conditioners. The unmistakable message to the customer—relax. For you, nothing has changed.

Customer acceptance, not the technology, is the biggest risk with the Spectrum line. The big question for HP is whether it can radically revise its product line while presenting an unchanged interface to its customers, a feat much like taking off your vest without removing your coat.

Young, however, says he is weary of headlines that make puns on RISC and *risk* and news stories that imply that because Spectrum is RISC-based, HP is betting its future on a new and untried architecture. To Young, the important aspect of the new technology is not its architecture but its ability to operate over the whole spectrum of HP computers and beyond. That will unify HP's three computer lines and end the burden of having to make all engineering changes three times.

BETTER SOLUTION. Compatibility with existing software was one of the four design goals set for Spectrum, along with scalability, unity, and longevity (see "A simple design may pay off big for Hewlett-Packard," p. 39). Without it, HP would have been able to change only by abandoning its clientele. Dataquest's Peterson thinks HP succeeded in this task. "I expect their customers will like it very much, because they won't have to do [code] conversions, in most cases. It's a far better solution than any other firm has been able to provide."

The company had no choice but to change. Not only were its machines outdated, but its three computer lines had different architectures and different operating systems. That was all right when businesses ran accounting programs and laboratories analyzed measurements and work stations were special-purpose curiosities. But the popularity of networking and the new demands of distributed data processing meant that HP would eventually face a nightmare in trying to get its machines to communicate with one another.

Spectrum was a deliberate attempt to awaken from this nightmare. What was needed, Young decided, was a world-class computer-science operation. In 1980, he took the step—unusual for HP—of going outside the company to hire Joel S. Birnbaum away from IBM Corp., where he had been director of computer science at the Thomas J. Watson Laboratories, Yorktown Heights, N. Y.

HP GETS CAUGHT IN THE SLUMP ($ millions)

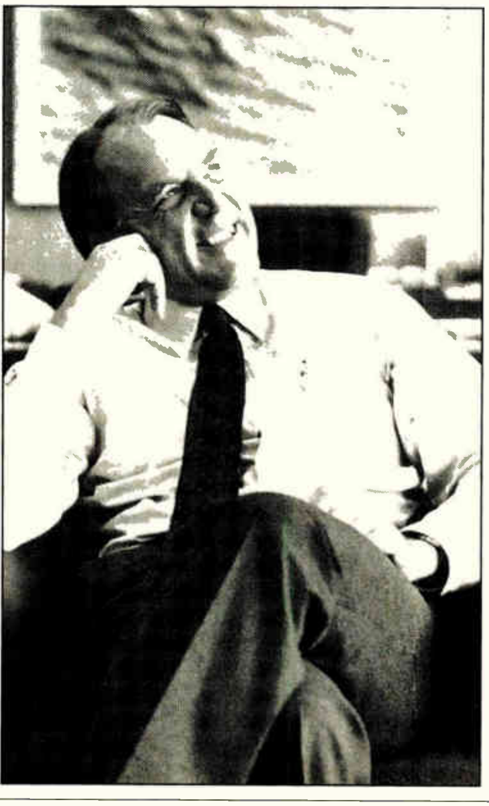
Product or service	1984 orders	1984 shipments	1985 orders	1985 shipments
Measurement, design, information, and manufacturing equipment and systems	3,135	2,879	2,819	2,929
Peripherals and network products	1,440	1,375	1,537	1,560
Service for equipment, systems, and peripherals	904	970	1,135	1,125
Medical electronic equipment and service	402	377	458	448
Analytical instrumentation and service	238	229	256	248
Electronic components	231	214	190	195
Totals	6,350	6,044	6,395	6,505

Note: In 1984 the backlog, the amount by which orders exceeded shipments, was $306 million. In 1985, shipments exceeded orders by $110 million.

SOURCE: HEWLETT-PACKARD CO.

Birnbaum, who had worked on the 801 project at IBM, the first RISC design, jumped at the chance to engineer a computer system from the ground up. He began forming an organization, luring experts in the new science of computer measurement from Amdahl, Burroughs, and IBM itself, and subverting the HP style of autonomy within divisions by pulling personnel from different divisions together in an Information Technology Group with its own building in Cupertino, Calif.

HP bought an Amdahl Corp. mainframe—and the group began measuring and analyzing what actually happens when computer programs are executed, what happens in a central processing unit's memory when a benchmark is run, where the bottlenecks are, and how well the cache performs. Then they tested architectures on customer programs, seeing how much work they could do.



JOHN A. YOUNG: HP president believes broad applications are the key.

The RISC architecture that resulted reflects the goals of unity, scalability, and compatibility, Birnbaum says. "For instance, if we didn't have the requirement of designing for a technical computer, we'd have a different I/O," he notes. He likens RISC to a car engine—the engine may run fast but how fast the car goes depends on other factors such as weight, gearing, roads, weather, and so on. Spectrum allows for such variations with ways to tune performance: coprocessors, special instructions, and a new kind of software assist.

TRAPS FEARED. Birnbaum acknowledges that RISC architecture may have some boobytraps, in that the simple instruction set could conceivably lead to a longer data path. All the analyses performed by the Information Technology Group were directed against that possibility, but "whether we did a good job depends on whether those measurements accurately reflect how customers will use these machines," he says.

He believes the real message of Spectrum is not whether HP did an elegant job of designing a new architecture but that the design was an engineering task. "This is an engineering discipline. This is the best-measured architecture ever done. We didn't change a transistor until we had 50,000 address traces. There is no theology of RISC or non-RISC—it's all engineering design."

And the payoff, Birnbaum contends, is that "we have finally got the company singing to the same sheet of music: one architecture, one family, good for the next 10 years."

The architecture scales to "dozens of mips [million instructions per second] in ECL or the next generation of submicron CMOS," he says. But even the early versions of Spectrum in conventional TTL and n-MOS outperform older architectures implemented in nominally fast-

PROBING THE NEWS

HP TAKES CAREFUL APPROACH WITH NEW SPECTRUM COMPUTERS

TIGHT ENGINEERING ENSURES A GOOD FIT WITH EXISTING MODELS

by Clifford Barney

PALO ALTO

To Hewlett-Packard Co. president John A. Young, the worst thing about the reduced-instruction-set computer is that its acronym sounds like *risk*. Staid, buttoned-down HP has never been known for running major risks in the way it does business. Instead, the company has made its reputation by building test and measurement equipment that takes the risk out of decision making and turns it into a process based on carefully engineered choices.

So when HP finally took the wraps off its new Spectrum line of RISC computers last week, introducing two machines at the high end of its 3000 business computer family, it went to great lengths to emphasize the continuity with its current computers and the utter lack of anything resembling risk in the switch to a new architecture.

Late with 32-bit architecture, HP plays catch-up

HP does not want to rock any boats with Spectrum. Too much depends on it. HP is bringing the technology to market at a time when the company has been in the doldrums for over a year. Caught in what Young believes is a general electronic slump—not just a slowdown in computers, from which HP derives about 45% of its revenue—it grew barely over 8% last year, from $6.0 billion to $6.5 billion, a particularly galling performance after the nearly 30% growth recorded in 1984 (table, p. 46).

SLOW YEAR AHEAD. Young predicts only modest growth in 1986, and Spectrum will contribute almost nothing (see "First RISC machine will appear late this year," p. 47). Only one of the machines will be available this year, and it will be 1987 before the new technology makes an impact on the balance sheet.

Nevertheless, the arrival of Spectrum means that HP is ready to play a much stronger role in the minicomputer and technical computer markets. It has lagged behind in all three main product areas: its 3000 family and its 1000 scientific computer line are late with 32-bit architectures, and its 9000 work stations have failed in the engineering market.

Spectrum was generally welcomed by industry analysts, though some question its timing. "This is a big event for HP," says Adam Cuhney of Kidder Peabody Inc., San Francisco. "They haven't had anything to talk about for some time." Spectrum, Cuhney says, can help generate orders for HP, despite the sluggish pace of capital spending.

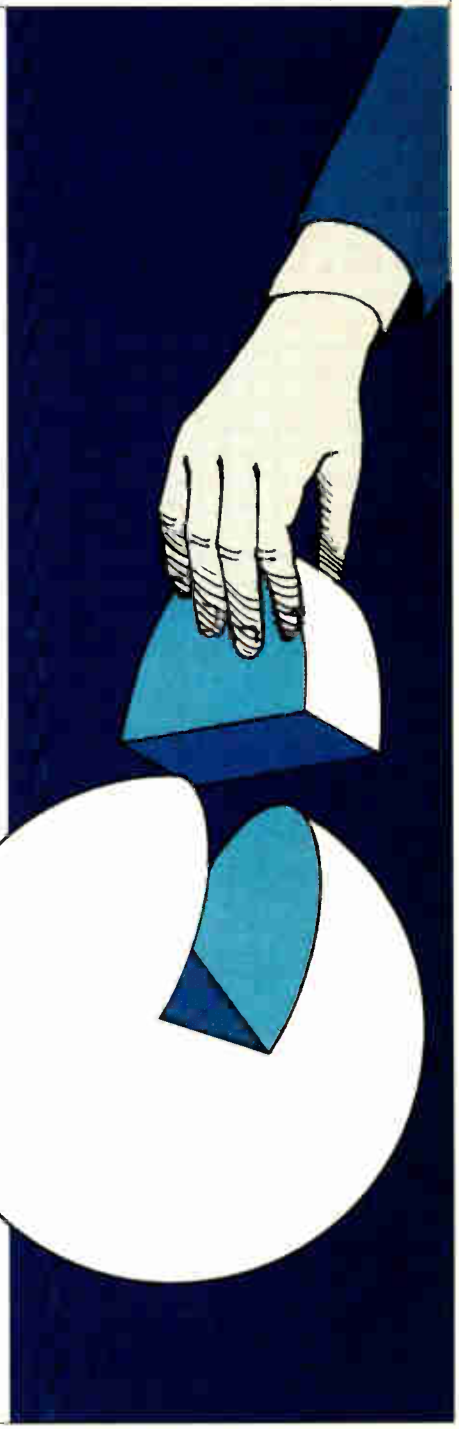
Cuhney and other observers were impressed with Spectrum's versatility. Its architecture is applicable across product lines and technologies, so the company can make upgrades without disturbing the installed base.

Spectrum's architecture will put HP in the enviable position of being able to add new products very quickly, according to Gwen Peterson, who tracks minicomputers for Dataquest Inc., the San Jose, Calif., market researcher. "That's a major benefit whose magnitude may not be appreciated for a couple of years or more."

In introducing Spectrum, HP has attempted the technical feat of making a big splash without making waves. It pulled out all the stops on press coverage, putting on two major press conferences, linking others by satellite, flying in a planeload of European reporters, and sending HP executives on the road to explain the significance of Spectrum.

Yet to balance all this fanfare, the first formal announcement of the Spectrum machines was a masterpiece of understatement. "Three new high-performance members of the HP 3000 family of business computers, including the first two products from the Spectrum program, were announced today," it reads.

First mentioning it in so offhand a manner, and giving it equal billing with the third family member, the conventional series 70, could not have been an



delete instruction sequences, and because these optimizations are useful for production, the two more-extensive optimization levels can be invoked after the programmer has demonstrated the correctness of the program.

Level 1 optimization adds a few more optimizations, but requires no data-flow information, and so is still a simple process. This level adds optimization of peepholes and branches and full instruction scheduling. Peepholes are tiny "windows" that are the means by which the optimizer looks at short instruction sequences. These are matched to templates of common instruction sequences. When a match is found, the short instruction sequence is replaced by a single instruction or a shorter sequence. The branch optimizer's task is to eliminate unnecessary branches and some unreachable code. It can replace some chains of branches with a single branch. It can also notice when the targets of conditional branches are unconditional branches and replace the two branches with one conditional branch.

In instruction scheduling, Level 1 optimization includes the limited replacement or removal of NOP instructions following branches—the only instruction scheduling done by Level 0. But Level 1 does more instruction scheduling to minimize memory interlocks.

To do this, the optimizer needs to know the data dependencies between instructions, so it first constructs a dependency graph. Targeted instructions are separated by data-independent instructions discovered in the graph for more throughput. Other instruction-scheduling transformations performed include separating the load from the instruction that uses the loaded register, separating store and load sequences, and separating floating-point instructions from each other.

For full optimization, Level 2 is called upon. This level, however, requires that data-flow information be calculated. Level 2 optimization includes all of Level 1 plus most of the optimization techniques of modern optimizing compilers, such as local constant propagation, local peephole transformations, local redundant-definition elimination, common-subexpression elimination, redundant load/store elimination, loop invariant code motion, induction variable elaboration and strength reduction, and another register allocator.

The register allocator used in Level 2 is based partially on the graph-coloring technology developed for register-based machines. Fully optimized code contains many more live registers than partially optimized or unoptimized code. Therefore, the Level 2 allocator is designed to handle many live registers better than the allocator used in levels 0 and 1. The Level 2 allocator has access to the data-flow information that has been calculated for the symbolic registers in the programs and, in addition, information regarding the frequency of execution of each program block.

All of the optimizations introduced in Level 2 require this data-flow information plus some control-flow information. Data-flow analysis provides information to the optimizer about the pattern of definition and use of each machine resource. For each basic block in the program, the data-flow information indicates what definitions may reach that block and what later uses may be affected by local definitions.

BASIC BLOCK ANALYSIS

Control-flow information in the optimizer is contained in the basic block and interval structures. Basic block analysis identifies blocks of code that have no internal branching. Interval analysis identifies patterns of control flow such as if-then-elses and loops. Identifying intervals simplifies data-flow calculations, identifies loops for the loop-based optimizations, and enables the partial updating of data-flow information.

The optimizer first identifies basic blocks. It then calculates local data-flow information for each basic block. Next the optimizer exposes the structure of the program through the interval analysis. Then it uses the interval structure as a basis for doing the global data-flow analysis. When the analysis is complete, the optimizer knows what resources are used and defined by the blocks.

The optimizer's resource manager is responsible for maintaining the information regarding the numbers and types of resources within each procedure. The resource manager's role is especially important in the HP Precision Architecture's compiler system. It provides a way for the front ends, which deal with memory resources in terms of programmer variable names, and the optimizer, which deals with memory resources in terms of actual memory locations, to communicate the relationship between the two.

Efficient procedure calls were also critical in this architecture, because programmers are now taught to write small, well-structured procedures rather than large monolithic routines. Efficient procedure calling is achieved without a complex procedure-call instruction, but rather through a software convention using the simple instruction set.

Though it is complex itself, the compiler system is the capstone to HP's goals with the Precision Architecture. By automating the compilation process, it adds significantly to the overall simplicity of the system. HP sees such simplicity as a spearhead to its survival in the computer business. □

MANY IDEAS LEAD TO A SIMPLE SCHEME

Hewlett-Packard's Spectrum project was the largest project ever undertaken by the 47-year-old electronics pioneer. At its peak, the five-year effort involved more than 1,000 engineers. Besides their many different backgrounds in computer science, software, and engineering, many of the team members brought prior experience from companies such as Apple Computer, Burroughs, Digital Equipment, and IBM.

The job of directing this diverse team went to Joel S. Birnbaum, vice president and director of Hewlett-Packard Laboratories, the company's central research and development organization. Before coming to HP in November 1980, he spent 15 years at IBM Corp.'s Thomas J. Watson Research Laboratory in Yorktown Heights, N. Y. He was one of the lead researchers on the 801 reduced-instruction-set computer. Birnbaum left as its director of computer sciences.

With a bachelor's degree in engineering physics from Cornell University and master's and doctoral degrees in nuclear physics from Yale University, Birnbaum brought a mathematical and scientific discipline to the Spectrum project, instilling a scientist's approach to computer design.


GUIDING LIGHT. Joel Birnbaum directed HP's Spectrum project.

For the first five weeks of the project, every team member was asked to present all the computer architectures and ideas he or she was familiar with. Then the engineers studied computational behavior using the many measurements they had done and zeroed in on the reduced-complexity idea—effi-cient execution of frequently used instructions. Consequently, they took a close look at the various emerging RISC designs. For the starting point of the new HP architecture, they sorted through the RISC concepts and instructions, kept those that contributed to the project's goals, discovered what could be discarded, and added what was missing. □

wide interrupts. As with everything else, these are under high-level-language program control.

Because every system function is available to high-level-language programs, the software is a key engineering discipline in the HP Precision Architecture design. In fact, many details in the architecture are determined from the point of view of the software it must run. The richness of functions that can be controlled by high-level software is a challenge to a compiler system. But in this case, the instruction set makes the challenge easier. The short, precise, primitive instruction set, with its regularity and symmetry, is a better match to high-level languages than a complex instruction set.

STRUCTURE OF THE COMPILER

Modern compilers of high-level languages have become much more capable of analyzing and optimizing programs. In addition, compiler technology has advanced to the point of compiler systems in which language-specific front ends produce a common intermediate code that is then further processed by optimizers, linkers, loaders, and debuggers. These are shared by all languages. The compiler system for HP's new-generation architecture has such a structure (Fig. 5). Pascal, Fortran 77, and Cobol share one code generator; C has its own. Both code generators produce code in a common data structure called Spectrum Low-Level Intermediate Code (SLLIC). Much analysis information, such as information about branches and their targets, is contained in the SLLIC data structure for use by the optimizer stage.

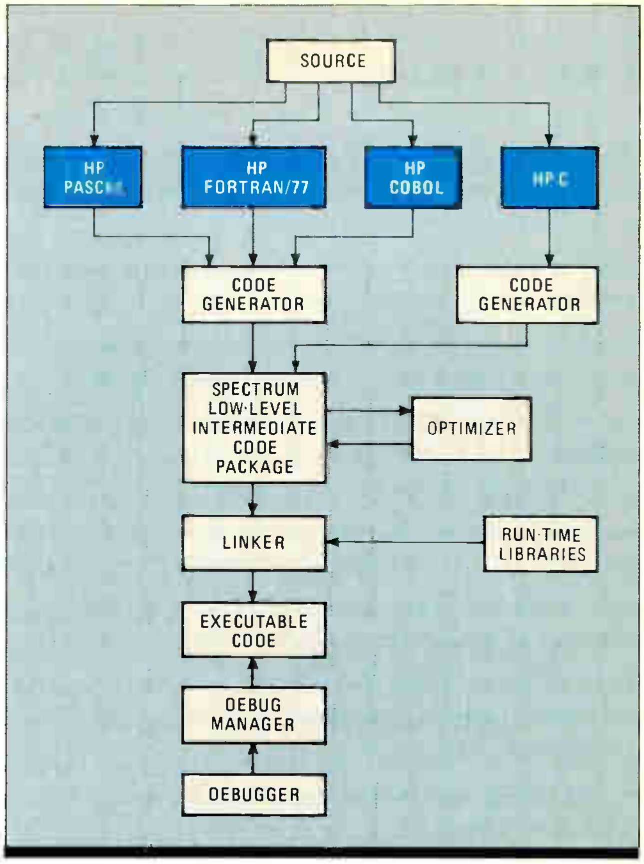
The front ends perform the lexical, syntactic, and semantic analyses prescribed by each language standard. They are also responsible for producing the data to be used later in the compiling process. Front ends generate intermediate-level codes representing the source statements for use by the code generators, plus other data concerning source statements and types, scope and locations of procedures, and function and variable names for use by the symbolic debugger.

Code generators produce the machine code—in the precision instruction set—plus the specifications for the run-time environment, including the program data space, the literal pool, and data initialization. The reduced instruction set makes the code generators work a bit harder when producing code for complex high-level-language commands such as byte moves, decimal arithmetic, and procedure calls. The precision instruction set contains no complex instructions for the code generators to use here. So the code generators must be smart enough to use combinations of the simple instructions to achieve the results.

They do not have to be too smart, however, because these code sequences can be streamlined later by the optimizer. In fact, the optimizer is the best place to do this because there is only one optimizer for the entire compiler system. The single-compiler system serves multiple operating systems and produces object-code files that are compatible across operating systems. The compiler-system design was driven by optimizing considerations and these, in fact, place restrictions on the code generators.

One class of such restrictions involves branch instructions. The optimizer requires that all branches created by the generators have an NOP (no operation) instruction immediately following the branch instruction. This allows the optimizer to reschedule instructions to minimize interlocks caused by the sequence of data and register accesses. The optimizer replaces the NOPs with useful instructions or eliminates them. For example, the optimizer could set up the execution of the first instruction following the branch while the branch is being set up, as long as that instruction does not depend on any values generated during the branch.

Another class of restrictions concerns the use of registers, because register assignment is in the purview of the optimizer. The code generators are limited to assigning symbolic



5. OPTIMIZING COMPILER. The optimizing compiler for high-level-language support has separate front ends for specific languages.

registers from an infinite register set. They are not allowed to use actual machine registers. The optimizer is responsible for making the most efficient assignment of the machine registers as part of its overall task.

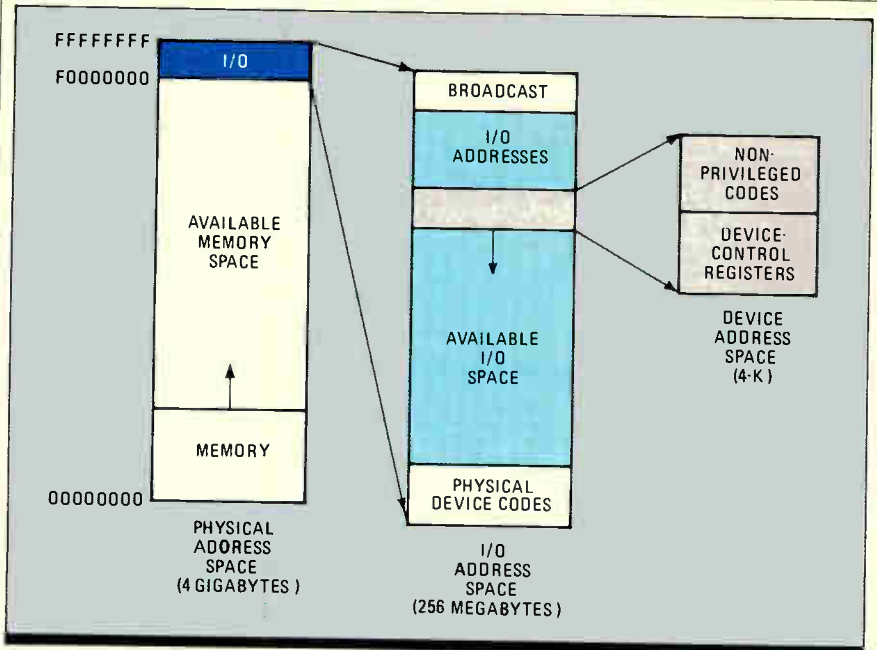
The system handles a number of tasks at compilation time. Because complex operations are broken into simple operations in the HP Precision Architecture, there is a chance that some of these suboperations are unchangeable during execution (done once at the beginning of the program) and therefore can be done at compilation time.

Among suboperations that cannot be handled this way, some can be pulled out from inside loops by the compiler to be executed once before the loop is entered. Even when that cannot be done, the optimizing compiler is intelligent enough to reuse without recalculation certain immediate values in the loop. These optimization techniques are effective because such events happen often in programs.

"There is a general rule in computers that for each instruction there is a memory reference," says Michael Mahon, manager of HP's Systems Architecture Laboratory. Some register-based computer designs have improved on this and have achieved as few as half a memory reference per instruction. "We have gotten it down to one third to one fifth, which shows just how effective the register set is and how efficiently the compilers and optimizer use them," says Mahon.

The optimizer, which works at the machine-instruction level, performs intraprocedural local and global optimizations. The programmer can turn it on or off on a procedure-by-procedure basis through compiler options and directives. Three levels of optimization are available, which the programmer can also select at the procedural level.

Level 0 optimization is intended to be used during program development. Because it is difficult to support symbolic debugging in conjunction with optimizations, which reorder or



4. I/O STRUCTURE. A map in the main memory handles all input/output functions. The same management and protection mechanisms for memory apply to I/O functions.

alternative path through its execution unit. Examples of special-function units include fixed-point binary multiplication and division units, emulation assists, and encryption and decryption hardware. The HP 3000 Model 950's CPU uses a mathematics special-function unit (Fig. 2).

At the next level—the cache—the assist processors are called coprocessors. They generally have their own registers. Examples of coprocessors include graphics and floating-point engines.

The next level of assist processors attaches at the level of main memory. At this level, the HP Precision Architecture supports multiprocessing either as homogeneous, tightly coupled CPUs or as attached special-purpose processors such as array processors or I/O controllers. Attached processors at the memory level typically have their own registers and local storage.

CACHING IT

The general registers are only the tip of the storage hierarchy. The next level is cache. In the HP architecture, cache memory has been split into two parts. Because it is designed as an integral part of the architecture, the cache is visible to the software, just as the register set is visible, which yields more efficient operation. Cache memory is divided into an instruction cache and a data cache (Fig. 3). Because the system can perform a data reference and an instruction fetch simultaneously, the cache bandwidth is doubled.

One example of how the visible cache is used is the way a piece of software can manage the cache when modifying code on the fly. Hidden caches can cause side effects for self-modifying code. But with the visible cache, a program can call a small protocol to flush and reload the cache when necessary. Such protocol code contributes less overhead and costs much less than the watchdog logic used in other architectures.

Another big gain from a visible cache is in I/O operations. In other computers that have cache, when an I/O operation updates data in memory, the I/O subsystem performs a shadow operation to flush the cache. In the HP architecture, when the operating system executes an I/O buffer operation, it invalidates the cache contents. In this way, the user program is actually managing the cache; the I/O subsystem does not interfere. The processor owns the cache without interference, so the cache logic is simplified and cache control is faster. Otherwise, arbitration would be required between the processor and something outside it—such as an intelligent I/O subsystem.

The cache design in this architecture also was done with tightly coupled multiprocessing in mind. Each processor has cache. All the caches watch what is going on with the bus to see if any data changes will affect any of the data they are holding. Through this scheme, the cache hardware guarantees that all the caches are kept up to date.

The level of storage hierarchy below the cache is main memory, which is handled as a large virtual memory space. The 32-bit architecture contains a 64-bit virtual address. The architecture provides for up to 2^{32}, or some 4 billion, distinct virtual address spaces, each ranging in length up to 2^{32} bytes, or 4 gigabytes. Certain implementations may limit the number of virtual address spaces to zero (for real addressing) or 2^{16} (64-K address spaces, as in the HP 3000 Model 930). The physical address space is also 4 gigabytes, of which the top 256 megabytes, or 1/16 of the total space, are allocated for I/O address space.

Because the I/O architecture is based on a memory-mapped addressing structure using the upper 1/16 of the physical memory, the goal of doing all programming in high-level languages can be met for I/O programming. Both privileged and nonprivileged high-level language codes have complete control of all I/O devices. Nonprivileged code normally has no control of devices.

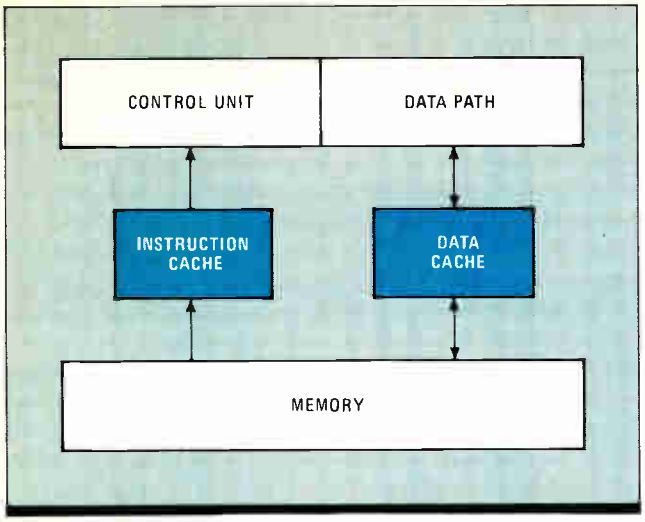
GETTING IN AND OUT

All communication between programs and I/O devices is done through the memory-mapped I/O structure (Fig. 4) that is addressed in exactly the same way as other memory references—through normal Load and Store instructions. This addressing uniformity simplifies I/O handling. Device drivers are not treated as specialized cases. The I/O space—addressed in 2-K pages, the unit of virtual memory mapping in the system—contains the same memory protection features as the rest of the memory.

This granularity, or low level, of protection and the provision for nonprivileged address space mean that protection can be extended to individual devices. For example, a program can control a device and be totally protected from other programs and devices on the machine. This is handy for real-time and instrument-control applications. The I/O space can address up to 65,536 devices because each device is represented as two 2-K pages.

I/O access bypasses the cache and goes directly to memory for minimum interference with the storage hierarchy. This allows the processor to run at a reasonable speed, even when the full I/O bandwidth is in use. All forms of I/O show up in the I/O space. Everything on a given bus shows up in the memory-mapped I/O space, including the memory controller, the processors, and bus converters to other buses on the system that connect to channel adapters and I/O controllers. All traffic is therefore controlled in the same simple way.

As one example, the interrupt-register vector is visible in the I/O space. This means that 32 levels of processor interrupts are not special—they are in the I/O space and are available to any software in the system, just as the I/O subsystems are. The I/O space also supports a broadcast area for such functions as global resets and some types of system-



3. SPLIT CACHE. Cache memory has one part for instructions and another for data, doubling the cache bandwidth.

sis in the late 1970s was that about 20% of the instructions in a complex-instruction-set computer—the simplest ones such as Add, Branch, and simple Load and Store instructions—were the ones being executed about 80% of the time. This finding was one of the basic facts that led to the RISC concept. HP's Precision Architecture, with its simple instructions and generous general-register set, is one of the designs to grow out of this work.

The final instruction set—about 70 basic instructions, which expand to about 140 when conditional permutations are included—was chosen on the basis of instruction-execution frequencies determined by the extensive measurements across a variety of workloads and through a thorough examination, analysis, and discussion of the cost and utility tradeoffs. By comparison, complex-instruction-set computers have many more. For example the current HP 3000 architecture has 231, the IBM Corp. 370/XA architecture has 207, and the Digital Equipment Corp. VAX system has 304 instructions with nine addressing modes.

FAST REGISTERS

Registers play a key role in the basic architecture. The 32 general registers in the data path (Fig. 1) are at the top of the memory hierarchy. This register set, the fastest storage in the hierarchy, is an integral part of the data path and is visible, meaning that it is directly available to the software. Software can control two reads from the registers and one write to the registers in each machine cycle. Only the Load and Store instructions access the other levels of the memory hierarchy.

Computations done by all other instructions take place in the data path. Data manipulation takes place among the registers or between a register and an immediate field that is contained within an instruction. In an immediate field, actual data, rather than the address of a piece of data, is stored in an instruction.

The wide data bandwidth created by the bigger, faster register set at the tip of the storage hierarchy is used as often as possible. Because everything done within the data path is accomplished in one cycle, the compilers are designed to use the data path as much as possible. For example, through astute register allocation, the optimizer can assign the most frequently used variables to the registers to reduce the number of memory references to far below that incurred by architectures that do not have such a large register set.

Some complex functions cannot be done entirely within the registers using the primitive instructions. Many applications, especially commercial ones, expect to find complex, high-level instructions that often are implemented in microcode in most of today's machines. But because the HP Precision Architecture was designed with neither complex instructions nor microcode, something had to be done to serve these applications. The design team therefore invented a substitute for microcode, called millicode, and added assist processors to provide the functionality of complex instructions.

Millicode provides highly optimized in-line subroutines of 10 or so primitive machine instructions that can be called up efficiently. The millicode subroutines are for special, frequently used routines, and they outperform average compilers on the same functions. Though this seems similar to microcode, it differs in several significant ways.

MILLICODE'S ADVANTAGES

First, millicode does not place any of the hidden performance penalties on all instructions that microcode often does. Because millicode is a collection of subroutines, the expense of executing a millicode instruction is incurred only when it is called. Second, the addition of millicode instructions exacts no hardware cost and has no direct influence on system cost. Also, it is relatively easy and inexpensive to extend, improve, and tune millicode in the field.

Millicode has yet other advantages. It is written, debugged, and optimized with the same compiler system used for other programs. There is no limit to the size and number of millicode instructions. And common millicode routines can be used across all members of the HP product families and operating systems.

To provide peak performance for certain heavily used performance-critical functions such as floating-point arithmetic or graphics, HP designers have gone beyond millicode and have provided for the addition of high-performance hardware in the form of assist processors, which can be added at several levels of the Precision Architecture.

Three categories of assist processors can be added. They are differentiated by the level at which they interface to the memory hierarchy. Processors coming in at the general-register level are called special-function units and are treated as alternative processing units to the main processor or as an

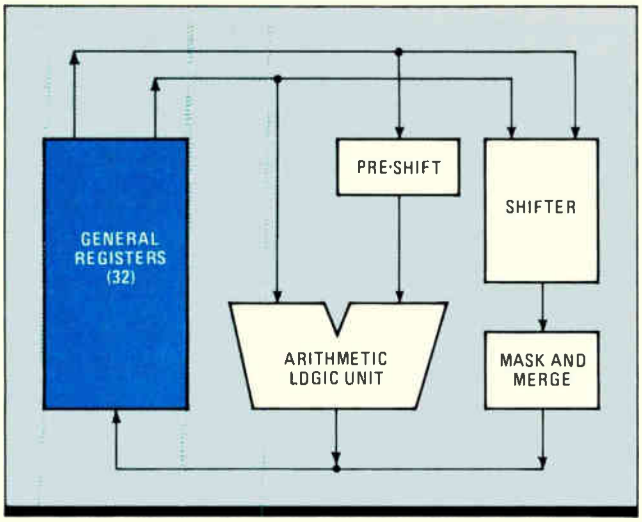
MULTIPLY DIDN'T MAKE THE CUT

When the Spectrum team took a look at a diagram of the hardware for a processor, it decided to circle in red all the portions that were needed for the Multiply instruction. The diagram became a red blur. HP designers decided that Multiply was too costly an instruction, and wondered if it could be eliminated.

The measurements showed that most multiplications are done by small integer constants. The designers realized that these multiplications could be done using the preshifter in the data path. This started the engineers thinking up ways to do other multiplications with the primitive instructions. Three Shift-and-Add instructions were already in the instruction set to do indexed loads. They shift data by 1, 2, or 3 bits and add. Engineers kept coming up with ideas to use these instructions to multiply ever larger constants—up to 512—in no more than five cycles, with most taking two or three cycles.

Design engineer Steve Muchnick then developed a program to generate the best sequence of instructions to multiply by any given constant. One of the compiler specialists, Dan Magenheimer, extended the work on multiplying by a constant into a very fast subroutine for multiplying by variables.

In the Precision Architecture, multiplications by both variables and constants are done in an average of three or four cycles—faster than the 20 or so cycles many multiplications consume in other machines. Thus, there turned out to be no need for a separate Multiply instruction. □



1. COMMON CORE. The data path in which the simple instructions are executed is the core of the HP Precision Architecture.

system at HP will evolve from one base technology, one architecture, and two operating systems—HP 3000 MPE and HP-UX, HP's version of AT&T Co.'s Unix. "No other major computer vendor has announced plans to offer such a broad range of products, all based on a single architecture, and fully independent of the technologies in which they're implemented," says HP president John Young.

HP engineers may have achieved a painless major-system changeover for the first time in computer history—for not just one but for three systems at once. Earlier changeovers by HP and other computer vendors were done by throwing out the old architecture and inventing the new, without retaining any compatibility. Now, all HP 3000 and 9000 series systems will be compatible with previous systems in those lines.

The new machines to replace the HP 1000 series, however, will not have quite the same level of compatibility with the current 1000 series because HP will be switching from RTE, the HP 1000's real-time operating system, to HP-UX with real-time extensions. A migration path, however, will be provided through analysis and transport utilities and RTE emulation.

The job of making new computers upwardly compatible with existing HP systems will be relatively easy because the short, precise instructions of this simple architecture provide a good environment for emulation. For example, the first products using the Precision Architecture, the HP 3000 models 930 and 950, which have just been introduced, are made fully compatible with HP 3000 MPE software. Programs have only to be stored from the old system and reloaded to run on the new 930. To gain performance of two to three times over the current top-of-the-line machine, the HP 3000 Series 68, programs and applications have only to be recompiled. The new optimizing compilers take advantage of the performance attributes of the new architecture.

The Precision Architecture is also scalable—that is, independent of circuit technology—because it consists of a basically simple architectural core that gives HP's system designers broad flexibility for implementation. Systems in this architecture can represent an extremely wide performance range because the architecture and instruction set can be implemented in any hardware technology.

For instance, TTL is represented in the first Precision Architecture product, the HP 3000 Model 930, and HP's NMOS III in the second product, the HP 3000 Model 950. Planned for the future are fast emitter-coupled-logic systems. Beyond that, the architecture could be implemented in even faster circuit technologies such as gallium arsenide, which HP engineers are currently researching.

Not only is a changeover made easy for the customer, but once accomplished, it will be a long time before another will be required. Because the HP Precision Architecture yields unified systems and is both scalable and upwardly compatible, software application systems built on it are designed to last into the next century, according to the company.

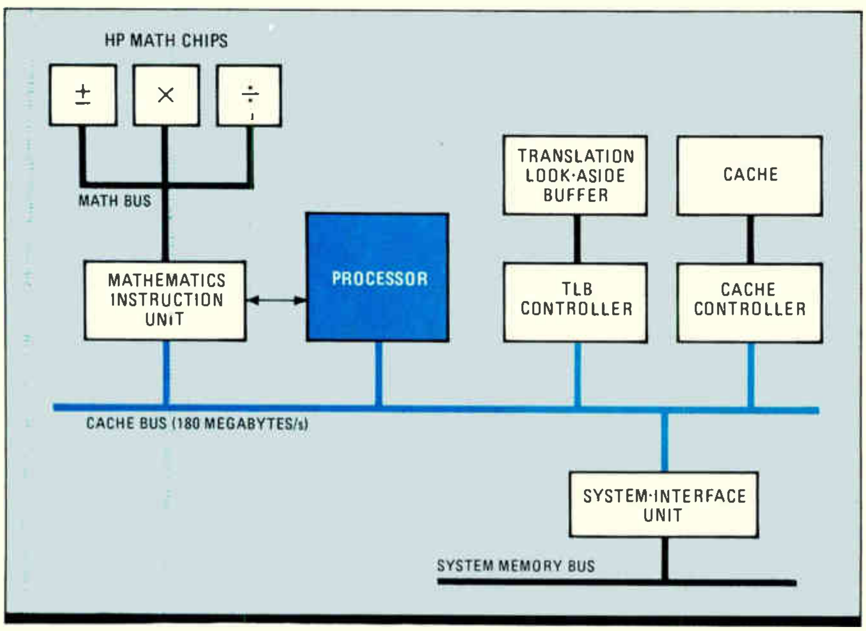
KEEPING IT SIMPLE

Simplicity was achieved by applying a strict engineering discipline to the design. "It's the best-measured architecture ever done," says Joel S. Birnbaum, vice president and director of Hewlett-Packard Laboratories. The engineered architecture was made possible by two types of extensive instrumentation and measurements.

First, instruction-execution frequencies were measured heavily to see what was going on in a central processing unit, memory, and I/O hierarchy. Second, and perhaps more important, according to Birnbaum, were the measurements done on hundreds of customer jobs for over 100 customers in HP's three computer markets. Codes representing billions of instructions were run and analyzed by the Spectrum team to determine an instruction set best suited to serving customer applications.

The small set of directly executed hardwired instructions is one of the key engineering achievements in the design. Yet a reduced instruction set itself was not a design goal—it was a result of the instrumented and engineered design. No instruction was included until it was thoroughly analyzed and unless it paid off in performance and cost/performance considerations (see "Multiply didn't make the cut," opposite). "If a feature has some value, put it in if it pays its way. In other words, you don't do it unless you have a reason for it," says Birnbaum.

The HP Precision Architecture grew partly out of previous work done on what is now called reduced-instruction-set-computer architecture (RISC). One discovery that came out of early instruction analy-



2. HELPING OUT. The math chips and instruction unit assist the processor in the central processing unit of the HP 3000 Model 950, the second machine to use HP's new architecture.

A SIMPLE DESIGN MAY PAY OFF BIG FOR HEWLETT-PACKARD

SPECTRUM: GAMBLING FIVE YEARS OF R&D TO CATCH UP IN COMPUTERS

It has taken five years for Hewlett-Packard Co. to come up with a new generation of computers, but its customers may find that the wait was worthwhile. The new family, code-named Spectrum, is coming just in the nick of time. HP has been supporting three computer lines, two of them based entirely on aging 16-bit architectures in a time when its major competitors have long since turned to 32-bit designs. Moreover, the three architectures are incompatible, and computer users are looking for the kind of unified line that the Palo Alto company's major competitors have long been pursuing.

Yet the task of updating all three architectures would have been a crushing burden, even for HP. So the company took a bold step: a five-year program to replace the three architectures with one. The result is the HP Precision Architecture, which will be the common core for a wide variety of computer systems and computer-based instrumentation that will carry the company into the 21st century.

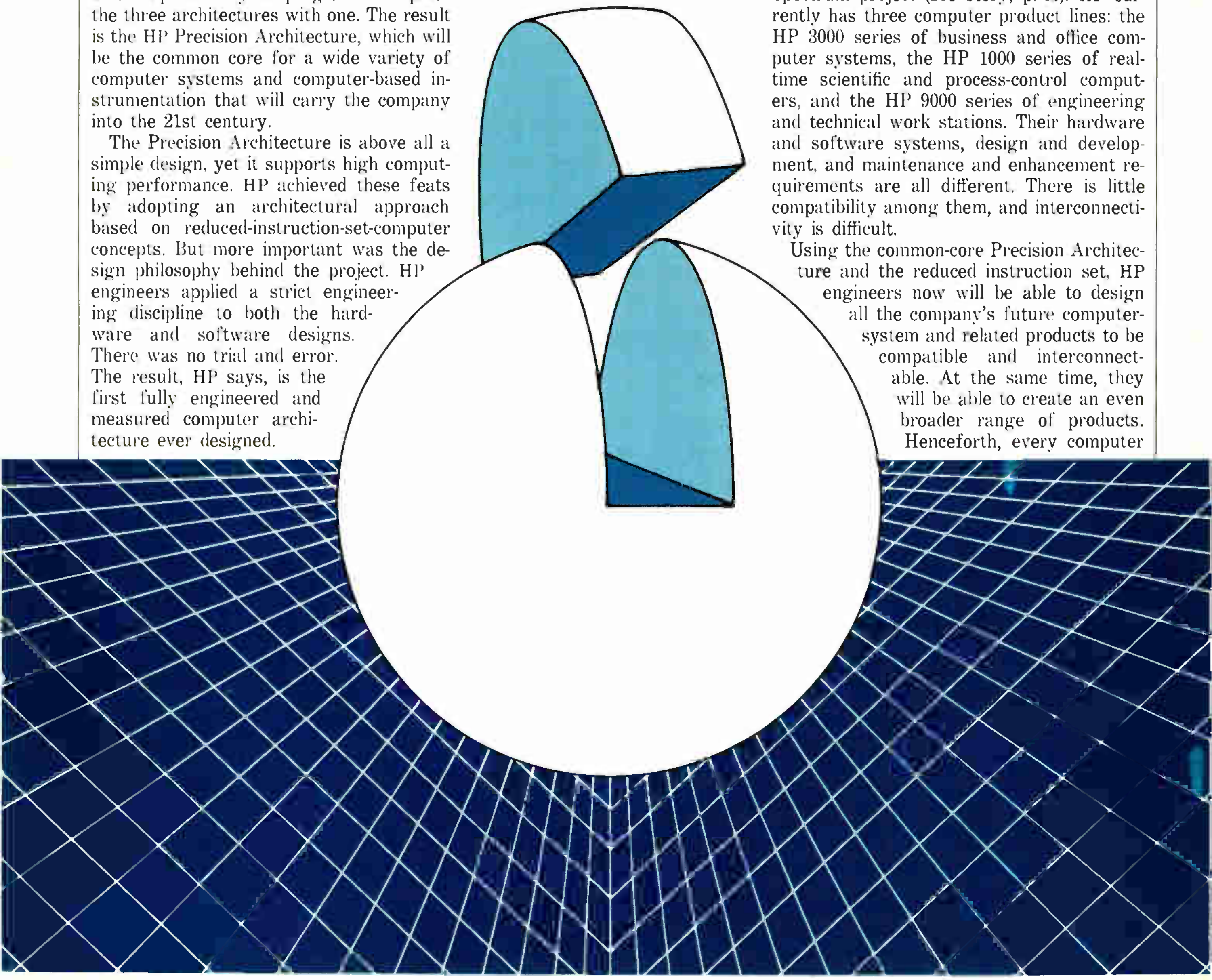
The Precision Architecture is above all a simple design, yet it supports high computing performance. HP achieved these feats by adopting an architectural approach based on reduced-instruction-set-computer concepts. But more important was the design philosophy behind the project. HP engineers applied a strict engineering discipline to both the hardware and software designs. There was no trial and error. The result, HP says, is the first fully engineered and measured computer architecture ever designed.

The massive Spectrum project had as its goals four major benefits for both the company and its customers: unity and compatibility among systems, scalability to circuit technologies, and longevity.

The architecture is based on several simplifications of existing designs. Most prominent of these are a reduced number of simple, regular instructions that have the same length and format, a large set of 32 general registers, a new class of subroutines, a memory cache that is easily managed by software, memory-mapped input/output functions handled like memory, and an optimizing compiler system that generates code matched to the architecture.

A unified product line was one of the major goals of the Spectrum project (see story, p. 45). HP currently has three computer product lines: the HP 3000 series of business and office computer systems, the HP 1000 series of real-time scientific and process-control computers, and the HP 9000 series of engineering and technical work stations. Their hardware and software systems, design and development, and maintenance and enhancement requirements are all different. There is little compatibility among them, and interconnectivity is difficult.

Using the common-core Precision Architecture and the reduced instruction set, HP engineers now will be able to design all the company's future computer-system and related products to be compatible and interconnectable. At the same time, they will be able to create an even broader range of products. Henceforth, every computer



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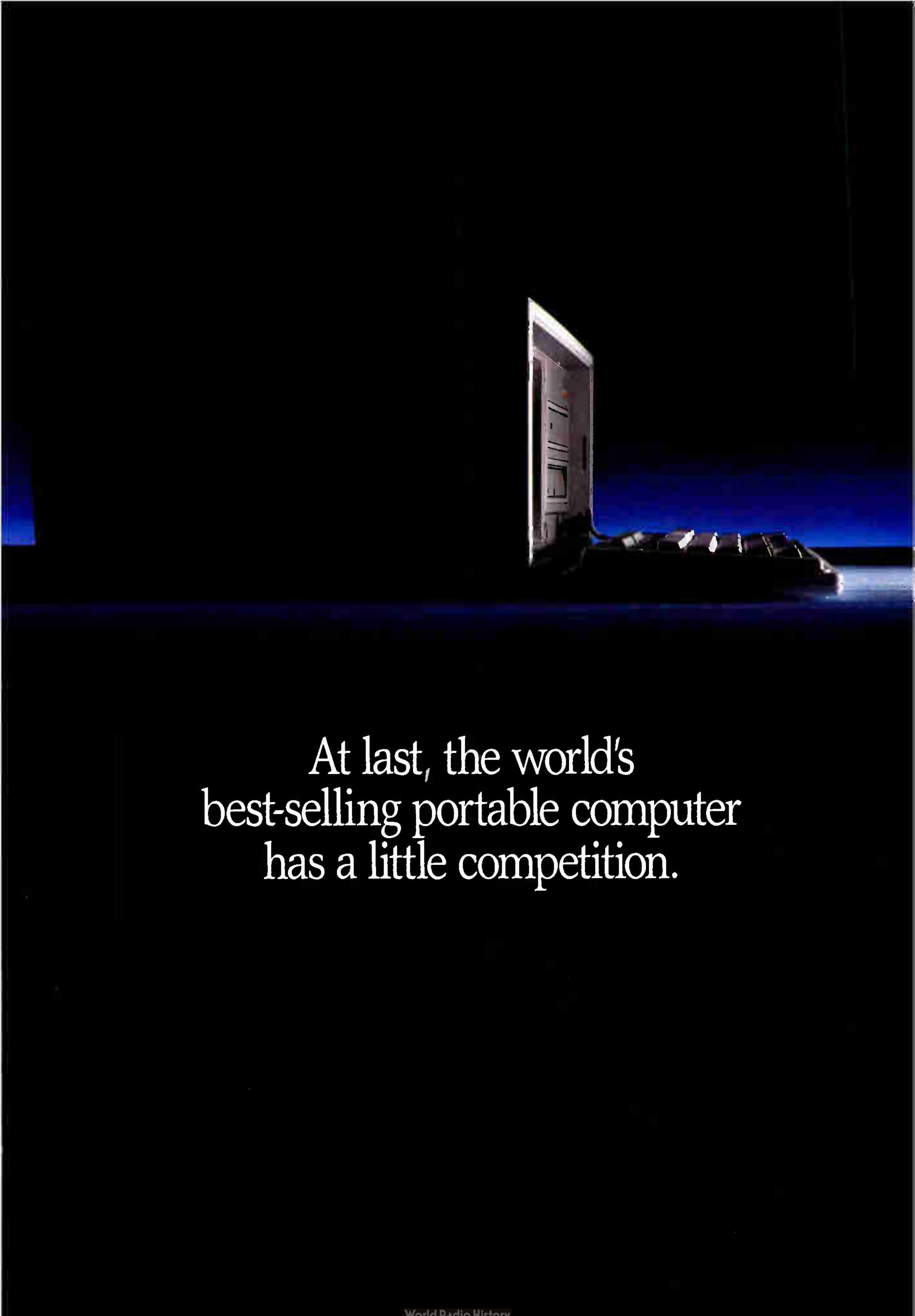

At last, the world's
best-selling portable computer
has a little competition.

guage that provides iterative control of the system's functions. Ordinary ASCII files represent the complete command structure of the tester. These commands can be embedded into the program language for such tasks as strobe-timing tests (changing variables incrementally until the DUT goes in or out of tolerance limits). The language provides control of each measurement subsystem through easy-to-remember, three-letter acronyms. These input/output statements can be embedded in the program language of choice—Fortran, Pascal, Basic, C, or whatever language is used to program the host system. The resulting program places a great deal of flexibility in the hands of an engineer who is not a test specialist. The user can readily increment a voltage level or current quantity, or change a critical timing specification, for example, while querying the system for a failure.

ANY HOST WILL DO

The Logic Master is also integrated with the PMU to run test programs designed to execute on any host computer. Because of the Logic Master's resident 8088-based controller and read-only-memory-based firmware, the host can be as simple as a VT100/ANSI 3.64 terminal or virtually any computing or terminal-emulation environment. "More than 50% of our customers use a stand-alone IBM Personal Computer," notes Lindsay, "while others tie into a work station such as an Apollo. In either case, the host computer is most often used to save and store files and perform some data-reduction function."

One example of the system in action is testing for leakage current. This procedure is assuming special importance now that CMOS has become the process of choice for high circuit density, good electrical noise immunity, and all-important low power dissipation. Theoretically, CMOS gates draw no current unless switching. Thus gross leakage is a good indicator of an IC's electrical quality.

A PMU leakage-test sequence will power up a device, precondition internal states if the device has sequential logic, and measure either I_{ss} or I_{dd} in the V_{ss} or V_{dd} leads, respectively. Generally, such tests reveal whether a particular fabrication process has worked at all; if the gross current leakage is high, it usually indicates that the process has slipped. IMS engineers established the PMU to address the need for conventional bipolar and n-MOS—as well as CMOS—parameter testing.

The PMU features force-and-measure subsystem autoranging (which can be overridden), two timing channels (clocked or strobed) for every 16 channels of data, a maximum 3-ms measurement time, and a 3.5-ms settling time to within 0.1% of the programmed change once a voltage or current is forced. To improve resolution, IMS provides a dual-range voltage and a triple-range current subsystem (Fig. 3). Voltages can be forced in two ranges—±2 V or ±20 V. Accuracy, on a par with other PMUs, is within 0.05% of any setting; at an ambient temperature of 25°C, there will be a worst-case error of 1 least significant bit and 2 mV. Current can be sourced or sunk to any point with a choice of a 0-to-1-mA, a 0-to-10-mA, or a 0-to-100-mA range. Accuracy is within 0.05% of a setting (at plus 1 LSB and 2 μA at 25°C). On the lowest range, current quantities can be resolved to 500 nA. Current can also be measured over six ranges between ±1 μA and ±100 mA with a spec-sheet accuracy of 0.05% of reading (at plus 1 LSB and 2 nA).

Integral to the system is a high-accuracy dc voltmeter with a 10-MΩ input impedance, which can be used separately. Offering three full-scale voltage ranges spanning 200 mV to 20 V, the voltmeter features 0.05% of reading accuracy (at plus 1 LSB and 200 μV). Resolution of 100 μV is possible on the lowest range, which makes the voltmeter a laboratory-grade instrument. The PMU's switching matrix and low-capacitance test fixture feature four force-and-measure channels, individually selectable and programmable to any channel. The PMU is the primary input to the matrix, but the three other inputs can be switched; connectors are installed on the test head. There is also one unassigned input and two low-impedance 50-Ω analog stimulus ports for future enhancements. □

MAKING DESIGN VALIDATION USER-FRIENDLY

One reason high technology industries have taken off in the Portland, Ore., area is the abundance of Tektronix-spawned expertise in the local workforce. In fact, two ex-"Tekkies" were key players in developing Integrated Measurement Systems' parametric measurement unit.

David McCracken, IMS's senior engineer, got his start at Tektronix back in 1968. He subsequently worked in the firm's Automatic Test Systems Division, where he honed his hardware engineering skills. John Miller, senior software engineer, spent his formative engineering years developing both the widely used Tektronix Model 1240 Logic Analyzer and the Digital Analysis System.


HARDWARE. David McCracken developed the PMU hardware.

Both McCracken and Miller looked at the impact the burgeoning semicustom integrated-circuit industry was having on the average circuit designer. Both were convinced a low-cost but user-friendly approach to design validation was going to open vast new markets for startup IMS, so they eagerly joined the fledgling firm. Their efforts have changed the design environment forever.

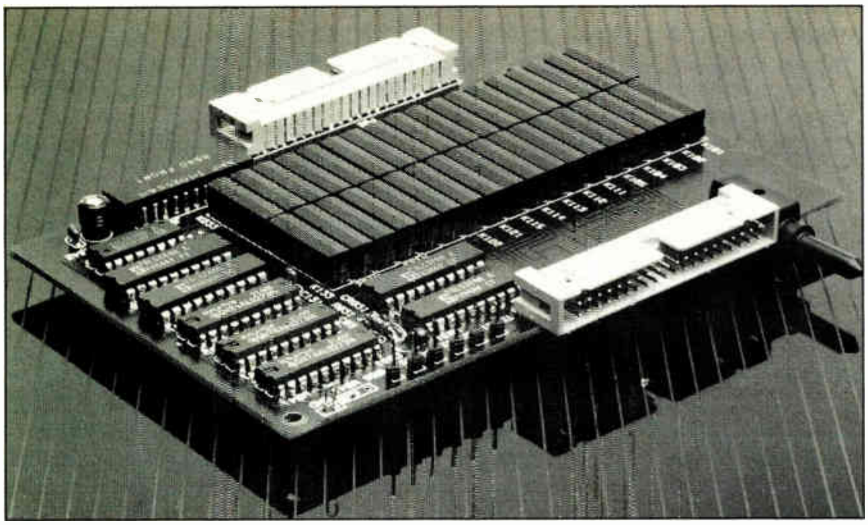
At IMS, McCracken set about designing the PMU while Miller attacked the software and user interface. Miller was on the job with IMS only three days when he was assigned the PMU project. One of his first tasks was marrying parametric testing with the existing Logic Master screen interface.

"I envisioned two types of users," says Miller. "One is the analog designer who knows a lot about parametrics and wants his hands on the control functions of the box. I had to give him full power to be able to put tests where and when he wanted to, and to set limits. The other guy is the one who really doesn't want much to do with parametrics. He knows he has to perform the measurements, but he's a digital designer at heart, and less concerned with the analog aspects of the parts."

The challenge for Miller was to satisfy both types. As he considered the project, he was struck with an inspiration: allow the software to run the test vectors, and stop when a pin is toggled. Then the parametric test would be applied, thus automating the process. Miller went about writing the code, and IMS Automeasure was born.

"We set our targets, define them, and work to meet deadlines," says Miller. They both agree it's one of the joys of working for a small company. "Large companies keep moving the target out. They keep redefining their goals," Miller says. □


SOFTWARE. John Miller handled the software and user interface.



2. REED RELAYS. A compact plug-in relay card is at the heart of the PMU's matrix. Silver contact potted reed relays and high-quality connectors ensure accuracy and reliability.

installations would cost four to five times as much as the new IMS unit. Silicon foundries will undoubtedly also use the Logic Master PMU to ensure support for their customers during the early phases of a design's verification. The effects of processing on pulse skew, drive capability, and thresholds have become of major concern to those designers savvy enough to realize they can't leave this responsibility to fabricators.

SOFTWARE KEYS

While designing the PMU, the engineering team at IMS knew it was important to ensure ease of use. They realized that very few engineers specialized in test engineering, few were well versed in analog systems, and fewer still would consider parametric testing unless it was easy to implement. "Most digital designers don't place parametric characterization at the top of their design approach," notes Lindsay.

Thus the company decided that easy-to-learn "pop-up" on-screen menus would be the best way for the typical circuit designer to learn the system. Called up by a single keystroke on a single Logic Master screen, the menus let the novice user quickly specify the type of test and the limits expected or encountered. Parameters displayed on the menus can then be entered easily and edited quickly.

To make it easy to get up and running, parameters are already established for common logic families such as low-power Schottky TTL or 10K ECL. They need only to be called up; other thresholds don't have to be established unless the operator wishes to override the preset values, which most users will do once they're familiar with the system.

Operationally, the host Logic Master can go in anywhere in the functional test pattern and insert parametric measurement statements. Users can then run a part to a specified state, hold the test vector of interest, and make a parametric test measurement.

A single keystroke begins the measurement sequence, with software looking for the first high and low logical event that occurs on each pin as the functional test pattern exercises the part. Then the system automatically routes the parametric stimulus and measurement to the pin. The user-friendly interface also provides a description of the program flow with halts and reinitialization. It is an extension of the Logic Master's screen interface that provides power-up system configuration, resource assignment (naming and organizing device signals), operational conditions, and pattern control.

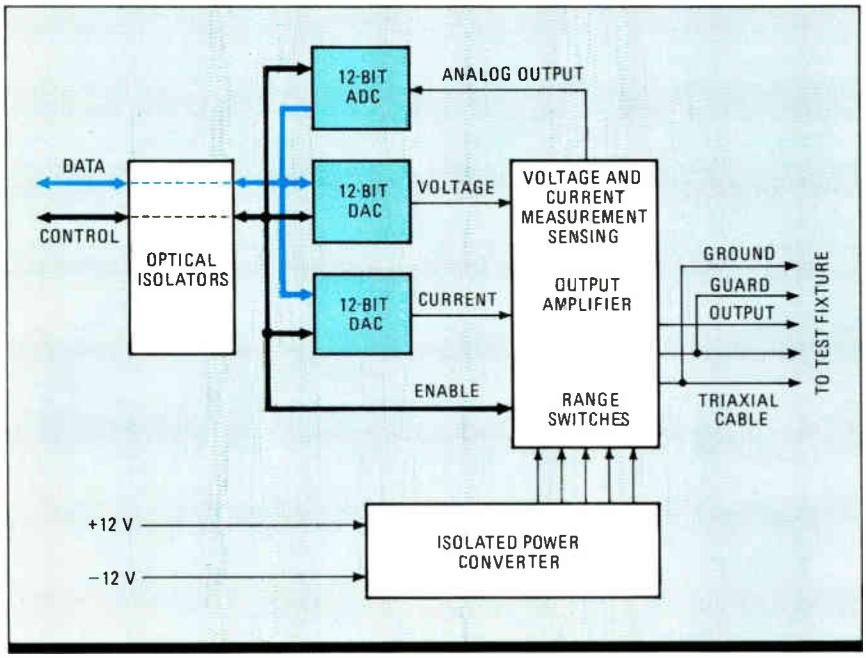
All measurements are clearly displayed, with voltage and current values shown pin by pin in a tabular format. Limit, error, and untested-pin indications are also provided to alert the user to out-of-range values or untested or missed pins. This feature also serves to flag incomplete functional test-pattern coverage—an added debugging bonus that verifies that pins are exercised, allowing upgrading of test patterns.

If the engineer conducting the test wishes to override the software-driven program, he can intervene manually. The operator simply enters the functional test-pattern screen display and selects a parametrics menu. A window is then moved over the functional vector, showing where the parametric test will be made. No cumbersome connect statements need to be added to test programs. Users can specify measurements for any device pin at specific pattern locations; worst-case analysis can thus be readily forced. The manual mode can also save time by sidestepping the requirement for multiple reinitialization occurring under the automatic mode. If desired, manual and automode operation can be combined for maximum effectiveness and enhanced throughput.

In a third mode—the interactive measurement mode—users can make measurements on a displayed pin group while executing a particular single test vector. This enables the user to make changes by writing a single vector and immediately viewing the results of the measurement.

Finally, a summary-of-coverage list is generated—in any of the modes—to help assess fault coverage and debug a test pattern. This is essential, considering the huge amounts of data generated by testing a VLSI device with a high pin count.

The PMU's host—the Logic Master—includes a standard full-command lan-



3. ACCURACY. Resolution equal to costly ATE is made possible by 12-bit data-converter stages, opto-isolators, and dual-range-voltage and triple-range-current subsystems.

NOW IC DESIGNERS CAN VALIDATE THEIR OWN PROTOTYPES

LOW-COST MODULE DELIVERS EASY-TO-RUN PARAMETRIC TESTS

1. HOST MAINFRAME. The host-independent Logic Master now accommodates a PMU, thus combining parametric evaluation with pattern generation, data acquisition, device powering, and fixturing.

Parametric tests that measure and verify a prototype integrated circuit's electrical characteristics can be instrumental in ensuring the soundness of a new chip design. Early discovery of major failure modes can spell the difference between success and costly postproduction engineering changes. Indeed, parametric testing is becoming mandatory as the complexity and pin counts of ICs continue to increase.

Until now, ready-to-run parametric measurement units (PMUs) have been adjuncts to large and costly automatic-test-equipment systems. As such, they have been relegated generally to production testing applications. Now Integrated Measurement Systems Inc. has come up with a low-cost, user-friendly approach that brings parametric testing to the IC designer. It is introducing a $19,200 dc PMU module.

The module is available as a one-slot plug-in for use with the Portland, Ore., company's Logic Master series of 20-MHz prototype-verification systems (which are priced from $29,500 to $41,500), and it combines the power of easy-to-use proprietary software with exceptionally high pin-count test fixturing and drive and measurement electronics. PMU-equipped IMS Logic Master systems now provide not only functional and timing characterization but also absolute parameter limits that reveal an IC's quality. The system (Fig. 1) is also designed to be accessible to the testing novice, thanks to its automeasure (automatic operation) mode.

Users control the system with interactive software. It can test ICs that contain as many as 384 pins. Because the interface between the PMU and the IMS Logic Master conforms to the IEEE-488 bus specification, even those companies that do not have a Logic Master can use the new PMU; virtually any IEEE-488 system can run the IMS module.

Test-system makers have emphasized functional testing in the past few years, says IMS director Ken Lindsay. Parametric testing was performed mostly by silicon foundries seeking tighter control over their products. But designers "were pushing the limitations of vendor design centers," he says. "So we decided it was high time that IC and systems designers had dc parametric test results available for verification during the design process. before commitment to large runs."

The increased complexity of today's devices shifts the responsibility for testing from the silicon foundry over to the chip designer. "They need design tools so they can talk back and forth with the foundry to get the part right," explains Lindsay. "By the same token, vendors who don't want to tie up their million-dollar Sentry [ATE] systems for debugging are keenly interested in our approach, too."

The IMS PMU offers equivalent or better accuracy and resolution than a Sentry/Schlumberger or GenRad Inc. PMU, Lindsay claims. "It's just not optimized for high throughput. But in the engineering environment, who cares? It doesn't much matter whether a single-pin test takes 100 ms or 10 ms."

A high-quality but inexpensive silver-contact reed-relay switching matrix—the verification station—lies at the interface to the device under test (Fig. 2). An associated fixture board connects the PMU to any given pin of the DUT; this enables the user to apply voltage to take current measurements or to apply current for voltage measurements, and to measure total leakage current, referred to as gross leakage current. Drivers and receivers are automatically disconnected to ensure that only the device under test—and not the test-head electronics and probes—is being measured.

The fixturing board is identical to that supplied with the IMS Logic Master, so IMS customers with Logic Masters can add the PMU as a field-installable upgrade to their existing fixtures. Plug-in probe cards and cable interfaces can also accommodate wafer-probe parametric testing. For this reason, the company expects some users to put IMS PMUs in fab areas where dedicated million-dollar ATE can't be placed cost-effectively to look at first silicon parts quickly. The PMUs in such

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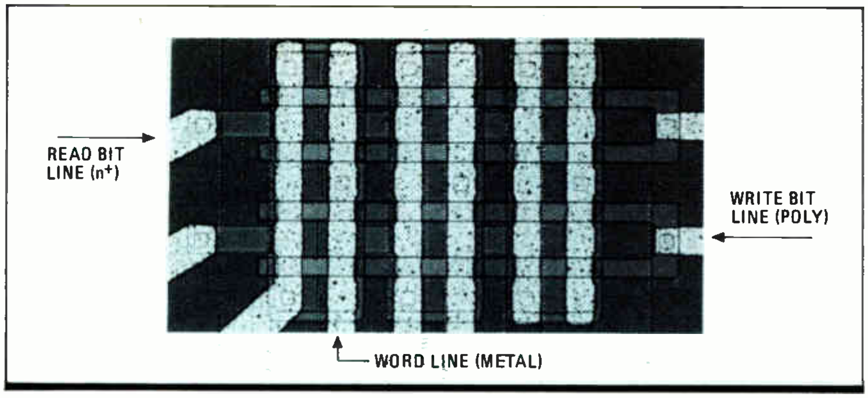


7. SMALL CELLS. A junction-CMOS cell-array structure from the University of Waterloo incorporates 100-μm DRAM cells—about half the size of current designs.

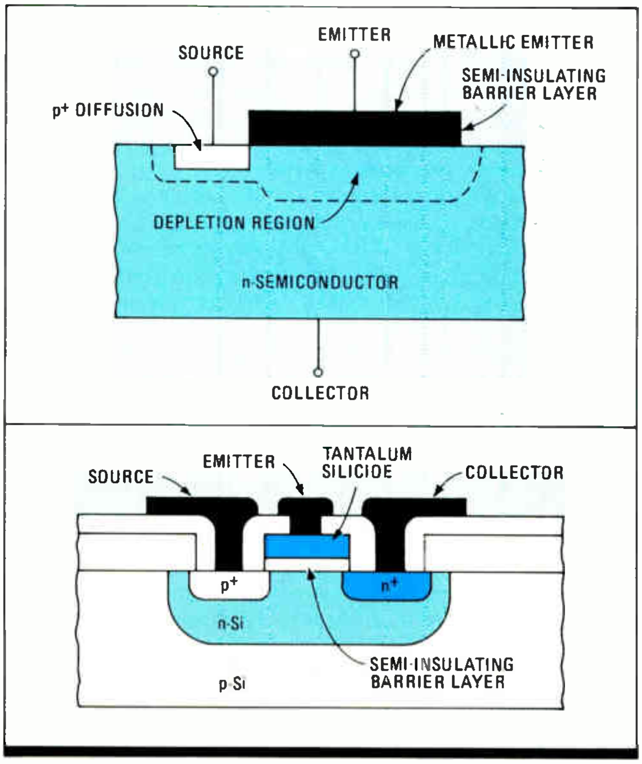
structure significantly improves reading and writing speeds, he adds, and it promises megabit designs operating at speeds equivalent to the fastest 64- and 256-K DRAM designs.

The use of such a hybrid structure offers several advantages over traditional approaches, says Elmasry. First, because the surface MOS transistor operates in the accumulation mode, storage capacitance as well as the sensitivity of the read current to the stored data is improved. Second, the use of the JFET as a sensing device, rather than a MOS FET, eliminates the latter's short-channel effects. This means much smaller cells can be fabricated. And because of its bipolar structure, the JCMOS cell has a much larger readout signal than present one-transistor configurations, so different sensing techniques can be used. "As a result, the sense amplifier can be integrated into a much smaller area compared to present one transistor cells, but with much larger readout signals," says Eldin.

"Moreover, since the magnitude and duration of this current can be controlled directly, through proper design of the word-lines bias circuit, high writing speeds are possible," notes Elmasry. "Also, since this design uses a nondestructive reading technique, rewriting is not necessary, resulting in much shorter read cycles than are presently possible."

Another significant plus in favor of the bipolar-CMOS structure, say the two researchers, is that it can be implemented by most existing CMOS processes with only minor modifications. A particularly good match is standard twin-tub CMOS, because a single n well is shared by a large number of cells. Using 2.5-μm design rules, a cell array fabricated using this technique (Fig. 7) results in an area of 100 μm, compared with 170 to 200 μm for a standard one-transistor cell with the same feature sizes. A shift to 1.5-μm design rules would allow cell sizes approaching 10 μm^2. And by using trench-isolation techniques and trench capacitors, even denser arrays are possible. With minor modifications, the same JCMOS structure can build very high-density VLSI logic chips, the researchers say.

Another intriguing approach is embodied in the work of Geoffrey W. Taylor and John G. Simmons at AT&T Bell Laboratories, Murray Hill, N. J., who have developed a solid-state device they've christened Bicfet, for bipolar inversion-channel FET. Relying on the field-effect inducement of an inversion layer (Fig. 8), which corresponds to the conventional neutral base of a bipolar transistor, the Bicfet has a three-terminal structure: a metallic emitter that makes ohmic contact to a semi-insulating wide-bandgap semiconductor; a source that contacts the inversion layer formed at the interface between the semi-insulator and the semiconductor depletion region; and the bulk silicon substrate, which acts as the collector. According to Taylor, the Bicfet works by controlling the flow of majority carriers through the semi-insulating region to the collector by the biasing action of charge in the inversion channel.



8. BELL'S BICFET. Key to operation of Bell Lab's bipolar inversion-channel FET is the absence of a base layer.

NO LIMITS TO SCALABILITY

Featuring very high current gains (approaching 10,000), very high current operation (1 million A/cm^2) and low capacitance, the key element in the Bicfet is the absence of a base layer and all its associated problems. "By far the greatest advantage of such a structure is the fact that the Bicfet is not subject to the scaling limits in either the vertical or planar dimensions," says Taylor.

Unlike a standard bipolar structure, a Bicfet has no base to limit scaling in the vertical direction, and unlike a MOS FET, it has no drain to limit scaling in the planar direction. Thus, says Taylor, it is an ideal candidate for scaling down to 0.1 μm and below. Also, since it has no base, a Bicfet has a much lower capacitance than a conventional bipolar transistor. This low capacitance, coupled with high transconductance, results in very high speeds—in the sub-picosecond range—in both analog and digital applications.

To date, Bicfets have been fabricated only with III-IV materials such as gallium arsenide or indium phosphide, says Taylor, because the structures require molecular beam epitaxy, rapid thermal processing, and other advanced techniques. Such techniques are becoming common in the fabrication of ICs based on heterojunction compounds, such as aluminum gallium arsenide, but are not in general use for fabricating silicon chips.

Among other things, fabrication requires laying down extremely thin semi-insulating silicon-rich silicon oxide layers, to build the necessary high-gain heterojunction structures, and the use of silicides, to implement self-aligned source junctions. "But if there were no other way to get down to the low end of the submicron range with silicon structures, the investment would be worth it," he says. □

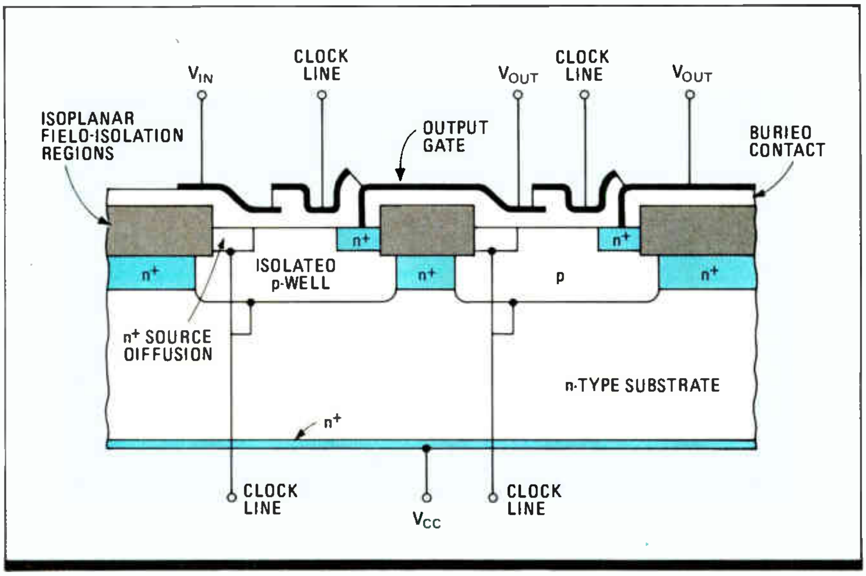
use of dynamic logic with inverters in the form of a charge-pumped load circuit or a bipolar load element. Where high drive capability is required, as in very large dynamic logic arrays, the charge-pumped load is replaced with a dynamic vertical npn bipolar load driven by one of two clock lines (Fig. 5).

For serial memory and logic applications, this design has several features that offer significant density advantages over traditional techniques. The p-well and the base region are merged, as are the drain and emitter region; the substrate supplies the ground line; and the source diffusion acts both as a virtual ground and as one of the clock lines. In addition, the design eliminates substrate charge-injection problems, and is thus insensitive to alpha particles.

Several European companies also are chasing niche applications, notably Telefunken electronic GmbH, a joint venture of AEG AG and United Technologies Corp., Hartford, Conn. Telefunken plans to apply its BiCMOS process to digital radio and TV, interface and signal processing, data collection and conversion ICs for automotive applications, and telecommunications [*Electronics*, Jan. 6, 1986, p. 23]. This year, the Heilbronn, West Germany, company will introduce its first products based on its 2-μm BiCMOS-1 process, which makes use of an n-well on a p-type substrate with a p-type epi layer. The bipolar side has self-adjusting vertical npn and pnp transistors in their associated n-wells.

Telefunken's current 2-μm BiCMOS-1 packs about 3,000 transistors/cm^2. Gate delays on the CMOS side are less than 2 ns, and cutoff frequencies for npn transistors are from 1 to 1.5 GHz at 10 V. On BiCMOS-2, scheduled for the end of 1988, gate geometries will be about 1 μm or below, resulting in packing densities of about 10,000 transistors/mm^2, or about 100,000 transistors per chip. Cutoff frequency for the bipolar transistors is expected to be in excess of 2 GHz.

Italy's SGS-ATES SpA is pursuing applications that require high-density logic and the ability to drive high voltages, such as automotive electronics, printers, display drivers, motor controllers, TV circuitry, and protection circuits. The two requirements are met with a process that combines isolated double-diffused MOS transistors with bipolar and CMOS structures, says David J. Hage, marketing director at U. S. subsidiary SGS Semiconductor Corp., Phoenix. Called Multipower BCD, the process combines a potpourri of structures, including self-aligned vertical DMOS n-channel gates, lateral DMOS transistors, p-channel MOS FETs with drain extension, CMOS transistors, bipolar npn and pnp transistors, junction and poly resistors, and oxide and junction capacitors.



5. MERGED BIMOS LOADS. Targeting dynamic logic applications, Wafer Scale Integration Inc.'s dynamic merged-load technology combines a CMOS inverter with bipolar load elements.

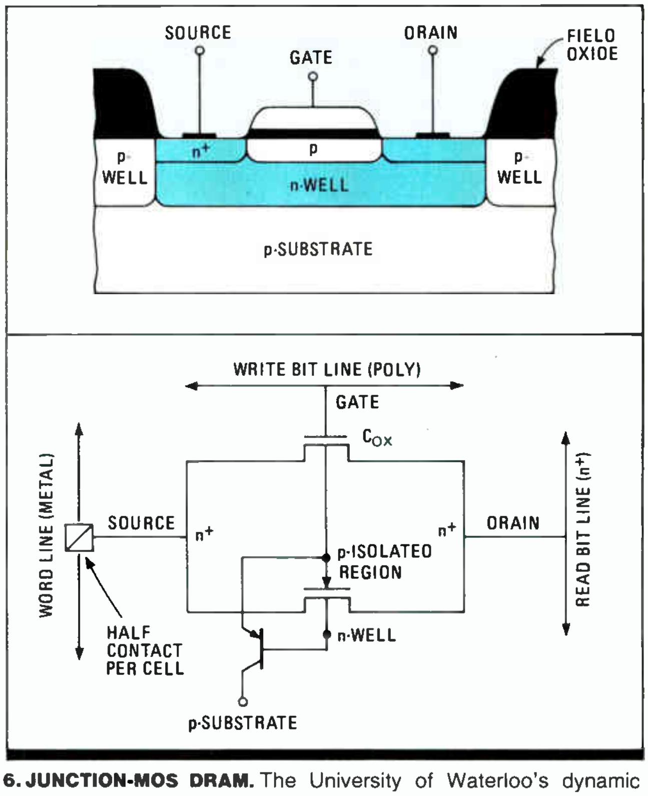
MEANWHILE, BACK IN THE LABS

As if designers did not have enough on their mixed bipolar-CMOS plate, a number of new structures and processing alternatives are emerging from university and private research laboratories. They promise even more tantalizing opportunities for combining high performance and low power.

Rather than look for ways to merge traditional CMOS and bipolar structures, the University of Waterloo's Elmasry and Ali G. Eldin, a doctoral candidate, are taking a different tack. "We are going back to the basics, looking first at the basic requirements of the VLSI environment, then developing a structure that meets them, and finally, building a process to implement it," says Eldin. The first result of this effort is JCMOS, a novel junction CMOS dynamic-RAM structure. Its cell is no more than 10 μm^2 and is built with 1.5-μm design rules equivalent in size to those of current 1- and 4-Mb designs, which must use 1-μm geometries as well as exotic new structures such as trench isolation, trench capacitors, trench transistors, and stacked transistor structures [*Electronics*, Dec. 2, 1985, p. 50].

According to Elmasry, this new structure (Fig. 6) merges into a single cell three basic elements—a surface n-MOS FET, which stores data and acts as a MOS capacitor when it is turned off; an n-channel JFET, which senses the data; and a pnp transistor, which writes data into the cell.

The JCMOS cell storage cell has better isolation than present designs, says Elmasry, and consequently has smaller leakage current and higher immunity to soft errors. The



6. JUNCTION-MOS DRAM. The University of Waterloo's dynamic RAM cell puts MOS-FET, JFET, and bipolar elements in one structure.

will be a family of low-power, three-state 74LS-type TTL chips in the fourth quarter. Also in the works is a mixed process aimed at high-density logic and memory.

Honeywell Inc.'s Signal Processing Technologies Division in Colorado Springs is leveraging its participation in the Defense Department's Very High Speed Integrated Circuits program to develop what it calls a bipolar enhanced MOS (BeMOS) process. An extension of Honeywell's single-layer-poly, two-layer-metal CMOS process, BeMOS adds only three masking steps to the original 11, says Ramish Sirsi, director of the company's data-acquisition product line. These are a capacitor poly layer, an active base implant, and fabrication of chromium-silicon resistors. Sirsi says initial plans call for use of BeMOS in custom and semicustom chips that require high-density analog and digital circuitry as well as in high-performance standard products, such as high-precision 12-bit analog-to-digital and digital-to-analog converters (Fig. 3).

BeMOS II, the current 3-μm version, yields gate densities as high as 8,000. Gate speed is 5 to 6.5 ns, cutoff frequency is 50 MHz, and analog performance is from 2 to 3 MHz. In the VHSIC-derived 1.25-μm BeMOS III process, densities approaching 40,000 gates are expected, says Sirsi, with gate speeds from 400 to 800 ps at a cutoff frequency of 200 MHz.

RECLAIMING THE MARKET

Fairchild Semiconductor Corp., Cupertino, Calif., is planning an entry into bipolar-CMOS technology to help reestablish its dominance in high-performance memory and logic [*Electronics*, Feb. 24, 1986, p. 72]. President Donald Brooks says the company has had an active program in mixed bipolar and CMOS processes under development for the past two years. "We see a number of application areas in which these types of processes will be integral to our high-performance strategy," he says. "Memories will be one of those areas. Mixed processes are also under consideration for at least two other segments of our product line. It is planned that at least two of our manufacturing facilities will run these types of mixed processes."

And RCA Corp., which pioneered the use of bipolar-CMOS in a family of linear products during the early 1980s, is considering an expansion of its process into other product areas. Aside from these major players, most efforts in mixed processing aim at meeting the performance and power requirements of niche markets. For example, Digital Equipment Corp. seeks to reduce the latchup phenomenon common to most CMOS processes as well as improve performance.

In Hudson, Mass., DEC designers have developed MCB, a bipolar-CMOS process combining fully isolated lateral npn bipolar transistors of low collector-series resistance with a 1.5-μm single-level-metal n-well CMOS process. Aimed at providing ECL performance and CMOS density and power savings for digital applications, MCB adds only two masking steps—a buried layer implant and diffusion sequence plus a tailored base ion implant—to a 10-mask CMOS process.

From Hughes Aircraft Co.'s Semiconductor Division in Carlsbad, Calif., comes an unusual process that mixes complementary vertical bipolar transistors (npn and pnp) with high-speed CMOS and trimmable resistors. Aimed at medium- and small-scale integration of analog and digital functions, the 1.5-μm process was an outgrowth of the company's participation in the VHSIC program.

The mixed complementary process takes two forms: a thin-epitaxy process designed for high speed and low voltage (below 10 V), and a thick-epi process that sacrifices speed for higher voltages. The thin-epi process realizes npn transistors with cutoff frequencies in excess of 5 GHz and pnp devices of over 2.5 GHz. Transistors made with the thick process perform at about half that speed.

Hughes uses two poly and two metal levels. Trench isolation, junction-isolated epi layers, and three buried layers create the complementary vertical bipolar transistors that are essential to achieving high-performance linear ICs as well as symmetrical clock drivers on the same chip, says BiMOS program manager Hank M. Gerard. "The bipolar capability is essential for low noise and wideband amplifiers and their high drive capability, while the CMOS is used for logic functions and sample-and-hold circuitry."

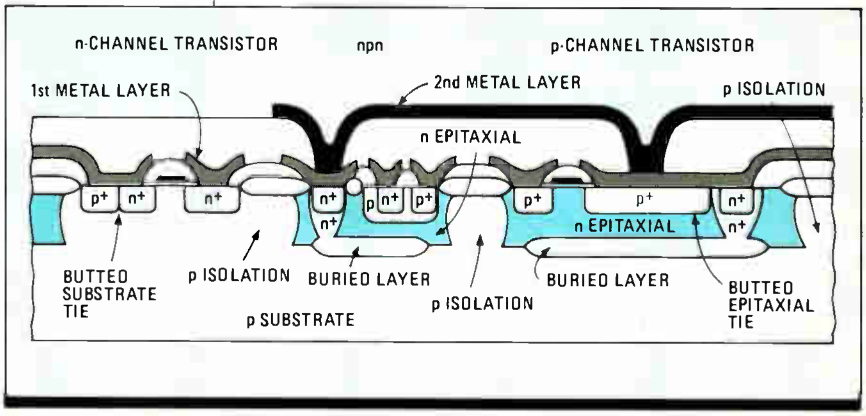
With 20 masking steps, the Hughes process is somewhat more complex and expensive than most other mixed processes. Gerard says the company has identified a number of applications in two market niches for which the added costs are well justified: analog circuits, where minimization of size or power is vital, and high-performance data conversion. Typical applications are in the military area, he says, such as combining analog comparators on an IC with digital multiplexers and implantable prosthetic devices.

Looking to take advantage of its highly reliable tungsten-fuse technology in a family of programmable logic devices, National Semiconductor Corp., Santa Clara, Calif., has merged a standard 3-μm junction-isolated bipolar process with a standard 2-μm local-oxide isolation CMOS process. The resulting structure (Fig. 4) consists of partially oxide-isolated bipolar transistors, p-channel devices isolated in the n-type epi layer, and n-channel devices in the p-isolation regions.

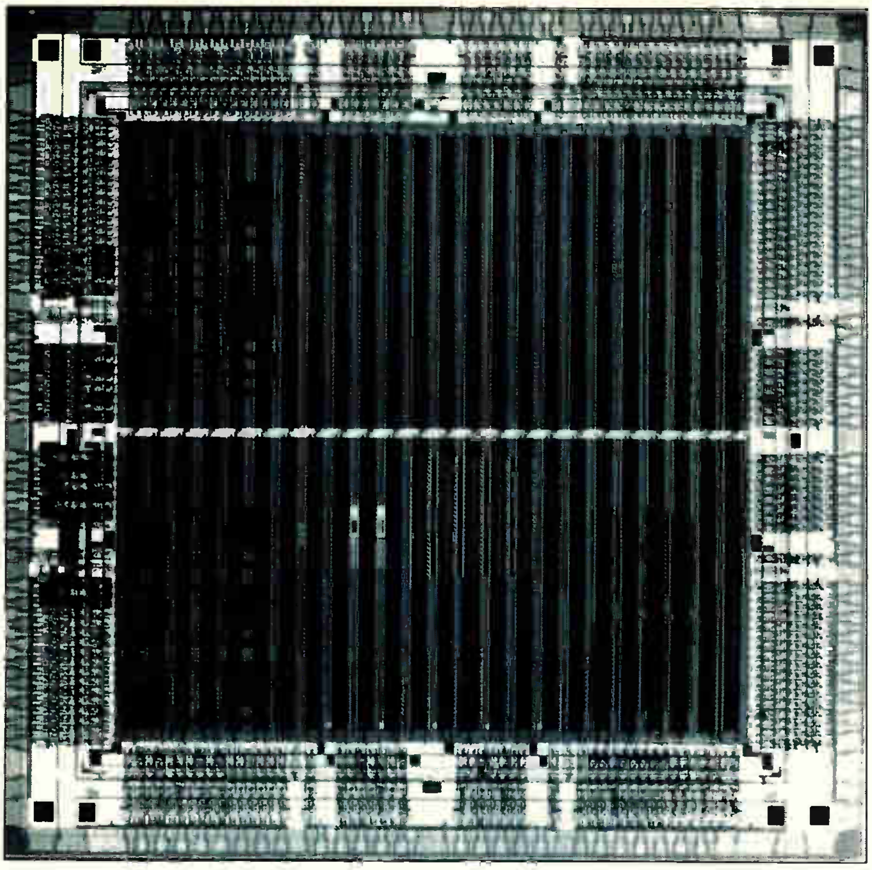
National's PLAs merge CMOS and bipolar technologies

A standard programmable logic array thus fabricated boasts 16 inputs, 64 product terms, 8 outputs, and 24-ns propagation delay. Active power dissipation is 625 mW and standby power is 5 μW. Bipolar devices are used in the programmable elements for the product-term array and the architectural configuration cells, while a merged bipolar-CMOS structure is used in the sense amps and in the internal data latch that holds the state of the AND/OR terms when the part goes into standby mode. During standby, all bipolar devices shut off and only zero-power CMOS devices stay active. An input-change detector circuit, previously unused in PLAs, reactivates the bipolar sections of the die whenever it senses input transitions.

A novel dynamic merged-load technology from Wafer Scale Integration Inc., Los Altos, Calif., targets such dynamic logic applications as low-power digital signal processing, serial memories and correlators, and digital image processors. Compatible with standard poly CMOS processing, the technique enables the



4. BIMOS FPLD. National Semiconductor Corp. combines 2-μm CMOS with 3-μm junction-isolated bipolar transistors to fabricate field-programmable logic devices.



2. HIGH DENSITY. Motorola's mixed-process array is highly dense, with 6,144 gates. The chip uses a variation of the company's BiMOS process that involves 15 masks.

tures 20-V breakdown on both bipolar and MOS transistors, gain as high as 100, and cutoff frequencies approaching 400 MHz. The bipolar side of an analog-digital chip made with this process holds a 2-MHz oscillator, an 80-mA bipolar power transistor, high-precision frequency control, and identification comparators. On the CMOS side is a 1,500-gate digital signal processor, an input data scanner and display decoder, and a programmable 280-bit SRAM. The high-voltage BiCMOS process requires a deep p+ diffusion for the power transistor and a local oxidation step to isolate the CMOS section.

Also in development at Takasaki is ABC, for Advanced Bipolar CMOS, a first-generation 3-μm process that merges npn, pnp, and integrated-injection-logic bipolar structures with p- and n-MOS transistors. ABC uses a 2-μm epitaxial layer to achieve very small high-performance (3-GHz) bipolar transistors.

Hitachi is not alone among the Japanese companies in its efforts toward development of high-performance bipolar-CMOS memory and logic circuits. From Ricoh Ltd., Ikeda, comes a 10-mask bipolar-CMOS process used in an analog-digital cell array aimed at semicustom ICs for printer interfaces, cameras, floppy-disk data-separators, telecommunications, and video recorders.

In the chip's digital portion is a metal-gate CMOS array of 405 two-input NAND gates (about 1,600 transistors); 30 input/output blocks containing a mix of npn, pnp, and n-MOS transistors; and 4-to-16-line decoder circuits. The linear portion incorporates 104 npn and 76 pnp transistors that can build up to 20 types of high-speed bipolar operational amplifiers, voltage comparators, and reference circuits; two pairs of p-MOS transistors, rated at 40-V breakdown voltage, for building MOS input op amps; four CMOS analog switches; and two large npn drivers with 60-V breakdown voltages for directly driving solenoids, lamps, light-emitting diodes, or for rapid charging and discharging of external capacitors.

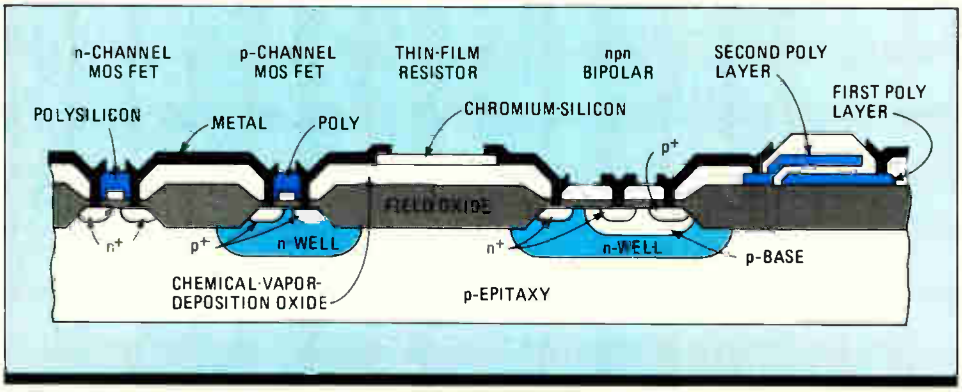
And at the upcoming Custom Integrated Circuits Conference to be held in May in Rochester, N. Y., a design team from NEC Corp.'s Application-Specific LSI Product Division in Kanagawa will describe a 1.6-μm-gate CMOS process that merges npn transistors with 1.5-μm emitters in a 3,100-gate array. The chip has an 800-ps internal gate delay and a 3-ns output buffer delay. Operating at 10 MHz, the chip dissipates only 1.2 W, enabling the use of low-cost plastic packaging.

In the U. S., only Motorola has an effort as sweeping and as aggressive as Hitachi's. Already a substantial presence in such market segments as mixed bipolar-CMOS linear chips, power transistors, and high-voltage interfaces, the company's Semiconductor Sector, Phoenix, Ariz., has developed a BiMOS process optimized for macrocell gate arrays.

The 1.75-μm BiMOS variation requires 15 masks and couples a twin-tub CMOS process to an n+ buried layer and p-type epitaxial layer. Bipolar npn transistors are built from a very shallow polysilicon emitter with four oxide walls and an active base formed in a manner like that required for the MOS buried-contact step. Used in the new MCA6000ETL macrocell array, the result is a 6,144-gate array with a two-input NAND gate delay of only 900 ps and a fanout of one (Fig. 2).

Texas Instruments also plans to be a dominant force in mixed bipolar-CMOS technology. The Dallas company will broaden its longstanding participation in mixed-process linear ICs with its BidFet technology and make a major push into the digital arena with Impact-C, which combines its new EPIC CMOS logic process with its Impact-S bipolar technology [*Electronics*, Dec. 23, 1985, p. 45].

According to TI's Stehlin, the approach is a twist on traditional mixed processes in that Impact-C is in essence a bipolar process to which steps have been added to form the appropriate n- and p-channel CMOS structures. TI's first products



3. BIPOLAR-ENHANCED. Honeywell Inc.'s 3-μm bipolar-enhanced MOS adds only three more masks to the 11 used in the standard MOS process in order to achieve 8,000-gate densities.

INSIDE TECHNOLOGY

MIXED-PROCESS CHIPS ARE ABOUT TO HIT THE BIG TIME

BIMOS AND BICMOS CHIPS ARE MOVING INTO MEMORY, LOGIC, AND ASICs

by Bernard Conrad Cole

Mixed bipolar-MOS processes are breaking out of their niche applications into the mainstream of semiconductor technology. Chip makers have long known that both BiMOS and BiCMOS can produce faster and denser integrated circuits than can either technology alone—but it has taken time to master the complex processing these ICs require. They also are finding that the fast-developing field of application-specific ICs is stirring new demand for designs that mix analog and digital functions. Companies around the world are making major investments in mixed-processing technology, most notably Hitachi, Sony, and Toshiba in Japan and Fairchild, Honeywell, and Motorola in the U. S.

The increased activity is having a synergistic effect on traditional niche-market suppliers of bipolar-CMOS integrated circuits, pushing new developments in the analog area, in discrete power transistors, and in high-voltage interface ICs. A host of other companies are entering the mixed-process fray, aiming at specialized niches, and research labs also are devoting more time and effort to the field.

Companies are investigating methods of merging or mixing bipolar and MOS structures on the same chip because it satisfies requirements that are ordinarily diametrically opposed, says Mohamed Elmasry, director of the very large-scale-integration group in the electrical engineering department at the University of Waterloo, Ontario. "On the one hand, in a BiMOS or BiCMOS circuit, one can take advantage of the MOS transistor's edge in packing density and ability to integrate large complex functions as well as CMOS's inherently low power dissipation, large noise margins, and noise immunity," he says. "On the other, one can take advantage of the bipolar transistor's advantages in switching speed, superior analog performance, and greater current drive per area."

The advantage in current drive is clear at high densities—for example, in memory circuits—when considering gate delay as a function of capacitive load, notes Robert Stehlin, new products and technology manager at Texas Instrument Inc.'s Logic Division in Dallas. "Ideally, at VLSI densities, what one would like is a bipolar device with the power dissipation of CMOS," he says. "In the absence of such an impossibility, a mixed bipolar-CMOS process technology does quite well."

For the same load, CMOS gate delays degrade by more than an order of magnitude over straight bipolar, compared with only 50% degradation for BiMOS or BiCMOS delays, says Elmasry. "This is becoming particularly crucial in high-density DRAMs. As the densities get higher, the interconnect gets longer, as does the delay time. BiMOS designs offer a way out."

These advantages have been apparent since the early 1970s, says Stehlin. "But at that point, bipolar and MOS structures required totally different techniques and tools to fabricate, and to design a mixed-process device meant considerable expense, only justified by high average-selling-price niche-market applications. Now, however, many of the features distinguishing bipolar and MOS technologies are blurring, especially at the VLSI level."

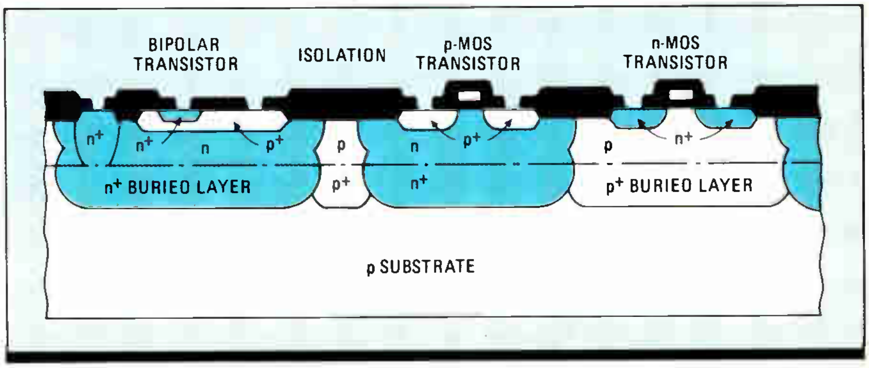
As a result, it is now possible to merge the two process flows such that both transistors can be optimized in a few mask steps. "Usually, depending on device parameters and application requirements, it is possible to develop a mixed process that requires no more than three or four additional steps, and often only one or two," says Elmasry.

THE JAPANESE CHALLENGE

The company with the most commanding presence in the development of mixed bipolar-CMOS processes for use in high-performance logic and memory has been Hitachi Ltd. Already in production is the Tokyo company's 800-ps/gate HGA 28 series of 2,500-gate arrays using its vaunted 2-μm BiCMOS process [*Electronics*, Nov. 5, 1984, p. 17]. Hitachi also plans to market a 25-ns 64-K static random-access memory [*Electronics*, June 3, 1985, p. 22]. More recently, Hitachi designers have developed HiBiCMOS, a 1.2-μm extension of this process, using a buried twin-well CMOS structure (Fig. 1). Gates have been fabricated with delays of 400 ns, about three to five times faster than CMOS gates of similar size.

Researchers from Hitachi's Device Development Center, Tokyo, described at this month's International Solid State Circuits Conference a 64-K SRAM fabricated using a mixed ECL-HiBiCMOS process [*Electronics*, Feb. 17, 1986, p. 23]. It features a 13-ns access time at an active power of about 500 mW—about half that of a conventional 64-K bipolar ECL RAM. Standby power is 350 mW.

For chips integrating high-density logic and analog circuitry, researchers at Hitachi's Takasaki Works, Gunma, have developed a 5-μm variation of the BiCMOS process that fea-



1. TWO WORLDS. Hitachi Ltd.'s HiBiCMOS process combines a buried twin-well CMOS structure with bipolar transistors on chip.

whether it could be done by using off-the-shelf gear. If that doesn't seem reasonable, the FCC asks for comments on a shift to such new technologies as amplitude-compandored sideband transmission, frequency modulation, and linear-predictive coding.

John J. Borkowski, an attorney in the special services division, says the commission's notice didn't specify technical requirements such as handshake parameters because it first wants to gather information on whether an evolution of the mobile-radio service toward narrower channels is technically possible.

In the past, the FCC notice contends, the service has provided relatively high-quality two-way communications, "but at a considerable cost in terms of both price and spectrum consumption." The

Mobile-radio users regard it as a spectrum takeaway

FCC's Kowalski acknowledges the opposition to the creation of the Consumer Radio Service, particularly from within the private mobile-radio community. But he says the commission will remain "open-minded about the pros and cons."

PETITION FILED. The call for comments stems in part from a petition filed with the commission last June by the Personal Radio Steering Group Inc., an Ann Arbor, Mich., organization created by several hundred private and business mobile-radio licensees. Its petition called for revising the mobile-radio service's rules to incorporate new technologies—but it seeks a 12- to 20-year transition period.

Corwin Moore, the group's administrative coordinator, says it has "long pushed for more efficient use of the spectrum," but he doesn't see the FCC proposal as the answer. "Rather than improving [the mobile-radio service], they're going to destroy it." So Moore's group is encouraging opposition to the FCC proposal and sending out literature to "several tens of thousands of people." He contends that "the commission has opened a tremendous can of worms," and argues that private-radio users could lose millions of dollars already invested in radio equipment.

The comment period for the proposal extends through June 30. At that point, the commission will evaluate comments before deciding whether to end the proceeding or issue a notice of proposed rulemaking. Kowalski expects a determination to be made "by the end of the calendar year."

But Moore thinks he already knows the outcome. "What they want is less spectrum for us." *–George Leopold*

MEDICAL ELECTRONICS

AN ELECTRONIC 'HAMMER' BEATS OUT X RAYS

ERLANGEN, WEST GERMANY

The age-old method of moving a tooth with a finger or an instrument to test its firmness could soon be replaced by an electronic diagnostic tool that gives more objective and scientific answers to a dentist's questions about a tooth's health. Called Periotest, the device points to developing diseases of the tooth-embedding tissue—diseases that cause a tooth to lose its firmness—long before they can be identified by X-ray analysis.

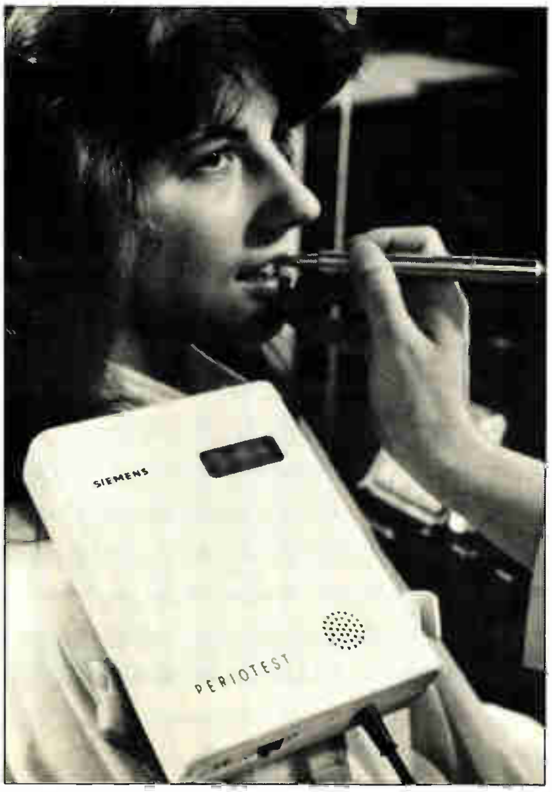
Periotest, a joint development of the Medical Electronics Group of Siemens AG in Erlangen, the University of Tübingen, and the Fraunhofer Institute for Information and Data Processing, in Karlsruhe, exploits relatively simple mechanical phenomena. A tiny, electronically controlled pin strikes the tooth. Periotest measures the time the tooth and pin are in contact, which is an indication of the damping characteristics of the bony tissue that embeds the roots and keeps the tooth in place. The device indicates the degree of firmness both visually and acoustically.

Consisting of a pencil-like handheld probe and a notebook-size microprocessor-equipped measurement and control unit, Periotest can determine if a tooth is too loose to support a bridge, how far along the decay of the gum's bone tissue may be, and what effect therapeutic measures will have on such decay or periodontal diseases.

CONTACT TIME MEASURED. In operation, the pin shoots out of the probe and strikes the tooth four times a second. The contact between the tooth and pin lasts about 1 ms, so little that the tooth's periodontal membrane, which covers the socket and cushions the tooth, does not appreciably deform. Neither does the impact cause any bleeding. Any periodontal disease causing a tooth to lose its firmness shows up because the contact time differs by fractions of a millisecond from that encountered with a healthy, firm tooth.

Using about 16 "percussion" signals to take a reading, the microprocessor in the measurement and control unit determines the average contact time. It also checks statistically whether these signals are plausible and disregards those that are too far off the mark. The result is the Periotest value of the tooth.

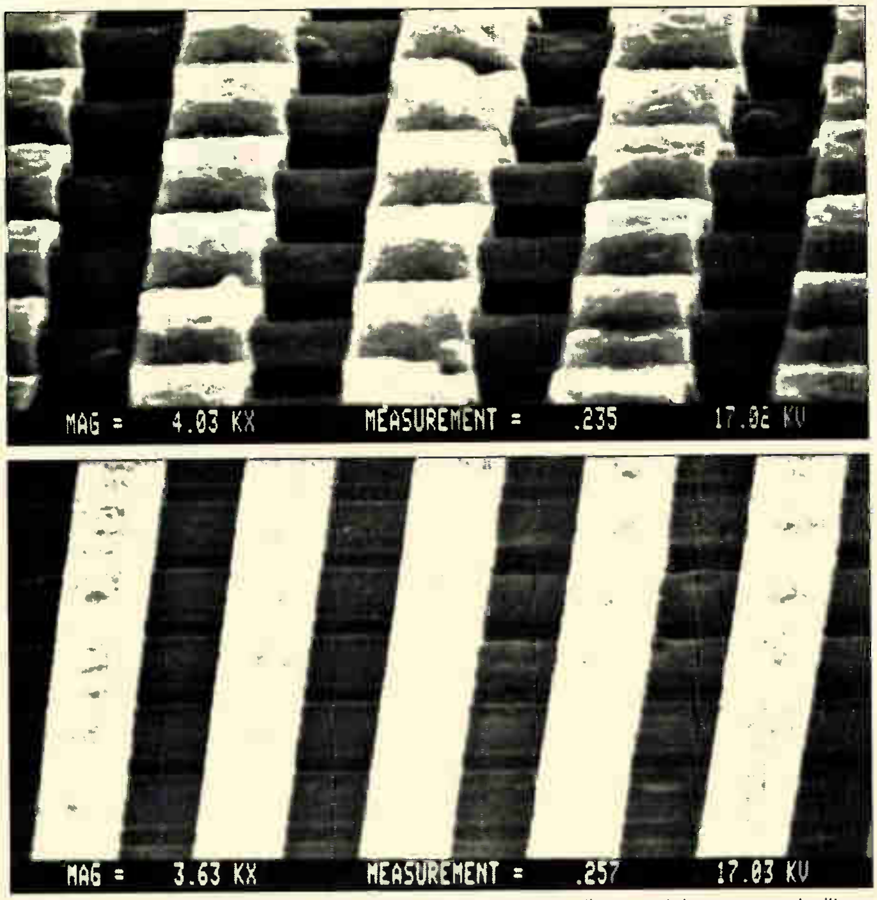
This value is a measure of the health of the bony tissue, and closely relates to the tooth's degree of firmness. To make Periotest easy and practical to use, the value is indicated in relative numbers. These are arranged in a scale from –8 to +50. For example, the range of numbers from –8 to +9 indicates firm teeth; the numbers from 30 to 50 point to teeth that are so loose they can be moved by the lips or the tongue.



TAP TAP TAP. Siemens's Periotest system gives the dentist an early indication of diseases that slowly loosen teeth.

In addition to their visual display, these numbers are also read out by electronically synthesized speech—either in German or English, initially. Thanks to this feature, the dentist can concentrate on the probe and point it to an exact spot on the tooth without having to look toward the display to read the numbers.

The Periotest unit will be introduced publicly in April at the International Dental Exhibition held in Cologne, West Germany. It will be manufactured at Siemens's dental-equipment production facilities in Bensheim, near Frankfurt. *–John Gosch*



FLATTOP. In a conventional IC (top), metal interconnection lines undulate over polysilicon lines (horizontal). Plasma planarization eliminates the troughs (bottom).

figure). The presence of hillocks in a two-level metal chip "seriously increases the incidence of electrical shorts, thus increasing the number of unusable ICs on a wafer," explains Thomas Hill, an engineer in Sandia's IC Interconnection and Deposition Division.

But smoothing out the hillocks was only part of the job, Gregory points out. Sandia researchers also had to develop a plasma planarization technique to get a perfectly flat silicon dioxide layer between the two metals. A third key item of technology for the rad-hard chip was an etching process that could produce either straight or tapered walls for the vias that make connections between the metal layers.

Sandia researchers "integrated a lot of processes" into development of the chip, says Hill. One of the more important techniques is entirely new, and another was adapted from one used by commercial chip makers.

The new process calls for capping a 0.7-μm layer of aluminum with a 0.1-μm strip of tantalum silicide. Use of the cap is what prevents growth of hillocks, which usually swell up on aluminum during thermal cycling.

Another advantage of the tantalum silicide cap, says Hill, is that it tends to absorb ultraviolet light in the range used for photolithography, making that process easier. Aluminum, he points out, reflects UV rays and can cause problems in etching.

Tantalum silicide at the bottom of a via hole also enhances formation of a stable electrical contact between the two metal levels, says Sandia.

The other technique, called plasma planarization, is used in industry for the similar double-metal-layer ICs, says Sandia, and enables formation of a smooth layer of silicon-dioxide dielectric between the two metal layers.

LOW-TEMPERATURE PROCESS. The process starts with plasma-assisted deposition of a 1.5-μm layer of silicon dioxide on top of the IC's aluminum-tantalum silicide interconnection layer. This deposition technique takes place at only about 300°C, compared with the typical 400° to 500°C for chemical vapor deposition. Following the SiO_2, a layer of photoresist 2-μm thick is spun on.

Once the resist is on, Sandia does a double-phase etching. The first, rapid phase takes off the upper resist layer. Then a slow etch removes the remaining resist; in this step, the depth of the etch can be controlled to 100 Å.

The chip has tested well so far, surviving a continuous radiation level of 2×10^5 rads, as well as higher levels of transient radiation. Gregory is optimistic that a 1.5-μm CMOS, double-metalization, 10-Mrad IC can be developed by the end of the year. *–John F. King*

COMMUNICATIONS

FLAK FOR A DIAL-UP WALKIE-TALKIE

WASHINGTON

The Federal Communications Commission is running into some strong interference on its proposed Consumer Radio Service, which would resemble a dial-up walkie-talkie system. The new service would affect present mobile-radio services, which could lose spectrum, and users are out to scuttle the FCC proposal.

The Consumer Radio Service is part of the FCC's drive to make more efficient use of the frequency spectrum. To get it going, the FCC wants to squeeze the necessary spectrum out of the 16 existing channels assigned to the General Mobile Radio Service. The frequencies the FCC has in mind are in two 200-kHz frequency segments within the 460- to 470-MHz band.

The resulting switch in assignments would mean a restructuring of the mobile-radio service, says Raymond Kowalski, chief of the FCC's Special Services Division. Operators of systems that are already working in these channels, however, say the new service could be the first step toward a dismantling of the old.

In an early-February notice—part of the routine procedure the agency goes through before it hands down a ruling—the FCC requested comments on the feasibility of providing two-way voice communication between users a short distance apart—say, within a football stadium—each carrying a personal transceiver. The transceivers would perform a handshake on one frequency and then move to a free frequency to carry the conversation. Such a system could be built with off-the-shelf components, the FCC figures.

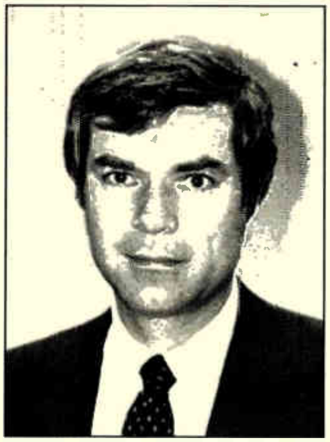
However, the agency would much prefer to cut the channel width for the service from the current 25 kHz. So the FCC is asking for ideas on how much the channels could be trimmed and

APOLLO INTRODUCES A PARALLEL PROCESSOR THAT HAS NO PARALLEL.

John A. Neff told a conference on advanced materials held last Friday in Pittsburgh. Such devices include two-dimensional spatial light modulators, reconfigurable diffraction gratings, and perhaps most important for long-range optical-computing goals, bistable optical devices [*Electronics*, Oct. 28, 1985, p. 16], according to Neff.

Darpa, along with university and industrial contractors, has for the past two years concentrated on three alternative types of nonlinear materials: inorganic insulators, large-molecule organic materials, and superlattices. The agency is even looking at combining these materials to improve nonlinear effects.

"This emerging technology is very materials-limited," explains Neff, program manager for Darpa's Electronics Sciences Division. Until now, devices have been based on lithium niobate crystals and integrated gallium arsenide compounds [*Electronics*, Jan. 13, 1986, p. 20].



RIGHT STUFF NEEDED. Darpa's Neff says optoelectronics industry is "materials limited."

A primary characteristic of nonlinear optical materials is their ability to create charge separations. These separations are the result of photons imparting their energy to those electrons that are loosely coupled to the nuclei, causing them to separate from their atoms. "If the separation of the charges can be maintained momentarily, the resulting electric field leads to a nonlinear response of the material that is related to the degree of separation," explains the Darpa official.

TRAPPED ELECTRONS. For inorganic insulators, the charge separation is primarily the result of free electrons being trapped at other sites in the material. Work on inorganic insulators currently is being carried out at the University of Southern California, Massachusetts Institute of Technology, and Rockwell International Corp. (A project at Hughes Aircraft Co. has been discontinued.)

Neff says the three leading materials in this category are cerium-doped strontium barium niobate, bismuth silicon oxide, and barium titanate. More is understood about these materials and they are in greater use than organic materials and superlattices, he says. But their response times are only in milliseconds.

Many more organic materials exhibit a greater degree of nonlinearity than inorganic insulators, with potential response times in the nanosecond range, Neff says. The major disadvantage of these materials is their relative instability compared with inorganic insulators. For example, oxidation can be a serious problem, he says.

But promising work recently begun at the Air Force Office of Scientific Research in Washington, at the University of Florida, and at the University of California at Los Angeles using porous glasses called sol-gels has yielded an organic material that is both nonlinear and environmentally stable.

Celanese Corp.'s Research Company Division in Summit, N. J., the University of Pennsylvania, and the Naval Ocean Systems Center in San Diego have also received Darpa contracts to study large-molecule organic materials. Celanese has recently initiated its own work on sol-gels.

Superlattices, which make up the third group of materials, are being studied by Honeywell Inc. These are built up using alternating thin-film layers of two semiconductor materials. Different photon-energy levels are required to break electrons free from adjacent layers because of the bandgap discrepancy between the semiconductor materials. Freed electrons are swept rapidly into neighboring layers, which act as potential wells to trap the electrons. Electrons trapped in separated layers create the desired charge separation, and with it, improved nonlinearity and efficiency.

Neff says most superlattices have been fabricated with alternating layers of either aluminum gallium arsenide and GaAs or mercury telluride and cadmium telluride. "A great deal of materials engineering is possible with these structures," Neff notes. By changing the layer thicknesses or potential well depths, for instance, devices with very different operating characteristics can be created. Current stumbling blocks to further research include interface problems between lattices and the expensive equipment needed to grow epitaxial layers.

ORGANIC SUPERLATTICES. The next step in Darpa's nonlinear-optics research may be to combine organic materials with superlattices to enhance nonlinear effects. By growing organic superlattices, the charge separation of the loosely bound electrons of the organic materials—which ordinarily sweep down long molecular chains to achieve charge separation—would be confined to a separate plane by the semiconductor superlattices, Neff explains. First studies on the feasibility of growing organic superlattices will begin this summer, he says.

Darpa's long-term research goal—a bistable device for optical computing—remains elusive, however. Neff says that a practical all-optical switching device won't be possible until order-of-magnitude increases in power levels are achieved. *–George Leopold*

MILITARY ICs

SANDIA OPENS THE WAY TO DENSER RAD-HARD ICs

ALBUQUERQUE, N. M.

More and more, radiation-hardened integrated circuits are becoming mandatory for military gear. And so far only a handful of chip makers have met that requirement for ICs up to the level of 16-K static random-access memories.

Sandia National Laboratories, a major player in rad-hard parts, has laid the groundwork to move another notch upward. The facility, operated for the U. S. Department of Energy by AT&T Technologies Inc., has developed a double-metal-level rad-hard CMOS technology that uses 1.5-μm design rules and proved it out with a 100,000-transistor memory chip.

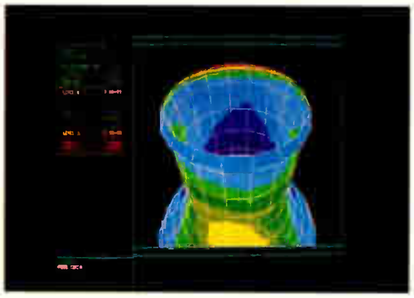
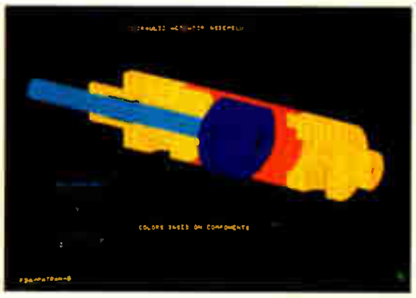
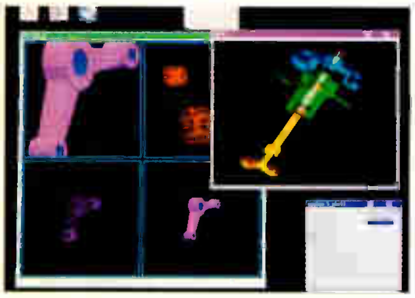
Two metal layers could yield 32-bit rad-hard chips

Now Sandia will exploit the technology in a rad-hard version of National Semiconductor Corp.'s 32-bit NS32000 microprocessor. "We should have first silicon by the first quarter of 1987," says Bob Gregory, Sandia's director of microelectronics.

Crucial to the 32-bit microprocessor's speed is its double-level layout, Gregory insists. Because of its shorter interconnections, the chip is inherently faster than a single-layer IC. Although extensively used in conventional ICs, double-layer metal is rare in rad-hard chips; the processing needed to add the second layer involves temperatures too high for the thin, hard oxides needed to protect chips from excess radiation doses.

Sandia found the way to work with double-level metal mainly by doing away with hillocks, the surface roughness and irregularities that ordinarily form on aluminum interconnection lines during thermal processing (top

OUR 3D GRAPHICS WORKSTATION IS SO FAST IT'S AMAZING THESE PICTURES AREN'T BLURRED.




Until now, if you wanted realtime 3D graphics on a powerful workstation, you had only two choices. Both of them a compromise.

You could purchase a specialized graphics workstation but sacrifice a compatible product family, software and application choice. Or you could opt for a reputable engineering workstation and settle for color graphics that could only be labeled dull.

Introducing Apollo's new DN580. It asks no sacrifice. Instead, this powerful 32-bit graphics workstation overwhelms anything that claims to be either graphic or a workstation.

Its powerful graphics pipeline processor performs 3D graphics at an amazing 100,000-plus vectors per second, a record well beyond the reach of any other computer or workstation supplier.

Yet despite such speed, the DN580 complies with PHIGS and supports UNIX,™ dispelling the myth that performance and standards are contradictory terms.

Of course the DN580 offers more than alacrity. As part of an advanced distributed processing network, its speed is greatly enhanced by an ability to access other Apollo workstations. As well as systems made by DEC® and IBM®

And with Apollo's open architecture, you can perform all these stunts with a single system view.

The Apollo DN580. The only thing faster is the rate at which our competitors will have to work to catch up.

apollo

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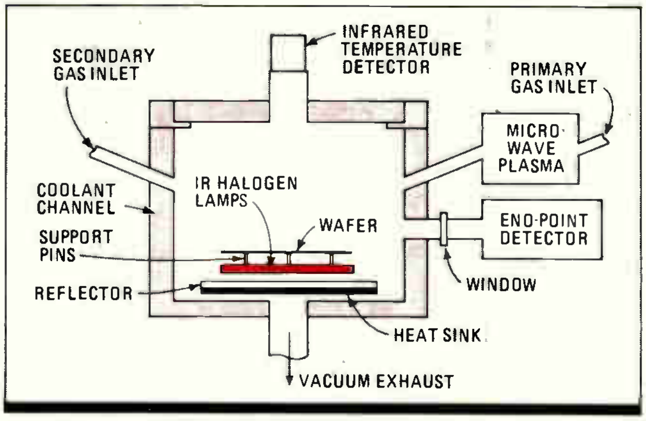
nies argue, it's better to generate the plasma in a location upstream. Then the plasma's less-caustic afterglow, consisting of gases in a less excited state, can do the stripping, etching, or deposition.

Radiation damage in plasma systems has several effects, says Richard Bersin, president and founder of Emergent Technologies Corp., New Haven. Dielectric breakdown caused by electrostatic discharge and sputtering contamination from chamber materials are potential hazards. Threshold shifts on transistors are among the undesired results.



REMOTE. Emergent's NORD afterglow stripper locates plasma generator to one side and heats the wafer quickly with lamps.

The idea has been tried before—Perkin-Elmer Corp.'s OmniEtch system used it in a built-in stripper in the early 1980s, for example. But Perkin-Elmer stopped making the stripper because customers, who wanted to examine the wafers between processing steps, did not want a stripper built into an etcher.

Afterglow processing's new champions say they have licked the problems that kept the technology in the closet until now. "Afterglow technology is what the industry has been asking for for years—a new generation of dry processing," says Ken Linxwiler, vice president of Machine Technology Inc.'s AfterGlo Division in Richardson, Texas. Linxwiler left Texas Instruments to join MTI, when the latter decided to pursue the technology last year. He boldly predicts that "by the end of this decade, plasma will be a thing of the past."

MTI, a maker of spin-gear and small-scale processing equipment, is still a relative newcomer to large-scale wafer processing. It announced a remote plasma stripper, the first product in its AfterGlo series, last October [*Electronics*, Oct. 28, 1985, p. 64]. MTI says it has already shipped 20 of the serial-processing strippers at $100,000 to $120,000 each. The company will unveil the second product in the series, the AfterGlo/CVD chemical-vapor-deposition unit, this week in Zurich, Switzerland, at Semicon/Europa '86, and Linxwiler says an etcher will round out the line by late August. That's despite a market depression that's lasted 18 months, according to Bob McGeary, manager of market researcher Dataquest Inc.'s Semiconductor Equipment and Materials Service in San Jose, Calif.

Critics wonder if MTI and others will be able to succeed in etching, where chip makers' demands for smaller and smaller feature sizes and such difficult-to-etch features as trenched capacitors are a formidable challenge to any technology. Controlling the free-radical gas molecules in an afterglow system, they say, may not be possible. But Linxwiler and Bersin are confident the technology to overcome those problems is already in their grasp, though they won't tell what it is.

MTI expects to ship an anisotropic etching system by August to a customer it will not name. The company has been able to etch GaAs, says CVD project engineering manager Richard Jackson, but has not yet demonstrated aluminum etching.

Linxwiler says remote plasmas are a natural for CVD because it is an inherently cleaner process. Using the same chamber developed for the AfterGlo stripper, MTI claims the self-cleaning AfterGlo/CVD can operate with wafers at only about 250° to 275°C, thereby avoiding the uneven surfaces that are commonplace in conventional CVD systems operating at up to 350°C.

> *Plasma's less-caustic afterglow can do the processing*

Bersin's Emergent Technologies has been developing a line of remote plasma processors it calls NORD (no radiation damage). He pioneered the use of plasma technology in wafer processing in the late 1960s, founded International Plasma Corp., Hayward, Calif., in 1968, and was marketing director for Perkin-Elmer's plasma systems division from 1982 to 1984.

His one-year-old startup shipped its first $110,000 NORD stripper to a Japanese client in January. Emergent does plan to build an etcher, but Bersin says it will be a year before the company can develop its etching technology.

Both companies began with strippers because the demands are simpler than in other process stages. A stripper must be able to burn hardened photoresist off a wafer surface without stripping too far or heating the wafer too much. It must also be fast. Both MTI and Emergent claim throughput in the range of 60 to 100 wafers/h. But their machines use different means to those ends. For example, Emergent heats the wafer in a load-locked chamber with a bank of tungsten halogen heat lamps, while MTI pumps the chamber down for each new wafer and heats the substrate on a steel chuck, or hot plate. (MTI says a load-lock option will be available in April.)

MTI put its microwave plasma-generation tube above the processing area, but Emergent placed its generator to the side to prevent contact between wafer and plasma. Both systems are fully automated, but MTI was able to adapt existing equipment from its Multi-Fab line—including the frame, handling system, and computer controller—to cut costs, while Emergent had to look outside for commercially available robotics and an IBM Corp. Personal Computer/XT to run the machine.

"I think it's going to turn out that there are big advantages to downstream processing," Bersin says. "I think it's going to be faster, cleaner, and I have no question that it's going to be more reliable." *–Tobias Naegele*

OPTOELECTRONICS

WANTED: MATERIALS TO BUILD OPTICAL DEVICES

ARLINGTON, VA.

Much attention is being focused on optoelectronic devices for multiprocessor and optical computing architectures, but relatively little effort has been devoted to the nonlinear optical materials from which these parts would be fabricated. Taking the lead in research into nonlinear optical materials is the Defense Advanced Research Projects Agency, whose optics program is aiming to develop optical interconnections for, among other things, intracomputer communications and large-scale parallel processing.

Optoelectronic materials "must exhibit a large degree of nonlinearity, because only in the presence of such nonlinearity can two optical beams be made to interact with one another," Darpa's

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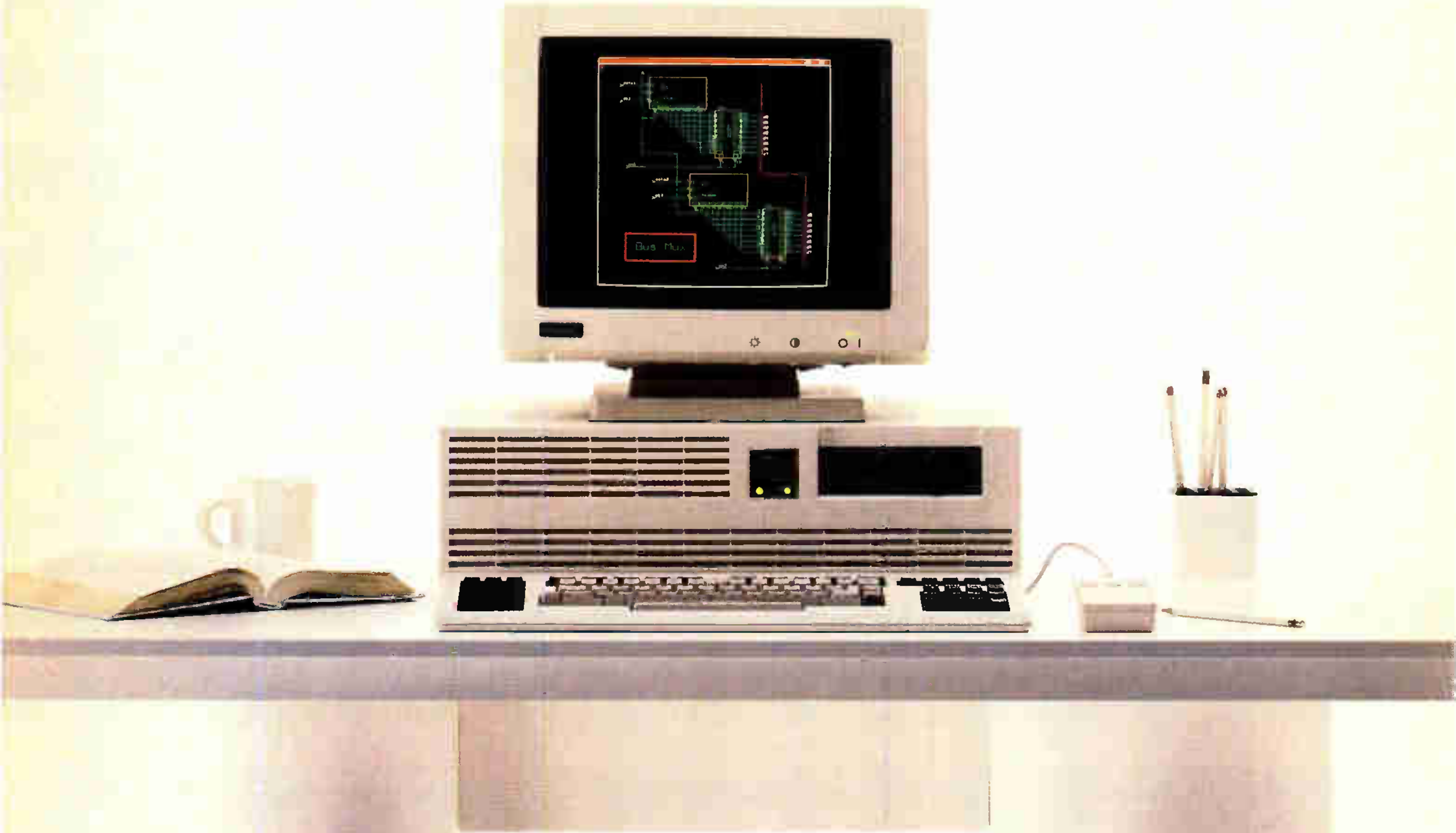

The personal power shortage is over. Introducing the Apollo DOMAIN® Series 3000. A family of personal workstations that are priced like PCs, packaged like PCs, easy to use like PCs. Yet they perform with the authority of machines twice the size and three times the price.

Consider their raw power. Despite the fact that DN3000s fit comfortably on the corner of your desk, they have room inside for a 32-bit, virtual memory engine that includes a Motorola 68020 and 68881 floating point chip. Sufficient force to deliver processing speeds that overwhelm the IBM PC.

Their processing proficiency is equalled only by their graphics. A monochrome DN3000 exhibits 1280 x 1024 resolution on a 19-inch monitor. While a color version, with its four-bit planes, displays 16 colors simultaneously on a high-resolution, 15-inch flicker-free screen.

While such qualities alone are cause enough for celebration, the DN3000s were notably designed with an understanding that technical professionals work as much with each other as they do with their workstations.

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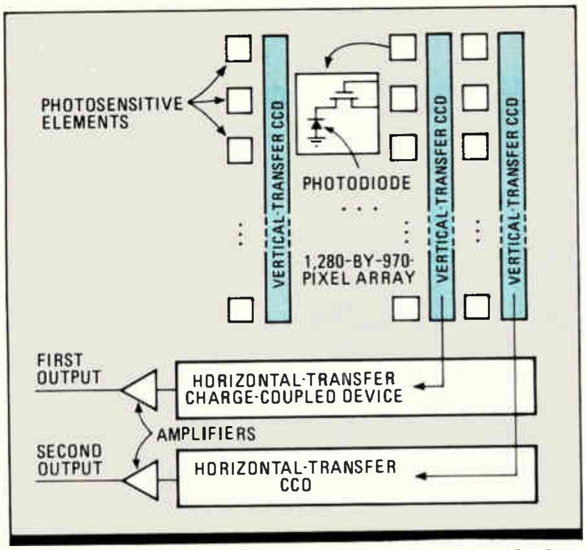


HIGH DEFINITION. NEC's 1,280-by-970-pixel sensor uses two horizontal registers to achieve video rates.

scan lines' worth of signal, some of the lines are preempted for system purposes and no more than 482 are used for video. The NEC sensor's 1,280 elements in the horizontal direction provide balanced resolution with a square pixel.

Although fine-pattern technology is needed to fabricate NEC's sensors, the size of cells cannot be reduced beyond a certain point because light sensitivity would be too low, says Ayaki. That's why the total area covered by the chip's 1.24 million cells is roughly equivalent to that of a 1-in. camera tube, rather than the 0.67- or 0.50-in. equivalent size of charge-coupled-device imagers used in consumer video cameras.

The high-definition imaging chip presses the limits for both the minimum cell size for good sensitivity and the maximum chip size for manufacturability with acceptable yield. At 14.5 by 12.0 mm, the chip's area is slightly less than that of NEC's recently announced V60 32-bit microprocessor, which measures 13.9 by 13.8 mm.

TIGHTER REQUIREMENTS. The photodiodes and the CCD registers in the sensor operate in an analog mode, making uniformity requirements much more stringent than those of digital circuits. The output is sampled at a 48.2-MHz rate, 4.3 to 7 times that for the chips used in consumer cameras and many times faster than the cycle times of large DRAMs.

Furthermore, Tanigawa points out, the sensor is harder to make than a processor even if the sensor is somewhat smaller, because a relatively high percentage of the chip area is devoted to active circuits. Most of the interconnection in the imager consists of functional CCD registers, whereas in a processor, significant area is taken up by metal interconnections that have only a small impact on yield.

Because it was not possible to implement a horizontal register operating at 48.2 MHz, twin horizontal registers operating at 24.1 MHz are connected to alternate vertical registers instead. A transfer efficiency of 99.995% per stage has been achieved. Use of two horizontal registers, however, makes it imperative that these two registers be identical. Any difference would show up as a fixed pattern on alternate vertical dots.

Aside from halving the required operating speed, use of the twin-register configuration provides twice the available width for each register stage, which makes it possible to fabricate the chips with 1.5-μm design rules. A single horizontal register would have called for submicron rules, Tanigawa says.

In typical operation with scene illumination of 2,000 lux and an *f*8 lens, the sensor's signal-to-noise ratio is 48 dB. The chip's output current under these conditions is 14% of that at the saturation level. The saturation level is set by the vertical CCD register's charge-handling capability—about 68,000 electrons. The total root-mean-square noise charge under dark conditions and a bandwidth of 20 MHz is 36 electrons. Thus the dynamic range—the ratio of saturation signal charge to noise—is 65 dB.

Color capability can be added in the same manner as for existing consumer-oriented devices: by the use of color filters. Color would be used in cinematography and videotex as well as for color TV. NEC sees cinematography as an attractive new application for high-definition TV equipment because editing and addition of special effects are fast and inexpensive. *–Charles L. Cohen*

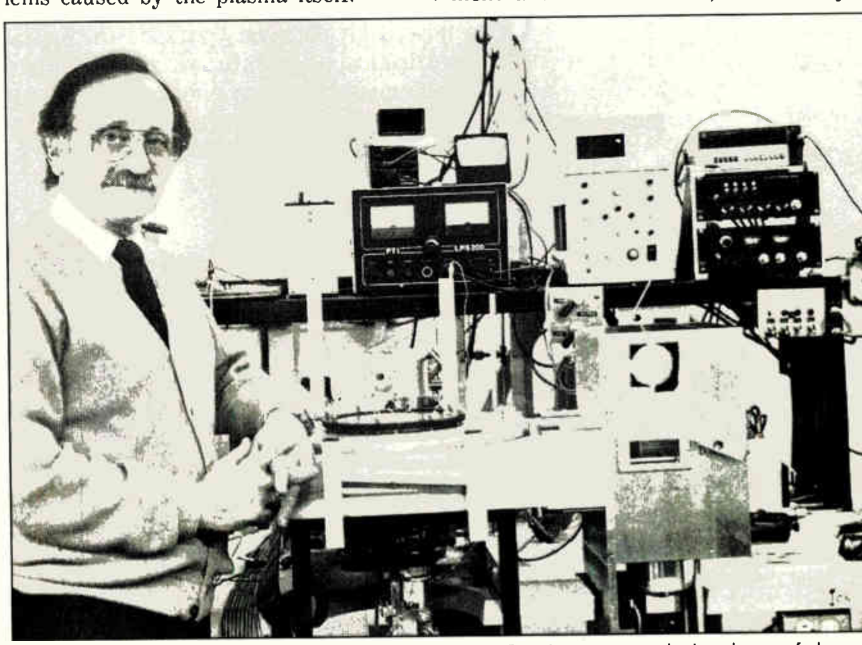
IC PROCESSING

TAMING PLASMA SOURCES TO CUT WAFER DAMAGE

NEW HAVEN, CONN.

Semiconductor makers have known for years that wet chemical processing is not an ideal way to produce wafers. But later-generation dry processing systems, which use gas plasmas to process wafers faster and more precisely than chemical baths, have struggled with radiation damage and other problems caused by the plasma itself.

Now a couple of trailblazing companies are gearing up development of a new generation of dry, plasma-based wafer processing systems—strippers, chemical-vapor-deposition systems, and even etchers—using remote plasma processing. Rather than create the volatile plasma in the process chamber and subject the delicate wafer to ion bombardment and other hazards, these compa-



PIONEER. Emergent Technologies president Richard Bersin was an early developer of plasma technology, and now his startup is a leader in remote-plasma IC-processing systems.


UNIX

bile that has a variety of options, this approach will make for easy and flexible configuration of the numbers and combinations of electronic modules, he adds.

The CAN also comes with powerful error-detection mechanisms and automatic error handling and confinement features, Kiencke points out.

Intel will build the CAN peripheral chips in the same 1.5-μm CMOS single-metal double-polysilicon process used for its general-purpose automotive microcontrollers. The next step will be to integrate CAN functions on chip with Intel's automotive microcontrollers.

CAN could start showing up in production-built cars by model year 1990, says Intel's Brannon. "We have an 18-month to two-year lead over everyone else." *–Wesley R. Iversen*

PORTABLE COMPUTERS

SURPRISE! ZENITH WINS GIANT IRS LAPTOP AWARD

GLENVIEW, ILL.

Personal computer industry watchers got a jolt last week when the Internal Revenue Service awarded a contract for up to 15,000 portable machines for use by IRS field auditors. The surprise was not the contract itself, which had been expected since last fall, but rather that Zenith Data Systems got the business instead of IBM Corp.

TAX MACHINE. IRS agents will hit the road with 15,000 Zenith Z-171 portable computers.

Industry analysts and trade publications had been confidently predicting the award would go to IBM in mid-January, and that the computer giant would use the occasion to introduce a lightweight portable or laptop Personal Computer. "Everybody I've talked to says their sources were IBM sales people who were saying that they'd won it. But we never thought they had," says a Zenith official who asked not to be named. One tipoff that Zenith was strongly in the running was that some IRS offices started buying its IBM PC-compatible portable, known as the Z-171, last December.

RIPPLE EFFECT. The IRS award "will have a significant ripple effect into the commercial market," according to John Frank, marketing vice president at the Zenith Electronics Corp. subsidiary. "All of the publicity surrounding the IRS request for proposals [last fall] drew a lot of attention from potential portable [computer] users. This will give us lots of credibility in developing other customers."

Under terms of the pact, valued at an estimated $27 million, the IRS is expected over the next 18 months to buy 15,000 Z-171 machines equipped with 512-K bytes of random-access memory, modems, video cards (for use with an external monitor), and Enable, an integrated business software package supplied by The Software Group, Ballston Lake, N.Y. The 14.3-lb Zenith machine relies on a back-lit liquid-crystal display and comes with two 5¼-in. floppy-disk drives. Zenith will also provide software, technical support, and maintenance for the systems through 1995.

Frank says three major factors, in descending order, played into the Zenith win: price, technical capabilities, and vendor support. "We came out of the bottom of the funnel when they combined those three factors," Frank says. ZDS was up against bidders that included AT&T Information Systems, Data General, Falcon Systems, Federal Data, Grid Systems, JWK International, PCA Microsystems, Replitech, Sperry, and Texas Instruments.

George Colony, president of Forrester Research Inc., a Cambridge, Mass., market research company, believes Zenith's pricing was probably the most important factor in the win. The $27 million ZDS award compares with $34 million to $36 million reportedly bid by IBM. Colony notes that Zenith's strong record as a major supplier of desktop machines to the Air Force, Navy, and other government agencies [*ElectronicsWeek*, April 29, 1985, p. 44] probably helped, too. "The fact that IBM didn't have a commercial product available also hurt [IBM's] chances," Colony adds.

For personal computer vendors, the IRS choice will prolong the agony of guessing when and if IBM will enter the laptop market. "A lot of vendors are hanging back to see what IBM does," notes Zenith's Frank. If Big Blue does jump into the business, many observers expect its system to use 3½-in. floppy-disk drives, so lack of an IBM entry now could further delay widespread introduction of 3½-in. floppy media.

At the IRS, the focus may shift to the desktop arena: the agency expects to issue a request for proposals for up to 11,000 desktop computers this summer. But all eyes remain on IBM. Forrester Research's Colony, for one, says the IBM laptop is imminent. "IBM will be announcing at the end of March," he says. *–W. R. I.*

TELEVISION

NEC BUILDS IMAGER FOR HDTV; IT WASN'T EASY

KAWASAKI, JAPAN

Image sensors for next-generation high-definition TV would appear to present a fabrication challenge similar to that of 1-Mb dynamic random-access memory chips: the imagers need somewhat more than 1 million cells. But the TV sensor is much harder, which is shown by the difficulties NEC Corp. faced before it succeeded in building its 1,280-by-970-pixel imager. Kazuo Ayaki, general manager of the company's Microelectronics Research Laboratories in Kawasaki, expects it will take NEC another 2½ years to develop a commercial version, while many manufacturers will be shipping 1-Mb DRAMs this year.

Texas Instruments Inc. of Dallas has already made a sensor of comparable size—1,024 by 1,024 pixels—for a special application. But the TI part is limited to a scanning speed well below that needed for the 60-Hz field operation of TV.

The NEC chip was developed with twice the number of scanning lines used in NTSC broadcasting. Thus it offers performance on the order of that considered necessary for high-definition TV experiments, according to Hiroshi Tanigawa, manager of the Sensor Research Laboratory at the Kawasaki labs.

The 970 scanning lines that make up the NEC sensor's vertical dimension might seem insufficient, but that number is slightly more than what's needed. Although the NTSC system provides 525 first to cut inventory and personnel before the downturn accelerated in 1984.

So far, the 1986 improvement is largely "inventory-driven, rebounding from levels that were far too low," Clough says. In retrospect, what he estimates as a 31% drop in 1985 for U. S. IC sales, "wasn't a recession and wasn't a depression—it was a holocaust."

The only ingredient missing for even the most doubtful observers is what all hands admit is vital—orders given directly to chip producers by major customers, who must fuel any lasting recovery. "We don't yet see a major strength in the major accounts, especially the computer segment and in particular the mainframe business," says Bruno Pagliuca, vice president and semiconductor head at Texas Instruments Inc.

The TI executive nevertheless acknowledges the upswing in distribution, along with a pickup in smaller account activity. He believes much of this ordering comes from another key development that other sources identify also: Overstocked inventories that have overhung the business since 1984 are finally running out. Pagliuca singles this out as a good sign of "our market coming back to normal growth."

Other major semiconductor houses, including Advanced Micro Devices Inc. and National Semiconductor Corp., agree with Pagliuca, particularly on the pickup from distributors. National says, however, that its orders from original-equipment manufacturers are getting better and that sales for the year should be up 10% to 15%. *–Larry Waller*

AUTOMOTIVE

INTEL AND BOSCH TEAM FOR REAL-TIME CAR NET

DETROIT

Intent on getting into high gear before their competition, Intel Corp. and Robert Bosch GmbH have developed a serial network to link computers and other modules on automobile power trains. It is fast enough for real-time control, the two say, so the network will add to a car's performance and reliability.

The companies intend to promote their network scheme as an automotive-industry standard. But other players in the market are skeptical about that ambition. They also question the need for networking at so high a level.

Intel and Bosch signed their joint-development deal late last year, and released details last week in Detroit at the 1986 International Congress and Exposition sponsored by the Society of Automotive Engineers. The West German automotive-equipment supplier will provide the network-communications protocol; the Santa Clara, Calif., semiconductor maker will develop the chips to implement it. Intel expects to have first working versions of the CAN (controller area network) chip by late 1987.

IN THE CAN. The two companies say linking multiple computers into a real-time distributed control network will lead to improved vehicle performance and reliability. For example, a command to the engine controller from the transmission controller could reduce engine torque during shifting, explains Ewe Kiencke, CAN project manager for Bosch in Stuttgart. That would make gears shift more smoothly and reduce clutch wear.

"By the 1990s, the sophistication [of automotive electronics] will be such that it will have to be tied together," argues Robert Brannon, general manager of Intel's automotive operation in Chandler, Ariz. He points out that the electronics content in a U.S. car is expected to more than double from today's $550 to $1,383 by 1995 (see graph).

The stand-alone network chip will work as a peripheral with any vendor's microcontroller—including those built by leading automotive electronics vendor Motorola Inc. But Intel and Bosch could find themselves on a rocky road as they seek to establish CAN as a standard.

"We have purposely shied away from trying to establish a standard, because our belief is that automakers will establish their own," says James D. Edson, market development manager for Motorola's automotive strategic marketing operation in Phoenix, Ariz. In fact, Chrysler Corp. and Ford Motor Co. unveiled details of their own networking and multiplexing schemes at the show.

CAN will go beyond Ford's, Chrysler's, and Motorola's prototype system displayed at its show booth. CAN will run at up to 1 Mb/s to link such modules as the engine controller, automatic transmission, and antiskid controllers.

LOWER-SPEED NETS. Other networks address lower-speed applications. The Ford and Chrysler networks, for example, belong to a category that an SAE subcommittee on vehicle network requirements has labeled data communications multiplexing. Nets in that category would link intelligent modules such as engine controllers and body computers to the instrument cluster, providing parametric data at less than real-time speeds, explains Fred Miesterfeld, a Chrysler engineering supervisor and chairman of the SAE subcommittee.

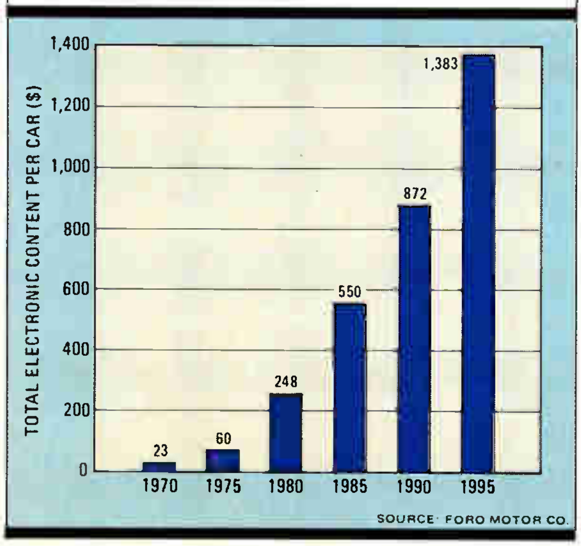
The data communications multiplexing category falls between the high-end network type that Bosch and Intel are proposing and another SAE-defined network type intended for multiplexed control of items such as headlamps, tail lamps, horns, and windshield wipers. Miesterfeld notes there are clear reasons to develop the two lower-level network types—they could lead to easier diagnostics and unravel the rat's nest of wires in today's nonmultiplexed systems. But for the high-end CAN type, he contends, the reasons are less urgent.

Both Miesterfeld and Motorola's Edson also say CAN would likely require costly coaxial cable or optical fiber. But Bosch's Kiencke says two years of testing have shown that a pair of untwisted telephone wires can handle speeds up to 1 Mb/s, as long as they are shielded against noise.

The CAN protocol will relieve the microcontroller of message-transfer administration, Bosch says, by using "communication objects," each consisting of a data message up to 8 bytes long, a unique identifier for the message, and a control segment for message transfer. CAN will transmit and receive the objects through a dual-port random-access memory, with address locations assigned through software by car designers.

The transmitting node will broadcast to all stations; CAN hardware in every station will contain a message-acceptance filter. "For the microprocessor, the whole interface looks like a RAM," says Kiencke. For an automo-

ELECTRONICS IN U.S. CARS TO GROW RAPIDLY



SOURCE: FORD MOTOR CO.

Electronics

U.S. SEMICONDUCTOR MARKET LOOKING BETTER ALL THE TIME

FORECASTS ARE GOING UP; NEXT YEAR COULD BE A BOOMER

LOS ANGELES

The outlook for the U.S. semiconductor industry continues to brighten. Not only are some experts hiking their sales forecasts, but a growing number of them are expecting a real boom next year.

As usual, the distributors are leading the way. It was their report of improving sales in December that some industry observers took to be a solid early indicator of an upturn in orders [*Electronics*, Dec. 16, 1985, p. 22]. Skeptics, however, maintained at the time that such signals often amount only to "pipeline filling" that sometimes fades.

The California-based distributors are seeing most of the new action. "If anything, I'm more positive," says Charles M. Clough, president of Wyle Laboratories Inc., El Segundo. First to proclaim an improvement last year, he says sales are continuing their upward swing. He reports his semiconductor sales in January amounted to $22 million, up from $16 million in December.

Wyle isn't the only one to report a good January. "January was an excellent month, the best in 15 months," says Howard B. Franklin, Bell Industries Inc.'s senior vice president in charge of distributor operations. He adds that higher sales are spreading steadily eastward to the Los Angeles company's Midwest locations.

Giant Hamilton/Avnet Electronics Inc., in Culver City, Calif., is having a similar experience. Bookings have been rising for four months, a spokesman says. Even in depressed 1985, the nation's distribution leader reported substantially more than $1 billion in sales.

Jack Beedle, ordinarily one of the industry's most pessimistic market consultants—and the most accurate in calling the downturn—is still bearish about this year's shipments. He holds to his earlier view that 1986 started from such a depressed level that it amounts to a lost cause. He expects sales to be off 3.7% from 1985.

CONFIRMATION. Clough says the upward trend strengthens.

But Beedle is getting positively excited about next year. The president and founder of In-Stat Inc., Scottsdale, Ariz., sees a take-off coming in chip sales, building through the year. "I'm becoming very positive," he adds. Beedle predicts a very strong 1987—no less than a 31% rise in U.S. IC revenues.

Wyle's Clough agrees that the real growth will come next year. He says it will be fueled primarily by new generations of desktop reduced-instruction-set computers. A robotics boom will help, too. But he is far more optimistic about this year's sales than is Beedle. Clough believes that U.S. industry will show a 13% to 15% growth; distributors, he says, will beat that increase by 3%, and Western distributors will add 3% more. As to the worrisome shortage of orders from mainframe computer manufacturers, Clough is sticking his neck out with another prediction he made earlier: "They'll be back by May or June."

Some observers continue to doubt the staying power of this distribution upswing. "Distributors are doing much of the ordering today to prepare themselves for an eventual recovery . . . but this could lead to a false impression of the real demand in the industry," warns financial analyst Andrew J. Kessler of Paine Webber Inc., New York. He cites a similar occurrence in 1982, when sales rose and fell months before the 1983-1984 boom. For 1986, he forecasts only "modest 1% to 3% growth.

Profits are still eluding chip makers, says Kessler. He estimates that the break-even point for U.S. industry sales is $650 million a month, based on a three-month average. Sales reached only about $610 million in January, he estimates, which means that the return to profitability probably will not take place until midyear.

Clough of Wyle has heard all the caveats against his upturn call, and rejects them. "The historical record shows distributors leading the industry by six to eight months, and we're on schedule," he declares. He has a reputation as an indefatigable optimist but points out that Wyle was one of the

NICHE IC MAKERS NEGOTIATE SLUMP UNSCATHED

A marked difference between the 1984-86 semiconductor recession and earlier hard times, when all participants suffered, is how well niche companies have fared. These companies, largely startups or existing businesses that have narrowed their focus to specialty products, in many cases have sailed through the troubles without losses. Financial analysts have touted them as a new wave that will prosper through strength in a few areas, such as application-specific chips, arrays, and power semiconductors.

Among those getting a fast start in the improving business climate for chips are LSI Logic, Siliconix, and Silicon Systems. Officials at such companies see far rosier prospects than their counterparts at battered major houses. At Silicon Systems Inc., for example, chief executive officer Carmelo J. Santoro notes proudly that the Tustin, Calif., company had only a single quarter with a loss in 1985, "and bookings are taking off."

But even so, fortunes of such smaller highfliers still are linked with the majors, if only by their participation in the same general market. The mounting losses of the majors hang over everyone, Santoro says.

"I don't know how long they can keep losing that kind of money. I feel good about the market, but I'd feel better if AMD's Jerry Sanders, Intel's Andrew Grove, and National Semiconductor's Charles Sporck were more positive." *–L. W.*

PRODUCTS NEWSLETTER

VLSI TECHNOLOGY TO INTRODUCE ITS FIRST STANDARD PRODUCT

Look for VLSI Technology Inc. to push into standard products with a general-purpose 16-bit microprocessor licensed from Western Design Center Inc., Mesa, Ariz. The San Jose, Calif., company, which built its early success in semicustom ICs, wants to capture a piece of the much bigger market in standard parts. So it is introducing the 65C816, a CMOS part that has a 16-bit internal architecture and an 8-bit external data bus. It is fully compatible with software running on the 6502, the 8-bit microprocessor used in the Apple II line. Western Design Center now owns the rights to the 6502. VTI's new Application-Specific Logic Products Division, Phoenix, Ariz., plans to offer samples of the 40-pin part by summer at less than $10 in volume. ☐

ADAPTEC ADDS CONTROLLER FOR ENHANCED SMALL DISK INTERFACE

Adaptec Inc. has designed its disk-controller chip set into Small Computer System Interface boards that support the 10-Mb/s Enhanced Small Disk Interface specification, which is gaining popularity as a 5¼-in. Winchester disk drive standard. The Milpitas, Calif., company's ACB-4520 ESDI controller sells for $327 in 100-piece lots. Adaptec also has single-ended and differential line-driver SCSI cards for the 15-Mb/s extended Storage Module Drive controllers; these sell for $895 and $920 each. All will be available this month. ☐

NEC CHOOSES 1.2-MICRON CMOS FOR ITS 1-Mb 150-NS EPROM

Although NEC Corp. is not the first to introduce a 1-Mb EPROM, its new part is the fastest version built in CMOS. The Tokyo company uses its 1.2-μm CMOS process to get an access time of 150 ns. The NEC chip follows Advanced Micro Devices Inc.'s 170-ns CMOS EPROM and Intel Corp.'s 200- and 150-ns n-MOS chips. Samples are selling for $55 in Japan. The 64-K-by-16-bit memory can be programmed in 30 seconds, compared with 15 seconds for the Intel parts and 49 for the AMD EPROM. NEC will also offer 200- and 250-ns versions. ☐

CMOS BUS-INTERFACE CHIPS RUN AT BIPOLAR SPEEDS

Integrated Device Technology Inc. squeezes bipolar speeds out of CMOS with its 39C800 series of bus-interface logic chips. The chips are pin-compatible with Advanced Micro Devices' 29800 bipolar series, but at 5 μW dissipate one twentieth the power. Propagation delays are from 4 to 8 ns. Made with the company's 1.2-μm CMOS technology, the series handles both TTL and CMOS input signals. Samples are available now of three 9-bit noninverting parts—the 39C823 register, the 39C843 latch, and the 39C863 transceiver. By May, the Santa Clara, Calif., company will offer samples of 8- and 10-bit registers and latches, a 10-bit transceiver, and 10-bit buffers. Prices start at $5.90 each in lots of 100 pieces. ☐

MATERIALS RESEARCH UNVEILS PRODUCTION-LINE PLASMA ETCHER

Materials Research Corp. is unveiling a production-oriented etching system based on the same technology used in its MIE 710 and 720 research and development machines. The fully automated Advanced Reactive Ion Etching System (Aries) uses magnetron-enhanced plasma for good anisotropy with minimal undercut at very low pressure. A single-wafer, cassette-to-cassette system capable of processing up to 70 six-inch wafers per hour, it affords more precise etch control and greater wafer yield than other process technologies, the Orangeburg, N. Y., company says. Aries will debut at Semicon/Europa in Zurich this week. It sells for $395,000. ☐

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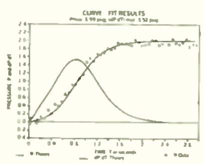

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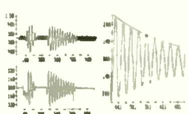

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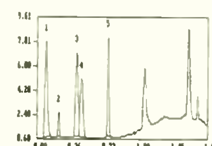

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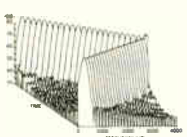

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ELECTRONICS NEWSLETTER

SEQUENT SIGNS $50 MILLION DEAL WITH SIEMENS...

Parallel processing will make its first breakthrough into commercial applications with a $50 million, multiyear original-equipment-manufacturing agreement signed this week between Sequent Computer Systems Inc., Portland, Ore., and Siemens AG. The Munich electrical and electronics giant will market Sequent's multiprocessor Balance 8000 system in Europe and later manufacture Balance-based products under a technology exchange. Siemens already makes personal computers and work stations that use the National Semiconductor Corp. 32032 microprocessor and support AT&T Co.'s Unix operating system, but had no multiprocessor system of its own. Sequent chief operating officer Scott Gibson says a key selling point for Siemens was the system's ability to expand without software changes. He calls the agreement the largest such OEM deal ever for parallel-processing computers. □

...AND HAS TWO MORE OEM PACTS IN SIGHT

Continuing its roll in original-equipment-manufacturing arrangements, three-year-old Sequent, which reported 1985 sales of only $5 million, will disclose two more large commercial OEM agreements for the Balance system within the next 60 days, Gibson says. The company has already closed OEM agreements for technical parallel computers with Teradyne Inc. of Boston and Shiva Multisystems Corp. of Menlo Park, Calif. The Balance systems use 2 to 30 National 32032 chips and runs Sequent's multiprocessing operating system, Dynix, based on AT&T Co.'s Unix System V, including the 4.2bsd enhancements originated at the University of California, Berkeley. □

EUROPE'S ESPRIT BRANCHES INTO SOFTWARE RESEARCH, WHILE 'RACE' IS ON

The European Communities plan to diversify their pan-European research program in data-processing by promoting software development and engineering. EC officials say 11 new projects they launched in late February will correct a basic weakness of the European Strategic Program for Research in Information Technologies (Esprit): an overconcentration on components research and equipment development. The 11 projects will be funded by some $38 million in EC grants and matching funds, bringing the monies committed to Esprit research to $650 million.

Meanwhile, the first phase of the separate Research in Advanced Communications for Europe (Race) program to develop a wide broadband network got under way last week. Some $38 million—half of it contributed by the EC—was awarded for 31 projects. All told, 109 companies will take part, including virtually every major European producer of telecommunications equipment. □

NATIONAL SEMICONDUCTOR WON'T TAKE DISTRIBUTORS' BIPOLAR ORDERS

A surge in distributor orders for 5-V bipolar logic devices has led National Semiconductor Corp. to put a moratorium on bookings for the parts, saying that most are remaining on distributors' shelves. Incoming orders for 5-V bipolar devices have doubled since mid-December, says a National representative. With 5-V bipolar logic devices found in nearly all system designs, distributors evidently were expecting a business rebound that has not yet been met by customer demand, he says, adding that "we're not in the position to whipsaw the factory up and down based on that ordering scenario." Distributors have accumulated a nine-months' supply of the products; National considers a 90-day supply sufficient. The Santa Clara, Calif., company expects to end its moratorium, which started Feb. 1, within three to four weeks. Other chip suppliers, including Intel, Motorola, and Signetics, are also keeping a close eye on heavy orders from distributors, sources report. □

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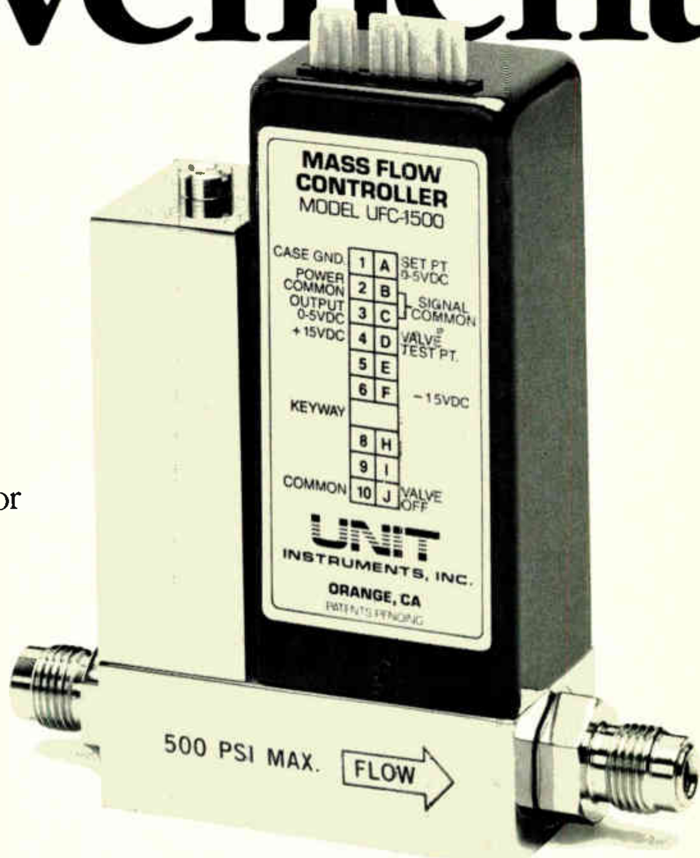

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TECHNOLOGY NEWSLETTER

VLSI CHIPS PROCESS SIGHT AND SOUND MUCH AS THE BRAIN DOES

Chips that process sight and sound information much as the human brain does have been built. These very large-scale integrated circuits, which contain 100,000 analog transistors, have emerged from a long-running study at the California Institute of Technology, Pasadena, that is investigating alternative methods of computing. The chips, representing a new approach to understanding the systems architecture of the brain, replicate the human retina and the cochlea. The retina chip, which uses photodetectors for sensors, already has demonstrated that it can detect motion in a laboratory experiment. The project has been under way for nearly five years and is directed by Caltech computer science professor Carver Mead, who with Lynn Conway pioneered structured VLSI circuit design. □

ENHANCED CZOCHRALSKI PROCESS PROMISES HIGHER MOS YIELDS

Sony Corp. has developed ingots with high oxygen content for improved yield in MOS memory and bipolar analog chips. The Tokyo company uses a variation of the magnetic-field Czochralski process it developed six years ago to grow more-uniform ingots with low oxygen content [*Electronics*, July 3, 1980, p. 83]. Sony says it achieves oxygen content higher than is possible with the conventional Czochralski process by rotating the crucible while a magnetic field holds the melt stationary. During wafer processing, oxygen near the surface is driven off to provide a low-oxygen striation-free region for device fabrication, while oxygen in the interior provides intrinsic gettering to remove process contaminants. Sony has licensed the basic process to wafer manufacturers in Japan and the U. S.; the company itself uses the process for charge-coupled-device image sensors and thyristors. □

CHIP-ON-REEL FORMAT GETS BACKING FROM THREE MAJORS

An informal agreement among three major U. S. chip makers could get the tape-and-reel shipping medium rolling in integrated-circuit markets. The nested vinyl tape and reels that can hold thousands of ICs are a proposed replacement for conventional shipping tubes, or rails, which carry only 50 to 100 chips. National Semiconductor, Signetics, and Texas Instruments have recently settled on several formats, including the number of surface-mountable ICs per reel, and a labeling scheme combining bar codes with alphanumeric characters. The parts count per reel ranges from 2,500 for small-outline packages with 8, 14, and 16 leads, to 100 for large plastic chip carriers with 100 and 124 leads. □

INTEL TO HIT THE ROAD IN NISSAN AUTOS

Autos built by Nissan Motor Co. in the 1990s will have a comprehensive electronic engine-management system built around a new 16-bit microcontroller from Intel Corp. After a five-year joint development effort, the Santa Clara, Calif., chip maker and the Tokyo auto company unveiled details of the MCS-96 circuit last week at the Society of Automotive Engineers' International Congress (see related story, p. 15). "It's not a custom part, but we listened to what Nissan's requirements were and designed the chip with them in mind," says an Intel official. Intel will offer versions of the 16-bit design for use by other automakers. The MCS-96 features 12.5-μs average instruction times and high-speed, precision input/output functions. In the Nissan system, it will be paired with an 8-bit Nissan microprocessor in a module that will control a range of functions, including fuel injection, ignition timing, a twin variable-nozzle turbocharger, valve timing, and a four-speed automatic transmission with lockup clutch. □

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IMS1423 4K x 4	25,35,45	660	33 CMOS	CMOS
IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

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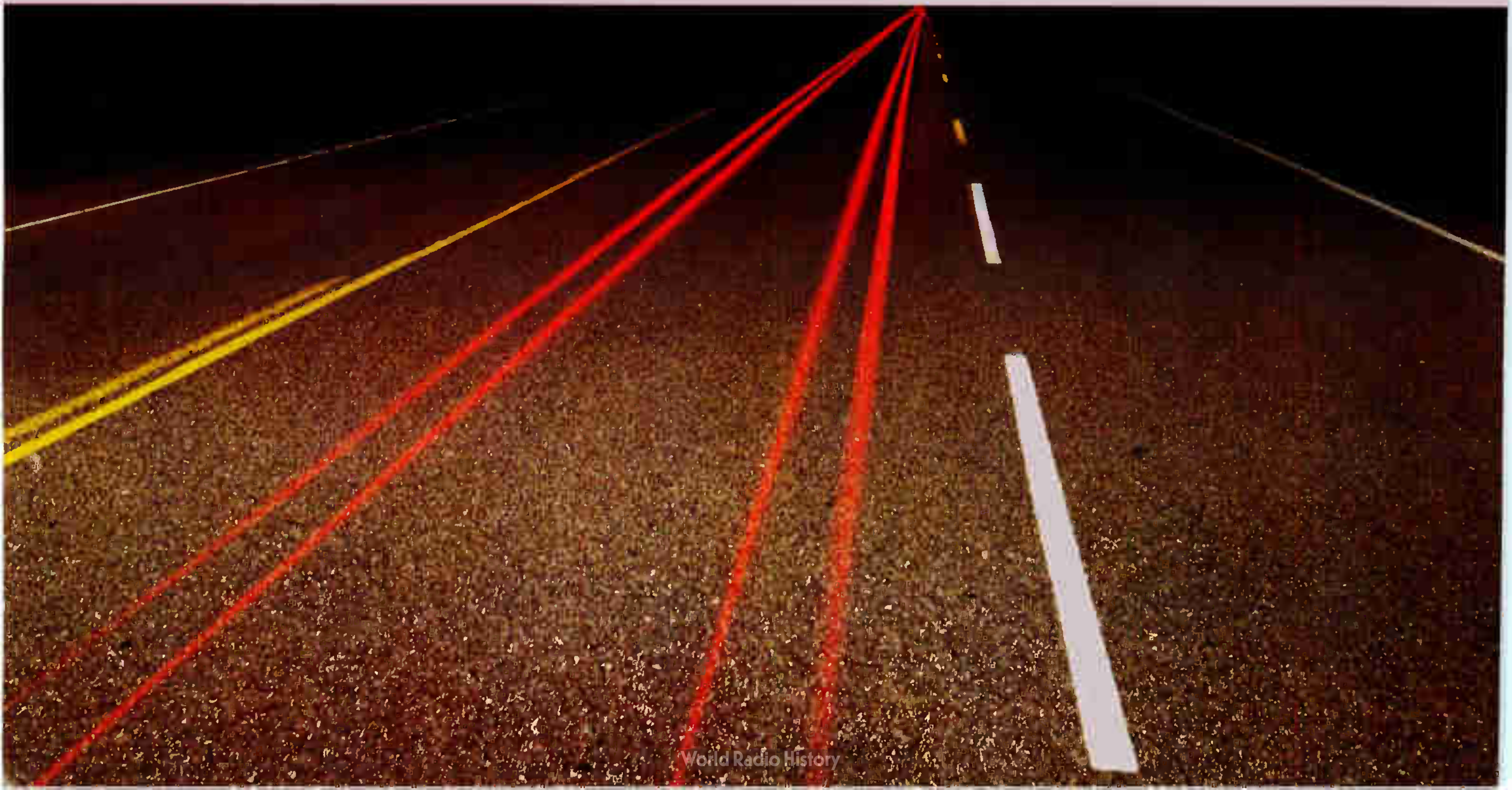


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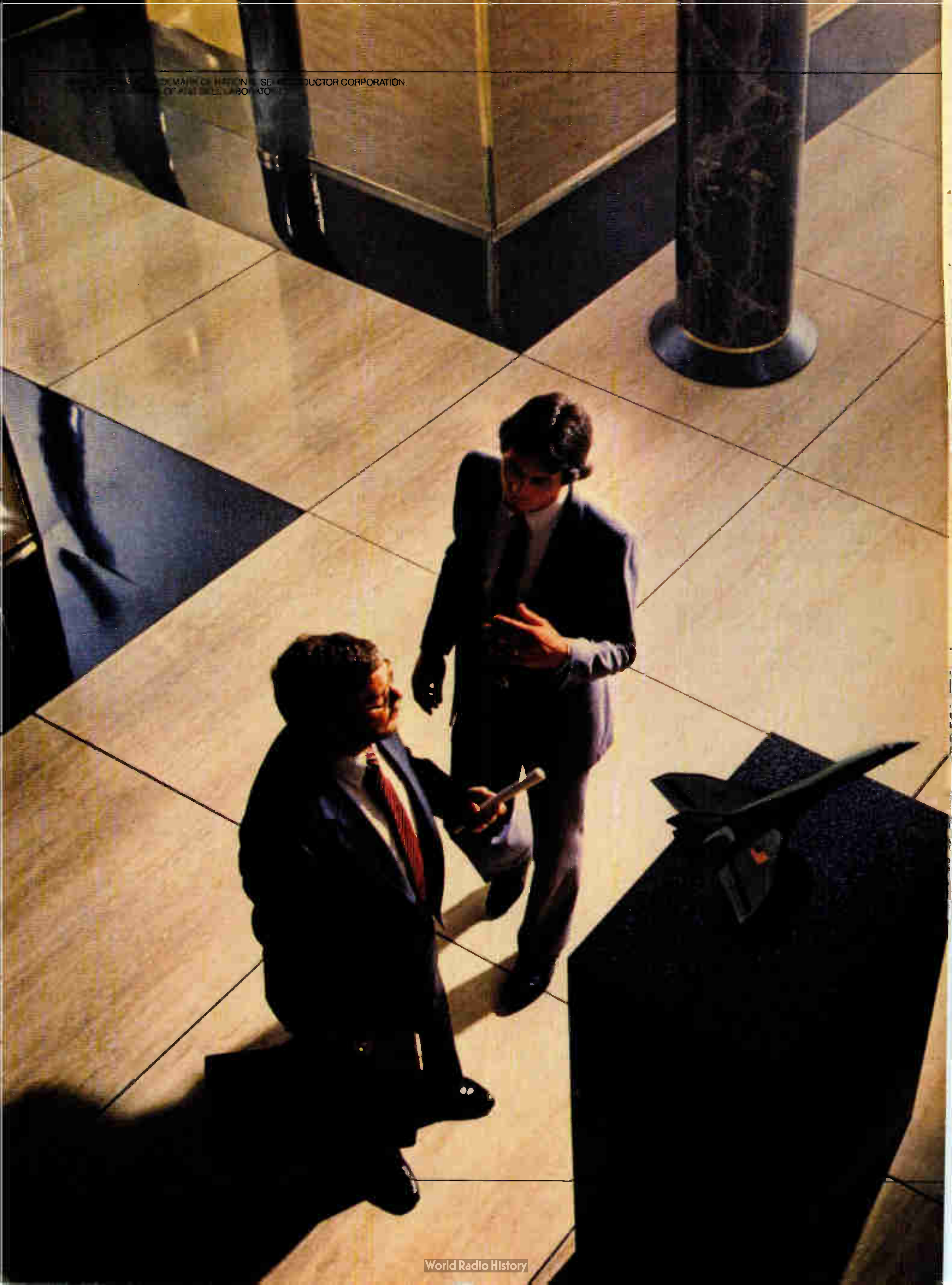

Electronics

When Tom Manuel visited Hewlett-Packard Co. for his Technology to Watch on HP's new Spectrum computer architecture (p. 39), he found something even more impressive than the program's sheer size and scope. It was "the thoroughness of, and strict adherence to, engineering principles that appeared to provide the lifeblood of the project." When Tom is impressed, we at *Electronics* listen.

The reason is his experience. Tom, who has a BS in physics from the University of Alberta in his native Canada and studied for an MBA at Stanford, spent 10 years at Tymshare Inc. in jobs ranging from quality and reliability assurance to pilot applications.

Then, for the three years before he joined us in 1980, he was president of a company he had founded to do market research, product marketing, and program-management consulting in consumer computer products and microcomputer systems. That's perfect training for his responsibility on the magazine, which is to direct our information-technology coverage.

Tom considers himself fortunate to be doing something he truly enjoys. "It is one of the great pleasures of my job to sit down with the executives and designers, like those at HP. It is actually fun to learn some of the details of a technical achievement like the HP Precision Architecture, get a small peak at how it was done, and then present that clearly to our readers."

Take the Spectrum story. Says Manuel, "After getting the gist and scope of Spectrum from HP Laboratories chief Joel Birnbaum, and then plenty of detailed information from the engineering and architecture manager, Michael Mahon, I still have this sense that I have only seen the tip of the iceberg. So many people did so many measurements and analyses, and had so many brainstorming and detailed engineering sessions, that it is clear this was an engineering project by a company with a long history of technical and engineering expertise. The beautifully simple architectural result of all this careful engineering reminds one of other engineering achievements, such as the building of a great bridge."


TOM MANUEL: The pleasure of exploration.

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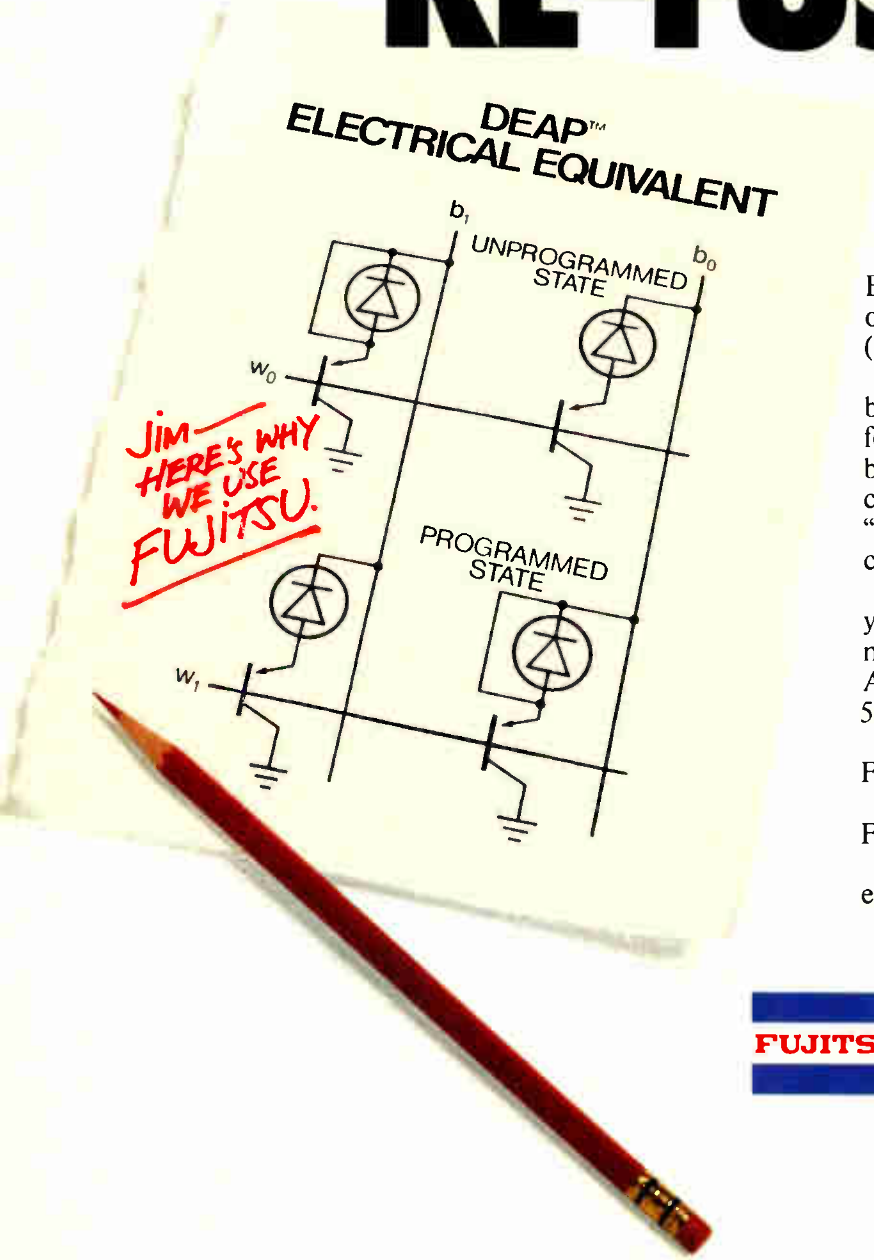

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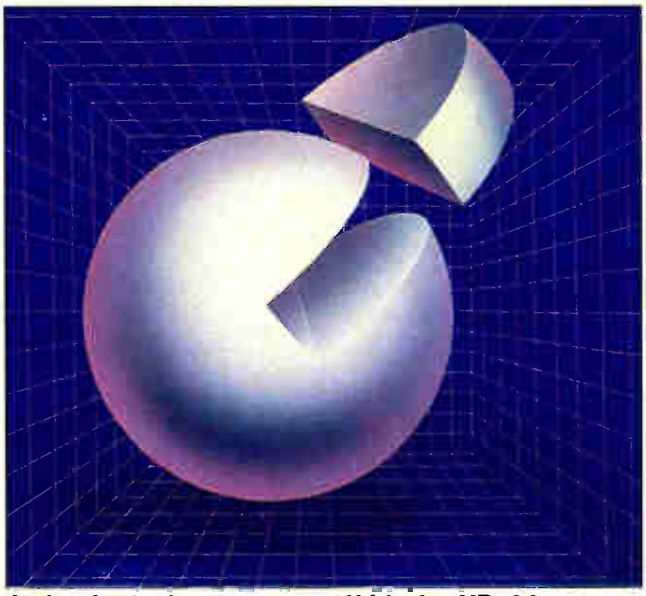
Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER



NEW PRODUCTS

DEPARTMENTS

THE ONLY QUICK–TURN GUARANTEE.

Feature Size: 2μ

	N-Channel	P-Channel
VTEO	$0.5–1.0_V$	$0.5–1.0_V$
BVDSS	$>10_V$	$>10_V$
$K' = \frac{\mu c}{2}$ linear region	21–25	6.5—8.5
B_E(Long Channel)	$0.8–1.2_V{}^{1/2}$	$0.4–0.6_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	8–10	8–10
Cap. Poly to Sub 10^4 PF/cm^2	0.55–0.65	0.55–0.65
Cap. Metal to Sub 10^4 PF/cm^2	0.27–0.32	0.27–0.32
Junction Depth	$0.4\mu–0.6\mu$	$0.2\mu–0.4\mu$
P-Well Junction	$2.5\mu–3.5\mu$	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	20–40Ω/□	60–100Ω/□
VTF Poly	$>10_V$	$>10_V$
ΔW	$—1.0\mu$	$—1.2\mu$
LEFF	$1.0\mu–1.4\mu$	$1.3\mu–1.7\mu$
Substrate Resistivity	2.5KΩ/□	1.2Ω/cm

Feature Size: 3μ

	N-Channel	P-Channel
VTEO	$0.5–1.0_V$	$0.5–1.0_V$
BVDSS	$>10_V$	$>10_V$
$K' = \frac{\mu c}{2}$ linear region	18–21	6–8
B_E(Long Channel)	$0.8–1.4_V{}^{1/2}$	$0.4–0.6_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	5.9–7.0	5.9– 7.0
Cap. Poly to Sub 10^4 PF/cm^2	0.45–0.55	0.45–0.55
Cap. Metal to Sub 10^4 PF/cm^2	0.2–0.25	0.2–0.25
Junction Depth	$0.6\mu–1.0\mu$	$0.4\mu–0.8\mu$
P-Well Junction	$3.5\mu–4.5\mu$	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	10–30Ω/□	30–70Ω/□
VTF Poly	$>10_V$	$>10_V$
ΔW	$—1.0\mu$	$—1.0\mu$
LEFF	$1.4\mu–2.0\mu$	$1.8\mu–2.4\mu$
Substrate Resistivity	2.5KΩ/□	1.0–1.5Ω/cm

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