

OCTOBER 20, 1983

SPECIAL REPORT: TRANSFORMING THE FACTORY WITH TECHNOLOGY/120

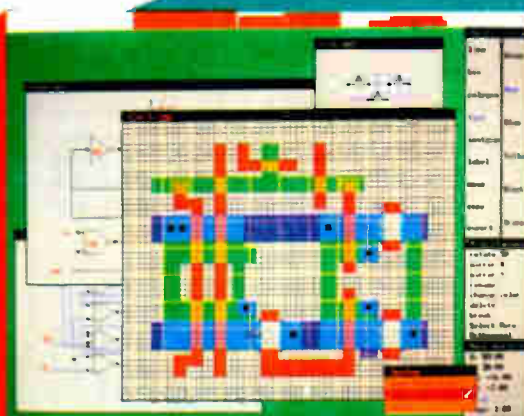
How VLSI chips are influencing computer architecture/97

Eight-bit slices offer precision and performance/133

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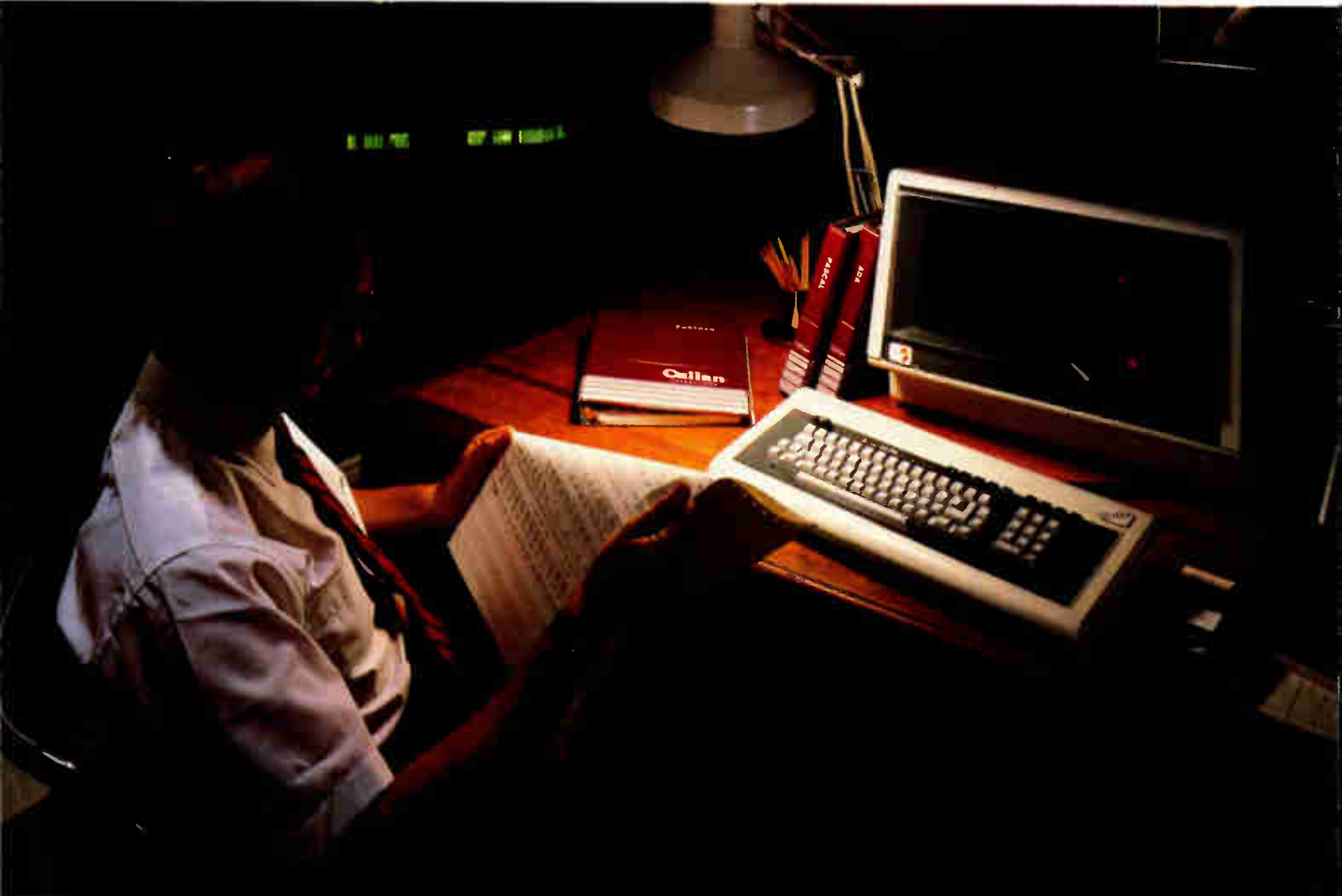
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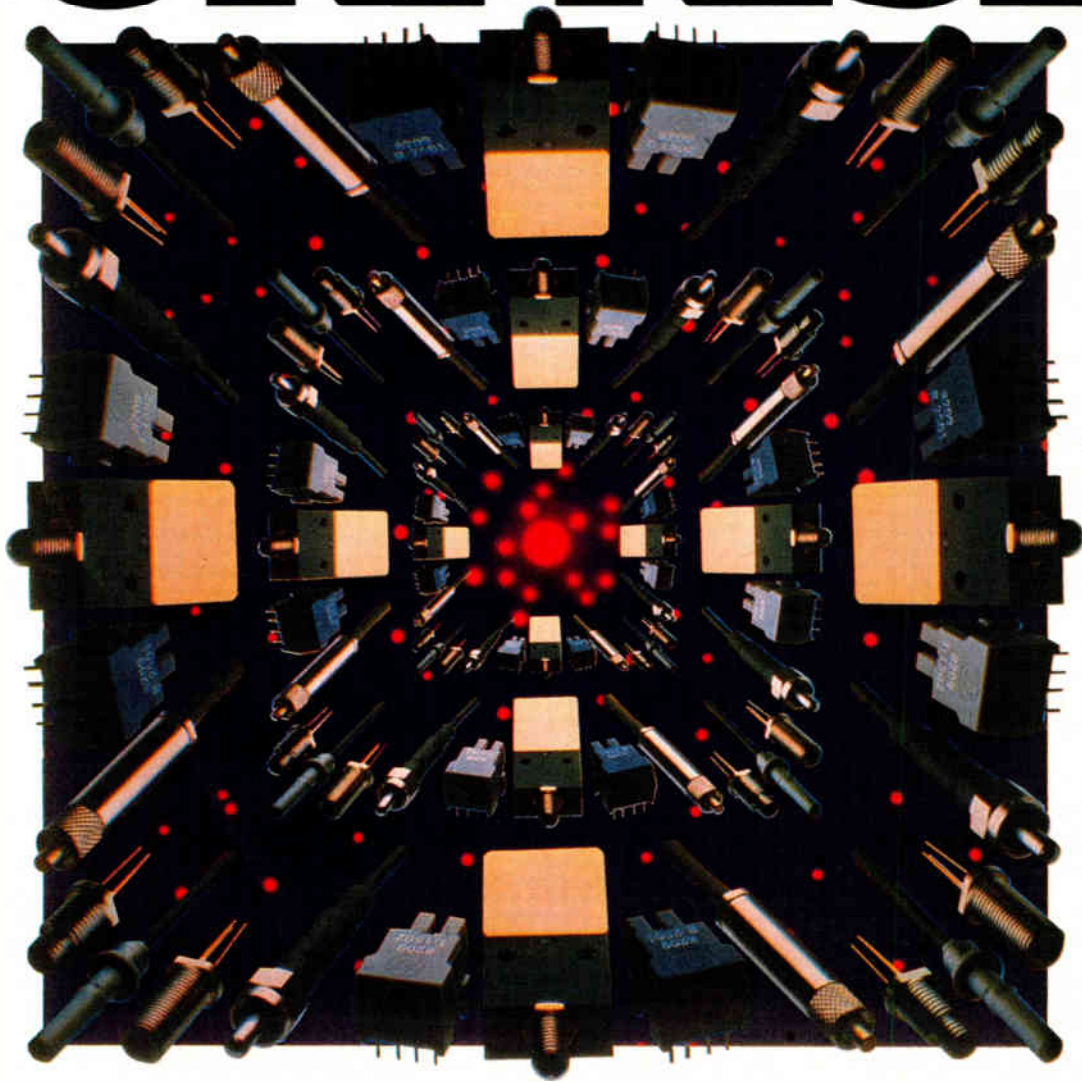


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Cover designed by Art Director Fred Sklenar

The Cover Story

Work station handles real-time graphics, 113

Designs become images in real time on a new work station that runs a virtual-memory form of Bell Laboratories' Unix operating system and hooks into the Ethernet local network.

Major New Developments

Modernizing the production line

The melding of computer-aided design and manufacturing into computer-integrated manufacturing is starting to revolutionize factory automation, says this special report. Five articles describe its facets, from decision-support systems to autonomous robot cells, 120

Silicon compiler speeds microcomputer to market

The processor for Digital Equipment Corp.'s MicroVAX I machine was readied in less than a year, thanks largely to a custom chip prepared by a silicon compiler, 47

Network welcomes all comers

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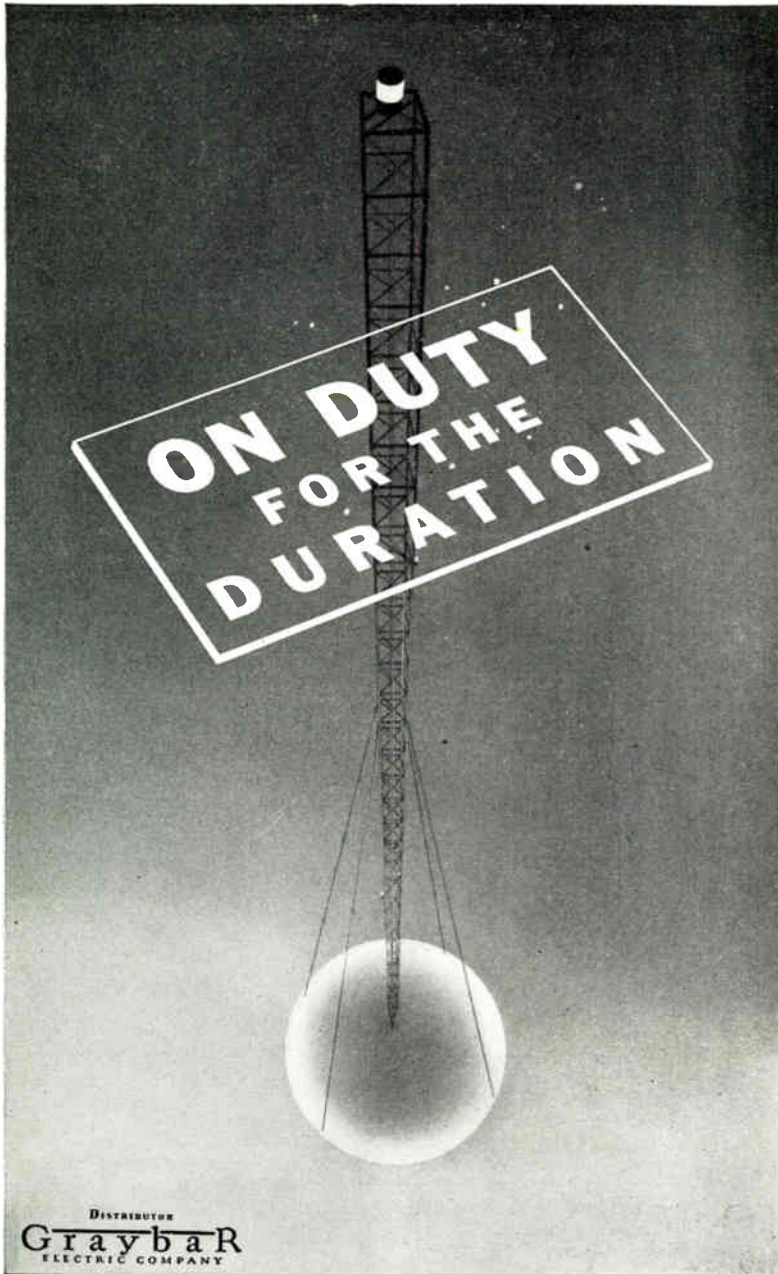
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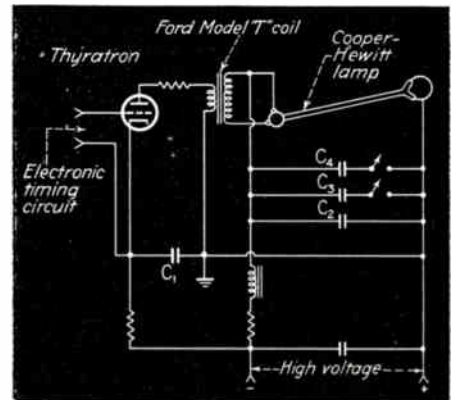


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A Cooper-Hewitt mercury vapor lamp connected in the circuit shown makes a good high speed stroboscopic light source. A lamp that has been retired from regular illuminating service because of starting difficulty will fire satisfactorily in this circuit

The high voltage power supply connected across the ends of the lamp causes further ionization and capacitor C_2 discharges through the Cooper-Hewitt. Additional brilliancy may be obtained by closing one or both switches, connecting C_3 and C_4 in parallel with C_2 . The associated electronic timing circuit regains control of the thyatron by swinging the thyatron grid sharply negative soon after C_1 discharges, at which time the anode voltage is at a minimum. —Street, *ELECTRONICS*, April, 1940, p. 36.

Stimulus-Physical or Chemical

(Continued from page 76)

Motor Speed Checker

THE SPEED OF SMALL motors may be determined under conditions approximating no-load by the method shown in the diagram.

A small metal fitting, *A*, is fastened

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BOOKS & SPECIAL PROJECTS MANAGER

June A. Noto

Cover: Real-time graphics, Unix, Ethernet meet in a work station, 113

Supporting a real-time three-dimensional color-raster graphics system, a new work station boasts AT&T Bell Laboratories' general-purpose Unix operating system. Because it is equipped with Ethernet capability, the machine can run in a network of shared resources in which it may be configured as a graphics processor, as well as a stand-alone station.

Optical storage stakes its claim in high-density realm, 101

Laser-based optical-disk systems are attracting attention, as practical systems prepare to challenge magnetic-storage techniques for high-density applications like archival storage. Achieving erasability is the next goal.

Computer automation invades the production line, 120

Factory automation is moving from concept to reality, with computerized manufacturing techniques starting to spread. This collection of articles gives a picture of the way in which the automated factory is developing.

■ Computer-integrated manufacturing, in which automated operations are linked into a comprehensive data base, is the ultimate goal, 121

■ For flexible manufacturing in which small batches of different products run down the same line, decision-support software is essential, 123

■ Computerized gear is coming from many sources, so a communications network that links units from many sources jumps a major roadblock, 125

■ To make proper use of robots, a new system fully simulates the setup in which the automatons will be functioning, 128

■ High-precision electronic systems can be turned out solely by robots, a prominent example being the production of Winchester disk drives, 131

Bit-slice processor, microsequencer hit video speeds, 133

An 8-bit-wide bipolar bit-slice processor reaches new performance heights through such advances as a denser process and multiple data paths. A companion microsequencer boosts system responsiveness by harnessing the processor's computing power efficiently.

Superminis cluster together for multiprocessing, 143

General-purpose computer hardware and software can be the basis for a highly sophisticated multiprocessor setup, providing a highly available, easy-to-extend system incorporating a widely used operating system and backed by abundant programming support.

Coming up . . .

Artificial intelligence enters the realm of practicality: Part I of a two-part special report . . . reactive-ion etching hits its stride . . . what's doing at Wescon/83: key technical sessions and major product introductions.

October 20, 1983 Volume 56, Number 21
112,416 copies of this issue printed

Electronics (ISSN 0013-5070). Published every other Thursday except the Dec. 29th issue, by McGraw-Hill, Inc. Founder: James H. McGraw 1860-1948. Publication office 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, N.Y. and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 997-1221. Teletype 12-7960 TWX 710-581-4879. Cable address: MCGRAW HILL NEW YORK.

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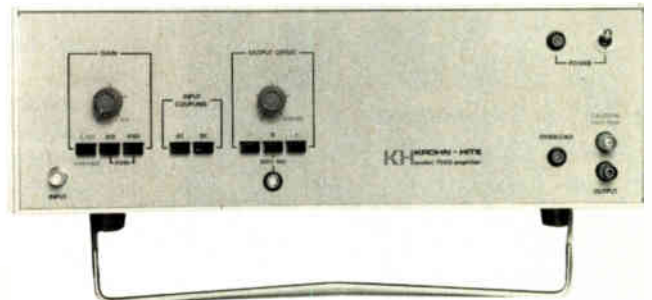
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Publisher's letter

Our technical editors all have to keep track of a variety of topics within their specialties, but the beat that industrial and consumer editor Erik Keller covers embraces more different technologies than any other. In the world's factories, however, many of these technologies come together, as companies strive to speed up throughputs and improve the quality of their products. Indeed, a little bit of all the other editors' domains includes modernizing production processes.

This issue's special report on Computerizing the Factory Floor (p. 120) takes into account a range of technologies and shows how they all interrelate. "It's not an easy matter to modernize a factory. You have production schedules that must be kept as well as the need to convince management that it is cost-effective for them to make these changes," says Erik.

"After all the arguing is over, then comes the hardest task: integrating organized technology into an environment that is usually far removed from anything approaching the ordered. In addition, because the production process is so complex, the matrix of decisions that must be made is staggering."

So for this report, Erik tied together five technical articles along with an overview that he thought could give a bare-bones representation of the sort of things that are needed for automating production. Data bases, networks, support software, simulation, and a good idea of how to implement them are crucial to bringing today's factories up to date, he thinks.

"Behind any attempt to get modern equipment into a factory in a big way, rather than just replacing a relay board with a programmable controller, is the use of good software to help planners make decisions and come up with designs long before a system is physically constructed. After a system is built, simulation and decision support techniques help managers tweak designs and repair problems quickly," Erik explains.

Perhaps the most interesting thing about automating industry is that

these techniques have been adopted first by manufacturers more familiar with ingots of steel than wafers of silicon. "It is difficult to guess why traditional industry has embraced automation more than high-tech firms, but one thing is sure: many U. S. traditional industries are going through rough times now, though it has been easier for the ones that have modernized. Electronics firms haven't reached that point yet. But they seem to see that if they don't bring their manufacturing technology up to date, they could face hard times, too."

A symbiosis between computers and integrated circuits has existed ever since the first chips emerged, and the two have become even more interdependent with the advent of very large-scale integration. That is so much the case that the annual meeting where computer people and semiconductor people get together to talk about the state of the art in their disciplines has become, in the words of computer editor Tom Manuel, "one of the most exciting events of the year."

This year's "VLSI in Computers" conference is scheduled for the end of the month in Rye, N. Y., and our preview of it starts on page 98. Fittingly, the piece is a joint effort by Tom and Roger Godin, who this month switched over to the solid-state beat from communications and microwave.

Both rate the papers on computer-aided design for VLSI circuits as very impressive. And Tom expects keen interest in the updates on artificial intelligence and on leading-edge devices like Josephson junctions and the quiteron.

For Roger, this is a return to familiar ground. Before signing on with us, he was a field sales engineer for VLSI/MOS at Texas Instruments' office in Boston.



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Readers' comments

Kudos

To the Editor: Recently, while I was reviewing back issues of *Electronics*, including the reprint of the very first issue [April 1930] and the momentous 50th anniversary issue [April 17, 1980], I realized how important a role your magazine has played in shaping my whole career and hence my life. I first started reading *Electronics*, secondhand, when I was a college student, back in 1960. I do not think that I have missed even a single issue since then, nor, says my wife, have I thrown out a single issue.

The editorial quality of *Electronics* has always been of the highest. The lucid and clear writing in your pages is always a pleasure to read. In my opinion, *Electronics* stands above other technical publications for the simple reason that it and it alone is literate.

Having been guided by your writers and editors through vacuum tubes and relays into transistors, through the first monolithic circuits, and now through the present state of the art, I continue to look to *Electronics* for definitive reporting on our industry and its impact in the world. So this letter is of a personal nature—one that I have been meaning to write, my attempt to thank you and your staff for all that I have learned from your pages.

Michael Callahan
Winchester, Mass.

The move to 6-inch wafers

To the Editor: Your article "Jury still out on 6-in. wafers" [Aug. 25, p. 110] left out one very important factor in the present move to 6-inch wafers. As a supplier of very large-scale integration equipment, Ultra-tech Stepper can convert its stepper to 3-, 4-, 5-, or 6-in.-wafer handling in just half a day, at a cost of only \$30,000. We have sold steppers to four semiconductor houses other than the giants you mentioned—houses that are planning to go from 4- to 6-in. steppers.

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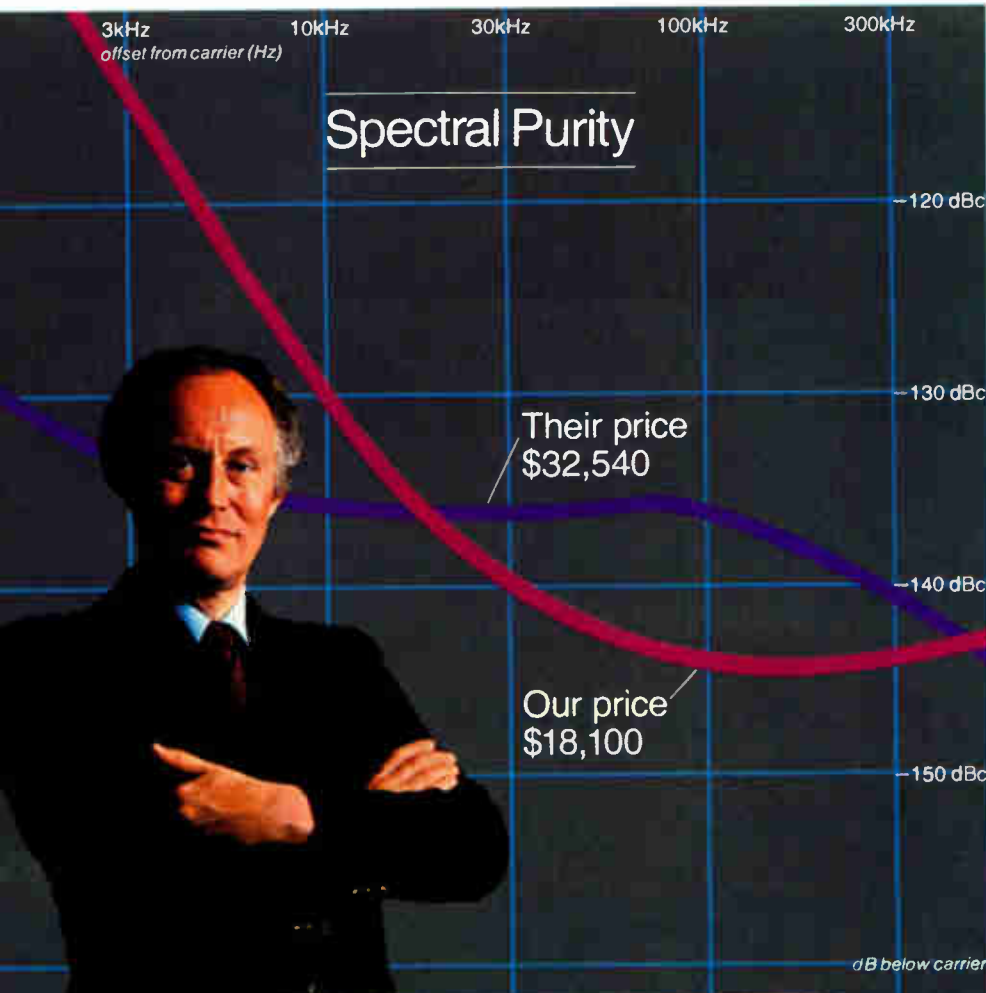
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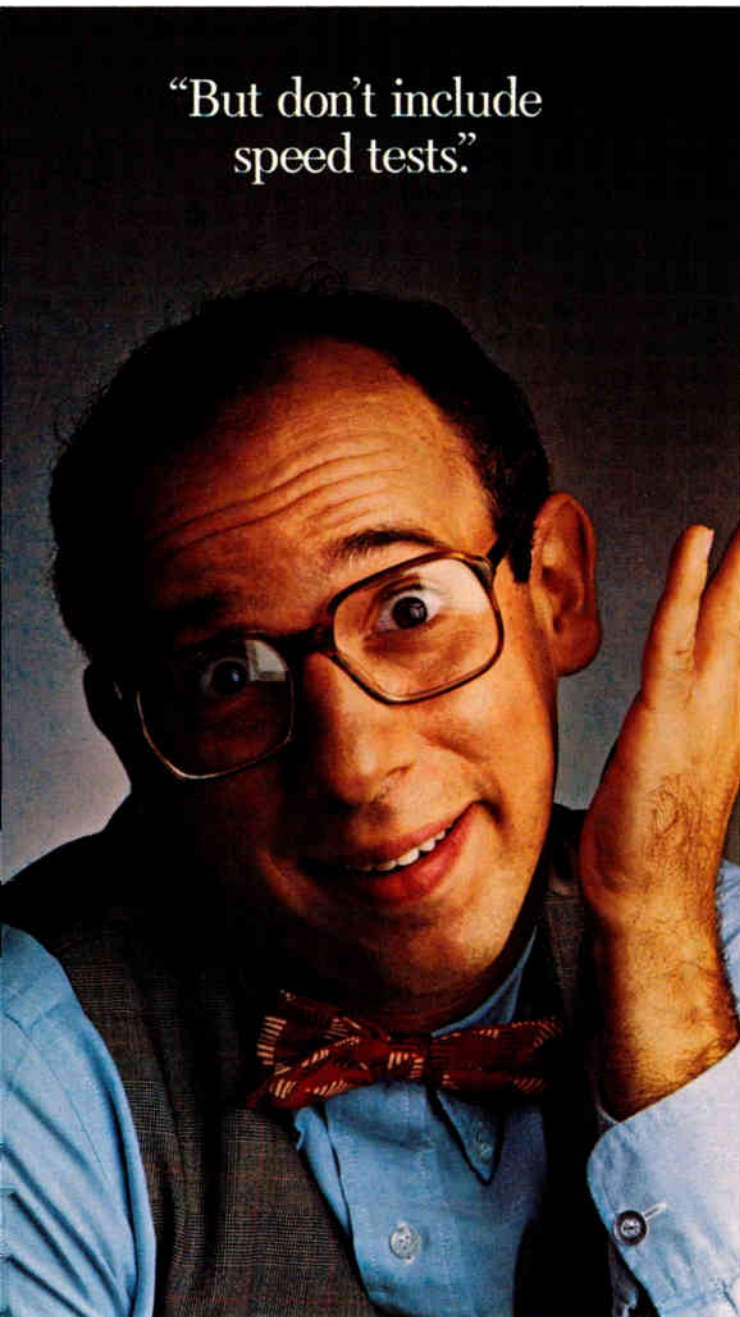


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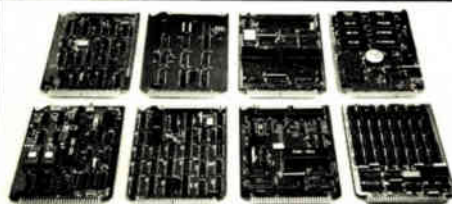
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Readers' comments

start-ups are taking advantage of the production increases possible with 6 in. and have bought our equipment. The trend-setters are not going to be the large companies—although in fact we have shipped 6-in. steppers to Intel—but rather the small companies, those attempting to get an edge on the giants.

Dale Ann Springer
Sales and Marketing
Ultratech Stepper
Santa Clara, Calif.

To the Editor: Your article on 6-in. wafers did not offer the perspective of corporations that are now starting to enter semiconductor production. It is surely no surprise that major semiconductor manufacturers are not inclined to convert 4- and 5-in. facilities into 6 in., given the vast capital investment they have made in old equipment. An industry that is still deciding whether or not the recovery is real can no doubt well afford to wait until current utilization levels rise above 50% before starting to add capacity.

However, for a company to choose 4- or 5-in. equipment for a new, large-volume facility would be anything but prudent. The difference in die per wafer, in terms of factory output, is greater than your article suggests. In surface area, 6-in. wafers are 2.25 times the size of 4 in., but the edge effect (the loss of usable die at the wafer's edge because of curvature) gives 6-in. wafers 2.75 times more net die per wafer. Reduced handling and processing make further contributions to the larger wafer's advantage.

Lattice Semiconductor Corp. regards the timing of its debut in the industry as most opportune. Our ability to begin production with 6-in. wafers—a turning point in process-equipment generations—not only gives us a cost advantage over established chip manufacturers but also cuts our capital requirements: our \$25 million 6-in. facility will produce more chips than three \$22 million 4-in. facilities would.

Raymond P. Capece
Lattice Semiconductor Corp.
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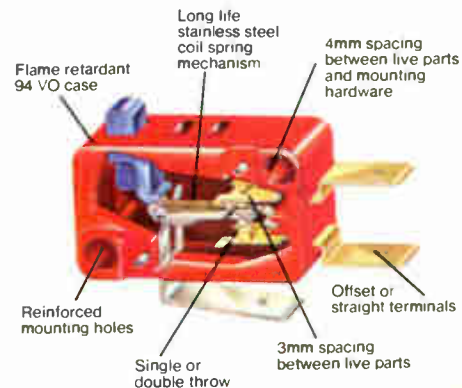
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People

Skantek is the culmination of Paradis's professional life

Roger Paradis has been training all his adult life to start a company and run with it. About a year ago, Paradis and two partners formed Skantek Corp. [*Electronics*, Sept. 8, p. 52] to build and market a compact machine that digitizes engineering drawings for entry into computer-aided-design systems. It is the confluence of his technical, marketing, and managerial experiences.

Tall and urbane, Paradis breaks out of character when he talks excitedly about Skantek. Its digitizer, marrying fiber optics and charge-coupled-device technology, "will bring the technology into being within the market," now dominated by cumbersome laser scanners.

Skantek's compact and convenient digitizer is brought to the user, says Paradis, instead of the reverse. He predicts its \$100,000 price, about a third of the others, will "blow the market wide open."

When he founded the Warren, N. J., company, Paradis, now 38, worked just down the road in Morristown as head of Tetrion Consulting Group, which he also founded, advising businesses on technologies concerning voice, data, image, and text. Before that, from 1975 to 1980, he reported to nearby AT&T corporate headquarters as a planning manager on the president's staff, after serving as a marketing manager.

"AT&T was starting to go through a period of change," he recalls. "I was involved in making it marketing-sensitive." Thus, although the company is large, his experience there was entrepreneurial.

Paradis received an MBA from Harvard in 1974, capping a master's in nuclear physics from the U. S. Naval Nuclear Power School—perhaps, surprisingly, "some of the best management training I've received," he says—and a Naval Academy BS. At Harvard, he had formed a corpora-

tion to publish a handbook on business terms he co-authored. The book sold 60,000 copies and is still going strong. His first job was as line sales manager for Raychem Corp., which makes parts for the electronics and aerospace industries. "It gave me a sense of engineering markets and



Changing direction. Roger Paradis says Skantek digitizer goes to the customer instead of the reverse.

strategy," he says.

At the time that Skantek was first envisioned, at the nadir of the recent recession, "most people thought the timing was wrong," Paradis recounts. "But we projected the economy would pick up as we built up, and we'd end up on the right side of the curve." His projections, he thinks, are bearing out. He is already planning to take the company public.

InterFET has roots in Hoye's hourly job at TI

Some budding entrepreneurs were apparently born with start-ups on their minds. Others achieved new venture opportunities through insomnia and indigestion. Michael B. Hoye had entrepreneurship thrust upon him by traveling a path of seemingly unrelated milestones.

At 18, Hoye took an hourly production job with Texas Instruments Inc., in Dallas. He wanted to move up in the world as an aeronautical engineer but instead developed an interest in semiconductors. Today, the 37-year-old native of Providence, R. I., is president of a new company



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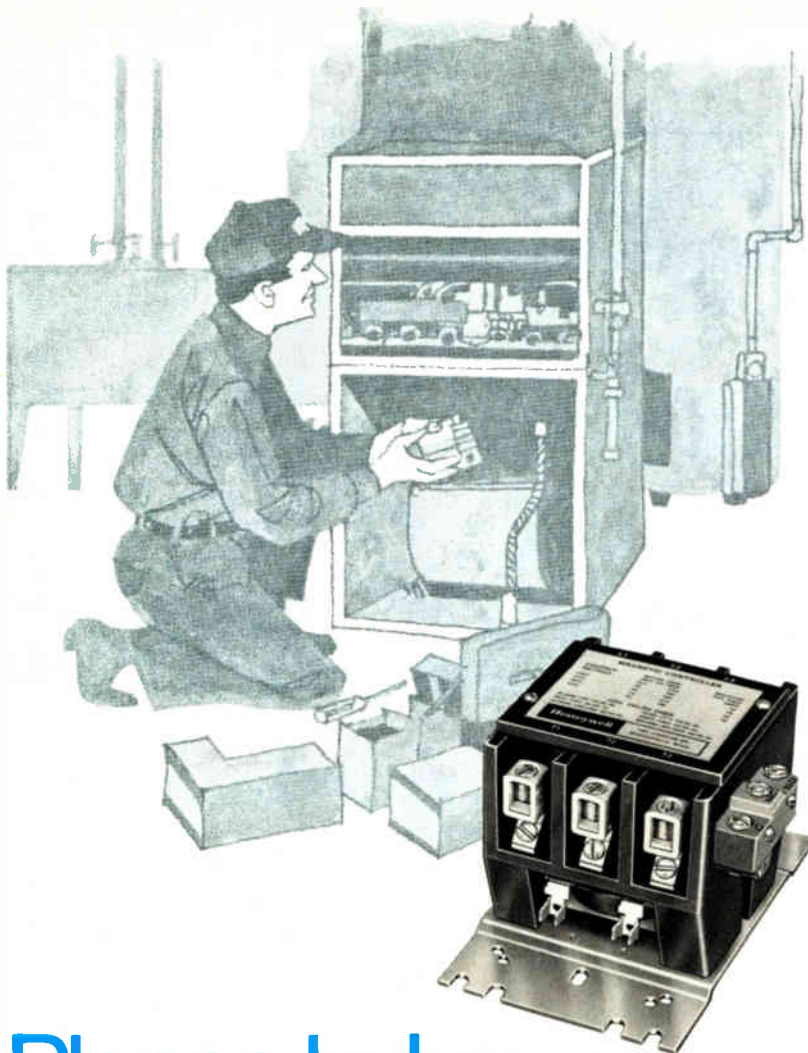
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People



Filling a void. Michael Hoye's InterFET sells where big companies find it unprofitable.

that he and a few former TI associates formed in 1982.

InterFET Corp., in Garland, Texas, manufactures junction field-effect transistors—devices used in a growing number of military and commercial instrumentation systems and in hybrid-circuit markets. The company is carving out its initial market niche in the small-signal discrete business by providing both standard and custom-designed J-FETs, in packaged and unencapsulated form.

Much of InterFET's strategy is targeted at hybrid-circuit companies, which, according to Hoye, are now having more trouble dealing with large semiconductor firms, whose monolithic integrated circuits often compete against hybrids.

"Selling unencapsulated chips is not easy for large companies," Hoye notes. "It's not as profitable for them as packaged devices, and it tends to expose the technology."

Some estimates suggest that the small-signal market may be growing at a rate of 9% a year, but Hoye says that InterFET is focusing strictly on J-FETs, whose sales are rising at a 17% annual rate. "The motivation in the discrete field-effect transistor area is that while MOS FET technology accounts for much of the integrated circuits today, high-performance J-FETs are very difficult and rarely included," he notes.

InterFET has begun taking orders on some 79 part numbers, which represent nine basic J-FET device types. Hoye believes InterFET will have revenues of \$3 million in 1984, rising to \$6 million in 1986. "But \$5 million could come in 1985." □

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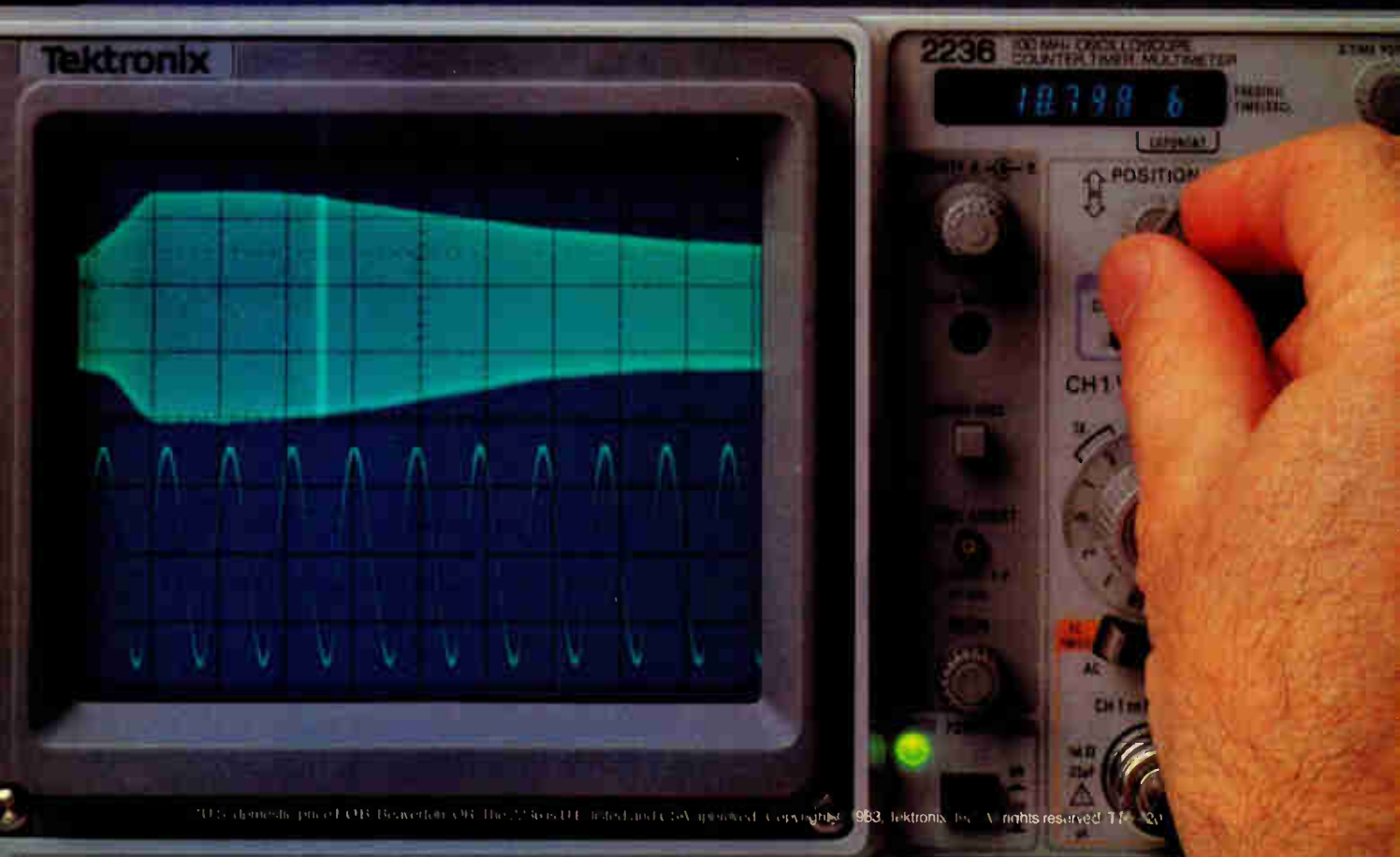
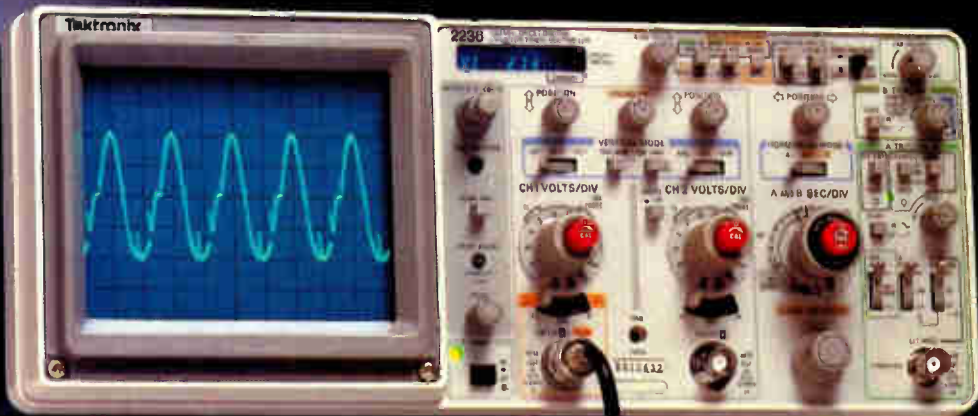


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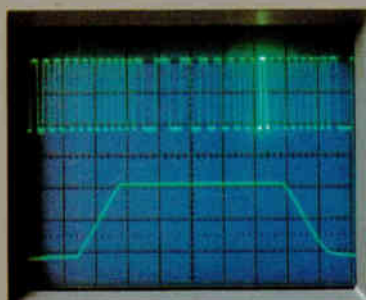
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Left top: Ch 1 true RMS & DC volts measurements. Made easily at the probe tip. (The 2236 adjusts automatically to 1X or 10X probes.) The 2236 includes relative reference capability for subtracting offsets.

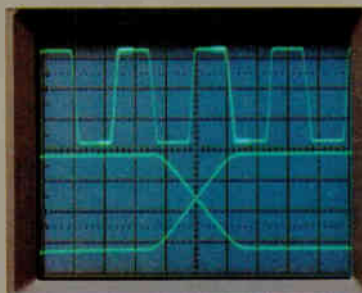
Left bottom: Gated frequency measurement. Intensified zone brackets the period of interest by means of the delayed sweep, allowing easy frequency measurement on any specified portion of the waveform.

vides resistance measurements ranging from 0.01Ω to $G\Omega$ —as well as audible continuity. Oper-



39504.6

Gated width measurement. Pulse of interest is selected with the intensified zone. Both width and period measurements are made with up to 10 ps resolution.



377000.6

Delta time measurement. Time between two intensified zones on the A sweep is measured with up to 50 ps accuracy.

ator prompts, auto-ranging and audible, automatic diode/junction detection features serve to simplify set-up and enhance confidence in your measurements.

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Absolutely no clocks or timing strobes.

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ORGANIZATION	ACCESS TIME (MAX)	PART NO.	PACKAGE TYPE	OPERATING CURRENT (MAX)	STANDBY CURRENT (MAX)	TECHNOLOGY
16K x 1	35,45,55	MCM2167HL	300 Mil Ceramic DIP	120 mA	20 mA	HMOS
	35,45,55	MCM2167HZ	Leadless Chip Carrier	120 mA	20 mA	HMOS
	35,45,55	MCM2167HP	300 Mil Plastic DIP	120 mA	20 mA	HMOS
2K x 8	45,55,70	MCM2016HY	300 Mil Ceramic DIP	120 mA	20 mA	HMOS
	45,55,70	MCM2016HL	600 Mil Ceramic DIP	120 mA	20 mA	HMOS
	45,55,70	MCM2016HP	600 Mil Plastic DIP	120 mA	20 mA	HMOS
2K x 8	120,150,200	MCM6116P	600 Mil Plastic DIP	55 mA	2000 uA	CMOS
	120,150,200	MCM611L16P	600 Mil Plastic DIP	55 mA	100 uA	CMOS
4K x 1	55,70	MCM6147P	300 Mil Plastic DIP	35 mA	800 uA	CMOS
	55,70	MCM61L47P	300 Mil Plastic DIP	35 mA	100 uA	CMOS



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Please send me more information on Static Rams

A MCM2167H B MCM2016H C CMOS

157ELEX102083

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Title _____

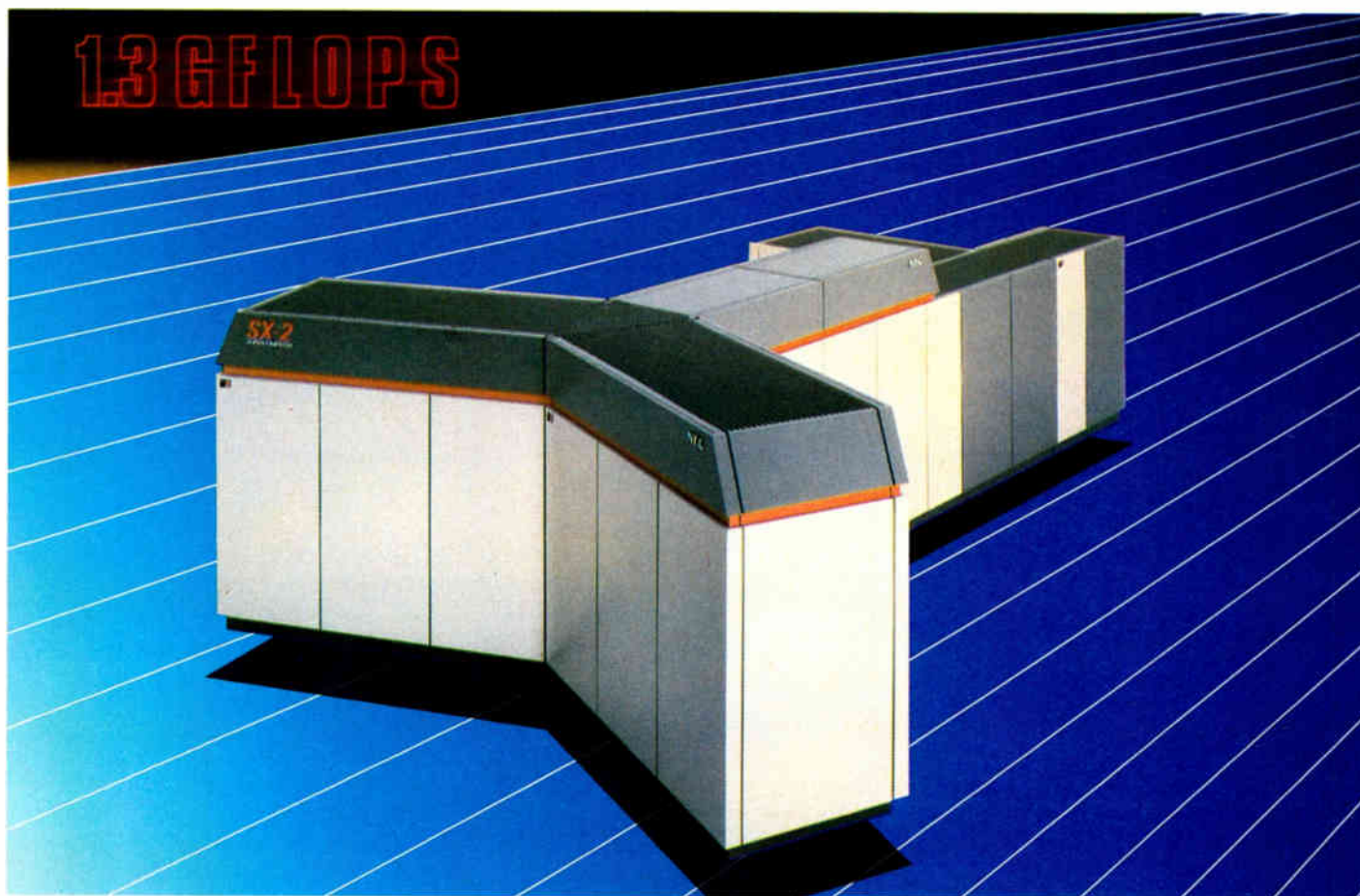
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NEC NEWSCOPE



NEC SUPERCOMPUTER OPERATES AT 1.3 GIGA-FLOPS

Large-scale scientific computations can be processed at giga-level speeds up to 1,300 Million-FLOPS* by NEC Supercomputer SX-2.

Its advanced architecture employs: Four vector pipelines for multi-parallel processing; extensive vector operation function support; scaler pipeline and associated flow analysis techniques; 256Mbyte main memory with 11 gigabyte/sec

throughput, 2 gigabyte extended memory; and independent arithmetic processor and control processor.

NEC Supercomputer SX-2 shares new high-speed LSI chips and high-density LSI packaging technology with NEC Supercomputer SX-1, which operates at up to 570 M FLOPS. The new chips are: a 1K-bit bipolar memory for registers with a fast access time of 3.5 nano-

seconds; and a 1,000-gate logic chip with a delay time per gate of 250 picoseconds. These logic chips are mounted in groups of 36 per 10cm square ceramic substrate and use a new liquid-cooling system.

Available as software is FORTRAN 77/SX, which has a highly sophisticated automatic vectorization function and can compile generally-used FORTRAN 77 programs. To improve the vectorizing ratio, VECTORIZER/SX and ANALYZER/SX are also offered.

NEC will begin domestic delivery of the supercomputers in early 1985.

*Floating point operations per second.

FIRST INMARSAT- APPROVED SHIP EARTH STATION

The first compact Standard-A ship earth station type approved by INMARSAT is on the market for maritime users.

The ST11A is designed to let ships as small as 100 tons handle voice, telex, facsimile and medium-speed data communications. Its high-efficiency L-band parabolic antenna is only 0.85m in diameter, and its above-deck equipment has a combined weight of approximately 150kg, making it much smaller and lighter than equipment built around the conventional 1.2m antenna.

The below-deck equipment—also built compact—uses modular and microprocessor circuits extensively to achieve easy operation, high station performance, and reduced power consumption.

Made to withstand the most severe weather conditions, the ST11A offers ship owners substantial benefits in convenience and safety.



NEC ST11A INMARSAT ship earth station.

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Digital audio's superb sound fidelity is acknowledged by audio connoisseurs. For example, dynamic range and signal-to-noise ratio both exceed 90dB, and channel separation is better than 70dB across an audio band extending from 5Hz to 20kHz.

But NEC's CD-803E compact disc digital audio player incorporates three innovations that set it apart from other CD players: (1) A three-stage servo for the disc motor which detects and

corrects severe dropouts caused by external noise or disc damage; (2) A high-speed switch which operates 10 times faster than commonly used CMOS devices or analog switches, to lower high-frequency distortion; and (3) a Non-Delay filter.

The Non-Delay filter eliminates the sampling frequency (44.1kHz) after the digital signals have been converted into analog by the D/A converter. Commonly used active and passive filters suffer phase-related distortion called group delay. The Non-Delay filter reduces group delay at 20kHz to 1/25th the value of other filter designs and significantly reduces unwanted spurious-frequency response, thereby making high notes pure and clear.



1GHz SILICON MONOLITHIC IC AMPLIFIER

A microwave amp can now be built simply by connecting input, output, and power supply to a monolithic IC from NEC.

By eliminating the laborious design and assembly procedures required to make a microwave amp using discrete devices, the new silicon ICs offer tremendous

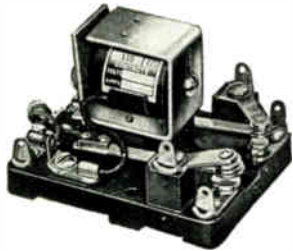
cost and time advantages. They feature 19dB gain and 5dB NF. For 5V operation, they come in Disk Mold, 8-pin MINIFLAT, 8-pin DIP and TO-72 types. For 10V, 8-pin DIP and TO-33 are available.

NEC monolithic microwave ICs will find many applications in communications, instrumentation, and consumer products.

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NEC Corporation
P.O. Box 1, Takahawa, Tokyo, Japan.

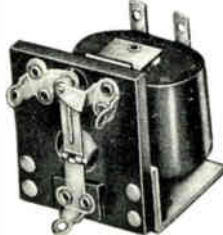
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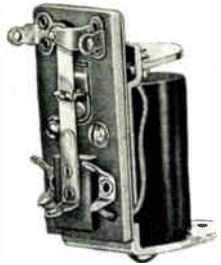
GUIDE TO KURMAN RELAY SPECIFICATIONS

SERIES	RATED INPUT		AMPERE CONTACT RATING	WEIGHT OUNCES	DIMENSIONS INCHES
	DC WATTS	AC V.A.			
5	2.5	8.0	15	7 3/8	3x2 1/4 x2 1/4
10	.35	—	.5	1 3/8	1 1/8 x1 1/8 x1 1/8
11	.80	4.4	1	2 1/8	1 3/8 x1 3/8 x1 3/8
12	.018	—	.25	1 1/8	1 1/8 x1 1/8 x1 1/8
15	2.0	6.0	1	3 3/8	1 3/8 x1 3/8 x1 3/8
25	2.0	4.0	10	4	2 1/8 x1 3/8 x1 3/8
200	.014	.36	3	6 3/8	2 1/8 x2 3/8 x1 3/8
300	.014	.36	3	6 7/8	2 1/8 x2 3/8 x1 3/8

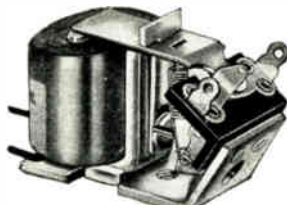
NOTES

- I. All current contact ratings are in amperes at 110 volts 60 cycle AC.
- II. Dielectric strength of 1500 volts exists between contacts and ground in Series 10, 11, 15.
- III. Insulated armature, shown on Series 300, is recommended for high frequency transfer. This feature may be specified for Series 200.
- IV. Ferronickel alloy is used in the magnetic circuits for Series 10, 12, 200, 300.
- V. Ceramic insulation in Series 25 permits

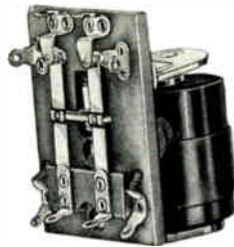
- high frequency transfer with low capacitive leakage.
- VI. Dampened armature action in Series 25 is designed to reduce contact bounce after initial pull down.
- VII. Rated watts represents practical minimum input at standard adjustments.
- VIII. AC relays have approximately .5 power factor.
- IX. List prices vary with specific voltage and insulation requirements.



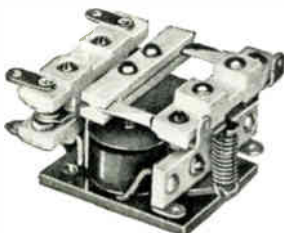
Series 11



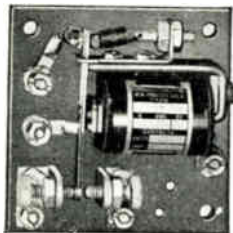
Series 12



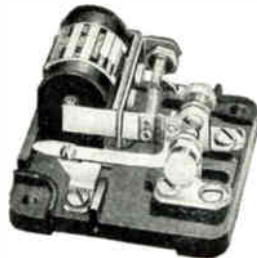
Series 15



Series 25



Series 200



Series 300

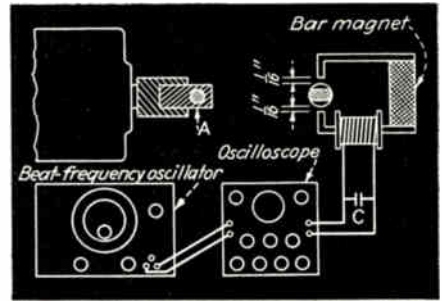
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to the motor shaft and acts as the rotor element of an a-c generator. The frequency of the a.c. generated in the coil surrounding the magnet of the generator is directly proportional to the speed of the motor and can be used as the basis of a comparison measurement. The output of the coil is connected to the vertical deflection plates of a cathode-ray oscilloscope, while the horizontal plates lead to a beat-frequency oscillator whose frequency calibration may be marked directly in rpm. The beat frequency is adjusted until the pattern formed on the oscilloscope is a simple ellipse, which is the Lissajous figure indicating that the two oscilloscope input frequencies are the same.

The a-c generator does not produce a true sine-wave but the harmonics introduced may be attenuated by the capacitance *C*, connected across the generator output.—Clough Brengle, *ELECTRONICS*, October, 1939, p. 47.

Temperature Control

A CONTROL FOR maintaining the temperature of any enclosed chamber within a few thousandths of a degree has been developed in the laboratories of the Shell Development Co. It uses a resistance thermometer controlling a thyratron tube through a phase-shifting network. The resistance changes with temperature and therefore is useful for converting a temperature change into a voltage change the thermometer is located in the chamber and is connected in a Wheatstone bridge circuit to which is applied a 60-cps voltage. When the bridge is balanced the temperature is at the desired point and nothing happens. If, however, the temperature falls below the

Congress should make joint R&D more attractive

If two or more U. S. companies competing in, say, the consumer audio business had decided that it would have been beneficial and fruitful to establish a joint research effort designed to bring to the market a pocket-size portable cassette-tape player with miniaturized earphones, the chances are they would have had to do so over the vehement objections of their attorneys. Such an enterprise could have been construed as a violation of the nation's strict antitrust laws, and they would have been subject to a lawsuit and, if found guilty, to treble damages.

But times have changed. With high technology now one of the nation's basic resources and with research in the various individual technologies—notably computers and communications—becoming increasingly complex and expensive, the initiative and world leadership has been slipping slowly away from America's shores. Companies in the U. S. maintain that their foreign competitors labor without such fetters and point to government-sponsored joint R&D thrusts in Japan and elsewhere. In fact, some movement in the direction of Government-blessed joint R&D has started, particularly with the advent of the Microelectronics & Computer Technology Corp. Still, most executives agree that the time has come for some form of statutory relief from the severe penalties.

Such an easement might be coming. The Reagan Administration has sent a bill to Capitol Hill, labeled the National Productivity and Innovation Act of 1983. Executive-branch staff members who keep an eye on such things think it has a good chance of passing; their opposite numbers in the Con-

gress are somewhat less sanguine.

The bill has made a bit more progress in the Senate than in the House. There, sponsored by Strom Thurmond (R., S. C.), it is before the Judiciary Committee, which is scheduled to start hearings on Oct. 18. On the House side, where it has been referred to the monopolies subcommittee of the Judiciary Committee, it will probably be sponsored by Peter V. Rodino (D., N. J.).

The measure's provisions include actual damages plus costs rather than treble damages for antitrust violators, as well as virtually automatic immunity attainable simply by notifying the Department of Justice of a proposed venture, who is involved, and its scope. Also, there are two Democratic bills that originated in the House and would effect less sweeping changes; with an eye on the 1984 elections, the Administration is eager to get its version approved.

There is some fear in the capital that any relief measure would merely open the floodgates to abuses. That is understandable—after all, human nature being what it is there will always be the unscrupulous trying to find a loophole large enough to slither through. But there will be provisions for punishment; malefactors still will face the wrath of the courts. Finally, the risk must be reckoned as a small thing compared to the potential gain: the opportunity to bring to bear the full strength of American technological genius in the worldwide high-technology derby. We urge Congress to move on this issue, and we urge our readers to inform their representatives and senators of the need for positive action.

How can the best DMM and Calibrator increase your productivity?

The new Fluke 8506A Thermal RMS Digital Multimeter and the 5440A Direct Voltage Calibrator meet your tough demands in the calibration and performance verification of electronic products. What is normally a very time consuming and tedious job can now be performed fast, simply, and accurately.

The best for production or calibration.

Each instrument offers the highest performance available in its class. The 8506A measures ac voltages with a 24 hour accuracy of 120 ppm from 40 Hz to 20 kHz, while the 5440A supplies bipolar output voltages to 4 ppm! Add to this their straight-forward, micro-

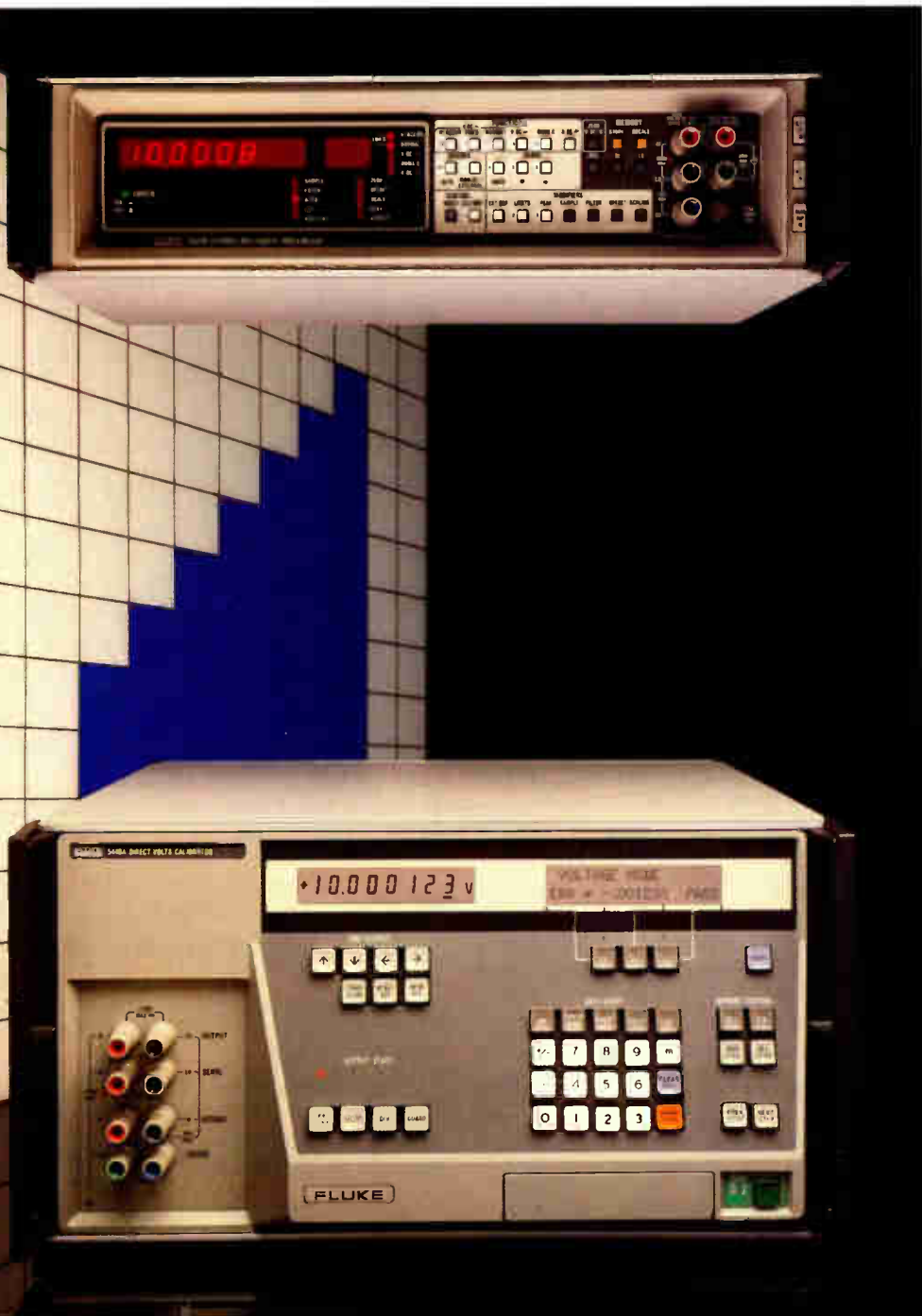
processor aided operation, and you can easily integrate a 5440A and 8506A into your measurement system. As a result, your traditional measurements can be made with reduced effort in less time!

System capabilities.

High performance on the bench is not all that this Calibrator and DMM offer. Complete remote programming and data output is available via the IEEE-488 bus. Adding the new Fluke 1722A Instrument Controller puts a complete measurement system at your fingertips! Performing closed-loop calibration and accuracy enhancement of DMMs, sources, or other products is a snap!

Find out more.

Why settle for anything less? Find out how easily the 5440A and the 8506A can enhance any of your calibration or measurement tasks. For more information call us at 800-426-0361, or contact your local Fluke Sales Engineer or Representative.

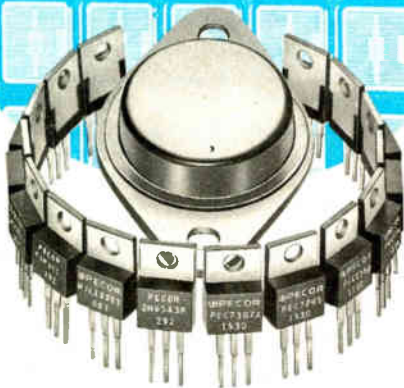


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Meetings

9th European Conference on Optical Communication, IEEE *et al.* (A. Solberger, Institute for Applied Physics, Swiss Federal Institute of Technology, 8093 Zurich, Switzerland), International Conference Center, Geneva, Oct. 23-26.

3rd International Packaging Conference, International Electronics Packaging Society (P. O. Box 333, Glen Ellyn, Ill. 60137), Hamilton Hotel, Itasca, Ill., Oct. 24-26.

National Communications Forum/National Electronics Conference, National Engineering Consortium (Robert M. Jonowiak, NCF, 505 N. Lake Shore Dr., Suite 4808, Chicago, Ill. 60611), Marriott Oak Brook Hotel, Oak Brook, Ill., Oct. 24-26.

ACM '83 Conference, Association for Computing Machinery (11 West 42nd St., New York, N. Y. 10036), Sheraton Centre Hotel, New York, N. Y., Oct. 24-26.

Computers in Aerospace Conference IV, American Institute of Aeronautics and Astronautics (Suzanne W. Lore, AIAA, P. O. Box 5837, Mail Point 170, Orlando, Fla. 32855), Hartford, Conn., Oct. 24-26.

Electromagnetic Compatibility Symposium, IEEE (A. H. Sullivan Jr., 7121 Wolfree Lane, Rockville, Md. 20852), Shoreham Hotel, Washington, D. C., Oct. 24-26.

Gallium Arsenide IC Symposium, IEEE (Thomas M. Reeder, Tektronix Inc., M. S. 50-370, Box 500, Beaverton, Ore. 97077), Ramada Towne House, Phoenix, Ariz., Oct. 25-27.

Seminar on Frequency Measurements and Calibrations, National Bureau of Standards (S. Howe, 1-4032, NBS, Boulder, Colo. 80303), National Bureau of Standards, Boulder, Oct. 25-27.

Broadcast Equipment Exhibition in Japan, Japan Electronics Show Association (3-23-5 Nishi Shinbashi ku, Tokyo 105), Tokyo Ryutsu Center, Tokyo, Oct. 25-27.

Semicon/Southwest '83, Semiconductor Equipment and Materials Institute (SEMI, 625 Ellis St., Suite 212, Mountain View, Calif. 94043), Market Hall, Dallas, Texas, Oct. 26-27.

4th World Telecommunication Exhibition, International Telecommunications Union (John S. Ryan, AT&T Bell Laboratories, Room 2C-620, Corner Road, Holmdel, N. J. 07333), Nouveau Palais des Expositions, Geneva, Switzerland, Oct. 26-Nov. 1.

Apple Fest, National Computer Shows (822 Boylston St., Chestnut Hill, Mass. 02167), Moscone Center, San Francisco, Calif., Oct. 28-30.

Milcom '83—Military Communications Conference, IEEE (Lynn Jeunette, Box 3273, Mclean, Va. 22103), Hyatt Regency—Capital City Hotel, Arlington, Va., Oct. 31-Nov. 2.

International Technical Symposium, International Society for Hybrid Microelectronics (P. O. Box 3255, Montgomery, Ala. 36109), Civic Center, Philadelphia, Pa., Oct. 31-Nov. 2.

Ultrasonics Symposium, IEEE (Prof. Levy, University of Wisconsin, Physics Department, Milwaukee, Wis. 53201), Marriott Hotel, Atlanta, Ga., Oct. 31-Nov. 2.

5th Digital Avionics Systems Conference, IEEE *et al.* (Cary R. Spitzer, MS 472, NASA, Langley Research Center, Hampton, Va. 23665), Sheraton Hotel, Seattle, Wash., Oct. 31-Nov. 3.

International Conference on Computer Design/VLSI in Computers, IEEE (Harold W. Carter, 24 Long Street Lane, Wright-Patterson Air Force Base, Ohio 45433), Rye Town Hilton, Port Chester, N. Y., Oct. 31-Nov. 3.

The 9th Annual Satellite Communications Symposium, Scientific-Atlanta Inc. (Betsy Crawley, 3845 Pleasantdale Rd., Atlanta, Ga. 30340), Hyatt Regency—Atlanta Hotel, Atlanta, Nov. 7-9.



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The most powerful product the M68000 Family just

THE NEW HD5-400



development system for became the most flexible.

Motorola's HDS-400™ Hardware/Software Development Station now allows real-time emulation of three M68000 Family microprocessors, and operates under four host/operating system configurations. Many more users can now apply the demonstrated development efficiencies of the high-performance HDS-400 to a broader range of products.

Four host/operating system configurations.

The HDS-400 Control Station introduced last year operates with Motorola's EXORmacs® host over an RS-422 serial link. It's joined now by the new M68KHDS400A Control Station with an RS-232C serial link for interface to either Motorola's VME/10™ or a DEC VAX™ host. Both the EXORmacs and VME/10 hosts operate under the VERSAdos™ operating system. The VAX host can operate under either VMS™ or UNIX™.

Choose your host: EXORmacs for multi-user support; VME/10 for integrated host/terminal operation; VAX, with either VMS or UNIX to let you utilize your current system. With any of these hosts or operating systems, the HDS-400 provides a complete development system for the M68000 Family of microprocessors.

Three emulator modules.

Three interchangeable emulator modules are now available to operate with any of the four HDS-400/host/operating system configurations. In addition to the 16-bit MC68000 Emulator, modules for real-time emulation of the 8-bit MC68008 and the 16-bit Virtual-Memory MC68010 are also available. It's the **only** development system that supports all three — the perfect match of a high-performance development system with the M68000 Family of high-performance microprocessors.

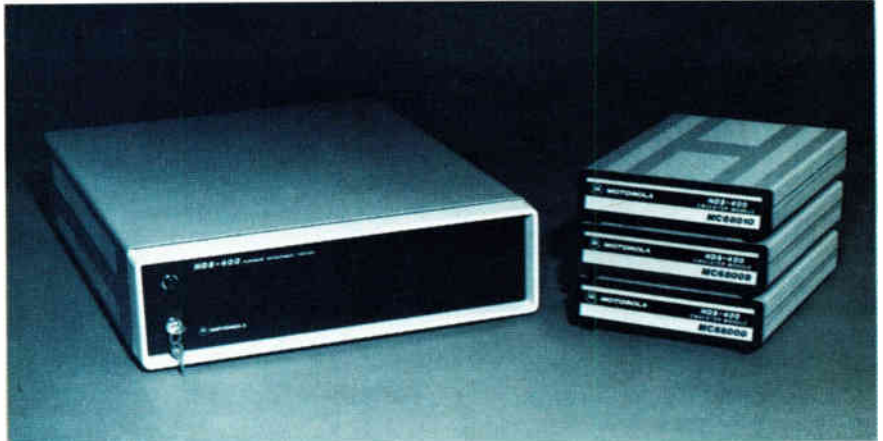
You choose the HDS-400 Development Station with complete confidence that you have full compatibility for your growth path throughout the M68000 Family, including upgrade to the 32-bit MC68020 in 1984. If you're already designing with the M68000 Family, the HDS-400 is the ideal complement: compatibility and growth path are powerful reasons to choose the M68000 Family for future product development.

Optional BSA enhances functionality.

Each HDS-400 emulator supports up to 16 target program breakpoints, within four address ranges, in either RAM or ROM. Optional incorporation of the Real-Time Bus State Analyzer (BSA) significantly enhances system functionality. The BSA provides

MC68000, the MC68008, the MC68010 or all three, the HDS-400 is the perfect complement. That's compatibility.

Now you can support this powerful development station from either of two Motorola hosts or from your VAX host with either of two operating systems. That's flexibility.



additional complex event breakpoints which can be specified by up to seven events from 79 qualifier lines. It also adds a sequential trigger mode, a window trigger mode, and performance histograms — powerful debugging and monitoring utilities.

Compatibility plus flexibility.

You can do hardware development and software debugging on the same HDS-400 Development Station. The system helps simplify and shorten your product development cycle, and reduce your development costs. It helps you put a better product on the market faster.

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Gould Logic Analyzers

16 Trace Control™ levels store widely-separated segments of program flow.

Imagine a logic analyzer sophisticated enough to sort through countless megabytes of program flow and store just the occurrences that caused a particular system failure.

One that wouldn't limit you to capturing a single, contiguous segment of your program activity, but would store relevant slices separated by minutes or even hours. In a single recording.

Think of the time and frustration you'd save tracking down hardware and software relationships in your system design with such a powerful instrument. That instrument is the K101-D (48-channel) or K102-D (32-channel) logic analyzer.

Now, with the Trace Control capabilities of these Gould logic analyzers, you can find solutions to problems you couldn't solve any other way. In applications ranging from 8- and 16-bit microprocessor systems to a multi-user, multi-tasking mainframe or

communications environment.

The K101-D and K102-D feature 16 separate conditional Trace Control levels, each with four powerful conditional commands. Each command is executed based on the occurrence of words and/or delay conditions, which are different for each trace level. So you can define precisely the windows or areas in your software execution where you want to concentrate your efforts. You minimize gathering of unnecessary data. And determine what *caused* the failure, not just where the failure occurred.

Capture multiple subroutines in a single pass.

With Trace Control, you can record the execution and timing of many different subroutines in a single pass, without tracing or timing the execution sequences in between.

For example, in a numerically controlled mill, A is a port-reading subroutine for measuring a motor's position during the calibration cycle. B is the arithmetic subroutine that calculates the required calibration

change. C outputs the new motor position, and D displays and prints the adjustment. The time between each subroutine is substantial but the data is irrelevant.

With Trace Control, you can record from the entry point of each routine to its exit point, without losing the initial information or wading through the unwanted data between the subroutines of interest. Up to 512 samples in each recording can be allocated as you choose, for truly flexible data capture.

... [A] ... [B] ... [C] ... [D] ...

Find unknown execution errors in real time.

The K101-D or K102-D continuously monitors system execution, in real time, and displays a trace level status message. When a problem occurs, you can often identify the faulty sequence area immediately, just by reading the trace level status.

This allows you to dynamically

Circle 30 for further information on the K101D

Circle 31 for further information on the K102D

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test multiple execution points, narrow down the problem area and simplify your debugging job.

8- and 16-bit disassemblers speed software debugging.

It's a lot easier to debug software when you can get your system's microprocessor to speak assembly language mnemonics rather than object code. Our disassemblers for the 68000, 8086, 8088, 8080, 8085 and Z80B do just that.

And they even set up the analyzer format and clocking for you. So you can devote your valuable time to analysis rather than set-up.

To save you yet more time, the K101-D and K102-D feature convenient DIP clips, which allow you to hook up directly to the microprocessor.

Uncompromising dedication to high performance.

The Gould philosophy dictates that every instrument we make be clearly the best.

The impressive Trace Control capabilities of the K101-D and K102-D are evidence of that commitment to excellence.

For detailed application notes or a demonstration, write Gould, Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279.

For fastest response, call toll-free: Nationwide (800) 538-9320; In California (800) 662-9231 or (408) 988-6800.

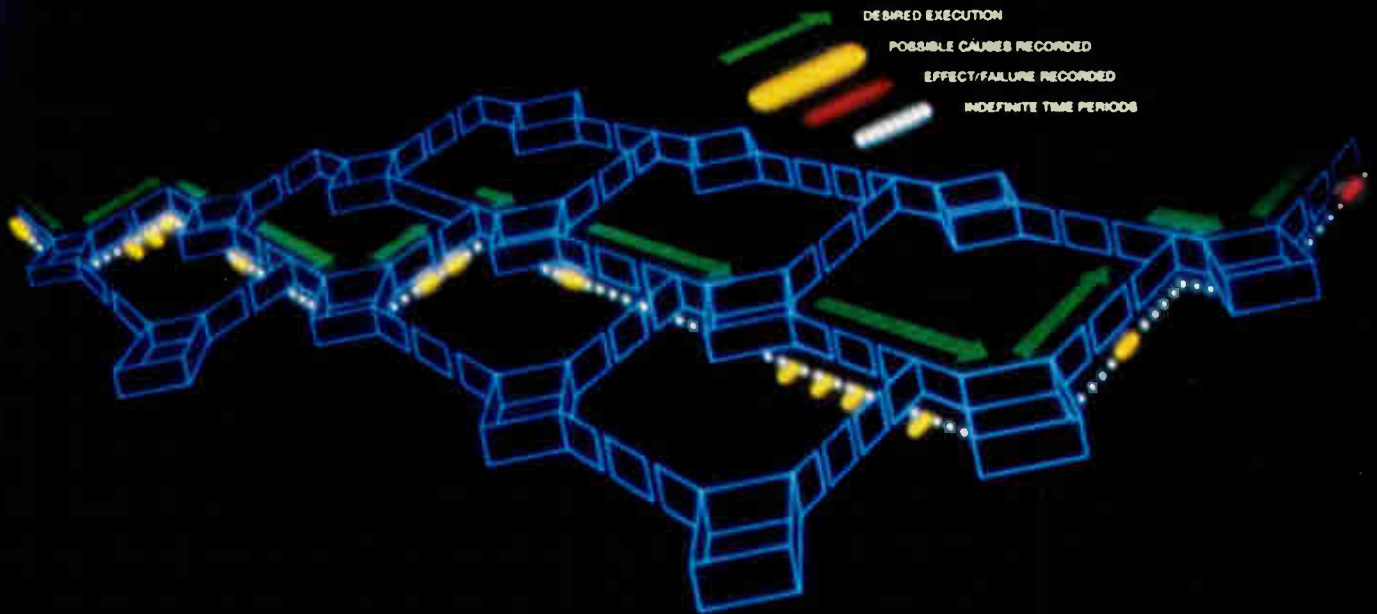
*Trace Control is a trademark of Gould, Inc., Design & Test Systems Division.

AND NOW...
68000 DISASSEMBLY.



How to find the ticking time bomb.

In the diagram below, the failure indicated in red occurs intermittently and only when the execution route in green is taken. Yet the actual cause may be hundreds or thousands of megabytes back in time. Such "time bombs" can be nearly impossible to isolate using a conventional logic analyzer. Trace control lets you capture and examine several possible "cause" areas in one compact recording, when the specified route is executed and the failure actually occurs.



TOTAL TRACE TIME = 10.5µS
C= 2 R=514 (R-C)=+514(10.28µS) CL=0 LEVEL=0 RDY

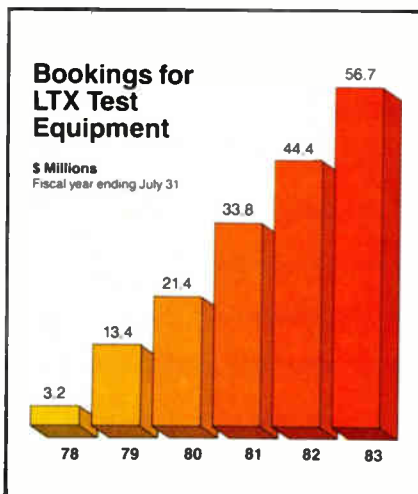
 **GOULD**
Electronics & Electrical Products

Test market update

LTX Record Bookings result as industry leaders turn on production

It was inevitable. "Solving tough test problems has always been our philosophy. We have to increase our efforts in this area to keep up with the fast pace of the semiconductor industry. We expect a super return, in the form of multiple sales, once these new circuits go into mass production." (Graham Miller, Electronic Business, March, 1983)

Unit sales of LTX Test Systems a year ago enabled LTX's well established customer base to develop productive test techniques for new devices. 1983 saw the beginning of a dramatic increase in multi-unit sales as those same customers moved into production of these new devices. Currently, 18 of the top 20 integrated circuit manufacturers rely on LTX to provide test support for the new device production.



Graham Miller believes that LTX's dominant market share will continue to increase during the industry upturn. In addition to the production expansion of the major integrated circuit manufacturers, LTX is presently adding ten new customers each quarter. Further, the LTX installed base of \$160 million will generate a significant market for expanded system capability with the introduction of new, back-fittable system options.

How can LTX continue at this pace? Just take a look at some of the new product offerings in the last six months alone. The new TS 88 Test Station offers more testing power at lower cost per socket with plenty of room for the addition of new, retrofit capabilities. The PMC 2000, an innovative ATE networking concept, uses a powerful 32-bit computer and industry standard Ethernet™ LAN for rapid data transfer and global communications.

LTX's aggressive product development (16% of revenue) and the potential of their joint venture with Trillium Corporation means semiconductor manufacturers and users can expect that LTX will continue to respond to their growing needs.

It's becoming easier to believe that LTX will achieve their stated goal of becoming the largest STE manufacturer within this decade

— Joseph Toomey

News update

■ When a major mainframe maker introduces a new machine, upward migrations are almost sure to follow. But the enhancement that Control Data Corp. has worked up for the Cyber 170 series 800, introduced 18 months ago [*Electronics*, May 5, 1982, p. 40], is unusual. The add-on Cyberplus system, which the Minneapolis firm unveiled this month, can propel the series 800 into the supercomputer class or beyond for certain scalar operations.

Cyberplus is actually a version of the multiple-parallel-processor Advanced Flexible Processor offered by CDC's Government Systems division since 1976 [*Electronics*, June 2, 1982, p. 207]. By developing a commercial version that allows 1 to 64 processors to be attached to a series 800, CDC says it can offer users a way to move incrementally toward supercomputer performance at less than the typical \$4 million to \$11 million supercomputer price.

A single Cyberplus processor runs anywhere from \$750,000 to \$1.6 million. CDC expects most buyers will start with one or two processors, adding more as their needs and budget dictate. A system using eight Cyberplus processors would sell for \$5 million to \$7 million, not counting the series 800 host, whose prices start at \$195,000.

Speedster. Cyberplus processors are not capable of the vector-processing jobs performed by general-purpose supercomputers such as CDC's Cyber 205. But the firm expects Cyberplus's high-speed scalar capability to be useful in such computation-intensive tasks as simulation, petroleum exploration, and image or signal processing. Each added processor is capable of speeds exceeding 100 million 32-bit floating point operations per second (65 megaflops in 64-bit mode). With eight such processors running in parallel, a series 800 could equal the 800-megaflop (32-bit) rating of a Cyber 205. A maximum Cyberplus system linking 64 processors to a single host would push the computational capability well beyond the capacity of any currently available system, CDC says.

—Wesley R. Iversen

"AFTER MONTHS OF EVALUATION, OUR RESULTS SAID 'BUY LTX.' BUT IT WAS OUR CUSTOMERS WHO REALLY SOLD US."

Frank F.E. Owen, Telecom Manager,
European Semiconductor Group, Texas Instruments, France



"Texas Instruments is dedicated to producing high quality devices, which means we need equally high quality test equipment.

"We analyzed systems from all the major manufacturers, comparing such items as reliability, cost-per-test, efficiency and applications support.

"But the real test came when we talked to our customers. Our goal was to have a high degree of testing correlation, and we found that almost all of our customers were using LTX."

European users have found the flexibility and speed of LTX equipment to be major advantages. In the case of Texas Instruments, correlations with customers came in a matter of weeks, not months. LTX's automatic system calibration at the socket enables users to calibrate from one system to another quickly and accurately.

"Our newest achievement at TI is the V23, a bug-free modem of the highest quality. And it's LTX test equipment that helps us make it that way."

LTX Corporation
LTX Park at
University Avenue
Westwood, MA 02090

Call us at:
Boston: 617/329-7550
Santa Clara: 408/727-1212
Europe: 44 4862 22322
Japan: 03-342-1481

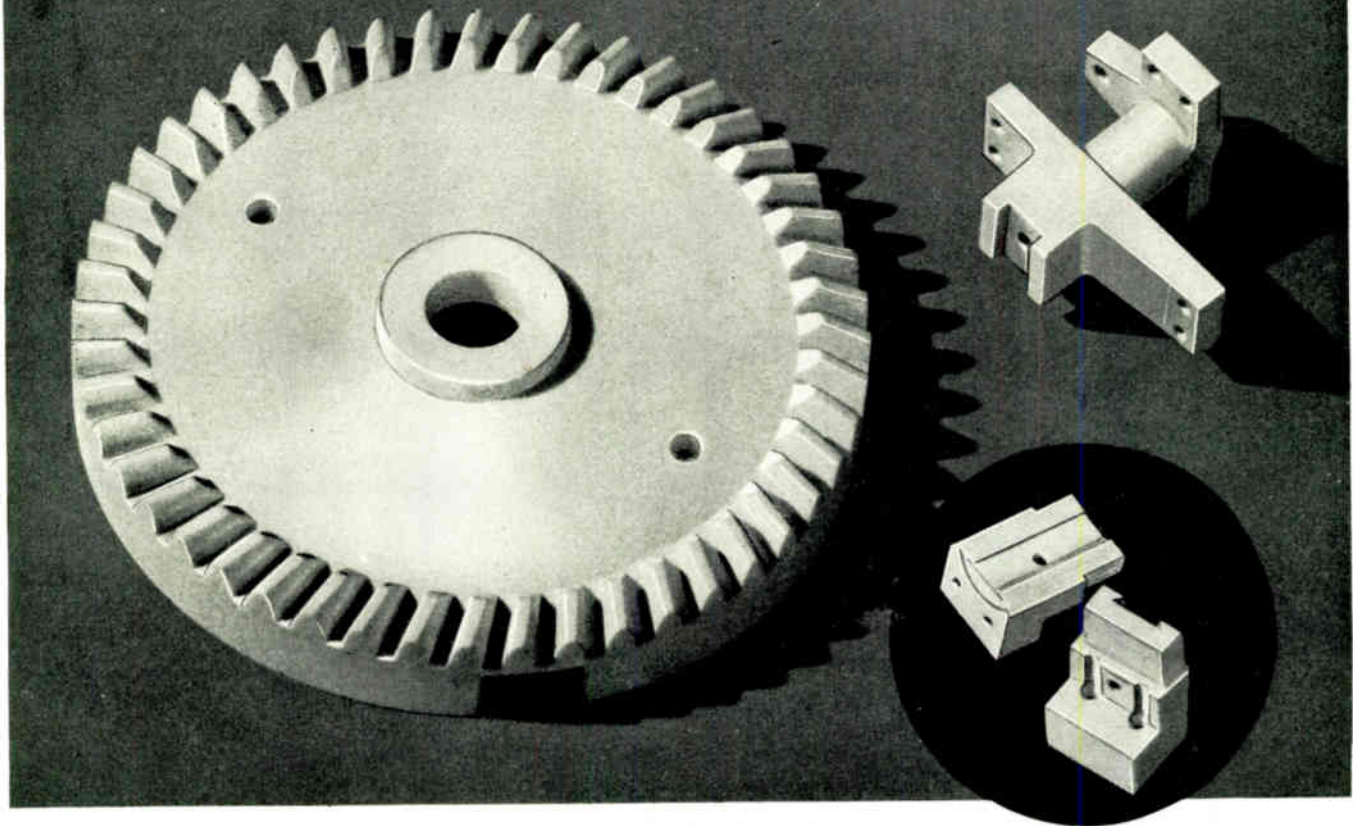
Or see us at:
1983 International Test Conference
Salon 6
October 18, 19, 20

"The LTX equipment is able to handle such a wide range of devices, we can respond rapidly to changing telecom applications and bring new products on line faster than ever before."

LTX RESPONDS

Circle 33 on reader service card

INTRICATE CERAMIC PARTS PRODUCED WITHOUT SPECIAL TOOLS



WHEN special ceramic parts are required in small quantities for vital wartime applications, the adaptability of Isolantite* to the production of intricate shapes is a feature of major importance.

Through years of experience in the manufacture of steatite ceramics, Isolantite Inc. has developed fabricating techniques that permit the production of intricate shapes without the necessity of providing expensive special tools. In addition, Isolantite's manufacturing processes permit extremely close dimensional tolerances as compared with general ceramic requirements. Critical dimensions can be held within close limits to facilitate equipment assembly.

Suitability for the production of intricate shapes to accurate dimensions is only one of Isolantite's many advantages. Uniformity of product, high mechani-

cal strength, electrical efficiency, nonabsorption of moisture—these factors all contribute to dependable insulation performance. Because of its unique combination of properties in a single ceramic body, Isolantite is the choice of leading manufacturers, not only in the high-frequency fields, but for all applications where high-grade insulation is required in intricate shapes.

ISOLANTITE

CERAMIC INSULATORS

ISOLANTITE INC., BELLEVILLE, NEW JERSEY

*Registered trade-name for the products of Isolantite Inc.

THE AMD WORLD-CHIP™



THE FIRST AND ONLY MONOLITHIC MODEM CHIP THAT MEETS BELL & CCITT STANDARDS.

Schweber Stocks AMD's FSK Modem WORLD-CHIP.™

AMD's new Am7910, the first complete asynchronous Frequency Shift Keying modem ever offered on a single LSI chip, is now available from Schweber.

The AM7910 gives you the biggest advantage of space age technology—more space. Designed to be used in equipment all over the world, it can be switched to any of 9 variations* of Bell or CCITT standards without any additional circuitry or modifications.

Now you can forget about external filters, hybrids and tuned circuits. All the

features a modem should have are built right into the chip. Filters, handshake signals, auto-answer and local loopback are already there—taking up less space than ever before.

And the Am7910 leaves no room for aging or drift. It uses digital signal processing techniques to perform all major functions. It's perfectly predictable and inherently stable without regard to time or temperature.

The Am7910 offers you all the performance capabilities of a standard high performance modem, but takes up about half the budget requirements. So if you're interested, call Schweber today and let us help you win the space race in telecommunications.

Schweber's New Low Prices:

AM7910DC	100-999	10-99	1-9
Price	\$58.00 \$28.00	\$72.00 \$35.00	\$96.00 \$40.00

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 Irvine, CA: 714/863-0200, 213/537-4321

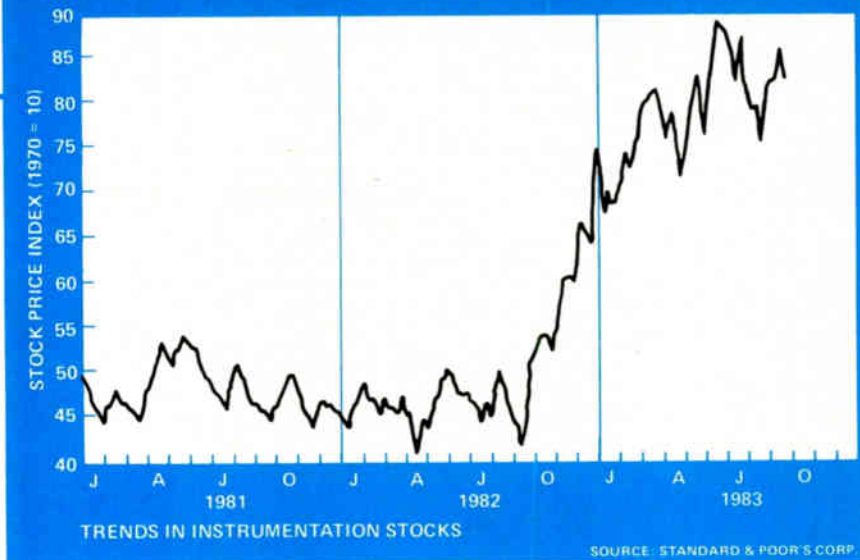
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*Bell 103, 202 and CCITT V 21, V 23 World-Chip is a trademark of Advanced Micro Devices.



Business activity

“Trends in instrumentation stocks” records the stock market activity of a selected group of publicly owned manufacturers of test, measurement, and analytical instrumentation. The index weights the companies by size and therefore reflects their relative performances.



The increasing demand for microcomputer software—from both users and suppliers seeking to diversify—has led to a bigger business in mergers and acquisitions in the computer services industry in the first half of 1983, says the sector's main trade group. The Association of Data Processing Service Organizations (Adapso) says its index of merger and acquisition activity shows 60 takeovers of businesses that perform data transactions with some value-added software services, provide software consulting, or write software. The pace is about that of 1982's first half—61 transactions—but the value has more than doubled—a 1983 first-half collective value of \$409 million in cash and stock, compared to 1982's \$201 million.

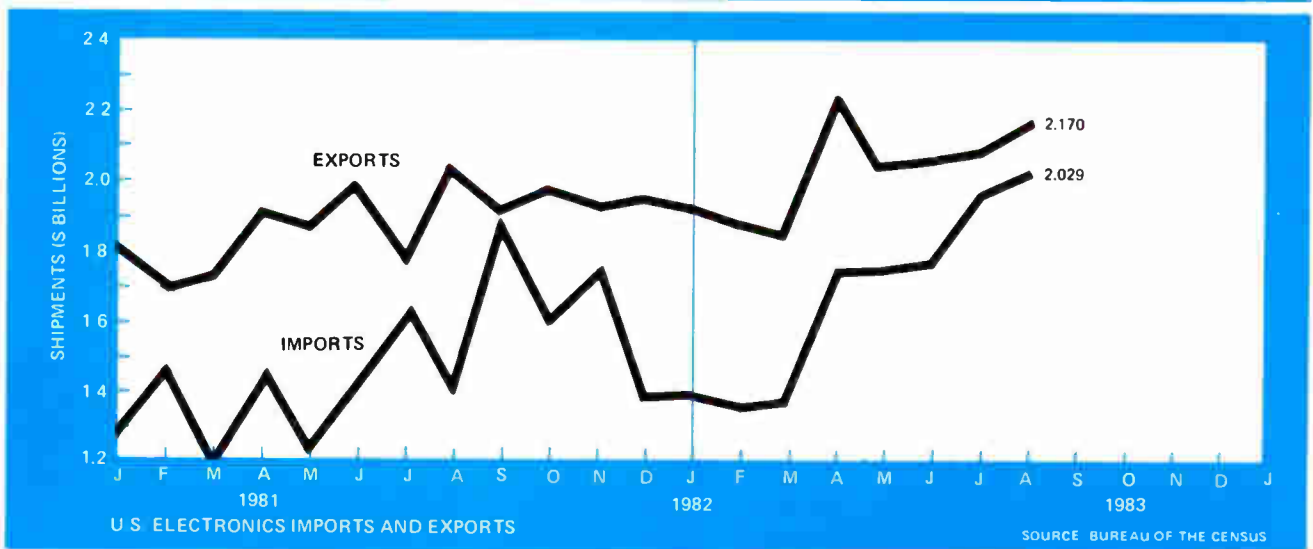
“A hot stock market and relatively low interest rates have combined to fuel an already active interest by leading companies hungry for growth by acquisition,” notes Bernard Goldstein, a partner in *Broadview Associates*, a Fort Lee, N. J., consulting firm that produces the index with Adapso. He notes the pace so far in 1983 is reversing the 1981–82 dropoff in per-transaction value, at \$6.8 million per transaction. In 1981, the Adapso index recorded a per-transaction value of \$6.5 million (118 transactions worth \$766 million); and in 1980, \$7.9 million (87 transactions worth \$688 million).

“There is increasing interest in software for microcomputers,” Goldstein says, “and for buyers [of software companies], mergers and acquisitions provide one of the best methods of entry and growth.” Established suppliers of software for mainframe computers are moving downscale into this market and are coming face to face with publishers and other manufacturers hunting for opportunities, Goldstein adds. Among the transactions involving microcomputer-software vendors: *ASK Computer Systems* purchased *Software Dimensions Inc.*, *Computer Associates International* acquired *Information Unlimited Software*, and *McGraw-Hill Inc.* acquired *Aardvark Software Inc.* In addition, *Wyly Corp.* plans to acquire *Open Systems*, a developer of application software.

Financings . . . Retail computer store operator *Businessland Inc.*, in San Jose, Calif., arranged a \$25 million line of credit from Bank of America. *Businessland*, which operates 13 centers, primarily in California, will use the funds for further expansion around the U. S. . . . *Microcom Inc.*, Norwood, Mass., raised \$3.75 million in its third round of venture-capital financing. The company develops and markets data-communications hardware and software.

—Robert J. Kozma

Business activity



U.S. ELECTRONICS IMPORTS AND EXPORTS¹ (MILLIONS OF DOLLARS)

	IMPORTS			EXPORTS		
	July 1983	June 1983	July 1982	July 1983	June 1983	July 1982
Accounting, computing, and data-processing machines	195.194	186.879	64.451	441.637	477.048	400.761
Calculators	34.808	31.895	24.231	6.822	6.877	12.440
Parts for data-processing machines and office calculators	245.484	269.712	125.403	448.329	424.492	315.895
Telecommunications, sound-recording, and sound-reproducing equipment	945.404	898.868	655.571	357.168	289.941	397.292
Electronic or electric instruments	88.078	78.968	85.130	498.889	473.177	513.378
Printed-circuit boards	11.220	15.825	22.272	14.602	14.779	10.865
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	519.095	461.572	415.170	390.232	398.586	315.880
Fixed and variable resistors	20.573	17.097	13.720	12.582	11.821	11.993

U.S. ELECTRONIC COMPONENTS PRODUCER PRICE INDEX² (1967 = 100)

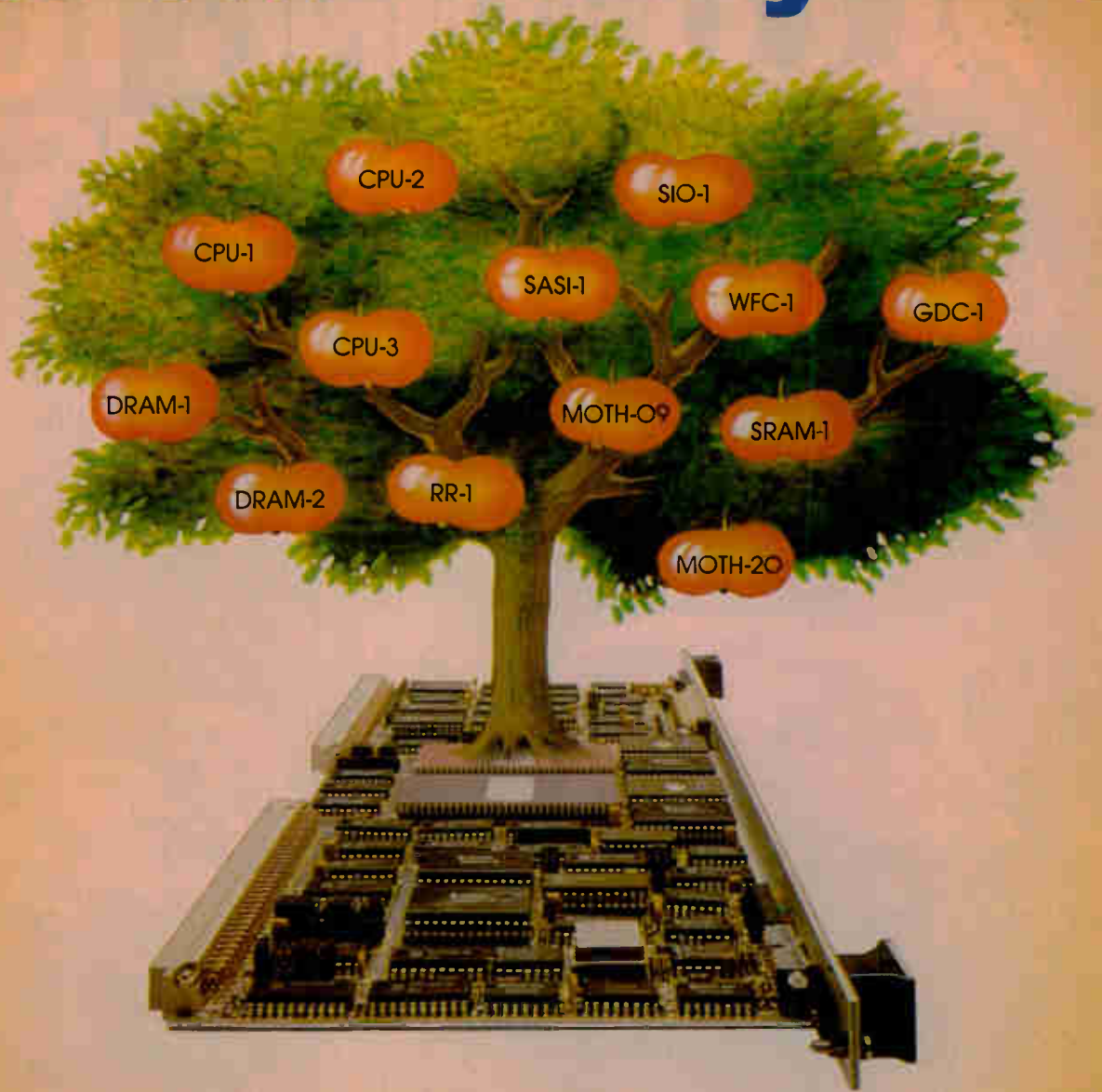
	August 1983	July 1983	August 1982
Digital bipolar integrated circuits	64.3	62.6	48.7
Digital MOS ICs	40.5	40.3	44.8
Linear ICs	63.0	62.8	57.7
Capacitors	193.4	191.1	195.7
Resistors	184.1	185.2	176.7
Relays	301.2	301.2	241.0
Connectors	222.4	222.1	218.4

GENERAL U.S. ECONOMIC INDICATORS

	August 1983	July 1983	August 1982
Average prime rate (%) ³	10.89	10.50	14.39
Retail sales (\$ billions) ⁴	97.602	98.953	89.069
Unemployment rate (%) ²	9.4	9.3	9.7

SOURCES: ¹Bureau of the Census ²Bureau of Labor Statistics ³Federal Reserve Board ⁴U.S. Department of Commerce

The VME Family Tree



SYS68K/CPU-1, 68000MPU
8 MHz (10 MHz) 128KB DRAM expandable to 512KB, RTC, 3xRS232. Price \$ 1450,- + Tax, available.

SYS68K/CPU-2, 68000MPU
8 MHz (10 MHz) 128 KB dual ported (512KB) DRAM, RS232 parallel I/O, slave bus arbitration. Price \$ 1795,- + Tax, available Oct 83.

SYS68K/CPU-3, 68000MPU
10 MHz optional, DMAC, MMU, bus arbitration. Price \$ 2200,- + Tax, available Dec. 83

SYS68K/DRAM-1/-2, 512KB/2MB
byte parity, write acc. 210 ns (max.), read acc. 320 ns (max.).

Price DRAM-1 \$ 1680,- + Tax
DRAM-2 \$ 5590,- + Tax, available.

SYS68K/SRAM-1, 128KB SRAM
expandable to 512KB, battery back-up. Price \$ 1600,- + Tax, available.

SYS68K/MOTH-09/20, 9/20
DIN 41612C Female connectors. Price MOTH-09 \$ 470,- + Tax
MOTH-20 \$ 980,- + Tax, available.

SYS68K/SASI-1, handling processor. DMA-controller for up to 4 MByte per sec. transfer rate and interrupt capability Floppy, Winchester, and Tape control via SASI Bus. Price \$ 1680,- + Tax, available.

SYS68K/SIO-1, 6 serial multi protocol channels RS232 and RS422 programmable Baud rate. Price \$ 985,- + Tax, available.

SYS68K/RR-1, 8 memory banks max. 512KB, mixed use of ROM's, EPROM's, PROM's or SRAM's, each bank separately jumperable, battery back-up. Price \$ 885,- + Tax, available.

SYS68K/WFC-1, up to 4 Flappy + 3 Winchester drives 5 1/4 inch, programmable sector size ECC diagnostics. Price \$ 1680,- + Tax, available Oct 83.

SYS68K/GDC-1, up to 16 colors, 256KB display memory, 1k x 1K

Pixels 512x512 Pixels display window, handling processor. Price \$ 2780,- + Tax, available Dec 83.

Available Software: Monitor Editor/68000 Ass., Basic-68K, Forth-68K, Realtime multitasking Nov 83, Multiuser operating system Dec 83.

All CPU boards are prepared to run UNIX* and CPM68K**
*UNIX is a trademark of Bell Labs
**CPM68K is a trademark of Digital Research

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Tlx 172465



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Since we first entered the Winchester market two years ago, we've accomplished many things our competition claimed were impossible.

It was impossible, they said, for a floppy disk company to make a significant dent in the highly competitive Winchester market.

We've not only made a dent, we're the second-largest company in the business, and we have the capacity in place to be first.

It was impossible to expand our production capacity from 0 to 60,000 drives a month practically overnight. But we did it.

It was impossible to sell Winchesters at

such a low cost. But last year our 500 series drives were introduced at under \$500, 30% under then-standard industry costs. And since then, we've led the industry to ever-lower costs on full and half-height drives.

It was impossible to produce and ship high-performance plated media drives in high volume at prices lower than most vendors are charging for oxide media drives. One of our competitors backed away from plated media because they couldn't buy enough of it to build drives in efficient quantities.

We solved that problem by building our

OUR COMPETITION, POSSIBLE.



own plated media factory dedicated to plated media production in high volume. Because we make our own, our costs are low and we are independent of outside vendors for supply.

It was impossible for a start-up company to produce and ship a broad line of products: full and half-height drives, open and closed-loop, from 6.4 to 50 MB. But we've done it. With the help of one of the industry's best-funded R&D programs. And with our steady supply of plated media, we will soon be offering 5¼" drives that push Winchester technology to the limits of its

capacity. In high volume. At prices that are pure Tandon.

Impossible?

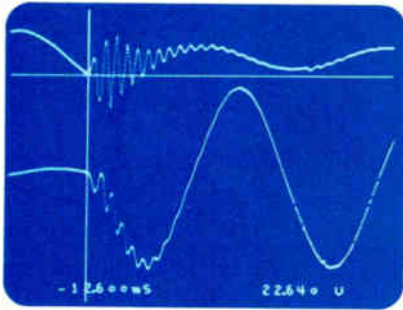
For our competition, yes.

But not for the Tandon Winchester Company.

TANDON WINCHESTER COMPANY.

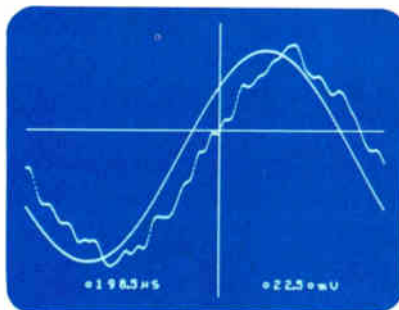
Tandon
**THE MOST SUCCESSFUL DRIVE
COMPANIES YOU EVER HEARD OF.**

Compare.



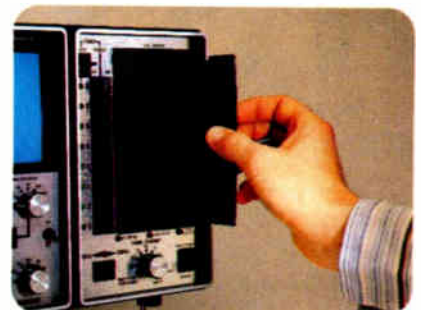
Realtime Monitoring and Storage.

Nicolet Oscilloscopes can monitor, capture, and store signals with both pre- and post-trigger information.



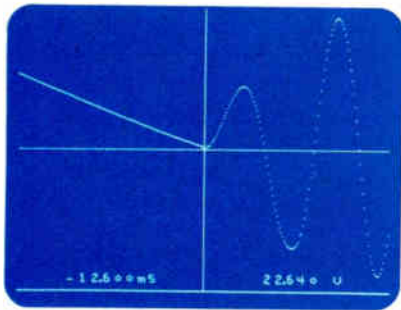
Waveform Comparison.

Nicolet Oscilloscopes can display a live or stored signal with a previously stored reference or a second signal.



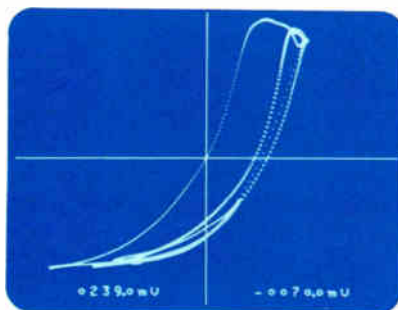
Permanent Storage and Hardcopy Records.

Nicolet Oscilloscopes can store waveforms permanently on a built-in floppy disk for later recall and/or output to an external plotter.



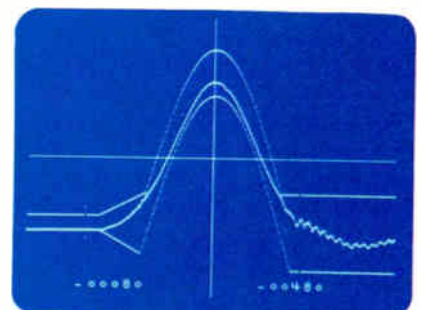
Expansion, Resolution and Accuracy.

Nicolet Oscilloscopes can expand any selected feature up to X256 with resolution up to 0.002% and accuracy as high as 0.2%.



X/Y Display.

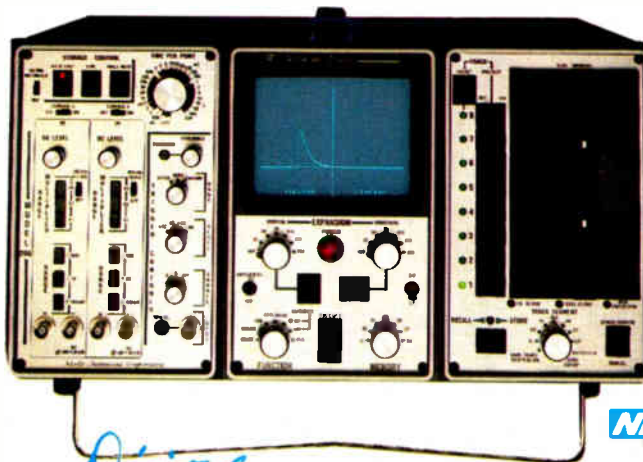
Nicolet Oscilloscopes can display a waveform as a function of another, either in live or stored mode.



Digital Interfaces.

Nicolet Oscilloscopes can interact with computers or calculators. (In this case, comparing a live waveform to computer-drawn limits.)

Compare these features with any other oscilloscope. The choice should be obvious.



For more information on the 2090 Series or the more powerful 4094, call 608/273-5008. Or write Nicolet Oscilloscope Division, 5225 Verona Road, Madison, Wisconsin 53711.

 Nicolet

Nicolet Oscilloscopes

Most personal computers violate its patents, says TI

Now that a settlement has been reached with Houston-based Compaq Computer Corp., Texas Instruments Inc. says it will seek to enforce three U. S. patents that it believes a large percentage of personal-computer and microprocessor manufacturers are violating. TI patent lawyers are preparing attempts to make others honor the patents, based on the company's pioneering work in single-chip calculators and large-scale scientific computers during the late 1960s and early 1970s. Two patents deal with what are called bit-pusher techniques; to cut processing time, they use a single instruction to directly address 1 bit in a communications register that then controls a peripheral device. The third patent covers the combination of a manual input device—such as keyboards—a single-chip microcomputer, and a display. **“By our analysis, this covers a very large percentage of the personal computers,”** says TI patent-attorney James Comfort, adding that the firm already has licensing agreements with a number of manufacturers. The bit-pusher is also patented in Japan, he adds, while the input-display scheme has patents pending in a number of countries. Meanwhile, Compaq—founded in 1982 by three former employees—has agreed to license the technology for its portable personal computer.

Honeywell hardware links computers in factories, offices . . .

Honeywell Inc. was one of two companies to announce in Houston last week, at Instrument Society of America show, systems that link factory-floor computer networks with the automated office. The firm's TDC 3000 process-management system provides a bridge between its process-connected TDC 2000 Data Hiways and its DPS 6 32-bit minicomputer for management-information markets. **The TDC 3000 is centered on a token-passing ring network** that distributes primary-system monitoring, optimization of control programs, and computing functions—all usually performed with a large computer. Made by Honeywell's Process Management Systems division in Phoenix, Ariz., a typical TDC 3000 system will start at \$100,000 and (with thousands of process control points) could cost more than \$10 million.

. . . Bailey Control plans a similar bridge

The other project, carried out by the Bailey Control division of Babcock & Wilcox Co., in Wickliffe, Ohio, involves a large-scale linkage of the company's Network 90 process-control system with office computers **using AT&T Information Systems' Dimension 85 private automated branch exchange.** Bailey Control plans to implement the system at its headquarters in the first quarter of 1984. The remote link will be made without a modem through Dimension 85's digital data interface, at speeds of 9.6 to 64 kb/s.

TI pushes 99/4A after dropping plans for 99/8

Now that it has decided against introducing any new home computers in 1983, Texas Instruments Inc. is once again putting big advertising dollars behind its 2½-year-old 99/4A unit to boost its visibility during the Christmas shopping season. The firm had planned to introduce a more powerful consumer model, the 99/8, **but uncertainty in the marketplace, heavy losses stemming from the fierce competition, and management changes have all but killed the new unit,** which was based on TI's 16-bit

microprocessor. Instead, Consumer Group officials are now studying ways to make any future models more compatible with TI's 16-bit Professional Computer, which, like IBM's Personal Computer, is based on an Intel 8088.

System houses, OEMs lead productivity list

Turnkey-system houses and original-equipment manufacturers produce \$134,552 of revenue per employee, making them the best performers among its members, says the just-released 1982-83 Operating Ratios Survey conducted by the Association of Data Processing Service Organizations. **That stacks up against \$106,296 for mainframe- and minicomputer-software firms, \$80,272 for companies that do remote data processing, \$78,131 for outfits that consult and perform custom programming, and \$53,424 for microcomputer-software firms.** Average equity-to-debt ratios range from 3.1 : 1 for companies selling processing services to a low of 1.0 : 1 for microcomputer-software firms, the range being due to the relative stability of the former and the relative youth of the latter, says Julia Johnson, Adapso director of research and statistics.

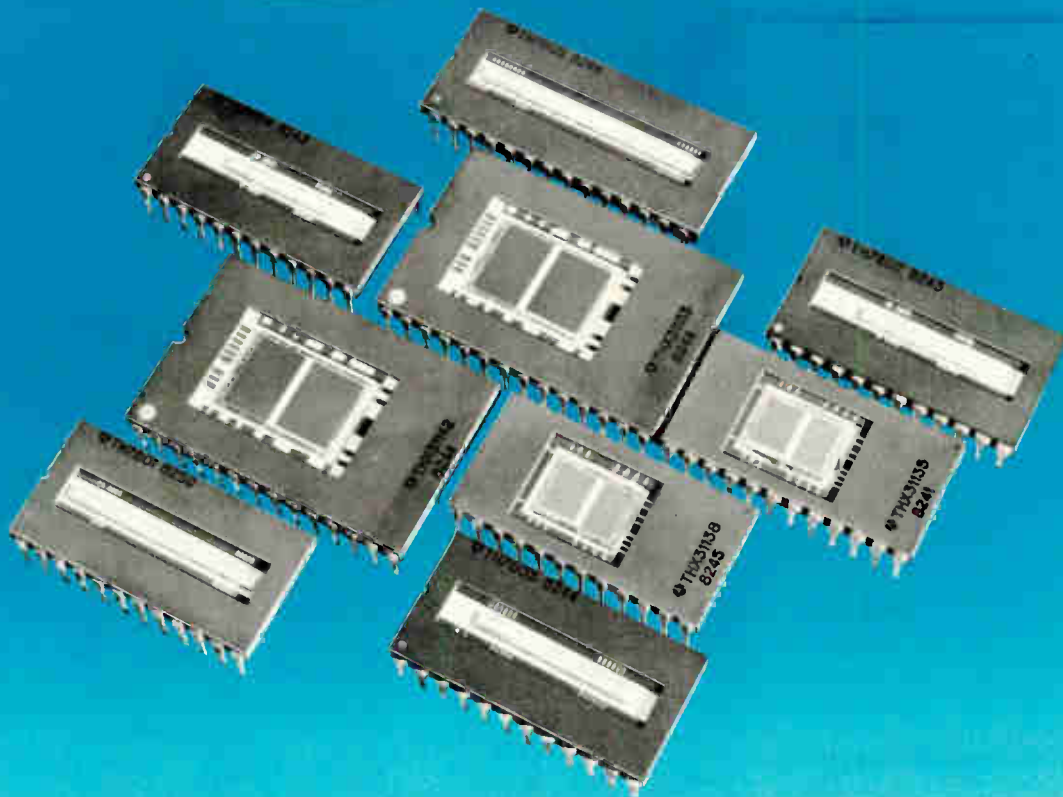
New VAX machine takes on microcomputers

The smallest member yet of Digital Equipment Corp.'s VAX supermini-computer line is about to bring its 32-bit muscle to applications currently targeted by 16-bit microcomputer systems. The Maynard, Mass., firm says it will start delivering the new machine, called MicroVAX, early next year. **Promising slightly superior performance to the low-end VAX-11/730 at only half the price,** the new MicroVAX I compresses the 32-bit-wide VAX data path onto a single custom chip (see p. 47). Enclosed in the same 21.5-by-27-by-6-in. package that houses DEC's Micro/PDP-11 microcomputer, a bare-bones MicroVAX I costs \$9,995. More capable configurations of the system, which supports up to four users and addresses a maximum of 4 megabytes of physical memory and 4 gigabytes of virtual memory, range up to about \$20,000. Compatible with its larger VAX brethren, the MicroVAX I runs either on a subset of the VAX/VMS operating system or on DEC's implementation of AT&T Bell Laboratories' Unix operating system; an additional package called VAXelan lets the new computer run real-time programs developed on higher-end VAX machines.

Shortages seen crimping production of IBM Peanut

Introduction of IBM Corp.'s Peanut home computer is considered imminent—one report says it will be called the PC Junior and sell for \$800 in its 64-K version—but industry observers are wondering if the Armonk, N. Y., industry kingpin will be able to meet an anticipated avalanche of demand. **Peripherals and components, especially floppy-disk drives, are in short supply,** they say. "They won't be able to meet demand for the Peanut," predicts Michele Preston, analyst at L. F. Rothschild, Unterberg, Tobin, the New York City investment firm. Nonetheless, she feels IBM should be able to sell 100,000 Peanuts in the waning months of 1983 alone, and to meet demand by the second half of 1984. Chris Christiansen, an analyst with Boston's Yankee Group, foresees sales of 75,000 to 100,000 of the Peanut by the end of this year.

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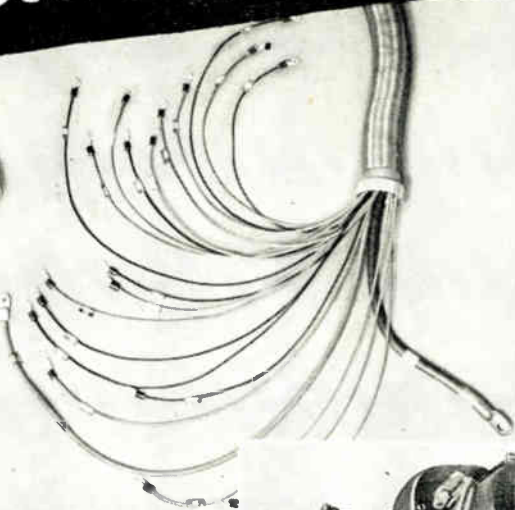
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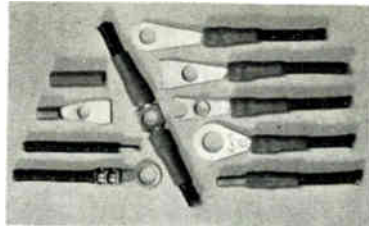
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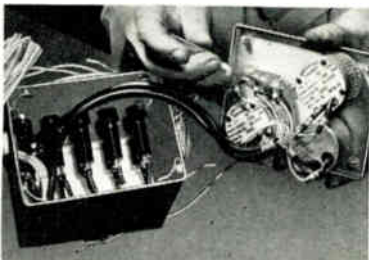


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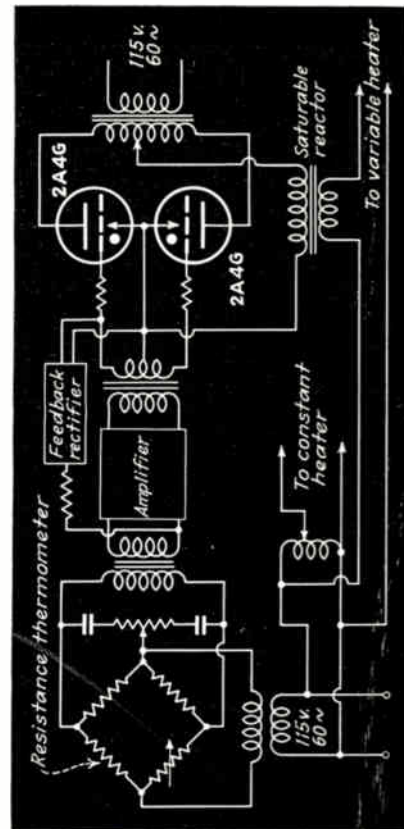
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desired point, the resistance thermometer changes in resistance by a very small amount and the balance of the Wheatstone bridge is upset. There is then a voltage across the output of the bridge and this is fed into the phase shifting network and the primary of a transformer. The voltage developed across the secondary of the transformer is now out of phase with the line voltage by an amount depending on the phase shifting network and it is fed through a two-stage amplifier. The output of the amplifier, even with temperature changes of a few thousandths of a degree in the chamber, is sufficient to operate the two 2A4G thyratrons. The amplified out-of-phase voltage is applied to the grids of the thyratrons and a voltage 180 degrees out of phase with line voltage (a step-up transformer is used) is applied to the anodes. The thyatron pass anode current whenever a very slight decrease in temperature in the chamber occurs. The anode current must be made to control the application of heat to the chamber. In this case, the anode current is

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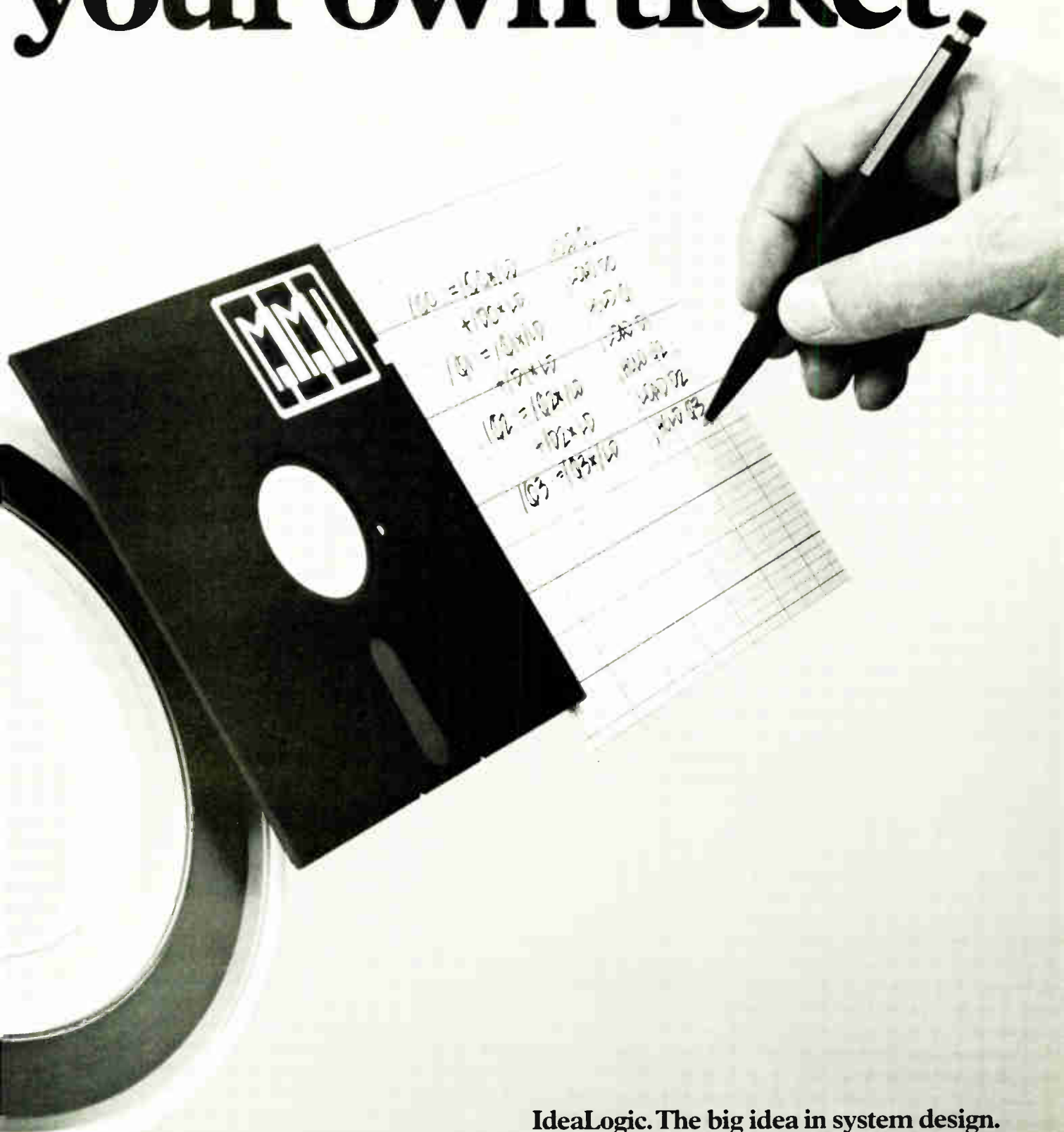
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Silicon compiler cuts time to market for DEC's MicroVAX I

by Stephen W. Fields, San Francisco regional bureau manager

A single chip carries all the processor's essentials; the journey from design to silicon took only seven months

Computer makers, with their marketplace and technology in ferment, can ill afford the three to four years usually required to design and introduce a new system. As much as anything else, time to market now determines whether or not a new computer will be a winner or an also-ran.

If time to market were the only factor, Digital Equipment Corp. would have a guaranteed winner in its MicroVAX I computer, unveiled this month. A custom chip, which carries nearly all of the computer's processing power, went from design to silicon in just seven months. The chip will let the Maynard, Mass., firm sell the new machine for \$10,000 to \$20,000, even though it outperforms the roughly twice as expensive VAX 11/730 minicomputer.

DEC put itself on a fast development track last fall by setting up an independent design group called DECwest to prepare a riposte to competitors introducing cut-rate VAX-like machines almost every month. The group, established in Bellevue, Wash., had "no charter except to come up with something soon," says Larry Copenrath, the group's hardware-engineering manager. "We had four goals in mind," he explains:

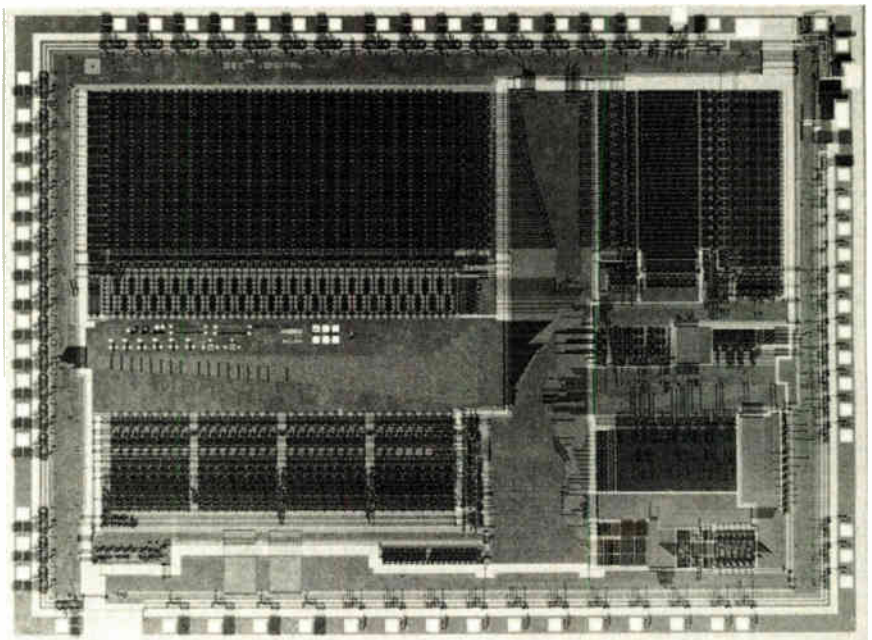
"high quality; schedule (a product by the fall of 1983); function (more than an 11/730); and cost (lower than the 11/730)." Silicon Compilers Inc., a two-year-old Los Gatos, Calif., firm, helped DEC meet its goals.

Right path. The key to developing a lower-cost, higher-performance machine was a decision to integrate the full 32-bit-wide data path—the arithmetic and logic unit, the timing and decoding circuits, the barrel shifter and stack, and 48 registers—onto a single chip. "When you look for things to shrink," says Copenrath, "you usually don't look at the data path [the central processing unit minus the microcode and the input/output control]; you usually look at the random control logic, like the microsequencer. But we felt that was much more risky because it's hard to get a good spec for the IC designer,

just because that stuff is so random."

DECwest had its product's hardware and software defined by January. To meet its schedule, the company had to find a semiconductor company willing and able to put the custom processor into production within seven months. Most semiconductor houses wanted two years for the project, and that did not much surprise Copenrath, since DEC's own semiconductor facility, in Hudson, Mass., has been working on a similar project for several years. He turned to Silicon Compilers, whose name defines its purpose: converting high-level functional descriptions of circuit elements into a form that controls mask-generating equipment.

Dennis Sabo, Silicon Compiler's vice president for marketing, explains that the company is "about six months away from introducing a



Data path. This 280-by-350-mil chip, readied in just seven months, implements a 32-bit data path that contains nearly all the essentials for a powerful host processor.

complete compiling system, but much of the work has been done; and to prove it out, we've taken on several custom designs, and they've all worked the first time out." The firm has also done an Ethernet controller chip for Seeq, best known for nonvolatile memories, and another IC it will not talk about.

The compiler software is not wholly complete, so some of the MicroVAX design had to be done by hand. This was not much of a problem, since Silicon Compiler's vice president for engineering, Edmund Cheng, helped design Intel's 80186 and 80286 32-bit processors. He says that the 11/730 uses fast bipolar 2901 bit-slice processors to achieve a 90-nanosecond cycle time. "We did the MicroVAX I processor in 3-micrometer n-MOS, which is slower—running at a clock rate of 8 megahertz, it has a cycle time of 250 ns," he explains. "But we do more in one cycle than the 11/730 does in three, so the end result is an increase in performance."

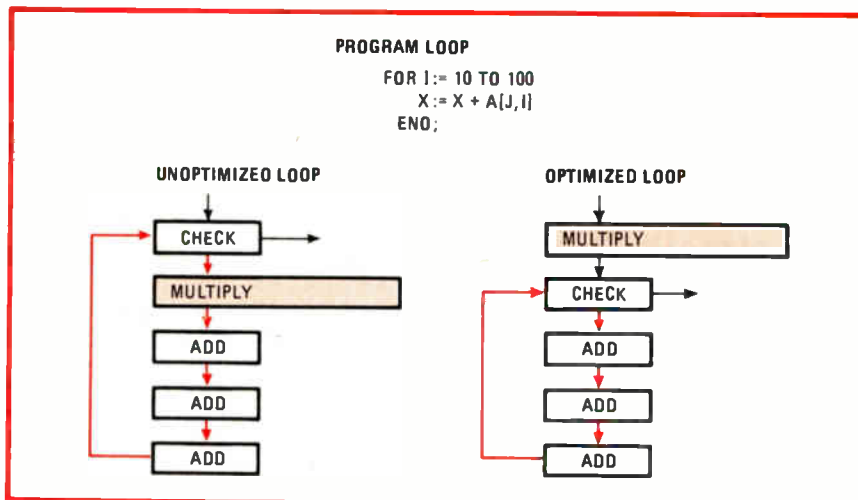
Along with the chip, the whole machine was slimmed. An 11/730 without memory requires three hex boards, which measure some 8 by 15 inches each. "We've been able to put the MicroVAX I on two quad [8 by 10 in.] boards," says Coppenrath.

Cloned. Besides getting a chance to prove the merits of its silicon compiler, Silicon Compilers got the right to market the data-path circuit to other companies, so long as it has a different pinout and uses different operational codes. DEC's competitors most likely will do to MicroVAX what IBM's have done to the Personal Computer: clone it by using the same processor and the same operating system (or a very similar one) and by writing their own microcode.

Software

C compiler in one pass optimizes source code

In the competition to score with a state-of-the-art compiler for optimizing application software, Green Hills



Speedup. In this array-subscripting operation, an implicit multiplication inside the loop calculates array locations. Because successive iterations result in array references separated by a constant value, an optimizing compiler like Green Hills's replaces the multiply by an add to speed up the loop. The relative time for each operation is shown by the length of its box.

Software, a start-up firm in Pasadena, Calif., is racing for a front position. The four-year tide of faster and smaller 16-bit microcomputers is coming up against hardware limits, and, with many designers looking for the software that will spur the next wave of performance boosts, the optimizing compiler may be the answer.

Green Hills has already delivered C-language versions for computers built around Motorola Inc.'s 68000 microprocessor chips. It expects to have another for National Semiconductor Corp.'s 16000 microprocessor within a month.

The company is anything but shy about making performance claims for its handiwork. On its compiler, maintains Conrad Schneiker, the firm's marketing director, "the generated code runs up to four times faster than other portable C compilers." Furthermore, he says, the compiler does it by generating up to 30% less code than its competitors.

Optimizing compilers are software packages that take programming instructions and rearrange them into more efficient source code for running the computers. About a dozen such compilers, mostly from small software houses, have made it to market; but they are hoary, born from pioneering work done by computer scientists at the Massachusetts Institute of Technology and AT&T

Bell Laboratories in the mid-1970s.

Green Hills president Dan O'Dowd explains that his package differs greatly from earlier versions because "we started over from scratch, using compiler techniques already proven in mainframes and big minis." The goal, he continues, was speed: a timesaving one-pass operation gives it an edge over other compilers, which can require as many as three passes.

O'Dowd, a principal designer of the National Semiconductor's 16000 microprocessor, says this single-pass feature became practical only during the past year, as microcomputer-memory capacity approached the 1-megabyte level. "With that much memory, we write straightforward code and implement algorithms to do a clear speed job," he says.

One key characteristic of the Green Hills compiler, say company officials, is global register allocation. This scheme embraces the program as a whole, rather than in small chunks—analogue to what a top programmer would do working in assembly language. The most frequently used variables, for example, are kept in the registers at all times, thus saving fetch time.

Other techniques eliminate redundant computations, plus carry out such usual optimizations as folding together common expressions, con-

verting multiplies into shifts when possible, and eliminating redundancies and unreachable code. In addition, Green Hills' compiler is compatible with Bell Laboratories' Unix operating system, the version of C language written at the University of California at Berkeley, and the Institute of Electrical and Electronics Engineers' floating-point standards, and it even includes a cross-compiler linking VAX/11 computers to the 68000 machines.

Word of mouth. With word spreading only through the software grapevine so far, the Green Hills compiler is selling steadily for \$2,000. This price is about double that of other versions but evidently not an obstacle, says Schneiker. After all, he adds, the firm's objective was not to wipe out competitors but to entice them to license the product.

Equipment manufacturers are interested and dickering for rights as well, he adds. Among those who now supply vintage optimizing C compilers is Motorola, which is closely following the Green Hills software. David Trissel, the firm's software product manager for advanced microprocessors, in Austin, Texas, calls it "good news. We need compilers that can utilize registers efficiently, and most of our customers say the others are unsatisfactory."

A user, William Jolitz, president of start-up Symmetric Computer Systems, Los Gatos, Calif., thinks the development squarely hits the prime mark of raising speed and efficiency. "It's really a black box that spews out optimized code," he says. His company is finishing a work station that is based on the National Semiconductor 16000 processor.

Consultants view the compiler as "illustrating the software thrust in improving microcomputer performance," as James Kane puts it. He is project manager at Technology Marketing Inc., an Irvine, Calif., firm that designs processors and turnkey computer systems. His only caveat: serious software glitches take longer to emerge than hardware bugs, so more run time is going to be needed before the Green Hills compiler totally proves itself. —Larry Waller

Natural language expands AI program

Next January, Frey Associates Inc., an Amherst, N. H., software house, will start to deliver a natural-language data-base query program that makes use of artificial intelligence to enlarge its vocabulary—without any help from a programmer. Commercial natural-language programs are rather few, and those that are currently on the market require a skilled programmer to insert new terms and phrases into their vocabularies.

The repertoire of Frey's Themis package, which will run at first on Digital Equipment Corp.'s VAX family of superminicomputers, can be expanded with a little assistance from any operator who knows a bit of basic English grammar. "We'll deliver Themis with a basic vocabulary of over 900 words, and the ease with which users can add new ones means it can then be tailored for a variety of special applications," says Eric D. Frey, the firm's founder and chief executive officer.

Themis, implemented with the InterLisp artificial-intelligence language, requires from 1.5 to 2 megabytes of a VAX computer's main memory. It interfaces directly with the VAX data-base-management system, DBMS/32, as well as with all standard VAX computer files. The package, which Frey Associates will sell for a single-copy price of \$24,500, can also interface with Data General Corp.'s version of Oracle, a relational-data-base-management system. Themis not only permits users to query a data base but in addition handles calculations and data manipulation, says Frey.

Bulletproof. Of course, Frey is not the first to offer a natural-language program. Artificial Intelligence Corp., for example, has tapped a substantial market for its natural-language interfaces with large computer systems, mainly those of IBM Corp. Since the Waltham, Mass., firm introduced its Intellect package, in 1980, it has sold about 150 of them,

priced from \$49,500 to \$69,500, depending on the operating system. Other firms—for instance, Cognitive Systems Inc., of New Haven, Conn.—have natural-language products but have made them available only on a custom basis.

"Making programs like this [Intellect] easily extensible is nothing new for the laboratory; we've been doing it for the last decade," notes artificial-intelligence researcher David McDonald, assistant professor of computer and information science at the University of Massachusetts in Amherst. "But then again, we didn't have to make our programs bulletproof." Bulletproofing is what a commercial market demands, and "the amount of work that entails is considerable," McDonald adds.

Frey will not divulge the details of the armor that succeeded in making his program bulletproof. He notes, however, that the components of Themis include a software driver that translates conversational-English queries from the operator terminal into a "language-understander module." A single copy of this module serves all the operators who use Themis on a VAX system by creating an internal representation of the query. The system can make sense of this representation in about four tenths of a second, Frey explains. The language understander then translates information from the data base back into English for display on the operator's terminal.

Swearing off. To comprehend an operator's command or inquiry, the language understander can pursue one of many possible logic sequences. In common with other natural-language programs like Intellect, Themis tolerates many misspellings, varying word orders, and incomplete sentences, Frey explains. It also accepts new words or phrases into a dialog by running a brief, interactive exchange in which the operator defines a term's grammatical construction and meaning.

The Themis package also gives operators a choice of keeping new terms either permanently or just temporarily, to be used in a single, special routine. Different operators can

introduce the same word but specify different meanings for their own use, and an authorized user with a password that controls a whole system can introduce a term with a single meaning, common to all the terminals in that system.

In only one instance does the package balk at an operator's attempts to expand the vocabulary of human-machine discourse: when the proposed expansion is too racy. "We've programmed Themis to disapprove politely but firmly when a user resorts to expletives," Frey says. —Linda Lowe

Microsystems

Intel's 32-bit bus challenges Motorola's

Original-equipment manufacturers with 32-bit systems on their minds will soon have a choice of buses: Intel's new Multibus II or Motorola's established VMEbus. To ensure that Intel Corp.'s new bus would move smoothly, the firm formed a consortium to put it together. Seventeen companies helped the Santa Clara, Calif., company write the specifications, and an additional 51 firms have expressed interest in supporting the bus.

Intel's route resembles the one that Motorola Semiconductor Products Inc. took when it became the first company to offer a major 32-bit bus. Two years ago, the Phoenix, Ariz., company put the VMEbus (Versa Module Europa bus) on the market in cooperation with such impressive allies as Mostek Corp., France's Thomson-CSF, and Signetics Corp. and its Dutch parent, Philips Gloeilampenfabrieken.

Popular. Although Intel is a late starter in 32-bit buses, its original Multibus has long been the most popular competitor for 8- and 16-bit single-board computers. Multibus, which works with a variety of microprocessors, has been adopted by more than 200 vendors and designed into more than 1,250 products, with a total value this year of more than

\$200 million. By contrast, the VMEbus has claimed fewer than 100 vendors and probably a tenth of the dollar volume for product sales.

The VMEbus continues to come on strong, however. For one thing, Motorola's 32-bit 68000 microprocessor is increasingly popular; for another, the trend is now to replace conventional edge-backplane connectors with the more reliable Eurocard plug-and-socket connector in the VMEbus. One semiconductor executive estimates that its sales are growing at five times those of Multibus I—not surprising, perhaps, in view of its smaller but nonetheless significant base, since its growth seems to be tied to the fortunes of the 68000 family. These processors—despite their internal 32-bit architecture—have mostly been used for 16-bit off-chip data transfer, but OEMs who want full 32-bit power have turned to them and to the VMEbus.

Quintet. Intel will formally launch Multibus II at the late-November Comdex show, in Las Vegas. Intel will show five interconnected, software-configurable buses:

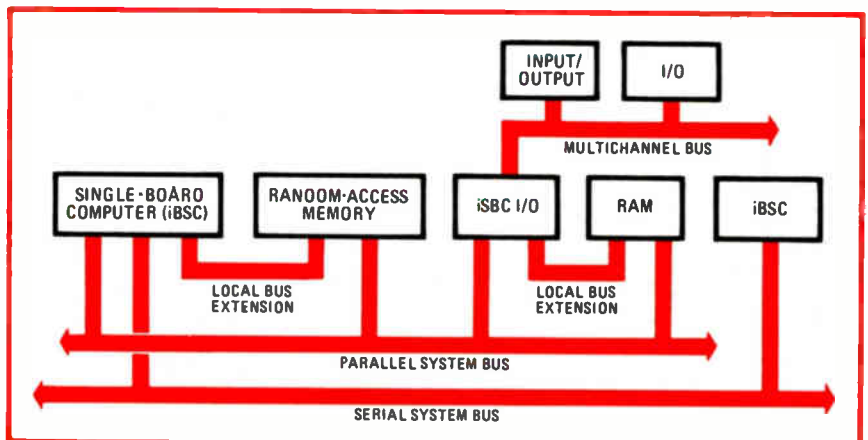
- A 32-bit-wide, 10-megahertz synchronous parallel system bus, which can operate at 40 megabytes per second in a pipelined "burst" mode.
- A 12-MHz local bus extension that provides arbitration-free access for up to 64 megabytes of local memory for any central processor.
- A low-bandwidth (2-MHz) serial system bus for message passing.

■ Two Multibus I carryovers, a multichannel direct memory access (DMA) input/output bus and an I/O expansion bus. (Both the parallel system bus and the serial system bus use the same VLSI interface, so they are software-compatible.)

By contrast, the VMEbus architecture consists of a single 32-bit-wide asynchronous data path. At each cycle, it is dynamically configurable into a data-transfer bus, a seven-level priority interrupt bus, a four-level arbitration bus, and a utility bus.

As for software, the new bus is compatible with Multibus I, says product marketing manager Frank Costa, who adds that the only change required will be the writing of new device drivers. To some extent, Costa notes, the complexity of any upgrade depends on the operating system. In any case, "we don't think it will be a major exercise to revise the software."

Standard stuff. Like the VMEbus, Multibus II will use Eurocard connectors, though Intel has opted for a card 220 millimeters deep rather than for the 160-mm standard Eurocard depth that has proved popular in Europe. And like the VMEbus and Multibus I, the new 32-bit package is being considered by the Institute of Electrical and Electronics Engineers for adoption as a standard. Multibus I has already been adopted as IEEE 796; the VMEbus should be established as IEEE 1014 by next spring. IEEE committee 896—the



Specialized. Intel's Multibus II divides the chore of shuttling instructions and data among single-board computers, memory, and the input/output channels of five specialized buses. The synchronous parallel system bus runs at 10 MHz, local bus extensions at 12 MHz.

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Next page, next part.

Futurebus committee, formed to set a 32-bit standard—has now split into two parts. One will specify a synchronous standard matching Multibus II.

Meanwhile, Motorola has moved to meet its new competition. An intercompany group is at work on several added system-level buses, which will not be part of the VMEbus spec but will complement it. They sound remarkably like Multibus features: a high-speed secondary bus for memory access, a bus for additional I/O channels, and a serial sub-bus. Motorola will discuss them at Wescon, early next month. —Clifford Barney

Peripherals

Office computers get digitizing scanners

Personal computers for the office are getting the tools they need in order to read. A new electronic digitizing camera available now from Datacopy Corp., Palo Alto, Calif., for example, will scan, digitize, and store documents, photos, drawings, microfilm, and even three-dimensional objects.

The unit does not come cheap, however. Single-quantity price of the model 610 to system integrators is \$7,850. This buys a top digitizing resolution of 2,846 (X-axis) by 1,728 (Y-axis) picture elements—higher than any present-day cathode-ray-tube terminal can display. Eight-bit encoding for each pixel produces up to 256 shades of gray, sufficient for digitizing photographs.

Image digitizers are the newest wrinkle in a string of sophisticated input peripherals becoming available for personal business and professional computers. Wang Laboratories, Lowell, Mass., also this month introduced a desktop computer system with an image digitizer that will be available in February.

The Wang Professional Image Computer, starting at \$14,965 per unit, is compatible with Wang's existing VS/11S, VS/Alliance, OIS, and Alliance office systems. It allows users to digitize (at 1,728 pixels in the

X axis, 2,200 in the Y), display, merge with text, and transmit anything from handwritten notes to pictures and diagrams. Hard copy is produced on the laser printers available from Wang, or the PIC system will drive a new thermal printer with both image and text capabilities.

The advantage of digitizing images is that once converted into digital form, the image can be manipulated and stored like any other data—modified, extracted from, scaled in size, combined, stored, and transported over communication lines.

Scanning. Datacopy's camera contains a linear array of 1,728 charge-coupled-device photosensors that moves across the image plane. The X axis is scanned physically, the Y axis electronically (see diagram below). Most 35-millimeter camera optics, such as standard Nikon lenses, are suitable, and the camera can be adapted to microscopes and telescopes. Digitizing electronics in the camera produces a stream of up to 4,917,888 8-bit pixels for each image.

Datacopy, an early developer (since 1973) of low-cost, high-resolution imaging devices, also has the hardware and software for interfacing the camera with the IBM Personal Computer. A powerful image-processing subsystem rather than an interface alone, the package does both threshold conversion and halftone creation. Each of these techniques reduce by a factor of eight the amount

of data, but not necessarily the amount of information, to be stored in the computer.

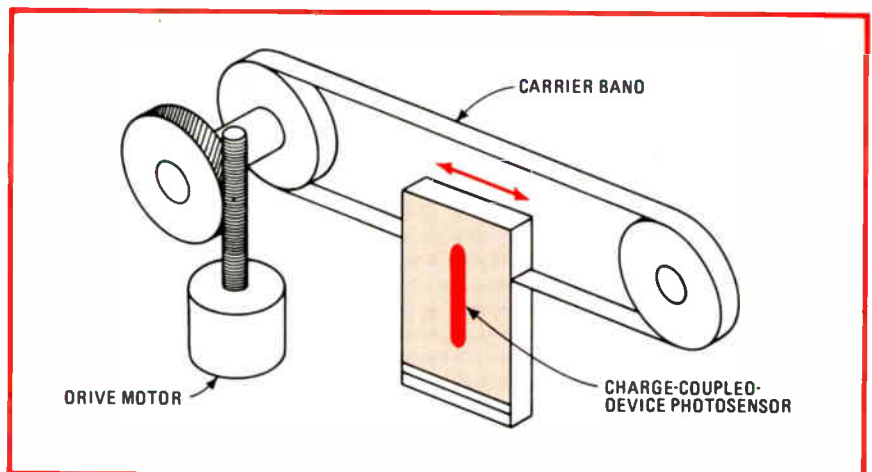
Thresholding is used for black and white images like text and line drawings. It converts the 8-bit pixel data into 1 bit—either black or white. Gray scale is not needed here, and the threshold level is set under program control at any of the 256 shades of gray. The halftone processing, used primarily for photographs, simplifies the gray-scale image by controlling the density of the halftone's black dots to produce an illusion of gray scale.

Price of the image processor-interface is \$795. An integrated imaging system with camera, image processor and interface, camera power supply, camera stand, light unit, a lens, cables, and service manual costs \$9,945. Interfaces with other popular computers are planned.—Tom Manuel

Communications

Airliner phone nets compete for takeoff

The Federal Communications Commission is about ready to assign 4 megahertz of spectrum in the 900-MHz region for in-flight telephone service. Backers of each of the three contending systems are stepping up their lobbying to convince the FCC



Back and forth. Sweeping this charge-coupled-device photosensor array across an image develops the X-axis input—2,846 pixels—for the Datacopy digitizing camera. The electronic scan of the Y axis has 1,728-pixel resolution, equal to the number of CCDs in the array.

EAST PART 5:



The 74F548 Octal Decoder/Demultiplexer

Welcome to the fifth part in our new 12-part series on FAST, Fairchild Advanced Schottky TTL.

The 74F548 Octal Decoder/Demultiplexer has a maximum address or enable to output delay time of 11.0ns and a low power spec of 21mA (max). It's a 3-to-8-line address decoder with four enable inputs, pin-compatible with the 25LS2548, only much faster.

The 74F548 offers address extension by multiple enables. Also provided is an active LOW acknowledge output that responds to either a Read or Write input

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signal when the enables are active.

The 74F548 is ideal for chip select decoding in small, medium or large address systems where multiple chip selects must be generated and where address space must be allocated conservatively.

Add a little zip to your address decoder. With the 74F548 from FAST.

For samples and additional information, contact Fairchild Digital Products Division, Marketing Department, 333 Western Avenue, South Portland, ME 04106.

Next page, next part.



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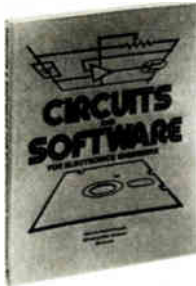
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Electronics review

News briefs

MCC close to announcing its seven top project managers

Hoping to kick off its research efforts no later than February, Microelectronics & Computer Technology Corp.—the Austin, Texas, electronics-industry cooperative—is set to announce the names of the seven managers of its advanced technology programs, says president and chairman Bobby R. Inman. Inman had hoped to start work Dec. 1, but, he says, it has taken longer than expected to review job candidates from MCC's 13 shareholding companies and other organizations. He projects MCC employment at 40 to 60 by Jan. 1 and at 150 to 160 by midsummer. The cooperative now has a dozen on staff, including recently named vice president and chief scientist John Pinkston, former deputy director of research for the National Security Agency.

The research areas include data-base management, software, packaging, computer-aided design and manufacturing, and the human interface with computers, or ergonomics. "Industrywide, I would have to say the smallest pool of talent related to our programs comes in the artificial-intelligence field. The next-scarcest area is parallel processing," Inman notes.

Inman expects MCC employment growth to slow after July 1984 and to pick up again after the cooperative's permanent facility is completed in north Austin around the third quarter of 1985. By then, MCC could be in a position to consider additional long-range research programs, says Inman, suggesting such fields as robotics and "the entire area of telecommunications."

Corning gets research contract for optical waveguides of halide glass

A basic research contract for the development of halide glasses for optical waveguide fibers has been awarded to Corning Glass Works, Corning, N. Y., by the U. S. Air Force Office of Scientific Research, Bolling Air Force Base, D. C. Studies at Corning had shown that optical waveguides made of a beryllium-fluoride halide glass might offer an optical loss at least two orders of magnitude lower than that of standard silica-based optical fibers. Such low loss could allow data to be transmitted over hundreds or even thousands of kilometers without amplification, says Corning. Also, beryllium-fluoride-based glasses have inherently better tolerance to nuclear radiation than silica-based glasses. The one-year research contract, worth \$150,000, calls for evaluation of optical, structural, mechanical, and other physical properties.

Semicustom ICs to top market growth at 40% yearly, says Predicasts

At over 40% annually, the fastest-growing segment of the integrated-circuit market over the next four years will be semicustom ICs—gate and programmable-logic arrays and standard cells—according to "U. S. Semiconductor & Other Electronic Components Markets," a recent study by Predicasts Inc., Cleveland. The market research firm pegs U. S. semicustom sales at \$220 million in 1982, \$1.275 billion in 1987, and \$3.5 billion in 1995. It also has total sales of digital ICs growing 15% annually from 1982 (\$4.931 billion) through 1987 (\$9.850 billion), moderating to about 9% annually through the middle of the next decade, and reaching \$19.3 billion in 1995. Other projections in the study, which sells for \$1,400, include the growth of linear ICs from \$900 million in 1982 to \$1.5 billion in 1987, or 8% annually, and of discrete semiconductors from more than \$2 billion in 1982 to \$3.3 billion in 1987, or 9% annually.

that their system's scheme is best at frequency conservation, which the agency deems essential as demand mounts for space in the crowded radio-frequency spectrum.

The latest firm to make its case to

the regulators charged with setting the service's technical parameters is Millicom Airborne Telephone Services Inc., a Washington, D. C., subsidiary of New York City-based Millicom Inc. MATS late last month

In head-to-head comparison, there's really no comparison. Our OS4040 stacks up best.

The Gould OS4040 digital storage oscilloscope vs. the Philips PM3310 and Tektronix® 468.

The right balance between sampling speed and detail, for accurate measurement. The faster sampling rates of the Philips and Tek units don't mean much without supporting memory. The Gould OS4040 can capture and store 5,120 words on a single waveform compared with 256 for the PM3310 and 512 for the Tek 468. That means the OS4040 can expand a stored trace by 50 times horizontally and still give you 100 data points across the screen. Under the same circumstances, with Philips' 256 words you would get only 5 actual data points. Tek would give you 10 data points. For a detailed display, the OS4040 is the clear winner.

Fast capture of sequential signal events, as in digital logic circuits.

The OS4040 can capture up to four signals from a single channel and hold them in separate storage for later analysis. It does this with direct store access at up to 10 MHz. While the Philips can capture the signals, it requires considerably more time between the capture of each event since it can only access its store via a 78 kHz ADC from its CCD line. Tek can only capture up to two sequential events from a single channel.

The most flexible interface facilities. Only the OS4040 can copy captured waveforms onto a chart recorder from both channels simultaneously, and is able to plot one signal against another, for example, as in hysteresis curve plotting. The PM3310 and

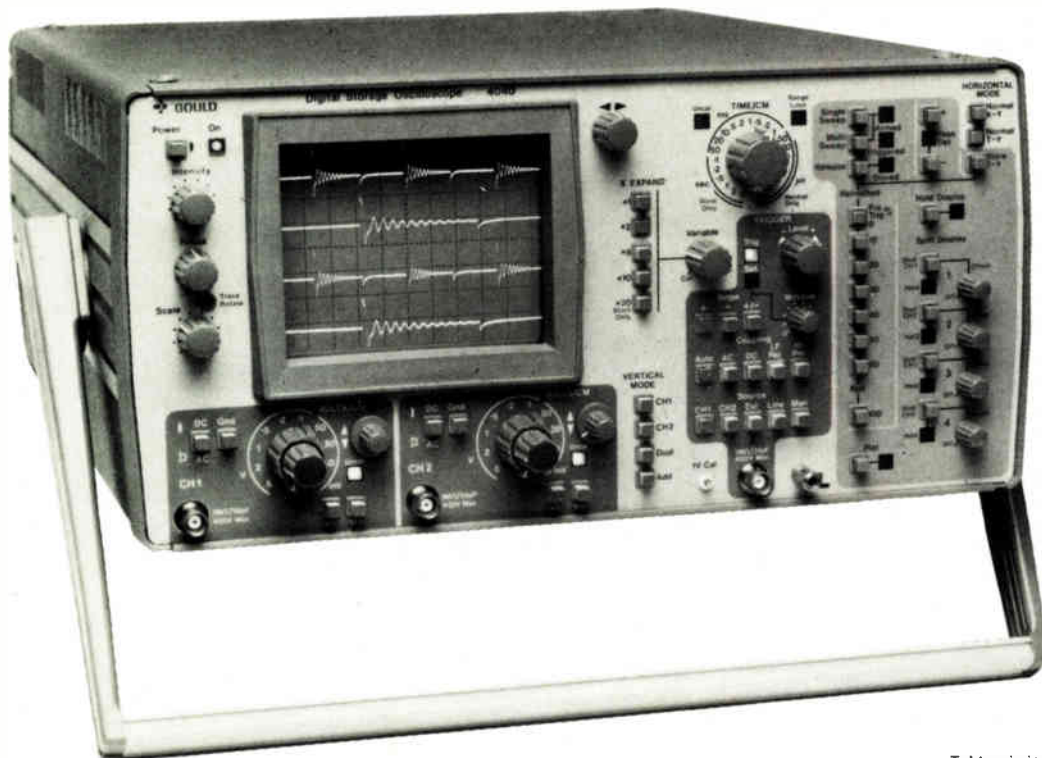
the Tek 468 can only output one channel at a time.

The OS4040 can "baby-sit" for you. It has a "baby-sitter" mode, so each signal captured can be automatically transferred to the chart recorder, and the store armed for the next signal event. The PM3310 offers neither repetitive analog output nor a "baby-sitter" mode. And while the 468 provides an analog option, it is not capable of "baby-sitting."

Exclusive direct digital user port.

Even though all three systems offer an IEEE output, only the OS4040 offers a direct digital user port as a standard option for situations where the IEEE is too slow for the buffer store to be cleared before the next signal capture.

The Gould OS4040 digital storage oscilloscope. For the whole story, contact Gould Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279. Nationwide (800) 538-9320. California (800) 662-9231 or (408) 988-6800.

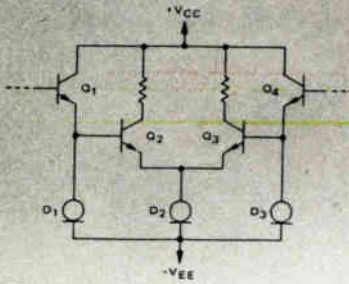


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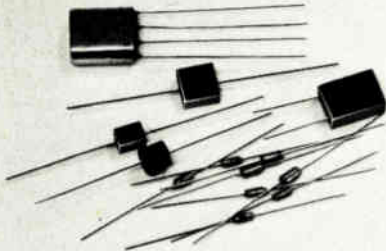
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Electronics review

asked the FCC for a license to set up a test system, based on land cellular-radio technology, to cover the New York-Chicago air route [*Electronics*, Sept. 22, p. 67].

Using cellular radio's three main concepts—call hand-off, frequency modulation, and 30-kilohertz channels—MATS says it can pack about 60 voice channels into each of 30 ground-station sites, allowing a total of 1,800 simultaneous calls to be initiated from airliners flying at an average altitude of 14,000 feet. "The innovation is that we can do this with a 4-MHz allocation and achieve 100% frequency re-use," states Jerry Schmitt, chief engineer for MATS. That contrasts with a 7:1 (roughly 14%) re-use ratio for land-based cellular systems, he adds.

Spaced out. Schmitt claims that the same 60 frequencies can be used by adjacent stations, spaced about 340 miles apart. Not so, maintains Aeronautical Radio Inc., of Annapolis, Md. Arinc has its hand-off approach and insists that co-channel-interference protection from aircraft flying at altitudes of 45,000 ft necessitates frequency re-use at a minimum distance of 650 miles.

Airfone Inc., headquartered in Oakwood, Ill., has much the same view as Arinc. The only company with a test system up and running (it will go nationwide on Jan. 15, 1984), Airfone reports that it needs a spread of 450 to 500 miles between ground stations for reassignment of the same frequency.

The way MATS achieves its spectrum efficiency is proprietary, says Schmitt. But an FCC engineer privy to parts of the MATS filing says they are probably using polarization techniques, like those used for satellites. A 100% re-use factor, he explains, could result from transmitting two signals on the same frequency with right and left polarizations.

The polarization diversity puts into play an fm capture effect, whereby the receiver's discriminator locks onto one signal and rejects interference from the other. The larger the bandwidth, the higher the rejection level, he points out. Schmitt declines to say whether MATS' ap-

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When Texas Instruments and Hewlett-Packard team up, quality in technical computers goes up.

- TI device quality is so high, Hewlett-Packard's Fort Collins Systems Division will greatly reduce incoming testing (Page 2).
- TI's Quality Improvement Program assures consistently high-quality standard semiconductors for all TI customers (Page 3).
- More than 100 quality TI Advanced Low-power Schottky/Advanced Schottky devices offer still greater performance (Page 4).

The high technical

Incoming bipolar digital and linear integrated circuits from Texas Instruments rank among the highest quality ever received by Hewlett-Packard's Fort Collins Systems Division.

Result: The extra quality built into each TI device helps HP design technical computers noted around the world for performance and reliability.

An example is the new HP Series 200 Model 16 Personal Technical Computer shown on the previous page. This powerful 16-bit computer is designed for the most demanding technical and scientific applications.

HP technical computers, in fact, include a wide range of TI bipolar digital components: Advanced Low-power Schottky, Advanced Schottky, Low-power Schottky, Schottky TTL, and regular TTL. Quality TI linear circuits and interface devices also are incorporated.

TI/HP team effort achieves best PPM quality levels

Three years of close cooperative teamwork between TI and HP have reduced the number of total electrical defects in parts per million (PPM) to well under 500 (see graph).

The quality of incoming TI devices is so high, HP will significantly reduce incoming testing.

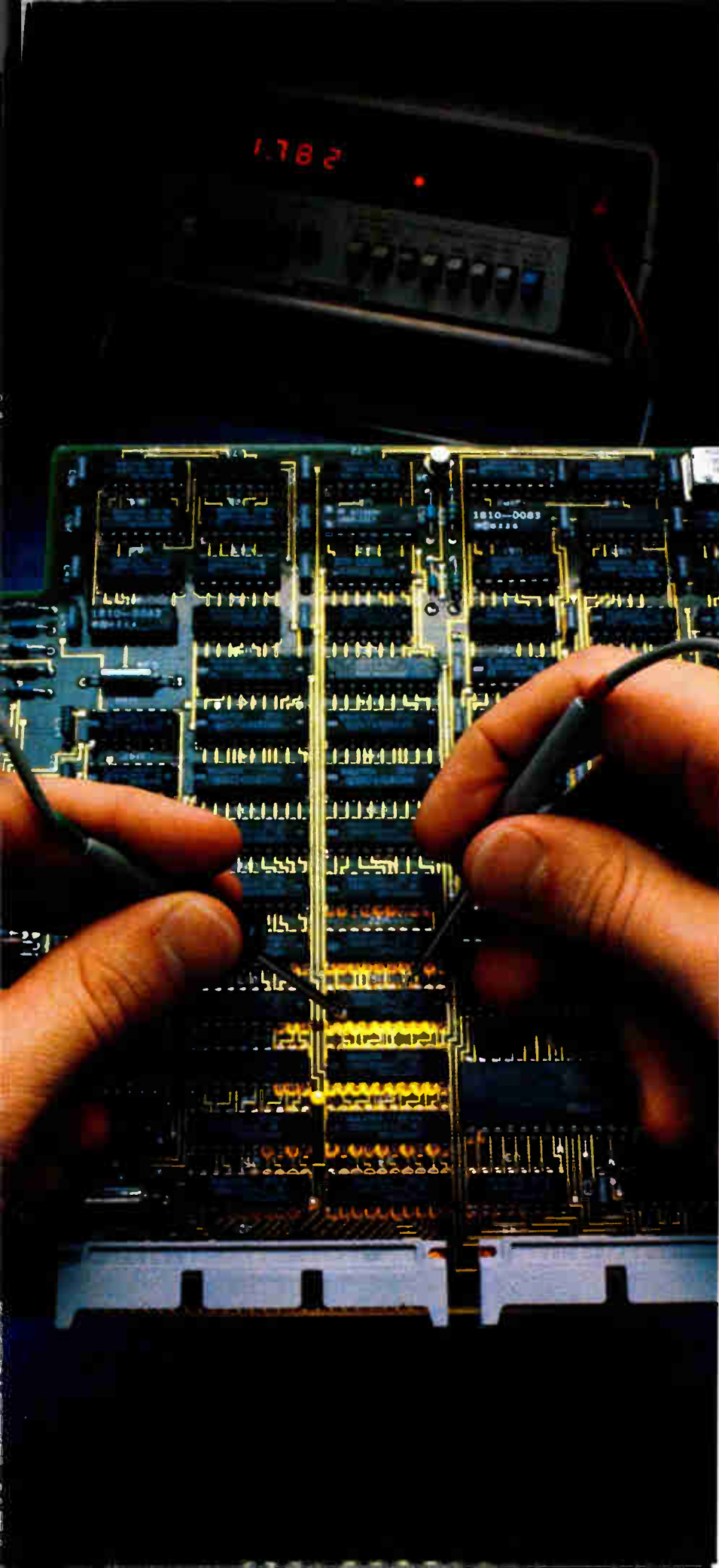
Crucial to achieving these unprecedented quality levels has been the formation of a "Quality Team" made up of members from both TI and HP. The team regularly meets to exchange information, establish goals, and measure progress.

Higher quality TI devices speed HP products to market

The superior quality of TI ICs pays off for HP. In several ways.

First, without exceptionally reliable components, HP could not build increasingly powerful scientific computers. Equipment reliability simply would not be good enough.

◀ **Board-level test results**, in addition to data from incoming parts inspection, are passed on to TI from HP's Fort Collins Systems Division to further improve IC quality.



TI quality that helps improve computers for HP also helps you.

In fact, the extra quality built into each TI device has helped HP's Fort Collins Systems Division achieve product improvement goals. Compared with its 1980 units, HP's comparable products now offer triple the reliability at one-third the price.

Second, the extra quality built into advanced TI logic functions (74ALS and 74AS) enables HP to incorporate leading-edge technology into its products — without having to wait for years for the technology to prove itself.

The bottom line is this: Quality TI devices help HP get innovative products into production and to market faster.

You get the same higher quality TI semiconductors

The standard TI semiconductor devices your local distributor stocks are *exactly* the same — up to symbolization — as those we ship to HP and all other TI customers. The ICs come off the same production line. Receive the same processing. And are 100% DC tested.

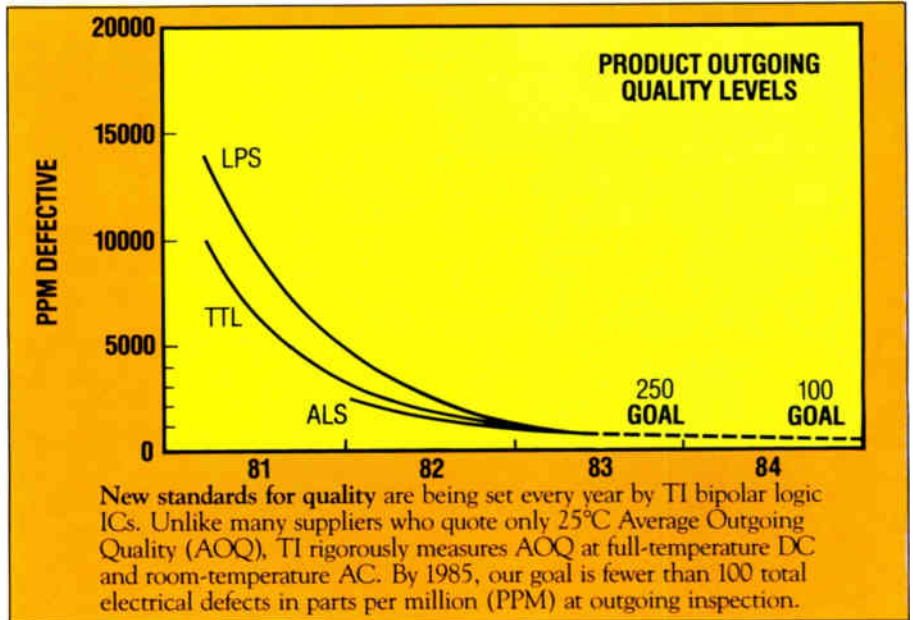
The TI approach to quality is simple: Do it right the first time. At TI, quality/reliability is designed and built into every device, rather than just testing out defects.



Testing of TI devices at HP's Incoming Quality Audit will be substantially reduced because ICs are of such high quality.

A quality program that works for you

The close teamwork between TI and HP is just one aspect of the TI Quality Improvement Program. A comprehensive



program designed to lower the cost of TI components to all our customers by reducing defective ICs. By eliminating the need for incoming testing. By minimizing board-level failures. And by preventing even more costly equipment failures in the field.

To achieve this, TI's 100% testing of all standard devices is followed by rigorous QA sampling (see table). Advanced multitesting, as well as automated handling, fabrication, and inspection, also is utilized to push quality levels higher.

The bottom line? When you want the highest quality, most cost-effective components, do what HP does. Specify standard TI bipolar digital and linear ICs.

Built-in TI quality can save you money

Higher quality TI parts can cut your costs substantially.

The cost of defects to you depends on when the failure occurs. For example, the cost to detect and replace components at your incoming inspection may amount to only a few pennies per device.

Your costs, however, rise significantly as undetected defective ICs are integrated into systems.

Still more costly are defective components that go undetected at the system test level, but later fail in field applications. Here, the damage inflicted not only applies to the thousands of dollars

lost in trouble-shooting, downtime, and replacements, but it also affects your company's reputation for high-quality, reliable equipment and systems.

For all these reasons, the extra quality built into every TI device means added value for you and your customers. And tremendous cost savings over the years.

GUARANTEED AQL		
TEST	CONDITION	PPM (parts per million)
DC PARAMETRIC	0°C to 70°C	400
AC PARAMETRIC	25°C*	1,500

*Sampled and guaranteed.

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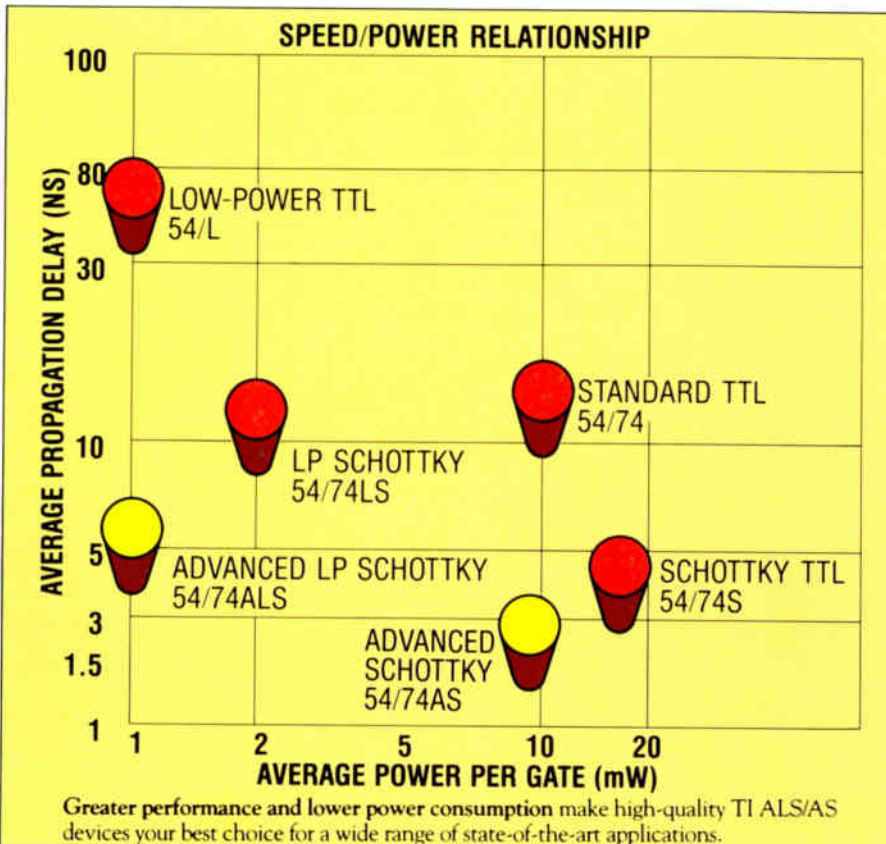
Higher quality ICs mean higher profits

For every dollar decrease in reported failure costs, there is a positive "multiplier effect" on your profit margins. Estimates for electronic equipment range from five to 10 times.

By incorporating a "do it right the first time" concept, the TI Quality Improvement Program eliminates defects before they happen. To you, this means greater profits. Today and tomorrow.

High-performance ALS/AS logic. 100 quality reasons to choose TI.

Authorized TI Distributors



Superior quality. Higher performance. And reduced power consumption. You get all this and more from TI's Advanced Low-power Schottky (74ALS) and Advanced Schottky (74AS) TTL devices.

Twice the speed, half the power

With a typical 1.5-ns gate delay and 8-mW gate power dissipation, TI's 74AS Series devices give you double the speed and less than half the power dissipation of earlier Schottky ICs. Internal gate delay for MSI functions is typically less than 1 ns, while power consumption is less than 5 mW.

TI's 74ALS Series devices offer you typically 50% lower power consumption than 74LS ICs, with speed approaching that of standard Schottky devices. Featuring 1-mW gate power dissipation and a typical 4-ns gate delay, TI's 74ALS family is ideal for low-power, high-speed applications.

Save board space

Many of these new Schottky ICs are MSI and LSI functions offered in plastic dual-in-line packages — 300-mil wide, 24-

pin; and 600-mil wide, 52-pin. This lets you virtually double functional densities and reduce board space by 30% — or more.

Still greater improvements in functional densities can be yours with 20-, 28-, 44-, and 68-pin plastic chip carriers. All are JEDEC standard with lead spacings on 50-mil centers.

Economical for the '80s

We project TI's 74ALS devices will reach price parity with today's widely used Low-power Schottky (LS) functions by the second half of 1984.

Today you can choose from more than 100 ALS/AS functions from your local TI distributor or direct from TI. In 1983 alone, TI plans to add more than 100 new functions.

For military systems, data processing, telecommunications, or process control, TI's ALS/AS devices can be your key to cost-effective TTL solutions in the '80s.

For more information on the TI Quality Improvement Program and a complete list of TI bipolar logic devices, write Texas Instruments Incorporated, Dept. SDA013EC, P.O. Box 401560, Dallas, Texas 75240.

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Electronics review

proach works that way but does admit that a wide bandwidth is crucial.

Pros and cons. MATS' competitors, by contrast, doubt the FCC will accept the bandwidth penalty that comes with fm. Ronald Weber, director of transmission-systems engineering at Arinc, argues that amplitude-modulated single-sideband techniques, in addition to permitting frequency sharing, require only one third to one fifth the bandwidth that fm does for an equivalent grade of service. Tom Dennis, AirFone's vice president of engineering, agrees.

Schmitt counters that SSB's greater susceptibility to multipath negates the frequency advantages; Weber and Dennis deny that. In Arinc's design, multipath is controlled through companding. AirFone has a patent pending on a computerized system that analyzes doppler shifts, as well as signal strength, to select the ground station farthest in front of the aircraft with a usable signal.

More players. Over and above its concern for spectrum efficiency, the FCC wants competition to develop in the still-nascent airborne-telephone market. That could mean points for Arinc, as it is the only operator to propose a design with room for more than one player. Consequently, on the grounds that "sufficiency is as critical as efficiency," Arinc is urging the agency to allocate at least 12 MHz to the service. With that bandwidth, it wants to establish eight families of frequencies that could be divided into five subfamilies of 25 channels in high-density cell areas and three subfamilies of 15 channels. Such a scheme, utilizing 8-kHz SSB channels, would allow up to five competing systems and future traffic growth.

—Karen Berney

Local networks

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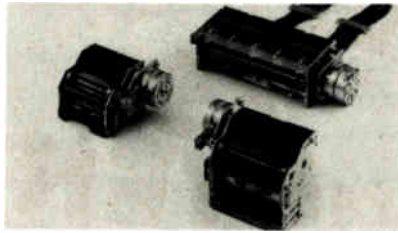
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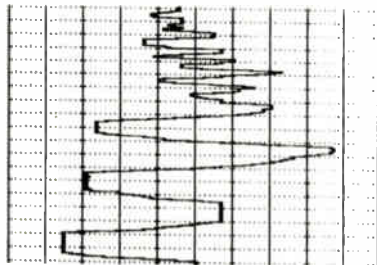


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Electronics review

sion for network planners—with one firm proviso. The network's uses must be well defined and its makeup stay relatively fixed.

Planners who expect their local nets to grow in size and diversity of applications, however, face a considerably more difficult choice. They may find it somewhat less of a Solomon decision, though, if the promise of a networking product from a young Massachusetts company is borne out.

The available schemes are carrier-sensing multiple-access with collision detection (CSMA/CD)—the approach used for Ethernet and championed by Xerox Corp., Digital Equipment Corp., and Intel Corp.—and token passing, backed by IBM Corp. CSMA/CD works best with low-traffic nodes; token passing ensures that heavy-traffic nodes have guaranteed access to the network.

Bridged. Two-year-old Applitek Corp., of Wakefield, is looking to carve a niche for itself in the local-net market and will unveil this month its UniLAN networking product, aimed at bridging the two approaches. Says its inventor, Ashraf M. Dahod, Applitek's founder and chairman: "In five years, people will look back and laugh over this so-called debate about which was better. If you can have both, the whole matter becomes irrelevant."

UniLAN provides both, albeit at a cost some 10% to 15% higher than that of an Ethernet or token-passing network. It does so by means of an access protocol that breaks up time

Assignments. Applitek's local network combines CSMA/CD and token passing. It assigns individual slots to heavy-traffic nodes but makes low-traffic nodes share slots.



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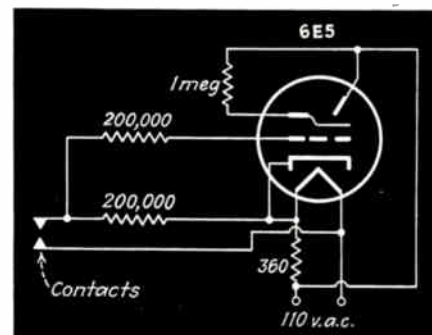
passed through a saturable reactor, one winding of which is in series with the power line and an electric heater. When zero current passes through the saturable reactor, the heater winding acts as a current-limiting reactor and no voltage is applied to the heater. However, when current does flow through it, it becomes saturated and the inductance drops to a very low value. Voltage is applied to the heating element whenever thyatron current flows. When the temperature reaches the desired level, the bridge is again balanced, thyatron anode current flows and application of heat ceases.

To avoid overloading the circuit when a relatively great drop in temperature occurs, automatic gain control is used on the amplifier. This is obtained by the application of automatic bias control derived from part of the output transformer.—Penther and Pompeo, *ELECTRONICS*, April 1941, p. 20.

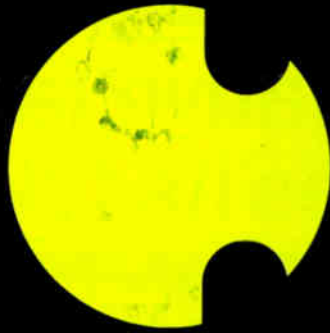
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Referring to the figure, the grid of the 6E5 is biased sufficiently nega-



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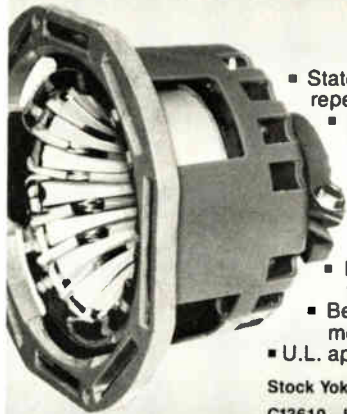


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			(3A, 2°/1700)			(3A, 3°/1700)
C13610-A	43.5	0.13	8.50	8.50	12.3	0.52
C13610-B	110	0.30	5.40	8.50	12.3	0.52
C13610-C	110	0.30	5.40	0.13	0.24	4.20

C13710—Portrait/Vertical Format*

	L _H (μH)	R _H (ohm)	I _H (A)	L _V (mH)	R _V (ohm)	I _V (A)
			(3A, 2°/1700)			(3A, 2°/1700)
C13710-A	43.5	0.13	7.00	8.50	12.3	0.63
C13710-B	110	0.30	4.50	8.50	12.3	0.63
C13710-C	110	0.30	4.50	0.13	0.24	5.10

*Horizontal is fast scan axis. Table shows nominal values. Samples and production available. Call factory for details.



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on the network, which runs at 10 megabits per second, into "messages"—periods during which data packets of fixed or variable lengths may be transmitted. These periods are numbered sequentially and are assigned to specific equipment on the network.

Fair share. Devices with low duty cycles, whose infrequent, "bursty" transmissions would waste most of a regularly scheduled message slot, however, share slots and so access the network on a contention basis during their assigned periods. Mainframes and intelligent terminals have one or more slots exclusively, which guarantees them a known frequency of access.

Counters in the network's interface units monitor message-period number boundaries as they occur. Through a process called pacing, any interface unit can synchronize all interface units' counters so that all correctly track the numbers. Thus, nodes having dedicated message-period assignments require no electrical pulse to trigger their transmission, as is the case with conventional token passing; they merely go to work when their interface unit senses their assigned number on the network, eliminating the problem of missing tokens, which can disturb normal token-passing arrangements.

The interface units, based on Motorola's 68000 microprocessor, contain software that conforms to the layering scheme proposed in the International Standards Organization's open-system interconnection (ISO/OSI) model. Through menus, users can connect or disconnect virtual-circuit links for passing data between network nodes, determine the size of data packets for each node, send messages, or call up and log network-diagnostic reports.

Users can also specify (and change) a ratio of contention to dedicated access assignments on UniLAN or specify a network-traffic threshold. The latter permits nodes normally assigned access on a contention basis to request and receive dedicated, guaranteed access if network traffic increases or there is a backlog of unsent messages.

—Linda Lowe

SCIENCE/SCOPE

The first electro-optical use of a flexible machining system will be for manufacturing large numbers of ultra-precision optical housings. The new Hughes Aircraft Company "flex-fab" system is a combination of nine computer-controlled milling machines connected by carts that are pulled on an endless chain towline built into the floor. Each machine has 68 different tools to choose from. Altogether there are 612 tools available, enabling flex-fab to do the work of 25 individual machines. At first, flex-fab will machine aluminum chunks into housings for TOW antitank missile systems with an exactness to one thousandth of an inch. Soon, design engineers will be able to ask flex-fab to build parts, thus eliminating the need for blueprints.

Among many innovations built into the new AMRAAM missile are a special safety mechanism and a high-power coaxial cable. The safety device will prevent the missile from exploding when subjected to fire, yet will not be activated by the high temperatures generated by burning fuel when the missile is launched. The new cable handles much more power than conventional cables and yet costs about one-tenth as much. Hughes designed and developed the Advanced Medium-Range Air-to-Air Missile for the U.S. Air Force and Navy.

Very High Speed Integrated Circuit technology will be introduced in a system that lets U.S. Army and Marine Corps units automatically report navigation data and their locations to command centers. Hughes VHSIC chips will be used in the Position Location Reporting System. The chips will significantly increase communications and encoding capability, and reduce vulnerability to jamming. The VHSIC program is being conducted by the Department of Defense to develop chips that will give military electronic systems a tenfold increase in signal processing capability. The high-speed, compact VHSIC chips will be more reliable and will require less power than integrated circuits now in use.

The improved Phoenix missile has passed severe environmental testing by the U.S. Navy and demonstrated that the air-to-air weapon will operate reliably throughout its intended lifetime of service. No failures were recorded during 600 hours of severe vibration and exposure to temperature extremes. Up to five failures were allowed before results would have been judged unsatisfactory. (A failure would have been any fault in the missile's internal systems that would have prevented it from being launched.) The test was the first in a series of evaluations to certify the new-generation Hughes AIM-54C for service with the fleet. The improved Phoenix is the principal long-range, radar-guided missile for the F-14.

Hughes Missile Systems Group, located in Canoga Park, California, an attractive suburb of Los Angeles, is seeking engineers and scientists for such developmental and engineering programs as AMRAAM, multimode guidance, Phoenix, and IR Maverick. Openings are in radar and electro-optical systems design, systems software and hardware/software integration, analog and digital circuits design, hybrid process engineering, and systems performance. Qualified applicants are assured prompt replies. Please send resume to Hughes Engineering Employment Manager, Dept. SE, Fallbrook at Roscoe, Canoga Park, CA 91304. Equal opportunity employer.

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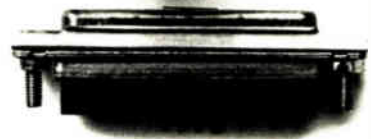
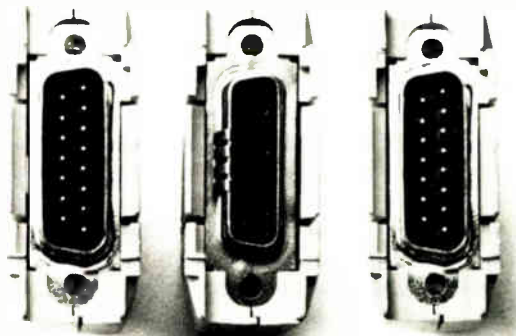
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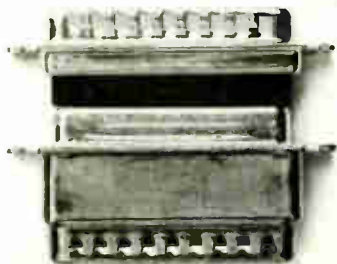
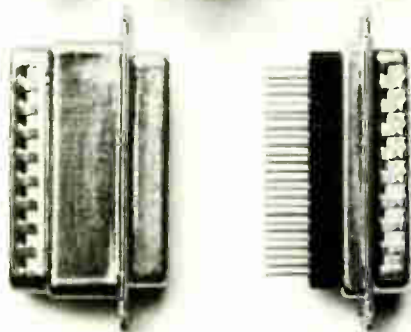
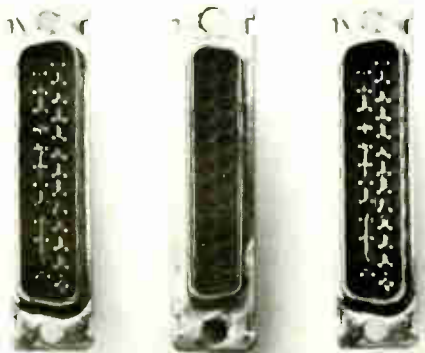
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Washington newsletter

E-l-f still favored as alert for submarines

The Navy's plan to develop a laser satellite system by 1986 for emergency communication with missile-launching submarines is now in trouble. Newly released congressional testimony shows why: Pentagon and congressional officials believe that the costly laser system offers no clear conceptual advantage over the Navy's large ground-based extremely low-frequency (e-l-f) radio system, being built in the upper peninsula of Michigan and Wisconsin. Donald R. Latham, deputy under secretary of defense for command, control, communications, and intelligence, told a House Defense subcommittee that although both e-l-f and the laser system are troubled by slow data rates, **the blue-green laser has an additional handicap: it is essentially useless in bad weather and stormy seas.** Limited e-l-f operations, set to begin next year, will use a "bellringer" system—a continuous signal that alerts commanders to a possible emergency if it stops. Navy sources say that this feature is meant to discourage surprise attacks against e-l-f sites. In a national emergency, either system would be capable of sending submarines one of only three coded commands: surface to receive detailed information at other frequencies, remain submerged on alert for 24 hours, or launch missiles.

Westinghouse gets FAA radar contract

In its first major air-traffic-control procurement in two decades, the U. S. Department of Transportation has awarded Westinghouse Electric Corp.'s Defense and Electronic Systems division of Lithicum, Md., a \$480.5 million contract to replace the Federal Aviation Administration's obsolete vacuum-tube radars. **The five-year project calls for proven technologies rather than state-of-the-art designs,** reports Guinn Clark, marketing manager for air-traffic-control systems at Westinghouse. Slated for installation at 137 sites by the end of 1985, the radars are based on an array-signal processor that performs 30 million instructions per second. With this processing power, an air-traffic control system can detect small low-flying aircraft not equipped with transponders. There will be a separate channel for weather data.

FCC urged to decentralize spectrum assignment

The Federal Communications Commission should get out of the business of assigning slots in the radio spectrum nationwide and establish instead a new service **that would vest assignment powers in the hands of local government and operators.** That is the recommendation of a commission staff report now circulating within Washington's communications community. "The FCC centralized regime is slow to react to change. . . . Increasingly, technology must be proved out in the laboratory to the nth degree before it is licensed," lament the study's two authors, Kenneth Gordon and Alex Felker, both electronics engineers in the Office of Plans and Policy.

In the deregulated framework they propose, local governments would grant licenses to operators who would be free to choose the types of services offered on their channels. The FCC's role would be limited to requiring applicants to engineer a system guaranteeing protection from interference. The interference standard for low-power TV stations—based on outputs, that is, signal-strength contours—should serve as a model of how protection can be achieved with a minimum of technical regulations, asserts the study.

White House plans to computerize Federal bureaucracy

Computers will be applied to nearly every Federal operation by 1988 in an effort to streamline the nation's bureaucratic machinery. Labeled Reform 88, the program has identified nine projects that the Administration predicts will **save the equivalent of \$2,000 per American over a six-year period**. Three of the most important projects are fully automated budgeting—from formulation through final congressional appropriations—in every agency, enlargement of a telecommunications network for electronic mail among and within all Government departments, and standardization of the 332 incompatible accounting systems. Another project, the modernization of cash-management practices by electronic funds collection and disbursement, is expected to generate between \$2 billion and \$3 billion in interest savings over a three-year period; that, along with other improvements, will provide the wherewithal to make Reform 88 a self-financed initiative.

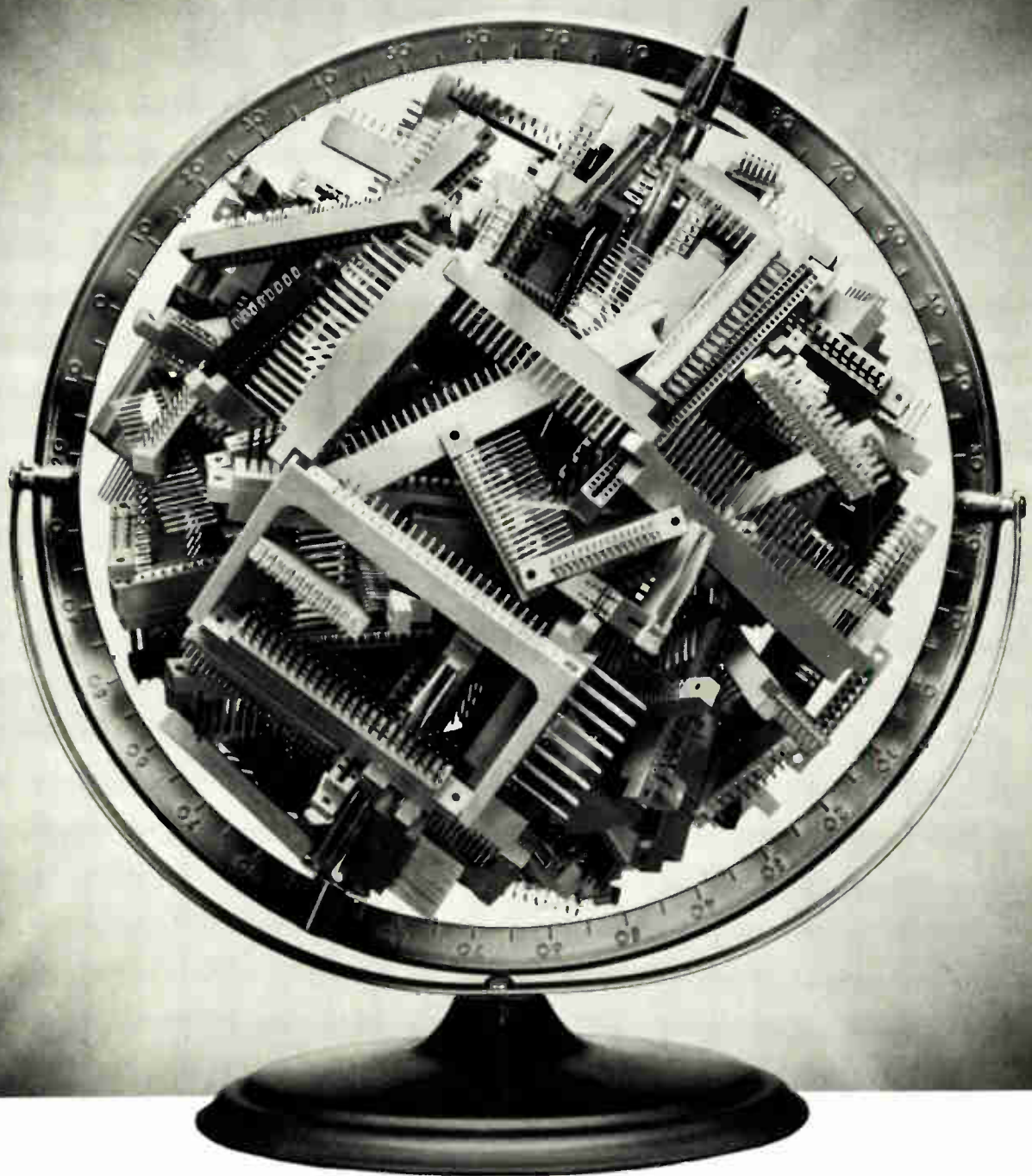
AT&T's rivals unite to oppose access plan

Eight long-distance carriers have called on the Federal Communications Commission to reconsider and revise a Jan. 1 order that will double the interconnection costs they pay to hook into American Telephone & Telegraph Co.'s local lines. In a letter to FCC chairman Mark S. Fowler, top officers of such firms as MCI Communications Corp., GTE Corp., and Satellite Business Systems maintain that **the 1984 impact of the FCC plan would be a "devastating" pretax operating loss of up to \$721 million**. By contrast, they say, maintenance of the current access-fee arrangement, under which they pay from 65% to 75% less than AT&T for inferior connections, would mean pretax income of \$484 million. The FCC plans the fee hike in anticipation of phone-line upgrades to give all long-distance carriers equal access to the nationwide net. The ultimate result of the plan, concludes the letter, "would be a return to a monopolization of the interchange market by AT&T, making the coming division of the Long Lines/BOC [Bell Operating Company] transmission enterprise a totally futile and senseless action."

Addenda

Bending under pressure from U. S. officials who are considering not renewing a 2½-year-old telecommunications trade agreement, Nippon Telegraph & Telephone Public Corp. says it **will more than triple its purchases of American equipment this year to \$140 million**—about 15% of what the U. S. industry currently buys from Japan. The top items on NTT's list include an advanced \$64 million telephone traffic and management system from AT&T International and a \$21 million supercomputer from Cray Research Inc. . . . At the same time, NTT **has asked U. S. industry to bid on research and development contracts for four new products in the areas of fiber optics for high-definition TV and integrated services and one- and two-way video-communications terminals**. . . . The Federal Communications Commission has granted the first license for an operational cellular radio system to Chicago SMSA Limited Partnership, which after Jan. 1 will be 93% owned by Ameritech Mobile Communications Inc., made up of former Bell operating companies. With regard to approving the service in medium-sized and small markets, **the FCC wants to use a lottery**.

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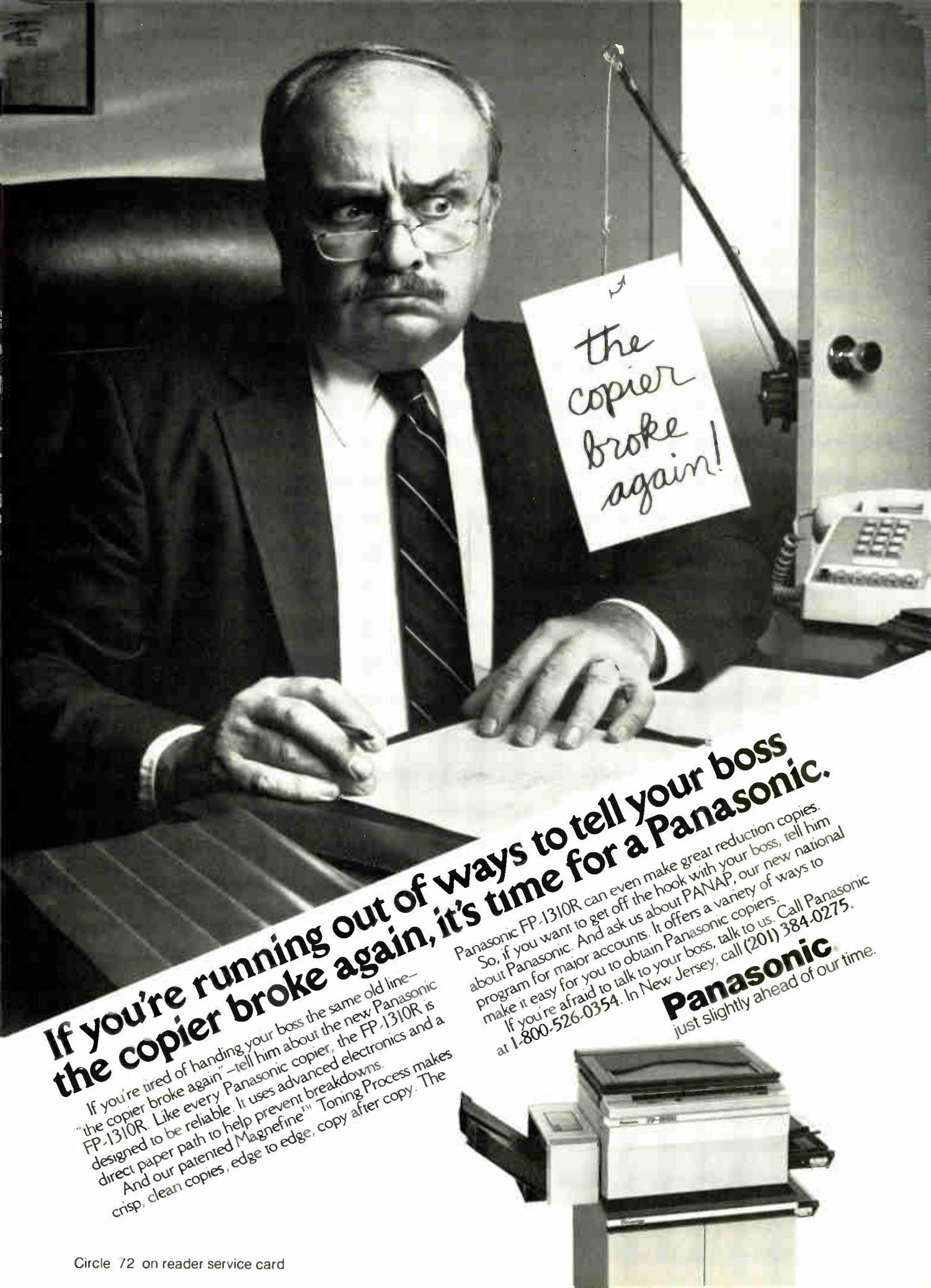
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The EDAC logo consists of the letters 'EDAC' in a bold, green, sans-serif font. The letters are closely spaced and have a slight shadow effect, giving them a three-dimensional appearance.

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Circle 71 on reader service card



the copier broke again!

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Sellers of computers, systems and software will meet their buyers in **Electronics' Special Report: Artificial Intelligence.**

November 3 Issue.
Closes October 10.

This Special Report will put the flood of claims about Artificial Intelligence into perspective, because management needs to know how AI will affect them and their companies. What part of AI technology can realistically be applied now and in the near future? The report will cover hardware, languages, programming environments and high-level system building tools. There will be an analysis and evaluation of where AI R&D and technology transfer is headed. And the report will look inside the AI technology workshop, breaking through the "science fiction" of some claims for intelligent software to give you a realistic view of AI engineering.

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Sellers of robots and the sensory instruments, computers, systems and software that support them will meet their buyers in **Electronics' Special Report: Robotics.**

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The new workers punching the time clock at modern factories have arms of steel—literally! Robots are bettering the way manufacturers make products through smart sensors, programming languages, and computer-backed control systems. These servo-driven workers give new meaning to accuracy and quality. Manufacturers who use robots, especially in electronics, are pushing the development of off-line programming, vision and tactile sensing. The robot arms range from snake-like welders to precise articulated 3- or 4-axis units with accuracy around 1 mil. The computer will exploit these accuracies.

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TUESDAY NOVEMBER 15, 1983
INTERNATIONAL ROUND TABLES

New trends in integrated circuits

Chaired by Mr. Jacques BOUYER, President of SITELESC and EECA,
the 1983 International Panels are organized by:

- SITELESC - French Active Components Manufacturers Association,
and co-sponsored by:
- EECA - European Electronic Component Manufacturers Association,
- EIAJ - Electronic Industries Association of Japan,
- SIA - Semiconductor Industry Association (USA).

PANEL 1

Shifts in product structure and in significance of software to the microelectronics industry.

The trend to higher complexity, lower prices, larger production volumes is likely to prevail more than ever during the years to come for the Integrated Circuits world industry.

Equipment makers will similarly keep on designing in their new products larger numbers of new and advanced ICs.

Both ICs and equipment makers will have to build in their respective products more intelligence than in the past, following somehow the same evolution as the data-processing industry has experienced in the past decades.

This Round Table will estimate the foreseeable growth rates of these main Integrated Circuits families. It will survey the growing capital requirements of the industry and the increasing use of software in design, manufacture and use of Integrated Circuits.

Chairman: Dr. OUCHI Atsuyoshi
Senior Executive Vice-President and Director:
NEC - JAPAN

PANEL 2

Availability and training of skilled microelectronics personnel

Demand for skilled engineers and technicians at ICs manufacturers, ICs users and Research Institutions levels is likely to continue increasing exponentially in the years to come.

Imbalance between demand and availability challenges the education community as well as the industry post-education personnel training abilities.

This Round Table aims first at quantifying the problem and then at appraising the existing and proposed solutions.

The Round Table will endeavour to assess the respective present and expected positions of the key microelectronic geopolitical areas such as Western Europe, USA and Japan vis-à-vis this most vital and critical domain of the microelectronics revolution.

Chairman: SIA Chairman

Simultaneous translation: English/French/Japanese - Registration Fee: FF 900 net rate

West Germany tries to make up for lost time in aiding electronics . . .

Trying to make up for past neglect, West Germany has begun an ambitious program in venture-capital spending to help young high-technology companies in electronics get off the ground. Toward that end, a deal is in the works whereby **West German and U. S. venture-capital firms will raise more than \$50 million**, both at home and abroad, to establish Techno Venture—the biggest West German industrial venture fund to date. A major contributor is Siemens AG, the country's largest electronics group, which has already put about \$8 million into the pool and says it will give engineering know-how to the young firms without influencing their operations. Techno Venture, to be administered by Siemens as well as by financial groups in Munich, Boston, and London, will support West German start-up companies in components communications, data processing, automation and process control, medical electronics, and measuring technology.

. . . and funding production technologies to recapture lost markets

The Bonn government is also concerned over the loss of West Germany's once-dominant position in machine tools and the slow acceptance of computer-aided design and manufacturing techniques by small companies there. It has decided, therefore, to sharply step up the funding of production technologies, robotics, and CAD/CAM. About \$208 million has been earmarked for the period from 1984 to 1987, **more than a threefold increase over what was spent in this sector during the previous four-year period**. The Ministry for Research and Technology does not intend to support individual projects as it has. Instead, it will aid firms that show competence in specific fields but lack broad research-and-development activities to compete on world markets.

ICL net to test open-systems standards

The separate strands of ICL plc's networking strategy for linking digital private automated branch exchanges and an ICL local network will be drawn together in a test site at the Edinburgh Regional Computing Centre. Paired with a Mitel digital PABX at the center, an Ethernet-based system will support layer-4 transport protocols—as defined by the European Computer Manufacturers Association in accordance with the International Standards Organization's open-systems interconnection model—and will be used to test such emerging international standards. **It will also support a gateway to Edinburgh University's X.25 packet-switching network** and be used to evaluate voice- and image-messaging technology. Planned are a voice server that digitizes voice messages and plays them back on demand, as well as a multifunction laser printer that can double as a facsimile terminal. Terminals will be able to access a dual ICL 2976 or a Digital Equipment Corp. VAX-11/750.

Million-bit-plus ROM fits on 8-mm-square chip

NEC Corp. has packed more than a million bits into what it claims is the world's largest read-only memory designed for the 24-by-24-dot-matrix kanji-character generators finding their way into office automation and similar products. The 1,244,160-bit n-channel MOS chip, configured as 103,680 words by 12 bits, is used for direct addressing. Two of the new integrated circuits replace nine 256-K ROMs and some external logic in popularly priced systems. Advanced 1.75- μ m design rules made it possible to fit this large capacity onto a chip measuring only 7.81 by

7.42 mm and to achieve the respectable access time of 250 ns. Delivery of samples starts at year-end; mass production will begin in March. At the same time, the firm will start taking orders for parts programmed to customer specifications.

Further in the future the firm will produce a low-power complementary-MOS version of the ROM for **printers, battery-operated computers, and hand-held educational units**, including translators and character-learning units. Access time will be about an order of magnitude slower, more than sufficient for intended applications—but the use of series, rather than parallel, circuits will enable this even more complex design to fit on a chip measuring 7 mm on a side or less.

Comecon ministers urge revitalizing stagnant industry

Comecon's Standing Committee on the Telecommunications and Electronics Industries, made up of ministers or vice ministers of the member countries, is moving to rationalize the sophisticated but stagnating East European electronics industry. Meeting at Balatonszeplak, Hungary, **the committee resolved to set up a uniform component base, including standardization of production technology, and extend specialization and technical-scientific cooperation among the member countries.** It also called for development of a new generation of color TV sets, studio equipment, cable TV, video-cassette recorders and video-disk players, as well as a uniform switching and digital-transmission system, and for setting up production of high-purity metals and chemicals for the electronics industry.

Olivetti arranges Japanese production of portable computer

Ing. C. Olivetti & C. will soon add an in-house-designed but Japanese-produced portable computer to its product line. Designated the Olivetti M 10, the machine is based on the Intel 80C85 microprocessor and **has from 8-K bytes to 32-K bytes of random-access memory and an eight-line liquid-crystal display.** The M 10 can dialog with the Ivrea, Italy, company's M family of desktop and minicomputers, and will be available with an optional newly designed modem and printer. Olivetti will test-market the computer in Italy and Belgium later this year, and introduce it to the U. S. market sometime in 1984. The M 10, which measures 30 by 5 by 21 cm and weighs 1.7 kg, will sell for about \$750.

16-K-byte MSX computer to cost \$200 to \$300

Seven Japanese manufacturers will start marketing compatible low-cost home computers in late October at prices ranging from \$200 to \$300 for a computer with at least 16-K bytes of random-access memory and Microsoft's 32-K-byte extended Basic in read-only memory. The machines will all adhere to the MSX hardware and software standard [*Electronics*, June 30, p. 48]. The seven companies—Matsushita, Toshiba, Sony, Sanyo, Mitsubishi, Nippon Gakki, and Hitachi—will aim their machines at elementary and junior-high-school students. They expect to sell 100,000 units in Japan before year-end, 500,000 units in 1984, and twice that in 1985. **Software houses also expect an exploding market and plan to increase MSX-compatible software from the roughly 30 programs now available to 500 by the end of the year.** Exports to the U. S. should start in time for Christmas 1984.



WHOSE TESTERS DO THE LEADERS USE FOR THEIR HOTTEST MEMORIES?

In the fiercely competitive memory market slight variations in testing efficiency can make the difference between winning and losing. The leading memory manufacturers and users have long chosen Megatest systems because they are simply the most efficient, most reliable, and most versatile systems available.

Now Megatest's newest test system, the Q2/52, equips these manufacturers with an even more effective solution for the challenges of tomorrow's memories.

For the huge memories of the future, the Q2/52 provides a 4 megaword address space

and 16 data channels in a multiprocessor test station built for speed. For maximum throughput it tests four dynamic RAMs in parallel. For improved yields it tests and repairs memories with redundant elements and provides a wide spectrum of yield analysis and characterization software. And for even broader application its 4 additional I/O channels handle pseudo-static RAM, self-timed EEPROM and other devices combining memory and logic elements.

The Q2/52 — part of a system of tools, technology and support, keeping the leaders ahead.

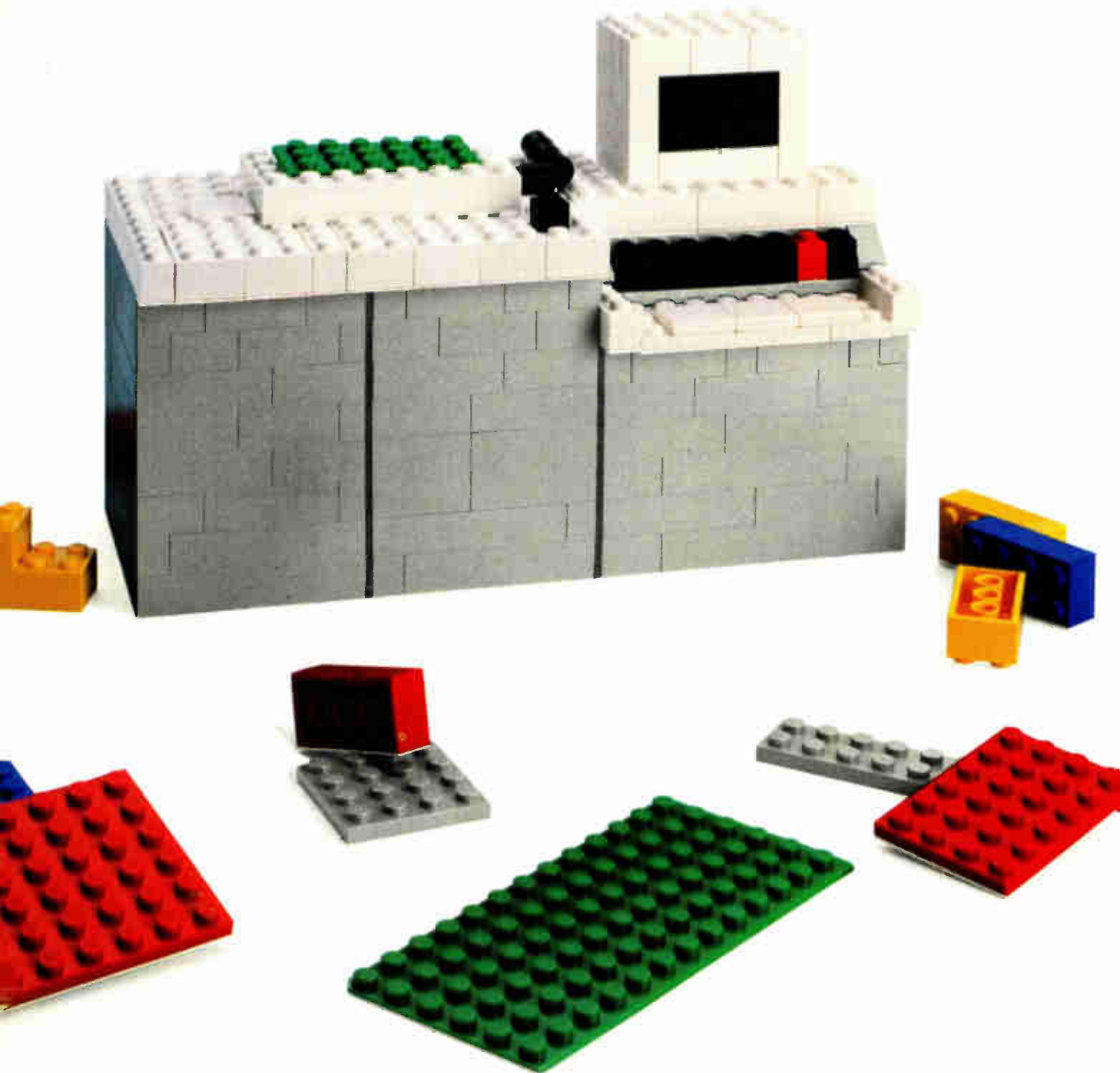
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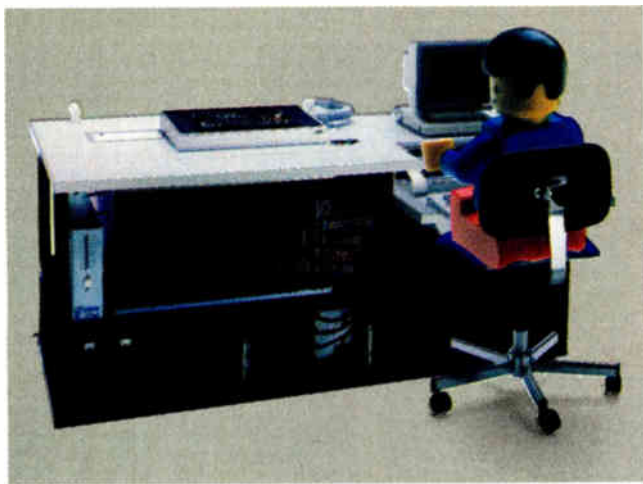
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Somebody did.

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Consequently, you don't need multiple test systems to meet your specialized board testing needs.

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Built around a 68000 CPU and the UNIX® operating system, the 850 delivers up to twice the throughput of conventional testers. Program generation is quicker. User programs run faster. Debug time is reduced. And multi-user response time is slashed.

The modular architecture of our state-of-the-art Analog Test Module (ATM™) allows you to add a variety of advanced special function sub-modules. It has the frequency range and resolution to test high impedance RLC components. Its high level programming language delivers simplified test transistor BETA checking.

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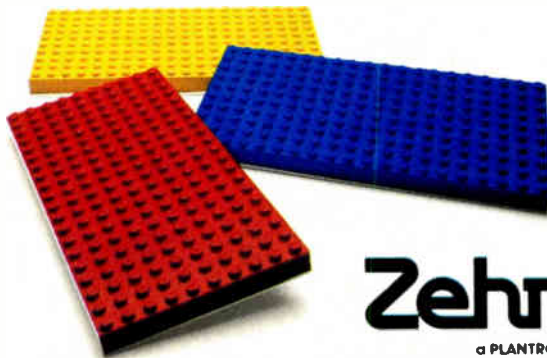
On the outside, the 850 is designed with the user in mind. The programmer workstation is a comfortable desktop height. And all operator controls are located in an easy-access central control panel. The display monitor is portable. The programmer's keyboard is detachable. And the uncluttered tester surface easily accommodates board handling robotics.

Of course, the 850 is compatible with our advanced automatic program generator, PRODUCER2,™ as well as all past and future Zehntel 800 Series test systems and our Factory Automation Products. Like our 700 Net Workstation,™ Paperless Repair Stations and 600 Robotic Board Handling System.™

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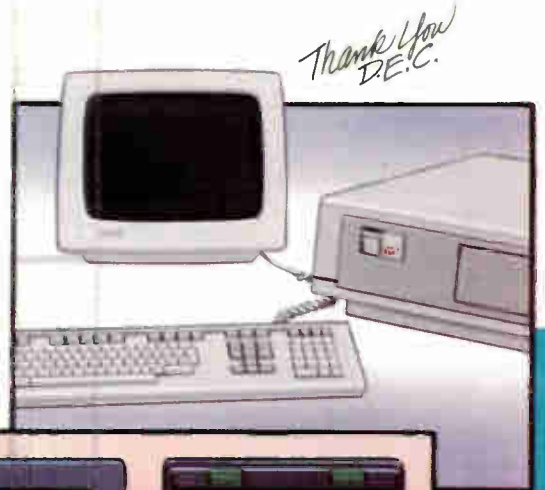
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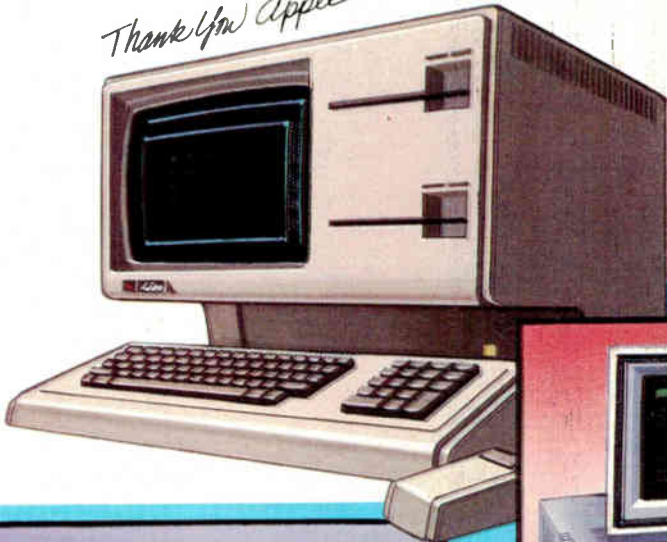


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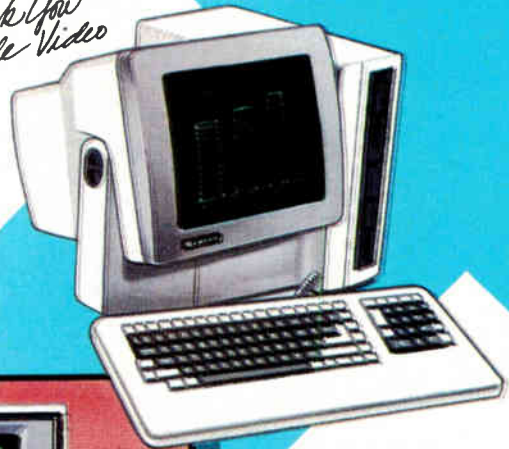
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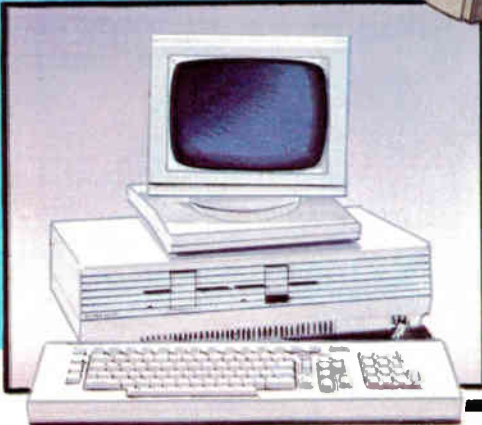
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Jerry R. Crowley
President, OKI Semiconductor

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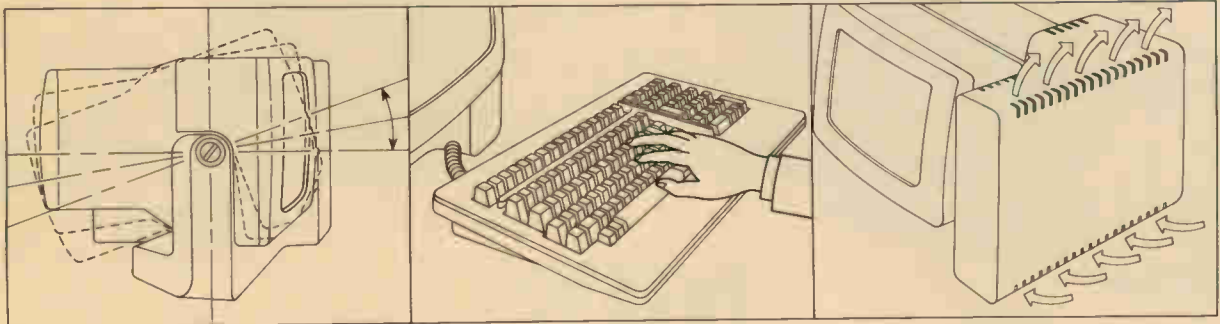
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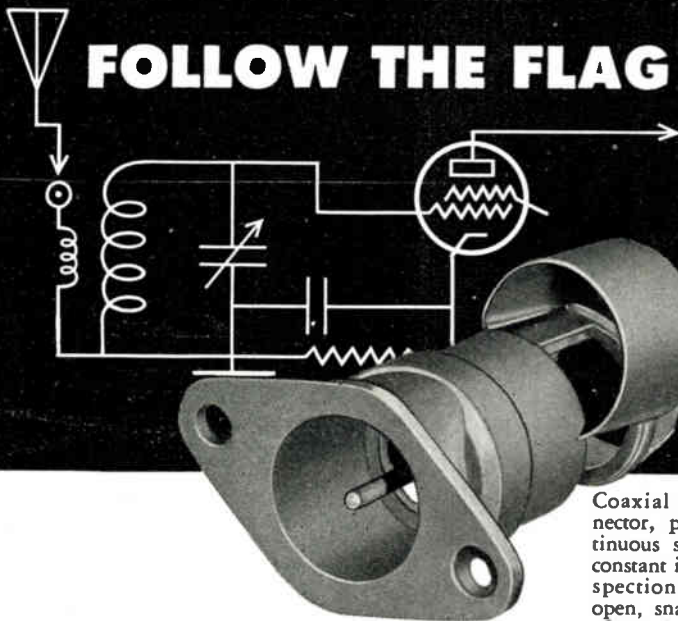
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tive with respect to the cathode to cut off anode current and the target fluoresces all around. When the contacts touch, the grid of the tube is made positive with respect to the anode and target, anode current flows and a shadow appears on the target.—Mills, *Review of Scientific Instruments*, February, 1941, p. 105.

Casting Tester

CERTAIN METAL CASTINGS may be tested for cracks or other imperfections by striking them with a hammer and comparing the "ring" with that of a similar casting known to be perfect. The value of such a test depends to a large extent upon identical suspension or mounting of sample and standard castings, striking of both with the same force at the same relative point and the accuracy with which differences in sound pitch can be distinguished.

Suspension of samples and test castings may be made uniform by any one of a number of mechanical means which need not be mentioned here. Uniformity of striking point and power may be solved by using rigidly positioned and mechanically or electrically driven hammers. Sound output at a given standard pitch may be measured by feeding the "ring" into a microphone mounted a fixed distance from the hammer, amplifying the microphone output by an a-c amplifier equipped with a band-pass filter designed to accept the standard frequency only and, finally, operating an output meter giving a visual peak reading. *Electronic Control Corp.*, *ELECTRONICS*—February, 1939, p. 25.

Vibration Burglar Alarm

THE VIBRATION ACCOMPANYING an attempt to cut or break through a property boundary fence, or vibration induced in a fence from the ground by attempts to tunnel beneath or jump over a fence, or vibration of a fence by sound waves produced in the vicinity of the fence, can be transmitted along the rails or other inter-connecting members of the fence for a considerable distance. Such vibration may be used to actuate an electronic alarm circuit, a vibration unit converting me-



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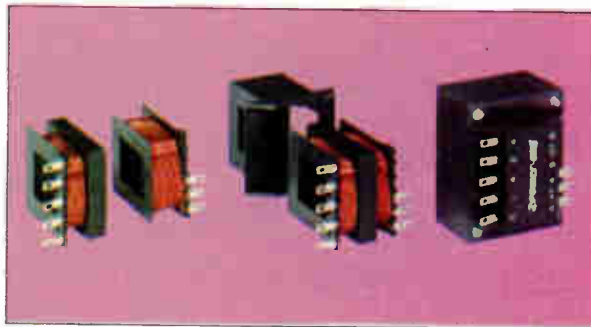
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Local network links machines that are incompatible

by Kevin Smith, Senior Editor

Philips scheme distributes protocol-conversion facilities throughout the nodes of a packet-switched network

There are two ways of bridging a language barrier: either the participants in the dialogue find a common tongue or they converse through an interpreter. In the world of data processing—currently a morass of many different communications protocols—it is no different. So for its wide-area network, intended to link incompatible systems, Philips Telecommunicatie Industrie BV, Hilversum, the Netherlands, has chosen the second route: distributing protocol-conversion facilities throughout the nodes of its new packet-switched communications network.

This scheme means, for example, that a Digital Equipment Corp. terminal could address an International Business Machines Corp. computer or a Philips word processor through Sopho-net, as it is called, without any software modifications. Eventually, Philips plans to support major *de facto* communications protocols, starting with IBM's Systems Network Architecture and DEC's DECnet.

At the same time, however, Philips is keeping a watchful eye on the ideal goal of establishing a universal language for the data-processing community. The best known of these initiatives is the International Standards Organization's seven-layer open-systems interconnection model for computer communications, and indeed the Philips Communications Network Structure is broadly based

on the OSI seven-layer model.

However, J. C. Leanard, chief engineer of Project Telesoft, Philips Telesoft International, Brussels, who has headed up the software development for Sopho-net, thinks the ISO model still faces grave problems when it comes to practical implementations. "It's impossible to avoid a tower of Babel," he says.

Stumbling blocks. True, companies such as Britain's ICL plc and France's Bull have based their networking strategy on the OSI model. However, Leanard says that, even when there is general agreement between manufacturers, differences of detail could still prevent one system from talking to another.

Even where there is a well-defined goal, as in the European Computer

Manufacturer Association's standard for the transport layer 4 of the ISO model, detail differences between manufacturers will hamper interconnection. Nonetheless, Philips intends to support the ECMA layer-4 standard as soon as hardware becomes available in significant quantities.

But there are more fundamental problems with the ISO model, says Leanard. It had divided the full spectrum of processing and communications activities in such a way that usually only the adjacent layers in its seven-layer model interact unless peer-to-peer communications is used. Indeed, the model draws a clear separation between processing and communications domains above layer 4.

There are thus three basic layers in the data-processing domain. The

APPLICATION ORIENTED		
OPEN SYSTEMS INTERCOMMUNICATION STRUCTURE	PHILIPS' COMMUNICATIONS NETWORK STRUCTURE	
LAYER	INFORMATION DOMAIN (APPLICATIONS)	
7. APPLICATION		
6. PRESENTATION		
5. SESSION		
COMMUNICATION ORIENTED		
4. TRANSPORT	COMMUNICATION DOMAIN	END-TO-END ERROR RECOVERY AND FUNCTIONALITY FLOW CONTROL
3c. NETWORK	TRANSFER DOMAIN	GLOBAL ADDRESSING, ROUTING, AND CONGESTION CONTROL
3b. NETWORK		SUBNETWORK ENHANCEMENT
3a. NETWORK	LOCAL NETWORK DOMAIN	PACKET DOMAIN (X.25 ONLY) SUBNETWORK ACCESS
2. DATA LINK	LINK DOMAIN	
1. PHYSICAL	PHYSICAL DOMAIN	

Compartmented. Philips' implementation of the ISO model solves the problem of data-processing and -communications activities in which only the adjacent layers in the seven-layer model interact.

Dismantling the Tower of Babel

Philips Telecommunicatie Industrie BV, Hilversum, the Netherlands, is targeting its new wide-area network at the large corporation spread over several geographical locations that needs to integrate all its communications resources into a single network. Sopho-net also provides a gateway to public carrier services such as Telex, Teletex, videotex, and facsimile. It operates over any data-communications medium, whether private- or leased-line or public data network. Additionally, the transmission resources can include any public switched telephone network, a private automated branch exchange, or one of the many newly developed local networks.

Each network node employs a multimicroprocessor architecture, so processing power can be matched to the traffic load, typically processing up to 1,500 packets per second. Node transit times for packets are typically less than 20 milliseconds, thus causing very little delay in response times. For smaller areas, Philips will be offering its Sopho-lan, a broadband local network to be launched at Telecom '83 in Geneva later this month. Sopho-net will interface with this, as it will with other wide-area offerings. —Kevin Smith

top is the user application layer 7, which is concerned with the details of the data-processing function being performed at the time. The presentation layer 6 is intended to provide device independence by the use of virtual-device protocols, be they displays, printers, or card readers. And the session layer 5 provides the needed protocols for controlling dialogue.

A merging. That is the system in theory, but in many applications such as Teletex—basically a super Telex service—it is impossible to distinguish between the application and presentation layers or in data-base applications to separate the session and presentation functions. “We do not believe that there is a significantly important common set of functions which is of general applicability,” says Leonard.

So Philips has discarded the three-layer approach, substituting instead a set of single vertical protocols which are application-specific—Teletex and data-base applications, for example.

That is not to say that Philips does not see a role for the ISO model. “It provides a measure of the difference between systems,” says Leonard. As do other interested parties, he says the ISO debate does provide a clear basis for discussion between manufacturers towards the goal of seeking for data processing the same universality that the telecommunications industry achieved generations ago.

The Netherlands

Electron beam writes 10 billion pixels/s

A writing speed of 10 billion 0.1-micrometer picture elements a second is the promise of an electron-beam pattern generator now in the predevelopment stage at the Delft (Netherlands) University of Technology's department of applied physics. The prototype is expected to process about a hundred 4-inch wafers per hour with a 0.1- μm resolution and a 0.5- μm minimum line width for typically complex very large-scale integrated-circuit structures.

With their apparatus, the Delft researchers will reach the specifications of the U.S. government's VHSIC (very high-speed IC) program. They say the most advanced electron-beam pattern generator now in practical use is the EL-3—a vector-scanning variable-spot-size system from International Business Machines Corp. This machine has a throughput of twenty 3-in. wafers/h at 1- μm line widths and 0.25- μm resolution.

The key to the high pixel rate is a matrix of 32 by 32 beamlets into which the source beam is split. The multiple beam so obtained is raster-scanned across the wafer. A raster

scan sweeps across the entire wafer, with the beam gatted on in desired pattern areas; vector scanning is slower because it jumps for one pattern area to the next, requiring a wider bandwidth for the data-processing system.

“Beam splitting is about the only way of overcoming the limitations imposed by physics on obtaining a 0.1- μm resolution at a particular beam current,” points out project leader Rob Roelofs. These limitations are set by the interaction of electrons with one another. The impact of this interaction is large in a single, large electron beam, where there are many electrons pushing each other away and so limiting resolution, but it is less if many smaller beams are used.

Spotlets produced. In the Dutch system, each of the 1,024 beamlets produces a 0.1- μm pixel, or spotlet. Thus, the maximum surface area exposed in one flash is 3.2 by 3.2 μm . As the beam scans across the entire chip surface, each beamlet covers a 1- μm -square area.

The beamlets may be individually blanked by computer command and the distance between spotlets set by adjusting the lenses. The 10-billion-pixel/s rate assumes a resist sensitivity of 10 microcoulombs per square centimeter and a maximum total beam current of 30 microamperes.

The Delft machine, Roelofs says, contrasts with multiple-beam equipment being investigated in the U.S., in that it uses an optical column in which the spotlets of the matrix are blanked individually instead of one that writes in parallel fashion. The result is a more flexible machine with a higher throughput.

Multiple-beam imaging is accomplished with gauze lenses in the optical column. Typically, a gauze consists of a platinum or gold-coated stainless-steel plate 0.25 cm square and 0.1 millimeter thick. The plate contains a matrix of 32 by 32 holes, each roughly 0.1 mm in diameter, and is installed in the electrostatic lens between the electrodes.

Beamlet blanking is accomplished with an array of 32 by 32 beam deflectors arranged on a plate. Each



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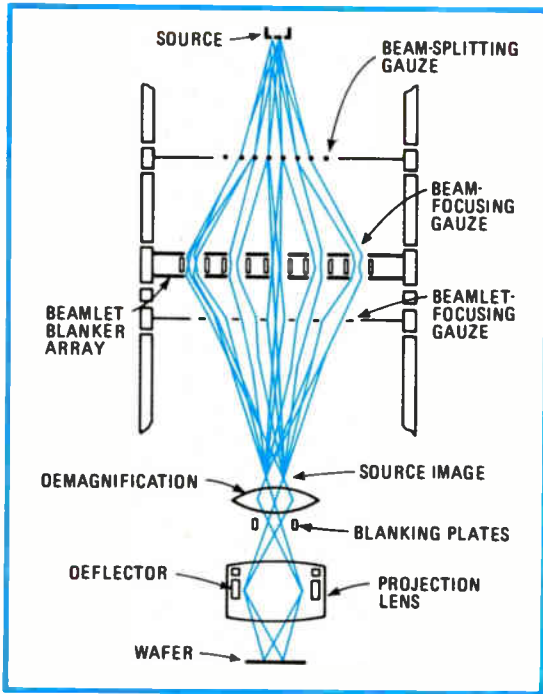
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Individualist. Electron-beam machine uses an optical column in which beamlets are blanked individually, instead of being used for writing in parallel fashion.

deflector consists of a pair of small electrodes between which an electric field can be set up through which the beamlets normally pass. Under computer control, voltages are applied to the deflectors in accordance with the pattern to be written. These voltages act to deflect a beamlet away from the aperture, thus blanking it.

In an electrostatic lens without a gauze, a converging-lens effect is always obtained. When the gauze is installed between the electrodes, the alteration of the electric field results in a diverging-lens effect. However, the individual holes in the gauze act like converging lenslets. These lenslets focus the beamlets, while the direction of the beamlets spreads out.

The spherical aberration of a gauze lens can be corrected by inducing a proper charge distribution on the gauze. This can be done by subdividing the lens electrodes and applying a correction voltage to each subdivision, Roelofs says. Therefore, large opening angles are possible without an increase of the focal length, thus reducing the electron-electron interaction that would otherwise limit the resolution.

In the Delft machine (see figure) the first gauze lens follows the high-brightness 100- μ A electron source. It creates a multiple image of the source and, by virtue of its diverging effect, spreads the beamlets to provide space for the deflectors.

A second gauze lens, one with a converging effect, focuses the beamlets through the deflector array. There they may be either blanked or passed through (depending on the voltage applied to the deflector plates).

A third gauze lens, again with a diverging effect, brings the images into coincidence in the aperture plane of the final lens system. Consisting of a demagnification lens, a deflector, and a projection lens, this system produces a demagnified image of the gauze holes on the wafer. —John Gosch

France

Spectral encoding ups transmissions

A team of French engineers has come up with a scheme for multiplexed transmission by encoding signals into spectral information that could significantly increase the number of transmissions possible in optical communications systems. The technique's principal advantage is that it can be used in addition to standard wavelength multiplexing, thus offering a potential bonus in communications capacity.

To be described at the European Conference on Optical Communications in Geneva, Oct. 23–25, the technique is called spectral coding because the coding process disturbs the continuous spectrum of white light so that what is received is a spectrum with certain tones missing,

or a channel spectrum. This term, however, is purely descriptive. The technique translates light into intensity variations that can be detected by a photodiode.

Developed at the Laboratoire de Physique Générale et Optique of the University of Franche-Comté in Besançon, the scheme has already transmitted TV images with a bandwidth of 6 megahertz both in free space and using multimode optical fibers some 12 meters long.

According to Jean-Pierre Goedgebuer, the engineer who is coordinating the project, the maximum number of messages that can be multiplexed using the technique is a function of the luminance of the light source.

Light choice. The laboratory realization uses an incoherent-white-light source, though Goedgebuer asserts it could be adapted without difficulty to light-emitting diodes and diode lasers. For white light, he says, the multiplexing technique might piggyback 10 messages onto the signal usually carrying but one, because only a tenth of the light's total power is needed to send a single message.

In addition to the light source (which emits light with a carrier wave that can be modulated), the emitting end of the system consists of a quartz crystalline plate and an electro-optical modulator (see figure). Because the source is incoherent, polarizers are added, though these would be unnecessary for operation with lasers.

The system is based on the Pockels effect that describes the directly proportional influence of the intensity of electrical fields on certain crystals. In operation, this means that the emitter's modulator behaves as a two-beam interferometer by splitting every incident wave-group—a segment of the incident light that corresponds to the wavelength of the carrier signal—into two twin wave-groups separated by a time interval proportional to the voltage applied to the electrodes of the modulator. The carrier signal is coded by phase modulation of the white light at the output of the emitter.

At the receiving end, birefringent

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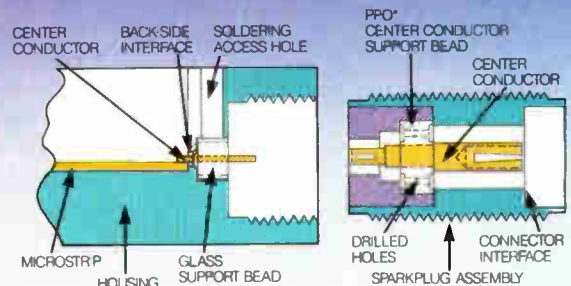
Assembly of K Connectors on the 0.118 inch diameter semirigid cable is similar to that of SMA. Transmission loss is less than 14 dB per foot at 40 GHz.



The kit contains one 10-inch straight cable assembly, one 5-inch 90° bend cable assembly, two female sparkplug launchers, four glass beads, one thru-line assembly with two sparkplug launchers, one 10-inch piece of coaxial cable, and two unassembled male K cable connectors.

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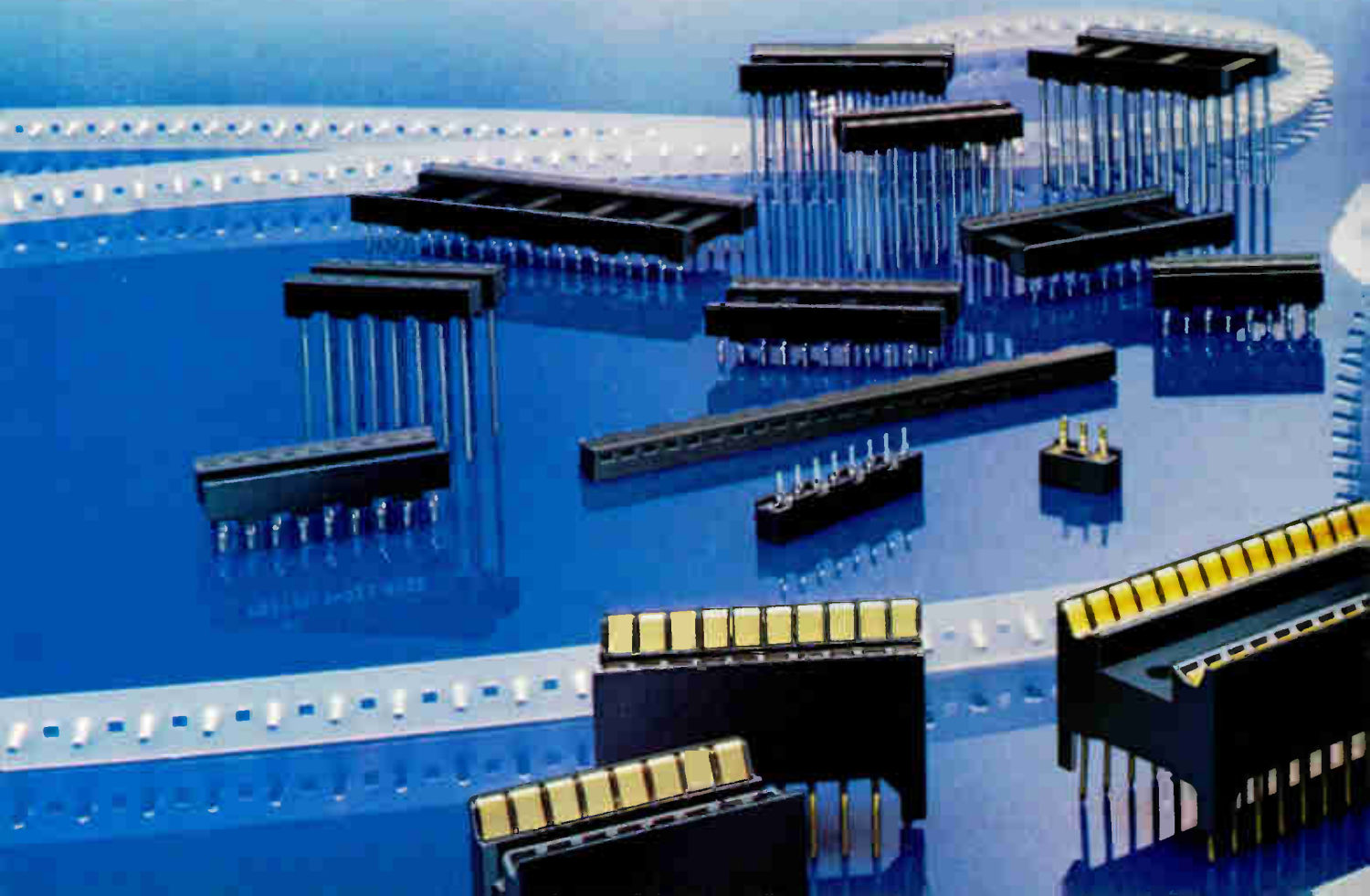
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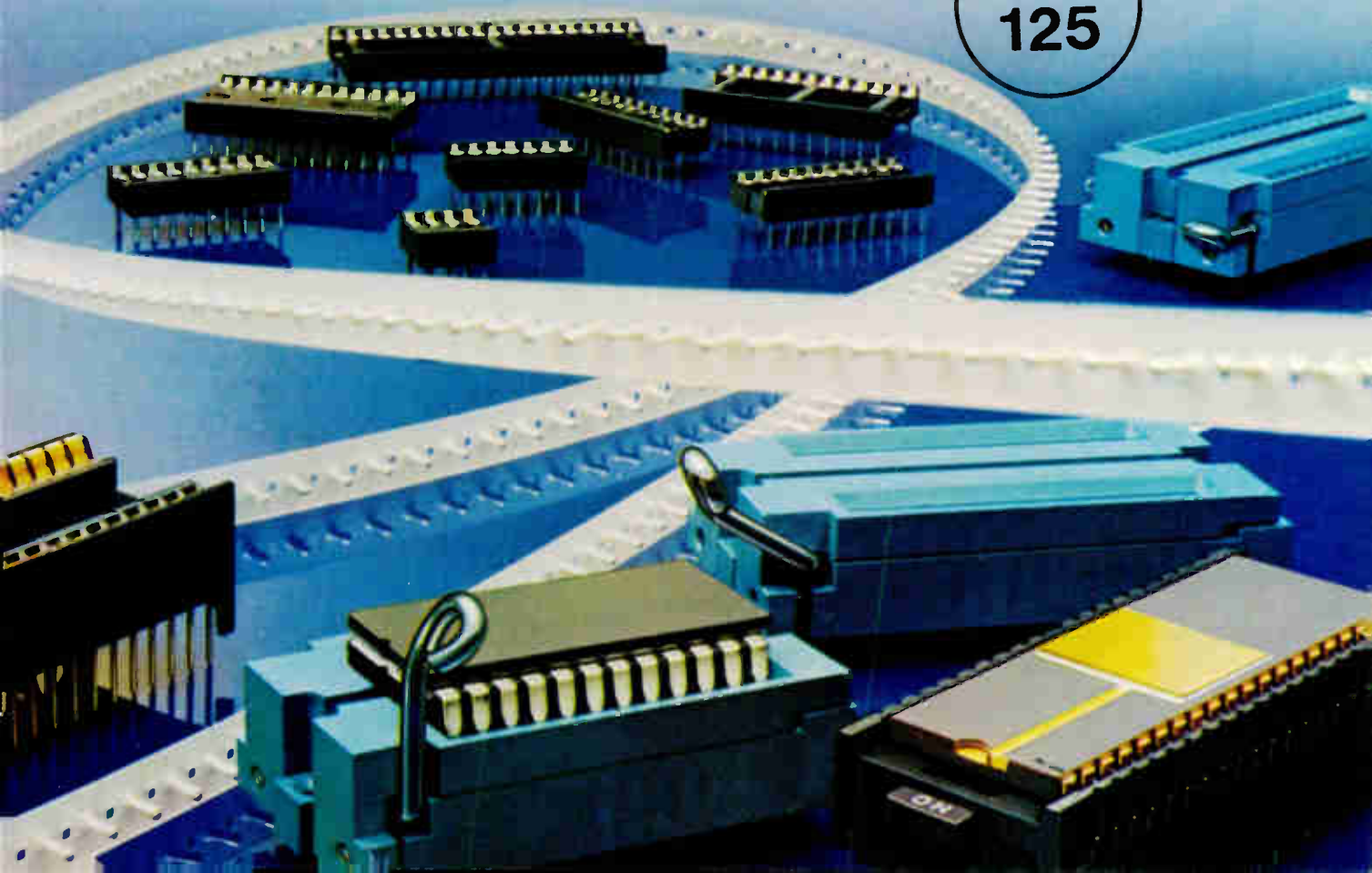
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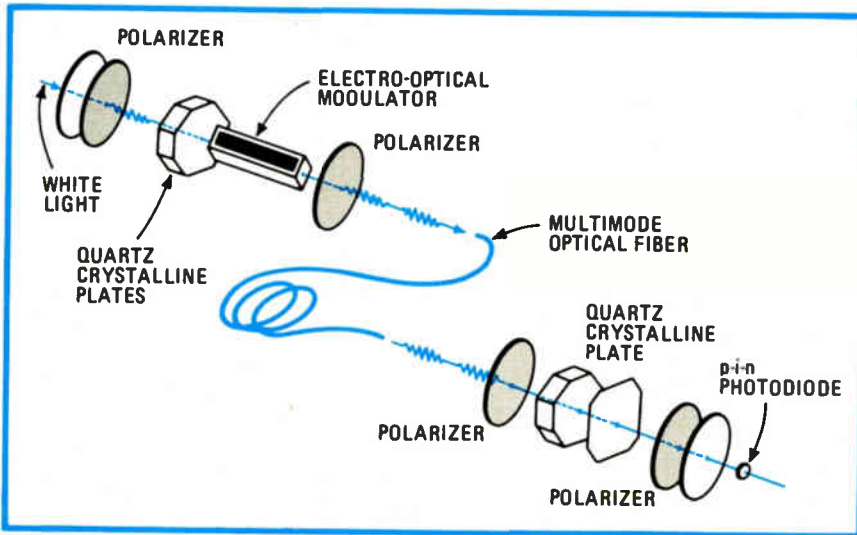
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Bright. Scheme for multiplexed transmission by encoding signals into spectral information translates a white-light source into intensity variations to be detected by a photodiode.

quartz plates act as a spectroscop to permit decoding by spectral analysis of the light. A p-i-n photodiode converts the phase modulation of the white light into intensity variations proportional to the original voltage applied at the modulator, thus allowing detection of the message.

Wave groups. Multiplexing of the signal is carried out by using sets of birefringent quartz plates and transverse electro-optical modulators. At the output of an emitter sending, say, two messages, coding would be in the form of four twin wave-groups, each with its proper path difference proportional to the voltage applied to its respective modulator.

At the decoder, the beam of light is divided using a beam splitter, after which birefringent quartz plates introduce time intervals tuned on the emitter intervals. The messages are reproduced simultaneously and are detected as variations in light intensities.

—Robert T. Gallagher

Japan

Teletext service takes first step

Experimental teletext broadcasts unveiled earlier this month are intended as the Japanese trailblazer for an ambitious nationwide service. Teletext is

expected to be an important factor in what the Japanese call the "new media market"—interactive TV, home computing, high-fidelity component systems, and the like.

The initial service, offered in Tokyo and Osaka by public-service broadcast network Japan Broadcasting Corp. (NHK), is directed at the hard-of-hearing and consists of eight programs daily, mostly national and local news, weather reports, program announcements, and dramatic shows. Teletext material is scanned and transmitted in the form of binary pulse signals, which are inserted during two lines of the vertical blanking interval in the NHK TV signal.

In the Japanese system, there are 284 horizontal scanning lines on each channel, and teletext signals can be inserted into the gaps between signals on the NHK channels. There are five display modes: full-page, vertical and horizontal scrolling, and superimposed and subtitled, which can be used with conventional TV shows.

The present system has a transmission rate of 5.727272 megabits per second—relatively slow compared with Western systems, but, unlike Western systems, the Japanese must transmit complex ideographs and fine graphics, so the pattern-transmission method was selected. The graphics system being used is based on one developed by the Nippon Telegraph & Telephone Public Corp.

for its Captain videotex system.

The Ministry of Posts and Telecommunications, which is directing the project, is researching a more efficient transmission system combining code- and pattern-transmission characteristics. "The hybrid system will give us 5 or 10 times the broadcast capacity we now have," says Makoto Yoshimuro, deputy director of the engineering division in the broadcast department, Ministry of Posts and Telecommunications. This project will take three to four years, he said, and within 10 years, "we shall have a broadcast capacity of between 400 to 800 teletext programs on a single channel."

All alone. Until further research is completed and a standard system adopted, NHK will be the only TV network in Japan offering teletext. However, NHK and several private networks are already involved in an experimental network that will result in general service when the new hybrid system is ready.

NHK says about 16 million homes (11 million in the Tokyo area and 5 million in Osaka) can receive the teletext service, for which a special adapter is needed. Every major Japanese electronics firm markets an adapter, priced at about \$460, but because the Japanese system is not compatible with those in use abroad, there are no export plans at present.

The new media market in Japan is still in its early stages, but a recent study by the respected Nomura Research Institute, Tokyo, forecasts a 1990 market in Japan of \$11 billion and in the U. S. of \$38 billion.

The report predicts that within seven to eight years sophisticated home entertainment systems would make up 40% of the new market, with home terminals (electronic files and in-house information-transfer equipment), in-house communications systems, home clerical and study equipment (family accounting systems, programming language converters, and voice-input typewriters), and hi-fi video equipment (high-definition video-cassette recorders, animation production systems, and VCR editing machines) also making a strong impact.

—Michael Berger

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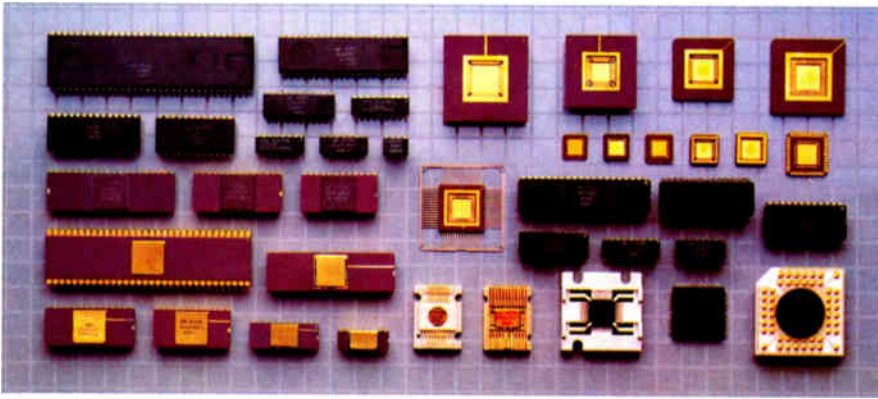
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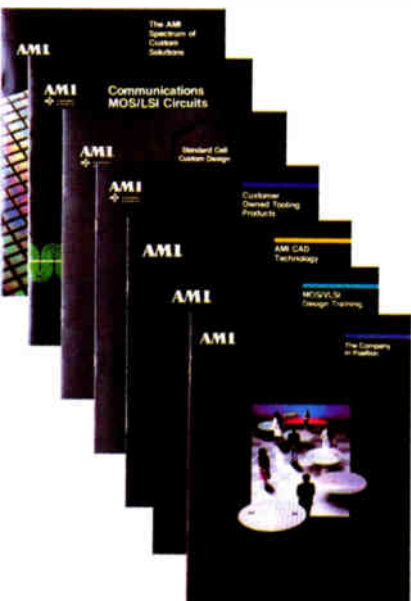
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VLSI, computer designers swap ideas

Computer-design conference to explore the leading edge of ICs, computer architecture, CAD, and processes

by Roger J. Godin, Solid State Editor, and Tom Manuel, Computers & Peripherals Editor

It has become a commonplace that developments in very large-scale integrated circuits have an impact on computer design. But it is equally true that new ideas in both hardware and software architecture influence VLSI. That is the rationale behind a conference bringing together the leaders of these disciplines to discuss the state of the VLSI art in computers: the International Conference on Computer Design: VLSI in Computers, which the Institute of Electrical and Electronics Engineers is putting on Oct. 31 through Nov. 3 at the Rye Town Hilton, Port Chester, N. Y., north of New York City.

In addition to the main program of more than 170 papers in 48 sessions, there will be several promising panels and four keynote speakers. Keynoters are Kaneyuki Kurokawa, vice president of Fujitsu Ltd.; Paul Low, vice president of International Business Machines Corp.'s General Technology division; Alan Kay, vice president and chief scientist at Atari Inc.; and Yuichiro Oya, general manager of Hitachi Ltd.

Top technical managers from leading companies will sit on panels on supercomputers (Burrroughs, Control Data, Cray Research, Honeywell, IBM, Sperry, and Trilogy) and VLSI (AT&T Bell Laboratories, Digital Equipment, Fairchild, Hewlett-Packard, IBM, Siemens, and Texas Instruments).

Sessions exploring the leading edge of several technologies will include advances in VLSI computer-assisted design, artificial intelligence in CAD, Josephson junctions and quiteron devices, advanced work stations, complementary MOS technologies, and the impact of VLSI on architecture.

In recognition of the difficulty of managing the complexity presented by VLSI circuits, prodigious efforts have been made to improve the efficiency of CAD aids.

Four areas—IC technology, circuit and computer design, computer-aided design, and computer architecture—will receive thorough coverage. The many papers on these subjects attest to progress: they will be delivered in fully 50% of this year's ICCD sessions.

These projects appear to have two major focuses. The first is interactive-design systems that use a common data base for the entire design-to-production cycle. The second major focus is the need for regularity in fundamental VLSI circuit structures, in order to facilitate automatic layout and verification.

International Business Machines Corp.'s Los Gatos (Calif.) Laboratory highlights the advantages of interactive design in VLSI CAD in two dedicated sessions on Thursday afternoon (see table below). The first session is dedicated to a detailed

description of the IBM logic-simulation machine. A dedicated, highly parallel hardware system for simulation of VLSI chips—the LSM, as IBM calls it—works in conjunction with a Series 1 interface computer and a 3081 mainframe to evaluate 64,512 logic expressions at a rate of 640 million expressions per second. Such speed means that VLSI designs can be simulated completely in seconds, which allows engineers to make changes and experiment with alternative designs in real time and greatly increases the odds of first-pass success.

The session closes with a paper covering several actual examples of the machine's benefits when it simulates both systems and chips, as in use of the LSM to simulate an entire memory tester containing 12 megabits of system memory and 64 control boards, each holding more than 1,000 logic gates. The result is a machine free of design errors.

New tools. Another session highlights IBM's efforts to develop advanced software tools for interactive-

INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: PROGRAM OUTLINE

	Technology	Design	Computer-aided design	Architecture
Tuesday morning	Very large-scale integration technology	VLSI testing	VLSI placement Automated technique	Custom architecture Impact of VLSI
Tuesday afternoon	Arrays	Design concepts Packaging	Work stations	Residue number Real-time systems
Wednesday morning	VLSI technology; VLSI/mass storage	VLSI verification VLSI evaluation	Physical design	Chip architecture VLSI logic design
Wednesday afternoon	Complementary MOS	VLSI simulation	Artificial intelligence	Digital systems
Thursday morning	Josephson junctions	Design steps The IBM machine	CAD and VLSI	VLSI architecture Tradeoffs in design
Thursday afternoon	Novel design issues	High-level aids VLSI architecture	Interactive design VLSI logic design	Computer architecture Signal processing

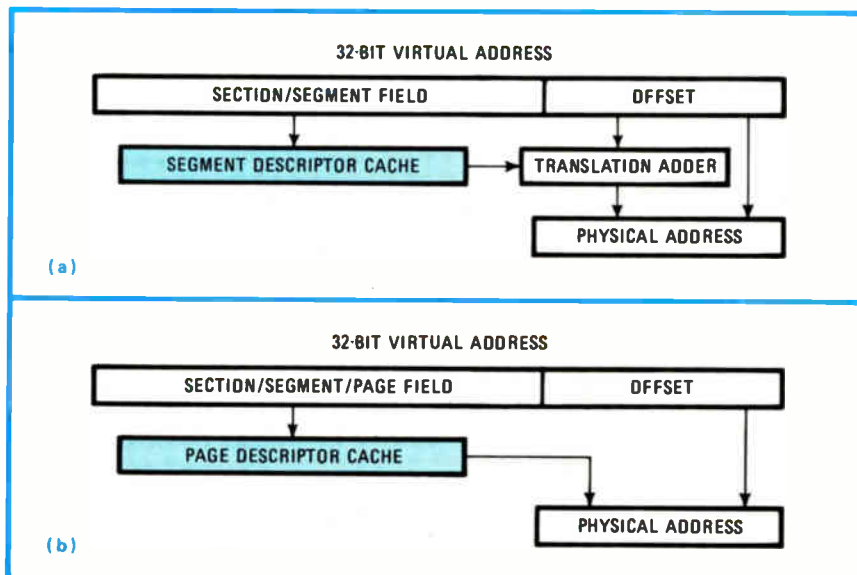
Probing the news

IC design. To further enhance productivity, these tools are integrated into an overall IC-development environment where the data base for high-level schematic description is used at all levels of design, including simulation, verification, placement, and layout. A key feature of the interactive-design language is its technology independence, as when a microprocessor designed with the language was realized in custom n-channel MOS, master-slice n-MOS, and a TTL lab version.

AT&T Bell Laboratories, Murray Hill, N. J., also has VLSI CAD tools to give pause to some potential competitors of its parent, AT&T Western Electric. First, in Tuesday afternoon's design-concepts session, M. R. Buric, C. Christensen, and T. G. Matheson will present a paper on PLEX, a program written in C that automatically generates layouts for VLSI single-chip microcomputers based on user-specified data-word size, register count, and instruction- and data-memory size. From a user's high-level specifications, PLEX produces the complete mask-level layout of the central processing unit, as well as read-only and random-access memory. Examples for 8- and 16-bit chips will demonstrate throughput rates that run between 6 million and 8 million instructions per second.

On Wednesday morning, K. W. Wu, also from Bell Labs, will lead a session on physical design devoted to papers outlining various verification aspects of Bell's layout and extraction programs. The highlight promises to be the discussion of HCAP, an analysis tool that extracts connectivity and parasitic-device from layout artwork. The program is technology-independent and allows users to define subcircuits, of arbitrary size and complexity, that do not need to be completely analyzed, thereby speeding overall execution.

As a striking example of its design-system capability and VLSI C-MOS process technology, Bell Labs will present the work of a team of engineers that resulted in the design and first production of an advanced memory-management unit for the Bellmac-32. The 100,000-transistor



Address-change request. The memory-management device for Bell Labs' Bellmac-32 features two virtual-to-physical address translations on chip for contiguous and paged segments.

device was built with 2.5- μm twin-well C-MOS to minimize latchup; it features titanium silicide gates to reach 8-megahertz speed, with some units hitting 15 MHz.

Using the design system described in the other sessions, the design time from proposal to fully functional units was only 10 months. With a dual-data-path architecture and three on-chip cache memories configured as a 32-bit segment-descriptor cache, the MMU chip supports both paged and unpagged segments, multiple users, and a protection scheme using one type of privilege for each of four accessibility levels. Translations from virtual to physical addresses are done in two ways in order to handle contiguous- and paged-memory segments (see figure).

Next generation. Nor are next-generation tools being ignored at ICCD. Anticipating the orders-of-magnitude improvement in speed-power products that semiconductor technologies will need for fifth-generation computers, scientists from the process research and development labs of semiconductor companies and systems makers will debate the status and relative merits of advanced bipolar, C-MOS, gallium arsenide, and Josephson-junction processes. Special emphasis goes to C-MOS, for its near-term importance, and Josephson technology, for the potential it holds for the future.

Beyond the latest information on

advanced IC processes, those attending the conference will have an opportunity to see VLSI's impact on computer architecture. In a session Tuesday morning, P. Schenk of the National Aeronautics and Space Administration's Goddard Space Flight Center, in Greenbelt, Md., will present a cause-and-effect case study on the center's new massively parallel processor (MPP).

Eight elements. A custom chip with eight processing elements is the basis for the machine, which has a 128-by-128-processor array. With 16,384 1-bit processing elements capable of 6 billion additions per second, the MPP was designed and built by the Goodyear Aerospace Corp., Akron, Ohio. It was then delivered to NASA in May; the agency uses it to process images from the Landsat-4 satellite, where each frame contains more than 10^8 bits of data.

VLSI's impact on computer performance will also be discussed in that session, in a paper on MIPS, for microprocessor without interlocked pipe stages, a single-chip microprocessor developed at Stanford University, Palo Alto, Calif., by a team led by John Hennessy.

With the computer geared for high-speed execution of compiled code, the compiler directly encodes the microengine with a streamlined instruction set. Pipelines are used, but software, not hardware, controls interlocking. \square

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Optical memory

Optical memories stampede to market

A developing need for mass-storage media and optimistic forecasts for sales are spurring a flood of product introductions

by J. Robert Lineback, Dallas bureau

Envisioning mass-storage applications that will soon outstrip today's magnetic media in capacity, the producers of laser-based optical-disk systems are continuing apace with product introductions this fall. The point is to heat up the new memory market and take an early lead in 1984. By some estimates, nearly 50 companies worldwide are going for a piece of this market—which is expected to climb as high as \$10 billion by the early 1990s.

Announcements of new products in Japan preceded those from a number of U.S. and West European manufacturers—including Storage Technology Corp., Shugart Corp., and Philips Information Systems Ltd. Still more are slated before the end of the year. Next month's Comdex '83, in Las Vegas, is expected to spotlight nearly a dozen new and recently introduced systems. Early in 1984, Control Data Corp., Minneapolis, will unveil a single-platter unit able to store a gigabyte of data on a 12-inch disk.

So far, the embryonic market has split into two camps: read-only-memory drives (for software distribution, electronic publishing, and distributed data bases) and nonerasable direct-read-after-write, or DRAW, drives (generally targeted at archival storage). Although a few erasable-disk drives have appeared, most market analysts agree that DRAW and ROM optical-storage systems will be the mainstays until the late 1980s.

The first generation of removable

digital-optical-storage units will feature write-once media, with laser beams marking and reading tiny spots on platters. Using DRAW techniques, the systems are expected to carve out entirely new archival applications. By the decade's end, second-generation erasable optic-storage systems are expected to begin stealing sales from conventional magnetic storage—especially tape drives.

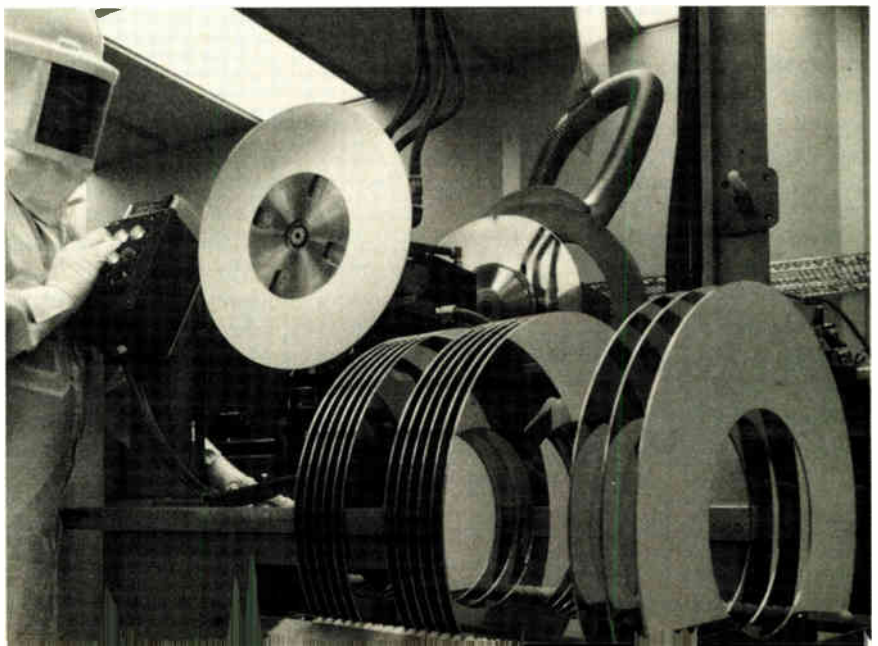
As for bit density, optical mass storage outperforms conventional magnetic media by as much as 100:1. With disk diameters varying from 2 to 16 in., the laser-sensitive platters introduced so far can hold up to 4 gigabytes of data—roughly 40 times a magnetic-tape reel's capacity. Furthermore, data stays intact for at least a decade without refreshing, and some manufacturers claim a shelf life of up to 40 years.

In Longmont, Colo., Storage Technology—which plans to begin limited shipments in December of its 7600 optical-storage subsystem [*Electronics*, Sept. 22, p. 42]—is looking for

explosive growth in large-computer-system markets. Selling for \$130,000, the 7600 can store 4 gigabytes on one side of a 14-in. platter by using a diode laser to increase the reflectivity of 1-micrometer spots on a polished tellurium-based disk. A helium-neon gas laser is used to read those marks as 1s and 0s. Volume shipment begins in the second quarter of 1984.

Next year, Storage Technology expects its optical-storage sales to yield revenues of \$100 million, increasing to \$1 billion in five years. Also producing the 14-in. DRAW medium is Du Pont, of Wilmington, Del., which will spend \$10 million on a pilot line for second-sourcing the disks.

Backing away. But not all views of optical storage are that bright. Last spring, Burroughs Corp. dropped a development program after spending \$20 million [*Electronics*, April 21, p. 41]. Officials at the Detroit-based firm believe it is impossible to produce a reliable medium for high-performance applications at prices competitive with magnetic storage. Bur-



Protected. Introduced this month, Shugart's Optimem 1000 protects its medium with a plastic sleeve. Here, a cartridge is being removed from the uncovered drive.

Probing the news

roughs is continuing basic optical-storage research, however.

Melissa Yonge, market analyst with Venture Development Corp., of Boston, predicts that companies will concentrate on sales in their own countries before exporting systems. Optical mass-storage growth, she thinks, initially will lag behind the optimistic growth projections coming from some systems manufacturers. But Venture Development estimates that U. S. sales of DRAW systems in the mid-1980s will grow about 300% annually, reaching \$3 billion in 1987.

Inertia factor. San Francisco optical-storage consultant Edward Rothchild also believes the immediate hurdle for system vendors is the inertia associated with bringing new technology into markets. He estimates that the total U. S. market for optical storage products will exceed \$5 billion by the end of the 1980s and account for about two thirds of worldwide demand. "It could hit that number before the end of the decade," he says, adding that this year's flurry of new products spurred an upward revision of his figures.

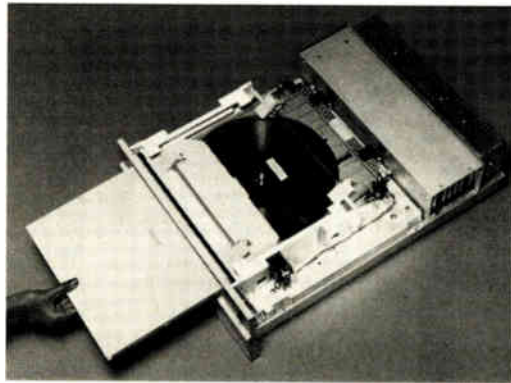
Furthermore, Rothchild thinks the difficulty in achieving higher magnetic-bit densities through promising perpendicular-recording techniques "seems to be creating a marketing window for erasable, reusable optical-storage media." Perpendicular storage has already enjoyed some success, increasing bit densities tenfold over conventional magnetic methods. The window for erasable-optic products will close around 1990, says Rothchild, who expects that perpendicular recording will eventually place magnetic-storage density levels near those of optical memories.

Paired techniques. To gain erasability in optical storage, most companies are trying to combine perpendicular magnetic recording with optical storage, known as magneto-optics. Most believe erasable-optic sales will account for about half the total market in the 1990s, with write-once drives preferable in applications needing audit trails.

This month, Xerox Corp.'s Shugart operation, in Sunnyvale, Calif.,

pulled the wraps off its optical drive, the Optimem 1000, which can store a gigabyte of information—equal to 400,000 pages of text—on one side of a removable 12-in. platter. Shipments are expected to begin in the first quarter of 1984, with volume deliveries following in the third. In quantities of 250, the Optimem 1000—which is 7 in. high, 19 in. wide, and 24 in. deep—will sell for \$6,000.

For the domestic market, Dallas-based Philips Information Systems, a subsidiary of NV Philips Gloeilampenfabrieken, of the Netherlands, has



Clean. This Storage Technology Optical Media Unit is being built in a class-10 clean room, comparable to those in which space-program parts are assembled.

introduced the Megadoc system, which can store as many as 128 gigabytes of data on line inside a "juke box" that automatically handles up to 64 12-in. disks. The optical-storage unit, which will be made in Colorado Springs through a Philips-Control Data joint venture, will be attached to a high-speed image scanner, display terminal, and printer for document-storage applications.

The scanner converts documents into optical-storage data by way of bit-mapping techniques (4 million pixels per page). One side of the disk contains a gigabyte of user storage. An entry-level Megadoc system sells for \$250,000.

North American Philips, in New York, is also readying a compact disk—similar to the 4¾-in. audio-laser disks that are being sold in the recording industry. The CD ROM, which is expected to hit the market next year, can hold 525 megabytes of formatted data. A 2-in. erasable magneto-optic read-write drive continues to be under development in Philips' European labs.

The U. S.-based firms that are in the course of developing and offering optical media for a range of storage systems include Drexler Technology Corp., of Mountain View, Calif. (offering media for disk, tape, and credit-card film strips); 3-M Co., of St. Paul, Minn. (which is doubling capacity at its Mountain View, Calif., facility); and Eastman Kodak Co., of Rochester, N. Y. (which uses a photographic-like polymer-dye-binder medium).

Staying home. Meanwhile, in Japan—where optical memories for document storage and retrieval have seen a great deal of activity—firms are concentrating first on domestic markets before exporting technology to foreign markets. Matsushita Electric Industrial Co. claims to have 400 orders for a system it introduced a year ago. The fully configured document system, including printer, scanner, and terminal, sells for about \$48,000. One gigabyte can be stored on a single-sided 20-centimeter platter.

Toshiba is offering three document-filing systems using optical disks that hold 1 gigabyte of unformatted data per side. The firm sells the optical-disk system by itself—double-sided for about \$200 and single-sided for about \$120. Hitachi Ltd. expects to sell 3,000 of its write-only optical-document-filing systems in Japan. The system's 30-cm disk stores 1.3 megabytes of data per side and can hold document and computer data on both sides. A minimum document-storage system sells for about \$44,000.

In two years, Sony Corp. expects to start selling an erasable magneto-optical disk it developed jointly with Kokusai Denshin Denwa Co. [*Electronics*, Oct. 6, p. 84]. Sharp Corp. also has a prototype of an erasable magneto-optic system using 13-cm disks with 150 megabytes of unformatted storage. The firm hopes to start marketing the system in Japan next year. In March, NEC Corp. began selling office markets in Japan an optical-disk drive along with its 6300 intelligent terminal [*Electronics*, April 7, p. 75]. □

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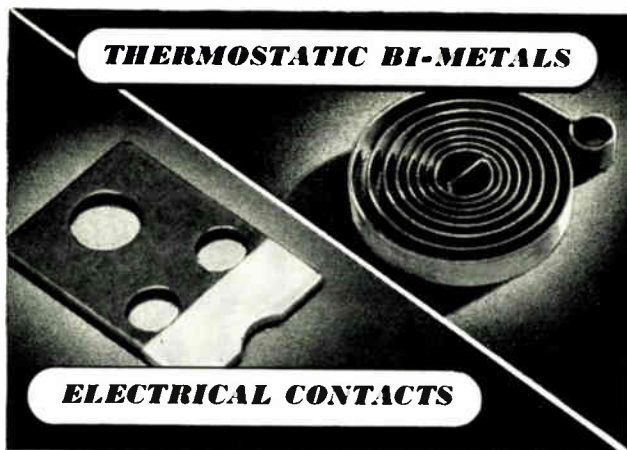
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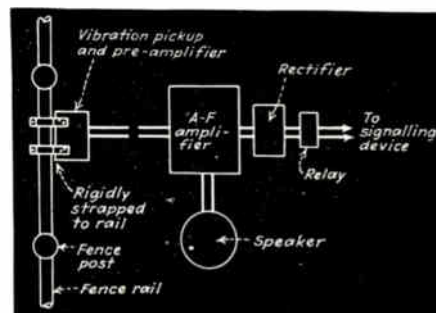
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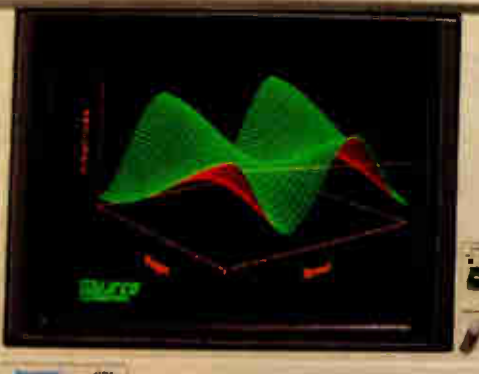


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Europeans rush into telecom alliances

Moves forced by union of communications and data processing
and the increasing cost and complexity of product lines

by Robert Gallagher, Paris bureau manager

Geneva, whose very existence depends on international encounters, could hardly be a more appropriate place to hold Telecom '83. Of course, the hardware will be more sophisticated this time (Oct. 26–Nov. 1) than it was at the last conference, four years ago. The other significant change is the fact that many companies then fiercely competitive have since become allies.

The reason is clear: data processing and telecommunications are merging in private data and communications networks and in the public integrated-services digital network (ISDN). Not even the largest corporations can offer the complete product lines needed to compete in a market complicated by complex standards dictated both by governments and international organizations.

These pressures gave birth to such agreements as the one between AT&T and NV Philips Gloeilampenfabrieken, as well as to marketing and licensing accords for key products like

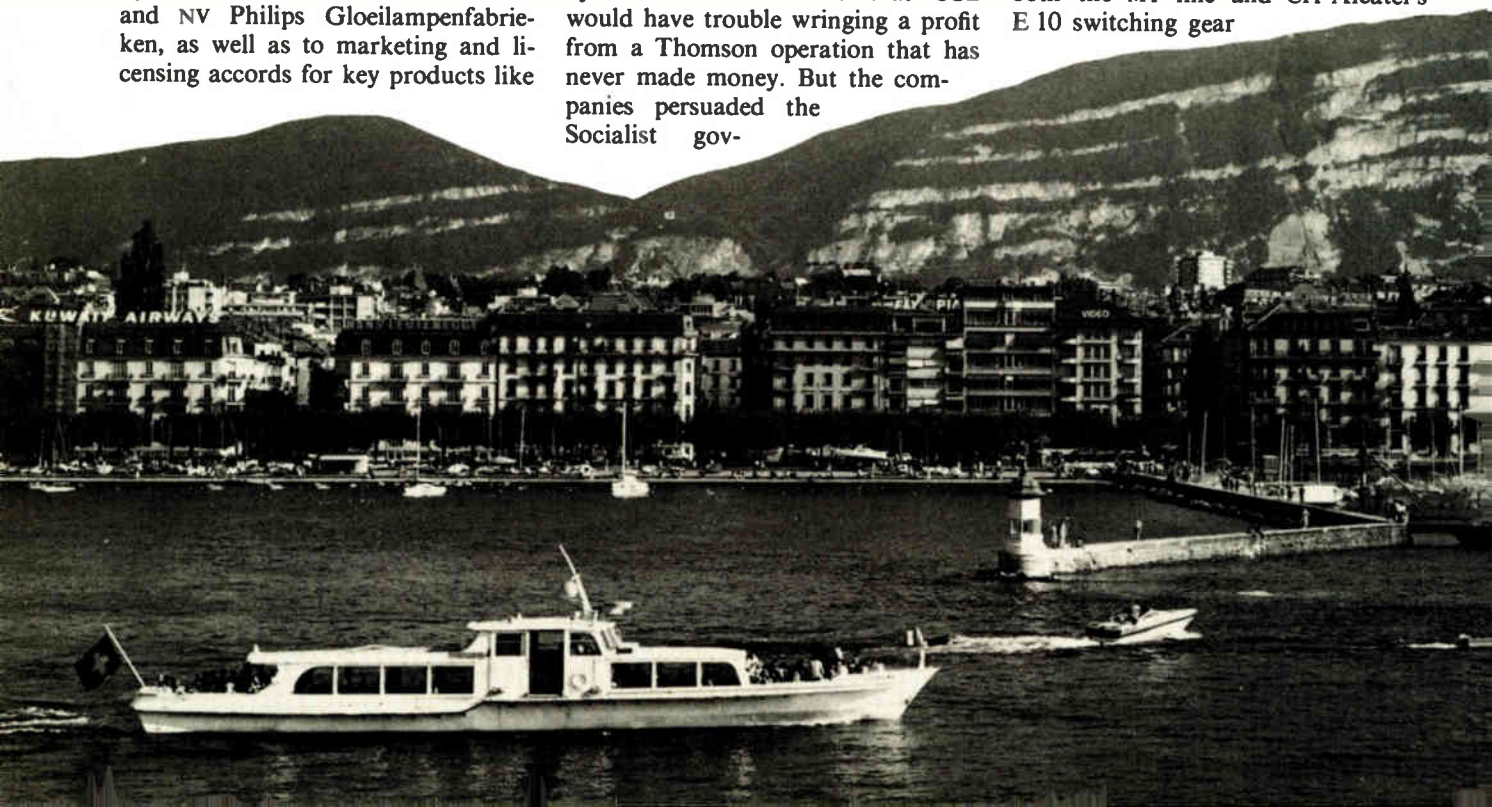
digital private automatic branch exchanges and packet-switching systems. Says one industry executive: "If you think we've seen a lot of strange bedfellows getting together in the last couple of years, wait until you see the next few years."

By far the most dramatic alliance in Europe was the recent all-French affair, in which Thomson-CSF's failing telecommunications activities were merged with the profitable efforts of CIT-Alcatel, the Compagnie Générale d'Electricité subsidiary that produces digital switches. The result was the fifth-largest telecommunications-equipment producer in the world.

Pair needed. The move generated strong resistance from the French telecommunications agency, which wanted two domestic suppliers of digital switches. It was also criticized by observers who felt that CGE would have trouble wringing a profit from a Thomson operation that has never made money. But the companies persuaded the Socialist gov-

ernment's industry ministry. "It is impossible for French industry to remain passive when faced with recent agreements like those between AT&T and Philips, L. M. Ericsson and Honeywell, and IBM and Rolm," asserts Georges Pebereau, CGE's managing director, who hammered out the accord with Thomson's president, Alain Gomez. "Our priority must be to achieve that critical size where we can compete on the worldwide market."

Several years will be needed to consummate the Thomson-CGE marriage. For the moment, Thomson will be pressing ahead to meet orders for its MT family of digital switches, a product line plagued by technical hitches. The company claims that the switches are now in working order and will be showing them in operation at Telecom '83. For now, both the MT line and CIT-Alcatel's E 10 switching gear



will survive. In the future, the joint effort will produce a single, rationalized product line administered by CGE but held by both Parisian companies. Some 11 million lines of the E 10 are used in 33 countries, and the number of lines rises by 2 million a year. There is little doubt that it works. But at Geneva's Nouveau Palais des Expositions et des Congrès, visitors trying to get a glimpse of the future will be looking for switches that can deal with the transmission rates demanded by the ISDN.

CIT-Alcatel will show prototype versions of standard copper pairs and optical fibers. Italtel Società Italiana Telecomunicazioni SPA will discuss an intermediate scheme for adapting current-generation digital-communications networks to offer some but not all ISDN services. The Milan company hopes to test its approach next year in Florence.

High price. Italtel's idea may interest many people because of the breathtaking cost of developing ISDN exchanges: about \$600 million to \$1 billion each, says C. J. van der Klugt, vice president of Philips. In the U. S., notes van der Klugt, four companies compete for a domestic market estimated at 40% of the world total. Two Japanese companies compete for a 5% share. In Europe, nine companies fight for 20% of the market. If Europe is to fall in line with the U. S. and Japan, the present line-up of nine European public-

switch manufacturers must dwindle to about three, he says.

In the U. S., Government deregulation has encouraged many companies to develop advanced digital central-office switches for large private organizations and traditional telephone operating companies. The number of companies competing for these big sales is growing quickly, and foreign competitors want a piece of the action, too. One driving force is market's realization that under deregulation, it will be crucial to have more control over communications and to use transmission services most efficiently. Large PABXs have filled some of this need in the past, but more advanced central-office switches now offer efficient interfaces to every large-area network, including packet-switched and local-area data transport. This equipment is based on stored program control, so upgrades and enhanced data-processing features can be absorbed effectively.

Major U. S. computer companies, sensing that a market has begun to develop, are allying with switch makers to counter the overall system sales pitch of large competitors like AT&T and ITT. Many overseas companies, among them Ericsson and NEC, also anticipate a chance to score big in the open U. S. market—the most important market of all.

Over there. AT&T's moves to team up with Philips and Olivetti are largely a part of the American giant's plan to penetrate overseas markets not available to it before divestiture. Europe's postal, telegraph, and telephone ministries still have regulatory power. In the European market, association with local producers is therefore the best way for AT&T to promote the equipment and services of its subsidiaries, AT&T Western Electric and AT&T Communications (formerly Long Lines).

The European Communities' Commission is well aware of how fragmented the European market is. Last week, the EC Council of Ministers agreed to a six-point plan to overcome that fragmentation by coordinating medium- and long-term plan-

ning through common research and development programs in user interfaces, optoelectronics, broadband networks, and the like, by accelerating agreements on interface standards, and by developing transnational links and Third World telecommunications infrastructures. A detailed plan will be presented to the EC heads of state at their meeting in Athens, in December.

In the United Kingdom, too, some rationalization is taking place. As a result of British Telecom's anxiety at the slow pace of System X development, Plessey Telecommunications Ltd. has been appointed as lead contractor, and Standard Telephones and Cables plc has been dropped. GEC Telecommunications Ltd. becomes a Plessey subcontractor for the System X processor.

The new consortium will probably have to compete with overseas firms even in its own market. This week, for example, Northern Telecom, which claims to be far and away the world's largest supplier of digital switching gear, announced that it would test the UK market's liberalization by establishing local manufacture. "We would like to enter the public packet-switched business in the UK with our SL-10, and we would like to sell our DMS switch as an alternative to System X," says Walter F. Light, the company's chairman and chief executive.

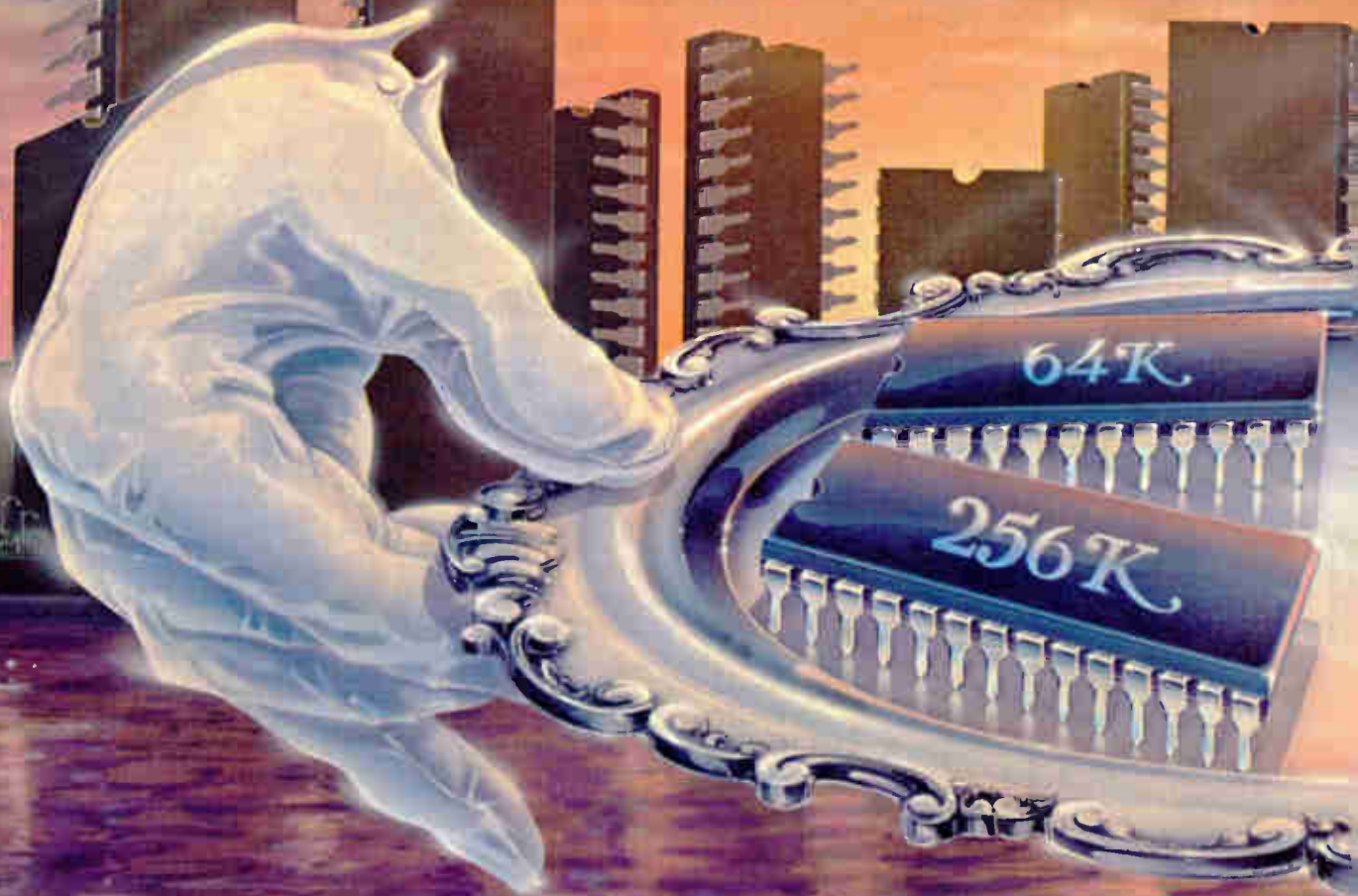
No hurry. Some companies feel they have enough muscle to succeed with little help. An official at West Germany's Siemens AG says that "nothing is planned in the foreseeable future" to imitate the AT&T-Philips accord. "We will not put all our cards on the table in the way that an outright alliance might entail," he says. However, the company already has limited agreements with French, British, Dutch, American, and Japanese companies to fill some niches and will not rule out more.

Olivetti, whose telecommunications activities depended heavily on such agreements, will move in the other direction. Having won access to digital PABX hardware through accords with Northern Telecom, Olivetti will introduce its own 64-extension digital PABX. □

Tranquility. This peaceful view of Geneva, the site of Telecom '83, is a contrast to the unsettled state of European telecommunications, where new alliances are the rule.

Reporting for this article was provided by Kevin Smith, John Gosch, and Roger J. Godin.

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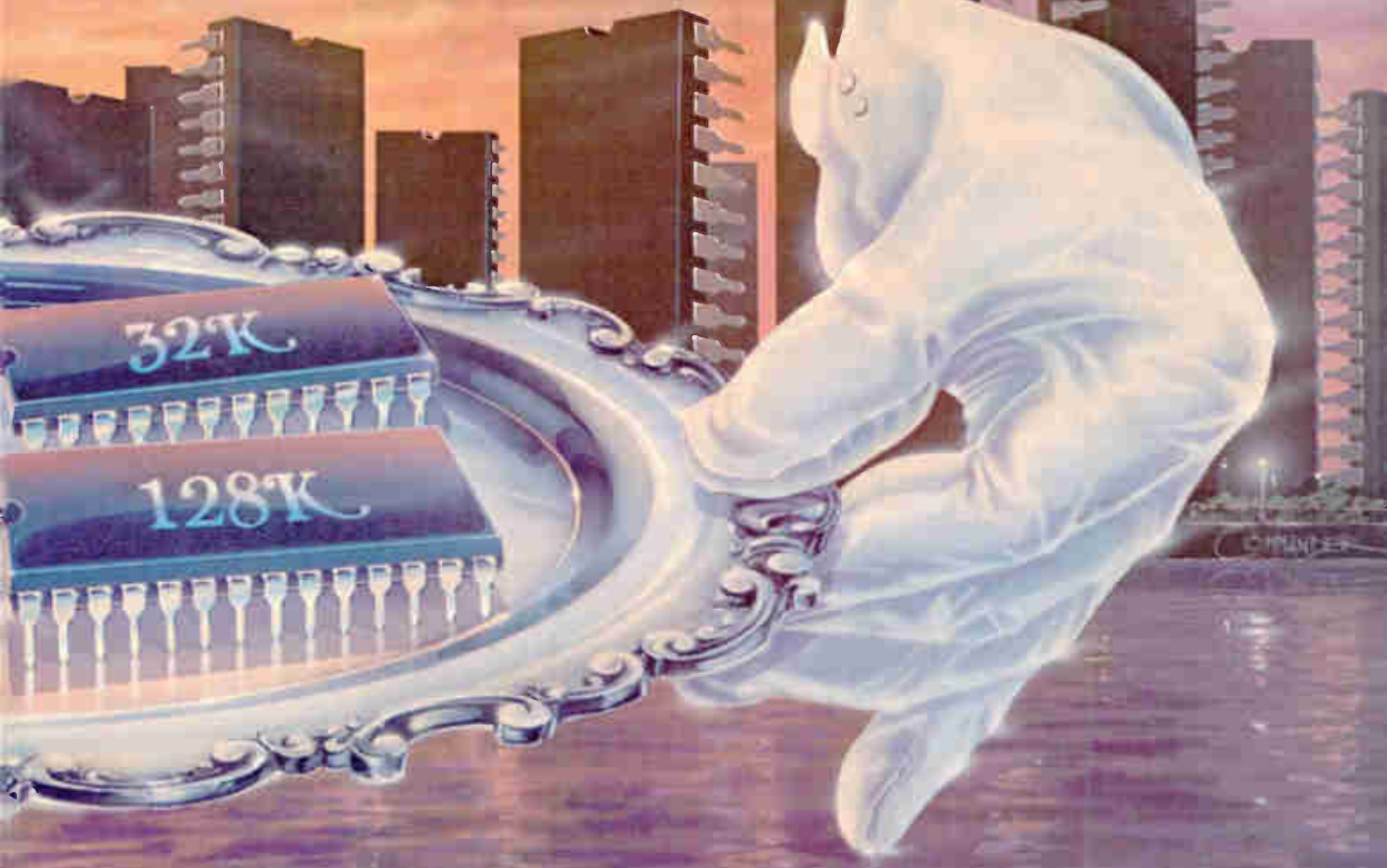
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				Active	Standby
16K Bit	TMM3334P*	2K x 8	450	40	—
32K Bit	TMM3333P*	4K x 8	450	100	—
32K Bit	TMM2332P*	4K x 8	350	100	15
40K Bit	T6635**	4K x 10	350	9	—
64K Bit	TMM2364P**	8K x 8	250	40	15
64K Bit	TMM2365P**	8K x 8	200	100	25
64K Bit	TMM2366P*	8K x 8	200	100	25
64K Bit	TMM2368P*	8K x 8	200	100	—
80K Bit	T6436**	8K x 10	350	0	—
128K Bit+	TMM23128P**	16K x 8	200	0	20
128K Bit	TMM23127P**	16K x 8	200	80	—
256K Bit	TMM23256P**	32K x 8	150	40	10
CMOS MASK PROGRAMMABLE ROM					
32K Bit	TC5332P*	4K x 8	450	7	20
32K Bit	TC5333P*	4K x 8	450	7	20
32K Bit	TC5334P*	4K x 8	450	7	20
32K Bit	TC5335P*	4K x 8	450	7	20
64K Bit+	TC5364P**	8K x 8	250	7	20
64K Bit+	TC5365P**	8K x 8	250	7	20
64K Bit+	TC5366P*	8K x 8	250	7	20
256K Bit+	TC53257P**	32K x 8	200	40	20

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Computers and peripherals

U. S. drive makers fear price war

Seagate's Conner avers a Japanese firm is following a dumping strategy in selling a hard-disk drive for about \$100 below the usual U. S. price

by Larry Waller, Los Angeles bureau

U. S. makers of 5¼-inch hard-disk drives could hardly be blamed for taking their continued success for granted. After all, since 1980, when the product first saw the light of day, its growth—closely tied to the emergence of the personal computer—has been truly spectacular even for a fast-track industry. In fact, the small-disk business has crashed right through the \$1 billion sales barrier, and its participants are now looking forward to at least three additional boom years (see "1.1 million 5¼-in. drives to be sold in 1983," opposite).

Despite the good news, the U. S. industry is not at all complacent—at least not if the reaction to a story in general circulation is any indication. What puts worry lines on the faces of disk-industry officials is the first solid evidence of a serious Japanese effort to move into the lucrative U. S. market.

Until now, Japanese competition had been widely feared and widely predicted. Yet, as in the printer business, Japanese suppliers had been content merely to dip a toe into the U. S. market. To date, their sales of small drives (both 8- and 5¼-in.) have not been significant, industry sources agree.

But a new wave of concern has been triggered by Finis F. Conner, the cofounder and vice chairman of Seagate Technology, in Scotts Valley, Calif. That company's nearly 45% stake in the 5¼-in. Winchester business makes Conner a very interested market observer indeed. As a panel member at an American Electronics Associa-

tion meeting held late last month in Los Angeles, he disclosed that quotes from a Japanese competitor revealed a startlingly low pricing policy. "It's low-balling," he charged. "Aggressive pricing is nothing new to us; it's something we live with, but this is not even in the same ballpark."

Tough competition. The outspoken Seagate executive declines to identify the Japanese firm or to give specific prices, but a competing company's top marketing official, who prefers to remain anonymous, has supplied some details. The Japanese firm is Nippon Electric Industry Co., a part-

ly owned subsidiary of giant NEC Corp. The product itself carries a Densai brand name, and its price level is "in the \$300s," which makes him jumpy, too. In the U. S., the current price barrier is now about \$400. A salesman has seen a sample of the product—a Seagate-compatible unit, the marketing official adds.

NEC refuses to say anything at all about its plans for this hard-disk drive, whose arrival in California is compared by one observer to the appearance of the first Mediterranean fruit fly in the Golden State, back in 1981. However, sources in Japan say that Densai is exporting four types of drives, all compatible with Seagate's 400 series: 5, 10, 15, and 20 megabytes.

Conner and others are quick to suggest that the Densai move is the first step in a classic dumping strategy, in which overseas prices are dropped below domestic levels to help a product take over a market. That charge against the Japanese, although often repeated, has seldom been proved.

Similar costs. Many drive producers buy components—heads, castings, and the like—from the selfsame offshore suppliers, including Japanese drive makers. So "we know their costs, the same way they know ours," explains Conner. What sets prices for users is therefore the volume any particular manufacturer manages to reach. "And we know they [the Japanese] are not building enough drives to sell them for that price," Conner insists.

What's more, the U. S. drive



business already is so hotly competitive—particularly the hammer-and-tongs contest between Seagate and No. 2 Tandon Corp., with its 20% of the Winchester business—that customers get the benefit of the higher-volume, lower-cost spiral quickly. “It [the 5-¼-in. market] is already a good value that doesn’t need much more competition,” observes consultant Raymond Freeman, of Santa Barbara, Calif.’s Freeman & Associates. “If prices decline too fast, it will come out of somebody’s hide.” The present \$400 level for Winchesters (in large quantities) is itself one third to one quarter of their cost several years ago.

Although the immediate concern is pricing, Conner and rival executives are more fearful of the longer-term effects of Japanese competition, especially the profits they will need to finance the high-speed growth they foresee for the mid-1980s. U. S. firms are enjoying returns on sales far above what Japanese firms are willing to accept.

As Conner puts it, “We [the U. S. firms] can compete and do a good job, but profit is a problem *vis-à-vis* the Japanese. They can live on 4%

to 5% of sales. The U. S. can’t.” Seconding his opinion were fellow AEA panel members and disk-business veterans Stuart P. Mabon, chairman and president of Micropolis Corp., and Raymond Brooke, president and chief operating officer of Computer Memories Inc., along with moderator Ralph Gabai, chairman and chief executive of Micro Peripherals Inc.—all of Chatsworth, Calif.

Broader question. Whether or not the Densai challenge proves real is not the basic question before the small-drive business, all hands agree. “It’s coming sometime, and we have to be prepared,” notes Conner. His firm’s thrust is relentlessly to seek greater efficiency through automation, design improvements, and continually higher volumes, a course he advises competitors to follow. They need little urging.

Conner voices one concern over which U. S. firms have no control. “We still lead in technology. All the drive innovations come from here; we are the equal of the Japanese in manufacturing; and we sell hard. But what can you do about financing, when they can get money at half the cost of ours?” □

1.1 million 5¼-in. drives to be sold in 1983

The newest market projections make it obvious that U. S. 5¼-inch disk-drive makers have hitched their wagons to a meteoric business. Industry consultant James Porter, whose Disk/Trend Inc., Mountain View, Calif., provided the data in question, has more than doubled his estimate of 1983 unit sales over an earlier forecast.

Sales of drives with fewer than 30 megabytes will hit 1,158,000 units this year, up from only some 240,000 in 1982. IBM—the driving force, says Porter—“is in there buying now.” Sales should continue to rocket, peaking in 1985 at some 2,500,000 units before backing off slightly, in 1986. What will finally cool the 5¼-in. boom, says Porter, is a still-newer product, the 3½-in. drive, whose rise to greatness will involve some old players and some new ones. Slated to sell only a paltry 8,000 units this year, they should take off and match the 5¼-in. devices by 1986, he thinks, if no unforeseen production glitches develop in the meantime. Still, it’s important to remember that even top drive makers seldom meet their optimistic schedules.

Porter’s U. S. clients should be somewhat gladdened by his outright skepticism about the near-term prospects for serious Japanese inroads. “They haven’t been a factor for two reasons,” he says. Most important, drives have moved up the technology-improvement curve so quickly that slow Japanese consensus decision making was left behind. In addition, “they haven’t yet caught on to the trick of selling in depth to U. S. OEMs.”

But the potential for tough competition still exists, he warns, “if heavyweight Japanese firms commit wholeheartedly to grabbing a chunk of the market.” For example, parent NEC lacks the capacity to sell the Densai drive in volume. But if the company decided to move, this could change overnight. —L. W.

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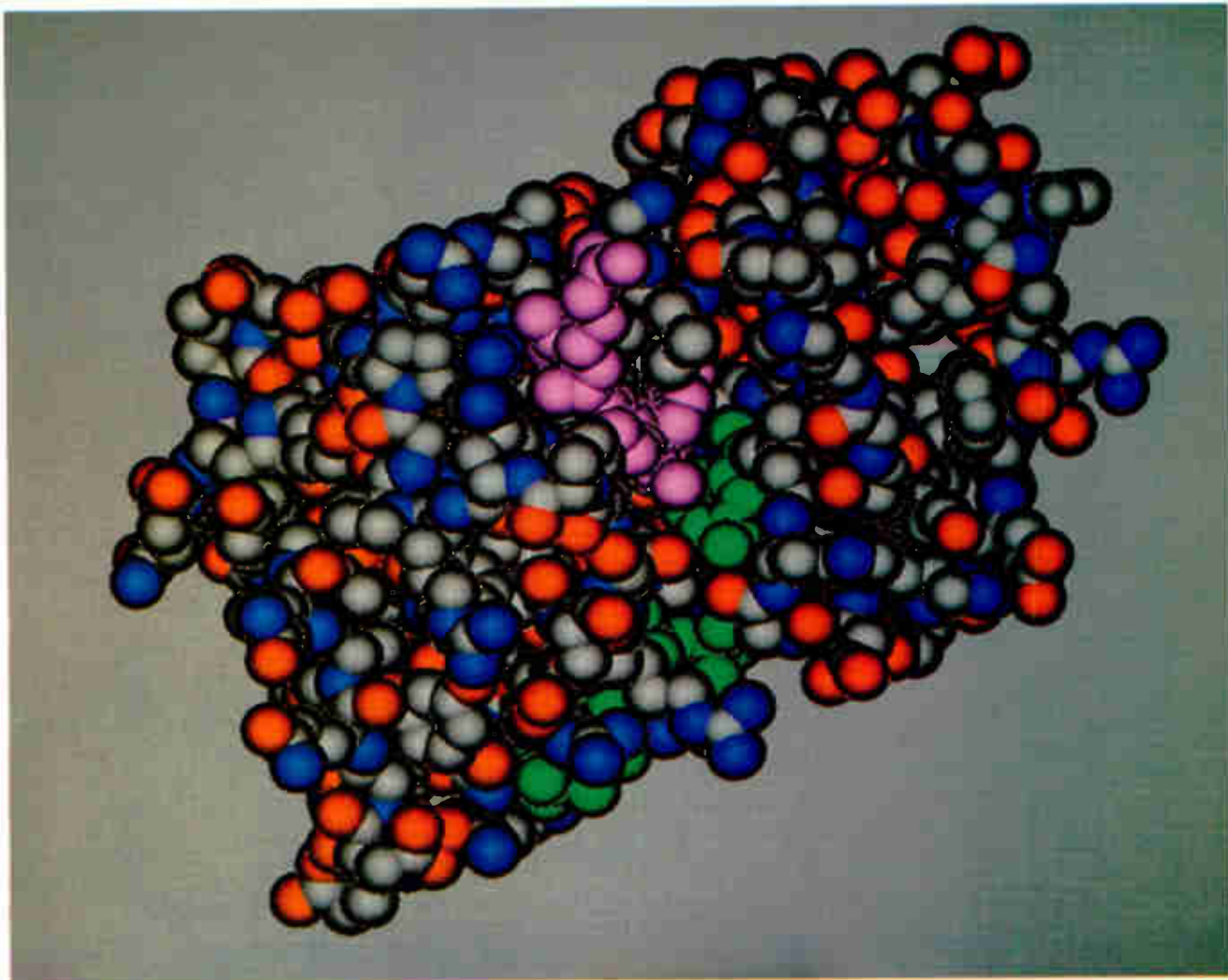
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Work station unites real-time graphics with Unix, Ethernet

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lighten the programmer's burden

by James H. Clark* and Tom Davis
Silicon Graphics Inc., Mountain View, Calif.

*On leave of absence from the Computer Systems
Laboratory, Stanford University, Palo Alto, Calif.

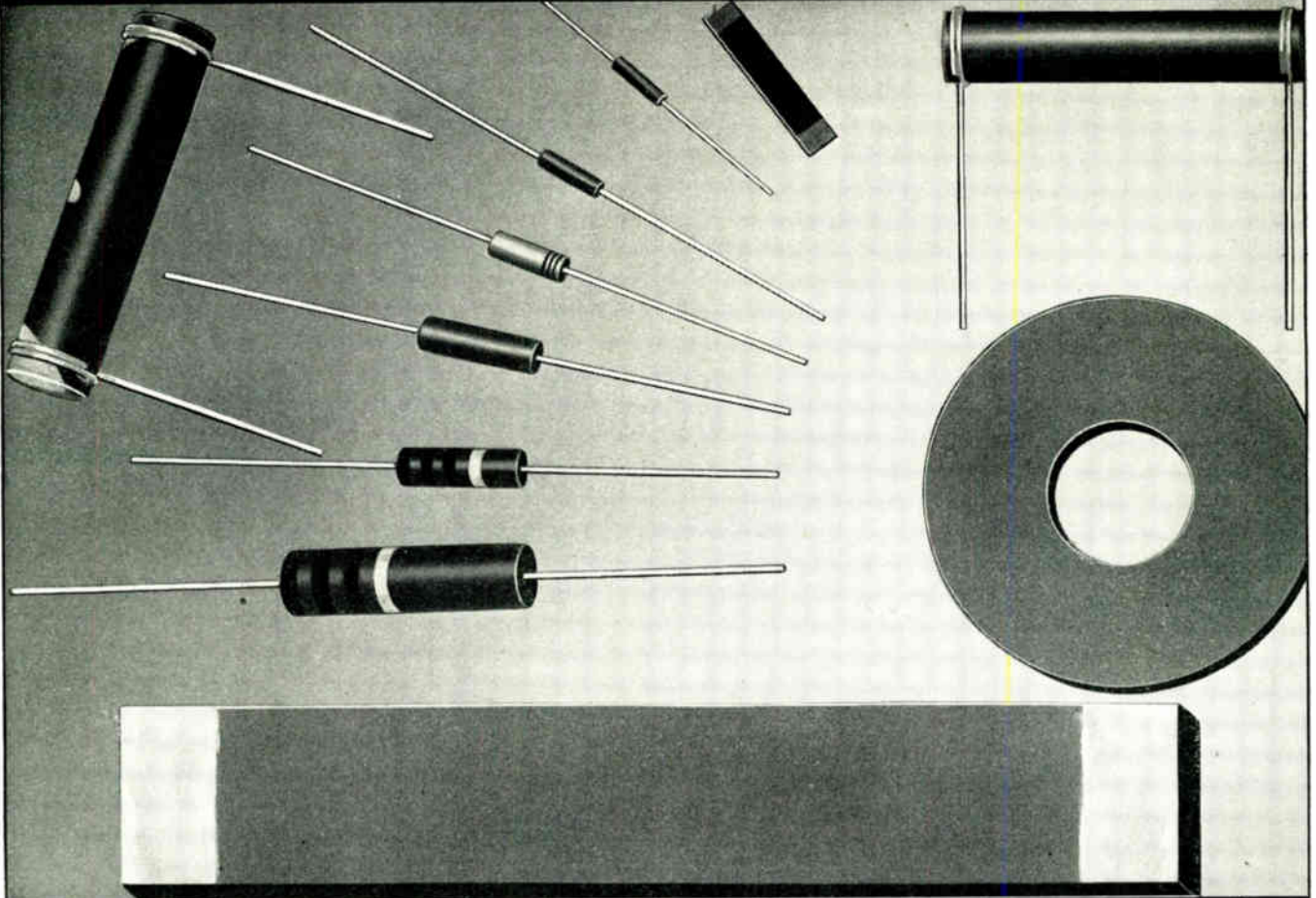
□ Productivity in engineering design requires powerful computing tools that reduce the time needed to do the design. Because virtually all forms of engineering require manipulation of geometrical and graphical constructs as well as general-purpose computing, a work station with real-time graphics decreases the time the engineer must wait to see the results of design changes and hence increases productivity.

Still, for general scientific and engineering use, computer work stations require more than graphics. A work station's computation should be supported by a general-purpose operating system and by appropriate languages and tools for developing application programs. Besides allowing for the local development and execution of programs, the work station must also be able to serve other computers as a graphics terminal.

Thus, as the engineer's principal connection to the outside world, the work station needs to function within a communications network, allowing separate work stations to share data and resources such as disk drives,

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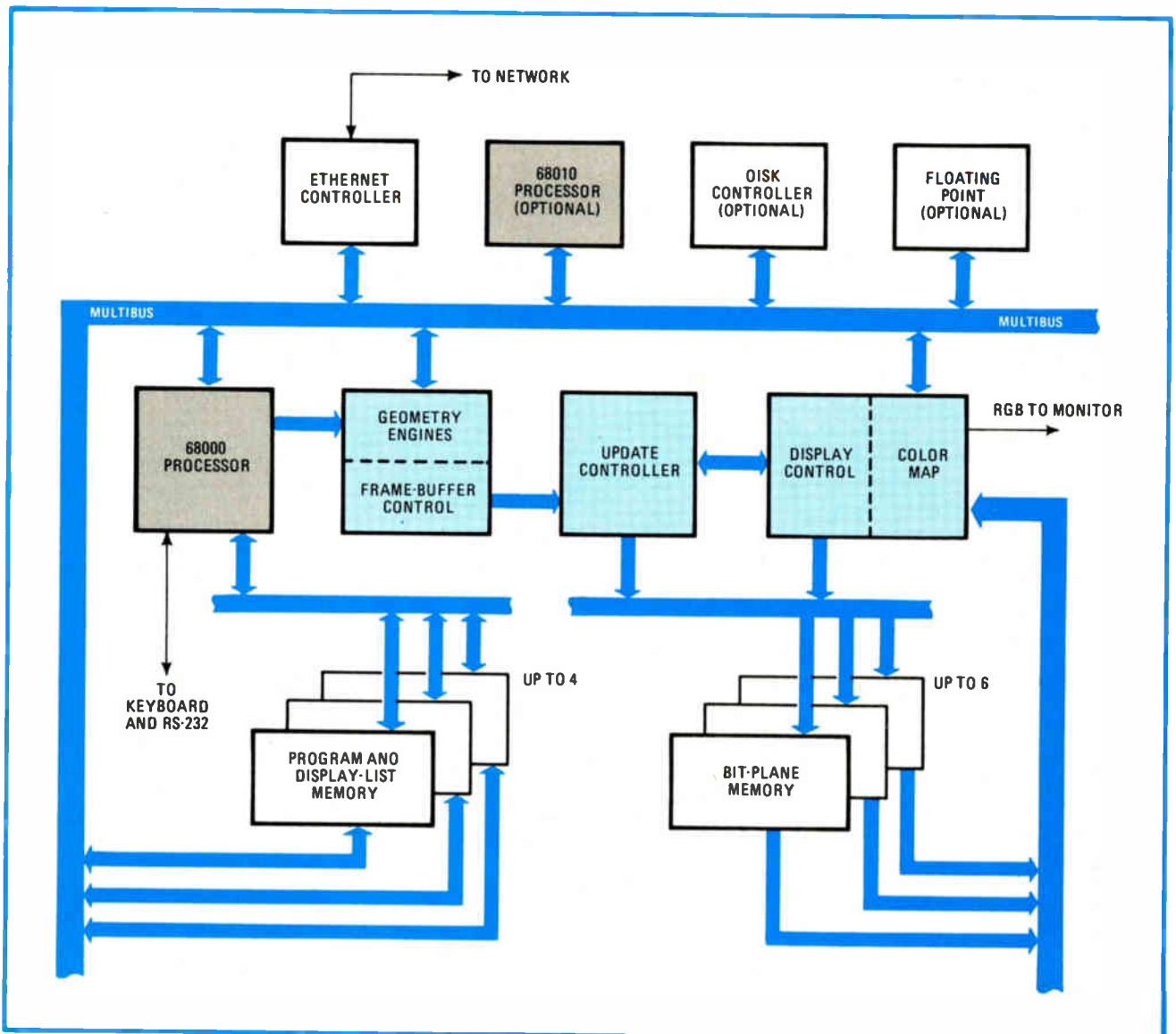
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2. Architecture. In addition to the system's standard 68000 microprocessor, which runs a real-time kernel, an optional 68010 runs virtual-memory Unix 4.2BSD. Proprietary geometry chips perform the matrix manipulations that are needed for real-time graphics.

hardcopy devices, and other computers. Simultaneously, as the engineer's principal connection to the computer, the work station must be capable of high-speed graphics to simplify the manipulation and analysis of data but must not expose the user to excessive delays.

Powerful real-time graphics is fundamental to an engineering work station and is a fundamental part of the IRIS work station from Silicon Graphics Inc. The IRIS combines Bell Laboratories' Unix operating system and the Ethernet communications network with a general-purpose, real-time, three-dimensional color-raster graphics system. Custom very large-scale integrated circuits in the IRIS, such as Silicon Graphics' trademarked Geometry Engine (see p. 117), reduce its cost and power requirements, increase its reliability, and provide real-time speed and high graphics functionality suitable for a broad spectrum of two- and three-dimensional applications.

In addition to general-purpose computing, the IRIS supports real-time color display and manipulation of bit-

mapped or stroked characters, 2-d or 3-d vectors, parametric curves and surfaces, 2-d areas, and 3-d solids with shading and hidden surfaces removed. These graphic objects are defined in the user's coordinate system, in either 32-bit floating-point or 24-bit integer values. All the geometric transformations, rotations, translations, scaling, clipping, multiple windows and viewports, perspective projections, and so forth are done by the engine at rates approaching 10 million floating-point operations a second. In addition, the geometry chip is provided as a general-purpose geometric computing subsystem suitable for calculating the intersection of solids and for matrix arithmetic at these floating-point rates.

Instantaneous drawing rates decrease engineering design time. Engineering work requires the manipulation of complex 2-d and 3-d geometric models that frequently are hard to visualize or contain large amounts of information. If the display of information is instantaneous, the engineer spends less time in analysis of the information

and hence is more productive. The list of applications needing this high level of performance spans engineering disciplines from mechanical to electrical engineering (Figs. 1, 3, 6, and 7). Even fields such as physical chemistry—where shaded models of molecules provide hints of chemical properties (Fig. 1)—require high-performance real-time graphics. Circuit designers need to be able to view multiple windows of graphics and textual data (Fig. 3 and cover). For architectural engineers, the ability to view 3-d architectural layouts speeds the design process (see cover). Similarly, viewing trajectories of robot manipulators and checking for collisions allows for faster programming of movements (Fig. 6). Aircraft, automobile, and ship designers continually need to model exterior surfaces based on parametric curves (Fig. 7) and even to simulate their motion (again, see the cover illustration).

The IRIS is a real-time graphics computing node in an Ethernet communications environment. Three main configurations are possible: work stations, terminals, and file servers. The IRIS terminal runs a small real-time operating system called the V Kernel—developed by David Cheriton and co-workers at Stanford University—and provides a multiwindow environment for access to one or more computers on the network. The work station runs Bell Laboratories' Unix operating system and, with a disk, is capable of operating independently. A file server supplies data files to other computing nodes over the network. Both terminals and work stations provide the graphics capability.

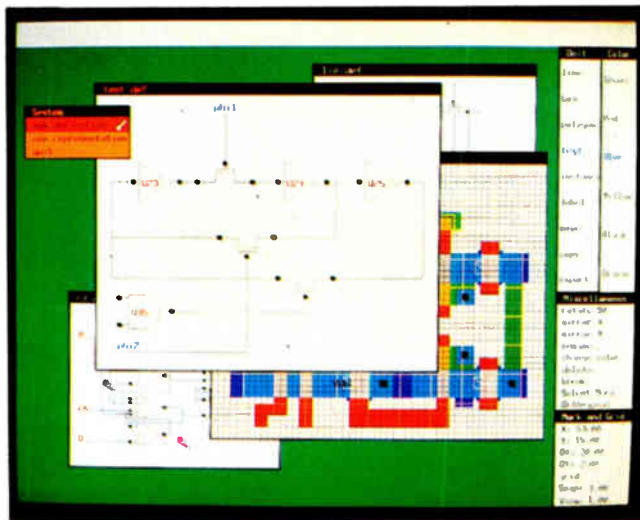
Graphics node

When the IRIS is used as a terminal, the graphics application runs on a remote host connected to the terminal by a network. (Serial and parallel connections to the host are also possible.) Graphics commands issued on the host are sent to the IRIS to be executed, where it either draws them immediately or stores them in display lists for local rapid drawing, depending upon the mode. Once a display list is defined, the application program typically sends only editing and redraw commands, so that instantaneous response is achieved over the network.

The terminal uses the Motorola 68000 and a geometry-chip pipeline with output to a high-resolution color raster-scan display. All graphics pipeline data is transmitted on a private data bus, and all the circuit boards use the standard Institute of Electrical and Electronics Engineers (or Intel) Multibus for general communications.

The work station may have either one or two processors. The dual-processor form just adds a second processor to the backplane, which serves as the host to the terminal processor. The second processor runs a 68010 with Virtual Memory Unix 4.2BSD, while the terminal processor continues to run the V Kernel. Here, the "terminal" has a dedicated host, and communication is through shared memory, rather than with the network.

The single-processor work station runs Unix 4.2BSD on a 68010 processor and memory subsystem, which serves as the real-time graphics processor as well. The Unix kernel is slightly modified so as to provide real-time graphics service. For most real-time applications, performance can be improved by a factor of almost two with



3. VLSI design. Two-dimensional area-fill functions—along with pan, zoom, rotation, and scale operations—help circuit design all the way from VLSI layout to schematic entry. Engineers can use the system's multiple windows to view sections of circuits.

the assistance of a dual-processor work station.

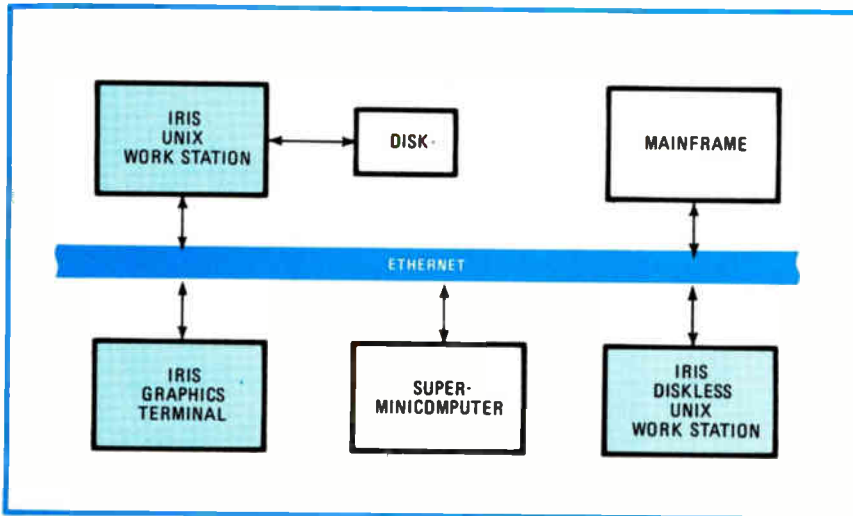
The electronics consists of one or more general-purpose processors and a geometry pipeline made up of the engine subsystem, the frame-buffer controller, the update controller, and the display controller. Also, standard network and disk controllers may be present (Fig. 2).

The 68010 processor and memory subsystem generates 24-bit virtual addresses that are applied to the memory map, on-board read-only memory, and on-board input/output interfaces. The page map uses a fast, 1.5-level structure and 4-K-byte pages to provide up to 16-megabytes of virtual address space for up to 256 process contexts in a demand-paged Unix environment. Physical addresses from the page map contend with accesses from the Multibus and the hardware memory-refresh circuit through a triple-ported arbiter. Space is provided for up to 128-K bytes of erasable programmable ROM and four RS-232-C serial lines. Using 64-K random-access memory, the 0.5 megabyte of memory on the processor board can be extended in 1-megabyte increments. With 256-K parts, these numbers increase to 2 and 4 megabytes, respectively. Memory references from the Multibus are mapped to provide scatter-gather direct memory access, as well as control, when there is more than one central processing unit on the Multibus.

In the terminal form, the 68000 acts as the display processor, executing all graphics drawing instructions and directing data into the graphics pipeline. It manages display-list memory, input devices such as the keyboard, and communications with the host processor. In the single-processor work station, the 68010 does these functions as well as running Unix 4.2BSD.

Graphics pipeline

Graphical output is initiated by the CPU when it sends commands and data to the graphics pipeline. In normal mode, the engines do matrix transformations, clip to normalized coordinates, and finally scale the transformed, clipped points to screen coordinates. The frame-



4. Multiple modes. Real-time graphics is not enough by itself to enhance productivity. The IRIS work station meets the challenge by fitting into an Ethernet network as a stand-alone work station, graphics terminal, and server for other network nodes.

current color with the current write mask. Both the write mask and the color have 1 bit per bit-plane. Only if the bit in the write mask is on is the color bit written into the corresponding bit-plane.

The IRIS system handles three display modes: single-buffer, double-buffer, and red-green-blue. With 24 bit-planes, the system can be configured in the RGB mode, where 8 bits of the color specify the intensity for

red, for green, and for blue. Both the other modes work through a color map that has 4,096 entries of 24 bits each. The 24 bits contain the red, green, and blue intensities for each of the two entries. One access mode uses the values in the bit-planes as the entry into the map. Another method (especially useful with 8 or fewer bit-planes) is to use the bit-planes for the 8 low-order bits in the map and a software-controlled map register for the top 4 bits. Thus the map may be configured either as one 12-bit map or as 16 8-bit maps.

In single-buffer mode, all the bit-planes are visible, and changes appear on the screen as soon as they are made in the bit-planes. This is unsuitable for fast, animated graphics, since the image must immediately be erased before the next frame can begin to be drawn, and the viewer will see, on the average, a half-drawn image.

Real-time graphics is therefore usually done in double-buffer mode—one image is viewed while the next one is being drawn. In double-buffer mode, the bit-planes are divided into halves. One half is viewed while the other half is modified. When the modified frame is complete, the halves are exchanged and the new frame appears all at once. There are routines to synchronize buffer swapping with a real clock to get uniform motion. All the color-mapping features described in the last section work the same way in single- or double-buffer mode.

The raster subsystem has hardware support for the cursor. The cursor is any 16-by-16 pattern that always appears at the current cursor position drawn in the cursor color with the cursor's write mask. Commands to set the cursor's current position are set automatically by the software, so that the application program need not do it. The cursor color and write mask are independent of the geometry color and write mask. In double-buffer mode, the cursor is drawn on the front buffer, while the geometry is written on the back one.

The raster subsystem supports variable-pitch raster fonts and stores them in a 64-K-byte font RAM. The contents of the font RAM are controlled by software on the 68000, which allocates the memory for fonts with different numbers and sizes of characters. As characters from the raster font are drawn, the current character position is automatically updated by the width of the

buffer controller (a 16-bit 2903 bit-slice processor) does such things as interpret characters, control the font memory, and compute coefficients for rendering lines and polygons. The update controller does scan conversion, including filling polygons and lines, clipping characters, and placing the results in the frame buffer. Finally, the display controller fetches picture-element values from the frame buffer and draws them on the face of the color cathode-ray tube.

The Multibus is normally used only for I/O communication with the disk or the Ethernet. The graphics pipeline is a separate data path, not on the Multibus. Likewise, the memory on the processor is dual-ported, and accesses to it need not use the Multibus.

The geometry subsystem consists of a pipeline of up to 12 identical engine chips (see "Gearing up for real-time graphics," p. 117). Each chip can be configured in software to do dot products, clipping, scaling, or nothing (a null device). A 12-chip pipeline is typically configured with the first four as dot product chips (forming a 4-by-4 matrix multiplier), the next six as clippers (to clip against the left, right, top, bottom, near, and far planes), and the last two as scalars to convert the normalized coordinates into physical screen coordinates.

The matrix multiplier transforms points from their original coordinate system into a normalized eye-coordinate system. The clippers clip those lines and polygons that would have extended outside the viewing area (clipping is different for lines and polygons). The clippers may need to add or delete points in the process. Finally, the scalars convert the transformed and clipped points into physical screen coordinates.

The data that comes out of the geometry pipeline is primarily a set of commands in absolute screen coordinates. The raster subsystem's main jobs are to fill in the pixels between the endpoints of the lines, fill the interiors of polygons, and convert character codes into bit-mapped characters. Each line that is drawn has certain attributes, among them a width (of 1 or 2 pixels), a stipple pattern, and a mode.

An IRIS system may have from 4 to 24 bit-planes in increments of 4. Any graphical object that is drawn—whether a line, a polygon, or text—is drawn in the

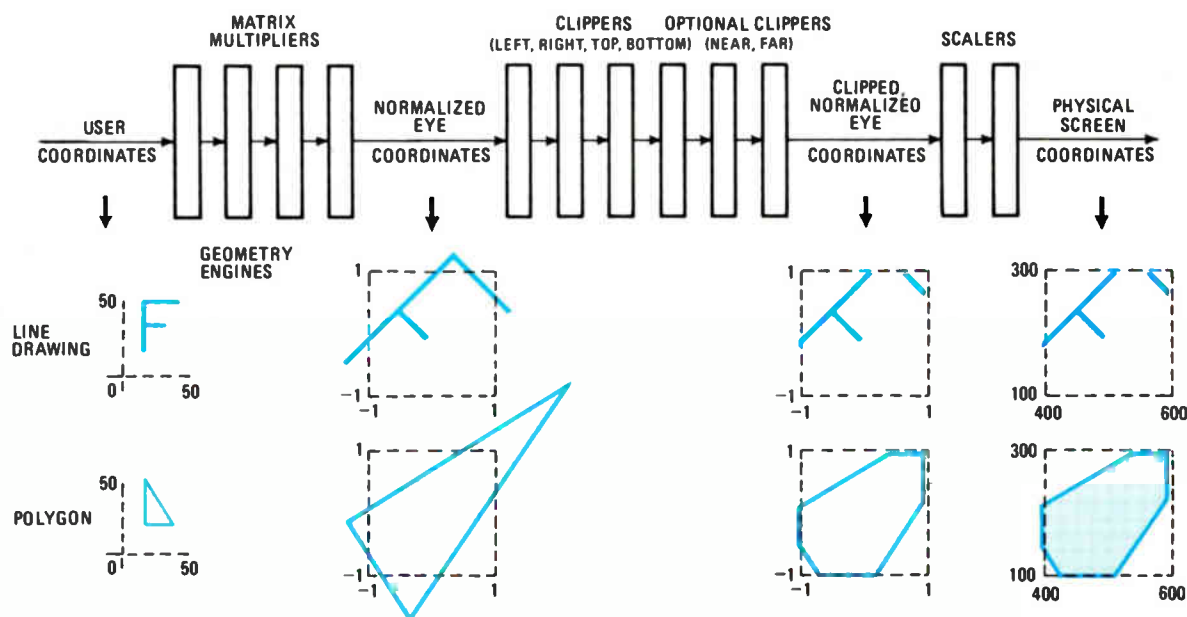
Gearing up for real-time graphics

The Geometry Engine, trademarked by Silicon Graphics, is a very large-scale integrated circuit with about 75,000 transistors that can be configured to do one of three basic operations: matrix transformation, geometric clipping, and mapping to output device coordinates. Working internally with four-dimensional vectors of floating-point numbers, the hardware directly supports all the commands necessary to save the internal state of the system, manipulate matrixes and viewports, draw lines, curves, surfaces, polygons, and characters, and change colors and other attributes of the system.

Besides four floating-point arithmetic and logic units, the engine contains a control store for the microcode to implement floating-point operations, line and polygon clipping, perspective division, stack management, and curve generation. For example, in the engine's curve command, microcode generates points along any three-dimensional rational cubic spline, employing user-supplied coefficients and endpoints, which it treats as if they had been sent with separate move and draw commands.

In another mode of operation, called hit-testing, a pair of commands causes the engine to indicate against which planes an item is clipped, without actually drawing the item. For example, a polygon surrounding the viewport would record four clips, even though none of its lines passes through a visible region. The figure shows how a line drawing and polygon would appear at various stages in the pipeline.

Besides the configuration illustrated, others are sometimes useful. For example, if special commands are employed to make the clippers and scalers merely pass data without operating on it, the pipeline can be used as a hardware 4-by-4 matrix multiplier. Furthermore, the pipeline can be configured to clip polygons against an arbitrary plane—ideal for solid-modeling applications. The first four geometry chips can transform the coordinate system to make that plane a standard clipping plane, the fifth is a clipper, and the next four invert the transformation. All polygons passed through this pipeline will be clipped against the given plane.



characters drawn. Characters are clipped by a screen window on bit boundaries, so a character does not suddenly disappear as soon as a part of it moves off the screen. It is possible to read and write individual pixels on the screen—a useful feature in such applications as interactive “video painting” as used in the graphic arts.

System software

The IRIS work station is a 68010-based Unix 4.2BSD machine with network support and real-time graphics hardware supported by a graphics library. All standard Unix utilities are available, so the system can be used as a stand-alone work station. The IRIS system software is

written in C, but the graphics library is callable from other languages (currently Pascal and Fortran).

The IRIS terminal is attached to its remote host or hosts over a network or through a serial connection (Fig. 4). The graphics software is independent of the type of connection used, but greater network bandwidth gives better performance. IRIS systems use network protocols that are compatible with both the Government-sponsored IP/TCP and Xerox's XNS. A VAX machine running the Unix 4.2BSD operating system uses IP/TCP, for example, but a VMS VAX communicates with IRIS terminals with XNS software provided by Silicon Graphics Inc.

The IRIS graphics software provides a convenient,

high-level interface with the hardware. It also provides low-level access for applications demanding it. Its main features are:

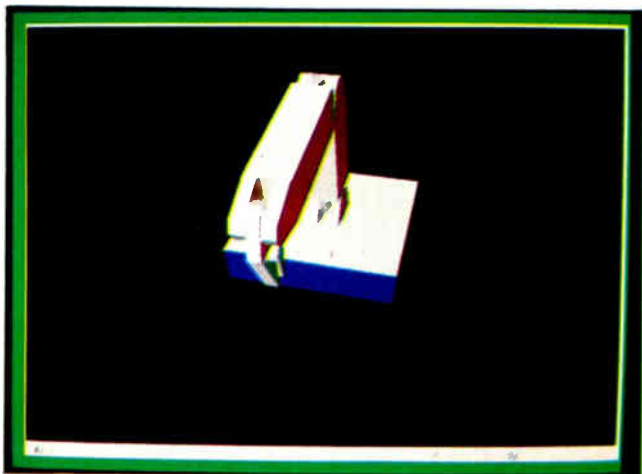
- Multiple windows and multiple viewports for mixed text and graphics.
- Hierarchical display-list definition and maintenance.
- User-space object transformations at the command level.
- Immediate and compiled display-list modes.
- Display-list editing.
- Object-selection mechanism, including picking and collision detection.
- Geometric computation.
- Queued I/O.

Proposed graphics standards such as CORE and GKS could be implemented using a subset of the IRIS graphics library. Unfortunately, CORE treats transformations as an adjunct to a graphics system, so that the CORE system is not as suitable for real-time applications. GKS, on the other hand, does not provide the 3-d applications, although it does allow transformations to be applied to all objects. The IRIS graphics library is basically a combination of the two systems, but it is specifically tailored to the IRIS, rather than designed to be the sum of GKS and CORE.

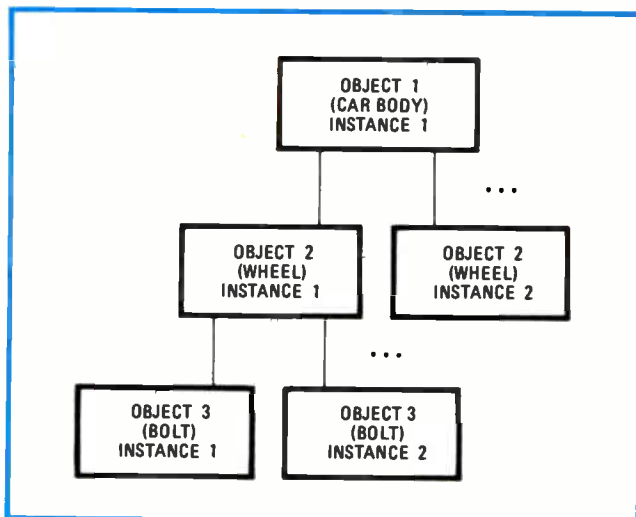
Hierarchy and naming

Both the hardware and software support hierarchical graphical objects. A hierarchical description of an automobile, for example, might include one list of commands that draws the body and another that draws a wheel. To draw the car, the software must draw only the body, then draw the wheel four times, each with appropriate translations and rotations. The wheel itself may contain still simpler objects—perhaps five instances of a bolt.

The basic graphical data structure is called an object. It is made up of primitive drawing commands together with calls on other objects that are transformed (rotated, translated, and scaled). In the example above, the bolt object might consist only of move and draw commands. The wheel has commands to draw the rim and tire, plus



6. Robot animation. Animated shaded-picture generation in real time allows rapid determination of robot manipulator paths through space. IRIS software can also check for collision detection to ensure that the planned trajectory does not conflict with other objects.



5. Hierarchical nesting. Although the final drawing may be a complex combination of several objects, IRIS software allows designers to deal with multiple objects simply as separate instances of some distinct object, like a car body, a wheel, or a bolt.

five calls on the bolt object. The car object consists of the body-drawing commands plus four calls on the wheel object. Only three object descriptions are needed, although there will be 20 bolts in the final drawing (Fig. 5). This hierarchical nesting can be arbitrarily deep, and the transformations for intermediate values are saved in the engine's matrix stack.

Naming is a problem with hierarchical objects. An engineer editing the car drawing needs to know that the bolt he has pointed to is, say, the third bolt on the left front wheel of the car. To specify an object completely, a path of names is required—instance “three” of object “bolt” in instance “left front” of object “wheel” in instance “one” of object “car.” Deeper nesting requires a longer path. The graphics library supports paths of instance and object names for both selection and editing.

Since a transformation can be applied every time an object is called within another object, each object can be described in the most convenient coordinate system. This is even true of the highest level of object, since arbitrary viewing and windowing transformations are applied.

Any objects that are conveniently described in terms of smaller objects are good candidates for a hierarchical description. Mechanical parts, automobiles, VLSI and circuit designs, and documentation (chapters, sections, and paragraphs) all fall into this category.

High-level access

Programmers usually deal with the system on a high level. For example, the IRIS internally uses 4-by-4 matrixes to represent all the perspective, windowing, rotation, translation, and scaling transformations, but the user commands look like “rotate (angle, axis)” or “translate (x-dist, y-dist, z-dist)” or “perspective (field-of-view, aspect-ratio, near-clipping-dist, far-clipping-dist).” Curves and surfaces are specified in terms of control points instead of different matrixes. Cursor drawing and undrawing is handled automatically, and the system is automatically initialized in a reasonable way.

The graphics software can be used in immediate or compiled mode. In immediate mode, the effects of a drawing command appear immediately on the screen. Programming is easy in this mode, but there are two disadvantages: there is no way to save object definitions so they can be called by other objects, and the overhead associated with a subroutine call makes the 68000 the performance bottleneck. Compiled display lists solve these problems. Each graphical object is stored internally as a display list that can be traversed rapidly enough by the 68000 processor to keep up with the geometry pipeline. For example, the car object shown in Fig. 5 might be compiled as:

```
makeobj(car);
[commands for drawing the body]
translate(0.0,7.0,0.0) /* position first wheel */
callobj(wheel); /* draw the first wheel */
[commands to draw the other wheels]
closeobj( );
```

Then, all the commands between MAKEOBJ and CLOSEOBJ become part of the object called CAR.

Compiled mode runs fastest, but an existing application can be converted to run on the IRIS very quickly using immediate-mode commands. Later, critical sections of the code can be converted to build display lists for better performance.

Editing objects

Display-list objects can be edited—entries can be added, deleted, or replaced, and an entire object can be rotated in real time by repeatedly editing the rotate command, changing the angle, and redrawing the object. If the IRIS work station is acting as a network terminal, only a few network transactions are necessary—open the object, edit the rotate, close the object, and draw it. Memory management for display-list code space is done automatically.

The IRIS graphics software supports standard graphics primitives—points, lines, polygons, rectangles, circles, arcs, cubic splines, and so on. Most can be filled or

unfilled, in two or three dimensions, and in fixed- or floating-point terms.

The graphics pipeline can be put into a feedback mode, where it does not draw anything on the screen but instead sends the data back to the 68000 for further processing. This feature can be exploited in many ways. To select an object, its name must be recovered from the screen coordinates. To accomplish this, the system software modifies the windowing transformation, so that the view is a tiny window around the selection point, and then draws the object again in hit-testing mode. In this mode, an indication of what would have been drawn (including its name path) is fed back to the 68000. Area selection is the same, but with a larger window.

Selection is important for any application where the user needs to point interactively to objects on the screen. Drafting tools, circuit editors, simulators, and document-production tools all fall into this category. In many applications (robot-arm simulation or games, for instance), collision detection is needed. This is similar to selection but uses a 3-d box as a window around the object being tested for collisions.

Real-time support

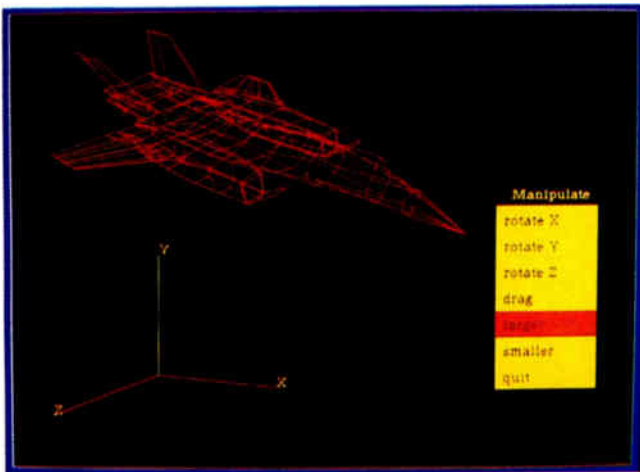
Real-time graphics is usually performed in a double-buffer mode. Here, while one image is being viewed, another is being constructed in a separate memory area. Special routines synchronize swapping between the two buffers to give uniform motion.

Any object transformed by modeling and viewing transformations may have a very small screen area or may even be outside the viewing area. Rather than wasting resources on drawing such objects, the system can automatically prune the display list of them. A bounding box for the object is passed through in feedback mode, and the rest of the object is skipped if the bounding box is either too small or out of range.

Delays associated with network communications make dragging objects on the screen from a remote host difficult. To avoid this problem, the MODIFY command ties a parameter of a drawing command to a linear function of an input-device value. For example, binding a mouse's X and Y positions to the X and Y parameters of a translation command will cause the translated object to be dragged by the movements of the mouse. By confining this type of interaction to the local work station, this technique avoids any network-associated delays.

The software allows either polled or queued input. An application reads the current state of a button (up or down), the current mouse coordinates, or the current setting of a dial. In addition, any combination of input devices may be queued in an event queue. If the state of a queued device changes (a button goes down or up, or the mouse or dial position changes by more than a certain amount), an event is added to the queue. The application then has a time-ordered list of events that can be processed asynchronously.

The keyboard is unencoded, so if desired, the user knows when a key goes down and when it comes up. The usual mode is to have the unencoded keyboard interpreted as if it were standard ASCII, and standard software routines do this. □



7. Aircraft design. Parametric curves and surfaces model exterior surfaces, and vector drawings display results to industrial designers. The ability to examine different portions of the object through rotation and zoom further helps designers to visualize mechanical parts.

Computerizing the factory floor

Microprocessor-controlled robots, programmable devices, and networks centralize control directly under the plant manager

by Erik L. Keller, *Industrial & Consumer Editor*

Information and control are today's factory-floor watchwords. Production-line mainstays like relays and timers are fairly efficient and trouble-free but cannot quickly be reconfigured for different tasks. This deficiency and the limited data they provide will restrict them to only minor roles in modern factories. As for the other factory-floor problem—the assembly-line worker—he rarely lives up to modern manufacturing's need for quality and consistency.

Factory work stations and robots are relieving these devices and people. By permitting managers to check and tweak production from afar—with more than just guesswork—smart silicon is changing the way factories run. And robots—with their great precision, tirelessness, and ability to carry out repetitive assignments exactly and to perform different tasks after simple programming changes, with no decline in throughput or quality—are arm-wrestling their human counterparts out of assembly-line jobs.

Although the hardware for setting up very efficient and flexible production lines does exist, the lines' complexity often makes the task difficult. Still, manufacturers must have some way of ferreting out, from a morass of alternatives, a production line that will be economical and easy to change. The decisions involved are intricate and so are being left to computers. Decisions about other production-line changes—when machines break down and work cells or stations must be altered to maintain production schedules, for instance—are too complex for human beings and are also being left to computers.

Still, writing the software that enables a computer to change production-equipment and robot-assembly tasks is also tricky. Moreover, a manufacturer must have a network that can relay commands to the hardware. Without such downloading capabilities, robots must be manually retrained with a teaching pendant—an expensive and time-consuming process. Downloading program instructions from computer-aided-design and -manufacturing work stations is not always easy, of course. Indeed, manufacturers who use different brands of microprocessor-based devices may find it impossible to get them to communicate with one another.

Providing a sufficiently large data base, the heart of a computer-integrated-manufacturing (CIM) set-up, is another problem. Such information is essential for CAD simulations, for the design speedups they make possible, and for the down-

loading of information, through CAM, to the factory floor. So robots or programmable controllers or networks by themselves will not create the factory of the future. That consummation demands the integration of all these technologies, along with the right kind of human supervision.

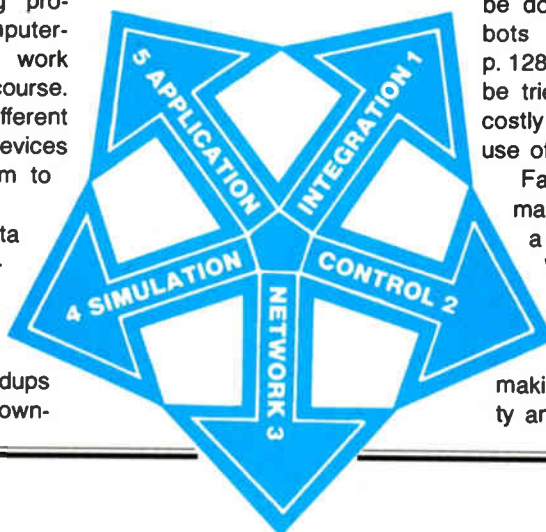
The following five articles provide a skeleton of the way U. S. factories are using industrial electronics. An overview by Motorola Inc. shows how CAD, CAM, and CIM technologies have affected its Fort Lauderdale, Fla., facility (see p. 121). As Motorola found out, integrating the trio of computerized manufacturing techniques is neither easy nor fast; it takes much planning and employee training. But the benefits are unmistakable: a better product in less time and a highly motivated work crew.

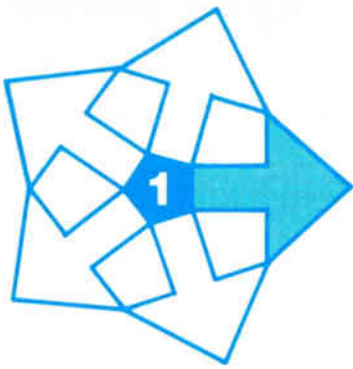
Getting and sending information is just one part of automation. A truly automated system is able to think for itself, and that in effect is what Draper Laboratory's Decision Support System can do (see p. 123). If something needs to be changed, the system can make the decision or at least provide the manager with a list of choices.

Some vendors, such as International Business Machines Corp., offer bundled answers to factory automation, but that answer is not wanted by manufacturers who have already installed smart devices having different protocols, hardware requirements, and interfaces. However, Advanced Control Technologies' Factory Information System, links many of the commonest controllers, computers, and terminals into a network that makes it possible for plant managers to get information to and from the factory floor quickly (see p. 126).

When these decisions have been made, they are implemented by work cells, most of which use robots. McAuto's work-cell software package permits almost any robotic set-up to be simulated on a CAD system, and motion data to be downloaded to devices such as robots and numerical controllers (see p. 128). Different work-cell scenarios may be tried quickly, eliminating difficult and costly manual programming and actual use of equipment on the factory floor.

Fared Robot Systems has linked many industrial electronic elements in a robot assembly line that builds Winchester disk drives *sans* human beings (see p. 131). Such a line has one big advantage: it can be controlled precisely, thus making possible a product of high quality and constant throughput.





CAD, CAM, and CIM revolutionize the electronics factory

Integrating data bases already available for computer-aided design and manufacturing facilitates the design of new products

by Don Krumin, *Motorola Inc., Fort Lauderdale, Fla.*

□ Computer-aided design and manufacturing are generally considered the best answers to the demand for increased productivity and quality. But computer-integrated manufacturing goes one better: it offers manufacturers new control of the production process and prevents many problems on the factory floor. Motorola Inc., like many firms, is gradually integrating these manufacturing techniques into its factories.

Motorola's Fort Lauderdale CAD-CAM-CIM facility is an "open" environment with on-line design activity, which permits any of the firm's designers to use CAD/CAM equipment. In the last two years, its Computervision CAD/CAM design-system terminals for printed-circuit and mechanical-design activity have increased from 2 to 24. In addition, its General Electric Calma work stations, for integrated-circuit design, have increased from four to eight. This equipment is used over three six-hour shifts each day and was instrumental in designing Motorola's latest portable computer system [*Electronics*, Aug. 25, 1983, p. 142].

The portable computer was developed in its entirety on a CAD/CAM system with data-base links to the factory for automated assembly and testing of high-density pc boards. The use of CAD/CAM techniques helped to improve designs and shorten development cycles. For instance, animated graphics were used to check the clearance of the computer's battery door to the lower housing during operation (Fig. 1), and Computervision's tolerance-stack-up program automatically calculated clearances between parts.

Estimates of the ratio of manual product-design times to CAD times range from 0.5 : 1 to 20 : 1. The 0.5 : 1 ratio represents complex mechanical de-

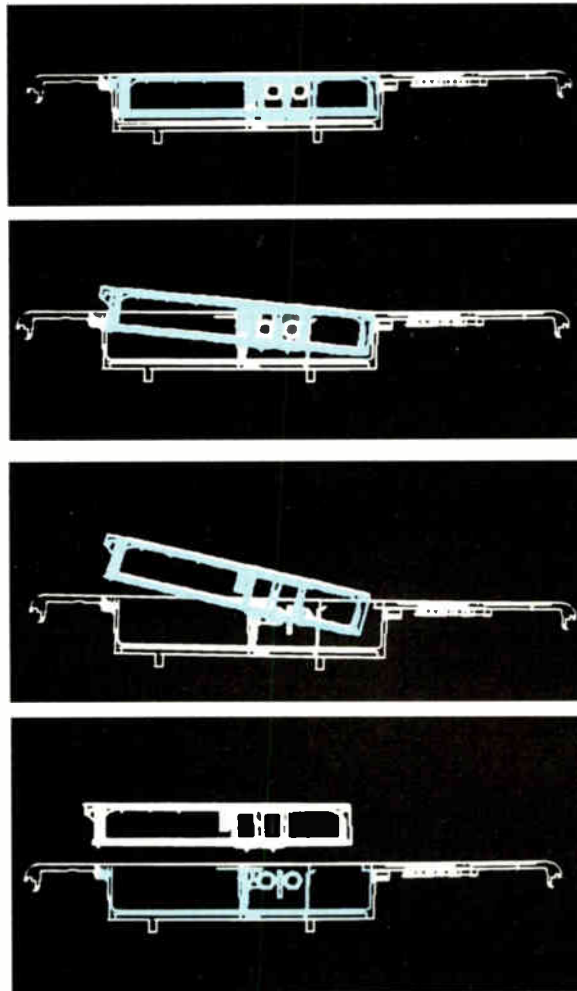
signs of radio housings requiring over 5,000 CAD entities, such as lines, arcs, and points, and designs of multilayer printed-circuit boards with over 17,000 entities. Part designs that are already in the data base reach a productivity of 20 : 1.

Whereas CAD applications are important in the product design and development process, CAM is equally important for the manufacturing process. This CAD/CAM data base forms a foundation for CIM, where all operations are linked into a comprehensive data base. CIM, in its broadest definition, lets the user integrate an organiza-

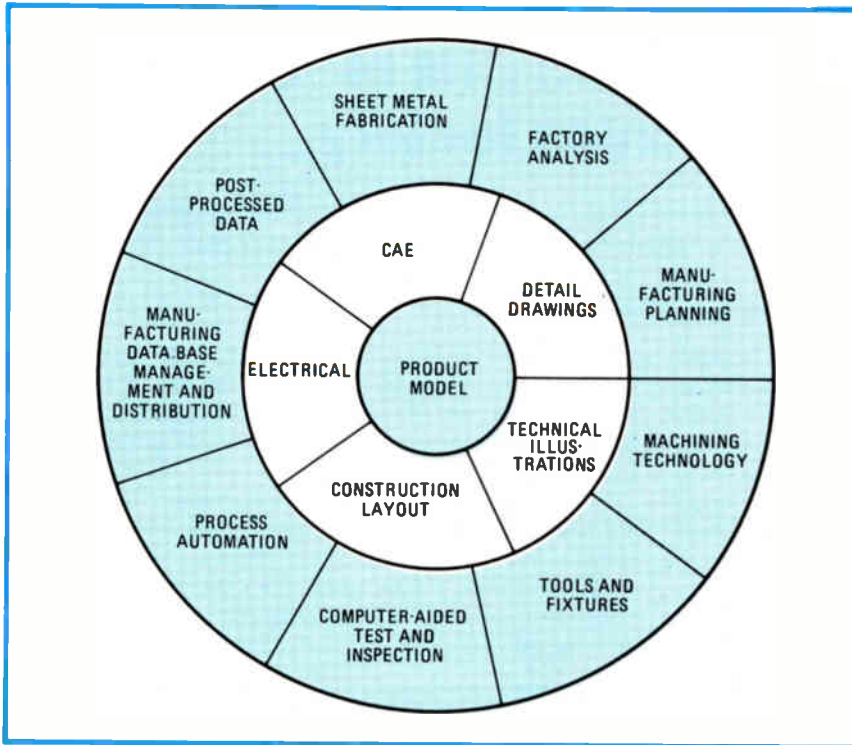
tion's design, engineering, manufacturing, and business functions. But in order for CIM to work most effectively, users should focus first on developing the CAD/CAM data base and leave till later the job of integrating it with their various machines and manufacturing processes.

For example, the design of a pc board begins with the entry of the components' schematic data and graphic representation into the system. From the schematic, a net list is generated to use as input for the autoroute program, which automatically interconnects common signal pins on the board. Once the interconnections have been checked and edited, the pc-board data base is used to produce full-scale artwork, drill information, and documentation. This CAD/CAM data base is now being expanded into a CIM data base, from which information is extracted to produce data for automated assembly, graphical aids for manufacturing processes, pc-board inspection, and in-line testing.

Several areas for CIM ties are being addressed. A few years ago, for instance, the



1. Open and shut. A CAD system checked the battery panel of Motorola's portable computer for opening and closing clearances by going through a sequence of motions based on part geometry stored in the system's data base.



2. One base. An automated factory needs to integrate the data bases for CAD and CAM (center and inner ring) and CIM (outer ring).

Documentation, like blueprints for numerical-control processes, could use CIM. Designers from Motorola's technical support groups are now beginning to use the design data base to develop designs for multipurpose fixturing and tooling.

First, to evaluate the project's technical feasibility and financial impact, pre-audits must be completed for all potential CIM applications. A CIM steering committee set up to deal with strategic decisions does this evaluation. Then, a technical task force deals with the implementation of these decisions.

CIM is being implemented in two stages at Motorola. The first deals with the procedures and software necessary to run the machine tool; the second provides the communications link between the CAD system and other automated equipment. As

links are implemented, follow-through activity with post-production audits occurs on a six-month basis to measure dollar payback and productivity.

Facilitating this development are expanding uses for the centralized data base. These include computer numerical-control machine centers for metalworking but extend beyond to a host of more exotic high-technology machines and processors—such as laser trimmers, optical scanners, and robots—for electronics manufacturing.

It takes training

A major CAD/CAM training effort is in progress, with a full-time trainer conducting classes each day. Already from January to September 1983, 63 designers have received some 2,500 hours of instruction. The program features advanced classes concentrating on such areas as numerical control, advanced pc-board design, and finite-element modeling.

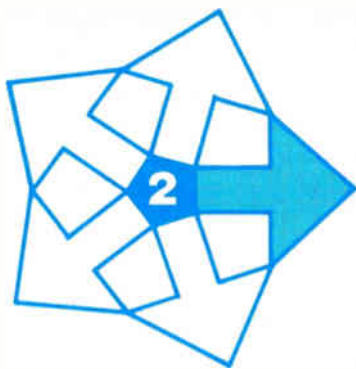
Basic classes in pc-board and mechanical design include two weeks of classroom instruction, while most advanced classes take one week. Advanced classes provide a deeper understanding of particular CAD/CAM and CIM operations and also increase familiarity with nongraphics operations, which helps to increase productivity. Training seminars, which are held occasionally for experienced users, cover the generation of data output from the CAD/CAM system to new machine and process ties in development and manufacturing.

Organizations throughout the Motorola facility are continually requesting ties. Software development is becoming of major importance: in many cases, simple-to-use software is needed to bridge gaps as the CAD/CAM data base is enlarged into the CIM data base (Fig. 2). Integrating the CAD/CAM data base with manufacturing machines and processes requires careful planning.

tiny electronic sockets on pc boards were inserted manually by many people on several production lines. These people are now applying newly learned skills in more responsible positions. In their place are variable center-distance machines for socket insertion. These machines provide component locations and tool-path routing with a corresponding X-Y coordinate for insertion through tape outputs from the CAD-system data base. Ongoing CIM links include coordinate measuring, pc-board routing, chip-component placement, laser trimming, and use of robots. Thus, with the same number of people, industrial output increases significantly, while employees learn to apply new skills.

Early this year, a Brown & Sharpe VC1000 four-axis machine center and a Computervision Designer M CAD/CAM work station were added to Motorola's model-shop facility, and machinists there have learned new skills in numerical-control tool-path generation. The Designer M station was selected because it is compatible with the current CAD/CAM-system data base and with the Brown & Sharpe machining center, which can handle the tiny and precise repeat machining needed in pc-board manufacture, as well as the machining used to create mold bases and similar products.

The machine center develops 11 horsepower with a spindle speed of 4,000 revolutions per minute, has a table measuring 24 by 46 inches, and has a full fourth axis that allows many machining functions to be performed without changing holding fixtures. This machining center has an automatic tool changer that is capable of holding up to 24 tools and can change tools automatically in 10 seconds. Several programs have been developed allowing this complex machine center to make all the machined components for portable-communications radios and their accessories.



Decision support helps manage flexible manufacturing systems

With software making the decisions, managers can quickly and accurately set up, troubleshoot, and alter a modern production line

by Ivan Johnson, Charles Stark Draper Laboratory Inc., Cambridge, Mass.

□ In today's rapidly changing markets, flexible-manufacturing systems that allow random production of small product batches on the same line have become the stuff of dreams for managers wanting to alter and control production flow easily and inexpensively. But because many systems' components must be interconnected, the decisions that must be made by operators during production can be very complex.

Besides the difficulty of scheduling a mix of machines and parts when so many parts and tools have to be dealt with, conflicting objectives complicate the production process. These can include maximizing throughput, balancing machine work loads, meeting due dates, enhancing the operation of the FMS, and minimizing tool changing and handling. Such problems call for computer assistance in the form of decision-support aids. A computerized support system can help manufacturers meet such flexible-manufacturing goals as high equipment utilization, reduced direct-labor costs, and reduced work-in-process inventory. It can also let them respond to demand-volume changes and machinery outages relatively easily, without having to make substantial changes in the fabrication-line configuration.

Computer-based aids support an operator in two ways: they make decisions that the operator may or may not choose to implement, and they forecast the impact of these changes. In this way, an operator can explore with relative ease several high-quality alternatives and get a clear presentation of their impact.

Decision-support aids implemented to date have focused on discrete parts metal-cutting and batch job-shop manufacturing. As flexible-manufacturing systems spread into the electronics industries, however, these methods can be applied as well.

Planning and operations management for an FMS is decision-intensive—and information-intensive—from the first conceptual design to the day-to-day scheduling and dispatching of a suitable product mix. The decisions faced by a planner and plant manager are composed of work and hardware selection. These decisions begin as early as the factory's planning stage and continue through actual production.

Work selection proceeds through four steps: part preselection, part se-

lection, part grouping, and scheduling-dispatching. A decision-support aid for part preselection eliminates candidates when factors like geometry and process requirements make them unsuitable. From this general list of parts, the most economically attractive subset is selected. These parts are then grouped according to which sets will work together most effectively. Finally, for each work cell a work sequence is selected that meets deadline requirements, balances the assigned work load, and helps to minimize in-process inventory.

Hardware selection follows a similar pattern and comprises four parts: machine selection, materials handling and fixturing, utilization, and operation and changing conditions. First, machines that are appropriate for a flexible-manufacturing system are selected, and a subgroup best suited to the candidate workload for characteristics like capability, cost, and return-on-investment is picked. Then, the most efficient materials-handling system for the proposed production process is selected. The next step balances the various tasks among the work stations or cells, so that the work load is distributed evenly. Once the line is set up, a schedule for tool transfers must be designed, so that work-station outages cause only minimal disruption.

The figure represents products assigned to a flexible-manufacturing system in subgroups for concurrent manufacturing during different time periods. For instance, group 1 might include 42% of the product items during the first two weeks of the month, a second group might include 37% of the items during the third week, and a

WORK STATION DUTIES AND TOOL SELECTIONS			
Work station	Work segment	Required tools	Number of empty slots
1	part segment 1 - A	No. 17, 22, 25	2
	PS2 - B	No. 18, 22, 27, 28	
2	PS1 - B	No. 9, 52, 71	3
	PS1 - C	No. 9, 52, 70, 82	
3	PS2 - A	No. 17, 18, 52, 59	2
	PS2 - C	No. 17, 52, 70, 84	

The advertisement features a dark background with several metallic components. At the top left, the 'ELMET' logo is displayed in a stylized, outlined font. To its right, the words 'MOLYBDENUM' and 'TUNGSTEN' are written in large, bold, white capital letters. Below this, the text 'AND ALLOYS FOR THE ELECTRONIC INDUSTRY' is centered. In the middle section, a list of products is provided: 'POWDERS', 'RODS', 'WIRES', 'RIBBONS', and 'SHEETS'. At the bottom, the company name 'AMERICAN ELECTRO METAL CORP.' is printed in a bold, white font. The background images include a large cylindrical rod, a smaller rod, a thick metal ribbon, several thin rods, and a tray containing a pile of fine powder with some wires and a coil nearby.

ELMET

**MOLYBDENUM
TUNGSTEN**

**AND ALLOYS
FOR THE
ELECTRONIC
INDUSTRY**

**POWDERS
RODS
WIRES
RIBBONS
SHEETS**

AMERICAN ELECTRO METAL CORP.

Office: 165 BROADWAY NEW YORK, N. Y.

Factory: LEWISTON MAINE

tively low-level sounds produced by intruders moving around within vaults. Pickup devices range from sound-pressure actuated non-electronic "switches" to crystal and other type microphones having inherently low noise levels. Where microphones are used their output is amplified and then rectified and the resultant d.c. actuates a signal relay.

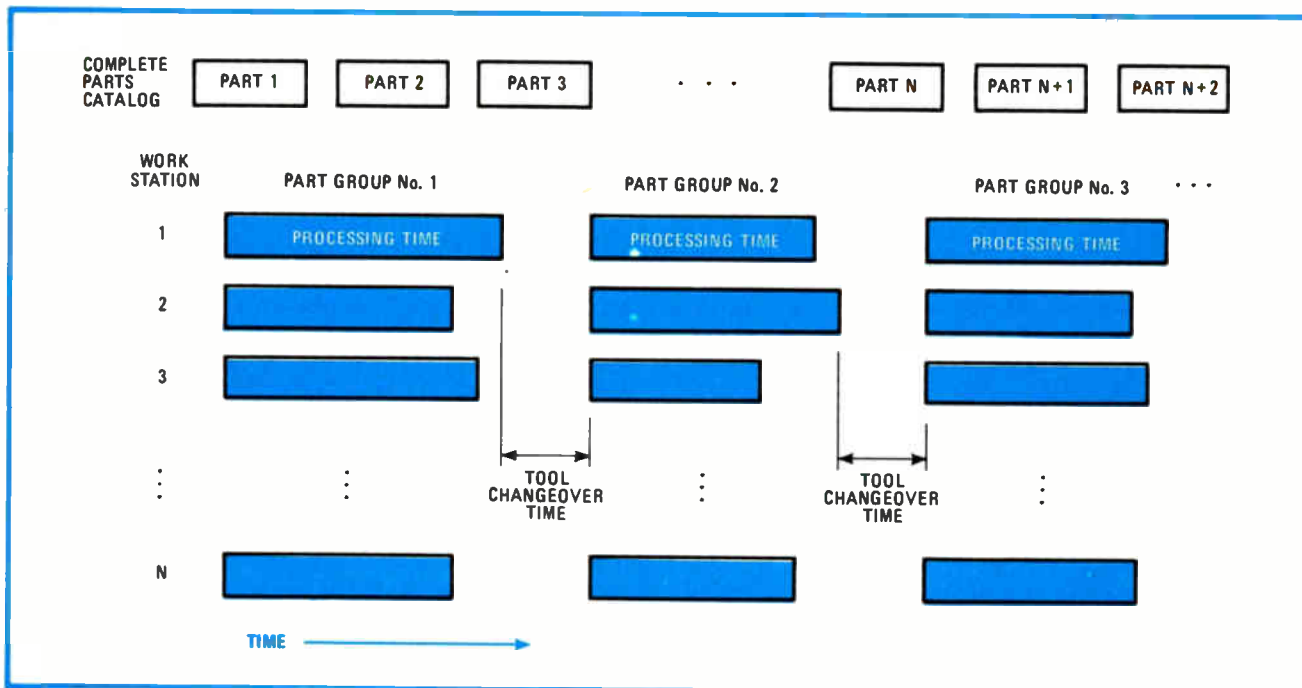
Sensitivity required of vault alarms depends upon whether or not vaults are reverberant or non-reverberant, a non-reverberant vault being normally defined as one in which the average coefficient of sound absorption of exposed interior surfaces exceeds 0.5, or is variable because of merchandise in storage. In reverberant vaults it is customary to adjust alarms to transmit a signal at sound levels of the order of 80 to 90 db for a sound of impact origin. In non-reverberant vaults the alarm systems should transmit a signal at a sound level 15 db above the normal ambient. Required amplifier frequency response varies with the type of vault and its contents, most frequently encountered conditions requiring a range readily obtainable through conventional a-f amplifier design.—MacDonald, *ELECTRONICS*, February, 1942, p. 38.

**Engine Cylinder
Pressure Indicators**

MECHANICAL INDICATORS were used for many years to study the pressure variations inside the cylinders of internal combustion engines. Electronic indicators having less moving-part inertia are now generally used, the usual method of measurement involving conversion of pressure variations into electrical variations and the reading of the electrical variations on the screen of a cathode-ray oscilloscope.

One method of conversion involves the insertion of a small, flexible and highly polished metal diaphragm in the wall of the cylinder under test. A light beam is directed at the diaphragm and is reflected to a phototube. As cylinder pressure variations flex the diaphragm, light reflected from it diverges and a lesser amount, proportional to cylinder pressure, reaches the phototube. Phototube output is thus proportional to cylinder pressure.

Other energy conversion devices



Flexible batch manufacturing. Because parts may reach the factory at different times and only a certain number of work stations can build a certain unit, the order and flow of product parts must be carefully considered when a flexible manufacturing system is set up and operated.

third group might handle the products remaining during the final week.

One reason for grouping parts is their schedule of availability at the FMS-input stations. For instance, if a certain component is not expected to arrive until late in the month, it may make little sense to configure some work stations for that component's production. Another motive might be the finite capacity of auxiliary materials or tooling on the work cells, which act as constraints on the system so that some items can be produced only during specified times.

Solving a problem

A decision-support aid developed by Charles Stark Draper Laboratories under the sponsorship of the U. S. Army Defense and Readiness Command (Darcom) and guided by the Tank-Automotive Command (Tacom) solves the problem of specifying these times and assigns specific work segments to specific work stations, along with auxiliary equipment, materials, and tooling. To solve the problem, the following factors are considered: production quantity and due dates, raw- and auxiliary-materials availability, materials-handling equipment availability and capacity, and user-input rules regarding the potential for sharing auxiliary materials (such as tool sharing across parts).

The result is a schedule of time intervals, during each of which a different mix of parts may be produced, and the work cells are configured accordingly. This organization is set up to meet due dates and production targets, as well as to maximize machine utilization and system throughput. The problem's complexity makes manual resolution impractical. Further, changing production targets, inserting urgent orders, the failure of work-cell equipment for substantial periods of time, and other cir-

cumstances may require the problem to be resolved several times a month or even daily.

Once the product groups have been defined for an FMS, the problem of sequence remains. A decision-support-aid scheduler can take into account the following factors: production requirements and due dates, work-cell availability, work-segment content, avoidance of scheduling work past the shift's end, and the materials-handling capabilities of the system. Aspects such as choosing products most suitable for third-shift, unattended production and prioritization based on reducing current work-in-process inventory can be accommodated easily by a sequential-decision approach, which is a common feature of these decision-support-aid modules.

A scheduler linked with the control system would track real-time work-cell and materials-handling status. It could thus forecast when the next few parts will leave the system and schedule variable worker breaks or fixture access from storage in anticipation of its use. Commonly used interval or demand schedulers, which can neither maintain a reasonable balance of work across the system nor prioritize products that are falling behind schedule, lack the flexibility of this approach.

As FMSs become more complex and are used to manufacture larger groups of products—over 600 pieces, rather than the current 30 to 40—the flexible characteristics of the decision-support-aid scheduler will become even more effective. Furthermore, the scheduler's heuristic formulation permits the code to be tailored readily to each individual application, providing both flexible planning and operation aids for flexible fabrication.

Typical FMS setups use redundancy to permit work on a particular part at two or more alternative work cells: if one of the cells goes down, the part in question may still be fabricated on a remaining cell, albeit at a reduced

production rate. When the reduced production rate would not be acceptable or the backup capability offered by work-cell redundancy has not been provided, it must be decided whether one or more operating work cells should be reconfigured to permit full-scale fabrication of one or more parts while the failed cell is being repaired.

Using the React module

A React decision-support aid first determines whether tool complements on functioning machines could handle extra work segments. For parts that cannot find an appropriate tool to share, empty tool slots are sought in conjunction with subsets of available needed tools; if a slot is found, it may be outfitted with the appropriate tool. Failing this, an operator may elect to return to the parts-grouping decision-support aid and redefine the parts groups.

The React module, in conjunction with the scheduler and FMS simulation, can also be used to explore a series of alternative tool transfers according to production rates. Because its basic approach permits straightforward evaluation of proposed urgent part insertion into an otherwise smoothly functioning system, it can indicate which work station can most efficiently accommodate the proposed parts and estimate the impact on other parts already in production.

A simple example of how the React module would work is shown in the table, which lists three work stations in a hypothetical FMS and each station's tool list. The work stations are similar, although they are set up differently. Each handles two different part-insertion work segments nonredundantly.

For example, if a device in work station 3 fails, an operator must decide whether to move some or all of that station's work segments to another one. If so, then a good changeover scenario must be determined. A check is made first to see if any tools need to be transferred. For part segment 2-A, neither work station 1 nor 2 has sufficient tooling; this is also true for part segment 2-C.

The next step is to check for a combination of like tools and empty tool slots that could accommodate the parts being built on work station 3. Work station 1 has two tools in common with work station 3—numbers 17

and 18. It also has two empty slots available for numbers 52 and 59. As a result, part segment 2-A is assigned to work station 1. Part segment 2-C would be assigned to station 2 in a similar fashion.

In some situations, a part insertion could be done on more than one station or on none at all. In addition, as the complexity of building a device grows, so do its possible rerouting choices.

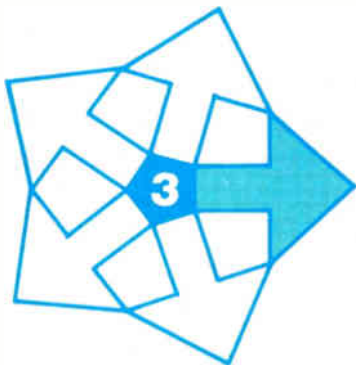
A sequential approach

Underlying the software is a sequential-decision approach. Many other optimization scenarios impose computing requirements that tend to grow exponentially. The sequential-decision approach, however, imposes computing requirements that grow polynomially with the number of problem elements, thereby cutting the computer-resource load by orders of magnitude for problems of reasonable size, like those requiring 10 to 15 machines and 50 to 100 different parts.

Also to be considered are multiple-attribute tradeoffs; these are often dealt with by voting schemes, in which different attributes have different numerical weights that are chosen by the decision maker. This method may appear to be arbitrary. Sequential-decision methodology, however, trades off attributes not just by numerical weighting factors but also with estimates of the probability of assigning all the remaining needed elements satisfactorily.

The basic approach is to list all the problems to be dealt with and to define the basic constraints of the problem. This list is then processed, at which time a probability of success is computed for each candidate. The item with the highest probability of success will be chosen in the current iteration. It is withdrawn from the list, and the process is repeated until either all the candidates are assigned or one of the resources is exhausted.

The sequential-decision approach goes a long way from strictly random assignment toward full optimization. It does not look at earlier decisions and, in this way, is not truly optimal or exhaustive. In some product-line-grouping problems, the work cells were used about 79% of the time, compared with 85% for truly optimal solutions and about 60% for purely random ones.



Network lets different devices communicate on the factory floor

Different makes of terminals, computers, instruments, and controllers can talk with one another through the Factory Information System

by Jerold L. Stockweather, *Advanced Control Technology Inc., Albany, Ore.*

□ Although all the physical tools for computer-integrated manufacturing have by now been developed, the fundamental problem of getting dissimilar makes of devices to communicate and interface with one another and with their human overseers continues to perplex engineers and

factory-floor workers. A number of firms are now offering solutions that force users to purchase the products of one company—an impractical and costly prospect for a facility that is trying to upgrade its manufacturing process rather than start from scratch. However, the Fac-

tory Information System (see figure) is one network that is indeed designed to talk with many different types of equipment, from many different manufacturers.

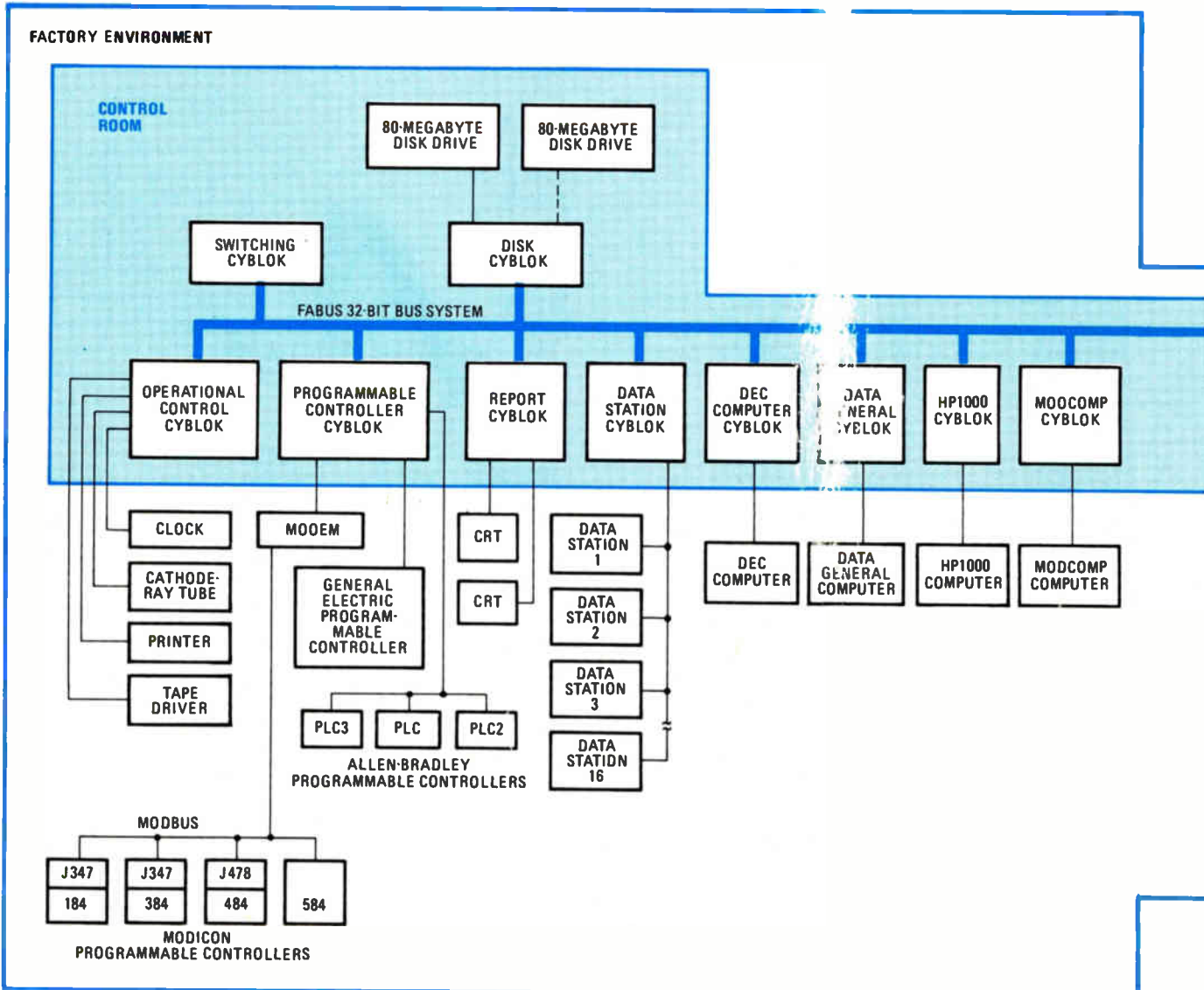
The Factory Information System, which is being implemented in five phases, will be finished this coming December and promises to tie together on a common network the communications, displays, computers, programmable controllers, and instrumentation systems that form the controlling heart of the factory. The network is based on Gould Inc.'s Factory Automation Bus and Gould Cyblok controllers, which act as the interface between the devices and the network.

Through an industrial network, the system allows communications to and among programmable controllers by Allen-Bradley, General Electric, and Gould/Modicon; instrumentation controllers by Fisher, Foxboro, Honeywell, and Taylor; computers by Data General, Hewlett-Packard, Digital Equipment Corp., International Business Machines, Gould/SEL, and ModComp, to say nothing of a great many different peripherals, such as displays, data-entry stations, and printers, among others. This combined hardware and software information sys-

tem as a result creates a total plant data-communications and information system.

A factory information-system network requires both manual and automatic data collection, so that the benefits of the controller may be tapped. Manual data collection is accomplished either through a manual data-entry station by operators, maintenance personnel, and supervisors for product codes or downtime reasons or through a bar-code-reader station for product type or finished goods. This type of data collection requires accurate and timely entry, and the factory controller acknowledges that it has received the data and transmits an acknowledge signal back to the data-entry station.

The system's automatic data collection is provided by interfacing production-line programmable controllers with the network. Timers, counters, machine status contacts, and alarm data stored in the programmable controller's memory registers are therefore polled continuously and update the factory controller's data base. This type of factory data—including production counts and alarm faults for machines, conveyors, and palletizers; the temperatures and the pressures of curing ovens; and qual-



ity and calibration data from inspection and testing stations—does not require the intervention of operators to be entered into the Factory Information System.

By combining these two methods of data collection, a factory worker can easily gather and implement the information needed to run a plant efficiently. This real-time data, not just reports that might be hours or days old, results in better supervision and control. For example, if a data terminal is used to enter such reasons for downtime as idleness and lack of material, that information can later be correlated and analyzed for statistics like mean time between failures or mean time to respond. Such features as a help function, which would inform centralized supervisors about any problem and give them the data, lets production-floor workers get assistance quickly and minimizes downtime.

Network configuration

The network has three main features: standard interfaces, factory controllers, and special data-entry and display terminals. Gould Inc.'s 32-bit Fabus bus system and the software and Cyblok interface units are the basis of the network. Each Cyblok is specifically configured through an operational-control Cyblok unit, so that peripheral devices can communicate with one another in the network. In addition, each of the network's Cybloks has a software driver written for it, so it can communicate with the devices attached to it.

The data base is configured through the operational-control Cyblok. The Factory Information System directs and preprocesses information through a distributed network of microprocessors and minicomputers that inter-

face with the factory through the Fabus network. It accesses and stores the system configuration and thereby permits each Cyblok to communicate with the others in the network. In addition, the controller continuously scans all of the connected devices to offload and acquire data for preprocessing, for display, for sending alarms, and for reporting.

All of the commands and information are routed through the system's data base, which has a maximum storage of 320 megabytes, resident on four 80-megabyte Winchester disk drives. This data base allows data terminals to implement maintenance dispatch, factory diagnostics, and other application tasks through the factory controller. Designed to be used by factory personnel, the controller does not slow down in performance as units are added to the network.

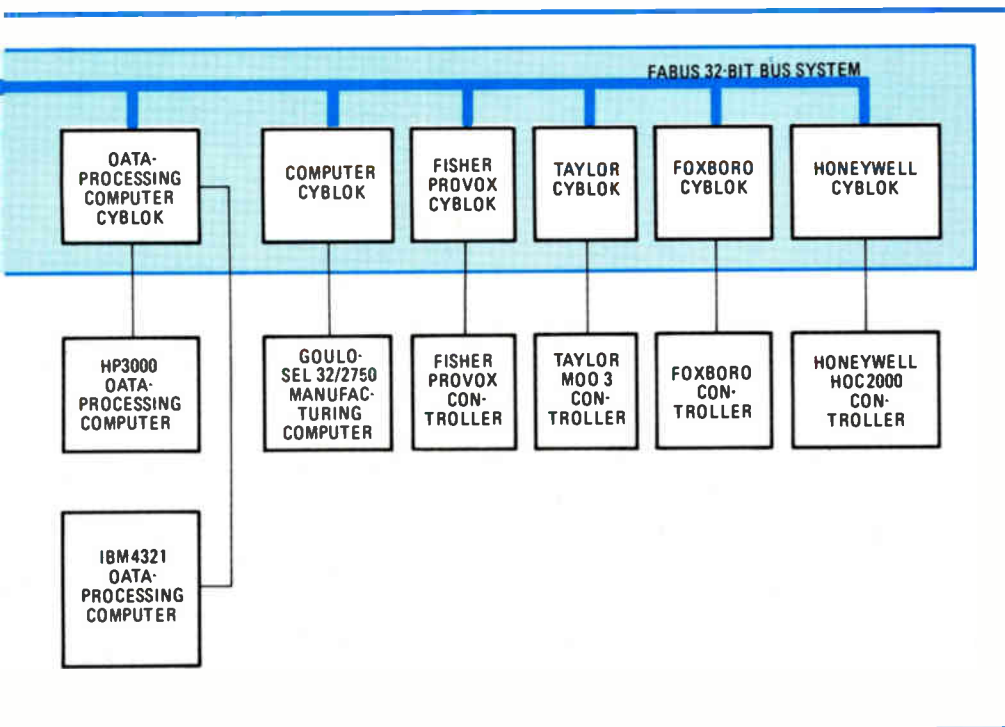
The controller uses information from the system to generate reports for factory personnel. To help analyze the efficiency and productivity of machines, production reports are generated in real time for each section of the factory. Downtime reports are compiled for maintenance evaluation and for preventive-maintenance scheduling. Work-order generation and tracking can be implemented in addition.

Functional interfaces

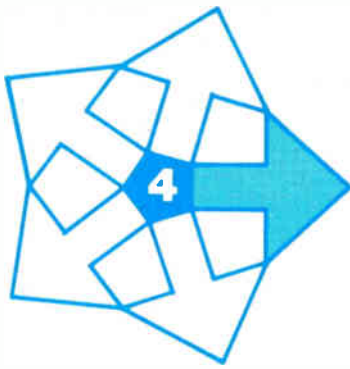
As many as 16 functional Cyblok interfaces can be connected to the data bus of any one system. If additional computer power should for any reason be needed, a transfer-interface Cyblok can be used to link two systems together, thus increasing the total number of possible Cyblok interfaces to 32.

Each Cyblok has two ports capable of interfacing with a certain type of device. For instance, as many as 20 programmable controllers can be linked in parallel for each line. For the computers, a single computer is dedicated to each port of the Cyblok, but for the instrumentation controllers, the entire Cyblok is dedicated to the unit.

Both managers and production-floor workers benefit from such a system. They may now quickly receive accurate and up-to-date production data in real time. This information can then be stored in a data base and used for future reference or control. In addition, such systems allow plant awareness, consistent sensor calibration and monitoring, and the ability to program the different devices spread throughout a plant from a central location.



Netting a factory. The Factory Information System is capable of linking the terminals, programmable and instrumentation controllers, and computers of different manufacturers on a single network. It does so by using Gould's Fabus 32-bit bus system together with Cyblok controllers, which are kept in the factory's control room and are linked to devices on the factory through an industrial network.



Simulation software eases robotic work-cell construction

Four software packages permit manufacturers to design, debug, and test work cells with just a light pen and a keyboard

by Nick Jackovich, *McDonnell Douglas Automation Co., St. Louis, Mo.*

□ Now that the robot is becoming the strong right arm of the automated factory, a different kind of factory foreman is emerging—one who watches machines rather than people. Besides monitoring machines during production and repairing them when they break down, these new factory foremen must also set up and train each robotic work cell for a particular job by laboriously “walking” the robot or robot team through a production process. Alas, this training sequence is time-consuming and costly to implement, and it does not readily exploit the mil accuracy of many robots.

With the right software these obstacles can be overcome. McDonnell Douglas Automation Co. (McAuto) has developed a quartet of programs (Fig. 1) that make a variety of robots and work-cell fixtures more cost-effective and flexible: Place, a graphics-oriented manufacturing-cell-design and -analysis system; Build, a system that automatically creates the kinematic, or motion, control of a robot's movements; Command, an off-line programming system for robots; and a new package called Adjust, a calibration tool that helps robots adapt to their work cell. Such tools permit robotic work cells to be programmed quickly and to be tested before they are built.

Place—positioner layout and cell evaluator—the heart of this software set, uses computers to create simulated and animated models that let users analyze every component in robot-controlled work cells (Fig. 2). With Place, such cells may be designed more than 70% faster than with conventional methods: drawing sketches and manually positioning the robot, the conveyors, the machine tools, and other devices.

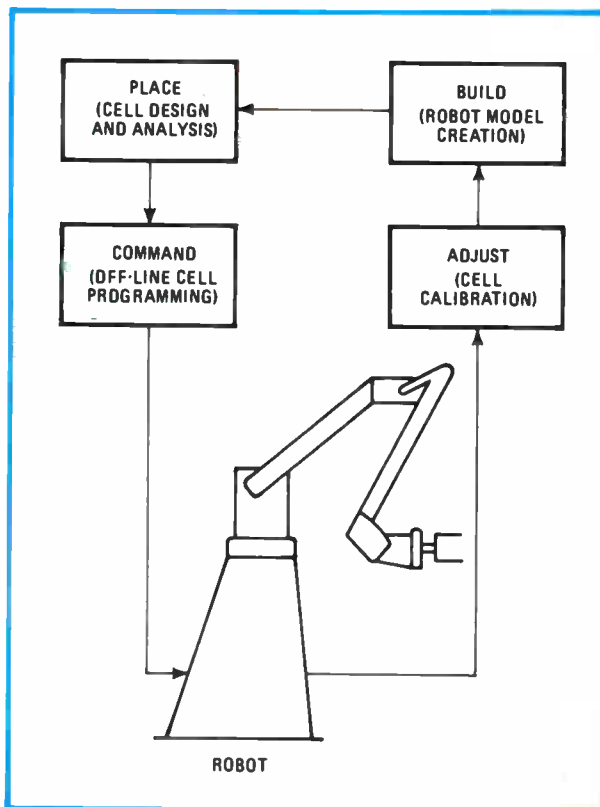
By facilitating quick, thorough cell-design analysis on

display terminals, before hardware commitments have been made, Place speeds up the implementation of robots. Many of those who use robots—large automobile manufacturers, for instance—buy them and create work cells in a trial-and-error fashion, only to discover that some setups just do not work. Place can prevent such mishaps and eliminate the need to tie up production facilities by testing work cells.

Place operates on Digital Equipment Corp.'s VAX minicomputers and is displayed on McAuto's R-100 work station, which is based on Evans & Sutherland's vector-refresh display terminal. Three-dimensional models of a robot's manipulator (arm), gripper (hand), and other fixtures are designed on a computer-aided design and manufacturing system and transferred to Place's robotic cell files.

When these cell devices are displayed on the R-100 terminal, a function called MOVE FRAME transfers them with respect to any point in the cell or rotates them around any point, so designers can solve reach and location problems quickly. The R-100 work station has a second cathode-ray-tube screen, which displays messages that help users operate Place, and a function keyboard, control dials, and a data tablet. A hard-copy plotter, which makes drawings of work-cell designs, can be tied into the work station, too.

Place's cell-description files contain graphical representations of all cell components, including the necessary geometric and kinematic equations for each robot in the library. Robotic motion and arm-reach capabilities vary, like those of human beings, so Place describes the limits and allowable movements of each robot joint dynamically. This function lets Place users compare and evaluate



1. Learning by software. Because of four software packages called Place, Command, Build, and Adjust, a work cell for a robot may now be designed and adjusted on a screen rather than on the factory floor—an economical approach. Place helps design the cell, Command programs the robots off line, Build works on their motion control, and Adjust calibrates them within the work cell.

different robots in the work cell, providing them with the best possible cell design and making them more productive by freeing them from manual programming activities. Without Place, these comparisons and evaluations can be made only with an investment in robots themselves.

Place helps save time for end-effector design, as well. Work cells must often be rearranged to accommodate the gripper, which varies according to task. Place puts on and takes off grippers graphically while the work cell is in the course of being rearranged and before hardware commitments have been made.

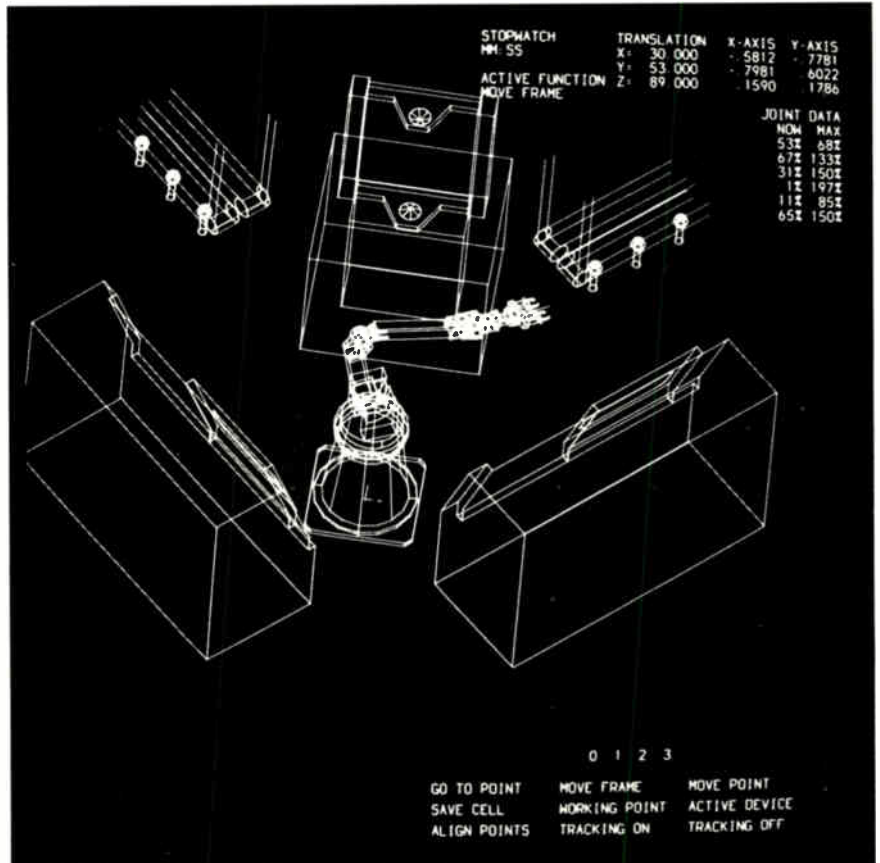
Animated work cells are created by using a graphics stylus to identify the destination, or GOTO points, of the robot's end effector. As the designer touches the stylus to the data tablet and selects one of several GOTO points, the animated representation of the robot moves its end effector toward the point, with the user controlling the robot's motion and speed.

While the robot is moving toward these destination points, the CRT displays its joint positions for analysis. Two columns of real-time data represent these positions, measured as the percentage of each joint's total available motion utilized by the arm. One column displays the current (and continuously changing) position of the robot's arm, and the other column indicates the most extreme position it encounters. A value of more than 100 indicates that the robot has exceeded a joint limitation; a value of zero indicates the midrange of joint motion.

By combining the motions of a robot going from one point to another, designers can form motion sequences just by specifying what functions the robot is to perform. These motions are stored automatically in a process sequence. Once the sequences have been defined, they are combined, replayed, and graphically edited to simulate a continuous work-cell operation, and the real time of a sequence can be determined by a stopwatch function that is displayed on the screen. A whole operation can be worked out before any robots have been bought.

Another feature of Place is the ability to detect collisions between robots and cell parts. Hardware control dials let designers change the viewing orientation of cells dynamically and use scaling features to get a close look at particular parts of cells (Fig. 3). In order to make viewing easier, unwanted geometry positions can be blanked from the screen.

A conveyor system's operation can be simulated, too. By activating a tracking function that commands the robot to follow a part to its designated destination, this



2. Place your robot. The Place interactive software package, which runs on a Digital Equipment VAX computer, uses simulation and animation techniques to design and lay out a manufacturing cell, which may include robots, machine tools, inspection machines, conveyors, and fixtures. Because Place allows such cells to be designed rapidly, it is possible to employ robots even in short production runs for machining, welding, and assembly.

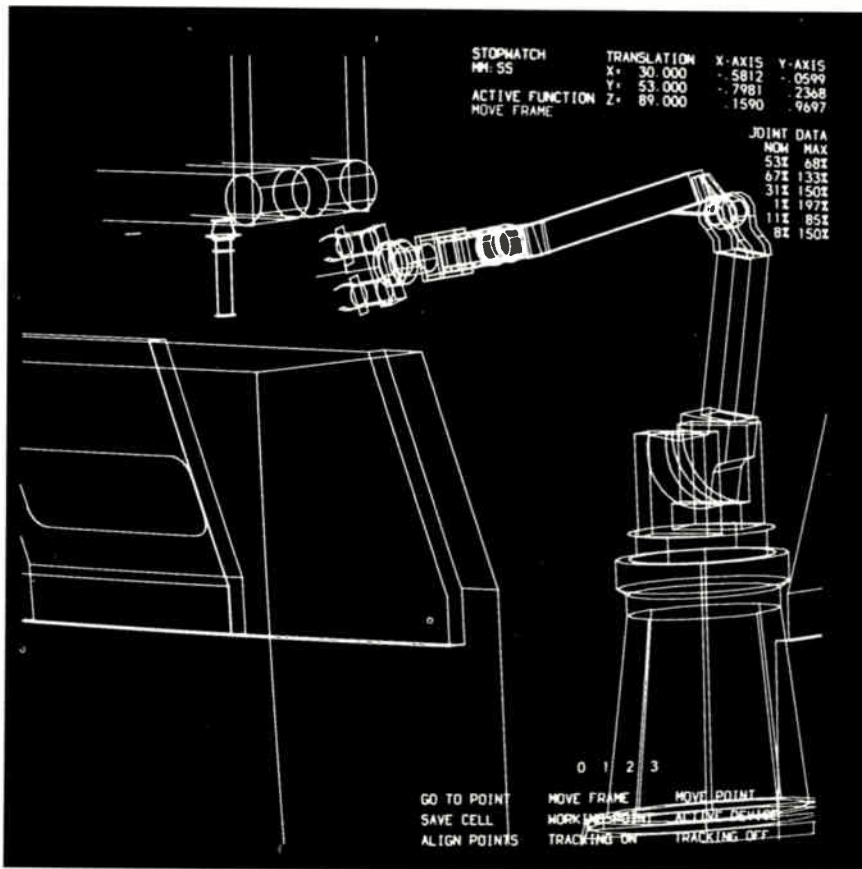
function shows where the robot should start to reach for the incoming part and where the robot is no longer capable of reaching it.

Build, the system that automatically creates the motion control of a robot's animated movements, is an effective solution to an otherwise serious limitation of any system for designing and analyzing robot cells: a small data base of robots. By providing automatic kinematic analysis and a program that prompts users for information, Build makes it easy to describe new robots for the computer model. All users need in order to add new robots to the system library is a basic knowledge of robot kinematics.

The Place library now contains 18 robots, any five of which are included with every basic software package. The library consists of a set of simple file entries containing information on the robot's degrees of freedom, type of joint motion, and motion limitations, among other things.

Giving commands

After a cell has been designed and analyzed, an off-line program can be developed with Command. Most robots are programmed in the teach mode, so programmers must physically lead them through the motions with teach pendants. These sequences of teach points and



placed on the robot's arm may cause the robot to deviate from its off-line programming position. Some work cells, such as the large, complex ones involving many work units, may require several off-line programs plugged into a central control system to coordinate the work units. Work cells that are coordinated by a robot controller may need only one off-line program.

This system is a vast improvement over teach-mode programming. But one off-line program will not work for all robots. Because of the great variation in standards, no two robot manufacturers make robots in the same way. There are many models of robots, each having a different language that must be adapted for an off-line program. But with a single simulation package, users will have to know only a single off-line language.

Time for adjustment

Once a robot has been designed, the hardware implemented, and the robot programmed, the actual cell may or may not match the Place cell perfectly. Tolerances that are permitted in the installation of the production cell may create locational differences between the real-world shop

3. A closer look. Using the R-100 work station's zoom feature, manufacturing or assembly cells designed with Place can be enlarged, so that the operator may submit the equipment and processes to close inspection for proper operation, interference, or collisions.

operations are stored for later replay. Teach-mode programming wastes time, ties up production equipment that could be used for actual production, and is somewhat dangerous, especially with larger robots, because the programmer must work on the shop floor, within the robot's work envelope.

The off-line Command system has no such drawbacks. Together with Place, this software permits users quickly and easily to develop and debug programs for robots. Place defines, graphically displays, and records the required robot motions—for instance, the velocity of a robot's arm movements—as a sequence. The sequence is then played back, so that errors can be detected. When the robot's sequences and cell makeup have been perfected in Place, they are passed back to the CAD system interfaced with it, drawings of the cell are made, and the cell is built.

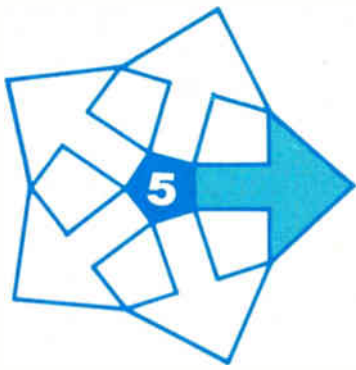
The Place sequence information is next sent to the Command software, which processes the Place data and combines it with commands that are written in the language specific to a particular model of robot. Command generates a complete robot program, which can be sent to a cassette, a diskette, or an input device plugged into a robot's controller. Command then checks out the program for errors and validates the position points.

The complexities of the manufacturing process and the dynamics of the production work cell may create a need for teach-mode touch-up. For example, load stresses

floor and the ideal-world Place model. Minute differences in the work cell's dimensions can also account for such differences. On the shop floor, some work units can be misplaced by several inches or so without hurting the work flow of human employees. Robots, of course, cannot move on their own, so such work units as conveyor belts must be installed accurately.

Adjust, a calibration tool, increases off-line programming's effectiveness by updating the Place model to reflect the actual locations of the cell components. Adjust does so by feeding positional data about their spatial arrangements back to the computer, which updates the cell model. The Adjust procedure involves a calibration probe that users must mount on a robot's face plate or on the mounting area of an end effector. A calibration program written in the robot's native language is loaded into the robot controller, and the Command program then steps the robot through its required motions in the work cell while data is recorded.

Users then input this data to the Place system's Adjust calibration program, which updates the actual positions of the equipment in the Place cell. The result is a cell model that can actually take into account the errors affecting the robot's view of the real world. This updated information puts the robot programs closer to their desired positions in the robot cell and also reduces floor touch-up. The Adjust software can be used to recalibrate operational cells, as well.



On their own, robots build Winchester disk drives

With smart robots, advanced programming and control systems, and accurate parts handling, flexible automation can be class-100 clean

by Charles S. Duncheon, *Fared Robot Systems Inc., Denver, Colo.*

□ Though robots are typically thought of as lumbering workers that hoist and move objects in hostile environments, a breed of high-technology robots—accurate to a mil or so and programmable to emulate the movements of a human—are being put to work in electronics factories. For instance, by using a robot (Fig. 1) to build the head and disk-drive assemblies and the head-to-disk assembly and to test the components of a Winchester disk drive, a manufacturer can get a higher-quality product having a one-year payback time.

A robot system may be no faster in instantaneous-rate capability than a human operator, but it does have a higher throughput over several shifts. A robot cell that is designed as a system and properly maintained will deliver products on schedule a high percentage of the time (98% or more), with a constant throughput rate. Personal breaks or delays associated with people disappear with a robot cell. In addition, through the use of automated handling systems and remote programming and control, no human beings—often the dirtiest part of the system—come into contact with the product.

Substituting robots for people in a class-100 clean room, which has fewer than 100 particulates per cubic foot, can be a help to both labor and management. In general, clean rooms have a high turnover rate, which leads to high training costs and learning-curve errors. One computer-peripheral manufacturer who replaced a manual assembly line with a robot system reported a spoilage rate decrease from 24% to 4%.

Total assembly

A Winchester disk drive is assembled by robots in the same order that human assemblers go about the task (Fig. 2). First, the spindle, or hub, is built and sent to a robotic hub-and-disk assembly cell. There the disks containing the servomotor information, along with those for recording information, are loaded onto the hub and separated by robotic-inserted build spacers. Next, the disks are clamped to the spindle and, if required, sent to a station for total-indicator-readout testing, which indicates whether the disks

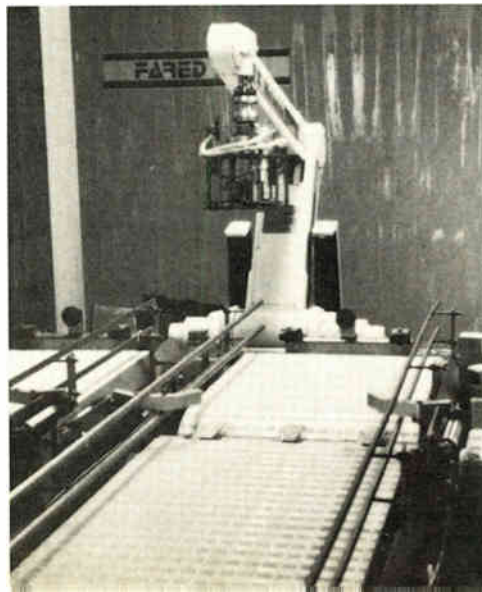
are centered and balanced properly. The disks are then balanced (if required) and sent to the head-to-disk assembly station, where the spindle with the disks is combined with the head subassembly. The final stage takes the unit to a station that assembles magnets, which are used to create the field that drives the assembly.

The operation sequence for robotic hub-and-disk assembly mimics the robotic assembly line (Fig. 3). As canisters of disks are sent down the conveyor, a conveyor sensor notes their position and activates a fixture in the work cell to accept them. At the same time, the spindle assembly, which is also sent to the work cell via a conveyor, is placed in a fixture. A conveyor sensor notes the position of this device and readies a fixture for acceptance. Finally, the build spacers that go between different disks are placed in an indexer so that a robot may handle them.

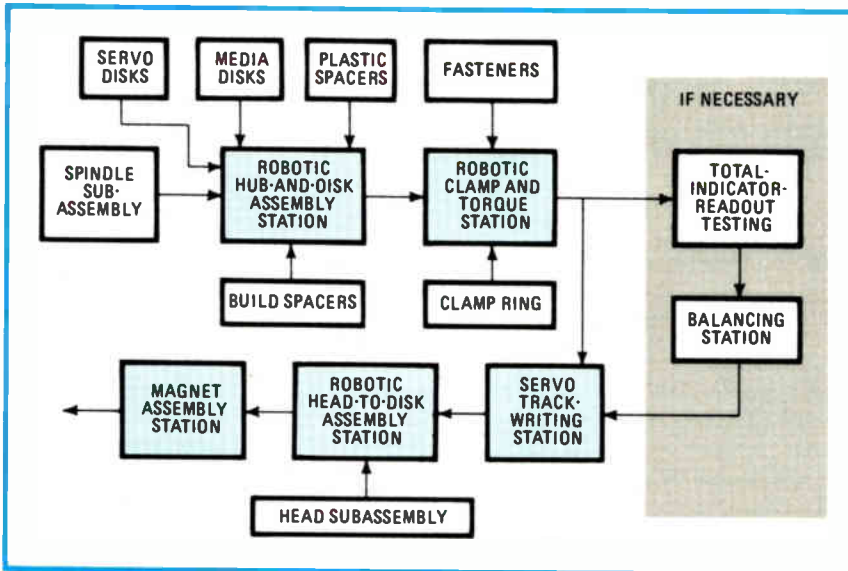
Once these steps are complete, the robot receives signals from all the sensors that all parts are in position for assembly. As the robot picks disks from a canister, it uses a search function built into the software control along with tactile sensing to ensure that the disk is picked up properly. Despite the low clearance between the disk and the hub—as low as 0.0005 in.—robots with ± 0.008 -in. repeatability can perform this assembly easily through adaptive control and compliant tooling. If misalignment occurs, however, a subroutine in the control software makes the robot search for the proper alignment without harming the disk. These steps are repeated for each disk placed on the hub.

The source of these smarts is a supervisory control center run by a minicomputer like a Digital Equipment Corp. LSI/11 or a programmable controller like a Texas Instruments 5. Control selection depends on the complexity of signal-coordination and quality-control requirements. The controller sends signals to and accepts them from microprocessors embedded in each work cell, like head-to-disk assembly, and sends signals to the microprocessors in the robot and the conveyor system. Each work cell has separate processors for various controls.

After the relatively easy chores of clamping, testing, and balancing are accomplished, the disk-drive assembly's read head is put on the drive. Building the head is usually a high source of spoilage



1. A strong arm. Using conveyor belts and robotic work cells, a Fared production line fully automates the head and disk-drive assembly and component testing of Winchester drives.



in human assembly (using people for this process results in a rejection rate as high as 30% from heads damaging disks during assembly) and may be automated with a high-precision electric robot, tight-tolerance fixtures, and slight modifications to the part designs. The read-head subassemblies are presented to the robots in precise position for pickup and insertion into the disk-drive assembly, which has been captured by a fixture.

To get the robot arm to move smoothly, its path and gripping sequence must be programmed precisely. This type of assembly is becoming quite popular with manufacturers, and many are beginning to use robots for such tasks [*Electronics*, June 16, 1983, p. 120]. The Japanese-developed Scara (for selective-compliance assembly robot arm) robot lends itself quite well to this task because of its inherently accurate motion in the horizontal plane.

Automated devices in the clean room must be placed with utmost care to minimize product contamination. If

2. Moving disks. Work cells are connected through a conveyor system, so that a drive assembly can move from one cell to another with no human intervention.

the air flow is horizontal, the build-up or product process should flow opposite to it, allowing the finished or assembled product to receive the cleanest air. In the case of top-to-bottom air flow, no moving mechanical parts should be placed above the path of the product.

Placement problems

Though it may be difficult to determine where devices should be placed within a work cell, the following formula can be used to compare layouts for hub-and-disk assembly. Z, which is an objective function for

manufacturing systems, is to be minimized for:

$$Z = \sum_{n=1}^N np \times D$$

where N is the total number of assembly parts, P is the part rating, and D is the distance through which each part moves. The part rating represents the importance of each part to final product quality. For instance, a disk may have a rating of 10, build spacers a rating of 8, clamps a rating of 7, plastic spacers a rating of 2, and the disk canisters a rating of 1.

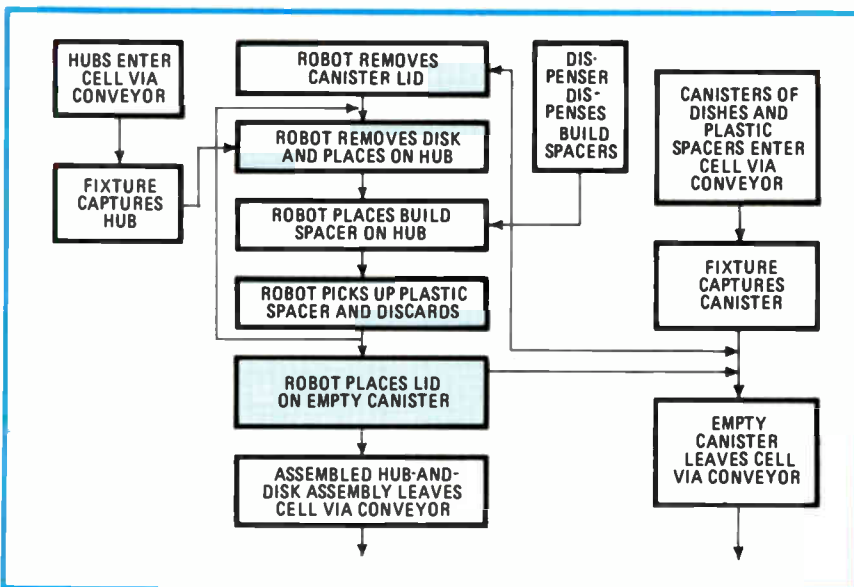
Robot types

The best robots for clean-room applications are electric servo-driven units because they are the most accurate. In placing such robots in a clean room, however, particular attention should be given to their lubrication systems to prevent particle generation. Additional guards and boots may be needed to cover up the joints.

Though five- and six-axis robots offer the most versatility for assembly operations, a four-axis Scara or cylindrical-coordinate robot can handle many tasks. Overhead gantry robots are not recommended because of the risk of particle generation over the surface of the product.

Disk drives lend themselves quite well to automated assembly because they require precision parts. This requirement, in turn, eases the integration of assembled units into a tightly controlled work cell.

One or two programmable robots with peripheral-handling equipment and fixtures can meet throughput rates as high as 20 units an hour, where those units may have three to nine disks per assembly. A common gripper is able to handle disks, incoming spacers, build spacers, and disk clamps. □



3. Hub to disk. The hub-to-disk-assembly work cell is typical of the cells on the disk-drive production line. It uses extensive control software along with sensors and programmed robots.

Chip set eases bit-slice design while tackling video-speed processing

PART 1

Multiple internal buses speed 8-bit-wide slices

by Jeff Niehaus, Jim Duval, and Jesse Glagle
Texas Instruments Inc., Dallas, Texas

□ Although the general-purpose architecture of typical computer systems is a reasonable compromise for a wide variety of operations, its performance is often insufficient when an application like image processing demands high speed in certain highly repetitive computations. In these high-performance applications, special-purpose architectures are more suitable—especially systems implemented with bit-slice components. These are the optimal approach because they make possible both the large word widths that are needed for high-precision calculations and the multiple internal data paths necessary for exploiting parallel computations.

Adding a new meaning to the term “bit-slice”—and bypassing older 4-bit parts in the process—Texas Instruments' SN74AS888 is an 8-bit, expandable, bipolar bit-slice processor that will offer the utilities required to perform these types of functions. Moreover, with the accompanying high-speed microsequencer also in development (see accompanying article, p. 135), designers will be able to create video-speed circuits without losing the flexibility of programmed architectures.

TI's advanced Schottky process technology, called Impact (for implanted, advanced, composed technology), squeezes 15,000 components on the 35,000-square-mil 'AS888 chip (Fig. 1). With the oxide-isolated Impact process, the combination of 2-micrometer geometries, 1.2-nanosecond gate switching, and 50-microwatt-per-gate power drain results in chips with a higher level of integration than older bipolar technology would allow. Nevertheless, these dense chips perform at significantly reduced power levels (typically 800 milliwatts), greatly benefiting packaging and reliability.

In the 'AS888, the increased complexity possible with this dense process allows implementation of a highly comprehensive instruction set. The instruction set includes several features that facilitate the development of systems such as signal and image processors, high-speed mechanical controllers, and high-speed wide-word-width data processors.

Besides the power of the instruction set, the 'AS888

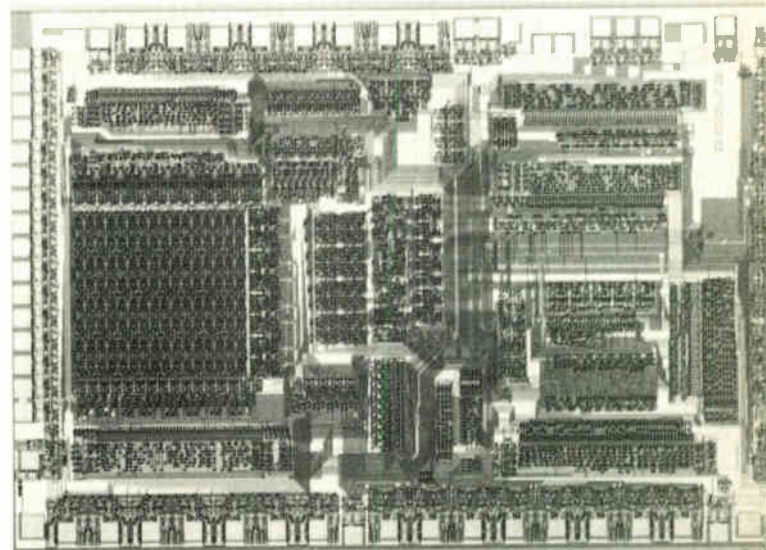
bit-slice expandable logic offers designers a flexible approach to high performance (see “What is a bit-slice?,” p. 134). Bit-slice applications range from system clocking speeds above 5 megahertz—where MOS microprocessors, already limited in word width, become unfeasible—to the very high-speed 20-MHz realm, which has typically been associated with emitter-coupled logic. The high degree of parallelism afforded by the 'AS888's architecture is a primary reason for the improved system performance it offers. Its multiple data paths support the necessary shuffling of large quantities of data, which can enter the machine serially, byte-parallel, or as full words.

Multiple buses

The 'AS888 includes a three-port (or three-operand) 8-bit-wide 16-word register file, an 8-bit arithmetic and logic unit (ALU), various shifters and multiplexers, and a status decoder (Fig. 2). Three data buses, designated DA, DB, and Y, enable parallel data to be entered and stored or retrieved from the 'AS888. One of the ALU's operands is chosen from either the DA bus or a register-file location, and the other from either the DB bus or another register-file location. Since they are separate buses controlled by microcode, the DA and DB buses can transfer data from the register file simultaneously without the need for arbitration.

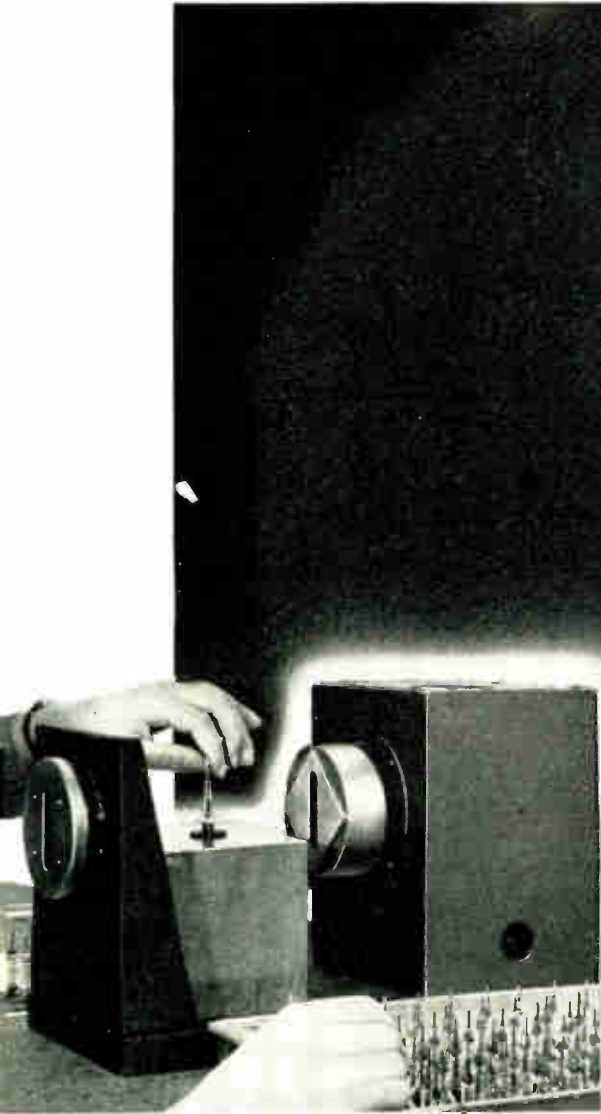
Serial data can enter and leave the 'AS888 through the ALU shifter's least-significant-bit port, SIO₀. When working in a system that uses multiple 888s for word widths larger than 8 bits, the packages are tied together through SIO₀ and SIO₇, and through QIO₀ and QIO₇. Other internal registers are involved in manipulating words that are wider than 8 bits.

For example, when double-precision shifting is re-

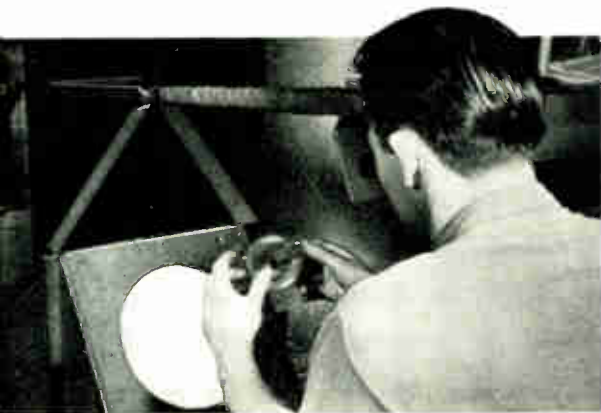


1. Bit slice. An advanced Schottky process puts 15,000 components into 35,000 square mils in this SN74AS888 8-bit-wide bit-slice processor. The 16-word-by-8-bit register file appears on the far left. To its immediate right is the 8-bit arithmetic and logic unit.

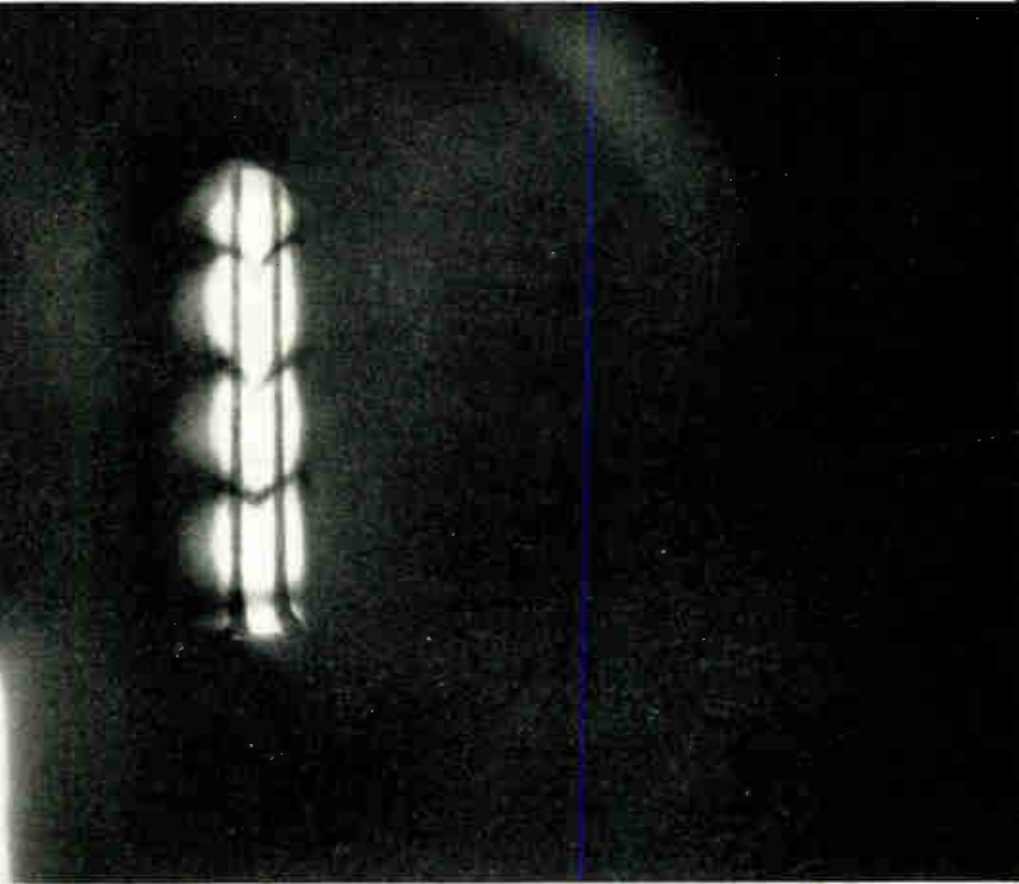
DEATH *before* DISHONOR!



Observation of the stress points on glass bead seals around vacuum tube leads is made with this device. Close-up photo above shows the actual view of a faulty lead. Note the change in polarized light creating distorted shadows which show up stress and strain in beads. Such strain sometimes occurs where metal and glass are sealed together.



Inspecting the entire glass bulb with the help of a polarized light. This device shows up stress and strain on the glass which might be created during the shaping operations.



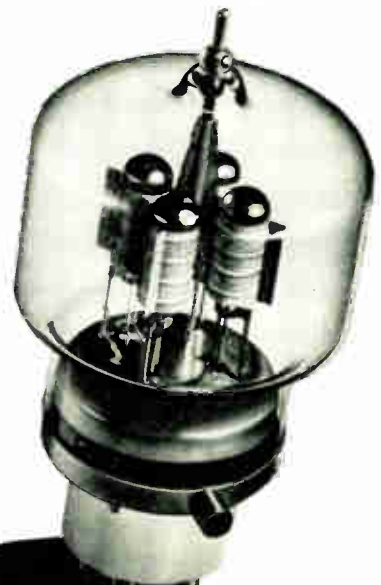
Casual observation of a vacuum tube does not reveal its flaws. That's why Eimac engineers have developed many devices for the purpose of exposing even slight weaknesses in construction. The above is not a dungeon window, but a close-up photo of a faulty bead on a filament stem as viewed through a special bead testing device. Needless to say, this stem will never reach final assembly . . . better "death before dishonor" to the Eimac tradition of dependability.

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What is a bit slice?

Classically defined, a bit slice is a universal building block—a large-scale integrated circuit—that can be cascaded to perform a processing function of any word length. Since bit slices can be used to develop the processing section for any application, it is impossible to encompass all aspects of a bit-slice in a single paragraph.

Nevertheless, a bit slice generally includes certain basic structures. These include an arithmetic and logic unit, some shifters, registers for temporary data storage, and multiplexers for selecting the paths for data flow to and from the individual bit-slice element.

With the bit-slice approach, designers can follow the trend of expanding the data word length to obtain greater computer accuracy even though the general-purpose microprocessor has probably reached a practical limit. The stumbling block is not that microprocessors are incapable of handling longer words; rather, semiconductor manufacturers are constrained by another set of limitations—those of modern packaging techniques.

The bit-slice approach gives designers an alternative solution to this problem. Here, the essential functions of the processing segment are placed together on a single chip of short word length. Nevertheless, the chip is designed for ease of expansion—allowing its user to create a machine of the desired width. From this concept of a processor vertically divided into building blocks that are equal in size and

functionally equivalent comes the name bit slice.

Going hand in hand with bit-slice designs is the subject of microprogramming. The concept of microprogramming is basically easy to understand, but its efficient implementation is a "black art" in which very few designers can claim expertise. The instructions, or microinstructions, that make up the controlling microprogram reduce the need for sequential hardware logic in a digital system. These microinstructions are stored in a read-only memory—possibly user-programmable—called the control store.

Each microinstruction supplies a parallel combination of logical 1s and 0s in order to control the basic logic devices of the system. Operating independently of the data flow, the microprogram sequence performs a function that is separate from that of the main application program, although a relationship does exist between them since the application program will "call" microprogram sequences.

To increase its throughput capability, a bit-slice machine includes special registers, called pipeline registers, that allow the processor to anticipate and access the next sequential control word. This so-called pipelining process shaves a significant amount of time from the system cycle time by performing memory-access simultaneously with processing functions. As long as the regular procedure of the microprogram is not interrupted, this pipeline design is a highly efficient method of operating the machine.

quired, the ALU shifter is combined with the memory quotient (MQ) shifter. This MQ shifter serves the MQ register, which is used for storage of the partial products generated by multiplication and divide routines, and the double-precision shift functions. MQ register contents can then be routed either back to the ALU (if the operation needs to be repeated) or on to the register file (a set of registers used as a temporary data-storage location).

This high degree of flexibility in moving data is further reflected in the sources of data available to the ALU. Separate multiplexers at the two inputs to the ALU select

the point of origin of the next data word to the ALU. Data may pass to the ALU from either the register file or from the DA or DB bus lines or may even be routed around the ALU. This unique feature of the 'AS888 allows the chip to handle multiplication and division at the same clock rate as addition and subtraction, eliminating the need for manipulating clock pulse widths in order to optimize throughput.

Because even the chip's very sophisticated instructions can be executed in one clock cycle, the user never will have to "stretch" clock cycles, say, for a multiplication,

Unpacking a floating-point number

In the IEEE floating-point format, a single-precision number consists of 32 bits—a sign bit, 8 exponent bits, and 23 mantissa bits, in that order—a format that may present problems to other bit-slice processors. However, with the power of the 'AS888 instruction set, designers need just a few instructions to unpack such a number.

Assuming that the number resides in some section R_0 of the register file (and for simplicity ignoring the problem of generating R_0 's address), unpacking the number requires the following operations. The first instruction shifts the number from R_0 circularly one position to the left (using the SLC instruction) and stores it in section R_1 . This circular left shift packs the most significant bit of the original number into the least-significant-bit position.

Consequently, R_1 contains a re-ordered version of the

original, so that the exponent is first, followed by the significand, with the original sign bit occupying the least-significant-bit position. The second instruction extracts the exponent (most significant byte) by enabling the three least-significant bytes designated 0, 1, and 2, as an operand (using the byte-select utility). These three bytes are then eliminated with a subtraction (using the byte-subtract instructions—BSUBR and BSUBS). The resulting exponent is placed in section R_2 as part of the same instruction.

A circular shift to the right (using the SRC instruction) and an exclusive-OR operation between R_1 and R_2 (using the byte exclusive-OR instruction—BXOR) then extracts the sign bit and the significand, and realigns them as required. The final instruction (using the set-bit instruction—SET1) sets the implicit, or hidden, bit to a 1.

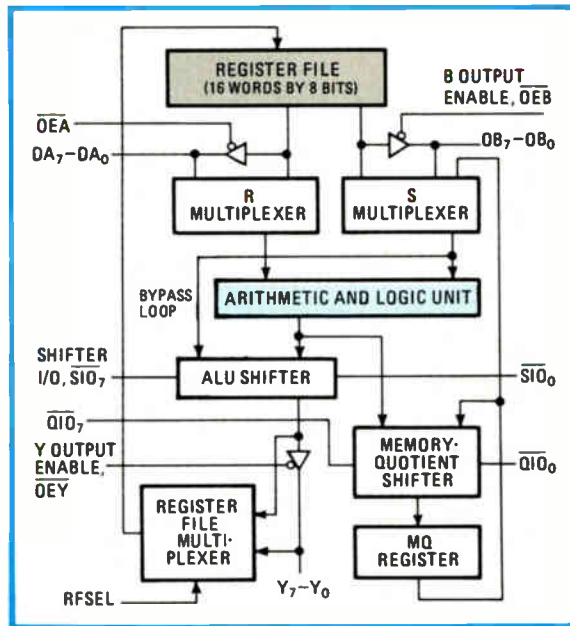
or reduce the clock frequency to accommodate some slow instruction. For example, the SELECT S/R instruction, which can select the larger or smaller of the ALU's two operands (S or R) depending on the result of a previous subtraction, is the heart of a very important operation of sorting according to magnitude. With the less sophisticated instruction sets of most comparable processors, such a selecting operation would require many steps.

Powerful instructions

Once data has entered the 'AS888, it can be processed in a variety of packet sizes. Individual bits within a byte can be checked or set with TEST BIT OR, TEST BIT AND, SET BIT, or RESET BIT instructions. Individual bytes can be added together, subtracted, OR-ed, AND-ed, and exclusive-OR-ed. In the ALU, full-word operands can undergo 14 standard arithmetic and 8 logic functions, including signed and unsigned multiplication and division and a polynomial division.

With its extensive set of shift instructions, the 'AS888 is particularly adept at handling long words resulting from multiplication, division, and floating-point operations. Even in complex shifting operations, the chip maintains high performance, since logical, arithmetic, and circular shifts are all performed within the same clock cycle as an arithmetic or logical operation. Particularly useful in applications like signal processing or array processing—where overflow detection is critical—conditional shift instructions dependent on external data can be conveniently implemented.

One application is in block floating-point arithmetic in FFT calculations (see "Application to the fast Fourier transform," p. 136). Here, the numbers are all converted into fractions with magnitudes lying between 0 and 1/2. Each successive pass through the array is kept within these bounds by a scaling operation that ensures that no



2. Multiple data paths. Once in the 'AS888 bit-slice processor, data can be moved through the chip in various ways. Data can enter the ALU through the R and S multiplexers or even bypass it. For extending word lengths by cascading 'AS888 chips, separate ports address the ALU and MQ shifters.

computation is done. Of course, the instruction set supports arithmetic operations, storing data in binary or binary-coded decimal form.

Usually a nightmare for the microprogrammer, the task of maintaining the integrity of ALU and shift-operation results is easily handled by the 'AS888. For example, the status of a combined ALU and shifting operation is indicated by an overflow signal when either operation produces an invalid 2's complement result. A 0 is detected at the output of the shifter, and the carry output of the ALU and its sign are provided. Further supporting arithmetic operations, the chip flags an overflow signal when the result of a division operation cannot fit into the word length of the machine or when an attempt is made to divide by zero. □

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PART 2

Sequencer handles microcode interrupts

by Jeff Niehaus, Jim Duval, and Bill Kronlage
Texas Instruments Inc., Dallas, Texas

□ Although raw computing speed is impressive, the real measure of computing power—the timely execution of

programs—depends on the responsiveness of the system. Just as a high-performance sports car is useless without a steering mechanism that can respond quickly to the driver's commands, a high-speed processor must be able to respond rapidly to a variety of computing tasks and external interrupts. Steering the high-performance SN74AS888 bit-slice processor (see accompanying article on p. 133), the SN74AS890 microsequencer will provide microaddress sequences and can redirect the 'AS888 to switch tasks when necessary. Thus the 'AS890 will work in close cooperation with the 'AS888 bit-slice processor

overflow can occur.

Other instructions in the chip's extensive instruction set further make the processor especially well suited for floating-point arithmetic (see "Unpacking a floating-point number," p. 134). Instructions that manipulate individual bytes of data provide an efficient vehicle for operating separately upon the mantissa and exponent of floating-point numbers. This utility is particularly useful for evaluating the components of floating-point numbers as established by the Institute of Electrical and Electronics Engineers.

These boundaries define "special cases" in the IEEE format specification. These special cases include positive or negative infinity, 0, and a NaN (not a number) and must be identified as such before any arithmetic computation is done.

to implement high-performance circuits such as the fast Fourier transform (see "Application to the fast Fourier transform," below).

Implemented with TI's advanced-Schottky (AS) and Schottky-transistor logic (STL), the 'AS890 contains approximately 2,400 Schottky gate equivalents and typically consumes just 800 milliwatts (Fig. 1). All internal STL logic in these devices operates from a 2-volt power supply, but the internal logic communicates with the rest of the system through 5-v advanced-Schottky TTL-compatible input/output ports.

Besides this 64-pin side-brazed dual-in-line-packaged version, the part is available in a 68-pin chip-carrier, designated 'AS891. The 68-pin carrier features an extra 4-bit port that appends four user-definable bits to the two 14-bit data ports, DRA or DRB, to create address values for support of 16-way branches.

The 890—the most powerful microsequencer available—provides sequencing of microaddresses to a bit-slice like the 'AS888. The 890's typical address-genera-

tion time—26 nanoseconds—is maintained regardless of whether a simple straight-line code algorithm is being executed or one of the other 64 powerful instructions—which may involve external branch flags, counter decrements, and stack operations—are being performed.

The 'AS890 architecture allows 16,384 microaddresses to be addressed directly. Nine tasks may be awaiting completion at any given time and may remain queued in the nine-deep, first-in, last-out (FILO) stack. These tasks may consist of a combination of expected subroutines and random interrupts. If the system commands the 'AS890 to operate simultaneously on more than nine tasks, an error flag becomes active and the system is then allowed to dump the pending tasks for diagnostic purposes without destroying their place in the queue.

Microcoding easy to understand

The concept of microprogramming is basically easy to understand, but its efficient implementation is an art that requires intimate knowledge of the system's hardware.

Application to the fast Fourier transform

Because of its speed and special operational features, the SN74'AS890 microsequencer is particularly applicable for performing fast Fourier transforms. In particular, the so-called FFT kernel, or butterfly—upon which the entire FFT procedure is built—can be implemented with an 890 and several bit-slice units like the 888. The butterfly is so dubbed

because of its appearance (see tinted parts of upper figure).

The FFT generates transforms by implementing the equation:

$$X(k) = \sum_{n=0}^{n=N-1} x(n) e^{-j\omega n k / N}$$

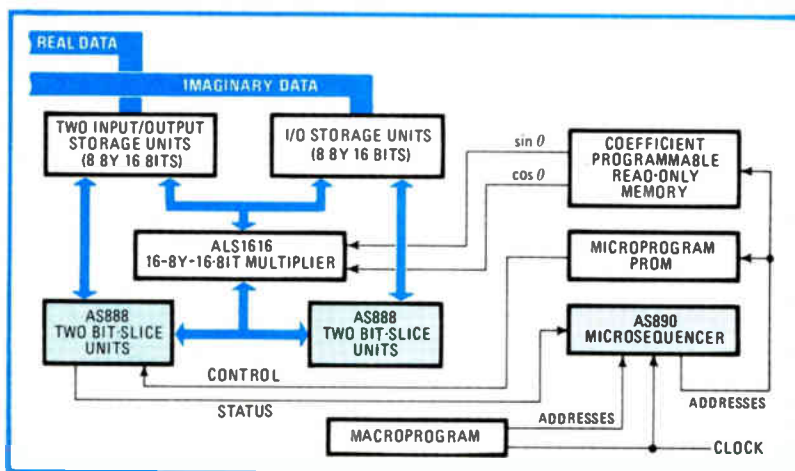
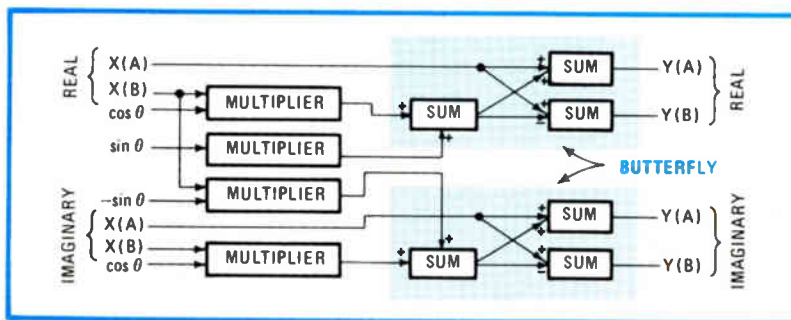
where $k = 0, 1, 2, 3, \dots (N-1)$ and $X(k)$ is the discrete

Fourier transform of the sampled signal $x(n)$. The FFT reduces the number of operations required to implement this equation by removing those that are redundant. Thus it succeeds in reducing them to $(N/2)\log_2 N$ from the N^2 that is implied by the equation as it stands.

The 890, when used to perform FFTs in the system shown in the lower figure takes the macrocode program and generates entry points; in an FFT subroutine, the 890 generates addresses that control:

- Instructions to the 888 ALUs and the ALS1616 multiplier.
- Addresses for the lookup table for sine and cosine information.
- Addresses for the register file for input/output operation— $x(n)$ in, $X(k)$ out.
- All addresses in the register files and 888s for temporary storage of intermediate butterfly results.

The advantage of the 890 in this application is its raw speed—it is two to four times faster than ordinary microsequencers. The implication of such speed at the system level is that higher-frequency signals will be capable of being processed.



Storing the microinstructions, which comprise the microprogram, in a memory—usually a programmable read-only memory—reduces the need for sequential hardware logic in a digital system. Each microinstruction supplies in parallel a combination of 1s and 0s to control the logic devices of the system. Operating independently of the data flow, the microprogram sequence performs a function separate from the main source program, although a relationship does exist.

Each main program instruction is decoded to address a microinstruction or set of microinstructions that resides in the control storage memory, hidden from the programmer's view. Each microinstruction can be separated into several smaller instructions, called micro-orders, that direct several events to take place simultaneously; they may, for instance, instruct shifters to shift data while multiplexers select registers for loading or releasing data in parallel.

Microcode selection

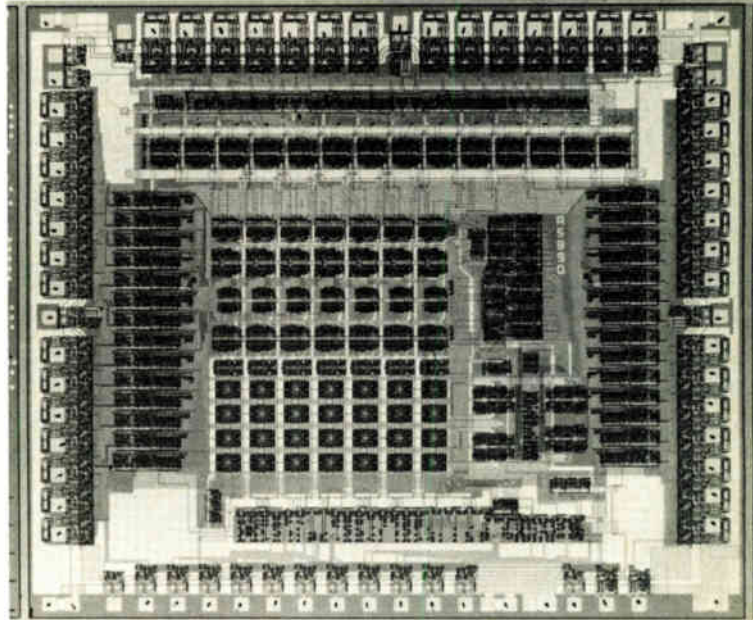
In operation, the 'AS890 takes the current microinstruction, its address, the condition of its counters, and the condition-control input—a signal that represents the 'AS888 status—and decides where the next microword is stored and whether any subroutine linkage needs to be updated. The microword, in turn, controls the 888 and allows the 890 to decide where the next microword is stored. This basic process continues until the program is completed. (One common method of speeding this process is to store the address generated by the 890 in a pipeline register before it is sent to the control-store memory. This technique is similar to an instruction pre-fetch in a mainframe computer.)

The control block includes an instruction decoder and provides ports for the status information from the bit slice to the 890 (Fig. 2). The 890 uses the condition code (CC), the stack-instruction ports (S_0 to S_2), the multiplexer (MUX_0 to MUX_2) inputs, and an internal status flag to select the next microcode address either from an internal location or from some external source. The 890 processes one microinstruction per clock cycle, then decodes the condition, or status, of the system at the completion of the microinstruction to select the address of the next microinstruction or to support a subroutine or interrupt. The sequencer uses a special condition code (CC) input to effect conditional branches and jumps.

Eight address sources

A 14-bit microaddress can be selected from one of eight sources to provide the proper microinstruction sequence for a bit-slice processor or other microcode-based systems. Two 14-bit data ports, DRA and DRB, enable 14-bit address or data words to enter the 890. In addition, the Y-output multiplexer can select the next branch address from one of six other sources:

- The top of the 14-bit-by-9-word address stack.
- Internal register/counter A.
- Internal register/counter B.
- An internal microprogram counter (MPC register).
- A 16-way branch—4 bits (B_0 to B_3), which are appended to the DRA, DRB, A counter/register, or B register/counter (on the 'AS891 only).



1. Microsequencer. Using TI's advanced Schottky process, this SN74AS890 microsequencer dissipates typically just 800 mW while generating addresses in about 26 ns. The 9-word-by-14-bit first-in, last-out stack (the array in the chip center) lets it queue nine tasks.

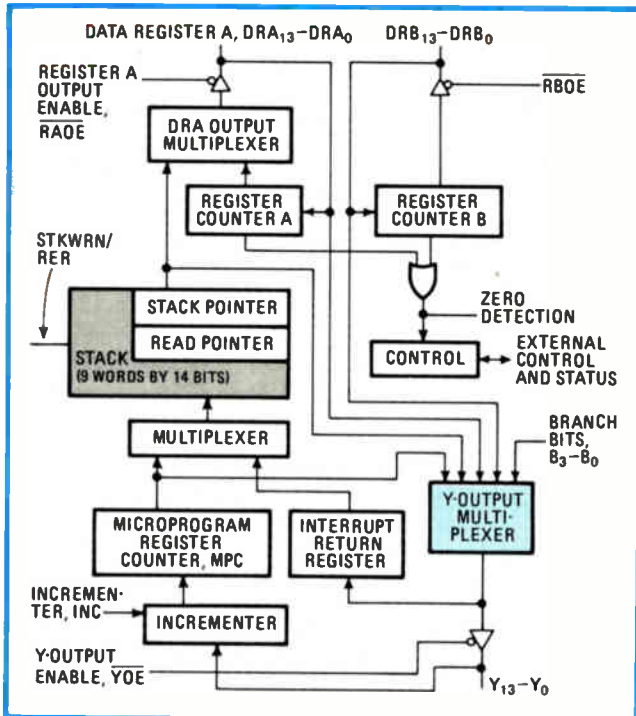
This multiway branching capability, coupled with a 14-bit-by-9-word-deep FILO stack consisting of 14 registers, allows the programmer to arrange the code in blocks so that microprograms may be structured in the same fashion as such high-level languages as Algol, Pascal, or Ada. The FILO's on-board storage of nine control-store addresses is capable of supporting altogether nine nested levels of microsubroutine, looping, and real-time interrupt functions.

For instance, a subroutine might be invoked to perform an often repeated task, after which the system returns to the main program. To do this, the system must preserve the location of where the main program left off when the subroutine was called. The 890 makes use of the stack so as to perform this function in the following manner.

In the event of an interrupt, the 890's Y-bus output drivers are rendered inoperative by being put into their high-impedance state. This allows the address of the first microinstruction of the subroutine to be directed onto the bidirectional Y bus from an external source and into the microprogram register (MPC).

At the same time, the address of the last instruction before the interrupt subroutine was called is preserved in the interrupt-return register (INT RT). The (INT RT) register constantly monitors the contents of the Y bus and is updated on every clock cycle.

As this return address is stored in the INT RT register, the address of the second microword of the subroutine is generated for loading into the MPC register. Then the processor, acting on the first microinstruction, pushes the INT RT register contents onto the stack, preserving the return linkage. Thereafter, beginning with the second microword, the rest of the interrupt subroutine is processed until the subroutine is complete. At this



2. Well-controlled. With its multiple inputs, the Y-output multiplexer is a flexible means of selecting the next microaddress. Debugging becomes easier using the STKWRN/RER signal, which warns when a program tries to overfill the stack or to draw data from an empty stack.

point, the return address “pops” (in other words, leaves) the stack and the main program resumes.

Obtaining an address (or other data) from the top of the stack requires a so-called POP instruction. As the data leaves the stack, the stack pointer (SP) decrements by one. With a PUSH operation, an address stored in the microprogram register (MPC) loads into the stack location addressed by the stack pointer, and the stack pointer increments one step.

The two next address sources available—the loadable register-counters RA and RB—not only operate as 14-bit counters to control looping operations, but also can be used for the temporary storage of microaddresses, loaded directly from the DRA and DRB ports, respectively. Iterative routines can be generated by loading RA and RB and operating them as down counters. The ZERO output going high indicates that a register contains a binary 1 and a decrement is on the point of taking place, which would signal the end of a looping operation. Because of the existence of this facility, a “decrement and branch-on-loop” termination can be executed in the same clock cycle.

Another register-counter associated with addressing—the microprogram register (MPC) and its associated incrementer (INC)—can generate the next microprogram address for sequential-addressing operations. The MPC may be loaded via the Y bus with either an internal or external address for processing subroutine and interrupt operations. This value may be incremented prior to storage in the MPC for sequential addressing of subroutines or interrupt routines.

Also, the 4-bit B_0 -to- B_3 port handles a 4-bit address

(in the 891 version), which supports 16-way branching operations—almost all the types covered by any other processor.

For those applications where polling would impede system throughput, the system supports real-time vectored interrupt routines as well as polled interrupt handling. Any instruction, including PUSHes and POPs, may be interrupted.

Interrupts and polling

To process an interrupt, a two-step procedure should be followed. First, the bidirectional Y bus is placed into a high-impedance state (with YOE high). Second, the interrupt-entry-point vector is entered on the Y bus and incremented by 1 (with an INC high), so that it becomes the second microinstruction of the interrupt routine.

At the following clock edge, this second microaddress is stored in the MPC, and the interrupt address is stored in the INT RT register (which always contains a value that is going out on the Y bus). Also, the processor begins execution of the first instruction of the interrupt routine, which must PUSH the address stored in the INT RT register onto the stack (with INT low) to keep the proper return linkage. The proper return linkage is preserved even when an interrupt is itself interrupted, by merely repeating the above sequence.

Diagnostic support

With the trend toward the use of more sophisticated software and the reduction in hardware-development time afforded by large-scale integrated circuits, software debugging occupies a larger share of the system design cycle. As the microcode used in an application becomes more complex through the use of more subroutines and interrupt handlers, the chance of a nonrecoverable stack overflow becomes greater. Without the capability to back-trace through a program to find, for example, an offending subroutine, software debugging is very difficult.

A key support function of the 890 is the provision of a read pointer to the address stack, which simplifies microcode diagnostics to speed software debugging and reduce system design time. With this pointer, stack contents can be nondestructively read, thereby enabling a microprogrammer to retrace the footprints of a system during debugging procedures. During normal operation, the read pointer contains the same value as the stack pointer and is transparent to the user.

Another diagnostic help allows detection of potential underflows and overflows by using the address stack's STKWRN/RER output. If seven of the nine stack locations are full and a PUSH operation occurs, the STKWRN/RER pin will produce a high-level signal to warn that the stack is approaching its capacity, and will be full after one more PUSH. Knowledge that overflow potential exists allows bit-slice-based systems continuously to process real-time interrupt vectors. This signal remains high, until the stack pointer is decremented below 7.

Similarly, the STKWRN/RER can provide protection against POPping an empty stack. A high level signifies that the last data entry has been removed from the stack. This condition remains until an address is pushed onto the stack and the stack pointer is incremented. □

Dual timer supplies high-voltage ramp

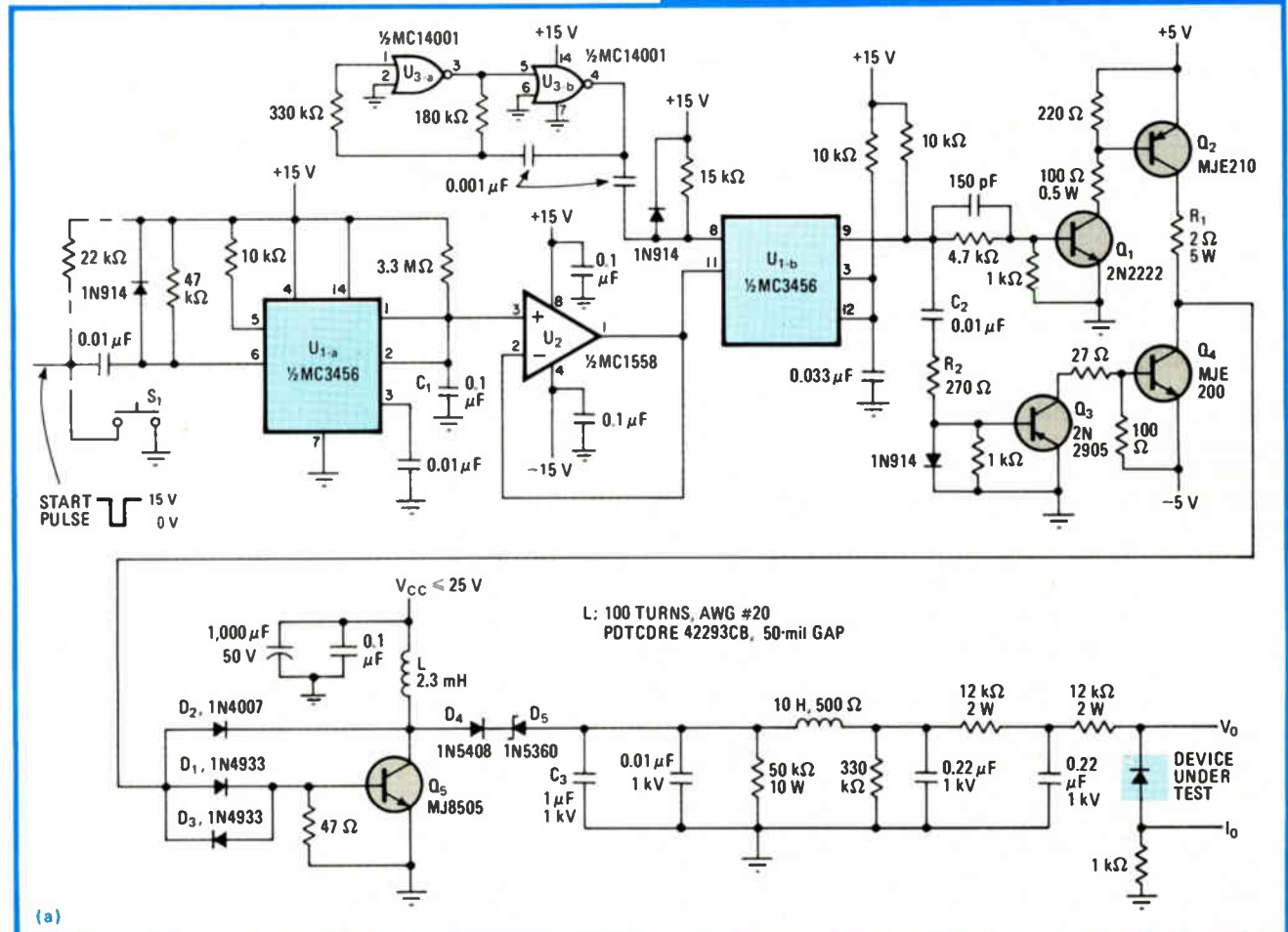
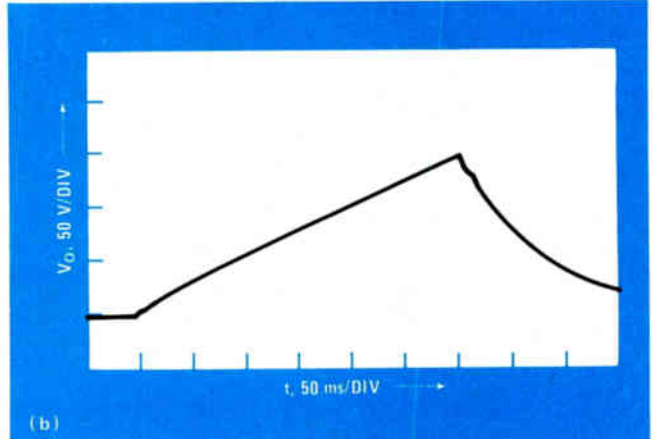
by Al Pshaenich
Motorola Semiconductor Products Sector, Phoenix, Ariz.

Although switching-mode power supplies using closed-loop, pulse-width-modulated flyback converters are quite common, this circuit is unique in providing the high-voltage-ramp power supply often required to automatically test semiconductor devices in the avalanche mode.

High-voltage ramp. Connected as a pulse-width modulator (a), timer U_{1-b} generates a ramp-controlled 1.7-kHz PWM waveform, which is fed to a power amplifier comprising transistor stages Q_1 through Q_4 . Forward and reverse bias currents generated by these transistors further control the switching action of Q_5 , whose output is fed to C_3 to produce the desired high-voltage ramp. The output filter reduces the 1.7-kHz ripple on the output ramp. A typical unloaded output ramp, generated with a V_{cc} of 7 V, is shown in (b).

For about 350 milliseconds, monostable multivibrator U_{1-a} generates a low-voltage ramp, which is fed to timer U_{1-b} , configured as a pulse-width modulator, via buffer U_2 . A 1.7-kilohertz clock consisting of NOR gates U_{3-a} and U_{3-b} provides the timer's control input. The system start can be single-pulsed by S_1 or externally clocked by a negative-going start pulse (Fig. 1a).

The PWM signal is then fed to the power amplifier,



which consists of cascaded-transistor stages Q_1 and Q_2 , for generating forward bias current I_{b1} , and transistors Q_3 and Q_4 , for generating reverse bias current I_{b2} . I_{b1} is set to 1.5 amperes, while I_{b2} is provided by the negative-going differentiated pulse formed by network R_2C_2 . The baker clamp and speed-up diodes D_1 through D_3 minimize switching-mode power transistor Q_3 's storage time, thereby permitting the flyback converter to be operated on a high-duty cycle.

Flyback voltages as high as 700 volts, derived from peak collector currents of about 4 A, are easy to reach. This energy is then fed to output capacitor C_3 via clamp diode D_4 to produce the desired high-voltage output ramp. An output filter precedes the device under test and minimizes the 1.7-kHz ripple on the output ramp. The oscilloscope photograph (Fig. 1b) shows a typical unloaded voltage ramp, generated with a power supply of 7 V dc. □

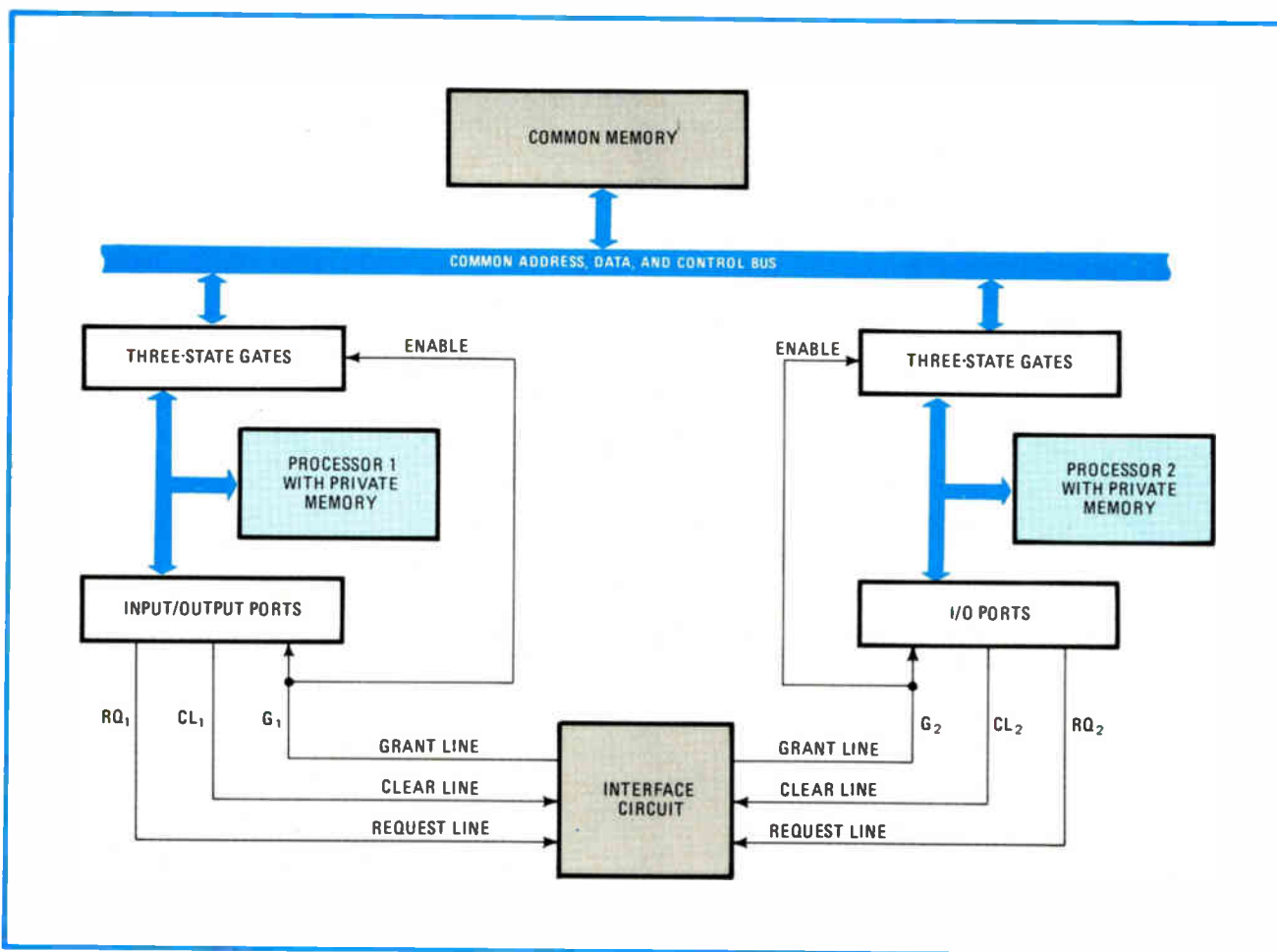
Interface links 8-bit chips to provide multiprocessing

by D. Sundararajan, M. O. Ahmad, and S. Ganesan
Concordia University, Montreal, Quebec, Canada

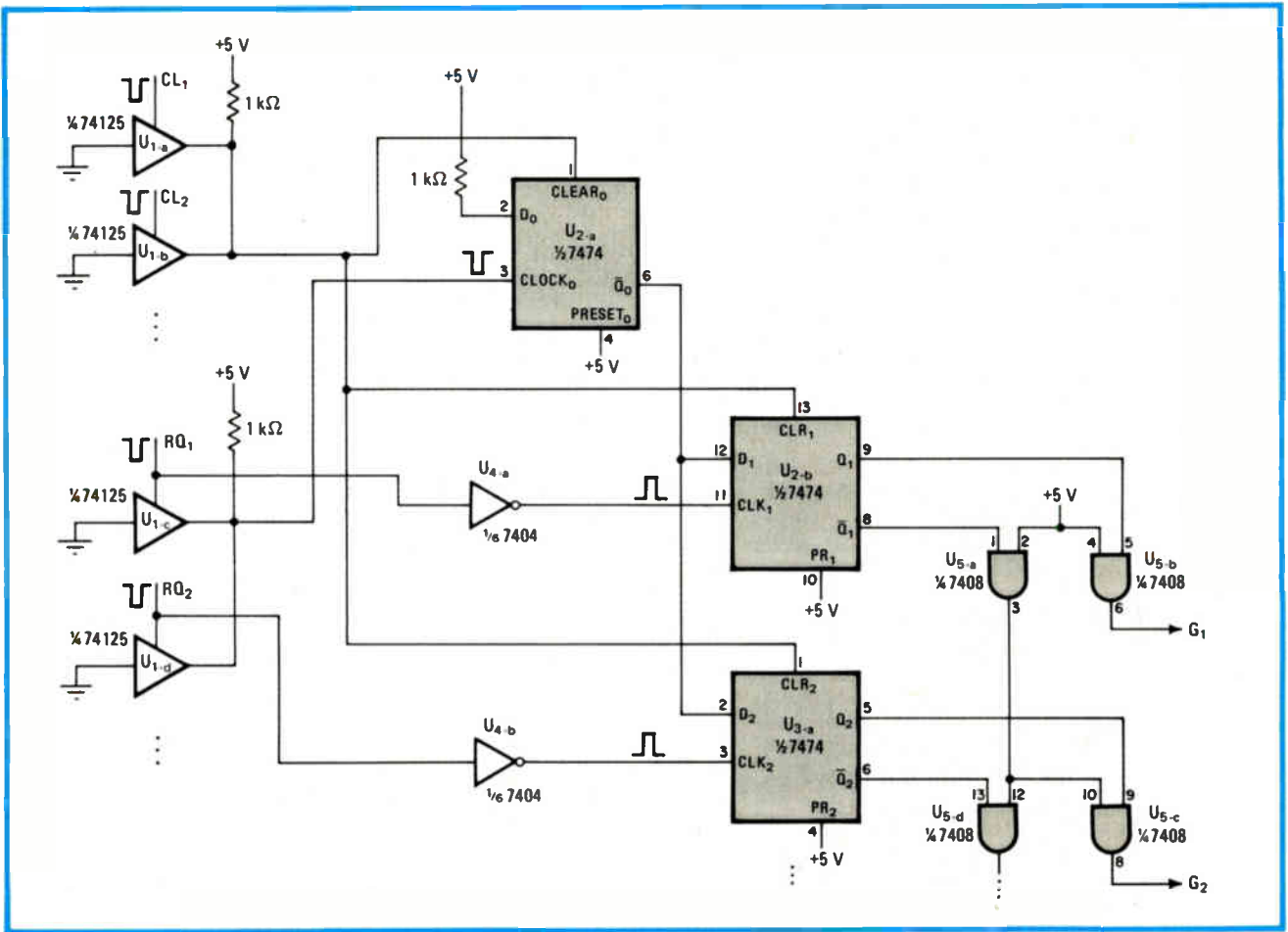
With the proliferation of low-cost microprocessors, multiprocessing has become attractive for many applications. The popular 8-bit microprocessors, however, do not have

such features built in and therefore must be linked by an external circuit. This interface, which allows multiple microprocessors to share a common memory, uses a circuit that basically comprises a flip-flop flag to indicate the availability of the common resource—the semaphore—and the serial priority-assignment section. Though the design illustrated uses two microprocessors, it can be expanded easily to interface several processors with common memory.

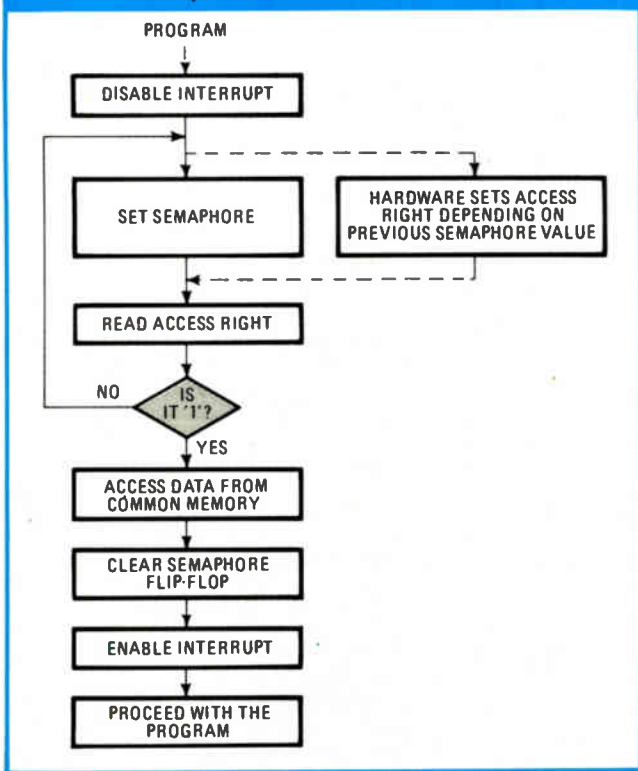
The fundamental scheme (below) shows two processors connected to a common memory, accomplished by the interface circuit shown on the page opposite. When the



Multiprocessing. The basic scheme (above) illustrates a technique of connecting multiple microprocessors with a common memory. Though the illustration (top of opposite page) shows two processors, the design can be expanded easily by adding two three-state gates, one inverter, two AND gates, and one flip-flop per additional microprocessor. The flip-flops indicate the availability of the common resource, while the AND gates implement the serial daisy-chain-priority scheme, ensuring priority access to the common memory.



FLOWCHART TO ACCESS COMMON RESOURCE



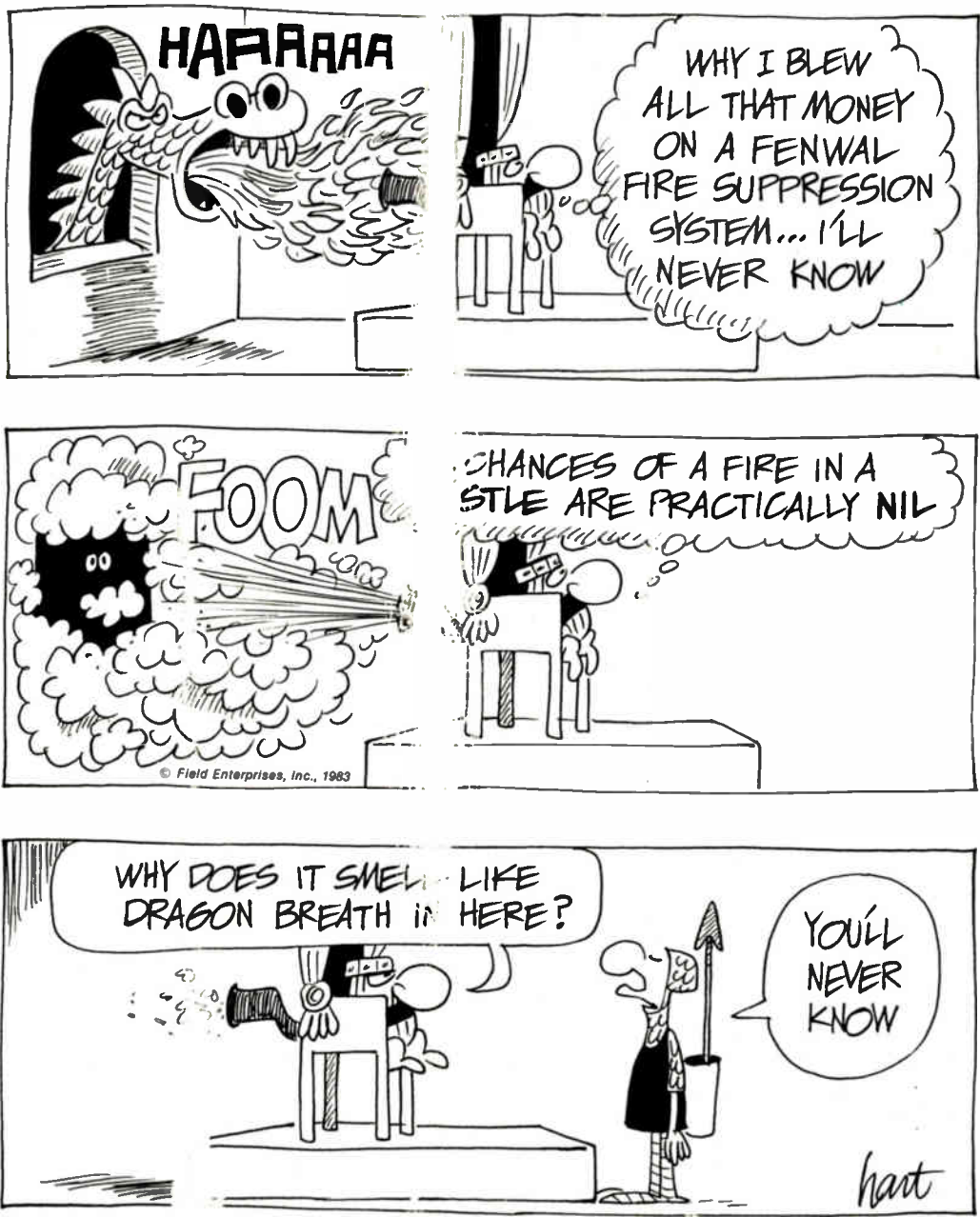
power is switched on, the input/output ports are initialized, the flip-flops are cleared, the three-state buffers are disabled, and the common memory is disconnected from the processors. Each processor executes its own program using its private memory. When a processor requires access to the common memory, however, a routine set and test (see table) is executed. In this routine, instructions produce clear and request pulses.

The request lines enable the three-state gates U_{1-c} and U_{1-d} , whose output now turns low. This high to low transition sets U_{2-b} or U_{3-a} depending on the Q output of U_{2-a} . Its low to high transition sets flip-flop U_{2-a} . The Q outputs of flip-flops U_{2-b} and U_{3-a} in turn determine the state of the two grant lines, G_1 and G_2 . Access to common memory is allowed when a processor's grant line is high; so a processor requesting access to common memory has to wait till its grant line goes high.

The AND gates U_i implement the serial daisy-chain-priority scheme and ensure that processor 1 has higher priority than processor 2. If request signals are sent simultaneously by the two processors, only processor 1 receives the grant signal although the flip-flops U_{2-a} - U_{3-a} are all set. Once a processor gets access to the common memory, the interface circuit ensures that the operation is executed without interruption. □

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Clustering VAX superminicomputers into large multiprocessor systems

Hardware and software developments integrate standard VAX-11 processors into highly available, easy-to-extend systems with distributed, shared files

by William D. Strecker, *Digital Equipment Corp., Littleton, Mass.*

□ Multicomputer systems typically fall into one of two classes: tightly coupled or loosely coupled. The computers in a tightly coupled system are physically close, the processors communicate through high-bandwidth shared primary memory, and there is one copy of the operating system. In loosely coupled systems, the computers are physically separate, the interprocessor bandwidth is lower, communications are message-oriented, and operating systems are independent.

Hardware and software engineers at Digital Equipment Corp. recently built a multicomputer system—the VAXcluster—that uses the VAX-11 line of superminicomputers. The VAXcluster's goals were high availability and ease of extension to large configurations—goals best served by a loosely coupled system. The independent operating systems increase the likelihood of survival when operating systems fail, and message-oriented inter-computer communications provide hardware redundancy and ease of expansion into large configurations.

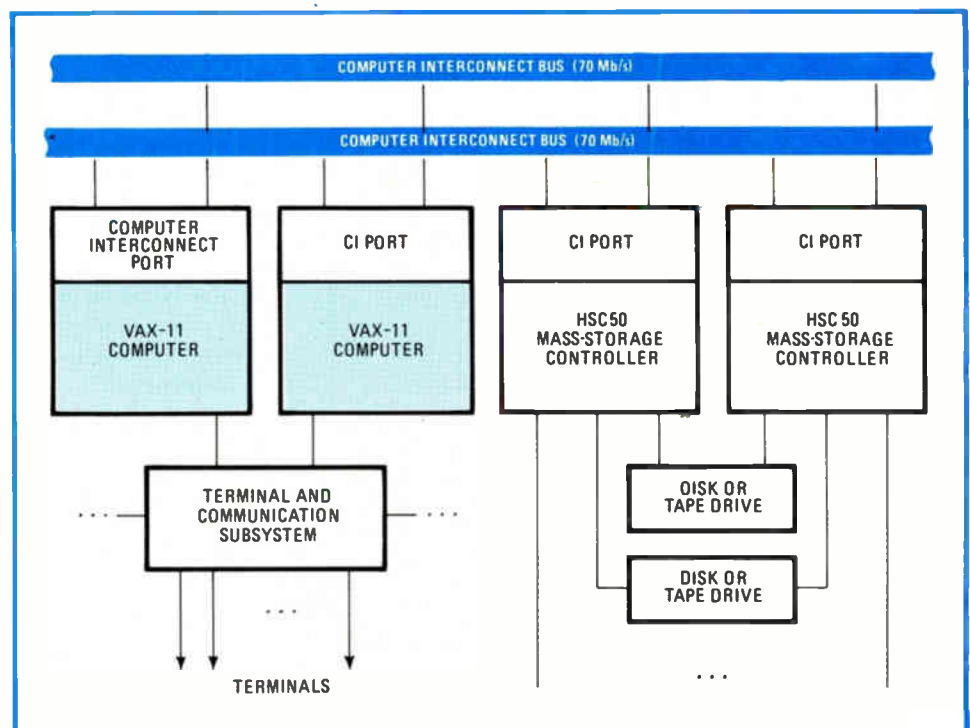
The VAXcluster's strength lies in its ability to provide this rather sophisticated structure with general-purpose computer hardware and software—not with specialized processors whose peripherals options are limited and with very specialized operating systems that have no more than limited software support. Such a structure can therefore be built with the widely used VAX/VMS operating system, which has interactive, batch, and real-time computing modes and can also support

a great many programming languages and applications.

In a loosely coupled system the speed of interconnection and the communications-software overhead limit performance. The VAXcluster's development team got performance by creating a very high-speed message-oriented computer interconnect (CI) and a simple, low-overhead system-communications architecture (SCA) and by implementing much of it in an intelligent hardware interface—the CI port—between the computers and the CI.

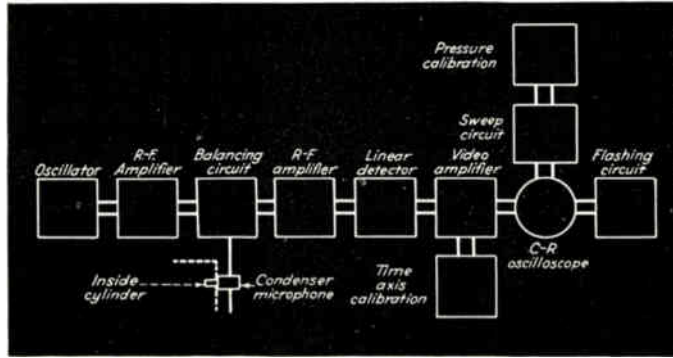
The VAXcluster's hardware structure comprises five major kinds of components: the CI, the CI port, the computer, the model HSC50 intelligent mass-storage controller, and a terminal and communications subsystem (Fig. 1). The CI is a dual-path serial bus, each path running at 70 megabits/s. Duplication of paths mainly provides backup in case of failure, but the two paths can speed up transfers when used together. Each has two coaxial cables, one for transmitting signals and one for receiving them.

The CI's central hub, the star coupler, is connected to



1. Gathering. Two 70-megabit/s computer interconnects (CIs) cluster VAX-11 superminicomputers and mass-storage systems for highly available, easily expandable systems. Replication of computers, mass-storage controllers, disks, buses, and operating systems creates fault tolerance.

Block diagram of the apparatus necessary for the measurement of cylinder pressures by the use of a condenser microphone and a cathode-ray oscilloscope



used to transform pressure into electrical impulses include carbon stacks (variable resistance), quartz crystals (piezoelectric effect), moving coils or variable reluctance (electromagnetic conversion) and condenser microphones (variable capacity). Numerous refinements have been made in connection with such systems of measurement. For example, measurement of engine pressure variations by means of a condenser microphone polarized with high d-c potential and driving a high-gain d-c amplifier has several disadvantages. Inasmuch as a condenser microphone used in this manner operates as a high impedance device the microphone circuit has a tendency to pick up and indicate undesired voltages induced from nearby ignition systems. Variation in microphone-cable-to-ground capacity due to vibration affects measurements since the high impedance cable capacity is essentially in parallel with the capacity of the microphone. Instability is frequently serious due to changes in microphone insulation and changes in the input resistance of the initial d-c amplifier tube. In the circuit shown in block form the difficulties outlined above are resolved by energizing the microphone with high frequency voltage of the order of several Mc, employing it to modulate an r-f amplifier rather than to operate a d-c amplifier. A linear detector removes the r-f component of the modulated signal and delivers voltages comparable to the output of the microphone to the video amplifier of the associated cathode-ray oscilloscope.—Robertson, *Review of Scientific Instruments*, June, 1940, p. 142; Penther and Pompeo, *ELECTRONICS*, May, 1941, p. 43.

Temperature Control

ONE JUNCTION OF A thermocouple is placed within the chamber whose

temperature is to be controlled and the other junction at some reference point. A milliammeter is connected in series with the thermocouple and a calibrating resistance. As the temperature within the chamber increases, the thermocouple current passes through the meter and deflects its pointer. A small and light metallic vane mounted on the pointer passes between two coils mounted close to the plane of pointer travel. The pointer may be free to move along the pointer path for operation at various temperature levels. The two coils, L_1 and L_2 , are part of the grid and plate circuits, respectively, of a vacuum tube oscillator. In normal operation, when the vane is not between the two coils and the temperature is below the desired value, the circuit is not oscillating because of the degenerative action of L_2 on L_1 , and the plate current has an average value of about 10 ma. This is sufficient to energize the relay M , which controls the operation of the fuel injection apparatus or the damper system of the furnace thereby permitting the

continued application of heat to the chamber.

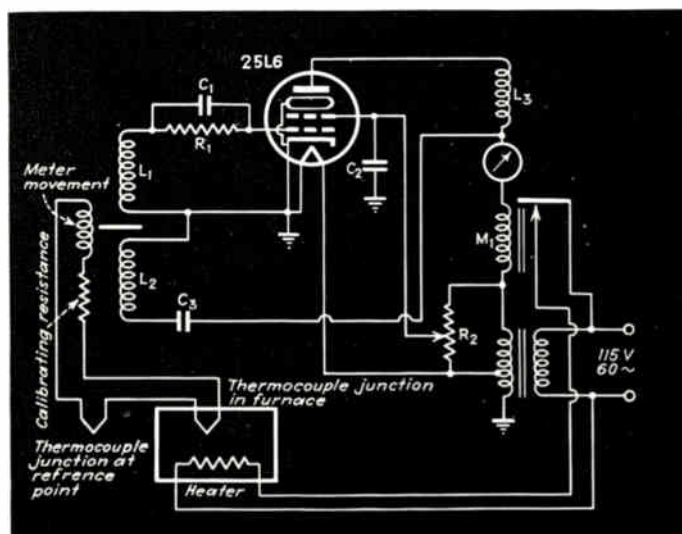
When the temperature rises to the desired value, the vane passes between the two coils and acts as a shield to isolate them from each other electromagnetically and prevent the degenerative action of coil L_2 , thereby allowing the circuit to oscillate. When the circuit oscillates the control grid draws current and a voltage drop appears across the grid leak resistor R_1 and condenser C_1 . This drives the grid to a more negative potential and reduces the plate current to an average value of about 5 ma. The drop-out current of the relay M , is somewhat greater than 5 ma and it therefore opens the circuit to the fuel injection apparatus and cuts off the supply of heat.—McLaren, *ELECTRONICS*, November, 1941, p. 50.

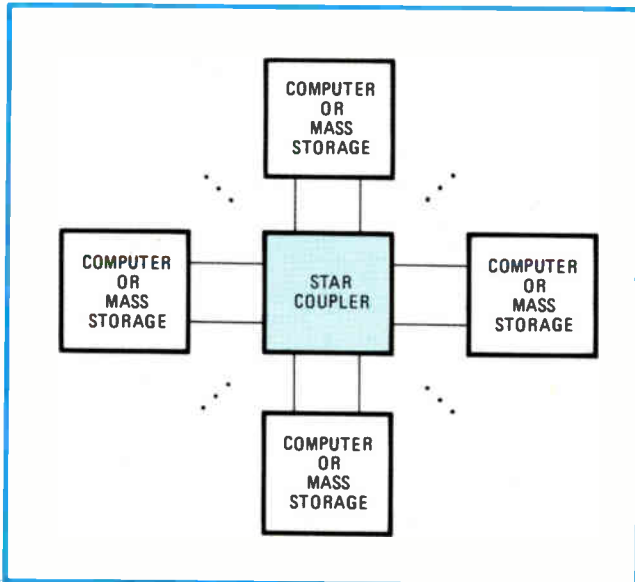
Mechanical Conveyor Synchronizer

WHERE A CONVEYOR belt travels over independently driven wheels or sprockets the straightening or sag in the belt which occurs between units when motors get out of step may be used as a source of power to force them back into synchronization.

A roller rides the conveyor belt between driving units and is mechanically linked to the movable core of a reactor. Up or down movement of the roller varies the inductance of the reactor and this variation in inductance controls the firing of thy-

Circuit diagram of the thermocouple and meter movement temperature controller. Although a type 25L6 tube is used here, other similar tubes may be used. Note that a-c power is used



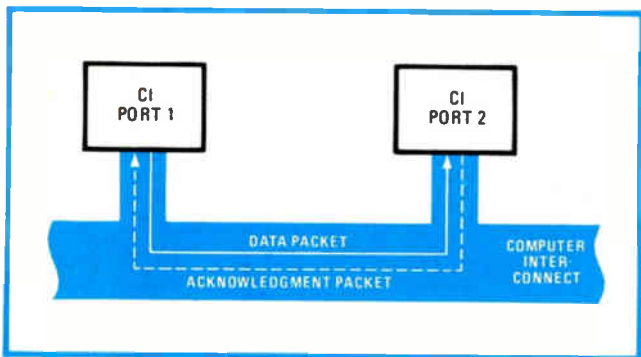


2. Twinkle, twinkle. The VAXcluster's physical topology is a star with a passive central coupler. Additional points can be added as needed, without disrupting the cluster. Each radial path can be up to 45 meters long. The interconnecting links are coaxial cables.

each computer through radial paths of as long as 45 meters (Fig. 2). This star coupler—a passive device made from transformers and resistors—supports 16 nodes: either computers or mass-storage controllers.

The VAXcluster's designers choose the star in preference to a linear topology for three reasons. First, the arbitration efficiency of a serial bus is related to the transit time between the most widely separated nodes, and the star shortens the distance between nodes. Since they can be anywhere within a 45-m radius, the maximum node separation is 90 m. A linear bus threaded through 16 nodes in the same area would generally be much longer.

Then, too, the star's central coupler lets nodes be added and removed with little risk of disrupting the CI, electrically or mechanically. Finally, the star topology will make it easier to enhance the CI with an active star coupler, permitting many more than 16 nodes, and possibly to replace the CI's coaxial cables by fiber-optic cables.



3. Acknowledged. Communication in the VAXcluster occurs through variable-length packets. The data packets are acknowledged immediately by the receiving computer's interconnect port and do not require re-arbitration of the CI. The round-robin arbitration scheme used after each packet is acknowledged guarantees equal access to the CI.

The CI transfers data in variable-length packets of up to 512 data bytes. After sending a packet, the sender waits for an immediate acknowledgment. A deterministic round-robin arbitration algorithm guarantees all nodes equal access to the CI.

The CI port tests all packets for errors with a 32-bit cyclical redundancy check. To ensure electrical isolation between nodes, CI interfaces are coupled through transformers. The CI has been engineered to rigid guidelines for both electromagnetic radiation and susceptibility.

Intelligent transporter

The CI port interface between the CI and a computer does much of the work of communicating between the computers and the mass-storage subsystems. At the lowest level, it arbitrates the CI. After winning the arbitration, a sending port (for example, port 1 in Fig. 3) sends a data packet and awaits acknowledgment. If the packet is received, the receiving port (port 2 in the example) immediately and without arbitration returns the acknowledgment. But if the packet is not received, the sending CI port re-arbitrates and tries the operation again, up to a specified limit.

Should both CI paths be available, the CI port statistically distributes transmissions across both, to balance the load and to verify that both paths are indeed operational. Each port maintains a path-status table with node-by-node information about the availability of paths. Consider a hypothetical path-status table for node 1. If path one is bad to node 1, and path two is bad to node 15, there is still a good path to each node. The CI port uses only the paths marked "good" in the path-status table. Should a transfer on such a path fail, the CI port marks it "bad" in the table and tries the other path. Only if both are bad can operations fail.

Besides the CI's speed and reliability, the VAXcluster's high level of performance stems from its ability to transfer data directly between virtual-memory buffers in different computers. With a single command to the CI port, a computer can read from or write to a virtual-memory buffer of any size in another of the cluster's computers (Fig. 4). The two CI ports cooperate by breaking up the transfer into data packets of at most 512 bytes, ensure that all packets are sent and received correctly, and reference the virtual-memory buffers specified in the transfer through the same page tables used by the host computer's central processing unit. In most loosely coupled systems, moving data between virtual-memory buffers involves multiple levels of software processing. The CI port performs all this in hardware.

Cooperating computers

A computer for the VAXcluster might be any member of the VAX-11 family, so long as it has a CI port—and such ports can now be added to the medium-scale VAX-11/750 and to the large-scale VAX-11/780 and VAX-11/782. As new medium- and large-scale VAX-11s become available, they too will have CI ports.

The HSC50 controller can support any combination of as many as six disk channels (each in turn supporting up to 4 disk drives) and tape channels (16 drives). The controller also gives all computers direct access to all

4. Buffer to buffer. VAXcluster's performance is improved by the ability of the VAX computers to transfer data directly between virtual-memory buffers by issuing a single command to the computer-interconnect port. The two CI ports cooperate to handle the details of the transfer.

mass-storage devices, so that a mass-storage request by one computer does not require any intervention by the others. All the mass-storage devices of an HSC50 can be dual-ported to the other HSC50 of a cooperating pair, and if one HSC50 should for some reason fail, the other will take over automatically.

The HSC50 optimizes the VAXcluster's throughput by performing seek and rotational optimization across outstanding disk operation requests. In these optimizations, disk requests are serviced in the order that produces the highest completion rate, not in the order of issue.

Me and my shadow

To prevent data from getting lost when one disk fails, the HSC50 has disk shadowing. Two disk drives can be combined in a disk-shadow set. When a computer issues a disk write operation to a drive in a shadow set, the HSC50 automatically writes to both drives, sending identical data. Should one fail, the other still operates. No data is lost.

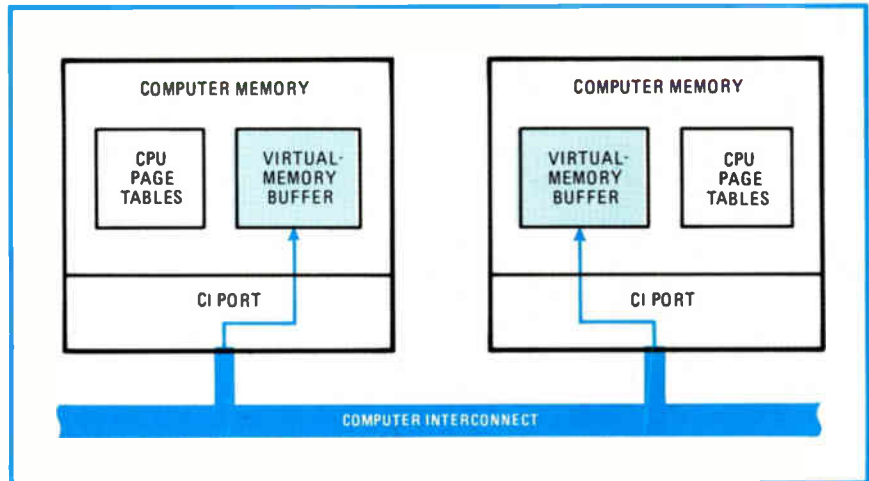
In addition, the HSC50 controller can offload the computers and present them with error-free logical disks; hide all details of disk geometry, such as sector size, track size, and number of surfaces; perform all bad-block handling, operation retry, and error correction; copy disks; and back them up to tape—all without intervention by the host computer.

The needs of terminal and other external-communications support vary a good deal. Sometimes, directly attaching terminals to the individual computers is enough. The VAXcluster's software allows any terminal to communicate transparently with any computer, though terminals attached to computers that fail are denied access to the VAXcluster.

The VAXcluster provides two alternatives to directly attached terminals. The first, a standard communications switch, can reroute terminals when a computer fails. The second connects all the computers and terminals through an Ethernet network, which gives all terminals direct access to all host computers.

Software

The VAXcluster's software structure comprises a set of independent VAX/VMS operating systems that communicate through the system-communication architecture (SCA). To understand how VAX/VMS evolves from a one-computer operating system into a VAXcluster operating system, consider the example of a simple file-processing operation for a single computer and then for the VAXcluster.



In a single computer (Fig. 5), file requests pass to the file manager. The file manager maps the file operation into reads or writes of specific disk blocks, and it calls the disk manager, which does the physical reading or writing of the disk.

In the VAXcluster, of the three nodes (Fig. 6), two are VAX-11 computers and one is an HSC50 mass-storage controller. The file managers and disk managers of each computer are structured as they were in the first example. SCA services and the CI ports provide communications paths between the disk managers and the disk controller and between the file managers. The paths from the disk managers to the disk controllers permit each computer to access the disk directly, and the path between the file managers synchronizes state changes in the file system, ensuring that each file manager has a consistent definition of it.

Communications services

SCA provides the mechanism that lets the VAXcluster's software components communicate. Of its four basic communications services, the first is connection management. A connection is a logical communications path between two processes. The example (Fig. 6) presents three independent connections, each of them made through the computer interconnect: from disk manager 1 to disk controller, from disk manager 2 to disk controller, and from file manager 1 to file manager 2 (important for file synchronization). The connection-management service establishes these links.

When they have been established, the three other services—datagram transfer, message transfer, and block-data transfer—can all be used. Datagrams are small information units (each typically containing tens to hundreds of bytes) sent through a connection. Delivery is not guaranteed, for datagrams are used to send status information that is generated periodically and can be lost without disaster. They are also used by software with its own protocols to ensure reliable communication—the DECnet network manager, for example.

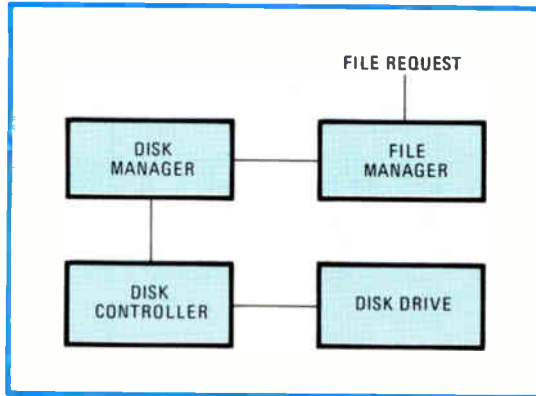
Both messages and datagrams are small units of information sent through connections. But the delivery of a message is guaranteed by protocols more elaborate than those required by datagrams. Messages are used, among

other things, to carry disk read and write requests.

In block-data transfers, data moves in blocks of arbitrary size between virtual-memory buffers, and its delivery is guaranteed. The block-data service is used, among other things, to move data associated with disk read or write requests.

The VAXcluster's most important innovation is its distributed file system, which makes VAXcluster files local to each VAX/VMS operating system. Distributed-file support upholds the VAXcluster's goals of ease of extension and availability. As more disks are added, associated files are immediately available to all computers, and as more computers are added, all stored files are immediately available to them. When a computer running a given application fails, the application can be moved to another computer, which has the same access to files.

Any file system that supports sharing should be able to lock files and records selectively. Rather than create a special lock mechanism for each VAXcluster resource, the VAXcluster provides a common facility: a distributed lock manager that provides a space where processes can lock and unlock resource names. Should a process require access to resources whose names are locked, it can be



5. Single computer. On this single computer, file requests go to the file manager. It determines which blocks on the disk are to be read or written and then requests them from the disk manager, which sends commands to the disk controller for the reads and writes. The file and the disk managers are operating-system software modules.

resource B. Process 2 has locked resource B and is blocked waiting for resource A. If not for deadlock detection, both processes would wait indefinitely. With it, the deadlock is detected and resolved. If a computer fails, the lock manager releases the locks held by all processes running on the failed machine, so the processes waiting on the others can continue.

A common journal facility provides services for the distributed-file system. The journal notes all of any file's state changes and can be used to roll a file back from a later to an earlier state, or to roll a file forward from an

queued in a wait state until they are unlocked.

The distributed lock manager provides a name space that is a tree structure allowing complex objects to be locked at different levels. For instance, the tree structure reflects the correct relation between the locks on a file and the locks on its individual records. In addition, the distributed lock manager can detect deadlock, in which a set of processes is blocked awaiting resources held by processes in the set.

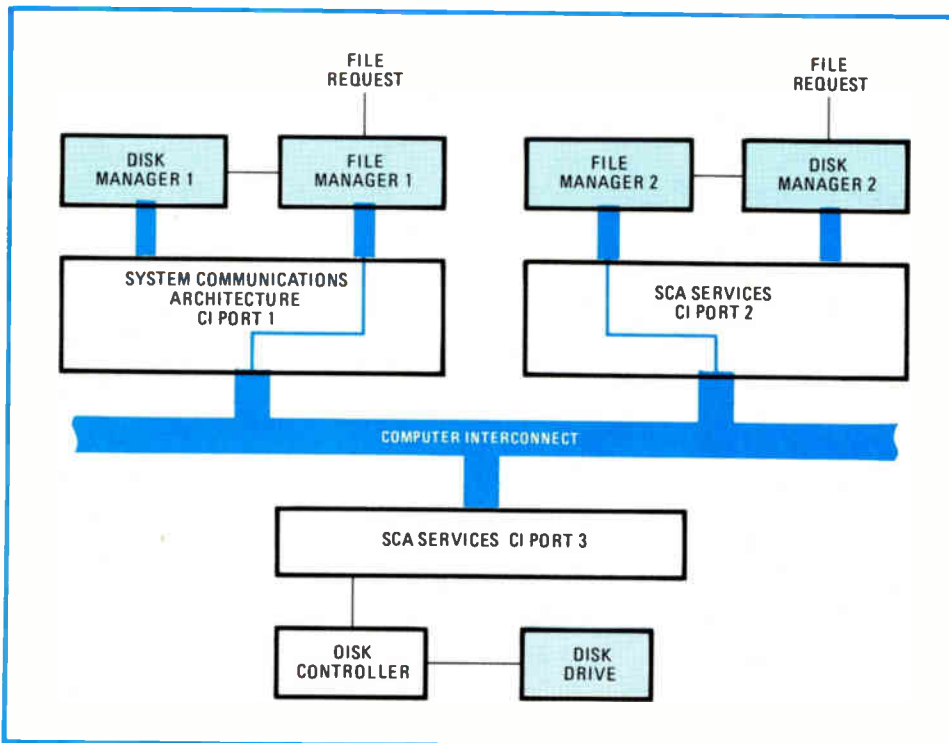
Consider a simple case of deadlock: two processes, 1 and 2, and two resources, A and B. Process 1 has locked resource A and is blocked waiting for

resource B. Process 2 has locked resource B and is blocked waiting for resource A. If not for deadlock detection, both processes would wait indefinitely. With it, the deadlock is detected and resolved. If a computer fails, the lock manager releases the locks held by all processes running on the failed machine, so the processes waiting on the others can continue.

A common journal facility provides services for the distributed-file system. The journal notes all of any file's state changes and can be used to roll a file back from a later to an earlier state, or to roll a file forward from an earlier to a later state. By recording the source of each file's state changes, the journal provides an audit trail.

Data-base operations often involve a series of changes to one or more files. To maintain the consistency of the data base, all the changes must be made—or none. The series is called a recovery unit. Should such a failure occur within it, the recovery-unit facility uses the journal to restore the file system to its former state.

When an application program issues checkpoint calls, the system's checkpoint and restart facility stores the complete state of the application. If the computer fails, the application can start over from the most recent checkpoint, not from the beginning. Before it starts again, the recovery-unit facility restores the files to their state at the last checkpoint. □



6. Cooperation. In this case of VAXcluster file processing, two computers access one disk subsystem. Software handles communications between the two disk managers and the disk controller and between the two file managers. The path between file managers synchronizes changes to the file system.

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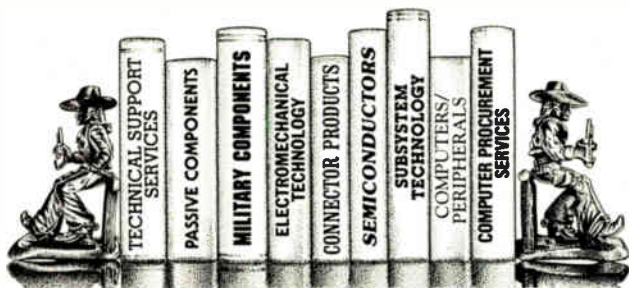
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Video-speed filtering gets its own digital IC

Single chip paves the way to faster filter implementation in a design process that depends on careful analysis of the application

by Fred Williams, TRW LSI Products, La Jolla, Calif.

□ Video-speed digital filtering jumps into the realm of practicality with the advent of the TDC1028 single-chip filter. This bit-slice pipelined part makes it easy to design and implement both fixed and adaptive filters.

Filter design has not yet reached the simplicity of the black-box level. Still, close attention to the concerns outlined below and ample use of the computerized aid available to implement today's filters do make it easier. Finite impulse-response (FIR) digital filters provide stability (no drift of performance characteristics with time, temperature, or voltage), repeatability (every filter of a given design provides exactly the same characteristics), exact linear phase, and high performance.

The basic idea underlying digital filtering is that any signal can be represented exactly by equally spaced samples, provided that they are taken often enough by analog-to-digital converters with sufficient precision. Once these samples are taken and formed into a sequence of numbers, calculations can generate a different numerical sequence that represent the filtered output signal. If needed, the numerical, or digital, output can then be converted to analog form for further use. The only inaccuracy in the entire process is the rounding involved in expressing the value in a fixed number of digits.

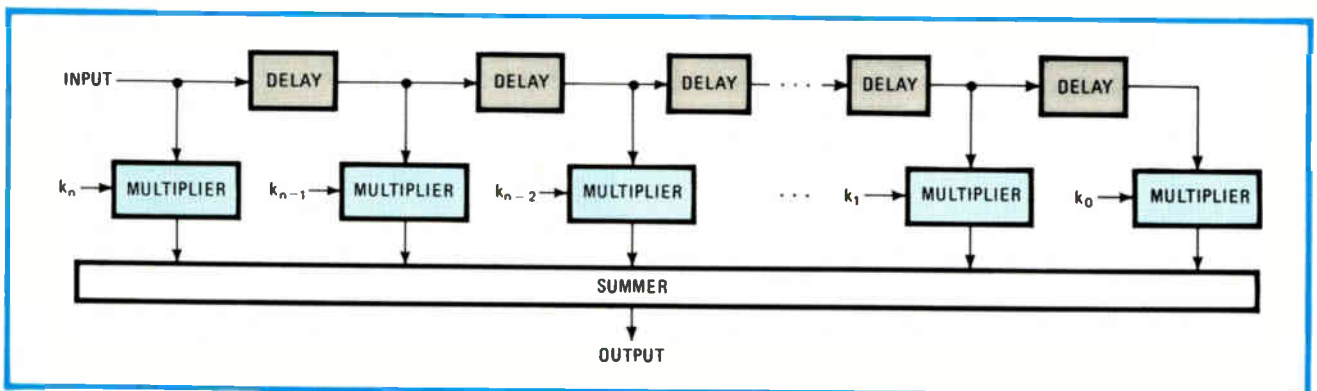
In working with a sequence of numbers, only a limited number of elementary operations can be performed. The numbers can be multiplied by various constants, divided, added, subtracted, and delayed. Since the basic realm of operation for numerical, or digital, filters is the time (rather than the frequency) domain, these limited mathe-

matical operations can result in filtering, even though the basic operations do not include any frequency-sensitive function. For example, when a delayed version of a sine wave is added to the original sine wave, their phase differences cause them to be added at low phase differences, canceled at 180°, and added again at 360°.

Time and frequency

Since a frequency response with this shape cannot be used for very many operations, some way of obtaining a more general response is needed. Examining the relationship between the time domain and the frequency domain provides an idea of how this is done. One of the basic relationships is that a single feature in one domain corresponds to a periodic feature in the other. For example, a pure sine wave in the time domain becomes a single impulse at the frequency of that sine wave in the frequency domain.

The key to designing any desired frequency response lies in a fact known from Fourier analysis—that any waveform or response can be decomposed into a sum of different sine waves in either time or frequency. These different sine waves correspond to different delays, and their amplitudes correspond to different weights. The amplitudes of these sines are given by the Fourier series representing that waveform or response. So, to design a filter, designers just state the desired frequency response as a Fourier series, and then each term corresponds to a specific delay and weight for that delay in a block diagram (Fig. 1). All this has been automated in computer



1. **FIR filter.** A finite impulse-response filter of this type produces a weighted average of the present and past input-signal samples. In this canonical configuration, an input signal passes through n delays and requires n multiplications to produce the filtered output signal.

2. Gibbs phenomenon. An ideal low-pass filter (a) produces a corresponding impulse response (b). But when this ideal impulse response is truncated by physical (finite-length) devices, the resulting frequency response exhibits characteristic passband and stopband ripples (c).

programs, so a hand solution is not necessary.

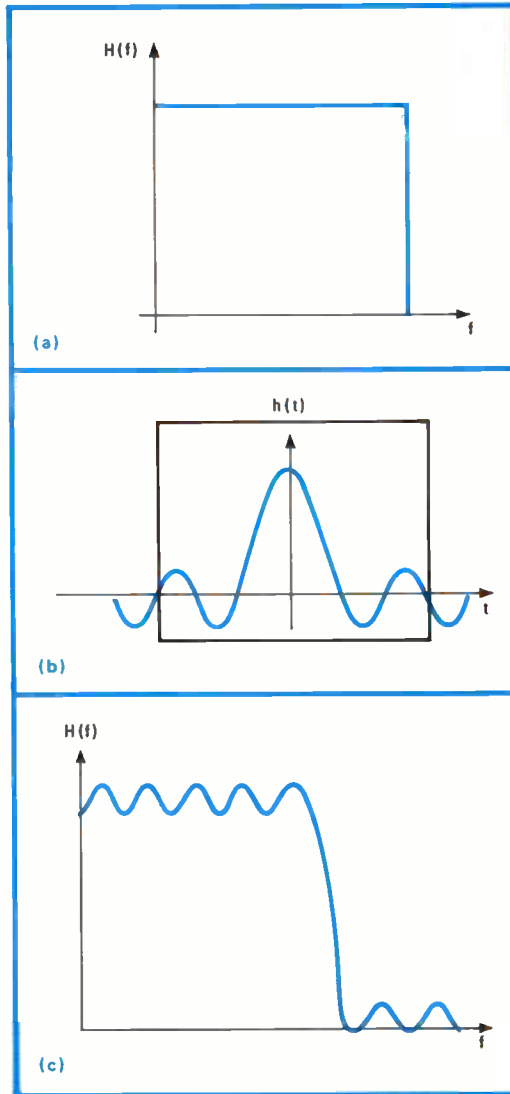
Although designers aim for perfect response from their filters, the corresponding Fourier series for such a response needs an infinite number of terms. Not only is the impulse response of a perfect low-pass filter infinitely long, but it starts before the impulse. In other words, the circuit must predict an input before it happens. The usual approach to this problem is to add a fixed delay, so that all the response occurs after the input. In the case of the ideal filter, this means adding an infinite delay, which is unacceptable. The immediate, but only partially correct, solution is to take just the largest terms of the impulse response and use those for the weights in the classic block diagram illustrated in Fig. 1.

Still, in using this approach, the ripples in the frequency response, called the Gibbs phenomenon, must be eliminated or at least reduced. Gibbs phenomena can be explained by an examination of the effect of selecting only some of the coefficients as a result of multiplying the infinite series by a square pulse (Fig. 2). Multiplication of a signal by another in the time domain is the same as convolution in the frequency domain. Since the spectrum of a square pulse is expressed as a $(\sin x)/x$ ripple, one way to get rid of the ripples is to use some other method that tapers off to zero.

This operation, called windowing, was used in much of the early work with this type of filter. Although some current books still advocate windowing, it is not efficient. To get the desired performance, the circuit needs more costly multipliers and delays.

Computer optimization, fortunately, provides designers with a more efficient means of optimizing their filter designs. Based on a mathematical procedure published in 1949 by the Russian mathematician E. Ya. Remez, two American researchers, T. W. Parks and J. H. McClellan, developed a computer program for the design of FIR filters. This program—available at low cost from the Institute of Electrical and Electronics Engineers—is very widely used because it provides the best possible designs for given specifications using a finite number of sines.

Given a conceptual block diagram and a set of coeffi-



icients, the major task in designing an FIR filter is to select and implement an architecture that performs the function of the block diagram at adequate speeds. Four general design approaches are available for building an FIR filter: creating an architecture identical to the basic architecture of Fig. 1, modifying the basic architecture, using general-purpose digital signal-processing architectures, or using general-purpose computer architectures (including microprocessors).

The basic architecture is capable of high-speed operation but is not always the most cost-efficient choice. Furthermore, the design of an adder tree with a large number of wide input words is not easy, given the limited selection of adders available in most logic families. Often, to reach the desired throughput rate for the available output bandwidth, multiple pipeline stages are required, with their attendant design complexity.

One way to avoid the design of a large adder tree is to distribute the summation function over the whole circuit by using multiplier-accumulators. Each data input value is multiplied by every coefficient and added to the sum in each register. Ev-

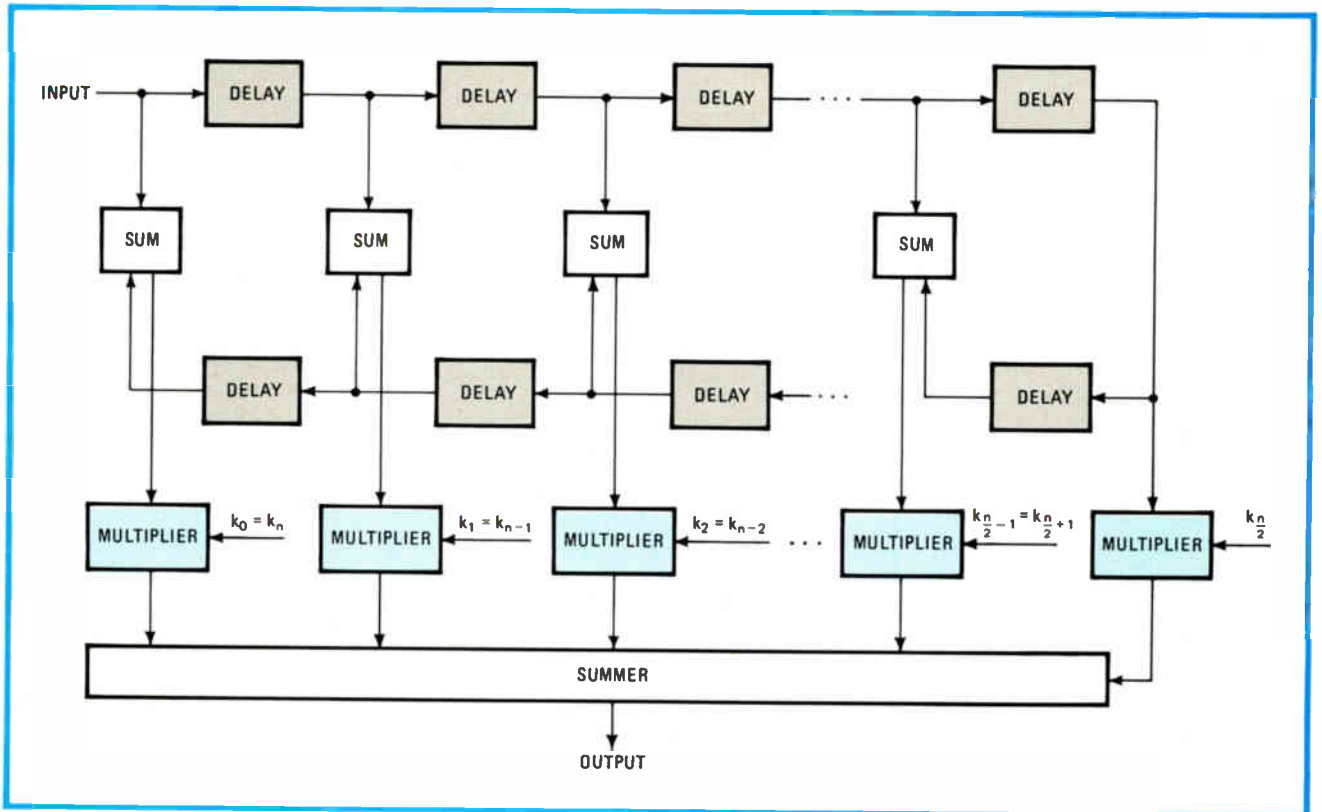
ery coefficient is then shifted to the right, and the process repeated. The result is taken from the accumulator register, which has the whole set of points accumulated, and that register is then reset.

Eliminating the adder tree

Thus the input data can be processed in the cycle time of the multiplier-accumulator. This approach eliminates the adder tree, but it is limited by the cycle time of the multiplier-accumulator. There is no convenient way of obtaining higher speed: methods like alternating or "ping-ponging" devices are impractical because of the critical synchrony involved.

Because most FIR designs are linear-phase designs, the coefficients are symmetrical about the filter midpoint, suggesting another possible improvement on the basic architecture. According to the distributive law of algebra, the number of multiplications may be cut in half by first adding the two data points with the same coefficient and then multiplying (Fig. 3). However, this approach still requires a large adder tree.

In general-purpose digital signal processors, several techniques result in high performance. First, because con-



3. Folded FIR. By taking advantage of the symmetry of the coefficients, this configuration of an FIR filter reduces the number of multipliers needed. Instead, input samples corresponding to symmetrical points on the filter are added before being multiplied by the coefficient.

ditional operations are not usually necessary, control circuitry can be completely separated from calculation circuitry. Furthermore, the basic design allows the use of pipelined operations. Finally, the use of microprogrammed control makes the design extremely versatile. Unfortunately, such microprogrammed devices are very complex and difficult to design. A more recent development in digital signal processing is the single-chip digital processor, such as the Intel 2920, AMI2711, NEC7720, and TMS320. Although these chips are powerful enough to handle lower-bandwidth signals, none is capable of video-speed operation.

Of course, standard digital computers and microprocessors can be used to process signals. However, the performance of most general-purpose architectures is constrained by bottlenecks in the arithmetic and logic unit—used for both data and address manipulations—and the bus—used for data flowing in several directions. Consequently, such parts are an inefficient solution to the general problem.

Beating common problems

Despite their various advantages or disadvantages, all these approaches still share some common problems. Unequal word sizes for signal data and filter coefficients lead to inefficient use of the circuitry. To use these approaches, a designer must be skilled not only in filter specification and design but also in high-speed digital design and possibly in microcoding. Finally, none of these approaches can handle video operation.

TRW's TDC1028 was designed to address the draw-

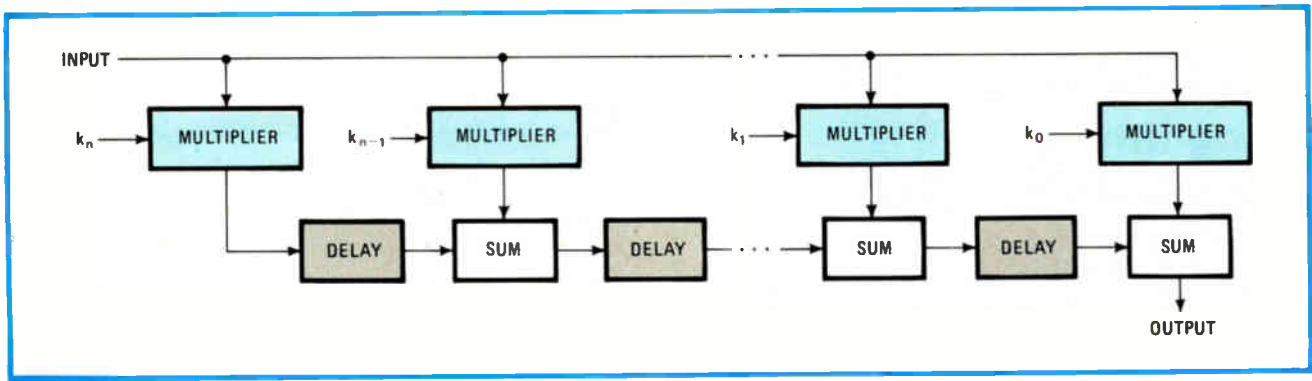
backs of all these approaches. The chip directly addresses one problem in high-speed digital design—that of delay between components—by providing a high level of on-chip integration. It offers several stages of multiplication, addition, and pipeline registers on a single chip.

Furthermore, the problems of circuit complexity have been dramatically reduced by the observation that delay, multiplication by a constant, and addition are all linear operations. As a result, their order can be interchanged, subject to a few constraints (Fig. 4).

Because it is intended for use by circuit and systems designers whose expertise is in the area of their specific application, the 1028 has been designed for easy expansion of filter length, the size of the coefficients, and the size of the signal data word. Any given filter will have its signal data words and its coefficient words in multiples of 4 bits, and the 1028 does not require equal word lengths for both. This arrangement allows the number of bits in the signal data words to be chosen to provide the necessary signal-to-quantizing-noise ratio for proper system operation.

On the other hand, the number of bits in the coefficients can be chosen to provide the desired accuracy in the frequency response. Although the signal-to-quantizing-noise ratio is usually the main factor in choosing the number of bits in the signal data word, the decision is also based on distortion—harmonic and intermodulation—and on dynamic range. These requirements can vary dramatically from one application to another.

The ability to control the word size helps designers deal directly with one source of deviation from the ideal



4. Dual response. The architecture of the TDC1028 and the canonical design (shown in Fig. 1) exhibit an identical response. In the TDC1028, the result of the operation is passed along through the delay lines; in the canonical design, the input signal is passed along.

response specified by the filter designer: the deviation caused by the limited resolution of the coefficient word. By choosing the proper number of bits in the coefficient word, the designer can reduce errors introduced by the difference between the physical resolution and that of the perfect mathematical expression. (Another source of error is the difference between the desired theoretical response and the polynomial used to approximate that desired response. This deviation is due to the finite filter length and can only be improved by increasing the filter length.)

Partitioning bits

Regardless of the word dimension in which the 1028 is to be expanded, the basic approach is the same. A single binary number can be partitioned into groups of 4 bits (possibly with one group containing fewer bits). For example, to multiply two such numbers together, all possible ordered pairs of groups from the multiplicand and from the multiplier must be multiplied together, properly weighted, and added.

The output of each 1028 or cascade of 1028s is a 13-bit word with a weighting that is either 1 or a power of 16. These values must be added to give the final result. The straightforward way uses a tree of adder chips to produce the product. Alternatively, the normally unused adder associated with each cascade may be used to construct filters with no external adders. However, to use the internal adders, the signals for the more significant bytes must be delayed so that the latency is the same for all parts of all signals. This delay can be achieved with simple short shift registers. Since there is a very limited selection of medium-scale integrated shift registers, TRW is developing a variable-length, 8-bit-wide shift register as a support part.

Expansion of filter length merely requires connecting the devices end to end using the internal adders. The setup and hold times have been optimized to permit direct interconnection even at the highest clock frequencies. A cascade of two or more 1028s will behave as a single part in circuits where the data-word sizes are increased (with the exception of a longer filter characteristic, of course).

One of the most important characteristics of FIR filters is their unconditional stability. There are no coefficient combinations that yield an unstable system, as there is no

feedback to create any form of oscillation. This feature is most important in adaptive filtering, which is an extremely important and rapidly growing area of digital signal processing.

The reason for the importance and growth of adaptive filtering lies at the very root of filtering. In many systems the exact specifications of both the desired and unwanted parts of the waveforms are not known precisely at the time of design. Although compromise filters can cover most of the possibilities, the cost of such a compromise is lower performance than could be obtained by a properly matched filter. If the filter is made so that its response can be adjusted as a reaction to how well the output matches the ideal signal, performance can be increased—sometimes dramatically.

To use an automatically adjustable filter, the circuitry must be able to detect the desired or the unwanted signal, making a comparison signal necessary. This reference signal may either be stored internally or applied as a separate input. Usually, the desired, or reference, signal is subtracted from the actual output, giving an error signal. At this point, some technique must be used to change the filter coefficients to minimize the error signal.

A handy algorithm

Although this subject is still undergoing intense research, many applications use an algorithm developed by Bernard Widrow at Stanford University, Palo Alto, Calif. In the Widrow algorithm, larger changes are made in the coefficients when the total error signal is large than when the error signal is small. Individual coefficients are adjusted according to the error at the point in the signal that corresponds to that individual coefficient. This is a straightforward technique with good performance. In classical implementations of the Widrow algorithm, each coefficient is updated each n clock cycles, where n is the filter length.

The 1028 facilitates the construction of adaptive filters by storing all coefficients in internal registers. One coefficient in each device can be changed every clock period (which, of course, can be down to 50 nanoseconds). This capability means that the filter coefficients can be updated faster than the updating values can be calculated for many applications. Special attention has been paid to the ability to make clean transitions between two different response characteristics. □

Using timers to drive three steppers concurrently

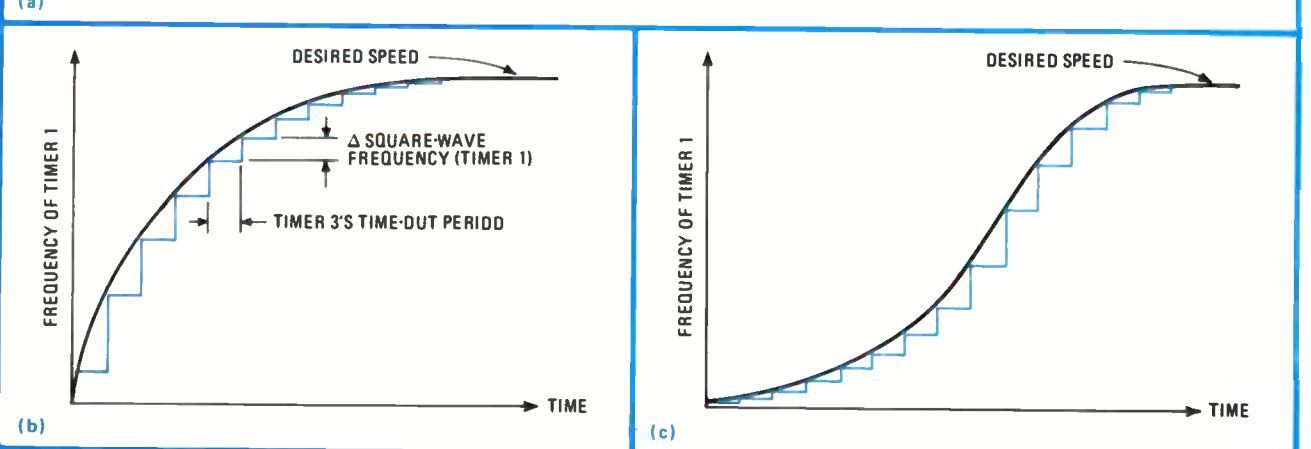
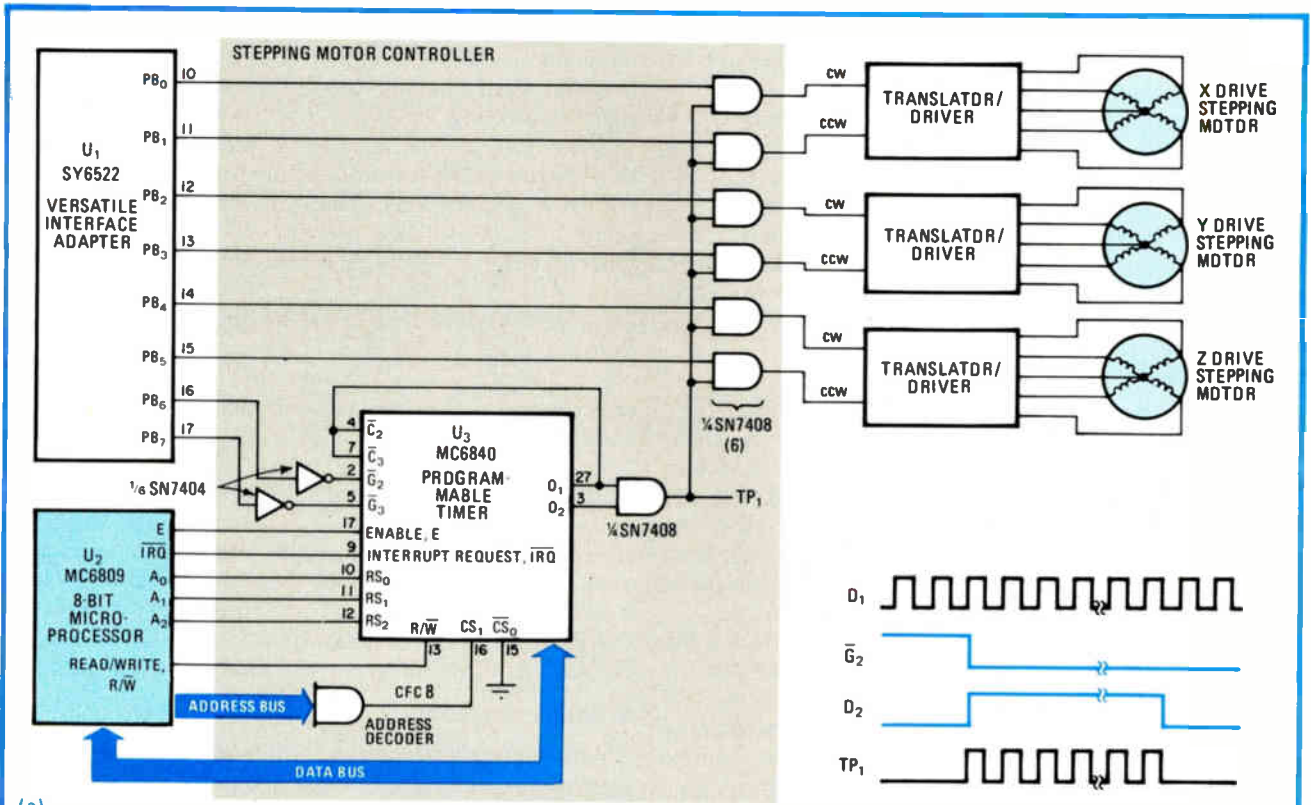
by Dan Hamden
Ontario Hydro, Pickering, Ontario, Canada

A design using Motorola's microprocessor MC6809 and programmable timer MC6840 drives up to three stepping motors simultaneously (a). In addition, it can control the

motor's speed and number of revolutions independently. The microprocessor programs the timers such that timer 1 functions as a square-wave generator and timer 2 serves as a single-shot.

To drive the motor, microprocessor U₂ initializes timer 2 with a count equal to the number of pulses that need to be transmitted to the stepping motor. The processor then simultaneously triggers timer 2 and enables the appropriate AND gates via port B of U₁. The stepping motor starts and continues to run until timer 2 times out.

The microprocessor employs sense or interrupt modes to detect the motor's motion. In the sense mode, the



Controller. This design (a) provides a controller that is capable of handling up to three stepping motors. When a motor is turned on, U₂ programs U₃ to make timer 1 function as a square-wave generator and timer 2 as a single-shot. Also, U₂ enables the gates via U₁. If two motors are driven simultaneously, timer 3 functions as a single-shot. The acceleration (b and c) is achieved by adjusting the frequency increments in timer 3.

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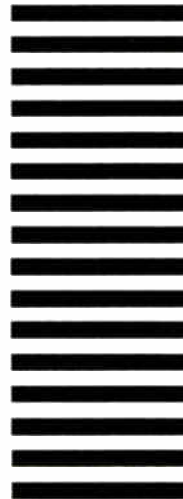


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- F. Medical, industrial controls, systems or equipment
- G. Semiconductor production equipment (component insertion, coil winding, etc.)
- H. Electronic sub-assemblies, components and materials (passive, active components, IC's, discretes, hybrids, power supplies)
- I. Other manufacturers using electronics equipment as part of their product (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
- J. Government and military
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- M. Independent software developers
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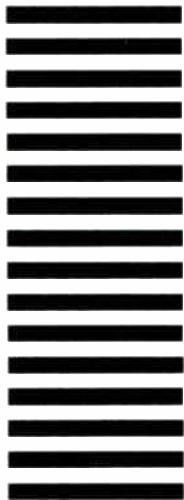


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```

00100 ;
00110 ;
00120 ; THIS DEMONSTRATION PROGRAM WILL ILLUSTRATE THE USE
00130 ; OF THE STEPPING MOTOR CONTROLLER. THIS PROGRAM
00140 ; FUNCTIONS IN SENSE MODE AND WILL DRIVE 2 STEPPING
00150 ; MOTORS AT ONCE.
00160 ;
00170 ;
00180 ;
00190 ;
00200 ;
1000          00210      ORG    $1000
                1000    00220 START EQU    *
1000 10FE    3FFF    00230      LDS    STKTOP ;INITIALIZE STACK POINTER
1004 86      FF      00240      LDA    = $FF ;ASSIGN ALL BITS OF
1006 87      CFE2    00250      STA    VIADR8 ;PORT B AS OUTPUTS
00260 ;
00270 ; SET UP 6840 PROGRAMMABLE TIMER
1009 86      21      00280      LDA    = $21 ;SET UP
100B 87      CFC9    00290      STA    CNTLR2 ;CONTROL
100E 87      106A    00300      STA    CREG2 ;REGISTER 2
1011 86      02      00310      LDA    = $02 ;SET UP
1013 87      CFC8    00320      STA    CNTLR1 ;CONTROL
1016 87      1069    00330      STA    CREG1 ;REGISTER 1
1019 FC      106C    00340      LDD    FREQ ;SET UP FREQUENCY OF
101C FD      CFCA    00350      STD    CTR1 ;SQUARE WAVE
101F 86      1069    00360      LDA    CREG1 ;TURN
1022 8A      80      00370      ORA    = $80 ;ON
1024 87      1069    00380      STA    CREG1 ;SQUARE WAVE
1027 87      CFC8    00390      STA    CNTLR1 ;OUTPUT
00400 ;
00410 ; DRIVE THE DESIRED STEPPING MOTORS
00420 ;
102A 86      06      00430      LDA    = $06 ;SELECT MOTORS AND
102C 87      106E    00440      STA    DIREC ;DIRECTION OF TRAVEL
102F CC      2600    00450      LDD    = $2600 ;SET UP THE SINGLE
1032 FD      CFCC    00460      STD    CTR2 ;SHOT'S TIME
1035 8D      03      00470      BSR    DRIVE ;TURN THE MOTORS ON
1037 8D      18      00480      BSR    WAIT ;WAIT FOR MOTORS TO STOP
1039 3F      00490      SWI     ;END OF DEMONSTRATION
00500 ;
00510 ;
00520 ; DRIVE : THIS ROUTINE WILL TURN ON THE DESIRED MOTORS
00530 ;
00540 ;
103A 34      06      00550 DRIVE PSHS    D
103C 86      106A    00560      LDA    CREG2 ;ENABLE
103F 8A      80      00570      ORA    = $80 ;OUTPUT
1041 87      106A    00580      STA    CREG2 ;OF
1044 87      CFC9    00590      STA    CNTLR2 ;SINGLE SHOT
1047 86      40      00600      LDA    = $40 ;TURN ON MOTORS BY TRIGGERING
1049 BA      106E    00610      ORA    DIREC ;SINGLE SHOT AND ENABLING THE
104C 87      CFEO    00620      STA    VIAPT8 ;APPROPRIATE GATES
104F 35      86      00630      PULS    D,PC
00640 ;
00650 ;
00660 ; WAIT : THIS ROUTINE WILL SENSE WHEN THE STEPPING
00670 ; MOTOR MOVEMENT IS COMPLETE. IT WILL THEN DISABLE THE
00680 ; SINGLE SHOT'S OUTPUT AND ALL GATES.
00690 ;
00700 ;

```

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```

1051 34 06 00710 WAIT PSHS D
1053 FC CFCC 00720 WAIT1 LDD CTR2
1056 26 FB 00730 BNE WAIT1
1058 B6 106A 00740 LDA CREG2 ;DISABLE
105B 84 7F 00750 ANDA #$7F ;THE
105D B7 106A 00760 STA CREG2 ;SINGLE SHOT'S
1060 B7 CFC9 00770 STA CNTLR2 ;OUTPUT
1063 4F 00780 CLRA ;DISABLE ALL
1064 B7 CFE0 00790 STA VIAPT8 ;GATES
1067 35 86 00800 PULS D,PC
00810 ;
00820 ;
00830 ; DATABASE
00840 ;
00850 ;
00860 ; VIA EQUATES
CFE0 00870 VIAPT8 EQU SCFE0 ;PORT B ADDRESS
CFE2 00880 VIADRB EQU SCFE2 ;DATA DIRECTION REGISTER B
00890 ;
00900 ; PROGRAMMABLE TIMER EQUATES
CFC8 00910 CNTLR1 EQU SCFC8 ;CONTROL REG 1 (SQ. WAVE GEN.)
CFC9 00920 CNTLR2 EQU SCFC9 ; " " 2 (SINGLE SHOT)
CFC8 00930 CNTLR3 EQU SCFC8 ; " " 3
CFC9 00940 SREG EQU SCFC9 ;STATUS REG.
CFCA 00950 CTR1 EQU SCFCA ;TIMER 1 LATCH/COUNTER
CFCC 00960 CTR2 EQU SCFCC ; " 2 " "
CFCE 00970 CTR3 EQU SCFCE ; " 3 " "
00980 ;
3FFF 00990 STKTOP EQU $3FFF ;TOP OF STACK
01000 ;
1069 01010 CREG1 RMB 1 ;CONTROL REG. 1 IMAGE
106A 01020 CREG2 RMB 1 ; " " 2 "
106B 01030 CREG3 RMB 1 ; " " 3 "
106C 0500 01040 FREQ FDB $500 ;FREQUENCY DIVIDE FACTOR
;[SQUARE WAVE FREQ. =
; CLK FREQ./FREQ. DIV. FACTOR]
01050 ;
01060 ;
01070 ;
106E 01080 DIREC RMB 1 ;DIRECTION STATUS WORD
01090 ;:BIT0 - X DRIVE CW
01100 ;:BIT1 - " " CCW
01110 ;:BIT2 - Y DRIVE CW
01120 ;:BIT3 - " " CCW
01130 ;:BIT4 - Z DRIVE CW
01140 ;:BIT5 - " " CCW
01150 ;
1000 01160 END START
00000 TOTAL ERRORS

```

single-shot's counter is continually read, and when it reaches 0 the motor's movement stops; in the interrupt mode, the single-shot generates an interrupt when its counter reaches 0.

Bit 4 of U_2 's condition-code register must be reset and bit 6 of timer 2 control register in U_3 must be set when the controller is being operated in the interrupt mode. Similarly, when operating in the sense mode, the state of at least one of the above bits must be complemented.

The assembly-language program in the table illustrates the method for simultaneously turning on two motors for a different number of steps. In this case, timer 3 of U_3 is used as a single-shot. Timer 2 is loaded with the count for the motor requiring the most steps, and timer 3 is loaded with the count for the motor requiring the least steps. The processor triggers both timers simultaneously. When timer 3 times out, the AND gate for the motor requiring the fewest steps is disabled.

Acceleration is accomplished by using timer 3 of U_3 as a single-shot, with a much smaller count than timer 2. After the timers are triggered simultaneously by the microprocessor, timer 3 times out relatively quickly. When this occurs, the square-wave generator's frequency increases and timer 3 is retriggered. This procedure is repeated until the desired speed is achieved, at which point timer 3 is no longer triggered. Adjusting the frequency increments and the count in timer 3 achieves the desired acceleration curve (b and c). Deceleration proceeds similarly, except that the frequency of the square-wave generator is decreased.

The translator driver, which distributes an incoming pulse train to the stepping-motor windings in a proper sequence, depends on the type of stepping motor used. □

Electronics invites readers to submit short, original, unpublished programs and software solutions to engineering problems. Explain briefly and thoroughly the program's operation and send to Ashok Bindra, Circuit Design Editor. We'll pay \$75 for each item published.

Magnetic-media care is topic of new guide

Can overheated or water-damaged computer tapes and disks be salvaged? Can the little memo magnets found in many offices erase floppy disks? How clean should storage areas for magnetic tapes or disks be? A new publication from the National Bureau of Standards reviews the care and handling of all types of magnetic data-storage media and makes 56 recommendations on proper maintenance. Available from NBS for \$5.50, "Care and Handling of Computer Magnetic Storage Media" (SP 500-101) may be ordered from the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. Specify stock No. 003-003-02486-4.

I'll see that bit and raise you a byte

Computer cards have come a long way from 80-column Hollerith days. In fact, Sam Pitroda, an engineer with over 50 telecommunications patents, has invented a novelty deck of playing cards based on binary powers of 2^0 through 2^7 . Math operators of sum and multiply create 16 cards per suit. Values of 64 and 128 are "computer" and "programmer" cards and take the place of the king and queen, and a "software bug" has replaced the traditional joker. **Each 64-card deck has four suits and can be used for all kinds of games, including poker.**

The deck comes with simple game instructions, and users who invent new games can win a Game-of-the-Month prize. For a free copy of a book that describes some of these new games and for information on the cards, write to Compucards Inc., P. O. Box 4745, Oak Brook, Ill. 60521, or phone (312) 850-7244.

Beating interference and static in electronic gear

Today all design engineers require expertise in electromagnetic interference in addition to the troublesome problem of electrostatic discharge. "Emi and ESD Control in Electronic Systems" is the name of a seminar that will run in Philadelphia on Dec. 5 and 6 and should help satisfy this need.

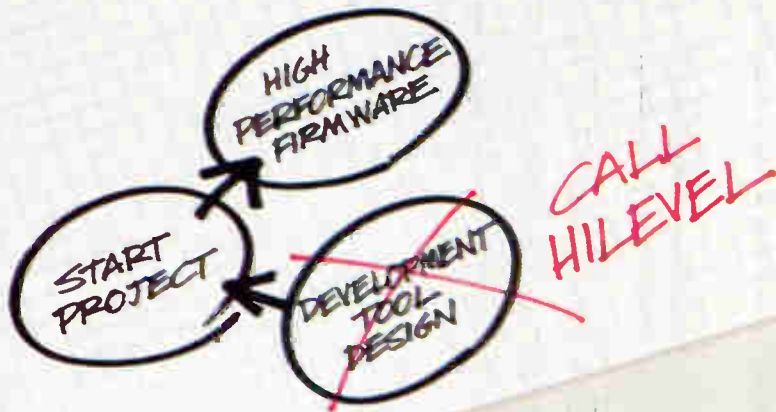
The first day will cover "The ESD Threat—Designs for Production and Control," and the second day will deal with "Printed-Circuit-Board and Wiring Designs for emi Control." Sponsored by R&JB Enterprises, a division of Robar Industries Inc., 20 Clipper Rd., West Conshohocken, Pa. 19428, the seminar costs \$495.

Software catalog covers third-party programs for Apollo Domain

Because personal computers have attracted consumers who favor one-stop shopping for all of their system needs, Apollo Computer Inc. has joined the herd of computer companies providing catalogs of the software applications available from independent software houses. The "Catalog of Applications for the Domain," the company's engineering system, contains more than 120 programs, from 40 vendors, covering 14 categories of applications.

Aiming primarily at engineering and architectural problems, the 200-page catalog also lists consultants and sources of hardware peripherals. For a copy, get in touch with a local Apollo sales office or with Steve Weinberger, Apollo Computer Inc., 15 Elizabeth Drive, Chelmsford, Mass. 01824.

—Roger J. Godin



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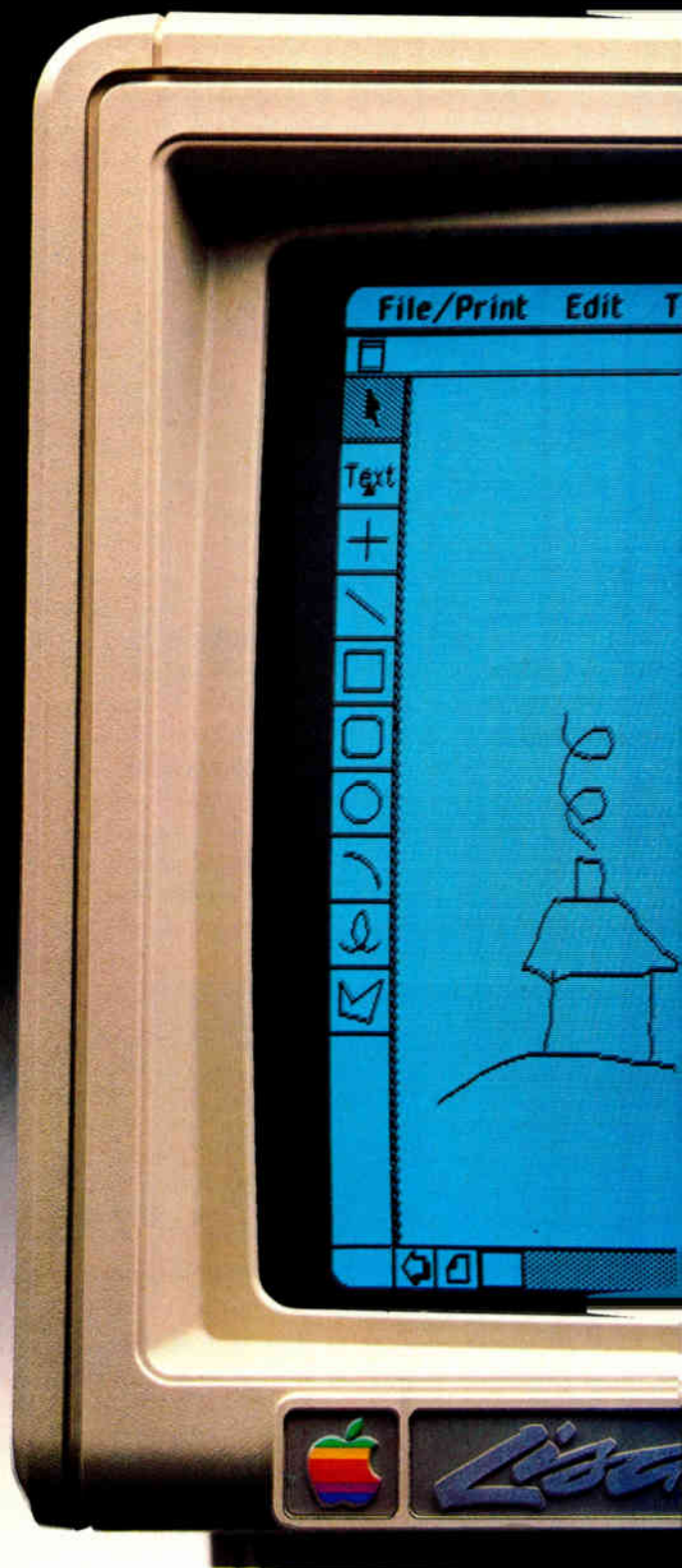
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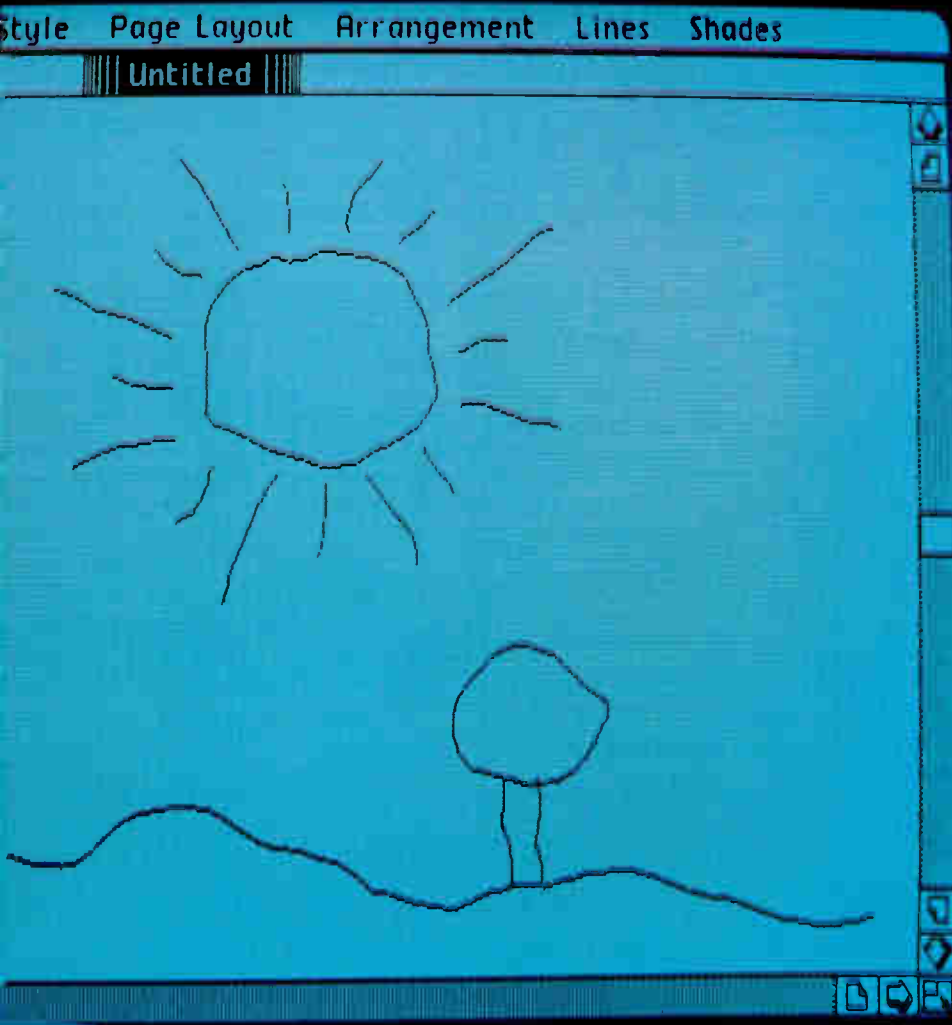
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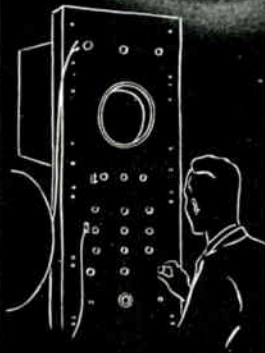
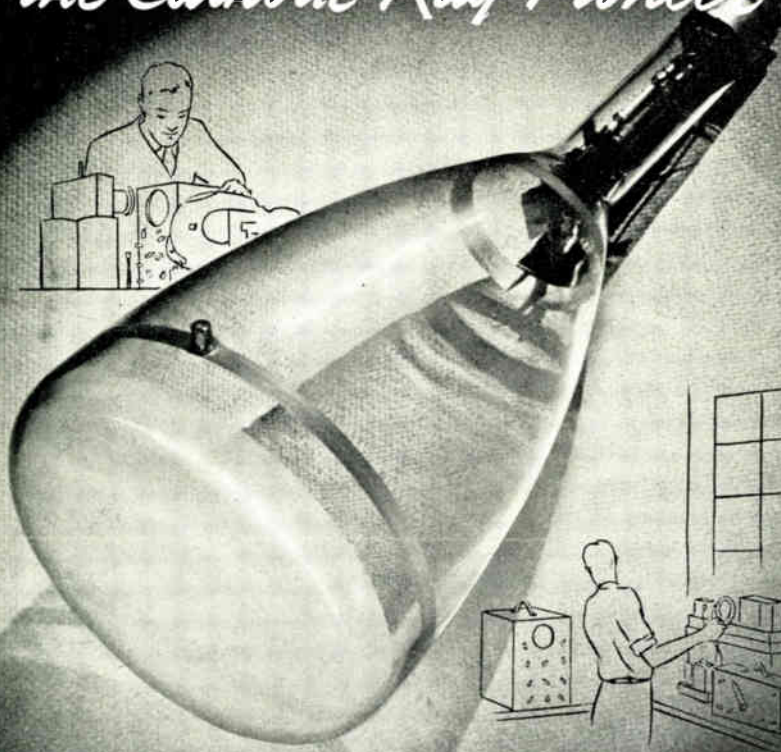
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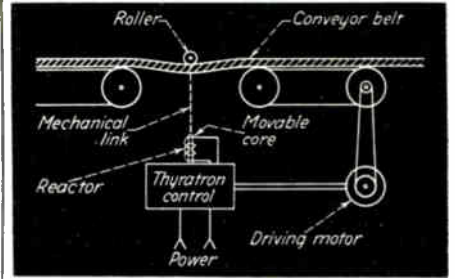
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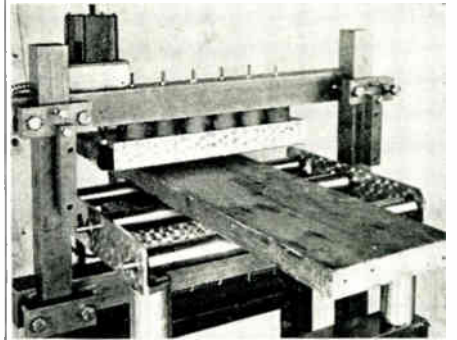
Conveyor synchronizer using thyatron control, shown in elemental form

thyatron tubes by the phase-shift method. The belt-driving motor is connected to the power line through the thyatrons in such a manner that when the belt sags the motor speeds up while straightening of the belt causes the motor to slow down.

Many variations and refinements of this synchronizing scheme are possible.—Henney, *ELECTRON TUBES IN INDUSTRY*.

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Nail detector. If lumber passing through the jaws contain nails an alarm is operated or the board is marked at the location of the nails

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BUILDING BETTER COMMUNICATIONS WORLDWIDE

Distributed system controls factory

Factory-automation system links wide range of equipment by distributing microprocessor-based intelligence along local net

by Wesley R. Iversen, Chicago bureau manager

Turnkey factory automation takes a step closer to reality with a powerful distributed-control system and factory network slated for first public showing at the Autofact 5 Conference and Exposition, to be held in Detroit, Nov. 14-16. Offered by GCA Corp.'s Industrial Systems Group, the Cimcell controller and associated Ethernet-based Cimnet is billed as the most cost-effective means yet for integrated manufacturing control. It can provide a 30% to 50% price advantage over techniques that rely on a general-purpose superminicomputer for control, contends Dennis E. Wisnosky, group vice president.

"Cimcell will typically go in applications where a company wants unmanned flexible manufacturing," Wisnosky explains. Once a manufacturing schedule is fed into the system, Cimcell will not only control and monitor work but will also modify the sequence to maintain real-time operation as the need arises.

The system generates up-to-the-moment reports on everything from the number of good and bad parts produced to machine use and down time. Cimcell can also watch for emergencies: Wisnosky envisions applications in which a voice-synthesis module might be tied into the system to notify plant personnel of problems, even over a phone line.

The GCA system is equally well suited for a wide spectrum of batch-manufacturing jobs, ranging from semiconductor-wafer fabrication or printed-circuit-board handling to tasks like metal cutting and bending, the company says. A key to this flexibility is Cimcell's ability to tie in factory equipment from any number of different vendors. Though the sys-

tem's heart is a cabinet housing at least four 16-bit 8086 microprocessors and up to 1.2 gigabytes of fixed and removable disk memory, the Cimcell architecture is nonetheless highly distributed—8086-based interface modules scattered around the factory floor provide the links to the 10-Mb/s Cimnet.

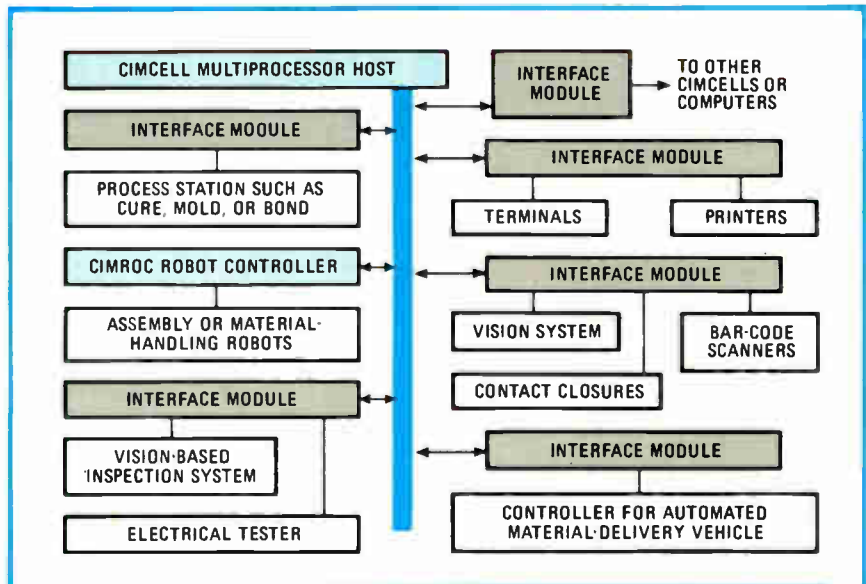
The company is developing a software library aimed at accommodating a broad range of standard computer and industrial-equipment protocols, according to Margaret A. Eastwood, GCA's vice president and general manager for integrated-factory controls. Software is complete for linking to specific computerized numerical controllers, such as Allen-Bradley's model 8200, as well as RS-232-C- and RS-422-based devices like the Burr-Brown TM71B Microterminal bar-code reader. Synchron-

ous Data-Link Control and 3270-compatible links are also ready.

Software is also complete for an automated guided vehicle called Cartrac from SI Handling Co. and six other pieces of equipment that GCA will not name due to customer-confidentiality agreements. Many more are in the works, the firm says.

Program store. GCA will provide a Cimcell connection to a company's host mainframe computer along with connections to a variety of computer-aided-design systems to download parts programs. Robot or machine programs can be downloaded from Cimcell to the equipment, and programs developed on a robot can be uploaded to Cimcell for storage.

A typical Cimcell application links computerized numerical and other controllers that are handling various machine tools, robots, or other



Typical cell. Cimcell's 8086-based interface modules, linked to the Ethernet-based Cimnet and scattered about factory floor, bind equipment such as that shown into coordinated system.

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New products

equipment, as well as bar-code, vision, tactile, and other sensor systems that provide the necessary real-time inputs. Several color terminals might also be spread around the network, some equipped with printers. Automated materials-handling systems might also be connected.

Depending on the complexity of the equipment, one interface module can connect up to 16 devices to the Cimnet. GCA's own Cimroc robot controller—which itself incorporates up to eight 8086s for control of GCA robots—has a built-in Cimnet interface. Though GCA says that customers will have to do very little, if any, software development for Cimcell, the system does support Cimpler, the same GCA language used for off-line Cimroc programming. Pascal programming is also an option. Both Cimroc and Cimcell rely on Intel's iRMX-86 operating system.

Although GCA's Eastwood recommends Cimcell for use in controlling factory "cells," she adds that a large factory could be totally automated by linking several Cimcells under the control of a central Cimcell. One Cimnet can accommodate 1,024 interface modules.

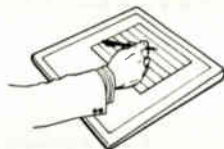
Takes heat. Cimcell is packaged for placement directly on the factory floor, without a special air-conditioned environment; a color graphics terminal and printer are part of the system. Several Cimcell systems have already been sold, and GCA plans to make initial deliveries during the second quarter next year.

A minimum Cimcell setup with 300 megabytes of disk storage, linking four or five machine tools and at least one GCA robot on the Cimnet would be priced at around \$500,000, Wisnosky estimates, not including the robot or other factory machines. Additional interface modules for linking machines already in the GCA library will cost \$8,000 to \$12,000 each, Wisnosky says. Modules to link equipment not in the library would require software development by GCA, and might be priced higher. GCA Corp., Industrial Systems Group, One Energy Center, Naperville, Ill. 60566. Phone (312) 369-2110 [Circle reader service number 338]

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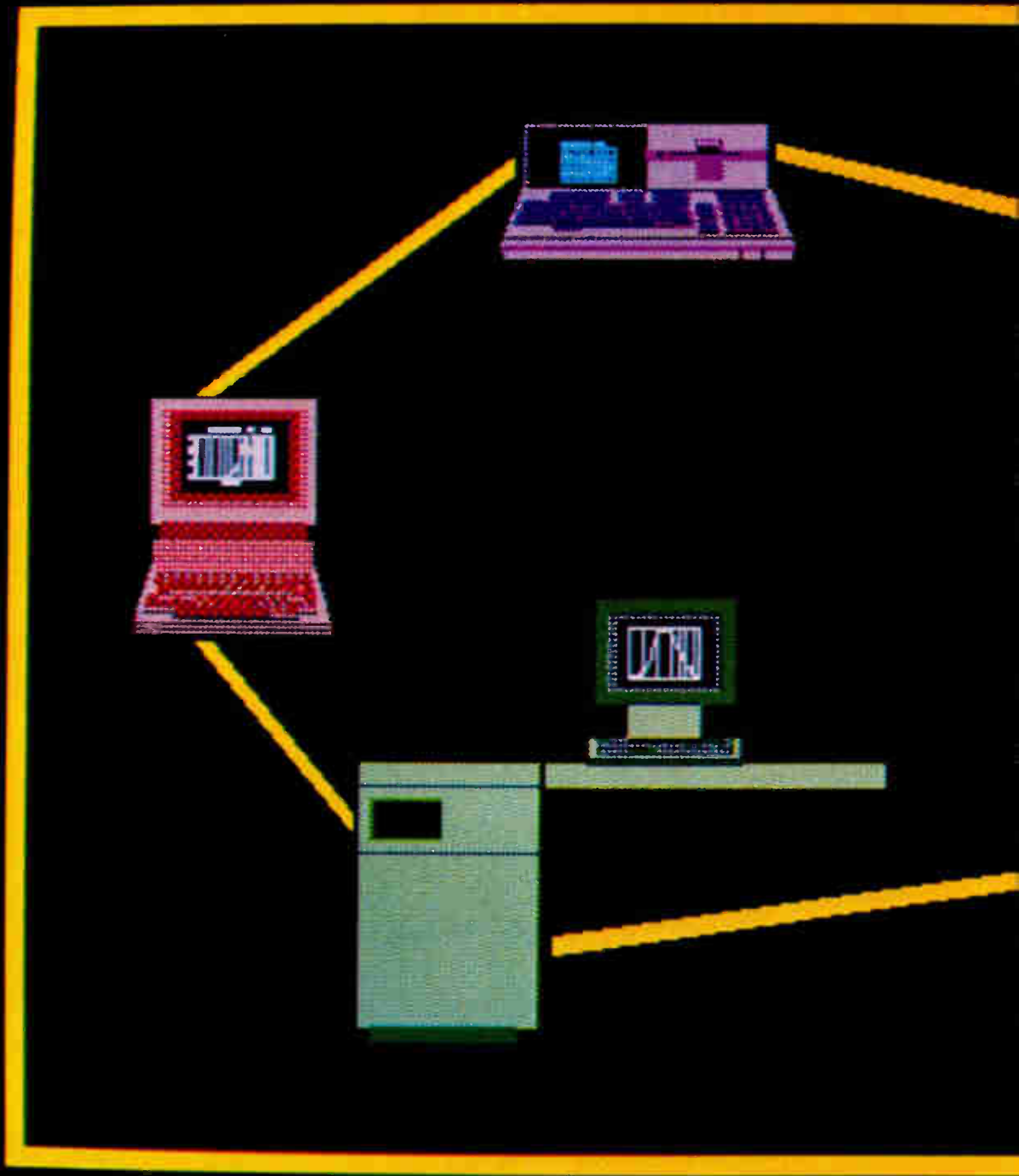
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It's called the Engineering Productivity Network. As you can see, it includes the broadest range of workstations available anywhere. From the recently-introduced 32-bit HP 9000 desktop mainframe to our personal computer designed just for engineers.

With such a wide range to choose from, you can match the computing power to the individual task. And give every engineer the tool it takes to do the best possible job.

To help you tailor every workstation to a task even more closely, we have over 200 specific application software packages. And since our workstations use HP-UX—our enhanced version of the UNIX* operating system—we'll be able to bring you a lot more in the future.

Of course, when you tie all these individually-optimized workstations together into a network, you can look for an even higher level of performance. Whether you choose our HP-UX networking, Ethernet local area network, or Shared Resource Manager, your engineers can share data and peripherals, communicate much better, and get more done than ever before.

The HP Engineering Productivity Network. You can start with one workstation, or with dozens. But no matter where you start, you're actually making your whole department more productive. One step at a time.

To find out more, just call the nearest HP office listed in the white pages of your telephone book, and ask for a Technical Computer Representative. Or write to Pat Welch, Dept. 44167, Hewlett-Packard, 19447 Pruneridge Avenue, Cupertino, CA 95014. In Europe, write Henk van Lammeren, Hewlett-Packard, Dept. 44167, P.O. Box 529, 1180 AM Amstelveen, The Netherlands.

We'll be happy to show you how far you can really go with a good idea.

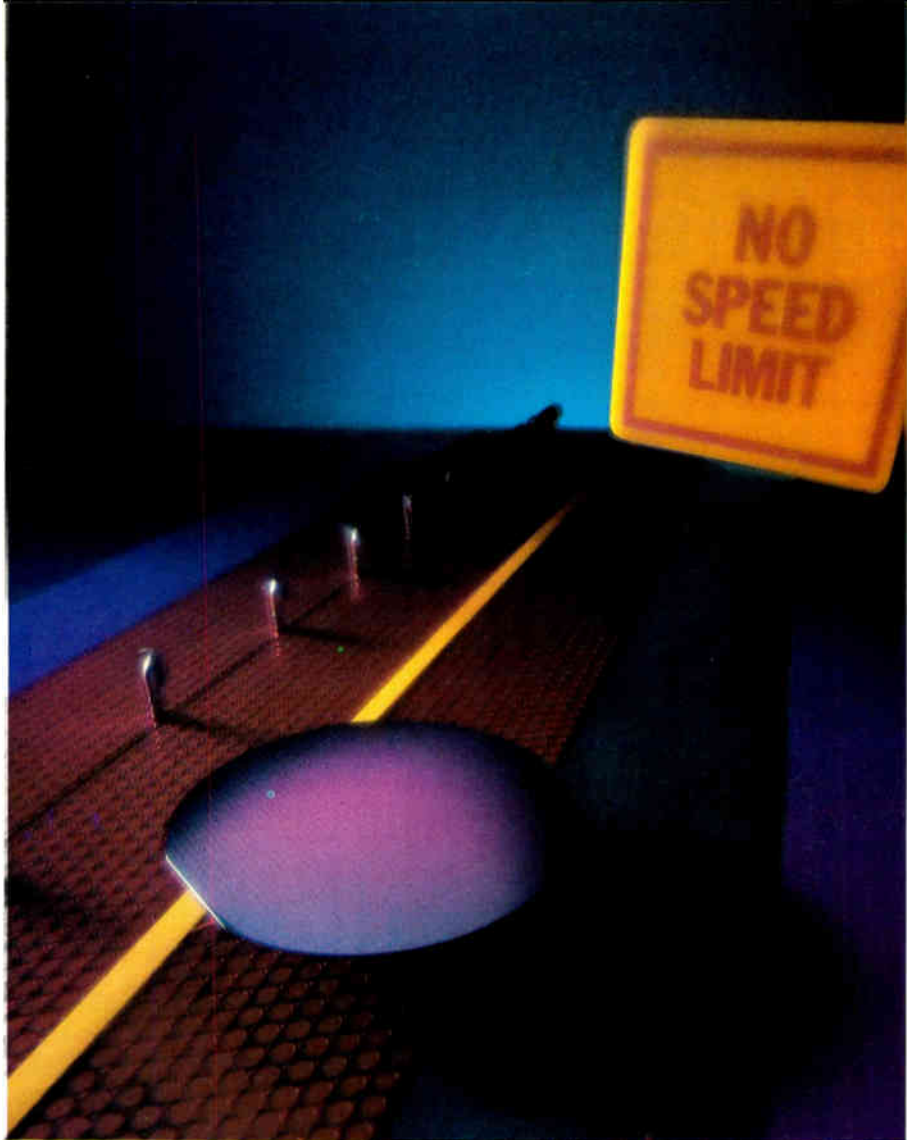
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7C-03309

Circle 165 on reader service card



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Circle 167 on reader service card

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Gates Energy cells deliver dependable back-up power that keeps your lines alive. They're rated at 2 volts with capacities at 2.5 Ah, 5 Ah, 12.5 Ah and 25 Ah. And they can be assembled into an endless variety of configurations.



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Gates Energy cells provide outstanding cold weather performance (50% of C/10 room temperature capacity at -40°C). And you'll get 8-10 years life at 23°C in float applications.

Learn how Gates Energy cells can keep your electronic equipment working when the local power company can't.

Call, or write, Gates Energy Products Inc., 1050 S. Broadway, Denver, CO 80217. (303) 744-4806.



Industrial**Multibus system is portable**

Portable personal computer is targeted at industrial and scientific applications

The recent flood of portable personal computers has provided business professionals with a selection of machines. Engineers, scientists, and technicians also need transportability, but in a different product, according to Monolithic Systems Corp., which is introducing a portable microcomputer designed for multitasking needs in laboratory and industrial environments.

To achieve the speeds and flexibility necessary for such jobs, Monolithic Systems has designed the MSC 8807 portable computer—dubbed the Indy (for industrial) PC—around a Multibus architecture, using an 8-MHz 80186 microprocessor. The Multibus supports up to 2 million transactions/s, providing the data rates needed to conduct real-time tests and measurements.

Customers will have a choice between iRMX-86—Intel Corp.'s multiuser multitasking real-time operating system—and Concurrent CP/M-86—Digital Research Corp.'s single-user package that executes up to four tasks at one time. Compilers are available for software development in Fortran, Pascal, version 7 of C, and Basic (for which an interpreter also is available).

Utilities running under CP/M-86 or iRMX-86 will appear identical to users and will operate in the same way. A formatting utility can handle both Winchester and microfloppy disks. Other software modules include: full-screen editor, assembler-linker, and routines for burning programmable read-only memories.

"Portable-business-computer customers are interested in the systems primarily for application software packages—what they see, they get.

Business customers are not going to be plugging in additional cards for testing, data acquisition, and software development," notes Daniel P. Campbell, product line manager. "But in the scientific-industrial community, customers are more interested in hardware features and the development tools."

To the work. The engineers and scientists at whom the Indy PC is aimed "will be attracted to a portable system because it saves laboratory desktop space, which is getting very expensive," says Jack Bakeman, manager of software engineering. "And computers are getting small enough now that people prefer to take them to the work, rather than taking the work to the computer."

Housed in a metal casing, the Indy PC weighs 35 lbs, including a 9-in. cathode-ray tube; two 3½-in. floppy-disk drives; detachable keyboard; 6-slot Multibus chassis; 100-w power supply; cooling fan; and built-in carrying handle. The unit also has serial and parallel ports, as well as a standard Small-Computer System Interface (SCSI). The main-processor board carries 128-K bytes of dual-port dynamic random-access memory with parity, a RAM controller, and up to 128-K bytes of erasable PROM.

Three basic versions of the system

will be available for volume shipments in the first quarter of 1984. A portable-terminal version (with all boards removed except the CRT controller and with no disk drives) sells for \$1,975 in single quantities. This product is aimed at original-equipment manufacturers who wish to add their own processor cards.

An Indy PC with 128-K bytes of RAM costs \$4,875 including Concurrent CP/M-86, and the same unit with iRMX-86 support is priced at \$5,475. Monolithic Systems also plans to make available an evaluation unit with 512-K bytes of RAM (using 256-K dynamic RAMs), at \$6,775. Volume deliveries of the latter are slated for the third quarter of 1984.

The system's host processor—the MSC 8186 single-board microcomputer, which is also being made available separately—offers two ISBX bus connectors for adding special-function modules. These piggyback modules can add a wide range of analog functions, expanded input/output capability, and fixed or floating-point math operations. By late 1984, Monolithic Systems plans to offer computers with the 8087 coprocessor for such jobs as real-time waveform analysis.

Only half of the chassis' six slots are occupied; three are open for stan-

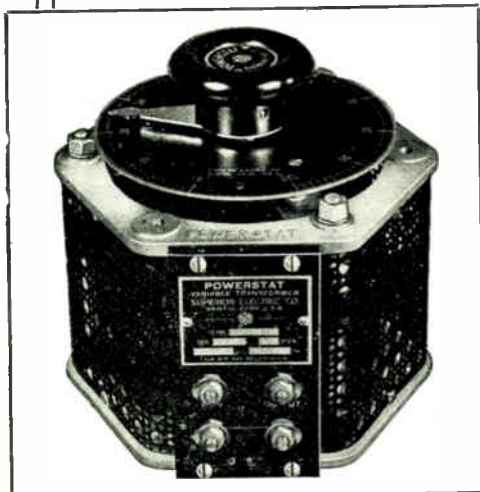




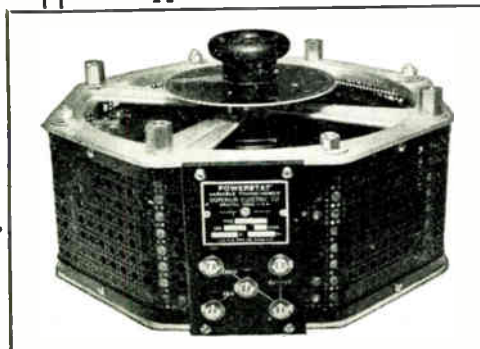
POWERSTAT

VARIABLE TRANSFORMERS

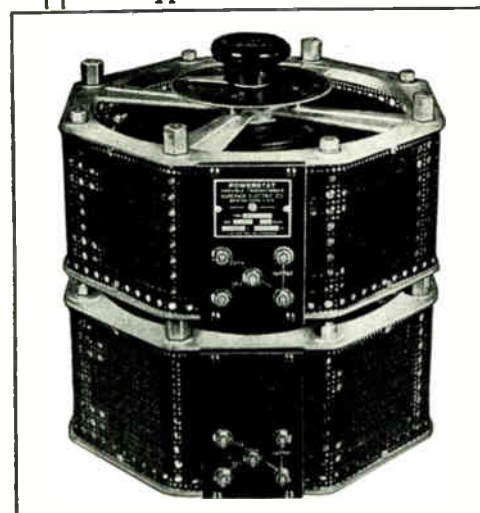
And Seco Automatic Voltage Regulators



Type 1126 Powerstat



Type 1256 Powerstat



Three-Phase Powerstat

Powerstat — the Variable transformer that accurately controls power for all electronic and radio purposes as Tube Filament Voltage Control, Transmitter Bias Power Supply Voltage Control, and Transmitter Plate Supply Control.

Type 1126 Powerstat

Input: 115 volts 50/60 cycles

Output: 2.0 KVA

Max. Rated Output Current: 15 amp. available over entire range of output voltages

Output Voltage Range: 0 to 135 volts

No-load Power Loss: 16 watts

Over-all Dimensions: 8 x 8 x 7³/₈ inches

Net weight: 20 lbs.

Type 1256 Powerstat

Input: 230/115 volts 50/60 cycles

Output: 7.5 KVA on 230 volt line

Max. Rated Output Current: 28 amp. available over entire range of output voltages

Output Voltage Range: 0 to 270 volts

No-load Power Loss: 40 watts

Over-all Dimensions: 14³/₄ x 14³/₄ x 8 inches

Net Weight: 66 lbs.

Typical Three-Phase Powerstat Type 1256-2

Input: 230/115 volts 3 phase 50/60 cycles

Output: 13.1 KVA on 230 volt line

Max. Rated Output Current: 28 amp. available over entire range of output voltages

Output Voltage Range: 0 to 270 volts

Connection: See figure 7 of Bulletin 149

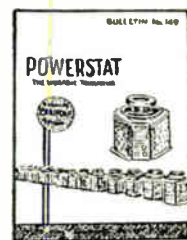


Oil Mounted Powerstat in Stainless Steel Tank



Seco Automatic Voltage Regulator

is used for radio transmitters and many types of electronic devices requiring reasonably close tolerances of line voltages. Important for radio transmitters located at the ends of long feeder lines where regulation is poor and voltage fluctuation wide (Send for Bulletin 163 LE).



Send for Powerstat Bulletin 149LE

Superior Electric Co.

36 HARRISON ST.

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New products

standard Multibus boards. The firm estimates some 190 manufacturers are offering about 900 Multibus products, which span the range of industrial and laboratory applications.

Monolithic Systems is planning to make available soon a Winchester disk drive in the system, along with the two Sony-format 80-track 3½-in. floppy-disk drives, each holding 409-K bytes. The firm chose the single-sided 3½-in. drives because of their

size and speed, Bakeman says. They have a 500-kb/s transfer rate, twice that of most 5¼-in. drives.

The unit, which can slip under an airline seat, has an operating temperature range of 10° to 45°C. Customers may select 120- or 230-v power supplies.

Monolithic Systems Corp., 84 Inverness Circle East, Englewood, Colo. 80112. Phone (800) 525-7661 or (303) 770-7400 [Circle reader service number 371]

Vision system checks boards

General-purpose system looks for badly inserted parts, can recognize serial numbers

Currently, electrical inspection is the most accurate way to find manufacturing flaws in printed-circuit boards. Unfortunately, this method can only be used after the solder goes down on the board, so that mistakes in component placement become expensive to repair. Checkpoint is a hardware and software package designed to perform automated visual inspection for pc-board manufacturers and in other quality-control applications.

Based on the image-recognition technology of Cognex's DataMan vision system, Checkpoint can read the serial number on a circuit board to call up board and component layouts for which it was previously trained. Using this data, it will verify proper lead insertion on the board's bottom side prior to soldering. Software for checking for the presence and absence of components, determining component orientation, verifying part numbers on dual in-line packages, and bad-lot identification of DIPs will be available next year.

The inspection system will be trainable for board layout, component shapes, and part numbers on DIPs. Mul-

tiply component shapes and part numbers may be defined as valid in the same position to allow components from different vendors to be verified properly.

The system uses an optional integrated X-Y table that moves pc boards in view of the camera. As a result, accurate placement of the board on the table is unnecessary.

DEC host. The system recognizes 64 levels of gray and has a resolution of 576 by 452 picture elements. Its host microprocessor is a DEC LSI-11/23 with 256-K bytes of memory and will be upgradable with a J11-based board in a few months.

In order to check both the top and bottom of the board, two cameras along with the needed software and data-base options will be necessary and will cost around \$100,000. The standard Checkpoint system, which costs \$30,000, stores and identifies images. Such a system would be good for checking keys on keyboards, for instance. Software for printing or pc-board applications costs between \$10,000 and \$15,000.

The vision system looks for learned characteristics when scan-

ning a particular area, and its speed is dependent upon the resolution desired. For instance, for a low-resolution scan of an image measuring 10 to 20 pixels, Checkpoint can recognize 100 characters/s. For high-resolution scans of 60 to 100 pixels, the system is slowed to 2 characters/s.

Checkpoint may be used to read printing and was designed to recognize shapes; it is primarily a quality-control tool. It is available now.

Cognex Corp., 72 River Park St., Needham, Mass. 02194. Phone (617) 449-6030

[Circle 372]

Portable industrial controller runs intelligent peripherals

A portable industrial controller, called the Linker 100, runs a single intelligent peripheral from a central location. Featuring an intelligent display and keyboard, and a central processing unit, the Linker 100 can be programmed to run any industrial



controller, printer, simulator, or other peripheral through an RS-232-C full-duplex asynchronous serial input/output port.

The controller's Z8 microcomputer communicates with the keyboard and the display and the equipment under control; it is these intelligent peripherals that allow the Linker to provide overlapped concurrent processing. For example, the display could perform a monitoring function while the user changes operating parameters from the keyboard.

The Z8 is supported by a battery-backed 16-K random-access memory, 64-K read-only memory, and 32-K of programmable ROM and uses a Basic Debug operating system. Two lines of up to 40 characters each can be



viewed on the liquid-crystal display. All 48 keypad keys are software-definable to suit individual requirements; a customized overlay identifies each key's function.

Carrying a price of \$400 each in lots of 100, the Linker 100 is available in six weeks.

Analogic Corp., 14 Electronics Ave., Danvers, Mass. 01923. Phone (617) 777-4500

[Circle 373]

Visual inspection system shows board's faults on a monitor

A real-time microprocessor-based inspection system examines printed-circuit boards and art without reprogramming. The IVS Inspector can compare individual pc boards (or films) with an error-free control image to pinpoint discrepancies, which are displayed in red on a monitor.

By eliminating reprogramming between inspections, the IVS Inspector can totally examine an 18-by-24-in. board in less than 1 s, with up to 0.000125-in. field-of-view resolution. The system, which can check boards and artwork at all stages of production, examines boards up to 27 in. on a side with a high-resolution vidicon camera, 512-by-512 picture-element digital visual analyzer, 64-K bytes of random-access memory, a microprocessor, and color monitor.

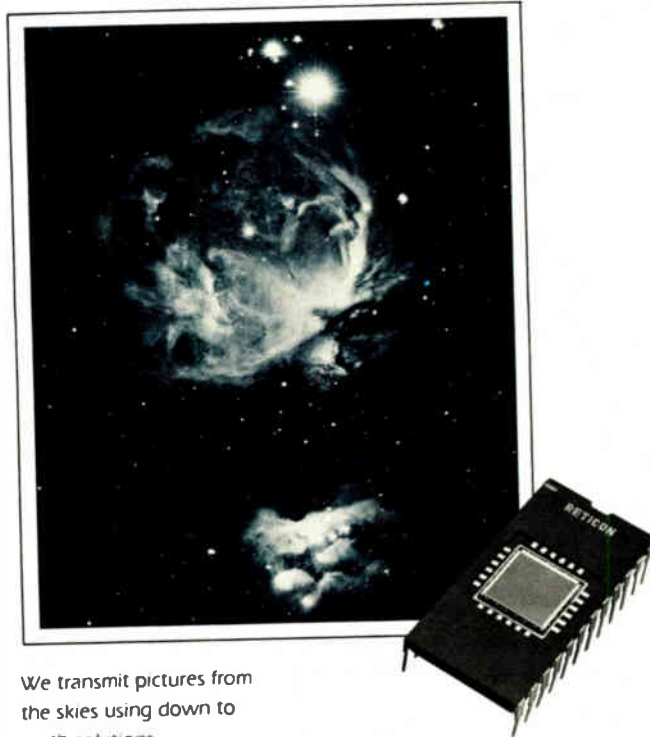
Available now, the IVS Inspector sells for \$48,000, depending on system configuration and options. Options include custom software, robotics interface, and specialized alignment fixturing.

Interactive Video Systems Inc., 358 Baker Ave., Concord, Mass. 01742. Phone (617) 371-0104 [Circle 375]

System evaluates accuracy, repeatability of robot motion

A robotic evaluation system consisting of a camera, light-emitting diodes, a LED-control unit, and a main controller measures the repeatability, trajectory, and accuracy of a robot's movements. Selective Electronics'

THE PERFECT IMAGE SENSOR



We transmit pictures from the skies using down to earth solutions.

Problem. Your image analyzer design needs to be computer compatible, have high resolution, a wide range of gray scale, be frame resettable with low blooming and zero defects.

The Perfect Solution. Reticon's new 128 x 128 area array. The 128 x 128 will give you the flexibility and quality you need.

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With the world's largest selection of image sensors, Reticon leads in quality and reliability.

Call us about your application. We'll be glad to discuss your image sensor requirement - either standard product or custom.

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New products

system combines a software package to optimize robotic movement and efficiency with the Selspot II noncontact motion-analysis system, which monitors motion.

LEDs are attached to selected points on the robot being monitored. Invisible infrared beams transmit minute changes in positions through an optoelectronic detector, which determines the center of the light image and generates output signals that are converted into precise position information. The main controller converts the positions into digital or analog output data for real-time recording and analysis; three-dimensional measurements can be made.

Available in 90 to 120 days, the robotic evaluation system sells for about \$70,000.

Selective Electronic Inc., P. O. Box 250, Val-dese, N. C. 28690. Phone (704) 874-2289

[Circle 376]

Vision system gives a part's size, determines deviation

At the push of a button, the View 1200 vision system makes high-speed measurements of radii, diameters, centers, distances, angles, and intersections, as well as of any angle in the X, Y, or Z axis. It can take three-dimensional measurements in 1/100th of the usual time, according to its manufacturer.

Employing the company's video-

image-processing technology and a moving stage, the View 1200 makes accurate measurement automatic and does not need a skilled operator. In measuring a part, the system's camera sends a video image to the processor, which electronically detects the black-white transitions that define the part's features.

The part is measured and compared to tolerances stored in memory, after which the View 1200 flashes on the monitor the exact measurements, deviations from standard, and pass-fail notification. The View 1200 can be multiplexed with up to four data-gathering units operated by one system-control unit.

Available now, the stand-alone system sells for \$87,500. Included are the data-gathering unit—which has a large granite stand with X, Y, and Z stages, table control, and video-processing electronics—and the system control unit—which has disk storage, monitor, keyboard, and processing electronics.

View Engineering, 1650 N. Voyager Ave., Simi Valley, Calif. 93063. Phone (805) 522-8439

[Circle 374]

Indexer interfaces stepping motor drivers with controllers

An indexer accurately controls a stepping-motor-driver system or provides an interface between a programmable controller and the motor system. The model 3016A's output is compatible with practically all available stepping-motor drivers—either those using step-step or those using step-direction sequences.

The indexer provides pulse-output command sequences of up to 999,999 pulses. Pulse-output number (distance) is set manually with a thumbwheel on the front panel. Index, alternate, and continuous-run operational modes enable the model 3016A to run through a sequence once, reverse direction, and then repeat the sequence or simply continue at the set rate until it is commanded to pause.

Start-stop rates range from 100 Hz to 1 MHz. Velocity—adjustable in the



field—ranges from 100 Hz to 20 kHz. Ramping time (from start-stop rate to maximum velocity) can be adjusted from 0.05 to 5 s.

The indexer is also available as a board-level unit with power supply and binary-coded-decimal inputs for use with a programmable controller. This version, the model 3020A, is an economical means of interfacing a stepping-motor driver to a programmable controller.

Both models are available from stock. The 3016A sells for \$650 and the 3020A for \$350.

Sigma Motion Control, 170 Pearl St., Braintree, Mass. 02184. Phone (617) 843-5000

[Circle 377]

Gate turn-off thyristors have 1,200-V blocking capability

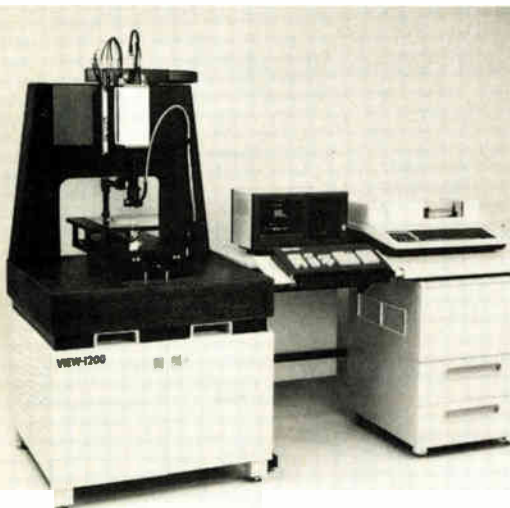
Featuring a 1,200-v blocking capability for 480-v ac three-phase operation, a line of gate turn-off thyristors serve the 10- to 200-hp ac adjustable-frequency motor-control market. Products include 100- and 200-A (turn-off) dual-thyristor isolated-base-plate modules and 450- and 600-A disk packages.

Integrated diodes are optional with the 100- and 200-A models. Used with the firm's Pow-R-Blok line of thyristor and rectifier modules, these diodes can connect an entire ac drive's power electronics to a single heat sink.

The company claims that the thyristors fill the need for greater capacities than Darlington transistors provide, enabling implementation of a broader horsepower spectrum using single-control techniques.

Available from stock, the thyristors range in price from \$70 to \$325 in lots of 100.

Westinghouse Electric Corp., Westinghouse Building, Gateway Center, Pittsburgh, Pa. 15222. Phone (412) 255-3329 [Circle 379]





Never has so little analyzed so much.

The new Sony/Tek 338 packs more power per pound and delivers more features per dollar than any other logic analyzer. Bar none.

You get both parallel and serial capabilities in the same machine. A cost-effective combination for either the first-time user or the experienced engineer.

For software work, you can utilize up to 3 levels of triggering

and 32 channels of parallel data at 20 MHz. And for hardware, there's the Sony/Tek 318, a 16-channel, 50 MHz version of the 338.

A menu-driven interface, glitch capture and reference memory make testing simple. An RS-232 interface permits remote control. And non-volatile memory permanently retains setups and reference data.

And when it comes to portability, the 338's super light weight and compact size put it in a class by itself.

The Sony/Tek 318/338. The undisputed leader in combined performance, price and portability. For more details, contact your local Tek Sales engineer or write us.

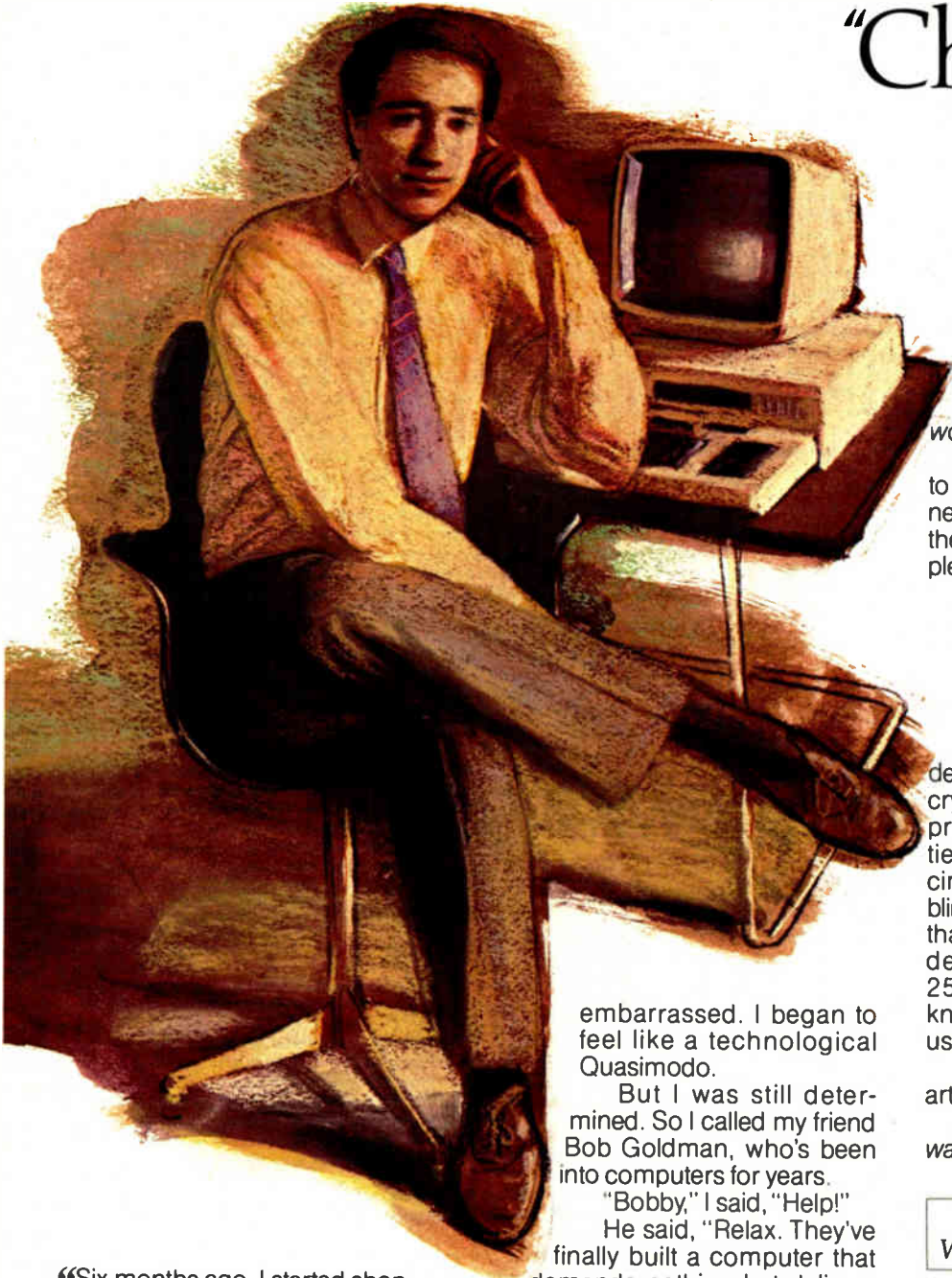
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CONFESSIONS OF A LOW TECHNOLOGY MAN.

"Choosing a about as Until I



...two personal computer printers sold worldwide comes from Epson.

Now they've turned their attention to the computer itself. And have engineered a breakthrough that has caught the other computer companies completely off guard:

STATE-OF-THE-ART SIMPLICITY.

That's the best way you could describe the Epson. For instance, the crystal sharp resolution of the screen provides amazing graphics capabilities. (Anyone who's tried to draw a circle and gotten something resembling an octagon knows how important that can be.) Yet, despite its double-density disk drives and powerful 256k memory, you don't have to know anything about computers to use the Epson.

No "computerese" to learn. No artificial routines to memorize.

All you have to know is *what you want*.

THE ERA OF PUSH-BUTTON WORK HAS FINALLY ARRIVED.

Across the top of Epson's keyboard is a row of keys labeled in simple English.



Each key does exactly what you'd think it would do.

If you want to draw a graph, for example, you press "Draw." Step-by-step, the Epson asks you what kind of graph, where you want the title, how many bars or slices it should have, and so on.

embarrassed. I began to feel like a technological Quasimodo.

But I was still determined. So I called my friend Bob Goldman, who's been into computers for years.

"Bobby," I said, "Help!"

He said, "Relax. They've finally built a computer that demands nothing but delivers everything. The Epson. And the only language you need to operate it you've already shown a reasonable mastery of: English."

EPSON???

As usual, Bobby knew what he was talking about. It seems that

Epson has become something of a legend in the computer industry by making the world's most reliable computer printer. *Today one out of every*

"Six months ago, I started shopping for a personal computer.

It was not a pleasant experience.

Half the sales people sized me up as "low tech" and avoided me like the plague. The other half said things I couldn't understand, showed me machines I couldn't operate without taking a computer class, or gave me demonstrations that had absolutely nothing to do with my business.

I was confused. I was



TECHNOLOGICAL QUASIMODO

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Peachcalc* is a trademark of Peachtree Software.

Wordstar* is a trademark of Micropro Inc.
Microplan* is a trademark of Chang Labs.

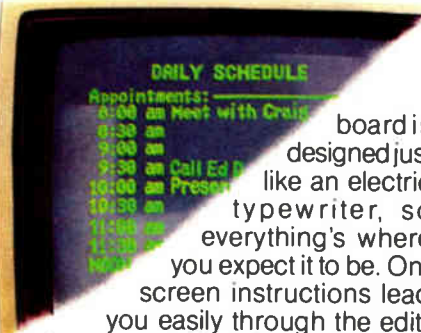
personal computer was much fun as having a root canal. discovered the Epson."

When you're done answering the questions, it displays the finished graph. You smirk.



Hit the 'Schedule' key and up comes today's electronic appointment calendar, ready for you to check your meeting schedule, make appointments, jot down notes, or update your things-to-do list.

Word processing?
The Epson's special HASCI™ key-



board is designed just like an electric typewriter, so everything's where you expect it to be. On-screen instructions lead you easily through the editing process. There's even a "Help" button to bail you out if you get in trouble. Best of all, if you do manage to make a mistake, you simply push "Undo" to back up a step and start over.

In less than a day, I was banging out error-free letters and perfect reports. All of which I was filing electronically.

**ELECTRONIC FILING, ALONE,
MAKES THE EPSON WORTH
ITS WEIGHT IN GOLD.**

When I finish writing something, I touch "Store." My Epson asks me what I'd like to call the document, then lets me file it away by using up to 16 words.

dBase II® is a trademark of Ashton-Tate.
Microsoft® is a trademark of Microsoft Corp.

I could, for instance, file a letter under the title "Letter to Bob Goldman thanking him for recommending the Epson and inviting him to dinner Saturday."

The letter can then be instantly retrieved by telling the Epson to look for "Letter to Bob Goldman," or just "Bob," or even "Saturday dinner." It automatically searches through a vast electronic file drawer to find the letter — using whatever slight bit of information I can remember.

Very slick. Very useful. And nothing like the cumbersome file and retrieve codes demanded by other computers.

In fact, the Epson is so easy to use and undemanding that it's hard to believe that you're on the leading edge of technology.

Yet that's exactly where I find myself. In one day, I was tearing through my work — while guys who've had computers for months (even years) were still tearing through their instruction manuals.

In one day, I was doing more work, faster, and *better* than I ever thought possible.

In one day, this low technology man had caught up with the computer age.

Bobby... Epson... it's a nice age. I thank you both."

Naturally, the Epson is expandable to whatever degree of complexity you choose, and accepts a full line of CP/M® software. This means that for a base price of less than \$3000, you get all of Epson's integrated software, plus, the capability to choose from literally hundreds of popular programs, including Wordstar®, Peachcalc®, Microplan® and dBase II®. Or, you can write your own, using Microsoft® BASIC, which is also included, free.

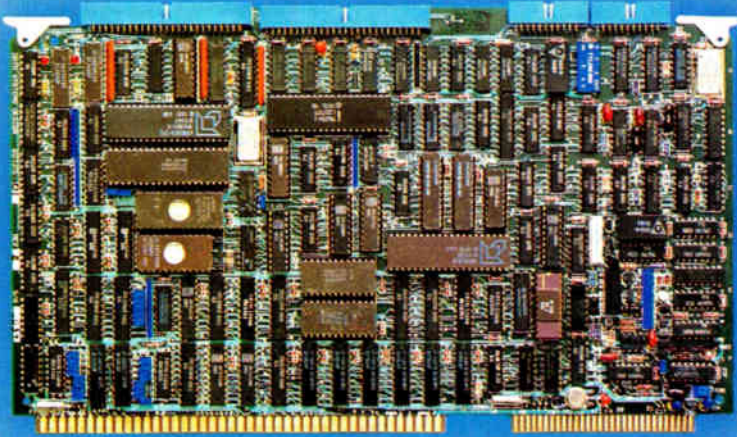
Epson also has a national service network that provides technical support, advice, and information. For a free brochure, or the name of your nearby Epson dealer, call toll-free (800) 421-5426. California residents call (213) 539-9140.



EPSON

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ONE SLOT SHOPPING.



INTRODUCING THE WINCHESTER/FLOPPY/TAPE THREE-IN-ONE MULTIBUS CONTROLLER.

Try this on for size.

DSD's new 7215 single-board Multibus® controller/interface handles two SA1000-type 40Mb Winchester, a 1/4" streamer, and two 8" floppies.

Plus on-board data separation, 32-bit ECC, and self-diagnostics. All on the same board.

There's also a version for 5 1/4" drives, the 5215, with similar capabilities.

And both are very, very quick.

Thanks to a pipelined architecture that moves data at non-interleaved speeds.

Top-of-the-line performance.

The 7215 and 5215 are the highest performance controllers on the market for 8" and 5 1/4" drives.

And that makes them ideal for multiuser and UNIX™ applications.

They also emulate Intel® iSBC® 215 and iSBX™ 218 controllers so you can run RMX 86 anytime.

And with 24-bit addressing support, you can take advantage of high performance microprocessors like the 68000 and the new inexpensive memory chips to address larger physical RAM memory.

To tune system performance, both boards offer four alternatives for bus arbitration. As well as having the capability to boost system performance by performing overlapped seeks and multisector operations.

Plus the convenience to match.

The best part about all this performance is that it comes on one board. So it only takes up one back-plane slot. And there are no extra boards to fool with.

As easy as that sounds, there are those of you who'd rather not do-it-yourself. For you, the 7215 controller is also available in our 770 storage systems.

And like all DSD products, our Multibus boards and systems are supported by our exclusive Rapid Module Exchange™ and regional service centers.

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New products

Communications

Modems act like peripherals

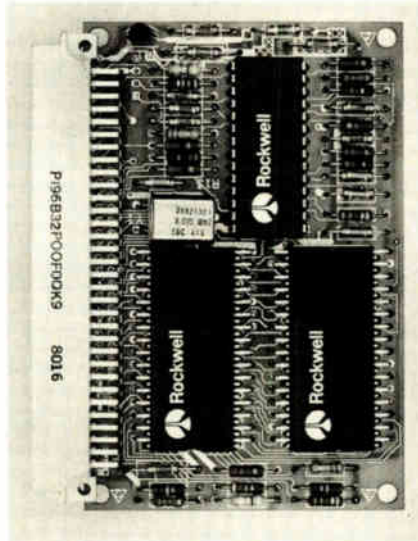
LSI-based modems are designed to link to microprocessor bus, offer error rate of 1 in 10^6

A family of highly integrated 1,200-, 2,400-, and 9,600-baud card-level modems designed to be addressed as microcomputer peripherals is aimed at several lucrative market segments. The models in the line cost as little as \$250 (in quantity) for 1,200-baud full-duplex units.

The 9,600-baud model R96FAX (see photo) is intended to maintain the position of Rockwell International's Semiconductor Products division—formerly the Electronic Devices division—as a supplier to manufacturers of facsimile equipment, especially in Japan. Housed on a 100-by-65-mm board and requiring only 2 w of 5- and 12-v dc power, it is smaller than earlier models and also sells for less—\$310 in production quantities.

The full-duplex 1,200- and 2,400-baud modems could ultimately grab most attention, say division officials. Both are intended for personal computers, which are expected to become the largest single market for modems. The 1,200-baud model R1212 and 2,400-baud R2424 both have automatic-originate and -answer features. Designed for remote and central-site computer applications, they are available with circuitry for direct connection to phone lines.

The modem family derives from Rockwell-designed very large-scale integrated circuits: two basic signal-processing devices with memory capacities that vary with performance. They might eliminate up to \$50 of components previously required to implement modems. More important, these chips boost the modems into full-fledged computer peripherals, with control data transferred over the microcomputer bus, explains



Dennis E. Kaliher, general manager for telecommunication products.

"Designing a modem into equipment becomes a programming job, which should aid those with little experience in data communications," he says. The modem interfaces with the bus, and control software can be developed with design aids used for the microcomputer itself.

The modems employ what the firm calls adaptive and fixed-compromise equalizer techniques to ensure accurate transmission over even unconditioned telephone lines. These techniques involve continuous monitoring of transmitted signals and compensation for shifts in amplitude response and group delays. Rockwell specifies error rates below 1 bit in 10^6 over long-distance lines.

Try again. Built-in diagnostics allow the computer to test the modems under local and remote loopback conditions. If line quality causes errors, the data can be retransmitted under computer control at whatever rates are necessary, says the firm.

Each modem requires 3.2 w at most and meets applicable U. S. and international communications standards, with software-selectable formats. Depending on speed, these include V.29, V.27 bis and ter, T.30, V.22 bis, Bell 208, Bell 212A, and Bell 103. The R96FAX, for example, satisfies V.29, V.27, and T.30 (which provides for a secondary 300-baud channel). The 1,200- and 2,400-baud

modems meet V.22, Bell 212A, and Bell 103 standards. In addition, the R2424 handles V.22 bis transmission. For self-contained-modem applications, any modem in the family can be ordered with an RS-232-C interface instead of the direct interface with the microprocessor bus.

Samples of the modems are currently being made available, with full production scheduled for winter. All members of the line are hardware- and plug-compatible, on printed-circuit cards no larger than 100 by 160 mm. (The 9,600-baud facsimile unit is smaller, though.)

In quantity, the R96FAX costs \$310, the R1212 \$250, and the R2424 \$325. The other modems in the family include models R96DP (\$495) and R48DP (\$310), which are 9,600- and 4,800-baud "data pumps" for boxed modems or multiplexers, and the R96FT, a fast-train unit for multipoint systems.

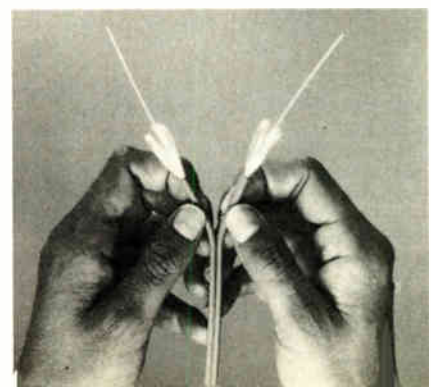
Rockwell assembles its modems in an automated plant at El Paso, Texas. Japanese facsimile-equipment manufacturers report acceptance rates approaching 99.6%, according to the firm. The figure given for mean time between failures is 200,000 hours, or 23 years of continuous operation.

Rockwell Semiconductor Products Division, P. O. Box C, Mail Code 501-300 (4311 Jamboree Rd.), Newport Beach, Calif. 92660. Phone (714) 833-4700 [Circle reader service number 401]

Duplex fiber-optic cable

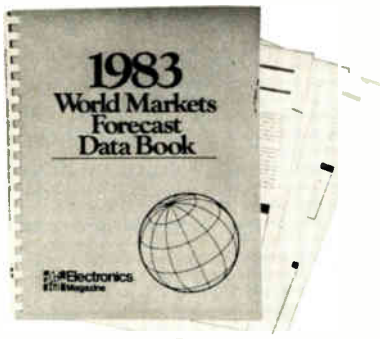
zips apart to ease termination

Flexibility in siting fiber terminations and improved operating performance are claimed for a tightly buffered, zippable duplex fiber-optic cable, whose design allows users to split it and to distribute its individual chan-



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New products

nels to different points at termination sites. It operates over a temperature range of -20° to $+65^{\circ}\text{C}$, with bandwidths as high as 600 MHz/km at 850 nm and with an attenuation of 3 dB/km at the same wavelength.

The zippable duplex cable consists of two buffered fibers with a 900- μm nylon skincoat. Kevlar is helically stranded around each fiber to protect it and provide high tensile strength, and the combination is surrounded with an outer flame-retardant polyurethane cable jacket that can easily be removed for termination. For easy channel separation, the cable's two tightly buffered, jacketed fibers lie parallel in a zip-cord configuration.

Available in four to six weeks, the cable sells for about \$2 a meter.

Valtec, 99 Hartwell St., West Boylston, Mass. 01583. Phone (617) 835-6082 [Circle 403]

Controller links IDX-3000 net with asynchronous networks

A stand-alone control unit for the DECsystem-20-based IDX-3000 local data-network system opens up asynchronous networks to the IDX-3000. The IDX-3000 system upgrades the traditional data switch, using only twisted pair wiring and T1-based architecture so as to economically serve distributed environments up to 4.5 square miles in area.

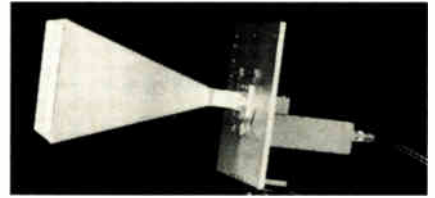
The unit's Bell DS-1 data format sets up a direct interface with microwave, fiber-optic, and satellite technologies. The IDX-3000 is a non-blocking system that supports up to 3,027 19.2-kb/s asynchronous ports.

Pricing for the IDX-3000, which can be delivered next month, was unavailable.

M/A-Com Linkabit Inc., 3033 Science Park Rd., San Diego, Calif. 92121. Phone (619) 457-2340 [Circle 406]

Pyramidal horn antenna serves C-band receive-only TV

No. 4377, a pyramidal horn gain-calibrated antenna that serves television's receive-only C-frequency band



(3.7 to 4.2 GHz), was designed as an interference survey tool. An accessory mounting bracket allows the horn to be set at any polarization on a standard camera tripod.

The horn, which has the same beam width (28°) in vertical and horizontal polarization, is sealed at the aperture with a thin glass-fiber sheet and terminates in a rectangular CPR229 waveguide flange. Its aperture is $8\frac{1}{2}$ by 11 in., and its length and width are 12 and 2.5 in., respectively. The antenna has an etched calibration plate that gives the effective gain at five frequencies.

The horn and mount sell for \$350 and \$275 each, respectively, and are available in three weeks.

Microwave Filter Co., 6743 Kinne St., E. Syracuse, N. Y. 13057. Phone (800) 448-1666

[Circle 405]

Unit secures 112-kb/s data over point-to-point circuits

The Datacryptor III, designed to prevent unauthorized access to computer information during transmission, secures data over point-to-point wideband circuits at data rates of up to 112 kb/s. Operating synchronously on full-duplex, leased-line facilities, it is equipped both with V.35 and with RS-232-C interfaces.

Key management and diagnostics can be controlled from the unit's front panel, and remote diagnostics can be performed unattended. Key transfers are made easier by the use of public key management.

The Datacryptor III uses the Data Encryption Standard in the single-bit cipher feedback mode, which provides complete protocol transparency. Available next month, the Datacryptor III will sell for \$4,995.

Racal-Milgo, 8600 N. W. 41st St., Miami, Fla. 33166. Phone (305) 592-8600 [Circle 404]

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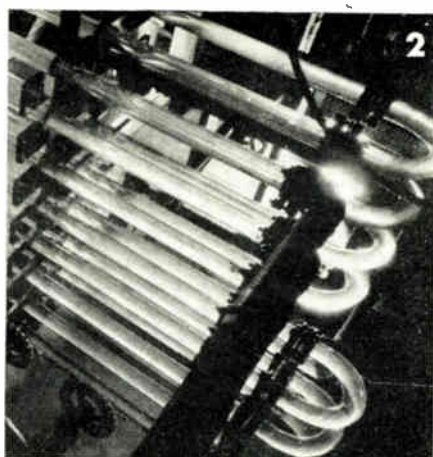
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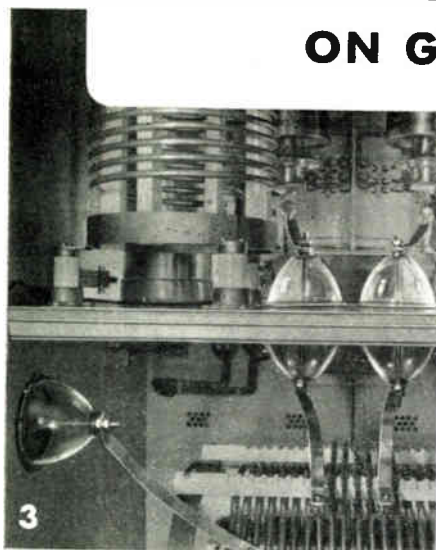
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Low dielectric constant	6	3	5	4	1
High volume resistivity	5	4	3	2	1
Total point score	28	18	17	11	10

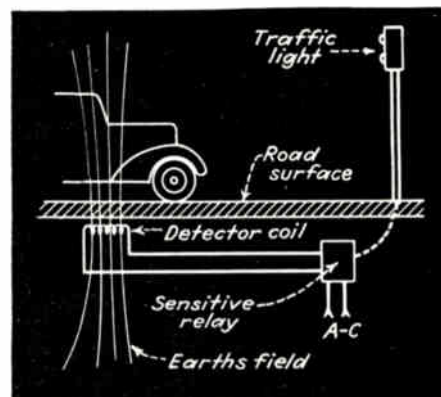
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Vehicle-Operated Traffic Light

TRAFFIC LIGHTS MAY be caused to operate at the approach of a car by the method shown. An induction or detector coil is installed beneath the road surface over which cars approaching the light must pass. Current is induced in the coil by the earth's magnetic field and the sensitive relay connected to the coil is adjusted to remain inoperative when this normal current is present. When



Distortion of the earth's magnetic field by an approaching car may be made to alter current flowing in a coil sufficiently to actuate a relay

a car passes over the road surface beneath which the coil has been installed the earth's magnetic field is distorted sufficiently to alter the amount of current flowing in the coil, tripping the relay and supplying power to the light.—Lamb, ELECTRONICS, December, 1940, p. 35.

Lumber Moisture Content Checker

THE CONVENTIONAL electric method of checking the moisture content of lumber is to use a sensitive ohmmeter, inserting test needles deeply into the wood some standard distance apart and comparing the d-c resistance reading with that of lumber known to be dry. An instrument made by the Moisture Register Company of Los Angeles dispenses with the test needles by utilizing the high-frequency field of a 12 Mc oscillator, as shown in the drawing on page 122.

An electrode forming part of the oscillator circuit is brought into intimate contact with the lumber to be tested. Power absorbed from the oscillator by the lumber causes a

First "Graphics Ready" monolithic raster scan DAC.

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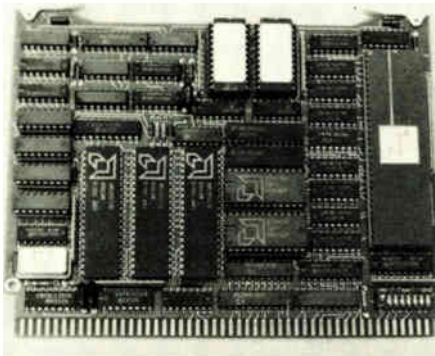
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LSI Products Division
TRW Electronic Components Group

Microcomputers & systems**FFT card fits in desktop system**

Small board performs integer fast Fourier transforms using C-MOS multiplier-accumulator IC

A single-board array processor helps Hewlett-Packard's 9826 and 9836 computers—desktop machines al-



ready well-entrenched in the scientific and engineering communities—take on more demanding tasks. The FFT-523, which fits in the space of a single series 200 board, calculates fast Fourier transforms, inverse FFTs, power spectral-density curves, and Hamming-window operations.

The FFT-523 can equip a 9826 or 9836 for computational tasks in geophysics, sonar analysis, data reduction, general spectrum analysis, speech research, and phase-response work. Original-equipment manufacturers also can use it to build such specialized instruments as spectrum analyzers.

Operating on 16-bit integer data arrays of up to 1,024 complex points, the FFT-523 speeds up transforms by more than two orders of magnitude over software-based approaches: a 1,024-point FFT takes just 9.2 ms. Thanks to complementary-MOS large-scale integrated circuitry, the processor attains this performance level with a power consumption of only 10 W. So low is the power drain that

throughput can be raised still further with two or more FFT-523s installed in a single host.

The heart of the FFT-523 is Analog Device's C-MOS 16-by-16-bit multiplier-and-accumulator chip, and its random-access memory chips are also C-MOS parts. HP 200-series boards are small, however. To fit the needed hardware on one card, the company had to create a six-layer circuit board and a design that closely couples the array processor with the HP processor and thus lowers the relatively high intelligence level required by array-processor cards that are meant to work with any microprocessor host. The array processor is memory-mapped into the host's address space.

The processor performs FFTs by executing a single program line in Basic, Pascal, or HPL. Disk-based machine-language device-driver routines come with the board. The company does not protect its software: customers receive the source code and are encouraged to modify it to suit their needs.

Optional algorithms. Standard programmable read-only memories house algorithms for calculating forward and inverse FFTs, power spectral density, and Hamming-window compensation. Kaiser, Bartlett, and Hanning algorithms come as options.

The board, priced at \$1,600 in single-unit quantities, will be available in about two months. The company is also working on a single-board array processor for the IBM Personal Computer and expects to introduce it in a few months.

Ariel Corp., 600 W. 116th St., New York, N. Y. 10027. Phone (212) 662-7324 [Circle reader service number 381]

68000-based board, software let IBM PC run Cobol

Carrying a 68000 microprocessor and supporting the Ryan-McFarland RM/COS operating system, Sritek Inc.'s processor card turns an IBM

Personal Computer or XT computer into a multiuser Cobol-oriented computer. The 68000 card provides the 8088-based machines with a powerful paged-memory-management unit to perform the address relocation and memory protection needed by sophisticated operating systems and business applications.

The board, available in 8- or 10-MHz versions, also increases system speed by using the 68000 for central processing and the 8088 as an input/output processor. As an I/O processor, the 8088 attends to such tasks as handling multiple terminals, disk I/O with disk/track caching, local networking, and remote-batch-communication protocols.

With the 256-K-byte memory add-on board, the RM/COS commercial operating system will support four users. Its Cobol software can execute the 400-plus RM/Cobol business packages available. The basic 68000 configuration with 256-K bytes of memory sells for \$2,495; with the additional 256-K bytes it goes for \$2,995. Boards are available now.

Sritek Inc., 10230 Brecksville Rd., Cleveland, Ohio 44141. Phone (216) 526-9433

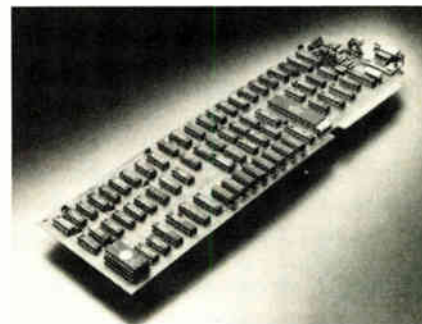
[Circle 383]

Ryan-McFarland Corp., 609 Deep Valley Dr., Rolling Hills Estates, Calif. 90274. Phone (213) 541-4828

[Circle 389]

Adapter card adds color graphics to personal computers

Fitting into a single expansion slot of an Eagle personal computer, Eagle 1600 series, or IBM Personal Computer, an adapter board provides graphics capabilities for a color or monochrome display. As many as 16



New products

foreground and 8 background colors are available in the color mode, which has a resolution of 320 by 200 picture elements.

In monochrome mode, resolution is 642 by 200 pixels. Reverse video, blinking, and highlighting features are available in the monochrome mode; in the color mode, character blinking is offered.

The adapter has two basic operational modes: alphanumeric and all-points-addressable (APA) graphics. The adapter board is tied to the monitor using either a composite video port, a direct-drive red-green-blue port, or an interface for driving a radio-frequency modulator supplied by the user.

Priced at \$295, the board is available immediately.

Eagle Computer Inc., 983 University Ave., Los Gatos, Calif. 95030. Phone (408) 395-5005 [Circle 384]

Kit allows designers to evaluate 16-bit processors

When connected to a terminal or host computer, the SAM-Z8003EVM evaluation kit provides a quick and inexpensive way to evaluate the latest 16-bit microprocessor technology. The evaluation module, built on a Multibus card, uses circuits like the Z8003 virtual-memory central processing unit and the Z8015 paged-memory-management unit.

The resident monitor program and control unit permit the control, inspection, and alteration of on- and off-board resources, including memory, input/output ports, virtual-memory processor and paged-MMU registers, breakpoint set and clear, run and single-step program execution, and time and date.

The evaluation module, including board, control unit, monitor program, and two serial RS-232-C connectors for terminal and host computer connections, is priced at \$2,500. It will be available for delivery starting next month.

SGS Semiconductor Corp., 1000 East Bell Rd., Phoenix, Ariz. 85022. Phone (602) 867-6100 [Circle 385]

68000-based computer board has 256-K bytes of RAM

A single-board computer built around a 68000 microprocessor and compatible with the VME bus packs up to 256-K bytes of random-access memory and 64-K bytes of programmable read-only memory or erasable PROM. The CPU 01 operates under the CPM-68K operating system, but Unix level 5 will be available in the second quarter of next year.

The board has three serial RS-232-C ports (one synchronous and two asynchronous) and a parallel port that consists of 23 input/output lines, 13 of which can be used with buffered outputs as a Centronics-compatible interface. The computer has one 8-bit timer, two universal 8-bit timer-counters, and one 24-bit timer-counter.

A variety of peripheral cards are available, including a floppy-disk controller that can run 3½-, 5¼-, or 8-in. drives. A lower-cost version of the card, the CPU 02, has 128-K bytes of RAM and just one serial port. Available now, the boards are priced from \$1,250 to \$1,950.

Dec-Tec Ltd., 2221 Jackson Circle, Carrollton, Texas 75006. Phone (214) 446-6765 [Circle 386]

\$2,745 desktop computer has 11-megabyte Winchester drive

Priced at just \$2,745, the Morrow MD11 desktop microcomputer offers 11 megabytes of Winchester disk storage, a 12-in. screen, 128-K bytes of random-access memory, a CP/M operating system, and five application packages. The MD11's single-board computer uses a Z80 microprocessor running at 4 MHz and carries 8-K bytes of read-only memory.

The machine also includes a 400-K-byte floppy-disk drive for backup, three standard RS-232-C serial ports, and a parallel port. One of the serial ports operates as an RS-432 high-speed port running at a 500-kb/s transfer rate or in bisynchronous,



Synchronous Data-Link Control or High-level Data-Link Control modes for compatibility with mainframes.

In addition to the CP/M operating system, software includes New Word word-processing package, LogiCalc financial spreadsheet, Correct-It spelling checker, Personal Pearl database manager, and the Quest Book-keeper system. The system will be available next month.

Morrow, 600 McCormick St., San Leandro, Calif. 94577. Phone (415) 430-1970 [Circle 388]

Small card holds computer with Tiny Basic interpreter

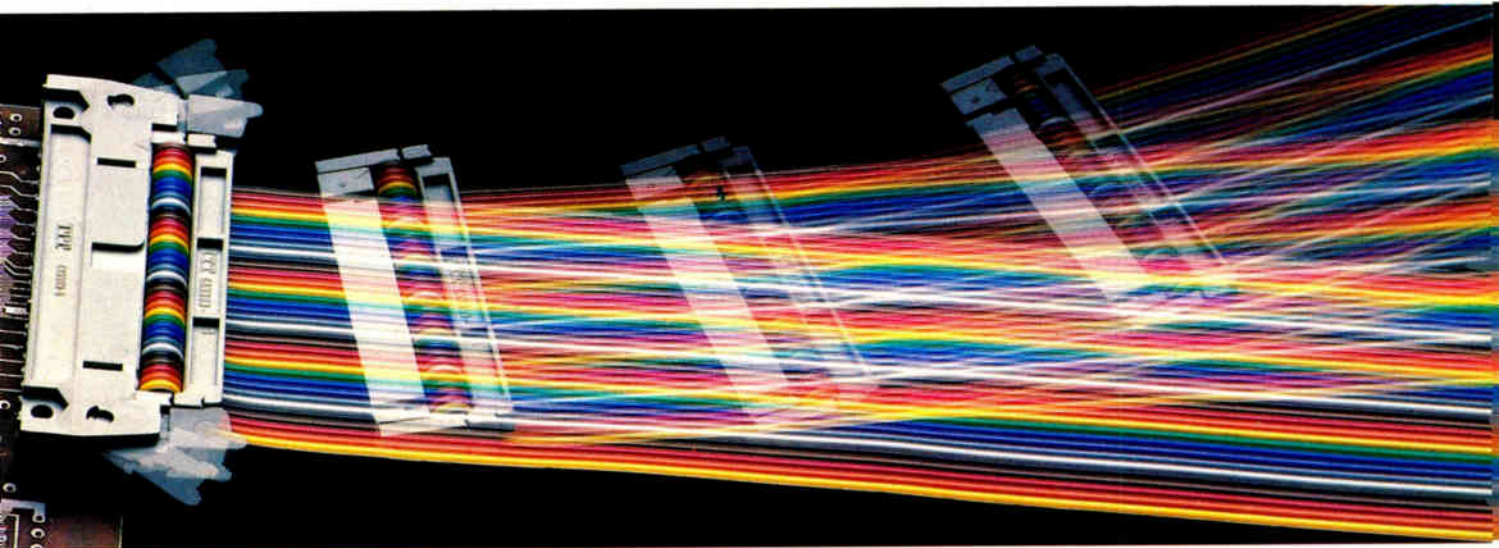
Built on a card that measures but 4 by 3.35 in. and mates to a 50-pin edge-card connector, the K-9000 tiny microcomputer has a Tiny Basic microinterpreter, 8-K bytes of battery-backed random-access memory, and 16-K bytes of erasable programmable read-only memory. Available in 4-, 8-, and 16-MHz versions, it can operate in a multiprocessor system of up to 90 cards.

The microcomputer's address, data, and control lines feature direct memory addressing, and its RS-232-C port offers handshaking.

Available for use with the microcomputer are a 32-K-byte memory card that has 16-K bytes each of battery-backed RAM and E-PROM; a communications card with cassette tape interface; a real-time clock card; a color-video generator; and an analog-to-digital converter card.

The microcomputer is available from stock and sells for \$195 each. Transwave Corp., Cedar Valley, P. O. Box 489, Vanderbilt, Pa., 15486. Phone (412) 628-6370 [Circle 387]

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Introducing the new G80 IDCs from ITT Cannon.

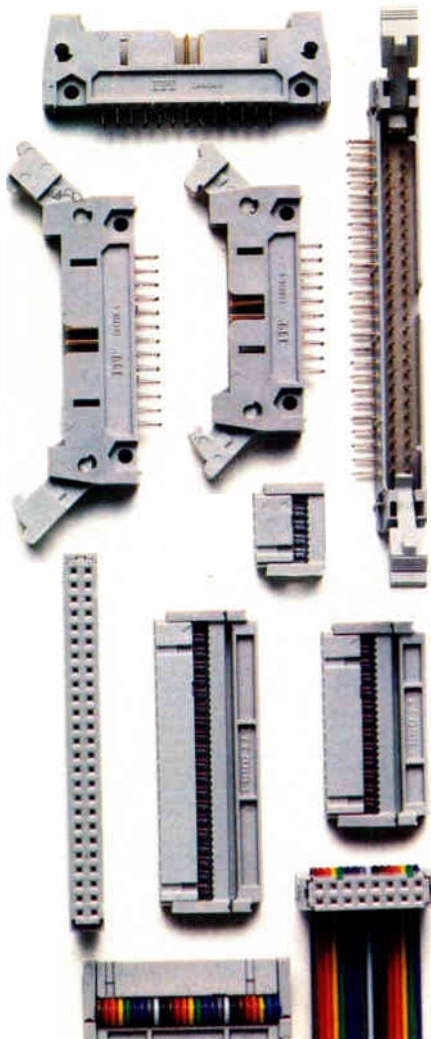
header terminations (straight and 90°).

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Now there's a connector that snaps to it. The new G80 IDC from ITT Cannon.

The G80s meet all MIL-C-83503 requirements and are interchangeable and intermateable with other MIL-C-83503 connectors. They feature integral polarization facilities that eliminate the need for user-installed polarizing keys. And their double-deep cavity improves connector retention.

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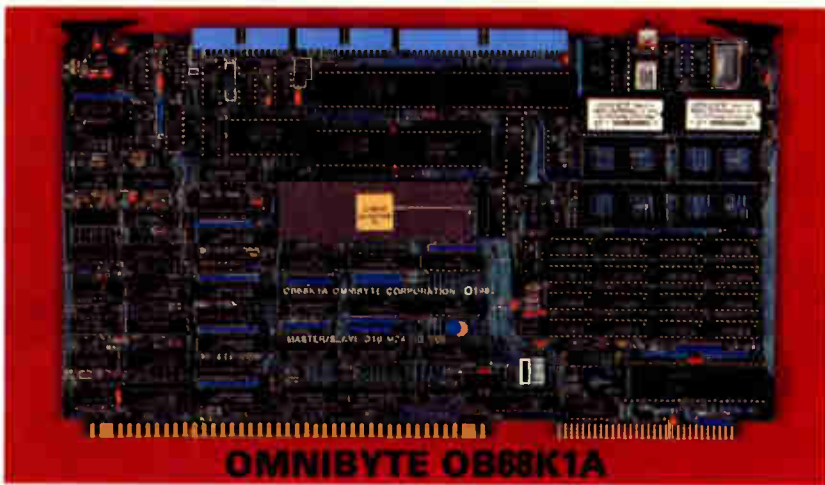
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OMNIBYTE OB68K1A

MC68000 CPU on the IEEE-796 (MULTIBUS)*

If your next project requires flexibility, reliability, and performance, OMNIBYTE has the solution. The OB68K1A is a high performance single board computer designed as a direct replacement for our OB68K1. Enhancements include a 10MHz MC68000 CPU, hardware ram refresh circuit with zero-wait-state operation, 32K or 128K-bytes of ram (512K-bytes in fourth qtr., 83), up to 192K-bytes of EPROM, and a low noise multi-layered design. Other features include (2) RS232C serial ports, crystal controlled baud rate

generator (50-19.2K), (2) 16-bit parallel ports, a triple 16-bit timer/counter, and 24 address lines for directly addressing up to 16M-bytes.

A variety of software packages are available for the OB68K1A. They range from the optional MACSBUG monitor/debugger to Realtime Executives and Target Operating Systems in silicon. Four commercial software manufacturers have complete operating systems, including development tools and high level languages.

FEATURES:

- ★ 10MHz MC68000 16/32 BIT CPU
- ★ 32K/128K/512K-bytes of dual ported RAM
- ★ Zero wait state RAM access
- ★ Up to 192K-bytes of EPROM
- ★ (2) RS232C serial ports
- ★ (2) 16-BIT parallel ports
- ★ A triple 16-BIT timer/counter
- ★ (7) prioritized-vectored interrupts
- ★ Switch selectable memory mapping
- ★ Software/hardware selectable baud rate generator
- ★ Directly addresses 16M-bytes
- ★ Multibus/IEEE 796 BUS compatible
- ★ A (2) year limited warranty

FOR MORE INFORMATION ABOUT THE OB68K1A, ASK FOR OUR FREE SUMMARY SHEET OR SEND \$10 FOR A TECHNICAL MANUAL.

CONTACT: SUE COCHRAN
Sales Manager



OMNIBYTE CORPORATION

245 W. Roosevelt Rd.
West Chicago, IL 60185
(312) 231-6880

Intl. Telex: 210070 MAGEX UR

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MULTIBUS is a trademark of Intel Corporation
MACSBUG* and MC68000 are trademarks of Motorola, Inc.

Circle 186 on reader service card

COLOR GRAPHICS BOARDS



MATROX GXB-1000 - The complete color graphics solution.

The GXB-1000 is a complete color graphics display system implemented on two Multibus boards. The system executes a display file containing high level graphics commands, generated by the user's host CPU. The GXB-1000 includes all the necessary hardware and software to draw lines, polygons, circles, characters, etc.

The unmatched performance and low cost of GXB-1000 make it the perfect solution for OEM color graphic displays. Additionally, Matrox can provide RGB monitors, CPU boards, memory boards, cardcages and keyboards for complete display system requirements.

Multibus - TM Intel, *QTY 100

1024 X 1024

DISPLAY RESOLUTION: 1024 x 768 pixels non-interlaced at 60Hz or up to 1600 x 1200 pixels interlaced at 30Hz

READ/WRITE AREA: 1024 x 1024 x 4 bits/pixel expandable to 1024 x 1024 x 16 or 2048 x 2048 x 4

SPEED: Four on-board processors draw graphics primitives at 50 to 600 nsec/pixel

COLOR: 16 display colors from a palette of 256

SOFTWARE: On-board 16 bit CPU with resident graphics software interprets over 256 commands

MODULARITY: GXB-1000 is fully Multibus compatible (IEEE-796), and requires only +5V

PRICE: \$3225.00 complete*



matrox
electronic systems ltd.

US & CANADA
5800 Andover ave. T.M.R. Québec Canada H4T 1H4
Tel. (514) 735-1182 Telex 05-825651

EUROPE
Herengracht 22, 4924 BH Drimmelen, Holland
Tel. 01626-3850 Telex 74341 MATRX NL

Components

**Display drivers
switch 80 V**

10-, 20-, and 32-bit drivers
for vacuum fluorescent displays
combine C-MOS, bipolar devices

Three serial-input latched drivers—the UCN-5810A, the -5812A, and the -5818A—are the first of a family of high-speed devices designed for vacuum fluorescent displays. The monolithic devices operate at 5-MHz clock rates (at 5 V) and switch 60 V at 40 mA per drive line. The drivers incorporate, respectively, 10-, 20-, and 32-bit complementary-MOS registers and a bipolar output device for each bit in them.

The drivers are the first of the Bi-MOS-II family, expected to include 16 drivers eventually. Ray Dewey, technical-information coordinator, says that "there are other drivers running at similar clock rates but not at these high voltages and currents."

The units interface directly with a microprocessor's input/output port, accepting data inputs of 5 to 15 V at 1 μ A, performing serial-to-parallel conversion, and controlling the power devices that switch the higher voltages and current levels required to drive vacuum fluorescent displays. At input levels from 10 to 12 V, clock speeds can be higher—10 to 15 MHz. For users who require higher-voltage outputs, selected devices (with a suffix of 1) have maximum ratings of 80 V.

Cascadable. Data is loaded serially into the 10-, 20-, or 32-bit C-MOS shift registers, and the parallel register outputs address the corresponding number of display elements. The drivers can be cascaded, so (among other possible combinations) two 32-bit 5818As can be used to address up to 64 elements.

The UCN-5810A comes in a standard 18-pin dual in-line plastic package. The -5812A and -5818A are supplied in 28- and 40-pin DIPs, re-

spectively, with pin rows on 15.24-mm centers.

In quantities of 100, the 5810A costs \$1.61, the 5812A \$2.81, and the 5818A \$4.78. As for the 80-V drivers, the 5810A-1 costs \$1.77, the 5812A-1 \$3.08, and the 5818A-1 \$5.25. Production quantities are available for delivery now.

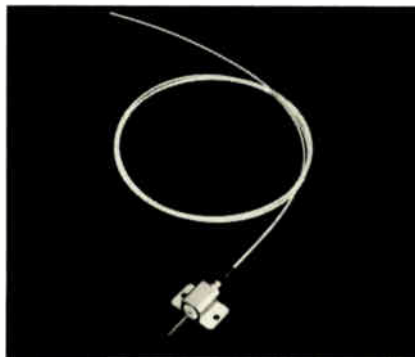
Sprague Electric Co., Semiconductor Division, 115 Northeast Cutoff, Worcester, Mass. 01606. Phone (617) 853-5000 [Circle reader service number 341]

**Ge avalanche photodiode
boasts 60% quantum efficiency**

A germanium avalanche photodiode, the model FDP13R12JT, uses the popular 100- μ m-diameter photosensitive chip, while the lens system that couples the fiber pigtail to the diode is said to provide at least 60% effective quantum efficiency. The unit's typical cutoff frequency, at 1,300-nm wavelengths, is above 700 MHz, and its dark current is typically 0.3 μ A at 90% of breakdown voltage (said to be about 30 V). Operable at case temperatures ranging from -40° to +70°C, the photodiode has a forward current of 100 mA and a reverse current of 200 μ A.

Typical applications include fiber-optic receivers, test equipment, and—thanks to the 1,300-nm wavelength—long-distance repeaters. The photodiode costs less than \$600 in small quantities and can be delivered in 8 to 10 weeks.

Fujitsu Microelectronics, Microwave and Optoelectronics Division, 3080 Oakmead Village Dr., Santa Clara, Calif. 95051. Phone (408) 980-8585



**Single-chip CRT controller
needs clock signal, RAM only**

A single-chip cathode-ray-tube display controller, the NCR 7250, can be mask-programmed to provide many special features and display modes. It needs only an input clock signal and a single random-access memory to produce a video-display output from digital input.

Mixed character and graphics modes, including mosaic and line graphics, are standard features. Nine externally addressed internal registers control all display features, such as page scrolling, complete cursor-position control, and eight different screen attributes, including blank screen, reverse video, video chop, and cursor enable. The unit also has such field attributes as reverse video, blink, blank, video highlight graphics, and underline. The controller, with a character-cell size of 9 by 12 picture elements, can be used to display up to 80 characters on 25 lines.

In lots of 100, the 7250 sells for \$18.80. Samples and production quantities should be available now.

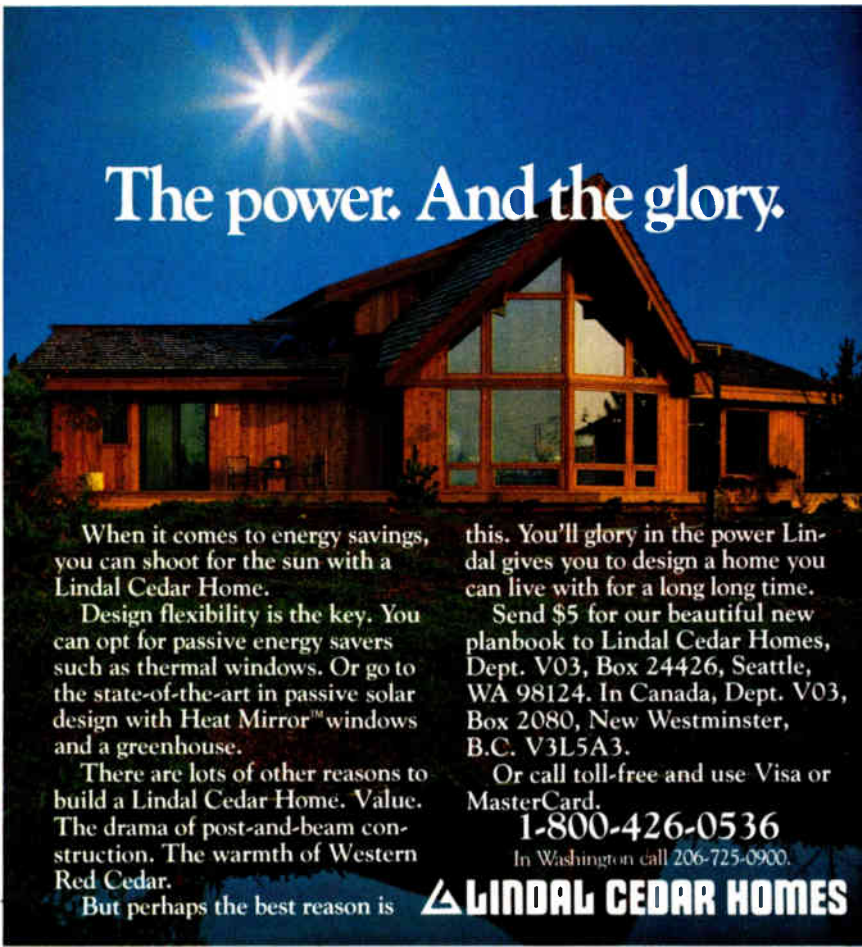
NCR Microelectronics Division, Product Marketing, 1635 Aero Plaza Dr., Colorado Springs, Colo. 80916. Phone (303) 596-5612 [Circle 343]

**Dual preamplifier for audio
boasts 0.7- μ V noise level**

A dual preamplifier chip with a total input noise of less than 0.7 μ V is designed for applications that require very low noise, like stereo cassette players and other high-quality audio systems. The low noise level comes from input transistors that are sized to be equivalent to 20 transistors in parallel and reduce the base resistance to 70 Ω , the company reports.

Each channel of the TDA3420 comprises two independent amplifiers, the first with a fixed gain of 30 dB, the second an operational amplifier for audio applications. The chip has a 0.03% distortion rating, a 10-mA current consumption, and a typi-

The power. And the glory.



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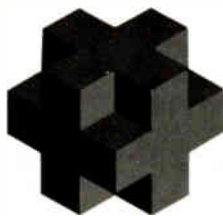
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188 Circle 242 on reader service card

New products

cal signal-to-noise ratio of 70 dB.

Available now in a 16-pin plastic dual in-line package, the TDA3420 costs \$2.25 each in lots of 100.

SGS Semiconductor Corp., 1000 East Bell Rd., Phoenix, Ariz. 85022. Phone (602) 867-6100 [Circle 345]

Low-noise toroidal transformers suit high-resolution displays

Thanks to special winding techniques, copper interwinding screens, and grounded metal cases, series 40 toroidal transformers have a radiated-noise figure about 8 times lower than conventional laminated transformers do. The units eliminate the air gap, and thus the fringing flux, because the toroid is a continuous strip of grain-oriented silicon steel.

These transformers can therefore be used to eliminate fatiguing picture jitter and line swim in high-resolution video-display units. Avel-Lindberg claims that a custom toroid could prove less expensive and easier to fit than retrofitting a metal casing around a conventional laminated transformer.

Available from stock, the series 40 includes 15-, 30-, 50-, 90-, and 130-VA models. Pricing in lots of 100 ranges from \$18.87 to \$30.37.

Avel-Lindberg Inc., Peacock Alley 116, 1 Padanaram Rd., Danbury, Conn. 06810. Phone (203) 797-8698 [Circle 347]



Electronics/October 20, 1983

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The Model 50 is a fully automatic Numbering Head sturdily built to last and perform. Consecutive character wheels advance after each impression. Wheels and index plates are fabricated from one piece to insure accurate and trouble free operation. The standard Model 50 is available with from 4 to 12 wheels, character sizes from 1/32" to 3/8"; and sharp, flat and round face characters. Options include air-tripping mechanisms and hot stamping capabilities as well as totally custom designs to meet your marking needs. Write or call

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Circle 243 on reader service card

THE WESTON SOLUTION

**10³
x5
49¢**
EACH

When you need to solve those tough budget questions, the Weston 830 trimmer gives you the answers. This high quality 3/4" rectangular trimmer now costs only 49¢ when purchased in quantities of 5,000.

And talk about value, the 830 stacks up with 12 turns of adjustability, a 3/4 watt power rating at 70°C with a maximum operating temperature of 125°C and having a standard resistance range of 10 ohms to 2 megohm.

With specs like these, at a price like that, it's easy to see that 5,000 830's are 5,000 solutions.



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Schlumberger

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Circle 244 on reader service card
Circle 189 on reader service card →

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The Prince Hotel will be managed by The Peninsula Group. With a hundred year heritage of dedicated service to business and pleasure travellers in the Orient, we know how to make your trip live up to all your expectations.



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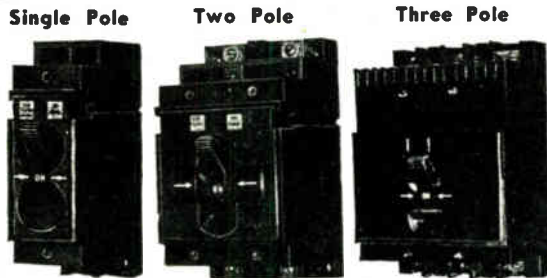
Reservations: Contact your travel agent, Cathay Pacific Air SRS (Steigenberger) Toll-free: 800-223-5652.

Hotels managed by The Peninsula Group: In Hong Kong: The Peninsula, The Discovery Bay Hotel (1985) In Harbour City: The Hongkong Hotel, The Marco Polo, The (January 1984) In Singapore: The Marco Polo In The Philippines: The Manila Peninsula In Thailand: The Bangkok Peninsula In The People's Republic of China: The Jiaquiao Hotel

3

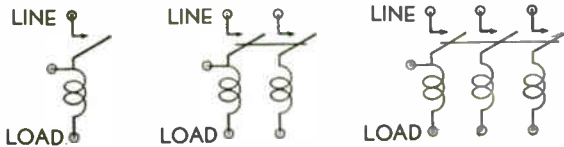
HEINEMANN "Re-Cirk-It" Fully Electro-Magnetic CIRCUIT BREAKERS

And



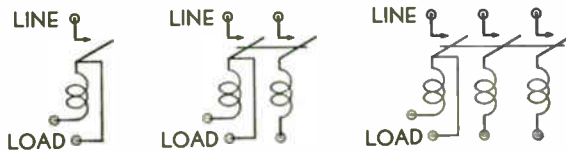
Here is what they do!

with
**CALIBRATING
TAP**



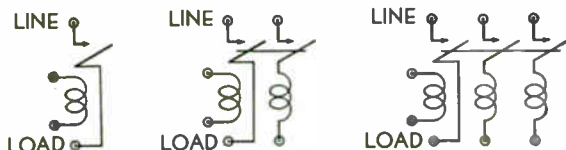
These "Re-Cirk-It" circuit breakers are assembled with an extra terminal attached to the load side of the interrupting mechanism which is the line side of the trip coil. This additional terminal can be used for an extra circuit not to have any effect on the trip coil; or it may be to provide means of connecting a rheostat or resistor in parallel with the trip coil to gain different fixed ratings; or an adjustable variation in the rating giving a much wider range in calibration of the tripping point.

with
**SHUNT
TRIP**



These "Re-Cirk-It" circuit breakers are assembled with the trip coil connected between an extra terminal and the load side of the interrupting means. The circuit connection from the line terminal through the contacts to the load terminal is solid without an overload coil, one end of the coil being connected to the load side of the contacts (interrupting means), the other end of the coil to the extra terminal. The use of this breaker is for remote control tripping so that a circuit of very low capacity at the same voltage may control the opening of the breaker.

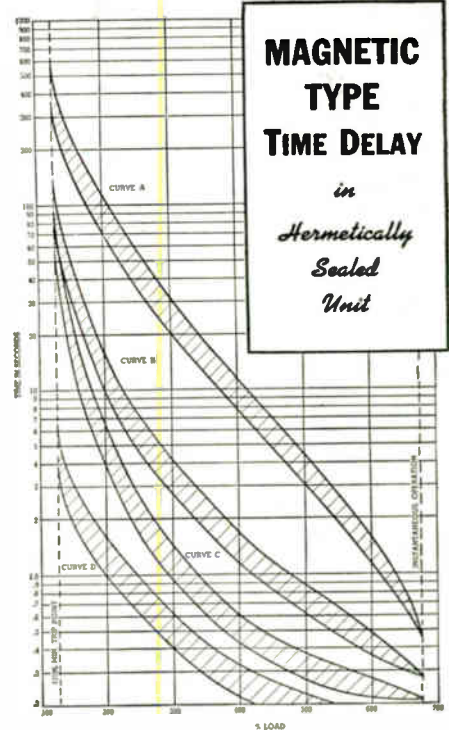
with
**RELAY
TRIP**



These "Re-Cirk-It" circuit breakers are assembled with the leads of the trip coil attached to separate terminals so that the interrupting mechanism (circuit opening means or contacts) may be in one circuit which is connected to the load and line terminals while the trip coil is connected to separate terminals and may be energized by a separate control circuit or may be used with the interrupting mechanism in the primary of a transformer and the coil in the secondary circuit. The trip coil can be arranged for as low as a few volts and up to several thousand.

Send for Catalog 40 with complete data.

TIME OVERLOAD CURVES



The time curves shown illustrate the wide range of adaptability of these breakers to various conditions. In other words, they can be assembled to meet specific requirements as to the time delay feature, since they are not dependent upon movement of thermostatic metal nor the heating of soft metal.

Curve "A" illustrates the standard time delay curve to which a standard time delay breaker will adhere. However, if so ordered, they may be had with other time curves. Curve "D," for instance, is the time curve of a breaker that would protect a load derived from gas filled lamps, and other circuits with similar characteristics, where the current returns to normal after about one cycle.

Curves "D" and "C" are also the ideal protection for small transformers since the breaker takes care of the relatively fast and high inrush of current during the first cycle when connected to the line.

If no time delay is desired, breakers can be had in instantaneous trip types. They will trip as soon as current rises to breaker rating.

HEINEMANN CIRCUIT BREAKER CO.,

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New products

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SMDs are ready for rough life

Ruggedized 48- and 84-megabyte disk drives are for mounting in trucks, boats, or oil rigs

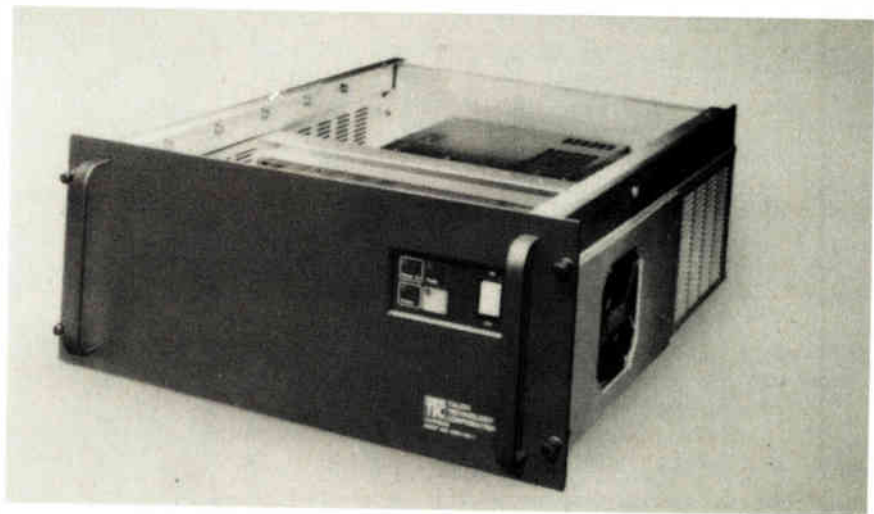
Intended for remote data storage in harsh, mobile applications, a new ruggedized hard-disk drive system from Talon Technology Corp. offers up to 84 megabytes of high-performance memory that will withstand a shock of 10 times gravity and vibration of 1 g during operation.

Using 8-in. storage module drives manufactured by Fujitsu Ltd., the company is offering two models of its series 2300 ruggedized SMD systems: the T2312 with 84 megabytes, and the 48-megabyte 2311. Both TuffDisk models offer track-to-track access times of 5 ms, average access times of 20 ms, and data-transfer rates of 1,229 kilobytes/s.

Talon Technology—founded late last year by former employees of Geophysical Services Inc., a petroleum-exploration subsidiary of Texas Instruments Inc.—is marketing these systems for remote computing applications in the military, oil drilling, and seismic realms, says Lynn B. Heitman, president.

"Obviously, this is not the kind of disk system you'd put in a computer room. Its packaging and shock protection is geared at mounting in trucks, ships, or offshore oil rigs," Heitman states.

Remote data-logging and computing applications these days call for amounts of on-site storage, and performance hard disks appear to be needed. However, these systems are generally sensitive to sudden shocks, since heads ride close to the disk surface. Positioning is critical to operation. The TuffDisk has shock-mounting and power supplies that are designed to withstand such movements. The systems are speci-



fied to have a mean time between failures of more than 10,000 hours.

The 84-megabyte TuffDisk will sell for \$15,000 in single quantities and \$7,500 each in 100-piece orders. Pricing for the 48-megabyte system is not yet available. Volume deliveries of both drives will begin in the first quarter of 1984.

The drives are housed in a standard 19-in. rack-mountable case with an 8.75-in.-high chassis. Included in the TuffDisk system are a factory-sealed disk drive, a power supply, a cooling fan, and a shock-and-vibration isolation system. Since field data-logging applications are often located in remote regions of the world with varying power supplies, the power supplies will accept 100-to-120- or 200-to-240-v power.

Density. Talon Technology says the 8-in. disk drives can offer their relatively high capacities thanks to a servo-controlled track-following technique that permits accurate head positioning at 720 tracks/in. Both models have 589 cylinders and store 20,480 bytes of unformatted data per track. The T2311 system has three disks and uses four tracks per cylinder; the T2312 has four disks and uses seven tracks per cylinder. A voice-coil rotary actuator employing a closed-loop servo system and a 3,600-rpm spindle motor result in the 1.2-megabyte/s transfer rate.

The TuffDisks have an operating temperature range of 5° to 40°C and a nonoperating range of -40° to +60°C. The average power con-

sumption of the drive is 126 w.

Talon Technology Corp., 1819 Firman Dr., Suite 137, Richardson, Texas 75081. Phone (214) 680-9913 [Circle reader service number 361]

Turnkey package adds speech to TI's Professional Computer

The TMS 320 digital signal processor is at the heart of a pair of products that give the Texas Instruments Professional Computer speech-recognition and -synthesis capabilities. A turnkey hardware-application package, Speech Command makes it possible to add speech as an input or output technique to existing designs incorporating the computer; a Speech Command Development Kit allows third-party designers to incorporate speech capabilities into software being developed.

The Speech Command package, which consists of two boards piggy-backed so they occupy only one expansion slot, accepts voice commands (as well as regular keyboard input) and allows the Professional Computer to deliver a vocal response. The software also offers telephone-management capabilities that allow the system to record incoming phone messages, dial numbers, deliver outgoing phone messages, and provide playback of recorded messages that can be actuated from a remote telephone.

A voice-coding feature, which con-

HOW STANDARD CELLS AND SILICON-LEVEL SIMULATION™ GUARANTEE THE PREDICTABILITY OF CIRCUIT PERFORMANCE.

Custom IC development has traditionally been a risky proposition. With the increasing complexity of VLSI devices, the challenge has never been greater.

In this report, third in a series, we'll explore the problems associated with commonly available CAD verification tools. And we'll explain how to eliminate custom development risk by using well-characterized standard cells and Silicon-Level Simulation techniques such as those employed by ZyMOS.

The Common Risk Of Common CAD Tools.

If you don't get working chips the first time out, you face higher-than-expected development costs and a protracted delivery schedule. And that can doom any design project.

Unfortunately, commonly used logic and circuit simulators offer no guarantee that your first prototypes will work. And you may not even get chips that meet specs on the second or third iteration. Let's explore why.

Commercially available logic simulators model "nominal" gate delay chip logic—not actual gate timing. Circuit simulators, such as SPICE, model the detailed transistor-level performance of small sub-circuit elements.



Design Automation

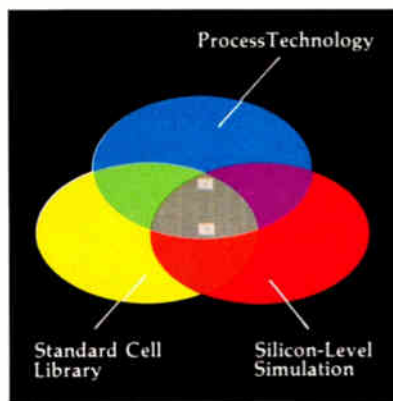
The design verification tools of the ZyP™ design system are well documented and easy to learn. ZyP design verification tools can be conveniently accessed in a number of ways including remote telephone connection.

The problem lies in poor integration of these commonly used design verification tools. Conventional logic simulators don't check actual gate delays, and circuit simulators check the detailed operation at the transistor-level of only a small portion of the overall circuit. Failure to identify and properly simulate a critical path in a complex circuit is all too easy. With conventional CAD verification tools, there's no guarantee you'll get working silicon.

The Guarantee of Silicon-Level Simulation.

To overcome the inherent risk in custom VLSI development, the logic functionality *and* timing of the entire circuit must be simulated concurrently. ZyMOS calls this Silicon-Level Simulation.

The key to Silicon-Level Simulation is a thoroughly characterized library of standard cells. Extensive transistor-level simulations—tied directly to actual wafer manufacturing data—are processed to create a linearized delay model for each cell.



Predictable Custom IC Design.

A predictable, low-risk custom IC program can be guaranteed only when the following three variables are tightly controlled, and integrated with one another: proven process technology; a thoroughly characterized, well-documented standard-cell library; and Silicon-Level Simulation using sophisticated CAD tools.

This delay model is then used in conjunction with a MOS-oriented, event-driven logic simulator, such as ZyMOS' proprietary ZyPSIM, to allow concurrent simulation of logic functionality and timing performance of the entire circuit.

With Silicon-Level Simulation, the integrated circuit manufacturer can guarantee delivery of circuits which match the predicted performance. This takes the risk out of custom VLSI development programs.

Moreover, since Silicon-Level Simulation provides both logic and timing information, it is possible to algorithmically create a production test program—ensuring there will be no delays in obtaining production quantities of the custom circuit.

We'd Like To Tell You More.

This report presents some key considerations in standard-cell chip design. Other reports are available upon request.

If your need is immediate, call or write us today. Ask about our 3½-day course that gets you ready to design your first custom chip. And ask for details on ZyPAWS (ZyP Automated Workstation), our turnkey workstation—complete with proprietary CAD software and standard-cell libraries.

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skimp by with no printer, no provision for document storage, and a maddeningly short battery life.

The Epson Notebook Computer has everything you need to get down to work. Exquisitely crafted into a sleek and silent package that you can take anywhere and use anywhere.

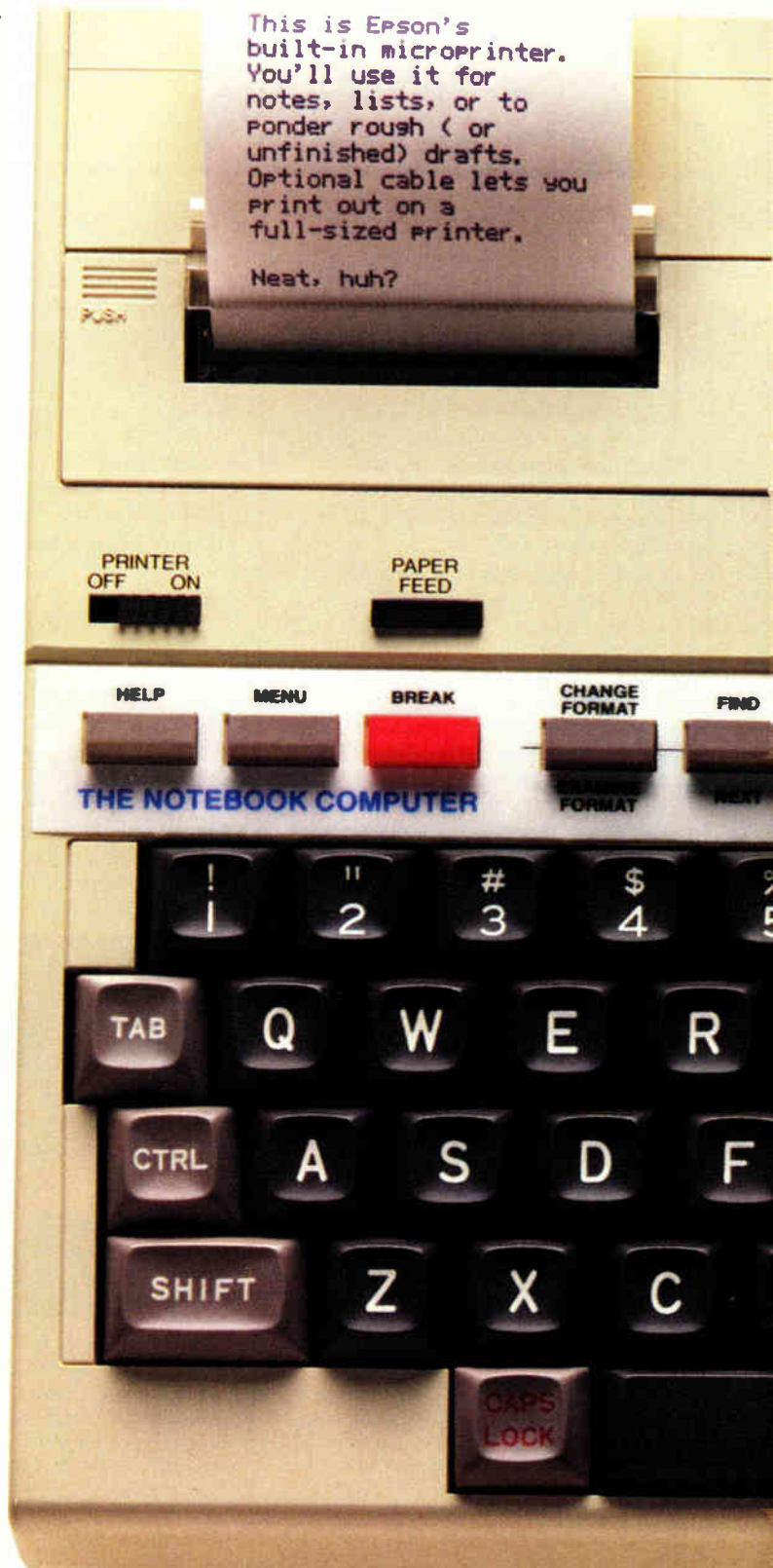
It weighs less than four pounds. Has a surface area the size of a sheet of typing paper. And it contains a whopping 16K of random memory (optionally expandable to 32K, if you need it).

You can program the Notebook Computer in a built-in, extended version of Microsoft® BASIC. An internal word processing program called SkiWriter® will have you turning out letters, notes, memos, or full reports after just fifteen minutes of reading the simple instructions.

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But be warned. Few who touch the "killer pigmy" go away empty-handed.



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actual size:

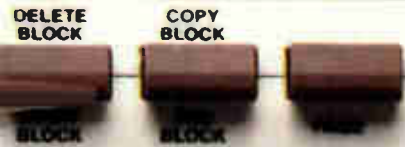
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When you test PCM primary multiplexes you need high accuracy, fast speed and more than a little flexibility.

Which are the exact qualities that put the Marconi Instruments 2830 PCM Multiplex Tester head and shoulders above the competition.

The 2830 is a simple to operate unit providing a wide range of test functions including frequency response, gain, linearity, quantizing distortion, idle channel noise and crosstalk.

When combined with Channel Access Switch 2831, the capabilities of the 2830 are extended to provide readings of impedance balance, return loss and signalling distortion.

The 2830 can handle four programmable automatic test sequences as determined by the user. They can even be repeatedly recycled.

Although intended for use as a stand-alone unit for A/A measurements (it needs no external

THE NEW MARCONI 2830 MULTIPLEX TESTER

controller) in either automatic or manual modes, the 2830 Multiplex Tester can also be used in conjunction with Marconi Channel Access Switches, Digital Simulators and Digital Analysers to provide a complete test set in D/A and A/D applications.

Other features include:

- * Automatic calibration function
- * Level measurement accuracy of ± 0.025 dB at 850 Hz from +20 to -60dBm. Speed approximately 2.5 readings per second.
- * Quantizing distortion measurement accuracy of ± 0.2 dB over 0 to 40 dB measurement range.
- * Results may be printed out under GPIB control.

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Circle 194 on reader service card

verts speech into digital values for storage and playback, uses a system that stores up to 16 min of speech on a standard 300-K-byte floppy disk.

The Speech Command package sells for \$2,600 and will be available next month. The Speech Command Development Kit, which includes a programmer's guide, the processing algorithms in object-code form, device service routines for the Speech Command hardware, and a library of runtime routines for high-level languages, will sell for \$8,000 plus product royalties.

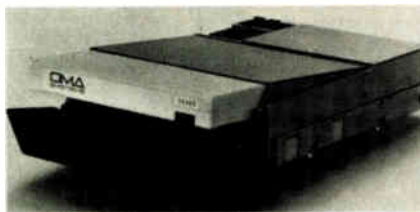
Texas Instruments Inc., Data Systems Group, P. O. Box 402430, H-678, Dallas, Texas 75240. Phone (800) 527-3500 [Circle 363]

Removable Winchester disk drives bow at \$500 each

DMA Systems Corp. hopes to make drives using removable Winchester-cartridge disks as popular as floppy-disk drives with its DMA 360, priced at \$500 in large quantities. The 5¼-in. half-height drive, which is compatible with the ST506 interface standard, stores 7.5 megabytes in each removable cartridge. The average access time is said to be 98 ms.

The safety features of the DMA 360 include a 30-s purge cycle and an extensive air-filtration system. As in the company's Micro-Magnum family of 5¼-in. removable-cartridge disk drives, the DMA 360 features fully retracted heads, which are dynamically loaded—that is, the head is loaded onto a spinning disk.

An on-board microprocessor permits the user to format a blank cartridge when it is inserted into the drive. This technique eliminates the need to write servo data on the disk surface prior to factory shipment and so cuts costs, the company claims. Samples of the drive, which is being



exhibited at next month's Comdex show, will be available in the first quarter of next year.

DMA Systems, 601 Pine Ave., Goleta, Calif. 93117. Phone (805) 683-3811 [Circle 364]

Smart interface supports different types of peripherals

Equipped with a microprocessor, memory, and input/output ports, the Dataserver is an intelligent peripheral interface that facilitates the integration of data-storage subsystems into high-performance multiuser computer systems. The Smart-T Dataserver is the first member of a family of intelligent interfaces being developed under the Priam Storage Architecture, a framework within which system manufacturers can develop system software without being constrained by the uniqueness of each device.

The Dataserver combines both high-level and low-level disk and tape functions to provide the host system with an integrated interface with Winchester and floppy disks and with streaming and start-stop tape drives. The system supports up to four Priam Winchester disk drives in any combination, and the auxiliary controller boards support streamer tapes with the QIC02 interface, as well as standard single- and double-density 8- and 5¼-in. floppy-disk drives. The data-transfer rate is 2.5 megabytes/s.

The Smart-T Dataserver is available now for \$875 in large quantities. Priam Corp., 20 West Montague Expressway, San Jose, Calif. 95134. Phone (408) 946-4600 [Circle 365]

3-in. cartridge disk drive uses 48 tracks per side

The MFD-80 3-in. cartridge disk drive is compatible with standard 5¼-in. floppy-disk drives and can store as much as 600-K bytes on double-sided, double-density disks. Unlike other 3-in. drives, however, the MFD-80 permits the use of all 48

tracks on each side of the disk.

Using the standard 40-track/side mode, the drives can store 500-K bytes per disk. Average track access time is 10 ms and settling time is specified at 15 ms. Average seek times are 245 ms in the 40-track/side mode, rising to 272 ms in the 48-track/side format.

The drive, which measures 3.54 by 1.58 in., including electronics, is small enough so that up to four drives may be placed vertically in a single 5¼-in. footprint. To be available in January of 1984, the MFD-80 will sell for \$125 each in original-equipment-manufacturer quantities. A version without the electronics will also be available.

Janome Ltd., 3533 Old Conejo Rd., No. 124, Newbury Park, Calif. 91320. Phone (805) 498-3512 [circle 367]

3¼-in. medium sits in flexible jacket; metal hub adds stability

Believing that only now is the market ready to choose a microflop-disk-drive standard, Dysan Corp. is



introducing its microflop medium: a 3¼-in. disk housed in a soft flexible jacket and compatible with 5¼-in. disks. A metal hub improves the stability and performance of the disk, which has a capacity of up to 1 megabyte.

In addition, the data-storage medium is designed to the same media-coating standard that the company uses on its 1.6- and 3.3-megabyte 5¼-in. disks and is produced using patented coating and burnishing processes and a special lubricant called DY10. Priced at \$21.50 per box of five, the disks are available now.

Dysan Corp., 5201 Patrick Henry Dr., Santa Clara, Calif. 95050. Phone (408) 988-3472

[Circle 366]



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Software

**Tool models
bipolar devices**

Version of university-developed program helps engineer predict results of process modifications

Semiconductor designers and process-development engineers can use a growing library of software tools to model device structures and fabrication before a circuit is actually laid out and built. Technology Modeling Associates offers commercially supported versions of several such programs that have been developed at Stanford University.

The latest, Sedan-2, models the operation of bipolar devices by calculating such characteristics as current gain, sheet resistances, junction capacitances, and cutoff frequency, using as inputs impurity distributions that may be specified analytically or derived from the firm's other simulation programs.

The firm has generalized and restructured Sedan-2 and provided it with a graphics-output capability. Originally, the Sedan program was limited to npn transistors; Sedan-2, however, operates with pnp devices, too. The firm's version also provides more than 300 error messages to assist users.

Infinite plane. Technology Modeling Associates markets two MOS-device-simulation programs, Gemini and Cande, as well, and two process-simulation packages, Supra and Sedan-3 [*Electronics*, Jan. 13, p. 262]. The company describes Sedan-2 as a "one-dimensional" simulation program, since it assumes an infinite two-dimensional plane and calculates values vertically, laterally, or diagonally across the device.

The program provides an organized way of stepping bias conditions, regardless of the step size. Current, for example, may be calculated as a function of the base-emitter bias by stepping through a range of val-

ues or picking an arbitrary value.

Users of Sedan-2, says the firm, can calculate how to change a process for better isolation specifications and how to change a value like junction capacitance. They may alter inputs to process specifications to check their impact on device characteristics or even modify inputs to the firm's other simulation programs, like Suprem-3 or Supra, and look at the outputs in Sedan.

The software runs on DEC VAX or similar 32-bit computers and on IBM systems that use the CMS operating system. Priced at \$20,000, Sedan-2 is available now.

Technology Modeling Associates Inc., 445 Burgess Dr., Menlo Park, Calif. 94025. Phone (415) 327-6300 [Circle reader service number 391]

**Personal-computer software
integrates business tasks**

A package to be shown at Comdex expands on the notion of integrated software with a trio of programs for the IBM Personal Computer for data-base management, spreadsheets, graphics, and word processing. Besides the ability to exchange data between applications—a feature users now expect as a matter of course—the package cuts through the intimidation barrier often encountered by new users by offering three different levels that gradually expose users to the full capabilities of the software. A special "remember" feature saves a series of commands in a file for later re-execution.

The word-processing package can handle multiple fonts and embedded graphics as well as arithmetic functions. For full math capability, the spreadsheet and graphics package handles typical math functions as well as transcendental, business, and financial functions in its matrix of 999 columns by 9,999 rows. Rather than storing blanks in unused spreadsheet cells, a sparse-matrix data structure stores only cells containing data. Users can specify relations between cells in separate spreadsheets.

The package's data-base manager

builds files of variable-length records accessed by an index file. The manager has a number of output modes and can store data from a number of different file types. Two layers of security—file and screen password—control access to data-base files.

As with the data-base manager and word processor, the spreadsheet-and-graphics package allows users to view any practical number of spreadsheets simultaneously through separate windows on the PC's graphics monitor. Graphics functions cover the full range of business needs.

The packages run on an IBM PC (and compatibles) equipped with 128-K bytes of memory and two 320-K floppy-disk drives and cost \$500 to \$700 individually, although a discount is available when purchased together. Versions will be available soon for the DEC Rainbow, TI Professional, and others.

Innovative Software Inc., 9300 W. 110th St., Suite 380, Overland Park, Kan. 66210. Phone (913) 383-1089 [Circle 400]

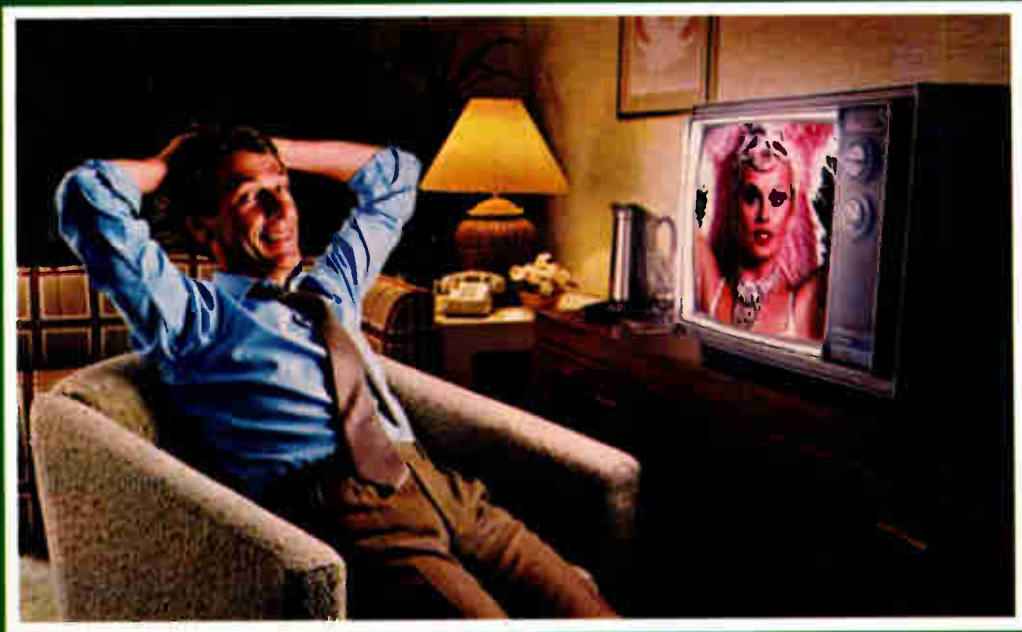
**Data-base system
works with CICS/VS**

"Imagine," an information-center reporting and query system that executes under the CICS/VS operating system, allows users to access corporate data in a friendly but secure environment. The system makes it unnecessary for users to learn syntax, memorize vocabulary lists, or know anything about file structures. Instead, they specify queries or reports by choosing options from menus to create report specifications.

The system comprises three types of on-line facilities—query, report writing, and administration—and a batch report generator. The query facilities provide control over report content, sorting, and data selection. The report-writing facilities give users full control over detailed formatting and let them create expressions, perform calculations, and create matrix or financial reports.

And the administration facilities include a data dictionary, security, resource control, and printer queue

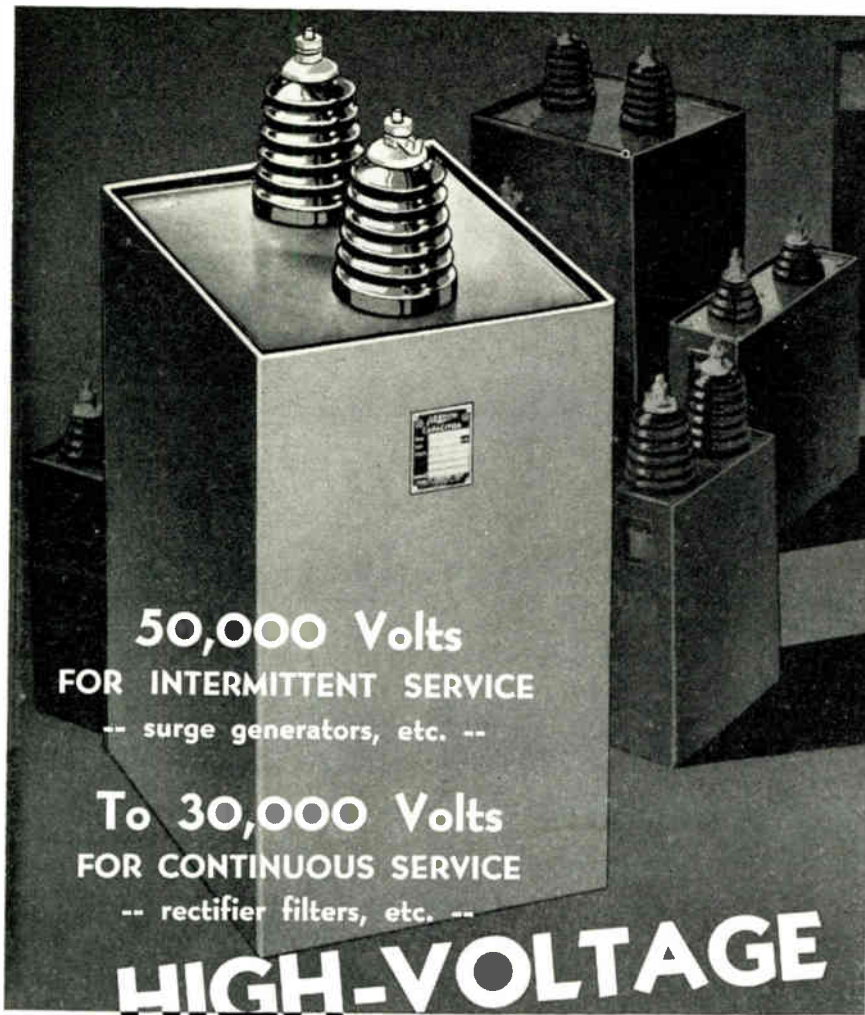
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- Type 25020 — 25,000 v.
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- Type 37520 — 37,500 v.
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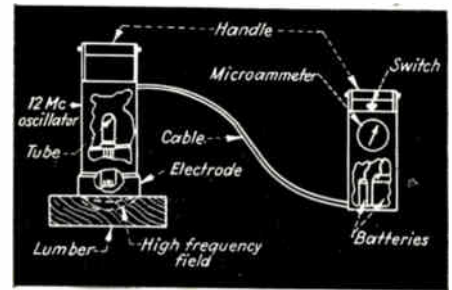
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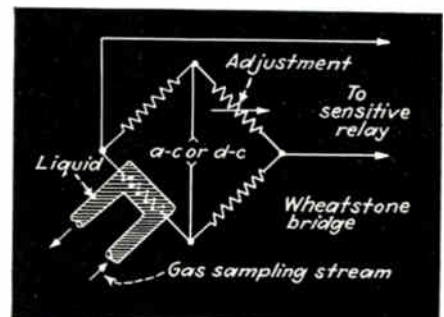
Lumber moisture checker. A high-frequency field is substituted for the conventional test needles and d-c ohmmeter

change in the anode current of the oscillator and this change is indirectly measured by means of a microammeter installed in a second unit along with operating batteries for convenience in handling. A chart furnished with the instrument tells what the microammeter reading should be when woods of various varieties are normally dry. Other microammeter readings indicate relative moisture content. Directly calibrated microammeter dials are available for certain frequently handled woods.

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Wheatstone bridge method of sampling noxious gases dissolved in liquid and used as one arm of the bridge

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New products

management. Imagine will be available for use with the OS/MVS, DOS/VSE, DOS/VMT, and OS/VSI operating systems, and it executes with CICS/VS 1.6. The OS/MVS version will be available next month at \$41,650; the DOS/VSE version, for \$31,500, will come early next year.

Multiplications Inc., 1050 Massachusetts Ave, Cambridge, Mass. 02138. Phone (617) 864-5810 [Circle 393]

Software brings graphics to MS-DOS, PC-DOS computers

The Graphics Systems Extension (GSX) software, which extends an operating system to include graphics output and input functions, is now available for IBM's PC-DOS and Microsoft's MS-DOS. With GSX, graphics application programs can be moved from one computer to another. GSX provides interfaces to graphics peripherals and lets operating systems control plotters, printers, and other graphics devices.

GSX is made up of two major subsystems. The Graphics Device Operating system—the device-independent portion, which is based on the Virtual Device Interface standard for graphics software—intercepts and services calls from graphics application programs and loads the device-driver modules to support different I/O devices. The Graphics Input Output System, the device-dependent modules, are device drivers that translate calls into the unique protocols of graphics devices.

The end-user price of GSX is expected to be about \$90, although it is currently available only to original-equipment manufacturers.

Digital Research, 160 Central Ave., Pacific Grove, Calif. 93950. Phone (408) 649-3896

[Circle 394]

Data-base system serves computers linked to DECnet

Ingres/Net gives users of the Ingres relational-data-base-management system distributed access to remote

data bases on any Digital Equipment Corp. VAX computer in networks connected by DECnet. Running remote application programs cuts the number and size of messages and communications costs and also improves response time for interactive applications, the company claims.

Ingres can be used to distribute and share data over many computers in a local or remote network. Available now to those holding Ingres licenses, Ingres/Net costs \$5,000 for the first network node and \$2,500 for each additional node.

In early 1984, the company expects to have Ingres/net available for 68000-based supermicrocomputers supporting Ingres and the Berkeley Unix 4.2 BSD release (which will support Ethernet).

Relational Technology Inc., 2855 Telegraph Ave., Berkeley, Calif. 94705. Phone (415) 845-1700 [Circle 395]

Ada compiler generates code for 68000-based computers

A low-cost Ada compiler runs on DEC VAX computers operating under Berkeley 4.2 BSD Unix and on small 68000-based computers operating under UniSoft's own UniPlus operating system. With Ada on small systems, low-cost work stations can be used to develop software, providing a more flexible environment for programmers, the company says.

The first of the compiler's two passes performs all lexical, syntactical, and semantic analyses. Its output is an intermediate file containing a low-level but mostly machine-independent program representation—which is the same in the VAX- and the 68000-based versions. Assembly code for a particular machine is generated from this intermediate file during the second pass.

Binary license fees for the VAX start at \$10,500 for one central processing unit; for the 68000 version, the fees start at \$3,500 for one CPU. Both versions are available now.

Unisoft Systems, 2405 Fourth St., Berkeley, Calif. 94710. Phone (415) 644-1230

[Circle 396]

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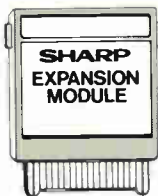
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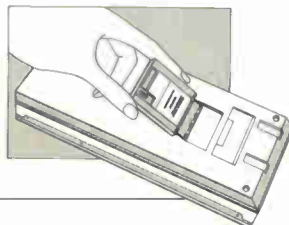
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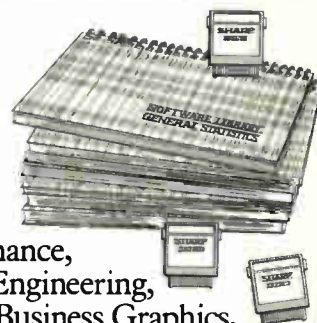


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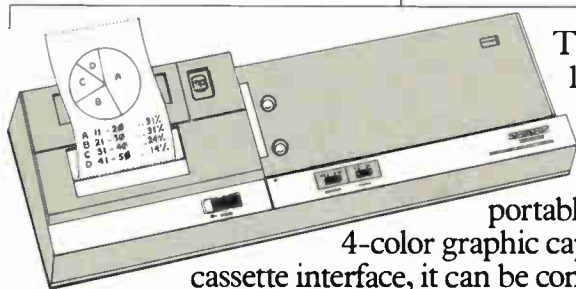
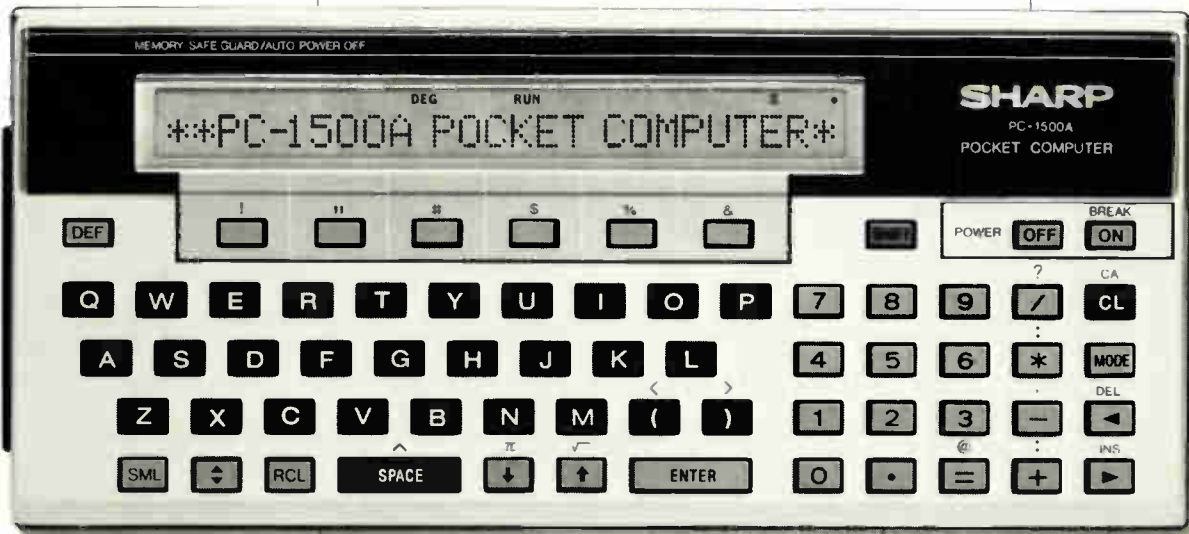
Now you can take 24K with you wherever you go—thanks to the new Sharp PC-1500A. It's the 8K hand-held computer that expands to a powerful portable 24K computer system when the optional 16K memory module is added. And because it's programmable in Basic, the most popular computer language, it gives you the power and capabilities to handle most scientific, engineering and management uses.



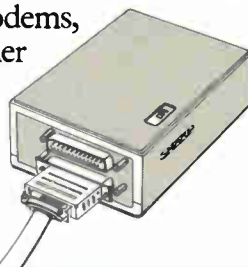
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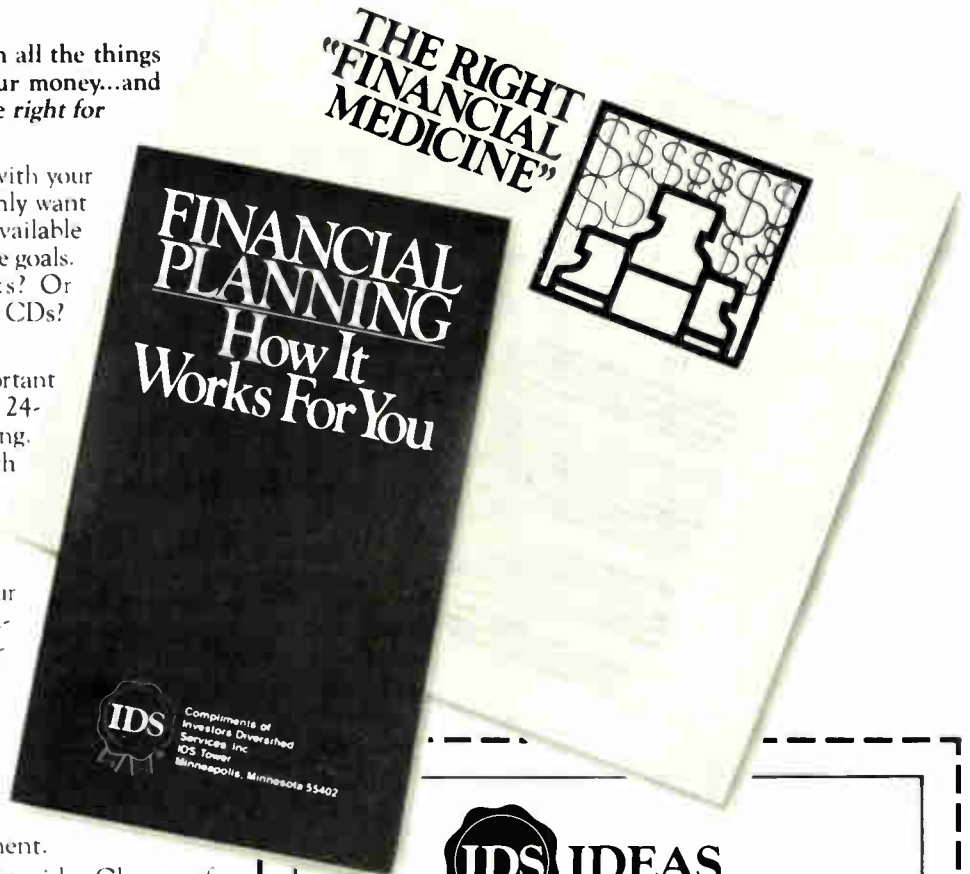
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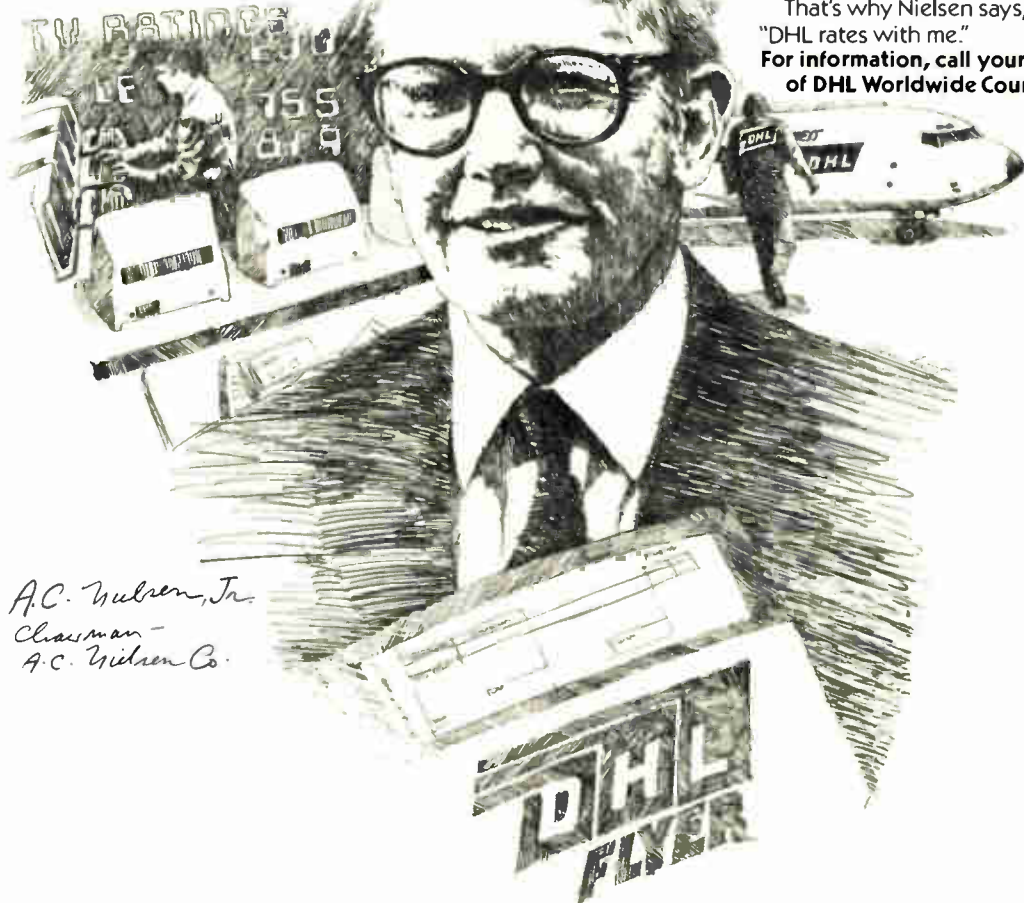
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NV-RAM protects data when voltage is low

Intel Corp., Santa Clara, Calif., has developed two nonvolatile semiconductor memories that include on-chip circuitry to prevent accidental erasure of data. When the power supply drops below 4 v, the circuit disables internal erase and write functions to prevent spurious system signals from destroying data. The 2004 NV-RAM (nonvolatile random-access memory, also known as a shadow RAM) is actually a 512-by-8-bit static RAM backed up by an electrically erasable programmable read-only memory array. When the system's power goes on, the contents of the EE-PROM array automatically move into the RAM. The other model, the 2817A, is a 5-v-only EE-PROM organized as 2,048 words by 8 bits. In quantities of 100, the 2004-3 (300-ns access time) sells for \$25.10 and the 2817A-4 (400 ns) for \$28.10. Samples are available now.

Digitizing camera emerges for microcomputers

A digitizing camera for personal computers puts two- or three-dimensional images into machine-readable and -storable form. Model 610, from Datacopy Corp., Palo Alto, Calif., uses a linear array of 1,728 photosensors to scan an image and organize it into a matrix of 4.9 million picture elements. The information can be displayed on a cathode-ray tube, stored on a disk, sent over communications lines, and processed like all other data. Available now for \$7,850, model 610 is the company's first digitizing camera for personal computers.

\$22,500 graphics system can be upgraded to 3-d

A \$22,500 graphics system with an upgrade path for full three-dimensional display has a range of graphics functions, including color raster display and a real-time dynamic transformation capability. Megatek Corp.'s Whizzard 3355 features a proprietary Graphics Engine: a local processor, including host interfaces, that supports local memory management, user tasks, and data transfer. A 16-bit microprocessor with local memory offloads the host computer, so the new system can perform locally all transformations needed for rotating two-dimensional displays. Deliveries from the San Diego, Calif., company are scheduled to start in the first quarter of 1984.

Winchester guarantees 98% quality acceptance

Century Data Systems contractually guarantees at least 98% "out-of-box" quality acceptance on its AMS 571 14-in. Winchester disk drive, positioned to compete against Fujitsu's M2351A but with 100 or so additional megabytes of storage. The 571-megabyte, 14-in. AMS-571 combines 32,000 bytes per track with a five-disk platter configuration. The Anaheim, Calif., company's high-performance drive uses 19 thin-film data heads, which can read 10,000 b/in. The AMS 571 has an average access time of 19 ms and is compatible with the *de facto* storage-module-drive interface standard, except for a higher data-transfer rate of 1,920 kb/s. It costs \$8,400 each in lots of 200.

In-circuit testers come as complete systems

The 310 and 320 series in-circuit testers, from Zehntel, Walnut Creek, Calif., are now available as complete turnkey test systems. Formerly offered as unbundled test instruments that had to be linked to a business or scientific computer, the firm's testers are now fully integrated with an HP 9826 or 9816 boosting board-production throughput by 25%. The 310 costs \$49,950, the 320 \$45,950. Both are available now.

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Career outlook

IEEE backs stable employment

The Institute of Electrical and Electronics Engineers has developed a new statement on professional practices, and its most significant addition to the IEEE's earlier guidelines is probably a recommendation that employers adopt a "stable employment policy." The new statement was put together by the Task Force on Career Maintenance and Development, which says it took into account many surveys of engineers and engineering managers. Recently approved by the U. S. Activities Board, the statement supplements the Guidelines to Professional Employment, developed in 1978 and later blessed by 28 professional societies.

The leader of the task force was Marlin Ristenblatt, a research engineer at the University of Michigan's Department of Electrical and Computer Engineering. He notes that the statement urges companies to adopt four-day work weeks and extended vacations—practices that have become more common with each recession, notably in the semiconductor industry—if they are needed to avoid outright layoffs.

The guidelines themselves defend the stable-employment recommendation by arguing that "companies which adopt no-layoff policies are attractive to engineers . . . Such a policy demonstrates that the company has concern for people and that people are not 'commodities' to be used and discarded at the convenience of the business."

Uneven needs. Ristenblatt says that many of the engineers surveyed felt that the recruitment and employment policies of start-up firms and defense and aerospace contractors made this provision important. Such companies often have urgent staffing needs in the short run but uncertain longer-term prospects. The statement calls on companies to give any prospective employee full information about their uneven labor needs. "These companies, when hiring, should put flags out all over the place and warn people," says Ristenblatt.

In essence, he adds, the new guide-

lines ventilate the concerns of many engineers about managements perceived as too tied to the bottom line. "I think this will put pressure on the MBA types," says Ristenblatt. "MBAs must give increasing attention to the care and feeding of professionals, as well as to their accounting sheets."

Steady-state badge. Many managements have been reluctant to recognize and reward the experience of engineers who choose to remain on the technical side. The statement urges employers to grant more responsibility and job mobility to these "steady-state engineers," who often find themselves restricted to a single product line or research team and have little chance for lateral mobility. Among other things, the statement points out that such engineers could help train younger ones.

The statement also encourages senior technical staff to seek added responsibility. "Even if you're not in a supervisory role, there are a great deal of leadership things you can do from a position of knowledge," says Ristenblatt. Such engineers should more aggressively make their knowledge and experience available to the organization, thereby raising their value to it and avoiding the "steady-state fate" of so many fellow engineers who disdain managerial roles.

While considerable attention is focused on how management can improve its treatment of nonmanagerial engineers and how they can enhance their own value to their firms, the statement also offers some general recommendations to engineers. "Improve your value," the guidelines advise, by increasing awareness of management issues and overall organizational needs. Also, it advises the engineer to "avoid routine work" to maximize the time for the technical areas he or she has been trained for.

The task force encourages all engineers to be "mature realists." Explains Ristenblatt: "Look ahead. Don't assume your job has tenure. Study whether the product you work on will have problems in the market down the road." Ristenblatt will present the new statement at the IEEE Careers Conference, in Palo Alto, Calif., Oct. 27-28. —Norman Alster



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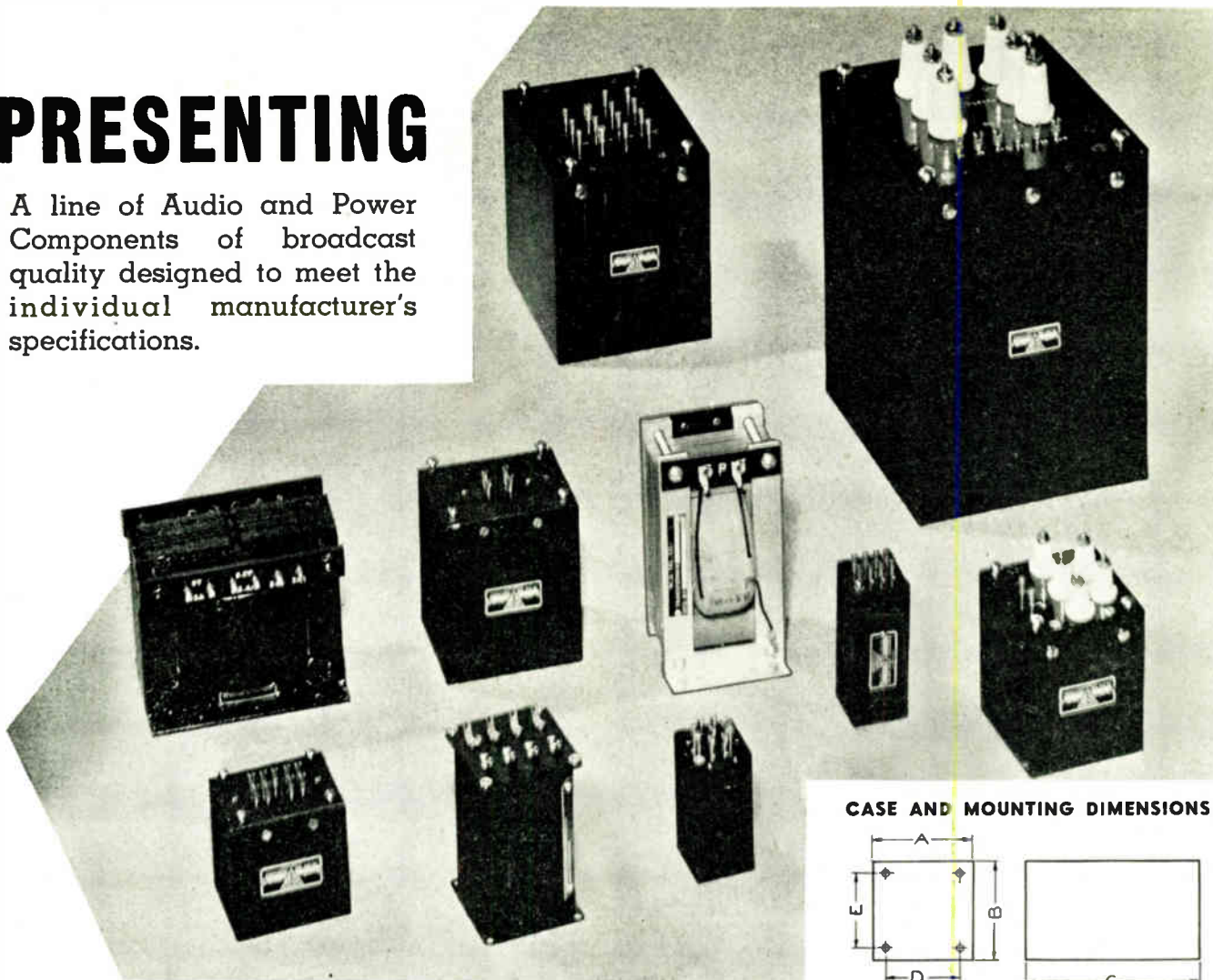
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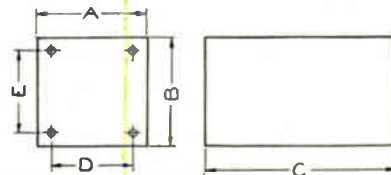
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2.

Please check which best describes your company's business at your location:

- Manufacturing Distribution Retailing Other _____

3.

Indicate the primary product manufactured or service performed at your plant or location (place applicable letter in box)

- A. Computers, data processing and peripheral equipment, office and business machines
B. Communications, data communications, telecommunications systems and equipment
C. Navigation and guidance, aircraft and missile systems or equipment (oceanography)
D. Test and measurement equipment
E. Consumer products (TV, radio, hi-fi, recorders, home computers, appliances)
F. Medical, industrial controls, systems or equipment
G. Semiconductor production equipment (component insertion, coil winding, etc.)
H. Electronic sub-assemblies, components and materials (passive, active components, IC's, discretes, hybrids, power supplies)
I. Other manufacturers using electronics equipment as part of their product (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
J. Government and military
K. Independent research and development laboratory or consultant
L. Research and development organizations which are part of an educational institution
M. Independent software developers
N. Operators of communications equipment (utilities, railroads, police and airlines, broadcasting, etc.)
O. Educational: 2-4 year college, university
P. Other _____

4.

Indicate your principal job function, occupation and/or title (place applicable letter in box. If letters O, P, or Q are used, fill in name of college or university).

- A. Corporate Management (Owners, Partners, Presidents, V.P.'s, etc.)
B. Operating Management (General Managers, Group Managers, Division Heads, etc.)
C. Engineering Management (Project Manager, Chief Engineer, Section Heads, V.P. Engineering, V.P. Research and Development, V.P. Quality Control, etc.)
D. Software Engineering
E. Systems Engineering/Integration
F. Quality Control Engineering (Reliability and Standards)
G. Design Engineering
H. Engineering Support (Lab Assistants, etc.)
I. Test Engineering (Materials, Test, Evaluation)
J. Field Service Engineering
K. Research and Development (Scientists, Chemists, Physicists)
L. Manufacturing and Production
M. Purchasing and Procurement
N. Marketing and Sales
O. Professor/Instructor at _____
P. Senior Student at _____
Q. Graduate Student at _____

5.

Indicate your principal job responsibility (place the appropriate number in box)

1. Management 2. Engineering Management 3. Engineering

6.

Estimated number of employees at this location: (check one)

- 1 to 49 50 to 249 250 to 999 over 1,000

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- h Components & Subassemblies

5 Source of Inquiry—DOMESTIC

- j Independent R&D Organizations
- k Government

Your design function (check each letter that applies):

- x I do electronic design or development engineering work.
- y I supervise electronic design or development engineering work.
- z I set standards for, or evaluate electronic components, systems and materials.

Your principal job responsibility (check one)

- t Management
- v Engineering Management
- r Engineering

Estimate number of employees (at this location): 1. under 20 2. 20-99 3. 100-999 4. over 1000

1	16	31	46	61	76	91	106	121	136	151	166	181	196	211	226	241	256	271	348	363	378	393	408	423	438	453	468	483	498	703	718
2	17	32	47	62	77	92	107	122	137	152	167	182	197	212	227	242	257	272	349	364	379	394	409	424	439	454	469	484	499	704	719
3	18	33	48	63	78	93	108	123	138	153	168	183	198	213	228	243	258	273	350	365	380	395	410	425	440	455	470	485	500	705	720
4	19	34	49	64	79	94	109	124	139	154	169	184	199	214	229	244	259	274	351	366	381	396	411	426	441	456	471	486	501	706	900
5	20	35	50	65	80	95	110	125	140	155	170	185	200	215	230	245	260	275	352	367	382	397	412	427	442	457	472	487	502	707	901
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7	22	37	52	67	82	97	112	127	142	157	172	187	202	217	232	247	262	339	354	369	384	399	414	429	444	459	474	489	504	709	951
8	23	38	53	68	83	98	113	128	143	158	173	188	203	218	233	248	263	340	355	370	385	400	415	430	445	460	475	490	505	710	952
9	24	39	54	69	84	99	114	129	144	159	174	189	204	219	234	249	264	341	356	371	386	401	416	431	446	461	476	491	506	711	953
10	25	40	55	70	85	100	115	130	145	160	175	190	205	220	235	250	265	342	357	372	387	402	417	432	447	462	477	492	507	712	954
11	26	41	56	71	86	101	116	131	146	161	176	191	206	221	236	251	266	343	358	373	388	403	418	433	448	463	478	493	508	713	956
12	27	42	57	72	87	102	117	132	147	162	177	192	207	222	237	252	267	344	359	374	389	404	419	434	449	464	479	494	509	714	957
13	28	43	58	73	88	103	118	133	148	163	178	193	208	223	238	253	268	345	360	375	390	405	420	435	450	465	480	495	510	715	958
14	29	44	59	74	89	104	119	134	149	164	179	194	209	224	239	254	269	346	361	376	391	406	421	436	451	466	481	496	701	716	959
15	30	45	60	75	90	105	120	135	150	165	180	195	210	225	240	255	270	347	362	377	392	407	422	437	452	467	482	497	702	717	960

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2 17 32 47	62 77 92 107	122 137 152 167	182 197 212 227	242 257 272 349	364 379 394 409	424 439 454 469	484 499 704 719
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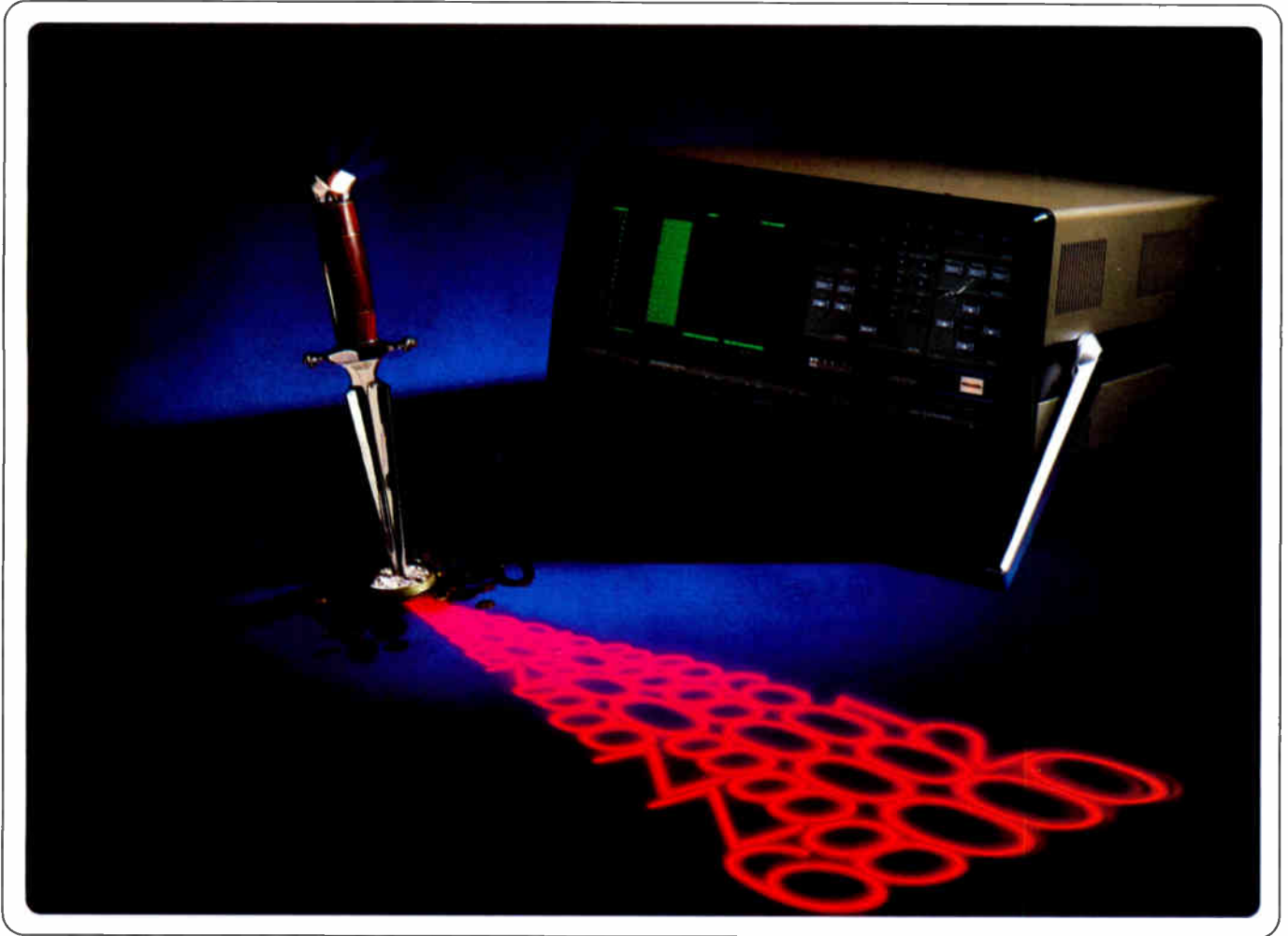
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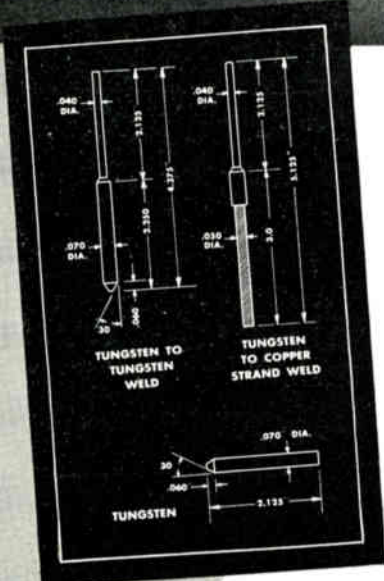
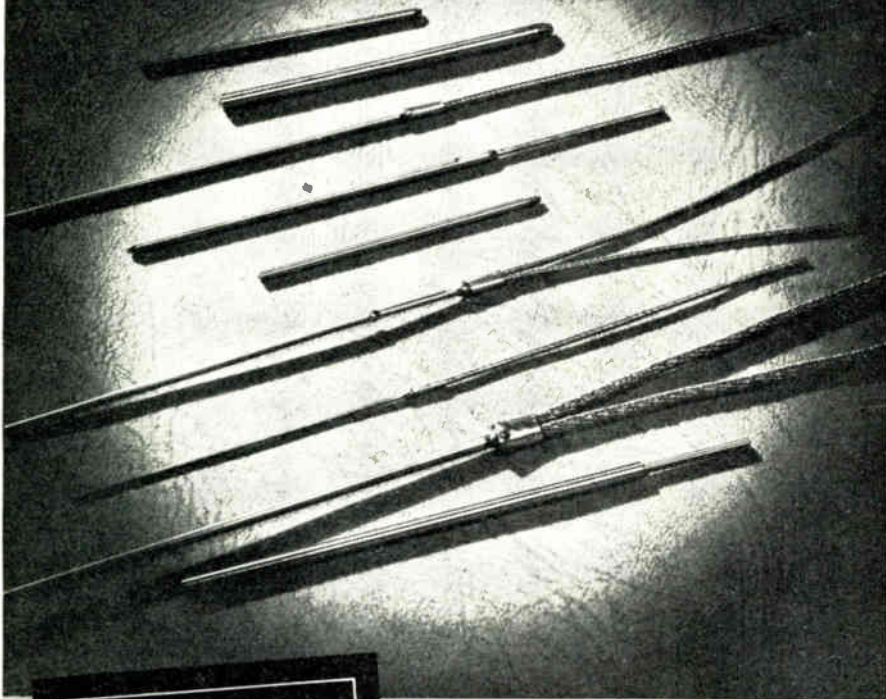
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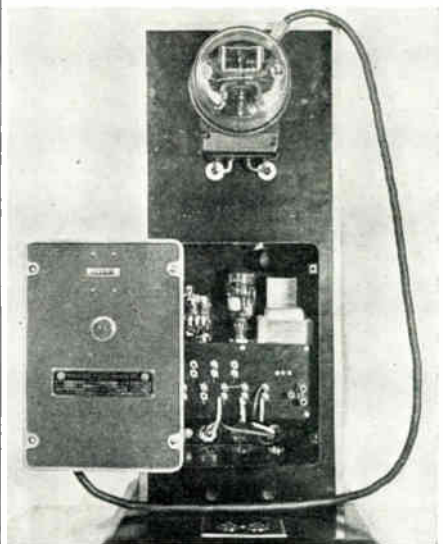


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mixed with the liquid in the sampling chamber. Any increase in sampling chamber conductivity due to the presence of such gas upsets the balance of the bridge and current proportional to the unbalance flows in the sensitive relay circuit, actuating an alarm.—Lamb, *ELECTRONICS*, December, 1940, p. 35.

Watt-Hour Meter Tester

THE DIRECT CURRENT in the anode circuit of a vacuum tube oscillator may be caused to change by introducing a metallic vane or shield between tube output and load circuits thereby altering the coupling between the two; or by introducing a metallic vane between an oscillator input and feedback coils, or into an oscillator field in such a manner that the frequency of oscillation is altered. The vane may be made of non-magnetic material and may be small and light, two factors which provide the basis for electronic control where magnetic or mechanical loading of the controlled device must be held to a minimum.



Electronic watt-hour meter tester. It counts the number of revolutions made by the meter disc or compares the speed of a test meter with that of a standard meter

The watt-hour meter tester pictured here and designed by Wheelco Instrument Co., uses the oscillator frequency-change principle. A small aluminum vane is mounted on the revolving disc of the meter to be tested. The vane passes between turns of wire in a pickup coil coupled to the tuned circuit of a remote oscillator through a flexible co-axial ca-

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