AUGUST 25, 1983

IC MAKERS SEE NEW PATTERN IN BUSINESS RECOVERY/105

Silicon compilers and layout compactor automate VLSI chip design/127

256-K RAM calls on 2-μm lithography, silicide interconnects/135

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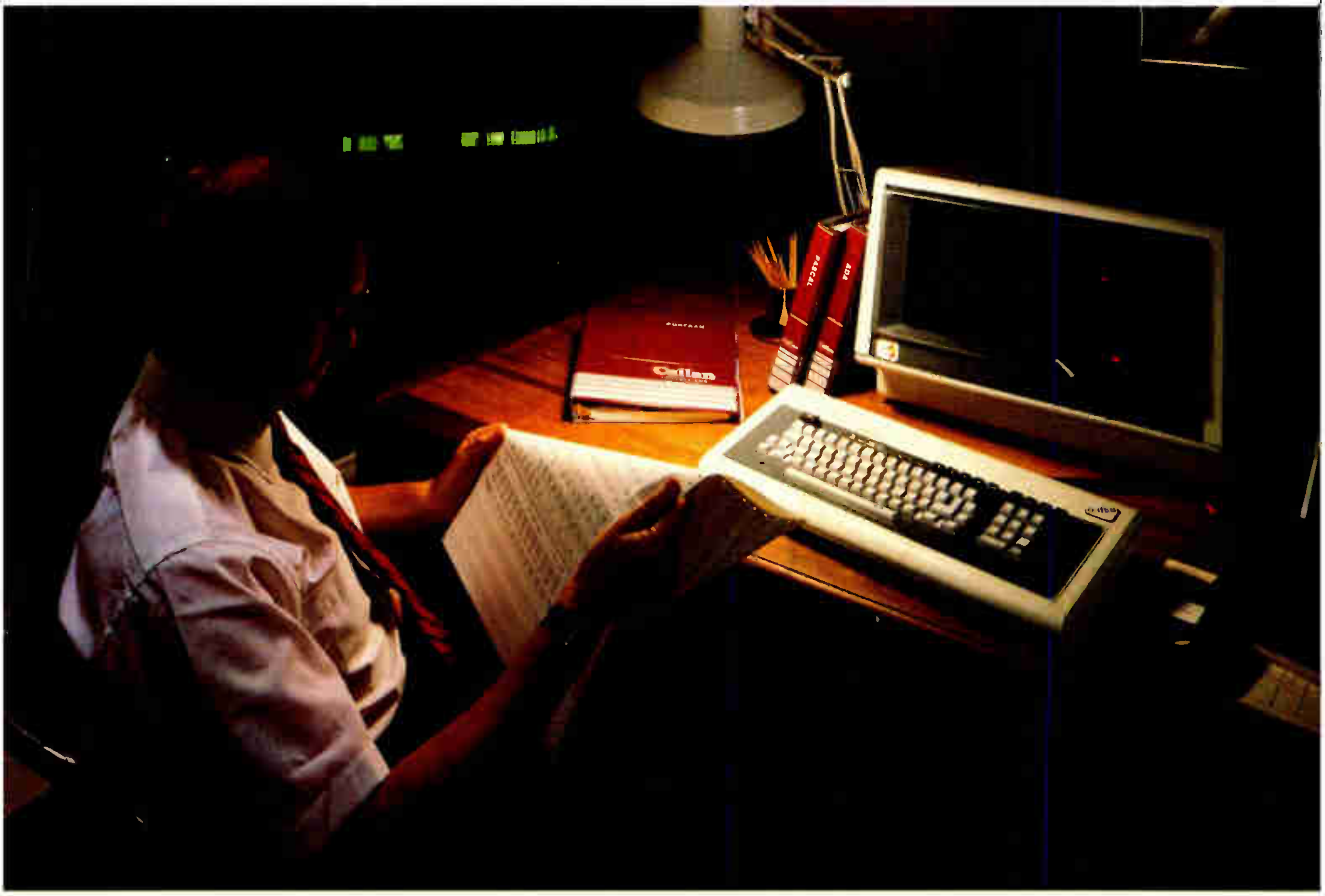

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The International Magazine of Electronic Technology and Business

Cover illustrated by Bob Clarke.

The Cover Story

One board computes and communicates, 121

A 16-bit processor, operating-system firmware, local-network chips, and most of the lower four layers of the International Standards Organization's computer communications model all fit on one board, easing life for system integrators.

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Electronics Review

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Highlights

Cover: Computer plus communications facilities fit on board, 121

Chalk up another victory for very large-scale integration: a single board that holds a 16-bit microprocessor with integrated peripheral functions and a coprocessing Ethernet chip set, plus operating-system and communications firmware, the latter incorporating the International Standards Organization's network- and transport-layer software for computer links.

Order rates buoy chip makers, but . . . , 105

Strong business from the manufacturers of small computer systems is swelling the order books at integrated-circuit makers, who expect a like increase in demand from large-system customers. But caution still rules, for the situation is too volatile for confident predictions of a long boom.

Cell compilers ease designing complex chips, 127

By generating layouts of circuit blocks from simple parameters furnished by the operator, a new silicon-compiler design approach makes it possible for inexperienced users to design optimized custom integrated circuits.

Emi suppression need not cost a bundle, 131

Complying with the tough rules regarding computer emission of electromagnetic interference can be done cost-effectively, so long as designers know proper ground, bypassing, and shielding procedures.

State-of-the-art-plus processes clear the way for 256-K RAM, 135

To craft a reasonably sized 256-K dynamic random-access memory that fights soft errors, short-channel effects, pattern definition, and related downscaling effects, major advances in fabrication processes are necessary, such as polycide interconnections and a lightly doped drain structure.

Radio-based computer links put terminals on the move, 142

A radio-based computer-communications system enables handheld intelligent terminals to communicate with a remote host processor. Advanced switching techniques maintain the links and let several hosts share the network.

Disk-drive testing grows in every arena, from designers to users, 147

Every engineer involved with disk drives, from designer through user, increasingly relies on testing to achieve the highest possible performance. Familiarity with the range of different tests is a *sine qua non.*

Coming up . . .

Test-system architecture tackles very large-scale integration. . . designing an error-correcting random-access memory. . . four chip makers implement the Unix System V operating system: an anthology.

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Publisher's letter

Reader interest tops the list of considerations when our editors evaluate technical manuscripts, but rarely does one get through the gauntlet leading to acceptance unless it also intrigues the editor who will shepherd it through the editorial production line.

For systems integration editor Harvey Hindin, Intel's communicating computers, dubbed COMMputers, (see p. 121), were more than simply intriguing. "They are the best idea in system integration that's come along in the past year or so," Harvey says. "This is a whole new theme, not just a variation."

What turned Harvey on about the COMMputer board family is what it does for system integrators: "They can concentrate on the application itself, which is where their true added value comes from, without worrying about the computer's operating system or the hardware and software for communications. It takes a lot of the torture out of system design."

On a single board, Intel packs a 16-bit microprocessor, firmware for a real-time operating system, Ethernet communication chips, and memory chips that store data-communications software. "Ordinarily, it would have taken three boards to provide all these functions," says Harvey.

But the high level of integration, impressive though it may be, is actually secondary in our editor's opinion. "In effect," he says, "the chips on the board implement most of the first four layers of the International Standards Organization's reference model for computer communications networks—the physical, data-link, network, and transport layers. Eventually, Intel and others will offer boards that cover all seven ISO layers." (The others are the session, presentation, and application layers.)

Harvey was equally impressed by the "open architecture" of the COMMputer family. "The boards satisfy many standards, among them DIN [West German standards widely used in West Europe], UL [Underwriters' Laboratories], and any of the collision-detection protocols defined by the IEEE's local-network standards committee."

Harvey rates the new boards as a major step for distributed processing, one he believes other computer-board makers will surely follow.

Major semiconductor makers are beset with two major preoccupations these days: the quality of the recovery in their markets that seems under way in the U. S. and Japan, and the imminent appearance in quantity of the 256-K dynamic random-access memory.

This issue takes a look at both concerns. Rob Lineback, our man in Dallas, talked about business prospects with the major semiconductor houses in Texas, and our correspondents around the world covered their bailiwicks.

Semiconductor suppliers were besieged in the spring and summer by small-system makers, our reporters found, but unmitigated euphoria has not set in. The market for personal computers is now so crowded that a shakeout seems inevitable. To keep from falling back into the resulting market trough, then, chip houses need a lift from mainframe makers.

Some think it has to happen; others are less sure (see p. 105). "The only thing that's certain," Rob says, "is that this recovery has a really different look than the previous ones."

Rob also had a hand in our story on Mostek's 256-K dynamic RAM (p. 49). Unlike the other 256-K chips on the market horizon, Mostek's has a "small-system" 32-by-8-bit layout rather than the more conventional 256-by-1-bit configuration. "Mostek actually put two teams to work on 256-K designs, one for a 32-by-8 chip having some new circuit twists and and one for a less adventurous 256-K-by-1," Rob says. Both designs were successful, and Mostek went to market first with the byte-wide chip. Rob reports a conventional 256-K chip will follow in about six months.

Readers' comments

EEs: too many or too few?

To the Editor: Thank you for your balanced coverage of the American Electronics Association's latest claim of an EE shortage ("Manpower surveys continue to disagree," July 28, p. 108). John Hansen's objection to projecting demand without regard to salaries and Paul Doigan's point that adding the five-year plans of companies ignores those that shrink or die both cause me to reach the same conclusion I reached last year: that the AEA survey belongs in the waste basket, not under a banner headline.

Richard G. Wiley, Ph. D.
Syracuse Research Corp.
Syracuse, N. Y.

To the Editor: Your dissection of the latest manpower report of the AEA deserves the thanks of every U. S. working engineer. Although the AEA's projections show a severe shortage, your careful examination of its methods, wording, and omissions shows that its survey is invalid.

What instructions did the AEA give respondents about growth in the GNP? What about the growth of Defense funding? Why did the AEA reduce by 16% the figures received from DOD contractors? This assumes that for every large, engineer-intensive DOD contract awarded, only one in every six bidders will not succeed. Common sense indicates that, more likely, only one in every six will get an award. The AEA should have reduced by 83% its estimate of how many engineers will be needed!

The AEA's Ms. Hubbard admits that we cannot draw conclusions about a shortage or glut of engineers from its report. Yet the AEA serves large employers of engineers. We can expect that the report will find its way to every member of Congress and will be used to show a need for additional engineers.

I have urged the Institute of Electrical and Electronics Engineers to fund a study of the shortcomings of the AEA's report and to make the results of this critique available to elected officials.

Irwin Feerst
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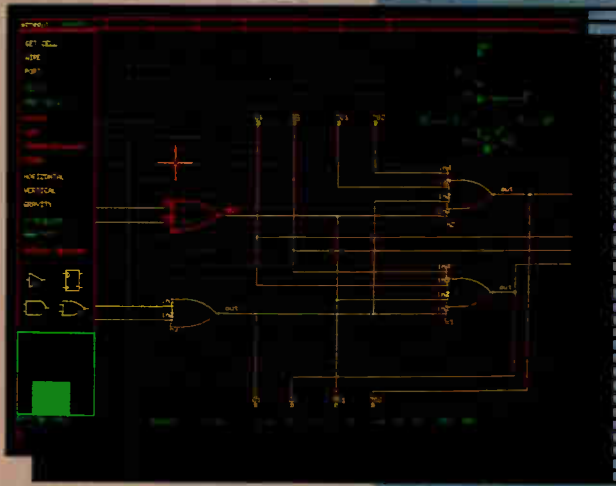

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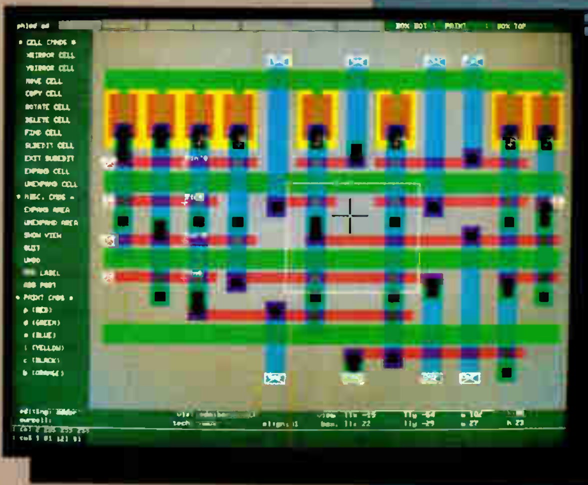

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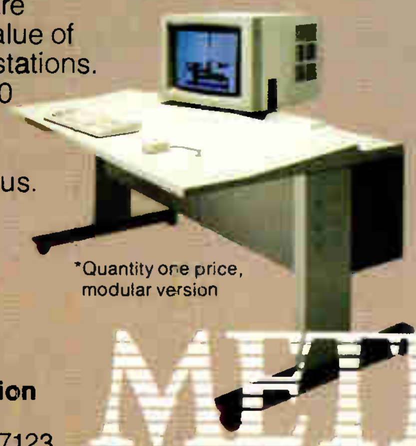

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Circle 11 on reader service card

A chance to boost U. S. competitiveness

A piece of important legislation now in the works in Congress is a good example of how Federal policy may influence the growth and health of high-technology industries—beneficially or detrimentally.

One problem that has been of much concern to the Government, particularly the Department of Defense, is the leak of high-technology knowhow to countries in the Soviet Bloc or to other unfriendly nations. The Export Administration Act, which came into law in 1979, was designed to prevent such leaks by embargoing many items and establishing some stringent licensing procedures to govern the export of high-technology products. The act has been effective in limiting the legal flow of technology to unfriendly nations, but unfortunately some of its provisions have made it extremely difficult for U. S. exporters to compete with companies in other Western nations. According to the American Electronics Association, too many items are embargoed by the U. S. unilaterally and arbitrarily, thereby allowing Japanese and Western European competitors to take away export markets from American suppliers—markets that may well have generated much-needed jobs in the U. S.

The importance of exports to the economic well-being of the country and the restraints in international competitiveness that have been imposed by EAA have become exceedingly clear to Congress, and bills have been introduced in both houses with a view to liberalizing the current legislation. The more liberal House bill, H. R. 3231, introduced by Rep. Don Bonker (D., Wash.), calls for, among other provisions, a single comprehensive list of truly critical items to be controlled and eliminates a number of noncritical items from the current list. It provides for simplification of the licensing procedures and mandates negotiations with Cocom countries. In general, it makes it easier to trade with Cocom countries on a less stringently defined list of noncritical items.

Although it does incorporate several improvements over the existing Export Administration Act, the Senate bill (S. 979) departs quite a bit from the liberality of H. R. 3231. The AEA is concerned about some provisions of the Senate bill: one grants the Secretary of Defense the opportunity to review any proposed exports of products or technology destined for a controlled area. Also, the bill transfers the responsibility for enforcing the act to the Customs Service as opposed to sharing the responsibility, as at present, between the Commerce Department and Customs. This, it is feared, will add significant new delays to the export procedures.

It's a good thing that Congress is addressing this issue and that progress is being made. The House bill will probably come up for a vote in mid-September. S. 979 is still in the Senate Banking Committee and will probably not be reported out until late in September and thus will not be acted upon before the current Export Administration Act expires.

No one can quarrel with the need for vigilance against the transfer of critical technology to potential enemies, nor for that matter to friendly but aggressive competitors. On the other hand, it can be extremely harmful if paranoia is allowed to overrule reason in assessing what is critical and what is not and thus needlessly depriving U. S. industry of its rightful share of the export market. We are hopeful that a reasonable compromise can be reached.

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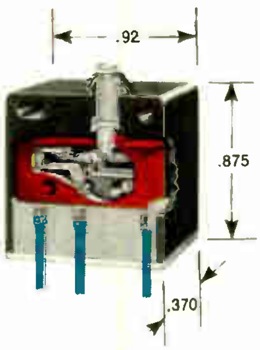

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People

Bode will help Wavetek catch the computer bus

It took a special kind of job to persuade Fred Bode to jump ship after moving steadily up for more than 20 years at Hewlett-Packard Co., which loses few of its executives. What attracted Bode, 46, to San Diego's Wavetek Inc. was the opportunity to have an impact at a smaller company entering the fast-moving electronics field of merging computers with test instrumentation.

Head start. Fred Bode will draw on his computer and instrumentation experience at Wavetek.

He found the niche earlier this year as new ventures manager at Wavetek. The firm, which makes function and pulse generators, is poised to plunge into computer instrumentation, or as some observers still call the gear, general-purpose–instrumentation-bus (GPIB) controllers.

Says Bode, "You can be sure I didn't make the decision lightly, but the timing and situation were right." Wavetek had nearly completed its model 6000 instrumentation computer, but needed an experienced computer hand to guide it to market. Bode's most recent post was marketing manager for HP's Desktop Computer division, Fort Collins, Colo.

With insight gained from this experience, Bode believes successful GPIB controllers increasingly will tilt to more computer capabilities. In fact, the MC68000-based Wavetek unit sports many such features, including multitasking and parallel processing, plus a high-speed analog-to-digital board that Bode says is missing from competitors' versions.

With characteristic marketing enthusiasm, he claims the model 6000 "has the performance of a mini and the ease of use of a desktop." For such computers, too, price competition is stiff, so Wavetek's price for the unit starts at $7,600.

To get the new computer to market in about a year, much shorter than a normal development cycle, Wavetek took a shortcut by starting with an existing product made and sold in Japan by Anritsu Electric Co. Although the finished model's software and operating features are more different from, than similar to, the Anritsu computer, "it's easier than starting from scratch," explains Bode.

"Inventing your way into a market doesn't get [you] there, because too many things are not right initially," he adds. "This is an intriguing way to do it." Similar products may be due from Wavetek, he hints. "This is going to be a big market, and Wavetek has a place in it."

Bode's career is well suited for the merging of the two formerly separate fields, since he has filled positions in instrument engineering and manufacturing, in addition to computer sales and marketing jobs that included a stint as manufacturing director in Tokyo. His first job after graduation from Yale University with a BSEE was in research and development for an aerospace firm.

Military software will go to war in chips, says Raytheon's Thun

The days of "catalog engineering" of military systems are ending, according to Rudolf E. Thun, newly named director of device technology at Raytheon Co., Lexington, Mass. Instead, he maintains, the software needed to obtain specialized functions will be put into custom and semicustom chips to hold down development costs.

Standard components are no longer efficient for implementing the architectures of real-time systems, he feels. "Five years ago, the problem

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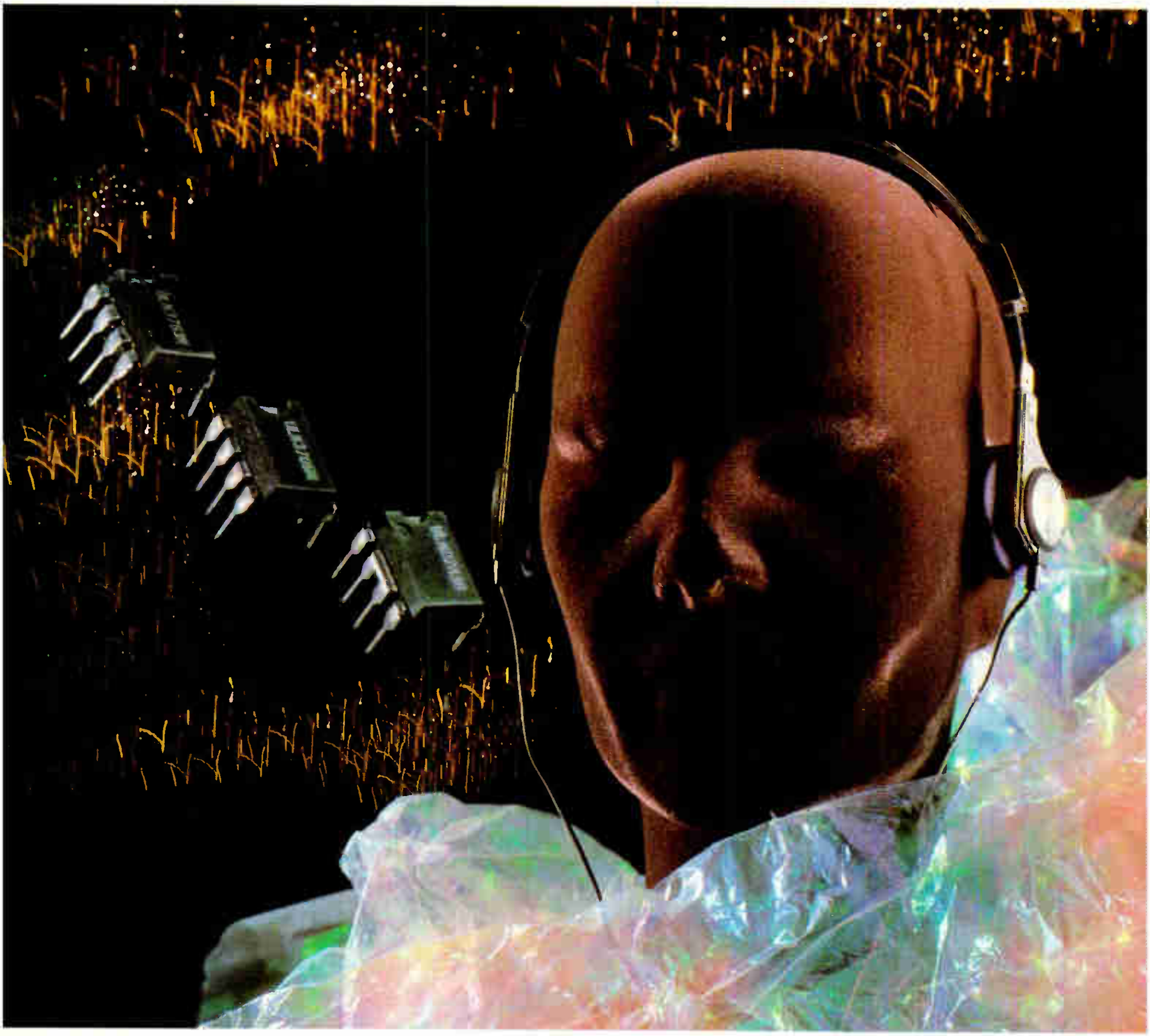

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People

Chipper. Rudolf Thun says software for military systems would be cheaper on chips.

was to put the system on a chip," he explains. "Now the challenge is to implement specialized algorithms. One of the great hopes is to reduce software costs through dedicated hardware."

For instance, multiprocessor systems would be built around specialized chips that are designed to execute specific algorithms. Breaking out repetitive subroutines that perform, for example, filtering or beam steering would reduce the software required to assign priorities to real-time processing tasks.

To produce the new very large-scale integrated generation of dedicated hardware, Raytheon is building a $40 million advanced microelectronics center, initially equipped to fabricate integrated circuits down to 1.25-micrometer geometries. The 62-year-old Thun will oversee research efforts in analog VLSI, non–von Neumann architectures, and gallium arsenide, among other things.

Somewhat more esoteric is his interest in cryogenic packaging. At liquid-nitrogen temperatures (around 55 K), complementary-MOS and GaAs circuits show two to five times their room-temperature performance. But so far, the effort has stalled short of packaging densities that would yield "the maximum effect from the minimum amount of cooling." Thun, though, would like to give it another shot: "With people fighting for every fraction of a nanosecond, why give up so much?"

Thun holds a Ph. D. in physics from the University of Frankfurt. He worked on thin-film–device development at IBM Corp. before joining Raytheon in 1967. □

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Each instrument offers the highest performance available in its class. The 8506A measures ac voltages with a 24 hour accuracy of 120 ppm from 40 Hz to 20 kHz, while the 5440A supplies bipolar output voltages to 4 ppm! Add to this their straight-forward, microprocessor aided operation, and you can easily integrate a 5440A and 8506A into your measurement system. As a result, your traditional measurements can be made with reduced effort in less time!

System capabilities.

High performance on the bench is not all that this Calibrator and DMM offer. Complete remote programming and data output is available via the IEEE-488 bus. Adding the new Fluke 1722A Instrument Controller puts a complete measurement system at your fingertips! Performing closed-loop calibration and accuracy enhancement of DMMs, sources, or other products is a snap!

Find out more.

Why settle for anything less? Find out how easily the 5440A and the 8506A can enhance any of your calibration or measurement tasks. For more information call us at **800-426-0361**, or contact your local Fluke Sales Engineer or Representative.

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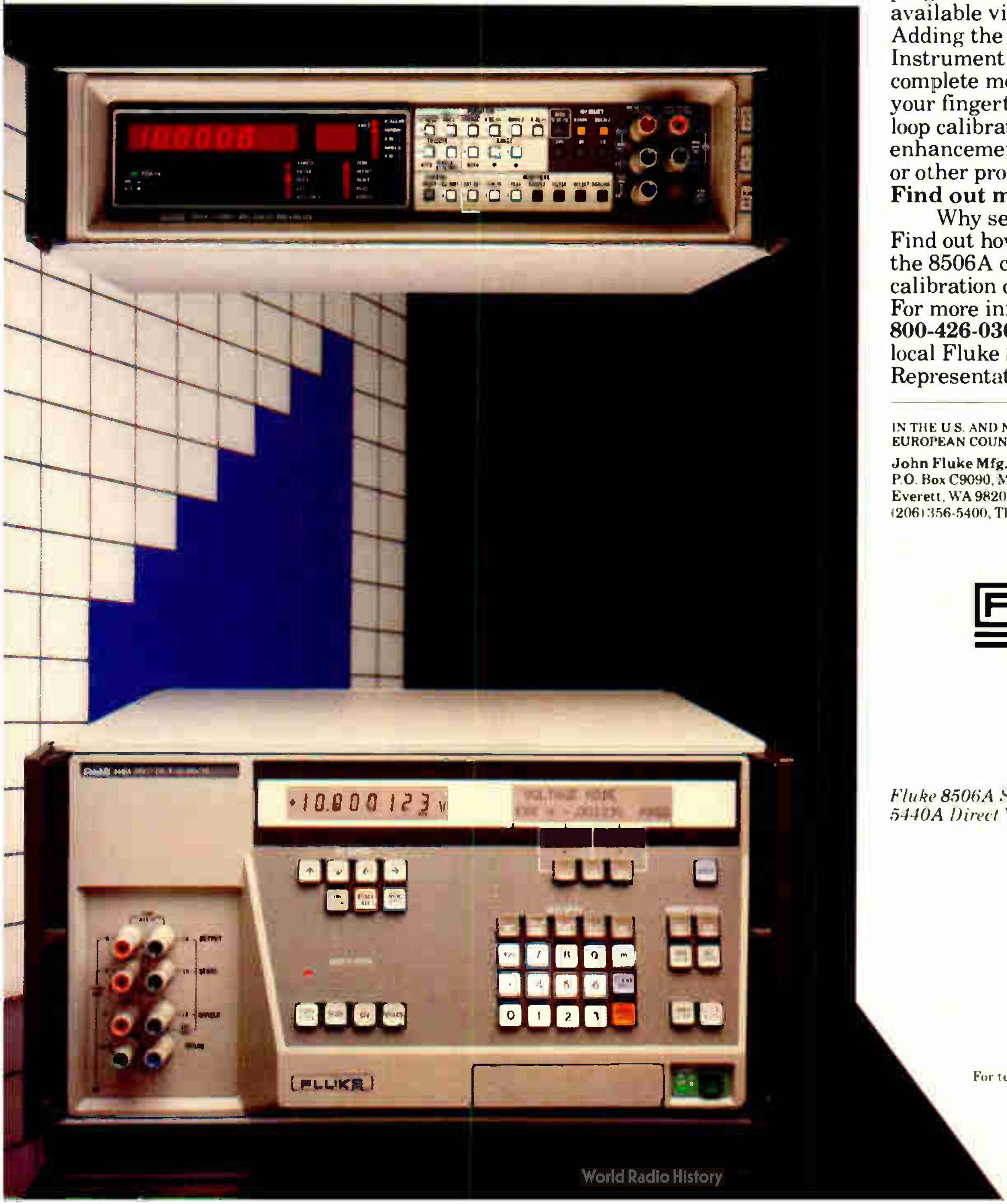

Fluke 8506A System Multimeter and 5440A Direct Voltage Calibrator

For technical information, circle no:17


PERMIAN BASIN DATA
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4685
Tektronix

Powerful text editing. High-speed graphics. Color copies. The new desktop family from Tek!

VT100 text editing and PLOT 10 color graphics are now packaged as basic desktop units and priced from $3995 complete.

Tek's new 4100 Series desktop terminals answer a range of resolution, screen size, color palette and local intelligence needs. All three feature outstanding 60 Hz non-interlaced displays and rapid 16-bit graphic processing speeds.

As simulated, Tek's 60 Hz refresh rate and bright phosphors result in a flicker-free image with perceivably better definition than that provided by 30 Hz terminals quoting greater pixel densities.

Standard capabilities include 38.4K baud communications; easy color selection from the keyboard; 4096 x 4096 addressable display space; a separate display surface for alphanumerics or communications dialog; and compatibility with ANSI X3.64 screen editors, including DEC VT100 extensions.

Each offers an unconditional, one-year on-site warranty. Tek Warranty-Plus extends this coverage two additional years at minimal cost.

	4105	4107	4109
Display Size	330mm (13")	330mm (13")	483mm (19")
Displayable Colors			
Graphics	8	16	16
Alphanumeric	8	8	8
Palette	64	64	4,096
Resolution	480x360	640x480	640x480
Segment Memory		128K Bytes	256K Bytes
Price	$3,995	$6,950	$9,950
Warranty-Plus	$195	$295	$395

For less than $1,600, you can add Tek's compact, plug-compatible 4695 Color Graphics Copier. With a palette of up to 125 shades, the 4695 lets you reproduce graphic and alphanumeric displays on report-size paper or transparency film at the push of a button.

All 4100 Series terminals feature programmable keyboards with innovative Joydisk for convenient graphics input.

At any time, you can plug into Tek's new 4170 Local Graphics Processing unit. The CP/M-86-based 4170 provides up to 886K RAM for standalone programming and pre- or post-processing—to help you conserve host power while you build upon a central data base.

Factor in compatibility with Tek PLOT 10 software and 4110 Series terminals, and you'll discover the first desktop graphics that you can't outgrow. Call your Tek Sales Engineer for a demonstration.

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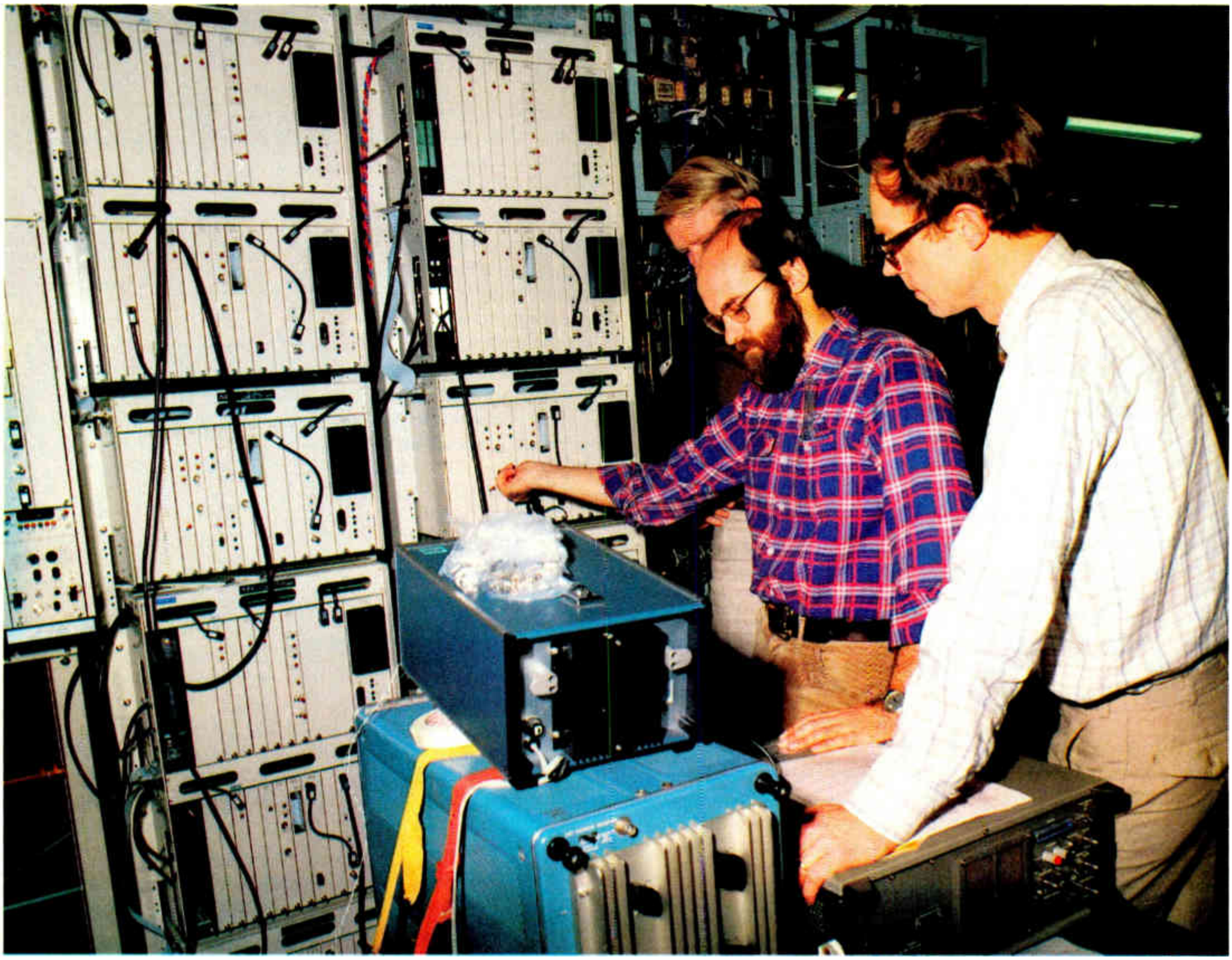
Circle 19 on reader service card



140Mbps DIGITAL MICROWAVE SYSTEMS TO SERVE SCANDINAVIA

As part of a drive to digitalize their telecommunications networks, Denmark, Sweden and Norway will employ 16QAM-140Mbps digital microwave systems from NEC.

Each country's link will provide high quality transmissions between its capital and other major cities. The combined length of these links is about 2,400 kilometers.

NEC's 16QAM-140Mbps digital microwave system has the highest bit rate recommended by CCITT and CCIR, and accommodates 1,920 communications channels.

Outside of Scandinavia, eight other countries around the world are using or have decided to use the same equipment.

Photo: Danish engineers test 16QAM-140Mbps digital microwave transmitter-receivers at NEC.

NUMBER 128

SINGAPORE INMARSAT STATION IN FULL OPERATION

Since the inauguration of its Sentosa coast earth station, the Telecommunications Authority of Singapore has been operating INMARSAT maritime telecommunications service.

The new station provides high-grade telephone and telex communications as well as facsimile and data transmission between land subscribers and ships in the Pacific Ocean.

For access, control, and signalling, the station uses a NEAX61 digital switching system capable of handling telex and data in addition to voice.

NEC, the world's leading manufacturer of INTELSAT earth station systems, completed the Sentosa coast earth station just 14 months after the contract was awarded.

The C/L dual band 13m diameter antenna, with an NEC-built INTELSAT Standard A earth station antenna in the background.

TWO TERMINALS FOR VOICE INPUT/OUTPUT

Verbal man/machine interface is offered by two compact, economical terminals—NEC's SR-100 and AR-100.

To program the SR-100 Voice Input Terminal, the user just speaks each word once. Almost any word, in any language, can become part of the SR-100's vocabulary. With its unique internal dynamic programming method, the SR-100 recognizes up to 120 words with over 99% accuracy. It is ideal for "no hands" situations.

Quick registration is also a feature of the AR-100 Voice Output Terminal. Built-in analysis circuitry lets vocabulary be changed in the field. The AR-100 uses NEC's bandwidth compression technology (adaptive differential pulse code modulation) for high-quality voice output. It takes up to 120 seconds of messages and has a built-in speaker, making it valuable in such applications as warning, instruction, or announcement systems.

Both the SR-100 and AR-100 interface with computers, numerical control machinery, medical equipment, and more. In combination, they become an efficient voice-operated control system that lets the user work away from the keyboard and display terminal area.

3-CHIP LSI OBEYS 512 SPOKEN COMMANDS

NEC is now marketing a 3-chip LSI that incorporates all the functions necessary for voice recognition and subsequent processing.

Consisting of the MC-4760 analog processor, μPD7761D recognition processor, and μPD7762G controller, the LSI is extremely easy to program. Voice patterns are registered when the operator speaks word-by-word through a microphone Recognition is achieved by referring sounds to these voice patterns. There is no need for an analog input circuit. The LSI holds up to 512 words using a 16K byte memory for every 128 words. Its recognition accuracy is over 98%, with an average recognition speed of 0.7 second per 2-second long word.

NEC's voice recognition LSI is easily interfaced with the main system host processor, either in parallel or in series. A special serial interface port is also available.

NEC

NEC Corporation

PO Box 1, Takanawa, Tokyo, Japan

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Since we first entered the Winchester market two years ago, we've accomplished many things our competition claimed were impossible.

It was impossible, they said, for a floppy disk company to make a significant dent in the highly competitive Winchester market.

We've not only made a dent, we're the second-largest company in the business, and we have the capacity in place to be first.

It was impossible to expand our production capacity from 0 to 60,000 drives a month practically overnight. But we did it.

It was impossible to sell Winchesters at such a low cost. But last year our 500 series drives were introduced at under $500, 30% under then-standard industry costs. And since then, we've led the industry to ever-lower costs on full and half-height drives.

It was impossible to produce and ship high-performance plated media drives in high volume at prices lower than most vendors are charging for oxide media drives. One of our competitors backed away from plated media because they couldn't buy enough of it to build drives in efficient quantities.

We solved that problem by building our

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own plated media factory dedicated to plated media production in high volume. Because we make our own, our costs are low and we are independent of outside vendors for supply.

It was impossible for a start-up company to produce and ship a broad line of products: full and half-height drives, open and closed-loop, from 6.4 to 50 MB. But we've done it. With the help of one of the industry's best-funded R&D programs. And with our steady supply of plated media, we will soon be offering 5¼″ drives that push Winchester technology to the limits of its capacity. In high volume. At prices that are pure Tandon.

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For our competition, yes.

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Circle 23 on reader service card

Disclaimer of liability for computer deficiency ignored

by **Marc E. Brown,** *patent attorney practicing in Los Angeles*

In an earlier column [*Electronics,* May 31, p. 24], I reviewed various ways in which liability for computer malfunctions could be limited by contract. The ways in which those limitations could be circumvented were, in turn, set forth in a subsequent column [*Electronics,* June 30, p. 24]. I concluded that "contractual limitations on liability are [only] unlikely to be honored when the sales transaction was induced by fraudulent oral misrepresentations or when the computer causes personal injury or property damage." If profits alone were lost (which is the commonest type of injury) and there was no fraud, no recovery could be had if the sales contract contained an appropriate liability-disclaimer clause.

In a significant departure from this existing law, the U. S. Court of Appeals for the Ninth Circuit has just held in Consolidated Data Terminals vs Applied Digital Data Systems Inc. (a decision filed on May 10, 1983) that lost profits can be recovered because of a defective computer, even in the absence of fraud and, in appropriate cases, even though the sales contract purports to disclaim such liability.

In the Consolidated Data case, a manufacturer of computer terminals (Applied Digital Data Systems) entered into a distributorship agreement with the plaintiff (Consolidated Data Terminals). The specifications for the terminals stated that they would operate at 19,200 baud.

In fact, however, none of the terminals was capable of operating at this rate. Following a year of unsuccessful efforts by the manufacturer to increase the speed of the terminals to specification, it decided instead to simply reduce the baud-rate specification to one tenth of its original amount.

This decision was unacceptable to the distributor. It terminated the distributorship agreement and brought a lawsuit to recover the profit that it would have made under the agreement if the terminals had performed in accordance with their original specifications.

Armed with what appeared to be an iron-clad liability-disclaimer clause in the distributorship agreement, the manufacturer proceeded to trial with confidence. The trial court, however, refused to respect the disclaimer and awarded the plaintiff judgment in the amount of $585,489.61.

On appeal, the manufacturer first argued that it could not be held liable because it did not guarantee the baud rate, but, to the contrary, disclaimed all warranties "other than a 90-day guarantee covering [defects in] materials and workmanship."

The Court of Appeals disagreed: "[B]ecause CDT [the distributor] relied on the [baud rate] specifications when ordering the terminals, this statement constituted an express warranty." Although the sales contract contained a disclaimer of all liability that did not arise from defects in materials and workmanship, the court concluded that "a disclaimer cannot be permitted to override a highly particularized warranty created by the specifications."

Even if a warranty had been breached, the manufacturer pointed to other language in the sales contract that stated that the manufacturer's "sole obligation under this warranty is limited to making good, at its factory, any product, or any part or parts thereof, found to be defective." Lost profits, the manufacturer argued, were implicitly excluded by this language.

Again, the Court of Appeals disagreed. Because the manufacturer had been totally unable to increase the baud rate of the terminals to the original specification, the court concluded that the exclusive contractual remedy of repair or replacement "failed of its essential purpose" and, for this reason, should be disregarded.

The manufacturer finally argued that, even if a warranty had been breached and even if the exclusive contractual remedy of repair or replacement failed of its essential purpose, the agreement still explicitly disclaimed "consequential damages," which in itself should be sufficient to bar recovery for lost profits (which is a type of "consequential damage"). Although the court reaffirmed that a manufacturer still had a right to disclaim liability for lost profits, the court narrowly interpreted language surrounding this disclaimer to mean that the disclaimer applied only when the damages resulted from use, as opposed to resale, of the terminals.

What does it all mean? Probably that computer manufacturers will not be able to so easily represent their products as having certain attributes, while simultaneously refusing to accept responsibility for those representations that turn out to be untrue.

This column sets forth basic principles of law and is not intended as a substitute for personal legal advice. Questions and comments are invited and should be sent to Mr. Brown in care of Electronics.

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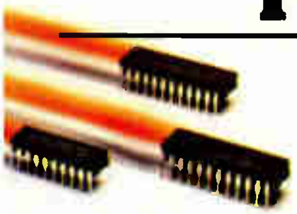

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These specs belong to the world's fastest ECL RAMs. Fujitsu's new MBM10422A-7 and MBM100422A-7. Both are results of our patented DOPOS (Doped Polysilicon) and IOP-II (Isolation by Oxide and Polysilicon) manufacturing processes. Both give you low power dissipation (0.7mW/bit) and 256 x 4 organization. And both are fully compatible with their respective industry standard 10K and 100K families. Plus, our 100K series gives you on-chip voltage compensation for improved noise margin.

When higher density is a must, but speed records aren't, look into our fully decoded 1K x 4 MBM10474 and MBM100474. Ideal for high speed scratch pad, control and buffer storage tasks, they deliver access times of 15nsec and low 0.7mW/bit power dissipation.

For main memory, control and buffer storage applications, our MBM10480 and MBM100480 give you the highest densities available anywhere. They're 16K x 1 products of an entirely new cell technology using the active pull-up (PNP) technique. They give you access times under 25nsec, extremely low power dissipation (0.04mW/bit) and very small cell and chip sizes.

Each of our ECL RAMs is fully compatible with industry standard 10K or 100K families. And if you're thinking about switching to an MOS part, you'll be happy to know these second-generation ECL RAMs deliver far lower cost per bit than the ECL products you've probably been dealing with.

For literature, call 800-556-1234 (ext. 82). In California, call 800-441-2345 (ext. 82). For samples, contact your nearest Fujitsu sales office. We'll set speed records to deliver the ECL RAMs you want.

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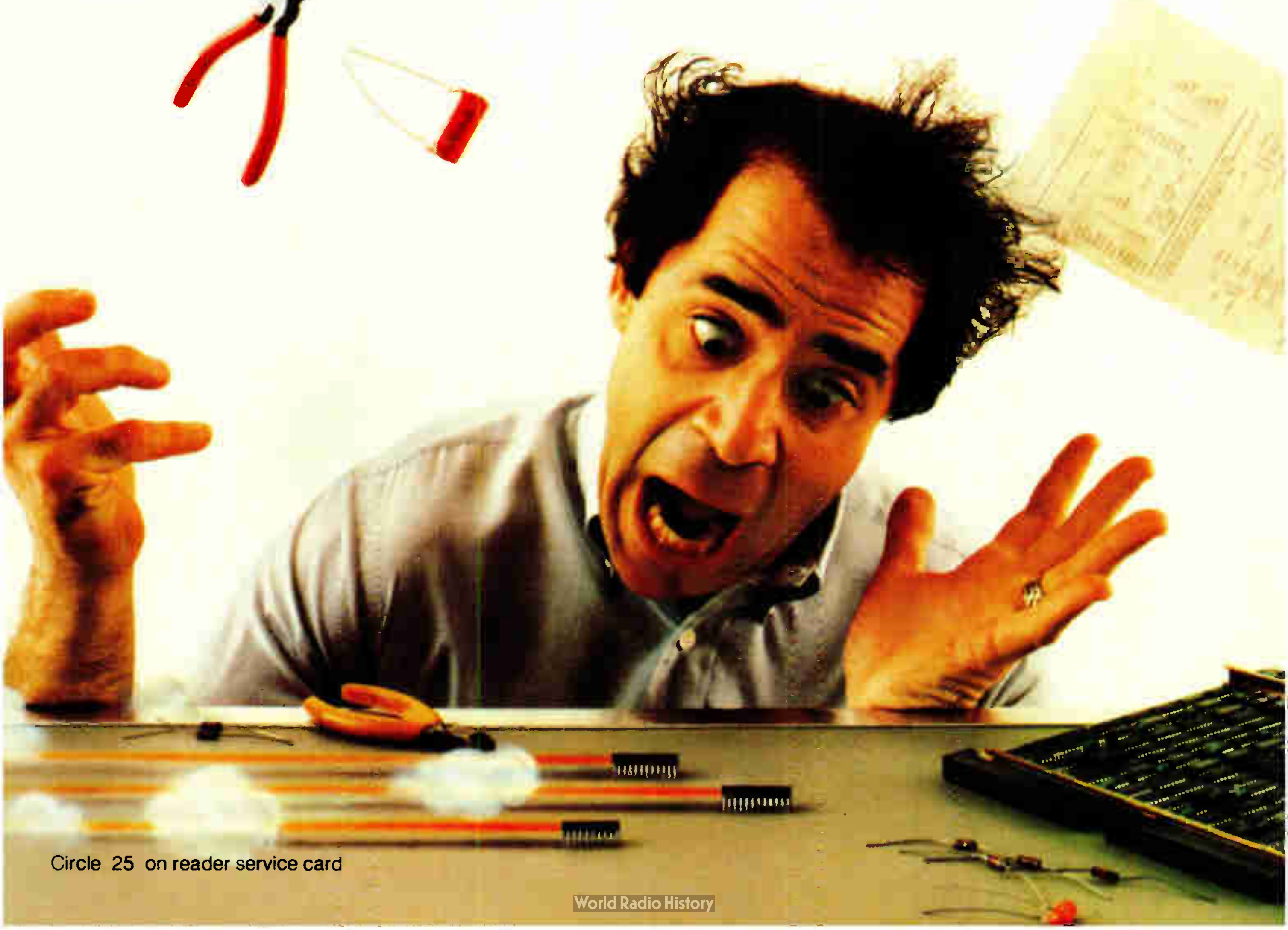

Circle 25 on reader service card

Meetings

International Conference on Computer-Aided Design, IEEE (445 Hoes Lane, Piscataway, N. J. 08854), Marriott Hotel, Santa Clara, Calif., Sept. 12–15.

2nd European Signal Processing Conference, European Association for Signal Processing (U. Arnold, Lehrstuhl für Nachrichtentechnik, Cauerstrasse 7, D-8520 Erlangen-Nuremberg, West Germany), University of Erlangen, Erlangen, West Germany, Sept. 12–16.

Autofact Europe, Society of Manufacturing Engineers (1 SME Dr., P. O. Box 930, Dearborn, Mich. 48128), Palexpo Conference Center, Geneva, Switzerland, Sept. 13–15.

Midcon/83, Electronic Conventions Inc. (8100 Airport Blvd., Los Angeles, Calif. 90045), O'Hare Exposition Center, Rosemont, Ill., Sept. 13–15.

Symposium on VLSI Technology, The Japan Society of Applied Physics (2-4-16 Yayoi, Bunkyo-ku, Tokyo 113, Japan), Surf Hotel, Maui, Hawaii, Sept. 13–15.

13th European Solid State Device Research Conference, IEEE *et al.* (Clive Jones, The Institute of Physics, 47 Belgrave Sq., London SWIX 8QX, UK), University of Kent, Canterbury, UK, Sept. 13–16.

Euromicro '83—9th Symposium on Microprocessing and Microprogramming, Euromicro Association (T. H. Twente, Department INF, P. O. 217, NL-7500 AE Enschede, The Netherlands), Madrid, Spain, Sept. 14–16.

Dry Process Symposium, Institute of Electrical Engineers of Japan (2-2-1 Katahira, Sendai 980, Tokyo), Tokyo, Sept. 19–20.

16th Electronics and Aerospace Conference, IEEE (Dr. John M. Walker, Westinghouse Electric Corp., Mail Stop 3200, P. O. Box 1521, Baltimore, Md. 21203), Shoreham Dunfey Hotel, Washington, D. C., Sept. 19–21.

6th Conference on Digital Satellite Communications, IEEE *et al.* (Howard Briley, Comsat Corp., 950 L'Enfant Plaza, Washington, D. C. 20024), Hyatt Regency Hotel, Phoenix, Ariz., Sept. 19–23.

9th World Computer Congress, International Federation for Information Processing *et al.* (Philip H. Dorn, Dorn Computer Consultants Inc., 25 East 86th St., New York, N. Y. 10028), Palais des Congrès, Paris, Sept. 19–23.

Semicon/East '83, Semiconductor Equipment and Materials Institute (Mary Beth Kern, SEMI, 625 Ellis St., Suite 212, Mountain View, Calif. 94043), Hynes Auditorium, Boston, Mass., Sept. 20–22.

9th European Solid-State Circuits Conference, Swiss Federal Institute of Technology (V. Valencic, EPFL-33 av. de Cour, CH-1007 Lausanne, Switzerland), Lausanne, Sept. 20–23.

33rd Broadcast Symposium, IEEE (Robert A. O'Connor, CBS TV Network, 51 West 52nd St., New York, N. Y. 10019), Hotel Washington, Washington, D. C., Sept. 21–23.

Electrical and Electronics Conference, IEEE (Southex Exhibitions, 1450 Don Mills Rd., Don Mills, Ont. M3B 2X7, Canada), Exhibition Place, Toronto, Sept. 26–28.

International Conference on Microlithography, Institute of Physics (Dr. G. A. C. Jones, Cambridge University Engineering Dept., Trumpington Street, Cambridge CB2 1PZ, UK), Cambridge, Sept. 26–29.

Seminars

Courses on **Data Communications Network Components, Network Design, Introduction to Network Architectures,** and **X.25 and Packet Switching** are among seminars being given in cities around the U. S. starting September. For a catalog, write Systems Technology Forum Inc., 9000 Fern Park Dr., Burke, Va. 22015.

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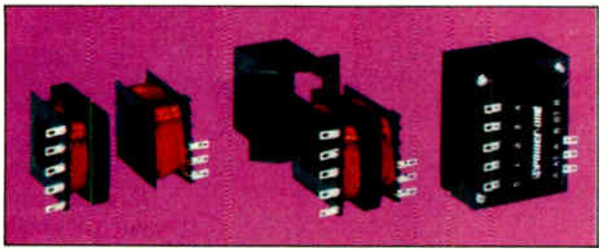

Power-One's patented International Series transformers feature separate, fully enclosed, primary and secondary coils. Meets safety requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.

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Circle 27 on reader service card

Low-cost now make

The new generation of word processors features flat-panel displays. Result: More efficient use of desk space. And an easier-to-read, more attractive, and more reliable terminal.

New display drivers from Texas Instruments are making AC plasma flat-panel displays practical. And providing reliable operation up to 225 volts.

The secret? TI's patented BIDFET process. It combines the best of several technologies—bipolar, JFET, CMOS, and high-voltage DMOS—all on one monolithic chip. Providing dramatic cost savings as well as reliable high-voltage operation.

In fact, only TI's BIDFET-based, flat-panel display drivers give you the extra margin of reliability built into DMOS high-voltage outputs. Plus high-speed, rugged inputs. Low power consumption. And the capability to integrate logic *and* drivers all on a single chip.

Cost-effective AC plasma display drivers

TI's leadership in AC plasma flat-panel display drivers is confirmed by the fact that we make the only totem-pole 32-bit drivers on the market. By integrating more lines per chip, these advanced drivers make AC plasma systems cost-competitive with high-character-density CRTs (see cost-projection chart).

You can select from four economical TI AC plasma display drivers. The SN75500AN and the SN75501CN have CMOS-compatible inputs. The SN55500AN and SN55501CN offer the same operation, but over the full −55° to 125°C temperature range. All can handle the 100-V swings. High speeds. And the complex logic required by AC plasma panel displays.

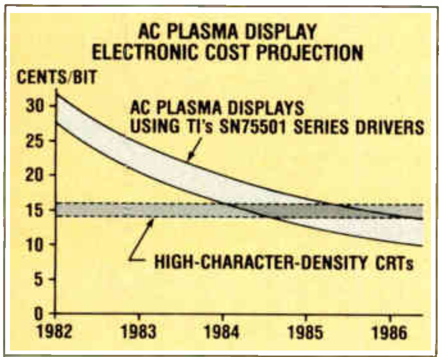
All feature thirty-two 100-V totem-pole outputs. 20-mA output-current capability. 4-MHz (max) input data rates. A 100-kHz (max) operating rate. And

◀ **Advanced word processors,** which are more compact, more reliable, and more attractive, incorporate flat-panel displays made possible by TI's new, cost-effective drivers. The flat-panel display shown is a mock-up that is conceptually similar to terminals now coming on the market from several manufacturers.

27-5087

TI BIDFET display drivers flat-panel displays practical.

200-ns output transition times. While consuming only 40 mW of power.



Bringing down the cost of AC plasma display systems to levels competitive with CRTs—just one of the advantages TI's patented BIDFET process brings to flat-panel displays.

Five VFD drivers for 60-V operation

Unique BIDFET technology enables all TI vacuum-fluorescent display (VFD) drivers to operate reliably up to 60 volts. These drivers include the widely used UCN4810A, plus the new TL4810A, SN75512A, SN75513A, and SN75518.

Pin compatible with the UCN4810A, the TL4810A gives you twice the speed and active totem-pole drivers on all 10 outputs. Plus, a strong 1-mA pull-down reduces interdigit blanking time to maximize system efficiency.

The SN75512A and the SN75513A offer the advantage of 12 drivers per package and complement each other in VFD applications. The SN75512A has a serial-input data register, data latches, and high-voltage buffers with totem-pole output structures—making it ideal for anode or grid control. The SN75513A—which includes a reset function instead of parallel data latches—is primarily used as the grid or line-select controller.

The SN75518, a 40-pin device, provides control and drive circuitry for 32 lines using the same architecture as the TL4810A (or SN75512A).

With the advantages of increased integration, the SN75518 represents a 30-percent reduction in equivalent system cost over the popular UCN4810A.

How TI BIDFET pays off for you

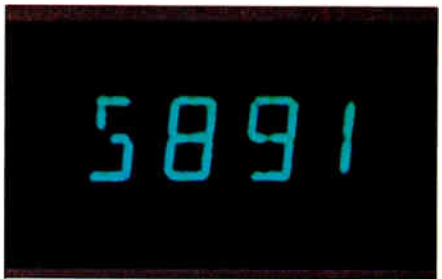
No other technology matches TI's BIDFET process for producing reliable large- or even medium-scale ICs with high-voltage capabilities. That's because only TI's BIDFET pools the advantages of many technologies.

JFETs are used to achieve high-input impedance, minimal loading, and compatibility with a variety of logic families.

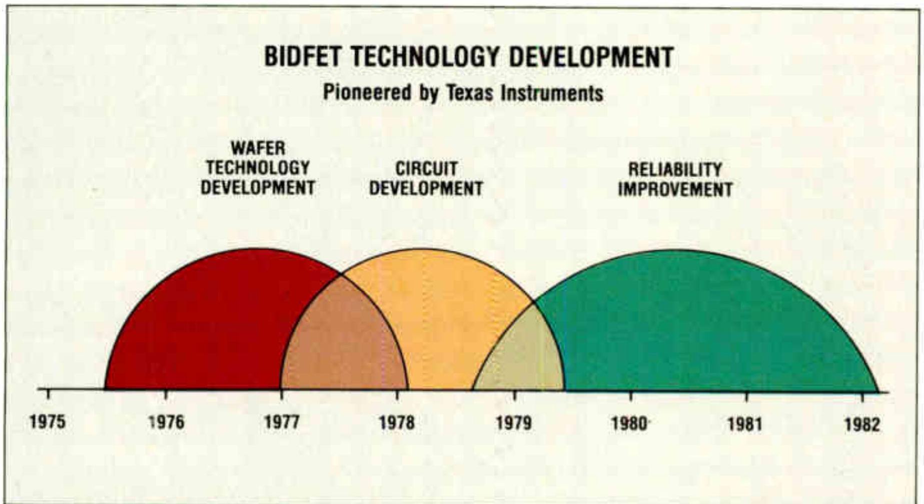
The bipolar section maintains the high speed of the input signal, with relative insensitivity to static discharge.

CMOS permits dense packing of the logic, while consuming very little power.

And DMOS transistors in the output stage handle exceptionally high voltages—up to 225 volts! Which makes TI's BIDFET-based drivers far superior to other display drivers, many of which can push the reliable limits of bipolar technology to only 60 volts.



Simple interfacing to VF displays of any size—from small segmented types to large dot matrix formats—can be achieved affordably with TI BIDFET drivers.



Reliable high-voltage operation results from BIDFET technology—a process TI has invested more than seven years in development.

A big, flat success

Outstanding today, TI's flat-panel display drivers will be even better in the future. That's because we soon will be applying BIDFET technology to electroluminescent display drivers. These will be able to operate reliably with DMOS output transistors up to 225 volts. And they will be available in space-saving plastic chip carriers. All ready to meet your needs for large, high-resolution panels that are thin and lightweight.

Find out how advanced TI flat-panel display drivers can increase reliability. Save money. Improve your design. And attract customers.

For more information, contact your nearest TI sales office or write Texas Instruments, Semiconductor Group LD, Dept. 013EC, P.O. Box 401560, Dallas, TX 75240. Or for direct applications assistance, call (214) 995-6162.

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When you sit down at our new K105 logic analyzer, the first thing you'll notice is that big, friendly red HELP button. Press it. You'll begin to feel better immediately.

You see, we wrote the book on logic analyzers. And now the book is in the machine. So when you press the button, you display easy-to-understand, step-by-step operating instructions right across the bottom of the screen. While the data from the operation you're performing remains on the screen.

And if you're still in trouble, just press again. The HELP button and an adjacent SHIFT button call up a HELP MENU and 28 pages of detailed instructions on every analyzer function.

We'll say it again. No other logic analyzer is so easy to use.

Modular design accommodates application changes.

The K105 isn't just easy to use. It's accommodating, too. By simply swapping boards, you can configure several different logic analyzers.

For instance, you can select up to 64 20 MHz channels in 32-channel increments for microprocessor analysis. Up to 16 100 MHz channels in 8-channel increments for hardware analysis. Or combine them to a maximum of 72 channels for software/hardware integration tasks.

And there's more. You can add a dual 5¼" floppy disk drive (IBM CP/M 86™ compatible) to store up to 70 setups or data files. While providing data portability and post-processing capabilities.

Disassemblers and Trace Control™ speed software debugging.

It's a lot easier to debug software when you can get your system's microprocessor to speak assembly language mnemonics rather than object code. And our disassembly modules for the 68000, 8086, 8088, 8080, 8085A and Z80B do just that.

And with the K105's 8 levels of Trace Control at 20 MHz, you can isolate and capture widely-separated slices of program flow to pinpoint failure causes . . . in a fraction of the time it would take with a conventional triggering scheme.

Two-analyzers-in-one enhances software/hardware integration.

When you're integrating hardware and software, the K105 is two analyzers in one. Just combine the 20 MHz and 100 MHz options to look at both state and timing. For trouble-shooting multi-processor systems, you can even monitor both processors and capture the asynchronous data between the two.

And the K105 offers a fast 5 ns glitch capture capability to pinpoint hard-to-find random problems.

Plus high-speed sampling for hardware analysis.

For high-speed sampling, you can configure the K105 with up to 16 100 MHz

To Simplify Logic Analyzer Operation, Press Here.

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Clearly the Best.

channels. Our unique automatic noise margin analysis feature enables you to verify specified system thresholds on as many as 16 channels simultaneously.

And design verification is simplified by a "don't care memory" that allows you to selectively mask out memory portions so you can compare only those portions you want to see.

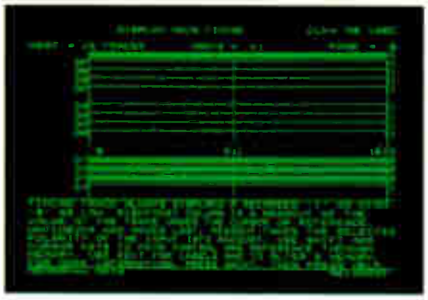
Uncompromising dedication to high performance.

The Gould philosophy dictates that every instrument we make be the best for the job it's designed to do.

The K105, with its unsurpassed ease-of-operation and modular flexibility to perform a wide range of analysis tasks, is evidence of that dedication.

For detailed application notes or a demonstration, write Gould, Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279, Gould Biomation and Gould Millennium Products.

For fastest response, call toll-free: Nationwide (800) 538-9320; In California (800) 662-9231 or (408) 988-6800.



The K105 offers you two levels of HELP at the press of a button. The first displays step-by-step operating instructions across the bottom of the analyzer screen. The second brings a menu to the screen, allowing you to select more detailed help from an integral 28-page manual.

GOULD
Electronics

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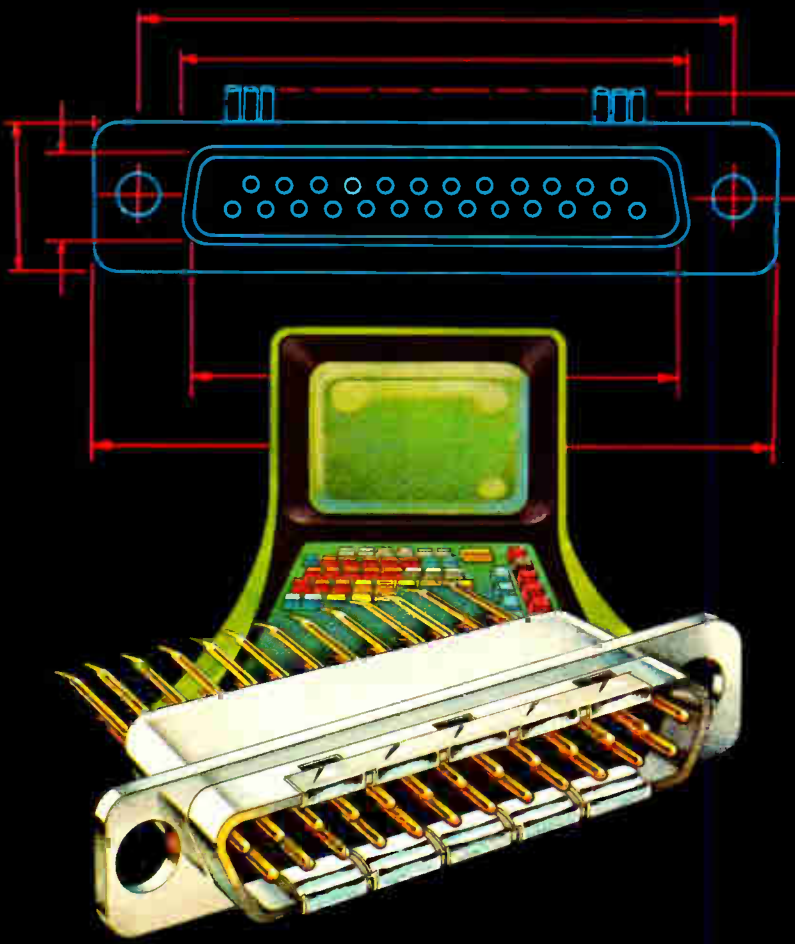


News update

■ Leonard I. Hafetz refuses to give up on a good idea. The founder of Interactive Images Inc., Woburn, Mass., Hafetz has finally been able to put on the market an enhanced version of a product he saw stalled at the starting gate three years ago.

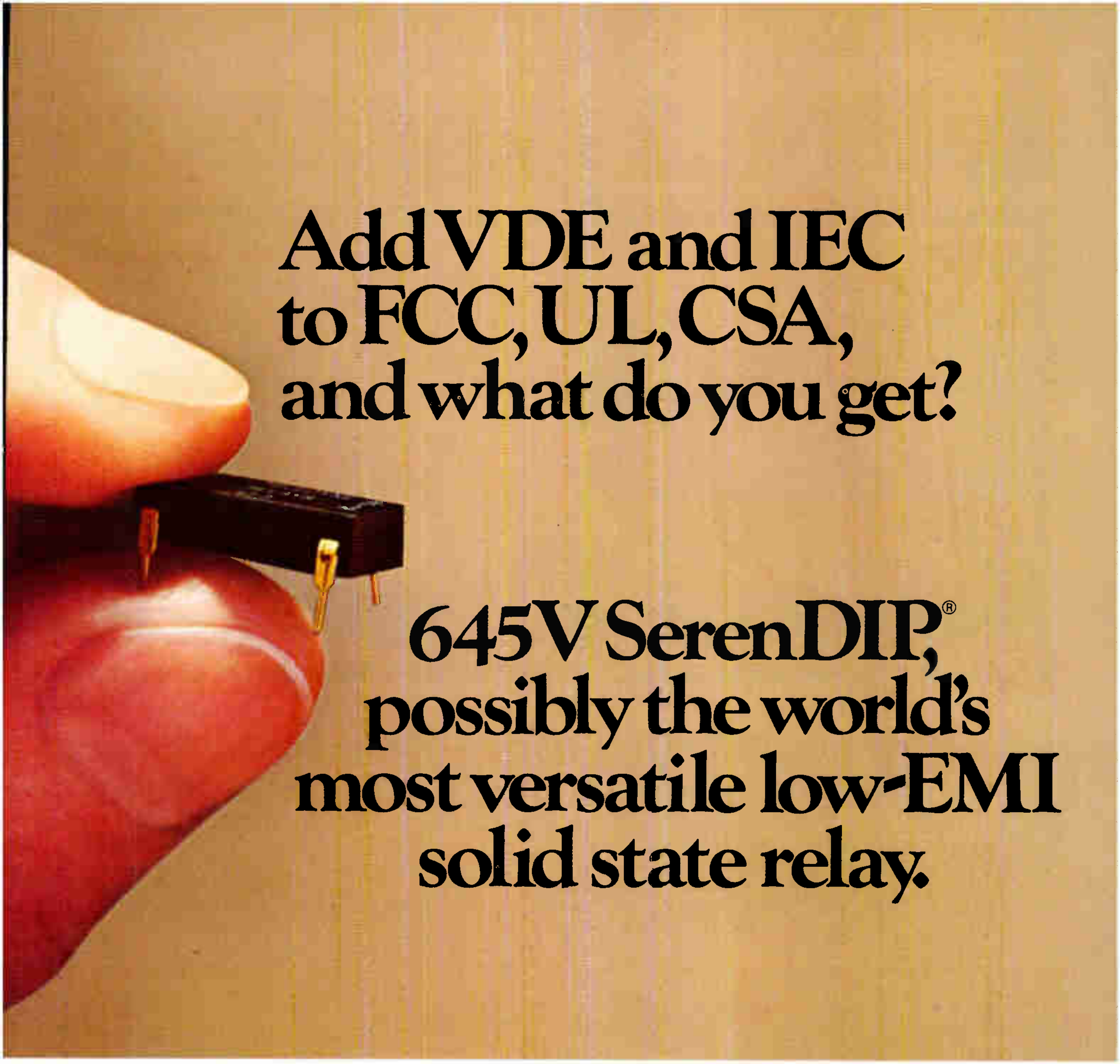
At that time, Hafetz was vice president of application engineering at Solid State Technology Inc., also of Woburn. The product, called Proteus [*Electronics*, June 5, 1980, p. 39], was a hardware-software package designed to let even inexperienced computer users run complex application programs.

Proteus provided helpful prompting by customized keyboards and menus displayed on a touch-sensitive screen. Typically, such menus make it possible to call up prepackaged blocks of information; this one lets users interact with the application program itself.

Nondelivery. But Solid State Technology, which developed Proteus under license from the Massachusetts Institute of Technology, never delivered the system. Just three months after its introduction, MIT terminated the agreement. An MIT spokeswoman in Cambridge, Mass., will say only that "the Institute felt it had grounds" for the termination.

Hafetz left Solid State Technology soon after, obtained the lapsed license himself in October, 1981, and formed Interactive Images. The company's first product was announced in June. Called Easel, it is a direct but more powerful descendant of Proteus, Hafetz says. Where Proteus was compatible with CP/M, Easel software runs under the multitasking Unix operating system and supports multiple program windows on its touch-sensitive screen.

Without modification by the user, software interfaces let Easel serve as a front end for programs written in many languages. An unbundled software package is available for about $650 and is included on dedicated 68000-based color-graphics terminals that start at $11,900. Easel is already off to a promising start. "We've shipped 20 systems so far," reports Hafetz. —**Linda Lowe**



We've made a good thing better.

Our 645V SerenDIP now complies with VDE and IEC standards. Added to previous FCC compliance, UL recognition, and CSA approval, that opens a whole new world to the 645V SerenDIP. And that can mean the solution to a world of problems. It meets VDE and IEC isolation, creepage and clearance spacing requirements. Combined with our special photo-coupling technique it reduces EMI well below the new FCC radiated emission specifications* and its VDE and IEC equivalents.

Engineered by Teledyne Relays, the 645V SerenDIP utilizes a patented zero-switch circuitry which practically eliminates switching transients with an advanced custom front-end IC design.

This newest addition to our solid state SerenDIP line is rated to switch up to 1 amp, without heat sink, at 250VRMS — with peak transient ratings up to 600 volts. It also features 3750VRMS input/output isolation.

Teledyne has been an industry leader for twenty years. We use our technical expertise and manufacturing know-how to create the world's best solid state relays.

If you need applications assistance or would like technical information about our SerenDIP relays please call or write.

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KRAMER VS. KRAMER

How FutureNet's DASH-1™ Revolutionizes Schematic Design and Documentation!

Efficient Schematic Designs

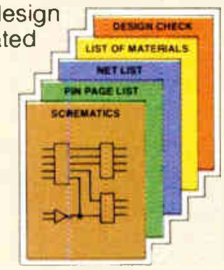
Poor Max Kramer is a slave to time. At 8:18 P.M. he's still tied to his drafting table laboring over his schematics and documentation. On the other hand, George Kramer has mastered time. He creates perfect schematics on his IBM-PC in a fraction of the time it takes Max to do it the old way. Then, his system automatically prints accurate Net Lists, Lists of Materials and other essential documents. As a designer, George is up to 5 times more efficient than Max and, at 4:51 P.M. he's ready for a night on the town with his best girl.

The Secret: FutureNet's DASH-1 Schematic Designer

DASH-1 is an amazing add-on package that converts any IBM-PC into an ultra-modern schematic designer. At the heart of the system is an expandable Parts Library which has hundreds of TTL, microprocessor, memory/support chips, and discrete component symbols — complete with pinouts and pin functions. With a keystroke you can display these symbols on screen and, using the mouse, move and interconnect them to complete your schematic in about one-fourth the time previously required. Incredible, but true!

Good-bye Documentation Errors

Not only is the design process accelerated but DASH-1 also insures accurate support documentation. That's because design data is captured automatically and key documents such as Net Lists, Lists of Materials, and Design Check Reports can be printed at will. No more frustrating error-prone manual documentation that exhausts your time — and your patience as well.



DASH-1 Talks to Other Systems

DASH-1 can interface with other computers or CAD systems too, transferring all of your schematic data in a flash. Direct connection to VAX's or PDP-11's is especially easy.

The $5980.00 Miracle

DASH-1 is the modern cost-effective way to create schematics and documentation. Best of all, a complete add-on package for your IBM-PC is only $5980. Turn-key systems are also available, including the IBM-PC or the new IBM-XT with 10 Mb Winchester hard disk and printer, at prices starting at $12,960. So don't live in the past. Step up to the FutureNet DASH-1, and become far more efficient.

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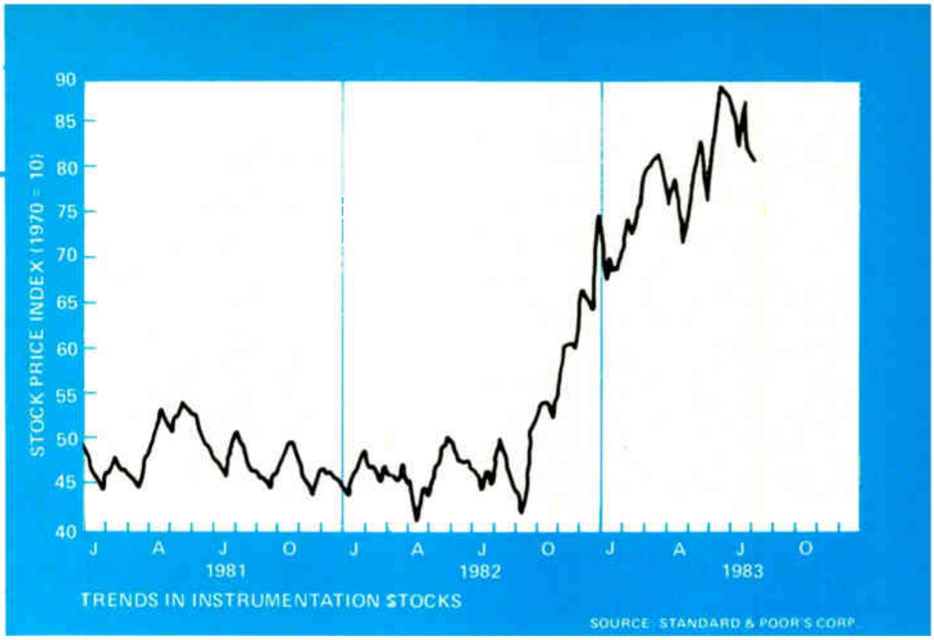
Business activity

"Trends in instrumentation stocks" records the stock market activity of a selected group of publicly owned manufacturers of test, measurement, and analytical instrumentation. The index weights the companies by size and therefore reflects their relative performance.



The strength of the U. S. dollar, compared with other currencies around the world (see chart and box on following page), has come in for renewed attention, as evidenced by recent governmental interventions in the foreign currency market. However, companies that do business overseas know that "it's not a new problem," as a spokeswoman for *Hewlett-Packard Co.* observes. The dollar "has appreciated about 23% over the last three years compared with our major trading partners," notes Kent Webb, an economist with *Gnostic Concepts Inc.*, Menlo Park, Calif.

One problem with the dollar's high valuation is that it hurts U. S. companies' ability to compete in foreign markets. As with other American firms selling abroad, HP sets prices based on the dollar. "When the dollar goes up, it takes more francs or Deutschemarks or yen to cover the cost. So our prices go up and it hurts us competitively," says the source at the Palo Alto, Calif., firm. In addition, foreign-made goods seem more attractive to U. S. consumers because the dollar prices of these products are lower than those of comparable American products. "There is no question that exports [from the U. S.] look much bleaker this year because of the dollar," Webb notes. "The trading balance is going to be dramatically negative." He believes the strong dollar and its stifling of exports is "dampening the recovery of the electronics industry."

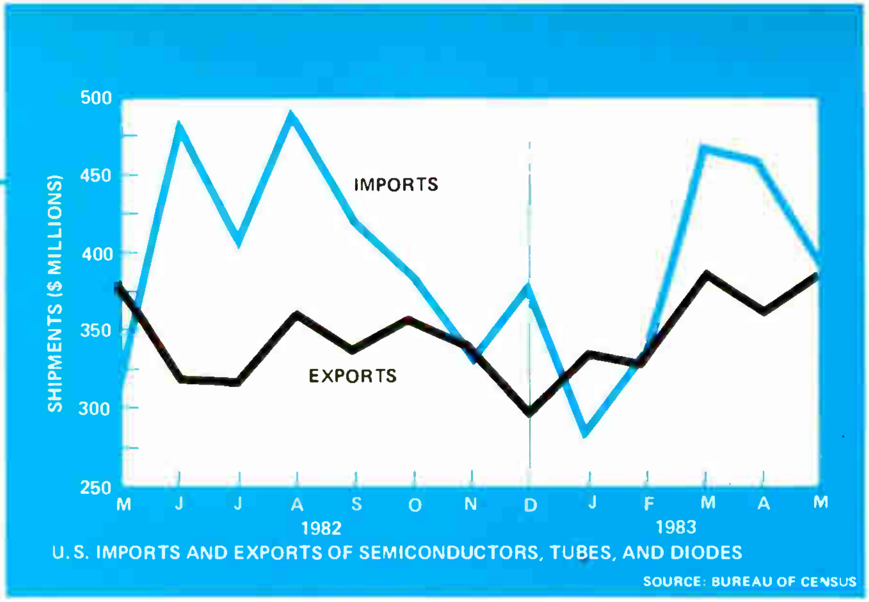
One solution for U. S. firms is to move their production facilities offshore, so that their products will be relatively cheaper than comparable American-made items. However, doing so weakens the U. S. economy because offshore production means sacrificing jobs in the States. High interest rates in the U. S. are responsible for the strength of the dollar, economists point out, and the one way out of the bind would be a substantial drop in those interest rates. Given a projected U. S. budget deficit of about $190 billion, this solution does not appear imminent.

Financings . . . Fort Lee, N. J.–based *Auragen Systems Corp.* has received $10 million in its latest round of financing. The firm is developing a 32-bit, fault-tolerant superminicomputer . . . . An initial round of venture-capital financing has raised $2.3 million for *Entrepo Corp.*, a Sunnyvale, Calif., maker of storage peripheral equipment. . . . Westford, Mass.–based *Tabor Corp.* has raised $6.3 million in its third round of financing. The firm makes memory storage peripherals, including a 3¼-inch microfloppy-disk drive.

–Robert J. Kozma

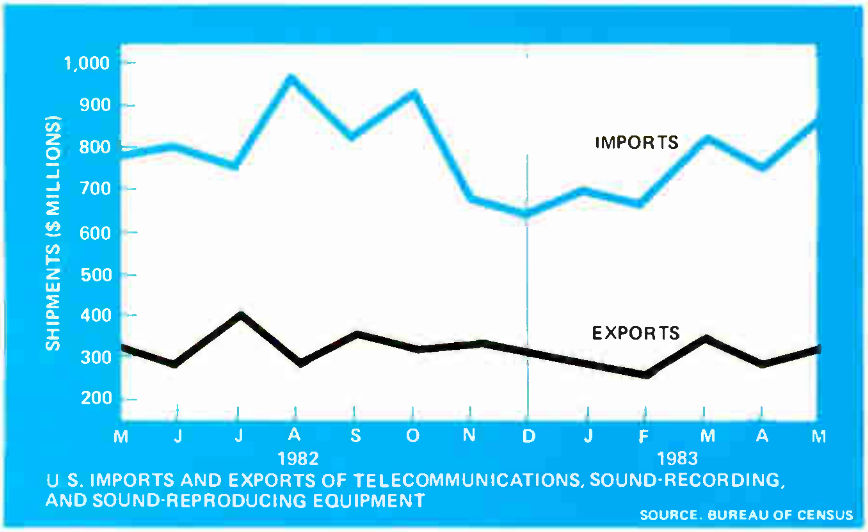
Business activity

Two of the accompanying charts (right upper and right lower) illustrate movements in the imports and exports of some selected U. S. categories of electronic equipment and supplies from May 1982 through May 1983. Also shown (second from bottom) are the changes in value of two dominant international currencies—the Japanese yen and the West German Deutschemark—in relation to the U. S. dollar from June of last year through June 1983. Last come the values of a selection of other foreign currencies in relation to the dollar. The data on monthly U. S. electronic imports and exports, the U. S. electronic-components producer price index, and U. S. economic indicators will appear in the issue of Sept. 22.



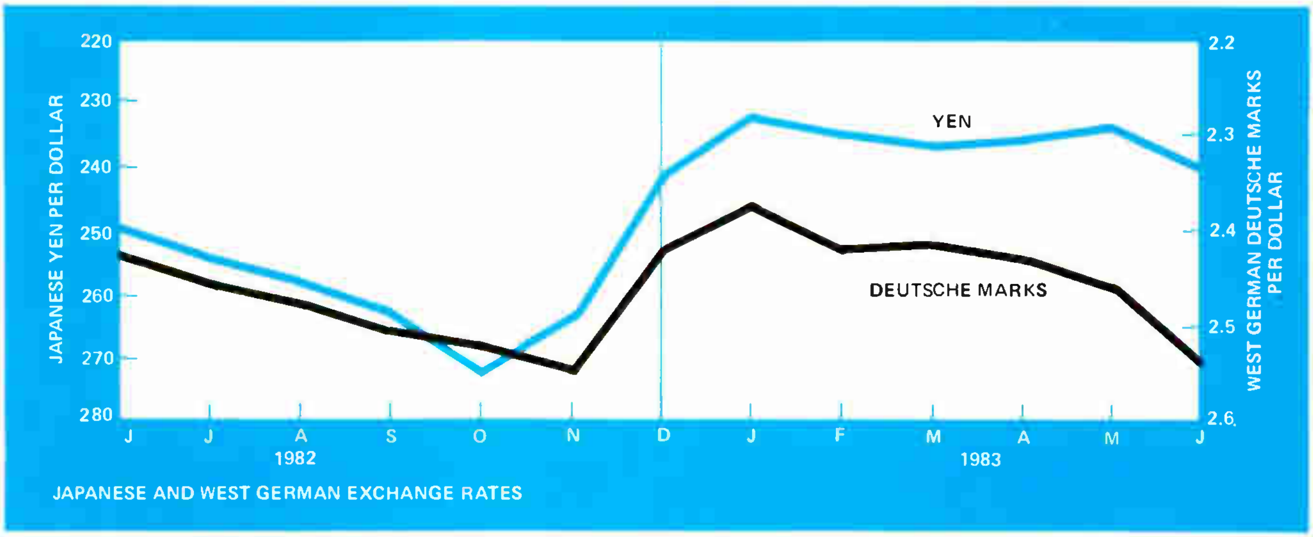
U. S. IMPORTS AND EXPORTS OF SEMICONDUCTORS, TUBES, AND DIODES

SOURCE: BUREAU OF CENSUS



U. S. IMPORTS AND EXPORTS OF TELECOMMUNICATIONS, SOUND-RECORDING, AND SOUND-REPRODUCING EQUIPMENT

SOURCE: BUREAU OF CENSUS



JAPANESE AND WEST GERMAN EXCHANGE RATES

SOME OTHER EXCHANGE RATES

	June 1983	May 1983	June 1982
British pound	0.646	0.636	0.569
French franc	7.6621	7.4163	6.5785
Swiss franc	2.1123	2.0572	2.0789
Canadian dollar	1.2323	1.2292	1.2756
Hong Kong dollar	7.180	7.143	5.915
Taiwanese dollar	39.970	39.970	38.950

If you don't find the logic
you probably don't need

Meet the logic analyzer family that spans a wide spectrum in design. It's a family you can rely on in hardware design, software test and debug and even system performance analysis. One that's equally at home testing and troubleshooting low-cost single processor designs or sophisticated multiprocessor systems.

You can choose from a wide selection of different logic analyzer configurations with HP. And when you do, you'll have an analysis solution that can help accelerate your design cycles...and speed your products to market.

The 1630A and 1630D...for confidence in tackling the day-to-day logic problems.

Choose one of these logic analyzers and you'll have the combined power of timing, state, and software performance analysis in one convenient, low-cost instrument. At just $8,600*, the 1630A gives you 35 channels of state/performance analysis (to 25 MHz), or 8 channels of timing (to 100 MHz). In the interactive measurement mode, it delivers 27 channels of state and 8 timing.

For $10,630*, the 1630D offers 43 channels of state/performance analysis or 16 timing. In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing.

As your primary tool in hardware test and debug, the 1630 provides new triggering power to help you isolate the source of timing errors. This includes pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. This is the capability that helps you quickly solve difficult hardware problems such as timing errors, transient effects and handshake malfunctions.

Use the 1630 in software development and integration phases and you have sequencing, triggering, store qualification, and sequence restart power to isolate targeted areas of code and view just the measurement information you desire.

To optimize your system performance, the 1630 gives you a nonintrusive view of system software in action. One that lets you analyze system activity at the level of procedures and tasks instead of the instruction level. Histogram displays make it easy to spot software bottlenecks and inefficiencies. The result can be improved system performance, and a more competitive product...with minimal additional design effort.

The 1630 also gives you interactive measurement capability for greatly enhanced analysis power. The ability to cross arm and trigger between state and timing analyzers helps you get to the problem source quickly when the difficulty could be either a hardware or software malfunction.

Throughout the development cycle, you'll find the 1630 easy to use. That's because menus simplify operation. Label assignments let you view results in your system's terminology. And inverse assembly, via low-cost peripherals, displays listings in familiar target microprocessor mnemonics.

The 64110A...a configurable analyzer that can handle those complex problems found in multiprocessor environments.

This logic analyzer is, in reality, a number of different analyzers, depending on how you configure it. For example, it can be a standalone timing analyzer with 8 or 16 channels.

It can also be a standalone state analyzer with up to 120 channels. You can combine timing and state with performance overview. Or, combine multiple state or timing analyzers in the same station.

Price for the 64110A,

analyzer you need here... a logic analyzer.

including a 60 channel state analyzer subsystem with performance overview is $21,870*.

Put the 64110A to work in the hardware test and debug phase and you can allocate high speed timing resources. For example, you might choose sampling speeds to 400 MHz. The resulting 2.5 ns resolution lets you make high-resolution measurements to resolve timing margin problems.

In addition, the timing analyzer provides new triggering capability. The dual threshold mode lets you trigger on marginal signal levels, which helps you spot excessive fan-out, bus loading problems, and slow transition times. Other trigger modes include time qualification of pattern triggering, sequential triggering, pattern triggering ANDed with a transition or glitch, glitch triggering, plus other modes that simplify the analysis of handshake problems.

In software test and debug, the 64110A gives you unequalled tracing, triggering, and store qualification power. With its master enable function, 16-level sequencer plus 8 user-definable terms for trigger, store qualification and count functions, you'll have little trouble locating the specific portion of code you want and displaying only the information of interest...even in the most complex multiprocessor software.

For system performance analysis, the 64110A gives you a nonintrusive view of software in action in the form of histogram and graph displays. The histogram modes provide a fast way to locate system bottlenecks and identify inefficient portions of software. These display modes help you identify a processor stuck in a loop, see where software went into the weeds, or spot activity occurring in a forbidden area. A graph mode shows software performance data in chronological order.

Interactive measurements between all analyzer subsystems multiplies the power of the 64110A far beyond the capability of other logic analyzers. Cross arming and triggering between any of the analyzer subsystems helps identify the source of difficult hardware/software interaction problems, and resolves hardware/software fingerpointing issues.

In any phase, the 64110A is a pleasure to use. Directed syntax softkeys guide you through setups and measurements with a minimum of keyboard entries. Symbolic tracing means you interface with the analyzer using terminology you're familiar with. And preprocessors with inverse assemblers let you view measurement results in familiar processor mnemonics. All of which lets you concentrate on the problem you're trying to solve...not the analyzer.

Choose both and you'll have your analysis needs covered.

When you combine both of these analyzers in your lab, you have a cost-effective solution to the day-to-day test and debug tasks, plus the power to deal efficiently with those complex troubleshooting jobs.

So before you buy any logic analyzer, be sure you explore the individual power of HP's standalone analyzers...and the synergistic effect of a combination of instruments.

For complete details, call your local HP sales office listed in the telephone directory white pages. Ask for an HP field engineer in the electronic instruments department.

*U.S.A. list price only.

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Bubble Machine.

This Nicolet digital scope can put a waveform in your pocket.

The two-channel 3091 offers the traditional advantages of a Nicolet digital storage oscilloscope in a compact portable package. The quartz crystal timing, precise A/D conversion and alphanumeric display combine to overcome the accuracy limitations of the analog oscilloscope. Its high resolution and 1MHz digitizing rate make it ideal for field calibration, fault diagnosis or transient analysis in mechanical, electrical, acoustical and biological applications.

Signals can be viewed live, stored for closer examination or compared in real time to previously stored references. Waveforms can be expanded, interrogated by cursor, output to pen recorders or even transmitted to a computer at the touch of a button. Important data can be stored on the optional magnetic bubble cassette for instant recall in either your 3091 or someone else's.

The 3091 is a digital storage oscilloscope, a transient recorder and a chart recorder all in one, easy-to-use instrument.

To find out how you can put digital precision in your pocket, call 608/273-5008 or write: Nicolet Oscilloscope Division, 5225 Verona Road, Madison, Wisconsin 53711.

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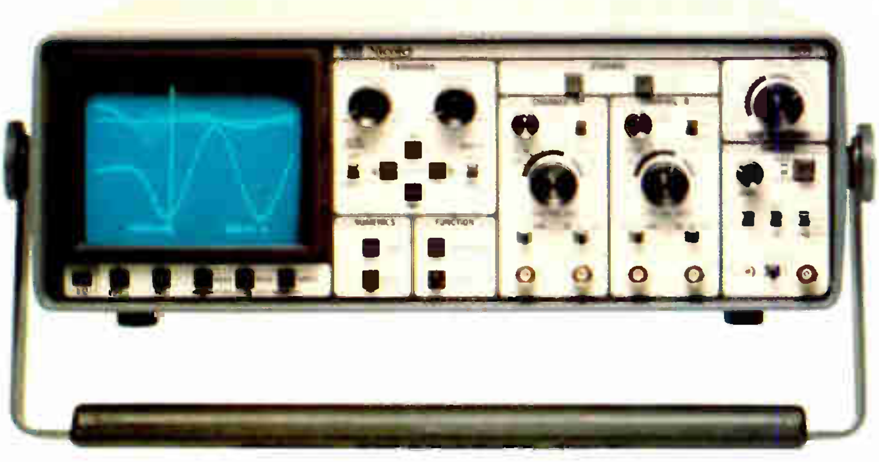


Nicolet

* U.S. domestic list price. Bubble cassette option additional at $1,500.

Circle 40 for more information

Electronics newsletter

MCC recruitment hits a snag

Recruiting for the new industry research cooperative, Microelectronics & Computer Technology Corp. (MCC), has been going so slowly that president Bobby R. Inman says it may miss its original goal: beginning actual research by Dec. 1. **MCC now has just eight employees while its 11 co-owners decide which of their researchers will be asked to join it** in Austin, Texas. There will be new hires, too, but MCC is not using professional recruiters, Inman pointed out last week during a stopover at Los Alamos, N. M.—he was keynote speaker there at a conference on supercomputers, whose builders will need the advanced components the research group will design. Inman said the cooperative has budgeted $28 million for use this year in Austin and $5 million more at Texas A&M University. In addition MCC will spend $750,000 in each of the next 10 years to support graduate students in computer science.

Industry, unions split on call for revelations of hazardous substances

Observers in the U. S. electronics industries are keeping their eyes on a political battle in Massachusetts over hazardous substances in the workplace and in the environment. The state AFL-CIO and its consumerist allies have filed a petition to place an initiative for stringent right-to-know regulations on the ballot in November 1984. But the Massachusetts High Technology Council Inc. and the Associated Industries of Massachusetts are seeking signatures **in support of a less strict measure.** Among the divisive issues: the substances that would be deemed hazardous, labeling requirements, ease of community access to corporate files, and the extent of protection for trade secrets. If the voters approve one or the other, it will become law.

Sandia says its 16-K RAM can withstand 1 megarad

At Sandia National Laboratories, in Albuquerque, N. M., designers have come up with what they say is the first very large-scale integrated circuit that can withstand the high radiation in space or of a nuclear explosion. **The complementary-MOS 16-K static random-access memory measures 0.6 by 0.4 cm and contains more than 100,000 transistors.** Its designers say it can function after a total exposure of 1 megarad. (Usually, 1,000 rads is fatal to humans.) The chip, which has been tested successfully, will be sold by Harris Corp.'s Semiconductor sector, in Melbourne, Fla.

TI starts shipping NuMachine work station

Texas Instruments Inc.'s Data Systems Group, in Austin, Texas, has quietly begun shipping limited quantities of its NuMachine-based engineering work station to selected customers "for experimental development" purposes. Stemming from development work at the Massachusetts Institute of Technology and licensed from Western Digital Corp. [*Electronics,* Feb. 10, p. 41], **the NuMachine is expected to find primary application in artificial-intelligence applications.** One recipient of the first shipments is Lisp Machine Inc., of Culver City, Calif., which has just introduced its Lambda Machine, based on NuMachine hardware and touted as an artificial-intelligence development system that offers virtual memory for writing microcode. Priced at $72,500, Lambda also features a Lisp-language microcode compiler. In a related move to beef up its involvement in emerging artificial-intelligence markets, TI said last week that it had purchased

25% of Lisp Machine for an undisclosed price. The firm declines to say when its NuMachine system, developed and being produced in an Irvine, Calif., facility, will be placed on the open market.

Semicon/East to feature sessions on materials

Semicon/East's organizers, who deplore what they regard as an information gap on the subject of materials, will spotlight that area at this year's session of the production-gear conference, in Boston, Sept. 20–22. "Materials coverage in the past has been pretty sketchy, and users are not fully aware of some of the materials capabilities now available," explains technical-program chairman Joseph Monkowski, of Pennsylvania State University. One highlight will be a report from Airco Industrial Gases, of Murray Hill, N. J., about producing ultrapure silane and disilane. **An epitaxial silane layer on silicon has a resistivity of 10,000 ohms-cm,** as well as improved carrier mobility and lifetime. Ultrapure silane will be especially important as a raw material for very high-speed integrated circuits, whose great packing densities require that trace-metallic contaminants be eliminated more effectively.

Meeting aims to nudge voice systems out of lab

In hopes of spurring the march of speaker-independent voice recognition out of the laboratory environment and into the real world, Voice Control Systems Inc.—a Dallas-based research and development firm—is hosting a "Robustness in Speech Recognition" meeting in Santa Barbara, Calif., Nov. 2–4, **with a list of over 20 speakers who are considered experts in their fields.** The conference will look at a number of challenges still facing the technology, such as background noise and electrical noise in communication channels.

Addenda

After a 2½-year delay, National Semiconductor Corp. is resuming construction of a 290,000-ft² wafer-fabrication facility in Arlington, Texas, west of Dallas. **The facility—slated to begin limited production in 1985 and employ 1,500 late in the decade—**will initially produce complementary-MOS components. The Santa Clara, Calif., firm halted construction two years ago because of depressed worldwide chip demand and is resuming it because of strengthening order rates (see p. 105). . . . While other home-computer makers lose money, Commodore International Ltd., of Norristown, Pa., **reports its profits in the quarter ended June 30 were $26.7 million, compared with $16.3 million a year ago.** . . . Defense-electronics behemoth Hughes Aircraft Co., El Segundo, Calif., has filed suit in U. S. District Court in San Francisco against Intel Corp., Santa Clara, Calif., **charging infringement of three Hughes patents for semiconductor manufacturing.** One of the patents covers ion implantation, a key processing step in wafer fabrication. An Intel statement professes surprise at the suit in light of continuing negotiations in the matter and vows a vigorous defense. . . . After a three-year testing of the waters, **General Electric Co. is expanding its efforts in the telecommunications distribution market.** The Fairfield, Conn., company will open 12 sales offices to sell and lease private automated branch exchanges. . . . The latest intelligence in the continuing drama, "Waiting for the IBM Peanut," has it that the low-cost version of the Personal Computer **is already being shipped to Europe** and will reach the U. S. market next month.

The World's Most Elegant Microprocessor Family is Banishing Current Benchmarks to Computer History.

Be advised: the NS16000 family is establishing all new benchmarks for 8-, 16-, and 32-bit microprocessors.

Here is proof beyond doubt that any NS16000-based product will outperform any other microprocessor-based product.

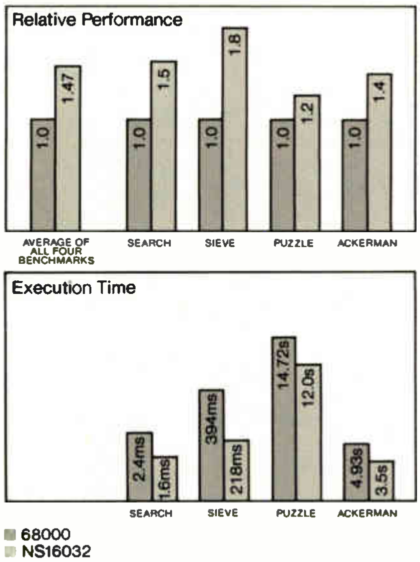
Of course, comparing the NS16000 family and the microprocessors your competition is banking on is difficult—perhaps even irrelevant—because the NS16000 family is, fundamentally, much more advanced.

No other commercial processor (micro, mini *or* mainframe) is designed to fully support the use of high-level languages. All members of the NS16000 family of CPUs[1] however, feature not only 32-bit internal architecture, but also a high degree of regularity in the arrangement and use of their 32-bit registers. Data can be read or written 1, 8, 16, or 32 bits at a time, as sophisticated programs require, and transfers from one register to another are not restricted.

Moreover, the symmetrical instruction set of the NS16000 CPUs includes over 100 genuine two-operand instruction types, but avoids special-case instructions that compilers cannot use. All instructions can be used with the addressing modes common to most microprocessors (register, immediate, absolute, and register relative), as well as with powerful HLL-oriented modes that only the NS16000 offers: top-of-stack, scaled indexing, memory relative, and external. And any operand length and any general-purpose register may be used with any mode.

The combination of these virtues makes it possible to write especially lean high-level language programs on NS16000-based systems. The simplicity with which a programmer can implement a compiler, for instance, is matched only by the compiler's increased speed of execution. In effect, the dream of being able to pack the enviable working environment and performance of a large computer into a microprocessor has become reality.

HIGH-LEVEL LANGUAGE COMPARISONS[2]



Putting large-computer performance into a microprocessor is further advanced through the implementation of the NS16000's Demand Paged Virtual Memory—a strategy equivalent to that used in such systems as the VAX-11 series and all present IBM mainframes.

With an architecture that supports uniform addressing, the NS16000 is the first commercial microprocessor able to feature Demand Paged Virtual Memory as a means of solving large-memory-management problems. As a result, an NS16000-based system, blessed with this completely flexible memory configuration, can maximize the use of its physical and virtual memory resources and achieve a level of performance heretofore unrealized.

With the NS16082 Memory Management Unit (MMU), only the information most recently used is kept in RAM: other information is swapped in and out from mass storage, as needed. Consequently, each programmer, each program, each task has access to a uniform addressing space of 16 Mbytes simultaneously and independently, without reservation or special exception. (And more efficiently than on any other commercial processor—micro, mini, or mainframe.)

Among the reasons for the MMU's prowess is its support of a *two-level* page-table translation, whose process is speeded up by an associative on-chip cache. Utilizing a very fast Least-Recently-Used (LRU) algorithm and a powerful "referenced bit," the NS16082 MMU achieves a translation cache hit rate of over 98 percent.

The NS16081 Floating Point Unit (FPU) extends the NS16000 instruction set with very high-speed floating-point operations for both single- and double-precision IEEE operands.

Designing the FPU into a system allows programmers to treat floating-point numbers as they would any other data types, and to use any of the addressing modes to reference them. For example, the scaled index mode permits an array of floating-point data elements to be addressed by its logical index, rather than its physical address. The power this can add to a system makes it especially applicable for graphics and engineering work-stations.

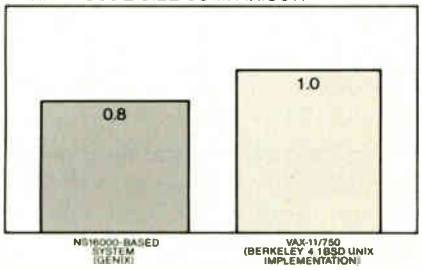
FLOATING POINT OPERATION COMPARISONS[3]

With the introduction of National's proprietary GENIX™ operating system, even the advantages of using UNIX® on a large computer have been ported to the NS16000 microprocessor family.

GENIX is an elegant implementation of the proven Berkeley 4.1 bsd version of UNIX. Created in-house, to facilitate the development of software for NS16000-based applications, it is the first UNIX operating system to support Demand Paged Virtual Memory in a microprocessor.

Here, then, is a demonstration not only of the pure functionality of the NS16000 family architecture, but of the large-computer-like results now possible on a microprocessor-based system using GENIX.

KERNEL CODE SIZE COMPARISON



When you consider applications for the NS16000 microprocessor family—from elegant personal and business computers, to graphics work-stations, to industrial control systems—keep in mind that:

1. The NS16032 CPU and the NS16201 TCU are in production now.
2. The NS16082 MMU, the NS16081 FPU, and the NS16202 ICU are being sampled now.
3. Evaluation tools are available now.
4. Development tools are available now.
5. Training classes are in progress now.
6. Third-party software for the family is available now and increasing daily.
7. The software you write now will work *without modification* if you move your product line from one NS16000 CPU to another in the future.

   Similarly, the optional use of the NS16000's MMU and FPU slave processors—integral parts of the NS16000 architecture—will allow you to determine price/performance trade-offs while preserving your initial software investment.
8. Only the NS16000 family can make it possible for you to put a large-computer-like product on the market today—at microprocessor prices.

Footnotes:

1.
The NS16032 CPU, the first of the NS16000 CPUs, has a 16-bit-wide data path to memory and 32-bit internal architecture. Before the end of this year, CPUs implementing the same 32-bit internal architecture, but with 8- and 32-bit-wide data paths to memory will also be available, to allow maximum price/performance flexibility within your product line.

2.
Results for the 68000 were taken from *Computer Architecture News*, Vol. 10, No. 4, June 1982, pp. 17-28. The 68000 was run at 10MHz, with no Wait States. Source programs in Pascal.

Results for the NS16032 were obtained on a DB16000 at 10MHz, with no Wait States. Source programs in Pascal. All variable sizes are 32-bit.

3.
Results for the 68000 were obtained on a SUN System at 10MHz, with no Wait States, using Motorola's ROM-based floating point subroutine package.

Results for the NS16032, utilizing the NS16081 FPU, were obtained on a DB16000 at 10MHz, with no Wait States. IEEE floating point, variable sizes.

Results for the VAX-11/750 were obtained without using floating point accelerator.

NS16000

Elegance is everything.

See it.

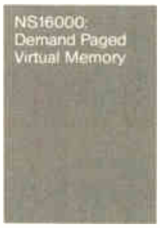
The NS16000 microprocessor family will be on exhibition at WESCON.

Talk with us.

Please call the National Sales Representative nearest you for more information, and the answers to your questions. Ask to meet with one of our Field Applications Engineers, too. Or, circle the number below.

Read about it.

You haven't heard the last word on the NS16000 microprocessor family yet. In the meantime, you may want to further your understanding of what we've accomplished by requesting copies of *NS16000: Demand Paged Virtual Memory* and *NS16000: Benchmarks*.



National Semiconductor

MICROCOMPUTER SYSTEMS DIVISION

Circle 45 on reader service card

In head-to-head comparison, there's really no comparison. Our OS4040 stacks up best.

The Gould OS4040 digital storage oscilloscope vs. the Philips PM3310 and Tektronix® 468.

The right balance between sampling speed and detail, for accurate measurement. The faster sampling rates of the Philips and Tek units don't mean much without supporting memory. The Gould OS4040 can capture and store 5,120 words on a single waveform compared with 256 for the PM3310 and 512 for the Tek 468. That means the OS4040 can expand a stored trace by 50 times horizontally and still give you 100 data points across the screen. Under the same circumstances, with Philips' 256 words you would get only 5 actual data points. Tek would give you 10 data points. For a detailed display, the OS4040 is the clear winner.

Fast capture of sequential signal events, as in digital logic circuits. The OS4040 can capture up to four signals from a single channel and hold them in separate storage for later analysis. It does this with direct store access at up to 10 MHz. While the Philips can capture the signals, it requires considerably more time between the capture of each event since it can only access its store via a 78 kHz ADC from its CCD line. Tek can only capture up to two sequential events from a single channel.

The most flexible interface facilities. Only the OS4040 can copy captured waveforms onto a chart recorder from both channels simultaneously, and is able to plot one signal against another, for example, as in hysterisis curve plotting. The PM3310 and the Tek 468 can only output one channel at a time.

The OS4040 can "baby-sit" for you. It has a "baby-sitter" mode, so each signal captured can be automatically transferred to the chart recorder, and the store re-armed for the next signal event. the PM3310 offers neither repetitive analog output nor a "baby-sitter" mode. And while the 468 provides an analog option, it is not capable of "baby-sitting."

Exclusive direct digital user port. Even though all three systems offer an IEEE output, only the OS4040 offers a direct digital user port as a standard option for situations where the IEEE is too slow for the buffer store to be cleared before the next signal capture.

The Gould OS4040 digital storage oscilloscope. For the whole story, contact Gould Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279. Nationwide (800) 538-9320. California (800) 662-9231 or (408) 988-6800.

GOULD
Electronics

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Fancy architecture, standard logic lead to fast minicomputer

by Larry Waller, Los Angeles bureau

Two ALUs operating in parallel help create 2-MIPS processors in upcoming multiprocessing 32-bit superminicomputer

Even seasoned computer buffs should be awed by the speed of a 32-bit superminicomputer nearing completion at an Irvine, Calif., computer architecture and design firm. In benchmark whetstone testing, the machine demonstrates a speed of more than 2 million instructions per second for each of up to four processors available with the system, says Alan D. Kraemer, engineering vice president of Technology Marketing Inc. That is about twice the rating of a single-processor VAX-11/780 from Digital Equipment Corp., a standard of comparison in the supermini field.

Architectural rather than circuit ingenuity is what lifts the machine to those heights. It relies on standard rather than custom chips and high-speed Schottky logic families instead of more expensive and heat-producing emitter-coupled logic. ECL's high power dissipation and cost were found to vitiate its speed advantages.

Such a design will certainly lead to a cheaper computer, although Technology Marketing will not quote a price. Its machine was developed under contract to a customer, identified by Kraemer only as a major computer manufacturer, for delivery for software integration at the end of October and market introduction—and pricing—toward year-end.

"Pushing a 32-bit machine to this speed demands a host of architectural changes, principally to produce a 100-nanosecond cycle time for the ALU [arithmetic and logic unit]," says Kraemer. Most important, the firm employs two parallel ALUs in place of the customary single unit (see diagram). This obviates an entire functional step normally required to buffer, propagate, and generate outputs from a bit-slice ALU to the look-ahead–carry generator.

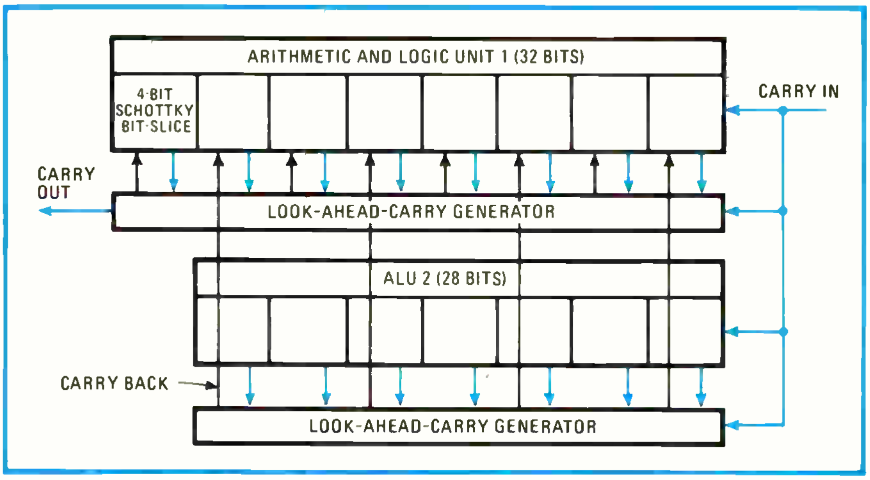
Instead of a buffer, the second ALU handles only the look-ahead–carry operation, the most time-consuming. This means anticipating and adding the carry digit to the next higher bit position when two digits are added and their sum exceeds one bit position.

"Elimination of the buffer knocks off 15% to 25% of ALU propagation delay time," explains Kraemer. The primary ALU performs the usual arithmetic jobs—adding, subtracting, and dividing—along with conventional logic comparisons.

Operation of the parallel ALUs required a microsequencer structure that allows simultaneous access to two instructions during one 100-ns microcycle. Both instructions are accessed at the same time, and selection between them is made only at the cycle's end. This technique dodges using an extra microcycle to set up test conditions for logic-signal execution, the usual method.

Another change that speeds operation takes the writable control-memory bits from a separate store, putting them physically as close as possible to their associated logic. "A tricky move that sprinkles memory all over the place, it still looks the same to the computer," Kraemer notes. The result chops access time by 5 ns for each signal transmission.

Finally, the logic architecture is also revamped, with the design relying on the high speed of separate multiplier chips to relieve the ALUs



Look Ma, no buffer. Two ALUs work in parallel in the central processing unit of the 32-bit minicomputer. Normally, a bit-slice ALU needs a buffer between it and the look-ahead–carry generator. Here, a second ALU produces propagate and generate outputs for a second look-ahead–carry generator. Faster than buffering, the result is an overall ALU speed of 100 ns.

of fixed- and floating-point arithmetic number crunching. A 32-bit multiplier provides a 64-bit product every 100 ns in a pipelined operation, a task vital in handling complex transcendental functions, says Kraemer.

The new machine brings together innovations till now demonstrated only individually and at much less complex levels, Kraemer continues. "Using all of them is the ticket," he says. "Without even one, the whole thing falls apart."

Since its founding in 1969 as a core-memory house, Technology Marketing has gone on to design more than 50 computer systems for its clients. It had revenues of nearly $8 million in its 1983 fiscal year.

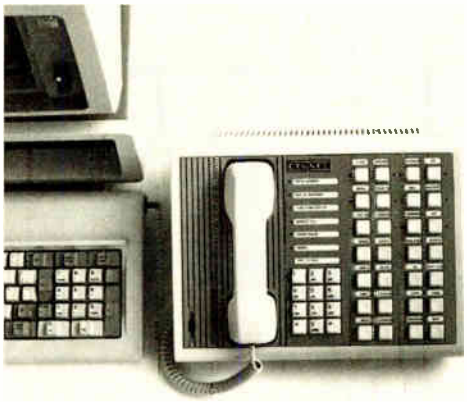
Work stations

Personal Computer gets executive look

A personal computer is one thing, an executive work station—with its special functions—a more expensive something else. But the boundary is blurring, especially now that a California start-up company, Cygnet Technologies Inc., has come up with a combined communications computer and intelligent phone that extends the cheaper machine's usefulness.

The Sunnyvale firm's Communications CoSystem (see photograph), for the popular IBM Corp. Personal Computer and its compatible look-alikes, provides many communications and management functions that the basic PC does not. The combined system can perform such intelligent telephony functions as finding and dialing phone numbers, teleconferencing with voice and text simultaneously, electronic mail, and terminal emulation for getting data from other computer systems. It also records communications activities.

The CoSystem does all these things without interrupting the PC's normal operation. Says Cygnet president and cofounder, Federico Faggin: "It is the other half of the PC." When it becomes available at computer retail stores, in September, nothing in the market will compete with it directly, he asserts.



Executive plug-in. Combination communications computer and intelligent telephone from Cygnet Technologies plugs into an IBM PC to give it the enhanced capabilities of an executive work station.

Some have it. Some of its functions can be performed by other devices, however. For example, modem and communications boards have been designed expressly for the PC, and integrated voice-and-data-communications terminals for executives have been provided by such companies as Tymshare Inc., Cupertino, Calif. (the Scanset); Northern Telecom Inc., Nashville, Tenn. (the Displayphone); and Texas Instruments Inc., Dallas (the newest portable Silent 700 terminals).

At $1,495 for the CoSystem with a 300-baud modem, plus $3,000 or more for a Personal Computer with a minimum of 128-K of memory, the package costs much less than executive work stations, like the $17,000 Xerox Star and Apple Computer's $10,000 Lisa. Though not exactly comparable, these work stations do provide a price ballpark. The Star terminal has greater capabilities but must be connected to other processors through an expensive Ethernet system. The Lisa does less than the CoSystem in communications but is a more powerful personal computer.

Easy to install. CoSystem simply plugs into the PC's RS-232 port. Its real-time executive links up with the PC DOS operating system, which, without stopping or interfering with the current program, passes communications jobs to CoSystem's executive. For example, the VisiCalc spreadsheet and electronic mail could run concurrently.

Much to the delight of Cygnet's founders, the explosion in personal computers goes on. It now seems that by the end of 1983 there will be an installed base of 2.5 million, growing at a rate of 1 million a year—a potential pot of gold to the firm. Aided by Merrill Lynch Venture Partners I, of New York, Faggin and cofounders Jerry A. Klein and Lauren F. Yazolino began by raising $2 million last June. One year later, about when a prototype was ready, $7 million more was raised.

A pioneer in integrated circuits, Faggin helped design the world's first microprocessor, the 4-bit MCS-4, at Intel Corp. He is also credited with two other Intel microprocessors, the 8008—the first 8-bit microprocessor—and the very successful 8080. In 1974 he helped found Zilog Inc., where he originated the Z80 microprocessor family, which he is using in his new machine. Before Cygnet, he was vice president of Exxon Corp.'s Computer Systems Group, which had become Zilog's parent.

Klein, Cygnet's vice president for marketing, was a founder of Ansonics Corp., later to become part of Dictaphone Corp., where he developed one of the first telephone-answering machines, the Ansafone. He then moved to Exxon Enterprises and the team that developed the Qyx electronic typewriter. Yazolino, vice president for engineering, helped found Two-Pi Corp., where he directed the development of an IBM-compatible mainframe. –**Tom Manuel**

Data processing

Coprocessors juggle specialized tasks

Whether it is called multiprocessing or coprocessing, the architectural scheme that outfits the same computer with different types of microprocessor chips tailored for different tasks is catching on. Aimed at the multitasking- and multiuser-minicomputer business, several machines with the new design have come to market in the past few months.

Two of the first were the Megaframe, from Convergent Technologies Inc., and the Omnix 186, from Computer Automation Inc., both unveiled in May at the National Computer Conference. This summer sees them joined by still others: the Desktop Generation series, announced last month by heavyweight minicomputer maker Data General Corp. and CompuPro's MultiPro Model MP 10, due in September. Other firms are known to be readying units as well.

The best. It is clear why so many are rushing to the well: the superior features of different microprocessors can be combined in a single machine. At Convergent Technologies, in Santa Clara, Calif., for example, few tradeoffs had to be made. "The best chip in the case of MegaFrame turned out to be two chips, Motorola's 68010 and Intel's iAPX186," says Steve Blank, marketing director for the Data Systems division.

For CompuPro, the best microprocessor combination for its four-user MultiPro MP 10 was an 8-megahertz Intel iAPX88 16-bit main processor teamed with four 6-MHz, 8-bit Z80Bs [*Electronics*, July 28, p. 156]. Thus standard software for 8- and 16-bit machines can be used simultaneously.

"We are aiming this at small organizations that have outgrown personal computers—the type of businesses that would buy the IBM System/34, for example," says CompuPro president William J. Godbout. "Our four-user system will cost less than $1,800 per work station—equivalent or less than typical 8-bit personal computers." This is about a quarter of the price of the System/34.

For companies like Data General, Digital Equipment, Honeywell, and Computer Automation, with customer bases that cannot run the newer operating systems and application programs, adding a state-of-the-art coprocessor makes this upgrade possible. Data General, for one, has equipped its Desktop Generation with a pair of tightly coupled processors: its own microEclipse and an 8-MHz Intel iAPX86. The first ensures compatibility with all Data General software, and the second opens up the vast world of personal-computer software available for the Intel 8086–8088 family [*Electronics*, July 28, p. 154].

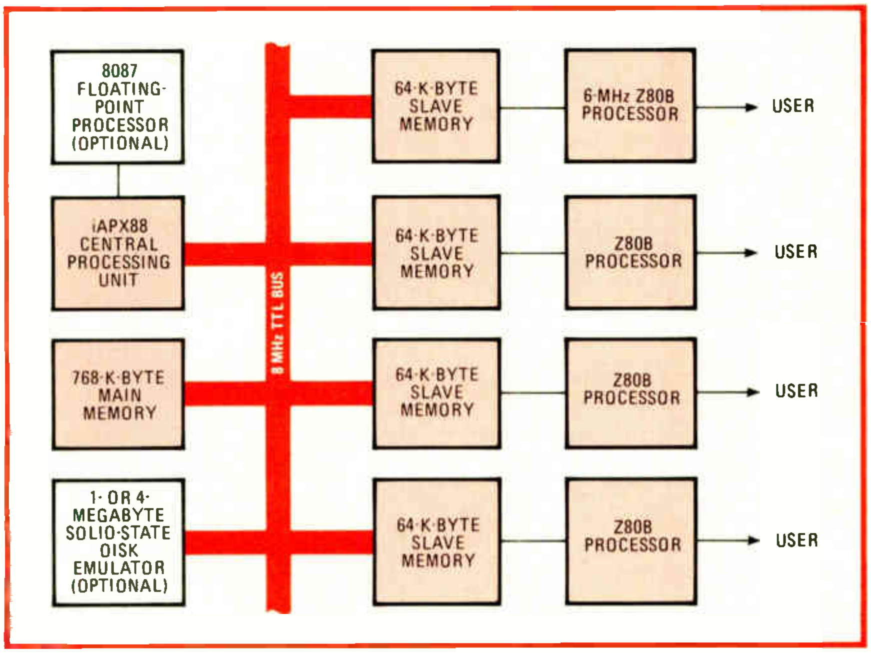
End users are equally attracted by coprocessing, says Al Kraemer, who is engineering vice president at Technology Marketing Inc., Irvine, Calif., a computer-design consultant firm (see p. 47). "Coprocessors let them cover many more bases," he says.

The achievement does not come easily. Writing software to control coprocessing is "an order of magnitude harder than ordinarily," notes Convergent's Blank. Software, using a variant of Bell Laboratories' Unix operating system [*Electronics*, July 28, p. 118], took the lion's share of the design time when his firm developed its Megaframe.

For its central processing unit, Convergent chose the 16/32-bit Motorola 68010, with up to 4 megabytes of dynamic random-access memory. The chip has the 32-bit virtual-memory addressing space needed for the Unix system software to operate most efficiently.

For data storage, file management, and communication with up to 256 peripherals, the Megaframe can have up to 28 of Intel's 16-bit 186s. Convergent ships its first $17,000 machine late this month.

For its part, Computer Automation wanted its Omnix compatible with its older 16-bit Naked Mini 4 systems. Omnix's processor, built around a three-chip custom n-channel MOS chip set available since 1977, handles disk and terminal management, while the 186 deals exclusively with multiple tasks. Both the host processor and 186 operate off the same bus, and extra 186s may be plugged in as peripherals; each Omnix supports up to eight users. The computer sells for $9,000, down to $5,000 in quantity. **–Larry Waller**



Co-workers. Coprocessors, shaded, selected for CompuPro's MultiPro MP 10 computer are the 16-bit iAPX88 for the main processor and 8-bit Z80Bs for interfacing with users.

Memory

Mostek offers 32-K-by-8 RAM

While a dozen chip makers jockey for position in the early rounds of the 256-K dynamic random-access–

memory competition, Mostek Corp. hopes to distinguish itself by breaking with tradition and placing a 32-K-by-8-bit RAM on the market six months ahead of its more conventional by-1-bit design. Temporarily sidestepping the 256-K-by-1-bit part, the unorthodox opening move further underscores the growing attention dynamic-RAM makers are giving to microprocessor-based system markets.

For the 32-K—or 64-K—byte memories typical of low-end computers, a 32-K-by-8-bit dynamic RAM makes for a one- or two-chip system, as well as a convenient increment for expansion. Furthermore, Mostek's MK4856 chip does not multiplex address lines, is housed in a standard 28-pin byte-wide (plastic) package, and incorporates a refresh counter. As a result, it is almost as simple to use as static RAM.

Tradition. In Japan and the U. S., other dynamic-RAM manufacturers are following more traditional paths, introducing 256-K-by-1-bit chips aimed at large-minicomputer and mainframe houses (see "256-K RAM is more than just an upgrade," p. 135). However, these chip firms will not wait long—some less than six months—before making by-4-bit and by-8-bit versions for small-system makers, which last year claimed a majority of dynamic-RAM consumption. Such multibit-wide memories enable designers to cut the chip count in small microprocessor-based computers, thus lowering costs.

In addition to its rarity, the MK4856 32-K-by-8-bit dynamic RAM will be the first U. S.-made 256-K device with quantity pricing when it makes its debut late this year: $100 each in 100-piece orders. Other U. S. makers plan introductions this fall, and Japanese chip firms also continue aggressively showing 256-K prototypes (see "How others shape the 256-K–RAM market," above).

Advantages. Mostek, of Carrollton, Texas, expects its byte-wide RAMs to enjoy a number of advantages, explains Jerry Taylor, volatile-memory development manager. Since it will be a year or two before 256-K-by-1-bit chips achieve cost-per-bit parity with older 64-K devices, Taylor says, the 32-K-by-8-bit RAM will likely thrive in the early premium-pricing rounds because of overall cost advantages for small-system markets. He notes too that these microprocessor-based systems—now the strongest computer segment in the current recovery—have short product development cycles and reach volume production sooner than large systems.

Laser. The MK4856 uses 2.5-micrometer geometries rather than the 2-μm or finer lines employed on other 256-K parts. As a result, the die is a whopping 100,000 square mils, too large to be produced economically without the laser-programmed redundant circuits included on chip for both rows and columns.

The byte-wide part—like Mostek's 256-K-by-1-bit RAM—is being processed in the firm's lightly-doped-drain, triple-diffused MOS technology (L-D^3), now producing sub-100-nanosecond 64-K dynamic-RAMs [*Electronics,* May 5, p. 54]. The 256-K n-channel MOS device is fabricated with a double-metal, double-polysilicon structure instead of the single-metal, double-poly construction of the high-speed 64-K.

The initial 32-K-by-8-bit chip will be available with three access speeds—100, 120, and 150 ns—but it will likely get much faster when the design is scaled down to 50,000 square mils in 1985.

Anticipating that the part will be used mostly in microprocessor-based systems with less than 256-K bytes of memory, Mostek estimates that byte-wide chips will account for 30% of shipments in the lifespan of the 256-K dynamic RAM. Some 30% will go to by-4-bit and 40% to by-1-bit markets. **–J. Robert Lineback**

How others shape the 256-K–RAM market

Although Mostek Corp. will be first to introduce a 32-K-by-8-bit dynamic random-access memory (see accompanying story), a handful of memory makers in both the U. S. and Japan intend to offer 64-K-by-4-bit parts within a year of their initial 256-K-bit-by-1-bit introductions. Backers of by-4-bit dynamic RAMs believe the configuration offers a greater range of system-level memory increments when compared with the byte-wide parts. In addition, the by-4-bit 256-K chips fit in 18-pin packages, rather than the larger 28-pin variety needed for byte-wide nonmultiplexed memories. One of the first firms offering samples of a 64-K-by-4-bit RAM is NEC Corp., which hopes to make the part available this fall. Volume deliveries of its by-1-bit part are to begin in early 1984.

Toshiba Corp., which will start to ship a 256-K-by-1-bit RAM in the autumn, will make available samples of a by-4-bit chip in 1984. Toshiba is also working on a byte-wide part. Hitachi Ltd., now qualifying samples of page- and nibble-mode 256-K-by-1-bit parts, is readying a 64-K-by-4-bit RAM for the fourth quarter of 1984. In addition, Hitachi is working on a 32-K-by-8-bit pseudostatic RAM that could bow as early as next year. The volume leaders are Fujitsu Ltd., which claims to be now producing more than 100,000 by-1-bit devices monthly, and Oki Semiconductor, which says it will turn out 50,000 per month at its Santa Clara, Calif., facility, beginning in October.

Elsewhere in the U. S., Texas Instruments Inc.—which last year was first to sell by-4-bit 64-K chips [*Electronics,* June 30, 1982, p. 49]—has included the "hooks" in its 256-K-by-1-bit design that will allow it to introduce a 64-K-by-4-bit part quickly next year. Its first by-1-bit chip is due later this year.

Motorola Inc. had hoped to start supplying samples of its 256-K-by-1-bit chip at the start of 1983 but has delayed things, as it tries to improve its design, till the first quarter of 1984. A 64-K-by-4-bit chip will be introduced 9 to 12 months later. Western Electric Co. began this summer to offer samples of a by-1-bit chip. Inmos Corp. will begin selling samples of a by-1-bit chip by early next year, and Micron Technology Inc. will do so by the end of the first quarter of 1984. **–J. R. L.**

Disk controller looks at more than speed

All too often, speed enhancements at one end of a computer system create bottlenecks at another, dulling the luster of expected gains. In fact, this quandary faces all system integrators who wish to benefit fully from the latest high-performance hard-disk drives for microprocessor-based gear.

The solution? "Working smarter, not merely faster," says Michael E. Cope, president of Interphase Corp., in Dallas. This month the company takes the wraps off its Multibus controller board for Storage Module Drives, a board that relies on firmware to optimize drive performance, initially for Bell Laboratories' Unix operating system.

Most disk-drive controllers are made to serve as broad a market as possible. Tailoring with firmware adds the "smarter" factor that Cope thinks is needed.

SMD drives are enticing system designers because their data rates reach 20 megahertz and their storage capacities exceed 800 megabytes. Cope says that the key to better performance—faster disk access, for example—is to study operating systems and discover the best way to manage the drives. Faster accesses would help microprocessor-based systems compete more equally with minicomputers in high-performance multiuser markets now served by production automation systems and work stations for computer-aided design, engineering, and graphics.

Scrutiny. For months, Interphase studied test-program benchmarks and interviewed key designers involved with operating systems—Unix and its crowd of look-alikes, in particular. The resulting firmware for the company's new SMD 2190 drive controller—optimized for the Unix operating system—will in many cases keep the new board several steps ahead of the host in multiple, consecutive-sector, or block, accesses from the disk.

Interphase achieved much of this

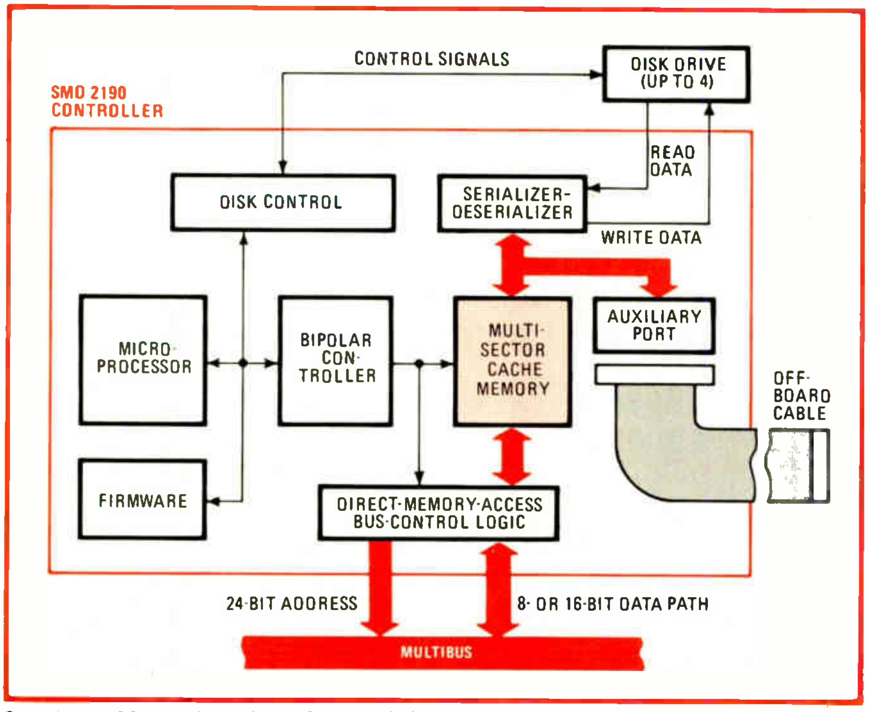
with what Cope describes as "forward-looking" cache-memory algorithms—different from typical memory cache schemes, which store and retain the most frequently used data for quick access. On the SMD controller, data from the disk is prefetched, with algorithms that are fixed in firmware and predict what data will be used next. Depending on how many sectors are taken from the disk at any one time, tests show the caching algorithms are two to five times faster than similar controllers, which use brute force to push their way through a 1 : 1 sector interleave.

Coping. SMD controllers must somehow cope with the fact that operating systems often access long streams of disk data a little at a time—usually four to eight sectors, but sometimes only one. When running compiles, for example, typical Unix installations break consecutive sector accesses into multiple independent operating-system transactions almost 80% of the time. While the access is being broken into separate transactions, the disk continues to spin, so milliseconds are lost as the SMD unit repositions its head and looks for the next consecutive sector.

To overcome this problem, the 2190 cache scheme pulls off about a half track of consecutive sectors and loads it into the on-board high-speed static random-access memory—all in the time taken up by the initial disk access. When the system is ready for the next group of sectors, the controller immediately pulls the data from RAM. In effect, latency time is zero, says Cope, and the board still does the 1 : 1 sector interleaving.

So long as the strings are shorter than 16 sectors the cache scheme is faster retrieving a full track of data in small successive strings. For the Unix system, this works out to 46 milliseconds, compared with 72 ms for eight sectors; 60 ms, compared with 137 ms for four sectors; 75 ms, compared with 265 ms for two; and just 114 ms compared with 521 ms for single-sector strings.

Interphase believes the optimal Unix cache is 16-K bytes. The SMD 2190 controller with 4-K bytes of cache sells for $2,250 each in units of one—$1,550 in lots of 100s. For $200 more, the full 16-K bytes is included. –**J. Robert Lineback**



Smarter and faster. Interphase Corp. optimizes the performance of its controller for Storage Module Drives by tailoring it to the operating system with firmware and relying on forward-looking cache-memory algorithms to predict what data is likely to be used next.

Computers

Hybrid computer automates patching

Even in this increasingly digital world, hybrid computers—strange beasts comprising both analog and digital processors—are favored by engineers who simulate dynamically changing, high-speed conditions. Though hybrids are considered a dying breed by proponents of massively parallel digital processing, the company with the lion's share of world hybrid sales has introduced a new, more automated version it hopes will revitalize its sagging market.

Electronic Associates Inc., of West Long Branch, N. J.—whose machines simulate things like wind-tunnel effects on aircraft and reentry envelopes for returning spacecraft—has been turning out hybrid and analog computers for more than 30 years. Hybrids make up some 40% of its $53.4 million in sales, and it garners 70% of the world total, says Edward Puth, vice president for finance.

Downward. However, orders are dropping even as the economy picks up, prompting the company to develop its new, easier-to-use machine. Called Simstar, it departs from earlier hybrids by eliminating the traditional patch cords that set up analog processing. It is slated to be demonstrated this fall.

The analog part of a typical hybrid computer comprises hardware macroinstructions that perform, in parallel, individual mathematical functions like integration, summing, and multiplying. Information need not be digitized, so a change in input is reflected in real time.

While the analog processing flashes along, a digital processor handles slower computations. Together, the two process information much more quickly than most digital computers. With one parallel analog processing module—more may be added—EA says that Simstar can take on 60 to 80 differential equations and perform 200 million normalized op-

News Brief

Bell uncorks fastest n-MOS chips

Bell Laboratories scored doubly this month in the submicrometer race. Last week it turned out a 1-gigabit-per-second n-channel MOS preamplifier with 1-μm features; earlier, it completed functional testing of a 1.5-μm n-MOS 16-by-16 multiplier chip and recorded a blazing 20-nanosecond multiply time. Both speeds are the fastest reported, says Martin Lepselter, director of the advanced LSI development lab in Murray Hill, N. J.

The 8,000-transistor multiplier, first described in February, far surpasses the Phase 1 design goals of the Pentagon's Very High-Speed Integrated Circuits program—its functional throughput rate is 3.6×10^{12} gate-hertz per square centimeter, versus VHSIC 's 0.5×10^{12} gate-Hz/cm^2 design goal. In pilot production—with a 1-μm version being debugged—the multiplier will be part of a 25,000-transistor digital flash signal-processing chip. Lepselter makes no bones about pinning his hopes on n-MOS for speed as well as producibility. "Gallium arsenide is just not a serious contender," he says.

erations per second—up from 15 million NOPS in the earlier, patch-cord model, the Hyshare 2000. This speed is equivalent, claims EA, to that of a Cray II supercomputer. Including a 32-bit digital processor and a Motorola 68000 as an interface controller, Simstar sells for about $250,000. It works with a Gould/SEL 32/8780 32-bit superminicomputer as host.

Poor patch. Traditionally, the analog portion is interconnected with patch cords in a pattern for each application. But the cords—wires with pins that plug into the macros—are unwieldy and unreliable. Pins bend, making for poor contact, points out an EA customer, Don Waller, head of simulation at Grumman Aerospace Corp., Bethpage, N. Y.

Simstar banishes the patch panel, connecting 203 hardware macros via a three-stage complementary-MOS switching matrix borrowed from telephone switching. Moreover, the machine is programmable in Fortran, obviating special training, and a standard continuous system simulation language is built into its software.

Even better, says Simstar program manager Ronald Embley, the machine is 10 times more accurate than its predecessor, resolving an output to five digits instead of four. He attributes this partly to compound operational amplifiers that attain high bandwidth and gain, with low input offset; an autobalancing system where some 600 digital-to-analog converters correct the op amps' drift; and autoranging computing components—digitally controlled attenuators and multipliers that improve their own accuracy at lower gain, extending the range of input and output variables by an order of magnitude.

EA's virtually solitary market position may discomfit it a bit, however. One erstwhile competitor, Denelcor Inc., of Aurora, Colo., recently forsook hybrids in favor of its $1.35 million digital multiprocessor, HEP I. "At some point simulation will be more effectively done digitally. Our architecture will bring the price-performance into an affordable range," says marketing vice president Philip Carley, "I'd be shocked if the hybrid market is still here in 10 years."

Digital processing could one day supplant analog, concedes Grumman's Waller, who may buy Simstar for its automated patching and modular software. But, "when you need to go to different points in a flight envelope quickly, a hybrid does it cheapest and best. You can't match the speed." —**Marilyn A. Harris**

Executive aid stores programmed worksheets

For the business executive who wants to tap the computer's power without learning how to program, Convergent Technologies Inc., of Santa Clara, Calif., has developed WorkSlate [*Electronics*, May 5, p.42], another unusual-looking computer that relies on flat-panel displays. This 8 ½-by-11-inch portable stores programmed worksheets, called Taskware, that let users handle such things as financial statements, sales reports, and job costing business tasks.

It is a battery-powered, complementary-MOS, microprocessor-based machine with a 16-line-by-46-character liquid-crystal display. Other goodies include a built-in 300-baud auto-answer–auto-dial modem, a built-in speaker phone, and a dual-track microcassette recorder both for voice and data.

WorkSlate is the first retail product from the four-year-old supplier to original-equipment makers of minicomputers and personal computers. Selling for $895, it is set to be introduced on the cover of the American Express Christmas catalog, and it will be shipped in volume starting in the first quarter of 1984. —**Stephen W. Fields**

Federal regulations

FCC sets new rules for computing devices

New rules from the Federal Communications Commission for testing computers, video games, and other devices, set to go into effect Sept. 1, could make things tougher for manufacturers to gain approval for their hardware. The rules add more detail to test procedures for devices falling under the commission's class A and B computer-equipment categories. In

SCIENCE/SCOPE

A Very High Speed Integrated Circuit chip built for the U.S. military uses technology that makes it inherently hardened against radiation. The chip, produced after less than two years of development, draws on complementary metal oxide semiconductor/silicon on sapphire technology. It has circuit dimensions of 1.25 micrometers, or about 50 millionths of an inch. The VHSIC program is being conducted by the Department of Defense to develop chips that will give electronic systems a tenfold increase in signal processing capability. The high-speed, compact VHSIC chips will be more reliable and will require less power than integrated circuits now in use. Hughes Aircraft Company is the only contractor in the tri-service program pursuing CMOS/SOS technology.

Studies have begun to see how an advanced airborne surveillance radar might serve military forces late in this century. The radar would have a large phased-array antenna capable of generating many pencil-shaped beams and would complement the Airborne Warning and Control System (AWACS), which performs command and control duties as well as surveillance. One use of the new radar might be to listen in directions other than that of its transmitter beam. If it were to detect another active radar transmitter, the radar could turn its transmitter off (thus foiling an enemy's antiradiation missile) and do its surveillance by using the other radar's transmitted pulse. These concepts are being investigated by Hughes under several study contracts for the U.S. Air Force's Rome Air Development Center.

A new era in sonar for U.S. Navy antisubmarine ships has begun with the first installation of the SQS-53B aboard the USS Moosbrugger. This surface-ship sonar is far more powerful and capable than existing systems. It detects, tracks, and classifies many targets simultaneously. The SQS-53B's sonar bulb creates sound waves and detects their echoes off targets. The system also is used to listen for unusual sounds. Hughes is building systems for more than 40 ships.

Of the improvements in productivity of electronics offered by computers, some of the most dramatic can be found on the manufacturing floor. Computer-controlled automation yields important savings through increased efficiency, flexibility, and accuracy. Computers can repeat virtually all processes -- machining, chemical processing, circuit board fabrication and assembly, quality inspection, and functional testing -- with infallible precision well beyond the abilities of a human. In the production of digital electronics modules at Hughes, productivity sometimes has been increased by a factor of 10 or more. Hughes is spending $240 million over five years on computer-aided manufacturing.

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particular, they eliminate unrealistic cable configurations that could lead to skewed test results.

Class A refers to commercial and industrial systems and class B to home systems, including personal computers, video games, and anything that connects to a television set. The specifications, listed in part 15 of the FCC rules, state that no equipment may radiate radio-frequency energy of a given magnitude over specific frequency ranges. Class A equipment is tested by an FCC-registered lab and the results submitted to the FCC. Class B tests, on the other hand, are done by the FCC.

Help. Usually, class B equipment is tested at a private lab first before going to the FCC to ensure it will pass. If something fails at the FCC, modifying and retesting it would severely delay its market introduction.

The problem, says consultant Glen Dash of Dash, Straus & Goodhue, Boxborough, Mass. (see p. 131), is that "about 75% of the companies do not test their equipment the way the FCC does. What the FCC is doing is trying to get people to test the way they do."

The new rules spell out in more detail the configuration of the equipment—the power cords, cables, and peripheral devices—during testing. Test limits remain unchanged.

In the past, FCC technicians extended power cords and connecting cables to create the maximum radiation, a situation an FCC spokesperson terms "unrealistic." For their part, the private labs would coil cables to minimize radiation—also unrealistic.

The new rules set forth in a July 26 memo and in a booklet known as MP-4 are somewhere in between. They call for tests in a configuration close to that of actual use. If a computer will be connected to a printer, for example, that should be part of the test, too. No longer can test labs route cables to minimize radiation.

The new rules are not retroactive. But until they get the knack, it may be harder for companies to push hardware through the FCC in time for introduction at, say, the Comdex computer dealers show in Las Vegas in November. **–Stephen W. Fields**

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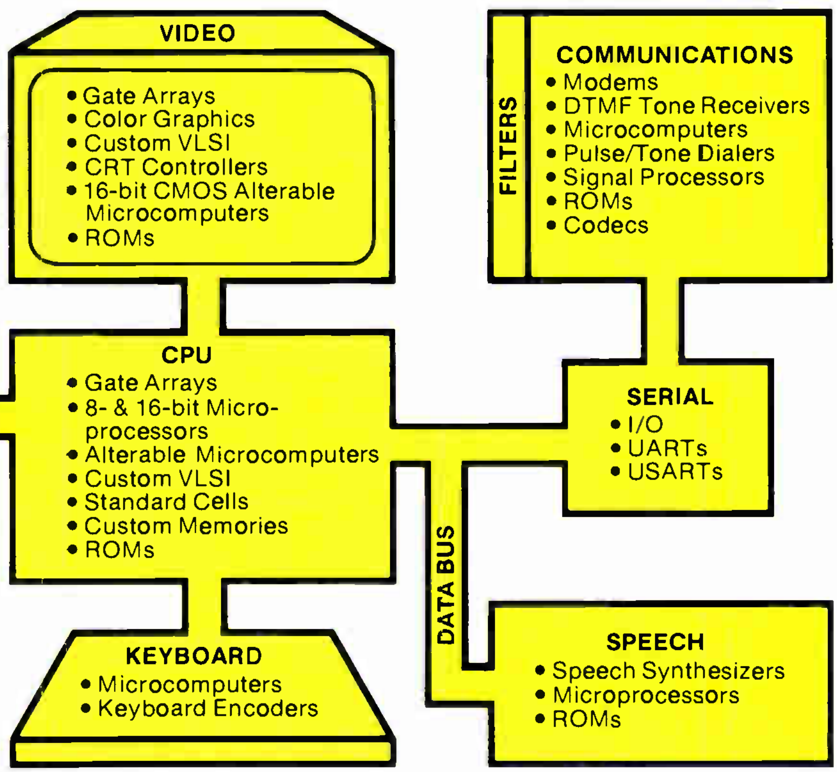

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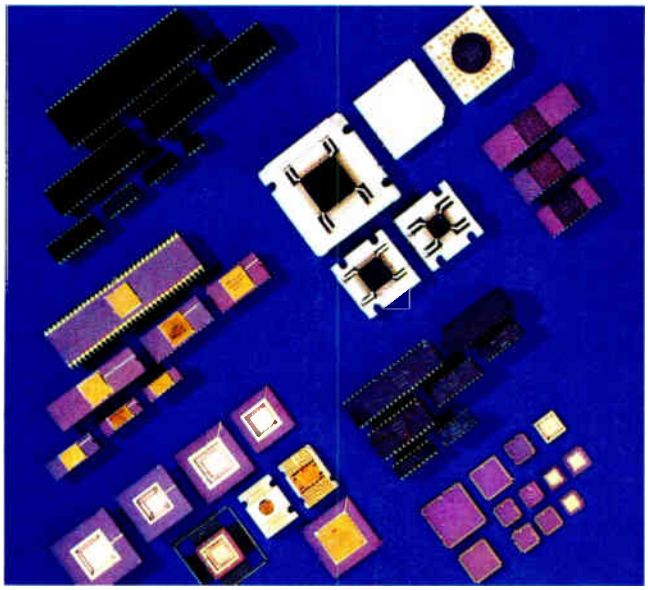

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Washington newsletter

FCC committee to eye direct-broadcast-satellite standards . . .

The Federal Communications Commission has asked its former chairman, Stephen Sharp, to head a new advisory committee that will recommend standards in support of the Regional Administrative Radio Conference's plan for direct-broadcast satelllites in the western hemisphere. During RARC's five-week conference in Geneva this summer, **the U. S. was assigned eight orbital slots for future satellites** that will operate in the K band with a 12.2-to-12.7-GHz downlink and 17.3-to-17.8-GHz uplink. Each position will accommodate up to 32 channels, and 36 of the U. S.'s 256 have already been allocated by the FCC to eight DBS operators.

. . . and consider new British coding format

High on the advisory committee's agenda is consideration of a new signal-coding format proposed for European direct-broadcast-satellite services by Great Britain's Independent Broadcasting Authority. The proposal is for a multiplexed analog-component format requiring neither subcarriers nor overlapping of the spectrum. **Its principal advantage is that it achieves close to 1,000 scan lines per frame within a 4-to-6-MHz video bandwidth,** in contrast with the 525 lines and 6 MHz that U. S. satellite transmissions now produce, reports J. E. Whitworth, a committee member representing Satellite Television Corp., Communications Satellite Corp.'s Washington, D. C., DBS subsidiary. Besides the British proposal, the committee will examine some 100 equipment parameters with which purveyors of satellite services will have to comply.

Defense fuels growth of R&D

Private and public investment for research and development in all industries will reach $97 billion next year, 12% above the 1983 level (or 7% when adjusted for inflation). The increase derives mainly from President Reagan's drive for a rapid defense buildup, says a study from the National Science Foundation. Of that amount, the electronics industries can expect a 14% to 15% share, with about two thirds coming from private resources and the rest from Government. Although an estimated 2.7% of the nation's gross national product will be allocated to R&D, **the share drops to 1.9% when defense spending is excluded,** notes the NSF report. That places U. S. civilian expenditures well below the 2.6% and 2.3% projected for West Germany and Japan, respectively.

Second firm mounts Intelsat challenge

Helping to heat the summer debate on the direction of Washington's international telecommunications policy, the newly formed International Satellite Inc. has become the second company to ask the Federal Communications Commisssion for permission to operate a satellite communications system for private users in the U. S. and Europe. The Wilmington, Del., firm, 43% owned by TRT Communications Inc., wants to orbit two 32-transponder Ku-band satellites for distribution of video and audio programming and high-speed data services. Its future will depend on how the forerunner, Orion Satellite Corp. [*Electronics,* March 24, p. 63], fares when the State Department and the National Technical Information Agency **decide between Washington's commitment to Intelsat—the International Telecommunications Satellite Organization—and increasing industry competition.** The notion that private transatlantic carriers will threaten Intelsat's economic well-being "is a popular misconception put forth for the unsuspecting," says Melvin Barmat, a stockholder in the new company. In a move it apparently is making for international goodwill, International Satellite has proposed to make one transponder's worth of capacity available to the United Nations free of charge.

Joint Stars radar draws four teams

Four contractor teams are set to vie for a contract worth more than $110 million to develop Joint Stars, an airborne surveillance and target-attack radar system for the U. S. Army and Air Force. The duos that will respond to the request for proposals, to be issued within the next two weeks, are: Westinghouse Defense & Electronics Center with Lockheed Missile & Space; Grumman Aerospace with United Technologies; Hughes Aircraft with E-Systems; and General Electric with Boeing Aerospace. **The two services' surveillance and attack systems must have many components in common but also must be able to meet the Air Force's more stringent requirement for weapon guidance.** For its part, the Army, which wants to deploy Joint Stars early, needs quick delivery of off-the-shelf hardware, such as parts already developed for the F-16 and B-1B aircraft radars.

Software companies selling like hotcakes

Companies that seek to grow through acquisitions are snatching up microcomputer software houses at a blistering rate, says the Association of Data Processing Service Organizations' new study on mergers and acquisitions in the $26-billion-a-year computer-services industry. The first half of the year saw some 60 transactions, worth about $409 million and nearly equal to the $436 million recorded for all of 1982, Adapso reports. **Most of the companies that have been bought produce microcomputer software, but such ventures are started up more rapidly than they are acquired,** notes Adapso's president, Jerome L. Dreyer. Because of the burgeoning demand for microcomputer software, the total number of computer-service companies will grow from 6,000 today to around 9,000 by 1990 and generate annual sales in the area of $90 billion, he predicts.

Reagan to give medals to high-tech achievers

President Reagan will award the first annual National Medals of Technology next spring to innovators who have, in the words of the White House announcement, "advanced U. S. competitiveness in world markets, created new jobs, and made technological improvements to industries and people everywhere." The medals will go to individuals or a company directly responsible for translating technology into commercial products or processes. However, Ken Hagerty, vice president of government operations at the American Electronics Association, was of two minds about the award: "The event could evolve into an incentive for goal-oriented corporate research and development teams *à la* the Nobel Prize," but **"in no way should this be seen as a substitute for more substantive Federal programs** to improve U. S. standing in world technology markets." Hagerty says the industry's top concerns are, rather, removal of the sunset provision on R&D tax credits and easing of the restrictions on high-technology exports.

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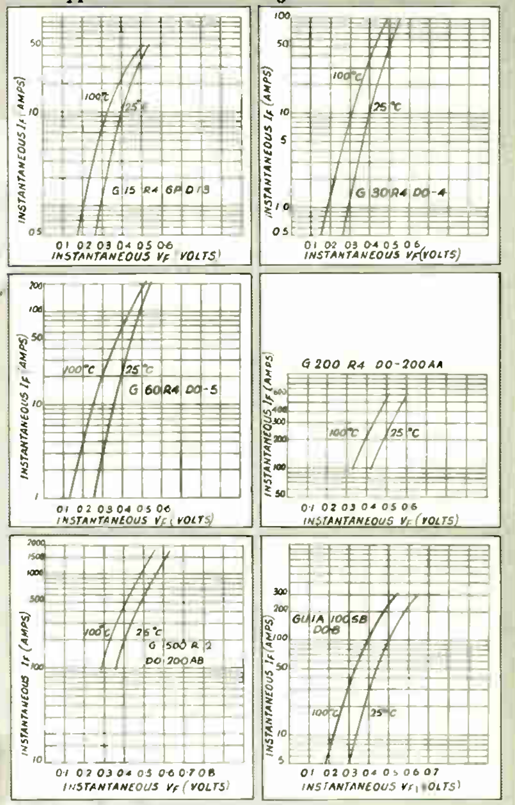

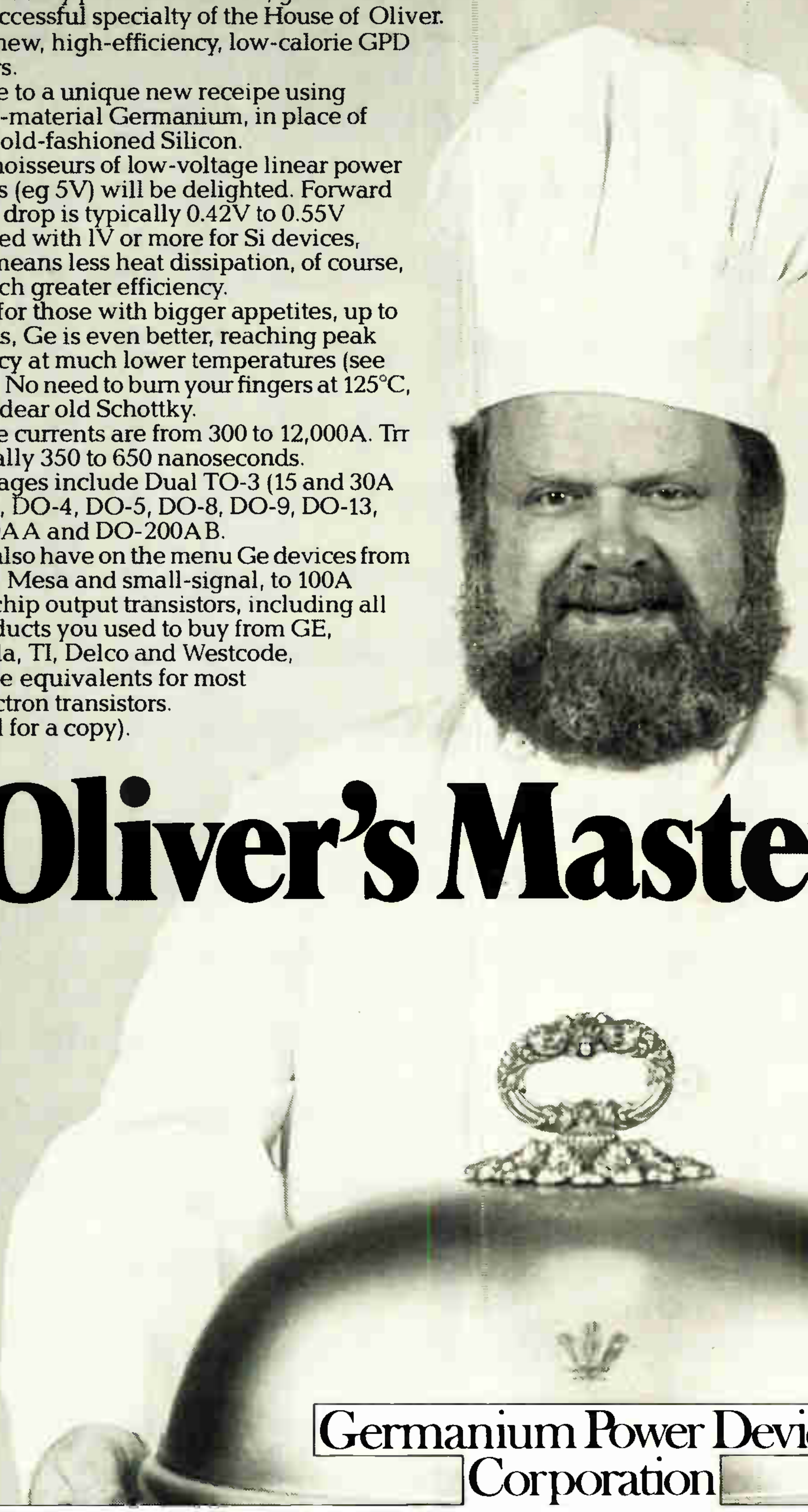

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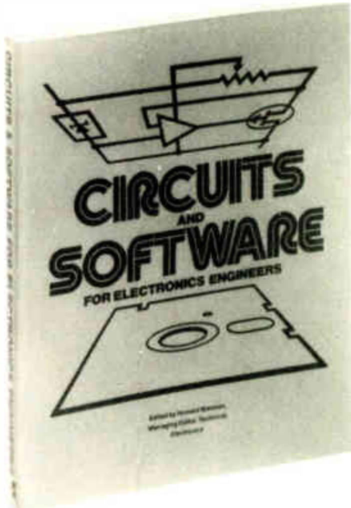

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International newsletter

Sony to show off digital TV sets

Giving a hint of its future product plans, Sony Corp. will show two prototype digital TV sets at the Berlin International Audio and Visual Fair, starting Sept. 2. One prototype gets a high-resolution display, with improved color and luminance fidelity, by digitally processing the NTSC signal broadcast in Japan and the U. S. The other, operating on PAL European standards, eliminates flicker with a one-field digital memory that facilitates doubling the field rate to 100 Hz. The high-resolution TV gives the present signal much better fidelity than an analog TV can. **A dynamic comb filter provides chroma- and luminance-signal separation superior to that of filters now in use.** Interpolation circuits provide noninterlaced scanning that improves resolution by doubling the number of scanning lines in each field. Sony expects to apply digital processing to one TV model in about a year but refuses to divulge set size, features, or price.

Silicon compiler halves PLA size

Watch for computer-aided-design specialist Silver-Lisco, located in Heverlee, Belgium, and Palo Alto, Calif., to market a silicon compiler that can translate a programmable-logic-array description directly into a layout pattern. The new compiler for n-MOS and complementary-MOS PLAs, developed at the Electrical Engineering department of the Catholic University of Leuven, Hevorlee, is important because any combinatorial logic system can be represented as a PLA (basically, a regular matrix of AND-OR product terms). So a silicon compiler that can translate such arrays into mask patterns directly from a logic table is an extremely powerful design tool. The Belgian group described the compiler last week at the VLSI '83 Conference, in Trondheim, Norway. **It comprises a set of programs that minimizes logic arrays, automatically generates test patterns for scan-path designs, and lays out the part.** This last program can map a PLA for different silicon process technologies by specifying process variables. The compiler produces a highly compact array. For example, the logic minimization routine running on a VAX 11/780 can typically reduce product terms by a factor of 5 : 1. Array folding, a technique that condenses sparse matrixes, further reduces chip area to between 30% and 60% of its original size. Silver-Lisco has marketing rights to all software developed at Leuven.

Two telecom producers seek to change their luck through collaboration

The French Socialist Government is about to take a risky gamble that collaboration between the Compagnie Générale des Constructions Téléphoniques and Thomson-CSF on developing and producing certain telecommunications product lines will succeed where neither company has done so on its own. CGCT is a former IT&T subsidiary suffering from severe financial and labor-relations difficulties. Thomson, the giant French conglomerate, piled up a significant portion of its massive 1982 loss—$280 million—in just those areas covered by the agreement [*Electronics,* May 5, p. 76]. In addition to the expected licensing of CGCT to produce Thomson's MT family of digital switches [*Electronics,* May 19, p. 108], **the two nationalized Parisian companies will jointly develop lines of telephone handsets and terminals,** presumably for use in public and private telecommunications networks. According to sources in the Ministry of Industry, the accord will be put into action "very quickly," although an exact date has not yet been announced.

International newsletter

$60 3-d TV kit heads for U. S.

A West German entrepreneur wants to bring to the U. S. three-dimensional color TV using the Abdy (for anaglyphic by delay) process [*Electronics,* Jan. 13, p. 75]. Hasso Hofmann, head of a Hamburg-based firm called Abdy Hasso Hofmann, is negotiating with one West Coast company and is looking for other U. S. firms to build and sell circuit kits that add the third dimension to the screen image—no change in broadcast and reception techniques is necessary. Installed by a repairman, **the kit consists essentially of a printed-circuit board with about 50 components** and includes special colored glasses that give viewers the sensation of depth. It will go on sale in West Germany next month for about $60, the same price Hofmann envisions for the U. S.

Credit-card calculator bowing in a big way

Casio Computer Co. has geared up to supply the world with more than 200,000 credit-card–sized calculators each month. As a result of their 85.5-by-54-by-0.8-mm dimensions, which match International Standards Organization specifications for credit cards, they come equipped with a standard magnetic-tape stripe for use in cash dispensers and similar applications. Their smallness and suitability for use as magnetic cards have led many firms, including American Express, to place large orders for the product even before Casio starts selling them in Japan this autumn for about $25 through its regular dealers. **The calculator is automatically assembled by laminating nine separate film layers,** including a film-encapsulated liquid-crystal display, a film-based solar battery for power, a microprocessor on a film carrier, and a multilayer film keyboard. Three of the layers are stainless steel—a front panel with holes at the key positions, a frame, and a back panel. A potting compound applied before the back panel is attached provides packaging for the microprocessor.

Addenda

Britain's Thorn EMI Electronics Ltd. has won a $1.58 million contract from Britain's Ministry of Defence to define a fully operational synthetic-aperture radar system. **The system will allow high-flying aircraft to undertake high-resolution surveillance of remote battlefields,** without exposing the planes to enemy fire. . . . All telecommunications-related divisions of Israel's Ministry of Communications have been transferred to the Bazak Corp., the government-owned telephone company that began operations last week. **The new company will be in charge of Israel's entire telecommunications network,** which will at first include telephones and related engineering services and later be expanded to include other sectors. . . . NV Philips Gloeilampenfabrieken of the Netherlands has established Philips Component (Phils.) Inc. in the Philippines to manufacture semiconductor devices for markets around the world. Capacity will be 60 million units annually, with light-emitting diodes being the first product. . . . SEL Computer Systems, Fort Lauderdale, Fla., a division of Gould Inc., is establishing an $11 million minicomputer manufacturing facility at a Dublin industrial park created and operated by Ireland's Industrial Development Authority. The 28,000-ft^2 operation, **SEL's first offshore assembly and testing facility,** will manufacture Concept/32 minicomputers for export.

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4. *Judging criteria are creativity of theme, uniqueness of application, practicality of implementation and potential for pleasing spectators.*
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BUILDING BETTER COMMUNICATIONS WORLDWIDE

Cell array sports 230-ps gate delay and 2,600 functions

by John Gosch, Frankfurt bureau manager

The increase in performance arises from the use of series-gated current-mode logic with three voltage levels

In the international race to bring to market master-slice cell arrays with ever-increasing speeds and complexity, Siemens AG may be pulling ahead of its U. S. competitors. The Munich firm is ready to introduce two new arrays, the larger sporting a minimum gate delay of 230 picoseconds and 2,600 equivalent gate functions on a 75-square-millimeter chip with 120 logic pins.

Whereas such speed and functionality put the West German firm's new family of bipolar master-slice arrays on a par with the best from Motorola and Fairchild (their MCA2500 and GE2000, respectively), the parts boast superior performance when complex logic circuits are involved, Siemens says. A 4-bit multiplexer, for example, switches in about 0.6 nanosecond, and its power consumption is only 18 milliwatts, roughly 15% less than in U. S. parts.

Next step. The key to this is a circuit technique based on series-gated current-mode logic with three voltage levels, which contrasts with the two-level series-gated emitter-coupled-logic technology other companies use. Siemens pioneered three-level CML for its first generation of cell arrays and has refined it for the new second generation by adapting it to more complex functions.

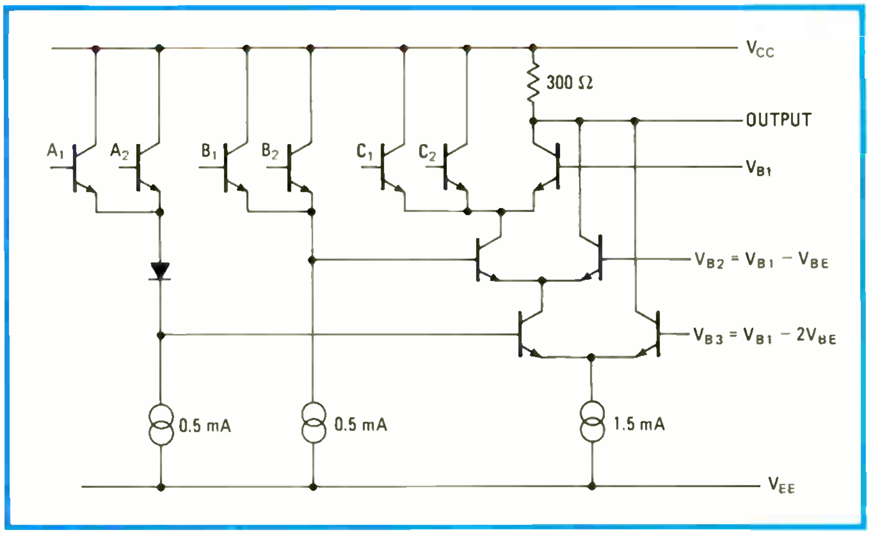
With the technique, it is also easier to implement complex logic functions (or circuits) than it is with the two-level series-gated method, points out Walter Bräckelmann, head of integrated circuits development in the Munich-based Data Systems Group. Complex cells such as 4-bit multiplexers or latches with input multiplexers can be made with only one series-gated structure and only one 1.5-milliampere switching source. The delay through such a structure is less—up to three times less in the case of a complex latch—than the combined delays of primitive NOR gates performing the same logic function.

Speed boost. Also of note is a three-layer metalization system to personalize and interconnect the cells, the third layer reducing chip size and shortening the interconnection lines. The use of polyimide, rather than an organic, isolation provides for a low dielectric constant, which helps to enhance speed.

The prime contributor to high density and performance, however, is the three-voltage-level CML structure (see figure). Reference voltages for each of the three levels are delivered by on-chip bias generators, each supplying two cells and each cell containing four series-gated CML switches. The switching current is 1.5 mA, and the auxiliary current for level switching 0.5 mA. An internal logic swing of 450 millivolts gives high driving capability at low currents.

The voltage difference between each switching level is the voltage drop across one base-emitter diode, so level shifters are very simple. Tight matching of the diodes on one chip enables good symmetry of the input reference at all levels.

The CML technique needs no output emitter followers. The switching current can thus be somewhat higher than in ECL arrays, yet the driving



Triple play. Prime contributor to this cell array's high density and performance is a three-voltage-level CML structure. Reference voltages for each level are delivered by on-chip bias generators, each supplying two cells, each of which contains four series-gated CML switches.

capability is as good as in ECL.

Besides a straightforward reduction of lateral and vertical device dimensions, what sets the new family apart from the first generation are on-chip serial-scan diagnostic logic, complex multicells, and drastically shortened customization turnaround times. With the Siemens Components Group's quick turnaround module—Qtam, for short—to be ready in mid-1984, it will be possible to implement a complex master-slice cell array in only one week.

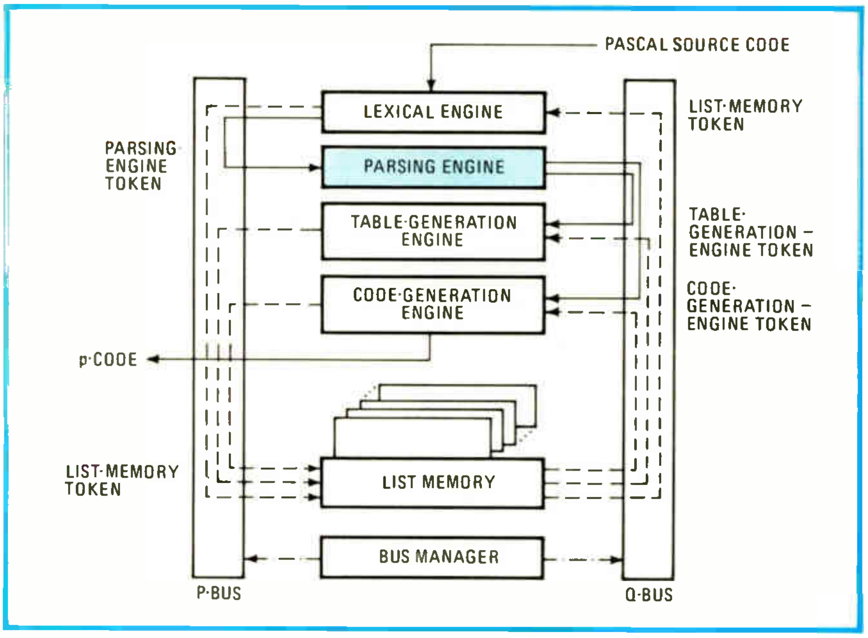
Of the new family's two members, the LSI36K, consuming about 2.5 watts, has 900 equivalent gates on a 25-mm²-chip and 64 pins, 58 of them logic pins. The 2,600-gate LSI20K has 144 pins and dissipates 6.5 W.

The Components Group will start producing a number of different array versions based on both family members during the fourth quarter. The Siemens products are compatible with the industry-standard 10,000-series and 100-series ECL arrays

Common to both members are the cell library, the computer-aided design support, and the Siemens Oxis (oxide isolation) process. The last uses double implantation for the base and emitter, which makes for speed-enhancing shallow junctions. A low-temperature profile and composed mask techniques are additional Oxis characteristics.

Japan

Hardware compiler speaks Pascal



Part and parcel. Compiler chip is constructed with four processing engines and a shared memory unit. First of the four to be designed, the parsing engine uses PLAs.

Intelligent terminals with far more power for engineering and scientific applications than those now available are the goal of a Japanese group developing a multichip very large-scale integrated hardware compiler for Pascal. With the compiler installed, all program-development steps could be performed efficiently and speedily by the terminal, instead of slowly and inefficiently by mainframe software, explains Masaharu Hirayama, research engineer in the Systems Control and Information Sciences department at Mitsubishi Electric Corp.'s Central Research Laboratory, Amagasaki, Hyogo.

Hirayama would add the compiler to a standard terminal that includes a central processing unit with random-access memory, keyboard, cathode-ray tube, and floppy disk. The terminal would be sufficient for source-code input, editing, compilation, test running, and debugging with simple data. Compiled object code would be transmitted to the host—such as Melcom Cosmos series mainframes or the Digital Equipment Corp. VAX 11/780 or system 2060 that Mitsubishi uses in its lab—for high-speed execution.

The host computer will be freed from the burden of symbolic compilation, which it does inefficiently anyway because most mainframes are designed for mathematical computations. Compilation and debugging would be speeded up because the hardware compiler is fast, and there is no need to transfer data through a 9,600-bit-per-second serial-communications line, often a bottleneck. Data-transmission charges will be reduced, too. Because the compiler will generate the intermediate UCSD p-Code developed by the University of California at San Diego as object code, programs could be run on IBM mainframes or other hosts.

Parser. As envisioned at Mitsubishi, the compiler will consist of four single-chip engines working together with a 100-K-byte intelligent list memory and a simple bus manager. The lexical engine will divide the program input into syntactic elements; the parsing engine will check those elements for grammatical correctness and pass them to the table-generation engine, which will create the compiling environment, or the code-generation engine, which will produce p-Code in terms of that compiling environment.

Design of the parsing engine, selected as the first device because it is the simplest, has been completed. Now the group is tackling the other engines and the list memory.

There is a good chance that an associative memory will be available from various sources by the end of the two years Mitsubishi estimates it will take to implement and debug the compiler. Other means of searching for data, such as loops, would make it harder to realize the table and code generators.

Favor Pascal. The Mitsubishi engineers selected the Pascal language because its regular structure allows

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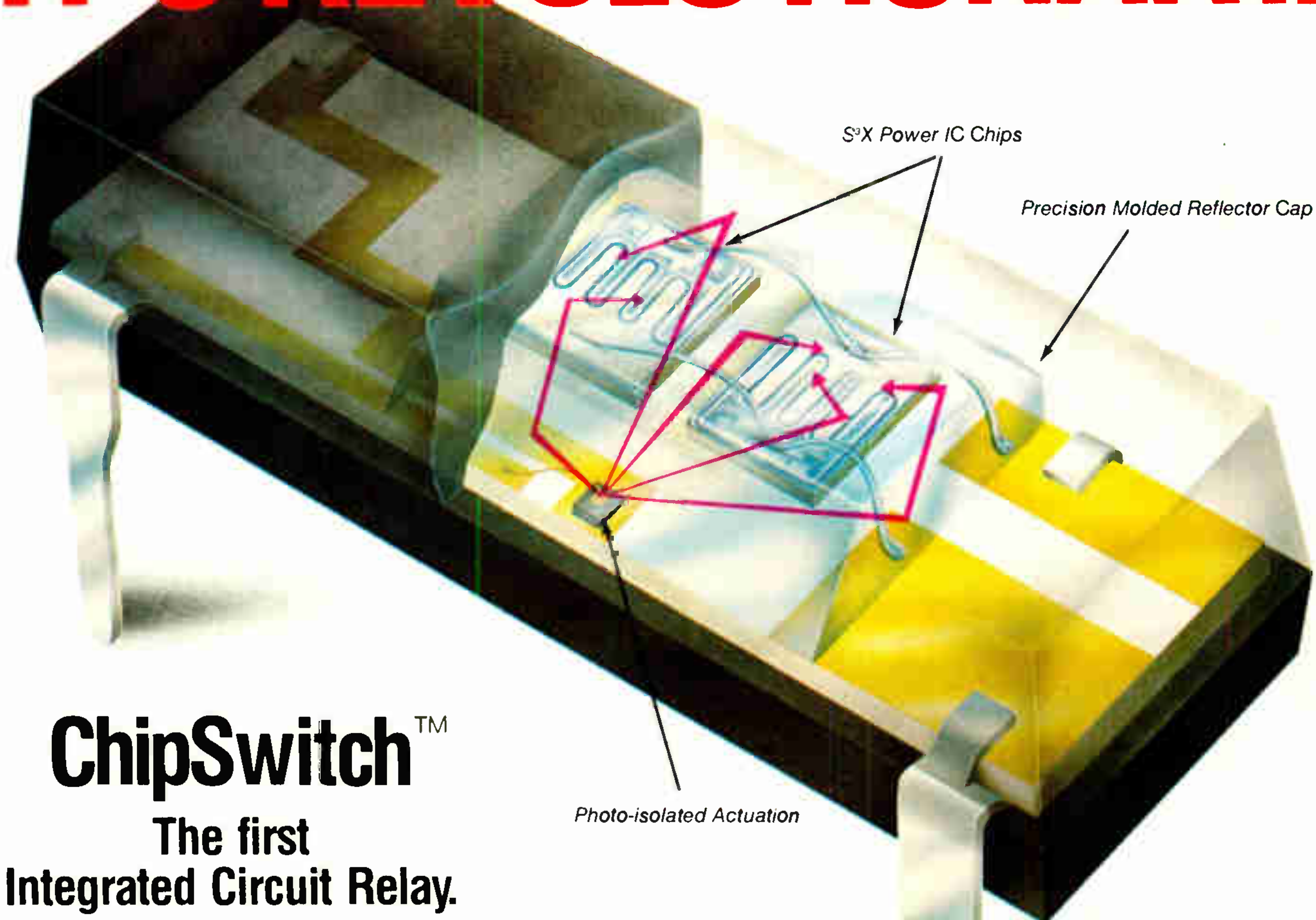

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compilation without backtracking—that is, having to look ahead to process what is on hand at the moment—permitting realization of a compiler with relatively simple hardware. They are confident that the compiler approach will succeed even though computers designed for directly executing high-level languages have not been particularly successful because they are stuck with one language and not amenable to changes.

Algol and its other derivatives, including Modula II and Ada as well as Pascal, are also suitable because they can process without backtracking. Fortran has been ruled out because it has to look ahead.

The straightforward operation of the Pascal parser made it possible to design it as a finite state machine with a single stack. Moreover, the nonnumerical symbolic manipulation nature of the logic facilitates its implementation in programmed logic arrays. This is fortunate because PLAs have a regular structure easy to design with and can be updated without changing their intrinsic layout.

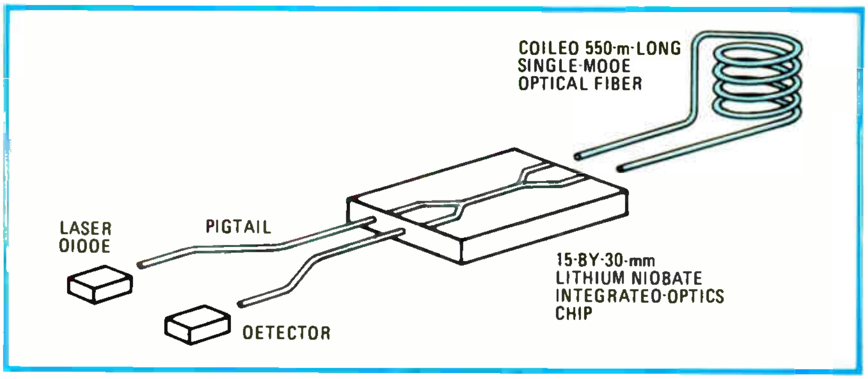
The parser includes five PLAs with six registers; two first-in, first-out memories as input and output buffers; and a state stack. The PLAs on the chip require only a moderate number of I/O lines—typically 8 or 16—but have a much higher number of product terms—as many as 437—than general-purpose devices.

Hirayama is confident the Mitsubishi approach is original, but he admits the implementation is based on the work of several U. S. groups. Software developed by these groups was executed on the same DEC system 2060 and VAX 11/780 computers. –Charles Cohen

France

Optical gyroscope uses single IC

In a development that could well put optical-fiber rotation sensors firmly into the commercial arena, a team of French engineers has successfully tested a brassboard of a gyroscope based on a single integrated optical circuit. This is the first step toward the production of a simple, inexpensive, and reliable gyro to be used not only in traditional aerospace applications, but in higher-volume roles in, say, the automotive field and as the basic component for accurate, wide-range current-measuring devices.



Even split. A simple planar integrated optical chip in the Thomson optical gyroscope splits the beam from the light source and directs the output from the sensing coil into the detector.

Designed at Thomson-CSF's Central Research Laboratories in the Paris suburb of Corbeville, the gyroscope exploits the Sagnac effect—the phase shift of light inside a moving object. Led by Hervé Arditty, the Thomson team has fabricated a single planar device implementing all the gyroscope functions in the form of single-mode strip waveguides. This technique avoids the disadvantages of both discrete optical components, which are difficult to adjust and of questionable stability and reliability, and precision optical-fiber couplers, which are expensive.

The actual operation of a Sagnac gyroscope is based on the perception that the phase of a light beam is affected by rotational motion. In an optical-fiber gyroscope, this phenomenon is exploited with a laser beam divided into two by a 50 : 50 beam splitter and coupled into two ends of a multiturn monomode-fiber coil.

In the absence of rotation, the two emerging beams interfere either destructively or constructively, depending on the way the beam is split. Either way, the output signals the lack of rotation.

During rotation of the equipment on which the gyro is mounted, a fringe or phase shift proportional to the amount of rotation will be detected. The light emerging from the two fiber ends is combined by the beam splitter and received by a photodetector that can transmit a signal to a navigational device.

The beam-splitting function in Thomson's one-axis brassboard is handled by the integrated optical circuit, a branching single-mode dielectric waveguide (see figure). This device divides light entering from the gryoscope's gallium arsenide laser diode equally between the two output branch waveguides.

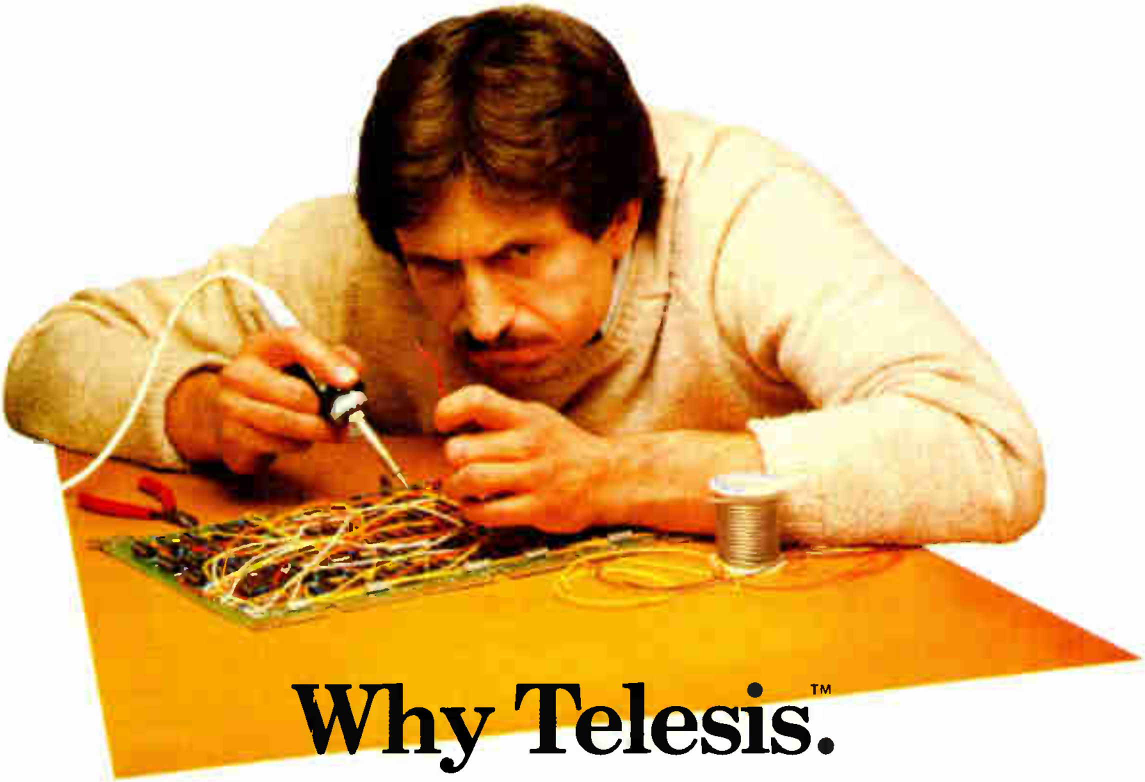
The waveguides are produced by titanium diffusion in a 15-by-30-millimeter lithium niobate substrate and are coupled to a 550-meter fiber coil wound in a toroidal metal container. System output is received by a low-noise silicon photodetector.

Two phase modulators, piezoelectric tubes wrapped with several turns of fiber, are placed at either end of the fiber coil and driven 180° out of phase to produce a modulation of the phase difference perfectly centered about zero. By modulating phase, Thomson maximizes signal response when the gyroscope is at rest. That, in turn, translates into much higher sensitivity to rotation.

Already the prospect of a $100 gyroscope has piqued interest for possible use in car navigation systems. In addition, applications that use the gyro for other than navigational purposes are on the horizon.

Under contract from the French national electric utility, the Thomson-CSF team has connected a monomode optical-fiber probe to the Sag-

Why CAD/CAM



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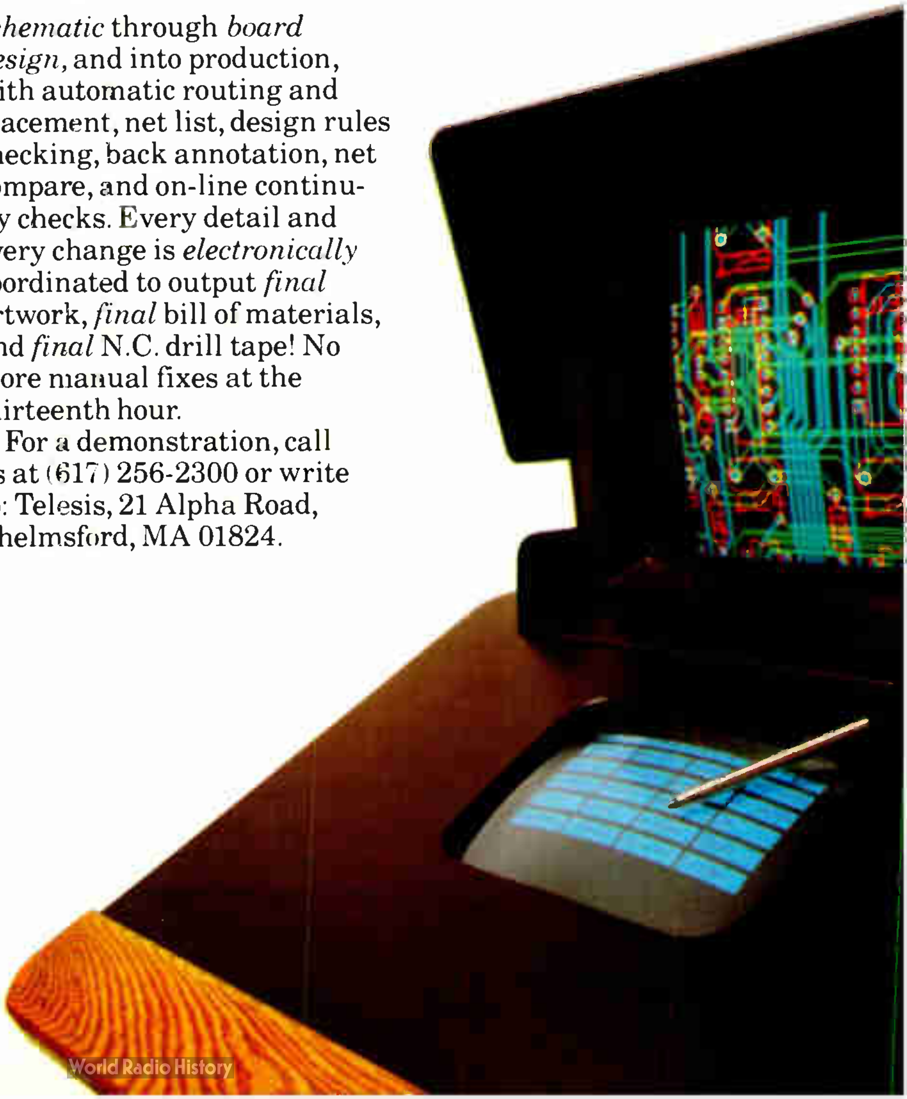

Telesis

CAD/CAM Systems: A Generation Ahead

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nac interferometer, realizing a device capable of measuring currents ranging from several milliamperes to several megamperes.

To do this, the device exploits the Faraday magneto-optic effect, a nonreciprocal phenomenon—like inertial rotation—that circumvents problems like temperature and pressure that are common at the high end of this range. –Robert T. Gallagher

Great Britain

Serial convolver to be fault-tolerant

On-chip fault-tolerant circuitry could be one key to economically feasible yet large and complex integrated circuits. Betting on this, the developer of a high-performance signal-processing IC—Britain's Royal Signals and Radar Research Establishment—is proposing to go that route in order to double the complexity of future generations of its device.

Being developed in collaboration with the General Electric Co. Ltd.'s Hirst Research Centre, the chip is a 16-stage 8-bit serial systolic-array convolver, to be used by the military in signal-matching applications. The 4-micrometer complementary-MOS silicon-on-sapphire IC was described at the VLSI '83 conference held last week in Trondheim, Norway.

It will likely be followed by a more complex 32-stage convolver incorporating fault-tolerant circuitry. Though the chip will be much larger, the Malvern group says yields will be comparable with the 16-stage IC's.

At RSRE, researchers have been developing bit-serial systolic arrays to execute high-performance signal-processing tasks. Like high-density random-access memory, these devices have a highly regular structure and are well suited to similar fault-tolerant circuit techniques.

The systolic array, first proposed by H. T. Kung at Carnegie-Mellon University, Pittsburgh, Pa., comprises a regular lattice of processing elements, each beating time to a common system clock. Enormous computational speed is achieved by streaming data through this array in a highly pipelined manner.

Though Kung worked at the word level, RSRE researchers John V. McCanny and John G. McWhirter and private consultant Ken Wood have patented a way of applying the technique at the bit level. With this approach, an entire signal-processing system can be put on one chip.

In the RSRE systolic array, the typical cell reduces to a gated full adder, a number of latches, and some simple control logic. Several hundred cells can be incorporated on a single chip—the 16-stage convolver, for example, is constructed as a 16-by-20 array of such cells. The systolic array's function is then determined by the pattern of cell interconnections.

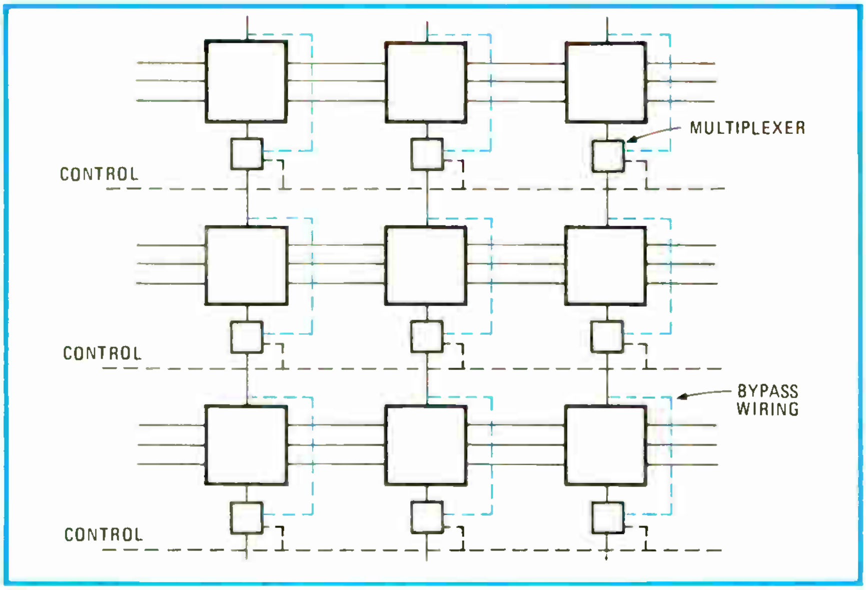
The effect of a few faulty cells in such an array could be overcome by introducing enough redundant cells to replace them. However, each cell is pipelined to its neighbor, so some form of bypass must be provided to preserve the lattice structure.

Bypass is answer. One solution is to provide each cell with a bypass connection to its second nearest neighbor. These connections are made by a common row-control line addressable from an on-chip multiplexer. The transfer gates and the multiplexer can easily be constructed using MOS gates and would add only 20% to the size of each cell.

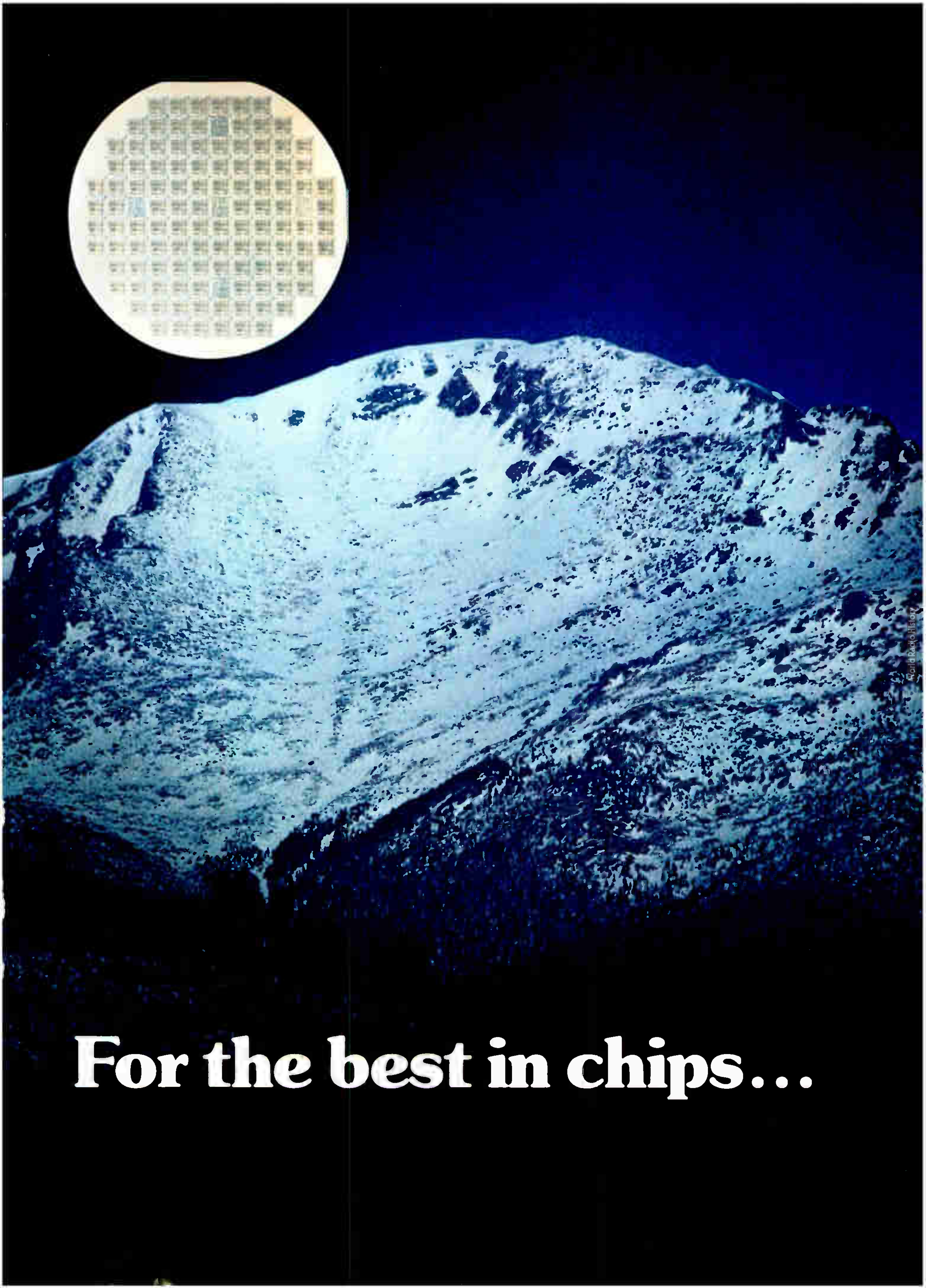
Of course the faulty row or cell must first be identified, but the systolic array's regular structure makes that a relatively easy task. Hirst's 16-stage convolver chip, for example, incorporates scan-path circuitry that can be used to check out the circuit and pinpoint any failed cells.

Though RSRE has not yet tried out its ideas in silicon, theoretical studies based on the 16-stage convolver are encouraging. For redundancy, a further three to five rows would be added to the 16-by-20 array of cells. According to the Poisson distribution, the yield would increase from 10% initially to over 40%, whereas the Bose-Einstein model would give a more modest yield improvement—from 30% initially to 50%.

Aside from RSRE's proposed use of redundancy in these systolic arrays, the Hirst Research Centre has independently made use of the approach to improve the yield of its GRID-64 (for GEC Rectangular II image and data processor) chip, which holds 64 identical processor elements. In the U. S., Gene Amdahl, founder and director of Trilogy Ltd., Cupertino, Calif., is proposing the use of fault-tolerant wafer-scale integration on the company's first computer products. –Kevin Smith



Short cut. In order to preserve the lattice structure of the processing elements in this systolic array, a bypass switch is used to provide redundancy.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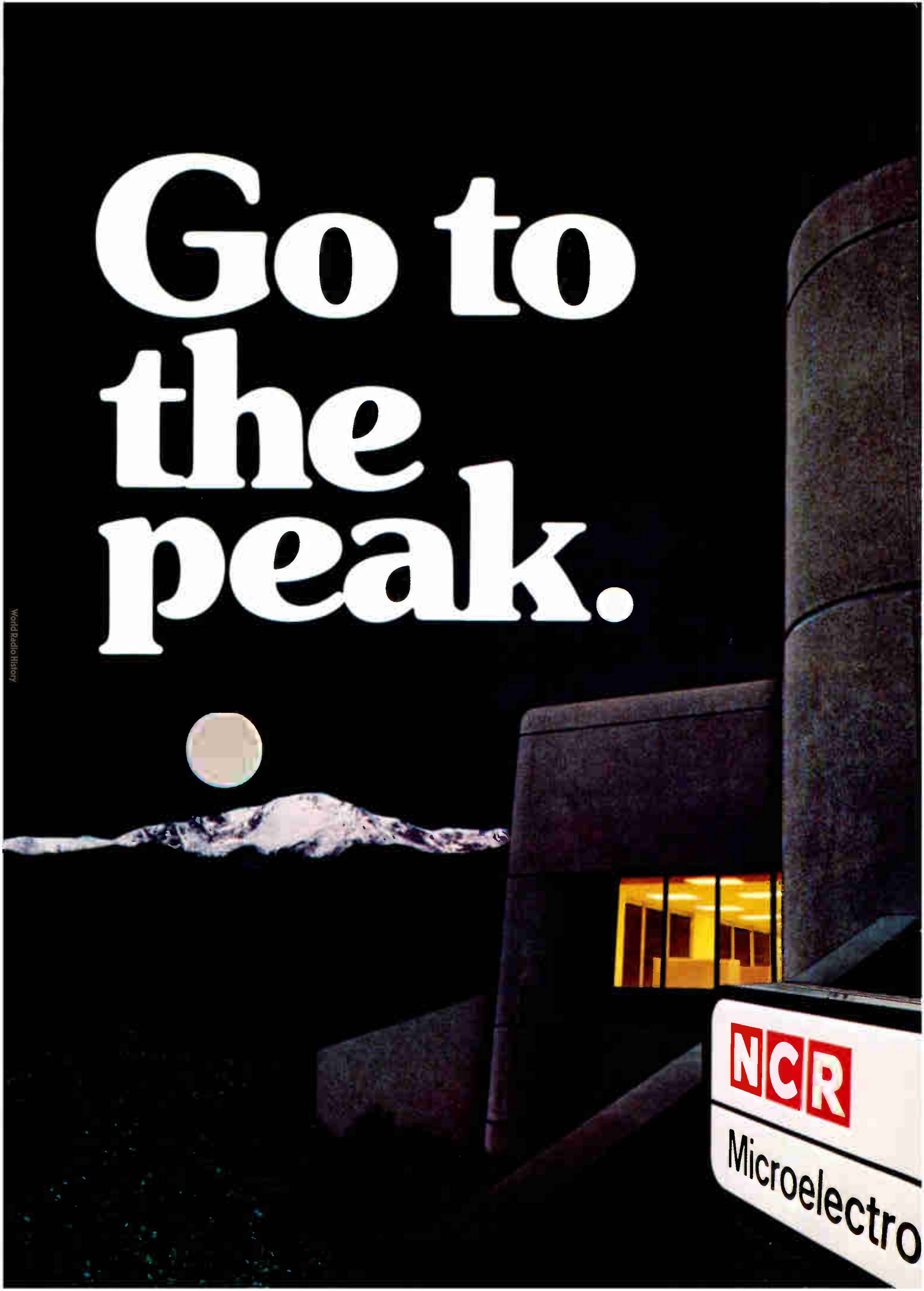
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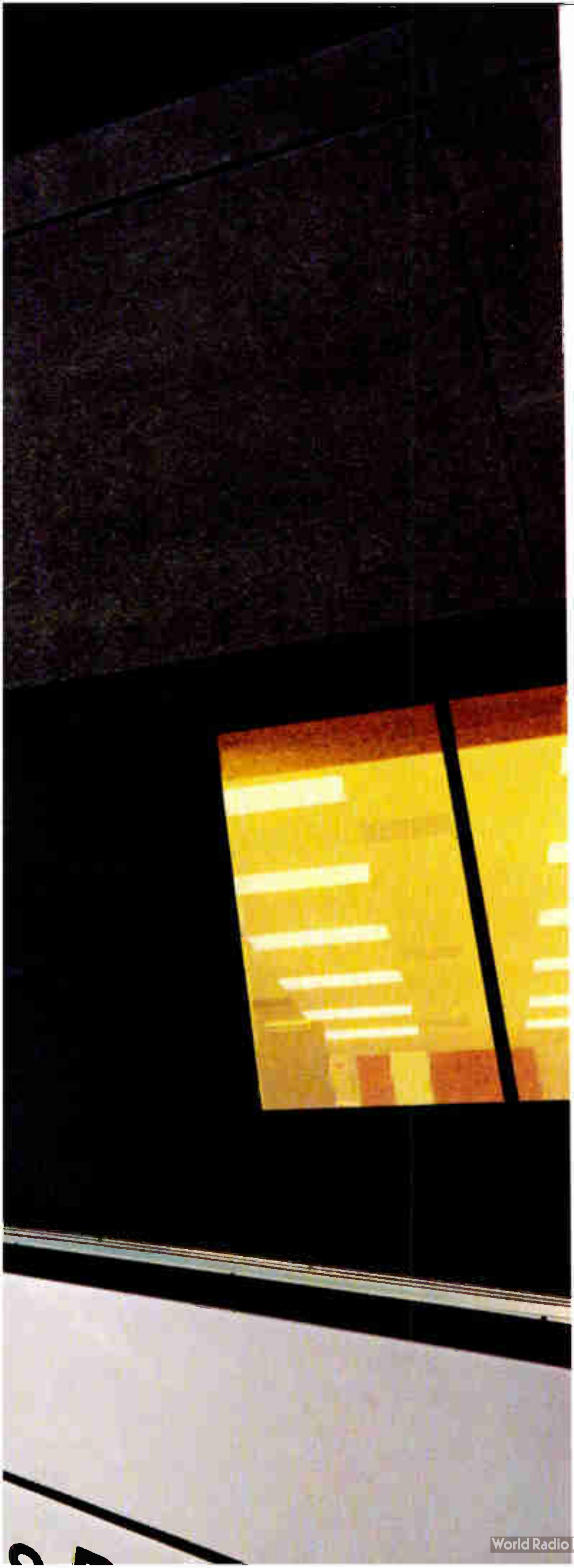

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NCR 2051	512-Bit Word Alterable ROM (32x16)
NCR 2055	512-Bit Word Alterable ROM (64x8)
NCR 2401	4096-Bit Word Alterable ROM (1Kx4)
NCR 3400 (Com)	4096-Bit Word Alterable ROM (1Kx4)
NCR 3400 (HR)	4096-Bit Word Alterable ROM (1Kx4)
NCR 7033	336-Bit Word Alterable ROM (21x16)
NCR 52001	10K-Bit Non Volatile RAM (128x8)
NCR 52002	2K-Bit Non Volatile RAM (256x8)
NCR 52004	4K-Bit Non Volatile RAM (256x4)
NCR 52210	256K-Bit Non Volatile RAM (64x4)
NCR 52211	512K-Bit Non Volatile RAM (128x4)
NCR 52212	1K-Bit Non Volatile RAM (256x4)
NCR 52801	256-Bit Electrically Alterable PROM (16x16)
NCR 52832	32K-Bit Electrically Alterable PROM (4Kx8)

(Com—commercial grade, HR—high reliability)

Read-Only Memory

NUMBER	DESCRIPTION
NCR 2264	64K (4Kx16) NMOS ROM
NCR 2316	16K (2Kx8) NMOS ROM
NCR 2332	32K (4Kx8) NMOS ROM
NCR 2333	32K (4Kx8) NMOS ROM
NCR 2364	64K (8Kx8) NMOS ROM
NCR 2365	64K (8Kx8) NMOS ROM
NCR 23C64	64K (8Kx8) CMOS ROM
NCR 23128	128K (16Kx8) NMOS ROM
NCR 23256	256K (32Kx8) NMOS ROM

Peripherals

NUMBER	DESCRIPTION
NCR 6518	8-Bit Microprocessor Combo
NCR 8415	Universal Product Code Scanner
NCR 7250	CRT Controller
NCR 5385	SCSI Protocol Controller

Processors

NUMBER	DESCRIPTION
NCR 32-000	32-Bit Central Processor Chip (CPC)
NCR 32-101	Address Translator Chip (ATC)
NCR 32-500	System Interface Controller (SIC)
NCR 32-580	System Interface Transmitter (SIT)
NCR 32-590	System Interface Receiver (SIR)
NCR 6500/1	(1MHz) 8-Bit Single Chip Microcomputer
NCR 6500/11	(2MHz) 8-Bit Single Chip Microcomputer
NCR 6500/41	8-Bit Single Chip Intelligent Peripheral Controller
NCR 65C02	8-Bit CMOS Microprocessor

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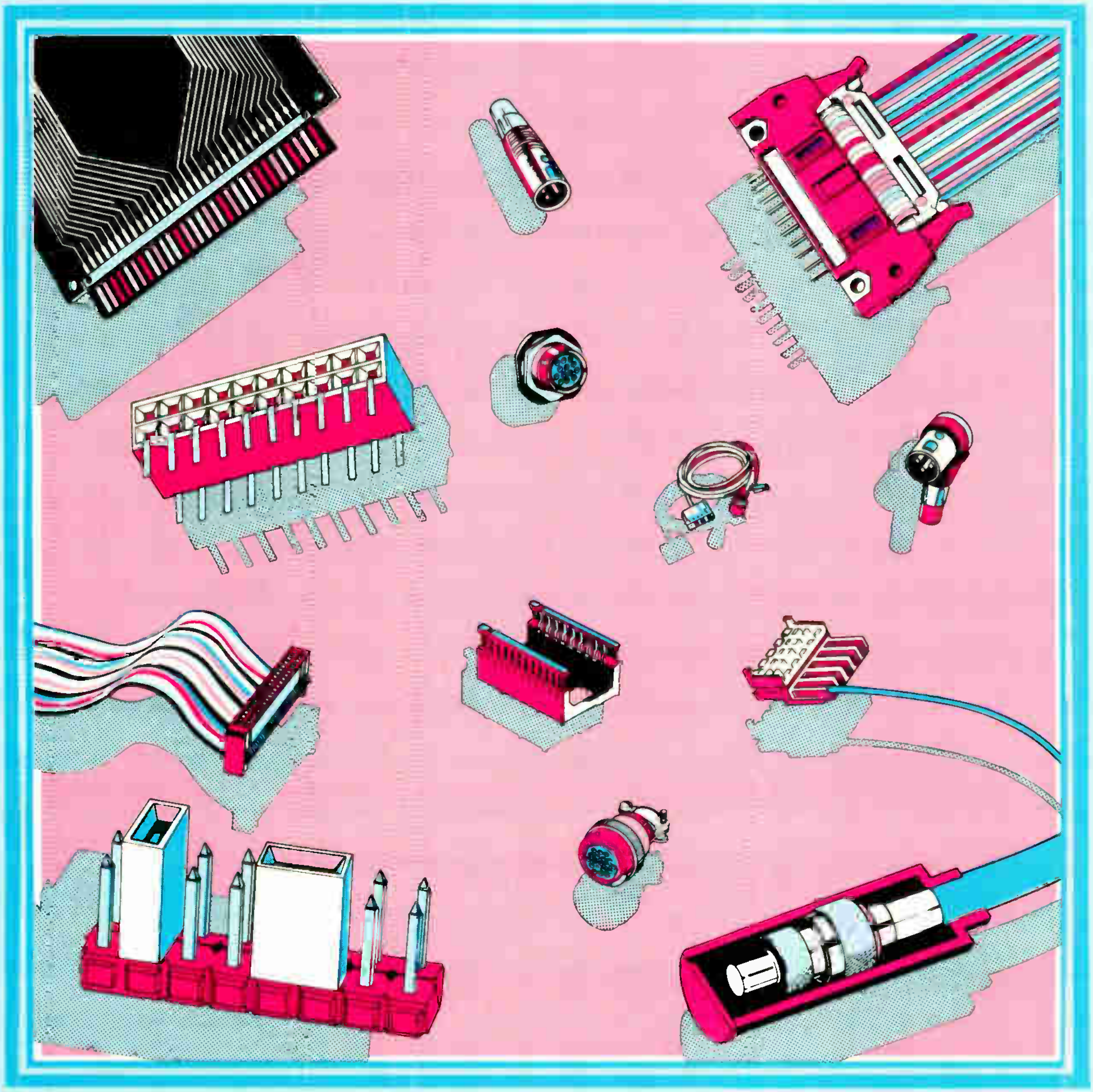


SPECIAL ADVERTISING SECTION   The Basics of Choosing Connectors   A Look at Different Connector Types

ABUNDANCE OF CONNECTORS CAN MEET EVERY NEED; BUT CHOOSING IS DIFFICULT

by Peter N. Budzilovich

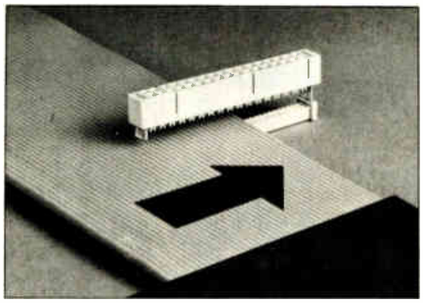
Gone are the days when the variety of connectors in a system would be limited to a two- or three-prong ac plug and a screw terminal strip on the back panel. Even a "simple" desktop computer will have several different types of connectors obvious to the naked eye: two to the monitor (one for data, one for ac input), one to the printer, one to the keyboard, and one to the ac power source (this is a minimum configuration, such as the one on which this article is being written).

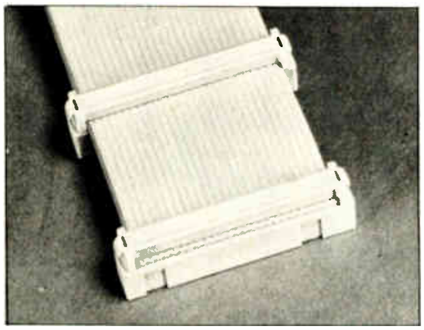
On the inside, a number of connectors may be there: individual pc boards will be plugged into a mother board; in addition to the connections provided on the mother board, there may be jumpers interconnecting two or more boards; integrated circuits and other components may use sockets (which are, after all, also connectors); a number of connectors will be used to provide the input/output links to the outside world by means of a header soldered to the board, a socket attached to flat cable, and an I/O D connector on the panel. All this variety is in what is basically a consumer product—a home or small-business computer. If we were to look at some truly sophisticated electronic equipment, the variety found there would be even greater.

A Knotty Chore

Add to this product variety the numbers of manufacturers supplying (seemingly) the same items, and it may become fairly obvious why cost is one of the major factors in connector selection. The word "cost," incidentally, here denotes the total cost associated with a connector—the item price, labor involved in mounting and terminating, and the costs of service, maintenance, and field replacement. That is to say, a connector costing $1 may, in the end, turn out quite a bit more costly than the one going for $2.

Clearly then, connector selection is no simple chore. Cost considerations alone can be quite perplexing—especially since a purchasing department, faced with the $1-versus-$2 choice for the "same" part, will be hard to sell on the virtues of labor and long-term field savings. On top of this, a variety of purely functional parameters covering electrical and mechanical performance must also be examined and compared.





An IDC Lat-Con connector for 0.050-in.-pitch flat cable from Panduit Corp. permits lateral, rather than axial entry of cable into open-side, preassembled sockets. Covers and sockets are joined on one side only by a metal retention barb. The other side can accept lateral entry of cable for end or daisy-chain applications. The precise recessing of cable ends protects against shorting. [411]

Given the complexity of the subject, this article will limit itself to key considerations involved in the art of connector selection and specification. At the same time, novel approaches to interconnection problem-solving and developing technologies will be highlighted. Overall, the idea is to present a broad overview of the field, without getting bogged down in unnecessary details.

After this introduction to some important selection criteria that apply to all connectors, this article focuses on several key types. Beginning by dealing with three types—insulation-displacement-contact, electromagnetic/radio-frequency interference, and rf/coaxial, the second chapter takes up printed-circuit-board connectors and backplanes and then integrated-circuit sockets.

Simplistically, any device that can physically break an electrical or optical signal path and just as easily restore it should be called a "connector." An ideal connector should have no effect upon the system operation, except when called upon to perform its connect/disconnect function, i.e., it should have zero contact resistance, should have the same electrical characteristics as the wires of the cable it is connecting, and should retain those ideal characteristics indefinitely.

For best results in selecting connectors, a user must conduct a thorough search of what is available, look at manufacturer's specs and descriptions, talk to as many vendor candidates as possible, even visit prospective vendors if a large-volume order is anticipated. Above all, before any of the above steps are made, the user must thoroughly study his or her requirements from every possible angle—environmental, electrical, mechanical, and others. Unless this homework is done, it is pointless to speak about connector selection.

After all this effort, there is still a good chance that something may go wrong. According to Richard L. Bergstrom,

---

Peter N. Budzilovich is a Teaneck, N. J., consultant in corporate and technical communications. He has a background in editing, engineering, and marketing.

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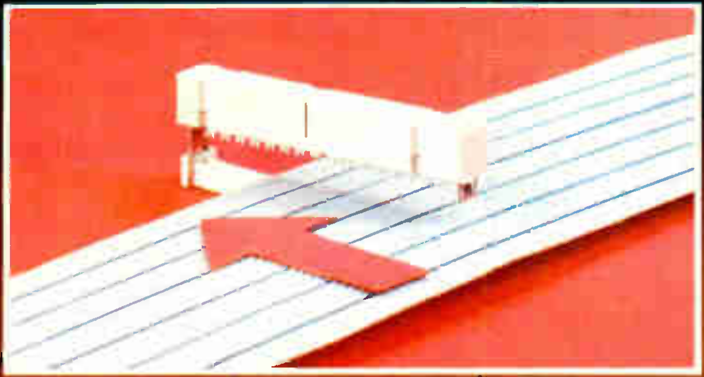

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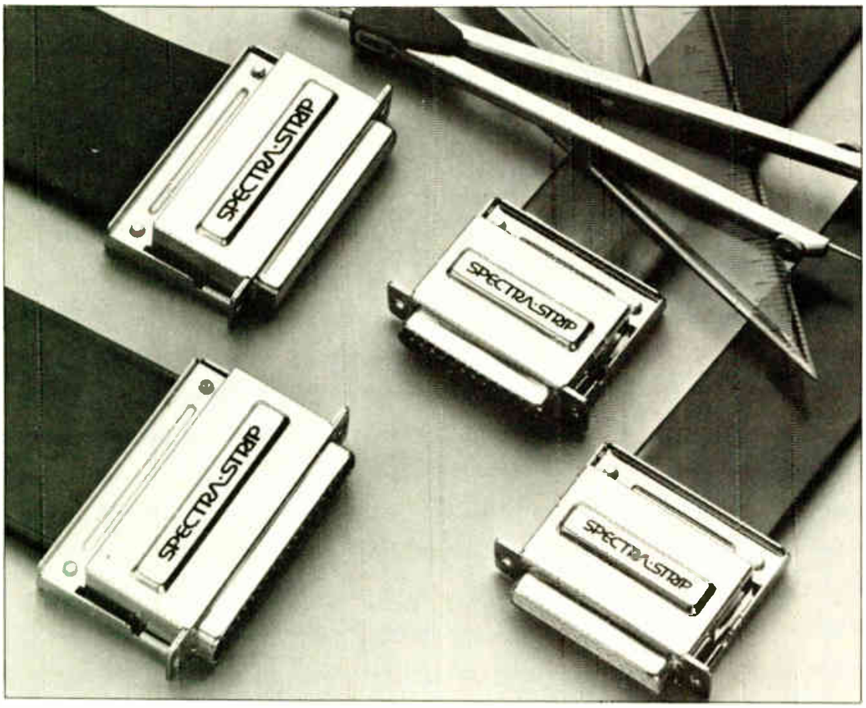


D-subminiature metal backshell that provides emi/rfi protection is now available from Amphenol, a division of Allied Electronic Components Co. Designated as the Spectra-Strip 817 Series, the backshell offers simple two-piece stainless steel construction. The backshell accepts all UL-listed 0.050-in.-pitch jacketed and shielded flat cables and provides strain relief. [412]

vice president of marketing at Kierulff Electronics in Los Angeles, a division of Ducommun Inc.: "Specification problems or misspecifications start with poor communications. Despite years of controversy, consideration by all departments influenced by a design decision are not being given by connector users and manufacturers. All too often, after the user defines the requirement, the manufacturer's representative loses important details when translating them to his or her company. Either the sales engineer must be upgraded, or the loop closed between the user's and manufacturer's engineering departments.

From Specs to Documentation

"Better documentation is another important solution. Prints on items such as IDC assemblies appear deceptively simple; however, missing details can result in major scrap costs because of the quick volume that can be produced on new highly automated production equipment by the manufacturer and at the distributor value-added centers.

"Demands for faster design reaction time are also contributing to more errors. The average gestation time for a new connector design used to be over six months. In the race to be first with new electronic products aimed at the consumer market and fueled by new semiconductor technology, a product can be designed, built, and obsolete in that same time frame. We will never completely rid ourselves of this problem, but by recognizing it, we can learn to control it."

Kierulff is, of course, a major distributor of electronic products, and so is intimately involved with the question of connector specifications. Actually, the "value-added" centers Bergstrom alludes to are, in effect, local manufacturers with many of the same problems as original-equipment makers. In fact, because many a value-added distributor is even more severely handicapped in communications when producing, say, IDC assemblies, he has a good feel for problems in this area.

Waiting is Fatal

A view from another source, Bennett W. Brachman, president, Xport Trading Inc. of Los Angeles which handles ODU Kontakt connectors is that "the major pitfall in specifying connectors is for the user to wait for the last minute to specify connectors and cable, then settle for what is available, instead of what was needed, because of a time restraint."

Some hints on the importance of connector selection were already stated above. The first step for proper selection is to understand some of the purely functional aspects of this process.

A key consideration is the number of positions. While its meaning is rather obvious, the implication is not: the insertion and withdrawal forces are directly proportional to the number of positions (about 4 ounces per contact). According to Mike Wiater, product manager at Thomas & Betts Corp.'s Ansley Electronics division, Raritan, N.J.: "While it is relatively easy to unplug a socket with a few pins (under 10), the chore becomes virtually impossible when pin count reaches 20 or more positions. While the addition of a strain relief may ease the problem somewhat, the best way is to have headers with vertical ejectors. In spite of the small increase in cost, they add greatly to the ease of unplugging a socket, as well as to the elimination of loose connections resulting from too much pulling on the connecting wires."

Another important consideration, duty cycle, has a considerable impact upon the determination of what connector is best for a particular job. For instance, if the only purpose of the connector is to permit separate assembly of a subsystem during manufacturing, then an inexpensive unit with high insertion/withdrawal forces can be specified (without such "luxuries" as vertical ejectors).

Shock and vibration, when discussed in conjunction with a connector, pertain to the ability of the unit to conduct

some rated current continuously. The proper way to test for this is by placing a number of mated connectors on a vibrating and shock table and then subjecting them to the specified vibration and shock. Because the loss of continuity due to either shock or vibration will be very brief, some automatic high-speed instrumentation for monitoring and recording failures should be provided.

Thinking about Space

The space requirement, is seemingly a straightforward consideration, yet it takes some thought. Obviously, in simpler cases (such as circular connectors mounted in the rear of a cabinet), space considerations have no ramifications. To figure out whether or not a given circular connector fits, the OEM simply checks the area on the panel and the space required by the wiring.

With pc-board connectors, however, space considerations may force the designer into real performance tradeoffs. For instance, suppose he or she is selecting a way to connect a pc board to a connector on the panel by means of an IDC flat cable. While the output (panel) end of the cable will, most likely, be terminated in some kind of a D connector, there are at least two choices for the pc-board end—a solder transition socket or a header/socket combination. In the first case, the area required by the socket is less than for the header/socket combo because it has a lower profile (thus allowing closer board spacing). Also, it is generally less expensive than the header/socket combo—but it also has some serious drawbacks.

Overall Cost Is Crucial

Since the cable is permanently attached to the board, scrapping the board means that the associated cable assembly has to go with it. Worse yet, if this technique is used to connect two pc boards (i.e., a case where a flat cable goes from one solder transition socket to another), then the second board might also have to be scrapped.

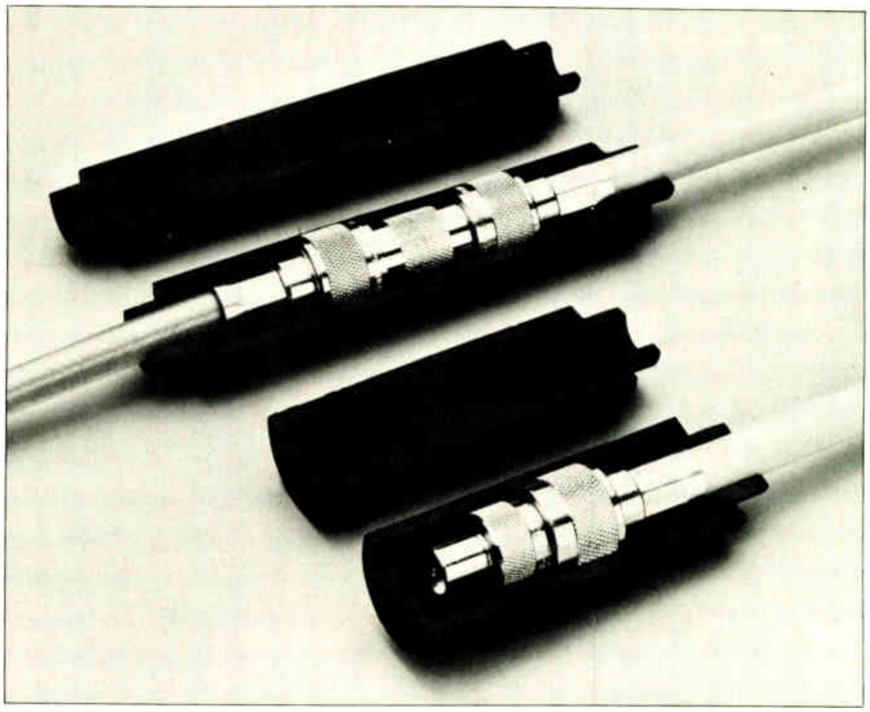
Even if the cable terminates in a panel-mounted (bolted) D connector, then the removal of the board for maintenance and repair involves the removal of that connector. With labor costs being what they are, even a single removal from a crowded panel of a D connector may well justify the use of the header/socket combo instead of the less expensive solder transition socket.

The body material of a connector is one area that is often overlooked. Somehow, there is a tendency to believe that a given material from a given manufacturer will never be changed. However, if a customer wants to have different insulation material and this change does not call for the development of new tooling, such a wish can be accommodated at a very low additional cost.

Contact resistance in a connector is a function of many things including the contact's material and surface condition, the kind of plating used (gold still seems to be the best), applied voltage and current, and the pressure exerted by one contact upon the other. Since all of these factors vary with time and surrounding conditions, users should note that contact resistance in a typical connector varies accordingly.

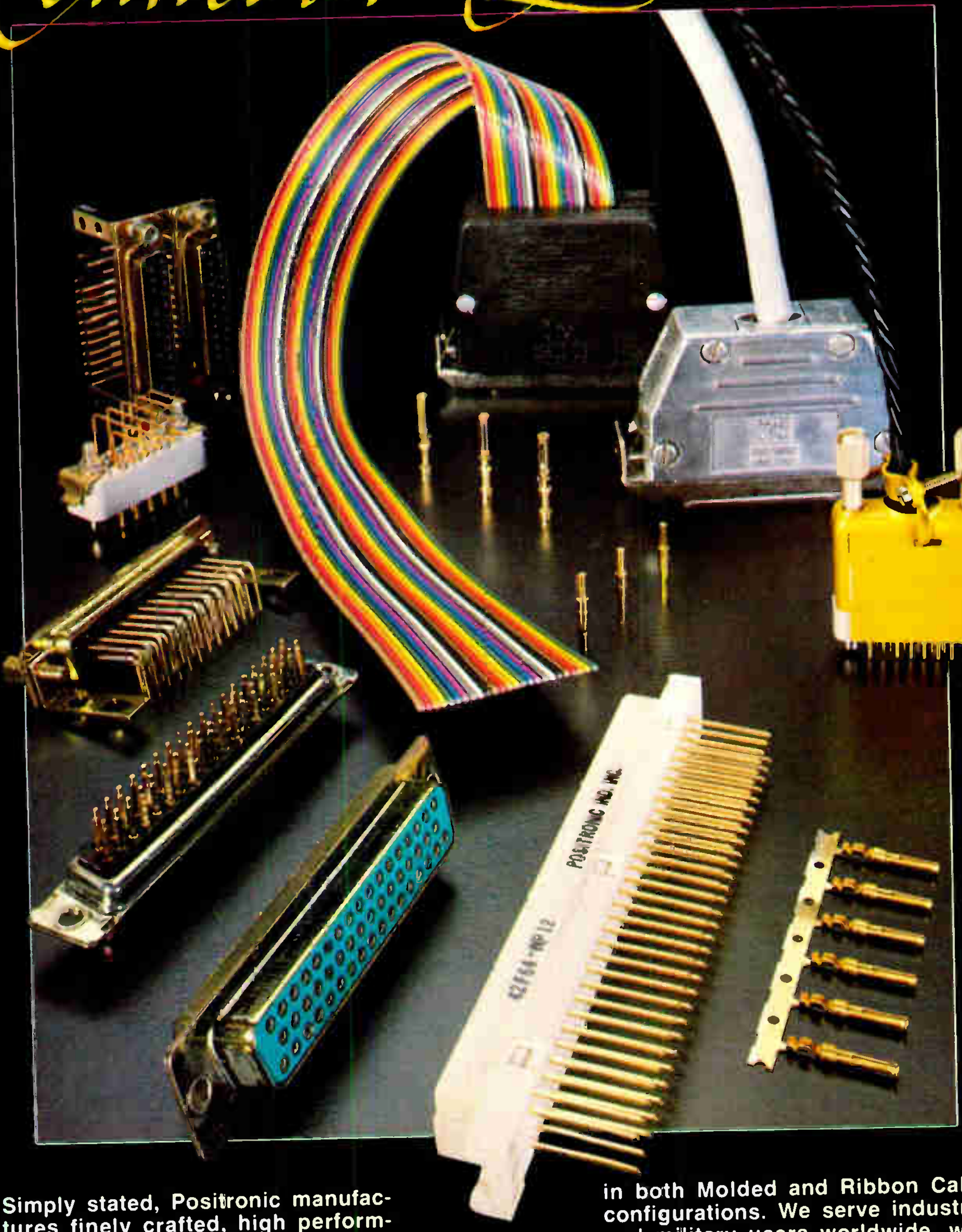
Since some contact resistance will always be present in a practical connector, its stability rather than its absolute magnitude is considered highly important. As a rule of thumb, a contact resistance of less than 10 milliohms at a current of around 0.1 ampere is acceptable in most cases involving the typical signal-level connector.

The next electrical item, crosstalk, is a function of contact spacing, insulation material, and the frequency of the signal passing through a contact—the higher the frequency, the stronger the



Type N coaxial connectors by Amphenol provide interconnection and termination for local-network-standard communications cable bus installations. They can be used in several local-net types, including Ethernet, Decnet, Wangnet, Cablenet, Interlan, and other IEEE-802 systems that use coaxial transmission lines for distributed data processing. [413]

Connector Excellence



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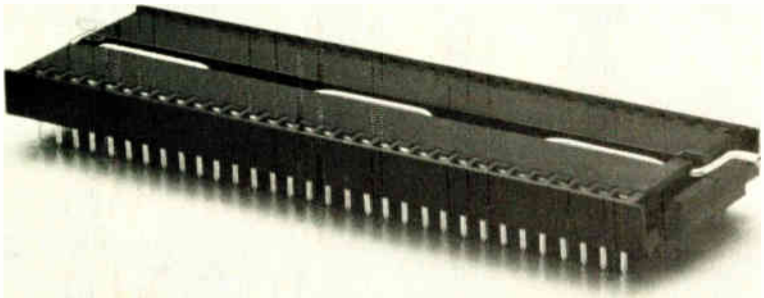


A ZIF 64-position socket from Wells Electronics Inc. operates with an integral lever. As the lever turns 90° either way, two sliding body members close the contacts with a light lead-wiping action. With the lever in its detent position, the IC is locked into place. Available with 24, 28, or 40 leads, the socket stands less than ¼ in. high. [414]

crosstalk. With more and more connectors being used in high-speed data transmission, this consideration takes on added importance. Because connector manufacturers realize the importance of this parameter to many users, most larger vendors have been testing their connectors and will make the test results available to qualified customers.

Buying Tips

Because of the numbers of different connectors on the market, as well as variations in materials, plating, contacts, and other particulars, any designer looking for a connector is advised to be extremely thorough. Finding an extraordinary bargain may be a not-so-subtle hint that an "equivalent" part may not be equivalent in the end. Although there will be differences in prices from manufacturer to manufacturer (and from distributor to distributor), they all will be in the same ballpark.

One aspect of connector buying peculiar to this field is that cable-mounted connectors generally may be purchased either by themselves or assembled to cables. Furthermore, such assembly can be performed either by the component manufacturer or by value-added distributors. Of course, a user can always simply purchase connectors and cable and do the assembly in house.

If the decision is made to buy completed and tested assemblies, then the buyer should strongly consider the local value-added distributor as the source. There are several reasons for doing so.

For one, a local distributor is just that. This propinquity greatly simplifies the problems of deliveries, reject return, and replacement, necessary corrections in manufacturing methods, and others.

For another, where a value-added service is provided by a certified distributor, the manufacturer stands behind his products with an unconditional guarantee. If a unit is faulty, there are no arguments: the manufacturer replaces it.

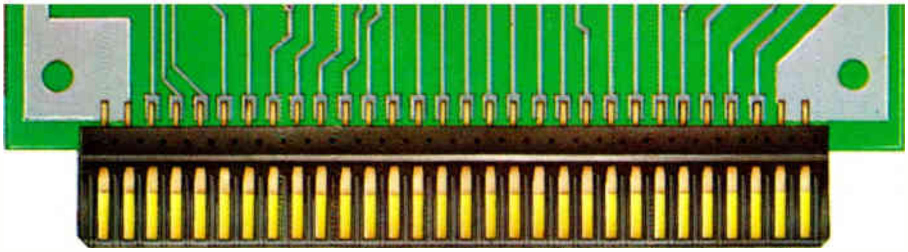
Finally, workmanship by a distributor generally is of the same level as that provided by the manufacturer. The manufacturer usually trains distributor personnel, so that a value-added shop may be looked upon as a local extension of the connector manufacturing facilities.

In addition to the value-added distributor manufacturing operations, there are job shops that provide manufacturing and assembly services on contract. Here the buyer should be rather careful. Such a shop owes no allegiance to any specific manufacturer. Thus, if it receives an order to make a quantity of IDC flat-cable/connector assemblies, it may attempt to use the lowest-cost components it can find. In the process, parts made by different manufacturers may fail to perform due to incompatibility. This situation can be easily prevented by specifying vendors and by a close monitoring of the manufacturing operation.

When it comes to specification interpreting, no amount of caution is excessive. In examining connector specs from different manufacturers it is important to be able to relate various data to the problem on hand.

For instance, suppose manufacturer "A" says that his sockets (female connector contacts) are made from beryllium copper, while manufacturer "B" says that his contacts are made from some other material or does not say anything at all. The price from "A" is somewhat higher than that by "B," while all other parameters appear to be identical. Since beryllium copper is considered to be among the best materials for applications where good electrical conductivity and long-term spring action are required, it is possible that the lower price by "B" is due to the fact that it uses an inferior contact material.

Since a typical designer cannot be an expert in all fields, there is a good, fast, and inexpensive way to get some connector education—talk to a number of competing connector salesmen and manufacturers. During their presentations, every one of them will praise his or her own products versus the competition. Thus, after a few in-depth sessions, one should be able to compile a rather extensive listing of product benefits and shortcomings pertinent to the application. With such a list in hand, a vendor selection can be made with a bit more insight than by simply examining product specs and descriptions from prospective vendors.



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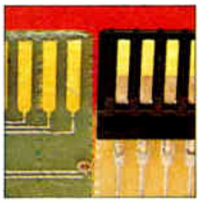
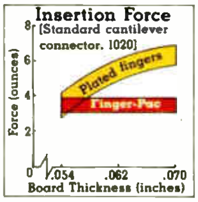
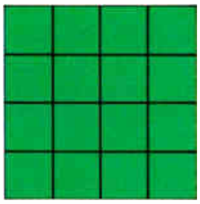




Savings by design.
Finger-Pac's durable inlaid gold means more mating cycles than gold-plated fingers. Its positioning ribs straighten your board — and center it within the mating connector — for uniform contact and reduced gold wear.



Money-saving repairability.
Unlike plated fingers, Finger-Pac contacts can be conveniently repaired in the field. You can replace an individual Finger-Pac contact in about one minute.

Less gold wear = More savings.
Finger-Pac's smooth molded lead-in edge — made of Ryton® polyphenylene sulfide resin — reduces wear on the gold surface of the mating card-edge connector. Minimal thickness (.056") and controlled tolerance (±.0015") add up to predictably lower insertion forces.

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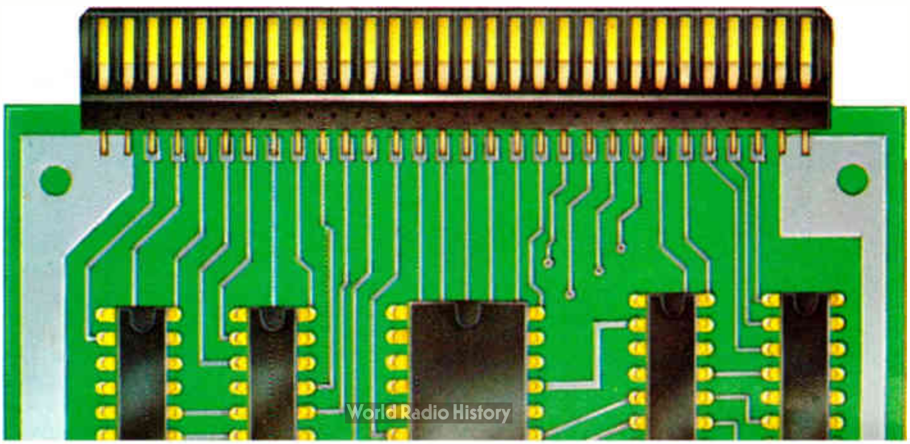

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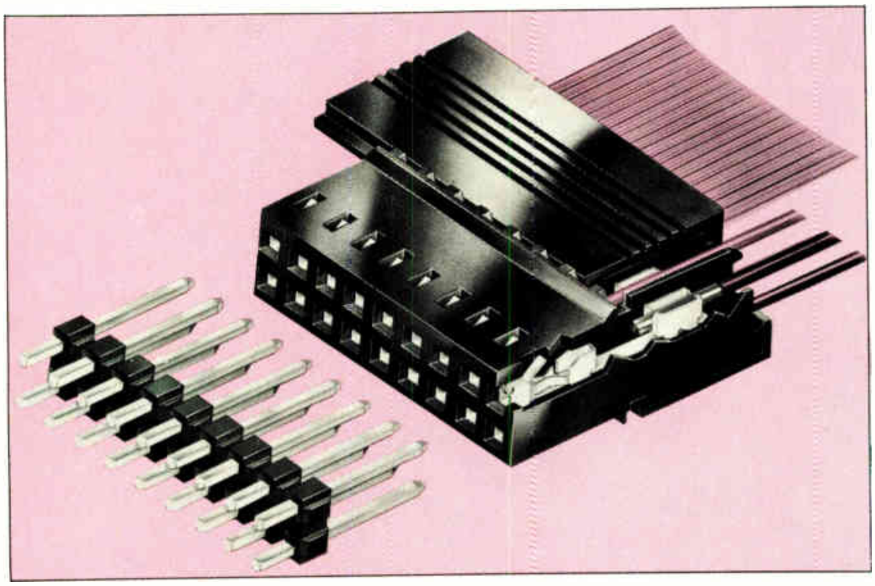
Patent Pending.

KEEPING UP WITH THE STATE OF THE ART IS THE TASK OF ALL CONNECTOR TYPES

Partly because of a lower terminating cost and partly because of the ever-increasing number of conductors in a cable, the IDC (insulation-displacement-contact) connector market has been experiencing a steady 20% or better annual growth. In most data-processing applications, practically every interconnection involves parallel data paths that need a number of parallel conductors. In such applications, the signal levels are low, so the typical 1-A rating of an IDC connector is more than adequate.

A recent innovation, by Molex Inc. of Lisle, Ill., is a dual-row header with a segmented body that can be cut into smaller sections (standard sizes range from 4 to 80 positions). Available as a part of Molex's C-Grid high-density digital-circuit-board interconnection system, the header mates with female connectors on a 0.100-by-0.100-in. grid and is stackable end-to-end. Mating areas of the contacts are selectively plated (15 or 30 microinches of gold).

Another interesting approach to IDC packaging is by Panduit Corp of Tinley Park, Ill., in its new line of Lat-Con connectors with up to 50 positions that accepts 0.050-in. flat cable laterally. That is to say, unlike most other connectors, the Lat-Con units open up on one end and the cable is inserted sideways. According to the company, this configuration greatly simplifies daisy-chain terminations because each connector can be placed on the cable at any point without disturbing any other connectors. Furthermore, daisy chaining can be accomplished even after other sockets have been attached to the ends of the cable. The company also claims that the lateral cable insertion method replaces the difficult and time-consuming process of axial insertion of the cable end ("threading the needle") into the narrow slot of a socket or press.



A dual-row header from Molex Inc. on a 0.100-in. matrix, offers 0.025-in.^{2} pins selectively plated with gold and a segmented body that can be cut to create smaller headers. Molex's wire-to-board connector permits mass termination of either discrete wire or 0.100-in.-pitch flat cable. Protective covers of flame-retardant thermoplastic slide on after the wires are terminated. [415]

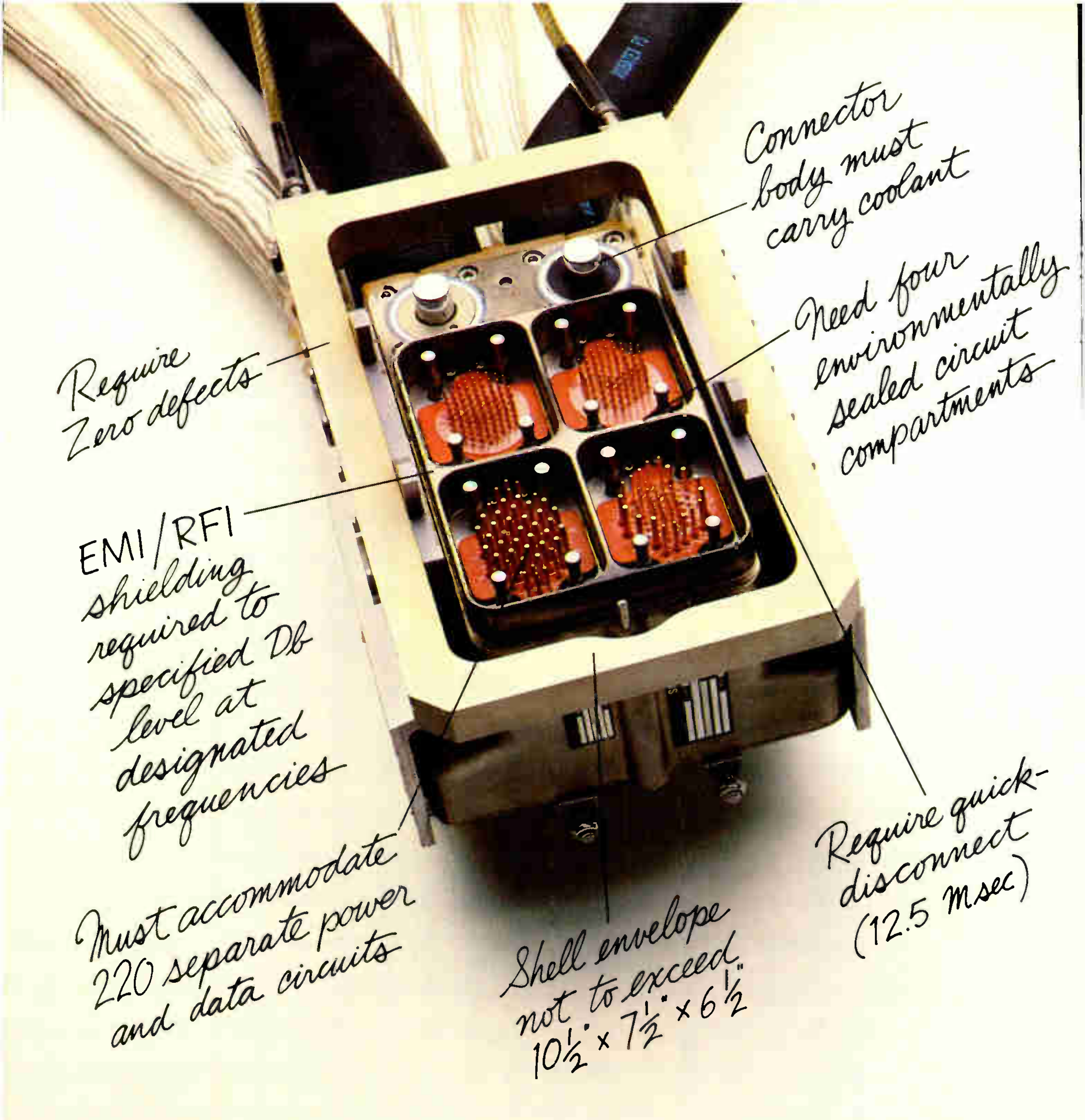
This enumeration of novel approaches to the IDC technology could go on, further reinforcing the point made earlier—in a search for an IDC connector, it pays to conduct a very thorough survey of available products before asking for a "special." Chances are that someone, somewhere, is making the exact connector needed. On the other hand, according to David Beck, product manager for Viking Connectors Inc. of Chatsworth, Calif.: "Connectors are a very diverse field, which at least has the advantage of leaving room for a multitude of manufacturers. But common is the feeling 'whatever you make, they always want some variation you don't have.' "

Fighting Emi/Rfi

The emi/rfi problem has been with us since the time when electricity was put to commercial use. In recent years, however, several new developments helped to bring the problem into a sharper focus:

- The proliferation of delicate and sensitive ICs (often complementary-MOS) in all kinds of industrial, military, commercial, and consumer products.
- Increased transmissions of very fast signals, both over wire and air.
- Increased pressure from the Federal Communications Commission, notably its recent regulation, Docket 20780.

The FCC believes that high-speed data transmission is the major emi/rfi culprit and is responsible for interference with radio and television reception. For this reason, the new regulation addresses itself to "computing devices" that includes an amazing variety of equipment only remotely associated with computing. Thus electronic games and digital telephones are in this category. Broadly speaking, the regulation covers any



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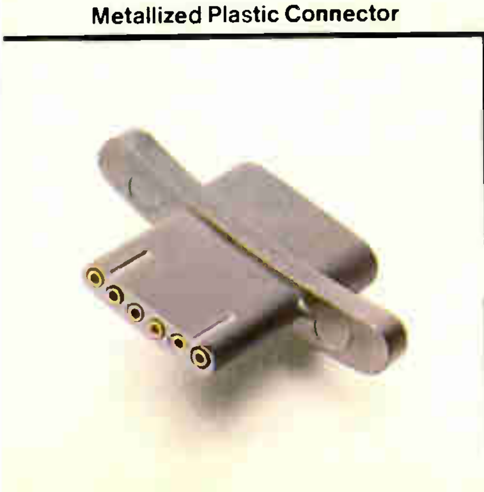

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CONNECTORS

reduce the amount of gold plating. This motive has been largely responsible for the acceptance of two-piece connectors instead of the traditional card-edge designs.

■ The demand on designers to come up with pc boards with higher functional integration. The need to achieve ever higher densities forces manufacturers of pc-board connectors to develop new products continuously.

Making Choices

Addressing the problem of higher density, Jean L. Littrell, Corporate Marketing Communications Manager for Stanford Applied Engineering, Santa Clara, Calif., says: "Connectors and interconnections are very important to the designer as the density of the board increases." Standard edge-board and pc connectors are "the least expensive method. They are excellent for single, double-sized, or multilayer boards.

"This type of connector is limited to the number of fingers on the pc board. For high-density high-speed applications, the logical choice is the two-piece connector. This is ideal for dry-circuitry (measured in milliamperes) applications and standard applications. The two-piece units cost more.

Press-Fitting

"Another way to achieve high density and reliability is to use the press-fit technique. The pins are staked into the board and then the insulator is press-fit over the contacts, thus eliminating the possibility of cold solder joints with expensive rework and unrepairable backplanes. This is a big consideration—backplanes are very costly. If pc/edge-board connectors are used, then the backplane is virtually unrepairable."

As Littrell points out, there are two problems with the card-edge connectors—limited numbers of pc-board fingers and the need to overplate those fingers. For these reasons, there is a universal trend today away from the card-edge approach to the two-piece design.

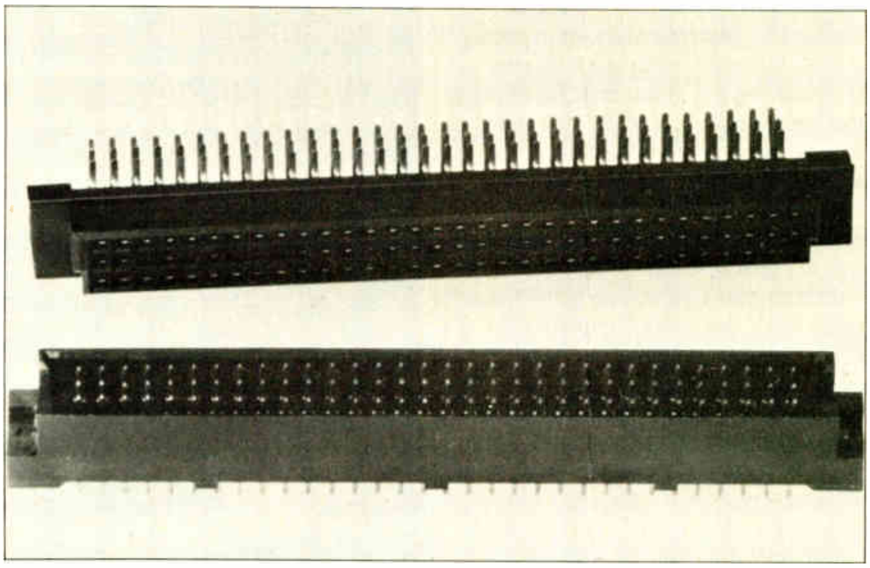
In a two-piece connector, the manufacturer will still plate the mating areas of the contacts. In doing so, he can use the exact amount of gold that may be needed to provide a reliable connection, because he is in full control of both connector halves.

Two-Piece Pluses

There are other considerations in favor of the two-piece design. For one, board thickness is no longer critical, as it is with the card-edge connector. Secondly, if the connector develops a problem, then the user can replace it and save the board. With card-edge connectors, a bad pc-board finger may mean that the whole board may have to be scrapped.

As this trend toward the two-piece pc connector picks up speed, there is growing acceptance of the Eurocard design—a two-piece connector based upon the European standard for two-piece pc connectors, DIN 41612. While this standard has been widely accepted in Europe it is only recently that it has begun gaining popularity and acceptance in the U.S.

There are several reasons for this acceptance. One reason is strictly functional—a three-row DIN connector with 96 contacts on a standard 0.100-in. grid will occupy the same space as a conventional card-edge configuration with about 60 contacts. It also offers relatively low insertion forces—around 3.5 oz per contact, whereas a MIL-C-21097 permits card-edge units to have insertion forces as high as 16 oz per contact. In fact, because of a number of desirable performance and design features, the DIN specification was recently incorporated into the MIL-C-55302 standard.



The Inverse DIN System from Elfab Corp. consists of a female right-angle connector that is flow-soldered onto a daughter board, plus a male press-fit connector mounted on the backplane. The male connector features Elfab's new press-fit compliant pin, which offers ease of installation as well as excellent repair characteristics. [417]

DIN Popularity

Another reason for acceptance of DIN 41612 is the degree of standardization it offers. First of all, a DIN connector must meet a number of dimensional requirements, including proper polarization.

In addition, meeting the DIN specification essentially means meeting four groups of functional tests. Group A tests serve to check the mechanical and environmental operating characteristics. Group B tests check the contact performance by subjecting a connector to 200 insertion and withdrawal cycles in a corrosive environment. Group C tests check long-term contact characteristics, electrical performance at maximum current, as well as the abilty to take 500 insertion/withdrawal cycles. Group D tests check contact and insulation resistances.

Standardization is Key

In other words, a user purchasing DIN connectors from any reputable manufacturer can be rather confident that a connector from manufacturer "A" will mate with a corresponding DIN part from manufacturer "B." This standardization permits a designer a degree of flexibility in design, selection, and purchasing that can go a long way in meeting production and delivery schedules. And, of course, a designer can expect uniform performance and reliability from a DIN part.

In addition to the DIN standard configuration—pins on the board, sockets on the plug—there is also the reversed, or inverted, DIN setup. Here, sockets are placed on the board and the less expensive pins go on the back panel. This configuration enhances repairability, for the pins may be worked on in either position, whereas sockets nearly always must be unplugged.

Lower the Force

The push toward higher pc-board densities and the increasing number of functions in modern large-scale and very large-scale integrated packages is fueling the development of low-insertion-force (LIF) and zero-insertion-force (ZIF) sockets with hundreds of contacts in a single unit. The reason for the LIF and ZIF designs is obvious—a conventional connector with, say, 400 contacts each requiring about 3.5 oz, of force will need about 100 pounds to engage or disengage it.

Backplanes (motherboards) have been around for quite some time in a variety of systems ranging from computers to industrial controls and military applications. Backplane production is a thriving industry that, according to some sources, will grow to an annual volume approaching $3 billion by 1986.

A backplane essentially is a large pc board (or a metal panel). It serves both as a mechanical support for the daughter boards and as a distribution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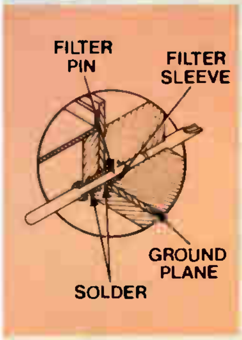

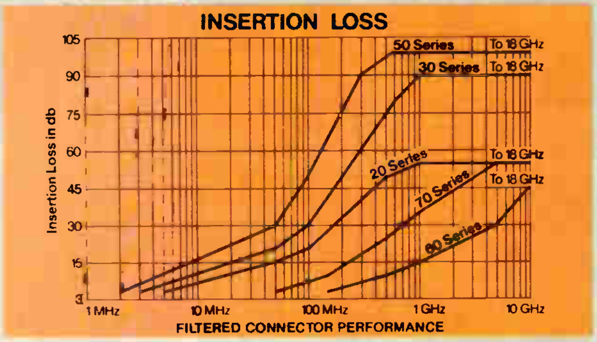

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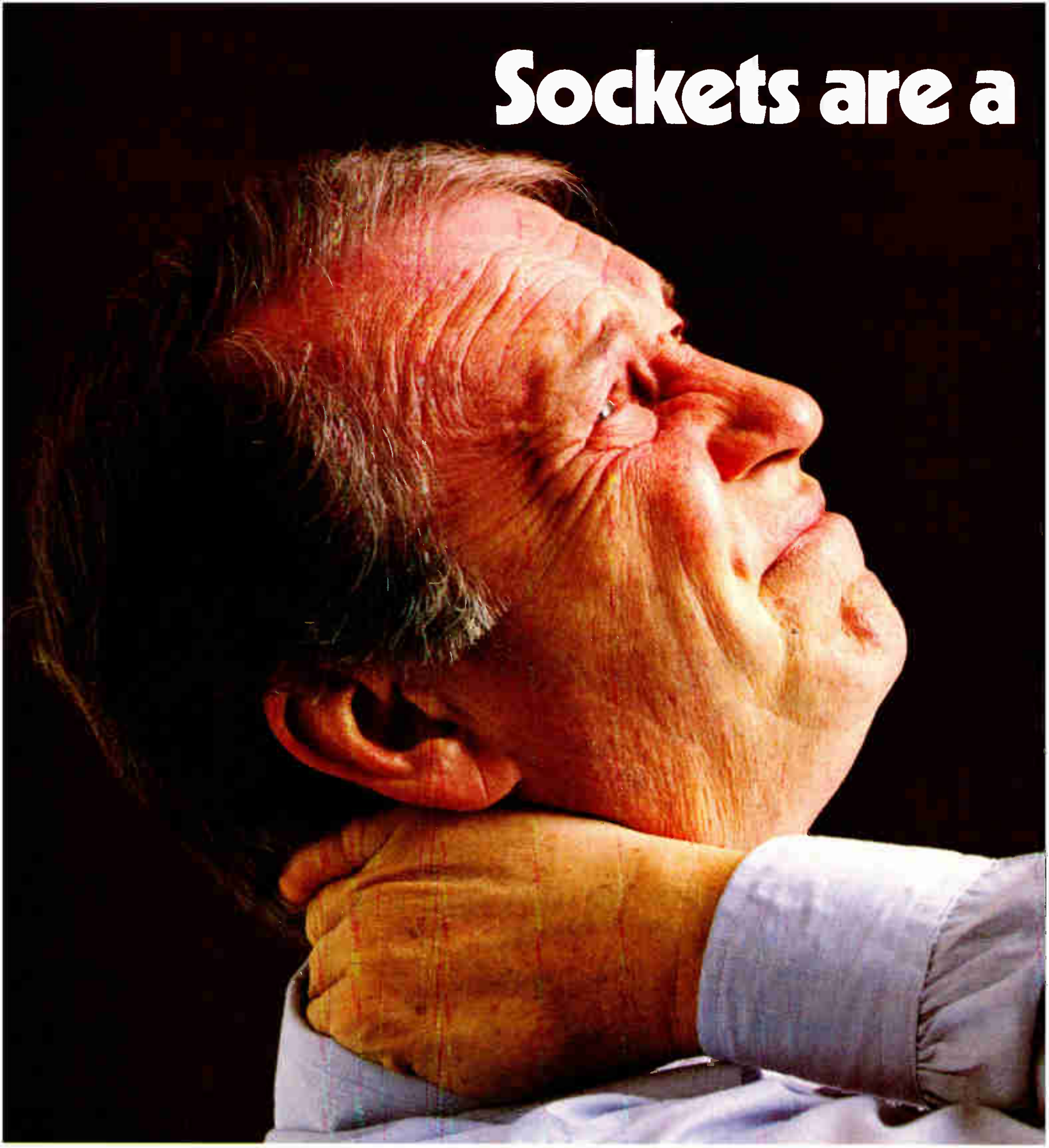

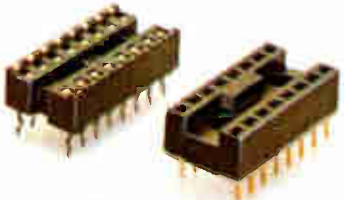

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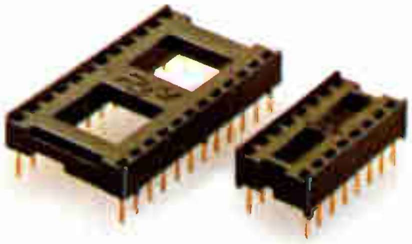

Low Profile Sockets
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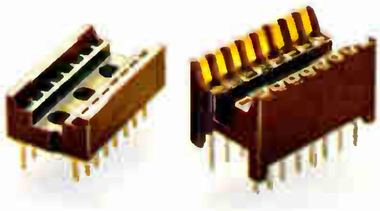

Burn-in Sockets
Circle No. 200

bus for their signals and their operating power. It has a number of connectors, usually headers (male pins, although, as mentioned earlier there is a trend toward a reversed DIN standard where sockets rather than pins go on the board). The connectors accept daughter boards on their mating ends while their back connections are made either by wire wrapping or by soldering. It should be noted that while wire-wrapped backplanes are preferred by the military, the general usage is going more and more toward solder connections.

After years of stagnation, the backplane industry today is alive with the spirit of innovation: as with general pc boards, the backplanes are feeling the demand of LSI and VLSI on accommodating greater densities and higher pin counts. In response, backplanes with multiple layers, increased connector densities, and finer pc lines are appearing. Then, as more and more power-hungry ICs per unit area of a typical backplane are squeezed in, the backplanes are called upon to handle ever higher currents. And as faster and faster signals are demanding bandwidths into the gigahertz range, connecting lines of backplanes must serve as controlled-impedance transmission lines.

IC Sockets Flourish

IC interconnection products currently account for about 20% to 25% of the overall connector market, according to Dennis Smith, manager of product development at Ansley Electronics. "By the end of 1984, the market is expected to expand by 60%." In spite of this acceptance, there is still a question—why ICs should be socketed rather than soldered?

It is a truism that newly-developed semiconductor devices are generally expensive, but their prices decline steadily as volumes and yields increase. The initial high prices of new ICs are usually accompanied by relatively poor reliability and high failure rates. To improve equipment servicing, Smith explains, it was felt early on that socketing devices for easy removal and replacement (much like the then-familiar vacuum tubes) were both desirable and necessary for ICs to reach their total potential.

In addition, there are other reasons for socketing ICs, according to Smith. To begin with, expensive ICs are often socketed so they may be easily salvaged if the board is scrapped. Also, the ICs are installed after the sockets have been safely soldered in place, thereby avoiding damage by the widely accepted wave soldering technique. Moreover, improvements in technology often make a one-to-one replacement of earlier-generation devices possible. With ICs socketed, such upgrading is quite painless.

Wide Price Range

Although the reasons why a user may want to socket ICs are fairly clear, choosing among different products often is difficult. For instance, prices of several "identical" IC sockets may differ by an order of magnitude. A closer look will show why this is so. There are three basic contact types used in IC sockets today: single- and dual-beam, both of them stamped and formed, and machined.

The single-beam contact is the most widely used. It is stamped and is generally tin-plated. The electrical contact between chip and socket contact is made to the face of the IC. Perhaps the biggest single reason for their popularity is low cost. In high volume, a 16-position socket will sell for 4.3¢ to 4.8¢, or about 0.3¢ per contact. These sockets are characterized by very high contact pressure (required by tin-plated surfaces), making them most suitable for lower-pin-count ICs.

Dual-beam contacts are also stamped and formed. About 60% of them are tin-plated, and the remainder use gold. These contacts come in two varieties—face-wipe that make connection to the wide, flat portion of the IC leg; and edge-wipe that grab the narrow edge of the IC leg. The prices are slightly more than for the single-beam versions.

The machined contact offers the best performance. It consists of a machined outer barrel and a four-leaf, beryllium-copper contact-spring insert. It permits good electrical connection with lower contact forces, making the contacts suitable for higher-pin-count devices. The inner contact spring is usually gold-plated, while the outer sleeve may be either tin- or gold-plated.

These contacts are considerably more expensive than the single-beam variety: a 16-position socket in high volume will command a price of around 34¢ to 36¢. However, they offer a number of significant functional advantages over their stamped and formed counterparts that include:

- No solder wicking. The contact body is completely enclosed on the bottom, isolating the contact area from the tail of the contact. Thus there is no possibility of solder wicking up into the contact—single- and dual-beam contacts use an extra part to fight this condition: an antiwicking wafer.
- Easier entry for IC pins. The relatively large tapered entry provides easy alignment when inserting an IC. This feature makes the socket ideally suited for automatic-insertion production techniques.
- Low contact forces. Gold-plated contacts require lower insertion forces (inherent in a machined contact) in order to reduce the chances of damage to an IC during insertion and removal. This type of contact is well-suited to higher pin counts—24 and higher.
- More contact points. The four individual leafs within the machined contact spring can provide up to four contact points with the leg of an IC. This feature obviously increases connection reliability.
- Better wiping action. Since the contact area in a machined contact is closer to the top of the connector, the wiping action during installation of an IC is increased. This feature also allows a wider tolerance on the IC leg length.
- Better heat dissipation. Because of its larger mass, the machined contact provides better heat dissipation for an IC, serving as a built-in heat sink. □

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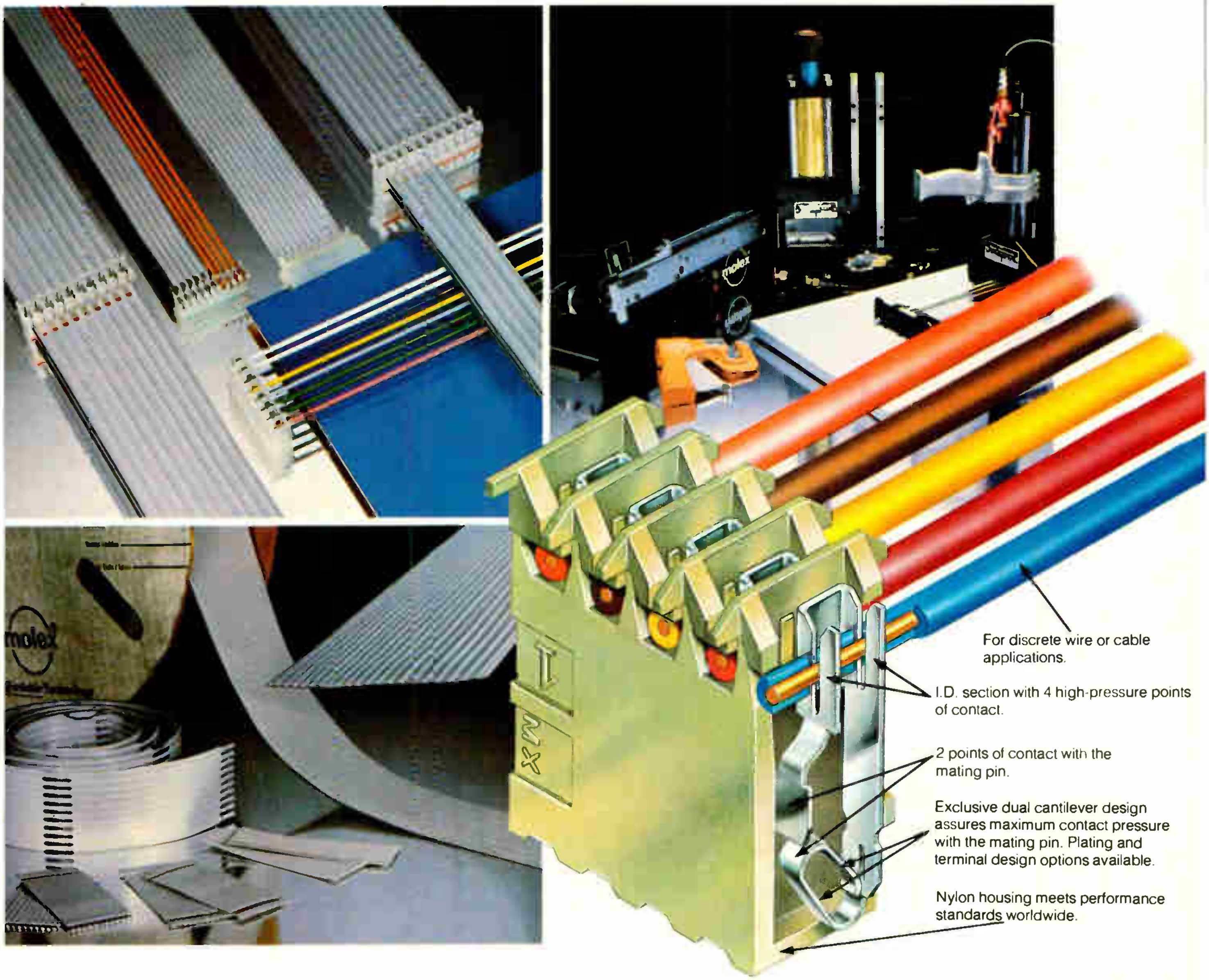

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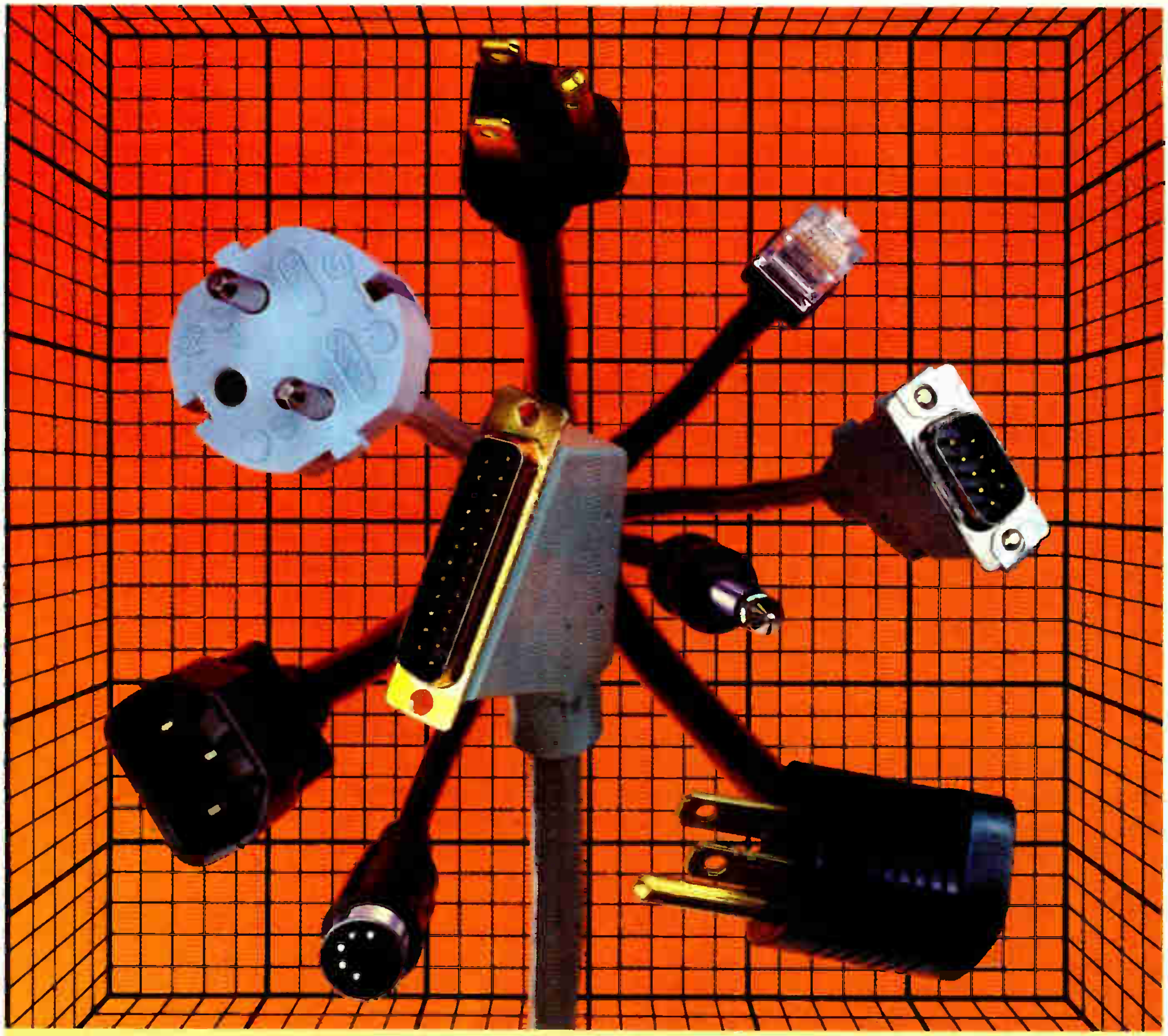

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IC makers warily watch the recovery

Upturn is fueled by demands of small systems, but the fall will show whether mainframes and minicomputers will sustain the trend

by J. Robert Lineback, Dallas bureau

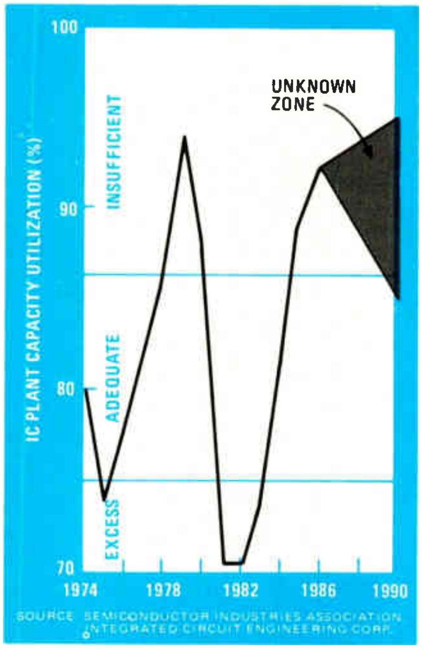
Buoyed by a sudden wave of demand from small-system makers, recession-weary chip makers are prolonging a rare summer fling with record order rates. Although confidence and sales are at last heating up, semiconductor merchants apprehensively await autumn, when many hope to have a clearer view of just how the untested recovery is taking shape.

Pivotal to it all is timing. By the fall, chip vendors hope, the aftershock of any small-system shakeout will be more than offset by the reappearance of their traditional mainframe and minicomputer customers. Too much of a gap between the two recoveries could lead to a minislump, further clouding the long-term outlook. If the two should overlap, however, shortages could hit logic and memory markets next year.

Ironically, much of the enigma can be linked to the industry's technology victories during the three-year recession. While volume sales remained flat, development of cost-effective large-scale integrated circuits continued at a normal pace. Those new chips have, in turn, generated new markets that have not yet been tested in a healthy economy. Also, proliferation into a wide range of commercial and consumer goods has more closely aligned the business with general economic glitches, complicating the tricky art of projecting semiconductor demand.

"I've been at it for 25 years and it's proven a very difficult market to forecast," says William N. Sick, executive vice president of Texas Instruments Inc.'s Dallas-based Semiconductor Group, which saw orders jump to record levels in May and June. "The semiconductor markets are buffered by a number of inventories between end consumer and chip manufacturer. Therefore, upturns tend to cause us to go up a little stronger, while dips hit us harder than the general economy."

Inventories were the malefactor in the 1982 minirecovery that left a number of silicon merchants ramping up production after demand had already abated. In fact, fear of being jilted once again by a false recovery continues to sap industry confidence, says Michael Kubiak, staff economist with the Semiconductor Industries Association, in San Jose, Calif. "Low inventories—which were the result of high interest rates and the long recession—have always played havoc with chip makers," he notes. But this year is different.



Using more. Estimating that first-half book-to-bill ratios hit a record 1.5 to 1, market-research firm ICE also foresees a long upswing in capacity utilization.

"We are seeing a much steeper ramp-up this time compared to the last full recovery, from the 1974–75 recession. It is still unclear whether or not it will sustain itself as long, however," Kubiak adds, noting the last ramp-up lasted more than four years. On the basis of this summer's steep order rates, the SIA is currently revising upward by 3% to 5% its projection of volume through 1986.

Record ratio. Similarly, Integrated Circuit Engineering Corp. now expects that "very healthy book-to-bill ratios of 1.2 to 1.3 [to 1] should be the norm for the fourth quarter of 1983." The Scottsdale, Ariz., market-research firm puts first-half book-to-bill ratios at nearly 1.5 to 1, which is an all-time high.

Anticipating at least 12% growth in semiconductor sales in the combined U. S.-European market, ICE predicts that 1984 could support growth rates around 18%. In Japan, which is expected to see a 16% jump this year, ICE says overall solid-state growth for 1984 will be 22%, with 29% for integrated circuits.

Assuming no new recession occurs later in the decade, U. S. merchant semiconductor production is expected to total $27 billion in 1990, compared with about $9 billion in 1983. With a recession around 1986, U. S. production might reach $18 billion.

Even though U. S. chip makers may now have idle capacity at the front end, much of it will be inadequate to serve the critical new markets that were born during the three-year slump, says W. R. Bottoms, president of Varian Associates' Semiconductor Equipment Group in Palo

Alto, Calif. "The turndown period lasted so long that the technology actually walked away from some of the existing installed capacity," he says, predicting "a considerable crunch in front-end capacity" by the end of the year.

No fear. While equipment suppliers anxiously wait for new orders, chip producers remember a year ago when the 1982 boom went bust, states Jack Beedle, president of In-Stat Inc., a Scottsdale, Ariz., market-research firm. "But this is probably the strongest recovery this industry's ever seen. We can even see allocation in discretes, which has not happened since the mid-1970s."

In Newport Beach, Calif., Rockwell International Corp.'s Gilbert F. Amelio, who heads the Electronics Devices division, cautions, "Bluntly, it's not really over. We're still having headaches." Although memory and logic lead times are being pushed out by strong demand, microprocessor and peripheral chips are "improving, but not great," signifying what may be the first sign of softness in the personal-computer market.

Likewise, Eric Lidow, president of International Rectifier Corp., El Segundo, Calif., believes there is still more to see before declaring the marathon recession finished. The power-circuit producer, which is heavily involved in capital-equipment markets, believes industrial sectors are not eyeing spending yet, with plant use running at only 70%. Further clouding the situation are still-high interest rates, which along with the stronger dollar have "destroyed the export market for high-tech products."

RCA Corp.'s Art Liebschutz, manager of marketing for bipolar ICs and MOS logic at the Solid State division, in Somerville, N. J., believes the recession is indeed over. What's more, he says, it will likely stay that way for at least the next six months because of the trend to lower interest rates, as well as the Reagan Administration's interest in continuing the recovery through the 1984 election.

In Carrollton, Texas, Mostek Corp.'s Timothy Propeck, director of marketing, believes, "This recovery is being driven by consumption on the low end, primarily the personal computer. A lot of the caution you still hear in the industry is because we are having a segmented recovery."

Also seeing a bright picture is James R. Fiebiger, Motorola Inc.'s vice president and assistant general manager of the Semiconductor Products Sector, in Phoenix, Ariz. He says the recovery appears to be in a little better shape than it was in June when he presented semiconductor market projections at San Diego's 1983 Semiconductor Forum.

Good cheer. From Melbourne, Fla., the feeling is also optimistic. Michael Graff, vice president of marketing at Harris Corp.'s Semiconductor Sector, says June and July were key months in declaring the recovery officially on, but "it will probably be September before the industry will be able to gage just how big."

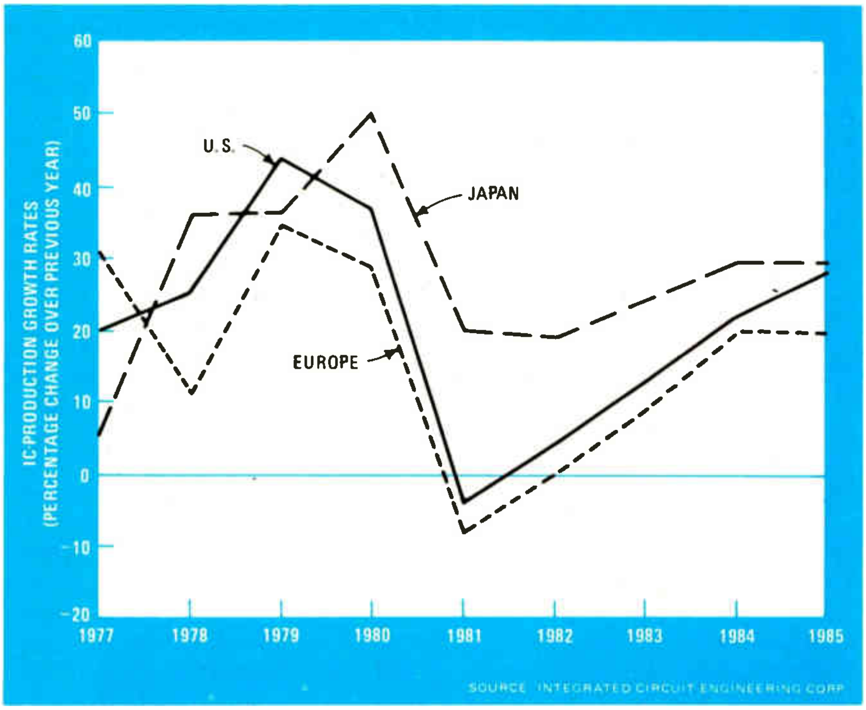
Similarly hopeful are Silicon Valley's chip makers. F. Joseph Van Poppelen, vice president of marketing at National Semiconductor Corp., in Santa Clara, Calif., says that microprocessor-based systems will continue to have a "long-term significant effect on the industry."

Intel Corp.'s Dave House, vice president and general manager of the Microcomputer Group, also in Santa Clara, says the company was caught adding capacity last year when the short upswing turned off, but that actually worked in its favor this year.

Lag overseas. In Europe, the recovery generally lags behind that of the U. S., says Malcom G. Penn, associate director of Dataquest UK Ltd. Just as in 1982, this year started out strongly for West European semiconductor bookings—up 23% to 25% over the fourth quarter, he says. Lack of a strong personal-computer industry is behind the Continent's lag, says Gernot Oswald, managing director of semiconductor sales at Siemens AG in West Germany.

Although jumps in consumer spending have boosted some chip volumes in Japan, sales to office-system manufacturers are accounting for much of the general increases. Fujitsu Ltd. reports it raised its semiconductor production rate by 25.1% last March over the same month in 1982. Hitachi Ltd. adds that, unlike the case in consumer-fueled recoveries of the 1970s, much of its chip shipments are now being consumed by office equipment. And NEC Corp. reports sales to consumer-electronics customers jumped 95% at the beginning of the year. □

Reporting contributed by Linda Lowe, Wesley R. Iversen, Larry Waller, Marilyn A. Harris, Eve Newman, Kiyo Inoue, Robert T. Gallagher, John Gosch, and Kevin Smith.



Growth race. Market-researcher ICE sees U. S. and European IC production growing at a faster rate than Japan's through 1985 and a 12% U. S.-Europe sales growth.

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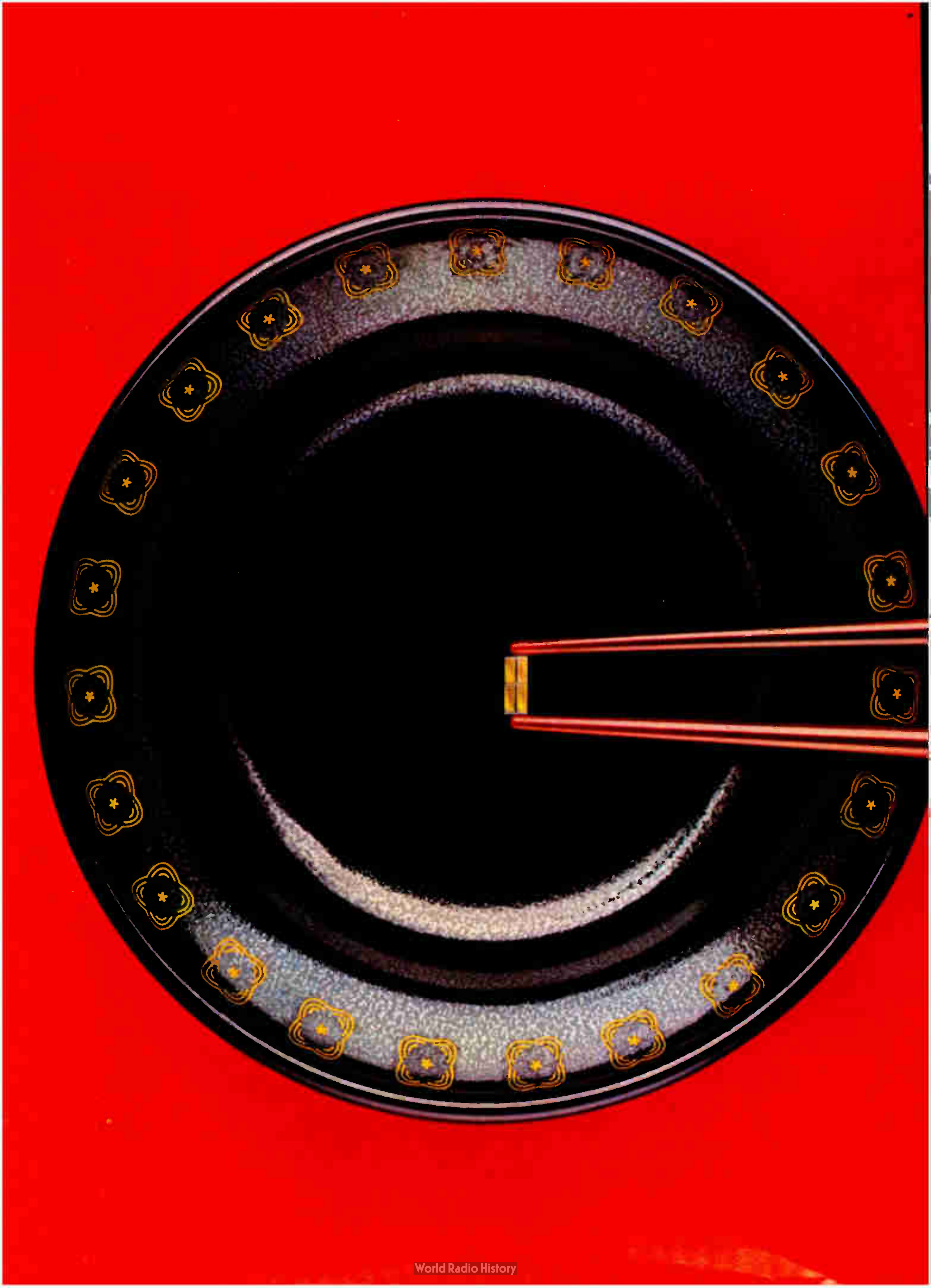

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Packaging & production

Jury still out on 6-in. wafers

IC makers insist on going to 5-in. size first even as equipment makers rush to get new fabrication systems to market

by Jerry Lyman, Packaging & Production Editor

Anyone about to bet that the 6-inch wafer will soon take the semiconductor world by storm had better look for someplace safer to invest his money. For despite the increased productivity that a shift to larger wafers brings and despite efforts by makers of fabrication equipment to rush the necessary new machinery to the market, there is a sharp difference of opinion in the worldwide integrated-circuit industry about whether a quick transition to the 6-inchers should take place.

To be sure, a few companies, like Texas Instruments, Mostek, and Intel, have such plans; but others, like Motorola and National Semiconductor, will stick to their pre-recession schedule of installing new 5-in. lines. Surprisingly, Japanese firms, which unceasingly strive for higher productivity, plan no move to the larger wafers for some time.

On the face of it, IC makers should be eager to leapfrog from their current 4-in. lines directly to 6-in. ones, bypassing the 5-in. step. A 6-in. wafer has 125% more surface area than a 4-in. one, but a 5-in. wafer has only 56% more. That is a better than 2 : 1 increase in differential surface area, and the resulting growth in the number of chip sites per wafer seems enough reason for the jump. However, the higher cost of equipment, the fact that complete lines will not be available before the end of next year, and a disinclination to drop well-laid plans to step up to the 5-in. mark are enough in many cases to offset the advantages.

Still, unlike their customers in the IC business, U. S. makers of lithography and wafer-fabrication gear seem to agree that the future of their $1.4 billion annual market demands that they think big. The upshot is that they are rushing to get 6-in.–compatible versions of their equipment into the field. In fact, some machines are now being delivered.

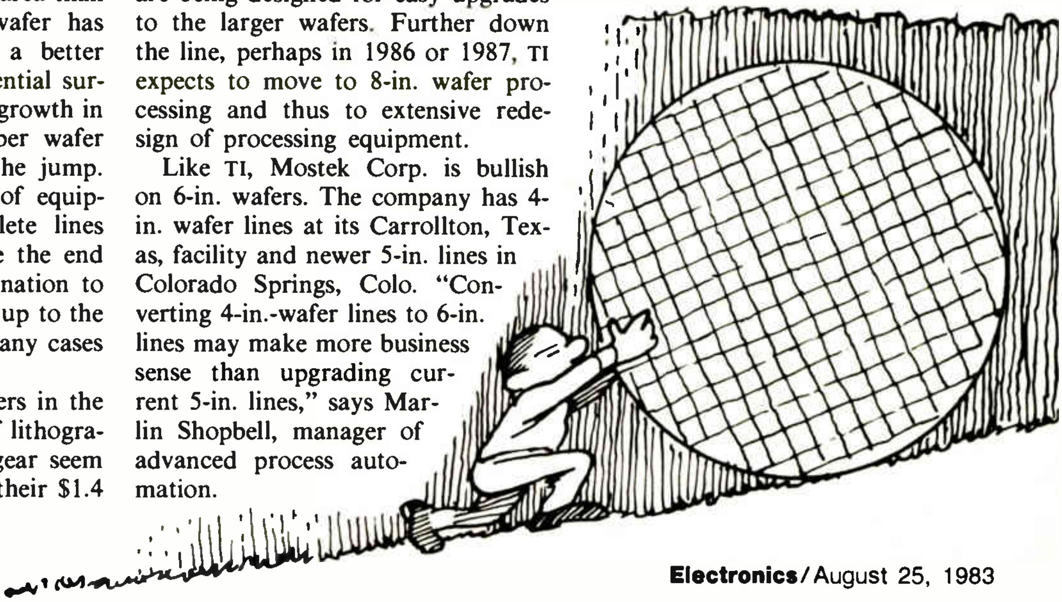
Silicon decisions. Among those inclined toward 6 in., Texas Instruments Inc. is one of the leaders and does not appear to be worried about the availability of new equipment. Walden C. Rhines, manager at TI's advanced development group in Dallas, says, "Most of the equipment necessary to produce and use 6-in. wafers is either already in place on today's leading-edge front ends or is being promised for availability by the beginning of 1984. Certainly, the capability to switch from 5-in. wafers to 6-in. wafers should be in place late this year or early next. So, it's only a tradeoff question of how quickly you want to make the conversions."

Though Rhines refuses to speculate about when TI will implement 6-in. slices, he says the company's new 5-in. front ends, now being installed, are being designed for easy upgrades to the larger wafers. Further down the line, perhaps in 1986 or 1987, TI expects to move to 8-in. wafer processing and thus to extensive redesign of processing equipment.

Like TI, Mostek Corp. is bullish on 6-in. wafers. The company has 4-in. wafer lines at its Carrollton, Texas, facility and newer 5-in. lines in Colorado Springs, Colo. "Converting 4-in.-wafer lines to 6-in. lines may make more business sense than upgrading current 5-in. lines," says Marlin Shopbell, manager of advanced process automation.

Motorola Inc. and National Semiconductor Corp., ranked second and third, respectively, in U. S. IC production, are more conservative in their projections. For example, Tom Filesi, operations manager of materials for Motorola's Semiconductor Sector, Phoenix, Ariz., says that U. S. firms have no reason to push the move to 6-in. wafers at this time, since it is an economic decision based on capacity. Because there is plenty to spare now, Motorola has no plans to move to the larger slice for at least 18 months. In fact, it is still mostly at the 4-in. stage, with only the most advanced lines at 5-in. Filesi says that the worldwide installed base is still struggling to convert to 5-in. slices.

For its part, National, Santa Clara, Calif., has "just completed the conversion to 5-in. equipment on



most" of its lines, says Nelson Walker, director of facilities. "And if we start anything new in the near future, it will be 5 in., too. But six months from now we might give 6-in. serious consideration, and in a year a new line would probably be 6-in. This is because the whole string of equipment is not there yet to build a complete 6-in. fab facility."

The situation in Japan is somewhat the same. Although most IC companies will not reveal any of their plans to change over to 6-in. wafers, the great majority of the Japanese firms are still switching over from 4- to 5-in. wafers. For example, at Toshiba Corp.'s facility in Kawasaki, virtually all production is still in 4-in. wafers. However, Toshiba does have a 5-in. pilot line running at its design center and plans to transfer the technology to full-fledged production plants by the end of this year. But it will be more than two years at best before the company starts making 6-in. wafers.

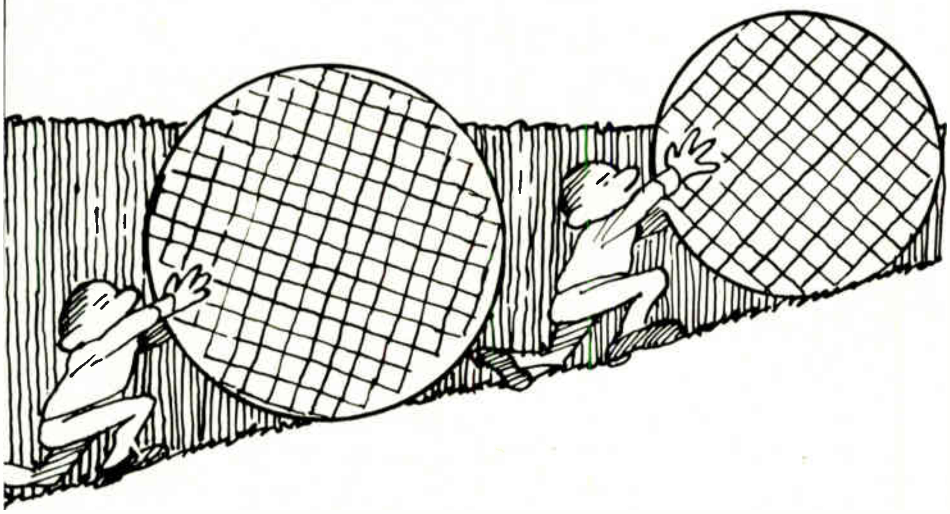
Masakatsu Nakamura, manager of the IC advanced manufacturing engineering department at Toshiba, points out that converting an existing 4-in. line to 5-in. would take at least a month. With current demand healthy, Toshiba cannot afford that kind of shutdown, so it will add 5-in. lines to keep up with demand, not as replacements for 4-in. lines. He believes other Japanese makers are taking the same approach and suspects that Toshiba will do the same when it converts to 6-in. machinery.

The great change. For the equipment industry, it is estimated that a 6-in. line would cost 15% to 25% more than a 5-in. version. The new line, however, would be more economical on a per-chip basis. But all such discussion is academic unless there is a complete array of equipment to implement such a line.

Currently, there are gaps in the lineup both for lithography and for wafer fabrication, the two facets of IC processing. The costliest lithography equipment poses the fewest problems. Big-ticket mask-to-wafer aligners, particularly step-and-repeat projection types, need comparatively little redesign for the shift to 6 in., but the processing modules and the conveyor tracks for the wafers have to be thoroughly reworked.

Comments Aubrey C. Tobey, formerly vice president of marketing at GCA's IC Systems Group, Bedford, Mass., before moving in June to Micronix Corp., Los Gatos, Calif.: "Larger wafers will mean more fluid in the cleaning stage; heavier wafers will mean different spinning speeds for removing the cleaning fluid and spreading the photoresists; and ovens that bake on the photoresists will have to be larger."

As for wafer-fabrication operations—diffusion, ion implantation, deposition, oxidation, and test and inspection—the difficulty of adapting production equipment to 6-in. wafers also varies. However, it appears now that most of the problems associated with the shift upward will be solved by the end of 1984. GCA, for one, is aiming at a mid-1984 debut for a 6-in. Wafertrac fabrication line. On the other hand, Eaton Corp.'s San Jose, Calif., semiconductor equipment operation will be supplying 6-in.–compatible processing modules and a track by year-end.



There already are 6-in.–compatible diffusion furnaces, ion implanters, and wafer probe stations. Not yet available is plasma-etching equipment, especially for the batch mode.

In the important dry-etching field, Applied Materials Inc., Santa Clara, Calif., is developing a 6-in.–compatible version of its hexode plasma reactor. Plasma-Therm Systems Inc., Kresson, N. J., and Anelva Corp., in Japan, already have single-wafer systems for dry etching of 6-in. wafers. And future machines like GCA's reactive-ion-etching single-wafer etcher have 6-in. capability as a design objective.

At least two diffusion-furnace makers, BTU Engineering Corp., Billerica, Mass., and Thermco Products Corp., Orange, Calif., already have units able to process 6-in. wafers. John Fabricus, BTU vice president, says that 40% of its furnaces have 8¼-in.-diameter tubes and are capable, with the proper quartzware, of running 6-in. wafers. BTU also makes furnaces with 7½-in. tubes that can be modified for about $5,000 per tube to accept 6-in. slices.

Ready with 6-in.–compatible equipment right now are the two major manufacturers of ion-implantation equipment, Varian Associates' Extrion division, Gloucester, Mass., and the Nova Implant Systems division of Eaton Corp., Beverly, Mass.

As for testing these large wafers, makers of computer-controlled automatic test equipment care little what size wafers their equipment sees, though wafer-probe–station makers are concerned. Most such firms are in California, such as Electroglas Corp., Santa Clara, and Rucker & Kolls and Pacific Western Systems, both in Mountain View. All are already supplying 6-in. types, and Rucker & Kolls already has an 8-in. prober in development. □

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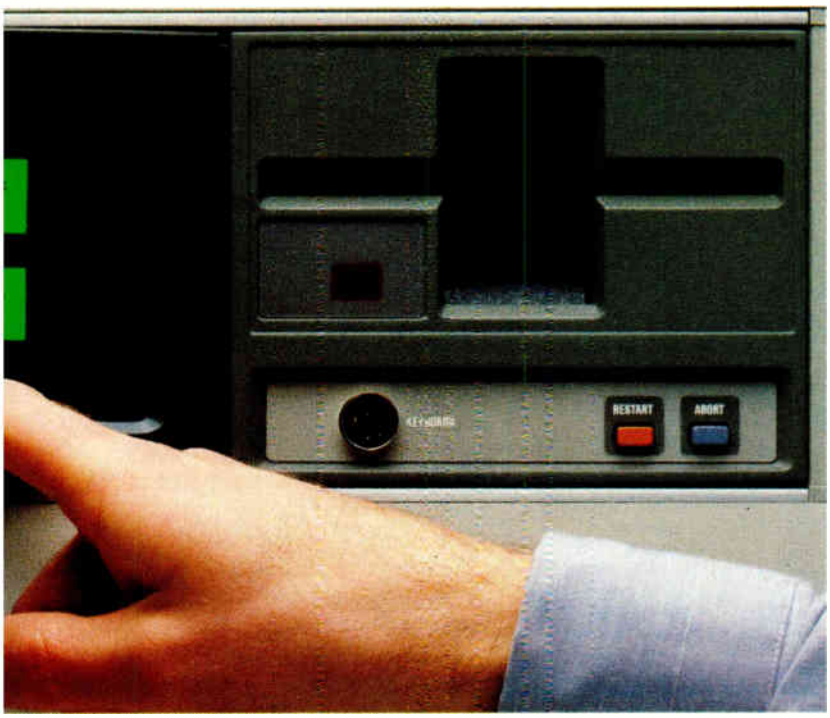

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Telecommunications abroad

Japan's INS taps home-grown technology

NTT has developed its own fiber-optic links, VLSI chips, digital switches, and K-band satellites for a nationwide integrated digital system

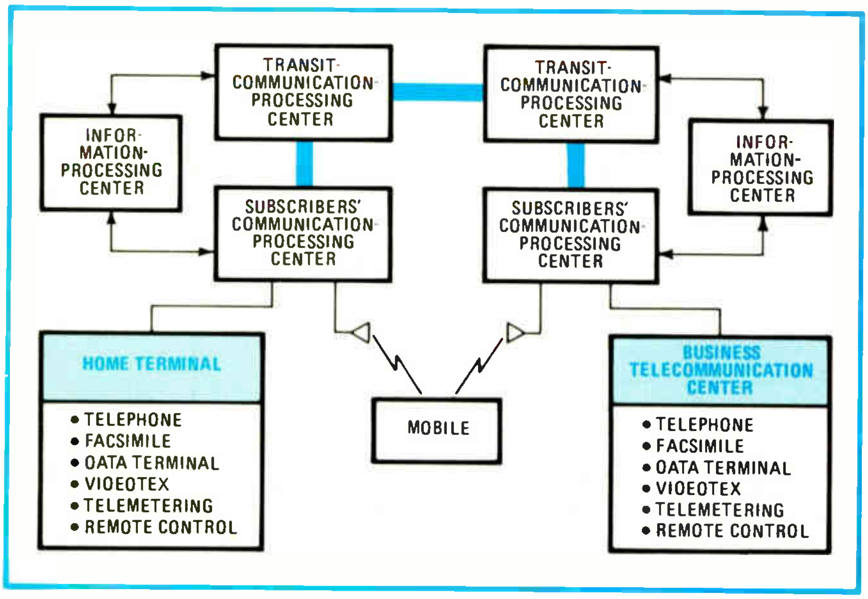
by Michael Berger, Tokyo bureau

Much could happen before Japan brings together all the pieces of its highly touted Information Network System (INS). The scheme is ambitious: under it, by the year 2000 the country is to be blanketed by an integrated all-digital network handling telephone, telex, facsimile, data, and video communications. Should the 20-year project, which could cost as much as $125 billion, fall short of its goal, it won't be for lack of the right technology.

To make sure of that, Nippon Telegraph & Telephone Public Corp., the agency shepherding the effort, has spent heavily for research and development on the leading-edge hardware the Information Network System will need. For basic research alone, NTT's budget will run to an estimated $375 million in the current fiscal year, and it has no fewer than 3,000 or so engineers at work in its four laboratories.

The results of the heavy R&D spending are already evident. "There is no doubt in my mind that the Japanese can build INS without any help," says Don Green, managing director of AT&T, Japan.

NTT is concentrating on four basic sectors, crucial to the kind of network it has in mind. Obviously, it has teams at work on digital switching. Fiber-optic links have come in for considerable attention, since they will turn up both in subscriber lines and trunks. NTT is whetting the technology for satellite circuits, which will carry much of the heavy traffic. The agency has even delved into the basic building blocks for the computers that will direct the vast network, developing a special 256-K random access memory, among other things.



Digitizing Japan. This schematic shows NTT's Information Network System. The plan calls for the phone, telex, facsimile, data, and video network to be complete by the year 2000.

But the most visible achievements so far have surely been in fiber optics. At the end of 1982, 12 fiber-optic transmission systems, ranging in length from 6 to 13 kilometers (3.7 to 8 miles), were operating in Japan. Nine of these systems have transmission capacities of 32 megabits per second, and three run at 100 Mb/s. By December, a 400-Mb/s line that is now undergoing tests should be operating. NTT says that 75 optical-fiber cable links will be in operation by the end of 1984.

Meanwhile, NTT continues to advance the technology. In fact, it successfully performed two significant fiber-optic experiments just this summer. First, NTT transmitted pulses at a rate of 1.6 billion/s—the equivalent of 23,040 telephone channels—over a link 40 km long, without a repeater. For the experiment, the agency put to work a 1.54-micrometer–wavelength distributed-feedback laser that it developed for the purpose of optical transmission [*Electronics,* Nov. 17, 1981, p. 68].

NTT's second summer success was announced in late June. At the Fourth International Conference on Integrated Optics and Optical Fiber Communication, in Tokyo, the agency reported on an experimental optical link 134 km long—the longest without a repeater, it claims. Bell Laboratories demonstrated a 119-km link earlier this year.

Fiber key. NTT credits its achievement to a very low-loss single-mode fiber (0.23 dB/km), to its 1.54-μm distributed-feedback laser transmitter, and to a new type of germanium avalanche photodiode for the receiver. The fiber cable has a capacity of 400 Mb/s, equivalent to 5,760 tele-

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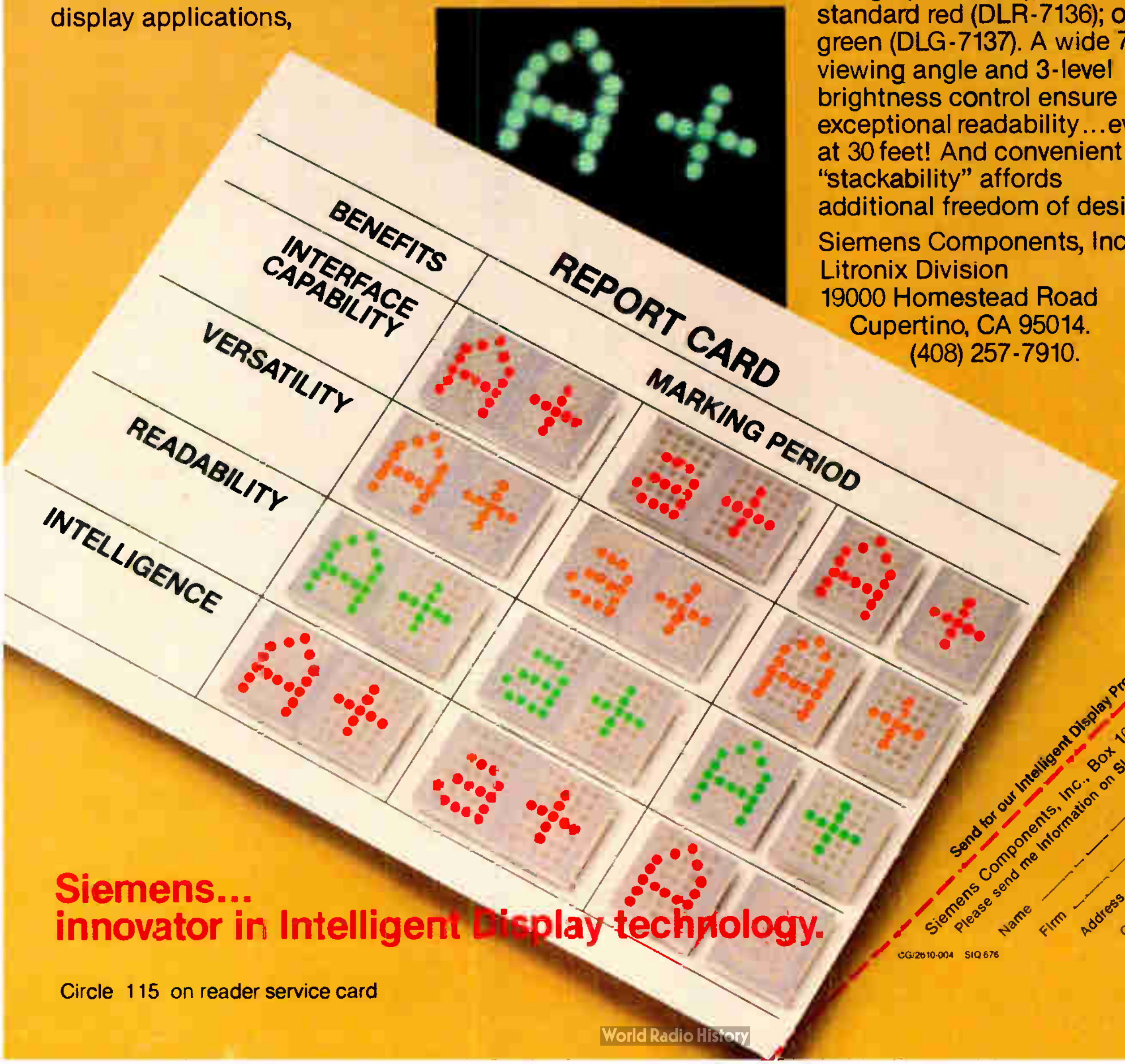

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phone channels. NTT expects to have its long-reach technology ready for field service within three years. At the moment, Japan's the longest repeaterless system in service is about 40 km (24.9 m) long.

Half a dozen years ago NTT developed an in-house technology, vapor axial deposition (VAD), for producing optical fiber. The method synthesizes the glass in the direction of the axis, thus permitting continuous manufacture of the parent body. The process also virtually removes the OH radical during the heating and transparency procedures, so the transmission-loss ratio can be cut to 0.2 dB/km. Although VAD is more complex than Corning Glass Works' vapor phase oxidation (VPO) method, NTT feels that its native technology will be better suited to low-cost mass production.

For short hops, NTT has high hopes for plastic fibers, which figure to be less expensive than glass. NTT has not made any cost estimates, because this research is still in the early stages, but it has pulled deuterated–acrylic-resin fibers that have losses of less than 20 dB/km. The maximum transmission distance achieved with these fibers is 1.3 km, but since that is adequate for circuits inside buildings, plastic optical fibers are on the worklist.

Teamwork. NTT's approach to developing very large-scale integrated circuits, essential for INS' digital switches and high-speed computers, is a cooperative one. At present, NTT's switches and information-processing equipment use 64-K RAM chips that evolved from NTT's joint research with NEC Corp., Hitachi Ltd., and Fujitsu Ltd. By 1985, NTT plans to step up to 256-K RAMS, again the outcome of joint research with private makers.

By the time NTT's 256-K chips start appearing in INS hardware, the country will be well on the way to an all-digital telephone network, which is supposed to be complete by 1986. Further integration of telex, data-communications, facsimile, and video-communications facilities is to come by the mid-1980s, too.

The pace of cutting over digital exchanges has been brisk. Last December, the first digital telephone switch, the D-60, was installed in Tokyo. Testing at a 5,000-circuit capacity, the D-60 is a large-capacity (57,000-circuit) switch for inner cities and outlying areas. By the end of 1984, NTT expects to have 80 digital exchanges in operation.

Soup to nuts. NTT has developed a range of technology, from chips to transponders for satellites whose channels will augument fiber-optic, coaxial, and microwave trunk links. The agency began its nationwide satellite communications services with last February's launching of the CS-2a built by Mitsubishi Heavy Industries on a Japanese version of a Thor-Delta launcher. Nicknamed the Sakura 2, the satellite has quasi-millimeter-wave (30/20 GHz) transponders, which make it the world's first to operate in the K band.

Despite its K-band strengths, the Sakura 2, carrying only 4,000 telephone channels, does not fit into the INS scheme. But NTT has designs for two large satellites that do. They will have capacities between 100,000 and 200,000 channels, and their scheduled launch dates are in 1988 and 1995, respectively.

Technology will not itself determine how the INS project fares in the long run. For INS to succeed, "two basic conditions must be met," admits Tadasu Murakami, director of NTT's engineering bureau. "The first is the establishment of a single, integrated, bit-based tariff system which assigns charges for all services on a bit-guideline basis, according to the amount of information transmitted. The second condition is that these services be provided at a reasonable cost which bears no relationship to distance."

One thing is certain: there is an enormous market for INS-related projects. In NTT's fiscal 1984 capital-spending budget they are earmarked for some \$1.5 billion out of a total of roughly \$7.3 billion. Earlier this year, Prudential-Bache Securities' Tokyo office predicted that the fiber-optic–systems market alone will be worth \$1.04 billion by 1985. Until the end of the century, the growth of INS-system markets will run 19% a year on average, reaching almost \$25 billion by then. □

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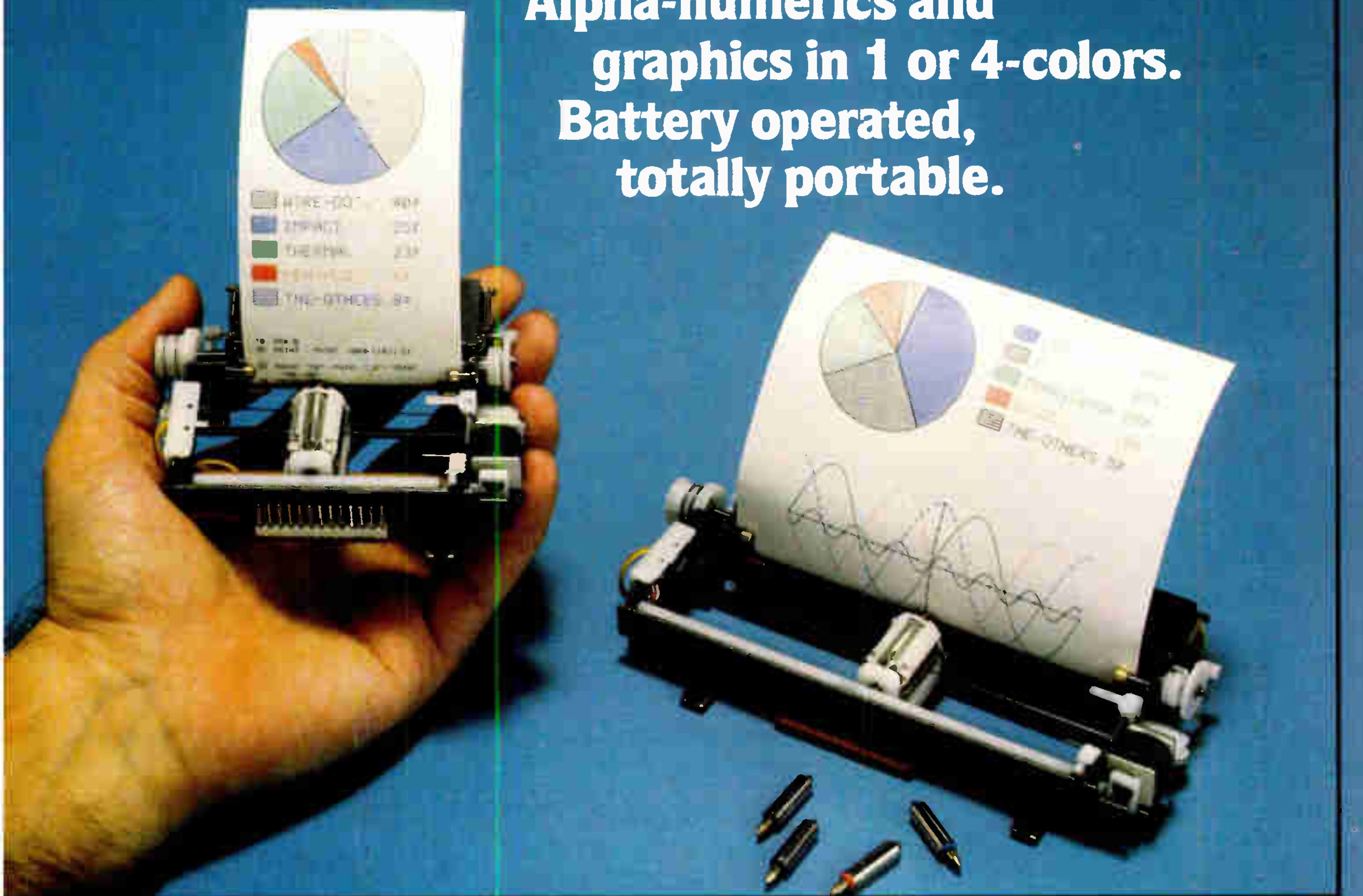


Computer peripherals

Disk-drive makers squabble over norms

This time, the dispute centers on interfaces for 5¼-in. Winchesters; support is split between ESDI and ANSI standards; Seagate is still a mystery

by Clifford Barney, San Francisco regional bureau

Still another skirmish among disk-drive makers over standards now seems inevitable. Last year, makers of microfloppy disks tried to agree on one standard and wound up with four that are now slugging it out. This year, the action has shifted to interfaces for high-density 5¼-inch Winchester disk drives using plated media. Once again, the outcome could be more than one standard.

For plated disks, new interfaces between the drive and its controller are necessary because the media have outstripped the technology for transferring data to and from the disk. So new drive and controller interfaces are now being implemented in drives that will store up to 400 megabytes and are expected to be on the market late this year. At 5 megabits a second, the current Seagate Technology ST506/412 *de facto* standard is too slow. The new interfaces double the data-transfer rate and hence the amount of data that can be stored on the high-density disk at the standard rotational speed of 3,600 rpm.

With the new drives on the way, the market potential is heady (see "How big a market for mini-Winchesters?"). And out of the usual early scramble for market position has arisen the usual dispute over standards.

As a result, a new generation of incompatible equipment is likely. Reacting to separate campaigns for each of two standards, disk makers have split into two factions: one supports the Enhanced Small Disk Interface (ESDI) derived from ST506/412; the other backs the American National Standards Institute (ANSI) specifications developed for 8-in. Winchesters.

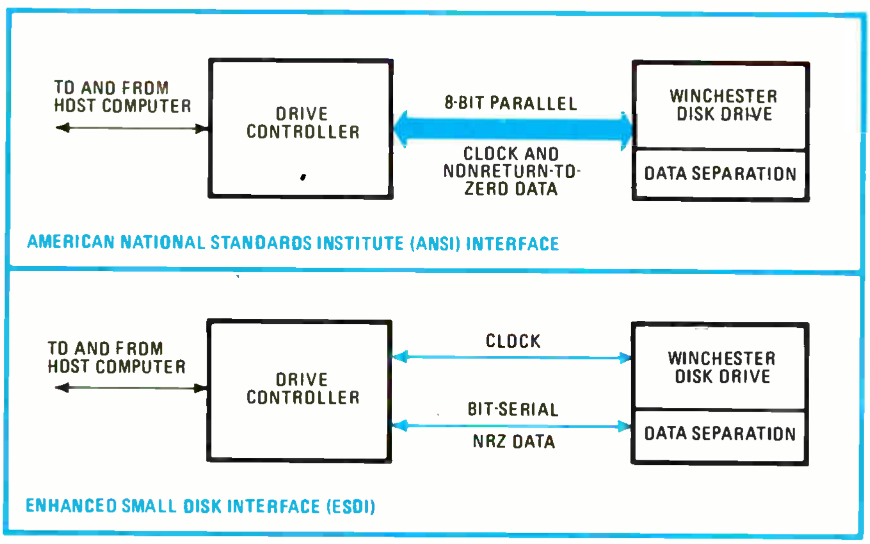
Neither faction shows any sign of compromising. They do agree, however, that Seagate, of Scotts Valley, Calif., could torpedo the whole movement toward a common standard by issuing one of its own.

Although Seagate currently ships only low-capacity disks, it leads the manufacturers of small Winchesters, accounting for some 40% of all units shipped; therefore, any move by Seagate will be significant. The other industry heavyweight, Tandon Corp., Chatsworth, Calif., is reported by industry insiders to be working on a new interface, possibly in cooperation with Seagate.

Thin-film. Both the ANSI and ESDI camps are made up mostly of smaller companies, some of them start-ups formed to exploit plated thin-film media and thin-film heads. This particular combination makes possible 5¼-in. drives that can store up to 400 megabytes.

The ANSI and ESDI interfaces are alike in that they support a 10-Mb/s transfer of data in a nonreturn-to-zero format with a separate clock. In addition, both perform data separation—the conversion of magnetic flux changes on the disk into a digital bit stream—on the drive itself, rather than in the drive controller.

But they differ in the design of the drive bus and in the cabling that is required between the drive and the controller. The ANSI interface has an 8-bit parallel bus and uses a single 50-conductor flat cable that carries multiplexed data and control signals. ESDI transfers data serially and uses 20-conductor cables connected radially from the controller to each drive for data and a 34-conductor daisy-chained cable for control. With the parallel bus, the ANSI interface permits concurrent reading and writing of data; with the radial data cables, ESDI can simultaneously read or



Putting on the gloves. The two contending standards for interfaces for 5¼-inch Winchester disk drives differ in cable requirements and design of the drive bus.

How big a mini-Winchester market?

The first high-performance 5¼-inch Winchester drives will not get to the market until late this year. For that reason, James N. Porter, a Mountain View, Calif., management consultant who tracks disk-drive markets, says it is too early to attempt to make forecasts about their sales. Nonetheless, Dataquest Inc., a market researcher in San Jose, Calif., has had a go at it (see chart below). Its figures, in units, cover drives that incorporate a form of data-rate transfer that differs from the Seagate ST506/412 5-megabit-per-second *de facto* standard. The low-end column, for models with a capacity of up to 30 megabytes, covers drives having interfaces that are modifications of ST506/412 only in the data rate and so do not employ the nonreturn-to-zero (NRZ) formatting used by the ESDI and ANSI interfaces (see accompanying story).

ESTIMATED ANNUAL SHIPMENTS IN UNITS OF HIGH-PERFORMANCE 5¼-IN. WINCHESTER DRIVES

Megabyte capacity	0 – 30	30 – 100	> 100
1984	9,000	1,500	700
1985	139,000	25,800	8,000
1986	580,000	125,000	38,000
1987	1,400,000	267,000	84,000

write and issue necessary commands.

Both interfaces permit easy determination of drive status. Also, by putting data separation on the drive they eliminate one cause of confusion: whether the drive or the controller is responsible for some errors. For data separation, the ST506/412 standard employs a modified fm format that is self-clocked by phase changes in the signal. The NRZ format is strobed by a separate clock.

"Either one of them—ANSI or ESDI—could do the job," says William Roberts, president of Emulex Corp., a controller manufacturer based in Costa Mesa, Calif. "It would be a shame if the industry goes in different directions." Roberts participated in the design of both standards, as a member of ANSI committee X3T9.3, which in the late 1970s came up with the 8-in. standard now called BSR X3.101, and as part of the informal committee that has been writing ESDI.

"The 8-in. ANSI standard just didn't catch on," adds Roberts, explaining why his company is now working on an ESDI controller. Even so, to promote the idea of compromise, he devoted a day early this month to attend an industry forum held in San Jose under the sponsorship of the ANSI group.

Compromise was not in the wind. Last spring, the ESDI faction, led by the Maxtor Corp., Santa Clara, Calif., had announced that 26 manufacturers of 5¼-in. Winchesters and controllers were "endorsing" the ESDI interface. But many of those companies quickly made it known that they merely meant that they would support ESDI if it were attractive to do so.

One of the listed supporters, Priam Corp., San Jose, Calif., subsequently defected to join Xebec, a controller maker in nearby Sunnyvale, in leading the drive to establish the ANSI interface. At the San Jose meeting, Priam and Xebec announced the formation of a nonprofit independent company, DISC Labs Inc., that will "certify" drives and controllers as conforming with the ANSI standard.

The announcement met with little enthusiasm from the assembly, which included 50 representatives of 30 companies (including some integrated-circuit manufacturers, which will make the chips for either kind of equipment). The objections raised at the meeting were mainly practical, concerning the difficulties and cost of testing; privately, several companies expressed serious reservations about submitting a new product for evaluation to any company whose directors came, by design, from competitors.

So far the discussion has been theoretical; there are no 5¼-in. ANSI or ESDI drives on the market because the controllers have not been available for them. But Priam and Xebec promise ANSI drive and controller products by the end of this year. Maxtor and the Control Data Corp., through its Oklahoma City subsidiary, Magnetic Peripherals Inc., plan ESDI versions of their high-capacity Winchesters; and besides Emulex, Data Technology Corp. of Santa Clara, Interphase Corp. of Dallas, and OMTI of Campbell, Calif., will have ESDI controllers also this year.

Going alone. Meanwhile, Seagate, which heretofore has claimed to have found little interest in 100-plus-megabyte drives among users and therefore would not comment about its plans, acknowledged that it is, indeed, working on its own interface. Seagate will have something to say about its intentions late in September, but until it makes them known, both the ANSI and ESDI camps are proceeding with their current plans.

"I can't make a decision based on rumors," says marketing manager Dick Gunderson of OMTI. Priam president William Schroeder is convinced that any Seagate interface based on ST506/412 would undercut ESDI, which itself was derived from that interface; the ESDI camp hopes that the new Seagate interface will actually be close to the "step" mode of ESDI, which is similar to ST506/412 except that it performs NRZ data separation on the drive.

Some observers maintain that the controversy is premature. They point out that the small Winchester market was built on low cost and size, so setting high-performance standards is jumping the gun.

In fact, even some makers of high-performance drives are skeptical. James W. Adkisson, vice president of Vertex Peripherals, San Jose, says that although high data rates and moving the data separator to the drive are clearly industry trends, the writing of detailed specifications for an interface is "presumptuous" before some market leadership has been demonstrated. Seagate seems poised to do just that. □

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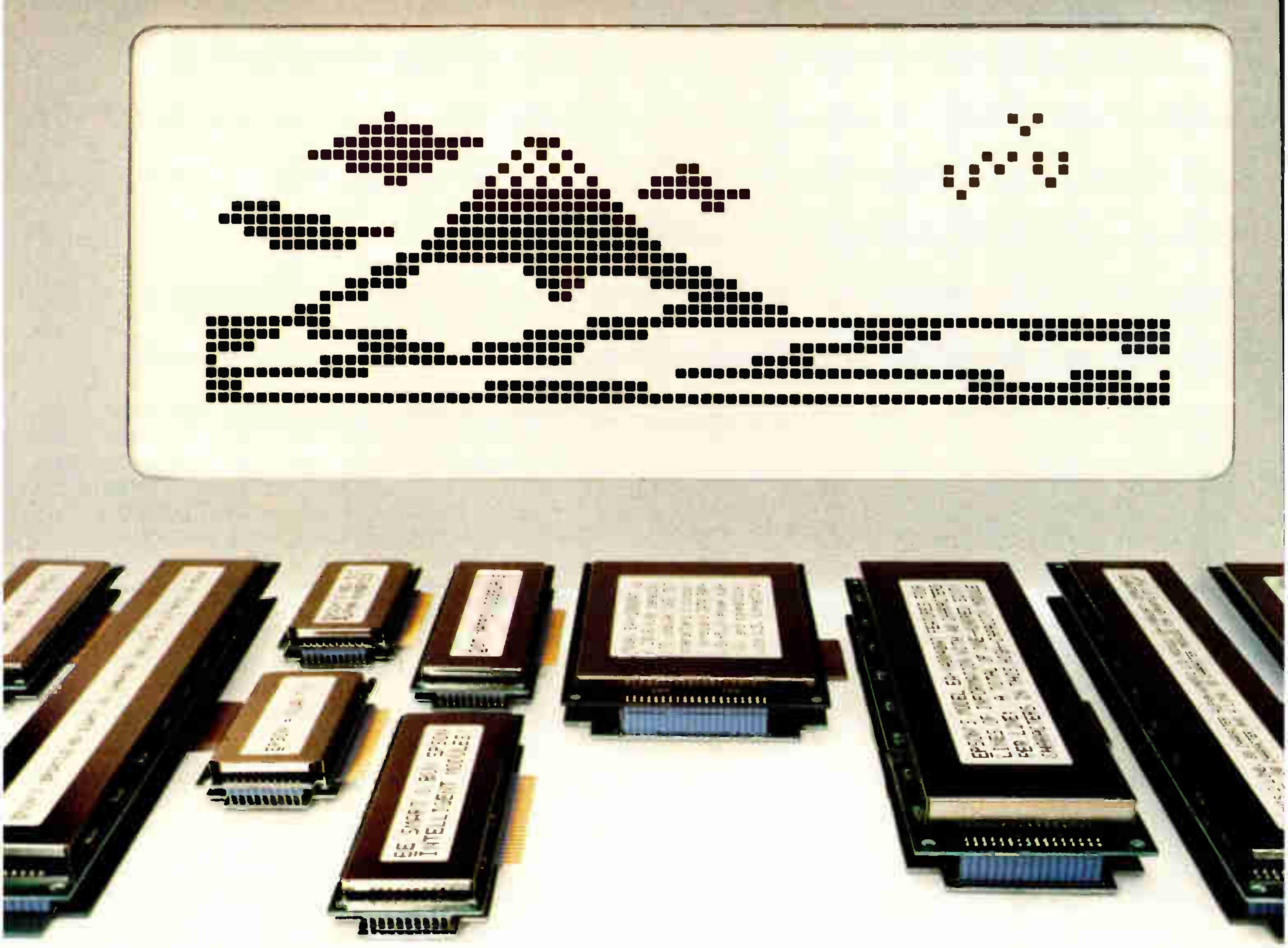

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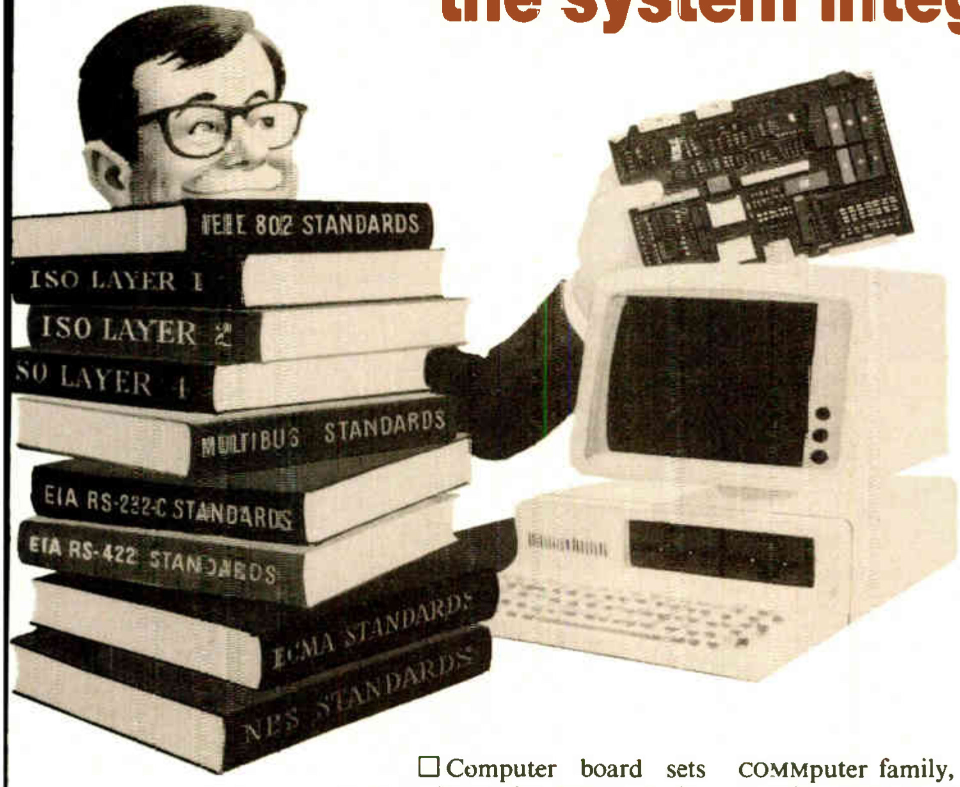
Communicating computer simplifies the system integrator's work

Single board boasts 16-bit processor with integrated support chips and Ethernet coprocessor, as well as an on-board operating system and communications software



by John Ketzner, Kelly Pan, Bob Beach, and Darcy Nelson
Intel Corp., Santa Clara, Calif.

☐ Computer board sets now available for Ethernet—indeed, for any local network accessed by collision-detection methods—are like all first-generation designs: they are large and costly and barely do the job. They lack the interface chips that would make them less expensive to connect to a network. Their computer throughput is diminished by their need to divert microprocessor resources into communication chores. No on-board firmware stores even an operating system, let alone the software layers of the International Standards Organization's reference model for computer communications.

The iSBC 186/51 computer satisfies all these needs for the first time on one board (Fig. 1). It incorporates the iAPX 186 16-bit microprocessor and iRMX 86 operating-system firmware; the 82586 and 82501 Ethernet communication chips [*Electronics*, Oct. 6, 1982, p. 89]; and memory chips for storing Intel's iNA 960 data-communications software, which implements ISO transport layer 4.

The 186/51 is the first of a line of single-board, Multibus-based computers intended for distributed processing. This second-generation family of COMMputers (communicating computers) is committed to national and international standards and open-system connections [*Electronics*, Aug. 11, 1983, p. 116]. All the communicating computers will be flexible enough to relieve system integrators of the burden of developing their own communications hardware and software. Thus, the integrators will be free to concentrate on what they do best for their companies—solve application-level problems and get to market quickly.

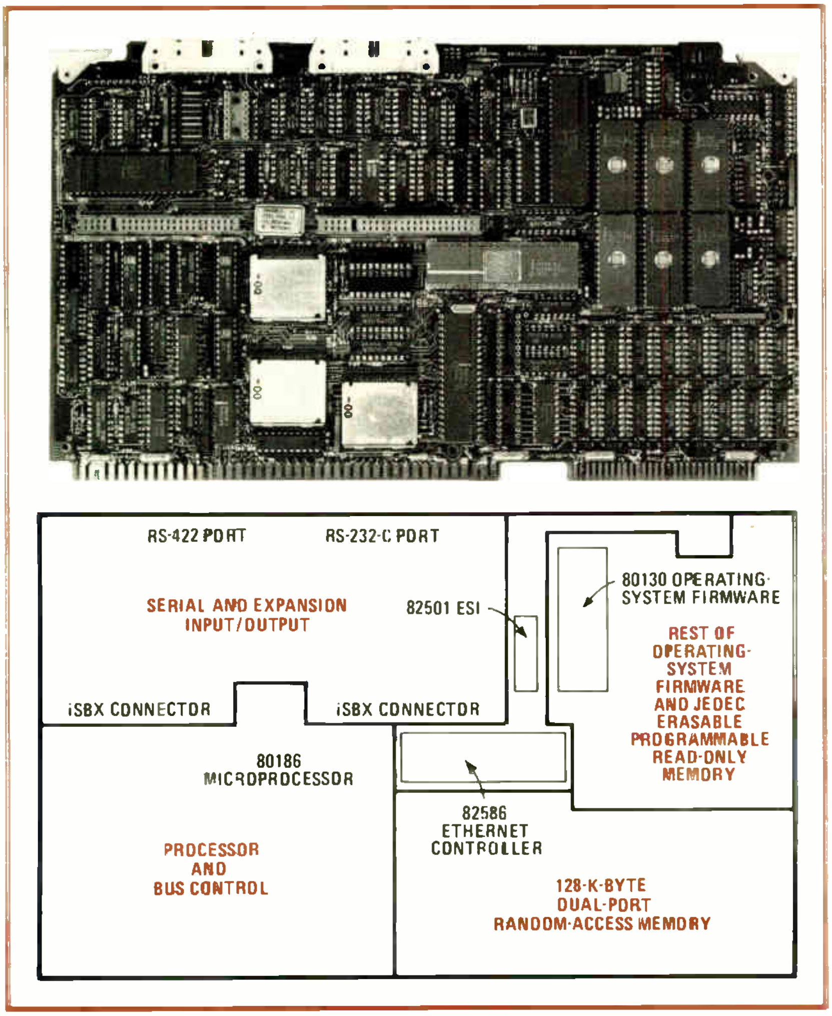
Possible applications for the first member of the COMMputer family, the 186/51 board, are wide-ranging. For instance, a complex industrial process-control network might use several 186/51 boards supported by other Intel boards. Alternatively, a simple, low-cost data-entry work station could conceal just one 186/51 board computer plus a display-electronics board behind its cathode-ray-tube display and keyboard.

Larger throughput

Moreover, system integrators using 186/51 boards can get higher performance out of both software applications and network communications than is possible with multiple-board products. Optimized for computation, it has 1.3 times their computational throughput and nearly twice their communications throughput. Optimized for communications, it provides five times the communications throughput and maintains the same level of computational throughput as current Intel board sets.

There are several reasons for this enhanced performance. The first is that the 80186 offers a 30% speed increase over the 8086. Secondly, the 82586 offloads many of the communications tasks from the processor. Finally, locating the 80186 and 82586 on a single board with local memory makes data transfers between them much more efficient than when they communicate over a Multibus system.

On the communications side, the two Ethernet chips are capable of all carrier-sense, multiple-access/collision-detection (CSMA/CD) communications, as defined by the Institute of Electrical and Electronics Engineers' Local Network Standards Committee. To top it off, the chips work closely with the iNA 960 software, which imple-



1. Fully packed. Intel's single-board communicating computer—the COMMputer—sports a 16-bit microprocessor with integrated support and peripheral chips and computer-communications software conforming to layers 1, 2, 3, and 4 of the International Standards Organization standard for computer communications.

ments ISO's layer 4 transport software. This transport software provides a virtual-circuit facility for reliable delivery of messages and is designed to run both the iRMX 86 real-time operating system and 82586/80186-based component designs.

The 186/51 board's dramatic rise in performance is accompanied by an equally dramatic fall in cost. A one-board functional equivalent of up to three first-generation boards slashes overall system cost. In fact, the cost of communications now adds only slightly to the cost of a processor board. The use of very large-scale, rather than medium-scale, integrated circuits also increases reliability and product life.

Three-part architecture

As Fig. 2 shows, the 186/51 board has three major hardware sections:

- A computation section, consisting of the iAPX 186 central processing unit and the 80130 chip storing the iRMX 86 operating system, plus on-board programmable read-only-memory and erasable PROM chips, programmable timer-counters, and programmable interrupt control.
- An input/output section, in which the 82586 and 82501 chip pair are supported by two programmable serial interfaces, plus two ISBX connectors included for expansion. This section also shares the computation section's timer-counters and interrupt control, which allow user-programmable baud rates for the I/O section's universal synchronous-asynchronous receiver-transmitters as well as the generation of priority-based interrupts from these Usarts. All of this I/O capability is under the control of the on-board 80186 microprocessor.
- A dual-port random-access-memory section, which serves to pass command and status information between the external Multibus masters and the on-board CPU and Ethernet controllers. The dual port also permits blocks of data, received or awaiting transmission, to accumulate in the on-board shared RAM, minimizing the need for an extra, dedicated memory board.

The chief element of the 186/51 board's computation section is of course the 16-bit iAPX 186 microprocessor [*Electronics*, May 5, 1983, p. 139]. This device has many functions integrated onto it that, until now, have had to be supplied by separate chips. For example, it includes the computer system components that take care of direct memory access, interval timing, clock generation, and programmable interrupt control.

The iAPX 186's software instruction set is a superset of the 8086's. Still, it maintains object-code compatibility while adding 10 new instruction types. Added instructions include: block I/O, enter and leave subroutines, push immediate, multiply quick, array bounds checking, shift and rotate by immediate, and pop/push all. Among other features, the iAPX 186 software retains the 8086's variable-length instruction format (including double-operand instructions); 8- and 16-bit signed and unsigned arithmetic operators for binary, binary-coded decimal, and unpacked ASCII data; and iterative word- and byte-string manipulations.

The new block I/O instructions and improved execution times for other string operations are valuable for text processing on, for example, networked word-processing stations. Also, the multiply and divide instructions are up to three times faster than the 8086's.

The functionality of the iAPX 186 is further extended by the operating system firmware of the 80130 chip. For example, the 80130 provides 35 operating-system primitive instructions and supports five new system data types. Internally, the 80130 firmware comprises two sections: an operating system unit and a control unit.

The former consists of a 16-K-byte control store, which houses the operating system kernel. The control unit contains an operating system timer, a delay timer, a baud-rate generator, and programmable interrupt logic. The 80130 is directly connected to the local bus of the 80186 processor, with address decoding, buffering, and bus-demultiplexing logic contained on chip.

It should be noted that the inclusion of the 80130 on the board does not limit the user to the iRMX operating system. For example, Digital Research's CPM-86 may be configured for operation on the 186/51 board.

Organized interruptions

The 186/51 board provides 13 vectored interrupt levels by means of its two programmable interrupt controllers—one working with the 80186 and one with the 80130. With the iRMX operating system in use, the 80186 interrupt controller acts as a slave to the 80130. It therefore services only internally generated interrupts from, for example, direct-memory-access channels.

The 80130 interrupt controller operates in the master mode and has eight prioritized inputs that can be programmed to be either voltage-edge– or voltage-level–sensitive. A selection of four priority processing modes aids the system integrator in minimizing delays in servicing interrupts.

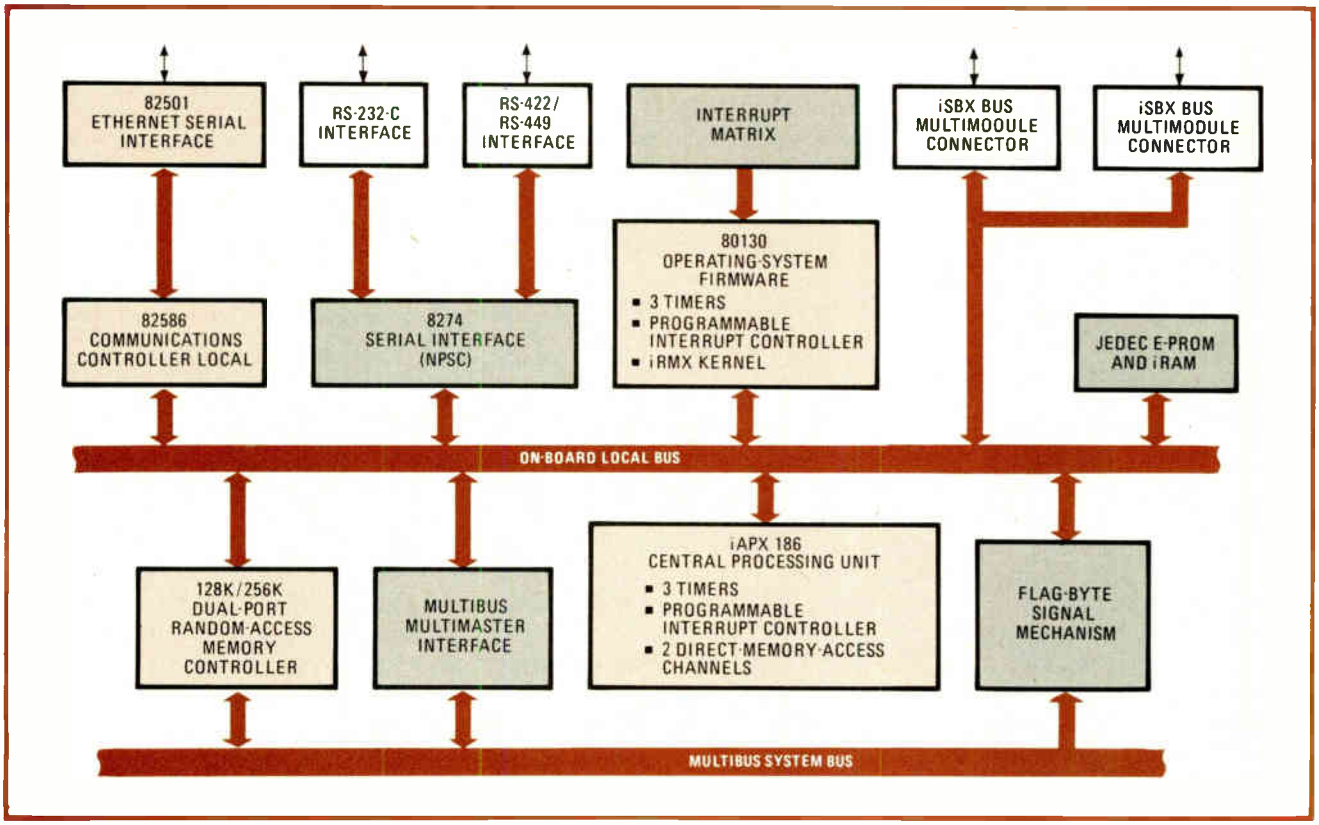
Interrupt operating modes and priority assignments may be reconfigured dynamically by software at any time. For example, the programmable interrupt controller accepts interrupt requests from all on-board I/O resources and from the Multibus. The interrupt controller then resolves requests according to the mode selected and, if appropriate, issues an interrupt to the CPU. In all, requests for the 186/51 interrupt service may originate from 25 different sources. All these interrupts are jumper-configurable with either suitcase or wrapped-wire techniques to the desired interrupt request level.

The 186/51 board has six programmable 16-bit timers—three on the 80186 chip and three on the 80130 chip. Of the timers internal to the 80186 chip, two are highly flexible and can be used to count and time external events or to generate nonrepetitive waveforms; the third is designed for real-time coding and time-delay applications and can also be used as a prescaler to the other two or as a DMA request source.

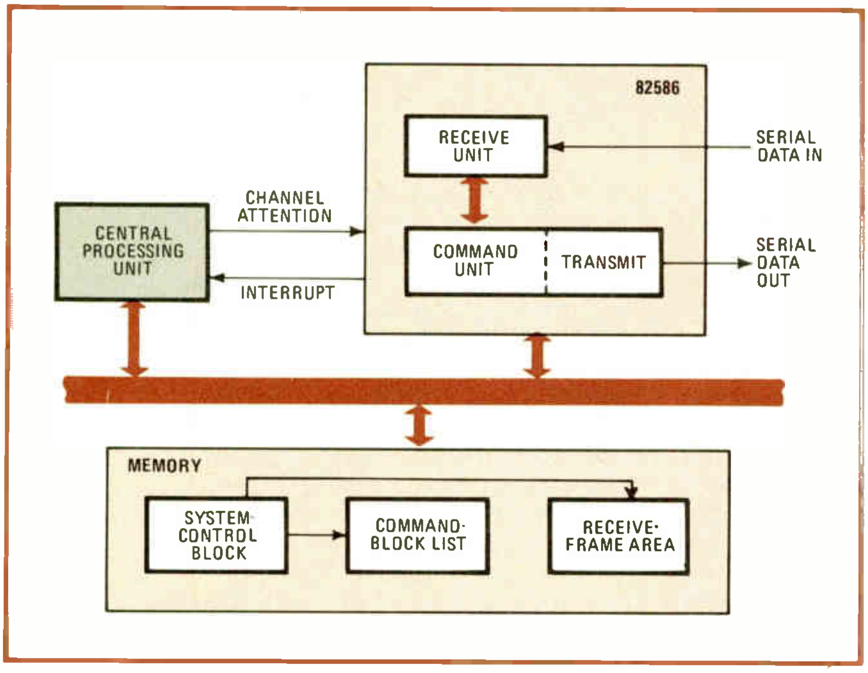
In contrast, the 80130's programmable timers have specific uses. One is a factory-set, default baud-rate generator and sends a square wave to the RS-232-C channel B, while the other two are assigned to the iRMX operating system and should not be altered by the user.

A windowing technique is used to make the 16-megabyte addressing range of the IEEE-796 Multibus standard available to the integrator of systems that are based on the 186/51 board. With this design, writing to an I/O-mapped port allows the user to map a 256-K-byte window in the 80186 microprocessor's memory space into any 256-K-byte block of the Multibus system.

Also, for multiprocessing systems, where communication among processors and synchronization of their activities must be arranged, an I/O-mapped flag-byte signal aids in creating an interprocessor-communication scheme. This scheme includes the ability both to set and



2. Count 'em. Playing together with the processors on the iSBC 186/51 board are a dual-port random-access memory, a local bus and a Multibus, timer and interrupt chips, multiple input/outputs, user-programmable chips, operating-system firmware, and collision-detection chips.



3. Two units. To the user, the 82586 chip appears as two independent, communicating parts: the command unit and the receive unit. The first executes commands from the iAPX 186, the second handles activities related to packet reception, address recognition, and cyclic redundancy checking, and both are run by a system control block (see Fig. 4).

reset interrupts with Multibus commands and to reset the board.

In the I/O section of the 186/51 board, the 82586 chip is a local-network coprocessor designed to relieve the iAPX 186 of many of the tasks associated with controlling a local network. Its memory-based architecture enables it and the iAPX 186 to communicate through a shared memory space (see Figs. 2 and 3).

The local-net coprocessor

The 82586 provides the functions normally associated with the data-link and physical-link layers of a local network (ISO layers 1 and 2). In particular, it performs framing (frame-boundary delineation, addressing, and bit-error detection), link management, and data modulation. The 82586 also provides a buffer management capability through specially designed memory structures (Fig. 4). It also supports a network management interface to aid in the operation and maintenance of the network.

All these 82586 features make it capable of highly autonomous operation, which, in turn, reduces processor overhead and increases board throughput. As a bonus, the 82586 automatically gathers statistics on cyclic redundancy check (CRC) errors, frame-alignment errors, overrun errors, and frames lost due to inadequate buffer memory. Finally, the user can output the status of all internal registers for examination and implement an internal loopback and on-chip time-domain reflectometer to help locate cable faults.

For its chores, the 82501 Ethernet serial interface chip (which is the companion of the 82586) sits between the 82586 and an Ethernet transceiver. It handles signal encoding and decoding, clock recovery, and signal-level conversions. The 82501 has the capability to retime badly distorted data before passing it to the controller. It also sports an internal loopback capability for board diagnostics, a watchdog timer to prevent channel hanging, and clock generation.

Two programmable communications interfaces using the Intel 8274 multiprotocol serial controller are on the 186/51 board. Also, two independent software-selectable baud-rate generators permit the user to operate the board's communications channels at all the common frequencies. The mode of operation (asynchronous, byte-synchronous, or bisynchronous), data format, control character format, parity, and baud rate are all under program control.

For its part in the board operation, the 8274 provides full-duplex double-buffered transmitting and receiving capability. It also handles parity, overrun, and framing-error detection. The 186/51 board supports operation in the polled, interrupt, and DMA-driven interfaces through jumper options. These options are set at the factory with channel A in the RS-422A/RS-449 configuration and channel B in RS-232-C, but they are user-alterable.

Another I/O option on the communications-computer board is two 8/16-bit iSBX Multimodule connectors, which support additional on-board I/O functions provided by VLSI peripheral components. These functions include parallel and serial I/O, analog I/O, and the control of small mass-storage devices, such as cassettes and floppy disks.

The iSBX connectors have all signals necessary to interface with the on-board bus, including 16 data lines for maximum data-transfer rates. Also supported by the 186/51 board are iSBC Multimodule boards designed with 8-bit data paths and using the 8-bit iSBX connector.

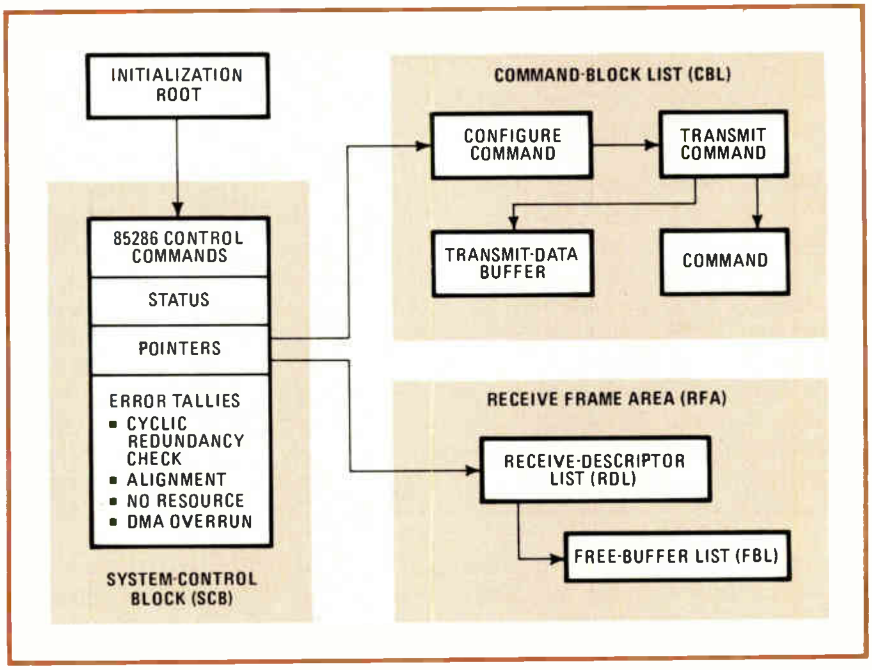
Memory's the trick

Because the iAPX 186 microprocessor and the 82586 local-network coprocessor communicate through memory-based structures, the memory section is a crucial part of the board. Both local and dual-ported memory are available.

The 128-K bytes of dual-port dynamic RAM may be expanded to 256-K bytes with the iSBC 304 Multimodule board mounted onto the iSBC 186/51 board. A dual-port controller allows access to this segment of on-board RAM (including RAM Multimodule options) from the 186/51 board and from any other Multibus master by way of the system bus.

This and other segments of on-board RAM may be configured as a private resource—that is, protected from Multibus system access. The amount of memory allocated as a private resource may be configured in increments of 25% of the total on-board memory ranging from 0%

4. Memory structures. Upon initialization, the 82586 local-net coprocessor gets the address of its system control block through the initialization root. The block contains control commands, status registers, pointers to the comand block list and receive frame area, and tallies for CRC, alignment, DMA overrun, and no-resource errors.



to 100%. An optional RAM Multimodule board doubles the increment size. This feature allows multiprocessor systems to establish local memory for each processor where the total system memory size (including local on-board memory) can exceed 1 megabyte without addressing conflicts.

The large amount of on-board memory allows network messages received or transmitted to accumulate without the need for a memory board. In addition, six 28-pin sockets are provided for the use of Intel's 2732, 2764, 27128, 27256 and their respective ROMs. When using the 27256s, the on-board E-PROM capacity is 192-K bytes. Other standard-pinout devices are supported, including byte-wide static RAMs and iRAMs. This feature allows the system integrator flexibility in configuring his local RAM and ROM resources.

All the hardware features that have been mentioned conform to industry standards. Thus, the board complies with the IEEE 796/Multibus specification, the IEEE 802.3/ECMA 80-82/Ethernet specifications, and the IEEE P959/iSBX specification. This commitment to standards eases the systems integrator's task as his interfaces are always well-defined.

Software galore

Because of its iAPX 186 microprocessor, the iSBC 186/51 communicating computer can take advantage of libraries of 8086-compatible software. So among the packages available to the 186/51 customer are operating systems, language processors, and application programs. The most important of these is the iRMX 86 real-time operating system. Included within iRMX 86 is a multitasking nucleus that handles scheduling, intertask communication, and memory management. Moreover, there is an I/O system that provides a hierarchical disk file system and a human interface.

As mentioned earlier, the iRMX 86 nucleus is present in silicon in the guise of the 80130 firmware. Not content with just implementing the iRMX 86 nucleus, the 80130 provides interrupt and timer facilities. As might be expected, the iRMX 86 on the 186/51 board is compatible with iRMX 86 on other 8086/88-based boards produced by Intel, making it easy to upgrade to the 186/51 from those boards. Also available on the 186/51 board is iMX 800 software, which permits interboard communications across the Multibus communicating computer bus.

In its role as a communications computer, the 186/51 exists in a distributed environment, communicating with other stations on a network. To accomplish this, Intel has developed the iNA 960 communications software. The first release of iNA 960 executes either under the iRMX 86 operating system or any 82586/80186-based component design. Future releases of the iNA 960 software will operate under additional operating systems.

The iNA 960 software provides capabilities at four different layers of the ISO reference model—the transport, network, data-link, and physical layers. It also provides network-management functions. For its part, the transport service supplies both virtual circuits and datagrams. The virtual-circuit service guarantees the reliability of the communications path between any two processes in the network; it utilizes the proposed ISO DP8073 draft transport standard. In contrast, the datagram provides a "best effort" service that offers users a basic process-to-process delivery service upon which many additional services can be built. The network layer initially provides access to a single IEEE standard 802.3 local network, with support for multiple local networks planned in future releases. The data-link and physical-layer service offered in the iNA 960 package complies with the IEEE 802.3 draft standard for such service and is straightforward.

The final part of the iNA 960 software package is the network-management capabilities, which are useful in initializing, operating, and maintaining a distributed computing network. For example, to assist in network operation, all iNA 960 software keeps operation statistics. that may be accessed on any node and therefore represent a fully distributed network-management facility. For support of network initialization, the iNA 960 provides a means of downloading software over a network for server or consumer. Under the iRMX 86 operating system users can access iNA 960 through either procedure calls or messages. For example, use of the message-based interfaces can yield a high degree of asynchronous operation.

The iNA software allows the user to configure any part of his software and access any ISO layer. In this way

Multiple data-transport standards

The transport protocol implemented by Intel shares its virtual-circuit orientation with various other protocols that ensure the reliable transport of data over a network. The most popular also provide services similar to Intel's.

The five best-known are the International Standards Organization's DP8073, on which Intel's protocol in fact is based; the European Computer Manufacturers Association's ECMA 72; the National Bureau of Standards' NBS transport; Xerox Corp.'s Xerox Network Services (XNS); and Arpanet's Transmission Control Protocol (TCP). The first three have only minor differences, which are even now being reconciled. The fourth was developed by Xerox as part of its office products activities and, though controlled by the company, has been widely distributed. TCP is the grandfather of the other four and the model for modern transport protocols.

TCP and all its "grandchildren," except XNS, allow for an expedited as well as a regular channel of data flow. The expedited service, of the kind provided also by the Intel transport software, enables important messages to bypass the regular mechanisms of data-flow control. The protocols use similar addressing conventions for the chore, though TCP's has the least flexible set of features.

The NBS and TCP transports also provide a "graceful close" mechanism. With this software and hardware procedure, users can ensure the delivery of all data sent prior to the closing of a virtual circuit. ISO, ECMA, and XNS make this the responsibility of the transport user.

user processes may utilize the transport virtual-circuit service concurrently with the data-link services.

The transport-layer protocol in the Intel implementation of the ISO DP8073 layer 4 standard provides what is called class 4 service. This service has four functions: reliability, multiplexing, control of data flow, and fragmentation/reassembly.

Layer 4's four functions

Reliability guarantees that user data is not lost, duplicated, or delivered out of sequence. Since most data links used in local networks do not guarantee delivery, such a service is needed for proper operation.

Multiplexing in ISO layer 4 provides process-to-process communication. In contrast, ISO's data-link and network layers—its layers 2 and 3—generally provide delivery only between nodes or physical boxes on a network. The ISO transport layer 4 builds on this node-to-node service by providing a process-to-process service—in short, it passes messages between processes and not just nodes.

Flow-control software exists to regulate the rate at which one process is allowed to send messages to another. It wastes network bandwidth and CPU cycles for one process to send another more messages than there are buffers available at the destination process. Flow control attempts to minimize this waste by setting a limit on the number of messages a given process may send to another—a limit based on a measure of the number of buffers free at the destination.

Fragmentation and reassembly free the user from having to limit messages to the size of data-link frames. Thus, a user can ask that 10,000 bytes be sent without having to worry (or know) that the maximum data link size is 1,500 bytes. Most transport software will fragment the message into a number of smaller packets and deliver them reliably to the destination where they are reassembled (see "Multiple data-transport standards," above).

The combined power of the iSBC 186/51 communicating computer product, and the iNA software open the door to a variety of applications that have not been as cost-effective as they can now be. Consider, for example, the kind of distributed data-collection system used in industrial process control. Such a distributed computer system would use several 186/51 boards for process-control stages connected to one another and to a monitoring station over Ethernet.

Each control station would consist of an 186/51, an iRMX 86 nucleus, iNA 960 communications software, and several Multimodule products. Two possible Multimodule options are the iSBX 311 analog input modules and the iSBX 350 parallel output module. With these multimodule boards, the iSBC 186/51 collects analog input (for example, temperature or flow rate) and controls the manufacturing process by means of digital output signals.

The application software executes under the iRMX 86 nucleus contained in the 80130 chip. Communication with the monitor node is handled by the iNA 960 software, which executes under the 80130 firmware. This control requires no local mass storage, nor does the application software have to reside in ROM.

The network-management service of the iNA 960 software can download application software from any node, although the monitor node is most likely. As a result, only the monitor node would require mass storage and therefore need a iSBC 215 disk-controller board in addition to the 186/51 board. All communication between the nodes would be fast and reliable and employ industry-standard protocols.

Another use for the 186/51 communicating computer board would be in a low-cost data-entry work station. Using much the same hardware and software as in the previous example, such a work station would have a 186/51 placed in a terminal enclosure together with an iSBX 270 video-display board to control its CRT display. It would also have a keyboard.

This station could be used by an operator to enter information about various transactions. Because of the low transmission delay of Ethernet, entire screens of data could be sent from a file-server node (also constructed using a 186/51) to the work station and back again within the response time of an operator. The iAPX 186 16-bit microprocessor would be capable of doing large amounts of processing at the work station before it returned the information to the file server. Such a system could also be used for program development. □

Structured-design system takes over the complexities in VLSI circuits

In an efficiently automated design method that produces dense custom chips, Cell Compilers optimize building blocks and Composition Editor assembles them

by Bob Duyn and Stephen Trimberger, *VLSI Technology Inc., San Jose, Calif.*

☐ Radically simplifying the task of fashioning complex, space-efficient very large-scale integrated circuits, a hierarchical computer-aided design system helps inexperienced users develop custom chips by shouldering many of the arcane tasks inherent in the process. In fact, the Logicomp VLSI design system operates much like a high-level programming language: the user works in familiar terms, and the system transforms his or her inputs into a fully developed chip.

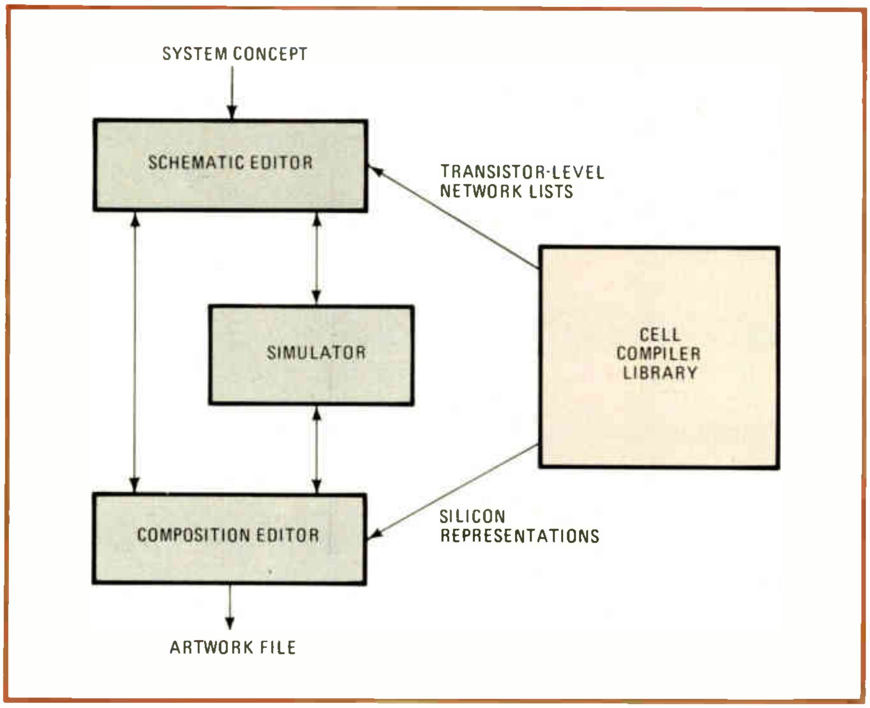
Until now, the growing flock of system designers bent on reaping the cost and performance rewards of custom ICs has had three options: gate arrays, standard cells, and fully customized chips. The first two methods attain a high level of automation, speed design times, and ask for little or no silicon savvy from the end user. But the fully customized approach generally requires the artistry of an IC expert. As a result, user-designed chips are sacrificing the flexibility, efficiency, and performance possible with the full-custom approach.

This new design methodology—termed structured custom—brings the benefits of fully custom ICs to system integrators demanding an easily learned and simply used tool for the rapid design of silicon. In the structured-custom approach, designers have ready access to Cell Compilers, common high-level building blocks absent from semicustom methods, such as arithmetic and logic units, memories, and programmable logic arrays. Furthermore, structured-custom chips need not sacrifice density or speed, resulting in more cost-effective ICs than gate arrays or standard cells can produce.

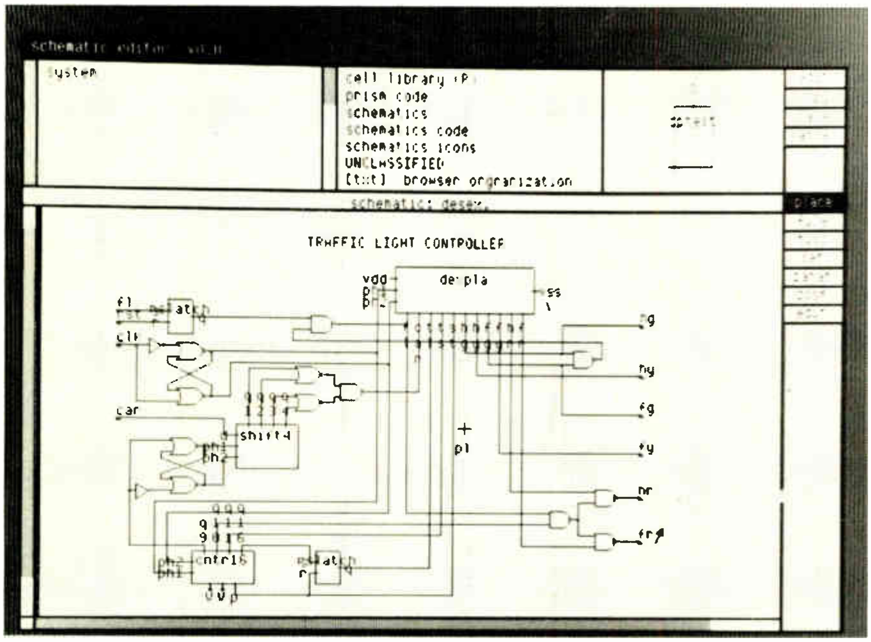
Silicon compiler technology is the heart of the Logicomp system, which implements the structured-custom approach. By hiding from the user the low-level details of IC mask geometry, Cell Compilers overcome the primary drawbacks of the traditional full-custom approach: long design times and unmanageable design complexity. Because the compilers are software routines assembling optimized circuit elements with user-specified parameters, they overcome the primary drawbacks of traditional standard-cell or gate-array approaches: limited flexibility and inefficient layouts.

With Cell Compilers and the other elements of the structured-custom approach, engineers familiar with board-level TTL designs can independently create custom logic chips in a matter of weeks. The design tools accommodate and encourage the hierarchical design style—keyed by well-defined interfaces between system modules—that is essential to managing complex designs. Once designed, low-cost prototype chips are available on multiproduct wafers, through which many users can share the costs of mask making and wafer processing.

The individual tools that constitute the compiler-based design system are shown in Fig. 1. A schematic editor provides a familiar interface for system designers and has access to the library of Cell Compilers. The compilers,



1. VLSI design. Four tools carry system designers from schematic entry through physical design of integrated circuits. All details of the silicon implementation are hidden from the user by the Cell Compilers that generate mask geometry from simple performance parameters.



2. Schema. A window on the schematic editor gives the means to place, name, interconnect, and manipulate graphical representations of the circuit elements. Cell Compilers automatically send block-level drawings of the functions they produce to the editor.

which consist of software procedures, generate particular logic functions optimized for specified performance characteristics. Once the wiring between these functional blocks is completed at the schematic level, the design is tried out with the simulator, which includes both logic and timing modes. The former is a unit-delay logic simulator, while the latter models delays due to the resistance and capacitance of devices and wiring.

In the next step, executing the physical design with the Composition Editor, the user merely positions the functional blocks that appear in the schematic. The design system then automatically extracts the interconnection pattern from the schematic and routes the appropriate wires. Another part of the Composition Editor, the compactor, squeezes this correctly wired layout into the minimum silicon area. The resulting rapid yet efficient design of a custom IC entirely frees system designers to concentrate on system-level design.

Each of these four basic tools dovetails with a flexible window system through which the user views and manipulates his or her design and its attributes. Any number of arbitrarily sized windows, each corresponding to a particular design task, can be opened and placed anywhere on the screen of the graphics terminal. Command menus pop up as needed; pointing to an instruction with a mouse-controlled cursor executes it. As a result, typing is virtually eliminated and the system itself guides the user through the design process.

The schematic editor captures a chip design in a manner analogous to the design of a board-level product—functional blocks defined by the system or the user are placed, named, connected together, and manipulated as required (Fig. 2). The hierarchical approach accommodates high-level blocks called out by the user and implemented later in terms of specific logic functions.

An entire design can be drawn using the Cell Compilers that are supplied in the system. When a compiler is called, the schematic editor automatically generates a unique graphical representation of the particular function generated, complete with input/output signals and electrical characteristics. Compiled blocks and those defined by the user can be combined as desired in a hierarchy of any depth.

Two compiler libraries are available: a primary collection of the elementary circuit functions and an extended library of more complex blocks. The former comprises the various I/O buffers, latches and flip-flops, and Boolean logic functions that make up any IC. The primary library also includes what are called foundry artifacts, which the chip maker needs to use in setting up the fabrication of a chip—the scribe channel, alignment and resolution marks, and so on.

The extended library supplies the commonly used functions of higher complexity: counters, adders and subtracters, multiplexers, shift registers, programmable logic arrays, read-only and random-access memories, and ALUs. In addition, a pad-ring generator makes quick work of bonding-pad placement and routing.

All of the compilers are similar in comprising software routines that automatically generate silicon representations of specific functions, with characteristics selected by the user. The compilers are written in VIP (VLSI implementation program), which is based on the Mainsail language of Xidak Inc. Despite their internal complexities, they appear to the user as simple circuit-function generators. All the details of the software implementation, as well as the details of the generated silicon, are completely hidden from the user (Fig. 3).

Compiling silicon

Selecting a particular compiler from the library menu causes the system to prompt the user for values of the parameters that can be varied in that cell. In a simple cell, such as a NAND gate, the user selects the number of inputs, the orientation of the inputs and outputs, and one of several speed grades (achieved by the system by varying transistor sizes within the cell). More complex functions are specified in straightforward ways, such as the number of bits in a counter or ALU, and shift direction and clocking order in a shift register.

Using the parameters passed by the user, the compiler generates the detailed silicon representation in the Caltech Intermediate Form, a language for describing the geometrical primitives of an IC layout. However, the user need never see this detailed information. Instead, the compilers return symbolic representations like blocks and gates to the schematic editor and automatically provide the transistor network lists needed by the simulators. This ability to represent configurable, complex structures holds distinct advantages among chip-design methodologies. Gate-array approaches can create complex structures only by stringing together simpler building blocks, resulting in a less efficient design. A subtle benefit of the compiler's ability to generate many different versions of a single generic function is that many fewer cells are needed to accommodate all the functions needed by designers and that the management of the library data is correspondingly simplified. In effect, several hundreds of fixed-height fixed-function standard cells can be replaced by a few tens of Cell Compilers.

Easy technology updates

Furthermore, process-technology improvements are transparent to the compilers. Within a given process—such as complementary-MOS or the high-performance MOS process, H-MOS—the compilers automatically incorporate geometrical shrinks and associated design-rule changes, protecting the user's investment in the design software. This orderly progress is achieved within the system by limiting all process-specific data to a single technology file that can be accessed by the compilers, editors, and simulators.

The Cell Compilers thus handle all of the lowest-level silicon design tasks. However, completing a chip's physical design also requires the capabilities of the Composition Editor. This tool reduces full-custom IC design to a task of mere interconnection of silicon building blocks.

Having completed a schematic design of the chip, the designer uses the Composition Editor to place outlines of the actual physical cells manually. Based on the connectivity that is already specified in the schematic, the Composition Editor routes wires among the cells and then adjusts the placement of cells and wires to achieve the smallest possible chip area, given the constraints of the design rules (Fig. 4).

Like an automatic router for a printed-circuit board, the Composition Editor frees the engineer to concentrate on electrical connections between functions, rather than geometrical connections on layouts. It supports a bottom-up hierarchical implementation, in which the lowest-level cells are first placed and routed to complete a larger functional block that is then placed and interconnected with other higher-level blocks. This process continues until the chip design is complete.

At any point, manual routing is also permitted, letting the designer retain control over the routing of critical signals. Furthermore, at the user's discretion, the compactor will enter a previously completed level of the hierarchy and recompact lower-level cells in the context in which they have been placed.

Through this iterative and hierarchical process, users with no IC design experience can quickly achieve efficient custom designs using familiar building blocks. The tools are at least as easy to learn and simple to use as those for gate-array or standard-cell design and result in less-costly, higher-performance chips. More specifically, compiled cells—including complex functions—are only 10% to 20% larger than cells obtained by traditional hand-crafting methods. Compaction by the Composition Editor produces layouts only about 10% larger than can be achieved by hand.

The fundamental operations of the Composition Editor are the interconnection and compaction of cell layouts. As mentioned, the initial relative placement of cells is performed by the user. Following routing, the compactor repositions cells and wires to minimize IC area. Both routing and compaction software exploit graph theory in executing the necessary computations.

Inside the Composition Editor

The router proceeds in two steps, global and then local. The global router first locates the open areas of the layout, where no cells have been placed, and sections these areas into rectangles. The necessary interconnections are extracted from the schematic drawing, and the router determines through which rectangles and in what order each wire must travel. That determination is made by constructing a graph in which the nodes represent the edges of the rectangles and the branches correspond to the routing areas themselves.

The global operations thus reduce the problem to a set of routing areas, or rectangles, each with a list of wires that must be routed through its interior. The local router then determines an ordering of the wires along the rectangle's edges and completes the connections. Two levels of wiring are available—in an H-MOS process they correspond to polysilicon and one metal layer. To take advantage of the metal's lower resistance, connections are completed in metal wherever possible. Because the router works with symbolic representations of wires and contacts and not with actual geometry, all designs can be

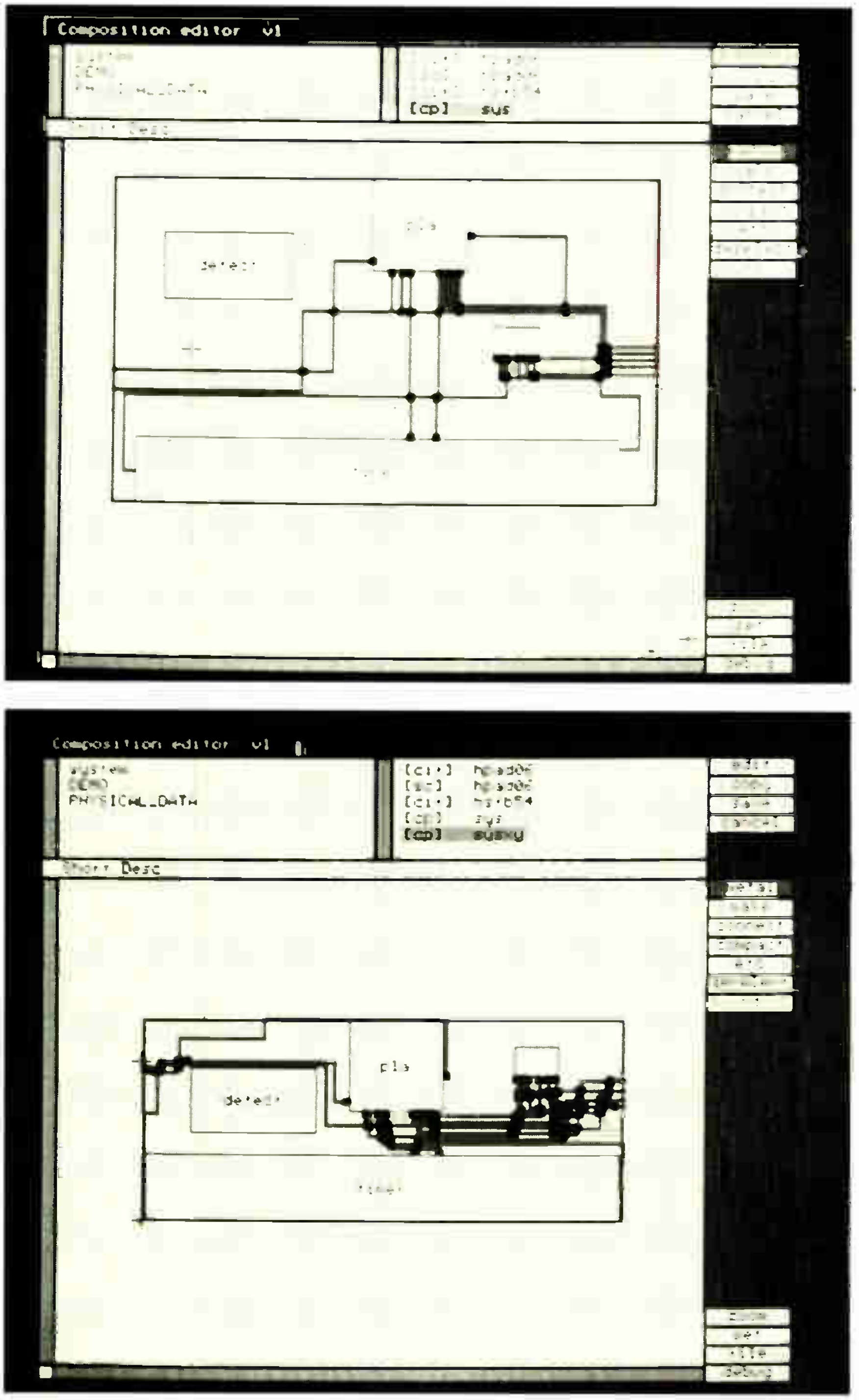
H BUF 11
1 pF Drive
2 pF Drive
3 pF Drive
4 pF Drive
5 pF Drive

(a)

```
libraryCell ("hbufi1", (long real vssw, vddw,
      aWidth, bWidth, cWidth, dWidth));
      ⋮
libval ("11_C_drive_width", cWidth);
libval ("11_D_pulldown_width", dWidth);
      ⋮
draw ("pushpull", "hpshpl:hpshpl", rightof ("inverter"),
      parameters (vssw, vddw, cWidth, dWidth, endargs));
      ⋮
enddef;
endof;
```

(b)

3. Compiled cells. Using a Cell Compiler requires responding to the system's prompts on the parameters that can be changed, such as the load capacitance a buffer must drive (a). The compiler consists of a software routine (b) that generates the necessary mask geometry.



4. Compactor. After the user places the cell outlines, such as "pla," the Composition Editor completes a symbolic wiring pattern (a) that corresponds to the schematic drawing. A compaction program then compresses the layout in two steps (b).

completely routed. In addition, the router can be modified easily for a double-metal process.

Once routing is completed, the compactor proceeds in two steps to minimize the area of the circuit, first in the vertical direction and then in the horizontal. To compress the vertical dimension, the program constructs a graph in which the nodes represent horizontal lines, contacts, and cells, and the branches correspond to the minimum spacings required between adjacent nodes. The longest path in the completed graph then gives the final vertical dimension, and the circuit elements are repositioned accordingly. The same procedure is then performed in the horizontal direction, with nodes corresponding to vertical wires, contacts, and cells.

The simulator is a software version of the system engineer's logic analyzer, incorporating both functional and performance verification. This transistor-level simulator operates on both schematic- and physical-design data, using any symbolic names attached to the circuit elements. As a result, users can debug high-level designs symbolically; that is, ignoring lower-level implementation details and thus speeding the process.

Design simulations are based on input data entered through the keyboard or from user-written programs. The output from the simulator can be displayed graphically as logic waveforms or as numbers. At the schematic stage of design, circuit elements are simulated on the basis of default characteristics supplied by the schematic editor or by the user. Once a physical design has been generated by the Composition Editor, the simulator operates on an extracted-transistor–level representation that includes all the interconnection and stray capacitance that will be present in the fabricated chip.

In order to perform useful circuit-level simulations in a reasonable time, transistors are modeled simply as dynamic resistances. This simplification over a full simulator such as Spice sacrifices some precision—the simulator's results differ from Spice calculations by as much as 20%. However, it is guaranteed to perform worst-case analyses; that is, to err by overestimating delays. As a result, circuits that perform adequately under simulation will perform as well or better in silicon.

For functional, as opposed to performance, verification, the simulator can be operated as a nine-state unit-delay logic simulator. The same command structure and instruction set are used in both modes. Functional verification typically is relied upon at the schematic stage, where quick inspection of trial circuits with user-settable breakpoints gives immediate feedback on design progress. Performance verification can be done throughout the process, although the most accurate results are not available until the physical design is completed. □

Minimizing emi at minimal cost in computing equipment

Complying with the new FCC rules on electromagnetic interference requires proper grounding, bypassing, and shielding procedures

by Glen Dash, *Dash, Straus & Goodhue Inc., Boxborough, Mass*

□ By October, almost every computer maker in the country must comply with the FCC's new rules on electromagnetic interference (emi). Compliance can be simple, straightforward, and relatively cheap. Yet many engineers seem to think that emi suppression calls for black magic, not technology, and many manufacturers report that they had difficulty meeting the emi specifications.

The Federal Communications Commission regulations divide computer interference into two classes: radiated emissions (specifically, the signal that equipment transmits into space between 30 and 1,000 megahertz) and line-conducted emissions (the signal fed back into the power lines between 0.45 and 30 MHz). The specification that covers radiated emissions is by far the more difficult of the two to meet.

The source

Current transients that are produced when logic chips change state are the basic source of these radiated emissions. The transients appear on the supply lines, or rails. In sophisticated hardware, synchronous gates can produce current pulses of several amperes on the supply rails. The resulting radiated emissions can be predicted if each gate is represented as an rf current source pulsing its signal into the supply rails. Limited IC rise times concentrate most of the energy below 300 MHz.

Figure 1a shows how these currents, building up on the supply lines, produce radiated interference. The figure's TTL buffer is used in a 10-MHz clock. Supply current I_s changes at a 10-MHz rate (see Fig. 1b). Relative to chassis ground, logic "ground" at point V_g has an associated voltage equal to I_s times the trace impedance of the ground return, which, to a first approximation, is an inductor. In this example, the power supply, bolted to a large metal plate, is at earth ground.

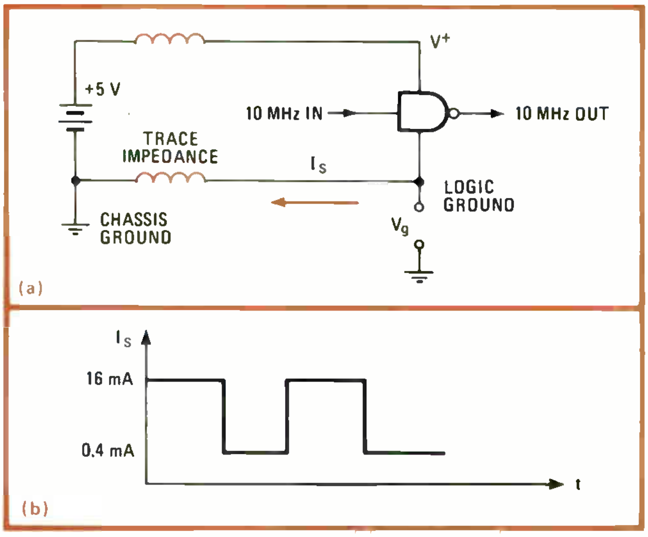
The amplitude of the ground noise, V_g, can be calculated if the trace impedance created by printed-circuit-board runs is known. The inductance, 20 or so nanohenries per inch, corresponds to an impedance of 1.25 ohms/in. at 10 MHz and 6.25 Ω/in. at 50 MHz.

The 10-MHz square wave of Fig. 1b is made up of sine waves at every odd harmonic of 10 MHz. A Fourier series expansion of the 10-MHz square wave shows that at its fifth harmonic, the amplitude of the gate's ground current is about 2 milliamperes, zero to peak. If the ground return in Fig. 1a is 4 in. long, the voltage at point V_g will be about 50 mV (zero to peak) at 50 MHz. The amount of radiation that will result depends on which kind of antenna is attached.

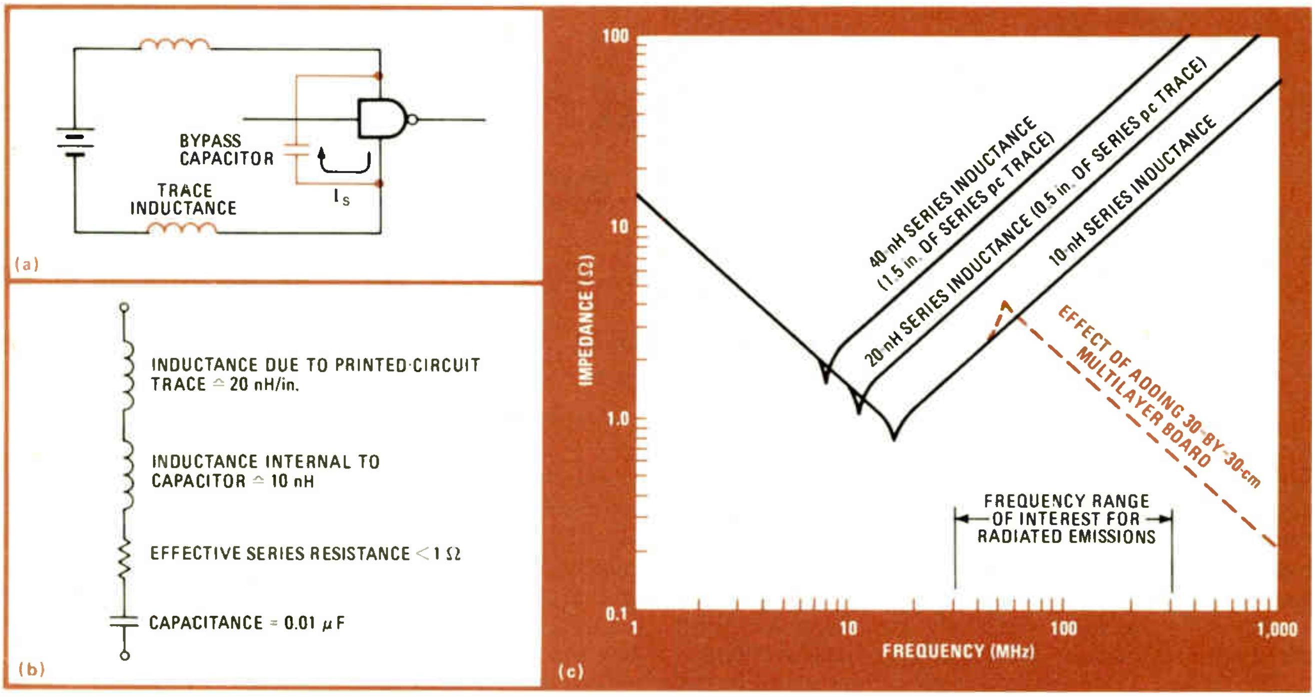
Four inches of pc trace do not make an effective radiating antenna. But the clock driver's ground pin excites the pc board's whole ground system. This common-mode noise appears on all points, including the I/O cables, whose ground return is often tied to logic ground. Any wire connected to logic ground will radiate. The radiation is a function of the common-mode noise and the attached wire's length and orientation.

Even shielded cables radiate when the shield is attached to a noisy logic ground. If the shield on the shielded cable is slightly more than 1.5 meters long (a quarter wavelength at 50 MHz), and if it and V_g are tied together, the resulting radiation (at a distance of 3 meters) can be as high as 3,000 microvolts per meter, 10 times the FCC's class A radiated limit—and this for one gate only.

Fortunately, capacitive bypassing, the shielding effect of the metal cabinets, and the finite rise times of digital ICs combine to reduce the radiation from most comput-



1. Logic ground. The sink current of a TTL buffer produces supply return current, Is. Common-mode noise, V_g, is the product of this current and the ground return impedance. The voltage is a square wave whose odd harmonics complicate emi suppression.



2. Bypassed. Bypassing (a) effectively reduces supply impedances. The inductance of the capacitor and the printed wiring (b) is capable of causing a 0.01-microfarad capacitor to exhibit high impedances at frequencies of interest (c).

ers. In fact, most devices—even those designed in total ignorance of FCC rules—are no more than 20 dB over the radiation limit. All the same, this common-mode noise is the chief cause of computer and peripheral radiated emissions.

Designers have three choices for reducing them. One is to lay out the pc board to cut the supply-line impedance, preferably to a value below 10 Ω at 100 MHz. Proper use of bypassing, multilayer boards, or bus bars can help. If good layout does not achieve compliance by shielding or filtering the "antennas," the cabling attached to the pc board or back plane may have to be shielded, too. In some cases, even the pc board and the internal wiring may have to be shielded.

Proper layout

Bypassing each IC is the simplest way to cut supply-rail impedance. Ideally, each bypass capacitor acts as an rf short circuit, preventing the current pulses from passing to the rest of the circuitry (Fig. 2a). Unfortunately, bypass capacitors often approach the limit of their usefulnesss just when help is most needed—in the region from 30 to 300 MHz.

The equivalent circuit of a bypass is an ideal capacitor in series with other elements (Fig. 2b). The most significant of these is the 20-nH/in. inductance caused by the length of the pc trace between the IC and the bypass capacitor. Figure 2c shows how a bypass capacitor can quickly become ineffective when even a small trace separates it from the IC.

For many applications, bypassing alone may satisfy the emi limit. In more complex applications, series inductance may demand other solutions—for instance, multilayer boards, whose buried ground and voltage planes have little or no trace inductance.

Pc traces on conventional two-sided pc boards have significant inductance because they are longer than they are wide. The width of a multilayer board's ground (or voltage) plane just about equals its length, and its impedance is limited only by the material's skin resistance, usually on the order of a few milliohms per square. On a typical multilayer board, the impedance of a 10-by-10-in. buried ground plane is about 10 mΩ.

The buried supply and ground layers of a multilayer board therefore offer a low impedance to each IC. Furthermore, at the frequencies of interest these two layers act as a feedthrough capacitor for the current going to each IC. Figure 2c shows the impedance of a multilayer board seen from the supply pins of a gate.

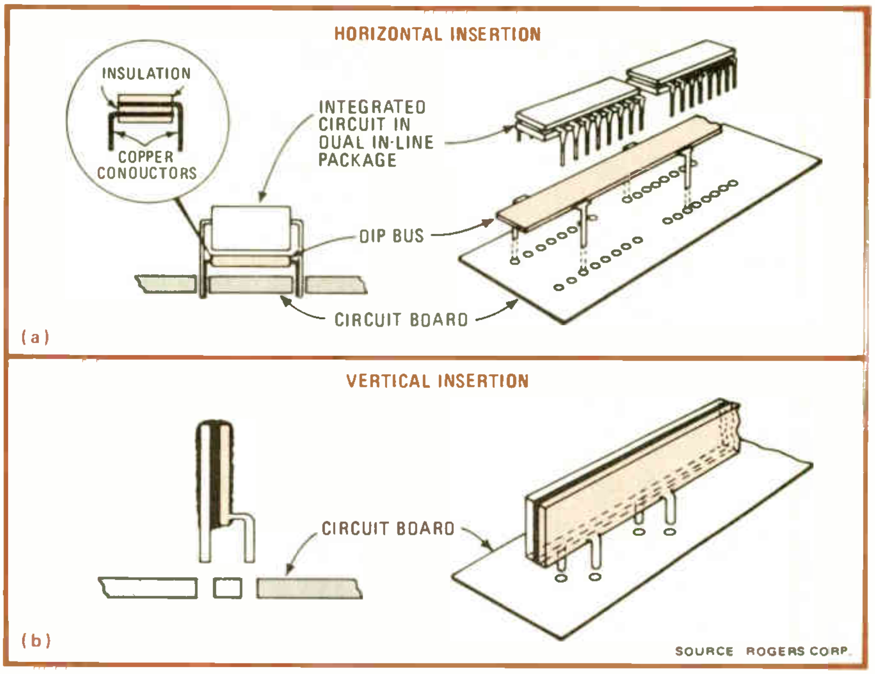
Yet another way of getting low supply-rail impedance is to have bus bars feed supply and ground to each IC (Fig. 3). The bus bars, acting as small multilayer boards, offer a feedthrough capacitance that helps cut power-supply line impedances effectively, though less effectively than multilayer boards do.

Cutting cable emi

Good pc layout can often bring a system into emi compliance. But when cables are attached to I/O ports, most devices generate enough common-mode noise to exceed FCC limits. And the FCC usually does require manufacturers to attach cables to units under test.

When a circuit's supply rails exhibit common-mode noise, so does every output of every gate. This noise signal, fed to the attached output cable, causes it to radiate like a long wire antenna.

Shielded cables are among the simplest ways of preventing radiation from I/O cables, but for full effectiveness the shields must be properly grounded. It is poor cable grounding that makes many engineers feel that emi



3. Bus bars. Supply-line impedances can also be reduced with a power distribution bus bar(a and b). This distributed network has low characteristic impedance and low inductance, which make it effective for suppressing high-frequency supply-line noise.

suppression trenches on black magic.

In some applications, a cable shield will not work because it is attached to the wrong point, such as a logic ground rather than the chassis. In other applications, the shield fails because the cable's boot—the portion that connects it to the chassis—is poorly designed. In Fig. 4a, for example, a computer housed in chassis 1 is connected through a shielded cable to chassis 2. The cable is bonded direct to chassis 2 but connected to chassis 1 through a drain or pigtail wire, a common though poor design that shields little if at all (Fig. 4b).

Every cable has a certain characteristic impedance—typically, between 50 and 300 Ω. Impedance (Z_1 in Fig. 4b) can vary as a function of the load at the cable's far end, but most data cables are lossy at rf, so they approach the characteristic impedance regardless of load.

The drain wire has impedance, too—for a short wire, a surprisingly high one in fact, about 12.5 Ω/in. at 100 MHz. The equivalent cable circuit can be modeled as a voltage divider. If the shield-to-ground wire measures 4 in., its impedance will be 50 Ω at 100 MHz. If the cable has the same impedance, approximately half the rf potential on its center conductor will appear on the outside shield, which then radiates like a long wire antenna even though the other end of the cable has been grounded.

The simple solution is a low-impedance connection created by linking the shield to the chassis with a continuous 360° metal boot instead of a drain wire. The quality of the shield, not the quality of the boot, will then determine the cable's effectiveness.

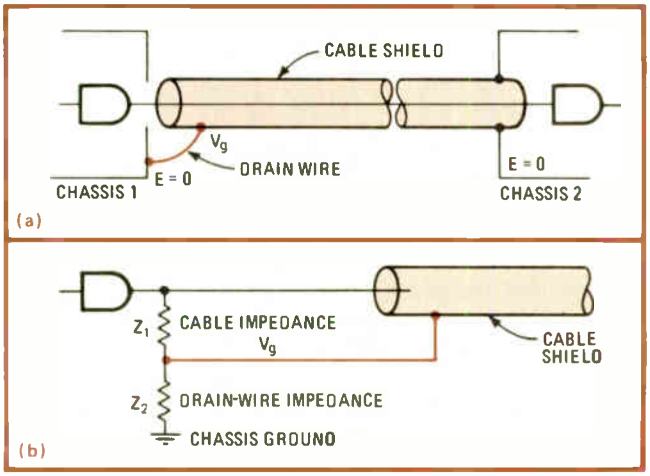
Shielded cables can also go bad if the shield is attached to the wrong ground. Newcomers to emi learn that "ground is not ground the world around"; even the finest shield radiates when connected to a noisy one. The moral is to pick the ground well.

True ground

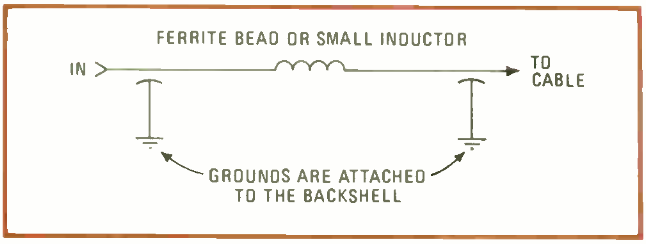
If a device under test should be housed in a metal chassis, that chassis is probably the closest point to earth ground. Grounds on most pc boards are poor, so cable shields should not be connected to them. Shielded cables are impractical in many applications because the proximity, number, or type of connectors frustrates good shielding. Another approach is in order—for instance, filtered connectors (Fig. 5), which can produce 30 dB or more suppression, without shielded cables.

These connectors, designed to replace standard chassis or pc-mounted connectors, have built-in pi-type filters whose component values were chosen to roll off high-frequency components but to leave lower-frequency data relatively unaffected.

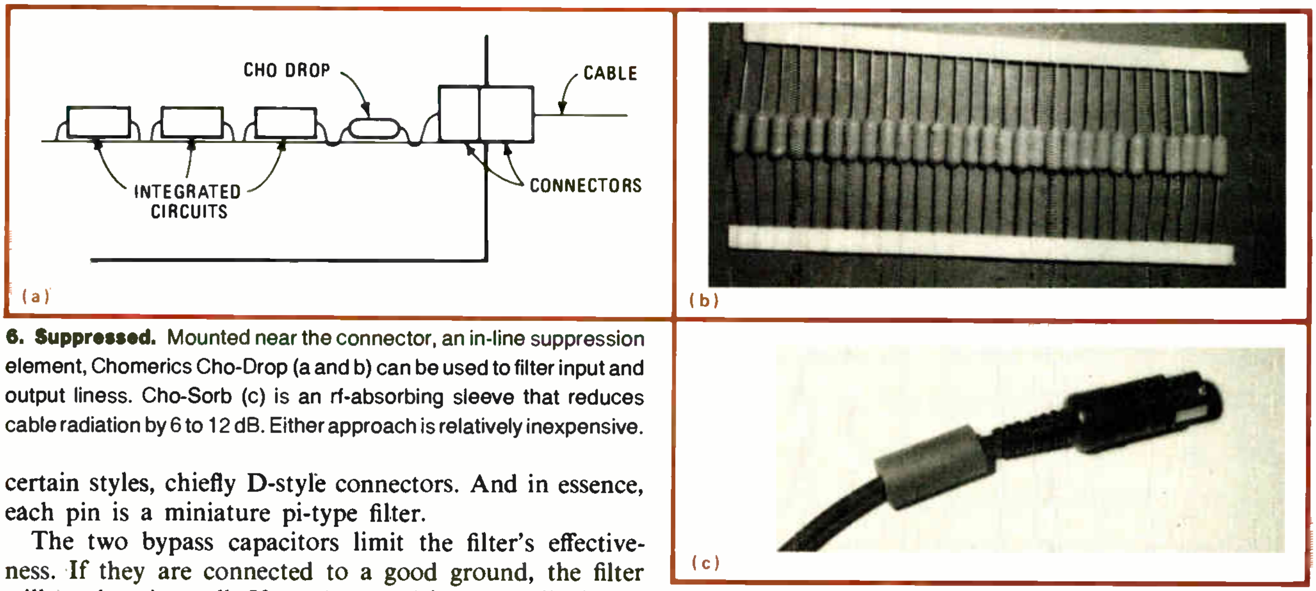
Filter connectors do have drawbacks, though. At $0.50 to $1.50 a pin, they are expensive. They come only in



4. Poorly booted. Poor cable-boot designs like (a) can cause high-impedance connections between the cable shield and the chassis. The result is a voltage divider action (b) that can cause much of the rf noise to appear on the outside shield.



5. Filtered. Filter connectors provide a way of filtering rf noise from input/output cables. Typically, they filter each pin separately, using a pi-type filter. To work effectively, the metal outside shell of a connector must be attached to a noise-free ground.



6. Suppressed. Mounted near the connector, an in-line suppression element, Chomerics Cho-Drop (a and b) can be used to filter input and output liness. Cho-Sorb (c) is an rf-absorbing sleeve that reduces cable radiation by 6 to 12 dB. Either approach is relatively inexpensive.

certain styles, chiefly D-style connectors. And in essence, each pin is a miniature pi-type filter.

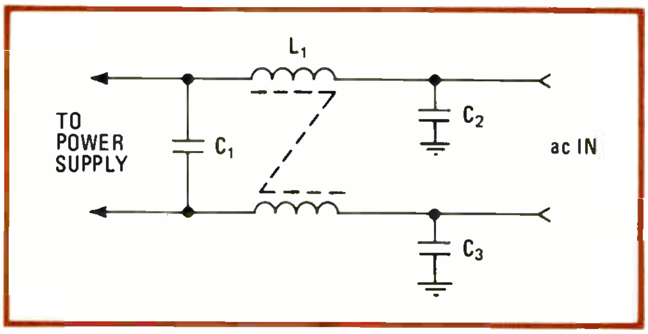
The two bypass capacitors limit the filter's effectiveness. If they are connected to a good ground, the filter will work quite well. If good ground is not available the filter will work poorly or not at all—as usually happens when the connectors are mounted on dense pc boards.

Other, less expensive methods, which do not require a good grounding system, can be used to achieve FCC compliance, however. Two products developed by Chomerics seem to have possibilities (Fig. 6). Cho-Drops, at about 25¢ to 50¢ a pin, is an axial device that can be inserted in series with each connector pin to be filtered. They are made of an rf-absorbant material that can suppress emissions from the filtered lead by about 15 to 20 dB but does not affect low-frequency signals. Most important, Cho-Drops, unlike filter connectors, does not depend on internal bypass capacitors and therefore does not require a good grounding system.

The other Chomerics' product, Cho-Sorb, a ferroceramic sleeve designed to fit over a whole cable assembly, works rather like Cho-Drops. For only a few cents a pin, these sleeves can reduce radiation off a shielded or unshielded cable by about 6 to 12 dB. Since they have an effect only at rf, the data on cable should not be affected.

These means often suffice for FCC compliance. But in more complex systems, radiation from boards and internal wiring systems can exceed FCC limits. These systems need cabinet shielding.

Metal cabinets can provide most of the shielding, so long as the cabinet seams are joined together electrically at enough points to create a shield. For computers that usually do not exceed the FCC limits by more than 20 to 30 dB, contacts every 6 to 8 in. will do the job.



7. Main line. Power rectifiers and switching power supplies can put rf noise into ac power lines. An ac line filter can eliminate the noise. In the unit shown, capacitor C_1 filters out differential noise, while the other passive components filter out common-mode noise.

Since plastic allows electromagnetic waves to pass unimpeded, plastic enclosures are harder to shield. The best way of doing so is to cover their insides with a conductive material, like vacuum metalization, arc sprays, and conductive paints. Nickel-acrylic–based paints, with 1-to-2-Ω/square conductivity, suffice for most applications.

Line-conducted emissions have two sources. Above 10 MHz, radiated emissions from the system under test (or the cables attached to it) couple on to the power line, which acts as a receiving antenna. The techniques discussed so far can eliminate these emissions but not those generated by noise from switching power supplies or rectifier diodes.

Rectifier noise comes from rectifier diodes that do not turn off quickly enough during zero crossings of the ac input. Switching supply noise shows up as harmonics of the switching frequency. For large supplies, the amplitude can be quite high. By and large, computers that use switching supplies need line filters, most of which comprise three capacitors and one two-winding inductor, as seen in Fig. 7.

The line-to-line capacitor, typically a 0.01- to 0.47-μF value, cancels out differential noise by shorting the two sides of the line at high frequencies. Bypassing each side, two other capacitors (together with the inductors) filter out common-mode signals. Leakage specs limit the size of these capacitors to between 0.001 and 0.01 μF, so they are not large enough to filter out most common-mode noise signals, especially those from switching power supplies.

That job calls for a series inductor, which generally ranges from 1 millihenry to 7 mH. The bifilar-wound series inductor can operate only on common-mode signals, ignoring differential currents passing through the inductor and therefore avoiding saturation. So the inductor limits common-mode noise but avoids saturation by the 60-cycle current. □

256-K dynamic RAM is more than just an upgrade

Silicides, lightly doped drain structures are being tuned for mass production of a next-generation part that improves on the 64-K workhorse

by Michael C. Smayling and Mike Maekawa, *Texas Instruments Inc., Houston, Texas*

☐ The 256-K dynamic RAM heralds the coming of a new generation of high-volume MOS processing technology. Better photolithography, for instance, will pack four times the capacity of a 64-K dynamic random-access-memory chip into less than two times the silicon area. As a result, the 256-K chip will fit into the familiar 16-pin dual in-line package.

The 256-K dynamic RAM must equal or better the performance of its 64-K progenitor. To achieve this, its device features must be scaled down (see table below). As in past generations of dynamic RAMs, the scaled-down processes that improve circuit performance will make stringent demands on processing technology.

The process for fabricating such high-density devices must be cost-effective yet ensure reliability. It must contend against an undergrowth of interrelated problems—including soft (or transient) errors, electrical noise, interconnection resistance, short-channel effects, pattern definition, and yield. The 256-K dynamic RAM will attract few users if high error rates and low voltage margins accompany the advance in capacity.

Chip manufacturers are especially intent on achieving soft-error immunity through both process and circuit design. Soft errors derive from a number of sources—stray radiation being the most worrisome. Alpha particles from trace contaminants in IC packaging materials and cosmic rays can generate millions of electron-hole pairs in the silicon substrate, discharging the storage-cell capacitors, the bit lines, or the sensing nodes in the sense amplifiers.

Errors induced by alpha particles are related almost exclusively to the amount of stored charge. Pattern-related errors also occur but, in contrast, are caused by leakage currents between adjacent bits or by capacitive coupling between bit lines or peripheral-circuit signals. Most of these internal coupling problems can be eliminated with a substrate bias generator, a high-resistivity epitaxial layer on a low-resistivity substrate, and careful circuit design and layout.

How well does the 256-K chip deal with the soft-error problem? Consider the dynamic-RAM storage cell. Three generations of dynamic RAMs have been based on a one-transistor storage cell whose active device accesses charge stored on a thin-oxide MOS capacitor. The transistor transfers stored charge to a bit line, which in turn connects to a differential amplifier for sensing.

If not for alpha particles, the storage capacitor would only need enough charge to ensure that data did not leak away between successive refresh operations (at 4-millisecond intervals). To prevent the loss of data from alpha-particle strikes, the number of stored charges must exceed the number of electron-hole pairs generated by a strike.

A capacitor of 50 femtofarads charged to 5 volts holds 250 femtocoulombs, corresponding to some 1.5 million electrons, roughly the minimum signal that can withstand an alpha-particle hit. To maintain a capacitance of 50 fF in the scaled-down area of a 256-K dynamic RAM's cell, the gate oxide is thinned to about 200 angstroms.

Some manufacturers propose to increase the stored charge by using insulators with a dielectric constant higher than that of silicon dioxide, universal in today's dynamic RAMs. Silicon nitride stores about 50% more charge than a comparable area of silicon dioxide, and sandwiching the nitride between oxide layers makes it easier to incorporate into existing processes. Tantalum pentoxide, with more than five times silicon dioxide's permitivity, has been considered, too. However, most firms do not yet regard the new technologies as cost-effective.

Higher cell capacitance also increases the signal at the sense amplifiers, speeding their response and alleviating the problem of imbalance, or offset. Through voltage division, the signal to the sense amplifier depends on the

COMPARISON OF TYPICAL 16-K, 64-K, AND 256-K DYNAMIC-RANDOM-ACCESS-MEMORY TECHNOLOGIES

Feature	16-K	64-K	256-K
Channel length (μm)	6 – 7	2.5 – 3	1.5 – 2.5
Gate oxide thickness (Å)	900 – 1,000	400 – 500	200 – 300
Junction depth (μm)	1 – 1.2	0.4 – 0.5	0.25 – 0.35
Area per bit (μm^2)	450	170	30 – 50
Bit-line composition	n^+ diffusion	n^+ diffusion	aluminum
Word-line composition	aluminum	aluminum	refractory metal or polysilicon/silicide

COMPARISON OF DYNAMIC-RAM INTERCONNECTION MATERIALS		
Material	Sheet resistance (Ω/sq for 2,500-Å film)	Step coverage
Polysilicon	10	excellent
Refractory metals	~ 0.3	poor
Silicides molybdenum tungsten tantalum titanium	 2.5 – 3.5 2.5 – 3.5 2 1	fair
Polycides	same as for corresponding silicides	excellent

ratio of bit-line to cell capacitance. For the 256-K dynamic RAM, a typical ratio might be 10 : 1. Under worst-case conditions, the resulting signal for sensing is often less than 100 millivolts.

A change in bit lines

On 16-K and 64-K dynamic RAMs, open diffused bit lines not only constitute a large capacitance but also form easy targets for alpha particles. To avoid these problems, the 256-K RAM's bit lines are folded to cut noise and are built in metal, rather than diffusion, in order to reduce capacitance and to increase sense signals. The folded layout, which connects adjacent bit lines to the differential sense amplifier's inputs, ensures that noise coupled locally to the bit lines forms a common-mode input to the amplifier and is rejected.

The 256-K's metal bit lines significantly affect the overall wiring strategy because low-resistivity layers are needed for bit and word lines to help the chip achieve access times below 100 nanoseconds. With diffused bit lines, aluminum served for the word lines, contacting the polysilicon gates of the access transistors. But with the only aluminum level devoted to bit lines, the choice for word lines (see table above) comes down to polysilicon, refractory metals, silicides, or polycides (polysilicon-silicide composites).

High sheet resistance eliminates polysilicon from consideration. Simulations indicate that polysilicon word-line delay increases access times by 20 to 30 ns—clearly intolerable in a high-performance part. Refractory metals occupy the other end of the resistance spectrum, but better deposition techniques and some form of protective layer will be needed to make them usable in the second wiring level.

Both silicides and polycides stand up well during the processing that follows their deposition. They can be treated much like polysilicon. Many manufacturers of 256-K dynamic RAMs have chosen polycides because they combine the best features of polysilicon and silicides; in fact, the first step in forming a polycide is to deposit polysilicon, so its excellent conformal step coverage and transistor-gate characteristics are retained.

For polysilicon thicknesses greater than 1,500 Å, the silicide has only a negligible effect on the transistor threshold voltage. In thinner layers, a threshold shift—caused by the different work functions of the silicon and the silicide—calls for extra effort to build suitable transistors. Thus, the transistors and the wiring of the polycide process can be optimized independently. For 256-K dynamic RAMs, the popular silicide alternatives include molybdenum, titanium, and tantalum.

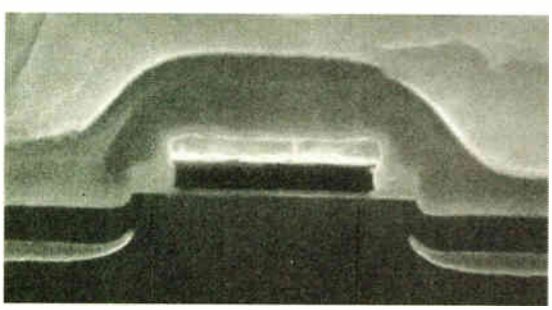
Polycide transistor gates are not the 256-K chip's sole departure from the self-aligned gate devices of older dynamic RAMs. Short-channel effects and hot-carrier problems preclude scaling down the transistors directly from 64-K devices. It can be quite hard to shorten the polysilicon gate to 2 μm from 3 μm, while maintaining the 64-K's 5-volt supply—among other reasons, because hot-carrier injection into the gate oxide can undermine long-term reliability.

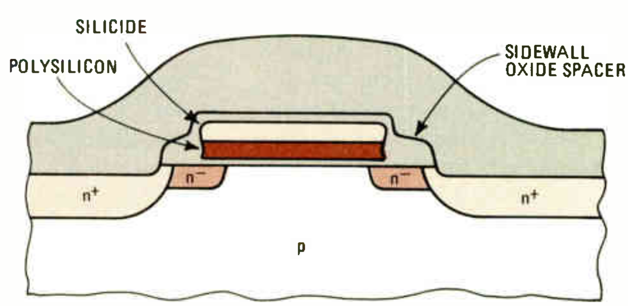
Lightly doped drains

All present methods of fabricating transistors with gates of 2 μm or less include some form of the lightly doped drain structure first disclosed by IBM Corp. Such a structure (Fig. 1) interposes an n^- region between the channel and the heavily implanted n^+ source and drain regions. By spreading out (and thus reducing the maximum value of) the electric field near the drain, the lightly doped region mitigates short-channel effects. Grading the drain-substrate junction can reduce the drain field further.

The reduced fields of the lightly doped drain structure translate into reduced hot-carrier generation and increased junction breakdown voltage. Figure 2 shows a current-voltage characteristic of the transistor in Fig. 1.

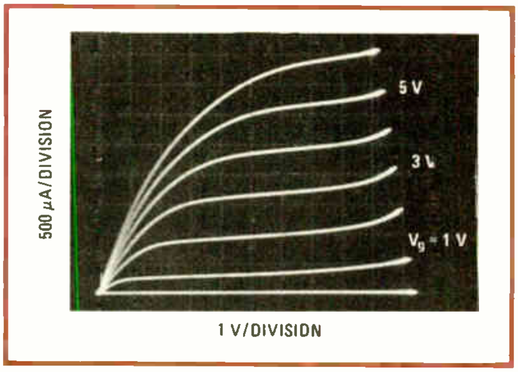
Even with device features scaled down to 2 μm, from 3 μm, industry plans now call for 256-K chip areas of





1. Field spreader. To combat short-channel effects, a lightly doped n^- region is interposed in the 256-K RAM's transistors, between the channel and the heavily doped source and drain (n^+ regions). The light implants are masked by the sidewall oxide spacer.

55,000 to 75,000 square mils—30% to 60% larger than typical 64-K parts. Since today's plastic-packaging technology cannot easily handle chips of this size in standard 16-pin 300-mil dual in-line packages, further chip scaling or advances in packaging technology are being pursued. Even so, the 64-K's pin definitions and refresh techniques were developed with an eye to the future, so it will be possible to upgrade many existing systems with 256-K parts.



2. Well-behaved. The current-voltage characteristic of the structure in Fig. 1 shows typical long-channel field-effect transistor behavior. Thanks to the lightly doped drain, the turn-on is sharp, and the drain-source punchthrough voltage is well above 10 V.

Despite the effort to make the smallest possible chip for a given memory capacity, the large 256-K chips will probably have lower initial yields than the smaller 64-K chips did. Redundancy can compensate for this, since the chip will have extra rows or columns of cells that can be switched in during wafer probing to replace defective bits.

In the early stages of volume production, redundancy may multiply the yield of usable chips three to five times. But redundant circuits can raise testing costs, access times (though by only about 3 ns in careful designs), and power consumption.

Laser blowing of fuses—a technique that minimizes the extra circuitry needed on chip—is a popular way to implement redundancy. Although the technique requires expensive equipment, its capital costs are reasonable for a high-volume product like the 256-K dynamic RAM.

The burden on lithography

Smaller device dimensions and larger chip area make the 256-K dyanamic RAM's printing and etching requirements far more difficult than those of previous dynamic RAMs. Smaller features call for finer lithographic resolution—and for greater precision, too, because sizing tolerances typically continue to be ±10% of the feature size.

Printing the wafers involves coating them with photoresist, baking, exposing, and developing them. Except in the exposing stage, the equipment used to produce 256-K dynamic RAMs will probably resemble the gear used for second-generation 64-Ks. Advanced photoresist processes (like multilayer or plasma-developable resists) may eventually be useful. However, the necessary resolution and precision can be achieved on the 256-K dynamic RAM with a simpler expedient: dyed resists, used during critical patterning steps. The dyes absorb almost all the exposing light and eliminate wafer-surface reflections, which can distort circuit patterns.

Choosing an exposure technology is less straightforward. The alternatives are full-wafer and step-and-repeat optical projection, X-ray proximity printing, and electron-beam direct writing.

Full-wafer optical projection now produce high volumes of first-generation 64-K dynamic RAMs. Unfortunatley, the equipment still falls short of the resolutions—1.5-μm or finer—needed for certain mask levels on 256-K parts. With such future improvements as deep-ultraviolet optics, resolution may no longer be a major problem—in theory.

In practice, without very tight control of wafer flatness or greatly improved depth of focus, the usable resolution over a 5- or 6-inch wafer would still not be adequate. Overlay alignment—the registration of one level of patterns to its predecessor—will be a problem, too. Automatic alignment and distortion diagnostics are not readily incorporated with full-wafer exposure, which may be used only for patterns with requirements that are less than exacting.

Electron-beam and X-ray lithography—the technologies of the future—are not developed enough for high-volume production. Of course, electron-beam resolution is on the order of 0.5 μm, with ±0.1-μm line-width control, but the present throughput is not satisfactory. Such recent advances as multiple-beam writing may lead to acceptable throughputs of about 4 minutes per wafer.

X-ray technology is developing rapidly: compact exposure equipment is now at work in pilot-line facilities. Mask making is the current obstacle to this technique. Building 1 : 1 masks of exotic materials with the tolerances needed for VLSI is especially hard for full-wafer exposure systems. X-ray step-and-repeat equipment, which has the resolution of X rays but greatly reduces the mask problem, could well be the route to a future generation of VLSI products.

At the moment, however, the 5 : 1 or 10 : 1 stepper is the popular choice for producing 256-K dynamic RAMs. Such equipment has already been used on scaled-down versions of the 64-K dynamic RAM. With currently available optics and automatic alignment, wafer-stepping equipment has produced first-generation 256-K dynamic RAMs with features under 2 μm and alignment tolerances of 0.75 μm. Automatic focusing for each exposure, as well as new site-by-site alignment accessories, will soon make further scaling practical.

Since film thicknesses have not fallen in tandem with line widths, etching has also been complicated by the scaling down of lateral dimensions. The aspect ratio of etched patterns has increased, demanding such highly directional processes as plasma etching. Plasma and reactive-ion processes etch anisotropically and uniformly by accelerating etchant molecules through an electric field perpendicular to the wafers.

All thin-film etching steps demand plasma-etching or reactive-ion–etching machines to achieve the vertical profiles needed as horizontal dimensions shrink. Single-wafer processing on critical steps also improves line-width precision and overall uniformity. New etches have been developed to deal with the stacked polycide films. Careful annealing removes damage done by plasma radiation; other post-etch treatments can avoid the potential corrosion problems of dry-etching aluminum. □

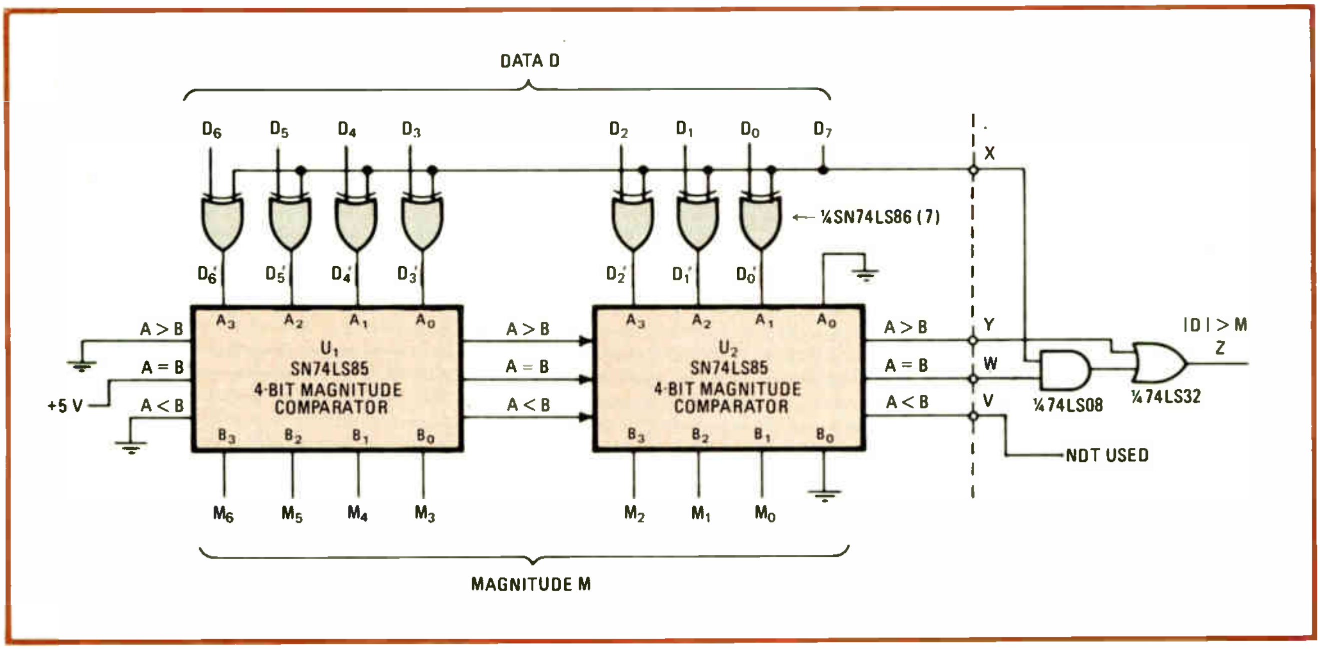
Comparator compares 2's complement numbers

by Stephen Ho and Christina Shyu
Perkin-Elmer Corp., Hayward, Calif.

This 8-bit absolute-magnitude comparator compares 2's complement numbers with a set magnitude, M. The circuit is quite useful for high-speed digital data-processing applications because it can also handle a dynamically changing M. To satisfy the condition $|D| > M$, the logic takes the absolute magnitude, $|D|$, of data input D.

The circuit compares an 8-bit data input, D_0–D_7, with a 7-bit magnitude, M. Since comparators U_1 and U_2 work with unsigned integer numbers, exclusive-OR gates invert the data if $D < 0 (D_7 = 1)$ or else noninvert it if $D \geq 0 (D_7 = 0)$.

Merely inverting the data does not, however, produce the right algorithm, so the most significant data bit, D_7,



Magnitude comparator. Using two 4-bit magnitude comparators and a few logic gates, this circuit compares an 8-bit data input with a 7-bit magnitude, M. The logic satisfies the condition $|D| > M$ and can compare higher-bit data by cascading an appropriate number of SN74LS85s.

TRUTH TABLE FOR M = 4

D	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6'	D_5'	D_4'	D_3'	D_2'	D_1'	D_0'	X	Y	W	V	Z (|D| > 4)
127	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	1
⋮								⋮												⋮
5	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	1
4	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
3	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0
⋮								⋮												⋮
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
−1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0
⋮								⋮												⋮
−4	1	1	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	0
−5	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	1	0	1	0	1
−6	1	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1
⋮								⋮												⋮
−128	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1

must be used to control output-condition pins A > B and A = B. For example, a glance at D = –5 (in the truth table for M = 4) shows that D' = |D|–1 = 4 and also that output pin A > B is not true. To get a proper output state, output-condition pin A = B is logically ANDed with the most significant data bit, D_7, whose output is then ORed with output-condition pin A > B.

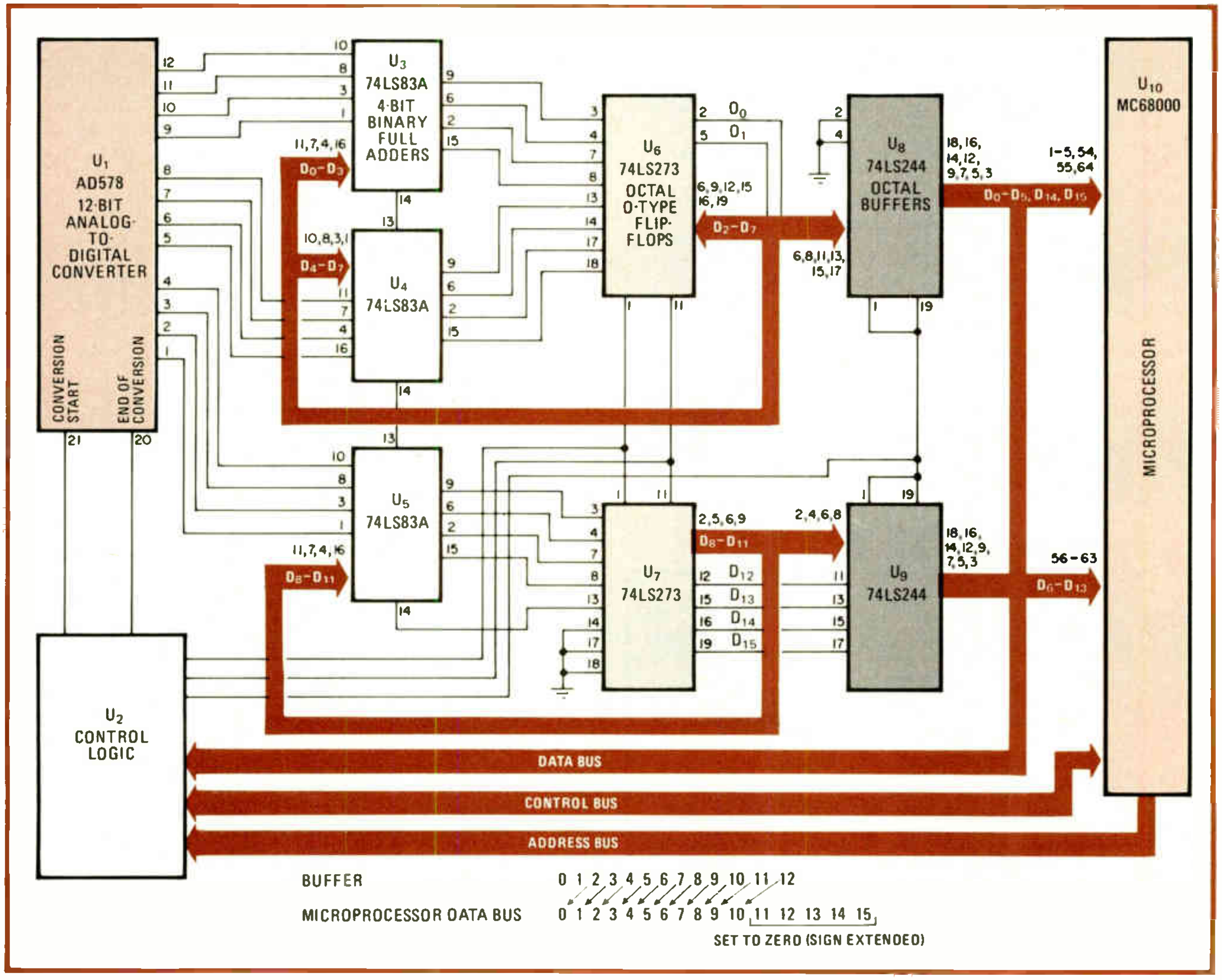
M = 4 is an example that demonstrates the design's exceptional simplicity. The table displays the truth table for detecting |D| > 4. Cascading a number of SN74LS85 4-bit magnitude comparators permits the circuit to compare larger data. □

Hardware refines digital samples quickly

by Sorin Zarnescu
Teledyne Controls, West Los Angeles, Calif.

In such applications as data acquisition, microprocessors must interface with analog-to-digital converters. Before the data can be processed digitally, the data must be smoothed to refine the sample and to cut noise-created system error.

Normally, the job would be done by adding a number of samples and averaging the sum. Although the smoothing can be accomplished with software, hardware opera-



Refining. This hardware technique improves the quality of a digital signal by taking a number of samples and averaging the sum. The logic takes up much less overall execution time than the software technique does. Four conversions are summed up and stored in the latch. The microprocessor then reads the result, shifted to the right by 2 bits—in effect, the same as dividing the sum by four.

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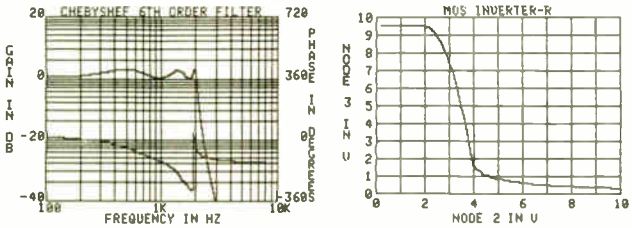

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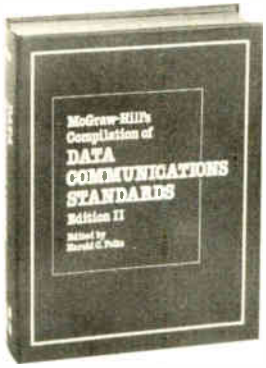

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tion reduces overall execution times, so it is attractive in high-speed processing. The method outlined here will work for any type of unipolar a-d converter—8-, 10-, or even 16-bit—and the logic is adaptable to other types of microprocessors. The design performs the division by shifting the bits to the right: for instance, it divides a sum by four by shifting rightward 2 bits.

A-d converter U_1, 8-bit latches U_6 and U_7, and octal buffers U_8 and U_9 are different locations in microprocessor U_{10}'s memory-mapped input/output space. When the microprocessor clears the latch and initiates the first conversion, a cycle comprising four conversions begins. At this point, the control logic takes over and starts to count the number of conversions and to initiate them through U_1's conversion-start pin. It does so by counting the end of the conversion signal that U_1 generates.

At the end of fourth conversion the sum is stored in latch U_6–U_7 and the control logic sends an interrupt to the microprocessor, which reads the result of the four successive additions and then extends the sign and calculates the average by dividing by four. The sign extension is obtained by grounding pins 14, 17, and 18 of U_7 and the average computed by connecting the output of U_8 and U_9 to the processor's data bus according to the scheme shown in the figure. As a result, the data is shifted by two—equivalent in effect to dividing by four—and the sign is extended without increasing execution times. □

Bipolar dc-dc converter requires no inductor

by E. Mendes
Electronics Corporation of Israel Ltd., Tel-Aviv, Israel

The saturable cores used in dc-dc converters often create radio-frequency interference that must be suppressed with filters. This coreless dc-dc converter circuit helps circumvent these rfi problems and also provides two dc voltages, one of negative and one of positive polarity with reference to ground. And it does so without using expensive and dilatory transformers or inductors.

In the circuit shown, inverters $U_{1\text{-a}}$ and $U_{1\text{-b}}$ form a 20-kilohertz oscillator whose square-wave output—further shaped by D_2, R_4, and R_5 and by D_3, R_6, and R_7—drives power field-effect transistors Q_2 and Q_3. The p-channel and n-channel FETs conduct alternately, in a push-pull configuration. When Q_2 conducts, the positive charge on C_{out} forces diode D_4 to conduct as well, which produces a positive voltage, determined by zener diode D_5, at terminal A.

Similarly, when Q_3 in its turn conducts, the negative charge on C_{out} forces D_7 to do so as well. A negative voltage therefore develops at terminal B, whose level is set by D_6. □

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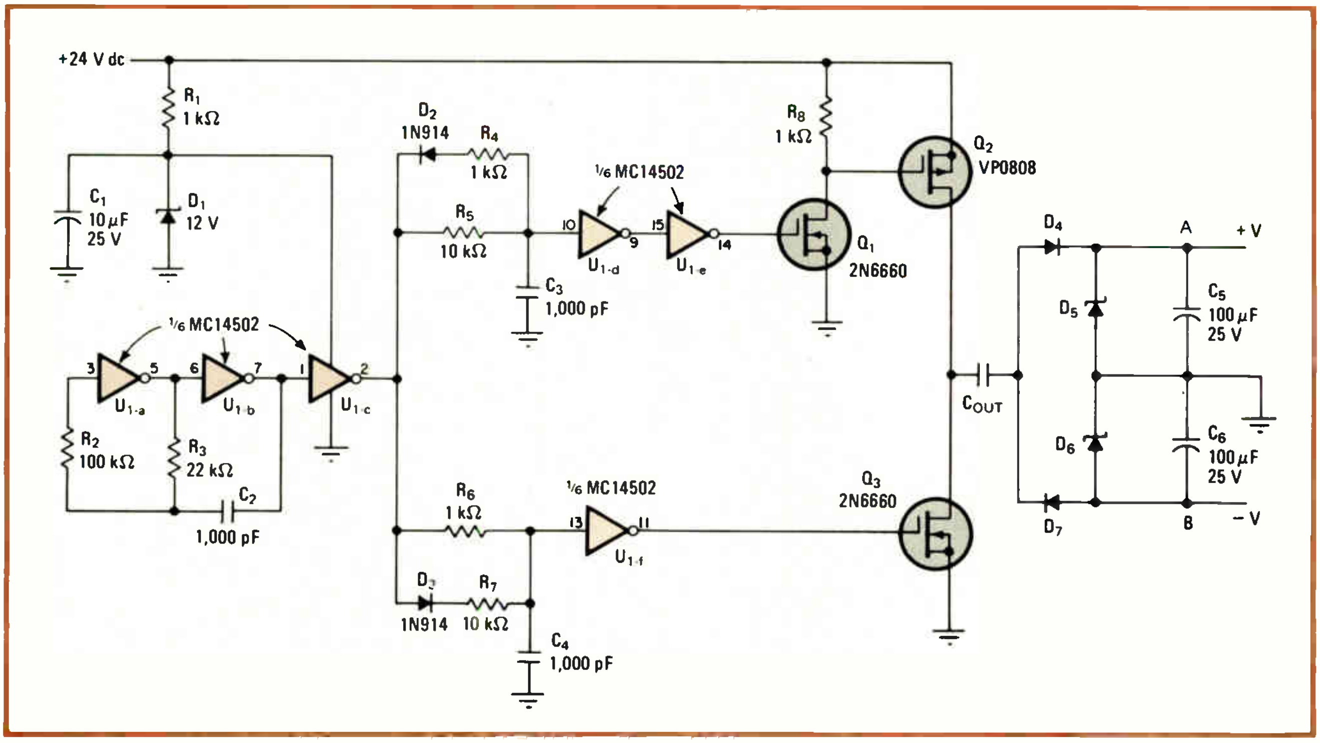


Converter. Unlike standard dc-dc converters, this circuit gives two dc voltages, one of positive, one of negative polarity—without using transformers or inductors. Only one inverter chip, three transistors, and a few discrete components are needed to realize the converter. Diodes D_5 and D_6 determine the level of positive and negative voltages at terminals A and B.

Portable computer and host talk over radio-frequency link

Advanced switching techniques in radio network connect intelligent handheld terminals to remote host processors

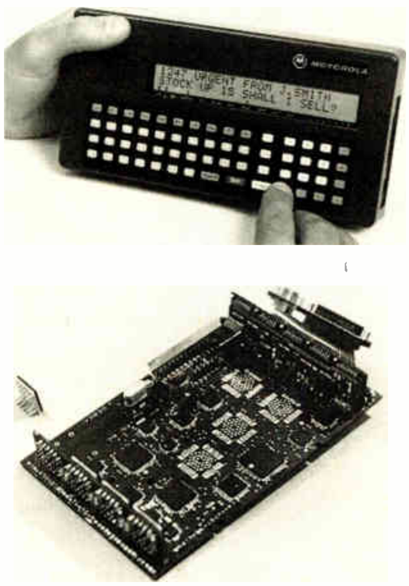
by Jay Krebs, *Motorola Inc., Communications Sector, Schaumburg, Ill.*

□ By synergizing expertise in radio systems, custom semiconductor technology, and advanced packaging techniques, Motorola has developed a truly portable computer system that not only eliminates size and weight problems, but is designed to interface directly with existing computer installations whether or not a telephone line is available. "System" is no misnomer, for the setup involves highly sophisticated communications facilities, including elaborate self-testing features.

Produced by the Communications Sector with important contributions from the Semiconductor Sector, the system features a terminal only slightly larger than a pocket calculator (Fig. 1), but with dual 8-bit processors, 160-K bytes of read-only memory, and 20-K bytes of static random-access memory (expandable to 80-K bytes). Furthermore, by incorporating both radio-frequency and telephone-line modems, it provides a choice of two-way data communications between users and remote mainframe computers.

With 32-K bytes of ROM holding the operating system, the rest, including one 32-K byte cartridge, is available for application programs. For bigger problems, the system links the portable processors to remote mainframes for calling on more data and running larger programs, as well as sending electronic mail.

The portable data-communications system was designed to provide wide-area rf coverage for a large number of users. To achieve this goal and maintain economic viability, a single pair of rf channels (at 810 and 855 megahertz for inbound and outbound communications, respectively) is continuously reused across the area of a major city and its suburbs by strategically locating base stations across the area and managing their operation with a computer. In this regard, the system resembles cellular radio-telephone networks, where 666 radio channels are reused for voice conversations.



1. Outside and inside. Inside the calculator-sized terminal hides an extremely compact computer. To meet design goals of functionality and portability, Motorola engineers needed several custom LSI circuits, high-density pin-array packages, and single in-line memory and power-control hybrids, as shown in the logic module at bottom.

System operation involves four major network components: portable data terminals, base-station radio transceivers, base-station channel controllers, and a network controller. Messages that are initiated from the portable terminal are transmitted by a single inbound 810-MHz radio channel to one or more base-station receivers (Fig. 2). Each channel's bandwidth is 25 kilohertz, and data is sent at 4,800 bits per second using direct frequency-shift modulation of the rf carriers.

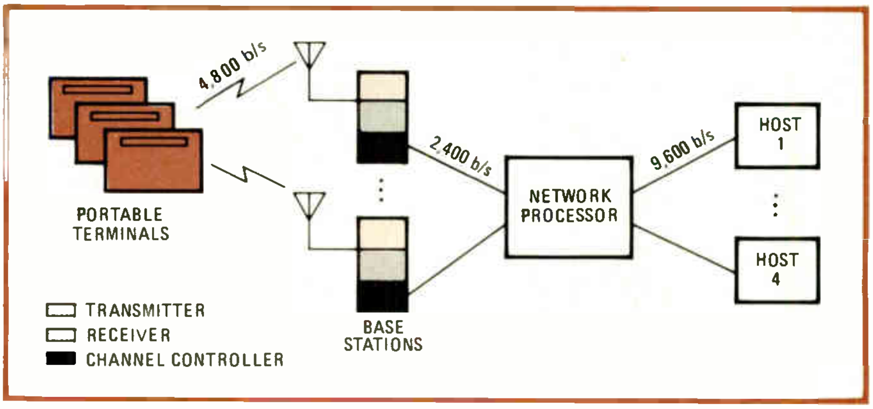
To overcome multipath fading (signal-level cancellations that occur when multiple copies of a radio signal arrive at a receiver out of phase), each base station is equipped with maximal-ratio–combining diversity receivers. Once a signal is received, it is demodulated and the resulting data is sent to the station's channel controller.

The controller recovers the data, decodes the message, performs error detection and correction, and prepares the data for land-line transmission to the central network processor. Data and control messages are exchanged between the controller and the processor using specially designed 201B-type modems and a standard bit-synchronous high-level–data-link–control protocol subset at 2,400 b/s.

The difference between the 4,800-b/s rf signaling speed and the 2,400-b/s land-line speed results from the convolutional error-correcting code employed over the rf channel. The channel controller overlaps the rf data transmission with the land-line transmission to achieve full-duplex operation, thereby reducing propagation delays in the network.

The network processor controls the net of up to 60 base-station sites and provides an interface with as many as four host computer systems. By comparing each received message's identification number and its time of arrival with prior messages from the same ID, the network processor reduces duplicate messages to a single copy—if messages arrive

2. Star topology. The network processor of Motorola's portable data-communications system is the hub of the network. Interfacing with as many as four host computers and up to 60 channel-controlling base stations, the processor supports 1,500 portable terminals.



within a defined interval, typically no more than 20 milliseconds.

Once it has decoded the message and its address, the network processor forwards it to the proper host computer system. Because each portable terminal is registered to a particular host by way of its identification number, several hosts may share the net without conflict or interference.

The host may initiate a message to a portable terminal (or group of terminals) by formatting the information with appropriate address data and routing it to a network processor. The system will support numerous host-to-terminal addressing schemes. Between the network processor and the channel controller, all of the message data including a 16-bit terminal address are embedded in the HDLC information frame. The network processor accepts the message to be delivered from the host and selects the best base station by which to communicate with the portable terminal.

In addition to furnishing message data, the channel controller provides the network processor with signal-strength information on each message copy. The digitized signal strength, in conjunction with other network topology information, is used by the network processor to select the best base station for return communications.

In the event that no recent communications have occurred with the portable terminal, or that it has moved significantly since the last communications, a search algorithm will be entered to locate it. Once the base-station selection has been made, the outbound message is scheduled for transmission.

Because there is only one outbound rf channel, base sites that could interfere with each other are not used simultaneously. An elaborate scheduling algorithm is implemented in the network processor's software to permit a high degree of frequency reuse in the system. About 1,500 portable terminals can be operated on a single inbound/outbound pair of rf channels in a typical city, depending on traffic volume and the dispersion of the base stations throughout the area.

Arbitrating random traffic

Once the outbound message has been sent by land lines to the base station, the channel controller encodes the message for rf transmission, adding error-detection-and-correction coding. The message is modulated using the same 4,800-b/s signaling scheme used on the inbound channel. The 45-watt 855-MHz base-station transmitter was specially designed for the system to permit the rapid key-up/key-down times required, while maintaining long-term reliability under continuous cycling.

The use of separate inbound and outbound rf channels increases throughput by permitting the base stations to handle inbound and outbound messages simultaneously. The rf channels are organized using a controlled contention-access technique.

The portable terminals contend with each other on the inbound channel using a technique similar to busy-tone multiple-access, providing rapid response to randomly organized traffic. To reduce the likelihood that units will interfere with each other, periodic bits in the outbound rf data stream are used to convey inhibiting information to the terminals.

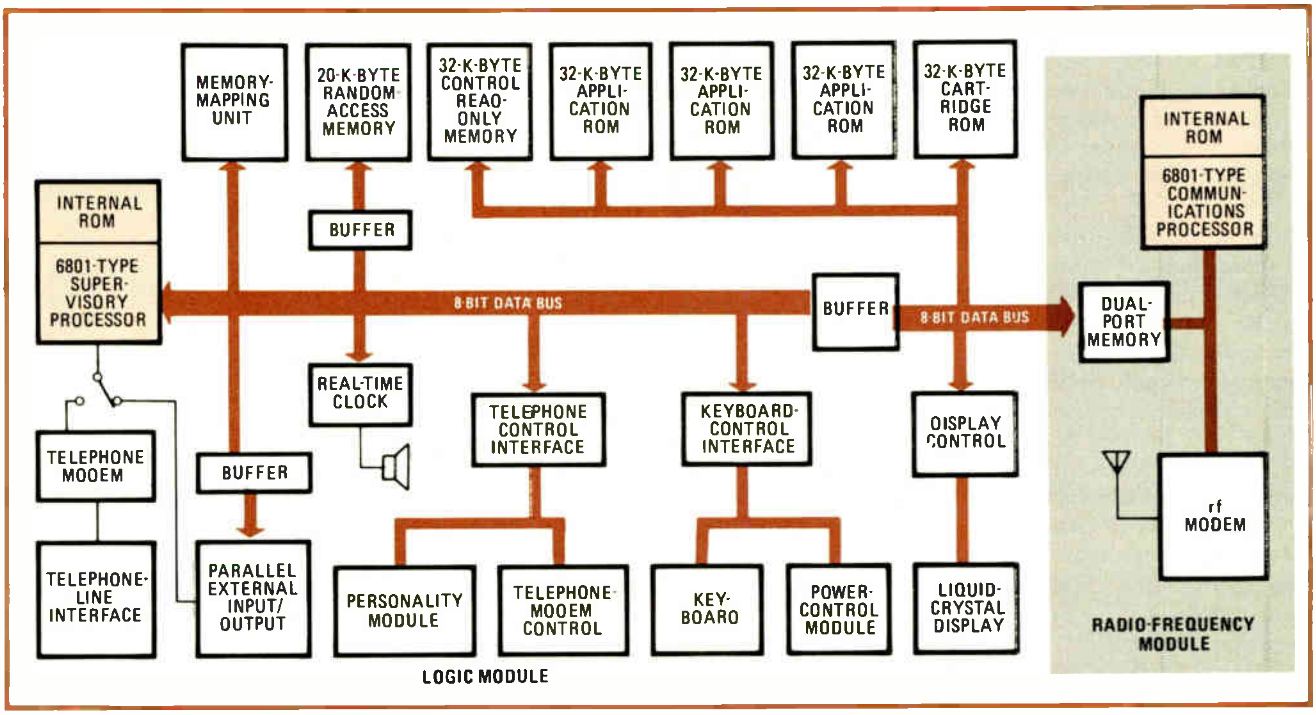
When the channel controller detects a message being received on the inbound channel and it is currently transmitting, it starts setting the inhibit indicator bits in the outbound rf data stream. When there is no outbound message being transmitted, a channel-idle message is used to carry inhibit information. The controller and the terminal perform error correction on messages received over the rf channel. Message errors that are beyond the error-correcting code's capability are detected by one or more cyclic-redundancy-check sequences built into the message formats. Errors that are detected by the CRC cause either a negative acknowledgment or no response from the message receiver.

The portable terminal or network processor will retransmit, up to three times, messages that were not immediately acknowledged or that were negatively acknowledged because of uncorrectable errors. In other words, the system incorporates forward-error correction by use of coding and backward-error correction by automatic message retransmission.

Shrinking the terminal

To realize a compact and lightweight terminal, several custom large-scale integrated circuits were designed, and innovative high-density packaging was developed. The hardware architecture of the portable terminal (Fig. 3) has two 6801-type complementary-MOS processors: one supports rf communications, and the other performs supervisory functions, plus application-specific tasks. In addition to its rf communications capability, the portable terminal contains a 300-b/s Bell-103–compatible telephone modem for use outside the network's coverage.

An external input/output connector supports both a serial interface and a memory-mapped parallel interface. The parallel interface is actually the buffered processor address and data bus with 256-K bytes of address space allocated to it. Therefore, compatible external devices



3. Terminal architecture. The portable terminal is divided into two modules. The system logic module features a supervisory processor, 160-K bytes of ROM (32-K bytes as a removable cartridge), 20-K bytes of RAM, a 300-b/s modem, and a parallel interface port. The communications module holds a dual-port memory, a communications processor, an rf modem, and a compact antenna system.

and memory can be interfaced with the terminal by means of this bus.

Since the supervisory processor directly supports only 64-K bytes of logical address space, a custom silicon-gate C-MOS memory-mapping chip was designed. The memory mapper divides 1 megabyte of physical address space into 4-K-byte segments that can be mapped into any 4-K-byte segment of the processor's 64-K-byte logical address space, on 4-K-byte boundaries. The memory mapper also provides all of the chip-selection decoding for the devices supported directly from the supervisory processor. Interrupt masking and interrupting-device identification are performed as well.

Dedicated processors: double power

A custom 256-byte dual-port C-MOS memory with semaphores provides the interface between the supervisory processor and the communications processor. One of the objectives of the portable-terminal design effort was to leave as much of the processing resources of the supervisory processor as possible for customer applications or for future system expansion. This objective led to the adoption of a dual-processor approach to the terminal design in order to offload the communications tasks into a dedicated processor.

The dual-port memory was chosen as the interface between the processors because it requires less software overhead than either serial or parallel interfaces. Also, buffering is inherent, and contention for access is controlled by simple hardware semaphores.

The software system for the portable terminal contains a number of special features. At its core is a multitasking executive control program, which permits several programs or tasks to execute concurrently. Thus communications functions can occur while an application program is executing.

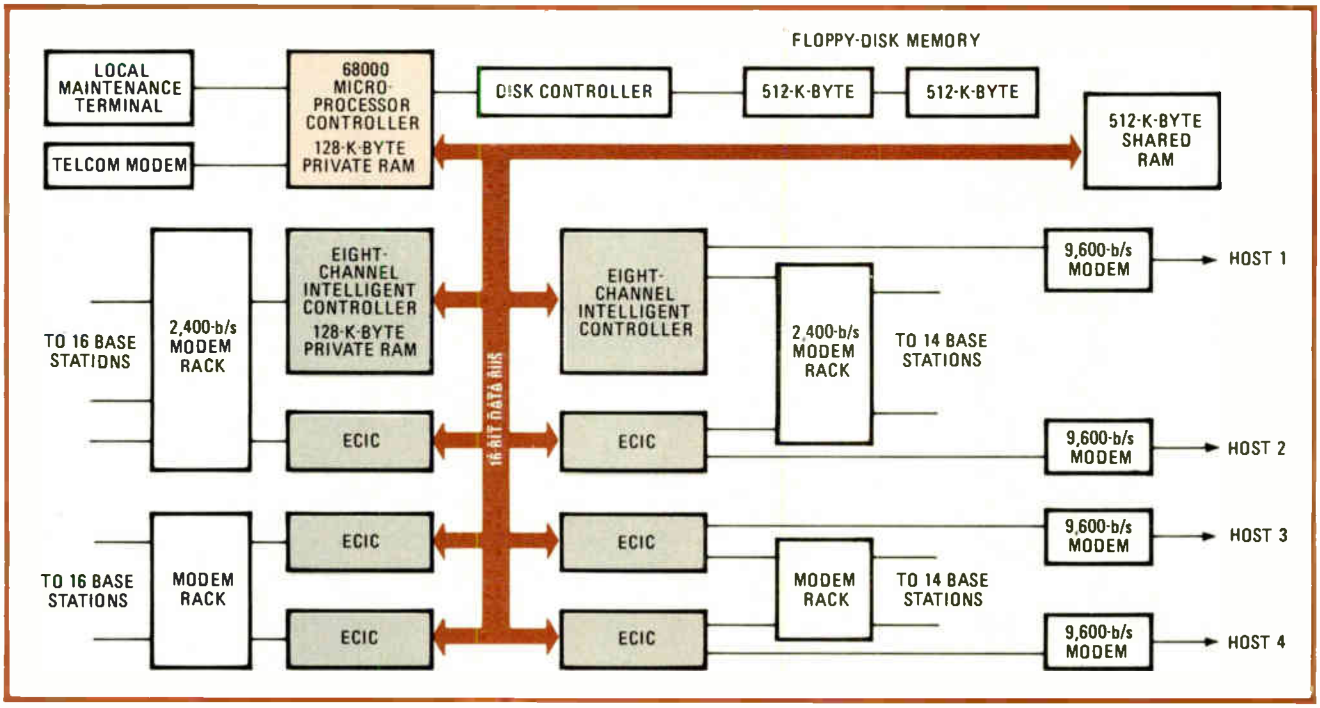
The control program also supports a RAM-based file system, allowing application programs to access data by file name and preserve data across different program invocations. With the file system, many variable-length messages can be stored, selected, and reviewed sequentially on the terminal's two-line-by-27-column liquid-crystal display. Messages (rf or telephone) are communicated to application programs using this file system, making it possible for a terminal to perform screening, encryption, data compression, and formatting before transmission. Messages transmitted from the host can be similarly intercepted by an application program to perform decryption, decompression, and reformatting before presentation to the operator.

The communications-management software supports the transmission of messages in the system. A single message transmission can contain up to 760 bytes of user data. Moreover, any number of them can be chained together, in separate transmissions, to form as long a message as a user needs to communicate. The communications manager disassembles and reassembles messages using sequence and control information that is carried in the message headers.

Wheeling and dealing from the hub

The network processor is the hub of the system. It is similar in function to a cluster controller for a hard-wired terminal network.

A typical population of 1,500 portable terminals can easily give rise to a substantial traffic load, particularly during peak periods of the work day. With the frequency-reuse feature of the rf network operating, the channel



4. Modular multiprocessor control. The system's network processor can be configured for up to four host computers and 60 base stations, depending on geographic and application needs. The maximum configuration uses 17 MC68000s to distribute control and speed response.

capacity could easily exceed the network processor's throughput capability.

Consequently, the network processor is structured around a 68000-based board that functions as the supervisory processor (Fig. 4). In addition to an 8-MHz 68000, the board also contains 128-K bytes of private RAM, 64-K bytes of programmable ROM for self-testing, two serial communications channels, and a parallel I/O channel. It communicates with eight-channel intelligent-controller (ECIC) boards and a 512-K-byte error-correcting RAM board that it shares with the ECICs over a 16-bit high-speed data bus.

The network processor's software system is divided between the supervisory subsystem, which operates from the supervisory board and the network communications subsystem, which is repeated in each ECIC. The ECIC's software subsystem supports both host and channel-controller communications. The host support is defined by the specific system implementation. Currently this is a full-function interface operating at 9,600 b/s under both synchronous–data-link–control and systems-network-architecture protocols. The interface between ECICs and the channel controllers is an HDLC subset operating at 2,400 b/s regardless of specific system configurations.

Trouble-shooting on the net

A primary concern in the design of the system was network problem determination. With multiple base sites and as many telephone links, a remote-testing capability was essential. A first step, however, is recognizing that a failure in some part of the network has occurred. These concerns are addressed by a multilevel problem-determination and on-line test facility.

The facility's first level is recognition that a problem in the network exists or that some net component has degraded to the point where a failure is imminent. Critical network links and processing nodes are continuously monitored for performance by themselves and by adjacent network nodes. When a deviation occurs, an alarm message is sent to the host system.

The base station contains numerous sensors that are monitored by the channel controller. Such hardware parameters as forward rf power, reflected rf power, the temperature of the power amplifier's heat sink, and the lock state of the voltage-controlled oscillator warn of base-station or antenna-system failure. Other parameters that are statistical in nature, such as error-to-traffic ratios, message-retransmittal counts, and error-burst hit counts, are also accumulated.

The second level of problem-determination support is on-line testing capability. When an alarm is recognized or when degraded performance is suspected, a battery of tests can be invoked on the portion of the network in question—without interrupting traffic flow. Loop tests, which send known message patterns and compare the result with the original, are used extensively. Each link has several loop-back points to enhance failure isolation. All base links can be looped at the network processor's modem interface, within that modem, and at the remote modem's analog and digital sections.

The base station's transmitter can be looped to its receiver through an rf test converter to form a complete end-to-end link test. A final loop can also be made to a portable terminal with an automatic echo-back message function.

Software can also be upgraded and tested from the remote-service link. The remote-service capability of the system is an important step in providing fast problem determination, short repair time through field-replaceable units, and a high degree of system availability. □

Testing disk drives from head to toe

To develop, produce, and use today's high-speed, high-density drives, their diverse elements must be tied together by a battery of tests

by Martin S. Albert, *Cambrian Systems Inc., Westlake Village, Calif.*

☐ The testing of disk drives has taken on new importance as the ever-increasing demand for mass storage has attracted a multitude of drive manufacturers. To compete in this market, companies must produce faster, higher-density units and therefore are seeking better testing tools with which to develop and produce drives. At the same time, users are looking for more efficient ways to check the performance of new drives, which are critical to overall computer system performance.

To develop a new drive, an engineer needs to characterize precisely the three critical disk-drive components—the head, the disk, and the data channel—as well as the complex relationship among them. In production and incoming inspection, workers must check the drive's performance and interface characteristics.

Unfortunately, there are few meaningful absolute numbers that can be applied to all drives, because the criteria against which heads, disks, and data channels are evaluated depend on the type and quality of the elements used, which in turn depend on a range of variables, such as bit density, track density, and the capability for error correction—to name but a few.

Since there is such a range of variables involved in testing disk drives, the equipment needed to test a drive must be flexible. However, certain tests apply to every phase of drive testing (see "A universal approach to disk-drive testing," p. 148). To select the right kind of instrumentation for drive testing, manufacturers and users must know the range of different tests to which a drive can be subjected.

Testing begins in the development phase. In this phase, there are five key measurements: determination of off-track-error tolerance, optimum servo-track performance, certification of the disk, head-disk performance, and data-channel capacity. The first of these measurements, that of off-track-error tolerance, tells how accurate the drive's positioning system is. In a disk-drive system (Fig. 1), the head-to-track positioning system, commonly referred to as the positioner, helps ensure the accuracy and integrity of the recorded data. It must operate reliably and with extremely close tolerances to prevent data errors.

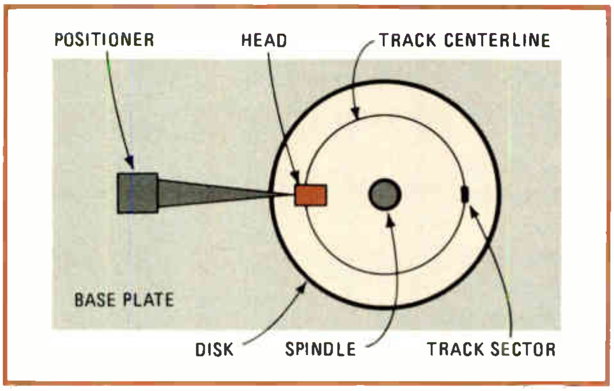
To write and read data reliably on, say, a Winchester drive, the heads must be predictably and accurately positioned over the recording tracks. The lateral position of the recording head over the data track can be affected by many factors, including thermal expansion of the components, bearing runout, disk-to-spindle alignment, vibration, and positional error. The positional error a system can tolerate is inversely related to the track density.

The worst-case assumption is that a track is written at one extreme and read at the opposite, and that two adjacent tracks are written with the positional errors both toward the other (Fig. 2). Since a Winchester-technology head does not have erase poles, the head may pick up previously recorded data in the intertrack spaces.

In off-track testing, the operator writes data to a track, the head is stepped off the track a small increment, and an attempt is made to read the data. Several iterations of this sequence—read, step, and read again—determine the tolerance within which the head must be positioned if data is to be read correctly (Fig. 3).

The absolute positioning accuracy is not as critical in such testing as is the accuracy with which the head is moved in incremental values and the speed with which the test is performed. Usually a drive can tolerate a positional error of roughly 15% of the track width before the data signal becomes unrecoverable. The actual amount tolerated depends on the performance of all system elements, including read-write circuitry, data separator, power-supply stability, and the level of the system's electrical noises.

For example, a 5¼-inch disk drive with a 1,000-track-per-inch density could have a track width of only 0.0007 in. For such a system, an off-track error tolerance of, say, 50 microinches



1. Overview. The initial attention in the design of a disk drive goes to those elements shown in this bird's-eye-view schematic. The combination of electrical, magnetic, and mechanical elements complicates the demands placed on testing drives.

would be acceptable—the head could move off the track that distance and still recover data.

Performing the test quickly ensures that temperature variances will not have an effect. The temperature across the entire disk surface must be carefully controlled in testing, to within ±0.5°F, to limit thermal expansion and contraction. With such controlled conditions, the designer can be certain that, when the head is moved off track

A universal approach to disk-drive testing

A new breed of test systems can provide an integrated approach for disk-drive testing. These systems can test individual components—heads, disks, and the head-disk assembly—as well as the entire disk drive, with modules whose accuracies are orders of magnitude greater than the component or drive to be tested.

In addition to supplying the tools needed for development of disk drives, such modular disk-drive test systems can easily be converted into task-oriented systems—such as disk, or media, certifiers, head-disk-assembly testers, or system testers. Consequently, individual disk-drive components can be tested during the production phase with essentially the same tools as were originally used to design it, and continuity between design and production is thereby maintained. The areas in which modules provided by Cambrian Systems can be used to configure test systems are shown in the accompanying table.

For a test system to tackle the various measurements needed during both design and production, as well as in incoming inspection, there are five areas of performance that must be scrutinized: head positioning, spindle speed control, servo pattern writing, selection of data-channel capacity, and programmability.

Precise and repeatable positioning capability is of crucial importance in characterizing a disk drive's head-to-disk interface. For current-technology drives, a test system should be able to position the magnetic recording head to a resolution of 1 microinch and to an accuracy of 3 or 4 μin. in a controlled-temperature environment. Cambrian Systems' units can attain a resolution far smaller than is currently needed, so that it will be possible to develop and test future disk drives with their aid.

The disk spindle must be rotated at variable speeds, accelerations, and decelerations. The spindle drive should be programmable for speeds from 500 to 6,000 revolutions per minute in 1-rpm increments, with an accuracy of 0.01%. Speed jitter should be no more than 1 microsecond, peak to peak, at 3,600 rpm, which translates into about 1 part in 16,000.

The ability to write a wide variety of servo patterns—data on the disk that allows the head to be quickly and accurately positioned—is crucial in developing drives with high accuracy and storage density. Although there is a wide variety of possible patterns and approaches that a designer can use, most servo patterns are chosen without first experimenting, because most test systems are unfriendly to the experimenter. To aid the designer, a test system should permit a programmable clock track to be written in an 8-to-75-megahertz bandwidth and should provide pattern generation up to 75,000 transitions per second.

To test present and future drives, an engineer needs a read-write data-channel bandwidth that will accommodate current and anticipated disk performance. For example, the high-performance IBM 3380 has a data transfer rate of 24 megabytes per second, which requires a data channel bandwidth of approximately 15 to 18 MHz. Cambrian Systems' test modules are specified over a 1-to-50-MHz bandwidth to within 1 decibel and for phase linearity to within 2°. For future needs, a disk-drive test system should have a bandwidth greater than 18 MHz, and a phase linearity of better than 1° over the entire frequency range is desirable.

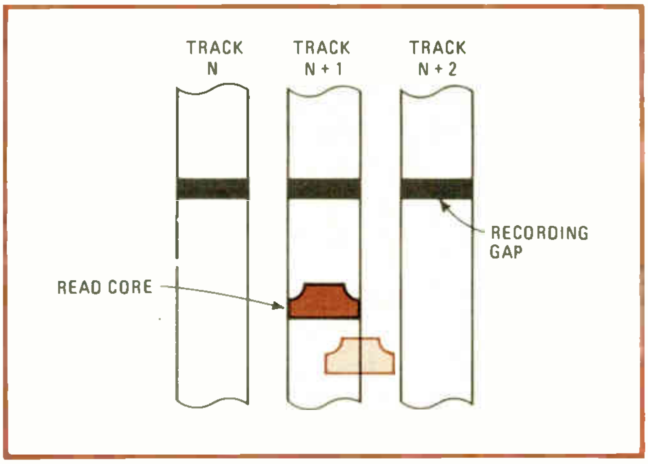
If a system is to tackle the diverse requirements of disk-drive testing, an extremely flexible means of programming tests is also mandatory. Cambrian Systems' tester uses the Forth programming language to create a library of primitive elements from which tests can be created.

The primitives, or microcommands, include such functions as an incremental seek, specified in microinches from the present head location; an absolute move from one head location to another, specified with respect to the center of the disk; the ability to change the write current and frequency; and the ability to alter spindle speed up or down with 1-rpm resolution. These tests can be strung together into macrocommands, from which, in turn, the user can create test sequences.

CONFIGURATION MATRIX FOR DISK-DRIVE TESTING

Module capability	Test arena						
	Development	Production					Final/ incoming
		Head	Media	Servo writer		HDA	
				disk	HDA		
Precision spin stand	X			X			
Low cost spin stand		X	X				
Head-and disk-assembly (HDA) spin stand					X	X	
Servo pattern generation	O			X	X		
Media defect testing	X		X			X	
Magnetic characterization	X	X	X			X	
Timing						X	X
Window margin	O	O	O			O	X
Various drive interfaces							X
Temperature-air control	X			O	O		

X = necessary, O = desirable



2. Offtrack. The relative position of the read head with respect to the track is critical for high-speed operation. In the ideal position (solid color), data is read without interference, but in the worst case (tint), pickup from other tracks can create noise and induce data errors.

in testing, the move was indeed 50 μin. and was not affected by spindle-bearing runout, temperature changes, or other variables.

With a test system that can accurately position the head, a disk-drive designer can determine how much position offset is actually present in a drive. The test system must have an error tolerance much lower than the actual tolerance—about a tenth of the actual tolerance, or 5 μin. in the example given above, if measurements are to be meaningful. Today, a 3-to-5-μin. accuracy in incremental positioning is achievable with state-of-the-art test systems.

Selecting the optimum servo pattern

Once the tolerance of the system is determined, the designer can begin to consider what type of servo pattern should be used in the system. In an operational disk drive, one of two basic techniques is used to control the head-positioning system: an open-loop stepper motor or a closed-loop track-following servo. An open-loop stepper system moves the head to the expected track location and remains at that location; it does not follow the track should it move.

To achieve higher track densities and to accommodate interchangeable disks in cartridges, a track-following system is needed. It finds a track and keeps the head over the track, even if the latter wanders out of its concentric pattern. The goal is to position the recording head over the track as accurately as possible and keep it on track. A typical servo track format is illustrated in Fig. 4.

Many servo formats have been developed and new concepts are continually being created because they are critical to the accurate operation of a disk drive. To develop an optimum servo format for a new disk drive, a designer first must decide what is technically feasible. Next, the designer must create the format, implement it, and test it. Finally, the servo pattern itself and the electronics that demodulates the raw pattern data to obtain position information are developed.

In testing a servo format, the servo head is positioned between the two servo tracks and is moved in and out until the amplitude of the position pulses in adjacent servo fields is equal. Doing this defines the positions of the data tracks. An automated disk-drive test system can speed and simplify this process immensely.

With such a system, the designer can write a variety of servo patterns on a disk surface in a highly accurate, repeatable manner, knowing exactly what and where data is written. The test system can eliminate external variables, such as position jitter, during the writing sequence. Thus a designer can write a pattern precisely.

If the test system itself is able to demodulate the data as it is read back, the designer can concentrate solely on the servo design by simply looking at the demodulated data to determine the kind of position error being caused by the pattern and servo hardware. Such a test system therefore provides real-time flexibility in creating and modifying a pattern.

Certifying the disk

To make sure that the system will work with standard disks, the designer must certify the disks he uses in testing. Tests used to certify a disk generally follow the definitions of the American National Standards Institute. That is, the integrity of the entire disk surface is first validated; pulse dropout, pulse drop-in, and modulation across the disk surface are identified. Next the disk is checked for resolution, overwrite, isolated-pulse width, and saturation, as well as linearity and residual noise.

Of all these tests, the ANSI PW50 one for measuring the width of an isolated pulse is particularly useful. The points of measurement are those on the pulse's rising and falling edge that are at 50% of the pulse's peak amplitude. Measuring the width of an isolated pulse determines the ability of the disk to record higher bit densities, and therefore the test is often used in place of a resolution test.

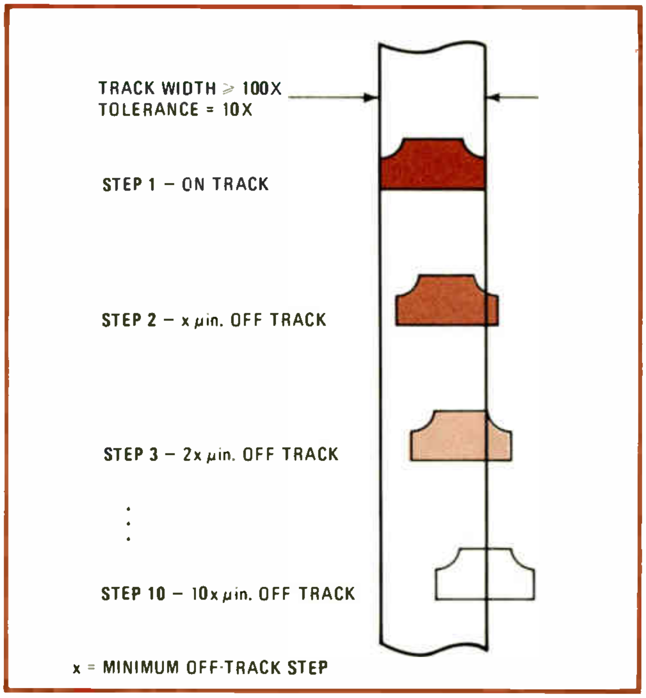
In effect, the pulse-width test is a composite measurement of the data channel's frequency response and phase error—including the head and the disk. As densities stretch beyond 10,000 b/in., this measurement becomes increasingly useful.

Checking head-disk performance

For disk certification, the designer needs well-characterized heads, so that the measurement results can be attributed to disk characterisitics. Conversely, when heads are being developed, the disk must be a constant. But measuring the performance of the head and disk together and determining their interface characteristics is a more essential part of disk-drive characterization. The designer must see how the disk and head work together to maximize drive performance.

The goal in head-disk testing is to eliminate all the other unknowns in the system, such as spindle runout, so that the designer can examine only those performance attributes related to the heads and the disk. A disk-drive development system can provide this capability, using many of the disk certification tests.

Head-disk tests include resolution, overwrite, pulse width, and saturation, as well as peak shift and pulse crowding. The tests can be combined in many different ways, depending on the results needed. With a program-



3. Position control. To determine off-track tolerance, the designer must precisely position the read head in increments and must read data until it begins to degrade. Typically, tolerance is about one tenth of the track width, and test increments are one tenth of this tolerance.

mable tester, designers can create and implement their own test sequences.

Once the designer is sure that the head and disk are working correctly, the path to them—the data channel—must be checked. To test the data channel, which consists typically of a head, a read-write chip, a phase-locked loop, a coding function, a decoding function, and perhaps an error-correction function, a pattern must be generated to simulate an actual file environment. By defining a particular file format in software, a designer can generate a pattern, output it through the data channel under test to the disk, and perform a read-back to verify the integrity of the data. In this way, the designer can identify the areas that do not verify to the bit, byte, field, or sector location in the record.

For this kind of testing, a sophisticated pattern generator is needed to interface to the user's data channel, through a serializer-deserializer. The data is typically sent in a nonreturn-to-zero format. The encoding-decoding function will usually be in the user's hardware.

Production and system tests

Once disk-drive design is completed and the commitment to production is made, a series of tests is required during assembly and before shipment to users. As in development, the first tests to be performed are those certifying the disk, testing the heads, writing the servo pattern, and verifying the servo writing, after which the head-and-disk assembly is tested. Finally, the complete disk-drive system is tested.

Absolute certainty about the integrity of the disk is required. In production, a manufacturer may choose to perform a disk-certification test, such as those used during development and by the disk manufacturer.

The disk is certified for surface defects, axial accelera-

Trends in disk-drive production testing

Several emerging trends in production testing of disk drives point to more testing in the factory, including window margin tests, and the use of more versatile test equipment and software to carry out these tests.

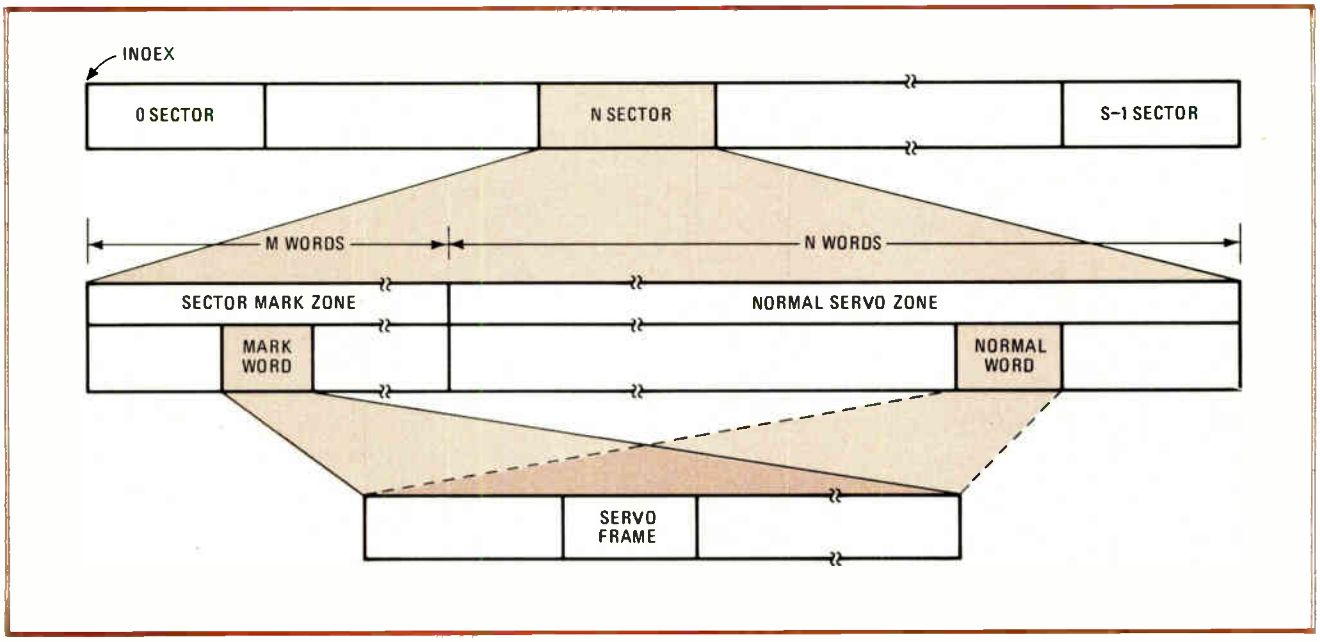
One trend is for manufacturers to perform tests at every step in the production process—from certification of the disk to final assembly. A second is greater use of margin testing to decrease the return of drives shipped to customers. Because drives contain thousands of components—thereby increasing potential failures—"forgiveness" must be designed into some of these components. The assumption is that the statistical mix of components will provide the needed margin. (To design a worst-case drive would be too expensive.) End-of-production-line testing, then, supports this intuition and analysis.

A third trend is for disk-drive manufacturers to perform all of the tests described in the accompanying article. In addition, the manufacturers are performing 48-hour burn-in and power-cycling tests before shipping drives.

A fourth trend is the growing availability of test equipment that can be operated by production personnel, as well as by skilled technicians. These testers can also be used by engineers in the developmental phase. Software allows engineers to access individual tests and get the repeatability they need for development.

Advances in magnetic recording technology promise to make possible new generations of disk drives with even higher densities and capacities in shrinking configurations. For instance, a spiraling increase in storage density can be predicted beyond the current 10,000 bits per inch nominally achieved with the combination of ferrite head and oxide coating. Industry estimates point to 15,000-b/in. and 800-track-per-in. densities using thin-film heads of the IBM 3380 type in conjunction with oxide media. Density could easily grow to 25,000 b/in. and 1,200 tracks/in. using ferrite heads and thin-film plated disks. Moreover, the application of vertical recording techniques augurs a phenomenal increase to 100,000-b/in. densities.

Development and test equipment is often one or two generations ahead of product development. Indeed, in disk drives, it can already accommodate the next level of parameters, such as bandwidths up to 50 megahertz, digital performance beyond 50,000 flux reversals per second, and track position accuracies in the subnanosecond range. The testing industry can also be expected to develop flexible, cost-effective systems to accommodate the upper reaches of magnetic recording technology, and, as needed, optical recording techniques. It is only with the help of this new generation of development and test equipment that the new storage devices will be possible.



4. Repositioning. To adjust for disk irregularities, which make tracks wander, drive designers embed position data in the tracks, as shown above, so that a closed-loop servo system can reposition the head. In designing a system, a variety of servo formats should be tried.

tion and other properties of the substrate, disk flatness, and disk runout. A transducer about 5 mils above the surface is used to check vertical runout; it is capable of picking up 10 to 20 μin. of runout. Only the total runout is measured, not the location of the irregularity.

Because a 90% yield in Winchester recording heads is typical, the manufacturer may choose to test individual heads. They are mounted on a well-characterized head and disk assembly and tested for resolution, overwrite, and saturation.

After certified disks are assembled into a module, servo patterns are written by a servo-track writer. Medium quality is the most stringent requirement for servo writing, since anomalies of the disk can affect the eventual position-error signal. Once the servo tracks are written, the accuracy of the servo writing is verified.

Testing the head and disk assembly

Following disk certification and servo writing and verification, the head, disk, positioner, and spindle assemblies are combined into an assembly in a clean room. After assembly, the clean-room-exit test is performed to verify the operation of the assembly.

In normal handling there is a high probability of damage occurring in assembly. Therefore the assembly test is used to verify the magnetic characteristics of the head and disk combination and to see that no new surface defects have cropped up during assembly operations. An assembly tester must perform resolution, overwrite, and defect tests over the entire surface of every disk.

If the head and disk assembly passes these tests, it leaves the clean room to be combined with electronics to form a completed disk drive. Then, if final system tests indicate that rework is needed, the fault can be isolated to the electronic elements, thereby averting costly disassembly, retesting, and reassembly in the clean room.

Once the head and disk assembly, electronics, and other components are mounted on a chassis, the manufacturer is ready to perform system tests—the final series of tests, in which the drive is tested as a complete system. The primary objective of these tests is to ensure that the disk drive operates to specifications. The secondary objective is to make certain it has the margins to function in the user's environment, which is usually more stringent than the manufacturer's. A wide range of system tests can be performed by the manufacturer, and a user may also wish to perform some or all of these tests as a part of incoming inspection.

Of the dozen or so tests that are usually conducted, one has become particularly useful: the read-margin test. The read-margin test, which is becoming a *de facto* standard, checks for shifts, or margins, in the window in which data is read. This is a measure of the maximum peak shift (in nanoseconds) due to pulse crowding in the data read by the drive head from the disk. Though many variables—such as the disk and head characteristics, write current, frequency response, and phase errors—can affect the results, in general the smaller the peak shift is, the less likely that read errors will occur.

There is a high correlation between low read margins and low drive error rates. Say a 5-megabyte Seagate-standard, 5¼-in. Winchester has a total available window of 100 ns. The test measures what is left over after peak shift and other variables have consumed portions of the window. It moves the window in 2-ns increments, first in one direction until it finds the limits of the window, then in the other direction. For a 100-ns shift window, a margin of 40 ns is considered superior.

The error rate of a disk drive designed at 10^{10} bits translates into less than one read error in every 10^{10} reads. Directly measuring this can take considerable time, that is, more than an hour; an alternative—the application of error-rate testing—correlates window size (margin) with expected error rate in much less time. □

Terminal program serves CP/M-based systems

by James P. Osburn
Applied Computing Devices Inc., Terre Haute, Ind.

This program, for CP/M 2.2–based microsystems, helps the keyboard integrated with the cathode-ray-tube display to behave like a terminal. The program uses the least significant 2 bits of the IOBYTE system variable to emulate one connection between the keyboard and the CRT and another between the CRT and the microsystem's RS-232 interface. When the bits are 01, the console in use is the CRT, and when the bits are 00, the console is the RS-232 interface connected to a teletypewriter or a modem. The program can be applied to any CP/M 2.2-based system that implements IOBYTE.

The program operates with and without local echo. To determine which, it first seeks the E option switch on the CP/M command line that decides the echo mode. Next, the program enters a loop that switches constantly, via the IOBYTE, between the TTY and CRT. When the program finds one device ready with a character, it sends the character to the other device until it sees the attention character. If the echo option is on and the character is from the keyboard, the program sends the character back to the CRT. When no local echo is desired, TERMINAL must be the response typed to >— TERMINAL E— the CP/M prompt for operation with local echo.

Finally, typing in control A terminates operation and returns control to the CP/M operating system. □

TERMINAL EMULATION PROGRAM FOR CP/M-BASED MICROSYSTEM

```
0100              terminal  org   100h        ;CP/M transient program to
                                              ;behave as a terminal.
                                              ;Use "terminal" command for
                                              ;operation without local echo.
                                              ;Use "terminal [E]" command
                                              ;for operation with local echo.

0001    =         cntrla    equ   1           ;attention code

0100    AF        main      xra   a           ;clear local echo flag
0101    328701              sta   echo
0104    CD8B01              call  scanopts    ;scan for command line options
0107    CA1401              jz    main1       ;IF options found THEN BEGIN
010A    23                  inx   h               ;advance to first option
010B    7E                  mov   a, m
010C    FE45                cpi   'E'             ;test first option
010E    C21401              jnz   main1           ;IF it is 'E' THEN
0111    328701              sta   echo                ;set local echo flag
                                              ;END
0114    CDAC01    main1     call  gtiobyte    ;save iobyte for exit
0117    328801              sta   sviobyte
011A    3EFF                mvi   a, 0ffh     ;set cathode-ray tube character
011C    328901              sta   crtchar
011F    CDAC01    main2     call  gtiobyte    ;REPEAT set console to crt
0122    E6FC                ani   0fch
0124    F601                ori   1
0126    CDB101              call  ptiobyte
0129    CDB701              call  dirin           ;check for crt input
012C    328901              sta   crtchar
012F    B7                  ora   a
0130    CA5601              jz    main4           ;IF crt input THEN BEGIN
0133    3A8901              lda   crtchar
0136    FE01                cpi   cntrla              ;check for attention code
0138    CA5601              jz    main4               .IF not attention THEN BEGIN
013B    3A8701              lda   echo                    ;check echo flag
013E    B7                  ora   a
013F    CA4801              jz    main3                   ;IF local echo THEN
0142    3A8901              lda   crtchar                     ;do local echo
0145    CDBE01              call  dirout
0148    CDAC01    main3     call  gtiobyte                  ;set console to tty
014B    E6FC                ani   0fch
014D    CDB101              call  ptiobyte
0150    3A8901              lda   crtchar                   ;send crt input to tty
0153    CDBE01              call  dirout              ;END
                                              ;END
```

```
0156  CDAC01   main4      call  gtiobyte        ;set console to tty
0159  E6FC                ani   0fch
015B  CDB101              call  ptiobyte
015E  CDB701              call  dirin           ;check for tty input
0161  328A01              sta   ttychar
0164  B7                  ora   a
0165  CA7801              jz    main5           ;IF tty input THEN BEGIN
0168  CDAC01              call  gtiobyte            ;switch console to crt
016B  E6FC                ani   0fch
016D  F601                ori   1
016F  CDB101              call  ptiobyte
0172  3A8A01              lda   ttychar             ;send tty input to crt
0175  CDBE01              call  dirout          ;END
0178  3A8901   main5      lda   crtchar       ;UNTIL crt character is attention code
017B  FE01                cpi   cntrla
017D  C21F01              jnz   main2
0180  3A8801              lda   sviobyte      ;restore  iobyte
0183  CDB101              call  ptiobyte
0186  C9                  ret
                                            ;mainline variables
0187  00       echo       db    S-S         ;local echo flag
0188  00       sviobyte   db    S-S         ;saved iobyte
0189  00       crtchar    db    S-S         ;crt input character
018A  00       ttychar    db    S-S         ;tty input character

                                            ;scan for '[' before option switch
018B  218000   scanopts   lxi   h, 80h      ;hl points to command string tail
018E  7E                  mov   a, m        ;get tail length
018F  B7                  ora   a
0190  C8                  rz                ;don't scan if no tail
0191  47                  mov   b, a        ;make b string counter
0192  3E5B                mvi   a, '['      ;a:=options token
0194  23                  inx   h           ;advance hl to first character
0195  BE       scanopt1   cmp   m           ;REPEAT
0196  C29B01              jnz   scanopt2        ;IF '[' found THEN
0199  0601                mvi   b, 1                ;counter := 1
019B  23       scanopt2   inx   h               ;advance hl to next character
019C  05                  dcr   b               ;counter :=counter -1
019D  C29501              jnz   scanopt1    ;UNTIL counter=0
01A0  2B                  dcx   h           ;back up to '['
01A1  06FF                mvi   b, 0ffh     ;b:=found flag
01A3  BE                  cmp   m
01A4  CAA901              jz    scanopt3    ;IF '[' not found THEN
01A7  0600                mvi   b, 0            ;b:=not found flag
01A9  78       scanopt3   mov   a, b
01AA  B7                  ora   a
01AB  C9                  ret
                                            ;CP/M iobyte functions
0005  =        bdos       equ   5

01AC  0E07     gtiobyte   mvi   c, 7        ;get iobyte into register A
01AE  C30500              jmp   bdos

01B1  0E08     ptiobyte   mvi   c, 8        ;put register A into iobyte
01B3  5F                  mov   e, a
01B4  C30500              jmp   bdos
                                            ;CP/M console functions

01B7  1EFF     dirin      mvi   e, 0ffh     ;direct input to register A
01B9  0E06                mvi   c, 6        ;zero means not ready
01BB  C30500              jmp   bdos

01BE  0E06     dirout     mvi   c, 6        ;register A to direct output
01C0  E67F                ani   7fh
01C2  5F                  mov   e, a
01C3  C30500              jmp   bdos

01C6                      end
```


- Key in program
- Initialize by pressing F2, V
- Enter data
- Execute

Engineer's newsletter

Keep your products quiet, avoid the long arm of the law

Electromagnetic interference can get out of electronic and computer products like enraged bees from a hive, causing plenty of noise in other electronic products. **Learn to make your own pesticides against emi from a five-page booklet,** "Shielding against Electromagnetic Interference," from Tecknit, a manufacturer of shielding materials. To get your free copy, contact Corporate Communications, Tecknit, 129 Dermody St., Cranford, N. J. 07016; (201) 272-5500 (and see related story, p. 131).

Staying in touch with foreign technology

A new weekly newsletter takes some of the drudgery out of searching for reports on technology developments outside the U. S. **Each issue contains 50 to 80 one-paragraph summaries of reports from some 50 countries** with which the National Technical Information Service has technical-information exchange agreements. NTIS will send its Foreign Technology/TAY Newsletter to you for $75 a year. Mail a check or money order to NTIS at 5285 Port Royal Rd., Springfield, Va. 22161, or else call (703) 487-4650 and use a credit card.

How to freeze a voltmeter reading

Haven't you often wished you could make a voltage measurement on a difficult-to-reach or -hold test point without having to lift your eyes to the voltmeter display? It is simple to build a little hold circuit with a 0.02-μF capacitor and a complementary-MOS operational amplifier. The capacitor charges up to the voltage, and the op amp buffer between the capacitor and the voltmeter keeps the measurement until you can look at the display. M. J. Salvati of Flushing Communications, in Flushing, N. Y., says you can use Fairchild's CA3130 or CA3160 or Intersil's ICL7611 op amps that have maximum ratings of 16 V. A pushbutton labelled Acquire uses a 1-MΩ resistor to connect the junction of the hold capacitor and the noninverting input of the op amp to the high end of the probe. Another pushbutton, Discharge, provides a 1-MΩ shunt across this hold capacitor to clear the display. **After applying the probe to the test point, press the Acquire switch for a second and then release it.** Your voltmeter display will show the reading until you press Discharge.

Like to fix your own VAX machine or other DEC computer?

Digital Equipment Corp. now has a handbook for maintaining the computers and associated equipment it makes. The 110-page volume, called the "The Self-Maintenance Handbook," **covers service planning, site preparation and installation, remedial and preventive maintenance, and product upgrades.** You can get a free copy by writing to Digital Equipment Corp., Self-Maintenance, MK01/W83, Continental Blvd., Merrimack, N. H. 03054.

Time to nominate a deserving colleague

The American Federation of Information Processing Societies invites you to nominate accomplished candidates for three awards to be presented July 9, 1984, at the National Computer Conference, in Las Vegas, Nev. **The awards are the Harry Goode Memorial Award, the Afips Education Award, and the Distinguished Service Award.** But you will have to hurry, as the nominations must be submitted by Oct. 1. For nomination forms, the selection criteria, and other information, call the Afips Communication Department at (703) 620-8914 or write to 1899 Preston White Dr., Reston, Va. 22091. **–Tom Manuel**

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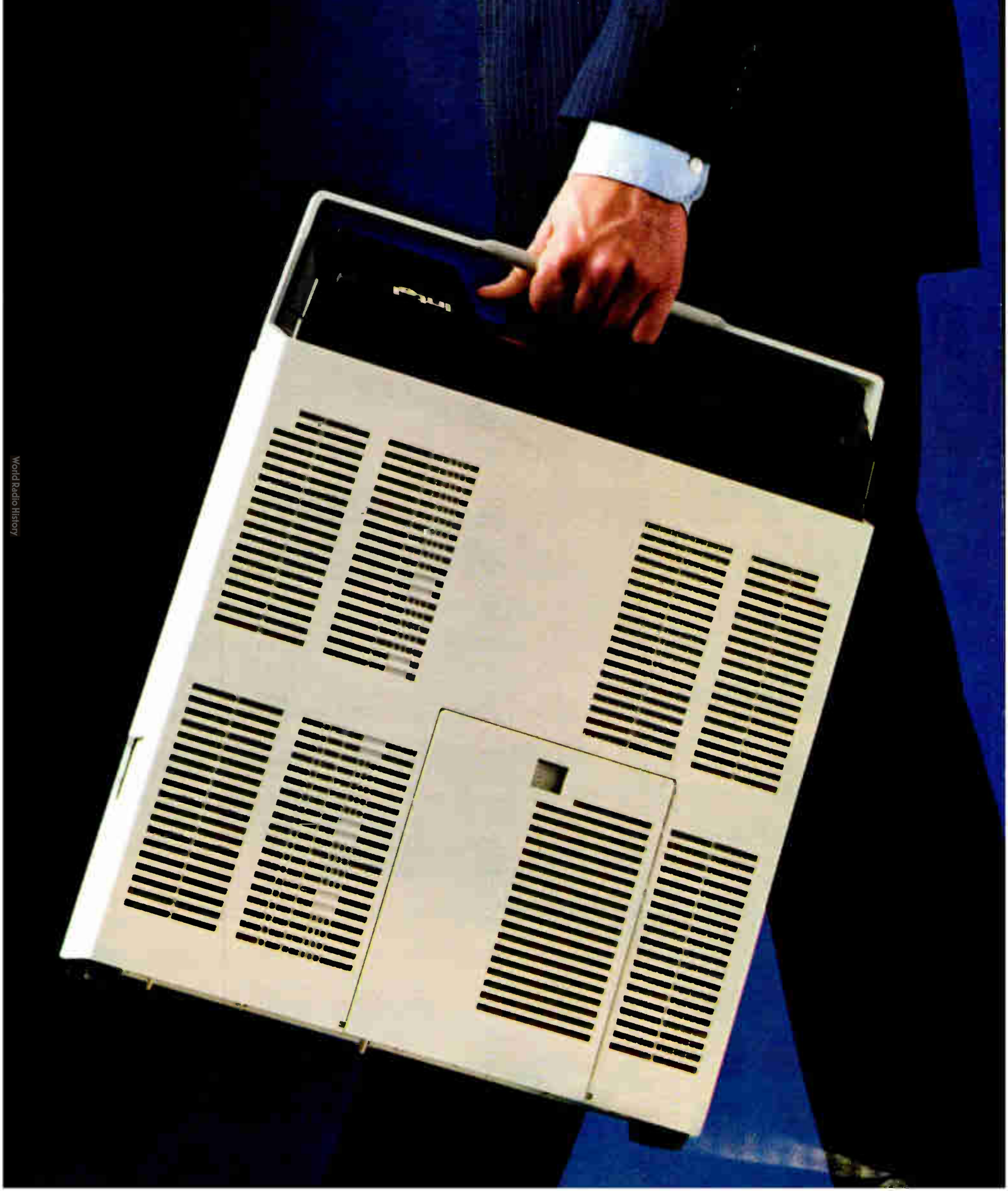

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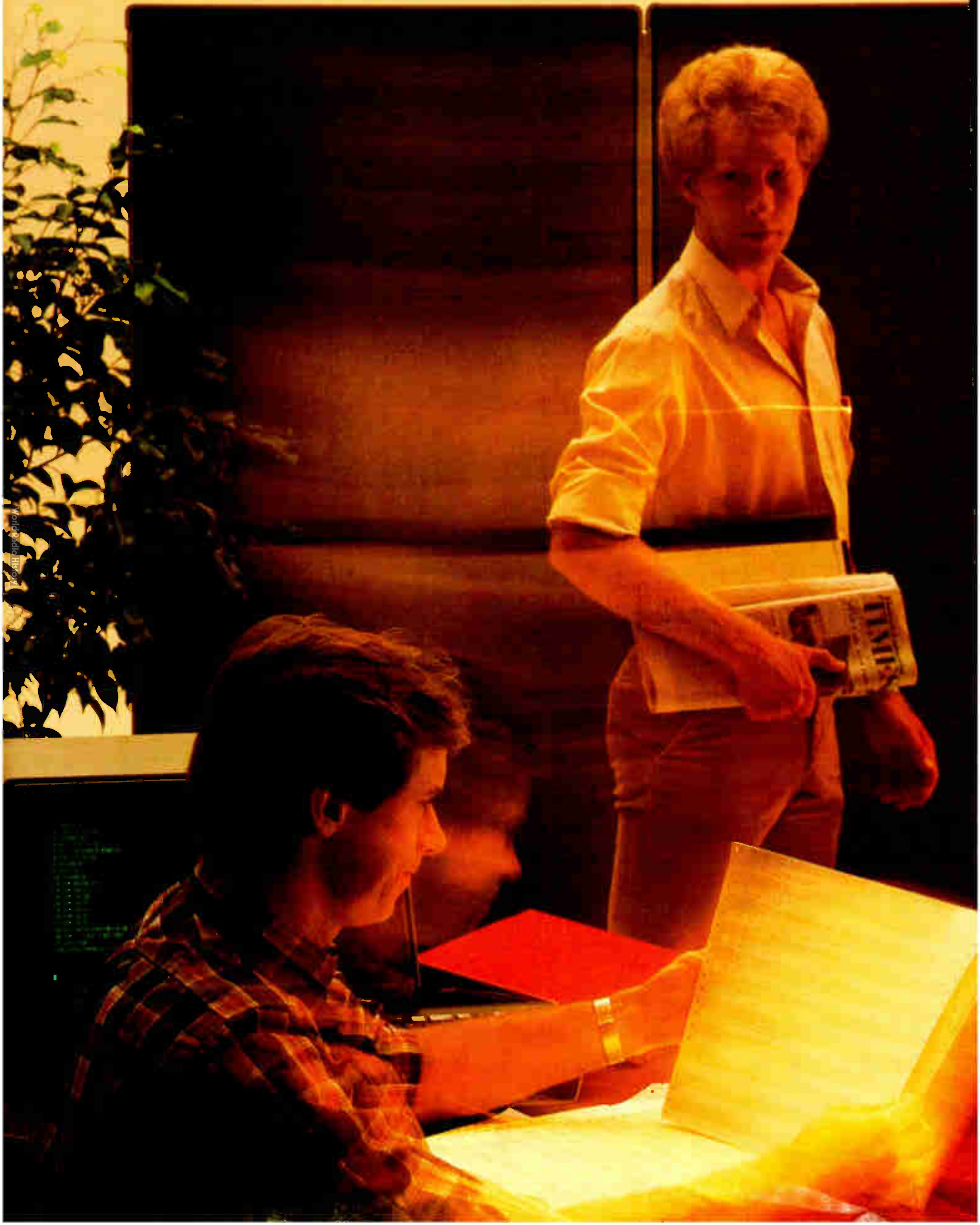

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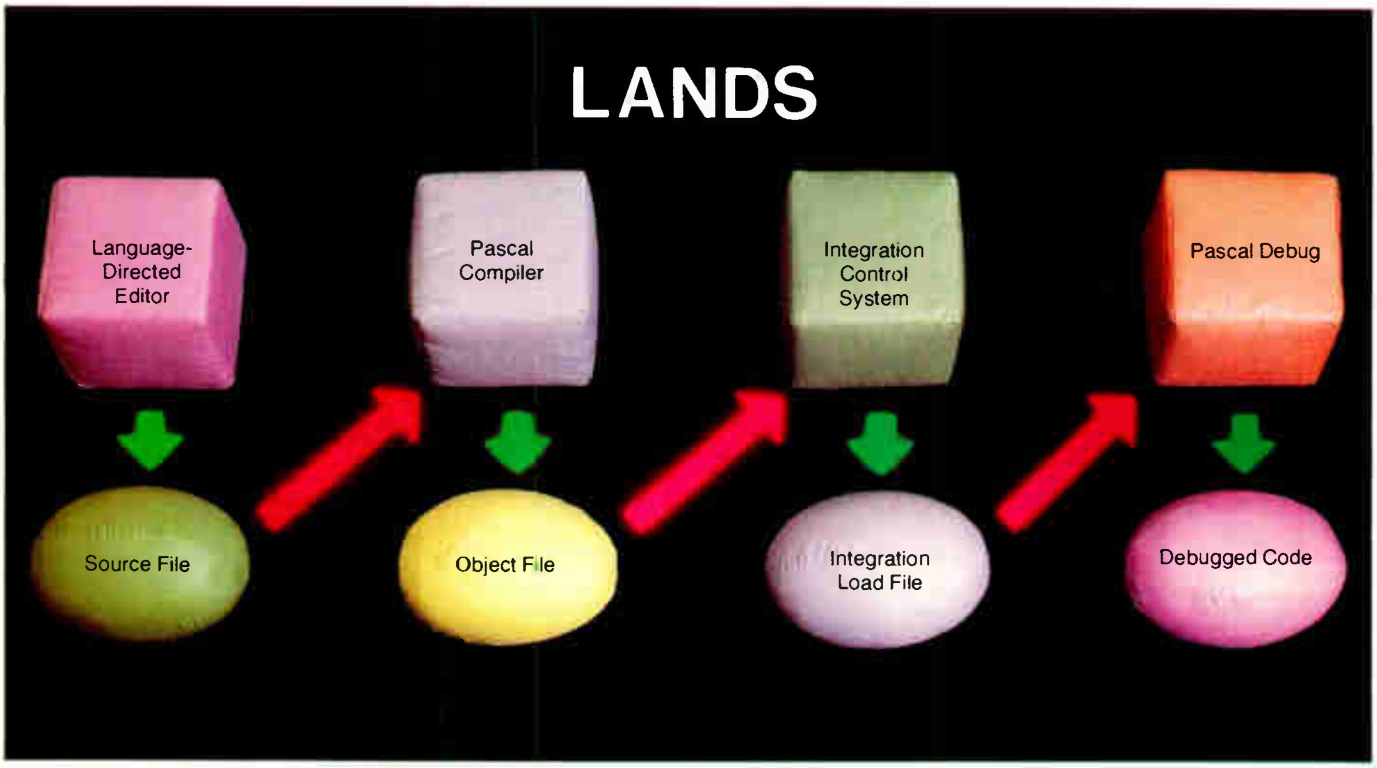

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System inspects board in 2.4 seconds

Two diagonally scanning cameras pick up high-resolution data to check boards carrying chip resistors and capacitors

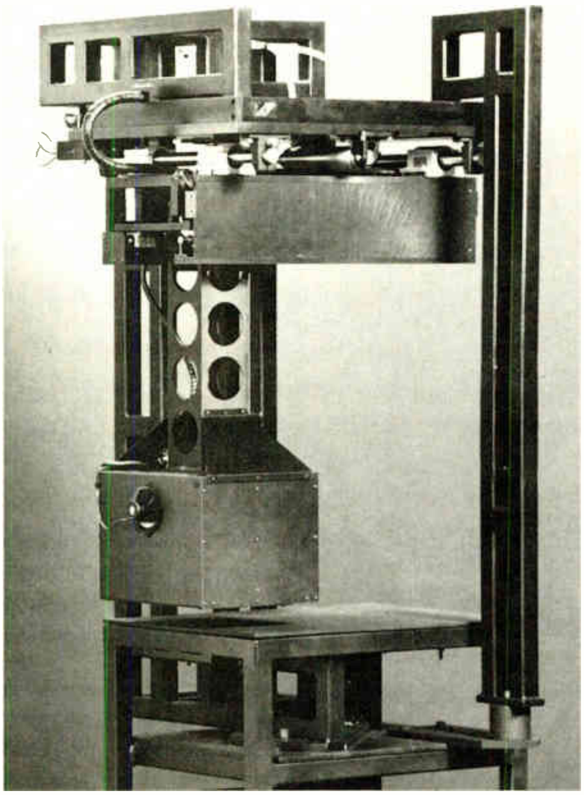
by Stephen W. Fields, San Francisco regional bureau manager

Circuit-board assembly times have been cut by automating the insertion of components and making greater use of surface-mounted devices like chip resistors, capacitors, and transistors. But these same boards still are usually inspected by hand—at rates much lower than those achieved on production lines. Now a system called Teknispec brings automated vision and pattern-recognition technologies to bear on the inspection of stuffed and bare printed-circuit boards.

Teknispec not only works at production-line rates but also cuts the cost of repair by using high-resolution optical-scanning and pattern-recognition techniques to examine the placement and orientation of all axial-leaded components, dual in-line packages, and surface-mounted devices before components are soldered in place.

For axial-leaded components and DIPs, the system checks the boards to verify that leads have been inserted properly in holes and correctly clinched. And Teknispec also ensures that surface-mounted devices are oriented properly with respect to solder pads. When it senses incorrect conditions, it rejects the board and prints out a report detailing the location and the type of problem for rework personnel.

Teknispec comprises a scanning head, an image processor, and a 68000-based microsystem with printer. It owes its speed to an image-processing algorithm implemented in the image processor's hardware. Cynthia Ott, Teknispec's project engineer and a founder of the five-year-old firm, says that "the algorithm was written in Pascal and run on a mainframe. But it took up to a minute for it to check a part's position against a 'mask' that corresponded to the correct position. After we proved the concept we built a special-purpose hard-wired processor that did the same job in 15 μs."



The system uses two cameras, each with a 2,048-element linear charge-coupled-device array. The cameras occupy a head assembly that is physically scanned across the board, at a 45° angle to its edges, looking down on the board from above. "By scanning at 45°," Ott says, "we can look at all four sides of a component with just two cameras."

Computers handle information better in orthogonal coordinates than in angles, so the image processor first eliminates unwanted image information from the corners of the scanned frame. (In a square tilted at a 45° angle within another square, the "blank" information relating to the space around the inside square is not useful.) Then the processor rotates the image 45°, so that the algorithm looks at rectangular data.

Warpage. Ott says that measuring a part's position requires two pieces of information: high-resolution (on the order of 0.1 mm) knowledge of the part's position and a frame of reference for knowing whether or not it is good. "One way to do this," she points out, "is to use an absolute frame of reference on the board, such as a pilot hole. But there are problems with this, the main one being that it requires extremely accurate calibration and can't tolerate any changes in geometry, such as warpage or misregistration on the board greater than the desired accuracy of 0.1 mm.

"However," she adds, "if a position reference next to each component, such as a solder pad, is used, the positional accuracy need only be controlled enough so that two components can't be confused; this is on the order of 0.5 mm, and the component can still be measured to 0.1-mm resolution to the located pad."

To locate that pad and the component, the scanned image is analyzed with a technique Ott calls template matching, which compares a selected portion of an image—a corner of a pad, for example—with an ideal picture, a mask, stored in the computer. "This mask is shifted over the image and the position and correctness of the 'best match' is flagged," she says.

Production rate. Each scan takes about 1.2 s—the rate at which boards move down the assembly line—and there is another 1.2 s of dwell time, the period between boards on the line. With two 2,048-element cameras, the image processor has 2.4 s to process more than 8 million pieces of data and analyze the positions of 250 parts. The image processor can handle data at 16 MHz—8 MHz from each camera. Both cameras "see" a new line at the same time, so a video multiplexer interfacing the cameras with the processor keeps the images separate.

The system can be configured for different assembly lines and for boards of various sizes. One system, the Teknispec-1000, mounts the cameras on a carriage that scans across the line. It can handle boards of up to 12 in. on a side. With the microsystem and the printer, this system sells for $87,000 and is delivered in 150 days. Ott points out that many different configurations are possible.

Formerly known as Teknetron Controls Inc., Integrated Automation specializes in applying pattern-recognition and scanning technologies to a wide variety of industrial problems. The company has applied X-ray, infrared, visible-light, and ultrasonic scanning and pattern recognition to inspection problems as diverse as tires, automobile parts, plastic films, and documents [*Electronics*, May 31, p. 54].

Until recently, Integrated Automation specialized in custom work. Teknispec is its first standard commercial offering.

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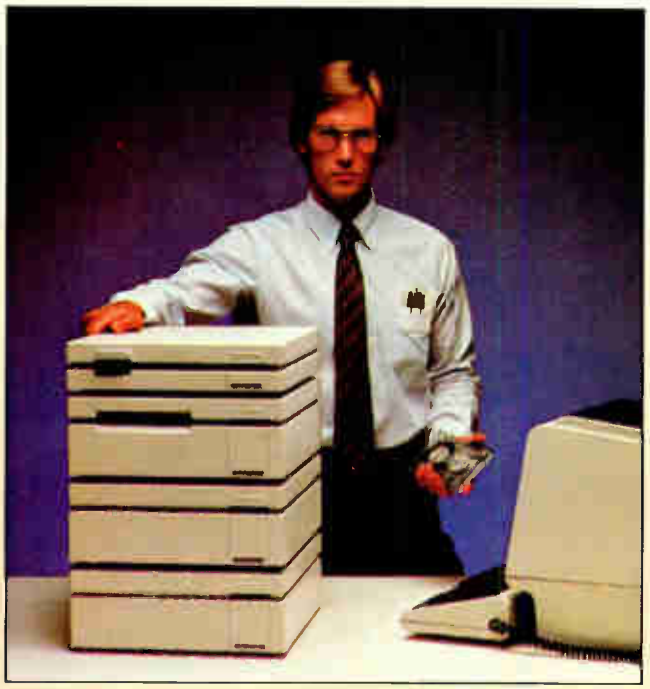

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Circle 169 on reader service card

Microcomputers & systems

DMA controllers support 68000

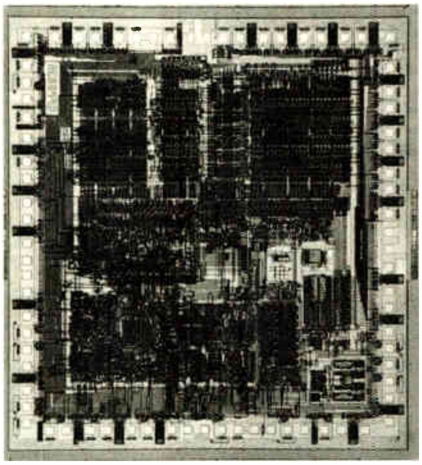
Two-channel chip from Motorola joins single- and four-channel ICs from Signetics and Hitachi

Rounding out a planned trio of direct-memory-access chips that enhance data transfers between peripherals and memory for the 68000 family of microprocessors, Motorola Inc. is taking the wraps off its 68440 two-channel DMA controller, which is pin-for-pin–compatible with a four-channel device introduced earlier by Hitachi Ltd., of Tokyo.

Also this month, Signetics Corp. is ramping up production of its recently introduced 68430 single-channel DMA peripheral, which is software-compatible with Motorola's 68440 and Hitachi's 68450 controllers. A pact covering the entire 68000 family gives all three firms the right to second-source one another's designs.

Motorola's 68440—like Hitachi's 68450—is made from n-channel MOS technology and housed in a 64-pin dual in-line package. The single-channel DMA chip is fabricated from Signetics' bipolar integrated Schottky logic technology and placed in a 48-pin DIP. All three controllers require a single 5-V supply and have been designed to meet the specifications of the 68000 bus by providing arbitration for control and transfer rates of up to 5 Mb/s. All three devices also support cycle-stealing transfer modes and burst modes in which up to 64-K operands can be handled. The three parts' register sets appear identical to system software.

However, the 68440 and 68450 support both single-address and dual-address transfers. The 68430 handles only single-address transferring, which moves data directly between peripherals and memory in one bus cycle. Dual-address transfer allows data movement to occur in two cycles—one, for example, to



read from the peripheral and another to write data to memory. Although the dual-address mode is slower, it is often easier to implement with fewer chips and thus cuts costs, says Robert Beims, a Motorola application engineer for the 68000 family, who is based in Austin, Texas.

Hardwired. Residing on a die measuring less than 250 mils on a side, the 68440 contains 35 registers (17 per channel plus a global register for bus-access allocation), a 32-bit address counter (24 bits are now used, with the rest reserved for the 32-bit version of the 68000), and a 16-bit transfer counter. Unlike the 68450, which is microcode-based, the 68440 has a hardwired architecture, which allows the four-channel controller to configure itself into modes for such operations as link chaining and sequential array chaining. To cut costs and design time, Motorola elected to hardwire the 68440.

In 100-piece orders, the 68440 sells for $45 each in ceramic DIP and $35 in plastic. Samples will be available in September, with initial volume deliveries expected in the fourth quarter. The high-performance n-MOS controller, available at first with a temperature operating range of 0° to +70°C, will come in 8- and 10-MHz versions. Motorola hopes to offer a 12-MHz part soon.

Signetics' single-channel 68430, available at first for 10-MHz operation, costs $34 each in quantities of 1,000 in 48-pin ceramic DIP. Plastic parts, slated for introduction in the final quarter, will cost $31 each. At that time Signetics plans to make a 12.5-MHz device available.

Meanwhile, Hitachi, which started supplying samples of its 68450 in the U. S. and Japan last fall, is to begin volume-production marketing by December. The four-channel DMA chip comes in 4-, 6-, and 8-MHz versions. In lots of 100, the 4- and 6-MHz devices are $102 in ceramic DIPs; 8-MHz chips cost $110 in the U. S.

Motorola Inc., Microprocessor Division, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6226 [371]

Signetics Corp., Microprocessor Applications, Mail Bin 2576, P. O. Box 3409, Sunnyvale, Calif., 94088-3409. Phone (408) 746-2196 [398]

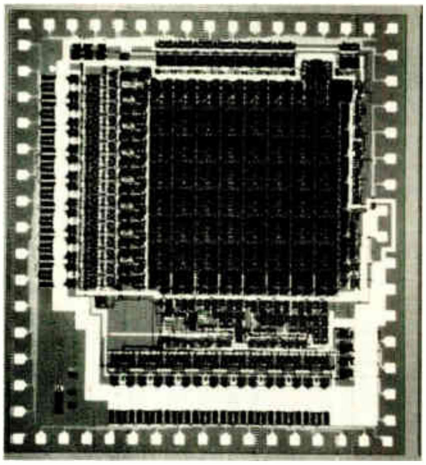
Hitachi America Ltd., 1800 Bering Dr., San Jose, Calif. 95112. Phone (408) 292-6404 [399]

12-bit multiplier bows in C-MOS

Nearly as fast as bipolar competition, 12-by-12-bit digital multiplier runs on 150 mW

Pin-for-pin–compatible replacements for two standard 12-by-12-bit digital multiplier chips exploit the advantages of a complementary-MOS implementation in consuming up to 95% less power than their bipolar counterparts. Analog Devices Inc.'s ADSP-1012 multiplier and ADSP-1009 multiplier-accumulator circuits, compatible with TRW Inc.'s MPY-12HJ and TDC1009J, respectively, use a maximum of 150 mW at a 6-MHz clock rate; by contrast, the TRW parts consume between 2.7 and 3 W, points out John Oxaal, product marketing manager at Analog Devices.

Besides some obvious advantages like eliminating the need for bulky heat sinks and heavy ground lines in digital signal-processing applications, the Analog Devices parts' low power dissipation helps extend device operation over a wider temperature



range, Oxaal adds. The C-MOS parts' military-grade models will run reliably up to the high end of the military temperature range, +125°C ambient. The TRW multipliers only deliver their specified performance up to 125°C case temperature, which translates into 95°C ambient, according to Oxaal.

Takes the heat. For military applications, which make up about half the current $10 million market for digital multipliers [*Electronics*, July 14, p. 155], the Analog Devices parts' extended operating temperatures should be particularly attractive, though the advantage is bought at the cost of some operating speed relative to TRW's products. The ADSP-1009 comes in two military-grade versions, both automatically processed to MIL-STD-883B; the fastest of these has a maximum multiplication and accumulation time of 180 ns, compared with 170 ns for the TRW TDC1009J's military model. Similarly, the faster of two commercial-grade versions of the ADSP-1009 runs at 155 ns, as against 145 ns for its TRW counterpart.

Like the ADSP-1009, the ADSP-1012 has two models each in the commercial temperature range of 0° to +70°C and in the –55°-to-+125°C military range. The fastest commercial and military versions have maximum multiplication speeds of 130 and 150 ns respectively over their full temperature ranges. The faster models of both the ADSP-1012 and -1009 are priced the same as the TRW parts they second-source, Oxaal says. Slower versions geared to less speed-critical applications offer about 80% the speed of their companion models for 30% lower cost.

As with the TRW parts, the ADSP-1012 and -1009 address applications in digital signal processing, including digital filtering, Fourier transformations, and correlations. The ADSP-1009 also handles applications in image processing and matrix manipulations. Both models are available in either 64-pin hermetically sealed ceramic dual in-line packages, 68-pin pin-grid arrays, or 68-terminal leadless chip-carriers. They operate using a single +5-V power supply.

The high-speed commercial versions of the ADSP-1012 and -1009 in lots of 100 cost $115 and $135, respectively, and are available from stock. In their fastest military-grade versions, the ADSP-1012 costs $300 and the ADSP-1009 multiplier-accumulator is priced at $340.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [372]

$500 board lets users evaluate the T11 single-chip PDP-11

For only $500, the T11 evaluation module (TEM), a single-board microcomputer built around the T11 16-bit PDP-11 microprocessor chip, provides a way of evaluating the chip's performance and uses. Compatible with the PDP-11 microcomputer line, TEM can also be used as a low-cost development prototyping system for T11-based designs or as a PDP-11 assembly-language trainer.

TEM is a fully assembled microcomputer unit ready to operate when connected to an external power supply. It contains a T11 microprocessor, up to 8-K bytes of random-access memory, 16-K bytes of erasable programmable read-only memory, an on-board octal keypad, and two rows (six digits each) of light-emitting-diode displays.

Two serial ports, an 8-bit parallel port, and a 60-pin connector permit users to connect external equipment to the board and to access its data paths. The E-PROM carries software, including a keypad monitor, a console monitor with a Macro-11 assembler, and diagnostics.

Delivery takes about 30 days. In quantities of one, TEM costs $475, and discounts are available on quantity orders.

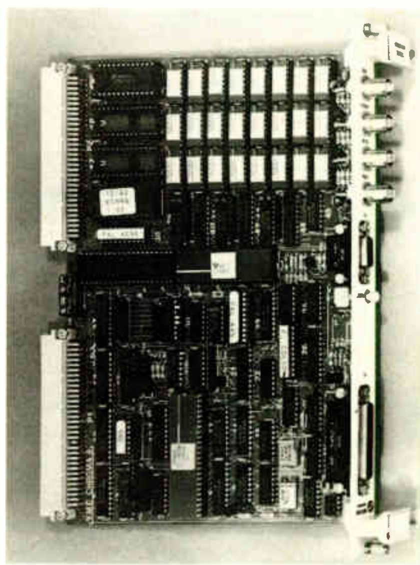
Digital Equipment Corp., 129 Parker St., Maynard, Mass. 01754 [373]

Eight-color video processor resides on VME board

A video-display processor board built around two processors—a 9367 graphics display processor and a 68121 intelligent peripheral controller—provides the capabilties for vector and point plotting; ASCII alphanumeric character display; and circle, disk, and ring figure generation. An eight-color, 512-by-512–picture-element board, the DSSE512CHROMA8-1 is designed for use on the VME bus.

The board has 192-K bytes of image memory divided into two screen pages of three planes each. Communication, at bit rates of 1,200, 2,400, 4,800, or 9,600 b/s, takes place through the VME bus, with the dual-ported RAM of the 68121, or through an RS-232-C line. A parallel interface for a keyboard or printer is available, too.

The video-display processor is delivered with firmware stored in a



2764 erasable programmable read-only memory and with a 2-K RAM for the monitor's memory needs. Two 28-pin sockets for RAMs or E-PROMs are available for user memory. Priced at $2,850, the board is available four weeks from receipt of order. A version built for the Motorola EXORciser bus costs $2,500.

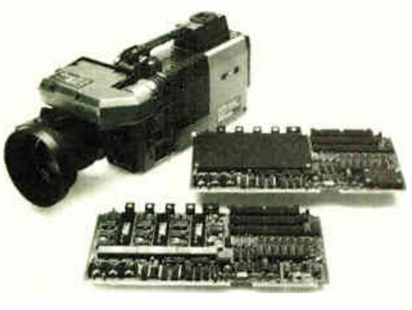
Data-Sud Systems/U. S. Inc., 2219 S. 49th St., Suite J, Tempe, Ariz. 85282. Phone (602) 966-3953 [374]

RGB digitizer does 3 channels in a fraction of a second

The RGB-512 single-board red-green-blue (RGB) video digitizer, which enhances the real-time color-processing capability of Imaging Technology's IP-512 modular image processors, can capture three channels of decoded RGB video images in 1/30 of a second. Three flash analog-to-digital converters digitize each signal at a 5- or 10-MHz rate to 6 or 8 bits of accuracy. The digitizer is offered in Multibus and Q-bus versions.

Three independent RGB 8-bit digital-to-analog converters, each with a 12-by-8-bit programmable look-up table, reconstruct digitized data back to full color, 24-bit-wide RGB video signals. Four bits of graphics overlays are provided for each channel.

Three companion FB-512 frame buffers store the digitized RGB picture-element data for processing by the host's central processing unit. The RGB-512 is suitable for colorimetry analysis, color teleconferencing, general image processing, and computer graphics. Available six to eight weeks from receipt of order, the digitizer sells for $7,495.



Imaging Technology Inc., 400 West Cummings Pk., Suite 4350, Woburn, Mass. 01801. Phone (617) 938-8444 [375]

Z80B-based CPU for 180+ line carries 128-K bytes of RAM

Xycom's 180+ microcomputer product line, which provides data acquisition, process control, and communications in harsh industrial settings, has been enhanced with a Z80B-based CPU board three times as fast as existing 180+ CPU boards. The 1864+, which can operate in humidity as high as 95% and temperatures ranging from 0° to 65°C, is equipped with 128-K bytes of dynamic RAM plus sockets that can hold 112-K bytes of nonvolatile memory.

The 1864+ also incorporates a serial input/output unit with two serial communications channels, a four-channel counter-timer circuit, and a battery-backed real-time clock. An optional arithmetic processor unit has 43 instructions and can perform 16- and 32-bit fixed and 32-bit floating-point arithmetic, as well as floating-point trigonometric functions. An optional floating-point processor unit contains 14 instructions and can perform 32- and 64-bit floating-point arithmetic.

Available in 30 days, the 1864+ sells for $1,700. Either optional processor board adds $240.

Xycom Inc., 750 N. Maple Rd., Sline, Mich. 48176. Phone (313) 429-4971 [377]

Multiuser system offers wide choice of software, peripherals

"Have it your way" could be the slogan of Rianda Electronics, whose Caribe line of multiuser microcomputers offers a choice among two operating systems, Blis/Cobol and Bits/Basic; the five programming languages of Basic, Cobol, Forth, Fortran, and Pascal; and a slate of peripherals from more than 60 different manufacturers.

Caribe's CPU board is designed around the Fairchild 9445 microprocessor, a 16-bit chip that is clocked at 16 MHz.

Caribe's five standard configurations offer 20, 30, or 50 megabytes of Winchester-disk storage and appropriate streaming tape backup. A typical five-user configuration—20 megabytes of Winchester disk storage, 6 megabytes of tape backup, and an operating system—might cost about $10,000. One-user operating systems cost $750, and four-user versions, typically, about $1,500. Shipments are scheduled to begin next month.

Rianda Electronics, 2535 Via Palma, Anaheim, Calif. 92801. Phone (714) 995-6552 [376]

Dual-port 68000-based board uses SUN architecture

The PM68D dual-port 68000-based single-board microcomputer, a redesign of the traditional Stanford University Network (SUN) architecture, incorporates changes requested by original-equipment manufacturers who used the first Multibus version. What's more, the PM68D can use the 68010 and support its demand paging and virtual memory.

Dual-ported RAM and memory management support up to 8 megabytes of on-board memory and 16 megabytes of Multibus memory. The microsystem's improvements on the basic SUN board include interrupt-handling facilities, dual-port memory, hardware-generated refresh, serial input/output, and parallel I/O.

The manufacturer provides a 16-bit programmable parallel I/O port, which can be used to drive the Shugart Associates Standard Interface (SASI) or the Centronics interface, as well as two serial ports with modem control signals for RS-232-C–, RS-423–, and RS-422–compatible lines. The computer runs under Unix and supports C, Fortran, Basic, and Pascal. Prices start at $2,590 each, and delivery takes four weeks.

Pacific Microcomputers Inc., 119 Aberdeen Dr., Suite 7, Cardiff-by-the-Sea, Calif. 92007. Phone (619) 436-8649 [378]

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*February 16, 1981. **Suggested U.S. list price. PG02322 214K

Instruments

Apple develops code for 68000

Plug-in card, software let Apple act as development station for 68000 assembly-language work

An add-on board and software package for three versions of the Apple II computer enable the microsystem to write and execute programs for the 68000 microprocessor. From Qwerty Inc., the $695 QPAK-68 system is the first of a series of microcomputer products intended for engineers, programmers, and students who want to develop programs the low-cost way, with a personal computer.

The board employs a 68008, the version of the 68000 with 8-bit data input/output. It may be plugged into any open slot on the Apple II, II+, or IIe, sharing the memory and I/O facilities of the computer, including the screen display. The QPAK processor may be started, stopped, and interrupted from the Apple keyboard. When executing, the 68008 processor runs simultaneously with the computer's 6502 processor, permitting 1-MHz operation. With its own local memory, the 68008 runs at 7 MHz.

The board carries 16-K (expandable to 32-K) bytes of erasable programmable read-only memory containing a monitor-debugger and 2-K (expandable to 8-K) bytes of random-access memory. The 68008 can access 64-K bytes of the Apple's RAM.

A 50-pin expansion connector atop the unit provides for future peripheral use and expansion of local memory—for example, RAM boards that can hold 1 megabyte are planned for introduction next year. Light-emitting diodes indicate whether the processor is running and whether it is in supervisory or user mode.

Assemble from RAM. Software on the diskette includes a line-oriented editor and macroassembler and is capable of editing and assembling programs directly from RAM at high speed or, alternatively, from the disk. With the board and diskette come two 68000 texts and a user guide.

Since the package is primarily intended for low-end development of assembly-language software, an emulation feature is not currently required, says Ron Baldridge, marketing director for the firm, but this too may be offered later. The program under development runs somewhat more slowly on the 68008 processor than it will on the target system, but it allows logic errors to be detected. For full-speed debugging on the target system, a logic analyzer may be employed, Baldridge points out.

Programs may be transported to target machines by several methods. The preferred way, says Baldridge, is to burn the code into a PROM using one of the plug-in PROM-programming boards available for the Apple. If compatible disk drives and system software are available for the Apple and the target system, disks may be used for program transfer.

The only present alternatives to the Qwerty package are full development systems, costing from $10,000, according to Baldridge. Many of these have inadequate RAM for realistic program development, he says.

Qwerty Inc., 9252 Chesapeake Dr., Suite 600, San Diego, Calif. 92123. Phone (619) 569-5283 [351]

Meter measures laser pulses

Unit detects pulse-to-pulse variations in laser output at up to 100 pulses/s

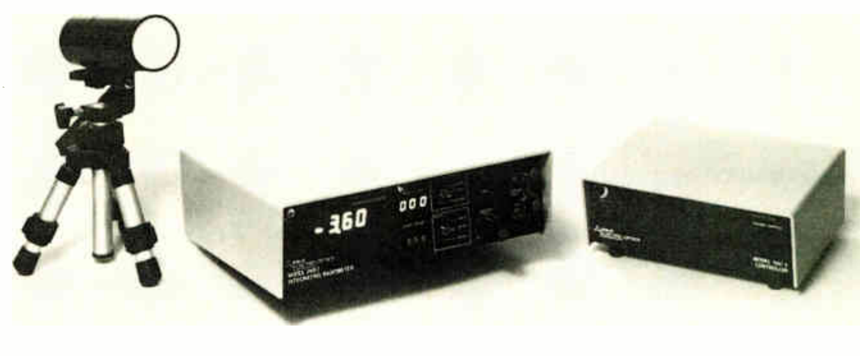
A newly developed laser energy meter allows measurement of pulse-to-pulse variations in lasers operating at up to 100 pulses/s. For tunable dye lasers, laser-based military range finders, and laser target designators, such measurements offer more reliable characterization of operating stability than do the averaging methods generally used. Readings are accurate to within 3%.

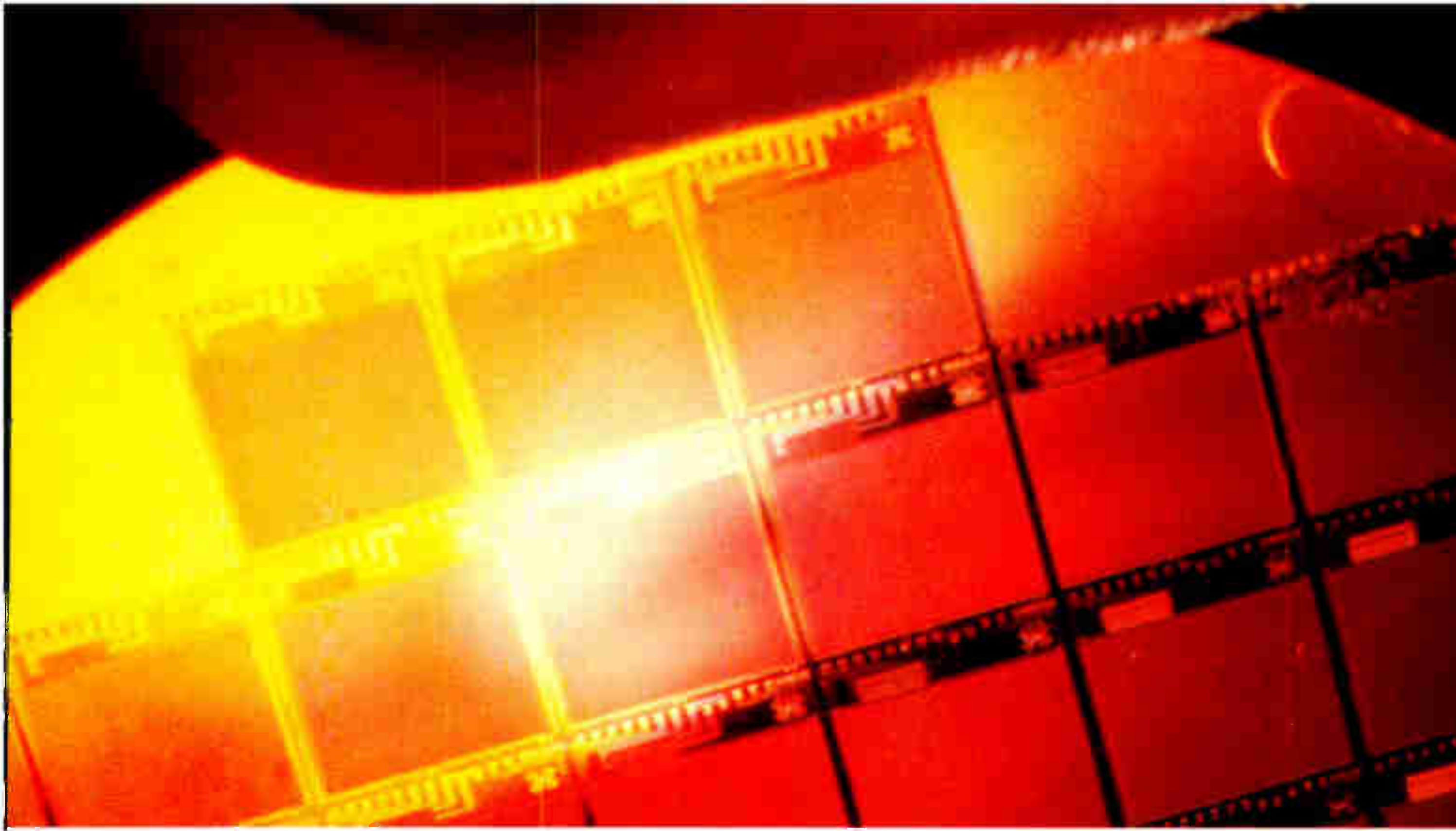
The model 360 from EG&G Electro Optics consists of a detector head, a measurement-display unit, and a temperature-control and power-supply unit, which stabilizes the detector at 30°C to maintain calibration. The detector head is composed of two silicon photodiodes and an attenuator, which reduces energy by a factor of 100,000 and diffuses the beam in order to assure uniform energy distribution.

Width check. One photodiode output goes to the meter. For users who want to track pulse width, a connector at the back of the detector head allows the other photodiode's output to be viewed on an oscilloscope.

The user manually adjusts the unit to synchronize with a specified laser pulse rate. Once adjusted, an internal synchronization clock resets and holds circuits to zero after each successive pulse. Readout is in nanocoulombs and software is provided for conversion to millijoules.

The reason the unit puts out charge readings instead of energy data directly is that the detector's sensitivity varies with the wavelength





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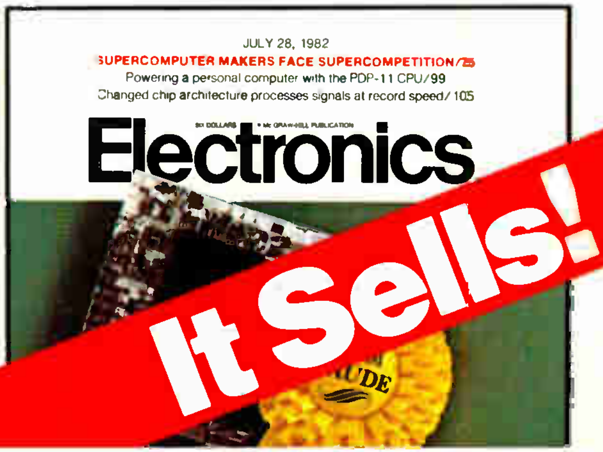


of the laser light. The software, which runs on HP 85 and other desktop microsystems, requires input of the wavelength and the charge reading to produce the energy figure.

The energy-detection range for the 360 is 0.1 to 200 mJ, and its spectral range is 350 to 1,100 nm. Other detector heads are available for alternative energy ranges.

The model 360 is priced at approximately $6,000. Delivery is four to six weeks after receipt of order.

EG&G Electro-Optics, 35 Congress St., Salem, Mass. 01970. Phone (617) 745-3200 [352]

Instrument uses stored charge to find a diode's turn-off time

The QS-83 stored-charge meter, which can replace recovery-time measuring equipment, determines the turn-off times of diodes and rectifiers without oscilloscopes, external pulse generators, or bias supplies. By measuring the difference between two bias conditions—leakage currents, diode capacitances, and jig capacitances are canceled—it calculates the

minority-carrier storage.

The QS-83 handles power rectifiers, power MOS FET integral rectifiers, the fast-recovery rectifiers found in switching-mode power supplies, and other parts with recovery times that range from 20 ns up to microseconds. Its stored-charge measurement ranges can be set at 3, 10, 30, 100, 300, and 1,000 nC, and its current range at either 10 or 100 mA. The instrument's pulse-repetition rate is listed at 10 kHz, and its pulse amplitude at 6 V.

Available in two to four weeks, the QS-83 sells for $1,050.

Bermar Corp., 6300 Westgate Rd., Raleigh, N. C. 27612. Phone (919) 821-5993 [353]

Microsystem plays host to a 16-channel logic analyzer

Built around a popular CP/M-based personal computer, the Omni II is an easy-to-use menu-driven timing and state logic analyzer that costs only $3,950. The portable instrument can collect 1,000 data samples on each of 16 channels or, optionally, up to 330 samples on 48 channels. It provides four channels of glitch detection, with a minimum detectable pulse of 10 ns.

The system uses internal or external clocks as fast as 20 MHz. Its triggering modes include the basic AND, OR, and NOT on data or glitch, with the trigger point positioned within the 1,000-word sample memory. After data collection, the Omni II performs timing analysis, displaying a standard timing diagram (a simultaneous view of 16 channels) and an edge waveform (a compressed timing diagram that permits an easy transition identification).

To analyze software, the Omni II becomes a state-analysis machine. Its state displays include a numeric dump, similar to a computer memory dump with the radix user-specified; instruction disassembly, with the data from microprocessors shown as instruction mnemonics; eight-channel matrix, logic-level occurrences shown in matrix format; and histograms, which show the system's time-interval distribution.

Available now, the Omni II comes with word-processing and spreadsheet software and with a high-level programming language.

OmniLogic Inc., P. O. Box 87, Renton, Wash. 98057. Phone (800) 228-6664 [354]

Hard-disk drive tester supplies power to drive under test

A tester for 5¼-in. Winchester-disk drives automatically performs both preprogrammed and linkable acceptance tests and also provides an output signal to a parallel printer. The microprocessor-controlled DX525-

AT, which includes the disk-drive power supply, can be nested in arrays of up to eight testers for testing multiple drives.

The DX525AT runs such performance tests as interface status, measurements of revolutions/min, format, window margin, flaw-map generation, and error rate. Operator prompts make the tester easy to use, and its simple control panel has only six control switches, a 16-switch keypad, an 8-digit display, an on-off switch, and six test points.

An internal disk-drive power supply, independent of the tester supply, is automatically energized at the start of a test sequence and de-energized at the end. With cables and power supply, the DX525AT costs $4,500 and is available now.

Applied Memory Technology, 2822 Walnut Ave., Tustin, Calif. 92680. Phone (714) 838-1860 [355]

Low-cost 1-GHz counter links to HP Interface Loop

The HP 5384A and 5385A frequency counters, for use in research and development and testing, have input sensitivity of 10 mV (root mean square) and extensive input-signal conditioning. Their frequency ranges extend from 10 Hz to 225 MHz and 10 Hz to 1 GHz, respectively.

Both models have measurement resolution of at least nine digits/s, a selectable four-to-eleven-digit display resolution, and three gate time selections (0.1, 1.0, and 10 s). Their signal conditioning includes automatic or manual attenuation, automatic or manual trigger-level control, and low-pass filtering. The IEEE-488 bus interface is standard, and one for the Hewlett-Packard Interface Loop is optional.

The counters' packaging design allows them to be mounted in a rack, used on a laboratory bench, or carried into the field. In the field, an oven time base gives the counters a laboratory level of accuracy, and there is an optional battery pack.

Available four weeks from receipt of order, the 5384A sells for $1,400, and the 5385A for $1,700.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [356]

Controller boasts graphics and touch-sensitive screen

Dot-addressable graphics and a touch-sensitive screen set off the 1722A instrument controller, compatible with Fluke's four-year-old 1720A. The 1722A has an 80-character-by-16-line screen with a 640-by-224 picture-element resolution, a 136-K-byte memory, a 400-K-byte floppy-disk drive, and RS-232-C and IEEE-488 interfaces.

The 1722A's standard language is a Basic interpreter with more than 25 extensions for IEEE-488-compatible instrumentation control; a Basic compiler, Fortran, and an assembly language are optional. Once a system has been programmed, the operator can run it directly from the controller's touch-sensitive display.

Random-access-memory expansion modules can enlarge the controller's standard memory to more than 2.6 megabytes. Some of this memory can function as an electronic disk and thus speed up execution. Another option offered by the company is magnetic-bubble memory, in 256-K- or 512-K-byte increments up to a maximum capacity of 1.3 megabytes.

With its 5°-to-40°C temperature range, the controller can be used in factories. Available immediately, the 1722A, including Basic interpreter, sells for $7,450.

John Fluke Manufacturing Co., P. O. Box C9090, Everett, Wash. 98206. Phone (206) 342-6300 [357]

Industrial

Plug-in cards adapt system

Line of 18 cards suits computer to practical tasks of controlling industrial equipment, processes

Although new computers, especially microprocessor-based systems, are crawling from every crack in the woodwork, only a small fraction of them are in any way suited to the practical tasks of monitoring and controlling industrial processes and equipment. To exploit what it sees as a product niche of high potential, a new firm, Industrial Computer Designs, has developed a microsystem whose adaptable bus structure will support a growing line of compact plug-in boards, now numbering 18.

Called the Vantage Point Computer, the microsystem is aimed not only at the original-equipment manufacturer and system packager, but also at engineers and hobbyists. Says Michael V. Ragsdale, founder and president of the firm, "This is an entirely new category of product. It is based on our own bus structure and different building-block cards that plug into it. They represent an effective set of tools for knowledgeable persons to build powerful computer systems." The cards, adapted to the firm's own bus, were designed initially for the S-100 bus and have been used in hundreds of applications custom-tailored by the firm, according to Ragsdale.

At the heart of the Vantage Point Computer is the Mother Board Bus, which has four slots for three basic cards: the ZPM-8 Z8OA processor, memory, and input/output card operating at 4 MHz; serial input/output and calendar clock; and 64-K-byte random-access memory. The bus cards are based on a 64-pin connector, with 40 pins for data, address, and control-signal lines. The remaining 24 pins are undefined; larger systems might use them for multiprocessor communication. The cards measure 3.6 by 5.4 in.

The microprocessor board has a selectable jump to a 16-K erasable programmable read-only memory containing a system monitor with test routines and upper-level functions that can free other software from many tasks, according to the company. Also on the card is a 16-K static RAM and sockets for an additional 32-K of E-PROM or RAM. An on-board programmable I/O chip provides three 8-bit parallel ports that can be individually configured to monitor switches or other functions, or for relay-control output.

Serial I/O is performed by the calendar card, with three RS-232-C channels for communication with a terminal, printer, modem or other peripheral devices. The clock generates interrupts to the processor in 1-s increments. Supplemental memory is available with other cards, both in E-PROM and RAM 64- and 128-K-byte versions. Slave memory may be added to total more than 1 megabyte of system capacity, says the company.

Real world. Other Vantage Point cards can be added, in a 12-slot expanded motherboard, to make a stand-alone computer, complete with peripherals including a high-resolution DT100 80-character-by-25-line terminal and separate numeric keypads. The total equipment offering extends to "controllers and monitoring devices to allow direct connection with the real world," Ragsdale says. Among them are sensors, valves, and switches that regulate temperature, moisture, voltage, current, position, and pressure.

Pricing on the line is based on individual cards, all now available. The combination of the basic three cards and motherboard runs about $950. A complete Vantage Point computer $6,500 for all cards and terminal, a figure that Ragsdale claims allows a typical industrial energy-management system to be built for half the price of existing equipment. A proprietary form of Basic is used.

Ragsdale's company arrived at building standard computers from a different direction than most start-up firms. "Instead of developing products and knocking on doors, we found vertical markets to sell our ideas to and then did the job for them," he says. From such custom tasks, standard lines evolved.

Other manufacturers already are planning to build cards compatible with the firm's bus, largely because it uses only off-the-shelf components, according to Ragsdale. A network of 18 representatives has been signed up to sell to industrial customers.

Industrial Computer Designs, 31121 Via Colinas, No. 1005, Westlake Village, Calif., 91362. Phone (213) 889-3179 [391]

Sensor reads directly in °C

IC temperature sensor does away with need to convert readings from kelvins to degrees Celsius

The LM35 series of precision integreted-circuit temperature sensors from National Semiconductor Corp. have output voltages that are linearly proportional to the centigrade temperature scale. The ICs are a major improvement over conventional temperature sensors, calibrated in kelvins, for the user does not have to subtract a constant voltage from the sensor's output to get the more convenient centigrade reading.

The LM35 employs trimming and calibration during the wafer test, so it yields typical accuracies of ±¼°C at room temperature and ±¾°C from −55° to +150°C. Since it does not itself generate much heat, its stability is within 0.1°C in free air.

On surface. Like other IC temperature sensors, if glued or cemented to a surface it will read within 0.01°C of a surface temperature. Typical applications include process control, laboratory ovens, and such appliances as washing machines and ovens.

Interfacing the device with readout or control circuitry is simplified by the LM35's low output impedance,

0.1 Ω at 2 mA, and by its linear output, 10 mV/°C. It can be used with single or dual power supplies ranging from 4 to 30 V, and it draws less than 60 μA.

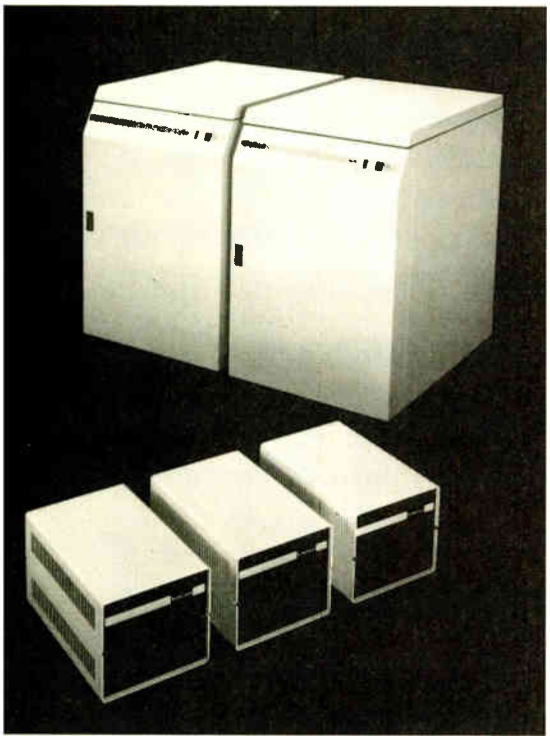
The series includes the LM35, rated from −55° to +150°C; the LM35C, from −40° to +110°C; and the LM35D, from 0° to 100°C. All come in three-lead TO-46 cans, and the LM35C is also offered in a three-lead TO-92 plastic package.

All units in the series cost $1.53 each in quantities of 100. Samples are available now, and production delivery will start in September.

National Semiconductor Corp. 2900 Semiconductor Dr., Santa Clara Calif. 95051. Phone (408) 721-5000 [382]

Power conditioners neutralize 6,000-V spikes, cut noise

Five power-conditioning systems that combine the functions of a power regulator, an isolator, and a filter can safeguard computer equipment and data from damage caused by electrical power irregularities. Depending on the model, the systems are rated to supply computers with ac output of 120, 208, or 240 V (±5%), and their input can range from 35% below to 15% above these voltages.



The systems neutralize voltage spikes up to 6,000 V lasting ½ μs. They also eliminate current-transmitted irregularities—transients or noise. Noise rejection is rated at 120 dB for common-mode and 60 dB for transverse mode.

Prices start at $595 for a 1-kVA model suited to typical desktop computers. The other systems, which protect larger computers, cost $995 (2 kVA), $1,595 (3 kVA), $2,650 (5 kVA), and $3,150 (7.5 kVA). Quantity discounts can be had for two or more units of any model. Delivery of the 1-, 2-, and 3-kVA models takes five days; the other models are shipped within 90 days.

Data General, Field Engineering Division, 50 Maple St., Milford, Mass. 01757. Phone (617) 478-4000 [383]

Controller and matching motor control air, fluid flow efficiently

The V*S variable-torque ac drives—which provide the basic functions of start, stop, and speed control—use 34% less energy than the valves, outlet dampers, inlet guides, vanes, and slip devices commonly used to control the flow of air and other fluids. All drives in this line come as a package comprising a controller and the firm's XE energy-efficient motor.

To match a broad range of pumping and variable-air-volume requirements, the drives in the V*S line are rated from 1½ to 500 hp. They can be used in new construction or retrofitted into existing applications.

The drives combine a 460-to-575-V capability with the simplicity, reliability, and the lower costs of high-power transistor designs. The transistors have redundant protection against short circuits, and each drive's components are temperature-cycled to design limits. All complete controllers are tested at full load.

To install the drives, users just connect the controller to the utility power, the output to a motor, and the speed-setting signal to the controller. A typical 40-hp motor and controller lists for $8,500, and most sizes are available from stock.

Reliance Electric Co., Electrical Drives Group, 24703 Euclid Ave., Cleveland, Ohio 44117. Phone (216) 266-2647 [388]

Forth-like language gives controllers real-time abilities

Sphere—a Forth-derived multitasking, real-time programming language—makes Fac Pac series M programmable controllers suitable for real-time industrial control. Built around an 8-bit 6809 microprocessor, the series M provides 32 input/output channels, expandable to 192 through 12 16-bit parallel ports with handshake control; 20-K bytes of main memory, expandable to 40-K bytes; and an RS-232-C or RS-422 communications channel, which operates at 50 to 9,600 baud.

Sphere offers multitasking support for an unlimited number of tasks. It has dynamic, preemptive, and event-driven scheduling; a screen-oriented editor; and drivers both for Datricon's ROM-12 programmers for erasable programmable read-only memories and for STD-bus peripheral boards. Its enhancements are built on more conventional Forth-type features, including built-in assemblers for speed-critical, stack-oriented operation for minimal run-time random-access memory, and user-definable interrupt handlers. Application programs are stored in ROMs, eliminating the need for disk drives.

Prices start at $1,750, and orders are filled from stock.

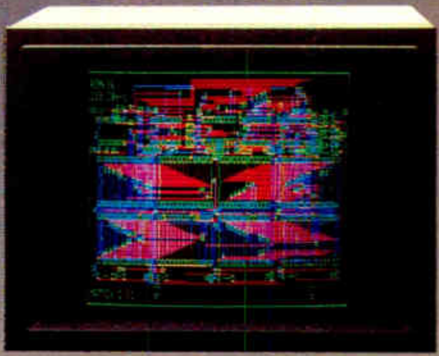
Datricon Corp., Datricon Pl., 155 B Ave., Lake Oswego, Ore. 97034. Phone (503) 636-7671 [384]

Solid-state air-flow transducers put out 5-V dc signal

An all-solid-state air-flow transducer with linear dc outputs of 0 to 5 V can suit measurement applications in electronic cooling, high-voltage ac energy management, fume hoods,

COLOR GRAPHICS BOARDS

1024 X 1024



DISPLAY RESOLUTION: 1024 x 768 pixels non-interlaced at 60Hz or up to 1600 x 1200 pixels interlaced at 30Hz

READ/WRITE AREA: 1024 x 1024 x 4 bits/pixel expandable to 1024 x 1024 x 16 or 2048 x 2048 x 4

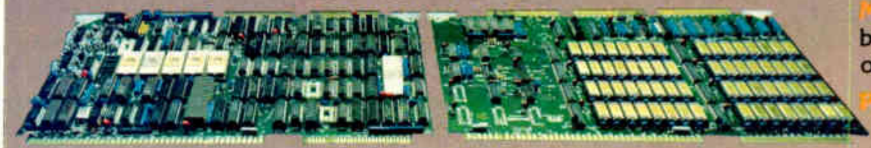
SPEED: Four on-board processors draw graphics primitives at 50 to 800 nsec/pixel

COLOR: 16 display colors from a palette of 256

SOFTWARE: On-board 16 bit CPU with resident graphics software interprets over 256 commands

MODULARITY: GXB-1000 is fully Multibus compatible (IEEE-796), and requires only + 5V

PRICE: $3225.00 complete*



MATROX GXB-1000 - The complete color graphics solution.

The GXB-1000 is a complete color graphics display system implemented on two Multibus boards. The system executes a display file containing high level graphics commands, generated by the user's host CPU. The GXB-1000 includes all the necessary hardware and software to draw lines, polygons, circles, characters, etc.

The unmatched performance and low cost of GXB-1000 make it the perfect solution for OEM color graphic displays. Additionally, Matrox can provide RGB monitors, CPU boards, memory boards, cardcages and keyboards for complete display system requirements.

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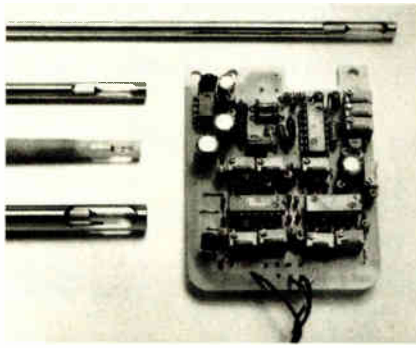


clean-air rooms, biomedical products, and process control.

The 435DC—traceable to the National Bureau of Standards—operates on 12 to 15 V dc and can be ranged to 15,000 standard ft/min. Probe lengths range from 2½ in. to more than 48 in. For interfacing with a computer's programmable controller, data logger, and recorder, the transducer has a linear 0-to-5-V dc output.

The 435DC series automatically corrects itself for temperature and pressure changes and is easily inserted—with no pressure-drop penalty—into ducts and pipes for air and gas mass-flow measurements. Available from stock in a bare-bones configuration for original-equipment manufacturers, the transducer costs $725.

Kurz Instruments Inc., P. O. Box 849, Carmel Valley, Calif. 93924. Phone (800) 424-7356 [386]

Programmable air-flow monitor scans up to 20 cables/s

The CSI 370, a solid-state electronic air-flow monitor, is programmable through a touch-sensitive keypad. Available in two models—a 10- and a 20-cable version—the monitor scans 20 cables/min and has a flow-rate resolution of 0.01 standard ft^3/h and 0.5 natural liters/h. Continuous scanning helps reduce cable losses.

The 370's flow-rate measurements range from 0.0 to 9.99 SCFH and from 0.0 to 280 NLPH, and their flow volumes are totalized in a range of 0 to 99,999 standard ft^3 or natural kiloliters. Only 8 in. high, the air-flow monitor can be mounted in a 19- or 23-in. rack. The 8370 costs less than $100 per cable and will be available in early October.

Chatlos Systems Inc., 125 Algonquin Pkwy., Whippany, N. J. 07981. Phone (201) 887-1456 [387]

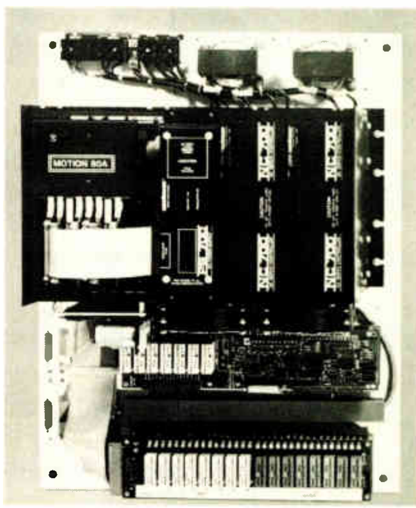
Compact motion controller has RS-232-C link

The Motion 80A programmable motion controller, an improved version of the Motion 80, has a new compact package design with integral power supply and servoamplifiers, as well as an electronics chassis, a motor, and a transformer. It can communicate with a supervisory process controller through an RS-232-C interface and is therefore useful in distributed process-control configurations for factory automation.

The Motion 80A permits users to program speed, position, acceleration, deceleration, and dwell time, among other things, and its closed-loop control prevents overshooting and promotes high-speed positioning with precise stopping position.

Mocol, an English-like programming language the company developed, allows the Motion 80A's users to program complex actions easily, by compiling various levels of acceleration, deceleration, and speeds in one move. Available now, the Motion 80A averages $5,000 per axis.

Contraves, Motion Control Division, 632 Fort Duquesne Blvd., Pittsburgh, Pa. 15222. Phone (412) 261-8600 [385]



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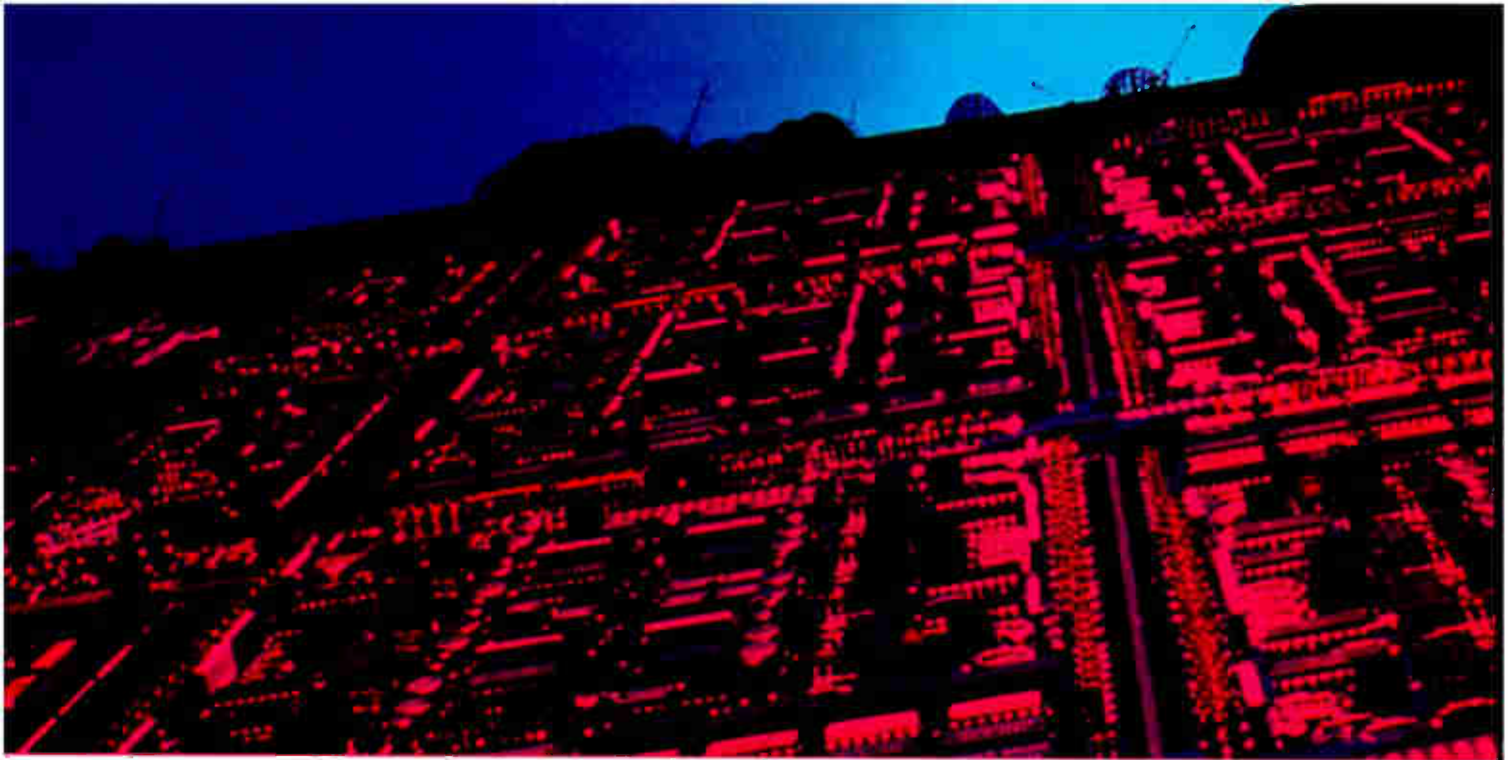

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Communications

Radio links get one-chip modem

1,200-baud full-duplex modem IC made in C-MOS meets standard for radio data transmission

Several single-chip modems exist for transmitting data over telephone lines, but this is not the case when it comes to radio links. So a specialist designer of large-scale integrated circuits, Consumer Microcircuits Ltd., is plugging the gap with a single-chip complementary-MOS modem that operates at 1,200 baud in the full-duplex mode.

In the FX409, fast frequency-shift keying (FFSK) is used to transmit data with logic levels represented by 1,200- and 1,800-Hz phase-continuous tones: the transition between tones occurs only at the zero-crossing point of the sine wave. Thus 1 cycle at 1,200 Hz and 1½ cycles at 1,800 Hz are used for each bit. These characteristics are used to meet the standard for radio data communication drawn up by the UK Electronic Engineering Association.

Though the FX409 can be used in any radio-telemetry application, its primary target is mobile radio. In particular, says sales manager Leslie G. Litwin, the company is intitially targeting manufacturers of mobile radios for the Nordic Mobile Telephone system as well as the West German Net B. Another prime target is Japan; for this cost-conscious market the company has produced a variant with somewhat less strict specifications, the FX509; it is $5 in quantities of 10,000. The premium-grade FX409 is priced at just under $15 in lots of 100. Both are available from stock.

The modem circuit makes use of switched-capacitor filter techniques and digital signal processing to pack all the needed circuitry onto a single chip with a minimum of external components. One of these off-chip components is a high-stability 1.008-MHz crystal, which regulates an on-chip oscillator used to set the baud rate and the transmit mark and space frequencies and to control transmit and receive synchronization.

Circuit options. The independence of the transmit and receive sections allows full-duplex operation at 1,200 baud. Among the facilities available to the system designer is a carrier-detect pin that can be used to activate external circuitry. Also, the output data is available in raw unclocked or clocked formats. That way designers have the option of devising their own phase-locked-loop synchronization circuitry to exploit the tradeoff between acquisition time and frequency stability.

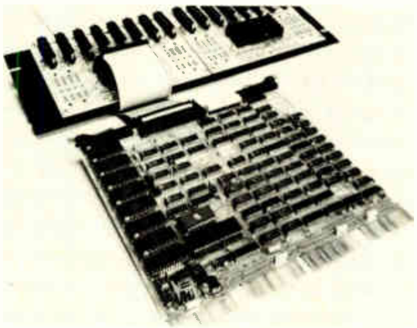
The chip itself works from a nominal 5-V power supply and consumes 2.8 mA with both transmit and receive sections enabled or a mere 450 μA when they are disabled. The circuit is available in either a 22-pin dual in-line package or as a flatpack.

Consumer Microcircuits Ltd., Wheaton Road, Industrial Estate East, Witham, Essex CM8 3TD, England [401]

MX-COM Inc., 8060-F North Point Blvd., Winston-Salem, N. C. 27106. Phone (919) 748-0505 [402]

Multiplexer's capacity is twice DEC DZV11's

A family of low-cost asynchronous multiplexers for DEC's LSI-11 bus provides double the channel capacity of DEC's own DZV11, according to its maker. The models in the 2133 line of asynchronous multiplexers interconnect eight serial data-communications channels with the LSI-11 bus in the space required by four channels when the DZV11 is used.



Thanks to a microprocessor-based interface along with on-board firmware diagnostic capabilities, the multiplexers provide programmable character formats and data rates of 50 to 19,200 baud. The multiplexers can handle single- or four-level interrupt priority capability and can be used with all DEC LSI-11 computers and the PDP-11/23-Plus.

Priced from $900, the multiplexers are supplied in quad-size board configurations. The models available range from single-board modules to systems complete with distribution panel and interconnect cable. Delivery is from stock.

Gen/Comp Inc., 6 Algonquin Rd., Canton, Mass. 02021. Phone (617) 828-2008 [403]

Modem plus multiplexer bows in one package

Called the Modemplexer, a single package functions both as a two-channel statistical multiplexer and a modem. The 2X212, as its model number suggests, is a 212A-compatible, full-duplex, 1,200-baud device.

Its modem capabilities include automatic dialing and answering, automatic redialing, and automatic selection of correct dialing mode. Also, the smart device, which is approved by the Federal Communications Commission, provides speed dialing, storage for up to 10 numbers, continuous memory, dynamic buffering (up to 3,000 characters per port), flow control, hangup code, and user prompts. As a multiplexer, it enables two remote terminals to transmit on one line, reducing phone expenses and network hardware.

To be available four weeks after

receipt of order, the Modemplexer is priced at $995.

Omnitec Data Inc., 2405 South 20th St., Phoenix, Ariz. 85034. Phone (800) 528-8423 [404]

Support for Wang protocols is added to Scitec's multiplexers

A software enhancement for Scitec Corp's CPX and MUX statistical data multiplexers simultaneously supports Wang's Xon/Xoff character format for cathode-ray-tube displays and printers. Handling up to 32 remote devices over a single telephone line, the multiplexers allow users to set priorities for their own channels through preassigned or dynamically allocated buffers.

Providing error-free transmission and reduced line costs, the multiplexers have no intermix restrictions on channel speeds or formats. They support all standard asynchronous and synchronous data rates and bisynchronous protocols. For ease of use, the multiplexers have user prompts and extensive diagnostics.

The enhancement is just one part of an optional package that sells for $300. The MUX sells for $1,200, and the CPX starts at $1,800. Delivery is from stock.

Scitec Corp., 811 Aquidneck Ave., Middletown, R. I. 02840. Phone (800) 849-4353 [405]

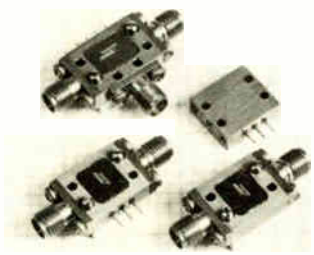
Small rf switches come with integral TTL-compatible drivers

Occupying about 1/20 to ¼ the volume of previously available rf switches, an eight-member family of broadband single-pole, single-throw and single-pole, double-throw p-i-n–diode rf switches covers the entire 2-to-18-GHz frequency range. What's more, the switches' dimensions are the same with or without integral TTL-compatible drivers.

The driver circuits incorporate logic gates at their inputs, providing a single TTL unit load to the user-suplied control interface. This can eliminate the need for buffers to increase the fanout of a complex system, thereby reducing power consumption and propagation delay.

All rf circuitry is fabricated in Avantek's thin-film MIC hybrid construction on a ceramic substrate. The components use laser-welded glass seals for rf and bias feedthroughs, and their lids are welded in a dry nitrogen atmosphere, achieving a high-integrity hermetic seal without the use of solders, fluxes, or epoxies.

Four broadband, low-loss rf limiters with the same frequency coverage



are also becoming available. The single-throw switches range in price from $200 to $400, and the double-throw versions go from $300 to $700. Delivery takes about 90 days.

Avantek Inc., 3175 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 727-0700 [406]

Multiplexer is adapted to split speeds to handle videotex

To gain entry into the rapidly growing world market for videotex and related services, Timeplex has adapted the Microplexer statistical multiplexer to operate at different speeds in sending and receiving. Standards for interactive computer services were set when dial-up modems supported only one channel at 1,200 b/s, half-duplex, with a 75-b/s reverse channel. Using both channels makes a full-duplex connection with split speeds. Most videotex traffic still operates at split speeds of 1,200 or 75 b/s to 2,400 or 300 b/s.

By replacing a pair of universal synchronous-asynchronous receiver-transmitter chips with a small daughterboard, Timeplex added the split-speed operation to its standard four-port expansion modules. With the optional split-speed board, a user may program either the transmit or receive speed of any port at any standard speed from 50 to 9,600 b/s.

The direction opposite to the one set by the option board is determined by the regular procedure through the supervisory port or from the front panel of the Microplexer. Selection of transmit and receive speeds is completely independent.

The split-speed option is available as a factory-installed feature on new Microplexer units, set to the configuration specified by the user. It is also offered as unprogrammed four-port expansion modules and as separate daughterboards for retrofitting existing equipment. The price for a two-channel daughterboard is $150. Delivery is from stock.

Timeplex Inc., 400 Chestnut Ridge Rd., Woodcliff Lake, N. J. 07675. Phone (201) 930-4600 [407]

Narrowband fm receiver resides on one chip

A single 22-pin dual in-line package houses a complete narrowband fm receiver. The bipolar receiver, called S 469, includes an rf stage (for input frequencies up to 50 MHz), an oscillator, a mixer, an adjustable intermediate-frequency limiter amplifier, coincidence demodulator circuits, and two audio-frequency amplifiers with mute and volume control.

In addition, a voltage reference is included on the chip, and it can operate on supply voltages from 3 to 12 V dc. The company believes that the Federal Communications Commission's release of the cellular-radio frequency band will help the receiver find many applications.

To build a receiver with the circuit, only a few external components need be added, including filters, capacitors, potentiometers, and a quartz crystal. In lots of 100 pieces, the chip sells for $4.75 each, with deliveries taking up to six weeks.

Siemens, 186 Wood Ave. S., Iselin, N. J. 08830. Phone (201) 321-4842 [409]

Products newsletter

After delay, TI ships high-speed C-MOS parts

After delaying its entry into high-speed complementary-MOS logic in order to boost performance of its initial designs, Texas Instruments Inc. has placed the first parts in the hands of distributors and plans to expand the family quickly during the next year. Since June, preliminary copies of TI's C-MOS–logic data books proved hot items at chip distributors, but it was not until recently that **the Dallas firm began shipping about 20 chips—including standard gates, quad and octal bus transceivers, and an 8-bit shift register.** In quantities of 1 to 99, prices range from 69¢ each for HC00, 08, 10, 11, 20, and 21 gates to $3.96 each for HC620, 623, 640, and 643 octal bus transceivers.

Converters boast 12-mV offset voltage

Geared to a variety of military and avionics position-control applications like radar, navigational systems, and flight-position simulation, two **hybrid digital-to-resolver converters guarantee two to four times lower output offset voltage than their competitors,** says developer Analog Devices Inc. The Norwood, Mass., firm's 14-bit DRC1765 and 16-bit DRC1766 have a maximum offset voltage of ±12 mV over the full military temperature range of –55° to +125°C. A complementary-MOS version dissipates a maximum of 735 mW, while a low-power Schottky version uses 1.12 W maximum. Available from stock, the DRC1765 starts at $404 each, and the DRC1766 at $513.

Development system goes multiuser

Exploiting a virtual-disk architecture and high-speed data links, Emulogic Inc. has made a multiuser microprocessor–development-system network out of its ECL-3211 work stations [*Electronics,* Feb. 24, 1982, p. 174]. Emunet-2 attaches the Norwood, Mass., firm's single-user work stations to any VAX system **along as many as four 1-Mb/s multidrop coaxial cables that each handle a maximum of 15 work stations.** An Emunet-2 system composed of six ECL-3211 stations and six Digital Equipment Corp. VT100 terminals costs between $110,000 and $160,000, excluding the host VAX computer. Delivery takes 60 days.

$29,995 drafting system targeted at architects

Recognizing that 85% of all architectural firms in the U. S. employ less than 15 people, the Interactive Graphics division of Bausch & Lomb, in Houston, Texas, has put together a turnkey computer-aided drafting system that, at $29,995, may meet tight budgets. **The ProDraft hardware package includes a 15-in. 1,024-by-800–picture-element raster display** controlled by a 68000-based graphics processor, a menu tablet for selecting figures and functions used repeatedly, a plotter, and a 6.7-megabyte Winchester disk drive. Five menu-driven software packages tailor the system to architects. Deliveries should begin in November.

32-K-by-10-bit E-PROM serves HP-41C/CV

For those needing extra nonvolatile memory in the field, the HHP-PE erasable programmable read-only-memory module aims to please. The $349 unit for the HP-41C/CV calculator is being introduced by Hand Held Products Inc., Charlotte, N. C., and will be available Sept. 1. Starting with 8-K by 10 bits of E-PROM, **the unit may be expanded up to 32-K by 10 bits using standard Intel chips.** These parts are data-compatible with the current HHP-16K and -32K E-PROM units.

Career outlook

IEEE helps the EE get ahead

What with the recent fuss about a possible shortage of engineers and the resulting preoccupation with the newly graduated engineers and computer scientists, established professionals may be forgiven for feeling neglected. This neglect and the breakneck pace of change in electronics have created seemingly insurmountable obstacles to keeping up—let alone getting ahead.

Even so, people who seek to expand their careers beyond electronics engineering as traditionally defined can follow many paths—among them, advanced education, short courses, in-plant seminars, and home videocassette offerings. More and more companies now make a practice of paying all or part of the cost of tuition for such pursuits.

Amid all this, one of the most obvious sources might turn out to the the best in many cases. The Institute of Electrical and Electronics Engineers, through its 10-year-old U. S. Activities Board, has involved itself in a variety of career-related pursuits. Among the most valuable is the series of annual conferences it inaugurated in 1981.

The third annual Career Conference will be held this Oct. 27 and 28 at Hyatt Rickeys, in Palo Alto, Calif., hard by the legions of EEs toiling in Silicon Valley. For a members' registration fee of $160—$185 to nonmembers—professionals who want to move up or out will get a day and a half of papers, responses to papers, and panels devoted to the theme, "Enhancing Engineering Careers by Fulfilling Individual and Organizational Goals."

Four areas. Conference chairman Wallace D. Decker—a member of the senior engineering staff at Lawrence Livermore National Laboratory, in Livermore, Calif.—thinks that the meeting will be especially valuable for practicing engineers, corporate managers and supervisors, human-resources managers, education directors, and social and behavioral educators.

Decker says the sessions will provide information for attendees in four major areas:

- How to bring company goals closer to personal goals.
- How different firms have responded to career issues in engineering.
- How to help engineers and companies alike by improving career prospects for engineers.
- How professional societies can help their members enjoy more fulfilling careers.

Two evening workshops on the first day, Thursday, exemplify the thrust of this conference: one on preparing engineers and engineering managers for their roles and another on "Overcoming Engineering Career Roadblocks." Next morning, a Career Strengthening Workshop will delve into the nontechnical aspects of engineering performance, covering such matters as getting along with supervisors and fellow engineers.

On the first day, four sessions will cover a range of subjects, including career transitions and the use made of engineers. The two sessions on the second day will explore improved practices in the workplace and "Who Is Responsible for My Career?" (the title of one of the sessions), among other topics.

One of the more interesting sessions, on the first day, will dissect "mentoring," a social-science label that describes the relationship beween junior and senior colleagues. Kathy E. Kram, assistant professor of organizational management at Boston University, will discuss companies that base their job-performance ratings and pay raises on their employees' success in developing relationships with subordinates.

Papers will be given not only by the usual flock of independent consultants and academics but also by employees of General Electric Co., Honeywell Inc., and Hewlett-Packard Co. James B. Owens, president of the IEEE, will speak at the luncheon that closes the conference.

Conference registration information is available from William R. Anderson, IEEE/USAB, 1111 19th Street N. W., Suite 608, Washington, D. C. 20036. The telephone number is (202) 785-0017. ☐

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