JANUARY 27, 1982

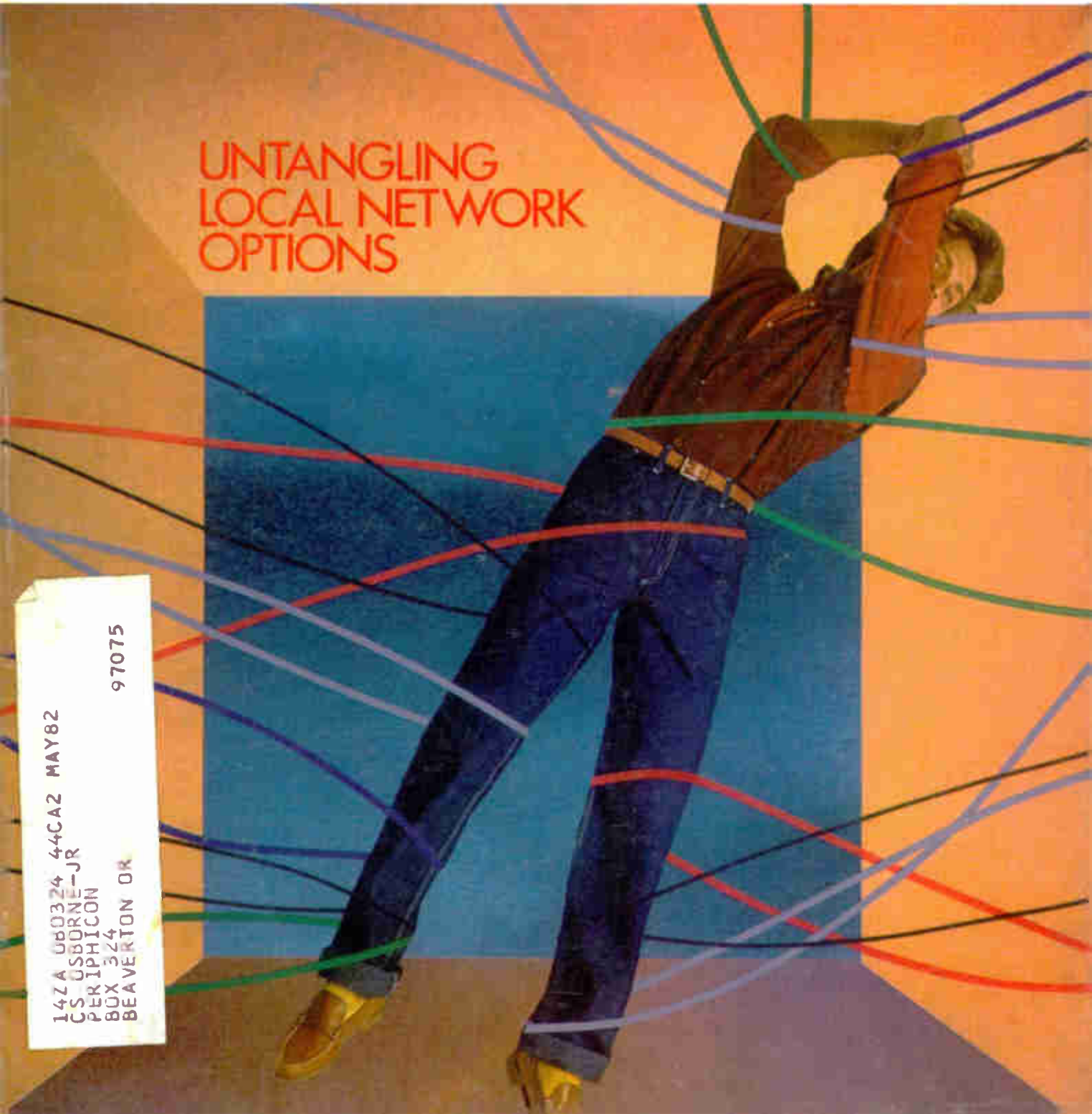
**WILL AT&T's BREAKUP BE A BOON TO TECHNOLOGY?/73**

Design automation: turnkey system covers logic to layout/108

Memories move to leadless chip-carriers/119

SIX DOLLARS A Mc GRAW-HILL PUBLICATION

# Electronics



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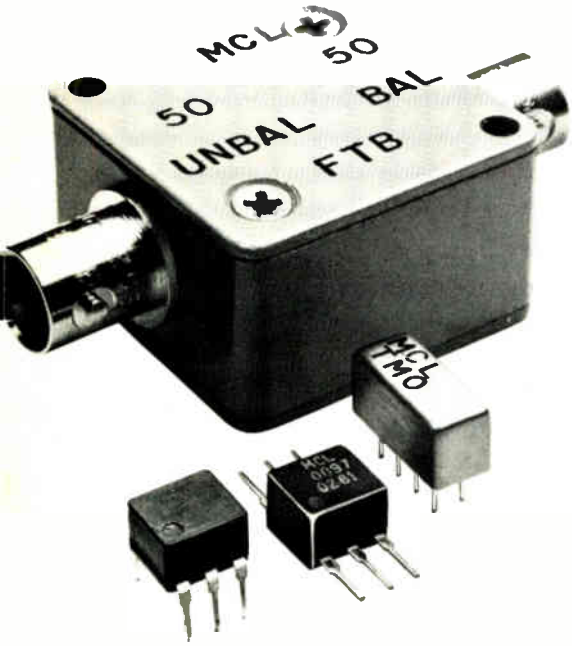

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# Electronics

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# Highlights

### Cover: Local nets, once unsnarled, carry opportunities, 89

Local networks are starting to burgeon, a state of affairs that mixes confusion and opportunity. A roundup of present local nets (p. 90) will help dispel the confusion for the would-be network designer. The following article (p. 96) details how one such opportunity was grasped: the expansion of the CP/M operating system into local-net applications.

The cover collage is by Marc Yankus.

### Unshackled AT&T and IBM to go head to head, 73

With their antitrust cases behind them, American Telephone & Telegraph Co. and International Business Machines Corp. can be expected to move in on each other's territory. There look to be five major areas of competition, each dependent on computer and software technology. However, the impact on each other may not be as great as the effect on the rest of their respective industries around the world.

### Board debugging is straightforward with static checks, 100

Checking out microprocessor-based designs even before the software is added on is easy with static stimulus testing, which treats a board as a producer of a series of electrical states to be debugged in sequence. This article is another in the Test Tactics for the '80s series.

### VLSI doesn't faze microelectronics design system, 108

Automated layout in a turnkey design-automation system can take on very large-scale integration with a data-base manager tailored to computer-aided design. The system also can learn design heuristics from its users. This article is ninth in a series on design automation of integrated circuits.

### Navy looks to fiber optics for shipboard links, 113

The link between an aircraft carrier's radar and its operations center uses 7 tons of copper wire that costs $1 million to install; a multiplexed fiber-optic cable would weigh 15 pounds and cost about $30,000 for installation. Qualification testing of such a system is under way.

### Rectangular leadless chip-carriers for memories gain favor, 119

Now that integrated-circuit memories are mostly rectangular, a leadless chip-carrier of the same shape makes sense to improve packing densities. With a standard for these chip-carriers in the offing, users' attention is focusing on how best to attach them to a substrate.

### . . . and in the next issue

The International Solid State Circuits Conference . . . a 5-volt-only electrically erasable programmable read-only memory . . . a complementary-MOS random-access memory that hits emitter-coupled-logic speeds.


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# Publisher's letter

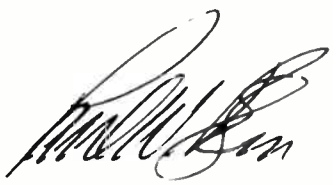
One of the toughest challenges our news editors face is coping with a major story that breaks just after we have put an issue to bed. Word that the Justice Department had settled its antitrust suits against the American Telephone & Telegraph Co. and International Business Machines Corp. reached us at about the worst possible time—on the Friday afternoon that our first issue for January had just been printed and was being mailed. On Saturday, the landmark antitrust decisions hit the front pages of the nation's newspapers. And the business pages of the Sunday papers carried long second-day stories analyzing the impact of the two decisions.

Knowing that the general newsmagazines as well would follow with their extensive versions of what had happened and what it might mean, our editors on Monday started thinking about story lines that would bring special insights to readers of *Electronics*. The most promising one came from computers editor Tom Manuel and communications editor Harvey Hindin, who singled out five sectors where the two unleashed giants will compete with products that involve both computers and communications.

The competition between AT&T and IBM won't be head-to-head; many other companies are striving for shares of the burgeoning markets for equipment and services that juxtapose computers and communications. So to flesh out the basic story line, we had every one of our field bureaus—domestic and foreign—interview executives of other communications-computer companies to get a fix on how the heightened competition would accelerate technology in equipment like PABXs, intelligent terminals, computer mainframes, and personal computers.

A particularly heavy file came from our man in Washington, Ray Connolly, who tipped us off about the AT&T decision minutes after it was announced and who later made himself privy to much first-hand insight by cornering executives of AT&T and IBM who had come to the Capital for the court hearings. The story, assembled in New York by associate managing editor Howard Wolff, starts on page 73.

For our leadoff pair of technical articles, the timing of the Justice Department was near perfect. The section starts with a short introduction by Tom and Harvey titled "Local networks will multiply opportunities in the 1980s" (p. 89)—opportunities that both IBM and AT&T fully intend to exploit. "We have done a half-dozen stories on local networks since the first one in September 1980," says Tom. "But so much new hardware has surfaced recently that we decided to do an overview of it." For the overview, Manuel enlisted as authors two well-known consultants, Kenneth Thurber and Harvey Freeman, both of whom taught computer science at the University of Minnesota while working in Minneapolis for Sperry-Univac. For the software side of networking, software editor R. Colin Johnson enlisted the operating-systems expert of Digital Research, Thomas Rolander.



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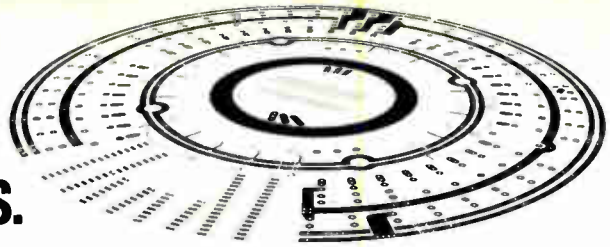
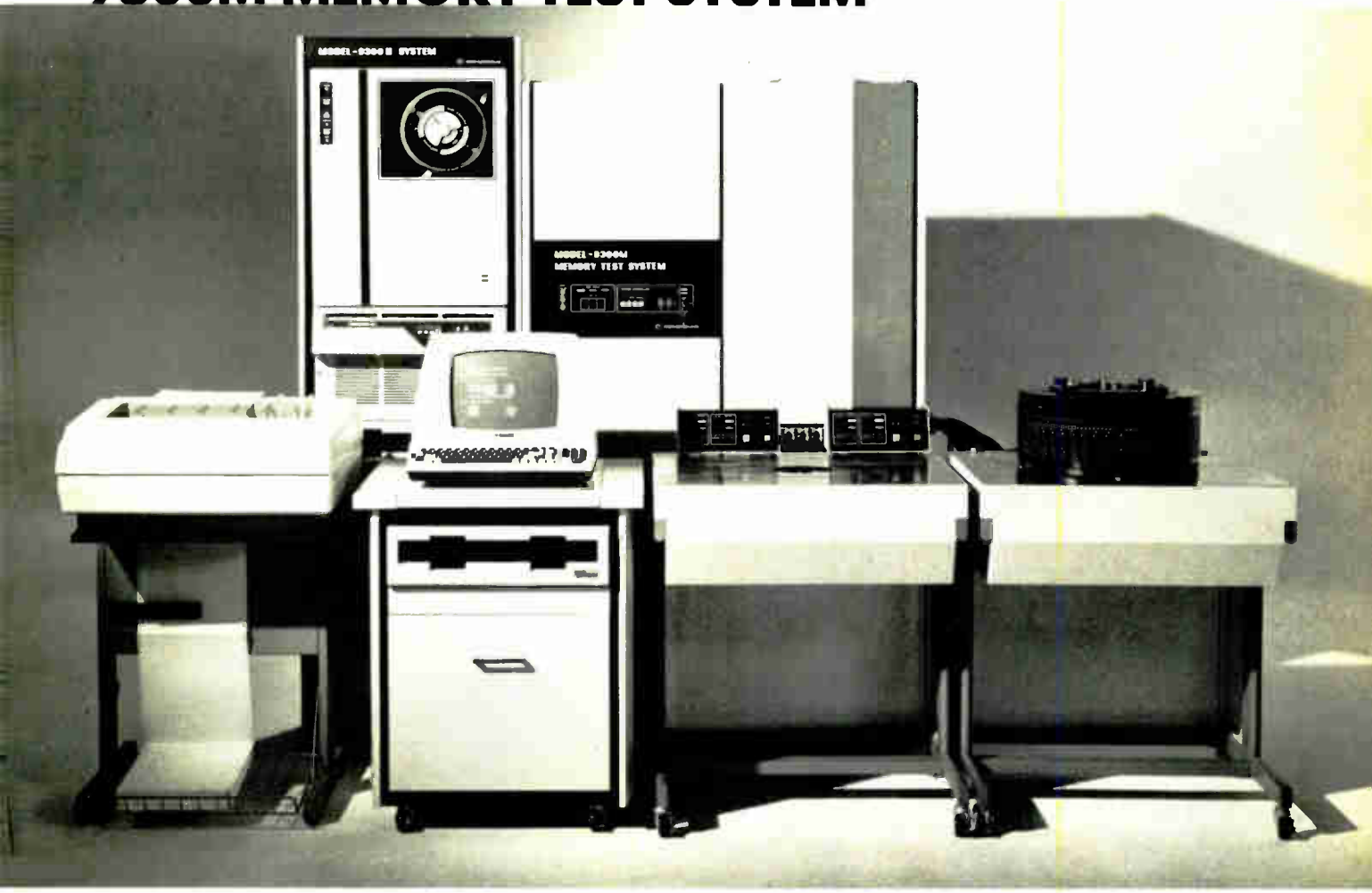


# 9300M MEMORY TEST SYSTEM



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# Readers' comments

## Packing them in

**To the Editor:** I would like to take issue with the article on page 57 of the Dec. 15, 1981, issue of *Electronics*, by Martin Marshall, regarding the development of optical storage tape. When Mr. Marshall talks about the promise of optical storage tape, which will offer data storage at a lower cost per bit and higher packing density than magnetic tape, he has overlooked what has been produced many years ago and is currently in wide use in the instrumentation tape-recorder field.

I agree that the bit densities used in the present generation of computer tape handlers are very low. However, Derritron has been recording digital data on 1-inch-wide magnetic tape, at a bit density per square inch of $1.34\times10^6$ bits, for over three years. Currently, with narrow-gap heads and high-energy tape, we are able to record data at $2.8\times10^6$ b/in.$^2$, and developments are already well-advanced in Japan and in the U. S. to increase the longitudinal packing density, which will result in densities of $40\times10^6$ b/in.$^2$. These developments use microgap heads and unoriented small-particle tape and should bear fruit before those anticipated for optical storage tape.

I have calculated the bit densities per square inch stated in the article for optical tape, and these are $5\times10^6$ b/in.$^2$ for the 5-micrometer holes and $20\times10^6$ b/in.$^2$ for the 2.5-$\mu$m holes. The bit density is apparently reduced to $0.28\times10^6$ b/in.$^2$ for the 50-foot length of 3-millimeter-wide optical tape that is stored in a cassette housing.

It is obvious from the above that the optical storage tape does not offer bit densities that are of magnitude greater than that currently achieved with instrumentation magnetic tape. In addition, I am aware that IBM Corp. is due to launch in 1982 a tape handler that will make use of the techniques similar to that used in the instrumentation tape recorder field, so as to offer a product with greater storage capability. These developments, together with those projected for instrumentation and video magnetic tape, will certainly give optical tape a good run in the data storage arena.

J. R. D'Silva
Derritron Environmental Recorders Ltd.
Surrey, England

■ **Martin Marshall replies:** *The developments at Derritron do indeed represent a state-of-the-art advance over what is available in the commercial computer magnetic-tape market. Even so, they fall short of the expectations of optical tape researchers. Jerome Drexler, president of Drexler Technology Corp. of Mount View, Calif., points out that, although his firm's prototype tape currently used 5-$\mu$m holes, "we believe that the tape can go down to 0.8-$\mu$m holes" for a bit density of $200\times10^6$ b/in.$^2$, which is a fivefold improvement over the most optimistic projections at Derritron.*

## Interchangeable parts

**To the Editor:** A question from one of the 12 million small-business owners in this country: why are computers not sold in the form of standardized interchangeable components like, for example, electrical and plumbing products?

Perhaps you will agree with my answer that, as a group of prospective customers, we will only get the flexibility that standardization provides if we insist on it.

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While some computer companies will resist standardization, it will come. After all, standards have not hurt the electrical or plumbing industry.

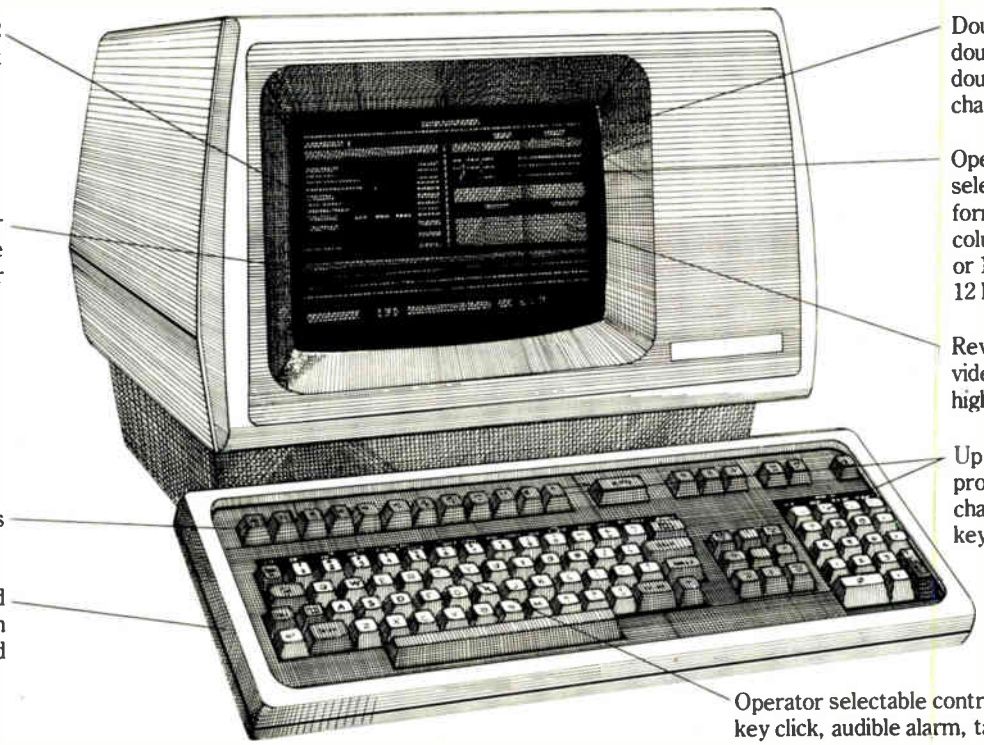
Henry Keultjes
Microdyne Co.
Mansfield, Ohio

## Correction

*In "ISSCC: VLSI earning its keep" (Dec. 15, 1981, p. 101), the 256-channel cross-point array mentioned was developed solely by Plessey Ltd. with funding from British Telecom, rather than as a joint venture.*

# Managing Editor.

## 940
## Electronic Video Terminal

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Circle 11 on reader service card

# Antitrust settlements are a boost for innovation

There's still a lot of detail to be clarified, and undoubtedly many legal obstacles remain to be removed, but the emergence of a leaner and meaner American Telephone & Telegraph Co. in the commercial competitive marketplace and a more dynamic International Business Machines Corp., unencumbered by threats of antitrust action, will soon be a reality. Although freeing up these two giants with their huge technical, marketing, and capital resources will certainly be a threat to some companies, overall the settlement of the IBM and AT&T cases will prove beneficial to the U. S. and industry.

In the case of IBM, the ending of the antitrust suit was long overdue. Indeed, one wonders why this case was allowed to drag on for so long, with its expenditure of millions of dollars and much energy that could have been used in better ways. If the case had been resolved with a decision to break up the giant computer company, the cost, in our opinion, would have been even greater—comparable with the loss of an important natural resource.

As for AT&T, there are still many unanswered questions as to what the economic effects of divesting the 22 operating companies will be, and what that will mean to telephone users. But there is very little doubt that AT&T, now able to turn the incomparable talents assembled in its Bell Laboratories toward commercial pursuits, will provide a powerful stimulus to innovation both within the company and among its competitors. Admittedly, it will have to become a new kind of organization, shedding its academic, sheltered image and moving out into a world where being first is just as important as being best.

Another important aspect of these settlements is that they represent a step toward a new national perspective on competition. In a world where the competitors clashed only on the home grounds of the U. S., then bigness could be—and often was—a bad thing. But the world has changed, and the competitive situation now encompasses foreign governments that have recognized—with more insight than has been exhibited by our own—that high technology is key to national economic growth. As a result, they are providing support and encouragement to their industries, and the U. S. is now hard pressed to maintain its formerly unquestioned leadership position. However, it is in those areas where AT&T and IBM excel—communications and computers—that the battle stands to become most fierce. Thus, in the new international competitive arena, the U. S. will at least have the world's heaviest hitters on its side.

This strength is particularly welcome in view of the coming joint effort by the Japanese government and computer manufacturers to produce a so-called fifth generation of computers. They make no bones about their goals: the 10-year research and development program is dedicated to leapfrogging U. S. computer technology and capturing dominance in the worldwide market. But any fifth-generation machine will be more than just a computer—the problem-solving capabilities of their systems will go far beyond even the most advanced concepts of today in a blend of hardware, software, and communications. An AT&T and an IBM that are free to explore this blend would then be in a much stronger position to meet such a challenge.

This is not to say that we should no longer be alert to the possible abuse of economic power on the part of these giants or others that may develop by sheer excellence and drive. The public must still be on guard against the incursion of robber barons. But the new thesis that bigness is not always bad has validity—and the blessing of the courts.

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Circle 13 on reader service card

# People

## Karatsu honored for role in quality assurance

The nomination of Hajime Karatsu as the 1981 Deming Prize winner for his work in the field of quality assurance was a surprise only because most in Japan assumed he had won it long ago. It was Karatsu who pioneered QA at the Electrical Communication Laboratory of Nippon Telegraph & Telephone Public Corp. in the 1950s, and it was after his 1961 move to Matsushita Communication Industrial Co. that that firm pulled among the top three leaders in the field.

**Apostle of quality.** Hajime Karatsu's espousal of quality-assurance concepts has won for him the 1981 Deming Prize.

Karatsu also promoted the idea that high quality, not price dumping, was responsible for high U. S. sales of Japan-made integrated circuits and other products. His exploration of this idea at a Washington, D. C., seminar in March 1980 [*Electronics*, April 10, 1980, p. 81] prompted American industry to send study groups to Japan to research the techniques.

Along with Akira Harada, Karatsu started worker-participation groups called quality circles at Matsushita, in parallel with the formation of similar groups at Nippon Kokan KK and Tanabe Seiyaku Ltd. Now, of course, quality circles are entrenched worldwide.

It is Karatsu's shadow, too, behind the monopoly by the Denden family of NTT's high-technology communications equipment purchases—Denden is a Japanese acronym for NTT. He pushed the view that the route to quality was not through tighter inspection of finished products, but through the choice of qualified vendors.

As a result, plant inspections to audit quality control were initiated as part of an integrated system of procurement and QA. It became possible to order specific product lines from the same reliable two to four vendors, now an industry practice.

Karatsu dabbled in market research, as well, as head for two years of a committee that sifted through the world's future social and economic needs in an attempt to predefine Japan's upcoming fifth generation of computers.

"I was very busy during those two years," he recalls, "with meetings that lasted until late at night as well as an all-weekend meeting two times a year." He is now on the steering committee for the project. "The pace has slackened temporarily," he says,"because the various working groups have not yet come up to speed. But by the end of March, there will again be many decisions to be made."

## Kuhn sees RCA adding new video disks faster

Though sales of RCA Corp.'s VideoDisc players are running behind projections, sales of the disks themselves in 1981 were two times the volume predicted. That is the mixed message from Thomas G. Kuhn, the new division vice president for the product line at RCA.

The 46-year-old native of Chicago points out that the average owner of a VideoDisc player has more than 18 albums. "People are building libraries," he says. "They are becoming collectors." He contrasts this with a consumer trend toward rentals of cassettes in the competing vid-

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Any way you configure your new 8860A DMM, you'll streamline your applications today and leave the door open for new opportunities tomorrow. For more information, call toll free **800-426-0361**; use the coupon below; or contact your Fluke sales office or representative.

*"We designed the 8860A to be a powerful, accurate multimeter, with low-cost options that make it fully programmable. This kind of flexibility makes the 8860A a practical solution for a wide range of measurement needs."*




***Input protection to 1000V;*** *safety design uses recessed input jacks and eliminates four-terminal ohms and guard shorting links.*

***5½-digit resolution*** *with function annunciators.*

***Five-function DMM*** *features autoranging, four advanced math functions and 0.01% basic dc accuracy.*

***Exclusive Portable Test Instrument Packaging*** *lets you stack-and-latch the 8860A with other Fluke PTI Instruments.*

***Excellent value*** *in an easy-to-operate DMM. The basic 8860A is $1395; add $295 for the IEEE-488 interface, or $550 for the calculating controller.*

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For technical data circle no. 15

eo-cassette recorder market.

Kuhn can be considered something of an expert in the new field of entertainment software, with most of his professional background in television production. He comes to the top VideoDisc spot at RCA's Rockefeller Center headquarters in New York from Los Angeles, where he headed West Coast operations. Before that, he was vice president in charge of production at Warner Bros. Television and then executive vice president in charge of television operations and program development for Allen Landsburg Productions. He also has has a master's degree in business administration from the University of Southern California.

Based on the sales statistics, then, part of RCA's strategy for 1982 is to accelerate its issuance of new disks. Plans are for 160 titles to appear this year, which means that by the time 1983 rolls around there will be 300 from RCA alone that are available to the new American collector.

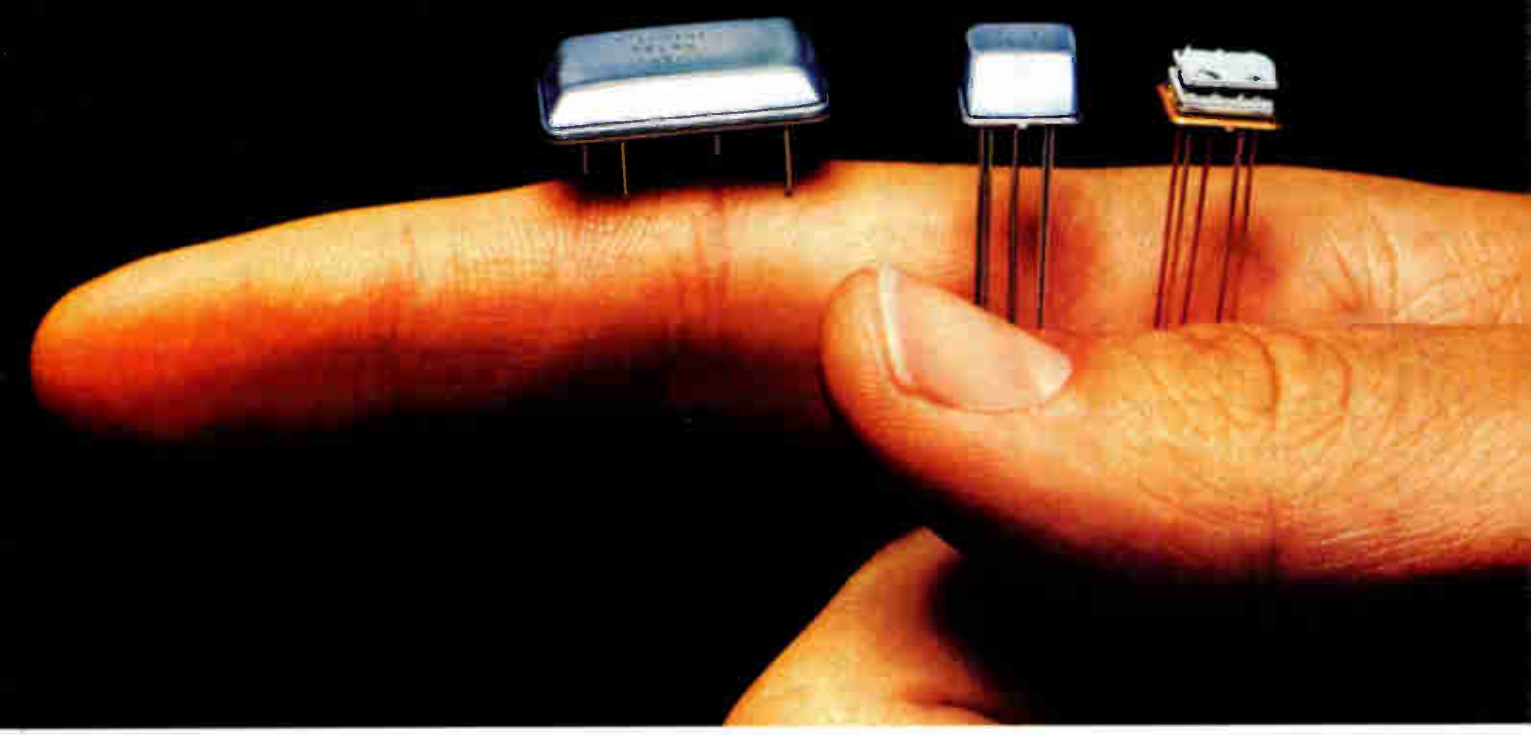
RCA hopes stereo models will boost lagging sales of players after they appear in midyear, says Kuhn.

Bearing out RCA's prediction that VideoDisc and VCR are compatible market mates, says Kuhn, is a survey showing that 20% of disk-player owners also have cassette players. "We maintained all along they were complementary, with disk players appealing to those who wanted to build an entertainment library and VCRs to those who, if they can't see a program when it is shown, want to record it for later viewing," Kuhn says. □

**Disk fan.** Thomas G. Kuhn says sales of RCA's VideoDiscs are ahead of schedule.

# The Power FET SSR

# Its low resistance is a real turn-on



It certainly is. We've used power FET technology to reduce the ON resistance in the output stage below 0.3 ohms. That means it can switch low level signals with no offset voltage. It also means it can handle full load currents at higher ambient temperatures.

But the low ON resistance is only one of the goodies. We've included buffering so the relay can be driven directly by CMOS as well as TTL logic. And we incorporated a Schmitt trigger in the CMOS mode to prevent false triggering in a noisy environment.

We've used some special circuits to control turn-on and turn-off times. That virtually eliminates the on-off spikes and results in very low EMI. And optical isolation is used to protect the sensitive input circuits from voltage transients.

By use of hybrid microelectronic techniques, we've been able to package all this capability in a tiny Centigrid® package (690 Series), or in a metal DIP (685 Series) which permits full current operation up to 75°C. Both are designed to meet MIL-R-28750, and are available for either AC or DC operation.

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# For the microcomputer design manager who wants to bring out the best in his team.

## Tek introduces the 8560.

To help his people work as a team, a design manager's got to pull together every designer. But he can't do it alone.

Code volumes are heading toward the megabyte range. Soon, a single project may require designers to develop and debug hundreds of modules — all against ever tightening production schedules.

As microcomputer design becomes this demanding, only a team working tightly together can be successful.

But not until now has a microcomputer development system been dedicated specifically to the needs of a team of designers.

Not until the Tek 8560 Multi-User Software Development Unit. **The 8560 is targeted directly at the team effort.**

For openers, the 8560 sup-

# TEK 8560 MULTI-USER SOFTWARE DEVELOPMENT UNIT

FLEXIBLE SOLUTIONS FOR A FUTURE OF CHANGE

ports up to eight workstations. With each station configurable as either a software development terminal or a hardware/software integration site.

You get all the standard tools you'd expect from a high-performance development system: editors, language translators, loaders, linkers, spooling line printers and hard disc mass storage.

But that's just the start. The 8560 goes on to organize these tools specifically for use in a closely knit team effort. One that channels individual efforts into a workable, synergistic whole.

All through TNIX*.

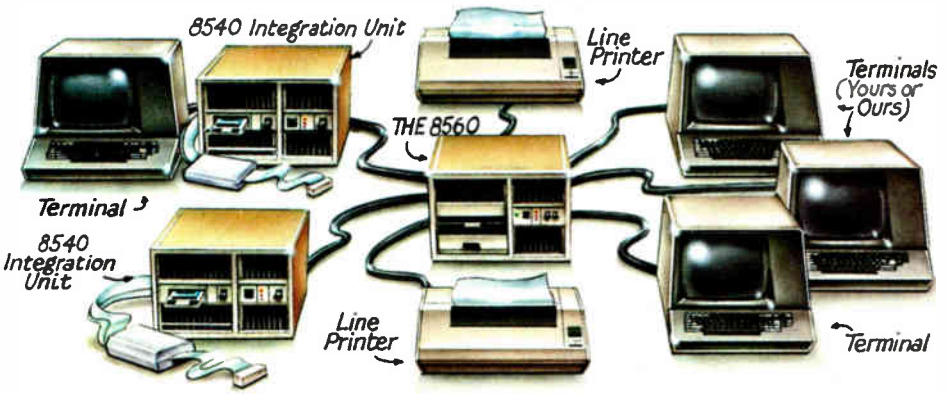
**TNIX ties the team together.**

TNIX, an operating system derived directly from Bell Laboratories' UNIX** V.7 operating system, runs the 8560. Refined specifically for microcomputer development, TNIX includes a multitude of features that enhance the team effort.

| The 8560 Supports: | | |
|---|---|---|
| 68000 | 6800 | 8035 |
| Z8001 | 6801 | 8748 |
| Z8002 | 6802 | 8049 |
| 8086 | 6809 | 8021 |
| 8088 | Z80A | 8041A |
| 8080A | 8048 | 8022 |
| 8085A | 8039 | |

A hierarchical filing system allows you to organize your files by project, in sub-directories. So you can quickly locate any file: yours or your team-members'.

**TYPICAL 8560 SYSTEM CONFIGURATION**




Plus multi-level read/write protection that lets users' files become more accessible as they become more complete.

Text processing keeps team members well informed by facilitating timely documentation. All design specifications are easily updated working documents.

With the number of code modules running into the hundreds, the integration of different "versions" of source modules from multiple team members can result in very bothersome program bugs. TNIX provides a powerful solution through "make", a utility which tracks dependencies between source and object modules, and insures that only up-to-date object modules are included in the final program.

**TNIX extends to hardware/software integration as well.**

For hardware/software integration, the 8560 uses the Tektronix 8540 Integration Unit as an intelligent subsystem. The 8540 employs Real-Time Emulation for fast, efficient debugging. And for tracing real-time program execution, an optional Trigger Trace Analyzer allows highly selective acquisition of bus transactions and other prototype logic events.

And because the 8540's debug commands are fully integrated into TNIX, you have unprecedented power to process debug data. For instance, a few simple commands provide the capability to sift through debug trace data and produce a frequency distribution of all subroutine calls as executed by the prototype program.

Put the 8560 on your team.

For more information, contact your nearest Tektronix Sales Engineer about buying or renting the 8560. Or contact us at any of the addresses listed below.


GUIDE, a friendly user interface, provides a menu-driven path through system operations, while allowing a return to the conventional TNIX command interface at any time.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Technological leadership.

# The MC68000 directly of memory. Other 16-bit

All 16-bit microprocessors are not created equal.

Motorola's MC68000 has extra ALU capacity, 32-bit address registers and linear address space. It can directly address 16 megabytes of memory.

Some highly-publicized 16-bit microprocessors are limited by segmented architecture, 16-bit registers and less ALU capacity than the MC68000. They address only a 64K byte memory segment directly, and just a fraction of the MC68000's memory resources even with extra instructions and tortured, costly and time consuming coding schemes.

Only the MC68000 is equipped to do the job a 16-bit microprocessor is expected to do for today and tomorrow, simply and without severe memory limitations.

Other strengths also contribute to the unprecedented recent design-in rate of the MC68000. Documented leadership in benchmarked performance and the powerful, but simple, instruction set are important factors. So are the flexibility of the seventeen 32-bit multi-purpose registers and the comprehensive M68000 Family of VLSI peripherals. So is the multiuser EXORmacs™ 16-/32-bit development system. And, the MC68000 is sourced by numerous leading high-technology suppliers around the world.

Among the many assets of the MC68000, one that very often tips the balance in its favor is the linear architecture which permits efficient, cost-effective, direct address of very large memory.

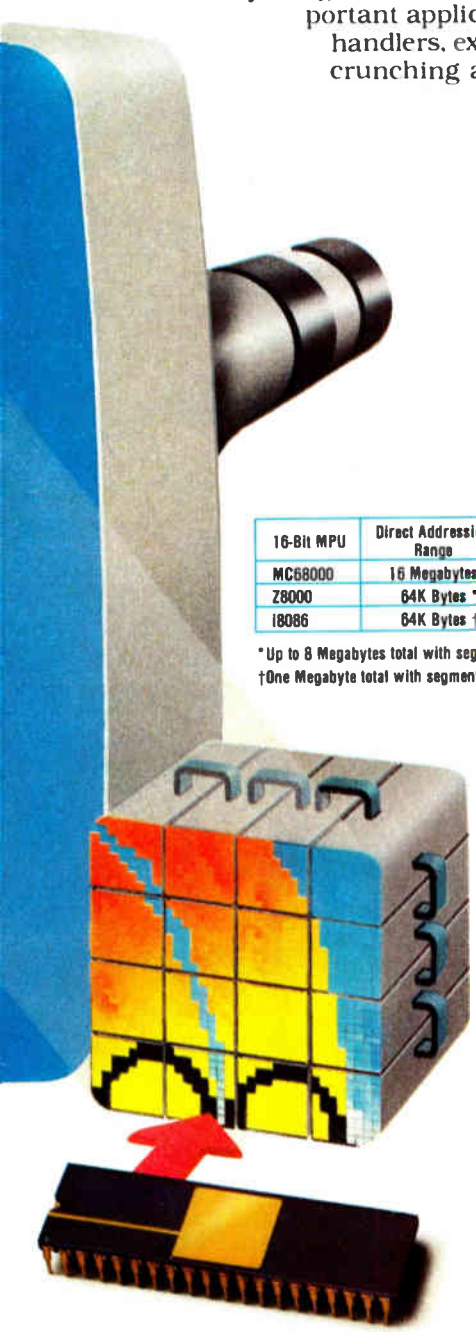
In non-MC68000 systems, extra instructions required for manipulating addresses in a segmented environment use memory resources wastefully, and require costly and time-consuming extra code.


**MC68000**

**Direct memory address capability 256 to 1**
**Total memory address capability 16 to 1**

# addresses 16 megabytes MPUs can't come close.

Limitation of the maximum data structure for 64K byte segments is devastating in important applications like data handlers, extended number crunching and graphics, as illustrated here.



| 16-Bit MPU | Direct Addressing Range | Free of Segmentation Overhead |
|---|---|---|
| MC68000 | 16 Megabytes | yes |
| Z8000 | 64K Bytes * | no |
| I8086 | 64K Bytes † | no |

*Up to 8 Megabytes total with segmentation.
†One Megabyte total with segmentation.

**Ordinary 16-Bit MPU**

System expandability is practical and easy with MC68000's direct access to 16 megabytes of resources. With segmented architectures it is cumbersome at best and severely limited at worst.

It also pays to remember that in addition to space limitations and the time and cost disadvantages imposed by segmentation, the coding gymnastics required to work around the segments slows down system speed, often drastically.

Certain segmented architectures cause additional problems by requiring dedicated registers. Others have only 16-bit registers that must be paired. By contrast, the MC68000 has a 32-bit architecture with 32-bit registers. Many additional coding requirements are avoided and valuable high-speed register space is efficiently used.

There are times, of course, when you prefer dividing-up memory resources: for protective purposes, for example. Our MC68451 Memory Management Unit is appropriate for these occasions. The choice is yours when you want it, but you're not forced into anything by a permanent, inflexible MPU architecture.

Don't fall into the segmentation trap. Beware of 16-bit MPUs with segmented architecture that result in slower system speed, costly extra instruction and coding requirements, and limited memory.

Get the rest of the MC68000 story. Write or send the coupon below to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036. Then do as so many forward-looking designers are doing today. Design in the MC68000 for your

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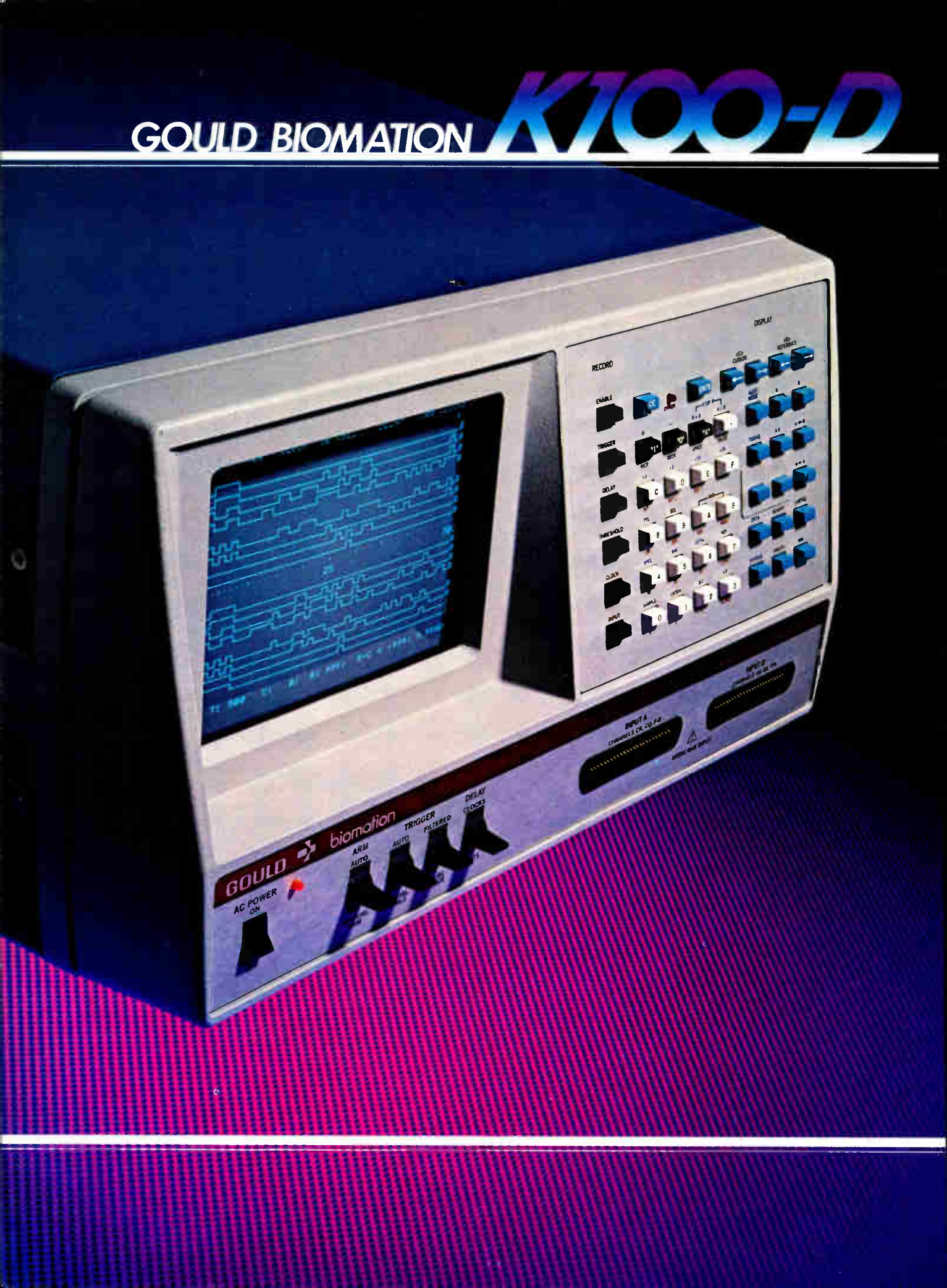
# GOULD BIOMATION K100-D



# 7 reasons why the K100-D is now the world's best-selling logic analyzer.

## How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

**1. It's easy to systematize.**

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

**2. It's concise.**

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

**3. It's fast.**

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

**4. It's deep.**

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

**5. It's clear.**

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

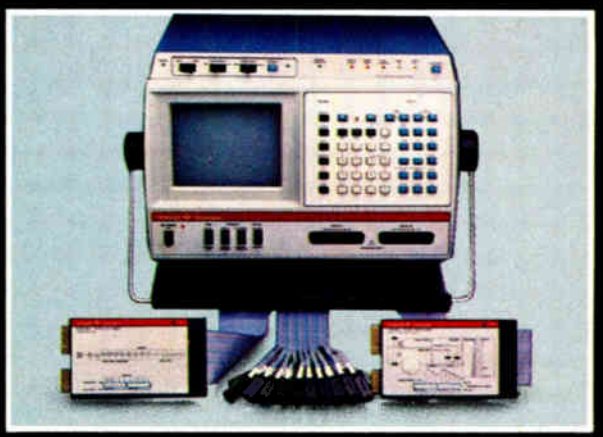
**6. It has remote diagnostics.**

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

**7. It's well supported.**

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.



The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

GOULD

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Circle 177 for Comparison Guide
Circle 178 for APP Note request form
Circle 23 for T-12 communicator data

# Free enterprise versus the sole-source syndrome

**by John Callahan,** *manager, contracts, National Semiconductor Corp., Santa Clara, Calif.*

The Department of Defense has long been concerned with the amount of bargaining power it relinquishes by having sole-source suppliers for various pieces of equipment. So to promote and ensure parts availability from more than one source, contractual provisions have been drafted by the DOD to give it the rights to patents and processes that have been developed under or used on DOD-funded contracts—the so-called patent-rights and technology-transfer clauses.

The patent-rights clause applies only to inventions and discoveries made under a specific Government contract. On the other hand, the technology-transfer clause allows the Government to use and disseminate not only processes developed under a specific Government contract to whomever it chooses, but whatever expertise the contractor has developed at its own expense to create a better product.

For the primarily commercially oriented manufacturer, the existing patent-rights and technology-transfer clauses—especially the latter-represent what amounts to a forfeiture of vital and costly competitive advantages for the right to participate in a Government program that will yield a much lower profit rate than what would be obtained on the commercial market. A major and continuing need of these companies is capital, and the correct allocation of scarce resources is crucial to the success of any high-technology firm. After all, the most valuable possession of high-technology companies is their technical expertise. Because of these factors, top management must direct its limited technical resources into channels that will prove to be most lucrative for the company.

The technology-transfer clause requires a company to license a competitor, enabling him to use the owning company's processes. However, restricting the license to Government work is ineffective due to the fact that the technology is readily transferable and a licensing-agreement violation is virtually impossible to prove.

In addition, Government contracts in no way compensate the prospective contractor for the potential market loss due to the forced sharing of proprietary processes. Inadequate compensation for the license strikes home when it is realized that the party setting the appropriate fee (the Government) also pays it!

Although not as onerous as the technology-transfer clause, the patent-rights clause also causes problems in commercially oriented high-technology industries. One trouble with this clause is that it is difficult to determine if a specific development is an original idea or just something that came from working experience. In addition, many concepts that can be patented are just modifications or improvements of existing proprietary processes and, if taken by themselves, have very little value. Finally, the administrative nightmare involved in accounting for the limited portions of processes that the Government will have rights to is considerable.

The Government's position on technology ownership presents a major disincentive for commercially oriented high-technology industries to participate in DOD projects. These firms must continuously improve and develop products in order to maintain a competitive position in a rapidly changing market. For these companies, Government sales represent a comparatively small portion of their business and do not warrant jeopardizing their position in the larger commercial market. As a result, the financial return obtained from Government contracts cannot be justified unless additional commercial-market benefits are received.

The current technology-transfer clause actively discourages participation in Government research and development efforts by offering the nonparticipant, at no cost, technical breakthroughs developed by other companies working on low-profit Government contracts. To prevent this technology transferal, high-technology contractors will make a conscious effort to avoid investigating promising areas for Government projects and, if it is at all possible, will use a third-rate technology they can easily share.

---

*Electronics will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

# Standard, yes.
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STD BUS

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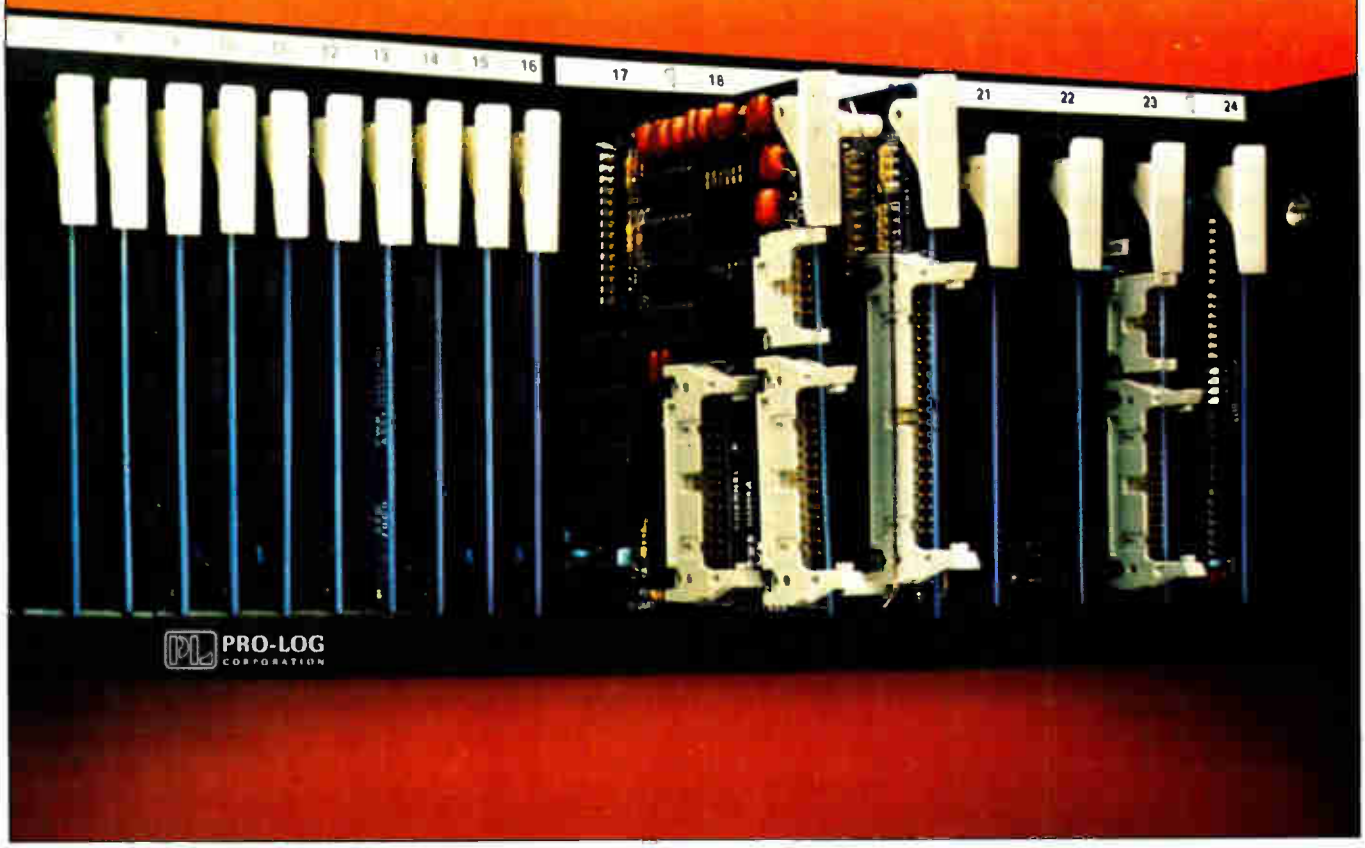


# Meetings

**Compcon Spring,** IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Jack Tar Hotel, San Francisco, Feb. 26–28.

**Robots VI Conference and Exposition,** Society of Manufacturing Engineers (1 SME Dr., P. O. Box 930, Dearborn, Mich. 48128), Cobo Hall, Detroit, March 1–4.

**9th Communications Satellite Systems Conference,** American Institute of Aeronautics and Astronautics (1290 Avenue of the Americas, New York, N. Y. 10104), Town and Country Hotel, San Diego, Calif., March 7–11.

**Spring Engineering Conference,** Society of Cable Television Engineers (1900 L Street, N. W., Suite 614, Washington, D. C. 20036), Copley Plaza Hotel, Boston, March 8–10.

**Southeast Printed Circuits & Microelectronics Exposition,** Cahners Exposition Group (222 West Adams St., Suite 999, Chicago, Ill. 60606), Sheraton Twin Towers Convention Center, Orlando, Fla., March 9–10.

**Informatics and Industrial Development Conference,** Intergovernmental Bureau for Informatics (Dorothy Barry, Shelbourne House, Shelbourne Road, Dublin 4, Ireland), Trinity College, Dublin, Ireland, March 9–13.

**15th Annual Simulation Symposium,** IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Tampa, Fla., March 17–19.

**4th Annual Microelectronics Measurement and Test Conference,** Benwill Exposition Group (1050 Commonwealth Ave., Boston, Mass. 02215), Hyatt San Jose, San Jose, Calif., March 23–24.

**Southcon/82,** IEEE (Robert Myers, Electronic Conventions Inc., 999 North Sepulveda Blvd., El Segundo, Calif. 90245), Expo Center, Orlando, Fla., March 23–25.

**4th International Power Conversion Conference,** Intertec Communications Inc. (P. O. Box 2889, Oxnard, Calif. 93034), Moscone Convention Center, San Francisco, March 29–31.

**Infocon 82,** IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Sahara Hotel, Las Vegas, March 29–April 2.

**Reliability Physics Symposium,** IEEE (David S. Yaney, 837 East Langhorne Ave., Bethlehem, Pa. 18017), Town and Country Hotel, San Diego, March 30–April 1.

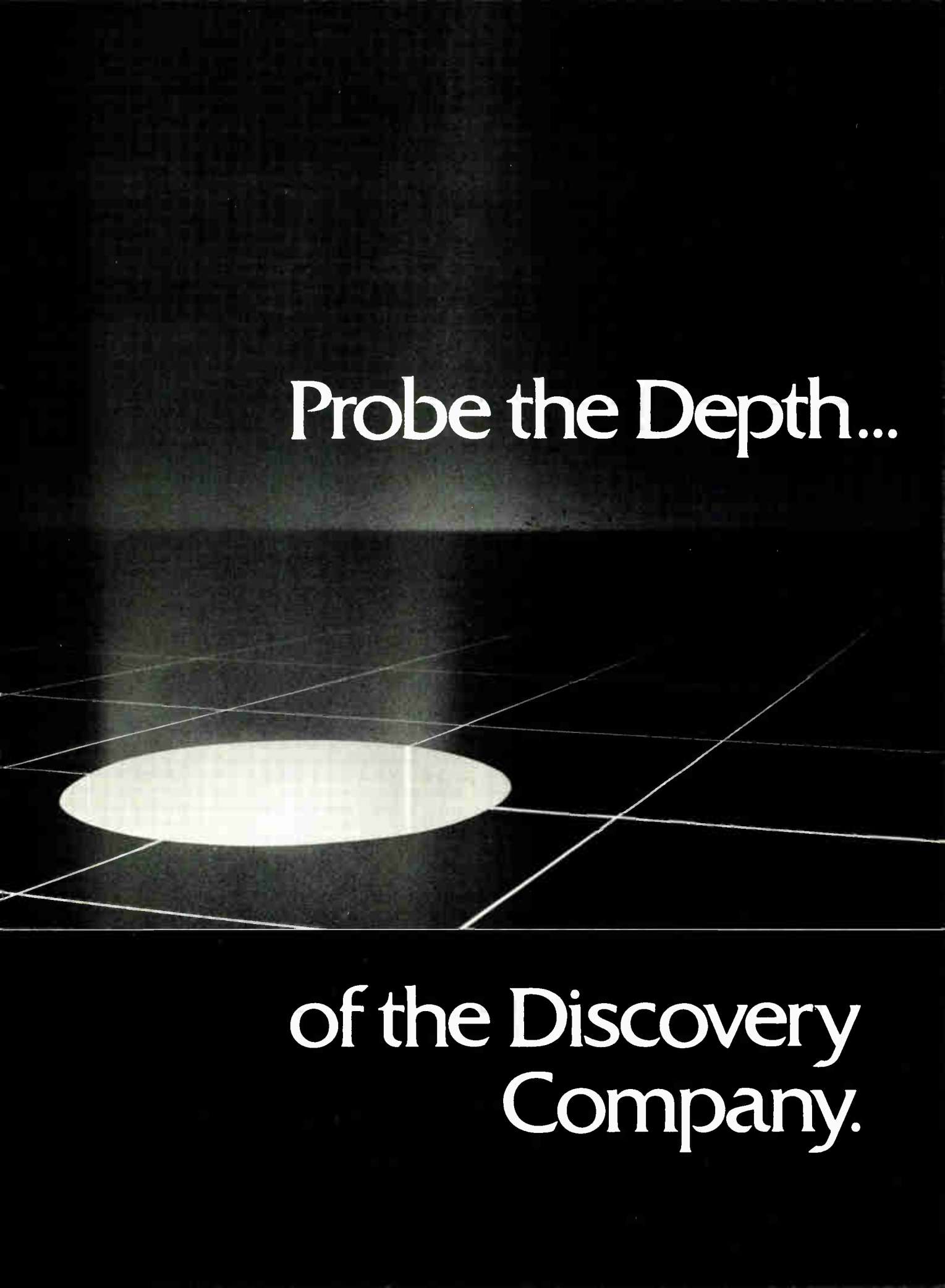
**5th International Conference and Exhibition on Computers in Design Engineering,** Computer-Aided Design Magazine (Alan Pipes, IPC Science and Technology Press, P. O. Box 63, Westbury House, Bury Street, Guildford GU2 5BH, UK), Brighton Metropole Hotel, Sussex, UK, March 30–April 1.

**25th International Electronics Components Exhibition,** Société pour la Diffusion Scientifique et Artistique (Jean-Pierre Duclos, 20 rue Hamelin, F 75116 Paris, France), Parc des Expositions, Paris, France, April 1–7.

## Seminars

**International Invitational Computer Conference,** technical presentations and equipment displays for original-equipment manufacturers, B. J. Johnson & Associates Inc., 2503 Eastbluff Dr., Suite 203, Newport Beach, Calif. 92660. One-day programs will be held in London, March 11; Stockholm, March 18; and Frankfurt, March 23. For information in Europe, contact Tom Lewis at (01) 994 6477 or telex number 8811418.

**8th Annual Reliability Testing Institute,** sponsored by University of Arizona, Ramada Inn, Tucson, Ariz., April 19–23. For information, contact Dimitri Kececioglu, Aerospace and Mechanical Engineering department, University of Arizona, Building 16, Tucson, Ariz. 85721.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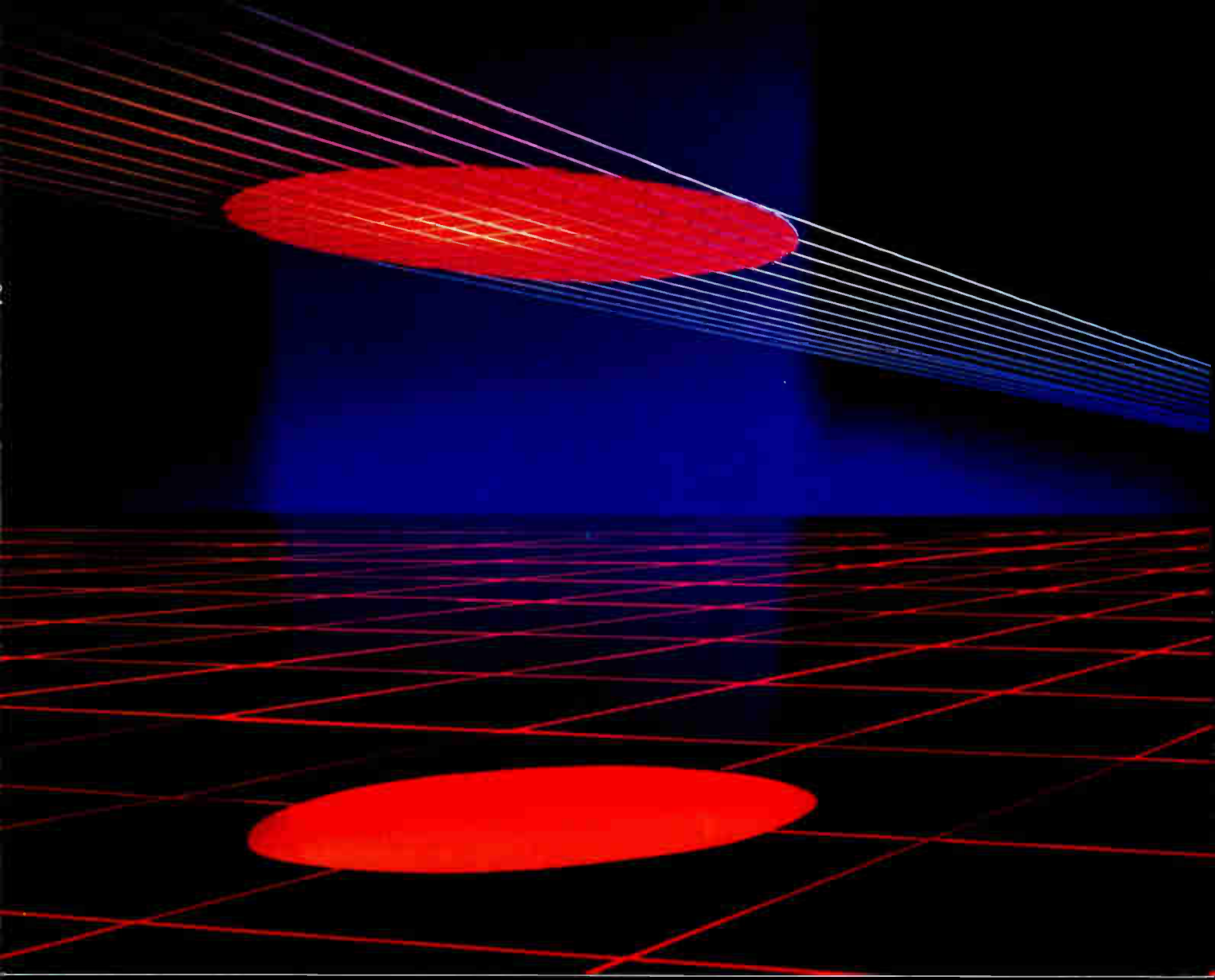

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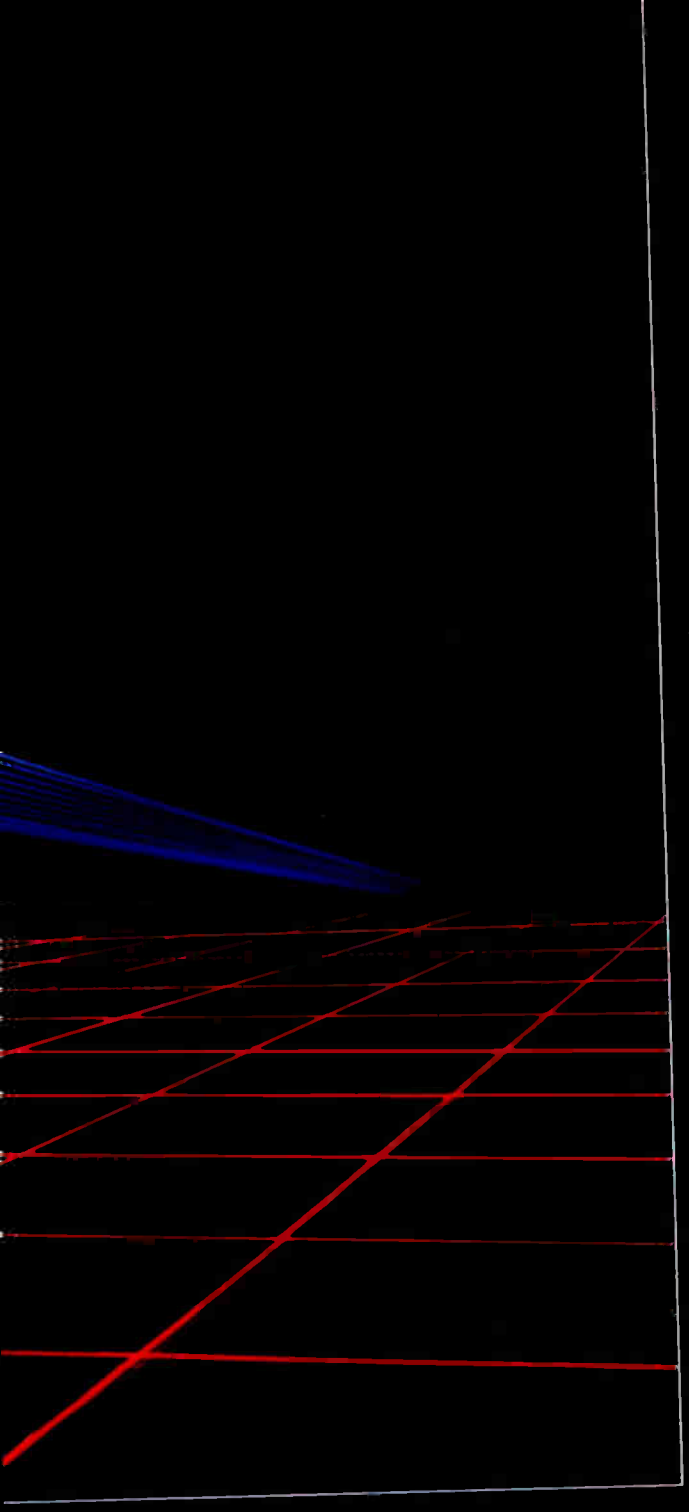

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Circle 32 on reader service card

# Electronics newsletter

## Signal processor controls codec

Codecs relying almost exclusively on digital signal-processing techniques may start replacing analog-based codecs in telephone voice-to-digital conversion during the next two or three years. That's the prediction of researchers at GTE Laboratories Inc. of Waltham, Mass., and at Microtel Pacific Research Ltd. of Burnaby, B. C., Canada. **Their experimental version of a digitally based codec meets AT&T standards for such devices,** they say. It also displays none of the amplification and noise problems of analog codecs, and it requires no precision components since its accuracy depends solely on its sampling rate.

## Intel ready to build CPU for iAPX 286

Industry sources indicate that Intel Corp. has come up with a production schedule for the long-rumored 80286 central processing unit, which forms the heart of the iAPX 286 microsystem. **The 80286, expected to be Intel's answer to Motorola's 68000, is six times faster than the 8086.** As it looks now, Intel should begin shipping samples of the 80286 in the third quarter at $230 each for hundred-piece lots. The first units will have an 8-MHz clock, with 10-MHz units due in 1983.

## Better speech chip attracts bidders

The Votrax division of Federal Screw Works, Troy, Mich., is considering bids from several semiconductor firms to develop and fabricate a second-generation speech-synthesis circuit. Like the predecessor SC-01 single-chip device [*Electronics*, July 3, 1980, p. 43], the new chip will rely upon a phoneme-synthesis approach, **but is said to employ additional filtering and other techniques to vastly improve voice quality.** Dubbed the SC-02A, the new design will offer 256 inflection levels, for example, compared with the two inflection levels possible with the SC-01.

## Mostek to enter logic-array market

Mostek Corp., the MOS firm that made its name in high-volume memory markets, plans to step into the semicustom world of logic arrays with the introduction of several devices by the middle of this year. The Carrollton, Texas, subsidiary of United Technologies Corp. **has created an array-logic product department and will base its new circuits on gate-array technology** from United Technologies' 1½-year-old Microelectronics Center in Colorado Springs, Colo. The center is currently producing devices for internal use by United Technologies' subsidiaries. In addition, this summer, Mostek plans to offer a commercial series of logic products featuring from 300 to 4,000 gates. The devices will be made with double-level–polysilicon complementary-MOS having 3-$\mu$m geometries.

## Standard Microsystems, Fujitsu in patent deal

Continuing its aggressive semiconductor patent-protection policy, Standard Microsystems Corp. of Hauppauge, N. Y., has signed an agreement with Fujitsu Ltd. that provides for worldwide nonexclusive cross-licensing of each company's patents. Standard Microsystems president Paul Richman points out that Fujitsu is the second Japanese company to be licensed (Hitachi Ltd. was first) since his company received a Japanese patent in July 1979 for its n-channel Coplamos MOS structure. **Industry insiders speculate that the next target for Standard Microsystems is Nippon Electric Co.** The company also has granted patent licenses in the U. S. to companies like Texas Instruments, Western Electric, Mostek, and IBM.

# Electronics newsletter

### Chinese chips at 1972 U. S. level

The status of semiconductor technology in the People's Republic of China is roughly equivalent to that of the U. S. in 1972, according to two consultants who recently toured the country. But in some process steps, **such as 5-to-6-$\mu$m features and research and development in chemical-vapor deposition,** the Chinese have reached the 1976 level, says Mel H. Eklund, vice president of Integrated Circuit Engineering Corp. of Scottsdale, Ariz. He and ICE communications director Will Strauss visited mainland China under the auspices of the Bank of America, which seeks a role in financing high-technology industry in the Far East. "What is most incredible," says Eklund, "is that China has bootstrapped itself into its present position with Chinese-built equipment and Western technology."

### Genisco readies graphics system

The first in a line of a graphics systems aimed at original-equipment manufacturers and based on the G-6000 Advanced Display Computer will be unveiled by Genisco Computers early next month. Priced at about $11,000 for single- and $15,000 for dual-channel models, **the G-6150 includes a 16-bit processor, a postprocessor, and a full bit-map refresh memory** of 768 by 512 by 4 bits, providing monochrome or 16 colors. The G-6150 will be the low end of the G-6000 line from the Costa Mesa, Calif., division of Genisco Technology Corp.

### TRS-80 16-bit model to offer multitasking

Radio Shack's long-awaited 16-bit personal computer will soon provide a triple threat to its competition, say top officials at the firm's headquarters in Fort Worth, Texas. By the end of June, the retailer plans to make available a multitasking option that will allow connection of two dumb data terminals to the new TRS-80 Model 16. "In this manner, **the model 16 can grow to the equivalent of three separate computers at a very low incremental cost** to meet a growing user's need," explains Jon Shirley, vice president of computer merchandising at Tandy Corp., Radio Shack's parent company. Radio Shack follows IBM Corp. into the 16-bit era—along with Mitsubishi (p. 56). The new TRS-80 is a dual-processor system built around Motorola Inc's 68000 microprocessor, which provides more than enough power to handle the model 16's maximum 512-K random-access memory. An 8-bit Z80A is used as an input processor. Priced at $4,999, the basic configuration of the model 16 includes a single disk drive, 128-K RAM, and two serial communication ports (one of which can communicate with IBM and other mainframes).

### Addenda

Xicor Inc. of Milpitas, Calif., has built a 16-K electrically erasable programmable read-only memory working off of a single 5-V supply. It expects to start shipping samples of the 32,400-mil² chip in the second quarter, and have production quantities available in the second half. **The part is built in Xicor's proprietary triple-polysilicon process** that gives floating gates with asperities [*Electronics*, Oct. 11, 1979, p. 111]. . . . Ford Microelectronics, a new Ford Motor Co. subsidiary, will be located in Colorado Springs, Colo., **to design, develop, and later produce integrated circuits for the company's aerospace and automotive businesses.** On a 300-acre site near the Air Force Academy, the new operation is expected initially to employ about 70 persons.

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# Clocking technique simplifies structure of image-sensing CCDs

*by J. Robert Lineback, Dallas bureau*

'Virtual phase' design needs but one polysilicon-gate layer, boosting yields compared to those with multiple gates

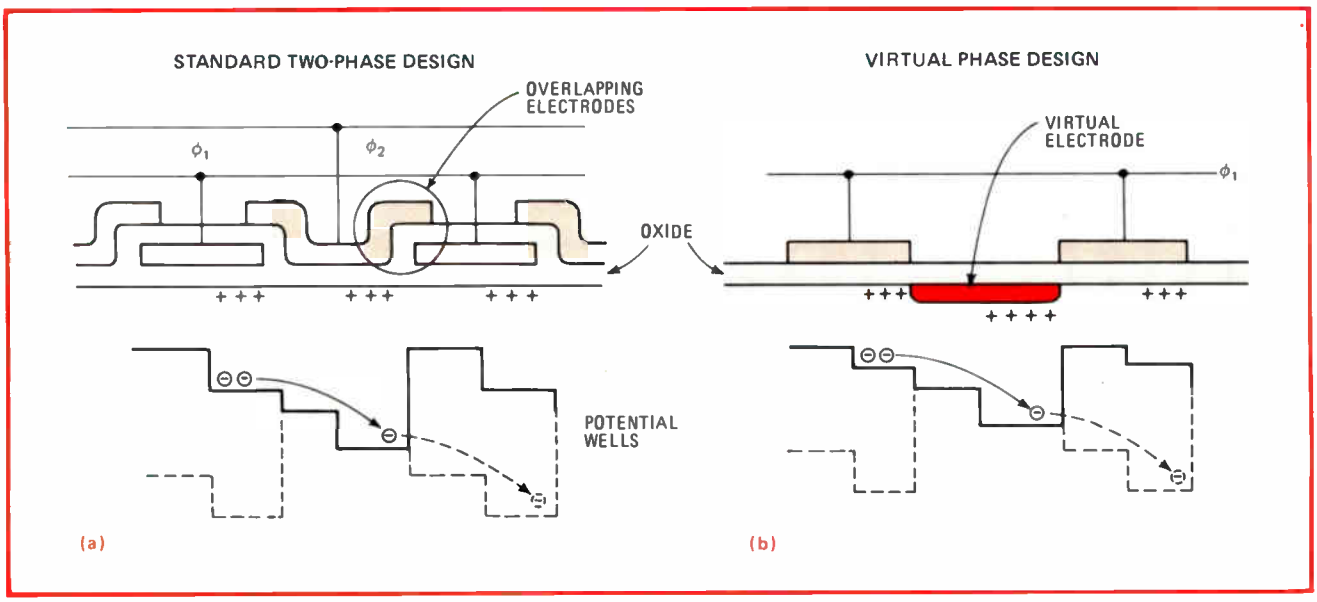
**Using a new** device structure that eliminates the need for two clock phases in charge-coupled devices, Texas Instruments Inc. is unveiling its first commercial CCD image-sensor chips. The patented technology, called the virtual-phase process, enables the Dallas, Texas, firm to manufacture CCD sensors with only a single layer of polysilicon-gate material on the die.

Until now, CCD circuits have required at least two layers of overlapping gates and multiple-clock phases to transfer image data in the form of charge packets. Two gate layers have been necessary because charge packets in CCDs are transferred under the control of phased signals that create potential barriers and wells in the silicon. Electrons generated by the incident light collect in a well and are kept there by a charge barrier. The next clock phase then removes the barrier and allows the data packet to filter across into the next well.

Data transfers, or shifts, are similar in the new virtual-phase structures; however, charge packets move from under the single polysilicon-gate layer to a virtual electrode—a junction gate in the die that replaces the second electrode of the conventional structure in other CCD chips. (See "What is a virtual-phase CCD?" p. 40 and the figure below.)

The virtual-phase structure "makes the device easier to manufacture," says Ron Jascott, marketing manager for imagers and microwave devices. "Inherent in the [two-phased] structure are some problems because of the [gate] overlap that's needed. If the oxide integrity is questionable—pinholes or some other defect—you will get level-to-level shorts. That degrades the yield and drives up the cost."

**Improved response.** Also, the elimination of the two-phase structure improves the sensor's response to blue colors since the light is not absorbed by a second gate layer, notes Eugene F. Rybaczewski, technical staff member of TI's Central Research Laboratory in Dallas, where the new process was developed for TI's optoelectronics operation. The devices work across the electro-




**One layer.** Two sets of gate electrodes control the transfer of charge in a standard CCD. In TI's design, right, an implanted np junction—the virtual electrode—functions as one of the gates. Doping beneath it helps set up potential wells similar to those in the two-gate device.

magnetic spectrum from visible to near-infrared light (about 4,000 to 9,000 angstroms), transmitting in black and white. Filters can be used in order to create color images.

Since the early 1970s, the Dallas firm has been working on CCD image sensors under Government contracts. Two virtual-phase parts, the TC101 and TC102, are its first to be commercially available.

**Family.** The n-channel MOS devices are the beginnings of a family of CCD sensors, says Jon H. Jackson, optoelectronics marketing manager. The 101, which sells for $250 each in lots of 100, has a 1,728-by-1-picture-element configuration of photodetectors. The smaller 102, with 128 by 1 pixels, is $100 in lots of 100.

The 101 is being targeted at facsimile and high-resolution optical-character-recognition applications and can deliver a resolution of 200 points an inch across an 8½-in. page; the 102 is being marketed for high-speed document readers and other applications that do not require the high degree of resolution possible with the denser part.

TI's new parts are currently priced higher than existing two-phase devices like Fairchild Semiconductor's CCD 122, a 1,728-pixel structure selling for $100 each in 100-piece orders. However, Jascott expects the cost benefits of the new technology to really pay off as volumes build up.

## What is a virtual-phase CCD?

In a charge-coupled device, packets of charge generated by exposure to light are transferred in one direction through a series of electric-potential wells and barriers. Two clock phases—and, hence, two sets of gate-electrode layers that overlap—are needed in the standard CCD structure to control this charge transfer, as shown in the cross-sectional diagram on page 39.

The wells are defined in the device by shallow n-type implants in a p-type substrate (indicated by + signs in the figure) that extend under half of each gate. While one set of gates (designated as $\phi_2$) is grounded, the other set (designated as $\phi_1$) receives a positive clock voltage that deepens the potential wells beneath them (dashed lines in the figure). Charge under each of the grounded gates, therefore, spills over into the well immediately to the right.

During the next part of the readout cycle, the roles of the two sets of gates are reversed. The $\phi_2$ gates receive a positive clock pulse, while the $\phi_1$ gates are returned to ground, setting up the well profile shown by the solid lines. This serves to move the charge under the $\phi_1$ gates along to the right. Alternating clock polarities are applied until the entire contents of the CCD is transferred out.

TI achieves a similar staircase-shaped potential well in its virtual-phase CCD by substituting an np junction—the so-called virtual electrode—for one set of gates. A deeper n-type implant both contains and helps move the charge. The single gate layer that remains is clocked betweeen ground and a positive voltage. When the gates are positive, the potential wells beneath them are below the level of the virtual electrode's well. When the gates are grounded, they are above this level, achieving the staircase effect of two-phase clocking.

**-Roderic Beresford**

**Production**

# Gas plasmas yield X rays for lithography

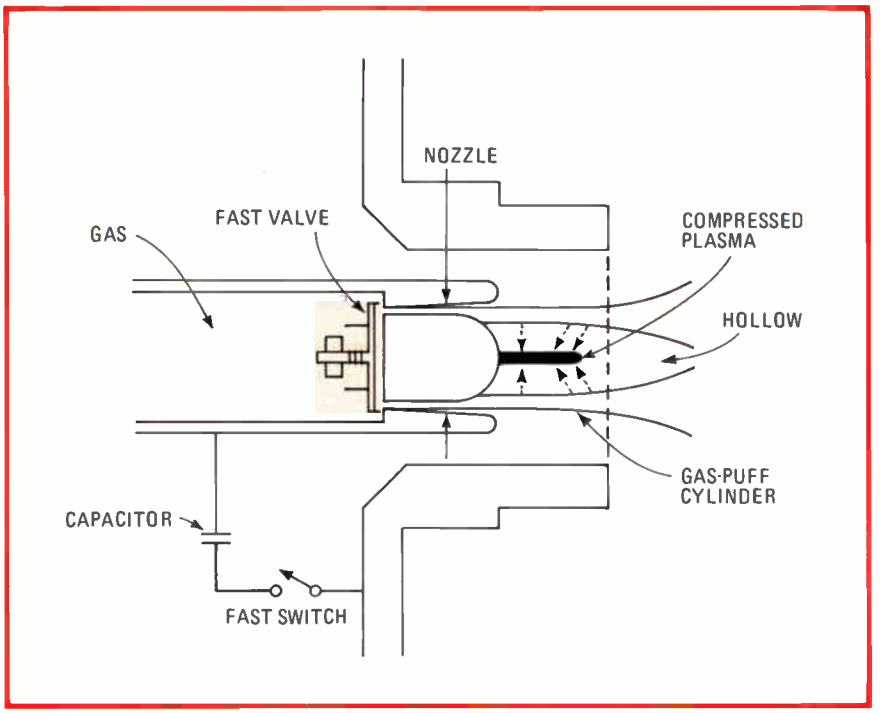
X-ray lithography could take an important step toward commercial reality if a technique for creating the X-ray source itself yields the kind of performance its developers expect. Pulsed-plasma sources, in which electrical energy driven through a gas transforms it into an X-ray–emitting plasma, could be applied in equipment to give it enough throughput to make high-resolution X-ray lithography feasible for production of semiconductor chips.

Two California firms say they have proved out the source using experimental prototypes and now have laboratory models. San Leandro–based Physics International Co.'s Pixi-10 currently is undergoing electrical characterization and will be ready for demonstration within a month, according to senior staff physicist Stephen M. Matthews. Already introduced and ranging in price from $100,000 to $150,000 is another X-ray source, Lexis-II from Maxwell Laboratories Inc. of San Diego.

**Nozzle.** Both models, dubbed gas-puff or gas-jet plasma sources, work by forcing a gas through a special nozzle in short bursts. The nozzle "shapes" the gas into a hollow cylinder (see diagram). The instant before this cylindrical shape dissipates, electrical energy stored in a capacitor bank discharges through the gas, causing it to implode about the cylinder's axis. The resulting energy momentarily transforms the gas into a compressed plasma, which emits X rays at wavelengths determined by the composition of the gas.

Although both companies caution that these sources need at least a couple of years' development before they are ready for the production floor, the benefits of such systems could well be worth the wait. The capital investment they require is a fraction that of a synchrotron, a particle-acceleration–based source that has been used experimentally. That may be the optimum X-ray source, but it carries a multimillion-dollar price tag.

**Bombardment.** In the X-ray source most commonly used at present, electrons bombard a fixed or rotating anode to produce X rays, but this approach suffers from poor efficiency and low output power, asserts Matthews at Physics International. "Even pushing that technology, as Perkin-Elmer is doing, will result in only a barely usable source for production lithography," he predicts. In contrast, the gas-jet solution permits 100 times better efficiency and 20 to 100 times greater output power, which helps trim exposure time and




**Pouf.** In Physics International's design, gas forced through a nozzle briefly assumes cylindrical shape, then collapses into dense, X-ray–emitting plasma when electricity is applied.

so increase throughput, he adds.

Jay S. Pearlman, technical director of the radiation physics department at Maxwell Laboratories, agrees with Matthews. The gas jet's intense output also permits use of thicker, less sensitive photoresists—which provide better resolution—and Pearlman adds that Lexis-II also can handle the very sensitive masks developed for electron-bombardment sources, exposing them in as little as one plasma pulse. Less sensitive resists might take anywhere from 10 to 30 pulses from the gas-jet source. The highest pulse rate either company claims for its source is 1 pulse per second; both, however, agree that 10 pulses per second is an achievable goal.

**Small source area.** Another advantage of the gas-jet systems is their small source area. The area from which X rays are emitted measures only about 1 millimeter in diameter, about a third the average size of the source area in electron bombardment. Finer resolutions are therefore attainable with gas-jet sources, their developers assert. Such sources also require none of the cooling mechanisms needed to keep an electron-bombardment source's anode from melting. At this stage of their development, the major problem facing the designers of the gas-jet source is making their systems reliable for continuous use. **-Linda Lowe**

**Automotive**

# Erasable PROMs slated for Cadillac

After four years of consideration and some 18 months of serious testing, General Motors Corp.'s Delco Electronics division has decided that MOS erasable programmable read-only memories are reliable enough for use in production cars.

Beginning in model year 1983, 16-K MOS E-PROMs will replace fusable-link bipolar PROMs in all Delco engine-control systems supplied for gasoline-powered V8-engined Cadillacs, according to Robert J. McMillin, Delco director of engineering, Kokomo, Ind. The move could pave the way for eventual use of E-PROMs in all of GM's gasoline cars, McMillin confirms. This phase-in could start as soon as model year 1984.

Delco's current-generation Computer Command Control System contains most of its memory code in mask ROM, but also employs an 8-K bipolar PROM to provide the final calibration code that tailors the system to a particular combination of body and power train. The Cadillac system uses two 8-K PROMs.

By replacing the PROM with an E-PROM, Delco hopes to improve flexibility and reduce scrap. "Right now, if a car division decides to change its calibration, we end up scrapping the PROMs that we've blown," McMillin explains. An E-PROM can be erased by exposure to ultraviolet light and reprogrammed as necessary. The MOS devices are also significantly cheaper per bit than the bipolar parts, their vendors point out.

**Concern.** Delco had been concerned about the E-PROM's ability to retain memory for the life of an automobile. But recent high-temperature operating tests on 2716-type devices from several vendors show that the parts could live well beyond 20 years when used in the passenger compartment, says Bruce Myers, who is a senior product engineer in Delco's product assurance department.

Because of the potentially large volumes involved—more than 3 million GM cars with Computer Command Control were sold last year—semiconductor vendors are following Delco developments closely. Delco acceptance of E-PROM technology is "a major breakthrough for us in the nonvolatile memory area. It's going to amount to some huge dollars down the road," says David Ford, strategic-marketing manager for MOS memory at Motorola Inc.'s Austin, Texas, MOS integrated-circuits group. The prospect of a GM switchover to MOS E-PROMs is already causing some price cutting by bipolar PROM suppliers, Delco sources report.

E-PROM devices from four vendors—Motorola, Intel, Texas Instruments, and Hitachi—are currently undergoing qualification tests, says McMillin. Assembly of the Cadillac

systems should begin this summer.

Some vendors see Delco's E-PROM endorsement as a stepping stone to the firm's eventual use of the electrically erasable PROM, which is under development at a number of semiconductor houses. Delco is also considering development of a custom device that would integrate the E-PROM on chip with a mask ROM.

**Other plans differ.** Though GM competitors Ford Motor Co. and Chrysler Corp. both are using E-PROM for development purposes, neither currently has plans to employ the MOS devices in production engine-control systems. Ford's current-generation EEC-III system has all its calibration code in ROM, and Chrysler's Spark Control Computer relies on bipolar PROM for fine-tuning calibration. But PROM scrap costs due to calibration changes have not been high enough to justify consideration of using E-PROMs as replacements, says Gary A. Chunn, manager of power-plant electronics at Chrysler's Huntsville, Ala., Electronics division. **-Wesley R. Iversen**


## Japanese personal computer takes different tack for U. S.

For the U. S. personal-computer market, Casio Inc. is taking a different tack with its FX-9000P machine from the one it used in its home market in Japan. On sale there since March 1981 for $720, the 8-bit computer was aimed at a broad market that welcomed low price and simplicity [*Electronics*, March 24, 1981, p. 82]. In the U. S., however, it is targeting the FX-9000P at the statistical, business, engineering, and scientific fields, says Richard L. Grogan, product manager for Casio's Personal Computer division, located in Fairfield, N. J.

It carries a $1,199 retail price, far below the $3,250-and-up price of the market pacesetter, Hewlett-Packard's HP-85, says Grogan. It comes with a built-in 5½-inch cathode-ray tube and a 67-key keyboard. To be sold through Casio's calculator, watch, office-machine, and musical-instrument network of representative and retail outlets, the FX-9000P will be available later this quarter with some 30 software packages written for Casio's version of Basic. It is also possible to convert application software from such best-selling U. S. personal computers as the TRS-80, Casio claims.

The machine has random-access memory to hold data and programs, plus battery backup. Programs can be stored for three years without external power. The basic 4-K bytes of complementary-MOS RAM can be expanded to 32-K bytes in 4-K-byte packs that sell for $189 each ($111 in Japan). **-Larry Waller**

### Microprocessors

## Chip implements military instruction set

By next August, prototypes will be available of a new high-speed microprocessor chip that could be the military's "chip of the future." Developed by the Fairchild subsidiary of Schlumberger Ltd., Mountain View, Calif., the device, along with the peripheral chips that enhance its processing power, will be the first microprocessor to implement the MIL STD 1750A instruction set as its native language.

This standard, adopted in July 1980 and currently implemented mainly with TTL packages on printed-circuit boards, spells out a computer architecture that uses a 16-bit instruction set and is optimized for such tasks as floating-point processing and real-time calculations. It was developed several years ago to help slow down the proliferation of microprocessor-based systems in the military and the software support they each required, points out Jeffrey Pesler, a project engineer and member of the staff of the deputy program manager for the F-16 fighter program at Wright-Patterson Air Force Base, Dayton, Ohio. Pesler is also the project engineer for MIL STD 1750A and is guiding the effort at Fairchild, which is building its chips to go aboard the F-16. General Dynamics is the prime contractor for the F-16.

However, just how soon military systems designers will accept the new Fairchild chip remains to be seen. "We're not going to be jamming this chip set down anyone's throat, but many other military project managers have expressed the desire to have a MIL STD 1750A processor," says Pesler. He will be conducting twice-yearly forums on the instruction set and believes there is enough interest in this device for it to become the military's universal 16-bit microprocessor.

**Isoplanar.** At Fairchild's advanced research and development laboratory, the processor is being implemented in the company's 3-micrometer advanced Isoplanar integrated injection logic, $I^3L$-II. It has a designed clock rate of 20 megahertz, will include single- and double-precision arithmetic, and will manipulate 32- and 48-bit floating-point num-


# Look to the linear leader. Product trends from Texas Instruments.

**Here's what happened in '81.** For op amps or comparators, voltage regulators or data acquisition devices, line drivers or receivers, peripheral or display drivers — even special function ICs, *look to the linear leader.*

**NFET Op Amps/Comparators:** TL091 series of single, dual, and quad op amps. The industry's first to combine the advantages of N-channel JFET inputs for high-impedance single-supply operation with low distortion bipolar outputs on a single monolithic chip. TL311 too, the first NFET comparator.

**Voltage Regulators:** *Brand new* TL783. First adjustable, high-voltage DMOS regulator — shatters 40-V bipolar barrier — handles input to output voltage differentials up to 125 V — delivers up to 0.7 amps output current. Another innovative product is the TL780 regulator, available in +5, +12, +15-volt versions with output tolerance of +/− 1% at 25°C. Improved line and load regulation, ripple rejection, and temperature coefficient.

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**EIA STD Line Circuits:** First transceiver to meet RS422: SN75176. First repeaters, too: SN75177 and SN75178. Low power requirements, high impedance to the bus, thermal shutdown protection, positive and negative current limiting, 60-mA driver output capability. Designed for multi-point bus (party-line) applications, for data rates to 4 MHz, distances to 4000 feet.

**Switched-Capacitor A/D Converter:** Another first. TL520. 8 multiplexed inputs, 8 bit resolution, +/− ½ LSB linearity error, operates from a wide 2.5-6.0V supply range, low operating current — 500 µA at 5 V. Uses 9 capacitors and 26 switches to achieve 50-µs conversion speed.

**V/F Display Drivers:** SN75512, SN75513. 12-bit vacuum-fluorescent display drivers featuring 60-V, 25-mA totem-pole outputs, serial data output for cascading devices. High speed serial data and TTL-compatible inputs, optional latch (SN75512) or reset (SN75513) capabilities.

**Special Functions:** TL195. First NFET Sample and Hold Circuit. True single-supply operation, input and output common mode ranges include $V_{CC}$, high impedance inputs, 10-µs acquisition time. Offset null and easy compensation of hold-step error for true sampling of low-mV signal levels.

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bers. The first prototypes are not scheduled to be put into silicon until August, but the design of the F9450, as it is referred to by Fairchild, is nearly complete and scheduled for a critical review next month.

**Fast.** The design specification calls for the F9450 to perform a 16-by-16-bit multiplication in 1.8 microseconds, which would make it twice as fast as the fastest currently available microprocessor, Fairchild's F9445 introduced last summer and now available in sample quantities. It should reach a level of 0.7 million instructions per second (MIPS) when measured against the Air Force's avionics Dais (digital avionics instruction set) benchmark with the inclusion of a 16-bit floating point. Without the floating point, in a measurement against the Air Force's missile Dais benchmark, the 64-pin dual-in-line-packaged processor will operate at 1.5 MIPS.

"After we deliver the prototypes to General Dynamics, our objective will be full JAN [Joint Army-Navy] qualification of the 9450," asserts Ron Byrne, Fairchild's bipolar microprocessor marketing manager. He notes that the 9450 will be accompanied by a number of support chips, including three for a memory management function (the 9451) and six to act as a block-protect random-access memory (the 9452).

**Boost.** Both circuits will be derived from Fairchild's 9480 gate array and implemented in its present $I^3L$ process. The memory management unit will let the F9450, which normally addresses 64 kilowords, address one megaword.

The MMU will be composed of four F93479 2-K static RAMs and one 54F373 latch. It will provide write protection in blocks of one kiloword, plus protection in a logical space of four kiloword pages for the access key, writing, and executing.

In addition, the unit will contain two maps: an instruction and an operand map. The block-protect RAM requires the gate array and two F93479 RAMs. It implements write protection for the central processing unit and direct memory access.

The CPU, the MMU, and the block-protect RAM will each dissipate less than 5 watts and will be radiation-hardened against a total dosage of $10^5$ rads. **-Martin Marshall**

## News brief

**Experiment demonstrates wave nature of electrons**

A basic experiment on the wave nature of electrons—one that has eluded physicists for 50 years—has been carried out at the IBM Research Laboratory in Zurich, Switzerland. It involves the tunneling of electrons from within metal through a narrow vacuum region. The electrons leave the metal with less energy than that required for a particle to escape, something they could only do as waves and not as the small, hard particles envisioned in classical physics. The modern view of electrons having properties of both particles and waves, called quantum mechanics, was formulated in the late 1920s.

The tunneling occurred in the vacuum between two electrodes, one a needle point and the other a flat platinum plate, a few angstroms apart. This apparatus was floated in a magnetic field to reduce external vibration, which was the main problem encountered in previous attempts to carry out this experiment in a vacuum. The researchers point out that with vacuum tunneling many important features of the growth and behavior of ultrathin insulating layers on metals and semiconductors can be investigated with spatial resolution at the atomic level.

**Packaging**

# Leadless carrier cuts noise for ECL

For computer-system designers who use the highest-speed logic chips, the problem is simple: not to let the chip package affect the operation of the chips themselves. For Digital Equipment Corp. and Sperry Univac, this problem was one of preventing inductance-coupled switching noise from showing up on leads where it should not be, and it led them to embark on a joint development program that has resulted in a new ceramic leadless chip-carrier, one with four layers instead of three. The extra layer is a ground plane that cuts noise by reducing the inductive coupling among the package leads.

The two companies knew they had a problem when they put one of Motorola's 10,000 series emitter-coupled-logic chips into a standard type A leadless ceramic chip-carrier and found that the noise induced on an unswitched (high-state) lead reached the 200-millivolt noise threshold of the logic. Actually, the test chip (with a 200-megahertz operating speed and a 2-nanosecond propagation delay) was bonded into a 68-pad chip-carrier. This combination was inserted, in turn, into a 68-terminal soldertail socket from Amp Inc. Seven outputs of the integrated circuit were switched and an eighth was left unswitched. The noise spike induced on the eighth lead was caused by package-lead inductance and the high rate of change in current due to the simultaneous switching.

**Extras.** In part, coupled noise was reduced by increasing the number of bonding wires to each ground from three to four, says Bruce Weaver, engineering supervisor at DEC's Marlboro facility. More important, however, was adding the ground plane to the chip-carrier.

Standard leadless ceramic chip-carriers have three layers: one with conductors, a bonding-pad layer, and the bottom ceramic surface. The ground plane was inserted between the bottom surface and the bonding-pad layer, according to Weaver. Moreover, ground paths on the bonding-pad layer were thickened to provide an additional ground-plane effect, and four ground pads were added to the bottom surface.

Four extra pins also were added to the socket. When the chip-carrier is placed face down into a socket, the socket's metal cover mates with the

# Type MG Precision High Voltage Resistors from CADDOCK deliver 6 big advantages:


## 1. For maximum design flexibility, there are 19 standard models with 10 voltage ratings in the Type MG 'family'.

The Type MG family of high voltage resistors includes a selection of voltage ratings from 600 volts to 30,000 volts in various resistor lengths to provide maximum flexibility in the design of high voltage assemblies.

In addition to this wide range of voltage ratings, the Type MG family provides a selection of resistor diameters at many of the standard voltage ratings, as illustrated by the three models of 4,000 volt, 1-inch long resistors shown here.


Important performance specifications for all Type MG resistors include:

- Full power rating to + 125°C.
- + 225°C maximum operating temperature.
- Resistance values that cover the range from 200 ohms to 2000 Megohms.

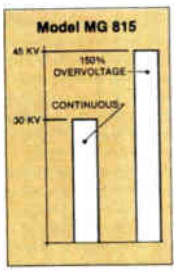
## 2. The standard TC of 80 PPM/°C and resistance tolerances from 1.0 % to 0.1% combine to improve circuit accuracy.

Through the full range of resistance values from 200 ohms to 2000 Megohms, the Type MG resistors maintain a temperature coefficient of 80 PPM/°C over the range from − 15°C to + 105°C, referenced to + 25°.

The combination of precision and low TC achieves a significant improvement over other high voltage resistor technologies, particularly in the higher resistance values.

## 3. Overvoltage rating of 150% is standard for all models.

Every model of the Type MG resistors has a *standard* overvoltage/overload rating of 1.5 times the maximum working voltage where this level does not exceed 5 times the rated power. As an example, in the Model MG 815 this capability provides for short-term overloads as high as 45,000 volts.




And for even tougher applications, special factory conditioning can boost the maximum *continuous* operating voltage of many models to 160% above the standard specifications.

## 4. Matched resistor sets with 0.1% ratio tolerances and TC tracking as close as 10 PPM/°C from -15°C to +105°C.

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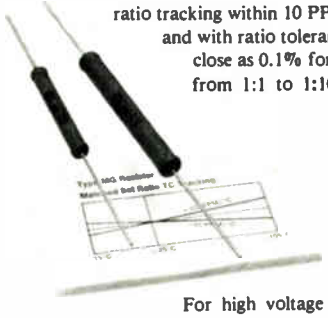
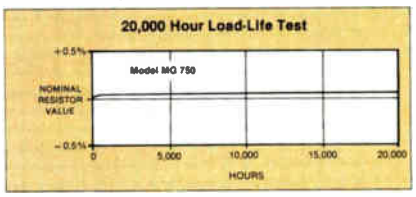


For high voltage divider applications, 1% ratio tolerance is standard.

## 5. Extended-life stability that is typically better than 0.02% per 1000 hours.

20,000 hour *continuous* load-life tests have proven the exceptional stability of Caddock Micronox® resistance films. This graph illustrating the 20,000 hour test results of the 10,000 volt rated Model MG 750 shows extended-life stability well within 0.02% per 1000 hours.




A complete data summary of these test results is available on request.

## 6. Exclusive Non-Inductive Performance.

Caddock's Exclusive Non-Inductive Design is the answer wherever there are special requirements for excellent high-voltage pulse fidelity and wide bandwidths.

To keep the inductance to an absolute minimum, the special serpentine pattern provides for neighboring lines to carry the current in opposite directions to achieve maximum cancellation of flux fields over the entire length of the resistor.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## Electronics review

carrier's four bottom-surface pads, providing still another ground path through the four pins, says Weaver. These modifications produced an overall induced coupled noise to an unswitched output of 122 mV, well below the 200-mV level, he notes.

**Clip-ons.** Sperry has also attached the modified chip-carrier to printed-circuit boards with soldered-on metal clips, a common attachment method that the company has used for small- and medium-scale integrated ECL 10K circuits. The clips provide roughly the same reduction in noise gained by adding four ground pins to the socket.

The new four-layer ECL chip-carrier is available from Kyocera International Inc., San Diego, which worked on the project with DEC and Sperry. **-Jerry Lyman**

## Robotics

# Automaking robots pose problems

Though Japanese automakers seem to be happily embracing industrial robots, an engineer at one of the Big Three U. S. automakers has a jaundiced view. Robots still are not ready for prolonged periods of work in a factory environment, said Dan Kuckens, an electrical design engineer at Ford Motor Co.'s Milpitas, Calif., assembly plant.

Speaking at a panel discussion on industrial robots at a technology conference sponsored earlier this month in San Francisco by the New York-based Financial Analysts Federation, Kuckens summarized the results of 10 years of personal experience with 13 robots used for spot welding. Eight work on the front ends of Escort and Lynx cars and five work on trucks.

He characterized some of the problems with the $100,000-per-robot installation as horrendous. When a robot became "ill," repairs could take as little as an hour or as much as a day and a half, depending on what was wrong. And when a robot went down, it was often neces-

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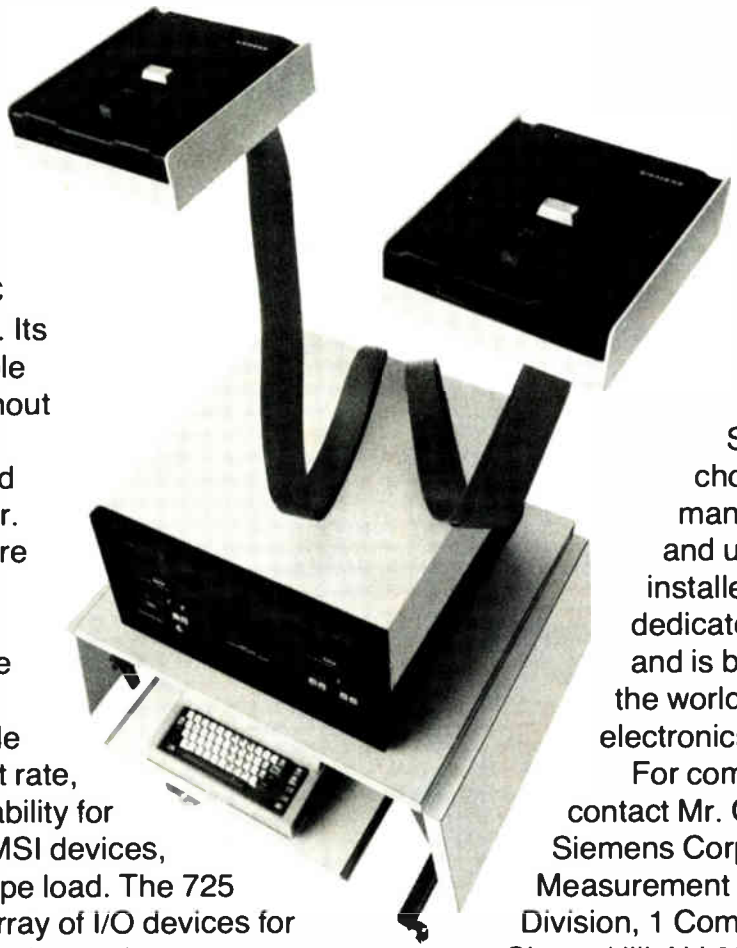
# Two heads are better than one.



The Model 725 IC Tester is multiplexed. Its two heads offer double testing capability without double testing cost. Start with both, or add the second head later.

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## The Siemens 725 Multiplexed Digital IC Tester.

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sary to replace it with two human welders, which can lead to labor-related problems for top management. A staunch defender of robots on the panel, Philippe Villers, president of Automatix Inc., Burlington, Mass., said that older robots may be failure-prone. But Kuckens said 8 of Ford's 13 robots were only a year old.

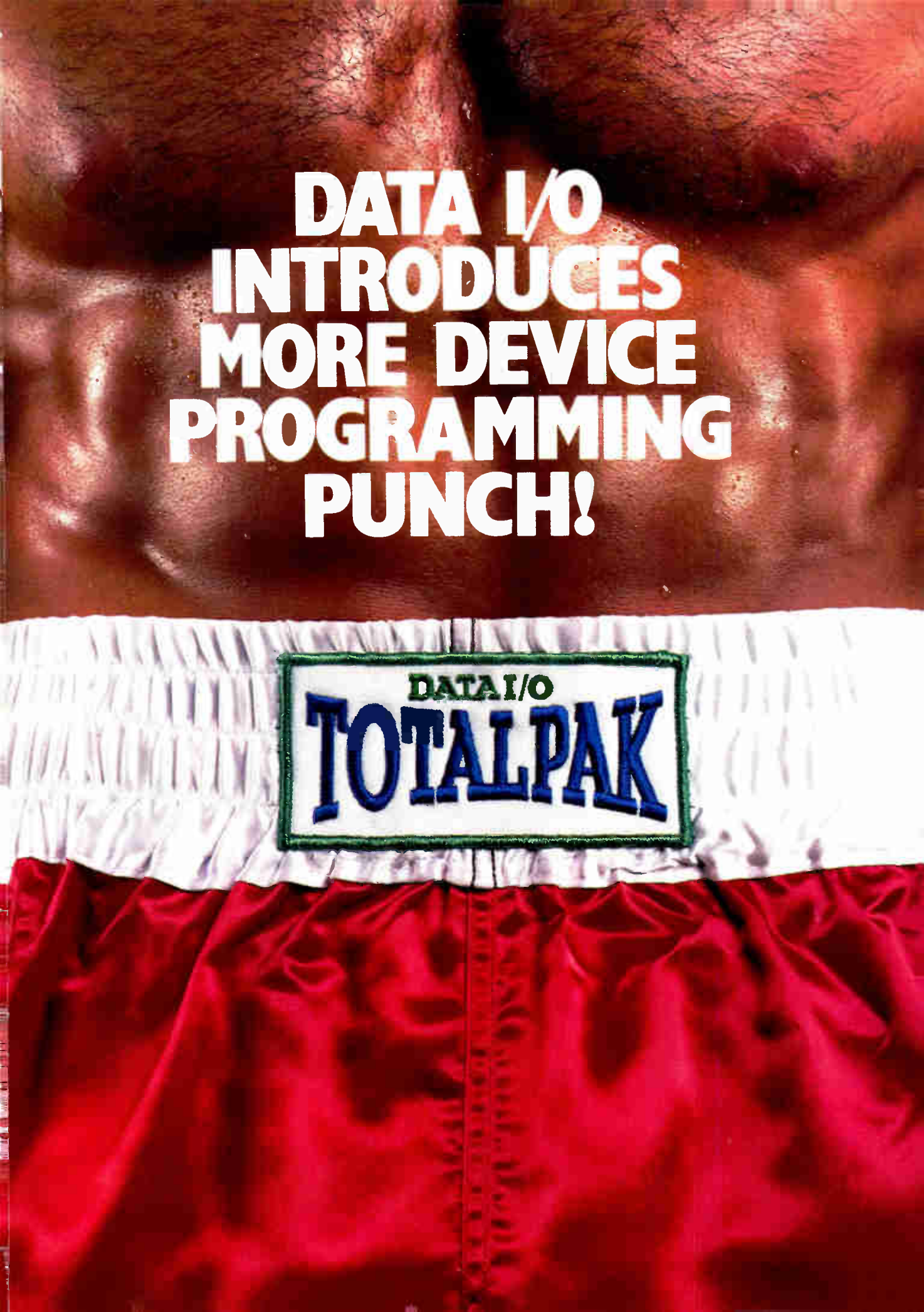
The breakdowns, he said, may have occurred because the robots were not designed to cope with the prolonged welding periods demanded in U. S. assembly plants. Nevertheless, Ford is firmly committed to introducing automation into its factories, as are all U. S. automakers.

Part of the problem, according to Kuckens, is that U. S. plants are not designed to accommodate robots. Auto plants in Japan are designed with robot stations in mind.

Training assembly-line production workers to work with robots also poses difficult challenges. Workers in U. S. plants view robots as a threat to their employment security and bargaining power; Japanese workers are anxious to move these automatons into tedious, laborious tasks so they can be assigned to less strenuous, more challenging jobs.

**Japanese interest.** As revealed during the panel discussion, the commitment by Japan to the aggressive pursuit of robotics is not unlike its dedication to dominate the automotive and consumer-electronics industries. Its Ministry of International Trade and Industry (MITI) has initiated a program to supply $150 million in the next seven years to develop intelligent robots. Also, an organization has been set up by the government that leases robots to industrial concerns at low rates.

Although Japan intends to market robots in foreign countries within several years, only 15% to 20% of the total output is expected to be exported by 1985. More than 100 Japanese robot manufacturers are busy in this new technology, compared with less than 20 in the U. S. Some forecasters predict Japan will have as many as 1 million robots in their assembly plants by the year 2000. **-Howard Bierman**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# DATA I/O
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TOTALPak 1 is a universal NMOS memory programmer that can be used to program NMOS EPROMs or Intel single-chip microcomputers with on-board EPROM. TOTALPak 1 may be used as a stand-alone programmer or used interactively with your terminal or microprocessor development system.

TOTALPak 1's RS-232C serial port makes it compatible with a wide variety of peripherals, and its standard remote control feature allows for data manipulation and control by a host system.

TOTALPak 2 enables you to program all currently available NMOS EPROMs and it has enough built-in additional capability to program future EPROMs up to 32K x 8. TOTALPak 2's standard remote control, 26 data formats and RS-232C serial port give you the ability to interface directly with all popular development systems and peripheral equipment. TOTALPak 2 is easy to operate and prompts the operator in plain English via a 16 character alpha-numeric display.


TOTALPak 3 handles virtually all of your MOS and bipolar programming needs. Remote control, 26 communication formats and RS-232C serial port make TOTALPak 3 compatible with all popular development systems and peripheral hardware. The System's seven-socket, software selectable module programs more than 250 devices and replaces more than a dozen individual programming paks. This means that you can select the best PROM for each application and second-source for the best price and availability.

TOTALPak 3's easy to read, 16 character display prompts the user in plain English and displays data in hexadecimal, octal and binary.

| Comparison Chart | TOTALPak 3 | Competitor #1 | Competitor #2 |
|---|---|---|---|
| MOS and Bipolar programming capability | 250 plus devices | 250 plus devices | 250 plus devices |
| Personality modules required in addition to basic package | NOT REQUIRED | 11 | 17 |
| Socket adapters and configurators required in addition to basic package | NOT REQUIRED | 52 | 38 |
| Data formats | 26 | 13 | 17 |
| Standard RAM | 8K x 8 | 4K x 8 | 4K x 8 |

TOTALPak 3 combines our new 29A programmer with our unique UniPak.

# THREE COMPLETE DEVICE PROGRAMMING SOLUTIONS. NO NEED FOR ADDITIONAL HARDWARE.

| Comparison Chart | TOTALPak 1 | Competitor #1 | Competitor #2 |
|---|---|---|---|
| NMOS programming capability | 50 plus devices | 50 plus devices | 50 plus devices |
| Microcomputer programming capability | YES | YES | YES |
| Personality modules required in addition to basic package | NOT REQUIRED | 4 | 13 |
| Socket adapters and configurators required in addition to basic package | NOT REQUIRED | 5 | 10 |
| Data formats | 6 | NONE | 17 |
| Standard RAM | 2K x 8 | NONE | 4K x 8 |

TOTALPak 1 combines our new Model 20B with a socket adapter for Intel single-chip microcomputers.

## Programs EPROMs and microcomputers at a price that puts the competition on the ropes.

| Comparison Chart | TOTALPak 2 | Competitor #1 | Competitor #2 |
|---|---|---|---|
| MOS programming capability | 50 plus devices | 50 plus devices | 50 plus devices |
| Personality modules required in addition to basic package | NOT REQUIRED | 3 | 8 |
| Socket adapters and configurators required in addition to basic package | NOT REQUIRED | 9 | 11 |
| Data Formats | 26 | 13 | 17 |
| Standard RAM | 8K x 8 | 4K x 8 | 4K x 8 |

TOTALPak 2 combines our new 29A programmer with our MOSPak.

## Universal EPROM capability for today's devices and the EPROMs of the future.


## The only universal MOS and bipolar programmer that programs more than 250 devices without extra hardware.

# LOOK AT THE REAL COSTS.

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# Washington newsletter

**Glenn to blast technology policy**

Sparks are expected to fly on Feb. 24 when Sen. John Glenn (D., Ohio) critiques President Reagan's science and technology policies. The occasion will be Glenn's keynote address at the 1982 Conference on U. S. Technology Policy sponsored by the Institute of Electrical and Electronics Engineers at Washington's Mayflower Hotel. **The former astronaut and Marine Corps pilot is believed to be building toward a 1984 bid for the Democratic presidential nomination.** Speakers to follow Glenn at the conference include presidential Science Adviser George A. Keyworth; Rep. Don Fuqua (D., Fla.), chairman of the House Science and Technology Committee; John W. Gibbons, director of the congressional Office of Technology Assessment; John J. Slaughter, director of the National Science Foundation; and Courtland D. Perkins, president of the National Academy of Engineering.

**Lamps copter cost doubled to $6 billion**

Production costs for the Navy's Lamps Mark III antisubmarine-warfare helicopters are now estimated to hit about $6 billion, about double the original 1976 estimates. Capt. Joseph M. Purtell, manager of the Naval Air Systems Command program, says the Light Airborne Multi-Purpose System's costs break down into about $4 billion for 204 of the Sikorsky SH-60B helicopters and $2 billion for 105 of International Business Machines Corp.'s ASW systems. Even though some system capabilities were dropped to hold down costs, **Purtell attributes more than half the price escalation for the electronics-laden choppers to inflation,** with another third the result of bad estimating. Limited initial production of Lamps III was approved last year [*Electronics*, Dec. 15, p. 63]. New cost-control wrinkles sought in production contracts now being negotiated include a 50:50 sharing between the Navy and contractors of cost overruns and underruns, plus tougher reliability standards that will require IBM and others to screen 100% of components from subcontractors.

**EIA wants standards set by FCC, not by marketplace**

The Electronics Industries Association is urging the Federal Communications Commission to set a single technical standard for a-m stereo radio from the start, another for teletext, and a third for multichannel sound. In adopting its position officially, the EIA's Consumer Electronics Group **rejected the tack favored by some FCC commissioners, the so-called competitive marketplace approach,** under which consumer reponse would determine which system or systems should prevail. The group has also formed a new Personal Electronics division that pulls together manufacturers of personal computers, calculators, and electronic games. John McDonald of Casio Inc. is chairman of the new division.

**$2.2 billion contract for B-1B bomber goes to Rockwell**

California's Rockwell International Corp. will get more than $2.2 billion from the Air Force to proceed with full-scale development of the B-1B bomber. **One $886 million contract covers the costs of building the first of the projected fleet of 50 planes,** plus the purchase of specialized electronics and other strategic materials for future planes. The second $1.3 billion award is for final B-1B design and for modification and test flights of two of the four original B-1 prototypes now in storage.

# Washington commentary

## AT&T: who goes where from here

Few in the national capital's telecommunications community, including the Congress, give much credibility to William H. Diefenderfer's forecast last week that no new telecommunications law will emerge from this Congress. Diefenderfer, 36 and chief counsel for the Senate Commerce, Science, and Transportation Committee, said in a New York seminar that a telecommunications bill pending in the House "would be unacceptable to the Senate" because it is "anticompetitive," among other things.

The House bill, H.R. 5158, introduced by Colorado Democrat Timothy Wirth, chairman of the telecommunications subcommittee, is unquestionably tougher on controlling the future actions of American Telephone & Telegraph Co. than its counterpart passed earlier last year by a Republican-controlled Senate [*Electronics*, Nov. 17, 1981, p. 52]. "But the differences in those bills don't mean that legislation won't be passed," says one House committee official. "Diefenderfer is just playing political games." If that estimate is correct, Diefenderfer may well be the loser.

### Pressures on Congress

With the possible exceptions of the Justice Department and AT&T, which have settled their differences, support for a new law is coming from every quarter of government, industry, and the public in general. "Pressures to keep local telephone rates down, the quality of service up, and the domestic market in the hands of domestic manufacturers are already strong and getting stronger," notes the House committee source. No member of either chamber wants to see these telecommunications features changed by a "worst-case" scenario (see p. 73) that would be unacceptable to an electorate finally awakened to the issues by the AT&T antitrust settlement proposed in early January. Businessmen and consumers, voters all, are running scared in the face of the reports of possibly major rate hikes in local telephone rates.

"You're going to have legislation pretty quickly," predicted Continental Telephone Co. chairman Charles Wohlstetter before the same New York seminar. Continental is the fourth largest U. S. common carrier. Robert C. Hall, president of Satellite Business Systems in McLean, Va., also favors legislation to deal with the local rates issue and close possible loopholes in the AT&T and Justice Department settlement.

What disturbs a number of potential AT&T competitors who have read the proposed antitrust settlement is the substantial amount of time left to AT&T to restructure itself and continue dealing with its divested operating companies. A second disturbing consideration is the three post-settlement moves taken by the giant company within a mere two weeks of the Jan. 8 announcement.

### Time is on AT&T's side

Wide publicity has been given to the 18 months that AT&T has for divesting itself of its operating companies—except the two it may keep because of having only a minority interest in them: Cincinnati Bell of Ohio and Southern New England Telephone of Connecticut. But beyond that, the settlement also orders AT&T to provide "until September 1, 1987 . . . on a priority basis all research, development, manufacturing, and other support services" requested by the operating companies.

What's more, each operating company has until Sept. 1, 1984, before it must begin offering unbundled, tariffed interconnections to AT&T competitors. They then have another year to implement that service on one third of their interexchange lines and until Sept. 1, 1986, before they must offer it at all end offices.

AT&T's post-settlement moves also indicate the company has three priorities on the technology side. The first is to accelerate the creation of its fully separated subsidiary so as to begin marketing its revitalized Advanced Communications Service as quickly as possible. The subsidiary concept was approved earlier by the Federal Communications Commission in its 1980 decision in the Second Computer Inquiry.

The second is another hard drive before the FCC to market its Advanced Mobile Phone Service, despite congressional and FCC reservations about AT&T's entry into the cellular land-mobile marketplace [*Electronics*, Jan. 13, p. 97]. That drive may stall, for the FCC now seems to regard cellular land-mobile service as a local one that should fall to the divested operating companies. Yet AT&T is still pushing.

Finally comes AT&T's petition of Jan. 14 to more than double the charges to its long-distance competitors for interconnecting them with the local Bell System net. Set to expire on April 15, the existing tariff is already excessive, say the specialized carriers. Nevertheless, AT&T wants it raised to provide the company with a 12.75% rate of return.

Clearly, the Break-Up-Bell war is a long way from over, and a new series of battles in the Congress and before the FCC is only just beginning.

**-Ray Connolly**

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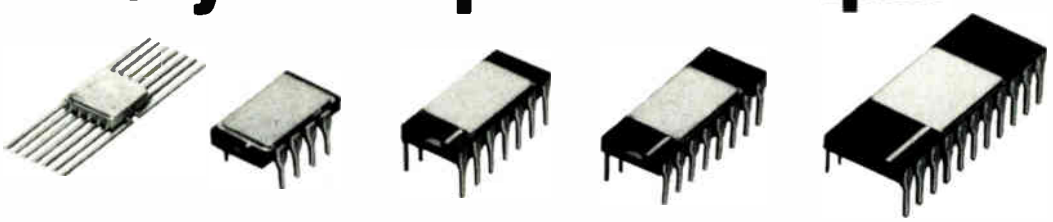

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| 7-Channel Darlington Arrays | ULS-2000H<br>ULS-2010H<br>ULS-2020H | 50V<br>50V<br>95V | 500mA<br>600mA<br>500mA | 29304.1 |
| Quad Darlington Switches | ULS-2064H to 77H | 50/80V | 1.5A | 29305.1 |
| 8-Channel Darlington Arrays | ULS-2800H<br>ULS-2810H<br>ULS-2820H | 50V<br>50V<br>95V | 500mA<br>600mA<br>500mA | 29304.4 |
| 8-Channel Source Drivers | UDS-2980H | 50/80V | −500mA | 29310.1 |
| Dual Power Drivers | UDS-3610H | 80V | 600mA | 29308.1 |
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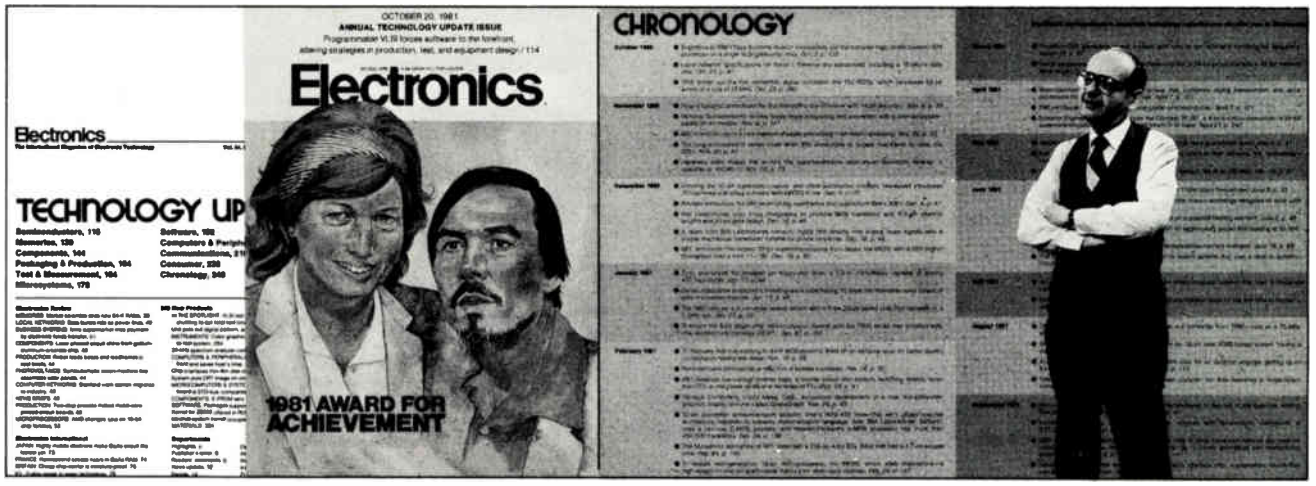


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Sam ought to know about Tech Update, because each year he marshals the expeditionary forces, deploying them into strategic areas around the world where they gather the intelligence necessary to create this important editorial. In fact, in pursuit of the worldwide data which appear in the 1981 Tech Update issue, our troops covered tens of thousands of miles, gulped 10,000 cups of office-machine coffee and devoured 246 buttered bagels!

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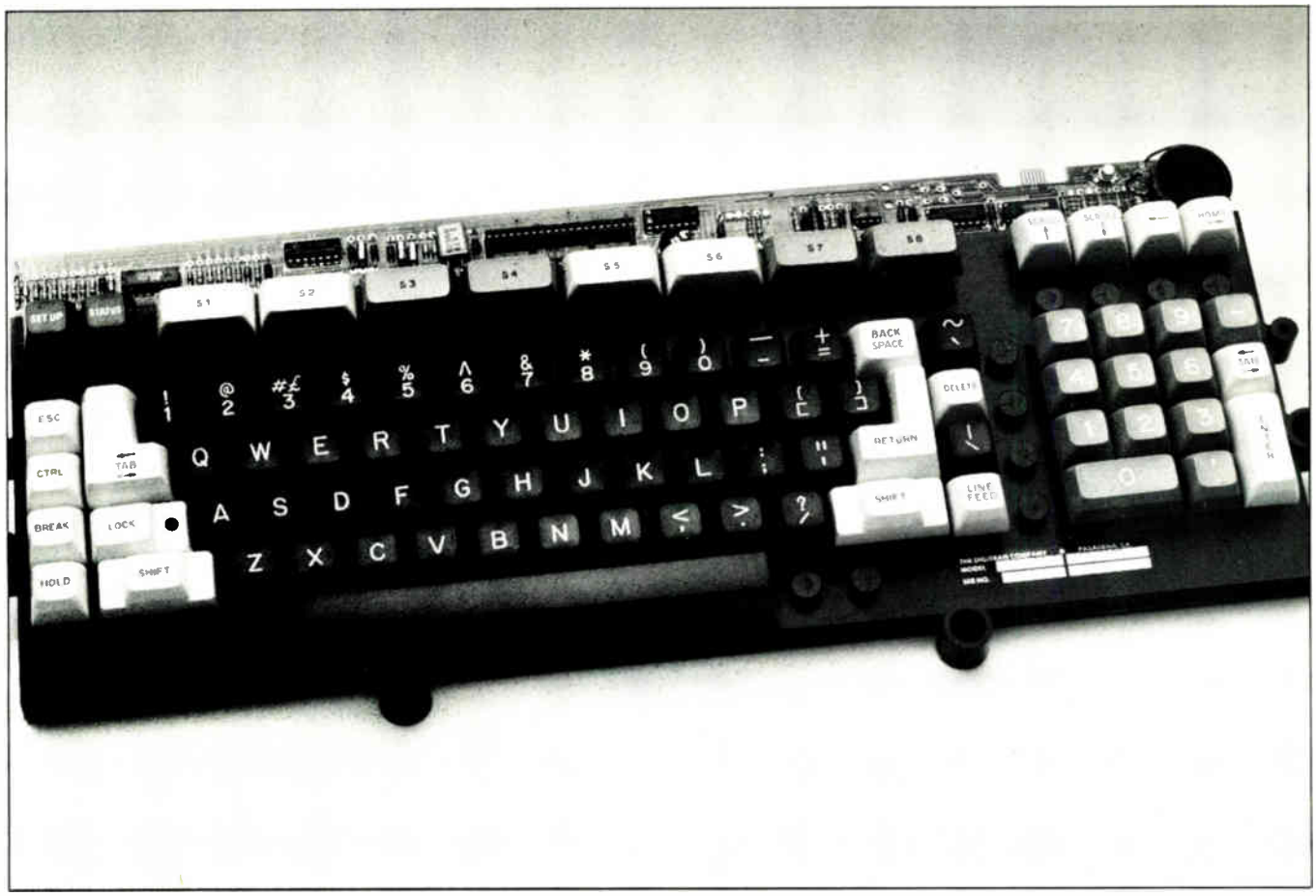


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# The case for CMOS crosspoints: Just these two RCA devices do the job of 48 relay switches.

If you're still using relays or high-current discrete switches in your telecommunications equipment, here are some good reasons to switch to RCA CMOS crosspoints.

With a single IC you can replace as many as 32 discrete switches, as well as the additional support circuitry normally needed for decoding and latching. This can improve reliability. Because the lower the parts count, the higher your reliability. And you can design much smaller products.

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For further information, contact your local RCA Solid State Distributor.

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Circle 54 on reader service card

# International newsletter

## NEC launches superfast mini

A superminicomputer with a throughput of 4 million instructions a second and a gate delay of only 0.5 ns has been put on the market by Nippon Electric Co. Although the company claims its new MS190 is the fastest minicomputer in the world, it appears nearly identical in power to Gould Inc.'s Concept 32/87 system [*Electronics*, Jan. 13, p. 155]. The MS190 has a main memory space of 16 megabytes, but virtual memory capability is not provided because the firm thinks such needs should be filled by its ACOS mainframe computers. **High speed is attained by using the large hybrid circuits the firm developed for its largest ACOS 1000 mainframe and a cache memory,** usually 32-K bytes in size. In a standard configuration with a scientific instruction processor, 4 megabytes of main memory, a complement of peripherals including eight work stations, and 32 communications lines, the computer sells in Japan for $530,000. Deliveries will start this autumn.

## High laser coupling efficiency achieved

By a simple modification of the end facets of glass fibers, researchers at ITT affiliate Standard Elektrik Lorenz AG in Stuttgart, West Germany, have raised laser-to-fiber light-coupling efficiency to as high as 80%. This, they say, compares to 20% to 30% for conventional coupling techniques. **The high efficiency is achieved by simply grinding the fiber end to the shape of a roof,** the angle being 65° with respect to the fiber axis. This adapts the graded-index fiber to the emission characteristics of the laser. For coupling, the fiber roof ridge is aligned parallel to the laser stripe at a distance of about 10 $\mu$m. In conventional coupling techniques, the fiber is cut perpendicularly to its axis and placed opposite the laser.

## Crosspoint array is extremely dense

To control switching in its Proteo UT 10/3 electronic digital exchange [*Electronics*, April 21, 1981, p. 86], Italtel Società Italiana Telecomunicazioni SpA of Milan has developed an integrated matrix **capable of handling connections for the 256 bidirectional time slots belonging to eight 2,048-Mb/s lines.** Driven by a Z80 microprocessor, the 40-pin MOS component can be used for time-slot switching and for byte insertion or extraction in any time slot. The matrix will be produced by SGS-ATES Componenti Elettronici SpA in Agrate, Italy.

## Satellite to test video conferencing

One of the first assignments for the European Communications Satellite, slated for a 1983 launch, will be to test the commercial waters for a European videoconferencing service. The aim of the European Visual Service Experiment is to cut costs by using compressed digital techniques of video transmission and to provide portable studio equipment on a customer's premises. As a first step, a CEPT (Council of European Post and Telecommunication authorities) standard is in preparation—at present, only every other line in a standard 625-line picture is transmitted. **The resulting 1-MHz 313-line video signal can run through a 2-Mb/s codec**—developed initially for British Telecom by McMichael Ltd., a GEC company—and at the far end, the missing lines are restored by interpolation. By comparison, the bandwidth required for a broadcast-quality transmission is 5 MHz analog and 140 Mb/s digital. Yet, in an alternative slow-scan mode, it can transmit documents at high definition.

# International newsletter

### Westinghouse to build Olivetti robots

Another major U. S. company has turned to Italian technology as a shortcut to the marketplace with proven robot systems. Westinghouse Electric Corp. has signed a five-year agreement with Olivetti Sistemi per l'Automazione Industriale, a company in the Turin-based Olivetti group, **to purchase 40 Sigma robots and secure the exclusive license** for their manufacture, sale, and service in North America. Sigma is a high-performance assembly robot for precision mechanical, electromechanical, and electronic applications.

### 16-bit personal computer arriving from Mitsubishi

Mitsubishi Electric Corp. has started selling a 16-bit personal computer built around Intel's 8088 processor. It appears very similar to IBM's Personal Computer (although it was designed earlier and is arriving later), even having a socket for an optional 8087 mathematics coprocessor. **The product is called Multi-16 because of its ability to use a multiplicity of languages,** including Basic, Cobol, Fortran, and Pascal in professional applications. It is available in three configurations: the lowest-price model has 128-K bytes of random-access memory and includes a built-in black and white display and single floppy disk for $3,235. The highest-price configuration has 256-K bytes of RAM and includes a color display and a dual floppy disk for $5,450. Add-on RAM permits expansion to a total of 384 kilobytes. Mitsubishi will start making deliveries April 1.

### Racal readies local network

Watch for data-communications specialists Racal-Milgo Ltd. to enter the local network market in the second quarter of 1982 with its Planet net, billed as a second-generation Cambridge Ring system. In Racal's approach, **the network controller takes on the majority of administrative tasks, thereby reducing the cost per port—which uses Racal custom logic arrays—well below that of the hardware in other local nets,** says the company. Planet can also detect component failures—in the controller, cable or access ports—and immediately reconfigure itself, isolating the faulty component. There will also be a fiber-optic version and gateways to trunk networks and other local nets.

### Addenda

Using a new but still secret manufacturing technology, Norway's Norsk LCD A/S, a small company in Drammen, near Oslo, is producing what it claims are **the largest liquid-crystal displays on the market.** Measuring up to 30 by 30 cm, it has individual LCD cells said to be several times larger than those currently available. . . . From the research laboratories of Siemens AG comes a ceramic material that **suppresses spurious modes in delay lines of traveling-wave tubes,** greatly increasing the TWT's output. Space-saving ceramic resonators the size of collar buttons are installed in the inner side walls alternately to the left and right of the delay line axis. . . . Rudolf Hell GmbH, West Germany's leading producer of cathode-ray-tube–based photo typesetting and picture reproduction systems, has **licensed the Soviet Union to produce its electronic color picture scanner,** the Chromograph DC 350. . . . Isotronix Inc. of San Antonio, Texas, and China Trade Corp. of New York have signed an agreement with the China Corp. for the Shipbuilding Industry, Peking, **to build two plants in China**—one to manufacture printed-circuit boards and another to produce computer components and subassemblies for the Anchorn MT-1 truck computer system, both using Isotronix designs and technology.

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The command set is in "standard engineering English" matching the abbreviations on instrument front panels. As is shown above, readable mnemonics in the command string set up the PS 5010 Programmable Power Supply. For example, in line 4190, VNEG 10.0; INEG 0.1 set the negative supply for −10 volts with a 0.1 amp current limit.

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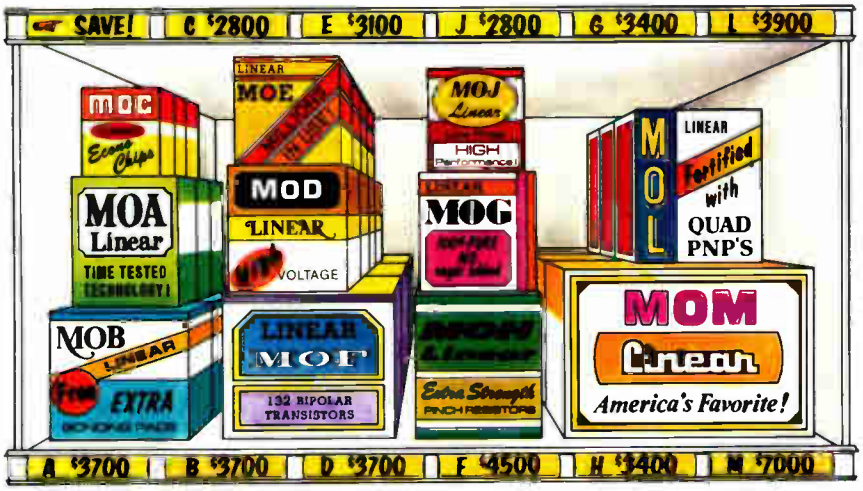


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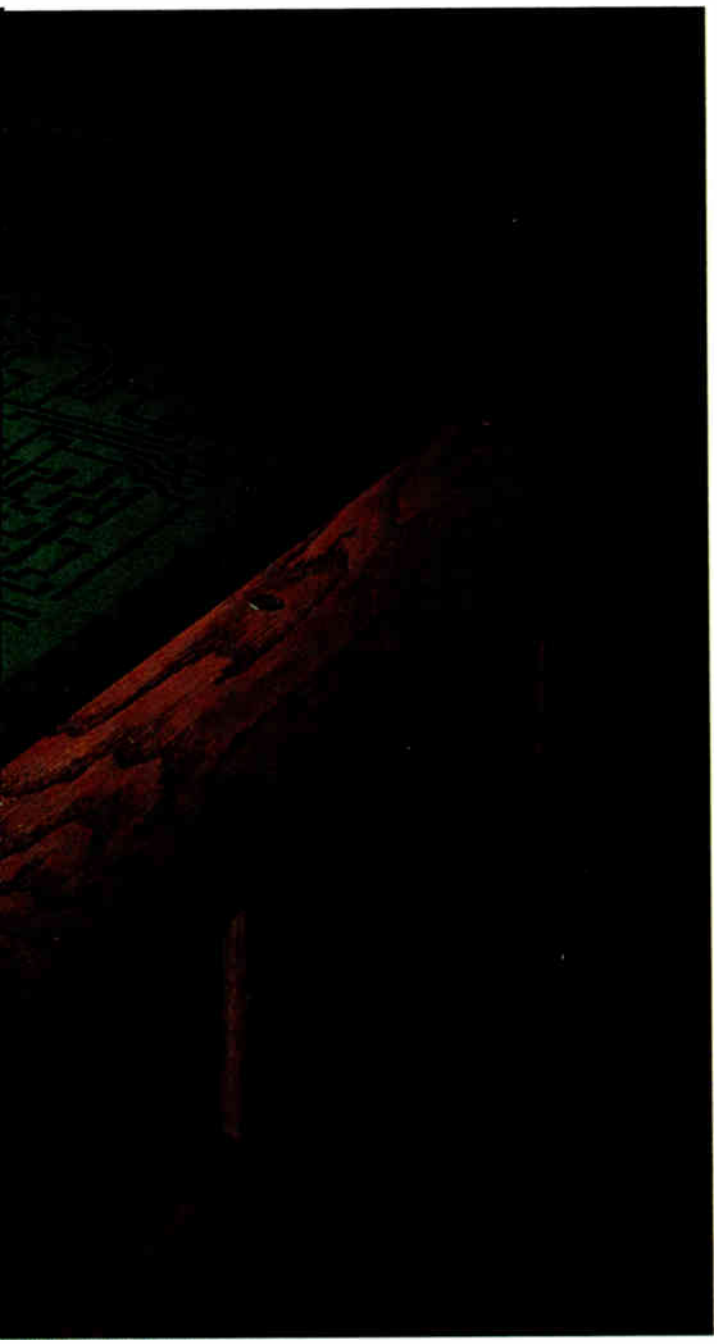

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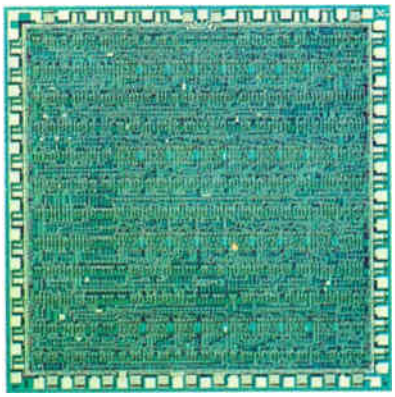

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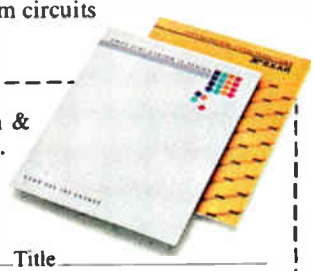

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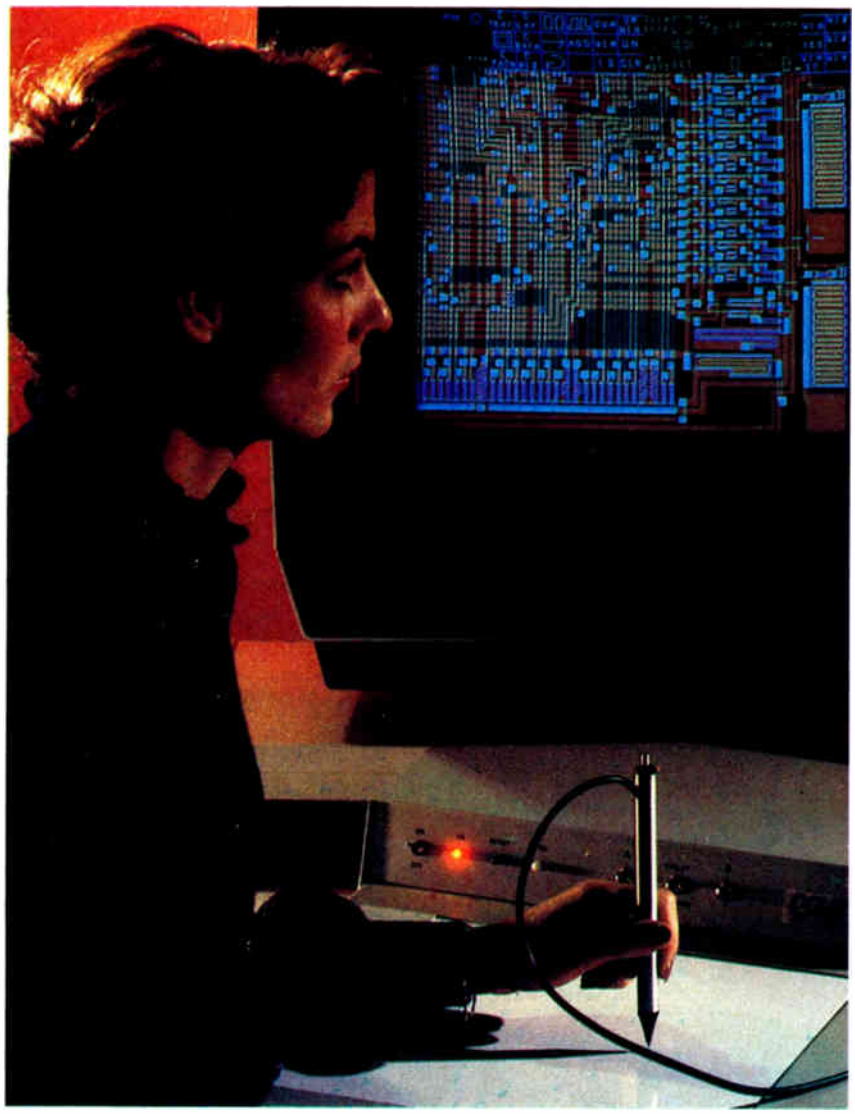

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# Versatile system determines profiles of optical fibers

*by Robert T. Gallagher, Paris bureau manager*

Multimode fibers' dispersion can be characterized by selective excitation done with laser diodes

**Signal dispersion** is a problem in multimode optical fibers because the propagation times of the different modes vary significantly. To find the wavelength at which the propagation times for all the modes for a given fiber are instead more or less the same, engineers at Thomson-CSF's central research laboratory in the Paris suburb of Corbeville have built a system that characterizes multimode fibers by the selective excitation of their modes.

Put another way, the problem that the Thomson designers faced was to determine how the refractive-index profile affected the dispersion at different light wavelengths.

"We became interested in this problem because we noticed that the stated bandwidth of fibers depended enormously on how they were rated," explains Bernard Muller, one of the engineers working on the development of the system. "When we began selective excitation of the modes, we found that the propagation time for a mode in the center of a fiber could vary as much as 250 picoseconds compared with a mode on the periphery."

**System.** To characterize fibers, Thomson uses a four-part system. It consists of a light source, an interface between the source and the fiber to be characterized, a television-like monitor to display the fiber face where the light is injected, and a data-processing oscilloscope to analyze the signals (see figure).

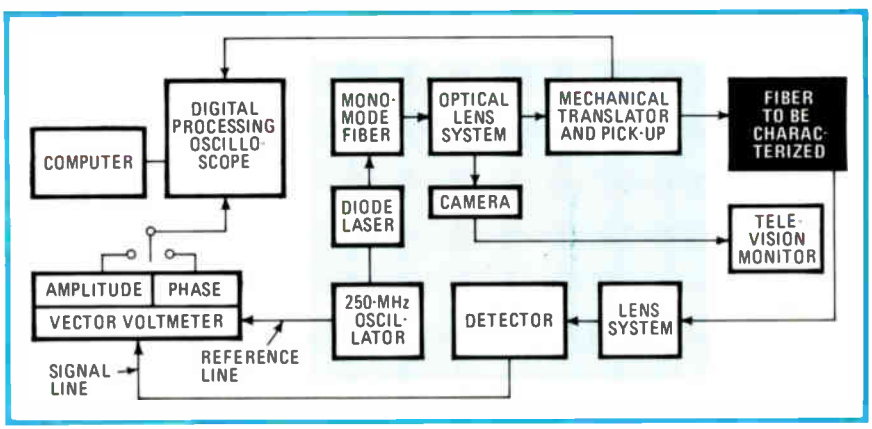
The laser-diode light source is either gallium aluminum arsenide with a 0.84-micrometer wavelength or gallium indium arsenic phosphorus at 1.27 $\mu$m. To maintain precise control of the test system's operating frequency, the source has a narrow spectral width, is temperature-stabilized, and is modulated at 250 megahertz so its phase may be measured by a vector voltmeter after it passes through the fiber under test.

Interfacing with the fiber to be characterized is achieved by a secondary source—a monomode fiber 20 meters long that carries out the selective mode excitation. To optimize the injection of the light signal, two microscope objectives connect the secondary source and the multimode fiber to be characterized.

When the light spot from the monomode fiber excites the face of the multimode fiber, the conditions of excitation can be seen on the TV monitor. A computer-driven mechanical device shifts the cross-sectional surface of the multimode fiber by 1-$\mu$m increments relative to the monomode secondary source to facilitate selection of the mode to be excited.

All of this care is quite necessary. "The optimum index profile of a fiber is so critical that measuring the amplitude of dispersion is insufficient as a means of attaining it," explains Jean-Paul Pochole, who is coordinating the development of the system. "Using selective excitation of the modes, we are able not only to judge the amplitude of the dispersion, but also in which direction we must go to correct it."

The light signal is received as it leaves the multimode fiber by a photodetector, either silicon for the 0.84-$\mu$m wavelength or germanium for 1.27 $\mu$m. The photodetector converts the light into current and passes it on to the vector voltmeter where variations in the phase and amplitude of the sinusoidal component of the signal are detected by comparison with the original signal. The parameters thus measured are pres-




**Less dispersion.** With the test setup shown, engineers can analyze the refractive-index profile of fiber-optic cable to see what wavelengths propagate with minimum dispersion.

ent in visual form on the screen of the digital processing scope.

**Defined.** Analysis of the variations in propagation time of the different modes leads to a definition of the kind and the order of modal dispersion according to the conditions of excitation, as well as a measure of the modal attenuation. A minicomputer integrated into the system then calculates the optimum index profile and displays the curve on its screen. It also helps calculate what changes in the doping of the fiber are necessary to correct the index profile.

Potential users of the system will be manufacturers of optical fibers who can use it to control fabrication processes and designers of optical communications systems who will be able to optimize modal-dispersion compensation operations, as well as determine the wavelength for which a given fiber shows low modal dispersion. With some modification, Thomson says, the system can also be adapted to the characterization of certain parameters of monomode fibers, like dispersion due to elliptic polarization.

## Great Britain

# Design-automation work station enables systems houses to lay out VLSI gate arrays

Systems companies have watched with increasing concern as control of the design process has slipped from them into the hands of the custom chip suppliers. Now they can breathe more easily because gate-array pioneer Ferranti Semiconductor Ltd. is offering a $70,000 computer-aided design station for very large-scale integrated gate arrays that puts the design task back in house.

The low-cost CAD work station provides the software tools needed to customize uncommitted logic arrays of up to 10,000-gate complexity with speed-power products that permit subnanosecond speeds or, alternatively, near–complementary-MOS levels of power dissipation at TTL speeds.

The ULA Designer, as it is called, turns out a pattern-generating tape for the final-layer metalization that customizes Ferranti's line of gate arrays. Such work stations are beginning to pop up in the design-automation world (see p. 108), and some even include automatic array routing, a feature that Ferranti does not yet provide on its offering.

Two elements make up the ULA Designer. First is a Digital Equipment Corp. PDP 11/23–based work station with an Applicor VLSI 860/870 graphics terminal on which interactive work such as data input, editing, and so on is performed.

Then, for the more arduous number-crunching tasks such as design-rule checking, test-pattern generation, and so on, the user can access a remote host computer. Ferranti has already in place VAX 11/780s at Scotts Valley, Calif., and Manchester, England, which can be dialed up over 2.4-kilobit-per-second links.

**Centers established.** For the small user who cannot afford the $70,000 outlay, Ferranti, like its competitors, will be setting up additional regional design centers, such as the long-established Munich operation, that will be staffed by ULA designers and equipped with its new work station. One is scheduled to start operation shortly in New York. The system can also be leased.

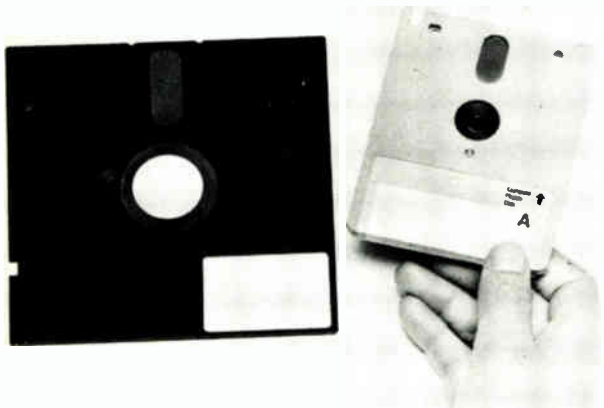
For the big systems houses, though, the ULA Designer provides a ready means of retaining control of the total design process. "We expect to sell 15 systems in Europe alone in the first 12 months," says Bryan Down, Ferranti Semiconductor's managing director.

Down says that CAD techniques of this sort will be needed to avoid a design crisis. Ferranti, for example, processes six different ULA designs

## Firms cooperate on compact floppy disk

Disk-drive-makers Matsushita Electric Industrial Co. and Hitachi Ltd. have teamed with media maker Hitachi Maxell Ltd. to cooperatively develop a compact 3-inch double-sided floppy disk. To facilitate acceptance, the data rate and capacity are identical with those of 5-in. disks despite the smaller size [*Electronics*, Dec. 29, p. 49]: drives can be plug-compatible; the same controllers can be used; and libraries can be copied on a one-for-one basis.

The media will be much more compact, however, and more resistant to damage from handling or use. Metal shutters protect the media from fingerprints, and a hard plastic hub prevents damage from repeated use. The companies will propose their format to disk and hardware manufacturers as a new standard for the industry, which may put them in conflict with Sony and its 3¼-in. single-sided floppy.



Although they cooperated in development, the two firms will compete in the sale of small drives. Initially, the price of disks will be similar to that of high-quality audio cassettes, but the price should fall as production increases. Disk samples will be available in April or May.

**-Charles Cohen**

per week and is limited in the number of new jobs that it can handle.

Other companies have reached the same conclusion. CAD manufacturer Racal-Redac, for example, will launch its gate-array design work station in the next few weeks. CAD software company Compeda also plans to add a ULA package to its Gaelic CAD system [*Electronics*, Dec. 15, p. 82].

**Trio.** Complementing its software design aids, Ferranti now offers three different performance families of gate arrays, amounting to some 20 different versions. The technology is the firm's stretched collector-diffusion isolation process [*Electronics*, June 16, 1981, p. 74]. The line includes at the high speed end a 1,000-gate array with a 0.5-nanosecond gate delay and a general-purpose 2,000-gate array family with a 2.5-ns gate delay. At the VLSI end, it offers a 4,000-gate array device, with a 10,000-gate array scheduled to be out in 1983.

Ferranti's software is specific to its process and gate-array family, though Down concedes that may change if the market so demands. It comprises a full complement of facilities, layout, design-rule checking, logic checking and simulation, a high-level test language and test program, as well as providing test-schedule verification.

Though it asserts that manually laid-out arrays achieve a far higher packing density, the Manchester firm realizes that it must offer companies the option of automatic routing, so later this year it is launching a new ULA range, optimized to permit auto-routing. According to David Grundy, who oversees the ULA Designer project, the additional underpasses provided add 25% to the chip area but retain the yield-giving advantages of auto-routing with single-layer metallization.

"We want to hold off from double-layer metallization for as long as possible," he says. Ferranti will be delivering 10,000-gate array chips, 0.4 inch on a side, by 1983 because of the high yields achievable with its present six-mask process, says Grundy. **-Kevin Smith**

**West Germany**

## Ultrasonic test uses laser, not transducer

A 10-year research and development effort at West Germany's Krautkrämer GmbH has resulted in a nondestructive ultrasonic test method that works without a transducer to contact the object under test. The absence of contact means that even red-hot materials can be tested, an advantage that comes in handy in many fields of metal processing.

In the new Krautkrämer technique, laser beams replace the piezoelectric transducers—devices that, in ordinary nondestructive methods, contact the material to set up the ultrasonic waves. The distance between the laser system and the object under test can be up to 10 meters, with the material under test at temperatures near the melting point.

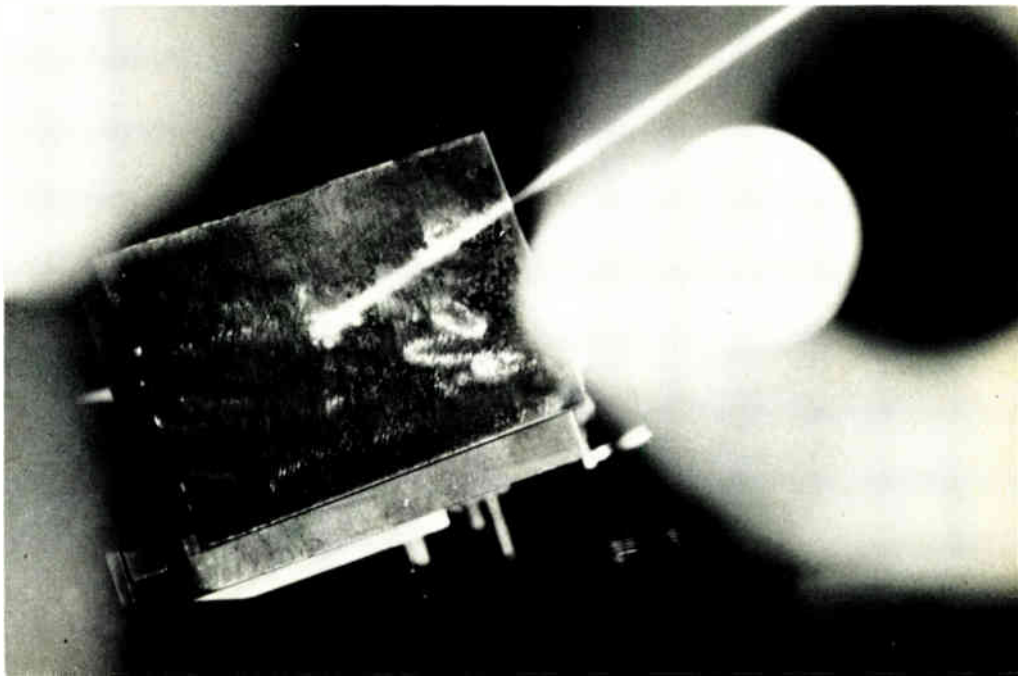
What's more, the surface characteristics of the material, such as roughness and curvature, do not influence the test accuracy. Therefore the technique lends itself well to performing checks on hot continuously cast sheet metal, forgings, billets, and the like, during deforming or metal-shaping processes. In short, the technique can be applied wherever conventional ultrasonic methods fail because of problems encountered with coupling a transducer to the material under test.

**Transmitting laser.** Cologne-based Krautkrämer, a heavyweight in nondestructive test equipment and a subsidiary of the Philadelphia-based pharmaceuticals firm SmithKline Corp., has implemented its method with a laboratory model consisting essentially of a gas laser as the light-transmitting device and a laser-interferometer combination functioning as a receiving system.

Through a lens, the transmitting laser focuses 20-nanosecond high-intensity light pulses onto the surface of the object under test. Due to thermomechanical effects, these pulses convert at the surface into ultrasonic pulses of about the same 20-ns width, producing ultrasound frequencies from 1 to 30 megahertz. At 1 joule, the intensity of the light pulses is such that the material's surface is not appreciably damaged.

The laser at the receiving system, an yttrium aluminum garnet laser, illuminates the surface during the test process. The ultrasound waves returning from the interior of the test object cause tiny deflections of the surface that, in turn, modulate the YAG laser's reflected light at a

**Red hot.** With Krautkrämer's nondestructive test method, laser beam hits the surface of a hot object to produce sound waves. These give clues as to the object's interior structure.



rate corresponding to that of the ultrasonic waves.

The interferometer demodulates the reflected light and produces signals that can be represented on the screen of a cathode-ray tube. Their delay and amplitude are a measure of the material's characteristics and give clues on faults within it.

In testing an object, its position relative to the lasers is not critical, Krautkrämer says. Regardless of the laser beam's angle of incidence, the ultrasonic waves always traverse the material in a direction perpendicular to its surface. **-John Gosch**

**Baby.** Table-top robot stands only 10 inches high, but can emulate the movements of the large industrial models. Computer-controller on the right programs the arm.

## Japan

# Low-cost baby robot teaches automation

A miniature robot standing less than 10 inches tall that can move as well as the big boys may seem like a toy, but Mitsubishi Electric Corp. sees it as an educational tool. Users can learn about robots' functions and how to program them—and there could be a host of potential practical and hobby uses as well.

Scheduled for April sale in Japan at less than $1,600, the Move Master robot can be guided by an Apple or similar personal computer. Alternatively, Mitsubishi will provide a $3,500 controller that also facilitates program development.

Although it stands only 245 millimeters tall and weighs but 8 kilograms, the Move Master features the same five axes of movement as many large general-purpose industrial robots used on production lines. Its built-in intelligence probably beats that of most of the full-size robots in use.

The design tradeoff in which the new robot takes a back seat to industrial models is its use of pulse motors with open-loop motion control, rather than more precise servo motors with feedback control. But the compromise on motors makes for greatly reduced costs.

Good accuracy at the 500-gram maximum load handled by this system is obtained, though, by gearing down the pulse motors for an output angle of 0.2° per pulse. Repeatability of positioning is said to be to within 1 mm, and Mitsubishi is aiming for as little as 0.3 mm.

**Flexible.** The Move Master consists of a swiveling body and articulated arm, jointed at shoulder, elbow, and wrist and ending in a gripper (see photo). Overall length from the tip of the gripper to the far end of the base is 645 mm. Suggested uses are applications where neither great precision nor strength is needed, such as moving test tubes to and from a source of heat.

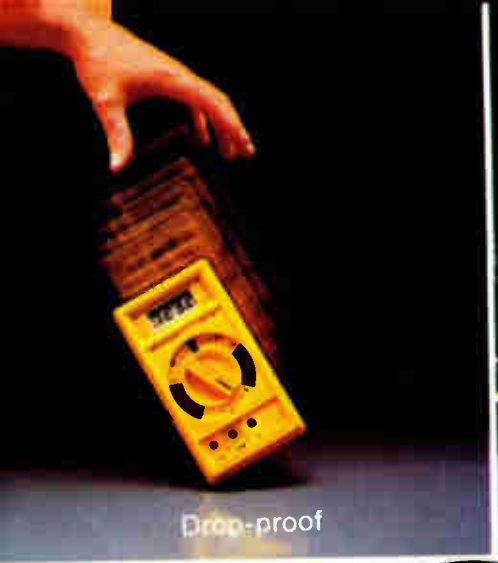
Intelligence in the robot includes a Z80 microprocessor with 16-K bytes of read-only memory and 8-K bytes of static random-access memory. Included in the ROM is a self-diagnosis program that puts the unit through its paces so that users can visually check it out.

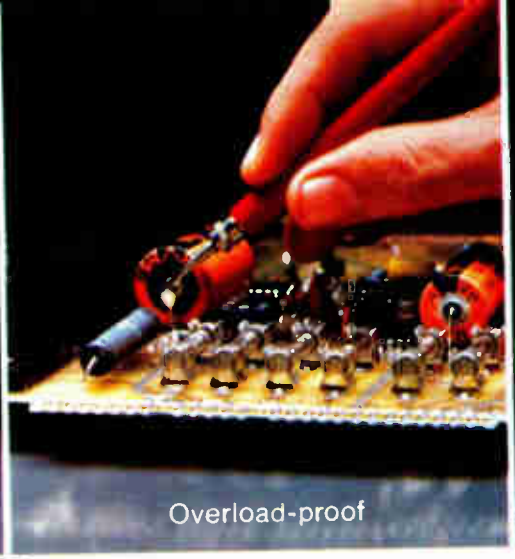
The educational and research uses of the robot favor a wide variety of software. There is a collection of controlling subroutines currently available that read and execute instructions written in robot Roly, Basic, or assembly languages.

Roly, which is an acronym for Robot Language by Yahagi, was written by Yahagi Consultants Co. It is a symbolic language for robots that is said to be similar to the VAL language used by Puma robots produced by Unimation. The language will be available in versions for five different computers—Mitsubishi's special-purpose controller, the Apple II, the Sharp MZ-80B, Nippon Electric Co.'s PC-8001, and Mitsubishi's Multi-16 personal computer, similar to IBM's (see p. 55).

For the many microprocessor users who prefer Basic, this language will call the subroutines in the robot, but it is slower and less convenient than Roly. Basic can also be used to drive the robot motors directly, a useful attribute in teaching applications. Users who want to exercise their ingenuity to the utmost can write their controller programs in assembly code.

The special-purpose controller, offered for program development and robot guidance to those who do not have a suitable microcomputer, is a complete Z80A computer operating at a 4-megahertz clock rate. It includes 64-K bytes of RAM and 4-K bytes of ROM (for the monitor) together with a 5-inch cathode-ray tube; built-in printer; and a double-sided, double-density 5-in. floppy disk, plus space for a second floppy. The operating system, assembler, and Basic interpreter, which total about 27-K bytes of memory space, and the Roly language, requiring another 32-K bytes, are loaded from the floppy. The computer has two Centronics printer interfaces, one for its printer and one for the robot. It also has an RS-232-C serial communications interface for supervisory control. **-Charles Cohen**





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# What next for AT&T and IBM?

Technology could receive big push as five prime areas are likely to see head-on clash now that antitrust fetters are broken

*by the staff of* Electronics

**The landmark antitrust** settlements involving American Telephone & Telegraph Co. and International Business Machines Corp. could mean a new world of markets, services, and technology for them. The two giants likely will find themselves for the first time competing for the same turf. Now, even as they wait for the Federal judiciary, the Congress, and state public utilities commissions to have their say, a small army of intensely interested observers—including competitors, suppliers, customers, and other interested parties—is busy focusing its brightest speculative spotlights on what is likely to happen.

At this early date the easiest answer is to say that AT&T will push ahead into computers while IBM moves into communications, but already there are several clear areas of overlap. With both companies free of antitrust worries—AT&T by giving up its 22 operating companies and IBM simply because the Justice Department decided its own case was too weak—technology should be the big gainer.

There are at least five areas of technology, all of which depend on computer and software technology, where the two companies can meet head-on. Three of these will probably actually see competition by the mid-1980s. They are:

- Voice- and data-handling private branch exchanges.
- Voice store-and-forward software and equipment.
- Information services and related equipment.

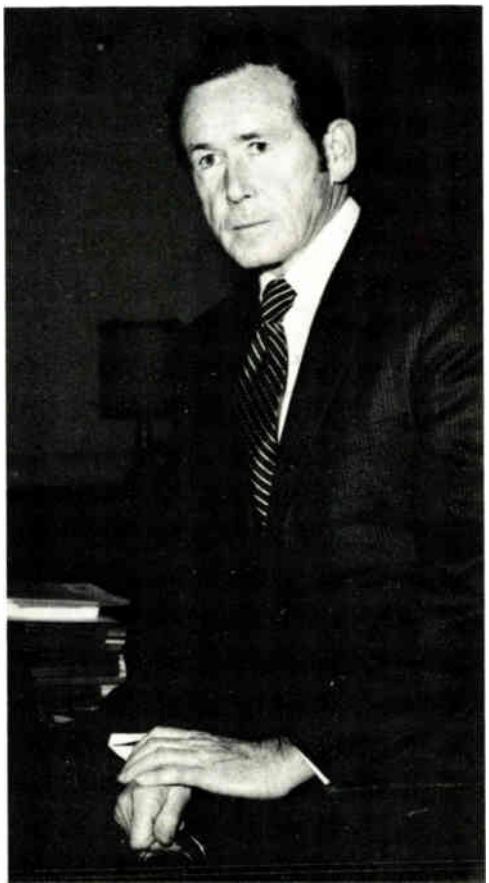
The two other areas will develop more slowly. They are:

- Data-communications facilities, as represented by AT&T's Advanced Communications Service and by Satellite Business Systems Inc., partly owned by IBM.
- On-line computation capability, as furnished, for example, by AT&T as its fully separated subsidiary gets rolling and provides end-user services. Operated at arm's length, such a subsidiary would give Bell entree into the unregulated data-processing and commuications business.

Of course, AT&T and IBM are economically strong, own two of the largest and best electronics research organizations in the world, and cover markets that are booming. Thus, it is quite likely that IBM will sell in the U. S. any line of PBXs it introduces and that AT&T will become a multinational company—it has applied for listing on the London stock exchange—and will aggressively sell its offerings overseas, just as IBM already does.

Similarly, there is nothing to stop AT&T from introducing a personal computer—Bell Laboratories is easily capable of that—and both will be selling intelligent and other kinds of terminals. It is also possible to envision desk phones with expanded keyboards and small displays for electronic mail and information services. Both could also sell home phones with built-in integrated-circuit facilities for at-home information, shopping, banking, and reservation services, and even electronic mail.

The PBX business is likely to be the first to show the effects as IBM will probably feel the need to get its



**Jurist.** U. S. District Court Judge Harold Greene must approve the settlement. He had been hearing the antitrust case brought against AT&T by the U. S.

**Deal is made.** William Baxter, assistant attorney general for antitrust, announced that the U. S. had settled its case when AT&T agreed to divest 22 operating companies.

units on the domestic market before AT&T's fully separated subsidiary—Baby Bell, as it has become known—moves in. Related to this area is voice messaging, where both companies have tested systems that store a message and use a computer to send it to a multitude of users at different times and in different places.

From the point of view of IBM's competitors, the picture is Janus-faced—there is good news and bad news. The way Michael Killen sees it from his seat as president of Strategic Inc., the San Jose, Calif., market-research outfit, the good news is that "this decision will enable IBM to keep the Japanese with their fifth-generation computer program from doing to the computer and communications industry what they have done to the automobile industry." While small companies will be unaffected by IBM's new freedom, Killen says, "it will make it tougher on the bigger ones like Digital Equipment, Hewlett-Packard, Honeywell, and so on. The net result is that everyone will become more competitive."

**New directions.** John R. Opel, president, will lead IBM into new marketing areas that will pit it against AT&T.

Another industry watcher, Victor Krueger, vice president at Dataquest Inc. in Cupertino, Calif., says, "I expect that the domestic microwave carriers such as MCI and Southern Pacific Communications will find stronger competition from AT&T Long Lines." He also sees the operating companies becoming more cost-conscious in their equipment purchases because outside vendors will compete with Western Electric. "Companies like Northern Telecom should gain market share," he says, adding that "Western Electric is not yet organized for aggressive marketing. They are still basically order takers."

Whatever they sell, there will be many David-like companies out there with them, seeking to supply as well as battle the two Goliaths. Among them, the prevailing mood soon after the settlements were announced was hopefulness. There is also the feeling in the computer industry that the impetus for growth will increase simply by virtue of AT&T's and IBM's presence.

**Opportunities.** David Methvin, president of Computer Automation Inc. in Irvine, Calif., points out that "Small companies have plenty of avenues for competition. There's always room around large companies, which must shoot for 60% to 80% of the market."

Overseas, suppliers of telecommunications equipment see a new market opening for them. While Japanese companies are generally unwilling to speculate, West Germany's Siemens AG says that the operating companies' independence will give it an opportunity in all product areas from cables to exchange systems, an opportunity it intends to pursue aggressively. The ITT subsidiary, Standard Electrik Lorenz AG, is a bit more cautious, pointing out that system specifications in the U. S. are different from West Germany's. And from the giant Philips Gloeilampenfabrieken comes a terse statement agreeing that the U. S. market is indeed important.

**Congress' mood.** But any estimates about the course of IBM and AT&T must take into account the mood of possibly the biggest player in the game, the one that has thus far been silent: the U. S. Congress. While IBM should have no trouble with the legislative branch, AT&T, as a Government-regulated monopoly, must be anxious about what could emerge from Capitol Hill.

Members of the House and Senate telecommunications subcommittees, their staffs, and telecommunications industry competitors of AT&T are all determined to avoid what a number of them see as a "worst case" scenario for the U. S. telecommunications market after AT&T has spun off its operating companies.

That scenario, set around 1986, envisions AT&T's chairman testifying before a joint hearing of the House and Senate subcommittees comprised of many angry and embarrassed members. "AT&T regrets," its chairman might say, "that the quality of America's service has declined while local telephone and terminal rates have tripled in the past four years. But let us remind you that the decision to force the breakup of the Bell System and its national network was not our idea. That decision, supported by many distinguished members of Congress, originated in the U. S. Department of Justice."

The chairman might continue: "We also regret that such a significant share of the American market for terminals and services is being lost to foreign competition, but competition is what the Federal government mandated in 1982."

**Rejected.** All interested parties agree they never want that scenario to materialize. They also agree that much remains to be done if it is to be avoided. "Much of it is detail," says one House subcommittee staff member, "and there is not yet much agreement on their precise structure. We have a lot of work ahead."

Chairman Timothy D. Wirth (D., Colo.) of the House Commerce telecommunications subcommittee agrees that "the need for legislation is urgent" in light of the AT&T settlement. Concurring in that view are House Judiciary Committee chairman Peter W. Rodino Jr. (D., N. J.) and Senate Commerce Committee chairman Robert Packwood (R., Ore.), whose group will take another look at the end of the month at the Senate-passed S. 898 [*Electronics*, Oct. 20, 1981, p. 59].

There are some 20 issues that Wirth's subcommittee believes legislation must now treat. In sum, they include: quality of service, local user charges, full and fair competition, national security, international trade, procedural reforms at the FCC, and prohibition of data processing from regulation.

## Behind AT&T's closed doors

American Telephone & Telegraph Co. chairman Charles L. Brown (pictured below), vice president and general counsel Howard J. Trienens, and executive vice president Morris Tannenbaum held a nationwide closed-circuit color-TV conference on Jan. 12 with top-level managers of the 22 Bell operating companies. The purpose: to explain and discuss the impact of the divestiture and AT&T's strategy. Although the conference with managers earning $20,000 to $110,000 lasted for about 1½ hours, "We didn't know any more about what's going on when we came out than we knew when we went in," says one. "It was very confusing, not to say depressing."

AT&T did disclose during the closed session that it does plan to continue establishing its fully separated subsidiary to handle new unregulated telecommunications and information industry ventures, according to another AT&T participant. That subsidiary, for which planning began with the Federal Communications Commission ruling in the Computer II inquiry, still proposes to take a number of employees from each of the 22 BOCs (Bell operating companies) to be divested and use them in the fully separated subsidiary to market, install, and service new products and services within the company areas that they now reach.

Athough the new "Baby Bell" organization would presumably leave the remaining BOC organization with sufficient numbers of persons with expertise to provide local telecommunications services, as required by the AT&T settlement with the Department of Justice, some participants in the meeting say "that's a matter for conjecture."

Another key concern of AT&T sources who participated in the session is the limited success of the company in establishing the new and aggressive marketing organization needed to compete in the unregulated marketplace with the likes of International Business Machines Corp. and a host of other companies entering the telecommunications field. Not least of these are Japanese exporters, who were described as "waiting offshore like a horde of locusts" to descend on the U. S. domestic market, as their counterparts in the consumer electronics industry did more than a decade ago.

Despite AT&T's recruitment of Archie J. McGill some five years ago from the corporate ranks of IBM to assume the new post of AT&T vice president of business marketing, "McGill's plan is not working," says another company executive. "He promised to get rid of the inbred Bell System people, and he did bring in a lot of new bright people from companies like Burroughs and Honeywell. But they have all come and gone. Many of them quit in disgust when they couldn't change the system. Some progress has been made, but Archie's plan is light years beyond the perception of Bell's senior management." AT&T is expected to get rid of the Bell System Purchased Products division, created with some fanfare about seven years ago to issue type approvals to equipment of non-Bell manufacturers, so that it could be linked to the company's network. The division has several hundred staff members. It was designed to increase the use of non-Bell equipment by the operating companies by means of Bell Laboratories' technical evaluation techniques. "Instead, all the division did was aggravate, annoy, and disturb" equipment makers that sought to get AT&T type acceptance, says one executive close to the operation. "Most companies just gave up trying" to crack the system. **-Ray Connolly**

Whereas Sen. Packwood's principal concern seems centered around the need for a new mechanism to substitute for AT&T's subsidy of local charges in sparsely populated areas, Rep. Wirth sees that as but one of many issues. By Wirth's staff estimate, based on 1980 data, local carriers would need a 46% rate increase to offset existing subsidies.

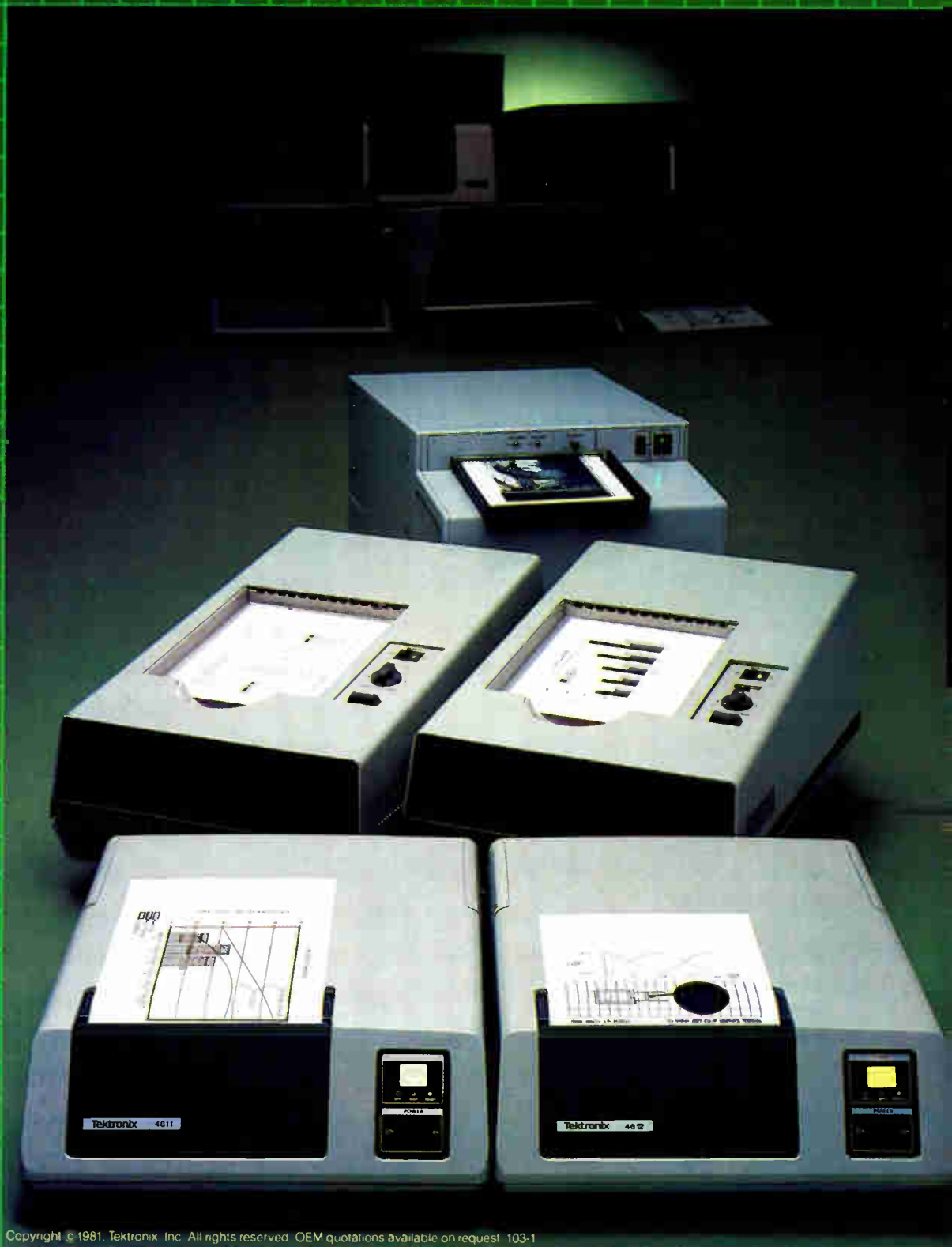
Local service revenues to all carriers totaled $27.18 billion, the subcommittee reports. A projected loss of $12.6 billion as a result of the settlement includes an estimated $880 million from Yellow Pages advertising, which AT&T would keep, plus $3.15 billion lost from terminal equipment transferred out of local rate bases; $1.3 billion from the transfer of inside wiring and another $7.54 billion lost from subsidies of local service by long distance.

Although AT&T antitrust counsel George Saunders insists the company is determined to protect the quality of the Bell System network despite the divestiture of the 22 operating companies, some competitors are not so sure. The settlement, says one, "is the best thing that could have happened to AT&T. They get rid of the BOCs [Bell operating companies], their least profitable business, and keep the rest. It looks like they may be out to gut the BOCs in the process."

**Flexibility.** AT&T rejects this, of course, but officials acknowledge the company is being given complete flexibility in its own restructuring, which must be submitted in six months for Justice Department approval. The divestitures must be completed a year after approval.

The prospect that AT&T may spin off a separate corporation of its 22 operating companies with an estimated $80 billion in assets is a likely possibility. In one little-noticed segment of the proposed settlement is the note that "notwithstanding separation of ownership, the BOCs may support and share the costs of a centralized organization for the provision of engineering, administrative, and other services which can most efficiently be provided on a centralized basis."

Another point is that AT&T, which retains Bell Laboratories and Western Electric Co., is ordered to provide "until Sept. 1, 1987 . . . on a priority basis all research, development, manufacturing, and other support services to enable the BOCs" to successfully function independently. The companies themselves would provide only local telecommunications and exchange access services—no hardware or customer-premises equipment. □



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Consumer electronics

# Home video-game sales are dazzling

Billion-dollar business, led by Atari, is expected to double this year as consumers seek entertainment at home

*by Larry Waller, Los Angeles bureau*

**That home video** games have scored heavily with consumers comes as no surprise, as their track record since a 1980 start has been closely monitored. But even savvy observers admit the games are a runaway success that is virtually unprecedented in an industry where quick stardom—and sometimes just as sudden oblivion—is commonplace.

"Overnight, it's a billion-dollar business," says Charles Daigneault, vice president of Sharp Electronics Corp., who presented the outlook for the games segment at the Winter Consumer Electronics Show early this month in Las Vegas. Moreover, the consensus estimates that sales to retailers will more than double this year, with market saturation still far in the distance.

Although suppliers of game-system hardware and individual game video-cassette cartridges cannot adequately articulate the phenomenon, they agree it is a happy circumstance of the right product hitting at the right time. With entertainment tastes evidently shifting from movie-going and record buying to home electronics, video games provide "the maximum pleasure at a reasonable price," as one games company executive says.

But the onslaught of heavy promotion, appealing games, and keen competition has whipped the consumer into a "feeding frenzy" for video-game products, according to financial analyst Ted James of San Francisco's Montgomery Securities Inc. He follows electronic entertainment and predicts that games, along with video recorders, cable television, and personal computers, will redirect consumer tastes irrevocably from the public accommodation to the privacy of the home.

Although a booming field can be counted on to create new business opportunities for years, the major contestants already have staked out their turf. In a dominating stance is Atari Inc. of Sunnyvale, Calif., subsidiary of Warner Communications Inc., whose estimated $650-million-plus sales in 1981 make it almost three times bigger than Mattel Inc.'s Electronics division, based in Hawthorne, Calif. Both firms make the game-playing hardware systems, Atari turning out some 3 million video computer systems to Mattel's 750,000 in 1981, along with game cartridges. Others doing likewise include North American Philips Consumer Electronics Corp. of Warren, Mich., with its Odyssey system, and Astrovision of Columbus, Ohio.

Companies that produce only game cartridges also participate. Among them are Activision Inc. of Santa Clara, Calif., and Coleco Industries Inc. in Hartford, Conn. Activision says its sales grew from $5 million to $50 million in a year.

Video arcade games are a different breed, with a sturdier free-standing design to take hard use and more read-only-memory capacity to support fancier display, sound effects, and interactive play. Home game equipment, by contrast, is light and portable to plug into television sets and receive game cassettes. The games themselves are not only similar, but often identical. For now, none of the home games is compatible with the others, a situation that allows cartridge-only software firms to supply to many systems.

For any doubters, if the high poten-


**Supergame.** Due from Atari at midyear is this Video X advanced system. It uses a 16-bit microprocessor to provide a better picture and more performance. It is to retail at $350.

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tial underpinnings of the home video business, which pays handsome profits to suppliers and retailers for hot-selling products, needed further illustration, it was evident at the consumer show. Exhibits of video game firms lured throngs of retailers who looked for new best-sellers to match the Asteroids, Missile Command, and Space Invaders of last year. And they found offerings from Atari, Mattel, and others that promise the boom will continue, they say almost to a man.

Indeed, much of the financial excitement from video games stems from its so-called razor-and-blades marketing formula, where the nice profits from players—the razor—are eclipsed by the unending stream of software cartridges—blades—demanded by the dedicated gameplayer. Mattel Electronics Products president Joshua W. Denham, for instance, estimates that selling each Intellivision player creates an initial sale of up to five game cartridges, not to mention follow-ons. These go for an average of $21, with higher levels in the offing. Atari's prices are somewhat higher, as are those of the other cartridge sellers.

Player price tags have stayed stable. Atari recommends a $199 retail figure, and Mattel sells Intellivision for $210 wholesale. However, retailers discount, even though Atari and Mattel sold out all production. The upshot is that the Atari unit, when available, sells for about $130 and the Intellivision, around $250.

**Peek at Atari.** During the Las Vegas show, normally close-mouthed Atari gave financial analysts a clearer look at its operation, validating its proponents' claim it is "the fastest-growing technology company ever." Projections for 1982, if met, would sustain this momentum. Atari is fully booked for all its production of video computer systems and expects to sell about 6 million units.

Furthermore, the lineup of at least one new game each month ensures a flow of software. One, the home video version of Pac-Man, an arcade leader, promises to break the record of its Asteroids, which sold about $100 million worth in only six months last year.

While much of the 1982 product offering constitutes improved versions of last year's fare, both Atari and Mattel are polishing hardware that should break new ground. Leader Atari has a Video X advanced system, dubbed Supergame for the time being, that uses a 16-bit microprocessor, due for debut at midyear

## Game chip sales have bright future

Selling chips to home video-game manufacturers could become one of the best markets for semiconductor firms whose other markets are sorely pressed by recession. Consider: each player has a central processing system and associated random-access memory, dedicated graphic-display generator, standard read-only memory for line refreshing, plus other special devices depending on the design. The total cost is $15, and more than 10 million players will be sold in 1982. But that total pales beside the numbers for game cartridges, each of which contains at least one ROM chip that generates game action and character sets. More than 40 million were sold last year, with at least double that in sight for 1982, at about $2 for a 16-K ROM and $2.50 to $2.75 for a 32-K version.

To date, General Instrument Corp.'s Microelectronics division, Hicksville, N. Y., has been the leading supplier to game builders. Its vice president and general manager, Bernhard J. Rohrbacher, referring to shortages, flatly predicts: "Growth of this business will not be held back by a silicon shortage." Other semiconductor executives echo him and note that substantial orders are starting to flow.

Besides GI, which not only sells standard 16-K and 32-K ROMs for cartridges, but supplies Mattel Inc. with its central processing system, other major ROM producers are: Honeywell's Synertek subsidiary in Santa Clara, Calif.; American Microsystems Inc. and National Semiconductor, both also in Santa Clara; Rockwell International's Device Products division, Anaheim, Calif.; and Toshiba Semiconductor (USA) Inc., Sunnyvale, Calif. **-L.W.**

and retailing at $350. For this price, the additional power and memory will mean a better picture and more performance from a single hand-held controller that combines joy stick, paddle, and keyboard. Upgraded versions of present games have animated graphics, too, Atari says, which provide more exciting play.

Although Atari hints at speech capability later, Mattel has beaten it to the punch with its Intellivoice voice-synthesis module, a first for the video game. To be available in late spring, the Mattel module uses a General Instrument Corp. voice-synthesis chip set with male and female voices that introduce games, "cheer winners, warn of imminent danger, and offer strategic assistance," according to the company.

Industry sources report Atari, accustomed to being the trail-blazer, is miffed by Mattel's voice offering and some of its officials are predicting its failure. They note that speech previously has bombed in the game business because it largely was an expensive add-on gimmick, not integrated into the game itself [*Electronics*, June 2, 1981, p. 42].

**Impressive talk.** Show-goers rated Intellivoice's chances as the best yet for game speech, noting it seems to offer an attractive new dimension of interactive play. The big drawback is its plug-in module status, which consumers might pass up, they say.

With video growth largely set through 1982 based on orders already in hand, suppliers are planning further ahead and like what they see. The U. S. market at year-end should have not much more than 15% penetration of color TV sets, against less than 7% now.

More, offshore business, principally Europe, is barely tapped at 1% penetration, points out Montgomery Securities' James. Atari alone, which sold 800,000 systems offshore last year, expects to boost this to 2.5 million—"and the prices run about double abroad," says James.

Capping off the promise is an edge not enjoyed by other parts of the industry: Japanese competition is not in the offing soon—although these firms do make arcade units. None of the major Japanese makers currently admits to plans to export home video games, a survey indicates. □





 


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Avionics

# FAA presses on-board anticollision unit

TCAS could start appearing in civilian aircraft by mid-decade if Reagan Administration's budget cuts don't intervene

*by Ray Connolly, Senior Editor*

**After more than** five years of studies and disputes, the Federal Aviation Administration has lined up the nation's airlines, pilots, avionics contractors, and the general aviation community to proceed with a new collision avoidance system. Called TCAS—for traffic alert and collision avoidance system—the two-part package for commercial air carriers and private pilots will be an air-to-air communications and warning system "capable of operating without reliance on ground equipment," says the FAA's Al Albrecht.

As associate administrator for engineering and development, Albrecht believes TCAS implementation can begin in the mid-1980s. However, other FAA officials, as well as aircraft and avionics manufacturers, warn that this timetable could easily slip if the FAA is subject to more Reagan Administration budget cuts, as expected.

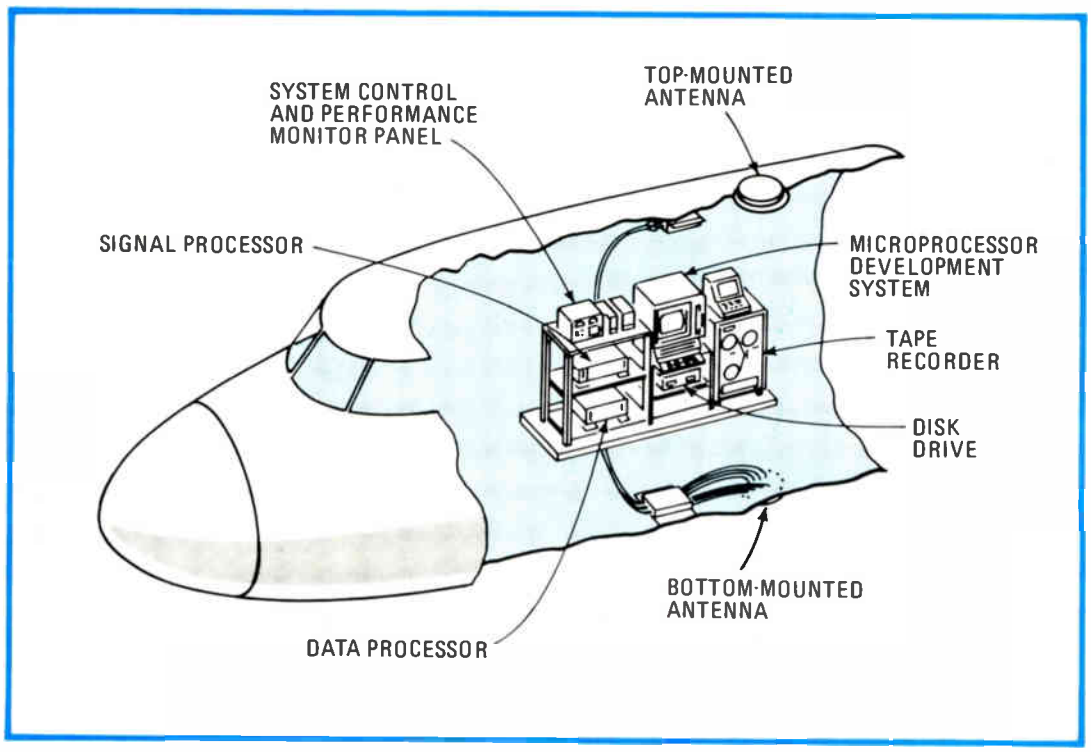
TCAS will come in three versions. The less complex and sophisticated model for small planes, TCAS I, which is currently at the flight testing stage, will cost $2,500 and up, depending on options. But the versions for larger planes, called TCAS II and enhanced TCAS II and which are still on the drawing boards, are expected to cost up to $50,000 per airliner.

The program calls for a draft of minimum operational standards, MOPS in agency argot, for TCAS II to be completed by June. For the upgraded or enhanced TCAS II, the final national standard and MOPS is due by June 1984.

The standard for all three TCAS systems is being drafted by a special committee of the Radio Technical Commission for Aeronautics. Albrecht calls the task of framing the standard for TCAS II "an immense undertaking," but says he is optimistic that it can be completed on time.

**Group effort.** Organizations involved in the program's engineering development include the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., and its not-for-profit Mitre Corp., as well as the FAA Technical Center. Working on TCAS II hardware development is Bendix Corp., while TCAS I is evolving at the Dalmo Victor operation of Textron Inc.'s Bell Aerospace division.

Designed to operate in areas with as many as 0.32 aircraft per square nautical mile—the equivalent of the crowded Los Angeles basin, which has more than 90 planes within 10




**To prevent midair collisions.** This TCAS II system is from Bendix Corp., which is developing hardware for the FAA's proposed new collision avoidance system. Racks include radar displays, transponder, and signal processor.

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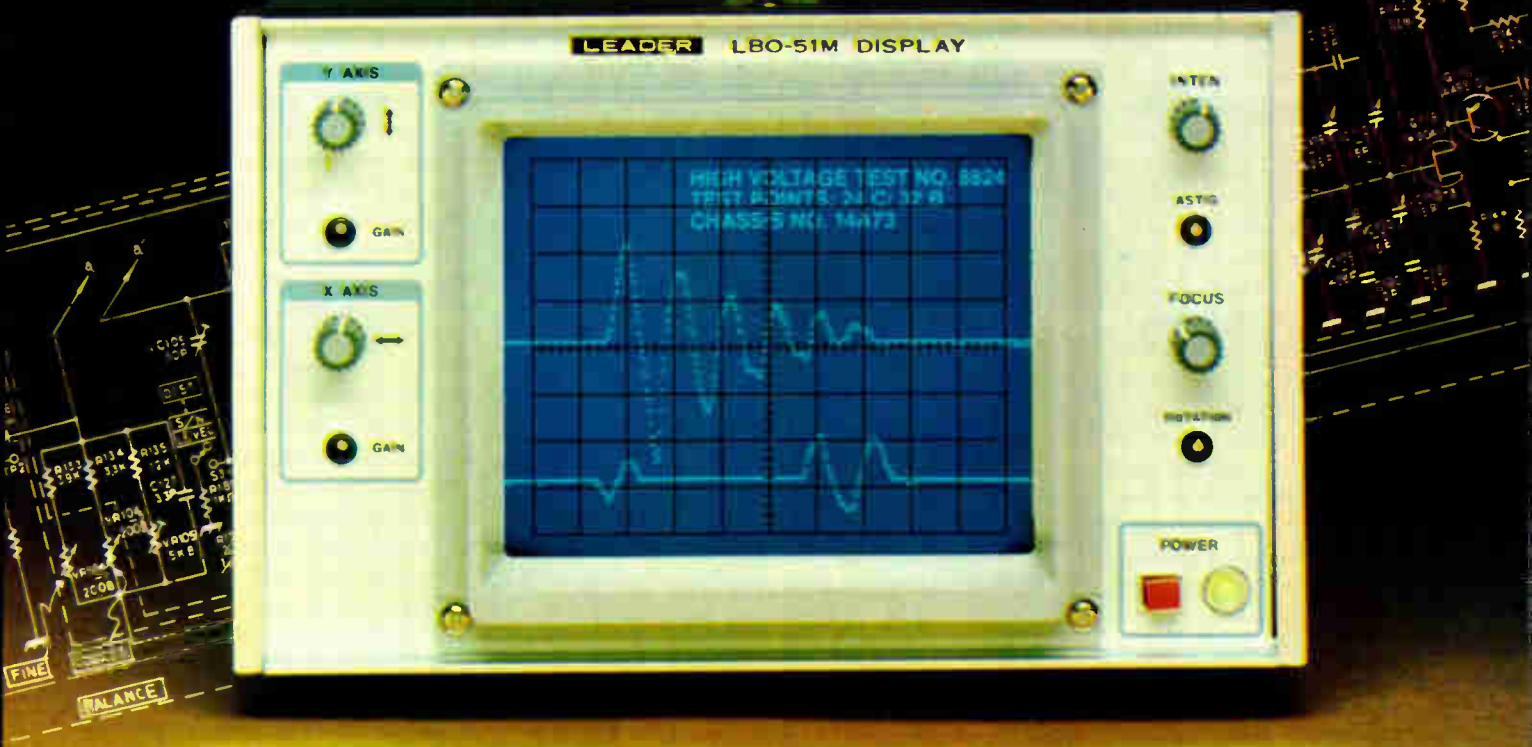


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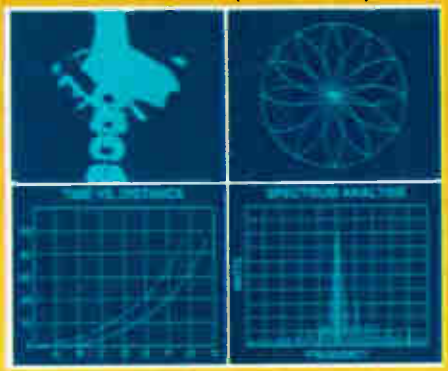

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## Probing the news

nautical miles of any given aircraft—TCAS II equipment will employ transponders to continuously interrogate sectors of the surrounding airspace.

Once contact is established with an intruder on a collision course, TCAS II will provide a cockpit-alert display, using video or voice, of the intruding aircraft's location, distance, and speed. At the same time, the system will compute and display a course that would avoid the potential accident.

The minimum TCAS II system to come first will generate resolution advisories in the vertical plane (climb and descend). The later enhanced TCAS II package is expected to be able to function in the horizontal, as well (turn right and turn left). If the intruder is also TCAS II-equipped, automatic air-to-air signals will ensure that both cockpit advisories are compatible. For example, one plane will climb while the other descends.

The communications link will employ the new Mode S transponder, a selective version of what the U. S. previously called DABS, the discrete-address beacon system. The Mode S refinement of DABS was adopted by the International Civil Aviation Organization last spring. While TCAS will not be dependent on ground terminals, the Mode S transponders will also be usable with new and upgraded DABS ground terminals, also to be called Mode S, and the system will also work with intruding aircraft equipped with today's conventional transponders known as ATCRBS, for air-traffic-control radar beacon system.

The FAA's Albrecht surprised conference participants with his disclosure that the agency "very recently held extremely successful tests" using a Mode S transponder "designed and built in the Soviet Union" and installed in an FAA aircraft.

**Taking cues.** TCAS I avionics, relatively low-performance hardware, will provide at the lowest level merely an intermittent light or audio alarm signal generated by another aircraft or ground station. Although the signal will get stronger as the planes near each other, the basic TCAS I mode will give no range, distance, or bearing. However, a TCAS II-equipped aircraft will broadcast an audio or video display alert to the intruder giving its position and course to the other craft.

Some idea of how TCAS is to work can be gained from examining the Bendix engineering model shown in the cutaway diagram on page 84. Based on equipment put together by the company's Communications division in Baltimore, the diagram shows the antennas and equipment rack. Top and bottom antennas pass signals via microwave cable through beam-forming and -steering network boxes to the cabin racks. They contain a panel with radar displays and a modified Teledyne instant vertical-speed indicator; the TRU-2 transponder; a modified TRA-65 interrogation transponder; a real-time signal processor designed by Bendix using an Intel 8086; and a processor containing five 8086s. There are also a floppy-disk drive and an in-fight performance monitor and data-extraction recording unit for tapes to be used by the FAA and other TCAS contractors.

TCAS I enhancements envisioned by the FAA include an alarm system that detects the location of nearby traffic by means of a direction-finding antenna, plus optional use of an altitude filter that would preclude alerts on traffic that is safely separated by altitude.

There are two means of eliciting transponder transmissions that trigger TCAS I alerts, says the FAA. The first is interrogation from secondary surveillance-radar ground stations that support conventional air-traffic-control operations. The second level is the intermittent, gratuitous transmissions put out at a low rate by the Mode S transponders. Called squitters by the FAA, these signals can also trigger an alert from other nearby transponders.

To counter what the FAA calls "asynchronous garble"—multiple responses from several nearby aircraft—TCAS will operate in what is known as a whisper or shout mode in which the cockpit-alert signal from the nearest threat will receive priority and override other incoming warnings. □

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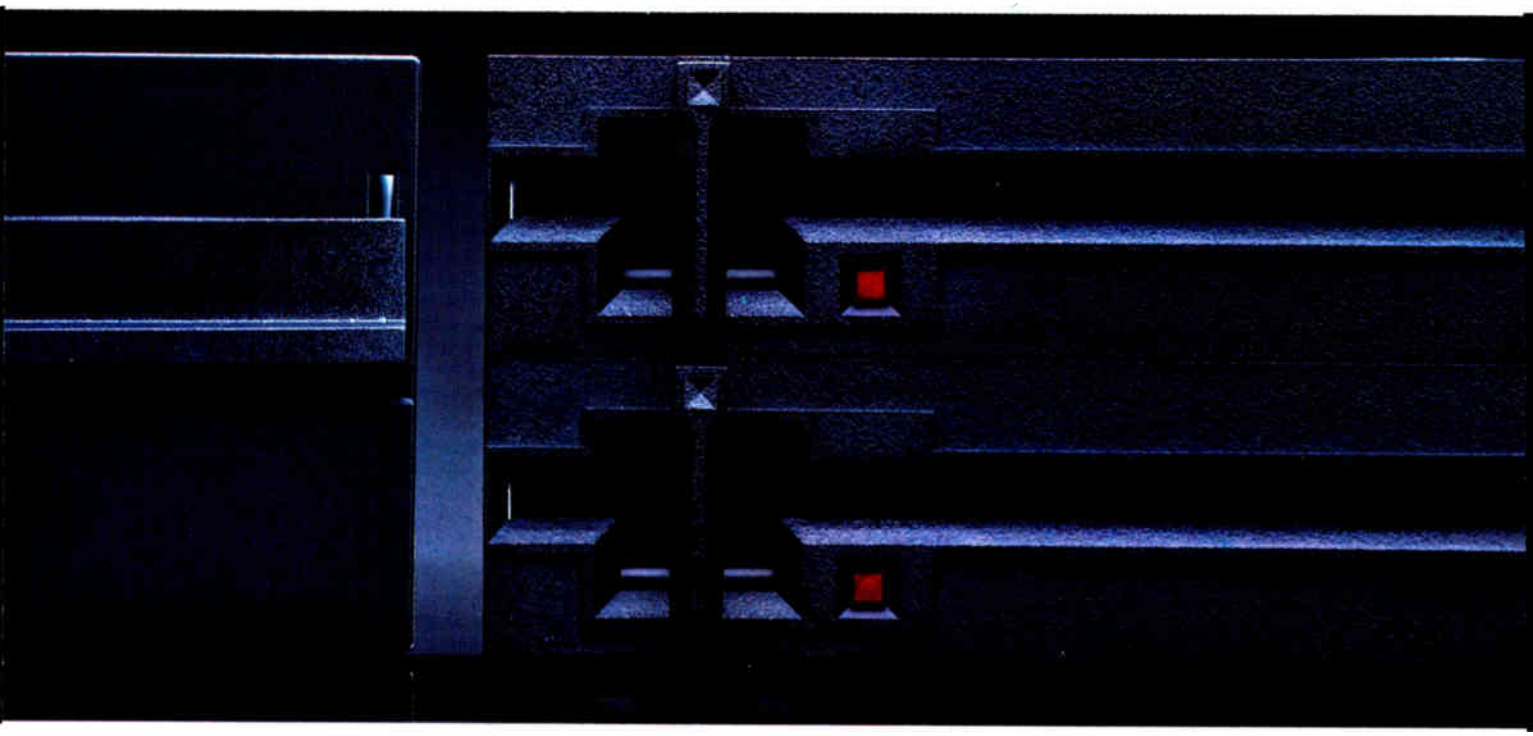

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# Local networks will multiply opportunities in the 1980s

## As local-net concepts spring up, OEMs and chip makers will benefit if they can sort out all the possibilities

by Harvey J. Hindin, *Communications & Microwave Editor*, and Tom Manuel, *Computers & Peripherals Editor*

☐ Local networks will provide two boons for the data-communications industry in this decade, and it is difficult to say which is the more important. They will allow small businesses to reap the benefits of data-generating and -receiving machines that communicate with each other and with those at remote sites. For large companies, local nets will take some of the data processing and communications out of the central corporate facility and put them at the departmental level, where they will be tailored to specific needs.

Local networks will also have an impact on the factory. Manufacturing management-information systems will be able to be linked with automated production systems. Separate local networks for the major computerized activities of a business—production automation, manufacturing information systems, and office automation—can be linked with corporate data-processing systems to enhance the speed and accuracy of the flow of information among them. The individual local nets will be extended into hierarchical networks linking all the information resources within a business and also tying into public information nets.

These benefits mean new opportunities will open at a rapid rate for original-equipment manufacturers. Some of these OEMs have already gotten on the bandwagon with either the local network itself or transceivers and interface gear for data-generating and -receiving equipment. Others, less ambitious, are content to supply the needed coaxial cable and small computers that can operate either in a stand-alone or local-net mode.

A lot of work remains, however. For example, the opportunities for the chip manufacturer are great. The most obvious new chips will set up Ethernet networks—these are being designed by Intel and others. Nor are other local networks being ignored. For example, Datapoint has developed a special chip to interface gear to its Arcnet. But these two undertakings are only the beginning of the opportunities for chip makers.

Unlike the integrated circuits hooking up mainframes in the older architectures such as IBM's point-to-point, Systems Network Architecture, local-net chips need to work with a bus structure. Thus the kinds of data-communications controller, interface, and other such chips that are needed vary widely from those designed in the past. Today these requirements are met by medium-scale ICs. Tomorrow they will be met by one-chip large-scale ICs.

High entry costs mean that most of these chip requirements will probably be met by the traditional vendors. Yet, new suppliers might gain entry by designing a chip in conjunction with an equipment supplier who wants to make such an IC compatible with local networks.

Other opportunities abound in communications software. Thus IBM's already-announced 16-bit Personal Computer—if included in local networks much like the Apple 8-bit machines are included now—will need a lot of communication software. The same requirement holds for Tandy Corp.'s soon-to-be-announced 16-bit personal computer. Tandy has already set up its 8-bit TRS-80 model 2 machine to be compatible with Datapoint's Arcnet. The firm is sure to try to make similar local-net arrangements for its 16-bit machine if it is to compete with IBM and Apple and others in the office-automation markets.

The first of the following two articles is an overview of today's available local networks from Architecture Technology Corp. It rounds up what the data-communication manager can choose from to meet his needs, which vary widely from application to application.

The second article is an excellent example of just how software, in the form of an operating system, can affect local-net data communications. It discusses Digital Research Inc.'s development of an operating system that lets CP/M-based computers talk with one another. Read these in conjunction with the articles already published [*Electronics*, Aug. 25, 1981, p. 119] to get a good idea of the state of the art of local networks.

# Many makers unloose a flood of local nets

## This survey of the equipment available will orient the would-be network designer

by Kenneth J. Thurber and Harvey A. Freeman
*Architecture Technology Corp., Minneapolis, Minn.*

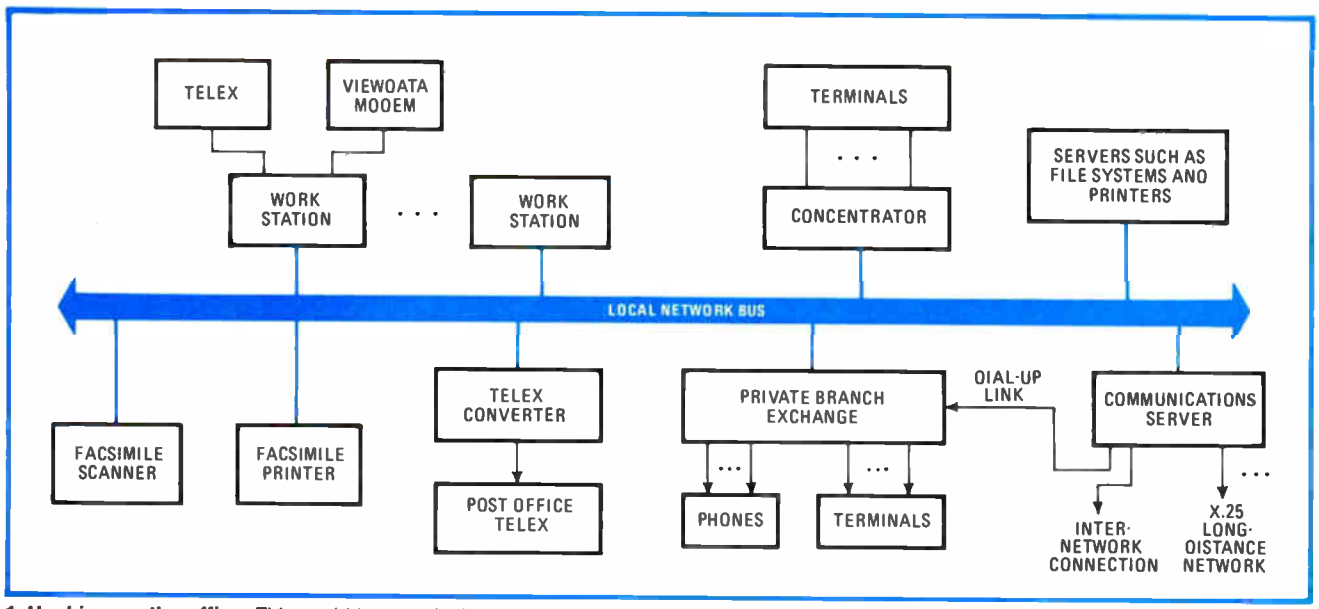
☐ Only four years ago just a gleam in a researcher's eye, today local computer networks are the up and coming technology in communications and are probably the fastest-growing segment of the computer industry. Over 100 companies now produce the hardware trappings for the local network, potentially one of the most pragmatic system concepts to emerge from a decade of thought on the subject of distributed processing.

The 1970s was the era of experimentation with distributed systems, which replace a mainframe computer and several terminals with multiple small computers. The 1980s will see their practical implementation in the form of the local network and its hierarchical system extensions. The concept is huge enough to dominate the marketplace in applications from office-automation to factory-management systems.

Though not precise, a workable definition of a local network is one where all the stations—computers, terminals, and other equipment (system nodes)—are located in a small geographic area—for example, within a radius of two miles. Typically, such a network is owned by a single organization and so tends to be more specialized than a widely scattered one. For example, the local network may be installed on a single floor of an office building and form the basic hardware and software structure for an office-automation system. Alternatively, it may be the basic element of a factory-automation system that collects data, monitors plant security with television cameras, and at the same time manages the energy usage in the building.

Figure 1 illustrates a typical local network that is used for office automation, showing the variety of equipment it may contain. Single ownership means that functions may be specialized, but this individuality also implies that the system may have to interface with others that are most probably dissimilar.

The short distances involved mean that communication among devices on the network is limited to the designated local area, unless the system is also connected into a long-distance network. Studies have come up with the information that the communication among coworkers in a business environment occurs within a distance of 5 miles approximately 60% of the time and over distances of 500 or more miles less than 10% of the time. Thus the local restriction of the network would in most cases have little detrimental effect.




**1. Hooking up the office.** This could be a typical local network for an office of the future. The local-network bus connects a variety of office equipment. The PBX, communications server, and telex converter provide access to the world beyond the proprietay local net.

Usually, networks are implemented using packet switching. That mode of operation is ideal for the bursts of traffic that customarily occur in configurations with many terminals.

Local networks can be variously categorized. The definition developed thus far is by K. J. Thurber and H. A. Freeman[1]. There are other suggested definitions and readings. For instance, D. D. Clark gives a detailed overview of the subject and reviews a particular system[2]. A. Franck and P. C. Patton not only survey the subject, but also illustrate developments in the area of large-computer local networks[3].

The article by I. W. Cotton[4], like Thurber and Freeman's, is important because some researchers feel that the term local network necessarily implies a system such as Xerox Corp.'s Ethernet. Rebutting this, Cotton and Thurber and Freeman show more varieties than just this packet-switched local network—for example, networks built upon circuit switches (private branch exchange technology) and such concepts as input/output channels and computer bus structures.

With the strides being made in PBX technology and its capabilities for the integration of voice and data and the advances in large-scale integration and bus structures, the less esoteric technologies demand equal attention. PBX makers such as Datapoint, InteCom, Rolm, Mitel, Northern Telecom, IBM and Nixdorf in Europe, and others offer data communications along with voice [*Electronics*, April 7, 1981, p. 139].

### Stars of the constellation

The proliferation of local-network concepts is not letting up. Close to 120 companies are either building or about to embark on a project in this field and there is an impressive base of local-network systems already installed. For example, Datapoint Corp. of San Antonio, Texas, reportedly has over 15,000 installed bus interfaces in over 1,500 Arcnets worldwide.

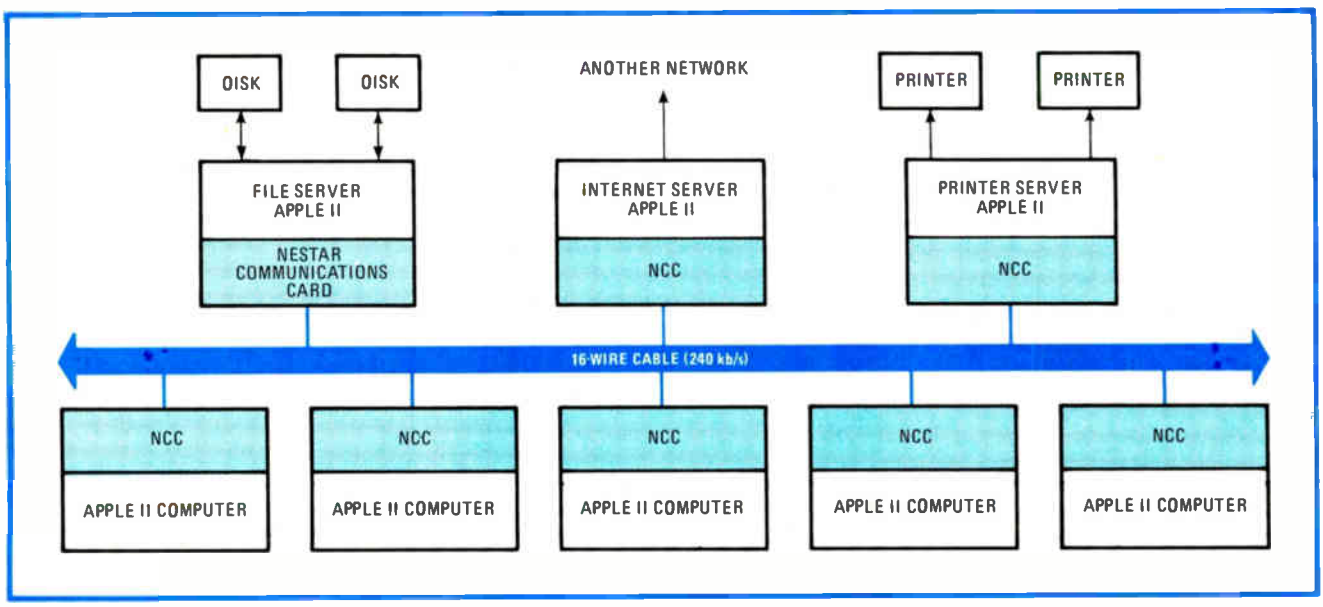
In contrast, however, Sytek Inc. of Sunnyvale, Calif., has just recently begun to produce and deliver bus-interface hardware and has entered the emerging market for radio-frequency–based local networks with a product called LocalNet. Until recently, Sytek had concentrated on systems design—now it is actually building sophisticated products. Printer Terminal Communications Corp. of Ramona, Calif., provides a wireless local network known as Local Area Data Distribution (LADD).

Because of this wide range of companies and products, only a representative sample, as follows, will be used to illustrate baseband networks. In the baseband technique, digital pulses are put directly on the cable without a carrier frequency, whereas in broadband schemes, a high-frequency carrier is modulated.

There are three levels of baseband local-network systems, categorized by performance and hardware complexity: the low-performance area at less than a megabit per second, the midperformance range between 3 and 10 Mb/s, and the high-performance nets at 50 Mb/s. Examples in each of these performance ranges are: in the low-performance, low-cost range, the Nestar ClusterBus; in the mid-range, the Xerox Ethernet, the Network Systems Corp. Hyperbus, and the Ungermann-Bass Net/One; and in the high-performance range, the Network Systems Hyperchannel.

Again, the wide variety of equipment and the attendant design goals impede comparing local network systems in a meaningful way unless there is a specific design problem against which to trade them off. Subtle differences that are not obvious at first glance and that nonetheless can radically change the system capabilities prevent sweeping comparisons.

The Clusterbus from Nestar Systems Inc., Palo Alto, Calif. (Fig. 2), is known as the Cluster/One model A, and it provides the designer with the ability to physically connect up to 64 Apple II computers [*Electronics*, June 16, 1981, p. 171]. The ClusterBus is a baseband contention-channel design, with parallel transmission of bytes over a 16-wire cable at 240 kilobits per second. The key




**2. Bushels of Apples.** The Nestar Cluster/One model A 240-kilobit-per-second local network connects as many as 64 Apple II computers together. It uses 16 parallel wires, either in a flat cable or as packaged, twisted pairs, transmitting data 1 byte at a time.

element of this system is an interface card that plugs into a peripheral slot on the Apple II—using the computer's power supply—which converts it from a stand-alone personal computer into a local-network work station.

Nestar sells a disk system designed to replace the floppy disks used on Apple II computers and to allow each Apple II station to work with the equivalent of 255 floppy disks. With the disk system the user receives a file server, and an electronic mail system is an option.

Corvus Systems Inc., San Jose, Calif., offers Omninet, a twisted-pair, 1-Mb/s baseband carrier-sense multiple-access (CSMA) network for the Apple personal computer, the Digital Equipment Corp. LSI-11, and, in the second quarter of this year, for the IBM Personal Computer, the Xerox 820, the Nippon Electric Co. PC-8000, the Commodore PET, the Zenith Z89, the TRS-80 models I and II, the Superbrain, and S-100 bus personal computers [*Electronics*, Aug. 25, 1981, p. 125]. Also, Tandy Corp., located in Fort Worth, Texas, is using Datapoint's Arcnet technology to offer local networks for its TRS-80 personal computer.

The Xerox Ethernet (Fig. 3) is a joint specification with Digital Equipment Corp., Maynard, Mass., and Intel Corp. of Santa Clara, Calif. It is a 10-Mb/s baseband CSMA network that specifies the two lowest levels of the International Standards Organization open systems interconnection reference model.

Ethernet is the backbone of Xerox's office-automation strategy. The company offers a low-cost license for it, 95 of which have been purchased in the U.S. and West Europe, with another 300 being negotiated. In December 1981, Xerox published its higher-level Network Systems protocols, which covers levels 4 through 6 of the ISO OSI reference model. Intel will be putting the Ethernet interface circuitry on a chip that is slated to be available sometime this year.

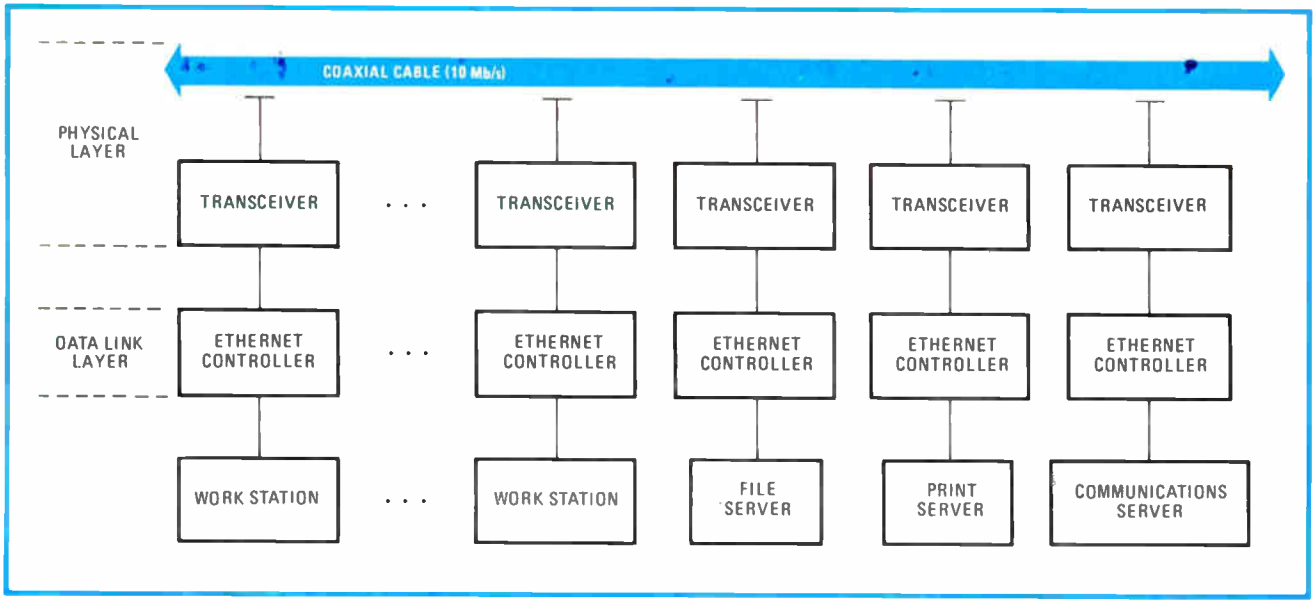
The Network Systems Hyperbus (Fig. 4) is a product planned by Network Systems Corp., Brooklyn Park, Minn., that is aimed at the midperformance range with its Bell System T2 speed of 6.312 Mb/s. The Hyperbus, sure to compete formidably with Ethernet, is designed to be compatible with multiple protocols including X.25, IBM's Systems Network Architecture, and Synchronous Data Link Control, and to interface with RS-232-C channels and IBM 3270 and compatible terminals. Hyperbus uses a hierarchical addressing concept that will give it a substantial advantage over systems like Ethernet in hierarchical-network implementations. The system entered beta test at a site with 20 nodes in mid-1981 and is scheduled to be available for purchase in quantity by the middle of this year.

The Ungermann-Bass Net/One (Fig. 5), currently available, is also designed to compete in the mid-range. It performs at 10 Mb/s, is Ethernet-compatible, and is also targeted for the RS-232-C and IBM 3270 markets. Additionally, the system is specifically designed to evolve along with Ethernet and track its design changes as closely as possible. As it now stands, the system allows for the connection of up to 16 RS-232-C ports to an adaptor and has been widely installed.

Of particular interest is Net/One's installation at the U.S. Military Academy at West Point, which has Prime, Univac, and Terac equipment and a variety of terminals. A system model is being developed at West Point that will provide a tool for design of Net/One installations. Although the current product closely follows Ethernet, the design has been modularized to allow for alternative media and media-access techniques such as broadband and token rings.

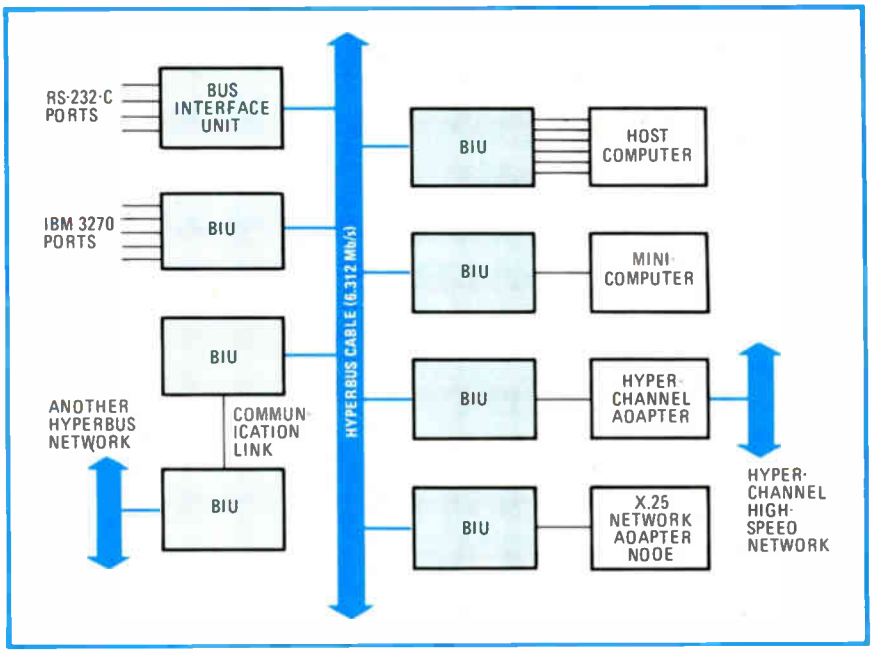
In the high-performance area, the only available system of local-network components is the Network Systems Hyperchannel. Hyperchannel provides the user with the ability to connect to most of the popular mainframes, but it is complex and thus costly. An adaptor for the channel costs about $40,000, though with it the user can connect to four independent channel trunks.

The hardware technology exists—though it would hardly be cost-effective—to connect every terminal in




**3. Ethereal.** The Ethernet local network, developed by Xerox Corp. and supported jointly by Xerox, Intel Corp., and Digital Equipment Corp., forms the basis for Xerox's thrust into office automation. Ethernet specifies the protocols for the two lower layers of a layered architecture.

**4. Variety.** The Hyperbus local network now under test has been designed for compatibility with many existing protocols such as the international standard X. 25, RS-232-C, IBM Systems Network Architecture and 3270, and various minicomputer systems. The design embodies hierarchical addressing.




the world and, under some suitable performance constraint, find a clear pathway for their communication through many levels of networks of varying lengths.

## Networks of networks

The future of network architecture is tending toward just such a hierarchy of networks, if on a smaller scale, and Fig. 6 shows a conceivable version. The concept is based on the premise that high volumes of communication are local and that communication among devices is inversely related to their distance apart. A hierarchy allows for economies of scale by limiting high-volume communications to the local level. With cost-effective devices that allow terminals to connect into the network, the local network can muster the aggregate capabilities that justify its connection to a larger, more capable system. Besides proving itself on a cost basis, the hierarchical configuration lines up with its user's structure, traffic patterns, and technology.

The system boasts other important benefits as well. In addition to simplifications in complexity and cost, subsystems within the hierarchy can be updated or changed with minimal material impact.

Local networks and hierarchical networks are ideas that developed by building on one another, an encouraging progression that generates the hope that future such innovative systems and their interrelationships will also come about. In fact, already, the movement to local networks and the emergence of personal computers have given rise to the concept of local networks composed of personal computers.

Personal computers are very capable and versatile devices, with some rather persuasive advantages over large systems. For example, the smaller computer is dedicated to an individual, so that the hardware and software can be custom-tailored to suit needs and capabilities. Nonetheless, there are cost problems with such devices—the personal-computer user may desire a letter-quality printer that not only is expensive but most probably will seldom be used by a single individual. Address space and on-line information storage are often limited.

The personal-computer network can resolve some of these problems. For example, the computers can share a printer and perhaps a large disk. In turn, if such features are provided from the network, then it may be possible to simplify the individual work stations. Clearly, the proper design and integration of a set of personal computers into the local-network configuration should allow advantageous use both of personal computers and of a large pool of expensive resources.

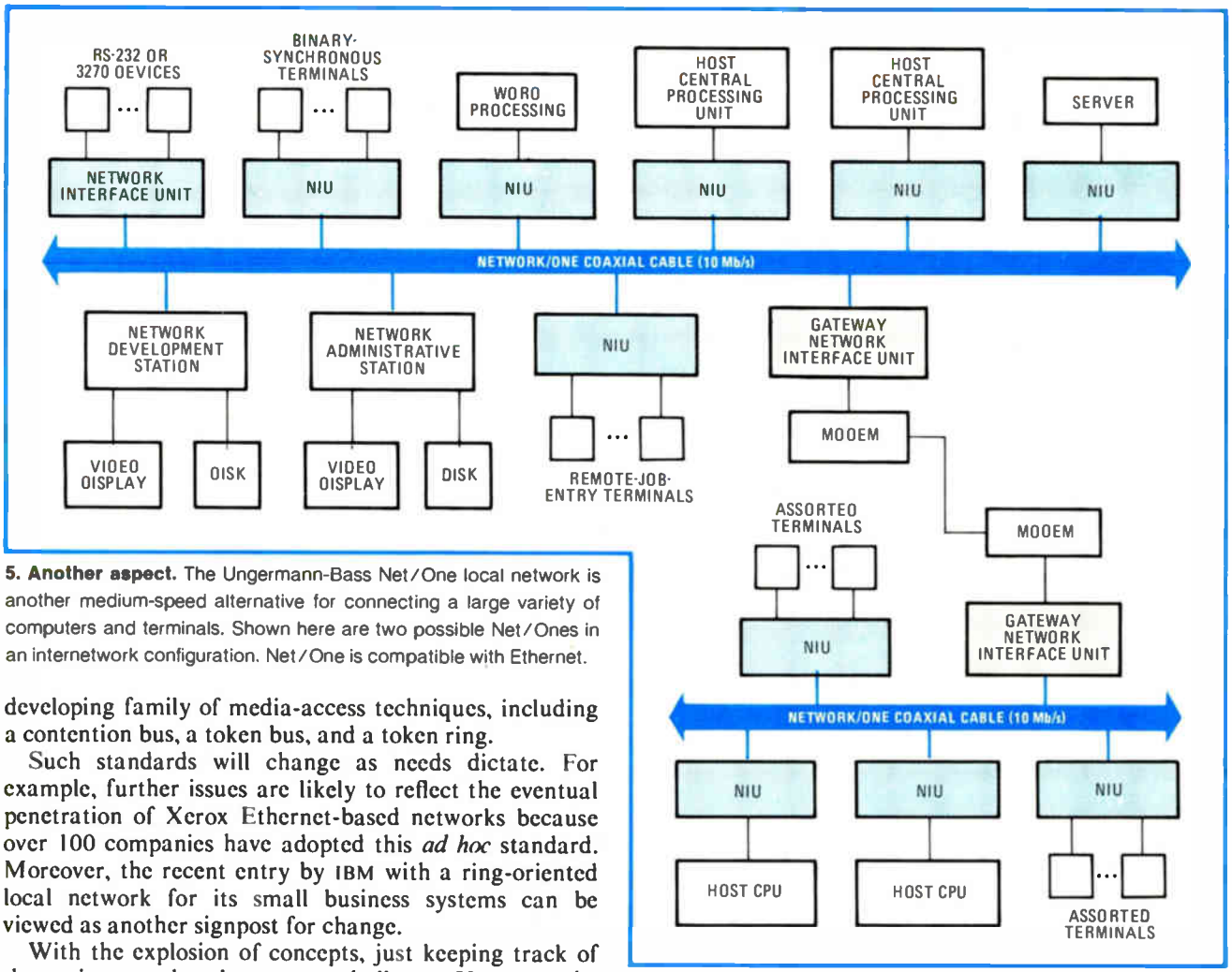
Such a system, from Nestar, has been applied in a number of dissimilar environments: schools, where it is used to transmit files to elementary-school children learning to program on Apple II computers (a highly rugged environment); in real-estate firms; and in diverse consulting houses.

An advocate of the local-network system for personal computers, Architecture Technology Corp. has designed a system using Nestar's hardware and software. It plans to develop the network over a period of time into a test-bed for internetworking, or linking, two or more networks and for interfacing equipment from different sources with the network.

## Fighting through the maze

The field of local networks is growing so fast that the biggest problem a designer faces is matching a specific piece of hardware to a specific goal. The selection is not at all obvious because of the many choices. Further, very little software is available to the user off the shelf. There are a few standard drivers for some specific I/O systems and some other pieces of software, but as yet the designer must really design the entire system.

In addition to such technical selection issues there are a wide variety of political issues. For example, no standards exist. The Institute of Electrical and Electronics Engineers, however, is trying to rectify this situation with its IEEE standard 802, which today consists of a




**5. Another aspect.** The Ungermann-Bass Net/One local network is another medium-speed alternative for connecting a large variety of computers and terminals. Shown here are two possible Net/Ones in an internetwork configuration. Net/One is compatible with Ethernet.

developing family of media-access techniques, including a contention bus, a token bus, and a token ring.

Such standards will change as needs dictate. For example, further issues are likely to reflect the eventual penetration of Xerox Ethernet-based networks because over 100 companies have adopted this *ad hoc* standard. Moreover, the recent entry by IBM with a ring-oriented local network for its small business systems can be viewed as another signpost for change.

With the explosion of concepts, just keeping track of the various vendors becomes a challenge. However, the problem is compounded in that computer, PBX, and office-equipment manufacturers and the communications companies all see the design of local communication systems as the key element in their entry into the potentially lucrative market for the office of the future. The state of the art is changing so fast that related information is outdated after six months.

However, some detailed fundamental questions remain unanswered—key design problems like choosing baseband versus broadband (rf) transmission; the effect of the backoff algorithm; the transaction vs file-transport nature of the systems; and the design of gateways.

Many local-network approaches make use of baseband-transmission schemes. Rf schemes have their proponents, because they promise to spare bandwidth by allowing multiple signals to be sent on a single available cable such as a cable TV system. A deterrent, though, is the relatively high cost of the rf modem, which bucks up the whole system's price.

Further, because the broadband network must be engineered as a total system, the initial installation and changes are expensive and difficult. Maintenance costs also are higher than those for baseband systems because the broadband type requires frequent balancing and the baseband, none. The Sytek system, though, proves that a cost-effective wideband system is in fact possible—one of the Sytek interfaces is available for $1,000, about the same as a comparable Ethernet part.

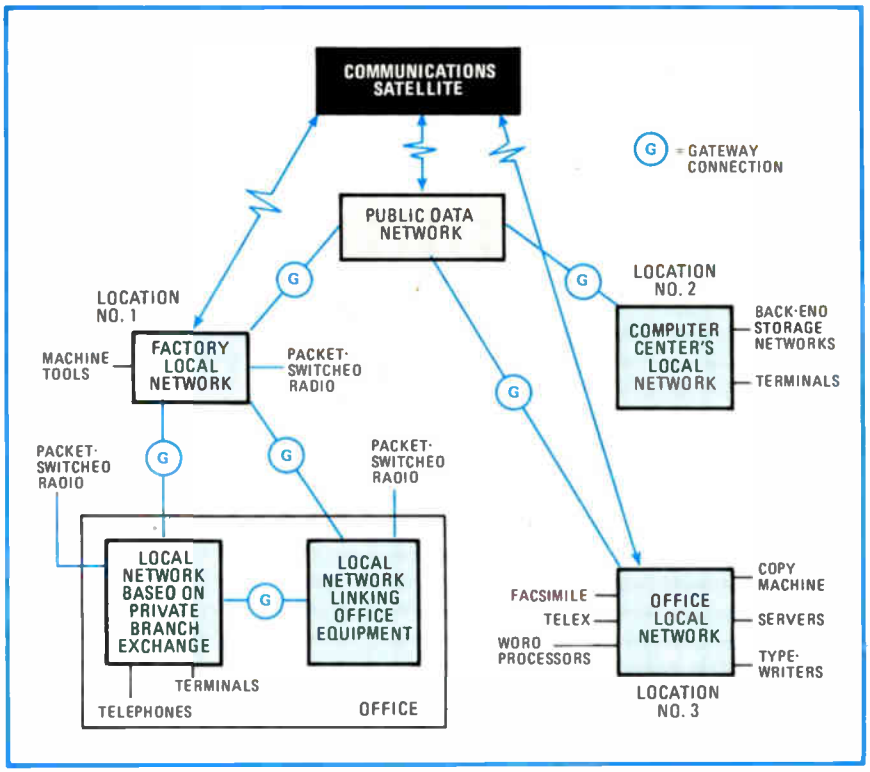
Another broadband network—Wangnet—was recently announced by Wang Laboratories Inc. of Lowell, Mass. However, just as it is difficult to compare baseband equipments, their differing capabilities prevent a fair comparison of wideband networks. It is safe to say, though, that the rf and baseband technologies will both be viable for the near future.

When two or more stations try to transmit on the cable at the same time, a data collision occurs and none of the transmissions can be used. The stations must wait and try again later. There are a number of schemes by which each of the stations can determine its waiting time—since there is no controlling station in collision-detection networks of this type, all stations must decide when to make a second attempt and of necessity must not all try again at the same instant.

It is possible and even easy to design a backoff algorithm that is quite efficient for light to medium loads on the net. However, design of a good one for heavy loads can be quite difficult. Like any good system design, a local-network setup will address the complete spectrum of issues associated with the use of the system during those periods that are most heavily loaded.

As an example of a backoff algorithm, the Ethernet

**6. Future link.** A hierarchical network for the future might look something like this, if designed for the communication links required by an organization. Different communications technologies are used where they are most cost-effective.




standard is one that appears to work well over a wide range of loads. The Ethernet backoff time is a random interval generated by a binary exponential algorithm. The interval is adjusted in proportion to the number of collisions that have occurred for the current transmission—as the number of collisions increases, so does each successive waiting time.

When a collision occurs, each station's Ethernet controller generates a new random retransmission interval based on the updated collision count. The retransmission intervals are multiples of what is called a slot, that is, the maximum time between starting a transmission and detecting a collision, or one end-to-end round trip on the cable. Each controller begins transmission of each new packet with a mean retransmission interval of one slot. In every instance when a transmission attempt ends in a collision, the controller waits for a random interval with a mean duration that is approximately twice that of the previous interval.

Many local-network products are designed for on-line terminals that produce a high volume of interactive traffic. But, once installed, the networks seem more suited for large-file traffic, and so manufacturers must consider designs that are transaction-oriented. The user should note when selecting a design that the cable used with the system can meet the required traffic loading.

## Many players

Since systems are being designed by so many manufacturers, gateway devices will have to be provided to link one local network to other proprietary local and geographically distributed networks. Some of these systems can be quite complex, so the matter of gateways should be one of the early design considerations, to minimize design and manufacturing costs.

As the technology of local networks begins to stake a claim on the market, the concept is being embraced by the major mainframe and minicomputer companies. The office-equipment group led by Datapoint's four-year-old ARC (Attached Resource Computing) system and Xerox's Ethernet, along with the competitive products from Wang, Digital Equipment Corp., Prime, A. B. Dick, and others, is fast becoming a battleground for the medium-performance local-network system. The entry of independent manufacturers such as Nestar, Corvus, 3COM Corp., the Destek Group, SDSystems, and Interlan Inc. is both enriching and heating up the competition, no doubt spurring the technology's advance.

Because of the meteoric growth in local networks—from $100 million in 1981 to possibly over $5 billion in 1991—the market will not thin out for yet some time. The current demand and the potential market size dictate that there can be unabated growth for two to three more years before the initial shakeout.

The comers of this burgeoning technology are the network hierarchies with local networks as the cornerstone. The emergence of practical systems with the integration of satellites, microwaves, and other long-haul mechanisms into interconnected local networks will cause the expansion of the technology to increase at a far faster rate than the original researchers envisioned. □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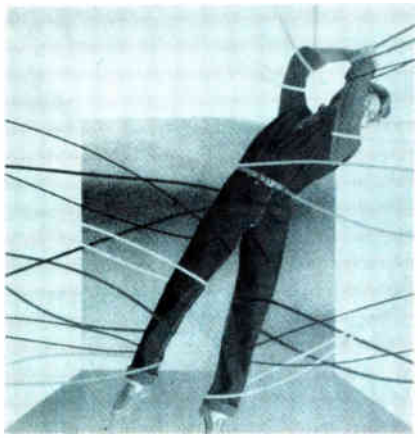


# Microcomputer software meshes with local nets

## CP/M-based line of operating systems expands to meet needs of varied local-network configurations

by Thomas A. Rolander, *Digital Research Inc., Pacific Grove, Calif.*

☐ Microcomputer operating systems are expanding in power and capabilities, just like the hardware they control. From their inception in modestly endowed single-user environments, this software has grown to serve a cluster of users sharing an inexpensive microcomputer and the expensive peripherals that can hang on it. The next step was an operating system for a network of microcomputers that shares memory resources and other peripherals, and beyond that are variants that run other network configurations.

A prime example of the growth of these operating systems is the family offered by Digital Research. It includes the single-user CP/M, which stands for control program for a microcomputer. There are currently more than 200,000 microcomputers using CP/M in over 3,000 different hardware configurations. More than 400 original-equipment manufacturers are using CP/M-based operating systems.

The next step in the evolution of these operating systems was to develop MP/M, a CP/M-compatible multiprogramming monitor. It enables multiple users to share expensive peripherals, as well as allowing each user to perform more than one task simultaneously, such as editing, compiling, and printing. However, MP/M does require a communal central processing unit. Thus the next evolutionary step is CP/NET, which stands for a control program for a network. It combines single-user slaves executing CP/M with masters executing MP/M to manage the shared resources.

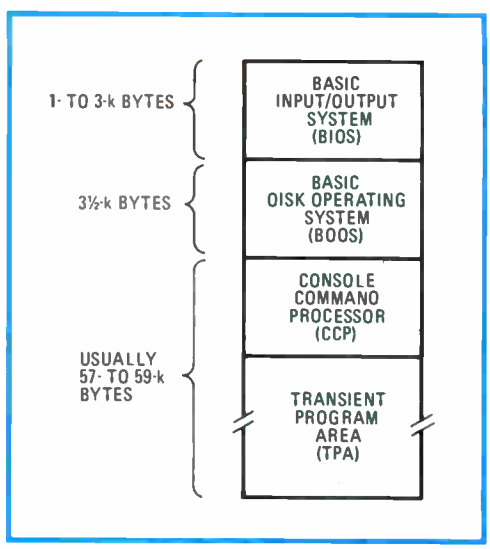
The entire family of operating systems from Digital Research is portable—each system is divided into an invariant portion that is the same in every application and a variant portion that is customized by the user. The invariant part is sometimes called the logical portion because it maps the data structures onto an arbitrary disk, console, and printer. The variant part is often labeled the physical portion because it contains the device drivers for each configuration.

CP/M is a monitor and control program for microcomputer systems, providing a general environment for program construction, storage, editing, assembly or compilation, program debugging, and application-program execution. An important feature is that it can be easily altered to execute on nearly any 8080, 8085, Z80, or 8086 or 8088 microcomputer configuration. As a single-user operating system, CP/M is quite small and fast and requires very little overhead.

### Four parts

There are four parts to the CP/M configuration (Fig. 1). The invariant portion is called the BDOS, for basic disk operating system, and the variant portion is called BIOS, for basic input/output system.

The BDOS has a single entry point at absolute memory location $0005_{16}$, which provides application programs access to a number of system functions including console, printer, and disk operations (see Table 1). It should be noted that the disk read and write operations are particularly simple because they operate on fixed-length, 128-byte sectors on up to 16 disk drives, each of which may hold 8 megabytes with an independent file directory on each drive. Examples of such mass storage devices are minifloppies, single- or double-density floppies, and hard disks.




**1. Memory configuration.** In CP/M, the BIOS portion contains the code that is hardware-specific, BDOS has the disk routines common to all CP/M systems, the CCP communicates with users' terminals, and the TPA holds users' programs.

The BDOS implements disk-allocation strategies that provide fully dynamic file construction while eliminating the possibility of lost and doubly allocated blocks. Thus files do not require space to be preallocated to them, and they can be extended at program-execution time to contain any number of records, up to the size of any single disk.

The BIOS portion provides the primitive operations necessary for access to the actual console, printer, and disk drives resident on a

TABLE 1: CP/M OPERATING-SYSTEM COMMANDS

| Command | Description |
|---|---|
| Search | look for a particular disk file by name |
| Open | open a file for further operations |
| Close | close a file after processing |
| Make | make the specified new file |
| Delete | remove the specified file and free the disk space |
| Rename | change the name of a particular file |
| Read | read a record from a particular file, sequential or random |
| Write | write a record to a particular file, sequential or random |

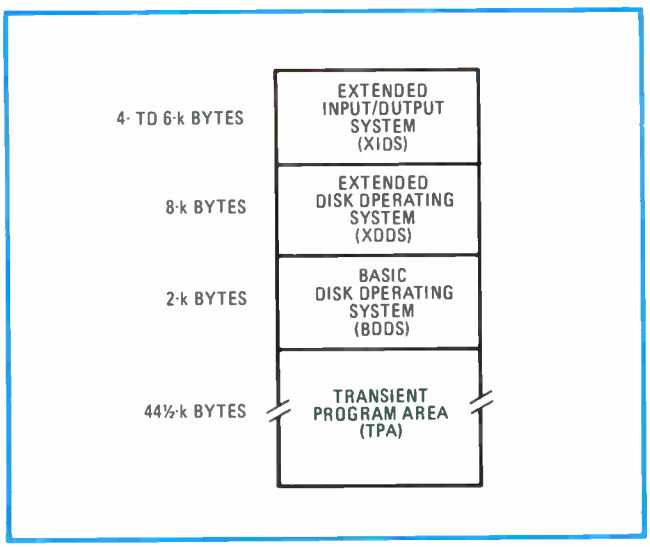
particular system. The interface with BIOS is provided through jump vectors, located at its beginning address, which identify a sequence of 17 subroutines. CP/M can be customized for any particular hardware environment by replacing this BIOS portion.

The third part of CP/M, the console command processor, provides the user interface between the console and the operating system. The CCP reads from the console and processes commands. Some of these commands are termed built-in, because they are a part of the CCP program. Other commands, called transient, specify programs to be loaded from disk and executed, such as editing and debugging routines.

The last segment of CP/M is called the transient program area. The TPA holds programs that are loaded from the disk and executed by the CCP. During program editing, for example, it holds the machine code for a text editor and the data areas. Similarly, programs created under CP/M can be debugged and executed by loading and running them in the TPA.

The MP/M operating system is an upward-compatible version of CP/M with a number of added facilities. Compatibility was essential in order to let the large existing base of CP/M software run with little or no modification.

From the perspective of the user, MP/M is simply a




**2. Multitasking configurations.** The MP/M multitasking operating system adds to the CP/M memory-space configuration XDOS, which contains the real-time nucleus. It also extends the BIOS basic input/output system, renaming it XIOS, for extended I/O system.

TABLE 2: MP/M ADDITIONAL FACILITIES

| |
|---|
| multiterminal support |
| multiprogramming at each terminal |
| support for bank switched memory and memory protection among banks |
| concurrency of input/output and processor operations |
| interprocess communication, mutual exclusion, and synchronization |
| ability to operate in sequential, polled, or interrupt driven environments |
| system timing functions, including the time of day |
| logical interrupt system utilizing event flags |
| selection of system options at system generation time |
| dynamic system configuration at load time |
| spooling list files to the printer |
| scheduling programs to be run by data and time |

multitasking CP/M system. It contains a priority-driven real-time multitasking nucleus that provides process-dispatching, memory-management, and system-timing functions. In general, these added facilities (Table 2) are transparent to the user, though a number of system functions have been added.

The BDOS used by MP/M has been taken directly from CP/M and is executed as a serially reusable resource through a mutual-exclusion queue that controls access to the code. This approach achieves two goals. First, the corresponding disk drivers can be taken directly from CP/M, requiring modification of only the busy-wait loop for I/O completion. Second, simplicity and size advantages were gained by avoiding a reentrant disk-file system. In fact, MP/M is comparable in size to several other single-user microcomputer operating systems.

To BDOS, the MP/M configuration adds two parts (Fig. 2): XDOS, for extended disk-operating system; and XIOS, for extended I/O system. The XDOS contains the MP/M real-time nucleus for multitasking. The nucleus contains the process dispatcher, queue management, flag management, memory management, terminal handler, command line interpreter, and time-base management routines. The system calls are summarized in Table 3.

## Queue management

XDOS provides several essential functions in a multitasking environment, notably queue management. In essence, a queue is a memory-resident first-in, first-out disk file. Queues can be used for the communication of messages between processes, to synchronize processes, and to provide mutual exclusion.

MP/M simplifies queue management for both application programs and system processes by treating queues in a manner similar to disk files. Queues can be created, opened, written to, read from, and deleted.

The command-line interpreter, contained in XDOS, processes commands passed from the console. The CLI reads the header record of the program to be executed, determines the program size, loads and relocates the program into the best-fitting memory segment, and then

TABLE 3: MP/M ADDITIONAL SYSTEM SUBROUTINES

| Name | Description |
|---|---|
| Rel_mem_rqst | relocatable memory request |
| Poll | poll specified device |
| Flag_wait | wait until specified flag is set |
| Flag_set | set specified flag |
| Make_queue | make the specified queue |
| Open_queue | open a queue for further operations |
| Read_queue | unconditionally read a message from a queue |
| Cread_queue | conditionally read a message from a queue |
| Write_queue | unconditionally write a message to a queue |
| Cwrite_queue | conditionally write a message to a queue |
| Delay | delay for a specified amount of time |
| Term_process | terminate a process |
| Create_process | create a process |
| Set_prior | set process priority |
| Attach_cns | attach console |
| Detach_cns | detach console |

creates a process to execute the program. The XIOS part provides the primitive operations necessary to access multiple consoles, printers, and disk drives. Also, it performs device-polling, interrupt-handling, and memory-management functions that support bank-switched memory. The interface with the XIOS is provided through jump vectors, beginning with 17 jump instructions identical to those in the CP/M BIOS and continues with eight more jump instructions. MP/M can be customized for any particular hardware environment by replacing the XIOS portion.

Although MP/M achieves the goals of multitasking and of sharing expensive peripherals, it also shares the CPU resource. CP/NET allows the sharing of expensive peripherals, as in a multiuser system, while maintaining the advantages of an unshared CPU.

Thus CP/NET allows separate microcomputers to share and transfer disk files, to share printers and consoles, and to share programs and data bases. It consists of microcomputer masters running MP/M and slaves running CP/M. The masters are hosts managing the communal resources that can be accessed by the network slaves.

The design approach of separate I/O modules has been carried through to CP/NET. It is network-independent: all network-dependent code for the slaves has been placed in the slave network I/O system (SNIOS), and all network-dependent code for the master has been placed in the network interface process (NETWRKIF) module. Logical messages that are passed to and from SNIOS or NETWRKIF are transmitted over the network between masters and slaves using an arbitrary network protocol.

## MP/M-86 aims at commercial use

MP/M-86, the version of MP/M developed for the 8086 and 8088 microprocessors, was designed by a Unix buff, Frank Holsworth, who used his experience with that Bell Laboratories-originated operating system to design his own. He believes that MP/M-86 is "safer and more convenient to use in business environments, since the files are not linked together—avoiding greater information losses during system crashes—and the user interface is friendlier to nonprogrammers."

Unlike Unix, MP/M-86 is built around a shared file system, which features file and record lock-out to enable concurrent access of a common data base by multiple programs. The file system also includes features such as password protection at the file level. This protection gives selected users the ability to modify sensitive data while a broader class of users can only read it. With archive flags and times of last modification and last access included in the file system, incremental backups are easily accomplished in this operating system using standard utilities.

Like Unix, MP/M-86 has a multitasking environment that allows a single user to run more than one program at a time. This feature has been improved to allow a user to start a program, let it run for a while, and at any time, place it into the background. The appearance of a prompt then allows a subsequent command to be typed.

### CP/NET configurations

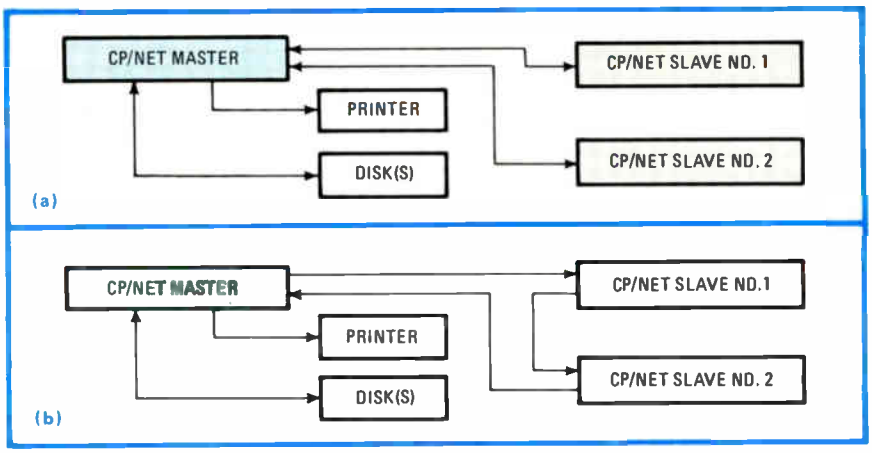
Figure 3 illustrates possible CP/NET configurations. The interprocessor message format permits multiple CP/NET masters so that, if the hardware capability exists, more than one master can be present in a net.

The slave portion of CP/NET is divided into two modules: SNIOS and the network disk-operating system (NDOS). The hardware-dependent SNIOS defines the low-level interface to the NDOS that is necessary for network I/O. Although a standard SNIOS is supplied by Digital Research, explicit instructions are provided for field reconfiguration to match nearly any network.

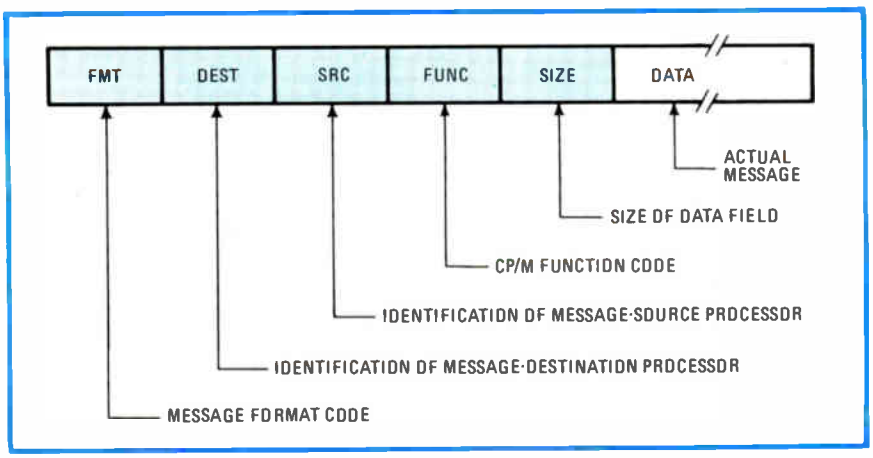
The purpose of the NDOS is to intercept all CP/M BDOS function calls and to determine if the operation is local, in which case control is transferred to the BDOS. If the operation is to be done on the network, the NDOS forms the appropriate logical message and sends it to the master via SNIOS.

The simple message format used by CP/NET for processor communication includes some packaging overhead plus the actual message itself (Fig. 4). The packag-

**3. Network configurations.** CP/NET can be set up to support the star (a), the ring (b), or other configurations, the only difference being the manner in which messages are transported. Any hardware network media will work with CP/NET.




**4. Message format.** Messages are sent around a CP/NET system using a fixed header format followed by a message of variable length that can be either data or commands or a mixture of both. The header defines the message's destination as well as its contents.




ing overhead consists of a message-format code, a CP/NET destination address, a CP/NET source address, a CP/M function code, and a message size.

The message format does not contain a cyclic redundancy code or any other error checking as a part of the packaging overhead. The user-written SNIOS can add the error checking when it actually places the message onto the network and then test it when a message is received from the network. This function is intentionally left to the user, avoiding redundant error checking where standard interface protocols, both in software and hardware, may already provide error checking.

The network interface processes, part of the user-written NETWRKIF module, perform the actual I/O for the CP/NET master. Typically there is one network interface process per slave that is supported by the master.

Queues are used to pass messages between the interface processes and the slave-support processes. The slave-support processes are provided for the CP/NET master in the form of a resident system process.

In CP/NET, the MP/M master manages resources that are considered public to the network. On the other hand, the slaves executing CP/M have both access to the public resources of the master and their own local resources that cannot be accessed from the network.

This choice of architecture guarantees the security of the resources of the slave while still permitting resources of the master to be shared among the slaves. The distinction between masters and slaves is also based on the ability of the MP/M masters to respond to the network asynchronously in real time, whereas the CP/M slaves perform sequential I/O and are not capable of monitoring a network interface in real time.

CP/NET is the first of a family of network operating system products from Digital Research. The second is named CP/NOS and is intended for applications in which the slave microcomputer has no disk resources and is therefore unable to run CP/M.

## Extensions to the family

CP/NOS consists of a bootstrap loader, which can be placed into a read-only memory or programmable ROM. It is a skeletal CP/M containing only the console- and printer-interface functions, and the logical and physical portions of the CP/NET slave. At the user level, CP/NOS provides a virtual CP/M system to the slave.

A slave microcomputer could consist of simply a processor, memory, and an interface to the network. Thus, a cathode-ray-tube display with sufficient random-access memory could execute CP/M programs, performing its computing locally while depending on the network to provide all disk, printer, and other I/O facilities.

A third network operating system, called MP/NET, provides the capability for MP/M systems to share each other's resources on the network. With MP/NET, there is no distinction between a master and a slave because all the nodes on a MP/NET can manage shared resources, as well as initiate network messages. Thus MP/NET provides a symmetrical network where all the nodes have equal opportunity. □

# Serially testing a board's states takes the trickiness out of debugging it

## Treating microprocessor operations as a sequence of electrical states makes it possible to check out even the earliest stages of system design

by James W. Coffron
*Hewlett-Packard Co., Santa Rosa, Calif.*

In the third article of the Test Tactics for the 1980s series, James W. Coffron describes the application of a simple technique he invented. In keeping with Jon Torino's and H. Frank Binnendyk's dictum "Test earlier and easier" [*Electronics*, Dec. 29, 1981, p. 80], his static stimulus testing method allows technicians unfamiliar with microprocessor operations to check out the hardware of processor-based designs even before the system can run software.

In addition, a static stimulus tester can teach its operator how a processor actually works in a system. Thus for field service it lets that person troubleshoot a system that cannot, for example, run any diagnostics because of a fault in the system's control lines or memory hardware.

The article also indicates some of the circuits basic to a static stimulus tester. A company can decide to build such a tester itself. Alternatively, manual and automated versions for a number of common processors are available from Creative Microprocessor Systems Inc. of Los Gatos, Calif. [*Electronics*, March 10, 1981, p .48]. **-Richard W. Comerford**

☐ As microprocessor applications have expanded, two major digital techniques have emerged for troubleshooting microprocessor-based equipment—logic analysis and signature analysis. However, these techniques can be applied to a new product only if the system being checked can execute some software and the user is to some extent familiar with the microprocessor. When neither of these conditions holds, neither of the approaches is any help.

For example, company A wanted to verify the operation of the individual parts of a prototype system. As each board was constructed and wrap-wired, the company wished to check the components' operation and the wire routing—only to realize that logic and signature analysis would not be usable because the system could not yet execute the software needed to provide a test stimulus. Further, the signatures needed for signature analysis would not be available at this stage, while the technicians who would be checking the parts lacked formal training in the operation of microprocessors and thus could not understand the dynamics of the system. In short, like others before it, the firm found itself in the analysis gap shown in Fig. 1.

### Static test dynamics

To solve its problem, company A turned to static stimulus testing. Using this new technique, it was able to develop the prototype parts and debug them separately. Once the system was assembled and able to execute some software, debugging could proceed using standard techniques to concentrate on system, rather than hardware, integration.

To understand how and why static stimulus testing works, it is necessary to view the microprocessor's job, regardless of the complexity and overall function of the system in which it performs, from a different perspective—as a series of operations rather than as a single dynamic process. Furthermore, each possible operation, described in the accompanying table, may be subdivided into a set of electrical hardware states.

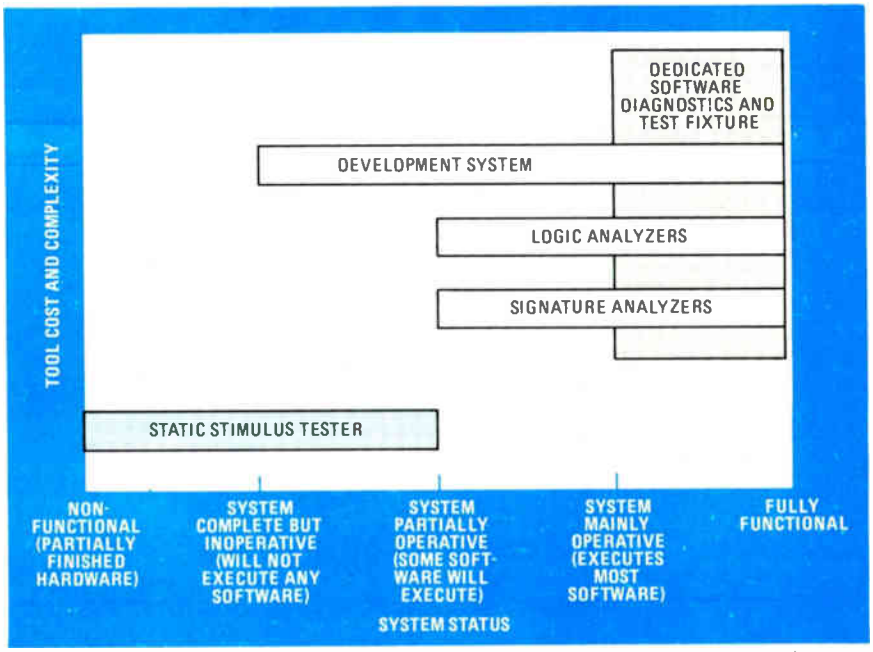
### Pause for thought

Consider, for example, the steps that a microprocessor, such as the Z80 used in company A's design, performs in reading information from a memory—during an operating-code or data fetch or a stack read, say. The major operation, memory read, embraces altogether four electrical states of the hardware—address output, memory-request line set, read-control line set low, and read-control line set high.

In the first of the states, the microprocessor has set the lines of the system's address bus high or low, such that an address has appeared at the address input lines of the system's memory chips or, alternatively, of select decoders for the chips.

To achieve the second state, the Z80 processor sets its memory-request ($\overline{\text{MREQ}}$) line low to indicate that data is to be transferred. Following this, the third state is reached: the read-control ($\overline{\text{RD}}$) line is set low to indicate that data will be read into the processor.

At this point, the system is essentially still. The system address is stable at the memory input lines and the chip-enable signals have been decoded and are also stable. The memory data buffers are enabled and data from memory is stable on the system data bus. The microprocessor's bidirectional buffers are also enabled in the




**1. The gap.** Until the static stimulus tester (tinted bar), no digital tools existed for troubleshooting the incomplete hardware of a processor-based system. Even complete but inoperative hardware could only be checked by a costly development system.

correct direction (that is, for receiving data from memory).

The conditions will remain stable until they are altered by the microprocessor in moving on to the next electrical hardware state. Consequently, if a processor or its electrical equivalent can be halted in this state, a person troubleshooting the system can trace various important paths and check the action of, say, the address decoders.

That such tests are possible can be inferred from the fact that no reference has been made to the duration of any state. Although their sequence is important, the elapsed time of each is not. Thus, reading data from memory can be seen as a sequence of states whose rapid succession in normal operation creates an intimidating but illusory aura of dynamic operation.

In the last state in a Z80 memory-read operation, the read-control line is set high by the microprocessor and memory data is removed from the system's data bus. The processor is then ready to move on to another of its six major operations.

The electrical hardware states that make up a read or any other major processor operation do not require a detailed technical evaluation of the microprocessor by the user. Instead, those states can be readily derived from the processor's data sheet, on which pin waveforms are shown in relation to one another for a particular operation. Thus, information supplied by the chip manufacturer makes it easy to apply static stimulus testing to any microprocessor-based design. Also, the technique can be used to a large degree in systems that employ devices like dynamic random-access memories.

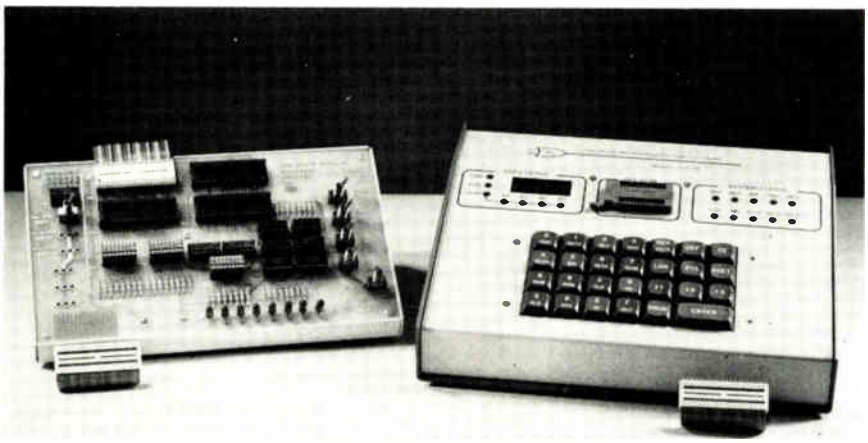
**MAJOR MICROPROCESSOR OPERATIONS**

| Operation | Description |
|---|---|
| memory read | data is transferred from a device such as a read-only memory or a static or dynamic random-access memory to a processor |
| memory write | data is transferred from a processor to a RAM or other register |
| input read | data is transferred from an input/output device, such as an analog-to-digital converter, to the processor |
| output write | data is transferred from a processor to an I/O device such as a digital-to-analog converter |
| interrupt service | system devices are set to known states by the processor's control lines and data is latched |
| direct-memory-access handling | most system devices are placed by the processor in a high impedance state by control lines to permit one device to transfer data directly to memory |

## One step at a time

To apply a static stimulus to a processor-based design, it is necessary to operate a processor in a single-step mode, freeing it from the dictates of its clock inputs. This is most easily done by removing the processor from its socket and replacing it with the dual in-line plug of a static stimulus tester, such as the one shown in Fig. 2.

The stimulus box contains the necessary hardware to set the address bus, data bus, and system control lines to either a logical 1 or logical 0. The address and data bus can be set using single-pole, single-throw switches as shown in Fig. 3a. The control signals, on the other hand, need to be debounced so that they are not misinterpreted by the devices that actually perform the data transfers.



**2. State controllers.** The manual static stimulus tester seen at far left allows its operator, who plugs its dual in-line connector into a processor socket, to control the state of each line with a toggle switch. The automated version at left permits groups of lines to be set more quickly with ASCII words.

A circuit for simulating a processor control line in a static stimulus tester (SST) is shown in Fig. 3b. Despite the simplicity of these circuits, the SST can produce all the hardware states of a processor.

The stimulus hardware can also monitor the data bus in such a way that the user can actually see what data is being sent to the microprocessor by the system and vice versa. This monitoring may be done by the circuit shown in Fig. 4. The hardware is operated by setting the logical level of the switch to the position desired.

The sequence of electrical states characteristic of some typical operations of an 8085, with its multiplexed address and data lines, and a 16-bit Z8000 demonstrates the ease with which static stimulus testing can be done. In both examples, it should again be noted that the element of time dependence has been eliminated from the troubleshooting process.

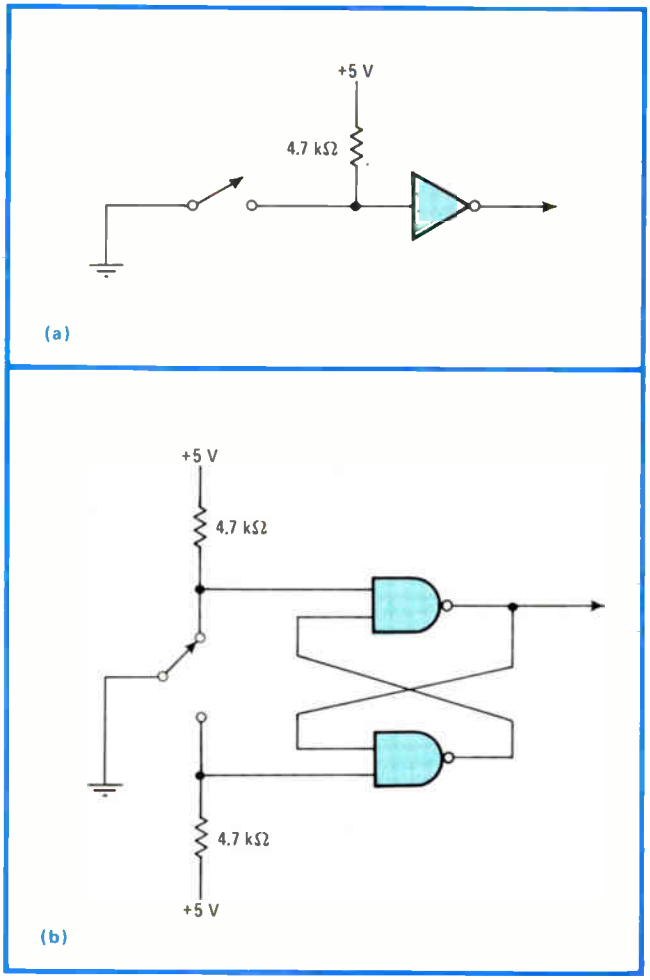
### An 8085 read

The electrical states that make up an 8085 memory-read operation each reflect a system hardware response. The person troubleshooting the system has only to use standard tools, ranging from a logic probe to an oscilloscope, to determine if the hardware is responding as it should be.

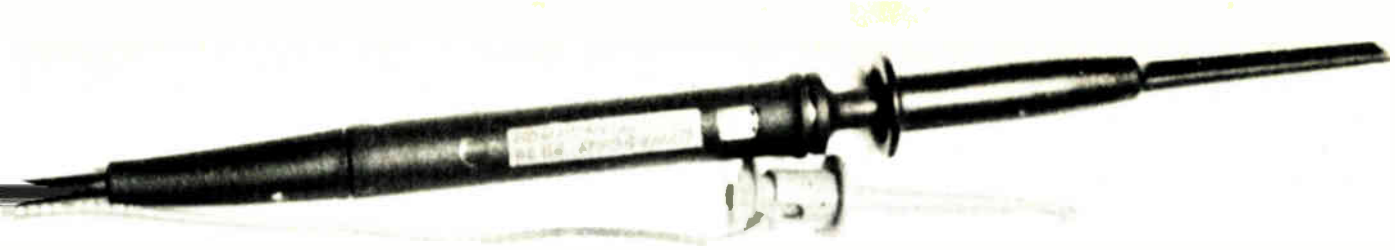
The first electrical state achieved in an 8085 read operation results from the processor placing an address on the appropriate lines. Address bits $A_{15}$ through $A_8$ are put onto the address-only processor pins, while address data $A_7$ through $A_0$ is placed on the processor's address-and-data pins.

The next two states result from the latching of the address lines. The processor's address-latch-enable (ALE) is first set high to 1, enabling the low-order address data, and is then set low to 0, latching the address. At this point in the execution cycle, the complete address is stable and has been broadcast to the system. This condition may be verified by using common measurement tools.

Next, the input-output/memory (IO/$\overline{M}$) line is set to 0 to indicate a memory operation and the $\overline{RD}$ line is set to 0. At this point in the sequence, the memory data is placed on the system data bus, ready to be sent from the




**3. Simple out.** To control the address- and data-line outputs of the processor-emulating tester, the simple circuit shown in (a) at top is sufficient; closing the switch drives the output high. Control lines, however, must be debounced to prevent undesired data transfers, say, so the two NAND gates in (b) are used.



selected address to the microprocessor. Light-emitting-diode indicators on each data line of the SST show the logical values of this data.

If the data being sent to the microprocessor is not correct, then the operator can trace the data from the source (memory) to the destination (microprocessor). This condition will remain stable in the system until the operator changes it with the SST. All conditions for a correct memory operation can thus be verified using static digital troubleshooting techniques.

The final state assumed by an 8085-based system in reading from memory occurs once the $\overline{RD}$ line has been set to a 1. This action removes the memory data from the system data bus and completes the operation.

It is to be noted that at each step in this sequence the system hardware responds to each change on the SST; if the hardware does not respond as expected, the troubleshooter may concentrate on finding the cause of the malfunction. Further, troubleshooting is accomplished using static techniques familiar to the average technician; he or she does not have to learn a new set of troubleshooting techniques for microprocessor systems.

### Double the bits

The technique can easily be adapted to systems based on a 16-bit microprocessor. For example, consider the sequence of electrical hardware states a system passes through when data is being written to a Z8002A output port, assuming that the I/O transfer is a 16-bit (or word) output operation.

The first is the placement of the address of the output port by a Z8000 SST on the $AD_0$ through $AD_{15}$ pins of the microprocessor.

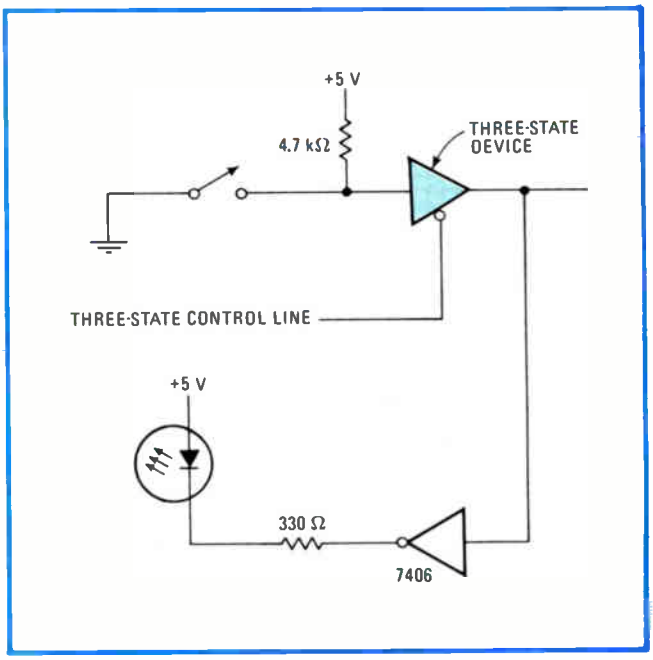
Next the SST sets the $\overline{AS}$ control line from the Z8002 first to 0 and then to 1. At this point the system is told that the address on the output of the address latch is valid. The address lines may be verified using static troubleshooting techniques.

To reach the next hardware state, the status word for an I/O operation is set on line outputs $ST_3$ through $ST_0$ via switches on the SST. The byte or word ($B/\overline{W}$) line is then set to 0, to indicate to external hardware that a word transfer is on the point of occurring.

The next state in the sequence occurs when the data to be written to the output port has been placed on the lines $AD_0$ through $AD_{15}$ . The $\overline{DS}$ line is set to a logical 0 and then to a logical 1. At this point the data placed on the lines $AD_0$ through $AD_{15}$ will be transferred to the output port that has been addressed.

### Clear checkpoints

As before, each transition in the sequence described causes the peripheral hardware to respond in some way. Thus if the hardware does not assume the correct state each time, the system troubleshooter can focus on the area that is not acting as it should.




**4. Monitored three-state.** To let the static stimulus tester perform like a processor with bidirectional lines, for example, the above circuit with its controllable three-state amplifier is used. The logic state of the line is made visible using the LED at bottom left.

The preceding examples show that the ability to control any microprocessor line can be an extremely effective method of troubleshooting. But if all lines must be controlled from discrete switches, troubleshooting can become a tedious and time-consuming process.

A natural extension of the stimulus concept is to give the stimulus box intelligence, that is, to automate the user interface and keep the concept the same. This idea was realized with an automatic static stimulus tester, which uses a keyboard to apply the static test signals to a system much faster than is possible manually.

### Static testing of dynamic-RAM systems

A major argument against using static stimulus testing has been its supposed inability to troubleshoot systems employing dynamic RAMs. The assumption here is that the RAMs must be refreshed by the processor at millisecond intervals that are impossible for an SST to keep up with.

However, if a dynamic RAM system is dissected into functional blocks, it turns out that its only truly dynamic element is the RAM cell itself. All peripheral support hardware for the dynamic RAM can be tested and verified in a static manner.

Moreover, if multiplexed-address RAMs are used, the multiplexing can also be verified using static techniques. The row- and column-address strobe lines and all chip-enables, write-enables, data-in, and data-out lines can also be verified statically. □

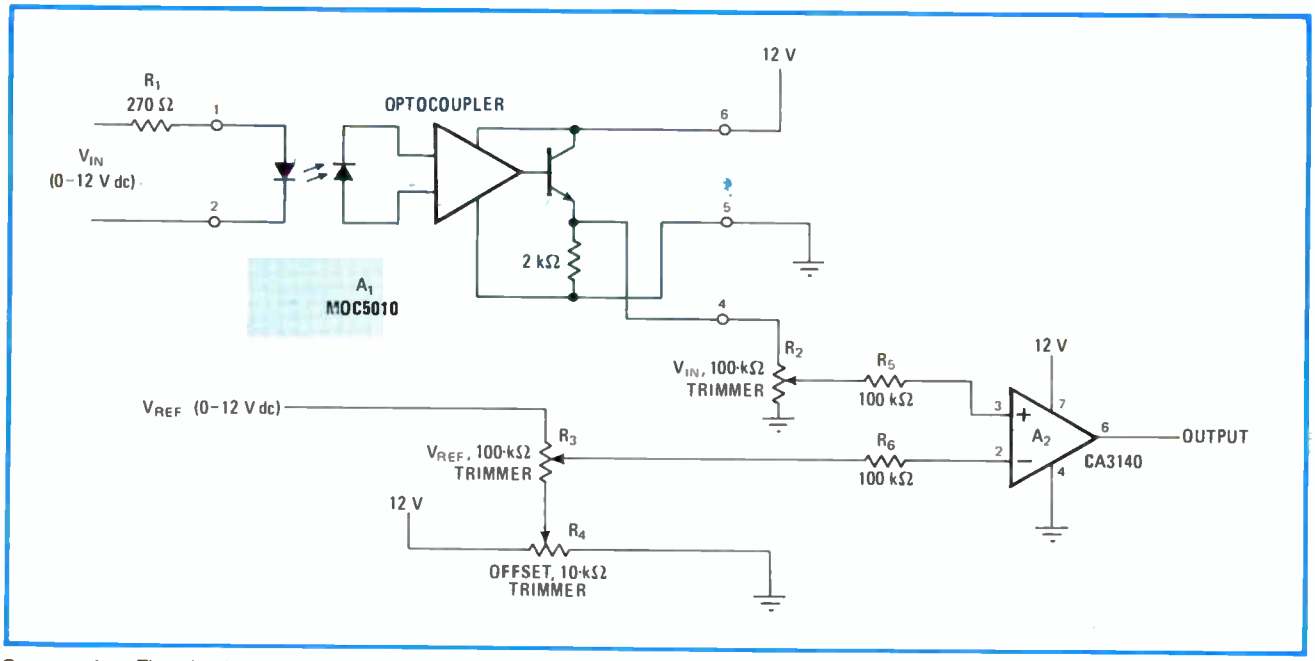
# Optical coupler isolates comparator inputs

by Dennis J. Eichenberg
*Cleveland, Ohio*

Many dc-comparator applications need complete signal isolation. However, Motorola's optically isolated linear coupler MOC5010 eases this problem by eliminating the complex circuitry that is required with other techniques. The circuit's use of a single-ended power supply further simplifies the design.

The comparator circuit (see figure) compares two 0-to-12-volt signals that must be completely isolated. Resistor $R_1$, calculated for a current of 40 milliamperes, creates an acceptable current from $V_{in}$ for the light-emitting diode of optocoupler $A_1$. Because there is an offset voltage at the output of $A_1$ ($V_{in}$ = 0 v), the voltage at the inverting input of $A_2$ is made equal to the voltage at the noninverting input by adjusting the offset trimmer potentiomenter $R_4$. This adjustment is done when $V_{in}$ and $V_{ref}$ are zero. Resistors $R_5$ and $R_6$ protect $A_2$ by limiting surge current.

Potentiometers $R_2$ and $R_3$ permit the slope of the input voltage for $A_2$ to be adjusted at the maximum $V_{in}$ and $V_{ref}$ by a desired ratio. When $V_{in}$ exceeds $V_{ref}$ by this ratio, the output goes high. Hysteresis may be provided by connecting an appropriate resistor from the output to the comparator's noninverting input. □




**Comparator.** The circuit compares two 0-to-12-V dc signals and provides complete isolation between the two signals. The circuit uses optocoupler MOC5010 to provide isolation and requires a single-ended power supply. Potentiometer $R_4$ balances the offset voltage.

# Thumbwheel switch programs retriggerable one-shot

by Dil Sukh Jain
*National Remote Sensing Agency, Hyderabad, India*

This programmable synchronous one-shot is a few jumps ahead of the rest by being able to generate a synchronized output pulse whose width can be varied through an externally controlled clock period or a programmable thumbwheel switch. In addition, the circuit is retriggerable with a provision for a clear input.

A narrow negative pulse applied at the trigger input loads the synchronous binary-coded-decimal down-up counter 74190 with the number (N) set on the thumbwheel switch and simultaneously sets $Q_1$ of flip-flop $A_1$ high. This loading in turn sets $Q_2$ of flip-flop $A_2$ high. The low level at $\overline{Q}_1$ enables the counter to count down from N on successive positive edges of the clock.

When the counter reaches zero, a negative pulse is produced at the ripple clock output of the counter 74190, which corresponds to the negative edge of the clock. This negative pulse, inverted by the 7404 chip, triggers $A_1$ to make $Q_1$ low and the enable ($\overline{Q}_1$) input high, which in turn disables the counter and inhibits the circuit. The

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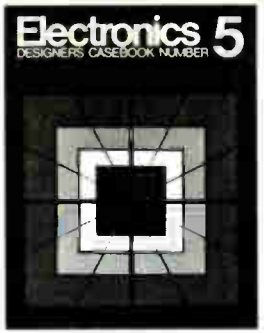


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D Software Engineering
E Systems Engineering, Integration
F Quality Control Engineering (Reliability and Standards)
G Design Engineering
H Engineering Support (Lab Assistants, etc.)
I Test Engineering (Materials, Test, Evaluation)
J Field Service Engineering
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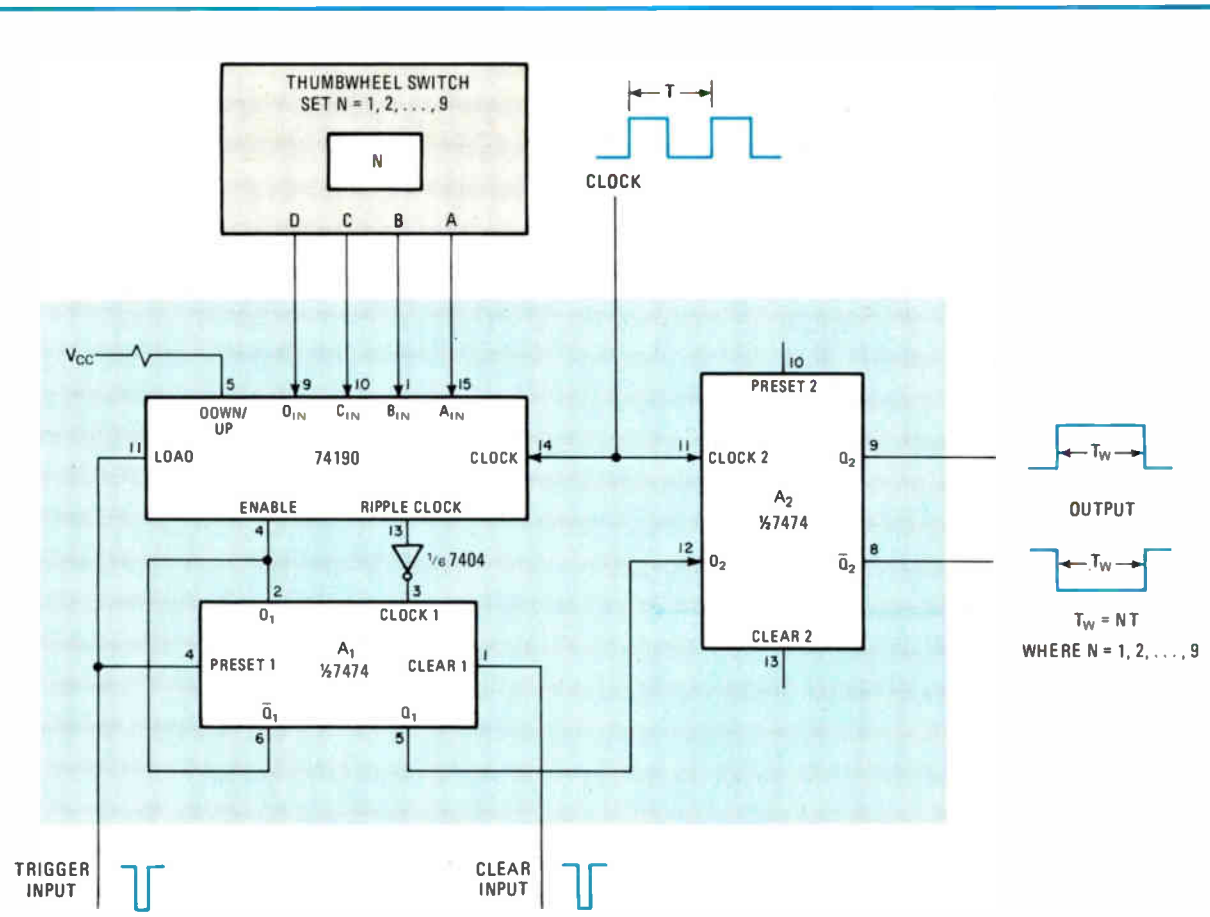
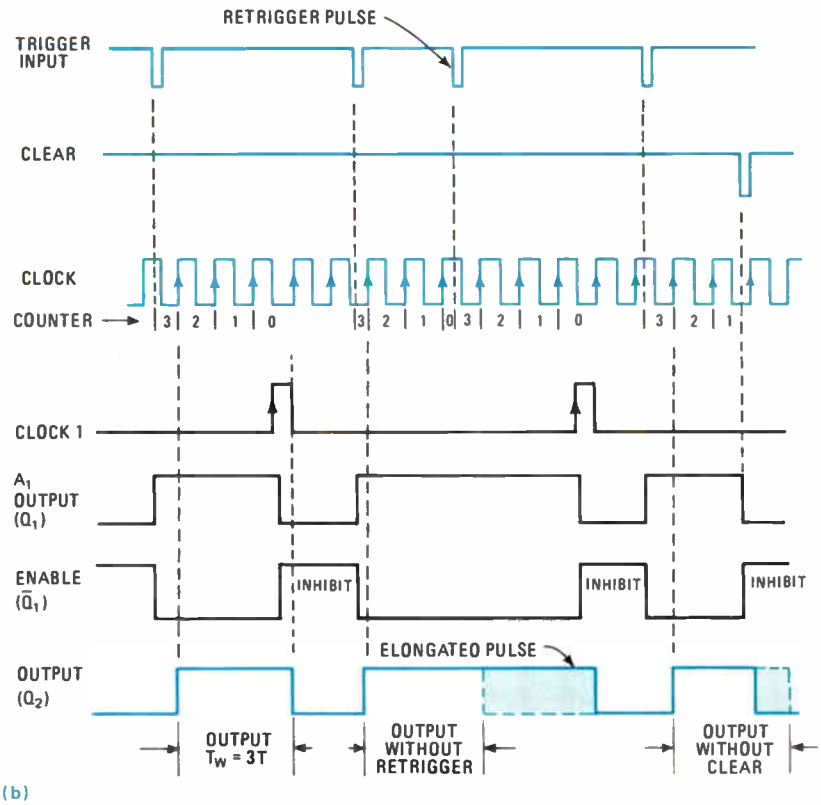



(a)




(b)

**Programmable one-shot.** The output pulse width of this synchronized one-shot (a) is programmed with a thumbwheel switch. The circuit uses a binary-coded-decimal counter 74190 and D type flip-flop 7474 to provide the retrigger and clear feature. The timing diagram (b) for N = 3 illustrates the control of retrigger and clear inputs on the output pulse.

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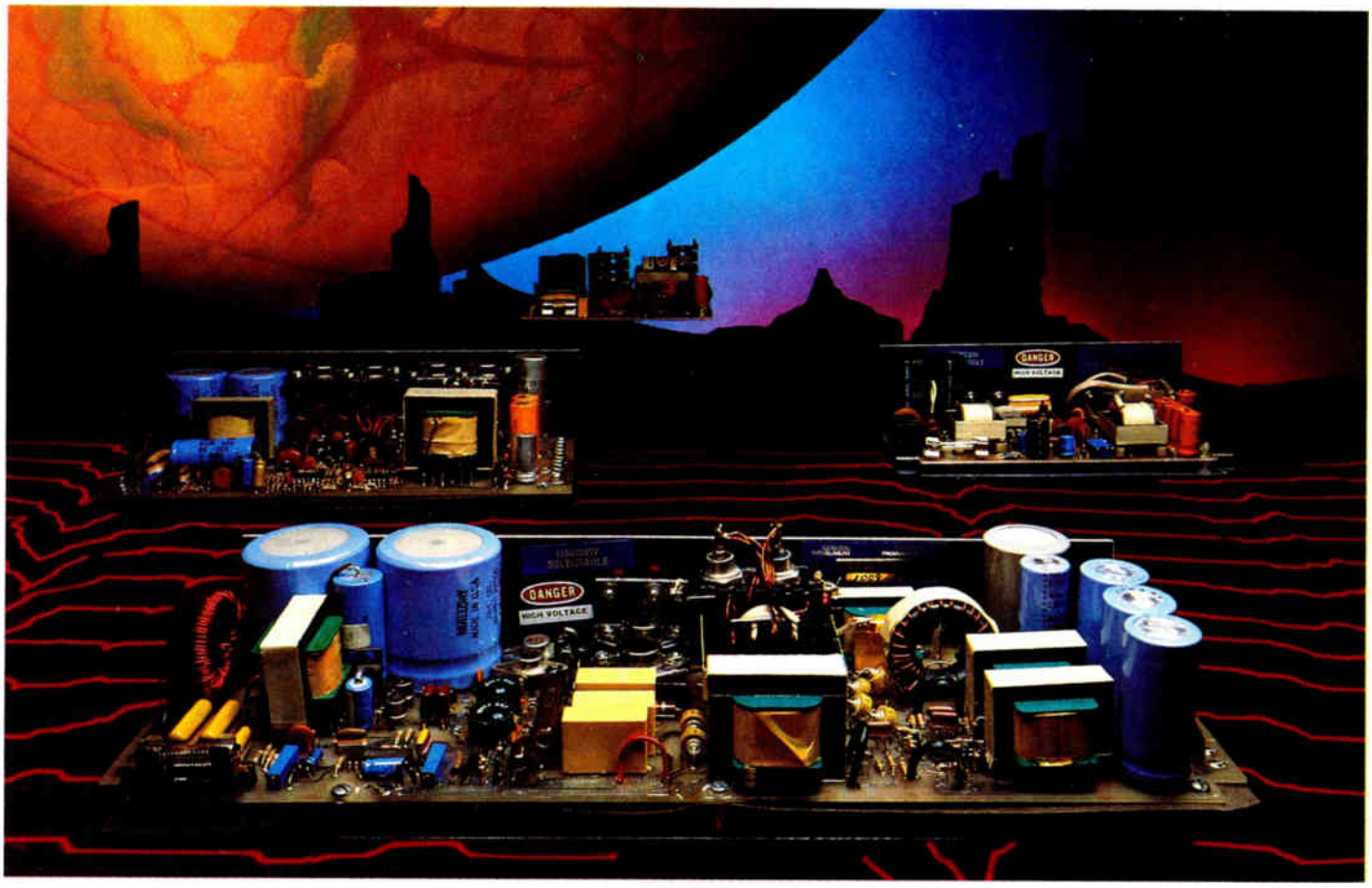


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low input level at $D_2$ terminates the output pulse whose width is given by $T_w = NT$, where T is the clock's period. The one-shot output pulse width when N = 3 is 3T(b).

A retrigger pulse applied while the counter is counting down reloads the circuit with set number N and begins a new countdown, resulting in a single stretched pulse at output $Q_2$. A negative pulse applied at the clear input (while the counter is counting down) terminates the output pulse at the clock's following positive edge. □

# Ultrafast hybrid counter converts BCD into binary

by L. J. Herbst
*Teesside Polytechnic, Middlesbrough, England*

Most ultrafast integrated-circuit counters that are capable of operating at 500 megahertz and above with a reset facility employ a binary-coded-decimal format. However, this ultrafast hybrid counter with a binary output and external reset control contains a BCD input stage followed by binary counters—it has a special conversion for a binary output. Because a conventional BCD-to-binary counter uses more integrated circuits, money is saved and conversion time shortened for this hybrid circuit. In addition, the method uses a novel decoding technique for faster conversions.

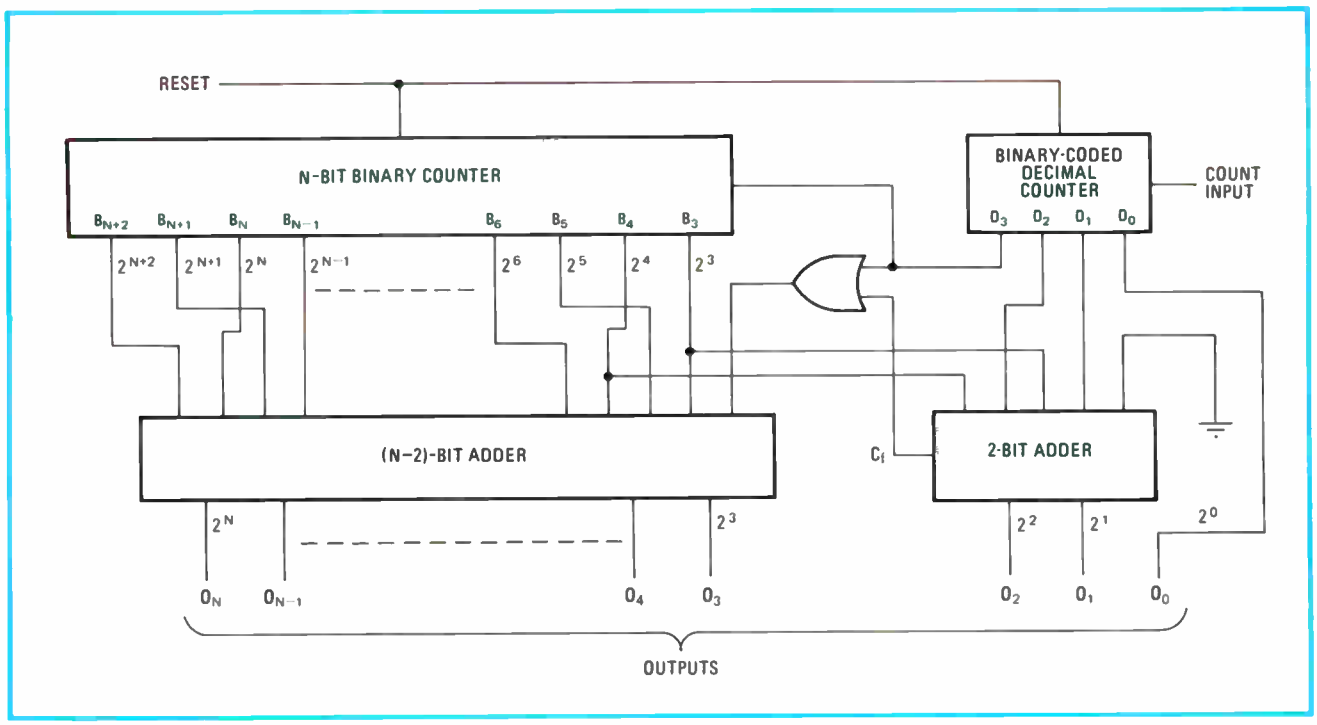
The counter output of the circuit (see figure) is $10N_B + N_D$, where $N_B$ and $N_D$ are the contents of the binary and decade counters respectively. The output is rewritten in the form $8N_B + 2N_B + N_D$, for code conversion. It is expressed through the following summation when the weight of $2^3$ is assigned to the least significant bit of the binary conversion:

| | | | | | | |
|---|---|---|---|---|---|---|
| | | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $N_D$ Term |
| $B_n$ | $B_4$ | $B_3$ | | | | $8N_B$ Term |
| $B_{n+2}$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | | $2N_B$ Term |
| $O_n$ | $O_4$ | $O_3$ | $O_2$ | $O_1$ | $O_0$ | Output |

If standard full adders are used, the code conversion that is needed to implement the above expression is achieved with a normal two-word addition—except when output $O_3$ is selected. In this case, the input consists of $D_3$, $B_3$, $B_5$, and $C_f$ (the carry forward from the 2-bit adder)—$D_3 + C_f$ is implemented with an OR gate. Because $D_3$ is 1 only when both $D_2$ and $D_1$ are 0, the input to yield $O_3$ is reduced to $B_3$, $B_5$, and $D_3 + C_f$.

The method is superior in cost and speed to an all-decade counter or the standard BCD-to-binary conversion technique. A hybrid counter with a 12-bit output, that uses the schematic shown, sports a Plessey Semiconductor BCD counter (SP8636B) and Texas Instruments' binary counters (SN74197) and adders (SN7483, SN7482). A BCD counter would have required four decades and 11 SN74184 BCD-to-binary decoders, giving a conversion time of 196 nanoseconds. However, the add time for two 16-bit words, using the SN7483s for example, is typically 43 ns. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.




**Hybrid counter.** This ultrafast hybrid counter provides BCD-to-binary conversion. It consists of a BCD input stage followed by binary counters and full adders to achieve code conversion. The OR gate is used to reduce the inputs that yield $O_3$.

Design AUTOMATION AUTOMATION

# Teachable work station brings order to VLSI chip design

## Turnkey system assimilates use-specific commands; ranks tasks with its data-base manager; displays two views of circuit at one time

by Stephen C. Johnson, Gerd H. Schlitt, and Vicki Perkins, *Scientific Calculations Inc., Sunnyvale, Calif.*

☐ The history of integrated circuits charts an ongoing demand for advances in design and production techniques. With very large-scale integration, however, process and manufacturing technology is outstripping design expertise. This capability gap has created an unprecedented need for advanced VLSI design tools.

Only major advancements will close this gap. A more powerful menu or a more natural language represents improvements—not significant overall advances. The requirements for an automated VLSI design system include real-world modeling capabilities, efficient information transfers, and design discipline and control. Another need is educability, the ability for the system to learn design heuristics from users.

The Microelectronics Design System incorporates all of these elements, freeing users from the necessity of purchasing or maintaining a traditional drafting system. It integrates automated layout features in a natural and user-friendly way and provides the comprehensive design discipline and implementation safeguards so necessary for a high-quality design.

The generation of mask-tooling tapes is a standard feature of the system, eliminating the need for programs or interfaces to generate such tooling. It supports user-oriented libraries and gives them a new level of protection. Also, the work station allows two concurrent views of a layout (Fig. 1), enabling graphics-editing problems to be solved in a fraction of the time that previously available systems take.

A hierarchical menu provides a simple and easily remembered command structure that speeds interaction and reduces clutter on the screen. Automatic symbolic-layout and -routing features improve design productivity by reducing superfluous data and by simplifying the interpretation of graphics information. Finally, a powerful macrocommand structure permits users to teach the system successful layout strategies, thus easing future interaction. Employing macrocommands, users can actually run jobs in a batch mode.

### Automatic, interactive designs

The Microelectronics Design System is a self-contained turnkey design-automation system, useful for all tasks from logic definition through pattern generation—exclusive of simulation. The system may be used with any IC process and is auto-interactive: users can design layouts automatically, interactively, or through any combination thereof. A proprietary data-base-management system called Assist eliminates program and data interdependence, avoids program and data obsolescence, and provides run-time protection (see "Help from the Assist data-base manager," p. 112).

The Microelectronics Design System is modular and easily expanded and interfaced with less versatile design-automation tools. Dramatic new graphics-display features allow virtually any IC to be modeled, including custom, semicustom, and random logic chips. The system's mainframe is a Digital Equipment Corp. VAX 11/780, on which many commercially available design-automation tools can run without conversion. More than 300 user commands, organized in a hierarchical manner, are provided.

Logic simulation and network analysis are absent from the system because several excellent packages

This is the ninth article in a series on the design automation of integrated circuits. Four articles each appeared in the Nov. 17 and 30 issues of *Electronics*. The focus is the new hardware and software tools available to the IC designer. Previous articles have explored such topics as logic gates and macrocell structures for design automation, systems for simulation, semicustom chip development, and computer-aided testing. This installment describes a new color-graphics work station with integral data-base manager.

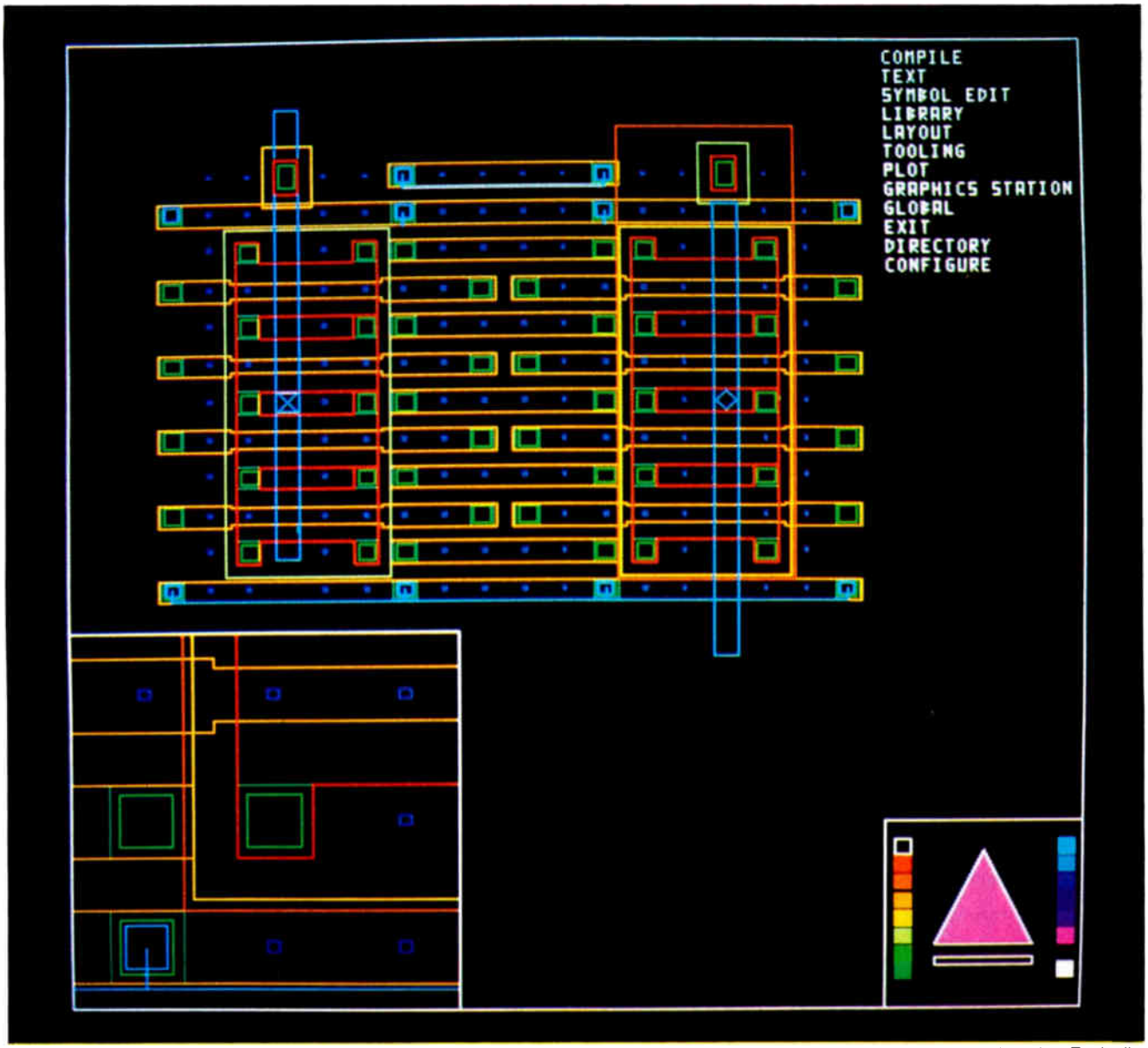
exist today. However, the system's data structure is nearly identical to those required for logic simulation. Thus user-friendly interfaces with popular logic simulators will be supported as standard options.

The system is organized as shown in Fig. 2. It consists of a central data-base, partitioned into public and private (user) libraries, that is managed and organized by the Assist system. All data transactions are handled by the Assist system.

Grouped around this core are the major application modules for automatic placement and routing, interactive layout, mask-tooling generation, design-rule checking, and other such features. This grouping is apparent in the software organization, but it is otherwise transparent to the user.

For users who wish to extend the system by adding their own modules, a menu programming language is available that allows menus and any required control structure to be generated automatically. Available to all modules is a proprietary graphics subsystem that controls all display functions—including data reporting and editing—as well as the menu handling.

After any command is selected, a sub-menu is displayed automatically, if appropriate. Alternatively, users




**1. Two views.** The Microelectronics Design System allows two views of a circuit layout to be viewed simultaneously and in color. Typically, users exploit this feature to look at a wide-angle view of a layout and a blown-up detail at the same time, as in the inset above.

may type commands directly from the keyboard, making it possible to operate nearly all the features of the system without even using the graphics display. Since only graphics-intensive operations like geometric editing require the display, the system can be expanded to include several dozen low-cost design stations, with the centrally located graphics services on hand as required.

### Describing ICs

Logic-circuit characteristics are described using the module description language (MDL), which is hierarchical and node-oriented, permitting designers to describe their circuits as nested modules having the same structure throughout. There is no practical limit to the level of nesting in the hierarchy, and MDL can be mapped directly into available logic simulators. For the first scheduled system upgrade, the netlist, which describes the required interconnections, may also be entered by an interactive schematic-generation system.

Each hierarchical block or module of the circuit may be described by a different MDL program or file. Before layout actually commences, one module is designated as the root module, and the layout is linked in a manner familiar to programmers. During the linking operation, all data necessary for the layout is organized into the system's internal data structure, and module-to-module consistency checks are performed. Also, if any prespecified layout constraints exist, such as the location of bonding pads or grid points for gate arrays, they are also incorporated into the data structure at this time. The linking need only be done once.

Since the lowest level of any hierarchical IC description references other geometrical objects, the system—out of necessity—features a complete geometrical editor, designated the Symbol Editor. This tool has all of the operations found in the most modern drafting systems, but also incorporates several new concepts necessary for IC design automation.

For effective automated layout, there are several other simple artifacts that should also be included in the graphics data base. For example, in the geometric description of the fundamental, or base, symbol of a gate array, users may wish to include predefined routing grid locations, as well as a placement grid. The placement grid would be used during automatic placement to allocate particular cells or transistors to specific sites. For a fully automated custom layout, such sites typically would not be required.

Easier interactive layout is provided through the Multi-Viewport display system. Others have experimented with providing two simultaneous views of a circuit on two displays; however, for the first time, two views of one design are available on the same color display. In addition to allowing the operator to focus attention more directly on the problem at hand, the single display is more cost-effective.

Users can display the second view anywhere on the screen, and it may contain—independent of the primary view—any system data that can be displayed. The user, in effect, has two separate graphics systems in one. However, the most frequent use of the second Viewport is to provide a closeup view, at perhaps a 1,000× magnification, of the area under the cursor on the primary wide-angle view.

Since the system also features dynamic and continuous panning and zooming, users may move the cursor across the wide-angle Viewport and watch the closeup Viewport pan automatically. Digitizing and editing can be done from either view, at any time, and each view can be panned or zoomed independently.

The Symbol Editor offers 15 usable colors plus a background color, all controllable by the operator through a feature called the Color-palette. Other novel features, such as automatic decluttering and rubberband digitizing, are also supported. For users wishing to enter graphics by way of a language, a proprietary graphics language has been developed that is terse, symbolic, hierarchical, canonical, and self-documenting.

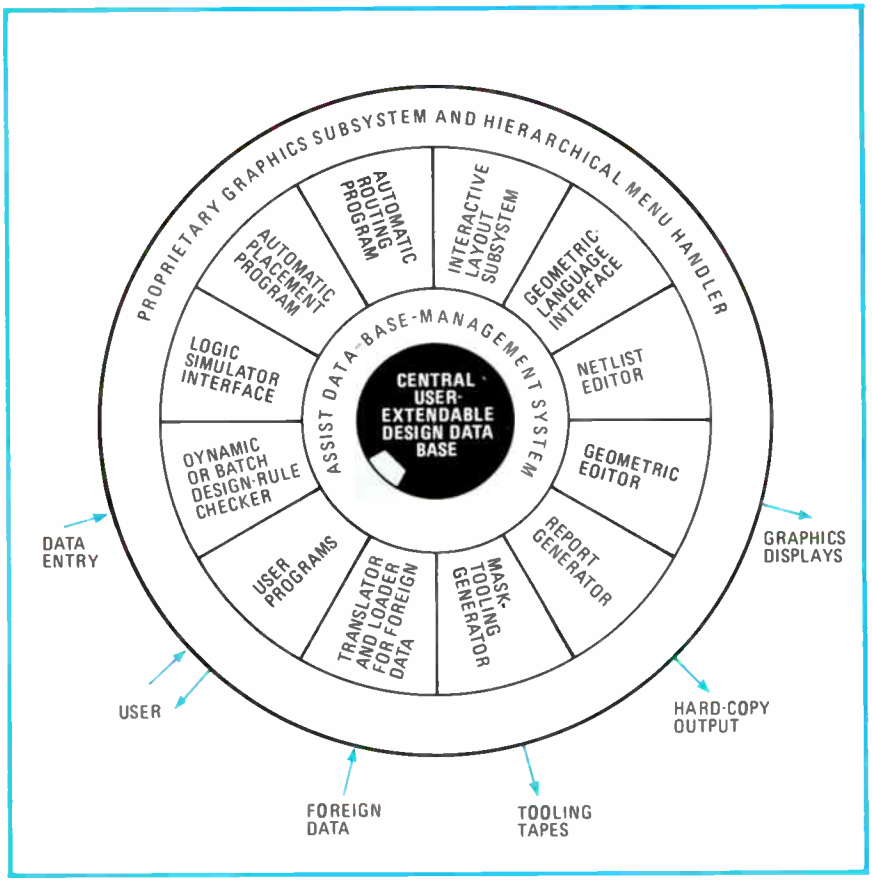
The automatic-placement system, called Auto-plus, comprises two algorithms—one oriented toward circuits of a regular nature and the other toward the general case. The former is extremely powerful for implementing placements on both cell- or transistor-based layouts, including all gate arrays. The second algorithm, which interacts dynamically with the routers, will be available in the second release of the system.

### Placement and routing

Examples of Auto-plus placement strategies include module ordering, location or orientation constraints, breakpoints for manual intervention, hierarchical routing (which implies hierarchical placement), and selection of the placement engine or algorithms. The control of the placement strategy is totally in the hands of the user. Certain strategies work best under certain conditions, so successful strategies may be saved in macro-command files for later use by anyone. Several proven strategies will also be provided with production versions of the system.

Manual intervention may occur at any time and may again be followed by automatic placement. The single constraint on manual placement is that only objects specified in the original MDL description may be placed in the circuit. Also, the manual placement system will not allow modules to be placed contrary to any constraints programmed by the designer. The same philosophies were applied to the Auto-Plus routing portion of the system.

The Auto-plus routing system has been specifically engineered for IC design tasks. It currently supports four user-selectable routing engines, which may be used repeatedly in any order. This feature allows users to




**Interconnections.** The software structure of the design tool resembles a data-base–management system: at the heart is a central design library surrounded by a comprehensive manager called Assist. Around these are the various input and output utilities.

match a router to the problem or to use a stepwise approach, invoking faster but less comprehensive routers during the earlier phases of the routing process.

The routing strategy is left to the user, though there is a built-in set of default strategies that have proven best in the general case. Users may control such items as connection sequencing, routing costs by layer, area-specific routing, or special routing treatment by signal name. Limits can also be placed on the number of routing layers or vias per node, and trace width can be specified. More advanced features, such as routing search limits, rip-up and reroute strategies, and post-route optimization may also be selected.

The routers all recognize the existence of off-grid barriers, preexisting interconnections, oddly shaped terminals, predefined connection points, terminals with multiple connection points, and a host of other situations common to IC layout. The user will also find many provisions for completing routes that the system may not productively solve on its own, such as the rubber-band display of deferred connections.

As with placement, routing can be performed manually at any time. The system requires only that connections entered by the user be consistent with the original MDL netlist description. In fact, upon completing a layout, the system will check to see that all connections have been made. All routers can work with any number of layers, and recognize the existence of predefined traces like the polysilicon feedthroughs that are so common in single-layer metal-gate arrays.

The system's data library is modeled after several popular interactive operating systems available on mainframes and minicomputers. Each design in progress is assigned its own user identifier, and access is restricted by password. Every user ID has control of a private library containing data such as module descriptions (netlists), geometric data, design-rule files, layouts in progress, and schematics.

Standard library maintenance commands are available to copy, rename, and delete files. To move files between user IDs, sending and receiving commands are provided. Users may refer to data in other libraries during their layouts, with protection against changes to such referenced data afforded by a unique protection system. Automatic backup is also standard. The library system does not claim to be a data-base–management system, but it is implemented using Assist.

Although the initial system release will support only those design rules pertinent to the Auto-plus placement and routing programs (such as line width and spacing and intermodule spacing), a powerful IC-oriented design-rule–checking language will be offered that includes not only the more familiar checks, but such items as step coverage, reflection checking, crevasse checking, and conditional specifications.

### User extendibility by design

The system has been designed so that knowledgeable users may extend it. This extension may be casual, by adding fields or subrecords to the data structure, or it may be expert in that entire modules and menus can be created. The overriding concept is that users can extend the system with their own software, yet retain the original feel. User extendibility requires the entire Assist data-base–management system, hierarchical menu programming system, graphics subsystem, and the Assist

## Help from the Assist data-base manager

The Assist data-base–management system is tailored to the design-automation environment. To meet this goal, it supports complex data relationships, large real-time transactions, dynamic array allocation, and other features that are not usually found in commercial data-base–management systems.

It also includes a text macrocommand processor and languages to define and manipulate data. Fortran programs can interface with the dictionary by data manipulation statements embedded within application programs. The text macrocommand processor then translates the data manipulation statements into standard Fortran subroutine calls. Both the data definition language and the data manipulation language are easily mastered by program writers who are familar with the necessary basic data-base concepts.

Users may extend Assist's standard data structures by creating their own data dictionary. The program will automatically upgrade the data base to conform with the user's data dictionary without any conversion programs being necessary to perform this function.

In the design-automation environment, data-base transactions may be complex and time-consuming. If the machine crashes during a transaction, some information may be entered into the data base without having the necessary relationships established. Assist provides fail-soft recovery and a transaction-locking mechanism to prevent partial updates. During all data transactions, a backup copy of the affected portions of the data base is maintained. Assist automatically restores this backup following a machine crash or on command. It supports multiple-user access, with appropriate safeguards to prevent data loss or overwrites.

To facilitate complex data relationships, the data manager provides indexes (for keyed retrieval and insertion of records of any type), linked lists, explicit pointers, and sequential data structures. An individual record may belong to several data structures simultaneously and may be removed from one data structure without affecting its other relationships. In addition, several different types of records may belong to the same data structure.

Assist supports character strings, real numbers (4 bytes), integers (2 and 4 bytes), and Boolean data. These data types may be arranged as records, subrecord arrays, and groups. Subrecord arrays are defined by an initial allocation and an extension quantity. Unlike standard Fortran, Assist arrays are allocated dynamically and therefore use only as much space as required for their actual data. Group data allows data types of less than one 4-byte word to be packed for maximum efficiency. All data fields may be manipulated within the applications program as normal Fortran variables.

Installation parameters are provided that can tune Assist's performance to various environments and machine configurations. Files are regarded by the operating system as standard RMS-11 files and may be manipulated by standard operating-system commands, such as copy or delete. Assist files may span several disk drives and can be backed up and restored using VAX/VMS operating-system utilities.

macrocommand library, the latter being necessary to use the data-base–management system. No source code is required or available.

The system supports many symbolic-layout concepts. For example, the logical hierarchy of a circuit can be displayed with its levels differentiated by color. Alternatively, several levels of abstraction can be invoked to show only the graphics data relevant to the task on hand. This data may include terminals, trace center lines, or vias, and the display can be made to look exactly like a block diagram. Several IC manufacturers that use cell-library systems have demonstrated that such a representation is extremely productive.

At any time, users may request to see more details on a particular level. As modules are constructed during placement and routing phases or by user intervention, the system computes and displays module boundaries if they are requested. Also, when entering data by means of a data tablet or digitizer, the input can be restricted to a minimal set of symbolic items.

There is a specific set of commands and features in the system just for manipulating gate arrays. Also, the Symbol Editor includes built-in artifacts for automating gate-array design. It is possible to convert an existing gate-array design to run on the system in a matter of hours. All other Microelectronics Design System features are available for gate-array design, including predefined traces (feedthroughs) and routing grids, routing control zones, multipoint terminals, and graphical and logical macrocells especially.

### Layout library

Since the system permits successful placement and routing strategies to be saved for future use, gate-array designers can tune the system to support their array. This ability is appealing to manufacturers who might like to package the layout strategies most useful for their array with their cell librarys and make these available to gate-array customers that also have the Microelectronics Design System.

To control a gate-array layout in house, a customer-control module permits the manufacturer to set up a time-sharing service for its customers. This service lets customers specify their netlist and invoke the system to do the layout remotely. Layouts that are completed automatically would be scheduled for tooling-tape generation, and particularly difficult layouts would be queued up for completion by an in-house layout operator. □

# Warship may draft fiber link for service with its radar

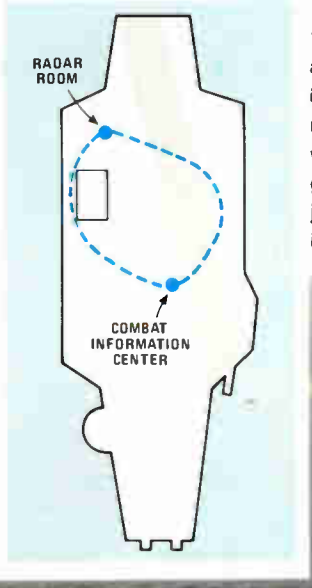
## Seven optical fibers multiplex 375 signals passing to and from the vessel's control center

by Thomas P. Dixon, *International Telephone & Telegraph Corp., Gilfillan Division, Van Nuys, Calif.*

☐ When a shipboard radar is connected to its operations center, merely installing the copper cable can cost a million dollars. Even so, the cabling is vulnerable to everything from radio-frequency interference to enemy firepower and also adds several tons of destabilizing deadweight above the ship's waterline.

Redundant fiber-optic data links would appear to be an easy solution to these cost, rfi, and weight problems. But the signals generated by multibeam radars have such a wide variety of data rates, functions, and critical interfaces that no commercial product is adequate. ITT's Gilfillan division has therefore developed a multiplexed fiber-optic interface and retrofit capability that can apply to any radar installation, new or old, regardless of manufacturer. Qualification testing of this capability is already under way on land.

The benefits of the multiplexed-signal concept are evident in the case of an aircraft carrier that has an AN/SPS-48C radar transceiver located below deck and




**1. No comparison.** Connecting an aircraft carrier's radar transceiver to its combat information center formerly required 47 copper cables as well as cable grounds. Now, a single fiber-optic cable consisting of just seven strands plus a spare one is more than sufficient.

**2. Clear winner.** Much less weight and size distinguish the fiber-optic from the copper-cable approach to routing radar signals. The former requires no ground wires and even incorporates a spare fiber.

750 feet away from the ship's combat information center, which is also below deck (Fig. 1). The two sites are usually linked by a bundle of 47 cables carrying 375 separate signal lines and five hefty copper wires to help subdue the effects of large ground loops. The fiber-optic link, in contrast, is contained in a single cable of seven strands and a spare (Fig. 2). The latter also costs about $30,000 to install, as against $1 million for the copper cable. The fiber cable weighs a mere 15 pounds, the wire connection seven tons. Multiple redundant cables are economically feasible with the fiber link; none is feasible with cable. The fiber link is expandable when the data link is upgraded; the cable link is not.

### How 8 can equal 375

Multiplexing enables the fiber-optic data link to accommodate an unusually wide variety of different signals. In the aircraft carrier's case there are 27 analog video signals, 101 timing pulses, and 247 digitized control signals to be handled.

The design approach could have simply been to multiplex these 375 lines onto a single, wideband fiber. But such a system's input laser, at the necessary bandwidth, would have had to be driven too hard for a design goal of a system lifetime of 40 years.

At the other design extreme, 375 individual fibers could have replaced 375 copper wires. But though the result would have been great reliability and simplicity, the cost would have been too high.

Final system cost and reliability tradeoffs dictated that the light sources be light-emitting diodes and the actual number of active fibers used be seven. Three of the seven fibers transmit the 27 analog video signals. The aircraft carrier's AN/SPS-48C radar is a three-dimensional air surveillance radar whose nine beams generate three video signals each. These signals each have a bandwidth of 0.5 megahertz and nine of them are multiplexed onto each of three optical fibers at a 10-MHz rate. The rate was made the same for all the fibers so as to provide board commonality for easy service and low spare-parts count.

Two more fibers transmit the 247 narrowband control signals. Formerly, each of these signals used a twisted pair of copper wires. Of the 247 signals, 165 originate at the transceiver and 82 at the control site. One fiber handles all the signals going in one direction; the other passes those going in the other direction. The sum of all the control signals' bandwidths is much less than 10 MHz, but the channels are multiplexed at 10 MHz anyway, to maintain circuit-board commonality.

The sixth fiber replaced 101 individual copper wires that transmit 101 system timing pulses. There was a potential problem here. The aggregate bandwidth exceeds 1 gigahertz, a large figure that does not readily allow a common 10-MHz multiplexing rate on all seven fibers. However, the 101 timing pulses are derived from five basic logic states, which are strobed in various combinations with the system clock. Even though the circuit boards that generate the 101 signals are located at the radar end of the link, nothing prevents them from being moved to the control end. Thus, only five signals need be multiplexed. Since each of the timing signals is routinely reclocked after transmission, any errors and jitter introduced by the needed time-division multiplexing are as a consequence transparent to the system.

Since one fiber is dedicated to the system clock and one is spare, seven optical fibers suffice to carry 375 signals. An eight-fiber bundle does the job, for there is no need for extra conductors (as in the previous coaxial cable) to guard against ground loops. Also, the two sites are electrically isolated from one another, enhancing freedom from such common radar vulnerabilities as the effects of lightning strikes, radio-frequency interference, stray pickup, and crosstalk.

### Thin but tough

The fiber bundle itself comprises eight graded-index fibers and their structural support. Although step-index fibers would have been marginally adequate for the 20 MHz needed, they might inhibit future data-rate enhancement. The small cost premium for graded-index fibers was deemed insignificant for this type of military

system. Each of the eight fiber cores has a diameter of 55 micrometers. The cladding is 125 $\mu$m in diameter and the outside plastic coating is 500 $\mu$m thick.

Mechanically, the eight fibers are packed into the center of the cable in order to minimize stress around sharp bends. The strands are surrounded by a polyurethane inner jacket for crush resistance. Tensile strength is boosted by a Kevlar strength member woven like a rope. The cables are a quarter inch in diameter and have a pull strength of 500 pounds. Consequently, they are many times stronger than an ordinary coaxial cable of comparable girth.

Eight-channel fiber-optic connectors are provided at both ends of the link. These are ITT Cannon jeweled-ferrule type connectors. Attenuation is only 1.5 decibels, even after 1,000 mate-unmate cycles.

### Room for reliability

High reliability and exceptionally long life are the prime requisites of the link design. These were achieved by operating the system at far less than its capacity. For example, one design option was bandwidths of hundreds of megahertz over a distance of 0.5 kilometer. At the outset, however, a decision was made to limit the maximum bandwidth of each channel to 20 MHz, thus dramatically extending light source lifetime and enhancing overall system reliability.

At the front end of a typical channel of the data link either injection lasers or light-emitting diodes could have been used (Fig. 3). Injection lasers emit more power, have greater bandwidth, and can be driven at data rates in excess of 1 GHz. However, the need for just 20 MHz of bandwidth and 750 ft of cable make it possible to use the lower-cost LEDs.

The outer case of the LED is similar in size to a TO-18 transistor can—less than ¼ in. in diameter. A fiber-optic pigtail is attached to the LED, and light is coupled from the junction into the link by means of an optical connector.

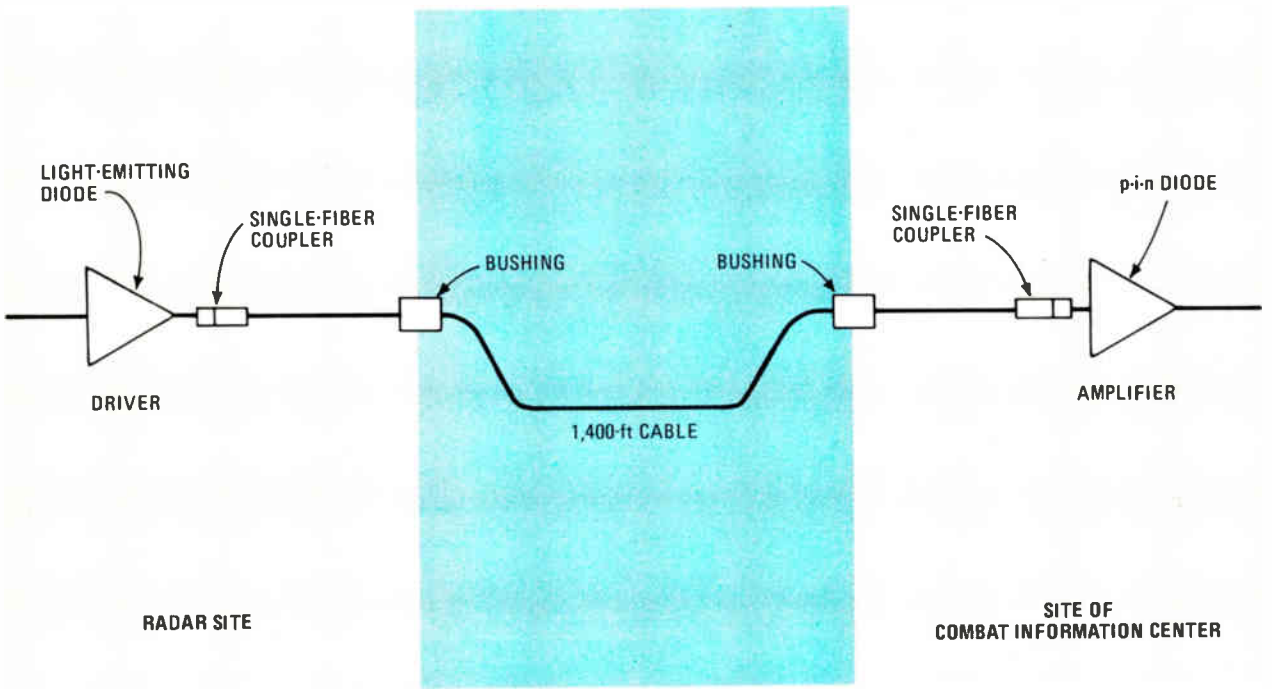
At the data-receiving end, data-encoded light passes through a second connector and into an interface device. This interface consists of a silicon diode detector that converts optical power into electrical current. Either a p-i-n or avalanche device can be used. For wideband applications, or where the signal level is very low, costly avalanche photodetectors must be chosen. But because of the limited bandwidth of the channels and the relatively short cable distance between the combat information center and the radar, a simple, low-cost p-i-n diode is preferable. An amplifier equipped with automatic gain control follows the p-i-n detector.

Link analysis and performance projections for fiber-optics data links are relatively straightforward. All necessary data is usually available from manufacturers' data sheets. The following analysis, typical for any fiber-optic data link, is for the performance of ITT Gilfillan's fiber-optic radar data link, connected in an AN/SPS-48C system.

### Plugging in the figures

Commonly available LEDs can launch at least 30 to 50 microwatts of optical power into a graded-index fiber with a 55-$\mu$m core and a numerical aperture of 0.25. To be conservative and allow for aging and the accommodation of production LEDs, the total launch power is assumed to be 20 $\mu$W (−17 dBm).

Since combinations of p-i-n diodes and preamplifiers have noise-equivalent powers of $5\times10^{-12}$ watt/hertz$^{1/2}$ typically, the noise-equivalent power for a 20-MHz bandwidth works out at $2.4\times10^{-8}$ W (−46.5 dBm). Thus, to meet a required voltage signal-to-noise ratio of 30 dB, the optical power arriving at the detector must be −31.5




**3. Typical link.** Each of the operational fiber-optic channels is a simple link with inexpensive light-emitting-diode generators and p-i-n diode detectors. The test site on land has a 1,400-foot link, although an aircraft-carrier run is about half this length.

## Military standards for fiber optics emerge

To qualify for use aboard a ship in the U. S. Navy, all the elements of a fiber-optic data link must meet all the requirements of MIL-E-16400G and any other applicable military specification. Almost none of these documents, however, calls out tests specific to fiber optics. For the MIL-E-16400G qualification, for instance, fiber-optic data links are divided simply into functional elements like the cable, connectors, transmitters and receivers, and terminal electronics.

In all but two of these areas specific standards are still being thrashed out in committee. Only for fiber-optic cable and connectors has any documentation yet appeared—a draft has just been released of MIL-STD-188-111, known as subsystem design and engineering standards for common long-haul and tactical fiber-optic communications. Final military specifications should start being issued some time this year.

Nonetheless, several military programs are already using fiber optics and are proceeding on schedule. In each case, detailed specifications were written for both the cable and connectors, not to mention other system elements, that require environmental and performance testing for each specific application. The results will help define the final military standards.

dBm, which allows the total link attenuation to be as high as [−17 dBm−(−31.5 dBm)], or 14.5 dB.

In the link described here two connectors are in series. On the conservative assumption of a 2.5-dB loss per connector, the total cable attenuation may amount to as much as 9.5 dB.

### Qualification grounds

To verify the fiber-optic data link's performance and data integrity projections, an operational system has been built and integrated with an operational, land-based radar test facility run by the Naval Sea Systems Command at Point Loma near San Diego, Calif. This site was selected because its topography simulated a naval warship's. A jut of land rising 100 ft above the mean high tide sustains a tower containing a suite of test-radar antennas and transceivers.

All transmitter and receiver electronics for the fiber-optic data link are located in the building at the foot of the tower. The combat information center (in this case a remote-operation center) is 1,400 ft from the tower and houses a variety of computers, signal processors, and displays. The presence of this equipment makes it possible to simulate and test shipboard radars and tactical data systems for most U. S. warships.

The 1,400-ft cable run at Point Loma is about double the 750-ft distance on aircraft carriers. Consequently, success in meeting this extra distance requirement implies that design margins for actual shipboard installations will be sufficient.

In keeping with the total allowable cable attenuation of 9.5 dB, the multifiber demonstration cable could have had a specified attenuation as high as 22 dB/km. But instead, a lowest-cost commercially available graded-index fiber with a 10-dB/km rating was used. All test results for this system indicate that the fiber-optic data link design is satisfactory in all respects.

The basic criterion (figure of merit) for data links is, of course, not the cable attenuation, but the signal-to-noise ratio of the system. This ratio, in turn, determines the system's bit-error rate. An examination of the characteristics of radar signals such as leading-edge jitter and rise time show that an S/N ratio of 20 dB is sufficient for the fiber-optic link.

But, to be even more conservative, the specification for the S/N ratio was established at 30 dB. A figure that caused no problem during the formal acceptance testing, the S/N ratio was found to exceed 40 dB on all the digital channels and 35 dB or better on the analog video channels from the radar.

Consequently, it is possible to operate the front-end driving LEDs at a far lower power level than in the previous already conservative design. This, in turn, extends the LED life expectancy and the system MTBF. Moreover, it leaves additional margin for LED degradation over time. Also, if the cables should ever be damaged and need splicing, the small signal loss per splice can easily be accommodated without degrading the overall system performance. Just what the final system specifications will be awaits further analysis. For one thing, the unique environmental effects of a ship on an optical-fiber link cannot be ignored and additional testing will be required in this area.

### Land, sea, and air

As it happens, most of the testing done on fiber-optic cables for military field use is also applicable to shipboard requirements (see "Military standards for fiber optics emerge," above). However, flammability, toxicity, and water blockage are additional requirements. Armoring also may be required for some installations.

These extra requirements can be met with little more than routine effort. For example, four different makes of multipin fiber-optic connectors are now undergoing environmental and life-cycle testing by the connector manufacturer. It is expected that these connectors, which fully qualify for tactical field use, will be suitable for shipboard use as well. However, they have yet to undergo a rigorous salt-spray test.

Because of its enormous savings in weight and bulk over conventional copper wire links, a fiber-optic data link is applicable to mobile, land-based radar systems for tactical field use, as well as to ships at sea. Readily deployable by jeep or light helicopter, these links can help remove field commanders and intelligence centers from missile-attracting radar transmitters. For example, field operations centers were previously limited to a mere 1,000-ft distance from radar sites by the attenuation of the wideband signals in the heavy copper cables. Now, with fiber optics, field information centers may be located as far away as 5 km from the site of a radar transmitter. □

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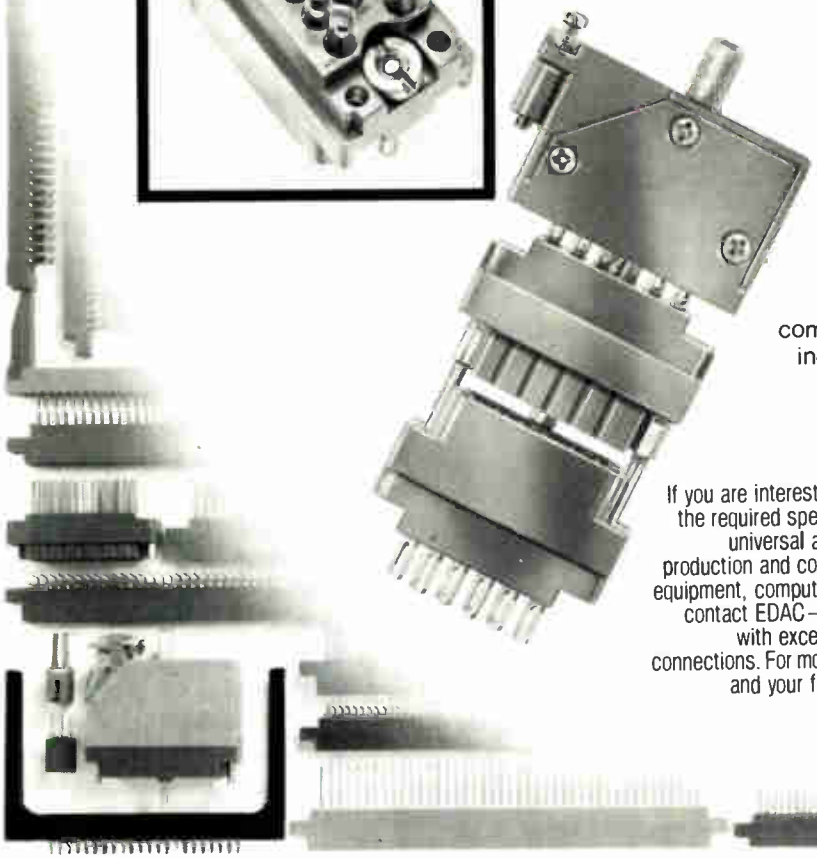

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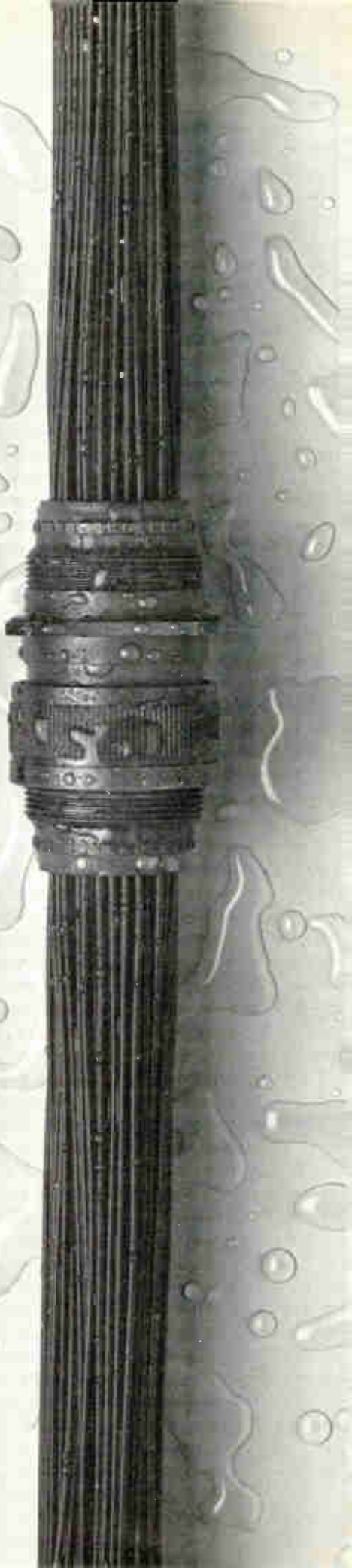


# Rectangular chip-carriers double memory-board density

## These leadless packages, a snug fit for elongated memory chips, will benefit the end user who knows how to attach them

by Bill Woodruff, *Mostek Corp., Carrollton, Texas*

☐ When the contribution each component makes in building a system is assessed, memory parts are found to be among the most heavily used semiconductors. In fact, in most computers and information-handling systems, multiple printed-circuit boards are committed to whole arrays of a single part type, such as a 16-K dynamic random-access memory. Until now, these memory boards have been populated by RAMs in dual in-line packages (DIPs), but memory chips in leadless ceramic chip-carriers, which have the advantages of increased board density and lower lead length, are gradually displacing or supplementing the DIP.

Originally, memory chips were placed in square leadless carriers conforming to the standards of the Joint Electron Device Engineering Council, mostly on leaded ceramic motherboards in dual and single in-line package configurations. The latest development is a Jedec-proposed rectangular leadless package, which is bidding to be the next standard memory package. It is already being used by some of the major integrated-circuit firms to house rectangular memory chips. Yet, before assessing the outlook for memories in chip-carriers, it is best to quickly review the status and shortcomings of the leadless carrier's predecessor, the DIP.

The earliest industry standard for memory DIPs was a 22-pin type, 400 mils wide. In 1973, Mostek introduced the 4096 4-K dynamic RAM in a 16-pin, 300-mil-wide package. The size reduction was achieved by multiplexing the row and column addresses—a configuration that has now been completely accepted for all 16-K, 64-K, and even the coming 256-K RAMs.

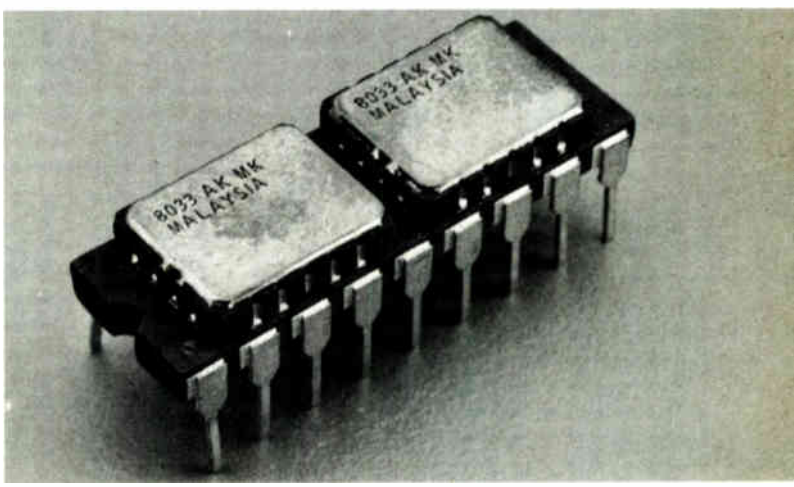
### Deficient DIPs

However, the DIP is large and heavy, and as pin counts increase, these factors are aggravated (Table 1). A more important drawback for some applications is the electrical characteristics of the DIP. The resistance and inductance from the corner pins to the input/output terminals of the die becomes significant for high-speed functions, particularly for the larger DIPs. As advancing technology and the Defense Department's Very High-Speed Integrated Circuits program raise speeds, the 4-gigahertz speed limit for leadless carriers will be significantly better than the DIP's 500-megahertz limit.

Chip-carriers present an opportunity for military and commercial manufacturers to halve their memory real estate on printed-wiring boards. In 1978, Mostek and a major computer manufacturer collaborated on an approach to an application problem that resulted in the introduction of the MK4332 (Fig. 1). By placing two MK4116 16-K RAMs in chip-carriers side by side on a ceramic DIP daughterboard, end users can reap the advantages of leadless carriers while using existing DIP manufacturing techniques in assembly. Over 3 million such MK4332s have since been shipped, making it one of the first large commercial usages of memories in chip-carriers in which cost and volume availability had made their use finally feasible.

The mechanical configuration for a family of standard square leadless packages has been defined for years now by Jedec [*Electronics*, March 17, 1977, p. 89]. Package types A, B, C, and D have become available in a range of sizes and have made it possible to purchase many logic functions in leadless carriers from both logic manufacturer and their die distributors.

Today's memory ICs, however, differ from their earlier small- and medium-scale integration counterparts. Their dice tend not only to be much larger but also rectangular instead of square. These factors, combined with the added packing density of memories in rectangular packages, will aid in creating denser pc-board layouts, and




**1. Togetherness.** One of the first approaches to using rectangular chip-carriers was this Mostek Ram-pak, in which two 16-K dynamic RAMs mounted in two ceramic chip-carriers were reflow-soldered onto a ceramic motherboard whose leads were on 100-mil centers.

TABLE 1: COMPARISON OF DUAL IN-LINE PACKAGES AND LEADLESS CHIP CARRIERS

| Number of leads | | Package area (in.$^2$) | | Package weight (g) | |
|---|---|---|---|---|---|
| DIP | LCC | DIP | LCC | DIP | LCC |
| 16 | 18* | 0.24 | 0.10 | 1.4 | 0.4 |
| 16 | 20 | 0.24 | 0.12 | 1.4 | 0.5 |
| 24 | 32* | 0.72 | 0.25 | 4.7 | 0.9 |
| 40 | 44 | 1.20 | 0.42 | 6.4 | 1.6 |
| 64 | 68 | 2.88 | 0.90 | 12.11 | 3.2 |

* Rectangular packages.

new Jedec packages, types E and F, have been proposed. These new types will be similar to the square type C (a leadless cavity-up type) carrier in construction.

Figure 2 shows an MKB2716E 2-K-by-8-bit erasable programmable read-only memory in a leadless type E package. This standard includes the 32-pad, 450-by-550-mil and a 28-pad, 350-by-550-mil package.

The two variations of the leadless type F package are shown in Fig. 3 with their footprints (solder pads) up. As can be seen, each has 18 pads—with an interesting difference. The pads on each end of the longer 425-mil-by-285-mil device have been extended inward. In this way, a degree of compatibility has been achieved because the footprint of the larger device will thus extend inward so as to cover the same footprint as the smaller 285-by-350 mil device.

The larger leadless type F device was not "stretched" to add extra pads but to house the large die of the 64-K dynamic RAM. As can be seen in Fig. 4, the die size and configuration force the use of these rectangular leadless carriers to obtain optimal packing density.

When the chosen leadless carrier has the same number of pads as the DIP it replaces, locating the interconnects is simple as, for example, with 4-K-by-1-bit and 16-K-by-1-bit static RAMs. However, when extra pads appear, an opportunity arises for differences to develop between vendors. Fortunately, a *de facto* standard has emerged for dynamic RAMs based on the MK4116E, which has been offered since 1978.


**2. The right shape.** Chip-carriers for memory chips are rectangular rather than square because of their elongated memory die within. The MKB 2716E 2-K-by-8-bit E-PROM is this view in a leadless type E package that measures 450 by 550 mils.

Byte-wide memories in 32-pad type E 450-by-550-mil leadless packages are becoming available. Mostek's pinout for byte-wide parts takes advantage of the 32 pads in a configuration that is capable of accepting all current and future members of the Jedec family of RAMs, ROMs, and E-PROMs.

One the greatest problems facing any prospective user of memories in leadless packages is how to attach them directly to a substrate. Direct attachment of the package to a substrate is most often performed by reflow soldering. Different methods exist for this operation since many firms have experience in reflow-soldering flat packs, chip capacitors, and other devices.

Basically, either one or both of the surfaces is pretinned with solder prior to the component being placed on the joint. The temperature of the joint is then raised to the melting point of the solder, whereupon the solid solder melts, wetting to itself and forming a single, quality solder joint.

With a leadless chip-carrier array, the above process becomes much more involved than the familiar one of "tacking" a capacitor to a pc board with reflow soldering. A variety of designs, materials, and processes have been successfully used. However, for the leadless carrier, unlike simple leaded components, an element of fine tuning is needed to obtain optimal results.

A pattern of footprints (pads) is normally plated onto the surface of a pc board or screened onto that of a ceramic substrate. Solder paste is applied to these footprints by normal screening methods. The variables introduced at this point are the thickness of the screen (determining the height of the solder buildup) and the characteristics of the solder paste. The solder paste includes grains of solder plus a resin flux.

## Another screening

Following the first screening, the board is brought to the reflow temperature of the solder, forming even bumps on each of the equally sized pads. This step may be replaced by the plating of nonfused solder on the board. Either process achieves a two-fold goal—confirmation of the solderability of the board and an initial buildup of the solder mass that will contribute to the eventual gap which will develop between the leadless carrier and the pc board.

Next, the screening operation is repeated, except that the tacky nature of the solder paste will not go to waste. Following the solder screening, the carriers can be positioned on their footprints, where they will be protected against normal handling shock by the solder paste.

Mostek's Ram-pak assembly process, in which leadless packages are attached to a ceramic motherboard, exemplifies one extreme of conditions in that a production rate of 50,000 pieces a week can be maintained on a single part type. However, such an output is difficult for end users to achieve because solderability of the carrier's

pinouts decreases with storage time.

Another key advantage that can be gained only by manufacturing in volume is a streamlined production flow. Following the pick-and-place operation, the Ram-paks are transferred to the belt of an infrared furnace. As the parts emerge, they fall into a solvent, where they accumulate prior to being subjected to a conventional vapor degreasing operation. Ram-pak parts have other advantages due to their simple configuration. Inspection may be done visually, due to the 5-mil gap under the carrier. The systems house performing its own reflow operation will typically have neither the ability to inspect visually nor the 5-mil height of the air gap.

A production process that can yield better results for the end user involves the pretinning of individual leadless carriers by floating them in a solder pot. The resultant solder bump on the carrier pad not only permits inspection of the pad surface for solderability, but also adds to the quantity of solder in the final joint. Such pretinned carriers can be placed on the same surfaces as described earlier, except that instead of going straight into a furnace, the assembly is dried at about 80°C to drive the solvents from the flux. At this point, a prepared unit awaits the choice of heating methods.

In a reflow-soldering operation, no solder is added to a board surface. The board is then brought up to the eutectic point of the solder, at which point the prewetted joints become molten again and a single fillet results where two distinct surfaces once existed. Various furnaces have different advantages, but the technique most commonly associated with leadless chip-carriers is vapor-phase soldering.

Vapor-phase reflow soldering, which has been made viable by HTC Corp., Concord, Mass., is a true reflow technique. The technique hinges on immersing the relatively cool parts into boiling FC-70, an inert fluorocarbon manufactured by the 3M Co., St. Paul, Minn.

As the FC-70 vapor condenses on the assembly, it is quickly and uniformly heated to the boiling temperature of the fluid. Since FC-70 has a boiling point of 215°C, any properly prepared joints quickly reflow. Vapor-phase soldering has become synonymous with leadless carriers because of its uniformity in applying heat and the repeatability of its results over a variety of part types. But vapor phase does suffer from the high cost of the FC-70 fluid, and for well-controlled volume runs, other heating methods deserve consideration.

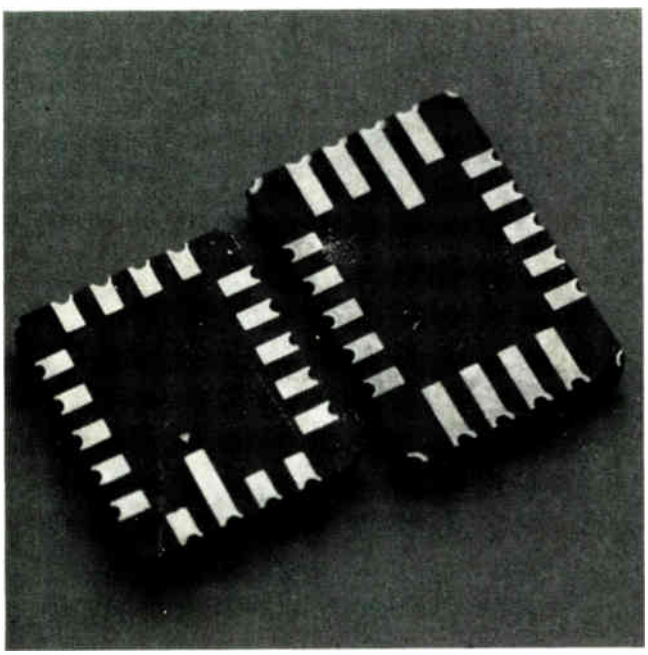
The Ram-pak assembly line uses an infrared furnace to attach leadless carriers to cofired ceramic substrates. This method is not without faults in that the gold lids of the packages reflect infrared energy. For a high-volume assembly that can be characterized over time, proper belt speed and energy levels can be determined to achieve an acceptable quality level; however, the amount of testing required with this method could cause excessive rejection rates on small-volume runs.

Convection furnaces and controlled temperature hotplates may be used with success. Since leadless-carrier attachment is simply a heating process to reach reflow temperature, any heating method should work.

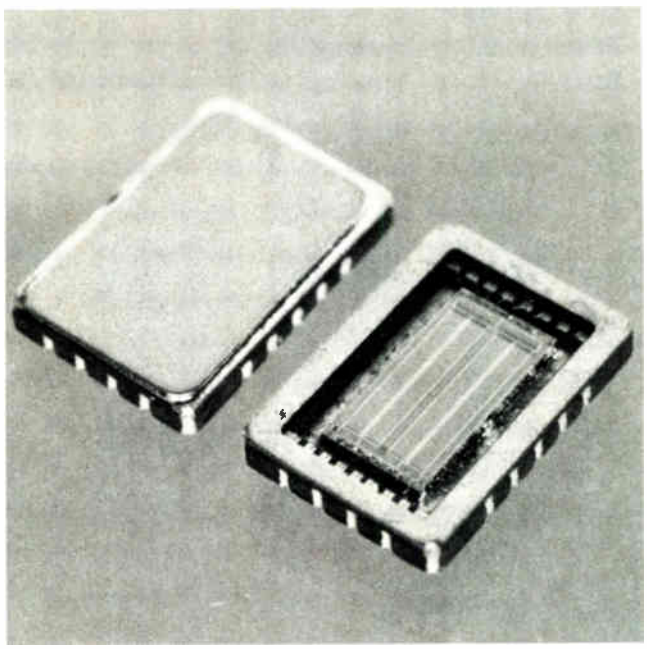
### Choosing a substrate

The preceding soldering techniques can be used on any type substrate, so the material is typically chosen on the basis of system constraints and not processing limitations. Yet, other factors beyond the thermal characteristics should be considered.

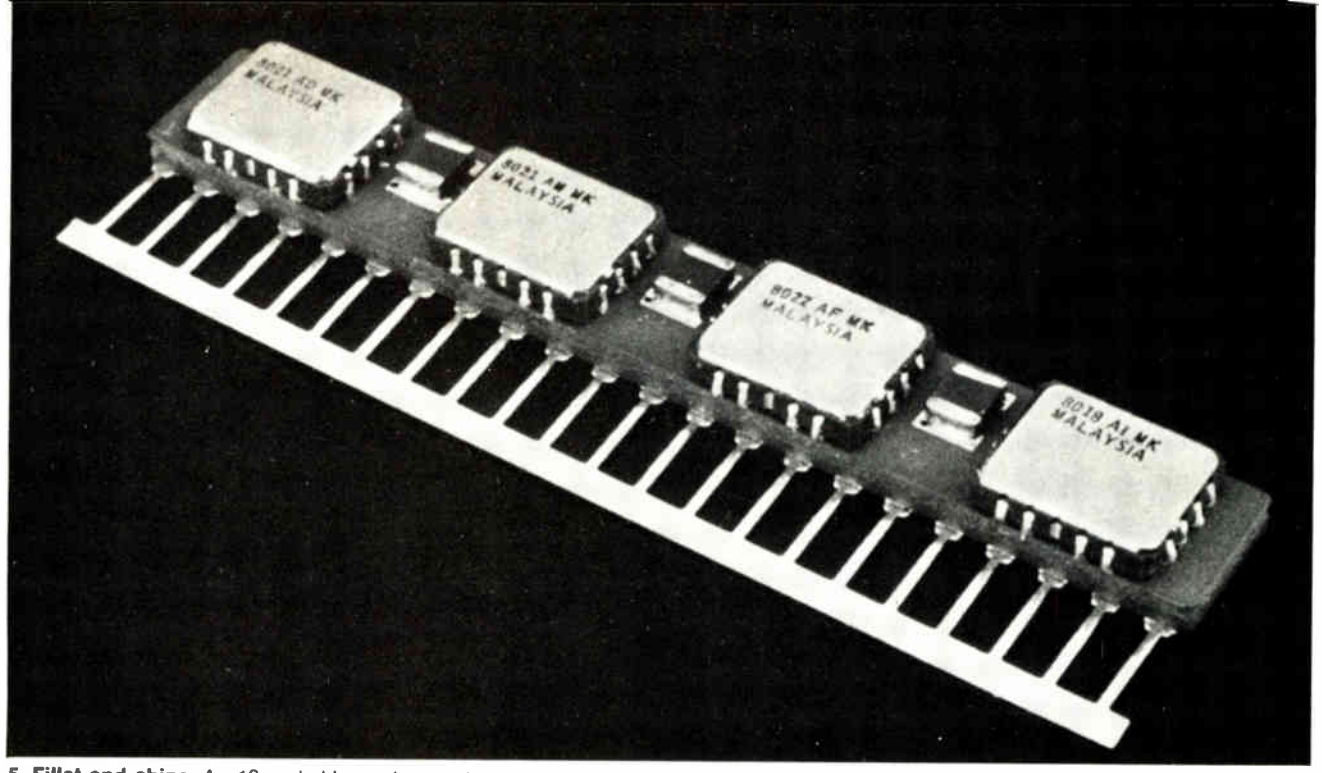
How a system is partitioned affects its design in many ways. Enclosure costs, manufacturing costs, and repairability are all affected. Because of the limited size of a



**3. Variations on a theme.** The leadless F carrier is an 18-pad package. The two F variations are shown with their mounting pads up. The pads of the larger carrier have been extended inward, allowing both packages to match with a common substrate pattern.



**4. Loaded dice.** A type F chip-carrier is designed to carry the large die of the 64-K dynamic random-access memory. The photo at the right shows a 64-K RAM chip bonded into the carrier's cavity. Note the rectangular shape of the large memory die.



**5. Fillet and chips.** An 18-pad chip-carrier can be reliably soldered to glass-epoxy boards. Here the solder pads of the board have been extended out from the edge of the carriers a distance equal to the height of the carriers' castellation, resulting in strong solder fillets.

single piece of ceramic, placing leadless carriers onto a leaded ceramic substrate is an easy first stratagem.

The 4332 shown earlier represents a minimal configuration with two 4116Es mounted on a ceramic daughterboard. Many end users can now successfully use leadless carriers by buying the assembled 4332D. The ceramic motherboard concept can be further expanded to accommodate a 16-K-by-4-bit memory in a SIP for vertical mounting, or into four, eight, or more chips per substrate as the designer chooses. Augat Inc., Attleboro, Mass., for example, offers a variety of substrates designed to accept the 4116E.

The ceramic substrates discussed so far reflect the importance of selecting a compatible substrate material to be used in systems employing leadless carriers. Since reflow soldering is the preferred method of carrier attachment, mechanical constraints are raised that have not been of importance with DIPs.

TABLE 2: THERMAL EXPANSION COEFFICIENTS OF MATERIALS USED WITH LEADLESS CHIP CARRIERS

| Material | Temperature coefficient of expansion (ppm/°C) | Difference from expansion coefficient for LCC (%) | Thermal conductivity (Btu/h/ft²) |
|---|---|---|---|
| 90% to 94% alumina LCC package | 6.5 | – | 9.6 |
| 96% to 99.5% alumina thick film substrate | 6.8 | 5 | 12.0 |
| 90% to 94% alumina cofired substrate | 6.5 | — | 9.6 |
| Epoxy-glass (G-10) | 18.0 | 177 | 0.17 |
| Polyimide-glass | 13.0 | 100 | – |
| Polyimide-Kevlar | 5.5 | 15 | – |
| Alloy 42 0.025 in. | 5.8 | 11 | 8.8 |
| Steel 0.025 in. | 10.0 | 54 | 27.0 |

Thermal coefficients of expansion reflect the amount of give that a material will require as it is cycled over temperature (generally implying a transition from −55° to +125°C). When materials of different expansion coefficients are bonded together, the bond must either flex or be strong enough to withstand the resultant forces. Table 2 gives the tempco for leadless chip-carriers and for a number of popular (or potentially viable) substrates. As the table shows, ceramic on ceramic will result in the lowest mismatch and, therefore, the highest joint reliability.

Ceramic is not as difficult to use as it may seem. The DIP and SIP concepts previously discussed can easily be modified to handle other configurations, and the smaller user need not handle the assembly right away. EDI of Ashland, Mass., for example, produces a 256-K-by-1-bit memory in a SIP and can provide design and assembly services to the user. The firm's designs will typically be prototyped with thick-film ceramics that have multiple screened layers on a single preformed piece of ceramic. As volumes approach the 1,000-piece level, conversion to cofired ceramic begins to be cost-effective.

Here each screening layer is put on a separate sheet of greenware, which is then stacked and fired. The resulting ceramic assembly is in effect a solid piece of ceramic with all electrical connections implemented internally. Ceramics manufacturers have made up to 43-layer assemblies this way, and in fact, this process is the assembly method for the 3-layer–style leadless package that is offered by most IC manufacturers.

While ceramic does have a number of virtues that are prompting its use, it is heavy, breakable, and available in a maximum size. These factors, combined with the constraint that ceramic assemblies for leadless carriers are generally daughterboards that then go onto a pc board, raises the question of the feasibility of directly attaching ceramic chip-carriers to pc boards.

The primary problem with such a pairing is joint reliability. The obvious worst-case example is that of a large (over 40-pad) leadless carrier mounted on a G-10 glass-epoxy pc board. This combination has repeatedly been tested with consistently bad results.

But what about the best case? A large aerospace firm recently examined the problem of attaching 18-pad leadless carriers onto G-10 glass-epoxy boards and came up with some interesting results.

### Free flow

Since previous work demonstrated that solder joints directly under carrier pads fail quickly, the effect of extending the pads was analyzed. Researchers found that as the reflow soldering process occurs, the molten solder will flow wherever it can along the pad, the board, and the castellation on the side of the carrier. If the pad extends out from the edge of the package a distance equal to the height of the castellation, then a good fillet will form. The fillet is easily inspected (Fig. 5) and also provides a degree of resiliency that allows the joint to survive the stress of over 200 thermal cycles well.

The worst tempco shown in Table 2 is for glass-epoxy G-10 pc board material so other materials might perform even better with the same technique. Polyimide is a board material that is gaining acceptance and demonstrates better reliability for plated through-holes, as well as better repairability due to its resistance to lifted pads. When polyimide is used with a Kevlar core, even better tempcos result. However, cutting and drilling are difficult in this tough material.

Metal-core and laminated circuit cards are other ways of getting better coefficients. The PCK division of Kollmorgen Corp. in Melville, N. Y., is developing one such approach using its Microwire technique. Other approaches using porcelain-coated steel and copper laminates are also being studied.

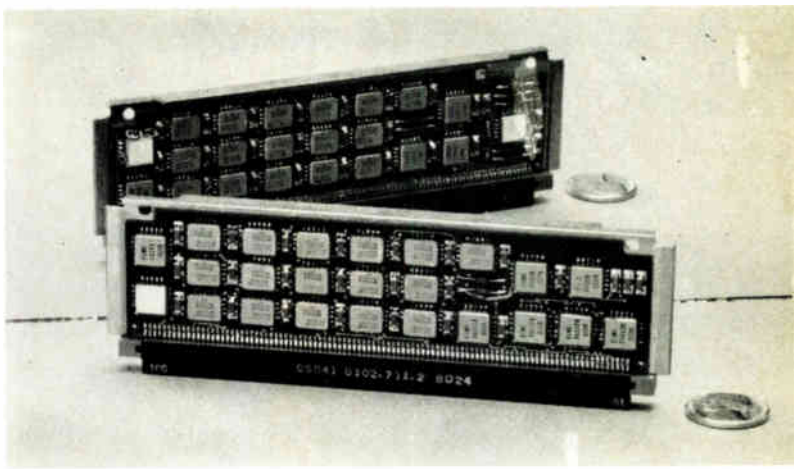
The entire subject of attachment of leadless ceramic chip-carriers, reliability, and repairability is being studied under Air Force contract. These studies will complement the work being carried out by many military manufacturers and will greatly increase the knowledge of mounting leadless carriers during the next year.

### Repair and replacement

So far, manufacturing techniques have been described that are applicable at the assembly level, but the repair of leadless–chip-carrier assemblies has not yet been considered. When a ceramic substrate is used, it can simply be placed back onto a hotplate and the defective carrier lifted off with a vacuum pencil once the solder melts. A pretinned replacement unit is dropped into place, and the surface tension of the molten solder will align it.

Repairing pc boards containing chip-carriers is more difficult, but then so is removing defective DIPs. One method in use involves a specially made "soldering tong" that clamps onto all four sides of the package, heating up the device. Again, replacement should be the opposite of removal when a pretinned carrier is used.

Integrated-circuit reliability is directly related to junction temperature, so an effective thermal design is a must in today's reliability-conscious environment. Leadless chip-carriers offer the system designer some unique opportunities for creative design because they are mounted onto surfaces.



**6. Hot plates.** This standard electronic module has two multilayer epoxy-glass printed-circuit boards, each with an array of memory chips in ceramic leadless carriers, bonded to each side of a copper frame. Board heat is conducted away by the copper heat sink.

Jedec standards have recognized this by specifying two basic types of carriers. The type A and type D carriers are cavity down. In these carriers, the die is closer to the top, where the best heat-radiating surface exists. But an extra penalty is paid in that the package's outside dimensions are larger than cavity-up configurations for a given die size. The types B and C carriers will be more common for that very reason, given the importance of density.

Thus, most leadless carriers will have a cavity-up configuration with the major heat-radiating surface facing the board. Tests show that the thermal resistance of the package is roughly equivalent to a DIP's, so the mounting method directly affects junction temperature.

Two types of heat transfer occur: conduction and convection. Most commercial systems employ forced-air and convection cooling, so surface area is a key to good heat transfer. The daughterboard approach employing the SIP is a perfect blend of pc boards and leadless carriers in that the SIP, with carriers can be mounted vertically. Not only is the density greater than with leadless carriers directly attached to pc boards, but forced air can cool the assembly.

Most military manufacturers and some commercial ones do not have the luxury of moving in outside air with a fan and blowing it around their devices. They rely on conduction to transfer the heat through the frame to an outside heat sink. Thus, the firms are concerned about the thermal properties of their substrates.

The thermal conductivity data in Table 2 shows that solid metals are excellent for removing heat, but poor in tempco match. So a solution such as the one shown in the standard electronic module in Fig. 6 can be used. Here two multilayer G-10 pc boards are bonded to both sides of a copper frame. The bonding compound must be compliant since the copper is present for rigidity and thermal transfer and is not meant to force a match in tempcos of the boards and the frame. □

# 8-bit DMA controller handles 16-bit data transfers

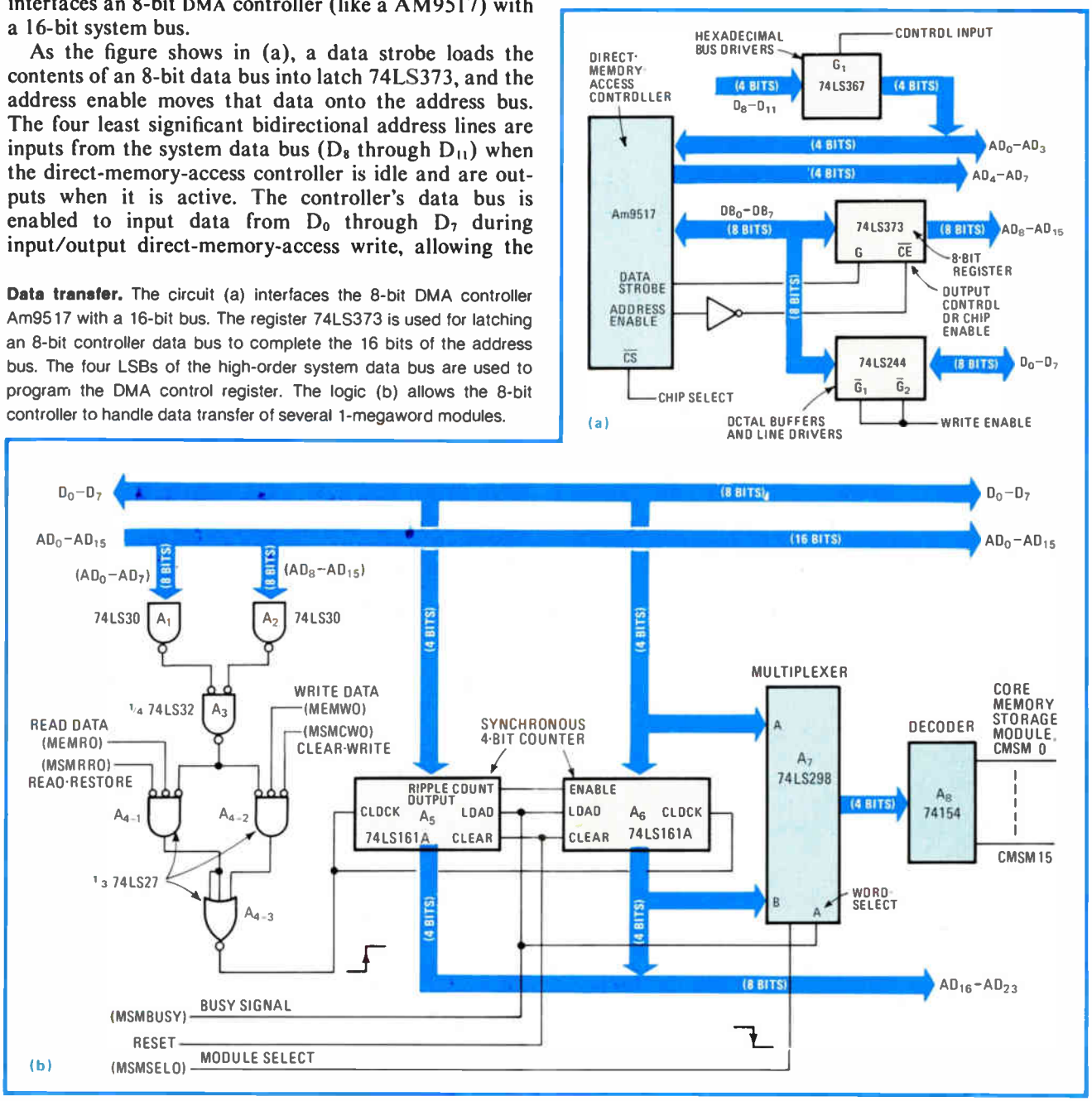
by Trung D. Nguyen
*Litton Data Systems Division, Van Nuys, Calif.*

Many microcomputer systems today are 16 bits wide. But only 8-bit controllers are available to handle direct memory access for them should they need it. This circuit interfaces an 8-bit DMA controller (like a AM9517) with a 16-bit system bus.

As the figure shows in (a), a data strobe loads the contents of an 8-bit data bus into latch 74LS373, and the address enable moves that data onto the address bus. The four least significant bidirectional address lines are inputs from the system data bus ($D_8$ through $D_{11}$) when the direct-memory-access controller is idle and are outputs when it is active. The controller's data bus is enabled to input data from $D_0$ through $D_7$ during input/output direct-memory-access write, allowing the processor to program the DMA control register.

The circuit (b) allows the 8-bit controller to transfer data between several 1-megaword core-memory storage modules and a 16-bit system bus. Initially, the outputs of counters $A_5$ and $A_6$ are reset to all 0s by the reset line. The A inputs selected by multiplexer $A_7$ are decoded by $A_8$ to select a desired module when the module select signal (MSMSELO) is active. Data (not shown) is stored at the addressed location selected by controller's address lines ($AD_0$ through $AD_{15}$). The busy signal (MSMBUSY) switches to the busy state when the controller initiates either the reading of data (MEMRO) from the storage

**Data transfer.** The circuit (a) interfaces the 8-bit DMA controller Am9517 with a 16-bit bus. The register 74LS373 is used for latching an 8-bit controller data bus to complete the 16 bits of the address bus. The four LSBs of the high-order system data bus are used to program the DMA control register. The logic (b) allows the 8-bit controller to handle data transfer of several 1-megaword modules.



module during a read-restore (MSMRRO) or writing of data (MEMWO) into the storage module during a clear-write (MSMCWO).

If an address location larger than 64-K is needed to access the storage module, the controller's addresses $AD_0$–$AD_{15}$ are all high, causing the gate $A_3$ output to go low. The leading edge of the $A_4$–$A_3$ output advances counter $A_5$ whose output ($AD_{16}$ through $AD_{19}$) together with $AD_0$ through $AD_{15}$ is used to access the entire 1-megabit address of the module.

If more than a 1-Mb address location is required, the ripple count output of $A_5$ goes high, enabling counter $A_6$ to select the next–higher-order module. The outputs $AD_{20}$–$AD_{23}$ of $A_6$ are used for higher address locations. Decoder $A_8$ selects up to 16 modules. Extra counters and decoders may be added for more modules. □

# Capacitive voltage doubler forms ±12-to-±15-V converter

by Tom Durgavich
*National Semiconductor Corp., Santa Clara, Calif.*

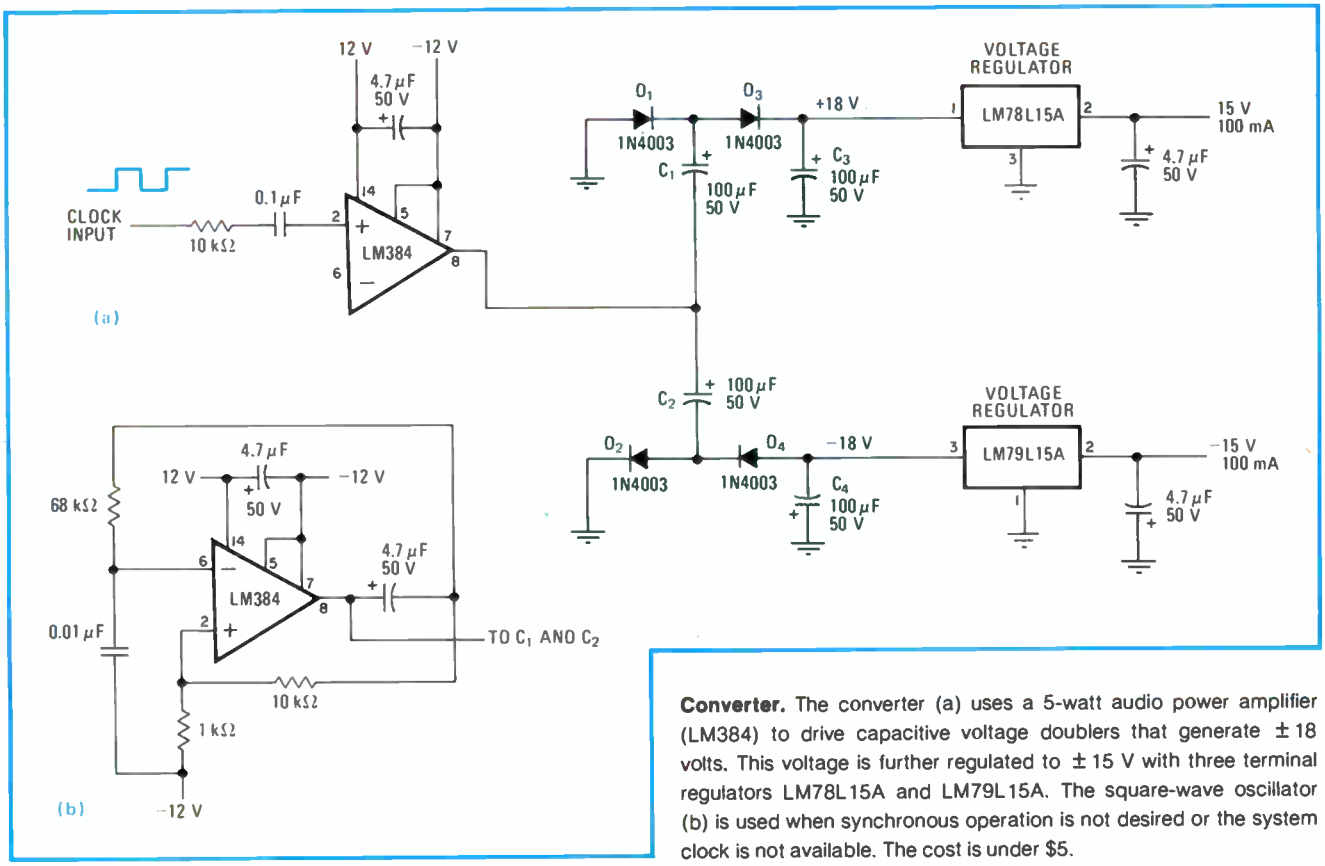
Pairing a capacitive voltage doubler with a regulator provides a simple solution to the problem of converting ±12 volts dc into ±15 V dc. Such a conversion is often required in systems using Intel's Multibus, for example, which puts out only ±12 V dc. Such a conversion is often tional amplifiers and data converters to a guaranteed voltage swing of ±10 V. Unlike conventional dc-to-dc converters, this approach is inexpensive and occupies little board space.

The circuit (a) uses a 5-watt audio power amplifier (LM384) to drive capacitive voltage doublers that generate ±18 V. One doubler, consisting of capacitors $C_1$ and $C_3$ and diodes $D_1$ and $D_3$, generates +18 V and the other, consisting of $C_2$ and $C_4$ and $D_2$ and $D_4$, −18 V. The saturation voltage of the 384 op amp along with the voltage drop across the diodes prevents these voltages from ever reaching ±24 V.

The power-amplifier clock input derived from the system clock keeps the switching waveform synchronous and random noise to a minimum. The clock input voltage and frequency can vary from 2 to 12 V peak to peak and 3 to 20 kilohertz, respectively. The 7-kHz square-wave oscillator (b) is used when the system clock is not available or synchronous operation is not desired.

The output current of this converter is limited to 100 milliamperes but can be slightly increased by providing the op amp with a good heat sink. The ±18 V unregulated voltages may be increased to greater then ±30 V by connecting diodes $D_1$ and $D_2$ to +12-V and −12-V sources instead of to a ground connection. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.




**Converter.** The converter (a) uses a 5-watt audio power amplifier (LM384) to drive capacitive voltage doublers that generate ±18 volts. This voltage is further regulated to ±15 V with three terminal regulators LM78L15A and LM79L15A. The square-wave oscillator (b) is used when synchronous operation is not desired or the system clock is not available. The cost is under $5.

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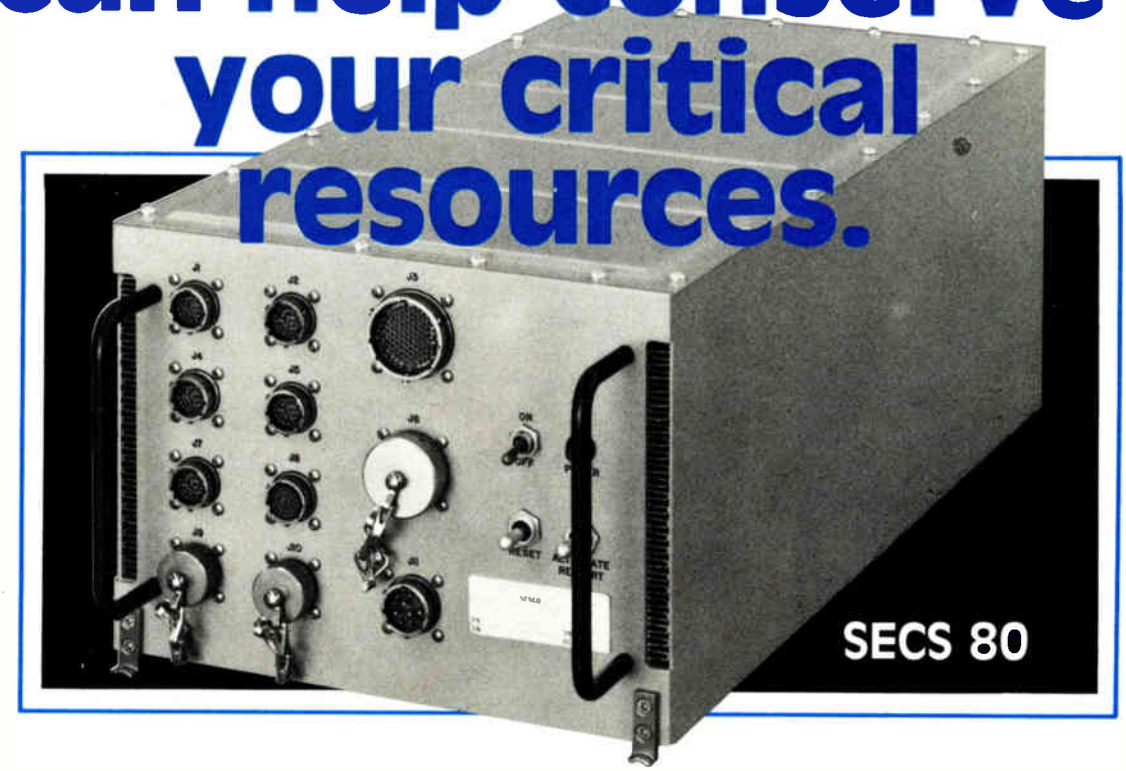


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**COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS**

# C-MOS IC achieves triggered phase-locked oscillations

by N. Miron, M. N. Ion, and D. Sporea
*Central Institute of Physics, Romania*

The application of dual vernier interpolation to time-interval measurements requires a triggered phase-locked oscillator that is phase-synchronized with the external trigger signal. This circuit (a) is a modification of the idea proposed by D. C. Chu[1] and uses a complementary-MOS medium-scale integrated circuit to make it simple and inexpensive.

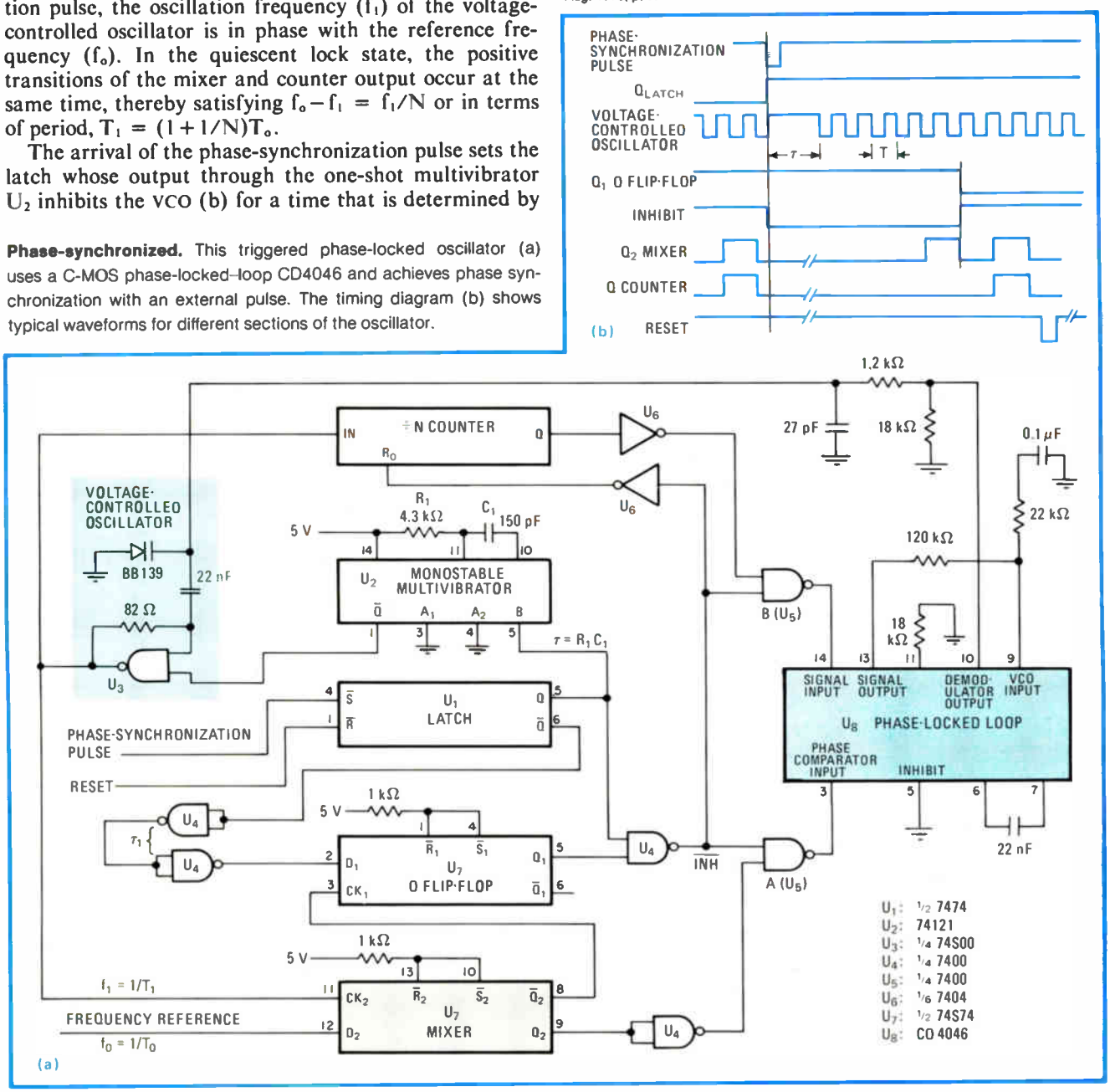
Prior to the arrival of an external-phase–synchronization pulse, the oscillation frequency ($f_1$) of the voltage-controlled oscillator is in phase with the reference frequency ($f_o$). In the quiescent lock state, the positive transitions of the mixer and counter output occur at the same time, thereby satisfying $f_o - f_1 = f_1/N$ or in terms of period, $T_1 = (1 + 1/N)T_o$.

The arrival of the phase-synchronization pulse sets the latch whose output through the one-shot multivibrator $U_2$ inhibits the VCO (b) for a time that is determined by $R_1C_1$ ($\tau$ = 600 ns). However, when the VCO starts again with a zero phase shift, the signal $\overline{INH}$ (inhibit) resets the divide-by-N counter.

This $\overline{INH}$ signal through NAND gates A and B also inhibits the three-state phase comparator ($U_8$) that will remain in a high-impedance state between the arrival of the phase-synchronization pulse and the first negative transition of mixer output $\overline{Q_2}$. The $\overline{INH}$ state is changed by this sequence, thereby enabling gates A and B and directing the mixer and counter outputs to the phase-comparator inputs.

The delay $\tau_1$ introduced at the latch's output $\overline{Q}$ avoids locking a possible initial mixer negative transition that is not related to phase crossover. The circuit is set to the initial state with an external RESET signal. □

**References**
1. D. C. Chu, "The triggered phase-locked oscillator," Hewlett-Packard Journal, Vol. 29, Aug. 1978, p. 8.




**Phase-synchronized.** This triggered phase-locked oscillator (a) uses a C-MOS phase-locked-loop CD4046 and achieves phase synchronization with an external pulse. The timing diagram (b) shows typical waveforms for different sections of the oscillator.

# Engineer's newsletter

## Three measurements check values of components in circuit

Have you ever tried to calculate the value of a component from measurements taken with the component still wired in a circuit? Frank D. Witmer has, and reports, "The problem is like Rubik's cube—you can burn up a lot of time trying to figure it out." So here is the simple method he developed for use at Motorola Inc. in Franklin Park, Ill. **First measure the impedance across the component of interest, calling this reading X.** Then move one of the probes to any other circuit node; let Y stand for this value. Finally, repeat the second measurement with a short across the component of interest; call this value Z. The three readings determine the component's value, according to the equation $XZ \div [Y - (XY - XZ)^{1/2}]$.

## NBS goes on line with computer news

Those with an eye toward improving computer performance will want to dial up the National Bureau of Standards' inside line on the subject. NBS has developed a computerized bulletin-board system (CBBS) to help you **find out about current tools and techniques for measuring a machine's efficiency.** The system is designed for Federal users, but your participation is wanted. To read the message board, you need a 300-b/s terminal and an acoustic coupler—just dial (301) 948-5717 and press the return key several times after the CBBS comes on line. No account numbers are needed, and the system prompts users with menus. The messages will tell you how to measure performance and avoid processing bottlenecks. And if you have a hint you'd like to share, anyone can put messages up on the board. For further information, call Ken Moore of the NBS Institute for Computer Sciences and Technology at (301) 921-3861.

## Cheap op amps suffice for mini tape decks

The low supply voltage in a battery-operated cassette player will effectively increase the power bandwidth of your amplifiers, so less expensive operational amplifiers are enough for the job. Paolo Antonaiazzi of SGS-Ates in Agrate, Italy, reminds you that the highest operating frequency for an op amp without significant slew-rate distortion is directly proportional to the slew rate and inversely proportional to the signal swing. **Thus, for a 3-to-6-V supply of the kind found in battery-operated equipment, large-signal bandwidth is increased.** As an example, Antonaiazzi shows that the low-cost LS141 op amp—with a 0.5-V/$\mu$s slew rate—maintains a 1% distortion figure only to 8 kHz for a 20-V voltage swing, but for a 4-V swing, the bandwidth extends to more than 30 kHz.

## Where to learn about VLSI modeling

A short course at the University of California at Los Angeles will be devoted to the capabilities and limitations of small MOS devices and the models used to simulate their behavior. C. R. Viswanathan, professor and chairman of the electrical engineering department, will give the course on March 2 to 4. Call him at (213) 825-5214 for more information.

Need more help? The Advanced Study Institute of the North Atlantic Treaty Organization will present a systematic study of the physics, modeling, and simulation algorithms related to the fabrication and operation of MOS devices in very large-scale integrated circuits. **The course will be held at the Sogesta Institute, near Urbino, Italy, July 12 to 23, with lectures by prominent American and European experts.** Further information and application forms may be obtained from the director of the Advanced Study Institute, Prof. P. Antognetti, Istituto di Elettrotecnica Viale, Cause 13, 16145 Genova, Italy.

**-Roderic Beresford**

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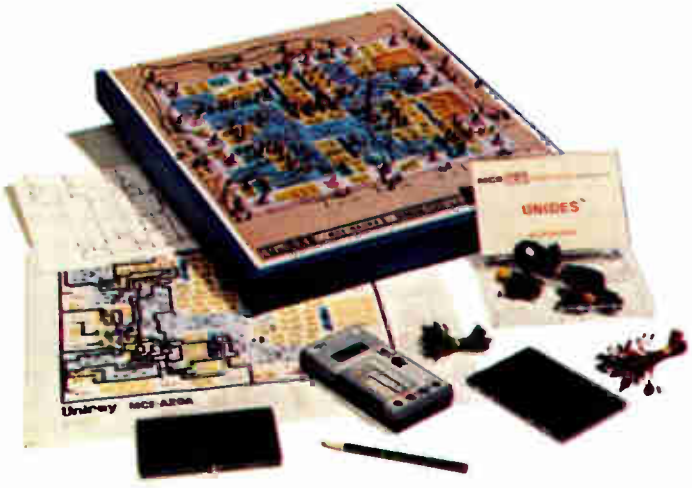


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**MCE can integrate your IC designs in the shortest time possible by:** providing the UniDES™ board (MCE's powerful new circuit development and evaluation system) to evaluate circuit performance, to determine interconnect errors and judge performance... circuit simulation by computer models before generating production masks... and computer-aided mask design.

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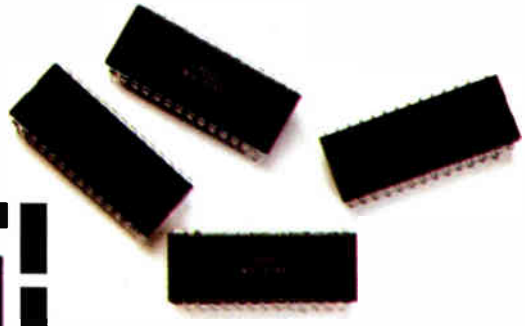
Circle 131 on reader service card




Gentlemen: I'm very interested in how you might be able to support and assist me in developing my integrated circuits. Please send me a copy of your new capabilities brochure **"A World of Possibilities."**

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Micro-Circuit Electronics, 1270 Oakmead Parkway, Suite 101, Sunnyvale, CA 94086. Telephone (408) 732-6090, Telex 171895 (M CELECTR SUVL).

Micro-Circuit Engineering Vertr. GmbH, Pirckheimer Str. 124, D-8500, Nürnberg, W. Germany. Telephone 0911-533993, Telex 06-22748 (SVOLKD).

Micro-Circuit Engineering Vertr. GmbH, Blumenstr. 9A, D-8013, Haar/München, W. Germany. Telephone 089-463085, Telex 05-212965 (MCEMD).

# High density digital recording with fingertip control of data rate and density.

With Honeywell's new HD-96, you can instantly program data rate and packing density at the touch of a thumbwheel, and record or reproduce high density digital data *without recalibration.*

Other major features of our new High Density Digital Magnetic Tape Recorder include:

- Automatic equalization
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**Honeywell**

Circle 132 on reader service card

# iAPX 432 enhances board CAD

32-bit Intel processor does automatic placement and routing; the same option adds networking capability to the system

*by J. Robert Lineback, Dallas bureau*

**The CX-I option** for Summit CAD Corp.'s SX-II computer-aided design station for printed-circuit boards is one of the first offerings of a system using Intel Corp.'s iAPX 432 32-bit microprocessor chip set. The option makes the SX-II station the center of a Pathfinder CAD network with up to 60 stations and gives the user automatic-placement and -routing capability; logic simulation is a planned addition to the system's functions.

According to Gregg Young, cofounder and chief executive officer of Summit, the first CX-I packages will execute "fairly straightforward algorithms." First-pass prototyping was done with 8086 microprocessors; Intel's release of Ada is being used by the firm.

**Add-in.** The recently introduced SX-II design station is priced at $62,500; the CX-I hardware, which is installed in vacant slots of the SX-II, and associated software bring the price of a central Pathfinder station to $75,000. Deliveries of the CX-I option will take 60 days.

The price includes 1 megabyte of error-correcting random-access memory for the 432 processor (using 64-K RAM chips); 2 megabytes are also available. This large semiconductor memory allows automatic-placement and -routing software to be loaded from Winchester disk storage and then executed rapidly without disk access.

Central-network functions are performed by an 8-bit microprocessor in a communications-controller module; only one such module is needed to link up to 60 stations. The serial transmission rate is 1 Mb/s over twisted wire pairs that can be thousands of feet in length. In addition to SX-II design stations, the network links Summit's RT engineering terminals and LX-I photoplotters. The LX-I produces masters on glass plates or film, which are then used for board production.

The RT engineering terminal, which allows engineers to work directly on board designs, is based on International Business Machines Corp.'s Personal Computer. Summit has added extra memory and hardware for networking and a light pen to the Personal Computer as well as its own graphics language. The $29,000 RT terminal has a monochrome display with a resolution of 200 by 600 picture elements.

The CX-I option highlights Summit's overall concept of CAD systems, says Young. "Our total concept is to provide not only traditional CAD and design-automation tools, but to also provide a true network for not only schematic entry but also simulation," he explains. By bringing these tools together on a single network system, the company can offer pc-board designers many of the same capabilities that are currently available to IC designers.

Logic simulation, when it is ready, will use the RT engineering terminal. Programs will be downloaded from the central station to the RT terminal, and the latter will itself be able to simulate small subcircuits. For larger, more complex simulations, the RT terminal will access the 32-bit hardware at the central station.

In addition to the network and design-automation functions, the first-release CX-I option provides a numerical-control paper-tape reader and punch and a 45-in./s nine-track magnetic-tape drive for interfacing the Pathfinder with older systems.

The SX-II design station, which uses 8086 and 8085 microprocessors and either an Apple II or IBM Personal Computer as a keyboard, is slated to get a plotter-digitizer with a larger (36-by-48-in.) interactive area later this year. Other Pathfinder enhancements planned for this year include voice entry of commands and a photoplotter with a larger active area.

Summit CAD Corp., 5222 FM 1960 West 102, Houston, Texas 77069. Phone (713) 440-1468 [338]

Software

# Executive in ROM fits 8086, 68000

## Software components support interrupt-driven multitasking for 16-bit microprocessors

VRTX, an interrupt-driven real-time multitasking executive kernel (or nucleus), is well on its way to becoming processor-transparent at the 16-bit level. In other words, code that is written for multitasking applications in such high-level languages as C, Pascal, or PL/M and using VRTX system calls can run on 16-bit microprocessor-based systems using different central processing units: the move to a different CPU can be made without modifying the source code.

The version for Zilog's Z8002 was available first [*Electronics*, Oct. 20, 1981, p. 318]; a version is on the way for the 16000 from National Semiconductor; VRTX for Motorola's 68000 and the Intel 8086 is just now becoming available.

The 22 VRTX system calls perform task management, intertask communication and synchronization, interrupt servicing, and static or dynamic memory allocation. Real-time clocks and character-oriented input/output are also supported. Up to 256 separate tasks can be assigned unique priority levels.

Tasks can create other tasks; they can delete, suspend, resume, and change the priority of themselves or other tasks. If a real-time clock is present, VRTX system calls support task delays and round-robin scheduling. The system calls simply extend the architecture of the processor to perform these operations in real-time multitasking environments.

VRTX (for versatile real-time executive, pronounced vertex) represents the best example to date of what should be called software components, according to Hunter & Ready. Code in VRTX's 4-K bytes of programmable read-only memory makes no assumptions about the system in which it is to be used, except that the system must have at least 1-K byte of random-access memory. And VRTX is designed with "hooks" that support interfacing and extension without any need for code modification, considerably different from standard programs and operating sytems that cannot be adapted to changing system environments without expensive and risky tampering with the source code.

**Components.** The firm compares this concept of a software component with an Ada package, which is completely specified externally such that the user need never concern himself with its internal workings. Software components can be fully specified and listed in a catalog, just as are hardware components (see table).

The hooks that make it possible to interface VRTX with very different systems include its configuration table and the built-in potential for the definition by the user of up to 128 other system calls. Other operating systems do not give the system designer the option of adding his own system calls, interrupt handlers, device-initialization routines, or status-saving routines in a clean manner as does VRTX, and thus they cannot be extended without source-code modification.

The user-supplied configuration table is used to interface VRTX with its board environment. The table is a small block of code (as few as 14, 16, or 21 bytes for the Z8002, 8086, and 68000, respectively) specifying the locations of memory available to VRTX or for system, user, or task stacks and other parameters.

Access to VRTX varies with the microprocessor used. For the Z8002, access is through the execution of the SC instruction with various request codes. For the 8086, it is the INT 32 instruction followed by an identifying command byte. And for the 68000, the instruction used is TRAP 0 followed by an identifying command word. With those exceptions, the user can specify the entire interrupt structure for a system.

VRTX may be located anywhere in memory and does not interfere with the microprocessor's addressing features. For example, the status lines of the Z8002 and 68000 allow separation of four address spaces for various purposes; VRTX is compatible with boards that make the separation as well as boards that do not.

Hunter & Ready supplies interface libraries that allow VRTX system calls to be made from programs written in C, Pascal, or (for the 8086 only) PL/M. The firm also offers support software for programmable I/O chips and boards from original-equipment manufacturers.

A customer's first copy of VRTX is priced at $2,500, including licensing fees, documentation, and warranty. Thereafter, copies cost $595, $475 in quantities of 11 to 50, and under $100 in 1,000s. The firm intends to shift over a period of time from this software-like pricing to simple proprietary-component pricing. VRTX for the Z8002 is available immediately; shipments of the 8086 version are set to begin Feb. 15; and orders

PERFORMANCE OF VRTX MULTITASKING EXECUTIVE ON THREE 16-BIT MICROPROCESSORS*

| Function | Z8002 (μs) | 8086 (μs) | 68000 (μs) |
|---|---|---|---|
| Create task | 128 | 191 | 144 |
| Send message (with a task switch) | 129 | 173 | 143 |
| Send message (without task switch) | 53 | 111 | 59 |
| Receive message and wait | 110 | 133 | 130 |
| Receive message (with another message already waiting) | 32 | 66 | 38 |
| All functions: maximum time interrupts will be off (n = number of active tasks) | 13 + 6n | 16 + 8n | 14 + 7n |

*All figures assume a normalized clock rate of 8 MHz.

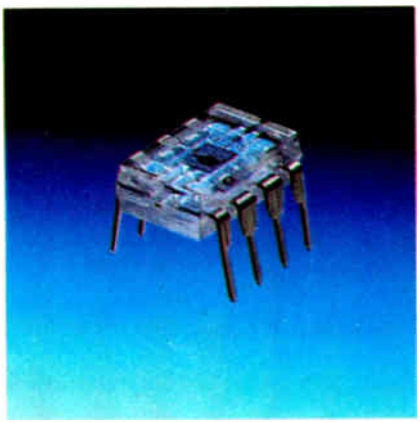
SOURCE: HUNTER & READY INC.

# Introducing the new TRW Optron Automatic Brightness Controller.

**It's the first time that ambient light sensing and automatic brightness control functions have been integrated on a single chip.**

Pulse width modulation is the key. The output duty cycle varies proportionately with the ambient light level so that the brightness of vacuum fluorescent, LED, incandescent and other types of displays and display drivers can be varied from 0% to 100%. An analog output, which varies linearly with ambient light, is provided for simultaneous or separate operation. Sensitivity can be adjusted externally and independent of ambient light.

Imagine the applications! Stereos, television displays and screens, test equipment, aircraft instrument displays, industrial light



levels, appliances, gasoline pumps, automobile dash displays... the list is virtually endless.

The new TRW Optron Automatic Brightness Controller (OPL100) is incredibly versatile. It can operate from supply voltages of 4.5V to 24V, and offers totem pole output to sink 20 mA or source 50 mA. And it will operate in synchronous or asynchronous modes. It is also available in a hermetically sealed TO-5 eight pin package (OPL105).

This technical innovation from TRW Optron means that for the first time with a single chip, you have the capability of precise automatic control over the brightness of your light source, independent of its non-linearities and sensitivity.

Let us tell you more. For a comprehensive data sheet and application note, ask for Product Bulletin 2091 and Application Bulletin 115. **Contact TRW Optron, 1201 Tappan Circle, Carrollton, Texas 75006, (214) 323-2200.**

**TRW OPTRON**

*An Electronic Components Division of TRW Inc.*

## New products

of the 68000 version will start to be shipped on March 15.
Hunter & Ready Inc., 445 Sherman Ave., Palo Alto, Calif. 94306. Phone (415) 326-2950 [371]

### Packages evaluate designs and do stress simulations

Extending the engineering and manufacturing graphics capabilities of IBM 4300 and 3081 computer systems, two computer-aided design programs provide three-dimensional and solid geometrical evaluation of conceptual design, as well as engineering modeling and analysis.

The first package, developed by Dassault Systèmes of Paris, is called Computer-graphics–Aided Three-dimensional Interactive Application, or Catia. It lets users construct 3-d objects like wire frames, complex surfaces, and solids on IBM 3250 graphics-display systems. In addition, users can view, manipulate, and analyze the images. The software also produces machining instructions automatically. The basic wire-frame geometry module can be licensed for $1,420 per month.

Structural Dynamics Research Corp., of Milford, Ohio, developed Computer-Aided Engineering Design Systems, or Caeds, for evaluating structural and mechanical designs. The system permits simulated stress evaluation of computer-generated prototypes through modeling and analysis. Caeds is available for an initial license charge of $3,275 and monthly charges of $865 per license and $55 per terminal.
International Business Machines Corp., Data Processing Division, 1133 Westchester Avenue, White Plains, N. Y. 10604. Phone (914) 696-1900 [373]

### Menus provide friendly interface with CP/M

Acting as a mediator between a user and any microcomputer under CP/M, the five-program Supervyz lets users communicate with the operating system in English. Using a sequence of easy-to-follow menus, it gives a series of choices that guides such tasks as word processing, accounting, and data verification. Responses are translated into instructions that CP/M recognizes.

Supervyz will work on any computer running the standard versions of Digital Research's CP/M 2.2, MP/M 1.1, or compatible derivatives. It needs a minimum of 32-K bytes of random-access memory.

One of its internal programs configures Supervyz to work with all of the most popular terminals and video boards. Also included are sample menus for the most commonly used word-processing and business software; users, however, can create their own custom menus.

Available now, Supervyz sells for $95. In early 1982, versions for Unix and CP/M-86–compatible systems will be available.
Epic Computer Corp., 7542 Trade St., San Diego, Calif. 92121. Phone (714) 695-3560 [374]

### Buffering system shortens CP/M-system run time

By buffering transfers to and from disk drives and by reducing the amount of disk activity, Cache/Q software increases the speed of CP/M systems by up to 35 times. It is transparent to all user and system programs, and no operating-procedure modifications are required.

It can be installed in a system under CP/M 2.2, requiring 64-K bytes of memory or less. Features included are an interactive installation program; a reconfiguration program, by which a user may specify which files or class of files are to be buffered; and a display program that provides the operating statistics.

The program is available now for CP/M 2.2 systems for $195. Versions for systems running under MP/M, CP/M-86, and MP/M-86 will follow.
Queue Computer Corp., 75 Pelican Way, Unit F, San Rafael, Calif. 94901. Phone (415) 457-6900 [375]

# "Old Reliable" introduces a new family of high-speed CMOS memories.

**RCA's three new 1Kx4 static RAMs offer high-speed from 0°C to 70°C, with industry standard pin-outs.**

These new RAMs give you TTL speed with CMOS benefits, at any temperature between 0° and 70°C.

They retain data on battery back-up voltage as low as 2V.

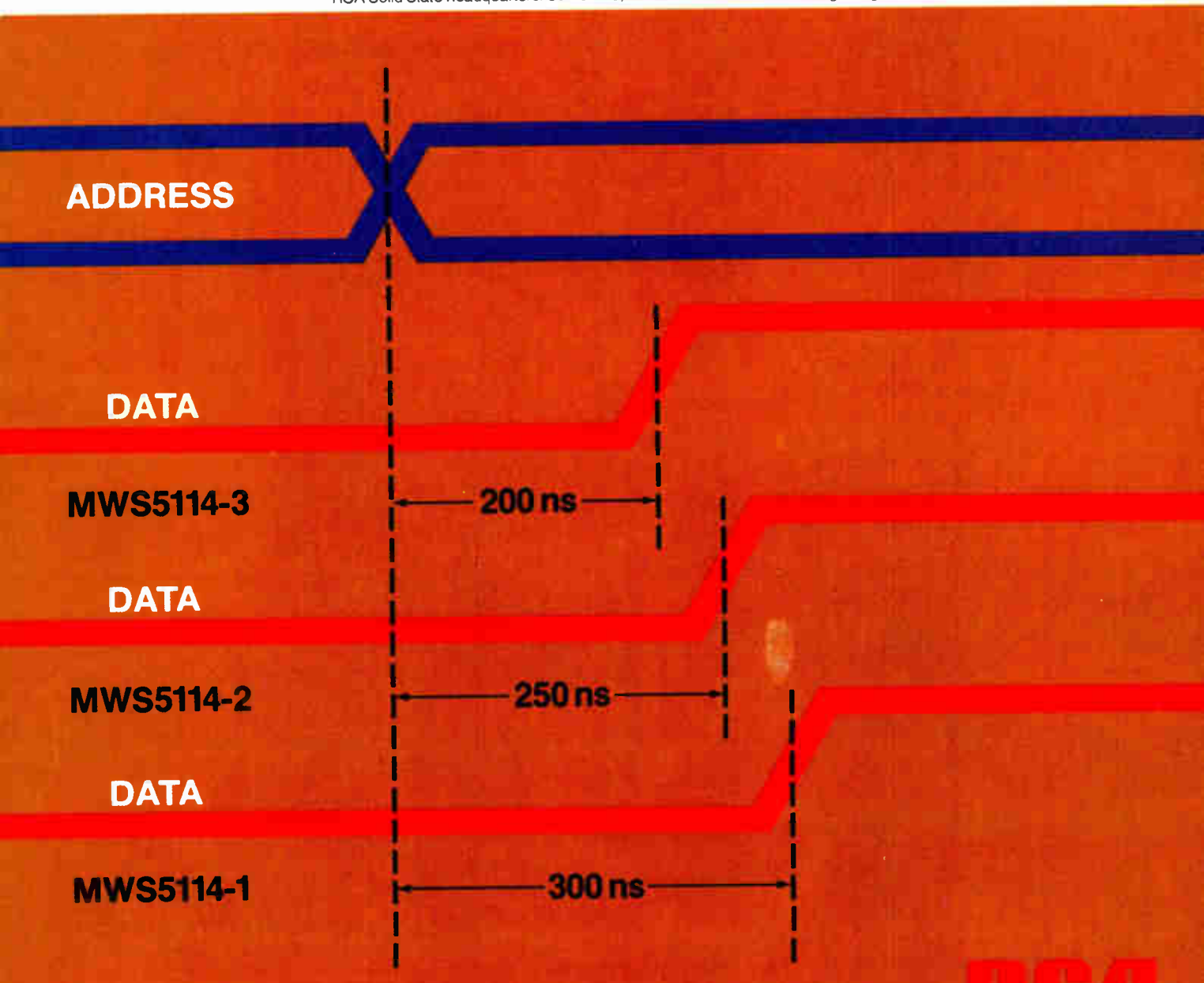
And all the inputs and outputs are directly TTL-compatible.

When used with high-speed microprocessors and peripherals (such as those in our 1800 series), these RAMs are ideal for applications that require low-cost power supplies or low-voltage standby power.

Best of all, these three new parts are available immediately in volume, in either plastic or ceramic packaging. And their price is as impressive as their performance.

For more information, contact any RCA Solid State sales office or appointed distributor.

RCA Solid State headquarters: Somerville, NJ. Brussels. Sao Paulo. Hong Kong.




Circle 137 on reader service card

Computer & peripherals

# Color helps spot trouble in CAD

## VLSI design system tints erroneously overlapped integrated-circuit elements

Its eye appeal is not the prime allure of a color graphics capability for the designer of very large-scale integrated circuits. On such a graphics display, an unusual color can flag the designer to warn him of errors, for there is enough complexity even in a partitioned design to make it all too easy to overlook an unintentional overlapping of metal and diffusion layers or the accidental joining of two pieces of circuitry. On a black and white display, these overlappings can very easily be missed in the maze of gray.

Aware of color's advantage here, Avera Corp. created its GS1220, a color graphics system intended for partitioned VLSI design. It employs a 13-in. monitor with a resolution of 488 by 668 picture elements. The graphics area on the monitor is 464 by 464 pixels, and the remainder of the screen is used to provide menu boxes, on-line reference guides, and an area for the user's responses. The entire screen display area is mapped by the video subsystem, and it is refreshed at the standard interlaced video rate of 30 Hz.

Among the features that the color version offers over its black and white predecessor [*Electronics*, April 7, 1981, p. 171] are two tables, each capable of holding eight basic colors that can be combined into a possible 256 different shades.

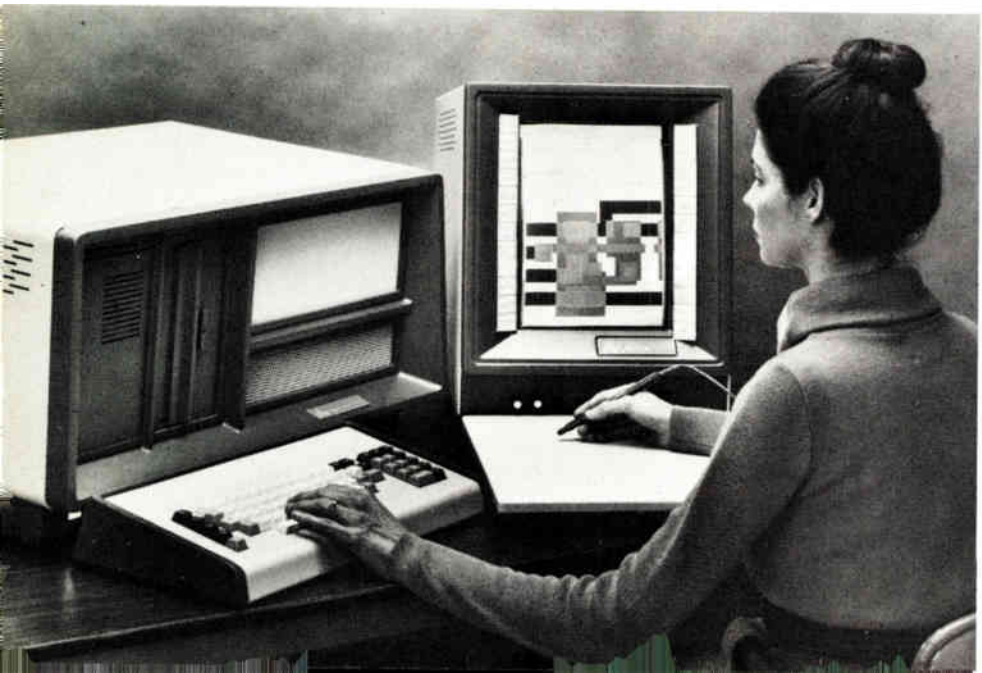
The user may treat each of the two color tables as representing a different function, such as pastel tints to lay out and bright colors to check the design. By making the tables different only in some hues, a blinking effect is produced when the display is switched back and forth between the two tables.

Unlike color systems that use software control to fill in areas, the GS1220 uses hardware control to fill in areas as fast as it outlines. The outline of an area can be either the same color as the fill, an intensified version of the fill color, or a different one. The intersection of two colors can be chosen to be any color in the palette, to make it easier to spot. Moreover, a layer can be assigned a dominant hue in order to shadow all other layers it overlaps. A unique feature of the system is that it can handle three layers of overlap as well as two, particularly useful when checking alignment.

The GS1220 also updates the system's two 8086 central processing units, using the 8-MHz versions of the microprocessor instead of the 5-MHz versions. Like its predecessor, the GS1220 contains a 10-megabyte 8-in. Winchester disk drive, 128-K bytes of random-access memory for each processor, two RS-232-C ports transmitting at up to 19.2 kb/s, and two 8-in. floppy-disk drives holding 500-K bytes each.

The addition of the color features to the Avera system comes at a premium of $8,000 above its black and white counterpart, with a standard GS1220 color system priced at $55,250. Delivery is in 30 days.

Avera Systems Corp., 200 Technology Circle, Scotts Valley, Calif. 95066. Phone (408) 438-1401 [361]



## Graphics system supports several printer-plotters

The HP 1360 graphics-system display can operate several mass-storage devices for program development and printer-plotters for making hard-copy printouts. It consists of a HP 9826A desktop computer, which controls functions like input/output, calculations, and information storage; the HP 1351A graphics generator, which receives picture data from the computer through a 16-bit parallel interface, stores it in its internal memory, and displays it on the HP 1311B cathode-ray tube; the HP 9111A graphics tablet, which allows the user to draw lines, pick elements for editing, and position text on the CRT display; and the HP 52113A Integral/60 interactive graphics library, which consists of three parts—a device handler, graphics functions, and a data base—and contains 81 Pascal procedures.

The 1360 system is priced at $14,750. The HP 9111A graphics tablet costs $2,050. Delivery takes 10 weeks.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [363]

## Computer work station adds printing to its capabilities

Three Rivers Computer Corp.'s single-user computer work stations now have the ability to print multiple-

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# FAST Delivery.

Until now, there were only 134 reasons to think FAST.™ 134 low-power, high-speed, defined functions. Including latches, buffers, flip-flops, counters, registers, multiplexers and LSI.

Now there's another reason. Delivery. FAST delivery. (Over 1/3 of the FAST logic family is already introduced and in stock. More of the 134 functions are being approved every month.)

The fact is, we've been going at a fast and furious pace for the last three years. Millions of units are being produced every month. And we're getting them off our shelves, and into the hands of our customers, at a fast clip.

If you've been thinking about upgrading your TTL system, think about upgrading the FAST way. Call or write us and we'll send you a working poster. A poster that includes a complete product listing, logic symbols, and pinouts of our 134 FAST designs. (And if you haven't already done it, don't forget to order our FAST evaluation kit.)

Whatever you do, just make sure you're on the FAST track. Fairchild Digital Division, 333 Western Avenue, South Portland, Maine 04106. Tel: (207) 775-8100. TWX: 710-221-1980.

**Digital**

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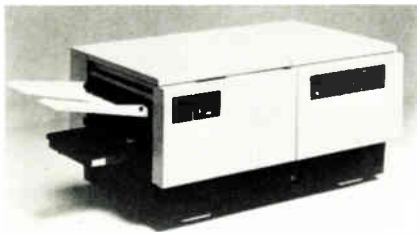


font text, lines, and halftones at a rate of 10 letter-size pages a minute on plain paper using the LBP-10 graphics printer.

The printer has a cassette capacity of 190 sheets a cassette and built-in self-diagnosing functions that tell the user where a problem can be located so that the defective module can be quickly replaced. It also includes such features as a solid-state laser, a polygonal mirror scanner, 240-dot/in. horizontal and vertical resolution, and an electrophotographic marking engine.

The unit meets with the laser performance standards published by the U. S. Department of Health and Human Services and the Underwriters Laboratories' UL-114 standard. Including simple text printing, screen-dumping software, cables, accessories, and a starter set of consumables, the LBP-10 graphics printer is priced at $15,000.

Three Rivers Computer Corp., 720 Gross St., Pittsburgh, Pa. 15224. Phone (412) 621-6250 [364]

## Copiers duplicate 5¼-in. diskettes for office use

Targeted for industrial, business, and personal users are two desktop 5¼-in. floppy-diskette copiers: the models 5208 and 5248. Both copiers can duplicate and verify single- and double-sided 5¼-in. diskettes in operator-selectable quantities from 1 to 999 and feature an automatic accept-reject output stacker.

The 5208 copier operates as a peripheral subsystem and is compatible with personal and business computers through an RS-232-C serial interface. The 5248 is a complete stand-alone system for both single- and double-sided formatted diskettes in single or double densities and can produce 68 single-sided copies/h, or 35 double-sided copies/h, of unformatted diskettes. It can be expanded by adding optional personality modules. Custom-designed personality modules are available on request.

Limited quantities of both copiers are scheduled for early 1982, with full production planned by midyear. Preliminary pricing in single-unit amounts is below $10,000 for the 5208 and approximately $13,000 for the 5248. Quantity discounts are available.

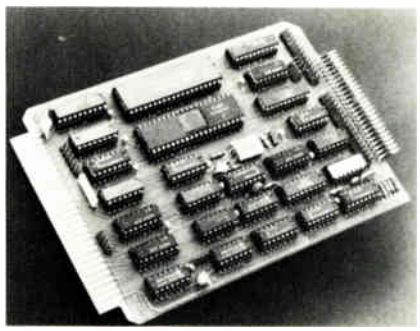
Media Systems Technology, 17991 Fitch Ave., Irvine, Calif. 92714. Phone (714) 752-6171 [365]

## Disk-drive controller allows changes in density and size

The ST4316 double-density floppy-disk controller, incorporating a Z80 microprocessor, is designed to operate within the STD BUS microsystem environment. It can support up to four IBM standard soft-sectored floppy-disk drives in any combination of 5¼- or 8-in. single- or double-sided disks, in single- or double-density mode, and mode-2 interrupt-structured software.

The unit is compatible with the 50-pin Shugart SA800/801 and 36-pin Shugart SA400/450 disk drives and the 26-pin Konan/Seagate hard-disk drive. Communication with a hard-disk controller can be had through 16 input/output lines.

Optionally available with the ST4316 is a software-support package that includes a CP/M 2. X operating system on 5¼- or 8-in. diskettes, input/output routines, and software utilities and documentation. Other user-selectable options include programmed I/O or direct-memory access, a single- or multiple-port hard-disk interface, and a choice of either 4- or 6-MHz system clock rates.



The controller sells for $345, and delivery is from stock to four weeks.

Applied Micro Technology Inc., P. O. Box 3042, Tucson, Ariz. 85702. Phone (602) 622-8605 [366]

## Portable terminal prints at 120 characters/s

The Execuport 4120 portable terminal with a 16-element columnar print head prints at a continuous speed of 120 characters/s. It comes with a 9-by-11-dot character font for printing standard and high-resolution characters at 10 characters/in. and a 5-by-7-dot font for producing compressed characters at 16¾ characters/in., which permits 136 characters/line to fit on standard 8¾-in.-wide paper. Also, true descenders permit printing below the line.

Used for cost-effective scientific and business applications and time-sharing, program development and maintenance, and remote access to large data bases, the 4120 operates with a choice of direct-connect or acoustically coupled modems. It can communicate at 1,200 b/s with built-in modems and at up to 9,600 b/s through an RS-232-C port.

The terminal's operating modes can be changed directly through keyboard instructions and its parameters can be set by a command key. Its nonvolatile memory allows the terminal's parameters to be reestablished each time the unit is powered up and maintained until new ones are selected.

The Execuport 4120 sells for $3,295 with quantity discounts available. It can be custom-designed with character sets for printing in Japanese (katakana), Arabic, Greek, and italic.

Computer Transceiver Systems Inc., P. O. Box 15, East 66 Midland Ave., Paramus, N. J. 07652. Phone (201) 251-6800 [367]

# For timeless architecture... the R6500/1.

## Build in Rockwell's proven microcomputer family. And build out business risks.

When you take advantage of the computer history lessons we've learned, you'll find you're managing your business risks better.

**Get off the instruction-set treadmill.**
At Rockwell, we think systems, not just devices. That's why we made the R6500/1 truly object-code compatible throughout the family, along with its well-established predecessors. And we've maintained architectural compatibility with our powerful new 16-bit microprocessor, the R68000.

**Get high performance through "less time" architecture.**
The real measure of data throughput is the time it takes to execute an instruction. That we deliver in 1 μsec at 4 MHz. While others push all the way up to 11 MHz trying, we haven't even begun to crank up the clock.

And you get this performance distilled onto one remarkable chip. One that offers the industry's smallest and fastest CPU. On-board RAM and ROM. Thirty-two I/O ports. And the most versatile counter/timer made to date. Plus the R6500/1 family offers virtually endless expansion opportunities with low-cost peripheral chips—the most complete family in the business.

**Minimize your costs and time-to-market.**
The real power of our 8- and 16-bit families lies in the fact that their efficiency and design capabilities are intended for your convenience, not ours. This makes them easy to learn and easy to use, allowing you to get your product to market faster—without destroying your investment in training and software.

Your investment in development support can be minimal, too. Let us show you how to utilize your current development system to design the R6500/1 into your product. Or, we can supply a complete set of economical support tools and application aids. Even applications engineers, if you need them.

**Build timeless reliability into your designs.**
Best of all, Rockwell's microprocessors have a history of high-volume, high-reliability use. That means the R6500/1 will be manufactured and delivered on time. And in the quantities you need.

So before you commit to a part for your next generation product, look at the only one that will endure the test of time: the R6500/1. Call Rockwell at (714) 632-3698. For complete technical literature, call (800) 854-8099, or (800) 422-4230 in California. In Europe, telex 0571/2650. In the Far East, telex J22198.

**Rockwell International**
...where science gets down to business

Circle 141 on reader service card

Semiconductors

# 8-bit multiplier responds in 60 ns

## Emitter-follower logic shrinks die of 8-by-8-bit part for high-speed processing

In the game of speed leapfrog being played by 8-bit multipliers from Advanced Micro Devices and Monolithic Memories, it is now MMI's turn to jump. Five years ago, MMI introduced the 67558-1, an 8-bit Cray multiplier that was intended for big systems. The 67558-1's 125-ns worst-case multiply time was later bettered, however, by AMD's pin-compatible Am25S558 [*Electronics*, Sept. 27, 1979, p. 196], which has a 75-ns response time. Now MMI has bounced back with the 74S558, a pin-compatible 8-bit multiplier with a 60-ns worst-case response time.

Like its predecessors, the 74S558 is a three-state part. It uses some emitter-follower logic internally, but most of the design is advanced Schottky logic. The 74S558 will normally be used with edge-triggered registers in such applications as super-minicomputers, radar, and sonar, and high-speed signal processing, array-processing, communications, real-time instrumentation, and fast Fourier transforms. A second device, the 74S557, is like the 74S558, except that three of its control lines were condensed to two through an encoding trick. The liberated line is used for output-latch control.

Because of this "extra" pin, encoding is different for the 74S557 and 74S558. The latch pin on the 74S557 allows the system to freeze whatever information is in the latch until it is opened again and keep the data available indefinitely at the multiplier's outputs. Both the 74S557 and 74S558 may be used to construct larger multipliers with 16-by-16-, 32-by-32-, or 64-by-64-bit configurations. Both multipliers may also implement the divide function by being used in an iterated-multiplication scheme.

MMI's previous offering, the 67558, employed a 32,400-mil² die, and AMD's 25S558 has an area of 28,215 mil². However, MMI's 74S558 is only 18,000 mil². This reduction is not due to a lithographic improvement—the parts are designed with an 8-μm pitch using 4-μm lines and 4-μm spaces. It is the result of using EFL technology, which tends to make a design more compact. The reduced die size and the speed of EFL contribute to the parts' performance: each requires only 30 ns to enter or exit one of the three states.

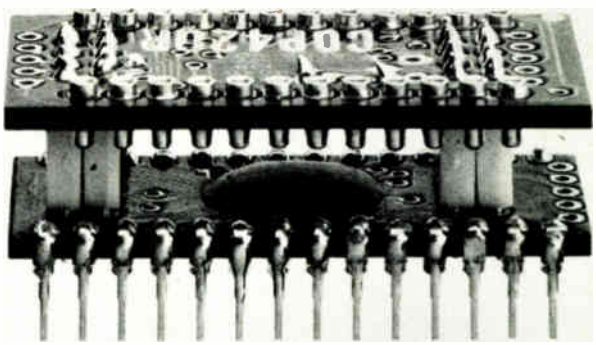
This technology, however, does not use inverted signals, which points up another difference between the MMI and AMD designs. For inverted signals, the MMI response specification slips by 5 ns to a worst case of 65 ns, whereas the AMD design remains the same with 75 ns for the 25S558 and 80 ns for the 25S557. That is because AMD's parts use emitter-coupled logic internally, which handles direct and inverted signals equally well. For the military temperature range of −55° (ambient) to +125°C (case temperature), the MMI time slows 10 ns for either part.

The pricing of the 74S557 and 74S558 is expected to be under $100 each in production quantities of 1,000 or more, with first deliveries expected in April.

Monolithic Memories Inc., 1165 East Arques Ave., Sunnyvale, Calif. 94806. Phone (408) 739-3535 [411]

# E-PROM plugs in above controller

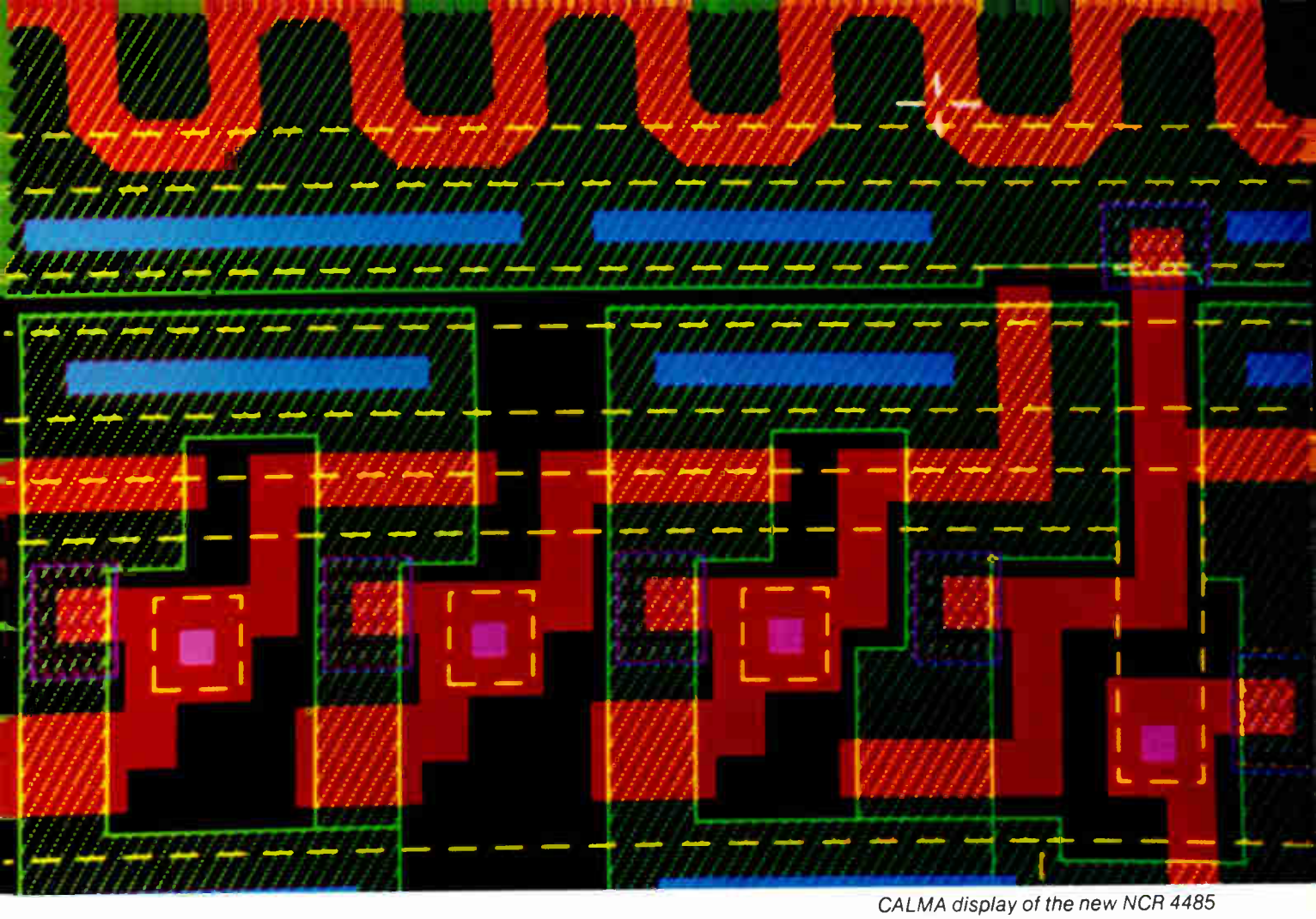
## Standard E-PROMs stand in for on-chip instruction ROM of control microcomputers



National Semiconductor is supporting prototype work with its COPS line of microcontrollers, adding two models that allow erasable programmable read-only memories such as the 2716 or 2758 to ride piggyback above the controller. The E-PROM stands in for the on-chip ROM of the standard microcontrollers, allowing the user to field-test a control system in its final electrical and mechanical configuration before ordering mask-programmed controller chips.

The new devices, designated COP42OR and COP444LR, are functionally equivalent to their mask-programmed counterparts. Aimed at control of remote data-acquisition systems, instrumentation, and industrial applications, both single-supply parts are hardware- and software-compatible with other members of the COPS family of control-oriented processors. Each has on-chip random-access memory, provision for vectored interrupts, drivers for 23 input/output lines, and an internal timer.

The 420R has 64 4-bit RAM words on chip and can access 1,024 instruc-



*CALMA display of the new NCR 4485*

# Now you can draw on NCR's experience for the highest density, n-channel NV-RAM available.

NCR's newly patented SNOS (Silicon Nitride Oxide Silicon) process brings you the NCR 4485 — the highest density, microprocessor compatible NV-RAM available. Its 512x8 bit organization gives you 512 bytes of RAM and 512 bytes of EEPROM. All on the same chip.

With the NCR 4485, you get TTL compatibility, JEDEC standard byte-wide pinout, and a 450 ns worse case access time.

Plus, the NCR 4485 is available right now. So there's no need to wait for the combined advantages of EEPROM non-volatility and fast static RAM alterability.

The NCR 4485 is just the first member of a new n-channel family using SNOS. A family whose MNOS heritage ensures high quality and reliability. And because we're in the business to stay, you can look forward to even higher densities from NCR.

You can test the NCR 4485 for yourself with our new evaluation kit. It includes: 5-NV-RAMS, data sheet, application report, reliability report, and erase/store voltage generation/control parts. All for only $200.

For more information, call Dave Major at (800) 543-5618, in Ohio (513) 866-7217. Or write Dave at NCR Microelectronics Division, Box 606, Dayton, Ohio 45401.

**NCR — NV MEMORY GUIDE**

| Device No | Organization | Type |
|---|---|---|
| 2051 | 32x16 | WAROM |
| 2055 | 64x8 | WAROM |
| 7033 | 21x16 | WAROM |
| 1400 | 100x14 | WAROM |
| 3400 | 1024x4 | WAROM |
| 2811 | 2048x4 | EAROM |
| 2168* | 2048x8 | EAROM |
| 2161* | 2048x8 | WAROM |
| 4485 | 512x8 | NVRAM |

*Pin conservative bus structured devices

MNOS p-channel description
WAROM — Word alterable ROM
EAROM — Electrically alterable ROM

NCR
Microelectronics Division

tion bytes from the E-PROM, executing each one in 4 μs. The 444LR is a low-power processor with 128 4-bit words of RAM and can address up to 2,048 bytes of E-PROM code; its instruction-execution time is 16 μs. Its package houses a voltage regulator that permits it to operate with supply potentials of up to 9.5 V. To interface with the E-PROM, each unit has an address-latch chip mounted on the underside of the upper layer of the two-tiered packages used for the piggyback design.

In addition to prototype work, the E-PROM approach is likely to be cost-effective where total volume of parts is low, or where the programming may be required to change from one unit to the next. Both of the new controllers can be used with COPS peripherals, including analog-to-digital converters, display drivers, timers, and standby memory.

In lots of 100, the COP42OR sells for $37 and the COP444LR goes for $46. Delivery is from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [412]

## 4-K ECL RAM series reaches 15-ns access time at 180 mA

Three additions to the DM104X family of emitter-coupled-logic random-access memories provide expansion capabilities through wired-OR compatibility. Each of the 4-K-by-1-bit RAMs has a chip-select input and open emitter-follower outputs that allow the user to tie two or more outputs together to achieve the logical-OR function of the output data.

The standard DM10470 has a maximum access time of 25 ns at 180 mA; while the high-speed version of this RAM, the DM10470A, has a maximum access time of 15 ns at the same power consumption. A low-power model, the DM10470L, has a maximum access time of 25 ns at 135 mA.

All the devices are voltage-compensated and fully compatible with 10,000-series ECL and feature separate data-in and -out pins. The memories are manufactured in Oxiss III, National Semiconductor's oxide-isolated process. Oxiss III makes use of conventional photolithograpic equipment and well-established process technology.

Sample quantities are available now, with production quantities available in the spring. In lots of 100 or more, the DM10470 is priced at $30 each, and the DM10470L sells for $39.85 each. The fast device goes for $55.80 each.

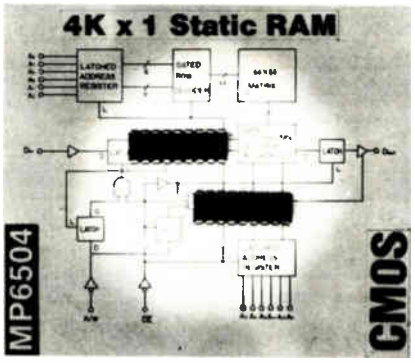
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [414]

## Static 4-K C-MOS memory draws 1 μA on standby

Serving as a pin-for-pin replacement of the Harris HM6504 random-access memory, the MP6504 4-K-by-1-bit complementary-MOS static RAM boasts a 1-μA standby power consumption. In the idle or non-switching state, it consumes only 40 μA maximum. The low-power values are credited to the use of a high-density silicon-gate process.

The chip has a 250-ns access time and TTL-compatible inputs and outputs. A three-state output and on-chip address registers allow the device to interface with microprocessor-based designs.

The MP6504 is suitable for non-volatile storage with battery backup. The device is powered from a single +5-V supply, but data is retained even when power drops to 2 V. The maximum voltage of 7 V permits the use of four 1.5-V batteries in portable applications.




The 100-piece price for the device in an 18-pin plastic dual in-line package is $6.25 each. Cerdip and ceramic packages are also available. Delivery takes 60 days after receipt of order.

Micro Power Systems, 3100 Alfred St., Santa Clara, Calif. 95050. Phone (408) 247-5350 [415]

## C-MOS gate arrays consume 0.2 nA/gate

With a 0.2-nA/gate power consumption and a typical gate propagation delay of 5 ns at 5 V, the NC9000 series of semicustom complementary-MOS gate arrays can be applied in high-speed, low-power applications currently using Schottky TTL devices. The six-member family, offering from 360 to 1,500 gates, has a maximum low-state noise immunity of 1.5 V, a minimum high-state noise immunity of 3.5 V, and a +3-to-+10-V supply range.

Prototypes supplied for evaluation usually take 8 to 12 weeks. Screening for military and high-reliability specifications is also available. The devices are offered in plastic, cerdip, and ceramic dual in-line packages, as well as in special packages.

In lots of 50,000, a typical price for the NC9360 with 360 gates replacing up to 20 TTL devices will be between $4 and $5. There is also an engineering fee ranging from $15,000 to $20,000.

Nitron, 10402 Bubb Rd., Cupertino, Calif. 95014. Phone (408) 255-7550 [416]

## N- and p-channel MOSFETs switch on in under 5 ns

A vertical double-diffused MOS process and compact interdigitated geometries give a new n- and p-channel series of power MOS field-effect transistors an input capacitance of less than 30 pF, a turn-on time of less than 5 ns, and an under 7-ns turn-off time.

Both the ZVN13 and ZVP13 series consist of eight devices, with

ratings ranging from 40 to 200 V and maximum drain currents up to 1.5 A. Each comes in TO-39, TO-92, and 14-pin dual in-line packages.

The devices can be paralleled without base current-sharing resistors, and they do not fail due to thermal runaway or thermally induced secondary breakdown. They are suitable for microprocessor and integrated-logic interface driving, sensing and timing circuits, and general-purpose switching.

Pricing for 100-unit lots begins at 60¢ each for the n-channel devices and 75¢ for the p-channel versions. Delivery takes up to 10 weeks, depending on rating and package.

Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N. Y. 11725. Phone (516) 543-0200 [417]

## Video-display generator features katakana subset

Offering a frequency range up to 20 MHz, the SND8002, a cathode-ray-tube video-display generator and attributes converter, features four modes of character and graphics operation. The internal character generator is offered with a choice of a 5-by-7- or 7-by-9-dot ASCII character set or a 5-by-7-dot katakana Japanese subset.

Wide and thin graphics comprise the second and third modes. The internal read-only-memory character set and graphics modes can be extended by use of an external ROM, programmable ROM, or random-access memory housing additional symbols.

The device's attributes, available in all modes, include reverse video, character blanking, two programmable blinking rates, strike-through, and underlining. The SND8002 is available in both plastic and cerdip 28-pin packages. It needs one 5-V supply and operates from 0° to 70°C.

In 1,000-piece quantities, the plastic model sells for $13.50 each, and the cerdip version goes for $15.65 each. Delivery is from stock.

Solid State Scientific Inc., Montgomeryville, Pa. 18936. Phone (215) 855-8400 [418]

Communications

# Codec with filter needs only 16 pins

C-MOS chip for the U. S. or European markets needs no external parts

Perhaps 16 is the winning number for pinouts when it comes to single-chip coder-decoder and filter devices aimed at the telecommunications switching industry—after all, Motorola Inc.'s telecommunications circuit designers spent 2½ years of work and filed nine patents on the 16-pin MC14403 codec-and-filter "monocircuit," which went into volume production this month [*Electronics*, Jan. 13, p. 33].

The monocircuit requires no additional external components like capacitors or resistors. The part is available now for delivery and comes in two versions: the 14403L1 for Europe and other markets using the standards of the International Consultative Committee on Telegraphy and Telephony (CCITT), at a price of $27.25 each in quantities of 100, and the 14403L2 for D3-D4 markets—the U. S.—at a price of $23.36.

**Prescaler.** One example of the patented pin-saving circuitry is the device's automatic dividing prescaler, which allows it to establish its own internal master-clock frequency from any one of four standard system frequencies: 1.536, 1.544, 2.048, or 2.56 MHz. This function eliminates the need for external pins to select a master-clock frequency. Once the system frequency enters the chip, the device automatically divides to get its own 128-kHz clock.

Another innovation is the chip's use of the same digital-to-analog converter to accomplish both d-a and analog-to-digital conversion. According to Robert Karasch, telecommunications product manager for Motorola in Austin, Texas, this feature offers a 15% to 20% reduction in the die size, to just 36,000 mil².

Both L1 and L2 versions of the 14403 are made from the same mask, says Karasch. However, each is tested by Motorola to meet either CCITT or U. S. specifications. The part uses a pin to select the operating mode, so Motorola can quickly ramp to production volumes and pass on benefits in cost and reliability to customers, he notes.

**Remote applications.** The chip is made with Motorola's silicon-gate complementary-MOS process and has a low power-consumption rating of 60 mW at 2.048 MHz in the active mode and 2 mW in the power-down (on-hook) mode. "It was designed with remote applications in mind," says Karasch, referring to use of the codec-and-filter chip in the telephone itself. "But I think anybody who has a part must be looking at this, because that's where the systems are going," he continues.

Motorola's codec-and-filter chip, which has TTL- and C-MOS–compatible inputs, also has an on-board precision 3.1-V reference that eliminates the additional costs of external references. The 14403's reference is able to meet the device's tight specifications without laser trimming, says Karasch, alluding to another patented process.

Motorola believes the chip's standard 16-pin package will attract telecommunications system manufacturers, who are constantly battling space problems in new designs as well as when enhancing existing equipment. A leadless chip-carrier package will be available for the device later this year.

The telecommunications equipment makers "might want to add features to their board, for example, in order to add features to the line circuit. But where are they going to get that space?" asks Karasch, who estimates that the total available codec-and-filter market will be $150 million to $175 million in 1985. "The logical place would be replacing the individual filters and codec with a single 16-pin monocircuit."

In March, Motorola plans to introduce three fully synchronous members to the codec-and-filter line: the 14400, 14401, and 14402. Mostek Corp. of Carrollton, Texas, which has agreed to second-source the 14403, says it expects to go into production of the devices later this year. In turn, Motorola has agreed to second-source Mostek's C-MOS codec-and-filter device after its introduction in the next quarter.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6985 [401]

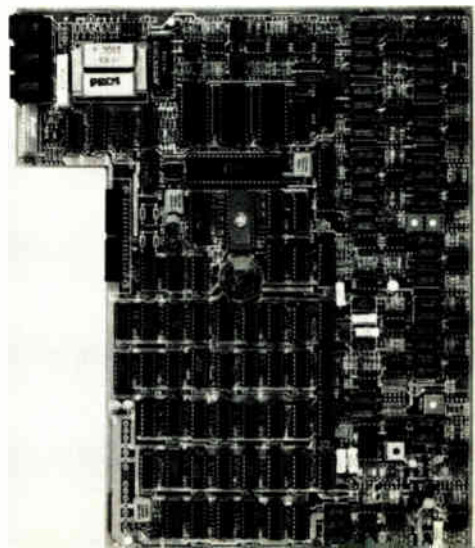
# Smart modem fits inside terminal

Direct-connect board stores numbers, automatically redials or tries others if line is busy

A Bell 212A–compatible modem board, the TS-1-212 Plus, which occupies a single card slot in a Falco TS-1 terminal, includes an integral telephone dialer and a number of automatic features.

Approved by the Federal Communications Commission for direct connection, the TS-1-212 Plus automatically dials telephone numbers stored by an operator in the modem's memory. Five numbers of up to 30 digits each can be stored in the unit's battery-backed memory.

Numbers can be linked so that if the first one dialed is busy, an alternative will be dialed automatically.



Any that are not stored can be dialed from the terminal keyboard, from which dual-tone or pulse-type dialing may also be specified.

**Help.** A built-in help function can be activated to display stored numbers or operating instructions. Such features as redialing the last number, redialing numbers until a connection is reached, and displaying messages like "no answer," "busy," or "on line" are included with the TS-1-212 Plus. A pause character can be inserted within a number when a waiting period for a second dial tone is necessary.

Both analog and digital testing can be controlled through rear-panel switches. With the modem idle, it can perform a high-speed analog-loopback self-test. Another rear-panel switch closes the line-control relay to provide a busy signal when the unit is in the analog-loopback mode. When activated, the remote modem automatically enters the digital-loopback mode to facilitate testing the modem of a remote station.

The TS-1-212 Plus is compatible with both Bell 212A and 100 series modems and provides full-duplex operation at 300 or 1,200 b/s over the two-wire switched network. The Z80-based software-driven TS-1 [*Electronics*, Nov. 17, 1981, p. 190] features a "terminal nest," designed for easy insertion and removal of read-only memories and printed-circuit boards for upgrading and enhancing the terminal; the 12-by-8-in. modem board is the first such enhancement.

The +5-, +12-, and −12-v operating currents needed are supplied by the terminal. The $995 modem can be delivered 30 to 45 days after receipt of order.

Falco Data Products Inc., 1286 Lawrence Station Rd., Sunnyvale, Calif. 94086. Phone (408) 745-7123 [401]

## Coupler communicates in Bell 212 mode

Performing a feat previously thought impossible, the AJ 1233 acoustic coupler communicates with a Bell 212 modem, overcoming data errors caused by harmonic distortion. In addition to communicating with Bell 212, Racal Vadic's VA 3400, and Anderson Jacobson's AJ 1200 series modems, the AJ 1233 communicates in the Bell 103/113 mode.

The AJ 1233, an originate-only full-duplex acoustic-coupler modem, can select by switch either synchronous or asynchronous communications, at data rates of 1,200 b/s and asynchronous rates of 0 to 450 b/s. It may be used in all modes as either an acoustic coupler or a modem directly connected to the switched network by a modular RJ-11C jack.

For Bell 212 communications, a digitally synthesized signal is inserted into the transmitted signal. This is accomplished through a patented technique that linearizes the response of the carbon microphone in the telephone handset.

Used as a Bell 103 modem, the microprocessor-controlled AJ 1233 allows its operator to communicate with a computer for interactive time-sharing or for data entry. To do this, the unit chooses the most economical line speed through either directly dialed or operator-assisted calls. Scheduled to be available in March, the AJ 1233 will sell for $995 in single units.

Anderson Jacobson Inc., 521 Charcot Ave., San Jose, Calif. 95131. Phone (408) 286-7960 [403]

## Gigahertz link sends video signal over 1.5 miles

Transmitting and receiving one way on one of eight uncluttered gigahertz frequencies at distances up to 1.5 miles, the Gemlink LSV-112A, a link with a superheterodyne receiver for video transmission, is well-suited to the surveillance and monitoring needs of banks, airports, toll booths, and industrial sites. The frequencies include 21.825, 21.875, 21.925, and 21.975 GHz as well as 23.025, 23.075, 23.125, and 23.175 GHz. Up to four systems may be simultaneously operated over the same path.

In addition to a transmitter and receiver unit, the Gemlink system requires a closed-circuit television camera and a video monitor. Its microwave source is a solid-state Gunn-diode oscillator that uses little power and presents no radiation-caused health hazards.

The output from the receiver [*Electronics*, Jan. 13, p. 167] is designed to recreate the same composite video signals given the transmitter. The link output works with a similarly specified monitor input impedance. The specifications are compatible

with both domestic and foreign closed-circuit TV components.

The Gemlink local-loop system can replace dedicated lines, lasers, coaxial cable, infrared, and conventional microwave systems. Because it needs no cable, it eliminates right-of-way complications and overcomes natural and man-made obstacles like rivers, lakes, canyons, and expressways. The unit, in a weather-resistant housing, operates outdoors on a line of sight.

The Gemlink LSV-112A microwave video system sells for $4,950.

General Electric Co., P. O. Box 3900, Peoria, Ill. 61614. Phone (800) 447-4700 [402]

## Local-network data link frees host for other tasks

Freeing the host computer for other tasks, a local-network data link called Microlink offloads link and network software from the host to the coprocessor, an Intel 8086. The controlling software is embedded in a multilayered programmable read-only memory.

Each Microlink unit employs di-

rect memory access between the data link and its associated 8086 coprocessor central processing unit and between the coprocessor and the host CPU.

Microlink permits an LSI-11 or PDP-11 computer to communicate by means of the High-level Data-Link Control protocol to as many as 255 other stations at distances up to 30,000 ft. Transmission is at 1 Mb/s down a multidrop line such as a coaxial cable.

Software programs for the link interface, networking, transport layer, and HDLC are included, as well as X.25 compatibility and expandable memory. An RS-422 interface consisting of a shielded twisted wire pair and also a synchronous modem are available as options. With a delivery time of 90 days, Microlink sells for $2,995.

Standard Engineering Corp., 44800 Industrial Dr., Fremont, Calif. 94538. Phone (415) 657-7562 [404]

### Teleconferencing system sends still color pictures in 5 s

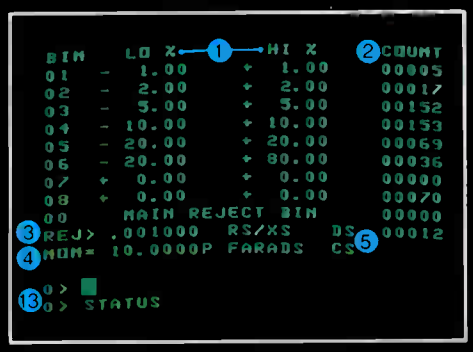
Reduced travel and increased productivity may be the upshot of a video teleconferencing system for transmitting color still pictures over conventional telephone circuits.

The model TVS-783's transceiver is fed a standard color video signal originating from cameras placed in a conference area to photograph people as well as display areas, document stands, and chalk boards. Single cameras with remote pan-tilt heads and zoom lenses are used to cover several areas within the room.

The TVS-783 captures one still picture from the incoming video signal, digitizes it, and stores it in buffer memory. This stored data is analyzed, compressed, and fed through an RS-232-C port into an external modem, which converts the data into analog tones and sends it through either standard voice or data-grade telephone lines to the receiving end.

The data passes through a receiving modem, is converted from analog into serial digital form, and enters


# LRC test and evaluation.




1. High & Low Sorting Limits
2. Parts Count Per Bin
3. Loss Reject Limit
4. Nominal Value
5. Measurement Functions
6. Programmable Test Frequency
7. Programmable Test Voltage
8. Measurement Modes
9. Settling & Integration Time
10. No. of Measurements for Averaging
11. Capacitance Measurement
12. Dissipation Factor
13. Communication Lines


# Now you get the full picture ...at LED prices.

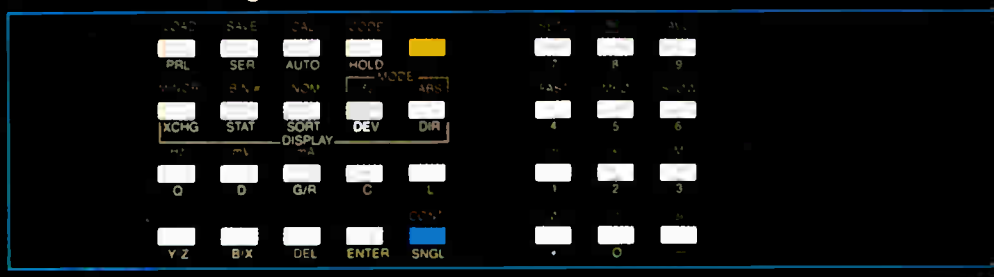
Get the complete view of your LRC measurements with the new 2100 and 2110 VideoBridges from ESI. They're the first LRC meters to combine effective software, memory, a CRT and keyboard, to give you interactive operation... with a price comparable to LRC meters with only LED readout.

Both VideoBridges will display 12 impedance and loss characteristics, measureable at test frequencies from 20 Hz to 20 kHz, at programmable voltage or current levels, with accuracy from 0.05%.

With the 2110 VideoBridge, you can program your test conditions on cassette, acquire the data, store it, and manage and display your test results. You can store test programs for different components, for repetitive testing needs.

Find out how our VideoBridges can fill your impedance measuring requirements, both today and tomorrow. Call your nearest ESI representative or circle the reader service number below.

**ESI VideoBridges.™ You can communicate with them.**

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Circle 149 on reader service card

## New products

the TVS terminal at the receiving site. In the TVS-783, the digital data is reconstructed in memory and is then read out onto a standard color television monitor in the form of a still picture.

With a dial-up voice-grade interconnection running at 4.8 kb/s, it takes about 90 s to send an image; at 56 kb/s, the time can be as short as 5 to 8 s. The TVS-783 transceiver is priced at under $15,000.

NEC America Inc., Broadcast Equipment Division, 130 Martin La., Elk Grove Village, Ill. 60007. Phone (312) 640-3792 [405]

### Fiber-optic system carries digital data at 100 Mb/s

Featuring an automatic threshold-control processor, the 5330 fiber-optic system operates at nonreturn-to-zero data rates of up to 100 Mb/s. The 5330 system, consisting of a 5330T fiber-optic transmitter and a 5330R receiver, is dc-coupled from transmitter logic input to received data output. The automatic threshold-control processor continually monitors the receiver output level and optimizes the discriminator threshold.

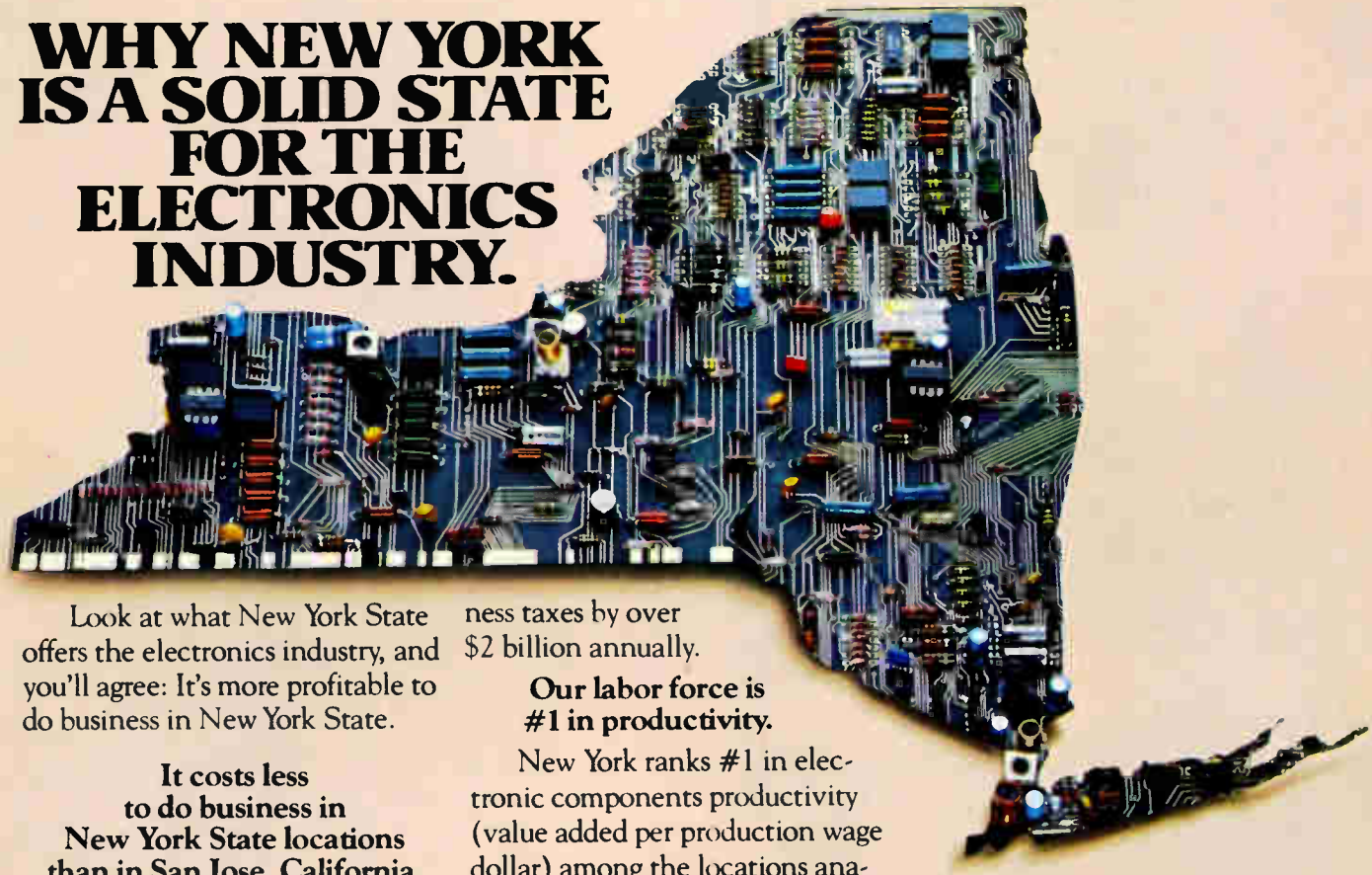
An infinite-hold memory circuit within the ATC processor is updated only if peak received power changes by 20 dB. With its combination of dc coupling and automatic threshold control, the 5330 system is able to be completely independent of the transmitted data pattern or data rate.

The 5330 system has data inputs and outputs compatible with emitter-coupled-logic needs. It operates at 820 nm and may be used with a fiber of a 100-$\mu$m or 200-$\mu$m diameter. A link 300 meters long is possible with 200-$\mu$m fiber.

The design of the transmitter and receiver modules allows dense front-panel or printed-circuit-card mounting; connections are made via an Amphenol model 905 fiber-optic or a standard 0.1-in. edge connector. The 5330 is priced at $695 and is available in 12 weeks.

LeCroy Research Systems Corp., 700 South Main St., Spring Valley, N. Y. 10977. [406]

# WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



Look at what New York State offers the electronics industry, and you'll agree: It's more profitable to do business in New York State.

**It costs less to do business in New York State locations than in San Jose, California. And we can prove it.**

An independent study analyzed the four critical costs of taxes, wages, power and construction for a model new electronics firm. It showed that New York State offers locations where these costs are less than they are for choice electronics industry locations around the country.

For example, these costs would total $7.6 million annually in San Jose, versus only $6.4 million in, say, Brookhaven, New York.

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- ☐ Small Computers
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Circle 151 on reader service card

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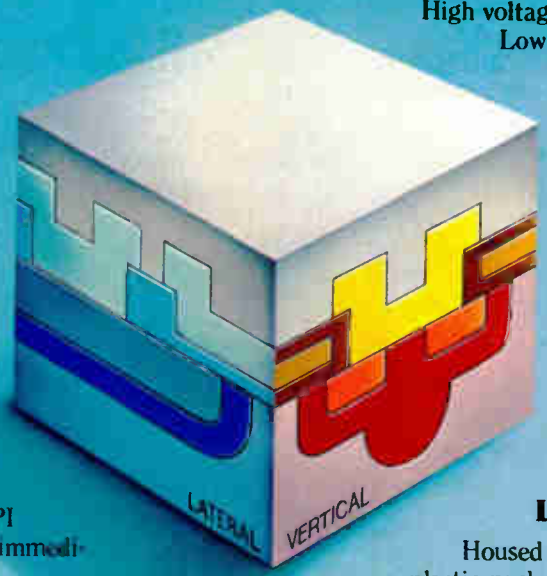


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Circle 152 on reader service card

# Products Newsletter

## Dual tunable filter aims at speech circuits

Looking to deepen its speech markets, Motorola's telecommunications operation in Austin, Texas, is unveiling a dual tunable low-pass sample data filter that provides band limiting and signal restoration over 1 to 10 kHz. Made using a metal-gate complementary-MOS process, the **MC145414 has two fifth-order elliptic low-pass filters and two uncommitted operational amplifiers,** which can be used for gain adjustment.

In addition to speech applications, penny arcade games, which use filters for sounds, may use the chip. The device is useful in applications of linear predictive coding and continuously variable-slope delta modulation. The part has a dynamic range better than 80 dB, a passband ripple less than 0.3 dB, and idle noise typically −100 dBrnC0. It also has typical power dissipation of 30 mW when active and 1 mW when in the power-down mode. In orders of 1,000, the unit price is $4.50.

## CAD makers have design on price

Believing a favorable worldwide demand exists for computer-aided–design systems, **Racal-Redac Inc. reduced its Cadet printed-circuit-board design system to a competitive $29,000.** The Littleton, Mass., supplier of turnkey CAD systems has designed Cadet for the manual circuit-board designer.

Meanwhile, Gerber Scientific Instrument Co., Hartford, Conn., has cut the price of its model 41 photo plotter by 35% to $39,000. Used alone or with Gerber's PC-800 board CAD system, the 41 produces master artwork.

## Software splices CAD/CAM systems

Data-base conversion software from Octal Inc. of Mountain View, Calif., translates computer-aided–design and –manufacturing drawings in Calma GDS1-LU into Applicon AGS/860, or drawings in AGS/860 into Calma GDS2. The programs, now running on a Digital Equipment Corp. VAX computer, **log any design limitations violated in the conversion process** and let users choose how components will be represented.

## Bipolar controller cycles in 200 ns

After a year in which its bipolar 8X300 microcontroller was designed into more than 100 systems, Signetics' Bipolar LSI division, Sunnyvale, Calif., is introducing a faster version, the 8X305. The 305's instruction-cycle time is 200 ns, compared with the 300's 250-ns cycle. **The 305 also has gained another seven registers** and executes an improved instruction set.

Other upgraded parts announced by the division include the 8X320 two-port random-access memory for 8- or 16-bit bus or mailbox interfacing and the 8X330 "companion processor" for floppy-disk control, which can transfer data at 1 Mb/s. Peripherals are being also added to the family: an interrupt controller, synchronous and asynchronous addressable input/output ports, and a 9-bit port, among others.

## 8-bit shift register has three-state latch

The CD4094B complementary-MOS 8-bit shift register from National Semiconductor, Santa Clara, Calif., has a three-state latch that holds all 8 bits until an unlatch signal is received. **A separate output from the last stage allows them to be cascaded, creating much larger registers.** The device's worst-case power dissipation is 25 μW, compared with 135 mW for TTL units. In plastic and ceramic 16-pin dual in-line packages, each device sells for $2.13 and $2.39, respectively, in lots of 100. A military version that meets Jedec B specifications for C-MOS circuits sells for $2.55 in like quantities.

# Career outlook

## Pension rule fogs picture

The subject of pensions has always been a volatile one for the electronics engineer. Engaged in a profession that sometimes rewards the more mobile of its members but at other times seems to penalize those who have reached their forties and fifties, many individual EEs have agonized over job changes that would lose them to their pension equity. Now they also face a group threat to the retirement nest egg.

It comes in the form of a new accounting rule, FAS-36, promulgated by the Financial Accounting Standards Board. So far, what the rule has done is cause a serious controversy over the actual status of pension funding. A 75-page study just released by Johnson & Higgins, a New York employee-benefit consulting firm, emphasizes that pension plans in the electronics and appliance industries would for the most part be able to pay promised benefits should the plans be terminated today. However, the new rule makes it difficult to assess the ability of plans to pay future benefits.

In short, the report goes on to say, FAS-36 "has led to confusion" about the specific status of pension funding by tending to inflate the value of the different plans' assets.

FAS-36 went into effect when companies issued their 1980 annual reports. Although accounting rules can be complicated, this new one, stated simply, changes pension-reporting requirements. The change can be seen most clearly in the case of the ratio of net assets to the value of accumulated vested benefits.

In 1979 annual reports, before FAS-36 came into force, only about a quarter of the industrial companies reported net assets that were equal to or greater than their accumulated vested benefits, reports Johnson & Higgins. However, with the new rule in place, more than half of the companies reported net assets equal to or greater than the value of accumulated vested benefits.

The new method of reporting, however, is based on the average salary at age 30 and thus manages to exaggerate the seeming worth of pension funds by ignoring the greater claims of those who earn more. Or, to quote Kenneth K. Keene, who is senior vice president of Johnson & Higgins, "One difficulty with FAS-36 arises from the fact that the new rule does not take into consideration future salary increases. Thus, future pension-plan obligations may be understated."

However, the study is reassuring on at least one point. It says that pension plans covering almost 2 million workers in 36 of the Fortune 500 companies that are in the electronics and appliance field "are generally as financially healthy as they have been in the recent past."

Johnson & Higgins found that in 1980 the electronics-appliance group averaged expenditures of $62.5 million a company, or $1,155 for each employee, to maintain pension plans. In 1979, the figures were $57.7 million for each company and $1,063 each employee. On the other hand, pension cost as a percentage of pretax profits for the group in 1980 dipped to 17.8% compared with 18.7% for the preceding year.

**In step.** These figures compare favorably with those for the average Fortune 500 firm, according to the study's statistics. Each of these industrial companies averaged $46 million or $1,329 per employee in 1980, while the average nonindustrial firm spent $40 million or $1,279 per person. The total in 1980 to maintain pension plans for 645 industrial and nonindustrial firms, says Johnson & Higgins, came to $28.6 billion for more than 21 million employees. This amount represents a 10.1% increase over the previous year's totals.

Keene points out that FAS-36 is an interim rule designed to help the accounting profession gain some time "in its struggle to obtain a greater degree of comparability among the corporations with respect to pension disclosure. In the meantime, employers, employees, financial analysts, and other users of corporate annual reports will have to make their own judgments on the relevancy of the new data."

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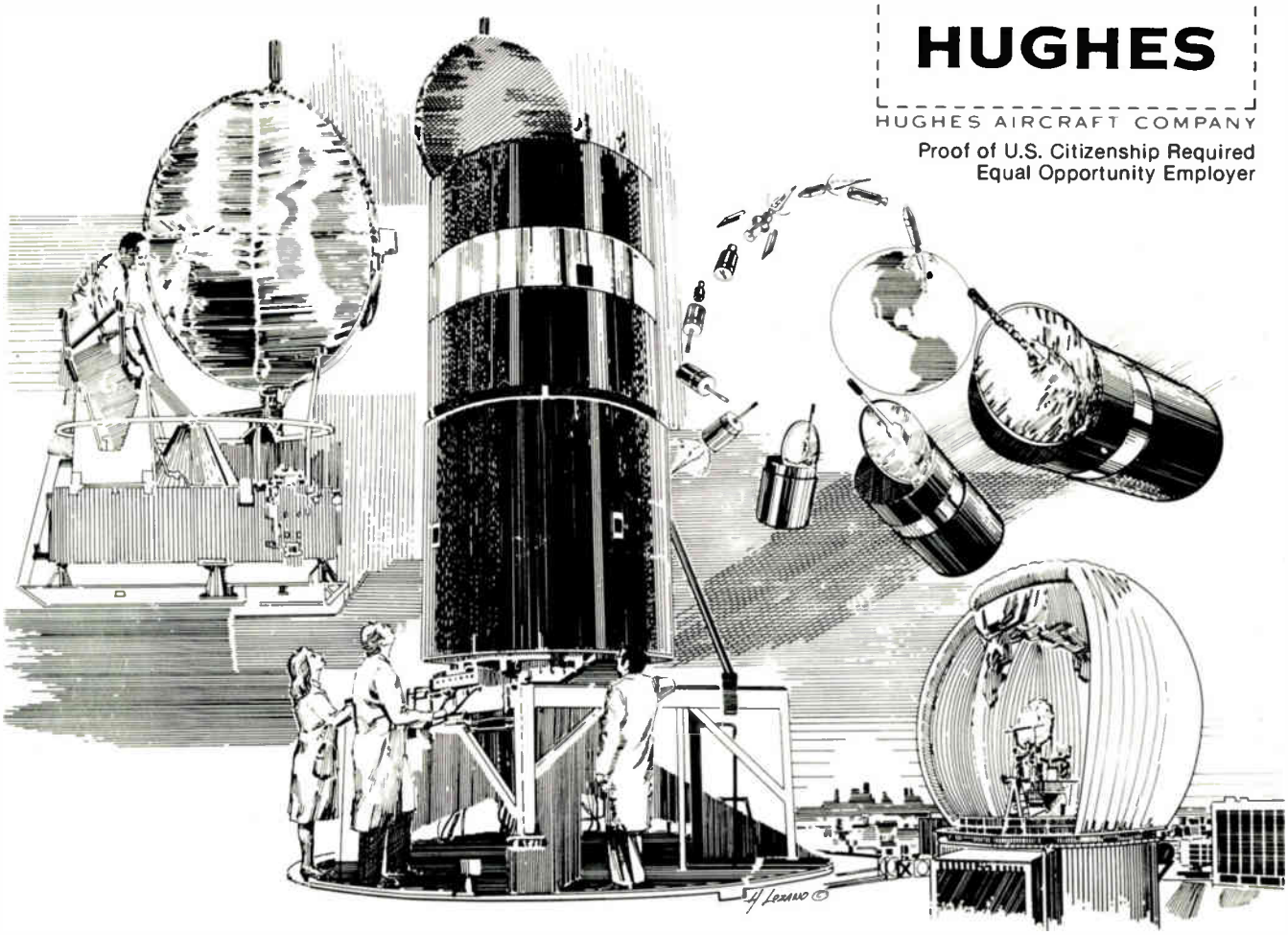

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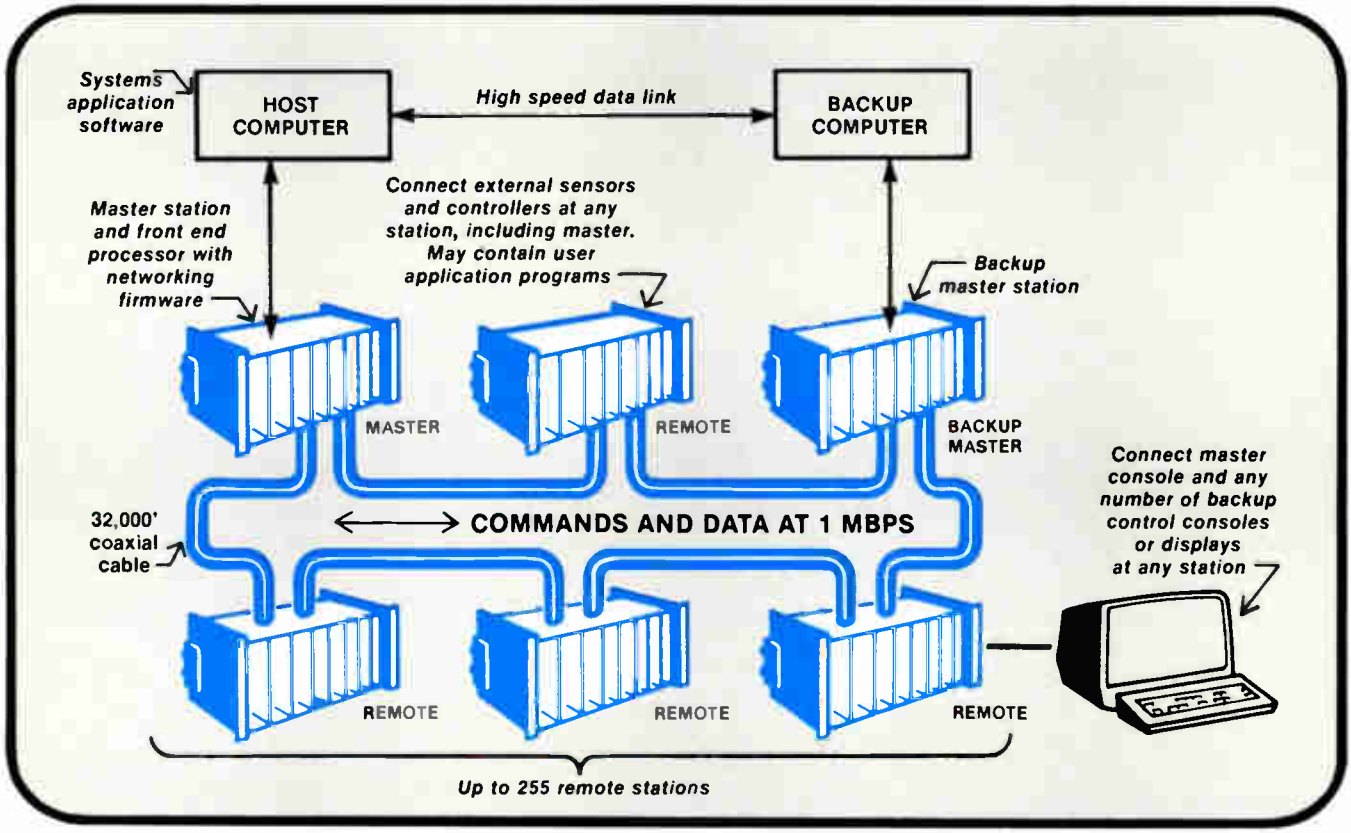


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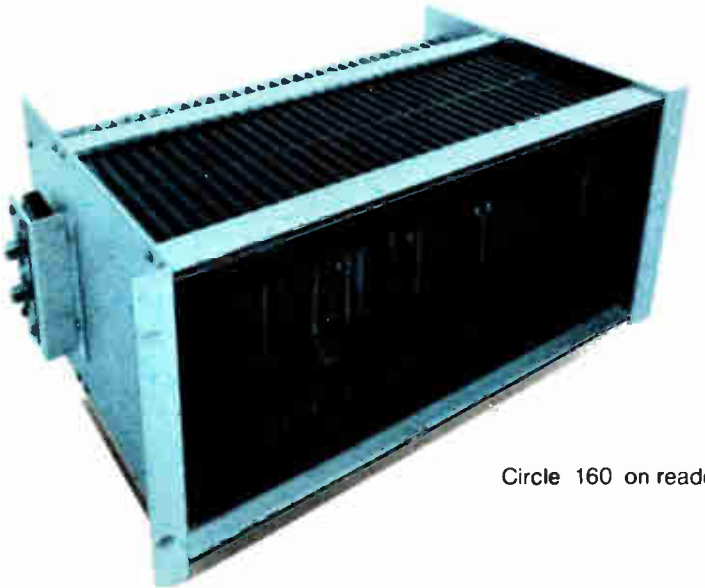

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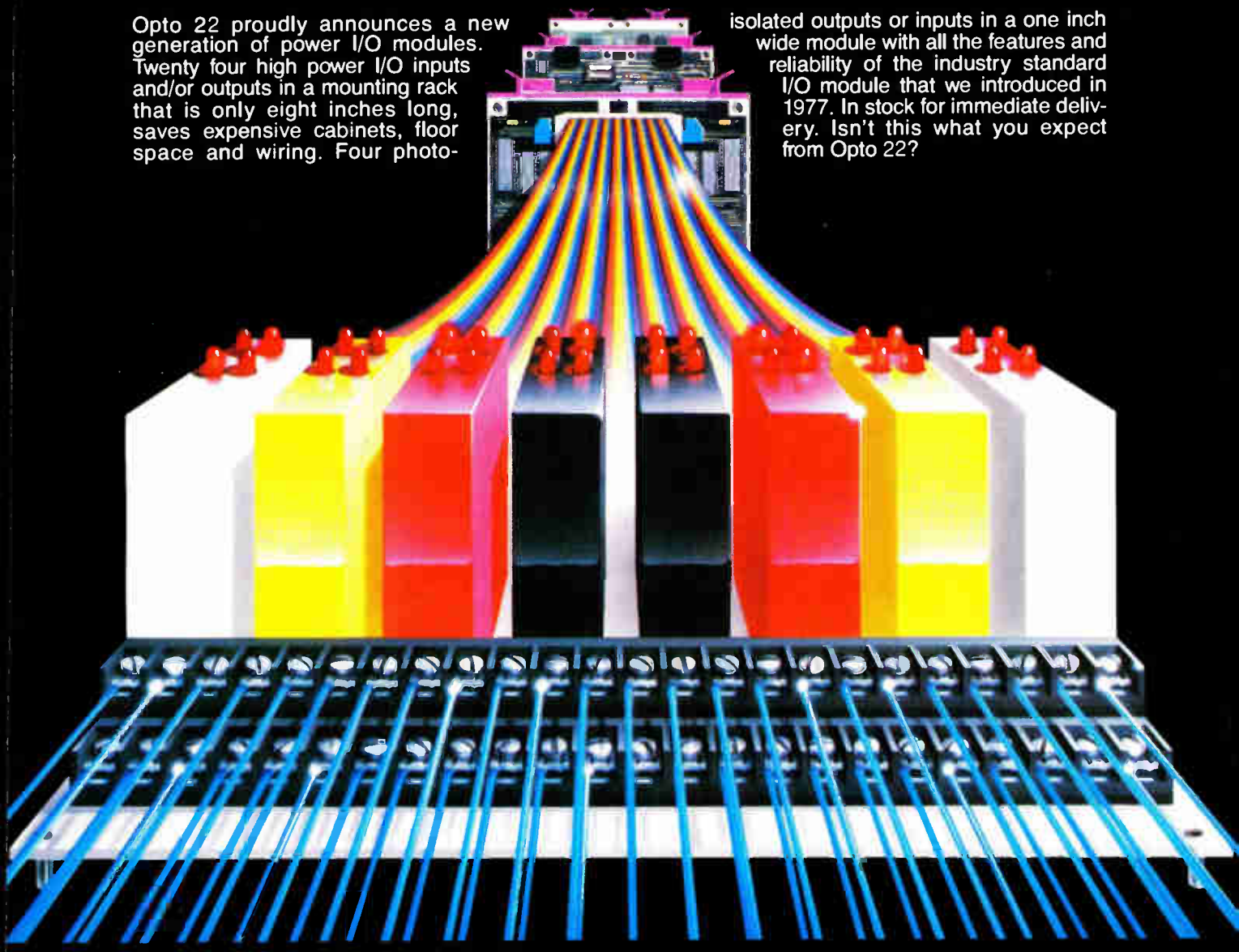

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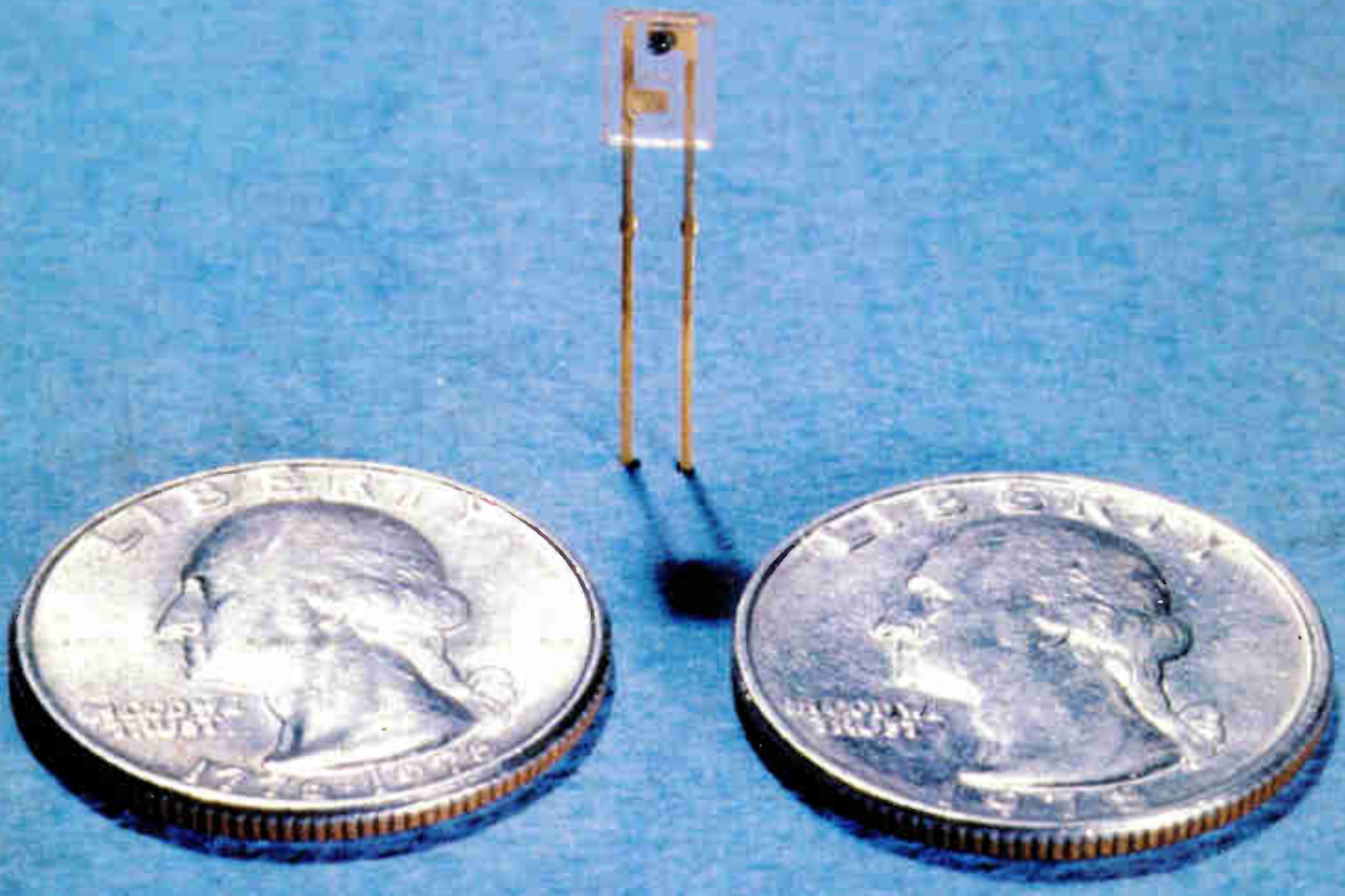

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