

NOVEMBER 3, 1981

SILICIDES SPEED UP COMMERCIAL ICs/101

Putting the PDP-11 minicomputer on a chip/ 130

Electron-beam lithography gets set for production/ 138

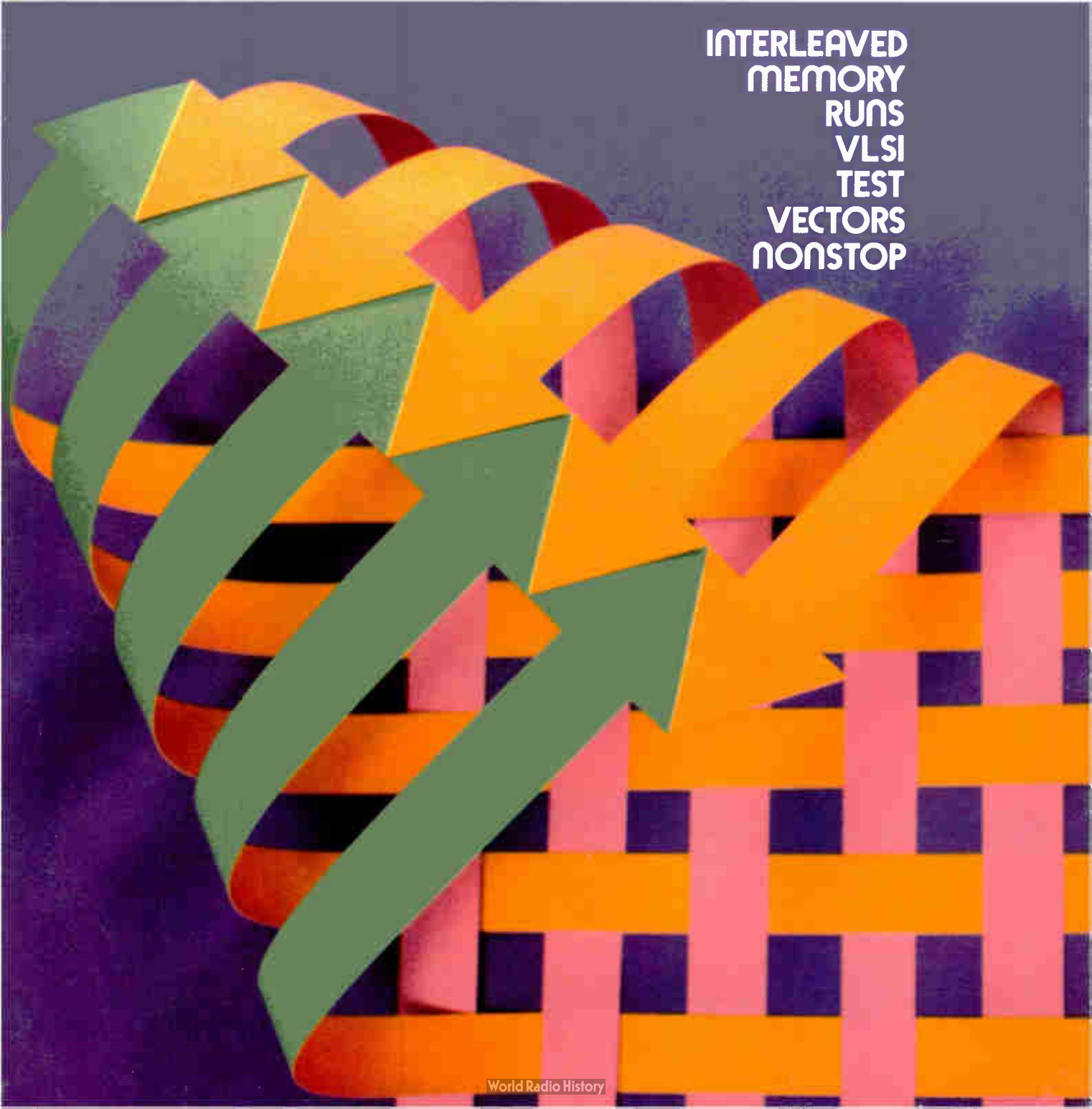
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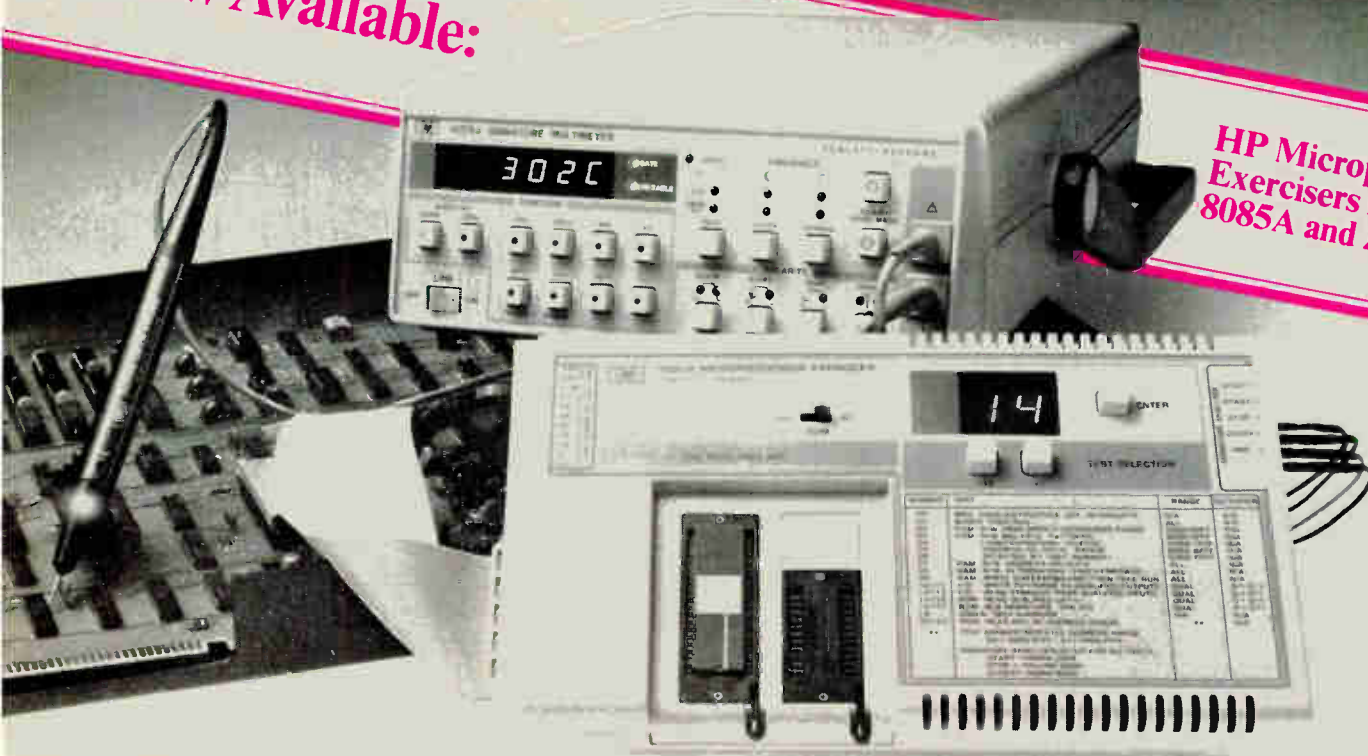
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Cover: Test system speeds VLSI checks, 122

Improved pattern-generation techniques in a new test system hasten the exercising of complex very large-scale integrated circuits, primarily through the use of interleaved memories. For automated program generation, the unit is designed to link with computer-aided design systems.

The cover illustration is by Art Director Fred Sklenar.

HP, DEC target office-automation market, 106, 110

Two more computer heavyweights are moving to become major competitors in the burgeoning office-automation market. Hewlett-Packard Co. is inaugurating an entire product line (p. 106), and Digital Equipment Corp. is making a tactical switch by going after the end user rather than its traditional customer, the original-equipment manufacturer (p. 110).

IC holds guts of 16-bit minicomputer, 129

A PDP-11 processor fits on a single chip, reducing cost and retaining minicomputer performance, through space-saving architectural and design concepts. For application flexibility, program memory is off chip.

Shaped electron beam writes finer pattern faster, 138

A third-generation direct-writing electron-beam machine can tailor its beam spot size and shape to fit various pattern elements. It can write features as fine as 1 micrometer on as many as forty-five 3-inch wafers per hour.

Electron-beam projector defines features as small as 0.2 μ m, 144

An electron-beam machine that projects mask patterns onto a wafer has achieved features as fine as 0.2 micrometer, with ultimate resolution expected to be less than 0.1 μ m. The experimental machine has shown that image distortion and alignment problems are hardly the insurmountable barriers envisioned for electron image projectors.

Resistors fight temperature drift, hit new accuracy heights, 151

A new family of nickel-chromium foil resistors cancels much of its intrinsic resistivity variance with temperature by using a ceramic substrate having a thermal expansion that imparts a counter strain-induced resistance change to the metal foil. This improves accuracy over the previous generation of foil resistors by an order of magnitude.

In the next issue . . .

Where computer-aided design is going: a special series of articles . . . a data-base manager for microcomputer systems . . . automated capabilities in a radio-frequency level meter . . . inexpensive home TV reception from a 12-gigahertz satellite.

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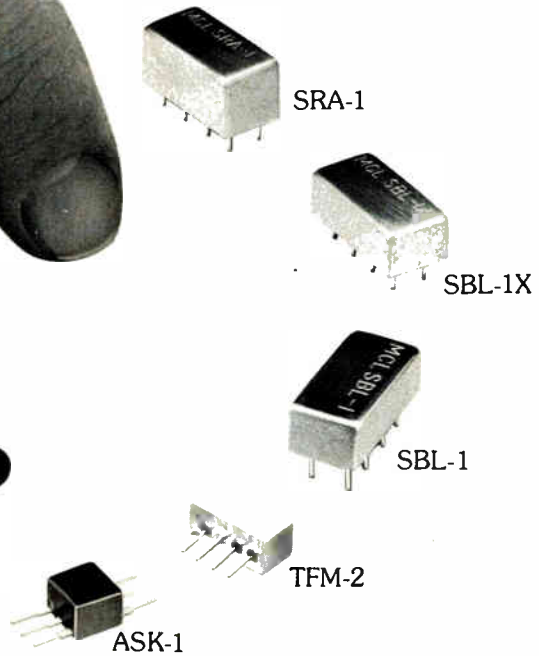
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CONVERSION LOSS, dB					
one octave bandedge	6.5	6.0	7.5	7.5	7.0
total range	8.5	7.0	8.5	9.0	8.5
ISOLATION, dB, L TO R					
lower bandedge	50	50	45	45	50
mid range	40	40	35	30	35
upper bandedge	30	30	25	20	20

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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Publisher's letter

One of the major strengths of *Electronics* is its peripatetic editorial staff, which each year logs thousands of miles of travel (and dollars expended) throughout the world seeking articles and news about evolving technologies. Often these stories are continuing sagas that start as news of developmental prototypes and end up as full disclosures in bylined technical articles. Excellent examples of editorial wanderings being converted into important articles are this issue's two articles on high-throughput electron-beam lithography.

The article by Rodney Ward of Philips on its new electron-beam projector began in 1978 when Sam Weber, then executive editor, and Kevin Smith, our London bureau manager, visited Philips Research Laboratories in Redhill, England, and were shown a prototype of an experimental image projector being developed for the production of very large-scale integrated-circuit masks. The immediate result was a news story that appeared a month later [*Electronics*, Nov. 23, 1978, p. 73].

But so intrigued were Sam and Kevin by this unconventional approach to the then nascent electron-beam technology, that they asked for and received a commitment from Philips for a technical article on the image projector. It took some time, however, because the machine described in Rodney Ward's article on page 144 is a considerably refined and improved version that eliminates the distortion and alignment problems inherent in the original system.

The turnaround for the story on IBM's EL-3 machine was somewhat faster. This past March, packaging and production editor Jerry Lyman

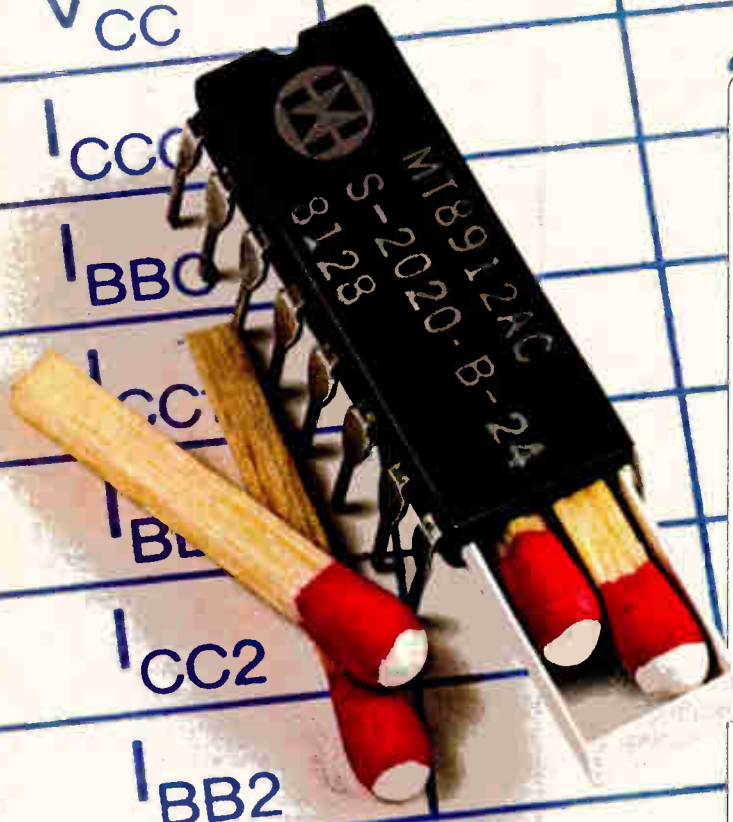
(who edited both these pieces) visited IBM's East Fishkill, N. Y., facility for input on a story he was doing about computer-aided design. While there, he was given a tour of the then new and highly automated IC-production line known as the QTAT (Quick Turn Around Time) line. An IBMer offhandedly pointed out a brand new scanning electron-beam machine being debugged: the subject of the article beginning on page 138.

Having worked on the first major article about the EL-1, IBM's first electron-beam system back in 1977, Jerry immediately tried to get the lowdown on the EL-3. Although the company would reveal no details at the time, Jerry nailed down a promise for a full article on the new high-throughput system at the appropriate time, and here it is.

Both of these articles reflect a continuing recognition by *Electronics* of the significance of this emerging technology to the development of semiconductor technology. "Advanced lithography techniques are the driving force behind VLSI," says Jerry who has been following and reporting on them for more than five years. "And we're still only at the beginning. The electron-beam approach is developing rapidly and will be the VLSI engine for at least the next decade. And right behind it is X-ray lithography."

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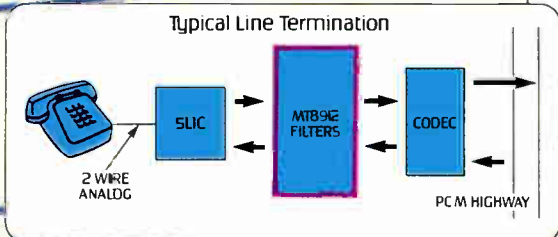
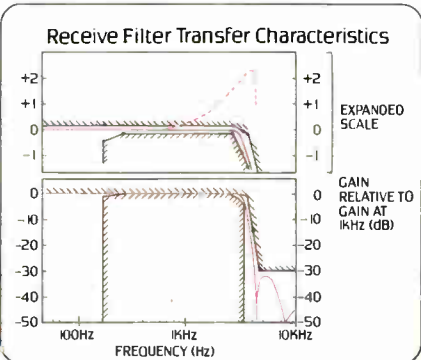
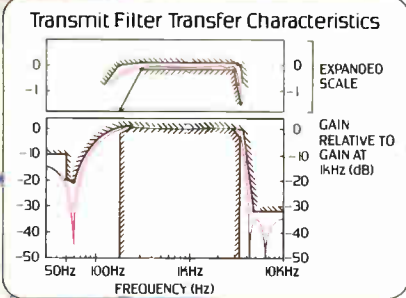
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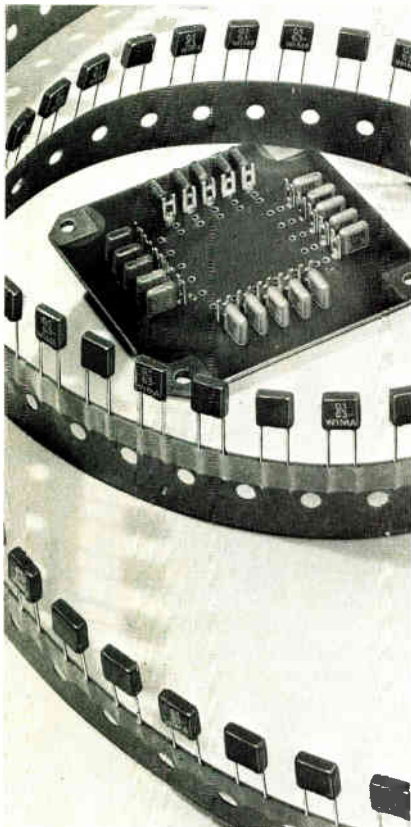
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Readers' comments

The cost of conversion

To the Editor: The article, "Japanese slow to gain in computers," appearing in the July 14th issue of *Electronics* (p. 101) contains erroneous and misleading information about Hitachi Ltd.'s computer operations, apparently based on a research report by Martin Simpson & Co.

We regard the publication of these incorrect statistics to be an extremely serious matter—especially since your readership is exceptionally knowledgeable and influential in the area of computer products.

In fact, the report by Martin Simpson & Co. referred to in your article estimates Hitachi computer revenue in 1980 at 250 billion yen and in 1981 at 290 billion yen. This results in a 1981 growth rate of 16% over 1980 revenues. In addition, the Simpson report estimates that "Hitachi's computer revenues will grow at an annualized rate of 15% from 1981 to 1986" (p. 49). This obviously contradicts the figure of 11.4%, which is quoted as Hitachi's annual growth rate over the five-year period from 1980 to 1985.

As a matter of fact, Hitachi currently has a plan to double its computer sales over the next five years, and it expects to be able to maintain an average annual growth rate of at least 15% during this period.

K. Kanzaki
Hitachi Ltd.
Tokyo, Japan

■ **The Editor replies:** *The difference between the figures in the Simpson chart and the one used with the article is apparently due to a change in the conversion rate in the latter. The rate used for 1980 was 226 yen to the dollar; for 1985, it was 200.*

Corrections

On page 170 of the Sept. 22 issue, the cost of GenRad Inc.'s 2272 board test system in its smallest usable configuration should have been \$180,000, instead of \$200,000. In the August 25 issue, the price of a 2-ft-wide roll of Vynastat antistatic floor mat from Tepromark International Inc. mentioned on page 247 is \$482.

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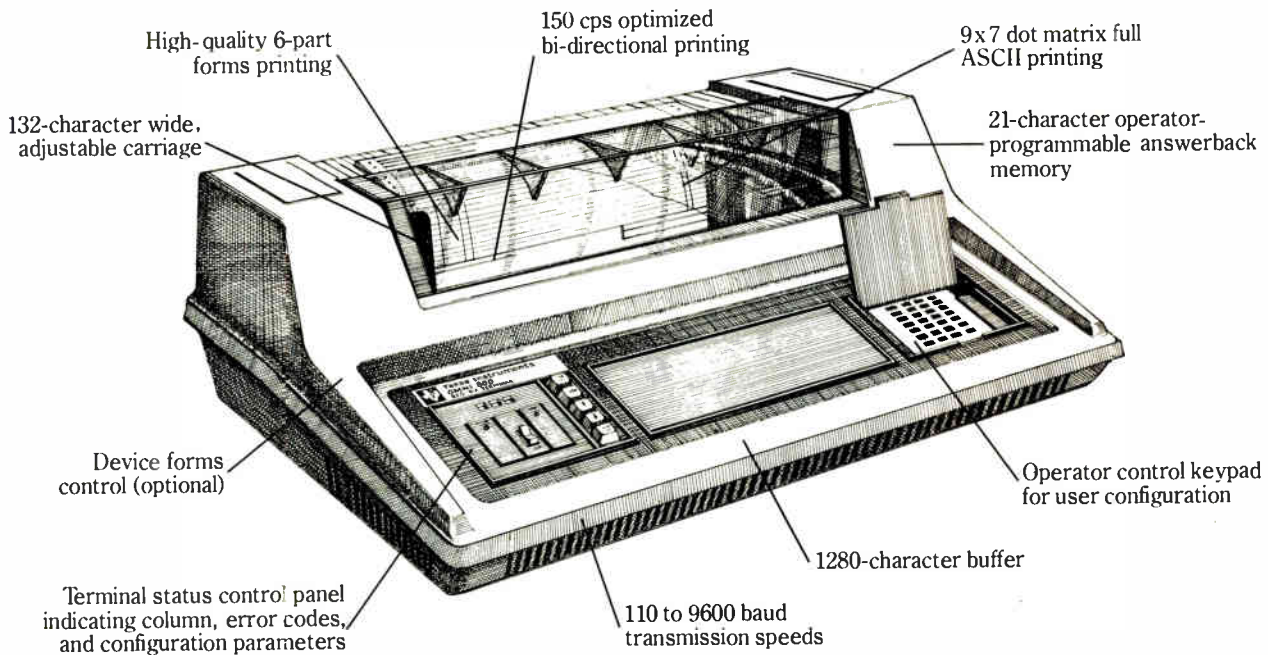
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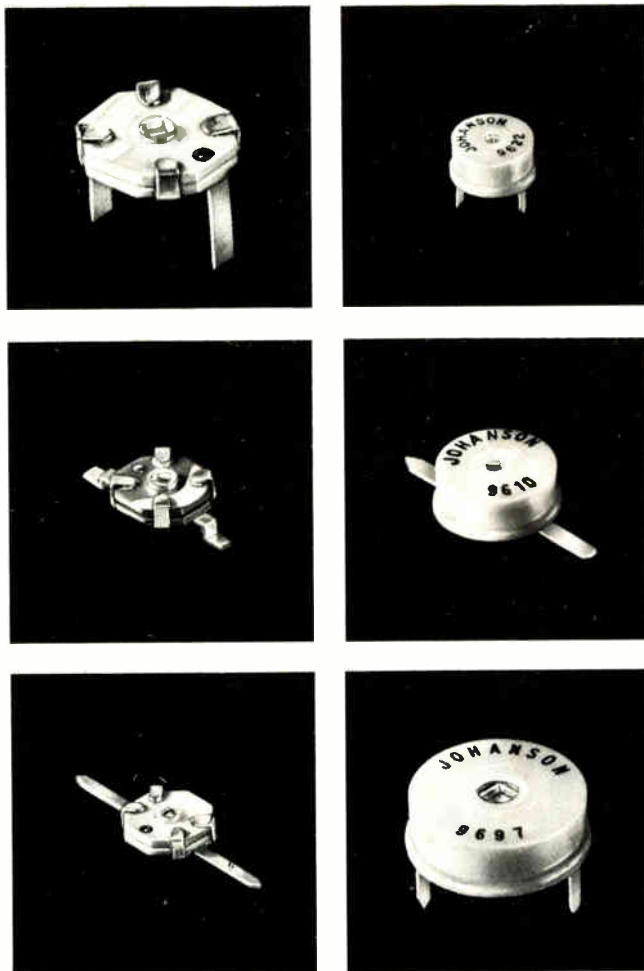
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News update

■ The bugs in computer programs are so insidious that it would be foolhardy to assume that there will be no software problems during the space shuttle Columbia's second voyage, scheduled for early November. But Houston Space Center deputy director of data systems and analysis Richard P. Parten knows one that won't cause any trouble. It's the glitch that caused the shuttle's four primary computers (IBM AP 101s) to fail to synchronize when they were switched on for the first voyage, delaying the launch by two days.

"We have instituted procedures at Cape Kennedy so that when the computers are initialized, we can check to determine if the lack-of-synchronization condition exists," Parten says. The latest calculations by the National Aeronautics and Space Administration show that there is only a 1.5% probability of this happening and if it does, NASA plans to reinitialize the computers.

Double check. What the NASA engineers do is look at "downlist information." This is the computer's contribution to the downlink telemetry information—the data sent from the shuttle to the ground. "We can tell from the nature of the parameters in the downlist information if the glitch is present," Parten notes. But he adds that the test is not 100% certain.

So NASA makes a second check. It cycles the primary computers to the beginning of their operation and then initializes the backup system just as it would do on launch day. This ensures that the backup and the primary machines can communicate with each other. Even though the primary computers must be restored to the start of their countdown sequence, their and the backup's time bases remain turned on and in synchronization.

Why not just fix the timing glitch and be done with it? Parten has a ready answer. "We elected not to fix the problem itself, because it occurs in some of the most complex code in the computer's operating system. And, we would want to get a lot of testing of any change before we fly it."

-Harvey Hindin



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People

**Executives shun terminals,
says Ruebel of Xerox**

It may be a while before computer work stations make it all the way to the top and are commonly found inside the offices of top management, says Robert J. Ruebel, recently named senior vice president of Xerox Corp.'s Office Products division.



Preparing for market drive. Xerox's Ruebel says professionals are the market of the future for sophisticated data systems.

"There has been a lot of discussion about executive and managerial work stations, but I think the problem is the fact that there's not a lot of local executive information floating around in either office networks or computer networks," explains the 40-year-old native of San Francisco, who heads sales and marketing at the Dallas-based division. "There will always be the early adapters—the executive who has the work station in his or her office—but I think they will be a very small percentage of the population until the data base supports information that is of interest to them."

However, the greatest untapped opportunities in the office marketplace are professionals (marketers, financial specialists, technical employees, personnel staff members) and others who need more than conventional terminals or personal computers, he states. That's why after many years of development Xerox introduced last spring the 8010 Star information system [*Electronics*, May 5, p. 46]. And that's why the

industry should expect to see Xerox make a push in this professional market area.

"We really expect to own that aspect of professional productivity," says the San Francisco State college graduate—he has a bachelor's in English language arts and a master's in business administration. After receiving his MBA in 1966, Ruebel went to work for TRW Systems in Southern California and took a

management training course in computer science that condensed "10 years of experience into three." In 1968, he left TRW to join a new business-computing service firm called Data Station. The next year, he joined Xerox, which was then starting its own computer services operation.

"Two and three years ago when we called on major accounts, customers were thinking only of text processing," he explains. "We used to get some funny looks when we talked about the professional user and a variety of devices needed to suit a variety of users and local area networks."


But that has all changed in the past 18 months. Customers are now asking about local network capabilities, and "the awareness is growing that there is more than text editing to productivity improvements and there are different kinds of devices involved, personal computers among them."

**Bailey's, Norton's Iomega
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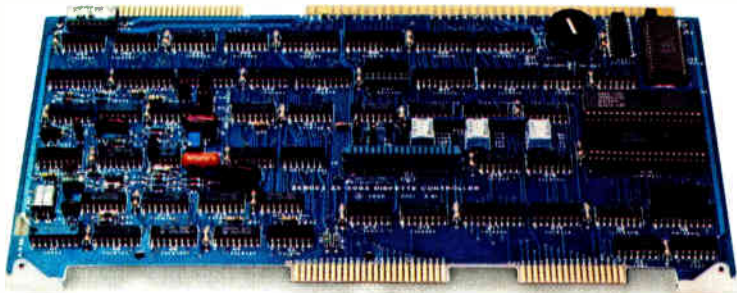
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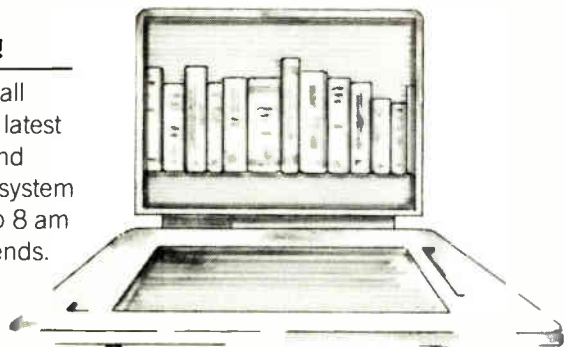
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People

associates in Ogden, Utah, have done is create a memory technology that just might be the missing link between the hard disks used with Winchester-technology drives and the floppy diskette. The 8-inch Iomega drive uses the basics of floppy-disk technology, yet promises the capacity and reliability usually associated with Winchester-type hard-disk drives [*Electronics*, May 5, p. 106]. Using a floppy-disk cartridge, the 10-megabyte Iomega drive thus displays the archival ability, removability, and cost-effectiveness that is usually associated with lower performance.

Advancing beyond on-paper specifications to building the hardware is a substantial step. Bailey and Norton, with 15 and 16 years, respectively, of experience behind them in disk drives at IBM, have taken it.

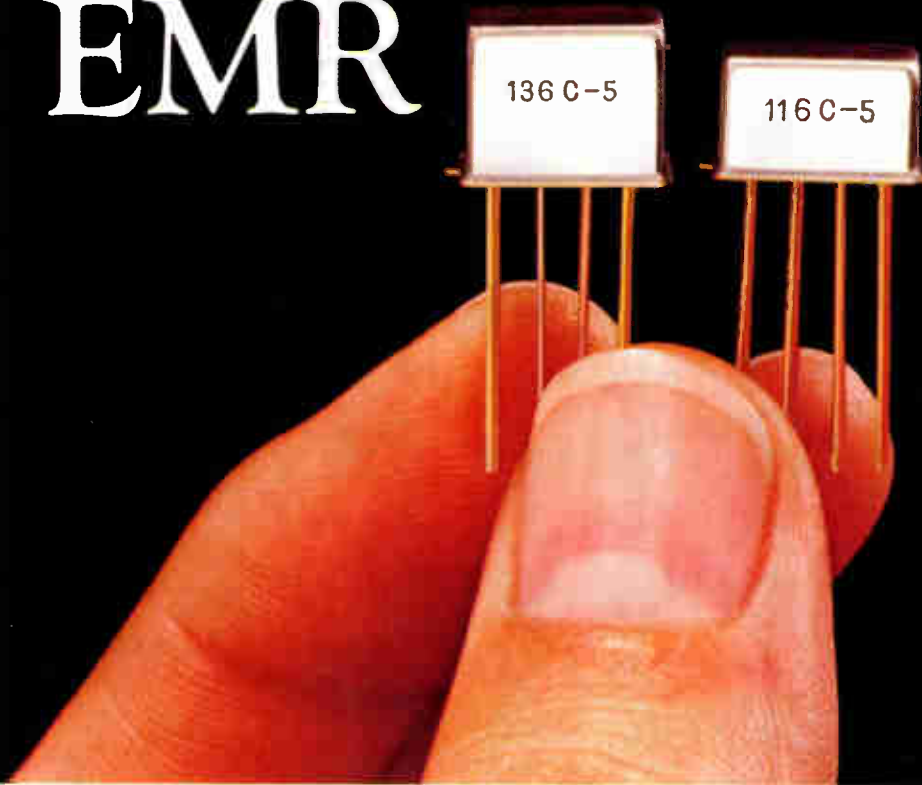
Their secret is the Bernoulli effect, a fluid-flow phenomenon that was first described more than two centuries ago. In their disk drive; a vacuum created by rapid airflow pulls the diskette down, striking a delicate but reliable balance with the centrifugal force holding it up. The recording head flies over the medium, just as in Winchester drive, clearing the copper by 20 to 40 microinches and the gap of the head by less than 10 μ in. The medium itself flies 4 to 7 mils over the Bernoulli plate.

"We spent 14 to 16 months looking at the flying height to get the right specifications," recalls Bailey. "We also had to tune the read-write channel and optimize the servo mechanism." With the drive, Norton asserts, Iomega "essentially has eliminated the mechanical perturbations." Now the company is ironing out the variations in the physics associated with recording data.

Norton and Bailey have remarkably similar backgrounds. They are both 41 years old and natives of Utah. Each earned bachelor's and master's degrees at Utah State university—Norton in mechanical engineering and Bailey in electrical engineering—and Norton has a doctorate from Colorado State University. Both are married and have four children each. □

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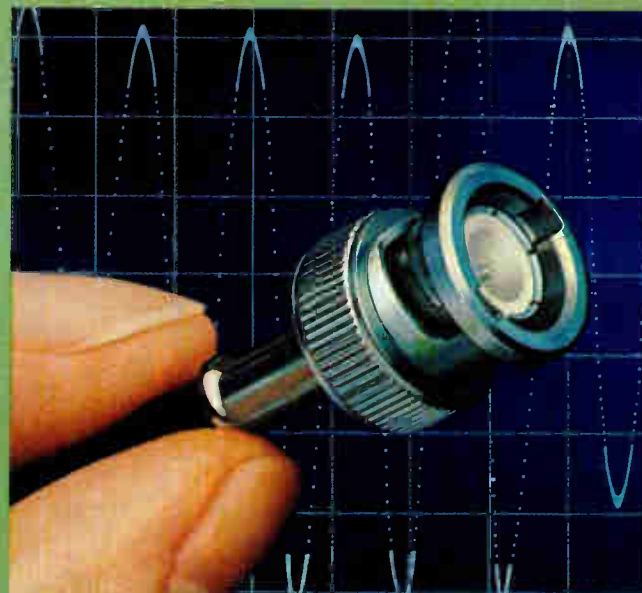
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Dielectric Withstanding Voltage—1500 volts RMS/minute

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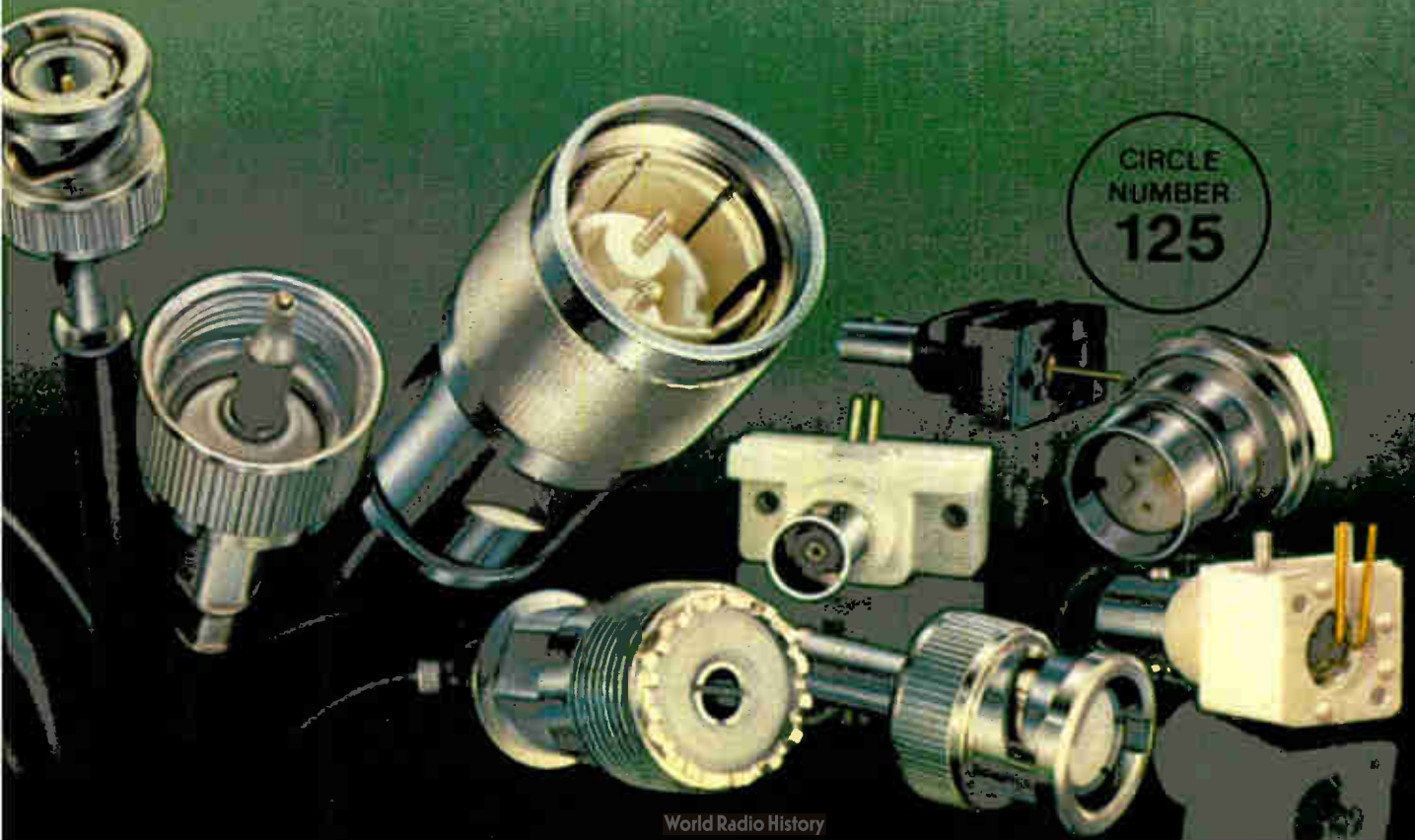


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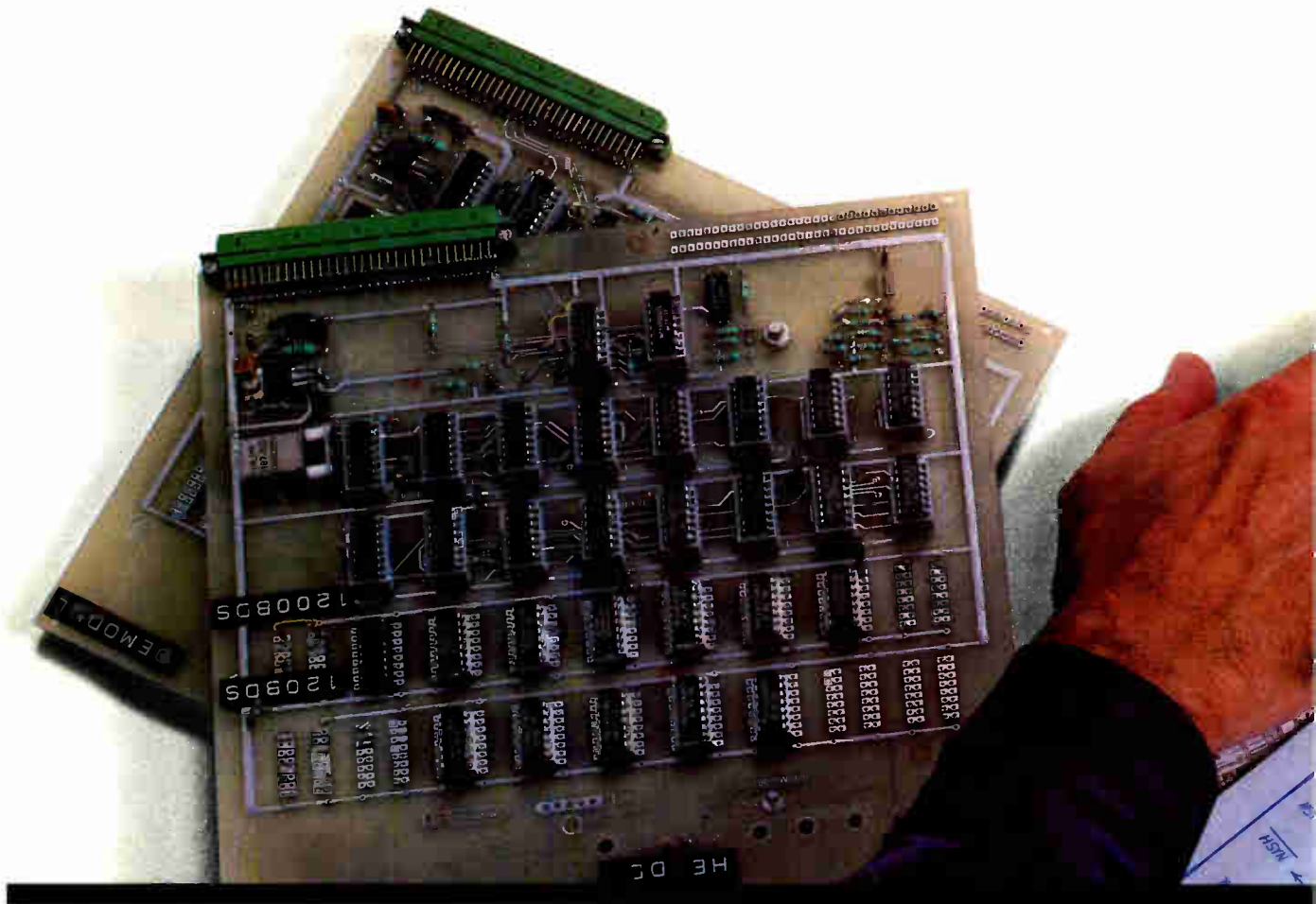
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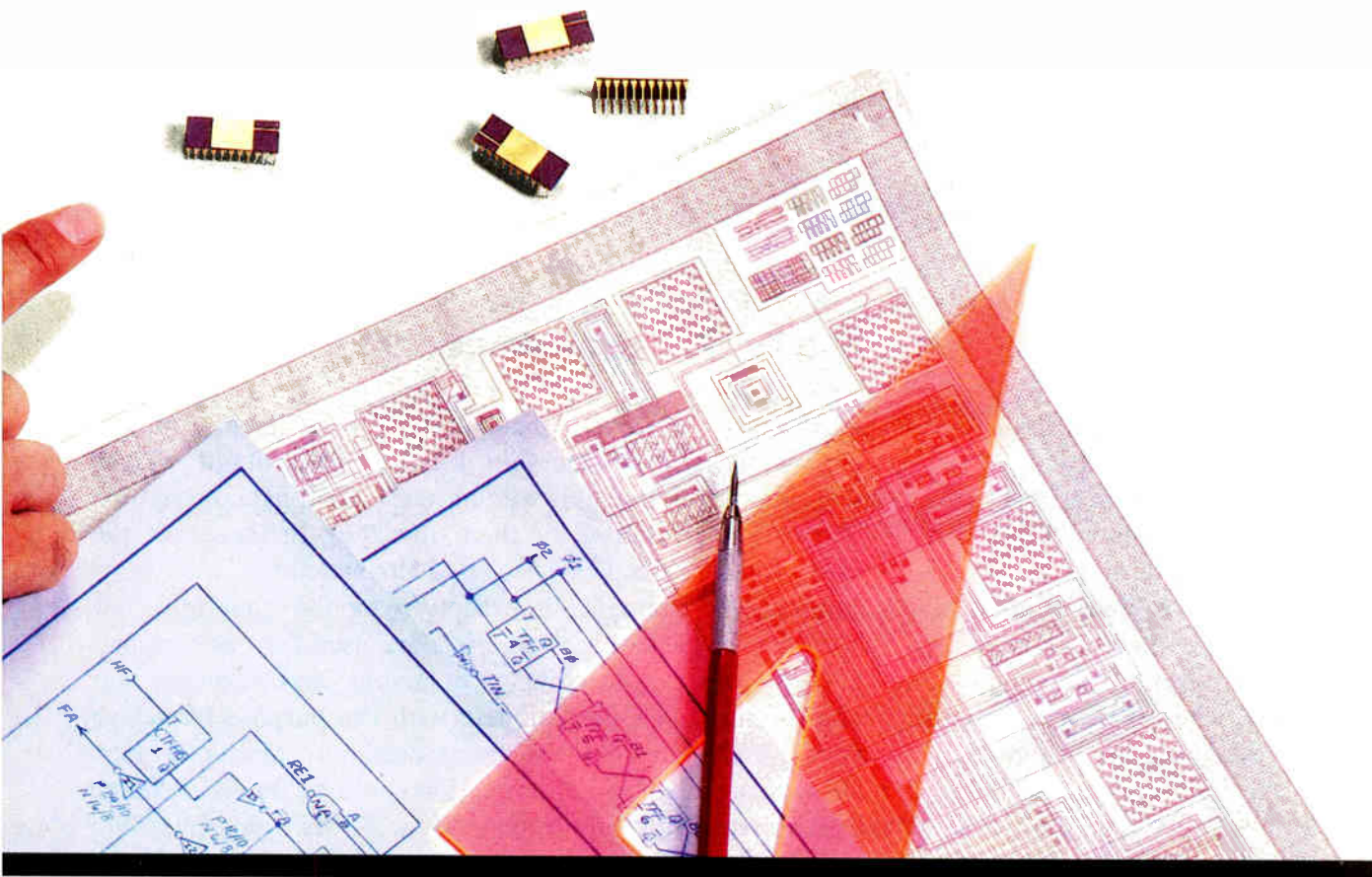
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Circle 23 on reader service card

Video recorder threat: a cause for concern

The Federal appellate court in San Francisco has handed down a puzzling ruling, one that affects a strong and growing segment of the consumer electronics industry. The court, overturning a decision reached by a lower court, decided that anyone making a video-tape recording of a copyrighted television program is infringing on the rights of those who own the program—even if the recording is done at home only for private use.

At first glance, the decision pulls the rug from under the burgeoning video-cassette recorder business. But all the parties to the action, the result of a suit filed in 1976 by two major movie studios, agree that the latest decision is just another step on the way to the U. S. Supreme Court. As a spokesman for Sony Corp. sees it, from the start that route was predicted by everyone who was involved in the litigation.

Nevertheless, it is difficult for the lay person of average intelligence to understand fully the court's rationale. First of all, it would seem constitutionally clear that programmed material, transmitted to the home, becomes the property of those receiving it at home once it arrives. If the recipient of the material wishes to record it, and provided the recording is not done for commercial purposes, that is the business of the individual and not of the Government.

Furthermore, what of all the tape recording that is done of audio programs—music recorded off the air? That activity has been going on unimpeded for years, and it is not

evident that anyone has been terribly injured by the pursuit. Finally, what about all the individuals who have photocopied copyrighted material for their own use? In that case, the so-called fair-use doctrine comes into play: there is an exception to the copyright law where the materials are used for news reporting, teaching, scholarship, and research that does not compete with the purpose for which the materials were originally produced. Perhaps a like exception could be made for home video recorders—after all, the materials were originally made to be viewed by individuals for entertainment.

Equipment makers profess little concern about the San Francisco ruling and say they are confident that the Supreme Court ultimately will see the issue their way. We certainly hope so, for two reasons. First of all, such a restriction would be virtually unenforceable and is sure to be breached with impunity. And since the only other remedy being suggested—royalty fees to owners of the broadcast to be paid by equipment manufacturers—would increase the cost to the consumer of the recording equipment, this would put a damper on a promising new industry. It could be another case of murdering the goose that laid the golden egg.

It might be a good idea for the Congress to look into this situation. It's possible it could redress by legislation what appears to us as a potential injustice perpetrated on the public for the sake of a technicality.

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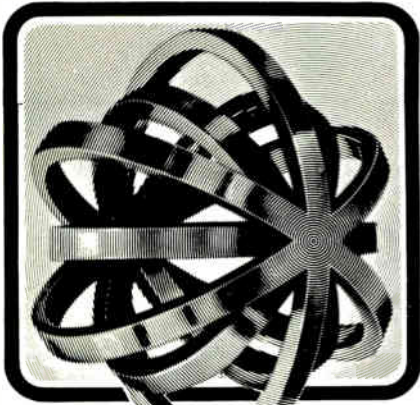
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Meetings

National Telecommunications Conference and Exhibition, IEEE (J. W. Joyner, South Central Bell Telephone Co., 518 Baronne St., Room 1035, New Orleans, La. 70140), Marriott Hotel, New Orleans, Nov. 29-Dec. 3.

5th Canadian Symposium, International Information Word-Processing Association (IWP, 1015 North York Rd., Willow Grove, Pa. 19090), Chateau Laurier, Ottawa, Ont., Dec. 1-3.

21st Symposium on Semiconductors and Integrated-Circuits Technology, The Electrochemical Society of Japan (Shin Yuraku-cho Building, 1-12-1 Yuraku-cho, Chiyoda-ku, Tokyo 100), Bridgestone Hall, 101 Kyobashi, Chuo-ku, Tokyo, Dec. 3-4.

International Electron Devices Meeting, IEEE (Melissa Widerkehr, Courtesy Associates, 1629 K St., N. W., Washington, D. C. 20006), Washington Hilton Hotel, Washington, D. C., Dec. 7-9.

Infrared and Millimeter Waves Conference and Exhibition, IEEE (K. J. Button, Massachusetts Institute of Technology, National Magnet Laboratory, Cambridge, Mass. 01239), Carillon Hotel, Miami Beach, Fla., Dec. 7-11.

Computer Networking Symposium, National Bureau of Standards and IEEE (Robert Toense, B226 Technology Buildings, NBS, Washington, D. C. 20234), NBS, Gaithersburg, Md., Dec. 8.

Winter Simulation Conference, IEEE (Claude Delfosse, CACI Inc., 1815 North Fort Myer Dr., Arlington, Va. 22209), Peachtree Plaza Hotel, Atlanta, Ga., Dec. 9-11.

6th Meeting on Integrated and Guided-Wave Optics, Optical Society of America and IEEE (OSA, 1816 Jefferson Pl., N. W., Washington, D. C. 20036), Asilomar Conference Center, Pacific Grove, Calif., Jan. 6-8, 1982.

5th Los Angeles Technical Symposium, International Society for Optical Engineering (SPIE, P. O. Box 10, Bellingham, Wash. 98227), Los Angeles Marriott Hotel, Los Angeles, Jan. 25-29.

First Spacecraft Electronics Conference, EIA (Frank A. Mitchell, EIA, 2001 Eye St., N. W., Washington, D. C. 20006), Hyatt Hotel, Los Angeles, Jan. 26-28.

Advanced Semiconductor Equipment Exposition and Conference, Electronic Representatives Association and Cartledge & Associates Inc. (CAI, 491 Macara Ave., Sunnyvale, Calif. 94086), Convention Center, San Jose, Calif., Jan. 26-28.

Annual Reliability and Maintainability Symposium, American Society for Quality Control, IEEE *et al.* (H. C. Jones, Westinghouse, MS 3608, P. O. Box 1521, Baltimore, Md. 21203), Biltmore Hotel, Los Angeles, Jan. 26-28.

First Military Computers and Software Seminar, American Defense Preparedness Association (ADPA, 900 Rosslyn Center, 170 N. Moore St., Arlington, Va. 22209), Sheraton National Hotel, Arlington, Va., Jan. 27-28.

Seminars

Smart Plastic Cards—Electronics Transactions in a Wired Society, Stanford Business Research Foundation (770 Welch Rd., Suite 154, Palo Alto, Calif. 94304), Stanford Court Hotel, San Francisco, Nov. 18-19.

Computer Graphics and CAD/CAM Systems Implementations, National Computer Graphics Association (NCGA Seminars, 2033 M St., N. W., Suite 300, Washington, D. C.), the Airport Hyatt, Los Angeles, Nov. 30-Dec. 1.

Electromagnetic Compatibility Engineering, Center for Professional Advancement (P. O. Box H, East Brunswick, N. J.), Villa Hotel, San Mateo, Calif., Dec. 14-17.



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PQ 50-1	0 to 50	0 to 1	Quarter-rack
PQ 100-0.5	0 to 100	0 to 0.5	Quarter-rack
PH 10-10	0 to 10	0 to 10	Half-rack
PH 20-6	0 to 20	0 to 6	Half-rack
PH 50-3	0 to 50	0 to 3	Half-rack
PH 100-1.5	0 to 100	0 to 1.5	Half-rack
PHR 20-12	0 to 20	0 to 12	Half-rack
PHR 50-8	0 to 50	0 to 8	Half-rack
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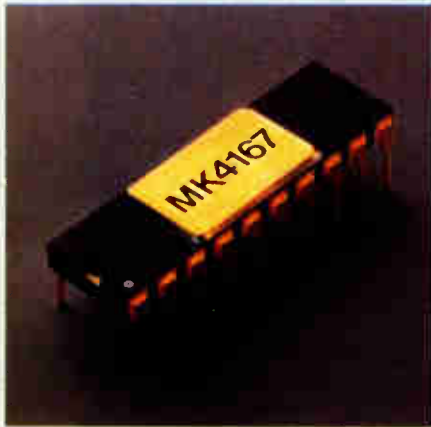


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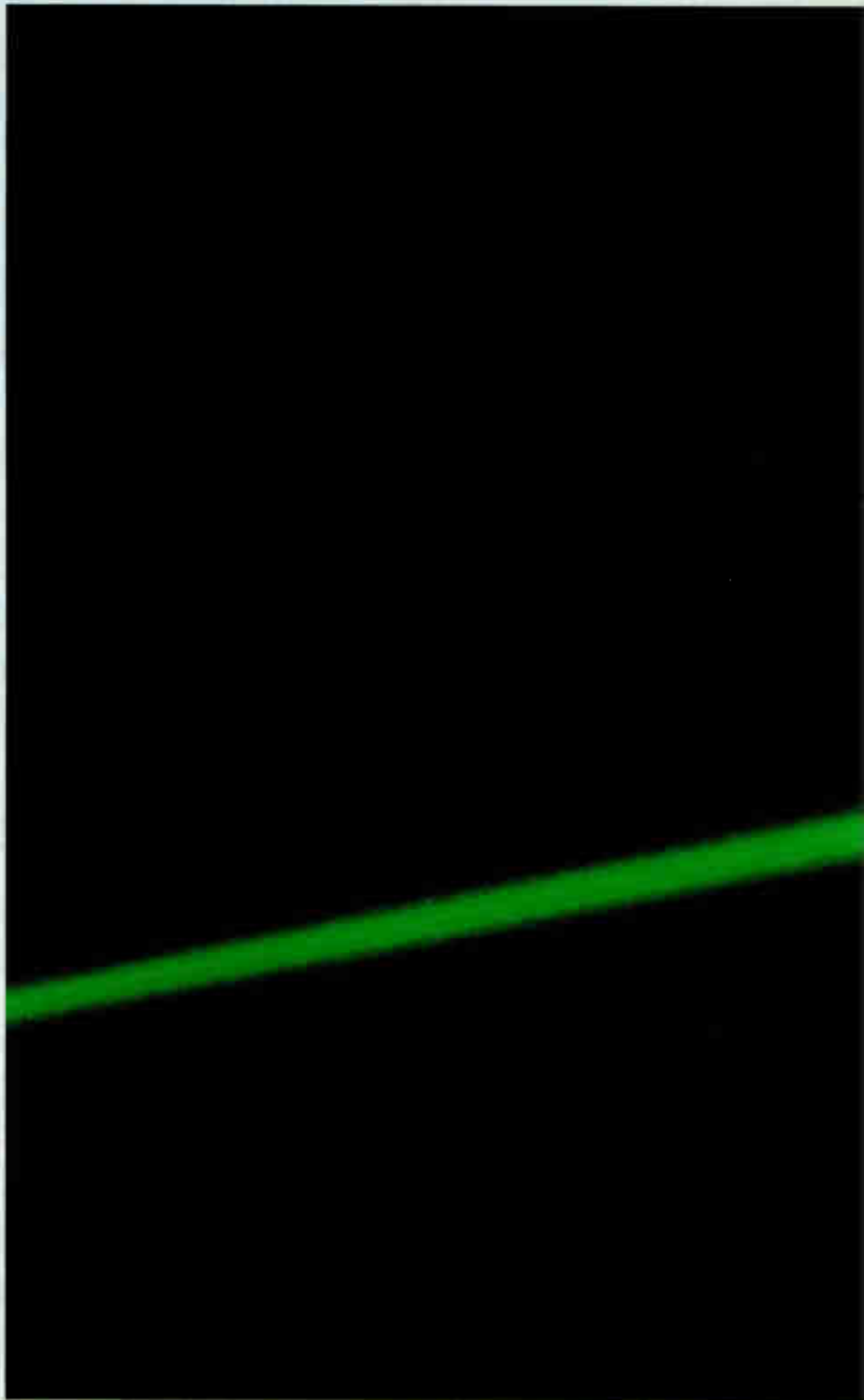
The MK4167 has a JEDEC-proposed, standard 20-pin configuration. It's organized as 16K x 1. Has fast 55ns access and cycle times. Low 120ma active and 40ma stand-by currents. A single +5 volt power supply. It has speed, low power, reliability — everything you've been looking for in a 16K static RAM. So, we could have stopped there.

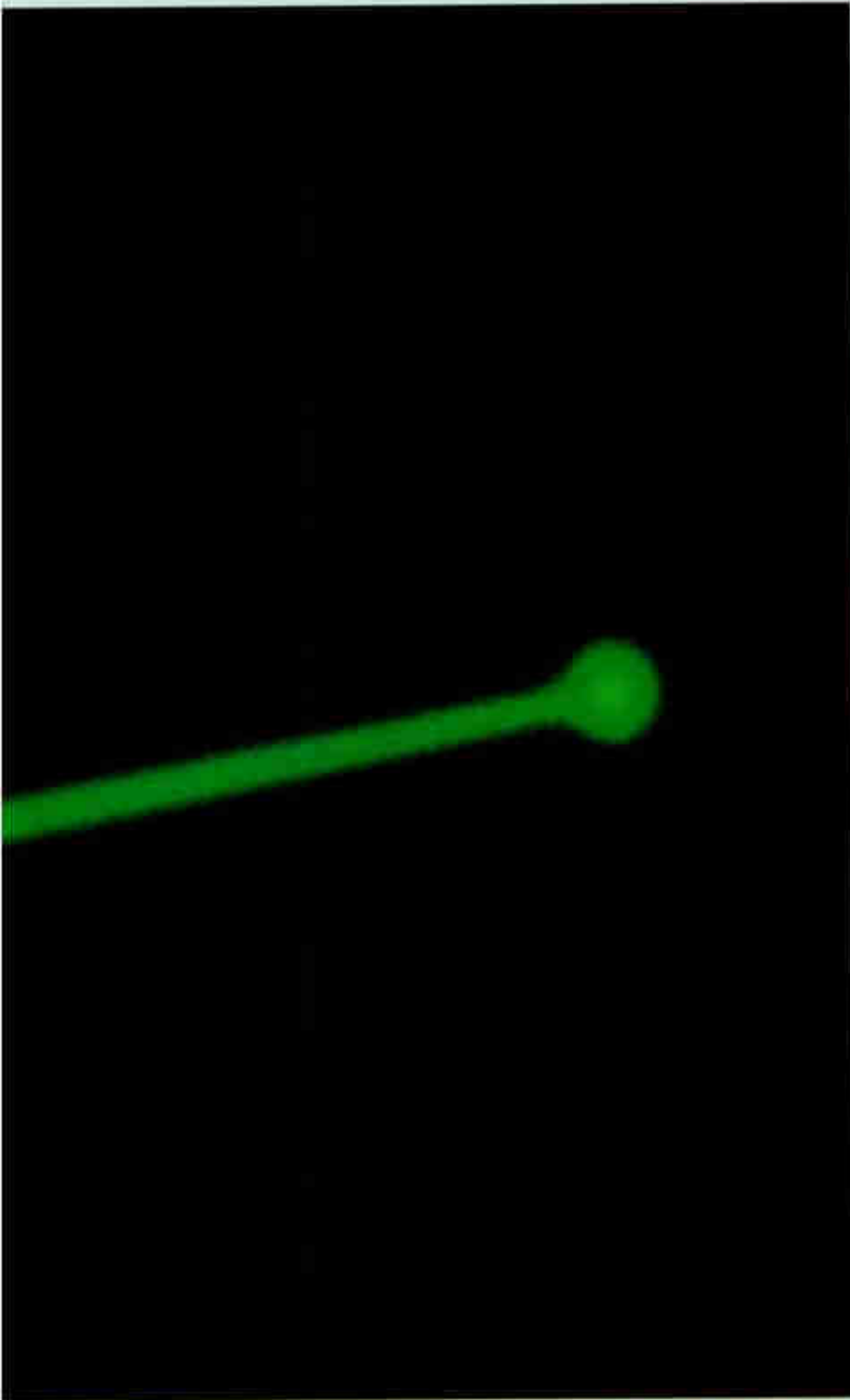
But that's not Mostek.

On top of its other features, we designed the MK4167 to satisfy high volume demands. We enhanced manufacturability and lowered cost with smaller die size and redundancy. Redundant columns are used to replace non-functional bits, resulting in significantly higher yield per wafer.

LASER PULSES VAPORIZE LINKS

We use laser pulses to open polysilicon links and select redundant columns within the circuit. This technique completely isolates the non-functional bits. Mostek is one





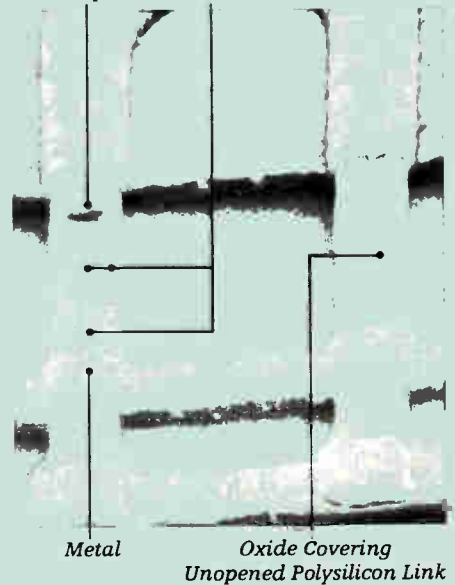
of the pioneers of this state-of-the-art process.

The MK4167 has the ideal organization, speed, and power characteristics for a broad range of applications, including main, buffer, cache, and control storage memories. With its superior performance, high density, and low cost, many new applications for this device are possible. So, once you've designed it in, you will need a supplier you can depend on to deliver next week. And next year.

That's Mostek.

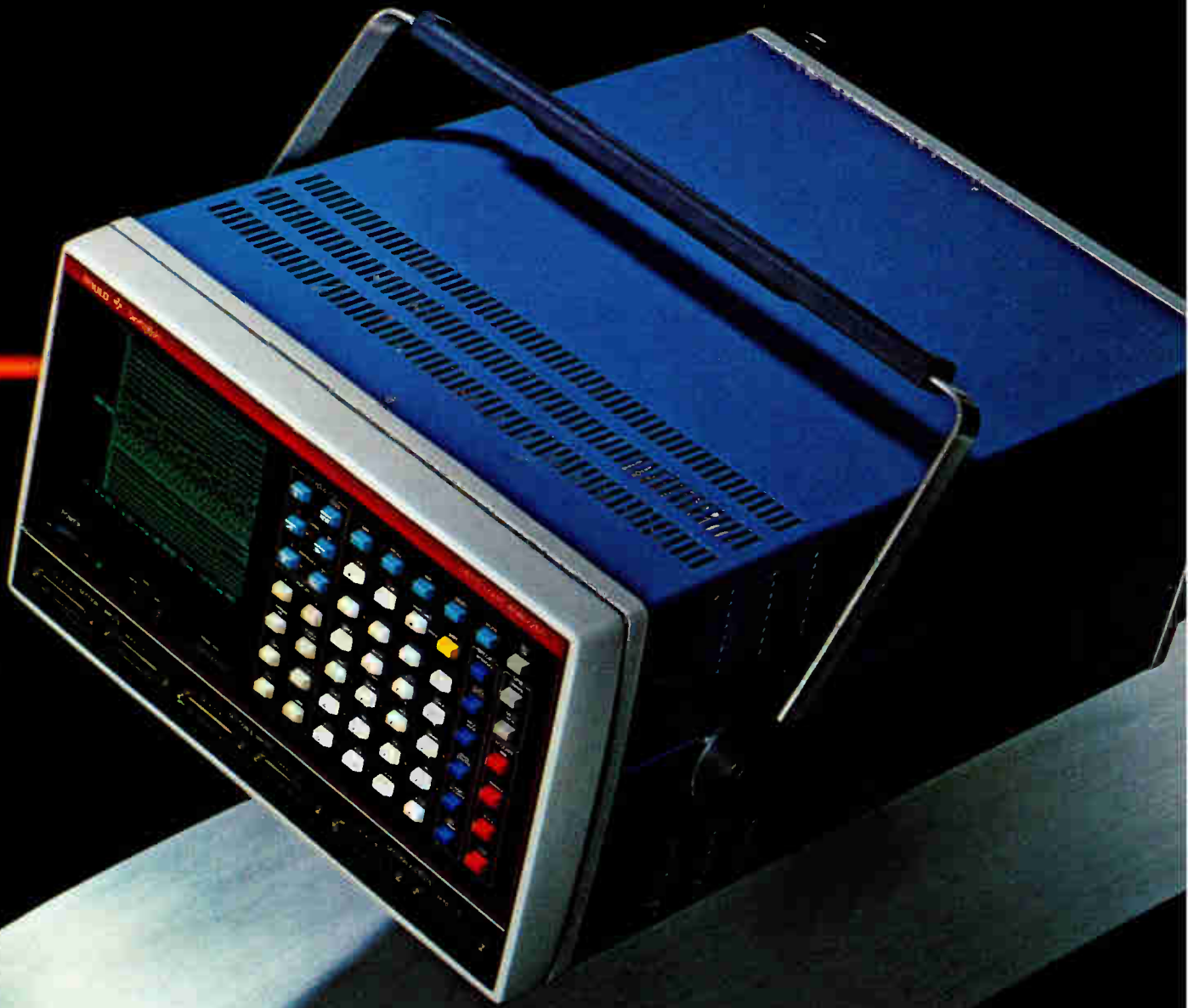
Send for more information on the MK4167. Write Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. Or phone (214) 323-6000. In Europe, contact Mostek International at (32) 2.762.18.80. In the Far East, Mostek Japan KK (03)-404-7261.

*Polysilicon
Link (opened) Oxide*



Scanning Electron Micrograph of a polysilicon link which has been opened to select a redundant column. The link was vaporized by a precision laser pulse.

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For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.

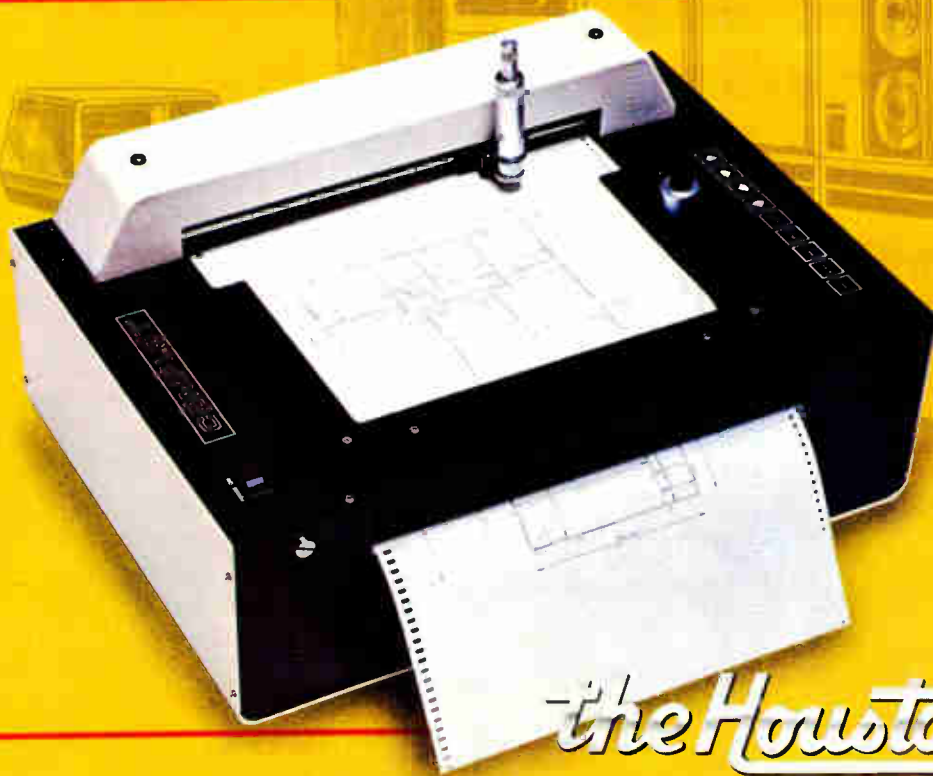


For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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30 semiconductor, computer firms form R&D cooperative

To make sure that the U.S. stays ahead of Japan in fundamental microelectronic technology, some 30 member firms of the Semiconductor Industries Association plan to form a research and development cooperative and fund it with \$30 million to \$50 million. Backers of the scheme include major computer makers, as well as heavyweight semiconductor producers like Intel, Motorola, and National. Texas Instruments, although not a member of the SIA, may sign on for the effort. **To avoid antitrust problems, the cooperative would concentrate on basic research,** giving grants to universities for specific areas of investigation like electron-beam lithography or computer-aided design. Companies would tap the research pool by sending fellows to the universities. Erich Bloch, an IBM vice president for technical personnel and development, is informally heading the effort until the SIA can find a full-time director.

16-K RAM to use RCA's C-MOS II

Look for RCA Corp. to introduce a 16-K complementary-MOS static random-access memory in the third quarter of 1982. It will be the first chip from the Solid State division in Somerville, N. J., to be produced with the 3- μ m C-MOS II process. Also in development is an advanced line of C-MOS logic tentatively called QMOS (for quick). **With approximately a 5-ns switching speed, QMOS is touted as the next generation to succeed the existing CD 4000 line.** RCA wants to work with a partner in developing the line and is currently talking with several "interested worldwide suppliers," says Robert S. Pepper, general manager.

Joining a growing trend, RCA will create an operation to build gate arrays and semicustom chips. It will be part of the integrated-circuit operation headed by vice president Carm Santoro and will be a separate profit center with its own manufacturing and engineering departments. A major decision is still being mulled over: which of the existing 16-bit n-channel MOS microprocessors to adapt to C-MOS. RCA's 16-bit entry will not be an extension of its 8-bit 1802 processor.

\$800 computer has PDP-11's power, instruction set

The first application of Digital Equipment Corp.'s new T-11 microprocessor chip (see p. 129) will be in the company's soon-to-be-announced small-board computer. The SBC-11/21 offers the basic instruction set and power of the PDP-11 minicomputer on a 5-by-8-in. board, and will sell in single units for less than \$800. Designed for firmware-driven applications, **the 11/21 interfaces with the LSI-11 bus and holds up to 8-K bytes of random-access memory and up to 32-K bytes of programmable read-only memory.** The board will offer RS-232-C and RS-423 ports, plus a 24-bit-wide parallel input/output port subsuming two 8-bit data ports and one 8-bit control port.

Board tester uses networking

Heightened productivity and flexibility in printed-circuit-board testing are the promises of Computer Automation Inc.'s new Marathon tester, which uses a network configuration. The heart of the Irvine, Calif., firm's system is a **16-bit host called the resource manager, which coordinates the activity of the remote work stations.** This processor unit runs a multitasking operating system with which users can write programs and perform functional testing, simulation, and reworking at the same time. The Marathon incorporates the company's 4900M functional tester and the Sprint simulation station.

A. B. Dick adds Basic and CP/M to word processors

Expect a series of moves soon from A. B. Dick Co. aimed at strengthening its push into office information processing, a market the Chicago-based firm has been attacking more vigorously since its 1979 acquisition by General Electric Co. Ltd. of Great Britain. Before the end of the year, the firm plans to add Basic and CP/M capability to its line of Magna III word processors. **That step will allow it to capitalize on the large amount of CP/M-based data-processing software available**, providing integrated word-processing and data-processing capabilities for its loop network architecture brought out earlier this year [*Electronics*, Jan. 27, p. 47].

Winchester tops 100 megabytes

Racing to be the first maker of an 8-in. Winchester disk with a capacity in excess of 100 megabytes, Micropolis Corp. of Chatsworth, Calif., plans to utilize **thin-film heads and other new technologies to produce a 180-megabyte drive**, scheduled to be unveiled at the 1982 National Computer Conference. It will be shipped for evaluation in the third quarter next year.

Fairchild introduces four test systems

Having been relatively quiet since being taken over by Schlumberger Ltd. more than a year ago, Fairchild Camera & Instrument Corp. made a lot of noise at the International Test Conference in Philadelphia last week. The company unveiled four test systems, the 10-MHz series 10 production tester, the series 30/333 hybrid in-circuit board tester, the 5583 memory test system, and the 5587 focused memory tester. **The 5587, which checks 16-, 64-, and 256-K dynamic random-access memories, typically costs \$130,000.** For this model Fairchild will make available "liveware:" a full-time support engineer with each system delivered to a major customer. Within a year, the company expects to introduce the series 50 general-purpose test system for very large-scale integrated circuits. It will differ in architecture from units such as those of GenRad, Teradyne, and Accutest in having fully distributed processing power rather than a large central controller. The entry-level price for the system will be around \$400,000.

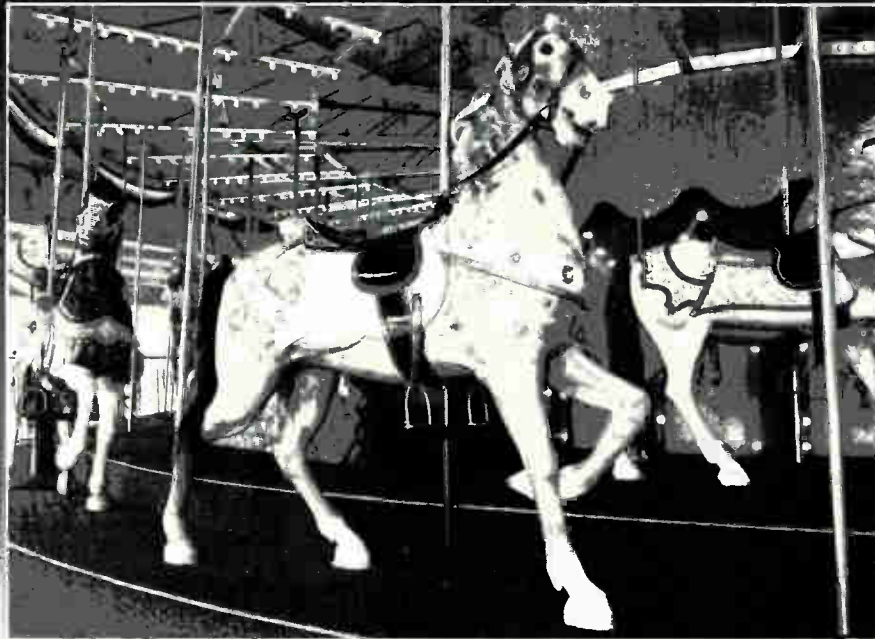
Universal field tester is coming from NCR, GenRad

NCR Corp. of Dayton, Ohio, and GenRad Inc.'s Advanced Technology division in Phoenix are developing a briefcase-sized universal field tester that goes beyond troubleshooting hardware to the component level on site **to perform software and firmware troubleshooting as well.** The tester will patch firmware with read-only memories, unload data while the system is diagnosed and repaired, analyze software remotely, and check data communications. It will also communicate time charges, repair actions, parts used, and call effectiveness to a central office.

Addenda

Radio Shack is planning to have **a 16-bit version of its home computer in its stores by next February or March.** The machine will be based on Motorola's 68000 microprocessor. At the same time, Radio Shack's Fort Worth, Texas, parent company, Tandy Corp., has signed an agreement with Matra SA of France to produce TRS-80 model III computers there. . . . Advanced Micro Devices Inc. of Sunnyvale, Calif., **is shutting its systems house, Advanced Micro Computers.** . . . Weitek Corp., the Santa Clara, Calif., semiconductor design house, **has hired Arthur J. Kollmeyer as president.** He was vice president and general manager of Calma Corp.'s Microelectronics division.

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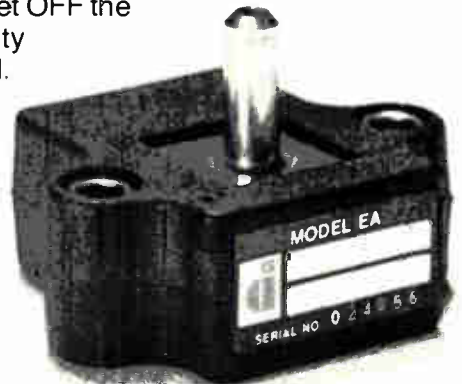
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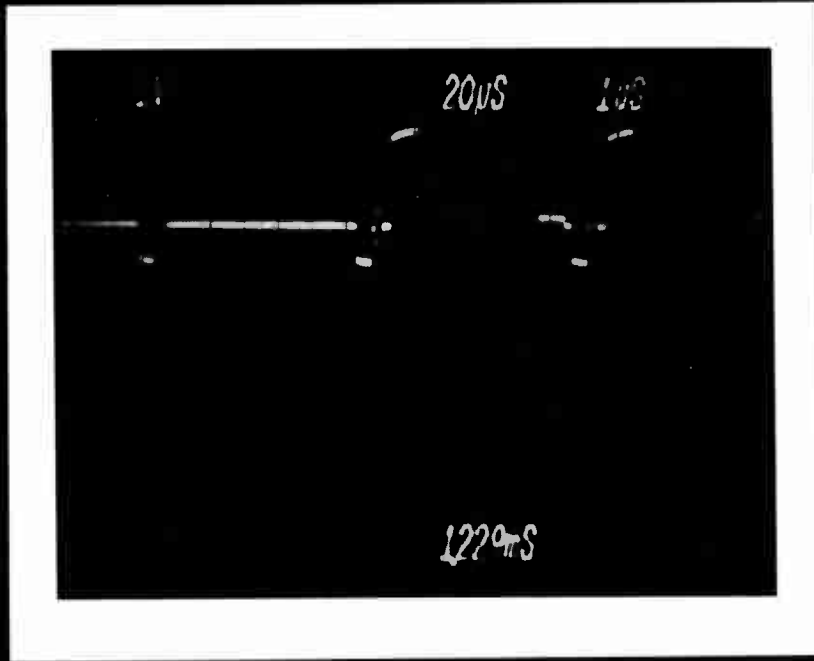
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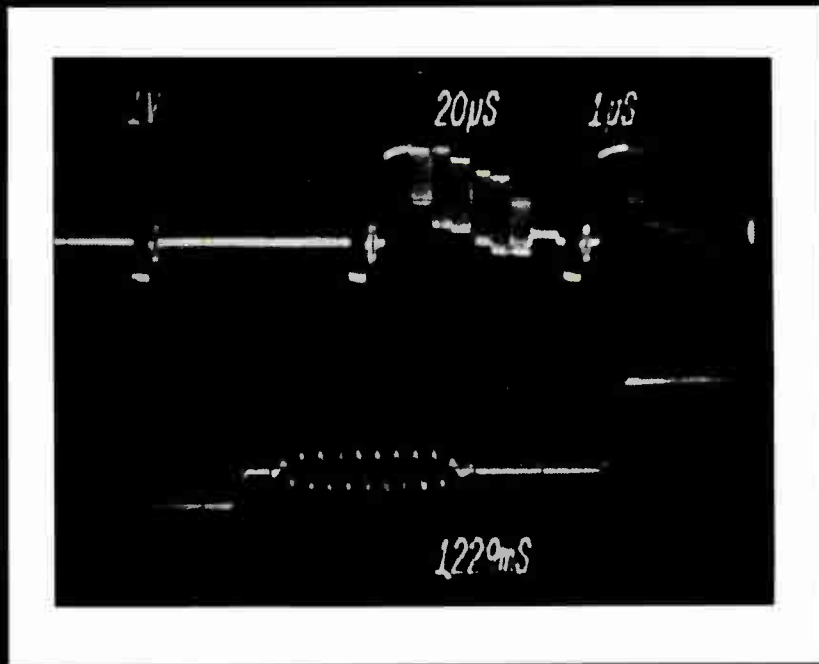
sensitive, you can record frequencies up to 420 MHz at speeds of 5 nanoseconds or less from a single sweep. And you can record with enhanced contrast, super fine detail, and good tonal separation.

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*Equivalent film speed

where our new, faster one starts.



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Circle 38 on reader service card

World Radio History

Piezoelectric bender actuates tiny relays and dot-matrix printers

by Roderic Beresford, Components Editor

Small, fast-acting drivers consume little power; they can operate blowers, electrical generators, too

The idea of using piezoelectric benders to actuate relays has been around for more than 40 years. But only this month did the first practical hardware appear, as Piezo Electric Products Inc. (PEPI) bared details on its mass-produced bending piezoelectric blade.

The benders are smaller and faster than their magnetic counterparts and need power only when switched. As a result, they have high promise as drivers for dot-matrix printers as well as for relays. What's more, PEPI foresees totally new uses for its piezoelectric devices.

At first glance, it might seem simple to devise a piezoelectric bender with enough displacement to open and close contacts. When a voltage is applied across two thin piezoelectric wafers bonded to a metal-strip core—the bilaminated assembly is commonly called a bilam—one wafer contracts and the other expands, causing the assembly to bend.

But there is a drawback to such bilams—there is not sufficient force at the end of their throw to close contacts. This is because the restoring force of the strip increases roughly linearly with the bending and causes the piezoelectric wafers to generate voltages that oppose the one applied.

Back stroke. Eric and Henry Kolm—brothers, graduates of the Massachusetts Institute of Technolo-

gy and the principal shareholders in the Cambridge, Mass., firm—found a way to overcome this lack of force by coupling the bilam to a bistable spring. The relay is designed so that its contacts stop the snap spring near its point of maximum opposing force. In effect, the bilam stalls near the beginning of its stroke, where it develops the most force. Once the snap spring changes positions, all of this force is available from the spring to close the contacts.

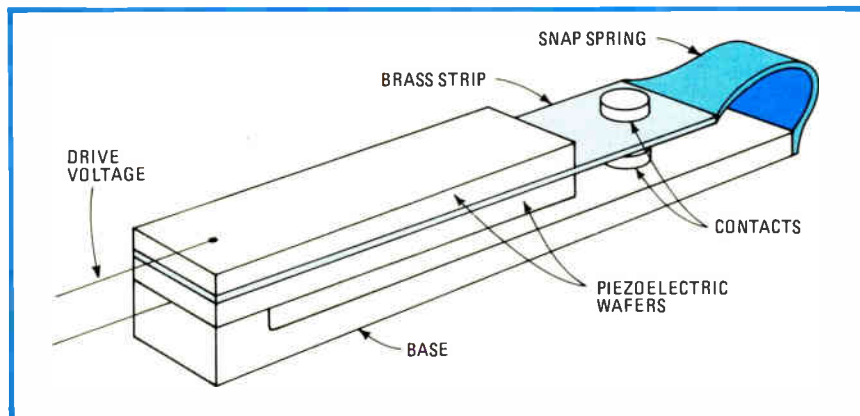
The bilam actuators range in length up to about 1 inch and in width to $\frac{3}{8}$ in. "There is nothing special about any of the materials," says Henry Kolm, PEPI's vice president for research. "We use phosphor-bronze springs and off-the-shelf ceramics"—like sintered lead zirconate or ammonium dihydrogen phosphate.

The first prototype relays need a pulse of about 40 volts to obtain a throw of 1 millimeter in 70 microseconds. Kolm thinks that "with the use of multilayer structures, this can

be reduced to around 12 v." As for size, the Kolms claim that 10 relays could be packed into a square inch by using printed-circuit techniques to mass-produce them.

Bright prospects. Because of the bender's inherent advantages, the Kolms envisage a number of totally new and in some cases eye-opening applications. PEPI already has produced working models of generators where vibrating piezoelectric devices convert auto-exhaust gases into electricity. The concept could lead to piezoelectric "windmills," as well. Other ideas are for piezoelectric blowers and quadrature motors.

In fact, the Kolms are so convinced that applications like relays and dot-matrix printers will touch off a demand for piezoelectrics that PEPI last month bought for \$1.8 million the piezoelectric business of Gulton Industries, a leading producer of synthetic thin-sheet piezoelectric materials. The Metuchen, N. J., plant is "the first in the world capable of mass-producing the thin



It's a snap. A bilam—an assembly of piezoelectric wafers and a brass strip—will bend when a drive voltage is applied. But there is not enough force at the end of the stroke to make good contact, so the bilam must be coupled to a snap spring.

ceramic wafers needed for this type of relay," claims Henry Kolm. When PEPI starts to mass-produce the relays in its new plant, they might well become cheaper than magnetic types, as well as smaller and less power-consuming.

Computers

IBM builds the first Josephson system

An entire system based on Josephson junctions, complete with chips, boards, and input and output connectors to the room-temperature world, has been built by IBM Corp. The fully functional system, operated at 4.2 K, simulates the data path of a prototype signal processor that the computer maker is developing. It exhibits a cycle time of 3.7 ns, and if current levels on the chips can be sufficiently controlled, cycle times below 3 ns should result.

The system comprises two cards with two Josephson chips apiece. The cards plug into a socket that mates with a silicon adapter having

two flexible ribbon cables for I/O connections. The bottom edge of each card contains rows of micropins that plug into mercury-filled wells on the socket; micropin arrays are used as well for socket-adaptor connections (see figure).

Lots of logic. The chips use all members of IBM's current-injection-logic series including OR and AND gates, latches, drivers, and receivers. They are based on lead-alloy junctions and were built using 2.5-micrometer design rules. Identical features are anticipated for a possible future processor, though circuit and wiring densities will be by that time probably doubled.

The four identical chips include circuitry for data flow, interfacing, and memory that is modeled with a 700-picosecond delay line. To test the system's backplane signal propagation, different circuit elements were wired on each of the chips. A low-magnetism environment avoids flux-trapping in the chips.

Power play. Power is distributed to the system through a two-level transformer. Voltage regulators on the Josephson chips clip the incoming ac waveform, transforming it

into a regulated bipolar power supply for the latching logic. The system's power supply was designed to handle 16 fully populated logic chips, however, so excess current is dissipated by dummy loads on the four chips.

The chips were selected and designed to model a critical path in the prototype processor under development, namely a jump-control sequence and a cache memory access in each machine cycle. The 3.7-ns cycle time comprised 2.6 ns of path delay and about 1.1 ns for the rise and fall of the power supply.

IBM encountered many technological problems during the experiment, and it solved most of them except current-level instabilities in the on-chip wiring. The firm also wants to take a closer look at critical super currents tunneling through the junctions. All told, says IBM, the exercise brings a sub-4-ns Josephson computer for the late 1980s much closer to reality.

-John G. Posa

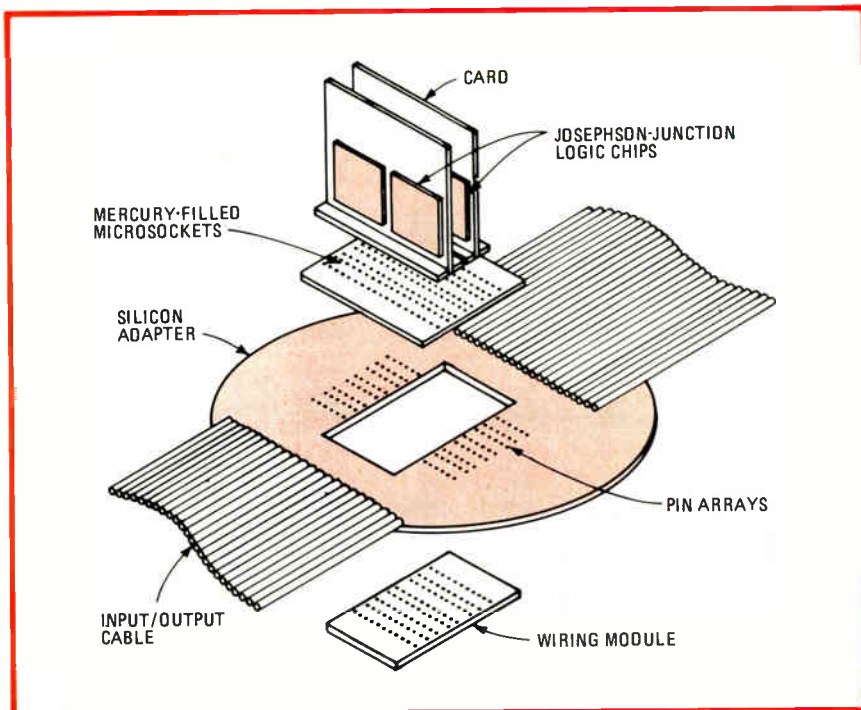
Word processing

Software lets typists key in ideographs

Word processing in the Far East, for anyone who wants to do it in the native ideograms, is a nightmare. Chinese, Japanese, and Korean have so many thousands of distinct characters that straightforward keyboards are not feasible.

Nonetheless, direct ideographic text entry from an ordinary alphanumeric keyboard is on its way. Asia-graphics, a new company started up nine months ago in Mount Sinai, N. Y., went to market in mid-October with a \$2,000 software package that makes ideographic input possible for computers with bit-mapped displays. The system comes with a stock of 4,800 characters, but that capacity can be more than doubled if the computer has enough memory.

Double code. Crucial to Asia-graphics' system are its "descriptors," five-to-seven-letter codes unique to each character. The



Inside out. To connect the cryogenic Josephson logic with ribbon cables to the temperate outside world, IBM uses arrays of micropins that plug into mercury-filled sockets.

descriptors are composed of two parts: one represents the phonetics of the character (katakana or romanji for Japanese, and pinyin or bo po mo fo for Chinese); the other part indicates the radical family to which the character belongs.

Thus, typing in T and U on the keyboard (if the system were working in English and English words were indivisible entities) would indicate the sound for "tu," which could mean "to," "too," or "two." Typing in the letter code for the phonetic representation of the radical family would resolve the ambiguity. Radical families—there are 57 of them—are familiar to literate Orientals because their dictionaries are organized that way. With a half-dozen or so keystrokes, then, even the more complex characters can be entered at a speed that is comparable to that of Roman-alphabet typing.

Sound selection. Needless to say, the Japanese and Chinese themselves also have been striving to solve the problem of entering ideographic text into computers. Nippon Electric Co., for example, tried a giant keyboard having hundreds of keys, each of which is capable of representing several characters.

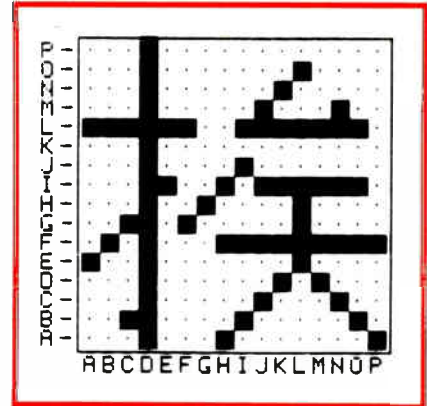
Hardware based on the Japan Industrial Standard (JIS) keyboard has been more successful, although the text to be entered has to be written in a Japanese kana syllabary text, which the computer converts into Chinese kanji characters. Toshi-

ba Corp. pioneered this approach. It has surrounded the JIS keyboard with a collection of function keys and a numerical keypad that total 105 keys, although only 58 of these are needed for text input. All the major computer and word-processor makers have adopted similar kana-to-kanji converters. Hitachi Ltd. and Ricoh Co. have word processors in which a two-stroke kana code represents each kana character uniquely. Canon Inc. has a word processor with Roman-to-kanji conversion. Another tack, taken by Wang Laboratories Inc. of Lowell, Mass., has been stroke assembly, where users compose characters from a smaller subset of possible stroke elements.

There are also phonetic-input systems. Some such systems display all the characters corresponding to a given sound, requiring the user to specify which particular one he meant; others show the most frequently used character for the input sound, so the typist has to verify it.

Quartet. The Asiagraphics software package consists of four segments, currently written in Hewlett-Packard Basic. The package will be reconfigured later for other popular computer languages.

Chief among the segments is the descriptor table. It holds the unique codes for over 6,600 characters, each needing 36 bytes. The second segment is a character and graphics data base that holds the bit patterns for over 4,800 characters.



Larger kanji store. New ideographs can be added by drawing them on an enlarged 16-by-16-element matrix. The normal-size character (not shown) is displayed alongside.

New characters can be added to these lists, even in the midst of text entry, by means of the third segment, an interactive new-character generator. With the generator, the user can define a new character by reproducing it on a large 16-by-16 matrix, using high-level, single-key-stroke commands. At the same time, the normal-sized character is simultaneously displayed alongside (see figure). In this way existing characters can be edited and new ones added to the character set on the fly.

The fourth segment is a word-processing program that ties together the other three. It allows users to insert or delete, to move the cursor, to control file storage and retrieval, to page forward and backward, to call the new-character program, and to mix text with numbers.

The original release is for the HP-85 personal computer, with others to follow. Asiagraphics sells the software alone or packaged with an HP-85 unit. **-R. Colin Johnson**

Computer-aided design

Mask layout program slated for next year

The time-consuming task of moving from very large-scale integrated-circuit design to cutting rubyliths for making masks will be considerably abbreviated next year when the Cal-

TURNING IDEOGRAPHS INTO KEYSTROKES			
Character	Type		Output
	Phonetic	Radical family	
愛	AI	TSUME	愛
哀	AI	KOROMO	哀
挨	AI	TE	挨

SOURCE: ASIAGRAPHICS

ma division of General Electric Co. delivers its first Sticks system.

The idea of Sticks—that of linking a symbolic display of an IC design to the machines making the production masks—is not new. A similar program was developed by Hewlett-Packard Co. for its own use [*Electronics*, July 31, 1980, p. 73]. But the Calma program—it gets its name from the stick-like appearance of some of its symbols—is the first to be available commercially.

Calma, in Santa Clara, Calif., claims a factor of nine or ten improvement in productivity in VLSI design when Sticks is implemented on its GDS II design system. Selling for between \$250,000 and \$500,000, this original system enables a designer to draw the masks for an IC within a grid displayed on a cathode-ray tube.

The mask data—much of it already available within the system in a cell library—is digitized and stored until the layout is completed. The data can then be used to drive the precision plotting table that draws the mask rubyliths. The 13-year-old Calma, acquired by GE last April, is the largest manufacturer of such systems, with more than 200 in the field.

More automatic. The importance of Sticks is that it relieves the designer of the responsibility for implementing the design rules while laying out the mask; rules are stored as a separate program module. Moreover, a compacting and stretching algorithm allows the designer to work freehand without the grid required previously; software takes care of the exact line spacings.

Designers will be able to switch from symbolic representation of the circuitry to a mask-level representation almost instantaneously, points out Sticks program manager Sue Schedler. "We hope to get it to the point where IC designers don't even look at mask data anymore."

To correct the ways in which a designer can go wrong, Calma also includes various checking modules. There is, for example, an "attach mode" module which makes sure that an interconnection, or wire, as it

Wang adds voice, data management

Being introduced today by Wang Laboratories Inc. are some important new capabilities for its office automation systems. Most come in a system dubbed Alliance and include the voice-handling capability predicted for the WangNet local network last summer, a data-base management system, and an image-transmission capability that employs a new printout unit.

Built around the combined word and data processor used in Wang's Office Information System, Alliance can upgrade sites already using that system. It has two types of operator terminals—one for data-base management alone, the other also including the audio capability.

The first terminal handles up to four 275-megabyte disk drives. The audio work station accepts spoken inputs, lets users edit what has been said, digitizes the messages, and then transmits them. At the receiving station, the message is recreated and spoken. As an OIS-based peripheral device, the audio work station can link up to WangNet [*Electronics*, June 30, p. 139].

The 128-K-byte main memory board in Alliance uses 64-K random-access memory chips, rather than the 16-K RAMs of the earlier OIS equipment, points out the Lowell, Mass.-based company. Another 64-K of memory supports the Alliance terminal, and 64-K more supports the work station that includes audio facility.

Alliance capabilities also include a simplified data-retrieval scheme, automatic phone dialing, and electronic mail. Other Wang entries bowing this week include several enhancements to WangNet itself and to the Wangwriter, the company's low-cost word-processing system. First deliveries of Alliance, as well as of a stand-alone version of the image-transfer system, are slated for the second quarter of 1982.

-Linda Lowe

is referred to, is small enough to fit into a port. The program also checks that the end of each wire is attached to an appropriate port, be it diffusion, polysilicon, or metal. By the middle of 1982, a "net list" program will also be available to check on the total connectivity of the design.

Primitives. Nearly any size cell can be used as a primitive, or fundamental element, in the symbolic design. Symbols for these primitives can then be laid out, hooked up, and spaced to form a new and more complex symbol. With each symbol, the program associates a set of summary polygons that display the boundaries of each layer. These borders show the extent of all data, with the spacer algorithm adjusting the design either to the edges of the display or the summary polygon.

A preliminary release of Sticks will be delivered to first customers next March. The first official release will not come until June.

Sticks will sell for about \$80,000 in single quantities. "I can see us penetrating half of the GDS II systems in the field with the product during 1982," predicts Art Kollmeyer, general manager of Calma's

Microelectronics division.

However, getting started does require some hand holding. "This is not the kind of product where we can just hand [customers] a computer tape and tell them to load it," Schedler notes. "We have to go through the types of functions in their circuits and also set [Sticks] up for their processes and design rules."

She points out that Sticks can keep track of some 64 function types—such as power lines, grounds, clock-1 and clock-2 lines, and outputs—that can be called up on as many as 64 layers. It will provide support for p- and n-channel and complementary-MOS and bipolar processes.

-Martin Marshall

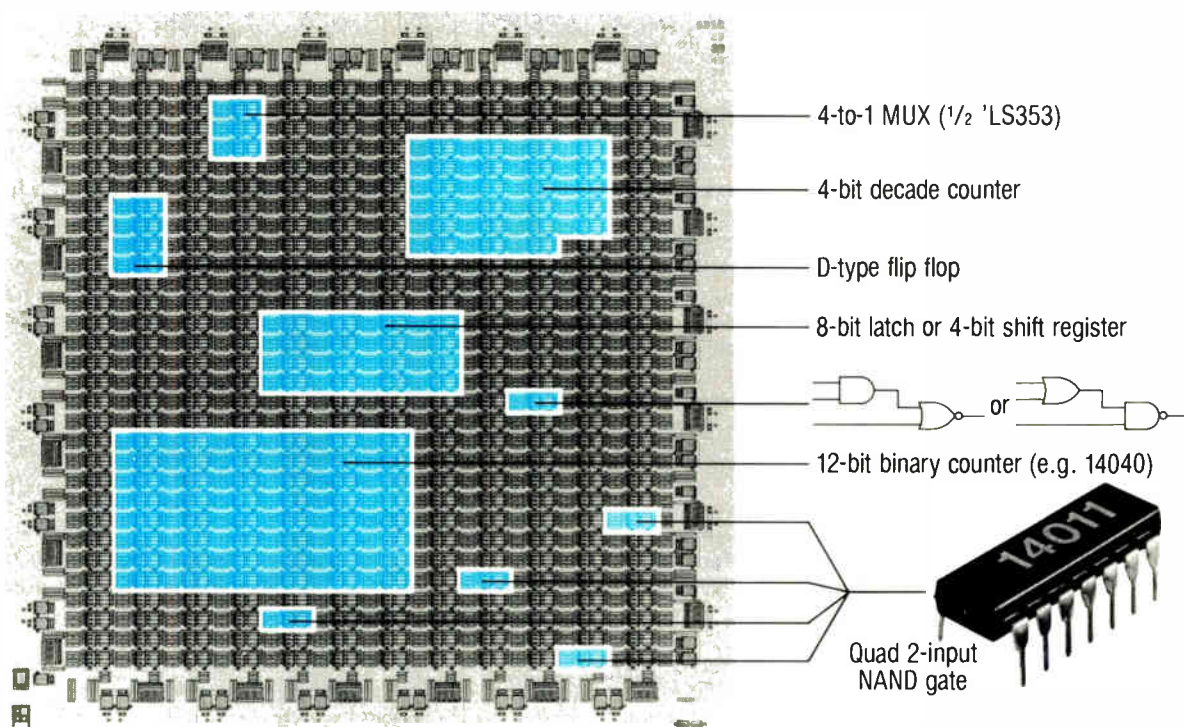
Data processing

Look-up chips check entire data base fast

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through everything—not the usual way of handling information whether in a file cabinet or in a computer data base.

But it could become a sensible way to check through data bases, thanks to the development of a custom n-channel MOS chip set by General Electric Co.'s military and data systems operation, part of the company's space division in Arlington, Va. The two-chip set implements an algorithm for matching patterns of characters in text, processing 2 million of them every second.

This sort of task is usually done much more slowly in software, points out engineering manager Dave Morris, but the GE chips do it "very, very fast." One chip is dedicated to the hard-wired logic of the text-matching algorithm. It matches up to 18 characters. For more characters, the 184-by-202-millimeter chips can be strung together in a row.

The second chip is smaller and handles the rest of the query resolution involving the logical conditions applied once a text-pattern match is found. Only one of these chips is needed per row; multiple rows can be used for processing more than one query at a time.

Four rows. GE's basic version of what it calls its text array processor has four rows of pattern-matching chips, each capable of handling 144 characters. The processor also contains a 128-K-byte cache memory that sends characters past the matching array at the 2-million character-per-second rate.

The simultaneous multiple searches at high speed of the full text of a large text-only data base has several advantages over the procedures in conventionally structured data bases. First, there are no indexes to store and maintain—all the information is searched each time at a fast, fixed search rate that does not vary with the number of users. Moreover, the data bases are easy to maintain, as information is simply added or subtracted and no time-consuming and costly processing of indexes is required.

At present, General Electric has designed what it calls the GESCAN

News briefs

IBM extends the top of its line

Playing a modified form of catch-up late last month, IBM Corp. introduced a new top-of-the-line mainframe computer, the model group K in the 3081 series, that more closely matches the price performance of machines from IBM's plug-compatible competitors like Amdahl, Hitachi, and National Advanced Systems. At about 14 million instructions per second, the new 3081 outperforms the original 3081 by 40% but still achieves only about half the instruction rate of some of the competitive machines. However, at a price of \$4.32 million for a 16-channel system with 16 megabytes of main memory, the new entry costs only 17% more than IBM's older machine. Also among its product introductions was an enhanced version of the Multiple Virtual Storage Operating System. New programs can now be run using 31-bit addressing to access up to 2 billion bytes of virtual or real memory. The operating system will also run programs using the older 24-bit addressing.

U. S. bubble supplier gets second source

The remaining U. S. supplier of megabit bubble-memory chips, the Magnetics subsidiary of Intel Corp., Santa Clara, Calif., has entered a technology-exchange pact for bubbles with Mitel Semiconductor, a division of Mitel Corp., a major Canadian producer of telecommunications equipment. The Kanata, Ont., company will become an alternative supplier of Intel's 7110 1-Mb bubble chip; later Mitel may second-source larger memories and support devices, as well.

Profits plunge, but TI eyes 64-K RAMs

Following a sluggish third quarter that caused profits to plunge 49%, Texas Instruments Inc. says it has trimmed an extra \$30 million from 1981 capital expenditures. Last summer, TI cut \$45 million from capital expenditures after laying off 3% of its workforce and dropping over a half-dozen product lines. The 1981 figure now stands at \$375 million. Net income in the third quarter ended Sept. 30 was \$27.1 million, or \$1.15 per share, compared with \$52.9 million, or \$2.30 per share, in 1980. TI says semiconductor and distributed computing operations both suffered declines in the period. Some of the semiconductor drop was blamed on start-up costs of new products, in particular the 64-K dynamic random-access-memory chip. But the company believes that the investment will be well worth the price as it ramps up 64-K production to annual rates it projects at over 7 million by the end of this year and 26 million by the end of next.

Communications industry increases capital investment

Investment in physical plants and equipment by the communications industry will increase 12% in 1982, according to William E. Gibson, senior vice president for economics and financial policy at McGraw-Hill Inc. Basing his forecast on a recent McGraw-Hill survey, Gibson sees communications industry expenditures in 1982 rising to \$31.9 billion from \$28.5 billion this year. In the nation's economy as a whole, capital goods will show a sharp expansion for 1982, with annual plant and equipment expenditures rising 16% to \$371 billion, says Gibson. The rise will be due to three factors, he adds: "a considerably stronger economic environment than this year, important tax incentives for investment and savings, and a gentler regulatory treatment of investment projects."

Las Vegas computer show looks like a hit

The Comdex computer and software show to be held Nov. 19-21 in Las Vegas could turn out to be one of the best-attended computer events this year. Touted by its promoters as the largest computer event ever, it has more exhibitors than even the National Computer Conference in Chicago in May, which attracted more than 80,000 people. Among the Comdex exhibitors are almost all the major minicomputer manufacturers, semiconductor houses, and software vendors.

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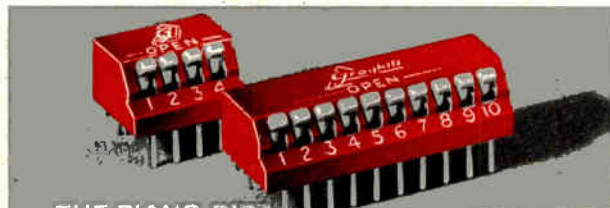
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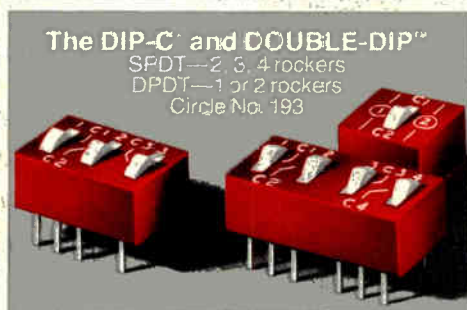
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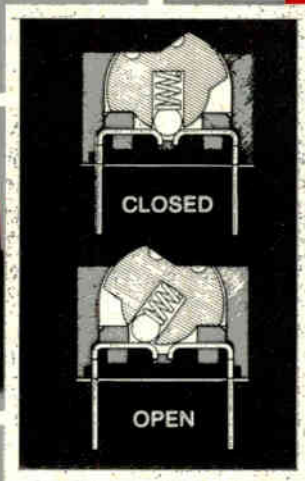


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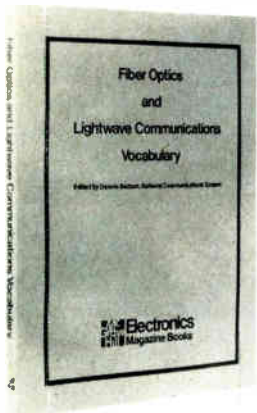
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Electronics review

2 search and retrieval system to be attached as a peripheral to the Digital Equipment Corp. PDP and VAX minicomputer systems. The basic system, including a 128-K-byte PDP-11/34, 100 megabytes of disk storage, a tape drive, printer, and one terminal, costs \$249,750. GE plans to market it initially among its Space division's present Government and military customers.

The system can be used in three configurations: as a stand-alone retrieval unit, as a back-end processor for a larger host where it can offload the information-retrieval work, or as a front-end processor. In this last setup, it can direct messages on the basis of their content in a message-handling system.

It will also be offered in a wide range of customized configurations. GE has no plans to offer the text array processor alone to original-equipment manufacturers, but company officials say they would be willing to talk about it. **-Tom Manuel**

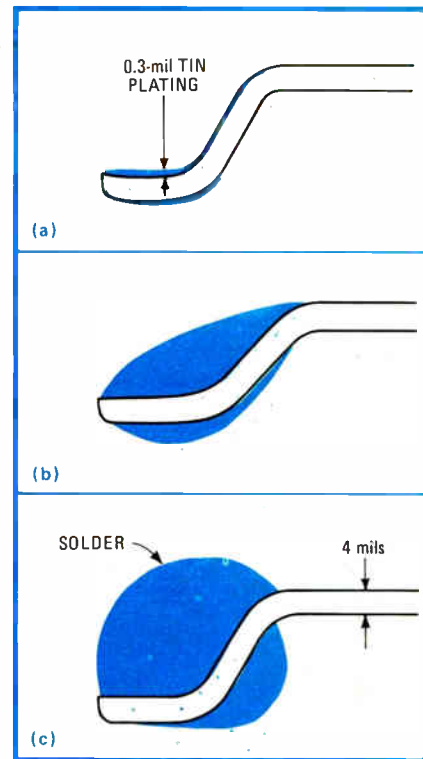
Packaging

Sized solder bumps make solid joints

A surprisingly simple controlled-solder technique has been developed to attach components to thick-film hybrid substrates solidly enough to withstand rapid thermal cycling. The new process is actually a better way of reflow soldering.

Called STAT, which stands for solder-transfer application technique, it was developed at Bell Laboratories in Allentown, Pa. Researchers Richard Kerchner, Nicholas Pannousis, and Donald Jaffe found that solder bumps that were larger than usual held up better under accelerated temperature cycling.

Ordinarily, bumps of about 0.14 milligram build up when leads of components—typically transistors in SOT-23 packages—are dipped into molten solder, usually a mixture of 60% tin and 40% lead (see figure). These bumps are normally adequate for reflow soldering these packages



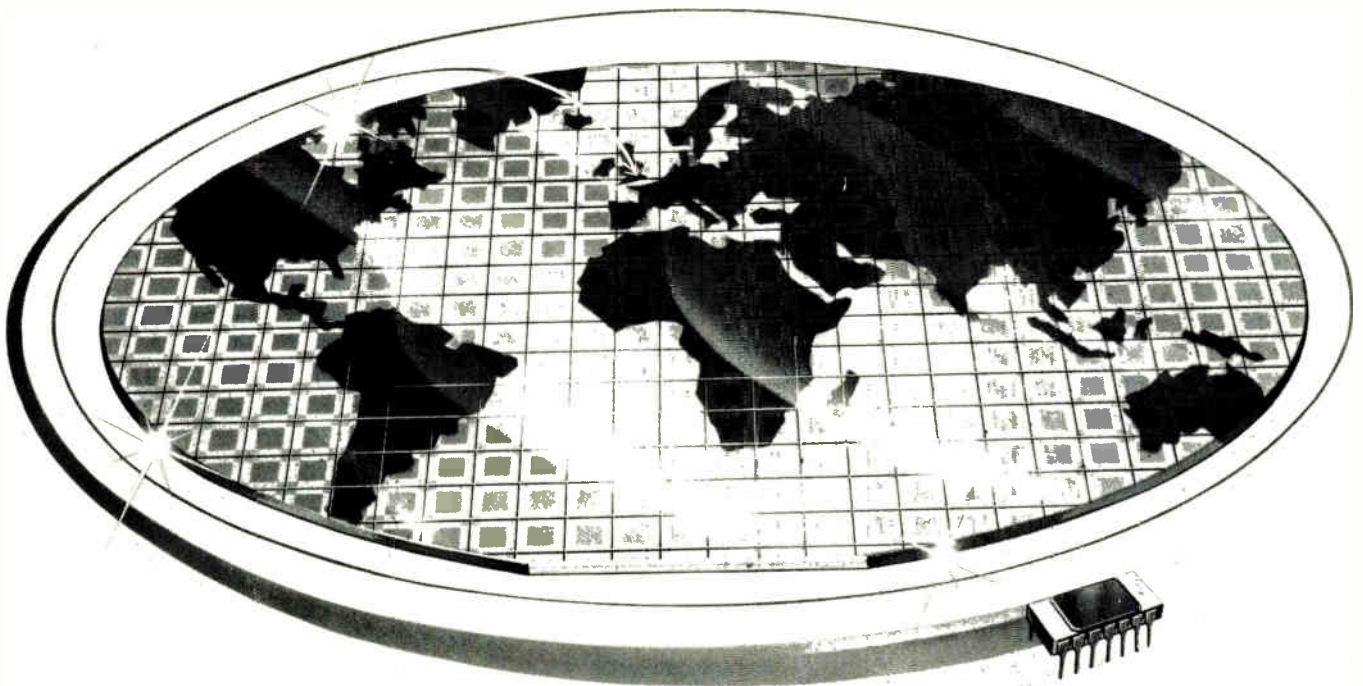
Drawing a bead. Dip a tin-plated lead (top) into molten solder and a small bump (center) builds up on it. Larger, controlled-size bumps can be had (bottom) by pressing leads into arrays of solder dots, Bell Labs has found.

on hybrid-circuit substrates, but the resulting connections often fracture under thermal cycling. Larger bumps that weigh 1 to 2 mg, the Bell Labs trio found, are more reliable in similar stress situations.

Solder dots. The STAT process they developed employs an unmetallized alumina substrate that has had an array of large solder dots screened onto it. The leads of the package are then pressed into the solder dots, the solder transferring to the leads.

Then the substrate and the devices mounted on it pass through a linear reflow furnace. The furnace is at a preheating temperature of 151°C and a reflow zone temperature of 251°C. After reflow, the components remain held in place on the substrate by the residual solder flux. Finally, the flux is removed by a solvent and the parts lifted off and dried, ready for reflow soldering to a hybrid-circuit substrate.

The bumps formed around the



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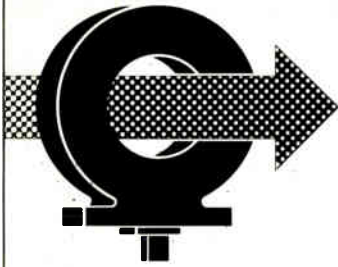
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leads in the usual solder-dip process sometimes failed prematurely after about 40 cycles at temperatures accelerated over the -40° -to- $+130^{\circ}$ C range. However, SOT-23 packages coated by the STAT process with an average of 1.5 mg of solder per lead averaged 5.7 pounds per package in pull-strength testing, according to the researchers. In fact, it was usually the epoxy package that fractured first, rather than the lead joints. Furthermore, the flat underside of the bumps facilitated the application of the components to the substrate.

STAT coating has proved successful with other components as well, including chip capacitors, ceramic chip-carriers, discrete power transistors, surface-mounted dual in-line packages, and custom packages for very large-scale integrated circuits. The procedure was discussed by its creators in mid-October at the International Microelectronics Symposium in Chicago. **-Jerry Lyman**

Microprocessors

TI's 16-bit chip bows ahead of schedule

All too often, semiconductor makers postpone market dates for complex chips. But Texas Instruments, after using a large mainframe to verify die layout and a specially built minicomputer to test it, was actually two months ahead of schedule when it announced the first chips for its new 16-bit TMS9000 microprocessor family in mid-October (see "New TI 16-bit machine has on-chip memory," p. 57).

This mainframe-mini approach to computer-aided design and debugging was a major factor in TI's achieving a fully functional chip on the first pass at realizing the design in silicon. The Dallas firm believes no other 16-bit microprocessor has holed out in one, but it expects that such first-silicon successes will become common as computerized verification of die layouts becomes widespread.

TI attributes its early 99000 success to the development of CAD tools that compare logic designs with die layout. After the 99000 design was completed and device spacings and width rules were checked by hand, the logic diagram and device sizes were coded into an IBM 370.

Comparing the logic design against the die layout, the computer discovered five hook-up errors and 212 device-size deviations that were missed during the lengthy manual calculations. Karl M. Gutttag, who headed the team that developed the 99000 architecture and logic design, says the hook-up errors were not "fatal ones, but would most likely have caused the chip not to be functional on the first pass." The 212 discrepancies in size were less serious, but probably would have affected yields, he explains.

After those errors were corrected and the layout verified again, TI produced the first 99000 prototypes. Following a successful run on pre-production test patterns, the parts were used as the central processing unit of a multiuser minicomputer specially built for testing the new device. The test system has the same power as TI's DS990/10 minicomputer, which is manufactured by the company's Digital Systems Group in Austin, Texas.

Emulator. To guarantee that the minicomputer would accurately test the 99000, its designers first constructed a full-scale, state-of-the-art emulator having about 900 medium- and large-scale integrated devices. These devices, which filled three printed-circuit boards, helped to locate possible 99000 design problems (such as prefetch overlapping and interrupts) before the first 16-bit prototype came off the line.

While plugged into the special minicomputer, the emulator ran a wide range of software correctly—diagnostic packages for three single and multiuser operating systems, as well as system and application software for these three systems.

As a result, TI discovered a few obscure design problems in the emulator that probably would not have been found until the microprocessor

NATIONAL ANTHEM[®]

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The first full spec low power op amps.

THE LINEAR LEADER STRIKES AGAIN WITH
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The only BI-FET™ op amps that offer full performance and low power operation.

Only National could provide the first BI-FET low power op amps with true op amp characteristics—and do it at such a low cost.

The Linear Leaders at National continue to set new industry standards in op amps.

This time, it's their LF441 family of low power op amps. These devices offer the same AC characteristics of the industry's currently available low power BI-FET op amps, but also provide vastly improved DC characteristics (see the Data Comparison Table below).

Higher performance for the same price.

The LF441 family—which includes the LF441 single, LF442 dual, and LF444 quad op amps—provides very distinct performance advantages over the current low power industry standards. Advantages one would expect of a true BI-FET op amp. Consider:

- low input offset voltage—0.5mV max.
- low input offset voltage drift—10 μ V/°C max.
- high gain ($V_O = \pm 10V$, $R_L = 10k$)—25k min.
- supply current—150 μ A (typ) per amp.

Yet despite these and other significant enhancements, National's LF441 family costs no more than the pin-compatible parts they now obsolete.

In quantities of 100 and up, the LF441 is now available for only \$.55,* the LF442 for \$.90,* and the LF444 for \$1.55.*

The BI-FET lineage marches on. This new family of products is a further extension of National's powerful LF4XX line of BI-FET op amps.

Other recent additions, the LF411 and LF412 (also pin-compatible with the LM741 and LM1458, respectively), are ideally suited for designs requiring superior performance specs.

Leave it to the Linear Leader to come up with unbeatable price/performance in low



LOW POWER BI-FET OP AMP DATA COMPARISON TABLE

SPEC	NEW LF441 OP AMPS	COMPETITOR'S OP AMPS	UNITS
SUPPLY CURRENT	250 (max)	250	μ A
INPUT BIAS CURRENT	100 (max)	200	pA
INPUT OFFSET VOLTAGE	5 (max)	15	mV
INPUT OFFSET VOLTAGE DRIFT	10	10	μ V/°C
GAIN ($V_O = \pm 10V$, $R_L = 10k$)	25 (min)	3 (min)	V/mV
NOISE VOLTAGE	40	42	nV/ \sqrt{Hz}

power BI-FET op amps. All others pale by comparison.

For complete information on the LF441 family and National's entire line of BI-FET op

amps, check boxes O53 and A8 on this issue's coupon.

*U.S. prices only.

BI-FET is a trademark of National Semiconductor Corporation.

The BI-FET lineage.

In 1975, the linear leaders at National made significant strides forward when they first introduced BI-FET technology. Because the op amps that resulted were the first monolithic op amps that combined low input bias current and high impedance with high speed.

This winning combination was further reinforced with each new BI-FET product introduction. The LF355, LF356 and the LF357.

Then, in 1978, these same Practical Wizards pioneered an extension of their field-proven technology: BI-FET II. The enhancements incorporated into BI-FET II include faster FETs and trimming of the input offset voltage of each amp.

The results of these efforts, beginning with the LF351 and LF353 and epitomized by the LF411 and LF412 op amps, show up in higher performance at a lower cost.

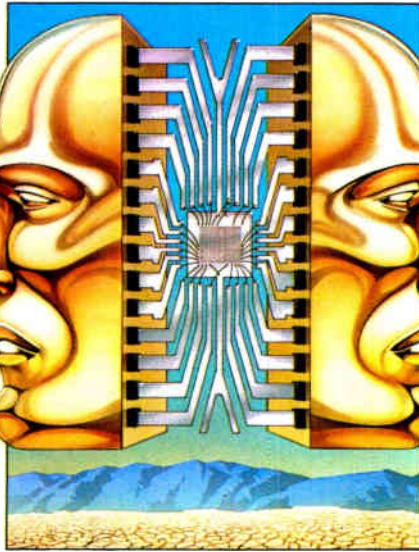
And now they've taken the same technology one step further to produce the only full performance, low power BI-FET op amp series—the LF441 (single), LF442 (dual), and LF444 (quad).

This is exactly the kind of practical innovation that has maintained National's linear leadership for over ten years.

The first single-chip dual CPU microcontroller simplifies programming.

The COP2440 makes dual CPU hardware and software implementation simple and economical.

National's new COP2440 represents the first progressive step away from the tradi-



tional "double the memory" approach to microcontroller development.

A new multiprocessor architecture* makes hardware implementation of a dual CPU microcontroller possible at low cost.

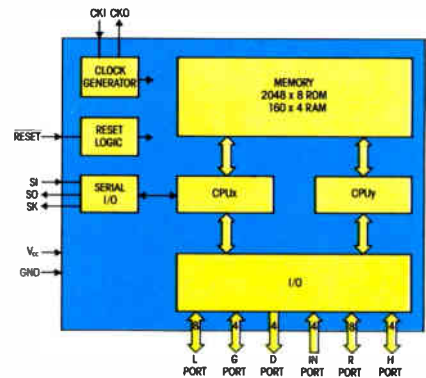
Two identical CPUs allow this latest addition to their COPS™ Family to process two simultaneous asynchronous time-critical events. The COP2440 can, for example, scan its input/output lines while processing data.

CPUs that work together. With dual on-chip CPUs, programs can now be conveniently partitioned. Regular events can be processed in an orderly manner by one CPU leaving the second free to handle random tasks as they occur.

In time-critical applications, dual CPUs allow a single microcontroller to easily work on two jobs at once.

The COP2440 features 2Kx8 ROM and 160x4 RAM, an enhanced COPS instruction set, zero-crossing detect circuitry, true multi-vectored interrupt from four selectable sources, on-chip timer/counter, a four-level subroutine stack (in RAM) for each processor, a 4ms execution time per processor, TTL/CMOS compatible I/O, and it's both

COP2440 ARCHITECTURE



MICROBUS™ and MICROWIRE™ compatible.

Software and hardware development is fully supported by National's COP400-PDS system or their STARPLEX™ systems with COPS ISE™.

To get more information, check box 098 on this Anthem's coupon.

*Patent pending.

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Volume boosted on 16K 5V DRAM production.

National's NMC5295s meet the demands of high volume users of 16K 5V DRAMs.

Engineers looking for a steady, high volume supply of 16K DRAMs are finding their source at National. The NMC5295s are rolling off the production line in large quantities and at highly competitive prices.

The NMC5295 line includes parts with access times of 120ns, 150ns and 200ns. The 200ns part is attractively priced at 1¢ per ns.

The ideal family. As the first product in their Triple-Poly dynamic RAM family, the NMC5295 offers a host of features that make it ideal for a variety of high-speed memory system applications.

The NMC5295 is configured in a 16K X 1 bit organization and is specified over the full 0°C to 70°C operating temperature range. All this is powered by a single ±5V supply.

Also, it's designed using a triple-poly memory cell structure and a folded bit line architecture. This results in a smaller die (13,000 square mils), higher performance and increased reliability.

The complete memory system solution.

National has developed a family of memory system support chips to complement its 16K and 64K dynamic RAMs. The DP8400, with expandable error checker and corrector functions, assures system integrity by detecting single or double bit errors in memory data, and correcting single bit errors. A single DRAM controller/driver chip is now available in the form of the DP8408 or DP8409.



16K 5V DRAM PRODUCTION



These support chips constitute the complete 5V-only solution for any system.

Boosting the volume on 16K 5V DRAMs.

National's technical expertise and manufacturing muscle allow them to produce the NMC5295s in high volume and offer them at very competitive prices.

To start a high quantity flow of 16K DRAMs, just call the nearest NSC field rep or distributor. For data sheets, check box A9 on this Anthem's coupon.

NATIONAL'S 16K 5V DRAMs

PART NUMBER	ACCESS TIME (ns)	REFRESH TIME (ms)	SINGLE POWER SUPPLY
NMC5295-12	120	2	5V
NMC5295-15	150	2	5V
NMC5295-20	200	2	5V

Announcing high speed PROMs—the road to faster access.

National asserts their memory technology leadership with their new highly reliable 45ns PROMs.

The Practical Wizards are expanding their family of 4K PROMs with six new high speed 45ns parts. They're the first in a series of PROMs that bring together ultra high speed and time-proven reliability.

These PROMs are Schottky-clamped for a typical address access time of 30ns and a typical enable access time of 15ns.

Their high volume Schottky production process, combined with titanium-tungsten fusing has given these PROMs their high measure of reliability.

For example, AQL's less than .03% are routinely achieved. And test results rate them at programming yields exceeding 95%.


High speed PROMs incorporate TRI-SAFE™ for low voltage programming. PNP inputs are used to reduce input loading. All DC and AC parameters are guaranteed over temperature. What's more, they're available right now in versions that offer: 512 x 8 or 1024 x 4 organization, military or commercial flows open collector or TRI-STATE™ outputs,



and N or J packages.

For quick and easy programming of these devices, National also offers their STARPLEX™ development systems with an optional Universal PROM Programmer.

Check the PROM product table below for part number, organization and T_{AA}. Then just check box number 096 on this Anthem's coupon for more information.

High speed PROMs from National—breaking the limits on fast access. 

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PROM SUMMARY TABLE

PART NUMBER	T _{AA} (MAX COMM)	ORGANIZATION
DM74S188/288	35	32 x 8
DM72S287/387	50	256 x 4
DM74S570/571	55	512 x 4
DM74S472/473	60	512 x 8
DM74S472A/473A	45	512 x 8
DM74S474/475	65	512 x 8
DM74S474A/475A	45	512 x 8
DM74S572/573	60	1024 x 4
DM74S572A/573A	45	1024 x 4
DM87S180/181	60	1024 x 8
DM87S184/185	55	2048 x 4
DM87S190/191	65	2048 x 8

The first 16K CMOS EPROMs have arrived.

National's P²CMOS™ 27C16/6716: today's memory solution for CMOS microprocessor systems.

National answers every CMOS μ P's need for high density program memory with their new 16K UV erasable P²CMOS EPROM.

It's byte wide organization (2K X 8),

single 5V power supply operation, and low standby current (100 μ A) make this new device ideal for today's and tomorrow's CMOS microprocessor systems, such as National's NSC800 μ P. Depending on their system design, users can also choose between a asynchronous (NMC27C16) or synchronous


(NMC6716) 16K version.

The NMC27C16, with its low active (25mA) and standby current, is also an excellent pin-for-pin replacement for the n-channel 2716 EPROM in power sensitive systems. It dissipates 75% less active power and has 1000 times less standby power than the 2716. This substantial power savings means higher reliability and potentially lower systems cost.

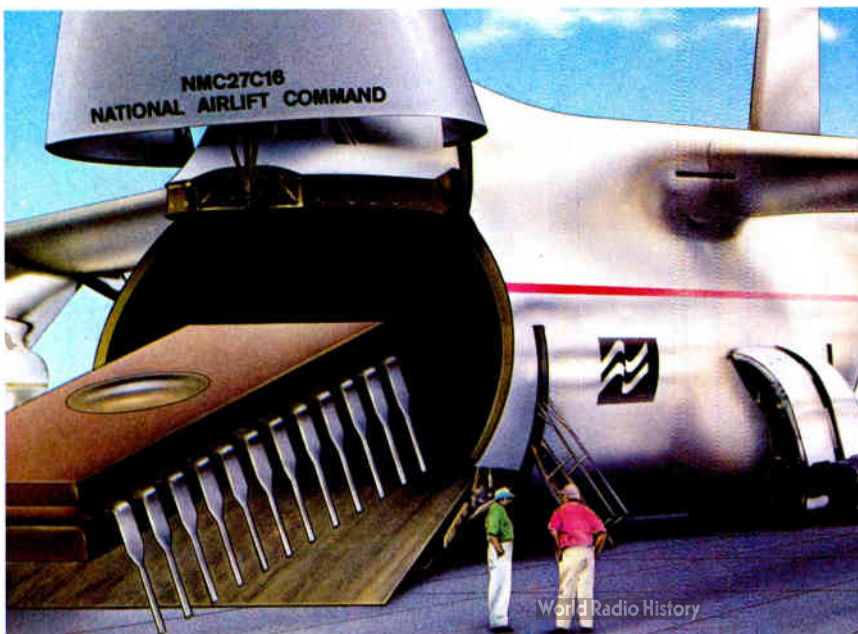
For their military customers, National will be offering both the NMC27C16 and NMC6716 in MIL-STD-883.

Both the NMC27C16 and 6716 come with a transparent lid to allow the user to erase the chip with ultraviolet light. Once erased, a new bit pattern can be programmed using National's STARPLEX™ development system with the optional Universal PROM Programmer.

To get the full story on the biggest CEPROM available, just check box B1 on the National Archives coupon.

The high speed, low power 16K CEPROM—another industry first from the Practical Wizards. 

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New Fast PALs are the quicker version of National's programmable array logic devices for low cost, space saving designs.

The leader in PAL technology has now strengthened their PAL line with the introduction of the fastest PALs yet.

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PALs were designed to replace standard TTL logic. A single PAL can replace more than 12 SSI/MSI packages.

At the higher levels of package replacement, PALs, in low volume, are now cost-competitive with the SSI/MSI parts they replace.

At higher volumes, PALs can be cost-competitive even at the lower replacement levels. This is especially true when a few more logic functions are required than a single board can accommodate.

PAL's basic logic implementation is the familiar AND-OR array, where the AND array is programmable and the OR array is fixed.

PAL's standard AND-OR logic and flexi-

ble I/O programming provides design and production efficiency unknown up to now. That's because logic modifications can be made more quickly and easily with PAL than with discrete random logic.

Field programmability made simple. Program development and debugging of PALs is supported by National's STARPLEX[™] development system with PALASM.[™]

PALASM is a new software module incorporated into the Universal PROM Programmer, as an option of the STARPLEX development system. PALASM serves as the software interface between STARPLEX and the PROM Programmer.

And with 15 different PAL devices to choose from, logic design efficiency and reliability are truly maximized.

To obtain a PAL brochure and more STARPLEX and PALASM information, simply check boxes Q25 and Q85 on this Anthem's coupon.

National—the inexpensive source for reliable PALs.

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PALASM.[™] National's new software to develop PALs.

The easy-to-use PAL assembler supports PAL programming on STARPLEX[™] the fully developed development system.

The Practical Wizards have recently introduced complete development support for their entire line of standard PAL (Programmable Array Logic) devices.

It's called PALASM—a new software module executed on their powerful STARPLEX development system. PALASM serves as the

software interface between the STARPLEX system bus and the optional Universal PROM Programmer and its associated PAL personality card.

Basically, PALASM converts PAL logic (Boolean equations, etc.) into a form that the Universal PROM Programmer can readily understand. So it can then turn around and burn that logic into the PAL array.

Easy-to-use development interface. PALASM offers the programmer a highly inter-

active easy-to-use method to develop and debug PAL logic. It does, for example, allow PAL programs to be debugged in standard PROM debug mode.

This same convenience-oriented approach to PAL programming is, in fact, carried throughout the versatile STARPLEX system.

Because in addition to PALs and PROMs, STARPLEX with ISE[™] (In-System Emulation) is used to develop, test, analyze and debug prototype hardware/software for all of National's programmables: INS8080, 8048, 8049, 8050, 8070, 8085 and NSC800 microprocessors, COPS[™] microcontrollers, and even Z80[®] μ Ps. Plus their line of board-level microcomputer products.

And now, with the addition of PALASM, STARPLEX is truly the fully developed development system.

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Meet the maker of over 100 board level SuperChip™ solutions.

National has created board level flexibility with SuperChip Multibus™ boards with a full 12-month warranty.

National has created board level flexibility the competition can't even begin to match. It's their BLC and BLX SuperChip line, with over 100 board level solutions for almost any application problem.

The Practical Wizard's entire line of high quality SuperChip products carries a full 12-month warranty—four times the industry standard.

Breadth of product versatility. National's broad line of SuperChips includes peripheral controllers, analog I/O, prototyping, extender boards, and a software operating system. For example:

- BLC-8488 high speed intelligent interface between Multibus and IEEE 488-1978 (GPIB) systems. Its 125KB/sec throughput rate makes it over 20 times faster than any other controller board available.
- BLC-0128 128K byte add-in memory card, available with or without parity. It comes with an on board 16 bit control and status register for parity storage information.
- BLC-8737 analog I/O board and BLC-8715 intelligent analog input board offer quick and easy interface with the real world for process control applications.

Building blocks—expansion modules and host boards. The broadest range of

flexibility yet is made possible by the BLX expansion modules. The modules, which measure only eleven square inches, plug directly into sockets on the SuperChip host boards (such as the BLC-80/11A, BLC-80/116 and BLC-86/12B).

Each host board will accept any two expansion modules, allowing maximum system versatility.

BLX modules are now available to expand board level capabilities with speech synthesis, analog output, fixed or floating point math, parallel I/O, serial I/O, and prototyping.

The growing BLC and BLX line allows designers an even greater latitude in innovative system designs.

BLMX-80 software: the easy way to system software development. National's BLMX-80 is a sophisticated yet easy-to-use real-time, multi-tasking executive that is supported on STARPLEX™ and operates on any Multibus board.

In addition to dramatically cutting software development time and costs over the "do-it-yourself" approach, BLMX-80 provides highly structured modular application programming. This not only makes programs easier to write, test and debug, but also easily expandable and maintainable as well.

Broadline support for any application.

National's STARPLEX development systems fully support their BLMX-80 and their Super-


Chip boards with real-time ISE™ (In-System Emulation).

Whatever the design need may be, National's BLC and BLX products are backed by a full line of support and peripheral devices including firmware, cables, connectors, accessories, system chassis, card cages and power supplies. It's the Practical Wizard's approach to meeting total system needs.

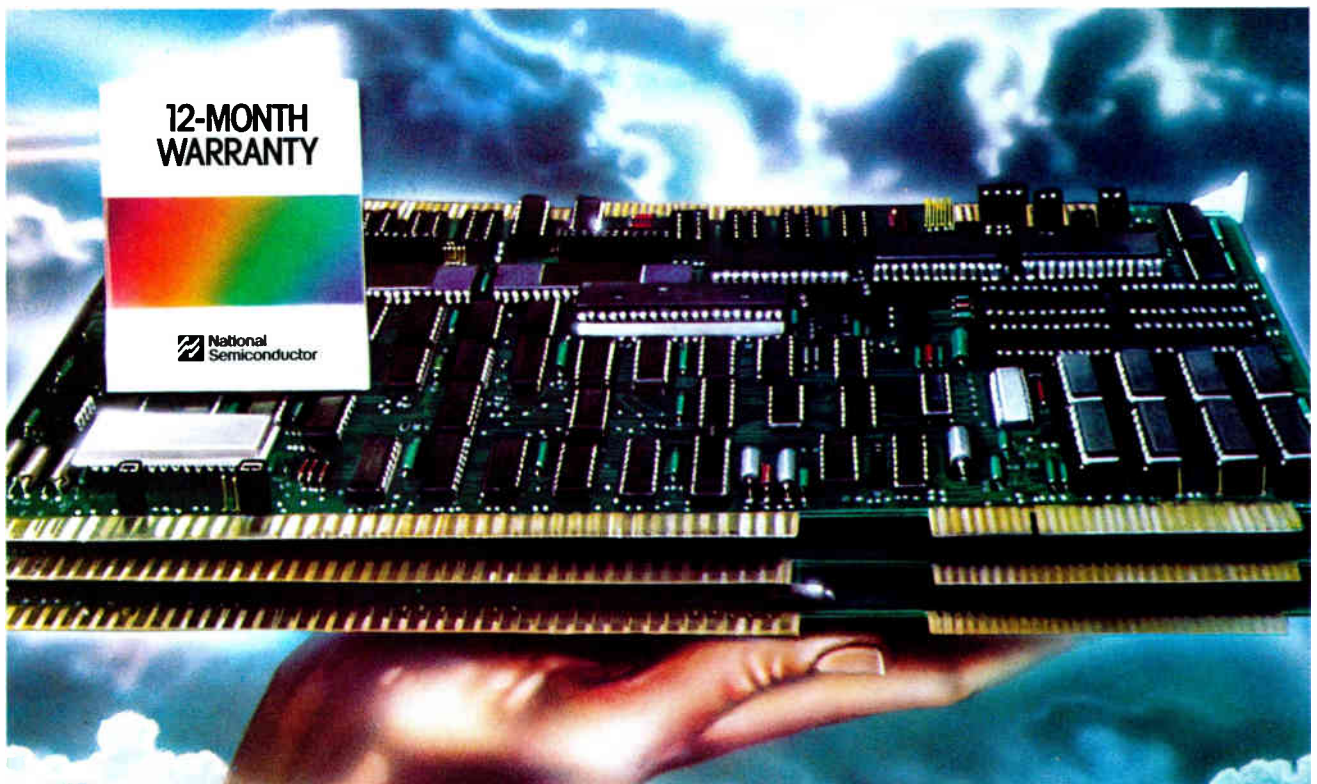
Backed by a 12-month warranty. SuperChips have testability designed in from the start by incorporating valuable test points and logic to be used during the rigid five-phase test program they receive. By applying their high-criteria test standards to each SuperChip board, National can back their boards with the confidence of a 12-month warranty.

National's established manufacturing capabilities combined with their strong Quality Assurance and Reliability test programs set them apart as a large supplier of highly reliable products from the chip up. So they're a natural for making the industry's most versatile board level products.

For more information on National's complete line of board level solutions, check box 088 on this Anthem's coupon.

BLC and BLX SuperChips. Because man cannot live by chips alone. 

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Bringing lower cost and high performance to 8-bit A-to-D and D-to-A conversion.

The Practical Wizards' 8-bit DACs and ADCs offer the lowest cost, easiest-to-use system solution for interfacing a μ P to the analog world.

As the use of microprocessors expands into low cost systems, the semiconductor industry is faced with a challenge: design low cost data interface circuits with the performance and versatility that lend themselves to a wide range of applications. Everything from monitoring system voltages to complex control and measurement.

National answers this challenge with a broad line of 8-bit A-to-D and D-to-A converters that lead the industry in price/performance and ease of use.

Two perfect examples of this leadership are their ADC0804 and the DAC0830. Both devices offer unequalled performance for a very low cost. Taken together (at 100 unit prices), National's ADC/DAC solution costs only \$7.45,* a fraction of the competitors' prices.

The specs tell the story. National's practical approach to 8-bit data conversion not only saves money, it provides significant

performance advantages as well.

Their ADC0801/2/3/4 A-to-D converters feature differential input and span adjustment, so they can replace 10-bit A/Ds in some applications. And since they're completely μ P compatible, the need for external interface components is eliminated. They also offer:

- Total Error $\pm 1/4$ LSB, $\pm 1/2$ LSB, ± 1 LSB.
- 100 μ sec conversion time.
- Narrow 0.3" center 20-pin package.
- Single +5V operation.
- Low power 20mW.
- Prices start at \$2.95.*

In addition, their ADC0808/9 and ADC0816/17 provide $1/2$ or 1 LSB accuracy and 8- or 16-channel multiplexers. Prices start at \$3.60.*

In terms of D-to-A converters, National's DAC0830/31/32 are also fully μ P compatible and can be configured for either current mode or voltage mode operation. They can even be used as system building blocks for digital control.

And like the A/Ds, these D/As allow span accommodation. They also offer:

- Linearity Error 0.05% of FSR, 0.1% of FSR, 0.2% of FSR.

- Guaranteed monotonic.
- Double latched digital data inputs.
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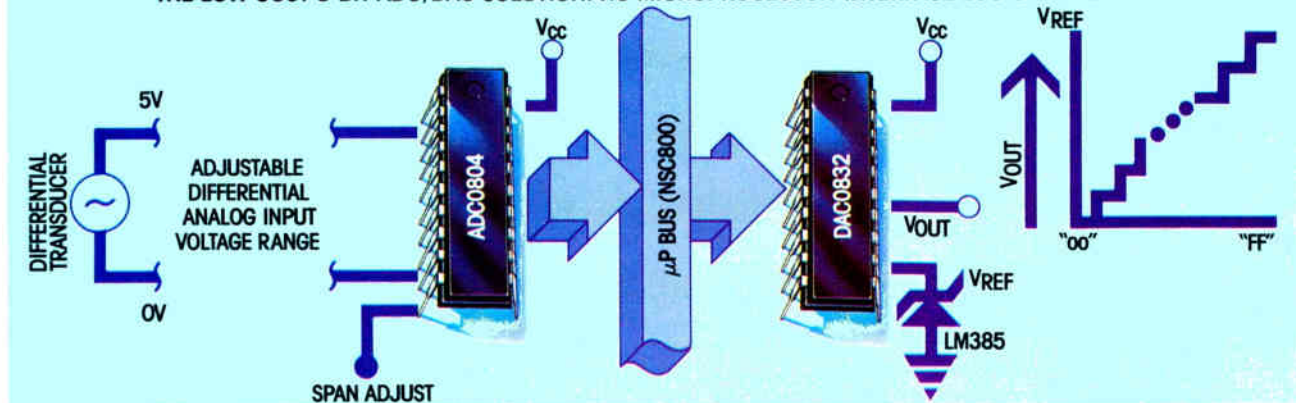
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out their manufacturing cycle. Quality is built into every part they produce—during design, wafer fab, assembly, and test.

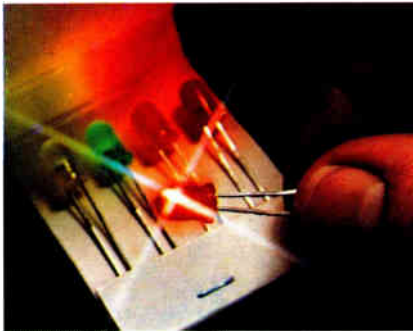
For example, the diodes built into all of their CMOS D/As and A/Ds provide superior static input protection.

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For the best in high quality Data Conversion/Acquisition components, look to National—because Practical Wizardry doesn't stop with performance.

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New MV5X5X Series cuts LED system costs.


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NA 36

New TI 16-bit machine has on-chip memory

An on-chip macrostore with 512 words of read-only memory and 16 words of random-access memory distinguishes TI's new 99000 family from its TMS9900 predecessors [*Electronics*, Feb. 24, p. 157]. Routines stored in a special location will execute up to twice as fast as those stored conventionally in main memory. The first two members of the new 16-bit family will be the 99105 base-line processor and the 99110 floating-point microprocessor, the world's first, TI maintains. The 99105 will sell for \$65 (in 100-up quantities); volume deliveries will start in late 1981. Samples of the 99110 will be available starting in December, with volume production to follow in the first quarter of 1982. Its price is \$99 (in 100-up quantities).

TI plans four other 99000 peripheral chips for early next year. **-J. R. L.**

had been introduced. Once the 99000 prototypes were ready, TI replaced the emulator with one of them and ran a variety of diagnostic programs.

-J. Robert Lineback

Solid state

One-chip optocoupler triggers triacs

There are many takers for a simple, cheap way to safely interface sensitive microprocessor logic with power circuits. So optically isolated triac drivers have become one of the few bright spots in the currently poor market for discrete semiconductors.

These monolithic emitter-detector devices trigger power-control triacs on alternating-current power lines. Previously, this ticklish job fell largely to silicon controlled rectifiers or solid-state relays, plus many out-boarded parts—a solution that is both more complex and costly.

Light touch. "They took off like a shot because without peripheral components you can hook them to a power triac and you're in business," says Marty Levy, optoelectronic product market engineer of the High-Frequency and Optical Products division of Motorola Inc.'s Semiconductor Sector. The Phoenix, Ariz., organization was the one that started it all in late 1978 with the MOC 3010-11 optically triggered triac driver, rated at 250 volts peak.

Since then, Motorola has added 400-v-peak versions that can handle 220-v ac power supplies; and last

year the division brought out a zero-crossing version, which suppresses the troubling radio-frequency noise that occurs when triacs are switched at current peaks. This version has an isolation-voltage rating of 7,500 v and a breakdown rating of 250 v.

Applications are multiplying in such equipment as industrial controls, traffic lights, scoreboards, and vending machines, where microprocessors have rapidly taken hold. As a result, there is a scramble among suppliers to nail down design-in positions. Some second-source competitors are General Electric Co., which dominates in SCRs; TRW Inc.'s Optron; and Theta-J Corp.

One customer that already has the coupler in its equipment is Traffic Sensor Corp., Corona, Calif. "We needed a coupler device for years as an interface immune to noise," says Ramey Metz, vice president for engineering. The firm's traffic signals draw from 10 to 20 amperes off a 120-v supply and must meet a two-year warranty. Thousands of the signals are now in operation, he says.

Trigger. Motorola will roll out a new kind of trigger this month, the MRD920 120-v, which has a transparent plastic housing. Levy is enthusiastic about its potential because equipment makers can control ac power loads by shining their own remote light sources on the trigger.

The takeoff of the coupler triac driver line has not escaped the notice of Motorola brass. They look for 25% compound growth through 1985 in the market, which now amounts to some \$72 million annually.

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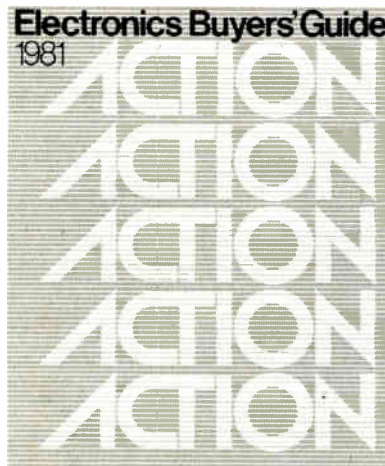
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Electronics review

rollton, Texas, officials also see vast potential for the optical devices. The debut of its line early this year, in fact, triggered a best-ever initial response to a product. The 120-v and 240-v Optron drivers, carrying part numbers identical to Motorola's, will soon offer the key zero-crossing feature. **-Larry Waller**

Personal computers

DEC has high hopes for VT18X option

All the major computer makers have their eyes on the desktop computer market, but none—except, as always, IBM—has launched a personal and small-business computer with as large an inherent potential customer base as Digital Equipment Corp. has for its new VT18X. Introduced in mid-October, the \$2,400 conversion module that includes two 5¼-inch floppy-disk drives plugs directly into DEC's VT100 display terminal to convert it into a CP/M-compatible personal or small-business computer [*Electronics*, Oct. 20, p. 33].

Other than exploiting its 250,000-unit VT100 base, DEC's reasons for launching the VT18X were twofold. "First, we didn't want our customers to have to buy something from the likes of Apple for small-scale computation; we want them to be able to be one-stop shoppers with brand loyalty to DEC," says one marketer at the Maynard, Mass. firm.

Secondly, a VT18X-equipped VT100 does more than offer small users easy entry into DEC's product line—and DEC a foothold in an explosive market sector. It is also a growth path into more powerful DEC products, including VT100 variants, which may emerge from the company in the next few years.

Sure thing. Success of the VT18X seems certain. Inquiries poured in right after it was announced, and DEC officials think they could total 100,000 for the first month. To handle them, the company has installed hot-line phone banks to take care of established customers and to shunt

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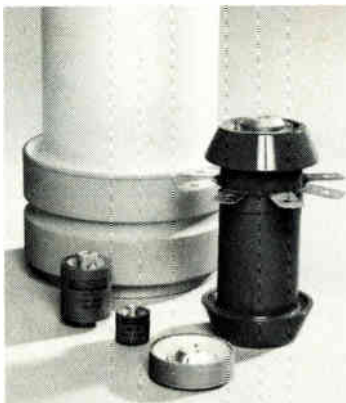
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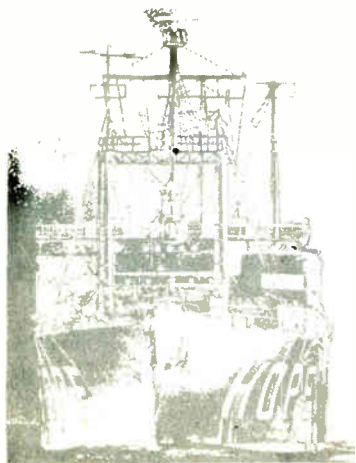
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Electronics review

new customers to its distributors and retail outlets. "The economy would almost have to implode for this thing to fail," says one small-computer market watcher.

A VT100 fitted with a VT18X module can change its personality from that of a computer terminal to that of a free-standing 8-bit micro-computer with a single keystroke. However, data generated while the machine is operating on its own cannot be directly injected into an associated DEC computer system because of operating-system and file incompatibilities. The VT100 must be in its terminal mode for such communication. DEC is working on the protocols to solve this problem, but has yet to commit itself on availability.

Processor changes. The market watchers already are speculating about 16-bit versions of the VT18X. Allen G. Hueffner, manager of planning and product marketing for DEC's terminals group, says that nothing like that is yet in the cards, but notes that "versions of the option with a variety of [microprocessor] engines" are plausible.

Some observers wonder whether DEC might not come out with a 16-bit system compatible with the 8088-based IBM personal computer. Others ask whether an independent supplier might not offer a similar product to VT100 users now that DEC itself has broken the seal on the terminal as a market area.

Also, DEC watchers, aware of the PDP-11 on a chip just being announced (see p. 129), anticipate a scenario in which a PDP-11-class microcomputer would slip into a VT100 as easily as the VT18X.

DEC's Arthur T. Campbell, terminal products group manager, says that the company designed the VT100 with an extra large power supply, accessory ports, and the space to accommodate upgrade options such as integral intelligence. It does not take much imagination to anticipate that some of the advanced very large scale integrated circuits now coming out of DEC's Hudson, Mass., IC facility will eventually appear in options that are similar to the VT18X. **-James B. Brinton**

SCIENCE/SCOPE

A new photochemical vapor deposition process forms oxide layers on selected substrates at low temperatures. The Hughes PHOTOX™ process deposits silicon dioxide and other oxide dielectrics on semiconductor devices, and coats temperature-sensitive electro-optical components. The oxide forms when chosen gas phase reactants absorb selected wavelengths of light. A significant advantage of this process is that it's free from charged species that can damage the substrate. Because it is done at low temperatures (50° to 300°C), it is useful for making certain kinds of solid-state devices. The process has been used to form pinhole-free dielectrics for temperature-sensitive elemental and compound semiconductor materials, as well as optical coatings for plastics. The PHOTOX process is available for non-exclusive licenses.

Better and timelier weather forecasts will be possible when a microwave sensor is launched aboard a military satellite in the mid-1980s. The instrument will tell how hard rain is falling in a specific area rather than simply how much has fallen over a wide area within 24 hours. It also will determine wind speed, atmospheric water content, soil moisture, and sea ice conditions. Because the satellite will follow a low polar orbit, the sensor will gather important data on the little-studied polar regions and oceans. Hughes will soon deliver the prototype Special Sensor Microwave/Imager to the U.S. Air Force.

The U.S. Forest Service is using satellite pictures to monitor and manage national forests. The agency has gotten detailed views of its lands from NASA's Landsat 2 spacecraft. Landsat data can be adapted by computers to create false-color maps for categorizing different vegetation and ecological zones. The pictures, covering an area about 115 miles square, help the Forest Service measure changes in the growth and health of forests. Tests begun in South Carolina last year are to be followed by a complete inventory of Idaho's forests in 1982. Landsat 2's electronic camera, a multispectral scanner, was built by Hughes.

The Manufacturing Division of Hughes Missile Systems Group in Tucson has many immediate openings for engineers. These career opportunities require expertise in designing test equipment for advanced major electronic and missile system programs. Openings range from digital logic, analog, and IF/RF circuit design to electro-optical and IR system design. Also needed are industrial engineers and manufacturing production engineers. For immediate consideration, send your resume to Engineering Recruitment, Hughes Aircraft Company, P.O. Box 11337, Dept. SE, Tucson AZ 85734. Or call (602) 746-8925. Equal opportunity employer.

A millimeter-wave radar has demonstrated its ability to track targets and guide missiles accurately through smoke and rain. The radar, under study because it has more resolution than conventional radar and can penetrate adverse weather better than infrared, was used to guide TOW (Tube-launched, Optically tracked, Wire-guided) missiles to stationary targets. In three of the successful launches, the target was obscured by heavy smoke and aerosols. In one of those, visibility was further deteriorated by rain. The demonstration was conducted by Hughes for the U.S. Army and the Defense Advanced Research Projects Agency.

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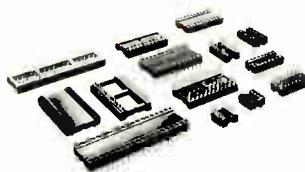
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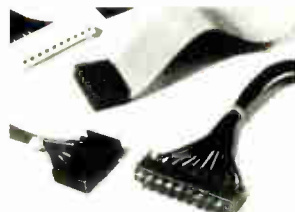
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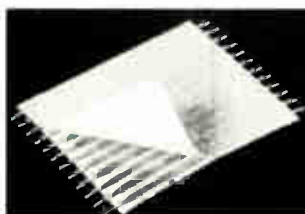


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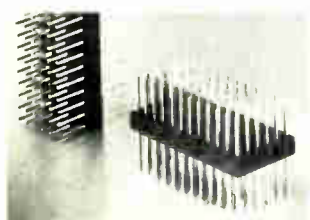
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Congressional report hits lack of U. S. data policy . . .

Despite the explosive growth of U. S. computer technology and the information systems that use them, the Federal government has failed to evolve a national policy to monitor and protect the interests of builders, users, and consumers of such systems, much less the individual subjects of data banks. That warning to Congress by its Office of Technology Assessment highlights a recently issued 166-page study, "Computer-Based National Information Systems." Not only is there "neither a strong trend nor sentiment among policymakers in favor of a uniform Federal information policy" that would encompass all the problems in the 14 principal areas of law and regulation that could arise from the use of data systems, says the OTA, but there is also **"a lack of congressional focus on information policy as such, and consequently the emerging issues are not being directly addressed."** Nevertheless, "there are numerous laws and regulations, some overlapping or actually conflicting." During the 95th Congress in 1977-78, the study notes, "74 new public laws emerged dealing with some aspect of information law and policy," while the most recent listing, in August 1980, showed nearly 100 computer and telecommunications projects going on or completed in the preceding six months by four congressional agencies.

. . . as absence of software R&D is criticized

The analysis by the Office of Technology Assessment also expressed concern over the absence of broad-based Federal research and development support for computer technology and the concentration of the bulk of that funding within the Department of Defense. It also decried the limited attention being paid by the Government to what it called "the software bottleneck," **while an increasingly competitive Japan has assigned that problem a high priority.** "An important issue is whether research in the applications of computer technology to problems in the civilian sector—in such areas as education, health, transportation, environmental quality, and job safety—is receiving adequate Federal support," says the OTA study.

Moreover, "eliminating software bottlenecks may be the key to maintaining the [U. S.] lead in computer technology in the coming decade. In Japan, for example, the software problem has now been given a very high priority for R&D. In the U. S., although a few defense agencies are investing in research to solve some of the problems, Federal R&D budgets for computer science and technology have not accorded software a similar priority." Citing private industry as the source of most software activity in the U. S., the OTA notes that "reportedly, one third of the research at Bell Labs is devoted to the software problem."

U. S. warns Japan to import more

In one of the Reagan Administration's toughest warnings yet to Japan to open its market, Secretary of Commerce Malcolm Baldrige told a Tokyo investment group that it faces a rising mood of protectionism in the U. S. and Europe. Baldrige said American unemployment will soon rise to the 8% level prevailing in Western Europe in the face of declining industrial production, **creating "almost laboratory-perfect conditions for protectionism."** Compounding that threat, he said, is the fact that Japan's 1981 trade surplus with the U. S. will reach an all-time record of \$15 billion. A simple projection of existing trends "show the U. S. could be running a \$50 billion deficit with Japan by the end of the decade" unless that country, the free world's second largest economy, increases imports of manufactured goods.

FCC reverses field, approves domsat use outside U. S. . . .

In a major policy reversal that may put the U.S. in conflict with Intelsat—the international telecommunications satellite consortium—the Federal Communications Commission has unanimously approved the applications by nine U.S. companies to use American or Canadian domestic satellites for transborder services. Since 1972, the FCC has refused to permit use of domestic satellites for data and television communications services outside U.S. borders. **The recently approved long-standing petitions must now be coordinated with Intelsat**—which might regard the FCC action as a breach of the 1971 treaty designed to protect the Intelsat global system from significant economic harm. The petitions also must be approved by the Canadian government and Canadian carriers, which will operate earth stations.

. . . with SBS, ASC seen as chief beneficiaries

U.S. companies whose petitions were approved include Satellite Business Systems and American Satellite Co., **which want to extend their customers' private integrated digital networks to their business sites in Canada.** Other corporations that seek authority to send or receive TV programming to or from points in Canada, the Caribbean, and Central America are RCA American Communications, Eastern Microwave, Southern Satellite Systems, Satellite Signals Unlimited, United Video, 220 Television, and Visions Ltd.

Military boosts to increase jobs for engineers by 3%

Jobs for engineers and scientists in U.S. aerospace industries are expected to rise by 3% to 202,000 from the 1980 level by year's end after holding steady during the first half of 1981. The upturn is expected to continue at the same rate through 1982 as a result of the Reagan Administration's military spending increases. **These increases more than offset the decline in jobs in the civil aviation industry** that "mirror the pressure on commercial airlines' profitability, high interest rates, and increased competition from abroad." That forecast by the Aerospace Industries Association of America is based on a survey of 51 member companies. Engineering and scientific jobs at missile and space companies and other aerospace-related product producers are both projected to rise 6% this year, says the AIAA. While aerospace-related product employment is forecast to continue that rate of growth in 1982, missiles and space producers see a slower growth rate of 1.2% next year.

B-1B cost boosts anger senators

Senate anger among both Republicans and Democrats is rising at increasing reports of cost overruns in military weapons. At the end of October, it focused on the Rockwell International Corp.'s B-1B manned bomber program for the Air Force. At a hearing of the Governmental Affairs Committee, Pentagon witnesses testified that the 100-aircraft program approved early in the month by President Reagan may incur additional research and development costs that Sen. Carl Levin (D., Mich.) says **could add another \$500 million to \$1 billion to the program.** Arkansas Democrat David Pryor says total B-1B project cost estimates now range between \$20 billion and \$30 billion, compared with contractor estimates early this year of less than \$12 billion. The disclosures should provide even greater support for the move by Sen. Sam Nunn (D., Ga.), a strong supporter of military programs, to require program cancellations or cutbacks of those with excessive costs.

ECONOMISERS



Sprague SIP/DIP Thick-Film Resistor Networks Minimize Space and Cost

Sprague networks help you to economize on space, time, and money. For example, Type 420C SIP networks require only 0.006 to 0.011 sq. in. per resistor—and at prices less than 2.5¢ per resistor in volume. Type 914C-916C laser-trimmed resistor networks contain up to 28 resistors in a standard 16-pin dual in-line package. As a result, Sprague SIP/DIP Thick-Film Resistor Networks reduce indirect costs associated with component count, inventory level, and assembly.

To economize on time, these precision molded networks have the dimensional uniformity required by automatic insertion equipment. They are supplied in anti-static magazines which also provide protection and ease of handling.

You can optimize for product cost, circuit configuration, number of resistors per package, system size, power requirement, and assembly cost, by choosing from over 900 standard networks in more than 30 circuit designs.

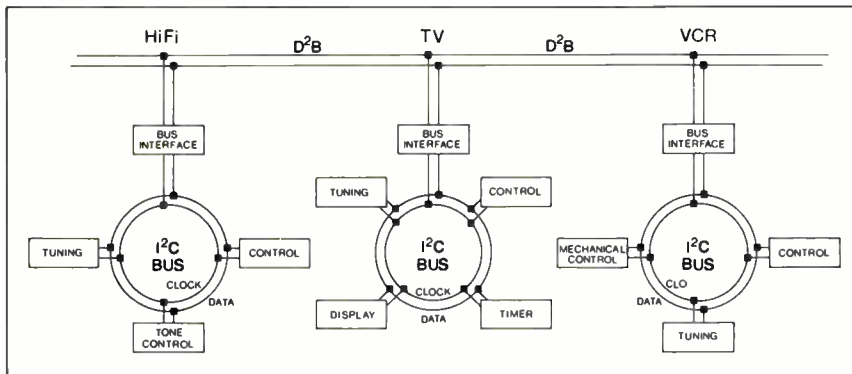
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NEWS FROM PHILIPS

NEW BUSES TO SOLVE CONSUMER PROBLEMS



General concept of bus system

Two new digital buses solve consumer problems in connecting together different pieces of home entertainment equipment.

The Domestic Digital Bus (D²B) will enable a consumer to extend his system by connecting up to 50 units together without having to consider any of the technical aspects. The Inter-IC bus (I²C) will connect together the ICs or modules inside of the equipment, and at the same time generate and process messages to and from the D²B.

The buses will be welcomed by set-makers, too. VLSI circuits are developed and manufactured as building bricks, each designed to perform very specific functions. The setmaker therefore has to combine these functions in his equipment, and he is also faced with problems if the interface between units is not standardized.

A large number of ICs for use with the I²C bus, some dedicated, are either available now, or in development. We foresee that these two buses will have an important role to play in the equipment designs of the next few years.

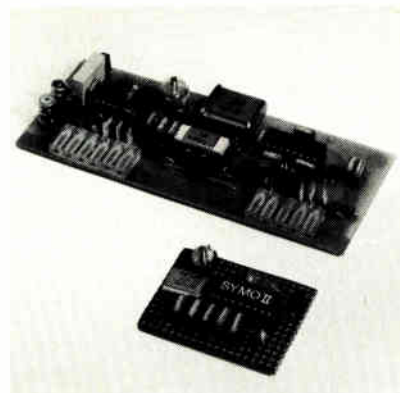
SYMO II SINGLE-CHIP SYNTHESIZER

Our new SYnthesizer MOdule SYMO II now incorporates all the synthesizer functions for digital tuning of a radio receiver on a single LSI chip. SYMO II uses one SAA1057 IC and 16 external components to replace the previous system which had three ICs and 67 external components. Current consumption is now typically 20 mA, against 100 mA of the nearest comparable system.

A wide variety of control systems can be connected to SYMO II to suit the individual requirements of the cost-conscious set maker. A SYMO II system is modular; it enables the signal sections of the tuner to be mounted close to the tuner, and the control and display sections to be mounted close to the keyboard and display on the front panel. This keeps radiation to a minimum, and reduces

wiring and screening costs. It therefore saves the designer money, and spares him grey hairs.

SYMO II is simple to use in all-elec-



Size comparison of SYMO II (bottom) and SYMO I.

tronic radio tuning systems in which the F.M. and/or A.M. sections are varicap tuned. Digital tuning in a radio replaces costly moving parts such as tuning capacitors and potentiometers by electronic circuits; thus saving space, increasing reliability, and also allowing a broad range of additional features to be included in the receiver.

SYMO II combines a prescaler, synthesizer and loop filter amplifier; all of these functions used to be performed by separate ICs. The tuning section of SYMO II contains two high-sensitivity preamplifiers and frequency dividers for A.M. and F.M., and a phase-locked loop synthesizer which can be directly programmed. The chip has a single reference frequency for both A.M. and F.M., and the programmable counter gives a choice of two tuning steps: 1 or 1,25 kHz for A.M. over a frequency range of 0,5 to 32 MHz, and 10 or 12,5 kHz for F.M. over a frequency range of 60 to 120 MHz. The chip size of the SAA1057 is 14,4 mm².

CIRCLE 51 ONREADER SERVICE CARD



Electronic Components and Materials

NEWS FROM PHILIPS

800 V DARLINGTON IN SOT-93

The 800 V Darlington transistor BU826 can be driven directly from bipolar IC logic. The BU826 has a total power dissipation of 125 W, and is suitable for both consumer and industrial applications.

When the BU826 is used in the SMPS of a colour TV, it eliminates the need for a separate driver transformer. This, together with the low mounting costs associated with the SOT-93 clip-mounted package, gives a large cost saving to the TV manufacturer.

The BU826 is a Darlington version of the BU426. The new transistor has an I_{CSAT} of 2,5 A for a collector voltage of 2 V and a base drive of only 55 mA, instead of the 500 mA drive required by the BU426.

CIRCLE 52 ON READER SERVICE CARD

HIGH RESOLUTION 90° DGD TUBES

Following the successful introduction of our high resolution 110° picture tubes, we now announce a range of 9" and 12", 90° narrow-neck tubes. The improved sharpness of these new tubes makes them especially suitable for highly readable 1000 to 2000 character displays for use in word processors, small business computers and stand-alone monitors.

These new tubes complete Philips high-resolution range of Data Graphic Display tubes. The 9" M24-306/307 and 12" M31-335/336 tubes have a neck diameter of 20 mm, and give a resolution of approximately 1300 lines; more than 50% higher than the previous models. There is a choice of four different phosphor layers, and optional anti-reflective treatments are also available. Circuit designers are given full support with a comprehensive range of wound

DUAL TRANSCONDUCTANCE AMPLIFIER

High quality noise reduction systems can be built at low cost using a Signetics NE5517 dual operational transconductance amplifier. The high signal-to-noise ratio, large bandwidth and excellent linearity make the NE5517 suitable as an amplifier for all types of electronic music equipment (including electronic organs, synthesizers and guitars) and hi-fi amplifiers. It is for example recommended as the preferred circuit in the Dolby HX* (Headroom Extension) system. The NE5517 is also suitable for multiplexers and timers in instruments and industrial equipment.

The NE5517 has a high typical transconductance g_m of almost 10 000 micromhos, and linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to a 0,5% THD. The NE5517 therefore has sufficiently high performance to be used in studio applications such as high-quality tape recorders, where its constant-impedance buffers give excellent tone burst handling.

The NE5517 accepts a supply of ± 18 or ± 22 V. Power dissipation is 570 mW. Common mode rejection is typically 110 dB, open-loop crosstalk is

100 dB for 20 Hz to 20 kHz, and open-loop bandwidth is 2 MHz.

The NE5517 is available in an N-type or D-type 16-pin SO-16 package.

* *Dolby HX is a registered trademark of Dolby Laboratories.*

CIRCLE 54 ON READER SERVICE CARD

LCD DUPLEX DRIVERS

Up to 64 LCD segments may be driven by a new range of three single chip duplex drivers. The PCE2100/2110/2111 range of CMOS drivers interfaces the LCDs with a microcomputer, and is aimed at low-voltage applications. The drivers accept a voltage supply of 2,25 to 6,5 V with a current consumption of only 10 μ A.

The 28-pin PCE2100, the 40-pin PCE2110, and the 40-pin PCE2111 can drive up to 40 segments, 60 segments plus 2 LEDs, and 64 segments respectively. Each driver works in duplex mode, has bus control, a single-pin built-in oscillator, and serial data input. The drivers can be easily cascaded to drive more than 64 LCD segments.

A choice of DIL or flat pack packages is available, while the PCE2110 and 2111 can also be supplied in our unique VSO-40 (SOT-158) Very Small Outline package. The VSO-40 has the same body dimensions as the 24-pin SO package (SOT-137A), but with leads on a 0,762 mm (30 mil) pitch. This package is suitable for all soldering methods, including wave soldering. The DIL arrangement of the leads means that it is, for example, possible to cascade several PCE2110 or PCE2111 drivers on a single-sided printed circuit board only 20 mm wide.

The VSO-40 package can also be delivered in rails, and is therefore very suitable for automatic assembly.

CIRCLE 55 ON READER SERVICE CARD

**Philips Industries
Electronic Components and
Materials Division
Eindhoven - The Netherlands**

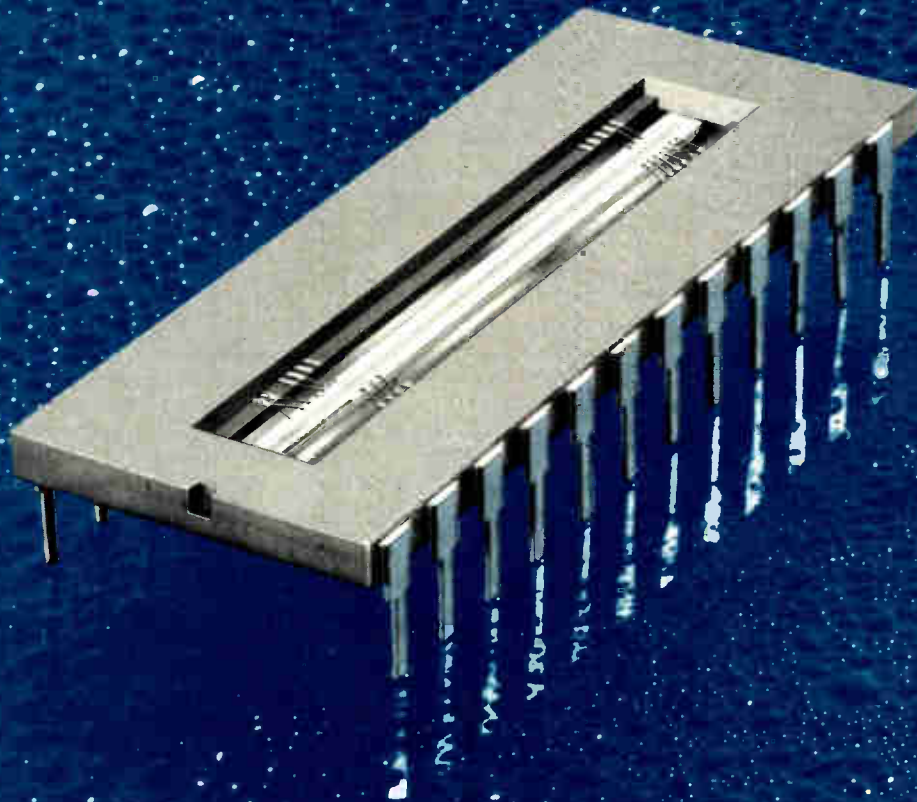


components which includes deflection yokes, line output transformers (fly-back), linearity controls and line driver transformers. Philips also offers full application support.

CIRCLE 53 ON READER SERVICE CARD

PHILIPS

LINE UP YOUR VIEWS WITH OUR CCD



Now from THOMSON-CSF a linear charge-coupled device incorporating the latest advances in n-channel MOS technology. This solid-state image pickup device for line-by-line viewing, is designed to meet your image scanning requirements.

APPLICATIONS • Facsimile • Flaw detection • Character recognition
• Surveillance • Dimensional checking • Identification • Positioning • etc.

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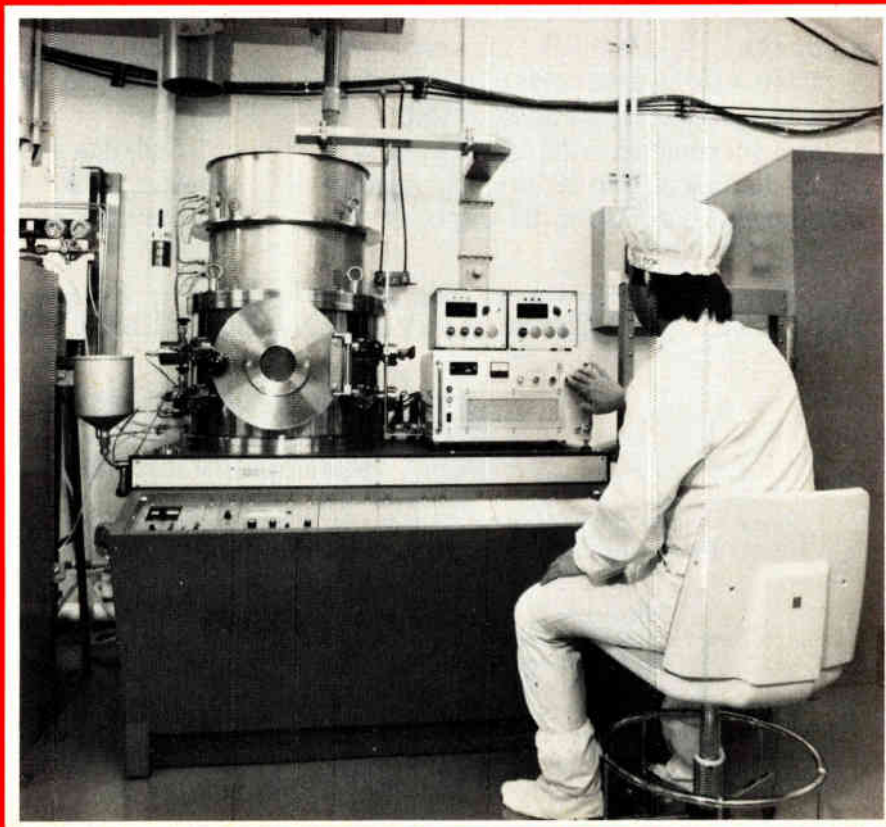
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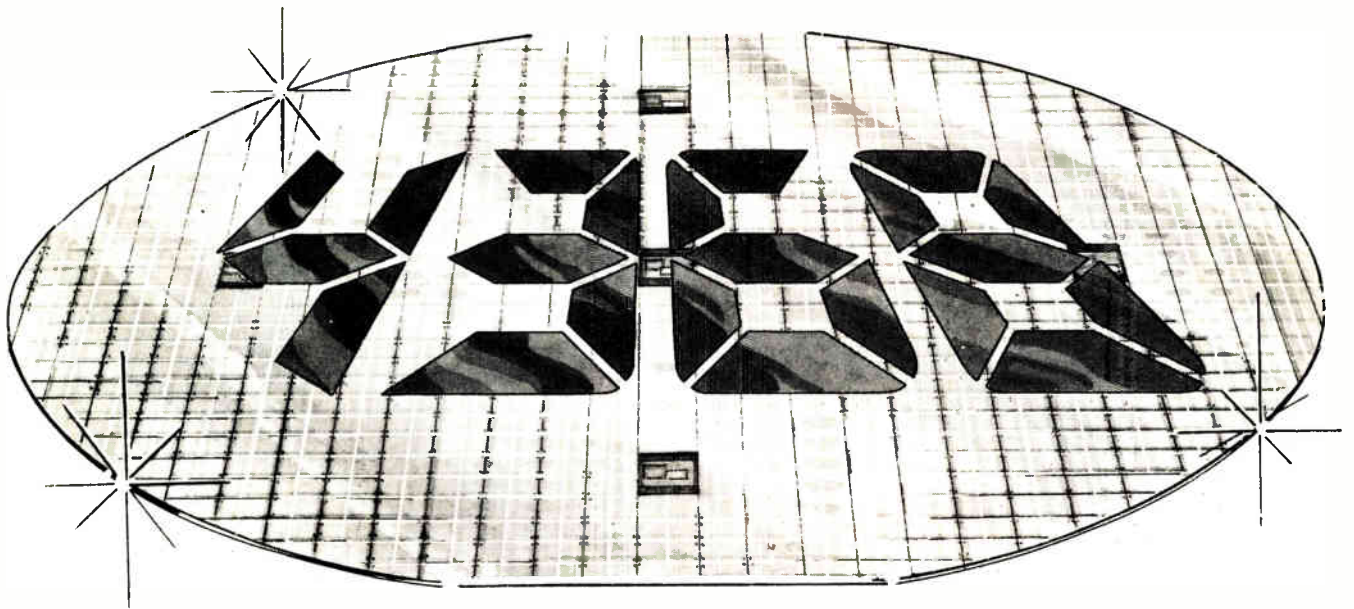
Electronics

International®

X-ray stepper sets record for alignment accuracy: page 81

Japanese researcher monitors new apparatus capable of depositing thin silicon dioxide films on wafers at room temperature: page 82





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No less than twenty-one new Plessey CMOS MSI devices for buffering, decoding, interfacing and selection in high speed/low power microprocessor and memory subsystems. And fast. Like 25ns typical tpd.

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Inductive machines planned in Japan

Last month Japan told the world of its plans for doing research on fifth-generation computers during the decade starting early 1982. Discussed at a four-day conference in Tokyo held Oct. 19 through 21, the project envisions not an extension of the mathematical power of present-day computers, but rather "knowledge information-processing systems" (KIPS) that will be available to untrained persons and meet the social needs of the 1990s and beyond. **Large knowledge bases will be contained in memory, with the central processing unit providing problem-solving and inference engines.** The three-phase project is devoted primarily to the advancement of software technology including innovative (other than von Neumann) architectures, but an integrated-circuit target of 10 million transistors on a high-throughput chip is also called for. The Ministry of International Trade and Industry will attempt to obtain a budget of \$43 million from the Ministry of Finance for the three-year first phase.

VCRs boom in West Germany

Thriving sales of video cassette recorders in West Germany have marketing people revising their figures drastically upward. Forecasts early this year had 1981 sales pegged at around half a million units, but they are now up to 700,000 and higher. Some market observers are even predicting that **demand will temporarily fall short of supply during the pre-Christmas buying spree.** European VCR producers—Philips Gloeilampenfabrieken NV in the Netherlands and Grundig AG of West Germany with their jointly developed Video 2000 system—are said to have the advantage of proximity to the market. But Japanese producers with their VHS and Betamax systems (plus European firms selling these under their own labels) still corner about three quarters of West Germany's VCR market.

UK to start electronic mail

As a first step toward electronic mail service, British Telecom is to establish a store-and-forward electronic letterbox service early next year in collaboration with the U. S. company Dialcom Inc. **Users of the service, primarily medium-sized to large businesses,** will be able to dial up the central computer facility, based on Prime 750 computers, log on, and type in addressed messages that will be forwarded automatically to other users. The service, whose facilities include user text processing and automatic spelling correction, will interface automatically with a viewdata or computer terminal or a packet-switched interface.

Hitachi finishes upgrading line of large computers

Hitachi Ltd. has filled in the hole between its large M-280H and M-240H mainframes announced in February with the M-260H, which has 3.5 to 4 times the performance of the earlier M-170. This addition completes the task of providing a step-up replacement for all of the firm's large computers announced earlier than 1977. The new mainframe uses the same advanced semiconductors as the M-240H and M-280H. Architectural features that enhance speed include a 64-K-byte buffer memory using 4-K bipolar random-access memories with an access time of 13 ns, advanced pipeline control, and distributed microprogram control. The computer is available with 8 to 24 megabytes of main memory and 8 to 24 channels, each with a throughput of 56 megabytes. The system rents for \$78,000 and up per month, with first deliveries scheduled for the first quarter of 1982. **Hitachi expects to export aggressively** through National Semiconductor in the U. S. and Olivetti in Italy.

Nixdorf adds third plug-compatible model

Nixdorf Computer AG, one of Europe's most successful data-processing equipment makers, will add a third model to its 8890 plug-compatible computer family, which is aimed primarily at users of the IBM 360 and 4300 systems. Designated 8890/70, the new model boasts three times the performance of the 8890/30, the smallest in the family. Its main memory, based on 64-K chips, is expandable to 8 megabytes. In addition, the new model has a buffer memory with a 16-K-byte capacity. The access time for 4 bytes is 500 ns, the same as for the 8890/30 and 8890/50. **Intended for use at medium-sized firms and for integration into data-processing networks at large organizations**, the 8890/70 will rent for about \$6,000 a month in its basic configuration. Deliveries should start during the second half of next year, the Paderborn, West Germany, company says.

Unit recognizes words spoken in any language

Speech recognition should start to become a fixture in Japanese offices and plants and laboratories when Nippon Electric Co. starts shipping its \$2,140 SR-100 voice-input terminal in March. The speaker-dependent unit can **recognize up to 120 unconnected words with an accuracy of better than 99%**. Response in both the recognition and the registration mode, in which the speaker trains the unit to recognize each word he will use, takes about 300 ms from the completion of the word. A single utterance of each word is sufficient for registration, enabling the process to be completed in about 2 minutes or less. Applications range from office or personal computer input and through computer-aided design input. NEC says it will export the SR-100. Language is not a problem because the terminal will recognize whatever words the speaker registers.

Cobalt raises disk density

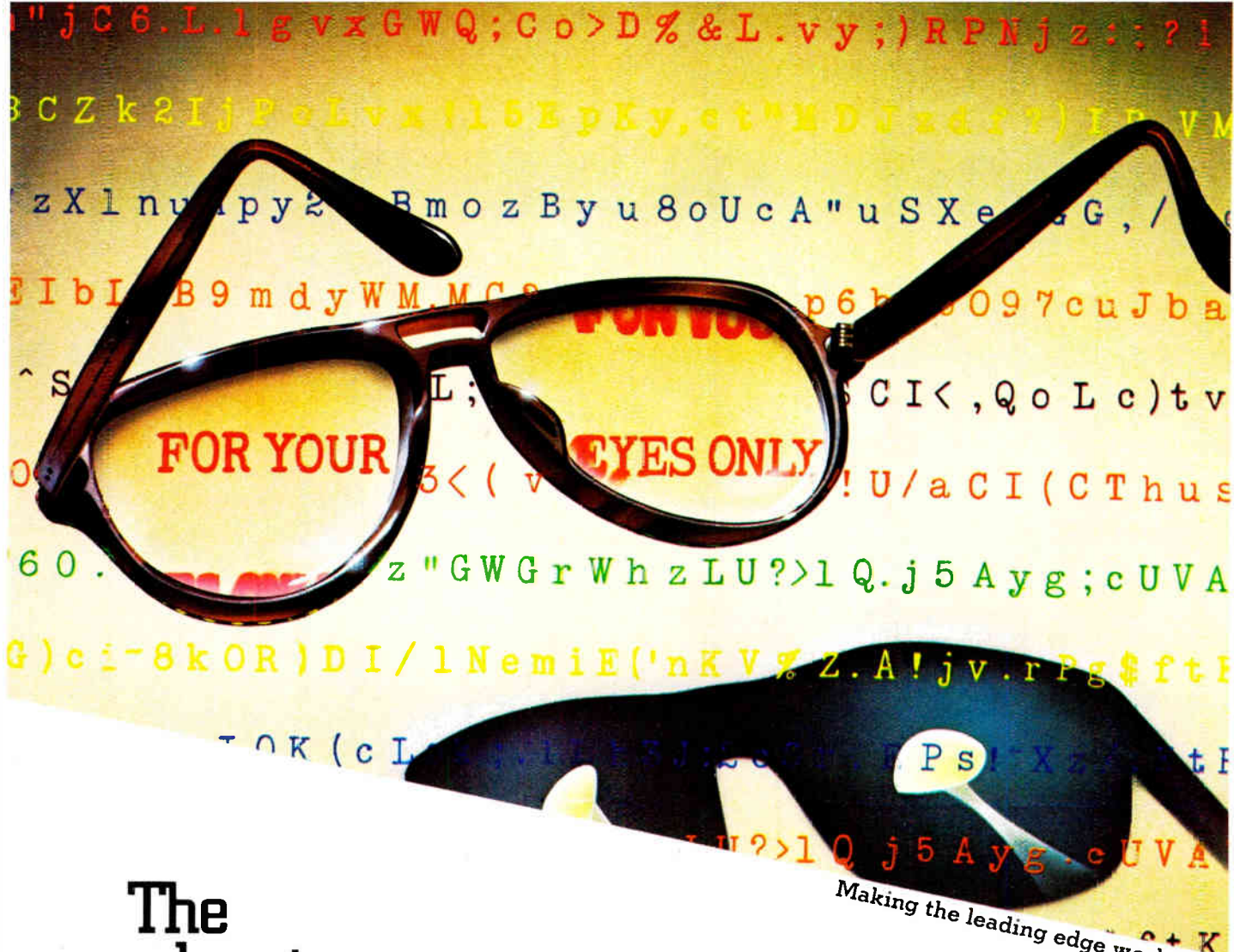
Research into hard disks with a cobalt-on-chrome magnetic layer on glass has reached the stage where they will now be developed as a product by CII-Honeywell Bull of Paris. When deposited on chrome, cobalt crystallizes and its coercivity rises significantly. This increases its potential recording density, already high because of its very high magnetization. The company expects that, for example, 12-cm (4.7-in.) disks produced in this way will have a **capacity of 25 to 30 megabytes per face** and that even that could be doubled by improving the electronics of disk reading.

Electronics solos as fly-by-wire system

When a British Aerospace Corp. Jaguar aircraft flew from the company's Warton, Lancs., airport on Oct. 20, it had no mechanical actuators to fall back on should its electronic fly-by-wire system—which controls the flight surfaces—have failed. Instead, four channels relayed digital commands to servo actuators from four high-speed self-monitoring computers, supplied by Marconi Avionics Ltd. Fly-by-wire systems make it possible to fly aerodynamically unstable (and hence highly maneuverable) fighter aircraft **by applying flight corrections many times a second**.

Videotex sent to Siberia

Videotex will be used by the USSR **to control the maintenance and supervision of its new Siberian gas pipeline**. The \$14 million contract, won by Britain's Rediffusion Computers Ltd. in Crawley, Sussex, calls for 46 of the company's R1800 data-base computers and 200 of its new "teleputer" terminals, a portable Z80-based personal computer with a color display and videotex and floppy-disk interfaces.



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Making the leading edge work for you.

The writing's on the wall.

File security is the feature more and more end-users are demanding. Especially in word processing and small business systems.

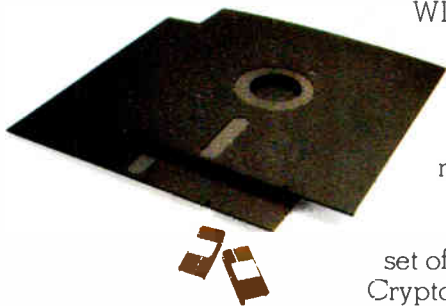
And that can translate into a significant product advantage. If you make the effort to include data encryption in your next design.

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Based on the NBS Data Encryption Algorithm, our compact WD 2001 is a single-chip solution that delivers full NBS certification, a 1.3 Mb/s throughput rate and can be bus or hardware controlled.

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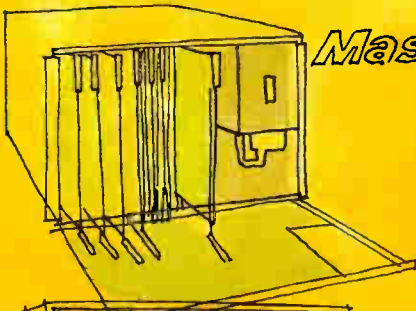


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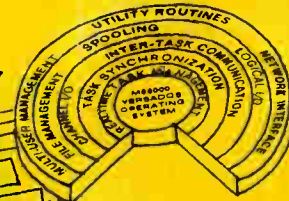
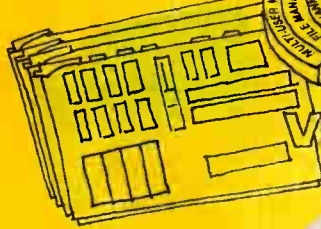
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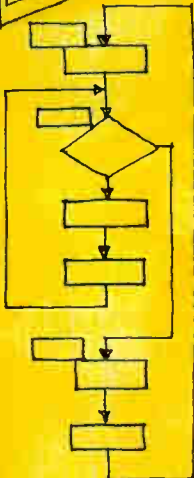


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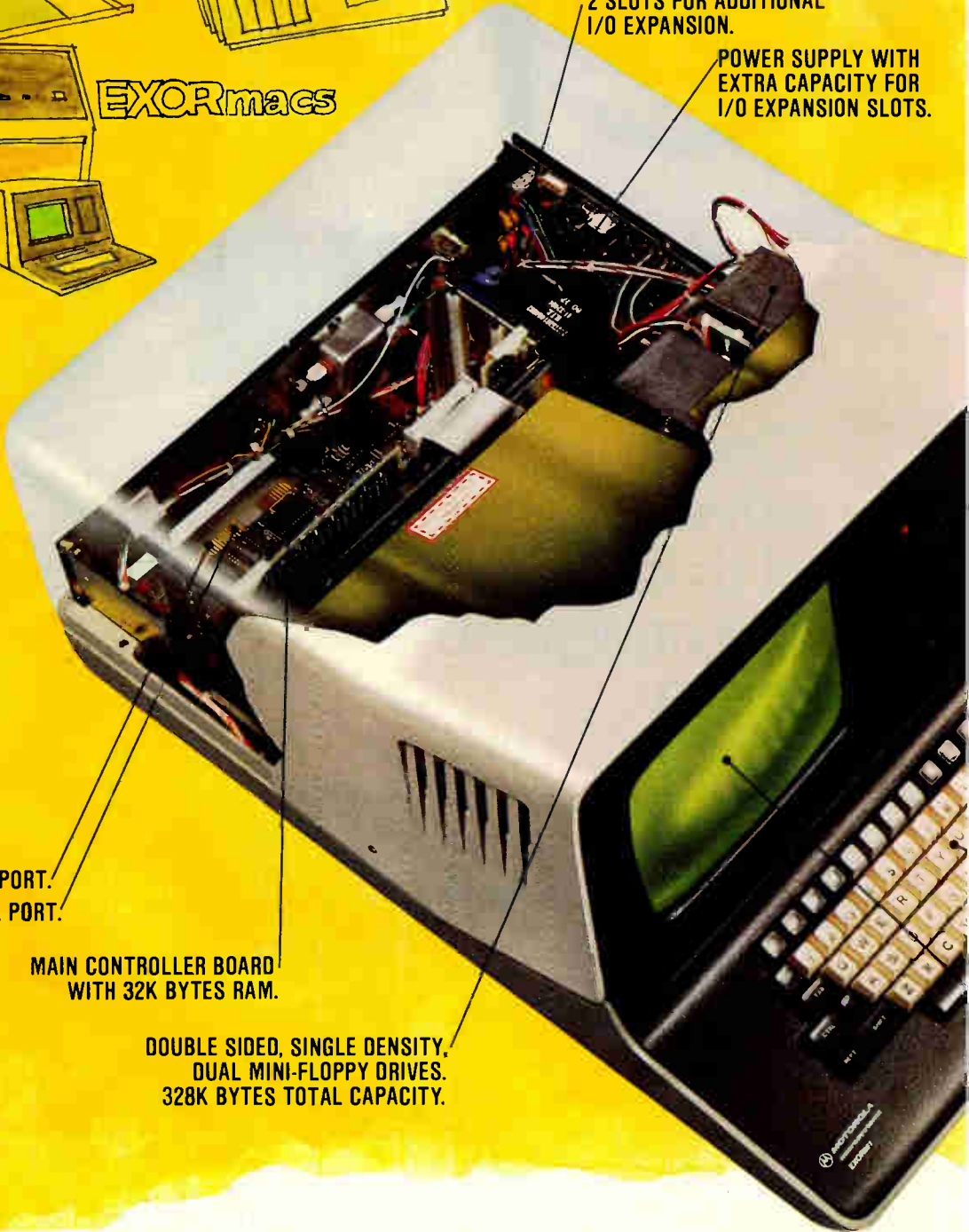


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SERIAL PORT.

MAIN CONTROLLER BOARD WITH 32K BYTES RAM.

DOUBLE SIDED, SINGLE DENSITY, DUAL MINI-FLOPPY DRIVES. 328K BYTES TOTAL CAPACITY.



for the 80s.

1

**Low-Cost
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Systems**

Powerful, economical EXORset.™ The desk-top development system for demanding 8-bit designs.

Increasing power and pervasiveness of 8-bit microcomputers today create a growing demand for practical, high-capability system development support.

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EXORset is an ideal development system for the entire range of M6800/6801, M6805/146805 and M6809 families of 8-bit MPUs, MCUs and peripherals.

Its speed and processing power, rivaling many low-end minicomputers, are derived from the MC6809 MPU.

EXORset also boasts integral parallel interface, programmable timer, serial RS-232C interface, 48K bytes of RAM with expansion capability to 56K bytes, and additional sockets for your own firmware.

Mass storage for the desk-top EXORset includes a total of 328K bytes of program or data storage in high-quality dual, double-sided, single-density 5-1/4-inch

diskette drives, plus expansion capability for two or four additional 8-inch diskette drives.

The high-resolution 9-inch display has both 80-character by 22-line and 40-character by 16-line formats, plus a graphic display. The keyboard contains the full ASCII character set, plus 16 user-programmable function keys that enhance EXORset versatility.

Powerful, versatile, easy-to-use software complements EXORset hardware. The EXORbug™ firmware monitor provides program debug and control facilities. The XDOS Operating System controls all disk operations and file directory management, and imposes minimal overhead.

Macro assemblers are offered for each of Motorola's 8-bit MPU families, giving EXORset full range as a software development station.

A disk-interactive, CRT-oriented text editor allows simple creation of new files, fast update of old files and a variety of powerful editing functions. The standard EXORset high-level language is Motorola's interactive compiler/interpreter, BASIC-M. A Pascal compiler is optional.

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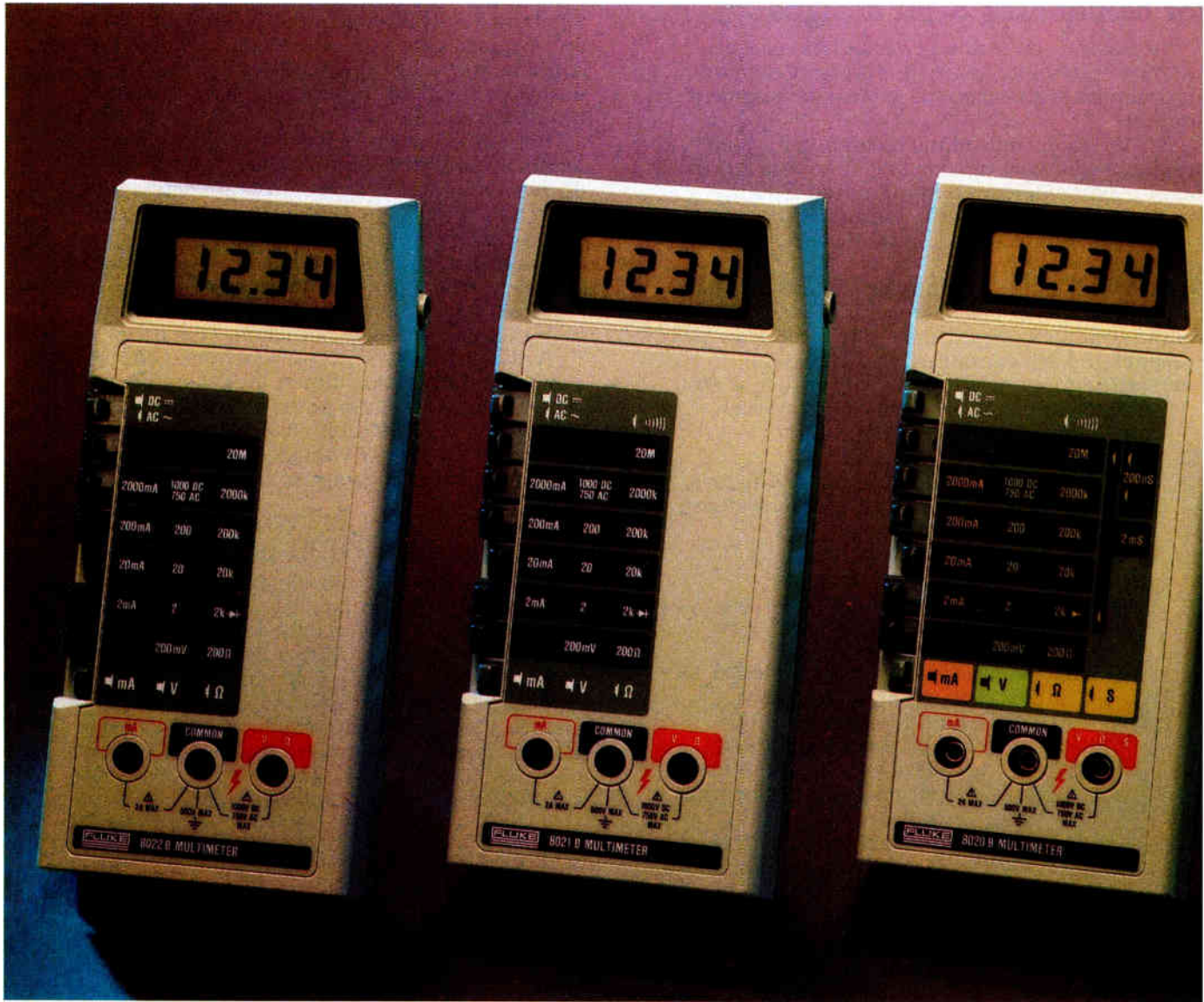
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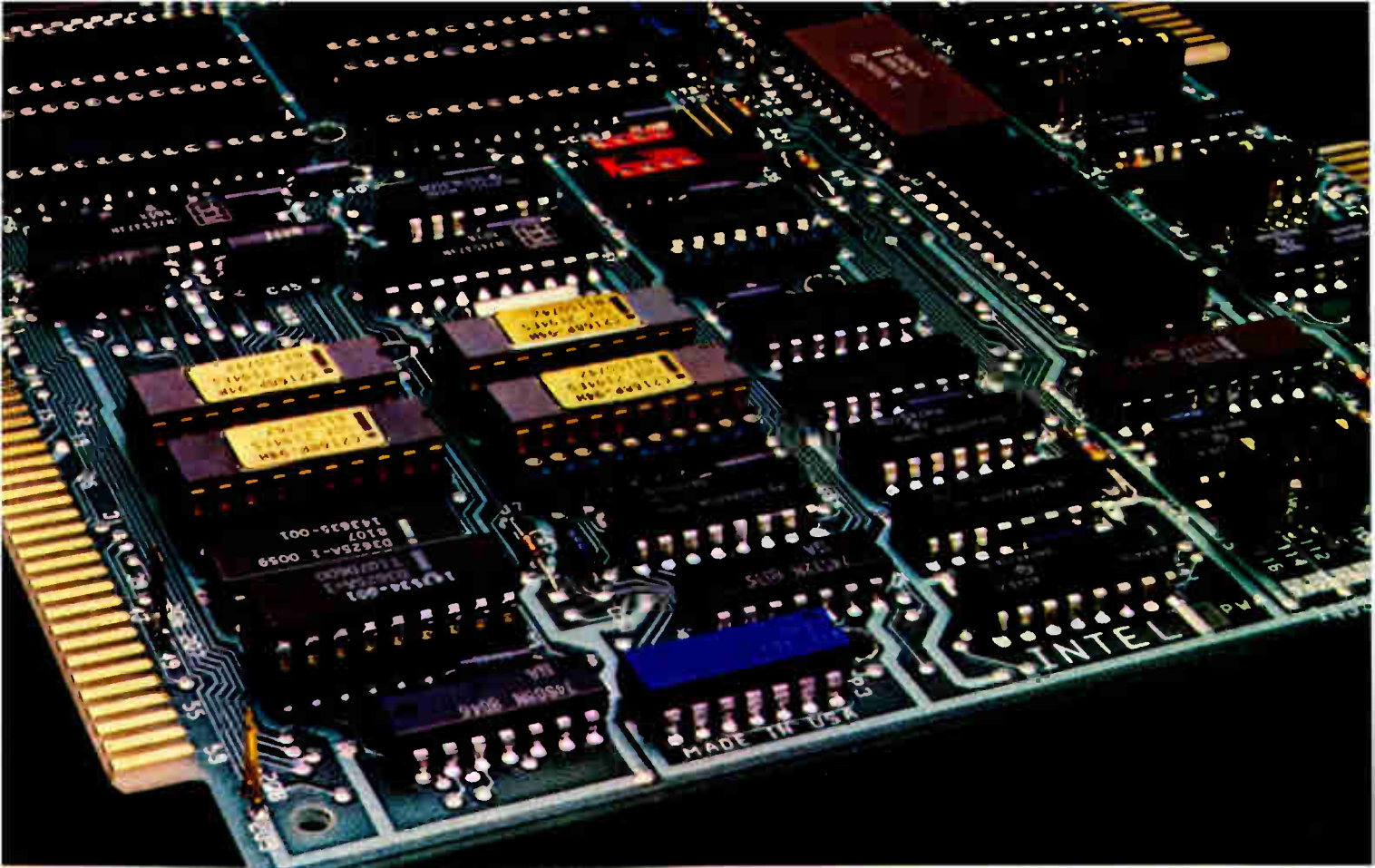
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X rays can align chip masks with 0.02- μm accuracy

by Robert T. Gallagher, Paris bureau manager

Step-and-repeat system uses copper X-ray source, aligns wafer continuously throughout its exposure

Most X-ray lithography systems expose wafers to a flood of X radiation. Now one of the first step-and-repeat X-ray machines has just become available and comfortably achieves the far greater resolution and alignment accuracy predicted for the approach.

Under ideal laboratory conditions, the new machine, built by Cameca, a Thomson-CSF subsidiary located in the Paris suburb of Courbevoie, can achieve a resolution of 0.1 micrometer and an alignment accuracy of 0.02 μm . Under normal laboratory conditions, 0.2 and 0.05 μm are typical. Designed for use in laboratory production of integrated circuits, the system can take up to a 3-inch wafer and has an exposure field of up to 100 square millimeters.

The two features that distinguish Cameca's system are its laser-optical alignment technique using Fresnel zone plates and diffraction grating and its high-power copper source of X rays with a long wavelength of 13.3 angstroms.

The alignment of wafer and mask is a completely automatic process that begins with etching the wafer with three arrays of diffraction gratings each 0.5 mm square. On each mask are three corresponding arrays of Fresnel zones. A parallel monochromatic light beam from a helium-neon laser is focused into the diffraction grating by way of a scanning

mirror. The light diffracted by the grating is refocused by the Fresnel zone plate and sent back toward its source as a parallel light beam where it is detected by a photodiode.

Nonstop. The photodiode analyzes the reflection, and the signal is amplified by a locking amplifier whose reference is the scanning mirror's driver. Any movement of the wafer and the mask relative to each other thus creates an error signal that is acted upon by the system's piezoelectrically controlled mask drive stage. In this way, alignment is a continuous process carried on even during the exposure of the wafer.

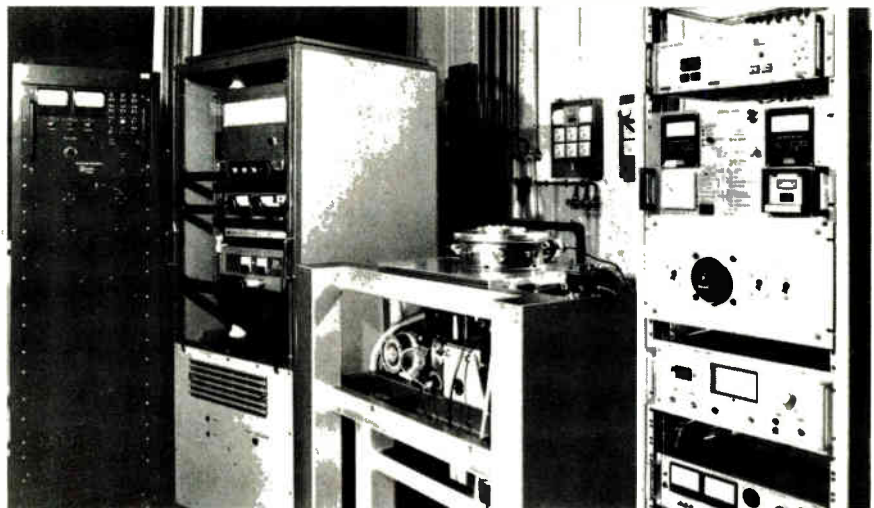
Most technical decisions imply advantages and disadvantages, and Cameca's to design its system with an X-ray wavelength of 13.3 \AA and, thus, a copper-line source is no exception.

"Our preoccupation was to achieve the best resolution possible, so we decided it was worth having to

expose in a vacuum," says Bernard Fay, the engineer at Thomson-CSF's central research laboratory who coordinated the development of the system. Other drawbacks were the fairly high continuous spectrum and the possible K-line excitation when the voltage exceeded a 9-kilovolt threshold.

But on the plus side, the wavelength makes it possible to work at the 10- μm wafer-mask gap that the company considers optimum. Resolution is also optimized because the degrading effects of photoelectron scattering and diffraction are of similar magnitude. In addition, copper is an ideal anode material because of its high thermal conductivity, and the X-ray absorption and hence sensitivity of organic resists is quite high at this wavelength. Polymethylmethacrylate resists need an exposure of 15 minutes, and FBM resists an exposure of 1 min.

Finally, because gold's X-ray ab-



The hardware. The long wavelength of its high-power copper X-ray source and its continual laser optical alignment help this lithography system to attain a 0.1- μm resolution.

sorption is also high at this wavelength (50 decibels/ μm), adequate contrast can be achieved with a thickness of 0.1 μm on the mask. At a wavelength of 4.4 \AA (a common choice of wavelength for X-ray lithography), 0.6 μm is necessary, thereby increasing shadow and concurrently decreasing resolution.

The 0.1- μm gold layer overlies a 0.5- μm layer of silicium nitride on a substrate of pure silicium containing several 2-by-2- up to one 10-by-10-mm hole. The entire mask is 30 mm square.

At the moment, Cameca has a working prototype of its system and is ready to begin taking orders. The expected delivery delay is 10 months, and the price about \$1.3 million.

Japan

Thin Si films can form at room temperature

The micrometer-sized features of very large-scale integrated circuits are especially prone to damage by the high temperatures typical of some of the later stages of wafer processing. So a new process that deposits thin films of silicon nitride and silicon dioxide at room temperature is expected to open new horizons in the fabrication of not only of silicon VLSI but also Josephson devices and compound semiconductor devices such as gallium arsenide and indium phosphide.

In the microwave electron-cyclotron-discharge apparatus developed at the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp., a highly activated plasma decomposes the gases carrying the materials to be deposited. This makes it possible to deposit pure silicon nitride, for example, free of the hydrogen in the silane that carries the silicon. Furthermore, ions and electrons from the plasma bombard the surface of the wafer, enhancing the deposition reaction. No thermal reaction is involved.

The conventional method of de-

positing thin films of compounds of silicon during semiconductor fabrication is the chemical vapor-deposition process. To deposit nitride, for example, silane and ammonia, NH_3 , are made to react thermally in a furnace on the surface of a wafer heated to between 500° and 1,000° C. Film quality is excellent but the substrate must be capable of withstanding the high temperature.

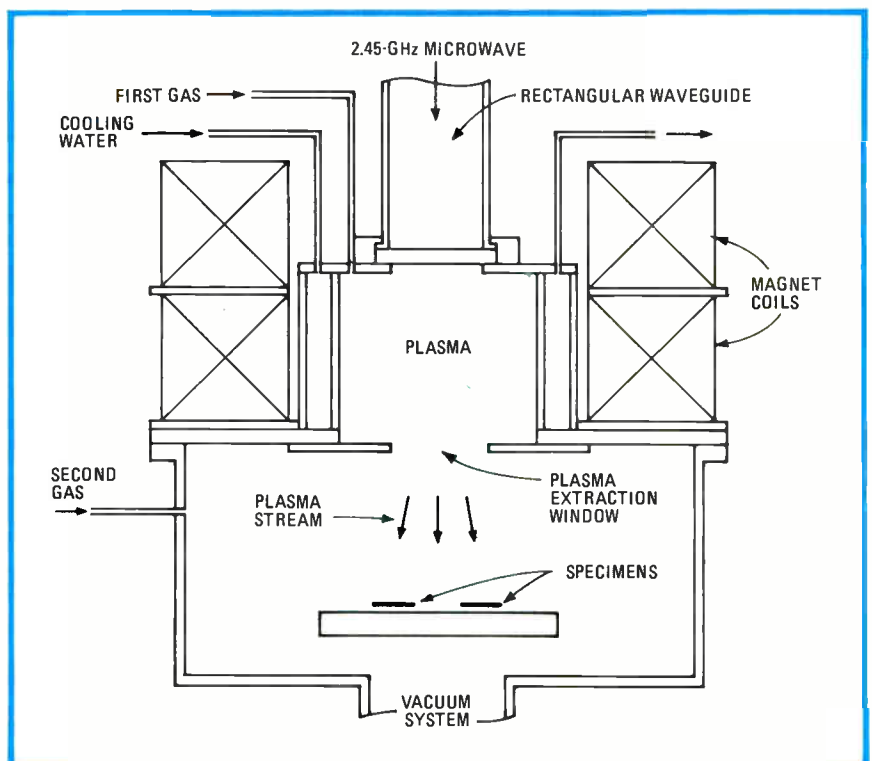
More recently, use has been made of the plasma CVD technique, which combines a radio-frequency plasma discharge with a thermal reaction at 250° to 350° C. This temperature is still too high for many substrates. Furthermore, the carrier gases do not completely decompose and the deposition reaction at the substrate surface is incomplete. Hydrogen remains in the film and the molecular bond is poor.

Hyperactivity. The Musashino apparatus generates plasma in a chamber by microwave energy at 2.45 gigahertz. Magnet coils control the circular motion of the electrons so that it resonates with the microwave frequency to produce an electron

cyclotron resonance plasma. This condition enables the plasma to effectively absorb the microwave and become highly activated. Interaction between the high-energy electrons in the plasma and the magnetic field accelerates the plasma through the plasma extraction window, causing electron and ion bombardment of the wafer surface.

Silicon nitride is deposited by introducing nitrogen into the plasma chamber and silane into the wafer chamber (see diagram). The deposition rate is about 300 angstroms per minute, which is comparable with or better than conventional methods. Silicon dioxide is deposited by substituting oxygen for nitrogen. The nitride and oxide films have high molecular density, and the oxide film is as good as one prepared by thermal oxidation. Both types of film can be deposited on substrates with patterns of photoresist, which need not be the heat-resisting variety, and patterned by the lift-off method.

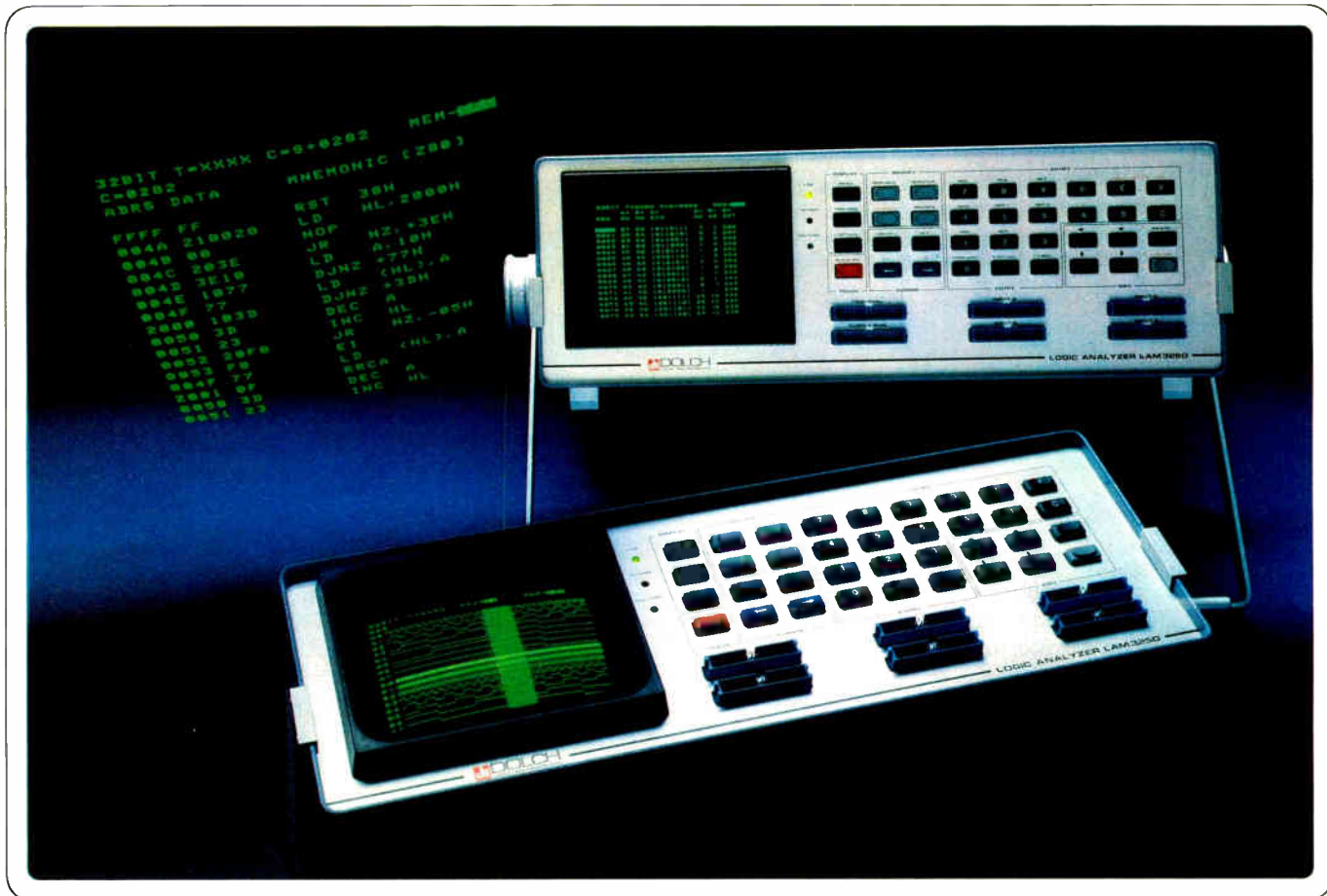
Silicon films can be deposited by using an inert gas such as argon as the activated gas. Silicon film depo-



Cool approach. When oxygen serves as the first gas and silane as the second, the highly active plasma causes a layer of silicon dioxide to form on a wafer without heating.

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LOGIC INSTRUMENTS

sition can be used for the fabrication of silicon solar cells and amorphous semiconductor devices as well as gates and interconnections in MOS field-effect transistors.

The experimental Musashino equipment uses slightly more than 3 kilowatts. The lab is conducting talks with a firm that is expected to announce a commercial unit before the end of the year. **-Charles Cohen**

Great Britain

SAW devices benefit defense measures

It's still an analog world when it comes to superfast signal processing, and nowhere is the requirement for speed more pressing than in modern electronic warfare. Newly available surface-acoustic-wave modules from one small British company, Signal Technology Ltd., for example, are carrying out the fast front-end signal processing in the following projected or potential applications:

- Discerning radar jamming and other electromagnetic signals by scanning the electromagnetic spectrum in 1-gigahertz gulps every half microsecond. Such spectrum analyzers can be used either in electronic intelligence, tracking enemy movements, or in electronic counter-measure systems by ducking radar jamming. The company is supplying against a firm contract.
- Decoding high-speed data streams that distinguish friend from foe. Signal Technology is producing a convolver to meet the new North Atlantic Treaty Organization Identification System (NIS) to be fitted to allied aircraft.
- Serving frequency-agile radar systems that can hop over gigahertz bandwidths at megahertz rates, faster than the following deception jammers, which track the illuminating radar and respond by retransmitting delayed echoes. As yet only a proposal exists for an agile radar system that would be used in possible beam-riding missiles and would be unfazed by such jammers.

The company is just one of several developing SAW technology, as most European countries want their own capability. Located in Swindon, it was spun off from the Plessey Co. to commercialize the parent's signal expertise. Plessey shares ownership of it with Anderson Laboratories Inc. of Bloomfield, Conn.

More than service. The original idea was to offer a design and manufacturing service for SAW devices, but the company has found itself developing complete subsystems. Its

latest compressive receiver module is a case in point. With a bandwidth of 250 megahertz, just four of these compact subsystems (each measuring approximately 1 by 3 by 4 inches) are all that's needed in order to analyze a gigahertz slice of the EM spectrum.

This compressive receiver approach, claims marketing manager Ron Towns, cuts by almost an order of magnitude the number of components needed in channelized receiver designs. The dispersive delay is 500

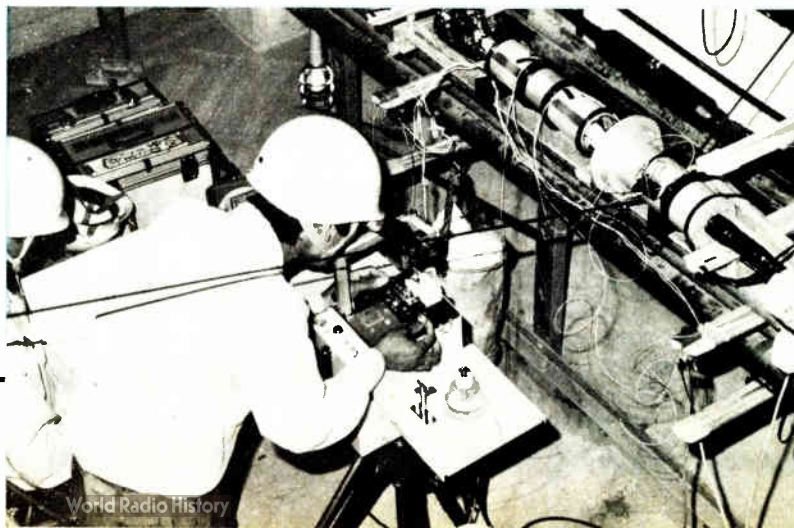
Tokyo testing 400-Mb/s fiber-optic system

Success has smiled on the first phase of Japan's first field trial of a high-capacity long-haul optical-fiber transmission system being installed on the outskirts of Tokyo. One 18-kilometer span with six single-mode fibers has been completed and tested on the 400-megabit-per-second 80-km route that will link the Musashino and Atsugi Electrical Communication Laboratories of the Nippon Telegraph & Telephone Public Corp. Data indicates that the system will perform according to plan when the field test of the entire test starts next March.

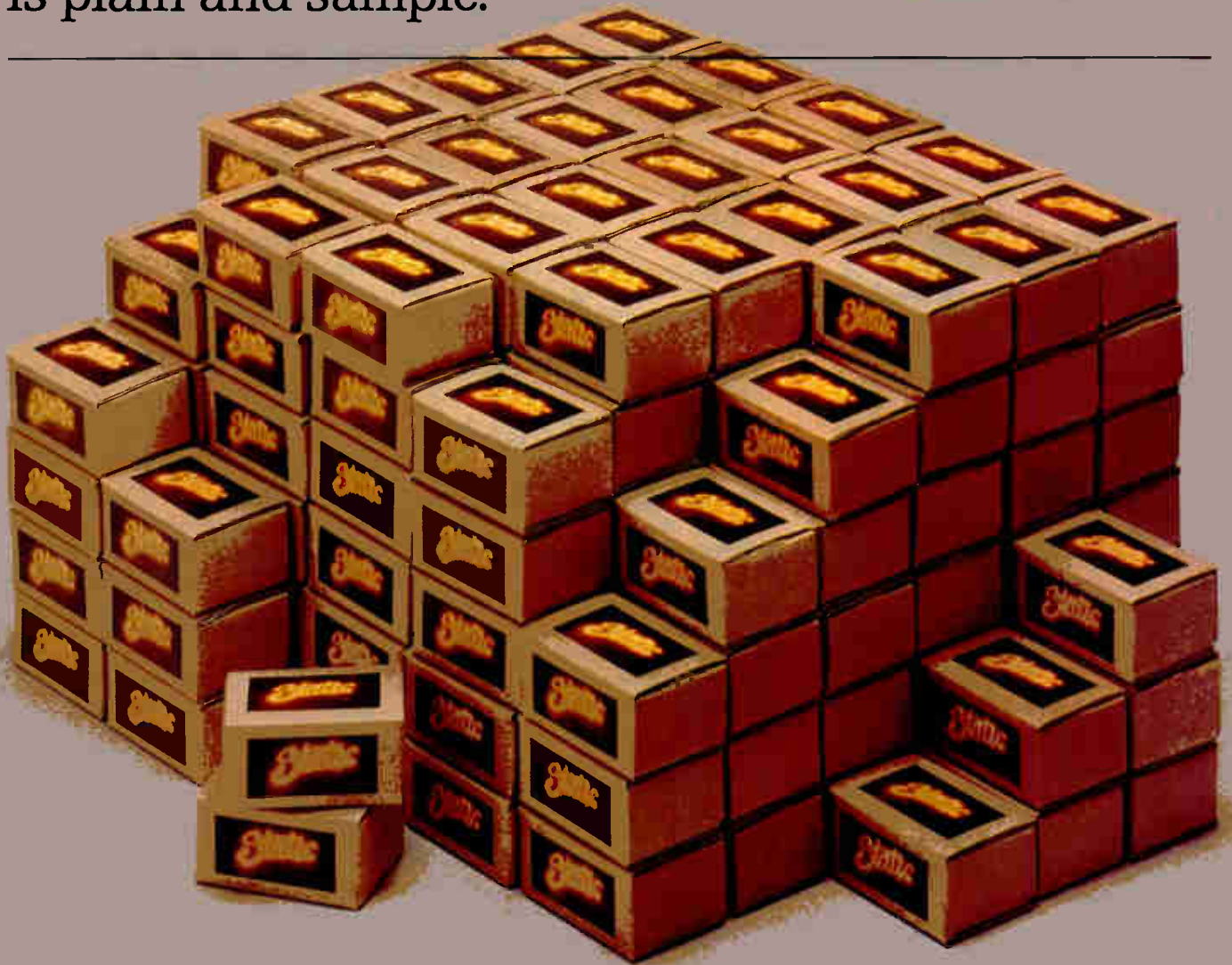
This spring installation of shorter commercial systems operating at 32 and 100 Mb/s was started [*Electronics*, March 10, 1981, p. 67]. NTT claims that its tests of the span are the first successful field tests of a 400-Mb/s optical-fiber system in the world. Tests have included the transmission of coded voice, television, and data. The cost of a commercial system will probably be only about 60% that of a coaxial cable system, a clear economic advantage for the new transmission method.

The F-400M long-haul system is designed for a maximum transmission distance of 2,500 km, with repeaters spaced 20 km apart. This is about 13 times the 1.5-km repeater spacing of the DC-400M 400-Mb/s coaxial cable system designed for the same purpose. The capacity of the fiber system is equivalent to 5,760 two-way telephone circuits per pair of fibers for voice transmission but many times that number of analog telephone circuits for data transmission, as is evident from the 400-Mb/s bit rate.

In these initial field tests, the six single-mode fibers in the cable are connected end to end through six repeaters for a total length of 110 km. The transmission source is an indium-gallium-arsenide-phosphide semiconductor laser with a 1.3-micrometer wavelength. Its estimated lifetime is 60,000 hours, and its coupling loss for launching its output into the single-mode fiber is less than 6 decibels. Furthermore, the average attenuation is 0.6 dB/km along the cable, a low 0.1 dB at the approximately 100 splices, and a low 0.6 dB at approximately 100 field-assembled connectors. **-Charles Cohen**



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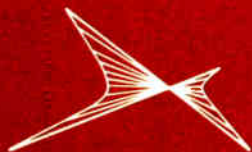
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picoseconds, within which time it has completed a Fourier separation of any EM signals present with a 4-MHz resolution.

The module consists essentially of a mixer, two nearly identical SAW convolvers, and an impulse generator. The receiver operates much like a scanning superheterodyne, using as its local oscillator a pulse generator and one of the two SAW chips. Every impulse applied to the SAW chip produces a chirped output—a low-to-high swept frequency that is mixed with the incoming rf signal and applied to a second convolver. This compresses the mixed output producing a $(\sin x)/x$ pulse whenever the local oscillator frequency coincides with the incoming one. A high-speed counter triggered by the pulse generator gives a direct measure of the frequency. Together, the compressive receiver's local oscillator and SAW convolver form a matched filter whose center frequency sweeps the spectrum searched.

Programmable. For NATO's NIS system, Signal Technology has developed a programmable convolver that can decode phase-coded identity calls consisting of 1,000 chirps—phase reversals that each represent 1 bit. Recognition is achieved by matching the incoming signal against a prestored signal that is simultaneously applied to the convolver. The two signals are simultaneously launched into the surface of the lithium niobate substrate and interact to produce a voltage proportional to their product. A parametric electrode integrates this distributed signal to provide an output when there is a match.

Yet another application of SAW technology, says Towns, would be for generating ultrafast hopping signals, with hop durations of between a few tens of nanoseconds and 100 microseconds and with bandwidths of 2 GHz. The concept could be realized within a volume of 6 cubic inches, excluding the digital word generator used to control it. Its applications would be in frequency-agile radars that could out-hop follower-jammers, but so far industry has not taken it up. —Kevin Smith

West Germany

Diesel engines to get electronic control

West Germany's Robert Bosch GmbH could well be the first company to go into production with microprocessor-based fuel-injection control systems for diesel engines. At present, such systems are going through their paces on a number of company-owned trucks and cars.

With electronic control, Bosch says, engine-related parameters can be selected to optimize engine operating conditions. For another, it becomes possible to compensate for deviations in an aging injection system's performance and to maintain close tolerances in allowable exhaust-gas emission values.

In the offing is yet another advantage—by simply exchanging chips and the associated program, an electronic control can be readily adapted to the different engine types. What's more, it should prove possible to integrate a diesel control with other systems like an electronically controlled automatic transmission. However, "electronic diesel control will not lead to any spectacular savings in fuel compared to mechanical control," a company official says.

Obstacles hurdled. Actually, Stuttgart-based Bosch, Europe's largest automotive accessories maker, started developing electronic diesel controls some 15 years ago. What kept the company from announcing a practical system sooner was the large number of components required, as well as insufficient reliability.

Now, though, advances in component design and particularly in microprocessor technology have eliminated those obstacles. However, Bosch is reluctant to say just when it will have a marketable system. "Volume production could come during the medium term," the official says, implying that systems for trucks may come by 1984 and for passenger cars somewhat later.

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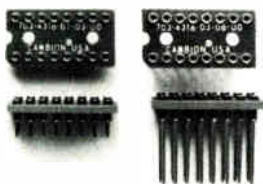
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the market potential for electronic diesel controls is likely to be substantial. "The '80s promise to be the decade of the diesel engine," says Klaus-Dieter Zimmermann, a member of the management team for Bosch's automotive equipment division. Between 1970 and 1980, he says, annual production of diesel engines in the Western world doubled to 8 million, including 5.9 million multicylinder types. According to Bosch, the number of multicylinder diesels produced annually in the Western hemisphere could go to 10.5 million in 1985.

The Bosch system consists essentially of the microprocessor-based electronic control unit, sensors, and actuators. Its most important input comes from an inductive pickup at the gas pedal. Other inputs include data on water, fuel, and intake air temperature, intake pressure, and engine speed. The data is stored as characteristic curves or performance graphs that may be one- or multi-dimensional.

The system reads out the data characteristic for specific engine operating condition, calculates the optimum amount of fuel to be injected, and injects that amount at the right time, ensuring the least possible fuel consumption at the lowest possible emission value.

In step. A couple of examples point up what the system can do. When the engine is started, a more-than-normal amount of fuel, depending on engine temperature, is required. The amount gets smaller with warmer engines, so as to prevent black smoke from forming at the exhaust. Here, the system's temperature-control aspects come into play. Depending on the engine temperature during start-up, fuel injection is automatically adjusted to start early or late. Once the engine is running, the start of injection attains its normal value for a specific temperature and engine speed.

The system also makes driving more comfortable. A characteristic curve in the memory modifies the gas pedal's inductive pickup output for jerk-free acceleration and deceleration.

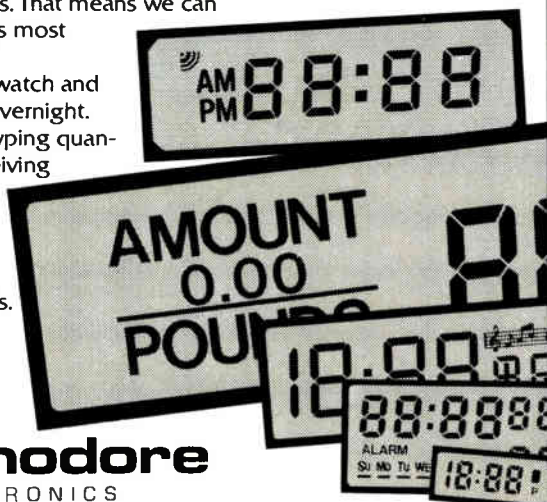
-John Gosch

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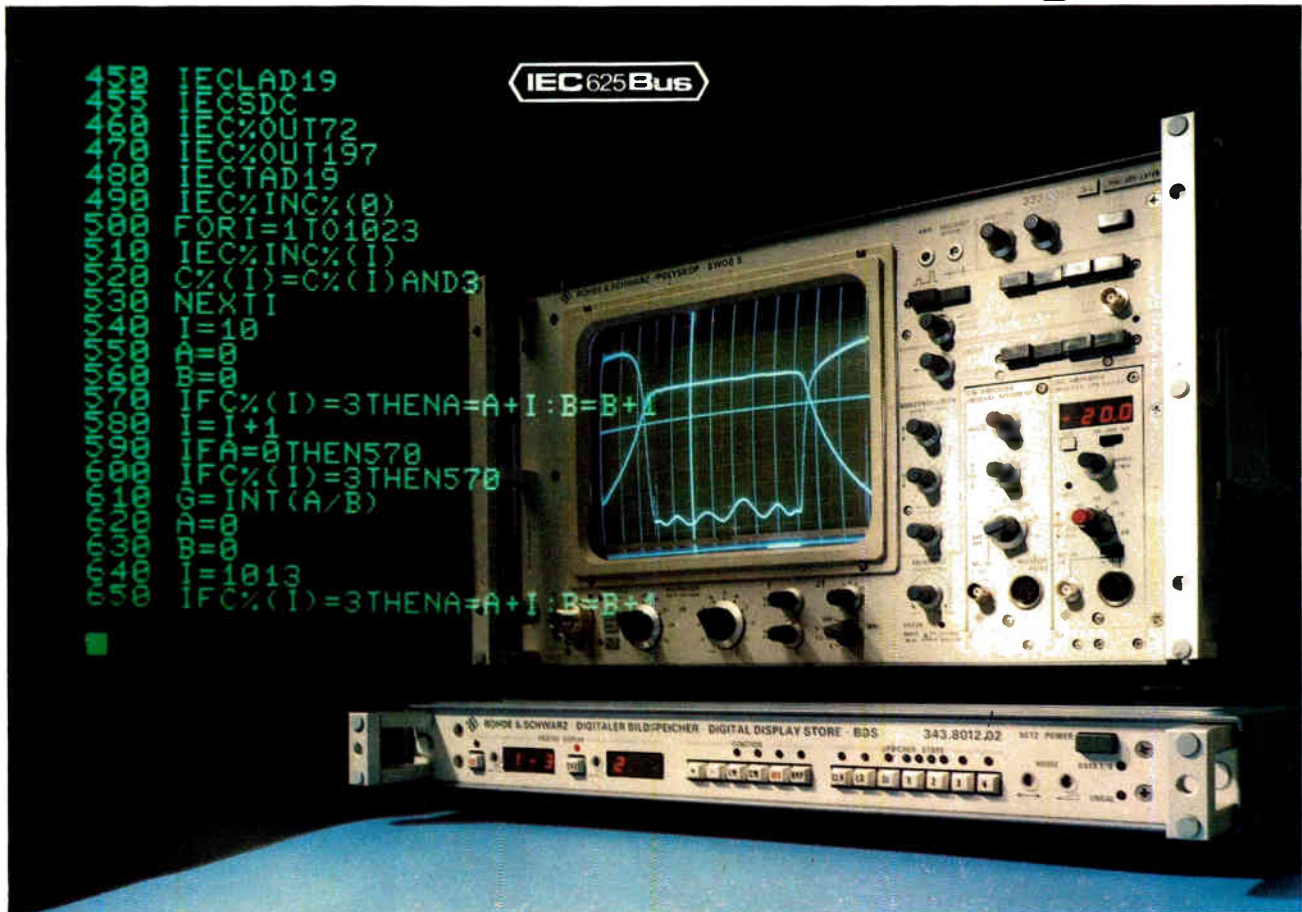
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Polyskop SWOB 5 with extra capability



The operating ease and performance of the compact sweep tester Polyskop SWOB 5 (now up to 1.3 GHz) have been enhanced even more through a new digital display store and a log-amplifier plug-in.

Digital display store BDS

Even at slow sweep rates the BDS permits simultaneous, flicker-free display of two test curves plus associated information like frequency markers and level lines. Storage of four sweep curves is possible, and the contents of any two memories can be added and subtracted, thus enabling compensation of frequency-response errors for instance. The optional **average-value memory** averages 4, 8 or 16 successive sweeps, making it possible to suppress random interference on the sweep curve (e. g. noise). If the BDS is used with its optional **IEC-bus interface**, the contents of all memories can be read out, converted and read in again by a desktop controller.

The log amplifier SWOB 5-E3 (right in the photo) has a digital level display and the following new features:

- AF input for test items with built-in rectifier
- automatic setting of reference levels
- signalling of excessive interfering-signal levels
- gain of active demodulator taken into account in level measurements

The measured value indicated can be absolute in dB (V) and mV (with auto-ranging) or relative in dB, and for relative measurements the reference level can be set anywhere between 0 and -100 dB (V).

**Ask for the new data sheets
SWOB 5 and BDS**

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Federal Republic of Germany

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Circle 42 on reader service card

How many amps? What voltage? ...



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How fast? No problem!

Switch on fast to a new world of power devices ... devices that are easy to drive from ICs and μ Ps ... devices like our unique GTO switches that turn off fast - in less than a microsecond ... devices that are ideal for this digital decade.

See Philips first, when you've got a power problem. We cover the technology and application spectrum with these and other exciting devices. Our advice is therefore objective and our concern is with making sure you get optimum design results.

Get your answer to the question of how many amps ... how fast ... and what voltage by sending today for our new brochure 'Power at your Command'. It gives full details of GTO and POWERMOS devices, plus the rest of our comprehensive range.

Philips Industries,
Electronic Components and Materials Division,
Eindhoven, The Netherlands

POWERMOS

POWERMOS is Philips' shorthand for Power MOS FETs. Features include:

Direct drive from TTL/LSI plus μ C output ports. Controls up to 30 A from a few volts and almost no drive power.

Fast switching. Several times faster than bipolar, even an order of magnitude for certain types.

Optimum reliability via outstanding SOAR characteristics.

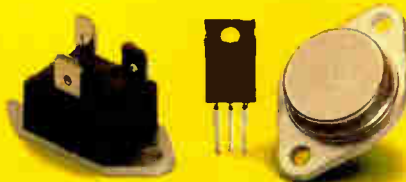
No secondary breakdown: as device heats up, resistance increases and current goes down. Therefore no hot spots or current hogging and automatic equalisation throughout chip.

Easy parallel operation. Devices share current evenly. Those that heat up will increase in on-resistance and shift current to another branch.

High power amplification. Typically, an order of magnitude higher than bipolar.

These features make POWERMOS ideal for inductive load switching, switched-mode power supplies (SMPS) and motor control. For SMPS they allow frequencies to be more than doubled, bringing further reductions in system size and weight.

POWER-MOS	Main Applications	GTO
●	Automotive	
	Light ballast (TL)	●
●	Telephony/EDP printers	
	Domestic appliances (washers; microwave ovens; cookers)	●
●	Low-power motor control (500 W typical)	
	Medium/high-power motor control	●
●	SMPS (switched-mode power supplies)	
	SRPS (series-resonance power supplies)	●
	CRT deflection	●



GTOs are available in isolated TO-238 and plastic TO-220 encapsulations. POWERMOS switches come in metal TO-3 and TO-220.

GTO

GTO ... standing for Gate Turn-Off ... is the nearest thing yet to the perfect semiconductor switch. Like the thyristor, it can be turned on by positive gate drive and like high-voltage transistors, it can be turned off by negative gate drive. The features of both devices combine to give the best of both worlds, for example:

High blocking voltage. Up to 1500 V.

Excellent overvoltage/current capability. Includes simple fuse protection.

No commutation problems. GTOs can handle dV/dt rates of up to $10\text{-kV}/\mu\text{s}$.

Controllable anode currents. Well in excess of average ratings.

Easy drive. Low gate trigger currents allow direct drive from ICs.

Fast turn-off. GTOs can be switched off in less than $1\mu\text{s}$. These last two features are typical for bipolar devices, but GTO figures are considerably superior. The overall combination of high current and voltage handling, easy gate drive, fast switching and rugged construction therefore make GTO devices ideal for a very wide range of applications.

We'll keep you well powered

PHILIPS

Circle 43 on reader service card

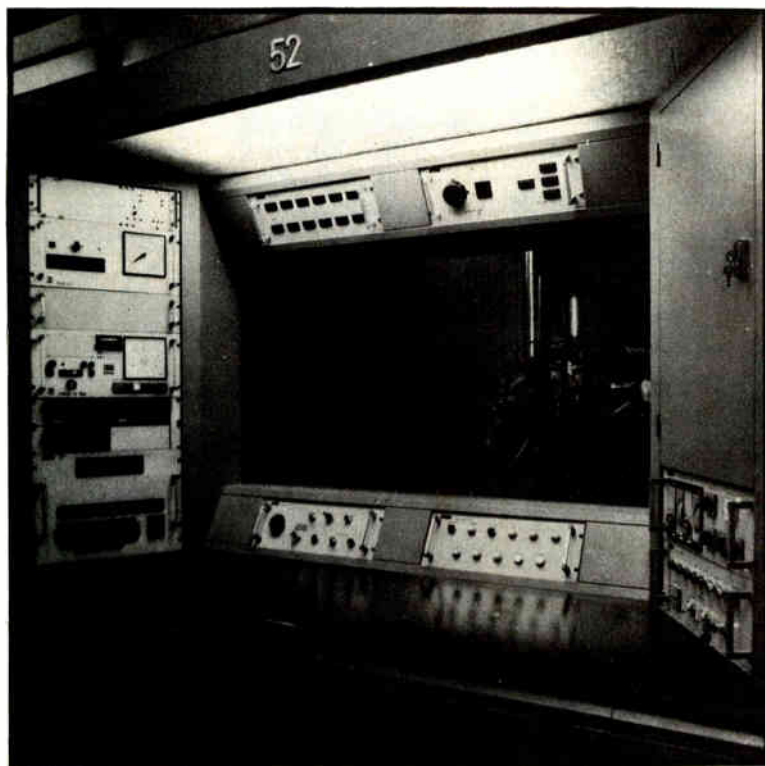
& SEPA AUTOMOBILES

SEPA has long been fully familiar with industrial instrumentation, especially that used in the automobile world. This fund of experience is freely available to customers to cater for their needs with regard to on-line or end-of-line inspection, tests and inspections in test rooms, and high-precision instruments.

Among the several systems SEPA offers, particular mention can be made of that devised for the automatic running of an engine test room.

This is a highly sophisticated system that permits the execution of test cycles programmed in computer language in either automatic or manual mode. The micros forming part of each local unit and the central unit gather, process or store data on the engine under test. These are then displayed locally (monitor, print-out, etc.) and centrally for graphic processing (plotter, discs, etc.).

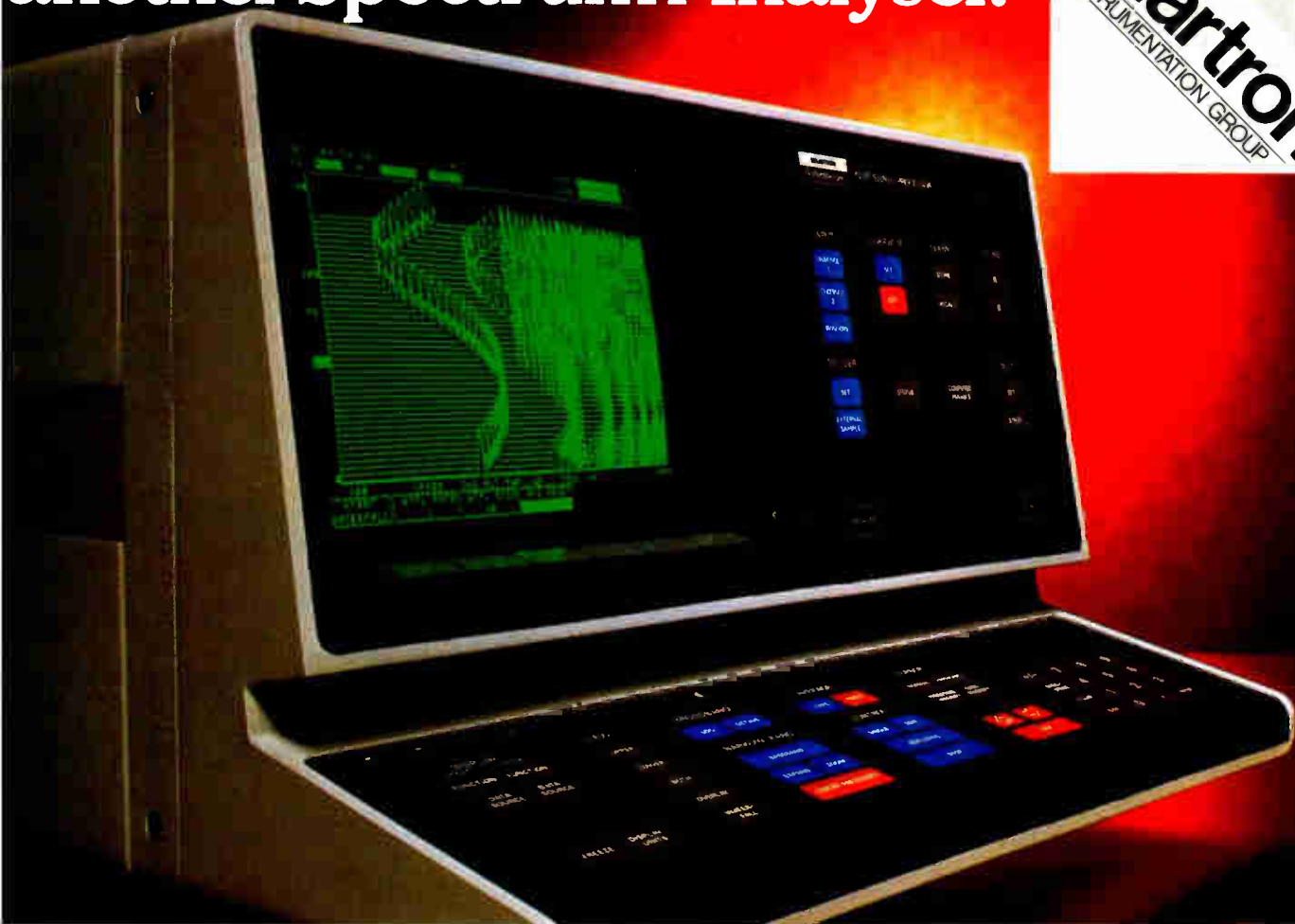
Systems designed and manufactured by SEPA for car electrical equipment automatic test, test benches automation, carburetors and distributors inspection and gearbox noise analysis are further dependable examples of SEPA's activity in the automobile instrumentation sector.



Società di Elettronica per l'Automazione S.p.A.
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More than just another Spectrum Analyser.

Solartron
INSTRUMENTATION GROUP



The Solartron 1200 Signal Processor.

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Windows: rectangular, flat-top, Hanning.
Integration, differentiation.
Engineering units.
Acoustic weightings.
Triggers, pre-triggers.
Synchronisation.

ANALYSIS

Resolution: 500 lines, 2mHz.
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Noise source: multi-sine, prbs, impulse.
Storage: analysis settings, data.
Auto- and cross-power and correlation.
Transfer function. Coherence.
Cepstrum. Synchronous spectrum.
Computed power and noise bandwidth.

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High resolution, 9-inch, raster scan.
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two functions overlaid.
Dual: two independent functions.
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Full cursor control. Variable resolution.

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IEEE 488 and plotter output.

Quite a list – and all features are standard. No need for add-on options; this is how the 1200 gives you more. A product designed with the engineer in mind and which has unrivalled ability to take maximum advantage of dynamic measurements, whether in the time or frequency domain.

Brilliant ergonomic design enables simple operation. A minimum of main controls supplemented by 'soft-keys' guide you to just the settings you need.

The 1200 provides a capability which gives unrivalled analysis of dynamic performance.

No other unit can offer such features as standard and at such a realistic price.

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8085



Z80



2650



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PMDS – Philips Microcomputer Development System – lets you get to work immediately with today's most important chips, thanks to a range of quickly interchangeable, plug-in MABs (Microcomputer Adapter Boxes). And that range is continually being updated to cover new μ Ps coming onto the market.

Available now is full support for 8085, Z80, 2650, 6809, 6500 family and 6500/1. To be added in the coming months are 6800, 6802, 6808, 68000, 8048 family and 8400 family. So PMDS is a highly versatile system, that keeps pace with your changing demands. In addition, PMDS has a powerful multi-emulation capability that allows simultaneous emulation of up to 4 different microprocessors to debug complex systems using synchronized or inter-related breakpoints, giving a complete picture of overall system performance.

68000 etc.

6800/02/08

6500/1

6500 family

6809



Multi-emulation in a 2-microprocessor system.

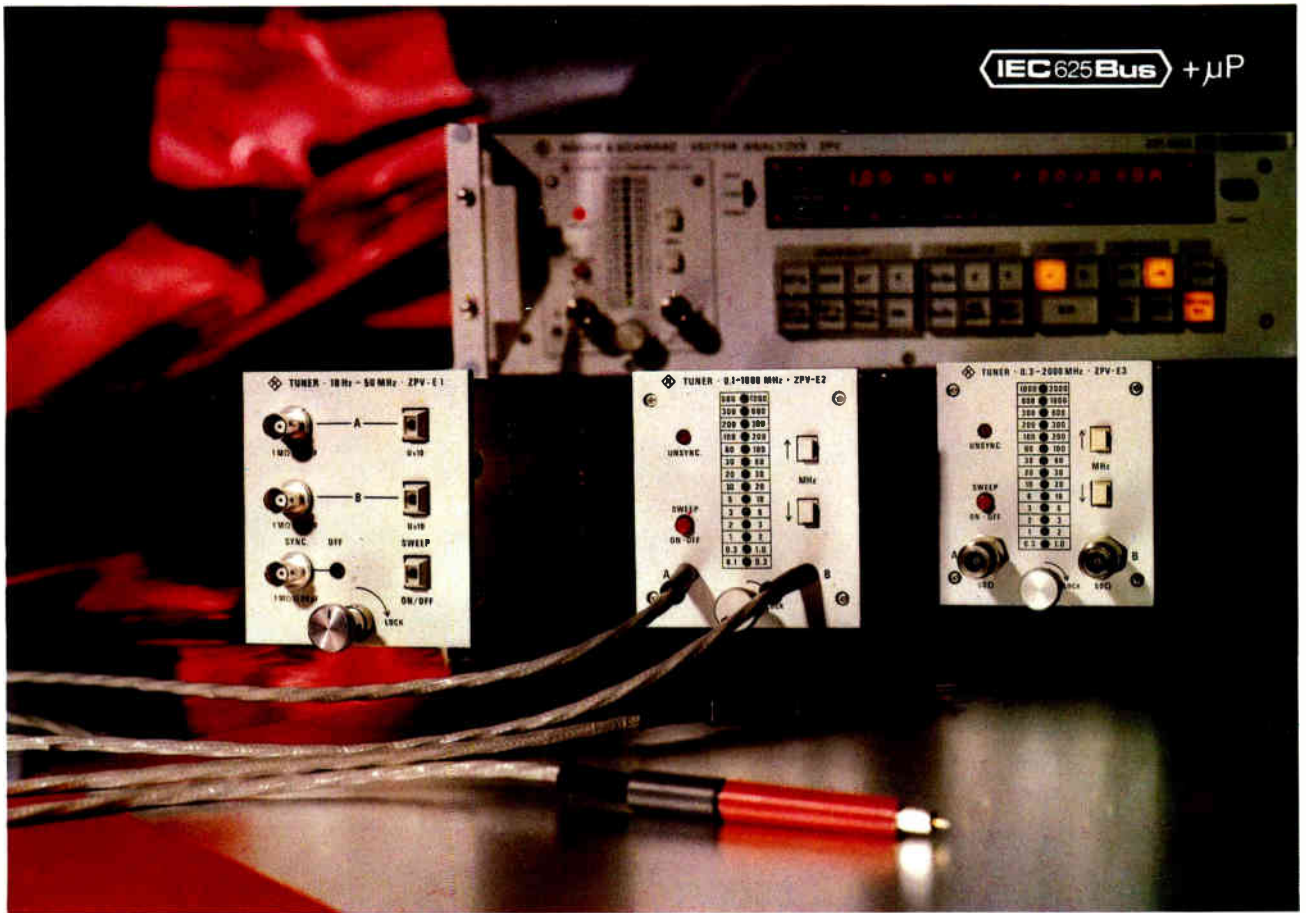
Other powerful PMDS development tools include: **PASCAL** for simple programming of 8085, Z80 and 6809 with extensive debug facilities; **real-time emulation** for testing and debugging at true system speed – up to 5 MHz for 8085-A2, 4 MHz for Z80A, 2 MHz for 68B09 etc.; **step-by-step logic analysis** with a 255-word, 48-bit wide trace memory to show you events in program and external history using pre-selected breakpoints; **symbolic debugging** with automatic cross-referencing of symbolic values to absolute hexadecimal values; and **I/O simulation** using built-in software commands to specify PMDS system elements.

And with PMDS, these tools are easy-to-use, thanks to interactive software that gives full operator guidance. To find out more about PMDS' comprehensive development tools, wide micro-computer coverage and programmed system extension, contact Philips Industries, Test & Measuring Dept., TQIII-4-62, 5600 MD Eindhoven, The Netherlands.

...Philips, of course!

PHILIPS

Network analysis for AF, video and IF circuits



The new tuner plug-in ZPV-E 1 now extends the frequency range of the vector analyzer ZPV down to 10 Hz. So, together with the other tuner plug-ins, the E 2 (0.1 to 1000 MHz) and E 3 (0.3 to 2000 MHz), the ZPV now gives you an overall range of 10 Hz through 2 GHz. The ZPV-E 1 offers:

a wide choice of parameters

voltage
phase
impedance
admittance
group delay
reflection
VSWR
s-parameters

a broad range of applications

control loops
crystals
crystal filters
AF subassemblies
video and IF subassemblies
switching power supplies
delay lines

and features like

frequency range 10 Hz to 50 MHz
dynamic range > 110 dB
sensitivity typically 1 μ V
listener/talker functions in line with
IEC 625-1 (IEEE-488)
high measuring rate
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One basic unit and three interchangeable plug-ins – that means the flexibility you need for uses from 10 Hz to 2 GHz, and at a price no similar unit can match. Ask for the new brochure:

Info ZPV-E 1

and if you're new to the world of the ZPV, ask for the 56-page
Info "ZPV Applications".

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Low-cost system lets personal computer control experiments

by Kevin Smith, London bureau

Personality modules interface with various computers; bus carries variety of analog conversion and control cards

Many an engineer has yearned to control an experiment or collect data using an inexpensive personal computer instead of a costlier minicomputer or data-logger system, but has encountered snags interfacing the computer with his or her system. Just this problem has provided a living for one small British company, Digital Design & Development Ltd., which has developed custom interfaces for the job.

Now the company has advanced a stage to market a universal interface system called Inlab that connects most personal computers to its range of interface modules. The company's modules can be configured to read parallel data, actuate external circuits, control instruments with binary-coded decimal logic inputs, sense contact closures, drive analog signals into proportional controllers, and communicate with remote terminals, to name only some possibilities.

The design approach is quite simple, says Kahtan T. Kibasi, a founder and director of the London-based firm—"to take most popular microcomputer buses and convert them into a standard interface bus." All of the company's standard interface modules, among them analog-to-digital and digital-to-analog converters, instrumentation amplifiers, multiplexers, opto-isolators, and so forth, can be directly addressed from the Inlab bus.

Physically, Inlab comprises a 19-in. card frame with DIN 4162 indirect connectors wired into a parallel backplane. A regulated power supply of ± 5 or ± 15 v occupies a card slot at one end of the rack and powers all modules plugged into the rack. A single-board controller—Digital Design calls it a personality module—for the target computer is installed at the other end of the rack to make Inlab appear either as an IEEE-488 talker-listener, an input-output mapped system, or a memory-mapped system.

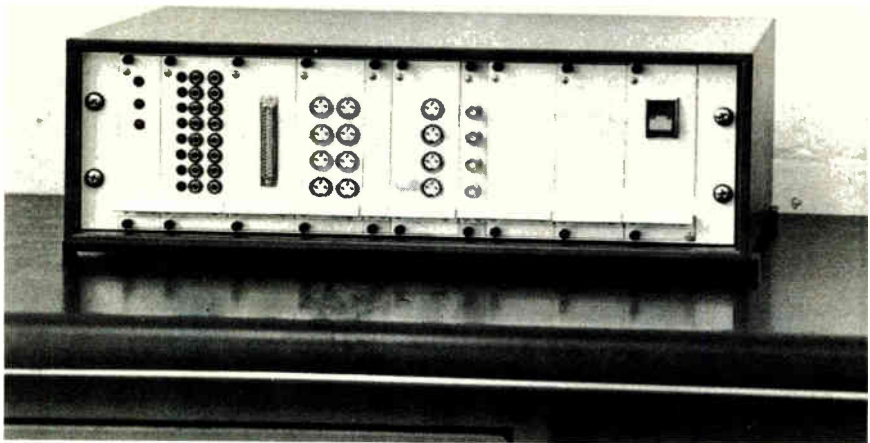
Multiple personalities. The desired interfacing with the outside world is then achieved by adding as many as 16 addressable cards from the company's interface selection. The firm has developed personality modules for most popular personal computers, among them the Commodore

Pet, Sharp MZ80, Aim 65, HP 85, Apple II, Superbrain, PDP-11, TRS-80, and VIC 20.

The interfaces vary in complexity and specification. The Apple, for example, was particularly tricky and required a card to fit into the Apple slot with address lines, buffer, and data-bus transceiver, as well as a socket for 2-K bytes of erasable programmable read-only memory.

The core of Digital Design's universal interface system is the computer interface board or personality module. It is built around an Intel 8255 programmable chip for peripheral interfacing, with its three latched bus ports connected to the Inlab's internal 24-bus lines. The 8255 accepts data, address, and control lines and proceeds to put them out in the Inlab bus format.

The unit works much like an



New products international

IEEE-488 bus with multiplexed cycles for separately addressing devices connected to it, then reading or writing data from or to the device so addressed. Port A is bidirectional and can read or write data. Port B is used with a nibble (4 bits) of port C to provide a 12-bit latched output, needed for driving the 12-bit d-a converter boards.

The last four lines of port C are used as an address-select enable. In addition to these 24 data lines, four bus lines are provided to pipe 5- and 15-v supply voltages to the boards; two lines are reserved to route analog signals to converters; and two lines carry read and bus-busy signals.

Digital Design now has a well-developed set of interface modules that includes 8-, 12-, and 13-bit a-d converter boards, multiplexing analog input boards, an amplifier card, an opto-isolated relay card, 12-bit d-a converter, a digital input card that accepts up to 6 BCD digits, an

RS-232-C serial communication card, a stepper motor indexer card, and a prototyping card.

Of course the IEEE-488 bus is designed to eliminate interface problems. But, says Kibasi, not every instrument and even fewer personal computers have that interface. Standardization aside, he believes his system can provide a cheaper solution. Many organizations will buy Digital Design's cards off the shelf, but nevertheless the company expects that some of its business will continue to come from customers wanting packaged systems.

Digital Design and Development Ltd., 18/19 Warren St., London W1 5DB, England. Phone 01 387 7388 [441]

Correction

In "Traveling-wave tube's brazed construction helps heat escape" (Sept. 8, p. 9E), the operating band of the TH3640 should have been listed as 5.850 GHz to 6.425 GHz, instead of 5.925 GHz to 6.425 GHz.

Low-cost voltage references drift only 25 ppm/°C

In line with the move towards the use of low-power high-density microcircuits is a range of low-power voltage-reference sources from Ferranti Electronics Ltd. The range of parts features a knee current of 150 μ A, excellent temperature stability, low dynamic impedance, and a choice of initial voltage tolerances of 1%, 2%, and 3%.

Initially, the reference line will consist of three generic types with voltages of 2.5, 5, and 10 v, designated ZNREF025, -050, and -100, respectively. These devices will be offered in full military and commercial grades. The full military grade, for example, will have a typical temperature coefficient of 35 ppm/°C and a maximum of 50 ppm/°C over the operating temperature range, -55° to +125°C. The commercial-

\$595?



\$595!

Yes, it's true.

The best selling terminal in its class now has the best price in any class.

That's the only way we could've improved our Dumb Terminal™ video display. We had already done everything else so well that the Dumb Terminal was renowned the world over. With over 150,000 shipped, and more on the way every day.

So now you can buy the ADM 3A for a mere \$595 (quantity one), and the ADM 5 for a paltry \$645. But don't let the price tags fool you. They're the same, dependable Dumb Terminals they've always been. We didn't change that.

The ADM 3A still has all the same reliable features that made it a best-seller. And the ADM 5 has even more operator conveniences. Like reverse video, reduced intensity and reverse video/reduced intensity. Limited edit-

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grade device will have a temperature coefficient of 15 ppm/°C typical and 25 ppm/°C maximum over the temperature range of 0° to 70°C.

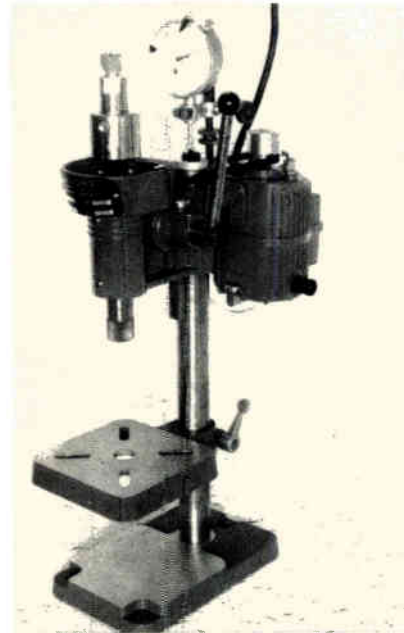
In volume, the devices will cost in the region of \$1 for the 1% tolerance part (with the 10-v part priced at about \$2). They are available in a three-lead transistor package, the third pin of which can be used to trim the output voltage over a $\pm 5\%$ range.

The design of these references uses an entirely new circuit concept, one feature of which is the ability to change reference voltage by a single interconnection-pattern modification. Already 4.0- and 6.2-v versions have been designed and will be added to the range in the near future. Applications include data-acquisition systems, portable instruments, codec systems, and digital voltmeters.

Ferranti Electronics Ltd., Fields New Road, Chadderton, Oldham OL9 8NP, England [462]



The Intellect 100 image-processing system comes in a desktop configuration for research and production-line applications. For more demanding tasks, the Intellect 200 multipurpose system is available. Micro Consultants Ltd., Kenley House, Kenley Lane, Kenley, Surrey CR2 5YR, England [442]



This ceramic drilling machine is capable of drilling holes from 0.001 to 0.25 in. in diameter in materials such as ceramics or glass. A 1/8-in.-deep hole can be drilled through glass in 3 to 4 seconds. The Meclec Co., 5/6 Towerfield Close, Shoeburyness, Essex SS3 9QP, England [448]

ing with erase to end of line and erase to end of page (which reduces the load on your host computer). A gated extension port. Even a full integral numeric keypad. And they said it couldn't be Dumb.

So there you have it. The same two proven Dumb Terminals, two new low prices to save you even more money.

And when you think about it, saving money is a pretty smart idea.

Contact your nearest Lear Siegler Authorized Distributor or: Lear Siegler Data Products Ltd., Orchard House, Connaught Road, Brookwood, Surrey GU24 0AT, United Kingdom Tel: Brookwood (048 67) 90666 Telex: 859415



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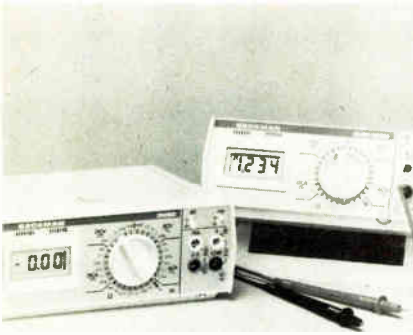
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\$645?



\$645!

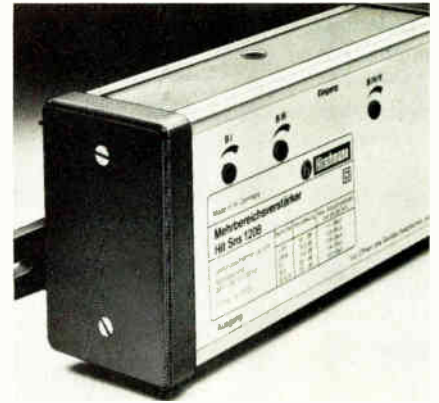
New products international



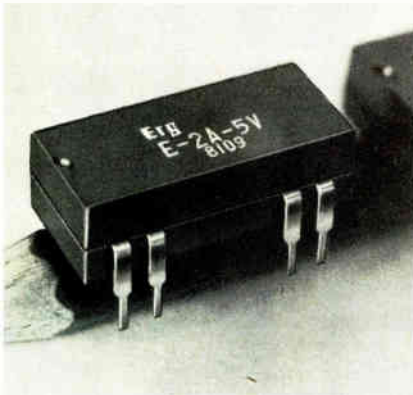
Benchtop multimeters with sine-wave (model 3050) or true root-mean-square (model RMS 3060) calibration measure voltages up to 1.5 and 1 kV, currents to 10 A, and resistance to 20 M Ω . Beckman Instruments Ltd., Mylen House, 11 Wagon Lane, Sheldon, Birmingham B26 3DU, UK [443]



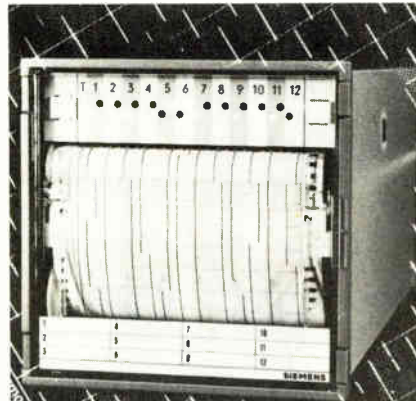
The Adcola 444 electronically controlled soldering tool operates from a 24-V, 50-A, 50-Hz supply and heats to a point adjustable from 220° to 420°C. It is free of line interference or magnetic effects. Adcola Products Ltd., Adcola House, 113 Gauden Rd., London SW4 6LH, England [446]



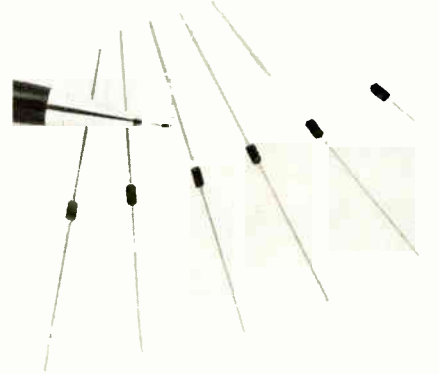
Type Sns 1208 is a multirange amplifier for use in fm radio and all television ranges. It provides output levels between 102 and 105 dB μ V at typical amplification values of 20 dB. It is intended for community antenna systems. Hirschmann, P. O. Box 110, D-7300 Esslingen, West Germany [450]



The E-2A-5V dual in-line reed relays are impervious to flow soldering and solvent cleaning. They have two make-break contacts, a coil resistance at 25°C of 200 Ω , and a mean time before failure of 4.7×10^8 operations. Erg Industrial Corp., Luton Road, Dunstable, Beds. LU5 4LJ, England [444]



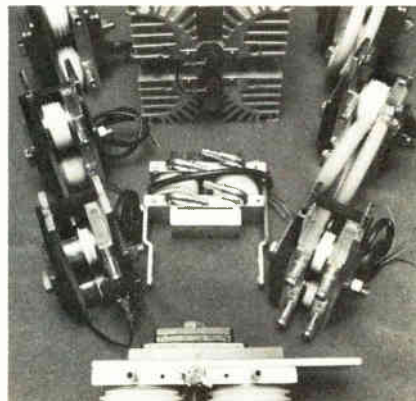
The 144-by-144-mm multigraph records on thermosensitized paper the state of up to 12 independent objects and enables their operational status to be signaled by light-emitting diodes. Siemens AG, Zentralstelle für Information, Postfach 103, D-8000 Munich 1, West Germany [447]



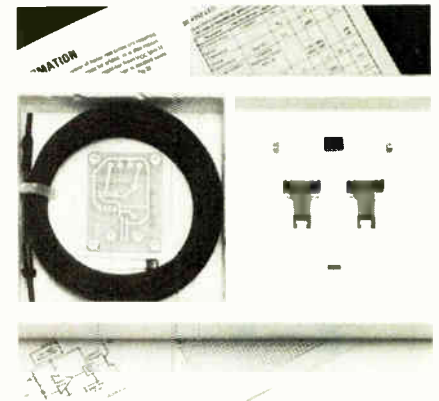
BZY88-series and 5-W axial zener diodes have power ratings of 400 mW to 5 W and voltages of 2.7 to 51 V. Nonstandard tolerances (down to 1%) and voltages are supplied on request. They come in glass or epoxy packages. Diodes Ltd., 16 The Broadway, Newbury, Berks RG13 1AZ UK [451]



The Milli-TO measures resistances of 0.1 m Ω to 2×10^{14} Ω . The measuring dc test current is limited to 500 mA in the low-resistance range. Measuring voltages are 10, 100, and 500 V. Dr. Kamphausen GmbH, Aachener Str. 30/31, D-1000 Berlin 31, West Germany [445]



Water- and air-cooled solid-state ac controllers for electric resistance welders deliver currents of 0.500 to 0.3300 A root mean square at peak voltages up to 2,900 V and with nonrepetitive surge currents up to 21 kA. Marconi Electronic Devices Ltd., Carlholme Road, Lincoln LN1 1SG, UK [449]



In the SPX 410 fiber-optic link kit are a Sweet Spot light-emitting diode, driver circuit, Schmitt-trigger receiver, 5 meters of fiber-optic cable, and connectors. Honeywell Control Systems Ltd., Honeywell House, Charles Square, Bracknell, Berks. RG12 1EB, UK [452]

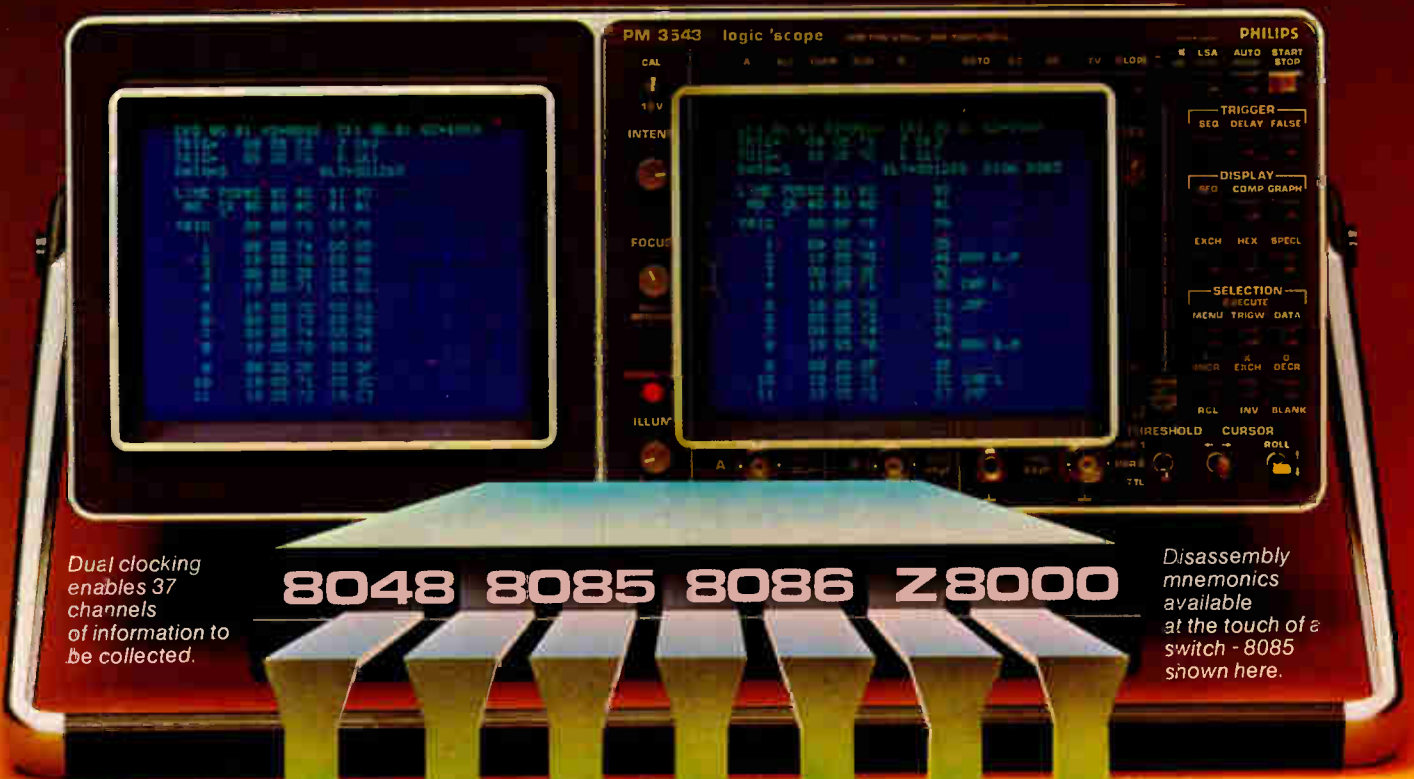
Logical Logic Analysis

The only logical way to analyse multiplexed data is to demultiplex it. Which is just what Philips PM 3543 and '42 Logic Analyzers do.

Moreover both instruments feature a disassembler

option, allowing data to be displayed in the same language as the relevant processor.

So what you see, is what you thought and wrote... for most popular 8- and 16-bit μ Ps.



Dual clocking enables 37 channels of information to be collected.

8048 8085 8086 Z8000

Disassembly mnemonics available at the touch of a switch - 8085 shown here.

LAs with dual clocks mean that multiplexed address and data can be captured sequentially, but displayed side-by-side, on the same line. Philips LAs also make the same kind of savings on probe connections as the multiplexed devices make on pins.

This makes PM3542 ideal for 8-bit μ Cs like the popular 8048,

while PM3543 covers all 8-bit and multiplexed 16-bit μ Ps.

The multiple disassembly option enhances analysis even further by supporting the 8048, 8080, 8085, Z80, 6800 and 6502 in a single package. (Note: a single package supporting 8086/88, Z8000, 6809 and 1802 will be available by end '81.)

Both LAs feature a real-time

analysis facility, allowing the software instruction and hardware implementation to be related directly. They also, as an added bonus, function as excellent 35 MHz/2 mV oscilloscopes.

Full details from:

Philips Industries, TQ III-4-62, Eindhoven, The Netherlands.

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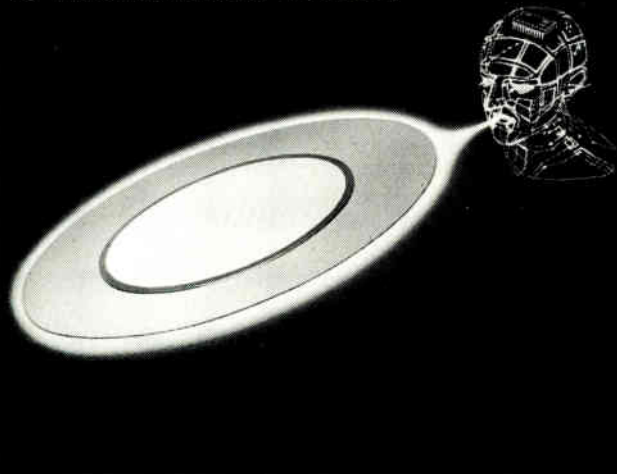
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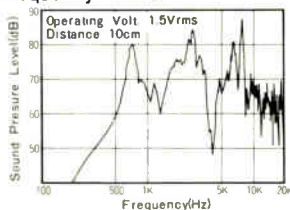
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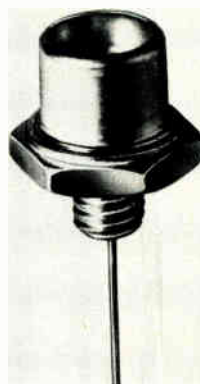
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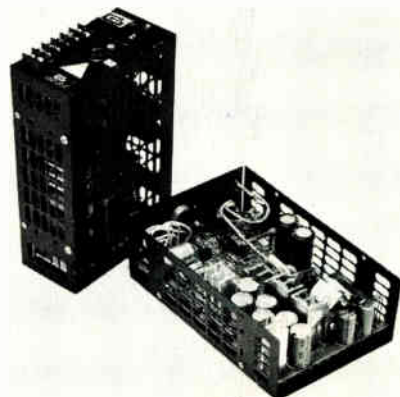
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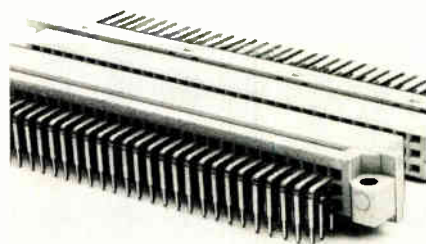
New products international



The QCW 123 continuous-wave laser diode provides 6 mW of power at a threshold current of 200 mA and at an operating current of 250 mA. The 1.3- μ m laser diode comes in a modified TO-5 package. Laser Optronics GmbH, Eversbuschstr. 200, D-8000 Munich 50, West Germany [453]



The GMOS range of 50-W switching power supplies have outputs of ± 5 , ± 12 , ± 15 , or ± 18 V dc. Their mean time between failures is 250,000 hours, and input voltages range from 198 to 264 V ac. Gresham Lion Ltd., Gresham House, Twickenham Road, Feltham, Middlesex TW13 6HA, England [454]



The 1696 two-part printed-circuit connector comes in two or three rows with up to 96 contacts inlaid with gold up to 3.0 μ m thick, on 2.54- or 5.08-mm centers. Contact resistance is at most 20 m Ω . Ultra Electronic Components Ltd., Fassetts Road, Loudwater, High Wycombe, Bucks. HP10 9UT, UK [455]

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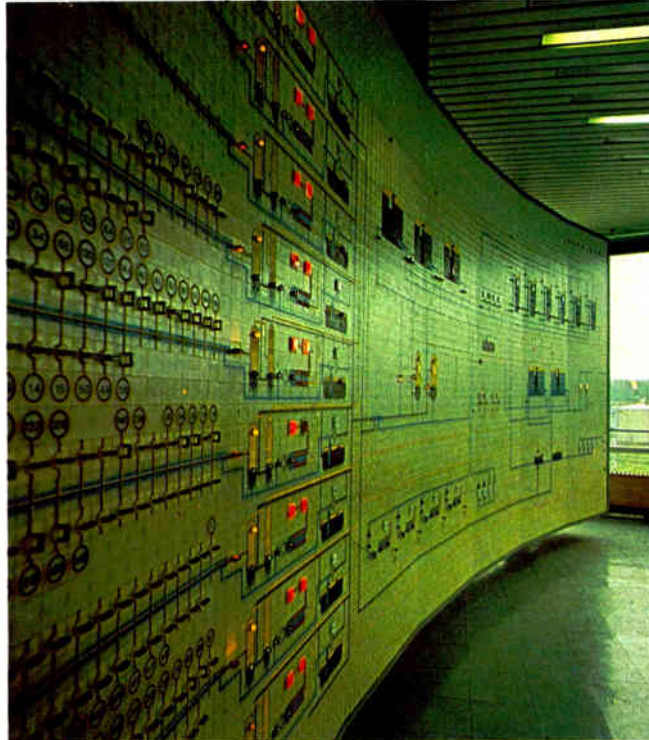
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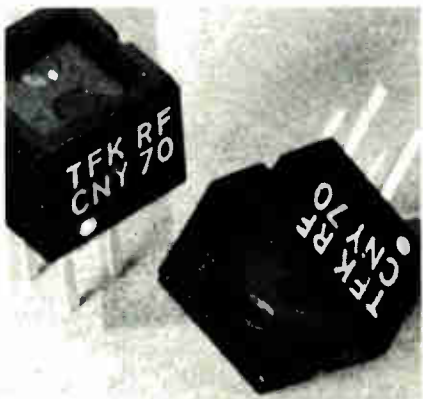
New products international



The model CM 5000 5 1/4-in. Winchester drive stores either 5.3, 10.7, or 16 megabytes, depending on the number of disks. All three have an average access time of 105 ms and feature a recording density of 8,650 b/in. Kontron GmbH, Breslauer Str. 2, D-8057 Eching, West Germany [456]



Types BPZ and BPX high-precision resistors have temperature coefficients of less than ± 1 ppm/ $^{\circ}$ C and a long-term instability of less than 0.01%. They come in values between 10 Ω and 100 k Ω and dissipate up to 0.7 W. Burster, Talstrasse 1-7, D-7562 Gernsbach, West Germany [457]



Optoelectronic reflex coupler CNY70 uses a gallium arsenide luminescence diode as a transmitter and a silicon npn phototransistor as a receiver. It has a high sensitivity and low temperature coefficient. No adjustments are necessary. AEG-Telefunken, P. O. Box 1109, D-7100 Heilbronn, West Germany [458]

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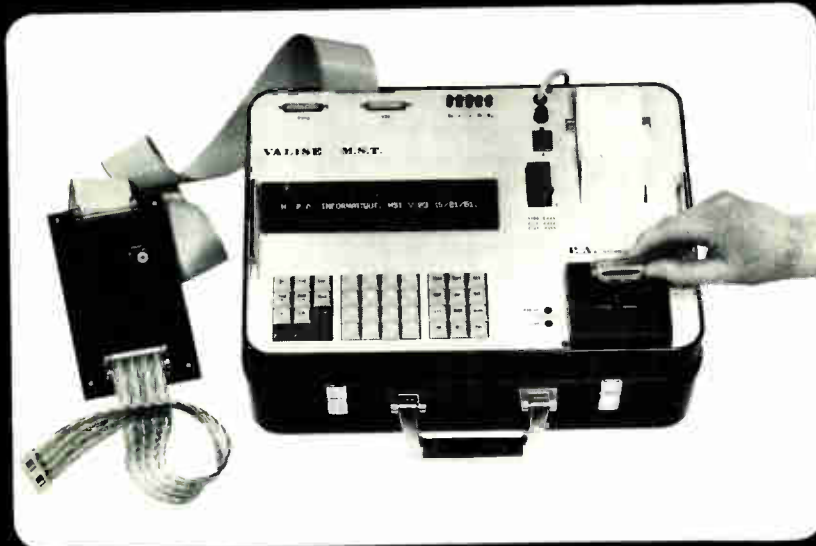
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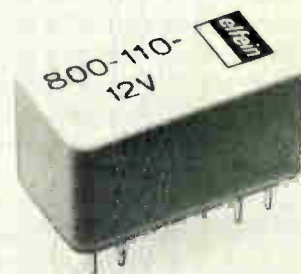
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The FM77T liquid-crystal-display frequency meter, for radio-receiver applications, measures frequencies up to 3.999 MHz. Stability is better than ± 1 digit over a 10° -to- 30° C range. Thurlby Electronics Ltd., Office Suite 1, Coach Mews, The Broadway, St. Ives, Huntingdon, Cambs. PE17 4BN, UK [459]



The series 800 relays have coils that operate at frequencies five times higher than conventional types. Current consumption for the 5-V version is only 3.8 mA, for the 12-V version 2.1 mA, and for the 24-V model 1.5 mA. Elfein GmbH, Weiner Str. 120, D-6000 Frankfurt, West Germany [460]



The MD206 meter measures ac and dc voltage, current, and resistance in 32 ranges. It has an electronic probe that covers temperatures from -55° to $+125^{\circ}$ C with an accuracy of $\pm 1^{\circ}$ C. The Weir Electrical Instrument Co., Bradford-on-Avon, Wiltshire BA15 1BU, England [461]

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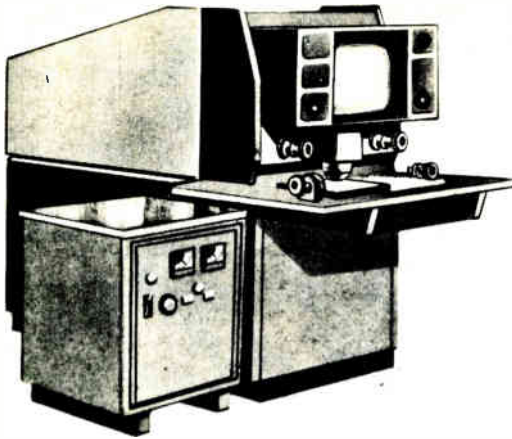
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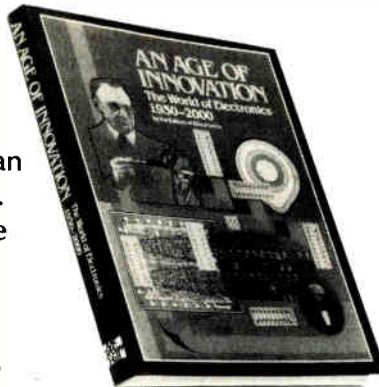
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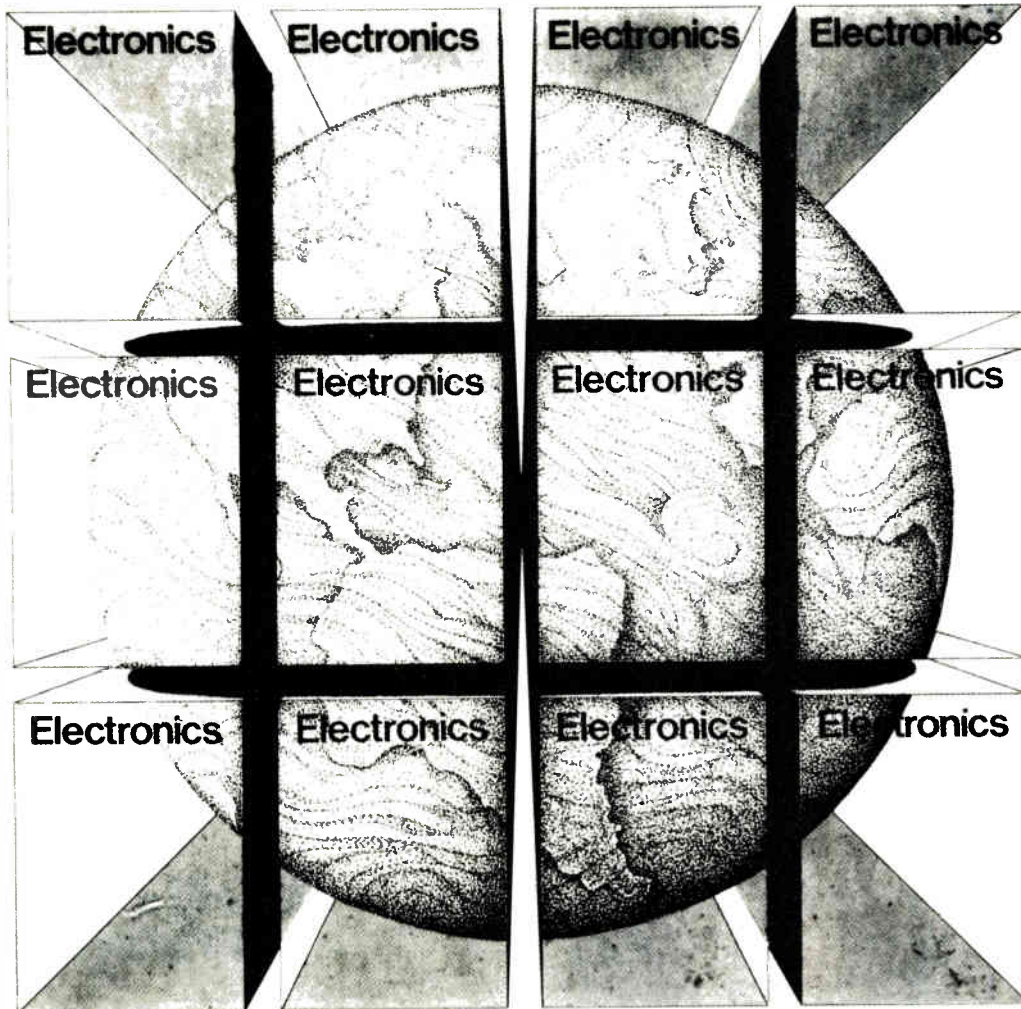
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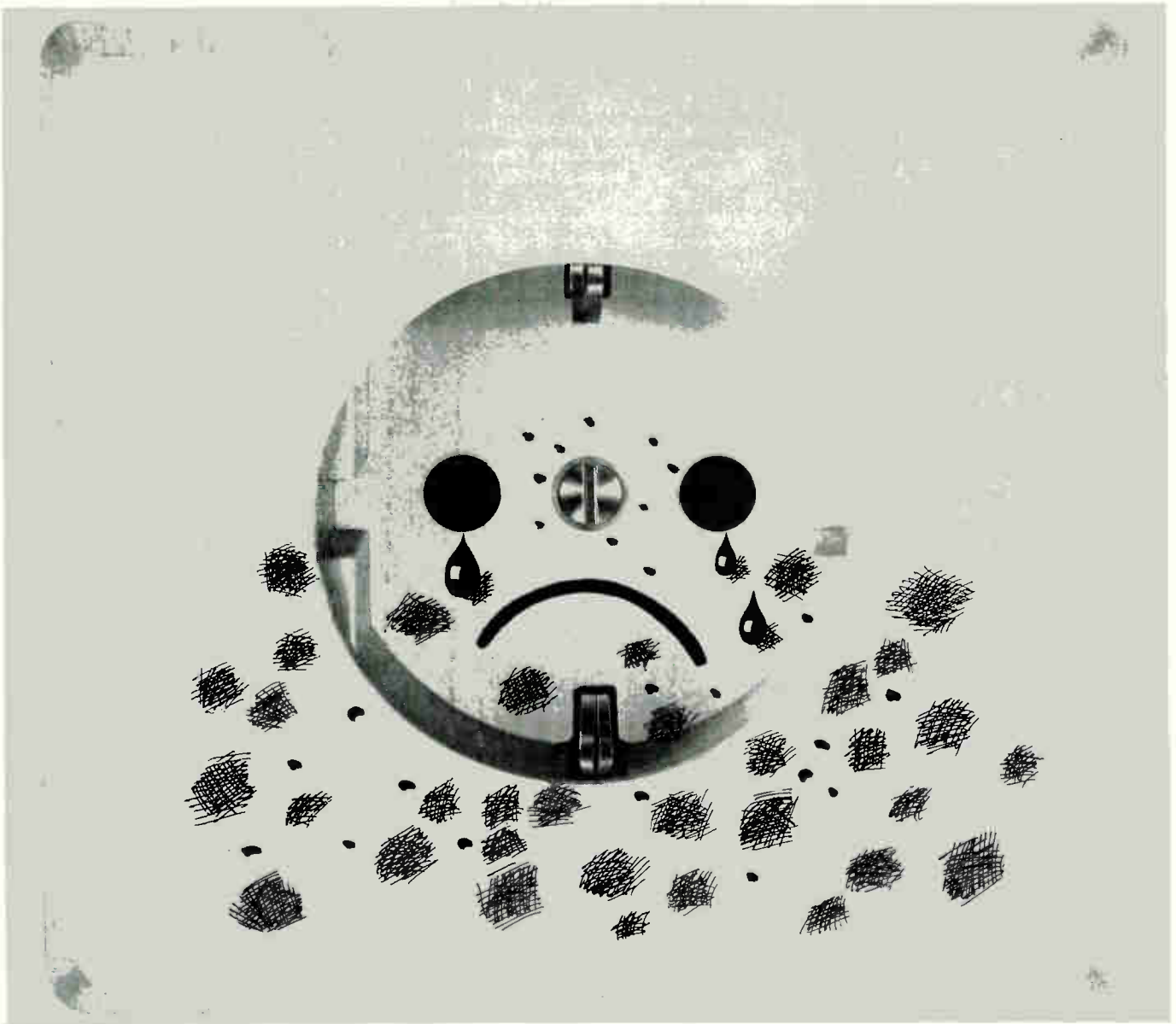
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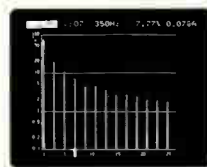
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Characteristics

Test Conditions
unless otherwise specified
TA = 25°C, V_A = 5V or 12V
V_B = V_{EE} = 0V

Symbol	Min	Max	Units
1 Valid			
2 Acceptable Signal Le			
3 Max			
4 Min T			
5 Frequ			
6 Differ			
7 Common			
8 Common			
9 Dial Tone			
10 Tone Pres			
11 Tone Abs			
12 Guard Time			
13 Guard Time			
14 Time to Re			
15 Invalid T			
16 Accept			
17 Accept			
18 Data V			

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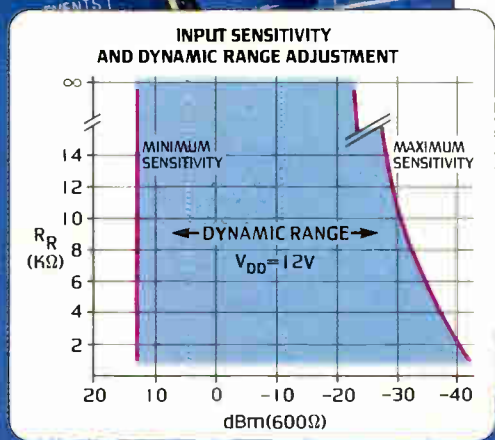
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BUILDING BETTER COMMUNICATIONS

Circle 96 on reader service card

World Radio History

Big ROMs find market waiting

256-K chips will be needed for 16-bit microprocessors
as Japanese manufacturers jump off to head start

by Charles Cohen, Tokyo bureau manager, and John G. Posa, Solid State Editor

The big ROMs are coming: read-only memories capable of storing a quarter megabit of data. But who needs all that mask-programmed storage anyway? After all, two such devices completely consume the entire address space of most 8-bit microprocessors.

However, applications like program storage for newer 16-bit machines abound, some of which will evolve to put high-level-language compilers or operating systems in ROM. Speech-recognition and -synthesis systems also eat up ROM bits, as do some look-up tables for cathode-ray-tube displays.

Japanese chip makers are further along on a 256-K ROM than U.S. firms—a key reason being the large amount of data required to display kanji characters. Despite their size, nine 256-K devices are needed for a comprehensive set.

U.S. companies are moving along on their 256-K ROMs, though, with several product announcements expected next year. In fact, unlike some Japanese parts, which essen-

tially exploit scaled-down design rules to cram more bits on a chip, devices from U.S. manufacturers will employ clever circuit techniques or proprietary support devices for higher speed or easier operation.

Mostek Corp. of Carrollton, Texas, for example, is finishing internal evaluations of its 38000 for sales early next year. It is considering the design of a companion part, called a patch chip, that would perform address translation like a rudimentary memory management unit.

Motorola Semiconductor in Austin, Texas, a leading supplier of 64-K ROMs, is also expecting to begin shipping its 0.25-Mb version early next year. To conserve chip area, it is toying with the idea of using a four-state cell that stores two data bits at each location. Intel Corp., Santa Clara, Calif., used this structure to build the control ROM in its 8087 mathematics microprocessor chip [*Electronics*, Feb. 24, p. 102], citing an overall area savings of 31% over standard ROM cells.

In Japan, five firms are producing

eight different 256-K chips. Fujitsu Ltd. already offers an off-the-shelf nine-chip set for a sample price of \$311 a set. The set contains a total of 453 alphanumeric characters and symbols—including Roman, Greek, and Russian alphabets and Japanese phonetic syllabary characters—and 2,965 Chinese characters for a Japanese language display printout.

Big capacity. For Western languages, the same memory capacity would provide a spelling dictionary of 288,000 characters—around 50,000 words for spelling only, or somewhat fewer for spelling and hyphenation. In addition, manufacturers on both sides of the Pacific will be able to use Basic and other language interpreters or compilers, which are normally written in English. The price should be right as production increases and other devices push the figure down toward the price set by Toshiba Ltd.—\$13 in lots of 50,000.

The majority of the devices are programmed in the channel of the memory-matrix transistors by ion

JAPANESE 8-K-BY-8-BIT READ-ONLY MEMORIES

	Fujitsu	Hitachi		Toshiba		Nippon Electric	Sharp
Part number	MB83256	HN61256	HN623256	T6745	TMM23256P	μPD23256	LH53256
Design rule and technology	2-μm p-well C-MOS	3-μm p-well C-MOS	2-μm p-well C-MOS	3-μm clocked C-MOS	2-μm n-channel MOS	2.5-μm n-MOS	3-μm n-well C-MOS
Chip/cell area (mm ² /μm ²)	30.6/63.8	37.2/63	27.5/49-56	40.7/65.7	24.3/48	35 (target)/...	36/49
Programmed layer/step	field oxide	depletion implant	enhancement implant	depletion implant	enhancement implant	drain contact via	depletion implant
Access/cycle time (ns)	250/250	3,500/4,000	250/250	350/420	150/230	250/250	380/380
Active/standby current (mA/μA)	16.6/33	3/50	20/30	5 at 1 MHz/n.a.	40/10,000	160/...	12/0.1
Availability/intended use	now/kanji set and later, custom	now/word processor, printer, translator	March 1982/displays, microcomputer programs	1982/word processor	Oct. 1981/displays, microcomputer programs	March 1982/kanji word processing	now/speech, kanji, translator

Probing the news

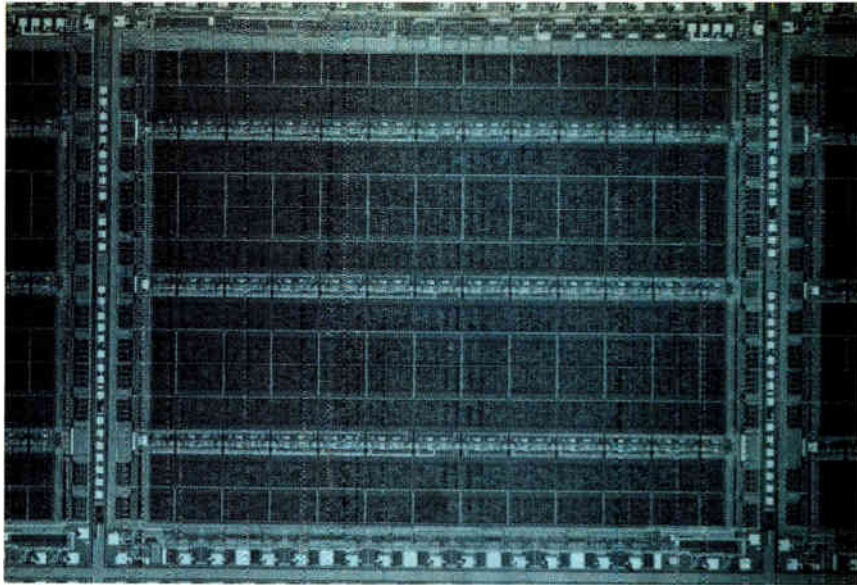
implants because designers feel that the implants provide the best trade-off between turnaround time and device performance. However, there is no consensus on the best type of implant. They range from a depletion type to a mode-enhancement threshold implant used by Hitachi, which raises the threshold of a regular-enhancement transistor to a value so high that it can never be turned on.

Nippon Electric Co. programs its n-channel-MOS device using the through-hole for drain contacts, the next-to-last fabrication step, for the fastest turnaround. Eiji Noguchi, manager of the static-memory-design section, says Fujitsu programs its devices using gate-oxide thickness, the second process step, because it allows a small cell even though turnaround time will be the longest in the industry.

Devices for CRT displays and microcomputer languages follow standard microcomputer practice. The power supply is a single 5 volts, access time is 250 nanoseconds maximum to match a 4-megahertz Z80 or similar processor, and the package is a 28-pin plastic dual in-line package with a version B pinout as set by the Joint Electron Device Engineering Council.

Fast and slow. Toshiba, though, has developed a high-speed device, which gives it the fastest as well as the slowest device on the market. The company says that an access time of 100 to 150 ns is needed for word processing with vertical CRTs, which have more runs of type than the common horizontal variety. It selected n-MOS because it is smaller and cheaper than complementary-MOS.

It is in the so-called education market—which includes handheld calculators—and in games that non-standard devices will probably proliferate. Here, low speed is no problem. Requirements in this market may include essentially zero leak current during standby, low-voltage operation, and packaging in small or miniature flatpacks. Three of the five firms are now participating in this market, where the designer has



More efficient. Toshiba's 288-K ROM is organized by 6 bits rather than by 8. Each 6-bit word can store one alphanumeric or Japanese character, giving 33% more capacity.

the greatest freedom to depart from the usual standards—albeit with a new set of constraints.

A C-MOS ROM from the fifth Japanese company making the devices, Sharp Corp., works at an “awkward speed that is higher than that needed by in-house users yet not fast enough for many CRT displays,” says a spokesman. It was actually designed to be modified in the future for lower-power handheld applications. Thus, it has an unconventional n-well configuration with the n-channel memory matrix fabricated in the substrate.

The company says that the doping profile in the substrate is constant up to the surface, rather than decreasing near the surface as it does in boron-doped p-wells. This profile means that the devices can be designed for operation from 3-v and even 1.5-v power supplies with threshold voltages as low as 0.4 v without incurring the subthreshold leakage current to which p-well devices would be prone.

Six bits match. Nobody will accuse Toshiba of settling for a compromise speed for its 288-K ROM, which is designed with a by-6-bit organization that matches the bus of the microprocessor with which it is used. It is also more efficient than a by-8-bit organization in educational applications because each 6-bit word can store a single alphanumeric or Japanese syllabary character, allowing the device to hold 33% more characters.

The 4-to-5-v chip rating is close to the standard 5 v and can be drawn

from three dry cells. Hiroaki Suzuki of Toshiba says the associated microprocessor and liquid-crystal display suffer from low voltage before the ROM does. A p-well design with p-channel MOS memory-matrix transistors is used because of extensive p-MOS experience in calculators, and an AND-OR arrangement with the many memory cells in series helps to keep the device compact despite the 3-micrometer rules. Dynamic circuits and some clocked C-MOS peripheral circuits are also used by Toshiba's designers.

Processors and toys. A more standard clocked C-MOS 256-K ROM from Toshiba will be packaged and specified differently in word processor, custom education, and toy applications. The n-well device also used AND-OR configuration and dynamic circuits, but fewer cells are in series because of the needed 250-ns access time. For this version, only maximum power is specified.

The custom version for education products is packaged in a miniature flatpack and operates from a 3-v power supply, with standby current rather than maximum power specified. Although the typical speed is 250 ns, maximum access time is almost twice that.

Toshiba's latest 256-K ROM, the T6793, is designed to store data for a parcor (partial auto correlation) speech synthesizer. Although the chip is organized internally as a byte-wide 256-K device, the technology is essentially the same as that used in Toshiba's 288-K model, and it will sell for the same price. □

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Design support.

A keyboard Encoder (CDP1871) com-

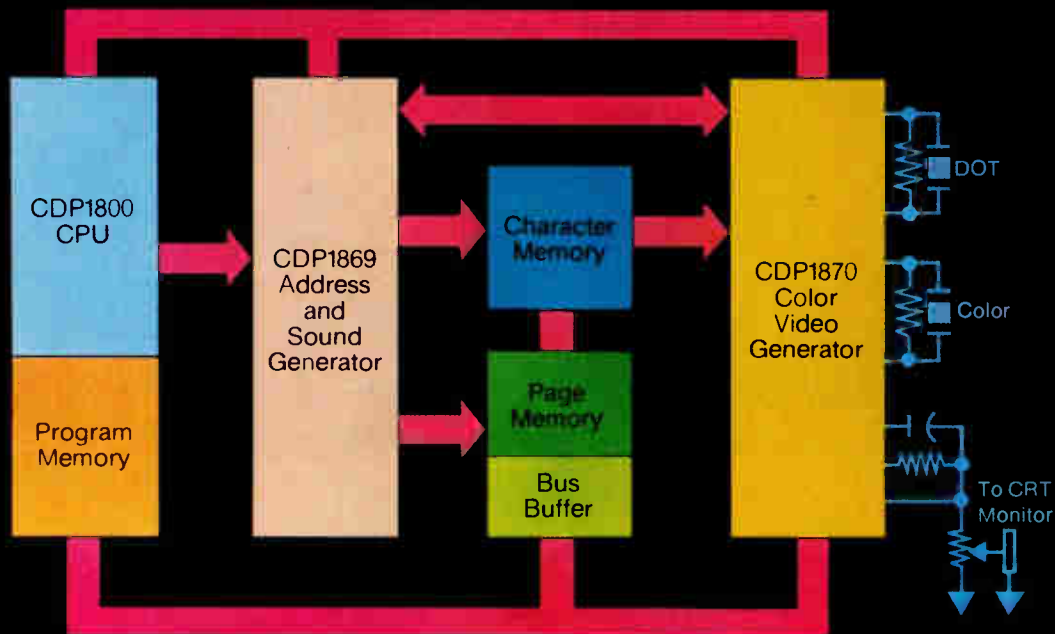
pletes the VIS interface package.

A VIS Interpreter, available on diskette, provides simple instruction codes that allow you to display character, graphics or motion, or to generate audio tones. You can also add your own instructions for special applications.

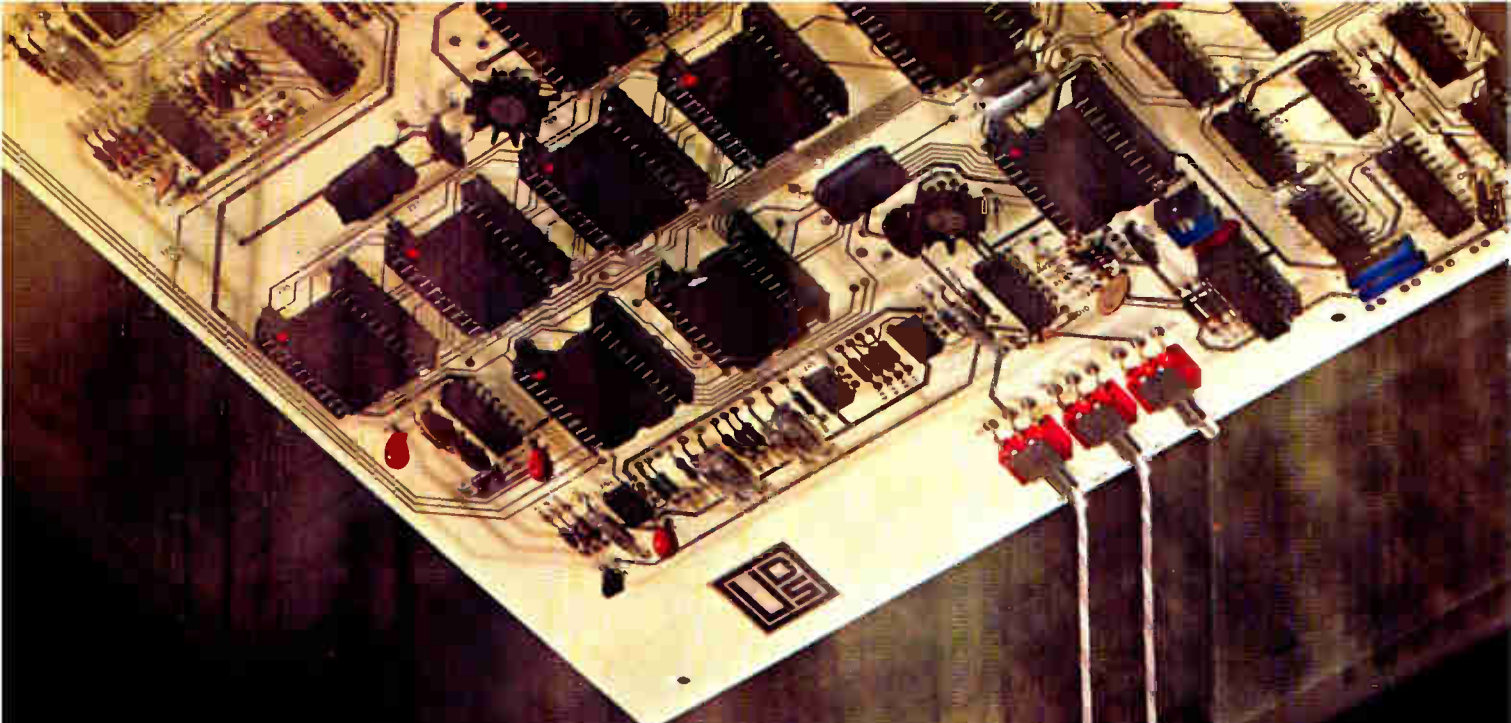
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Solid state

Silicides nudging out polysilicon

Pure metals are also being used, as VLSI circuitry demands lower sheet resistivity than the old standby can provide

by John G. Posa, Solid State Editor

Polysilicon, perhaps more than any other material besides single-crystal silicon itself, has allowed electronic circuits to be integrated on a very large scale. Suitable both for gate electrodes and interconnections, polysilicon has given the MOS transistor its short, self-aligned channel regions, and this has led to today's dense, fast chips.

But now polysilicon is being replaced with metal silicide—or pure metals, in some cases. The reason: even with the highest practical doping, the sheet resistivity of polysilicon cannot go much lower than about 10 ohms per square, a value that threatens to impede further advances in the performance of very large-scale integrated circuits.

Thanks to the need—and now, the means to process these tricky materials—metal silicides are finding their way into commercial MOS ICs. For instance, Standard Microsystems Corp. is using titanium disilicide to enhance the performance of its video-display attributes-controller chip (see photograph at right).

Faster. Before addition of the silicide, the chip supported a video dot rate of 20 megahertz, fast enough for cathode-ray-tube displays with 24 rows of 80 characters. With silicide, the dot rate jumped to 25 MHz—enough for 132-by-24-character displays and new markets.

All SMC had to do to the chip, called the CRT 8002H, was deposit the silicide. It did not have to add mask steps or adjust device layout. In fact, according to Paul Richman, president of the Hauppauge, N. Y., company, his silicide process is “totally compatible with standard MOS technology.”

Processing incompatibilities are the reason commercial MOS chips were not endowed with silicides earlier, even though bipolar products have used them for a long time. “Essentially, every bipolar device since the mid-1960s has used platinum-silicide contacts,” explains Martin Lepselter, director of Bell Laboratories' Murray Hill, N. J., advanced development laboratory, adding that just about all Schottky-TTL logic ICs employ silicide contacts.

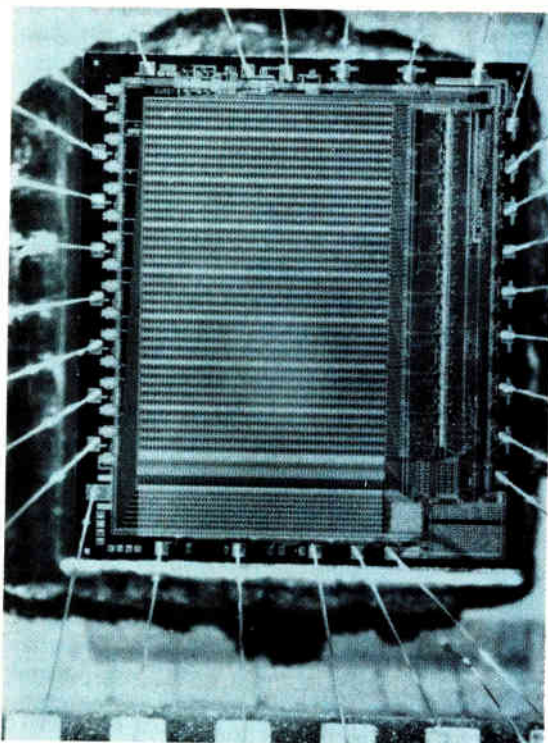
“But MOS circuits are more delicate” to work with, Lepselter continues, and prior to VLSI density levels, doped polysilicon sufficed. Silicide

formation on MOS circuits is trickier because the material has to be put on gate electrodes, and these rest on the thin gate oxide. In addition, the deposition has to be followed by etching and, usually, high-temperature passivation or oxidation. Bipolar chips, in contrast, use the silicides later in their processing and then only for contacts.

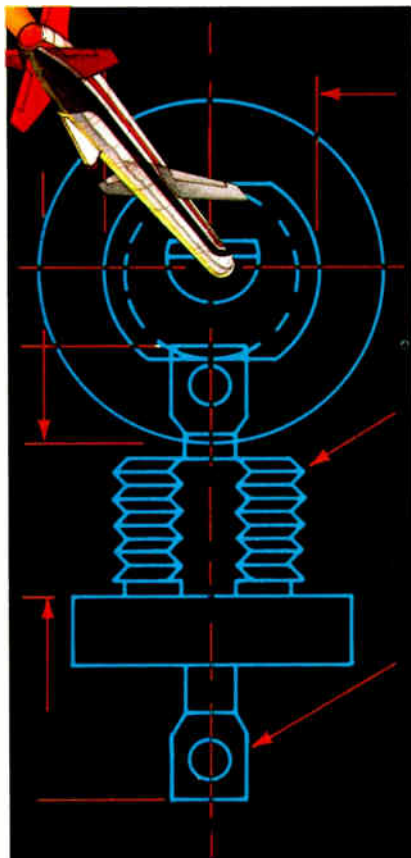
Choices. After concluding that silicides are essential, a MOS chip maker is faced with several options, the most crucial of them being which refractory metal to use. The factors that go into choosing a silicide include its resistivity and formation sequence, as well as compatibility with the particular manufacturer's fabrication sequence such as the etchants and temperatures used.

Richman says that SMC's choice of a material was reduced to titanium and tantalum. The former silicide was chosen because, in his words, “You might as well start off with the one that has the lowest resistivity.” With the company's titanium disilicide, sheet resistivity fell to less than 1 Ω /sq, compared to about 2 Ω /sq with tantalum. Titanium also features an advantageously lower annealing temperature—about 800°C versus 1,000° to 1,500° for tantalum.

A problem with titanium is that it is attacked by the most common wet



Silicized. The use of silicides on this MOS cathode-ray-tube display-attributes controller may evade the naked eye, but performance was increased by 25% at its pins.



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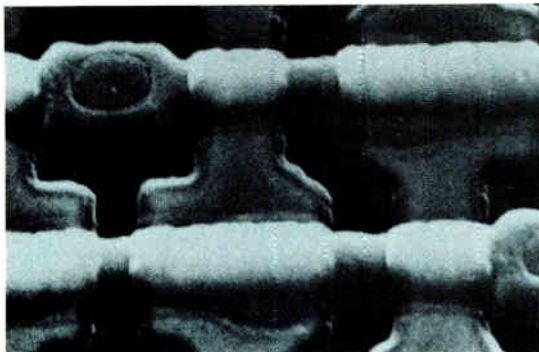
SPECTRUM CONTROL INC.

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Probing the news

chemical etchant: buffered hydrofluoric acid. SMC got around this problem with dry etching, a process that is already used extensively by the company.

Lepselter also cites low resistivity as a big asset for $TiSi_2$, adding that tantalum is a good second choice if



RAM rouser. A big application for silicides is in large memories where word-line delays threaten to stunt performance. This IBM memory cell uses tungsten silicide.

compatibility with existing processes that use wet etching must be met. That is Bell's main reason for pursuing tantalum for its MOS work.

Platinum, Lepselter points out, is attractive because it forms metal-rich $PtSi$ instead of $PtSi_2$. It also allows Schottky contacts with some of the highest voltage barriers possible, a property that Bell has exploited to build MOS transistors with Schottky drain and source contacts requiring no diffusions or implants at all.

Some troubles. Lepselter believes that tungsten and molybdenum are two of the most difficult materials to work with, and Richman agrees. The trouble stems from what Lepselter calls the pest reaction: incompatibility with silicon may cause microcracks to form—particularly with molybdenum—or the material might peel off or blister. Nevertheless, molybdenum silicide is extremely popular in Japan. The Nippon Electric Co., Toshiba, Sanyo Electric, and Matsushita have built memories or other devices with $MoSi_2$, and some are now starting to see commercial production.

Titanium is emerging as one of the most popular metals for silicide formation on MOS chips in the U. S.

Besides SMC and Bell Labs, Texas Instruments is fond of $TiSi_2$ and has been able to experimentally etch 1-micrometer-wide gates.

IBM Corp. has applied tungsten silicide to a MOS random-access memory. This procedure allows a simpler cell structure that needs only one polysilicon layer instead of two (see photograph below).

However, some chip makers, both in the U. S. and abroad, are electing to go with pure metal in lieu of silicides as polysilicon replacements. Intel and Hewlett-Packard, for instance, are using tungsten, and NEC, Matsushita, and others in Japan are experimenting with pure molybdenum in addition to its silicides.

The attraction of metals, of course, is their higher conductivity than silicides. However, they can melt, evaporate, or form silicides when heated, so techniques like low-temperature chemical vapor deposition are a must here also.

At Intel Corp.'s new Livermore, Calif., facility, researchers have devised a process that puts all high-temperature steps before the deposition of pure tungsten to avoid the unwanted effects from heating. The technique also permits the selective deposition of the tungsten only to silicon or polysilicon areas; thus, they can use the material both for gates and source and drain contacts without etching.

Hewlett-Packard Co. does not use its tungsten for gates, nor does NEC use its molybdenum for that purpose. Thus they get around the mobile-ion problem.

Whether metals or their silicides will win out for the future of VLSI MOS circuits remains uncertain. Perhaps silicides are a temporary measure until dry etching and all-low-temperature processing become a reality. However, Bell's Lepselter votes for the silicides, even in the long run. Silicon gates, with or without an added silicide layer, are marvelous from a reliability point of view, he says, "and we don't want to fool with that." □

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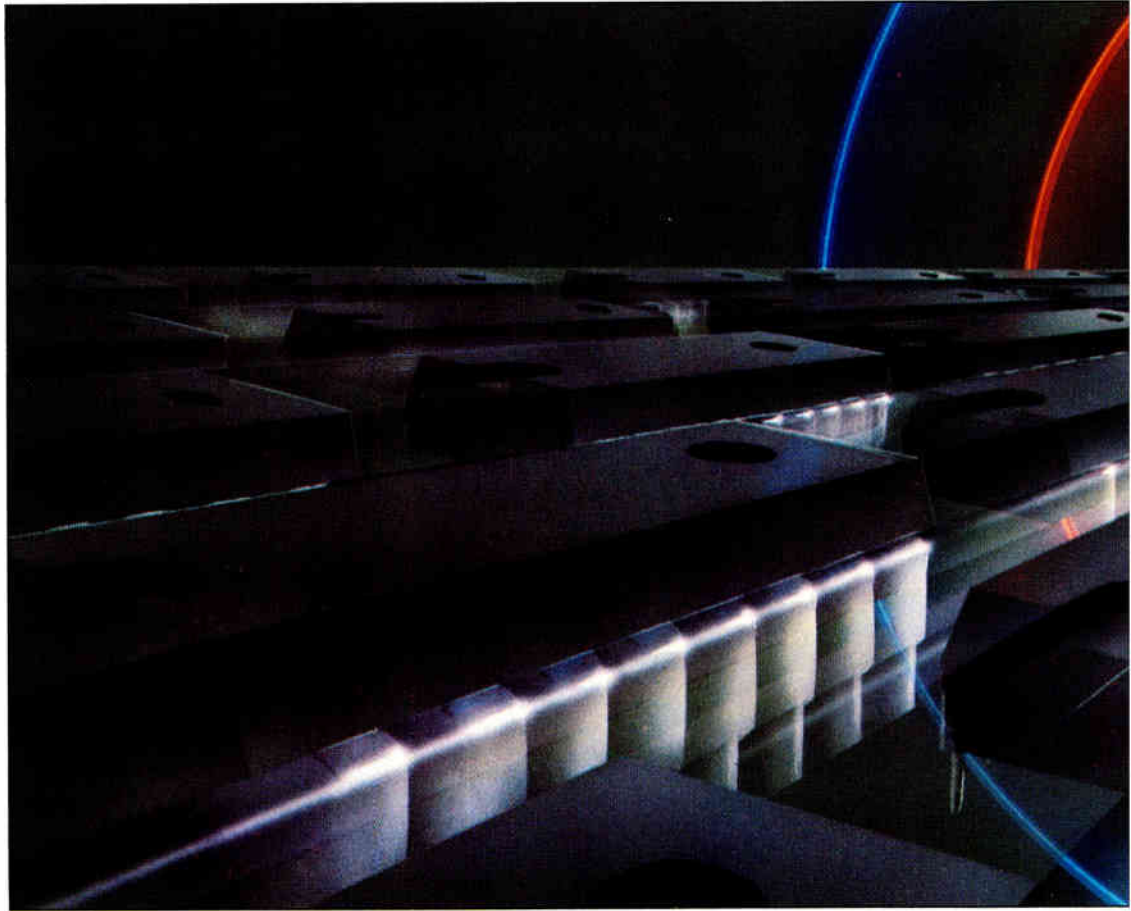
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Office automation

HP: a dive into office automation

All of 27 new hardware, software, and communications products recharge office-market drive and strengthen business-computing line

by Tom Manuel, Computers & Peripherals Editor

With the simultaneous debut last week of 27 new business computer products, Hewlett-Packard Co., the No. 2 minicomputer maker, has revealed a big chunk of its business computer and office automation strategy for the 1980s. The HP Business Computer Group sees the next decade as the frontier of the computer's contributions to productivity in business organizations.

The Palo Alto, Calif., company—in keeping with the current trend of transcending the mere automation of typing—is aiming its new computer systems, software, and communications schemes, as well as its future products, at the full spectrum of a business's professional tasks. "The use of computers by the entire range of operating professionals presents the next great opportunity for computers to multiply business productivity. Our strategy is to place interactive computer power directly into the hands of all office professionals, specialists, and managers, as well as secretaries and the data-processing staff," says John A. Young, president and chief executive officer.

Among the many models the company unveiled are two in the HP 3000 series of business computers: a top performer in the million-instruction-per-second 32-bit class and a low-price model listing for under \$50,000. Other new hardware products are four disk drives storing from

The world's two largest makers of minicomputers, No. 1 Digital Equipment Corp. and No. 2 Hewlett-Packard Co., are announcing important products and strategies in the office automation area. For HP, whose computer business accounts for half its sales, the emphasis is on a new product line including computers, software, and communications equipment. For DEC (see p. 110), the move involves not only equipment but a shift in business philosophy. The action by both giants is easy to understand: according to DEC's own estimates, the office market could conceivably reach as much as \$36 billion annually by 1990.

16 to 403 megabytes and a word-processing station. Significantly boosting the already extensive 3000 software base are a package of four programming tools, a word-processing package for secretaries, a text-processing package for professionals, and the Pascal high-level language, plus the promise for next year of electronic-mail and electronic-filing packages.

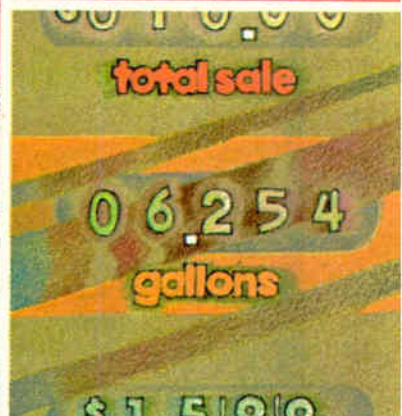
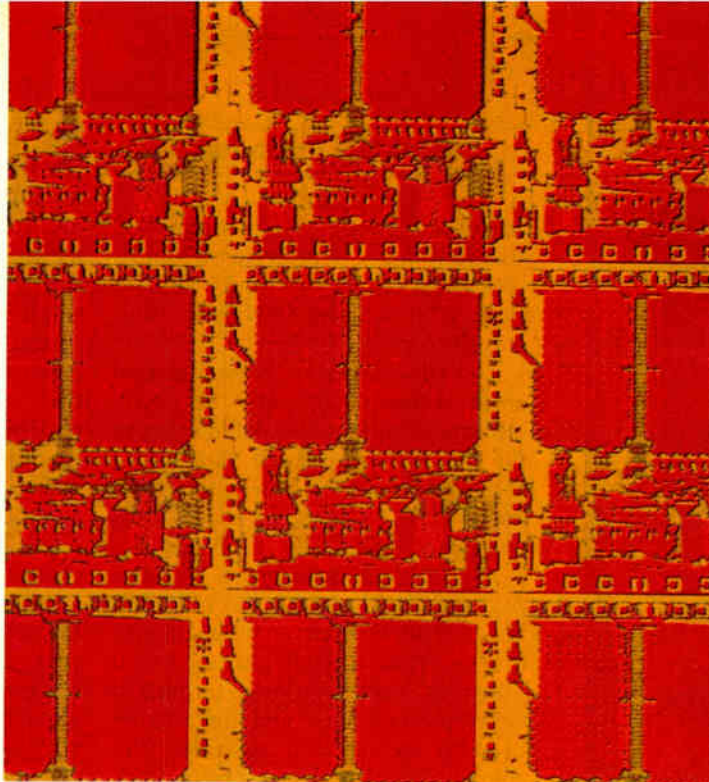
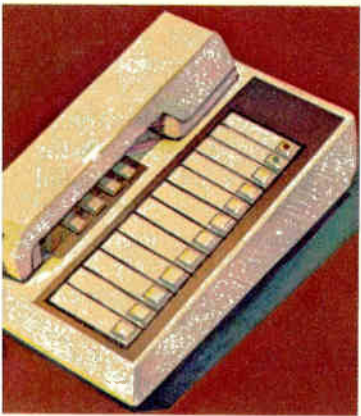
In communications, HP seems to be attempting to cover all bases in an effort to provide its customers with

the wherewithal to connect HP business and office automation systems with the rest of the world. That takes the shape of 3000-series support for the international X.25 packet-switched network standard, the European X.21 digital circuit-switched network standard, and IBM Corp.'s Systems Network Architecture through emulation of an SNA Synchronous-Data-Link-Control-protocol version of the IBM 3270 terminal family. In addition, HP is offering a new terminal controller that supports both the new RS-422 standard and the old RS-232-C one and is also unveiling for the first time an eight-channel fiber-optic multiplexer for local communications.

Getting ready. The company also had the future in mind in two communications policy statements. HP is committing itself to support one of the options likely to be included in the forthcoming Institute of Electri-



Top of the line. Series 64 is the new performance leader in the HP 3000 family. It can handle 1 million instructions per second.



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cal and Electronics Engineers 802 standard for a carrier-sense multiple-access local network with a scheme for collision detection—similar to Ethernet.

The HP concept of the automated office includes not only the newly introduced products. Contributing to the company's renewed thrust into the market are the previously introduced HP 125 personal professional computer [*Electronics*, Aug. 11, p. 85], a decision-support graphics package (DSG/3000), the HP 2680 laser printer, and a letter-quality printer. With all this plus its broad range of work stations, terminals, desktop computers, and links to its factory automation systems, the company thinks it has the right products for the job.

The office automation market is expected to triple to \$36 billion by 1990, according to a market research report released last month by International Resource Development

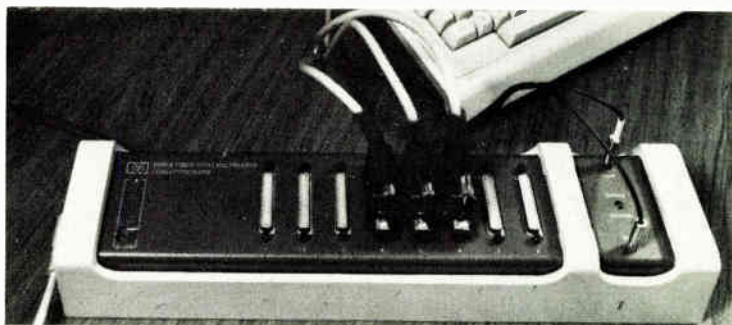
Inc. of Norwalk, Conn. No doubt the major contenders will scramble to dominate the market while the multitude of small firms just entering the new market may have to struggle to stay afloat. But so far, no single company has managed to secure for itself the corner on the business, though it is safe to predict that IBM, AT&T, Xerox, and very possibly Wang and Datapoint will be leading competing vendors.

The two biggest minicomputer companies, DEC and HP, have the background for especially good chances of success. HP is building on a computer business of more than \$1.5 billion growing at nearly 40% a year, and its recent announcements underscore the company's commitment to office automation. The HP 3000 business computer, which is the target system of the recent flood of announcements, "now appears to be in fifth place among the 10 business computer models most widely used in the U. S.," according to Paul C. Ely Jr., HP executive vice president and general manager of the compa-

Optical multiplexer joins line

Users of Hewlett-Packard Co.'s system 3000 computers and other data-generating machines will welcome the 39301A fiber-optic multiplexer if they must control up to eight peripherals within a kilometer from their computer. The unit uses HP39200B fiber-optic cable, which cannot be tapped or interfered with. The full-duplex product provides eight RS-232-C channels, each with an asynchronous data rate of up to 19.2 kilobits per second and a bit-error rate of less than 1 in 10^9 bits. Each channel can operate with any asynchronous protocol without multiplexer adjustments. Diagnostics designed to ensure reliability are provided by loopback switch and fiber-optic loopback cable that together allow failure locations to be isolated. Any asynchronous peripheral may be hooked into the local communication network, which two or more 39301s can provide. To perform its time-domain multiplexing chores the fully user-transparent 39301A samples each input channel at a 300-kilohertz rate and serializes the resultant 7-megahertz composite-rate data channel for transmission.

-Harvey J. Hindin





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ny's various computer groups.

The new 3000 series models are completely software-compatible with the previous models. Also, HP customers can upgrade the processors of their older models by exchanging them for the new series 40 processor. The new price leader of the 3000 line, the HP 3000 series 40SX computer system, has a U. S. list price of \$45,454, which includes 256-K bytes of main memory, a 27-megabyte

disk drive with a built-in cartridge-tape drive, a system console, and four synchronous terminal ports. It costs 33% less than the series 30 it supersedes, though it is two and a half times as powerful.

Topping off the HP 3000 line is the new series 64 system, a processor that can handle 1 million instructions per second and has several 32-bit functions. The 64 has a memory 32 bits wide implemented with 150-nanosecond, 64-K random-access-memory chips on 1-megabyte memory boards. Maximum memory is 8

megabytes. Data flows on a 32-bit data bus and is manipulated by a dual 16-bit arithmetic and logic unit that can perform 32-bit arithmetic in one cycle, a big step toward a full 32-bit processor architecture, which HP will undoubtedly offer.

Also contributing to the throughput performance is a 75-ns 8-K-byte cache memory. The previous top-of-the-line unit, the HP 3000 series 44, introduced last December, is enhanced with the new 64-K RAMs and a new lower price and now becomes the midline model. □

DEC: new target, new approach

Special sales personnel, TV commercials, and a pitch aimed at executives mark thrust into vertical market

by James B. Brinton, Boston bureau manager

Digital Equipment Corp. is moving into vertical markets—and with an uncharacteristic panache. Consider the way the Maynard, Mass., firm announced its thrust into office automation: a satellite-relayed nationwide teleconference on Oct. 29 with the press, its customers, and its own employees. Earlier in the month, the company began training the first of several hundred special sales personnel to master the ins and outs of office automation.

What's more, DEC will unveil exhibits at seven office-oriented trade shows in the next eight months and to further increase its profile, will air its first television commercials this month. The company may even consider using an uncharacteristically high level of executive sell on its prime Fortune 500 prospects.

The reason behind this extraordinary flamboyance, and for a move that will bring the firm into at least partial competition with its original-equipment-manufacturer customer base, is market size. DEC's own estimates put the data-processing and networking sectors of the automated-office market at about \$9 billion per year by mid-decade. And this may be conservative—some estimates already show office automation as a \$12-billion-per-year market

and project as much as \$36 billion annually by 1990.

Although the office push will be supported by a number of new products, much if not most of the hardware DEC will pitch to its new end-user customers already is on the shelf. In the past, many of these products might have been routed to DEC's OEM customer base, which has been one of its market mainstays over the last 20 years.

Traditionally, DEC computer systems sales have been aimed at high-technology end users, typically engineering, scientific, and educational concerns. Its other key support area has been the so-called iron-market system OEMs that incorporate DEC products into their own. Now it will compete, if only marginally, with its own OEMs.

But competition is in the eye of the beholder, and DEC does not see

TI widens office computer line

In a move to extend both the medium and high ends of its DS990 computer family, Texas Instruments Inc. is introducing five new models, including TI's first multiuser system featuring Winchester disk drive technology. The expansion, coupled with the recent announcement of the Business System 200 line of single-user desktop computers, is part of a scheme to broaden TI's minicomputer offerings, increase market share, and boost visibility.

TI's Digital Systems Group in Austin, Texas, has created a new high end for its DS990 family with the introduction of model 36, which sells for \$86,500 in single quantities. It has a removable-disk-pack storage device, DS300, which has 241.2 megabytes of formatted data storage. The high-end minicomputer can store over a gigabyte of on-line data. The new models 16 and 26 also offer high-speed, random-access disk-pack devices with mass storage and cost \$50,000 and \$70,000, respectively.

With the addition of models 3W and 5, TI adds its own Winchester disk system to the DS990 line. The 3W, which is similar to the existing model 3, features a 5¼-inch Winchester subsystem and is priced at \$16,500. The model 5 uses TI's new 8-in. Winchester drive, which is now being used only internally by TI. The model 5 sells for \$28,950. Shipments of models 16, 26, and 36 are slated for December, while shipments of models 5 and 3W are scheduled to begin in April and May 1982, respectively. **-J. Robert Lineback**

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its office-automation efforts hurting the OEMs. The company expects market growth to support its invasion while leaving more than enough territory for the manufacturers. One company source also notes that "our entire office product line will be available to our OEMs, not just end users, and the OEMs will continue to be able to sell into their traditional markets. The difference to them will be small change; the people we are really competing with are IBM, Wang, and the like."

DEC will support its move with a raft of hardware and software, much of it either new or recently introduced. In fact, according to one company spokesman, "we have been announcing products for the past year or so with office automation in mind, but one at a time and slowly so as to attract minimal attention from competitors."

Fully armed. Thus does DEC arrive with full-blown capability. In addition to its traditional lines of 12-, 16-, and 32-bit computers, it currently offers its new DECmate "work processor," the WS78 and WS278 desktop computer systems, and a wide line of other equipment—for example, peripherals and its just-announced VT18X personal-computer option for the VT100 terminal that is compatible with CP/M (see also p. 58).

DEC's software offerings include word processing (DECword), combined word and data processing (DECword DP), and a terminal-oriented automatic typesetting package (DECset). Also—especially important as 32-bit computation gains strength in the minicomputer business—there are information storage, organization, retrieval, display, and reporting (through VIA, the VAX information architecture using Data-trieve, a "fourth-generation, nonprocedural" language designed for this application). Finally, an electronic mail system with editing capabilities (DECmail) based on the firm's successful DECnet III local networking system is included.

According to David R. Fernald, DEC's Commercial Group marketing director, a key competitive edge will

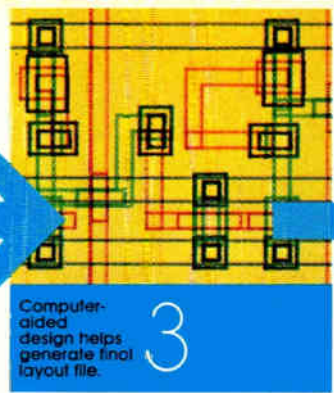
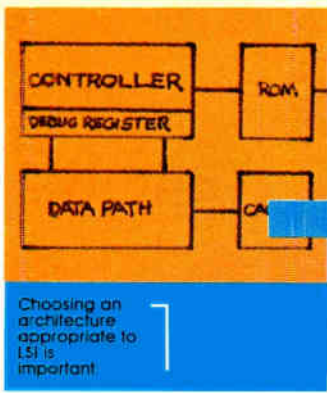
be the company's ability to bring all its office-automation capabilities to the user's fingertips at a single terminal. He says this is not possible now with systems from IBM and Wang. DEC, however, soon will make its whole arsenal of word-, text-, mail-, and data-processing systems accessible from, typically, a model VT125(W). Not only does this give any member of an automated office group access to the full power of the system, but it also leverages the cost of terminal equipment, a factor that should appeal to customers in search of discounts.

Keeping it simple. The single-terminal approach characterizes DEC's market orientation—its new hardware and software offerings will form an umbrella over existing capabilities, allowing the company to make more orderly market penetration and allowing users to service their needs through a single vendor.

Thus, DEC is in the "complete solutions" business, says Fernald; he feels that is appropriate. "We probably have as much internal experience in this area as anyone. DEC put its first in-house electronic mail system into operation in 1978, and we were trying to engineer together earlier than that. Originally a 40-user system, it has now grown to a community of 3,500 worldwide served by seven major computer nodes."

In addition, DEC's recent entry into manufacturing management and control also strengthens its position. Based on the VAX architecture, its manufacturing management and control systems consist of inventory control, manufacturing standards, purchasing, material requirements planning, and shop-floor control software. According to Commercial Group vice president Roger C. Cady, the company's eventual goal is a complete computer-aided manufacturing capability, with some software and systems integration remaining the responsibility of OEMs.

Manufacturing management, also announced in October, meshes so neatly with the office-automation effort that the two should act to reinforce each other, in the opinion of the company's executives, putting DEC in contention for a top-10 position in the industrial-office-automation market of the coming decade. □



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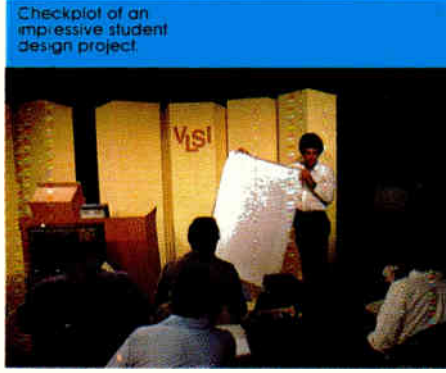
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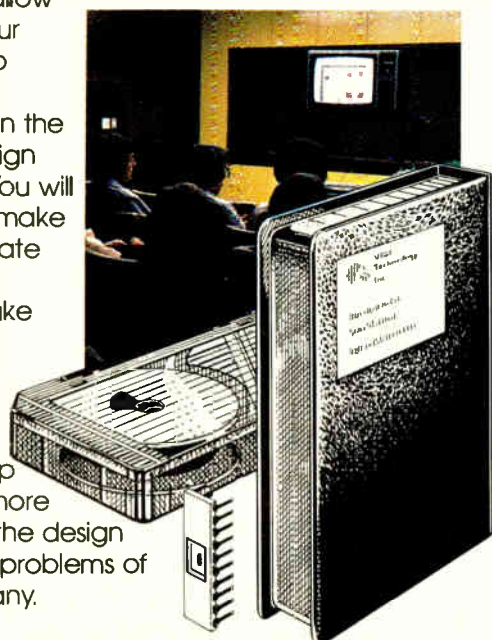
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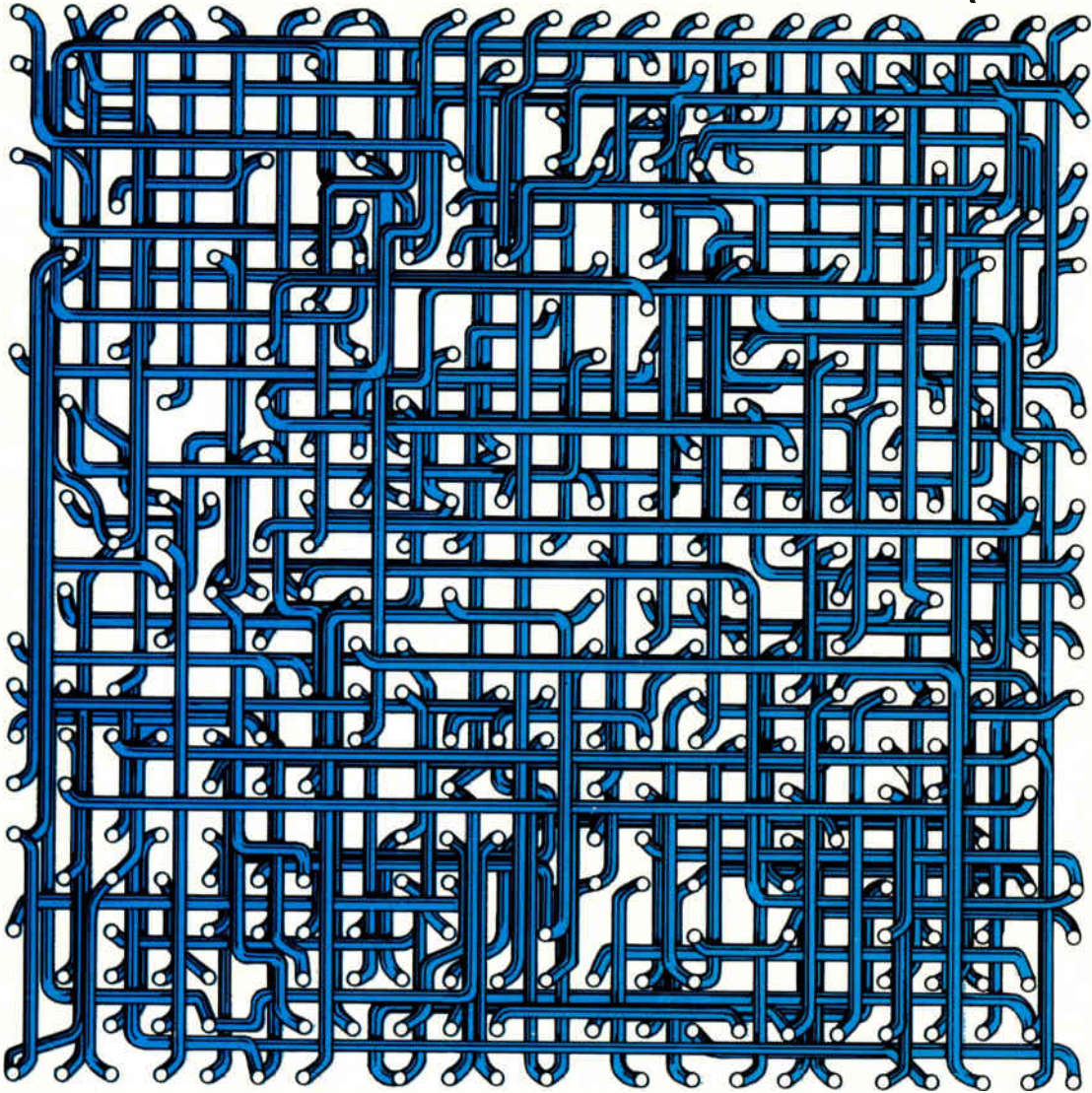


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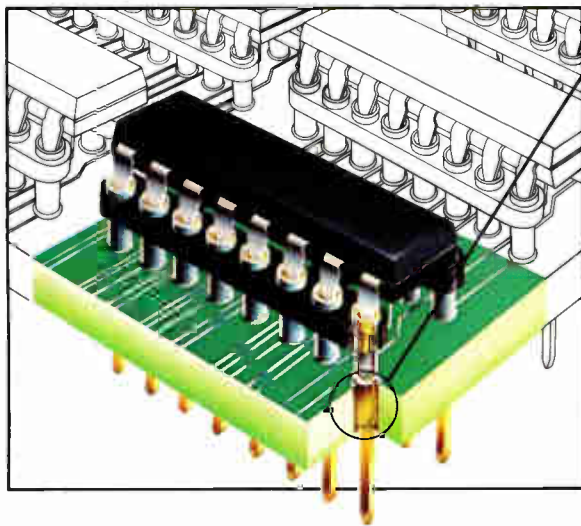
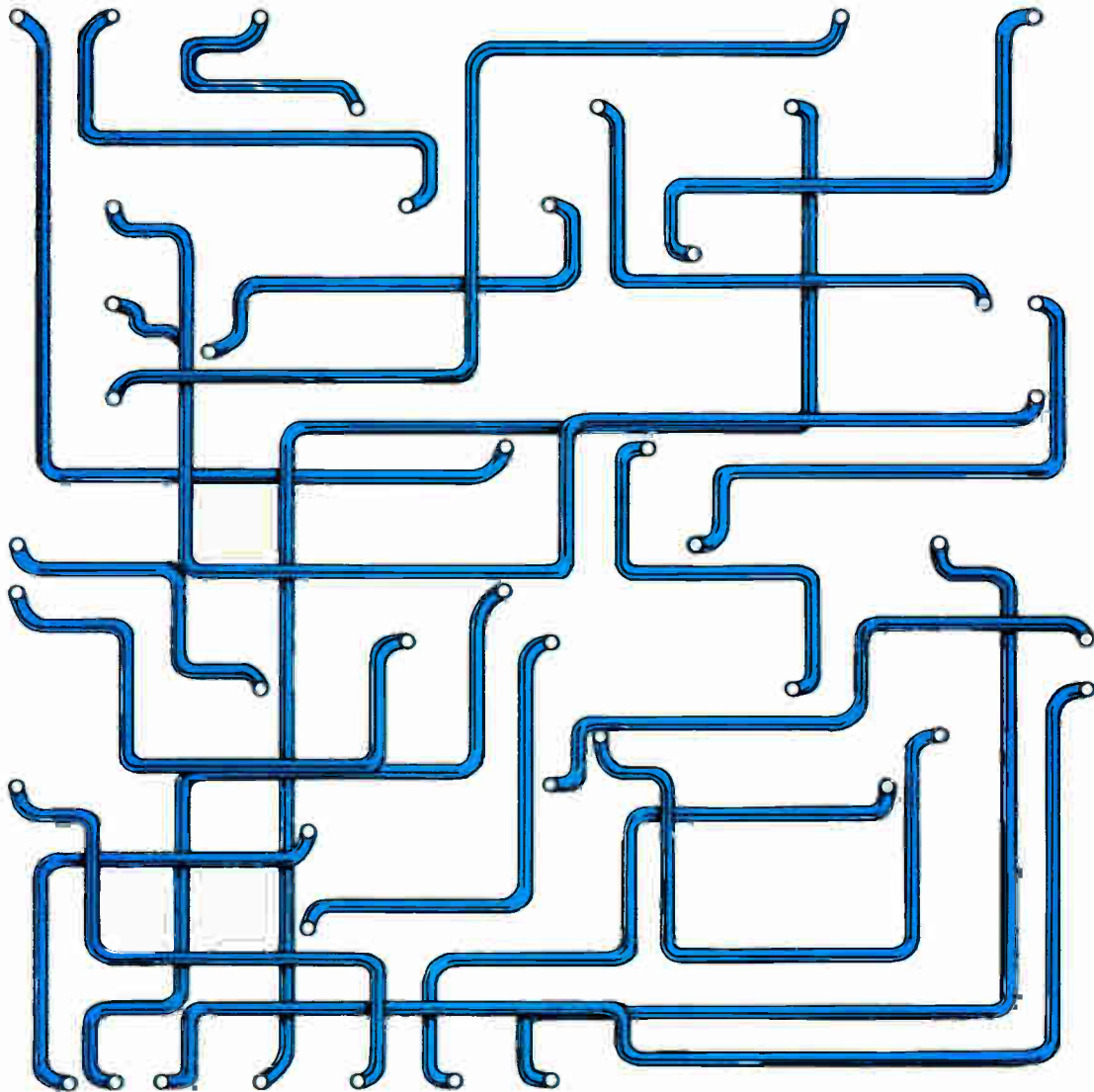
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You have mail.
```

```
%mail
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```
From doug, Thurs Aug 27 11:07:35 1981
```

```
Please reschedule our 3:30 meeting to 8 am tomorrow  
thanks, doug
```

```
?q
```

```
%ls
```

```
bin      lpr      mch.o    newobj    mail.c  
bench    uucp     plz      test.c    memo.report
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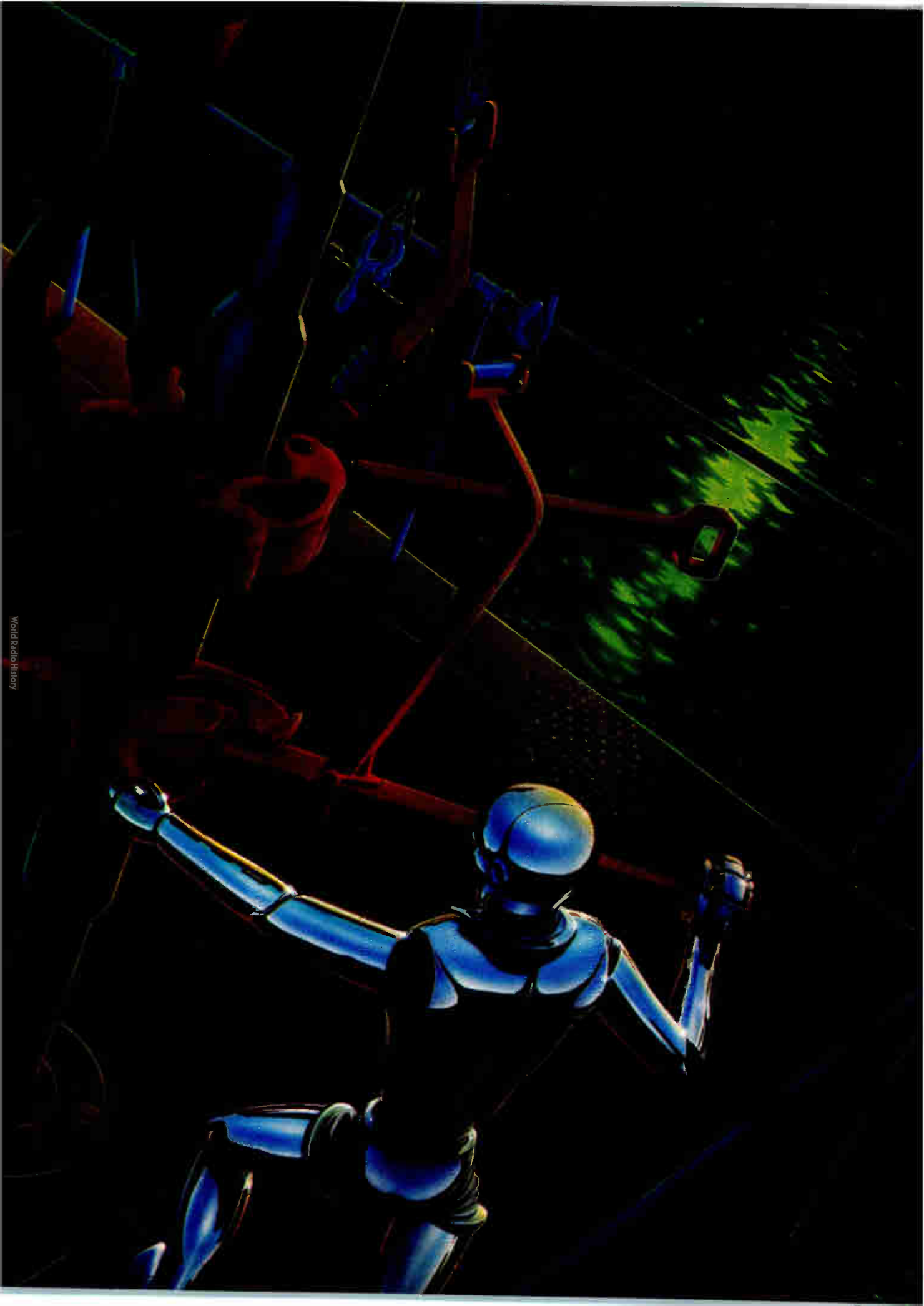
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Tester takes on VLSI with 264-K vectors behind its pins

Combining both high-speed static and denser dynamic RAMs, the 40-MHz system will also serve in computer-aided design networks

by Garry C. Gillette, *Teradyne Inc., Semiconductor Test Division, Woodland Hills, Calif.*

□ The advent of very large-scale integration has given rise to a set of resource problems in testing that, unless solved, could ultimately limit the economies of increased VLSI production capacity. These problems include the increasing number of dollars and test floor space needed for test equipment, as well as the exponentially growing cost of test-program development.

In general, the rise in the cost of testers has been due to the larger pin counts and higher speed of the chips that the testers must check. The rise in the amount of floor space needed can be attributed to the decrease in throughput rate as testers become bogged down by the large test-vector lengths needed for devices. The chips take longer to test, and thus more testers have been needed to keep parts flowing out the door.

As for developing test programs, extending the present manual and semiautomatic program generation techniques for VLSI would result in test-program generation times measured in person-years. Because of device complexity, programs generated using these techniques would provide unknown or low fault coverage. In addition, programs generated by the chip user would run the risk of being uncorrelatable with the test programs created and used by the manufacturer.

The J941 VLSI test system shown in Fig. 1 was designed as a solution to these testing efficiency problems. Using new pattern generation techniques, it minimizes both test and test-generation times for today's parts. In addition, its architecture permits the system to be linked to computer-aided design systems for automated test-program generation.

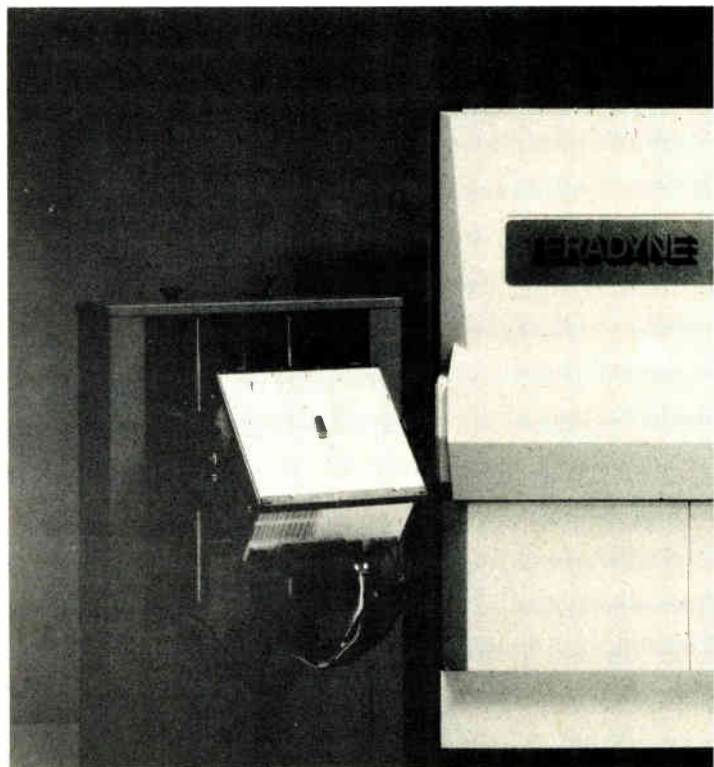
Saving time

One of the most direct ways a VLSI tester can reduce program development time is to simply free programmers from having to deal with the quirks of its pattern generator. This can be done by putting enough pattern memory space behind each pin to directly execute a test pattern without having to pause and fetch patterns from

1. Vector vector. The J941 general-purpose VLSI test system seen at right can store more vectors behind its maximum of 96 pins than earlier generations of test systems. It can be configured as shown for a single test station or supply vectors to two stations.

another storage medium during testing. Generating vectors for VLSI testing is complicated enough without having to additionally go through an unnatural process of "shoe horning" the program into multiple 4-k loads of pattern generator memory.

While a device is in the test socket, test time is consumed in two areas—dynamic functional testing and dc parametric testing. By far the greatest percentage of LSI and VLSI test time is taken up by functional testing, and a test time overhead problem has arisen as today's more complex devices require many pattern reloads. VLSI devices can easily require over 100,000 different test vectors, and the sequencing of these may require them to be used in multiple loops or in local repetition. Taking some projected growth into account, VLSI tests will be containing over 1 million different vectors within the next five years.



To increase the functionality of VLSI devices while keeping pin counts from growing astronomically, designers are increasing the device cycle rate and number of multiplexed input/output pins. Thus, with multiplexing, the number of vector state bits crossing the pins of a device under test is increasing, and so is the frequency at which they occur. The product of the state vector rate required to test a device and equivalent number of bits per vector yields a measure of these increases (Fig. 2).

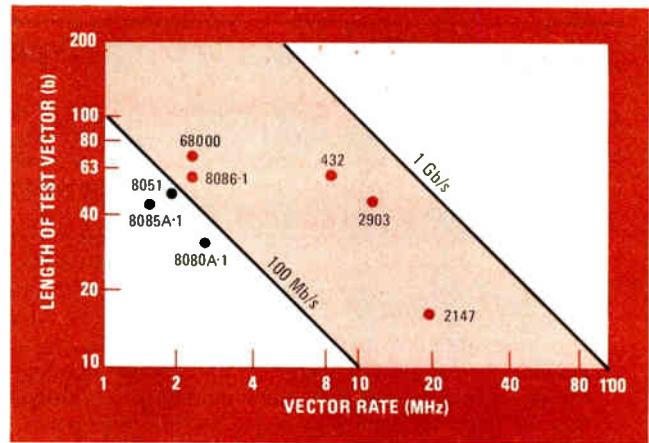
If reloading is required during the device test, most of the state vector bits must be funneled through a tester bus with the capability of handling from 1 to 100 million bits/second. This reloading causes the efficiency of the tester for the dynamic part of the test to range from 2% to 50% today and possibly 0.2% to 5% in five years.

To avoid a severe time penalty for the dynamic testing, an increasing number of vectors must be stored in the test system both to avoid bottlenecks on the data bus and to make vectors available at the rate required by the device under test. When these criteria are satisfied, dynamic test times tend to remain constant, even with the increase in functionality.

Saving overhead

For example, 100,000 vectors at 10 megahertz take 10 milliseconds, and thus, a complete multicornered test may require only a few tens of milliseconds. That, however, is an order of magnitude faster than current test times, which currently require pattern reloads. Thus, while the problem of minimizing dynamic functional test time is complex, the solution is conceptually straightforward: for a given test program, execute the desired vectors in a single pass with no overhead from the tester's pattern generator.

Overhead—or time lost while reloading memories and



2. Faster and wider. The test-bit/second rate, shown as solid black lines in the graph above, is a product of the number of bits per vector needed to test a device and the speed with which vectors must be delivered. VLSI devices will soon pass the 1-gigabit/s level.

resetting digital-to-analog converters and control registers—not only retards throughput in production testing, but also necessitates refreshing the device under test. Since most LSI devices can hold information only for a limited time, the device under test must be continually clocked to retain data during the overhead or reloading pauses. Also, lost cycles cause programming difficulty and introduce a new variable into the testing process due to the device's unpredictable thermal and electrical response during pauses.

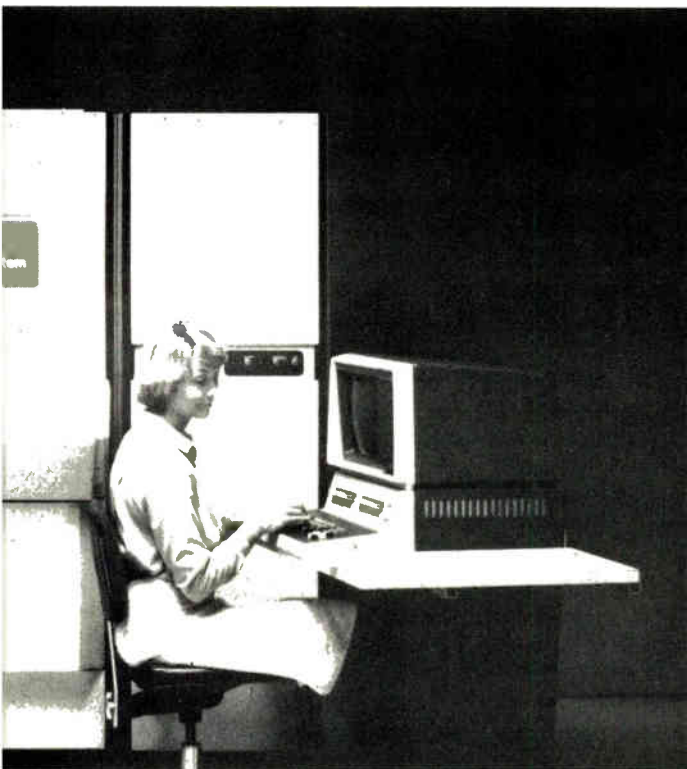
Thus, pauses in vector bursts caused by moving pattern data from a local buffer to the tester over a data bus can mean less accurate testing. Vector bursts with dead cycles and pauses do not necessarily constitute the same test as a continuous stream of vectors.

Heretofore, VLSI testers have incurred overhead cycles primarily because they have been limited by the high cost of supplying sufficient pattern storage capacity. Most pattern generators contribute no overhead until the traditional 4,096 locations of stored program memory overflow—and with current VLSI devices, that happens quickly. For a test with 100,000 vectors, this means reloading 24 times; future tests could require as many as 250 reloads.

Interleaved memory

The J941 test system increases the number of test vectors that can be stored in random-access memory, so that the entire functional pattern for a VLSI device can reside in the system's pattern generator and recalled at once, without overhead, at the rate of the device test. The large number of clock-rate bits behind each pin of the device under test are supplied by combining the fastest 4-K static memories, 10470s and 2147Hs, with interleaved dynamic memories. At about the same package price and size, the latter have 16 times the density and one fourth the power of the former. In effect the interleaved memories operate as a static test-rate memory requiring no refresh cycles. (See "Dynamically backed pins keep test vectors flowing," p. 124.)

The interleaved-memory approach is made possible by a new pattern generator architecture. Today, it can



Dynamically backed pins keep test vectors flowing

The pattern generator of the J941 can now supply 264-K vectors to a device under test without having to be reloaded. And though this is extremely large compared with most current systems, further increases are planned as very large-scale integration matures.

This vector generation capability was achieved by using a memory-intensive design that combines the performance of the fastest static random-access memories with the larger storage capacity of less costly dynamic RAMs. The memories are used in an interleaved fashion in a manner similar to that seen in the cache memory of mainframe computers. One advantage of this approach is that the depth of pattern generated is thus limited only by the storage capabilities of the next generation of dynamic RAMs, a property already exploited to increase memory capacity from 72-K to 264-K during the design phase.

The pattern generator's operation can be understood with the aid of the figure below. During each test cycle, the pattern sequence controller sends four addresses to the channel data buffers' four memory locations—the source-select memory and the X, Y, and Z memories.

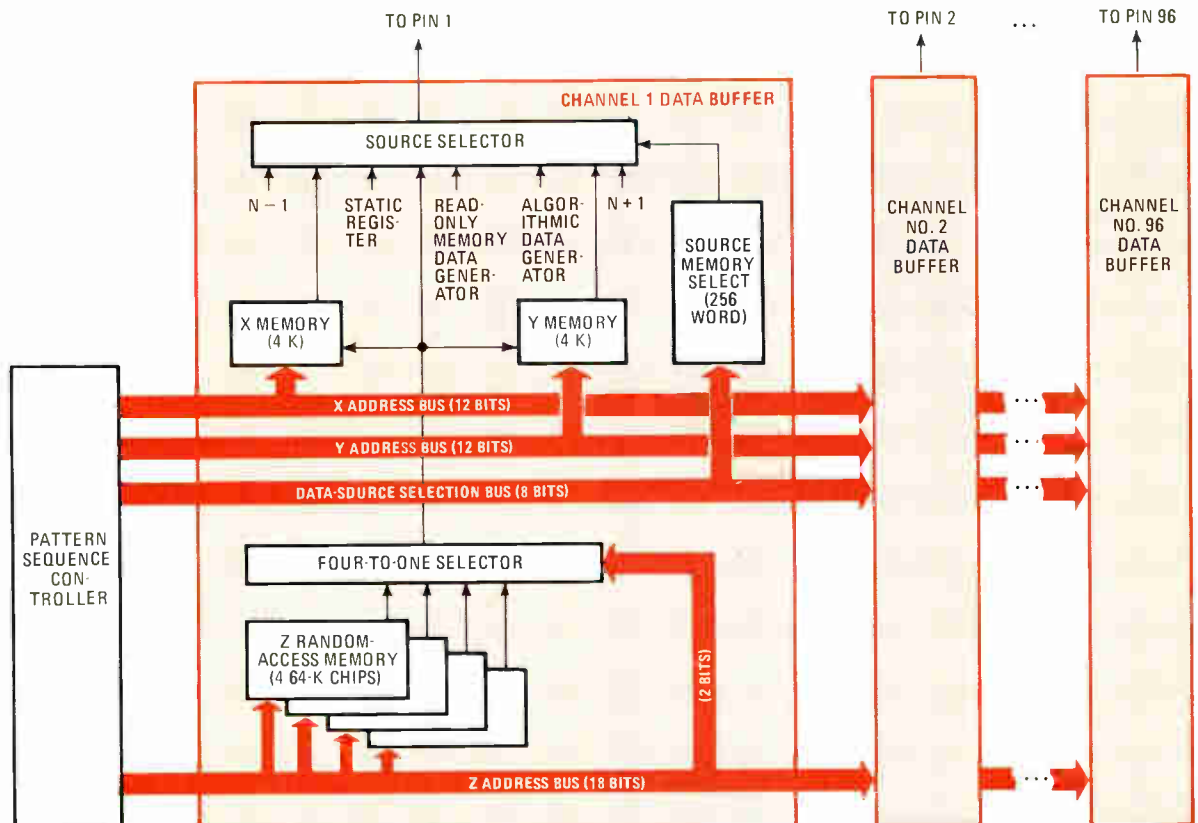
The source-select memory can choose pattern data from any of eight sources, although sequential data is typically provided through a selection of either the X or Y memory. The unselected X or Y memory can be reloaded asynchronously and transparent to the test being run by the Z memory in under 200 microseconds—less time than it takes to sequentially scan the selected X or Y memory. This interval also guarantees time for refreshing the Z RAM, since, when it is not in use, the Z address bus is

interrupted by a refresh counter to give continuous access to each cell in the Z memory. Hardware parity checking at clock rate controls soft errors at the test head.

Thus, for sequential patterns, continuous 4-K blocks of vectors are available at the device test rate. Further, using the source-select memory, test data can be obtained by shifting through data from channel (N + 1) or (N - 1), permitting serial scan path patterns to be generated without dead cycles. Other alternatives for data sources are data derived from the device addresses for testing programmable read-only memory and RAM and data from the Z memory, which can be used synchronously as an independent third field when not reloading the X or Y memory.

Other pattern configurations use the X and Y source fields in address mapping (descrambling) for RAM testing. Here, testing performance is limited in speed only by the static memory and the ability of the pattern sequence controller to provide a common address to all 96 pattern data buffers. The J941's performance was conservatively rated at 20 megahertz to permit the use of available emitter-coupled logic and a common backplane for the whole system. The address to the 16-pin 64-K dynamic memories, which are connected in what is termed a nibble-mode configuration, is presented at a slower 5 MHz to keep in step with the faster static RAMs.

In the near future, through such design factors as scaling theory and refractory metal lines, the 256-K dynamic memory will be even faster. When VLSI devices require 1,024-K vectors from the Z memory, an upgrading of the system will be feasible.



provide up to 264-K of pattern storage behind each pin of the device under test, and as dynamic-RAM technology improves, it can readily evolve to over 1 million bits behind each pin. In addition, all other digitally controlled functions in the test system—including the digital-to-analog converters—are memory-based, permitting libraries of program control values to be resident before a test is started.

This architecture results in minimum traffic over the test system data bus while a device is being tested and thus maximizes test efficiency, with dramatic reductions in test time for current and future VLSI designs. Since test times could be short relative to the index time of a device handler, provision has been made for test-head multiplexing and parallel test-head configurations. Current versions have 96 common I/O pins operating at 20 MHz, with 40-MHz operation made possible by multiplexing pairs of channels to each of 48 pins.

Gearing up for CAD

In addition to affecting the physical size of patterns needed, VLSI with its reliance on computer-aided design will affect the way in which test patterns are generated. At present, the industry is in the throes of conversion to CAD, and thus, there is a very wide range of program generation environments to which a test system must be able to adapt, from those that use hand-generated, highly compressed patterns to those that use CAD simulation or hardware emulation to obtain output vectors, with input vectors being derived by cross-assembling native-language programs of the device under test. Ultimately, software programs such as Lasar will automatically generate both output and input vectors for devices included in the model library.

These environments all require program-generating, -loading, -editing, and -debugging resources, yet vary significantly in cost and complexity. For example, the Lasar program runs on Digital Equipment Corp.'s VAX-11 32-bit minicomputer under the VMS operating system with a large disk memory—a hardware configuration whose price is significant. Yet some production environments require only a minimum system configuration, for slight editing of programs written elsewhere. An original source program may not even be available in some production areas, with distribution of object-level tapes being used to control revisions.

A flexible solution to this wide range of software and computer hardware requirements was achieved by extending the techniques used with computing controllers to that of a minicomputer operating system. Commercial minicomputers running standard multitasking operating systems are inefficient when used for critical real-time control of a test system, because of problems with peripherals, limited memory-page size, timing uncertainty in getting the attention of the operating system, and hardware development cost in customizing bus and interfaces to unique tester requirements.

Over many years, an efficient combination of in-house software and hardware tools has been evolved at Tera-dyne to solve this problem. So-called job-level language programs are interpreted on a controller by a master operating program (MOP) and protect the system as well

as automatically analyze test results. The system controller itself has 256-K 18-bit words of directly addressable memory, and the J941 adds a 35-megabyte Winchester-technology disk, since VLSI programs can easily exceed controller memory. This stand-alone capability can then optionally be networked to a Unibus on a high-speed Teranet link, as shown in Fig. 3, allowing access to either PDP-11 or VAX-11 minicomputers for sharing more general-purpose resources.

The software bridge across these environments is a compiler based on the Pascal language and optimized for VLSI logic testing. Called Pascal-T, the compiler runs on the J941's M963 controller and on the RSX-11X (PDP-11) and VMS (VAX-11) operating systems. This permits transportability across a wide range of configurations.

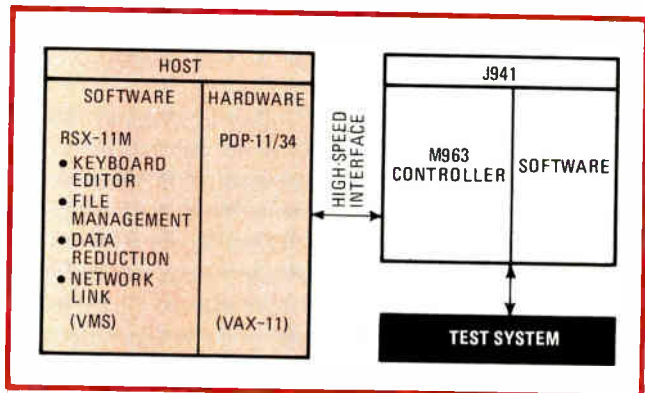
The compiler generates an intermediate code that can be directly interpreted by the MOP. An intermediate code permits elaborate trace modes to be used in debugging programs, as well as running the Pascal-T compiler on the tester controller in a stand-alone configuration. Thus, although widely varying system and computer configurations may exist in a single facility, programmers will need only to learn the Pascal-T language for test and utility program generation, debugging, and maintenance.

Transportable upgrade

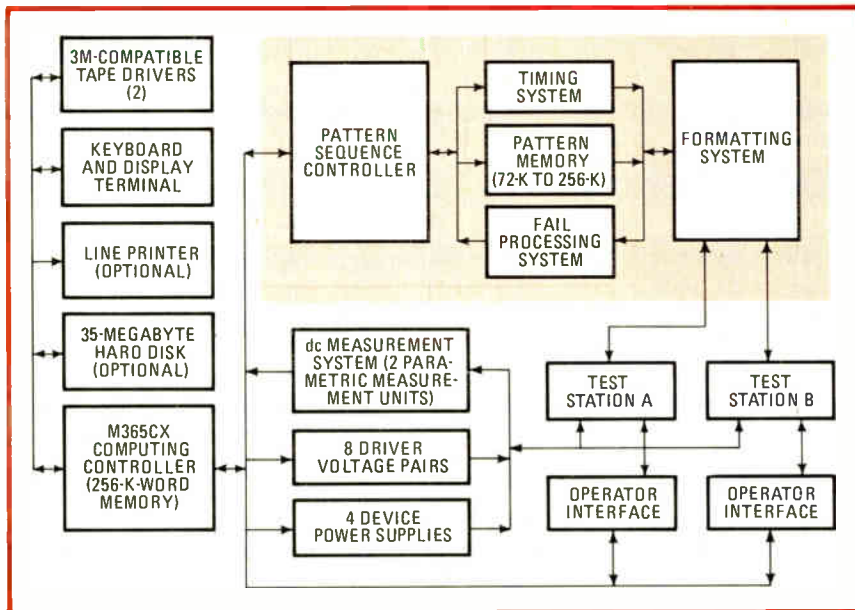
Any improvements or upgrades in the operating system, pattern utility debugging programs, file systems, and editors are transportable to all levels through use of the network link and a common language. For programmers desiring to access hardware directly, Pascal-T permits assembly-level code to be employed at any point in a program, and provides high-level statements that generate directly executable code if no interpretation or indirect (run-time) variable references are implied.

Other features include extensive bit and string manipulation (which can be used to operate directly on a single pin or groups of pins), the ability to refer to variables in any base (hexadecimal, octal, binary, etc.) without conversion, and provision for readily generating inputs from a software simulator operating on a program written in the native assembly language of the device under test.

If a known good device exists, outputs can then be



3. Net growth. Allowances have been made in the design of the J941's hardware and software to permit its incorporation into the computer-aided design system through networking to a host. The high-speed link shown is the Teranet 1-Mb/s data path to Unibus.



4. Architectural planning. Designed for modular growth, the tester's various functional elements can be expanded as the need arises. The pattern memory within the functional test area, for example, can be augmented with algorithmic and read-only-memory data generators.

captured for each pin by a 256-word clock-rate fail-sequence memory for analysis or program development. Ultimately, for better fault coverage and faster program generation, output states will be delivered automatically by simulation using computer-aided-design files. Thus, for design, product engineering, and production environments, new powerful hardware and software pattern-generation tools promise to help control testing time, turnaround time, and critical programmer resources.

Pins by the slice

In addition to patterning, architectural versatility and high-performance instrumentation also contribute to reductions in test and programming time in a VLSI test system. Since a family of test systems would be required to meet the even more complex VLSI testing needs of the future, the J941 was designed for modularity and in a channel, or pin-slice, configuration.

Architectural and performance improvements evolved from extensive test system experience driven by advances in design and process technology. For example, as devices shrink and become faster, they are more susceptible to driver spikes during the I/O switching of pins. Faster devices mean lower breakdown voltages in parametric testing and the need for the narrow (5 nanosecond) pulse widths to be generated and tested.

Simple precautions, like providing low output impedance and good ground sensing to the device under test, can help avoid time-consuming confusion. Correlation time between design, product engineering, and production of a device can be minimized by using the same high-performance instrumentation in test systems in each area. Elimination of custom load boards and automatic confirmation that the test head, load board, and interface to the device under test are configured, connected, and performing properly can substantially improve system uptime in a facility.

Fast and transparent automatic calibration, without fixtures at the pin of the device under test (even when socketed in a handler) and elimination of manual trim

adjustments throughout the whole system remove a level of uncertainty for the operator. Comprehensive system monitors and diagnostics, which allow problems to be pinpointed quickly and corrected (or under certain circumstances even to be anticipated), can control increasing hardware complexity. Features such as these, which ensure natural, predictable, and reliable behavior in a test system, are mandatory for VLSI testing and were design objectives of the J941.

The stand-alone J941, as seen in Fig. 4, consists of an M963 control group, pattern generator, test station electronics, and formatting, timing, and dc measurement systems. The mainframe in the J941 can support 96 I/O channels and, by multiplexing, two 96-I/O-pin test stations. Either or both of these stations can additionally be replaced by two 48-I/O-pin parallel test heads, for a maximum of four 48-I/O-pin test heads in high-volume production applications.

All together now

The M963 control group consists of an M365CX computing controller, a keyboard and display terminal, dual tape drives, an RS-232-C interface, a 35-megabyte Winchester-technology disk drive, interfaces with a printer and a nine-track tape, and a 1-megabit/second network link. The pattern generator includes a pattern sequence controller, pattern memory, source-select memory, data generators, and the fail processing system. The pattern sequence controller provides common addresses not only to the source-select and X, Y, and Z memories but also to timing and formatting memories. The configuration, pattern data, and timing for each pin is determined in look-up-table fashion on a per-cycle basis by the choices programmed in these memories.

The algorithmic and the read-only-memory data generators make possible memory-testing options. The algorithmic data generator derives the data to be passed into and out of a device from the device address at test time. For ROM, programmable ROM, and erasable PROM testing, the data generator provides a look-up table for

comparing the device output to a known ROM code.

The fail-processing system receives information on device failures from the formatter during functional testing. The failures are then processed and may be directed to the fail sequence memory or to the optional fail map. The fail bits from a memory device are stored in the map using device-based address information from the pattern sequence controller.

The formatting system supplies five independent bits for each pin on a per-cycle basis to configure it as an input, output, or both (I/O). The system also supplies demodulation or modulation formats for this process.

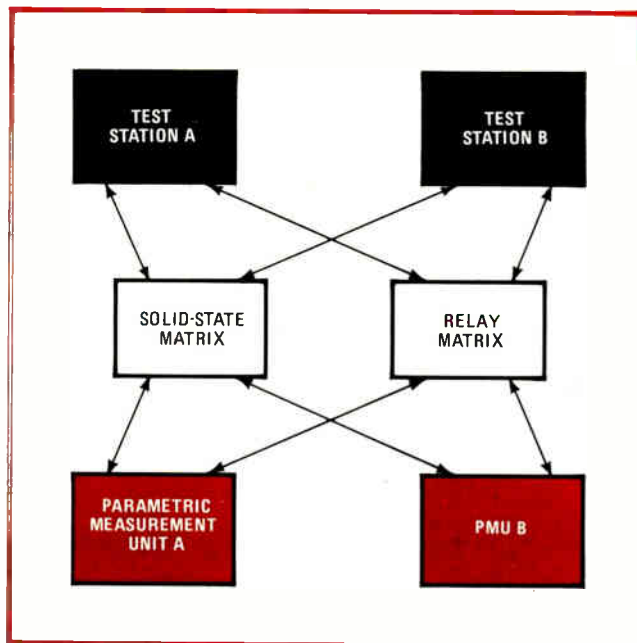
There are 256 look-up-table sets, each containing format sets for 96 channels, programmed by the pattern generator during each test cycle. Driver formats are selected from nonreturn-to-zero, return-one, return-to-zero, and return-to-complement options. Formats for the comparators can be chosen independently; they can be told to expect the pattern bit, the pattern bit's complement, midband (for three-state), or don't care.

Both of these format processes are independently de-skewed and timed by software. Timing is supplied by any one of 16 dual-edge timing pulses, and all transitions can extend past test-cycle boundaries without special programming. There is also independent control and timing of the driver's three-state function, and this may selectively be linked to the software-programmable current load or external resistive load of the device under test for intracycle I/O switching on a per-pin basis. For 40-MHz data rates or the testing of device buses, selected pairs of formatted channels in the mainframe may be multiplexed to corresponding pins in the test head. The multiplex timing configuration of the test system can be completely controlled in every cycle, even at maximum test rate, without restrictions.

The timing system contains 18 timing generators, a period generator, and a timing memory. The timing memory permits 256 independent choices for the control values of all timing functions controlled by the pattern generator on a per-cycle basis. Using the patented Digitime technique, the period generator provides crystal-oscillator-based, time-coherent control with a test-cycle resolution of 100 picoseconds. For all program values, the 18 timing generators also provide 100-ps resolution.

Parametric testing

The dc measurement system consists of two parametric measurement units (PMUs) and two analog conversion units (ACUs). One or more pins can be connected to either of the PMUs by either a relay matrix or a high-speed solid-state multiplexer matrix (Fig. 5). The PMUs can either force a wide range of voltages while measuring the resultant current drawn by the device under test (typically for input tests) or force a similar wide range of current while measuring the resultant voltage (typically for testing device outputs). The J941's minimum resolutions are 1 nanoampere and 1 millivolt, respectively. For measuring differential voltages between selected pins, a resolution of 100 microvolts is provided. The ACUs may be connected to measure many different sources: PMUs, any of the approximately 1,100 system d-a converters, power-supply current monitors, system sensors, system



5. Choice. For parametric tests, J941 gives users various choices using the high-speed solid-state and the high-voltage relay matrices. Each measurement unit can be configured to source voltage or current and to either or both test stations through the matrices.

power supplies, and system precision calibration sources. The ACUs have 16 bits of resolution for use by the internal calibration software, with the 12 most significant bits used for test-program data logging.

The test station electronics can be configured for two stations, with one 96-pin head or two 48-pin heads each, sharing eight device power supplies. Each channel of pin electronics has a 50-ohm backmatched three-state driver amplifier, a wideband high-impedance follower, dynamic constant-current loads (IOH and IOL), and a test-rate load switch for single-pass testing on device buses. By not analyzing signals directly in the test head, channel power has been minimized.

Each channel has three dedicated coaxial lines connecting it to the mainframe: a driver-amplifier input, a driver-amplifier three-state control, and a high-impedance buffer output. There are eight pairs of driver levels, with 2.5-mV resolution selectable for each driver and with the selected pair buffered on each channel to prevent loading when pins become shorted. A special high-voltage channel card for programming E-PROMs has software-controlled rise and fall times.

Eight pairs of load currents, with a 5- μ A resolution and switched by the output of the device under test, can be selected on each channel. The high-impedance follower, with its subnanosecond rise time and excellent level stability, allows remote observation of device pin voltages, even when the test station is mounted on a handler. Independent level comparison on all 96 dual-limit monolithic comparators is done in the mainframe.

Each pin of the device under test can be connected through a 50- Ω coaxial matrix to mainframe electronics for calibration by means of time-domain reflectometry, even with capacitive loading of the device on the 50- Ω backmatch impedance of the drivers. □

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Low-cost 16-bit microprocessor has performance of midrange minicomputer

Designing to pare silicon real estate cuts cost and increases speed of the latest PDP-11 IC implementation

by Raymond Ochester
Digital Equipment Corp., Hudson, Mass.

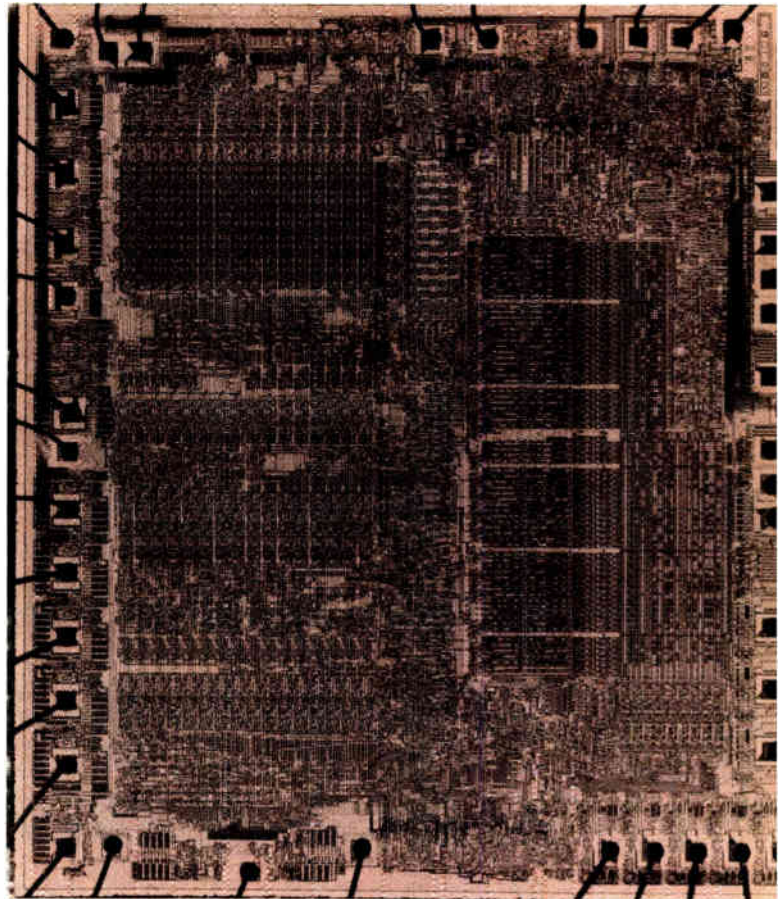
□ Extending the cost-performance benefits of the PDP-11 family into a new realm, the T-11 16-bit microprocessor realizes lower cost than other single-chip processing solutions, yet delivers performance equal to a conventional minicomputer. The new integrated circuit offers the same PDP-11 instruction subset and functionality as lower-end members of the series, yet has a higher execution speed than any of them—about the same as the PDP-11/34 midrange minicomputer.

The architecture and design concepts in the T-11 were influenced primarily by DEC's emphasis on low cost, both for the chip itself and for microcomputer systems and other applications to be built around it. The number of transistors was minimized—there are only 13,000—so that the silicon die size could be small for low unit cost. To accomplish what amounted to a complete redesign, a number of space-saving techniques sparing in their use of transistors were adopted.

The execution speed of the T-11 is 1.6 microseconds for a register-to-register ADD instruction, which is roughly equivalent to that of the PDP-11/34 and twice the speed of the PDP-11/05. The chip operates at a 7.5-megahertz clock frequency with a maximum power consumption of less than 0.8 watt at 25°C. This figure is substantially lower than some other 16-bit n-channel MOS microprocessor designs (1.2 W is given as typical for one; 1.8 W as maximum for another).

The T-11 (Fig. 1) consists of three semiautonomous machines based on programmable logic arrays—the control, data, and bus subunits. The control machine interprets PDP-11 macroinstructions and triggers the next control state. The data machine, which consists mainly of a static register file based on random-access memory and of an arithmetic and logic unit on main and secondary internal buses, computes data-based results. The bus machine handles all input/output flow, including data, address, interrupt, and control signals.

Fabricated in a 5-micrometer process in place of the



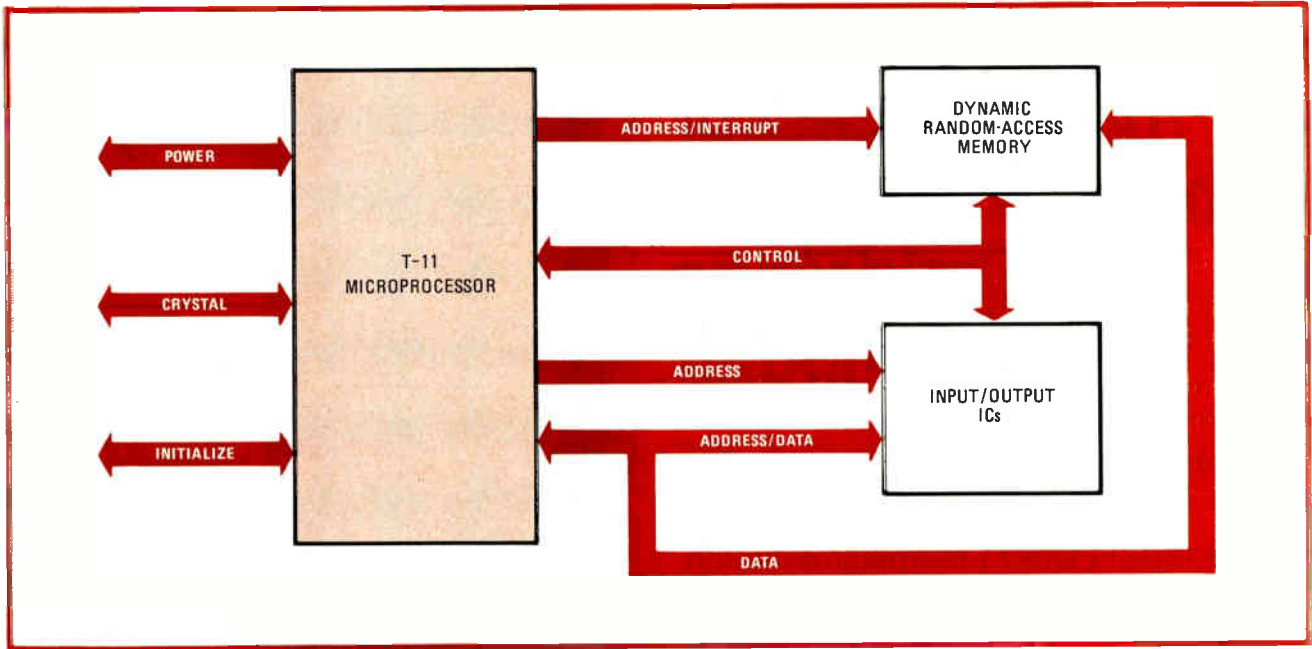
1. Tiny 11. The 5-by-5-mm die of the T-11 contains three somewhat independent data-processing machines—a control machine, a data machine, and a bus machine. The data machine is roughly the upper three quarters of the left side; the control machine is mostly on the right, with the bus machine above and below it.

6- μm process used for the LSI-11/23 two-chip implementation, the T-11 is faster, yet consumes 20% less power. The smaller-scale circuit geometry improves the speed-power product, as well as saving real estate. The higher transconductance and lower capacitance of the smaller transistors tend to increase speed and, potentially at least, reduce power.

Production ease

Production of the new chip uses existing DEC manufacturing equipment and does not require special processing that tends to reduce overall yield or requires further special processing to achieve acceptable yield. Moreover, the 5- μm process is more easily transferred to potential second sources than a finer process would be. Other microprocessor manufacturers have established processes with minimum features as small as 2 μm , but typical device cost is many times higher than what was considered acceptable for the T-11.

In moving to 5- μm geometry, it was necessary to rework layout rules in order to avoid possible merging of elements of the chip structure. If a linear shrink had been used to reduce all elements the same proportion, circuit density could have been increased only about 15% at a given production yield in going from 6 to 5 μm . In



2. Double identity. The T-11 microprocessor in its 40-pin dual in-line package can interface with either an 8- or 16-bit bus. The 8-bit version is shown; in the 16-bit configuration, all the lines at right, except the control lines, become multiplexed address and data lines.

contrast, the density of the T-11 was increased about 30% and achieved the same yield through selective shrinking, a longer and more difficult design process in which various circuit elements are shrunk to the maximum allowed for each element for a given yield.

The new microprocessor was designed to provide greater application flexibility than do single-chip microcomputers and more integrated support functions than bit-slice processors. The trend toward embedded processors places a premium on flexibility in configuring support functions. With such peripheral products as a video display terminal or floppy-disk drive, the processor and its support hardware can match that unit's needs. Use of a microcomputer would mean that the peripherals must be adapted to its characteristics.

Cost-reduction goals

Size and power constraints for the new IC were established initially to insure a product that would be internally cost-competitive. Since manufacturing costs in today's production technology are proportional to silicon area rather than to the number of chips, a die size of 5 by 5 millimeters was selected. The decision to use a plastic dual in-line package rather than the more expensive ceramic packaging set maximum allowable heat dissipation at 0.9 w.

N-MOS semiconductor technology was selected in preference to a complementary-MOS process because of its higher transistor density. The higher power requirements of n-MOS were considered manageable.

Early in the design process, a number of cost-related decisions were made regarding chip and support functions. For example, plans are to use the T-11 with off-the-shelf large-scale integrated I/O chips for such external hardware functions as memory, serial communications lines, and floppy-disk and video-terminal control. Therefore, the processor design included intelligence to

ensure timing compatibility with these support chips.

A single-voltage power supply of +5 volts was chosen with TTL-compatible signal input and output. This selection minimizes the number of power pins in the package, avoids the need for a second external power supply, helps to cut heat generation, and reduces the number of support chips.

The IC has a built-in oscillator clock for use with an external crystal. An external clock would have added substantially to the cost of support hardware, whereas a crystal is comparatively inexpensive.

Program memory was omitted from the T-11; however, the chip includes all the addressing and control signals required by low-cost external dynamic RAMs. The rationale for the first decision was that, with the tendency of program memory to grow rapidly from year to year, the limited chip real estate would require the periodic addition of memory chips anyway. On the other hand, the address- and control-signal configurations would remain constant with foreseeable increases in program-memory size.

Somewhere in time

One approach to help speed up the operation of other microprocessors has been to provide separate external buses for communications with dynamic RAM and I/O devices. However, a single-bus configuration was selected for the T-11 to simplify application and internal system design.

The dynamic RAM and I/O chips each receive control signals from the same pins of the microprocessor by precise positioning of these signals in time. Without time-multiplexed control signals, there would have had to be more pins on the chip package and more support chips, which would increase system costs.

A 40-pin plastic DIP was deemed capable of handling the functions assigned to the chip. A 48-pin package

would have cost more, and production testers for DIPs with more than 40 pins could not be implemented fast enough or cheaply enough.

In order to compete for applications against both 8- and 16-bit microprocessors, the T-11's internal data path is 16 bits wide, and the processor can be operated on an external data bus of either 16 bits for performance or 8 bits for lower cost. The schematic diagram of Fig. 2 shows the T-11 in an 8-bit external bus configuration, with a total of eight pins assigned to the service functions at left and eight for each of the four lines at right. In a 16-bit environment, the only difference is that all address lines become address and data lines.

The bus machine handles all I/O flow of data, address, interrupt, and control signals. The T-11 chip's operating mode is matched to application needs by initializing a unique mode register in the bus machine. For low-cost designs, for example, the mode register is set for an 8-bit external data path and dynamic RAM. For high performance, on the other hand, the designer specifies a 16-bit data path and static RAM.

Geneology of the T-11

In 1973, the PDP-11/05 minicomputer was implemented in TTL technology, and a good deal of microcode was built into the processor. For its control machine, more than 40,000 array sites were provided on 33 densely packed LSI chips. In addition, the gates and registers in the 11/05's data machine were implemented in medium-scale and small-scale integration, with 100 chips providing a total of 5,000 transistors.

In 1979, the LSI-11/23 was designed entirely in LSI technology on two chips in which cost-effective architecture demanded a significant reduction in microcode. By then, cost was evaluated in terms of total silicon area rather than of the number of chips.

Microcode in the 11/05 was converted to implicit functions of the ALU in the 11/23. The ALU in the 5,500-transistor 11/23 data machine can handle every PDP-11 macroinstruction of the two predominant types. The control machine contains 15,700 array sites, about 40% the number found in the 33 chips of the 11/05's control machine.

The T-11 contains 17,000 transistor sites (potential devices) and about 13,000 actual transistors distributed among the three machines: 6,550 in the control machine, 5,450 in the data machine, and 1,000 in the bus machine. The major reductions in transistor count and chip real estate are found in the control machine, where the number of transistor sites was reduced 40%—from 15,700 to 9,400—compared to the 11/23.

The control machine contains four submachines. The instruction submachine computes and retains a new value each time a PDP-11 macroinstruction is fetched. Each time instruction execution enters a new phase (fetch instruction, fetch operand, or execution), the instruction phase submachine computes a new value. The microcycle submachine updates each cycle of the data machine, and the microcycle phase submachine computes a new value for each phase of the microcycle within which the data machine is controlled by strobes (timed commands to registers).

Because one of the prime goals for this design was to minimize the size of the chip, a number of functions were shifted among the submachines. Shifting functions to different parts of a chip can reduce the number and length of interconnections, thereby reducing the area.

The number of sites in the control machine was reduced first in the LSI-11/23 and then further in the T-11 by redistributing data-handling assignments among the four submachines. First, the instruction phase submachine was made more important in the 11/23 by increasing the maximum possible number of instruction phases. While this modification added transistor sites in the instruction phase submachine, it saved far more decoding sites in the microcycle submachine. At the same time, the microcycle submachine was changed over from RAM to programmed logic arrays because Boolean equations could be represented with fewer gates in PLAs than in RAM.

The number of sites was cut even further in the T-11 microprocessor by moving tasks from the microcycle submachine to its phase submachine. Gates are uniformly wide in the microcycle submachine because many tasks require large I/O sections. However, certain tasks that did not need such large I/O sections were transferred to fewer sites in the microcycle phase submachine. Additionally, some tasks were shifted from the microcycle submachine to the data machine, also reducing the number of sites that are required.

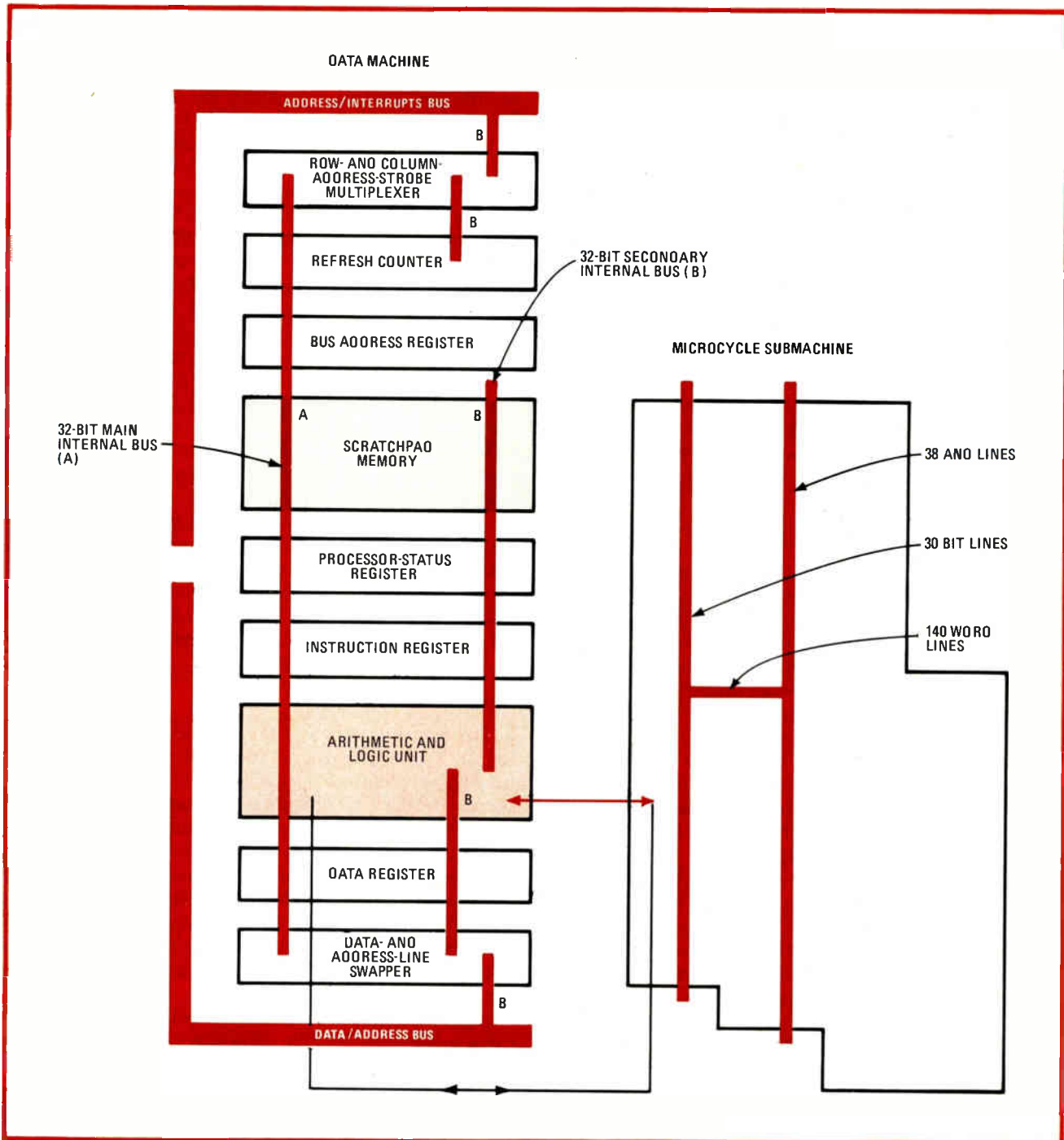
Simpler decoding

The decoding space of the microcycle submachine in the 11/23 must decode all 16 bits of the PDP-11 macroinstruction: 4 bits of operations code and 6 bits each of source and destination address. Depending on the operations code and particular instruction phase, however, only 10 bits are actually needed for the gate output of the operations code and either source or destination address. In the T-11, therefore, the instruction phase machine instead determines the appropriate 10 bits in advance, so that the microcycle submachine need decode only 10 bits. The move eliminated the address space needed for the additional 6 bits.

A branch instruction task was shifted from the microcycle submachine into the data machine, saving both the microword space for representing different branch possibilities and the time needed to select the microword in the control machine. To do this, a branch PLA was put between the 16-bit temporary instruction register at the bottom of the scratchpad memory and the processor status register below it.

Four bits in the branch PLA are compared to the 4 bits of condition code in the processor status register: a match switches the ALU to ADD, and no match switches it to NOP (no-operation). The entire matching function is performed in the data machine, using what would otherwise be open space between registers.

This shift of data-handling tasks out of the microcycle submachine has significantly reduced the total real estate, as well as the number of devices in the microprocessor. The area of the microcycle submachine has been cut nearly in half with only small increases in the smaller areas occupied by other circuit sectors. Also, putting the



3. Machine parts. In the T-11 design, functions were shifted among the machines. For example, the branch-instruction task was moved to the data machine from the microcycle portion of the control machine in the form of a branch PLA. Control lines are shortened wherever possible, such as substituting the colored path for the solid black one for links between the microcycle submachine and the data machine.

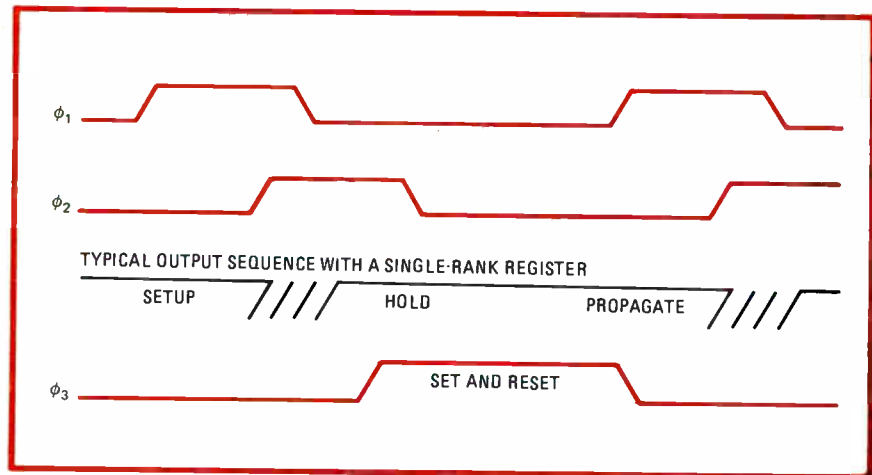
control and data machines on the same IC eliminates about 1,000 transistors needed to interconnect circuits on separate control and data chips.

There are significant differences in the circuitry of the T-11's data machine that have increased its execution speed. Fast paths for the address from the bus address register and data from the scratchpad memory to pass around the ALU to the bus output latch are added without penalty in cost and real estate by timesharing the internal buses extensively. In the data machines of

the earlier low-end PDP-11s, the bus address must be transmitted from the scratchpad through the ALU and back over the main bus to reach the bus address register.

The real estate occupied by the data machine was shrunk by adopting an internal architecture aimed at orderly geometry, which in turn minimizes the length and number of interconnections. In the data machine and microcycle submachine (Fig. 3), all the registers, including 12 in the scratchpad memory, are aligned for convenient multiplexing with the main and secondary

4. Relay race. The microcycle of the T-11 microprocessor has three phases that slightly overlap. The phases ϕ_1 , ϕ_2 , and ϕ_3 are shown in relation to a typical output sequence with a single-rank register. Because of circuit segment stability, each phase starts before the previous one ends.



internal buses that are oriented vertically in the layer above. Similarly, parallel control lines in another layer and perpendicular to the internal buses (but not shown in the figure) cross over the registers and the ALU.

Buses A and B consist of seven lines for each of 16 bits. One of the seven, called the X line, is available for any assigned data transfer. The uniform spacing of the horizontal control lines is such that additional lines can be inserted wherever needed. As a result, the registers and logic for condition codes, branches, priorities, variables, and constants can communicate by means of short links to existing vertical and horizontal metal, thereby avoiding the jogs or angular lines that can handicap high-density circuit designs.

The characteristics of n-MOS technology have contributed to orderly geometry in several ways. Rather than requiring the positioning of transistors and then of the interconnections, n-MOS permits first laying out the mutually perpendicular bus and control lines. The gates are placed below the crossing of the lines, substantially reducing the number of interconnections.

In addition, bidirectional buses can be used in conjunction with multiplexers so that single transfer devices linking registers and buses can handle both reading to and writing from the bus. The B bus links at top and bottom to the time-split external bus are also connected through transfer devices for two-way transmission.

However, the concept of orderly geometry in the data machine was not applied blindly, regardless of other space-saving techniques. Two modifications to the geometry further reduced the number and length of interconnections in this unit.

In the first modification, the carry condition code requires linking the outputs of transistors at bit positions 15, 7, and 0 in the ALU. One way to accomplish this would be to add three long horizontal lines to bring the bit-position signals out to one side of the ALU.

Instead, the bit positions scattered in the lower part of the ALU are connected in step fashion by linking vertical X lines and short line segments inserted between existing control lines. Even though the ALU must be slightly wider to accommodate the 16 extra X lines, the area under these lines is used in other layers of the chip and so space is saved in the ALU's vertical dimension.

In the second modification of orderly geometry, there

are a number of instances in which a position on a vertical bit line in the microcycle submachine must be connected to a horizontal control line in the data machine. Conventional practice would be to insert an interconnecting line down from the bit line out of the congested area and then back up to the control line in the data machine (the solid black line in Fig. 3).

Instead, wherever there are no transistors to the left of the particular bit line, the horizontal control line from the right is stopped at the bit line. Thus space is available to go directly left into the data machine (the colored line in Fig. 3)—a much shorter route than with the conventional method.

Overlapping clock phases

The simplest clocking scheme that operates effectively with the single-rank registers in the T-11 microprocessor is a three-phase microcycle with slightly overlapping phases (Fig. 4). A slightly overlapping arrangement like this is more process-tolerant and demands less total time and fewer circuit elements than a nonoverlapping clock would. The three-phase clock can overlap slightly because each circuit segment remains stable for two phases after its state changes.

With careful choice of the functions of the data and control machines in each phase, both machines can work together in a pipeline structure. All circuits have ample time to operate in each phase. Balancing data-handling tasks minimizes the number of devices and therefore power consumption in the control and data machines.

During the three microcycle phases, the data machine performs a complete operation by reading two registers and writing in one. Other logic on the chip modifies these operations by providing constants like vectors and addresses, indirect register addressing, and conditional data such as a branch or priority status based on data in particular registers. The control machine of the microprocessor computes new control signals during the last, or write, phase of the data machine.

The bus machine usually cycles in six phases. Its cycle begins one phase after the data machine reads and ends one phase after the data machine writes. During intervening phases, it generates external control strobes and waits for support chips to complete their portions of the data transfer. □

Bi-FET op amps invade 741's general-purpose domain

by Jim Williams
National Semiconductor Corp., Santa Clara, Calif.

Thanks to their low-drift microampere supply currents and picoampere bias currents, recently introduced bipolar field-effect-transistor operational amplifiers like National's LF441 can be used in applications that general-purpose amplifiers like the 741 cannot address. A high-performance pH meter, logarithmic amplifiers, and a voltmeter-checker reference source may be inexpensively built with this bi-FET operational amplifier.

The low-bias input of the 441 provides an excellent nonloading port for a pH probe, which is used to measure the acidity or alkalinity of a solution (Fig. 1). This simple four-chip interface yields a linear 0-to-10-volt output corresponding directly to the value of the pH (0 to 10) being measured, a range that is more than adequate for many applications.

The output from buffer A_1 is applied to A_2 , a tuned 60-hertz filter that removes power-line noise. A_2 also biases op amp A_3 , which provides a compensation adjustment for the probe's temperature. A_4 allows the probe to be calibrated.

To calibrate the circuit, the probe is immersed in a solution having a pH of 7. The solution's temperature is normalized for the meter by R_1 , a 10-turn 1,000-ohm potentiometer whose value may be set between 0 and 100 units. These values correspond directly to a solution temperature range of 0° to 100°C. Potentiometer R_2 is then adjusted for an output voltage of 7 v.

A conventional logarithmic amplifier (Fig. 2a) utilizes

the well-known logarithmic relationship between the base-to-emitter voltage drop in a transistor and its collector current. Here, A_1 acts as a clamp, forcing the current through Q_1 to equal the input current, E_{in}/R_{in} . Q_2 provides feedback to A_2 , forcing Q_2 's collector current to equal A_2 's input current, which is established by the LM185 zener-diode reference.

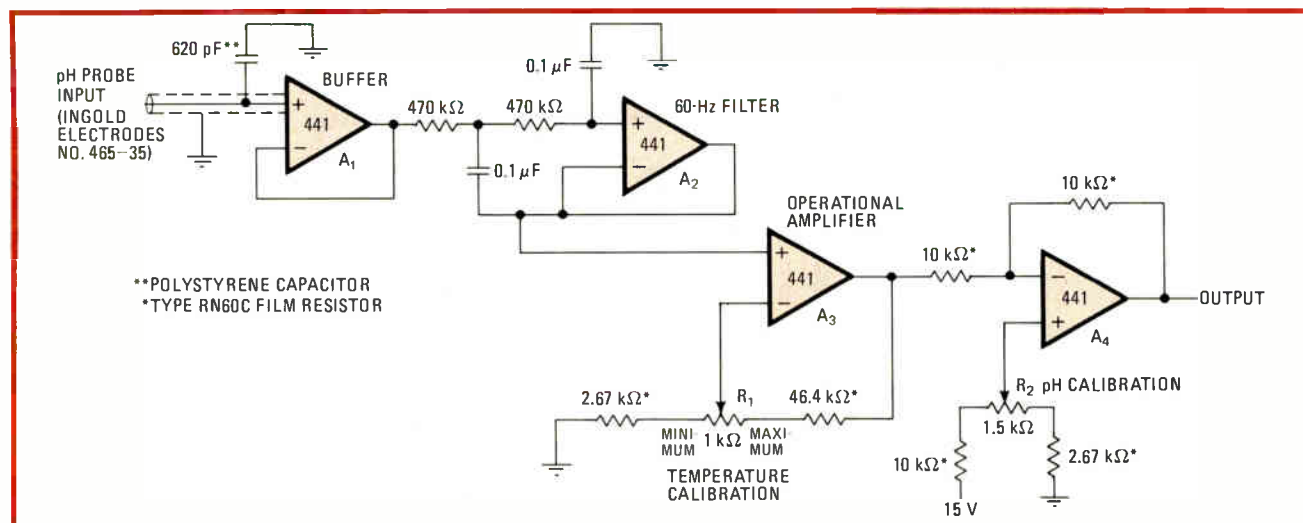
Because Q_2 's collector current is constant, its emitter-to-base voltage is fixed. The base-to-emitter drop of Q_1 , however, varies with the input current. The circuit's output voltage is therefore a function of the difference in the V_{be} voltages of Q_1 and Q_2 and is proportional to the logarithm of the input current. In this manner, the V_{be} drift is cancelled. The coefficient of this term will vary with temperature, however, and cause a drift in the output voltage. The 1,000- Ω thermistor compensates for this drift, stabilizing A_1 's gain.

The 441's 50-pA bias current allows accurate logging down into the nanoampere region. With the values shown in the circuit, the scale factor for the amplifier is 1 v/decade.

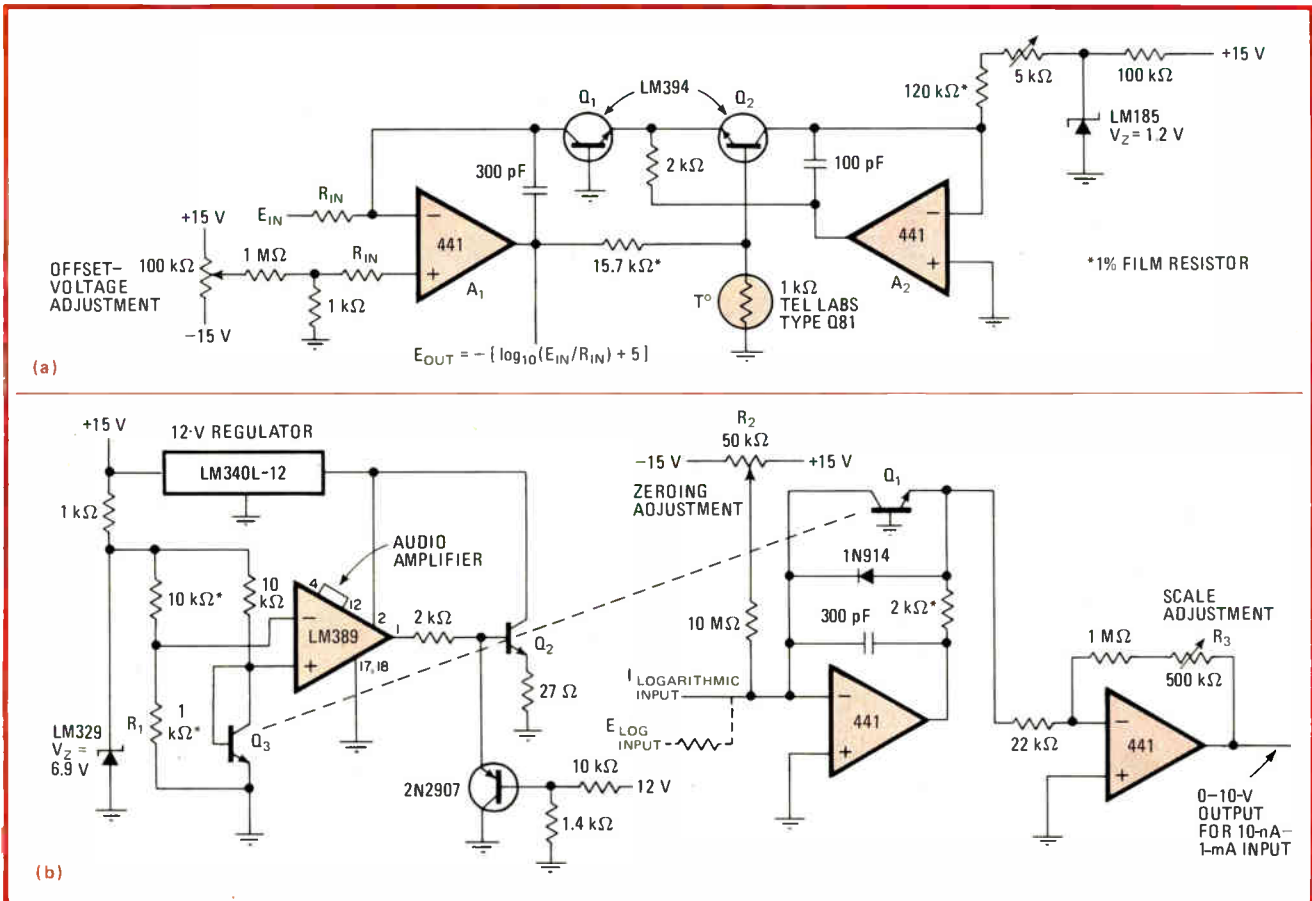
A second type of logarithmic amplifier is shown in (b). This unconventional design completely eliminates the temperature-compensation problems of (a) by temperature-stabilizing logging transistor Q_1 . This temperature problem is economically eliminated by utilizing the LM389 audio-amplifier-and-transistor array as an oven to control the logging transistor's environment.

Transistor Q_2 in the LM389 serves as a heater, and Q_3 functions as the chip's temperature sensor. The LM389 senses Q_3 's V_{be} , which is temperature-dependent, and drives Q_2 to feed back the chip's temperature to the set point established by the 1-to-10-kilohm divider. The LM329 reference ensures that the power supply is independent of temperature changes.

Q_1 , the logging transistor, operates in this tightly controlled thermal environment. When the circuit is first



1. Acids and bases. This four-chip interface converts the output of a pH probe into direct readings of a solution's acidity and alkalinity. The circuit has a filter to reject the ac line noise that plagues instruments of this type. This unit can easily compensate for temperature variations.



2. Low-power loggers. With amplifier A₁ clamping current through transistor Q₁ to input value E_{IN}/R_{IN} and with A₂ holding Q₂'s current constant with LM185's reference, circuit (a) yields a logarithmic response by virtue of proportional differences between Q₁ and Q₂'s well-known V_{be}-to-collector current relation. A more advanced version (b) uses an LM389 to eliminate temperature effects on output.

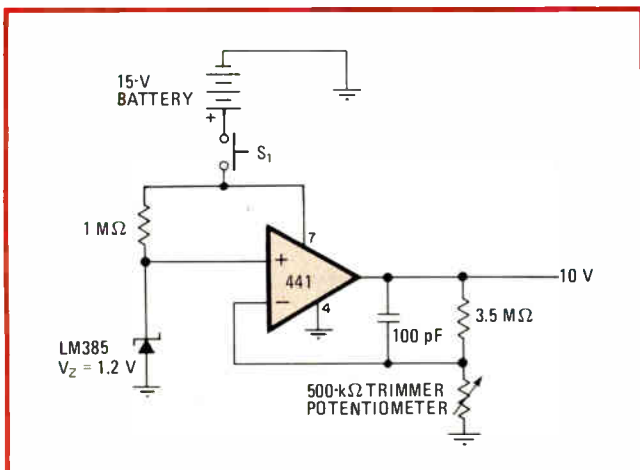
turned on, Q₂'s current flow becomes 50 milliamperes forcing the transistor to dissipate about 0.5 watt, which raises the chip to its operating temperature rapidly. At this point, the thermal-feedback circuit takes control and adjusts the chip's power dissipation accordingly. The LM340L voltage regulator has only 3 v across it, so it

never dissipates more than about 0.3 w. The pnp-transistor clamp at the base of Q₂ prevents feedback lock-up during circuit start-up.

To adjust this circuit, the base of Q₂ should be grounded, then the power applied to the circuit, and the collector voltage of Q₃ measured at room temperature. Next, Q₃'s potential at 50°C is calculated, a drop of -2.2 millivolts/°C being assumed. The value of R₁ should be selected to yield a voltage close to the calculated potential at the LM389's negative input. After Q₂'s base is removed from ground, the circuit will be operational.

A₁'s low bias current allows values as low as 10 nanoamperes to be logged within 3%. Potentiometer R₂ provides zeroing for the amplifier. Potentiometer R₃ sets the overall gain of the circuit.

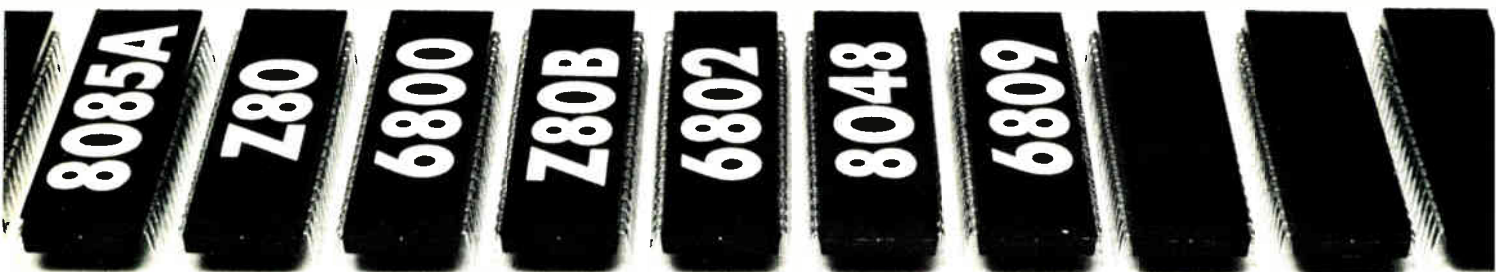
The low power consumption of the 441 is useful in a calibration checker for digital voltmeters that only draws 250 μA (Fig. 3). Here, the 441 is used as a noninverting amplifier. The LM385 is a low-power reference that provides 1.2 v to the input. This voltage is simply scaled by the feedback-resistor network to yield exactly 10 v at the circuit's output. The circuit will be accurate to within 0.1% for over a year, even with frequent use. □



3. Long-term accuracy. Using a single LF441 and a 1.2-volt reference, this circuit for calibrating digital voltmeters with a 10-V signal draws only 250 microamperes. Using a 15-v power source, the circuit has an output accuracy within 0.1% over a year's time.

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Current-biased transducer linearizes its response

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

Transducers that work on the principle of variable resistance produce a nonlinear response when voltage-biased, as in common bridge configurations. However, a single operational amplifier configured to provide current biasing for the transducer eliminates this difficulty and allows output offset voltages to be controlled or removed.

As a voltage-biased transducer's resistance varies, so does the current through it. Thus, any signal voltage taken from the transducer will be a function of both current and voltage variations and will be a nonlinear function of the transducer's resistance.

Current biasing rather than voltage biasing avoids this nonlinearity, but reference current sources are not as readily available as voltage ones. Fortunately, an op amp can convert a reference voltage for this purpose and in addition provide other benefits.

In (a), a voltage-to-current converter circuit is adapted for voltage control of the supply current and of the output offset voltage. As laid out, the transducer's bias current is $I_x = (V_2 - V_1)/R_1$, where V_1 and V_2 are the externally applied control voltages. The current polarity can be set at either + or -, allowing an inverted or noninverted voltage response to variations in transducer resistance.

The resulting current flow in the nominal transducer resistance, R , produces an offset voltage at the circuit's output with a counteracting voltage developed by V_1 : $V_{os0} = (1 + (R_2/R_1))I_x R - (R_2/R_1)V_1$. Thus, through the proper selection of V_1 , the output offset may be nulled to

zero or set to either a positive or negative polarity.

Signal variations about that level result from a change in transducer resistance. The net voltage output then becomes $e_o = [1 + (R_2/R_1)]I_x \Delta R + V_{os0}$. This response is linearly related to ΔR . Also the signal is amplified.

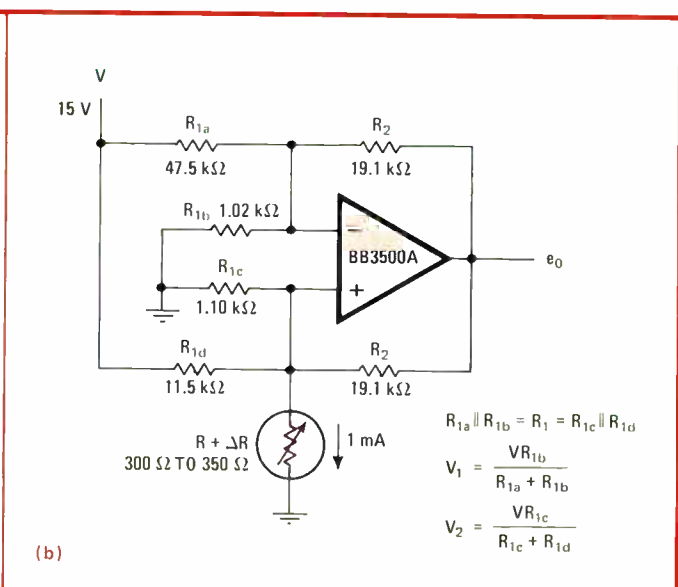
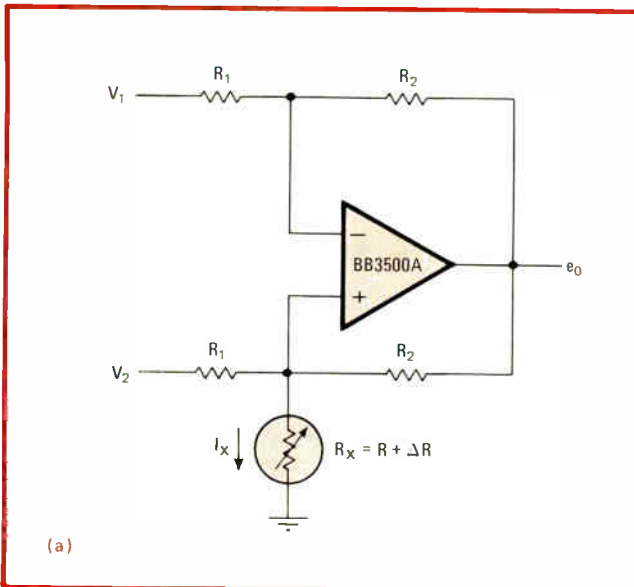
To set the gain, R_2 should be adjusted after R_1 , which sets the level of I_x , is selected. Because the output signal is taken directly from the amplifier's output, the transducer is buffered against loading effects.

Deviations in the described performance result primarily from voltage and resistor tolerances and from resistor-ratio error. Mismatch of the R_2/R_1 ratio is particularly serious, as this will make I_x somewhat a function of ΔR , thereby reintroducing nonlinearities in the circuit. Such a mismatch will alter the term in the denominator of the I_x formula to read $((R + \Delta R)/R_2) \times ((R_2/R_1) - (R_2'/R_1'))$, where R_1' and R_2' are the mismatched counterparts of R_1 and R_2 , respectively. Further errors will result from the dc input-error signals of the op amp. As a result, the deviation in e_o will be:

$$\Delta e_o = \left[1 + \frac{R_x}{R_2} \left(1 + \frac{R_2}{R_1} \right) \right] \left[\left(1 + \frac{R_2}{R_1} \right) V_{os} \right] + \left(1 + \frac{R_2}{R_1} \right) R_x I_{os} + R_2 I_B$$

where V_{os} , I_{os} , and I_B are the input offset voltage, input offset current, and the inverting input-bias current of the op amp, respectively. Making the R_2/R_x ratio large reduces this error.

In practice, it is either inconvenient or sometimes undesirable to supply two voltage references to the circuit. A single reference voltage may be applied, as shown in (b), which is the Thévenin equivalent of the circuit in (a). For the specific component values given, the amplifier will deliver a 1.0-volt full-scale output signal with a zero offset in response to a transducer resistance that ranges from 300 to 350 ohms. □



Holding constant. A voltage-controlled current source drives transducer (a) so that its output voltage is a function of its resistance change only, thereby reducing the circuit's nonlinear response. The output offset can also be virtually eliminated. The single-reference current source circuit (b), which is the Thévenin equivalent of (a), may be more attractive to implement in some cases.

Electron beam writes next-generation IC patterns

Variable spot shaping and subfield vector-writing techniques let beam write from twenty to forty-five 3-inch wafers per hour

by R. Moore, G. Caccoma, H. Pfeiffer, E. Weber, and O. Woodward, IBM Corp., General Technology Division, East Fishkill, N. Y.

International Business Machines Corp. has been employing its EL-1 and -2 direct-writing electron-beam lithography machines for more than five years to produce 1-to-2.5-micrometer logic chips. Now the EL-3 electron-beam tool, which incorporates a number of major improvements in electron optics, analog and mechanical operation, and electron-beam architecture, has started coming on line. This system achieves higher throughputs and finer line widths while adding mask making to its direct-writing functional mode.

Two versions of the machine are currently in use at the corporation's General Technology division in East Fishkill, N. Y. One is part of the division's QTAT (Quick Turn Around Time) wafer-processing line. The other

Despite their high resolution and overlay accuracy, electron-beam lithography systems are still mainly used to produce integrated-circuit masks. Though the machines can write directly on wafers, they take 15 minutes to an hour to complete each one—a pace that restricts that capability to research and development applications.

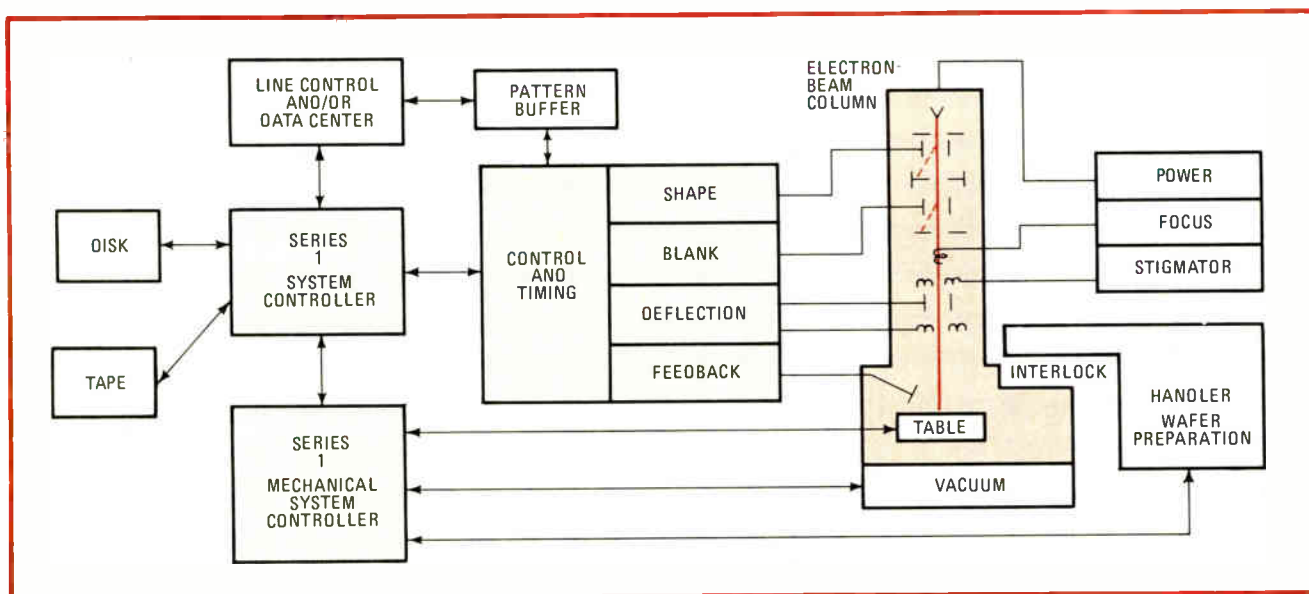
Now two new electron-beam systems with much greater throughputs have appeared. IBM Corp.'s EL-3 (this article) uses a variably shaped scanning electron beam to expose thirty 4-inch wafers an hour. In England, Philips Research Laboratories has revived and improved the electron-beam projector, which floods a wafer with electrons. This system (see p. 144) has an hourly throughput of twenty-four 4-in. wafers.

-Jerry Lyman

serves as a mask-making tool for 10× reticles and 1× optical masks. Under development since 1978, the EL-3 is currently being used to produce device patterns in the 1- μm -to-2- μm range. The design approach was to attack each of the operational sequences that affect system performance so that the system throughput would not be limited by a weak link in the overall system design.

The block diagram of an EL-3 system is shown in Fig. 1. Its operation is controlled by two IBM Series/1 computers. One acts as the system controller, initiating, monitoring, and controlling all system functions. A keyboard and cathode-ray-tube display form the operator station at which major system functions are initiated and monitored. The other com-

controlled by two IBM Series/1 computers. One acts as the system controller, initiating, monitoring, and controlling all system functions. A keyboard and cathode-ray-tube display form the operator station at which major system functions are initiated and monitored. The other com-



1. Dual control. IBM's EL-3 electron-beam lithography system is controlled by two Series/1 computers. The system controller initiates, monitors, and controls all electro-optic functions. The mechanical controller handles functions like vacuum control and wafer positioning.

puter is the mechanical-system controller, directing mechanical functions upon commands it receives from the system controller.

Wafers may be loaded either singly, by hand, or through a wafer preparation unit from multiwafer cartridges or an air-track system. Wafer serial numbers and other data are supplied by either the operator or optical readers on the air track in the automated QTAT line.

The variably-shaped-spot electron-beam column is mounted directly over the X-Y table, allowing it to write chip sites sequentially as the table moves them into position. A focus grid, calibration grid, and Faraday cup are also mounted permanently on the X-Y table, permitting both manual and automated calibration and diagnostic functions. Diodes located above the table detect backscattered electrons from registration marks and the calibration grid.

A column interface unit controls the electron beam's size, exposure time, and position for writing patterns and also processes backscattered signals for registration and calibration. It powers the column, maintains beam quality (its focus, current density, and alignment), and translates pattern data on rectangle position and size into data on individual spot sizes and positions.

The pattern buffer is a modified 3168/08 memory that gives fast access to pattern data so that throughput is not limited by data delivery. During wafer exposure, the pattern buffer streams data into the digital section of the column interface unit, using a direct 8-byte-wide data path. The pattern buffer is loaded from the system controller's disk storage via a Series/1 input/output data path. The resident pattern library is stored on disk or tape. Very large libraries, such as the one on the Fishkill QTAT line, house thousands of part numbers; here a host data processor provided the required part number.

Architectural features

The EL-3's architecture was designed to take advantage of state-of-the-art electro-optical and system techniques. New pattern-writing techniques use subfield vector deflection and rectangle pattern generation. Mechanical techniques incorporate laser control for mask making. New controller and memory approaches and innovative software apply to both system control and postprocessing of data.

The primary characteristics of the EL-3 are:

- Variable spot shaping with 0.025- μm size increments. This, along with the 0.025- μm spot positioning resolution, permits good process windage control, flexibility of design grid selection, and avoidance of spot overlapping.
- A subfield vector-writing technique. Fields are divided into subfields. Patterns are written by a vector technique within each subfield, so areas not occupied by pattern elements need not be covered. Electric plates used for deflection within a subfield are driven by wideband circuits at high speed to minimize writing time. Narrowband, low-noise magnetic deflection is used to step from subfield to subfield in a raster pattern. This repetitive deflection pattern allows an automated calibration similar to the process used in the EL-1 and -2 to correct for static and repetitive transient errors. The subfield vector-writing technique achieves throughputs similar to those

KEY SPECIFICATIONS OF EL-3 ADVANCED DIRECT-WRITING ELECTRON-BEAM SYSTEM

Parameters	Values	
	1- μm images	2- μm images
Field size	5 mm	10 mm
Beam edge resolution	0.25 μm	0.5 μm
Overlay accuracy (mean +3 σ)	0.4 μm	0.7 μm
Beam current density	50 A/cm ²	50 A/cm ²
Throughput (3-in. wafers/h at 10- $\mu\text{C}/\text{cm}^2$ doses)	10-20	20-45

of vector systems, and its pattern accuracies approach those of a well-calibrated raster-scanning system.

- A rectangle writing technique in which pattern elements within a subfield are composed by connecting rectangular elements. This allows the use of a hardware rectangle generator to expand pattern data from simple rectangle location and size data to the number of spot shapes and locations that are required to outline and fill in the rectangle.
- Dynamic exposure control where control data interspersed with pattern data can be used to vary beam dosage from rectangle to rectangle. This feature is useful to control pattern size errors due to proximity effects.
- A modular system concept in which the system is composed of a number of functional field-replaceable units. This design increases serviceability and makes it easier to tailor the system for various applications.
- A laser-interferometer X-Y table control whose resolution and accuracy successfully reduce table-related positioning errors.

The table lists key parameters for two typical applications. Tradeoffs are illustrated between patterns using 1- and 2- μm minimum line widths.

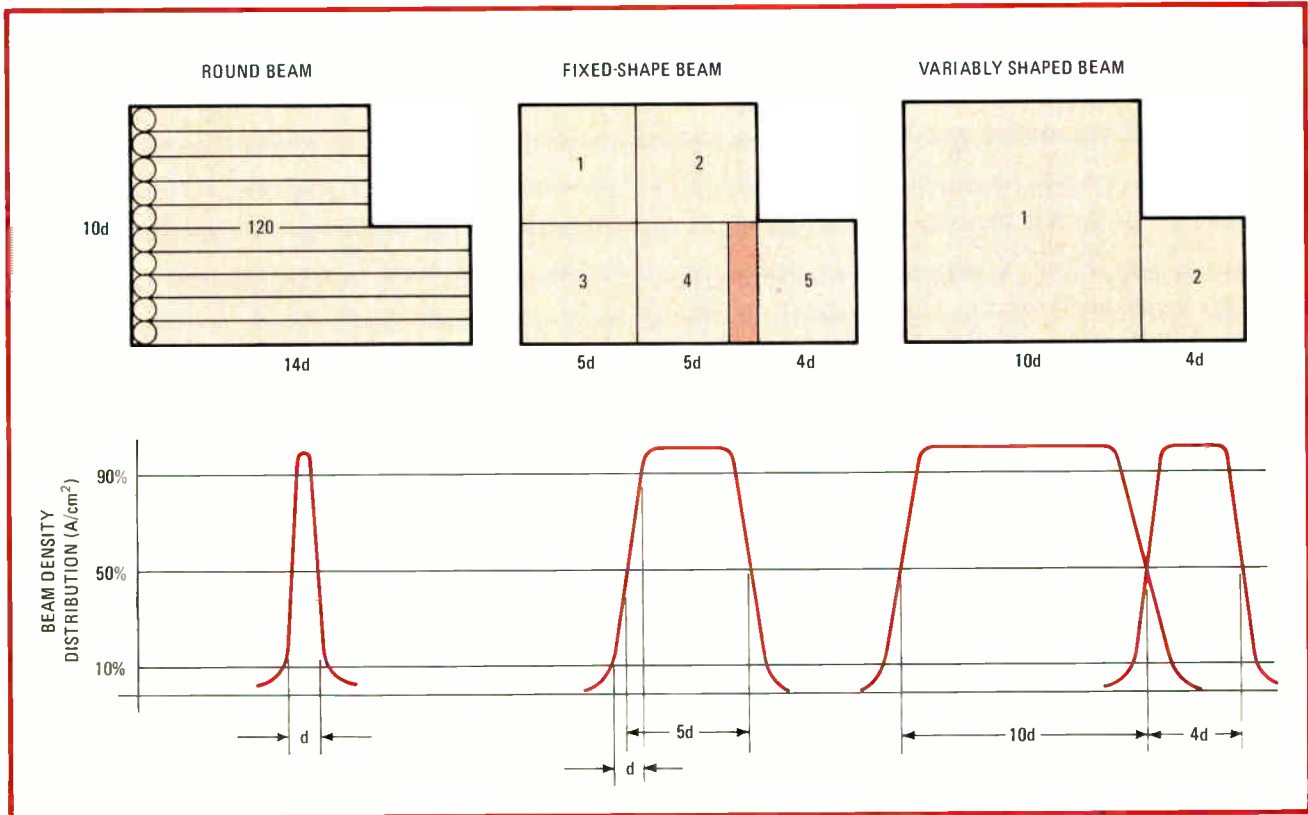
The field size ranges up to 10 millimeters, but is limited by the system resolution limit of 5,000 fabricated lines per field. Beam resolution itself is defined by the beam edge slope, which is one quarter of the minimum line width. This means that a pattern of 25 million spots can be addressed, or 2,500 by 2,500 square spots with spacing equal to the squares can be fabricated.

The available spot current density and the resist sensitivity together determine the required exposure time per spot. For example, 50 amperes applied to 1 square centimeter of 10-microcoulomb resist require a spot exposure time of 200 nanoseconds.

Overlay is limited by the calibrated accuracy and stability of the analog system, the quality of registration marks, resist thickness, and field size. The three-sigma overlay is for second-order registration for multiple tools.

Throughput variables

Throughput is affected by many factors. The major ones are pattern density or area to be written, X-Y table move time, wafer-handling time, registration time, spot-stepping time, and subfield stepping time. The throughput figures are typical for real patterns for logic and memory chips scaled to the resolutions and to the field



2. Shaped beams. A key to the EL-3's high throughput is its variable spot shaping. The area illustrated requires 120 exposures to a standard round beam but only 5 exposures to a fixed-shape beam with 25 image points and just 2 exposures to a variably shaped beam.

sizes shown. The geometrical average of throughputs from all levels are indicated in the table.

Variable spot shaping is a key feature of the EL-3. Spot shaping represents a combination of scanning and projection techniques. The fast exposure rate of pattern projection is combined with flexible, computer-controlled pattern writing. Figure 2 illustrates the beam characteristics that give shaped beams a basic throughput advantage over the conventional Gaussian round-beam approach.

The scanning-electron-microscope-type round beams expose one image point at a time—very much like the scanning beam in a television tube. The round beam dimension, d , defined as 50% of the width of the intensity distribution, represents the optical resolution and for most lithography applications is four or five times smaller than the minimum pattern feature. It requires a maximum of 120 beam diameters to expose the pattern element shown.

For shaped beams, the spatial resolution given by the edge slope, d , of the beam profile is decoupled from the size of the beam spot, $5d$. Consequently a plurality of image points can be projected in parallel without loss of resolution. The fixed-shape beam of IBM's EL-1 system represents the first step in the direction of parallel pattern exposure: 25 image points are projected and the exposure speed is increased accordingly, for only 5 exposures are required instead of 120. It is desirable to vary spot size to eliminate spot overlap in regions of partial spot exposures and to further increase exposure efficiency of multiple images on a wafer.

With the variably-shaped-spot technique it is possible to tailor beam spot size and shape to fit various pattern elements. Shaping variations take place within the few nanoseconds it takes the beam to step from position to position. This technique eliminates spot overlap. The maximum size of the spot can then be several times that of the minimum pattern feature, projecting 100 or more image points in parallel. Coulomb interaction between beam electrons imposes practical limits on the maximum spot size and resolution.

The spot-shaping method used for EL-3 is illustrated in Fig. 3. Two square apertures shape the beam spot. The image of the first aperture appears in the plane of the second one and can be shifted laterally with respect to it. A particular fraction of the total beam, which depends on the shaping signal applied to the electrostatic deflector, passes through both apertures. The compound image that as a result is formed by both apertures is subsequently demagnified.

The electron source illuminates the first square aperture and an alignment servo maintains stable illumination. The first condenser performs the two functions of imaging the first aperture onto the second one and projecting the source image onto the center of the spot-shaping deflector. A second alignment servo maintains the relative position of the two apertures. Two demagnification lenses reduce the size of the variable spot image by two orders of magnitude. This reduction brings it close to the dimensions of the final image, which is then projected onto the target.

The magnetic deflection system permits placement of

the variably shaped spot within a field of up to 10 by 10 mm with a maximum of 25,000 resolved lines per field, or 5,000 fabricated lines per field. Complex aberration-compensation schemes would have to be employed to achieve larger field coverage.

Deflecting decisions

The choice of a deflection system depends on many factors. The subfield vector technique has been implemented with a repeating magnetic deflection that is easily corrected by a learn technique as used on EL-1 and EL-2. Learn consists of scanning a reference grid prior to writing, so as to form corrections and then apply them to the deflection during writing to eliminate errors. Transient errors caused by electronics, eddy current, hysteresis, and so on are all corrected, as are linear deflection errors.

Dual-channel deflection solves the noise problem for both raster and vector. Raster system throughput is independent of pattern coverage as the whole field is scanned. A vector system, on the other hand, need scan only the written areas, but the time it requires to make the jumps between pattern features becomes long for complex patterns.

In a shaped-spot raster system, spot depletion can occur for complex patterns where the number of spots required in a given area exceeds the number available. A vector system, however, utilizes as many spots as required before moving to the next pattern element. Vector systems also have an inherently simpler data format—one that defines pattern elements as dimensional geometric shapes at a given field location. This feature makes it easier to utilize hardware for expansion of pattern data from geometric-shape definitions to the individual spot definitions that are required to generate deflection control signals.

The EL-3's architecture is based on experience gained in the development of the vector systems in IBM's Yorktown Heights division and the EL-1 and -2 at Fishkill. Features of both raster-scanning and vector-writing systems are combined as shown in Fig. 4. The field is divided into a large number of overlapping subfields with a periodicity of 75 μm .

Within each subfield, patterns are written as a series of rectangles that are addressed in vector fashion. Subfield-to-subfield moves are made in a stepped raster mode, with all subfields visited whether or not they contain patterns. This regular and repetitive deflection pattern allows an automated calibration system that corrects static and repetitive transient errors. Combining automated calibration with the dual-channel deflection system pioneered in the EL-1 and EL-2 results in high writing throughput.

Rectangles within a subfield are rapidly written using wideband circuitry to drive electric deflection plates at high speed. Deflection errors caused by electronic noise admitted by the wideband circuits are not significant

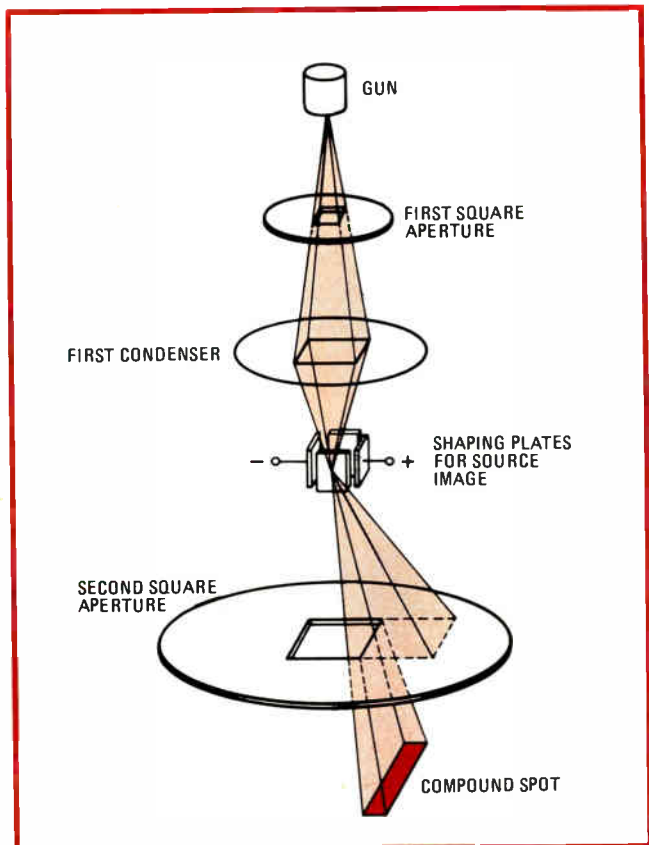
3. Squared electrons. In the EL-3's electron-beam column, the first aperture squares the beam. The condenser lens images the shaped beam onto a second square aperture. The resulting image's position can be shifted electronically by the shaping plates.

because the deflection range is limited to 100- μm subfields. Narrowband magnetic deflection circuits drive a deflection yoke to step the beam from subfield to subfield. Noise-related errors are kept to an acceptable value over a 10-mm range because the narrowband circuitry causes the stepping time between subfields to be relatively long. However, the number of subfields is relatively small compared with the number of pattern elements; it has been shown mathematically that a significant savings in writing time results by use of this dual-channel deflection system over a single-channel system, with equivalent errors. A single-channel deflection having the wide bandwidth required for high-speed writing would have objectionably high random noise errors. Combining a narrowband wide-range magnetic deflection with a wideband narrow-range electrostatic deflection minimizes noise errors.

Rectangles defined

The pattern data format employs 8 bytes of data per rectangle to define its position and size and the controls necessary for the rectangle generator hardware to generate the number of spots and shapes required to complete the rectangle. This technique, combined with the use of the pattern buffer accessed directly by the rectangle generator, relieves the Series/1 of high-speed data-transfer duties and reduces pattern storage requirements. Control data provides variable exposure time (gray levels). Each rectangle can have three specified values of gray: internal, plus edge and alternate-edge, either of which can be applied to any edge.

Integrated circuits are fabricated by successive pro-



cessing steps applied to a semiconductor wafer. Prior to most of these processing steps, a sensitive photo-resist layer is deposited on the wafer and a pattern is exposed onto it. When this resist is developed, the resulting pattern allows subsequent process steps to act selectively on different areas of the wafer.

The relationship of each succeeding pattern to the others makes it necessary for each layer to overlay the preceding ones precisely. Errors in mechanical handling, changes in a given exposure tool, and differences among tools make it difficult to align a pattern with underlying ones. These errors must be determined and corrected to assure good overlay of the next pattern.

In the EL-3, marks consisting of parallel bars are placed in the four corners of each chip on the wafer to allow the electron beam to register and overlay a pattern on lower-level patterns. The beam scans the horizontal and vertical bars to locate the corners of the chip relative to the writing fields. X and Y errors detected in each corner are used to compute the correction to be applied to the beam while writing the chip.

Registering details

One chip site contains wafer registration marks. These larger marks are scanned first, after a wafer is loaded onto the X-Y table, to determine and correct errors associated with mechanical handling. An accurate prediction of the location of the first chip site is made, a feature that allows the individual chip registration marks to be smaller and thus occupy less valuable silicon real estate. The corners of the chip and the writing field are forced to match by applying independently in both X

and Y directions corrections for translation, magnification, rotation, and trapezoidal distortion. These corrections are made for each individual spot by specialized digital hardware that can compute the correction required within each 200-ns spot time.

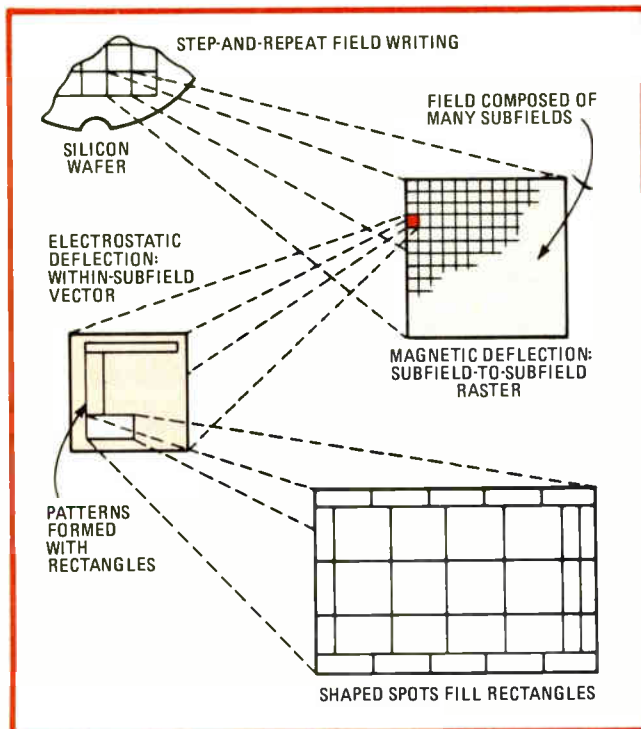
Combining a variably shaped spot and subfield vector deflection enables the EL-3 to write patterns very fast. Writing speed is influenced by pattern characteristics such as density, feature size, and element count. Beam current density and resist sensitivity determine the exposure time required per unit area.

Besides writing time, several other operations add their own overhead times. Deflection times required between spots and pattern elements further add writing intervals whose duration depends on pattern characteristics. Subfield-to-subfield deflection, registration, X-Y table moves, and wafer handling add overhead times independent of pattern characteristics.

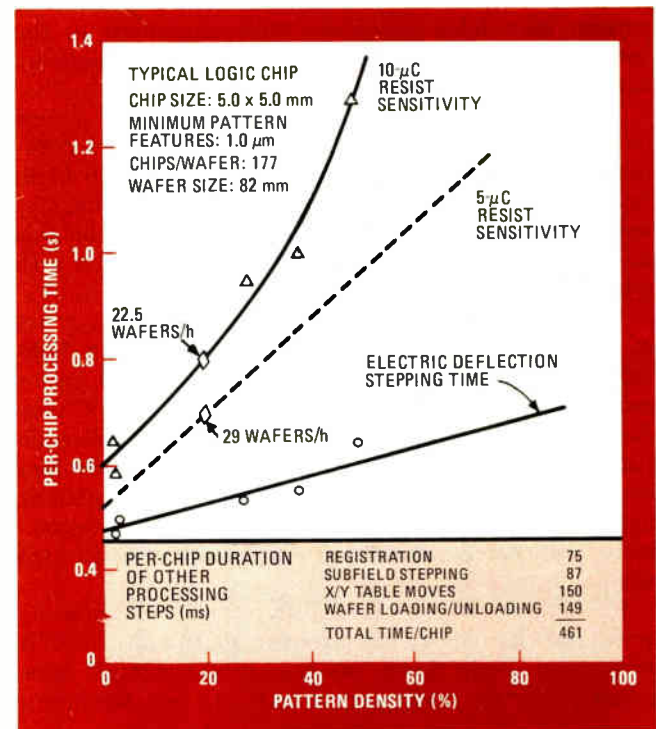
Figure 5 illustrates these influences on throughput for the case of a typical high-density logic chip with minimum features of 1 μm . The average hourly throughput for five exposure levels with pattern densities ranging from 2% to 50% is about 20 wafers for a 10- μC resist. Doubling resist sensitivity to 5 μC increases the average hourly throughput to 29 wafers.

The EL-3 mechanical systems represent the state of the art in automated wafer handling as far as electron-beam lithography systems are concerned. Key subsystems include a wafer-loading and -unloading unit, an X-Y positioner, and a vibration-isolation system.

The loading and unloading system transfers a pre-loaded wafer carrier from an external access point to an



4. Writing technique. The EL-3 combines both raster and vector writing. The field is first divided into subfields where patterns formed as rectangles are addressed vectorially. Subfield-to-subfield moves are made in a stepped-raster mode. All subfields are covered.



5. Throughput. Writing speed is influenced by pattern density, resist sensitivity, and housekeeping times. The top curve shows a 22.5-wafer-per-hour throughput for a 10-microcoulomb resist. Doubling resist sensitivity increases throughput to 29 wafers/h.

X-Y table within the vacuum chamber without disrupting vacuum integrity. The wafer carrier is placed in atmospheric pressure on the elevator platform, which protrudes over the top of the vacuum chamber (Fig. 6). A lid is lowered over the top of the elevator, forming a small auxiliary chamber around the carrier. This antechamber is evacuated through turbo pumping to 5×10^{-2} torr. When both sides of the elevator platform are within reasonable vacuum levels, the elevator is lowered and the two dissimilar pressures reach equilibrium without disrupting the main chamber's vacuum.

The carrier, located on the elevator, descends to a preset position, on a level with the X-Y table. Once elevator travel is complete, the transfer gripper arms (beginning from the home position) simultaneously extend, grip both wafer carriers (on the elevator and on the X-Y table), retract, rotate 180° , and extend again, placing the carriers on the elevator and X-Y table. Finally the gripper again retracts and rotates another 180° back to its home position, ready to begin another cycle.

The elevator then ascends to the diaphragm seal on the underside of the vacuum chamber's access plate below the auxiliary lid. The auxiliary chamber is filled with dry nitrogen gas until it reaches atmospheric pressure. The auxiliary lid rises and the carrier is removed. The entire wafer-carrier transfer process is typically completed in 20 seconds and can be done automatically.

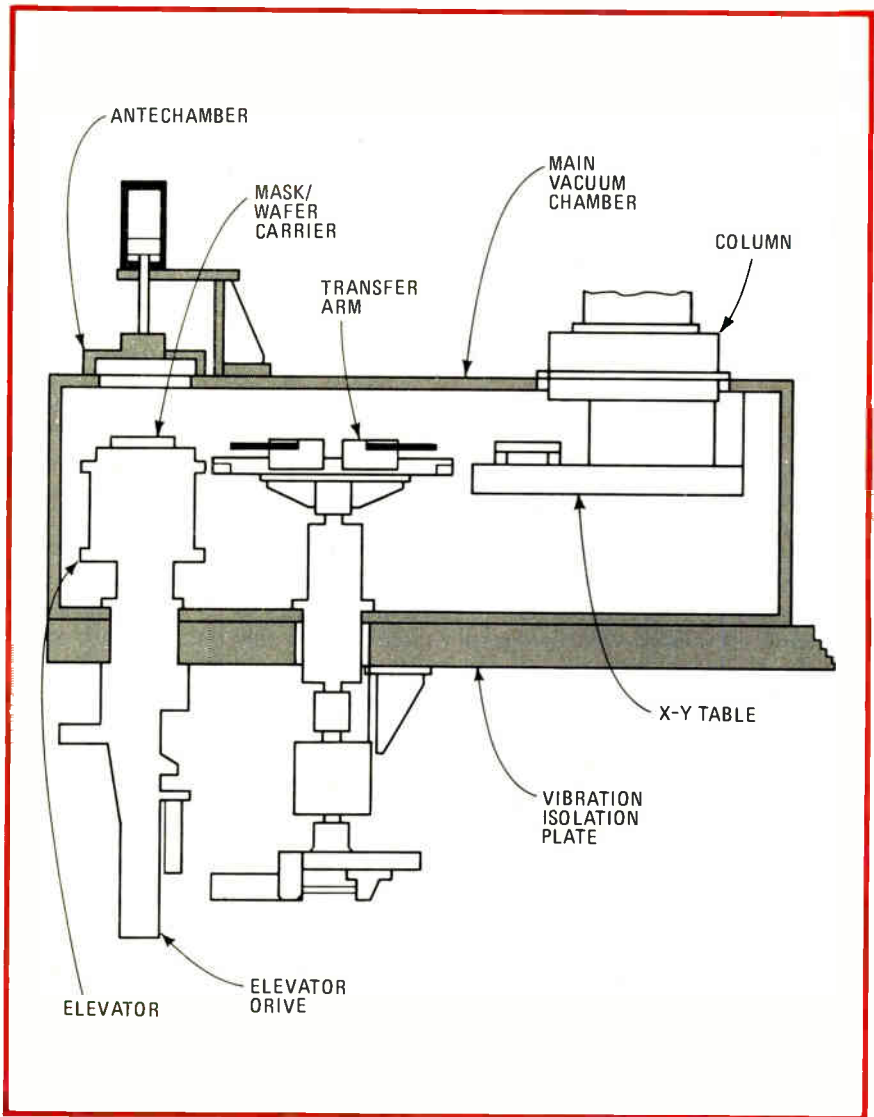
The X-Y positioning subsystem consists of a custom-design X-Y stage, a laser interferometer, and X-Y logic and control. The X-Y system is under the control of an IBM Series/1 computer.

The upper stage of the table is equipped to hold a carrier-mounted workpiece. The stage is moved under computer control to various X-Y coordinates to bring various portions of the workpiece under the beam for writing.

Precise positioning

The X-Y stage is equipped with mirrors mounted perpendicular to each axis. A laser transducer senses movement of the stage (via the mirrors) and thus feeds position information back to the system. A fast pulse converter, comparator, digital-to-analog converter, driver, motor, and tachometer combine to form a velocity servo system that moves and positions the X-Y stage quickly and automatically.

Magnetic materials are not used in the X-Y table



6. Load and unload. Automated wafer handling, X-Y positioning, and vibration isolation are illustrated in this view. Wafers can be transferred from outside the vacuum chamber to an X-Y table within the chamber without affecting the integrity of the vacuum.

construction so that the table position will not influence the magnetic fields associated with electron-beam deflection and cause the beam position to vary. Conductive materials that give rise to eddy currents are also minimized so as not to affect the beam position.

The mirror mounted on the X-Y stage, which the laser uses to determine the stage's position, is extremely flat, orthogonal, and stable to minimize error introduced by the absolute stage-positioning accuracy.

The vibration-isolation system, which is critical in high-resolution direct writing, decouples all the vibration-generating elements, including pumps and motors, from the vacuum chamber, particularly in the column-wafer region during writing and registration. It also reduces the transmission of building vibrations to an acceptable level while isolating disturbances induced in the connecting cables and supply lines. In addition, it ensures rapid recovery from shocks produced internally or externally during the transferral of the wafer carrier to its various positions. □

Electron-beam projector suits up for submicrometer race

Lithography machine can define chip features as small as $0.2\ \mu\text{m}$; system throughput can be as high as twenty-five 4-in. wafers an hour

by Rodney Ward, *Philips Research Laboratories, Redhill, Surrey, England*

□ In the VLSI patterning sweepstakes, electron-beam projection has been something of a dark horse, but recent research and development efforts are turning it into a real contender against 1:1 and step-and-repeat optical projection, X-ray lithography, and direct writing with a scanning electron beam. These R&D efforts have put to rest the mistaken beliefs that image distortion and poor alignment of masks are insurmountable barriers in producing very large-scale integrated circuits with this type of system.

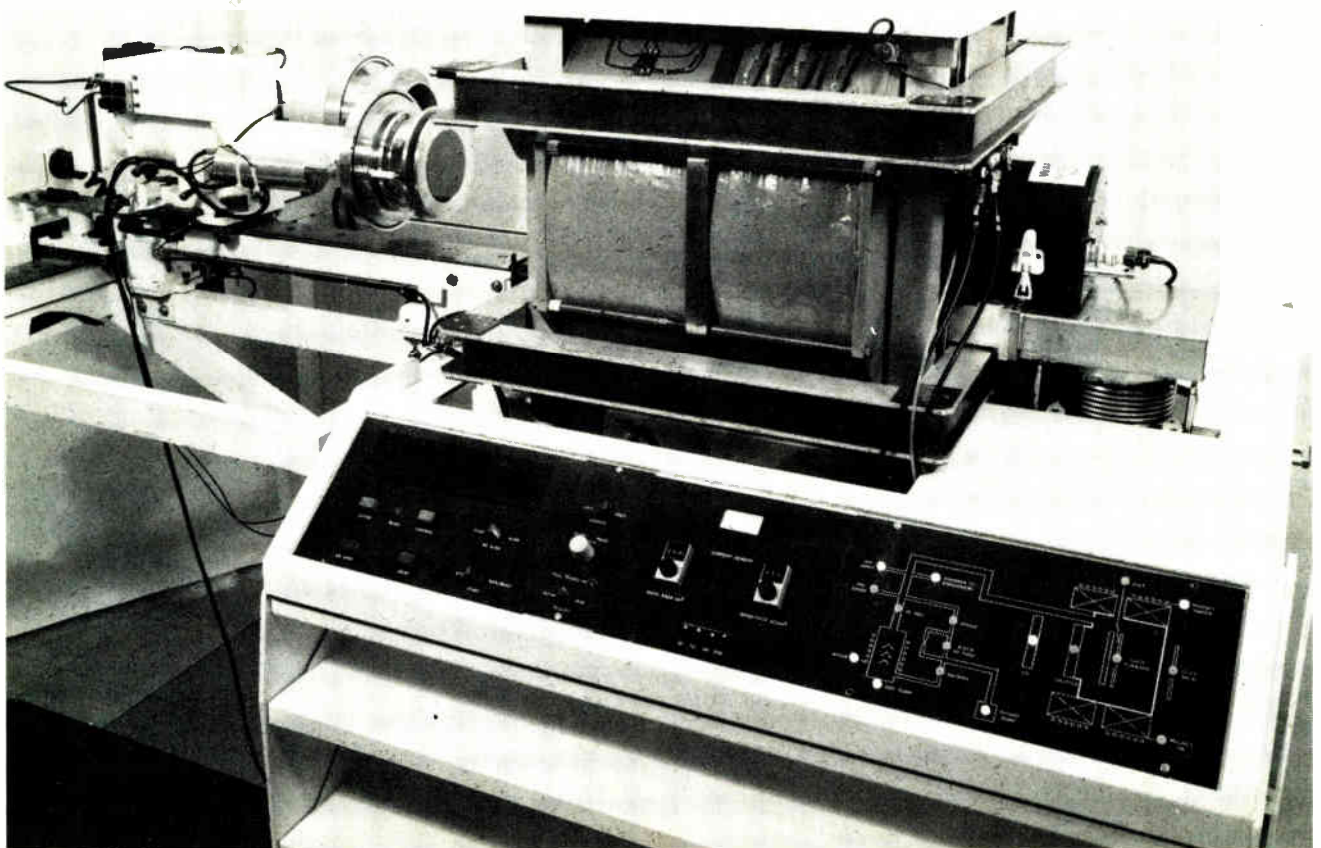
Actually, this lithography method has the potential for producing VLSI circuit details much smaller than those

The works. This electron-beam image projector can handle 4-in. wafers with exposure and alignment taking less than 30 seconds. Pattern features as small as $0.2\ \mu\text{m}$ can be defined, and the ultimate reduction should be less than $0.1\ \mu\text{m}$.

achieved optically and to do so more easily than with X-ray systems and more cheaply than with electron-beam direct writing. Image projectors are not ready for the production line, but the R&D effort described in detail here offers that promise.

The electron image projector is a pattern-copying machine that uses electrons to transfer the circuit image from a mask onto a silicon wafer. A number of companies have contributed to the development of the idea, notably Westinghouse Electric Corp.'s Defense and Electronic Systems Center, Baltimore, Md., Thompson-CSF in France, and Electron Beam Microfabrication Corp., San Diego, Calif.

However, R&D has been most energetically pursued at Philips, and a system has now been built that can expose 4-inch wafers. Featuring automatic alignment and magnification control, this machine can define patterns with



geometries as small as 0.2 micrometer. Exposure and alignment take less than 30 seconds, making the projector capable of a high throughput.

The structure of an electron-beam image projector (Fig. 1) is similar to that of its optical counterparts. Also, mask making—patterning a thin metal layer on a quartz substrate—uses techniques much like those employed in turning out conventional optical masks. The mask is coated with a thin evaporated layer of cesium iodide, which acts as a photoemitter. This material is particularly suitable because it can be rinsed off with water and replaced without any risk to the mask itself.

Image projection

Electrons are released into a vacuum from the clear areas of the mask by action of 1,849-angstrom radiation from an ultraviolet source and are accelerated across to the silicon wafer under the influence of an electric field. Focusing is achieved with a magnetic field parallel to the electric field.

Generally speaking, it is advantageous to work with a small separation between mask and wafer (that is, a large magnetic field) because this minimizes image distortion. In the assembled projector, shown in the opening photograph, an accelerating voltage of 20 kilovolts and a magnetic field of 250 kiloamperes per meter gives a separation of about 5 millimeters.

The large rectangular coils surrounding the focusing magnet in Fig. 1 deflect the image and are part of the alignment system. Masks and wafers are loaded into the machine on a trolley, which also accommodates the evaporator unit used to deposit the CsI photocathode.

The first requirement for any VLSI lithographic system

is that its resolution must be well into the submicrometer region. The fundamental resolution of the projector is determined by the energy spread of the emitted electrons (which also determines the depth of focus) and optical diffraction of the UV radiation. Together these two effects give a resolution limit of about 500 \AA (0.05 \mu m).

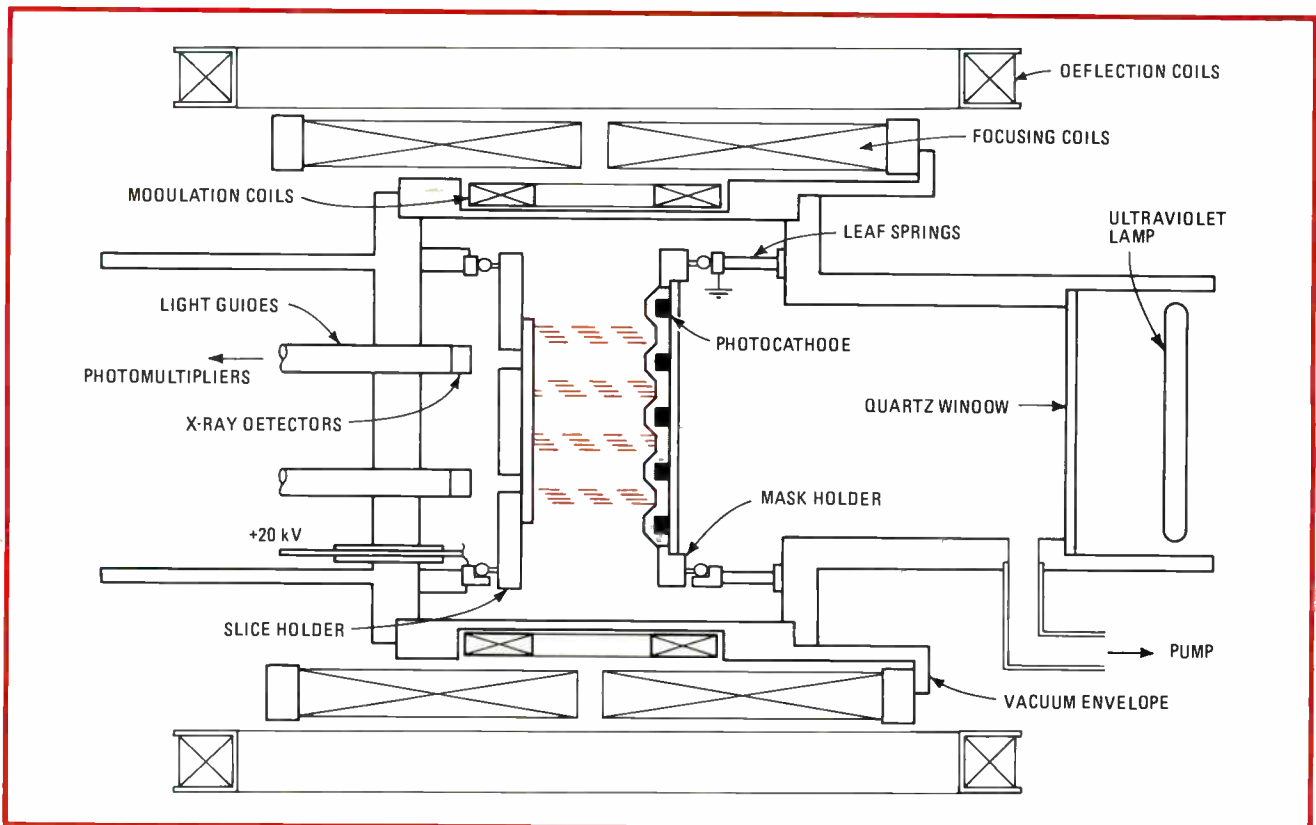
In practice, resolution is limited by the effects of electron scattering from the substrate—not by the edge profile of the projected beam, as theory would have it. Two scattering effects can be distinguished (Fig. 2), one of which has a range of a few micrometers (the proximity effect) and the other, caused by backscattered electrons, which has a range of a few millimeters.

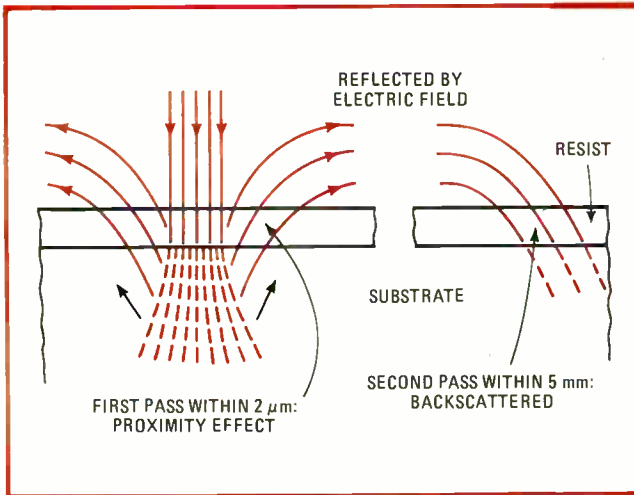
The proximity effect is well known because it occurs in scanning electron-beam systems also. In these systems, it is possible in principle to compensate by adjusting the dose at each point to allow for the contribution made by electrons scattered from neighboring points.

Although this solution is not available for the projector, there are nevertheless a number of ways in which the proximity effect may be reduced. The mask dimensions can be modified to produce a first-order correction, and multilevel resist techniques can be used to advantage. In a future development of the projector, the accelerating voltage can be increased from 20 kV to perhaps 50 kV, where the proximity effect is considerably smaller.

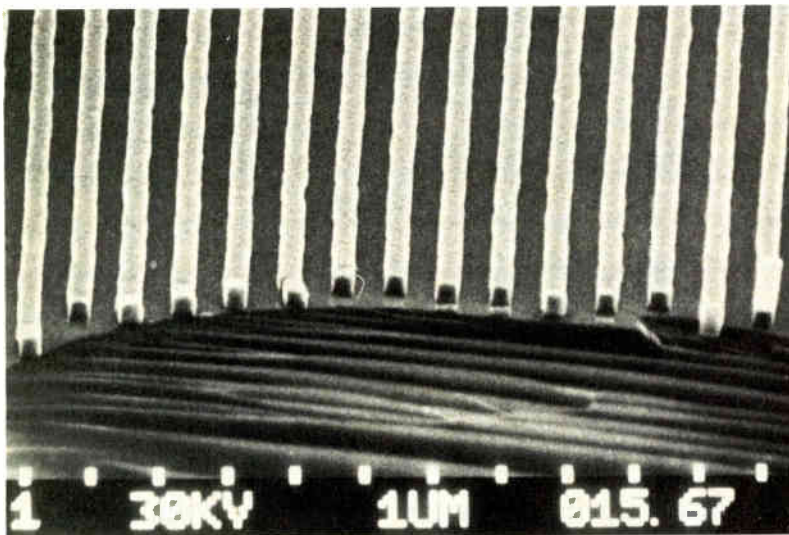
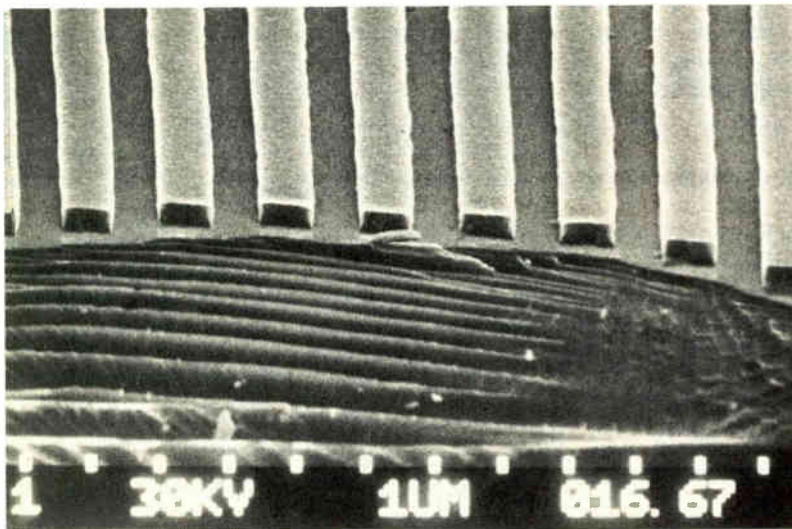
Backscattered electrons are returned to the substrate by the electric field at distances of up to 4 mm from the

1. Electron imaging. In the electron-beam image projector, a chrome-on-quartz mask coated with photoemissive cesium iodide is placed in a vacuum. UV illumination causes the unmetallized areas of the mask to emit electrons, which are accelerated onto a wafer.





2. Proximity and backscattering. The proximity effect, left, is caused by electron scattering in the resist and substrate and has a range of a few micrometers. Backscattering, right, occurs when electrons are returned to the substrate by an electric field.



3. High resolution. In these examples of the image projector's resolution, the upper view shows 0.8- μm lines and spaces in a positive resist, and the lower view displays 0.5- μm lines and spaces in a cross-linked positive resist. Note the verticality of the wall.

original image point. The effect can be serious, especially with a mask that is largely transparent. With such a mask, the circuit features are a few small opaque regions that ideally should remain completely unexposed on the wafer. But with such a large transparent area on the mask, the features on the wafer will receive a dose from electrons back-scattered from the neighboring large exposed regions.

All electrons landing within a diameter of about 8 μm around a feature will result in its undesired exposure. The effect is such that dimensional control is difficult to achieve. This situation can usually be avoided, however, because both positive and negative electron resists are available, making it unnecessary to use masks with a transparent area greater than 50%.

As the photographs in Fig. 3 show, the present version of the image projector can expose features well under a micrometer. The edges of the features are sharp, and the walls vertical, indicating that the ultimate resolution of the electron-beam projector is less than 0.1 μm .

An added bonus of working with electron projection is that the depth of focus is at least 100 μm , which can be compared with a figure of less than 5 μm for the 1:1 optical projector. Depth of focus is an important parameter because of the need to adjust to varying resist thicknesses, to cover oxide steps and to compensate for variations in the wafer's surface.

Also relevant is the fact that the edge profile for the electron projector is largely insensitive to variations in resist thickness and is hardly affected by whether the substrate is silicon or aluminum. Fig. 4 shows an example of imaging over a 1- μm oxide step. The three wider lines are 1 μm and the narrower line is 0.5 μm . The line width is very well controlled over the step, even in the submicrometer region.

It cannot be over-emphasized that the registration of a pattern with a previously defined image is at least as important in determining packing density as is the minimum achievable line width. One of the strongest points of the image projector is its fast, accurate, and fully automatic alignment system.

The system makes use of special marker areas shown in the inset in Fig. 5, which consist of coarse and fine pads with pitches of 200 μm . Two markers are defined, one on each side of the silicon wafer in a heavy metal (usually tantalum), and there is an identical pattern on each mask. The size of the alignment marks is exaggerated for clarity in the figure.

During alignment, electrons from the mask's markers strike the markers on the slice and generate X rays that are monitored with the combination of phosphor detectors, light guides, and photomultipliers shown in Fig. 1. The magnitude of

the detected signal is related to the misalignment of wafer and mask.

The alignment system is fully automated and uses deflection coils for X-Y alignment and small mechanical movements of the mask for rotation correction. It achieves magnification compensation by slightly converging or diverging the main focusing field. For the required accuracy, two stages of alignment are needed, making use of the fine and coarse patterns on the markers on the wafer and mask.

Alignment check

As a check on alignment accuracy, automatic electrical probing measurements were made on a large number of wafers, on sites close to the two markers. The total spread of results was only 0.1 μm in X-Y, rotation, and magnification alignments.

With this system for a single global alignment, care must be taken to control image distortion so that the patterns are registered over the whole slice and not just at the two marker sites. There are three main contributions to image distortion: inhomogeneity in the focusing and deflection magnetic fields, edge effects at the periphery of the mask and slice holders, and process-induced distortion, notably slice bow (mechanical distortion of the wafer).

Any transverse magnetic field will deflect electrons sideways; if the focusing field is inhomogeneous, there will be varying components of a transverse field over the wafer, resulting in distortion. With proper design and the

exclusion of all ferromagnetic materials, a magnetic-field uniformity of a few parts in 10^5 is readily achieved for the focusing magnet. This uniformity gives rise to image distortion that is below 0.1 μm . Similarly, there is no real problem with achieving adequate uniformity for the deflection fields.

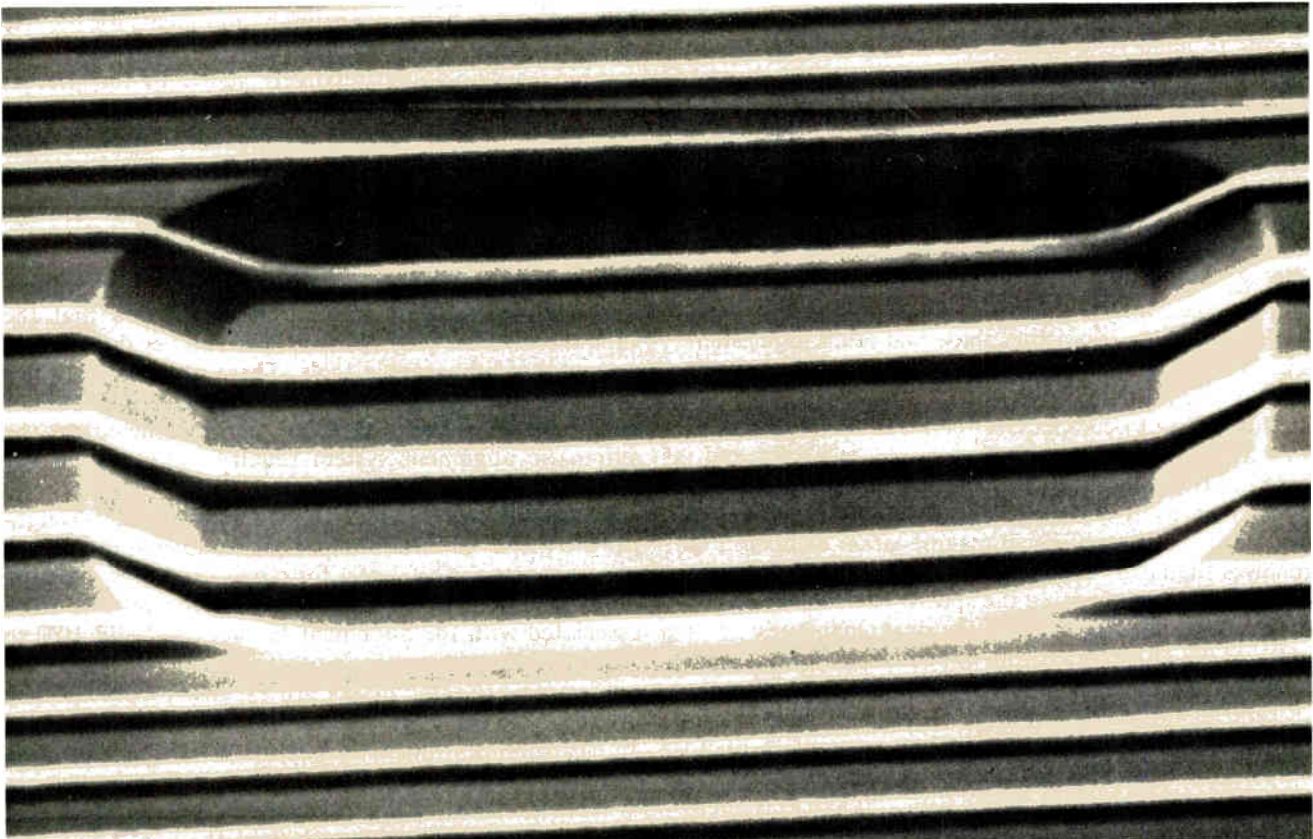
The silicon wafer forming the anode of the system inevitably has some kind of discontinuity at its edge, which distorts the electric field and hence the image. This distortion cannot be eliminated—but it can be made the same for all exposures, which is all that is necessary. To put it another way, it is the variation in distortion that is important and not the absolute value.

One effective way to keep the distortion uniform is to clamp the wafer onto a large flat surface. The distortion is caused by the step down from the wafer to this back-plane, but it is now a property of the slice and is carried with it through the subsequent processing steps.

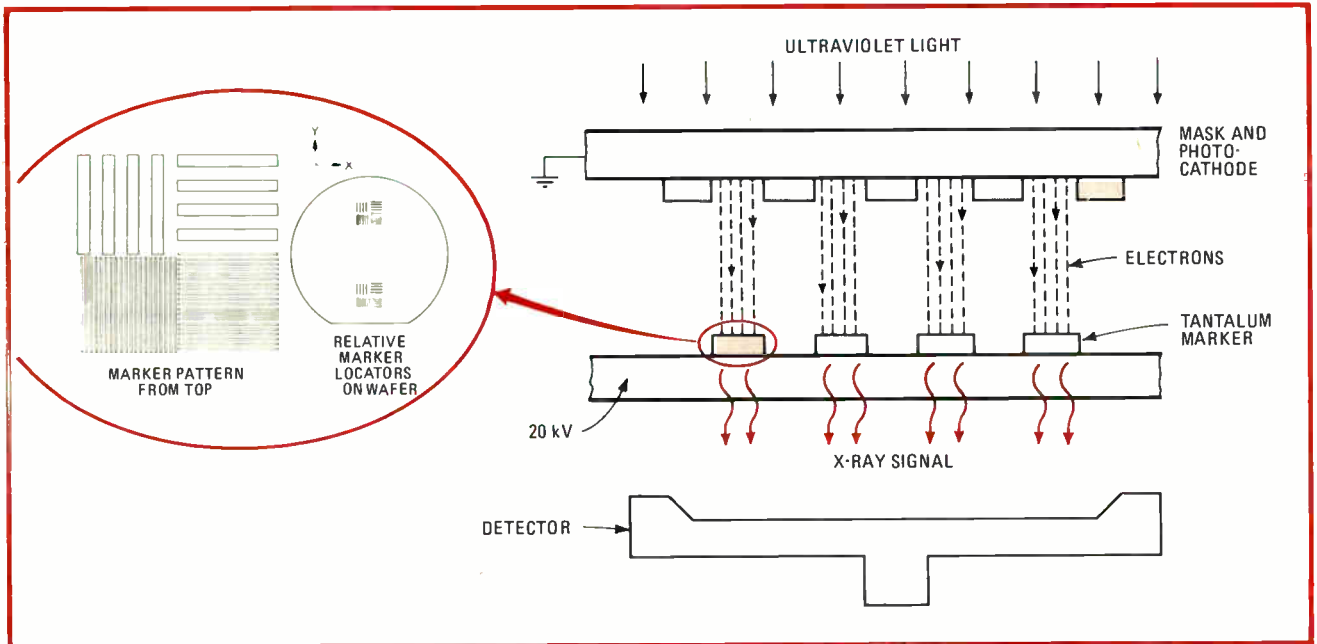
Stress compensation

Processing of silicon by oxidation, diffusion, or deposition of layers results in a surface with varying degrees of stress. Since the front and back of the wafer in general have different stresses, the wafer bows. More importantly, the bow changes from step to step in the processing, introducing different distortion patterns.

Problems with such a slice bow are usually dealt with in optical systems by using a vacuum chuck to clamp the wafers flat. This solution is not available for the image projector because the wafer is already in a vacuum. The



4. Stepped on. The edge profile of the electron-beam projector is largely insensitive to variations in resist thickness because the unit has no great depth of focus. In this view, 1- and 0.5- μm lines have been imaged over a 1- μm step with well-controlled line widths.



5. X-ray alignment. The magnitude of an X-ray signal proportional to mask-to-wafer misalignment is used to drive the image projector's automatic alignment servomechanism. This signal is generated by X-ray emission caused by electrons striking tantalum markers (see inset).

solution is an electrostatic chuck, in which the wafer is flattened by the force that exists between two charged conductors separated by an insulator.

Figure 6 shows the principle of the chuck; the wafer forms one electrode and the backplane the other. With an insulator thickness of 200 μm and a potential difference of 3 kV, the force holding the wafer down corresponds to about 0.2 atmosphere. An incidental advantage of the chuck is that the added thermal mass helps to stabilize the wafer temperature during exposure.

A criticism often leveled in the past at whole-wafer exposure systems is their inability to deal with random in-plane distortion believed to occur during slice processing such as oxidation, diffusion and ion implantation. Recent measurements have shown, however, that this kind of process-induced distortion is linear not random—that is, the wafer's diameter changes. Electron-beam image projection overcomes these and other dimensional changes by slightly correcting the magnification during the alignment phase.

This ability to compensate for magnification errors is an extremely important feature of the projector and is not readily achieved in other whole-slice projection systems, such as X-ray or 1:1 optical printing. It should also be noted that effective magnification compensation removes the need for strict temperature control of wafer or mask, thus eliminating the special environmental conditions demanded by many of the rival techniques.

Since the alignment of the image takes a few seconds, it is convenient to combine it with the exposure step, thereby avoiding the necessity of separately illuminating the marker areas. A typical current density is 5 microamperes per square centimeter, which only requires resists with sensitivity between, say, 100 and 200 microcoulombs/cm². This modest sensitivity requirement gives the freedom to optimize the resist for other desirable properties, such as resolution, etch resistance, or devel-

opment tolerance. Suitable positive resists are the well-known polymethyl methacrylate or a cross-linking methacrylate. Polystyrene and polymethyl-cyclo-siloxane are suitable negative resists.

Exposure times with the projector are a fraction of a minute. The machine must, of course, be evacuated between cycles, but the vacuum requirements for the CsI photocathode are very modest (5×10^{-5} torr) and so the pumping cycle can be relatively short. In the present laboratory model, it has proved possible to expose twenty-five 4-in. wafers per hour. Cassette loading and vacuum interlocks would achieve considerably higher throughputs.

The cost picture

Although a machine specifically designed for production has not yet been built, it is anticipated that the capital cost of the projector will be no higher than that of present-day lithographic tools. There are relatively few precision parts and no laser-controlled X-Y tables or hand-finished lenses. Machine control including the automatic alignment system requires only a modestly priced microcomputer system.

Processing costs, yields, packing density, and throughput are the other factors that must be taken into account in arriving at the total cost for circuits made by electron projection. The best estimate is that the process steps associated with the alignment markers will add 10% to 15% to usual MOS processing costs.

Electron projector masks are expensive because they are the same size as the final image, requiring the use of an electron-beam mask maker and elaborate inspection techniques. On the other hand, mask and wafer are not in contact, and mask life is consequently long. Mask cost should account for less than 10% of the final processed-wafer cost, according to estimates.

It is not possible at the present research stage to make

very definite statements about the yield, but it can be assumed that it will be limited largely by mask defects—provided the design rules are chosen to lie well within the alignment and resolution limitations of the equipment. This situation is not very different from that of present-day optical projection lithography, except that the electron image projector does require a photocathode, which may be expected to have some imperfections. The R&D evidence so far suggests that this will not be a significant problem. The remaining factors, namely packing density and throughput, have already been shown to be on the credit side.

The competition

Great progress has been made in recent years in photolithography, and conventional contact printing is now being replaced by 1:1 optical projection printing and step-and-repeat systems for large-scale integration and VLSI. The 1:1 machines have very high throughput and adequate alignment, but only modest resolution (about 2 μm) and, as noted previously, limited depth of focus. Some improvement in resolution may be realized by using shorter wavelengths, but this will increase the cost of the optics and aggravate problems with depth of focus. It is unlikely that feature sizes much below 1.5 μm will be replicated with this technique.

Step-and-repeat optical systems are capable of resolving smaller dimensions than the projection printers because they use reduction printing in which mask features are typically 5 to 10 times larger than the final-image features. The depth of focus is still small, but the image may be refocused for each chip, and chip-by-chip alignment is possible. The masks are much easier to make than same-size masks, and they can be inspected and even repaired to reduce defect levels. On the negative side, optical steppers require precision X-Y tables and hand-finished lenses, both of which contribute to a high capital cost. It looks increasingly likely that wafer steppers will find a place in the manufacture of ICs with dimensions between 1 and 2 μm .

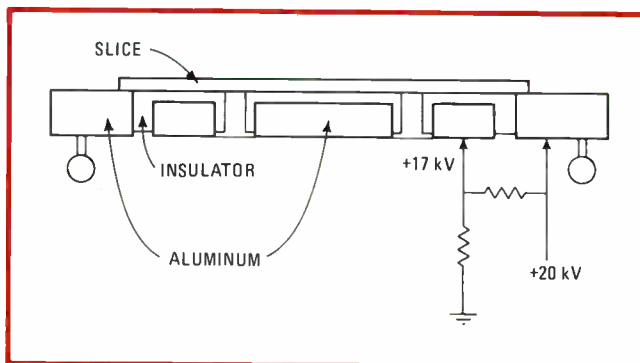
Advanced technologies

A great deal of R&D effort has been directed towards perfecting X-ray lithography. The attraction of this technique is its resolution capability and the simplicity of the basic system in which soft X-rays are used in a proximity mode of contact printing.

However, in place of the stable glass or quartz substrates used for optical and electron image-projector masks, X-ray lithography requires substrates consisting of membranes only a few micrometers thick. Stability of such masks is very difficult to achieve and, although great progress has been made, mask sets for large-diameter wafers present formidable problems.

A number of alignment techniques have been researched, but no reliable automatic system with adequate pull-in range has yet emerged. High throughput has also been difficult to achieve, and most prototype equipment that has been disclosed can expose less than 10 wafers an hour.

The other important lithographic technique for the near future is the electron-beam pattern generator. Basi-



6. Electrostatically chucked. In the electrostatic chuck, the wafer is held flat by the electrostatic force between two conductors separated by an insulator. The wafer is one electrode and the aluminum backplane is the other. Holding force is about 0.02 atmospheres.

cally an adaptation of the scanning electron microscope, it deflects a finely focused beam of electrons under computer control to draw a pattern in an electron-sensitive resist. The pattern specification resides in the computer memory as a list of coordinates that can be readily altered or adjusted. Such machines are in use for mask making and are beginning to be used for writing directly on the wafer.

Resolution and pattern registration are basically trouble-free, although it must be remembered that there still are proximity-effect problems. The only real question is whether this mode of serial writing can ever be made fast enough to be economic. To give some idea of the task ahead, it is estimated that a direct-writing machine would need a throughput about 100 times the present-day mask-maker versions to be economical for the mass production of ICs.

Researchers in this field have made progress towards this goal by introducing the concept of variably shaped beam systems, as discussed in the previous article. Instead of scanning every element in the pattern with a finely focused spot beam, rectangles of varying sizes up to 5 μm , typically, square can be exposed in a single shot. A considerable amount of R&D effort is required before the design of a commercially available variable beam machine is optimized.

Future trends

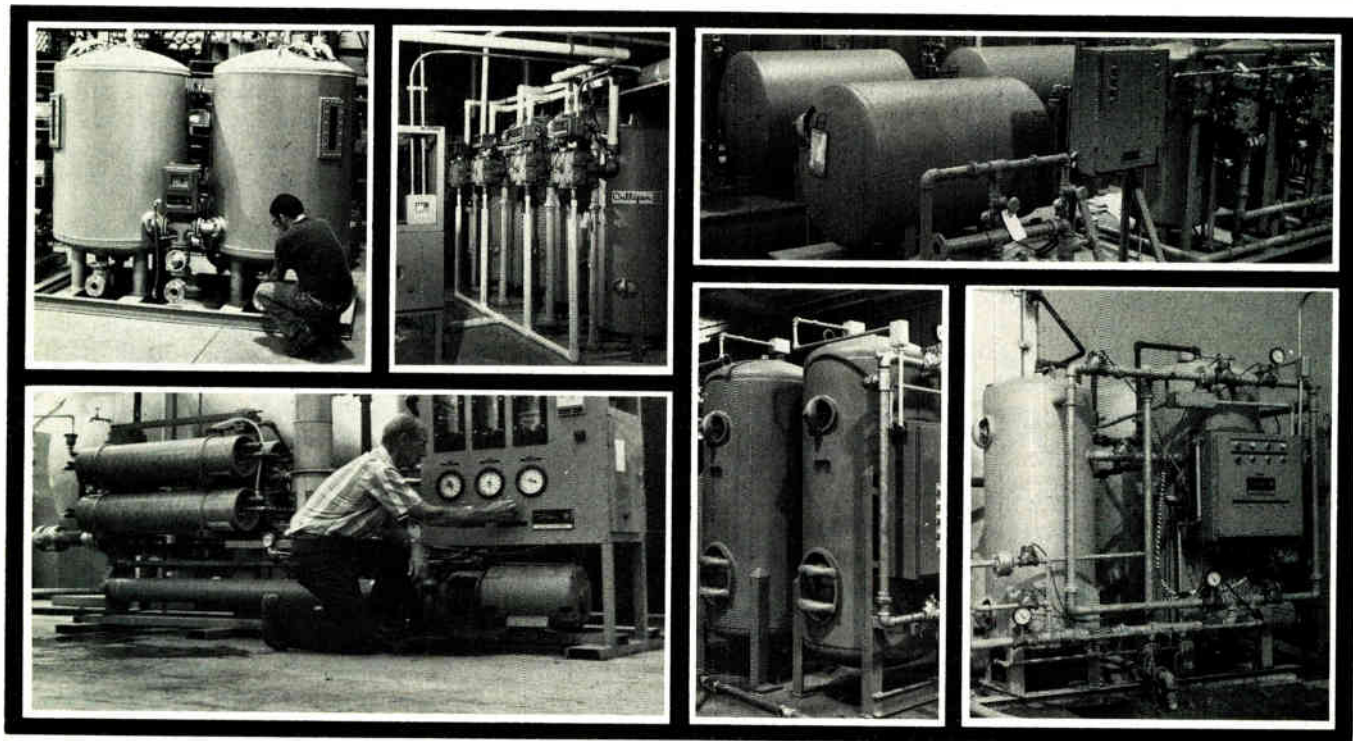
Electron image projection is currently a promising technique for the lithography of VLSI circuits with sub-micrometer dimensions. Its area of application is volume production; specialized low-volume circuits where cost is not the overriding consideration will be made by direct-writing machines.

The scanning electron-beam system will widen its area of application as higher throughputs are achieved. It is too early to predict whether the speed can be improved sufficiently for the technique to become economically viable for volume production.

X-ray lithography has already found application in the lithography of single-mask circuits like acoustic-wave filters and bubble devices where resolution is of prime importance. The extension of the technique to more complex ICs depends on further progress with alignment systems and the mask technology. □

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Layered substrate reins in resistors' temperature drift

Strain compensates for resistivity variations of Nichrome foil to within 30 ppm up to 125°C—a tenfold improvement

by Felix Zandman, Vishay Intertechnology Inc., Resistive Systems Group, Malvern, Pa.

□ The limitations imposed by a resistor's temperature drift often frustrate the designer of analog signal-processing circuits, particularly in high-temperature applications. But the structure of a new generation of nickel-chromium foil resistors inhibits that temperature variation, banishing the worry over accuracy that accompanies the use of wirewound, thin-film, and conventional foil resistors.

The resistive foil in the HP100 series is cemented to a specially constructed ceramic substrate whose thermal expansion gives just enough strain-induced resistance change to the metal foil to cancel almost completely the metal's intrinsic resistivity variation with temperature. As a result, a resistor specified for 0.01% tolerance at 25°C can maintain that accuracy anywhere up to 125°C within 30 parts per million (0.003%), compared with almost 300 ppm for the best foil resistors previously available. With slight modifications of the technique, resistors can be optimized for even lower variations over narrower temperature ranges.

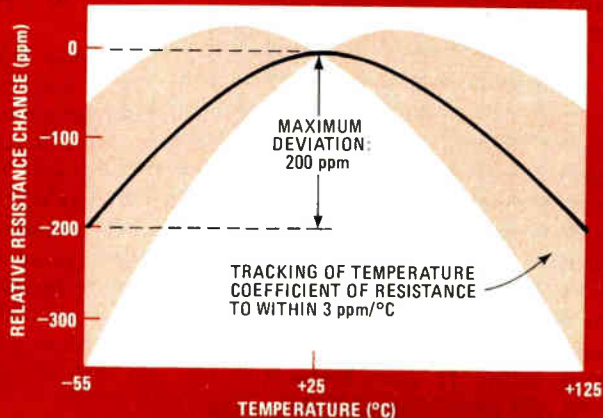
The technology will benefit all types of precision passive circuits, particularly Wheatstone bridges, ladder and summing networks, and voltage dividers in general. Instrument makers can improve accuracy by exploiting

the components' insensitivity to temperature changes, and military circuits can achieve precision at high temperatures with conventional designs.

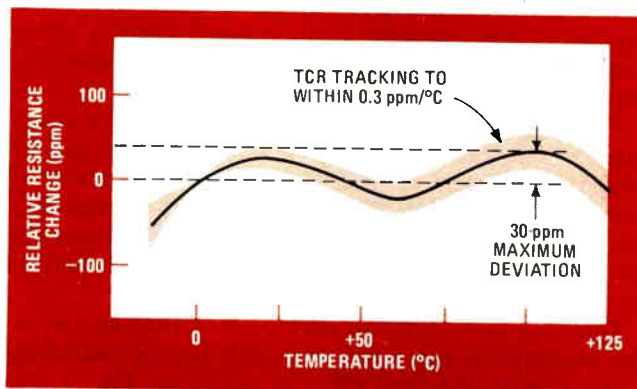
The ohmic value of the different resistive components used in electronics, like most physical quantities, is a function of temperature. Generally, the resistance increases with increasing temperature, a phenomenon that can be represented by a curve that is valid for all components made by identical technologies. Frequently, this curve can, at least in certain temperature regions, be approximated by a straight line that permits the temperature coefficient of resistance (TCR) to be expressed as the line's slope, usually given in ppm/°C.

There exists, however, as in all manufacturing, a spread of values of the TCR in mass-produced resistors. All resistors of the same family follow curves that lie between two extremes. Between two randomly chosen resistors there is a worst-case differential TCR called TCR tracking. For example, even in carefully made wirewound resistors, the temperature coefficients differ by ± 5 ppm/°C for a tracking of 10 ppm/°C. It is difficult to reduce this dispersion, especially if the resistors are unequal in value. The dispersion of TCR values results from variations in the metal used for the resistors and in residual stresses introduced during manufacture.

In 1964 Vishay devised a technology that would



1. Drifting away. The variations with temperature of the best precision resistors previously available follow these curves, with zero slope near room temperature and a maximum deviation of about 200 ppm/°C over the military range. The shaded region indicates the spread in TCRs due to variations in materials and manufacturing.



2. Self-correcting. The new-generation low-temperature-drift resistors are never more than 30 ppm away from their specified value over the range from 0° to 125°C. Strain-induced resistance changes compensate for the metal foil's resistivity variations in such a way as to give the oscillations shown. Below 0°C, the characteristics are similar to those of previous components, as illustrated in Fig. 1.

improve the TCR. It provides for a thin layer of photoetched metal foil that is cemented to a ceramic substrate to form the resistive circuit. The metal is a nickel-chromium alloy containing traces of other metals that modify its resistive properties. By a judicious choice of impurities, then, different thermal and electrical properties can be designed in.

The resistance of an individual component made according to this method varies with temperature mainly because of two phenomena: intrinsic resistivity changes in the metal and strain in the foil. Under a temperature change the metal foil is subjected to strain because the ceramic substrate has a different coefficient of thermal expansion from the resistive foil. The change in resistance is proportional to the strain, which in turn is proportional to the change in temperature.

In foil resistors the nickel-chromium alloy has a nonlinear resistivity versus temperature variation, whereas the strain versus temperature variation is linear. The net result of these two effects is a resistance versus temperature curve with a reasonably flat slope over a limited temperature range. Usually the resistor composition is adjusted to give a flat slope at room temperature. For Vishay resistors, therefore, the TCR obtained in this manner will be $-1.8 \text{ ppm}/^\circ\text{C}$ between $+25^\circ$ and $+125^\circ\text{C}$ and $+2.2 \text{ ppm}/^\circ\text{C}$ between $+25^\circ$ and -55°C , with a tracking of $3 \text{ ppm}/^\circ\text{C}$ (Fig. 1).

Though this resistor represents a significant improvement in TCR over wirewound and evaporated-film resistors, there is room for improvement in its performance around 100°C , where many aircraft and military products operate. In fact, as Fig. 1 shows, a precision resistor with an initial tolerance of 0.01% at 25°C would at $+125^\circ\text{C}$ have a tolerance of 0.043%, more than four times the error specified at room temperature.

Layered substrate

To produce more symmetry between the two, either the resistivity versus temperature curve must be linearized or the strain versus temperature curve be made nonlinear. Unfortunately, essentially all substrates used for precision resistors have linear coefficients of thermal expansion, and essentially all nickel-chromium alloys used as the resistive material have nonlinear resistivity variations as a function of temperature.

However, with the use of a layered sandwich structure, a nonlinear expansion versus temperature can be produced at certain of its surfaces. The proper choices of material and structure for the substrate and for the foil's composition can cause the strain at the surface where the foil is located to vary nonlinearly in an almost perfect mirror-image of the resistivity's variations.

Due to slightly different curvatures in the two curves, the net result is not a true zero TCR but an oscillating curve around the zero line, as shown in Fig. 2. As temperature changes cause the resistance to drift from the desired value, the corrective strain factors reverse the direction of change to restore the resistance toward its initial value. The changing temperature, which normally increases the error, instead reverses the temperature-induced error by activating the self-compensating nonlinear strain mechanisms that provide thermal stability.

PERFORMANCE OF HP100A FOIL RESISTORS

Characteristics	Values
Resistance range	100 Ω to 100 k Ω
Temperature coefficient of resistance (0°–125°C)	< 1 ppm/°C
Tolerance at 25°C	$\pm 0.005\%$ to $\pm 1.0\%$
Absolute tolerance variation (0°–125°C)	30 ppm
Power dissipation	0.3 W
Load-life stability: maximum change in resistance after 2,000 hours at 70°C and 0.3-W dissipation	0.02%
Shelf-life stability: maximum change in resistance after one year and three years	5 ppm; 10 ppm
Thermal electromotive force: due to temperature difference between leads (maximum)	0.04 $\mu\text{V}/^\circ\text{C}$
due to self-heating under 0.1-W dissipation	0.2 μV
Rise time (1-k Ω resistor)	1.0 ns
Inductance (maximum and typical)	0.1 μH ; 0.08 μH
Capacitance (maximum and typical)	1.0 pF; 0.5 pF
Maximum working voltage	300 V
Voltage coefficient of resistance	< 0.001%/V
Current noise (root mean square)	< 0.025 $\mu\text{V}/\text{V}$
Hermeticity	10^{-7} atmospheric cc/s

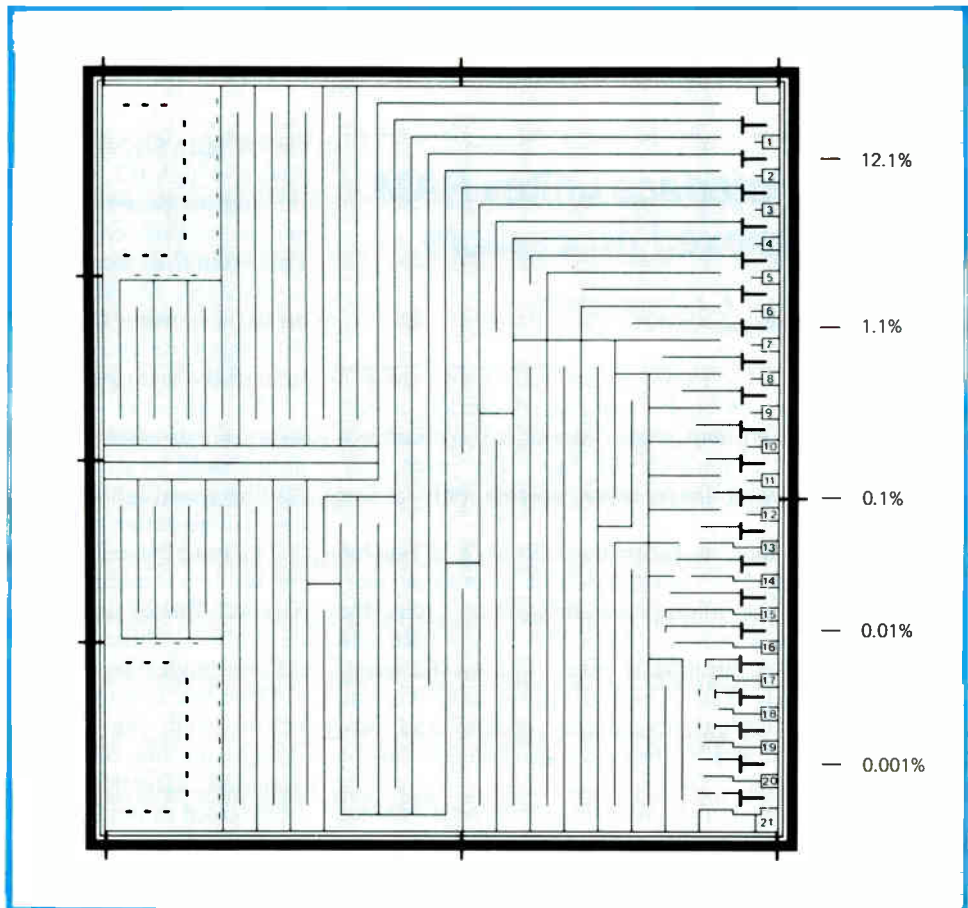
This technique keeps the resistance constant to within 30 ppm between 0° and $+125^\circ\text{C}$. These HP100A resistors can therefore maintain their initial tolerance of 0.01%, regardless of temperature, to within 30 ppm. At worst, the tolerance is degraded to 0.013%, which marks a threefold improvement. The spread in TCRs due to nonuniform materials and manufacturing processes is $\pm 15 \text{ ppm}$ at $+125^\circ\text{C}$. The TCRs of two regular metal-foil resistors might be approximately 300 ppm apart; with the new technology they will be only 30 ppm apart—an order of magnitude improvement.

In the region 0° to -55°C , however, the resistor loses its self-correcting properties and its TCR becomes $+2 \text{ ppm}/^\circ\text{C}$, similar to its predecessors'. Close examination of the resistance versus temperature curve in the region around room temperature ($+15^\circ$ to $+45^\circ\text{C}$) reveals that the improvement here over Vishay's past technology is not very significant. Since precision instruments are usually exposed to temperatures close to $+25^\circ\text{C}$, an attempt was made to optimize the techniques for a reduced range of temperatures. The HP100D resistor was thus developed, which has resistances constant within 10 ppm between $+15^\circ$ and $+45^\circ\text{C}$ and TCRs of $2 \text{ ppm}/^\circ\text{C}$ outside this range.

Stable structures

The resistor element is flat and about the same size and aspect as other metal-foil resistors and is encased in a hermetically sealed can to assure long-term stability. The photoetched pattern (Fig. 3) is designed for low inductance and capacitance—0.1 microhenry and 0.5

3. Trimming maze. This photoetching pattern for a 500-ohm foil resistor reveals complex current paths connecting the bonding pads at left. (The solid black lines represent etched regions with no metal.) Resistor values are trimmed by removing metal from the regions at the base of the T-shaped cuts along the right edge; current is then forced along a longer path, raising the resistance in precise steps. In addition, the resolution that is associated with selected trimming points is shown.



picofarad respectively. The performance characteristics of the HP100A resistors are shown in the table on the opposite page. The thermal electromotive force due to temperature differences between the leads is typically 0.04 microvolt/°C; during heating under an applied power of 0.1 watt, it is 0.2 μ V. Other characteristics are similar to those of the classic foil resistor.

Power sharing

These resistors will be key where TCR tracking is essential, as in voltage dividers, ladder networks, summation networks, and Wheatstone bridges. When, for example, two resistors in the ratio 1:10 are subjected to a current giving a power of 0.1 W in the larger resistor, the temperature of the resistive element in a $\frac{1}{4}$ -W resistor subjected to this power will rise about 9°C. The temperature difference between the two resistors will be approximately 8°C, because one resistor will dissipate 0.1 W and the other only 0.01 W. Further, if the pair of resistors is subjected to an ambient temperature rise of 30°C, from +15° to +45°C, the HP100D metal-foil resistors are a marked improvement not only over thin-film resistors with TCRs of 25 ppm/°C, but even over standard 2-ppm/°C foil resistors.

The TCR tracking in the film and conventional foil types might be the same and equal to 1 ppm/°C. But in the film resistors the ratio will change by altogether 230 ppm—the power inequality contributes 8°C \times 25 ppm/°C, or 200 ppm, and the temperature tracking of one resistor with respect to the other supplies the

remaining 30 ppm. Similarly, in the standard foil resistors, the ratio will change a total of 46 ppm. In spite of the same TCR tracking for both resistors, the foil resistors will exhibit a performance five times better than the thin metal film because of their low absolute TCR.

The resistance changes in the pair of HP100D resistors due to the power inequality will be negligible. About 10 ppm will be the change due to TCR tracking. The improvement over the classic metal-foil resistor is almost fivefold; over the evaporated-metal films the increase in accuracy is more like twentyfold.

Temperature gradients

Nevertheless, problems can crop up even if the resistance ratio is 1:1 and power is shared equally—in fact, even if the resistors are on the same substrate, in which case TCR tracking can be less than 1 ppm/°C. Any temperature gradient will leave its mark on the ratio stability, and often the effect of the TCR tracking will be significantly smaller in comparison.

Temperature gradients come from a number of sources—not only from power asymmetry, but also from hot air circulation inside an instrument, provoked by power dissipation from other components; from an instrument's exposure to external heat sources like sunlight; and from unequal heat dissipation inside the resistors due to such structural variations as their location inside the molding or the molding's thickness. Thus, close TCR tracking must be accompanied by low absolute TCRs as well. The new resistors achieve both. □

Low-cost interface unites RAM with multiplexed processors

by G. Aravanan and U. K. Kalyanaramudu
Bharat Electronics Ltd., Bangalore, India

This simple interface hooks a standard random-access memory directly, without using latches, to a microprocessor that has a multiplexed bus. The nine-gate, one-flip-flop array is inexpensive, costing only a few dollars.

General Telephone & Electronics' 8114-2, a 1-K-by-8-bit RAM, is joined to an Intel 8085A microprocessor. At the start of the microprocessor's write cycle, the 8085's address-latch-enable (ALE) line moves high and the 74LS74 D-type flip-flop is reset. The RAM's write-enable (\overline{WE}) line is then activated via OR gates G_2 and G_3 when the input/output memory control and bus-cycle-status (IO/\overline{M} and S_1) lines are also brought low by the processor.

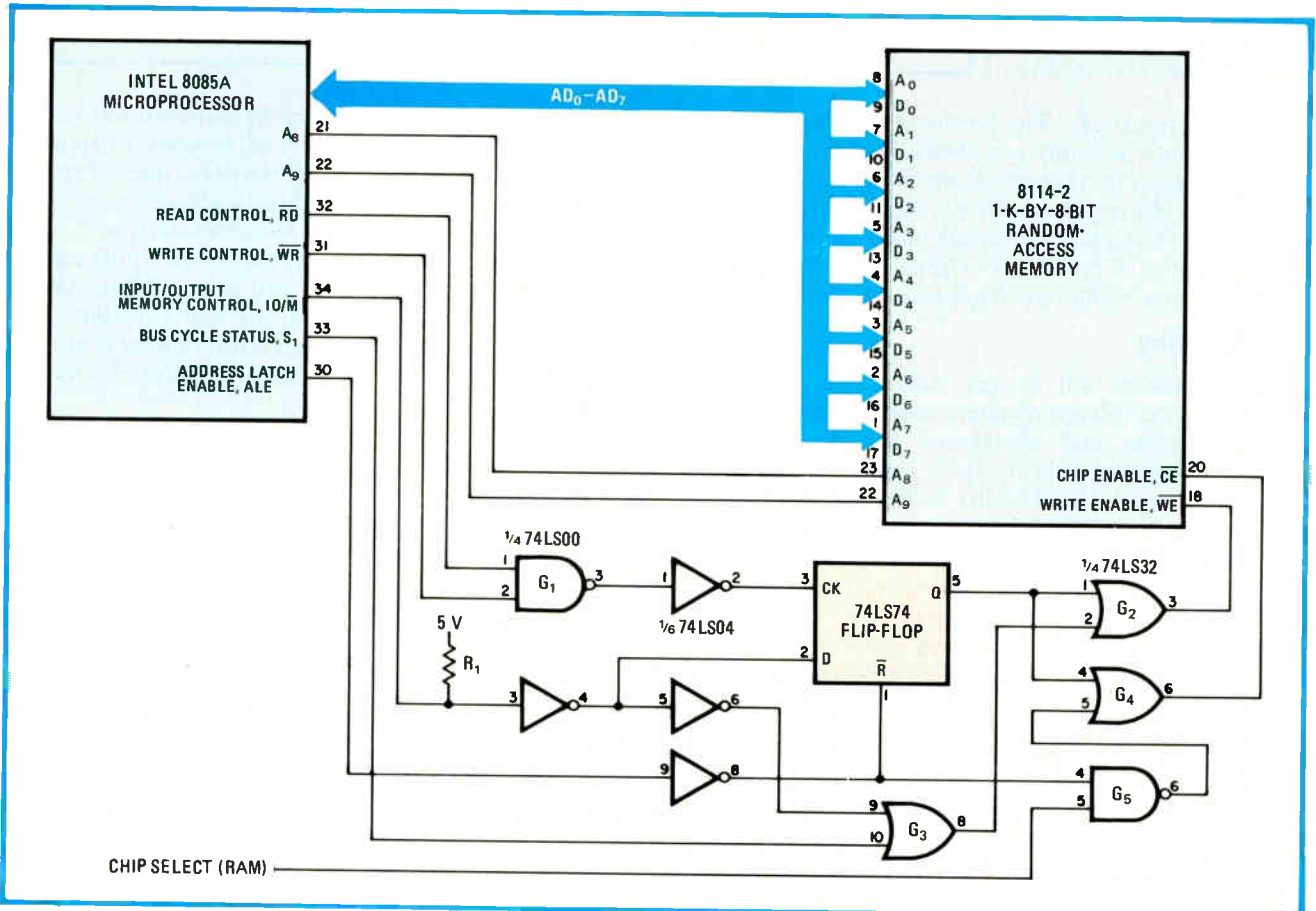
On the falling edge of the ALE line the RAM is enabled

via OR gate G_4 , given that the chip-select input for the device is high (G_5 would be low). Then the 8114 latches the address presented on lines AD_0 through AD_7 , which are tied to their corresponding address lines on the RAM. Following this, the data is transferred from the processor to the RAM. The 8085's write-control (\overline{WR}) line will then go high, causing the flip-flop to latch a high state, and thus the write cycle will terminate when the \overline{WE} and \overline{CE} lines of the RAM go high.

The address should remain on the lines for at least 100 nanoseconds after \overline{CE} line becomes active (low), and the data should be on the lines for at least 100 ns before the \overline{CE} line goes high—for at least 30 ns thereafter. The \overline{CE} line will be active in the cycle for 400 ns.

The read cycle is similar to the write cycle except that the \overline{WE} line remains high during the entire cycle interval. The ALE line of the processor initially goes high, as does its S_1 line, and the RAM's desired address is placed on the AD_0 through AD_7 output bus.

Once the ALE line falls flat, the \overline{CE} line is activated as before, and the address information, which should remain on the bus for at least 100 ns thereafter, is accepted. After 100 ns, the RAM's corresponding data is transferred to the bus and then to the processor. □



Link. A four-chip interface facilitates an easy exchange of data between processors having multiplexed data-address buses and standard random-access memories. Circuitry is simplified by tying a RAM's data and address lines together. The interface costs under \$5.

Standard C, L-input filters stabilize hf transistor amplifiers

by Ed Wetherhold
Honeywell Inc., Signal Analysis Center, Annapolis, Md.

This display updates the design table for low-pass Chebyshev filters that use standard-value capacitors [*Electronics*, June 19, 1980, p. 160]. It is based on an inductive-input configuration designed to provide the response of the capacitor configuration while stabilizing transistor amplifiers that tend to oscillate when faced with a capacitive input!. The filters may be scaled for any frequency

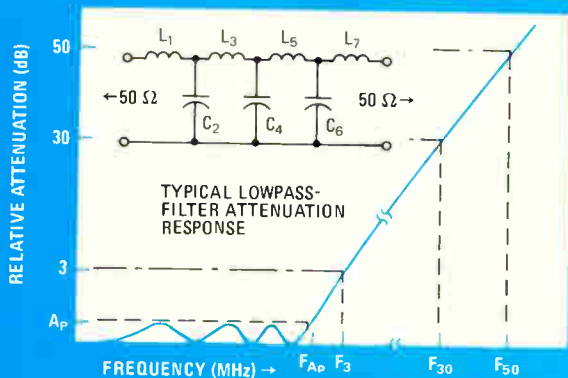
and input/output impedance that departs from their intended use in the 1-to-10-megahertz range with a 50-ohm source-load impedance; all designs yield more than 40 decibels of attenuation per octave.

Component values for these 30 seven-element designs (see table) were calculated using a simple Basic program. The passband response of all designs has equal ripple, and the reflection coefficient of the filters is less than 11% to minimize the voltage standing-wave ratio. For terminations that have an equal impedance, $L_1 = L_7$, $L_3 = L_5$, and $C_2 = C_6$.

To find the element values of a filter having an impedance level Z_x corresponding to a given frequency specification (and thus the frequencies corresponding to the equiripple point, A_p , and the 3-, 30-, and 50-dB attenuation points), the user must:

50-OHM LOWPASS CHEBYSHEV FILTERS WITH INDUCTIVE INPUT/OUTPUT

Filter No.	Frequency (MHz)				Reflection coefficient (%)	$C_{2,6}$ (pF)	C_4 (pF)	$L_{1,7}$ (μH)	$L_{3,5}$ (μH)
	A_p dB	3 dB	30 dB	50 dB					
1	0.921	1.08	1.50	1.98	3.57	4,700	5,600	6.33	14.58
2	1.014	1.18	1.63	2.15	3.89	4,300	5,100	5.89	13.37
3	1.087	1.29	1.81	2.40	2.88	3,900	4,700	5.06	12.04
4	1.197	1.41	1.96	2.58	3.41	3,600	4,300	4.81	11.15
5	1.065	1.45	2.14	2.88	0.61	3,300	4,300	3.59	10.35
6	1.328	1.54	2.12	2.80	4.16	3,300	3,900	4.58	10.29
7	1.179	1.60	2.35	3.16	0.64	3,000	3,900	3.28	9.40
8	1.425	1.68	2.35	3.11	3.12	3,000	3,600	3.95	9.27
9	1.528	1.86	2.63	3.49	2.21	2,700	3,300	3.36	8.32
10	1.634	2.06	2.96	3.95	1.43	2,400	3,000	2.83	7.41
11	1.906	2.07	2.75	3.57	10.65	2,400	2,700	4.31	8.19
12	1.859	2.27	3.22	4.28	2.04	2,200	2,700	2.71	6.78
13	2.137	2.53	3.53	4.66	3.12	2,000	2,400	2.63	6.18
14	2.291	2.78	3.94	5.23	2.21	1,800	2,200	2.24	5.54
15	2.452	3.09	4.44	5.92	1.43	1,600	2,000	1.89	4.94
16	2.859	3.11	4.13	5.36	10.65	1,600	1,800	2.88	5.46
17	2.849	3.37	4.71	6.22	3.12	1,500	1,800	1.97	4.64
18	3.126	3.84	5.46	7.26	1.93	1,300	1,600	1.59	4.00
19	3.475	3.90	5.29	6.91	6.53	1,300	1,500	2.00	4.17
20	3.269	4.12	5.92	7.89	1.43	1,200	1,500	1.41	3.70
21	3.985	4.61	6.37	8.39	4.16	1,100	1,300	1.53	3.43
22	3.538	4.80	7.06	9.49	0.64	1,000	1,300	1.09	3.13
23	4.274	5.05	7.06	9.33	3.12	1,000	1,200	1.32	3.09
24	4.633	5.53	7.78	10.29	2.72	910	1,100	1.17	2.81
25	5.053	6.12	8.64	11.47	2.30	820	1,000	1.03	2.53
26	5.581	6.70	9.44	12.51	2.54	750	910	.954	2.31
27	6.229	7.41	10.40	13.76	2.85	680	820	.881	2.10
28	6.791	8.12	11.41	15.11	2.68	620	750	.796	1.91
29	7.463	8.97	12.65	16.76	2.50	560	680	.711	1.73
30	8.176	9.85	13.89	18.41	2.44	510	620	.645	1.57



- Calculate the scaled impedance factor, $R = Z_x/50$.
- Calculate the 3-dB cutoff frequency of a 50-Ω filter from $F_3^{50} = R \times F_3$, dividing Z_x by 10^n , where $n = 1, 2, \dots$ if necessary to ensure that $F_3^{50} < 10$ MHz.
- Select from the table the design closest to that meeting the calculated F_3^{50} value. The tabulated values of C will be used in the new design, and the L values scaled.
- Calculate the exact value of $F_3' = F_3^{50}/R$, where F_3^{50} is the tabulated 3-dB frequency. In a similar manner, calculate the A_p , 30-, and 50-dB frequencies.
- Calculate the new L values for the desired termination impedance from $L = R^2 \times L_{50}$.

Consider a design example where $F_3' = 6.0$ MHz and

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$Z_x = 75 \Omega$. Then $R = 75/50 = 1.5$, and $R^2 = 2.25$. Therefore, $F_3^{30} = 1.5(6) = 9.0$ MHz. Filter No. 29 is selected because its F_3^{30} value is closest to the desired value. Thus $C_2 = C_6 = 560$ picofarads, and $C_4 = 680$ pF. Inductors $L_1 = L_7 = R^2(0.711) = 1.60$ microhenrys, and $L_3 = L_5 = R^2(1.73) = 3.89 \mu\text{H}$. The inductors will usually have nonstandard values, but this is no problem because any inductor may be conveniently hand-wound using iron-powdered cores that are commercially available. The exact f_A , and the 3-, 30-, and 50-dB frequencies are 4.98, 5.98, 8.43, and 11.17 MHz, respectively.

Although the design table addresses filters operating only in the 1-through-10-MHz decade, it is easy to scale

the filter data for other frequencies. For example, the 10-to-100-MHz and 100-to-1,000-MHz decades may be derived simply by multiplying the frequency by 10 or 100, respectively, and dividing all C and L values by that same number. Similarly, for the 1-to-10-kilohertz, 10-to-100-kHz, and 100-to-1,000-kHz decades, the frequency should be divided by 1,000, 100, or 10, and the component values multiplied by the same number. □

References

1. R. Jack Frost, "Large-scale S parameters help analyze stability," *Electronic Design*, May 24, 1980, pp. 93-98.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$75 for each item published.

Continuity tester buzzes out breadboards's flaws

by Douglas Holberg

Texas Micro Engineering Inc., Austin, Texas

A continuity tester with a buzzer for performing breadboard checks is probably the least exotic but most needed tool in the lab. However, the performance of many buzz boxes falls short in a few areas, especially for checking boards with active components. This device, which uses two CA3096 transistor arrays, nine resistors, and one ceramic resonator, does not.

Ideally a continuity tester should draw no current when probes are open-circuited, draw low current through the probes when continuity is established, have no on-off switch, have a low-threshold sense resistance (100 ohms or less), disregard a silicon diode's pn junction as a valid response for continuity, and be compact or have a minimal amount of circuitry to increase reliability and reduce cost. This simple-to-build continuity tester

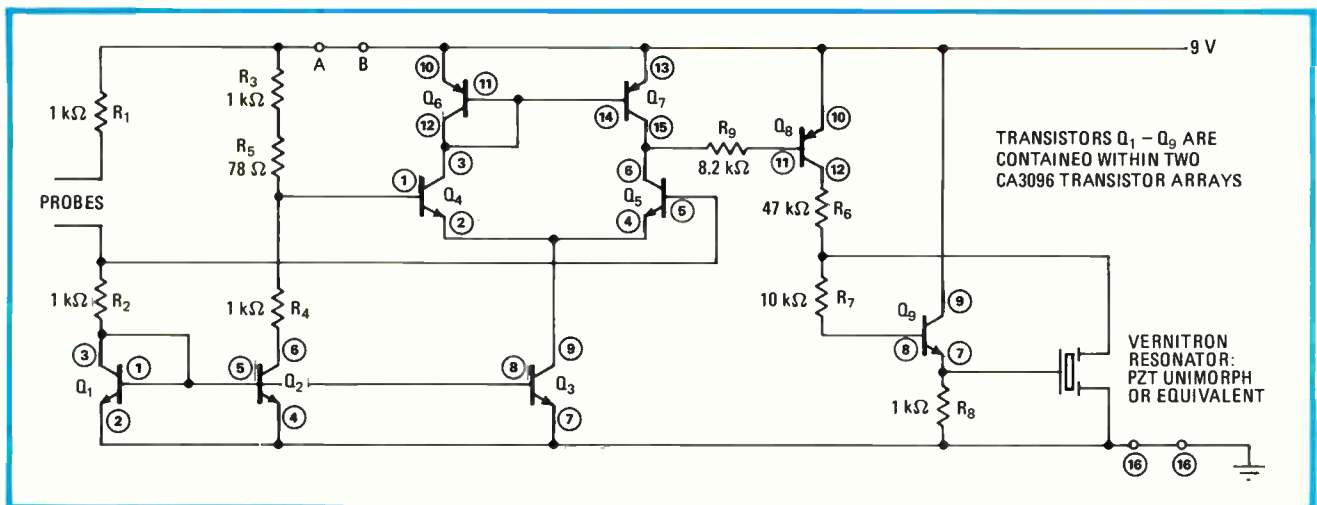
has all of these desired characteristics.

Nine of the ten available transistors in the CA3096s are used and wired with the pins of the first device designated within color-coded circles. The wiring pins of the second device are indicated by gray circles.

Transistors Q_1 and Q_2 with resistors R_1 through R_5 form a bridge circuit that becomes active when current is allowed to pass through the probes. Q_1 provides bias for Q_2 and Q_3 , with Q_3 providing the tail current for transistors Q_4 through Q_7 that comprise a differential amplifier. When the probes are open, Q_1 turns off, as does the remaining slaved circuitry. Thus, there is no current flow from the battery.

When the measured resistance across the probes becomes less than the value of R_5 (assuming a zero offset voltage in the differential amplifier), the output transistor, Q_8 , turns on. Operating current to the oscillator circuit Q_9 , R_6 , R_7 , and R_8 is then applied and the ceramic resonator will sound at a fundamental frequency of about 2 kilohertz.

The circuit draws about 18 milliamperes when sensing. About 4 mA flows through the probe when continuity is established. The probe current may be reduced by placing a low-value resistor between points A and B. □



Check it out. A two-chip continuity checker for bench-testing breadboards has a low-threshold sense resistance and will not falsely indicate upon sensing pn diodes in the circuit under test. An oscillator in the tester resonates at 2 kHz. The circuit draws a maximum of 18 mA in operation, with only 4 mA flowing through the probe tips when continuity is established.

Corrosion proofing extends battery life

By eliminating three failure modes of existing lithium and sulphur dioxide battery cells, Sandia National Laboratories of Albuquerque, N. M., has extended cell life from 18 months to five years. The 3-v battery, which is now undergoing long-term testing, looks like an ordinary 1.5-v D cell but has capacity of 8 to 9 Ah, about a tenfold increase. The failures of the original battery involved corrosion of three elements: glass in the glass-to-metal seal, tantalum used as the positive lead pin, and lithium at the anode-to-can contact.

Sandia researchers developed a new glass with about 20% less silica and significantly more alumina than the original glass, reducing corrosion by a factor of 1,000. Corrosion-resistant molybdenum was substituted for tantalum in the cathode pin. Corrosion of the lithium at the anode-to-can contact was eliminated by enclosing a nickel grid within the lithium, forming a new anode that prevents direct contact of the electrolyte with the lithium-nickel interface.

How to add test bars to ICs

The growing drive for quality and reliability has emphasized the importance of test structures or test bars to both the integrated-circuit designer and the IC fabrication process. Two developmental microelectronic test patterns have been assembled by the National Bureau of Standards' Electron Devices division. NBS-12 addresses geometric design considerations for cross-bridge sheet-resistor test structures. NBS-24 contains a variety of preliminary designs for the integrated gated-diode electrometer and a series of variations on the design of the MOS field-effect-transistor dc profiler. A report entitled Microelectronic Test Patterns, NBS-12 and NBS-24, is available for \$6.50 prepaid from the National Technical Information Service, Springfield, Va. 22161. Order by PB No. 81-214892.

Boards mimic computer uses

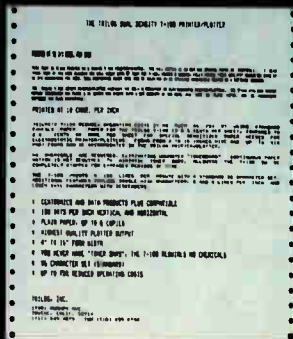
Training engineers to apply popular small computers like the TRS80, Pet or Apple to real-time monitoring and control may be an easier task, thanks to some useful application models and low-cost interfaces from Feedback Inc. These units provide hands-on experience for students of real-time computer applications. Feedback's system consists of a range of application models on 9-by-12-in. boards with separate dedicated interfaces for each computer type. A typical model, the MIC 954, shows how to control a four-phase stepper with a microcomputer. Other models simulate an automatic washing machine, closed-loop temperature control, and a microprocessor-controlled traffic controller. For more information, contact M. J. Lawson by letter at 620 Springfield Ave., Berkeley Heights, N. J. 07922 or by telephone on (201) 464-5181.

Booklet pins down pc-board trends

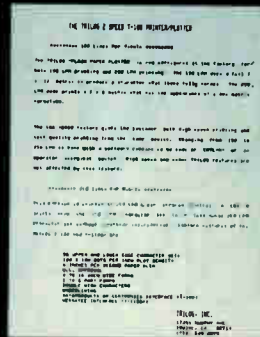
Designers of high-density printed-circuit boards may be interested in a thorough new booklet from DuPont Co.'s Riston Products division entitled "Designing High-Density Printed-Circuit Boards Cost-Effectively." Covered in the 18-page pamphlet are industry trends—spotlighting chip-carriers in case histories—basic design considerations, photo-imaging, and high-density conductor routing. For a copy, write Priscilla Tuminello, DuPont Co., Marketing Communications Department, Room N-2526-3, Wilmington, Del. 19898.

-Jerry Lyman

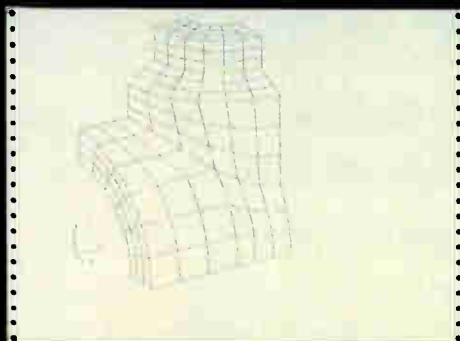
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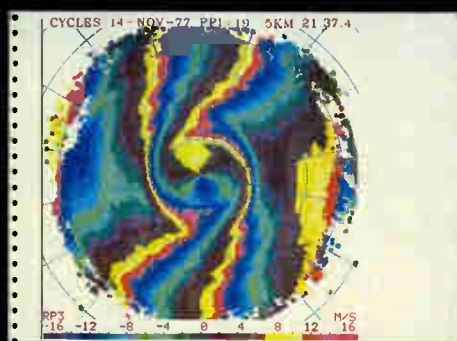
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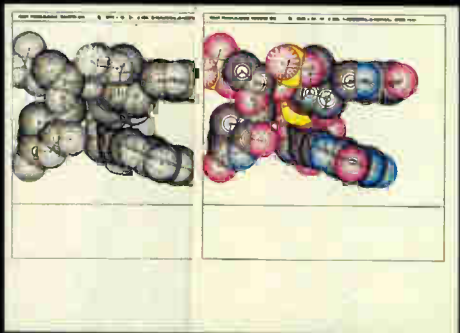
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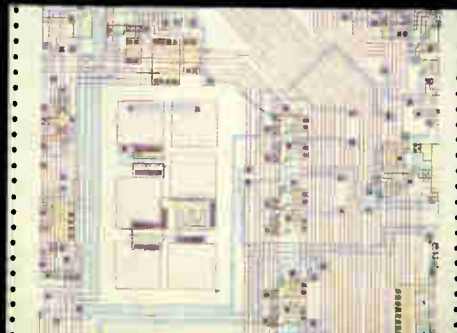
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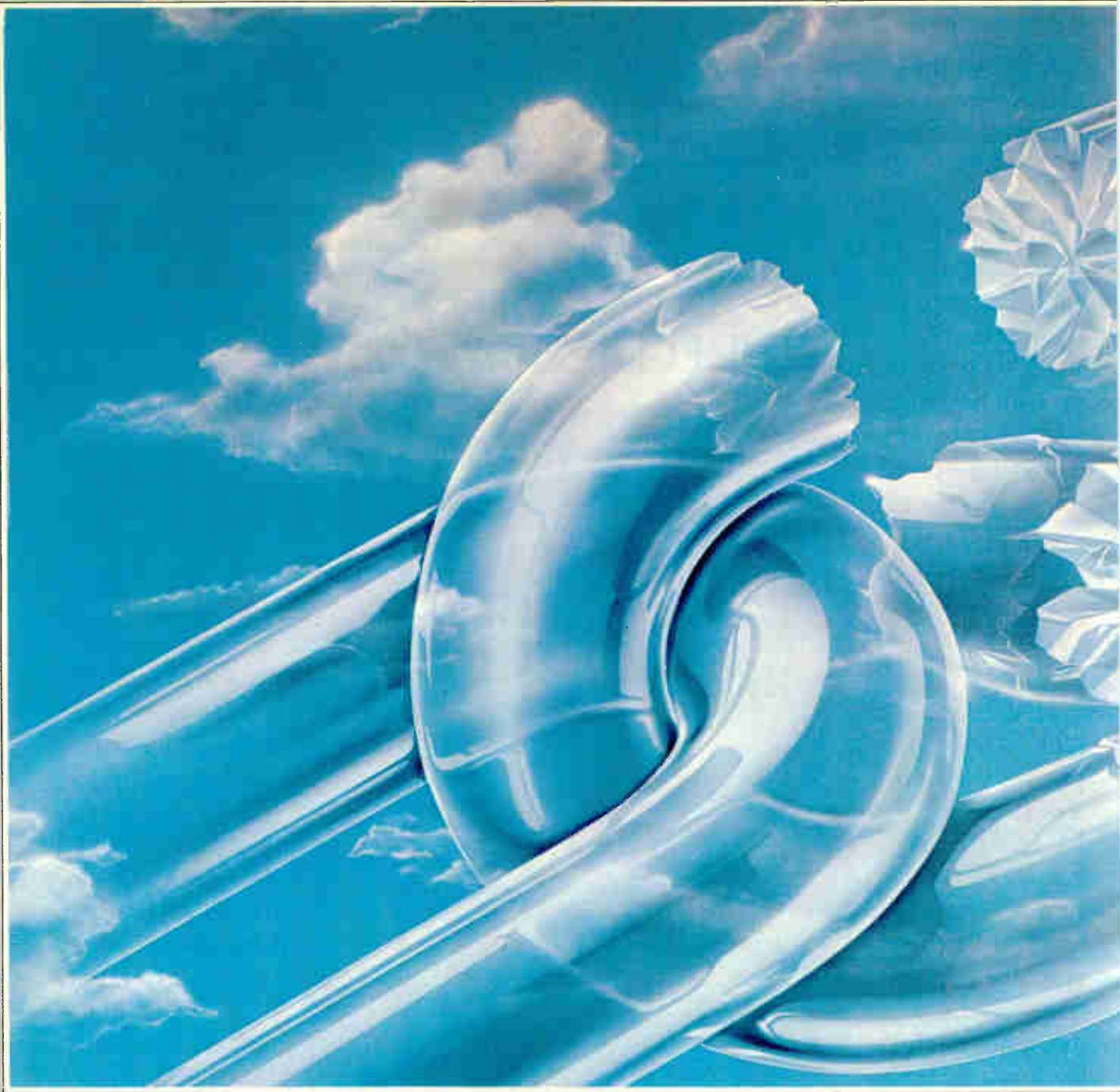
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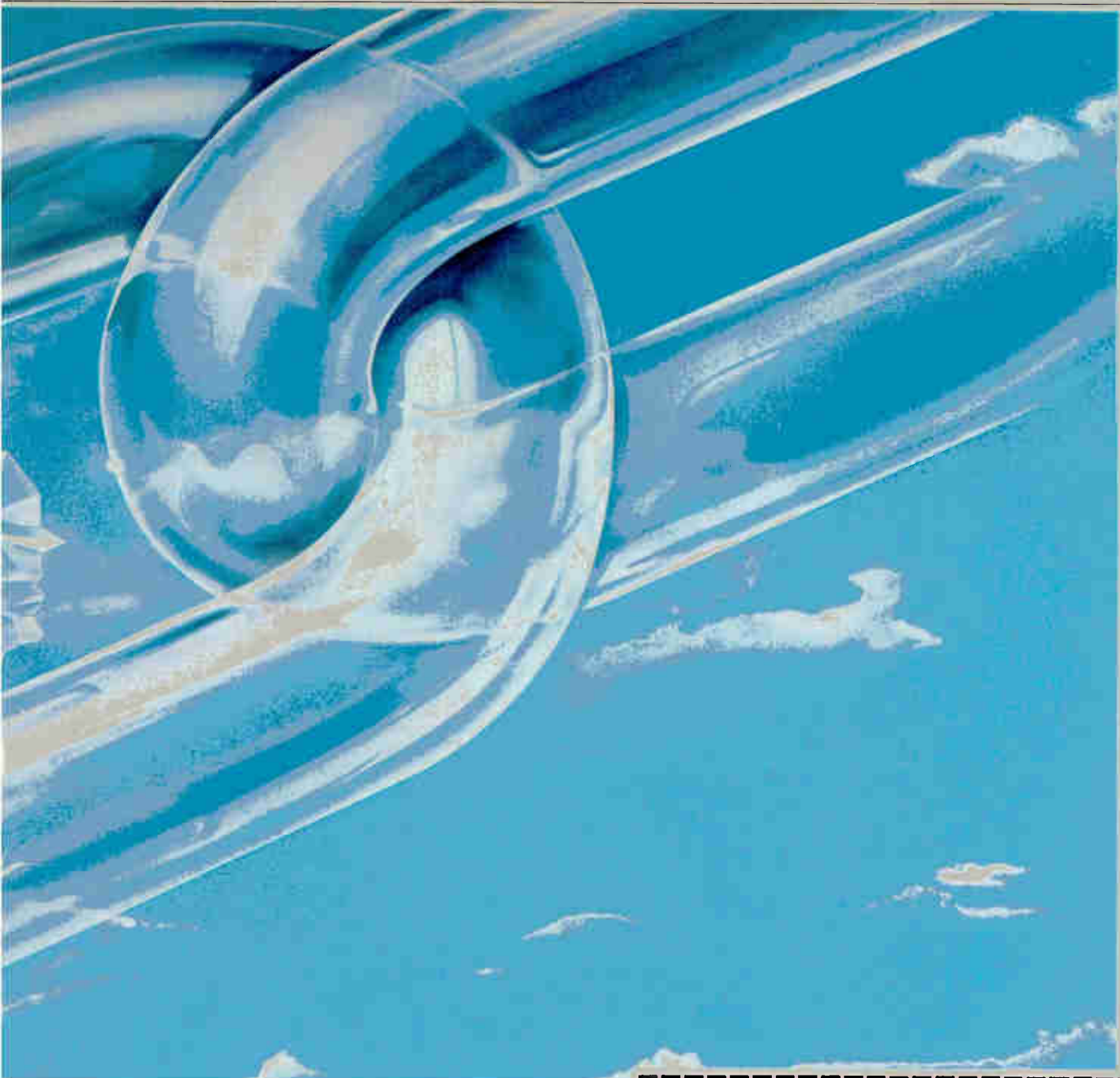
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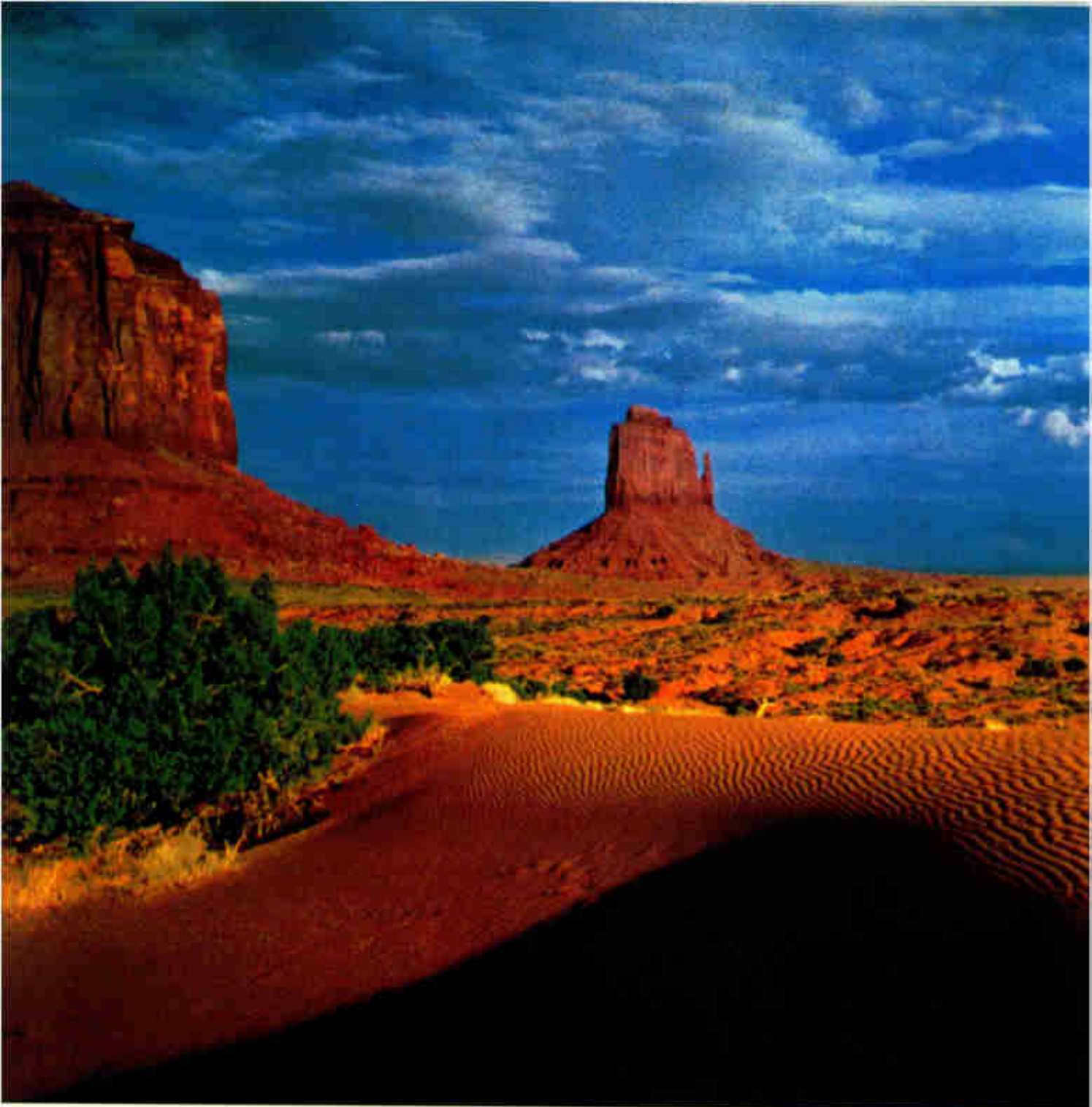
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1K	TBP24S10 TBP24SA10	256W x 4B	35 ns	375 mW
2K	TBP28L22 TBP28LA22	256W x 8B	45 ns	375 mW
4K	TBP28S42 TBP28SA42	512W x 8B	35 ns	500 mW
	TBP28S46 TBP28SA46	512W x 8B	35 ns	500 mW
	TBP24S41 TBP24SA41	1024W x 4B	40 ns	475 mW
8K	TBP28S86-60 TBP28SA86-60	1024W x 8B	35 ns	625 mW
	TBP28S86 TBP28SA86	1024W x 8B	45 ns	625 mW
	TBP28L86	1024W x 8B	65 ns	275 mW
	TBP24S81-55 TBP24SA81-55	2048W x 4B	35 ns	625 mW
	TBP24S81 TBP24SA81	2048W x 4B	45 ns	625 mW
16K	TBP28S166-55 TBP28S166	2048W x 8B 2048W x 8B	35 ns 45 ns	675 mW 675 mW

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power 2K; two 512W x 8B 4Ks; the "by 8" 24-pin 8K. All offer faster address access times and lower power consumption than previous designs.

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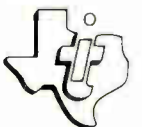
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World Radio History

Fail-safe computer grows modularly

Liberal use of redundant 68000s and Z80As and failure-locating hardware eliminate pauses and bad data due to faults

by James B. Brinton, Boston bureau manager

The market for fail-safe computers is growing, by some estimates as quickly as 50% per year, and according to a number of marketing organizations, users are placing system reliability higher on their list of desirable characteristics. Now there is a new 32-bit entry in the fail-safe market from Stratus Computers Inc. that is the most powerful fail-safe computer ever offered commercially and may also be the most powerful microprocessor-based system yet.

The Stratus/32 is built around Motorola's 16/32-bit 68000 chips and employs 8-bit Zilog Z80As for peripheral control. The smallest available Stratus/32, called a processing module but in fact a complete self-contained computer system, uses 18 microprocessors in redundant configurations.

A single module executes 700,000 instructions per second, and by simply adding modules, it is possible to turn the system into the equivalent of a number-crunching mainframe. As many as 32 modules can be combined to form a system capable of multiprocessing more than 22 million instructions per second, serving 2,048 display consoles, and using 256 megabytes of main memory, 80 gigabytes of disk storage, and 64 tape drives. Each module, which fills about two thirds of a system cabinet, provides fourfold redundancy within itself.

A single-module system may have up to 8 megabytes of memory made of 64-K parts, two disk drives with up to 2.5 gigabytes capacity, tape storage, and input/output control for up to 64 concurrently operating terminals, in addition to control for its several microprocessors. Such a sys-

tem, including somewhat less memory but several display consoles, would cost about \$150,000, depending on configuration—significantly less than the superminicomputers available from major manufacturers. Though the superminis are faster than a single Stratus module, they can not grow in modular fashion as it can.

But the computer with which Stratus expects to compete most directly is the NonStop system from Tandem Computers Inc. Not only is the Stratus a 16/32-bit system compared with the Tandem's pure 16-bit architecture, but, says Stratus, the price of its system should be about one half that for a Tandem machine in similar configurations.

Stratus president William E. Foster points to other aspects of his machine that he considers superior to the competition: its method of ensuring fail-safe operation and its macroarchitecture, which subsumes networking—including X.25—and its high-level portable software.

No checkpoints. According to Foster, most fail-safe computers use software to find hardware failures. Usually, there is a system called checkpointing that must be taken into account when application software is written, and Foster feels this can waste time. "When a hardware failure is detected, it is necessary to stop the computational process, step backward to a checkpoint, and start from there to assure removal of what may be bad data," he says.

"With the Stratus/32, every item of hardware is duplicated, and at least two subsystems perform each task. Then their results are checked against each other in comparators,

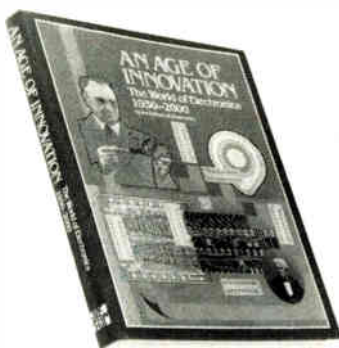
and if there is a difference, the board containing both subsystems is electronically ignored and a duplicate's results are used. Thus there is no need for checkpointing as there is never a chance for data to be contaminated. Also, as soon as an error is detected, a fault-location message is printed out and a light-emitting diode flashes on the edge of the board, spotting it for replacement."

"With the Stratus/32, the user should never realize a failure occurred," he maintains. Indeed, there should rarely even be any noticeable slowing of processing. On one of a module's two disk-control boards, for instance, are duplicate disk controllers with both their inputs and outputs scrutinized by comparators and blocked from the disk store or the system's dual 16-megabyte/s buses by gates. This simple comparator-controlled gate approach protects both the system as a whole and stored data from contamination due to a failed controller, and the same



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ELV

New products

approach is used with central processors, communications controllers, and other system subassemblies.

"We also wanted a system users could gracefully expand in the field," says Foster. The result is a system that grows module by module simply by connecting a pair of coaxial cables between old and new hardware, and then revising a directory that contains a map of system resources, software data files, and locations. It is not even necessary to perform a system generation routine, according to Foster.

Transparent communications. The modules are connected by what are called Stratalink cables running between buses that have speeds from 1.4 to 2.8 megabytes/s. But although this setup is adequate for local-area network applications, Foster wanted to expand the concept of the local network to include any hardware within a company regardless of location. So Stratus/32 comes equipped with the protocols needed to implement the X.25 standard, as well as those of a number of other standard networking systems. "To a terminal user, there should be no difference between access to a module in the same room or one thousands of miles away," says Foster, thanks to the Stratanet protocols.

In line with the idea of removing the burden of failure protection from the programmers' shoulders, Stratus has made it a point to offer high-level-language software across the board. Cobol, Basic, and PL-1 are among the initial languages offered, with more on the way.

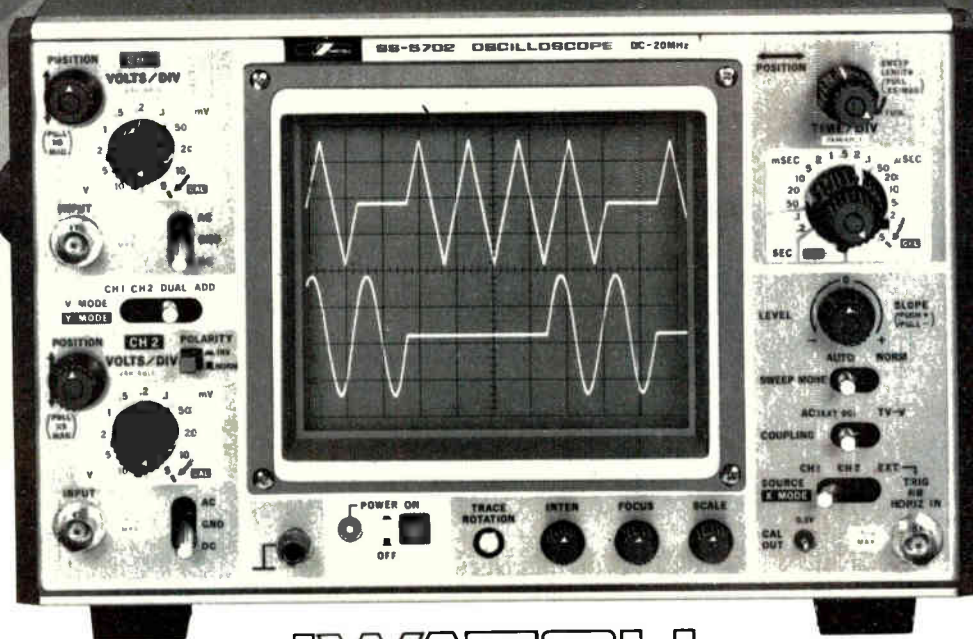
Finally, Stratus is offering parsers for each language for converting application programs into a common intermediate code that then can quickly be optimized by the system and converted into machine code. This method of speeding software generation has rarely, if ever, been offered to the public, says Stratus. Some firms consider such code-generation methods proprietary.

First shipments of the Stratus/32 are scheduled for early 1982.

Stratus Computer Inc., 17-19 Strathmore Rd., Natick, Mass. 01760. Phone (617) 653-1466 [338]

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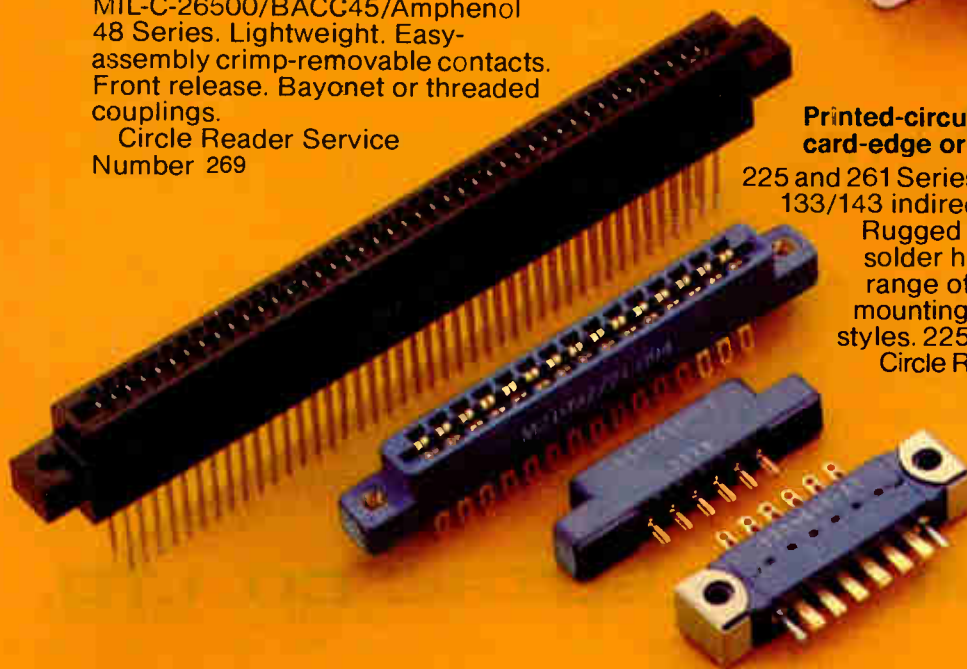


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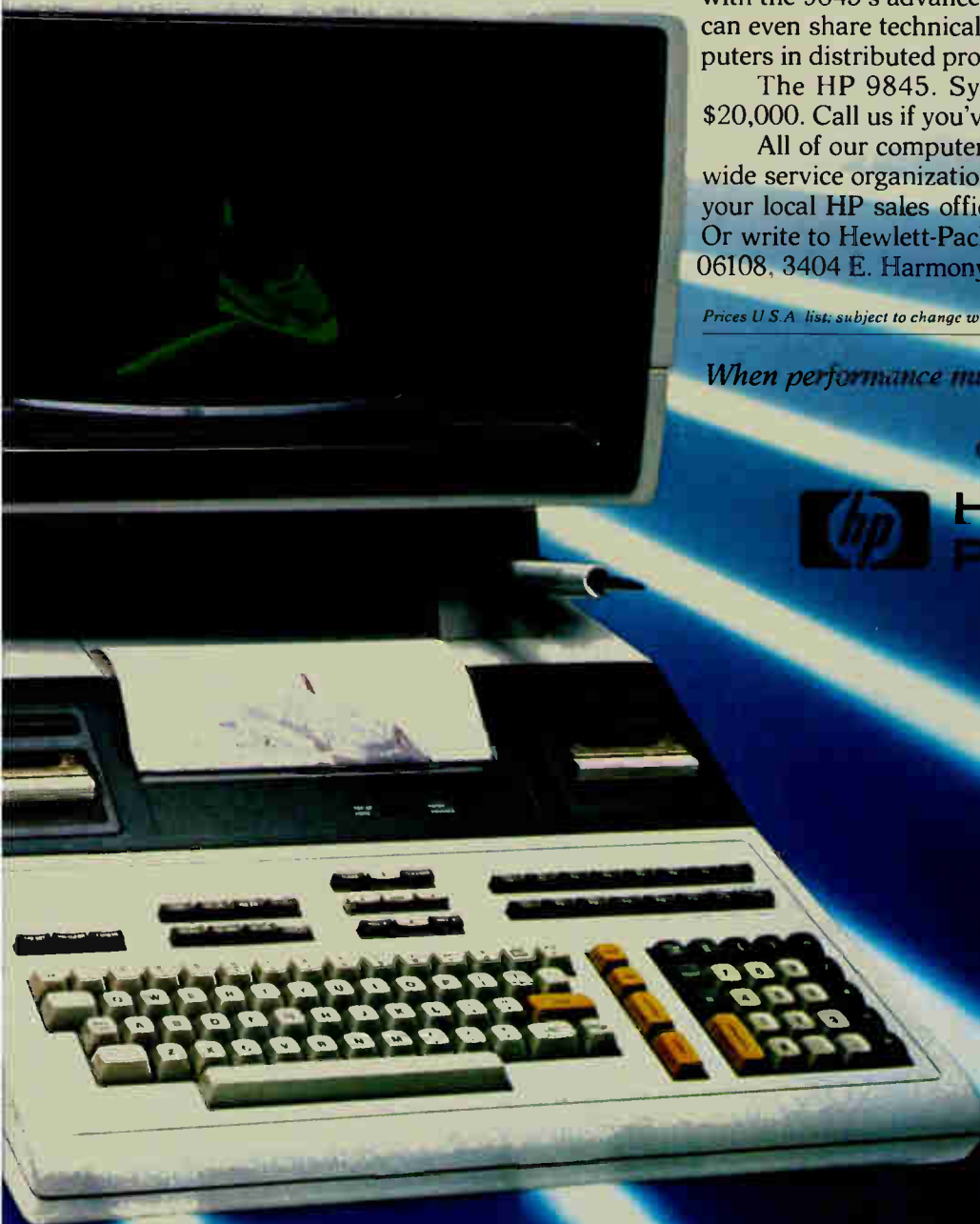
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Thermal Shock	MIL-STD-1344, Method 1003	No Damage $R_C=11.7 \text{ m}\Omega$
Mechanical Shock	MIL-STD-1344, Method 2004	No Discontinuity
Vibration	MIL-STD-1344, Method 2005	No Discontinuity
Socket Durability	500 mating/ unmating cycles	Initial $R_C=11.8 \text{ m}\Omega$ Final $R_C=11.8 \text{ m}\Omega$
Temperature Life	MIL-STD-1344, Method 1005, 1000 hours	Insulation Resistance > $5 \times 10^9 \Omega$ Initial $R_C=11.1 \text{ m}\Omega$ Final $R_C=14.9 \text{ m}\Omega$

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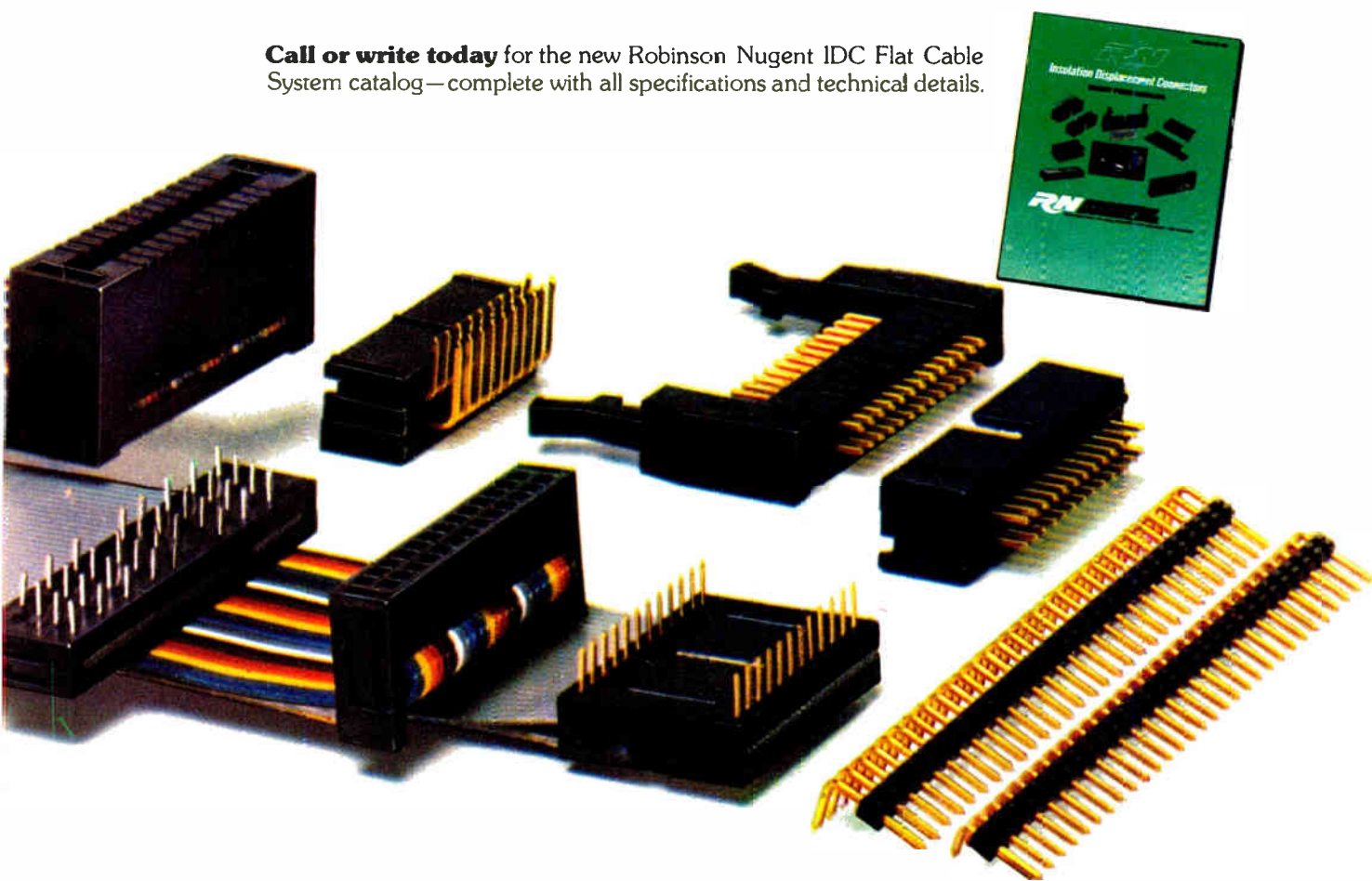
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World Radio History

Circle 174 on reader service card

VLSI design station has data base

8086-based station with Winchester drive edits schematics, interacts with layout and simulation routines on mainframe

by Martin Marshall, San Francisco regional bureau

Two top-flight designers from Intel and one technically oriented marketing man from Calma are the founders of a new company that competes with neither parent but bridges the technologies of the two. The new company is Daisy Systems Corp., whose principals are David Stamm and Aryeh Finegold, formerly engineering managers at Intel, and Harvey Jones, formerly marketing manager for microelectronic systems at Calma. Their product is the Logician, an 8086-based engineering work station containing both considerable hardware power as an individual unit and some very sophisticated resident software packages. These features link the station to mainframes and to interactive graphics systems, such as those of Calma, Applicon, and Avera.

The Logician is intended to be the primary design tool for engineers designing very large-scale integrated circuits, offering them a hierarchical methodology that has previously been seen only on designers' wish lists. The work station's foundation is a hierarchical electronic data base that serves as a single source of block and schematic diagrams, simulation models, connectivity specifications, and design documentation. A piece of software called

the data-base manager maintains the integrity of the interfaces between blocks and between levels of the design hierarchy. This feature not only makes it easier to partition the design task among a number of designers, it also enables the mixing of simulations between partially completed circuits and more fully completed ones.

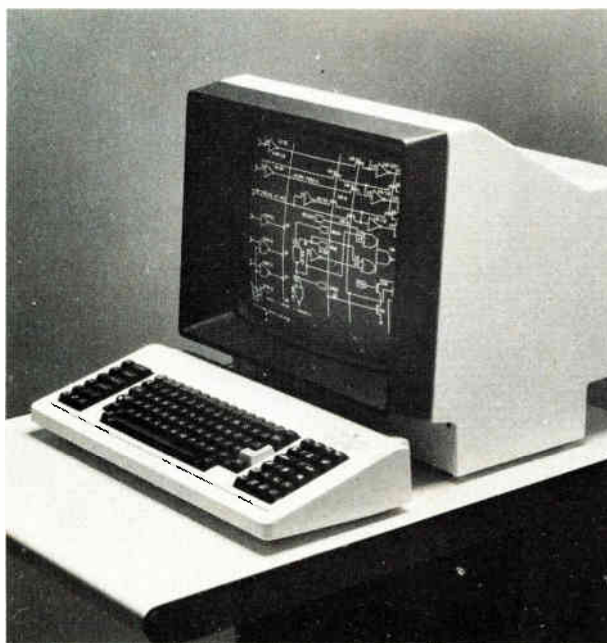
The interface with the designer is a powerful schematic editor that supports the use of such design elements as blocks, components, transistors, signals, buses, arrays, programmable logic arrays, and read-only memories. Although not ready for shipment with the first few systems, a few logical-analysis tools are being packaged by the company with the system, including subroutines for estimates of power consumption, circuit area, and the ratio of so-called

handcrafted to standard cells.

When the engineer is ready to submit a design (or a portion of it) for simulation, the Logician's modeling system extracts the relevant connectivity description and modeling statements from the data base, formats them for the target simulator, and submits the file to the user's mainframe computer. It can also support external automatic placement and routing programs, supplying them with the formatted logical network descriptions from the electronic data base. In interactive design environments, the work station can generate documentation on an optional Versatec V-80 printer-plotter. After the topological description of the circuit has been compiled on a Calma- or Applicon-type system, the unit can then compile the connectivity specification necessary to verify the validity of the mask design.

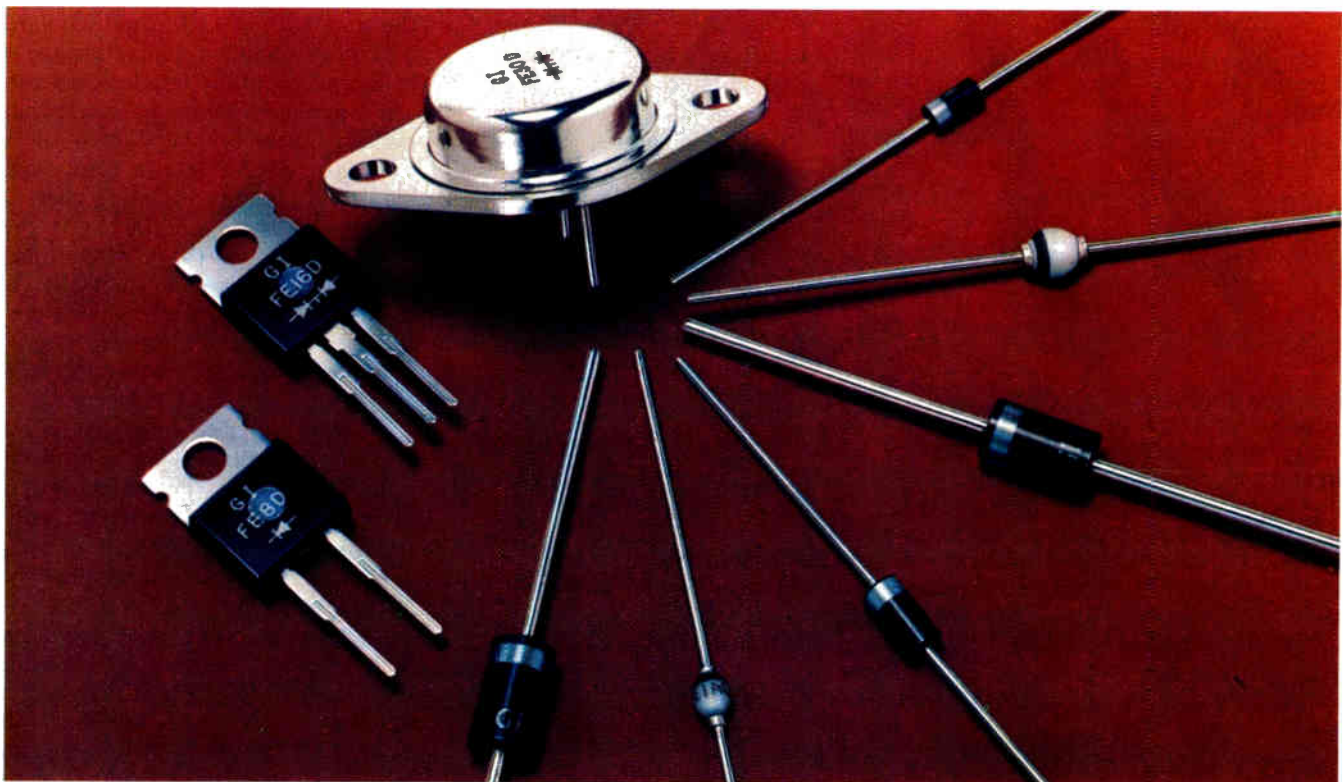
Engines. The hardware of the Logician includes the 8-MHZ 8086-based central-processing subsystem with 512-K bytes of random-access memory and a resident operating system. It also includes a graphics engine that can drive a 826-line display of 1,022 picture elements. The graphics display takes up 10 by 12.5 in. of the 17-in.-diagonal green-phosphor raster display; the remaining area is used for status and user input display.

The Logician system uses graphics as a language rather than as an end product (as a Calma system would do). This means that the designer can use symbolic elements and that those symbolic elements are checked for electrical context. The graphical data is grouped into pages of sche-



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matic symbols and components, each of which holds about the same amount of information as a D-size schematic sheet drawn with a 1/4-size template. An entire page fits in the Logician's page buffer and can yield instantaneous display updates.

A new page can be loaded from the work station's 10-megabyte hard disk in less than 3 s. Once the page is in the page buffer, the designer can use a dynamic panning feature that typically depicts one fourth of a schematic page. He can also zoom back to view the surrounding area.

The on-line storage, including the Logician's 8-in. Winchester disk, allows for the coresidence of all system software, schematics, block diagrams, component libraries, macro-definitions, user documentation, and circuit and logic models for a design. It contains about 9 megabytes of memory space under user control for archival storage. For user-to-user design transport, a 1-megabyte floppy-disk unit is included.

Communications. At present, the exchange of floppy diskettes is a primary form of sharing information among several Logician systems, but each work station is provided with a high-speed serial interface that will be used for future networking and an RS-232-C interface that links it to the host mainframe. Files can be transferred via the link, and the Logician can operate as an intelligent editing station with local storage. Its transmission rates are selectable from 110 b/s to 19.2 kb/s. Like the high-speed serial interface, the RS-232-C interface supports bisynchronous, Synchronous Data-Link Control, and High-level Data Link Control protocols.

The price of the Logician is \$300,000 for a minimum order of four stations, with discounts available for larger orders. Notes Jones: "In contrast to conventional interactive graphics systems, the Logician does not suffer performance degradation in a multiterminal environment." Deliveries will begin in December.

Daisy Systems Corp., 2118 Walsh Ave., Santa Clara, Calif. 95051. Phone (408) 727-5100 [339]

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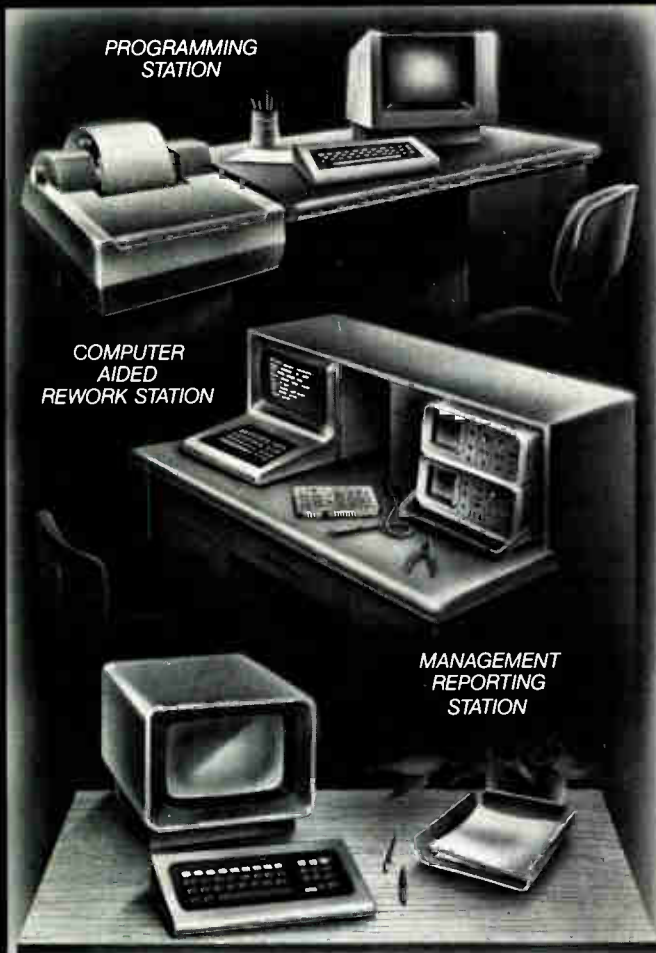
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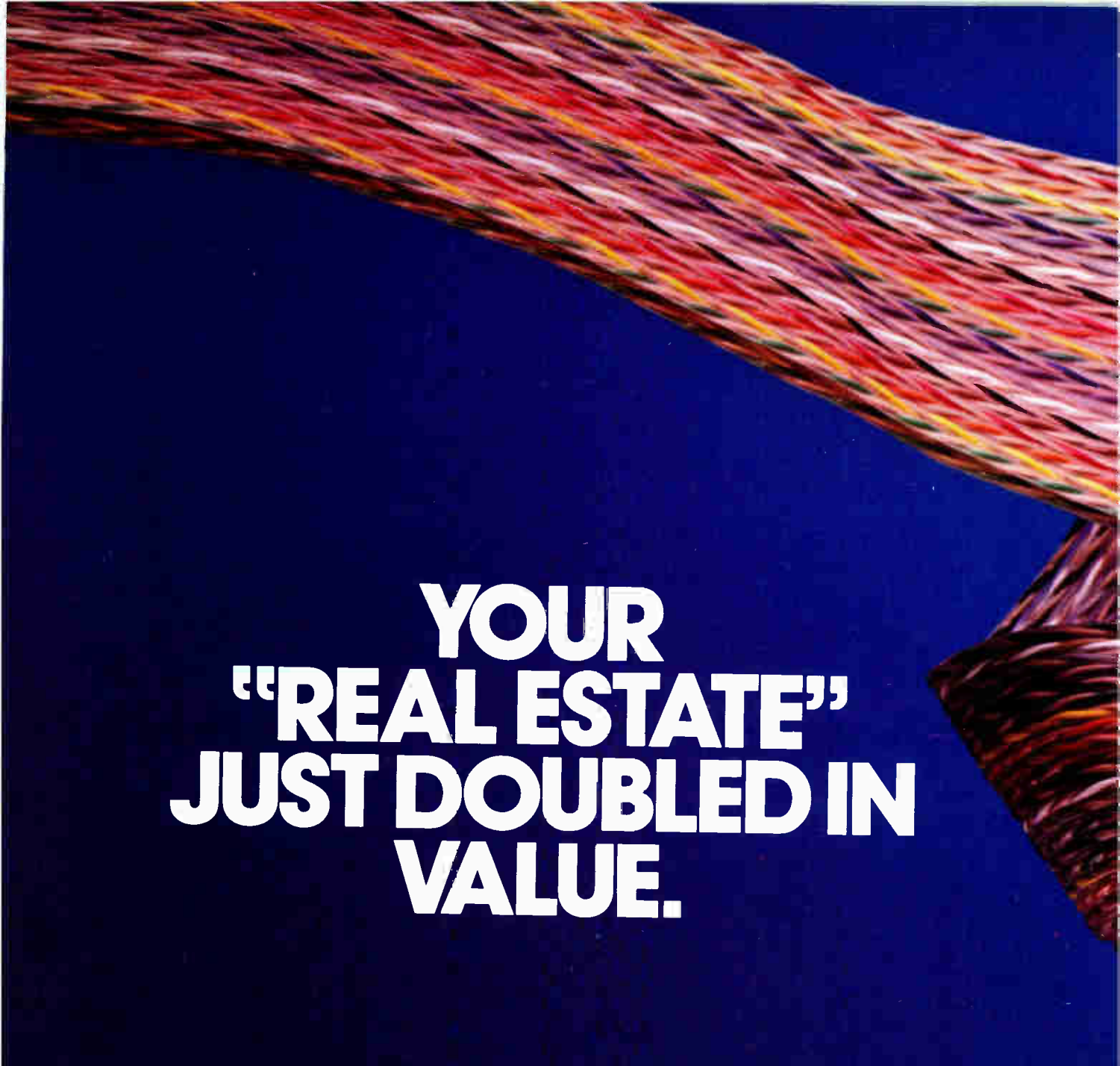
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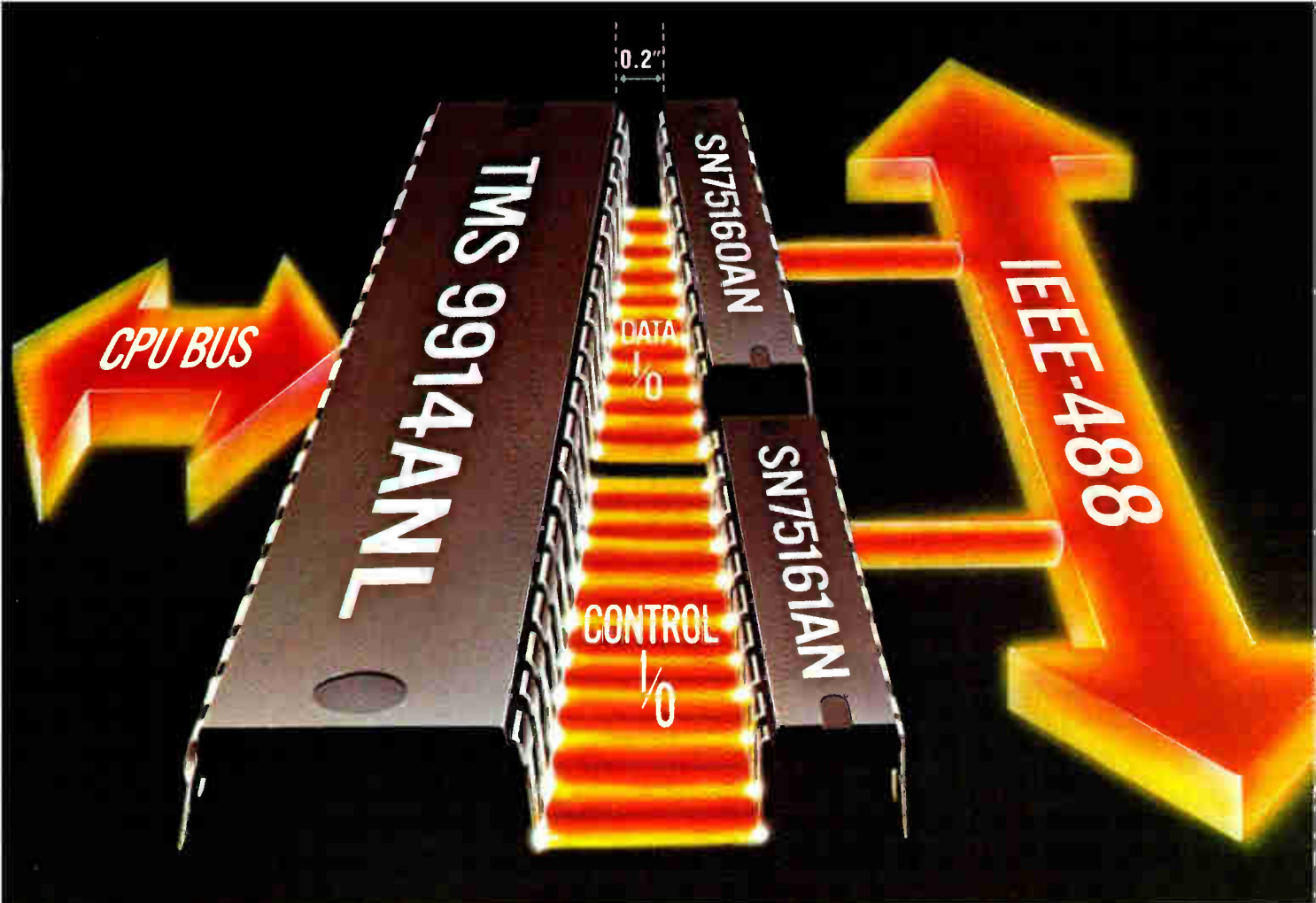
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85593D

Intel boxes system with disks, software

Semiconductor house takes on minicomputer makers with \$19,000 box housing 35-megabyte Winchester, floppy disk, CPU, and RAM

by R. Colin Johnson, *Microsystems & Software Editor*

The **System 86/330** microsystem from Intel is a full-blown computer that can be used in the same sort of embedded application areas that minicomputers are used in today. This first integrated package from the semiconductor giant pulls together its chip, board, chassis, and software offerings into a single package allowing original-equipment manufacturers to make or buy equivalent systems from a single source. It includes an iAPX-86/20 central-processing board, an 8086-based card with an 8087 numeric processor on a multimodule, 320-K bytes of random-access memory, a 35-megabyte Winchester-technology disk drive, and a 1-megabyte floppy-disk drive, all housed in a single enclosure.

All components, including the switching power supply but excluding the disk drives, are manufactured by Intel. The IEEE-796 Multi-bus card cage has two empty slots, the other four being occupied by the processor board, the RAM card, and the two disk controllers. The boards are standard Intel offerings; all the user need supply is a terminal to attach to the integral RS-232-C port and a printer that can interface with its parallel port. The enclosure measures 21 by 16 by 12 in.

The 86/330 is supplied with a full complement of preconfigured software that is based on the iRMX-86 real-time multitasking operating system whose layered architecture allows the user to remove memory-consuming routines that are not required in a particular application. There is an extensive set of self-test routines in erasable programmable read-only memory that are activated at power-up and reset. These rou-

tines can isolate problems to the board and sometimes even the component level. They also exercise the system software and peripherals.

On-site maintenance contracts are also available, as is a board exchange program, a software subscription service, and an applications engineering consulting service. Also available for the System 86/330 is the iMMX-800 multiprocessor message-passing software, which allows OEMs to configure systems that utilize up to two more central-processor boards sitting on the same bus.

Program development languages include Intel's own ISO-standard Pascal-86 compiler, a Fortran-77 subset compiler, and PL/M-86, in addition to an assembler. In addition, the third-party software being offered by Intel's software distribu-

tories' Unix and Digital Research's CP/M as alternatives running the same languages. All Intel languages may be offered with a re-sold system in addition to the application software developed by the vendor. The standard program-development tools for the software-compatible Intel development system also come with the 86/330.

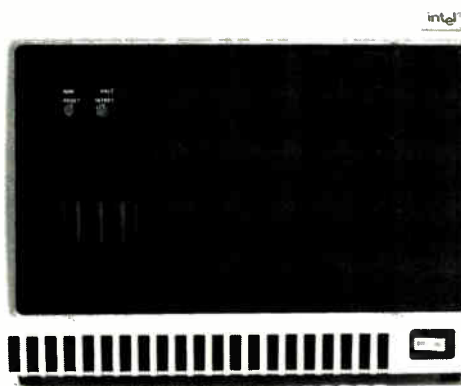
This wide variety of software is made possible by what is called the Universal Development Interface, which defines a standard connection methodology between languages and operating systems. There are 22 standard system calls included in UDI, and both language and operating-system vendors will conform to them. The UDI defines a software bus that permits application programs to be run under any of the operating systems.

The 86/330 is targeted at applications requiring fast response to terminals, instrumentation, communication lines, and other high-speed devices. It is easily configurable by the OEM through boards available from Intel and comparable in speed to a mid-range minicomputer.

The basic system, including the four boards described above, chassis,

power supply, Winchester and floppy-disk drives, preconfigured iRMX-86 software with configurable options, complete documentation, and is priced at \$19,000 in quantities of 10. Deliveries begin in January.

Intel Corp., 5200 Elam Young Pkwy., Hillsboro, Ore. 97123 [340]



tion operation in Santa Clara is pre-configured for the System 86/330. That makes available Microsoft's Basic interpreter and compiler, Whitesmith's C compiler, as well as both Microsoft's and Micro Focus' Cobol compilers.

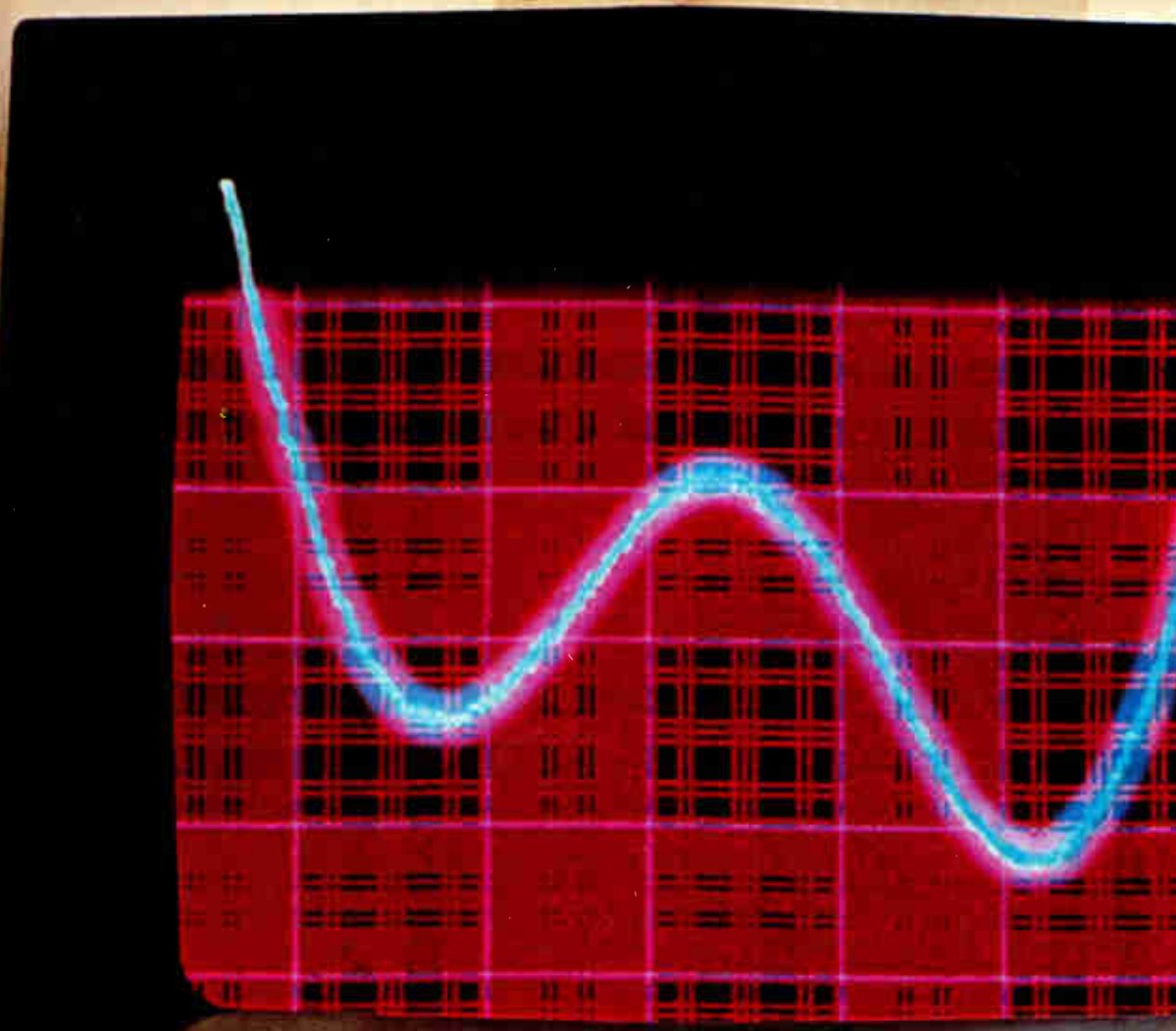
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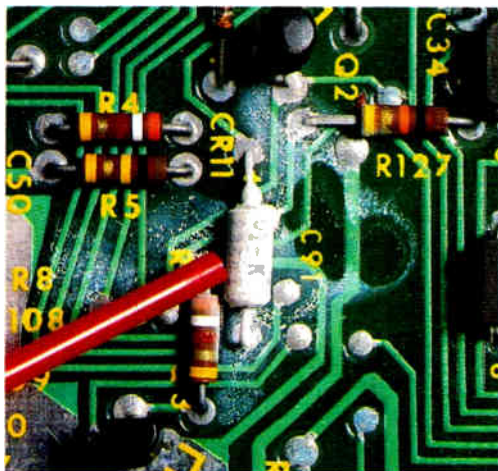
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Graphics display refreshes at 60 Hz

CAD station displays 8 or 16 colors, pans and zooms over field of 4-K by 4-K elements

Taking the basic design of its 4110 series of intelligent computer display terminals, Tektronix Inc. adds a new family member with a color raster-scanning display screen. The model 4113 offers the same processing capability for off-loading the host computer and providing the user interaction as the recently introduced monochromatic raster-scan model 4112 graphics station and the direct-view storage-tube model 4114.

The new model, with a resolution of 640 by 480 points on a 19-in.-diagonal screen refreshed at a noninterlaced 60-Hz rate, provides stability, resolution, and easy viewing for the intended market in computer-aided-design and -mapping applications. The terminal has a picture memory of 4,096 by 4,096 points for zooming and panning. Communications with a host computer can be up to 9,600 b/s.

To be shown for the first time at the Autofact III show in Detroit, Nov. 9-12, the 4113, with three bit planes, can display eight colors simultaneously from 4,096 possible colors—with an optional fourth bit plane, 16 colors can be used. The brightness, saturation, and hue of each color may be adjusted.

Speed emphasized. Control of the 4110 family of terminals, of which the 4113 is the first of a series of color raster displays, is handled by

an Intel 8086 16-bit microprocessor. Tektronix plans to put a lot of development emphasis on the 60-Hz noninterlaced refresh to ensure flicker-free pictures.

The speed of the display will also be a higher priority than resolution with a goal to get the raster terminals up to the speed of the 4114 direct-view storage-tube model. "It will take a little longer to go to higher resolutions at the 60-Hz rate, but we think the speed and stability are a good tradeoff for the type of customers at which we are aiming," says business unit marketing manager Michael J. Kondrat.

Product designers at Tektronix designed the 4110 series of intelligent display terminals to share the same basic software, data base, and user interface. Color capability was planned from the outset.

Customers may now choose from a compatible family of storage tube, monochromatic raster, and color raster terminals. "Much large-scale and very large-scale integrated-circuit design is virtually impossible without the color dimension," says Gary Romans, Tektronix 4113 marketing manager. "In many applications, users now view color as just as important as resolution.

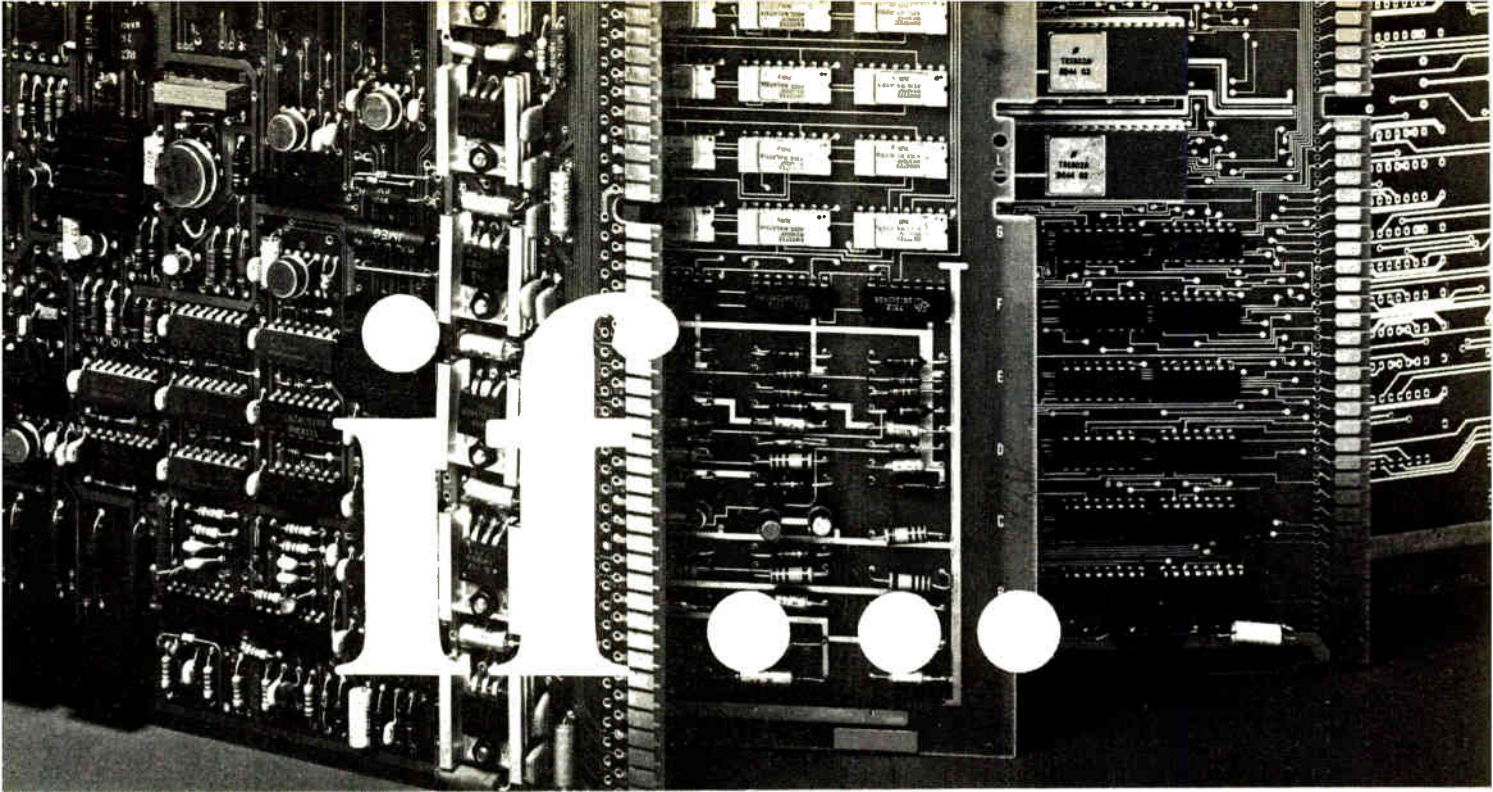
The price for the 4113 in the U. S. is \$16,500, with the optional fourth bit plane costing about \$1,500. It will be available with complete component and service support by early February at all Tektronix outlets.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077. Phone (503) 644-0161 [361]



Disk drive for OEMs holds 673 megabytes

The model 8775 disk drive for original-equipment manufacturers has Winchester fixed-media disk-drive technology, an unformatted capacity of 673 megabytes, and an ANSI storage-module drive interface. Much of the 8775's technology is derived from the firm's double-density 8650 disk drive, such as its head-disk assembly design and microprocessor-controlled diagnostics. The 8775 has



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eight 14-in. disk platters with a density of 957 tracks/in. and transfers data at 1.2 megabytes/s. It uses 30 read-write heads with a preamplifier, selection chips, and a dedicated servo surface to deliver a typical average seek time of 23 ms.

In typical original-equipment-manufacturer quantities, the drive will sell for \$19,000. Evaluation units will be available in the first quarter of 1982, and full production is expected to be under way in the third quarter.

Storage Technology Corp., 2270 South 88th St., Louisville, Colo. 80027. Phone (303) 673-5151 [363]

Large business system can support 127 interactive CRTs

Sequel, a large business computer system, boasts an automatic application-software generator, a 32-bit central processing unit, up to 2 megabytes of main memory, and 1 megabyte of disk storage, with enough power to support 127 interactive terminals. The system can run



up to 10 times faster than small business systems, gaining its improved performance through faster circuitry, larger memory capacity, and advanced logic. Languages available are Data/Basic and English, Microdata's data-base retrieval language.

An option on Sequel is All, an application development tool that virtually eliminates programming. Systems available in addition to All include Wordmate, a word-processing system; Admax, a system for advertising agencies; and Results, a financial applications system.

The basic Sequel system is available for \$155,500 and includes four terminals, 1 megabyte of main memory, 256 megabytes of disk storage, a tape drive, and a 300-line/min printer. The software carries a one-time licensing fee of \$22,700.

Microdata Corp., 17481 Red Hill Ave., Irvine, Calif. 92713. Phone (714) 540-6730 [364]

Printer makes copies from Xerox 350 color-slide system

With the Versatec V-80 electrostatic printer/plotter, users can make hard-copy proofs of slide visuals created on the Xerox 350 color-slide system. The V-80 captures the image from display memory and produces a black and white representation of the color visual on 11-by-8½-in. paper at a cost of approximately 4¢.

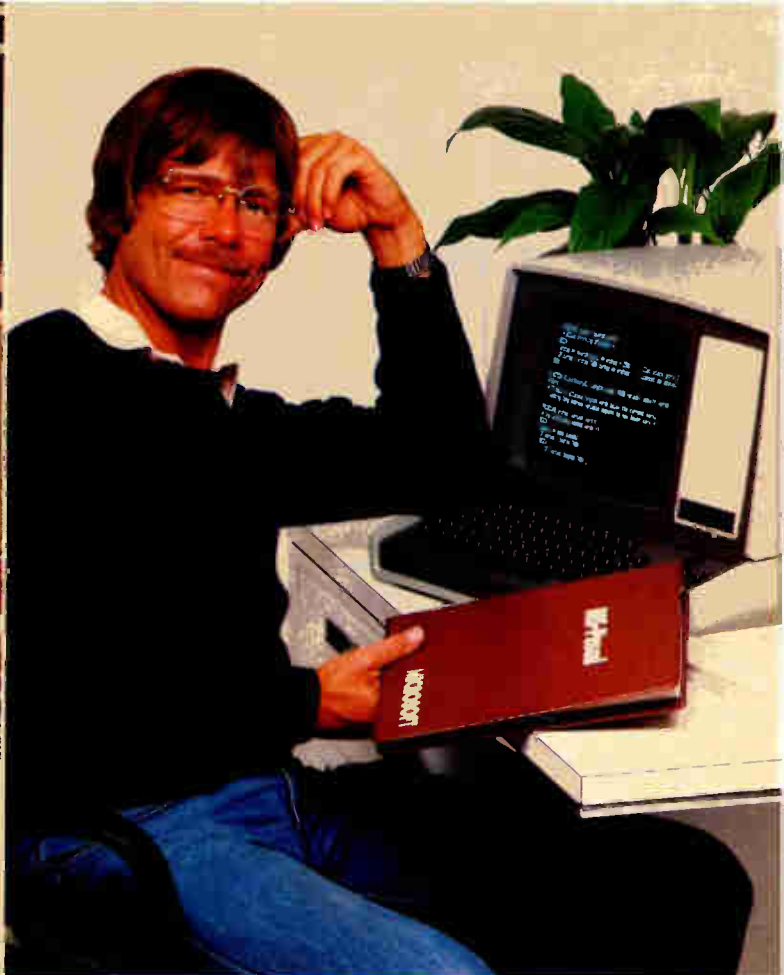
A 200-point/in. resolution accommodates complex graphics, and a dual-array writing head produces an overlapping dot pattern for high-contrast blacks and continuous lines. The Versatec hard copy will not fade or deteriorate, and it accepts pen or pencil notation.

The V-80 can also be used to produce hard copy from other storage-tube and raster-scanning displays. Controllers for various display types can be chained to serve a mix of display terminals with one printer/plotter. Long-line driver-receiver options allow the controller to operate up to 1,000 ft from the central processing unit or the plotter. The V-80 sells for \$8,500 and can be delivered in 30 to 60 days.

Versatec, 2805 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 988-2801 [365]

Copier prints from graphics terminals in 125 colors

The Act-1 color copier makes plain paper copies of color images displayed on computer graphics terminals. The size of a standard office typewriter, it employs an ink-jet printing technology to produce mul-



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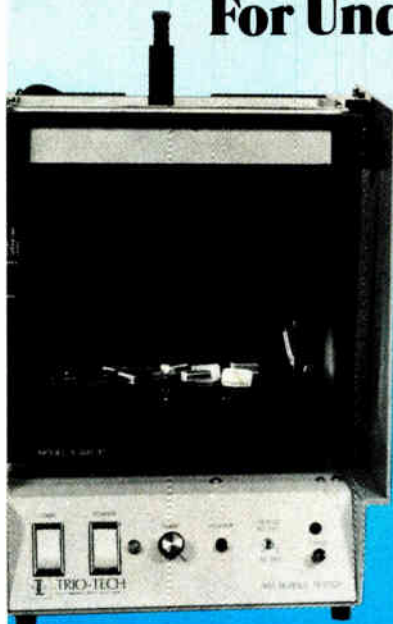
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ticolor images on paper in less than two minutes for an 8½-by-11-in. print.

Using a multiple-dot-per-picture-element shading technique, the Act-1 can reproduce up to 125 shades of color. It prints 85 dots/in. vertically and up to 140 dots/in. horizontally. It also features automatic black-to-white background color reversal.

Users can choose one of four interfaces: a parallel (line-printer type) interface for host computers or color graphics controllers; an RS-232-C serial interface for host computers; a floppy-disk drive interface, or a RS-170- and RS-343-compatible video interface for color monitors at additional cost. The copier sells for \$9,000.

Advanced Color Technology Inc., 187 Billerica Rd., Chelmsford, Mass. 01824. Phone (617) 256-1222 [366]

Drive, controller expand system's floppy-disk storage

Two Zenith Data Systems products expand diskette storage on its computers to more than 640,000 characters per 5¼-in. diskette, or more than six times the previously available capacity. Such an increase permits large programs such as accounting or data-base management programs to be put on 5¼-in. diskettes instead of 8-in. ones.

The high-density Z-37 has a pair of drives in a 9-in.-wide box, using both sides of the floppy diskette and doubling the number of tracks used on each side to 160. In addition, the Z-37 retrieves information 40% faster and uses industry-standard soft-sectored diskettes. The Z-37 sells for \$1,995.

The double-density disk controller card, the Z-89-37, increases the storage capacity of the 5¼-in. drives from 100,000 bytes to 160,000 bytes. It operates with either 40-track drives or 160-track drives. The controller card sells for \$395. Both products are available immediately.

Zenith Data Systems, 1000 Milwaukee Ave., Glenview, Ill. 60025. Phone (312) 391-8181 [367]

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Circle 33 on reader service card



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disk cartridge drives plus bootstrap card, and you'd pay about twice the cost of one DSD 880. Plus, you'd give up the high reliability of the DSD 880's winchester technology—a state-of-the-art choice DEC doesn't even offer LSI-11 and PDP-11 users. And you'd have three ungainly boxes over 30 inches high—as compared with the DSD 880's compact 5¼-inch panel height, which saves you rack space and cabinetry costs and allows use in space-critical applications.

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DSD 480 provides double-sided floppy storage for your LSI-11 or PDP-11.

For twice the capacity of DEC's RX02, choose the DSD 480. An optional EXCHNG™ software program lets the DSD 480 transfer files between IBM- and DEC-generated diskettes.

DSD 470 gives you low-cost double-sided floppy storage for your LSI-11.

The DSD 470 is software compatible and can be configured for single- or double-sided diskettes. And its single-board controller/interface* has far fewer parts than separate boards for better space utilization and improved reliability.

Choose DSD 440 for single-sided floppy storage with your LSI-11 or PDP-11.

The DSD 440 is RX01 and RX02 software-compatible. It can transfer data 20% faster than DEC's RX02, and features built-in self-diagnostics for easy servicing.

Choose DSD 430 for lowest entry cost with your LSI-11.



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DEC designs great CPUs. Data Systems Design gives you disk storage to match.

For CPU quality, you can't beat DEC's LSI-11 and PDP®-11. But their disk storage doesn't always measure up. At Data Systems Design, data storage is our *only* concern. That's why our DEC®-compatible disk systems are more reliable, less expensive, more compact and easier to maintain than the disk systems you get from DEC.

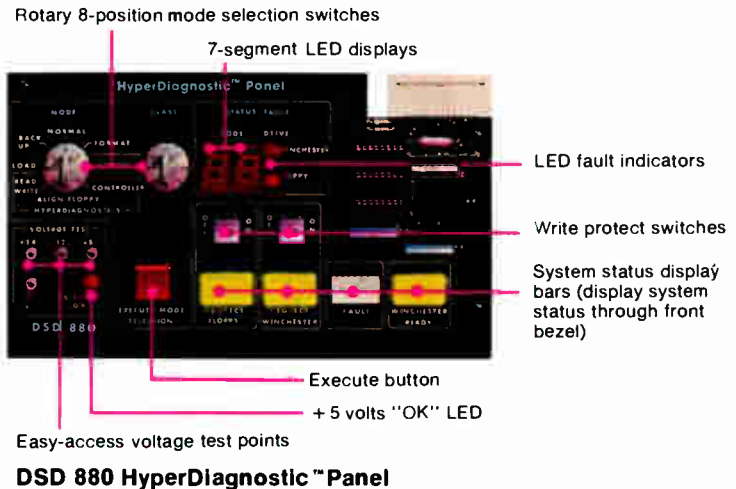
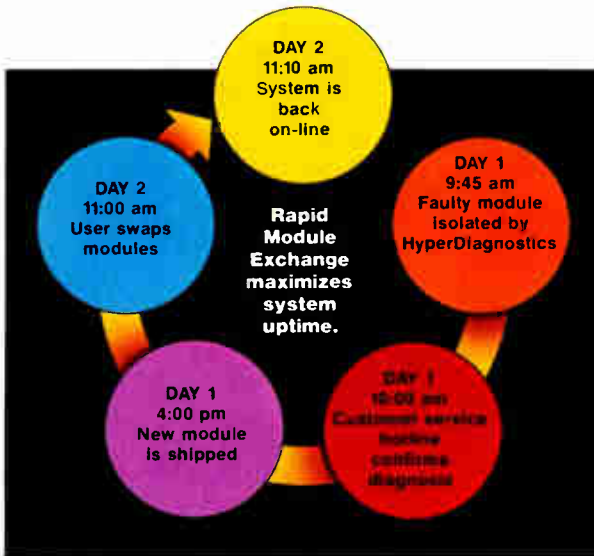
And you get more choices of systems, too, so you can pick the exact features your product application requires.

DSD 880 gives you more megabytes per buck for your PDP-11 and LSI-11.

With the addition of a new DSD 880 version, you now have three choices in winchester disk storage: 31.2, 20.8 or 7.8 megabytes. Each with a choice of 0.5 single- or 1-megabyte double-sided floppy backup. More capacity for less cost-per-megabyte than any comparable DEC alternative.

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More reliable performance and easier maintenance.



DSD 880 HyperDiagnostic™ Panel

A revolutionary concept in uptime: Remote diagnosis ends costly service calls.

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*This controller/interface is also available separately as the DSD 4140.

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Circle 101 for DSD 880 Information.
Circle 102 for DSD 480 information.
Circle 103 for DSD 470 Information.
Circle 104 for DSD 440 Information.
Circle 105 for DSD 430 information.



Data Systems



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LTX RESPONDS

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Circle 199 on reader service card

Communications

Optical links have a low profile

Transmitter and receiver modules contain multifunction master-slice integrated circuits

Honeywell Inc.'s Optoelectronics division is using a low-profile package to house a family of new fiber-optic transmitter and receiver modules built around master-slice integrated circuits. The modules are the first to use the bipolar master-slice chips, which also can be altered in the final stages of production to quickly produce semicustom products [*Electronics*, May 19, p. 39].

The series is being targeted at a wide range of fiber-optic applications, including point-to-point links and data buses. Initially, Honeywell will be offering seven standard versions of the low-profile transmitter and receiver modules, but use of master-slice ICs opens the door to changing bandwidths and combinations of functions. The transmitter and receiver master-slice ICs can be tailored with the final metal interconnect mask, linking predefined functional blocks located on the die, fulfilling objectives similar to those

of custom logic-gate arrays.

The firm's standard products offer two data formats: nonreturn to zero (NRZ) and a duty cycle with a constant average value of 50%. However, other versions—such as one that uses Manchester-encoded data or one that provides optical feedback for driving a laser—can be produced by changing the metal interconnections. The Optoelectronics division expects to begin production on some semicustom products next year.

The low-profile module comes in two classes: industrial-military and commercial. The industrial-military will feature hermetically sealed active components capable of -55° to $+125^{\circ}\text{C}$ operation and SMA cable connectors with hermetically sealed metal-can light-emitting diodes and p-i-n photodiode detectors. These modules are priced at \$150 for each transmitter-receiver pair in quantities of 100.

The commercial modules, which have an operating temperature range of 0° to 70°C , will use ADM connectors with LEDs and photodiodes in plastic packages. They cost \$100 for each transmitter-receiver pair in orders of 100. Some sampling has already begun and volume production of both classes is set for the beginning of 1982.

For point-to-point link applications with high data rates, Honeywell's series offers three basic transmitter-receiver sets. The HFM2010-

224 transmitter-HFM1010-221 receiver can handle a maximum of 10 Mb/s and a maximum transmission distance of 2,000 meters for those using NRZ data formats.

The HFM2025-224/HFM-1025-221 can handle up to 25 Mb/s and a maximum distance of 1,000 meters in NRZ formats. Both of these are industrial-military modules. In the commercial module, the HFM2010-001/HFM1010-001 can handle up to 10 Mb/s and a maximum distance of 1,500 meters in the NRZ format.

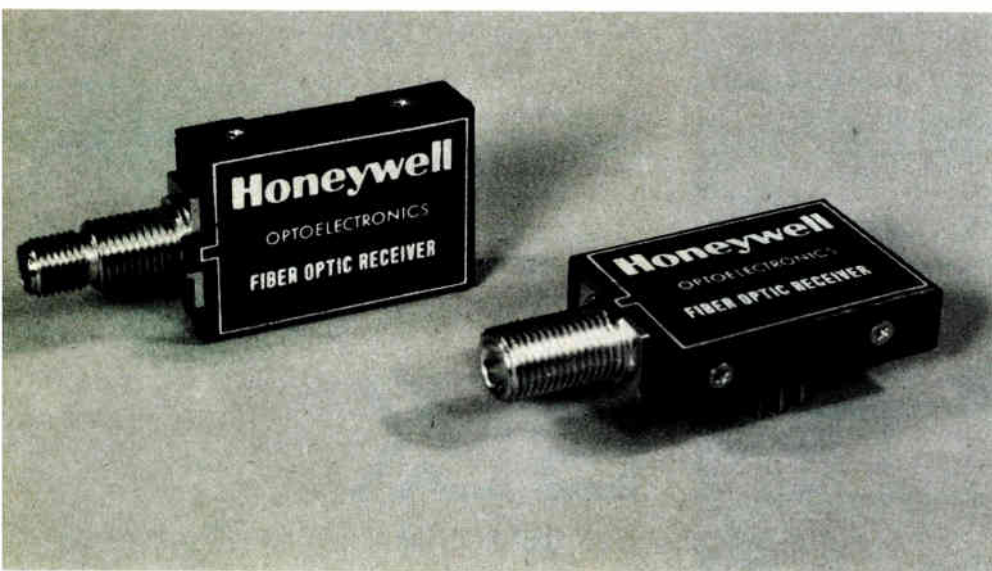
In duty-cycle formats with a constant average value of 50%, the HFM2110-22/HFM1200-221 can handle a maximum of 0.5 Mb/s and a maximum length of 3,000 meters in a burst mode. The HFM2110-222/HFM1201-221 can handle up to 1 Mb/s and a maximum distance of 500 meters in the 32-terminal star setup and 3,000 meters in a burst mode.

Others. The HFM2010-222/HFM1203-221 can handle 3 Mb/s and 500 meters in the 32-terminal star configuration or 3,000 meters in the burst mode. These are all in the industrial-military class. In the commercial category, the HFM-2110-001/HFM1202-001 can handle up to 1 Mb/s and 300 meters in the 32-terminal star setup and 2,500 meters in the burst mode. All of these figures are based on the use of a fiber with a $100\text{-}\mu\text{m}$ core diameter and a 0.25 numerical aperture.

The low-profile case, which measures 1.9 by 0.86 by 0.3 in. thick, has been designed for direct mounting on circuit boards spaced 0.5 in. apart center to center. The electrical connections are spaced like those of 24-pin dual in-line packages, with 0.1-in. lead spacings on 0.6-in. row centers.

The transmitter modules have 10 pins, the receivers 8, and their low profile allows proper clearance when boards are placed in standard computer racks. The new package is also suited for panel mounting. Chief scientist J. R. Biard says Honeywell will use this low-profile package on all future fiber-optic transmitter and receiver modules.

Inside each transmitter module



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New products

are a transmitter master-slice IC, capacitors, and a Honeywell Sweet Spot LED. The receiver module has a receiver master-slice IC, a resistor, and a p-i-n photodiode. The transmitter master-slice IC contains TTL inputs that drive encoder logic and timing circuits, plus high-current drivers for the LED.

The receiver master-slice chip contains the photodiode preamplifier that drives decoder logic and timing circuits, plus a TTL output buffer. There are six different functions on the transmitter IC, which measures 62 by 83 mils. The master-slice receiver chip implements 15 types of functions on a 64-by-85-mil die. The receiver module has a signal-quality TTL output that indicates when the optical signal is good enough to produce a 10^{-9} bit-error rate.

The master-slice chip, housed in an 18-pad ceramic leadless chip-carrier, is flush-mounted on a 30-mil ceramic substrate inside the module. In the transmitter, capacitors are mounted to the substrate by reflow soldering. The capacitors, which were not included on the master-slice chip because of their size, are used to change data rates and power-supply levels.

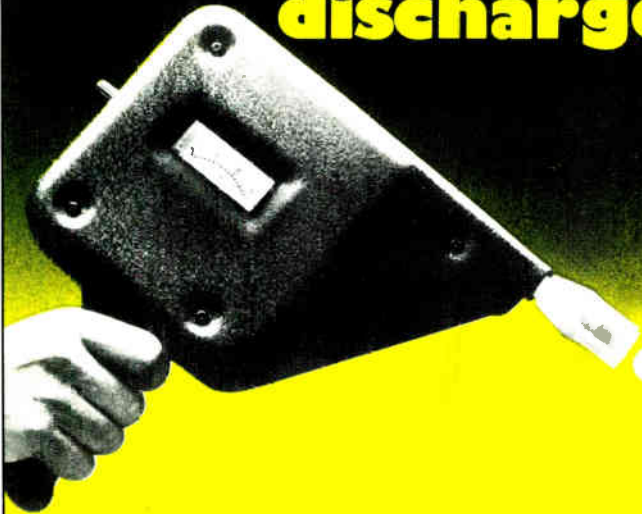
Honeywell Inc., Optoelectronics Division, 830 E. Arapaho Rd., Richardson, Texas 75081. Phone (214) 234-4271 [401]

Unit offers full-duplex data transmission at 5 Mb/s

The ODS-306+ 5-MHz wideband synchronous data set is intended for high-speed serial synchronous communication between computers and serves as a communication link for the IBM 3274 remote control unit to repeaterless distances of 5 km. In



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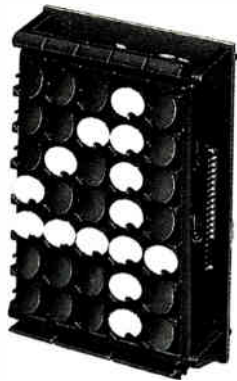
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New products

In addition, for T-1 digital transmission facilities, it provides a fiber-optic front end, replacing the Bell 306 data set and thus providing an alternative communication medium for the Bell 303 data set.

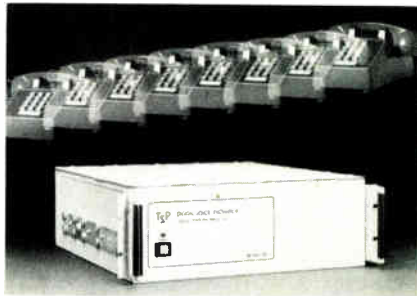
The unit is plug-compatible with the Bell 306 standards and the IBM 3274 remote-channel unit. The RS-232-C interface is available as an option.

The ODS-306+ data set can operate over standard internally supplied clock rates for 40.8, 57.6, 130, and 460 kb/s and 1.344 Mb/s. The ability to transmit asynchronous data at speeds of up to 300 kb/s is also provided. Three-level built-in automatic test circuits provide a remotely activated data-loopback mode, check the data-transmission path for loss of signal, signal quality, and level, and manually activate local data-loopback modes. A stand-alone version of the ODS-306+ sells for \$1,000, while a rack-mountable version is priced at \$900. Delivery takes six weeks.

Phalo/OSD, 9240 Deering Ave., Chatsworth, Calif. 91311. Phone (213) 998-3177 [403]

System makes conversations of eight users secure

The Digital Voice Exchange operates over standard dial-up telephone lines and enables users to connect as many as eight phones at any one site to a secure voice system. Specifically, while assuring privacy, it lets users conduct one-on-one conversations or employ up to eight phones at any site for conference calls. It can also serve as an internal secure intercom line. Unanswered calls are automatically sent to an attendant. The



Electronics / November 3, 1981

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4.4-5.0 GHz 1 KW CW
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6.2-6.6 GHz 200 KW .37 uS
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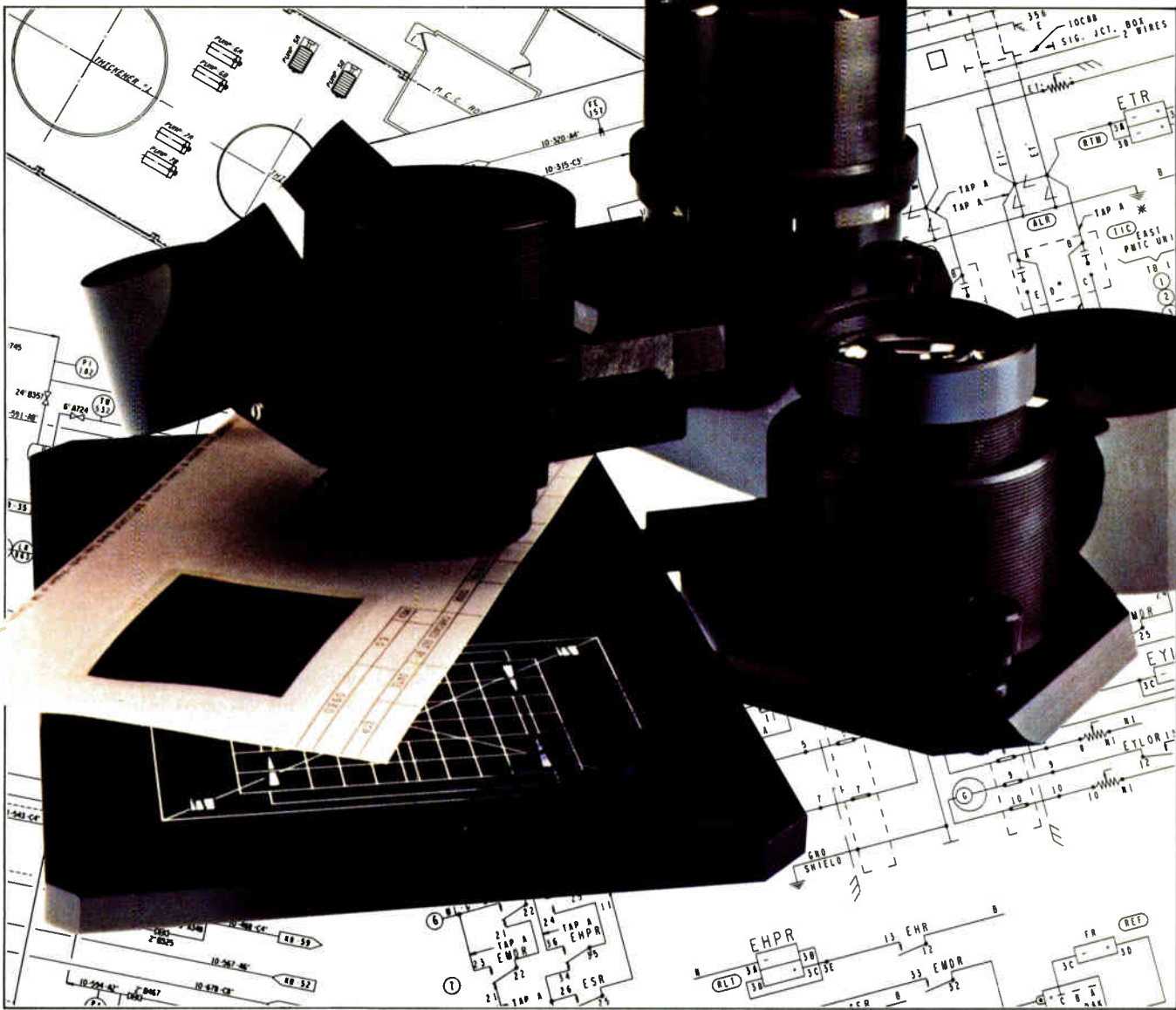
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The 2490 series is a family of high accuracy, 3½-Digit LCD panel meters with outstanding readability and minimum power consumption. Designed to solve your applications problems, it will interface with the most popular transducers. For complete details write to our Weston Literature Center, 614 Frelinghuysen Ave., Newark, NJ 07114

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New products

DVX can operate with Time & Space Processing's model 200 voice digitizer, and for secure voice applications a modem and user-furnished encryption unit may be used in conjunction with the equipment.

The DVX model 280 sells for \$6,875 and can be delivered in 60 days.

Time & Space Processing Inc., 10430 North Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-2200 [404]

Codec and filter join forces on one chip

A fully integrated coder-decoder and transmit-receive filter are combined on a single integrated circuit for use in a range of high-performance telecommunications applications. The resulting codec-filter combination chip, the synchronously clocked Intel 2913 or asynchronous 2913, encompasses the functions of two complex discrete codec and filter chips previously offered by Intel—the 2910A/2911A and 2912A.

The high-performance-MOS encoder internally samples the output of its own transmit filter and holds each sample in a special capacitive network. If there is any offset in dc current between sampling periods, an on-chip auto-zeroing circuit corrects for the difference. No external components are required by the circuit to perform sample, hold, and auto-zero functions.

Only clock and frame sync buffers are enabled in the power-down mode, keeping power consumption to 10 mW. In actual usage, the power-down mode may be in effect for up to 90% of the time; with power on, the chip uses 175 mW. In fixed mode, timing rates are either 1.536, 1,544, or 2.048 MHz. Variable-mode data rates can range from 64 kHz to 4.096 MHz. Available in sample form in the fourth quarter, the 20-pin 2913 and the 24-pin asynchronous model will sell for \$28.95 in lots of 100.

Intel Corp., 5000 W. Williams Field Rd., Chandler, Ariz. 85224. Phone (602) 961-2856 [405]



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- Z8613—4K EPROM Protopak
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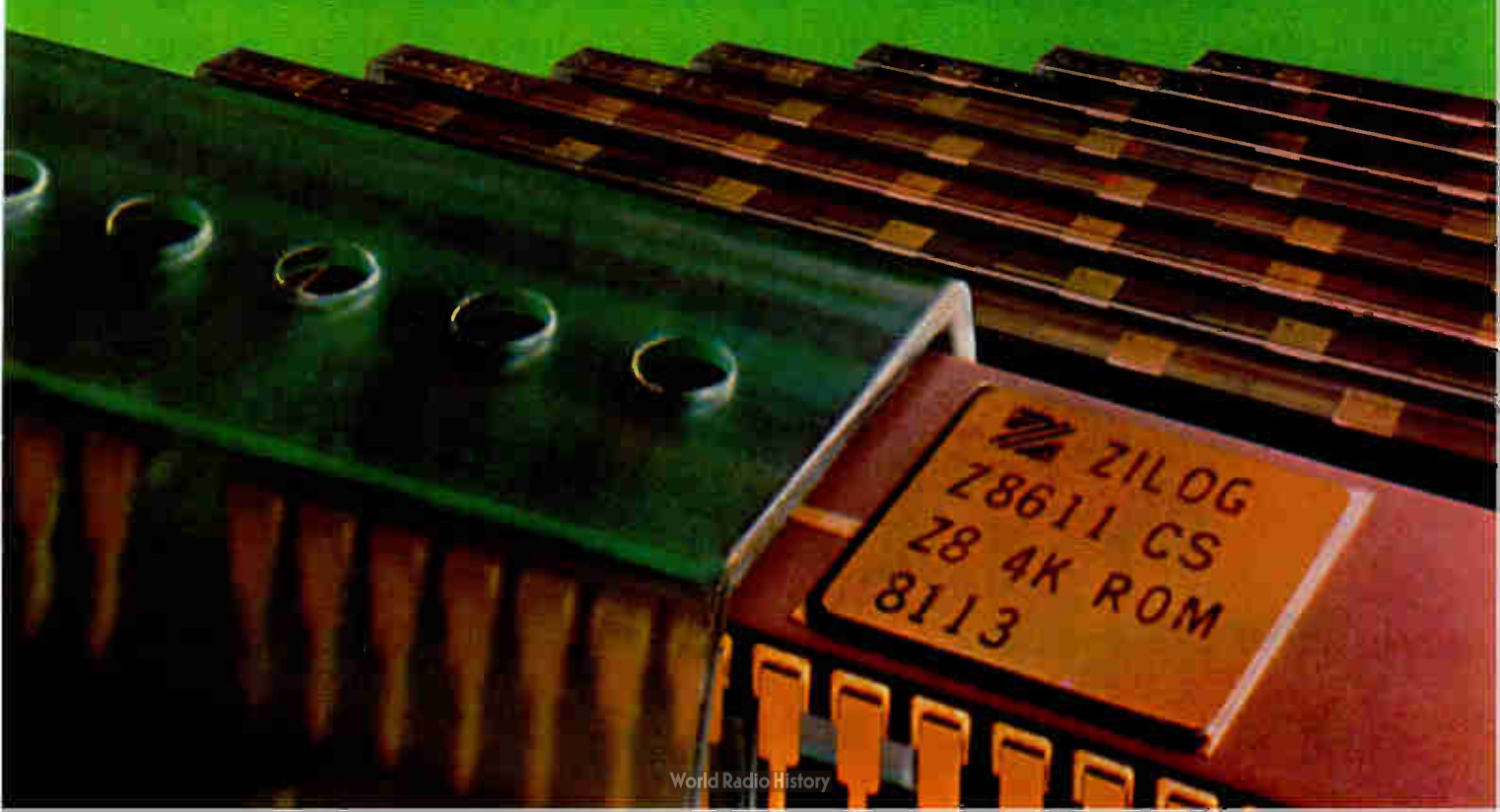
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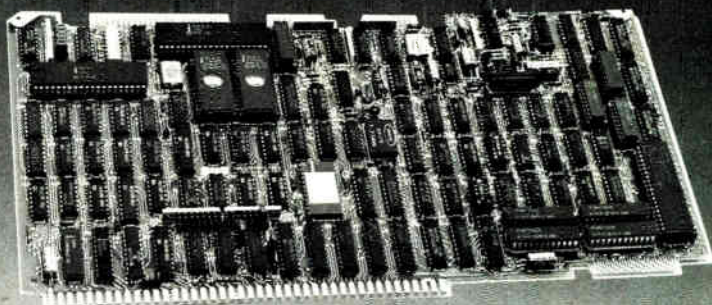
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Z8 and Protopak are trademarks of Zilog, Inc.

Circle 207 on reader service card



SMS' FWD8001 MULTIBUS* WINCHESTER/ FLOPPY DISK CONTROLLER



COMPATIBILITY

- INTEL iSBC* 215A/iSBX* 218 interface and command compatible.
- Direct connection to two Shugart/Quantum 8" Winchester drives, and two Shugart floppy disk drives.
- Supports IBM 3740 single density, IBM 2/2D double density and INTEL SBC 202 floppy formats.

RELIABILITY AND DATA INTEGRITY

- 40% fewer IC's than INTEL 215A/218
- Patented PLL circuitry recovers worst case bit shifted data.
- On-board controller and drive self test
- 6 bit burst error correction code (ECC).
- Automatic error retry recovers soft errors

PERFORMANCE

- Multisector DMA data transfer.
- Optional buffer transfer and disk interleave formats.
- Fast 63K byte/sec floppy disk data transfer.

AFFORDABILITY

- Requires only +5 volts input power.
- Eliminates costly external data separator and special cables.
- Requires only one Multibus card slot.

SMS Scientific Micro Systems

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Circle 208 on reader service card

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Microprocessor Compatible 20 Column Alphanumeric Thermal Printers from Memodyne Corporation

Parallel Input Model MAP-20P

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- Accepts rates up to 2000 characters per second

Programmable controls for:

- Text or lister printing
- Character size - normal or extended

Price: \$625.00 each in single quantities



Parallel Input Model MAP-20P



Serial Input Model MAP-20S



Serial Input Model MAP-20S

- Simple 2 wire data input
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- Baud rates from 75 to 9600
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 - Character size - normal or extended
 - Baud rate

Price \$725.00 each in single quantities.

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- Print rate of 2 lines per second
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- Small size measures 4.4" W x 2.75" H
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Only the CD100M
now supports
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in the perfect
desktop package.



Hear this,
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Only the CD100L
emulates a VT103,
an RL02 and an
RX02 in a single
desktop package.

And both now include a 10 megabyte Winchester!

CD100M — THE TOTAL OEM SOLUTION

To give your Multibus microcomputer system increased file storage, the Callan™ CD100M Integrated Work Station now includes a high performance 10 Mbyte 5¼-inch micro Winchester disk drive complete with full DMA and fully automatic and transparent burst error correction. A one Mbyte unformatted floppy provides file entry and back-up. With its integral 6 slot Multibus compatible card cage, intelligent video terminal, and Winchester/Floppy disk system, the CD100M is the *only* single desktop package available to OEM and volume end-users who wish to configure a modular micro-computer system using any Multibus compatible card set. It's the perfect solution, significantly reducing product costs and development time.

CP/M AND CP/M86 CONFIGURATIONS

If you prefer the popular CP/M operating system, Callan can provide the CD100M with either 8-bit or 16-bit micros. A Z80 with 64K RAM and CP/M, or an 8086 with 128K RAM with error correction and CP/M86 are both available as the complete solution for CP/M compatible software. And both systems include 10 Mbyte Winchester performance.

If you're using Multibus cards in your system you must see the Callan™ CD100M Integrated Work Station.

CP/M and CP/M86 are trademarks of Digital Research. Multibus and 8086 are trademarks of Intel Corp. Z80 is trademark of Zilog.

CD100L — COMPLETE DEC COMPATIBILITY

For the OEM or end-user configuring an LSI-11 system, only the Callan™ CD100L Integrated Work Station can emulate a 10 Mbyte RL02 Winchester disk, a 0.5 Mbyte RX02 floppy, and a VT103 Terminal in a *single* desktop unit. Software presently running on RT-11, RSX-11 or other LSI-11 operating systems can now run on the CD100L, reducing hardware costs by as much as 30%. For users who prefer a more complete solution, the CD100L can also be ordered complete with LSI-11/2 or LSI-11/23 and RT-11.

MORE FOR LESS

No other solution compares for performance, features and price. The VT100/VT52 compatible terminal offers 6 video attributes, true split screen with separate scrolling regions standard. The LSI-11 Q-bus compatible card cage provides 7 quad or 14 dual height slots to house even the largest configurations. A Winchester controller is available to directly emulate the 10 Mbyte RL02. RX02 emulation is available either in a 1 Mbyte dual floppy configuration or as 0.5 Mbyte back-up for the Winchester.

If you're tired of multiple package or multiple vendor solutions, you must see the CD100L.

DEC, LSI-11, VT103, RL02, RX02, RT-11, RSX-11, VT100/VT52, LSI-11/2, LSI-11/23 are trademarks of Digital Equipment Corp.

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Circle 209 on reader service card



Built-in card cage holds 6 Multibus or 7 quad/14 dual height LSI-11 cards.

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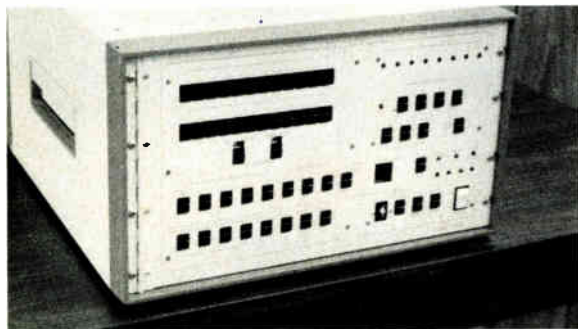
World Radio History

Instruments

**Memory tester
is easy to use**

Unit requires no programming,
has addressing capability for
256-K and larger devices

Incoming inspection, pre-burn-in, and post-assembly memory tests may be easier and less costly thanks to a new benchtop memory tester from Semiconductor Test Technolo-



gies Inc. Using TTL instead of a microprocessor as its test-pattern generator, the tester covers a broad range of device timings and specifications. The EMT-200 needs no programming, so less skilled operators can run the system, notes company president Toby Byrd. "The EMT-200 is also designed so that it can be maintained by the lowest-level technician on the floor," Byrd says.

Tests are set up on a simple front-panel control board. The operator selects the memory size and timing group, then starts the testing. The EMT-200 can check random-access memories, read-only memories, and programmable ROMs with up to 12 address lines. Its 24-bit addressing capability (12-bit column and 12-bit row addresses) allows the unit to accommodate upcoming parts with 2^{24} locations. The tester can be used for devices with TTL-compatible input/output and access times ranging between 200 ns and 1.3 μ s.

The tester, which connects to a single dual-in-line-package handler

via a 50- Ω coaxial cable, is capable of dc parametric testing for open and short circuits. Continuity testing is executed on a pin-to-pin basis, forcing -1 v and measuring greater than 50 μ A at the device pin. Short testing is also performed pin-to-pin. Functional tests are conducted with an algorithmic generator that develops a standard march pattern.

To switch the system from RAM to ROM testing, the operator merely pushes a button on the front panel, which reduces the functional march pattern from five passes to a single pass. The system can handle ROMs and PROMs with up to eight data channels, five clocks and three power supplies. The supplies provided are +5 v at 500 mA, -5 v at 500 mA, and 12 v at 500 mA. Each test channel of the EMT-200 tester can automatically switch among three functions: parametric, functional, or system ground. The user can choose from four sets of timing, and each system test clock is adjustable by a potentiometer and voltage network.

The EMT-200, which is Semiconductor Test Technologies' first product, can test a typical 16-K device in 182 ms (not including the time required by the handler)—82 ms for functional and 100 ms for parametric testing. The unit weighs 40 lb and measures 19.75 by 10.5 by 27.6 in. Power requirements are 108 to 120 v ac at 10 A.

The EMI-200 sells for \$25,000 in single quantities and is available for delivery in 90 days.

Semiconductor Test Technologies Inc., Honey Grove, Texas 75446. Phone (214) 378-7311 [351]

**50-MHz pulse generator
sells for just \$5,195**

A new 50-MHz programmable pulse generator offering dual-channel and summing options beats its competitors' price by 50%, according to its

manufacturer. Priced at \$5,195, the 2021 uses a vertical-MOS output amplifier that provides output immunity to short- and open-circuit faults even under high-energy summing conditions.

Designed for both automatic testing and benchtop applications, the model 2021 has a frequency range of 10 Hz to 50 MHz, a ± 20 -v output per channel, and transition times as low as 5 ns. Its memory can hold up to 10 complete settings for a particular pulse signal including duty cycle, voltage output, and pulse mode.

Standard features include continuous automatic calibration of frequency, voltage levels, delay, and width, as well as easily operated controls and displays and an IEEE-488 interface. The summing option combines both outputs of a dual-channel 2021D into a pulse of up to ± 40 v peak to peak. The dual output option provides a second output channel with independently programmable voltage levels, output impedance, waveform, delay width, duty cycle, and transition times.

Interstate Electronics, 1001 E. Ball Rd., Anaheim, Calif. 92803. Phone (714) 635-7210 [353]

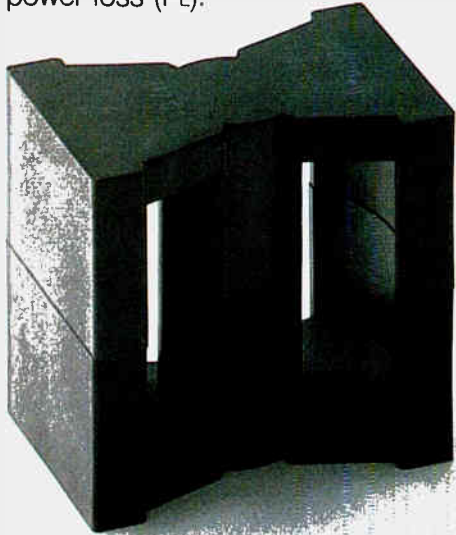
**Recorder permits packing
densities over 40 kb/in.**

The SE9000 tape recorder-reproducer for laboratory instrumentation comes with a built-in tape cleaner and offers a coding and formatting subsystem. It permits linear packing densities over 40 kb/in. for high-density digital recording using standard Inter-Range Instrumentation Group wideband headstacks. Bit-error rates are better than 1 in 10^8 using an error-correction system. The recorder is available with interchangeable modules for IRIG intermediate and wideband direct and frequency-modulated recording as well as voice, calibration, and shuttle modules. A servo reproduce module provides an equalized output from both bias and saturation recorded signals. A complete 42-channel record-and-reproduce system can be

ALTERED SPACE

With the PQ* core, TDK has come up with an original shape.

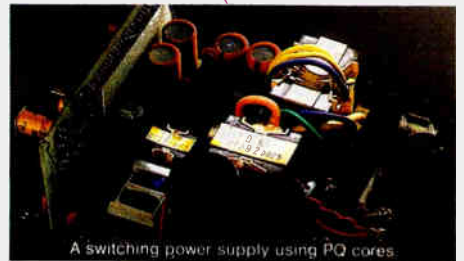
It is characterized by improved performance and power saving due to the use of H7c1 power ferrite material which has high saturation magnetic flux density (Bs) and low power loss (PL).



Another feature of the PQ core is its compactness.

For example, it occupies only 60% as much space as the EC core in a transformer.

This allows for a more effective use of space and a reduction in the overall size of the power supply.



A switching power supply using PQ cores

*PAT. PENDING

Circle 211 on reader service card

 **TDK**

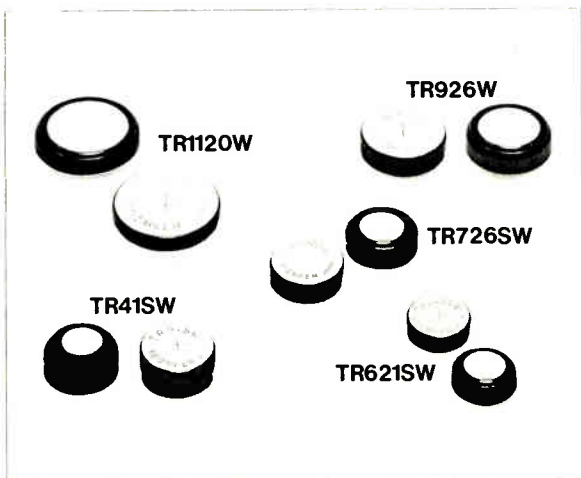
TDK ELECTRONICS CO., LTD. 13-1, Nihonbashi 1-chome, Chuo-ku, Tokyo 103, Japan Phone: Tokyo (03) 278-5111 Telex: J24270, J26937 (TODENKA)
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DAINI SEIKOSHA develops and manufactures high capacity button type silver oxide (II) batteries for wristwatches not available from anyone else. Our silver oxide (II) battery is a highly reliable battery based on our high level technology and fully satisfies all users.

[Specifications]

TYPE	TR621SW	TR721SW	TR726SW	TR1120W
CHEMICAL SYSTEM	AgO/NaOH	AgO/NaOH	AgO/NaOH	AgO/NaOH
VOLTEGE	1.55V			
CAPACITY	16mAH	23mAH	30mAH	
DIMENSIONS (mm) (Dia. x Height)	6.80 x 2.15	7.87 x 2.10	7.87 x 2.70	

TYPE	TR926W	TR41W	TR726W	TR1120W
CHEMICAL SYSTEM	AgO/KOH	AgO/KOH	AgO/KOH	AgO/KOH
VOLTEGE	1.55V			
CAPACITY	50mAH	45mAH	30mAH	45mAH
DIMENSIONS (mm) (Dia. x Height)	9.50 x 2.70	7.87 x 3.55	7.87 x 2.70	11.56 x 2.05

[Features]

- (1) The quantity and size matched to the user's needs can be selected.
 - Both large volume and small volume orders can be filled.
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 - Both high drain and low drain types are available.
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New products

contained in a single 6-ft cabinet.

The SE9000 accepts reels up to 16 in. in diameter, is specified for 7-, 14-, 28-, 32-, and 42-track formats in all recording modes, and provides nine electronically switchable tape speeds from 15/16 in./s to 250 in./s. All system functions except power on-off are remotely controlled by the standard parallel TTL interface or the optional IEEE-488 interface. The built-in tape cleaner, the first in the industry according to the company, is standard.

Prices vary for the system selected and begin at \$25,000.

EMI Technology Inc., 6445 Powers Ferry Rd., Atlanta, Ga. 30339. Phone (404) 952-8502 [355]



Coupler makes instruments IEEE-488-compatible

Now a low-cost series of couplers provides bidirectional talk-listen data links between parallel IEEE-488 bus and parallel binary or binary-coded decimal data for upgrading existing instruments that are not IEEE-488-compatible. The model 4880 can also put measured data on the IEEE-488 bus or control instruments from the bus. Further, the couplers eliminate the need for custom interfaces and thereby simplify



At AMI, all chips are created equal: 0.1% AQL or better.

Contrary to popular belief, quality in America is not an endangered species.

The industry's highest in-house standard. AMI tests every product to a 0.1% Acceptable Quality Level (AQL). Every product will meet that standard, or we won't transfer it to manufacturing. And we're ready and able to test to even more stringent specifications—and constantly working to tighten our own standards.

Since we're talking about our most complex, most powerful custom MOS/LSI circuits, too—not just ROM's, RAM's, catalog or

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Productivity and quality for all.

AMI's 0.1% AQL puts you in a superior competitive position, too. Assembly costs come down, because there's less reworking on your line. And most important, your customers enjoy a more reliable product. AMI's quality may be just the thing to get your products off the ground. To find out, call Gordon Morrison, Director of Product

Assurance at (408) 246-0330, Ext. 2736. Or write him at AMI, 3800 Homestead Road, Santa Clara, CA 95051.

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(FOR CIRCUIT PROTECTION)

● POINT

- (1) Usable at wider ambient condition, especially good under high humidity
- (2) Visibility for operation
- (3) Compact and easy assembly
- (4) Stable characteristics

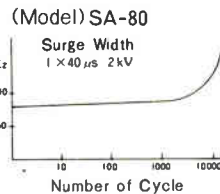
● APPLICATION

- Computer circuit
- Communication equipment
- Home Appliance
- Aircraft and Automobiles

● TYPE

Type	Breakdown Voltage (V) dc	Insulation Resistance (Ω)	Maximum Surge Current ($8 \times 20\mu s$) KA	Life Times at 500A
SA-80SS	80 \pm 10%	10 ⁷ min	0.7	3000
SA-200SS	200 \pm 10%	10 ⁷ min	0.7	3000
SA-80	80 \pm 10%	10 ¹⁰ min	1.5	3000
SA-140	140 \pm 10%	10 ¹⁰ min	1.5	3000
SA-200	200 \pm 10%	10 ¹⁰ min	1.5	3000
SA-250	250 \pm 10%	10 ¹⁰ min	1.5	3000
SA-300	300 \pm 10%	10 ¹⁰ min	1.5	3000
SA-7K	7000 \pm 1000V	10 ¹⁰ min	—	5000
SA-10K	10000 \pm 1000V	10 ¹⁰ min	—	5000

Change of Ez by cycling discharge



● MAIN PRODUCT

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MINIATURE : BLACK-LIGHT, UV-LIGHT, FLUORESCENT COLOR-LIGHT.

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Circle 214 on reader service card

New products

the development of unique automatic test systems.

The 4880 couplers operate with most BCD instruments, and an extensive program and cable library is available for unique instruments. Each coupler has a rear-panel address switch for setting the coupler's bus address as well as front-panel talking and listening lights for checking visual operation.

The units have 16 active lines—8 data lines and 8 lines for control and status messages. Data is transferred at 5 kb/s. The 4881 talker and 4882 listener are priced at \$795 each; configured as the 4883 talker-listener, the coupler is \$895. Delivery takes 30 days from receipt of order.

ICS Electronics Corp., 1620 Zanker Rd., San Jose, Calif. 95112. Phone (408) 298-4844 [356]

Unit measures, displays, and prints bit-error total and rate

A measurement system called the Berts-25 provides bit-error information on digital communications systems using coaxial or fiber-optic cable and related equipment. The unit operates from 100 Hz to 25 MHz, has programmable 16-bit words in addition to seven pseudo-random sequences of 2⁷ to 2²³ bits, and includes a real-time clock and built-in printer for long-term tests.

The system sports both a synthesizer-controlled transmitter and an automatic receiver and measures both the total number and the rate of bit errors, displaying both figures simultaneously. The 20-column printer also logs the time of day and various status conditions.

The receiver features automatic and manual pattern selection and synchronization, measurement start time and duration, and input-clock frequency measurements. An IEEE-488 interface is optional and a choice of 50- Ω TTL or 124- Ω Mil-Std-188-144 input/output is offered. The Berts-25 is priced at \$11,900 and delivery takes 8 to 12 weeks.

Tau-Tron Inc., 27 Industrial Ave., Chelmsford, Mass. 01824 [357]

MAGSTRIPE™



CARD READERS & READER / ENCODERS

Known world-wide for proven performance and unequalled reliability.

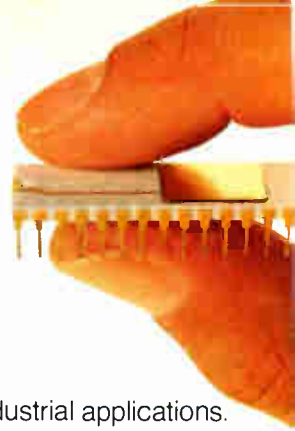
MAGSTRIPE™ CONTROLLER—Unequaled flexibility to interface Readers and Reader/Encoders with your system.



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- First supplier of Mil-M-38510 to attain Class A certification
- First Class S, Part-1 supplier of CMOS rad-hard devices

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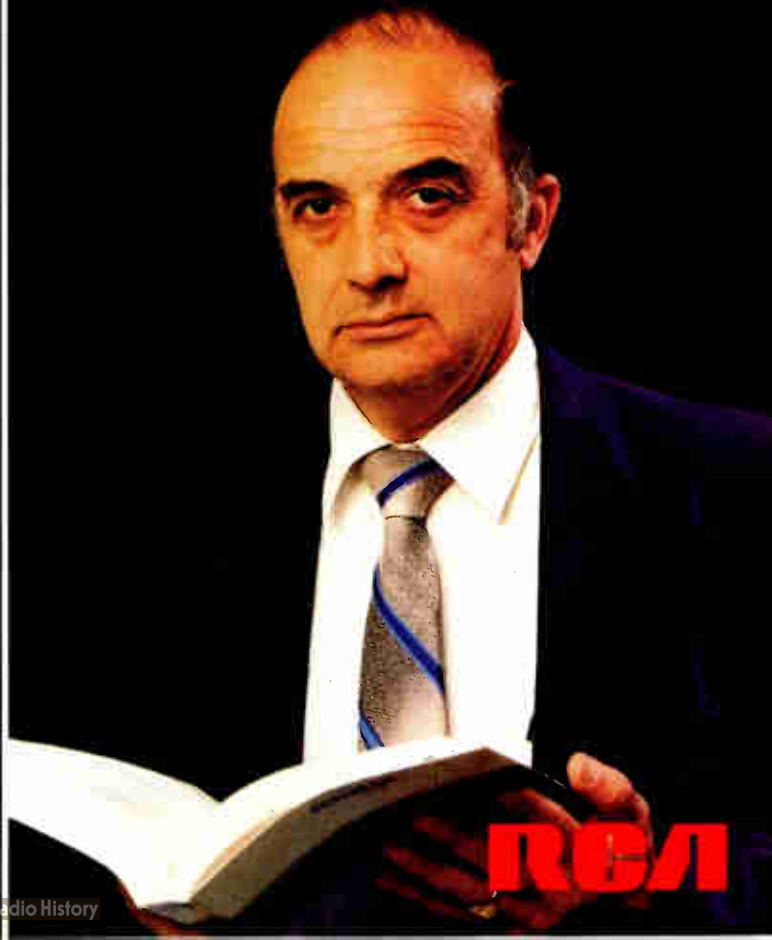
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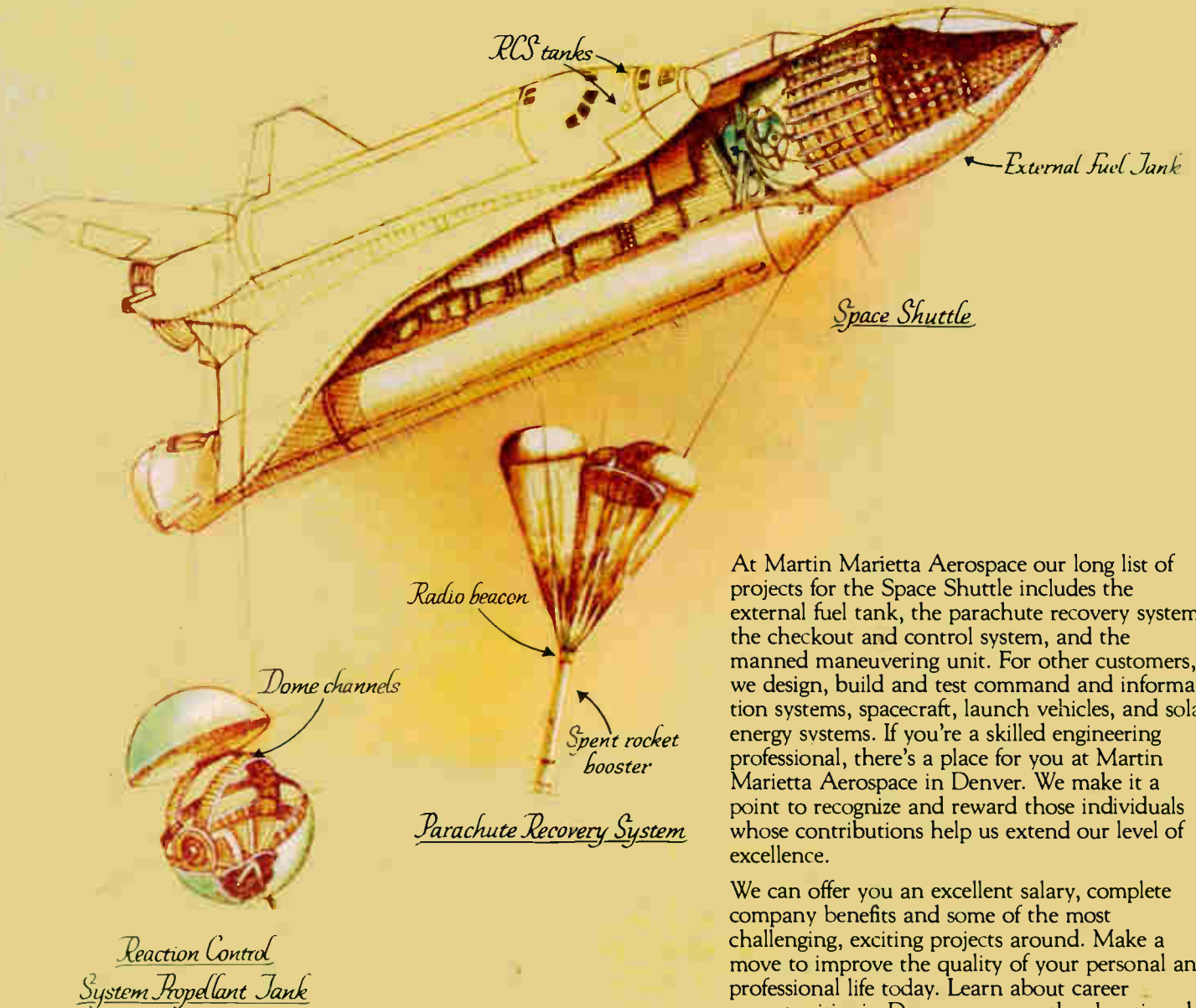
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Parameter	Character number (character x line)	Unit outline WxHxD (mm)	Character size WxHxD (mm)	Supply Voltage (V)
* LM-06151	6 Character. 1 Line	60x40 x 14.5	4.8x7.5	+5,
* LM-14151	14 Character. 1 Line	93x47 x 13.5	2.65x3.75	+5,
LM-24102	24 Character. 1 Line	175x46 x 12	3.3x5.05	+5, -5
* LM-24151	24 Character. 1 Line	174x51 x 13.5	3.3x5.05	+5,
LM-40101	40 Character. 1 Line	175x45.4x15	2.32x3.28	+5, -5
* LM-40151	40 Character. 1 Line	177x46 x 13.5	2.32x3.28	+5, -5
LM-40201	40 Character. 2 Line	230x50 x 15	3.4x4.8	+5, -5
LM-80101	80 Character. 1 Line	310x90 x 12	2.32x3.28	7V-13.5V

* Select the character combination appropriate for the number of lines required for the read out.
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Driver ICs also available.



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New products

Micromputers & systems

Tnix aids system development work

Multiple-user development system's Unix-like operating system helps coordinate team

The 8560 multiuser universal development system is now available from Tektronix Design Automation division. It joins the 8550 single-user system and the 8540 host integration unit, which is used for emulation and debugging. The 8560 uses Bell Laboratories' Unix version 7 operating system enhanced and renamed Tnix by Tektronix and employs a Digital Equipment Corp. LSI-11/23 processor in conjunction with front-end input/output processors to offload

also has a 1-megabyte floppy-disk drive and a 35-megabyte Winchester drive.

Work stations can be standard cathode-ray-tube terminals, but the preferred station is an 8540 for integration and debugging because it is optimized to communicate with the 8560. With the 8540s users also have the ability to perform real-time transparent emulation of many 8- and 16-bit processors.

The heart of the 8560 is the Tnix operating system. Tnix has a hierarchical file structure whose easily shared files aid the coordination of complex program development. Tnix has password protection, so that file owners can either make their files public or restrict them to read-only or execute-only access. Design team members can thus use working copies of files in their development work and permit alterations to the permanent copy to be made only by some users, such as team leaders.

With Tnix, multiple tasks can be performed concurrently. For example, a user can simultaneously have a file printed while another is being assembled and edit yet a third, maintaining throughout full control over task priorities to maximize use of the system's resources. A front-end menu called Guide prompts the user, but standard Unix syntax can also be used, if so desired.

Another utility program, called Make, tracks files that are interdependent so that modifications to one file automatically update dependent ones. This prevents bugs from creeping into programs built up from several modules. Make uses the time and date on each file to keep track.

The 8560 is \$27,500 with four ports; deliveries start in January. Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075 [371]

those functions. Intel 8088s handle each set of four I/O ports, and Z80s handle disk control. Each terminal I/O port can operate at speeds up to 9,600 b/s through RS-232-C interfaces or an optional interface that operates at 153.6 kb/s over a distance of up to 2,000 ft. The 8560 can support up to eight work stations and two spooling printers. It has 128-K bytes of main memory, which can be expanded to 256-K bytes. The unit

Microcomputer piggybacks E-PROMs over 1-K byte

The NS87P50 single-chip microcomputer has a piggybacked erasable programmable read-only memory that can emulate not only the 1-K-byte INS8048, as only on-board E-PROMs do, but also the 2-K-byte INS8049 and the 4-K-byte INS8050. Fabricated using National's proprietary XMOS process and housed in a 40-pin dual in-line package, the NS87P50 contains 27 input/output lines and the system timing to implement prototype program development and emulation.

The unit includes a plug-in adapter that also accepts the 2758, the 2716, or the 2732 24-pin E-PROM and a program module (IPM) that selects the mode of operation—either the INS-8048, which allows the use of 64 bytes of resident random-access memory, the -8049 allowing for 128 bytes, or the -8050 for 256 bytes. The program memory mounted on the top of the processor is 1-, 2-, or 4-K bytes of PROM.

The NS87P50 is priced at \$125 in quantities of 1 to 24. In quantities of 100 and up, it is priced at \$87.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [373]

Multifunction card cuts cost, saves space

The CPS multifunction card serves as a serial interface, a parallel output interface, and a real-time calendar/clock. Designed for the Apple II computer, it is almost one half the cost of the three, four, or even five cards it can replace in different user applications, according to the card's manufacturer.

The multifunction card is configured from a program that sets parameters, such as the bit rate, for all card functions and stores them in battery-backed complementary-MOS random-access memory. Once the parameters are established, they





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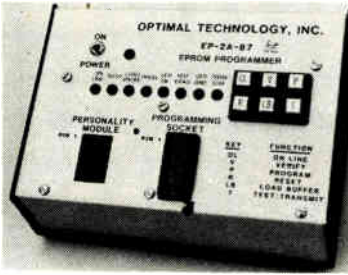
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The Model EP-2A-87 EPROM Programmer has an RS-232 compatible interface and includes a 2K, 4K or 8K buffer. Seventeen RS-232 commands allow another computer to download or remotely control the Programmer. INTEL, TEXTRONIX OR MOTOROLA formats are supported. The buffer may be edited directly from a CRT and EPROMS can be copied off-line. Power requirements are 115v 50/60 Hertz at 15 watts.



EP-2A-87-1	Programmer with 2K Buffer	\$575.00
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EP-2A-87-3	Programmer with 8K Buffer	\$725.00
	Non-Standard voltage (220v, 240v, or 100)	\$ 15.00

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PM-3	TMS 2716	26.00	PM9	2764	36.00
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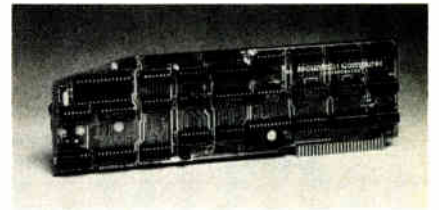
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New products

need not be set up again, though they can be changed by control commands from the keyboard.

Each function of the CPS can be assigned to different slots in the Apple II without the card actually being in that given slot. This on-board intelligence lets the card function in a wide variety of configurations, thus providing software compatibility with most existing programs. The card sells for \$239, with delivery from stock to two weeks.

Mountain Computer Inc., 300 El Pueblo Rd., Scotts Valley, Calif. 95066. Phone (408) 438-6650 [374]



Z8002-based system

develops in Pascal and C

The DPS-8000 16-bit multiuser development system is designed for systems integrators, application program developers, industrial and scientific laboratories, and educational institutions working under Unix. In addition to the standard commands, utilities, and operating characteristics of Unix, it includes compilers for Pascal and C, as well as loadable device drivers, bounded interrupt lockout time, and the handling of pipes in memory rather than input/output.

The DPS-8000, based on the Z8002 processor, incorporates the ZMU interrupt-driven memory management device, four parallel and eight serial I/O ports, and 256-K of random-access memory, not to mention parity and controller boards for floppy-disk drives with a 1.2-megabyte capacity and Winchester hard-disk drives with 10 to 40 megabytes of storage.

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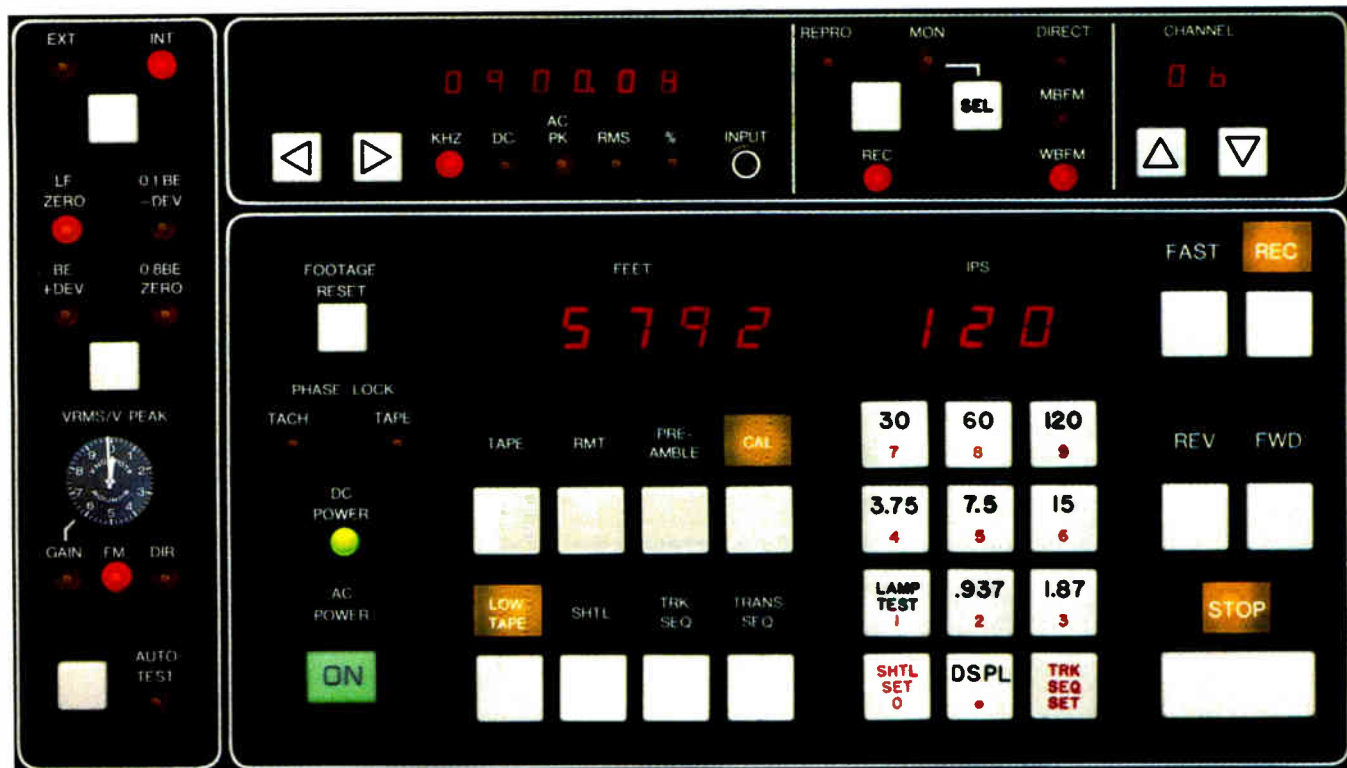


Activate AUTO TEST and the Model 101 will automatically check itself and tell you what, if anything, needs adjustment. Other controls bring into play programmable, automatic tape management and data handling features such as selective track recording, shuttle and transport sequencing and preamble.

For remote operation, there's a choice of three popular interfaces: RS-232C, RS-449, or IEEE-488. Other features of the Model 101 include long-life solid ferrite heads; eight tape speeds from 15/16 to 120 ips; up to 28 data channels; and 15" reel capacity for up to 32 hours of recording.

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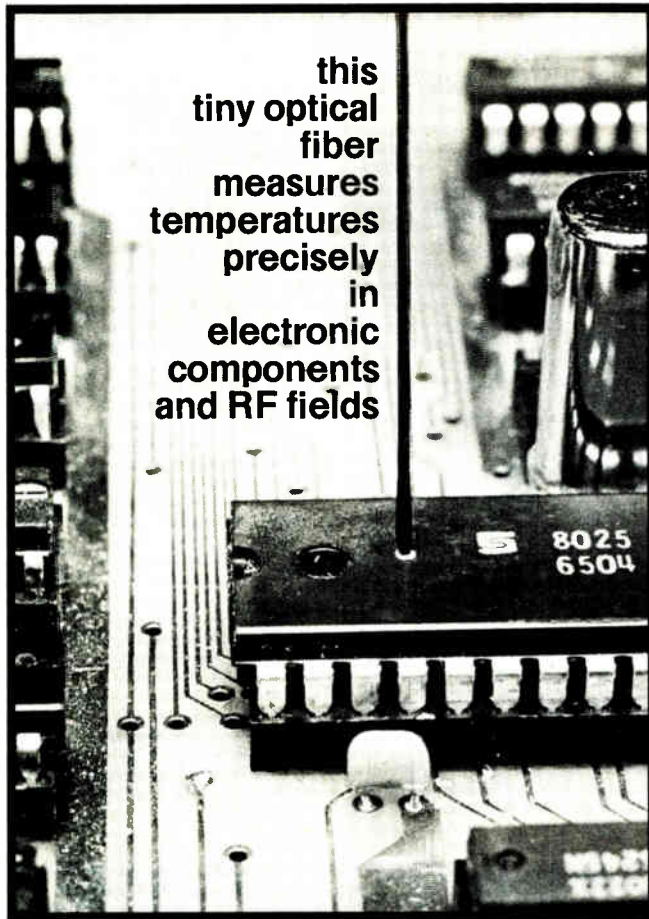
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Ithaca Intersystems Inc., 1650 Hanshaw Rd., Ithaca, N. Y. 14850 [375]

Custom 86 and GPC 86 take on memory management

The MM86 memory module gives the Custom 86 and GPC 86 series 16-bit single-board computers memory management without any re-design of the board. The unit plugs directly into the 8086 socket on either board and has two 8086 modes of operation—a system, or privileged, and a user mode.

When used with the GPC series single-board computers, the 86 permits users to combine an 8-MHz 8086 and up to 128-K bytes of random-access memory on a single board with memory management—a more efficient and faster approach to building a system at a low cost, according to the company.

The module can be modified to work with other 8086 designs not based on the IEEE-796 standard. It is currently available for \$495 in single-unit quantities for the GPC 86 version.

Microbar Systems Inc., 1120 San Antonio Rd., Palo Alto, Calif. 94303. Phone (415) 964-2862 [376]

Development system uses logic, trace analysis

The Z1802 complementary-MOS microprocessor development system uses a symbolic emulator-logic analyzer for trace analysis. Incorporating a 64-K microcomputer, it runs under the CP/M operating system and has interfaces available for the

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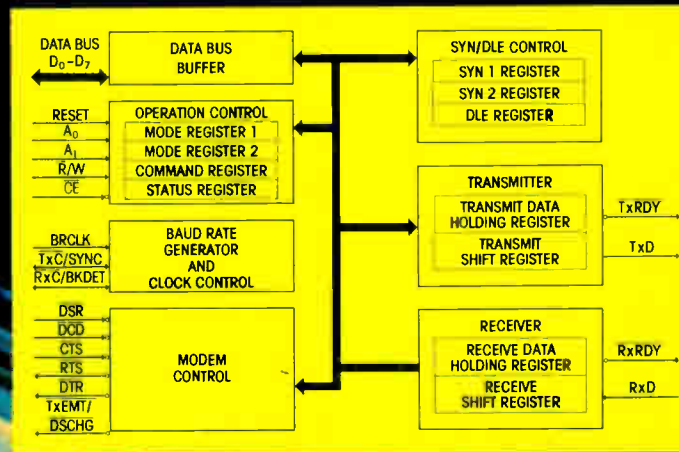
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The Z1802 can be purchased for \$8,995, or separate modules can be added for \$3,995. It is available for the 1802 microprocessor but will be expanded for the 1804, 1805, and 1806 as they become available. Delivery is in six to eight weeks.

Scientific Development Technologies Inc., Naperville, Ill. 60566. Phone (312) 369-6715 [377]


Multibus display board speeds program debugging

The model 1506 Multibus display plug-in board is for use with any Multibus-based system. It helps the user debug by indicating both static and dynamic conditions of program execution. It also automatically holds and displays the last bus cycle executed by the program under development by looking at either the memory read or write or the input/output read or write. Addresses 16 or 20 bits wide, interrupts, and last-data values 16 bits wide are displayed on the front panel by light-emitting diodes.

The 1506 features digital-to-analog conversion of upper and lower input/output addresses with outputs for X-Y mapping of an I/O field displayed in real time on oscilloscopes. Also included are bus-voltage monitoring and a switch for generating an artificial transfer-and-acknowledge signal. Available now, it sells in single-unit quantities for \$495.

LeCroy Research Systems Corp., Spring Valley, N. Y. 10977 [378]


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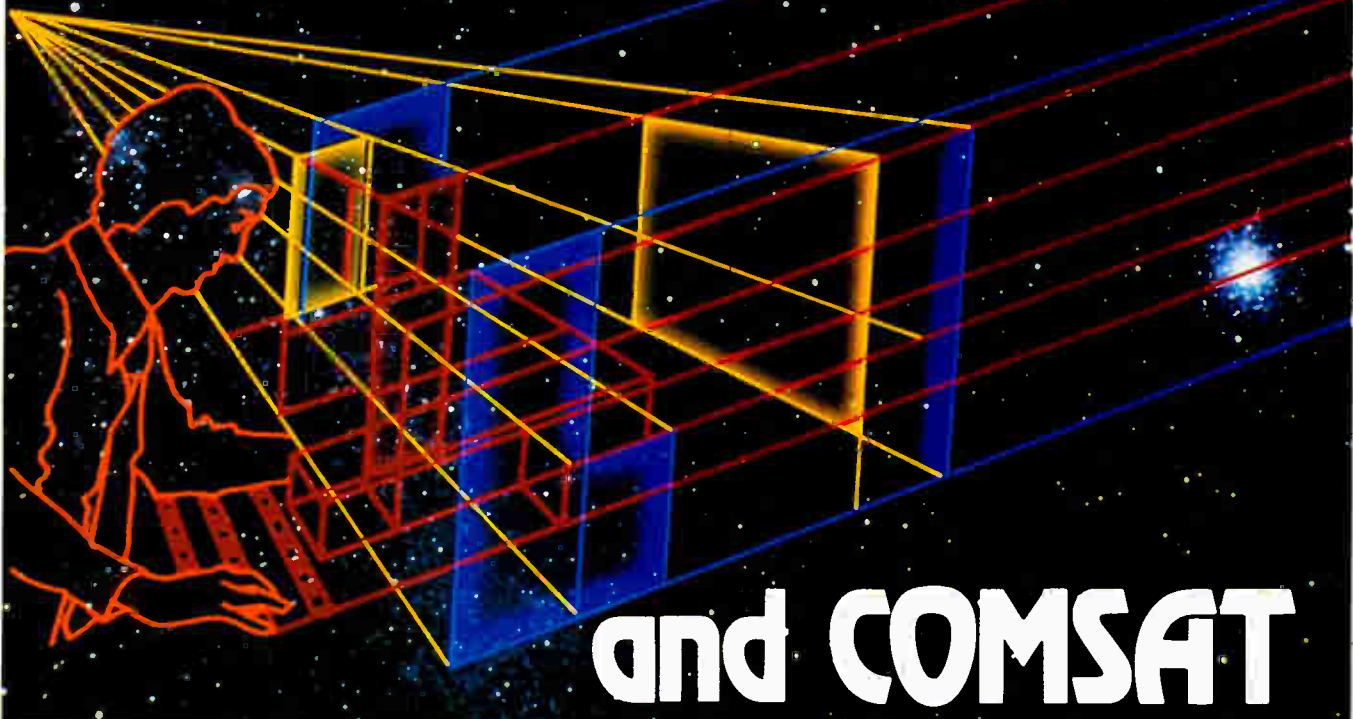
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The 83C silver-bearing solder can achieve a volume resistivity of $0.00035 \Omega\text{-cm}$ as tested recently in a new aerospace application and it is 50% cheaper than previous solders.

These heatless solders range in price from \$0.001 to \$0.014 per $\frac{1}{4}$ -in. dot or bond.

Emerson & Cuming Dielectric Materials, Dewey and Almy Chemical Division, W. R. Grace & Co., Canton, Mass. 02021. Phone (617) 828-3300 [476]

High-performance epoxy resins in the Tra-Con EpoxyLab F/O system are used for bonding glass and plastic fiber-optic bundles, potting fiber optics, bonding ferrules and connectors, and coating optically sensitive components. A 5-min curing adhesive, color-keyed high-temperature adhesive, a flexible polysulfide adhesive, and a high-impact optically clear adhesive, plus two casting formulations, are among the 11 resins in the system.

All two-component formulations are contained in Bipax packages that are designed for convenience, accuracy, and simplicity and to save clean-up time, minimize dermatitis problems, and eliminate compounding and mixing mistakes and epoxy mess.

The Tra-Con EpoxyLab F/O sells for \$52.80.

Tra-Con Inc., Resin Systems Division, 55 North St., Medford, Mass. 02155. Phone (617) 391-5550 [381]



A weatherable black grade of unreinforced 6/6 nylon resin offers a 50% increase in productivity over competitive resins when it is used for small, difficult-to-mold parts that require ultraviolet resistance.

Called Zytel 105F, it has an Izod value of 0.9 ft-lb/in. and an elongation at break twice as high as that of previous resins. It meets military specification 20693B Type II for cable ties used to bundle electrical wires in outdoor applications and carries the Underwriters Laboratories temperature index of 125°C , making it suitable for electrical applications. Other uses are in automotive exterior parts requiring thin walls, interior car knobs and connectors exposed to sunlight, nuts and bolts, and bearing retainer cages.

Zytel 105F nylon is priced at \$2.08 per pound for 40,000-pound truckload quantities.

Du Pont Co., Zytel 105F, Marketing Communications Department, Room X38642, Wilmington, Del. 19898 [477]

Conductive nylon in a 6/6 molding resin is an effective shield against electromagnetic and radio-frequency interference. Plasticon EC-636 provides 20 to 30 dB of shielding effectiveness for electronic enclosures in the 1-to-1,000-MHz range. Typical applications include instrument housings, control modules, calculators, terminal boxes, and hand-held electronic packages.

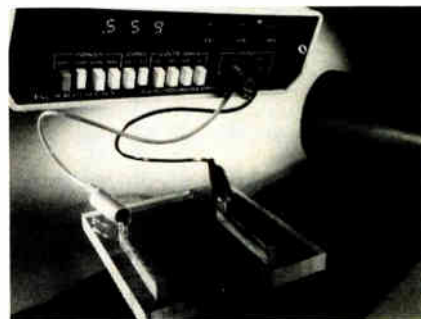
Plasticon EC-636 has a tensile strength of $7,600 \text{ lb/in.}^2$, elongation of 1.4%, flexural modulus of $6.4 \times 10^5 \text{ lb/in.}^2$, notched and unnotched Izod rating of 0.3 and 1.8 ft-lb/in., heat distortion temperature of 466°F at 66 lb/in.^2 , mold shrinkage of 0.005 in./in., and specific gravity of 1.49. These properties are specified under the American Society of Testing Methods. It should be dried by the recommended dehumidifying driers to achieve a water absorption of less than 0.2%. Depending on the quantity purchased, the Plasticon EC-636 is priced from \$8 to \$10 per pound.

Plastic Systems Inc., 88 Ellsworth St., Worcester, Mass. 01610. Phone (617) 799-2600 [479]

A solvent cast film saturated throughout with carbon particles, conducts electricity without metallization and has a volume resistivity as low as $0.36 \Omega\text{-cm}$. Designated as Kimflow, it can be as thin as 2 mm and is resistant to moisture and corrosion by most chemicals and stable up to 130°C . It is primarily a polycarbonate-based film resulting in a constant resistance up to its softening point of 150°C .

Kimflow may be metallized on one or both sides and is available in widths up to 48 in. It can be used by itself or in laminates with other conductive or nonconductive materials. Current application is as a shield or grounding agent to protect microcircuitry from damage by accumulated static charges or electromagnetic interferences. It is in prominent use as dielectric windings in the manufacture of ultraminiature capacitors.

Schweitzer Co., Kimberly-Clark Corp., Lee, Mass. 01238 Phone (413) 243-1000 [480]



Eccosil 4640 silicone rubber cures at room temperature to produce a syntactic foam material that weighs only 47 lb/ft^3 . This foam has less than 0.1% water absorption in a 25-h period, a dielectric constant of approximately 2.0 that is lower than in other silicones, and a 0.01 loss tangent. These properties along with its 500°F operating temperature make it suitable for aerospace applications where it can be used for potting, sealing, and caulking, and as a protective coating against shock and vibration.

Emerson & Cuming Dielectric Materials, Dewey and Almy Division, W. R. Grace & Co., Canton, Mass. 02021. Phone (617) 828-3000 [478]

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| • SP74SC237 | 1 of 8 Decoder with Input Latches | • SP74SC540 | Octal Buffer |
| • SP74SC238 | 1 of 8 Decoder | • SP74SC541 | Octal Buffer |
| • SP74SC239 | Dual 1 of 4 Decoder | • SP74SC563 | Octal Inverted Output, Transparent Latch |
| • SP74SC240 | Octal Inverting Buffer | • SP74SC564 | Octal Inverted Output, D-Type Flip-Flop |
| • SP74SC241 | Octal Buffer | • SP74SC573 | Octal Transparent Latch |
| • SP74SC244 | Octal Buffer | • SP74SC574 | Octal D-Type Flip-Flop |
| • SP74SC245 | Octal Transceiver | | |
| • SP74SC373 | Octal Transparent Latch | | |

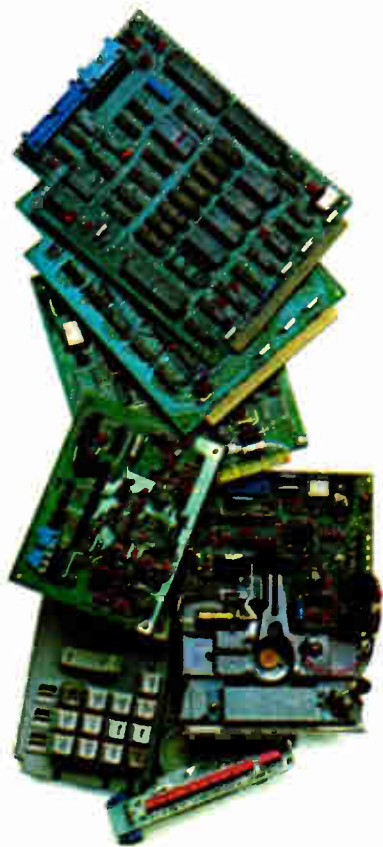
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Data-base applications. "Transferring HP 9845 Image Data Bases," a new application note from Hewlett-Packard, provides guidelines and procedures for shuttling Image data bases between the HP 9845 computer system and an HP 1000 or HP 3000 computer. In addition to general procedures, application note 409 gives detailed explanations of the four Image transfers: Image/45 to Image/1000, Image/45 to Image/3000, Image/1000 to Image/45, and Image/3000 to Image/45. Suggestions for creating a data base compatible with the destination system and a list of the needed equipment are also included. The note is available at no charge from Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304. Phone (415) 857-1501 [422]

Microprocessor chart. "Micro Charts," a comprehensive set of plastic reference charts, gives microprocessor users instruction sets, disassembly tables, ASCII, hexadecimal-to-decimal conversions, compare-versus-jump details, flag effects, interrupt structures, pinouts, cycle times, memory maps, diagrams, addressing, and powers of two. The

8½-by-11-in. charts retail for \$5.95 each, plus \$1 for postage and handling. Orders for charts on the Z80, 6500 series, 8080A, 8085A, 8048, and relatives should be sent to Micro Logic Corp., P. O. Box 174, Hackensack, N. J. 07602. Phone (201) 342-6518 [423]

Power supplies. The 144-page "1981-82 Power Supply Catalog-Handbook" lists Kepco's power-supply products and many applications. The supplies include smart IEEE-488-compatible models ranging up to 1,000 w in single- and four-quadrant styles and multiple-output open-frame switchers. More than 40 pages are devoted to theory and discuss bandwidth, stability criteria, feedback, RS-232-C interfacing, ferroresonance, switching techniques, and measurements. Ask for catalog-handbook No. 146-1402 from Kepco Inc., 131-38 Sanford Ave., Flushing,



N. Y. 11352. Phone (212) 461-7000 [424]

Etching. Etching processes at Tegal Corp. are described in two recently released applications notes. The first describes the process and operating conditions required for etching low-pressure chemical-vapor-deposited silicon nitride over silicon dioxide in Tegal's plasma in-line 700 plasma reactor. "Etching LPCVD Over Silicon Dioxide" has graphs of etch rate versus pressure and power and as a function of oxygen percentage. The

second note describes the dual-step etching of polysilicon performed in the plasma in-line 700 system for high densities and small geometries of very large-scale integrated circuits. For free copies contact Tegal Corp., 11 Digital Dr., Novato, Calif. 94947. Phone (415) 472-7500 [425]

TRS-80 encyclopedia. A 10-book encyclopedia for the TRS-80 contains such practical information as reviews of programs and accessories, ready-to-use programs, and commercial-program-modification and software-writing instructions for the TRS-80. Volume 1 is available in either paperback or hardback copies at computer stores throughout the U. S. or directly from Wayne Green Books of Peterborough, N. H. 03458. Phone (603) 924-7296 [426]

International directory. The "International Microcomputer Software Directory" is a microcomputer-software reference source for all applications and systems. Drawn from a large data base that is continually updated, the directory is divided into three main sections: system and subject classification and software houses. System classification is for users limited to a particular system. Subject classification is for those who can use any system or have not yet purchased a system. The third section lists programs by software house. The complete directory is available for \$29.95 plus \$2.95 postage and packing from Imprint Software, 420 South-Howes St., Fort Collins, Colo. 80521. Phone (303) 482-5574 [427]

CRT capabilities. Four major categories of cathode-ray tubes are described in a 36-page reference manual. Over 55 CRTs are presented, complete with dimensional drawings, features, and applications. An instructional section goes over technical aspects of electron-gun types, contrast-radio calculations, resolution-measurement methods, and display-and-recording-device technology. For a copy of the "Westinghouse Cathode Ray Tube Capabilities and Resource Manual," write Westing-

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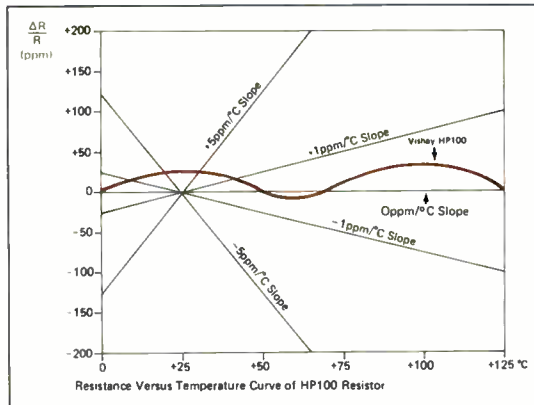
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New literature

house Electric Corp., Electro-Optical Sales, Westinghouse Circle, Horseheads, N. Y. 14845 [428]

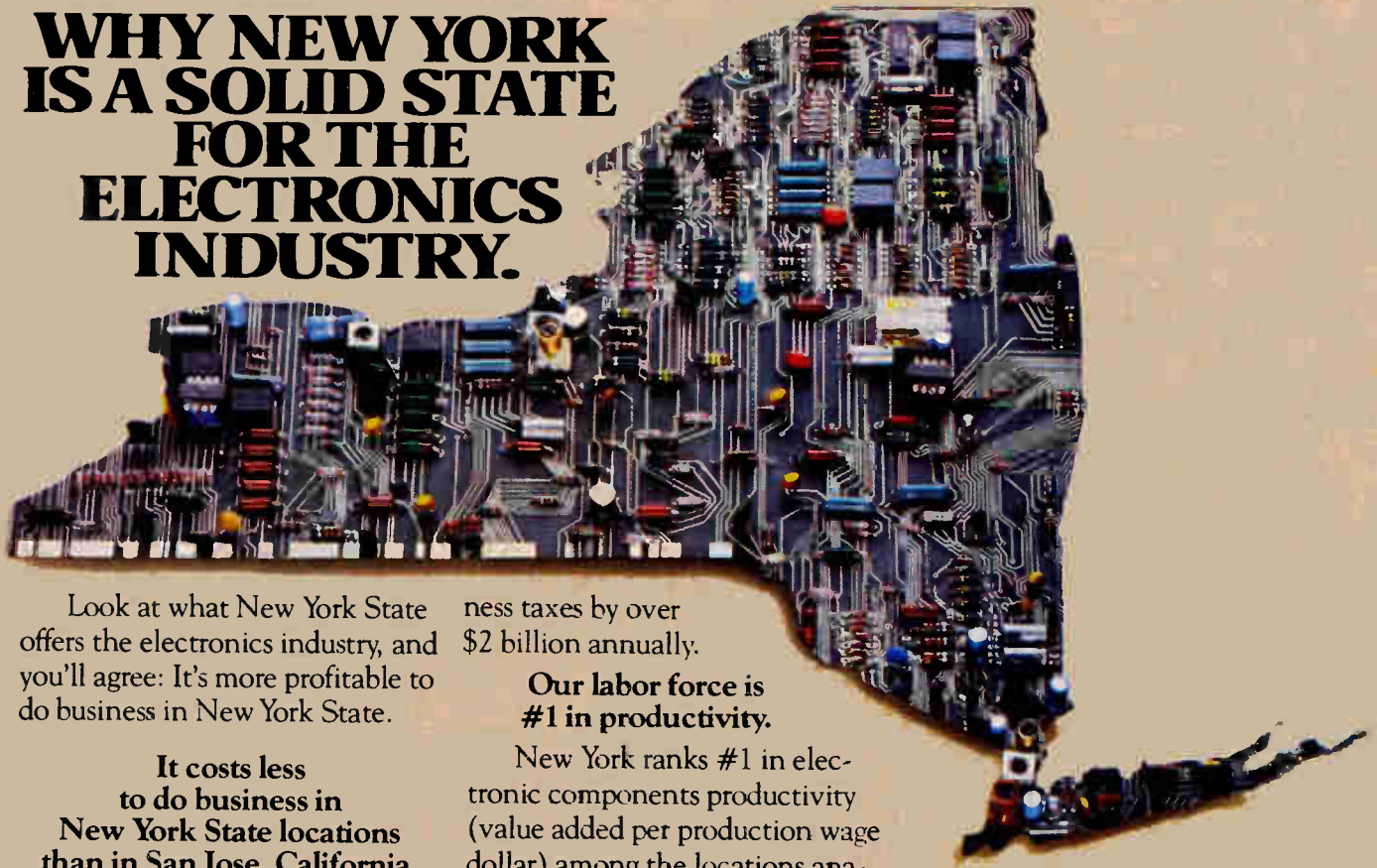


Communications products. A variety of synchronous and asynchronous limited-distance modems, terminal-, port-, and modem-sharing devices, and modem eliminators are listed in "Data Communications Products"—a 40-page catalog of the International Data Sciences line of data-communications equipment. The guide has descriptions, reviews, photographs, and specifications of the listed products. For a free catalog call or write the marketing department, International Data Sciences Inc., 7 Welling Rd., Lincoln, R. I. 02865. Phone (401) 333-6200 [429]

TRS-80 software. "Micro Yellow Pages," a 24-page catalog and newsletter describes business software packages for the model I, model II, and model III TRS-80 under CP/M or Heath HDOS. Issue 3.4, formerly known as the TRS-80 Yellow Pages, can be had for free by sending a long 35¢-stamped self-addressed envelope to Micro Architect Inc., 96 Dothan St., Arlington, Mass. 02174. Phone (617) 643-4713 [430]

SSR uses. The illustrated "Selecting Solid State Relays for Appliance Applications" compares electromechanical relays with solid-state relays in cost, acoustic noise, power, and reliability. It contains data on troubleshooting and make-or-buy decisions. For a copy write Magnecraft Electric Co., 5575 North Lynch Ave., Chicago, Ill. 60630 [431]

WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



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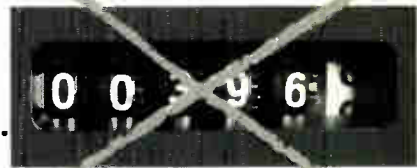


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Important editorial

Intel takes aim at the '80s

Microcomputers will shift from hardware- to software-intensive to ward off otherwise inevitable "programmer catastrophe"

Intel's chief executive officer, San Francisco regional division manager, said 1970s used about 100,000 lines of assembly code to build a hardware cost of just \$100. The software for such systems required about 1,000 lines of assembly language to be written. At a rate of 10 lines of debugged code per man-day and \$40,000 per man-year, this model requires 100,000 man-years and half a man-year and with all the necessary overhead \$30,000 to develop.

"No marketing software today,"



what with memory costing much less, a typical system might use 40 to 45 kilobytes of memory at a hard disk rate of 1320 per byte. These, though, have not been changed. Intel's Gene posits that software costs have risen dramatically. The day's system typically requires eight to 10,000 lines of assembly language or 1,000 lines of a high-level language. At the same number of lines of working code per day and an inflated cost of developing the necessary software, the cost of a man-year is \$400,000 using a high-level language. In a man-year or \$400,000 of developed with assembly language.

Typical customer capabilities will make costs as sky-rocketing. Gene posits that 10,000 lines of code in a system might have ranged from \$100,000 to \$300,000 in the mid-1970s. The system of the 1980s will cost \$100 million customer support costs between \$1 million with manufacturer support and \$5 million with application technology support.

Electronics

SOFTWARE SHAPES VLSI PROCESSOR



A history of the Aloha project

The iAPX 432 32-bit microprocessor has been in gestation for over six years, a third of that time in Santa Clara, Calif and the remainder in Aloha, Ore. There its development eventually became known as the special systems operation, or SSO, with Jean-Claude Cornet as director. But it shrouded of privacy led some to think SSO stood for "secret systems operation."



In the beginning the 432 was called the 8816, then the 8800. It had to be given a number because at Intel, "as soon as you give something a number, it is instantly perceived as this little thing with side-brained connection coming out of it," jokes principal engineer Justin Rattner (see photo). By November of 1975 the endeavor had coalesced into a working unit under William W. Lattin. It remained 432 program manager until April of last year when he moved over to another Intel division.

The original idea was to "do something interesting" with user program code interaction. But with Schottky TTL pro-

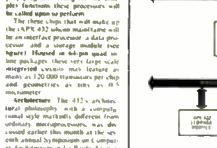
Three-chip mainframe to accompany other Intel processors

by John G. Posa, Solid State, and Richard Cornet, Measurement Equip.

Advanced announcements herald 32-bit computer on three-chip mainframe.

Object-based architecture that has been used by Intel Corp. for the past year or so is what makes the 32-bit three-chip mainframe possible. The 32-bit three-chip mainframe is a high-level development system, and the hardware designer, the hardware engineer, or the software programmer of the system. The hardware engineer will be responsible for the system's architecture.

The three-chip mainframe is a high-level development system. It is designed to be used by the hardware designer, the hardware engineer, or the software programmer of the system. The hardware engineer will be responsible for the system's architecture.



Electronics worldwide editorial announces and interprets all the important technological developments.

Take the Aloha Project.

The first hint was given in 1980 when Intel invited Electronics to hear what its top management was planning for the decade. In Electronics' February 28 issue, John Posa, our solid state editor, let the world know of Intel's vow to develop an operating system in silicon which would integrate a high-level language to help compensate for the shortage of software engineers.

In Intel's Aloha, Oregon facility, tight-

lipped designers were progressing with this five-year-old project, dubbed the Special Systems Operation or "SSO." The outcome would be the iAPX 432—the first 32-bit microprocessor to integrate a high-level language. The language? ADA—the Department of Defense's new standard programming language.

Even before the iAPX 432 was hinted at, Electronics was covering the competitive 16-bit microprocessor arena with reports on Intel, Motorola, Zilog, TI, Fujitsu and Philips. In May, we got a break on the "SSO" project.

While covering the 7th Annual Symposium on Computer Architecture in La Boule, our Paris News Bureau recognized Intel's principal engineer for the "SSO," Justin Rattner, leading a discussion on

the iAPX 432 philosophy. New York was contacted and John Posa investigated. He added this new information to what he had already gathered at an earlier visit to the Aloha Project as the first journalist ever to be admitted to the "SSO." Result: our May 22 issue carried the story quoting Rattner's advance announcement.

In November, Electronics reported Intel's plans to hold three invitation-only sessions to introduce the iAPX 432. And finally, on February 24, 1981, Electronics published the "full disclosure" special report on "SSO," authored by its designers, Justin Rattner and William Lattin.

Important editorial? You bet. The iAPX 432 evolved in the pages of Electronics. The only place important people could have read about it was in Electronics magazine.

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
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TI goes international with two telecom ICs

Texas Instruments is entering the international telecommunications market with an elastic store device and a line coder, both developed by TI's design center in Villeneuve-Loubet, France [*Electronics*, Oct. 6, p. 44]. The TCM2401 elastic store device provides buffer-store and pulse-stuffing justification functions required in a second-order pulse-coded-modulation multiplexer. The integrated circuit, which is available now in a plastic dual in-line package at \$11.28 each in 100-unit lots, has a -25° to $+70^{\circ}\text{C}$ operating range and a maximum 20-mw dissipation with a nominal 10-v power source. The line coder, TCM2201, is targeted at European telecommunication systems and features a standard clock rate of 2.048 MHz. **The metal-gate complementary-MOS chip** includes a transmission coder, reception decoder, and error detection. Operating at -25° to $+85^{\circ}\text{C}$, the unit dissipates only 300 mw with a 12-v supply. The device is also available now in 16-pin plastic dual in-line packages for \$9 each in 100-unit orders.

Options home in on precise measurements

Chicago Laser Systems has added two active-trim measurement modules as options to its CLS-33 laser-trimming system. Priced at \$12,000, the single-card MT-256 module is equipped with three time-measurement input channels and **is designed to allow high-throughput production trimming of dynamic circuits** to such time-oriented parameters as frequency, phase, pulse width, and rise time. A second single-card module, the MV-223 priced at \$3,000, is designed for use with an MT-256 to provide an ac-voltage measurement option by routing one input through an eight-pin switching matrix. The Chicago firm will provide CLS-33 software to accommodate the new modules, which can be delivered four to six weeks after receipt of order.

Processor card using STD bus achieves 4-MHz rate

Mostek's second single-card STD-bus computer runs at 4 MHz. The complete MD-SBC 1 Z80-based system includes 1-K byte of random-access memory, three TTL-buffered 8-bit output ports, two TTL-buffered 8-bit input ports, and four sockets for 2716 erasable programmable read-only memory devices, each capable of storing 2,048 words by 8 bits. **In orders up to nine units, the 4-MHz version sells for \$325 each**, while the earlier 2.5-MHz card goes for \$195. The Carrollton, Texas, firm is also introducing a 4-MHz high-speed math STD-bus card, called the MDX-Math. Also Z80-based, the card will cost \$475 each in quantities of one to nine. Lastly, Mostek is unveiling a new floppy-disk controller, the MDX-FLP 2, which can control up to three $5\frac{1}{4}$ -in. Shugart drives or four 8-in. Shugart drives. The Z80-based STD-bus card sells for \$400 each in orders of one to nine.

Switch lets digitizer serve many hosts

To keep price tags low, California Computer Products Inc. of Anaheim, Calif., has unveiled a standard switch-selectable digitizer with a variety of interfaces. The series 9000 models can communicate with up to three hosts simultaneously, using any combination of RS-232-C, 16-bit parallel, or IEEE-488 interfaces, which can be chosen by flipping switches. The 8085-based family includes five tablet sizes, ranging from 12 by 12 to 60 by 44 in. **Prices for the digitizers begin at \$2,500**, with the savings achieved because production runs for the standardized 9000 are larger than for machines geared to a single interface.

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Career outlook

Handle with care

In order to avoid losing potentially valuable employee timber, companies seeking to fill pivotal engineering and technical openings may have to change many of their basic attitudes toward applicants, warns a Los Angeles executive recruiter. Firms often invite the right persons to interviews only to drive them off with careless interviewing techniques, says J. Paul Sutton, president of Gemini Management Resources Inc. Too frequently forgotten by engineering management and other executives charged with hiring, says Sutton, is the status of the recruiting market. "Remember, it is a buyer's market for these people. They have to be sold on moving not only to a new job but perhaps cross-country as well."

Though today's scarcity of electronics engineers and scientists is an industry truism, the old attitude of expecting the applicant to sell himself has persisted, Sutton points out. "Even though a considerable amount of selling already has taken place just to bring the prospective employee into the executive's office, many recruiters expect the prospect then to sell himself on his worthiness for a position." In fact, the company's approach may even be a negative "convince us that you qualify"—a sure turn-off for the applicant.

In Sutton's opinion, top engineering and scientific candidates themselves are lax about polishing their interviewing skills. "We find heavyweight technical people often have disdain for personnel and industrial relations officials," he points out.

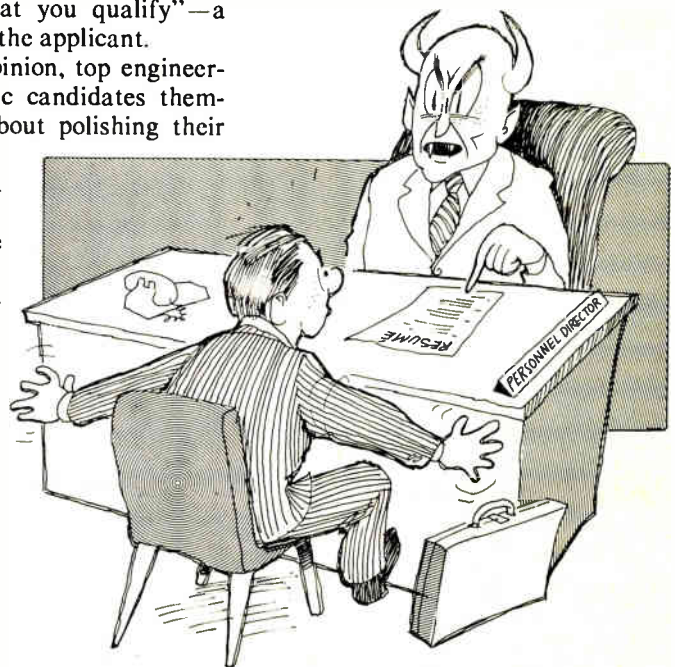
Sutton advises his clients, usually aerospace and electronics firms, to recognize these attitudes in the prospective employ-

ee and then ignore them. "If the applicant has a skill that is badly needed, overlook his unsophisticated interviewing technique or his lack of effort to hide his doubts about joining your firm. He wants to be convinced, so sell him on your company. Appeal to his basic motivations, such as the need for a place in the sun or for recognition of a job well done," counsels Sutton.

His own approach to an engineer or manager targeted for recruitment starts with stimulating excitement about the technical part of the job, then stresses the advancement opportunities and the life-style advantages for the candidate's family. Salary and fringe benefits are never used to open a discussion "because the other points psychologically are more important." In guiding client companies, Sutton tells them never to put a recruited candidate through the personnel gauntlet, "but treat him or her like a guest in your home." Finally, the company should make a prompt decision.

As for advice to the candidates, Sutton counsels them to use bad treatment by an interviewing company as a learning experience. "If the job is a real advancement, be above the firm and play its game. Get the offer as an exercise, if nothing else."

-Larry Waller



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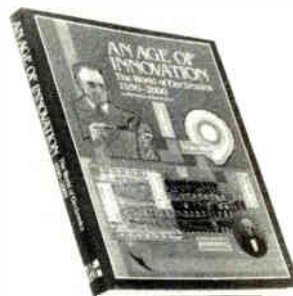
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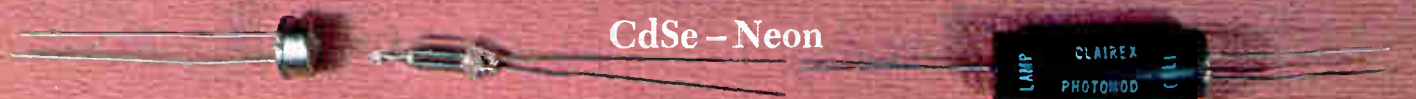
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