JULY 28, 1981

SPECIAL REPORT: STATISTICAL MULTIPLEXERS GETTING SMARTER/141

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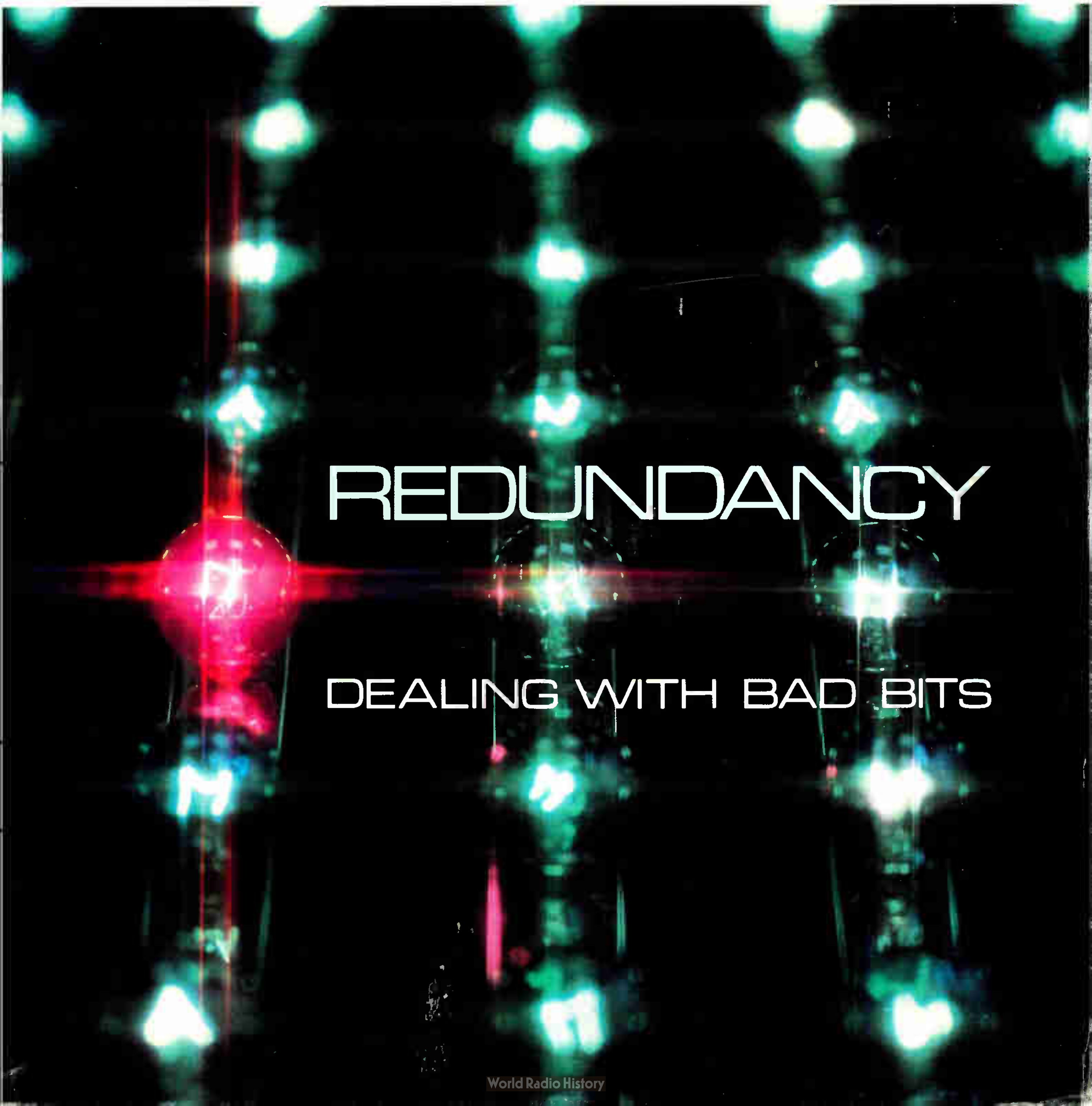

9. Circuit Testing Update/No. 9 in a series from Hewlett-Packard.

HOW CAN YOUR MICROPROCESSOR BOARD HELP TEST ITSELF?

It's ironic. The very intelligence that makes your products excel can also be the obstacle that makes testing difficult. Why? Because those intelligent microprocessors are difficult to model. And until they're put to work via code, they're no smarter than any other piece of silicon. Can they be awakened and used to test themselves? Let's look at some of today's testing techniques and see.

Alternatives for testing microprocessor boards.
Board testers available today generally use one of four approaches:

1) Simulator board testing. This is an edge-connector and guided probe testing technique that relies on patterns from a simulation model. The processor is usually removed from the board, and input patterns applied. Output patterns are then compared with those predicted by the simulator. If the patterns match, the support logic is judged good. Next the processor is inserted and different patterns are applied. Now the outputs are compared to those predicted based on the original model plus a high-level software model of the processor. If those patterns match, the entire board is said to be good. Excessive time can be consumed generating both high-level models and testing software.

2) In-circuit testing. Using a bed-of-nails fixture, contact is made with each logic circuit on the board, including the μP. Pulses are applied to input pins of each device. Outputs are compared to those predicted from device truth tables supplied by manufacturers. These libraries are programmed for common device configurations and must often be modified for actual configurations.

3) Comparison testing. In this edge-connector and guided probe method, a known good board must be available as a reference. The known and unknown are initialized, synchronized and then are compared by applying preprogrammed instructions or patterns, or by stimulating with pseudorandomly generated pattern sets. If the outputs match, the unknown board passes.

4) Processor-based testing. This technique uses the intelligence of the μP on the board. The board is powered up and operated at speeds up to 10 MHz using preprogrammed test code resident in the test system or on the board itself. The on-board μP executes this code to exercise the address and data buses, and support circuitry. Key nodes are monitored with signature analysis to detect faults.

Why does HP use processor-based testing?
Our experience in testing μP boards has revealed several benefits of processor-based testing. That's why we've incorporated it into our 3060A Board Test System with the High Speed Digital Functional Test option.

First of all, boards are tested at speed, with all components, buses and control lines operating in modes similar to actual use conditions. The result? Ability to test pins which are not exercised unless the processor is executing instructions (Fig. 1), plus detection of faults related to the address and data bus structure and timing faults.

Examples of Processor Pins Testable Only With Software

	8085		6800	Z80
Interrupts	INTR TRAP	RST 7.5 RST 6.5 RST 5.5	$\overline{IRQ}$ $\overline{NMI}$	$\overline{INT}$ $\overline{NMI}$
Control Outputs	S_0 S_1 $IO/\overline{M}$	$\overline{RD}$ $\overline{WR}$	VMA $R/\overline{W}$	$\overline{M1}$ $\overline{RD}$ $\overline{WR}$ $\overline{HALT}$
Other	SID SOD			

Fig. 1

In addition, processor-based testing permits fault detection using Signature Analysis (SA), which is complimented by new software in the digital functional testing package. SA allows rapid fault isolation to the component level on active bi-directional buses. That means high throughput in production.

Furthermore, with the programming aids available from HP, functional test program development time is minimized for μP, memory and IO boards. For example, you can either modify existing routines provided by HP, build your own stimulus routines using HP-supplied building blocks, or develop stimulus programs on a development system and download to the 3060A. The bottom line of processor-based testing is fast test program development, high throughput, and high yield at the final product level.

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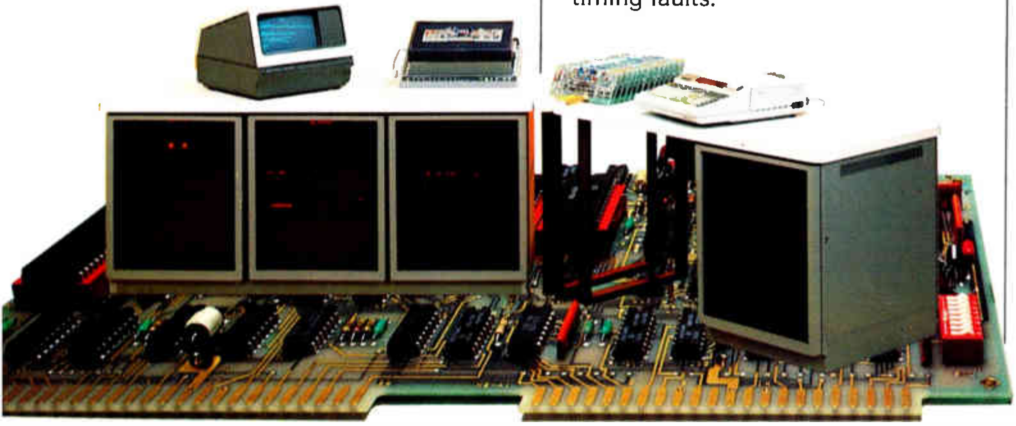

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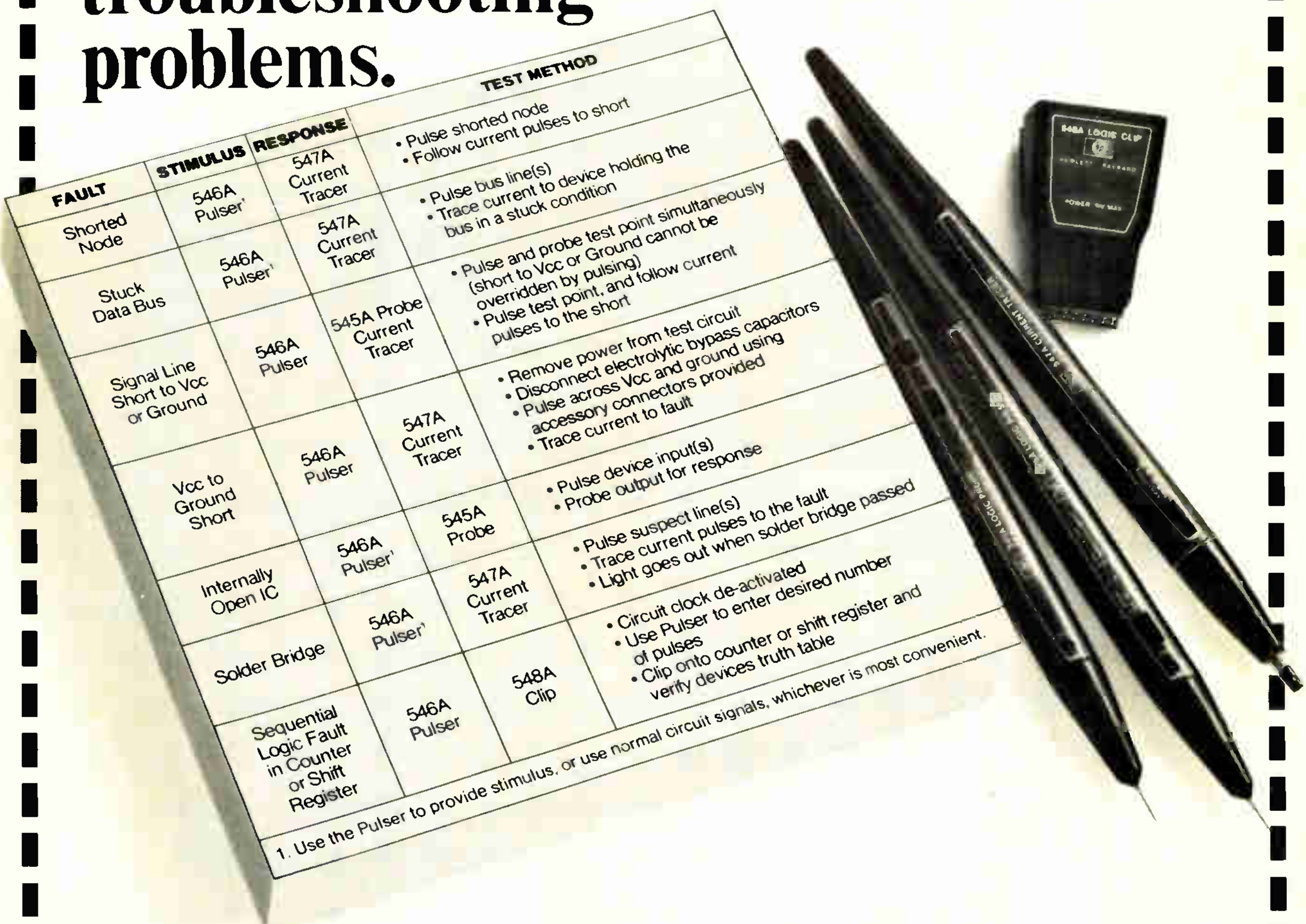

FAULT	STIMULUS	RESPONSE	TEST METHOD
Shorted Node	546A Pulser[1]	547A Current Tracer	• Pulse shorted node • Follow current pulses to short
Stuck Data Bus	546A Pulser[1]	547A Current Tracer	• Pulse bus line(s) • Trace current to device holding the bus in a stuck condition
Signal Line Short to Vcc or Ground	546A Pulser	545A Probe Current Tracer	• Pulse and probe test point simultaneously (short to Vcc or Ground cannot be overridden by pulsing) • Pulse test point, and follow current pulses to the short
Vcc to Ground Short	546A Pulser	547A Current Tracer	• Remove power from test circuit • Disconnect electrolytic bypass capacitors • Pulse across Vcc and ground using accessory connectors provided • Trace current to fault
Internally Open IC	546A Pulser[1]	545A Probe	• Pulse device input(s) • Probe output for response
Solder Bridge	546A Pulser[1]	547A Current Tracer	• Pulse suspect line(s) • Trace current pulses to the fault • Light goes out when solder bridge passed
Sequential Logic Fault in Counter or Shift Register	546A Pulser	548A Clip	• Circuit clock de-activated • Use Pulser to enter desired number of pulses • Clip onto counter or shift register and verify devices truth table

1. Use the Pulser to provide stimulus, or use normal circuit signals, whichever is most convenient.

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Highlights

Cover: Redundancy comes of age in semiconductor memories, 117

U. S. makers of semiconductor memories are embracing the idea of redundancy to improve yields, particularly for extradense random-access and read-only memories. Swapping in spare bits, in rows or columns, is already a feature in some 64-K dynamic RAMs and is likely to be near-universal for quarter-megabit and larger memories. To present the issues involved, a four-part package has been assembled.

An overview deals with the controversies over how and when to implement redundancy (p. 117). The organization of the spare bits is a particularly hot issue; so, too, is the question of electrical-pulse or laser-beam substitution.

One design article focuses on the planning needed to realize redundancy in static RAMs (p. 121). The optimization of technology and of cell layout for speed and yield is an art unto itself.

A second design article deals with equipping a line of memories with spare cells (p. 127). The implementation of the redundant elements varies according to what best suits the different memory types and whether the data is bit- or byte-wide.

The last article, on laser substitution, argues that laser programming will win out over electrically fused links because of the greater circuit design flexibility (p. 131).

The cover photograph is by Senior Editor John G. Posa.

Rfi hits computer makers in a big way, 93

The Federal Communications Commission has declared war on radio-frequency interference from high-speed digital electronics. Personal computers firms are in the thick of the fray; for makers of commercial and industrial gear, the fight is less intense.

Data paths add statistical multiplexing, 141

For data-communications networks, time-division multiplexing has become the technique of choice, and advances in statistical multiplexers detailed in this special report give a smarter tool to implement TDMs.

Terminal technique displays 3-d graphics, 150

To create graphics displays with volume and depth, a new technique combines a rapidly oscillating mirror with a cathode-ray-tube display and a custom computer. The mirror turns a series of two-dimensional images from the CRT into a continuous 3-d one.

In the next issue . . .

A special report on memory management . . . a noise-reduction integrated circuit . . . array logic for analog circuits.

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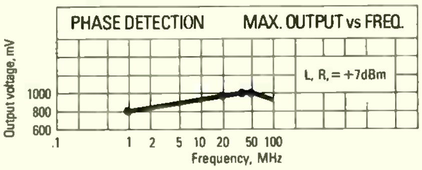

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ISOLATION, L-R	40 dB min
MAXIMUM DC OUTPUT, mV	1000 mV typ 750 mV min
DC OUTPUT POLARITY (L and R in-phase)	Negative
DC OUTPUT OFFSET VOLTAGE	0.2 mV typ 1 mV max
FIGURE-OF-MERIT, M	143 Typical

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63 REV. ORIG.

Publisher's letter

Bits, bits, and more bits—that's the cry of semiconductor memory users, whose insatiable appetite is one reason why many chip makers are adopting redundancy schemes to raise their yields on static and dynamic random-access memories. The anthology beginning on page 117 takes a hard look at the issues: the tradeoffs between redundant and nonredundant memories, the various schemes for placing the spare bits in either rows or columns, and the controversy over whether the spares should be activated by electrically blowing fuses or by zapping links with a laser beam.

The series of articles, which was organized by solid state editor John Posa and edited with the assistance of components editor Rod Beresford, leads off with an overview by John. "The situation is a very interesting one," he notes. "Not long ago, a shortage of bits opened the U. S. market door to Japanese RAM makers. Now it seems that no Japanese manufacturers—with the possible exception of Fujitsu—will elect redundancy at the 64-K level. So if redundancy does to yields what the manufacturers are expecting, that could mean that any U. S. chip makers adopting it will regain a significant competitive edge in the RAM market."

An article from Inmos Corp. follows John's report. Inmos, the Colorado Springs, Colo., memory-chip maker credited with introducing the first commercial RAM with redundancy, touts electrical blowing of fuses for its 16-K static and 64-K dynamic RAMs. The next article is from Intel Corp., which also blows fuses electrically. Here Intel describes, among other things, the tradeoffs associated with redundancy in byte-wide memories.

The anchor article is from Bell Laboratories, long a proponent of redundancy in memories. Bell's redundantly designed 64-K dynamic RAM was begun four years ago; back then only magnetic-bubble memory manufacturers were using redundancy. Today, with the labs' claims of a yield improvement factor of 30 on early prototype runs of the popular part, no one can afford to look away from the approach.

Bell uses the laser to fix its bad bits. Despite others' remarks that the fancy equipment and test software run up an inordinate expense, the labs claim that the equipment can "pay for itself" in an astonishingly short two weeks.

The data-communications network designer or manager has long used multiplexers to combine the data outputs of a number of relatively slow transmission lines onto one high-speed line. These days, he's taking a fresh look at new versions of these machines because, with the incorporation of microprocessors and built-in software, they now offer a lot more than plain old signal combining.

In fact, as communications editor Harvey Hindin points out in his special report on statistical, or intelligent, multiplexers (p. 141), they can perform data compression, switching, port contention, encryption, dynamic network reconfiguration, down-line loading, and other chores usually associated with mini- or mainframe-computer–controlled network processors or concentrators.

"The statistical multiplexer, unlike its older bit- and character-interleaved multiplexer cousins, doesn't just save transmission line costs. Now it processes and manipulates the signals applied to it, so that the data-communications network—even for the small user—is cost-effective," Harvey says. "And," he adds, "now that multiplexers based on 16-bit microprocessors are being introduced, a data-communications network designer will have even more flexibility in handling different signal protocols, coding, and speeds." Harvey says that several of these new multiplexers will be introduced this year, and machines based on the 32-bit microprocessor are already under study.

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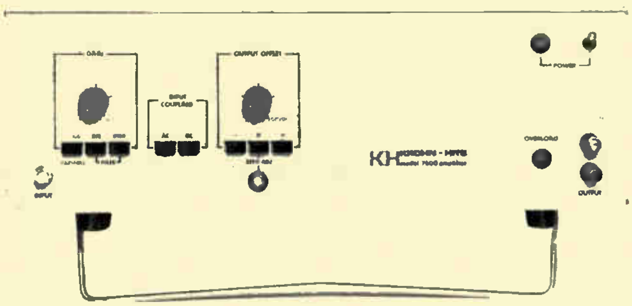

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Readers' comments

Reflections on a bus

To the Editor: I have to agree with Henry Keultjes' letter in your June 2 issue [p. 8] and maybe go a little further. Although the new buses are necessary to get all the capabilities built into the new generation of microprocessors like the 68000 and the Z8000, they are not what is needed to put them to work right away. Some of the demand is for more speed and more efficient interrupts and cycle stealing, but a lot of it is for architectures that answer the problems of second-generation 8-bit machines. In other words, it is at least as important that the internal architecture of a system is 16 bits wide with a regular instruction set as it is for the bus.

That being the case, it seems to me that there is a more immediate demand for better boards and board sets that can retrofit existing computers than there is for completely new maximum-performance systems. Thus, Keultjes is right in suggesting that the Multibus should get a board containing the new microprocessors before the new buses do, since there is a huge installed base of upgradable Multibus systems.

The other bus for which 68000 and Z8000 boards ought promptly to be built is the STD bus. Its installed base and popularity are growing fast, and the people who use it tend to write machine language. They could really use easily programmable CPUs, especially if the CPU board comes with a read-only memory carrying the operating-system kernel these processors need.

John A. Carroll
Instrumentation Laboratory Inc.
Lexington, Mass.

Corrections

In "Charge-balancing modulator aids analog-signal modulation" (June 2, p. 159), the voltage reference and a positive-going ramp were referred to as a current sink and a negative-going ramp, respectively. Also, the flip-flop can switch another voltage source on to the RC filter, rather than another current source to charge capacitor C_I, to restore the original input voltage.

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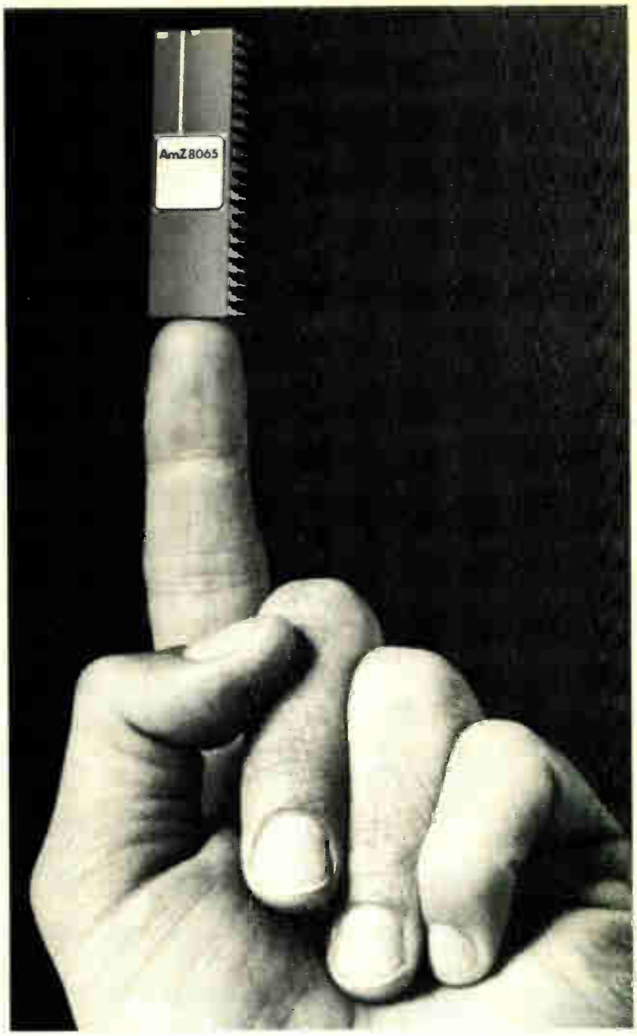

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INT STD 123

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News update

■ Lexicon Corp. seems to have made a specialty out of electronic packages that are small enough to fit in the hand but can do unusual things. Back in 1978 the Miami, Fla., company introduced the first hand-held language translator [*Electronics*, Dec. 7, 1978, p. 50]. But it got mired financially trying to dent the tough consumer marketplace, so it sold the rights to the translator to Nixdorf Computer in August 1979 for cash ($1.5 million) it needed to continue in business.

Its forte became custom terminal products. In the spring of 1980 it brought out an inexpensive acoustic coupler plus data modem that, like the translator, is small: it fits into half an attaché case. And next month, Lexicon starts shipping a portable computer terminal that can fill the other half of the case.

Five pounds. Like the language translator, the Lex-21 portable terminal is an eye-catcher. At 5 pounds, it is the smallest and lightest terminal to sport a full ASCII keyboard, printer, and modem, points out Michael Levy, Lexicon's president. Its thermal printer can produce 40 characters per line on a five-by-seven-dot matrix. The modem is a 300-bit-per-second, full-duplex design compatible with Bell's venerable 103A. At $1,195, it competes with units that are twice as large and sell for at least half again as much.

Lexicon, with total sales now at a $1.5 million yearly rate, has a pretty fair market to tackle. Levy is eyeing just about every Fortune 1,000 company with a computer and men in the field who want access to it. Other possible customers include time-sharing and computer services, as well as individual users of data services such as Compuserve and The Source. There are also plans to gain access to Western Union's network as well.

Lex-21 simply plugs into a common modular telephone wall socket, Levy points out. The telephone, in turn, plugs into the terminal. If there is no wall socket, the company is ready: a pair of optional rubber cups will couple the phone's handset to the modem. **-Tom Manuel**

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Genesis Linear Chips			
CS2000E	70 x 70 mils	187 components	18 bonding pads
CS2500G	80 x 83 mils	305 components	18 bonding pads
CS3000F	91 x 110 mils	437 components	24 bonding pads
Genesis I^2L Gate Arrays			
CS1200	192 gates	24 I/O ports	30 bonding pads
CS1300	288 gates	28 I/O ports	30 bonding pads
CS1400 (Analog/Digital)	256 gates; Up to 400 linear components	18 I/O ports	40 bonding pads

Note: CS1200, 1300 and 1400 are alternate source equivalents to Exar XR200, XR300 and XR400.

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Circle 13 on reader service card

People

Fujitsu's Yamamoto targets office automation market and wants other divisions to catch up with data processing

For Takuma Yamamoto, the reward for deposing IBM Corp. as king of the computer hill in Japan is the presidency of Fujitsu Ltd., where until this summer he headed the Computer Systems division as executive director and general manager. Fujitsu climbed over IBM two years ago and last year widened its lead, racking up computer sales of $1.7 billion to IBM's $1.5 billion.

Balance. Takuma Yamamoto wants Fujitsu to consist of three well-balanced divisions.

So when the company's directors promoted the 56-year-old Yamamoto to the top spot over three executive vice presidents, the new president broadened his view. "The structure of society will change fundamentally in the 1980s, so to comply with those changes we must alter the company's strategy," he says. "Specifically, we must emphasize office automation." Under that rubric Yamamoto includes computer-aided design, manufacturing, and testing. He thinks office automation will grow faster than any other data-processing market segment and wants Fujitsu to participate in the bonanza.

Fujitsu is getting a late start. It began making Japanese-language word processors only last year and has a paltry 5% market share. However, it is further along in facsimile machines, and has introduced five models since launching production two years ago. The company is also selling a CAD software package and has other office automation products under development.

Ironically, computer ace Yamamoto wants Fujitsu's other two key businesses—telecommunications and components—to grow even faster than data processing, which now accounts for 65% of company sales. "I want three relatively equal divisions with equal profits so we can have well-balanced, steady growth."

Unlike his earthy, outspoken predecessor, Taiyu Kobayashi, Yamamoto is taciturn, though pleasant. Perhaps that is a result of his army upbringing and graduation from a military academy before entering Tokyo University. There, he took a degree in electrical engineering with such classmates as Katsushige Mita, the new president of Hitachi Ltd., and Masahiko Morizono, a senior managing director at Sony Corp.

Consistent with the consensus-oriented tenets of traditional Japanese management, Yamamoto modestly describes the impact he wants to make on Fujitsu: "I want to be a president whose name isn't remembered."

Colorgraphic is the third terminal maker for Mintz

Ezra Mintz is doing it again. The founding of Colorgraphic Communications Corp. in Atlanta, marks his third venture in the area of intelligent color graphics terminals.

Atlanta, a center for color graphics activity, already has witnessed his involvement with the former Integrated Systems Inc. in the early 1970s ("I helped raise the capital for Integrated," says the 48-year-old Wall Streeter turned Georgian) and Intelligent Systems Corp. Until about 18 months ago, Mintz was president of Intelligent Systems, listed by some analysts as one of the 100 fastest growing companies in the United States.

Mintz left there early in 1980; by

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ALL disk storage subsystems are configured, integrated, and tested by First Computer Corporation to provide you with a totally plug-compatible disk storage subsystem. These subsystems can be installed on your system and be up and running the standard DEC diagnostics and operating systems within minutes.

MODEL	STORAGE CAPACITY		OPERATING SYSTEM EMULATION		MODIFIED HANDLER
	Removable	Fixed	RT-11	RSX11-M / RSTS/E	
9448-32	16	16	2 13.7MB RP02's	2 13.7MB RP02's	YES
			2 13.9MB RK06's	2 13.9MB RK06's	NO
9448-64	16	48	4 13.7MB RP02's	4 13.7MB RP02's	YES
			4 13.9MB RK06's	4 13.9MB RK06's	NO
9448-96	16	80	6 13.7MB RP02's	6 13.7MB RP02's	YES
			6 13.9MB RK06's	6 13.9MB RK06's	NO
9730-80	—	80	3 20.8MB RP02's	3 20.8MB RP02's	NO
				1 67.4MB RM02	NO

MODEL	STORAGE CAPACITY		OPERATING SYSTEM EMULATION		MODIFIED HANDLER
	Removable	Fixed	RT-11	RSX11-M / RSTS/E	
9730-160	—	160		2 67.4MB RM02's	NO
9762	80	—	3 20.8MB RP02's	3 20.8MB RP02's	NO
				1 67.4MB RM02	NO
9766	300	—		1 253.7MB RP06	YES
				1 256.1MB RM02	YES
9775		675		1 552.5MB RP06	YES
				1 552.5MB RM02	YES

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Circle 15 on reader service card

People

Objective. Ezra Mintz wants Colorgraphic to have 10% of market within five years.

midyear he had Colorgraphic in mind. As he says, "In the past 10 years I had learned to talk 'EE' and I knew a market when I saw one."

The market he saw was for what became the MVI-7, a medium-resolution color graphics terminal that does everything IBM Corp.'s 3279 does but sells for half the price. Interestingly, one of Mintz's first custom-deliveries will be to IBM, to a group that dislikes the interface requirements imposed upon them by their own product and finds the MVI-7 easier to use. Mintz's unit emulates the protocols for terminals from IBM, Lear-Siegler, Digital Equipment, Hazeltine, and others. The $3,000 unit is about to go into volume production, with deliveries to begin in August or September.

Mintz feels that color graphics "will be a commodity market within five years, and by then we will either have about 10% of the market or will have sold out in favor of something more attractive." For maximum penetration, Mintz plans to stay in the medium-price, high-performance sector of the market.

Mintz also is a believer in built-in diagnostic and board-swap maintenance. "A small company can't afford to see the same units that just went out coming back in the door, so we have consciously overengineered our equipment and added on-board diagnostics—simple stuff with light-emitting diodes to show what's gone wrong," he declares. □

The only 100 MHz scope that gives you three vertical input channels... Kikusui just had to do it better.

Three vertical input channels, two trigger views and an "add differential" trace. That's what you get with KIC's new 100 MHz KIK-scope. Use the third channel as an extra data channel, as an additional signal in an x-y display, or for a host of other applications. There's almost no limit to the versatility that this third channel adds to your scope. And, it's included at no extra cost in our new Model 6100.

The Model 6100 is comparable to TEK's Model 465B and HP's 1742 but displays more traces (six compared with three), and offers more screen brightness, more flexibility, greater simplicity of operation and a two-year warranty that substantially reduces the second year cost of ownership. The Model 6100 also features an auto-dynamic focus circuit for clear, sharp pictures and a metal housing that minimizes RFI interference.

Now for the surprising news: Despite all the extra features, the 6100 costs less than either the TEK or HP scopes.

For versatility of operation, an alternate trigger permits viewing a very wide range of non-synchronous signals. For simplicity of operation, a level-lock on the trigger level control for both A and B channels activates a peak-to-peak detector that automatically sets trigger level and triggers without operator intervention.

Rugged and compact, the 6100 is completely modular. Like all KIK-scopes, the construction is on plug-in boards that are supported by a board swap-out program that assures fast maintenance turn-around and minimum down-time.

And, just to give you a little added assurance, your KIK-scope comes with a 30-day "satisfaction-or-your-money-back" guarantee.

This new 100 MHz KIK-scope along with eleven other models for engineering labs, field service and production line applications, is described in our new brochure. Write for it. It's free.

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Circle 17 on reader service card

Blinding speed in

Intel introduces the world's fastest 16K bipolar PROM, the 3636B.

At a blinding 35ns, our new 3636B offers the fastest access time ever in a 16K bipolar.

The newest member of our complete family of 8K and 16K bipolar PROMs, the 3636B is now being produced in volume. Which means you not only get speed in access times, you get it in delivery times too.

Breaking speed barriers to performance

Exceptional speed...density... reliability. Super-high-performance applications demand them all.

Take microcode or program store in bit-slice microprocessors, for example. Or high-speed data-comm, telecom and military applications.

That's where the 3636B really shines. It's got what it takes to increase throughput in today's high-performance microprocessors. Plus it's got plenty of features to help simplify design cycles. Features like three chip-select inputs and three-state outputs. A 10% power supply tolerance. And an industry-standard 24-pin package.

Boosting yields and reliability too

How do we achieve the 3636B's remarkable speed, while reducing its die size, boosting yields and improving reliability figures? Simple. With our exclusive Stacked Fuse Bipolar* technology.

This is the same technology that's proven itself in millions of device hours over the past four years,

*Stacked Fuse Bipolar is patented by Intel Corporation.

Intel Bipolar PROMs		MAX.
3636B-1	2K x 8	35ns
3636B-2	2K x 8	45ns
3636-1	2K x 8	65ns
3636	2K x 8	80ns
3628A-1	1K x 8	50ns
3628A-3	1K x 8	70ns
3628A-4	1K x 8	90ns
M3636 (Military)	2K x 8	80ns

bipolar PROMs.

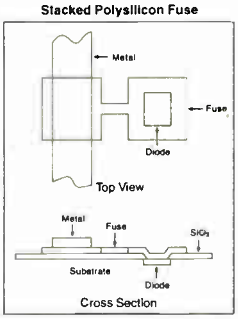
in our existing line of bipolar PROMs. And in millions of devices delivered—including military versions for hi-rel applications.

This dual layer metalization and polysilicon fuse process makes possible the inherently high reliability of our bipolar PROM family. And the higher yields you get from programmed parts.

Coming on strong with a full line

No matter what you need in high-density bipolar PROMs, Intel's got it. For hi-rel applications, there's our military-qualified 16K. Or if you're designing in 8K increments, you can put our bipolar technology to use with parts as fast as 50ns.

Stacked Polysilicon Fuse



Intel's new Stacked Fuse Bipolar process allows a 30% reduction in the 16K cell size. This dramatic density improvement yields faster access speeds than ever before possible. The illustration shows the "stacking" of our polysilicon fuse over the diode, instead of placing them side by side as in older designs.

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To order, or get complete specifications, reliability information, and our convenient Bipolar PROM Reference Guide, contact your local distributor or Intel sales office. Or write to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

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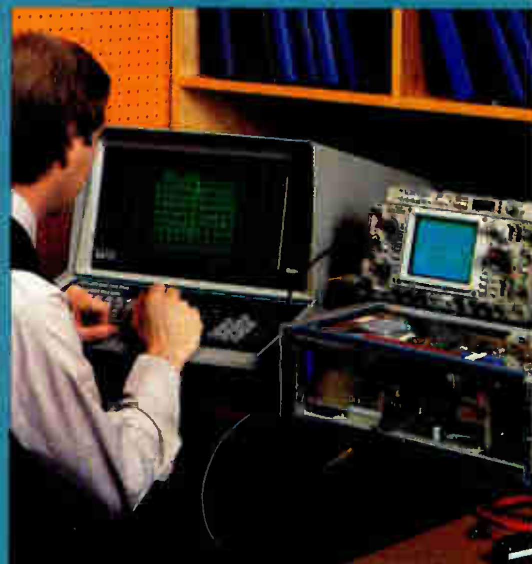
Circle 19 on reader service card

New powers of waveform analysis. From the



(above right) The Tektronix 468 portable digital storage oscilloscope becomes part of a powerful processing system when interfaced to the Tektronix 4052 Computer/Controller for analysis and processing.

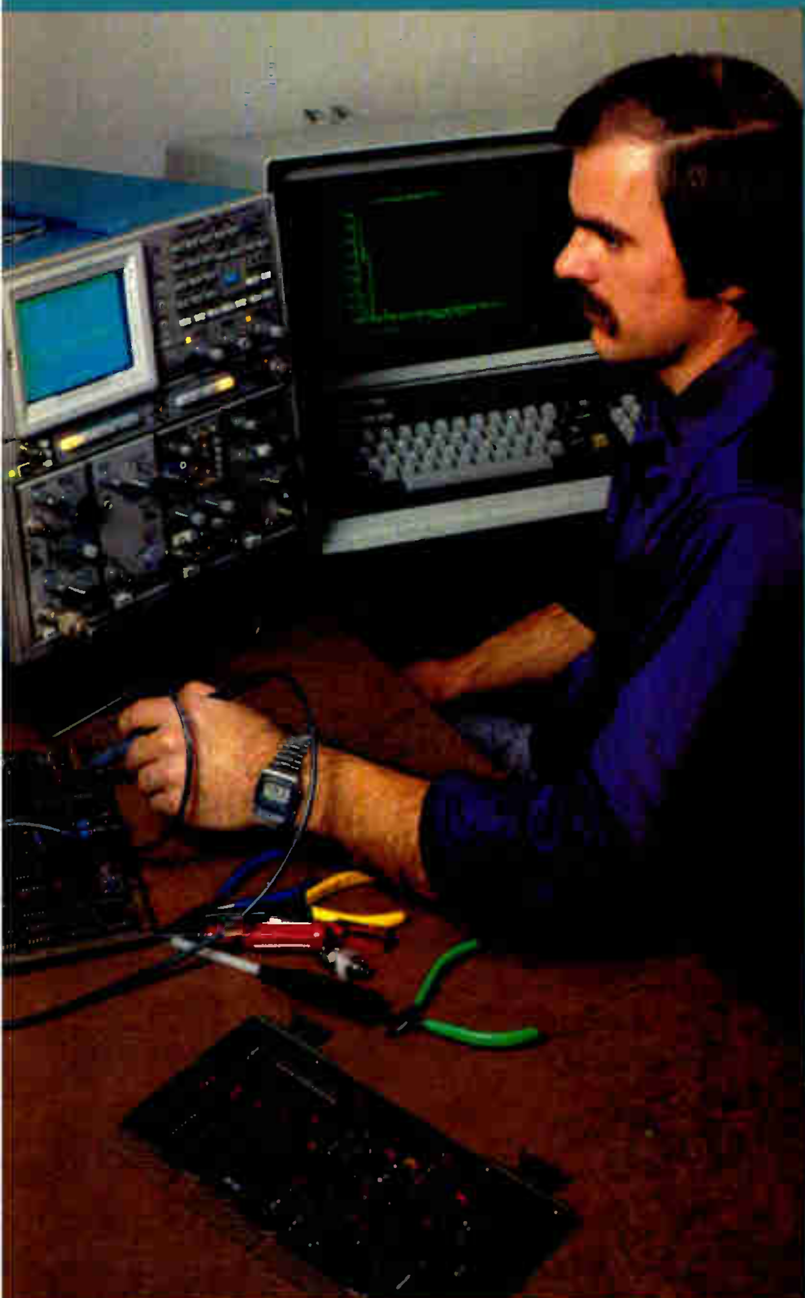
(above left) Users can link the Tektronix 492P Spectrum Analyzer with the 4052 to compare accumulated displays over successive sweeps. Right at hand are high-speed analysis, plus permanent records via the Tektronix hard copiers.

(far right) The Tektronix 7854 Oscilloscope interfaces with the 4052 to apply high-speed floating point calculations and simultaneous display of high-resolution graphics and tabular data to the most complex analytical problems.

(below left) To state-of-the-art Tektronix GPIB waveform measurement instruments, you can add the analytical capabilities of the 19-inch 4054 computer/controller for problems requiring both speed and large data display; the fast 4052 for computationally intensive applications; or the economical, general-purpose 4051.

measurement expert.

Productivity in the Tektronix tradition: Graphic. Interactive. Easy. And fast.



Start with state-of-the-art GPIB instrumentation built on 35 years of Tektronix waveform measurement leadership. Instruments like the fully programmable 492P Spectrum Analyzer. Our new 468 Oscilloscope. Or the extraordinary 400 MHz 7854 Oscilloscope. Each a huge productivity booster in its own right.

Add the analytical power of high-speed processing and interactive graphics with Tektronix 4050 Series GPIB Computer/Controllers. You can convert waveforms into any number of precise, storage tube graphics displays—like bode plots, log plots, histograms, Fast Fourier Transforms—so you can quickly analyze measurements.

Result: you not only acquire data, but process, compare and literally draw conclusions with devices that are easy, even a pleasure to use. There are no costly interface designs, difficult languages or complex procedures. Our GPIB codes and formats approach helps make our measurement instruments easy to interface and immediately compatible with each other, so engineers get results quickly no matter which devices are used.

Let Tektronix take you from raw data to finished results—many times faster than by the methods you're using now. For more information, contact your Tektronix Sales Engineer, or call toll-free, 1-800-547-1512 (in Oregon, 644-9051 collect).

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Circle 21 on reader service card

LATEST NEFAX MACHINES HAVE NEW CAPABILITIES

The NEFAX family of facsimile machines has grown with the addition of three new models.

The NEFAX-6500 meets both CCITT G3 and G2 standards for high and medium-speed transmission. And as an option, it can be provided with the low-speed mode to cover all speed ranges.

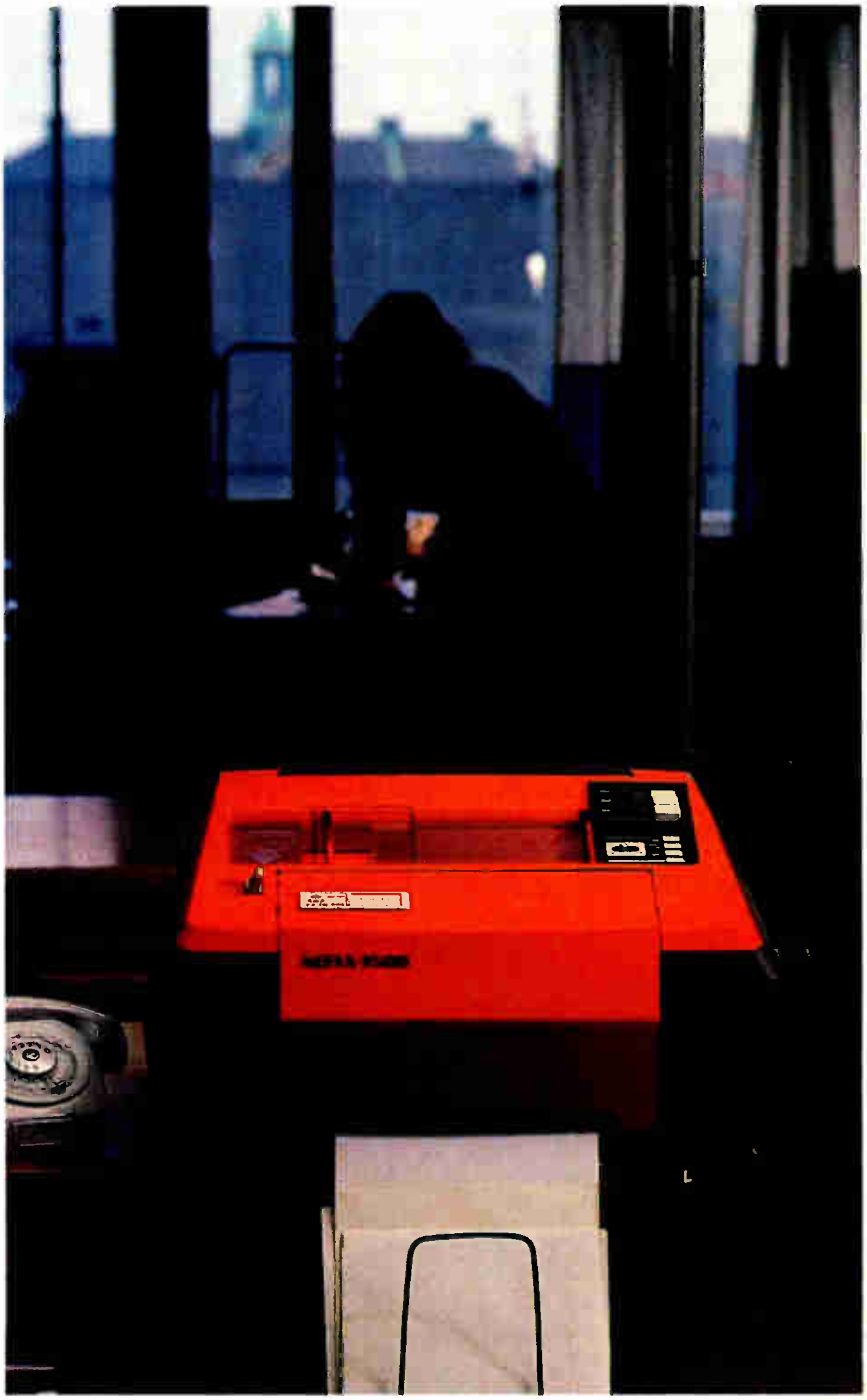
Through the use of LSI high-speed modem, the NEFAX-6500 can transmit a standard "A4" size page in 20 seconds—and through ultrahigh-speed mode in 10 seconds.

A switch on the NEFAX-6500 sets the number of scanning lines to either 7.7 lines/mm or 3.85 lines/mm in accordance with the resolution required. Its solid-state scanning system uses a CCD to enhance reliable operation.

The NEFAX-3700 is an addition to the NEFAX-3000 Series of medium-speed facsimile machines that meet CCITT G2 standards. It has a Super Express Mode that shortens transmission time by skipping over blank (white) portions of a document. Another new feature, Hi-Grey Scale Recording, reproduces half-tone nuances such as those found in photographs. And like the NEFAX-6500, the NEFAX-3700 can automatically send up to 30 pages in sequence.

Designed to fit on any office desk, the NEFAX-2000 is an economical medium-speed (G2) machine. It consumes little power—about 70VA—and is practically maintenance-free.

With these three new additions, the NEFAX line-up is now comprised of seven facsimile machines.



NUMBER 119

LSI TRANSMULTIPLEXER INTRODUCED

NEC's new DTM-2400 transmultiplexer converts two 12-channel FDM group signals in the 60-108kHz band to a 24-channel digital carrier signal at 1.544Mb/s or vice versa.

Designed to satisfy all CCITT Recommendation G. 792 specifications by a large margin, the DTM-2400 incorporates state-of-the-art LSI and digital signal processing technology that reduces equipment size, cost, and power consumption. It is housed in a compact W19" × H7" × D14" subrack mountable in an EIA standard 19" rack.

The DTM-2400 has various options for signalling conversion, clock synchronization and signal interface conditions. For example, two replaceable modules are available for signalling conversion: a 3,825 (or 3,850) Hz out-of-band signalling module and a 2,600Hz SF signalling module.

A transmultiplexer with a larger capacity will become available later this year. This, the DTM-1200, will be able to perform a bilateral conversion between two 60-channel supergroup signals (2 × FDM BSG) in the 312-552 kHz band and five 24-channel PCM (5 × 1.544Mb/s) signals or four 30-channel PCM (4 × 2.048Mb/s) signals.

FIP DISPLAYS FINE-PATTERN GRAPHICS

Because they are flat and provide easy-to-see displays without flickering or misregistration, graphic fluorescent indicator panels (FIP) are expected to replace cathode ray tubes in small display terminals.

The new FIP240A4XT from NEC is a large capacity 60 × 280 dot fluorescent indicator panel capable of displaying 240 characters (40ch. × 6 lines). In addition, it can display fine-pattern graphics such as illustrations, tables and drawings with even brightness, and free from deformation.

These capabilities are due to the FIP240A4XT's 16,800 dot cells that are arranged at uniform 0.65mm pitch intervals in an effective display area 38.80mm (vertical) × 181.80mm (horizontal). Each dot measures 0.45 × 0.45mm.

This large capacity graphic FIP is appropriate for a wide variety of hardware, including word processors, electronic typewriters, POS terminals and banking systems.

MEXICO TO EXPAND MICROWAVE COMMUNICATIONS SYSTEM

Mexico will have a fully solid-state 2700-channel microwave communications system installed by early 1982 along an existing link that extends about 2,200 kilometers from Guadalajara to Tijuana.

The new 45-station 2,200 kilometer microwave system was ordered from NEC by the Secretaría de Comunicaciones y Transportes, Dirección General de Telecomunicaciones (SCT), United States of Mexico. It will be equipped with NEC's latest 500 Series, including the TR-5G2700-500 microwave communications equipment.

The TR-5G2700-500 has a microwave signal output power of 7 watts, uses no travelling wave tubes, and can handle 2,700 telephone channels on one RF carrier. The new Mexican system will be designed so that its channel capacity can be expanded up to 13,500 in the future.

Notably absent from the project is the construction of new station buildings. This is because the slim 500 Series equipment requires minimum floor space and can be installed in existing stations.

The major equipment will be manufactured locally by NEC de Mexico, S.A., de C.V., headquartered at Edo. de Morelos, near Mexico City.

Setting high standards for standards

When the Supreme Court reconvenes in October, it will have on the docket an issue of extreme importance to engineers and to the way standards are set. The high court will hear an appeal by the American Society of Mechanical Engineers, which has been found by a trial judge and a Federal appeals court to have violated the Sherman Antitrust Act.

Although this case involves a very specific situation concerning how the ASME sets standards, the outcome could reach well beyond the suit. It could alter the way codes and standards are issued by engineering and scientific societies.

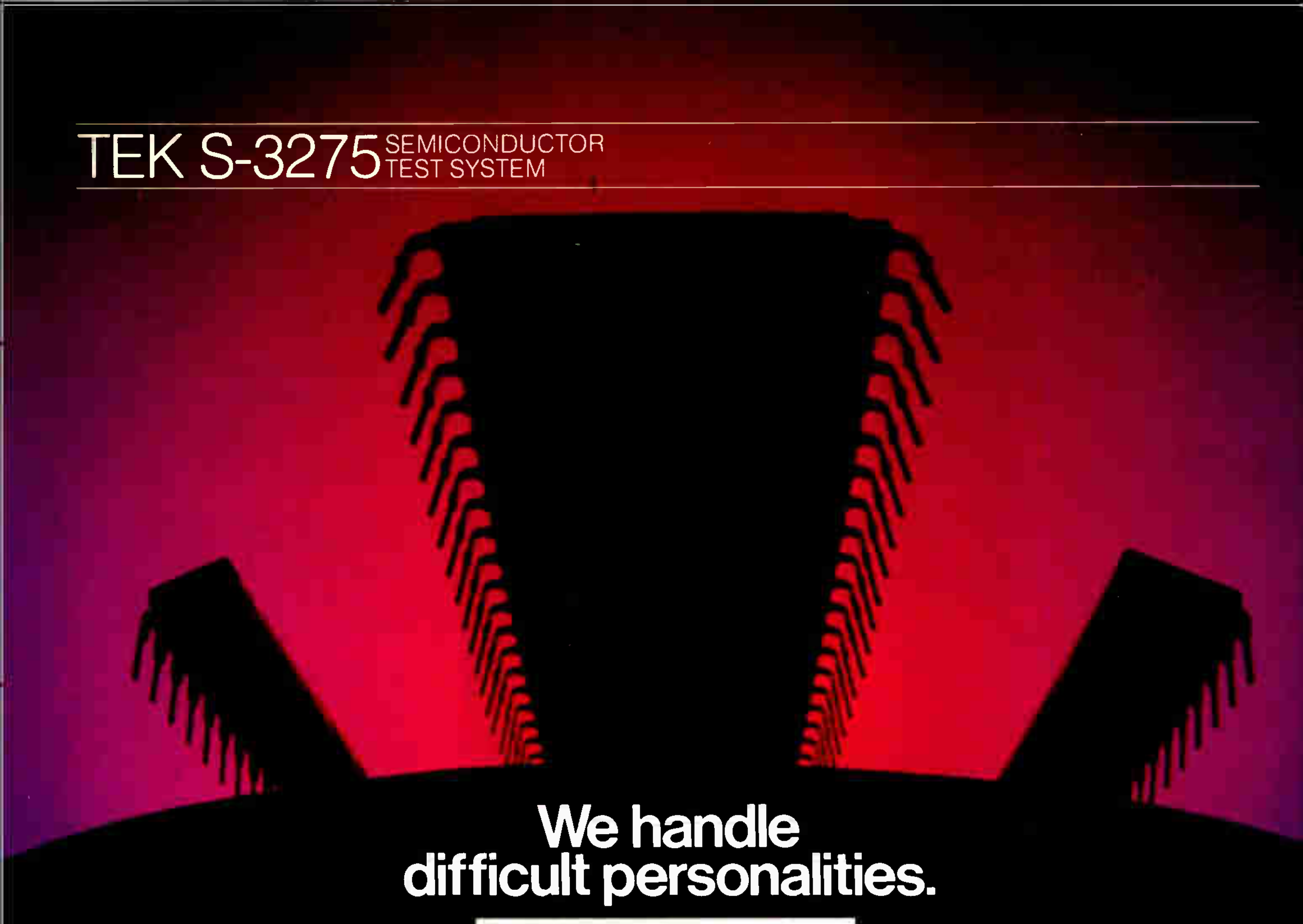
How did standards become a legal issue? According to a suit filed in 1975 by Hydrolevel Corp.—which is now out of business—another firm, which controlled the boiler-cutoff device market, allegedly conspired with an insurance company and the ASME to damage Hydrolevel's efforts to market a device that would automatically turn off a boiler when the water level is too low. The suit charged that the conspiracy hinged on codes for engineering standards issued by ASME and enforced through advisory opinions issued by committees made up of society members.

The particular standard, covering boiler cutoffs, damaged Hydrolevel when those allegedly involved in the conspiracy obtained an advisory opinion in their favor, the suit charged. Hydrolevel's lawyers maintained that its device met the standard. The other company settled with Hydrolevel before the trial, but the ASME proceeded to court and was found liable for conspiring to restrain trade. A Federal judge awarded $7.5 million in tripled damages. A Federal appeals court concurred with the finding but said that the judge should recalculate the damages. The ASME, however, appealed to the Supreme Court contending that it could not be held liable for the actions of its voluntary membership committees over which it says it has little control.

The outcome could have an enormous ripple effect, should societies be held liable for the actions of volunteer committees. It has been suggested that employees of the various scientific societies be responsible for writing standards rather than member committees. However, this solution is not viable, because it would require large staffs with a thorough understanding of a wide range of technology.

The case casts a strong light on the work of standards committees. These groups on the whole are composed of dedicated, hard-working individuals. They must, as the saying goes, be like Caesar's wife—above suspicion. The standards-making system depends on unselfish devotion to the cause. Even a hint that developing or promoting standards to advance one company over its competitors for commercial gain is enough to destroy the volunteer standards system.

If the Supreme Court rules against ASME, it could mean a restructuring of standards committees, since the society would be legally responsible for the standards it backs. This result would be unfortunate, because it implies the high professional and ethical standards that have been the hallmark of our engineering societies since their inception will have been called into public question, and standards activities would be forever suspect. The societies themselves will have to come to grips somehow with this sensitive problem. A firm reiteration of ethical considerations to all standards-committee participants is a beginning.



When it comes to characterization, many LSI/VLSI devices can be difficult little creatures. Normal evaluation procedures just won't work.

Like hybrids that present many simultaneous digital and analog operations. Or chips that require both algorithmic *and* random pattern testing. Plus the ability to change from one to the other on the fly.

There's only one test system that thrives on truly difficult personalities. The Tektronix S-3275. The more complex the device, the more you appreciate what the S-3275 can do.

Why? Because only the S-3275 combines all the right features into a single, powerful package. One that gives you the flexibility demanded by a growing versatility in device design and function.

A system that optimizes design engineering productivity.

With 128 channels at 20 MHz, the S-3275's state-of-the-art pattern processor combines the functions of pattern processing and algorithmic pattern generation. The clock system provides 125 pS resolution on each of 16 phases. Plus the S-3275 has a waveform digitizer to provide FFT and THD analysis.

With the S-3275, you get more than just sophisticated hardware. You get TEKTEST III™, an operating system that allows up to four concurrent tasks.

So when you've got some difficult LSI/VLSI devices to handle, ask us. We know what to do with those kind of personalities.

For more information about the S-3275, contact your Tek Sales Engineer.

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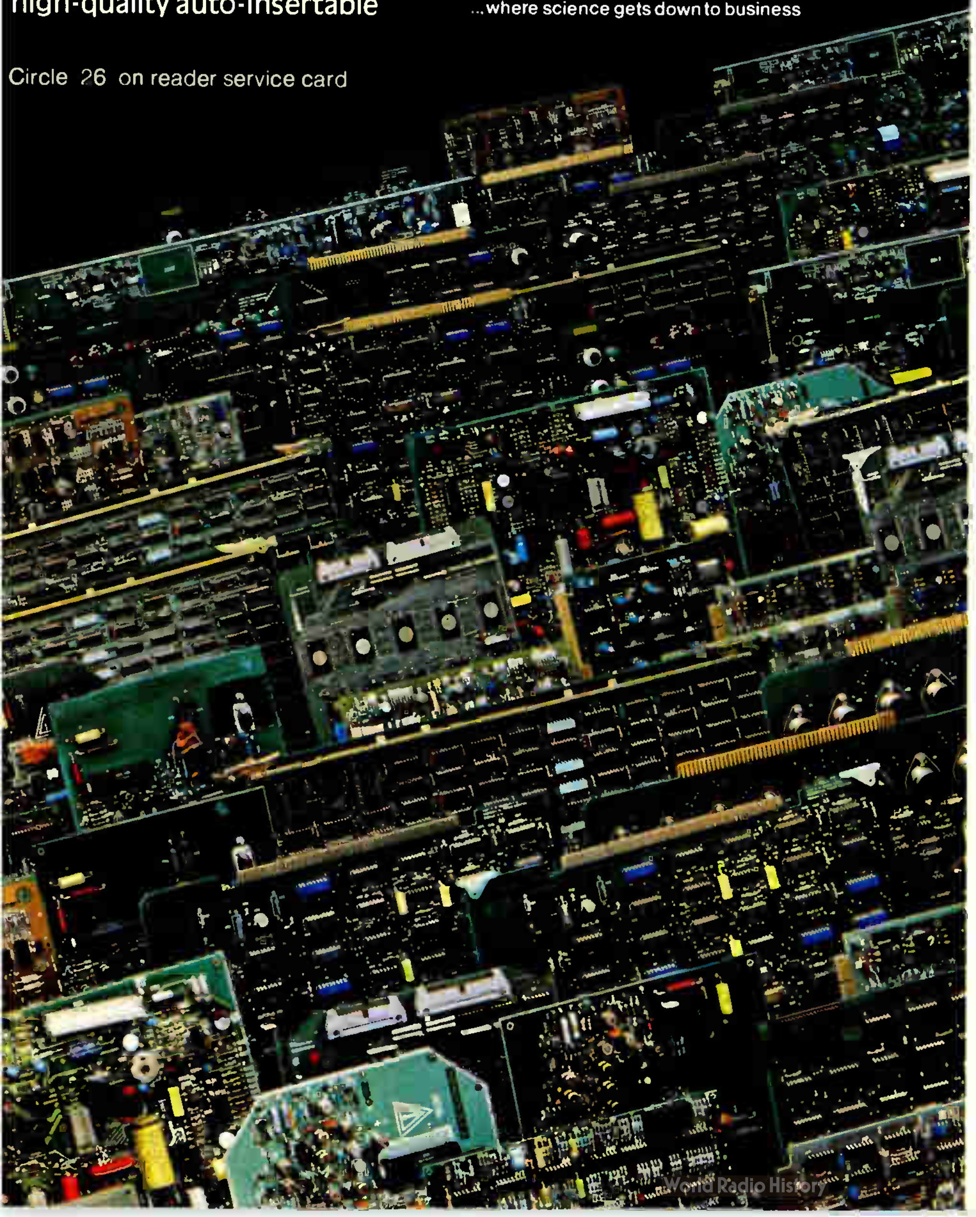

Meetings

FOC '81—Fourth International Fiber Optics and Communications Exposition, Information Gatekeepers Inc. (167 Corey Rd., Brookline, Mass. 02146), Hyatt Regency Embarcadero, San Francisco, Sept. 1–3.

European Conference on Electronic Design Automation, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL), University of Sussex, Brighton, UK, Sept. 1–4.

Home Video and Personal Computers Exposition, Epic Enterprises (6158 Mission Gorge Rd., San Diego, Calif. 92120), Convention Center, Los Angeles, Sept. 4–6.

International Audio and Video Fair, AMK Berlin (Ausstelungs-Messe-Kongress-GmbH, Messedamm 22, Berlin, West Germany), West Berlin Fairgrounds, Sept. 4–13.

11th European Microwave Conference, National Societies of Electrical and Electronics Engineers of Western Europe (Eurel), IEEE, *et al.* (M. T. Vlaardingerbroek, Philips, Elcoma EH5, 5600 MD Eindhoven, The Netherlands), RAI Congress Center, Amsterdam, Sept. 7–11.

Seventh European Conference on Optical Communication, Electromagnetics Institute, Technical University of Denmark (M. Danielsen, Electromagnetics Institute, Technical University of Denmark, DK-2800 Lyngby, Denmark), Bella Center, Copenhagen, Sept. 8–11.

Eurographics '81—International Congress for Computer Graphics and Exhibition, International Federation for Information Processing *et al.* (J. Vlietstra, c/o NV Philips Gloeilampenfabrieken, Bldg. VO-124, NL-5600 MD Eindhoven, The Netherlands), Technical University of Darmstadt, Germany, Sept. 9–11.

Wescon/81, IEEE (Electronic Conventions Inc., Suite 410, 999 N. Sepulveda Blvd., El Segundo, Calif. 90245), Brooks Hall and Municipal Auditorium and Hilton Hotel, San Francisco, Sept. 15–17.

The first user-programmable, 8-bit micro that runs hot and cold: MK38P70.

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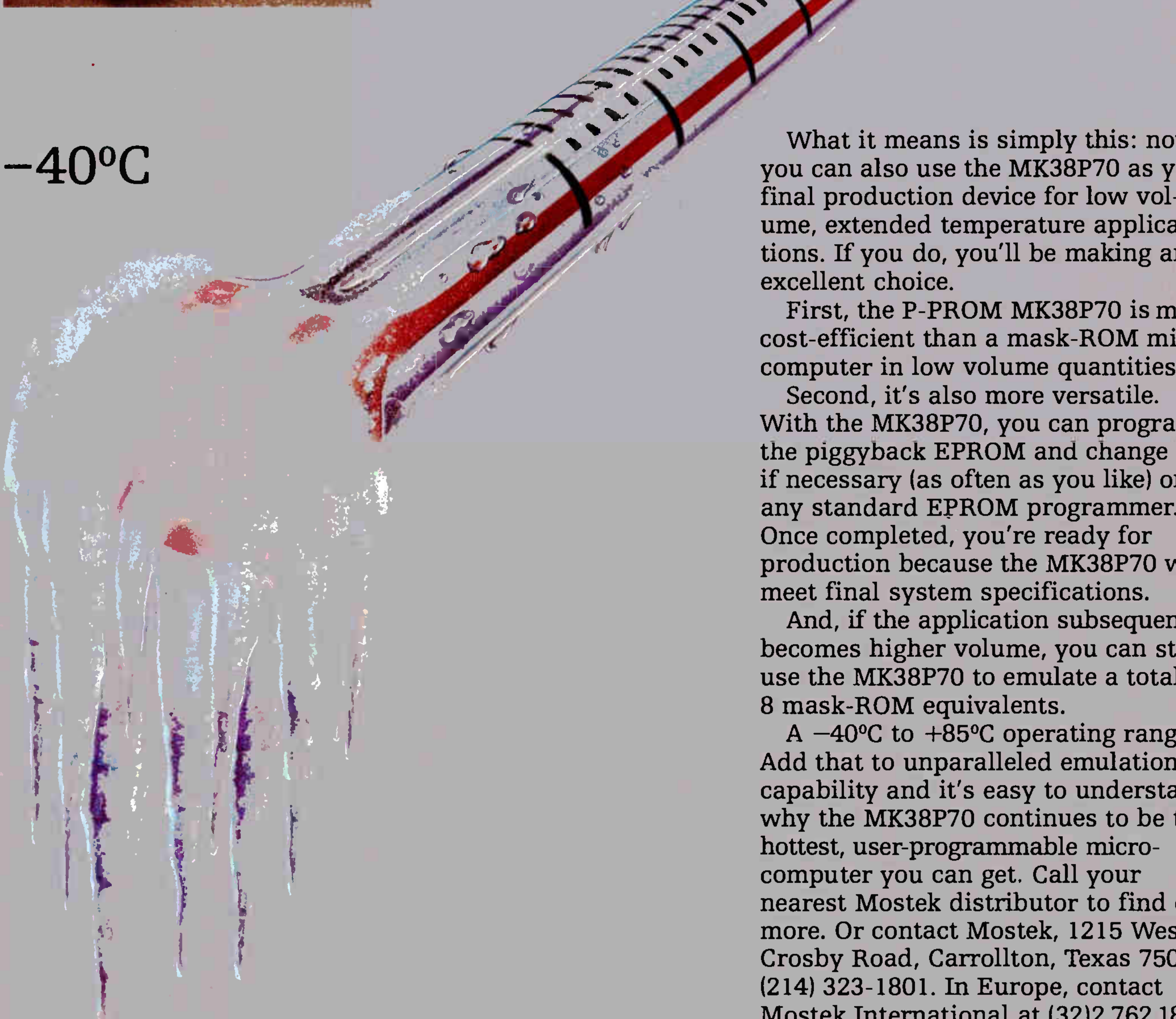

What it means is simply this: now you can also use the MK38P70 as your final production device for low volume, extended temperature applications. If you do, you'll be making an excellent choice.

First, the P-PROM MK38P70 is more cost-efficient than a mask-ROM microcomputer in low volume quantities.

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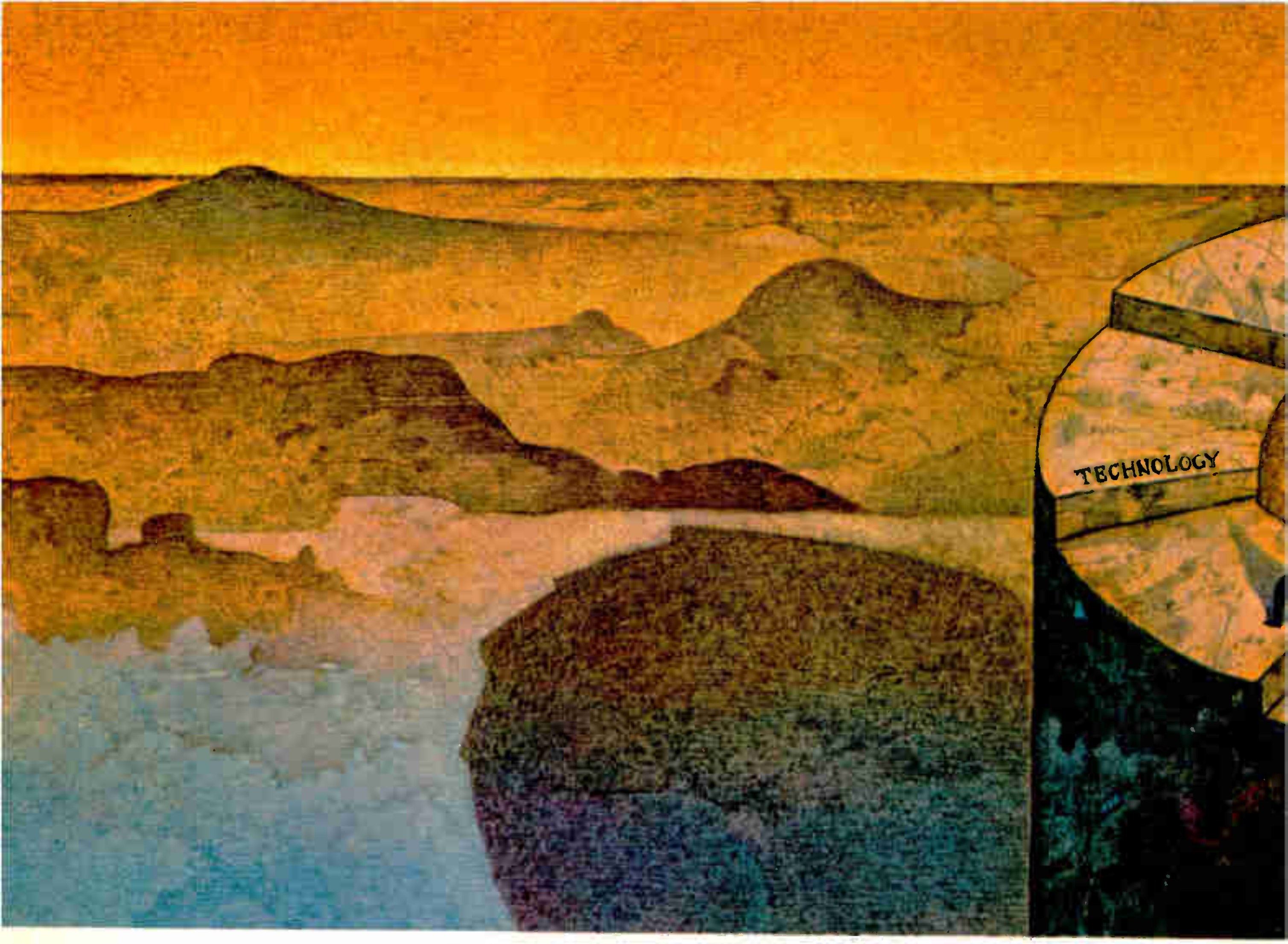


When you're looking in memory design, there's

Back in 1969, when we introduced the world's first integrated 64-bit RAM, we literally started the whole revolution in memory design.

And we've stayed way out in front ever since. Because of all the companies in this business, we're the only one with the common sense to drive the design process in a full circle. From memory systems to microprocessors right on up to the next generation of memories, we just keep raising the level of technology higher and higher every step of the way.

It's that simple. Because we're the only company in the entire VLSI industry that designs a complete, state-of-the-art line of both memories *and* microprocessors.

What it amounts to is a definite feedback loop between our memory and microprocessor divisions. And you get all the benefits from it. Like easy upgrades. And faster design cycles.

You know the way it works: we introduce a new memory, and it drives the technology forward. Our microprocessor people take advantage of this new technology. And use it to design new architecture. Which comes full cycle and drives our memory design group, who take the technology even farther forward.

Of course, it really amounts to momentum. And nobody else in the entire industry has the momentum we do.

Or the track record. We brought you the first MOS static RAM. The first integrated dynamic RAM. The first EPROM. The first 16K E^2PROM. The first 1 megabit bubble. In fact, of the 31 breakthroughs in VLSI over the last decade, we delivered 24 of them first.

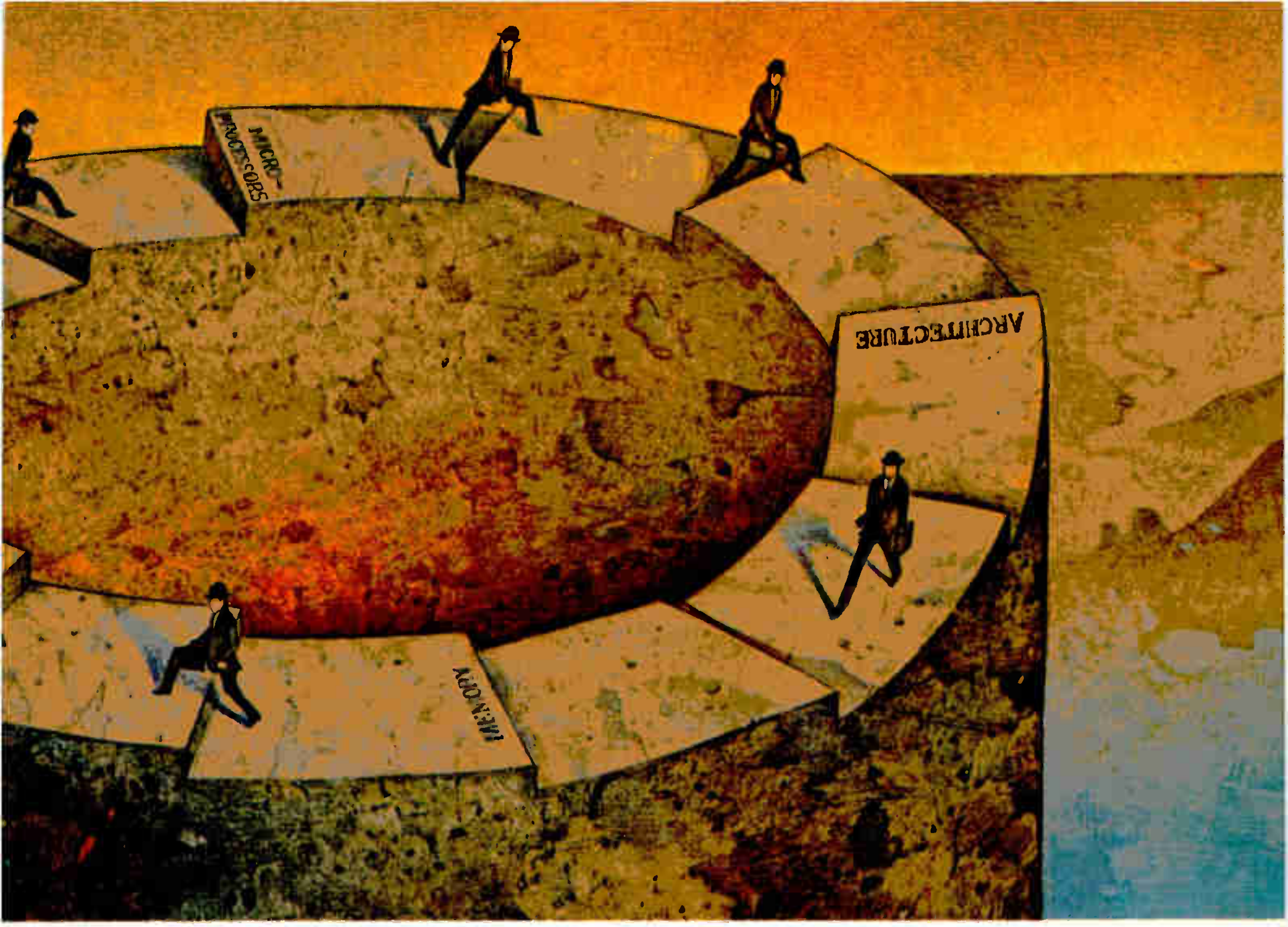
When you get right down to it, nobody else has the breadth we do, either. Our competitors might make memories for a few applications, but only Intel covers the entire scope of microprocessor-based products and gives you memories for every important system application. Commercial and military. Complete with development tools and applications support.

And since we plan to keep coming around full circle this way for years, we've invested an enormous percentage of our profits right back into our design and production capability. So we can deliver all the memory product you need. Right when you need it.

That's the broad picture. Now we'd like to show you product by product, how we're right on the leading edge of memory development.

RAMs

Ever since we introduced the first static and dynamic RAMs, we've gone on to develop just about every major breakthrough in this area to date. We're leading the way with redundancy techniques for high density 16K static and 64K dynamic RAMs. And with our new Series 800 family of RAMs, which we've designed to maximize effectiveness in specific microprocessor applications.



for a real breakthrough only one sensible way to go.

PROMs
Because of our process technology, we've always led the way in faster, denser PROMs, in MOS and bipolar.

In bipolar, we've developed a new process that gives our 16K PROM a 35ns access time. For its density, it's the fastest PROM available today. And with our new 32K, we'll take speed and density even further.

We're way out front with EPROMs, too. Because we invented them in the first place. And we've been upgrading them ever since. By giving you the first 5V only device. By establishing a complete byte-wide family.

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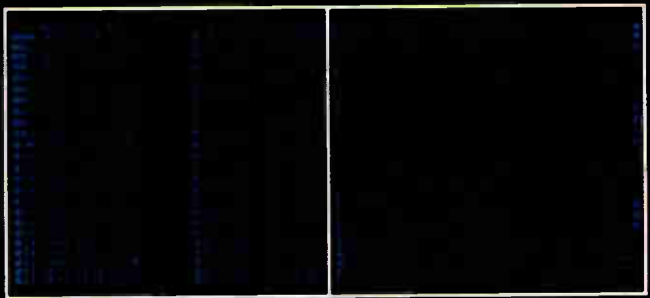
For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.



For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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Electronics newsletter

Exxon sheds technology firms

Exxon Enterprises Inc., New York, appears to be removing some of the eggs from its electronic high-technology basket. This subsidiary of the giant oil company, which has been reported to be unhappy with the results of its investments in that sector, acknowledges that its Optical Information Systems division in Elmsford, N. Y., is up for sale and it has already sold its Star division in Pasadena, Calif., to Storage Technology Corp. of Louisville, Colo. Industry analysts say that Kylex Inc. of Mountain View, Calif., is also being offered for sale, but Exxon would not comment. **The analysts believe that a shift in the availability of petrodollars is behind the moves,** which will result in the consolidation of Exxon Enterprises' Technology Components Group.

That group controls the former Star division, which is developing optical disk drives [*Electronics*, May 5, p. 97]; the Optical Information Systems division, a supplier of laser diodes for optical disks; Kylex, which is developing large-area flat-panel liquid-crystal displays; Epid Inc. of Sunnyvale, Calif., a developer of electrophoretic displays; and Magnex Inc. of San Jose, Calif., which manufactures thin-film heads for magnetic disk drives. Amid reports that the fate of Epid and Magnex have yet to be determined, Magnex president Frederick Lee says that the company "has achieved its milestones, and its position relative to Exxon Enterprises is stable." Epid officials will not comment. At the same time, Zilog Inc., the semiconductor maker that is a member of Exxon's Computer Systems Group, has moved its headquarters from Cupertino to Campbell, Calif.

TI gets 50% yields on 64-K RAMs, shuns redundancy

With monthly production of 64-K random-access memory chips now running at a rate of just over 2 million per year, Texas Instruments Inc. is turning out more than 50% of that in its fastest part—a 150-ns device, with yields high enough to prompt the Dallas firm to continue standing firm against the use of redundancy (see p. 117). **Currently, a total of 170,000 RAMs—150-, 200-, and 250-ns parts—is available for shipment each month.** Yields on the chip are also in the same range as the industry's 16-K dynamic RAM levels for early 1980. TI now has three front-end operations for the 64-K device and makes them in Lubbock, Texas, and Miho, Japan. Two were built specifically for the device and the third was converted from 16-K production.

New firms swap gate-array designs, CAD systems

Two new manufacturers of gate arrays, LSI Logic Corp. of Santa Clara, Calif., and California Devices Inc. of San Jose, Calif., have signed an agreement providing **the first multiple sourcing of a complete gate-array package.** For the right to manufacture and sell the 300-to-1,700-gate HC series of devices that California Devices has been shipping for over a year, LSI Logic will provide the firm with its LDS I design-automation system, which is tailored for designing gate arrays. The LDS I will offer integrated computer-aided design, simulation, layout, and test generation.

Add-in boards promise low-cost color . . .

Datacube Inc. of Reading, Mass., hopes to bring color graphics within the reach of even the smallest original-equipment manufacturer or end user with its VG and QAF plug-in display memory and processor. Built to interface with Digital Equipment Corp.'s LSI-11 Q-bus and Intel Corp.'s Multibus, **the pair of boards has software-controlled black-and-white raster-scan graphics, a palette of many colors, and a price tag of only**

$6,000 in single units—about $4,000 in lots of 10 to 24. First units should become available within about a month.

. . . as full set sports low price

A price breakthrough in the very high-resolution, high-performance range of color graphics display systems is coming from Ramtek Corp. The model RM-9450, with prices ranging from $19,450 to $30,350, will be unveiled by the Santa Clara, Calif., company at the Siggraph/81 conference beginning in Dallas on Aug. 3. **The 9450 has the same performance and resolution as the company's top-of-the-line RM-9400 system, but with only a subset of the 9400's features**—those most often requested by customers of the 9400—and prices approximately 40% lower.

Computer executes 200,000 instructions/s and dissipates 2 W

A fast silicon-on-sapphire microprocessor is the basis of a single-board computer to become available within nine months from Mikros Systems Corp. of Mercerville, N. J. Not only is the system fast for a microcomputer, executing 200,000 instructions per second, but in addition it dissipates only about 2 W. **Furthermore, the 20-in.-square board is compatible with the Air Force's MIL-STD-1750A architecture** and is radiation resistant, capable of withstanding 10^{10} rads. According to its developers, the unit is also easily adapted to the language Ada.

Radiation-hardened 4-K C-MOS static RAM to bow in September

Shipments of a radiation-hardened complementary-MOS 4-K static random-access memory should begin in September, according to the Programs division of Harris Corp.'s Semiconductor Group in Melbourne, Fla. The firm says that its hardening process, which uses localized oxidation rather than etching to define active areas on the chip, **permits finer geometries than earlier techniques.** Only 10% larger than its commercially available HM-6504 counterpart, the 1-bit-wide RAM is latch-up free and can withstand over 2×10^5 rads.

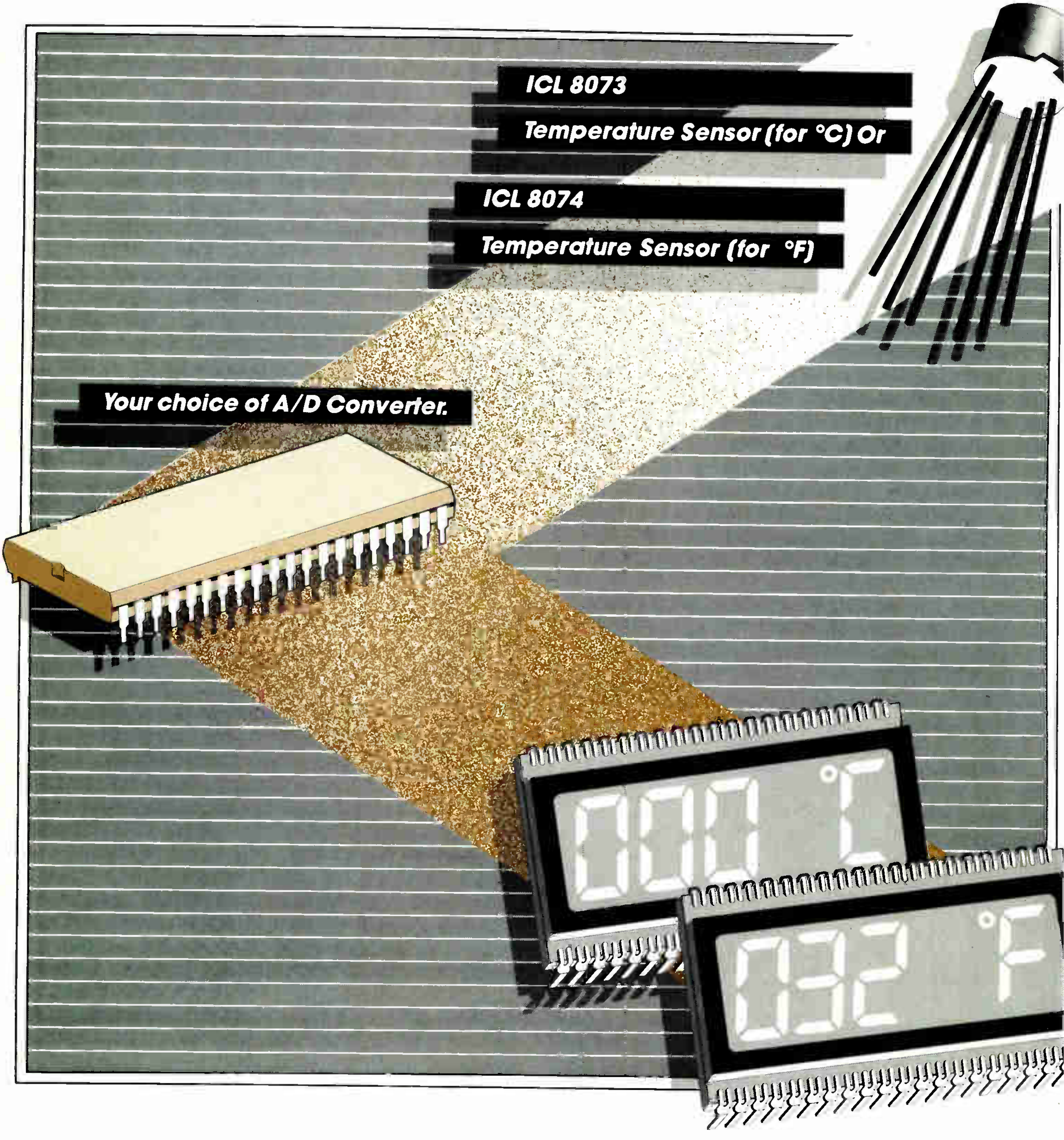
Western Digital pushes Ethernet chip

Moving to beat board-level Ethernet-compatible products off the production line, Western Digital Corp. of Newport Beach, Calif., is planning an August introduction of a single-chip alternative to the technology being developed by Xerox, Intel, and Digital Equipment. **Western Digital is using the token protocol approach to local networking,** utilizing its existing WD2501 packet-switching controller with software written for the application. The communications controller, internally dubbed Alternet, offers media independence, lower cost than board-level products, and communications over longer distances than Ethernet.

Data General's new MV6000 to compete with DEC's VAX 11/750

Data General Corp. of Westboro, Mass., is only weeks away from announcing a new, medium-sized 32-bit minicomputer. Designated the MV6000, **the new super-minicomputer is expected to have a central processing unit closely patterned after that in DG's Eclipse MV8000** and to retain compatibility with the company's 16-bit software library. According to insiders, the machine will be priced to compete with Digital Equipment Corp.'s VAX-11/750.

NEW ONE-CHIP °C OR °F WITH



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AT LAST—OUTPUT PROPORTIONAL TO °C OR °F.

Until now, all IC temperature sensors gave you one output—degrees Kelvin. Which only made life difficult for design engineers, since ninety percent of their applications called for Centigrade or Fahrenheit.

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And these new sensors are already laser trimmed. So you can forget about external trimming and scaling. Forget about precision resistors and amplifiers. Forget about multiple-part assemblies and the errors that creep in. Forget about interchangeability problems.

The bottom line is a better system at lower cost.

NO ADJUSTMENTS.

It's simple. Output voltage from the ICL8073 is directly proportional to degrees Centigrade. From the ICL8074, output is directly proportional to degrees Fahrenheit. So you can go directly to a numeric readout of degrees, for example, or send control information directly to a system in engineering units. Without intermediate conversions.

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Laser trimming gives you a choice of three grades of accuracy: ICL8073 is available in accuracies of 1°, 1.5° and 3°C, with 0.5°, 1° and 1.5°C linearity. ICL8074 comes in 1.8°, 2.7° and 5.4°F accuracies, with 0.9°, 1.8° and 2.7°F linearity.

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There may still be times when you'll want a Kelvin-output sensor. Or a current-output sensor you can move a greater distance from your system. For those times, Intersil's AD590 is your part. It's laser trimmed to 1°C accuracy. Its linearity is 0.5°C over the full range. And it's available in cans and miniature packages.

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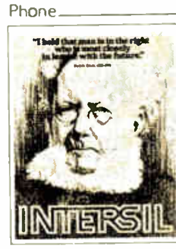

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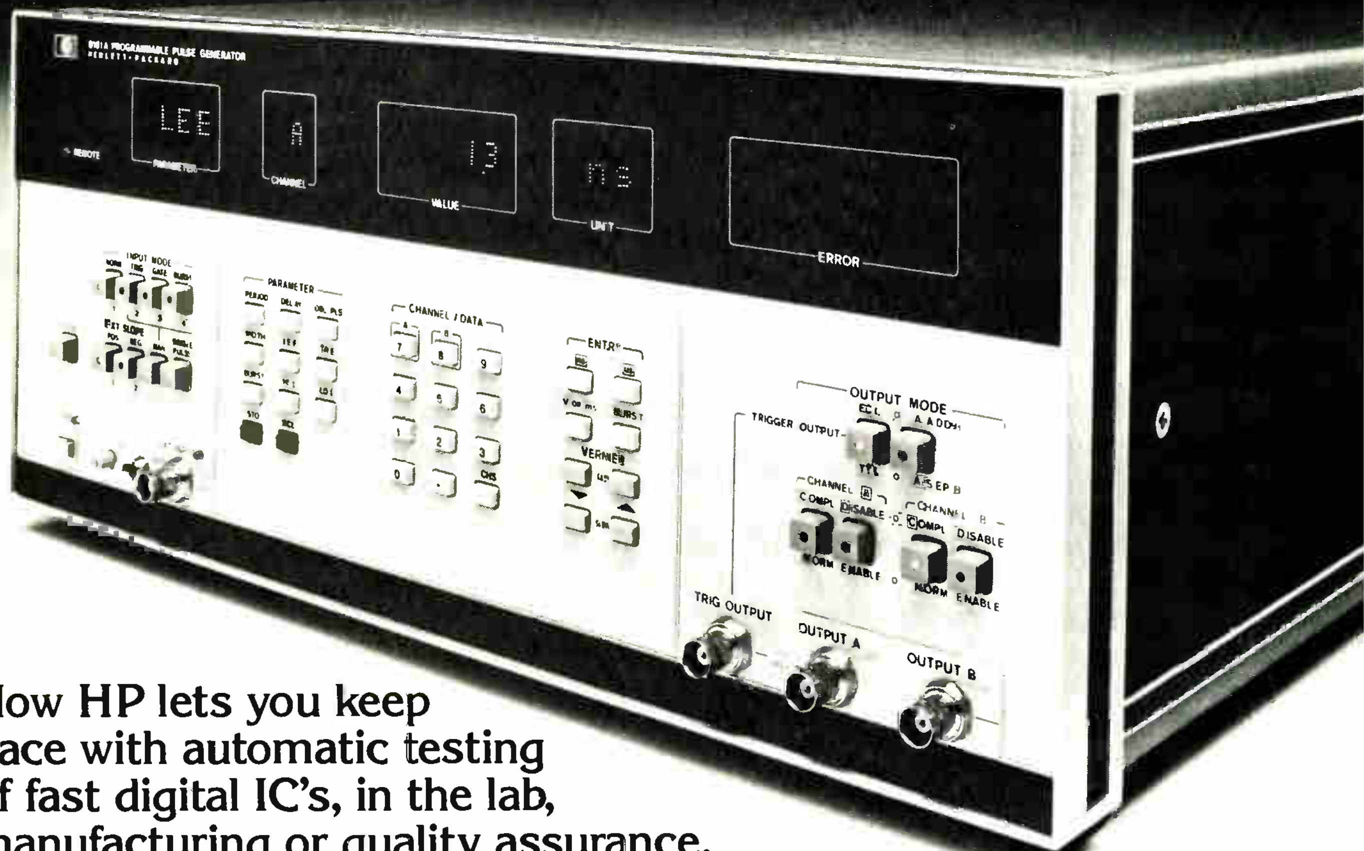

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Laser pulses form connections for system on a wafer

by James B. Brinton, Boston bureau manager

Experimental work at MIT's Lincoln Laboratory uses beam's energy to make or break metalization paths

Semiconductor engineers have been working toward "system-on-a-wafer" integration for years. The increased density and reliability, reduced size, and lower cost brought about through simplified packaging, and the elimination of most wire bonds would make price-performance ratios even more attractive than with today's emerging very large-scale integrated circuits.

Now, research, funded by the Air Force and the Defense Advanced Research Projects Agency, is under way at the Massachusetts Institute of Technology's Lincoln Laboratory, Lexington, Mass., that could produce its first experimental across-the-wafer circuits late this year or early next.

The lab's approach is called restructuable VLSI, or RVLSI. The scheme uses an argon laser to deliver energy pulses that help form conductive pathways of metal-silicon alloy between layers of metalization or that can sever undesired connections. This laser approach to joining logic blocks on the wafer is largely the work of Glenn H. Chapman, research staff member at the lab, and group leader Jack I. Raffel.

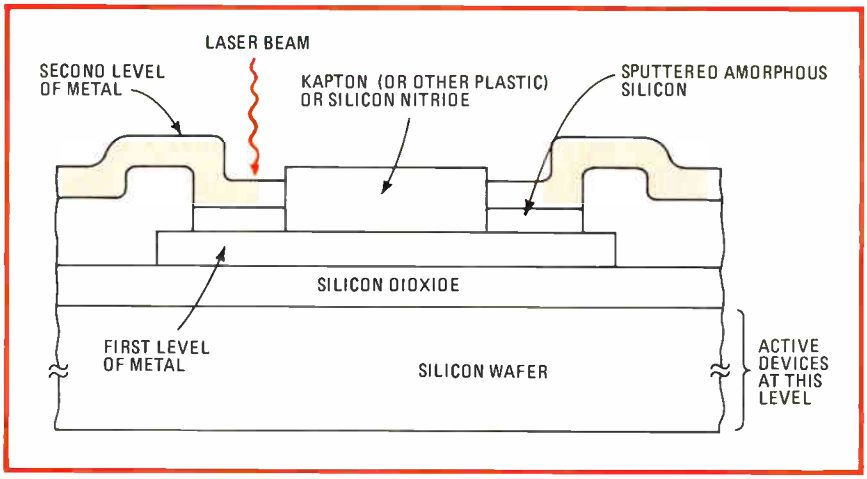
Bus pathways. On a full-blown RVLSI wafer, there might be several LSI- or VLSI-level logic blocks. Instead of dicing them apart, the Lincoln Lab approach would first lay down a set of bus pathways connected to the blocks' probe and input/output pads. Over that would be placed an insulating layer and then another layer of bus metalization, typically running at right angles to the first-level conductors. To connect the wafer's logic blocks, "we use the laser to force contacts between the upper- and lower-level metalizations," Chapman says.

For experimental purposes today, he goes on, "we use a sandwich of first-level metal, a layer of sputtered amorphous-silicon insulation, and on top another metalization layer. When we want to connect the two layers, we fire the laser at a point where upper and lower metal cross each other, using 2-to-5-watt pulses about 1 millisecond long. The result is a very low-resistance connection; we have repeatedly measured resistances as low as 0.1 ohm and get 0.2 Ω consistently. And the system works repeatably—in a recent experiment we made some 4,000 such connections with complete success."

These results were achieved using a lower-level metalization about 0.5 micrometer thick, 0.5 μm of sputtered amorphous silicon, and 0.75-μm-thick second-level metal.

One production method contemplated would be to design wafers with all subsystems present, perhaps redundantly. Each cell would be tested and the good ones used to form a system. Thus, not only would complex systems be possible, but also wafer yields could be high, as bad cells would be bypassed. And the cells would be large ones—like programmable logic or gate arrays. "We are looking at complex functional blocks," Chapman says.

By bus. Most designs envisioned at the lab already use the bus-oriented connection system. Present experimental wafers employ a number of 10-μm-wide bus lines separated by 50-μm spacings. "These dimensions are for global interconnections," emphasizes Chapman. "Device geometries on the order of a micron can



On top of things. Programmed laser beam punches through metalization layers added atop silicon wafers either to form conductive pathways or to sever undesired metal.

be used for internal fabrication."

Two-inch-diameter wafers are now being used; 3-in. wafers will be by early 1982.

There are other refinements to come. Chapman wants to experiment with smaller geometries and thinner insulation layers, as well as with different insulating materials—silicon nitride, for example. If nothing else, because of the need to process wafers at high temperatures, he wants to sandwich in the amorphous silicon with thin layers of silicon dioxide to prevent current leakage and possible short circuits.

The lab now has two experimental wafer-level systems in development. Farthest along is a 4-bit integrator, laser assembly of which could begin by September or October. Further away is a fast-Fourier-transform processor.

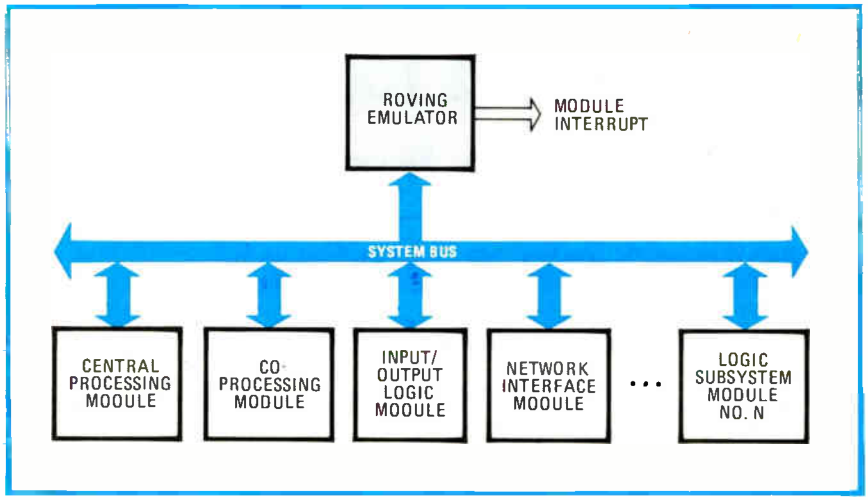
The lab has already done more than zap test patterns. In a demonstration for DARPA, the group used an off-the-shelf complementary-MOS gate-array wafer. Rather than dicing it, it laid down a RVLSI interconnection system atop it. The group then proceeded to connect the various sections of the wafer, successfully bringing in power and control signals and bringing out output signals to the appropriate pads.

Test equipment

Roving emulator checks logic modules

Determining whether a stand-alone computing element works properly is difficult enough; but the task gets even tougher when many such elements are linked together into a distributed network. It can require complex and expensive fault-modeling and error-checking techniques, and often involves backup duplication of each element.

A simpler answer may soon be in the offing, however, in a piece of hardware dubbed the roving emulator. This device could be plugged into a data network and programmed to monitor logic subsystems by switching between them. Researchers at the University of Southern California, Los Angeles, are working to define the emulator more fully under a contract awarded in February by the Department of Defense's Very High-Speed Integrated Circuits program.



Gadabout. The roving emulator proposed at USC would sit on the system bus and mimic sequentially the operation of logic subsystem modules. Comparison of the simulated and actual outputs of a module would help locate a fault, though not in real time.

The emulator is the brainchild of Melvin A. Breuer, professor of electrical engineering at USC and an authority on fault-tolerant computers and very large-scale integration. He came up with the idea several years ago. "The beauty of the emulator," he points out, "is its versatility in being able to rove between the different logic modules."

One at a time. In its basic format, the emulator is intended to monitor one module at a time by independently simulating what its output should be using the actual inputs and comparing this with actual output. These simulations will derive descriptions of the monitored subsystems from special-purpose algorithms and logic. While the project has not reached hardware design, the emulator would most likely consist of a microprocessor and enough memory to handle these simulation programs.

In its relationship to the data network, the emulator has an observer role that does not interfere with system operation in any way, according to Breuer. The only change required in the logic subsystems themselves would be brief, microsecond-range interrupts to acquire state data from module registers for use in the simulations. The emulator runs continuous off-line processing that compares its simulations with actual results and tells "which module is healthy and which is not working," Breuer explains.

Because of the lag between observing the operation of the logic modules and doing the simulations, the roving emulator is not suitable for real-time performance monitoring of the kind usually needed for process control. But it can be useful in checking, for example, business systems, where immediate detection is not imperative. "It fills this gap and others where you don't need a zero-error rate," says Breuer. The emulator also could be designed to run at speeds fast enough to close much of the real-time gap.

Since the VHSIC program is working toward producing military signal-processing and command-and-control equipment where distributed intelligence would be commonplace by the middle or late 1980s, the roving emulator could fit in well with these project objectives.

Fundamental properties. Breuer's researchers are now focusing on several fundamental emulator properties concerning speed and the optimum length of time, or window, for monitoring each logic module. Current thinking is for the emulator to be built in a configuration of several chips. But actual chip fabrication would come later since the present contract is for research only. The VHSIC Phase III support technology contract awarded Breuer is for one year, totals $240,000, and is sponsored by the Naval Surface Weapons Center, Dahlgren, Va.

The award is one of three VHSIC support awards at USC. The others include a three-year design automation effort, budgeted at $281,000 by the Army Electronics Technology Devices Laboratory at Fort Monmouth, N. J., and being performed by Breuer and colleague John Nelson. The resultant interactive graphics system will be used in a VHSIC design course for weapons being set up by Nelson. The other award—for $240,000—was given to Nelson by the Naval Ocean Systems Center in San Diego to explore the use of MOS technology for designing radar signal processing architectures with very high-speed ICs. **-Larry Waller**

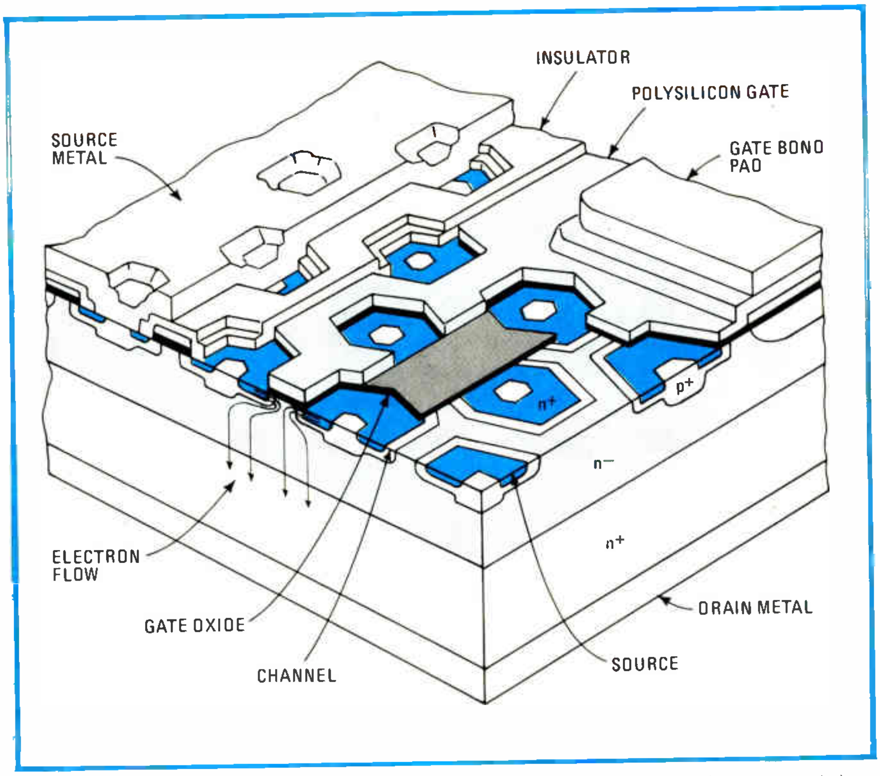
Components

RCA slates entry into power MOS field

Long a major supplier of bipolar power transistors, RCA Corp.'s Solid State division will soon be filling an empty but important space in its catalog—the one for power MOS field-effect transistors.

It is a market the company could not afford to miss, according to Frank J. Rohr, manager of product marketing for power devices in Somerville, N. J. Switching-mode power supplies, which benefit from the high speed and low drive power of the MOS devices, are one of the largest markets for power semiconductors, he points out. And in the future, power MOS will be a must.

"After power supply makers scale up their present 20- to 40-kilohertz designs, they are not going to go to 60 to 80 kHz," Rohr says. "They are going to make a quantum leap to 200 kHz and above."



Out the back. Electrons from hexagonal sources flow laterally beneath the gate and then vertically through the n$^-$ layer to the drain on the back of the power MOS die.

It is at this frequency range that RCA is aiming its new devices. Present design needs will be met by RCA's Switchmax line of bipolar transistors, according to Rohr. These will be expanded in September to include plastic-packaged devices rated up to 5 amperes and 500 volts. They should cost 40% less than current devices. Transistors rated to 1,000 V will also be available.

RCA believes it has benefitted from holding off on its entry into the power MOS market. "I think we have succeeded in learning some things from other people," Rohr says. An evaluation of competing designs led to the choice of a vertical-conduction device with a hexagonal source as the one promising the greatest reliability and reproducibility at the lowest cost, he continues. Moreover, "volt-amperes per square mil of silicon is highest for a six-sided cell."

The cell design is not unlike that in International Rectifier Corp.'s two-year-old Hexfet line and is similar to other vertical MOS devices [*Electronics*, May 22, 1980, p. 143].

"We've been aware of RCA's efforts for a long time," says Alex Lidow, vice president for research and development at IR, "and we're flattered they've chosen this design."

Source diffusions (n$^+$) are hexagonally shaped in p$^+$ wells, as shown in the figure. The channel, or inversion layer, exists in the p$^+$ region (shown in white) beneath the gate. Electrons first flow laterally a short distance through the channel, and then vertically through the n$^-$ layer to the drain on the die's back side.

A joint effort with RCA's research laboratories in Princeton, N. J., development of the process began in 1979. Production equipment is now in place, and the first parts will be out early in the fall. Initial offerings will be two low-voltage (up to 120 V) devices now being fine-tuned for a low on-resistance. Future, higher-voltage transistors will be made with essentially the same process.

"A single process for all the parts," notes Rohr, "means we can move down the learning curve faster." By paying attention to defects and keeping process yields high, RCA

GE cuts rectifier costs with plastic

General Electric Co. is bidding for a share of the low-end power-rectifier market with packages that are lighter and smaller—just 1 inch high overall—than conventional stud-mounted types. The usual glass-to-metal housings are replaced by phenolic ones. Also, the customary large and costly copper stud mounts are replaced by flat steel bases mounted conveniently from above by small screws that leave more room for fins on the underlying heat sinks.

The Hi-Line diodes have the same performance while costing 30% to 40% less than the 100-ampere to 300-A parts offered by Westinghouse and International Rectifier, according to GE. "This is a very mature and cost-sensitive market," says product planner Donald E. Lord, of the Semiconductor Products department, Auburn, N. Y., "and we intend to become a major supplier."

Now under GE's wing, Intersil Inc. of Cupertino, Calif., is also expected to benefit by applying plastic technology to its power-MOS parts. The low-end rectifier market available to U. S. suppliers amounts to around $70 million annually and is growing steadily at 5% to 7% per year. The major applications for these 800-volt diodes are in arc welders, battery chargers, and power supplies. "Once we have established this high-volume base," adds Lord, "we will be looking at fast-recovery and high-voltage diodes." **-R. B.**

hopes to make MOS FETs more competitive with bipolar switching transistors, which are still one third to one quarter the cost of their current MOS counterparts, he adds.

The full line, to be completed in the first half of 1982, will include both n- and p-channel devices, with drain current ratings of up to 12 A in the lower voltage parts and up to 4 A for 500-V devices. Furthermore, Rohr says, test data from the first 1-A devices show good performance at switching frequencies of up to 50 megahertz, easily qualifying RCA's new MOS FETs for the switching power supplies that operate at hundreds of kilohertz.-**Roderic Beresford**

Communications

AT&T wins a battle to enter new markets

American Telephone & Telegraph Co. got most of what it wanted in mid-July. The Senate Commerce Committee voted 16 to 1 to approve S. 898, a bill that would allow AT&T to move through separate subsidiaries into new competitive markets for unregulated telecommunications and data-processing equipment and most services. The Senate committee action took a mere 90 minutes. Yet though AT&T won a major battle, as one competitor noted, "They still haven't won the war." Among the remaining battles:

■ A new round of hearings by the Judiciary Committee whose chairman, Strom Thurmond (R., S. C.), blocked a floor vote by getting the bill referred to his committee to review antitrust aspects.

■ Actions in the House, where communications subcommittee chairman Timothy Wirth (D., Colo.) is holding back on the introduction of a bill until the ongoing Federal antitrust suit in Washington's Federal district court is resolved.

■ Dealing with the concerns of trial judge Harold H. Greene, who is reported to be upset that the Reagan Administration is considering dropping the suit [*Electronics*, June 30, p. 57]. With the prosecution recently completed, Greene believes that any judgment about dropping the case is his alone to make.

■ A renewed and equally controversial inquiry by the Federal Communications Commission into the purchasing practices of the 23 Bell System operating companies. The inquiry, approved the same day as the Senate committee vote, indicates that those companies are still too

FCC to reexamine Bell bias toward Western

The Federal Communications Commission will take a new look at the equipment-purchasing practices of Bell System operating companies. It wants to prevent their favoring Western Electric Co. at the expense of competitors that might provide better equipment at lower cost. But though all the commissioners see their notice of inquiry, Common Carrier Docket 80-53, as needed, a number of them dissent from the staff recommendation on how best to open the Bell companies to competition.

In a 1977 ruling on Docket 19129, the FCC found that those companies' procurement practices "created a bias in favor of Western Electric products." Under the latest staff proposal, the firms would have to create and control a central organization that would treat Western Electric and its competitors equally, performing technical, economic, and quality surveillance of all products and making recommendations on purchases.

Dissenters. Commissioner Abbott Washburn agreed with the need for a new look at the issue, but has "doubts about the staff's proposal—it does not fully address the problem and could create a paper mill for the commission." Moreover, the AT&T Long Lines department is excluded from consideration, yet its 1981 construction program totals $1.3 billion. "Is this volume not a part of the procurement and standardization design?" he asks.

Commissioners Joseph R. Fogarty and James H. Quello also believe the procurement issue is worth reexamination, but charge that the staff plan would result in the Bell System's *de facto* divestiture of Western Electric. Adoption of the staff recommendation, they argue, "would compel what the Justice Department has thus far failed to accomplish in two law suits, what the trial staff unsuccessfully recommended in Docket 19129, and what Congress has so far refused to legislate—divestiture." Searching for a better way to open Bell's purchasing to fair competition, the FCC asked industry for comments by Oct. 1 on the new inquiry, with replies due by Nov. 15. **-R. C.**

closely tied to Western Electric Co., AT&T's manufacturing arm ("FCC to reexamine Bell bias toward Western," p. 42).

Under S. 898, AT&T would have six years to set up one or more separate, unregulated subsidiaries to make and sell any competitive products and services, excepting only burglar and fire alarm systems linked to a telecommunications network. That would lift the constraints of the 1956 Federal antitrust consent decree that bars AT&T from everything except the telephone business. The FCC and its state counterparts would continue to regulate basic telephone services, however.

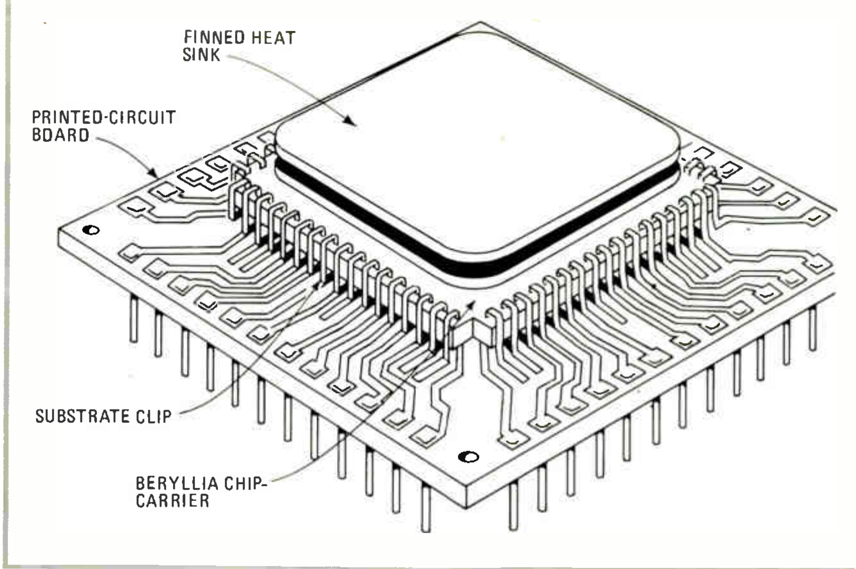
Mixed reviews. Chairman Robert Packwood (R., Ore.) of the Senate Commerce Committee, the principal sponsor of the bill, called the vote "a momentous occasion." The sole dissenter, Sen. Ernest F. Hollings (D., S. C.), former chairman of the Communications subcommittee, declared that S. 898 is "an AT&T bill," calling it "a cut and paste and patch job of what Bell would accept." Hollings lost eight to nine on an amendment that would have required AT&T to sell at least 10% of a subsidiary's stock to the public.

Perhaps the biggest battle to come will be in the Democrat-controlled House, where heavy lobbying by both sides is already in progress. Should efforts to achieve a compromise or block action there fail, competitors of AT&T suggest that any legislation may be challenged in court. **-Ray Connolly**

Packaging

Beryllia carriers cool hot chips

Chip-carriers will undoubtedly supplant dual in-line packages as the dominant package for large, dense integrated circuits. But the power-handling capability of today's alumina ceramic carriers is already beginning to look inadequate for the junction temperature requirements of tomorrow's very large-scale integrated circuits. Beryllia (beryllium oxide) now looks a likely candidate for housing the superchips of the future because it dissipates more power than alumina.



Heat beater. To determine the thermal performance of chip-carriers, Sperry Univac tested them sandwiched between a finned heat sink and a small pc board.

A handful of companies, among them computer maker Sperry Univac of Blue Bell, Pa., and General

Plastic chip-carriers show they can take it

Another important integrated-circuit package that recently passed environmental tests is the premolded plastic chip-carrier [*Electronics*, June 30, p. 39]. Researchers at Bell Laboratories, Murray Hill, N. J., checked out three sizes: a 24-lead type from Amp Inc. and 28- and 68-lead types from Bell. The Amp design was injection-molded with Ryton R-4, a glass-fiber–filled polyphenylene sulfide, while the Bell carriers were transfer-molded in Dow Corning DC-631, a fused silica and glass-fiber–filled silicone epoxy.

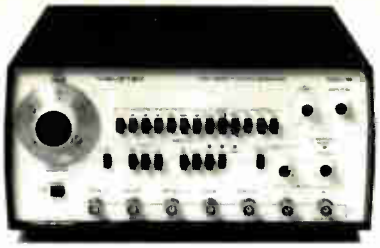
Each carrier had a special silicon-nitride–passivated chip bonded into its cavity and coated with either RTV silicone rubber or a drop of silicone gel.

The accelerated environmental tests consisted of aging at 80°C and 85% relative humidity; +125°, +150°, and +175°C aging under a 40-volt static bias; and −40° to +150°C thermal cycling without bias. In addition, thermal cycling and flexural tests were done to gauge the reliability of the solder joints between chip-carriers and circuit boards.

RTV-encapsulated chips had no corrosion failures in more than 2,000 hours of 85°C, 85% RH testing, according to Bell. But some gel-encapsulated devices did fail.

No temperature-related chip failures were produced by aging up to 175°C. Thermal cycling made a few solder joints fail, mostly because of faulty wire bonding. Overall, the tests showed both versions of the chip-carriers to be highly reliable, Bell concluded. Researchers calculate that the more than 2,000 hours of failure-free operation of the RTV-encapsulated devices in an 85°C, 85% environment translates into a failure rate of less than 100 FITs (failures in 10^9 device hours) after 40 years in a worst-case central-telephone-office environment.

Bell Labs is currently using chips in 68-lead plastic chip-carriers from Amp in several applications. One is in error-correction devices in the processor of an electronic switching system. The same 68-lead carrier is also used to house a diagnostic chip in a business communication system. **-J. L.**



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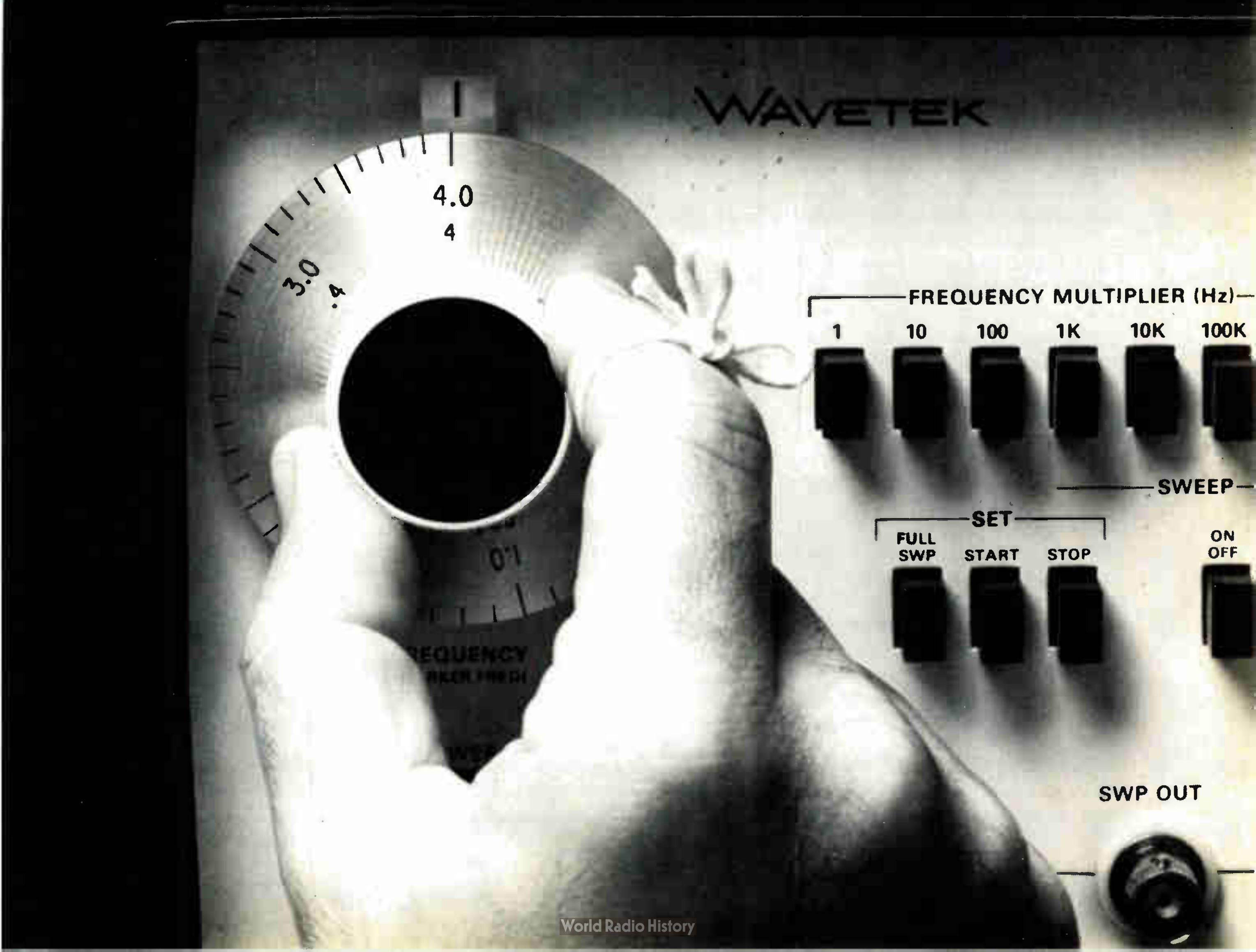


Electric Co., Schenectady, N.Y., already have started preliminary work on BeO materials for packages that could dissipate 3 watts or more and still keep the chip's junction temperature at acceptable levels. That is possible with beryllia because it conducts heat more than seven times more effectively than alumina (aluminum oxide), whose thermal conductivity is 0.066 calorie/second-centimeter-°C compared with 0.52 cal/s-cm-°C for BeO. However, the performance has to be paid for, so chip-carriers made of the higher-conductivity material will probably cost two or three times as much as those of alumina.

Powered up. In order to compare beryllia and alumina in real-world conditions, rather than by computer modeling, Sperry Univac engineers ran thermal tests on 68-terminal leadless chip-carriers. The test setup was designed to determine the thermal resistance, from the junction to the surrounding ambient air, of carriers dissipating the same power—3.5 W in this instance—while being cooled in a small wind tunnel. As for the carriers, those of alumina were stock Joint Electron Device Engineering Council Type A 68-pin units. Those of beryllia, with identical dimensions, were supplied by Brush Wellman Inc., Elmore, Ohio.

For the tests, the carriers were each loaded with a special heat-generating and -sensing die and fitted with three-fin aluminum-alloy heat sinks. Then, using conventional substrate clips, the carriers were soldered cavity down to a small epoxy-glass printed-circuit board. The die simulated emitter-coupled-logic chips of LSI density. Each had nine independent circuits on a common substrate, and each circuit, in turn, was made up of one silicon diode and six diffused resistors. The resistors heated the chip, and the resulting forward-voltage drop of the diode, calibrated against known temperatures before the test, accurately indicated the junction temperature.

As expected, the beryllia units performed better. In fact, their superiority turned out to be much greater than calculated. Instead of the pre-

News briefs

White laser uses relatively low power

Pushing towards a compact, low-power laser unit for commercial applications, engineers at Xerox Electro-Optical Systems, Pasadena, Calif., have developed a white laser that combines three primary colors—red, blue, and green—from one hollow-cathode tube. Also, the unit can emit single colors for a variety of applications such as providing color for printing, holographic recording, and medical endoscopy. The tube uses a helium-cadmium-vapor mixture and only 200 to 300 watts of power—compared to a kilowatt for other such systems. It is made of metal and ceramic and is cooled by air convection instead of bulkier water-cooling. Commercial applications are three to five years away, according to S. C. Wang, head of development at the Xerox division.

Hughes radars and missile reported as espionage targets

The most crucial material allegedly passed by Hughes Aircraft Co. radar manager William H. Bell to a Polish agent may have been details on the passive radar for the low-flying bomber program, which is known as Stealth for its ability to avoid detection [*Electronics*, Sept. 11, 1980, p. 46]. That possibility is not yet confirmed and is still under investigation, sources report.

Two other programs of the Culver City, Calif., company that sources are more sure were compromised by Bell's alleged espionage include the Low Probability of Intercept Radar, a developmental program supported by the Defense Advanced Research Projects Agency and the Air Force. The radar could help detect large enemy-troop concentrations beyond the horizon. The other reportedly compromised effort is a one-man fire-and-forget missile for Army use against tanks and low-flying aircraft.

Motorola consolidates Japan activities, names new managers

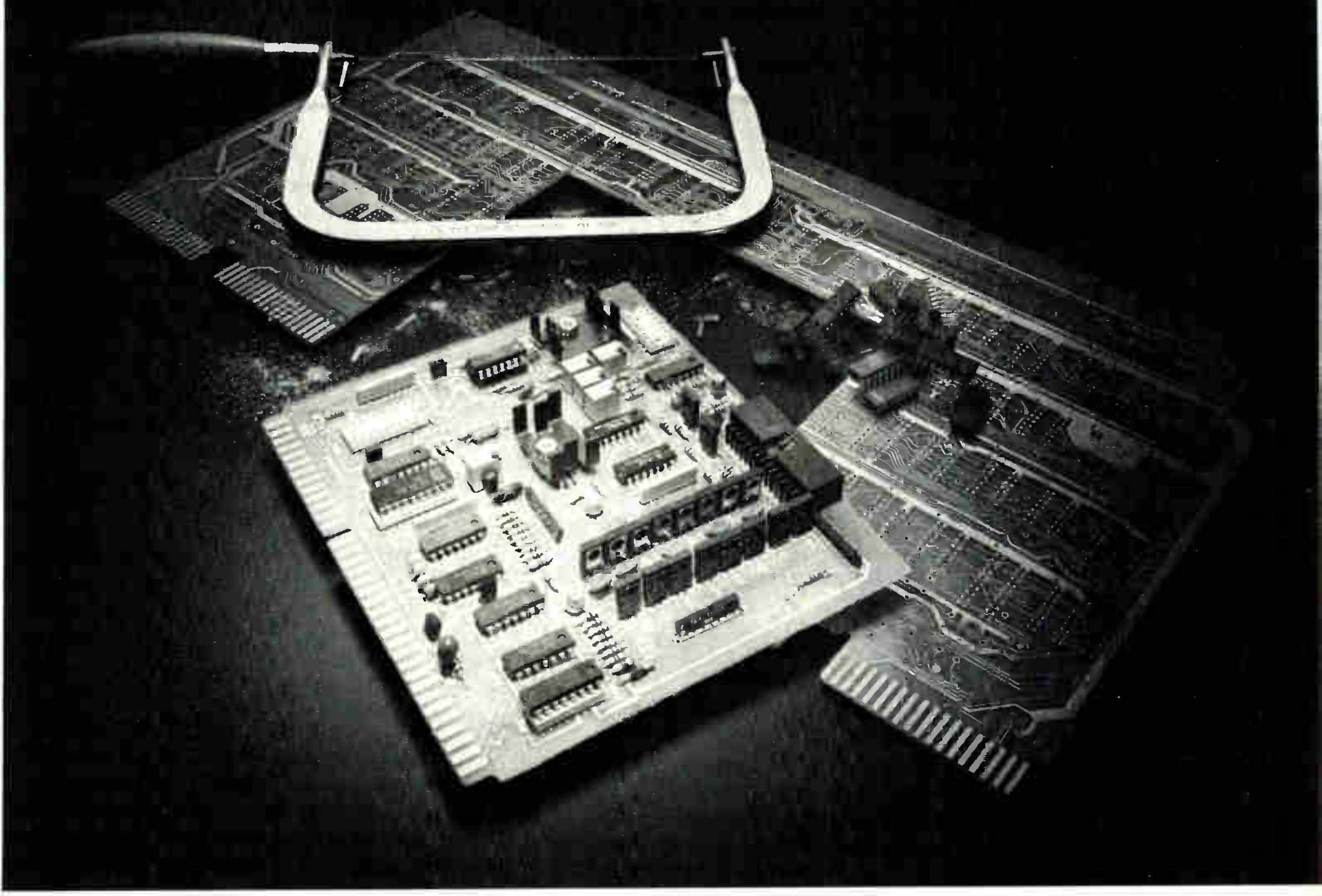
Signaling an increased emphasis on penetrating the Japanese market, Motorola Inc. is planning to consolidate its existing operations there under a new company, Nippon Motorola Ltd., and is creating a new corporate post with responsibilities for all Motorola activities in Japan. Stephen L. Levy, senior vice president and chief corporate staff officer, will assume the new title of senior vice president, Japanese operations, on Sept. 1. Replacing Levy is John R. Welty, who will move to the company's Schaumburg, Ill., headquarters from Phoenix, Ariz., where he is currently senior vice president and general manager of the Semiconductor Group. Welty's move up touches off a string of promotions within the Semiconductor Group, which under the new structure will be known as the Semiconductor Sector.

Replacing Welty in the top semiconductor spot is Gary L. Tooker, who will leave his current post as vice president and general manager of the International Semiconductor division. No. 2 man in the semiconductor hierarchy will be James R. Fiebiger, [*Electronics*, June 30, p. 14]. As vice president and assistant general manager of the Semiconductor sector, Fiebiger will fill the post in Phoenix held by Al Stein, who left last month to take a position with Arrow Electronics.

Spread-spectrum technology gets look from FCC

The Federal Communications Commission, concluding as a result of a study that spread-spectrum technology may now be cost-effective in civilian applications, has begun a public inquiry into whether advanced-class amateur radio users should be allowed to experiment with it. Experiments would be allowed in three bands: 50 to 54, 144 to 148, and 220 to 225 megahertz. The FCC is also opening public discussion as to whether radio-location applications should be allowed in the 420 to 450-MHz band. According to the study, by Walter C. Scales of Metrek division, Mitre Corp., McLean, Va., a promising application could be in mobile radio communications. Short-range service with random-channel access could be obtained with a slow-frequency-hopping system. He noted, however, that spread-spectrum designs require "substantial development and are not likely to be implemented soon."

Common sense logic.



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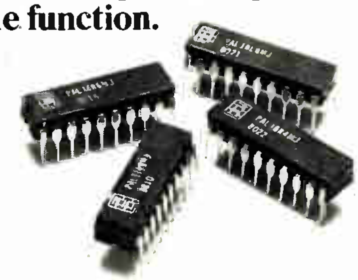

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than calculated. Instead of the predicted difference of 1°C/w, the measured value was 5°C/w.

More interest. General Electric is fired up for beryllia development as well. The company has a Phase III contract in the Department of Defense's Very High-Speed Integrated Circuits program to make an improved-performance package. The objective is a multilayer beryllia package, with all layers cured in a single firing, that has more than 100 pins and is compatible with standard pc-board technology.

Brush Wellman is a strong contender for subcontracting work in this development and has gone ahead with a preliminary design for a four-layer, two-tier leaded package. Thermal modeling suggests the chip-to-ambient thermal resistance will be below 4°C/w. That is almost a two-fold improvement over the resistance of present packages. **-Jerry Lyman**

Computers

Sperry Univac shifts minicomputer gears

After four years of struggling with its minicomputer operation without making much headway, Sperry Univac has begun a determined thrust to sell in its own backyard. It is aiming its efforts at the existing base of Sperry Univac mainframe users, hoping to sell them distributed processing equipment.

The new focus comes amid a restructuring of the Irvine, Calif., branch's product line and its establishment as a profit-and-loss center within the parent company.

Complete control. Since it was purchased from Varian Associates for around $25 million in 1977, Mini-Computer Operations, as it is called, has floundered with little or no direction, acknowledges Neil Gorchow, who recently took over as vice president and general manager. A 25-year veteran at Sperry Univac, Gorchow is the first executive in a while to have complete control.

In past years, control was diffused. The marketing department, for example, reported to three separate areas within the parent company, and other segments were similarly divided. The move to centralize control is designed "to give [the minicomputer operation] proper direction and to make it stand on its own two feet," Gorchow says.

Those feet have left small footprints indeed. Sperry Univac declines to release sales figures, but Gorchow reports that one of the corporate "disappointments is a lack of market share."

In a market survey released last year, Creative Strategies International, San Jose, Calif., ranked Mini-Computer Operations 19th in sales in 1979, placing it at an annual level of $55 million, or 1.1% of the total minicomputer marketplace. For 1980, a review by Sperry Univac had its minicomputer bookings increase by 38%, but this was about equal to the overall growth of the minicomputer market.

For Gorchow, then, there is little place to go but up. He will team his sales force with the Sperry Univac sales team, aiming at the $12-billion installed base of equipment that already exists.

His sales efforts will be built around the V-77 general-purpose, 16-bit processors acquired from Varian. This line basically covers the middle of the minicomputer range, competing against product lines like the PDP-11 from Digital Equipment Corp. and the Eclipse from Data General Corp. However, a year-long series of new product announcements has signaled a shift away from the company's well-known emphasis on engineering and scientific minicomputer markets.

Changing the line. These new offerings have sought to provide a measure of compatibility between Sperry Univac's mainframes and minicomputers. For example, controllers have been developed so that several of Sperry Univac's mainframe peripherals can be used with the V-77 line.

New software has been developed too. The result is a general beefing up of systems packaged for the man-

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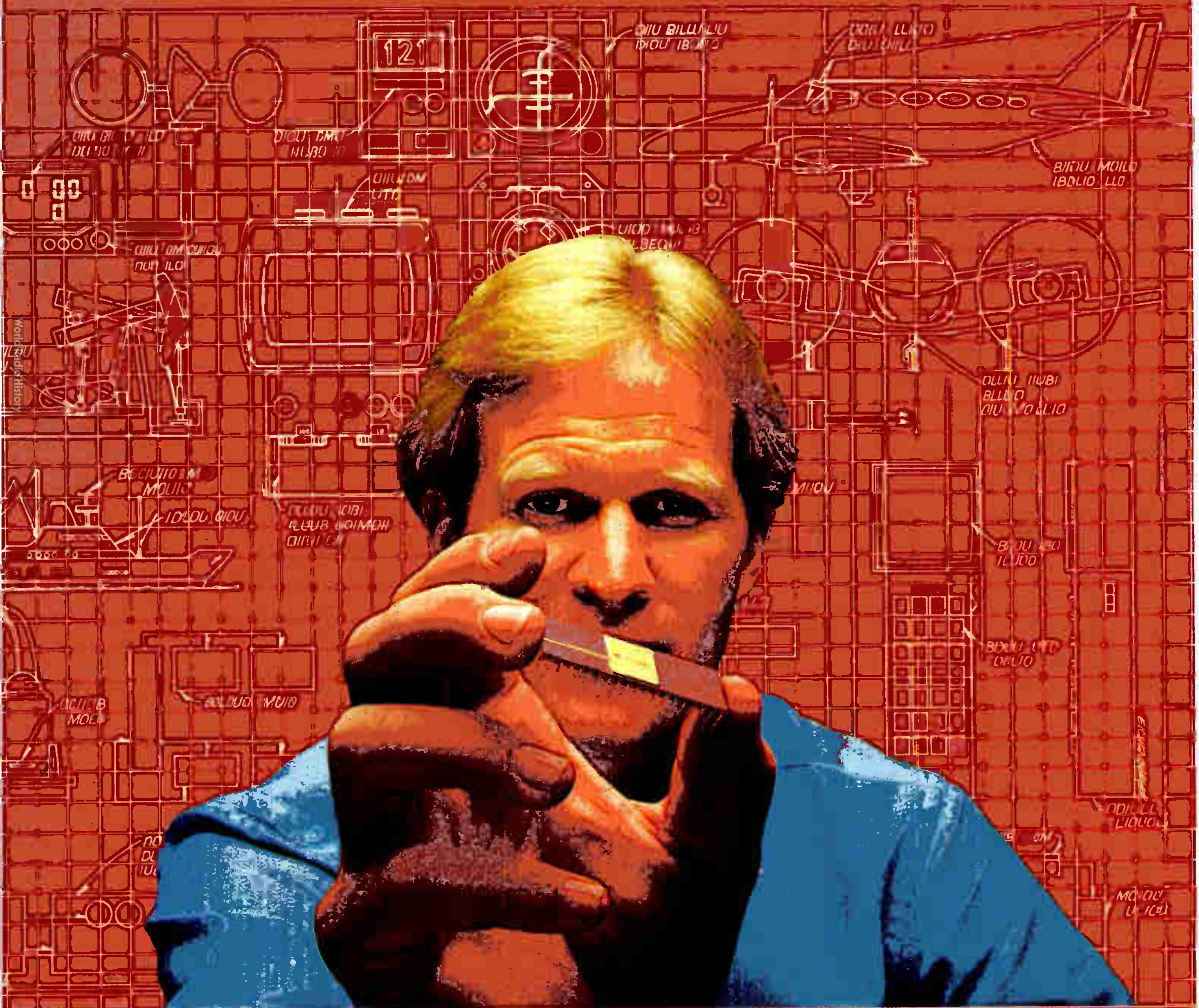

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SPECIAL ISSUE

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The best features of two popular NMOS chips are now available in CMOS. But not just any CMOS. National's high density P²CMOS yields a low power microprocessor family that matches NMOS speeds.

The NSC800 offers the multiplexed address and data bus of the 8085 and the sophisticated register and instruction set of the Z80. By taking advantage of a multiplexed address and data bus, we were able to free up extra pins and put more functions on the CPU, such as five interrupt levels, clock generation, bus control, and a unique power-save feature.

The NSC800 CPU uses the powerful 158 instructions, 10 addressing modes, and 22 registers of the Z80. Fully Z80 software compatible, the NSC800 also executes 8080 and 8085 code (with the exception of the RIM/SIM). Yet the NSC800 dissipates only 50mW operating at 5V at a 2.5MHz clock speed.

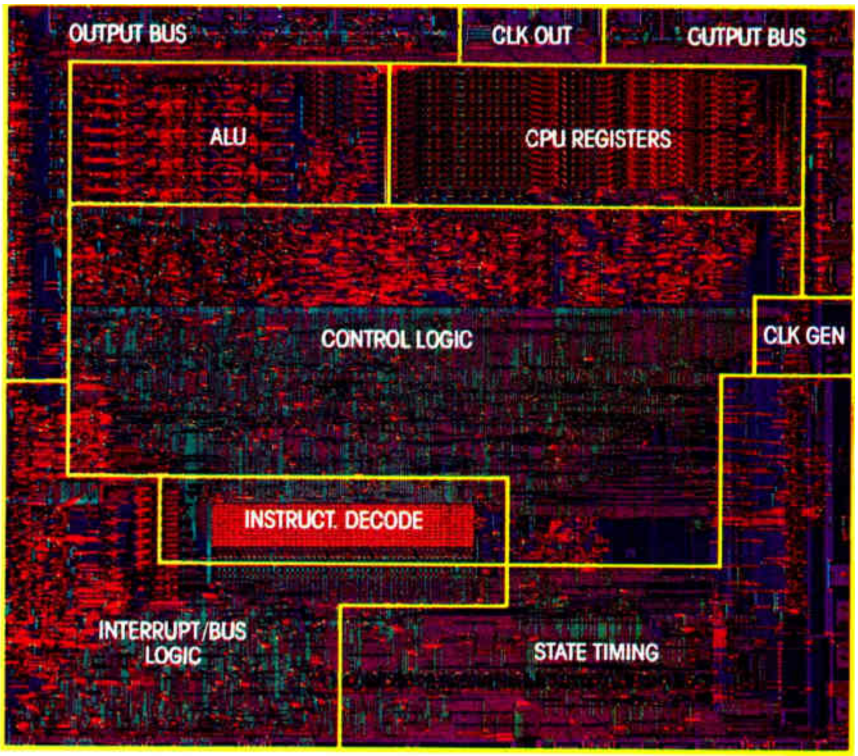
The other family members are the NSC810 RAM-I/O-Timer and the NSC830 ROM-I/O. Featuring two programmable 16-bit timers and 22 I/O lines, the NSC810 also provides 128 bytes of RAM.

The NSC830 provides 2K bytes of ROM plus 20 additional I/O lines. For extra design flexibility, all 42 I/O lines of the NSC810 and NSC830 may be independently defined as inputs or outputs.

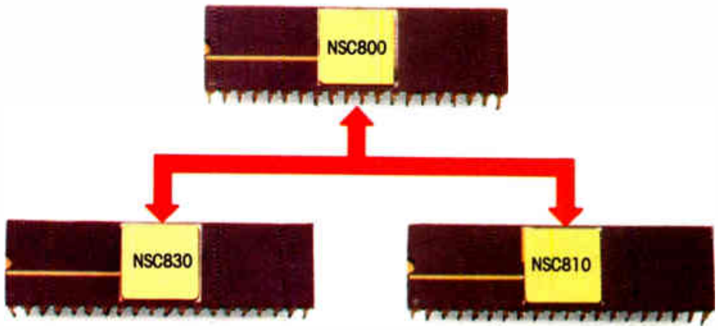
Additional P²CMOS support. A new line of logic circuits is also available. This family has the low power appetite of CMOS, while approaching LS speeds. The MM74PC04 hex inverter, for example, dissipates only 75μW, but boasts a propagation delay of just 12ns.

If memory expansion beyond the 810 and 830 is required, National has you covered there, too. The NMC6514 RAM family and the new NMC27C16 and latched NMC6716 EPROMs match the NSC800's speed and low power.

P²CMOS makes it possible. The goal: keep the attraction of low power, but boost the speed and circuit complexity.



The powerful NSC800 dissipates only 50mW.

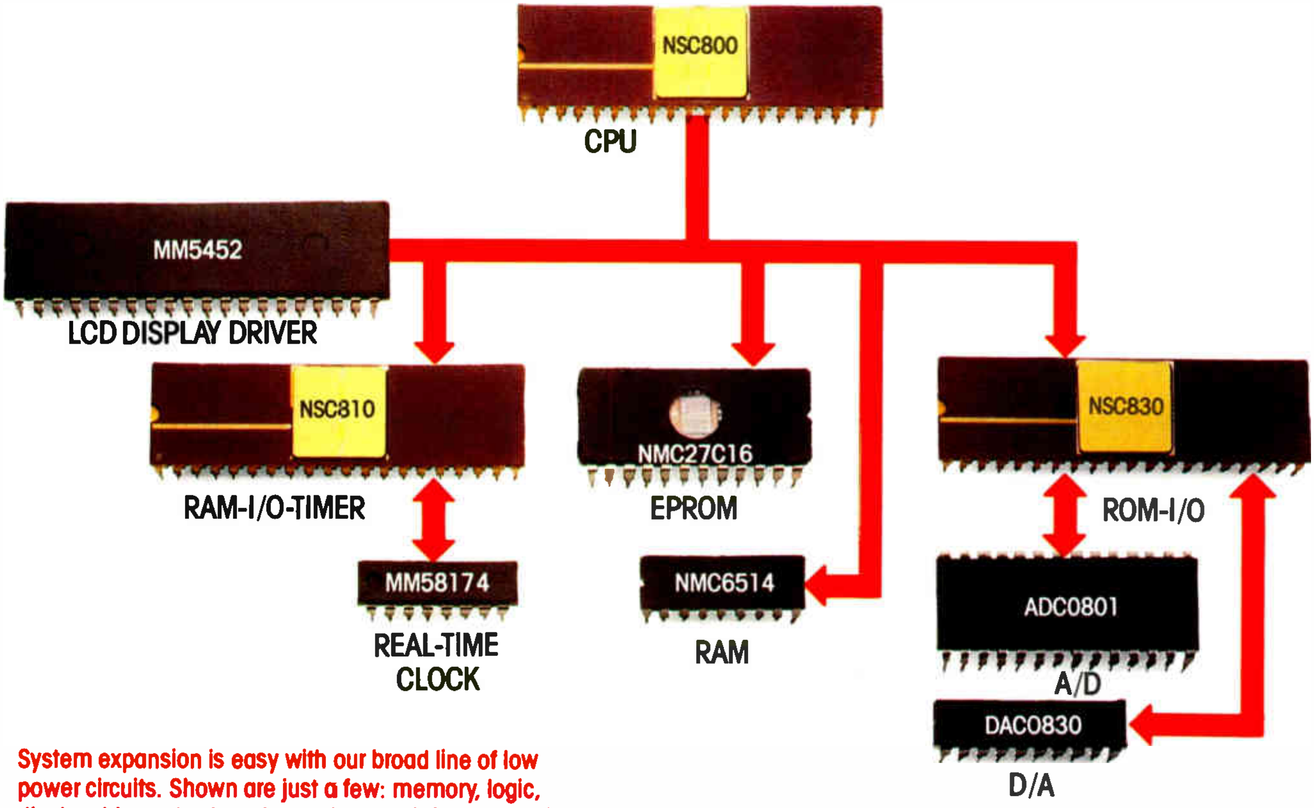


The heart of any system can be designed with just these three devices.

P²CMOS achieves this goal by using two layers of polysilicon in addition to the metal layer for interconnects. This silicon-gate, oxide isolated process yields decreased capacitance and increased circuit density. The final result—speed, a high degree of integration, and low power.

P²CMOS is an evolutionary extention of National's CMOS and XMOS™ processes. Products designed in P²CMOS are fabricated on a fully automated, high-volume production line.

Low power pays off. Now you can get the pay-off without sacrificing performance. For example, systems designed with low power circuits can be physically smaller. Power supplies, fans and cooling systems can be reduced or eliminated. PC boards can be designed for more dense configurations; and, if necessary, the whole system can be sealed for protection from harsh environments. And, of course,



System expansion is easy with our broad line of low power circuits. Shown are just a few: memory, logic, display drivers, keyboard encoders, real-time clock circuits plus fully microprocessor compatible A/D and D/A converters. The ADC0801, for example, features accuracy as good as ±¼ LSB, and eliminates the need for external zero and full-scale adjustments. We offer 8-, 10- or 12-bit devices. Our D/A converters—also in CMOS—are available in 10- and 12-bit resolutions.

low power systems are more reliable.

Built in Reliability. The lower the power dissipation, the higher the reliability. For example, consider the θ_{JA} of the NSC800 in a ceramic package, which is approximately 40°C/watt. At 50mW power dissipation, the die temperature will only be 2°C above ambient. This allows the NSC800 to easily operate at 125°C. As an exercise left to the reader, calculate the corresponding die temperature of one of the mentioned NMOS devices.

Military Applications. Because of its performance and reliability, the NSC800 Family is destined to become **the** military microprocessor of the future. Watch for the NSC800D/883, which will be supplied to meet the 883B military requirements.

Complete development support with ISE available now. The NSC800 family is totally supported by National's Starplex development system line. Real time In-System Emulation (ISE), high level languages (including PL/M and PASCAL), and complete cross-assembler support eases the development of the NCS800.

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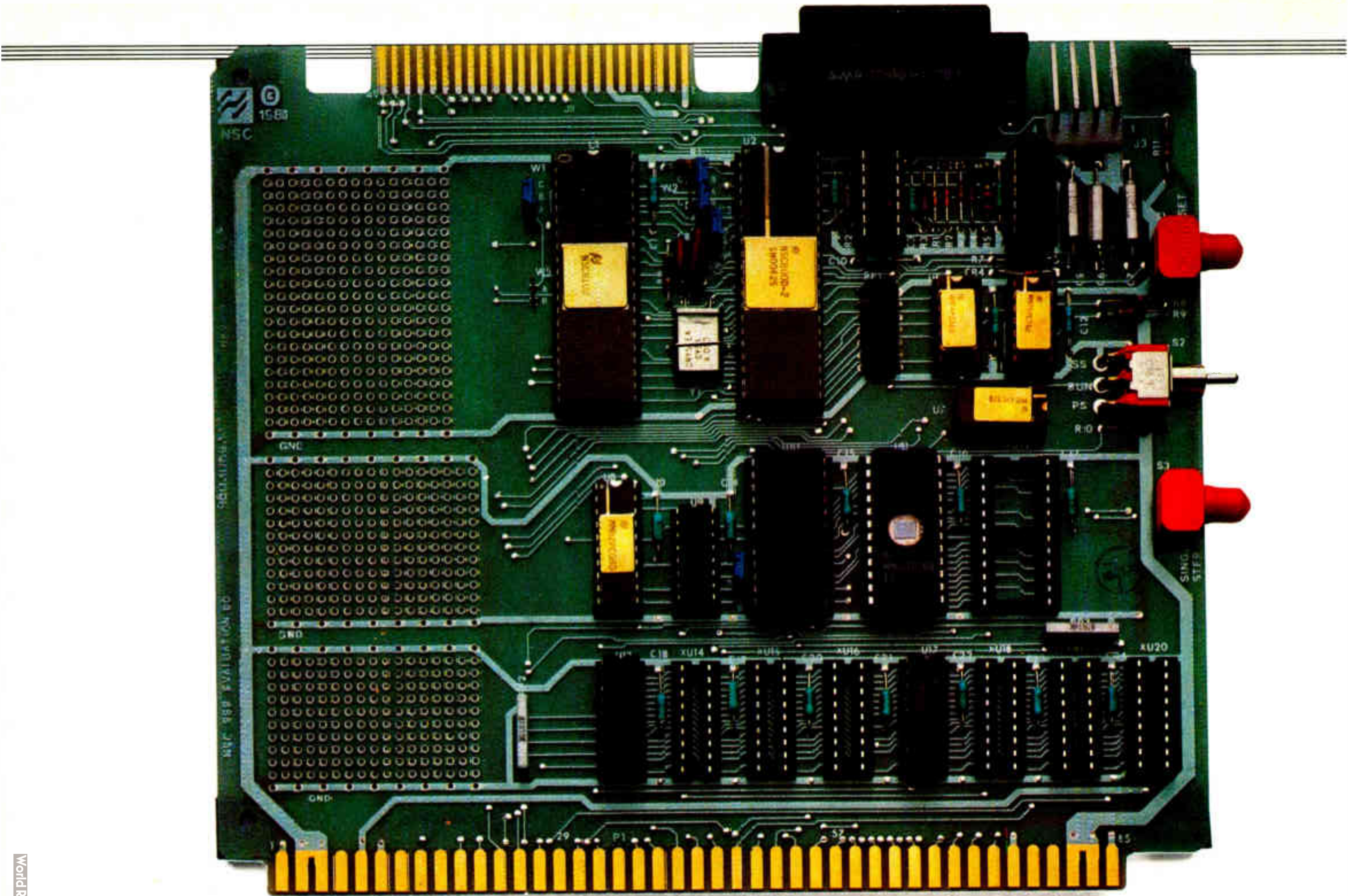


ufacturing, government, and business end-users that Sperry Univac serves and a downplaying of the past emphasis on board-level products.

The product line is now 50% different than it was just a year ago, notes Jan Krugers, director of minicomputer program management. "For the first time, we're getting away from the Varian image of selling to scientists," he says, although his organization will continue to sell to its traditional original-equipment and end-user markets.

Despite the management and product changes, some outsiders remain skeptical of Sperry Univac's chances of making a good showing. "They're relatively inexperienced in relation to DEC and Data General. They face an uphill battle," says Ulric Weil, vice president of Morgan Stanley & Co.

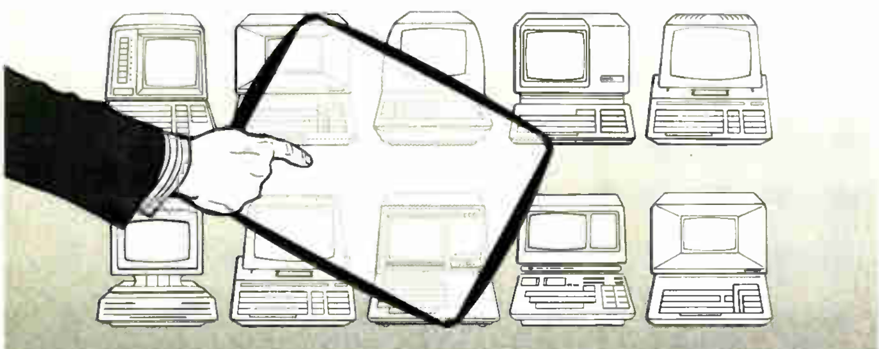
Gorchow counters that IBM and Honeywell also struggled with their first minicomputer attempts and are now doing well. Although its four-year learning curve is long in the minicomputer industry, Sperry has both the products and the financial strength to garner a good share of the market, even if that means supporting the operation for some time, he argues. -Terry Costlow

Solid state

VHSIC studied for antisub planes

The Navy is exploring its first application of very high-speed integrated circuits in airborne antisubmarine warfare, and Lockheed California Co. at Burbank is the beneficiary. Lockheed, prime contractor for the land-based P-3C Orion and the carrier-based S-3A Viking—the service's two leading antisubmarine warfare planes—expects to wrap up an investigation of such circuits' potential benefits to the aircraft by year's end.

At the same time, Lockheed's Glenn T. Webb says that the company is looking ahead at Navy development of an all-new maritime patrol

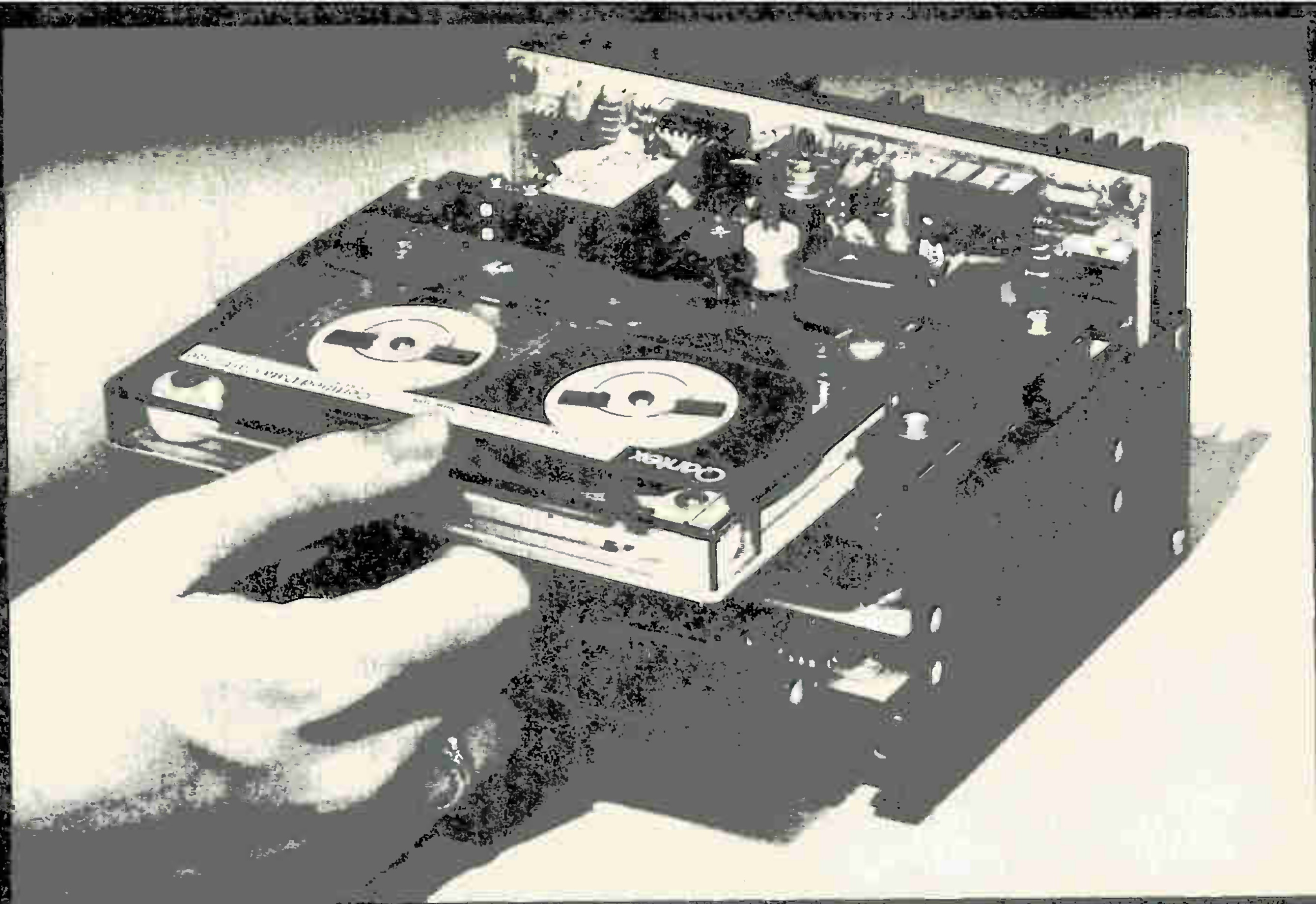


aircraft employing the very high-speed IC technology. Webb disclosed the $550,000 two-year program during a June review of the triservice VHSIC program at the Institute for Defense Analyses near the Pentagon.

The Lockheed study is being funded by the Naval Air Development Center, Warminster, Pa., as part of the VHSIC Phase III supporting-technology programs. The six-year effort, budgeted at $320.5 million, is being directed by the under secretary of defense for research and engineering [*Electronics*, May 19, p. 40].

Applications. Aircraft subsystems where the program may be applied include acoustics, communications, navigation, sensor, data processing, radar, and electronic support measures and countermeasures, as well as the man-machine interface between the antisubmarine warfare hardware and the crew. Webb also said the study—working from the top down by first defining the antisubmarine-warfare system's needs and then working down through to subsystems—is examining the impact of very high-speed ICs on system economics and effectiveness. The Navy expects to use the findings as a guide for VHSIC program contractors in selecting chip and card sets for patrol plane systems.

Assuming that the effort succeeds in developing subsystem brassboards and that their tests begin around 1984, Lockheed envisions applications in maritime patrol aircraft, provided that the Navy approves the program and Congress agrees to fund it. Lockheed is also proposing to use the technology in a new version of the S-3 carrier-based plane. But Webb sees that prospect as unlikely as the company has been working since 1980 on an avionics upgrade for 160 airplanes that will be designated the S-3B. When the first of those aircraft are deployed in 1987 with avionics already designed, they will carry new subsystems for processing acoustical, and radar data, electronic support measures, and a sonobuoy receiver, as well as the McDonnell Douglas antiship missile, Harpoon. **-Ray Connolly**



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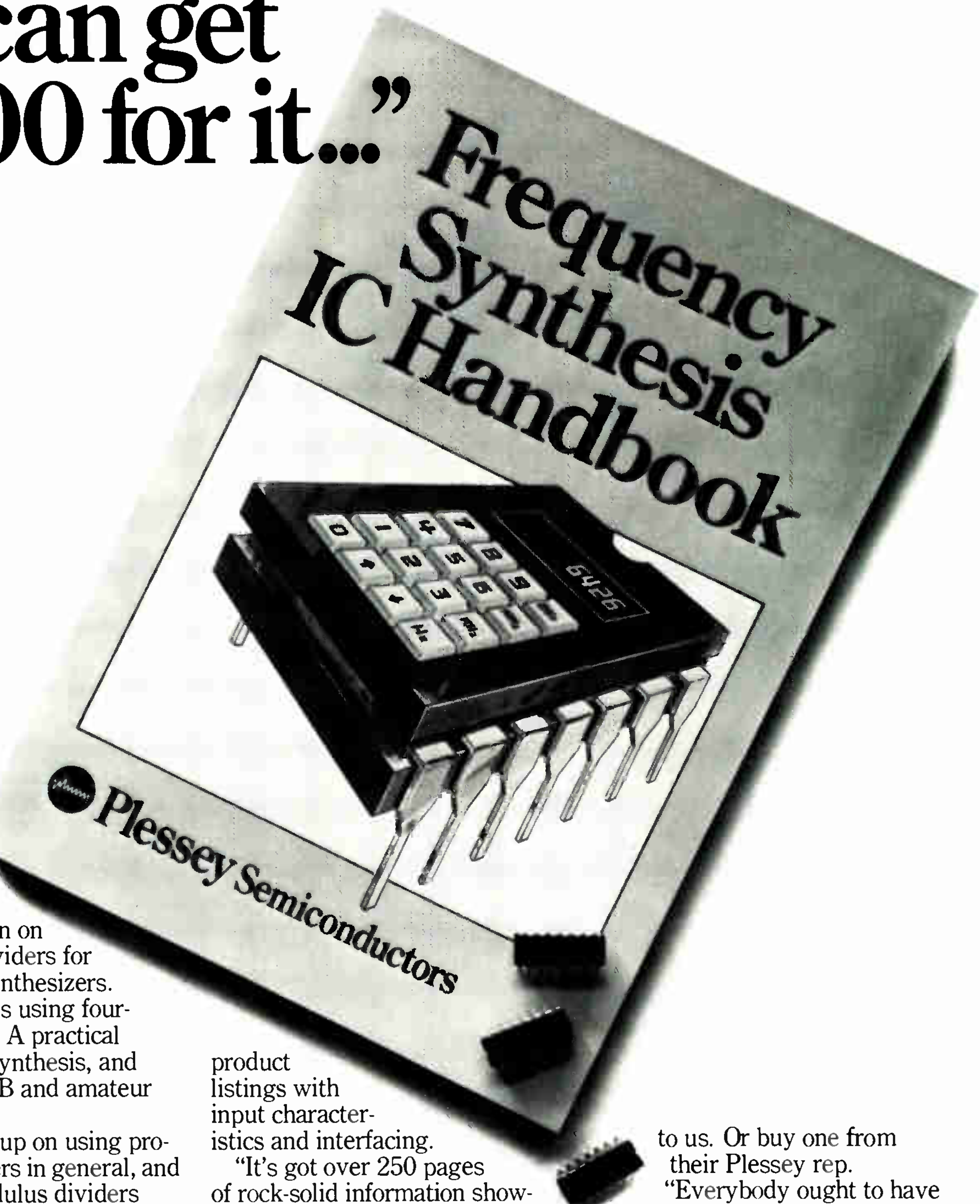

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Plessey: nice little chips.

Washington newsletter

U. S. R&D to total $79 billion in 1982 . . .

Fueled by military spending, U. S. research and development outlays in 1982 are expected to total $79 billion, a real growth of 6% from 1981 if inflation drops to the 8% level projected by the Office of Management and Budget. **The most growth will come in development programs,** which will rise 16% to $52 billion, largely as a result of defense spending, says a forecast by the National Science Foundation. Research outlays will rise 12% to $27 billion, however, maintaining the 1:2 ratio between R&D spending that had prevailed since 1975. The breakdown of 1982 funds, says the NSF, will be industry, $38.6 billion; the Federal government, $37.6 billion; universities and colleges, $1.55 billion; and other nonprofit institutions, $1.25 billion.

. . . with military outlays to climb 20%

Overall Federal R&D expenditures next year will reflect a real growth rate in defense spending of some 20% from 1981, reversing a trend to cut back on defense and space funding that began in the mid-1970s, says the NSF. **The climb in military outlays will be somewhat offset by a 4% spending drop** for the combined R&D budget of all other Federal agencies.

Lithography leads list in VHSIC awards . . .

Studies of lithography for making microcircuits are getting top-dollar priority in the 59 Phase III support contracts for the military's Very High-Speed Integrated Circuits (VHSIC) program. Of Phase III's 118 listed projects, covering nine areas of technology and budgeted for $32.3 million from fiscal 1980 through 1984, **lithography will account for 18 projects and a total of $11.9 million.** These undertakings encompass everything from electron-beam and X-ray techniques to intense plasma X-ray sources for submicrometer lithography.

. . . with reliability next in nine technology areas

Other Phase III VHSIC technology programs, ranked in order of dollars budgeted over the five fiscal years, include: **$7.46 million for 14 studies covering reliability, testing, characterization, and standardization;** $4 million for 18 architecture contracts examining both devices and weapons systems; $3.85 million to pay for 21 design-automation projects; $2.6 million for 13 contracts covering "other processing techniques" ranging from laser annealing to low-temperature silicon epitaxy; and $1.33 million for 10 studies in materials research and characterization. Areas budgeted for less than $1 million are: device technology ($765,000 for 16 studies), macrocell and chip fabrication ($590,000, three examinations), and hybrid packaging techniques ($415,000, five programs).

Pentagon to review electronics R&D

The Pentagon will get new evaluations in August of its accelerated research and development programs in electronics during three separate classified sessions of its Advisory Group on Electron Devices. AGED, **comprising specialists from academia, industry, and Federal laboratories,** has set an Aug. 13–14 session of its low-power devices working group to review R&D in integrated circuits, charge-coupled devices, and semiconductor memories. The microwave working group's Aug. 14 session will examine tubes and solid-state generators and receivers, millimeter-wavelength technology, and passive and active electronic-warfare systems. The Aug. 27 session of AGED's imaging and display working group will examine infrared and night sensor programs.

A bad bill for small-business R&D

The Small Business Research Act of 1981 is filled with good intentions and reads well. Nevertheless, S. 881 is a piece of legislation that seems destined to die, for it is poorly drafted, and the affected Federal agencies that would be obliged to use it to spur small-business innovative research and development in high technologies like electronics say they support the concept but not much more.

S. 881—brainchild of Senate Small Business Committee chairman Lowell P. Weicker Jr. (R., Conn.) and his subcommittee chairman for innovation and technology, Warren Rudman (R., N. H.)—comes close to being a carbon copy of the National Science Foundation's program for Small Business Innovative Research (SBIR). The bill's laudable goal would require all Federal agencies, working under the direction of the Small Business Administration, to set aside a small percentage of their R&D budgets for SBIR efforts. The first phase of SBIR support would award funds to determine a project's technical feasibility, and the second would fund R&D concepts found to be feasible up to the prototype stage. Finally, the third phase would provide funds to find private money to support commercialization or to produce the product for Government use.

Good motives gone wrong

What's wrong with that? At a time when an increasingly larger percentage of Government and industry R&D money is being diverted to military programs and inflation continues to limit the availability of capital for new high-technology industrial ventures, support for S. 881 should be overwhelming. But it is not. That was evident during the sparsely attended hearings conducted this month by Sen. Rudman in one of the Senate's smallest hearing rooms.

Opposed to segments of the bill—notably the mandatory set-aside of agency R&D budgets—are the Department of Defense; the National Aeronautics and Space Administration; the Department of Health and Human Services; the General Accounting Office, which functions as Congress's own auditor; and, yes, even the Small Business Administration. At best, all these agencies would like to see SBIR programs undertaken on an experimental pilot project basis, with each agency given greater flexibility to target R&D areas suited to its own needs. Opponents from academia also criticize the small-business funding set-asides, the role of the SBA as coordinator of the program, and the threat that small business might drain away even more Federal R&D money from the already diminished allocations for the nation's colleges and universities.

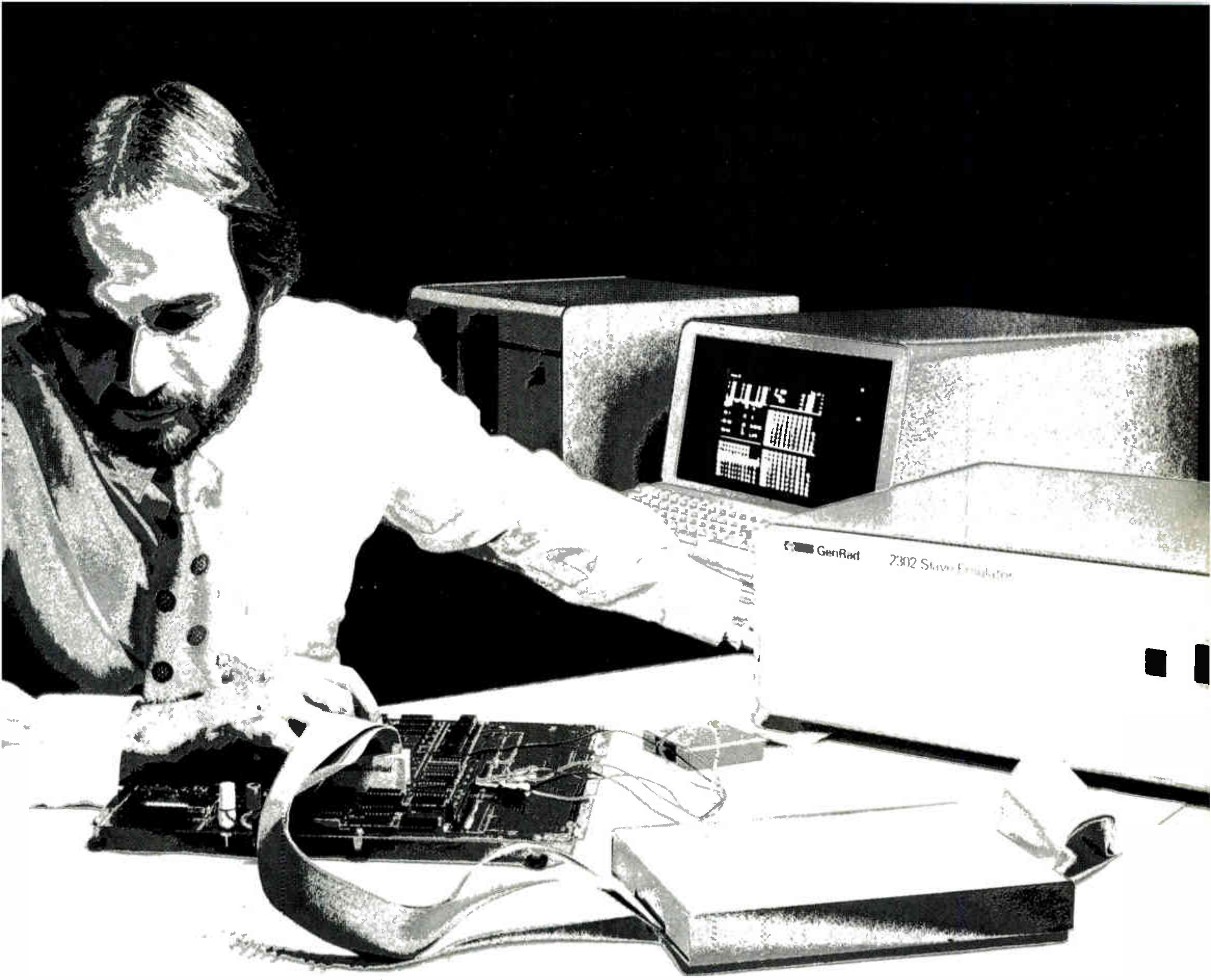
One of the more cogent points made during the hearings came from John A. DiBaggio, president of the University of Connecticut, testifying on behalf of three academic groups. To guarantee that a "sector or subsector will receive a certain share of funds is hardly likely to lead to quality research," he argues. Considering that congressional tax committees are now weighing proposals "that would give big business tax credits if they expand investment in R&D," DiBaggio adds, "proposals that would result in contracting out to small business may well belong in this legislation."

Challenging the SBA's capabilities

The Federation of American Scientists, which favors much of S. 881, believes that the SBA "lacks sufficient experience in dealing with complicated issues of science policy to function as the sole lead agency for implementing this legislation," according to its spokesman, Philip Speser. NASA's deputy director for procurement, Leroy E. Hopkins, makes the point more strongly: not only would the bill "overlay the Federal procurement process with another statute at a point when the focus of Federal procurement efforts—by [prior] congressional mandate—is to simplify the already overburdened process," Hopkins says, but "the bill would also give a significant procurement regulatory role to a nonprocurement, non–research-and-development agency, which by virtue of its mission, heritage, staffing and capability, is not in a position to deal with the complexities of advanced technology."

Like NASA, the Pentagon believes that what has been good for the National Science Foundation, which funds small-dollar R&D programs, will not necessarily be good for the DOD, where much funding goes to large-dollar contracts for major weapons systems. Moreover, Robert F. Trimble, deputy under secretary for research and engineering in charge of acquisition policy, makes the additional point that the DOD last year adopted its own variation on the NSF program to support small-business research.

Thus it seems that S. 881, however well-intended, may, at worst, die a quiet death. At best, the hearings demonstrated that it needs to be substantially reworked if it is to get the support it will need for passage. **-Ray Connolly**



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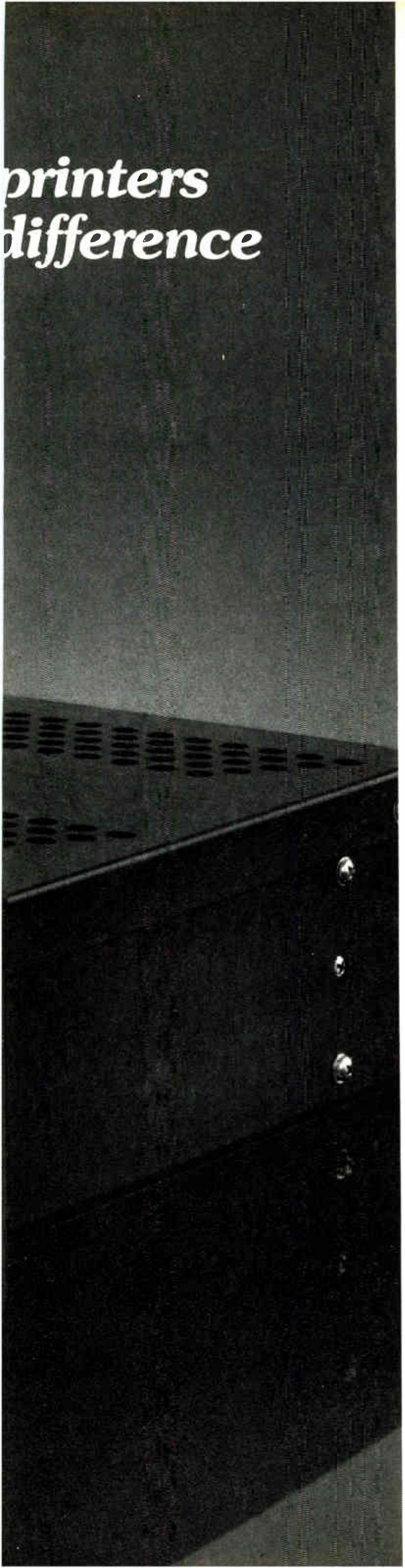

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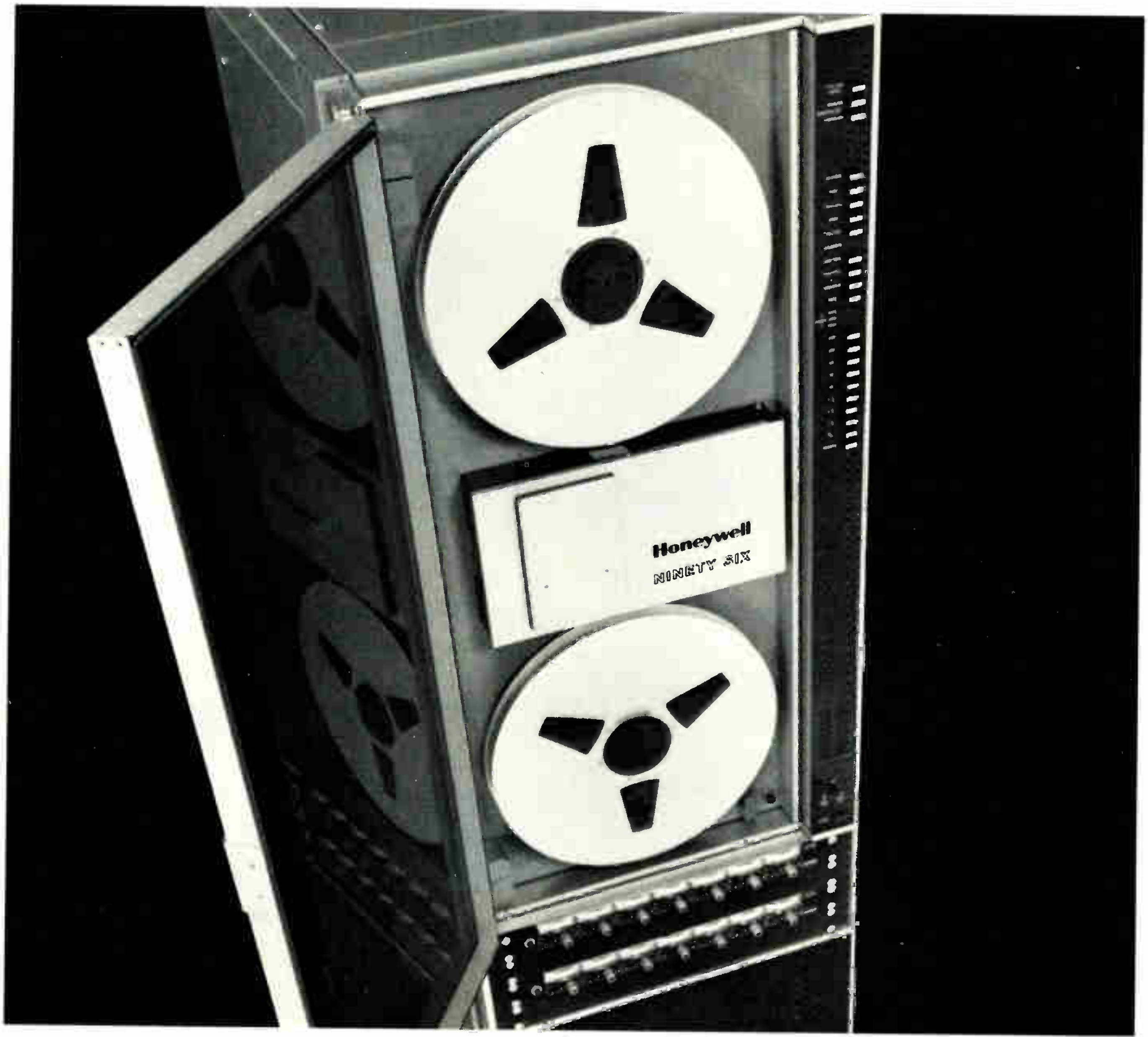

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International newsletter

British Telecom orders first single-mode fiber-optic link

British Telecom is moving its leading-edge single-mode fiber technology from the laboratory into the field with a first order to Standard Telephone & Cables Ltd. for **a 27-km link between Luton and Milton Keynes, to be operational by 1984.** In the laboratory British Telecom has demonstrated repeaterless transmission at 140 Mb/s employing a 1-μm wavelength over 49 km, but the link will transmit over 37-km spans using 1.3 μm laser diodes that have been in use longer. This order is one of a second round of orders worth $28 million that will add 803 km to the 450 km of fiber-optic cable now being laid or operational. Already, says British Telecom, fiber-optic cable is cheaper than conventional systems on trunk routes, with a cost of $10/km compared with $12.58/km. The orders will be split between Plessey, General Electric, and STC.

Japanese hand-held computer sells for $170

Casio Computer Co. started selling its $170 hand-held computer in mid-July, with sales in the U. S. due later this year. This makes it the second manufacturer after Sharp Corp. to offer a calculator-sized computer **capable of debugging and running programs written in Basic.** Said to have 10 times the speed of the competition, the FX-702P uses complementary-MOS memory with battery backup to provide 1,680 program steps and 26 data memory registers that can store 10 programs. All normally required mathematical and statistical functions are built in, and output is on a 20-character liquid-crystal display. In August Casio will start sales of the FA-2 adapter for program and data storage, on ordinary cassette tape recorders, for some $35. In October it expects to start sales of the FP-10 miniprinter for hard copy output for about $70.

Hungary to try viewdata services

Hungary, a trend setter in East European telecommunications activities, is getting ready to start trials of viewdata, thus becoming the first member of the Comecon bloc to begin the new television-based service. **The trials, to start this fall, will be with both France's Antiope and Britain's Prestel systems** and provide TV viewers by phone with 100 to 120 pages of information. After a year or so, communications officials will settle on either one of the two systems. Much is at stake because **Hungary's choice will become the standard for the entire 10-nation Comecon bloc,** according to sources in Vienna. The country will also start trials this year of West Germany's automobile drivers' radio information system called Ari.

Japan to enhance naval defense

The Japan Defense Agency will **try to move up purchases of P-3C antisubmarine patrol planes and F-15 fighters** to meet U. S. demands that the nation build up its naval patrol and air defense capabilities, but it expects strong resistance from the Ministry of Finance.

In its budget for fiscal 1982 (starting April 1) the agency will ask for funds to buy 43 F-15s, including 32 it originally planned to buy next year and the 11 it planned to buy in 1984. Together with planes ordered earlier, this would complete Japan's planned purchase of 100 F-15s. The agency will also ask for funds to buy 17 P-3Cs, including 12 it originally intended to purchase next year. That will leave another 10 to be ordered in 1984 to bring total purchase of P-3Cs to 45.

International newsletter

Process-control unit runs 48 Intel 8086s as one

A smooth progression of computer power with 1 to 48 Intel 8086s working in harness as one machine is the concept behind Scidac, a ground-breaking process-control and -monitoring system developed by Scicon Consultancy International, a British Petroleum Ltd. subsidiary, and scheduled for delivery in early 1982. Developed in collaboration with the National Physical Laboratory, Scidac initially ran sixteen 8086s [*Electronics*, Nov. 8, 1979, p. 63], but by exploiting Intel's now standard multiprocessor capability, which allows three Intel 8086s to share a common bus, Scicon can now run 48 microcomputers in parallel as one machine. Meanwhile, the state laboratory has **a more advanced bus in development that will run 250 microprocessors** as one machine.

Siemens to assemble power semiconductors in Japan . . .

Testifying to their growing popularity, Sipmos power components [*Electronics*, March 10, 1981, p. 12] are to be assembled at Fuji Electronic Components Ltd., a Tokyo-based firm owned jointly by Japan's Fuji Electric Co. and Sipmos maker Siemens AG of Munich, West Germany. Siemens's goal "is to be close to a power MOS device market that we think will eventually grow as fast as the one in the U. S.," a company executive says. He sees **worldwide sales of all types of power MOS components increasing to a staggering $250 million in 1985** from $10 million this year.

. . . while Fujitsu will market a U. S. CAD/CAM system there

Japan's Fujitsu Ltd. says it has obtained the rights to sell worldwide Lockheed Aircraft Corp.'s computer-aided design and manufacturing system, Cadam, which is applicable in industries ranging from aircraft, automobile, and shipbuilding to construction. The company says it **will concentrate on the Japanese market,** where until now IBM Corp. has had the exclusive license to sell the system.

Monolithic amplifier with 1-GHz bandwidth challenges hybrids

Manufacturers of high-performance and equally high-priced hybrid broadband amplifiers could soon be feeling the draught from cheap monolithic alternatives. Swindon-based Plessey Semiconductors Ltd., for one, is supplying samples of a broadband device **with a flat response over 100 MHz to 1 GHz,** with volume production scheduled for the fourth quarter. Instead of resorting to gallium arsenide technology, Plessey uses a high-performance ion-implanted bipolar process that produces transistors with a cutoff frequency of 6 GHz. With a 20-dB differential gain, the new SL565 should find applications in instrumentation and test equipment.

Addenda

Look for Thomson-CSF of Paris to introduce a new line of gallium arsenide abrupt tuning diodes at the European Microwave Conference and Exhibition in Amsterdam in September. Intended for use in microwave links, all 15 of the devices will be used **for modulating and tuning wideband (500-MHz) oscillators.** . . . Siemens AG is to develop an advanced direct-memory-access device and a cathode-ray-tube dot-rate generator **for the iAPX 16-bit microprocessor** to be introduced this fall by Intel Corp., with which the West German company has a highly successful five-year-old technology agreement . . . Burroughs Co., the Japanese subsidiary of Burroughs Corp., plans to build **a plant for assembling kanji data terminals,** with operation due to start in January.

16 TO 96

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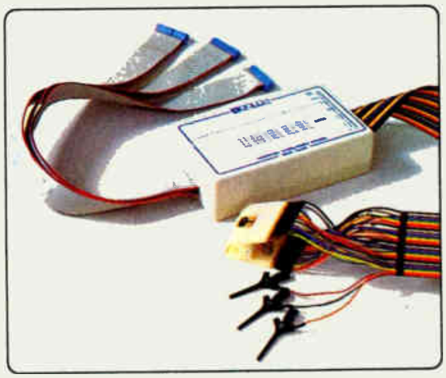

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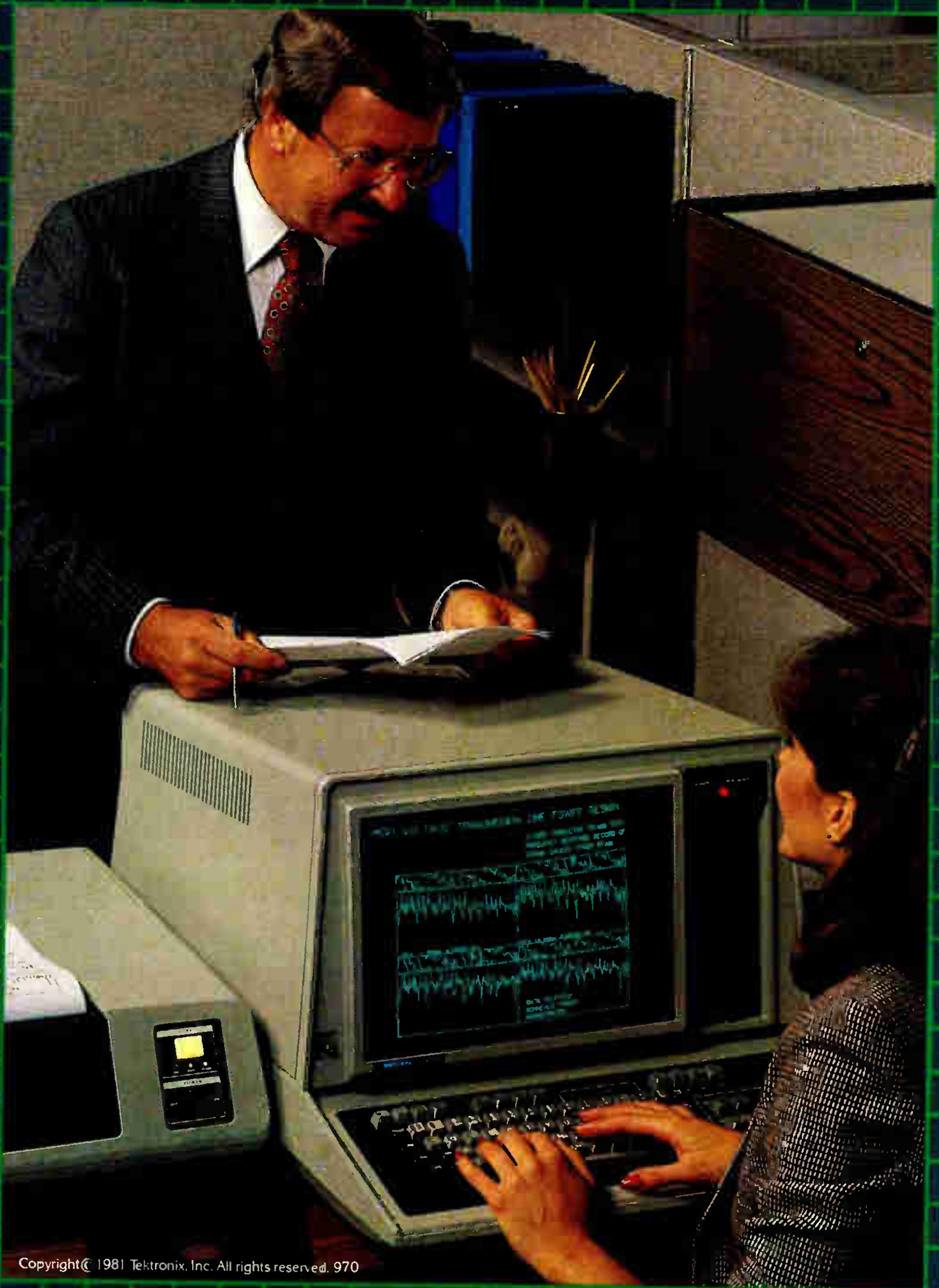
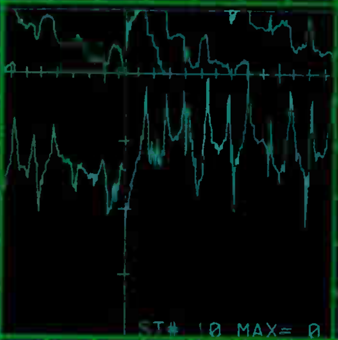
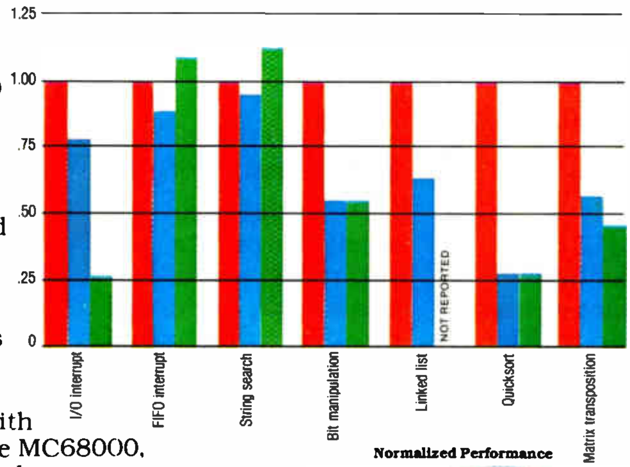


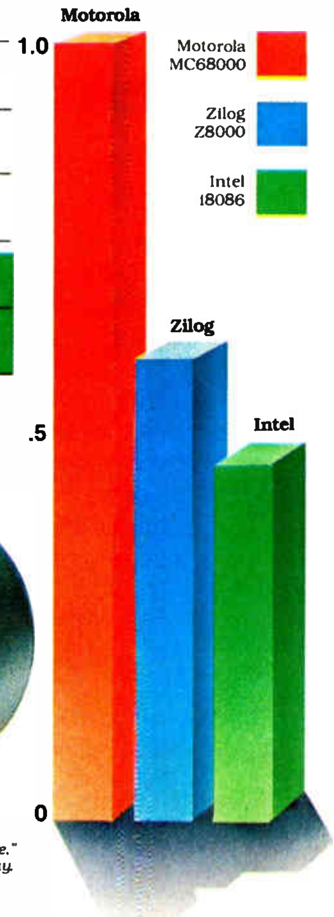
You can define from one to sixteen viewports on the 4112's 15-inch raster display. You can use local zoom and pan capability to select and magnify any portion of the 4096 x 4096 addressable points screen. Return to the full picture, and the terminal will automatically bracket the detail section last displayed.



Technological leadership.

Independent benchmarks MC68000 is first choice





Motorola's advanced MC68000 microprocessor is demonstrably superior for a broad range of 16-bit applications. The evidence is in, and it's conclusive.

The MC68000 consistently and significantly outperformed both the Z8000 and the i8086 in three current independent benchmark studies. Evaluations by engineers not associated with any microprocessor supplier demonstrate that the microprocessor system with the best overall performance is the MC68000, making it the clear choice for new designs.

And it's clear that the MC68000 is now recognized as the competitive edge for end-use systems. Design engineers recently confirmed that it is the first choice among 16-bit microprocessors in two independent product preference polls.*

Benchmarks measure MC68000 performance advantages.

Results of a performance comparison for a digital filter application by V.P. Nelson and H. T. Nagle, published in *IEEE Micro*, find the MC68000 nearly twice as fast as the Z8000 and almost three times as fast as the i8086.

A variety of benchmarks from the Carnegie-Mellon series as reported in *EDN* magazine by Grappel and Hemenway show that the MC68000 is significantly faster than each of these devices in handling routines for Bit Test/Set/Reset, Linked Lists,† Quicksort, and Boolean Matrix. In the same study, it also compares favorably for I/O interrupts. Overall, it outperforms the i8086 by 2.16 to 1.0 and the Z8000 by 1.71 to 1.0, even with the MC68000 addressing its full 16-Megabyte address space and the other two MPUs addressing only 64K.

Benchmarks from the Blacksburg Group, being published by Howard W. Sams and Co., indicate that the MC68000 is two times to three times as fast in four‡ out of five routines compared, including Sorts, Square Root, and Sine Look-up.

Still other benchmarks give the edge to the MC68000 for execution of multiprecision binary and BCD arithmetic operations, 32-bit array scans and string translations. Floating Point arithmetic operations can be carried out almost as fast as hardware implementations.

Results reported in "A Tale of Four MPUs: Benchmarks Quantify Performance," Robert D. Grappel and Jack E. Hemenway, April 1, 1981 EDN Magazine, a Cahners Publication

Memory address, 32-bit features enhance performance.

The performance advantages of the MC68000 demonstrated in the studies are impressive. And the MC68000 has still other capabilities of equal importance in helping keep you ahead of your competition.

The MC68000 has seventeen 32-bit multipurpose registers, with data and address registers separated for parallel operation. All registers can be used as index registers, and all address registers can be used as stack pointers.

No other 16-bit MPU can match the 16-Megabyte direct memory addressing, and programmers need not worry about segmentation and the overhead associated with it.

The simple, efficient instruction set includes 56 powerful types designed to minimize the number of mnemonics a programmer must know. Software development costs are minimized because addressing modes are usable with all applicable instructions.

One other thing. The MC68000 provides, in one high-quality device, what is often found in multi-

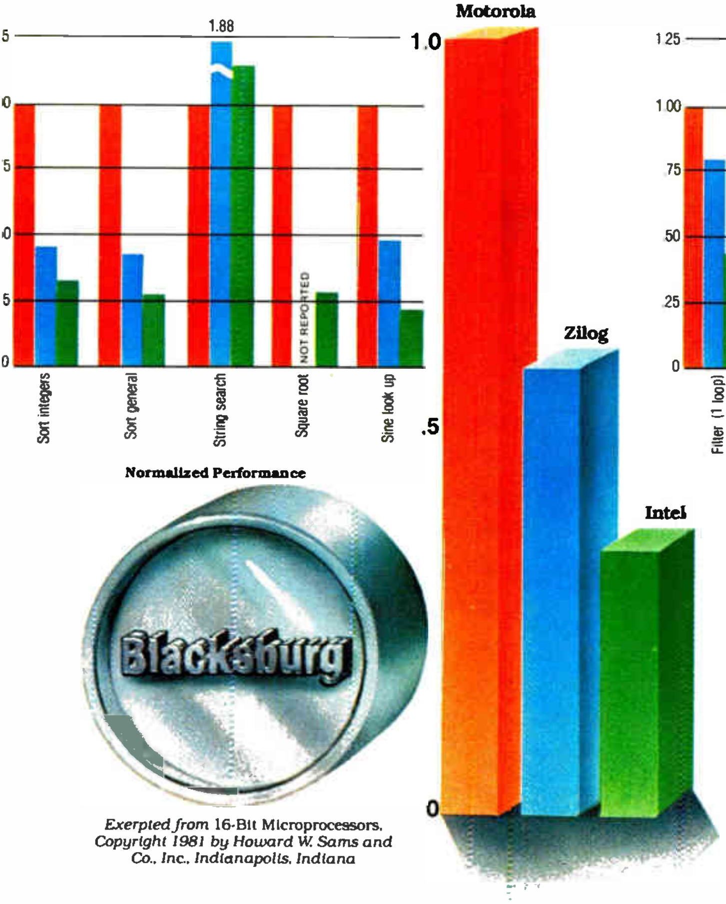
Annual Minicomputer Survey, November 1980, with permission of DATAMATION MAGAZINE, G.S. Grumman/Cowen & Co.

Electronics 1980 Product Preference Poll, with permission of ELECTRONICS MAGAZINE, McGraw-Hill, Inc.

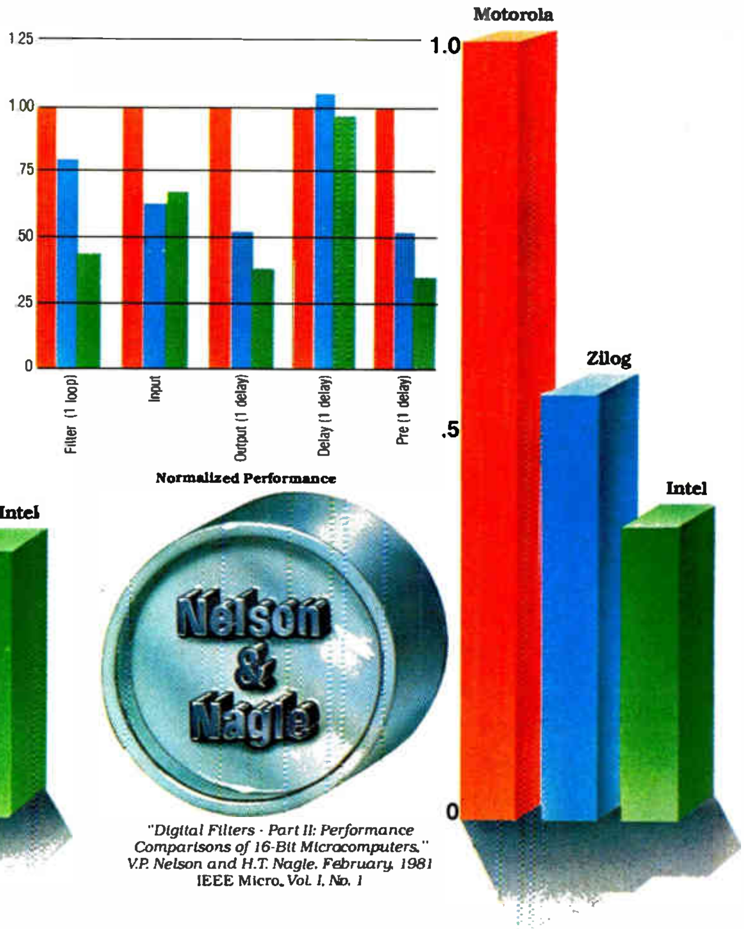
†Not reported for i8086, but Motorola data indicates the MC68000 is more than 20% faster.

‡No report for Z8000 on Linked List.

demonstrate why the
for 16-bit MPU applications.



Exerpted from 16-Bit Microprocessors, Copyright 1981 by Howard W. Sams and Co., Inc., Indianapolis, Indiana



"Digital Filters - Part II: Performance Comparisons of 16-Bit Microcomputers," V.P. Nelson and H.T. Nagle, February, 1981 IEEE Micro, Vol. I, No. 1

chip arrangements requiring more interconnects, bus coordination, space and cost.

Keep your systems state-of-the-art.

In addition to the MC68000 microprocessor, Motorola's well-rounded family of existing and future VLSI peripherals is designed so that you can keep your M68000-based systems state-of-the-art for years. And, the 8-bit M6800 Family peripherals interface directly with the MC68000, broadening support with an attractive low-cost, medium-performance option.

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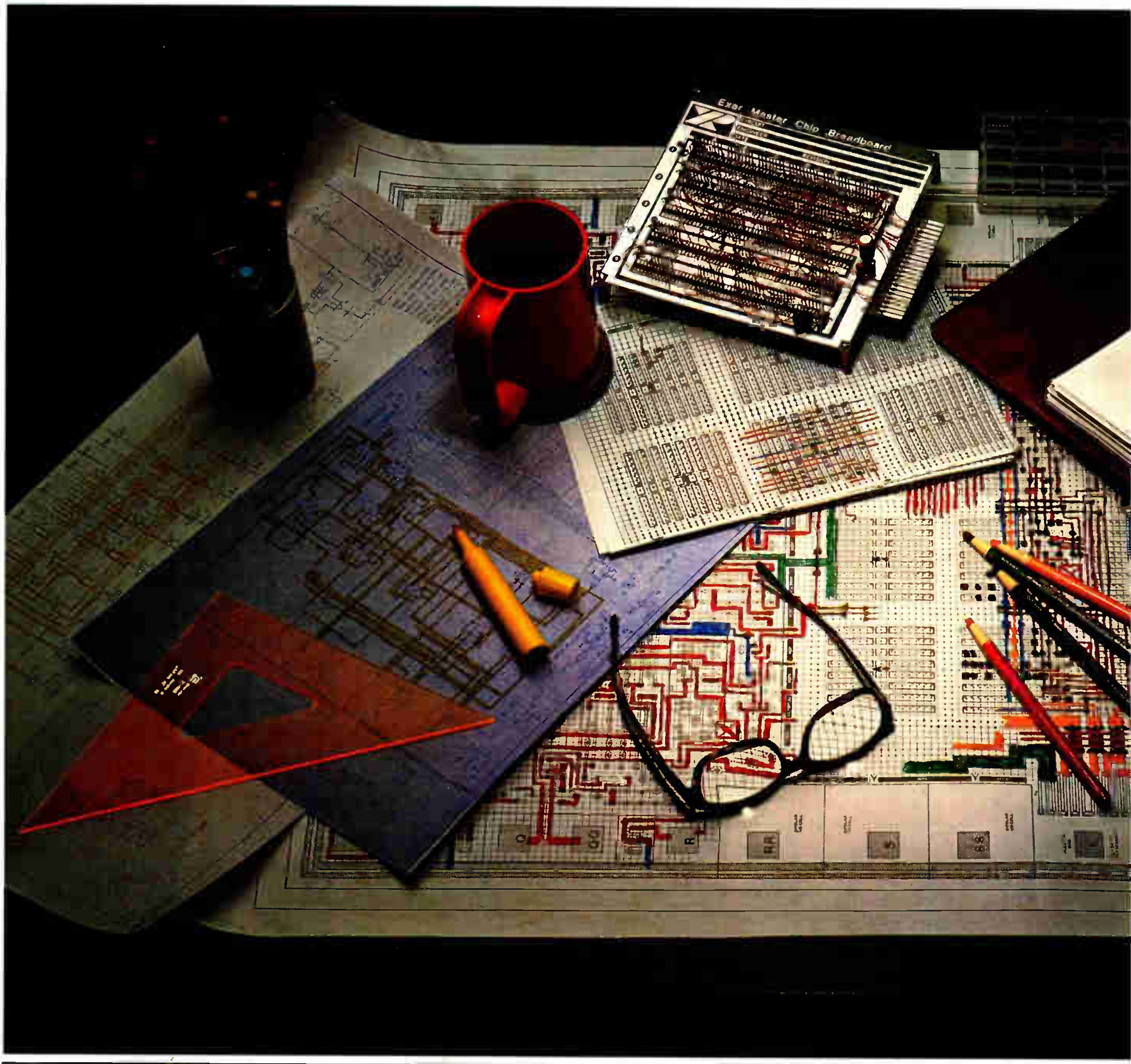

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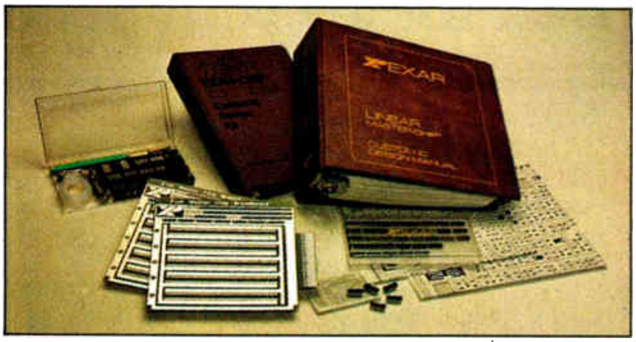

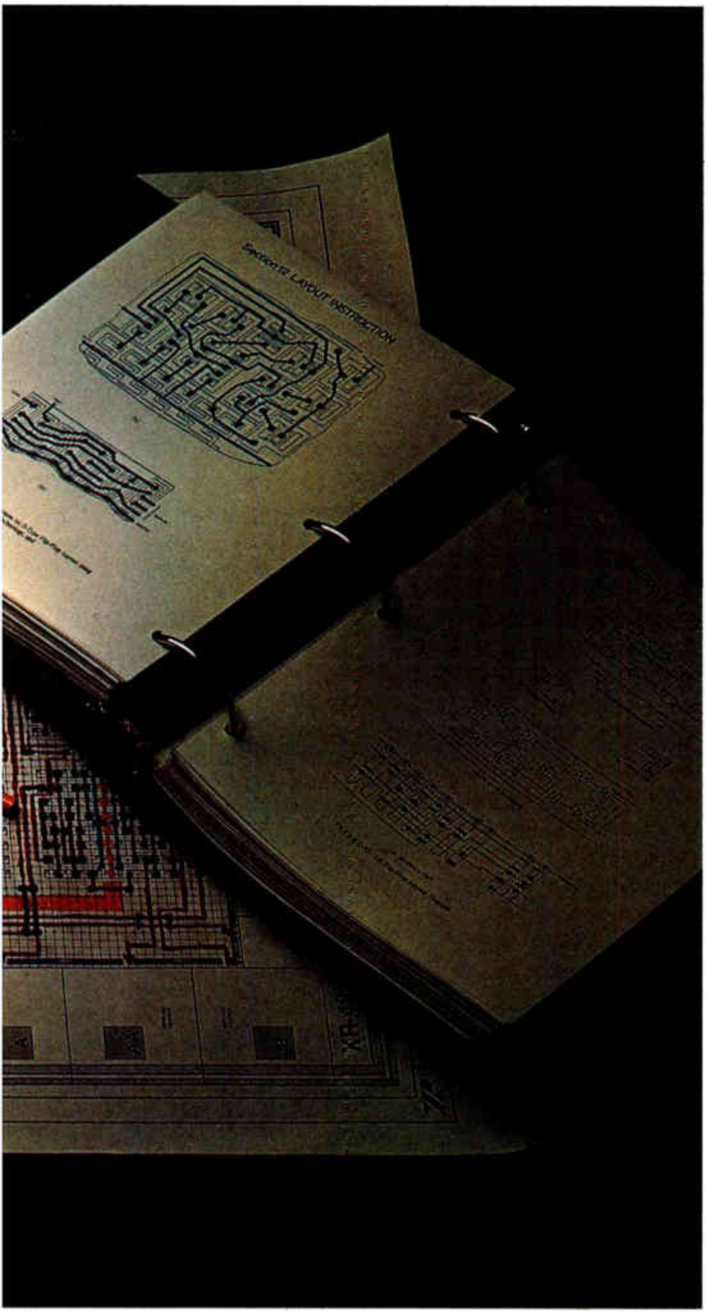

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Fiber transmits plane-polarized wave of light

by Charles Cohen, Tokyo bureau manager

Light propagates along axes of ellipse in round core under pressure from elliptical jacket

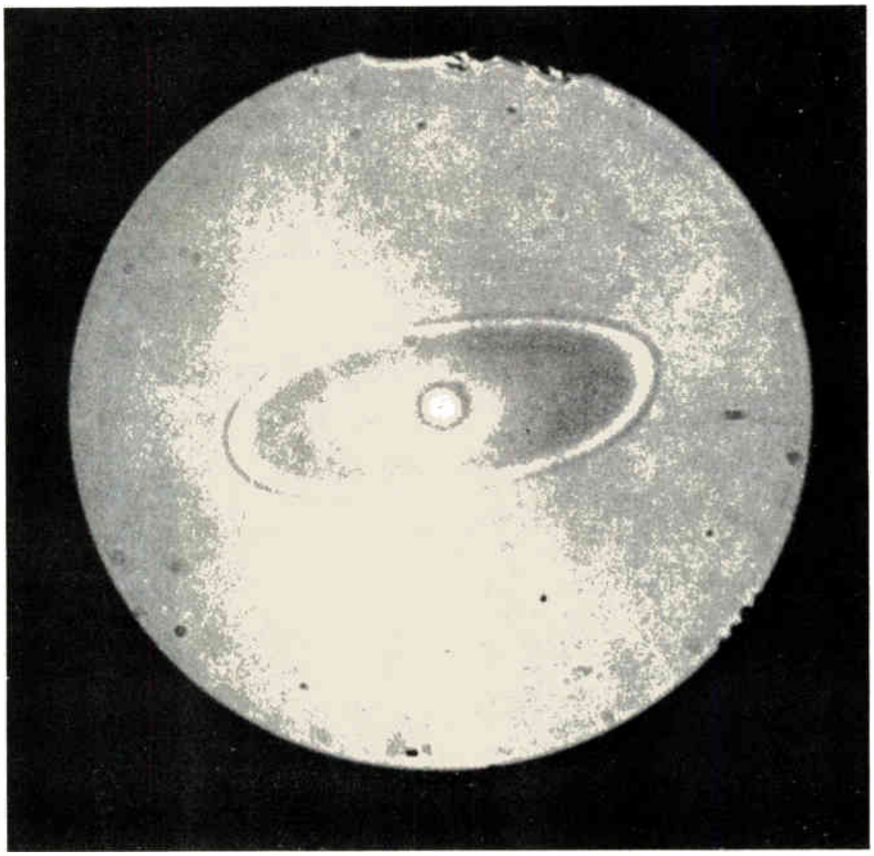
The planar (or single) polarization of light is preserved throughout the length of a new low-loss single-mode optical fiber from Japan. Though its transmission loss of 0.8 decibel per kilometer at a wavelength of 1.55 micrometers is like that of other high-quality optical fibers, Tsuneo Suganuma, senior researcher at Hitachi Ltd.'s Central Research Laboratory, says this fiber will be several times the price of standard low-loss cables and so may initially find more applications in measurement and test equipment.

The technology for the new fiber was developed at the laboratory and is now being transferred to the company's subsidiary, Hitachi Cable Ltd. Deliveries of samples are scheduled for this fall.

Resemblances. Basically the fiber is similar to other single-mode quartz types. It is fabricated by a commonly used modified chemical vapor deposition process, but with proprietary differences that the firm will not reveal. The 8-μm-diameter core through which the light travels consists of silicon dioxide with a small amount of germanium dioxide added to raise the index of refraction. The surrounding 16-μm cladding is made of pure silicon dioxide, whose slightly lower index of refraction keeps the polarized light being transmitted from escaping at its interface with the core.

The big difference in the new fiber is the presence of an 80-by-26-μm elliptical jacket surrounding the cladding and itself surrounded by the support. Boric oxide in the jacket material increases its temperature coefficient of expansion far above that of the support. Thus as the fiber drawn from the four-part preform (core, cladding, jacket, and support) cools down from the 2,000°C temperature at which it is fabricated, differences in the thickness of the jacket material exert anisotropic forces on the core along the major and minor axes of the ellipse. The direction with the higher compression, along the short axis of the ellipse, has the higher index of refraction. An elliptically cross-sectioned fiber has been studied in the UK [*Electronics*, Aug. 30, 1979, p. 67].

Boron needed. The boric oxide in the jacket is balanced with enough germanium oxide to cancel out their optical effects and yield the same index of refraction as the cladding.



Ready for production. An 80-by-26-μm elliptical jacket surrounds an 8-μm-diameter core in optical fiber developed by Hitachi for transmitting single-polarized light.

The support, which is standard, also has the same index of refraction as the cladding and the jacket.

Because the index of refraction is highest along the shorter of the ellipse's perpendicular axes and lowest along the longer one, a single-polarized wave of light launched into the cable along either axis will be transmitted unchanged. Even after transmission over 1 km, the polarization, as measured by the extinction ratio, will be better than 30 decibels—that is, the conversion of energy from one plane into the orthogonal one is less than 0.1%. For a standard fiber under the best of conditions the ratio would probably not exceed 10 dB. And the slightest vibration of a standard fiber, which causes anisotropic mechanical pressure on the core, can reduce the ratio to about 3 dB.

Applications. Hitachi engineers say that one application of the new fiber would be continuous-wave optical communications similar to that pioneered in an experiment at the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. [*Electronics*, Nov. 20, 1980, p. 73]. They say that maintenance of single polarization is necessary to obtain heterodyning.

For the nearer term, this type of fiber could be important for connecting optical integrated circuits to other ICs, where mechanical switching arrangements would be replaced by electro-optical switches using the Faraday effect, which causes rotation of single-polarized light waves.

Other applications include blood-flow meters, which make use of the Doppler effect, and optical gyroscopes. The gyroscope, which exploits the Sagnac effect (the shift in phase of light inside a moving object), is said to have an accuracy that is four orders of magnitude better than that of mechanical gyros. When a coil consisting of 1 km of optical fiber is used and light launched into it from either end at the same moment, the difference in phase between them as they emerge can be measured with a theoretical precision of 10^{-8} radian/second.

West Germany

2-carrier stereo TV to start this fall

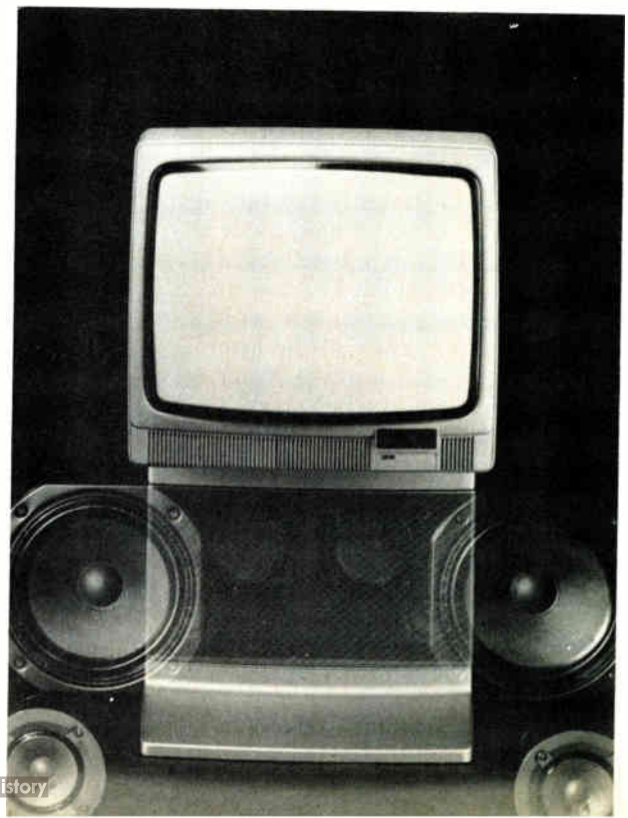
Two-channel stereo-sound television—that's the latest buzz word in West German TV circles. And with regular transmissions of the new service due to start on Sept. 4, the opening day of the Radio and Television Exhibition in West Berlin, broadcasters and set makers are gearing up for what the industry touts as the most significant TV event in West Germany since the 1967 debut of color broadcasting.

Stereo TV, as the new service is called, will add another dimension to the TV medium. Obviously, stereo enhances the quality of sound. But in addition, since the system transmits two widely separated sound channels simultaneously, it becomes possible to broadcast, say, a foreign movie in both its original language and a dubbed-in one.

The standards for the system were worked out by the Radio Operators' Committee of the Frankfurt-based Central Association of the Electrotechnical Industry together with the Institute for Radio Engineering in Munich and were made known early last year. Multilingual nations like Switzerland and Belgium are said to be particularly interested, as are Japanese TV authorities and set makers. The system is compatible with monaural TV.

The German stereo TV transmission system contrasts with fm stereo radio and Japan's stereo TV method. Those approaches transmit the two audio channels together with the pilot tone on one carrier. But though that works well in mountainous terrain for bilingual programs using the NTSC signal, it would work poorly with the PAL signal in, say, Switzerland, where reflections would cause too much crosstalk between the channels. The West German system therefore uses two carriers—the normal TV sound carrier, plus a new one, allowing for a high channel separation of 240 kilohertz.

The crosstalk attenuation checks in at better than 60 decibels and the bandwidth for each channel goes from 40 hertz to 15 kHz. The pilot carrier frequency is about 54.7 kHz. When their intermediate frequencies are taken into account, the additional sound carrier at 33.16 megahertz is 240 kHz away from the normal, 33.40-MHz sound carrier. In a typical stereo TV receiver, of the kind



First. Loewe Opta is Europe's first TV maker to produce stereo sound color TV sets. One of its three models is this 26-inch MCS11 floor model with two pairs of loudspeakers.

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Loewe Opta GmbH already builds, the i-f surface-wave filter that follows the tuner separates the two sound i-f frequencies from the video i-f and feeds them to the sound i-f amplifier. The signals are then applied to the stereo decoder, whence they pass to the audio-frequency power stages for the left and right loudspeaker systems.

Most observers feel stereo sound will boost West Germany's stagnant TV industry despite a stereo receiver's additional cost of around $170. Still, not everybody is happy over its introduction at this time. Some broadcasters feel that the necessary transmitter modifications will severely strain their budgets. And given the 600,000 to 800,000 unsold TV receivers on the industry's hands, some producers do not want to see consumers hold off on purchases in the hope of better things to come.

Nevertheless, officials at Kronach-based Loewe Opta, the first TV producer on the market with two-channel stereo sets [*Electronics*, March 24, p. 72], estimate that 40% of the color receivers sold next year will be stereo sets, rising probably to around 60% in 1983.

And indeed, when the 10-day Berlin show gets under way in September, almost all of West Germany's dozen or so set makers will have stereo receivers to offer. By then, too, the Second German TV Network will have already modified 27 of its 91 transmitters for stereo broadcasting, enough to reach roughly two thirds of the country's 22 million or so households.

The network's remaining transmitters are slated to be modified by the end of this decade, possibly sooner if stereo broadcasting gains acceptance. **-John Gosch**

Japan

X-ray aligner exposes 0.5-micrometer lines, processes five 75-mm wafers an hour

As device dimensions are scaled down to the submicrometer level, step-and-repeat lithography will have to substitute X rays for visible light to provide the necessary higher resolution. An experimental X-ray aligner has already been built by the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp., which believes that it is the first in the world that can replicate 0.5-micrometer patterns. Indeed, it can produce still finer lines, claims Satoshi Nakayama, chief of the physical and chemical processing section.

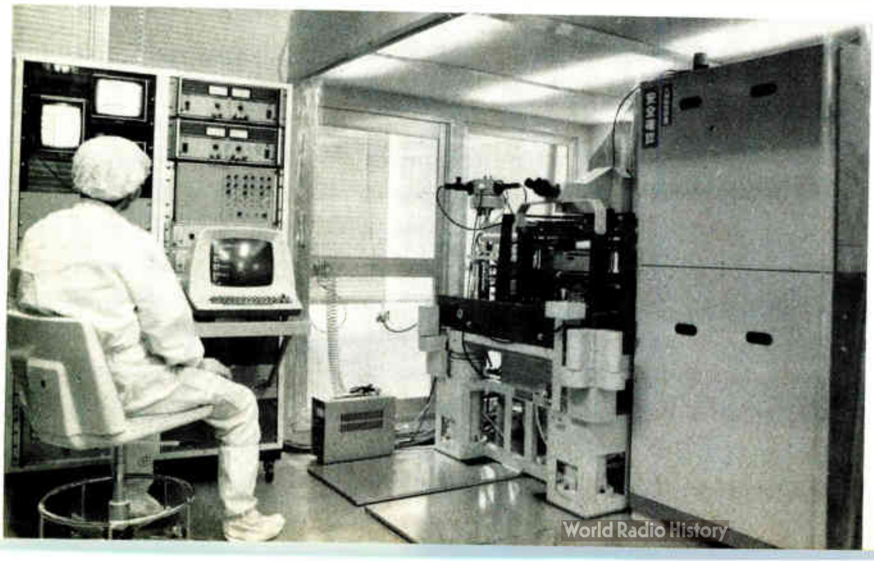
The X-ray approach to the mass production of submicrometer chip geometries has two advantages over the scanning electron beam, the only viable alternative. For one thing, the X-ray equipment costs only about a third as much, about the same as an optical stepper, because it exposes a chip at a time and so does not need pattern-generation memory and logic for "writing" circuit patterns. Furthermore, the lower energy of the X rays makes for higher resolution by eliminating backscattering from the substrate—the troublesome distortion of small dimensions that in electron-beam systems is caused by stray electrons and needs compensation.

There is no way, though, to stretch or shrink the X-ray pattern to compensate for wafer distortion, except by using step-and-repeat techniques to decrease the area over which the pattern is aligned. For the greatest precision, a single chip can be aligned, but the processing of batches of 4, 9 or 16 chips should be more typical. In the case of NTT's SR-1 step-and-repeat X-ray exposure system, the maximum effective size of the mask is a circle about 30 millimeters in diameter. Thus individual chips can be considerably larger than 10 mm on a side—the limit of many optical step-and-repeat systems except when multiple patterns are stitched together. The largest diameter of wafer the SR-1 can align is 100 mm.

Material. Masks consist of a single-layer 2-to-3-μm-thick membrane of silicon nitride overlaid with a gold pattern 0.8 μm thick. The nitride film is grown on a silicon wafer and the gold pattern fabricated on it by electron-beam lithography. For a 0.5-μm line width, the mask pattern would typically have a diameter of about 15 mm. Resists are similar to those used for electron-beam lithography and can be thicker than the line width for high yield.

In order to match up the different mask layers, it is necessary to align each mask with an accuracy of better than ± 0.1 μm and to maintain it at 10 μm ± 1 μm above the wafer. This is done with the aid of a television camera coupled to a bifocal microscope that can focus simultaneously on both wafer and mask reference marks. Video-signal–process-

Experimental. Step-and-repeat machine built at NTT's Musashino Electrical Communication Laboratory aligns masks with better than ± 0.1-μm accuracy.



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Both instruments feature a large output dynamic range — the 6070A covers frequencies from 200 kHz to 520 MHz; the 6071A range extends to 1040 MHz — and also deliver a high degree of spectral purity. Fluke engineers have developed a number of unique synthesis techniques resulting in noise performance that equals or exceeds that of the best cavity-tuned generators you can buy. Versatile AM, FM and ØM — internal or external, simultaneous or separate — give these new synthesizers the flexibility for wide-ranging applications.

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The 6070A and 6071A are equipped with an IEEE-488 bus interface as a standard feature for systems applications and all necessary front panel functions are remotely programmable. Complete status information can be supplied back to an instrument controller such as the Fluke 1720A. Both "teach" and "learn" modes are provided.

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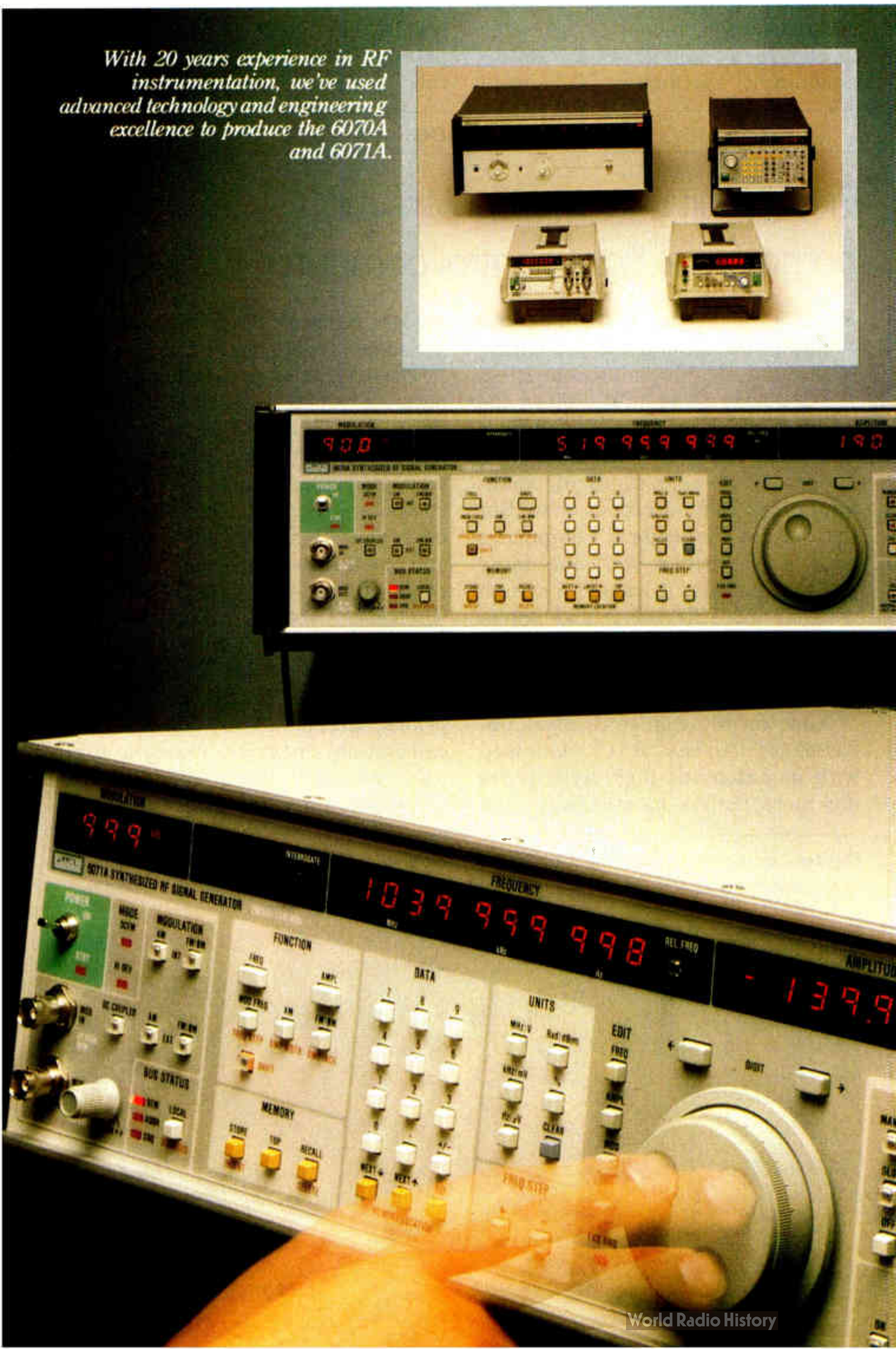

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ing circuits then measure the lateral alignment to within ±0.05 μm and mask height to within ±0.3 μm and make the required corrections automatically.

Output. The system's performance is enhanced by an air-bearing stage for the wafers that is driven in the X and Y directions by moving-coil linear motors with a resolution of 0.05 μm. Each movement and alignment is completed in half a second. At least five 75-mm wafers can be unloaded from a cassette, exposed, and reloaded each hour.

The X-ray source is a rotating anode tube, operated at 20 kilovolts and 1 ampere, that generates the 7.1-angstrom silicon K-alpha line. Since the aligner's working area is smaller than those of other X-ray aligners designed to expose full wafers, it was possible to decrease the source-to-wafer distance to 120 mm. The electron beam inside the X-ray tube is focused to a 3-mm spot on the anode so as to produce the small effective X-ray source area that will maintain high resolution despite the short distance. The attenuation of the X rays is negligible because 117 mm of the 120-mm path is inside the evacuated X-ray tube. **-Charles Cohen**

France

Five 16-bit microcomputers run commercial flight-control computer

In 1979, developing a flight-control computer for commercial use entirely around 16-bit microcomputers was a daring thing to do, given the speed at which the chips would have to handle the enormous amount of data involved—thousands of operations every 20 milliseconds or so. But the Société Française d'Equipments pour la Navigation Aérienne dared just that because it wanted a system with far more flexibility and potential for evolution than any based on discrete elements could hope to offer.

Now, certification trials of a 200-passenger Airbus A310 equipped with its automatic flight system are not more than a month away, and SFENA, based in the Paris suburb of Villacoublay, may have won its dare.

The AFS uses five in-flight computers to control three basic functions. Two flight-augmentation computers between them control trim, yaw, and speed; two flight-control computers together look after autopilot and flight-direction functions; and one thrust-control computer prevents excessive angle of attack, windsheer, and violation of upper and lower speed limits.

Central. The heart of all the computers is an identical set of four printed-circuit boards, one each for calculations, memory, analog-to-digital conversion, and a standard civil aeronautic interface card, the Aero-

Digital. On the flight control unit of SFENA's automatic flight system, the pilot uses push buttons or rotary selectors to enter commands and reads values from liquid-crystal displays.

nautical Radio Inc. 429. Each computer also has additional cards to adapt it to its precise function.

Commands radioed from ground stations enter the system through the Arinc 429 for conversion into 16 bits, 12 of which are correct. The analog sensors send their data to the a-d converter for conversion into 12 bits. The two inputs come together at a bus interface and are sent to the 8086 microcomputer on the calculation board, which computes any necessary changes in the flight pattern using the program stored in its 12-K-byte read-only memory board. The change is converted back into analog information and passed to the servos that physically control the flight of the plane.

Redundant. When all is working properly, the automatic flight system needs only half of its 144-K bytes of ROM and 5 of its 10 Intel 8086 microcomputers. In fact, because of the 10^{-9}-per-hour probability of serious breakdown required as a minimum for commercial flight, every element of the system is doubled—each computer is divided in half by a metal wall, on either side of which resides everything necessary to fulfill all its functions.

Once certified, such a digital flight control system will present numerous advantages over analog systems. Compared with the analog system that SFENA produced originally for the Airbus, the digital unit weighs less than half as much and occupies only one third the space. Also, it is far more reliable, with a mean time between failures of 500 hours, as against 180 hours, and uses only 550 watts as against 1,700 W.

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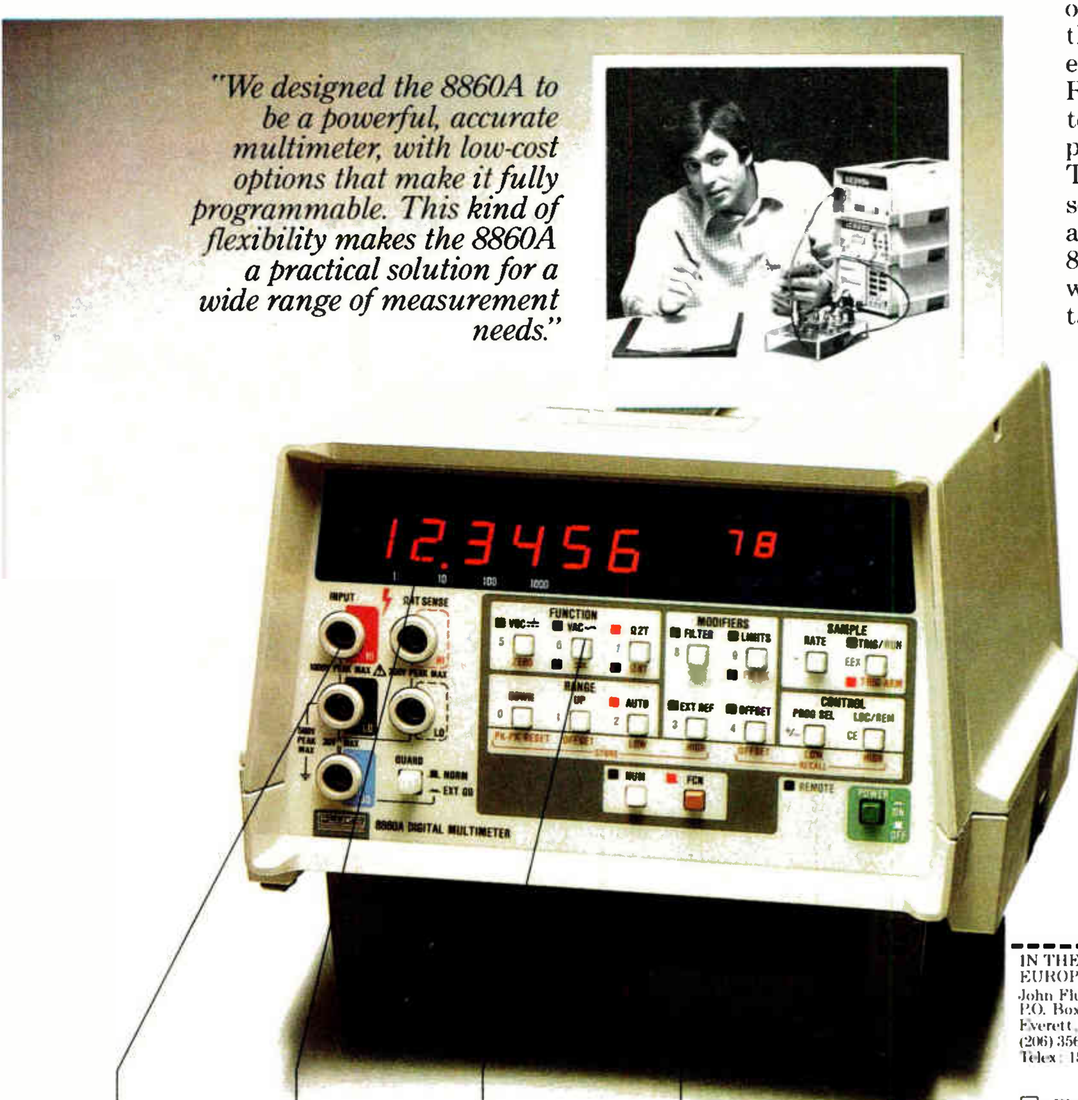

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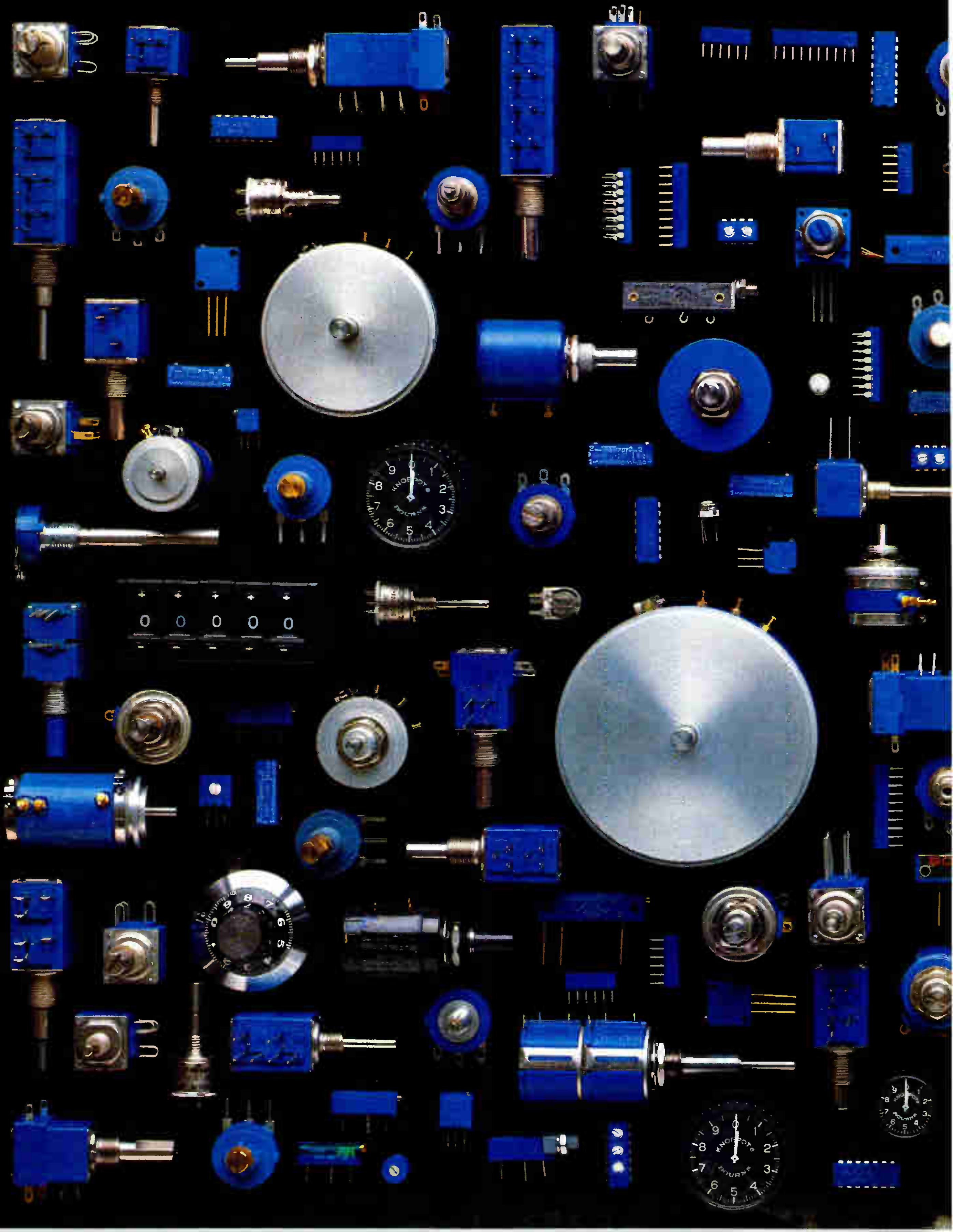

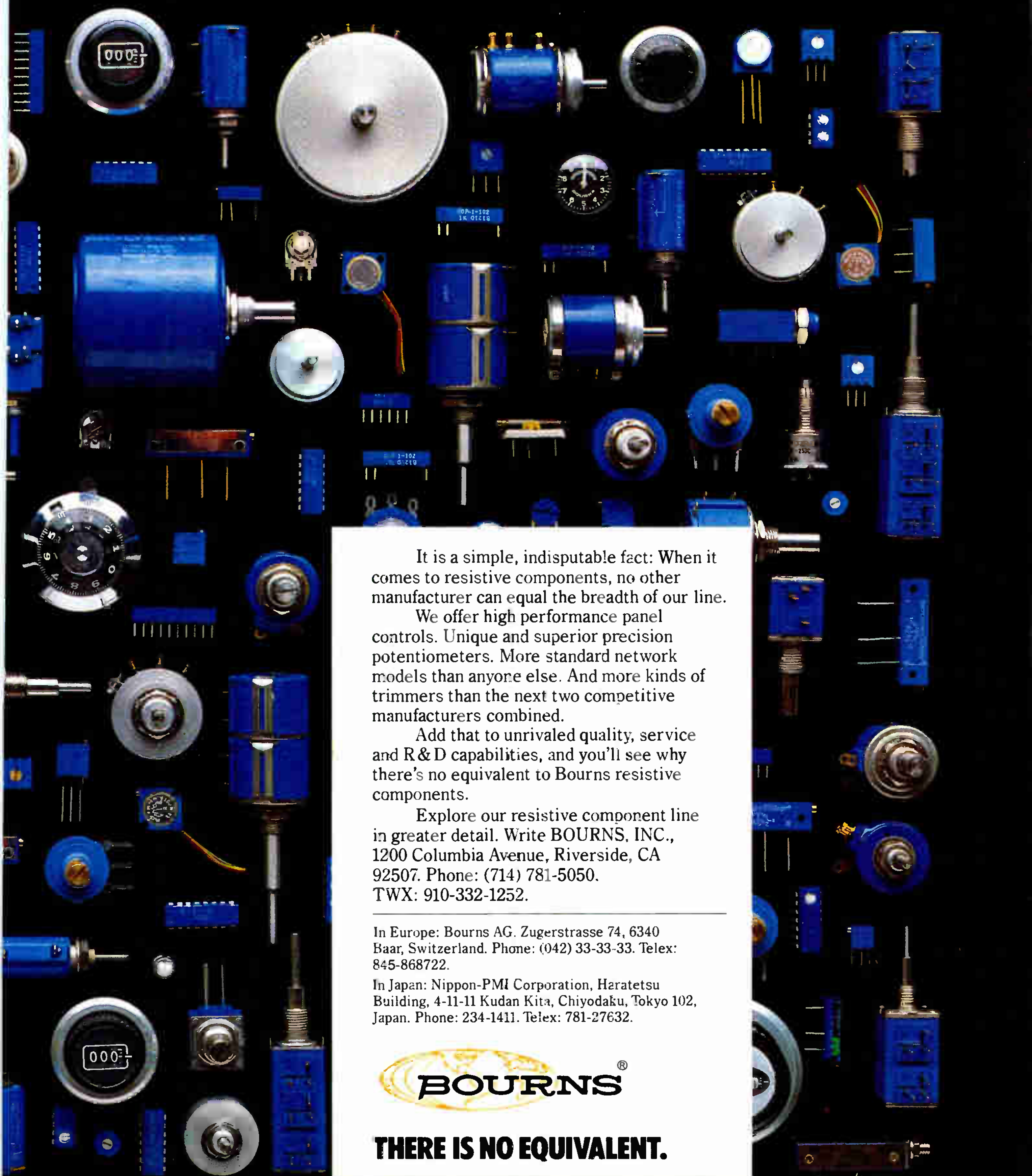

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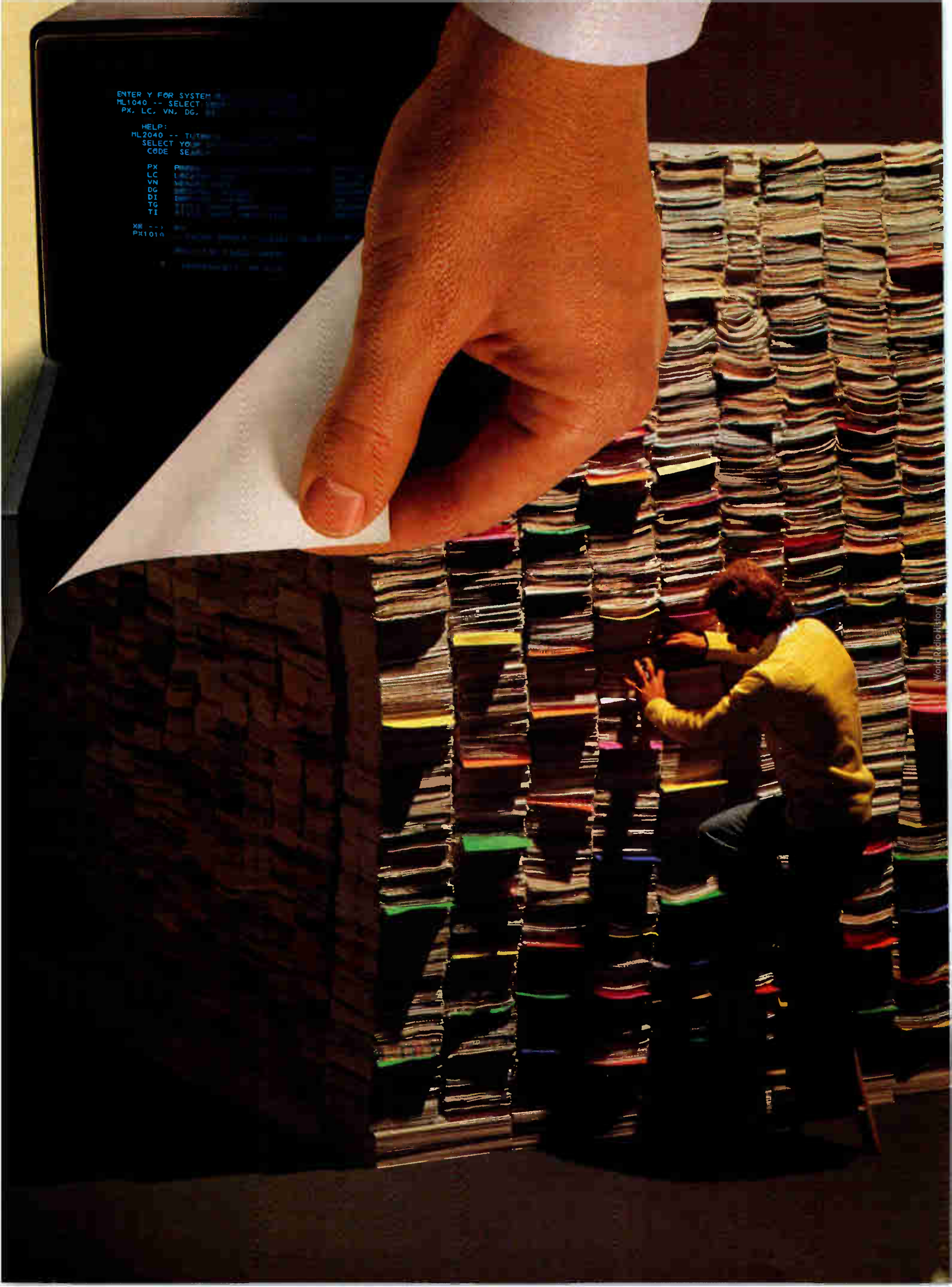
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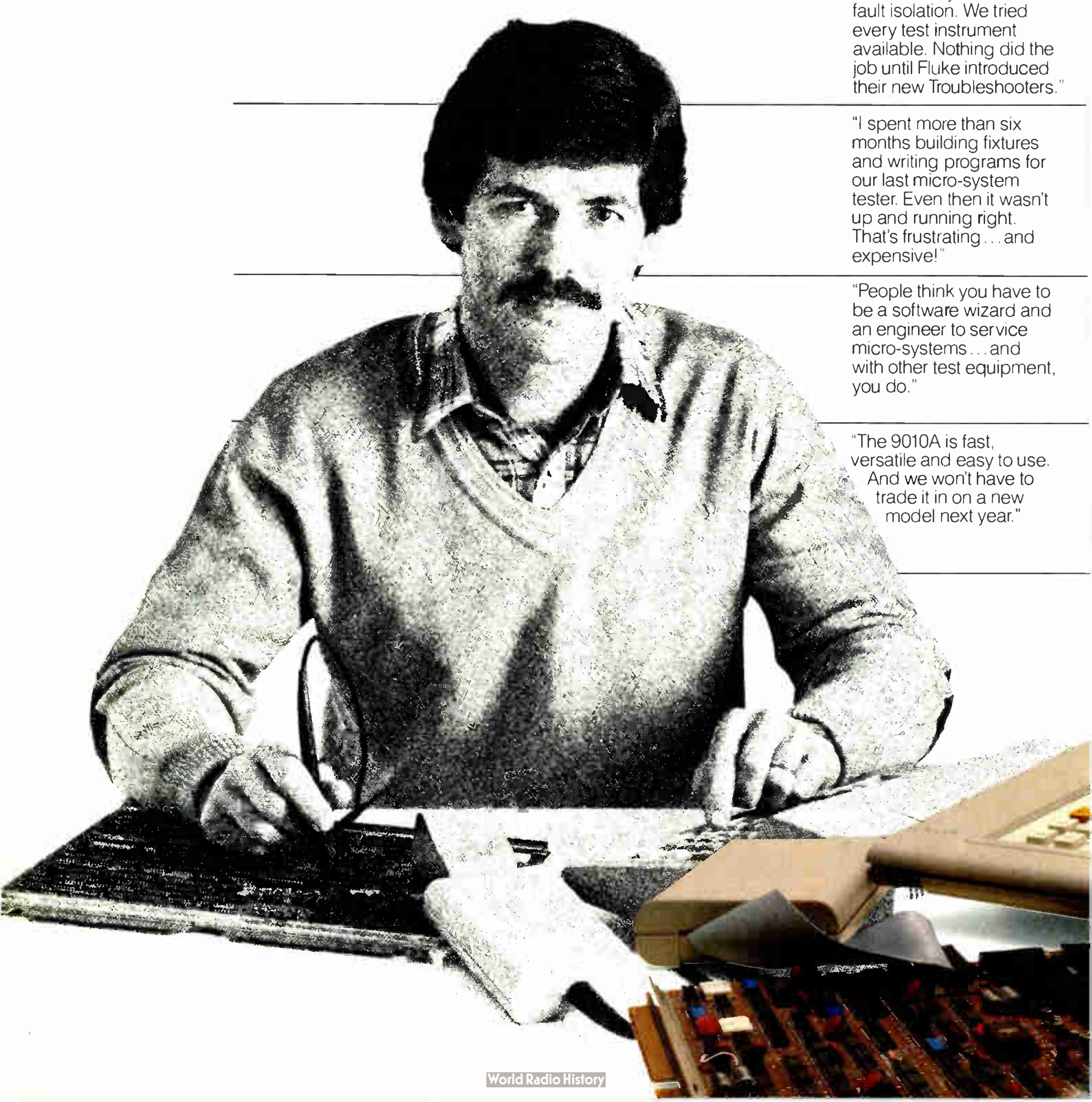

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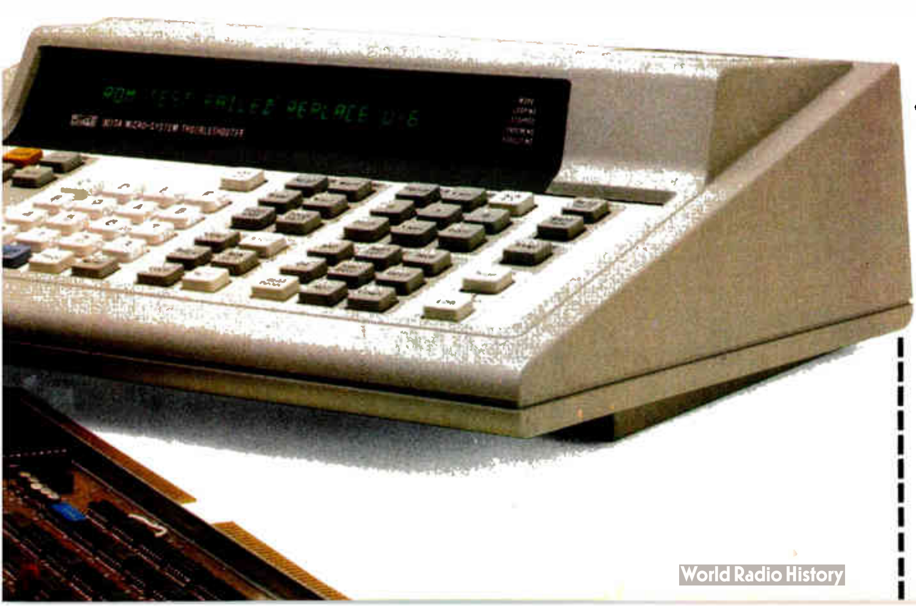

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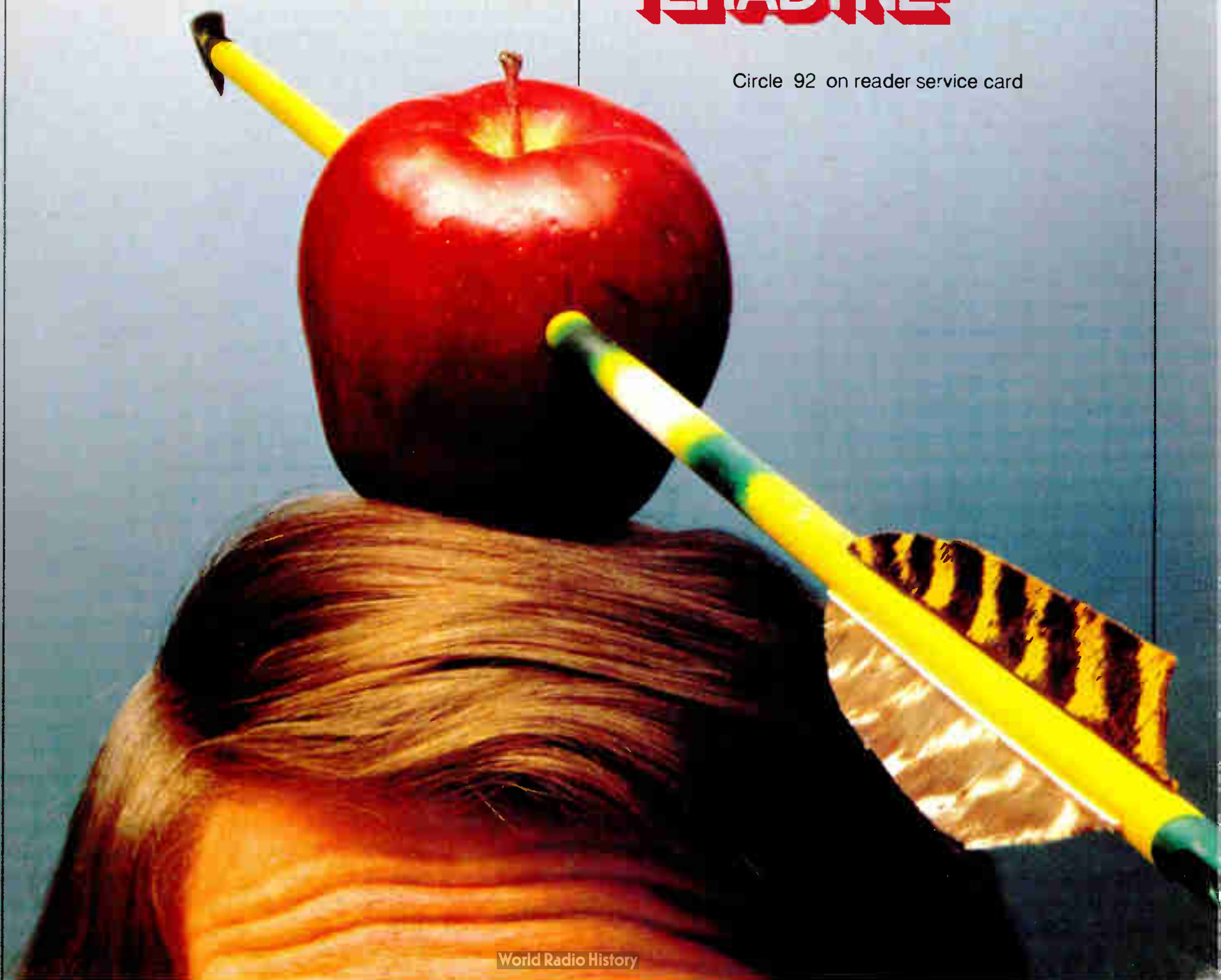

FCC hits computer interference

Testing labs are busy as agency prepares to stop granting waivers from rf interference standards for personal systems

by J. Robert Lineback, Dallas bureau

As microprocessors rapidly infiltrate new consumer and industrial markets, the Federal government has become increasingly concerned about the potential of radio-frequency interference from high-speed digital electronics. Personal computer manufacturers are already feeling the effects of that concern.

This year, the Federal Communications Commission began certifying home computers and other digital electronic consumer devices to ensure that the products do not disrupt television and radio reception. Equipment failing to meet those limits cannot be sold in the United States—unless a waiver has been obtained, but that relief may soon end.

Following the FCC's 1979 announcement that it intended to regulate the industry, computer makers made a dash to line up outside rfi testing facilities for aid in reaching compliance. Since then, independent laboratories have been experiencing a boom in rfi testing, and some labs say they have had to turn away customers. More than six months into the certification program, the FCC is still issuing extensions and waivers for manufacturers unable to meet the requirements.

Although most of the firms filing for waivers have been small peripherals manufacturers, companies like Apple Computer Inc., Commodore Business Machines Inc., and Heath Co. also have had to rely on deadline extensions to continue marketing of some products (see "The struggle for compliance," p. 94).

But the waiver well may soon be running dry, officials at the FCC's rf devices branch in Washington, D. C., hint. They say the agency will most likely clamp down on waiver requests for consumer gear on Oct. 1, the same day the commission begins regulating the commercial and industrial computer industry. Most new waivers will be granted only in "extreme hardship cases"—and most of them to small firms, the sources say.

Under the FCC requirement, Class B computing devices—those for consumer markets—could not be sold after Jan. 1, 1981, if they were not certified or under waiver. The commission's authorization and standards division laboratory in Columbia, Md., is responsible for testing and certifying the equipment.

Measurements are taken on both radiation and power-line–conducted interference. At a distance of 3 meters, radiation cannot be greater than a field strength of 100 microvolts per meter at 30 to 88 megahertz, 150 μV/m at 88 to 216 MHz, and 200 μV/m at 216 to 1,000 MHz. Under the line-conducted test, Class B equipment's maximum voltage feedback to power lines must not exceed 250 μV at frequencies between 0.45 and 30 MHz.

"Whenever we've had failures, I would say more often than not there's been some type of grounding problem with the interfacing cables. Somebody did not get a good enough ground," says Thomas N. Cokenias, engineer at the FCC's testing lab. "But enough are passing that we feel the rules we have made are pretty reasonable."

Tests to end. Currently, the agency is requiring all Class B equipment to be tested at the FCC lab before they can be certified. Because of a manpower shortage and the Federal hiring freeze, workloads have in-

Hemispheric lab. Digital Equipment Corp.'s FCC program office conducts rf interference testing in this air-supported structure.

creased, causing a 60-to-90-day turnaround before products can be certified, Cokenias says. Eventually, he says, the FCC will alter the certification requirement and end testing.

"We often do this [require FCC testing certification] when a new class of equipment comes under authorization. We did it, for example, with CBs," he explains. "Usually it runs about 6 to 18 months. But we have so many manufacturers—some small and some large—just getting around to coming in and there are so many different types of peripherals to be tested," he explains. "So I cannot say when we will decide to end the testing at the lab." When certification requirements end, Class B manufacturers will be required to guarantee their equipment will meet the FCC limits.

Meanwhile, the requirements for Class A gear—commercial and industrial equipment—are less stringent. For instance, at 3 m, Class A rules will allow equipment to have a field strength of 300 μV/m in the 30-to-88-MHz range.

Also, Class A equipment does not have to be certified. Companies must test their own equipment and guarantee that they are meeting the rules. The regulations apply to market entries after Oct. 1, 1981. Existing products (those in production before the October deadline) qualify for a two-year delay.

Digital Equipment Corp. has set up a special laboratory at its complex in Marlboro, Mass., 35 miles west of Boston, to conduct rfi tests for the new FCC rules. With the creation of the facility, DEC plans to do all of its rfi testing in house, says David L. Brown, manager for the firm's year-old FCC program office.

Some digital electronic products are exempt from the rules, however. They are: devices used in vehicles (like autos, boats, or airplanes); electronic control or power systems used by public utilities; industrial, commercial, and medical testing equipment; and computing devices used in home appliances. This month, the FCC's rf device panel proposed a ruling to broaden the exemptions to cover additional equipment.

"For the existing exemptions, we don't have any plans to revisit them in the immediate future," explains FCC engineer Julius P. Knapp in the rf devices branch. "What we more or less wanted to do is to alert manufacturers that we may look at those areas in the future."

Dirty computers. Consumer standards are tougher because there is a greater potential for interference with television and radio reception in the home, says Sid Bradfield, an engineer also in the rf devices branch. "This proceeding was really started because a lot of personal computers were 'dirty' and really were emitting a lot of rfi, which was causing a problem," he explains. "So we had to take a harder stance."

The FCC's position was also taken because it believes consumer products would not be maintained as well as Class A equipment.

The cost of redesign is not low. Glen Dash, president of the independent rfi testing lab and consulting firm of Dash, Straus & Goodhue Inc., Brookline, Mass., says redesign engineering cost for Class B manufacturers should range from $10,000 to $20,000. Dash, who has been doing work in the field since 1975, says manufacturers are falling into a common trap of testing only line-conducted interference and forgetting to attack radiation rfi. "This is a great area of confusion," he says. "The line-conducted measurements are much easier to perform, and conducted problems, in general, are much easier to fix."

FCC engineer Cokenias agrees that radiation testing can be tricky. "After correcting line-conducted problems, sometimes you've got to check the radiation levels again," he says. "I had one case where there was coupling between the power line and the interface bus. Usually that does not happen, but in this machine the physical proximity was such that it would pass the test one way and fail another."

Cokenias says most radiation failures can be corrected by better shielding and grounding. "With the equipment we are seeing here, you would pretty much be constrained to make sure it [rf] doesn't get out of the box, as opposed to lowering the signals inside the computer," he notes. "When you lower the signal, you risk losing logic." □

The struggle for compliance

So far, meeting the Federal Communications Commission's rules for radio-frequency interference on Class B, or consumer, computers has proven to be no small task for manufacturers. After getting a waiver earlier this year, the Heath Co. in Benton Harbor, Mich., spent hundreds of thousands of dollars to bring its computer kits, the H-8 and H-89, into compliance with the rfi rules. Apple Computer Inc. in Cupertino, Calif., finally received certification of its Apple II and Apple II Plus personal computers after a 90-day extension. However, Apple is still awaiting FCC certification on a number of peripherals.

The redesign of the Apple II "took more than several months," explains Michael Connor, product marketing manager. "It took lots of equipment and lots of manpower. And trying to find people that understand radio-frequency interference and digital electronics is not an easy task."

To meet the rfi rules, designers added more shielding (in the form of a nickel acrylic coating) and a special ground plane for cables connecting the Apple II with the disk drive. Some circuits were also changed to cut down on noise, Connor says. "It just takes time. You have to rethink your design to make these adjustments. Unfortunately, if your product is already in the marketplace, then there are a lot of viable parameters that you just cannot change," he explains.

The experience was similar at Commodore Business Machines Inc., which introduced its VIC 20 personal computer last May. To market the machine, Commodore had to obtain a waiver. However, the Norristown, Pa., firm plans to unveil a redesigned version of the VIC 20 within two months to meet the FCC rules, promises Michael S. Tomczyk, product manager. He says the redesign "was as costly as any research and development effort, considering that those efforts are all relative. But modifications are made in all new products after introduction, and I will say that it's simply the cost of doing business."

-J. R. L.

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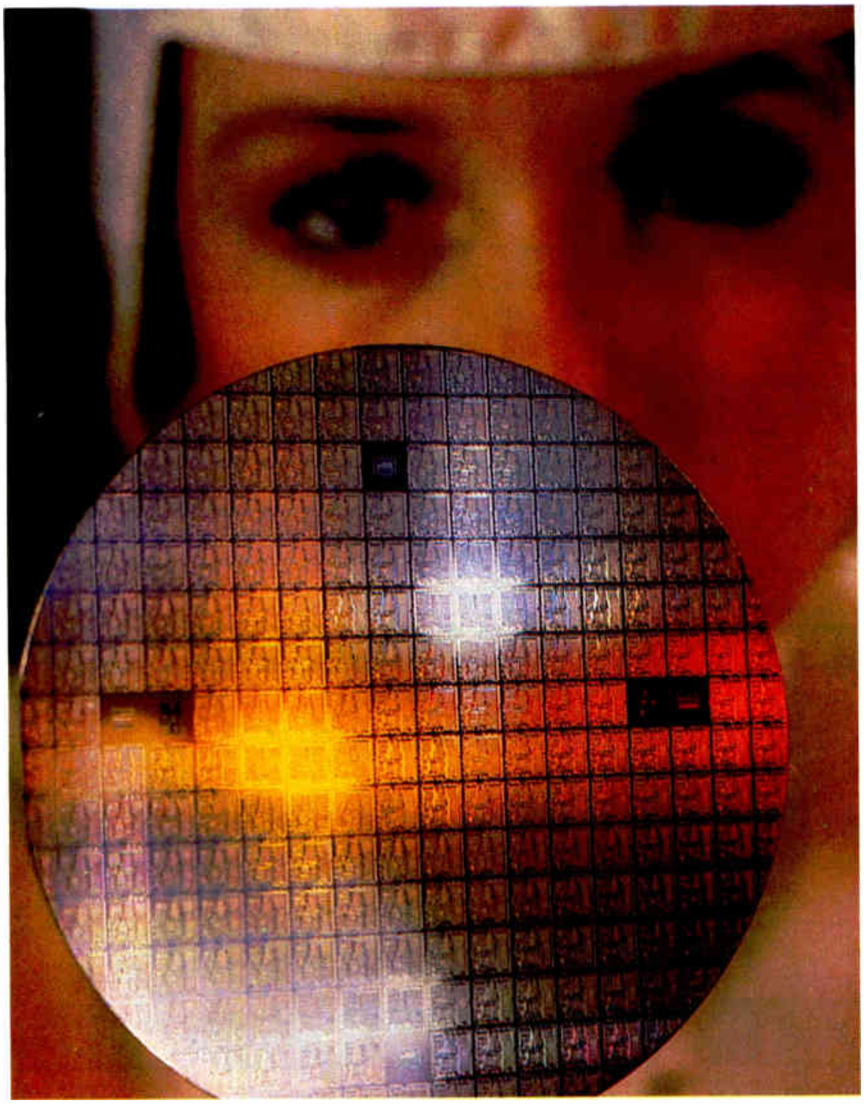

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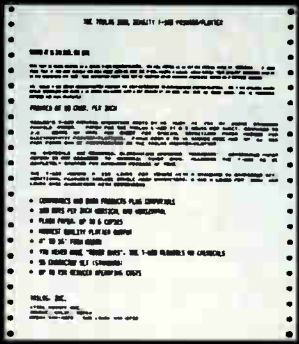

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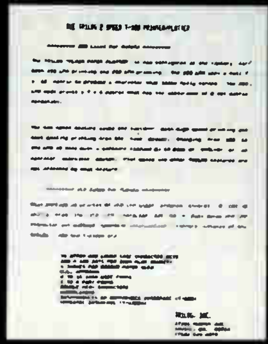

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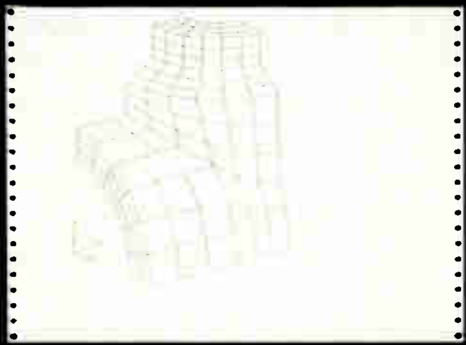

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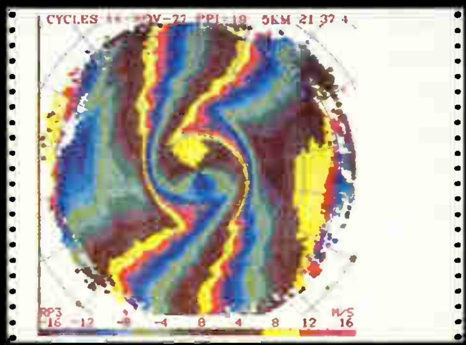

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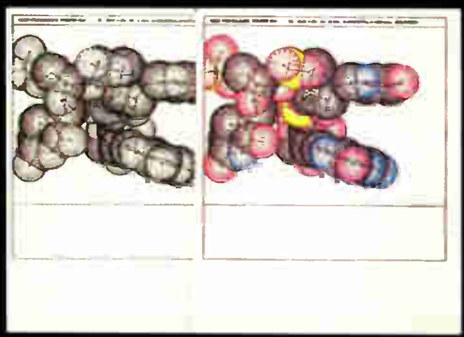

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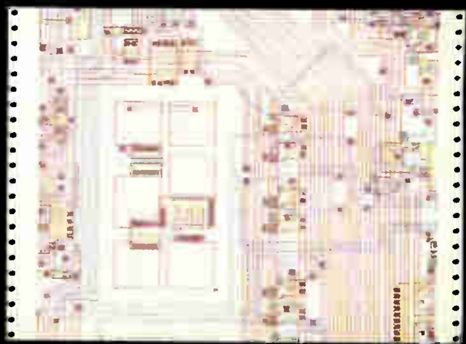

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Communications

Market forms for local-net bridges

Incompatibility of area communications links creates demand for devices enabling systems to talk to each other

by James B. Brinton, Boston bureau manager

With incompatible local-area communications networks proliferating, an ancillary market has been created for equipment to help the computers and terminals in them talk to each other. Such gear would solve the problems of large companies and organizations that find they have installed networks from different makers at different times.

Several companies are working on products for this market, and now a new firm has been tailored to fit into it: Interlan Inc. Paul J. Severino, cofounder and president of the Chelmsford, Mass., company says, "We will offer bridging products to make all these systems more usable," thereby allowing incompatible nets to talk to each other.

Although Ungermann-Bass Inc. of Santa Clara, Calif., and 3 Com Corp. of Menlo Park, Calif., are in the market, Interlan maintains that it has no direct competition. The reason, says Severino, is that in the case of 3 Com, the product is an Ethernet transceiver that Interlan may include in its system; Ungermann-Bass sells a unit that can interface serial or parallel data streams with a network and does not yet market an internetwork gateway. Such firms as Zilog Inc. and Intel Corp. are also working on products for a market that Interlan believes will grow from $264 million next year to $3.2 billion in 1990.

The 34-year-old Severino, formerly engineering vice president of Data Translation Inc., plans to use a modular approach in Interlan's products. Interlan's vice president for engineering, David Potter, 38, will be heavily involved in developing this approach. Most recently manager of the local-network-hardware development at Digital Equipment Corp., Potter is also on the Institute of Electrical and Electronics Engineers local area network standards committee.

"Logically," says Severino, "if you select as your first marketing targets the most common computers and networks and work outward from there, it should be possible to fill orders with minimal custom engineering, regardless of the combination of net and computer."

One board. Interlan is still defining the hardware of its product, but says Potter, the company envisions a single printed-circuit board that can be plugged into the backplane running between the board and local-area network connection point—initially Xerox's Ethernet outlet.

A block diagram would break the board into three sections. One a network block would send and receive serial data packets at whatever rate is needed by the net. Its functions would include serial-to-parallel conversion on receipt, parallel-to-serial conversion for transmission, carrier detection, error detection, and a contention-detection subsystem that

Starters. Three of four founders of Interlan are, from left, Paul Severino, president; Dave Potter, engineering vice president; Patrick Clark, marketing vice president. The fourth, Betsy Miller, is sales vice president.

would signal to the storage-and-control block to trigger retransmission when packets collide.

The microprocessor-based storage-and-control block would have a minimum of 16-K bytes of programmable read-only memory to hold the control code and diagnostic routines for the interface, plus enough random-access memory to store at least two incoming and outgoing packets—4- to 16-K bytes, according to Potter. He says that Interlan will probably use "a fairly fast, no-frills microprocessor," adding that any unit with an appropriate instruction set and speed is a candidate. "Intel's 8109 input/output processor might do the job," he maintains. The block would also supervise operation of the packet buffer and collect network-management statistics, among other tasks.

Latches and logic. The block nearest the computer would be the simplest of the three. It would have one or two latches, 16 bits wide by 1 bit deep, some discrete logic adapted to the control needs of particular computer buses, and direct-memory-access control circuitry.

Pricing at Interlan is as fluid as the bill of materials. "We hope to sell complete interconnection subsystems, including modifications to computer operating-system software, for no more than $4,000 to $7,000 each," says Patrick L. Clark, 34, vice president for marketing—a former manager of business and market planning at Prime Computer Inc. and a former DEC strategic planner.

Such systems would mostly go to end users, he notes, but for original-equipment manufacturers, with hardware and software knowledge, Interlan plans to sell extremely simple network interface cards for about $1,500. These cards would allow network access from already-compatible nodes.

Big game. "We will be going after the largest users of data processing on the Fortune 500 list initially," he says. "That helps us describe both the nets and computers we will be serving first: Ethernet and DEC." Clark is confident of the company's

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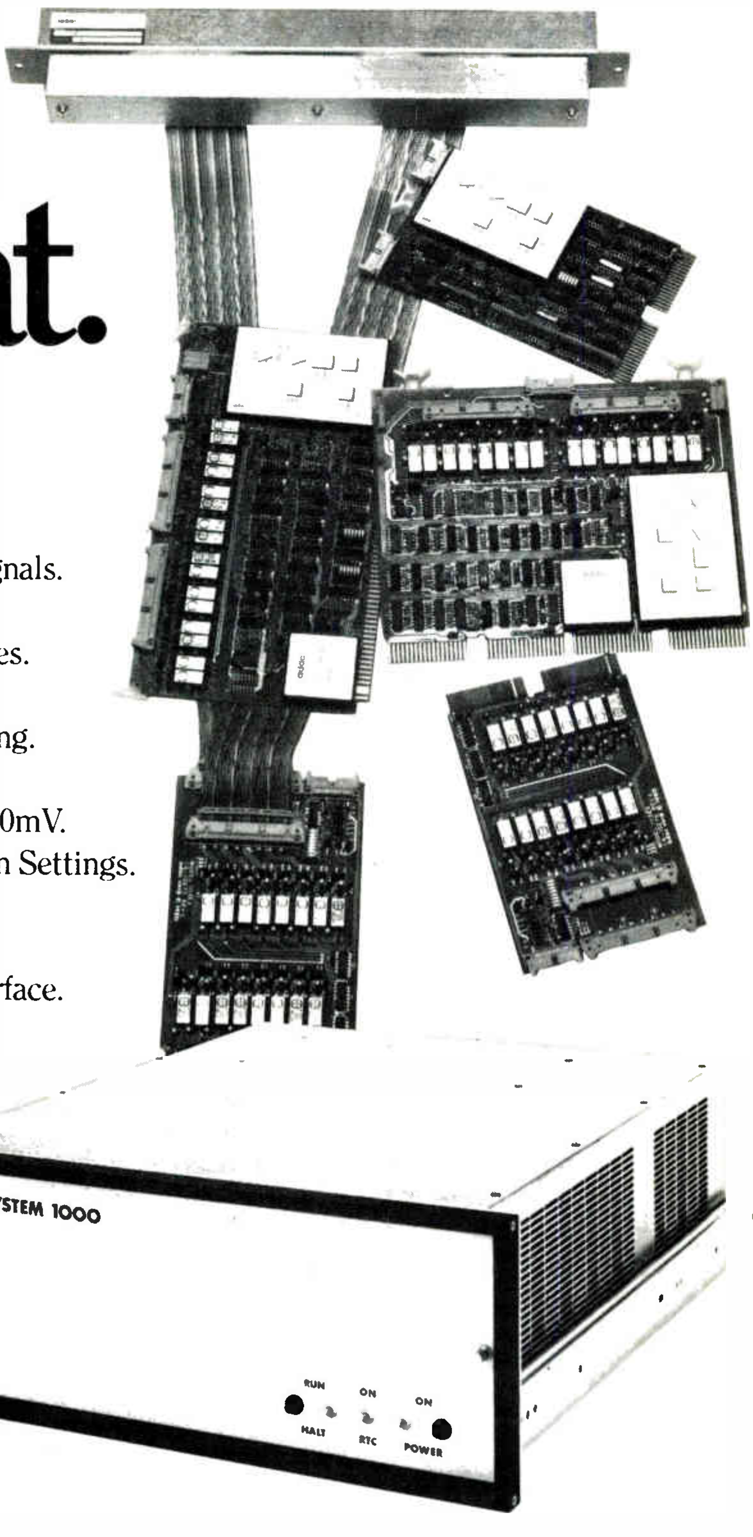

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market: "In five years, we will be a $50 million firm. Remember that the data-communications markets are growing at a 40%-per-year rate."

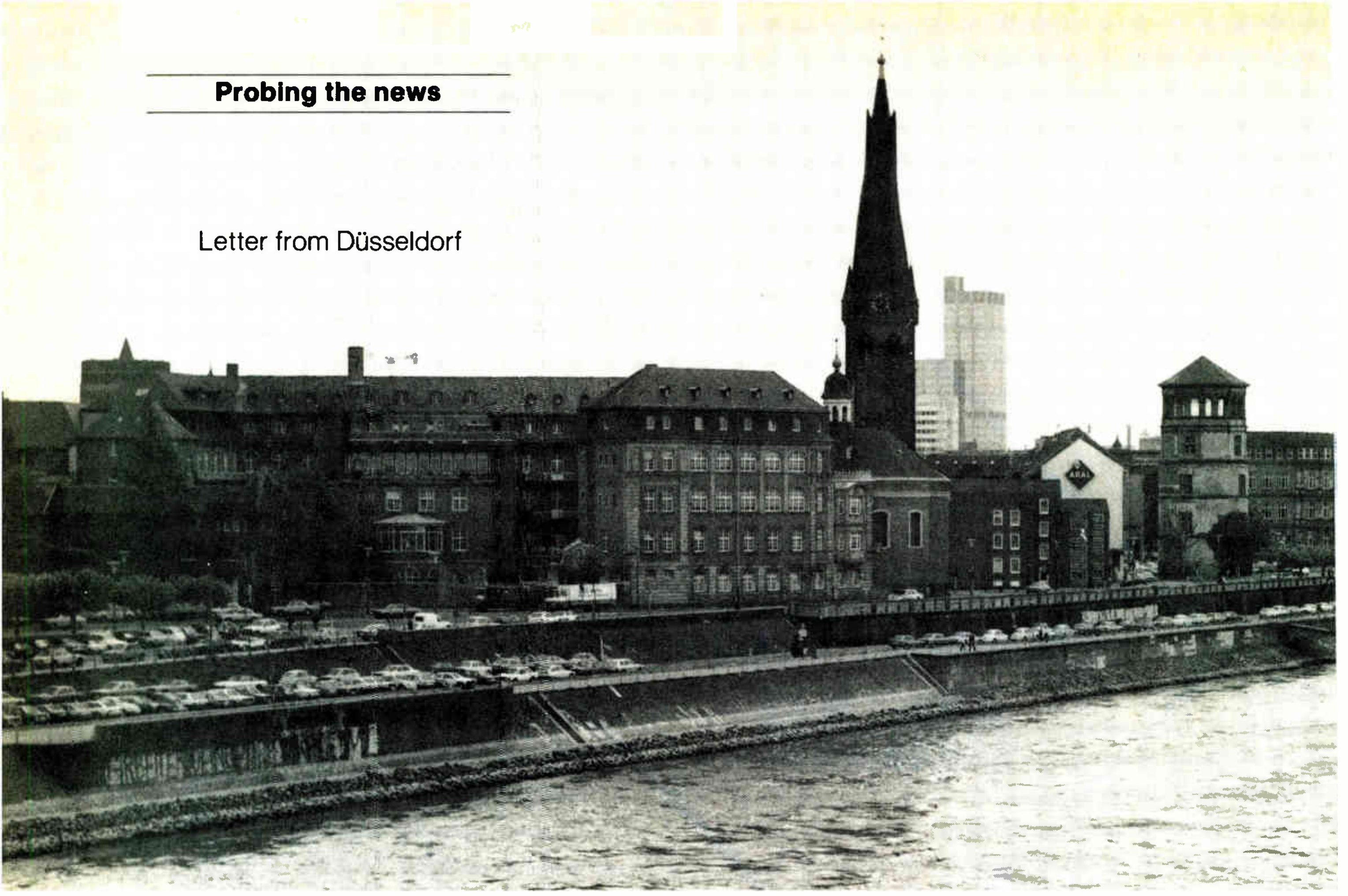
Ethernet is the most important local-area networking system commercially available, he argues. "As of the second quarter of 1981, there were about 45 Ethernets installed [on an experimental basis], serving about 2,000 nodes. The current growth rate both for new nets and added nodes appears to be very high," says Clark.

Bright outlook. The four founders, including Betsy S. Miller, vice president for sales, agree that the firm's markets will continue to evolve. Potter, especially, is convinced of a trend toward higher–data-rate networks—"broadband optical systems, perhaps with multigigabit data rates, subsuming baseband subsystems and capable of offering integrated data, voice, video, facsimile, and most other imaginable communications service" are only a few years away, he maintains.

Interlan should begin shipping by the second quarter of 1982, a fast start for a company with only four employees in mid-1981. According to Russell E. Planitzer, partner at J. H. Whitney & Co., New York, Interlan's corporate prospects are bright. Planitzer is Interlan's financial guru at the venture-capital firm. Until about seven months ago, he managed corporate marketing at Prime Computer. Now he feels that "the founders of Interlan may form a stronger team than we had at Prime in the beginning."

Varied systems. The market is wide open—"I really don't see any competition," says Planitzer. "I studied the market last year at Prime and figured that there would be little local-area network standardization in the next five years and only slow movement thereafter. It is in the interests of computer firms to keep their customers wedded to their own network systems, and therefore to their hardware. What we will probably see is about half a dozen competing local-area networking systems with 8 to 10 vendors, each wedded to one of them." □

Letter from Düsseldorf



Düsseldorf has Japanese flavor

Japanese companies like the location near European capitals and West Germany's Ruhr Valley industrial center

by John Gosch, Frankfurt bureau manager

Düsseldorf, sprawled along the Rhine River, has at least one striking feature that makes it different from other cities in West Germany. It has a large concentration of Japanese firms—in fact, outside of Japan, only New York has more.

The city of 590,000 is European or West German headquarters for some 250 Japanese banks, trading houses, and industrial companies—28 of them electronics firms. The center of their activities is the starkly modern Japan Trade Center, a building that houses legal and patent departments, the Japanese consulate-general, and various economic and trade offices. The European branch of the Electronic Industries Association of Japan is also located in the city.

All the big electronics names, from Canon to Toshiba, are in the phone book. Unlike many companies in other fields, most Japanese electronics firms in Düsseldorf have only national-marketing responsibilities. "The national electronics markets in Europe are too different for just one office to handle effectively," says Takao Negishi, who is director of the European branch of the EIA-J. "So we have, for example, Sony-France, Sony-UK, Sony-Germany, and so on."

Düsseldorf boasts a Japanese colony of roughly 4,500 people, according to the Japanese Chamber of Commerce's managing director, Arira Arikawa, earning for itself the nicknames Little Tokyo and Japan on the Rhine. It is the decision-making center for much of Japan's trading activities in Western Europe, as well as in West Germany. Last year's sales by Düsseldorf-based Japanese firms came to about $3.5 billion, West German sources say.

The Japanese presence in Düsseldorf dates back to the 1950s when trading houses settled in the city to be near West Germany's industrial heart, the Ruhr Valley. Their purpose was to buy machinery that Japan needed for her economic recovery after the war, says Negishi.

In time, as West Germany became a big market for Japanese goods, industrial firms, too, began putting down roots in Düsseldorf. What helped in drawing companies there

was the establishment of a Japanese school 10 years ago (current enrollment is nearly 700 students). "For many businessmen, the school tipped the scale in favor of settling in Germany," Negishi says.

Good transportation. "Also exerting a pull on Japanese businesses is Düsseldorf's excellent geographic location," the EIA-J director points out. A road, rail, and airway hub, the city is also near some of Western Europe's major capitals, trading centers, and sea terminals, with Paris, Brussels, Amsterdam, and Rotterdam all less than an hour away by air. "What's more, within a radius of 300 miles around Düsseldorf lies a market encompassing some 200 million consumers," Negishi adds.

The prime reason that Japanese companies have settled in West Germany is the country's big and open market, Negishi says. A staunch supporter of free trade, West Germany is a free-for-all for foreign firms. Given the German penchant for high-quality products, such as Japan can provide, it is not surprising that the Japanese command a sizeable share of some important market sectors, notably cameras, motorcycles, automobiles, and entertainment electronics equipment.

For all the Japanese marketing successes, Negishi is not without worries, though. One is the rising value of the yen in relation to the West German mark. As a result, the cost of Japanese products sold there has gone up sharply during the past year or so. For example, a Japanese 16-inch portable color-TV set now sells for as much as does a domestic 26-in. color table model.

Limit on TV. Also hurting Japanese competitiveness are the PAL color-TV patents held by West Germany's AEG-Telefunken. Until the last has expired in the mid-1980s, the exports of Japanese-made sets to a country using the PAL transmission standard are limited to 10% of the country's total annual consumption. Additionally, the sets may not have screens larger than 20 in. Negishi says: "Allowed to export only about a quarter of a million sets a year to West Germany, for example, TV makers in Japan cannot achieve economy of scale with PAL receivers." However, Japanese producers can sell more if they set up manufacturing facilities in PAL countries.

Another worry is the rising tide of protectionism in many European countries. Even in West Germany, some industries, including those in the entertainment sector, are clamoring for government help to throttle imports from the Far East through some sort of orderly marketing agreement or to persuade the Japanese to voluntarily limit their exports to West Germany.

Agreeing with West German industry observers, Negishi does not see the Bonn government taking any drastic import-restricting actions in the near future. With West German exports accounting for 23% of total industrial output—the corresponding figure for Japan is 12%, according to Negishi—any import limits the government would impose "would only boomerang and intensify the trade war, thus hurting the country more than benefitting it." □

Software

Object-oriented language feels natural

Languages such as Smalltalk and Flavors mark progress toward programming that matches human thought processes

by R. Colin Johnson, Microsystems & Software Editor

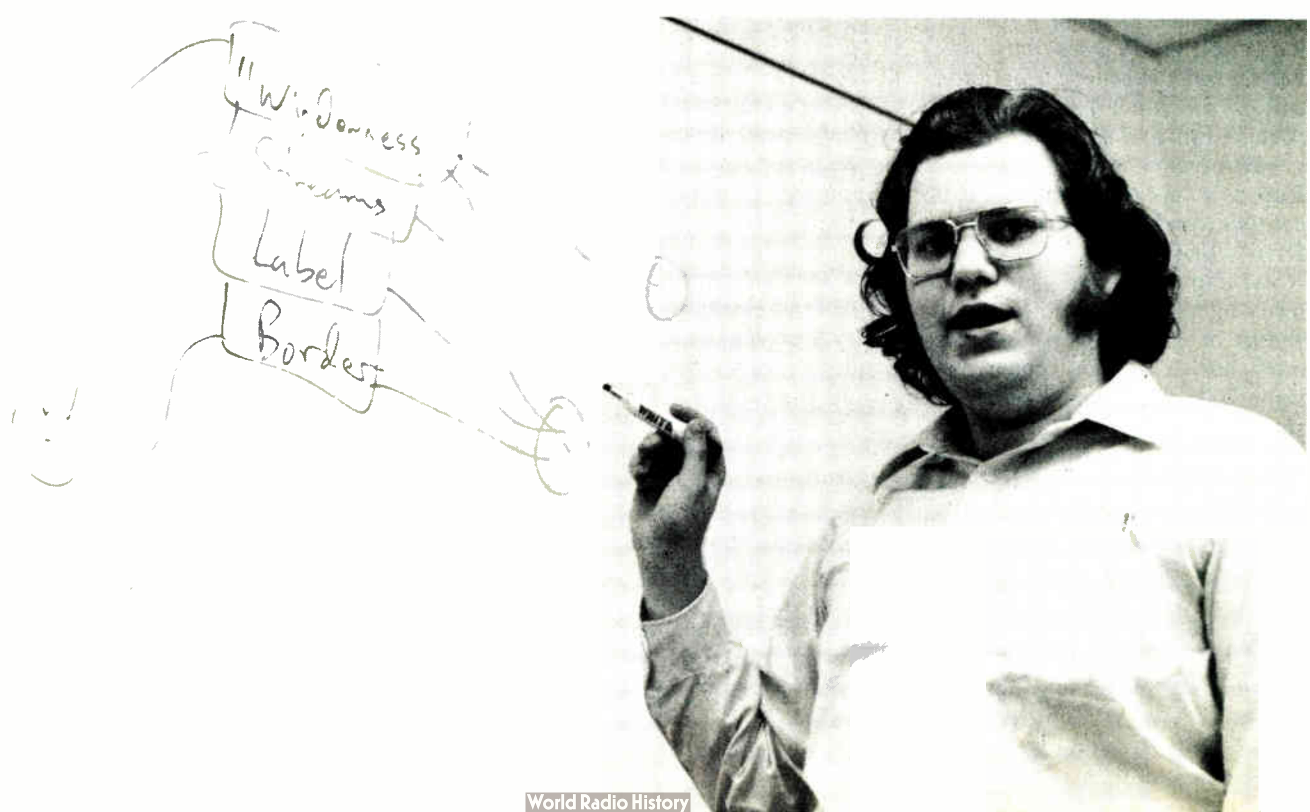
The ultimate in computer friendliness would be the capability of communicating with people in their own language. More and more, object-oriented programming is viewed by researchers as the technique by which that goal may be reached. Xerox Corp.'s learning research group's latest finding in its work toward that goal, to be released this August, is Smalltalk-80.

This language, the fifth iteration of Smalltalk since 1972, benefits from the extensive number of user inputs from noncomputer types—mostly children—who have taken part in the group's Palo Alto, Calif., research projects. These projects delved into how computer systems may become natural extensions of the human thought process.

However, Xerox is not alone in this task. Artificial-intelligence studies, using the language Lisp, have been attempting for years to model the human thought process. But recently both Intel Corp., in Aloha, Ore., with the iAPX-432, and Symbolics Inc., of Cambridge, Mass., with the LM-2 Lisp machine [*Electronics*, Nov. 20, 1980, p. 89], have implemented object-oriented languages similar to Smalltalk. One, Flavors, goes a step beyond Smalltalk by including in it an important feature slated to be incorporated into future Smalltalk versions, maintains Howard Cannon, a member of Symbolics' technical staff.

Object-oriented programming refers to a user-transparent information-storage technique in which contextual information is kept along with data, making the major language component—an object—have not just a value, but also a range of inherited characteristics. Therefore, it helps create languages that are more natural for people to work with, since everyday objects are thought of in just this way.

For instance, a bank account has characteristics such as being a repository for money, having checks written against its balance, and having deposits added to it. In a Smalltalk program, a bank-account object includes within its specification other objects like checks, deposit slips, and a balance, along with the ability to perform the operations applying



Taste. Symbolics' Howard Cannon uses a schematic representation to explain the window system written in his Flavors object-oriented programming language.

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A SMALLTALK GLOSSARY

Object	information and descriptions of the valid operations that can be performed by it
Message	a specification of one of an object's operations, which is then performed by the object
Method	the description of the sequence of actions to be implicitly performed when a message is received by an object
Class	a description of one or more similar objects
Instance	an individual object as described by a particular class
Method dictionary	a set of operations and the methods required to perform them—included in each class description
Metaclass	a class whose (single) instance is itself a class
Subclass	a class that is created by sharing the description of another class, often modifying some aspects of that description
Inheritance	the ability of an object to take on the characteristics of other members of its class as described in the method dictionary

to them. Consequently, operations are not done to objects under the supervision of an intelligent programmer, but instead a message is passed to the object and it performs the operations on itself because it "knows" what must be done.

Using the bank example, if a message is passed to the bank-account object saying that a check has been written for a certain amount, the bank-account object will deduct the amount from its balance, record it among the paid checks, update the monthly statement file, and so on.

This is a radically different scheme for data manipulation from the traditional method of separating operations from the data they operate on. Object-oriented programming emulates how people do things and is thus a more natural way to program.

Inherited traits. Because all of the valid operations that may be performed on an object must be contained within its specification, a method must be used that is less time-consuming than enumeration. This method is called inheritance; it allows an object to take on the characteristics of the class to which it belongs. For instance, the balance in the bank-account example contains an instance of the object "money." It inherits from money the fixed-point data type with two decimal places that people consider implicit in the concept of money, plus the ability to add, subtract, multiply, and divide while rounding to the penny; the concept of a debit implicit whenever a negative value results; and so on.

In this way, a programming problem can be defined in concepts natural to it by specifying objects in the problem and their characteristics and then proceeding to more specific instances while allowing them to inherit most of their characteristics from the various classes to which they belong.

This approach matches the top-down program-development method characteristic of structured-programming techniques. The higher levels are called metaclasses in Smalltalk, and they have instances that are themselves classes. Below those are subclasses that inherit the characteristics of a class plus any alterations to it; for example, the subclass called "foreign bank accounts" inherits all the characteristics of the class "bank accounts" except that a different monetary base is used. At the bottom are instances of the objects themselves plus the messages that are passed between them. In fact, in Smalltalk, an object is a generic type that subsumes all the other types. Ultimately, Smalltalk programs are simply a collection of objects and the messages that they pass among themselves.

In Smalltalk, the inheritance of properties by objects is from the class to which the object belongs. This is a hierarchical organization in which the class inherits properties from its superclass and so on upward until the top level, which is a template for all objects in the hierarchy, is reached. This top object describes the kinds of properties that an object can take on. Such an organization, though powerful, is not well suited to problems where things are not arranged hierarchically.

Xerox is remedying this drawback by including in the next version of Smalltalk the possibility of multiple inheritance: the ability to inherit characterics from several classes that are not related hierarchically.

No waiting. Symbolics, however, could not wait. When working on the program that manages the extensive graphics window system on the LM-2 minicomputer, Cannon realized that he needed a front-end language that could handle Smalltalk-like inheritance without hierarchies. The reason is that a multiple-window system is needed to handle several different types of windows, many of which share characteristics but are not related hierarchically (they are not progressively simpler windows, just different). Thus Flavors was born, a language that can build applications in the same way as Smalltalk because it includes many of Smalltalk's constructs plus multiple inheritance. Flavors, however, is a microcoded extension of Lisp; it is executed on Symbolics' all Lisp minicomputer.

In an attempt to make the iAPX-432's object-oriented architecture more accessible to the users of its evaluation board, Intel, too, has fashioned a language after Smalltalk. The Object Programming Language (OPL) uses basic Smalltalk building blocks, objects, and messages, plus the hierarchical inheritance structuring. However, it is optimized for the specific object-handling facilities of the 432 and is intended as an educational tool for learning the 432, not a general-purpose programming language. □

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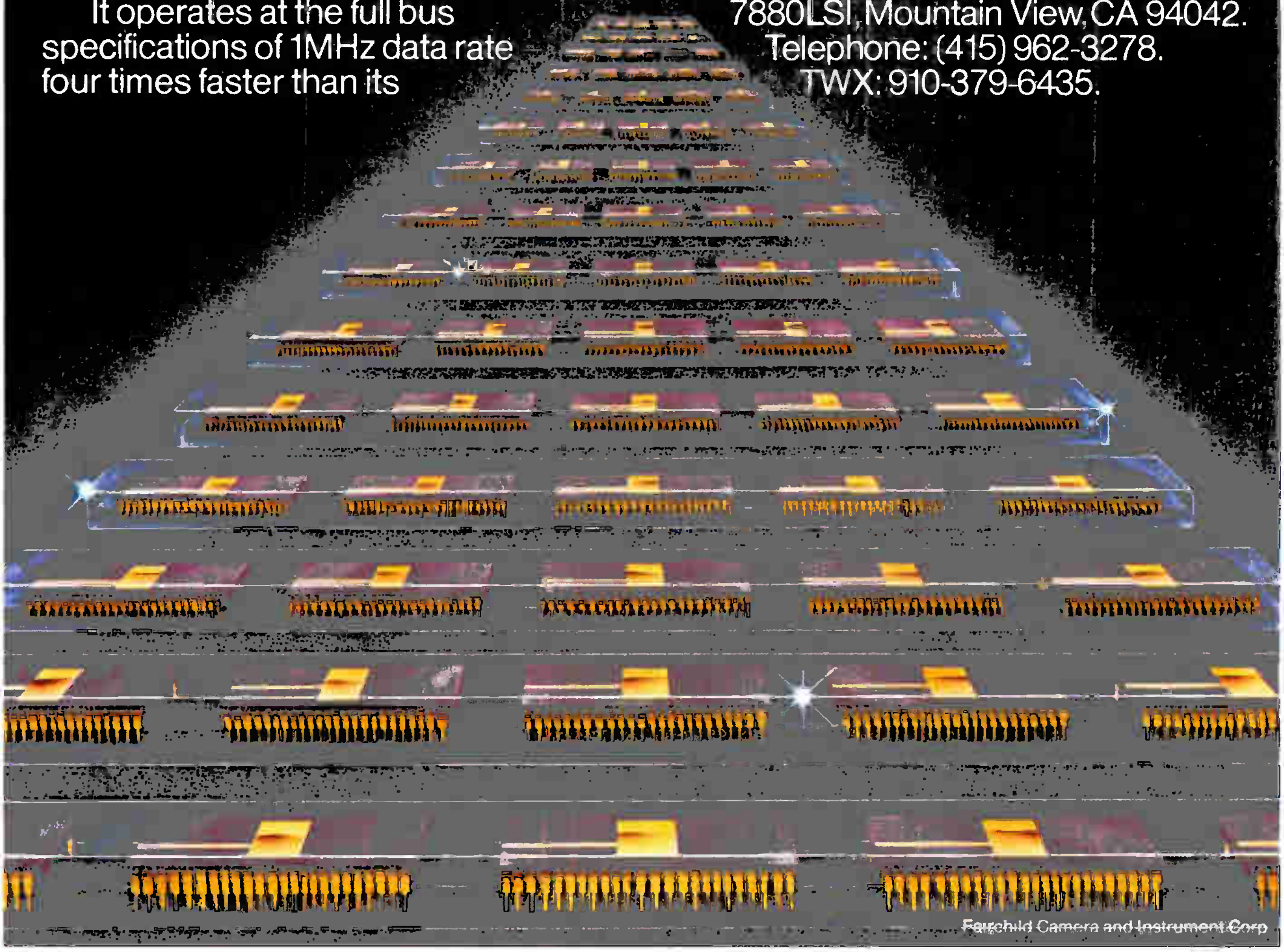

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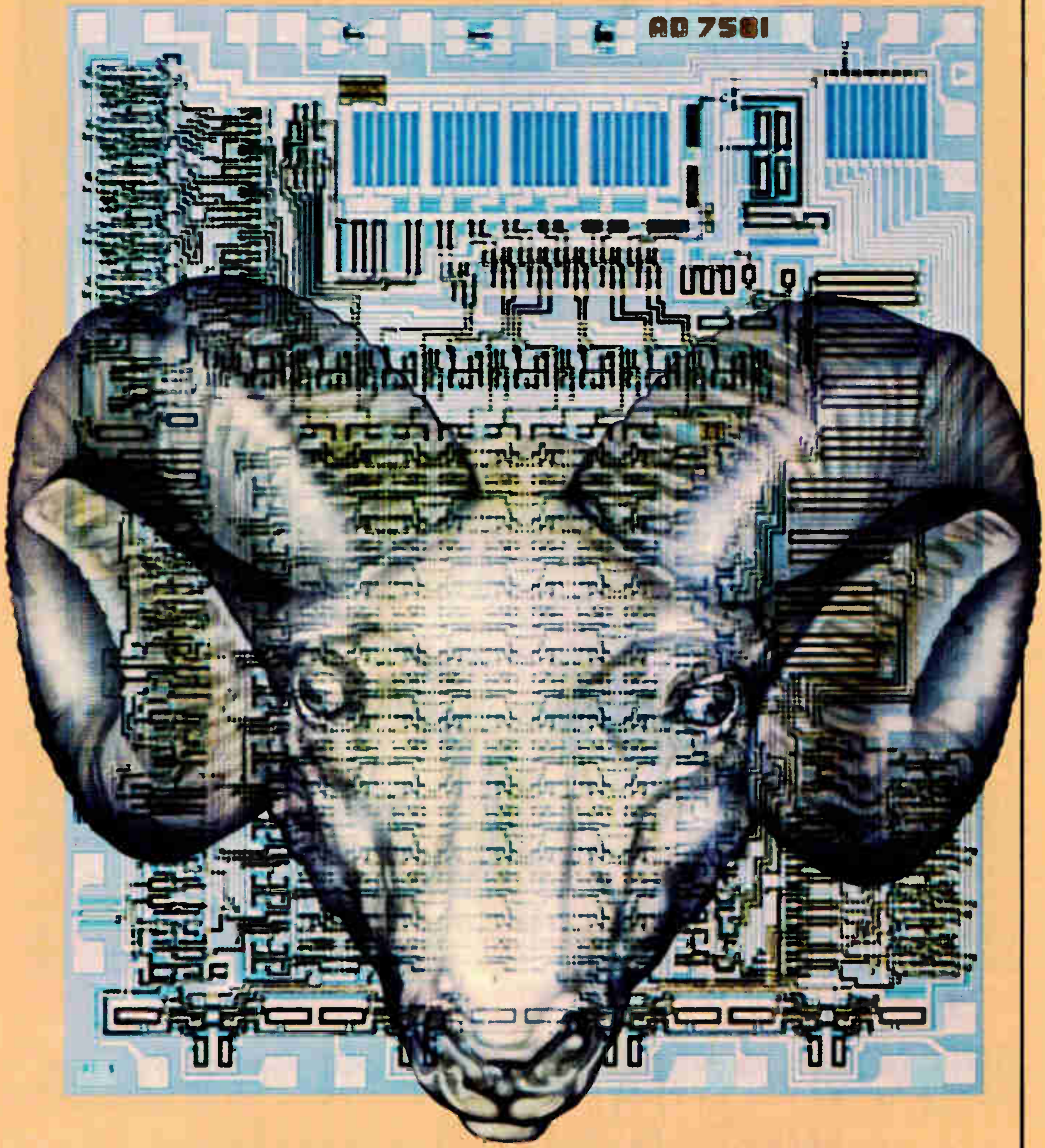

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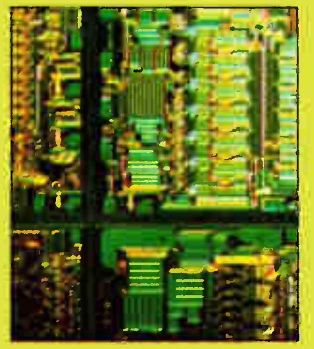

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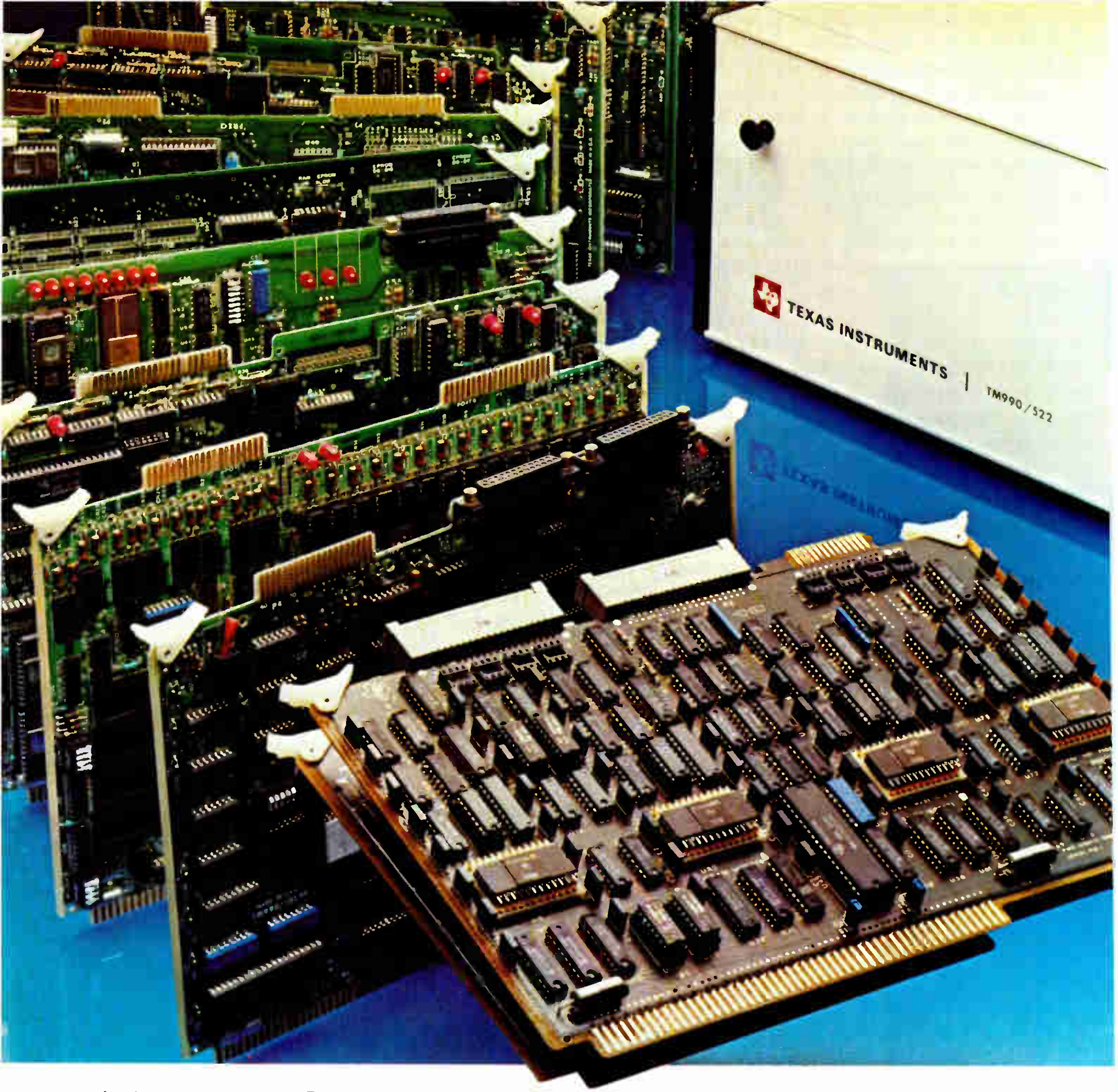

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What to do when the bits go out

Spare rows and columns of cells, swapped in with laser beams or pulses of electrical current, promise to multiply bit reserves

by John G. Posa, *Senior Editor*

☐ If it delivers on its promises, the use of redundancy in semiconductor memory will dramatically augment the industry's output of usable bits. It makes the biggest difference in early chip yields: instead of there being only 1% to 2% of good dice per wafer, the right combination of spare bits per die can suddenly—like magic—make half the wafer good. And the wafers for a mature product will be nearly perfect.

Regardless of the technique used to implement it, redundancy is bound to shake the very foundations of bit supply and demand. Even companies that take issue with the idea for the 64-K dynamic random-access memory agree that spare bits will be a must for quarter-megabit and larger memories.

Captive memory suppliers have already seen something of what just a few spare bits can do—some began several years ago—and that has captured the attention of merchant suppliers [*Electronics*, Dec. 4, 1980, p. 108]. It is said that IBM Corp. got its 64-K RAM off the ground two years early because bad bits in it could be replaced. Similarly, in the early stages of Bell Laboratories' 64-K RAM production, Western Electric Co. experienced yield improvement factors of more than 30 due to redundancy (see "The surprising statistics of yield enhancement," p. 118). And, of course, magnetic-bubble memory vendors would not think to build a chip without extra storage loops as a hedge against flaws.

Now Intel Corp., which has already begun to add redundancy to an entire new line of bit- and byte-organized RAMs and programmable read-only memory components, states that it will be almost impossible for a commercial semiconductor memory maker to compete without spare bits on chip. Likewise, Inmos Corp., credited with having introduced the first commercial RAM with redundancy, is committed to the approach for all future devices. Mostek and Motorola are equally sold on the concept for certain of their memory product lines.

Much controversy

With this sudden burst of enthusiasm for device-level redundancy has come much controversy about how and when to implement it. Although U.S. manufacturers using it swear by the approach, Nippon Electric, Hitachi, and other Japanese memory manufacturers submit by and large that it is too early for redundancy—that, at least for the time being, their memories will be more cost-effective even if the bad units are tossed out. (An exception is perhaps Fujitsu, which has reportedly begun notifying key accounts that its 64-K RAM incorporates spare elements yet to be exercised to bolster yields.)

That is not to say that memory redundancy has not been researched in Japan. At the February 1980 International Solid State Circuits Conference, the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. showed a 256-K dynamic RAM that contained 4-K spare cells, electrically substituted for bad ones by means of polysilicon fuses.

Although it is unclear whether that part will ever see production, NTT's laboratory did later design one of the first ROMs to use redundancy—a 1-megabit chip that will be built by Oki Electric Industry Co. [*Electronics*, Oct. 9, 1980, p. 65]. Realizing that it is practically impossible to go back and mask-program spare bits in accordance with a customer's proprietary pattern, the lab actually put 2 megabits on the ROM, hoping to get 1 million good bits (Fig. 1).

About the only other published work on redundancy in Japan was carried out at Hitachi Ltd. At this year's ISSCC, the company described how to heat up polysilicon with a laser so as to activate dopants and lower its resistance, thereby creating a conducting link where before there was none. Though the scheme was discussed in relation to a 4-K static RAM, Hitachi actually developed the technique for a 64-K static RAM now in design. It is an interesting idea, but the highly doped polysilicon regions are apparently high-impedance load resistors placed at the chip's periphery; thus, without added process steps, they can be used only on static RAMs.

Japan's cavalier attitude toward redundancy could mean two things. One is that Japanese memory manufacturers expect that their RAMs—particularly 64-K dynamic and 16-K static parts—will achieve high yields naturally and quickly. But it could also mean they have missed the boat on redundancy and are afraid to admit it. If that is so, redundancy could propel the yields on critical memory components of those U. S. manufacturers adopting it well above the competition's at a time when the parts are desperately needed.

In the U. S., component-level redundancy concepts predate the dynamic RAM itself, according to Mel H. Eklund, vice president of Integrated Circuit Engineering Corp., an industry consulting firm in Scottsdale, Ariz. In the early 1960s, IBM was actively investigating opportunities to enhance bipolar RAM yields, and this led to one of, if not the first, paper on redundancy in 1964.

In the late 1960s, says Eklund, Fairchild Camera & Instrument Corp. was building a bipolar RAM for the Illiac-IV computer, whose three-out-of-six addressing scheme allowed a fifth of the chip to be defective. In about 1973, Honeywell Inc. pioneered a full-wafer memory that used fuse elements not to exchange bad elements for good, but to circumvent bad addresses when defective blocks were referenced.

Memory-chip redundancy took over a decade to catch on because a reliable means of swapping in spare elements was lacking, because circuit densities did not justify the added complexity, and because of a reluctance to accept less-than-perfect parts. And despite its current popularity, the issues associated with redundancy have by no means been settled.

Even among the proponents of redundancy, dissension abounds over how many spare bits should be provided and how they should be organized. It is not obvious how many spare cells will most benefit the manufacturer in

Yield enhancement statistics

One of the growing list of people to have investigated the mathematical implications of memory redundancy is Al Tuszynski, an associate professor in the electrical engineering department of the University of Minnesota in Minneapolis. He explains that the incidence of small, random flaws on a wafer is modeled convincingly by the Poisson distribution, expressed as:

$$P(n,\lambda) = \frac{\lambda^n}{n!} e^{-\lambda}$$

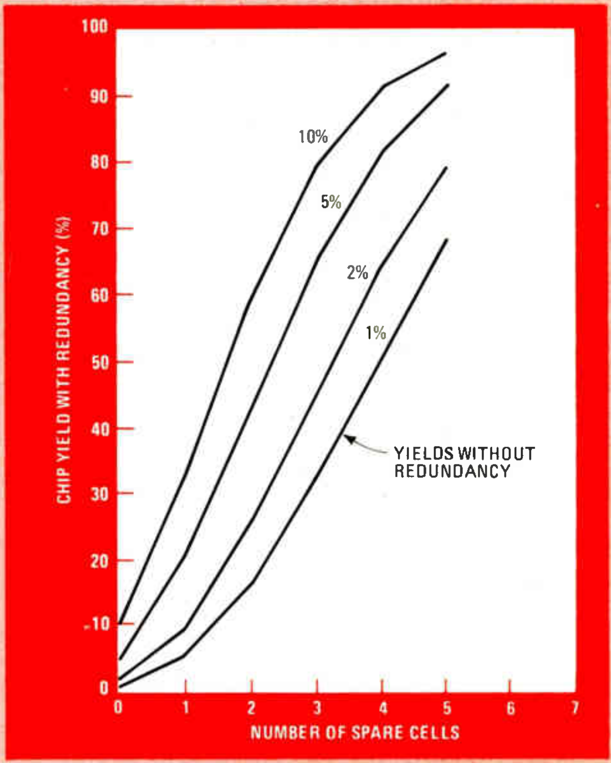
where $P(n,\lambda)$ is the probability of n defects per die and λ stands for $\bar{n}$, the average number of defects per die.

The yield allowing for m substitutions, $Q(m,\lambda)$, is obtained through the summation of all pertinent defect probabilities, or:

$$Q(m,\lambda) = e^{-\lambda} \sum_{i=0}^{m} \frac{\lambda^i}{i!}$$

The curves present the yield improvements possible given initial yields without redundancy of 1%, 2%, 5%, and 10%.

"The results," states Tuszynski, "are impressive to the point of being incredible—five excess cells boost the 1% yield to 67%." But he notes that the Poisson distribution applies only to small, random defects and "unfortunately, where the yield is low, defects are neither small nor random." Moreover, faults in peripheral circuits or cell failures that short power lines may simply be impossible to correct.



terms of yield improvement or what area or speed penalties, if any, might be incurred through their substitution. There is even debate about reducing the level of redundancy once a product has matured or removing it altogether. Also hotly contested is the means used to swap in the spare elements, whether redundancy poses any special reliability concerns, and whether or not users should be informed if otherwise imperfect ICs have been mended with spare bits—and, if so, where the substitutions have been made.

The need to know

Users may wish to know which rows or columns have been replaced in order to carry out pattern-sensitivity tests. These demand a thorough knowledge of how external addresses come to be mapped into a chip's physical cell array. To appease such users, Mostek Corp. has pioneered a "roll-call" function on a new 16-K-by-1-bit fast static RAM [*Electronics*, March 10, 1981, p. 228].

To activate the roll-call function, control lines are configured in a particular way as column addresses are cycled. The chip's output will go high only if the column addressed is a spare. It is not yet known whether Mostek will provide other memories—like its 64-K RAM—with the feature. Meanwhile, some other chip makers submit that making a customer privy to which substitutions have been made serves only to open a Pandora's box.

On a memory with redundancy, incoming addresses are compared with the locations of bad bits; when a match is found, spare bits take over. Substitutions can be made for individual bits, small clusters or large blocks, or rows or columns. Spare rows and columns have become the most popular approach because they represent a reasonable tradeoff between yield enhancement and the number of required programming elements and associated circuitry. If multiple lines of redundant cells are present, comparisons for each line occur in parallel.

A good example of large redundant blocks can be seen on Mostek's 64-K E-PROM [*Electronics*, March 13, 1980, p. 115]. This early effort at on-chip redundancy incorporated a huge, 25% bit surplus—and expanded die area by 20%—to limit the number of polysilicon fuses. Future static and dynamic RAMs from Mostek will go the row or column route to trim such area penalties.

The bad addresses can be programmed with the aid of electrical fuses, laser cuts, or nonvolatile storage elements like floating gates. Faulty locations could even be held in latched flip-flops or on-chip RAMs, but the volatility of these devices has precluded their commercial use. Future erasable and electrically erasable PROMs and perhaps even RAMs may incorporate nonvolatile elements to store bad addresses, but for now the rivals are electrical fuses and laser links. Although IBM Corp. blows out metal fuses on its current line of high-density RAMs, merchant memory suppliers have instead opted for polysilicon as the fuse material, probably because of their greater familiarity with that material than with metals and silicides. Intel is one of the only manufacturers of bipolar PROMs using polysilicon fuses.

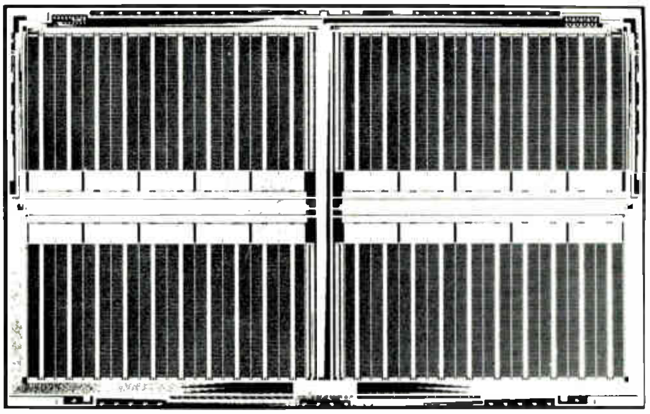
In a rudimentary redundancy scheme, when the user hits a bad address, a group of spare cells is enabled and access to the normal cells is somehow inhibited. This explanation makes redundancy sound simple to implement when in fact it can easily become very complicated. For instance, the access time of the memory may be longer for the redundant addresses because of delays through comparison logic and steering circuitry. In a high-performance device like a fast static RAM, such delays may be intolerable.

In addition, spare columns and spare rows usually exhibit different access-time penalties. According to IBM, faults along word lines (the rows) are harder to hide in terms of performance because word-line activation ordinarily occurs immediately after decoding. Unfortunately, a manufacturer may be forced to include spare rows (or columns) because its process technology may cause one or the other to be more defect-prone. Circuit design, too, must be considered. Redundant rows and columns are usually supplied with extra decoders so that these can be replaced when their associated cells go out. Bit-line redundancy can also be easily extended to replace delicate sense amplifiers.

Easily complicated

Problems also arise when a memory is wider than 1 bit. To save on the amount of redundant elements, logic can be added to determine which bit of the word, byte, or 4-bit nibble is defective and replace only that bit. On the other hand, to avoid the circuit-design and testing difficulties, it might be easier just to replace all the bits of a word—even the good ones—and be done with it.

One of the biggest controversies surrounding on-chip redundancy is whether to make the substitutions by blowing fuses electrically or by laser beam. Polysilicon fuses at first seemed to be the perfect solution because



1. Two for one. It is difficult to design redundancy into a mask-programmable read-only memory, since the spare cells would have to be encoded with a customer's personalized pattern. That led Japan's Musashino lab to a 1-Mb ROM with 100% redundancy.

they could be fashioned with standard processing and be blown with widely available test equipment while the wafers are probed. However, the circuit-design flexibility afforded by the small and simple laser links is making even the biggest supporters of electrical fuses once again weigh the alternatives.

Pulses versus beams

Unlike fuses, which require sufficient area for high-current transistors and associated logic, laser targets can be built with minimum features. Thus, there can be many more of them on a die and they can be put anywhere—even in the center of a chip—since they need no power lines whatsoever. Laser links may also be placed between the decoder and the memory array and configured as hardwired logic without the device's performance being inherently compromised. Electrical fuses, to limit their number, are usually placed before the decoders and considered in the on-chip decision of whether or not to enable a spare row or column. That in turn may force the designer to come up with a way to parallel operations to avoid delays.

So far, Bell Laboratories, Hitachi, and Mostek have made public the decision to use a laser for redundancy programming. In all cases, polysilicon targets are used in lieu of metal ones because the former absorb beam energy very efficiently, whereas the latter splatter conductive material on the surface of the die.

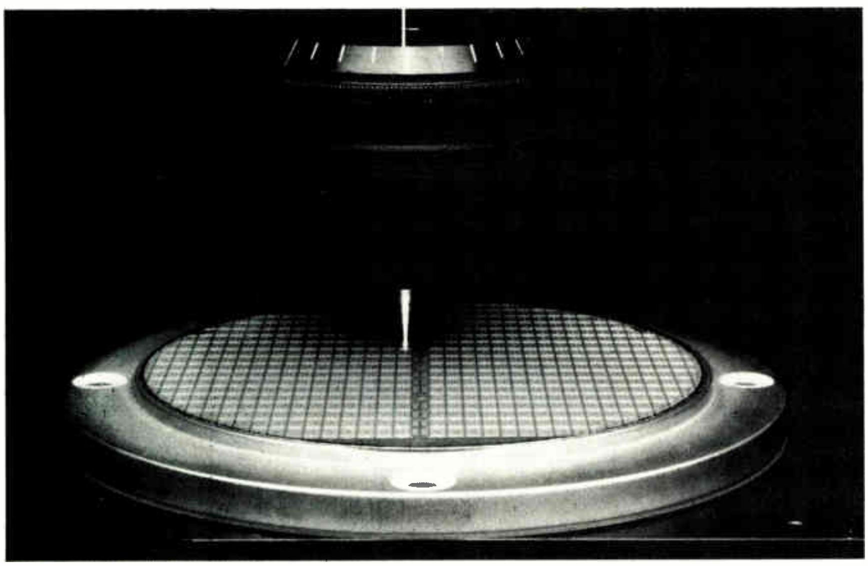
Lasers do not require a more sophisticated test machine, except for its more involved software, which does inflate testing time. Skeptics also cite the high price tag put on the laser and positioning system itself. True, such a system runs from $250,000 to $300,000 but, according to Robert T. Smith, a member of Bell Labs' Allentown, Pa., technical staff responsible for laser programming (and an author of one of the following articles), a complete production system handling a moderate volume of devices in the 30-to-40-square-millimeter size range can pay for itself in 7 to 13 weeks.

Opponents of laser programming also voice their concern about device reliability, since the beam has to be driven through a layer of polysilicate glass passivation before severing the polysilicon link beneath. "But I defy anybody to find a difference in reliability" is Smith's reaction to this.

It is said that the laser beam will be unable to dependably strike the links as they become finer and finer in future generations of memories. However, according to Joseph McCarthy, marketing manager for Electro Scientific Industries Inc. of Portland, Ore., a major supplier of lasers for redundancy programming and other IC applications, "Our machines now have sufficient accuracy in beam diameter and positioning to take care of 64-K and 256-K RAMs, and we have equipment in development for higher-density chips."

In meeting the challenge of redundancy programming, Electro Scientific came up with its Microlase wafer processor model 80, which manages the stringent requirements for spot size and positioning. Like other industrial lasers, the system incorporates a continuously pumped, repetitively Q-switched neodymium-doped yttrium-aluminum-garnet (Nd:YAG) laser operating at a primary wavelength of 1.064 micrometers. However, its highly stable beam lasts only 35 to 40 nanoseconds, and the firm recently introduced a second harmonic generator that produces a visible green beam (Fig. 2) at 0.532 μm. Besides Electro Scientific, Teradyne Inc. and others are tuning their lasers for redundancy.

Redundancy need not be limited to memory chips. IBM suggests that it could well be applied to charge-coupled devices and logic applications, with extensions for module and card uses. Single-chip microcomputers, with their swelling stores of on-chip RAM and ROM, also appear to be prime candidates. □



2. On target. Laser programming is becoming increasingly popular as a means of replacing bad memory elements with good spare ones. The targets can be placed anywhere on the die and configured so that performance is not degraded. The beam above is exaggerated by the length of the exposure; in fact, it is only micrometers wide.

DUNDANCY REDUNDANCY REDUN

Designing static RAMs for yield as well as speed

As with cell architecture and process technology, spare elements must be considered well in advance

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☐ Redundancy must be planned for at the outset of a memory design if high performance and high yields are to be simultaneously enjoyed. If technology and cell layout are optimized for speed alone, without regard for yield enhancement, spare elements will be only marginally effective. Likewise, if a completed design meets performance goals, retrofitting redundancy to it may increase yield but introduce delays that make it hard to attain the original goals for speed.

The right type and amount of redundancy for a given memory are dictated—indeed, predetermined—by the process technology and cell architecture selected at the beginning of the design. Redundancy implementation is in fact an iterative process that evaluates the various circuit, process, and cell-layout options available until the mix that achieves the most manageable defect density is found.

Fortunately, for a given memory cell layout and a given processing technology, it is possible to estimate the likely chip defect density, which in turn can be used to calculate the number of spare elements necessary to maximize the yield. Also to be factored into the equation is the cost of the testing and programming necessary to repair the defects.

Single polysilicon or spare rows?

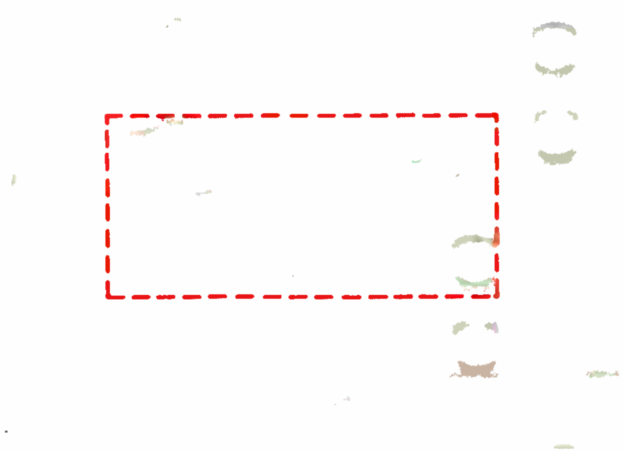
The use of spare bits, clusters of bits, or blocks of bits is either inefficient or impractical. The choice is therefore between spare rows or spare columns for maximum flexibility and ease of implementation. An iterative analysis can be performed, starting with memory cell design, followed by a preliminary study of the cell layout that will serve to identify the cell's most likely failure modes. These are determined by mask alignment tolerances, feature sizes, layout ground rules and process technology idiosyncrasies.

Double-polysilicon cell designs typically use selectively doped second-level polysilicon for the supply voltage (V_{cc}) line and the high-resistance loads. This memory cell layout requires first-level polysilicon rules—word-line and cell drivers—and buried-contact ground rules to be much tighter than metal and metal-silicon contact rules. Therefore, the most likely kinds of defects are related to the first polysilicon and the buried-contact mask levels. Specifically, there is a high probability of short circuits from word lines to cell nodes. A shorted resistive word-line will be "stuck" either high or low, causing a row failure that could be corrected by deselecting that row and enabling a spare one.

Furthermore, double-polysilicon structures often have a topography-related problem wherever two strips of the second polysilicon level cross a first-polysilicon-level line. With conventional etchants there is a significant statistical probability that they will leave a "stick" of polysilicon along the first-level line, producing a short between the two second-level elements. In a static random-access memory cell, this fault can cause correctable row failures by shorting V_{cc} and word lines to cell nodes. In general, rows are more likely to fail than columns with the double-polysilicon cell. Therefore, redundant rows would enhance the yield most—but at a significant penalty in performance, as will later be demonstrated.

In contrast, yields are inherently higher for a single-polysilicon-level static RAM cell, because fewer masks are required. Any random defects will cause single-bit or column failures more often than row failures, because this cell layout requires tighter metal and metal-silicon contact rules than polysilicon and buried-contact rules. The dominant column failure modes are shorts from bit lines to cell nodes or V_{cc} lines.

It is often the case that a given defect will span the boundary of two or more memory elements (rows or



1. Bigger but better. The single-polysilicon-level cell used in the IMS1400 series of static random-access memories is slightly larger than a double-polysilicon design. However, it allows column instead of row redundancy, which preserves the device's high speed.

TABLE 1: DEFECT SIZES FOR ROW FAILURES (THREE CRITICAL MASKS)

Type of defect	Defect size (μm)		
	One row	Two rows	Three rows
Holes in gate oxide (buried contact mask)	minimum	6.0	68.0
Holes in interlevel oxide (contact mask)	minimum	minimum	38.5
Missing polysilicon	2.7	9.5	72.5
Extra polysilicon	2.25	3.7	67.5

TABLE 2: DEFECT SIZES FOR COLUMN FAILURES (SEVEN CRITICAL MASKS)

Defect	Defect size (μm)		
	One column	Two columns	Three columns
Holes in field oxide (active area mask)	2.7	2.7	20.7
Extra source-voltage (V_{SS}) implant	minimum	2.7	20.7
Extra depletion implant	1.4	2.7	20.7
Holes in gate oxide (buried contact mask)	1.4	2.7	20.7
Holes in interlevel oxide (contact mask)	minimum	5.4	23.2
Missing polysilicon	1.4	2.7	20.7
Extra polysilicon	2.7	2.7	21.6
Missing metal	2.7	11.0	28.7
Extra metal	3.6	3.6	22.4

columns). For example, shorts between neighboring bit lines may cause two adjacent columns to fail. Designs that incorporate redundancy by dedicating one spare element to each half of the memory array do not allow for the correction of such faults.

Other defect mechanisms can cause shorts between bit and word lines. Such defects are generally not correctable because of the partial selection of unrelated memory cells. Proper cell layout minimizes the likelihood of such defects.

Bigger may be better

When a cell is laid out to meet redundancy requirements, it may take up extra space. A case in point is the single-polysilicon static RAM cell used in the IMS1400, 1420 and 1421 16-K static RAMs (Fig. 1). A double-polysilicon cell designed with the same layout rules is approximately 6% smaller. But the yield penalties due to the need for additional masking levels and the problems of step-coverage and related wafer-topography difficulties more than offset this benefit. Yield may, in effect, be further reduced with a double-polysilicon cell because the corrected devices are slower—the circuit requirements for row redundancy introduce delays.

If relaxation of a particular layout ground rule can significantly reduce the probability of an uncorrectable failure, these yield improvements may be well worth the somewhat increased chip size.

The preliminary evaluation discussed above can be quantified with reasonable accuracy by characterizing the failure modes of each mask level with respect to the cell layout. This is done in Tables 1 and 2 for the cell of Fig. 1. Each mask level may suffer from three types of defects—pin holes, extra features and missing features. With alignment tolerances, layout rules and technology nuances borne carefully in mind, each type of defect is evaluated to determine whether it could cause row, column, or single-bit failures.

Once each type of defect is categorized in this fashion, it is possible to determine the minimum size of defect that would cause the failure of one memory element (row or column), two memory elements, three memory elements, and so on. When the defect size required to cause N memory elements to fail is much larger than that required to cause N – 1 memory elements to fail, a point of diminishing returns has been identified.

From this analysis, several key observations can be made. Specifically, for the single-polysilicon cell cited in Tables 1 and 2, it turns out that there are four ways that rows can fail, but nine ways that columns can be defective. Column failures involve seven critical masks versus three for row failures, the minimum size of a defect necessary to cause a dual-column failure is less than half that required to cause a dual-row failure, and a defect capable of disabling three rows or columns is obviously much larger than one that is capable of disabling two rows or two columns.

Evidently, then, row failures are much less likely than column failures, so that column redundancy will benefit the yield the most. Furthermore, two redundant columns will benefit the yield quite significantly, whereas more than two columns may provide only marginal further improvement.

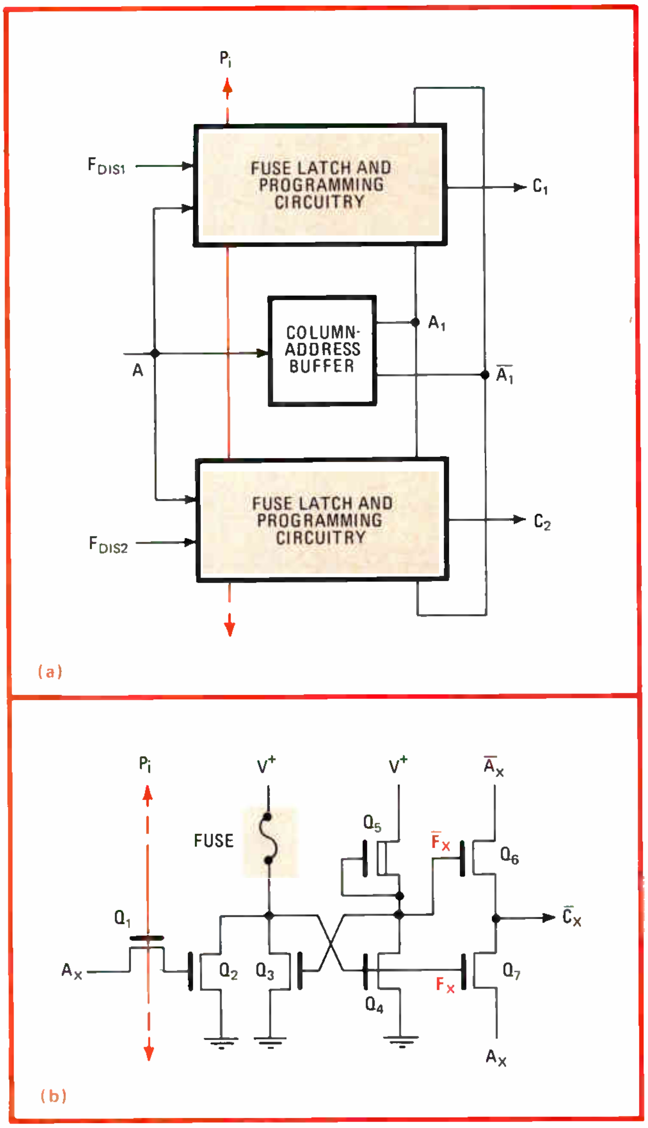
Fatal flaws

It is necessary to remember that not every type of defect can be corrected by multiple word-line or bit-line redundancy. Faults in clocks, input and output buffers, and power supply lines are generally difficult or impossible to repair since they will often create a power-supply short. Memory cells having no power supply lines to

TABLE 3: FAILURE PROBABILITIES FOR ROWS VERSUS COLUMNS

Probability[a]	Row, P_r	Column, P_c
Correctable	0.0654	0.342
Noncorrectable	0.0665	0.05
P_c/P_r (correctable) = 5.25		

[a] $P = 1 - e^{-(D_1A_{1c} + D_2A_{2c} + \cdots D_nA_{nc})}$ where D varies with mask level



2. Latch advantages. Each column-address buffer has two programmable latches (a), the circuit details of which are shown in (b). The fuse is embedded in a regenerative latch circuit that relaxes the requirements of the fuse's blown and unblown resistances.

individual cells, such as one-transistor dynamic RAM cells, will have a higher percentage of repairable array defects than dc-powered static RAM cells. Neglecting noncorrectable array defects, the ratio of noncorrectable to correctable faults is directly determined by the ratio of peripheral circuitry area to array area.

For the single-polysilicon static RAM cell, shorts between polysilicon and n^+ regions or between polysilicon and metal will cause word-to-bit-line shorts or shorts between V_{cc} and V_{ss} (ground). Both are fatal chip defects. The first will cause data disturbance problems, and the second will result in excessive power supply currents. Word-line breaks are also not repairable for the former reason, but these can be made correctable by holding off both ends of the word line with a high-valued resistor or active circuitry. Substrate-related defects are generally not correctable on chips with bias generators because of the latter's limited current capability.

Once the noncorrectable failure modes have been identified, they must be factored out of the analysis for determining the optimal type of redundancy. If the critical areas of the cell sensitive to noncorrectable defects add up to a significant fraction of the total cell area, a reconsideration of the cell design may be in order. For the remaining correctable defect types found in the analysis, the critical cell areas sensitive to each type of fault must be evaluated.

Failure probability

To calculate the probability of a row or column failure, the defect density characteristics of each relevant masking level must be observed in relation to critical chip areas. If defect monitor data is unavailable, it can be assumed that the defect density D is inversely proportional to the cube of the defect size.

The sum of these scaled critical areas for row and column failures can be used to calculate the failure probabilities for different representative defect densities by assuming a simple Poisson distribution of defects:

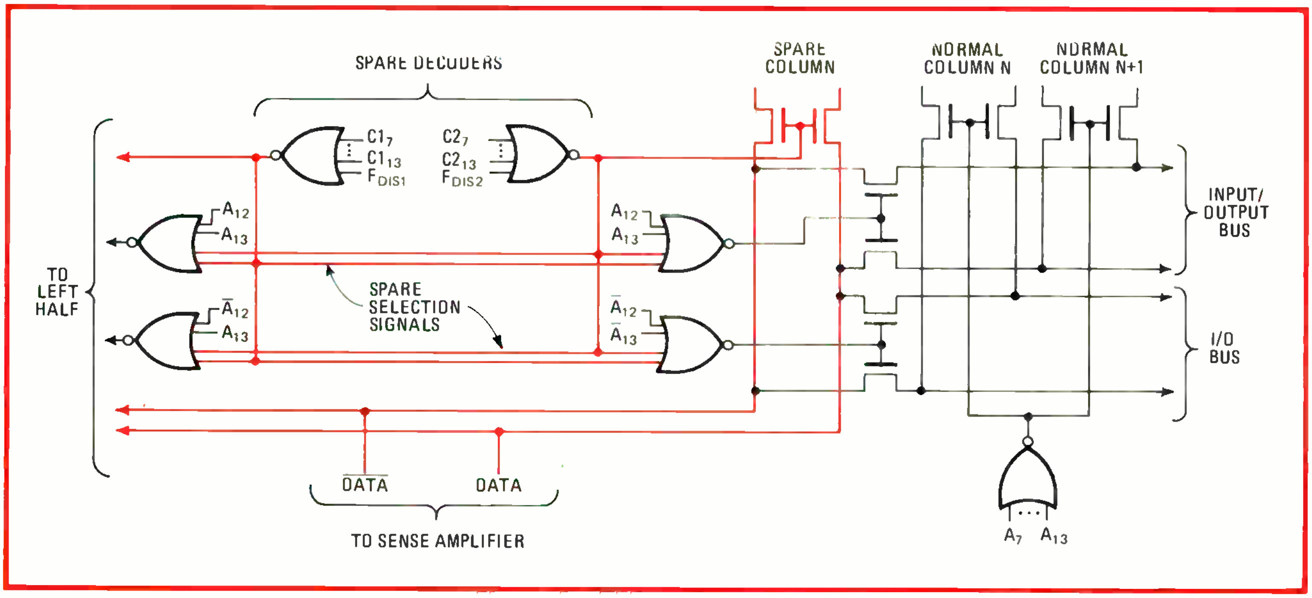
$$P_f = 1 - e^{-\Sigma DA_c}$$

where A_c is the total normalized critical area, P_f is the probability of a failure, and D is the defect density. As shown in Table 3, the predicted ratio of correctable column to row failures is 5.25. Wafer-probe test data from multiple production lots shows this ratio to be between 5 and 7 for the IMS1400 16-K static RAM—surprisingly close to that predicted by the simple analysis described above.

How many spares?

Once the relative probabilities of row and column failures have been estimated, a simple statistical analysis may be used to determine the optimal numbers of each type of spare element. As the number of spares is increased, the probability that one of them will fail also increases, not to mention the possible failure of the overhead peripheral circuitry that each spare element requires to be activated. As this overhead is not in itself repairable, a point will eventually be reached where the number of good dice per wafer starts decreasing because of the increased die area, the reduced number of dice per wafer, and the increased probability of irreparable defects in the peripheral circuitry.

Yield may be defined as the probability that a given area of the chip is free of defects. The total chip yield can then be expressed as the product of the probabilities of the array and the periphery being free of defects. Redundancy improves the array yield but reduces the periphery yield. Mathematically, the yield of a memory



3. Spare enable. The fuse latches of Fig. 2 feed the spare decoders above. A key feature of column redundancy is that the decoders need not be disabled to disconnect the regular columns from the normal data path—only the regular input/output buses must be isolated.

array with redundancy may be expressed as an additive probability—the probability that the entire array is defect-free plus the probability that if some fraction of the array is defective, the pattern of failures can be fixed with the available redundant elements.

The probability that all of the defective bits can be repaired is the sum of the probabilities of repair for all possible cases. For example, the IMS1400 16-K static RAM uses two redundant columns in addition to the 128 normal columns. Array yield in this case is the probability of finding 128 good columns, plus the probability that 1 normal column is bad and 1 spare is good, plus the probability that 2 columns are bad and both of the spares are good.

Using the Poisson distribution equation given on p. 118, this compound probability may be expressed as:

$$Y_{array} = \sum_{i=0}^{n} \binom{m}{m-i} P_E^{m-i} \cdot (1 - P_E)^i \cdot P_E^i$$

where m is the number of normal memory elements and n is the number of spare memory elements. Thus, for the IMS1400, this becomes:

$$Y_{array} = \binom{128}{128} P_E^{128} \cdot (1-P_E)^0 \cdot P_E^0 + \binom{128}{127} P_E^{127} \cdot (1-P_E)^1 \cdot P_E^1 + \binom{128}{126} P_E^{126} \cdot (1-P_E)^2 \cdot P_E^2$$

The yield improvement factor—the ratio of the yield with redundancy to that without redundancy—can be plotted as a function of the yield without redundancy for different numbers of spare elements. As more spares are added, these curves generally merge and eventually cross, showing that the point of diminishing returns is being approached and that further increases in the number of spare elements will start reducing the yield improvement factor.

The final choice of the optimal number of spare elements must include other considerations—the number of programming elements required, testing time, packaging constraints, and the possibility of faults that span the boundary of adjacent elements.

Programming elements

On-chip storage of the information that identifies the defective bit locations is a key issue in redundancy. The programming elements used for this purpose fall into two categories: the laser-programmable and the electrically programmable.

Laser-programmable elements occupy less chip area and do not normally affect circuit performance, but they do require special test equipment and increased wafer handling and testing time. Also, the laser spot size and beam-positioning requirements will become more stringent in future memories with ever finer line widths.

Electrical programming is done with standard test equipment, which is the main reason for its popularity among commercial semiconductor houses. Polysilicon fuses of the bipolar programmable read-only memory type are the most widely used elements because of their proven reliability. Usually a hole is cut in the passivation glass over such fuses to reduce the amount of programming current needed. The possibility of mobile-ion contamination of active circuit areas can be eliminated with guard-ring structures surrounding the fuse area or with other techniques.

The area and performance penalties of electrically programmable fuses can be minimized by careful circuit design. The number of fuses required is determined by the number of redundant blocks used. If 2^K is the number of regular element blocks, then each redundant block requires a minimum of K+1 fuses. In general, the cost-effectiveness of laser programming increases with the number of redundant blocks.

Fuse and compare

Polysilicon fuses are electrically blown open on the IMS1400 family of 16-K static RAMs in the course of wafer-probe testing. Electrical programming is used because the number of fuses required is not large enough to offset the negative aspects of laser programming. Figures 2a and 2b show, respectively, the circuitry that stores the address of a faulty element on the memory chip and that employed to compare the incoming address with the stored address.

Each column-address buffer has two fuse latches, which are enabled by programming pads. The address of the defective column is permanently programmed into the fuse latches by applying that address on input pads and enabling either one of the programming pads. This causes transfer gates such as Q_1 to transmit the defective address information to programming transistors like Q_2.

When the address pad is driven high during wafer probe testing, Q_2 will sink current through the polysilicon fuse and cause it to open, increasing its resistance from 100 to 300 ohms to greater than 25 megohms. If the fuse is not blown, the latch constituted by transistors Q_3, Q_4, and Q_5—and the fuse—are designed to power-up such that the fuse signal, F_X, is high while its complement, F_X, stays low. The opposite is true when the fuse is blown open to a high resistance.

The regenerative nature of a latch-type fuse-detection circuit offers significant advantages over other approaches. Although the fuse's resistance is increased from less than 300 Ω to about 25 MΩ, the fuse latch operates properly with any values less than 10 kilohms and greater than 30 kΩ for the fuse's unblown and blown states, respectively. The circuit in effect multiplies fuse reliability and repair yield by being able to tolerate large variations in blown and unblown fuse resistances. In addition, this circuit has only one power-consuming stage with an unblown fuse.

Transistors Q_6 and Q_7 in Fig. 2b, connected so as to implement an exclusive-NOR function, compare incoming addresses with the bad addresses stored in the fuse latches. If an incoming address bit matches the fuse data, the corresponding compare line, such as $\bar{C}_7$, goes low. When all seven compare lines go low, a spare decoder is enabled while the normal access path is cut off. Signals F_{DIS1} and F_{DIS2} keep spare decoders disabled if no repair is required.

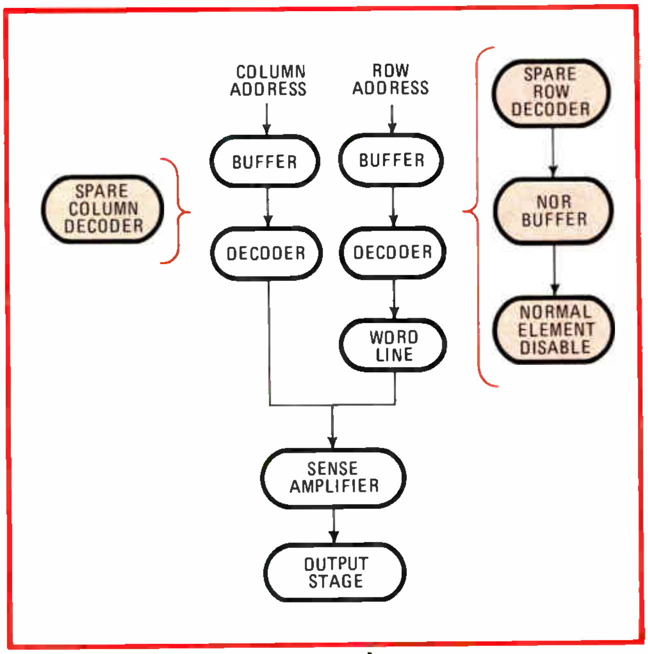
Intel, Mostek, Hitachi, and TI use double-polysilicon cells for their fast static RAMs because of their smaller size compared with single-polysilicon structures. Two have column redundancy, one has row redundancy, and one has no redundancy.

As shown earlier, a double-polysilicon static RAM will normally require row redundancy to improve yield. Because of requirements for high speed, actual yield improvement may be questionable on a memory chip that incorporates double-polysilicon cells and column redundancy. On the other hand, row redundancy will improve functional yield, but could degrade speed enough to defeat the very performance goals that the chip was designed to meet.

Row replacement

Replacement of a defective row involves disconnecting that row from its access circuitry and enabling a spare. Therefore, an additional transistor, driven by a common disable line, is necessary in every row decoder. The common normal-element-disable (NED) line must be taken high every time a spare row is selected to disable the regular row decoders. As such, the NED clock driver must be driven by a NOR buffer with the spare select signals as its inputs.

When a spare row is selected, the regular rows are disabled two buffer delays later. Provided the access time is not pushed out in turning off the regular rows—a process that includes a polysilicon word-line delay—and provided the transfer-gate delay in the comparison circuitry is minimal, the regular-to-spare access time will not be significantly different from a normal row-access time. However, the "spare-to-regular" access path is the

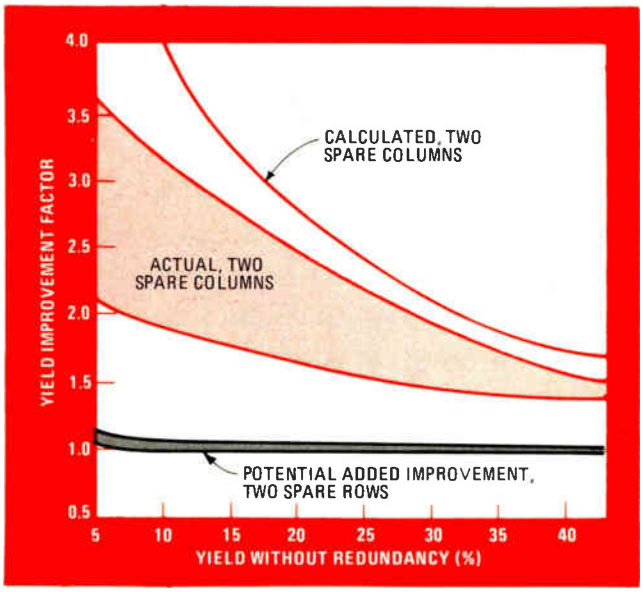


4. Critical timing. The center paths illustrate how column and row addresses are processed in an ordinary static RAM without redundancy. Row redundancy adds three delays but column redundancy adds only one and there is time enough to hide it.

slowest. Before the regular decoder output can go high, three events must occur: the spare decoder output must go low, then the NOR buffer output will go high and, finally, the NED driver will turn off to release the regular row decoder. Assuming a typical delay of 3.5 ns per buffer, row redundancy could add as much as 10.5 nanoseconds to the worst-case access time.

A key feature of column redundancy is that the decoders need not be disabled in order to disconnect the regular columns from the normal data path. As shown in Fig. 3, only the regular input/output buses must be isolated from the data bus. If, as in the IMS1400, a two-stage interleaved column decoding scheme is used with a one-of-four final decoding stage, isolation of the I/O buses can be achieved with the addition of a few extra transistors to each of the four second-stage column decoders. These transistors can be driven directly by the spare selection signals because of their low capacitive loading. Consequently, disabling the normal access path is accomplished swiftly as the spare selection signals begin to rise. The voltage on the I/O bus's isolation gates must get down only to a threshold voltage below V_{cc} to switch them off rapidly because of the relatively high common-mode voltage levels of the data buses. In contrast, to disable a normal row in the case of row redundancy, the word line must go almost to ground potential. The slow discharge of the word line is an additional limiting factor.

More importantly, as shown in Fig. 4, the spare-to-regular access path suffers only one buffer delay with column redundancy—the turn-off of the spare decoder—before one of the second-stage column decoders can be enabled. This extends the normal column access time slightly, but this access path is still significantly faster than the overall row access time. The area penalty of this column redundancy scheme is negligible since the disable function requires the addition of only a few transistors to the existing second-stage column decoders. Furthermore, the spare columns are conveniently placed between the two main column decoder arrays, in an area normally wasted in conventional memory designs due to the complex routing of address, data and control lines.



5. Calculated and actual. A simple, random-defect model was used for the calculated curve, and wafer-probe tests provided the data for the yield improvement with two spare columns. A simple statistical analysis supplied a reasonable approximation to the actual yield.

Since speed is a primary consideration in MOS RAMs designed to compete with bipolar memories, a single-polysilicon-level memory cell was chosen for the IMS1400 family despite a 4% die-size tradeoff. The design takes full advantage of column redundancy to boost yield without compromising performance.

Theory and practice

For redundancy to improve yields, the spare elements must consume a minimal amount of chip area. The IMS1400 16-K-by-1-bit static RAM uses two spare columns and associated circuitry that consume only 2% of the total chip area. The redundancy does not affect circuit speed and the chip power is not appreciably increased. The IMS1420/1421 4-K-by 4-bit static RAM uses two blocks of four spare columns and associated circuitry that consume 4% of the total chip area and, as in the IMS1400, do not affect the performance.

Production test results for the IMS1400 prove that redundancy greatly improves yield without degrading performance. The graph in Fig. 5 shows the calculated and actual yield improvement factors as a function of yield without redundancy. The calculated curve was obtained from a simple random defect analysis, and the data for yield improvement with two spare columns was taken from the results of wafer-probe tests of production wafers. The bottom curve, representing the additional yield improvement if two spare rows were to be added to the chip, is based on data obtained with a test program that screened for chips with one or two defective rows.

The reduction in actual yield improvement from the calculated values is due to noncorrectable defects and departures from a random defect distribution, neither of which were accounted for in the statistical analysis. As this graph illustrates, a simple statistical analysis provides a reasonable approximation to the actual yield.

Several conclusions can be drawn from the data. Although less than calculated, the yield improvement factor with two spare columns ranges from 1.5 to 3.5 for reasonable yields. One argument against redundancy has been that for the high yields characteristic of mature products, redundancy may be useless or even detrimental. The data shows, however, that even yields as high as 40% without redundancy are increased to 60% after repair. It also confirms that columns will fail more often than rows on this chip and that further increases in the yield with two spare rows would be negligible. □

Equipping a line of memories with spare cells

The best spare-bit implementation depends on whether a memory is read/write or erasable read-only and whether its data is bit- or byte-wide

by Robert Abbott, Kim Kokkonen, Roger I. Kung, and Ronald J. Smith, *Intel Corp., Santa Clara, Calif., and Aloha, Ore.*

☐ The world demand for memory bits continues to double roughly every year; by 1985 the total could exceed 50 trillion bits. Technological innovations like single-transistor storage cells have so far enabled the industry to keep pace with this voracious appetite. But by now component-level measures for increasing chip density are drying up.

To compensate for this, companies are adding to their fabrication capacity, even though increased investment in production plants is distinctly unattractive. A new factory with a capacity of 10,000 wafer starts per week currently costs over $50 million and takes about three years to complete.

On-chip redundancy brings the industry's attention back to the component level, where it belongs, and significantly enhances the productivity of existing fabrication facilities. Larger dice—incorporating redundancy—can actually cost less overall than smaller chips without the feature. Indeed, the larger memory cell allowed by redundancy also translates into more stored charge—and more substantial signals in turn mean a reduced soft-error rate and improved operating margins.

Across the board

Intel manufactures a wide variety of memory components, including static and dynamic random-access memories, erasable programmable read-only memories, and electrically erasable PROMs. The static RAMs will be available in 1-bit and 8-bit organizations, and the dynamic memories—in the form of self-refreshing units for microprocessor systems—will also be offered in byte-wide packages. At some point in the future, all of these product types will incorporate redundant elements. A unified effort to make this happen has involved a considerable number of tradeoffs.

The inefficiencies apparent with individual spare bits and clusters of bits led to a decision to provide redundant columns and rows. The number of each is subject to several considerations since spare cells in any form inflate die size and reduce the number of chips per wafer. Furthermore, each spare element demands extra support circuitry—which cannot be repaired—so too much redundancy reduces overall repair efficiency.

A large number of spare elements is needed to counter a high defect density, but as processing improvements reduce the number of defects over time, the optimum number of spare elements likewise declines. The net conclusion was the decision to equip the 2164 64-K RAM with four spare rows and four spare columns, increasing its die size by 7.5%. The 2167 16-K static RAM has only three spare rows, for a 6% greater area.

On the 16-K static RAM, spare rows resulted in twice the yield improvement that spare columns would have

FAILURE MECHANISM VERSUS TYPE OF DEFECT AND STORAGE CELL IN A DYNAMIC RANDOM-ACCESS MEMORY

Type of defect	Metal bit line			Diffused bit line		
	Failure mechanism	Redundancy		Failure mechanism	Redundancy	
		Row	Column		Row	Column
Diffusion short	single bit, double bit	•	•	single bit, double bit	•	•
Diffusion break	single bit	•	•	single bit, column		•
Polysilicon short	adjacent rows	•		rows	•	
Polysilicon break	row	•		single bit or double bit	•	•
Closed contact	double bit		•	double bit	•	
Blown contact	row and column	•	•	adjacent rows	•	
Metal short	adjacent column		•	adjacent rows	•	
Metal break	column		•	row	•	
First gate short	single bit	•	•	single bit	•	•
Second gate short	row, single bit	•		row, single bit	•	
Short between two polysilicon levels	row	•		row	•	
Cell leakage	single-bit refresh	•	•	single-bit refresh	•	•

provided. However, performance had also to be considered. Column redundancy does not degrade access time because decoding is carried out in parallel with other internal operations such as multiplexing. Row redundancy does add one 3- to 5-nanosecond stage delay as the decision to use an original or a replacement row is made. In most cases, though, this delay is insignificant; it hardly matters on a current 64-K RAM, which has an access time in the 150-ns range. Furthermore, tests on the 2167 16-K static RAM prove that fast, 55-ns access times are possible with or without row redundancy.

Defects versus fixes

As with static RAMs, the distribution of failures on dynamic RAMs is a function of the manufacturing process used and the aggressiveness of the design. The table lists various dynamic RAM defects, the failures that result, and the form of redundancy most appropriate for their repair. The actual distribution of defect types determines the number of spare rows and columns that should be used.

A major concern with dynamic memories is their sensitivity to sense amplifier or bit line imbalance. Any of a number of defect types may result in sense amplifier imbalance; hence, dynamic RAMs with redundancy should include some spare columns, if possible.

Many of the defects possible cause single-bit failures that can be corrected either with spare rows or with spare columns. Thus, there is not necessarily an ideal distribution of spare rows versus spare columns. The optimum number of redundant elements on a dynamic RAM is more than simply the number of defects. For example, metal bridging may cause adjacent columns to fail, requiring two spare columns. An over-etched contact may short a bit line to a word line, requiring a spare row and column. A sufficient number of spare elements is required for these types of defects.

The implementation of redundancy on dynamic RAMs may affect the chip's architecture in many ways. For example, word-line clamps are necessary on both ends of the line to prevent a nonselected or broken word line from floating. Also, it is useful to keep the number of input/output lines to a minimum, since to switch a single redundant column among multiple I/O lines requires an extra pair of column-selection devices for each pair of I/O lines, complicating the layout.

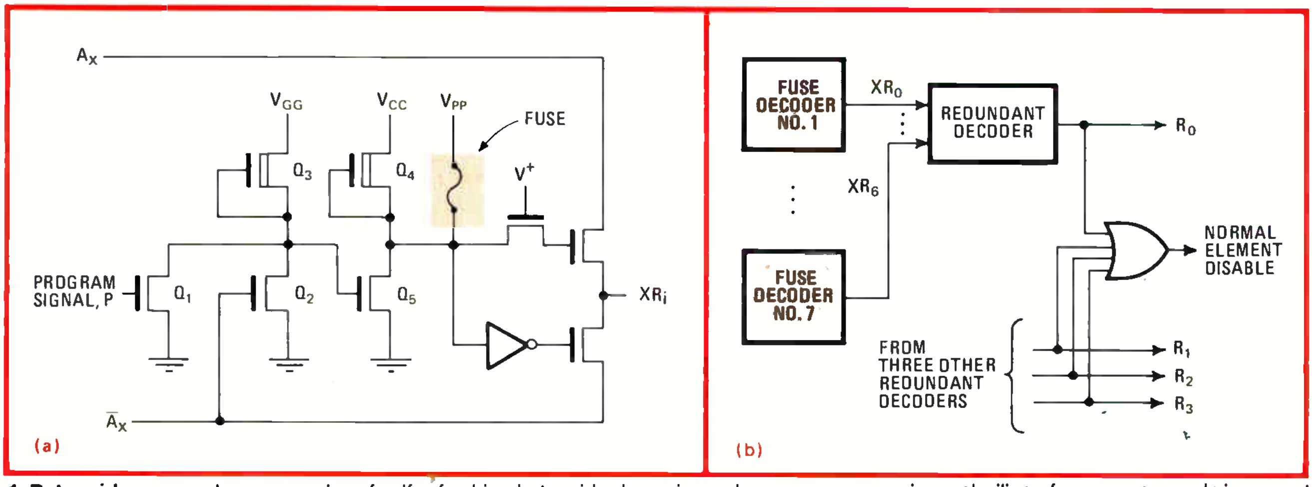
Byte-wide needs

Byte-wide memories call for unique design considerations not encountered with static or dynamic RAMs. Speed is not as critical as with bit-wide static devices, for instance, because byte-wide units are primarily intended for MOS microprocessor environments.

The redundancy on some of Intel's latest byte-wide memories does, however, involve some of the same considerations as conventional dynamic RAMs. These are called integrated, or IRAMs, since they surround a dynamic array with peripheral circuits for automatic refreshing and access arbitration to make the device appear static. (Similar devices from other makers are called pseudostatic or quasi-static RAMs.)

So far, two IRAMs have been announced: a 4-K-by-8-bit memory called the 21821, and an 8-K-byte part, the 21834. These, by virtue of their byte-wide data, necessitate eight I/O line pairs. Thus, unlike the case of an ordinary dynamic RAM, the number of I/O pairs cannot be further minimized.

Yield data suggests that it would be worthwhile to include column redundancy on a by-8-bit memory, but its use should still be limited because of the difficulty in multiplexing a redundant column between the multiple I/O lines. So the 32-K IRAM uses row redundancy only and, although the 64-K IRAM incorporates both spare rows and columns, it is assumed that most all defects can be handled with the redundant rows; the spare columns are used only as a last resort.



1. Byte-wide spares. In a new series of self-refreshing byte-wide dynamic random-access memories, polysilicon fuses are opened via current pulses as in (a). Each of four redundant decoders (b) contains eight fuses, one of which generates a validity signal.

The 32-K IRAM integrates eight redundant rows, four for each half of the array. The polysilicon fuses are opened by current pulses as shown in Fig. 1a. Transistor Q_5 sinks the programming current, which is controlled by voltages V_{GG} and V_{PP}. Transistors Q_1 and Q_2 comprise a NOR-type decoder that determines which fuses will be programmed. The remaining circuitry senses the status of the fuse and routes either an address or its complement to the XR_i line.

Figure 1b provides a block diagram of the overall byte-wide scheme. Each of the four redundant decoders contains eight fuses, one of which generates a validity signal called RDS that is asserted when that element has been programmed. The other seven fuses make up the redundant address.

If the seven row addresses coincide with the (programmed) address of a defective row, the redundant address decoder will generate an output signal for two purposes—to select an appropriate redundant word line and to disable the normal word line.

Enabling a row

Figure 2 indicates how a spare row is enabled on both the 2167 and 2164 by-1-bit memories. After buffering, all addresses and their complements are routed both to programming elements and to the chip's normal NOR-type decoder. If no fuses are blown, a unique address activates a single normal decoder, which in turn enables a row of cells. In this case, the spare row-enable signal is held high to ensure that the output of the spare decoder always remains low.

If, however, a faulty cell is discovered during wafer probing, the programming elements are encoded to recognize the address of its row and activate a spare instead. The spare row-enable signal is programmed low, so that when the bad address is reached, all of the inputs to the redundant decoder will be low. At this point, the decoder's output will rise and enable a redundant row.

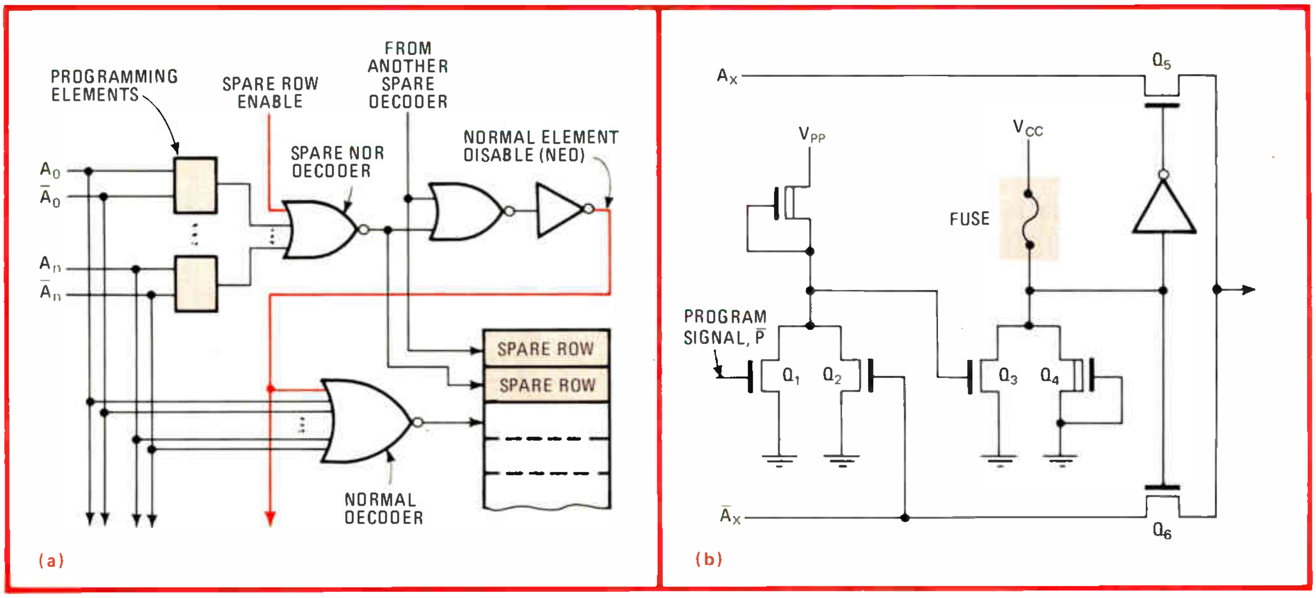
In addition, for the 2167, when any spare row is selected, a normal-element–disable (NED) signal rises as well. The NED line is fed to all of the NOR gates of the standard decoder, just as though it were another address line. This keeps all of the normal rows shut off when a redundant row is selected to avoid any possibility of incorrect data leaving the chip.

A defective address is encoded into the programming elements by instructing them to pass either an address or its complement. As shown in Fig. 2b, the instruction is based upon the status of the fuse.

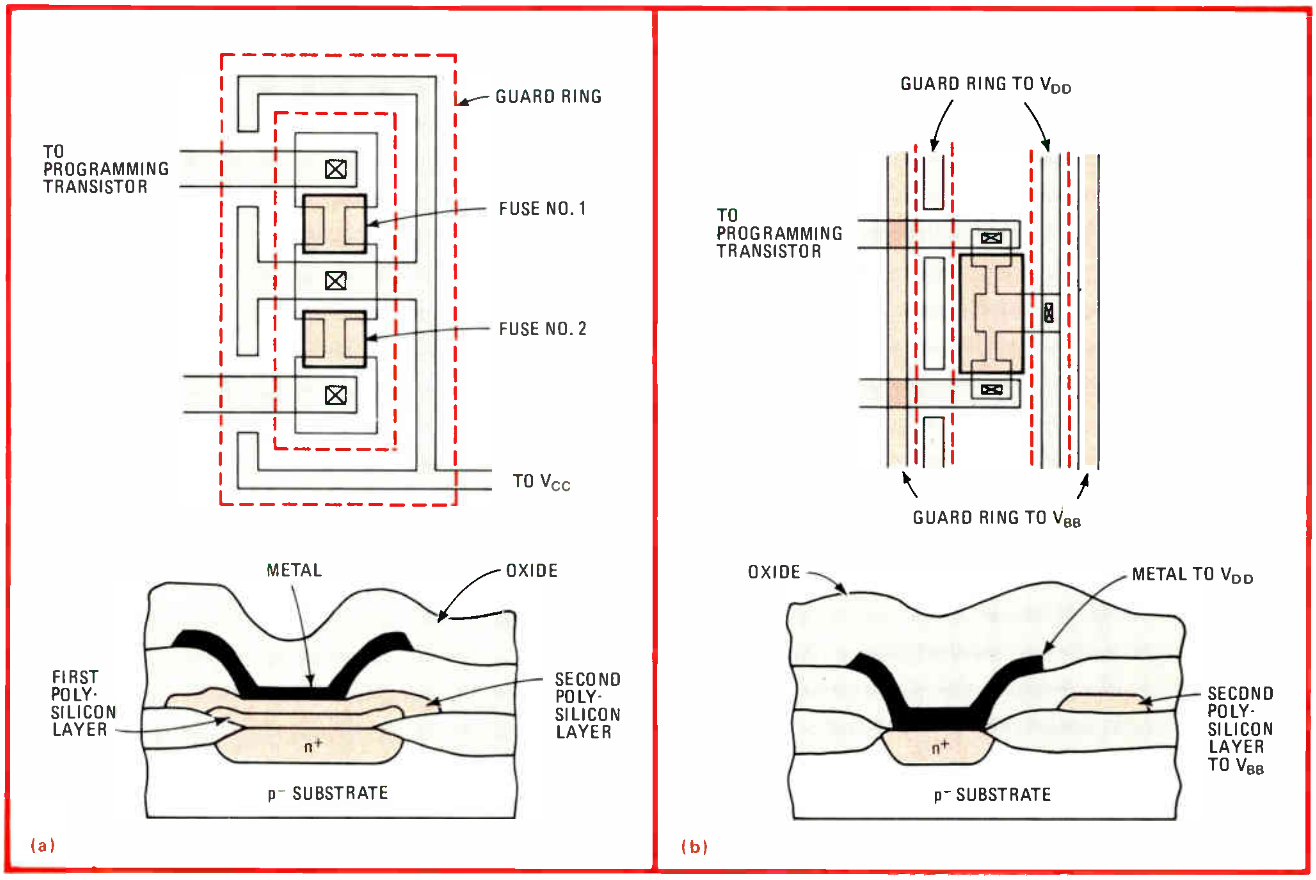
When the circuit's fuse is to be blown, the process starts by lowering the circuit's programming signal, $\overline{P}$. The address complement signal, $\overline{A}_x$, is also held down so that the programming voltage, V_{pp}, is allowed to reach the gate of the programming transistor, Q_3. A high current flows through the fuse and it opens. Depletion-mode transistor Q_4 is now allowed to ground the gate of Q_6 and present the inverter with a low input signal. The inverter turns on Q_5 and the address is passed to the output. Had it been required to leave this particular element's fuse intact, V_{cc} would appear on the gate of Q_6, passing the address's complement to the output instead.

The high-level programming voltage is used only to blow a fuse. An extra pad is provided so that this voltage may be applied while the wafer is being probed. This pad is not bonded out to package pins and the signal is held low internally after testing to prevent any inadvertent programming after probing the wafer.

The major advantage of electrical fuse blowing is that



2. Reroute. When a faulty location is reached on the 2167 16-K static or 2164 64-K dynamic RAMs, a normal-element–disable signal ensures that only spare cells are selected (a). As with byte-wide parts, electrical fuses store the bad addresses (b).



3. On guard. Holes are left in the passivation layer over the fuses. In order to guarantee that contaminants do not interfere with memory operation, guard ring structures are employed on the 2167 RAM (a) and the 2164 RAM (b). The chips prove to be completely protected.

the redundancy can be implemented with minimal initial capital expenditures and that existing test equipment may be used. In the future, electrical fuses could conceivably be blown inside the memory's package, opening up the possibility of field repair.

Careful aiming

Laser programming presents the obvious advantage of conserving valuable silicon real estate by eliminating the circuitry associated with blowing electrical fuses. On the other hand, precise alignment of the laser beam is required. If accurate alignment can be achieved in production, reliable, well-controlled burns will result; but decreasing line widths are likely to exacerbate future laser-positioning difficulties. Lasers may, however, allow a wider choice of potential fuse materials—Bell Laboratories has already disclosed the use of tantalum silicide for this purpose.

Tradeoffs between ease of design implementation, up-front capital investment, and final product cost determine whether laser or electrical programming is best for a particular memory product. By managing these trade-offs properly and by understanding the capabilities of the two technologies, an optimum combination of techniques can be applied to a comprehensive memory product line.

Comparison testing of redundant and nonredundant integrated circuits led to two major observations. First, holes in the passivation layer over the fuses to facilitate programming are potential entry points for contamination. Once on the surface, contaminants might spread to adjacent circuitry through the break in the fuse's metal guard ring, which is necessary for the interconnection of the fuse and its programming transistor (Fig. 3). However, deliberate sodium contamination and baking show that the 2164 and 2167 are completely protected by the guard ring structures used.

Secondly, no new failure mechanisms were found to be introduced by incorporating redundancy, so that standard reliability stress techniques could still be employed. Moreover, since most induced failures can be corrected with spare elements, stringent testing and stressing are more cost-effective on redundant arrays. It has been shown that overstressing is a dependable method of catching latent defects and enhancing component reliability. Consequently, the reliability of redundant parts can be made at least equivalent to that of their nonredundant counterparts. □

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Using a laser beam to substitute good cells for bad

The circuit design flexibility possible with the laser approach puts it in strong competition with electrical fuses

by R. T. Smith, *Bell Laboratories, Allentown, Pa.*

☐ The dust has long since settled in the debate whether, for very large-scale integrated memory design, the redundancy so necessary for decent yields is acceptable to users and economically affordable by makers. At what level of integration all this becomes true is, perhaps, still arguable; but in a cost war a 64-K dynamic random-access memory without redundancy stands little chance of even coming close to competing with 64-K designs incorporating the feature.

The benefits of redundancy may be quantified in terms of a yield improvement factor, defined as the ratio of all functional chips—including those that have had bad bits replaced with spares—to the number of devices that did not require redundancy programming. Yield improvement factors for the 64-K chip span an order of magnitude, from 30 on early prototypes down to 2 for very high-yielding wafer lots. Actually, factors of 3 to 5 are more representative of mature production runs.

What is still being debated, however, is which of the two principal competing redundancy technologies—laser programming or electrically fused links—will dominate. Industry speculation indicates that even those manufacturers now publicly committed to electrically fusible links are more than seriously considering laser programming. Why this is so can be seen from Table 1.

In the design of Bell Laboratories' 64-K RAM four years ago (Table 2), an acceptable and cost-effective means of implementing redundancy without sacrificing either performance or reliability was the paramount goal. The lack of optimized equipment, coupled with a large software development project, were quickly accepted as necessary evils by the design team.

Today, laser systems tailored for VLSI personalization are readily available, having evolved considerably in the interim. Although fully integrated laser programming and testing systems have yet to appear, one equipment manufacturer makes both of the major parts. Still, since most VLSI memory producers prefer their own particular flavor of tester anyway, what is really needed now is a well-defined high-speed communications link between the laser system and tester.

The reward

The higher equipment cost of the laser approach should be viewed in context with proven device production and cost-recovery improvements. At the 1981 International Solid State Circuits Conference, Bell Labs claimed that a $0.3 million capital investment in a laser-based programming system could be recovered in 7 to 13 weeks of moderate production of devices in the 30-to-40-square-millimeter (46,500 to 62,000 square mils) size range. Because of productivity and throughput improvements, the current recovery period is now less than two weeks, according to Western Electric Co. in Allentown, Pa.

The software development costs are formidable whether laser links or electrical fuses are used—the test and

TABLE 1: A COMPARISON BETWEEN LASER PROGRAMMING AND ELECTRICALLY FUSIBLE LINKS

Feature	Laser approach	Electrical fuses
Circuit layout	Links may be placed anywhere	Links must be accessible to external drivers via bonding pads or additional on-chip circuitry
Performance	Access times of programmed and nonprogrammed devices are indistinguishable	Speed is generally adversely affected, particularly if both row and column redundancy are used
Reliability	Since exploded links are covered with final nitride passivation layer, reliability is extremely high	High reliability requires guard rings around link regions
Area penalty	Area increase for redundancy is slight—increases will scale down with finer design rules in future devices	Area increase is also slight, but may not scale down as easily because of layout and reliability concerns
Flexibility	Performance margins are easily tailored with "quick fixes"	Layout is not adaptable to unforeseen circuit needs
Equipment costs	Software development requirements and hence costs are large	Initial costs are lower due to relaxed software demands

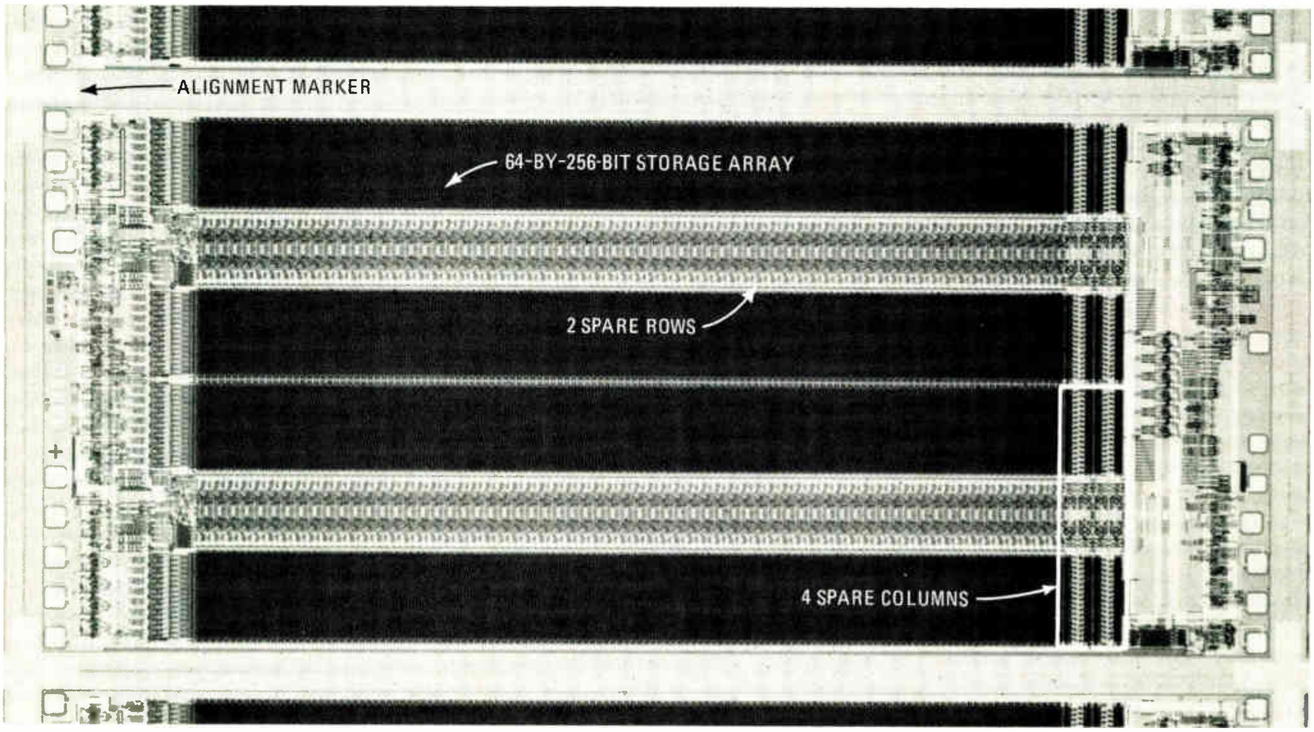
TABLE 2: CHRONOLOGY OF LASER PROGRAMMING DEVELOPMENTS AT BELL LABS	
Date	Action taken
July, 1977	Decision made to incorporate laser-programmable redundancy on 64-K dynamic random-access memory
September, 1977	Commercially available laser system ordered; hardware modifications to general-purpose test system initiated; preliminary design rules for laser target established
January, 1978	Laser delivered; link design rules refined
July, 1978	First 64-K chip programmed (off line, replacing 2 rows and 1 column)
December, 1978	Laser test system integrated; closed-loop testing, diagnosis, and laser-programming attempted
February, 1979	64-K RAMs with redundancy announced at the International Solid State Circuits Conference; laser programming illustrated with filmstrip
July, 1979	Automatic fine alignment added to laser system; first on-line production system installed at Western Electric
October, 1980	General-purpose tester replaced with low-cost unit for production
February, 1981	Yield improvements possible with laser programming are detailed at ISSCC
June, 1981	Laser-based redundancy programming extended to other memory devices

diagnosis algorithms are completely analogous in both cases. Laser alignment and positioning are complications not encountered in the electrical programming method, but extensive control software is required nonetheless. Throughput is probably a toss-up now between the two approaches, but the laser technique has a greater potential for improvement.

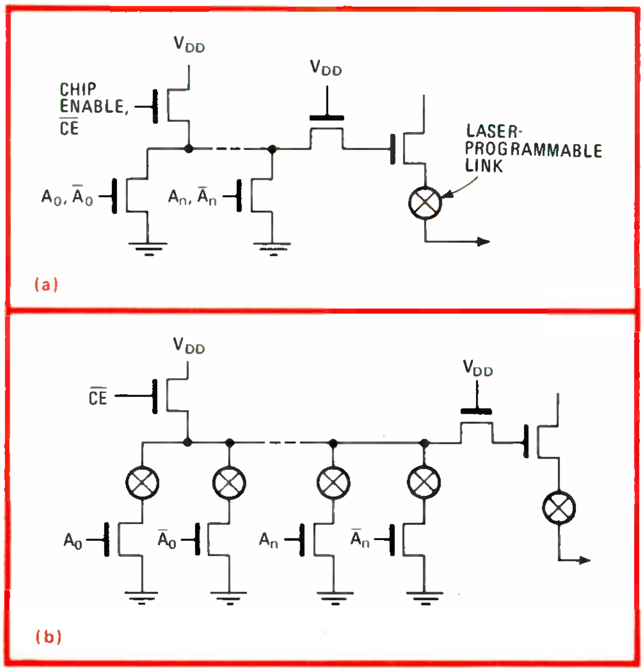
In providing Bell's 64-K dynamic RAM with redundant circuit elements, three design conditions were recognized. The first was that the laser beam and its attendant positioning would not be required for a good memory. Another was that the memory's performance—its access time, in particular—would not be impacted if faulty elements were replaced. A final objective was that it should also be possible to replace defective spare elements with yet other spares.

Figure 1 shows how the redundant circuit elements are positioned on the memory chip. Attached to each 16-K quadrant—organized as 64 rows by 256 columns—are 2 spare rows, complete with decoders and drivers. Either extra row may be substituted for one of the quadrant's 64 rows, or if necessary, they can replace each other. Similarly, 2 groups of 4 spare columns, equipped with decoders and sense amplifiers, are provided to replace any of the 256 columns in their associated quadrant pair or a faulty spare column of the same group.

Figure 2 illustrates the primary difference between a normal and a spare decoder: twice as many decoding transistors are used in the redundant circuit. Whereas



1. Extras. Bell Labs' 64-K random-access memory is partitioned into four 16-K quadrants, each organized as 64 rows by 256 columns. Each quadrant was allotted two spare rows of cells and four redundant columns are associated with each quadrant pair.



2. Doubled up. A normal decoder (a) contains half as many decoding transistors as a redundant decoder (b). If redundancy is not required—that is, if the chip is perfect—the spare decoders will be heavily deselected regardless of the input address.

the standard decoder is selected through a unique combination of address and address-complement signals, the redundant decoders receive all addresses and their complements. Thus, if redundancy is not required, a spare decoder will be heavily deselected, regardless of the address.

A bad row is removed by severing it from its driver, and a spare decoder is programmed by hitting the links in series with the decoding transistor drain electrodes. Row substitution necessitates striking 7 links, whereas the more complicated replacement of a column involves 14 links. However, the capacitive loading of an encoded spare is virtually undistinguishable from that of a normal decoder, so no differences in performance are seen if redundancy is used. It has already been mentioned that faulty spare elements can themselves be replaced; hence, all three of the previously mentioned design goals were met with the laser-based approach.

Basic hardware

The equipment required for VLSI memory repair comprises the laser and beam-positioning system, a memory tester, and a minicomputer to control the other two components in real time (Fig. 3). Commercial laser-trimming systems can be used or converted for redundancy programming if they meet rather stringent requirements for spot size and positioning accuracy. A spot size in the 7-to-8-micrometer range, positioned to $\pm 1\mu m$, has been adequate for Bell's current 64-K dynamic RAM, with its 3.5-μm geometries.

Laser-aiming accuracy is determined by the effective laser spot diameter, the size of the target, and the distance from the target to its nearest neighbor. The 7-to-8-μm spot size is smaller than the beam's diameter because it is limited to an internal section of the beam exhibiting an energy level above a certain threshold value. The targets are heavily doped polysilicon links measuring 3 by 14 μm and covered with a phosphorus-doped silicon dioxide layer. Links are closest in the row lines, where their centers are 9.5 μm apart.

These dimensions underscore just how critically the beam must be shaped and pointed. A targeting error on the order of micrometers may fail to disconnect a link. However, contributing to overall alignment reliability is a phenomenon known as wicking. As shown in Fig. 4, thermal energy generated by the beam is drawn into the heavily doped polysilicon, exploding an area longer than the beam's effective diameter. In fact, because of this wicking action, fully severed links have been observed in the presence of targeting errors—even when the beam is skewed perpendicular to the length of the link.

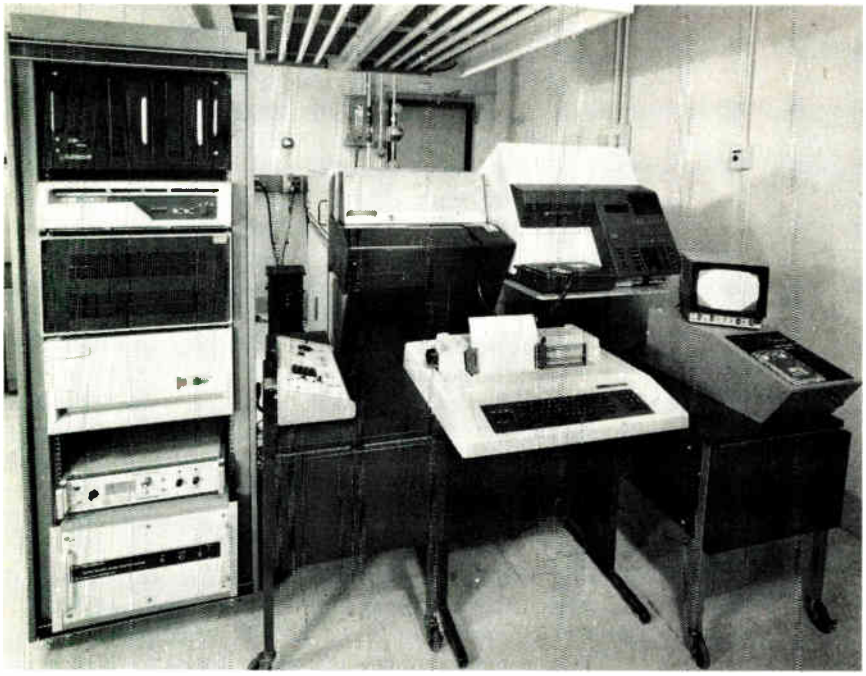
The complete removal of link material through wicking leads to steep-walled rupture of the overlying glass passivation. The lack of debris shown in the scanning electron micrograph is a direct consequence of the link material and structure and the removal technique. Final sealing of the resultant tiny holes in the phosphorus-doped glass with an insulating silicon nitride protective layer is standard with all Bell System MOS products.

Some preliminaries

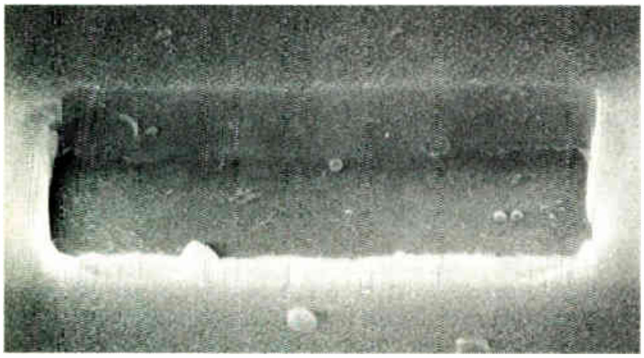
Before the laser is used, a test algorithm is first called upon to determine if there are any gross, catastrophic problems on the chip or more defects than the spare elements can handle. This test program writes and reads data at diagonal addresses and then increments both row and column address values. Any error occurring along a diagonal would require either a spare row or a spare column, so that if the total number of faults in either half exceeds 8 (in the case of the 64-K RAM), the chip cannot be fixed.

If the problems are few enough, a repair routine is called just prior to actual laser positioning. For each half of the memory, spares are allocated to remove the maximum number of defects with each assignment. Repair software keeps track of which spares have been assigned so that no attempt will be made to reuse them. Multiple loops through the setup are possible to ensure that a chip is indeed fully functional after programming.

A separate software module is executed by the minicomputer to line up the laser and fire the shots. The task of identifying a polysilicon target could involve a look-up table with each location; but since the 64-K RAM contains over 2,584 links, this would tax the machine's storage resources. So instead the regularity of the memory chip is exploited, and targets are computed with



3. Basic necessities. The equipment required for the laser-based repair of a random-access memory includes the laser and beam-positioning system, a memory tester, and a minicomputer to coordinate the other two components in real time.



4. Clean-cut. It is a challenge to repeatedly and accurately strike targets measuring 3 by 14 micrometers; however, a phenomenon known as wicking helps out. The laser beam's energy destroys much more than its diameter, being actually sucked into the link.

vectors: the vector to the first target is referenced to a corner of the die and subsequent targets are computed relative to the previous target. The vector approach dramatically cuts down on link-storage requirements.

The rule of thumb on effective laser spot size, to slightly overfill the gap between nearest-neighbor targets, will carry over to the tighter geometries of the 256-K dynamic RAM. A thinner beam can easily be achieved by reducing the focal length of the laser's final objective lens. The green, second harmonic of the neodymium yttrium-aluminum-garnet laser's 1.064-μm fundamental wavelength is already available, but this will not be needed for the smaller spot size. Instead, finer control of laser positioning is the outstanding problem.

A proprietary hardware and software system developed by Bell Labs for automatic fine alignment of the laser beam's position is currently good to ± 1 μm, which should be adequate for programming 256-K memories. The ultimate achievable targeting accuracy, probably around ± 0.25 μm, will limit the capabilities of laser programming. However, such a value would extend the use of the technique for several years—certainly long enough to recover the investment cost by boosting the yield of otherwise unmanufacturable devices.

Other constraints on throughput

Positioning accuracy of the laser beam is not the only area that demands attention. The diagnostic repair algorithm and the laser motion dominate the achievable throughput. The repair diagnostic routine is currently done entirely in software through a complicated analysis of the contents of the hardware error buffer in the memory tester.

Relatively minor enhancements of the error-buffer hardware would allow a dramatic reduction in the diagnostic time required for laser programming. The diagnosis could eventually be encoded in firmware to interrogate and analyze the error buffer within fractions of a second rather than the several seconds now typical. The throughput of the laser programming system could be virtually doubled by this improvement alone.

The remaining throughput-limiting factor is the motion and positioning of the laser beam over each target. By far the biggest component of this delay is dead time: waiting for the laser optics to come to rest before firing the laser pulse at the target link. A potential doubling in throughput is conceivable here as well by concentrating on the acceleration, deceleration and mechanical damping of the laser optics. □

Barney Stevenson just spent two years programming and de-bugging a process control system in assembly code.

Now Barney thinks he deserves some congratulations for his efforts.

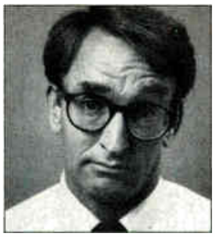
Sorry Barney,

NO CIGAR.

Barney Stevenson thought he deserved a pat on the back. As project manager at Smart Widgets, Inc., he had taken on the biggest real-time process control headache of his life. And after 24 months he'd finally succeeded in programming and de-bugging Smart's newest product.

We think Barney missed the boat.

Barney figured the choice was simple. High level languages like Pascal and Fortran could program quickly,



but would run too slowly and take up too much memory. Assembly code would take longer to program and de-bug, but was the only answer for real-time applications.

Wrong.

Real wrong.

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Circle 135 on reader service card

Dual-function amplifier eases circuit design

by Jim Williams
National Semiconductor Corp., Santa Clara, Calif.

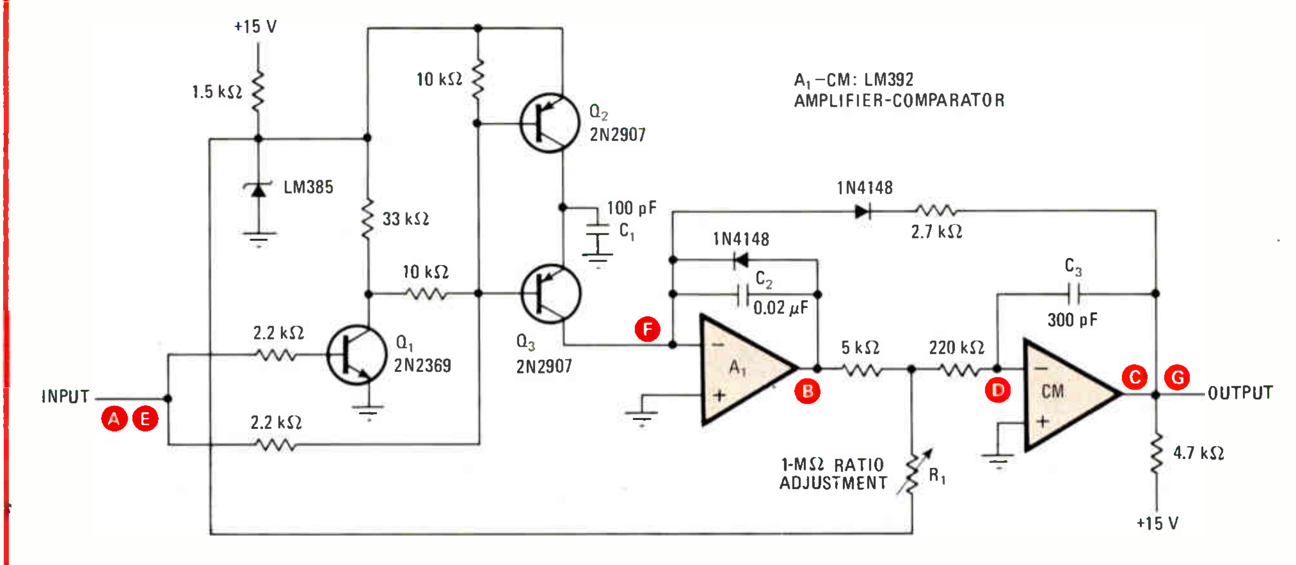
To simplify and cut the cost of the myriad of general-purpose and specialized circuits, chips like National's LM392 combine both amplifier and comparator functions on a single substrate. As has already been noted [*Electronics*, May 5, p. 142], it can be used to build a sample-and-hold circuit, a feed-forward low-pass filter and a linearized–platinum-resistor thermometer. This article will present designs for its use in the construction of a variable-ratio digital divider, an exponential voltage-to-frequency converter for electronic music, and a temperature controller for quartz-crystal stabilization.

Figure 1 shows a divider whose digital-pulse input can be divided by any number from 1 to 100 by means of a single-knob control. This function is ideal for bench-type work where the ability to set the division ratio rapidly is advantageous.

With no input signal, transistors Q_1 and Q_3 are off and Q_2 is on. Thus, the 100-picofarad capacitor (C_1) at the junction of Q_2 and Q_3 accumulates a charge equal to $Q_{cap} = C_1V_0$, where V_0 is the potential across the LM385 zener diode (1.2 volts), minus the saturated collector-to-emitter potential across Q_2.

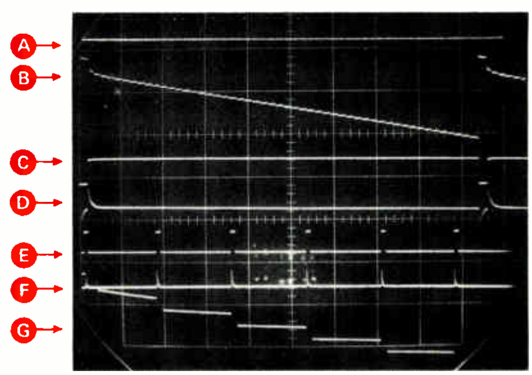
When the input signal to the circuit goes high (see trace A, in the photograph), Q_2 goes off and Q_1 turns on Q_3. As a result, the charge across C_1 is displaced into A_1's summing junction. A_1 responds by jumping to the value required to maintain its summing junction at zero (trace B).

This sequence is repeated for every input pulse. During this time, A_1's output will generate the staircase waveshape shown as the 0.02-microfarad feedback capacitor (C_2) is pumped by the charge-dispensing action to the A_1 summing junction. When A_1's output is

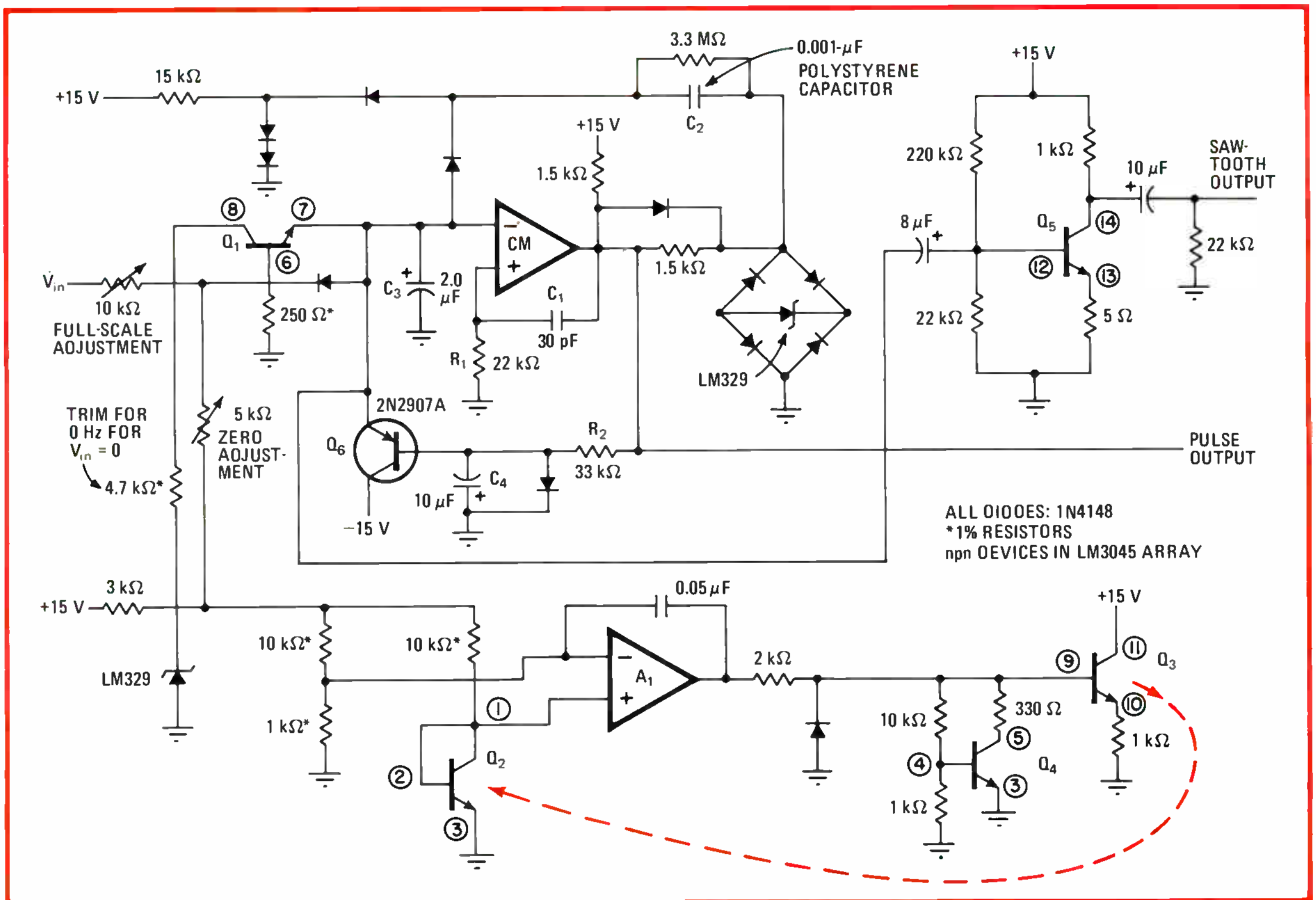


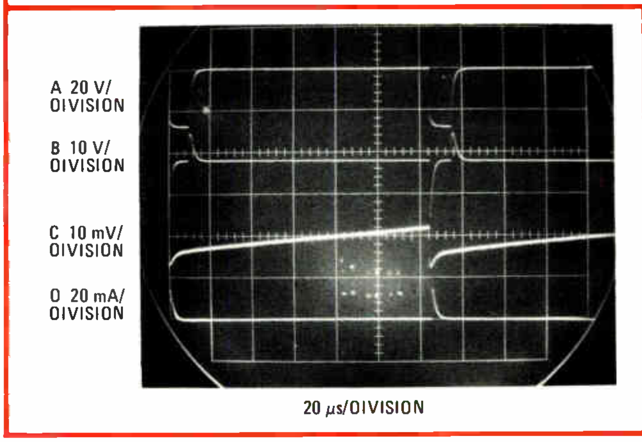
Trace	Vertical resolution (volts/division)*	Horizontal resolution (μs/division)
A	10	500
B	1	500
C	50	500
D	50	500
E	10	50
F	10 mA	50
G	0.1	50

*UNLESS OTHERWISE NOTED



1. Analog digitizer. A single-control potentiometer sets the digital signal's divider ratio from 1 to 100 using the LM392 comparator-amplifier chip. Thus, the division ratio may be rapidly set. Staircase signals are derived from a charge-balancing arrangement, which acts to maintain A_1's summing junction at a voltage null.





2. Sweet sawtooth. When combined with LM3045 transistor array, LM392 forms the heart of an exponential function generator that can easily be built. Waveform conformity to a pure exponential is excellent—±0.25% over the 20-Hz-to-15-kHz range. Thermal drift is minimized with a simple servo loop. Provision is made for eliminating servo lock-up under virtually all conditions.

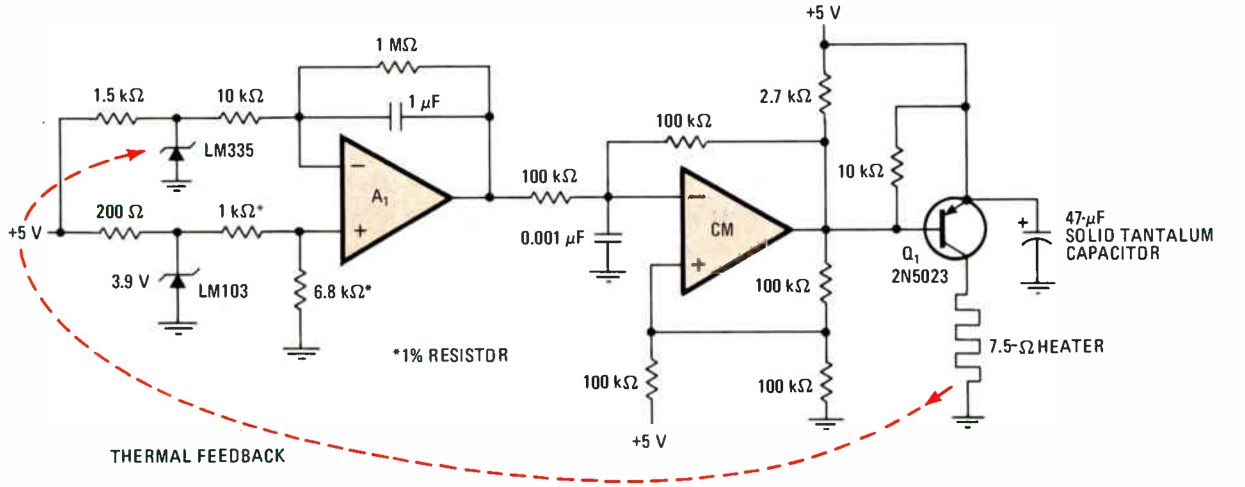
just great enough to bias the noninverting input of the comparator (CM) below ground, the output (trace C) goes low and resets A_1 to zero. Positive feedback to the comparator (trace D) is applied through the 300-pF capacitor (C_3), ensuring adequate reset time for A_1.

Potentiometer R_1 sets the number of steps in the ramp required to trip the comparator. Thus the circuit's input-to-output division ratio may be conveniently set. Traces E through G expand the scope trace to show the dividing action in detail. When the input E goes high, charge is deposited into A_1's summing junction F, and the resultant waveform G takes a step.

Professional-grade electronic-music synthesizers require voltage-controlled frequency generators whose output frequency is exponentially related to the input voltage. The one shown in Fig. 2 provides conformity within 0.25% over the range from 20 hertz to 15 kHz using a single LM392 and an LM3045 transistor array. These specifications will be adequate for all but the most demanding of applications.

The exponential function is generated by Q_1, whose collector current varies exponentially with its base-emitter voltage in accordance with the well-known relationship between that voltage and current in a bipolar transistor. An elaborate and expensive compensation scheme is usually required because the transistor's operating point varies widely with temperature. Here, Q_2 and Q_3, located in the array, serve as a heater-sensor pair for A_1, which controls the temperature of Q_2 by means of a simple servo loop. As a consequence, the LM3045 array maintains its constant temperature, eliminating thermal-drift problems in the operation of Q_1. Q_4 is a clamp, preventing the servo from locking up during circuit start-up.

In operation, Q_1's current output is fed into the summing junction of a charge-dispensing current-to-frequency converter. The comparator's output state is used to switch the 0.001-μF capacitor between a reference voltage and the comparator's inverting input, the reference



3. Oven cut. Quartz crystals are maintained at 75°C with this temperature controller, thus stabilizing output frequency of these sources. Switched-mode servo loop simplifies circuitry considerably. Long-term temperature accuracy is estimated at 10 parts per million.

being furnished by the LM329.

The comparator drives the capacitor C_1 and resistor R_1 combination, this network providing regenerative feedback to reinforce the direction of its output. Thus, positive feedback ceases when the voltage across the R_1C_1 combination decays, and any negative-going amplifier output will be followed by a single positive edge after the time constant R_1C_1 (see waveforms A and B in the photograph).

The integrating capacitor C_3 is never allowed to charge beyond 10 to 15 millivolts because it is constantly reset by charge dispensed from the switching of C_2 (trace C). If the amplifier's output goes negative, C_2 dumps a quantity of charge into C_3, forcing it to a lower potential (trace D). When a short pulse is transferred through to the comparator's noninverting input, C_2 is again able to charge and the cycle repeats. The rate at which this sequence occurs is directly related to the current into the comparator's summing junction from Q_1. Because this current is exponentially related to the circuit's input voltage, the overall current-to-frequency transfer function is exponentially related to the input voltage.

Any condition that allows C_3 to charge beyond 10 to 20 mV will cause circuit lock-up. Q_6 prevents this by pulling the inverting input of A_1 towards −15 V. The resistor and capacitor combination of R_2 and C_4 determines when the transistor comes on. When the circuit is running normally, Q_6 is biased off and is in effect out of the circuit.

The circuit is calibrated by simply grounding the input and adjusting first the zeroing potentiometer until oscillations just start and then the full-scale potentiometer so that the circuit's frequency output exactly doubles for each volt of input (1 V per octave for musical purposes). The comparator's output pulses while Q_5 amplifies the summing junction ramp for a sawtooth output.

The circuit in Fig. 3 will maintain the temperature of a quartz-crystal oven at 75°C. Five-volt single-supply operation permits the circuit to be powered directly from TTL-type rails.

A_1, operating at a gain of 100, determines the voltage difference between the temperature setpoint and the LM335 temperature sensor, which is located inside the oven. The temperature setpoint is established by the LM103 3.9-V reference and the 1-to-6.8-kilohm divider.

A_1's output biases the comparator, which functions as a pulse-width modulator and biases Q_1 to deliver switched-mode power to the heater. When power is applied, A_1's output goes high, causing the comparator's output to saturate low. Q_1 then comes on.

When the oven warms to the desired setpoint, A_1's output falls and the comparator begins to pulse-width–modulate the heater via the servo loop. In practice, the LM335 should be in good thermal contact with the heater to prevent oscillation in the servo loop. □

Programmable sine generator is linearly controlled

by S. Awad and B. Guerin

Laboratoire de la Communication Parlée, Grenoble, France

Because the frequency of this sine-wave oscillator is a linear function of a digitally controlled input, it is attractive for microprocessor and speech-synthesis applications. In addition, it is easy to implement—the digital controller, made up of two resistor modules, needs only to be inserted in place of the two passive resistors normally present in a standard sine-wave oscillator.

It can be shown from the basic circuit in the figure that the frequency of oscillation is given by:

$$f_o = (1/2\pi)(R_5/C_1C_2R_1R_2R_6)^{1/2}$$

with the condition for oscillation being given by:

$$C_3R_3R_6/R_4 \geq G$$

where G is a gain constant. As can be seen, the frequency of oscillation is a function of the virtually grounded resistors R_1 and R_2. They can be replaced by two AD7524 digitally controlled resistors, whose output value is given by:

$$R_1 = R_2 = R_0(2^n - 1)/N$$

where n is the number of digital bits available, N is the digital number that is programmed (set), and R_0 is a constant.

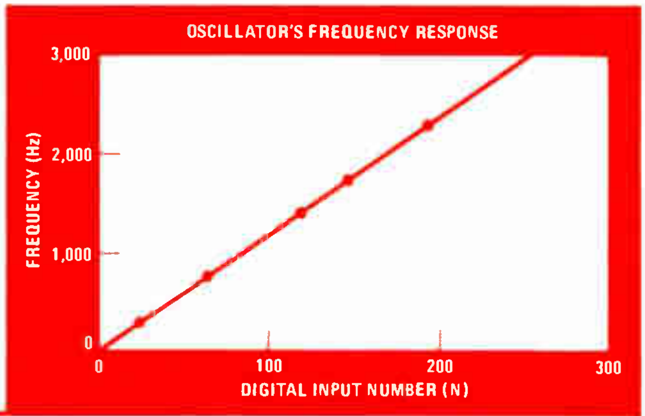
Substituting for R_1 and R_2:

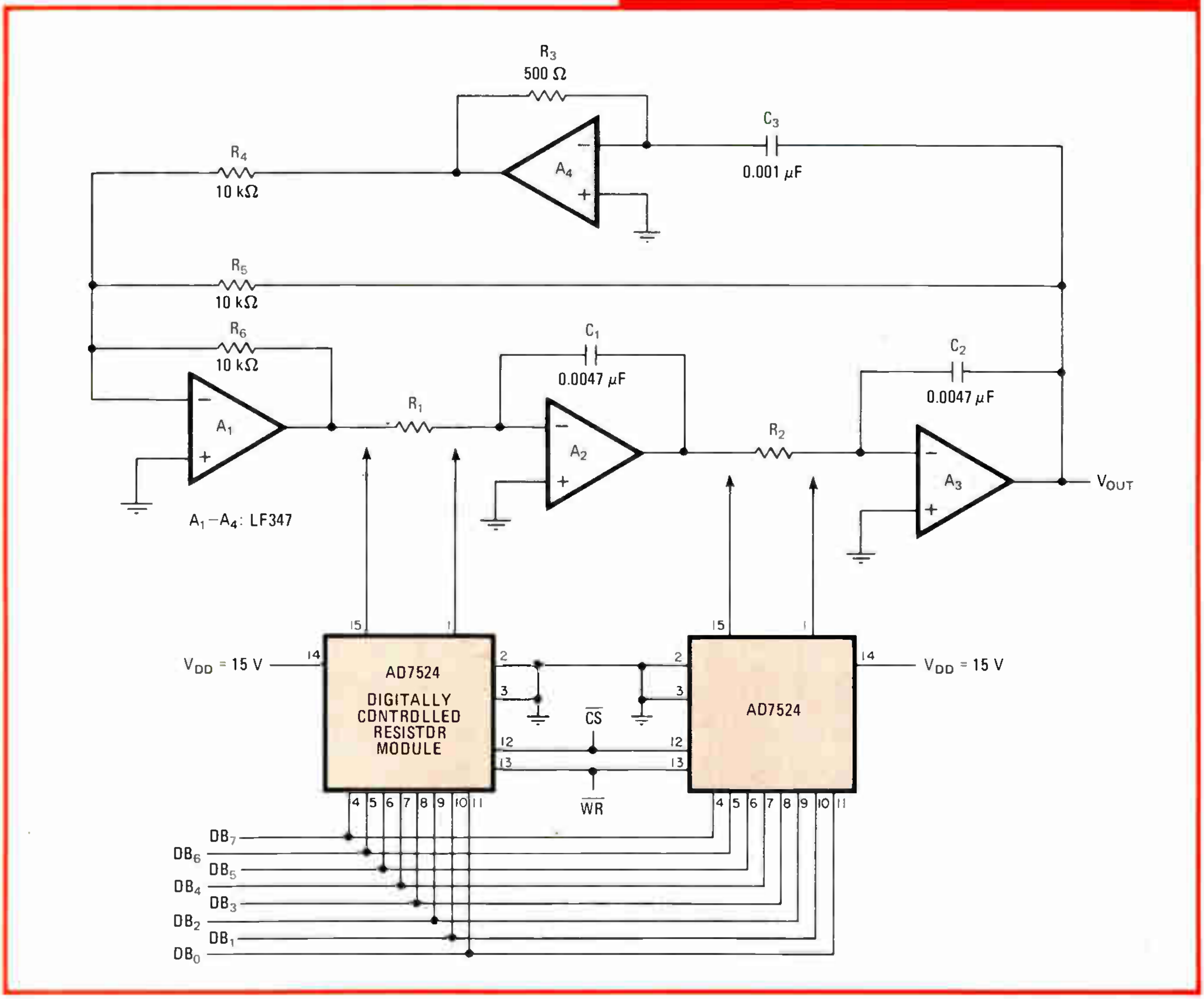
$$f_0 = (N/2\pi)[R_0(2^n - 1)(R_5/R_6C_1C_2)^{1/2}] = KN$$

where K is a constant. Thus the relationship between the output frequency and N is perfectly linear.

These theoretical results are confirmed in the laboratory model, as seen by the response (see plot at bottom of figure). These results were obtained with an R_0 of 11 kilohms. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.





Logically linearized. Oscillator frequency is a linear function of the setting of two digitally controlled resistor modules, making the circuit attractive for remote-control applications of all kinds. An oscillator is easily modified for digital control by the insertion of these modules in place of R_1 and R_2 of a standard sine-wave oscillator's network. Response has straight-line characteristics from zero to 3,000 Hz.

A SPECIAL REPORT

Controlling data communications: statistical multiplexers move in

Multiplexers were once capable only of signal combining, but the latest type is being designed to handle processing as well

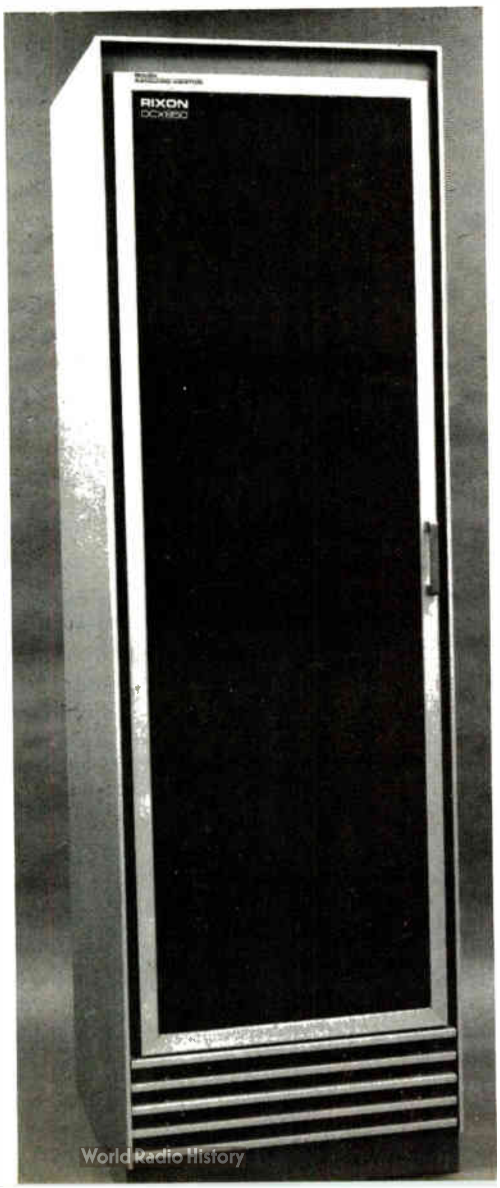
by Harvey J. Hindin, *Communications & Microwave Editor*

☐ When bit- and character-interleaving time-division multiplexers were introduced some 10 years ago, data-communications network designers thought they had the ultimate replacement for the classic frequency-division multiplexer. The new units, using time- rather than frequency-assignment techniques, could combine voice and data traffic from a multiplicity of transmission lines of different speeds onto one fast line with unheard-of cost-effectiveness.

Now it is becoming clear that the two newcomers will be replaced by yet another time-division device, known as the statistical or intelligent multiplexer. This equipment takes advantage of compact and inexpensive semiconductor memory, distributed microprocessor power, and software control to overcome what progress has revealed to be the limits of hard-wired bit- and character-interleaved TDMs (see "The 'ultimate' multiplexer," p. 143).

Statistical multiplexers offer the data-communications network many of the features of more costly minicomputer-based network processors and concentrators. Until now, only this equipment, placed between mainframe computers and a communication network, was able to perform such functions as terminal management, line-speed selection, protocol selection and conversion, data compression, collection of network statistics, monitoring and testing, and gateway interfacing to packet-switching networks. That is no longer the case, as statistical multiplexers are becoming smarter at a rapid rate.

Another advantage of statistical multiplexers is that their distributed intelligence also enables them to act as modems, switches, and port-contention devices. Thus their capabilities indicate that the days of distinct black boxes to perform these functions in communication networks are over.

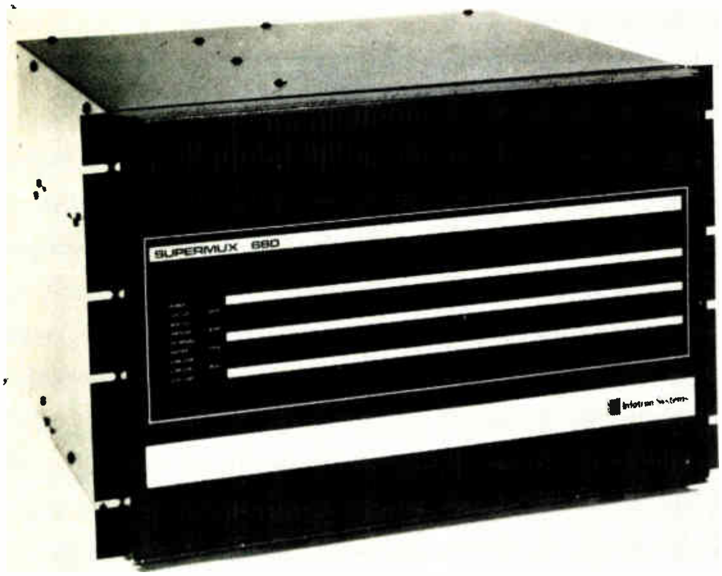


1. Nodal processor. Rixon Inc.'s DCX850 is a top-of-the-line unit that handles up to 240 input lines. It automatically sends hard-copy reports of network events to ports designated by the network supervisor, and it provides both port contention and switching.

Not that a single solution to data-communication problems exists. "Nothing will eliminate the need for anything else," asserts Edward Botwinick, president of Timeplex Inc. of Rochelle Park, N. J. "The development of statistical multiplexers is an evolutionary process. In fact, the next statistical multiplexer products will have so much added value, we will call them communication processors."

Many of tomorrow's networks, which will use 16- and then 32-bit processors, may well have but one highly intelligent statistical multiplexer between the computer and the network. And this multiplexer will need not have its software upgraded when terminals are added to or deleted from the network—there will be enough flexible software on board to do the job.

Statistical multiplexing is a technique for increasing the number of terminals that a time-domain multiplexer can handle without raising the speed of the connection between the multiplexer and the data user, or trunk. Conventional TDMs of either the bit- or the character-interleaving type assign dedicated time slots to each terminal. In this approach, the link between the two ends of the system is under utilized, as terminals are busy only a part of the time. Since the



2. Triple trunk. The Supermux 680 from Infotron Systems boosts capacity by transmitting data over two or three trunks rather than the usual one. The aggregate of all asynchronous inputs may be as much as 115,200 b/s and may be even higher for synchronous inputs.

link is a rented telephone line with a standard 3,000-hertz bandwidth; a dedicated higher-bandwidth line; or a special broadband line that may include costly coaxial-cable, fiber-optic, or satellite links, it is desirable to keep it working as much as possible.

With statistical multiplexing, the available bandwidth is assigned to active terminals only. When the output-line capacity is exceeded, incoming data is buffered and queued by the multiplexer's microprocessors and random-access memory until it can be accommodated. Because the multiplexers use error-detection and -correction codes such as cyclic redundancy checking, buffering, queuing, and transmission can be made almost error-free.

Cost-effective solutions

With all these features, statistical multiplexers are clearly cost-effective devices. "They offer more throughput for the dollar," says Arthur Lynch, senior director of product marketing at Motorola Inc.'s Codex Inc. in Mansfield, Mass. The reason the multiplexer is a successful product, he says, is that its software makes it easy for established multiplexer firms, modem-based manufacturers, and even newcomers to offer a wide variety of products to meet the needs of almost every data-communication network.

Despite the diversity of products, many features are common to most offerings as a result of the relative ease with which they are implemented by the on-board microprocessors. For example, the multiplexers are transparent to the network; that is, they may simply be plugged in. Furthermore, just about any 5- to 8-bit coding scheme on the input lines may be accommodated. And both point-to-point and point-to-multipoint applications are possible, though the former are more common.

The prime function of a multiplexer is to handle a mixture of input-line speeds. The model DCX840 from Rixon Inc. is a good example of this capability, although it is more than a multiplexer. In fact, it is called a nodal processor by the Silver Spring, Md., company because it serves up to 12 communication nodes. Its internal statistical multiplexer handles as many as 240 asynchronous input lines at speeds of up to 9,600 bits per second. A particular input line is made ready for a given speed by setting a switch that also allows for any 5- to 8-bit code with 1, 1½, or 2 stop bits. Any combination of input speeds within the given range can be multiplexed onto a 19.2-kilobit-per-second synchronous output line conforming to the Electronic Industries Association's RS-232 standard or its CCITT V.24 equivalent.

Using a 9900 processor to handle up to 64-K bytes of buffer, the 840 is self-testing and can supply its own usage statistics. It was introduced on the heels of the company's 836, which has much the same specifications except that it is designed for 60 asynchronous terminals and has a correspondingly smaller, 16-K-byte buffer. Unlike the 836, it is meant to serve as a point-to-point multiplexer only. Neither machine has a built-in modem, and each handles errors by means of automatic repeat requests. The latest version, the 850, also has switching capabilities (Fig. 1).

Rixon's 850 and the model 6050 from Codex are typical of the top-of-the-line network multiplexer, but the microprocessor has also made it possible for statistical multiplexing to be applied to the low end of the data-communications spectrum. For example, the SM/2A from Technical Analysis Corp. in Atlanta combines but two channels into one. According to company president Waverly Graham, the unit, which retransmits a message if a checksum error-detection procedure indicates an error has been made, "is useful in data-collection and -transmission schemes in the interference-prone environment of industrial plants." Surprisingly for a low-cost machine, the SM/2A compresses data, as well as coding embedded blank space such as might occur in formatted documents in order to reduce the transmission load on the high-speed output line. Separate buffers are provided for each 9,600-b/s input channel.

Compression, anyone?

Data is compressed to make transmission between statistical multiplexers even more efficient than the basic design concept would indicate. This approach, adopted by many machines, especially the more expensive ones, reduces the number of bits needed to transmit information. Of the multiplicity of schemes for compression, the simplest is to have the transmitting multiplexer scan the high-speed data stream. In that case, all that is required is that repeated characters be recognized. The microprocessor then sends the character once and follows it with another character indicating how many times the first character is repeated.

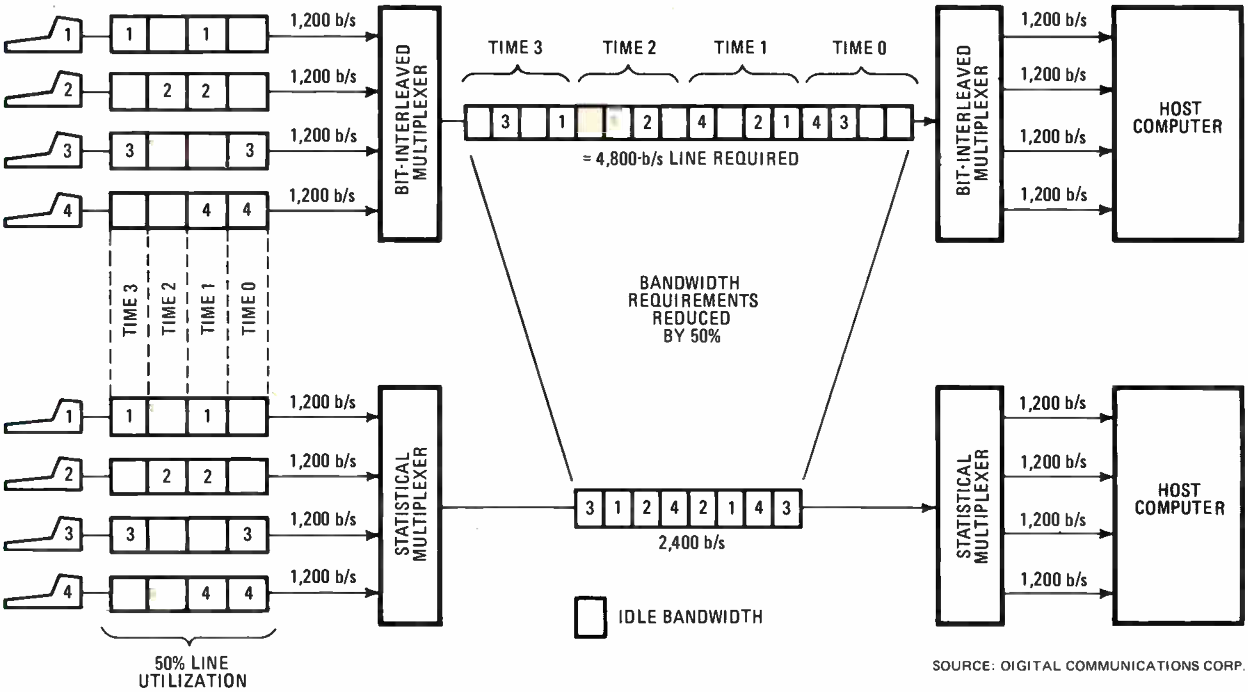
Huffman codes may also be used for data compression in much the same way as in high-speed facsimile machines [*Electronics*, Nov. 8, 1979, p. 85]. Relying on frequency-of-use statistics, a Huffman code converts frequently used characters into a small number of bits while

The 'ultimate' multiplexer

Multiplexers use either frequency- or time-division technology to accomplish their chores. Frequency division is limited in speed and the number of channels it can handle. Furthermore, it is not a digital technique and so cannot take advantage of the latest microprocessor, memory, and software technology. In contrast, time division, which may be broken down into the bit-interleaving, character-interleaving, and statistical approaches, is inherently digital. Multiplexers of this type accept multiple digital inputs and convert them into a composite output.

The input data to any TDM is loaded into a channel buffer and is read by common electronic circuitry. Each channel has its turn, or time slot, in the composite stream, and each sweep of the common electronics is called a frame. The names "bit interleaving" and "character interleaving" indicate how these frames are formed. The statistical approach is different because data-generating machines with no output are totally ignored. (see figure). Of the types of TDM, the most modern and the best in terms of efficiency, channel capacity, and the ability to correct and detect errors is the statistical multiplexer.

Statistical multiplexers are designed for the most common data-transmission situation—where there is dead time between characters or transmissions. These dead times are taken advantage of dynamically by a controlling microprocessor. An 8-bit machine is used in currently available devices to allocate output-line throughput only to active channels. In this approach, the frame length varies and is determined periodically according to the input activity of the multiplexer. The buffer, which stores the input data until it is transmitted, also stores a copy of the transmitted frame so that it can be resent if necessary.

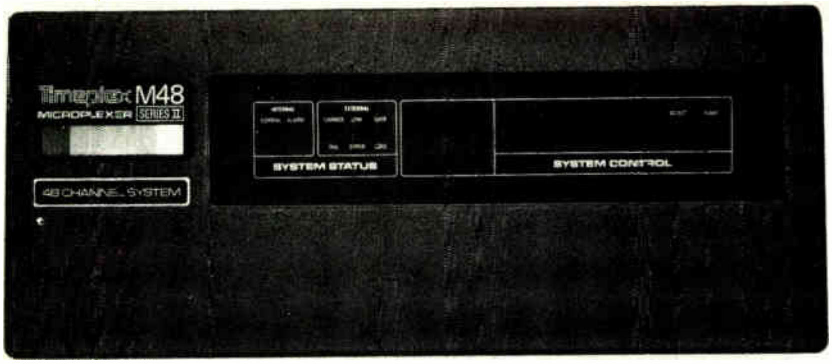


SOURCE: DIGITAL COMMUNICATIONS CORP.

allowing rarely used characters to run their normal length or more. For example, in one Huffman code, the average character is 5 bits long; this length can improve transmission efficiency by 55% over the standard 8-bit format.

The prices paid for these benefits are added hardware complexity and nonstandard software. Thus the question of whether compression should be incorporated into the multiplexer is open to debate. For example, Joseph Visvader, manager of software development at Timeplex, says that "reversing a recent trend, vendors are now de-emphasizing data compression." He points out that the simplest technique, redundant character suppression, has been shown by field experience to be effective only during high-traffic periods. "Only then are there enough characters in the buffer to allow the recognition of a repeated character stream. During low-traffic times, characters pass through the statistical multiplexer too quickly for repetitions to be recognized. And high traffic levels don't occur very often, since few terminals are in constant use," he says. "In any case, many terminals have built-in intelligence that suppresses redundant characters before they are passed to the multiplexer. What this amounts to is the fact that from a communications efficiency standpoint, the CPUs or the terminal can compress data more effectively."

Redundant character suppression may not help, but in practice it does not hurt either. That is not so for Huffman coding. Unless the coding used is adaptable to changing frequency-usage statistics of the multiplexer's input characters, data expansion may result when there is a significant disagreement with the multiplexer's expectations. On the other hand, the cost of adaptive software to handle different input statistics is a high price to



3. Two paths. Timeplex's M4828 Microplexer supports 48 data channels. It stores two routing tables in its memory to keep a system running despite a link failure. Front-panel lights and plain-English prompts are used for maintenance and down-line loading.

pay for what is often a marginal improvement.

In addition, there are several proprietary algorithms for data compression. Such a scheme is used, for example, in the Supermux 680 from Infotron Systems Corp. of Cherry Hill, N. J. (Fig. 2).

Between the Rixon and the Technical Analysis units is a diversity of models that prove out the great flexibility of statistical multiplexers. This flexibility means that manufacturers will apply their multiplexers to solve network problems besides the classic one of transmission-line cost.

Typical of the new problems is the need to connect data-communications gear to packet-switching networks governed by the CCITT X.25 protocol. "The statistical multiplexer will be used more and more to provide a gateway to an X.25 network," says Codex's product manager, Robert Whitcher. To do that, multiplexers will ultimately have to get involved in the packet-assembling and -disassembling process employed by X.25 networks to send their data through various network nodes to their correct address.

Levels of compatibility

For now, one approach to packet capability is to make the multiplexers compatible with the X.25 standard. For example, the Codex 6050 distributed communications processor performs statistical multiplexing, along with adaptive data compression for 250 input lines, while supporting the X.25 protocol. However, it does not necessarily take a big multiplexer or processor like the 6050 to provide X.25 support. For instance, the CM9100 from Digital Communications Corp., Germantown, Md., has this capability, and it is a straight multiplexer geared to only 32 input lines.

Various manufacturers offer different degrees of conformity to the X.25 standard, which is divided into seven levels, only two of which are usually needed for the functions statistical multiplexers currently perform. One company, Memotec Inc. of Montreal, even calls out level 3 compliance, although, according to product specialist Peter Ficocelli, the system is "more than level 2 but not quite full level 3." Others, such as the model TC-8 from ComDesign Inc. of Goleta, Calif., offer compliance with the American Standards Institute's X3.66 standard. Still others simply say their protocol is similar to or a modified version of X.25 level 2.

Statistical multiplexers complying with X.25 level 2 employ a type of bit-oriented protocol on the high-speed line to permit error checking. Typically, the X.25 level 2, which is equivalent to the High-level Data Link Control (HDLC) protocol, calls for a specific bit pattern to start the transmission as a flag or synchronization word. Next, most statistical multiplexers insert supervisory information, such as the length of the particular frame to come, so that the receiver can prepare for proper processing. The actual data follows. Then comes the frame sequence check, in the form of a 16th-order–polynomial cyclic redundancy check (CRC), which constantly monitors the data. A trailing flag concludes the transmission.

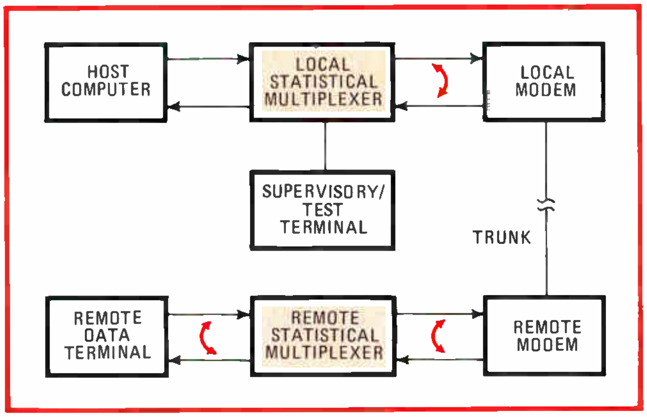
Check at reception

At the data-receiving end of the transmission line, the frame sequence check is compared with the receiving multiplexer's analysis of the incoming data. If all is well, an acknowledgment signal is sent to the transmitting multiplexer. It then clears the acknowledged frame from its buffer to make room for more input. If an error is indicated at the receiver, an automatic repeat request is generated and the offending frame is retransmitted.

Should many errors occur such that the transmitting multiplexer's buffer fills beyond a predefined threshold, the multiplexer stops the terminals attached to it from sending data. This flow-control procedure automatically turns the terminals on again when the transmission problem is cleared up and the buffer returns to a normal level.

The data-transmission efficiency of the statistical multiplexer (the ratio of the aggregate slow input rates and the fast output rate, expressed as a percentage) depends not only on the multiplexer's basic design but also on the size of the buffer and the quality of the transmission line connecting the data generator and receiver. A low-quality line will require many retransmissions, causing old data to be retained in the buffer and, therefore, transmitters to be switched off. The newest statistical multiplexers can achieve a rating of 800% or more, compared with slightly more than 100% for character-interleaved devices and slightly less than that for bit-interleaving types.

The data-communications software required for a statistical multiplexer to complete its tasks is usually written in the assembly language of the multiplexer's 8-bit microprocessor. This software controls port contention (if available), speed and code reconfiguration, capacity



expansion, diagnostics, buffer-overflow protection, down-line loading, data compression, and switching. The 16-bit microprocessors that will be introduced in various new models this year and next perform these functions with even greater flexibility.

Meanwhile, the not-yet-available 32-bit processors are under preliminary study. They are likely to be programmed in C. This language is the basis for Bell Laboratories' Unix operating system, which is proving popular in data-communication applications [*Electronics*, April 7, 1981, p. 108].

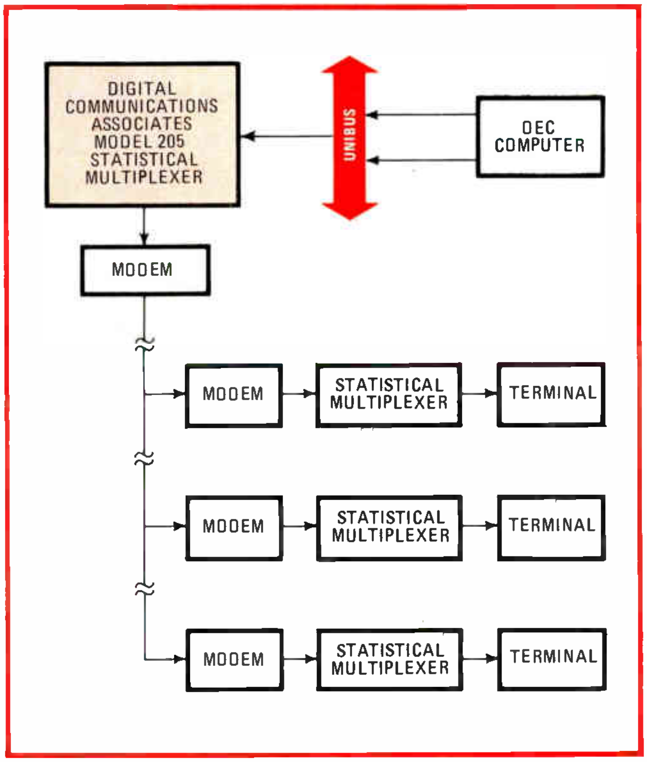
Why pick C? On the one hand, Pascal has inadequate input/output structures, Ada is not yet here, and PL-1 is just too large a language to be used conveniently in statistical multiplexers. On the other, assembly language is low-level, difficult to program in, and nonportable. In between lies C, which is intermediate-level and will be transportable to the many data-communications chips that statistical multiplexers use.

Software demultiplexing

Although most software applications in statistical multiplexers are straightforward, a few are difficult even for experts. One example is the use of the intelligence built into a host central processing unit to eliminate the statistical multiplexer on the CPU side of a data-communications link. This can be done with Digital Communications Corp.'s model CM9100 32-channel statistical multiplexer, for one. The process is called software demultiplexing and has the advantage of saving computer ports and eliminating the need for a central-site demultiplexer and concentrator. Because it is no easy chore to set up the software for such a system, it is cost-effective only when the data-communications system needs several multiplexers, all of which can be programmed to multiplex the same way.

When the X.25 level 2 protocol (HDLC) is supported by the high-speed line of the statistical multiplexer, the system designer can rely on many existing protocol software packages to help him develop host demultiplexing software for his particular application. But care must be exercised, because, as mentioned earlier, the degree of compliance with X.25 level 2 varies. For example, the Supermux 780 statistical multiplexer from Infotron Systems is said to employ a protocol "similar to the X.25 level 2 recommendations." This 128-input-line unit can handle an aggregate input data rate of 38,400 b/s, twice

4. Supervision. Statistical multiplexers allow both local and remote terminals to loop back and test the operation of a given channel. System status can be monitored and data gathered for front-panel display or printout, depending on the multiplexer used.



5. Special-purpose. Some statistical multiplexers like Digital Communications Associates' model 205 are designed for one special host. As shown, the 205 needs only one connection slot on the host's bus to emulate up to 16 DEC DZ11 communication modules.

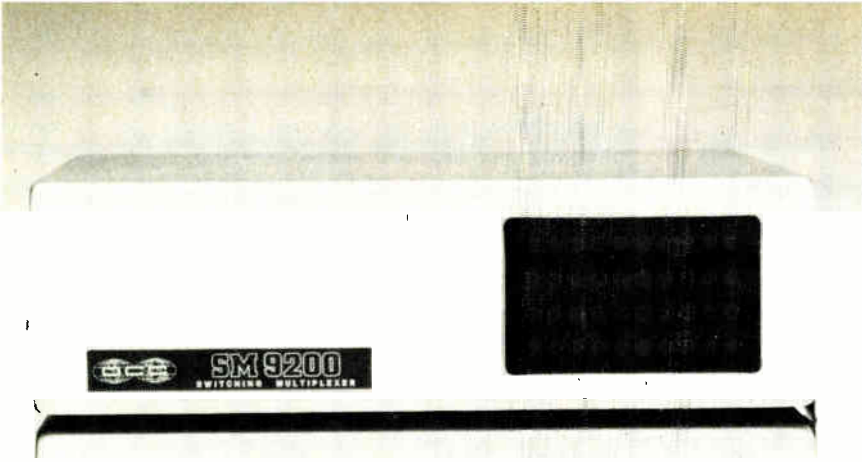
the maximum output speed. Its software controls sufficient buffer storage so that no data is lost even with outages lasting 10 seconds on a 9,600-b/s line.

The addition of intelligence to multiplexers has, as noted, enabled them to take on many functions previously reserved for more elaborate processors and concentrators. For example, suppose one of the slow input lines to a statistical multiplexer is changed in speed and in the number of bits per data word. Most units have enough intelligence to down-line–load—notify—a remote multiplexer so that each remote operator need not reprogram his machine.

Flexible programming

Although down-line loading is an inherent feature of statistical multiplexers, the degree of software flexibility of the particular unit can make a difference in this application. Consider, say, Timeplex's Microplexer statistical multiplexer (Fig. 3). Each time an operator reconfigures the input channels, the change is down-line–loaded without his having to reinitialize the multiplexer. That is desirable because reinitialization interrupts operation and can cause data loss—an often unacceptable risk for a data-communications system.

Down-line loading is not the only place software flexibility makes a difference. External connection to the



6. Switching with class. Digital Communications Corp.'s SM9200 switches and contends for data ports, as well as acting as a statistical multiplexer. It is a 32-input device that supports the X.25 level 2 protocol with a 16th-order–polynomial cyclic redundancy check. Errors are corrected automatically.

multiplexer for command and control can be implemented by the setting of switches—but it may also be implemented by means of some kind of supervisory control language. Such an English-like language makes programming the multiplexer relatively easy from any terminal in the system. Or, as is often the case, a supervisory/test port such as is available in Memotec's Statpac statistical multiplexer is used. In Memotec's approach, the language's critical commands are protected by passwords that are defined by the customer.

Statpac's supervisory control language enables each input data channel to be customized. Furthermore, it can interact with additional software available from the manufacturer to upgrade the multiplexer in the field to be fully compatible with X.25 packet-switching networks like Telenet, Transpac, and Euronet.

The supervisory control language in the Statpac and the front-panel prompt control of the Timeplex offering, among others, can operate through a supervisory/test port. Thus the unit may be tested for proper operation, or statistics gathered for network analysis and management. Both local and remote loop-back tests can be performed and a direct data channel established to a specific device (Fig. 4). Most systems use light-emitting diodes as status indicators for these tests.

16 bits

The TC-3 and TC-4 from ComDesign Corp. of Goleta, Calif., couple LEDs with English-language prompts. They are noteworthy in that they are among the first statistical multiplexers to use a 16-bit microprocessor. The resultant increased processing power makes their software unique. For example, the TC-3 is designed to enable up to eight remote asychronous terminals to communicate with a Digital Equipment Corp. PDP-11, VAX, or DECsystem 2020 computer. One subsystem of the TC-3, the local unit, is installed in the host computer and emulates Digital's DZ11-A or DZ11-C eight-line asychronous interface. This unit also compresses data and performs system diagnostics. The software is so easy on the user that any operating system that supports the DZ11-A or -C can use the TC-3 without software modification. The remote TC-3 functions much as other statistical multiplexers do.

Unlike the TC-3, which is available now, the TC-4 will first be delivered in the fourth quarter of 1981. Designed for PDP-11 and VAX users, it handles (with no software change needed anywhere in the sytem) up to 64 input ports, and the host computer's memory can be accessed directly from the multiplexer's output by way of DEC's DZ11 interface. Up to 16 remote sites will be able to be statistically multiplexed onto the single hex slot that the TC-4 local board requires on, for example, a PDP-11. The TC-4's 16-bit processor also handles down-line loading, status monitoring, and diagnostics.

Other statistical multiplexers, too, are designed to work with DEC systems. The model 205 from Digital Communications Associates Inc. of Atlanta is one such unit (Fig. 5).

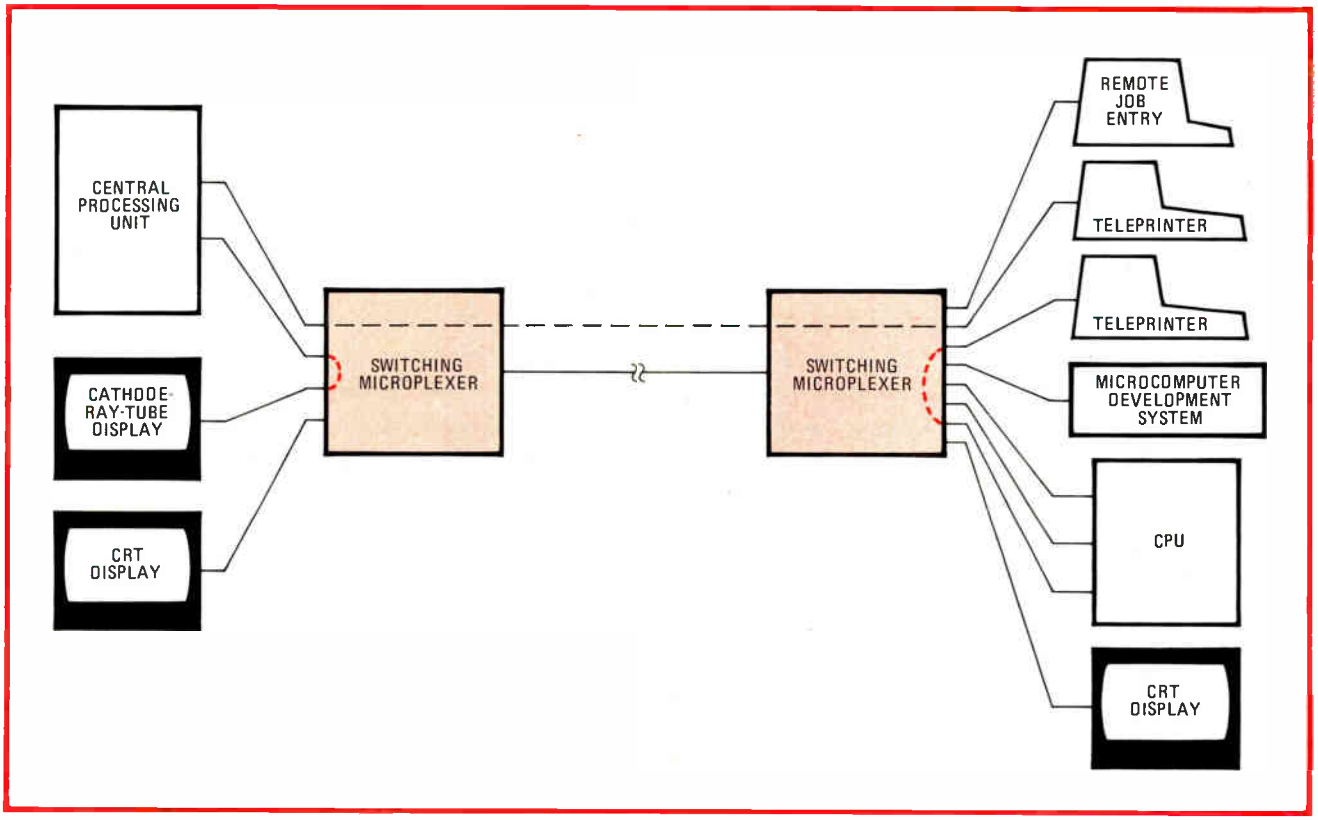
Pick a port

Another feature of statistical multiplexers that hitherto was available only in network processors or that required the intervention of a host computer is intelligent switching and port contention. Normally, multiplexers have fixed connections. However, a switching multiplexer like DCC's SM9200 (Fig. 6) or Rixon's DCX850 allows any CPU, terminal, or device in a network to be connected to any other on either the local multiplexer or a remote one. There are many kinds of switching multiplexers, and depending on the particular device and manufacturer, switching may be obtained with some or all of the usual statistical multiplexing features.

Along with switching, there is what is known as port contention. With this feature, the system designer can set up a network in which a port will contend for any other switched port on either the local or the remote end of the communications link. Here, there is no need to have a one-to-one correspondence between ports at both ends of the link, as is the case in less sophisticated units. It is even possible to have an unbalanced configuration; for example, four ports on the host CPU may service eight terminal ports (Fig. 7). The SM9200 handles up to 32 ports, and the large communications processors from Codex, Timeplex, and others perform similar switching chores.

More switching

Indeed, the statistical multiplexer with switching and port-contention functions is yet another candidate for controller of the office of the future [*Electronics*, April 7, 1981, p. 140]. And since some vendors sell analog-to digital converters so that voice signals may be carried on their statistical multiplexers, even telephones can be accommodated. Very simply, the switching and contention statistical multiplexer can work as a private branch exchange for a local network. Even electronic mail can be implemented.



7. Contention. A statistical multiplexer with port contention lets the network contend for any switched port on either the local or the remote end of the communications link. A 1:1 correspondence at both ends is not required, and four devices may communicate with eight, as shown.

Some statistical multiplexers perform still other forms of switching. For example, a machine may be able to reconfigure its high-speed line when too many automatic repeat requests are generated as a result of noise. Such reconfiguration can be done in gear from Digital Communications Corp., Timeplex, and other manufacturers. In Timeplex's 48-channel M4828, for instance, the software is set up so that two separate routing tables are stored in the unit's memory.

A switching multiplexer is possible because the fundamental hardware needed for port contention, statistical multiplexing, and switching are compatible. "Each piece of hardware," explains Thomas H. Scholl, DCC's director of advanced products, "consists of ROM, RAM, a microprocessor, and interface logic for I/O devices such as computer ports and terminals. The primary difference between these devices is their software, but the needed software is well within the state of the art." It is the combination of compatible hardware and flexible software that allows the multiplexer to treat local and remote port connections with equal ease and to communicate with all ports connected to it (Fig. 8).

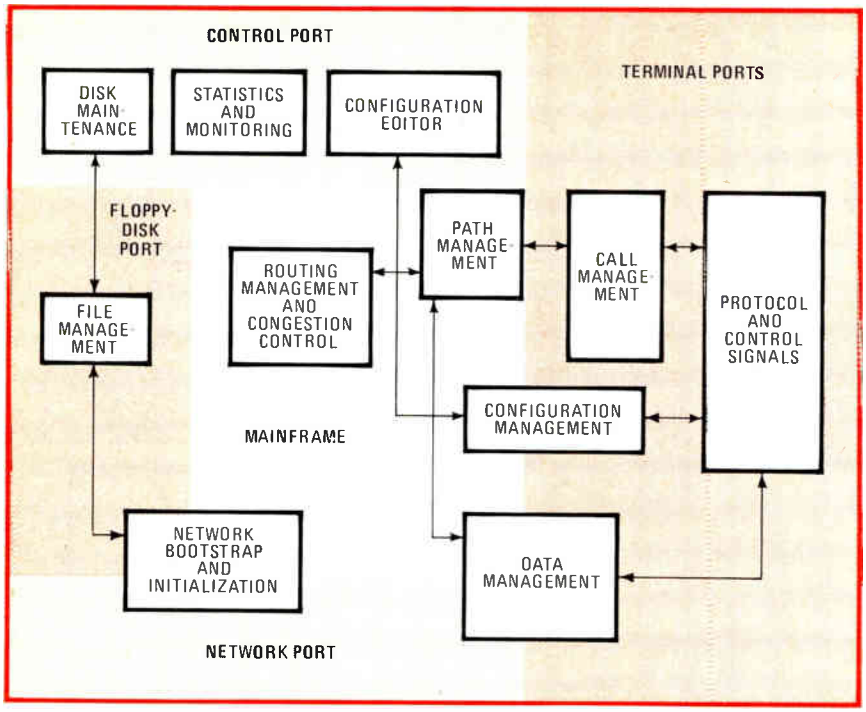
Developments in 8- and 16-bit microprocessors are, in the main, the driving force behind what can be achieved in intelligent multiplexers. But other products of large-scale integration have had their impact as well. For example, the input channels to statistical multiplexers can accept either synchronous or asychronous signals—and at any speed and any combination of stop bits, bits per data word, and parity, for a total of 576 combinations or more in some cases.

This capability is due to the flexibility of devices known as universal synchronous/asychronous receiver-transmitters (Usarts). Available in a multiplicity of forms from many manufacturers, they are far more flexible than their predecessors, universal asychronous receiver-transmitters (UARTs) or universal synchronous receiver-transmitters (USRTs).

What's more, the future holds chips offering even more flexibility. Devices such as Intel Corp.'s 8274 will simultaneously handle two channels, each employing one of a multiplicity of protocols. Because of its increased capabilities, the 8274, for one, will work along with the new 16-bit microprocessors whose computing power will be required for the larger number of channels and protocols that have to be accommodated.

The availability of inexpensive RAMs has had two effects on data-communications systems using statistical multiplexers. For one, now that it is easy to have as much buffer memory as desired, a multiplexer can contain enough storage for the data-generating machines connected to it to do their job without fear that the multiplexer will overload and lose data. For the other, the CPU or data generator can devote its time to computing rather than communications control, since for them inexpensive RAM means that the buffer in the statistical multiplexer functions as a peripheral memory.

The trend to put more and more memory in statistical multiplexers will likely continue. In fact, statistical multiplexer designers foresee the day when their units may even have enough memory to handle the high-speed output of fiber-optic data links. They emphasize that



8. Software. The Codex 6050 distributed communications processor is built around a statistical multiplexer. Because its software is modular and layered, new functions can be added easily, and they may be down-line-loaded with application modules.

with all this storage, the reliability of the buffer RAM is of the utmost importance.

Still other chips will make their mark. For example, some manufacturers are considering using chips implementing the National Bureau of Standards' data-encryption standard (DES) to encode the transmissions of statistical multiplexers. Also, new 16- and 32-order polynomial CRC chips are either now used for error checking or will be incorporated into newer multiplexers.

Who's got the market?

As for the business side, statistical multiplexers will dominate the market for time-division multiplexers within two years, according to industry marketing managers. Estimates indicate that statistical multiplexers had a 60% market share of TDMs in 1980 and will garner 80% by 1983, for about a 30% annual growth rate. In fact, the sales of frequency-division multiplexers and both bit- and character-interleaved time-division multiplexers all will drop substantially in the same period.

"The greatest growth will take place at the so-called low end of the line, which is any unit with a 16-input-channel capacity or smaller," says Alan Warshaw, director of product marketing at Micom Systems Inc. of Chatsworth, Calif. Of the $15 million to $20 million worth of low-end statistical multiplexers sold in 1980, Micom claims to have accounted for 50% to 75%, which makes it the market leader. High-end statistical multiplexers outsold the low-end devices in 1980, but by 1983 their sales will be about equal at $50 million or so, accounting for 80% of the total TDM market.

Warshaw also points out the difficulty of determining unit sales figures and the overall size of the business. He says that many companies in the statistical multiplexer business do not make their own devices but buy them from others and resell them. His view was supported by other product managers in the industry, but it was not their favorite subject of conversation.

As of February 1981, Datapro Research Corp. of Delran, N. J., an industry survey organization, listed 15 manufacturers of several dozen statistical multiplexers as having supplied information about their products when asked, and there are other manufacturers not on the Datapro listings. So, the data-communications system designer has a wide choice. Interestingly, American Telephone & Telegraph Co. does not have a statistical multiplexer product. It would seem a natural for the company, since AT&T already has the dominant share of the modem market. Further, most transmission lines that multiplexers connect to are furnished by the Bell System. Why not branch out into data communications with a more complete package?

According to a report by the consulting firm Creative Strategies International of San Jose, Calif., there are several reasons for Bell's decision. First, compared with the research and development time involved to produce a statistical multiplexer, the total profit opportunity is relatively small. What is a 1983 estimated market of $100 million to a company with revenues of over $1 billion per week? Second, says Creative Strategies, antitrust suspicion might be aroused by a statistical multiplexer product from an entrant of Bell's stature, since it would start to control essential customer-facility parts of a data-communication network.

Still, with statistical multiplexers taking on more of the characteristics of concentrators and processors and becoming ever more useful, the market is now increasing at 30% a year and may grow even faster. That might make it more attractive to Bell in the next few years. Says AT&T's business product marketing manager, Robert C. Hamer, "there is no legal reason for AT&T to not have a statistical multiplexer product and it will be introduced when the customer requires it to meet his needs." □

THE MONOLITHICS WITH MORE OF A PAST HAVE MORE OF A FUTURE

It's a black-and-white fact that's clearly underscored when failures of monolithic multi-layer ceramic capacitors are examined. Many brands have been affected with one significant exception: the Monolythic® capacitors of Sprague Electric.

There are two reasons.

First, Sprague prepares its own ceramic formulations unlike most other monolithic capacitor manufacturers. Second, Sprague Electric's unique wet process of layering the ceramic dielectric provides a truly homogeneous monolithic structure. It virtually eliminates internal voids and delamination, frequent causes of field failure of layer-built ceramic capacitors.

Sprague has more experience in the manufacture of Monolythic® capacitors than any other source, having pioneered the product back in 1958. The monolithics with more of a past certainly do have more of a future. Sprague Electric Company, North Adams, Mass. 01247.

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Terminal puts three-dimensional graphics on solid ground

A rapidly oscillating mirror combined with a CRT display and a custom computer creates images with volume and depth

by Henry S. Stover
Genisco Computers Corp., Costa Mesa, Calif.

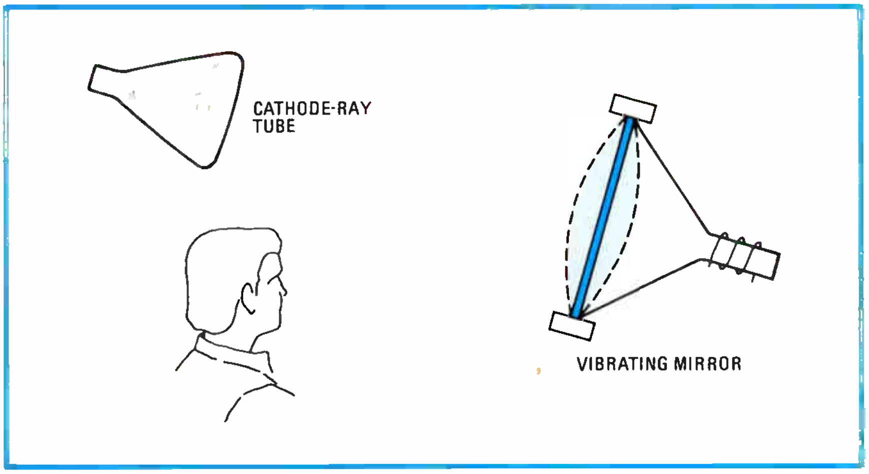
□ An exquisitely simple three-dimensional imaging technique has moved from the research laboratory to application in a 3-d graphics display device that is feasible for business and industry. The new technique, which uses a vibrating mirror to turn a series of two-dimensional images from a cathode-ray tube screen into a continuous 3-d one, has been incorporated into the first commercially available 3-d graphics display terminal [*Electronics*, Feb. 24, p. 49].

Called SpaceGraph, the graphics system has a host of near-term applications, including simulating processes for computer-aided design and computer-aided manufacturing and supplying a 3-d perspective for command and control systems. The device's long-term prospects include solid animation, real-time tomography, oil exploration, molecular research, motion analysis studies, ultrasonic diagnostics, and air traffic control. And, no doubt, other uses will be found wherever a true three-dimensional perspective can help expedite a task.

Images with 3-d properties have been produced in various forms in experimental systems for a long time. In

1. No gimmicks. The SpaceGraph three-dimensional computer graphics display terminal creates images so lifelike the user is tempted to reach into the display to see if the object really is solid. No special viewing aids are required to see the 3-d images.

2. **Do it with mirrors.** In principle, a true three-dimensional display could be achieved by oscillating a display terminal. In practice, however, this is not practical. Thus, an image on a display screen is synchronized with an oscillating mirror that reflects a 3-d image that appears to have greater depth (up to 30 centimeters) than the space in which the mirror actually moves (0.4 cm.).



addition, many people are familiar with stereopticons, stereoscopes, holograms, or 3-d movies. However, translating these 3-d techniques into practical products for the marketplace has been hampered by unrealistic costs and manufacturing problems, which have imposed such limitations on the finished product as too small an image, too clumsy a viewing apparatus, a lack of facilities for user manipulation of the image, or incompatibility of the optical technique and computer technology.

The SpaceGraph device, an interactive computer display terminal, overcomes these problems. High-resolution pictures or contours, vectors, and alphanumeric data can be displayed in a black-and-white or continuous gray-scale format in a volume of 20 by 25 by 30 centimeters. The images and graphics are space-filling, enabling the user to examine images at different angles and see behind them simply by changing viewing position—no glasses or other special viewing aids are needed. Using the keyboard, the operator can manipulate the 3-d image to the same extent as a two-dimensional computer graphics image.

Maintaining perspective

Among the unique electronic advances employed in the system are a very high-speed, bit-slice programmable logic-array graphics computer; memory control and timing circuitry for an anisochronous clock signal; and a translation table and circuitry for correcting anomalous perspective. Since the mirror is vibrating sinusoidally, the velocity of the image is constantly changing. The anisochronous, or unequal time, clock is needed to change the rate at which data is displayed so that the image is not distorted by the varying velocity.

Anomalous perspective arises because the image volume is not a regular rectangular solid but the frustrum (the base part of a pyramid that is left when part of the top is cut off) of a rectangular pyramid with the top side toward the viewer. The portions of the image farther away from the viewer would thus become bigger than they should be if the correction for anomalous perspective were not made.

With these compensating factors, the SpaceGraph terminal can equal the capabilities of flat displays but execute them in 3-d perspective. (See "What 3-d can do for computer graphics," p. 154).

Various schemes for creating a three-dimensional image have been described in technical journals over many years. One of the earliest involved moving a flat-plate mirror, which reflected a flat-screen CRT image (the X and Y coordinates), back and forth through the desired Z positions to create a volume display. But such a device was mechanically impractical.

The next advance in creating a usable Z depth was to flex a plastic mirror so that it would optically change focal length, causing the image to move toward and away from the viewer. By flexing two mirrors on an axis 90° apart and aligning them so that the viewer could see in both the reflection of a CRT, the inventor of this scheme was able to create a 3-d image. However, the mechanical nature of this scheme again made it commercially impractical.

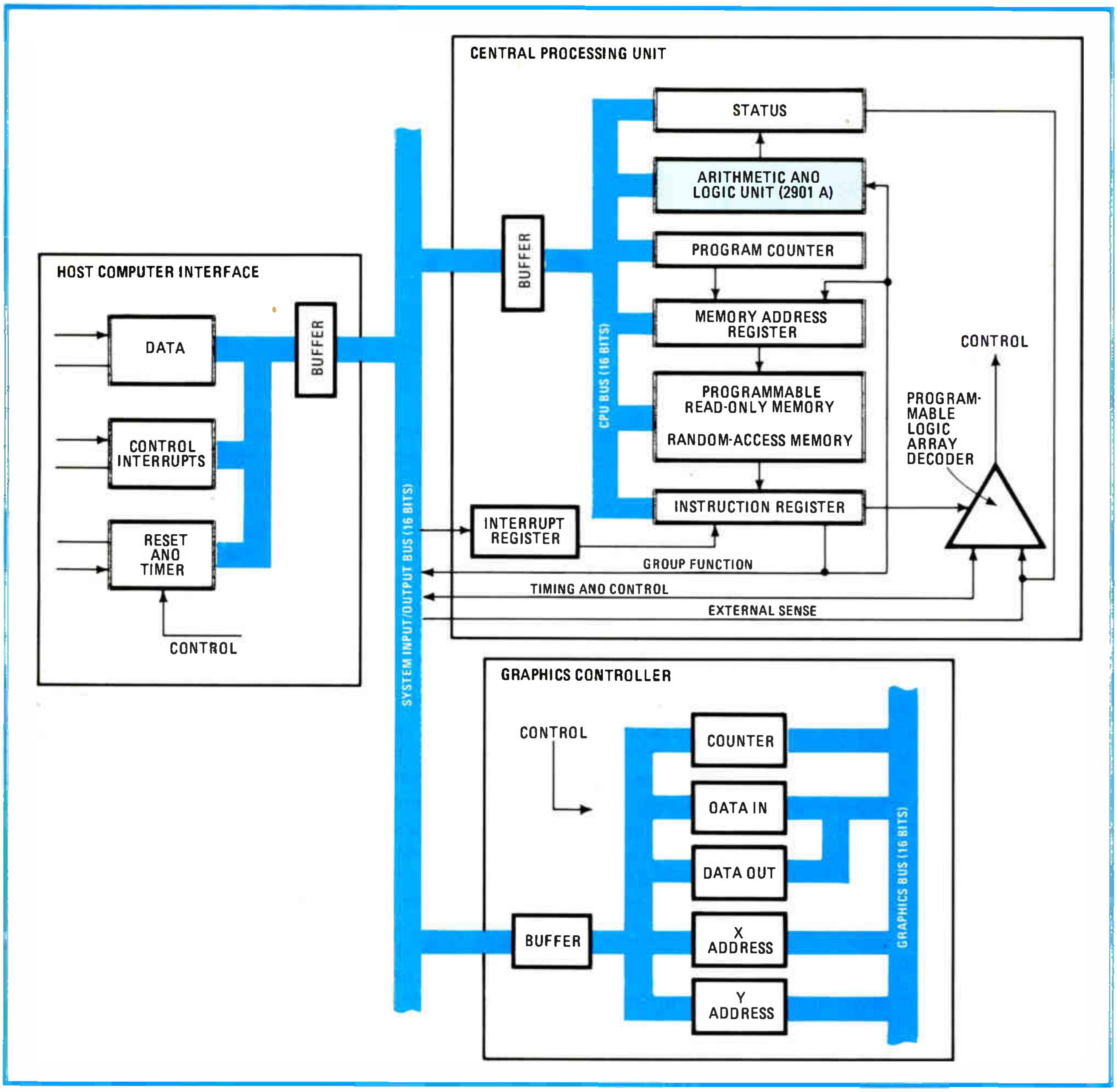
A second method of making a variable-focal-length mirror was developed by Mitre Corp. of Cambridge, Mass. The scheme employed a Mylar membrane stretched over a metal ring and silvered on the front surface. The resulting flexible mirror was vibrated with a hi-fi speaker and reflected the information displayed on a CRT in synchronism with the mirror motion.

This technology was adopted by Lawrence Sher of Bolt Beranek & Newman Inc. of Cambridge, Mass., when he was searching for a practical method of displaying molecular structures from data gathered from an electron microscope. The work at BB&N showed that while the Mylar membrane approach might be usable in a laboratory environment, it had many drawbacks that would make its use in industrial applications impractical.

Mirrors in motion

Thus, Sher embarked on a research project that led to the plastic-plate mirror employed in SpaceGraph—a design resulting in an extremely durable assembly that overcomes all the objections he found to the Mylar membrane (Fig. 2).

Rather than using a flat surface, the system employs a deforming plastic-plate mirror, which makes it possible to reduce the amplitude of the mirror's motion while keeping a large amplitude of image motion. What is lost, however, is the constancy of magnification obtainable with a flat-surface mirror, and as a result, the reflected image is deformed. Compensation in the form of oppo-



3. Fast processor. To handle the amount of display data in the short times required for the 3-d display, this Advanced Display Computer at the heart of the terminal has three fast, wide buses and performs rapid processing with a bipolar bit-slice 2901A arithmetic and logic unit.

site deformation must be made in the way the reflected image is processed for display on the CRT.

Because the vibrating mirror behaves much like an audio speaker, another possible problem is the production of unacceptable acoustic rumble. Since the sensitivity of the ear drops off notably at frequencies below 30 hertz, the problem can be minimized by keeping the distortion and power levels low. The fundamental resonant frequency of the mirror is 30 Hz, and the motion is kept as purely sinusoidal as possible at or below this frequency. The circular plate mirror vibrates on a concentric circular rubber hinge such that, as the center is moving in one direction, the edge is moving in the opposite direction, reducing the propagation of 30-Hz energy. The mechanical driving power for the mirror is actually a high-fidelity woofer situated behind it, which is powered by only a few watts.

SpaceGraph functions in two operating modes—a graphics mode, which displays lines and points in a 3-d array to be used, for example, in computer-aided design, and an imaging mode, which shows actual pictures or images as would be required for computerized tomography (sectionalized or 3-d radiographs).

The graphics mode of the system displays lines (vectors) or points in three-dimensional space. The Z axis, the direction of mirror motion, is divided into 32,768 time slices, each slice being a plane in the X and Y axes. Vectors are drawn and points are plotted by illuminating one volume picture element (pixel) per plane in up to 32,768 possible planes. The volume pixel, called a voxel, may be located anywhere in an X-Y plane, which has a resolution of 4,096 points by 4,096 points. There are more than one-half trillion possible voxel positions of which any 32,768 can be displayed at one time.

In the imaging mode, complex 3-d images are shown as planes of data stacked one behind the other with each plane representing a slice of the 3-d display. Planes are displayed on the CRT with raster scanning—one plane for each of the 32,768 possible positions of the mirror. The planes are interlaced with half of them being illuminated on the forestroke and half on the backstroke of the mirror's oscillation. Both the size of the planes in the X-Y dimension and the number of planes in Z can be selected. The total voxel capacity in the imaging mode is 262,144 for each refresh cycle. The matrix size of each plane can vary from 64 points by 64 points with 64 planes to 256 points by 256 points with 4 planes.

Each pixel of a plane in the imaging mode and each voxel in the graphics mode also have 128 intensity levels and a blinking option. An 8-bit value provides the intensity and blinking information for each pixel or voxel—7 bits for intensity and 1 bit for blinking. A programmable translation table determines the intensity level. This ability to vary the intensity of each pixel or voxel allows the system to be used for displaying data with four variable inputs. The user can intensify, dim or blink any part of the 3-d image to create additional effects. Scrolling of the image in the Z dimension is also possible in both display modes.

Mixing modes

The graphics and imaging modes can be interlaced in a variety of ways. For example, image planes could be displayed in the forestroke, while vector and point graphics are being displayed on the backstroke. By adding more memory to the terminal it is also possible to display one image or graphics piece while a second full display volume of data is held in memory ready for instant display. The user could ping-pong between different graphics and images or combinations of both.

The heart of the SpaceGraph control system is the Advanced Display Computer in Fig. 3, a graphics computer incorporating a bipolar bit-slice arithmetic-and-logic unit combined with a direct-decoding programmable logic array. The advanced architecture of the display computer makes possible execution times of 160 nanoseconds and word transfer rates of 3 megahertz.

The computer's unique bus structure contributes significantly to the terminal's speed and flexibility. Separate host and graphics buses access an input/output bus independently, and the graphics bus has a wide addressing capability. The configuration handles data automatically in either bytes or words.

The computer has 128-K bytes of memory for program and data storage, including space for extensive data lists and a translation table. This standard memory configuration comprises 16-K bytes of programmable read-only memory and 112-K bytes of random-access memory. Future options will extend the computer's capacity to as much as 2 megabytes.

A set of more than 140 mnemonic instructions is implemented for the display computer's central processing unit. Among those is a powerful block-transfer capacity that can handle up to 64,000 words with a single command at a maximum speed of 3 million words per second. This massive block transfer can be done between the host and the display computer memory, between the display computer memory and the graphics refresh memory, or directly between the host and the graphics refresh memory. Thus, it is possible to load image data into the refresh memory at computer or host-memory speeds. In addition, blocks of data may be stored on a disk drive or other optional system peripheral connected to the terminal and be paged into the display computer memory at high speed.

Pause that refreshes

The unique interaction between the refresh memory and the display computer greatly increases system flexibility. Since this processor will perform at twice the speed required for refresh, both it and the host computer can have continuous access to the refresh memory on an interleaved basis. The even memory cycles are reserved for refreshing the CRT from the refresh memory, the odd cycles for communication with the display or host computer. Thus, the refresh memory, which is structured as 32,768 64-bit words in the graphics mode and 16,384 128-bit words in the image mode, can be updated at high speed without disturbing the display.

There is a different addressing mode for each operating mode. In the graphics mode, one 64-bit word is used per voxel—32 bits for a tag, 12 bits for the X position, 12 bits for the Y position, and 8 bits for intensity and blinking. In the imaging mode, each 128-bit word represents 16 contiguous voxels, each with a 7-bit intensity value and one bit of blinking information.

An element of particular interest on the memory timing and control board is the anisochronous clock. Because the image motion on the mirror is not linear (the maximum rate of mirror motion is at the midpoint of its travel), a variable clock must be provided for controlling the timing of the transmission of data to the CRT so that it matches with the varying rates of travel for each position of the mirror. Only then will planes in the image mode and voxels in the graphics mode be properly spaced in the display volume.

Time becomes motion

The anisochronous clock controls memory access so that data is transferred from memory to the CRT at the appropriate rate. Using a proprietary technique, the clock monitors position, rather than time as do most clocks. In addition, the memory-timing and control board contains a complex set of programmable counters that control the variable X-Y scan timing required to accommodate the variable plane sizes and number of planes in the image mode.

In addition to the display computer, the SpaceGraph monitor control system includes a video translation table for controlling blinking, blanking, and intensity; a mirror drive control; X and Y sweep controls; digital-to-analog conversion for intensity, X, and Y variables; and anomalous perspective correction (Fig. 4).

The translation table is a 256-byte high-speed memory

What 3-d can do for computer graphics

There are at least five functional ways in which an interactive, space-filling display provides major qualitative improvements over flat displays, says Lawrence Sher of Bolt Beranek & Newman Inc.[1]

First, space-filling data or models can be shown objectively. The SpaceGraph display presents an objective visual scene similar to that provided by a physical model. It does not draw on the viewer's ability to perceive depth or his or her prior knowledge for the interpretation of depth cues. Therefore, it can be used in teaching subjects of which the viewer has little or no prior knowledge. He need not ask, "What do I see?", but can go straight to the more central question, "What is important in what I see?"

Second, the tremendous power of the human mind to recognize patterns is more fully exploited. With brightness added to the three dimensions, interactions of up to four parameters can be displayed at one time and more information can be comprehended much faster. Imagine an experiment that involves the correlation of four parameters, say, temperature, humidity, wind speed, and wind direction. On flat media, four parameters must be plotted two or three at a time, and patterns must be sought with the hope that no significant, influencing pattern has been introduced by the yet unplotted parameter. With a three-dimensional plot that also used brightness as a fourth parameter, each data point could represent all four parameters making all interdependencies fully visible.

Third, data of ephemeral value can be more quickly understood. In operator-assisted process control it is important that all data be easy to understand within a given time interval. Some examples are nuclear plant control, air traffic control, and the piloting of a vehicle. The addition of a third, spatial dimension presents data in a form that the mind can most quickly understand, as in explicitly showing the vertical separation between aircraft. Decisions can be made in seconds rather than minutes or, in extreme cases, in days rather than never.

Fourth, some kinds of data could be displayed it has so far been impossible to display. A fluid flow field, which is time-varying, cannot be represented adequately, even in a physical model. This is true also in the visual presentation of a complex structure with internal movement. A 3-d display can represent both these cases.

Finally, interactive computer graphics can be dimensionally matched to its subject. For such applications as computer-aided design, interacting with a space-filling image can be nearly as natural as interacting with a physical model. Curved surfaces can be shown as such, and through-holes seen through. Hidden-line removal as a depth cue is eliminated, since depth is explicit. And for team work, the object can be shown objectively to another person, the computer aiding the job process, instead of entangling the application in processing limitations.

References

1. Lawrence Sher, "The SpaceGraph Display: The Utility of One More Dimension," internal paper at Bolt Beranek & Newman Inc., August 1980.

that accepts 8 bits of intensity and blinking information from the refresh memory as its address. The output from the translation table drives the intensity digital-to-analog converter, permitting any of the 256 values in the translation table to be set to any of the 128 intensity levels. With the table, intensity values can be highlighted and others blanked in order to emphasize significant areas of the image. When blinking is used, the eighth bit chooses either the upper or lower half of the translation table. The lower half is generally used to display the data at normal intensity, while the upper half could be used to display it at a lower intensity.

Cutting software overhead

The anomalous perspective could be corrected in software by adjusting the X-Y coordinates to fit the Z depth values. However, this would add considerable software overhead. Thus, the monitor control circuitry includes an automatic anomalous-perspective correction function. The function applies a correction factor of $1-0.0239$ sine ωt, where ω equals the frequency of the mirror vibration—30 Hz—and t is time. The correction is applied to the d-a converters for X and Y.

A unique problem encountered in this 3-d display is Z contention. In the graphics mode, voxels are written one per plane with each point described as an X-Y position in that plane. There are 64 bits of memory available per plane to describe the X position, the Y position, and the intensity; and 32 bits are available for identifying and separating graphic entities. Because of this limitation, it is not possible to display a vector on the mirror that is perpendicular to the X axis in the Y direction.

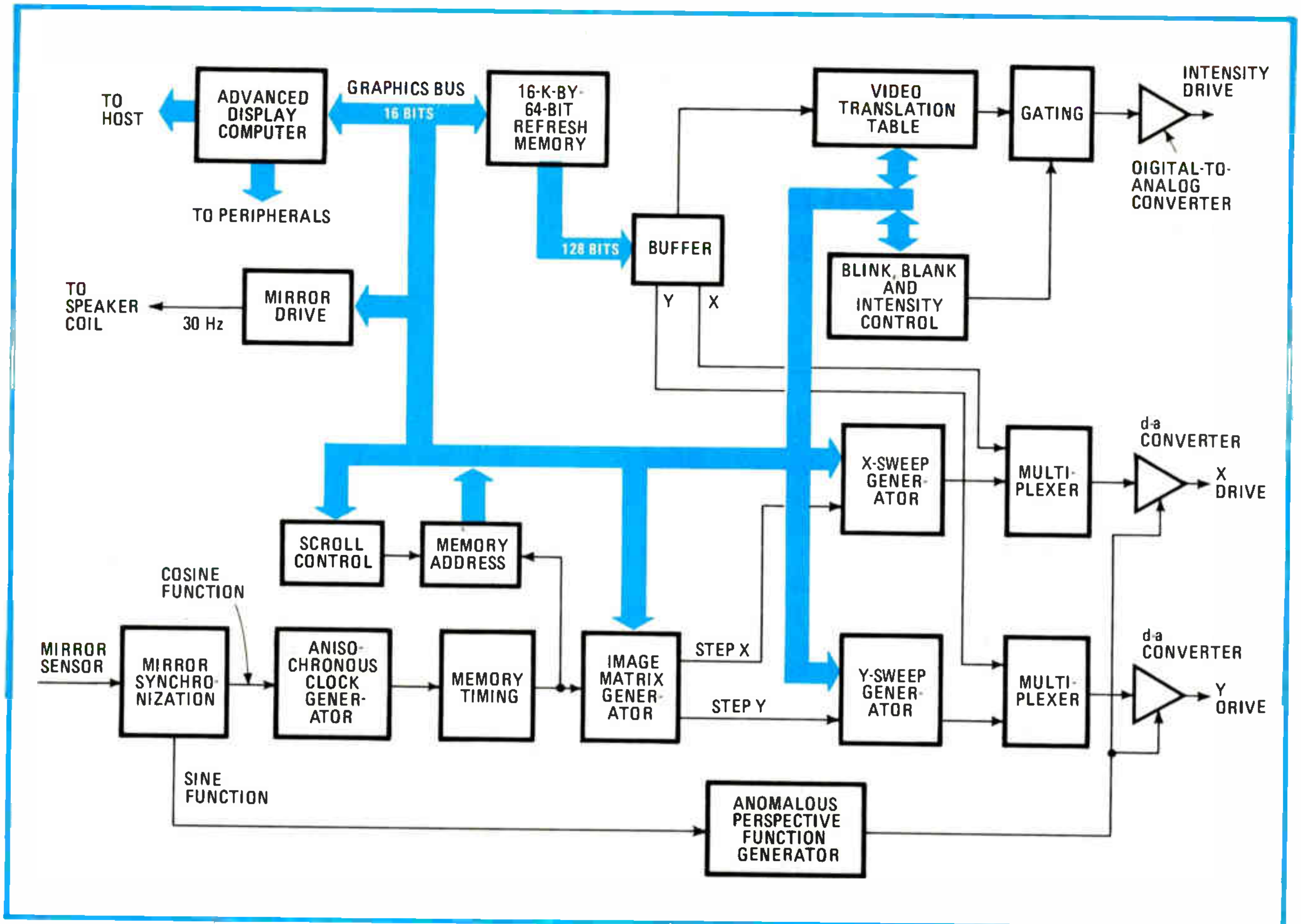
To compensate, a 3° tilt is used, which appears to the human eye to be flat. At 3°, a full-width vector (all the way across the screen) will encompass 714 planes. To draw a full-width vector that is solid, approximately 256 voxels are drawn through the 714 planes. At this rate, fewer than three full-width vectors can be drawn if they reside in the same Z space. This may be an adequate number of vectors for some applications, but when a display is more complex, many vectors then contend for the same plane—hence Z contention.

Since the number of voxels per vector can be reduced by half before the eye begins to notice the individual voxels, the system assigns an equal number of the available voxels to each contending vector, thereby diminishing the number of points per centimeter equally for all vectors. A vector drawn parallel to the Z axis requires only half the number of voxels to appear solid than does a vector perpendicular to the Z axis when the parallel vector is viewed at a 30° angle to the side.

Sorting in sequence

A complex sort algorithm programmed on the display computer operates on vector files downloaded from the host. These files are converted into a file of refresh data that, when sequenced onto the CRT, results in the vectors being properly displayed. The Z contention algorithm then assigns Z planes to the vectors, depending on their angle to the Z axis and how recently they have been given a plane relative to other vectors contending for a particular Z plane.

The SpaceGraph system is designed with both hardware and software as a satellite work station that can



4. Big picture. The SpaceGraph 3-d terminal contains more than just the Advanced Display Computer. In addition to regular video control, the special functions required for 3-d include the anomalous perspective function generator, anisochronous clock, and video translation table.

offload the graphics function from the host. With the addition of peripherals, the system can act as a stand-alone graphics computer in a number of applications. Complex applications requiring extensive memory or calculations will need access to a host computer more powerful than the graphics computer, with the system working as an intelligent graphics terminal.

Master of modes

The system will function in three software modes. In the first, it can function as a display terminal, receiving and displaying data from a host computer or from mass-storage peripherals connected to the display. In the second, it can receive commands interactively from a keyboard or another complete terminal connected through the graphics computer in the display terminal. In the third software mode, the system will respond to commands from the host with the graphics computer in the system performing some of the required functions. Data from interactive input devices attached to the system are available to the host through the graphics computer. Fortran-callable routines for a range of host computers will be available for this latter mode.

Modular design of the software makes SpaceGraph highly flexible for a wide variety of applications. The user can program on the host or write routines in the display computer's assembly language directly into the system. Either way, a user or system builder has access to all functions through Fortran calls in the host or display-computer protocol in the SpaceGraph system. In a simple application where the user wants to proceed through a data base and do simple manipulations, the system can perform all functions without having to assign a portion of the load to the host.

The software for processing the data base will perform all functions described in the Siggraph graphics standard, including such functions as selecting view, clipping, and transforming the data base. Some extra functions have been added to these standard ones to take advantage of the special capabilities of the system, such as interactive highlighting of planes and dynamic change of the video look-up table.

The software hierarchy includes graphics routines, nongraphic utilities for host communications, routines for downloading, debugging, interactive processing, control, and input/output handling routines.

In describing a product like SpaceGraph it is tempting to say "the future is now," but in fact, the potential of this technology has just begun to be tapped. The system will, no doubt, follow the present computer graphics trend in an increase of total image bits and increases in speed. And there is no reason why, given these improvements, full-color 3-d displays of this type cannot be built in the near future. □

Wired-OR ECL one-shot has near-zero propagation time

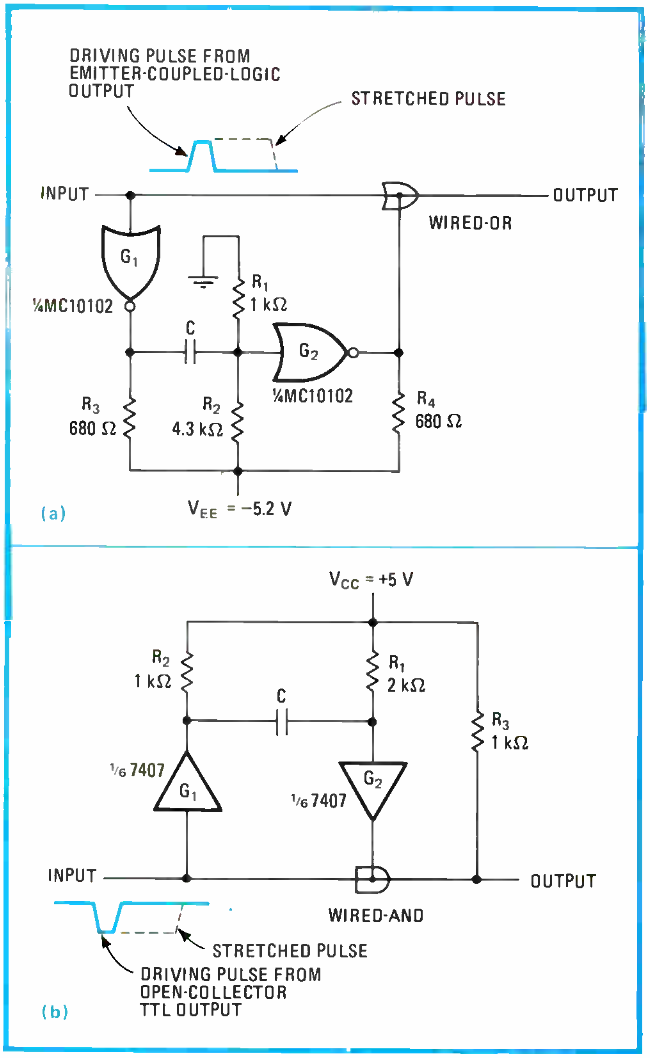
by Jozef Kalisz
Warsaw, Poland

Because of their output configurations and current-handling capabilities, emitter-coupled-logic and TTL circuits can easily yield the wired-OR function simply by having the outputs of two gates tied together. This trait may be employed to build a pulse-stretching circuit in either logic family that is equivalent to a monostable multivibrator having virtually zero propagation time.

Such a circuit, shown in (a) for ECL, relies on the positive-feedback loop created by gates G_1 and G_2. In the steady state, the input voltage of G_2 is maintained at the V_{IH} level of about −1 volt by resistors R_1 and R_2. The positive input trigger pulse, derived from a typical ECL gate, brings the driving-point potential to −1.8 V, permitting capacitor C to charge.

As long as the input voltage to G_2 remains below about −1.3 V, the gate's output voltage will be high, thus stretching the input pulse. If the propagation time of the gates is not taken into account, the output pulse width is approximately equal to $T = 0.98\ CR_1 \| R_2$. With the gates in the 10000 logic family, the minimum pulse width of the driving pulse can be made 4 nanoseconds, which is equal to the propagation time in the loop. The circuit may directly drive a coaxial cable or a microstrip line, provided they are correctly terminated. In such a case, pull-down resistor R_4 is not required.

A similar circuit is shown in (b), with open-collector TTL gates used to implement the wired-AND function. The output pulse width is approximately $T = 0.28 \times CR_1 \| R_{IL}$, where R_{IL} is the input resistance of G_2 when its input voltage remains below the 1.4-V threshold. Typically, R_{IL} = 4 kilohms. The shortest input pulse required is about 20 ns, and this value again is equal to the circuit's propagation time. □



Infinitesimal. Wired-OR connection of emitter-coupled-logic gates (a) permits the building of a pulse-stretching circuit that is equivalent to a one-shot having virtually zero propagation time. In this case, it is 4 nanoseconds, equal to that of the minimum pulse needed to excite the circuit. Similar results are derived from wired-AND gates of TTL (b), although the propagation time is a bit longer—20 ns.

Interface unites Z8000 with other families of peripheral devices

by S. Majundar, K. Kumar, and K. S. Raghunathan
Indian Telephone Industries Ltd., Bangalore, India

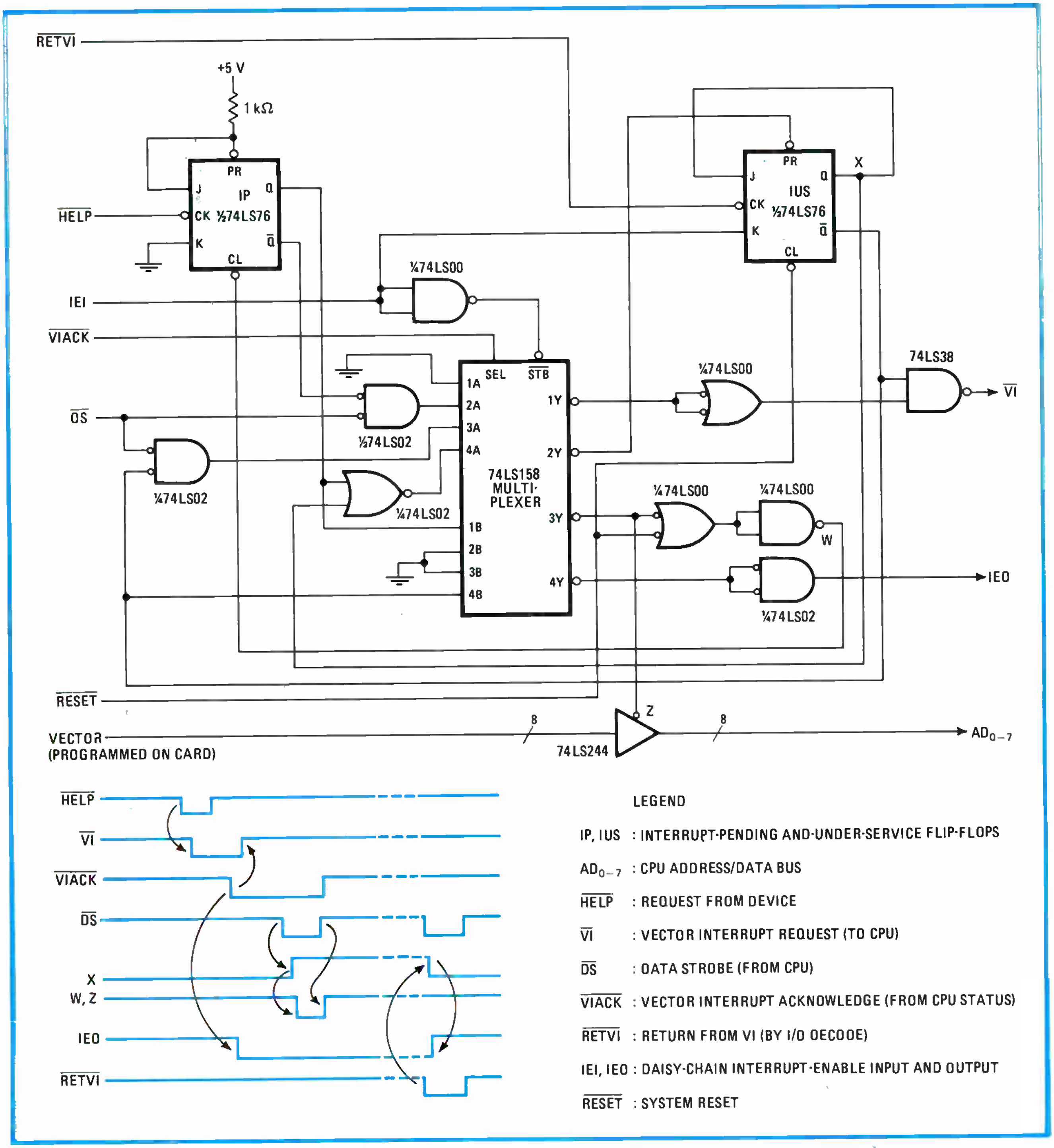
Users desiring to link up to the popular and versatile Z8000 microprocessor/microcomputer with peripherals belonging to other families will find the going much easier with this interface, which uses only six low-cost integrated circuits. Whether merging technologies in order to meet system requirements in a hurry or combining them to garner the advantages of both, the user will often find the new system most useful and cost-effective when appropriate software is at hand.

Operation of the circuit shown in the figure may be better visualized with the aid of the legend and the timing diagram shown at the lower right and bottom, respectively. Initialization occurs with the interrupt signal $\overline{\text{HELP}}$ for requesting attention from the processor. It is of course assumed that the daisy-chain interrupt line, IEI, is high and also that the vector-interrupt acknowledge line, $\overline{\text{VIACK}}$ is inactive, yielding the condition where the 74LS158 multiplexer outputs show $Y_i = B_i$.

With the falling edge of $\overline{\text{HELP}}$, the interrupt-pending (IP) flip-flop is set and the vector-interrupt-request line (VI) goes active. After completing execution of the current instruction, the processor will then enter the vector-interrupt-acknowledge cycle and the $\overline{\text{VIACK}}$ and data-strobe ($\overline{\text{DS}}$) signals will be activated in sequence (see timing diagram).

When the $\overline{\text{VIACK}}$ line falls, the 74LS158's Y_i outputs are switched to conform to $Y_i = A_i$, and the following sequence of operations is initialized:

- $\overline{\text{VI}}$ is deactivated and IEO goes low in order to disable other interrupting devices in the chain. The priority resolution process is initiated in the daisy chain, settling down before the data strobe ($\overline{\text{DS}}$) line goes active low.
- Assuming the device under discussion has the highest priority among all interrupting devices, the falling edge of DS sets the interrupt-under-service (IUS) flip-flop and the IP flip-flop is cleared. The data vector is then gated to the address bus as line Z goes low. Note that IEO is



Coupling cousins. Six-chip TTL interface joins popular Z8000 series of microprocessors with peripheral devices from other families, giving users extended facility. System thus becomes more readily adaptable for such tasks as parity checking and high-level diagnostics.

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held low by IUS throughout the interrupt service of the device, thereby disabling lower-priority devices.

■ Finally, as $\overline{\text{VIACK}}$ goes inactive (high), the outputs of the 74LS158 go to the inactive state. The same device will be prevented from interrupting its own interrupt because one of the inputs of the 74LS38 is disabled by the IUS flip-flop.

At the end of the interrupt, the return-from-VI ($\overline{\text{RETVI}}$) signal can be generated by the processor by programming it to generate an input/output write cycle in which the address is decoded and the signal will be run as a bus signal. The falling edge of $\overline{\text{RETVI}}$ releases the IUS flip-flop and IEO goes high. On the other hand, if the generation of a common signal such as $\overline{\text{RETVI}}$ is undesirable, the same function can be generated locally (decoding a unique I/O address for each interrupting device on the card) as the program initiates an I/O operation for resetting the IUS bit of the interrupting device. In the case where the IEI line goes low (as during an interrupt-acknowledge cycle with a higher-priority interrupt), the 74LS158's outputs go inactive, forcing IEO low. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

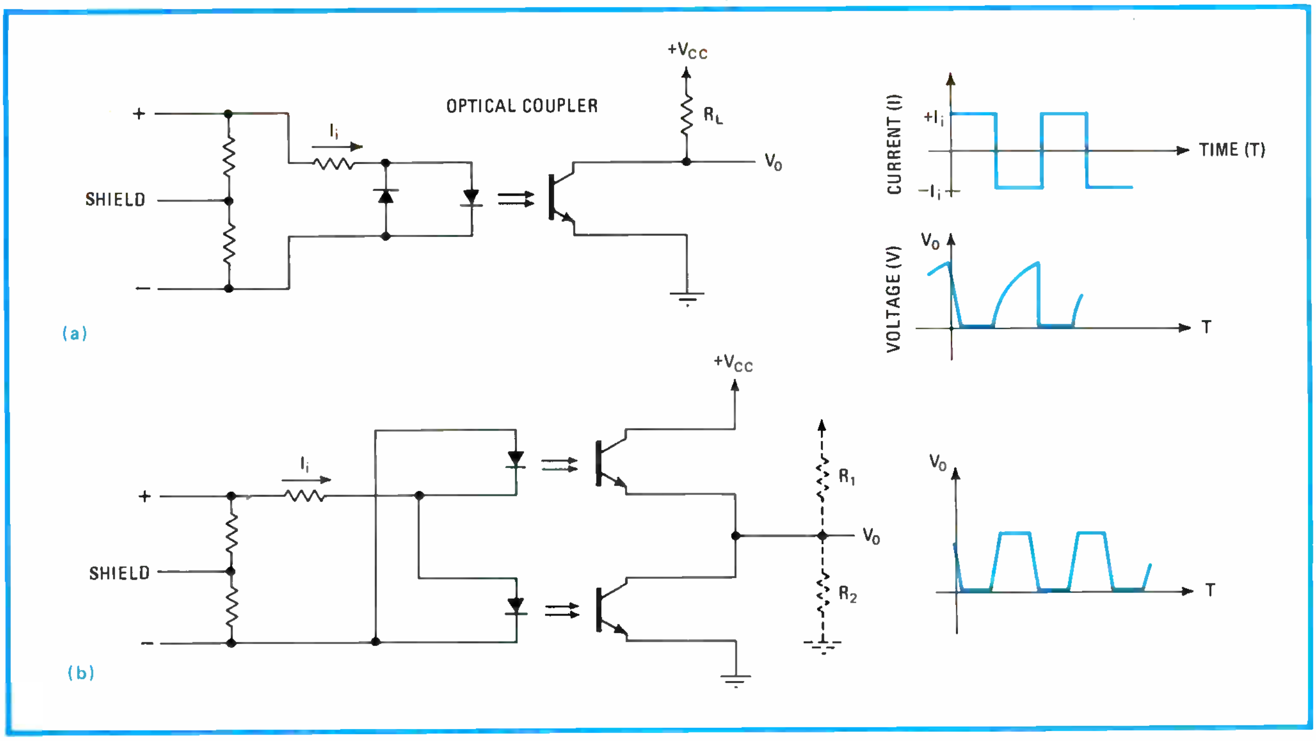
Twin optocouplers raise serial transmission speed

by Luis E. Murguis
Autotrol SA, Buenos Aires, Argentina

In a balanced 20-milliampere current loop for long-distance serial data transmission, optical couplers are a convenient way of connecting both receiver and transmitter to the transmission line, and provide isolation as well. However, an active pullup scheme employing an additional optical coupler at the receiver can improve transmission speed by an order of magnitude.

In the setup shown in (a), the fall time of the output voltage depends on the saturation current, I_i, of the coupler's input. However, the rise time of the output voltage, which determines the maximum transmission frequency, corresponds to the turn-off time of the coupler's output and is a function of load resistor R_L. Lowering the value of R_L raises the transmission rate, but only up to a limit set by the amount of current the optical coupler can handle.

Instead of trading off transmission speed and coupler loading, a second optical coupler produces a faster rise time and improves the transmission frequency almost 10 times over systems configured in the conventional way. The two optical couplers are connected as shown in (b) to produce an active pull-up and pull-down circuit at the output and thus speed up the output-voltage rise time. Both the rise and fall times are now a function of I_i, as the couplers alternate between their on and off states. Resistors R_1 and R_2 are optional and provide a fixed bias in case a circuit failure causes I_i to fall to zero. Another advantage of this circuit is that it improves fanout since a load resistor is no longer needed. □



Active output. A conventional, single-coupler design for a 20-milliampere current loop (a) limits the transmission rate because the signal rise time is a function of resistor R_L. Using two couplers in an active pull-up output (b) forces faster rise times and hence higher transmission rates.

Engineer's newsletter

Keep the IC waters pure

Control of ultrapure water systems will be the subject of an all-day seminar conducted by Balazs Analytical Laboratory on Aug. 20 at the Santa Clara (Calif.) Marriott Hotel. Hundreds of thousands of dollars are at stake, the Mountain View, Calif., company says, when the pure water system in a semiconductor fabrication facility fails. Contamination of the water can cause a steady loss in product yield or even halt an entire production line.

The seminar will cover every aspect of the water system, including filtration, sterilization, and common purification techniques. Potential malfunctions and how they can be avoided will also be discussed, with actual problems that occur in manufacturing serving as examples. For more information about the seminar, which costs $125, call Pat Westly, seminar manager, at (415) 494-7115.

Pull-up resistor protects furnace against overheating

Guillermo Mendoza of Audiotécnica SA, Mexico City, points out that V. J. H. Chin's circuit for regulating the temperature of an electric furnace using a thermocouple [*Electronics*, March 24, p. 136] can be made safer just by **adding a high-value pull-up resistor (1 MΩ, for example) between the +V supply voltage and the positive input terminal to the thermocouple.** In that way, if the thermocouple is accidentally disconnected or its junction opens up, the heating element is automatically turned off, thereby protecting the furnace against overheating.

Consider laser microsoldering for tough jobs

For a rough soldering problem like connecting a wire ribbon harness to a printed-circuit board, an integrated circuit in a dual in-line package to a Mylar flexible circuit, or a ceramic chip capacitor to a pc board, laser microsoldering might pay. Apollo Lasers Inc. offers **application notes on these three cases with details on the laser and the type of solder paste.** Write to the firm at 6357 Arizona Circle, Los Angeles, Calif. 90045.

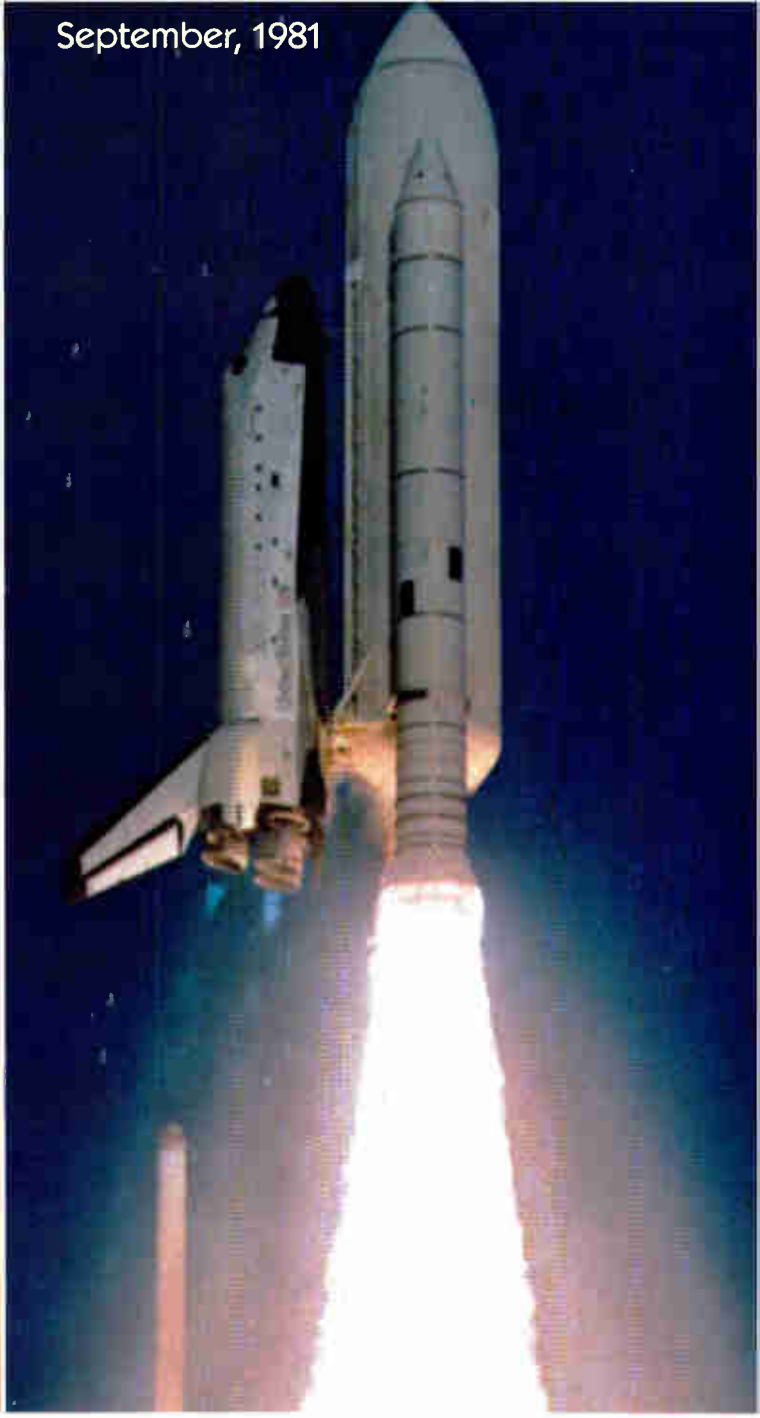
Special log book helps keep clean rooms clean

An ordinary laboratory notebook shouldn't be brought into a clean room, since its paper pages could conceivably generate enough static charge to zap a wafer full of costly integrated circuits. In addition, the paper could generate contaminating particles. Then, too, the paper could be damaged by chemicals and moisture. A special clean-room project log with pages of polyolefin-spun bond paper from MicRecord, San Jose, Calif., runs none of these risks, as the material is antistatic, chemical-resistant, and waterproof and will not generate particles. The log is distributed by VWR Scientific Inc., P. O. Box 3200, San Francisco, Calif. 94119.

Test results illuminate problems of multilayer boards

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has just released the results of its Fifth Multilayer Round Robin Testing Program. The program was used **to determine problems associated with materials, processing, and evaluation of multilayer printed-circuit boards and needs for future industry studies.** A three-year effort, it is the most complex testing ever undertaken by the institute's Multilayer Committee. A copy of IPC-TR-481 can be obtained from IPC headquarters at 3451 Church St., Evanston, Ill. 60203. The cost is $10 to members and $20 to nonmembers.

-Jerry Lyman



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Naturally, the 303S is compatible with all Fairchild Series 30 systems, so retraining is never a problem. And the 303S is backed by the largest service and support network in the industry.

If you're looking for a faster, easier and more accurate solution to in-circuit testing, take a closer look at the Fairchild 303S. It's got more speed, where speed counts most.

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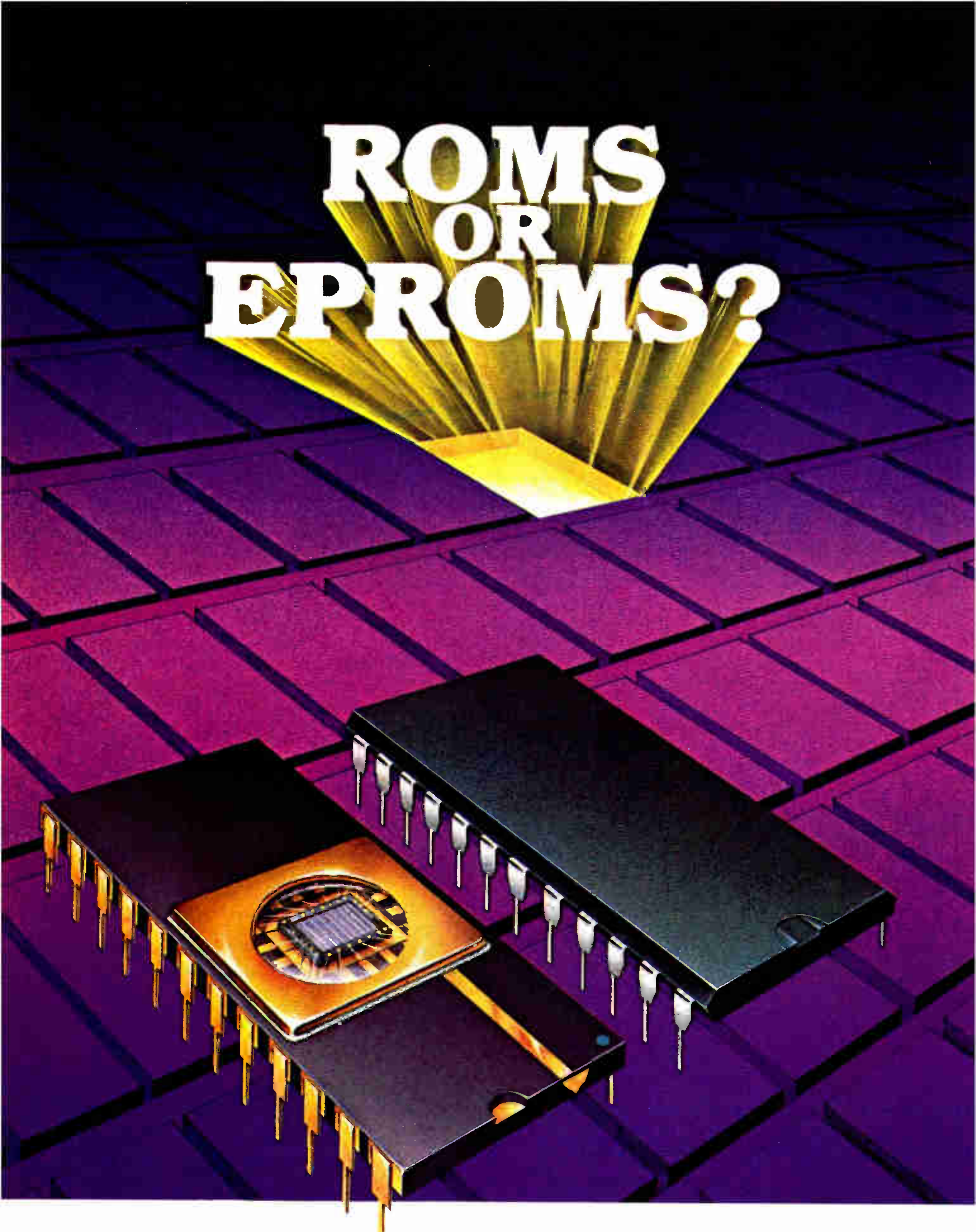

Interchangeable ROMs and EPROMs from Texas Instruments, the total memory supplier.

Here are tips from Texas Instruments on which to use when. Your decision may hinge on economics.

There are times when your system design will clearly dictate either ROMs or EPROMs. At other times, the dividing line between the two is hazy. That's when a careful analysis of the economics involved — particularly the recent substantial pricing changes in the marketplace — may tip you to one or the other with considerable long-term savings as a result.

Texas Instruments, a leader in non-volatile memories and a broad-based supplier, can deliver the byte-wide ROMs or EPROMs you need. And from its years of experience with these memory devices, TI offers suggestions that may help you decide on the least expensive solution for your system.

The case for ROMs

In general, ROMs provide more memory for less cost than any other semiconductor memory. The key to their use is high volume and high memory capacity — on the order of 32K and 64K. Coupled with programming — performed by the supplier — that will not change or need to be updated.

In these circumstances, ROMs are especially cost effective. Total costs are spread so widely that per-bit cost is relatively inexpensive.

Consumer and computer peripheral applications where the volume of end products is large can make very economical use of ROMs.

The case for EPROMs

Prices for 16K and 32K EPROMs have declined significantly, and those for 64K devices will follow suit. Making EPROMs economically attractive, especially for applications where the program is likely to change.

Programming is easily performed by the user, and there is no mask charge. One EPROM type can be used for many different programs. Which means lower inventory costs and no write-off costs when programs vary.

TI's High-Density ROMs

Device	Density	Power Dissipation*	Access Time*
TMS4732-35	32K	440 mW	350ns
TMS4764-35	64K	440 mW	350ns

TI's Leadership EPROM Family

Device	Density	Power Dissipation*	Access Time*
TMS2564-35	64K	840mW	350ns
TMS2564-45	64K	840mW	450ns
TMS2564-50	64K	840mW	500ns
TMS2532-25	32K	840mW	250ns
TMS2532-35	32K	840mW	350ns
TMS2532-45	32K	840mW	450ns
TMS25L32-45	32K	500mW	450ns
TMS2516-35	16K	525mW	350ns
TMS2516-45	16K	525mW	450ns
TMS2508-25	8K	446mW	250ns
TMS2508-30	8K	446mW	300ns

*Worst case over operating temperature range

If you are in a hurry to get to market, EPROMs can be your best bet. They are available from multiple sources on short lead times.

One additional advantage: Because of their programming flexibility, EPROMs are an excellent prototyping tool prior to conversion to ROMs. And, at the end of a product's life when both volume and the number of ROMs being used decline, converting back to EPROMs can cut costs.

The case for Texas Instruments

Whether ROMs or EPROMs or both, Texas Instruments fills your requirements with reliable, proven-in-the-marketplace memories that are fully compatible with each other.

A system designed with appropriate memory addressing can utilize TI's 16K or 32K EPROMs or TI's 32K or 64K ROMs on the same printed circuit board in the same 24-pin socket.

In ROMs, you have a choice of the high densities that spell economy — 32K and 64K (see table). These are fully static memories — no clocks, no refresh — that require only a single 5-V power supply. They are fabricated using N-channel silicon gate technology for utmost dependability. All inputs and outputs are TTL compatible. Maximum access and minimum cycle times are 350 ns.

In EPROMs, you have the broadest choice in the industry — 8K through 64K. All have the same basic pin configuration to ease memory capacity expansion.

Weigh the pros and cons of ROMs vs. EPROMs. Evaluate your system requirements and carefully check out the economics. Then call your nearest TI field sales office for prices and delivery on your choice. Of course, if you still have doubts about which is best for you, we are ready to consult with you at any time.

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48 Series standard plugs, ¾ actual size

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Three other hermetically sealed series —182, 348 (MIL-C-81511), 67—are available to meet your size, voltage, and contact density requirements.

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Circle 168 on reader service card

PBXs gear up for digital traffic

Seeing a potentially central niche in the office of the future, several firms announce private branch exchanges for voice and data

by Harvey J. Hindin, Communications & Microwave Editor

If the number of product introductions is the criterion, private branch exchanges that handle both voice and data traffic are the hottest item in the race to control the office of the future. As *Electronics* noted [April 7, 1981, p. 139], new entries are appearing at a rapid rate.

Typical of the recent crop is an integrated voice-and-data private branch exchange from the nation's second largest telephone conglomerate. According to principal engineer Barry Alper of GTE Telenet Inc., the firm's microprocessor-controlled subscriber data unit will hook up to existing GTE PBXs such as the models 1000 and 4600. It will use pulse-code modulation to switch synchronous data at speeds of up to 56 kb/s; asychronous data will be handled at speeds up to 19.2 kb/s.

Engineers responsible for data-communications networks cannot run right out, place an order for the GTE equipment, and get it quickly. As with most other voice-and-data PBXs, lead times are long. Alper says deliveries will start in June of 1982 and prices are not yet firm. They are, however, "expected to compare favorably with high-speed modems" in terms of price, he says.

The long lead times on the GTE and other announced systems are in line with the long period needed to plan and implement a data-communications network. Time is generally taken for field trials before orders go in for the millions of dollars worth of gear a net may require. If electronic offices are indeed "the shape of things to come," as Alper puts it, they must be cost-effective, and field trials offer proof. Westinghouse Electric Corp. in Pittsburgh will reportedly spend several months in 1982 testing one of the first GTE systems.

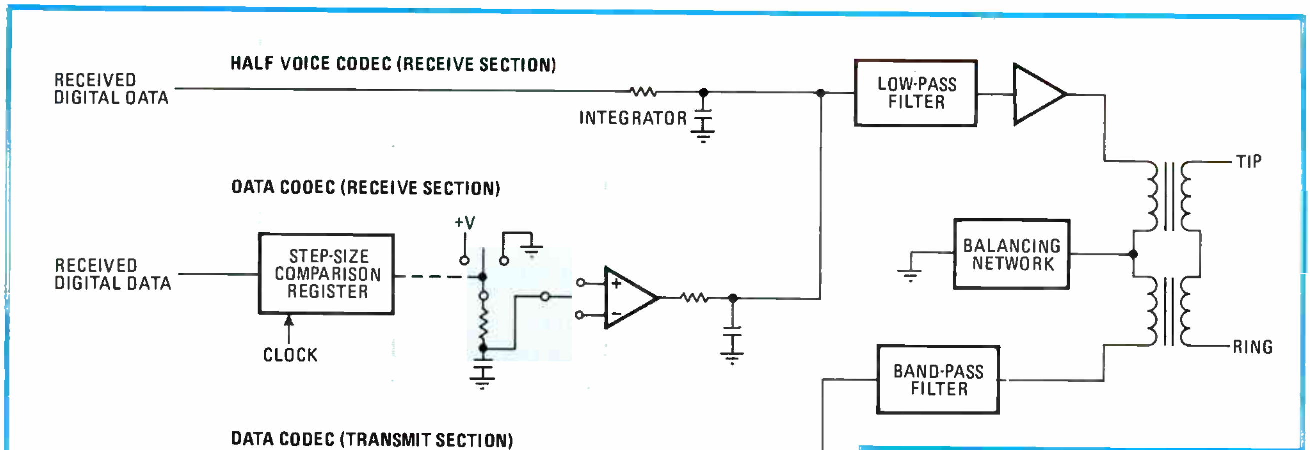
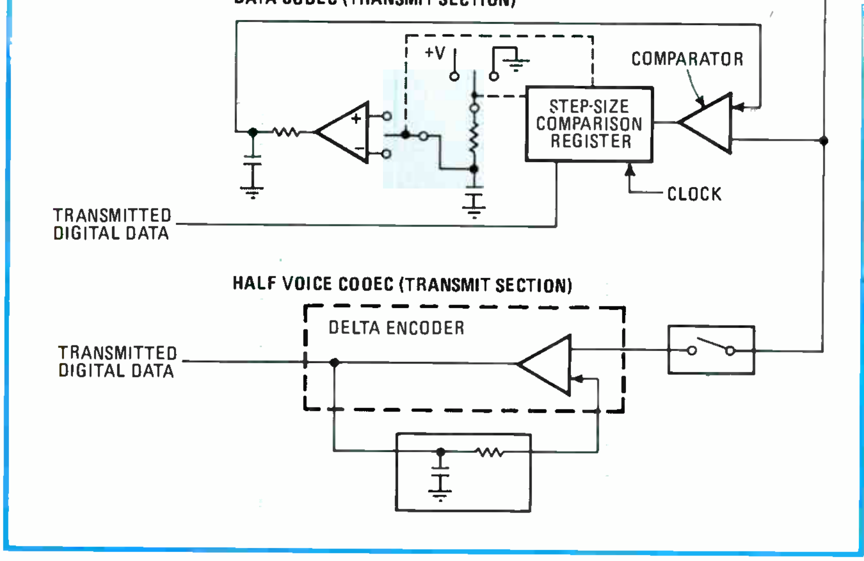
The subscriber data unit (SDU) is the heart of the GTE approach. It will accept inputs from word processors, facsimile equipment, computers, and other data-generating machines. It converts voice calls into digital signals, so that the PBX is digital from end to end. The GTE development requires the addition of what the company calls a data-access channel unit to plug into the PBX switching unit. And since the switching unit, the PBX's multiplexers, and the SDU need not be located in one place, the PBX can control a far-flung local voice- and data-handling network. This network in turn can interface with other networks through digital microwave, fiber-optic, or satellite links.

Since GTE's Telenet operation is geared to packet switching, the firm's new PBX will be able to interact with packet-switching devices. A large number of slow terminals may be attached to a packet switch, which frees the PBX for voice or high-speed data. The combined output of 100 or more slow terminals can then be made to occupy only one voice channel on the PBX instead of 100. The packet switch switches the group of slow terminals and passes the data traffic from them into and through the PBX by means of the SDU.

Harris Corp.'s Digital Telephone Systems operation has announced that its D1200 family of private branch exchanges now integrates voice and data switching at 9.6 kb/s. The only additional hardware needed is printed-circuit boards. Uniquely among the new offerings, the boards are available immediately and cost $475 per line or $675 per trunk circuit.

According to analog engineering supervisor Daniel Dillon at Digital Telephone Systems, the key to the capability of the add-on boards is a Motorola delta modulator with continuously variable slope. The modulator runs at the high clock speed of 112 kHz, enabling two 56-kHz voice channels to be used in the data mode to carry information through the PBX. "Filters without envelope distortion were designed to minimize pulse smearing and overshoot characteristics," Dillon says. "The high sampling rate simplified the design of the filter, allowing a gradual roll-off, yet retaining a great deal of attenuation at the sampling frequency. As a result, the bandwidth of 125 Hz to 5 kHz [3-dB points] is unusually broad and the envelope delay distortion is typically only 140 μs from

Data box. Each phone hooked to GTE Telenet's PBX gets a microprocessor-based subscriber data unit for connecting terminals.

Inside. The front end of Harris Corp.'s voice-and-data PBX uses a Motorola MC3418 delta-modulation codec and a voice codec custom made by AMI from a Harris design.

600 to 3,000 Hz." The data is "almost broadcast quality" in terms of distortion, according to the company.

Find out later. Unlike Harris, NEC America is being relatively close-mouthed about its Neax-22 series of PBXs. Like the other contenders for the office-of-the-future controller, the NEC offering will handle RS-232-C terminals interfaced with telephones connected to the PBX. The PCM-based system is expected to carry data internally at 56 kb/s and external asynchronous data at 19.2 kb/s. Prices are not available and delivery cannot be expected this year. Like the GTE system and others developed earlier, the NEC private branch exchange will be compatible with AT&T's standard T-1 communication channel, which has an overall data rate of 1.54 Mb/s.

As in other PBX designs, three-pair universal wiring can be used throughout the Neax-22 installation. One pair is for voice and the remaining two for data. The data module, which sits under the telephone, may be up to 4,000 feet from the Neax time-division-multiplexing switch. The system's end-to-end all-digital transmissions can be in either full- or half-duplex mode.

As if there were not enough choices, American Telecom Inc. and Telesciences Inc. are also offering voice- and data-handling private-branch exchanges. American Telecom has chosen delta modulation for its Focus III series of PBXs. Telecom is casting an eye at the large installed base (hundreds of thousands) of asychronous data terminals nationwide. In the first quarter of 1982, the company will accommodate these terminals at rates of up to 4.8 kb/s and a cost of $350 per line in a 700-station system, says James J. Marek Jr., director of product management for business systems.

Telesciences' X-80 PBX will use less-modern pulse-amplitude modulation for voice traffic (in this it is similar to AT&T's Dimension PBX) and a PCM scheme for digital traffic. The PBX will handle data at up to 9.6 kb/s at a cost of $600 to $800 per line; Telesciences plans to start production this year.

Anderson-Jacobson Inc. has a voice-and-data PBX that has been marking time in prototype for over a year. The firm has agreed in principle with the independent telephone company United Telephone Systems Inc. on a development, sale, and distribution proposal to get its PBX out on the market.

American Telecom Inc., 3190 Mira Loma Ave., Anaheim, Calif. 92806. Phone (714) 630-7721 [341]

Anderson-Jacobson Inc., 521 Charcot Ave., San Jose, Calif. 95101. Phone (408) 286-7960 [342]

GTE Telenet Inc., 1 Stamford Forum, Stamford, Conn. 06904. Phone (203) 357-2855 [343]

Harris Corp., Digital Telephone Systems, 1 Digital Drive, Novato, Calif. 94947. Phone (415) 472-2500 [344]

NEC America Ltd., 532 Brush Hollow Rd., Melville, N. Y. 11747. Phone (516) 752-9700 [345]

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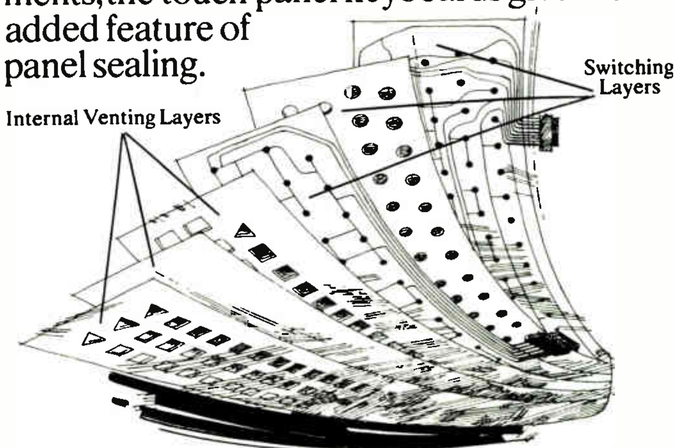

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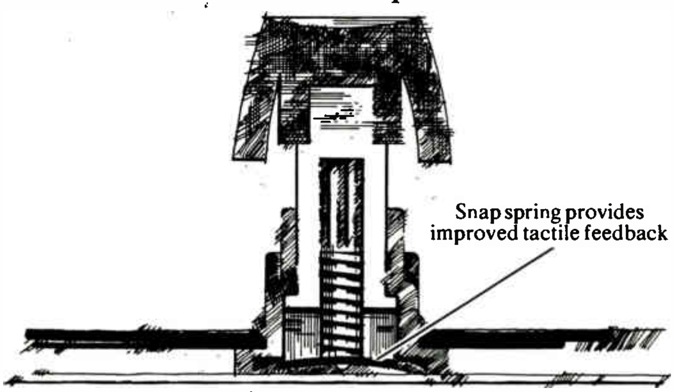

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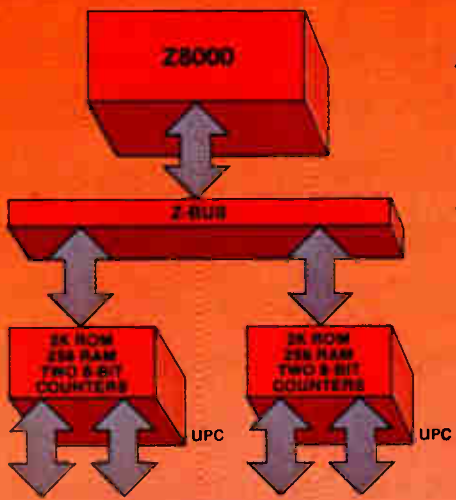
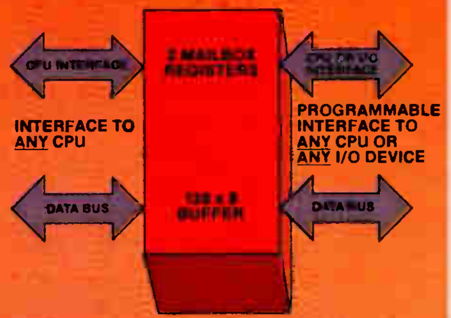


	ZILOG UPC Z8090	INTEL 8041	MOTOROLA 68120
On-board ROM	2K	1K	2K
On-board RAM	256 bytes	64 bytes	128 bytes
I/O lines	24	18	21
Counter/Timers	Two 8-bit or one 16-bit	One 8-bit	One 16-bit

FIO—**FIFO Input/Output Interface Unit—Z8038**—A programmable FIFO buffer designed for flexible subsystem interface, featuring message passing capability.

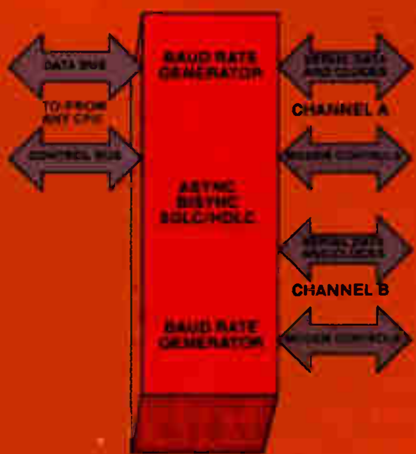


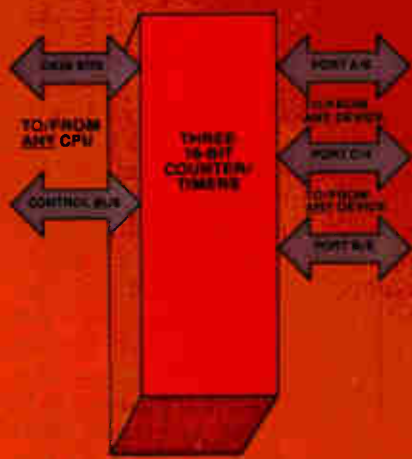
	ZILOG FIO Z8038	NO COMPETITION!!!!!!
Buffer Size	128 x 8 (expandable)	
Transfer Rate	1M bytes/sec.	
Buffer Between Multiplexed and Nonmultiplexed Bus	Yes-programmable for 12 different configurations	
Mailbox register for CPU messages	YES	

peripheral issue. will prove it to you.

SCC—**Serial Communications Controller—Z8030**—The industry's most versatile data communications controller featuring two full duplex channels capable of independent DMA transfer.

CIO—**Counter/Timer and Parallel I/O element—Z8036**—The optimum combination of I/O and counter/timers to provide flexibility for any application.





	ZILOG SCC Z8030	INTEL 8273 8274	MOTOROLA 68561
Async Byte-synchronous Bit-synchronous Capability	YES YES YES	NO (8273) YES YES	YES YES YES
Number of full duplex channels	2	1 (8273) 2 (8274)	1
On-chip baud rate generator	YES 2	NONE	NONE
NRZ/NRZI, FM/FM1 transmit receive capability	YES	NRZI ONLY (8273) MARK/SPACE ONLY (8274)	NRZ/NRZI ONLY

	ZILOG CIO Z8036	INTEL 8253/8255 COMBINATION	MOTOROLA 68230
Number of I/O lines with Hand-shaking	Two 8-bit ports or one 16-bit port (double buffered)	NONE (8253) Two 8-bit ports	Two 8-bit ports or one 16-bit port
Number of Count-er/Timers	Three 16-bit or one 32-bit and one 16-bit	NONE (8255) Three 16-bit (8253)	One 24-bit
Hand-shaking Modes	Interlocked, strobed, 3-wire pulsed	NONE (8253) strobed only (8255)	Interlocked, strobed
16-level interrupt priority control-ler	YES	NO	NO

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Low-cost S-100 card adds flexible I/O

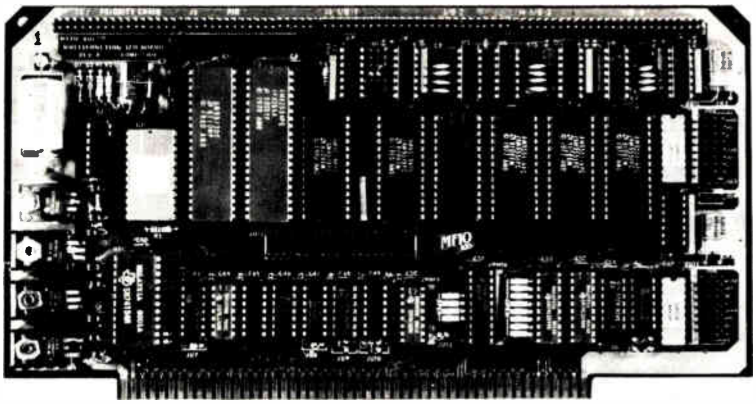
Multifunction input/output controller board has four serial ports, five timer-counters, and 16 levels of prioritized interrupts

by James B. Brinton, Boston bureau manager

Assembling an S-100 computer system can keep engineers awake nights. Depending on the number and type of ports, peripherals, and interrupts desired, original-equipment manufacturers often have to cobble up assemblies of several controller cards to obtain the flexibility they want. Having done so, they probably will have wasted backplane slots and some hardware, not to mention expending a lot of time on interrupt problems.

The MFIO-100 alleviates much of this agony. From Digicomp Research Inc., the multifunction input/output controller offers on a single, low-cost board: four hardware- or software- selectable synchronous or asynchronous full-duplex RS-232-C I/O ports with modem control and throughput to 19.2 kb/s; two, three, or four software-selectable, mode-programmable, 24-bit parallel I/O ports; and 16 levels of daisy-chained, prioritized, vectored interrupts with connection to all on-board devices as well as to interrupt commands derived from the S-100 bus.

Daisy chaining allows addition of other boards for an almost unlimited number of interrupts. The board also carries five 16-bit timer-counters that can be concatenated to reach lengths of 80 bits and whose outputs are available in binary or binary-coded decimal. A real-time clock with binary or BCD output, battery backup, and leap-year and day-light-savings-time features is optional.



The MFIO-100 is fully compatible with the IEEE's S-100 bus standard, IEEE 696; it is jumper-compatible with almost all existing pre-standard S-100 boards and systems, too. It operates as a module, occupying 32 consecutive locations in the I/O address space. It is not limited to use with any specific microprocessor running at any particular speed; it can accommodate 8- or 16-bit central processing units running at speeds of 6 to 8 MHz or more simply by using jumpers to insert wait states. Naturally, the subsystem recognizes both 8- and 16-bit I/O addresses.

The MFIO is able to pack all this functionality onto a single board through use of large-scale integrated circuitry from Intel, Motorola, and Advanced Micro Devices. At a unit price of $595, minus OEM discounts, Digicomp feels that the MFIO-100 probably has the most attractive price-performance ratio available in today's market.

The heart of the MFIO's serial-output capability is the AMD Am9551 programmable communication interface, a universal synchronous/asynchronous receiver/transmitter. The 9551 accepts data from the CPU, does a parallel-to-serial conversion, formats the data to conform with its programmed operating mode, and transmits it. The 9551s operate in a completely independent, full-duplex mode and contain all the electronics needed to control modems and printers over RS-232-C lines. Data control, operation, and format options all are under software control.

There are four 9551s on the board, and each can be addressed or put out interrupts separately. Also, the data rate for each can be individually set at from 50 to 19,200 b/s by hardware or software.

Parallel I/O makes use of the Intel 8255 programmable peripheral interface, a general-purpose device where 24 byte-oriented I/O lines may be deployed in a wide variety of ways. The options include: two 8-bit ports with handshake strobing, one of which can operate bidirectionally; three 8-bit ports without strobing; and a four-port configuration, with two 8-bit and two 4-bit ports without strobe. So the possible permutations are many. Inputs and outputs may or may not be latched, strobing is usually optional, ports can handle either data or control and status signals as needed, and finally, there is a strobed, bidirectional bus-oriented configuration that has interrupt generation and enable/disable functions available, among the

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The timer-counter centers on an Am9513 system timing controller, a LSI device integrating five general-purpose 16-bit up-down counters. A variety of internal frequency sources can be selected, as well as external pins as inputs to individual counters with software-selectable active-high or active-low input polarity. Outputs can be active-high or active-low and are available as voltage levels or pulses. Hardware- or software-controlled gating of each counter is standard, and the counters can be internally concatenated to form effective counter lengths of up to 80 bits.

The 9513 can be set up for one application or dynamically reconfigured under program control. Each timer/counter of the five can generate interrupts, and two of them have alarm comparators to flag accumulator counts.

Real time. The optional real-time clock is built around a Motorola MC146818 with a lithium battery backup and 50 bytes of random-access memory free for user data storage. Interrupts from the real-time clock may be selected for a given time, day, or date, or at any interval of from 122 μs to 1 hour.

Two Am9519s provide interrupt control; either can be programmed to have priority over the other; either can manage the masking, priority resolution, and vectoring of eight interrupts and can be expanded through daisy-chaining using on-board jumpers. Daisy-chaining can continue beyond the board.

The 9519s provide the CPU with any mix of responses between 1 and 4 bytes long, and the response bytes are fully programmable so that any desired vectoring, instruction, or addressing protocol can be used. The subsystem's direct-vectoring capability can be bypassed in favor of polling. The 9519s also can generate software interrupts.

The real-time clocks adds $95 to the $595 unit price for the MFIO-100. OEM discounts are available and delivery is in about one month.

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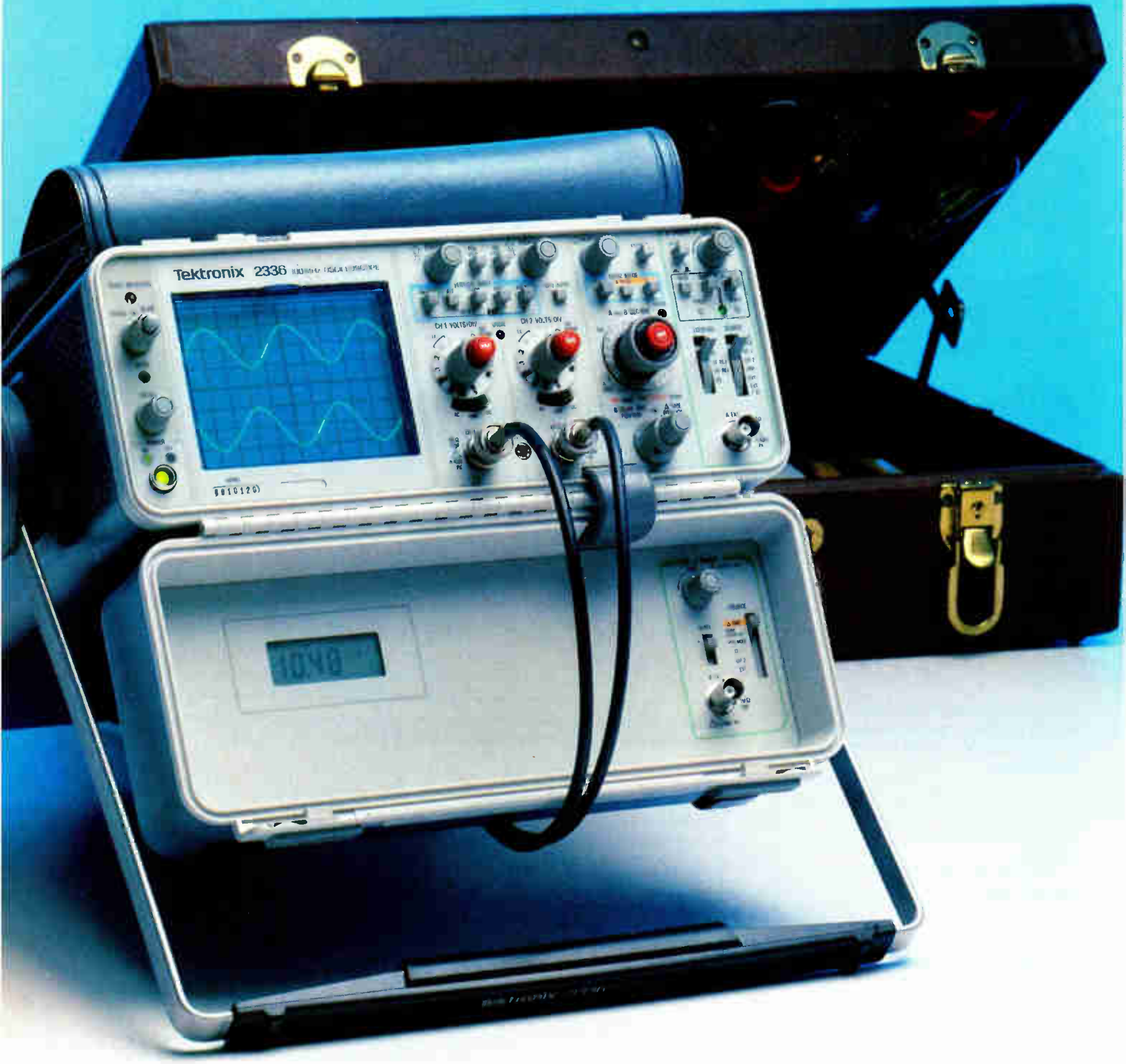

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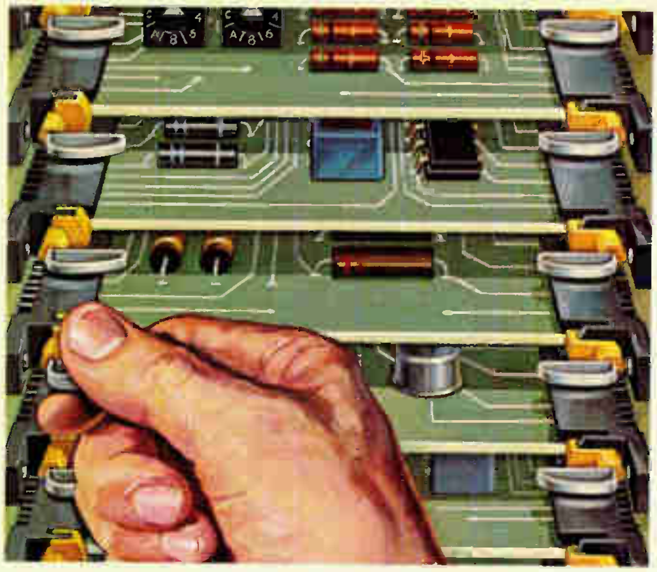

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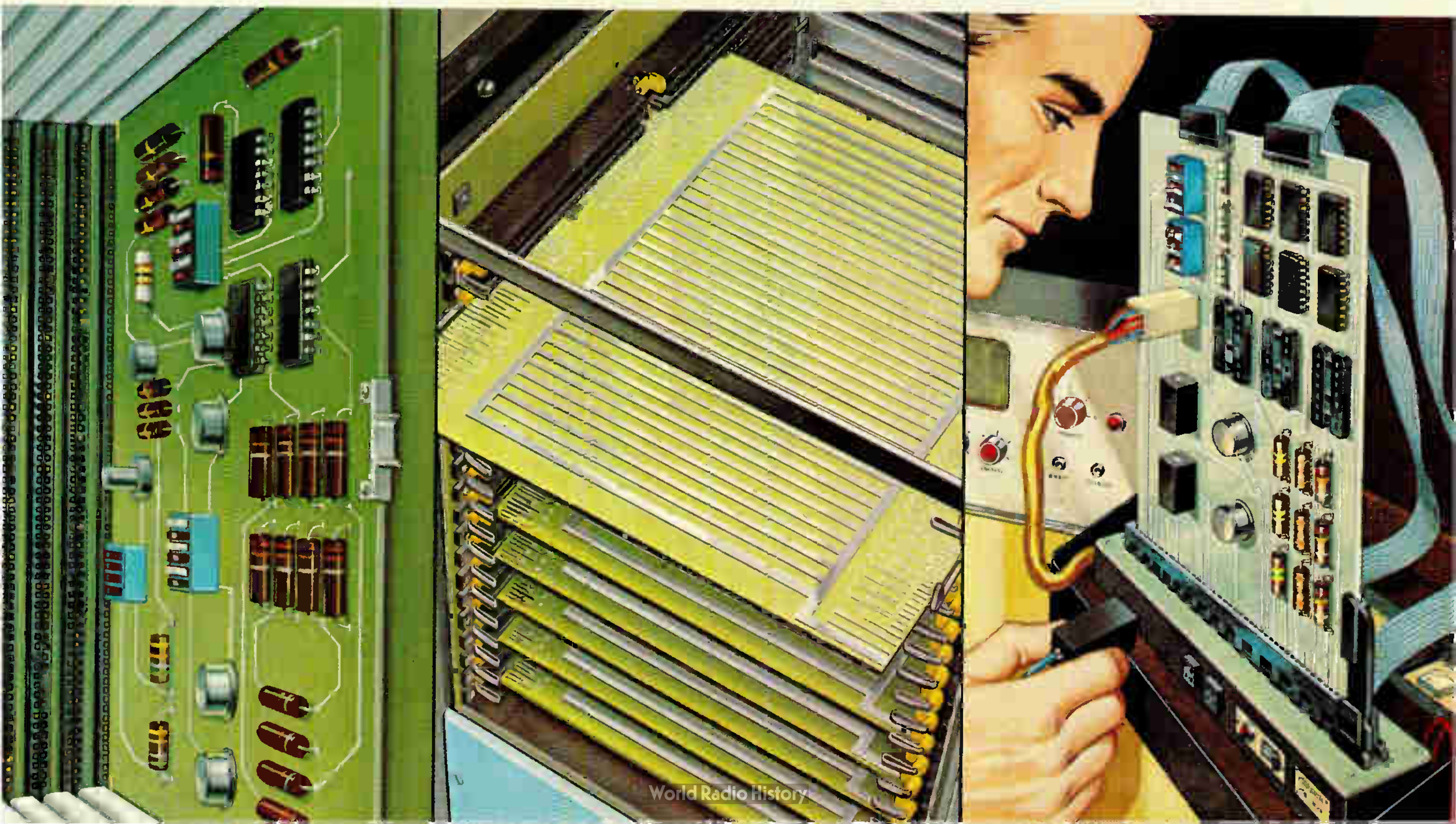

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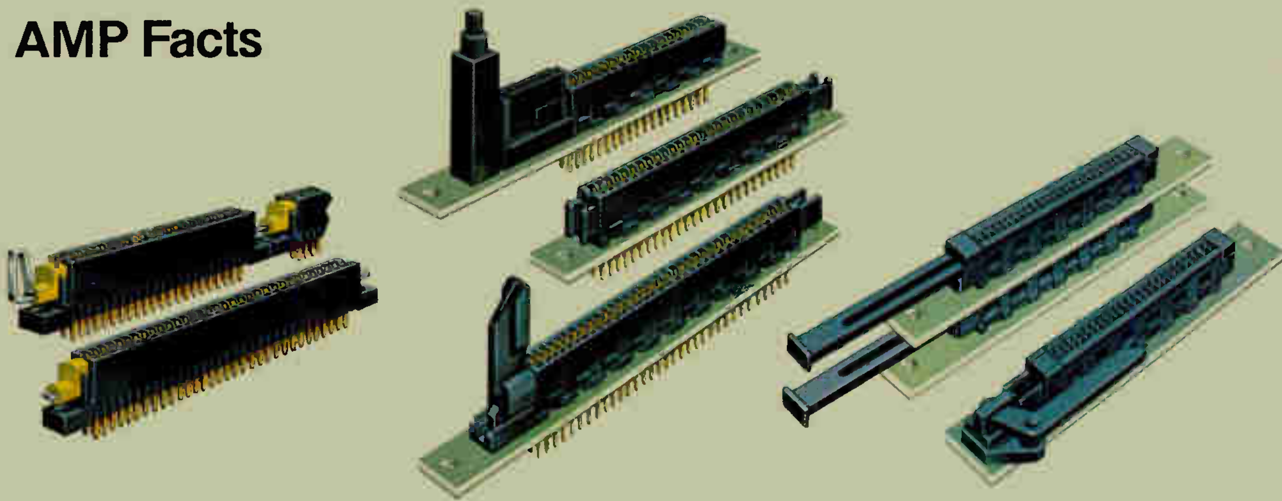

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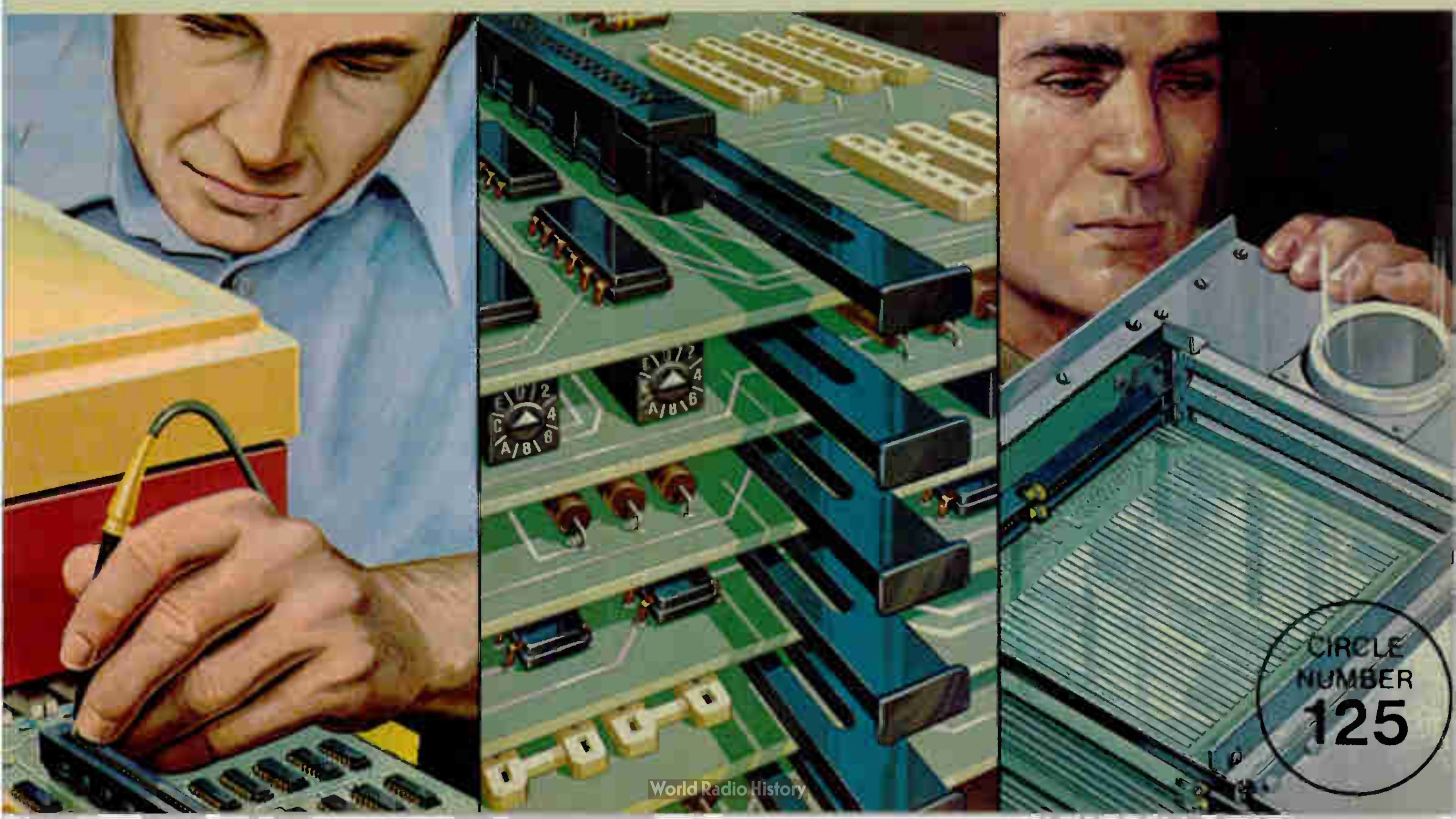

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Microcomputers & systems

ICE tests units with 8087, 8089

5-MHz ICE-86A version adds request/grant lines, data-type support for math, I/O chips

An enhanced version of the ICE-86 in-circuit emulator for 8086-based microcomputers allows debugging and testing of systems using an 8087 numeric processor that is closely coupled to the 8086. In addition, the enhanced ICE-86A supports the 8089 input/output processor, thus putting itself behind the entire iAPX product line.

The new emulator retains all the features of the ICE-86, which was introduced over two and a half years ago. These functions include complete access to user program symbols; single-step execution or real-time emulation at up to 5 MHz; triggered execution trace collection; breakpoints to halt real-time emulation; and user-defined emulation command macros and compound commands. Both emulators also permit memory mapping of user programs to the user's system, 2-K-bytes of high-speed ICE memory, Intellec system memory, or a diskette file.

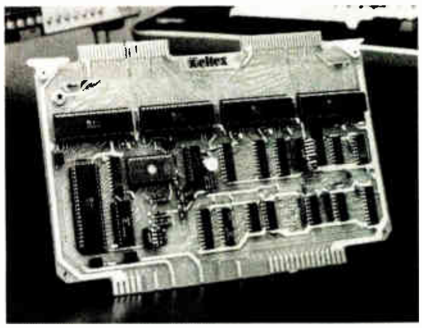
The enhanced ICE-86A adds emulation of both request/grant lines, allowing complete debugging of the 8087 or 8089 in local mode; integration of the RBF-89, formerly a separate product, for debugging systems that include an 8089 in local or remote mode; full support for 32-, 64-, and 80-bit 8087 data types (called Real, Dreal, and Treal, respectively) with the ability to enter or display data as decimal floating-point numbers; real-time tracing showing 8087 numeric instructions in disassembled form; and two additional emulation control lines on the ICE-86A buffer box that allow synchronization of the emulator with external events and equipment. Users can program in any of Intel's 16-bit languages: Pascal, PL/M, Fortran, or assembly language.

Upgrade package. In addition, an ICE-86U upgrade package provides a convenient upgrade path for current owners of the ICE-86 emulator. The addition of an ICE-86U upgrade converts any existing ICE-86 emulator to the new higher level of debugging support. Available now, the ICE-86A is priced at $6,500 and the ICE-86U is $1,800.

Intel Corporation, 5200 N. E. Elam Young Parkway, Hillsboro, Ore. 97123. Phone (503) 640-7792 [371]

6809 on EXORbus gets an IEEE-488 bus interface

The Z601 multifunction input/output board is compatible with the Motorola Micromodule and is designed for use with any 6809-based system using the EXORbus. It incorporates a real-time clock, programmable parallel I/O capabilities, and an IEEE-488 bus interface. The board extends the capability of the Motorola EXORset 30A for use as a data acquisition system, or as the basis for a production test system. All needed hardware and software for IEEE-488 interface are included on the Z601 to permit interfacing with instruments such as digital voltmeters, voltage standards, and frequency counters. For communications and user programming, the software is BASICM-compatible, and



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HP Series 80 Personal Computers for Professionals: HP-85 ($3250*) and HP-83 ($2250*) specifications: 16K RAM expands to 32K, 32K ROM expands to 80K; CRT with integrated graphics; (HP-85 only; built-in thermal printer, cassette tape unit). Software includes VisiCalc PLUS, Information Management, Graphics Presentations, Surveying, Data Communications (Fall '81), Statistics, Regression Analysis, Math, Linear Programming, Waveform & Circuit Analaysis, BASIC Training. HP peripherals include flexible disc drives, printers and plotters. VisiCalc™ is a trademark of Personal Software, Inc.
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four Synertek SY6522 interface adapters give the board bit-programmable parallel I/O, shift-register I/O, counter-timer, and clock generation capabilities.

The Z601 I/O board is memory-mapped into a contiguous 2-K address space, and all error messages are passed back to the user in a memory byte that is relative to the selected base. The $595 unit can be delivered in 60 days.

Zeltex Inc., 940 Detroit Ave., Concord, Calif. 94518. Phone (415) 686-6660 [372]

System design kit assembles microcontroller

The SDK-51 system design kit has the hardware, components, and software needed to assemble an evaluation and prototyping tool for Intel's MCS-51 microcontrollers. A monitor package, single-line assembler/disassembler, full ASCII keyboard, and light-emitting-diode display make up the SDK-51. The system monitor package offers utilities like command interpretation, user program debugging, and interface controls. The keyboard interface includes a 51-character ASCII subset, typewriter format, and a 12-key (3-by-4) matrix. The LED panel can display up to 24 alphanumeric characters. The kit includes 1-K byte of random-access memory; the board has space and circuitry for an additional 15-K bytes of RAM and 8-K bytes of read-only memory. And the kit also includes an Intel 8155 parallel input/output device to expand I/O

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capability by providing 22 dedicated parallel and TTL-compatible lines. The SDK-51 is $950, with delivery four to six weeks after receipt of order.

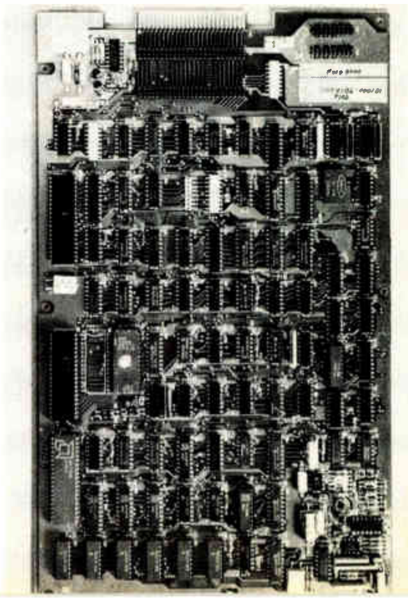
Intel Corp., 5200 N. E. Elam Young Parkway, Hillsboro, Ore. 97123. Phone (503) 640-7792 [376]

Controller board supports 2 Winchesters, 2 floppies

The FWD5001 single-board Winchester-plus-floppy-disk controller has a general-purpose interface compatible with the industry-standard Shugart 1403D controller. It is compatible with the SA1403D controller with respect to its hardware interface, dimensions, and connector. Existing products may use the FWD5001 in place of the other without changing power supplies.

Drives supported are the Shugart SA1002, SA1004, Quantum 2010/-2020/2030/2040 8-in. Winchester disks, plus the Shugart SA800/850 disks. A maximum of two Winchester and two floppy disks are supported to provide over 70 megabytes of storage for microprocessor-based systems. The FWD5001 features automatic error-correction and retry for both disk types. It requires a +5-V power source. Delivery is within 30 days; the unit is priced at $800 each in 100s.

Scientific Micro Systems Inc., 777 E. Middlefield Rd., Mountain View, Calif. 94043. Phone (415) 964-5700 [378]



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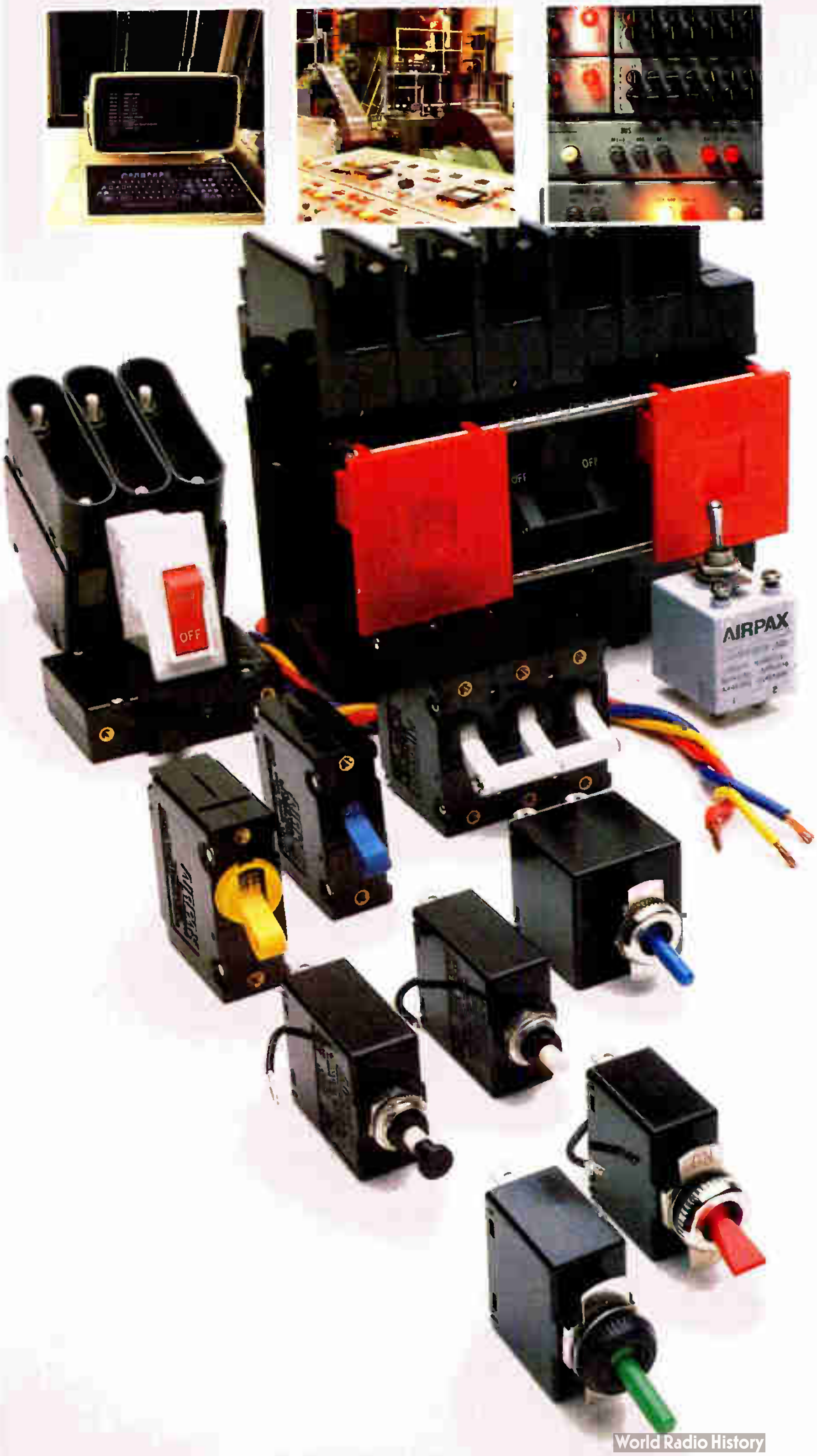

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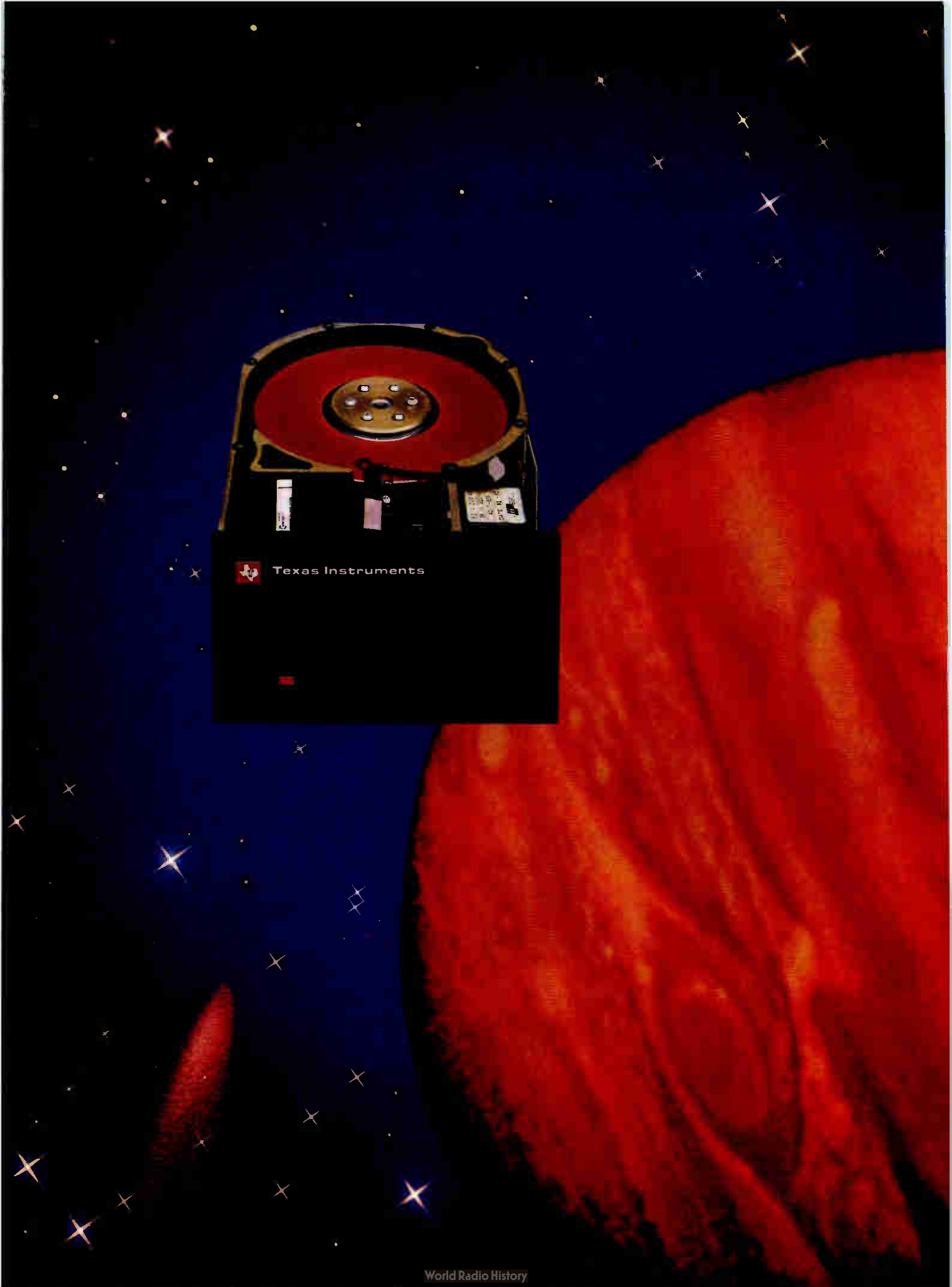
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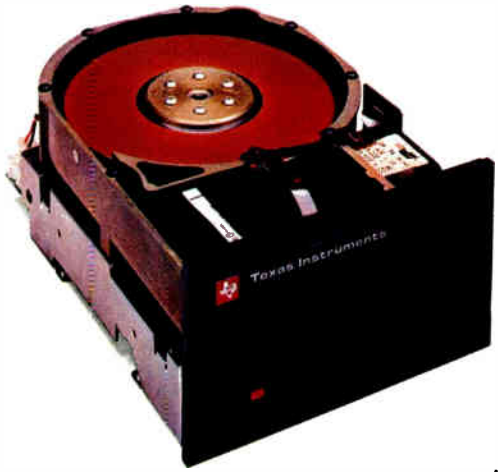

Announcing TI's new 5¼-inch Winchester Disk.

The future is now accessible with TI's new 5¼-inch mass storage disk featuring Winchester technology.

Now, a high-quality 5¼-inch Winchester Disk joins TI's growing family of terminal and peripheral products and offers a low-cost method of increasing information processing and data storage capabilities. It provides ideal storage support for small business and personal computers.

TI's 5¼-inch Winchester Disk is designed as a truly compact storage product and is packaged in the same size as an industry-standard minifloppy. This reliable disk can store up to thirty times as much data as a standard minifloppy at 6.38 million bytes per drive, access data approximately twice as fast as a minifloppy at a 170 milliseconds and transfer data nearly twenty times faster at 5.0 megabits per second. The speed and efficiency of most typical small scale system applications may be increased with the on-line capacity and performance of TI's 5¼-inch Winchester Disk.

Drive mechanics include a spindle mechanism, two 5¼-inch platters per drive and a stepper motor and head assembly with four read/write heads. Information can be written and stored on all four surfaces for maximum storage capacity. And, the disk's sealed nonremovable head/platter assembly provides maximum protection against external contaminants even in harsh application environments.

With built-in reliability, TI's 5¼-inch Winchester Disk is designed to offer an average of 11,000 Power-on Hours mean time between failures (MTBF). That means true dependability, minimal service and maintenance, and high-quality performance for meeting your storage requirements.

Reliability, big storage capacity and high-quality all at a low cost. That's what TI's new 5¼-inch Winchester Disk has in store for you.

TI is dedicated to producing quality, innovative products like the 5¼-inch Winchester Disk. And, TI's terminal and peripheral products shipped worldwide are backed by the technology and reliability that come from 50 years of experience.

For more information on the 5¼-inch Winchester Disk, contact the TI sales office nearest you, or write Texas Instruments Incorporated, P.O. Box 202145, Dallas, Texas 75220, or phone (713) 373-1050.

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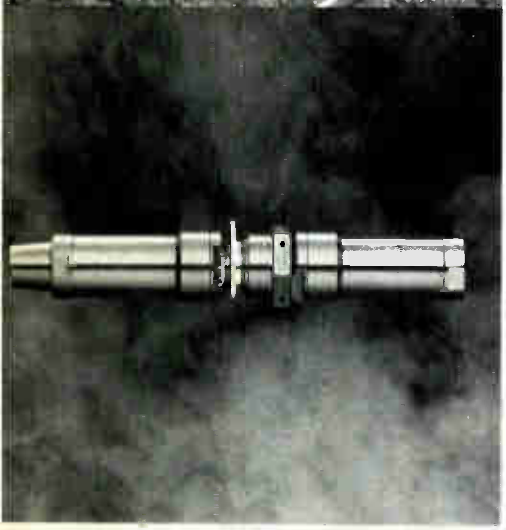

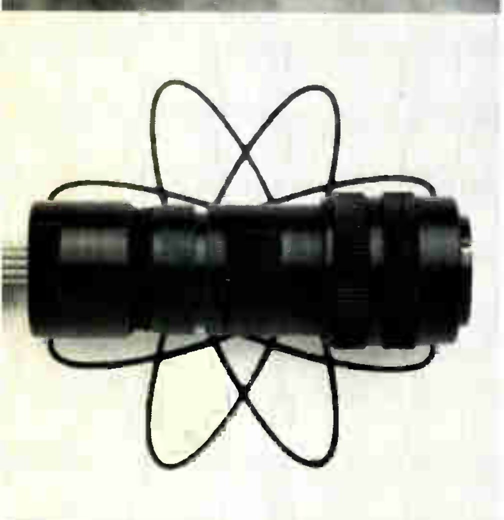

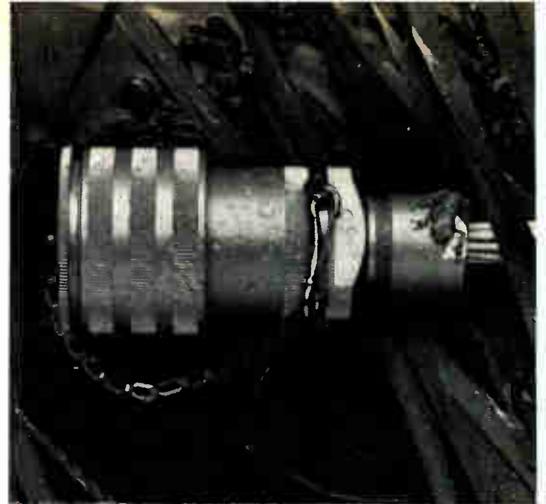

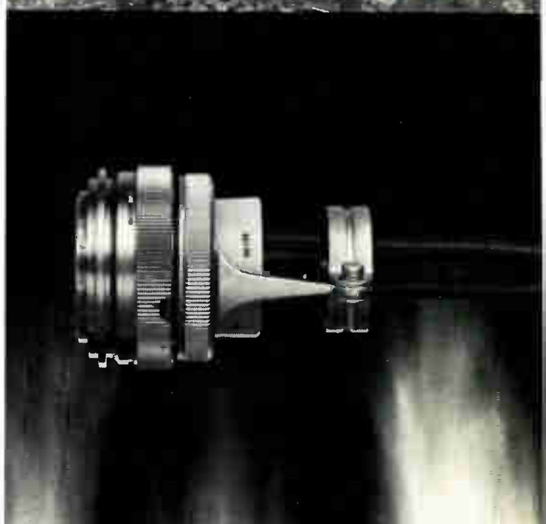

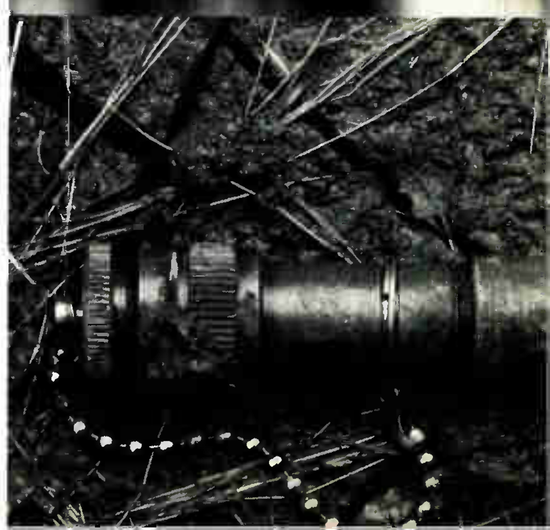

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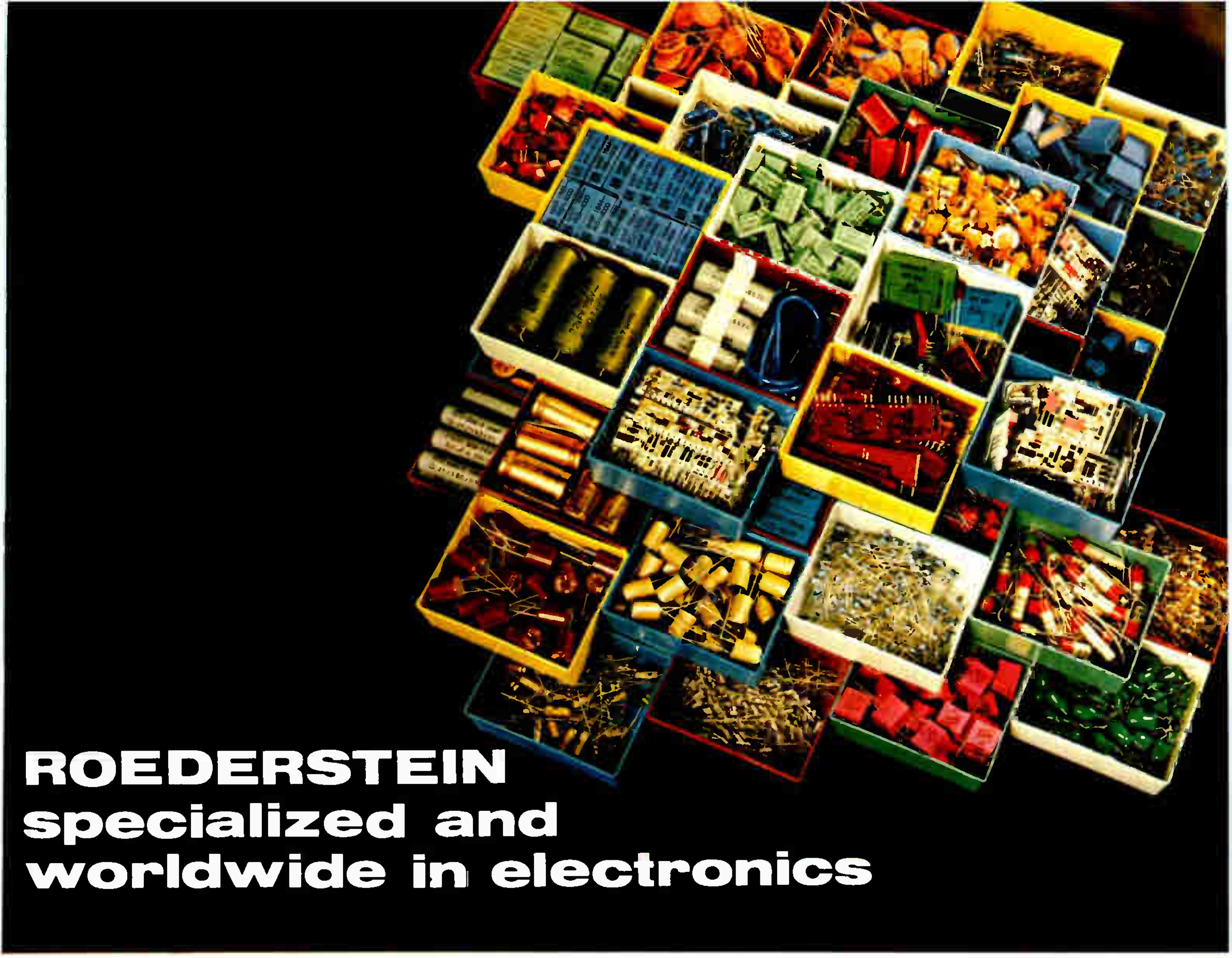

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Semiconductors

Tuning chip aims at cable-TV use

Frequency synthesizer's scanning channel input lowers device and system cost

A tuning chip for cable-television applications using up to 60 channels has been added to Motorola's line of integrated phase-locked-loop frequency synthesizers. The low-cost MC6195 stores channel-selection data in read-only memory and omits keyboard interfacing in favor of less expensive up- or down-scanning channel entry.

The n-channel MOS part is available now, priced at $2.50 each in quantities of 100,000, $4.00 in 1,000-unit lots. In like quantities, other members of the family, which support keyboard channel selection, are $3.50 and $5.22, respectively.

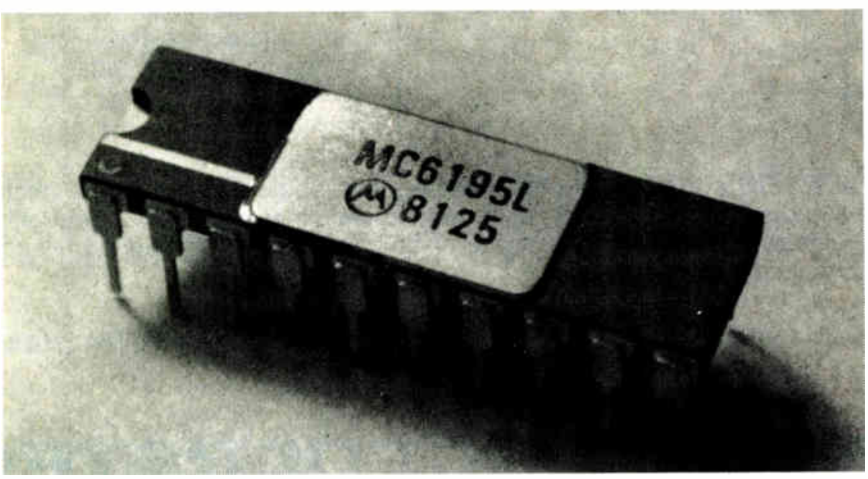
Members of the MC6190 family are designed to be the nuclei of digital tuning systems for cable TV converters and broadcast TV receivers. Each interfaces with a linear control chip and an emitter-coupled-logic prescaler to complete the tuning system. The PLL section of the 6195 has a 100-by-15-bit channel-conversion ROM that converts the channel number into the preset code for 12-bit prescaler dividers. The local-oscillator frequency is divided and compared to a reference frequency by a phase detector. The source of the reference frequency is an on-chip oscillator that uses either a 4-MHz or standard color-burst 3.58-MHz external crystal.

"This device provides a dedicated tuning function that is very cost-effective for PLL structures. And it's in n-MOS," says Allan Alaspa, a product planning manager for Motorola's Austin-based MOS Logic group. Spurred by the television industry's switch from mechanical channel selection systems to digital components, he continues, Motorola's MOS TV tuning operation "is moving into more of a large-scale integrated function, which combines the PLL with the control logic, keyboard interface, and display interface."

The 6195 features remote-control capability for power on-off control and for channel scanning. The device provides binary-coded-decimal channel data to the external light-emitting-diode display drivers.

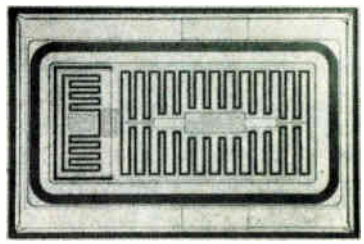
More coming. A seventh member of the PLL synthesizer family, the MC6196, will be introduced in five months, Alaspa discloses. It will be targeted at cost-effective broadcast-frequency TV applications. "Motorola is putting a tremendous emphasis on a whole family of devices to attack this TV market," says Alaspa. "We will be coming out with a family of devices with programmable cores—allowing us to offer programmable features as well as programmable frequencies."

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6369 [411]



Dielectrically isolated power Darlingtons switch in 2 μs

Dionics' PDI-4 dielectrically isolated power Darlington transistors increase reliability and lower assembly costs. Because dielectric isolation completely isolates the chip from the substrate, the assembler can eliminate the use of expensive ceramic such as beryllium oxide. The new



npn series of chips is housed in TO-220 packages. They feature continuous and peak collector currents of 1 and 2 A, respectively. The open collector emitter voltage (dc) base is 400 V, and the open collector-base voltage (dc) is 450 V minimum. Additional features of the PDI-4 include a dc current of 75, a saturation voltage of 1.7 V at 1 A, and a typical switching speed of 2 μs. Operating and storage temperatures are from −50° to +150°C. The transistors, 100 by 150 mils and gold-backed, start at $4.50 in 100s. Delivery is six to eight weeks.

Dionics Inc., 65 Rushmore St., Westbury, N. Y. 11590. Phone (516) 997-7474 [413]

8-bit microcomputer has register-file architecture

The PIC1670 8-bit microcomputer is a single MOS large-scale integrated circuit containing random-access memory, input/output, and a central

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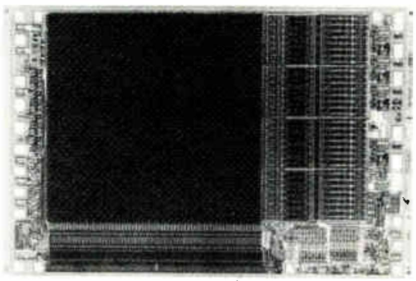
processing unit, as well as a customer-defined read-only memory. The firmware architecture is based on a register file concept with instruction commands designed to optimize the code for bit, byte, and register transfer operations. The instruction set also supports computing functions. The PIC1670 is equipped with a sophisticated interrupt structure and versatile self-contained oscillator that requires only an external crystal or RC network. The 1670 has an instruction execution time of 1 µs and a wide power-supply operating range of 4.5 to 5.5 V and is available with two temperature ranges, 0° to +70°C or −40° to +85°C. The chip, fabricated with n-channel silicon-gate technology, is under $5 in orders of 50,000 units. It is available now with a 12-week delivery time.

General Instrument Corp., Microelectronics Division, 600 West John St., Hicksville, N. Y. 11802. Phone (516) 733-3120 [414]

4-K-by-4-bit bipolar PROM sports 35-ns access time

The Am27S40/41 is a 4,096-by-4-bit bipolar programmable read-only memory. The Am27S40, with open-collector outputs, and the Am27S41, with three-state outputs, sport a maximum access time of 50 ns in their standard versions and 35 ns in the ultrafast A versions. A three-state power-switched Am27PS41 relieves system power problems by



reducing power consumption from 875 to 425 mW when deselected. The PROMs, in 20-pin dual in-line packages with rows on 300-mil centers, use AMD's proprietary advanced ion-implanted micro-oxide technology, IMOX II, are made with dual-layer metal and washed-emitter processing, and have platinum silicide fuses. They comply with MIL-STD-883 and have a 97% programming yield. Design features include active loading of all critical ac paths regulated by a built-in temperature- and voltage-compensated bias network to provide parametric stability over the commercial and military power-supply and temperature ranges. Pricing starts at $44.90 each for orders of 100 units or more.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94086. Phone (408) 732-2400 [416]

Solar panel array generates 10 to 15 A at nearly 5 V

The Powerline series of high-density photovoltaic panels are designed for multikilowatt solar power systems. Built with Solarex's Semix semicrystalline silicon technology, the panels offer features that eliminate many problems of large-scale photovoltaic arrays, particularly those caused by reverse-bias operation. Seventy-two 10-by-10-cm semicrystalline silicon solar cells are wired in a fully redundant 12-series 6-parallel arrangement to provide alternative current paths if one cell or interconnection is disturbed. In addition, multiple interconnection points across the back of each cell improve reliability and ensure current collection even from a cracked cell.

The panels, available in a range of power levels, generate 10 to 15 A at nearly 5 V. An array of three type PL-110 panels is rated at 200 W (peak) to deliver approximately 13 A at 15 V in full sunlight. It can produce approximately 1 kW-h per day in locations with favorable climates. The price for the array, including mounting hardware, is $3,000, with quantity discounts available. Delivery takes 30 to 60 days for a single panel and 90 days for a system. In addition, the company offers custom-designed accessory equipment.

Solarex, 1335 Piccard Dr., Rockville, Md. 20850. Phone (301) 948-0202 [417]

The "GE" in "GEM" assures you of the most capacitor value.

GEM metallized, high-performance capacitors offer you the most efficiency . . . in a compact size with reduced weight. And the lowest dielectric losses, resulting in important operating economies.

GEM capacitor superiority is not surprising when you consider the source . . . General Electric. The company with a worldwide reputation in research and development. A leader in capacitor technology. The manufacturer with the largest capacitor production facility in the world.

GEM capacitors are readily available from GE with a breadth of technical support and service backup no other company can match.

In short, you cannot find a better capacitor value anywhere. A new GEM information package gives details of the GE quality story and documents the reasons why users of GEM capacitors enjoy a wide range of benefits. Write today for your free copy. GENERAL ELECTRIC COMPANY, Capacitor Products Department, Hudson Falls, N.Y. 12839.

Our Capacitors Perform Best Because We Do.

GENERAL ELECTRIC

Time for CMOS Microboards.

We've added a timer to our $99 Microboard computer...and it still costs only $99.

Our new timer has a programmable period of 7.6 μsec to 64 seconds.

Operates in 6 modes:

- Square wave output.
- Re-triggerable one-shot.
- Re-triggerable one-shot with time-out feature.
- Software- or hardware-triggerable.
- Output available as system interrupt or flag input.
- External output and control.

Expanded temperature range. The timer isn't all that's new. The temperature range has been expanded: now it's from **-40°C** to **+85°C.**

And we've increased our RAM to 1K bytes.

Of course we've kept everything from the original:

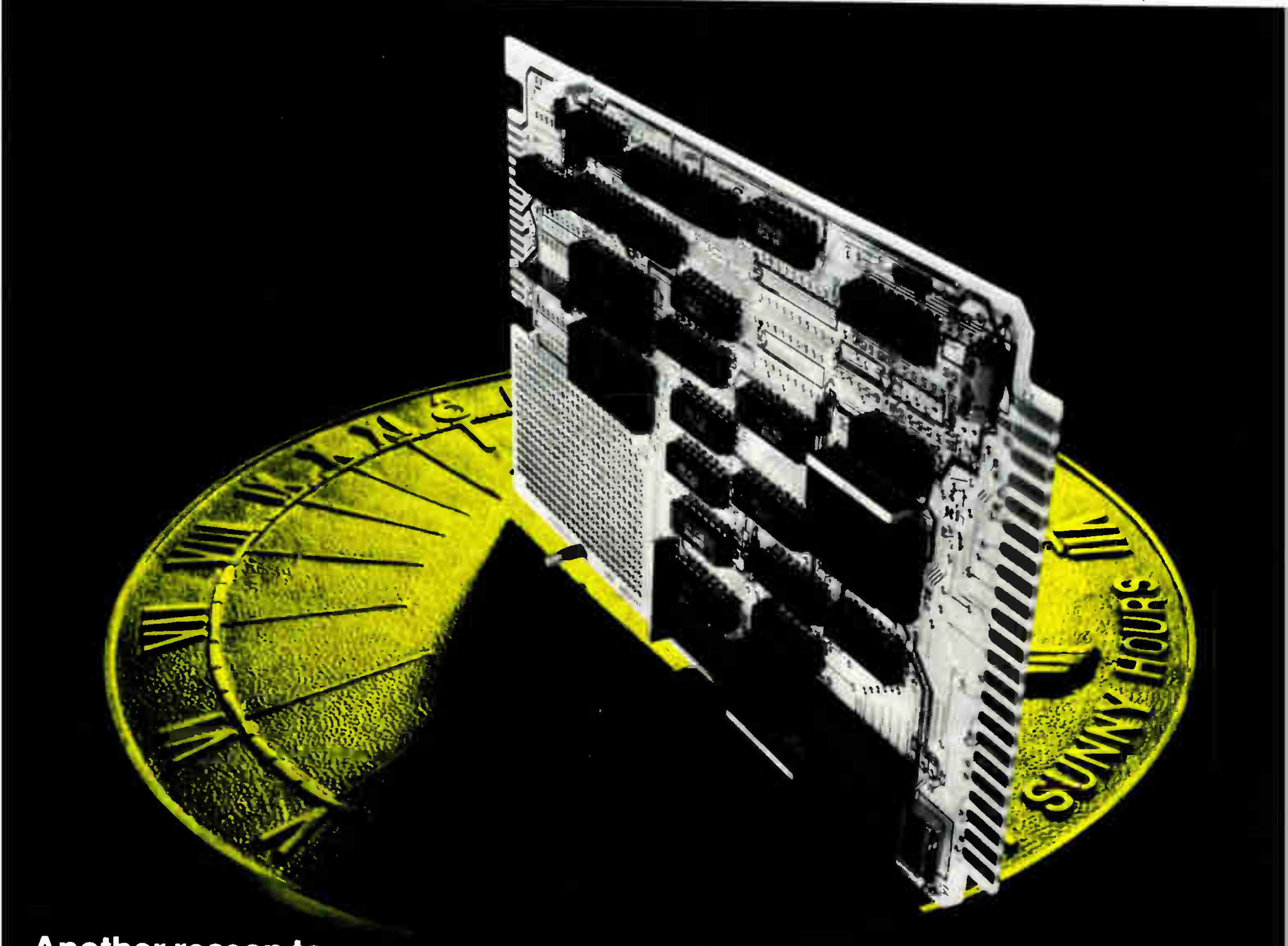
- 1802 microprocessor.
- Socket for 1K, 2K or 4K of ROM/EPROM.
- 21 parallel I/O lines.
- Convenient user breadboard area.
- Ultra-low power consumption (typical 4 mA @ 5.0 volts).

At $99,* the original was a bargain. At $99,* our enhanced CDP18S604A Microboard computer is a steal.

For more information on our full line of Microboards, contact any RCA Solid State sales office or appointed distributor.

Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong. **Or call Microsystems Marketing toll-free (800) 526-3862.**

*U.S. optional distributor resale, 100+ price.



Another reason to switch to CMOS.

Circle 204 on reader service card

RCA

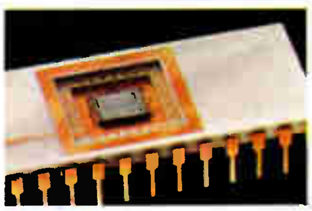
Circle 205 on reader service card

NCR - NON-VOLATILE MEMORY GUIDE

NCR Device No	Organization	Type
ER2051	32x16	Word alterable ROM
ER2055	64x8	Word alterable ROM
ER1400	100x14	Word alterable ROM
SR1734*	256x8	Non-volatile RAM
ER3400	1024x4	Word alterable ROM
ER2811	2048x4	Electrically alterable ROM
ER2168*	2048x8	Electrically alterable ROM
ER2161*	2048x8	Word alterable ROM

*Pin conservative bus structured devices

Now, you can draw on NCR's experience for NV-RAMs and in-circuit programmable ROMs.



NCR, pioneer of MNOS technology, now offers you the NV-RAMs and EAROMs we manufacture and use ourselves. These are the same memory devices used in NCR's broad product line—from electronic cash registers to self-service banking terminals.

With NCR non-volatile memory devices, you can choose the appropriate capability for your particular application. Our NV-RAMs give you protection of critical data for 30 days in a power down sequence.

Electrically alterable ROMs from NCR, with in-circuit programmability, give you reduced turn-around time and cost for ROM data pattern changes—especially for system development. Plus, our EAROMs—with bit densities from 512 to 16,384—are either block or word-alterable (WAROMs). In either case, memory is protected for up to 10 years.

But we don't stop with giving you choices. We give you reliable chips fast at competitive prices. In fact, we can meet many of your needs right off the shelf. We can do all of this because our continuing investments in semiconductor production facilities and technology mean we're in the business to stay.

For evaluation samples and details on how our experience as a user and manufacturer of non-volatile memory devices pays off for you, call Dave Major, at (800) 543-5618, in Ohio (513) 866-7217. Or write to Dave. His address is NCR Microelectronics Division, Box 606, Dayton, Ohio 45401.

NCR
Complete Computer Systems

Circle 207 on reader service card

New products

Industrial

Time-delay relay covers wide range

Multiple-range unit times 20-ms-to-30-min delays, reduces inventory costs

Able to span a delay-time range as wide as 20 ms to 30 min, the 319D series of adjustable multirange time-delay relays from Automatic Timing and Controls Co. are perhaps the most versatile on the market right now. They "probably replace a couple of thousand different units" and thereby reduce the costly inventory that must be kept when these devices are used, says marketing vice president Vincent McMahon.

The 319D, which comes in either three- or five-range models, meets the form, fit, and function of other octal-based time-delay relays and ranges on it can be simply changed by pulling out a knob and turning it.

The adjustable relays offer much more design flexibility than do fixed-delay relays. "Being able to change the delay time in a finished product gives engineers an important adjustment that can compensate for variations in their products' performance," McMahon points out.

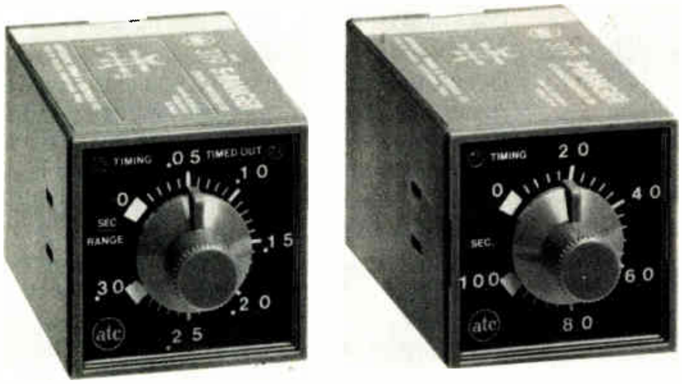
When a start switch is closed, a complementary-MOS relaxation oscillator is activated in the 319D and a light-emitting diode indicates that the unit is timing a delay. When the oscillator count is equal to a level that was set by the range switch, a load relay is energized and the LED turns off. The timing circuit is automatically de-energized. A second LED in the five-range version turns on when the load relay is energized and off when the start switch is opened or power is interrupted.

Worst case. The 319D maintains a worst-case repeat accuracy of within ±6% of setting, or 2 ms, over line voltage swings between 95- and 132-V ac and a temperature range of 0° to 70°C. Setting accuracy is to within ±10% of full scale. The unit's C-MOS timing circuit is not subject to the large error that plagues many electronic time-delay relays after long periods of disuse.

The 319D-016 has five ranges from 0.3 s to 30 min full scale and is available for operating voltages of 24, 120, and 240 V ac and 24 V dc. It lists for $46. The three-range 319D-134 has full-scale ranges of 1, 10, and 100 s and operates at 24 V dc and 120, and 240 V ac. It is priced at $41.

Both units operate only in the on-delay mode and switch a double-pole, double-throw load relay rated to handle 5-A resistive loads. Delivery is from stock.

Automatic Timing and Controls Co., King of Prussia, Pa. 19406. Phone (215) 265-0200 [391]



Power-factor controllers cut energy costs by up to 60%

Members of the ES-3 line of power-factor controllers for three-phase motors rated at up to 50 hp can cut power costs by as much as 60%, says their manufacturer. The controllers save power by automatically adjusting motor voltage to match load requirements while maintaining full motor speed and available torque. The units also protect motors from line-voltage variations.

The ES-3 comes in nine standard models for direct wiring to 230-, 460-, and 575-V three-phase motors with power ratings of 5 to 50 hp—up to 60 A. All have as standard a reduced-voltage starting (soft-start) feature but can be adjusted in the field for full-voltage starting. They are packaged in rugged wall-mountable cast aluminum enclosures measuring at most 9⅞ by 8⅛ by 6¾ in. deep and range in price from $490 to $1,140. They come with a one-year limited warranty against manufacturing defects. Delivery is from stock to two weeks.

Nordic Controls Co., 155 N. Van Nortwick Ave., Batavia, Ill. 60510. Phone (312) 879-7500 [393]

PWM servo-motor amplifier has extensive diagnostics

The A663 series pulse-width-modulation servo amplifier is designed to drive efficiently any dc motor, within the limits of its output ratings—a peak ±60 A (±30 A continuously) at ±120 V (±112 V continuously). It boasts extensive diagnostic features and open-collector TTL outputs to relay fault data to a computer. The digital outputs are joined by individual light-emitting diodes indicating overvoltage, overheating, shorts across the output or to ground, low dc bus or bias power, excessive current, and system oscillation.

The amplifier is designed for robotics, machine tools, or any automatic

ULTRA-PURE SIGNAL. ULTRA-WIDE RANGE.

THE 1618 MICROWAVE SYNTHESIZER. FROM SYSTRON DONNER.

Frequency range 50MHz to 18GHz.
The Systron Donner Model 1618 synthesizes fundamental frequencies from 2 to 18GHz. And a simple option extends that range down to 50MHz.

Resolution over the full range is 1kHz. And with external input, it goes as low as 1Hz.

Signal harmonics better than 50dB below the carrier.
The 1618 Microwave Synthesizer provides substantially greater spectral purity than its closest competitor. Internal filtering insures harmonics better than 50dB below carrier in the standard 2 to 18GHz range, and 40dB below carrier from 0.05 to 2GHz. Non-harmonic spurious levels are better than 50dB down throughout the entire range.

Synthesizer and all options fit in one instrument.
The 1618 provides you with one totally self-contained instrument package, measuring 5¼" x 16" x 22". All eight options may be accommodated with no increase in size. And the 1618's use of plug-in modules and off-the-shelf components makes servicing simple.

Optional internal pulse modulator.
A PM option permits very high speed pulse amplitude modulation: 20ns rise/fall time. And typical on/off ratios are 80dB, 2 to 18GHz.

The 1618 also lets you select combined modulation modes for very complex outputs, in manual or remote operation.

AM depth to 90%.
Set amplitude modulation depths to 90% at rates up to 100kHz with a simple front-panel control.

For FM applications, modulate the r.f. output at rates of 50kHz to 1MHz, with peak deviation greater than 1MHz.

Control r.f. output levels by an output step attenuator, with 10dB steps, and by a multi-turn level vernier. The calibrated output level is directly displayed in four digits, with 0.1dB resolution.

IEEE-488 interface is standard. Simple, flexible programming.
This interface provides you with remote control of all basic front panel functions. And 1618 programming combines flexibility with a logical, simple entry format. During remote control five LED annunciators display operating status and modes.

Clearly, the 1618 leads the field in range and purity. Find out more. Call us or send in the coupon. We'll rush you complete product literature—along with a list of our representatives in your area.

SYSTRON DONNER E72881
INSTRUMENT DIVISION/MS1
2727 Systron Drive, Concord, CA 94518
Phone: (415) 676-5000
TWX: 910-481-9479

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It sounds like the 1618 Microwave Synthesizer has the range and purity I need. Send me a brochure right away.

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Title ______________________

Company ______________________

Address ______________________

City/State/Zip ______________________

Phone ______________________

Product specifications subject to change without notice.

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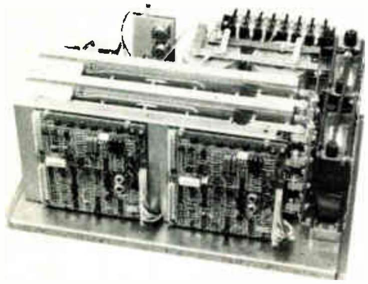
Circle 209 on reader service card



process using closed-loop motor control. Its compensation adjustment allows it to be quickly set up for a wide range of motors. It has a minimum frequency response of 500 Hz and no dead band, and it switches at 2 kHz. The chassis can carry from one to four axes (for a like number of motors) and varies in width from 11 to 19 in.; it is 17.5 in. deep and 7.25 in. high. An external power transformer must be supplied by the user, as must an external inductor for motors of less than 2.9 mH.

The two-axis model is priced at $1,760. Delivery takes approximately 12 weeks.

Westamp Inc., 1542 Fifteenth St., Santa Monica, Calif. 90404. Phone (213) 393-0401 [394]

Tiny robot motor produces 25 oz-in. of torque

The Magtech family of compact dc motors, intended specifically as "muscle" for robots, has been designed for maximum torque for weight and size. The smallest measures 1.75 in. long by 1.3. in. in diameter and puts out 25 oz-in. of torque. Its moment of inertia is 0.00036 oz-in.-s^2, allowing it to accelerate at nearly 70,000 rad/s^2

under no-load conditions.

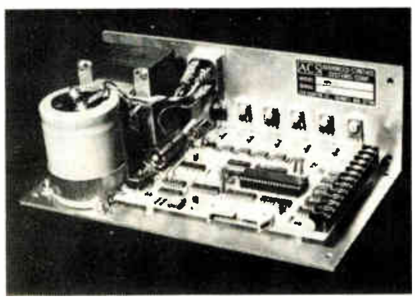
Larger members of the series produce 50, 75, 140, and 300 oz-in. of torque; the largest measures 4.5 in. by 3.1 in. in diameter. Windings are fully impregnated for low thermal resistance and insulation is rated to withstand 180°C. Brushes are replaceable from the outside.

Standard motors cost $50 to $200 in quantity, with 13-week delivery.

Magnetic Technology Division of Vernitron Corp., 2100 Kittridge St., Canoga Park, Calif. 91303 [397]

Unit controls and drives 3-to-5-phase stepper motor

The MCU-3 is a microprocessor-based controller and driver for three-, four-, and five-phase stepping



motors. The open-frame unit, which performs at speeds of up to 5,000 steps/s, is suitable for applications in automation and robotics. It contains a motor power supply rated for a 4-A load at a nominal unregulated dc potential of 28 V. No external supplies are needed unless larger loads must be carried. The power section and field control lines are optically isolated.

The controller has a three-state control-bus interface compatible with most 8-bit microprocessors. On-board address switches allow up to 16 MCU-3s to be paralleled on a 26-line flat-cable bus. Thirteen instructions give the unit flexible programming so that it may serve a wide range of applications. It is priced at $394 and discounted in quantity; delivery is in six weeks.

Advanced Control Systems Corp., 213 Centre St., Quincy, Mass. 02169 [398]

Factory data-entry terminal reads bar-coded badges

With the 6028B multifunction badge-reading terminal, workers' bar-coded badges may be inserted in a slot mounted on top or a light pen may be passed over the bar codes. In addition, data may be entered through a keyboard consisting of a pad of numbers and a pad of letters in alphabetical order. The unit's 32-character blue-green alphanumeric display is easily read in any working environment. An audible annunciator lets the operator know when a badge is acceptable. The light pen is housed in a rugged aluminum case and has wide latitude in the tilt of the bars read.

The terminal interfaces directly with an Identicon data-collection system 7300 processor or other computer. Its steel case protects it from the rigors of the factory environment. Pricing is $1,935 per unit, with quantity discounts available. Delivery is within 90 days.

Identicon Corp., One Kenwood Circle, Franklin, Mass. 02038. Phone (617) 528-6500 [399]

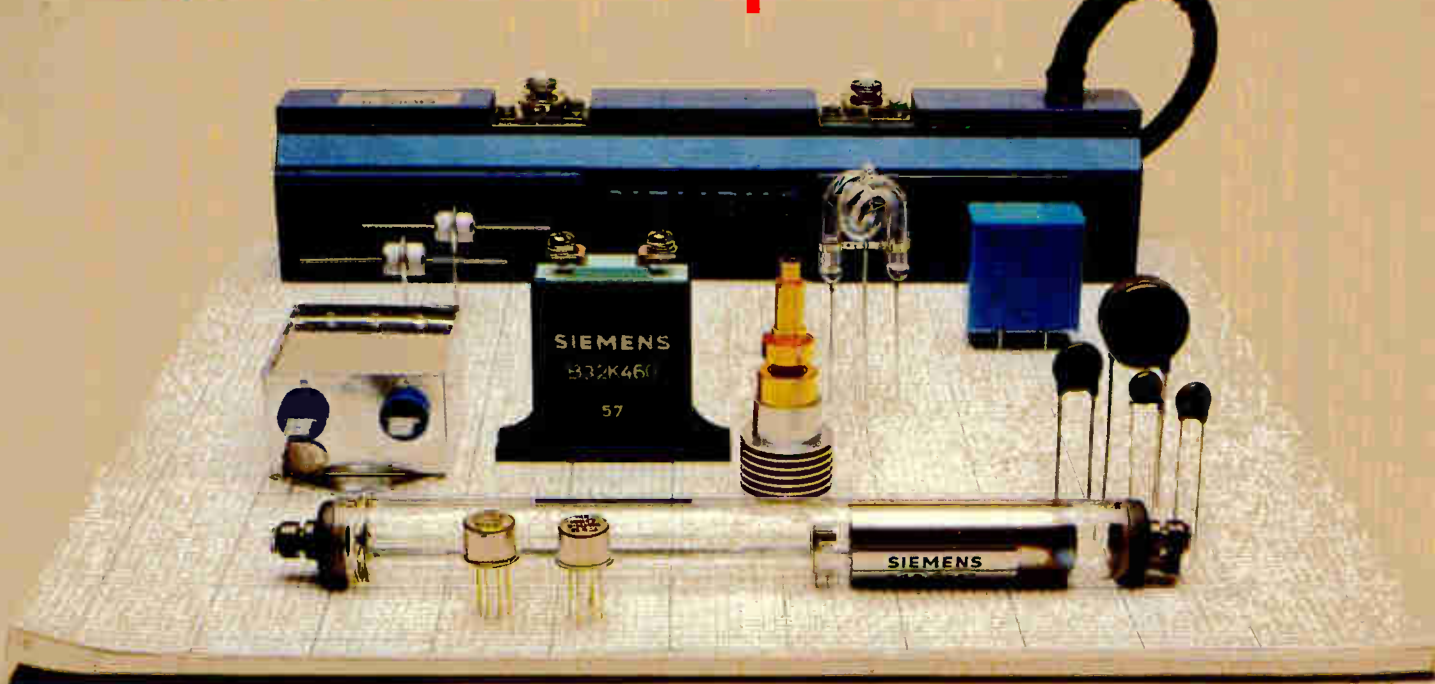
Paper thermometers record peak temperatures

Hermetically sealed and encapsulated adhesive-backed paper thermometers measure and record peak temperatures when attached to various machine equipment or components. The Thermax line includes thermometer strips, record indicators, and encapsulated clock indicators and are available in a variety of temperature ranges or in single temperatures. The strips change color from silver to black as temperatures reach or exceed indicated levels, permanently recording the peak temperature. They respond in 1 s and are accurate to within ±1%. A package of 10 is $7 when purchased in 100-piece lots; delivery is from stock.

American Thermographics Ltd., P. O. Box 572, East Longmeadow, Mass. 01028 [400]

SIEMENS

When it comes to specialized higher technology components, Siemens is the specialist.



If your design calls for higher technology components – turn to Siemens – because Siemens offers more answers. Positive answers – backed by Siemens recognized quality and years of experience. Now answers – because Siemens' wide variety makes it possible to meet your needs fast.

Be it flashtubes, crystal oscillators, or microwave tubes such as backward wave oscillators and travelling wave tubes ... SIOV's, RFI filters, or lasers ... Siemens components are engineered to support and reflect well on your product's design and function.

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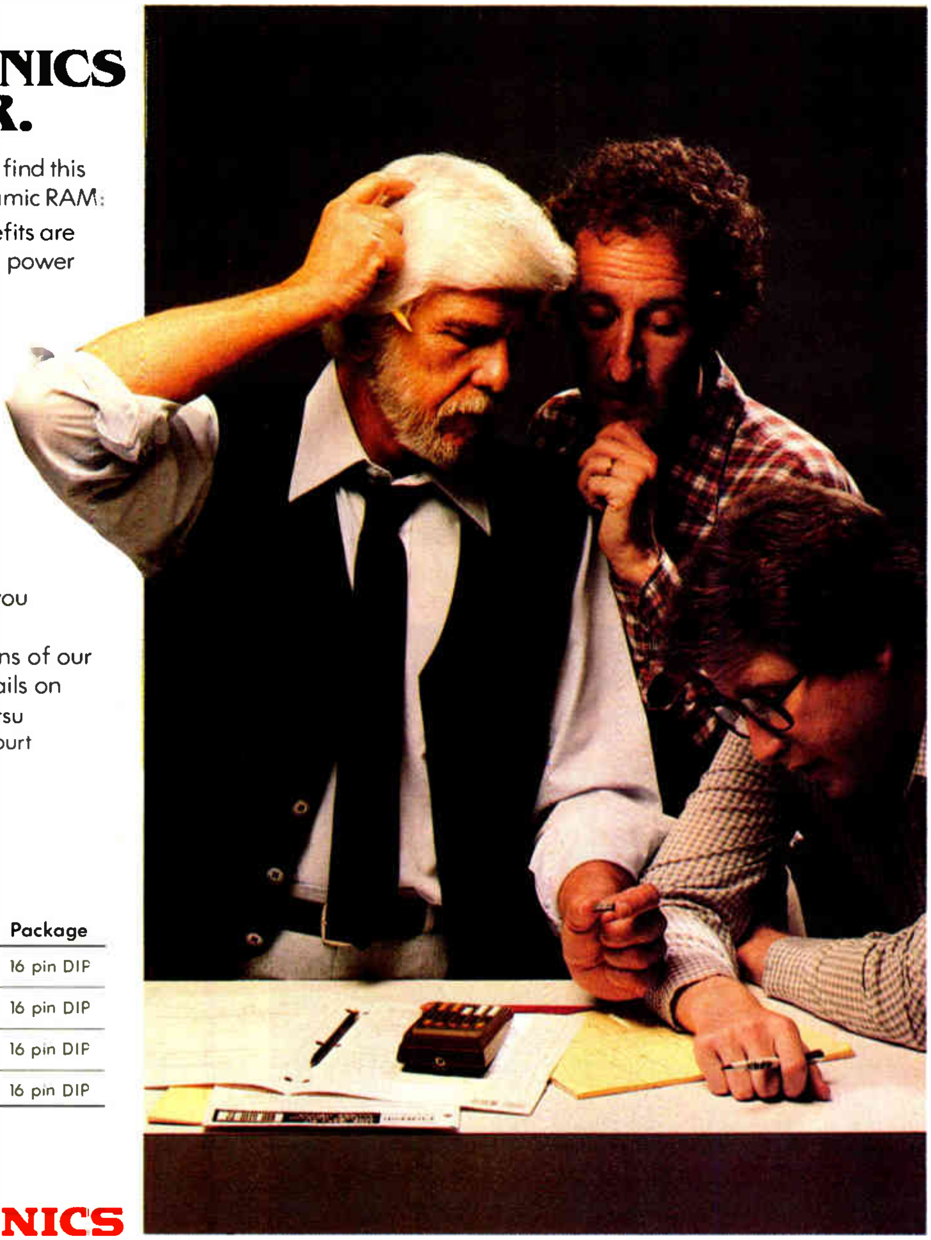
- Electromagnetic Pulse Analysis

FUNNY, IT LOOKS JUST LIKE EVERY OTHER 16K DYNAMIC RAM...

BUT FUJITSU MICROELECTRONICS BUILT IT BETTER.



It's better because nowhere else can you find this combination of features in one 16K dynamic RAM:

- **Single +5 Volt Power Supply.** The benefits are obvious. When you design out multiple power sources, you cut costs.
- **Upward Compatibility.** Go with our 16K RAM now and upgrade to our 64K RAM in the future. The move is easy, because they're pin-compatible.
- **Refresh Option.** Choose between two versions: On MB8117, pin 1 is for auto refresh; on MB8118 pin 1 is a no-connect.
- **All This Plus Speed!** Check the chart for access and cycle times. The speed you need is there.

Delivery is immediate on both versions of our new 16K dynamic RAM. For all the details on how we built it better, call or write: Fujitsu Microelectronics, 2945 Oakmead Village Court Santa Clara, CA 95051, (408) 727-1700 TWX 910-338-0047.

Fujitsu Microelectronics +5 Volt, 16K Dynamic RAMs

	Access Time	Cycle Time	Pin 1 Function	Package
MB8117-10	100ns	235ns	Refresh Control	16 pin DIP
MB8117-12	120ns	270ns	Refresh Control	16 pin DIP
MB8118-10	100ns	235ns	No Connect	16 pin DIP
MB8118-12	120ns	270ns	No Connect	16 pin DIP

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Circle 214 on reader service card

The assignment: design a pushbutton switch capable of evolving into many different forms without sacrificing reliability.

The result: ITT Schadow's "F" pushbutton series.

At ITT Schadow, we specialize in taking basic switch designs and changing them to fit your specific applications. We've built a reputation on our awareness that the first two syllables of "customer" are "custom."

Customized applications work best when they're based on products with a proven record of reliability. Our famous "F" series of pushbutton switches is a case in point. Coil spring-loaded, sliding silver-clad contacts wipe away oxide deposits each time the switch is actuated, providing reliability as good as gold in many applications. Lampless status indicators are an exclusive ITT Schadow feature. Solder eyelets, PC pins, and glueless snap-on buttons are standard. Mounting frames are available with 6 variations in spacing. Two to 16 poles, 8 different terminal options, make-before-break, break-before-make, and a wide choice of mechanical options are offered.

Over the past two decades, we've made millions of pushbutton, key-, rocker, and rotary switches for some of America's largest consumer and industrial OEM's. We are your "creative switchmaker" with the ability to design, adapt, and manufacture switches for nearly every requirement.

Your ITT Schadow manufacturer's representative or distributor can tell you more. Or contact ITT Schadow Inc., a subsidiary of International Telephone and Telegraph Corporation, 8081 Wallace Road, Eden Prairie, MN 55344. Phone 612/934-4400, TWX 910-576-2469, Telex 29-0556.

48 of ITT Schadow's countless standard and custom switches.

ITT Schadow

Circle 216 on reader service card

Computers & peripherals

Tape controller speeds Series/1

Two-board unit controls ANSI-standard tape drives running at 12.5 to 125 in./s

The TC 110 tape drive controller from the Western Peripherals division of Wespercorp lets the Series/1 from International Business Machines Corp. use tape drives from most manufacturers (including streaming types) that operate at tape speeds of from 12.5 to 125 in./s. Many ½-in. streaming drives have speeds of 125 in./s, but IBM's tape drive controller for the Series/1 handles either 45 or 75 in./s. In addition, the TC 110 dual-density controller is priced well below its IBM counterpart.

The controller is compatible with both the Event Driven Executive and Realtime Programming System operating software, and supports the IBM 4969 tape subsystem. Other plug-compatible controllers rely on their own software—software written before IBM decided to support the Series/1 with a tape drive and came out with the 4969.

The TC 110 has dual-density nonreturn-to-zero inverted and phase-encoded formats. It also interfaces with any drive—such as units from Kennedy, Pertec Computer, or Cipher Data Products—that conforms to the requirements of the American National Standards Institute. Drives can be interchanged without altering the controller.

Bit-slice. The two-board TC 110 may be installed in the Series/1's central-processing-unit card file or, on larger systems, in the expansion chamber. One of the four-layer, 7-by-10-in. boards holds the 2901 bit-slice microprocessor elements, the control store, and the sequencer. This board controls the interrupts and other aspects of the IBM input/output channel. The second board has drivers, receivers, and the formatting and interface electronics. Six 1-K-by-8-bit AMD 27S35 programmable read-only memories, chosen because they occupy 50% less space than conventional PROMs of the same configuration, house the control firmware, which is written in 48-bit words.

The tapes carry nine tracks of data; 1 byte and 1 parity bit are stored at each tape location. The TC 110 performs single-bit error detection and logging for both phase-encoded and nonreturn-to-zero inverted formats. In addition, single-bit errors may be quickly corrected when the phase-encoded format is used. Multiple-bit and parity errors in the phase-encoded data invoke an automatic retry operation.

A power-up diagnostic routine tests the controller's data paths and microprocessor operations; light-emitting diodes disclose the test being performed. Hardware problems can be resolved through signature analysis test points.

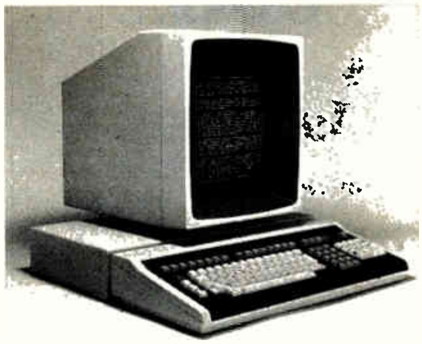
Up to eight drives running at any two speeds in the specified range can be daisy-chained together from the TC 110. Drives are connected to the controller with a standard flat cable up to 40 ft long. Each of the two boards draws about 3 A from a +5-V power supply.

Single units are priced at $3,500; quantity discounts are available. Delivery is in 90 days.

Western Peripherals, 14321 New Myford Rd., Tustin, Calif. 92680. Phone (714) 730-6250 [361]

8086-based PM 2010 terminal has ANSI-standard functions

The PM 2010 smart terminal combines the American National Standards Institute's X3.64-1979 standard with an 8086 microcomputer, 32-K bytes of random-access memory expandable to 256-K bytes, and a 66-by-80-character video display. It also features 8-K bytes of erasable programmable read-only memory, two RS-232-C ports, and a parallel printer port. Ten transmission rates



of between 75 and 19.2 kb/s are switch- or software-selectable.

The video display uses a 7-by-9-dot matrix in a 9-by-15-dot field. Up to 128 upper- and lower-case characters can be displayed in high or low intensity with blinking, reversal, blanking, or underlining. The 107-key detachable keyboard consists of a full alphanumeric set with N-key roll-over, eight function keys, a numeric keypad, and various dedicated keys. The terminal can preprocess data by performing such tasks as down-loading and running, form filling and transfer, area qualification, block-mode transmission, multipaging, and cursor control with associated numeric parameters.In lots of 500 units, the PM 2010 is $2,500, with delivery in 30 days.

Piiceon Inc., 2350 Bering Dr., San Jose, Calif. 95131. Phone (408) 946-8030 [363]

Low-priced color graphics terminal has 64-color option

A high-resolution raster-scanning color graphics desktop terminal is available for a limited time at a price of $5,995. This introductory offer includes the detachable optional keyboard and a discount on Ramtek's model 4100 Colorgraphic printer if both are bought together. The RM-6211 with RS-232-C interface has a resolution of 640 by 480 picture elements operating at 30 Hz, with an option of 640 by 512 pixels operating at 60 Hz. Its 13-in. monitor has a 64-dot-per-in. image. It can simultaneously display either up to 16 colors selected from a palette of 64 or 8 colors plus either an alphanumeric overlay or a blinking function. The RM-6211 uses Ramtek's Colorgraphic Programming Language, but is compatible with Tektronix' Plot 10 graphic software and Dispia, Tell-a-graf, DI-3000, Grafmaker, SAS/Graph, and Patran-G.

Options include a digitizing tablet with an 11-in.^{2} work surface, a light pen for direct screen interaction,

menu selection and high-speed cursor steering, and 16-K-byte random-access memory. The special price lasts only until Dec. 31, 1981. Shipments will be within 60 days of that date.

Ramtek Corp., 2211 Lawson Lane, Santa Clara, Calif. 95050. Phone (408) 988-2211 [364]

Small-business computer can handle 4 users, 1 printer

The desktop MBS3000 is a business computer system based on an 8088 16-bit microprocessor. The basic $19,900 system includes 64-K bytes of dynamic random-access memory, expandable to 0.5 megabyte; one video display terminal, using an RS-232-C interface; one parallel interface printer; and a 10-megabyte 8-in. Winchester disk drive with a tape cartridge backup. As many as four users can be accommodated, and a 20-megabyte drive is available. A port conforming to the Synchronous Data Link Control protocol is optional. Mercator supplies seven general-purpose accounting software packages, as well as vertical packages for the insurance, construction, medical, and legal professions. The MBS3000 is fully compatible with Mercator's larger MBS4000. A completely configured MBS3000 is $27,100, with delivery in 30 days.

Mercator Business Systems, 1294 Lawrence Station Rd., Sunnyvale, Calif. 94086. Phone (408) 734-5134 [365]

Whisperwriter communicates over phone with TWX, Telex

The Whisperwriter is an addition to the 3M Electronic Message Terminal Network family. Using existing telephone lines, the desktop Whisperwriter communicates with TWX and teletypewriter networks worldwide. It has a 4,000-character memory and is available in two models. The 1440 prints 40 characters per line and the 1480 prints 80. Both units operate at 110 or 300 b/s. The Whisperwriter automatically answers incoming calls and verifies that the correct number has been reached. Available now, the 1440 costs $980; the 1480, $1,090.

3M, P. O. Box 33600, St. Paul, Minn. 55133. Phone (612) 733-1133 [366]

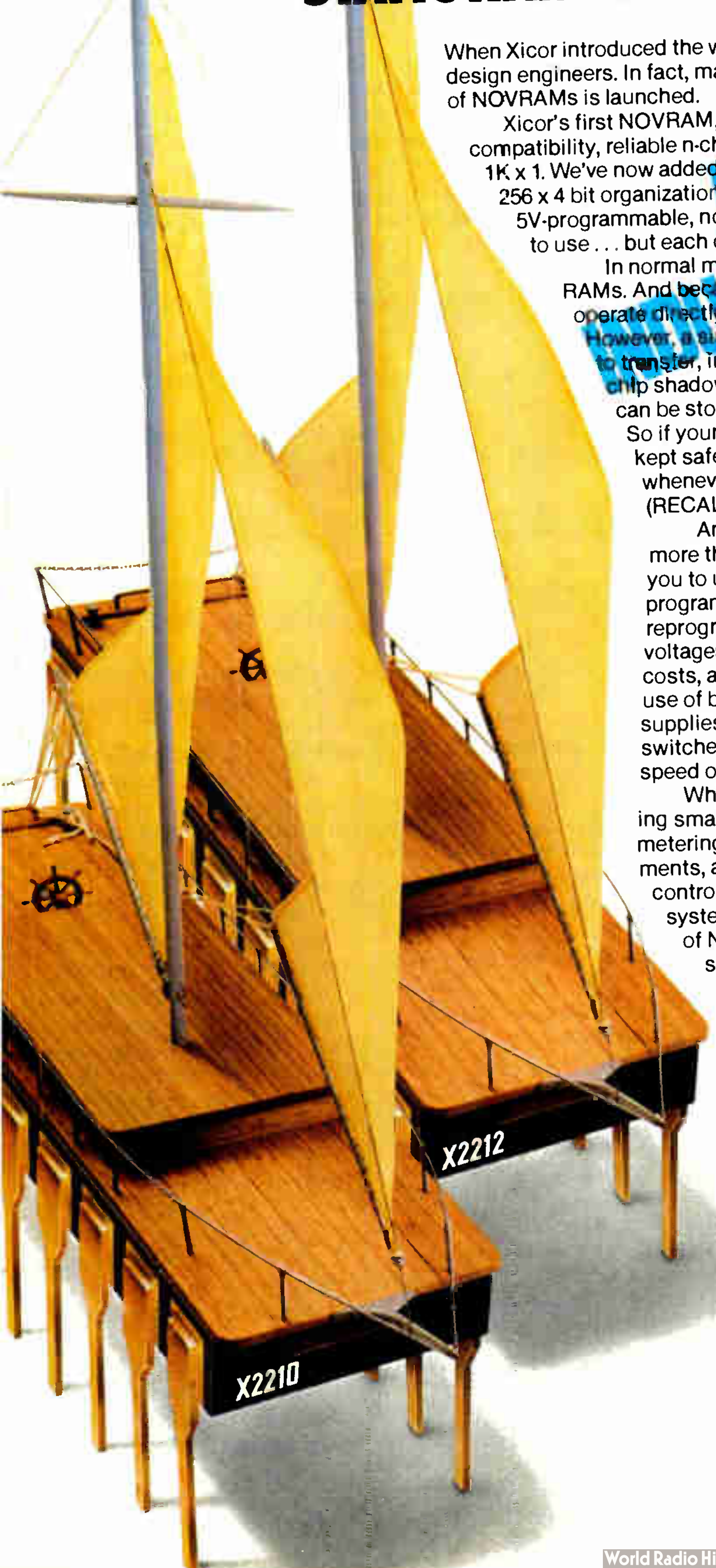
Low-cost terminal features 128-character set, graphics

The ABM 85 smart video terminal is offered at the low unit price of $550 in quantities of 500 and up. It features a 24-line-by-80-character display on a 12-by-15-in. screen with 23-MHz–bandwidth resolution. The display employs a 7-by-9-dot matrix with lower-case descenders in a 9-by-13-dot cell. It has a set of 128 ASCII characters, plus 95 alphanumeric and 33 control codes. There is an 11-key special graphics set and 8 programmable function keys that yield 16 functions. The ABM 85 has an RS-232-C interface; a 20-mA current loop interface is optional. Eight transmission rates range from 110 to 9,600 b/s. The 8085A-controlled terminal will be available for evaluation in September, with production quantities scheduled for October. A single unit is $850.

Amtek Business Machines Inc., 2255H Martin Ave., Santa Clara, Calif. 95050 [367]

TWO NEW NOVRAMs

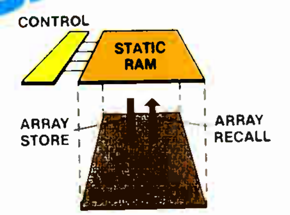
WORLD'S FIRST 5V-PROGRAMMABLE NONVOLATILE STATIC RAM FAMILY IS LAUNCHED!



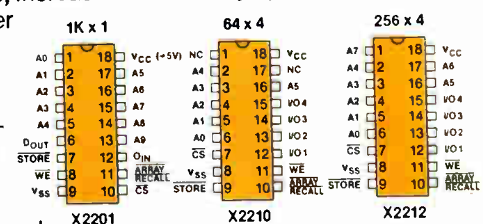
When Xicor introduced the world's first NOVRAM it caused a huge wave of interest among design engineers. In fact, many designers asked for more! Hence, the world's first family of NOVRAMs is launched.

Xicor's first NOVRAM, the X2201, offered convenient 'in system' programmability, TTL compatibility, reliable n-channel, floating gate MOS technology and a bit organization of 1K x 1. We've now added two new devices, the X2210 and the X2212, with 64 x 4 bit and 256 x 4 bit organizations respectively, to the series. Now you can select from three 5V-programmable, nonvolatile static RAMs . . . all with the same features, all easy to use . . . but each offering a different bit organization.

In normal mode, all three NOVRAMs function as conventional 5V static RAMs. And because of their 300ns cycle time, your microprocessor can operate directly with these NOVRAMs at full speed. However, a single TTL signal (STORE) is all it takes to transfer, in parallel, all RAM bits to a unique on-chip shadow memory (E² PROM). There, the data can be stored indefinitely—*and without power*. So if your power source fails, your data will be kept safe, and you can bring it back into RAM whenever you desire with another TTL signal (RECALL). It's as simple as that.



And there's more! Since it requires no more than 5 volts to perform all functions, a NOVRAM will also allow you to upgrade system firmware—from a single word to an entire program 'in system'—whenever you want. For the first time, onsite reprogramming can be done without the need for unsocketing, high voltages or UV light sources. This means you can reduce your system costs, and at the same time, increase its efficiency by eliminating the use of batteries, extra power supplies, counters or dip switches. And still get full speed operation!



Whether you're designing smart terminals, remote metering systems, instruments, avionics, process controls or any other μP-based system, it's time you explored the possibilities of Xicor's new family of NOVRAMs. Circle the reader service number below and we'll send you complete specifications. If you have a 'can't wait' situation call Bud Koch, our Marketing Manager at 408-946-6920. Xicor, Inc., 851 Buckeye Court, Milpitas, California 95035.

NOVRAM... EXPLORE THE POSSIBILITIES.

Xicor

THE WORLD'S SMARTEST MEMORIES

Circle 219 on reader service card

Software

Idris supports 8080 and 68000

Low-cost operating system supports standard Unix environment and Pascal

The Idris operating system from Whitesmiths Ltd. is now available for LSI-11 and PDP-11 computers and microcomputers based on the 68000, 8080, 8085, and Z80 devices. Idris/R11 is a memory-managed version for all Digital Equipment Corp.'s computers from the LSI-11 through the PDP-11/70. It is compatible with Version 6 of Unix from Bell Laboratories at the file-system and system-call levels, as is the earlier Idris/S11 implementation for the LSL-11/02.

Also making their debut are Idris/B80 for Intel's 8080 and 8085 and Zilog's Z80 in a bank-switched environment and Idris/S68k, which operates on products based on Motorola's 68000, such as Chromatics Inc.'s model 7900 color graphics computer.

All versions of Idris offer full implementations of Pascal and C, plus most of the popular utilities found in the standard Unix environment. These include a context-sensitive text editor, a powerful "shell" command line interpreter, sorting and word-processing tools, and a comprehensive set of portable program-development utilities. Simple facilities are also provided for document formatting and networking.

Moreover all versions of Idris support the same file-system and library formats, regardless of host-computer word size or byte order. This means that demountable file systems and object libraries can be freely interchanged among all machines that accept common media, which is not true with standard Unix.

To ensure maximum portability, all language translators and utilities are written in host-independent C. The resident is divided into a host-independent kernel, plus a small processor-dependent memory manager and a collection of bus-dependent device handlers. Memory requirements vary between 30-K and 60-K bytes for the resident and input/output buffers, plus an optional 0.1-to-1.0-megabyte swap area on disk.

Tested. Idris has been at selected field sites for nearly two years and is now in commercial use at dozens of installations throughout the world. The 8080 and 68000 implementations of Idris are expected to extend its useful range to applications both smaller and larger than has been traditional for Unix and Unix-like systems. Future plans call for an Idris/R780 for the VAX family, as well as for the Intel 8086, 8087, 8088, and iAPX 286 family of processors.

Idris/R11, /B80, and /S68k are available for September delivery in a number of configurations: $2,200 licenses a version that produces code only for the host; the "cross" version, for $2,550, produces code for a different target machine. These are single-processor binary licenses—source code is available for 10 times the price. Liberal original-equipment-manufacturer discounts are available, ranging from 75% for 100 copies ($550 per copy) to a 95% discount for quantities over 5,000 ($110 per copy). The quantities are cumulative, too, so that as the OEM sells more copies the price goes down regardless of the size of the lots they are bought in.

Whitesmiths Ltd., 1780 Broadway, Suite 601, New York, N. Y. 10019 [401]

Pascal development system supports Intel microprocessors

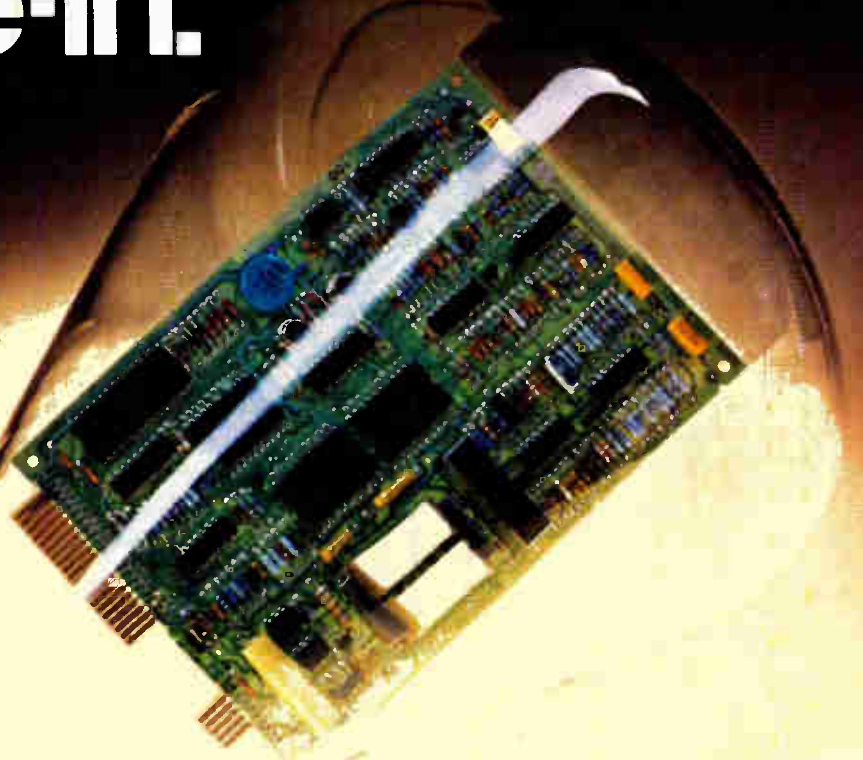
Language Resources' series of Pascal software development systems is based on the industry's first machine-independent, retargetable, Pascal compiler system. It allows a company to deliver packages to suppport new microprocessors a few months after the devices become available. The first PAS-86 packages run on Digital Equipment Corp. VAX and PDP computers and on IBM Systems/370s as hosts. They support Intel's 8086, −87, and −88 microprocessor family. The PAS-80 package for the 8080/8085 family runs on VAX computers. Each package includes the Pascal compiler, a macroassembler for the universal AL/M assembly language, a run-time support library, a resolver subsystem that generates a variety of code outputs, and a comprehensive human interface. All packages—PAS-86 VAX/VMS, PAS-86 PDP/UNIX, PAS-86/CPM, PAS-86 86/RS86, PAS-86 370/CMS, and PAS-80 VAX/VMS—are available now; a single-copy object user license is $4,800.

Language Resources Inc., 4885 Riverbend Rd., Boulder, Colo. 80301. Phone (303) 449-8087 [403]

Assembler supports bit-slice microprocessors

The Macro Meta assembler package is a tool for programming bit-slice microprocessors such as the AMD 2900 and Fairchild Macrologic chip sets, as well as other wide-word microcoded processors. Three programs make up the package: a definition program in which instruction mnemonics, macroinstructions, and the latters' associated bit patterns can be defined; an assembly program that operates like a conventional two-pass assembler, producing an output listing and object module; and a program for formatting programmable read-only memories that enables the user to break up object code into organizations compatible with the target PROM or ROM array. With the macro package the user can define microwords of variable length and noncontiguous variable fields and also represent complex overlaid instructions with a single mnemonic. Written in the American National Standards Institute's standard Fortran IV, the Macro Meta assembler will run on any general-purpose computer, including 16-bit minicomputers, and is upwardly

How to turn your modem outside-in.



Turn to Rockwell. We're showing designers how to replace a black-box modem that's outside their computer-based products—with one that's inside. One that's modular, integral, and MOS/LSI-based.

Our integral modems give your products added value, so you get a leg up on your competition. That's because they provide all the features of black-box modems—but at a fraction of their cost. Plus their compactness gives you new physical design freedom.

And Rockwell modems are available at a level of integration that meets your requirements. Take our R24, for example. A 2400-bps synchronous modem, it comes in three configurations—all exceptionally compact, and compatible with Bell 201 B/C and CCITT V.26 A/B standards.

First there's our fully assembled and tested single-board modem, ready to plug into your system—like the one shown above. Then there's our set of three discrete modules, ready to be designed into your own modem. They allow you to separate transmit and receive functions, if desired. And to speed your modem integration design cycle, there's also an R24 evaluation board available.

Which means that when you're designing computer-based terminals and communications equipment, you can now bring the modem inside your product. How? By integrating the R24's solid-state reliability and economy into your product, for both leased-line and switched-network applications.

That's just the kind of advantage you'd expect from Rockwell, the company that's delivered more integral LSI 4800/9600-bps modems than anyone else in the world. That's right—*anyone*. And Rockwell modems are in stock now—fully assembled, on production or evaluation boards, or as discrete modules.

So don't leave your modems on the outside looking in. For information or applications help, call toll free: (800) 854-8099; in California, (800) 422-4230. Or write: Rockwell International, Electronic Devices Division, RC55, P.O. Box 3669, Anaheim, CA 92803.

Rockwell International

...where science gets down to business

Circle 221 on reader service card

compatible with the basic AMDASM language. Delivery is to one week from stock for the $2,400 package.
Microtec, P. O. Box 60337, Sunnyvale, Calif. 94088. Phone (408) 733-2919 [407]

Z8000 PLZ/SYS constructs software for Z8001, Z8002s

Z8000 PLZ/SYS, the extended version of Z80 PLZ/SYS, is a high-level, procedure-oriented system implementation language for the Z8000 microprocessor. It is designed for constructing operating systems, compilers, data-base management systems, and other system software for the segmented Z8001 and unsegmented Z8002. Implemented to run on Zilog's development systems, the Z8000 PLS/SYS combines elements of the Pascal, Algol, PL/1 and C language in such a way that algorithms can be expressed in a high-level, structured fashion. Programs written for the Z80 in this language can be transported to the Z8000 via Z8000 PLZ/SYS. This latter is also fully compatible with Z8000 PLZ/ASM, a structured assembly language using the same object module format and data structure allocation rules. Available now, the Z8000 PLZ/SYS system programming language package is priced at $700.
Zilog, 10340 Bubb Road, Cupertino, Calif. 95014. Phone (408) 446-4666 [404]

Two packages give Apples communications capabilities

Two Microcom software packages give Apple computers communications capabilities. With Micro-Courier, an electronic mail package, the user of an Apple II desktop computer can transmit charts, graphs, correspondence, VisiCalc reports, and entire programs to other Apple computers over standard phone lines. Also, he or she can take advantage of low night phone rates because the transmission can be made automatically—1,000 sent in less than 1 minute for less than 25 cents.

With Micro-Telegram, on the other hand, the Apple owner can access Western Union Service worldwide, using it to send and receive mailgrams, TWX, Telex, and international cables, editing on screen and transmitting automatically. In addition, access to news, stock, foreign, exchange, gold, futures, and sports reports is available through Infomaster, the Western Union data base. Each package is now available for $250.
Microcom, 89 State St., Boston, Mass. 02109. Phone (617) 367-6362 [405]

C cross-compiler produces code for 6502 microprocessor

A C cross-compiler for the 6502 microprocessor is supported under the Unix, RT-11, RSTS/E, and RSX-11 operating systems on the PDP-11 series and under the Unix/V32 and VMS operating systems on the VAX series of Digital Equipment computers. It complements existing lines of C compilers and cross compilers producing code for the 8080/Z80, PDP-11, and VAX families, as well as the 68000 sold by Whitesmiths Ltd. of New York. As code produced by the compiler is symbolic assembly language, the C programs may be freely intermixed with assembler code or even other languages, with the use of suitable interface protocols. Most facilities of the C language are supported except floating point, bit fields, long integers, and the creation of new local variables by means of internal blocking structures. Available now, a binary license for use on a single host central processing unit is $1,600.
Advanced Digital Products Inc., 1701 21st Ave. S., Suite 222, Nashville, Tenn. 37212. Phone (615) 383-7520 [408]

ISIS-II software toolbox contains over 30 programs

The ISIS-II software toolbox is a package of over 30 utility programs that can reduce the cost and time of developing Intel microcomputer systems, aiding programmers in different design phases. Running under the ISIS-II operating system on an Intellec development system, the tools track different versions of program modules from source to object code, add conditional execution control to ISIS-II command files, and enhance other operating system and debugging functions. Included among eight categories of tools are submit file execution control and source file management. The first group allows structured programming techniques at the command level by supporting jumps, calls, and returns among ISIS-II commands. The source management tools make it possible for the programmer to identify different source versions and to determine which versions of each source module were used to create a load module. The ISIS-II software toolbox, which comes with source code, generation procedures, and documents, is available for $850.
Intel Corp., 3200 Lakeside Dr., Santa Clara, Calif. 95051. Phone (408) 496-9484 [406]

Compiler is easy to use, executes quickly

The Hayden Applesoft compiler combines the ease of writing and debugging in Basic with the speed inherent in executing machine language. It translates a standard Applesoft Basic program into true machine code, and the resulting binary program is claimed to run more than 12 times faster than normally interpreted code. Compilation is a one-step process in which the user specifies the name of the program to be compiled and then runs the compiler program. Optional compilation parameters may be specified to alter the default memory configuration of the target file. The compiler requires 48-K bytes of random-access memory, Applesoft, the Autostart read-only memory, and at least one disk drive. It costs $200 at computer dealers.
Hayden Book Co., 50 Essex St., Rochelle Park, N. J. 07662. [409]

SNAFU'ED*

by Real Time Data Acquisition?

Some Hidden Dangers in Many Real World Installations

After you invest hard dollars in data acquisition hardware and software, you're certainly justified in hoping that your new simulation, control, or test system will do everything you may need it to do. But then the UNTHINKABLE happens...suddenly you are:

- Awash in a sea of "software improvement" dollars
- Unable to steam along at a speed that keeps you ahead of your real-world process
- Uncertain of your position due to electrical interference
- Unable to tack quickly enough as the Requirement Winds change
- Adrift because accuracy drifts
- Unable to read the charts because documentation & support are incomplete
- Overboard as a result of inadequate reliability
- Deep-sixed by long software development times for simple tasks, like conversions to engineering units
- Or ______________________________

We'd like to hear of any data acquisition SNAFU that you may have experienced. Please describe it above, then mail this page to us (addressed to T. Ellard).

The Cold, Hard Facts

It happens constantly. Whether you buy data acquisition equipment for integration with your computer, or buy an "integrated" data acquisition system, suddenly you're spending a lot of time, energy, and money improving synchronization capabilities, overcoming software limitations, and learning that the accuracy of the analog-to-digital converter at the heart of the system is degraded by the rest of the system; or worse...suddenly you're just plain sunk!

It need never happen again.

FOCUS 5000™ (FORTRAN Controllable Universal System) is the most comprehensive programmable I/O and processing system available for real world analog and digital data. It economically meets the "hidden" data acquisition needs, as well as the more easily visible needs, of many critical installations such as engine test stands, process control systems, and simulators — by integrating field proven equipment into a flexible, new architecture with unique software and timing capabilities.

Depending on the application, FOCUS 5000's easy-to-use programmability lets installations come on-stream up to 90% sooner than with other data acquisition systems. And the advanced architecture lets installations operate several times faster...at rates up to 100,000 measurements and outputs per second (with synchronization to the microsecond)!

Now any real-time installation can *perform* as though it has a custom integrated data acquisition system, at the far greater *economy* of a standard system. In fact, FOCUS 5000 is priced competitively with slower, less accurate "standard" systems.

Don't be SNAFU'ed*

FOCUS 5000 includes a high level (economical-to-use) programming language tailored to the needs of engineers and scientists, plus comprehensive software utilities and debugging aids. Its single-call access to calendar time and relative time clocks simplifies synchronization, data correlation, and time-based processing such as calculating derivatives of analog inputs with respect to time. Further, its accuracy guarantee applies to the entire *system*, not just the A/D converter!

We not only deliver a thoroughly tested system ready for immediate connection to your I/O field wiring...we also include self-test hardware and software at no extra cost so that you can easily verify system integrity. That's just the start of a comprehensive field support package tailored to put you in control of your real world.

We Look Deeper

Thousands of Analogic multi-channel data acquisition and signal processing systems have been installed worldwide. FOCUS 5000 was evolved from this successful base to meet needs expressed by engineers in many different fields.

We think you'll like the result. Find out. Throw us a line (circle the reader service number) and we'll send you our free brochure. Or, if you need help now, give us a call at (617) 246-0300.

FEATURES

- Software engineering routines include thermocouple linearization to 0.2°C
- Direct connections for up to 1,000 I/O channels, with up to ±500V electrical isolation
- Analog resolution of 12 to 16 bits, with guaranteed accuracy
- Up to 10^5 measurements /sec.
- Full digital I/O including contact closures and interrupts

* *For those of you who are too young to remember World War II, SNAFU was a term commonly used then, meaning: Situation Normal, All "Fouled" Up. Based on comments we receive from a broad spectrum of engineers, SNAFU seems to fit a large percentage of the real time data acquisition systems commonly used today. That's why we developed FOCUS 5000. So system engineers won't be SNAFU'ed. And real time installations won't founder.*

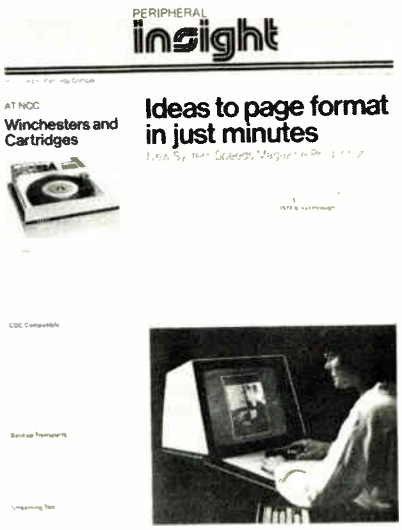
ANALOGIC®

We look deeper, so you can steer clear of the hidden dangers.

Audubon Road, Wakefield, MA 01880, Telephone (617) 246-0300

New literature

Peripheral insight. A four-page newsletter entitled "Peripheral Insight" describes computer applications, new Kennedy products, corporate news, and events in the peripheral industry, keeping readers



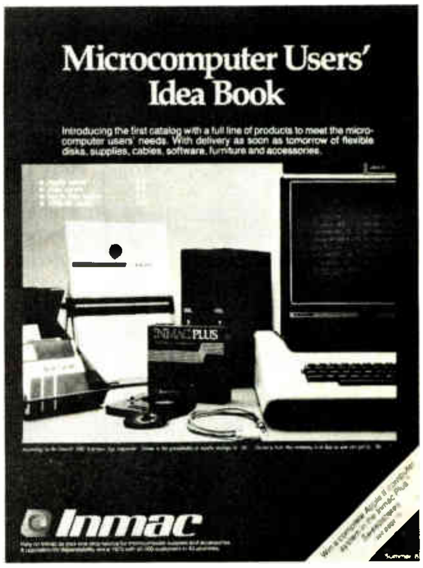
abreast of the state of the art. To receive a copy use the reader-service card or send a note on company letterhead to Kennedy Co., 1600 Shamrock Ave., Monrovia, Calif. 91016. Circle reader service number 421.

Intel handbook. The operation and possible applications of Intel's 16-K electrically erasable programmable read-only memory are described in the 96-page "E²PROM Family Applications Handbook." It shows how EE-PROMs may be interfaced with a microprocessor and programmed from a 5-V power supply. The handbook is free and can be obtained by writing to Intel Corp., Literature Department SV3-3, 3065 Bowers Ave., Santa Clara, Calif. 95051, or by calling (408) 734-8102. [422]

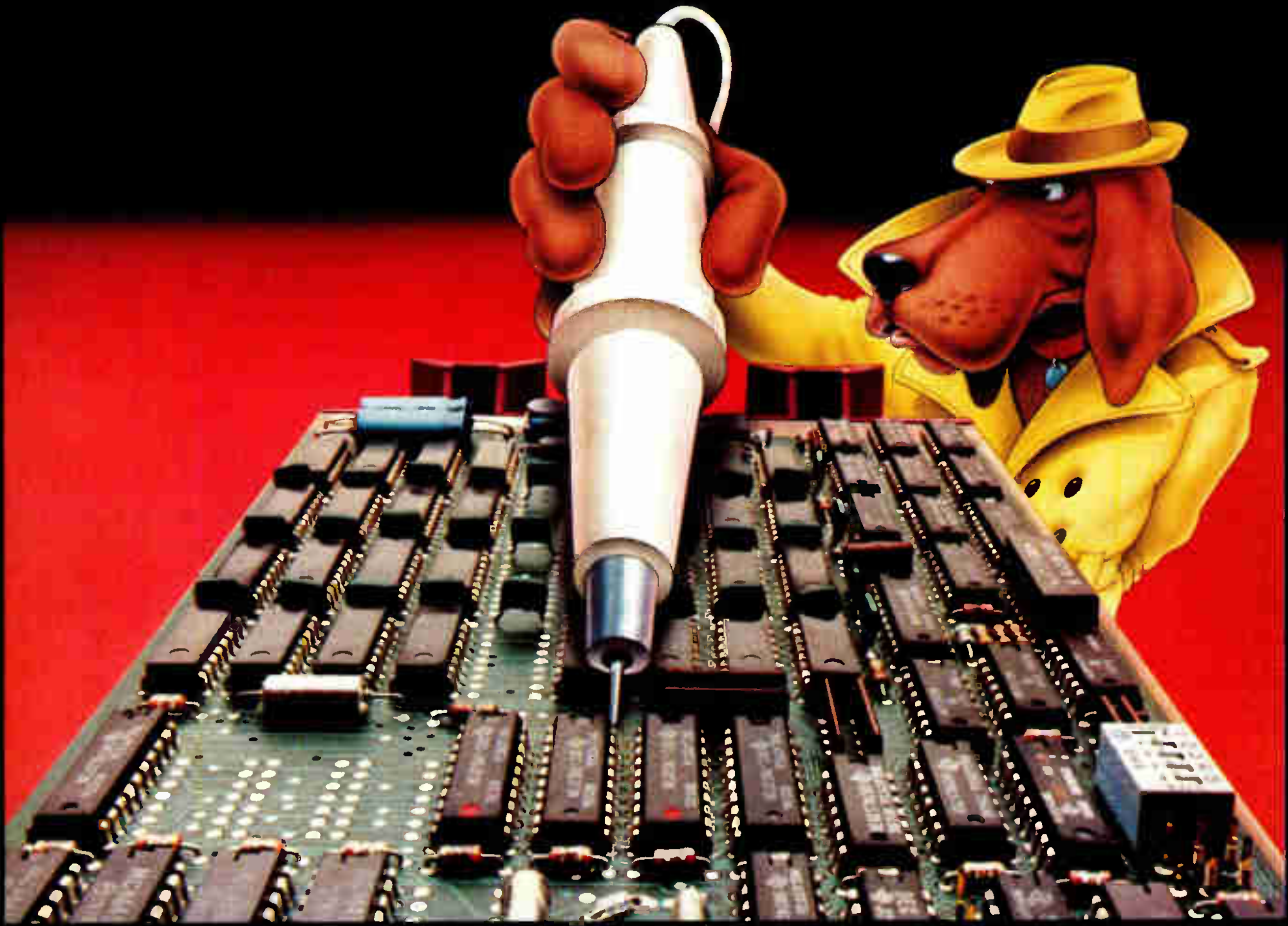
Field-effect-transistor kit. A field-effect transistor design kit from Siliconix contains a copy of the book "Designing with Field-Effect Transistors" that covers the theory and practical applications of FETs and offers a brief introduction to power MOS FETs. A copy of the Siliconix FET Design Catalog having data sheets and application notes on the company's entire FET product line, is also included, along with 10 FET samples—n- and p-channel, low-leakage and high-frequency FETs, amplifiers, switches, and amplifier and switch combinations. Retailing at $42.50, the kit sells for $28 to qualified engineers until the end of 1981. Mail request and check to Siliconix Inc., P. O. Box 4777, Santa Clara, Calif. 95054. [423]

CP/M-compatible software. The 24-page "CP/M-Compatible Software" catalog is the first publication available in the industry to list many different applications that run under CP/M, says John Katsaros, director of marketing. It describes application software and lists more than 100 different companies that write and distribute them. It was compiled as a tool for Digital Research's independent sales vendors support program for companies that write programs operating under CP/M. Priced at $5, the catalog can be obtained from Digital Research, P. O. Box 579, 801 Lighthouse Ave., Pacific Grove, Calif. 93940. [424]

Products for microcomputer users. "The Microcomputer User's Idea Book" is a 32-page catalog listing over 1,000 products such as flexible disks, cassettes, cables, ribbons, and printwheels available for the Apple II, Atari, TRS-80, and Northstar computers. The catalog covers the



PUT A BLOODHOUND ON THE CASE



For One-step Memory Board Testing.

"Sure," the Captain said, "a lot of people know about you – the MD-300 Macrodata Detective memory board tester, but not everybody knows how much of an edge our new Computer-guided Bloodhound Probe gives the user. The way this little guy sniffs out faults in the peripheral circuitry of memory boards puts any other probe system to shame.

"Nobody else can handle both synchronous and asynchronous memory board operations with the same quality of test. We're the ones who provide both a hard disk as well as a floppy disk for faster, increased storage. And that's just scratching the surface.

"Look at what else we can offer when we put our Computer-guided Bloodhound Probe to work with a Macrodata Detective MD-300: max-min programmable dual threshold input voltage levels of ±10V... float detect...10MHz operation ...1 megohm input impedance ...an H-P compatible signature analysis probe...transition counting to isolate difficult faults...isolation of faults in clocked feedback loops... multiple strobe in same cycle for one-pass testing...and windowed transition counting. That's the kind of fault detection in memory boards that every user deserves!

"Everybody out there with a Macrodata memory board tester should retrofit it with this powerful new Computer-guided Bloodhound Probe. And anybody thinking about taking custody of a new memory board tester should think twice about buying one of those other systems that doesn't offer the fault detection capabilities of our Macrodata MD-300."

Contact us today for more information on the Macrodata line of memory board and system testers and our new Computer-guided Probe.

Eaton Corporation, Test Systems, 21135 Erwin Street, Woodland Hills, CA 91365. Phone (213) 887-5550. Telex 69-8489.

EATON
Semiconductor Equipment

Circle 225 on reader service card

New literature

Centronic 739 read only printer, a line of Sanyo display monitors, VisiCalc and DB Master Software for Apple users, and Inmac's Data Master furniture system. For a free one-year subscription write to Inmac, Department 12, 2465 Augustine Dr., Santa Clara, Calif. 95051. [425]

Electronic equipment. Two catalogs have been released by the Systron Donner Instruments division. One is about electronic test instruments that include state-of-the-art microwave synthesizers and frequency counters, digital multimeters, pulse generators, timing equipment, and power supplies. The other, which is on switching and linear modular power supplies, includes power-conversion equipment with output-voltage ranges of ±5, ±12, and ±15 V, and current ranges of up to 15 A. For a copy of the instrument catalog contact Systron Donner Instrument Division, Sales Department, at 2700 Systron Dr., Concord, Calif. 94518. The power supply catalog can be obtained by writing to the power supplies sales department at the same address. Phone (415) 671-6637. [426]

Oasis operating system. Over 200 application software packages designed for the Oasis operating system are listed in the Software Monitor newsletter. The directory includes announcements of the Oasis-16 operating system for the 16-bit technology; Pascal, Fortran, and Forth high-level languages; the IBM 3740 formatting utility; Phase One Systems's training-center schedule and policy; and the establishment of a new Oasis users' group. A cross-reference chart to different application areas such as accounting, word processing, manufacturing control, and medical or dental packages is provided, as well as a list of national and international software sources. The Software Monitor newsletter, automatically sent to all licensed Oasis users, is available to anyone interested who contacts Phase One Systems Inc., 7700 Edgewater Dr., Suite 830, Oakland, Calif. 94621 or calls (415) 562-8085. [428]

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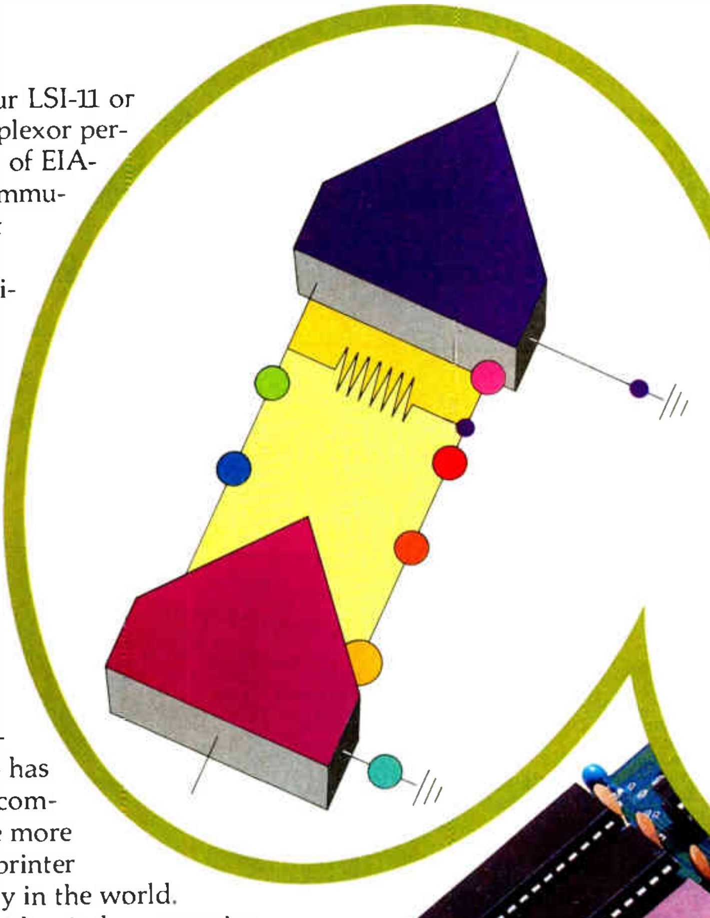

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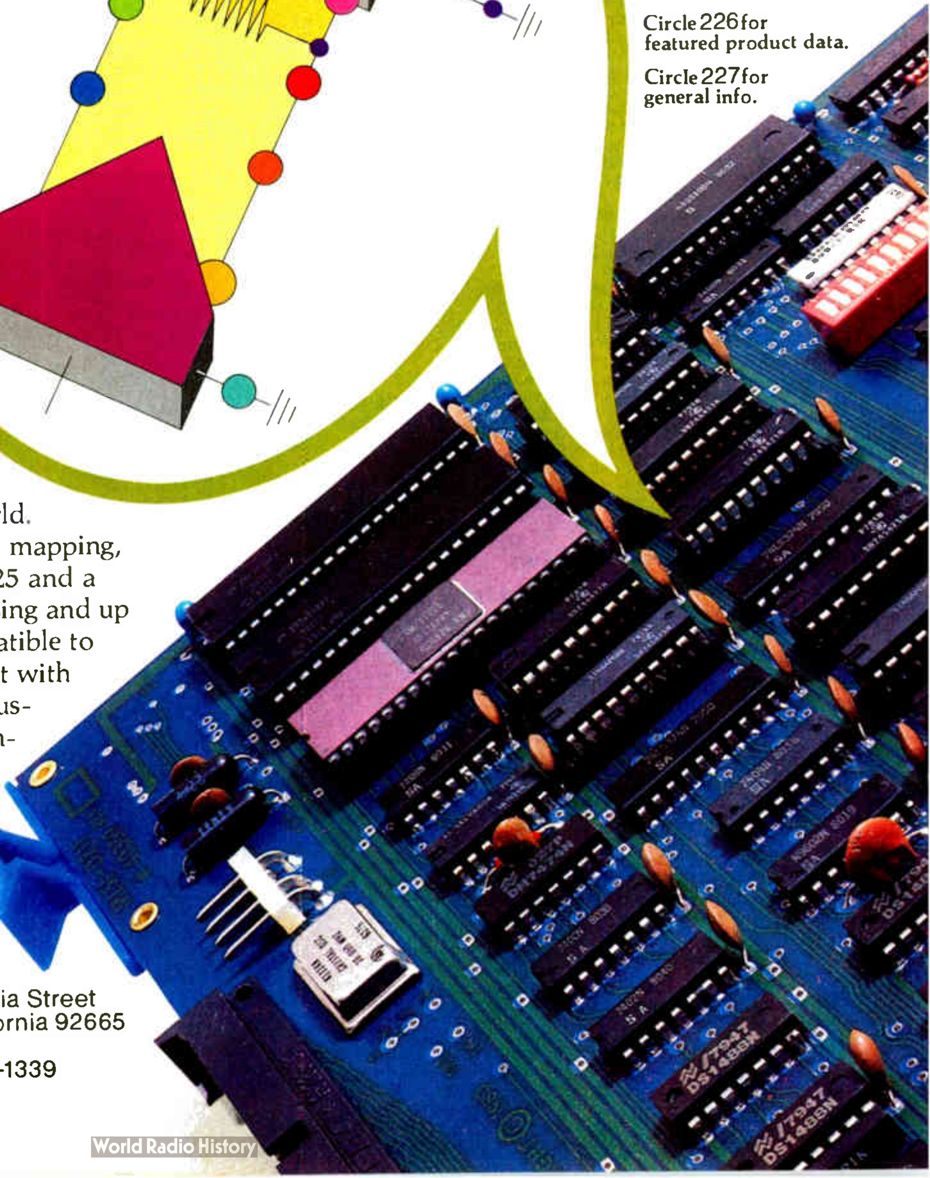

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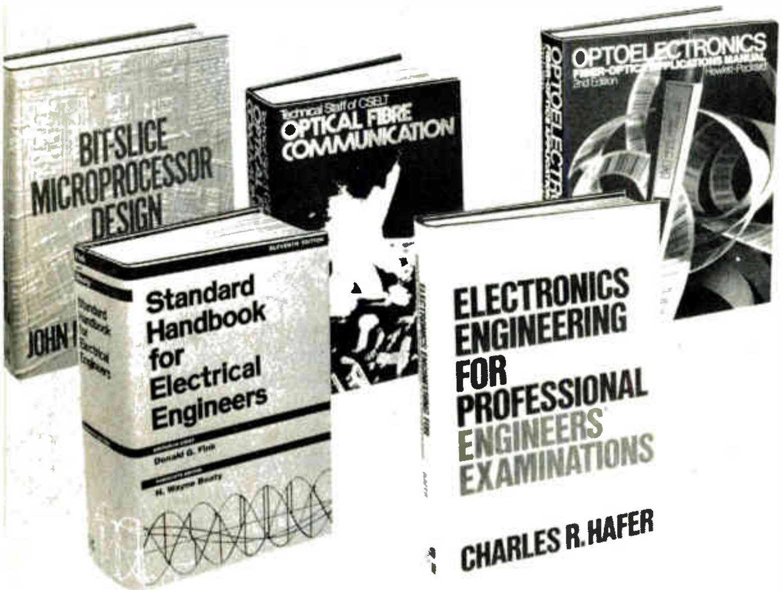

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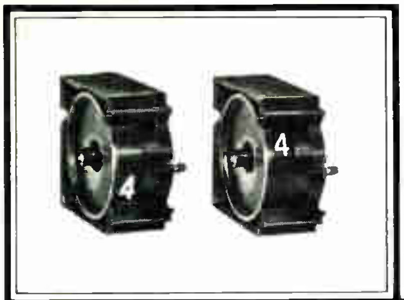

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Products newsletter

Bus transceiver chip reduces noise

Expect a new quad high-speed bus transceiver chip from National Semiconductor Corp., Santa Clara, Calif., that will upgrade the noise immunity of its current DS8641 transceivers. The DS3662 is compatible pin for pin with the DS8641, but it has a different scheme for recognizing and generating signal pulses. Whereas the DS8641 emits a square wave whose rise time is a function of load, **the DS3662 maintains a constant rise time of 15 ns and a similar constant fall time.** Its waveform-recognition circuitry is set up to reject pulses of less than 20 ns long, which create most of the noise environment for digital transmission. Although capable of data rates of up to 35 Mb/s, the DS3662 can more typically drive 200 ft of cable at 25 Mb/s. The price is $2.95 each in lots of 100.

Color raster terminal shades in polygons

Megatek Corp. will introduce **a polygon-fill processor that adds capabilities to its 7250 color raster display terminal** at the August Siggraph '81 in Dallas. The processor, based on the 2901 bit-slice processor, shades areas of polygons, offering an "order of magnitude speed improvement" over competitive units, the San Diego, Calif., firm says. The two-board set will be priced at about $5,000.

CRT reads magnetic cards for access

Tec Inc. is introducing a cathode-ray-tube terminal with a magnetic-card–reader keyboard to control access to computer and data files. The Tucson, Ariz., firm believes it is the first product for under $2,000 to **make confidential computer data secure through the use of encoded magnetic cards.** The model 630C smart terminal is priced at $1,300 in quantities of 250 or more.

Honeywell adapts DPS systems to IBM's SNA network architecture

Honeywell Inc. of Waltham, Mass., is unveiling three new software packages that allow its DPS 6 and level 6 computers to operate compatibly with IBM's Systems Network Architecture. With the new programs, Honeywell systems appear to an IBM host as if they were standard SNA controllers or peripheral devices. **Yearly license fees are $270 for an SNA transport package, plus $210 for an interactive SNA terminal package or $315 for an SNA remote-job-entry facility.**

Wang Labs augments word processor line

Lowell, Mass.–based Wang Laboratories Inc. will offer several enhancements to its OIS word and information processing systems: a spelling verification program with an 80,000-word expandable dictionary, a new **work station that formats proportionally spaced text on screen** and has a telecommunications capability, and a local archival memory on 5¼-in. diskettes. The work station is $5,500, or $7,000 with the telecommunications option; the diskette memory is about $1,000.

Pascal in ROM acts like Basic

Look for Rockwell International Corp.'s Microelectronic Devices division in Anaheim, Calif., to introduce **a Pascal interpreter stored in read-only memory for its AIM 65 single-board computer.** Instant Pascal, developed and marketed by M. Conway, Beverly, Mass., is like Basic, allowing a stand-alone system to do without file storage. It talks to the user only in Pascal and permits execution of a program immediately after a change is made in the source code.

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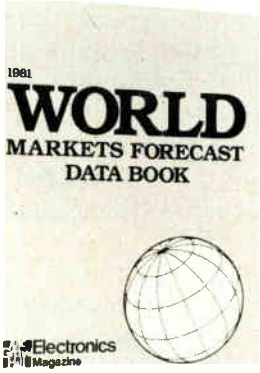

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Career outlook

Executives are prime targets

Reports from industry, government, and academia repeatedly warn the engineering community that there is a dire shortage of electronics engineers and computer programmers. Not surprisingly, the warning is also true for electronics executives.

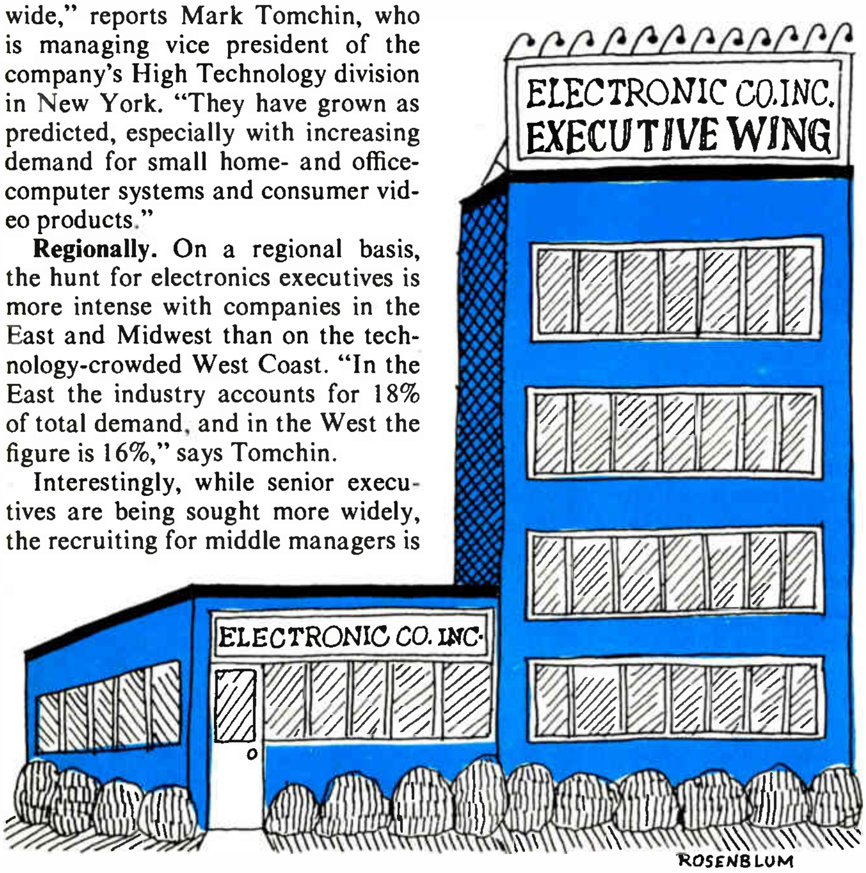
One indicator of the situation is the authoritative index maintained by the executive-search firm Korn/Ferry International. Based in both Los Angeles and New York, the firm will hunt for executives to fill jobs paying $40,000 a year or more, and generally, it has about 10 electronics companies as clients at any one time.

The Korn/Ferry index shows that the demand for electronics executives has doubled in the first quarter of this year by rising six percentage points over that of the first quarter of 1980 to 13% of the total national executive demand. "The electronics industries continue to hold second place [behind financial services] in executive-hiring demand nationwide," reports Mark Tomchin, who is managing vice president of the company's High Technology division in New York. "They have grown as predicted, especially with increasing demand for small home- and office-computer systems and consumer video products."

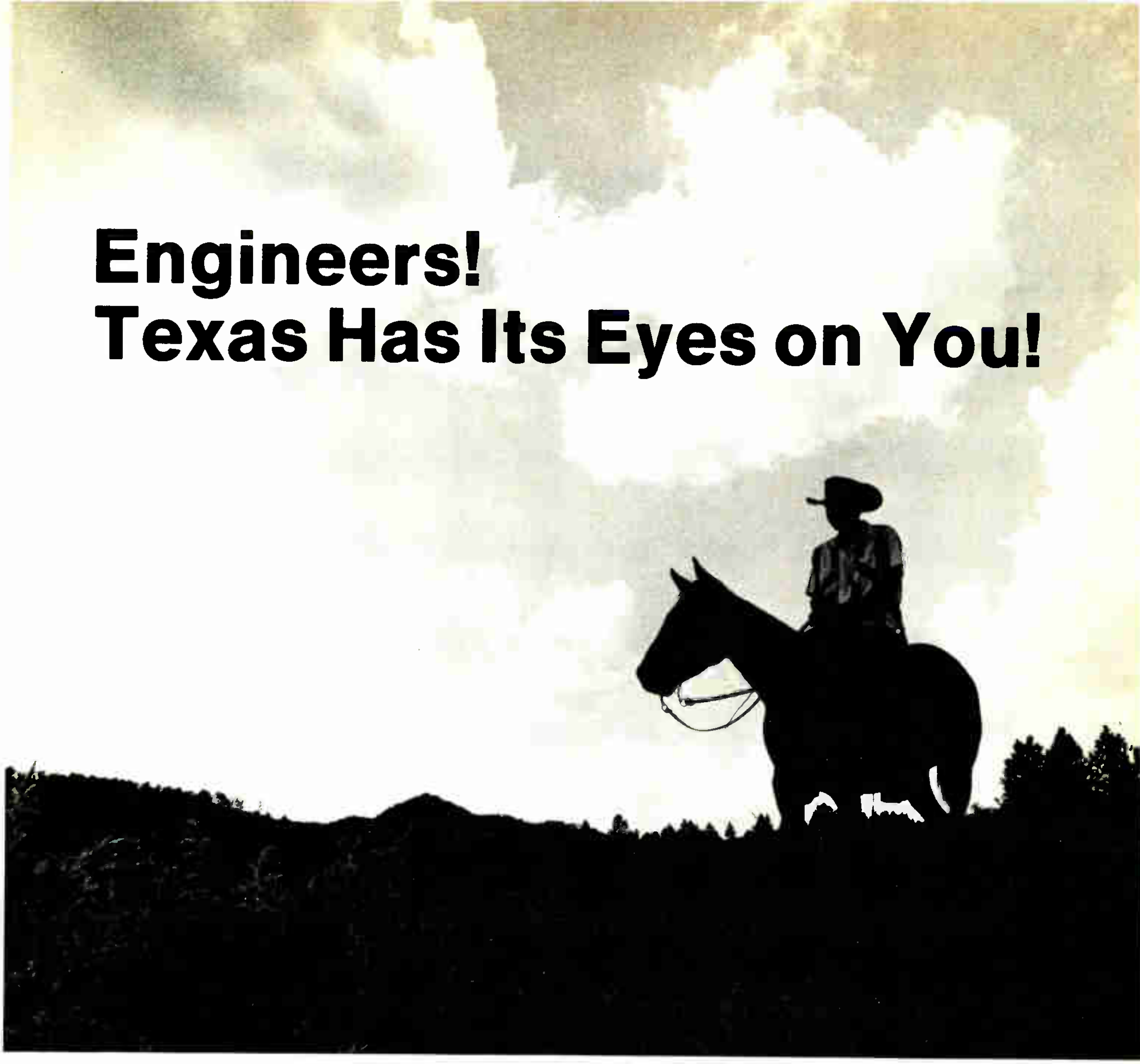
Regionally. On a regional basis, the hunt for electronics executives is more intense with companies in the East and Midwest than on the technology-crowded West Coast. "In the East the industry accounts for 18% of total demand, and in the West the figure is 16%," says Tomchin.

Interestingly, while senior executives are being sought more widely, the recruiting for middle managers is off for the quarter, according to the index. Lester B. Korn, chairman and chief executive officer of the search firm, says, "The surge in hiring of senior managers indicates a vote of confidence from our largest corporations that the outlook for the economy is more favorable in the long term, although we expect real economic growth to be insignificant during the remaining quarters" of 1981.

Most of Korn/Ferry's search requests are for marketing executives, and the company has had to open two offices in California to handle the business. The office in Palo Alto has mainly Silicon Valley firms in its electronics portfolio, while an Orange County office has a variety of electronics clients. Of the latter branch, vice president Frank Sanderson says, "There are many small, innovative medical electronics firms springing up in the Irvine area. We find a need there for marketing executives who have experience working with distributors."



Engineers! Texas Has Its Eyes on You!



The eyes of Texas are indeed upon you if you're an engineer qualified to work in a number of different high-tech industries. Business, industry and government are all on the look-out for engineers with specializations in avionics/aerospace, electrical/electronics, and computer science and data processing, and have a suitcase full of enticements to convince you to pack up and head for the Lone Star State.

Texas has a reputation for doing things in a big way, and its appetite for engineers is as big as its reputation. According to the Texas Employment Commission, the number of high-technology engineers in the state grew from 68,200 in 1974 to 78,000 in 1978. By 1985, the commission projects that Texas will need 95,300 engineers, a whopping 40% increase in a little over a decade.

And the demand for engineers will remain critical, according to Gov. William P. Clements. "Industrial growth in Texas has created an urgent need for engineers in the state. Critical shortages exist and will be exacerbated from 1985 through 1995 when a large number of engineers who graduated immediately after World War II will retire," he says, adding that the shortage "will continue well into the 1990's even with the importation of 50% of Texas engineers from other states and nations."

Gov. Clements underscores the need for stronger undergraduate and graduate programs in the engineering schools, pointing out that "an increasing amount of knowledge is required to practice engineering" in today's highly complex world. "We must support better quality education at an increasingly higher level of competency, and we must graduate more engineers at the doctorate level. Engineering professors must receive adequate salaries to assure that highly trained professionals are available to meet the demands of complex technology in Texas."

The heart of high-technology Texas is a triangle-shaped area stretching from Dallas-Fort Worth in the north central part of the state, southeast to Houston, west to San Antonio and then north to Austin. Each leg of the Texas Triangle is about 200 miles long, and within it approximately four out of every five persons in Texas reside.

And more are on the way. "It almost seems like Houston has swallowed part of Detroit," says one transplanted Northerner, pointing out that as Houston's population swelled to 1.7 million last year from 1.2 million a decade before, Detroit's population nosedived from 1.5 million to 1.2 million. Looking elsewhere in the state, in just one year the Dallas-Fort Worth labor force grew 5.1% to 1.5 million, according to the Texas Employment Commission. Unemployment in Texas is in the 5.5% range, more than two percentage points below the national average.

Some of the nation's largest high-technology companies are located in the Texas Triangle, with more companies moving into the state all the time. "It's the Sunbelt syndrome," explains the recruitment director of one of the largest electronics companies in the world. "Texas is growing and our industry's growing along with it."

Many high-tech firms are offering attractive perquisites to encourage engineering talent to emigrate to the Lone Star State. Some offer financial reimbursement of relocation costs, help in finding a new home and, often, job placement assistance if the new employee's spouse wishes to work as well.

Housing costs are still generally reasonable. According to the Texas Real Estate Research Center, the average price of a home in the state in the fourth quarter of 1980 was $63,300. Average rental for a two-bedroom, one-bath apartment in one of the major cities was about $300. "There are plenty of apartments available and there's a lot of new-home building going on," says an official with a Dallas-area high-tech company.

In addition to the many flourishing high-tech firms in the state, the National Aeronautics and Space Administration sits astride the southerly apex of the Texas Triangle in Houston. Following the brilliantly successful space flight of the shuttle Columbia and the promise of more such trips to come, there has been a resurgence of interest in the nation's space program—a program that would be impossible to achieve without highly capable computer, electronic and aeronautical engineers to guide it.

Some of the finest schools in the country are located in the Texas Triangle, and engineers who want to continue their education can choose from such fine institutions as Baylor, Rice, Texas A&M, the University of Houston and the University of Texas.

Texas A&M boasts the largest enrollment of engineering students in the U.S.—almost 10,500—and by 1985 it anticipates that number will jump to 14,400, according to Robert H. Page, dean of the engineering school. The number of women studying engineering there is over 1,600 and the figure grows yearly.

As the largest star in the galaxy of Sun Belt states, the Lone Star state has more than good jobs and year-round sunshine to offer. As the second-largest state in the union, with more than 262,000 square miles of land, Texas has scenery to suit every taste. From the starkness of the desert to soaring mile-high mountain peaks, from the bustle of the cities to the peacefulness of forests, Texas has it all and then some.

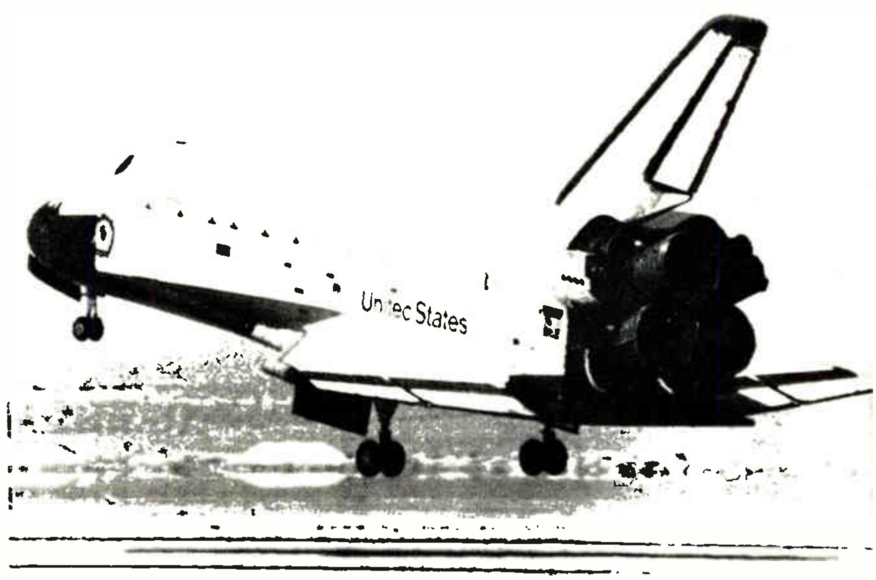
If deep-sea fishing is your bag, Galveston and the Gulf of Mexico are just a Texas-size jog down the road from Houston. Inland lakes and streams abound to the delight of fresh-water fishermen. There are about 80 state parks and recreational facilities for campers and backpackers, and over 1,000 road-side parks for picnickers.

You can't meet a Texan without talking football, and two of the finest pro teams are located in the state—the Dallas Cowboys and the Houston Oilers. Baseball buffs can catch a game at the Astrodome, watching last year's divisional championship team, the Houston Astros, make another bid for a place in the Series. Soccer and basketball fans aren't left out either—there's the Houston Rockets and Dallas Mavericks for the basketball enthusiasts, and the Dallas Tornados for soccer fans.

Texas is steeped in history and the influence of Old Mexico is evident at many of the frontier forts and museums that rub shoulders with the Rio Grande.

So grab your saddlebags, mount up and head for the Lone Star State. Engineers of all disciplines are in demand in the land where opportunity is as wide open as its spaces. To get an idea of the opportunities that await you, turn to the Career Opportunities section that follows this article and meet some of the companies that would like to give you a Texas-size welcome. —John Brand

Gov. William Clements: "Industrial growth in Texas has created an urgent need for engineers."



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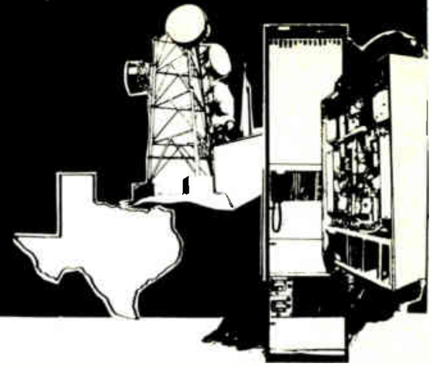

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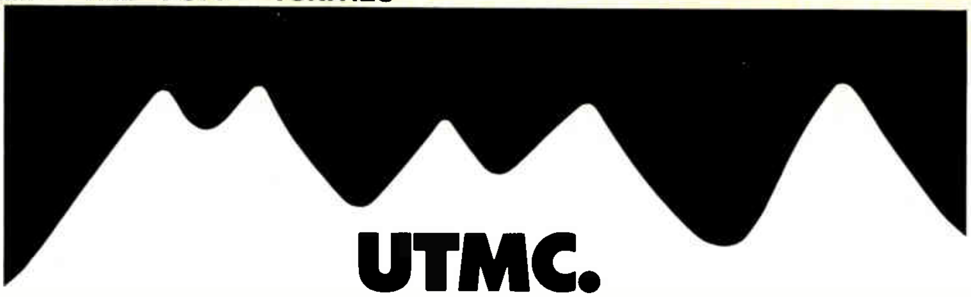

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