

DECEMBER 18, 1980

SPECIAL REPORT: TAPE AUTOMATED BONDING GAINS MOMENTUM/100

ISSCC promises ultra LSI and more/71

Bipolar transistors overpower MOS FETs at low frequencies/106



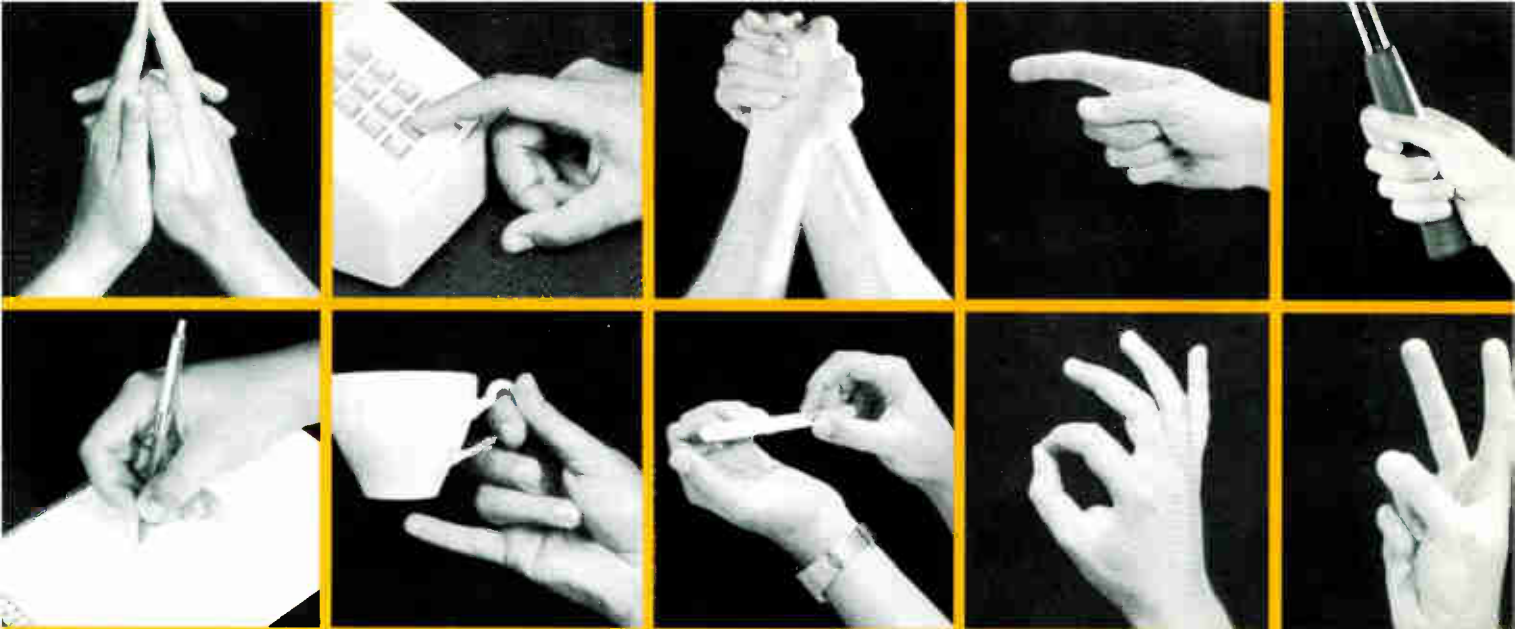
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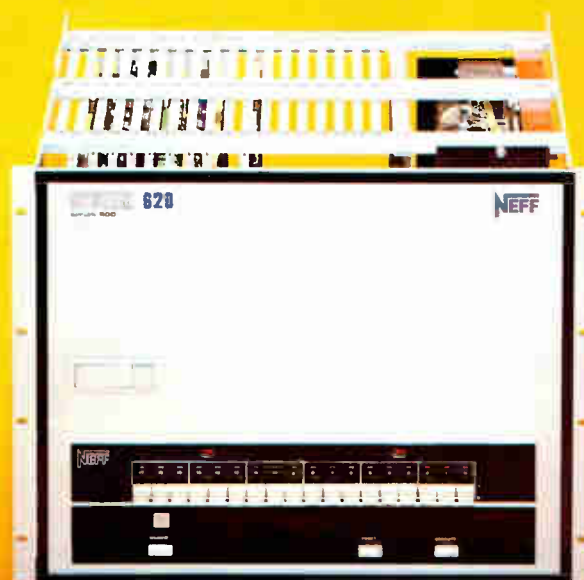
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Cover: Fiber-optic link is a snap to connect, 83

A low-cost data link for computer-to-peripheral connections of up to 20 meters simply snaps into place. And to aid designers, even nonexperts, in deciding whether it meets their needs, the 10-megabit/second transmitting and receiving system comes with a link design procedure.

Cover illustration by Sean Daly.

To test VLSI: build in or on? 76

All involved in the semiconductor industry know that very large-scale integrated circuits raise correspondingly large-scale problems for automated IC testing. Self-testing is a promising way to go, and mainframe computer makers are working on two approaches: building it onto circuit boards and building it into the ICs themselves.

Tape automated bonding heads for the big time, 100

After a decade of tryouts and road tours, tape automated bonding is preparing to take a leading role in the packaging of VLSI. Already a success in France and Japan, the technique is capable of processing thousands of chips an hour and of mass-bonding over 100 leads per chip. This special report tells who is doing what with TAB.

How to rate the power semiconductor contenders, 106

Bipolar and MOS field-effect transistors are repeatedly slugging it out in the power arena. As the promising challenger, MOS FETs have made good copy in the technical press, at the same time that bipolar devices' key advantage of low price continues to be acknowledged. But bipolar power transistors also can outpoint power MOS FETs in terms of minimum device size and operation at frequencies below 15 kilohertz.

16-K static RAMs take a byte at a time, 118

Following behind 16-K static random-access memories organized by 1 bit or by 4 bits, the 2-K-by-8-bit static part is destined for an even larger market than its siblings. Built with scaled-down processes—n-channel or complementary-MOS—it offers a lower cost per bit. Perhaps even more important, because it is organized in bytes, it will interface easily with microprocessor-based systems. This New Product Roundup takes a look at what is in production or scheduled for production by mid-1981.

And in the next issue . . .

Electronics' annual world markets survey . . . a new type of switch that combines the features of a thermistor and a circuit-breaker . . . eliminating external emi from a fiber-optic data link . . . uncommitted logic arrays that have analog as well as digital elements.

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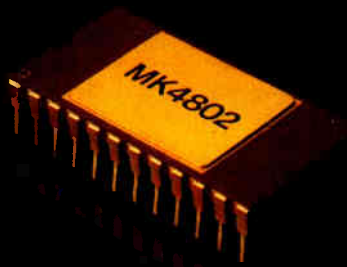
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Publisher's letter

Since the introduction of film carrier packaging by General Electric almost a decade ago, the technique has taken a remarkable course from the limelight to the back stage and out again to top billing. Film carrier packaging, now called tape automated bonding (TAB), is back because of its fortuitous match with very large-scale integration.

In fact, packaging and production editor Jerry Lyman points out that equipment manufacturers have already developed systems suitable for VLSI. For example, there are 300-lead test tapes being done now. Details of what has been going on in TAB can be found in Jerry's special report starting on page 100.

Even when film carriers took second billing, there was considerable behind-the-scenes development that will have major impact in the next few years. One group of companies primarily in France and Japan hewed close to the three-layer approach originally introduced by GE. They standardized the process and they have used it to bond chips directly to printed-circuit boards or to hybrid substrates.

Meanwhile, companies in the United States, especially semiconductor manufacturers, adapted the process to automated assembly. Here, the objective was to improve the making of dual in-line packages, not pc boards or hybrids. In any case, film carrier expertise has permeated industry.

"Its time has definitely come again," Jerry comments. "For VLSI, film carriers may be the only way to go. Not only are they here to stay, but what's more, they eventually will succeed ceramic chip-carriers as the primary package."

I wanted to provide an answer to the people who suggested that bipolar [power devices] will die. I don't think it's true." So says Philip L. Hower, semiconductor research engineer for Westinghouse Electric Corp.'s Research and Development Center in Pittsburgh. Hower's response in the form of a comparison between bipolar and MOS field-effect transistors appears on page 106.

Since joining Westinghouse in 1971, he has been deeply involved in bipolar technology, especially in the design of large-area power devices. Before that, he worked on high-voltage bipolar devices for television receiver applications while at Fairchild Camera & Instrument's semiconductor research and development laboratory.

But Hower maintains that he takes an objective view of MOS FETs. "As a bipolar person, I tended to give the benefit of the doubt to MOS FETs in the comparison. After all, we're talking about where to use silicon most effectively."

The recipient of a Ph.D. from Stanford University, he suggests that neither type of device will replace the other; instead each will be designed into systems to give the best performance for that application. He admits that MOS FETs have been getting all the attention in technical papers and product announcements. "Apparently the bipolar supporters don't feel compelled to make noise at this time," Hower observes. "I was happy to be invited by *Electronics* to do this comparison."

Hower's work on the two processes has not ended. He is involved in a continuing program to study the potential for designing a large MOS FET. "It will be interesting to see what happens next," he says.

Meanwhile, Hower believes that bipolar people like himself will become more familiar with MOS—especially at conferences.

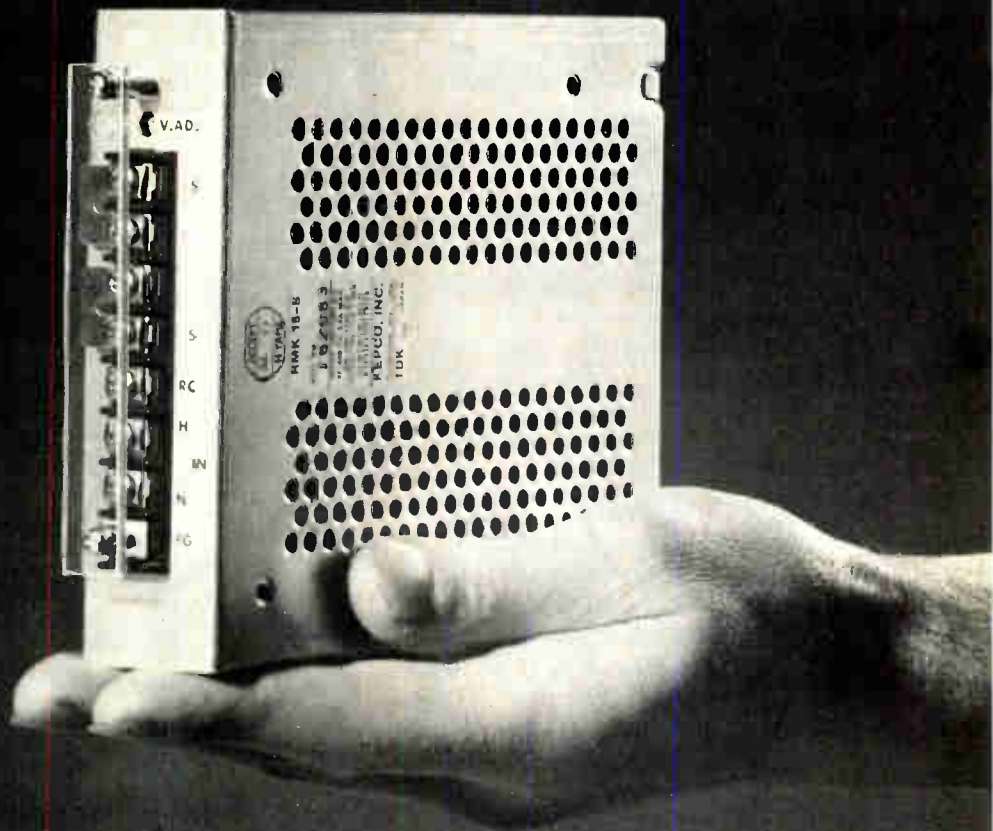
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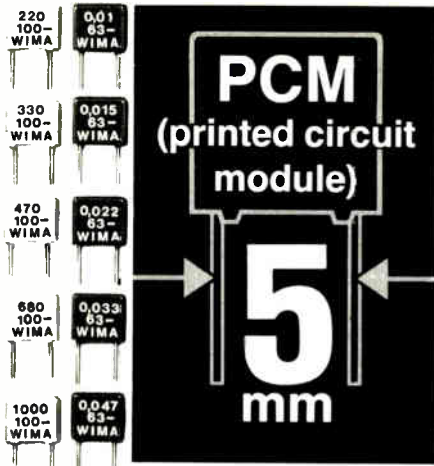


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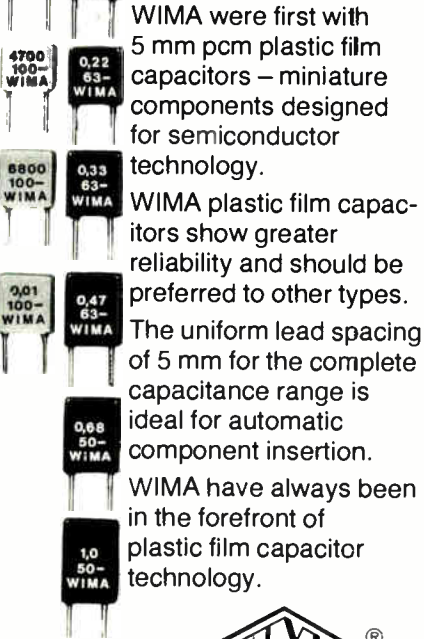
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Readers' comments

First a-d chip to market

To the Editor: In "The inside news on data converters" [July 17, p. 101], it is stated erroneously that Analog Devices has the only 10-bit analog-to-digital converter chip on the market.

The Ferranti ZN432 10-bit successive-approximation a-d converter was introduced to the world at Electronica in Munich in 1976, making it the first commercially available monolithic 10-bit device. The Ferranti ZN433 was introduced in 1977 and is still the only commercially available 10-bit monolithic tracking a-d converter on the market.

Ken Kushman
 Ferranti Electric Inc.
 Commack, N. Y.

How many gates?

To the Editor: In future gate array articles, gate counts should be subjected to a common definition that compares gates of the same size, so that readers are not misled. For instance, with the Fujitsu 3900 gate array ["Gate arrays: a special report," Sept. 25, p. 145], a gate is counted as two p-channel and one n-channel transistor. We count a gate as three p-channel and three n-channel transistors. If we were to count gates as Fujitsu does, our 2,000-gate array would have 4,000 gates.

Frank T. Deverse
 President
 International Microcircuits Inc.
 Santa Clara, Calif.

Education vs career realities

To the Editor: I agree completely with the conclusions drawn by Andrew Grove about motivating students early on to follow engineering careers [Aug. 14, p. 32], but I am afraid that his premises are totally false.

Is there really a free market in education? No. The American educational system (so-called) is dominated, impregnated, and polluted by such a mass of government bureaucracy as to be beyond belief. No way does this creature fit any supply-and-demand curve.

Why is there a problem with the

flow of career information? Because the poor wretches smothered at the bottom of the bureaucratic heap—the teachers—*don't care*. "Career counseling" is just another obnoxious demand on their time, like test grading and PTA meetings. And I doubt if you would care very much either, if you were a poor government hack caught between the parents, the students, the boards, the state, and the Feds.

Grove's article stresses the high school scene, but the situation in the state universities is even worse, with each containing within itself a group of petty bureaucracies called departments. And every year they all get together with the bigwigs for a swill-swinging ritual called "budget allocation." According to the rules, the departments that get the biggest buckets of swill are those with the greatest number of students within their bowels.

In other words, there exists a tremendous incentive for college counselors to search out "undecided" high school graduates (and the high school counselors make sure there are plenty of those) and snarfle them up for their own departments. It's warm bodies in the tent that count, not such trivial matters as the political science grads bumming quarters on street corners.

I know. I've been there. At our student-faculty meetings at the end of each academic year, our department head lied to us three years in a row concerning career opportunities in our field. (I was fortunate in being able to enter the electronics game through the back doors of Veterans Administration educational benefits, night classes, and on-the-job training).

David J. Kramer
 Sunnyvale, Calif.

Correction

The price of the fiber-optic measurement system introduced by Brookdeal Instruments Ltd., the Bracknell, Berks., England-based subsidiary of EG&G Inc., should be 16,000 pounds, rather than dollars as was previously reported (Oct. 9, p. 92).

Fluke Simplifies System Control

Fluke Obsoletes Cassette Memories in Instrument Controllers

Building efficient systems to control instrumentation places heavy demands on systems builders. There is a multitude of IEEE-488 and RS-232 instrumentation available. And instrumentation control has typically been left to calculator-type controllers. Unfortunately, the cassette tape memories used in these controllers are slow. Too slow for

the demands of programming and operating today's systems.

Two better choices for Instrument Controller Memory

Fluke has made cassette tape memories obsolete for instrumentation systems. A standard floppy disk and our own unique E-Disk™ (Electronic Disk) memory give the 1720A Instrument Controller more

speed, versatility and reliability than calculator-type controllers.

Floppy beats the cassette in more ways than speed

With the floppy, you don't have to rewind tapes or copy files to add or remove data. Because all data is stored in random access files, you shorten the data search time from seconds to milliseconds. And with our File Utility Programs and IEEE BASIC, data manipulation is both fast and easy.

E-Disk™—The Ultimate in Reliability

While cassettes can wear out or break, the E-Disk has no moving parts. It combines the best qualities of a floppy disk and advanced semiconductor technology.

For faster programming and versatile memory operations, both the floppy disk and the E-Disk™ let you implement our virtual arrays and program chaining features.

For your next instrumentation system, call your local Fluke representative to see the new 1720A. Or call 1-800-426-0361 for more information.



For Technical Data circle No. 9

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No other DMM delivers this performance under \$3,000 U.S.

Now you can improve your measurement and microprocessing capabilities at an affordable price (under \$3,000 U.S.). Fluke's new 8520A is a state-of-the-art system and bench meter with internal processing. It turns raw data into the information you can easily use.

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Analog and digital filtering techniques have been used to virtually eliminate the effects of unwanted signals and noise. This feature is extremely effective in systems where noise generated by other instrumentation is present.

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systems/bench DMM from Fluke

Readings can be captured at high speed for subsequent processing. Or they can be printed-out. Both operations had previously slowed the data acquisition process.

In systems applications, when the memory is filled, the 8520A signals the controller to gather all the data at once. This means your system can run faster because your controller isn't tied up retrieving individual readings from the DMM.

Put the power of distributed processing to work.

In your system, the internal processing of the 8520A reduces software overhead and makes your system controller more effective at doing its job, controlling instrumentation.

For bench applications, take advantage of internal processing to speed testing, improve repeatability, and reduce the factor of human error.

Complex tasks reduced to simple operations.

The new 8520A is remarkably easy to use. All functions are activated from an easy to understand panel. Even inexperienced personnel can quickly learn and use the 8520A.

For complex applications calling for statistics (standard deviation, averaged readings, variance, etc.) or dB ratios, an operator can easily initiate the appropriate program. The 8520A does the work and presents the operator with information, not the raw data.

The standard menu of programs for the 8520A includes:

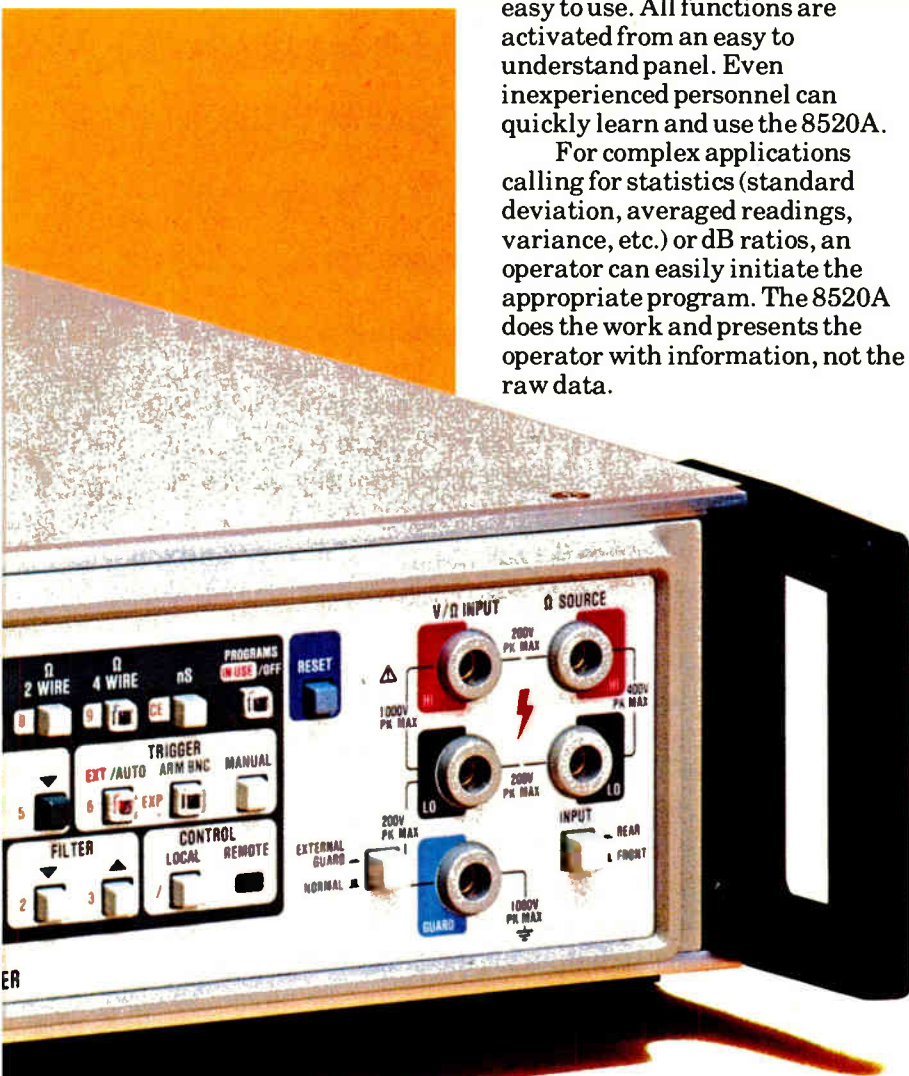
- Self Test—both analog and digital comprehensive tests
- "Zero" Program
- External Reference
- Offset, Scale & Ratio
- Percent Deviation
- Peak Storage
- Limits Testing

There's more to this powerful new DMM.

An extended math and memory package is also available for the 8520A. With it, you get 400 memory storage locations (50 locations are standard) and an additional seven math programs (above the standard seven). These include: statistics, low frequency ac, dB ratios, RTD, and thermistor temperature readings in centigrade, fahrenheit, or Kelvin. With the temperature programs, the 8520A can do the job of both an accurate thermometer and a voltmeter.

Call Fluke for the full story.

Before you invest in your next DMM, see the 8520A in action. It has the whole industry's attention. Call one of our nearby salespeople or attend a Fluke seminar on system multimeters. Or call toll-free 1-800-426-0361.



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. . . and to all a good night

'Tis the season, as if we all didn't know, to be jolly. And 'tis also the season to wish one's friends nothing but good things for the year ahead. So for 1981, even as we wonder about a new Administration, Western Europe, the Middle East, and all the woes and potential woes lurking in and about the next 12 months, these are our wishes:

- For semiconductor makers, high yields and delivery of the parts you promised in 1980.
- For memory manufacturers, an alpha-particle-free year.
- For components houses, a book-to-bill ratio of 1, no double ordering, and stable prices.
- For the same companies, an electron-beam system that you won't have to mortgage the company to afford.
- For instrument makers, a year in which the entire industry decides that the tools it *really* needs are the ones you have just released to production.
- For test engineers, having your advice sought *before* a chip is designed and hearing your automatic test equipment salesman say, "It doesn't need any new software—just give it the product number and it'll decide what to do."
- For logic manufacturers, a year in which all fuse links blow clean.
- For manufacturers of video disk, video cassette recorder, videotext, and digital audio systems, compatibility.
- For makers of speech synthesis systems, chips that sound like someone from this planet.
- For manufacturers of personal computers, \$1.98 software that works.
- For IBM-plug-compatible makers, a memo from Armonk detailing IBM's marketing and product plans.
- For makers of microcomputers and larger machines, bug-free software.
- For the manufacturers of small Winchester disk drives, a week without another new competitor announcing a product.
- For makers of toys and games, low-cost, low-power displays that are more flexible than those using light-emitting diodes or liquid crystal.
- For packaging designers, a way to attach chip-carriers directly to printed-circuit boards so that they don't pop off.
- For buyers of programmable controllers, devices that produce the warm, friendly, and familiar click of relays.
- For automobile manufacturers, electronic components with 100% reliability and zero cost.
- For engineers in California, four-bedroom, three-bathroom houses for \$60,000.
- For over-40 engineers, time off with pay to catch up with the latest technology.
- For personnel directors, the budget to hire over-40 engineers.
- For Intel's Andy Grove, a windfall of 1 million software engineers.
- And last but certainly not least, for the Institute of Electrical and Electronics Engineers, a kind word from Irwin Feerst; for Irwin, a kind word from the IEEE.

Use the microprocessor you like.

Some card manufacturers would have you believe you must use the Z80 microprocessor if you want the 'simple-to-design' STD BUS system. Not true.

Pro-Log builds 8085, Z80 & 6800 CPU cards.

Our STD 7000 CPU cards feature the three most popular microprocessors. But we don't force them on you. All our peripheral cards work with any 8-bit microprocessor you choose. And they're all totally unbundled, so you can buy one card or the whole system.

Modular by function. . .pick what you need.

We don't load our STD 7000 cards with extra functions either. That way you pay only for the functions your

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job requires. When you want to expand or change your system, just add or swap the 4.5 by 6.5-inch cards. What could be easier?

We build them to our own high standards.

Every part on every Pro-Log card is or soon will be a second-sourced industry standard. All components are 100% tested and burned-in. We're proud of our high quality and back it with a full one-year warranty.

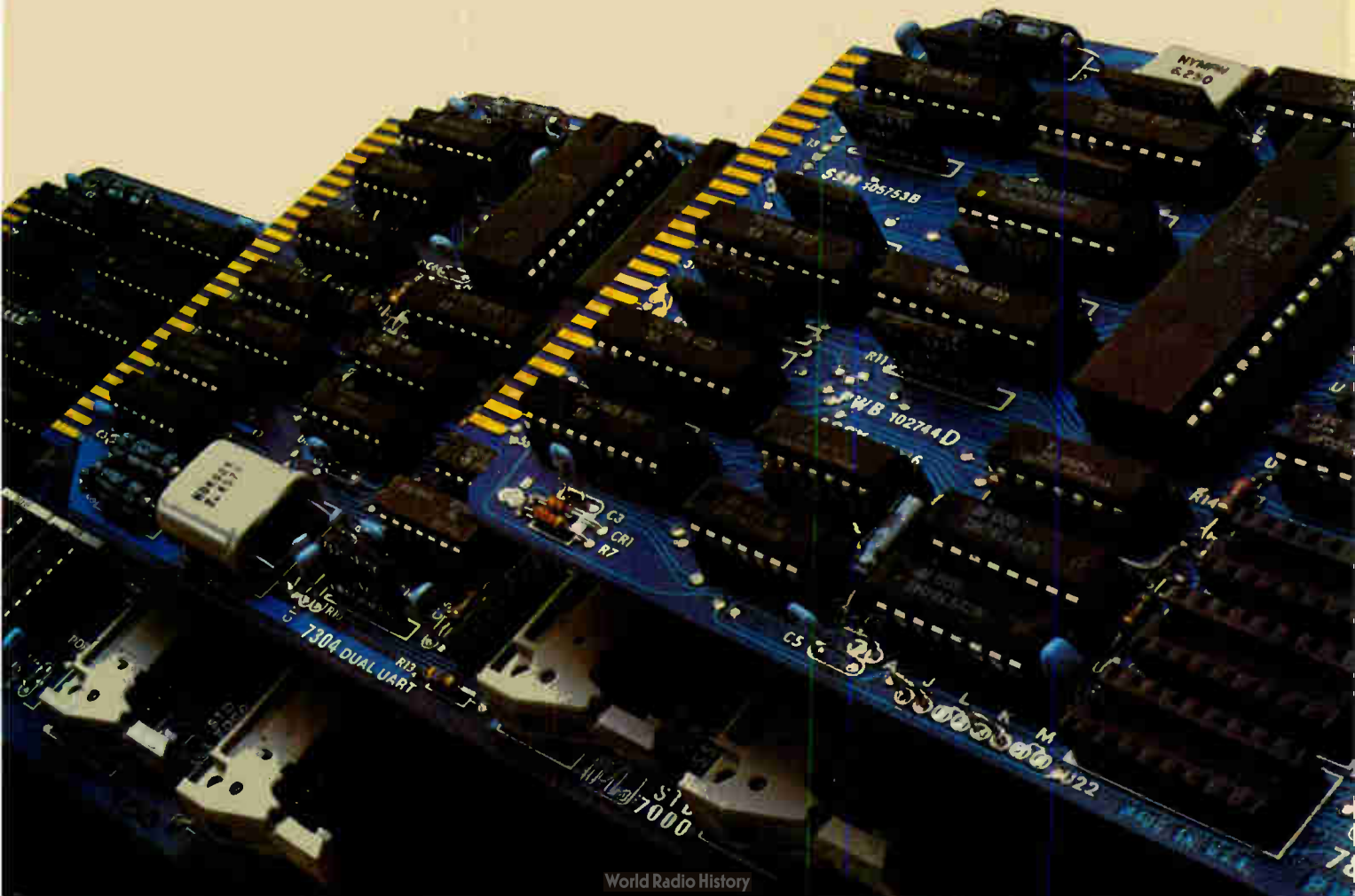
Get the facts. Send for our new 12-page STD 7000 Card brochure.

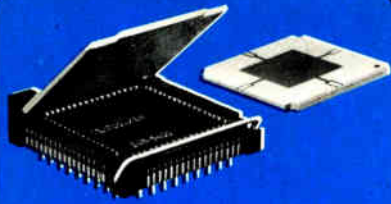
Write or call Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940, phone 408-372-4593.



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PRO-LOG STD BUS CARDS



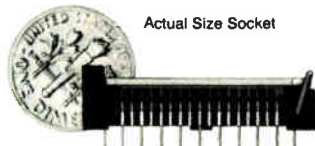


New 68 Lead Production Chip Carrier Socket

Durable, low cost Textool production socket accepts JEDEC "Type A" chip carrier package!

Designed to accept the JEDEC leadless "Type A" chip carrier package, this new Textool 68 lead socket offers the durability of a test socket while still maintaining the low cost and small size essential to a production socket.

Textool's years of experience as a leader in the manufacture of test sockets make it possible for this socket to include all those features most important to the user. Design of the socket footprint is in accordance with the JEDEC standard (.100 X .100" grid). The socket lid acts as a heatsink or can be provided with clearance for a device mounted heatsink.



Actual Size Socket

Other features include a low .342" profile for mounting on .500" centers; rugged .015 X .020" beryllium copper contacts; device to socket and socket to PC board orientation for a positive one-way fit; external probing capability; and a U.L. approved socket body material.

Now, Textool is the "one stop" supplier for your test, burn-in and production chip carrier socket requirements!

Detailed technical information on this new durable, inexpensive 68 lead production chip carrier socket, as well as Textool's full line of test and burn-in chip carrier sockets, is available on request.

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Electronic Products Division/3M**
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People

Kraemer sees real market for fiber optics in 10 years

With prices for fiber optics dropping 10% to 15% yearly, the technology for communication systems is already economical, says Arthur R. Kraemer, vice president and general manager of General Telephone & Electronics Corp.'s newly formed GTE Lenkurt Fiber Optics division. However, he adds, "The real market for fiber-optic cable and systems is probably another 10 years away, when services get into the homes of local subscribers."

According to Kraemer, the primary reasons for creating the new division are to bring together the past three year's worth of independent fiber-optic efforts at GTE and to serve as a support arm for other divisions active in the technology.

Although he does not foresee the San Carlos, Calif.-based division producing all fiber-optic components and systems for GTE, the 44-year-old Kraemer says, "We will assist in design and manufacturing, where we can produce at a cheaper cost because we are geared toward higher quantities." Many of GTE's fiber-optic products—laser diodes, light-emitting diodes, and optical connectors, among others—will continue to be made by their respective divisions. Also, GTE Laboratories will continue to grow material and process wafers and to serve as the research and development facility for fiber-optic materials.

Previously business unit manager of the electro-optics group at GTE Sylvania Systems' Western division, the 18-year GTE veteran foresees an "immediate major market in the telephone industry." The closed-circuit TV market, particularly data and surveillance applications, is running a close second. He expects users, such as railroads and utilities, to interface with GTE's new private, unregulated Communications Network Systems.

A native of Livingston, N. J., Kraemer holds a bachelor of science degree in electrical engineering from Cornell University and a master of



Union. Arthur Kraemer's new division brings together fiber work from throughout GTE.

science in EE from Stanford University. He is dedicated to hastening the marriage of fiber optics and consumer applications. Initially, he says, there will be some experimental work, such as "wired cities" to handle the combined voice, data, and video terminal needs of large companies and corporate complexes. But when electronic mail and banking services, among others, "reach the point where consumers will be willing to pay for them, that's when the market will explode. In the interim, we'll put in the backbone trunks so we can immediately handle those needs when they take off."

Solomon picks and chooses from GI's new-venture options

Although Lewis Solomon has been overseeing such activity for General Instrument Corp. for close to three years, it was not until just a few months ago that the New York-headquartered company formally made him vice president for new ventures. With a background in both marketing and engineering, Solomon, 47, is in a unique position within the company to judge the merits of would-be businesses.

"The *raison d'être* of any corporation is to bring together strengths at a high enough level so all divisions may grow," he observes. "Any company needs someone who cares and who focuses sufficient resources on

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NEW SUPER-100 MULTI-TASKING REAL-TIME SUPERVISOR

This new Real-Time Supervisor permits the execution of multiple Real-Time tasks on a priority basis. SUPER-100 can virtually place the FPS-100 in a stand-alone multi-tasking mode for the processing of multiple streams of input data with a minimum of host computer dependency.

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Select the Digital Equipment Corporation Operating System which best matches your application needs. FIRSTAR is available with either the RT-11 Real-Time Executive or the RSX-11M Resource-Sharing Executive. All Operating Systems are fully supported by Digital.

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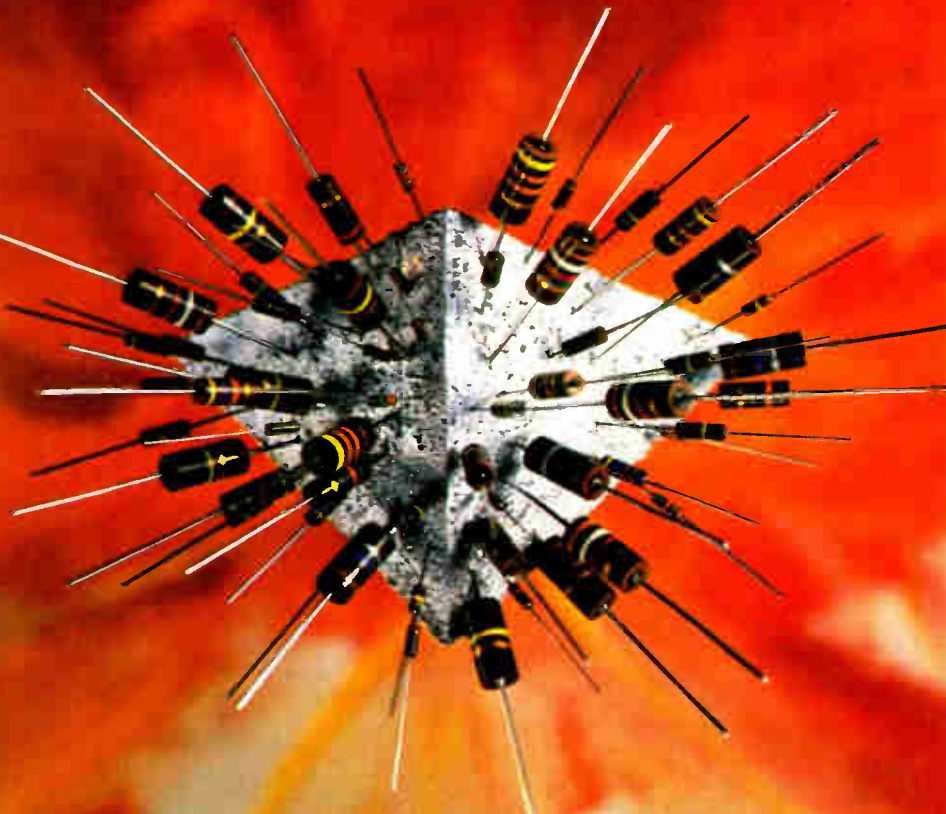
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Our standard RC Series:

- ▲ RC $\frac{1}{8}$, $\frac{1}{4}$, $\frac{1}{2}$, 1- and 2-watt sizes
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Make Stackpole your first choice in resistor products. For complete information on our carbon-comp and other resistor products, call or write: Marketing Department, Stackpole Components Co., Electronic Components Division, P.O. Box 14466, Raleigh, NC 27620. Phone: (919) 828-6201. TWX: 510-928-0520.

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Circle 16 on reader service card

People



Growth-minded. GI's Solomon believes CAD is key to future ventures for his firm.

new growth opportunities." With basic growth of 40% or more per year, GI can choose from many opportunities offered.

Solomon will continue to look to new projects that stress product programmability and flexibility. He believes one key to designing such programmability into a product in the future will be computer-aided design. "CAD is fundamental in the new-venture business because time is fundamental in getting a product to market. The quicker a company can bring a product to market, the bigger the lead it has," he says.

Some of the current projects that Solomon has been developing are:

- The planned acquisition of OTX Inc. of Elgin, Ill., a supplier of electronic slot machines. "OTX would be an extension of our systems business," comments Solomon. "We're currently in on-track and off-track parimutuel betting systems, as well as electronic lotteries. Systems for casino gambling fit our strategy."
- Playcable Inc. A joint venture of Mattel Inc. of Hawthorne, Calif., and GI through its Jerrold division in Hatboro, Pa., Playcable will supply a software package for games over cable TV networks.

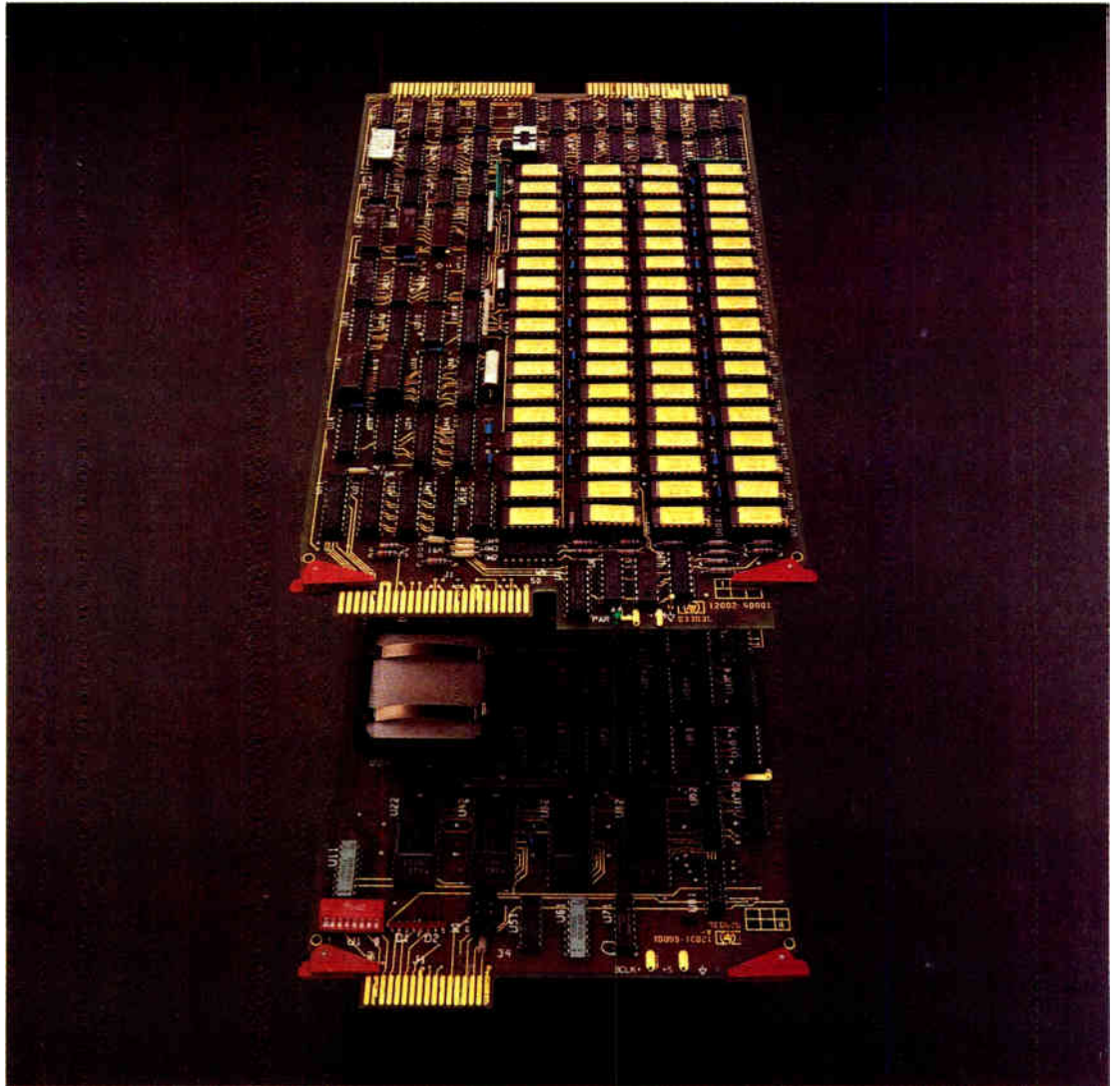
He is also in charge of a keyboard development. With the help of the corporate research and development facility in Chandler, Ariz., the Microelectronics division has been working on a new keyboard that will use an integrated-injection-logic circuit to enable GI to use one chip where competitors have two. □



MEASUREMENT COMPUTATION **news**

product advances from Hewlett-Packard

INTERNATIONAL edition DECEMBER 1980



Newly-available 64K RAMs make possible 512-K byte main memory in new Hewlett-Packard 1000 L-Series two-board microcomputer. So much main memory and computation power in so little space makes the L-Series easily adaptable to a wide range of applications—good news for OEMs.

HP's new two-board, half-megabyte microcomputer: small hardware with big software

By combining newly-available 64K RAMs with enhanced memory management capabilities, the low-cost HP 1000 L-Series computer is now available as a powerful 512K byte, two-board microcomputer.

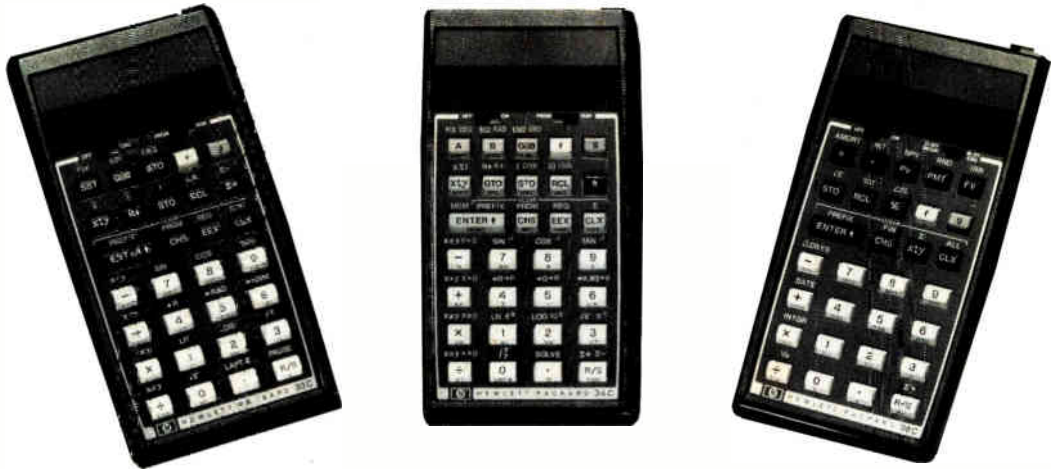
With a half-megabyte of state-of-the-art memory on one 6¾" x 11" (17.2 x 28.9 cm) board and a single-chip, Silicon-Sapphire CPU on the other board, the L-Series gives OEMs significantly expanded design freedom at the upper end of the microcomputer spectrum. That amount of main

memory and computation power in so little space makes the L-Series easily adaptable to a wide range of applications that previously were too complex or demanding to be met by the use of microprocessors or microcomputers.

The L-Series microcomputer is particularly well-suited to applications requiring high-speed I/O rates, such as communications front ends, data concentrators and message switchers. Other applications include data acquisition, in-

(continued on last page)

HP-33C, 34C and 38C calculators with continuous memory—they're ready when you are



These advanced programmable calculators from Hewlett-Packard retain your programs and data even after they've been turned off. Just think how much more quickly and easily you'll be able to solve your business or scientific problems.

But these remarkable calculators do more than just remember. For example, consider the HP-33C: with eight user-storage-registers and a program capacity of 49 fully merged lines, the HP-33C's programming capability can help you perform repetitive scientific calculations with pushbutton ease.

The HP-34C has advanced programming to handle frequent repetitive problems plus a full set of preprogrammed scientific functions including "Solve" and "Integrate." "Solve" finds real roots for an incredibly wide range of functions. "Integrate" computes the area of a function bounded by upper and lower limits. Other features of the HP-34C include 12 addressable labels, insert/delete editing, and a

controlled memory that varies between 210 program lines and 21 user storage registers.

The HP-38C offers a multitude of built-in financial functions, as well as 99 programming lines for easy-to-master programming capability. Discounted cash flow analysis, NPV or IRR are quickly and easily done by keying in the known values for a number of periods (n), interest (i), present value (PV), payment (PMT), or future value (FV), and then asking for the unknown.

Hewlett-Packard supports the Continuous Memory calculators, HP-33C, 34C and 38C, with comprehensive instruction manuals and many software solutions books for applications in science, engineering, and business.

For more information, check **A** on the HP Reply Card.

Telecommunications Test Equipment

New error measurement system interfaces with Bell digital equipment

The Hewlett-Packard 3781B Pattern Generator and the 3782B Error Detector form a dedicated error measurement system for testing and evaluating the performance of Bell-compatible, digital transmission systems. In one compact system, it has four bit rates relating to the DS-1, DS-1C, DS-2 and DS-3 levels. This forms an ideal system for production testing, field maintenance and commissioning of digital transmission over cable, radio, satellite or fibre optic links.

Based on microprocessor design, the 3781B/3782B provide a comprehensive measurement capability, including in-service error measurement. Binary, code or parity errors can be measured and displayed as error rate, error count, error seconds or error free seconds over a wide choice of gating periods.

Check **B** on the HP Reply Card for full information.



The 3781B Pattern Generator and 3782B Error Detector interface fully with the HP-IB for bus-controlled operation and automatic measurement sequencing.

Convenient scaling, calibration and remote pen control added to HP's 7040 series X-Y recorders

Four valuable, ease-of-use features have been added to three of HP's 7040 series X-Y recorders: the Model 7044B medium speed, general-purpose lab recorder, the Model 7045B high-speed, general-purpose lab recorder, and the Model 7046 two-pen high-speed lab recorder.

The new features are:

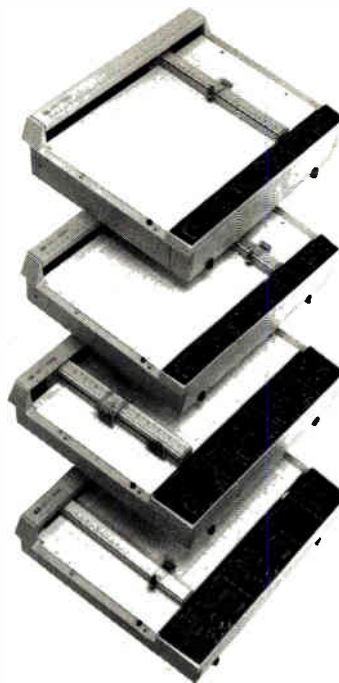
1. Convenient 1,2,5,10 scaling from .25 mV/cm (.5 mV/inch) to 5 V/cm (10V/inch) for quick set-up of calibrated graphs;
2. A 10 turn-vernier control for quick set-ups of non-calibrated graphs;
3. Separate calibration-vernier switch to change in and out of calibrated operation without moving vernier;
4. Additional remote pen lift control on rear panel banana jack receptacle.

Exceptional accuracy is achieved through rugged single-piece castings to ensure long-term alignment. A servo loop which closes at the pen tip, eliminates the inaccuracies introduced by gear and other mechanical wear. Operating under adverse conditions, these recorders greatly exceed specifications under normal laboratory use.

For example, the pen mechanism is constructed to exceed 50 kilometers (31.07 miles) of pen travel (about 5 years of normal use) without needing adjustment.

A graphic system accuracy of ± 0.2 percent is achievable with a combination of HP recorder, HP pens and HP paper, all carefully designed and crafted toward producing this highly accurate performance specification that delivers high-quality traces.

A number of other features contribute to the convenience of using 7040 Series recorders. Electrostatic holddown keeps the paper accurately fixed. HP pens are designed to provide a uniform line width through all pen velocities and weeks of cap-off use without drying out. The ink dries by absorption rather than evaporation, making it smear proof. HP paper is printed at 50 percent relative humidity and is cut with the



grain running at a 45° angle to minimize environmentally induced paper changes.

Optional time base and event marker are available to provide a full range of laboratory recording needs.

The 7044B, 7045B, and 7046B are available with either English or Metric calibration.

For more information, check **C** on the HP Reply Card.

Telecommunications Test Equipment



70 MHz modulator/demodulator allows baseband measurements at non-demodulating repeater stations

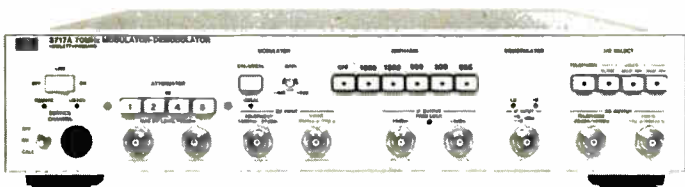
Hewlett-Packard's new 3717A 70 MHz Modulator/Demodulator is a portable test modem for use on 70 MHz IF heterodyne microwave radio links. Its primary application is to provide a baseband (BB) interface at non-demodulating repeater stations. The 3717A lets you carry out hop-by-hop,

conventional BB-BB qualitative measurements such as white-noise loading, video distortion and BB frequency response. In some instances you can substitute the 3717A for a link's own modem equipment.

Some of the many valuable features which make it possible to use HP's 3717A on a variety of microwave radio systems include:

- Provision for both video and telephony signals
- Up to five built-in selectable pre/de-emphasis networks
- Audio service channel available
- Demodulator input level range—10 to +6 dBm
- Variable modulator input sensitivity
- Built-in general-purpose attenuator
- HP-IB controllable for system surveillance applications
- Optional separate modulator or demodulator sections

For more information, check **D** on the HP Reply Card.



Perform BB qualitative measurements at IF repeaters using HP's new 3717A 70 MHz Modulator/Demodulator.

New HP printing terminal combines performance, mass storage and portability

The new HP 2675A is a versatile, 120 cps thermal printing terminal that combines sophisticated firmware design, ease of use, mass storage and portability.

The 22-pound terminal executes over 60 powerful commands with just a few simple keystrokes and features extensive escape sequences, compatible with the HP 2640 family of display terminals. Eight user-definable soft keys, a definable return key and complete editing capabilities augment the terminal's friendly versatility. Since terminal parameters such as page format and the two data communications structures are stored in soft, non-volatile configuration, they may be quickly defined and altered through the terminal COMMAND language. The 2675A has an RS232-C serial interface and supports multiple handshake protocols.

Fast dual cartridge tape drives feature updatable or compact record modes providing 320K bytes of storage per tape. Recorded information can be located by searching for absolute/relative record or file, file name, or string.

Printing capabilities include full 128-character ASCII with true descenders, national and line drawing character sets, and underlining and framing character enhancements. In addition, expanded and compressed printing modes provide a choice of 40, 80 or 132 columns. The standard character ROM provides character sets for six foreign languages.

For more details, check **E** on the HP Reply Card.



New thermal printing terminal for asynchronous communications as fast as 9,600 bit/sec offer selectable columns, and eight user-programmable softkeys and built-in phone jack.

(C) MEASUREMENT/COMPUTATION NEWS

"Flexible" memory systems available for HP-85



The HP-85 Mass Storage ROM, 00085-15001, provides convenient access to these disc memories through simple BASIC language commands. When you turn on the HP-85, the disc memory is totally integrated into the personal computer.

The power of random access mass storage is available to HP-85 Personal Computer owners through a progressive range of high-quality, double-sided, double-density flexible disc drives from Hewlett-Packard. Designed to meet the expanding application needs of professionals, the HP 82900 Series and HP 9895 Flexible Disc Memories offer graduated storage capacities through various configurations.

The HP 82900 Series adds from 270K to 1.08M bytes of on-line storage using 5¼" removable flexible discs. The HP 9895A provides from 1.18M to 4.72M bytes of mass storage using double-sided, double-density format on 8-inch flexible discs.

Both single and dual drives are available as masters (with controllers) and add-ons (must be used with the master). With these discs, large amounts of data can be quickly stored and read randomly. Also, very long programs can be stored on disc and "chained" into the HP-85. Data is transferred at 350 bytes per second and programs at 1.5K bytes per second. Average access time for both discs is 187 m/sec.

Approved media is available directly from HP. Through extensive testing, selection and control, these HP qualified flexible discs bring out the most reliable performance in your system.

For more information, check **F** on the HP Reply Card.

New HP Data Logger has full computation and analysis capability

Accurate measurements with full computational and analysis capabilities in HP's friendly new 3054DL Data Logger provide a powerful economic solution to transducer measurements, research and development, and production testing applications. HP's graduated, three-level software for the 3054DL enables the operator to start logging data immediately—without programming experience.

The 3054DL consists of a 5½-digit scanning DVM, low thermal scanner (multiplexer), ohmmeter, current source, real-time clock, HP-IB and the powerful HP 85F computer in a 16-inch high cabinet. Depending on the application, the HP 85F can serve as a dedicated computer for the 3054DL or as a separate computer when data logging is not taking place. For such occasions, HP offers HP 85F application software for mathematics, general statistics, electrical engineering, linear programming and regression analysis.

When data logging, the computer's printer can be used to show trend information or results of a test. Graphical plots and histograms, for example, can be made to gain insight into the process the operator is logging. The CRT display makes channel set-up easy. By typing simple commands which appear on the computer's CRT, you can enter data with engineering labels, store thousands of readings or convert non-linear transducer outputs into physical units. There is no need to learn a computer language.

Graduated Data Logging Software

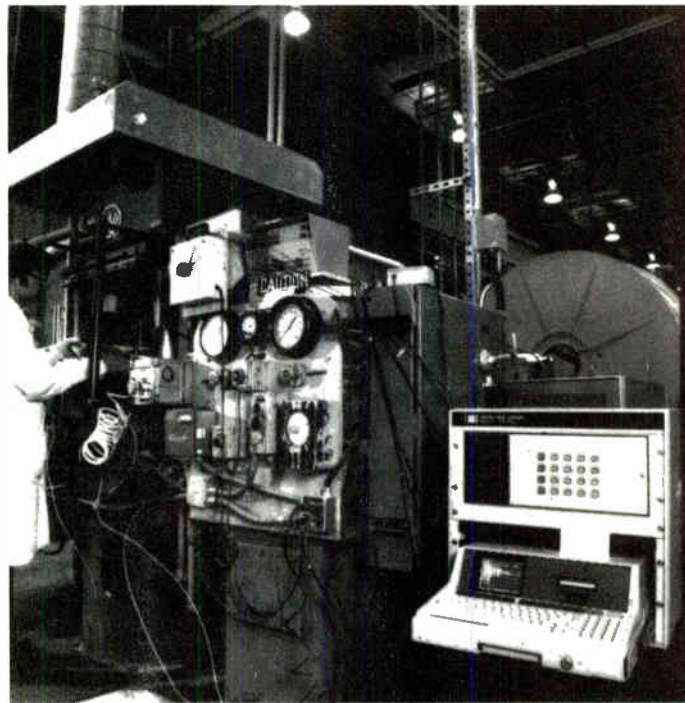
Three graduated levels of data logging software are available with each HP 3054DL. Level "one" software is a "menu-

data" entry method that enables the user to begin data logging immediately. Level "two" software offers line entry instructions for the operator to test for limits, print the logged data and/or close a relay if a limit does not meet specifications. Level "three" (optional) software enables the operator with minimal knowledge of BASIC to utilize the system's entire 32K and convert the data logger into a powerful data acquisition system. This level also features a group of pre-written subroutines which can be called to perform specific tasks. For example, transducers can be linearized and logged data can be stored on a tape cartridge. Two-variable graphs of the data can then be plotted using statistical histogram routines to determine distribution of the logged data. Level "three" comes with a comprehensive set of documentation capable of handling most complex measuring situations without requiring the operator to become a computer expert.

When logging data from transducers such as thermocouples and strain gauges, the autoranging voltmeter in the 3054DL makes excellent precision low level measurements. Resolution is 10 ppm, accuracy is $\pm 0.007\% + 1$ count and sensitivity is 1 milliohm, 1 microvolt and 0.1°C. Noise rejection is >150 dB ECMR and >60 dB NMR.

Up to 100 analog channels (20 channels per card) or up to 80 digital input/output slots (16 channels per slot) are available with plug-in assemblies. An autoranging frequency counter is also available for logging frequency and/or totalizing data.

For more information, check **G** on the HP Reply Card.



Easy set up, accurate measurements, linearization data reduction, display, hard-copy graphical plotting and storage on magnetic tape — enable the HP 3054DL to perform the whole data logging task. This powerful yet easy-to-master system offers an economic solution to production and research applications.

Accurate, intelligent pulse source for research/maintenance—now with confirmation software

When you require precision pulses, the benefits of rapid integration, easy HP-IB programming and microprocessor control are yours with HP's 8160A Programmable Pulse Generator.

The generator's built-in test, which provides visual and bus information, is now augmented by new confirmation software. Available as a mag tape cassette with HP-IB verification, performance check and adjustment programs, this software speeds servicing as well as proves specifications. This capability also allows you to be certain of system performance and to reduce down-time to a minimum.

The 8160A brings 1-3% accuracy to pulse settings and, with option 020, full 2-channel programmability of all pulse parameters. Accurate channel delay with independent control of the pulse shape in each channel is ideal for fast, reliable propagation measurements in module maintenance programs.

Many operating conveniences—such as non-volatile memory for rapid parameter and mode selection, and learn mode—save you time in integration, training and use. Accurate programming obviates the need for monitoring and therefore saves you hardware.



For further information, check **H** on the HP Reply Card.

Even the trigger levels are programmable in our lowest cost systems counter



HP's new 5316A Universal Counter provides all the Hewlett-Packard Interface Bus (HP-IB) capability you're likely to need in a reciprocal-taking universal counter at low cost.

You can save money, and get excellent performance too, with HP's new 5316A Universal Counter in your bench top or rack-mounted systems. All its major functions are HP-IB programmable. This includes trigger level programming, which is an expensive option in most other counters.

Frequency range of this economical, versatile, microprocessor-based instrument, is 100 MHz (1 GHz optional). It also measures time interval and period to 100 ns, time interval average to 10 ps, frequency ratio, and it will totalize too. The counter's reciprocal-taking frequency mea-

surements provide eight digits of resolution while its several digits of resolution-per-second of gate time is particularly useful in measuring low frequencies rapidly.

Radio frequency interference (RFI) is very low, and an option is available to normalize readings to engineering units and apply reading offsets.

Check **I** on the HP Reply Card.

HP's applications manual now offered at special price

Hewlett-Packard's **Optoelectronics Applications Manual**, published by McGraw-Hill, is now being offered at a special reduced price from your HP components distributors.

The **Optoelectronics Applications Manual** covers such subjects as photometry/radiometry, contrast enhancement in visible displays, and reliability of optoelectronic components and their mechanical handling. Designed both as a practical guide to the use of optoelectronic devices and as a foundation for the development of new design ideas, this volume demonstrates the broad potential for these components that exists in systems being designed today.

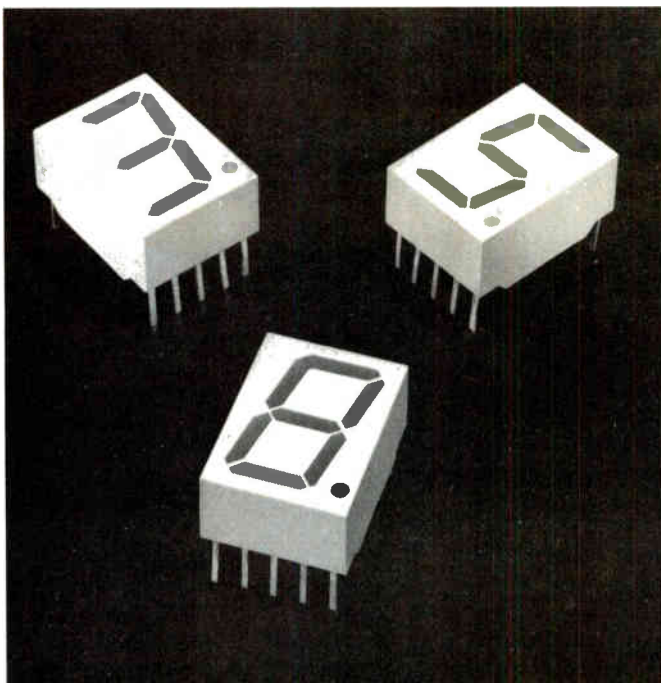
Of special interest to experienced designers is the OA Manual's treatment of CTR degradation, a controversial and frequently misunderstood subject among users of optically coupled isolators.

Copies may be purchased from your authorized HP distributor.

For more information, check **K** on the HP Reply Card.



New, 7-segment displays increase light yield plus provide efficient character size-to-package ratio



This new, 14.22-mm (0.56 in), seven-segment display is the brightest yet with the most efficient character size-to-package ratio from Hewlett-Packard. Designers now using HP's 10.92 mm (0.43 in) display can move up to this 14.22 mm (0.56 in) character family without using more panel space. Package size is only 12.573 mm (0.495 in) wide by 17.02 mm (0.673 in) long and 8.00 mm (0.315 in) deep. Light yield has been increased by a special leadframe design.

Red is designated HDSP-5300; high-efficiency red is HDSP-5500; yellow is HDSP-5700; green is HDSP-5800. All displays are categorized for luminous intensity. Yellow and green are also categorized for color. Such binning assures aesthetic uniformity in front panel displays.

Contrast and readability are optimized because of the gray scrambler body used. Character height allows good viewing at distances up to 7.01 m (23 ft). A wide viewing angle and uniform appearance are achieved by using mitered segments.

These new, full-color 14.22 mm- (0.56 in) character displays are TTL compatible and are available in a variety of electrical configurations. Built-in stand-offs on the scrambler reduce customer assembly time, and the DIP package accommodates standard printed circuit board layouts.

For more information, check **J** on the HP Reply Card.

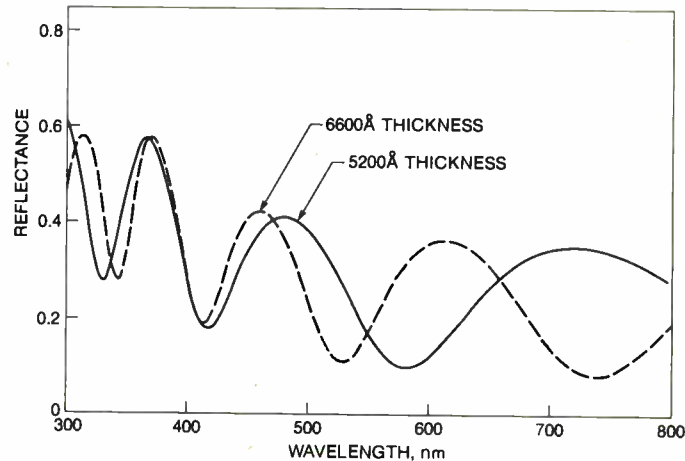
New reflectance accessory adapts spectrophotometer for precise, high-speed thin-film measurements

A new specular reflectance accessory, the HP 89007A, readily adapts the high-speed, microprocessor-controlled HP 8450A UV/VIS Spectrophotometer for measuring thin film thickness from about 1000 angstroms to several microns with a precision of 2% at 1σ ! Data are displayed on the built-in CRT in seconds and can be plotted as shown.

Ultraviolet-visible spectrophotometry is a well-accepted technique for fast, accurate thickness measurements of thin films. However, to be cost-effective this technique requires a spectrophotometer like the HP 8450A, capable of fast data acquisition and analysis. Its advantages can help achieve even small percentage increases in yield due to better control of photomask optical properties—in some cases this can mean savings of thousands of dollars per month.

The HP 8450A also makes an excellent choice for other semiconductor applications such as characterizing photoresists, measuring optical properties of photoplates and wafers and determining surface roughness from less than 100 angstroms to about 3 microns.

Check **L** on the HP Reply Card.



Actual plot of changes in spectral maxima and minima which occur as thickness of silicon dioxide film (deposited on silicon wafer) varies.

A microcomputer with minicomputer software

(continued from first page)

dustrial and lab automation, instrumentation and process control tasks where large main memory and high throughput are required.

OEMs designing 8 or 16-bit single board microcomputers into their products recognize that the level of software support can greatly impact the complexity and length of the product development cycle. The L-Series provides designers with an array of powerful software tools to help speed and simplify their efforts. Software includes a multiprogramming, multi-user Real Time Executive operating system supporting assembler, FORTRAN 4X, BASIC and PASCAL languages. The L-Series microcomputers also can utilize IMAGE/1000 data base management software, and be part of a

DS/1000 computer network.

This not only can greatly reduce costly software development time, but also provides an upward-compatible growth path to larger systems in the HP 1000 computer family.

HP 1000 L-Series microcomputers are available as boards, as rack-mountable processors, or in fully-integrated systems. If a full half-megabyte of memory is not required, HP also offers 64K and 28K byte main memory boards.

For more information, check **M** on the HP Reply Card.

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- Which of your hermetically sealed DIP SSR's will switch 1 amp 250 VAC? Do you have a DC version?
- How can my 10 MIL logic signal control a 25 amp 250 VAC load?
- My 3-phase motor load requires an SSR to switch 2 amps at 250 volts. I'd like to do it in a single package. Can you help me?

Sorry. You missed my question. Here it is. _____

Name _____ Title _____
 Company _____ Phone _____
 City _____ State _____ Zip _____



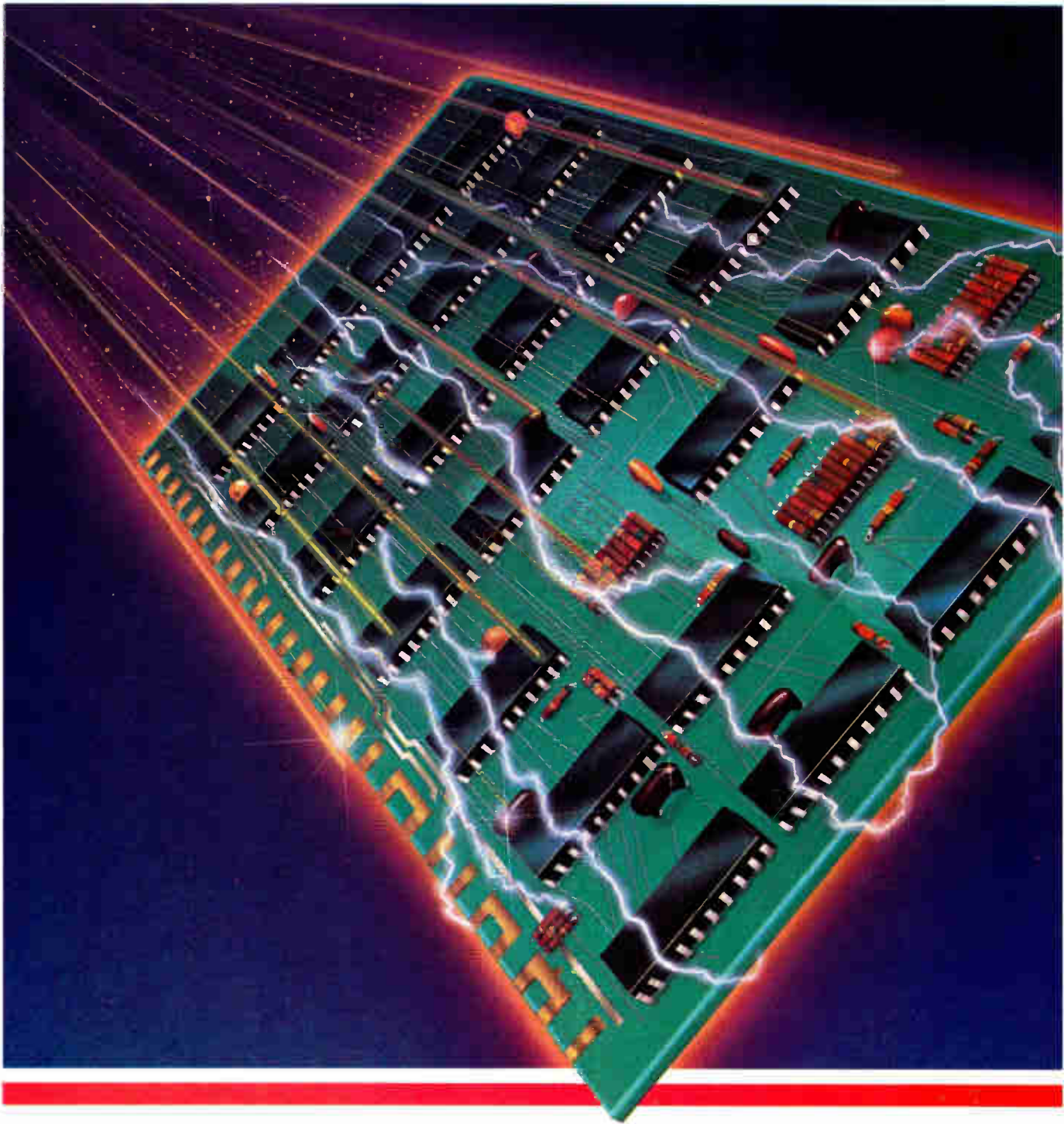
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REGISTERS

74F194 4-Bit Universal Shift Register

Shift

Frequency . . . 150 MHz typ

Clock-to-Output

Delay 4.0 ns typ

I_{CC} 33 mA typ

The 74F194 is 50% faster than Schottky and requires 65% less power. It's currently available in a plastic or ceramic package. And we have three octal shift registers planned for the near future: the 74F299, 74F322 and 74F323.

MULTIPLEXERS

Data-to-Output Delay

74F153

Dual 4-input. 5.0 ns typ

74F253

Dual 4-input with 3-state outputs 4.4 ns typ

74157

Quad 2-input 4.5 ns typ

74F257

Quad 2-input with 3-state outputs 4.0 ns typ

74F158

Quad input with inverted outputs 2.9 ns typ

Select-to-Output Delay

74F352/353

inverted versions of the 74F153/253. . . 6.3 ns typ

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Our total FAST offering.

There is a total of 30 FAST parts available now in production quantities, with additional functions coming soon. So you can upgrade your standard Schottky system or design a new system today, with Fairchild's high-speed, low-power, improved-density devices.

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To check our parts out further, order our evaluation kit that contains 14 different 74F Series devices. A total of 72 parts. Contact your nearest Fairchild sales office or distributor for our kit or information about our product delivery dates. Or call or write FAST, Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, CA 94042. Tel: (415) 962-FAST. TWX: 910-379-6435.

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Meetings

Automatic Test Equipment Seminar-Exhibit, Benwill Publishing Corp. (Test Conference Registrar, 1050 Commonwealth Ave., Boston, Mass. 02215), Pasadena Center, Pasadena, Calif., Jan. 19-22.

Eighth Plating in the Electronics Industry Symposium, American Electroplating Society (1201 Louisiana Ave., Winter Park, Fla. 32789), Adams Hotel, Phoenix, Ariz., Jan. 20-21.

Annual Reliability and Maintainability Symposium, IEEE Reliability Society, American Society for Quality Control, *et al.*, Marriott Motor Hotel, Philadelphia, Jan. 27-29.

ASEE 81—Advanced Semiconductor Equipment Exposition, Electronic Representatives Association (Cartledge & Associates, 491 Macara Ave., Suite 1014, Sunnyvale, Calif. 94086), San Jose Convention Center, San Jose, Calif., Jan. 27-29.

Second International Conference on Microprocessors in Automation and Communications, Institution of Electronics and Radio Engineers (99 Gower St., London WC1 6AZ, England), Penta Hotel, London, Jan. 27-30.

Fourth Annual SEMI Information Services Seminar, Semiconductor Equipment and Materials Institute Inc. (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Marriott Hotel, Newport Beach, Calif., Feb. 1-4.

Power Engineering Society Winter Meeting, IEEE, Atlanta Hilton Hotel, Atlanta, Feb. 1-6.

MECOM 81—Second Middle East Electronic Communications Show and Conference, Arabian Exhibition Management (TMAC, 680 Beach St., Suite 428, San Francisco, Calif. 94109) Bahrain Exhibition Centre, Bahrain, Feb. 2-5.

Los Angeles Technical Symposium, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bel-

lingham, Wash. 98225), Sheraton-Universal Hotel, North Hollywood, Calif., Feb. 9-13.

ISSCC—1981 IEEE International Solid-State Circuits Conference, IEEE, Grand Hyatt Hotel, New York City, Feb. 18-20.

Nepcon West '81, Industrial & Scientific Conference Management, Inc. (222 W. Adams St., Chicago, Ill. 60606), Anaheim Convention Center, Anaheim, Calif., Feb. 24-26.

Information Utilities '81, Online Inc. (11 Tannery Lane, Weston, Conn. 06883), New York Hilton, New York, March 2-4.

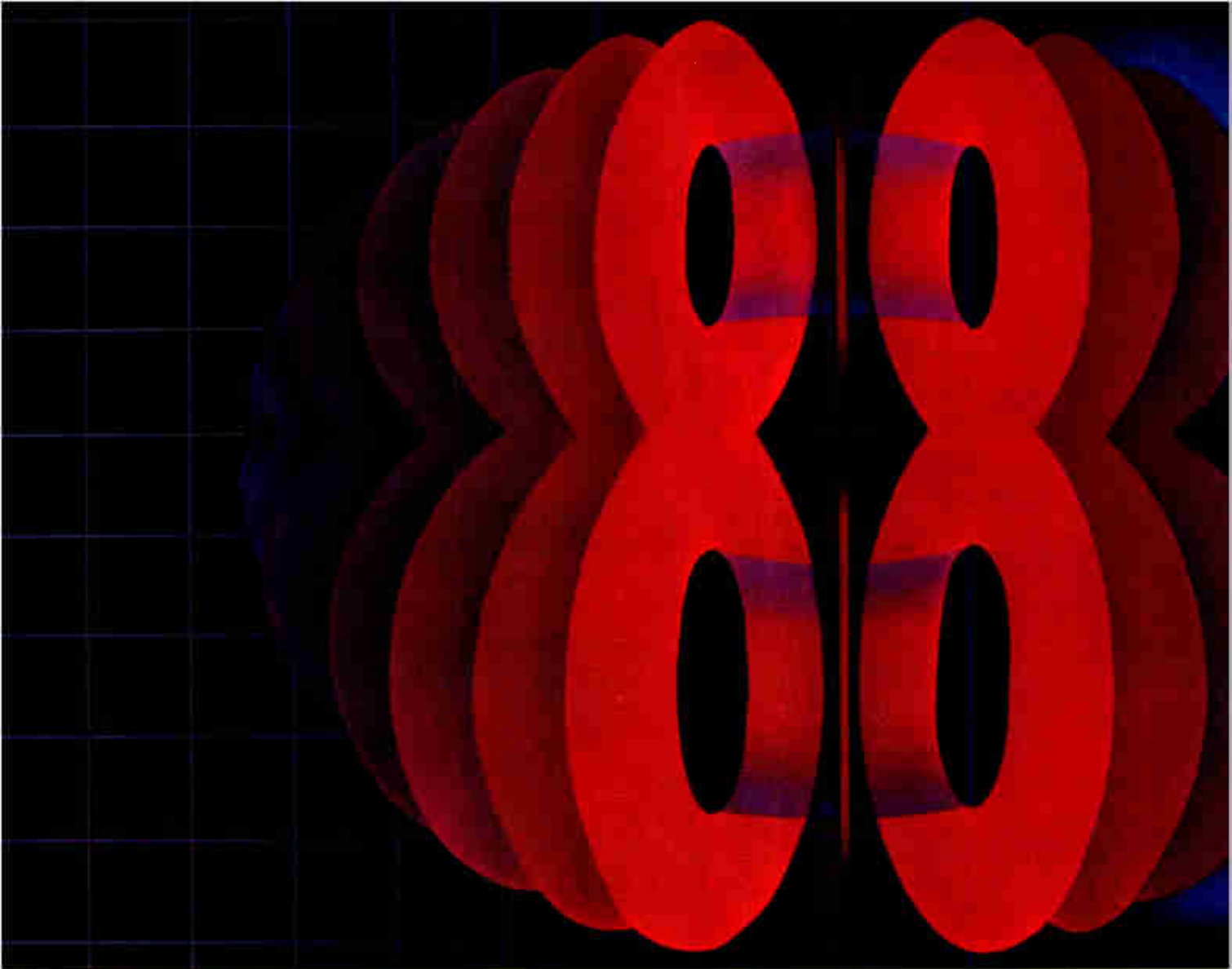
Micro-Delcon '81—Fourth Annual Conference on Computer Technology, IEEE Computer Society, Delaware Bay Section, (H. P. Morneau, E. I. du Pont de Nemours & Co., Engineering Dept., Louviers 3113, Wilmington, Del. 19898), John M. Clayton Hall, University of Delaware, Wilmington, March 10.

Fourth Electromagnetic Compatibility Symposium and Technical Exhibition, Institute for Communications Technology (T. Dvorak, The Federal Institute of Technology, Zurich, Switzerland), Federal Institute of Technology, March 10-12.

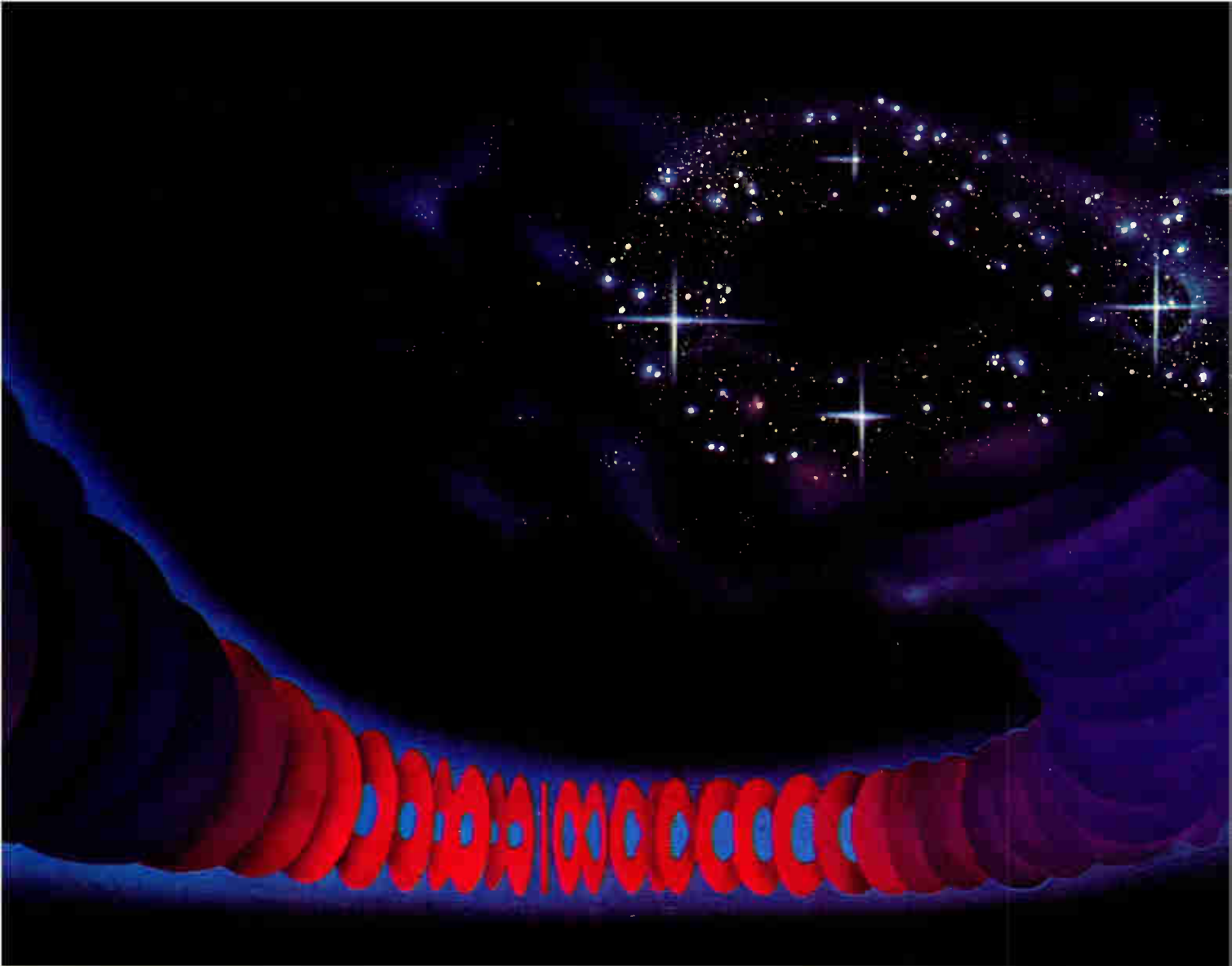
Semicon/Europa '81 and Second SEMI European Symposium on Materials and Processing, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Züspa Convention Center, Zurich, Switzerland, March 10-12.

14th Annual Simulation Symposium, IEEE, Association for Computing Machinery, *et al.*, Holiday Inn Resort, Tampa, Fla., March 16-20.

Third Annual Microelectronics Measurement Technology Seminar, Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215), San Jose Hyatt, San Jose, Calif., March 17-18.



**The 8-bit world is turning
to Intel's HMOS...**



Making the design possibilities almost infinite.

Intel's latest HMOS processor and peripheral introductions plus extensive development and software support now expand the universe of 8-bit applications.

Ever since Intel introduced the first 8-bit microprocessor in 1972, we've been the industry leader. We've always been committed to staying on the leading edge of 8-bit technology. That's what enabled Intel to be first in introducing a wide range of components, most of which are now industry standards. Today, we're continuing to apply this innovative technology both to develop new 8-bit products and to reduce costs and improve performance of existing ones.

Even more importantly, Intel always designs 8-bit parts to be members of a family of products, so they evolve in an orderly progression, as the technology evolves. By *planning* for technological change, we've been able not only to improve product performance, but to

extend product life-cycles and thus protect our customers' investments. That's the real reason why today Intel is the leading manufacturer of 8-bit microprocessors.

Expanding the 8-bit universe

For microprocessors, the greatest cost reductions and performance improvements have resulted from breakthroughs in *technology*—not volume production techniques and automation. That means breakthroughs such as Intel's advanced HMOS.*

This technology enables us to put more power and more functions on a smaller chip, and offer a range of devices that do more, while shrinking the price-performance ratio.

At the high-performance end of the 8-bit spectrum, for example, consider the new 8-bit champion: the iAPX 88. This state-of-the-art HMOS microprocessor outperforms its closest competitors in memory efficiency, ease of programming, and throughput—by as much as 4 to 1. It's also the only 8-bit microprocessor that addresses up to 1 million bytes of memory—without external memory management. And since the 8088 is the only 8-bit microprocessor whose instruction set is compatible with a 16-bit device, it's the only way you can move up to 16-bit power—such as the iAPX 86's—without sacrificing your software investment.

Or consider Intel's latest, highly integrated solution to design problems that previously required multiple chips: our new microcomputer hero, the 8051. This single-chip device contains twice as much program and data memory as

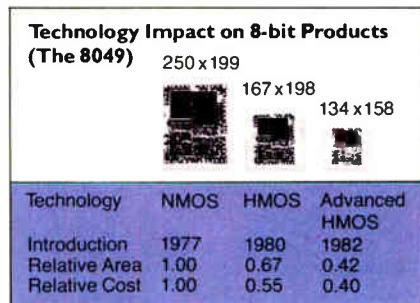


parts—like the 8085A—show similar price-performance improvements.

The key to these breakthroughs is our second-generation HMOS technology. That, combined with our pioneering computer-aided design techniques, allows transparent process conversions. Since our strategic design program allows us to plan for die-size reductions at the time of original design, we can make subsequent process conversions via CAD software, rather than having to re-design. Thus we can produce faster, lower power, less expensive devices—like the 8048H and 8085AH—while keeping identical circuitry and layouts.

The net result of these improvements is that your existing products can now evolve as Intel's technology evolves. Right now, you can improve your existing designs while lowering costs, thus extending the life cycles of your products and boosting profit margins.

Intel's Built-in Die Shrinkage Steps



Improved HMOS processors, however, constitute only a few points on the Intel 8-bit horizon. We've also used HMOS technology to enable our peripherals to cover a wide range of applications, from the 8274 multi-protocol serial controller, through the 8272 double-density floppy disk controller, to the 8741A universal peripheral interface, with on-chip EPROM memory. By doing more, these devices off-load your CPU, and increase system throughput.

HMOS also lets us build memories with a wide range of density and speed characteristics—from 16K statics through 64K dynamic RAMs, to a family of EPROMs ranging from our 2732A to our new E²PROM, the 2816. HMOS gives you the same flexibility in memory design that you have in designing other parts of your system.

Turning the competitive world around

When you want to make immediate use of the latest 8-bit VLSI technology at the board level, Intel has the solution. Our iSBC 88/25™ and iSBC 88/40 single board microcomputers, for example, will let you prototype systems or fill low-to-medium-volume production requirements rapidly. And they're only two out of eight single board microcomputers for you to choose from.

Then too, when you'd rather concentrate on your product than on re-inventing the

wheel, Intel offers two 8-bit real-time operating systems: the iRMX/80™ and iRMX/88. These operating systems are ideal for 8-bit designs, where memory space and response time are often critical. They require only 2K to 4K bytes of memory, and the iRMX/88 operating system is capable of providing up to 6000 samples per second in your real-time application.

Finally, to speed development time, we offer a full complement of development support tools. Such as the latest development system technology, the new Intellec® Series III. With its dual processor architecture, the Series III is ideal for 8088 development work. Then there's the Series II, and the new, low-cost Model 120—the choice for entry level 8085 or 8048/8049 microcontroller designs. As part of a planned path to protect your investment, both the Series II and the Model 120 are upgradable to the Series III, and further to the NDS-1 development network. And, by applying the same computer-aided design techniques we use to shrink our chips, we're also able to build bond-out chips for use in our ICE™ in-circuit emulators. So our ICE modules perform exactly the same way in your circuit as the original chip. Plus they're ready to go, as soon as a new chip is available.

To further reduce development time and enhance programmer productivity, Intel supports these hardware systems with the broadest range of development software available today. Up to five language translators, including Pascal, PL/M, FORTRAN, COBOL, and BASIC. Four different macro-assemblers. An extensive set of programmer utility routines. So you can always match the right language or program to the job—and offer your customers a way of further developing your products if they wish.

All of which means that now it's easy, convenient and cost-effective to get the most out of Intel's 8-bit world of advanced technology. And make your product design possibilities almost infinite. With these technology advantages, this degree of commitment to 8-bit users, this breadth of product line, and this level of development support, it's no wonder the 8-bit world is turning to Intel's HMOS.

Our new brochure gives further details on Intel's 8-bit world. You can get your copy by circling the reader response number, or contacting your Intel sales office/distributor. Or writing Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

Europe Intel International, Brussels, Belgium
 Japan Intel Japan, Tokyo
 United States and Canadian distributors Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L. A. Varah, Wyle Distribution Group, Zenitronics

intel delivers solutions

competitive parts; provides up to 10 times as much speed as the 8048; and offers a unique Boolean processor—particularly important in controller applications.

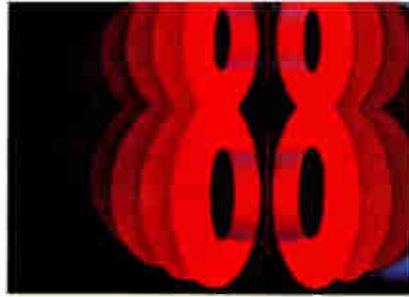
iAPX 88 Performance Comparisons

	iAPX 88	Z-80	MC6809	8085A
Relative performance	1 (5MHz)	0.4 (4MHz)	0.6 (2MHz)	0.3 (3MHz)
16-bit object code compatibility	8086	NONE	NONE	NONE
Relative assembly language code required	1	1.5	1.4	1.5
Memory/IO address space	1 Megabyte/ 64K	64K/256	64K/NONE	64K/256
Multi & co-processing	YES (with 8087, 8088)	NO	NO	NO
PASCAL, PL/M & FORTRAN	YES	NO	NO	YES
ICE symbolic debugging	YES	NO	NO	YES

Shrinking the 8-bit world

As part of a long-range plan to apply advanced HMOS technology to our existing products, we've developed versions of numerous parts that deliver greatly enhanced price-performance. Take our industry-standard 8048, for example. The new 8048H versions of this single-chip microcontroller now offer up to 80% more speed, at 67% less power. Other established Intel® 8-bit

The New World of Intel's 8-Bit HMOS



Intel's 8-Bit Microprocessors and Support

Microprocessor	Replaces	Description	Evaluation Kits	In-Circuit Emulators
8048H/8748 8048L	8048	Microcontroller New 11 MHz and 8 MHz CPU speeds; up to 70% lower power; on-chip EPROM at new lower price	PROMPT-48	ICE-49™
8049H/8749 8049L	8049	Microcontroller Same speed selections as 8048H; now available with 2K byte on-chip EPROM		ICE-49™
8051/8751	NEW	Microcontroller Intel's newest high integration micro with on-chip serial port; Boolean processor; 12 MHz CPU and 4K byte on-chip EPROM	SDK-51™	ICE-51™
8080A		Microprocessor Intel's original 8-bit processor, recently upgraded	SDK-85™	ICE-80™
8085AH	8085A	Microprocessor 30% lower power; 10% voltage margins; new high performance 6 MHz version	SDK-85™	ICE-85™
8088	NEW	Microprocessor Highest performance 8-bit CPU; 1 Mbyte address range; 16-bit instruction set; multi-processor support	SDK-86™	ICE-88™
iSBC 88/25	NEW	Single Board Computer 8088-based, with Multibus™ expansion, coming mid '81		
iSBC 88/40	NEW	Single Board Computer 8088-based measurement and control computer		

Intel's 8-Bit Peripheral Controllers

Model	Replaces	Description
8202A		Dynamic RAM Refresh Controller Makes dynamic RAM look static, handles refresh, address multiplexing and arbitration
8272	NEW	Double/Single Density Floppy Disk Controller Interfaces 8- or 16-bit CPU to four floppy disk drives; IBM-compatible formats
8274	NEW	Multiple Protocol Serial Controller Speeds up to 1M baud; protocols can be async, bisync or synchronous (HDLC/SDLC)
8276	NEW	Small System CRT Controller Allows complete CRT system implementation with less than 20 devices
8041AH/ 8741A	8041A	Universal Peripheral Interface Controllers with new 12 MHz and 8 MHz CPU versions; slave processor interface
8232	NEW	Floating Point Math Processor Four function 64-bit floating point operation; IEEE compatible; 4 MHz clock
8291, 8292		IEEE-488 GPIB Controller Talker/listener and controller functions for 500K bytes/sec data transfer

Intel's Hardware/Software Support

Support		Description
Intellec® Model 120	NEW	Development System New price/performance breakthrough; gives small program development capabilities including ICE™ support at lowest cost for 8-bit microcomputers; also acts as editing station for NDS-1
Intellec® Series II		Development System Versatile; provides support for Intel's entire 8- and 16-bit product lines, including high-level languages and ICE in-circuit emulators
Intellec® Series III	NEW	Development System High performance; two host processors to support Intel's entire 8- and 16-bit microprocessor family; resident 8088 Pascal, FORTRAN, PL/M, and assembler; compatible with hard disk
Intellec® NDS-1	NEW	Network Development System Provides distributed support for multiple 8- or 16-bit projects; offers shared file access, high-speed compilation, and low-cost debugging; coming mid '81
ICE™ Emulators		In-Circuit Emulators Detect design flaws; perform real-time hardware/software symbolic debugging, even in the most complex systems; versions available for all 8-bit processors
ASM™		Macroassemblers Available for every Intel 8-bit processor
PL/M Pascal		System Implementation Languages Available for system software development
Pascal FORTRAN COBOL BASIC	NEW	Application Languages All four languages for 8085AH application programming; Pascal and FORTRAN for the 8088; all available now
iRMX/88™ iRMX/80™	NEW	Real-Time Operating Systems User configurable, for 8088 and 8080A/8085AH; major facilities include: priority-based resource allocation; real-time clock; interrupt handling; task dispatching

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intel delivers solutions

Cleavage approach to GaAs growth promises low costs

Scientists at the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., have developed a technique that may greatly reduce the cost of gallium arsenide semiconductor material. **It might also make possible new sorts of integrated circuits with thin, single-crystal films on insulating substrates, or in multiple layers,** according to its developers. Called Cleft (cleavage of lateral epitaxial films for transfer), the approach uses—and reuses—a GaAs substrate that is bonded to glass. Single-crystal GaAs is grown on this substrate through vapor-phase epitaxy and then cleaved parallel to the plane of the substrate, creating a thin slab of high-quality crystal. The same substrate is used repeatedly to grow slabs 5 to 10 μm thick and comparable in their electrical characteristics with melt-grown GaAs. With Cleft, the usual GaAs substrate, typically 250 to 400 μm thick, is unnecessary, saving all but the few percent of the GaAs normally needed for a solar cell or IC and therefore drastically cutting cost. The Lincoln Lab team believes that Cleft can be applied to growth of other semiconductor materials as well.

Phased array aids cancer treatment

Antenna technology is overcoming a major disadvantage of rf hyperthermia, or tissue heating, in the treatment of cancer [*Electronics*, April 26, 1979, p. 88]. Developed by BSD Corp., Salt Lake City, Utah, **a doughnut-shaped phased array helps researchers and physicians reach tumors deep within the body.** Rf hyperthermia is attractive, as it requires neither surgery nor anesthesia and is therefore well tolerated by weaker patients; till now its use has been limited to the treatment of tumors at or near the skin because body tissue attenuates rf energy. With the annular phased array, a patient is placed within a ring of 16 waveguide antennas; the site of tissue heating is a function of phase reinforcement at the desired location. According to BSD spokesmen, the new technique heats tissue at the body's core.

Dynascan unit to make system for signature analysis

Indicative of the increasing acceptance of signature analysis as a field service technique is the growing number of instrument makers moving into the field. Dynascan Corp.'s B&K Precision Test Equipment Group, Chicago, has not yet introduced a product, but it has developed a prototype signature analyzer **with the potential to compete favorably in terms of cost and capability** with Hewlett-Packard's popular 5004A, brought out in 1977. Don't be surprised if B&K rolls out the unit—known internally as the SA1010—for showgoers' reaction at the Automatic Test Equipment Seminar-Exhibit in Pasadena, Calif., Jan. 19–22. Besides HP, the pioneer in the field, other firms with signature analysis products now on the market or in the works include Tektronix, Racal-Dana Instruments, Fluke, Millennium Systems, Phoenix Digital, and Kurz-Kasch [*Electronics*, Feb. 14, p. 102].

Commodore to show \$300 color computer

Trying to bridge the gap between the hobbyist and small-business computers, Commodore Business Machines Inc. will introduce a \$300 color graphics computer at next month's Consumer Electronics Show. Called the VIC 20, it contains a video interface chip that allows it to display material on an ordinary TV set through an external rf modulator. However, the display is limited to 23 lines of 22 characters each.

The VIC 20 uses Pet Basic. From the minimum configuration, which

has 5-K bytes of user memory, it is expandable to a total of 32-K bytes of random-access and read-only memory. An ASCII keyboard provides access to eight user-programmed functions through four keys. The computer has separate ports to address a tape cassette, an RS-232-C interface, and a serial interface for floppy drives, plus a game port for pointing devices and a memory-expansion port.

Memory-package decisions weighed

Some far-reaching memory-packaging decisions are being considered by the JC-42 committee of Jedec, the Joint Electron Device Engineering Council. In addition to casting ballots on leadless chip-carriers, the panel is listening to suggestions for housing 16-bit-wide devices in 28-pin dual in-line packages. A proposal by Mostek Corp. of Carrollton, Texas, to multiplex the data with a 20-bit address would allow for single- and double-byte transfers, with or without parity. Since such a scheme can accommodate 16 or more megabits of data, a standard could last to 1990 or beyond. So far, Intel Corp. of Santa Clara, Calif., agrees with the packaging idea in principle, but wants to add elements.

Lear Siegler's Falco starts own firm

Lee Falco, former president of terminal maker Lear Siegler Inc. of Anaheim, Calif., has formed his own company, Falco Data Products Inc. in Palo Alto, Calif. The new venture will introduce a terminal next month to compete with Lear Siegler's ADM 42 intelligent terminal. The TS-1 can hold eight pages of local memory (a \$125 option), and the basic terminal with detached keyboard will sell for an end-user price of \$1,195. The unit's switching power supply will power not only the terminal, but also future cards to be placed in its two extra card slots. Among those planned are a high-resolution graphics card and a complete single-board computer card to be introduced later in 1981.

Western finds another LSI use

Another large-scale integrated replacement for a bundle of TTL devices is coming from Western Digital Corp., which specializes in finding and filling this type of product niche. It is a 32-bit data-link controller for on-board avionic sensors that converts serial data into parallel form for processing, operating under the standard Arinc 429-1 protocol. The word length is programmable from one to eight characters. The Newport Beach, Calif., firm says avionics manufacturers already have samples.

Addenda

Wang Laboratories Inc. has introduced its Wangwriter, a word processor family, as well as the Wang Minidiskette Workstation and the Wang Remote Cluster Facility. The facility, which permits the company's office information system terminals to act as data processors when remotely linked to a Wang computer, is hailed by market planning and development vice president Frederick A. Wang as "the first result of our remote-networking development." . . . Data damaged because of head crashes or in catastrophes such as the recent Las Vegas, Nev., and White Plains, N. Y., hotel fires can be retrieved through a method devised by David Brown, a former manager of field engineering and support at Memorex Corp. The method combines manual scrubbing of the disk with examination and cleaning of the media using machines made by Randomex, a Signal Hill, Calif., disk-care services firm.

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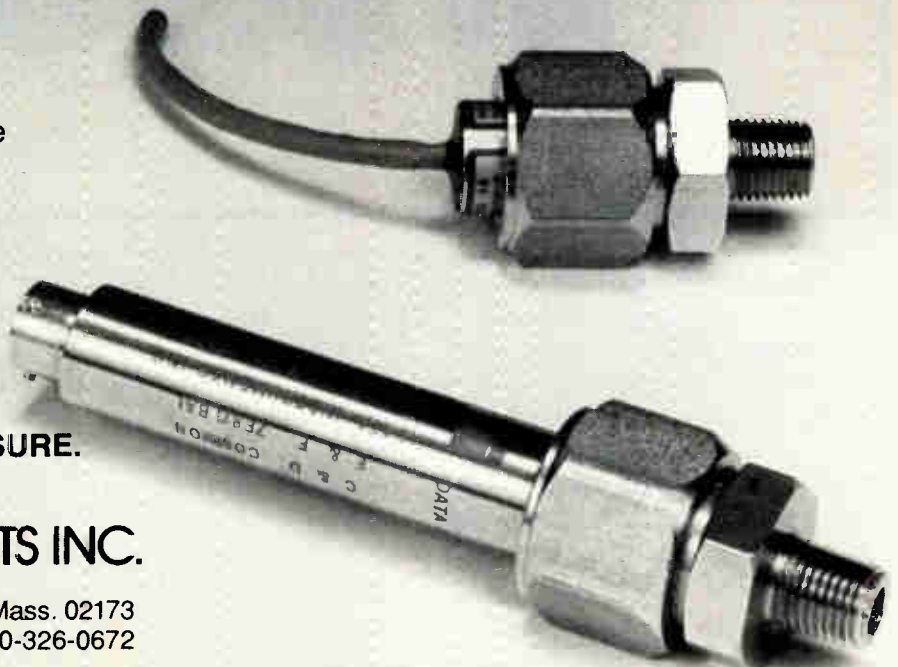
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Ada's modularity sparks interest for civilian uses

by R. Colin Johnson, *Microsystems & Software Editor*

Language developed for DOD is under consideration at all levels of computing; its universality is key

After some five years of deliberation, the verdict is in on the programming language Ada. It looks as if it might be the language of choice in the 1980s for all ranges of computing machinery, mainly because it allows efficient handling of programming applications by attaching packages that customize it.

Though the language was devel-

oped by CII-Honeywell Bull for the U. S. Department of Defense, Ada is likely to pop up in nonmilitary applications. A recent Minneapolis seminar held by Honeywell Inc., one of the principals of CII-HB, drew representatives from nearly 30 major companies that are gearing up to start programming in Ada.

To cite some of the work going on at these companies:

- A new software house is readying an Ada compiler for microprocessors, available initially for the 16-bit Pascal Microengine chip set from Western Digital Corp. This Ada subset, running in 128-K bytes of memory, comes from Telesoftware

Inc., founded by Kenneth L. Bowles [*Electronics*, July 3, p. 59], long associated with Pascal, one of the language bases for Ada. The San Diego, Calif., company plans to adapt its subset to other 16-bit microprocessors and eventually to extend its implementation to encompass the complete Ada language.

- The St. Paul, Minn., operation of Sperry Univac is constructing an interpreter for the language, called Bda, that will run on its Univac 1100 mainframe. If the work pans out, it will be able to write an Ada compiler in Ada and then convert into machine code with the Bda interpreter.

- Harris Corp. is investigating Ada

Ada's father speaks many languages

How did a Frenchman become project leader of the team that designed Ada for the U. S. Department of Defense? It all began when Jean D. Ichbiah (right) became enamored with computer languages while working on his doctorate in physics at the Massachusetts Institute of Technology—and he has been in the programming game ever since.

After earning his degree, Ichbiah went to work for the French computer maker, Compagnie Internationale pour l'Informatique, where one of his first projects was to write a compiler for the language Simula. His success gave him a free hand in writing a new language, called Lis, which incorporated many of Ada's design goals. He also became involved in the European Economic Community's project for a standard language for the Common Market.

Eventually his employer became part of the company now called CII-



Honeywell Bull, tied to the U. S. computer maker. Ichbiah's experience did no harm in the effort to land the DOD contract to develop specifications for a language that could handle any conceivable programming problem. "Ada incorporates the best features of the structured languages of the 1970s like Pascal, Algol 68, and Simula and will be the first programming language to support the idea of software components," Ichbiah says.

Following up on his design effort, he has just formed his own company, Alsys, to produce Ada compilers for two mainframes prominent in the EEC: Siemens' 7000 and Honeywell's Level 64 machines, with others to follow. Alsys will continue DOD work as subcontractors to CII-HB, which has a 15% share of the company. Ichbiah's firm also plans a campaign to bring programmers up to speed with Ada.

—R. C. J.

as a programming language for its line of scientific minicomputers. The Melbourne, Fla., company has been working on its own high-level language, called HPL, that has so many specifications identical to Ada's that it could make sense to move to the more universal language.

From the first, Ada was intended to be the universal programming language. The Department of Defense initiated the design project in hopes of consolidating its vastly differing programming applications into a single language. Recently the Army let the first DOD compiler contract to Softech Microsystems Inc., Waltham, Mass., for the VAX-780 minicomputer.

The resulting language allows customization of the types of data and even the basic operations of its constructs. For example, if scientific analysis is required, then a package can be attached that makes Ada Fortran-like.

Redefining. Such packages are much more than a group of subroutines, for they redefine the general-purpose language constructs to perform specific tasks. In effect, they are software components and the language is a general-purpose bus.

Such software components will greatly ease programming, maintains Jean D. Ichbiah, chief originator of Ada (see "Ada's father speaks many languages" p. 39) and principal speaker at the Minneapolis conference, which will be available on videotape.

Portable. They help solve the programmer crunch because they will be highly portable, and they will include reliability features to protect the algorithms from tampering by the user's programmers.

To achieve Ada's universality, the DOD and the design team headed by Ichbiah did extensive spadework on specifications for the language. The aim was to produce a highly standardized language, with general agreement on the specifications before software houses began writing compilers. In contrast, Pascal is bogged down in a morass of conflicting extensions because there was no general agreement on the precise speci-

fications for the language.

Such universality does exact a price: the full-blown Ada compiler will require about 256-K bytes of memory, whereas a typical Fortran compiler takes up 32-K bytes. However, Ichbiah points out, Ada will need only eight 256-K random-access memory chips, and these should be commercially available by the time the compilers are ready for the programming mainstream.

Solid state

N-MOS chips top GaAs in gate delays

In the race toward picosecond speeds, silicon can keep up with gallium arsenide, maintain Bell Laboratory researchers. Working with finely scaled-down geometries and advanced processing techniques, a Murray Hill, N. J., design team has achieved a 40-ps gate delay in a 19-stage ring-oscillator integrated circuit based on transistors with 0.3-micrometer channel lengths.

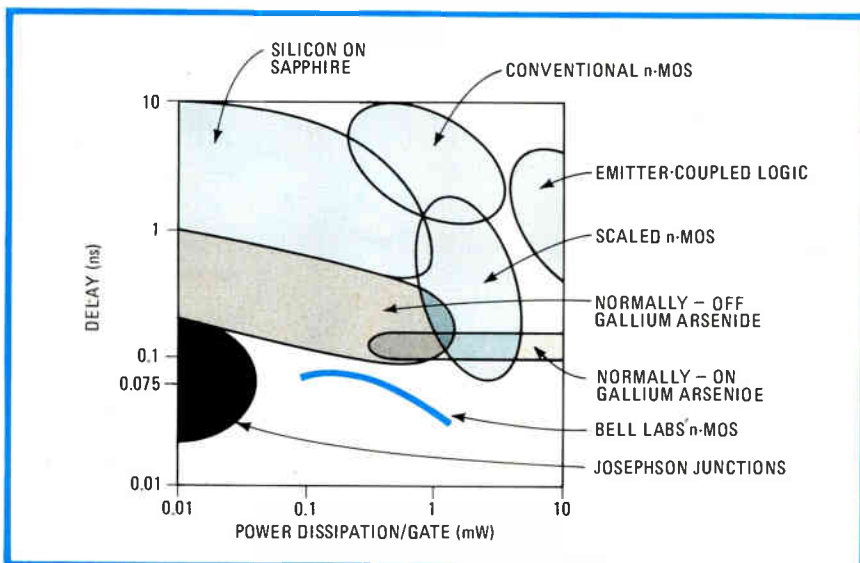
The design team's effort [*Electronics*, Dec. 4, p. 33] admittedly involves experimental circuits. However, these ICs were essentially produced by pushing standard technology, rather than by working with

exotic materials like GaAs or highly speculative structures like Josephson junctions.

"We've taken standard n-channel-gate silicon technology and made it better. There's no conceptual difference between what we've done and what is available today," says George E. Smith, head of the MOS device department at Bell Labs.

Still, the performance improves considerably upon that of today's processes and rivals that of the experimental GaAs and Josephson processes (see figure). GaAs is getting considerable attention [*Electronics*, July 31, p. 40]; for example, Nippon Telegraph and Telephone Public Corp. experimenters have achieved a 30-ps gate delay in a 15-stage ring oscillator based on transistors with 0.5- μm channel lengths.

Dimensions. The scaling in the Bell Labs oscillator and a companion 2.5-gigahertz divide-by-8 counter with 1- μm line widths results in oxides that measure 250 angstroms thick versus the 500-to-700- \AA oxides that are found in the typical MOS circuit. Smith also says that the junctions are shallower—0.25 μm vs 0.5 to 0.75 μm found in standard ICs—and that the doping is somewhat different. As in high-performance MOS processes, Bell uses arsenic for the source and drain dopants and polysilicon for the gate struc-



Leapfrogging. By paring line widths and watching doping levels carefully, Bell Labs' new n-channel MOS process hops over gallium arsenide in power-delay performance.

tures of the experimental chips
In its research, Bell Labs is interested in more than speed. "The real name of the game is power dissipation," Smith says. When geometries are reduced, electric fields intensify.

Working at 1.5 volts, the experimental parts sport a dissipation of 0.67 milliwatt per gate and a gate delay of 75 ps, giving a power-delay product of 5 femtojoules. With a 1.25-mW-per-gate dissipation and a 40-ps gate delay, the power-delay product is 50 fJ. A Lockheed team producing experimental GaAs ICs reports 0.5-mW gate dissipations.

To achieve the fine lines, the Bell team used X-ray lithography as well as reactive sputter etching. Smith notes that this etching method eliminates much of the undercutting of the film between the mask and the substrate material typically found in defining fine-line geometries.

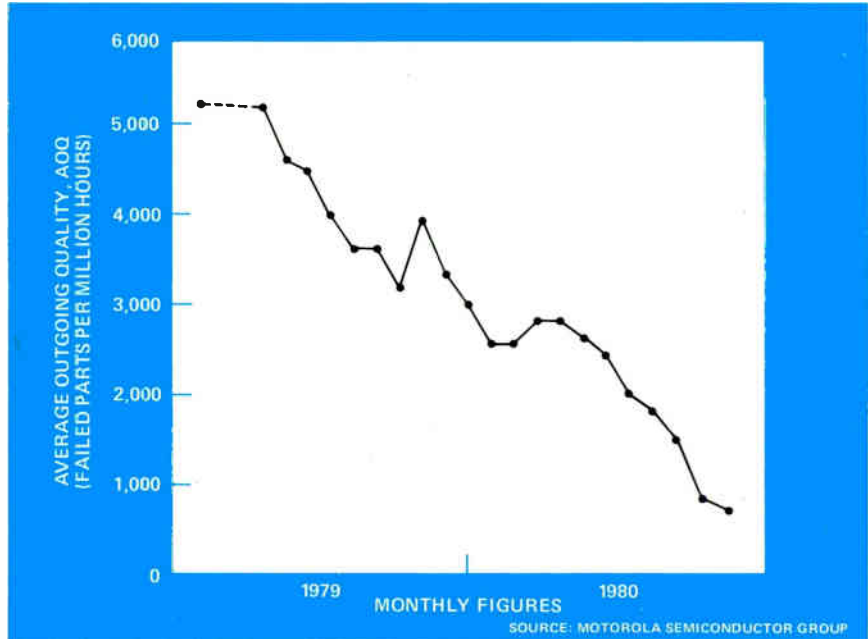
Team members also fine-tuned the X-ray machine to increase yields and to control line widths better, he says. In fact, this fine tuning was the principal method of paring line widths down from 1.5 μm .

Central to the design effort was a two-dimensional modeling of the fabrication process done with a Cray 1 computer. The designers were able to program substrate doping levels, the dose and energy of the implants, the times and temperatures of the diffusion furnaces, and the channel widths. They could vary a number of parameters in order to calculate the 2-d model. **-Pamela Hamilton**

Microsystems

U. S. makers raising processor quality

Spurred by competitive pressures and user demands, U. S. microprocessor makers are mounting campaigns to improve the quality of their parts. Three of the largest U. S. semiconductor manufacturers report that intensive upgrading programs, put into operation over the past year or so, are yielding big jumps in a key measurement of microprocessor



Quality up. By intensive attention to quality control methods, Motorola Semiconductor has seen better than a 600% improvement in AOQ figures for outgoing microprocessor quality.

quality, average outgoing quality.

At Motorola Inc.'s Semiconductor Group in Phoenix, for example, AOQ figures for some 50 bipolar and MOS microprocessor types slid from 5,200 defects per million projected operational hours in the first quarter of 1979 to 840 defects last month (see graph). These results also include Motorola's most complex device, the 16-bit 68000 processor.

National Semiconductor Corp., Santa Clara, Calif., reports that AOQ figures covering 73 processor types in the past six months dropped from the 1,000- to the 500-defect-per-million-hour level. Texas Instruments has AOQ figures for some 25 to 30 processor types of between 1,000 and 2,000 defects, according to a spokesman for the Dallas firm.

A major concern of U. S. manufacturers, of course, is the competition from Japan. For example, Toshiba Corp.'s Memory and Microcomputer Products division, Irvine, Calif., reports an AOQ figure of 250 failed parts per million hours for 12 processor types. It would appear that U. S. companies' quality levels in processors are closer to those of the Japanese than is the case in semiconductor memories.

Seasoned quality control hands do

caution against strict ranking of different firms' AOQ figures, because each company reaches them somewhat differently and each product mix is unique. However, the figures are regarded throughout the industry as the best single quality measurement. ("Our customers take them seriously enough," remarks one quality control official.)

Generally, AOQ is obtained by standard quality control statistical methods that sample each semiconductor product lot, test a fixed number of devices fully at high, low, and room temperatures, and then calculate the result in terms of failures per million projected operational hours. Defects in 1,000 parts may be expressed as a 0.1% failure rate.

Users. Comparative quality studies of microprocessors by users so far have not surfaced as have those concerning memories. Hewlett-Packard Co. for instance, which has performed attention-getting evaluations of memories [*Electronics*, Nov. 6, p. 46], has not initiated a similar effort with processors.

However, Richard W. Anderson, general manager of HP's Computer Systems division in Cupertino, Calif., expresses keen interest in the microprocessor AOQ figures. "I'm

pleased to see them," he says. "Nothing will have a bigger impact on the U. S. industry in the '80s."

The impetus spurring U. S. firms to step up quality efforts is not only the Japanese challenge, which many industry executives downplay. "It's really a combination of factors, led by our major customers demanding it," says Alfred J. Stein, vice president and assistant general manager of Motorola's Semiconductor Group.

Push. Such automotive customers as the Delco division of General Motors Corp. became big microprocessor buyers in 1978 and imposed far higher quality standards than semiconductor manufacturers had been meeting. Confirming this view is Thomas Griffiths, director of quality and reliability at National's Semiconductor division, who adds, "only a few years ago, 6,500 defects was an acceptable number."

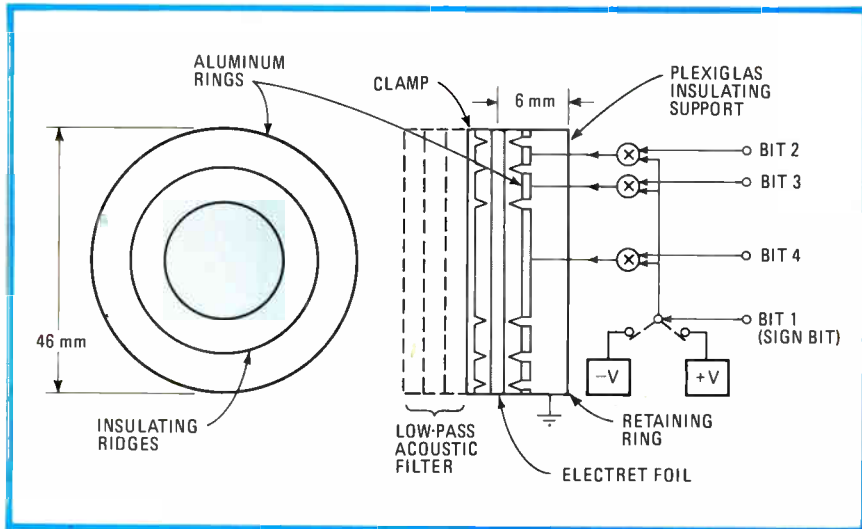
Stein puts quality inroads made by the Japanese in the memory area in second place as a motivator. "But it is an obvious kick in the pants. The Japanese have set a standard in memories," he says.

How the U. S. companies are getting the results is a contrast in styles, however. National goes about it with conventional quality control methods, though greatly intensified. Motorola and TI use these, too, but add management techniques similar to Japanese Quality Circles. As most U. S. firms report [*Electronics*, Dec. 4, p. 95], production workers respond enthusiastically when they are asked for suggestions and involvement in quality control through these Quality Circles. -Larry Waller

Communications

Phone translates digital signal

Digital telecommunications systems will always face the task of converting its signals into acoustic analog outputs as long as human ears are listening—but it need not take a mass of electronic circuitry and logic to accomplish it. Bell Laboratories is



Translator. Bell Labs has designed a transducer and low-pass filter for the phone earpiece, giving mechanical decoding of the digital signal and an acoustic output.

working on a simple transducer that plugs into the handset's earpiece and works with a filter to perform the conversion mechanically.

Digital words of 4, 5, or 6 bits can be handled by the active transducer design, which feeds the decoded signals to a passive mechanical filter for desampling. The careful working out of the complex mathematics of the design—by James L. Flanagan, head of the Acoustics Research Department at Bell Labs' Murray Hill, N. J., operation—makes the conversion method possible.

Advantages. This feat, still very much in the early developmental stages, could hasten the all-digital phone system by eliminating the need for expensive conversion circuitry at phone companies' local switching offices—and, of course, it will make the digital link that much longer. Flanagan's design also might be used in digital audio systems.

In operation, the telephone digital signal, representing a quantized sample of the original analog voice signal, must first be acoustically decoded into pulse-amplitude-modulation form and then desampled to recover the original. "Acoustic superposition of the radiated bit pulses produces the needed pulse-amplitude modulation for the acoustically decoded signal," Flanagan says. "The acoustic low-pass filter restores the full analog waveform."

To perform the acoustic superposition, he uses a condenser transducer that features a diaphragm displacement that is proportional to the electrical voltage across it. The digital signal enters in bit-parallel form—the design in the figure can handle 4-bit words.

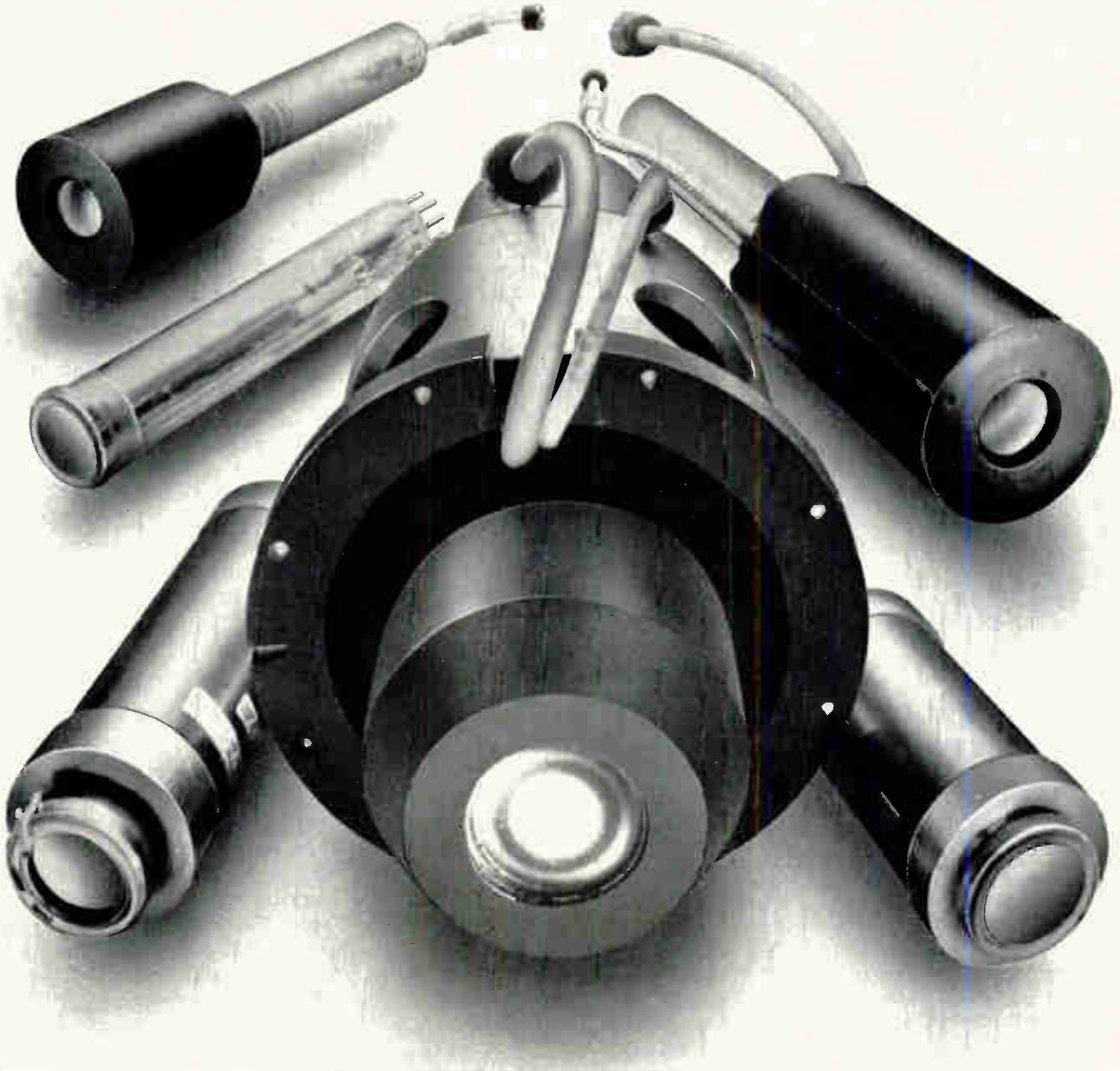
The first bit is a sign bit, activating the appropriate positive or negative voltage signal, depending on whether its pulse is a compression or rarefaction. Each successive bit feeds to an independent sound-radiating ring, which will produce a pulse of sound pressure if the bit is a 1. Flanagan determined how to scale the area of each of the rings so that the pulse's amplitude is directly proportional to the bit's significance.

For the experiments, an electret condenser transducer was the best choice, because of its economy and good performance. The filter that smooths the PAM waveform is a variant of the experimental plastic filter Flanagan's group devised for the microphone of the handset [*Electronics*, July 5, p. 46].

Other uses. "Even a 4-bit system retains useful fidelity and is attractive for voice-storage systems," Flanagan says. If such a system used microcircuitry, it could fit right into the handset along with the conversion transducer and filter.

Flanagan notes that the maximum 6-bit word that can be decoded by

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Electronics review

his present design falls short of good telephone quality, but he says 7- or 8-bit receivers are feasible and will be good enough. He also believes that the design's potentially wide dynamic range could help solve the old problem of achieving high fidelity from high sound levels if it were used in a digital loudspeaker.

Although measurements have been made on such parameters as linearity and frequency response, Flanagan says the work is only a first study. Further development at Bell Labs will include the study of other transducer materials and applications, as well as construction of an acoustic-to-digital transducer for the telephone mouthpiece—a much harder task.

-Harvey J. Hinden

Displays

**CRT system creates
 giant characters**

In the hurly-burly of futures trading, rapidly updated and easily accessible information on bidding is vital. So the newly opened New York Futures Exchange has installed a cathode-ray-tube system with a character-generation scheme displaying 1.5-inch-high alphanumeric symbols.

The system, from Conrac Corp.'s Systems-West division in Duarte, Calif., can display information visible from 65 feet away, whereas the typical electronic dot-matrix CRT display is blurry at 15 feet. Moreover, it can display characters up to

6 in. high. Thus it may extend CRT systems into a new field—large-character displays of public information, as in airline terminals.

Combination. Usually chosen for such displays are electromechanical systems employing characters or dots on flaps and dot-matrix systems based on common light bulbs—but both types take much longer to update. "The Conrac system provides us with a combination difficult to achieve in most CRT information displays on the market," says James S. Gallagher, vice president of market operations for the exchange.

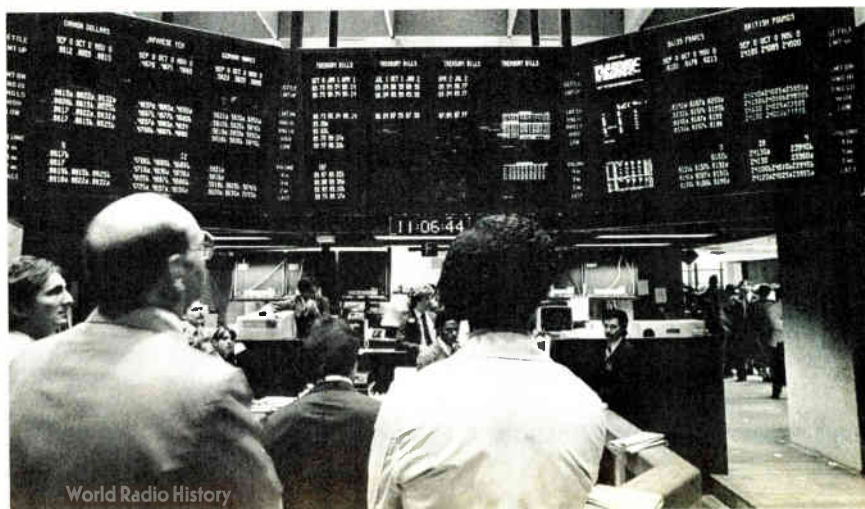
"That combination includes the high speed and reliability advantages of CRT technology and information display in a mass setting," he says. "Electromechanical display systems cannot satisfy our needs, and they require much maintenance."

The exchange has three displays of 30 CRTs each—for currency trading (see photograph), for bonds trading, and for commodities trading. A future display will be for Government housing-mortgage bonds.

During trading sessions, clerks write down each shouted bid to buy and sell on the appropriate magnetic card for the line to be updated and insert it into a reader, and the display changes immediately. In effect, they are updating a dot-matrix display system, but it is one in which the "dots" are much bigger than in the typical display.

To build up any alphanumeric character, the Systems-West display uses 128 basic shapes. Because each shape forms a much bigger area of

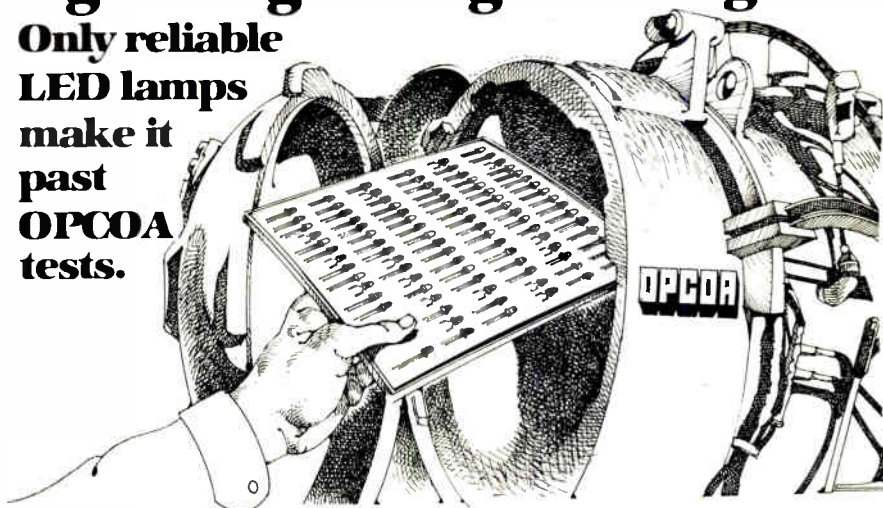
Big display. A matrix of 23-in. CRT displays from the Systems-West division of Conrac Corp. uses a new character-generation technique for large-character presentation of information.



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Business systems

Bell Canada unit looks to U. S. offices

Bell Canada plans to compete for a share of the U. S. market for integrated electronic office systems—at least by proxy. Northern Telecom Systems Corp. of Minneapolis, a supplier of distributed data-processing systems, is set to announce a complete word-processing package—and NTSC is a subsidiary of the Canadian equipment supplier Northern Telecom Ltd., in which Bell Canada owns a majority share.

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Electronics review

The package, including a letter-quality printer, runs on the firm's 400 series network distributed data-processing systems. That series grew from the lines of Sycor Inc. and Data 100 Corp., the pioneering companies in distributed processing that Northern Telecom bought and merged to form NTSC.

Adding words. The 400 series competes in the market for multi-processor-work-station shared-resource network systems. It is comparable in processing power to the Datapoint 1800 series and the lower end of both Datapoint's 6600 and IBM's 8100 series. By adding word-process-

ing capabilities to the extensive data-processing functions of the 400 family, NTSC is bidding to become a major contender in the emerging integrated electronic office market.

Omniword, the new word-processing package, includes an automatic filing system, a central document catalog, and a versatile document-merging function. It is driven by selecting operations from a menu and contains a tutorial to help the operator learn each function.

The new printer, called the Striker, is a letter-quality microprocessor-controlled Diablo daisy-wheel printer that can use both plastic and met-

Bar-code scanner reads in 3-d

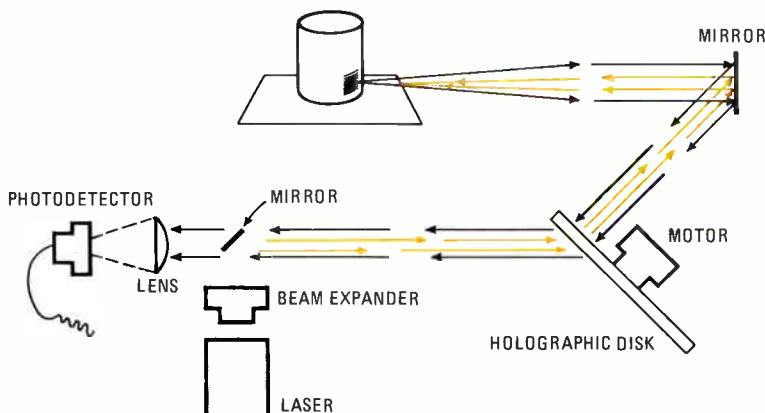
Bringing holographic technology into the world of commerce, International Business Machines Corp. is introducing a scanner that reads universal product codes on packages for point-of-sale terminals. Unlike the typical holographic application where a three-dimensional representation of an object is created, the 3687 scanner reads the bar code on a 3-d object.

A store clerk simply puts a package on the scanning window to activate the helium-neon reading laser. The bar code need not be passed across the window to be read; in fact, the system can read any bar code within the beam's 3-d range, which is a half sphere extending 4 to 5 inches up from the scanning window's surface.

The laser beam is deflected into a series of scan lines by the holographic disk, which also focuses these lines onto the package to be read. With the reflected beam, the disk collects the light to pass it to the photodetector, which is connected to the store's computer.

Made of dichromate gelatin material sandwiched between two glass plates 195 millimeters in diameter, the disk spins at 3,600 revolutions per minute. It acts as a prism to deflect the laser beam at an angle to give focal lengths to the scan lines. When the segmented beam hits the bar code on the package, the scanning of the bars creates light and dark variations that are sensed by the photodetector and interpreted by the computer.

IBM's Data Processing division in White Plains, N. Y., is pricing the 3687 at \$4,650 in a \$10,000 package that includes the complete point-of-sale system. The division's less versatile 3667 laser-based bar-code scanner costs about \$1,000 less, but it requires an adapter to hook it up to the POS terminal, which bumps the price well above the 3687's. —**Pamela Hamilton**



al print wheels. It will sell for \$4,290 and lease for \$145 a month; the Omniword software will be licensed for a one-time fee of \$750 or for \$30 per month, plus \$8 a month for software support for either option. Both products will be available in April, the company says. **-Tom Manuel**

HP mini boosts price-performance

In the face of a falling growth rate for its top-end series 3000 minicomputer line, Hewlett-Packard Co. is launching an upgrade that packs a big price-performance hike. What's more, HP also is introducing an on-line laser printer that gives users considerable flexibility in designing forms and other data formats.

The model 44 computer, which carried the code name Grizzly [*Electronics*, Nov. 6, p. 33], is said to have doubled the transaction-per-hour rate of the older series III. At a base system price of \$109,445, the new processor from the Computer Systems division in Cupertino, Calif., offers this improved performance at a price premium of only 5%.

The 2680A intelligent page printer [*Electronics*, Dec. 4, p. 33] can turn out 45 letter-sized pages a minute. Though other on-line printers may be faster—and costlier—the \$121,000 HP offering from the Boise (Idaho) division includes software that lets users design their forms on line, something comparable equipment does not permit.

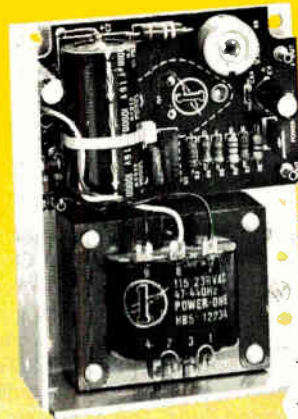
Slower growth. Like most mini-computer makers, HP is experiencing a major drop in its growth rate. Outside sources say that the company's growth rate in dollar volume in the 3000 line has been dropping steadily from 50% in fiscal 1979 over 1978 to no more than 10% to 15% in fiscal 1981's fourth quarter.

With the minicomputer industry maturing, 50% growth rates are probably a thing of the past, but other lines are still experiencing a growth about twice that of the latest HP figure. One reason for the dip at HP is probably the stiff price-per-

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News briefs

General Electric acquires Calma

In a move to bolster its revitalized semiconductor operations, General Electric Co. has acquired Calma Co. of Sunnyvale, Calif., a leading manufacturer of computer-aided design systems. Not only is GE expected to retain Calma's top management, but furthermore, the company plans to increase personnel at Calma from 1,000 to 8,000 employees in five years.

Last week's disclosure comes in the wake of GE's previous acquisitions of the semiconductor house Intersil Inc., Cupertino, Calif., and of a polysilicon-wafer fabrication facility, Great Western Silicon Corp. of Phoenix. Calma had been a division of United Telecom Inc. for only two years, but the parent company still made a tidy bundle on the deal. It acquired the firm for \$17 million and sold it to General Electric for \$100 million.

Zenith's computer chief plans venture capital effort

After heading Zenith Radio Corp.'s initial push into the minicomputer business, Edward J. Roberts has resigned his post with the Glenview, Ill., firm to head a venture capital firm that will specialize in backing high-technology companies. As managing partner for CR Investments, a fund backed by The Cavendish Investing Group, Toronto, Roberts says he hopes to provide management assistance as well as financial support for promising electronics-related firms. The emphasis will be on second- and third-round financing, with an eye toward aiding some firms to go public, he reports. "We're not looking for startup firms," he says. The 49-year-old executive [*Electronics*, March 13, p. 14] has served as general manager for Zenith's Computer Business Group and president of the firm's Zenith Data Systems subsidiary since its formation in late 1979. He declined to specify the amount of money CR Investments has available for investments.

formance competition from recently introduced machines from other companies, so the model 44 can be seen as a strong comeback bid in business systems.

Software. To enhance the attractiveness of the new machine, HP has paid as much attention to software as to hardware. The 16-bit central processing unit (implemented in standard and low-power Schottky TTL) and the 4-megabyte main memory (double that of the series III) contribute to the throughput boost—but so does the MPE-IV, the fourth generation of the company's operating systems.

"When the MPE-IV is made available for the HP 3000 series III, the performance advantage of the model 44 will revert to the 60% speed increase in the CPU," says a company spokesman. Also, the MPE-IV is designed for compatibility with HP's forthcoming 32-bit Vision family [*Electronics*, Oct. 23, p. 35], which is more than a year away.

The two software packages available with the 2680 laser printer are

called the interactive design system and the interactive formatting system. Resident in the host processor, they let the user sit at a terminal with graphics capabilities to design printout formats and handle such tasks as defining and modifying character sets, logos, and special symbols.

The user also can modify the form for a particular task. Thus a form letter with the company letterhead can be addressed to individual readers, or what amounts to a multipart form can be created.

-Martin Marshall and Bruce LeBoss

Government

FAA maps revamp of air-traffic control

Under the gun to revamp the overloaded U.S. air-traffic control system, the Federal Aviation Administration is proposing a massive modernization scheme that would last

into the 1990s. It is gambling that Congress will buy the ambitious project rather than push for a quick fix for the aging ATC setup.

Budgeted at \$2.8 billion for engineering and development, the project would entail sweeping revisions and additions to the hardware of the present nationwide network. The FAA envisions a winnowing that would begin with some five concept awards in July 1982 and culminate in a single three-year production contract in late 1988.

Congress. The proposal—called AERA, for automated en-route ATC—was disclosed earlier this month to a packed Washington, D. C., auditorium of potential bidders, some of whom immediately questioned the likelihood of congressional approval. The FAA's operation of the existing system drew sharp fire in a recent Senate investigation, and the proposal's 10-year span could be too long for Congress. The agency plans to improve the present setup in light of these criticisms.

A key feature of the renovation will be the replacement of the mainframes and radar displays, dating from the 1960s, that help control en-route air traffic. Proposed subsystems include:

- The National Airspace Data-Interchange Network, a digital net replacing a number of independent low-speed nets and switches.
- The Electronic Tabular Display System, which substitutes electronic displays for the flight-strip printers and paper flight-progress charts used for nonradar flight-control data.
- A new generation of weather radar based on doppler technology, plus an automated weather observation system. The FAA also wants a lower-cost weather system for general-aviation airports.

Also scheduled for inclusion in the new setup are several subsystems already under development. These include the Discrete Address Beacon System with radar interrogation of aircraft equipped to respond automatically, an automated cockpit-based collision-avoidance system, and a new microwave landing system.

-Ray Connolly

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SBC 732A 12-bit A/D, D/A (No 8-bit available)	\$1725.	CDP18S654 8-bit A/D, D/A	\$249.
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*Intel OEM price list July 14 1980

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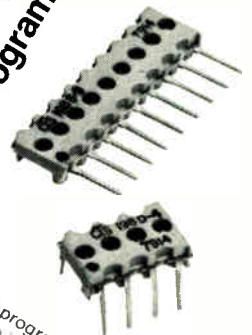
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Multiyear funding for weapons seen

Watch for strong support from the Reagan Administration and approval by the new 97th Congress of extensive use of three- to five-year weapons system production contracts, with up-front funding guarantees replacing the annual congressional funding battle. **The idea is to encourage investment by contractors** and stabilize what Pentagon and congressional leaders agree is a declining U. S. industrial base for defense. Long sought by the aerospace and military electronics industries, multiyear funding of major weapons and support systems—such as aircraft, ships, satellites, laser-guided ordnance, and digital telecommunications links—got strong support in December testimony before the House Armed Services Committee by military leaders and Under Secretary of Defense William Perry.

Post office approves five foreign OCRs

Five foreign manufacturers of optical-character readers will be asked by the U. S. Postal Service early next year to bid on the first 252 automated systems designed for implementation of the controversial nine-digit ZIP code. However, the successful bidder for the systems, estimated to cost nearly \$200 million, **will be required to make the automatic mail-sorting machines in the U. S.**, according to USPS officials. First deliveries are expected by the end of 1981. The five OCRs approved for the competition after Postal Service tests are made by Japan's Nippon Electric Co. and Toshiba Corp.; West Germany's AEG-Telefunken; Italy's Elettronica San-Giorgio; and Belgium's Bell Telephone Manufacturing Co., an ITT subsidiary. U. S. Postmaster General William Bolger says, "We have no choice in the matter" of selecting foreign-designed equipment, noting that no U. S. companies were interested in producing the systems in the short time before deliveries must begin. The total program, set to begin in 1984, is expected to cost \$887 million, with \$316 million for the first phase.

Drive to equalize semiconductor tariffs awaits Reagan

The Semiconductor Industry Association's drive to accelerate the equalization of U. S. and Japanese tariffs on semiconductors has stalled at least until next spring, according to R. Michael Gadbow, the SIA's Washington counsel. "Japan doesn't want to negotiate with a lame-duck administration," explains Gadbow, who has been pushing the association's efforts to equalize the two nation's semiconductor tariffs at 4.2% by April 1, rather than wait until 1987 as the U. S. and Japan agreed at the multilateral trade negotiations in Tokyo last year. Under the agreement, the SIA notes, the staged reductions will put American manufacturers at a relative trade disadvantage until 1987 **because the phased Japanese reduction began from a much higher base of 12%, compared with the 6% rate of the U. S.** The initial 1980 reduction, for example, has dropped Japan's tariff to 10.05%, still nearly twice that of the U. S. rate of 5.8%. Gadbow says he expects the Reagan Administration to be ready to address the issue in about April.

Army plans R&D on fiber optics to connect ICs

Can optical fibers be used to interconnect multiple integrated-circuit computing elements? That's what the Army wants to find out with a **new 14-month research and development program for which bids are due Jan. 15.** The project, being managed by the Ballistic Missile Defense Systems Command at Redstone Arsenal, Ala., calls for a laboratory demonstration of the feasibility of the concept.

The flap over 20 new satellites

In only seven months the Federal Communications Commission reviewed and approved the applications of eight U. S. companies—including five new market entries—to launch 20 new domestic communications satellites by the mid-1980s and build five other spares. But the timetable for those approvals amounts to a rush to judgment for the ordinarily slow-moving commission. The decision has distressed some of the applicants, as well as a number of America's allies in the Western Hemisphere with whom orbital slots must be shared. And, like some other recent FCC rulings, the domsat judgment may wind up in a U. S. Court of Appeals and perhaps become an international issue before the World Administrative Radio Conference, scheduled to meet in 1984.

Some domestic satellite companies are upset that their approved launch applications did not get exactly the orbit assignments they had sought, a potential earth-coverage problem for their new systems. Compounding that problem is the FCC disclosure at its early December meeting that it will now back up and take a look next spring at reducing the space separating satellites from 4° to 3°, leading to potential overcrowding. Even though the FCC has yet to receive a technical report on the impact of that reduction, its authorization of 20 new domsat launches requiring new orbital slots seems to guarantee adoption of the reduction.

Unhappy neighbors

On the international side, Canada is not pleased with the FCC's plans, since it wishes a 5° separation between satellites in that portion of the geostationary arc it shares with the U. S. But promoting the 3° separation policy here are the Commerce Department's National Telecommunications and Information Administration and the State Department. America's neighbors in Central and South America, contends the State Department, fear that the most desirable slots for them, between 55° and 75° west longitude, may be filled with U. S. domestic satellites before they are ready to launch systems of their own. To them, reduction is "arc conservation." The issue is "highly sensitive for the foreign affairs of the U. S.," notes NTIA chairman Henry Geller, who urges coordination of American policy by the FCC, the NTIA, and the State Department.

The satellite communications companies are not completely happy, either. Satellite Business Systems, which launched its first satellite last month, appeared most concerned when its pro-

posed orbits for two more satellites already completed were assigned to GTE Satellite Corp. SBS, which got launch approval for the second bird, with the third approval pending development of its market, is considered likely to appeal in court if it finds the alternative orbits granted by the FCC unacceptable.

GTE Satellite, which got approval to build three satellites and launch two, will use them to replace channels leased on three existing Comsat General Corp. satellites. American Telephone & Telegraph Co., which leased channels on the Comstar satellites, is also going its own way, with approval to build three and launch two satellites. Of the remaining domsat companies already operating, Western Union Corp. got approval to build and launch two replacements for its existing Westar systems, Comsat General was approved for launch of another satellite already completed, and RCA American Communications Inc. was approved to build six satellites and launch four to replace its Satcom I and II.

New entrants

The market entrants, in addition to GTE with its own systems, are Hughes Communications, which will build three satellites and launch two for an entertainment network; Southern Pacific Communications Corp., which will build three systems and launch two; and Space Communications Co., a new joint venture formed by Western Union and American Satellite Co. ASC, in turn, is owned jointly by Continental Telephone Co. and Fairchild Industries Inc. The new Spacecom will take over the Western Union space communications business, the FCC says. It will build and operate the Advanced Westar system for commercial markets and the Tracking and Data Relay Systems (TDRSS) for the National Aeronautics and Space Administration. Spacecom got approval for four satellites, whose total capacity will be split 2.5 for TDRSS and 1.5 for commercial services.

The fact that the FCC acted swiftly, if controversially, on a critical issue is more evidence that departing chairman Charles Ferris is determined to establish a record of breaking more new ground than any of his predecessors. The 20 new launch authorizations will represent an industry investment of more than \$2 billion and more than triple U. S. domsat capacity—provided that satellite separation can be successfully reduced by 1°, that Canada remains silent, and that none of the U. S. operators challenges the ruling in court.

-Ray Connolly

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32DX COMPULYTIC [®]	1.375 x 2.125 to 3.000 x 8.625	-40°C to +85°C	10 to 200	180 to 320,000	3441E
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- Reduction of testing preparation procedures
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Dec. 18, 1980

Electronics

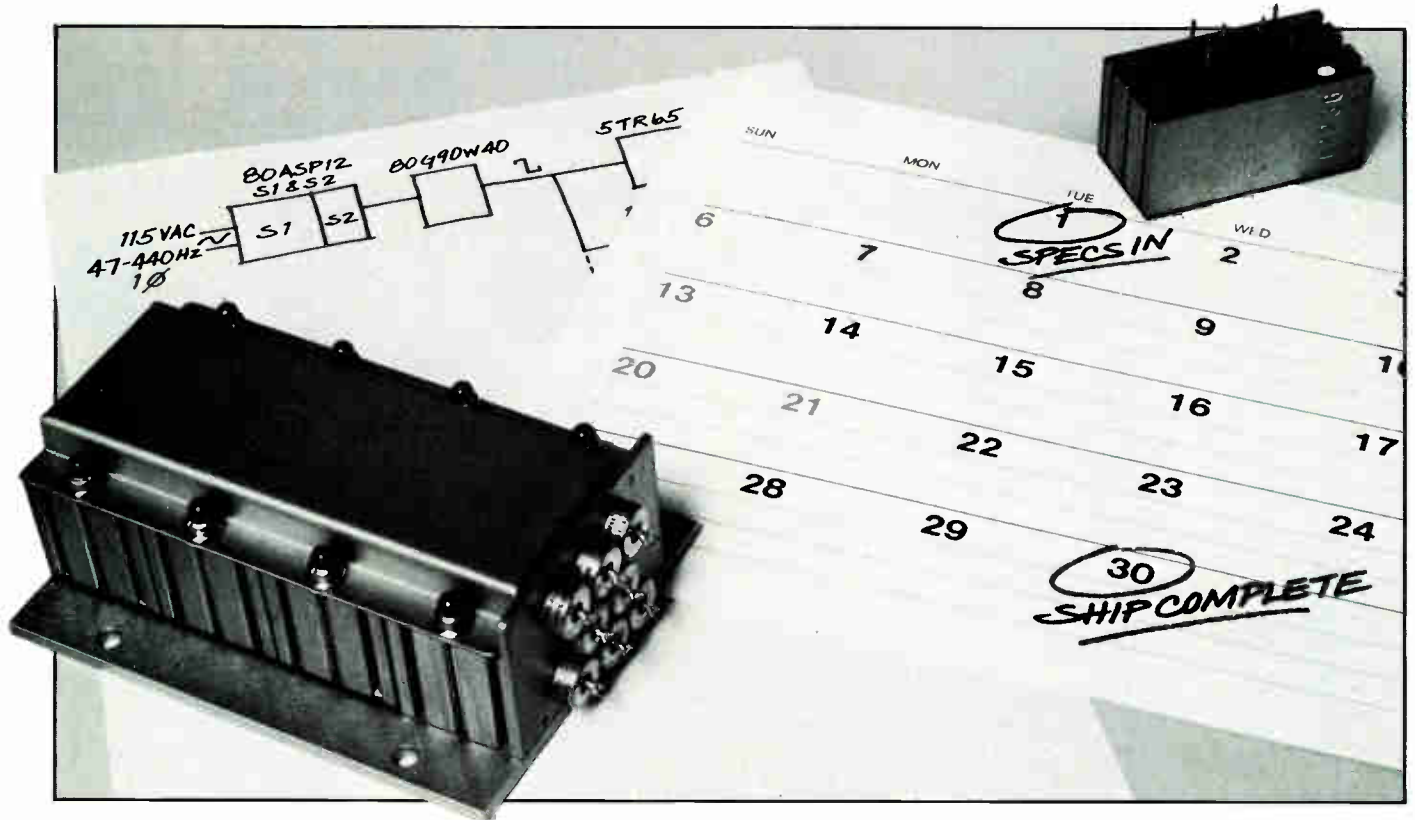
International®

8048-like devices adjust to special markets: page 61

Nippon Electric Co.'s MS70, the largest 32-bit minicomputer yet built in Japan, offers more than twice the performance of the 16-bit MS50 page 62



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X-ray unit checks wafer in 2 minutes for crystal defects

After more than five years of continuous development, an X-ray technique for nondestructively monitoring crystal defects in semiconductor materials is finally approaching production status. Developed at General Electric Co. Ltd.'s Hirst Research Centre, the equipment simultaneously exposes a semiconductor wafer over its entire surface to a divergent X-ray beam, instead of a scanned vertical-slit beam, and stresses it to alter the Bragg diffraction angle throughout the crystal. Since it takes only 2 to 3 minutes to perform an X-ray topographical analysis that till now has needed up to 2 hours, the equipment will make it possible to **introduce routine quality control of semiconductor wafers at high sampling rates at any stage in the production process.** Incorporating a 15-kw X-ray generator and X-ray camera, along with a specially designed bending frame, the system will cost around \$192,000 and be marketed by GEC's Neutron division, based at Marconi Avionics Ltd. of Boreham Wood, Herts.

Telefunken to aid China in making color TV sets . . .

Starting early next year, the Peking TV Industries Corp. and Telefunken GmbH, the entertainment electronics arm of West Germany's AEG-Telefunken, will jointly manufacture color TV sets in the People's Republic of China. That will make the Hanover-based company the first European maker of entertainment equipment to set up production in China, which is also **the biggest broadcast territory for the Telefunken-developed PAL color TV transmission system.**

According to the agreement, the West German company will ship components and TV subsystems to China and help the Peking personnel assemble sets, but in time the Chinese will make all the parts themselves. To be marketed under the Telefunken label by the Peking firm, the TV receivers will be sold initially only in China but eventually in other Far Eastern countries as well. The deal also provides for extending the production program to audio and eventually all other entertainment products.

. . . also acquires color TV interest in South America

Meanwhile, to strengthen its position in the expanding color TV market in Argentina, Telefunken GmbH has acquired a 25% share of Sigis SA, a Buenos Aires-based producer of entertainment equipment, including PAL color TV sets that use Telefunken parts. Since **the demand for 20- and 26-in. color sets is increasing rapidly in Argentina,** the West German firm has considerably stepped up its delivery of those parts to Sigis. The two firms will eventually extend their cooperation to include joint activities in the audio equipment field.

Laser-based device to print 10,000 lines of Japanese per minute

An agreement to develop a Japanese language laser printer that can spit out text, including Chinese characters, at speeds in excess of 10,000 lines per minute, has been signed by Fujitsu Ltd. and Toray Industries Ltd. A **prototype machine is to be completed next summer.** As Japan's leading computer manufacturer, Fujitsu brings to the deal its expertise in software and hardware and also in lasers. Toray, a leading chemical manufacturer that is diversifying into other areas, will contribute its knowledge of chemical processing, particularly in electrostatic copying and photography.

Both firms already manufacture Japanese language line printers—Toray a 3,600-line/min machine, and Fujitsu a 2,000-line/min unit. They will share the manufacture of the new laser-based model but will market it under their individual brand names.

Seven channels modulate laser In Japanese system

Cable TV trunk lines are among the applications Hitachi Cable Ltd. has in view for a possibly unique fiber-optic system in which the laser is modulated not by one channel but by seven—those of Japan's 90-to-222-MHz very high-frequency TV band. After demodulation, all seven stations are at their original frequencies and **can be tuned to by a standard TV set**. The laser output is 10 mw at 0.83 nm. Loss in the single-graded-index-fiber cable is only 3 dB/km, but dispersion and other effects limit its length to 2 km.

Low-cost British local net relies on personal computers

With individual schools as a prime target, personal computer manufacturer Acorn Computers Ltd. is introducing a local computer network, called **Econet, which at \$720 a station is claimed to be significantly cheaper** than other systems. Econet is a four-wire broadcast system that achieves a high level of noise immunity by differentially connecting wire pairs to provide clock and data lines. When two or more terminals seize the data bus simultaneously, a data clash is detected and a compact algorithm assigns a priority to one or other terminal.

Up to 256 Acorn computers—a 6502 with from 2- to 12-K bytes of random-access memory and 8- to 16-K bytes of read-only memory—can be T-coupled to the Econet ring. Alternatively, the net can be sectioned by gateways to increase system and in particular disk response time. **Its basic data-transfer rate of 210 kb/s is matched to the speeds of the floppy and minifloppy disks** attached to the computers. According to the Cambridge, England-based company, Econet could also find applications in process control and office automation, possibly forming part of a hierarchy of networks with gateways to high-speed rings like the 10-Mb/s Cambridge Ring or with concentrators to lower-speed devices.

Brazilian banks place large orders for Fujitsu computers

In its largest overseas computer sale ever, Fujitsu Ltd. has sold systems worth \$37.45 million all told to two Brazilian banks. The Banco do Brasil in Brasilia, the national bank, purchased two systems based on the firm's top-of-the-line Facom M-200 and four based on the smaller Facom M-160F for \$33.63 million. The Banco Auxilar in São Paulo purchased two systems based on the Facom M-160F. Between them the two banks' purchases include 40 disk drives, 92 tape drives, and 25 line printers.

According to a company spokesman, an important part in closing these deals was played by **the high reliability and excellent cost-performance ratio** of a Facom M-200 sold last summer to yet a third Brazilian bank.

Addenda

Siemens AG has won a contract from Australia's communications authority for the delivery of about \$58 million worth of its EMS private-branch exchanges by 1984. The Munich-based company has received **about 10,000 orders for small, medium-sized, and large EMS systems totaling roughly \$500 million** since it introduced the equipment at last year's Hanover Fair [*Electronics*, April 12, 1979, p. 63]. . . . The Canadian government's videotext, or two-way TV, system called **Telidon has been ratified as one of the world standards** by the United Nations' Plenary Assembly of the International Consultative Committee on Telephony and Telegraphy. . . . **Japan's Sord Computer Corp. will establish a \$6 million plant in Ireland**, at Santry, near Dublin, to manufacture its line of small professional and personal computers for the European market.

Resolve 10 bits with our latest complete DAC system.

Now you can choose from 5 μ P-compatible DACs with everything you need on-chip.

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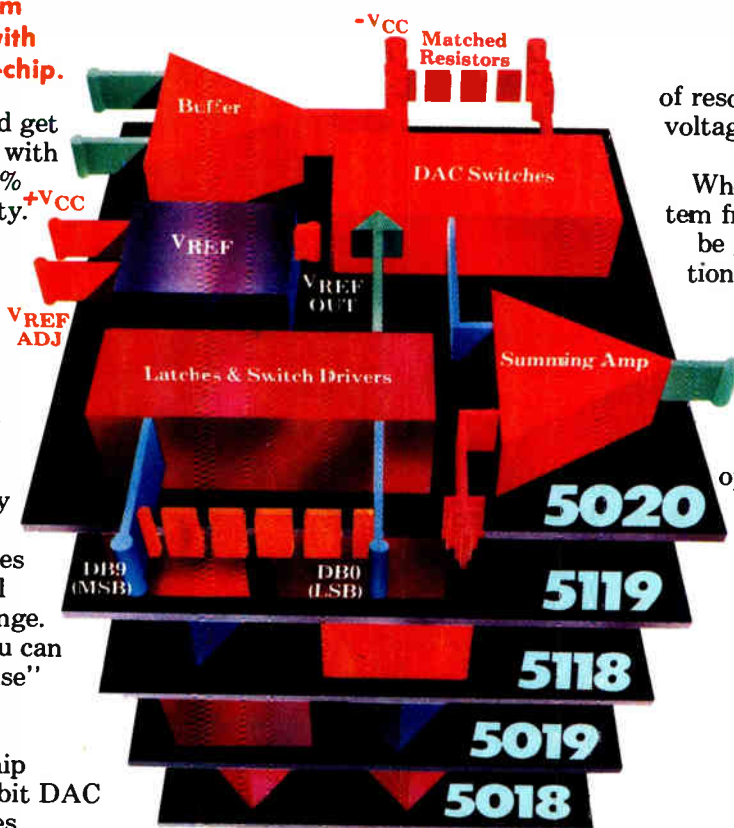
With powerful on-chip features, the 5020 saves you money over other 10-bit DACs. Because it cuts parts count and reduces design time.

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When you're down to the wire

8048-based chips zero in on specific consumer markets

by John Gosch, Frankfurt bureau manager

Entertainment electronics will be one beneficiary of two standard yet specialized microcomputers from Siemens

Semiconductor companies on both sides of the Atlantic are seeking to exploit specialized but potentially large-volume consumer markets with modified versions of standard microcomputers. Low-cost television and entertainment electronics is the area West Germany's Siemens AG has particularly in view for the SDA 2010 and 2110 it is now introducing. Both are based on the Intel/Siemens 8048 single-chip 8-bit microcomputer. Automotive applications, on the other hand, are the focus of such U. S. examples of the trend as Intel's 8061 version of its general-purpose 8051.

The benefits to the user are twofold. Being partially specialized, such devices both improve performance and reduce component counts and hence assembly cost. Yet being partially standard, they ease the designer's task by building on already existing software and microprocessor development hardware.

When the Siemens 2010, for instance, helps handle frequency-synthesis tuning in a TV set, it keeps the cost competitive with that of technically far inferior voltage-synthesis schemes. The parts count drops from 192 to 61, "and with that, the assembly cost of the set's tuning and control system is cut by more than half" points out Gerhard Weil, head of the integrated circuit systems development group at Si-

emens' Components division in Munich.

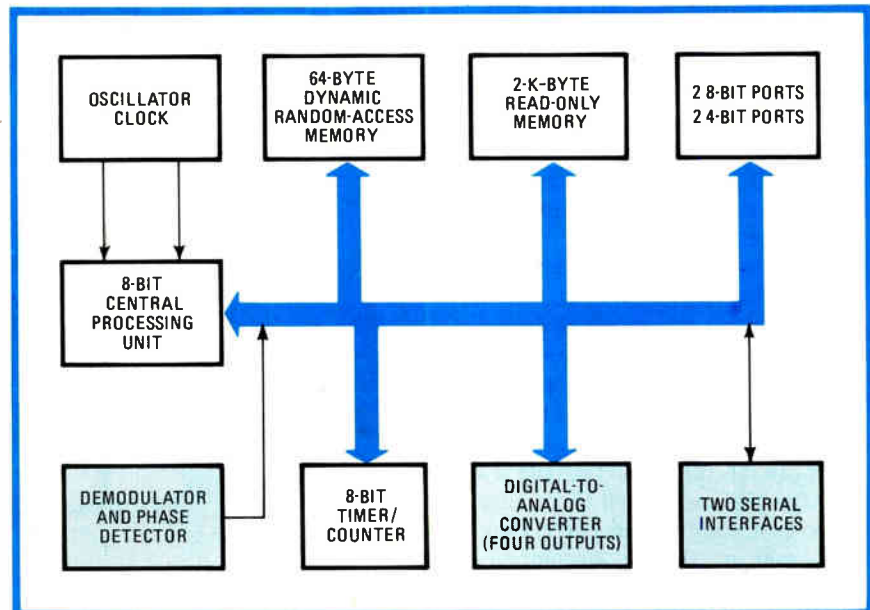
Further, because both the 2010 and the 2110 employ the 8048 8-bit central processing unit and a modified subset of the 8048 instruction set, the designer may use them with Intel's familiar MDS 800 and the equivalent Siemens SME microprocessor development systems, with Intel's ICE 48 and the equivalent Siemens Eta 48 in-circuit emulators, and with 8048 system software.

In hand. Mainly because of all these user benefits, Siemens has already received some handsome orders for the two parts, one from an unidentified cable TV maker in the U. S. for the 2110 and several from entertainment equipment producers in Europe for the 2010, according to Jürgen Lange, the division's product

marketing manager for entertainment ICs. Production of the devices is now getting under way.

As for its contents, the 2010 incorporates a 2-K-byte read-only memory for the program, a 64-byte dynamic random-access memory for data, and four 6-bit digital-to-analog converters (see figure). Further, in addition to an oscillator and a programmable counter-timer, the 2010 has 30 digital input/output lines. These comprise two 4-bit and two 8-bit ports, two test inputs and two serial interfaces, each interface being made up of one data and one clock line. The device comes in a 40-pin dual in-line plastic package.

Versatile. In the TV application, the 2010 not only helps tune the set but also reads out the channel number stored in a memory and activates



Changes. The functions the consumer-oriented SDA 2010 microcomputer adds to its 8048-based design are shown tinted. The program read-only memory is also doubled in size.

the channel number display driver. What's more, it processes the analog signals required to adjust the set's volume, brightness, contrast, and color saturation. And it can control videotext and viewdata text decoders, as well as video games.

Moreover, the 2010 can process the signals a TV set receives from infrared remote-control systems such as the Siemens SIR 60 [*Electronics*, May 26, 1977, p. 65 or 5E]. For transmitting commands, this 60-channel system uses a signal pulse-code-modulated onto a 31.25-kilohertz carrier. One input to the 2010 contains a demodulator for separating the PCM signal from the carrier. Another has a zero-crossing detector for determining the time at which a thyristor in the power supply must be fired. Both these inputs can also serve as normal digital inputs.

The device's instruction set comprises 65 1- or 2-byte instructions, each of which can be executed within two cycles. Numerical problems of the kind encountered in frequency-synthesis tuning can be handled with binary as well as binary-coded decimal arithmetic.

The 2110, a simplified version of the 2010, is intended for applications with fewer performance requirements, such as an automobile superheterodyne receiver. It has only a 1-k-byte program memory and a 40-byte static RAM data memory, contains only one 8-bit port, and has no d-a converters. As a result, it fits into a 28-pin plastic package. Both the 2010 and 2110 use 5-volt n-channel MOS technology with 4-micrometer gate lengths.

ROM-less. Also available are versions of the two parts that lack on-chip ROM and use external program memory instead. The SDA 3010 and 3110 come in piggyback packages that have a socket on top into which a type 2716 erasable programmable ROM can be plugged. For the user, the ROM-less parts spell three advantages: fast change and correction of the program during development, prototype testing under the same physical conditions as in the final equipment, and the cost savings they afford for short production runs.

Japan

Large superminicomputer can take on communications and industrial roles

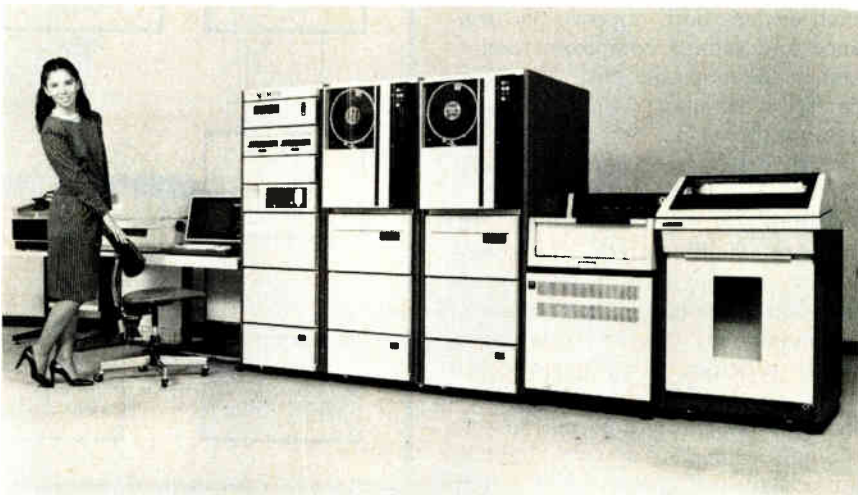
Japan's newest and largest superminicomputer takes as its primary target those companies that need more processing power to handle communications control. Nippon Electric Co. has accordingly designed its 32-bit MS70 to minimize its price in this application—its central processing unit provides just the fixed-decimal-point binary arithmetic such customers will require. But other applications can be accommodated by the MS70's optional double-precision floating-point and decimal plug-ins.

Announced late last month, the MS70 will sell in Japan for anywhere from about \$115,000 to four times that much. The minimum price buys a system with 512-k bytes of main memory, two 1-megabyte floppy disks, a console, an 80-megabyte disk, a 200-line-per-minute printer, and a card reader.

Completely compatible with the rest of the MS series, the new machine adds 43 32-bit instructions to the 124 basic and 62 optional 16-bit instructions of the earlier computers. It uses the same packaging as the present 16-bit MS50—

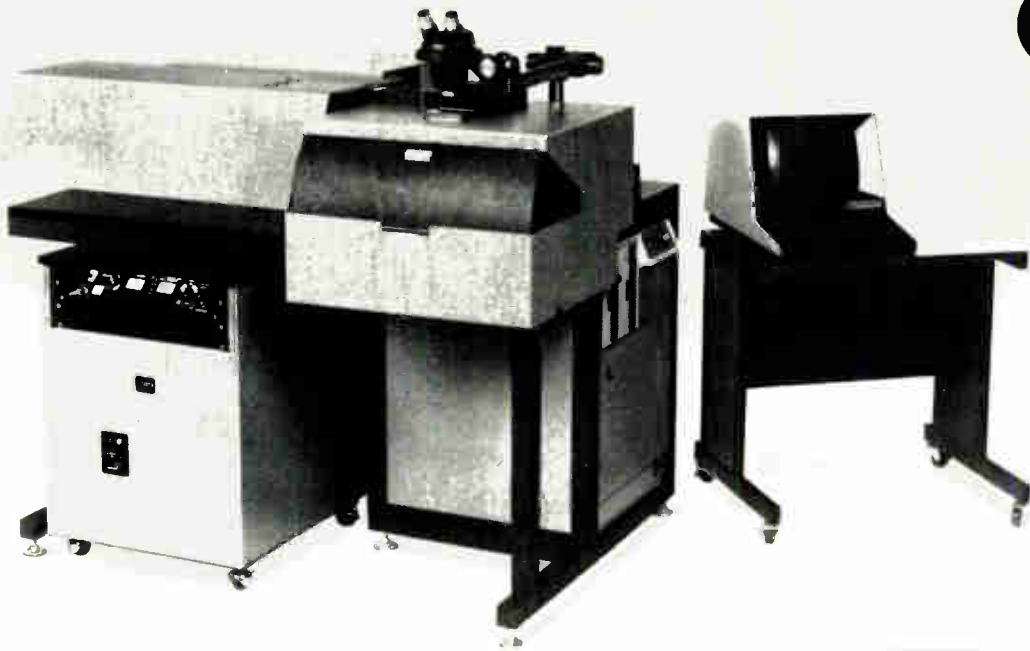
which has somewhat less than half its performance. The CPU in the MS70 is built around nine 2903 4-bit bit-slice chips from Advanced Micro Devices that provide the required word length and parity. Similar chips are also used in the optional (double-word-length) floating-point processor and the optional decimal processor (intended for customers who wish to develop programs in Cobol). The device controllers require the higher speed of TTL but are relatively simple. A larger machine would require custom or master-slice chips in its processors.

Throughput. In terms of throughput, the MS70 does about 20% better than Digital Equipment Corp.'s 32-bit VAX-11/780 superminicomputer, according to NEC. Partly this is due to the saving in overhead because the MS70 does not use virtual memory, not being intended to serve as an alternative to mainframes or small-business computers, both of which NEC also makes. But if a step-up model is made, its large size will require virtual memory, says Yoshiyuki Nagano, an engineering department manager in the



In control. Two of these 32-bit MS70 minicomputers from Nippon Electric Co. can replace five 16-bit MS50 machines, thus cutting energy costs as well as saving floor space.

CLS 33



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3 Intelligent software. The system microcomputer of the CLS-33 is backed up by the most intelligent software operating system in the laser trim industry. Its structure frees the operator to concentrate on trimming the



product, instead of on time-consuming computer programming procedures. Programming effort is further minimized thru on-line compiling and editing and thru program de-bugging in user language. This remarkable software operating system is another CLS exclusive.

4 Maintenance ease. The CLS-33 was built to require a minimum of maintenance, but at the same time was designed to be highly maintainable. Faults can be rapidly isolated to the module level with the systematic diagnostic programs. Disassembly of the entire system, for full access to modules,

requires just minutes. Efficient circuit design has reduced the total number of modules to be considered in fault finding — another time saver.

5 Free training. With every system sold, Chicago Laser provides complete training of operator and maintenance personnel at no extra cost and with no limits on time or number of operators. In addition, the easy-to-understand documentation supplied with the CLS-33 is so comprehensive that it is virtually a training course in itself.

6 Adaptability. From computer program inputs to system operation, the CLS-33 is adaptable to most any production demand. For high-volume applications, an available air-bearing step-and-repeat handler allows the CLS-33 to trim an incredible 100,000 resistors per hour. A stack-load station is also available.

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computer engineering division.

The MS70 has the physical space for 4 megabytes of 64-K memory chips but direct address space for 16 megabytes, so that main memory can be enlarged when 256-K chips hit the market. For speed, two-way interleaving of memory is provided, with an access time of 435 nanoseconds for every 4 bytes. Adding further to its speed is pipeline control and 32-K bytes of cache memory.

Uses. According to Minicomputer Systems division general manager Shigehiro Hirasawa, NEC should sell 1,000 systems over three years, 60% of them for communications applications, 30% for industrial applications, and 10% for scientific and engineering computation.

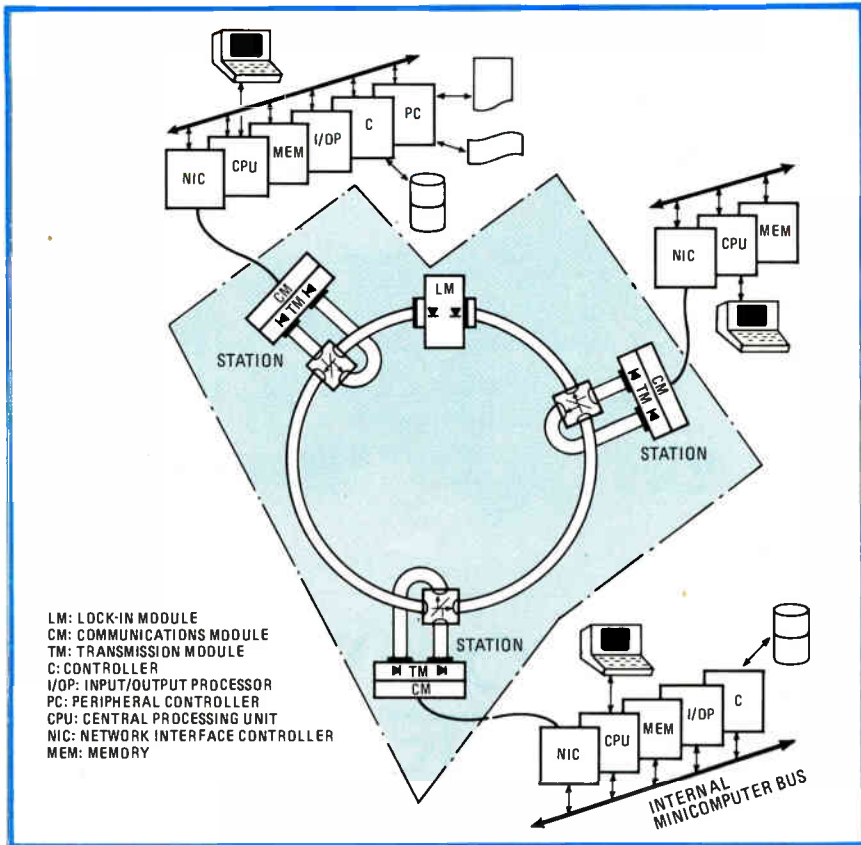
In the communications applications the new computer both competes with and complements IBM equipment. It is competitive even though there is no dedicated distributed-processing version of it directly comparable to IBM's 8100 series. It is complementary because it can be used as a gateway for protocol conversion in networks operating under IBM's Systems Network Architecture or NEC's Distributed Information Network Architecture.

Before deliveries start, the firm is contemplating adding C language support to the more traditional Fortran, Cobol, and Basic, which should facilitate application programming. Cross software is also available to develop MS70 programs on NEC's ACOS mainframes. **-Charles Cohen**

France

Fast fiber bus points to fast local nets

A laboratory version of one of the world's fastest data buses is to be unveiled in March by researchers from two French subsidiaries of the Netherlands' NV Philips Gloeilampenfabrieken. In fact, the 140-megabit-per-second optical bus should be fast enough to serve as a model for not only distributed processing networks, but also the real-time distri-



Video speed. A 140-Mb/s optical bus (tinted) will link three minicomputers in a laboratory network configured as a loop. T-coupler losses in this configuration are 2.5 to 3 dB.

bution of minicomputer operating systems.

The joint research team from the Laboratoires d'Electronique et de Physique Appliquée (LEP) and the Centre Technique Industriel of Philips Data Systems SA, located respectively in the Paris suburbs of Limeil-Brévannes and Fontenay-aux-Roses, began working on the project five years ago with an eye on networks capable of video transmission. Their laboratory model, when operating at a 0.85-micrometer wavelength, has fiber losses of only 5 decibels per kilometer and connector losses of between 1.5 and 2.5 dB.

Temperature-sensitive. Built almost entirely with optical fibers and components developed by various labs within the Philips group, the system also uses Fairchild 10000 emitter-coupled-logic gate arrays. But ECL tends to heat up and affect laser performance adversely, so fan cooling is used to keep system temperature between 20° and 28°C.

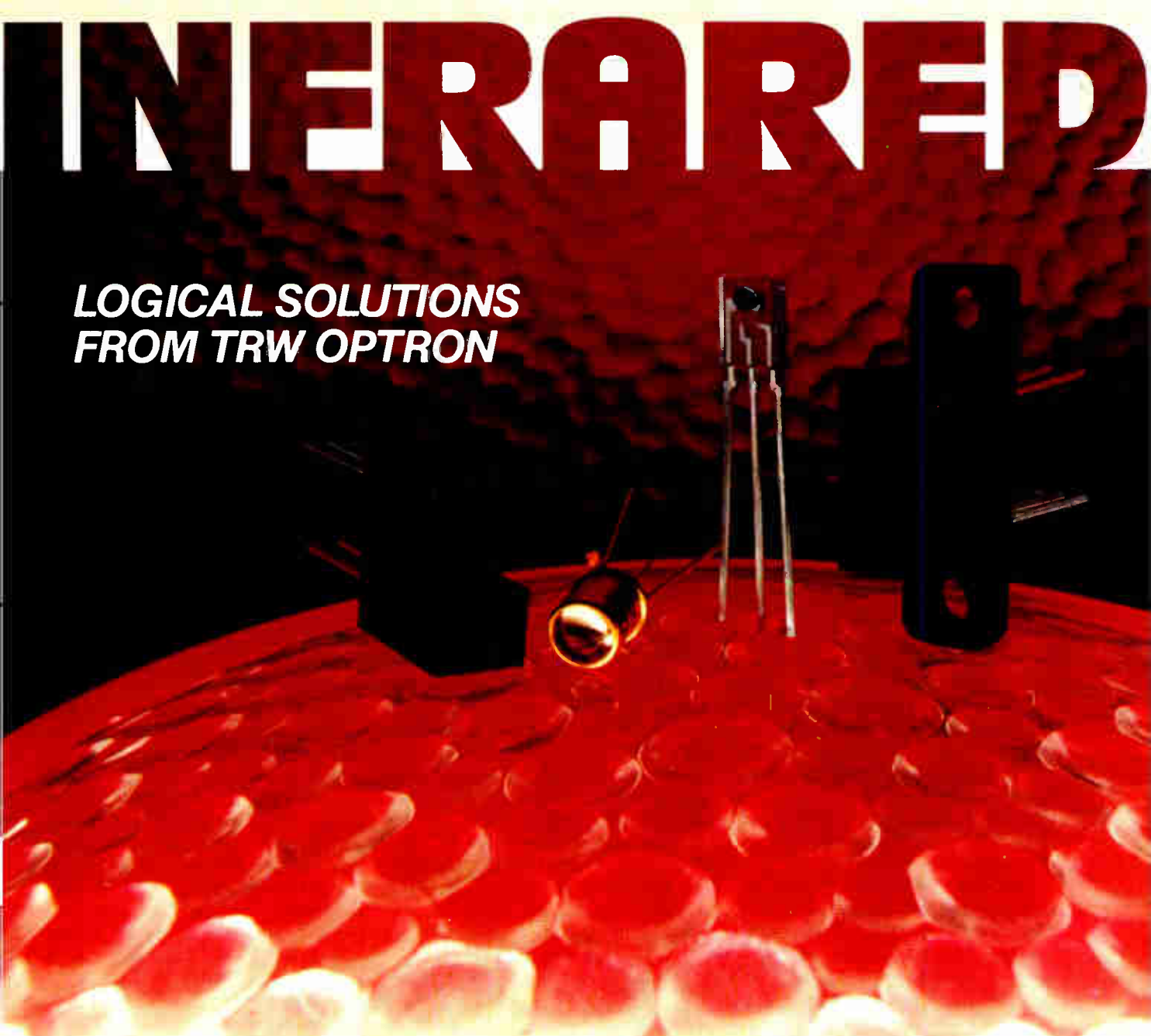
Although slower optic buses are easier to set up, since they can use diode rather than laser light sources and TTL rather than ECL circuits, LEP deputy director Gérard Marie notes that a high-speed bus is necessary for wideband video signals. The 140-Mb/s rate was chosen because it is the European high-speed telecommunications norm.

A network dubbed the Medium-Scale Distributed System (MSDS) is being built using the bus together with Philips' own P800 series of 16-bit minicomputers, though it could be adapted to use on almost any other minicomputers. The first operating laboratory model of MSDS will demonstrate a loop bus, though a star bus is also under development.

The loop configuration can accept up to 8 or 10 nodes, with a data rate of 340,000 16-bit words per second and per station. It is expected to prove operable up to a maximum length of a few kilometers. Set up as a star, the system can handle up to

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TRW OPTRON

16 nodes at the same rate, or 63 nodes transmitting 85,000 16-bit words per second and per station.

In either configuration, the basic elements are the same. The transmission principle is synchronous time-division multiplexing of 24-bit words, with each word consisting of 16 bits of data, 1 parity bit, 1 procedure bit, and 6 bits of code containing addresses and instructions for the system modules. Each station can write one 24-bit word every 2.9 microseconds into its own time slot. Communication between any two nodes is organized into 16-word packets to allow synchronization at the data link level. The relatively short packet length permits higher-priority communications to cut into lower-priority messages.

As explained by Gilles Aaron and François Phulpin, the LEP engineers who have been with the project since its outset, the organization of both the functional and physical aspects of the system generally corresponds to the principal layers of the seven-layer architectural model for open systems interconnection being promoted by the International Standards Organization.

Modules. At the base of the bus structure are the transmission modules, one for each node, responsible for bit and word synchronization, coding, and conversion of data into optic form and also partially responsible for initialization of the bus system. Data link layer and end-to-end transport control functions are handled by the communications modules—again, one per node.

The link protocols are entirely handled by the ECL circuits in the communications module. But for high-level end-to-end transport control protocols, the module's micro-programmed block level sequence works together with the system's microprocessor-controlled network interface controller. Built around an Intel 8086, this controller has direct memory access to the minicomputer and also contains a buffer memory through which all transfers between the minicomputer's central processing unit and the rest of the network pass.

-Kenneth Dreyfack

Great Britain

Fiber-optic data links could use GaAs ICs

High-speed gallium arsenide transistors are proving hard to integrate because the level-shifting circuits needed to connect them either occupy too much of the chip and soak up too much power or call for onerous processing techniques. But for some telecommunications applications, at any rate, a solution has been found at the Martlesham Research Centre that British Telecom, part of the British Post Office, runs near Ipswich, Suffolk.

Instead of using active level-shifting circuits, researchers there employ a passive approach, ac-coupling GaAs depletion-mode field-effect-transistor stages with a reverse-biased Schottky-diode capacitor. According to Alec W. Livingstone, who heads the development, the technique shifts voltage levels without needing an extra power line, requires little chip area (unlike Hewlett-Packard's buffered-FET logic), is not complex to fabricate (unlike Rockwell International's level-shifting Schottky-diode approach), and tolerates the wide process variations characteristic of GaAs fabrication. This last point is important, he says, "because it makes it easier to dual-source a circuit from a single design."

Minimum. Their ac coupling limits these high-speed circuits to a minimum operating frequency of a few kilohertz. That is an obstacle to their use in computers, where unchanging logic levels of some duration can be expected. But it is not a problem in the many telecommunications applications where, as Livingstone notes, "data streams are deliberately scrambled to ensure that there are no continuous logic levels more than a few data bits long."

In particular, the group plans to use capacitively coupled GaAs logic circuits in a 1.2-gigabit-per-second pulse-code-modulated optical-fiber

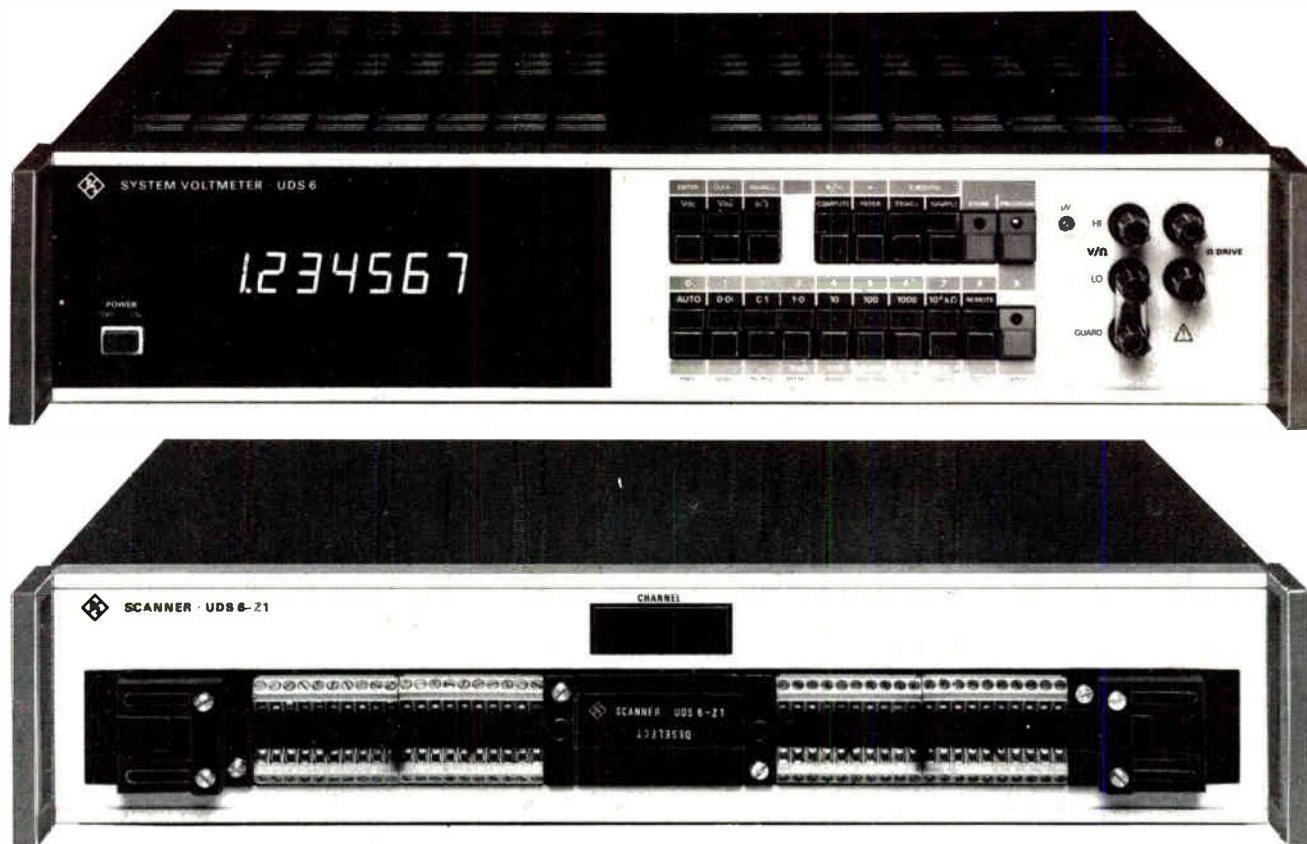
link combining eight 140-megabit/s data streams. Since British Telecom has yet to move from the 140-Mb/s systems now in operation to the 280-Mb/s systems in advanced development, that plan is long-term, but, says Livingstone, "we need to develop the technology now."

In fact the group has already produced its first ion-implanted test circuits, including an inverter, exclusive-OR gate, and ring oscillator, and is using data culled from them to design 50- to 80-gate circuits for operation at up to 1.2 Gb/s. In the 1.2-Gb/s PCM system, three circuits—the multiplexer, demultiplexer, and signal regenerator—must operate at the full data rate. The first two circuits are very similar, and some of the multiplexer parts already exist on test chips. The third component, the signal regenerator, consists of a photodetector, amplifier, and laser and ultimately could be integrated, probably on a gallium aluminum arsenide substrate.

Low power, too. Simple capacitively coupled logic of this kind will be capable of extremely high speeds, but British Telecom has another requirement. It wants clocked GaAs circuits with very low power consumption and therefore is willing for them to operate at speeds of 200 megahertz at most—still high by silicon standards. For this the group is proposing a form of four-phase logic and has carried out circuit simulations that suggest a power consumption in the region of 100 microwatts per gate at 200 MHz.

In a four-phase logic system employing dynamic MOS circuitry, the nodal capacitance to the silicon substrate can be used to store data in the form of charge. The nodal capacitance is far less on a GaAs substrate, which is semi-insulating. To meet the needs of their capacitively coupled level shifter, the British Telecom researchers therefore deliberately introduce a substrate capacitance. Logic levels are then established by capacitor charge sharing rather than transistor aspect ratios, so that all transistors can be of the same minimum size, further lowering power consumption. -Kevin Smith

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Measure: UDS 6 is a high-performance 6-1/2-digit voltmeter for demanding applications in research, development and calibration.

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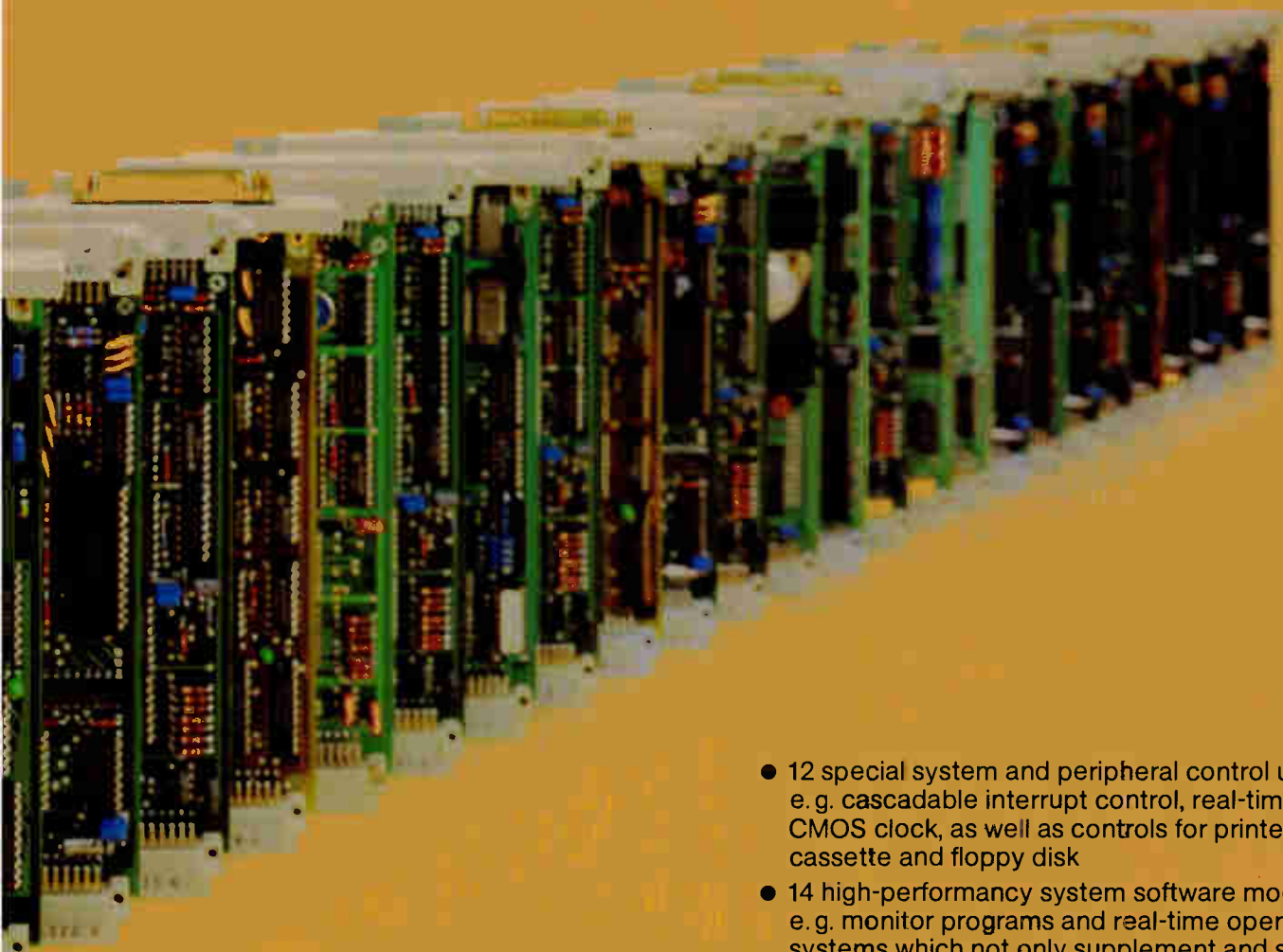
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World Radio History

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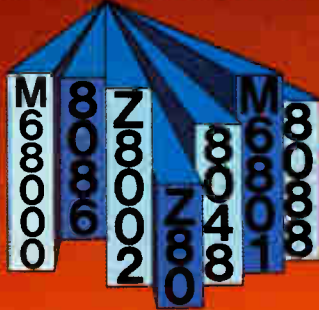
- 12 special system and peripheral control units, e.g. cascadable interrupt control, real-time CMOS clock, as well as controls for printer, cassette and floppy disk
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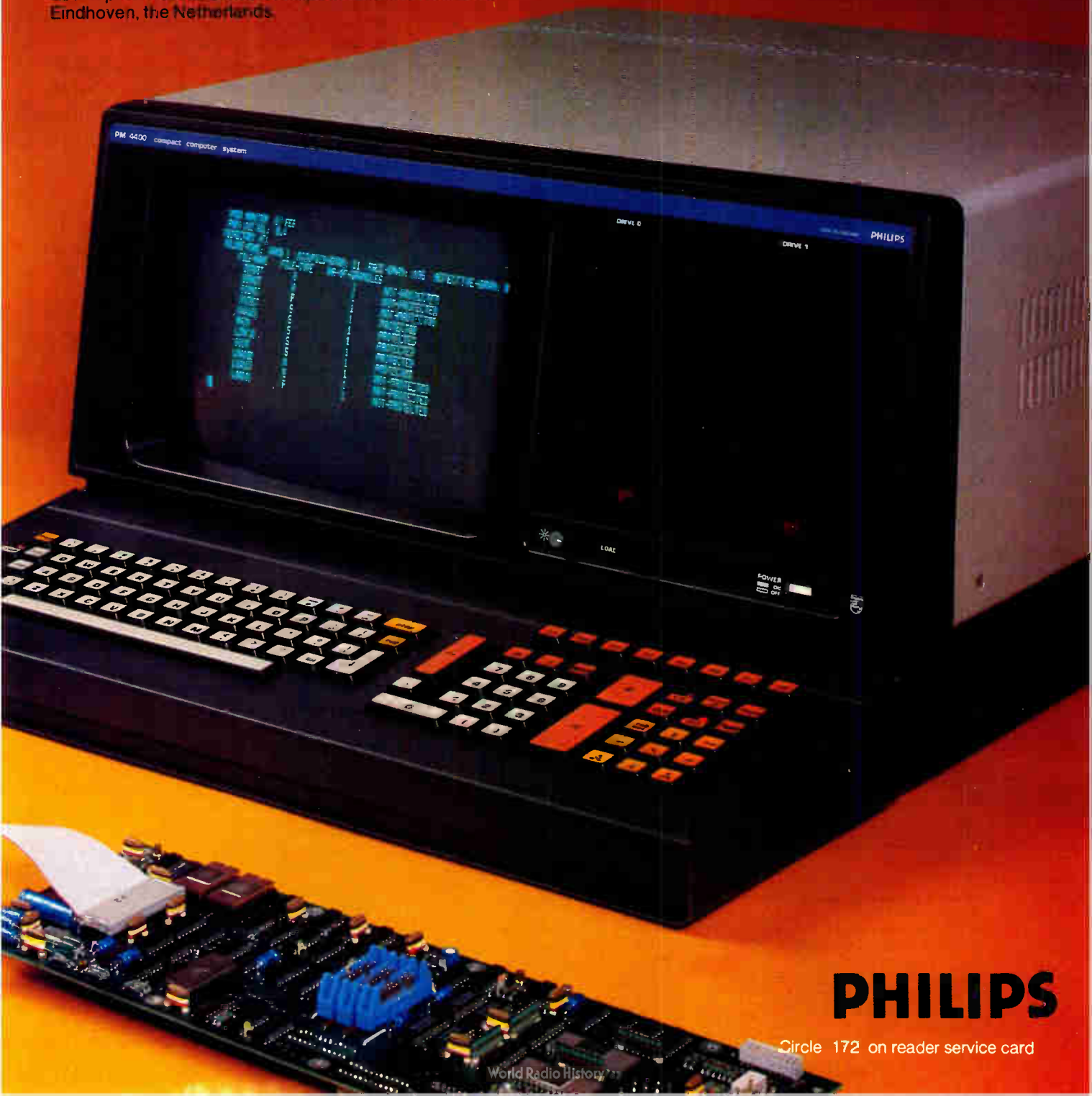
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Custom membrane keyboards suit consumer market

by Kenneth Dreyfack, Paris bureau

Guaranteed for 1 million operations per key at 125°C, Mylar keyboards use silver-, carbon-based conductive ink

To satisfy the growing hunger for keyboards for consumer goods, the instruments and components division of ITT in France suggests a triple-decker Mylar sandwich. The membrane keyboards from ITT Composants et Instruments, in the Paris suburb of Bagneux, are designed for such applications as television remote control units, appliance controls, and electronic games and toys.

"Our membrane keyboards become competitive with electromechanical keyboards when at least 20 keys are required and when the quantity runs to at least 10,000 pieces per year," says Yves Béraud, product manager for ITT's Commutateurs Jeanrenaud division. Jeanrenaud is handling assembly and marketing of the new keyboards, with an ITT printed-circuit division, Société France Cadran, doing the actual circuitry.

The keyboards consist of three sheets of Mylar sandwiched together. Two of the sheets are silk-screened with key contacts and interconnections using a low-temperature thick-film inking technique. The third sheet is a template from 150 to 190 μm thick. Holes cut in it separate the key contacts, making some 120 g of pressure necessary for contact between the upper and lower layers. A polycarbonate film, with adhesive on both sides, holds the lay-

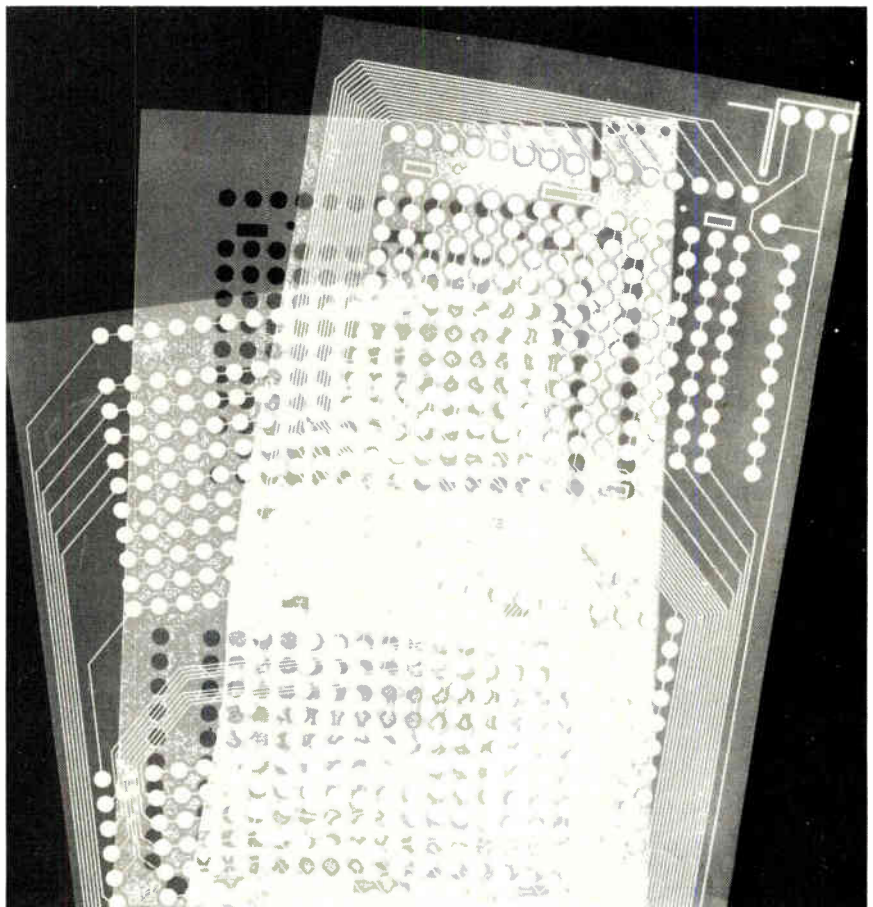
ers together and seals them.

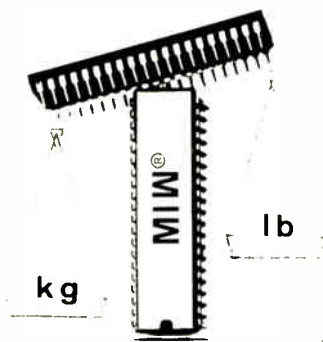
For keyboards requiring snap action, another Mylar sheet with bubbles over each key is added to the sandwich. The minimum pressure to make a key contact rises to about 300 g.

Choice of inks. With a conductive ink containing about 75% silver, the keyboard circuitry draws just a few milliamperes at 5 v, with less than 100 Ω of resistance in a typical circuit. A carbon conductive ink is much less expensive, but resistance is

more likely to be in the 10,000- Ω range. As Béraud points out, "10,000 Ω is not necessarily too high—some MOS circuits can still work with that." In either version, ITT guarantees at least 1 million operations per key, at temperatures of up to 125°C.

Béraud stresses that each customer can pretty much design his own keyboard because, at least so far, ITT is offering no standard versions. The principal limitation is physical size. The company now offers 400-by-





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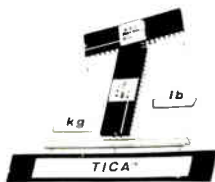
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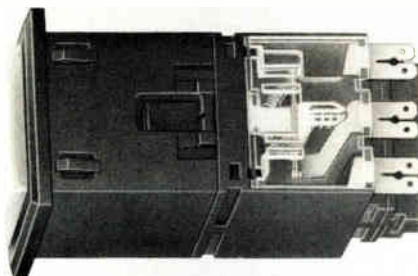


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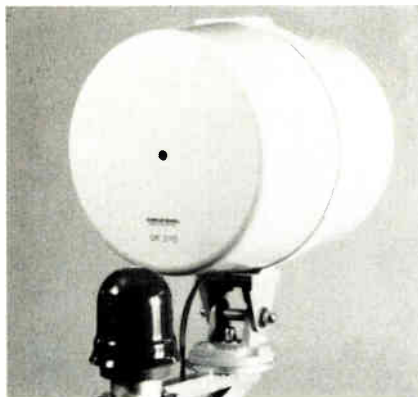
400-mm silk-screened Mylar sheets, but it can provide 400-by-600-mm keyboards for special cases and expects to be able to print 600-by-600-mm sheets within a few months. The contacts must be 10 mm apart.

The custom nature of the keyboards makes it difficult to cite specific prices, but Béraud says a typical typewriter-sized keyboard using silver conductive ink should go for about \$9, ordered in quantities of 100,000. The company already has about a dozen customers for its new keyboards, which are available throughout Europe.

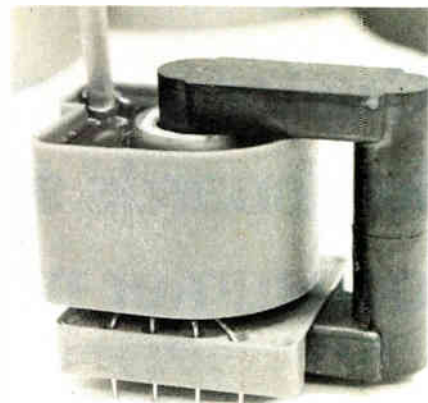
ITT Composants et Instruments, 157 rue des Blains, 92220 Bagneux, France [441]



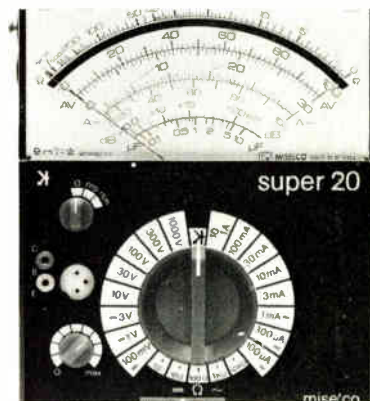
These illuminated push buttons have self-cleaning snap-action contacts in hard silver with a maximum switching power of 10 A at 250 V ac. They are available in single-pole, double-throw or double-pole, double-throw versions. Rafi GmbH & Co., 7980 Ravensburg, P. O. Box 2060, West Germany [442]



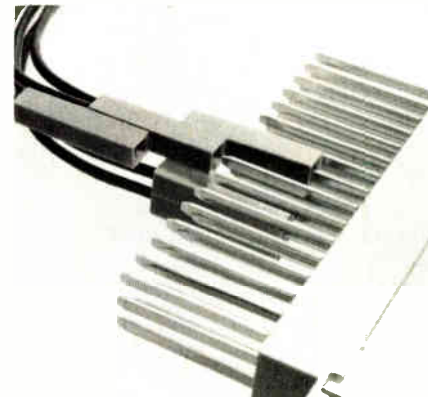
Microwave link equipment SR300 protects objects at power plants and industrial sites. The transmitter sends microwaves from its parabolic antenna to a receiving unit 250 m away. Any change in the received energy due to motion will sound an alarm. Grundig AG, 8510 Fürth, West Germany [443]



The AZ 3700 series of television-set line transformers with foil-wound ferrite cores is designed for use with various picture tubes. Their construction makes them smaller and lighter than equivalent wirewound line transformers. Siemens AG, 8000 Munich 1, P. O. Box 103, West Germany [444]



The Super 20 and 50 pocket-sized multimeters test basic semiconductor device functions. Each instrument has 39 ranges, including from 100 mV (150 mV for the S/50) to 1 kV dc and 10 V to 1 kV ac, full scale. Alcon Instruments Ltd., 19 Mulberry Walk, London SW3 6DZ, England [445]



The series DSA1 plug-in connectors are designed to be used on 0.8-by-1.6-, 0.8-by-2.4-, and 1-by-1-mm posts. They provide piggyback connections to wrapped-wire pins. Klippon Electricals Ltd., Terminal Works, Power Station Road, Sheerness, Kent ME12 3AB, England [446]

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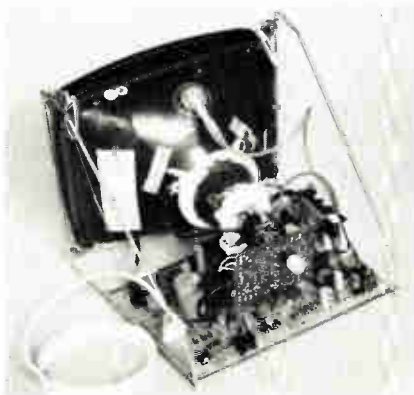


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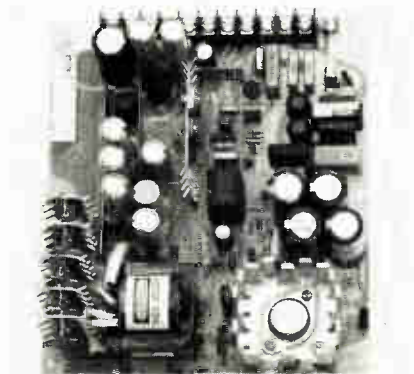
New products international



The A1000/A5100 automatic continuity tester has a keyboard for the writing and editing of test patterns. It provides test results in the user's language and incorporates a variable-threshold facility. Gould Instruments Division, Roebuck Road, Hainault, Essex IG6 3UE, England [447]



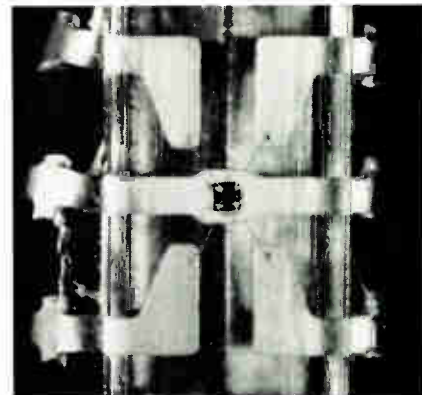
The Low Complexity Colour Display has a direct digital interface for video data and self-converging electron guns for red, blue, and green. Its cathode-ray tube resolves 492 by 585 picture elements. Microvitec Ltd., P. O. Box 188, Bolling Road, Bradford BD4 7TU, England [448]



Contained on a single 188-by-157-mm printed-circuit card, these open-frame switching power supplies offer an output of 90 W. They are designed to be convection-cooled and to operate from 0° to 50°C. Astec Europe Ltd., 4A Sheet St., Windsor, Berks. SL4 1BG, England [449]



The SL 6787 rotary joint, designed to be stacked in multichannel applications, contains on each half a strip-line multiple-feed system coupled to a central coaxial cavity. It has a frequency range of 1,010 to 1,110 MHz. Silvers Lab, Box 420 18, S-126 12 Stockholm 42, Sweden [450]



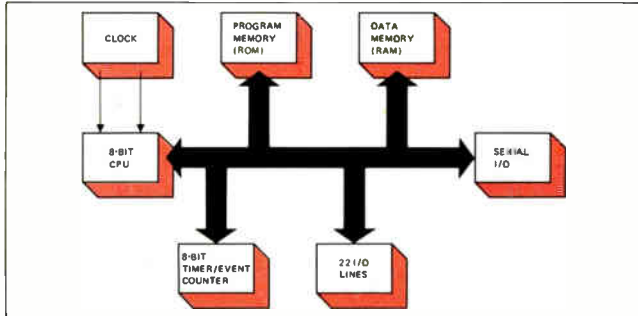
SFH 204 photodiode, sealed in a transparent case, is divided into four quadrants 12 μm apart, with individual contacts. The component can detect small deviations in impinging light of 0.35 A/W at 950 nm. Siemens AG, 8000 Munich 1, P. O. Box 103, West Germany [451]



The TM353 portable digital multimeter can measure voltages from 100 μV to 1,000 V (750 V ac), currents from 100 nA to 2 A, and resistance from 1 Ω to 20 MΩ. It has a maximum error of 0.25%. Sinclair Electronics Ltd., London Road, St. Ives, Huntingdon, Cambs. PE17 4HJ, England [452]

NEWS FROM PHILIPS

8400 FAMILY MICROCOMPUTERS



Dedication combined with flexibility is the design philosophy behind our new NMOS family of single-chip 8-bit microcomputers. Dedication comes in the size of program memory and the I/O; flexibility comes with programmability. Designated the 8400 family, the new devices which number five in all are planned to be available in the course of next year.

Principal feature of the new family is that serial I/O is implemented on the chip. This serial I/O has a multi-transmitter capability which facilitates communication between the micro-

computer and peripheral circuits or other microcomputers. This makes it possible to functionally split up the control of a system with all the advantages of fewer connections and lower costs in production and service.

The first of the new family will be designated 8400. This device will be a "piggyback" version without ROM, but with 128 bytes of RAM. A 4K or 8K EPROM can be plugged into a socket on the top of the 8400. It has been designed specially for prototyping, testing and low volume production and, apart from the program memory, has the same archi-

tectural features, pin-out and I/O lines as the other members of the family. Closely following the introduction of the 8400 will be four more types which will have mask-programmable ROM: the 8405 with 0,5 Kbytes ROM and 32 bytes RAM; the 8410 with 1 Kbytes ROM and 64 bytes RAM; the 8420 with 2 Kbytes ROM and 64 bytes RAM; and the 8440 with 4 Kbytes ROM and 128 bytes RAM.

The new devices have an 8-bit CPU, ROM, RAM, a timer/event counter, and 22 I/O lines in a single 28-pin package. Over 80 one and two byte instructions make up the instruction set which is about 90% identical to that of an 8048. The instruction cycle time is 6,77 μ s when a readily available 4,43 MHz crystal is used.

Full support for the 8400 family can be obtained using Philips Microcomputer Development System (PMDS). This can handle every operation from preliminary design through to final debugging and integration of hardware and software, with techniques including real-time in-circuit emulation, tracing and state analysis. A low cost design aid is also available.

CIRCLE 135 ON READER SERVICE CARD

MORE GENERAL PURPOSE RECTIFIERS

Two new families of rectifier diodes, designated PH40 and PH70, have been added to our range of general purpose power devices. They have average forward current ratings of 40 A and 70 A maximum, respectively. Both families have versions with peak repetitive reverse voltage ratings of 200 V, 600 V and 1000 V. Double diffusion coupled with proven assembly methods ensures reliable performance. They are supplied in a DO-5 encapsulation, which is specially suitable for power rectifiers of this class in industrial applications. Normal and reverse polarities are available for all versions.

CIRCLE 136 ON READER SERVICE CARD

HIGH VOLTAGE ELECTROLYTIC CAPACITORS

To meet the growing demand for electrolytics for use in high voltage circuits of televisions, monitors and other equipment, we have developed three complementary series, 041/042/043, and series 052 which is an extension of our popular 050 series. The 041-series are IEC 384-4 general purpose types with a capacitance range from 1 μ F (385 V) to 22 μ F (160 V). The 042 and 043 are IEC 384-4 long-life types, ranging from 10 μ F (385 V) to 100 μ F (160 V). These devices are available with standard axial leads, or with one extra-long lead for single-ended mounting. In addition, 041 types are available with PCB pins for single-ended mounting and 042 and 043 types can be supplied with a mounting ring and PCB pins for use in high vibration applications.

The 052-series are IEC 384-4 long-life types that range from 47 μ F (385 V) to 1000 μ F (250 V). These are available with either solder tags or pin terminations.

CIRCLE 139 ON READER SERVICE CARD

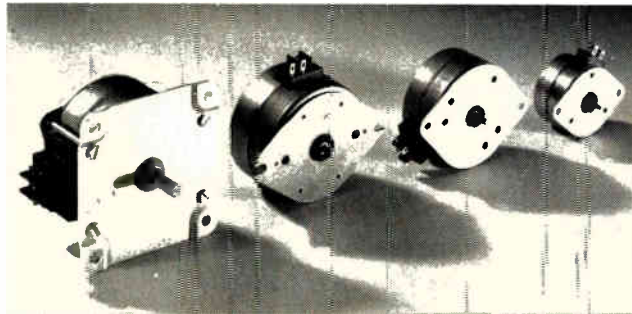
VERY FAST RECTIFIERS

Our range of fast recovery rectifier diodes has been further extended.

Two new series of Super Fast Soft-Recovery Rectifier Diodes are the BYV30 series in DO-4 and the BYV92 series in DO-5, with average forward currents of 12 A and 35 A respectively. Their features include a low forward voltage drop of less than 1,05 V at rated current, a high reverse voltage capability up to 400 V, very fast recovery times of less than 100 ns, and non snap-off characteristics. Reverse and normal polarity types are available.

Further new types include Very Fast Soft-Recovery Rectifier Diodes 1N3899/1N3903 and the 1N3909/1N3913 with average forward currents of 20 A and 30 A, respectively. Designed for use in high frequency power supplies and inverters, they have a high reverse voltage capability up to 400 V, a fast recovery time of less than 200 ns, and non snap-off characteristics. These types have DO-5 metal envelopes and are available in reverse and normal polarity versions.

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ECONOMY MOTORS

Our wide range of motors has been further extended by the introduction of a complete economy series of synchronous and permanent magnet stepper motors.

Two groups of 4-phase unipolar stepper motors are available now with step angles of 7° 30' and 15° and holding torque ratings from 7 mNm to 90 mNm. The first group are designed to operate in the pull-in area with optimum torque and speed; the second group are high-torque economy versions of existing types.

An economy series of reversible synchronous motors that are suitable for a variety of general industrial applications such as central heating or air conditioning systems are also announced.

These are available for use with a wide range of supply voltages, with speeds of 250 and 500 rpm, and torque ratings from 4 mNm to 70 mNm.

CIRCLE 138 ON READER SERVICE CARD

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PHILIPS

A Choice of 3 Highly Reliable 5 1/4" Floppy Disk Drives

TEAC has developed a series of 5-1/4 inch floppy disk drives which feature MFM and FM recording methods (no write precompensation necessary) in line with the industry's recent move towards standardization. All three models incorporate advanced TEAC technology which

gives them high reliability and capacity. A brushless motor has been used which has an extremely long lifetime (average 10,000 hours), while a high-precision lead screw method is used for positioning the head to the correct track, greatly reducing the possibility of data errors.

FD-50A

Single-Track Density

The FD-50A is TEAC's basic single-sided, single-track-density model. It features an extended 40 track format (48 tpi) and can also be used in 35 track mode for compatibility with the Shugart SA 400. In addition to the usual FM recording format, the MFM recording format can also be used, effectively doubling the disk's capacity. The interface specification complies with the proposed ANSI standard.

FD-50C

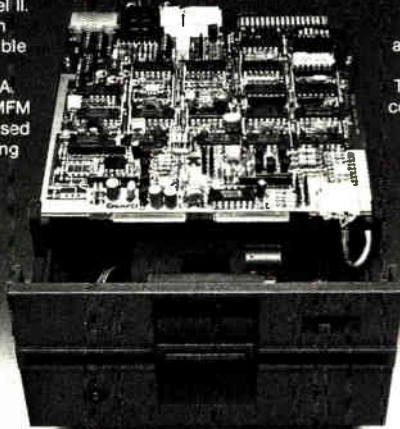
Double-Track Density (100 Tracks/Inch)

The FD-50C is a double-track-density version, compatible with the Micropolis 1015 Model II. It uses a 100-track/inch format, for more than double the capacity of the 48-track/inch FD-50A. And as with the FD-50A, MFM recording format can be used if desired, further doubling the disk's capacity.

FD-50E

Double-Track Density (96 Tracks/Inch)

The FD-50E is another double-track-density (80/70 tracks per disk) model. MFM and FM recording formats may be used, allowing a total capacity of up to 500K bytes. The interface specification complies with the proposed ANSI standard.



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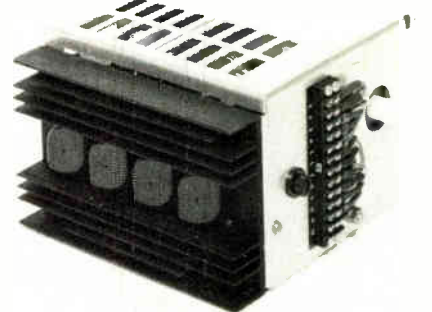
New products international



The model GID050-1 digitally controlled power supply produces constant voltage or constant current as designated by an IEEE-488 bus. It yields an output voltage of 0 to 49.99 V dc and an output current of 0 to 1 A. Takasago Ltd., 662 Futako Takatsu-ku, Kawasaki 213, Japan [453]



The HDR6 high-definition X-ray system is used with small-bore components. Its electron gun, with a 12-mm-diameter rod anode, focuses spots of approximately 0.04 mm. Andrex NDT Products (UK) Ltd., 12 Trafalgar Way, Bar Hill, Cambridge CB3 8SQ, England [454]



The 471-3100 range of modular high-voltage capacitor-charging units has a charging rate of 30 J/s from a 24-V dc supply. The five models have output voltages of 2.5 to 30 kV. Hartley Measurements Ltd., Kenward House, Hartley Wintney, Basingstoke, Hampshire, England [455]

Ever tried hardware and software debugging without the right tools?

Working with microcomputers, system debugging and integration are critical development phases. Without the right tools to help them, your hardware and software engineers are fighting a losing battle against mounting project costs and lead-time to completion.



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Symbolic debugging Cross-referencing of symbolic names to absolute hexadecimal values for establishing breakpoints, reading-out data, or other debug functions is done automatically by PMDS to let you concentrate on your job.

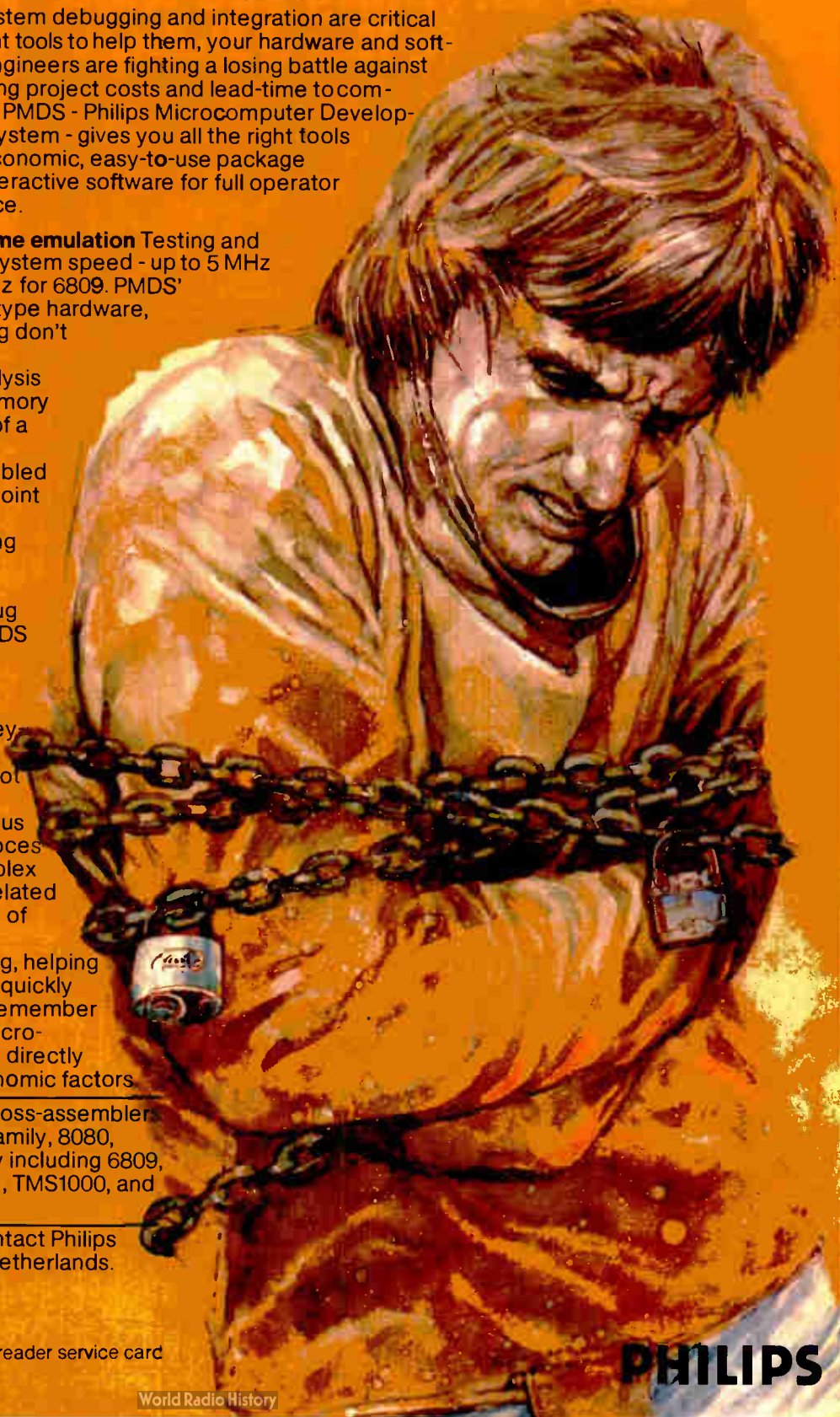
I/O simulation Built-in software commands can be used symbolically to specify PMDS system elements like keyboard, printer, screen and files for simulation of prototype I/Os that are not yet available.

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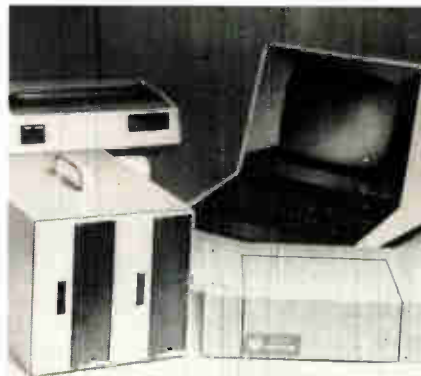
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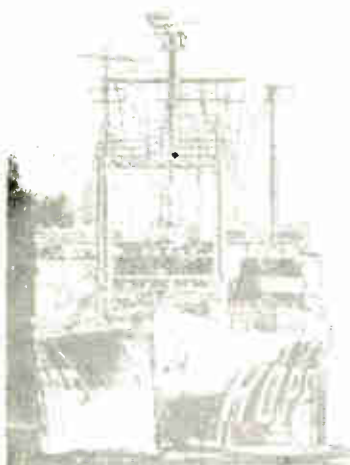
The UDS-1000 universal development system features a Z80 microprocessor with a 64-K-byte main-memory capacity and can emulate read-only memories and program erasable programmable ROMs. Multitech International Corp., 977 Min Shen E. Rd., Taipei, 105 Taiwan, Republic of China [456]



The JN 5302 digital calibrator measures dc voltages and currents in five ranges—20 mA at 1- μ A resolution, 200 mA at 10- μ A, 200 mV at 10- μ V, 2 V at 100- μ V, and 20 V at 1-mV. It has 13-mm liquid-crystal-display digits. AOIP, 1 boulevard Hippolyte Marquès, 75013 Paris, France [457]



A highly lithium-ion-conductive solid electrolyte was designed to produce solid-state batteries that are a maximum of 0.7 mm thick. It has a high energy density and a long shelf life without leakage. Hitachi Ltd., 5-1 Marunouchi 1-chome, Chiyoda-ku, Tokyo 100, Japan [458]



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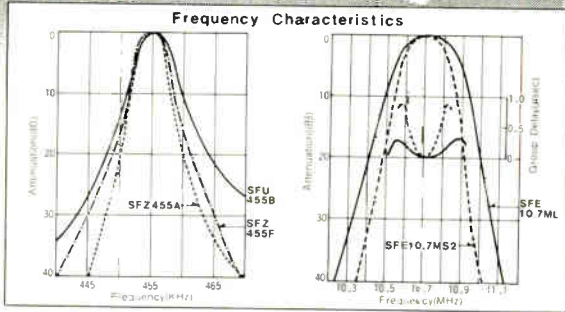
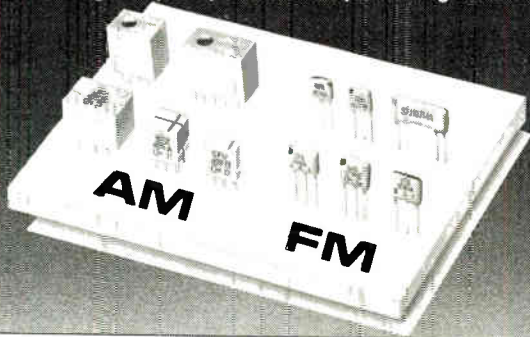
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3dB Band Width	4.5KHz±1KHz	6.5KHz±1KHz	4.5KHz±1KHz	10KHz±3KHz
Selectivity	-9KHz off +9KHz off	26dB min. 20dB min.	20dB min. 16dB min.	28dB min. 23dB min.
Insertion Loss	6dB max.	6dB max.	6dB max.	5dB max.

● 10.7MHz Ceramic Filter

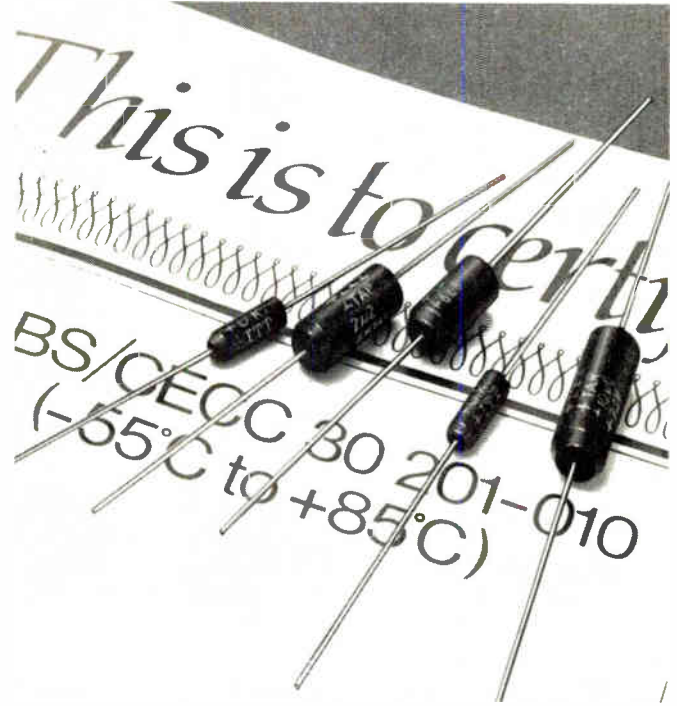
Part Number	For Radio			For FM IF Tuner	
	SFE10.7MA5	SFE10.7MS2	SFE10.7MJ	SFE10.7ML	SFE10.7MM
Center Frequency	A: 10.70MHz±30KHz (Red) B: 10.67MHz±30KHz (Blue) C: 10.73MHz±30KHz (Orange)			D: 10.54MHz±30KHz (Black) E: 10.76MHz±30KHz (White)	
3dB Band Width	280KHz ±50KHz	230KHz ±50KHz	150KHz ±40KHz	280KHz ±50KHz	230KHz ±50KHz
20dB Band Width	650KHz max.	600KHz max.	400KHz max.	700KHz max.	600KHz max.
Insertion Loss	6dB max.	6dB max.	10dB max.	9dB max.	11dB max.
Spurious Response (9~2MHz)	30dB min.	40dB min.	40dB min.	25dB min.	30dB min.
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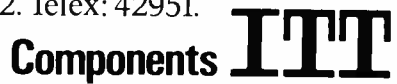
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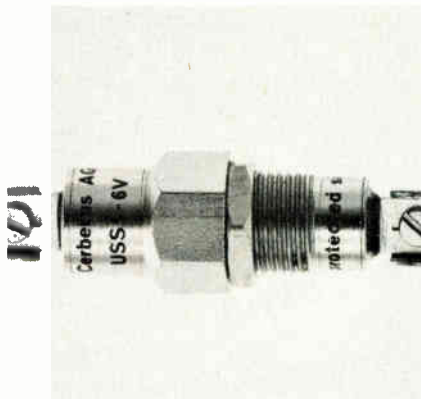


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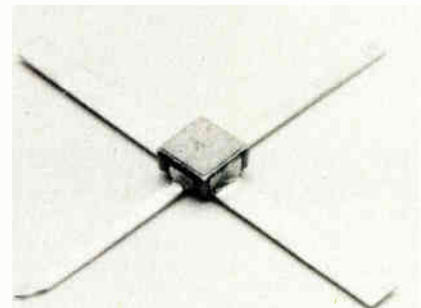
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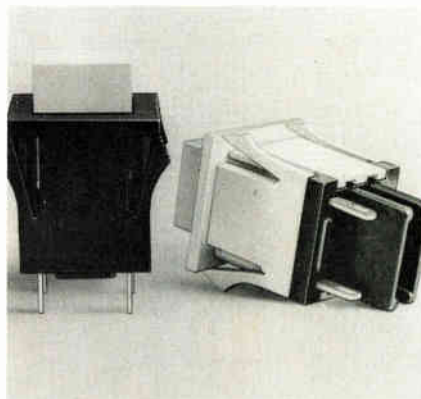
New products international



The USS 1 protection system is a mechanical feed-through unit designed to protect against overvoltages and interference. The protective circuits have discharge capacities of 25 kA and voltage ratings of 6 to 150 V. Cerberus AG, CH-8708, Männedorf, West Germany [459]



The MGF-1403 is a high-performance gallium arsenide field-effect transistor designed for Ku-band operation. It is a single-stage amplifier with a minimum noise figure of 2.7 dB and an associated gain of 6.4 dB at 18 GHz. Mitsubishi Electric Corp., 2-2-3 Marunouchi, Chiyoda-ku, Tokyo 100, Japan [460]



The 2200 series illuminated push-button switch has a contact resistance of 10 mΩ maximum and a dielectric strength of 2,000 V at 50 Hz minimum. It has a rating of 6 A at 250 V ac with a resistive load and 3 A at 250 V ac with a motor load. APR, 82270 Montpezat-de-Quercy, France [461]

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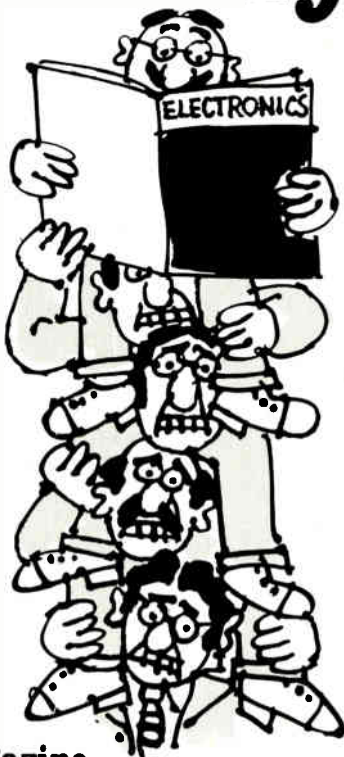
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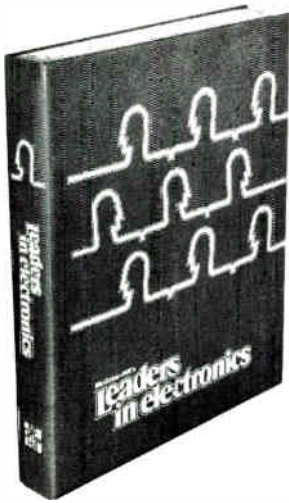
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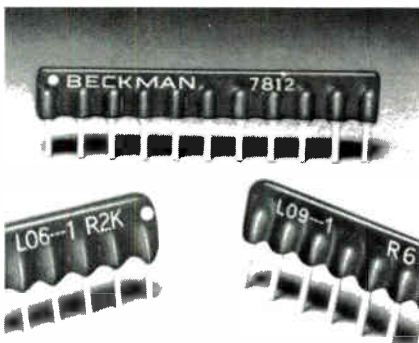
Electronics international



A solid-state electrostatic locator, housed in cast aluminum, runs off a single 9-V battery, which is included. The locator's two scales indicate 5,000- and 30,000-V deflection. Surrey Electro-Materials Ltd., Surrey House, London Road, Staines, Middlesex TW18 4HW, England [462]

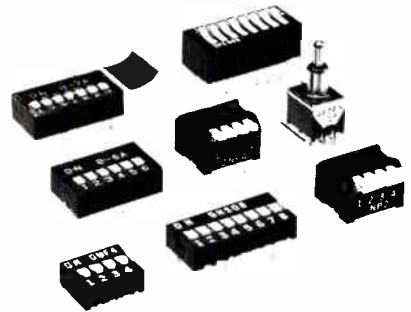


The QSF6 flowmeter employs silicon-chip technology to measure the flow of waste water in partially filled pipes and open channels. It uses a probe connected to a portable control and display unit. Quantum Science Ltd., 27 St. George's Rd., Cheltenham, Gloucestershire GL50 3DT, England [465]



The LXX series of resistor networks comes in low-profile 6-, 9-, 10-, and 11-pin single in-line packages with pull-up circuits or isolated resistors. Typical power dissipation is 180 to 200 mW per resistor. Beckman Instruments Ltd., Queensway, Glenrothes, Fife KY7 5PU, Scotland [464]

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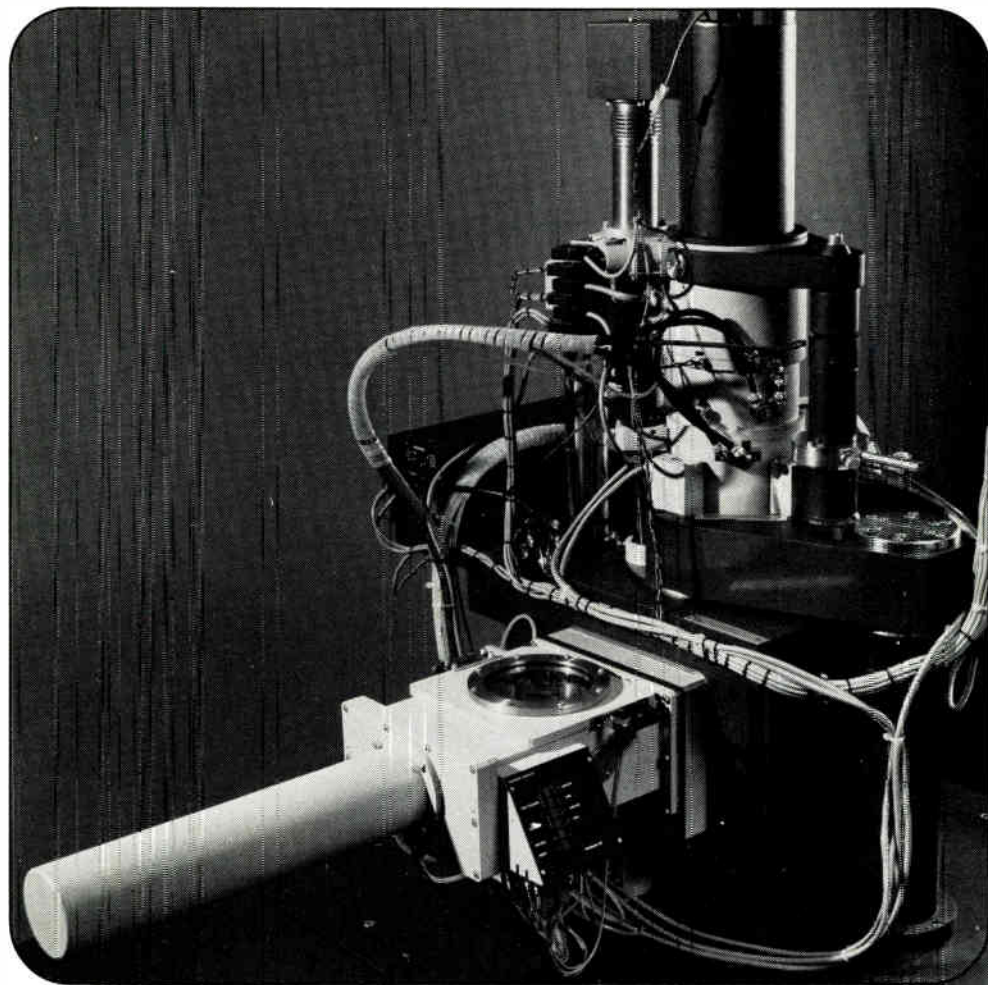
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Getting down to the finer details of microelectronics

As a leading manufacturer, and user, of micro-electronic technology, Philips is constantly searching for techniques that will improve the production process, or the product, or – ideally – both. This objective has now been achieved with the development of the 'Beamwriter' vector scan lithography system. In fact, it's the only production-oriented vector scan electron beam writing system available in the world.

Compared to conventional optical lithography techniques, vector scanning produces significant savings in the time taken to produce a set of masks or reticles; hours instead of days. It is also much more efficient than the raster scan E-beam method because the writing beam is directed only to points where exposure is required. The Beamwriter also generates an exposure dosage twenty times greater than other



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Invitation

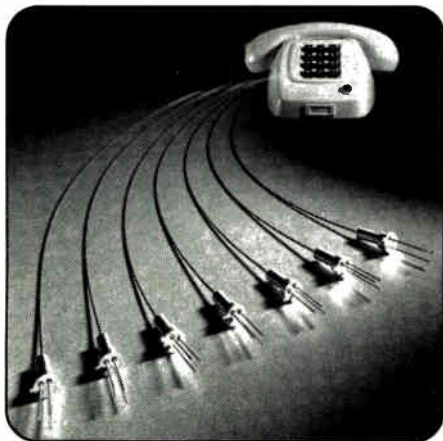
Please visit us at **Microelectronics** – international conference and exhibition of microelectronic production and test equipment – in **Eindhoven, Holland**.
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commercially available Electron Beam systems to provide a faster maximum writing speed and a wider choice of resists. Direct writing, with proximity correction if necessary, is also possible.

But perhaps the most remarkable feature of the Philips Beamwriter is its ability to produce beam spot sizes down to 0.025 microns. Which means that, while being right for the LSI circuit chips of today, it is

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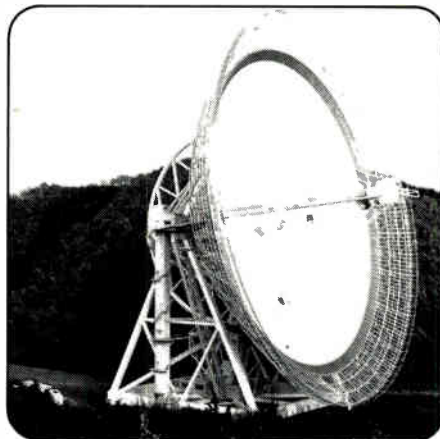
The Beamwriter is the result of integrating Philips' vast research facilities with the Company's expertise and experience in the fields of IC technology, electronics, computerised systems and electron optics. Here are some more examples of that multi-technology capability.



Long-haul optical transmission.

A 140Mbit/s optical transmission system utilizing the 5B/6B optical line code has been successfully completed in the Philips laboratories to demonstrate the feasibility of long-haul optical transmission. Intermediate repeaters, spaced 8km apart, were used to obtain a total length of 96km – the longest optical transmission run in the world! The system incorporates the remote alarm signalling, error monitoring and fault location facilities required for future operation. Presently, Philips is cooperating with the Dutch PTT in a 140Mbit/s field trial using 12-fibre armoured type buried cable connected between two nodal exchanges.

Circle 115 on reader service card



Data logging. Thermal distortion due to solar heating of the 100 metre dish of the Max Planck radio telescope in West Germany, is measured by means of temperature sensing at strategic points about the structure to an accuracy of 0.1°C by Philips PT100 probes and recorded on a Philips PM4000 data logger. The logged data is used to indicate when error-free observations can be made without correction for thermal distortion. **Circle 116**

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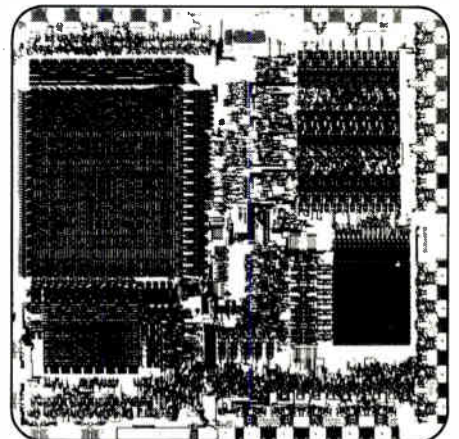
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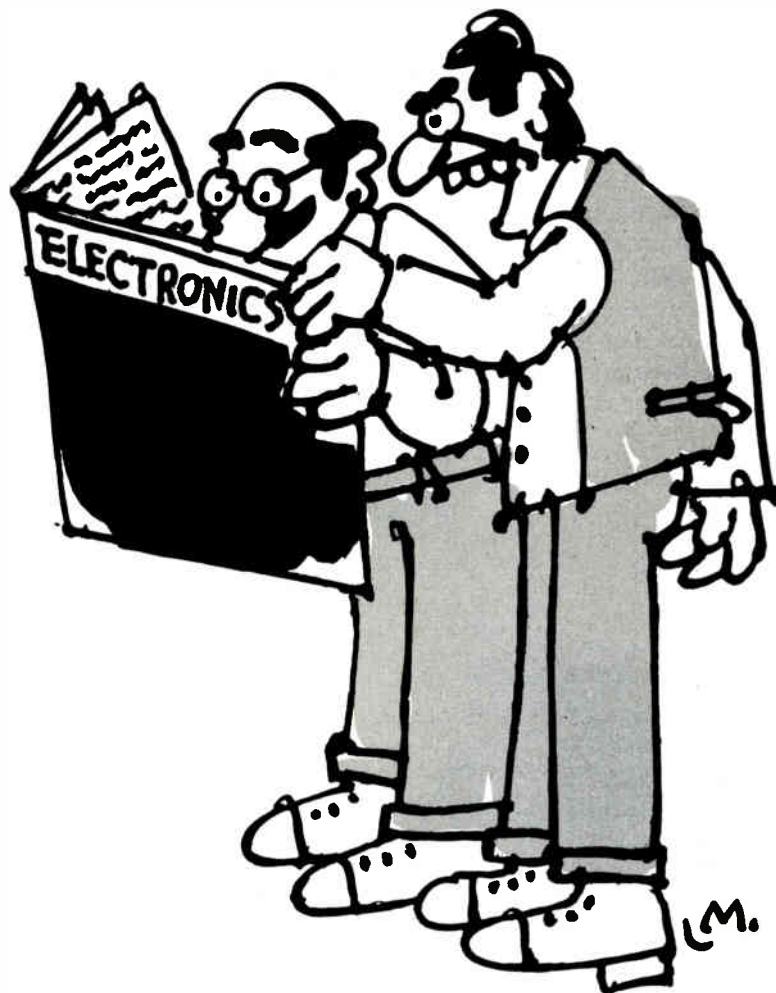
16-bit microprocessor chip, based on the Philips P851 hardware/software interface, has been developed by Philips Data Systems; one of the few computer manufacturers to have done so. Containing 17 000 active transistors in a 36mm surface area, the new chip will be used as a central processor in future systems. In addition to increased processing speed, the fact that the software interface does not change with regard to existing software means that the costly, time-consuming task of re-writing software is eliminated.

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Philips working on applied electronics

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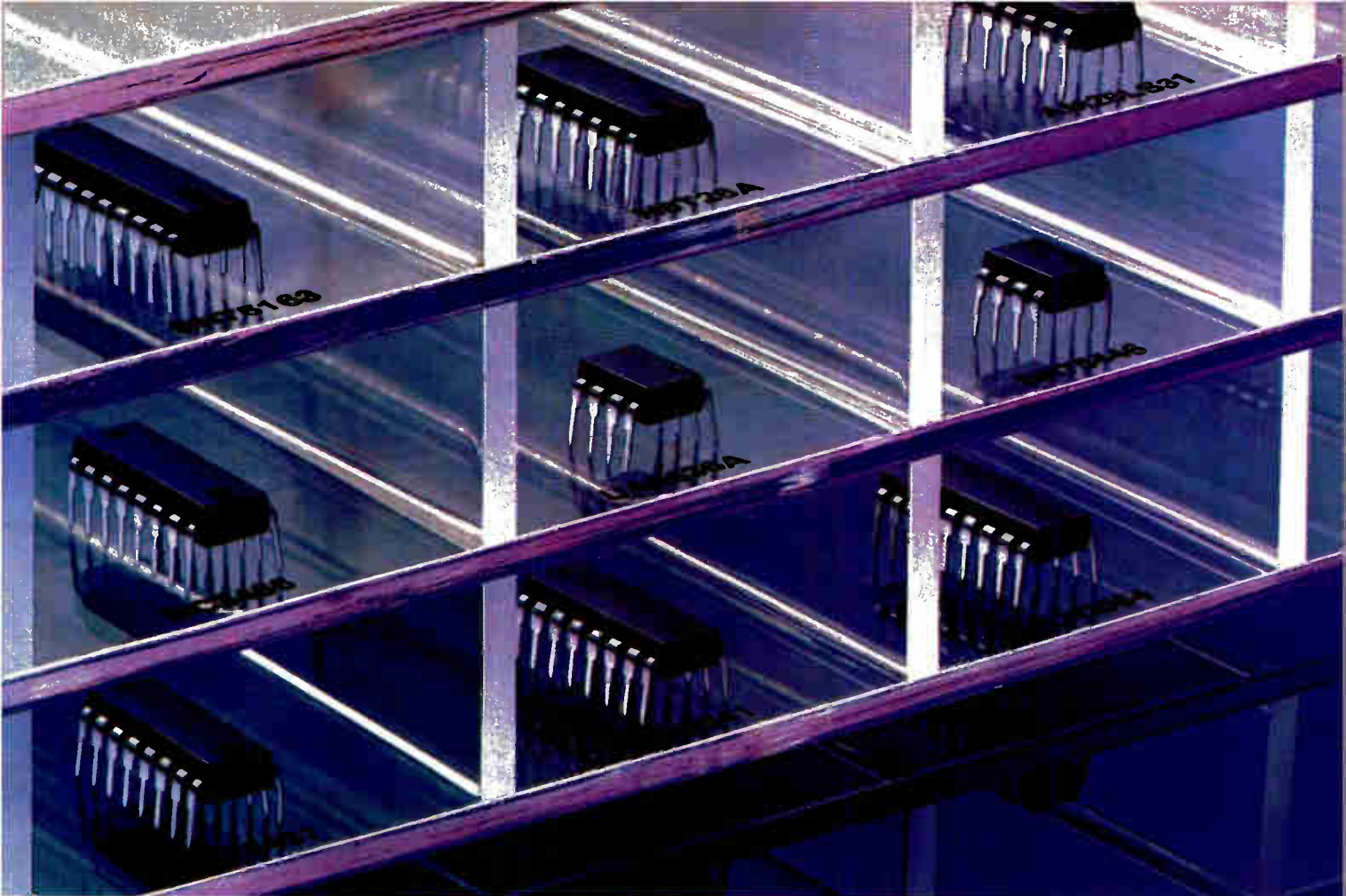
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Bus transceivers

For quick, easy board layout, octal SN75163, without internal line termination and with I/O pinouts directly across from each other. Choose three-state or open-collector output mode control for system flexibility. Other general-purpose bus transceivers are N8T26 and N8T26A — for high-speed, single-ended data transmission.

RS422/423 drivers/receivers

TI offers these versions of popular RS422 drivers/receivers as a second source. AM26LS31/32A and MC3486/87. Ideal for high-speed differential transmissions in a dedicated system. Enable for all four channels is a big plus, too.

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The industry leaders. Single package, monolithic devices that save assembly time and board space, improve reliability, cut component costs and drive all kinds of inductive loads. All the logic is on-the-chip. Availability is good and prices are competitive.

SN75446 is a low-power dual driver that checks in at 70 mW standby power (typ) and is capable of driving 400 mA and switching up to 50 V. Internal inductive clamp diodes, PNP inputs for very low (1 μ A) input current and all logic mode availability are some other key specifications.

SN75437, the next generation low-power quad driver with 700-mA drive capability, obtained by using unique single-saturated transistor output, features 200-mW standby (typ) and 35-V switching capability. This device is available in a 2-W copper lead-frame DIP.

UDN2841 and UDN2845 — 1.5-amp quad drivers with DTL, TTL and 5-V CMOS-compatible inputs. Switching power up to 35 V. UDN2841 sinks from a negative supply while UDN2845 sinks and sources. PNP level shifting allows operation to negative voltage. Offered in a 2-W copper lead-frame DIP.

Applications include DC motor drive, telephone relays and discharge printers, to name just a few.

The TI ULN2064 Series (2064 through 2069) and, additionally, ULN2074 and 2075, are quad Darlington drivers with 1.5-amp output current capability. Switching voltages vary from 35 to 50 V depending on the device. ULN2074 and ULN2075 employ sink or source mode outputs.

Prices and data sheets

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World Radio History

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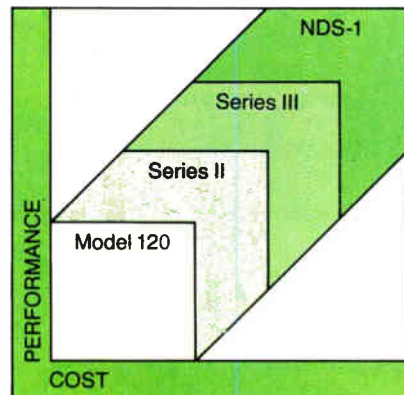
TYPE	CPU	SUPPORT
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	8022	ASM48, ICE49™
	8041A	ASM48, ICE41A™ Multi-ICE™
8-BIT	8080, 8085	ASM80, PL/M Pascal, FORTRAN COBOL, BASIC ICE80™/ICE85™ Multi-ICE™
	iAPX 88	ASM88, PL/M Pascal, FORTRAN ICE88™
16-BIT	iAPX 86	ASM86, PL/M Pascal, FORTRAN ICE86™
	iAPX 86/20, iAPX 88/20 (numeric data processor)	ICE86/88™ Extensions ASM89 Real Time Breakpoint Facility (RBF)
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World Radio History

ISSCC opens era of ultra LSI

HP's six-chip set goes beyond LSI as meeting also establishes that C-MOS is the leading technology for memories and processors

by John G. Posa, Solid State Editor, and Roger Allan, Components Editor

No sooner is the potential of very large-scale integration demonstrated than word comes of ultralarge-scale integration. How else is it possible to categorize a 32-bit processing system composed of six chips holding up to 600,000 transistors apiece? Such a system will be reported by Hewlett-Packard Co. at the next International Solid State Circuits Conference, to be held Feb. 18-20 at the Grand Hyatt Hotel in New York City.

In 17 day sessions and 10 evening panel discussions, this grandest of all semiconductor conferences will do more than prove the industry's ability to integrate 100,000-plus transistors onto a silicon substrate. It will remove all doubt that complementary-MOS technology is a clear winner for memories and microprocessors, perhaps for VLSI in general. ISSCC '81 will also help suggest new applications for an emerging class of very high-voltage integrated circuits and extremely accurate data-acquisition circuits.

In addition, with achievements like those from the Fort Collins (Colo.) division of HP and elsewhere, the conference will question whether the ever-specialized needs of VLSI chip consumers can be met with standard components from today's vendors or if they will need to be custom-crafted by captive suppliers. And, perhaps most importantly, the contributions will underscore the unrelenting productivity of Japan.

Where are dynamics? At last February's conference, 256-K and bigger Japanese dynamic random-access memories seemed to come out of the blue [*Electronics*, Feb. 14, 1980, p. 138]. This time, if not for a chip that was the original charter of

Inmos Corp. in Colorado Springs—a 64-K RAM—and a so-called pseudo-static device from Intel Corp.'s Aloha, Ore., operation intended for use with its microprocessors, dynamic RAMs would be practically absent. It was hoped that U. S. companies would have their quarter-megabit RAMs ready, but perhaps they are holding off for dramatic late-news slots as the Japanese did.

In place of dynamic devices, there are static RAMs of all kinds, hurdling density and performance barriers. The presence of 4-K static RAMs means that superfast C-MOS is not waiting for anything. For 18- to 25-nanosecond access times that handily surpass comparable n-channel devices, Toshiba Corp. opted for a bed of sapphire and molybdenum silicide [*Electronics*, Sept. 11, 1980, p. 80]. Hitachi Ltd. scaled its high-performance process into second-

generation Hi-C-MOS II, and Intel preferred n-type to p-type diffused wells for its new bulk silicon process [*Electronics*, Dec. 4, 1980, p. 39].

Mostek Corp. of Carrollton, Texas, will reveal a memory with dynamic features, such as a capacitor for storage, that latch data like a static RAM. The result is a 4-K-by-8-bit chip with only four elements per cell instead of six. IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., will present three papers on memory technology, one of which concerns a new dynamic cell that takes up an area of only 34 square micrometers. Even the smallest of today's 64-K RAM cells are well over 100 μm^2 . IBM reduced the size by using tungsten silicide to improve propagation to and from the cell.

Nippon Electric Co. is also using silicide technology to pep up polysili-

MICROPROCESSORS AND DIGITAL CIRCUITS AT THE ISSCC

Session	Description	Source
9.1, 9.2	A 32-bit processing system comprises a central processing unit, I/O processor, memory controller, 128-K RAM, and 512-K ROM.	Hewlett-Packard
9.3	13,000 transistors are integrated in a 16-bit n-MOS processor that executes minicomputer instructions over a microprocessor bus.	Digital Equipment, Integrated Circuit Systems
9.4, 9.5, 9.6, 9.7	An execution unit, instruction decoder, and I/O interface processor make up a very large-scale integrated 32-bit microcomputer.	Intel
16.1	An 8-bit reconfigurable single-chip microcomputer contains a 1-K-byte rewritable program memory and a 60-byte nonvolatile RAM.	Hitachi
13.3	Analog inputs are read by an implantable 4-bit C-MOS biomedical microcomputer that then generates analog output signals.	Intersil
13.4	A graphics display controller manipulates an off-chip 256-K-by-16-bit memory to draw color pictures at a rate of 800 ns per dot.	Nippon Electric
2.5	A complete single-chip speech-synthesis system will talk for 8 to 10 seconds from an internal ROM or longer with external memory.	General Instrument
16.4	A 2,500-gate bipolar master slice, with 0.8-ns, 0.5-mW gates, replaces a multitude of small- and medium-scale integrated chips.	Mitsubishi

Probing the news

con, but in a late-model 16-K static RAM. Texas Instruments Inc. of Dallas will show a competing memory that has nearly the speed of the NEC RAM—a 30-ns access time—without having to resort to refractory metals. Intel will again discuss its 16-K-by-1-bit static RAM, this time explaining why it went back and added redundancy to the chip [*Electronics*, Dec. 4, 1980, p. 108]. Inmos's 64-K RAM will also have on-chip spare parts for fault tolerance. In fact, component-level redundancy has become so consequential that an evening panel discussion will be devoted to it.

NEC will be the second to announce a 64-K static RAM, following Matsushita Electric Industrial Co. [*Electronics*, Nov. 6, 1980, p. 145] at the last ISSCC. But while Matsushita puts its 8-K-by-8-bit unit in a 24-pin package for plug compatibility with byte-organized read-only

HIGH-SPEED CIRCUITS AT THE ISSCC		
Session	Description	Source
7.1	Commercially available field-effect transistors in a three-stage amplifier provide 12 ±1.5 dB of gain from 150 MHz to 16 GHz.	Thomson-CSF
11.3	Hyperabrupt gallium arsenide varactor diodes tune an on-chip 4-mW GaAs FET oscillator over a frequency range of 7.3 to 15.6 GHz.	Texas Instruments
13.5	A single-chip fiber-optic receiver accepts inputs directly from a photodiode and converts them into digital data at 200 Mb/s.	IBM
15.6	Self-alignment and titanium-tungsten gates team up in ultrahigh-speed GaAs metal-semiconductor FETs having 50-ps propagation delays.	Fujitsu

memories, NEC's chip, curiously arranged by 1 bit, matches the pinout of 16-pin 64-K dynamic RAMs.

In terms of raw speed, however, the ribbon goes to the Musashino Electrical Research Laboratory of the Nippon Telegraph & Telephone Public Corp. It will unveil a 1-K emitter-coupled-logic RAM with an access time that dips below 3 ns. Self-alignment of polysilicon is in part responsible for its process, which could conceivably produce a

5-ns 4-K bipolar RAM. In the area of ROMs, Synertek Co. of Santa Clara, Calif., will describe a 45-ns mask-programmable device with a standby power consumption of 75 milliwatts, and West Germany's Aachen and Duisburg Universities will present a 1-K ROM that tests itself.

Chip computers. Along side HP's processor, which consists of a central processing unit, input/output processor, memory controller, 128-K RAM, and 512-K ROM, Intel and Digital Equipment Corp.'s Hudson, Mass., unit will discuss their own solid-state computers. Working with Integrated Circuit Systems of Worcester, Mass., DEC has taken a low-density approach in integrating one of its 16-bit minicomputers onto a 13,000-transistor chip. Intel managed to get a paper accepted on each chip in its set [*Electronics*, Nov. 6, 1980, p. 42]—an execution unit, a 32-bit instruction-decoding unit, and an I/O interface processor—as well as a fourth paper on the management of the project. Also, Toshiba will again discuss its 16-bit C-MOS-on-sapphire microprocessor, and the Hitachi Central Research Laboratory will apparently be the first to preview a microcomputer with an on-chip writable control store using electrically erasable storage.

Still, the bulk of the papers in the program will concern the latest analog ICs. Signetics Corp. of Sunnyvale, Calif., produced an open-loop programmable amplifier with a maximum gain-bandwidth product of 1 gigahertz. The device, which achieves such performance by localized positive feedback, is linear within 0.1% for a 1-volt peak-to-peak output signal over an externally programmable gain range of 0 to 100.

MEMORIES AT THE ISSCC		
Session	Description	Source
1.1	Complementary-MOS on sapphire and 2- μ m molybdenum-silicide gates produce an 18-ns 4-K static random-access memory with a 50- μ W standby power dissipation.	Toshiba
1.2	Double-polysilicon Hi-C-MOS II technology builds an 18-ns, 150-mW 4-K static RAM in bulk silicon using 2- μ m rules.	Hitachi
15.1	N-type wells in a high-resistivity substrate allow a 4-K C-MOS static RAM a 25-ns access time and microwatt standby consumption.	Intel
1.3	1.5- μ m design rules are used for a 64-K-by-1-bit static RAM that fits into a 16-pin package just like a dynamic memory.	Nippon Electric
1.4	Scaled-down n-channel technology and double-level polysilicon are all that is needed for a 30-ns 16-K-by-1-bit static RAM.	Texas Instruments
1.5	A 25-ns 16-K-by-1-bit n-MOS static RAM gets its speed from subnanosecond molybdenum word lines and 1.5- μ m photolithography.	Nippon Electric
8.3	Redundancy is used in a fault-tolerant 100-ns 64-K dynamic RAM with on-chip refreshing not controlled via pin 1.	Inmos
8.4	Three transistors and a storage capacitor—not six components—form cells in a 4-K-by-8-bit fully static RAM.	Mostek
8.5	Multiplexed address, data, and input/output signals interface a self-refreshing 4-K-by-8-bit dynamic RAM with 8- or 16-bit microprocessors.	Intel
12.3	1- μ m features result in a 34- μ m ² dynamic RAM cell, speeded up with tungsten silicide films.	IBM
12.4	Storage capabilities are multiplied in a multilevel charge-coupled-device memory insensitive to geometry and parameter tolerances.	IBM
12.6	Integrated injection logic and merged-transistor logic are given split emitters for an I ² L-MTL memory cell with double the speed of older designs.	IBM
13.7	Peripheral circuits double as logic-checking hardware on a self-testing 1-K read-only memory with error detection better than 99.6%.	Aachen and Duisburg universities
15.5	What is called super-self-alignment of polysilicon base with emitter regions takes credit for a 2.7-ns 256-by-4-bit emitter-coupled-logic RAM.	NTT Musashino Electrical Communication Laboratory

HIGH-VOLTAGE CIRCUITS AT THE ISSCC

Session	Description	Source
2.3	A multilayer bipolar and diffused-MOS video amplifier chip can drive color-TV-tube cathodes directly with 120-V output swings.	Thomson-CSF
3.5	Bipolar power transistors with transition frequencies of up to 50 MHz can dissipate 250 W with collector voltages of 200 V.	Robert J. Widlar
15.2	ICs fabricated in silicon grown epitaxially on spinel incorporate bipolar and MOS devices that can withstand 250 V.	Fujitsu
17.1	Dual-gate MOS FET circuitry makes for an optically coupled 450-V crosspoint array aimed at telecommunications applications.	Oki, NTT Musashino Electrical Communication Laboratory

Signetics also collaborated with the University of California at Berkeley to produce a 700-megahertz four-terminal IC amplifier with 18 decibels of gain and a noise figure of 4 dB. The 50-ohm-terminated device is housed in a four-lead TO-46 package and consumes a mere 180 mw.

Highly sensitive. Sony Corp. will discuss a silicon Hall-effect sensor whose saturation velocity principle allows it to achieve high magnetic sensitivity independent of bias voltage and temperature. A micropower modified bandgap voltage reference from National Semiconductor Corp., Santa Clara, Calif., that compensates for inherent transistor base-emitter thermal nonlinearities will also be described. And Cal-Berkeley researchers will discuss a 1.3-GHz bipolar voltage-controlled IC oscillator that drifts but 60 parts per million per °C from dc to 20 MHz.

Robert Widlar, now a consultant in Jalisco, Mexico, will discuss an active ballasting technique he has employed to increase bipolar power-transistor capabilities at high frequencies. Such oxide-passivated transistors with cutoff frequencies of 50 MHz are capable of dissipating 250 w at collector voltages over 200 v. Less than 1-v saturation is reported at a 10-ampere current.

A dual-channel high-fidelity audio IC for volume and tone control from Sony exhibits just 0.002% distortion and a 100-dB signal-to-noise ratio. Members of Thomson-CSF's Semiconductor division in Saint-Egrève, France, will discuss a 220-v dc IC that can drive the cathodes of a color TV cathode-ray tube. Made with a bipolar and double-diffused-MOS process, the IC features a peak-to-

peak output of 120 v.

From Japan comes a set of four bipolar analog-to-digital converters made by Hitachi. The LSI 40-MHz converters are made from a combination of integrated injection logic and Schottky devices. Hitachi will also show off a 14-bit monolithic d-a converter that needs no trimming. The self-compensating ¹²L device has a linearity error of $\pm 1/2$ least significant bit ($\pm 0.003\%$).

Nevertheless, U. S. semiconductor manufacturers are still in the forefront of data-converter technology. Intersil Inc. of Cupertino, Calif., has designed a 14-bit C-MOS a-d converter with a 20- μ s conversion time and error correction capability. The 4.1-by-4.2-millimeter chip has a thin-film nonbinary 17-bit d-a converter that resembles an R-2R ladder network but uses a radix of about 1.85 instead of the usual 2. The a-d converter includes a conversion algo-

rithm as well as an erasable programmable read-only memory for calibration. A two-chip 12-bit a-d converter from Harris Semiconductor Corp., Melbourne, Fla., will also be discussed. It is notable for its total error of less than ± 1 LSB over -55° to $+125^\circ\text{C}$.

Getting higher. The need for higher-frequency and higher-power microwave devices is forever on the rise, as evidenced by two complete sessions on this subject. TI will report on a K-band (10.9-to-63.0-GHz) gallium arsenide power field-effect transistor amplifier with an output of 675 mw and a gain of 5.8 dB at 20.5 GHz. Even at 25 GHz, its output is still a respectable 200 mw. TI has also developed an octave-band varactor-tuned GaAs FET oscillator that operates over 7.3 to 15.6 GHz with 4 mw of output power. Hyperabrupt GaAs tuning varactors are used in the gate and source networks of the new device.

The Massachusetts Institute of Technology's Lincoln Laboratory at Lexington has come up with a GaAs millimeter-wave receiver. The 31-GHz prototype monolithic unit was made by integrating mixer diodes and metal-semiconductor FETs on a GaAs substrate. The single-chip receiver exhibits a conversion gain of 4 dB and a receiver noise figure of 11.5 dB.

Information about attending the ISSCC is available from Lewis Winner at (305) 446-8193. □

DATA-ACQUISITION CIRCUITS AT THE ISSCC

Session	Description	Source
2.1	Linearity to within $\pm 0.003\%$ or $\pm 1/2$ LSB is achieved in a 14-bit digital-to-analog converter sans trimming.	Hitachi
6.1	A 12-bit analog-to-digital converter with integral track-and-hold circuitry exhibits less than ± 1 -LSB error over a range of -55° to 125°C .	Harris
6.5	A 17-bit nonbinary d-a converter and an erasable programmable ROM are found in an error-correcting 14-bit 20- μ s C-MOS a-d converter.	Intersil
14.1	A low-noise operational amplifier with a 30-MHz gain-bandwidth product has a peak-to-peak noise of only 80 nV from 0.1 to 10 Hz.	Precision Monolithics
14.4	A 700-MHz bandwidth, 18 dB of gain, and a 4-dB noise figure are some of the specifications of an 18-mW four-terminal amplifier.	University of California at Berkeley, Signetics
14.6	Linearity in a 1-V output signal is 0.1% for an open-loop amplifier, and this gain is externally programmable from 0 to 100.	Signetics
10.1	A passive recursive CCD bandpass filter for modems has a bandwidth of 97 ± 3 Hz at 131.85 kHz or a Q of 1,350.	Siemens

Consumer electronics

Toy and game consumer sales soften

Retailers cut Christmas inventories as hand-held games back away from their peak figures; home computers hold steady

by Pamela Hamilton, New York bureau manager, and Gil Bassak, Industrial/Consumer Editor

With the holiday shopping season at its peak, electronic toy, game, and entertainment manufacturers are cautious about evaluating the market. Perhaps because of the recessionary trends earlier this year or the uncertainty about the economy for the next, consumers are buying fewer electronic toys and games than last year and seem to be shying away from the bigger-ticket items. But nonentertainment items, such as home computers, are doing better.

Despite a predicted market of \$500 million for 1980, retailers have cut back their inventories of electronic games in some areas, stocking only one or two items they may have had half a dozen of last year. The popularity of hand-held games, the bulwark of the electronic game market for the past few years, may be decreasing, with sales this year just matching those of 1979. Personal computer and video disk system sales are on the upswing, though they still

represent a small part of the Christmas retail picture.

For G. A. (Tony) Clowes, president of Entex Industries Inc., maker of the hand-held Space Invaders, the electronic games market has two aspects. "The simpler toys will drop out in the next year, while the newer, higher-technology items will tend to command a price. Although these newer items will expand the market, there will be a fallout in the lower-technology toys, and the effect will be to level out the market," he comments. In fact, he notes that this trend has already started, with some of the bigger companies winding up with a large inventory of simple hand-held games, causing uneasiness throughout the industry. He does not expect Space Invaders, his Compton, Calif., company's biggest seller, to lose any headway this year or into the next.

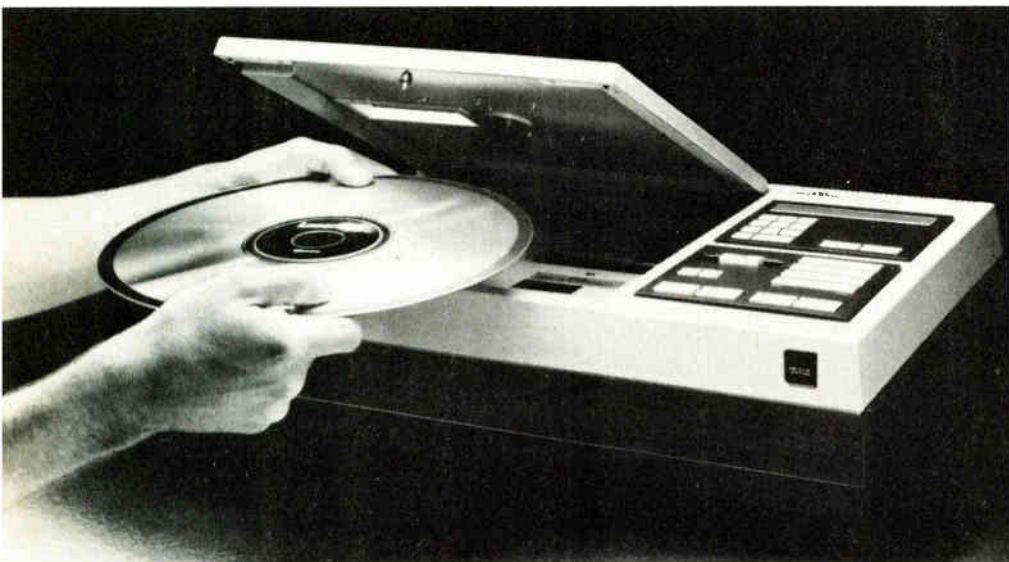
Mattel Inc. is one of the major companies experiencing a softening

in the sales of its hand-held games. The Hawthorne, Calif.-based manufacturer attributes the slowdown to effects of the recession, increased competition, and a glut in the market. Its hand-held games fall into four categories: sports, action, strategy, and personal service. A horse race analyzer, which is classified as a personal service item, is said to be doing somewhat better than the others. With a retail price of \$125, the microprocessor-based analyzer takes into account 31 factors from the daily tip sheet to rate horses.

Kenner Products in Cincinnati is in consensus with the industry belief that electronic toy sales are flat this year. "Economic conditions are making it hard for people to take \$50 and plop it down for one toy," notes a spokesman for the division of General Mills Creative Products group. He also notes that games appealing to adults are not doing well either, "because gift buyers are sticking more to the bare essentials like clothing rather than luxury items such as electronic games."

Ranks second. Kenner sales are said to be more than \$200 million annually, putting it second to Mattel with \$496 million. Kenner's product line includes Star Wars Battle Command, introduced last year and retailing for between \$30 and \$35, as well as Live Action Football and Redline Electronic Drag Race, both introduced this year for about \$40. Star Wars uses devices from National Semiconductor and Panasonic; the others use Texas Instruments chips.

Christmas pictures. LaserDisc from U. S. Pioneer, is one of two video disk systems available to consumers this Christmas.





Talk of Texas. TI's hand-held Speak & Read teaching aid is selling well this holiday season, says the company. Its educational nature helps to keep sales solid throughout the year.

For Parker Bros. in Beverly, Mass., the 1980 Christmas season will match last year's, even though the panic buying of scarce games that took place in 1979 will be absent this year and shoppers will face a slower economy. Parker's 1980 entries have been Bank Shot—an electronic pool game aimed at the eight-year-old to adult market—and Split Second—a manual dexterity game aimed at seven-year-olds to adults. The microprocessor-based games each contain 50 to 70 light-emitting diodes and cost \$50 to \$55.

A small computer aimed at children and a hand-held baseball game top Coleco Industries Inc.'s bestseller list this season. The Electronic Learning Machine uses a 4-bit microprocessor, with 1K of read-only memory for storing the program. A card reader and cartridge pack are used for the application data. The Head-to-Head baseball game is another in the Hartford, Conn., manufacturer's line. Both items retail for about \$40.

Tip-top at TI. According to a spokesman at Texas Instruments Inc. in Dallas, the company's Speak & Spell, Speak & Math, and Speak & Read are all selling well. "These products tend to be less seasonal than other toys because they are also educational," he says.

For Atari Inc., the home computer

market has not developed as quickly as was predicted, but nevertheless the company reports its model 400 and 800 home computers are doing well. The Sunnyvale, Calif., firm's hand-held Touch Me game, like its video-computer system with program cartridges, is also maintaining a strong market position.

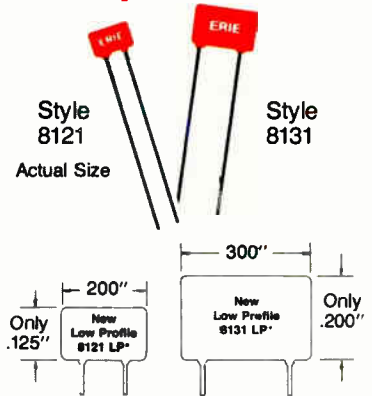
Some industry analysts have noted that home computers sold in retail computer shops may be doing better than those at toy counters. Sales of Commodore Business Machines Inc.'s CBM 8032 personal computer seem to bear this out. The under-\$5,000 system, including CPU, disk drive, and printer, had its first shipments this summer and has helped to push the Norristown, Pa., company's net sales for the first quarter of fiscal 1981 up 42.3% over last year's.

Optical Yule. Another growth area for electronic-based systems is video disks, and two are available for this Christmas season. Magnavox Consumer Electronics Co., Knoxville, Tenn., is marketing its laser-based Magnavision disk player in 33 cities, at a retail price of about \$775. LaserDisc, also an optical system, from U. S. Pioneer Electronics Corp., Moonachie, N. J., is available in 46 cities at a retail price of about \$750. A spokesman says that unit sales of the system for 1980 should be in the "five-figure bracket." □

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Testing

VLSI spurs self-testing

Test systems can be built on boards for go/no-go indication or onto the chips themselves for added fault detection

by Jerry Lyman, Packaging & Production Editor

The increasing density of very large-scale integrated circuits is challenging the limits of present automated testing technology. Soon, chips with more processing power than the machines available to test them will appear, and the sheer volume of devices per chip in the coming VLSI circuits will be staggering. In 1970, a typical IC had about 10,000 devices; this year, the total sometimes exceeds 100,000. By 1990, ICs with possibly over a million devices will be making unprecedented demands on device and board testers.

Two solutions have been advanced: boards with built-on self-testing and VLSI devices with on-chip self-testing. IBM Corp. and other large mainframe computer houses have been applying both techniques for some time to their own production testing. But a packaged VLSI device with built-in green and red light-emitting diodes functioning as go/no-go signals that would simplify chip testing is currently little more than a blue-sky idea.

Still, appreciable advances have been made in the development of both strategies for comprehensive self-testing. At Siemens Corp.'s corporate research and technology center in Cherry Hill, N. J., engineers are in the midst of a program aimed at a built-on board-level go/no-go test method for detecting faults in digital circuitry. Called Bidco (built-in digital circuit observer), the on-board hardware applies a set of pseudorandom stimuli to the circuit under test, captures the output response of the circuit with a parallel signature register, and decodes the output of the signature to determine if the circuit meets specifications.

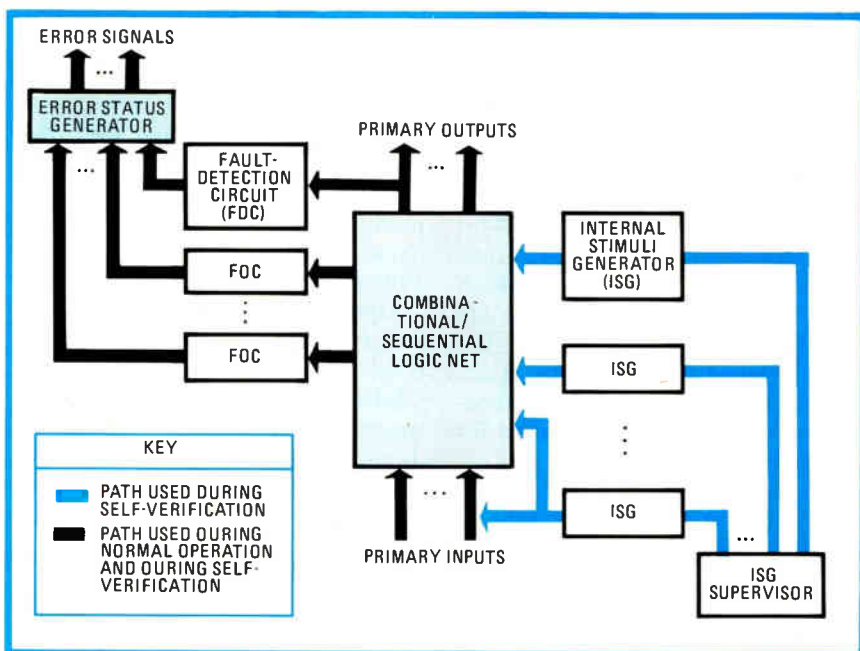
The whole process ultimately lights one of two status indicators signifying a pass or fail.

The key to the Siemens test system is its use of two identical general-purpose registers called Bilbos (built-in logic block observers). These circuits, presently built out of TTL ICs, can be externally configured as a pseudorandom pattern generator or a parallel signature register, or they can be combined into the normal circuitry. As shown in the block diagram of the Bidco method on page 78, Bilbo A is configured as a pseudorandom pattern generator and supplies patterns to the circuit under test. The circuit's outputs are then fed to Bilbo B, which is configured as a parallel signature register. Bilbo B's output in turn feeds a decoder

designed to detect a specific code. The output of the decoder, depending on its state, feeds either the fault or the fault-free indicator.

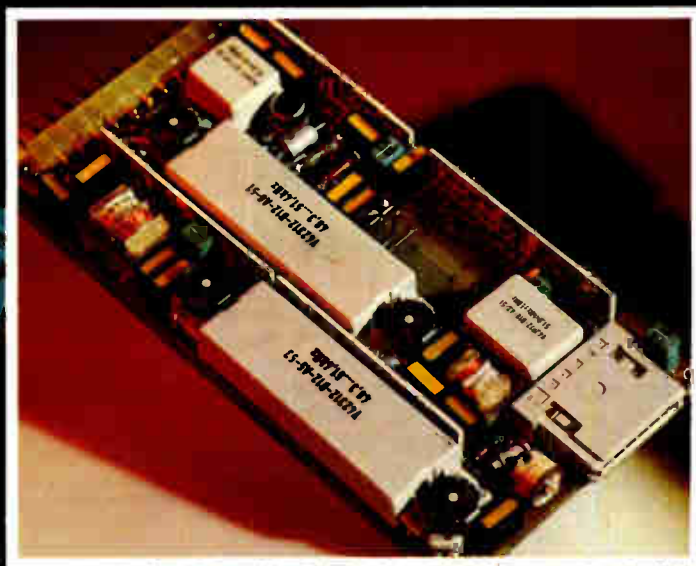
Bidco does have two disadvantages that impose limitations on its potential. First, it is only a go/no-go method and thus cannot isolate a specific fault. In addition, it is not possible to use the method on a microprocessor. Nevertheless, for circuits with many flip-flops, Bidco provides a rapid test.

On-chip test. A completely on-chip approach to VLSI testing is the self-verification technique developed by Richard Sedmak of Sperry Univac in Blue Bell, Pa. Self-verification is defined as the ability of logic to verify a failure-free status automatically, without the need for externally



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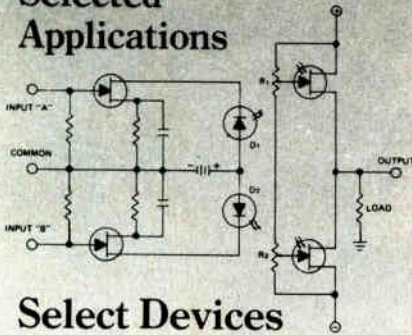
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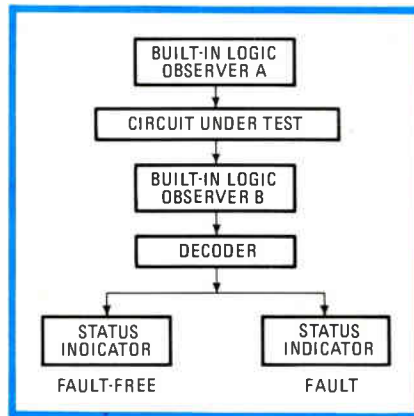
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Probing the news



On the board. Key to Siemens' Bidco (built-in digital circuit observer) are two identical Bilbos (built-in logic observers) that are implemented with TTL integrated circuits.

applied test stimuli (other than power and clock) or for test logic that is part of the system. This powerful technique can be applied to microprocessor testing and can isolate faults, in addition to providing go/no-go testing.

In self-verification, the logic runs at machine speeds; test generation and circuit modeling are not needed. There is no need for diagnostics and hardware for go/no-go tests, and a major portion of the logic required for self-verification is also used for automatic fault detection during normal operation.

A generalized block diagram of the self-verification approach is shown on page 76. Fault-detection circuits, internal stimuli generators, an internal stimuli generator supervisor, and an error-status generator are all integrated on a chip along with its basic logic function.

What and where. In the self-verification mode, the internal stimuli generator supervisor controls the stimuli generators, which exercise the logic thoroughly. The fault-detection circuits sense any faults and provide an input to the error-status generators, which assemble and encode information about the presence and location of faults.

During normal operation, the fault-detection circuits simply monitor the device's logic. Any intermittent or solid failures are detected by the circuits and transmitted to the error-status generator. □



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Communications

Britain opens telecom market a bit

The establishment of British Telecommunications as a separate entity from the post office permits some competition for sales of gear and servicing

by Kevin Smith, London bureau manager

Britain has opened the way for private companies to compete with the government in telecommunications services. A bill approved this month by Parliament separates the nation's postal and telecommunications wings and establishes British Telecom—actually, the legislation calls it British Telecommunications, but it refers to itself by the trendier version—as a new corporation. In addition, it permits private companies to

It pays. New pay phone from British Telecommunications contains a microprocessor that figures the toll and provides credit.

compete with BT in providing terminal equipment, value-added services such as electronic mail, and carrier facilities like Telex, satellite, and other communications links.

Loosening the British Post Office's monopoly will lead to explosive growth as private companies compete with the state to exploit new technologies—at least that's the scenario advanced by free-market Conservatives. But in practice, the demonopolization falls far short of Conservative plans for unfettered competition and makes major concessions to both BT and British

weeks, with IBM Corp. as one of its members.

Among the concessions to BT disliked by industry is its right to supply the first phone in each household, as well as to maintain privately supplied equipment. Jeff Samson, who heads Standard Telephones & Cables Ltd.'s Switching division, argues that service is part and parcel of equipment sales. He maintains that BT cannot possibly guarantee the needed stock levels or the technical expertise for the products of many different manufacturers and would not display the same sensitivity to customers' needs as the equipment maker. However, a compromise solution may have maintenance of some systems subcontracted back to the manufacturer.

Still, the proposed liberalization goes further than in other European countries in that Sir Keith will seek safeguards for British industry. First, the domestic suppliers have been granted a three-year period in which to prepare more competitive products before foreign manufacturers are allowed to enter the market. Furthermore, Sir Keith says, "We shall open our market to overseas competition only to the extent that overseas markets are open to us."

Eye standards. Another fear of British manufacturers is that the new bill, in replacing the post office's licensing authority with an independent body under the direct control of the state secretary, will perpetuate post office standards. Sir Keith, however, is aware that terminal gear has been tailored too minutely to British needs in the past.

Nevertheless, three of the largest telephone companies—Plessey Tele-

industry. Points out one industry observer, "Monopolies, like old soldiers, don't die, they just fade away."

In fact, the new bill says little about breaking BT's stranglehold on the communications market. Rather, it grants to the Secretary of State for Industry increased powers to make or break the post office monopoly in the public interest. The real battle will continue as BT and providers of new services seek to influence the minister, Sir Keith Joseph. For example, another lobbying group has emerged in the past few



communications Ltd., GEC Telecommunications Ltd., and TMC Ltd.—are already jointly developing a push-button phone line that is being honed to the bone in cost. Called the Inexpensive Telephone, it could rapidly replace BT's own version that was engineered, say competitors, to lavish "Rolls Royce" standards. Also, Plessey recently introduced a low-cost viewdata telephone [*Electronics*, Dec. 4, p. 84] that it intends to sell directly to the public once demonopolization is a fact.

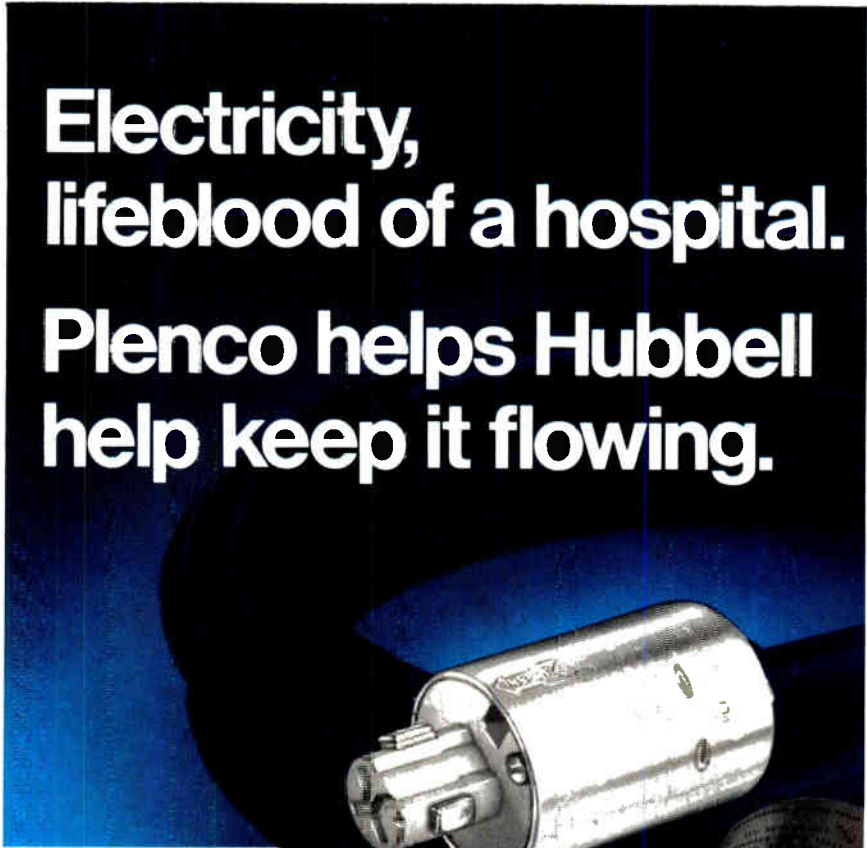
Though Sir Keith took the U. S. as his model for the telecommunications bill, he is moving cautiously with the second of his proposals: to open competition in value-added services such as data-base services, office-of-the-future facilities, interconnections for such equipment as facsimile devices and word processors, and monitoring and relay facilities. He has commissioned a study of likely revenue loss to the post office.

Carriers studied. Finally, Sir Keith is examining the case for allowing the private sector to provide carrier services. For example, he says, "there is a crying need for telex and good digital fast lines," and he is encouraging consortiums to come forward with concrete proposals. In the same vein, Sir Keith is examining the feasibility of wideband satellite links for business communications. However, not only would it be difficult to justify a \$24 million satellite in geographically small England, but a Europe-wide network could snarl the plans of other European postal and telecommunications authorities (PTTs)

Though the British demonopolization bill might fall short of its American model, few doubt that it will present British firms with the opportunity for increased growth and the challenge of foreign competition. However, Tim Johnson, a consultant with Logica Ltd., a software and systems house that has just completed a study of data-communications trends for 17 European PTTs, notes, "Experience shows that where PTTs have adopted a liberal attitude to terminal connection growth has been more rapid." □

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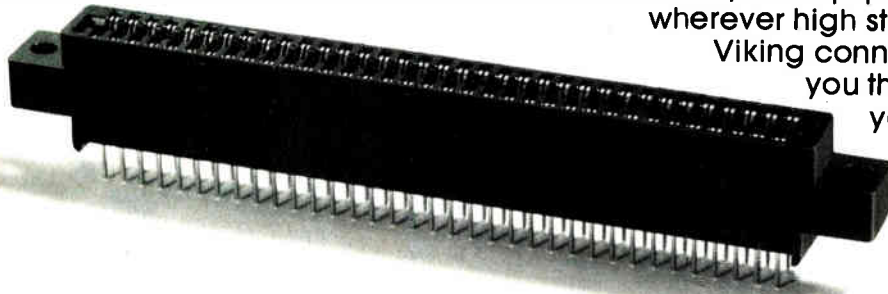
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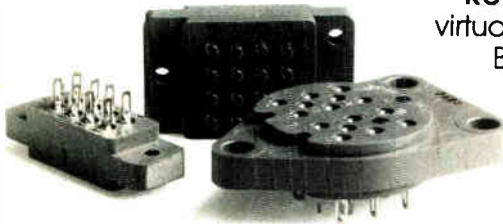
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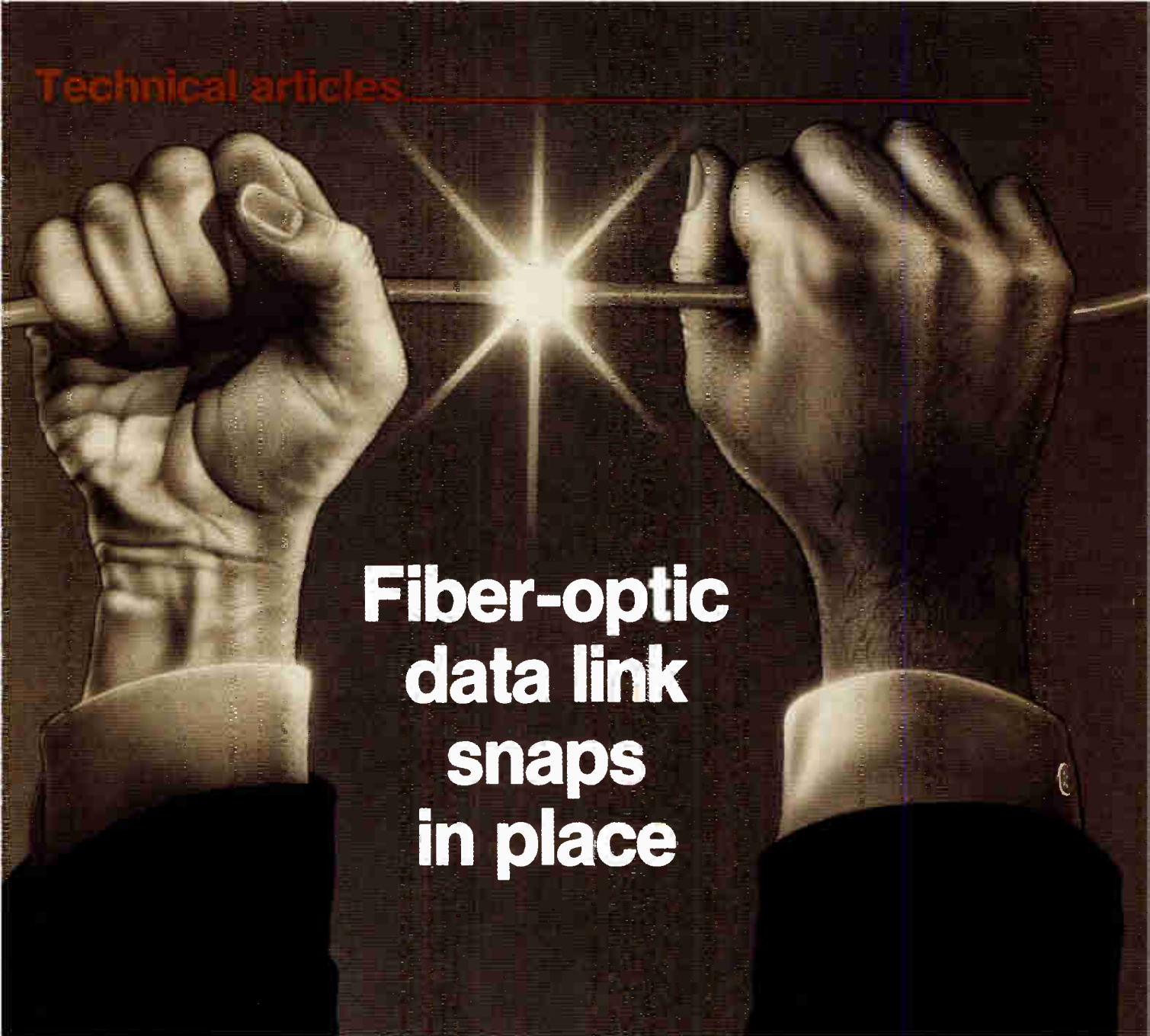
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Fiber-optic data link snaps in place

10-Mb/s transmitting/receiving system's suitability can be quickly determined by link design equations

by Robert Lombaerde, *Optoelectronics Division, Hewlett-Packard Co., Palo Alto, Calif.*

□ A fiber-optic data link offers systems designers three notable benefits: the ability to reduce susceptibility to noise from electromagnetic or radio-frequency interference, to isolate a system from high voltages, and to provide secure data communications. But the cost and complexity of real-life fiber-optic subsystems has limited the application of the technology. A \$55 digital data-transmission link now available, suitable for computer-to-peripheral connections up to 20 meters long, removes these limitations. This "snap-in" fiber-optic link, as it is

called, with a data-rate capacity of dc to 10 megabits per second, combines a quick connection and disconnection scheme with fiber and optical-device technology developed at Hewlett-Packard's Optoelectronics division.

The HFBR-0500 system consists of a fully characterized and specified transmitter module and a TTL-compatible receiver module, along with 5 m of plastic cable fitted with connectors (Fig. 1). To help the potential user decide if the snap-in link can meet his dynamic range and cable length requirements, a unique link



design procedure and instructions suitable for a wide range of practical systems are also included. This procedure is based on simplified design equations, which are in turn based on design graphs made possible by the complete determination of the transmitter diode light output and driving current relationship.

Both the HFBR-1500 and the more-powerful HFBR-1501 transmitter modules contain a 665-nanometer gallium arsenide phosphide light-emitting diode mounted (die-attached) on a copper-alloy lead frame to minimize LED junction temperature and ensure long life. The module also contains a small lens to improve the light coupling into the fiber.

The HFBR-2500 receiver module contains an integrated circuit that combines a photodiode and a TTL-compatible amplifier. In addition, this IC contains an optically transparent, electrically conductive shield over the photodiode and the first few sensitive gain stages. This shield shunts any induced rfi to ground, thus keeping the receiver's noise immunity high.

Before the link design procedure can be appreciated, it is necessary to understand how the link components were designed. It is also useful to show how simple link design parameters may be determined, even by the nonspecialist. The starting point for the link component's design was the parameters of the fiber cable that hooks the transmitter to the receiver.

Pick a fiber

Many low-cost all-plastic fiber-optic cables are available. Until now, they have been used primarily for "light-pipe" applications, that is, where high attenuation per kilometer is of no concern because only a few meters are used. Almost any of these cables may be employed with the HFBR-0500.

After the choice—based on price and delivery—was made, an LED was selected that has an operating wave-

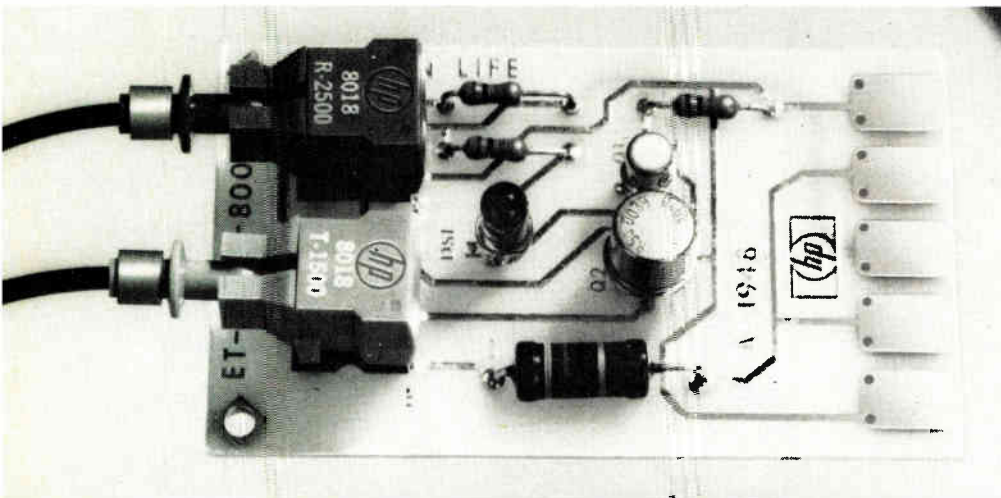
length corresponding to the wavelength at which the optical fiber has its lowest attenuation. To get most of the light into the fiber, the emitting area of the diode was chosen to match the area of the fiber core. Similarly, the detector had to operate at the transmitter diode's wavelength and the detecting area had to match or be larger than the cross-sectional area of the fiber core so as to minimize coupling tolerances. If coupling were too loose, too much light power would miss the detector's sensitive area.

The transmitter and detector diodes and cable chosen for this system are thus all optically matched to each other. Furthermore, they are mounted in plastic color-coded modules. To make interconnection to printed-circuit boards convenient, the electrical leads from the plastic modules are spaced the same as on a standard eight-pin dual in-line package. However, an optical port is fitted in place of pins 6 and 7.

This packaging makes possible a snap-in connection scheme. In this approach, the transmitter and receiver modules have jaws that grip the color-coded cable connectors. Alignment at the connector-module interface is ensured by mating a tapered connector end with a funnel-shaped hole—the jaws—in the module. Thus field installation of fiber-optic links is literally reduced to a simple snap-in. Terminations of fiber-optic cables—usually a time-consuming and frustrating experience—have been made simple and easy, too. After the outer jacket is stripped away, a simple crimp ring holds the cable in the connection. No adhesives are required, alignment tolerances are no problem, and the match of the diode's active area to the fiber core is maximized by the use of lenses molded into the plastic encapsulation.

The transmitter module can be driven by standard logic gates. For long-distance transmission—20 m or so—where more diode drive current is required to obtain higher optical flux output, a standard high-current line driver is needed. Access to both the anode and the cathode pins of the transmitter diode allows the system designer to implement any of these drive configurations—in series or parallel—to optimize system layout or performance.

Series drive circuits for the LED (Fig. 2a) minimize the power-supply current and are recommended for driv-



1. Versatile. Both the transmitter and the receiver of the HFBR-0500 snap-in fiber-optic data link are fitted with standard dual in-line package pins so that they may be directly inserted onto printed-circuit boards. The connectors snap on or off without any alignment problems.



ing more than one of these devices. However, in this design, the drive transistor must be taken into account when calculating the value of the LED's current-limiting resistor. Shunt drive circuits (Fig. 2b), on the other hand, have the advantage of a continuous power-supply current drain, so that less power-supply noise is generated. These circuits can also be used with a lower power-supply voltage and are recommended when driving single LEDs.

The transmitter LED may be driven with standard TTL open-collector drivers, such as the 7407. If more current is required, a 75450 series dual driver can be used. Interfacing with complementary-MOS circuits requires a high current driver with C-MOS-compatible inputs, like National Semiconductor's DS3631N.

Sometimes the shunt drive is preferable for the best possible heat sinking. For example, a heavy internal lead frame serves as a heat sink for the emitting diode, and increased thermal efficiency will be gained when a heat sink area is also provided for pins 2 and 3, the two cathodes of the LED. Here, shunt drive circuits allow the cathode pins to be grounded. Grounding results in increased thermal efficiency of the diode, since the ground plane acts as a heat sink.

The detector IC has an open-collector Schottky output transistor. System designs requiring wired-OR or bus interfaces can easily be directly linked at the receiver's output. If an output pull-up is required, a 1,000-ohm resistor internally tied to the supply voltage is available on chip.

The receiver's broad bandwidth is ideal for use in fast data-transmission systems. Asynchronous data—with the idle state either high or low—can be readily detected and amplified by the dc-coupled amplifier. Dc coupling at the receiver also allows the system to be used in interruptor, or interlock, circuits. In this design, a constant signal level indicates the intrusion status.

Such dc-coupled receiver amplifiers exhibit pulse distortion when overdriven. Therefore, a system design must include an analysis not only of the minimum flux received by the detector for a low error rate or minimum pulse width, but also of the maximum flux that can be received without overdriving the detector.

Receiver modules are used in many harsh emi and rfi

environments, since the fiber-optic cable is a dielectric and neither radiates nor picks up signals. Hence they must be shielded lest their error rates be high. As noted, the HFBR-2500 has a shield protecting the rfi-sensitive front end that provides better than 10 times the emi immunity of unshielded parts.

A preliminary design

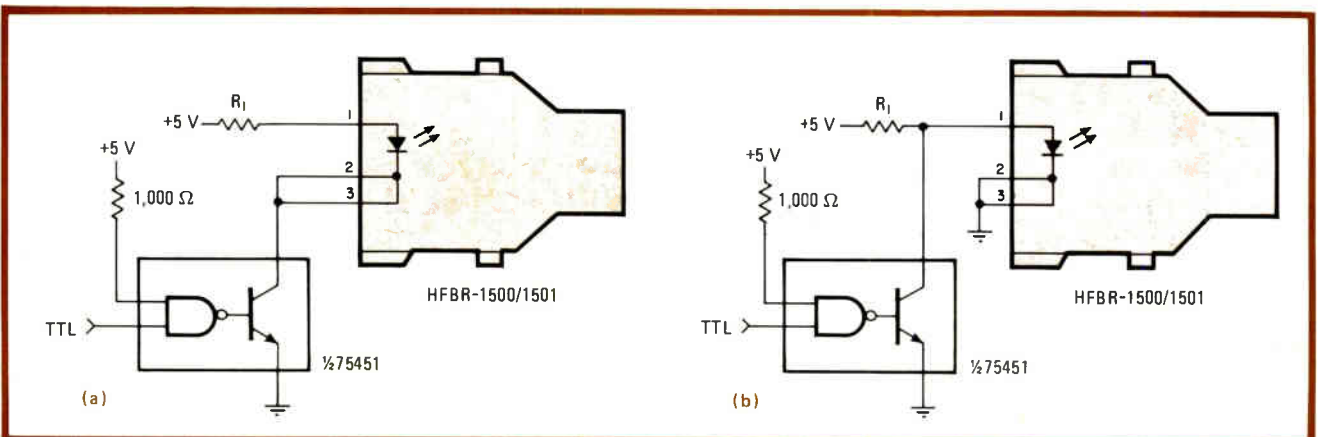
The transmitter, receiver, and cable have been designed to make them applicable to many practical optical data links. To determine the performance in a particular system, a flux budget must be calculated based on the transmitter's output flux, the receiver's sensitivity, and the losses of the interconnecting elements. When actual flux measurements are required as data for this flux budget, they are readily made (see "Measuring the optical flux," p. 87).

As with all receiver systems, to operate satisfactorily the total fiber system loss must not exceed the difference between the transmitter's output flux and the receiver's input sensitivity. This value is called the flux ratio. The difference between the flux ratio and the system loss is known as the system flux margin. For a system to operate satisfactorily, this parameter should be greater than 0 decibels. Expressed mathematically, the flux margin is:

$$\alpha_M = \alpha_{FR} - \alpha_{SL}$$

where α_M is the flux margin (dB); α_{FR} is the flux ratio (dB), which equals the transmitter's output flux, Φ_T (dBm), minus the receiver's input sensitivity, Φ_R (dBm); and α_{SL} is the system loss (dB), which equals the sum of the cable loss, the splice loss, the connection loss, and the interface loss.

The flux margin calculation also determines the dynamic range of the fiber system. To calculate this range, the flux margin, α_{M1} , is first calculated for the



2. Two choices. At the designer's discretion, either the series drive (a) or the shunt drive (b) may be used for the transmitter's LED. The choice depends on the characteristics of the transmitter used and is fully explained in the design information included with the data link.



maximum flux ratio, $\alpha_{FR(max)}$, and the minimum system loss, $\alpha_{SL(min)}$. Then, another calculation of the flux margin, α_{M2} , is made based on the minimum flux ratio, $\alpha_{FR(min)}$, expected and the maximum system loss, $\alpha_{SL(max)}$. Finally, the second flux margin is subtracted from the result of the first flux margin calculation. The difference

is the expected dynamic range of the receiver:

$$\begin{aligned} \alpha_{M1} &= \alpha_{FR(max)} - \alpha_{SL(min)} \\ \alpha_{M2} &= \alpha_{FR(min)} - \alpha_{SL(max)} \\ \text{dynamic range} &= \alpha_{M1} - \alpha_{M2} \end{aligned}$$

By changing the flux budget equations to subtract the losses due to intermediate components like cables or connectors from the transmitter's output flux, a calculation can be made of the amount of flux at the end of the cable. This is equivalent to the amount of flux into the receiver, or:

$$\Phi_T - \alpha_{SL} = \Phi_L \quad (1)$$

where Φ_L is the flux at end of cable (dBm), Φ_T is the transmitter's output flux (dBm), and α_{SL} is the sum of the intermediate losses (dB).

The flux budget equation when the snap-in fiber-optic link is used with HFBR-3500 cable is similar to Eq. 1. In this case, however, the system's intermediate loss has only one term—the cable attenuation. Thus:

$$\Phi_T - (\alpha_0 L) = \Phi_R \quad (2)$$

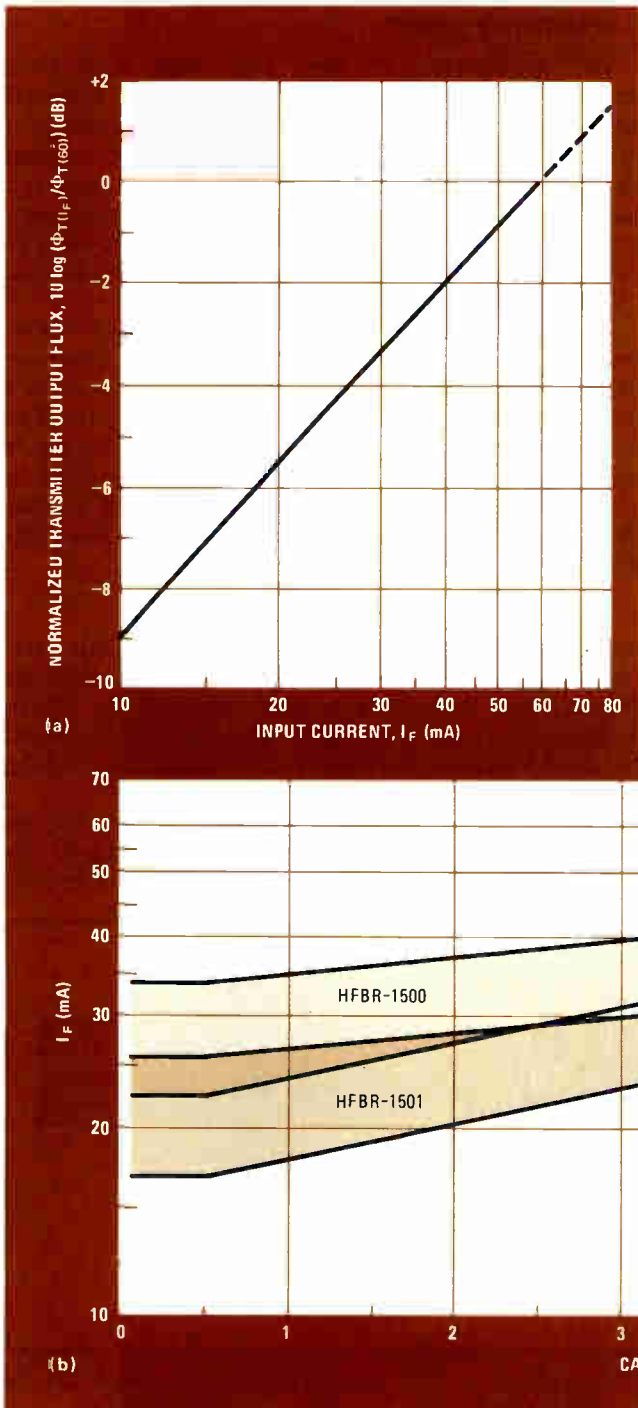
where α_0 is the cable attenuation per unit length (dB/m), L is the cable length (m), and Φ_R is the receiver's input optical flux sensitivity (dBm)

To derive the worst-case drive current for a 5-m cable—a typical case—the minimum and maximum specifications are substituted in Eq. 2 with the overall length decreased by 0.5 m, since stubs of this length are usually connected to both the transmitter and the receiver. Therefore:

$$\Phi_{T(max)} - \alpha_{0(min)}(L - 0.5) = \Phi_{R(max)} \quad (3)$$

$$\Phi_{T(min)} - \alpha_{0(max)}(L - 0.5) = \Phi_{R(min)} \quad (4)$$

3. Work savers. Many calculations are eliminated by a graph showing the LED output flux as a function of its drive current (a). A graph correlating this drive current with length link in a worst-case analysis (b) is also useful and is a great help to the nonexpert.





If Eq. 3 is satisfied, the receiver will not be overloaded. On the other hand Eq. 4 ensures enough flux at the receiver. For a system to operate properly, both equations must be satisfied.

The transmitter's drive current, I_r , is determined from the needed output flux (Fig. 3a). After this current is determined for any particular situation, it is used in the graph of Eqs. 3 and 4 in Fig. 3b. The drive current range at a particular cable length or the cable length range for a specific drive current under worst-case conditions can easily be determined.

It is important to realize that in some designs intermediate connectors, bulkhead interfaces, or splices are needed. For example, applications in which the fiber-optic modules are to be completely enclosed in a shielded box require the use of bulkhead-type connectors. These are available from AMP, as are connectors for the HFBR-3500 fiber.

A practical design

The flux budget must account for all losses in the optical transmission path. Consequently, an optical measurement may be required to determine the actual loss due to intermediate connectors.

If all the flux losses are known, the equations and graphs developed earlier are sufficient to determine the feasibility of a preliminary link design. Consider, for example, the maximum flux output of a transmitter in a 4-m link with one intermediate connector (assuming an insertion loss, α_{CC} , of 1.4 dB). The transmitter's maximum output is calculated using Eqs. 3 and 4, but the extra system loss of α_{CC} must be included. The general equation used is:

$$\Phi_T - \alpha_{CC} - \alpha_0(L - 0.5) = \Phi_R$$

Thus in this example:

$$\begin{aligned} \Phi_{T(\max)} &= \Phi_{R(\max)} + \alpha_{CC} + \alpha_{0(\min)}(4 - 0.5) \\ &= -12.5 + 1.5 + (0.3 \times 3.5) \\ &= -9.95 \text{ dBm} \end{aligned}$$

Similarly:

$$\begin{aligned} \Phi_{T(\min)} &= \Phi_{R(\min)} + \alpha_{CC} + \alpha_{0(\max)}(4 - 0.5) \\ &= -21.0 + 1.5 + (0.63 \times 3.5) = -17.3 \text{ dBm} \end{aligned}$$

Since $\Phi_{T(\max)}$ is greater than $\Phi_{T(\min)}$, the input current must be reduced from 60 milliamperes when the HFBR-

1501 is used, in order to limit the transmitter's maximum output flux to -9.95 dBm from the data sheet maximum of -8.4 dBm. The 1.55-dB reduction occurs at 44 mA (Fig. 3a).

To determine the minimum flux drive current, the $\Phi_{T(\min)}$ of -17.3 dBm is subtracted from the data sheet

Measuring the optical flux

The optical flux at the end of the HFBR-3500 series fiber-optic cable can be measured using a radiometer such as the EG&G-550, the Photodyne 88XL, or the United Detector Technology S550. Calibration should be done at 665 nanometers.

The output flux for the HFBR-1500/1501 transmitters is specified at the end of 0.5 meter of HFBR-3500 fiber-optic cable and can be measured using one of the above-mentioned instruments with a large-area detector. Similarly, the HFBR-2500 receiver's dc sensitivity may be measured by first adjusting the flux into a receiver until the output switches, then removing the receiver and determining the flux emerging from the cable end.

Usable flux range measurements can be made by determining the flux at the end of a cable when a receiver has the maximum acceptable pulse distortion due to insufficient flux and when the maximum acceptable pulse distortion is due to overdrive conditions. The difference in these two readings is the ac dynamic range of the receiver.

Cable loss measurements can be made by first determining the transmitter output flux through 0.5 m of cable. Then the flux emitted at the end of the longer cable under test is measured when the cable is plugged into the transmitter. The ratio of the two flux readings approximates the loss in the cable. This figure is close to the actual cable loss. It is not exact because of different coupling efficiencies between the 0.5-m cable and the cable under test to the transmitter. In most cases, this difference is no problem.

FIBER OPTIC CABLE CHARACTERISTICS

	Retractive index profile, α_l	Core diameter, D (mm)	Numerical aperture, NA	First splice			Length attenuation, α_0 (dB/m)	Second splice			Total insertion loss, α_{CC} (dB)
				Index mismatch, α_l (dB)	Diameter mismatch, α_A (dB)	NA mismatch, α_{NA} (dB)		Index mismatch, α_l (dB)	Diameter mismatch, α_A (dB)	NA mismatch, α_{NA} (dB)	
HFBR-3500	100	1,000	0.5	0	0	0	0.4	0	0	0	0
Galite-2000	100	1,140	0.66	-	-	-	0.7	0	1.1	2.4	3.5
Du Pont PIR-140	100	368	0.5	0	8.7	0	0.25	-	-	-	8.7
Belden 221001	100	300	0.22	0	10.5	7.1	0.012	-	-	-	17.6
Du Pont S120	100	200	0.42	0	14.0	1.5	0.035	-	-	-	15.5
Maxlite MSC 200A	100	200	0.4	0	14.0	2.0	0.01	-	-	-	16.0
Hewlett-Packard HFBR-3200	10	100	0.3	0.71	20.0	4.4	0.022	-	-	-	24.4



minimum of -14.8 dBm, yielding -2.5 dB. In other words, the transmitter's output flux must be lowered 2.5 dB, and that is accomplished by using a drive current of 35 mA instead of 60 mA (Fig. 3a).

All these calculations mean that, at 4 m with one intermediate connector having an insertion loss of 1.5 dB, the worst-case current can range from 34 to 44 mA when the HFBR-1501 and HFBR-2500 are used.

Another method of determining the input current graphically is first to find the current range for 4 m (Fig. 3b), then use Fig. 3a to determine what current is required for a 1.5-dB increase in optical flux to account for the 1.5-dB connector loss.

Other cables

System design may at times require the use of another type of fiber-optic cable as the main transmission link, with the HFBR-3500 cables acting as stubs. Any significant parameter difference between the two cables can cause high insertion loss at the interfaces. The flux budget calculation for this case is somewhat different from what has already been presented.

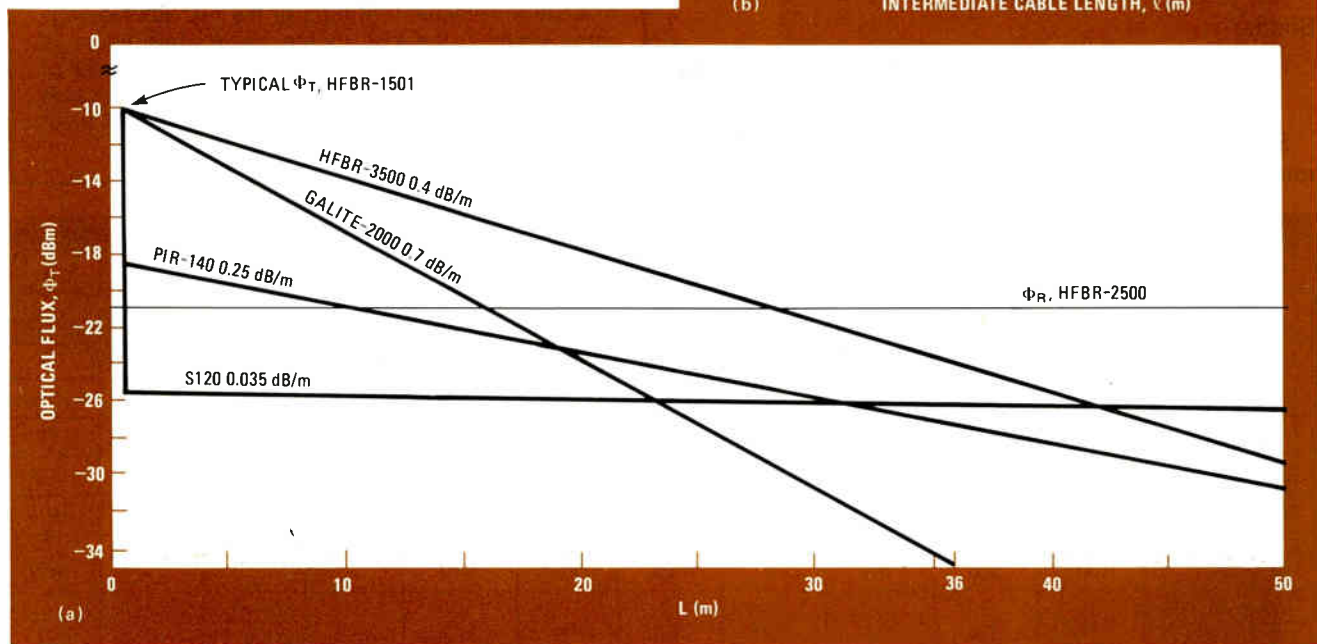
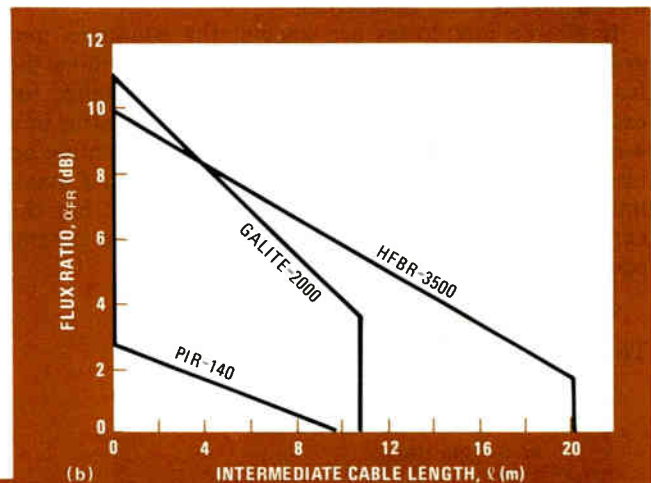
A listing of the interface and cable losses of several commonly used fiber-optic cables is employed to determine their suitability as intermediate fiber-optic links (see table). The losses at the interfaces with these fibers are due to several factors. These are refractive index

4. Typical design. Link design is facilitated by a knowledge of how the transmitter's output flux varies with the attenuation of any intermediate cable needed to hook the transmitter to the receiver (a). The system flux ratio (b) is also a function of this intermediate length.

profile mismatch, α_1 (dB), which is defined as $10 \log[(1 + 2/\alpha_2)/(1 + 2/\alpha_1)]$, where α_1 and α_2 are the refractive index profiles of fibers No. 1 and 2, respectively; area mismatch, α_{1A} (dB), which is defined as $20 \log(D_1/D_2)$, where D_1 and D_2 are the respective fiber diameters; and numerical aperture mismatch, α_{NA} (dB), which is given as $20 \log(NA_1/NA_2)$, where NA_1 and NA_2 are the respective fibers' numerical aperture.

The calculated insertion loss of a fiber connection in the cable includes only the losses caused by refractive index profile, diameter, and numerical aperture mismatching. When connectors are used to splice identical cables, account must be taken of the connector loss that is due to fiber misalignment by the connector; this loss is typically 1 to 3 dB. When interfacing fibers of different diameters, the losses are due mostly to area mismatching and the tolerances on the connectors are not critical. In the typical system design described here, the HFBR-3500 stubs are each 0.5 m long. In systems where the stubs are longer—at the choice of the designer—the additional HFBR-3500 fiber loss must be included.

As stated earlier, the total insertion loss is the sum of all the losses due to cable mismatch at the interfaces.



These numbers are used to calculate the maximum length of a specific cable that can be placed between the transmitter and receiver modules. Since only typical numbers are available for most of the optical-fiber cables, typical specifications will be used for the transmitter module rather than worst-case minimum and maximum specifications.



Intermediate links

If non-HP cables are used as an intermediate link and the HFBR-3500 cables as stubs, the extra interface losses at the intermediate connectors must also be included in the calculations (Fig. 4a). As before, the total insertion loss must be less than the available flux ratio for the system to operate. For example, suppose that one typical system flux ratio using the HFBR-1501 transmitter was calculated as 11.1 dB. As illustrations, consider three possible intermediate cables (Fig. 4b).

The Du Pont PIR-140 cable has less attenuation than the HFBR-3500. A typical transmission distance is calculated from the flux budget. As the flux margin is equal to the flux ratio minus the sum of the losses:

$$\alpha_M = \alpha_{FR} - (\alpha_{SL} + \alpha_0 L)$$

where:

α_{SL} = total insertion loss (dB)

α_0 = cable attenuation per unit length (dB/m)

α_{FR} = flux ratio (dB)

L = cable length (m)

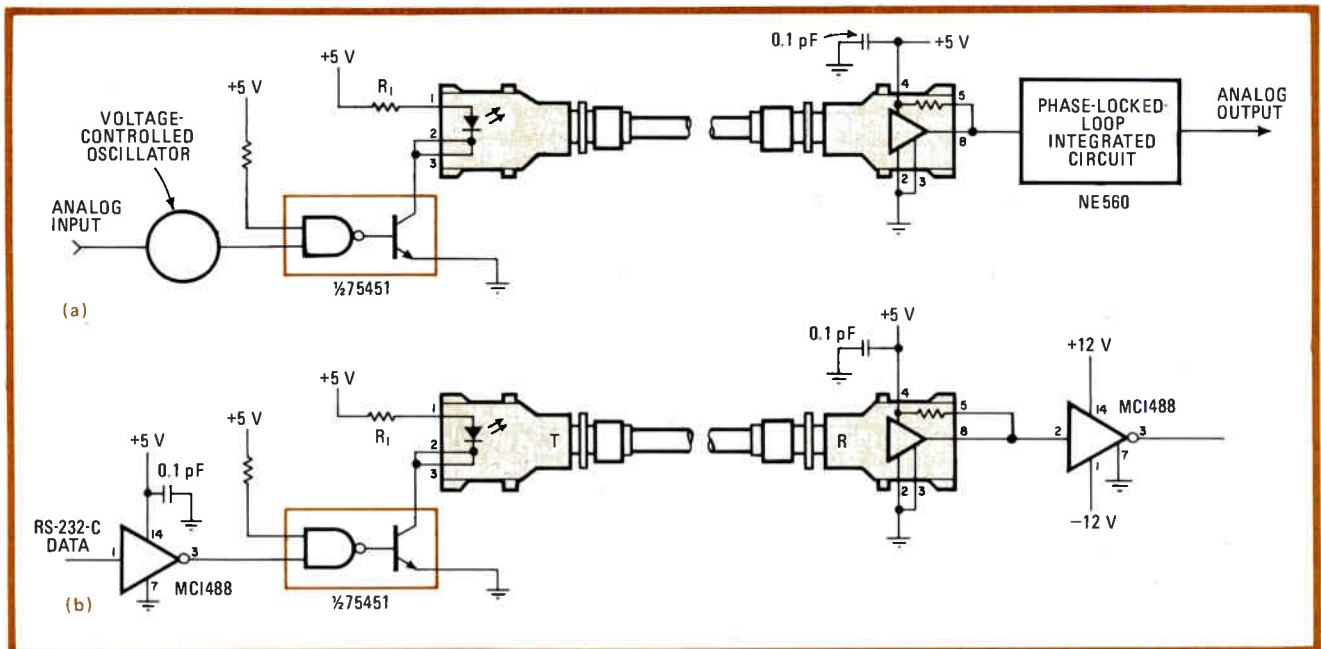
A typical cable length (assuming an α_{FR} of 11.1 dB) is $L = (\alpha_{FR} - \alpha_{SL}) / \alpha_0$. For the PIR-140 cable, $L = (11.1 - 8.7) / 0.25 = 9.6$ m. Using the same equations, the transmission distance for a Galite 2000 cable comes out to 10.9 m. Again using the same equations, the cable length for the HFBR-3500 may be calculated assuming an α_{CC} for two AMP connectors of 1.5 dB per splice. A typical length is $L = (11.1 - 3.0) / 0.4 = 20.3$ m.

The overall link length is limited by the dynamic range of the receiver. Consequently, since the transmitters have a large output flux, the input current must be reduced to prevent the receiver from overloading, which occurs for any flux greater than the data sheet input maximum of -12.5 dBm. When overdriven, the decoupled receiver exhibits pulse distortion. Furthermore, because of the amplifier peaking used to obtain a fast response, the receiver may produce an extra pulse or glitch from the overshoot.

Overdriven receiver

The data sheet specifications guard against overdriving the receiver by placing limits on the amount of input flux. However, other techniques can be used to drive the HFBR-2500 above the data sheet limits so that extra pulses or glitches are not produced. In reality, the overshoot always occurs on the low-to-high-pulse transition and can readily be eliminated from the link in low-speed systems.

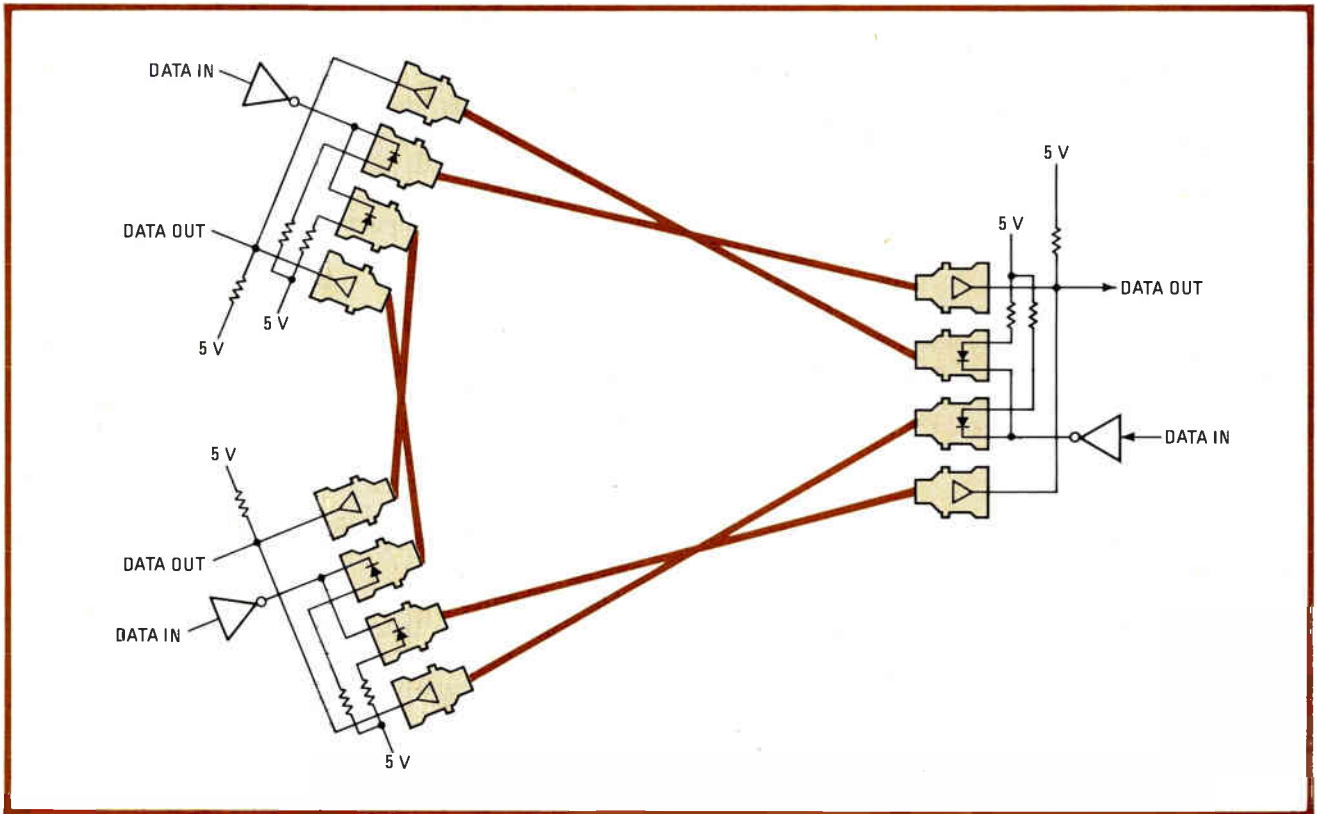
One technique is to increase the fall time of the input optical flux to the receiver. Placing a 1,500-picofarad capacitor across the LED in the HFBR-1500 or -1501 transmitter increases the transition of the receiver's output from low to high by 150 nanoseconds. Because of this increase, the link now has very asymmetrical propagation delays and should only be used in low-data-rate systems. In these systems, the propagation delay is a small percentage of the bit interval and is of no consequence. Moreover, under these conditions the maximum



5. Variations abound. The snap-in link can be hooked up as an analog transmission system (a) or as an RS-232-C data interface (b). The link is not limited to these configurations; other interface specifications such as the RS-488 may be satisfied by the use of auxiliary logic gates.



6. Combinations. It is also possible to hook up the snap-in data link to simultaneously connect three or more data generators and receivers. Here, multiple series-driven transmitters and wired-OR receivers are fiber-linked to construct a fully connected three-node data network. Other configurations with four or more nodes may be designed to satisfy RS-232-C and similar interface standards.



input flux to the HFBR-2500 receiver is not the limiting factor in the link design. Thus the system limiting factor is simply the receiver's input sensitivity.

The specification for the HFBR-1500/1501 has a worst-case flux variation of 6.4 dB to account for process variations, sorting tolerances, temperature effects, and coupling variations. When the link performance of any receiver is calculated, these tolerance variations and the dynamic range of each component are added to define the worst-case transmission distance. Although most tolerance variations are determined by processing and manufacturing limits, some variations such as temperature effects can be minimized by circuit design.

Temperature effects

Temperature effects account for greater than 2 dB, or one third of the transmitter's output flux variation, as typical experimental data shows. Receiver and cable variation with temperature is minimal, since these components are relatively temperature-insensitive. For the transmitter, a temperature-compensated drive circuit is used to reduce its output optical flux variation over temperature from 2 to 0.5 dB, increasing the worst-case transmission length by 1.5 dB/0.33 dB/m, or 4.5 m. There are several practical schemes for implementing a temperature-compensated drive circuit.

Frequently, an analog signal must be transmitted over a digital fiber-optic link. For low-bandwidth analog transmissions, a design scheme utilizing a voltage-controlled oscillator with a TTL-compatible output level (the 74S124, for example) can be used to modulate the transmitter LED. The analog data thus generated may be recovered with a discriminator or a TTL-compatible phase-locked-loop IC (Fig. 5a) such as the NE560. Using frequency modulation for analog transmission instead of pulse-position or pulse-width modulation eliminated any effects due to pulse-width distortion at the receiver.

Communication level interfaces such as the Electronic Industries Association RS-232-C or RS-422 recommended standard can easily be interfaced with the digital fiber-optic link using standard interface chips. The data interface at the electrical level also is easy to handle (Fig. 5b). Any handshaking signals required for communication exchange should follow the RS-232-C or RS-449 specification.

This link can also be used for other applications besides those involving simple digital or analog transmission. For example, networks utilizing multiple driven transmitters or wire-ORed receivers are often seen in systems for data interchange. Circuits for such multiple links can be readily implemented with the snap-in link (Fig. 6). □

Tough control tasks take 16 bits

The 9995 adds off-chip memory to extend the capabilities of the first single-chip 16-bit microcomputer

by John V. Schabowski, *Texas Instruments Inc., Houston, Texas*

□ High speed and high resolution are not usually associated with single-chip microcomputers. Four-bit chips, for all their popularity, have minimal computational power, and 8-bit devices cannot comfortably handle larger than byte-sized data types or offer more than moderate data processing within the time constraints of real-time operation.

The TMS9940 16-bit microcomputer [*Electronics*, June 23, 1977, p. 113] was the first to transcend those limitations. It can perform complex mathematical computations on data representing physical parameters that demand greater than 8-bit resolution, and it can do so at high speed. Also, since its instructions perform many more operations, it uses much shorter programs. Table 1 compares its principal applications with those of its predecessors.

The 9995 adds the ability to address up to 64-K bytes of off-chip memory to the 9940 (Fig. 1), which incorporates both data and program memory on chip and allows no external memory references whatsoever. The 9995, however, always locates its programs off chip since it has no read-only memory. The 9940's lack of external memory limits the number of applications the simple, small systems based on it can serve, but it is a big step up to the much larger and more complex systems based on the 9900 microprocessor. The 9995 fills that gap, since the addition of the memory chip or chips it needs yields a far from complex system.

Both the 9940

and the 9995 provide 16-bit power with on-chip random-access memory. The 9940 offers 128 bytes of RAM, while the 9995 provides 256 bytes, which are addressed as 128 words. In addition, both these devices are compatible with 9900 software and development systems.

Some comparisons

The 9940 also provides 2,048 bytes of nonvolatile program memory—either as mask-programmable ROM (9940M) or as user-programmable erasable PROM (9940E). The 9995 accesses its off-chip program memory a byte at a time through an 8-bit memory interface (Fig. 2). But it can access full 16-bit words from its internal RAM in a single cycle, making those locations ideal for workspace registers

As in all processors in the 9900 family, the operand registers are located in general memory, a method that can decrease throughput when slower external memory is used for register storage (see "How the 9995 shrinks chip and program size," p. 93). However, when the register file is located in the high-speed on-chip RAM,

this penalty disappears, since these locations can be accessed just as quickly as the dedicated registers of other processors. In addition, the 128-word on-chip RAM can act as eight separate files of 16 high-speed registers, whereas only a single register file is supplied with most other 8- and 16-bit processors. The on-chip RAM can also store programs.

The 9995 includes several

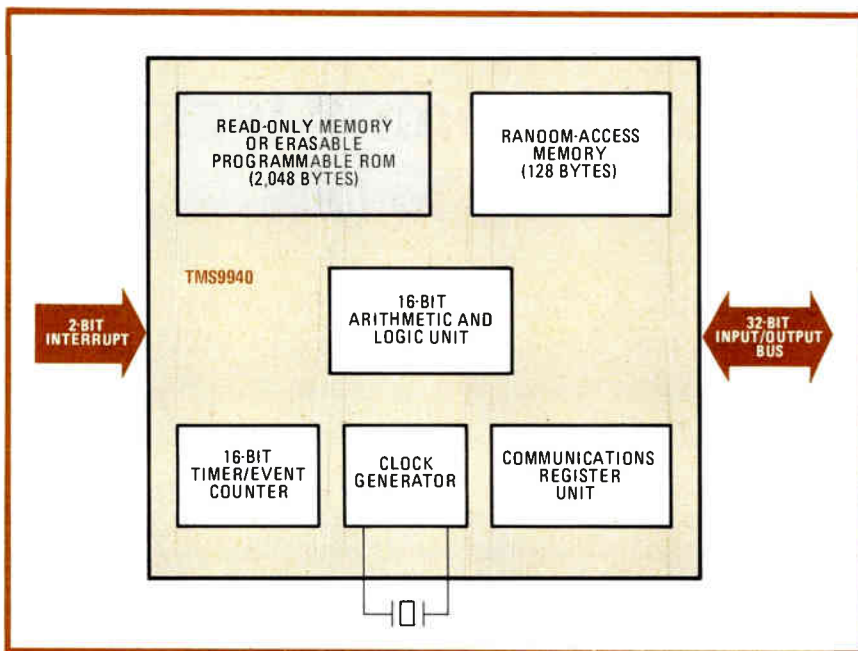
TABLE 1: TYPICAL APPLICATIONS OF SINGLE CHIP MICROCOMPUTERS HAVING VARIOUS WORD LENGTHS

Internal word width	Typical data type	Typical tasks	Relative level of performance required	Typical applications
4 bits	binary-coded decimal digits	simple sequencing and control	low	games, calculators, appliances
8 bits	alpha-numeric characters; bytes	sequencing and device control, simple data processing	medium	simple machine controls, computer peripherals, terminals
16 bits	physical-parameter values; analog-to-digital converter outputs	closed-loop control, complex arithmetic computations, data processing	high	industrial, process and vehicular controls, smart instruments, intelligent peripherals, terminals controllers, communications equipment

architectural refinements in addition to the capability of addressing off-chip memory. One of these enables it to determine the speed of its external memory at power-up. It can work with memories that have 120-nano-second access times and 330-ns cycle times with no wait states. But it also can accommodate less expensive, slower memories by automatically generating a wait state that lengthens the

normal memory transactions. At power-up it determines the speed of the memory by interrogating the logic level at one of its pins. If a slow memory is indicated, then it inserts a wait state during every subsequent memory cycle, thus accommodating external memory with 450-ns access times and 667-ns cycle times.

Another advanced feature, otherwise found only on sophisticated processors like Motorola's 68000, is the ability to use undefined operation codes for macro-operations—user-supplied subroutines that do not require the customary address operand but are instead called by a single-word instruction. Whenever it detects such an instruction, or op code, the 9995 vectors to a known memory location where the user-supplied subroutine resides. This feature is termed the macroinstruction-detect (MID) mechanism and is a form of the extended-operation (XOP) instruction resident in all 9900 family processors. With

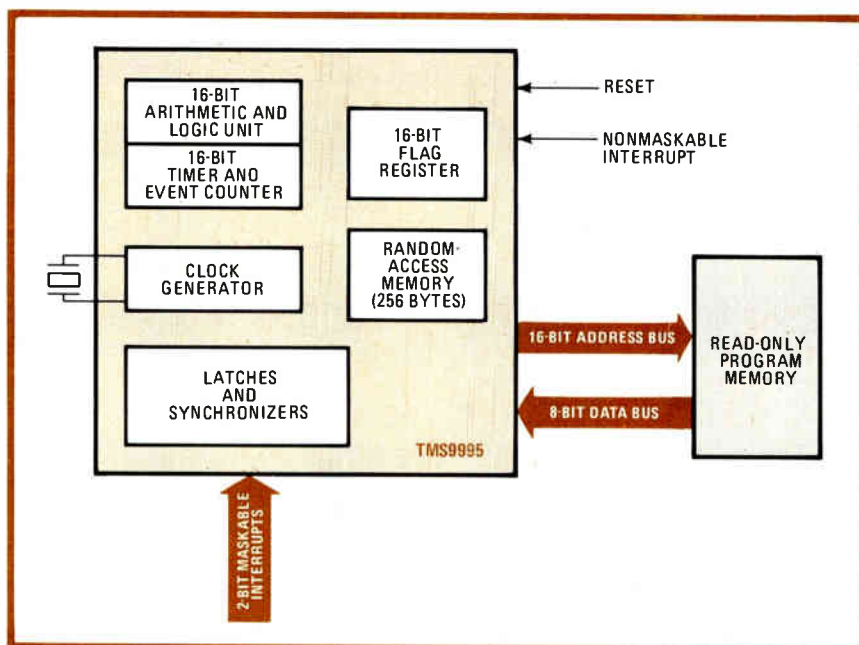


1. **The first.** The TMS 9940 is the first 16-bit single-chip microcomputer ever produced. It contains 2-K bytes of read-only memory, 128 bytes of random-access memory, a timer/event counter, and 32 discrete lines for input and output.

er an arithmetic overflow is detected. This ability saves the execution time and memory space of the software checks that otherwise would have to accompany arithmetic operations.

Another speed-enhancing feature of the 9995 is its ability to prefetch the next instruction from external memory while the processor is executing the present one, a feature found in only one other 16-bit family, Intel's 8088 (Table 2). When the processor is executing an instruction, the memory interface is normally free, so that the next instruction fetch can be started without

interfering with any operations already in progress. When executing an instruction whose operands are located in the on-chip RAM, the prefetch can be completed before the previous program step has finished executing; then while the prefetched instruction is decoded, the results of the previous one are stored. The net result is increased processing overlap—often called pipe-



2. **ROM-less.** The 9995 allows up to 64-K bytes of off-chip memory to supplement the 256 bytes of random-access memory it has on chip.

How the 9995 shrinks chip and program size

Two architectural features distinguish the 9995 from other processors. Its working registers are held in random-access memory, and it uses a two-address instruction format—the addresses of both the source and destination operands are specified by each two-operand instruction.

The first feature saves valuable die area by locating workspace registers off chip. This is accomplished by including a workspace-pointer register on chip that indicates where in memory the 16 contiguous workspace registers are located.

Access to workspace registers is much slower when a time-consuming round trip must be made from the processor to an off-chip memory containing them. However, context changes are quick since an interrupt needs only to replace the workspace-pointer register to get a fresh set. Processors using dedicated internal registers face the opposite problem. They have faster access to their registers, but respond to context changes much more slowly because they must first save the contents of the current registers before switching contexts.

With the 9995, the best of both worlds can be had now that the workspace registers may be located in the on-chip high-speed RAM. Since the time difference between on-chip RAM and dedicated register is quite negligible, fast register access is now combined with fast context switching.

The second distinctive architectural feature of the 9900 family processors is their two-address operation-code format. On these processors there is no dedicated accumulator serving as the assumed destination of all two-operand instructions, as is the case on all other microprocessors—they use what is called a one-address architecture, since the second operand is always assumed to be the dedicated accumulator. On 9900 family devices any workspace registers can serve as accumulators. For instance, consider the compiler output of the Pascal instruction:

$I = I + J$

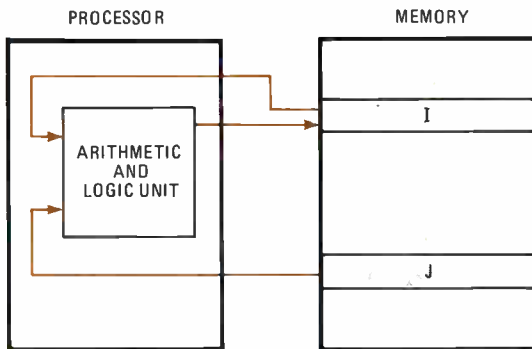
The 9900 Pascal compiler can translate this instruction into a single assembly language statement: `ADD J,I`. This is because any memory location can serve as either destination or source operand. But processors using a one-address architecture must use two instructions to accomplish the same goal. The two instructions would be:

```
MOV J,R      (move the J operand into an internal
              register, R)
ADD R,I      (add R, containing J, to I and put the
              result where I was)
```

In this way high-level language compilers have a much easier job of assigning locations to variables and produce shorter object-code modules.

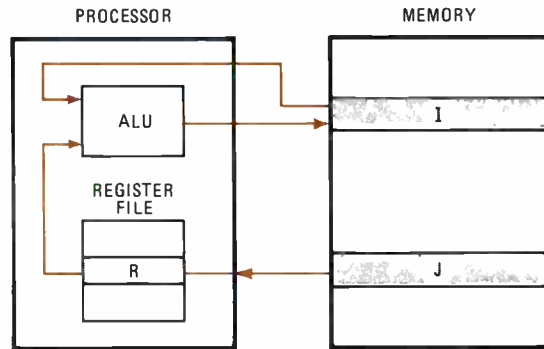
PASCAL STATEMENT $I = I + J$

MEMORY-TO-MEMORY ARCHITECTURE



COMPILER-GENERATED CODE:
`ADD J,I`

REGISTER-TYPE ARCHITECTURE



COMPILER-GENERATED CODE:
`MOV J,R`
`ADD R,I`

lining—that in essence eliminates the time required by two out of the six steps in a normal two-operand instruction execution sequence. In this way the extra time required to fetch instructions from external memory a byte at a time can be largely canceled out.

New and faster instructions

On the performance side of the ledger, the 9995 offers execution that is nearly three times as fast as that of the 9900. This is due not only to the pipelined architectural improvement and the 6-megahertz clock, but also to several refinements in the microcode that defines the steps taken to execute an instruction.

The instruction set of the 9995 also includes four new

instructions that provide greater power than the 9900 in applications that need fast 16-bit arithmetic capability. Two of the new instructions are a signed multiply and divide: the former executes in a mere 8.33 microseconds, whereas the latter needs only 11.0 μ s. The unsigned operations are correspondingly faster: 7.67 and 9.3 μ s for multiplying and dividing, respectively. The same operations on a 9900 microprocessor would take 17.33 and 41.33 μ s, respectively.

The other two new instructions are load-workspace pointer (LWP) and load-status register (LSR) from a variable. Multiple steps are needed on the 9900 to load from a variable. Consequently, the 9995's context switching, which is already fast since register contents

TABLE 2: COMPARATIVE CONTROL APPLICATION EXECUTION SPEEDS FOR THE 9995 AND 8088 MICROPROCESSORS

System configuration		Automated parts inspection (s)	Computer graphics X-Y transformation (s)	Bubble sort (ms)	Block translation (ms)
9995 (6 MHz) having workspace registers in on-chip random-access memory	with 120-ns programmable read-only memory	0.666	0.863	1.240	1.767
	with 450-ns erasable PROM	0.950	1.081	1.956	2.696
8088 (5 MHz) using dedicated registers	with 450-ns E-PROM	1.596	2.402	2.254	1.522

never need to be stored, tends to become even speedier. The instructions allow a program to adjust its processing context conveniently at run time: LWP dynamically allocates workspace register sets, and LST defines status parameters on the fly.

To further help keep a system's chip count low, the 9995 provides on-chip synchronization and latch circuitry for the two maskable external interrupt lines. This allows the 9995 to accept interrupt requests that are truly asynchronous and either levels or pulses.

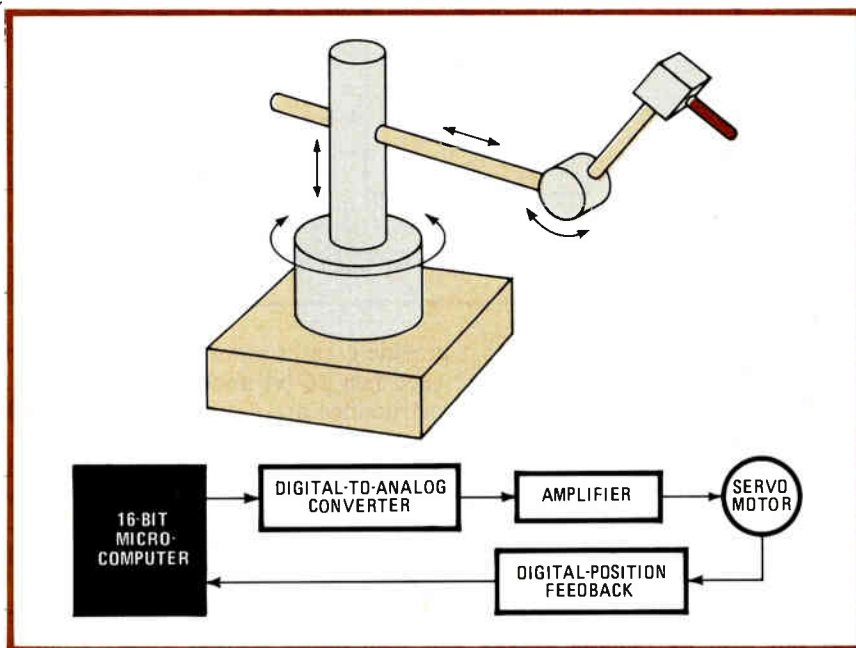
In addition to improvements in the chip's memory and processor sections, input/output—the third major section of any microcomputer—has had its share of enhancement also. The communications register unit (CRU) has been enlarged to address 32 K of serial I/O instead of the 4-K limit imposed on other 9900 family members. Another feature allows the bit-addressable CRU instructions to access a new 16-bit flag register. Three of these flags are dedicated to checking for inter-

rupt requests that the interrupt mask in the status register may otherwise block. With these bits, the program can dynamically reassign the priorities of its interrupt structure. Two more bits from the register control the operation of the on-chip 16-bit timer: one activates it, and the other determines whether it will act as an event counter or an interval timer. The remaining 11 bits are user-definable and are normally used as software flags.

The memory interface of the 9995 uses separate data and address pins, the latter being 16 bits wide. The 9995 has on-chip clock generation as well and is housed in a 40-pin package that requires only a single 5-volt supply.

In the appropriate applications, both the 9940 and the 9995 can lead to minimum-chip-count, software-efficient designs. Obviously, when the 9940 can handle a 16-bit job, it is the preferred solution. For example, the 9940 is quite capable of handling data communications with remote sites using a single protocol. The 9995 extends the range of applications to those requiring more memory—for example, one where several communications protocols must be handled so that the 2-K bytes of program ROM on the 9940 is not sufficient. Simply stated, solutions requiring more code than the 9940 can accommodate may migrate painlessly to 9995 systems.

A spot-welding application is illustrated by the robot arm in Fig. 3. Here, four separately controlled motions place the spot welder on the arm's tip at a point on a three-dimensional workpiece. A separate loop, closed by the microcontroller, controls each motion (only one loop is shown). The 16-bit resolution of the microcomputer represents rotational motion to an accuracy within 1% of a degree or translational motion to an accuracy within 0.001 inch over a 36-in. span. To provide the same resolution, an 8-bit processor would have to call on multiprecision arithmetic requiring many more instructions. □



3. Robot control. A 9995 microcontroller is capable of running this robot welder. Each of the four possible movement axes is controlled by a separate feedback loop consisting of a digital-to-analog converter whose amplified output runs a motor with position feedback.

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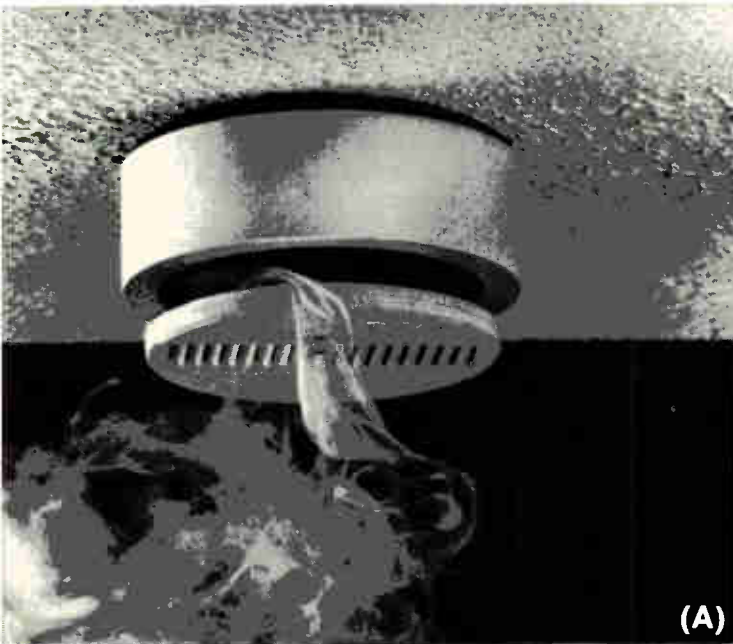
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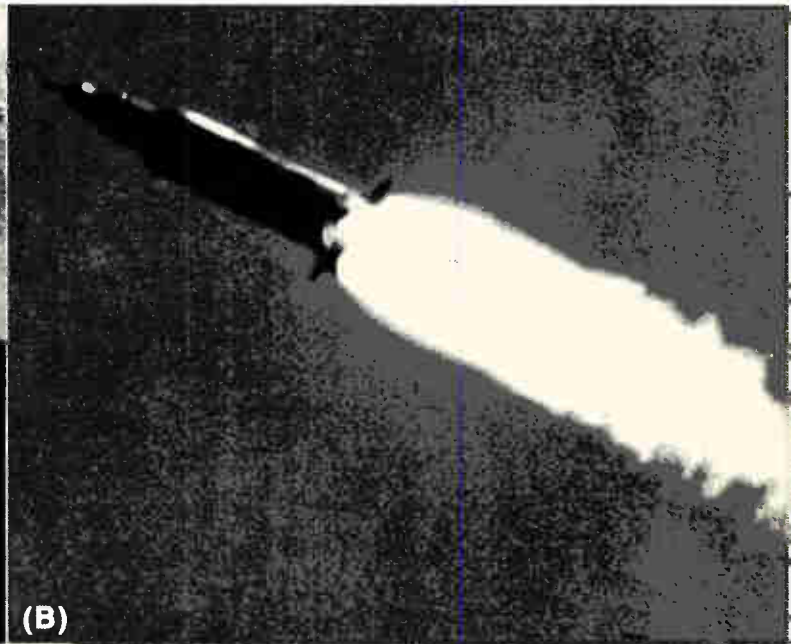
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(A) (B)



(C) (D)



RCA

One-chip tachometer simplifies motor controller

by Henrique Sarmiento Malvar
 Department of Electrical Engineering, University of Brazilia, Brazil

Setting and stabilizing the angular velocity of a dc motor by means of a charge pump and a servoamplifier, one-chip tachometers such as National Semiconductor's LM2917 serve well as a simple but elegant motor-speed controller. Such an arrangement is preferable to the widely used scheme in which both positive and negative feedback is utilized to keep the motor's back electromotive force, and thus its speed, constant by generating a voltage that is proportional to a given load.

As shown in the figure, a magnetic pickup coil detects the angular velocity of a motor-driven flywheel and feeds the low-amplitude pulses, whose frequency is proportional to the motor speed, to the LM2917's charge pump. As a result, the pump generates a current, I_1 , whose average value is directly proportional to the input frequency.

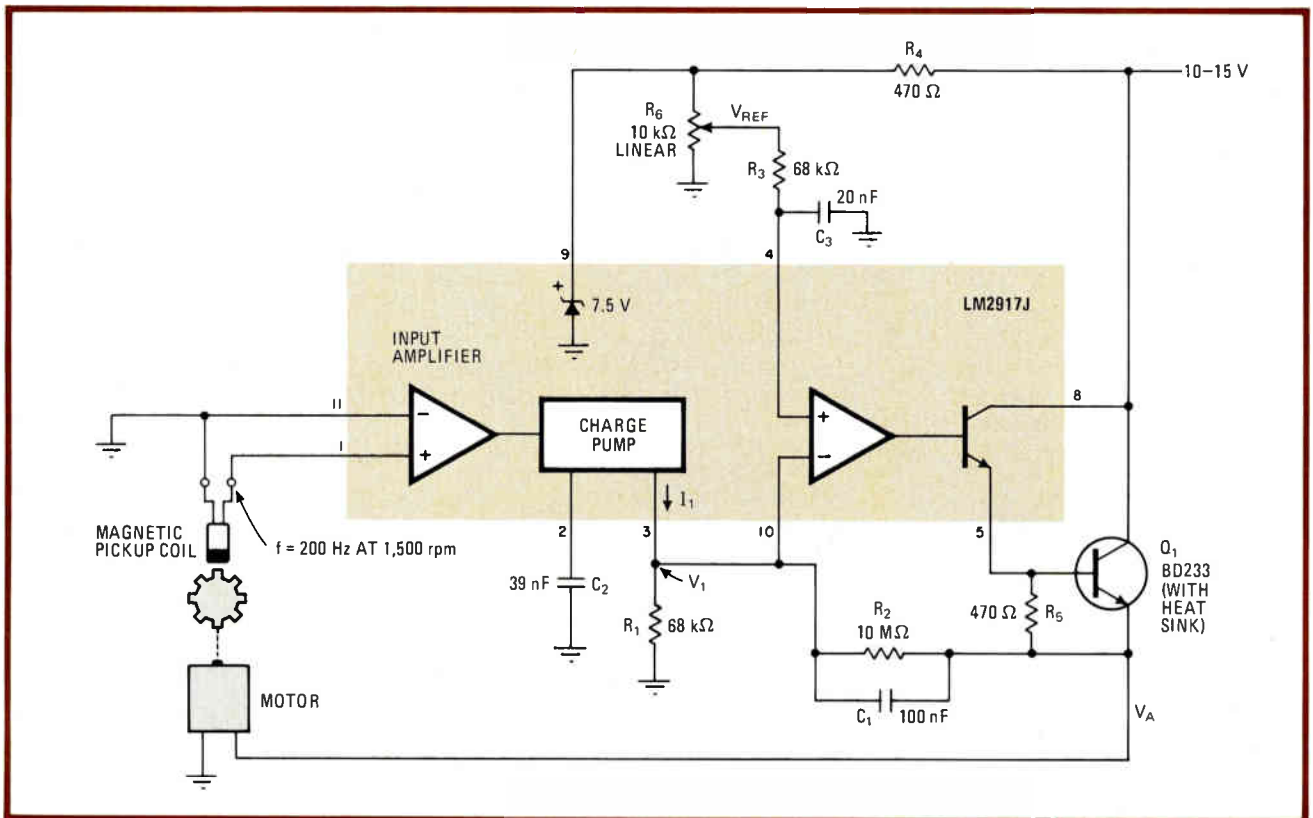
The operational amplifier that follows compares this voltage to a user-set reference and, through power trans-

istor Q_1 , generates a voltage for the motor's armature of $V_A = (R_2/R_1)(V_{ref} - I_1 R_1)$. Thus, potentiometer R_6 sets the motor's speed, for when $V_1 > V_{ref}$, voltage V_A decreases, and vice versa.

In this application, the gain of the operational amplifier, determined by resistors R_1 and R_2 , has been set at approximately 150. The greater the gain, the lower the variation of motor speed with changes in load resistance. However, the setting of very high gains should be avoided, because there will be a reduction in the gain and phase margins—that is to say, a loss of stability in the feedback control loop.

As for the selection of other components to meet any particular application, note that capacitor C_1 serves a double purpose: it integrates pulsed current I_1 , thereby performing a smoothing function, and it sets a low-frequency pole for the amplifier, thereby ensuring stability. C_2 sets the conversion factor of the tachometer and should be increased for low-speed motors. R_3 minimizes the offset due to the amplifier's bias currents at pins 4 and 10. Finally, C_3 functions as a noise filter.

As seen, the LM2917's tachometer conversion factor will be almost independent of its supply voltage, as a consequence of the zener diode connected at the device's supply port. The supply voltage should not fall outside the range of 10 to 15 volts, however. □



Setting speed. LM2917J tachometer, which is basically a frequency-to-voltage converter, sets and stabilizes motor speed. Few RC components are required, thereby simplifying circuitry. Power transistor Q_1 is the only external active element needed.

Low-cost timers govern switched-mode regulator

by Luces M. Faulkenberry
Texas State Technical Institute, Waco, Texas

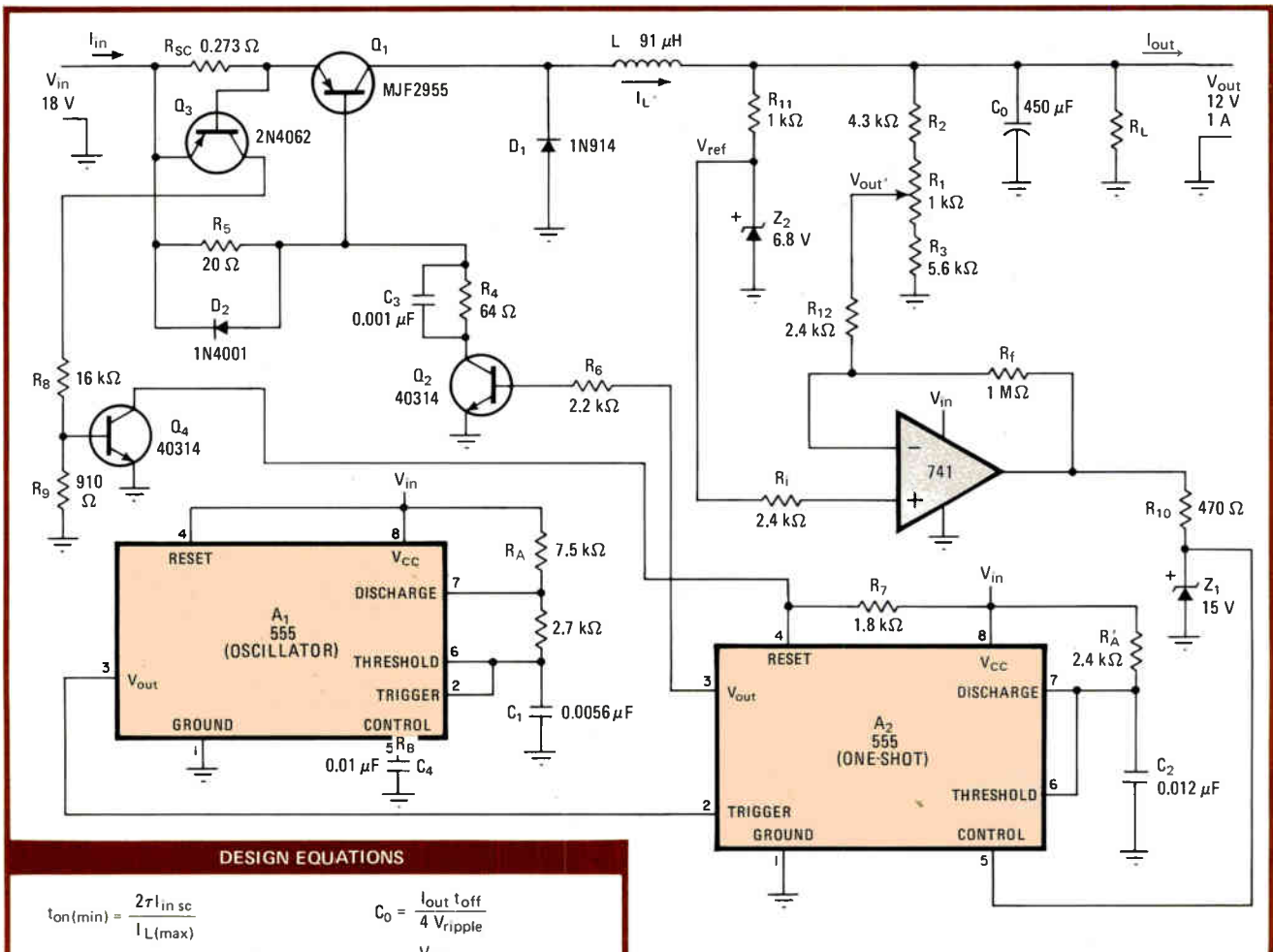
This step-down switching power supply, which uses 555 timers for pulse-width modulation, combines good performance with very reasonable cost. Providing an output of 12 volts at 1 ampere for an 18-v input, the unit offers input-current limiting, 0.1%/V line regulation, 0.5% load regulation, and an output ripple of only 20 mV. However, the design equations given here enable the user to specify his own requirements. The supply can be built for less than \$15.

Operating as an astable multivibrator at 20 kilohertz, timer A₁ generates the trigger pulses needed to switch the output of monostable multivibrator A₂ to logic 1 during each cycle. Modulating the control pin of one-

shot A₂ with the output of the 741 operational amplifier controls the width.

The op amp compares a preset fraction of the supply voltage, V_{out}, with the 6.8-v reference, V_{ref}. When V_{ref} > V_{out}, the control pin of the one-shot moves high and each pulse from the output of A₂ is lengthened accordingly until the reference and supply voltages are virtually equal. Similarly, if V_{ref} < V_{out}, the output pulses are shortened.

As seen, transistors Q₁ and Q₂ in the simple feedback loop perform the switching function. Monitoring transistors Q₃ and Q₄ limit the current by bringing A₂'s reset pin low when the design-maximum peak current through the inductor is reached, thereby shortening the width of the output pulses until the cause of the trouble is removed. Q₃ can also serve in a dual capacity as a switch to turn off the supply during overload conditions. For example, should automatic shutdown of the supply be necessary, Q₃ could be used to fire a silicon controlled rectifier in order to hold the reset pin of oscillator A₁ low permanently. In these cases, a simple circuit would also be needed to reset the supply manually. □



DESIGN EQUATIONS

$$t_{on(min)} = \frac{2\tau I_{in sc}}{I_L(max)}$$

$$C_0 = \frac{I_{out} t_{off}}{4 V_{ripple}}$$

$$t_{on}/t_{off} = \frac{V_{out} + 0.7}{V_{in} - (V_{out} + V_{ce sat Q_1})}$$

$$R_{sc} = \frac{V_{BEQ_3}}{1.1 I_p}$$

τ = OSCILLATION PERIOD

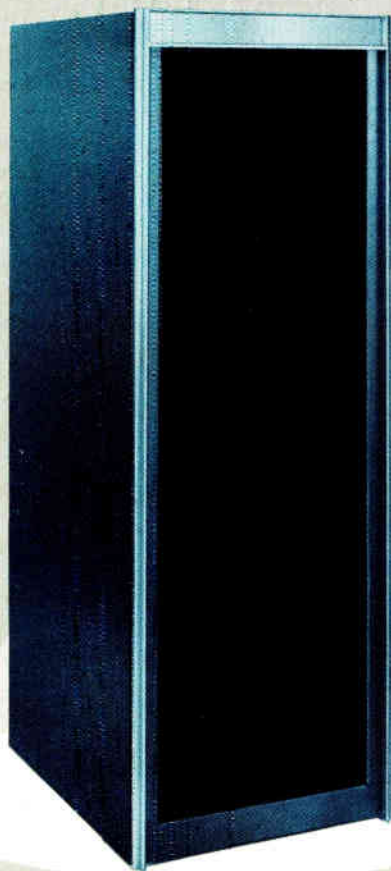
$I_{in sc}$ = SHORT-CIRCUIT INPUT CURRENT

$$I_p = 2 I_{out}$$

$$L = \frac{(V_{out} + 0.7) t_{off}}{I_p}$$

Rudimentary. Dc-dc switching regulator, using 555 timers, is simple and low-cost yet provides good performance. Typical specs of 18-V-in-to-12-V-out unit include 0.1%/V line regulation, 0.5% load regulation, and output ripple of 20 mV. User can design supply to meet his own requirements with aid of given equation set.

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Differential amp cancels integrator's crosstalk

by Elzbieta Nowicka
Atomic Energy of Canada Ltd., Ottawa

The performance of a high-speed integrator can be improved considerably by utilizing the excellent common-mode rejection characteristics of an operational amplifier to reduce crosstalk caused by the switching of waveforms during the circuit's integrate-and-hold sequence. More specifically, operating the amp in its differential mode enables the integrator to virtually cancel the switching offsets that are generated by the almost ideal switch—the complementary-MOS analog gate, which is inexpensive and has low on-resistance but rela-

tively high feedthrough. The supporting circuitry required (two extra gates) is minimal.

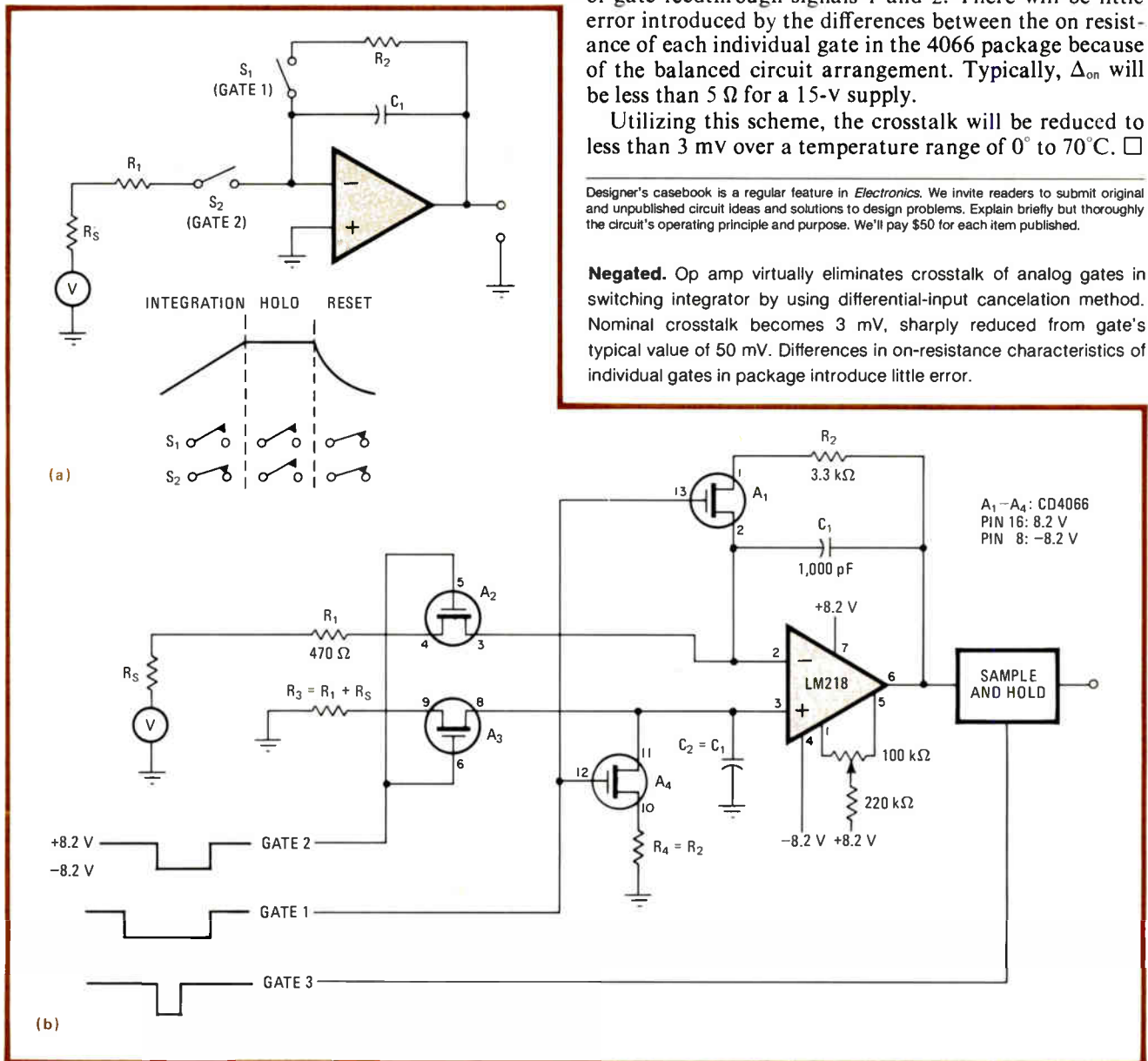
The technique generally used to start and terminate the three-step integration sequence is shown in (a), where S_1 and S_2 represent two electronic switches. These switches must be selected carefully, the main requirement being that the on-resistance of these devices be as low as possible, especially when the R_1C_1 time constant is small.

The C-MOS CD4066 transmission gate, with its nominal on-resistance of only 80 ohms for a supply voltage of 15 volts, would normally serve well in these applications, except that its crosstalk (the unwanted feedthrough of the gating signal) is high—typically, 50 millivolts for a 10-v square wave having $t_r = t_f = 20$ nanoseconds and a gate-output load of 1 kilohm. By introducing a pair of switches at each of both inputs of the LM218 op amp (b), however, the integrator will provide virtual elimination of the crosstalk by means of differential cancellation of gate feedthrough signals 1 and 2. There will be little error introduced by the differences between the on-resistance of each individual gate in the 4066 package because of the balanced circuit arrangement. Typically, Δ_{on} will be less than 5Ω for a 15-v supply.

Utilizing this scheme, the crosstalk will be reduced to less than 3 mV over a temperature range of 0° to 70°C . \square

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.

Negated. Op amp virtually eliminates crosstalk of analog gates in switching integrator by using differential-input cancellation method. Nominal crosstalk becomes 3 mV, sharply reduced from gate's typical value of 50 mV. Differences in on-resistance characteristics of individual gates in package introduce little error.



Special report

Tape automated bonding meets VLSI challenge

Japan and France lead the way in applying chips on tape directly to hybrid and pc substrates

by Jerry Lyman, *Packaging & Production Editor*

□ With the world's electronics industries poised on the brink of the era of very large-scale integration, tape automated bonding is picking up momentum at last. Already on automated assembly lines in France and Japan, arrays of tape-bonded LSI circuits with up to 40 leads are being reflow-soldered or thermocompression-bonded either to large digital hybrid circuits that are destined for computers or onto small rigid or flexible printed-circuit boards aimed at low-end consumer electronic products.

Meanwhile, back in the U.S., TAB remains for the most part at the experimental stage. Its usual implementation is in auto-

matic assembly used by just a few integrated-circuit firms to place small-scale devices in 14- to 16-pin plastic molded dual in-line packages. But the important technology of applying bare chips on tape to hybrid or pc substrates falls far below the overseas level. This technology is strictly confined to a small group of extremely large electronics and computer firms equipped to modify their own wafers with the interconnection bumps (see Fig. 1) that protect the chips' terminal pads during bonding—a vital service the U.S. semiconductor industry is still unwilling to supply to hybrid manufacturers.

Chips on tape are likely to be a serious contender for the VLSI package of the future. A recent report on high-density interconnections from BPA (Management Services) in Dorking, Surrey, England, predicts that by the end of the decade they will account for 20% to 30% of all IC packaging applications because of their significant advantages of size and testability.

Tape manufacturers can already produce tapes whose frames can accommodate chips with over 100 leads, so VLSI devices will pose no special problems in this area. Manufacturers of automatic bonding and placement machines for tape-bonded chips see no difficulty in handling these multileaded tapes.

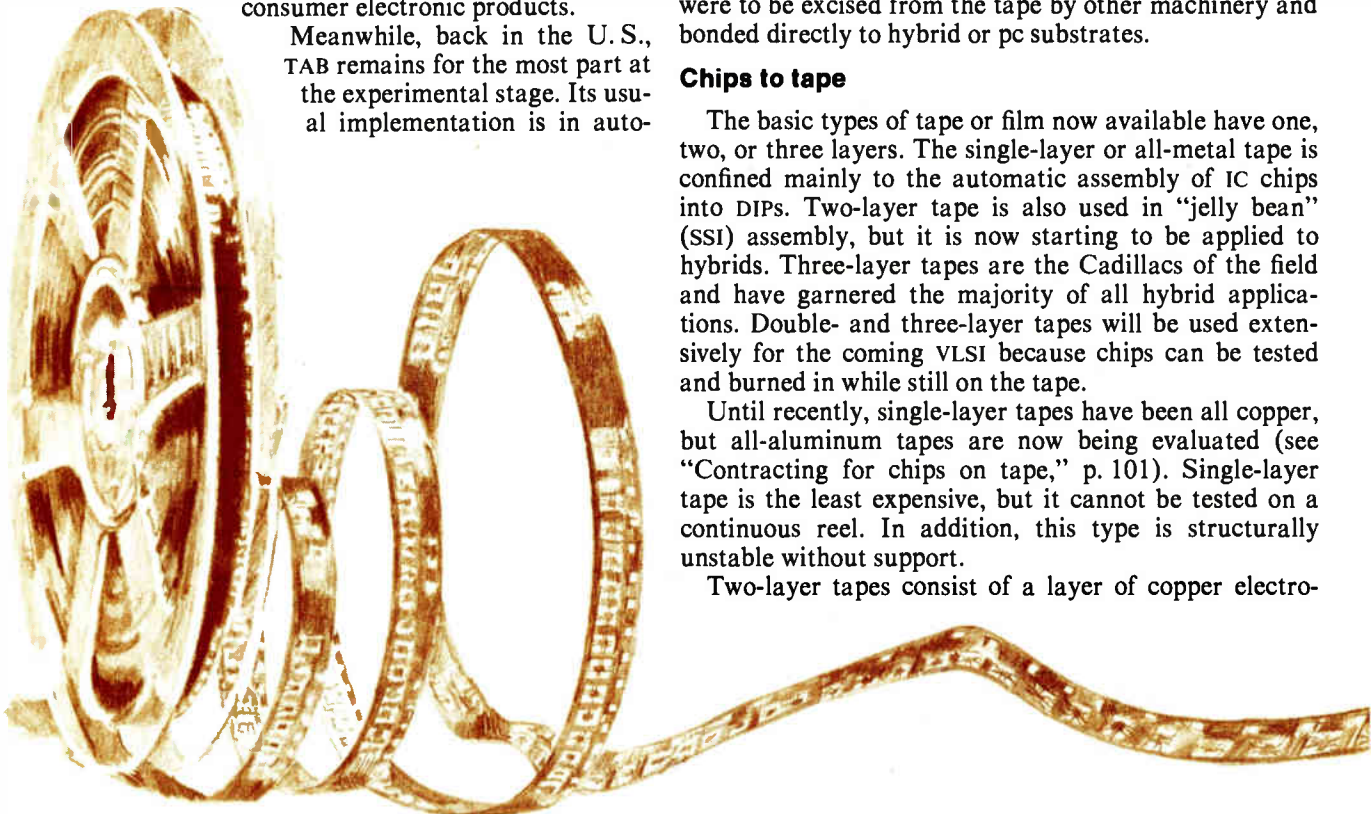
The concept of TAB, just beginning its second decade, was first announced by General Electric Co., Syracuse, N. Y., in 1971. It called for automated mass bonding of specially bumped SSI chips to specially prepared tape. Specifically, the chips were to be soldered to the inner lead pattern of spiderlike copper interconnections etched on successive frames of a copper-coated insulating film with a 35-millimeter sprocketed format. The tape was then to be moved on reels to special machines where the outer leads could be bonded to metal lead frames for eventual use in molded DIPs. Alternatively, the frames were to be excised from the tape by other machinery and bonded directly to hybrid or pc substrates.

Chips to tape

The basic types of tape or film now available have one, two, or three layers. The single-layer or all-metal tape is confined mainly to the automatic assembly of IC chips into DIPs. Two-layer tape is also used in "jelly bean" (SSI) assembly, but it is now starting to be applied to hybrids. Three-layer tapes are the Cadillacs of the field and have garnered the majority of all hybrid applications. Double- and three-layer tapes will be used extensively for the coming VLSI because chips can be tested and burned in while still on the tape.

Until recently, single-layer tapes have been all copper, but all-aluminum tapes are now being evaluated (see "Contracting for chips on tape," p. 101). Single-layer tape is the least expensive, but it cannot be tested on a continuous reel. In addition, this type is structurally unstable without support.

Two-layer tapes consist of a layer of copper electro-



deposited or laminated to polyimide (Kapton) film. This tape is perhaps twice as costly as single-layer tape, but it can take the heat of soldering and is testable. At the present time it is limited to 35-mm widths.

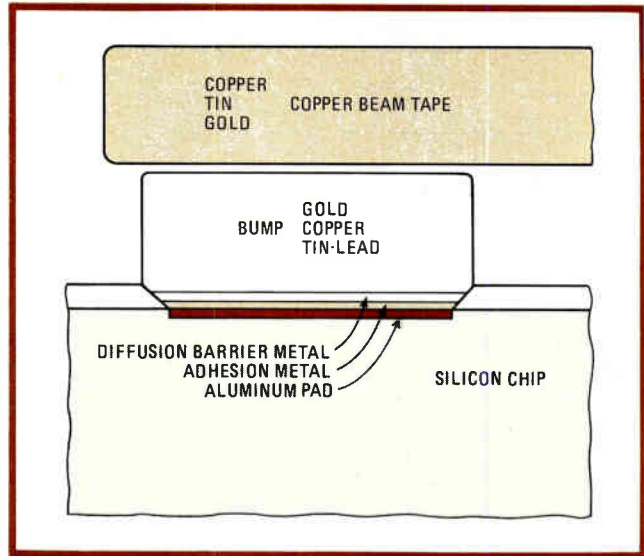
Three-layer tape has a layer of copper on a layer of adhesive over a polyimide or polyester film. This composite is fully testable and comes in widths up to 70 mm, so it is suitable for carrying large and costly multileaded LSI and VLSI devices. However, its adhesive layer limits the temperature that it can survive in and it has—at least in polyimide versions—about five times the cost of a comparable two-layer tape. Table 1 summarizes the construction and approximate cost of each tape type.

In multilayer tapes Kapton is normally the insulating material. Tradlon polyparabanic acid (PPA) film from Exxon Chemical Co. USA, Houston, has now been qualified for use by at least one film manufacturer, International Micro Industries of Cherry Hill, N. J., and is being evaluated by other TAB users. PPA costs less than polyimide film, and though it has a lower temperature limit, it will take the heat of soldering. Polyester film is another alternative and is currently used at CII-Honeywell Bull in Angers, France, but its low temperature limit has held down such application elsewhere.

Making tapes

All of the commercial manufacture of TAB tape is concentrated in five American companies—3M's Electronic Products division, St. Paul, Minn.; International Micro Industries; the Dynatape division of Dynacraft Inc., Santa Clara, Calif.; Fortin Laminating Corp., Sylmar, Calif.; and Koltron Corp., Sunnyvale, Calif.

3M, one of the first companies into the film-carrier business, is now producing one- and two-layer tapes plus a one-layer bumped tape. In addition, the company will supply unpatterned three-layer 35-mm tape for in-house TAB facilities. IMI has standardized on a 35-mm three-layer tape and Dynatape is concentrating on various types of bumped tape (see "The status of bumped tape,"



1. Bump metallurgy. Copper and gold bumps on the integrated circuit die effect a copper to copper bond, gold to gold bond, or gold to tin eutectic bond between the beam tape and the chip. Lead tin bumps to tin plated tape is a less popular combination.

p. 103). Fortin supplies a two-layer tape, a two-layer bumped tape (in limited quantities), and three-layer 35-mm material. Koltron is manufacturing single- and three-layer tapes.

These manufacturers are facing the advent of VLSI with confidence. For instance, Joe A. Zimmerman, marketing manager for microinterconnecting systems at 3M, says, "We think the coming high-lead devices are opening a new door for tape bonding." He continues, "We are building designs with up to 200 leads already but are talking with people about more than 300 leads. With our current technology of 3-mil tape beams on 3-mil spaces, we can do everything we have seen." An example of a 60-lead IC that has been bonded to a two-layer tape from 3M is illustrated in Fig. 2. Carmen Burns, who is general

Contracting for chips on tape

Contract tape bonding is a new arrival in the world of tape automated bonding. Ordinarily chips on tape are captive either at a large integrated circuit firm's assembly operations or in an in-house TAB facility. Now two California firms, American Automated Assembly Corp. Santa Clara, and Indy Electronics Inc., Manteca, are willing to take a customer's unbumped chips or wafers and bond them to all-metal tapes. This tape will then be bonded to a lead frame, which in turn will have epoxy dual in-line packages molded on.

American Automated Assembly's operation is targeted for full operation by Jan. 1, 1981. An all-aluminum tape with silver- and gold-plated bumps will be used. The Santa

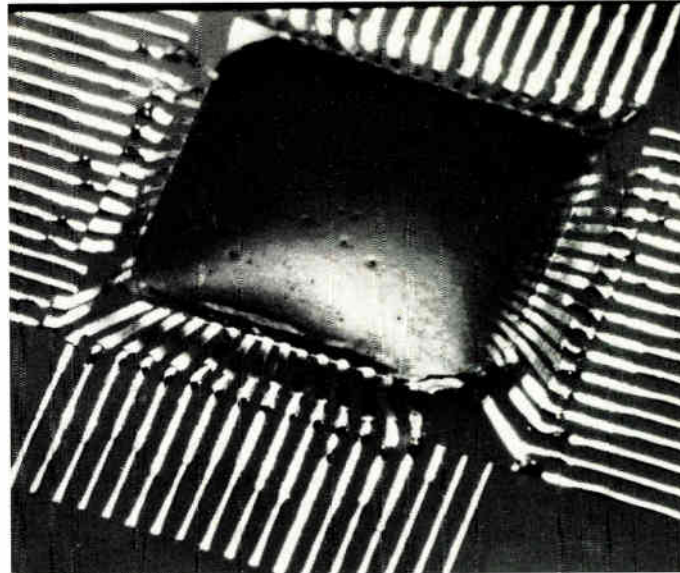
Clara company has developed its own inner and outer lead bonders and expects to be able to package devices with up to 40 pins in epoxy DIPs. John Manning, president of the firm, sees the possibility of supplying chips on tape rather than in DIPs further down the line. At present, American Automated Assembly is in a preproduction stage and can supply sample quantities.

Indy Electronics is planning a similar operation also based on a bumped aluminum tape and automatic assembly equipment designed in house. However, this operation is still in a development stage.

This service, if successful, will let users package runs of custom chips in discrete packages or on tape.

TAPE CONSTRUCTION AND COST			
Type	Pattern method	Thickness (μm)	Cost per frame (cents)
One-layer: copper	etched or punched	25-50	1-2
aluminum	punched	25-50	
Two-layer: copper polyimide	etched etched or printed	25-50 12-25	2-4
Three-layer: copper adhesive polyimide or polyester	etched punched punched	35 12-25 75-125	10-50

SOURCE: INTERNATIONAL MICRO INDUSTRIES



2. Silicon on tape. With the aid of a 3M two-layer beam tape, Kylex Corp. has mounted a 60-lead pretested liquid-crystal-display driver to a printed circuit board. A dielectric support ring acts as cover coat retainer as well as support for the inner lead bond.

manager of Dynacraft, sees no limit to the number of leads possible. Dynacraft produces tapes with 55 leads as a matter of routine, and it has had developmental projects with up to 200.

On the general growth of the TAB market, Burns notes that a decade ago tape bonding was fourth in assembly techniques behind wire bonding, film chips, and beam leads. Now it is second, and according to Burns, "tape is growing faster than wire bonding, and by the end of the 1980s it will be the dominant technique."

Tom Angelucci, president of IMI, a maker of both film and TAB bonders, sees TAB as the future dominant assembly technique for VLSI (that is, with greater than 100 leads) devices because of TAB tape's inherent lead resolution and because of its high throughput due to mass bonding.

Present LSI chips are based on input/output pads 4 mils on a side on 8-mil centers, but as lead count increases such an interface becomes too wasteful of precious real estate, so the I/O pads must shrink. But current wire bonders cannot connect to smaller pads without overlapping the adjoining ones. Only TAB tape, based on photolithography, will be able to create the fine beams needed to access the I/O pads 2 mils on a side on 4-mil centers of future VLSI chips.

Automatic wire bonding is the primary competitor of TAB in IC automatic assembly. The former is a serial process (one pad at a time) and as the number of pads goes up, bonding time increases. In TAB, where leads are mass-bonded [*Electronics*, Dec. 25, 1975, p. 61], bonding time is constant, rather than a function of I/O pad count. This gang bonding means that TAB will have a much higher throughput than wire bonding for VLSI chips.

John Hass, mass bonding product manager of

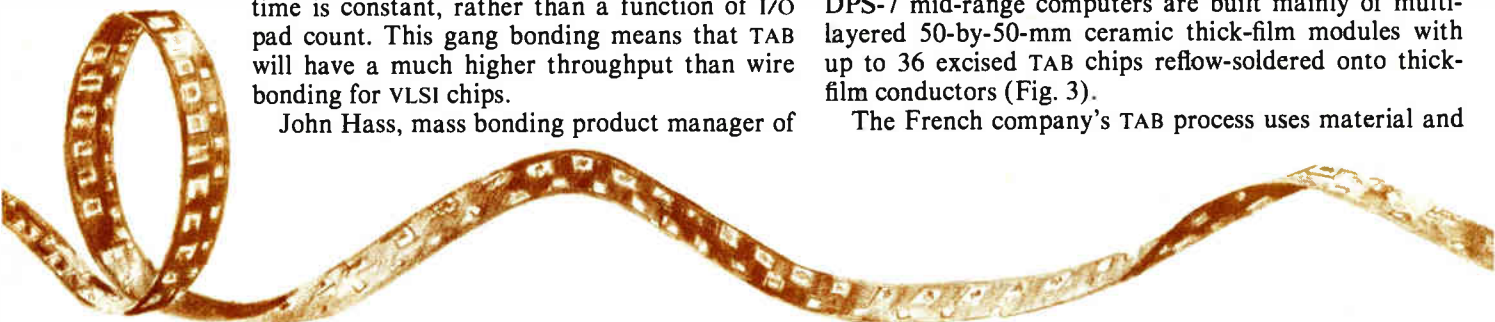
Jade Corp., Huntington, Pa., says present-day TAB bonders place no limit on the number of inner leads that can be mass-bonded, and up to 200 outer leads can be bonded with the Jade machines. So inner- and outer-lead TAB bonders already exist commercially for the coming wave of VLSI devices.

Hybrid TAB

The ultimate high-density chip package is a wire-bonded unit [*Electronics*, Sept. 28, 1978, p. 119]. However, a close second is a TAB-bonded chip that has been excised from its frame of tape. This tiny chip package with its copper beams is the basis of some of the most sophisticated packaging in France and Japan. Unfortunately, the United States, with about 1,600 independent hybrid companies and many large in-house facilities, lags sadly in the application of chips excised from tape to hybrids. This type of activity is confined to giant firms like Honeywell Inc. at its divisions in Phoenix, Ariz., and St. Petersburg, Fla.; Bell Laboratories in Allentown, Pa.; Burroughs Corp. of San Diego, Calif.; Westinghouse Systems Development Center of Baltimore, Md.; and General Dynamics Corp. of Pomona, Calif.

CII-HB originated the term tape automated bonding in the mid-1970s in France and has been using the technique successfully ever since. At present, this firm's DPS-7 mid-range computers are built mainly of multi-layered 50-by-50-mm ceramic thick-film modules with up to 36 excised TAB chips reflow-soldered onto thick-film conductors (Fig. 3).

The French company's TAB process uses material and



The status of bumped tape

One of the limitations of the tape automated bonding process is that it requires special metalized bumps to be plated up over an integrated circuit's aluminum input/output pads. This process protects the pads during the bonding process, which could be either soldering or thermo-compression bonding. IC companies in the U. S. have not on the whole been willing to supply bumped chips or wafers or chips on tape, so only large companies capable of bumping their own or purchased chips, such as Western Electric Corp. and Honeywell Inc.'s Honeywell Information Systems in Phoenix, Ariz., and its Avionics division in St. Petersburg, Fla., have been able to have in-house TAB operations.

To get around this situation and to allow the use of standard unbumped wafers or chips, tapes with the bumps already on them are now being manufactured and are available from companies like the Dynatape division of Dynacraft Inc., Santa Clara, Calif.; 3M's Electronic Products division, St. Paul, Minn.; and Fortin Laminating Corp., Sylmar, Calif.

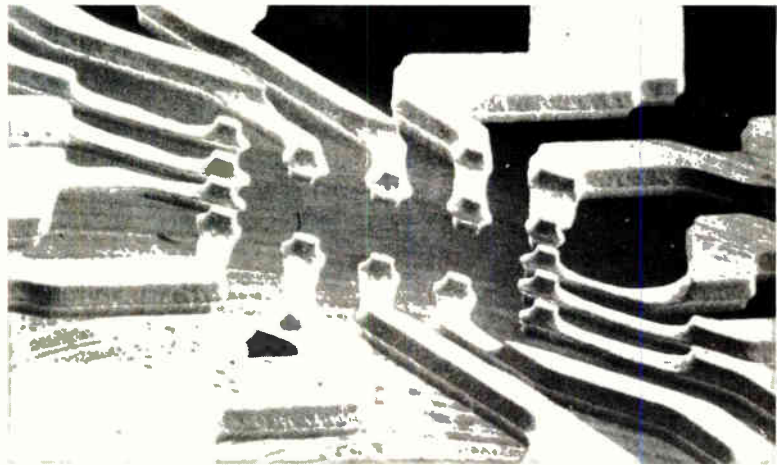
Since 1978, engineers at General Dynamics Corp., Pomona, Calif., have been evaluating bumped tapes for military hybrid applications, with mixed results. The technique is promising, but needs more work to make it applicable to either hybrid or automatic assembly operations.

Bumped tape is more complex and expensive than planar tape. Also, chips rather than sawed-up wafers must be interfaced with the inner lead bonders and then placed on a heated workholder. Finally a completely new type of inner lead bonder, with adequate viewing optics for alignment of the small tape bumps to the chip's alu-

minum I/O pads, must be used instead of a standard inner lead bonder.

Given these disadvantages, as well as the large amount of standard tape-bonding equipment already in place, it appears that the overwhelming amount of TAB work for at least the next several years will be with planar tape, particularly in hybrid work with large-scale and very large-scale integration.

However, Dynacraft, the company that developed bumped tape, is shipping it in volume. "It has been in the works for three years and we have just phased it into volume production," notes Carmen Burns, general manager of the company. Dynacraft's single-layer bumped tape seems headed for the automatic assembly of "jelly beans" (small-scale integrated circuits) and its three-layer bumped tape is being used as a hybrid module by European watch manufacturers.



mines developed in house. The tape is 35-mm Mylar (polyester) with standard sprocket holes and a layer of laminated copper 35 micrometers thick.

For computer design, CII-HB has now standardized two TAB chip configurations—with 24 and 40 leads. For VLSI chips in future computers, lead count may increase by a factor of four.

Jean Valin, technology development director for CII-HB, says that TAB works so well for its present generation of chips—customized current-mode logic (CML)—that a development program is already under way to extend its use to VLSI chips for the company's next generation of computers.

CII-HB will use the same 35-mm tape and automatic reel-to-reel machines and testers for its next generation of chips. It will also retain the same substrate size used in the DPS-7.

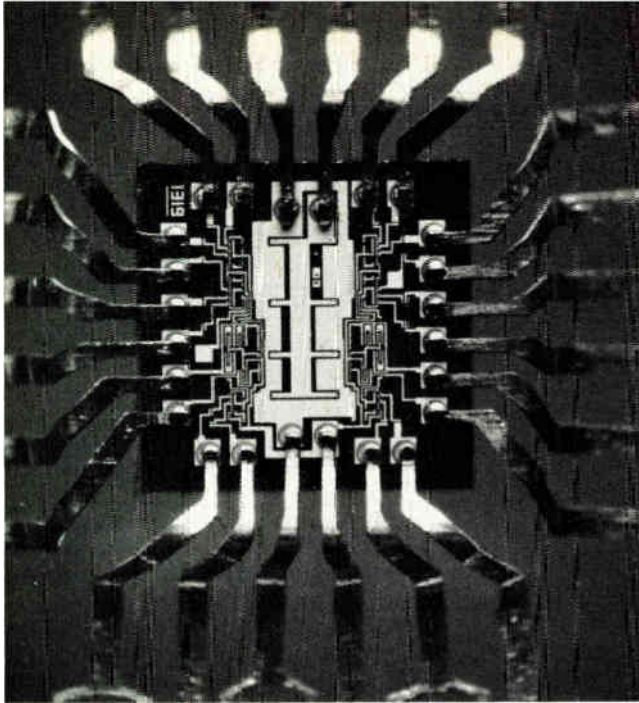
Honeywell Information Systems in Phoenix has devel-

oped a packaging system for computer use similar but not identical to the French system. The HIS system also employs a three-layer testable tape, the same family of CML chips, and an 80-by-80-mm multilayer ceramic substrate. HIS has not yet brought this technique to the production state, although work has been going on since 1977. However, the division has already designed automatic handling and testing equipment for this operation [*Electronics*, April 26, 1979, p. 115] based on strips of films in magazines rather than the reel-to-reel approach of CII-HB.

Japanese films

The Japanese are easily the most active participants in TAB. According to Tom Angelucci of IMI, at least 20 or more companies have several different circuits in production or in the planning stages.

Two companies using TAB in heavy volume in Japan



3. Hybrid TAB. Packaging of the CII-Honeywell Bull DPS-7 computer is based on multilayered ceramic modules carrying up to 36 TAB-bonded CML chips. This is a 24-lead device excised from a tape that has been reflow-soldered to a substrate's conductor pattern.

are Sharp Corp., in its low-priced digital consumer products, and Nippon Electric Co., in its computer products. Both are already applying TAB to I/O chips with more than 100 leads.

Sharp's Tsamu Washizuka, general manager of the electronic calculator division of its industrial instruments group, says that his division is using film-carrier chips in one- and two-chip calculators and a two-chip watch with voice output. No incoming inspection tests are done because rejects run less than 0.01%.

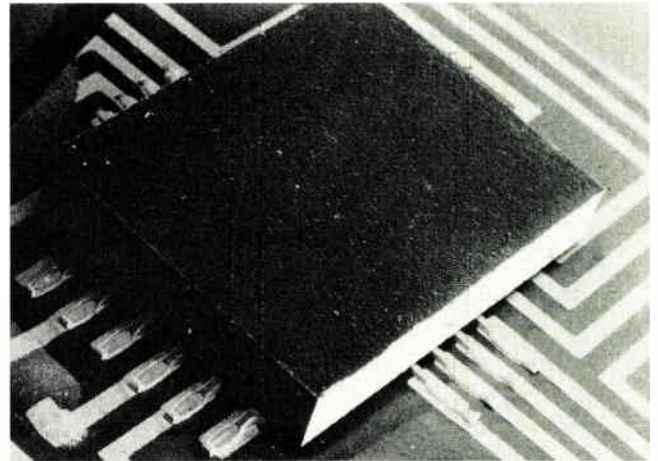
At Sharp, TAB devices are cut from the film and reflow-soldered to pc boards. The maximum number of leads is now 80 for a one-chip calculator with a dot-matrix display, although it is possible this will be increased to 100 or 120.

NEC manufactures CML devices on three-layer testable 35-mm tape for its largest computer. Kodo Kimura, engineering manager of the IC division of the IC design department, sees no problems in using 35-mm film for VLSI devices with up to 120 leads.

The chips on tape have been used extensively in NEC's largest computers—ACOS 800, 900, and 1000. The company will use them in the future, especially for VLSI.

In the NEC system, the excised CML devices are thermocompression-bonded rather than soldered to multilayer substrates as in the CII-HB and HIS systems. However, like the French and American TAB systems, all chips are tested on tape.

Though companies like CII-HB, Sharp, and NEC have made great advances in TAB for hybrids and pc boards, in the U.S. only large companies have the financial resources to bump their own wafers and to set up a highly expensive automated hybrid assembly flow. Some companies who are using or experimenting with hybrid TAB are



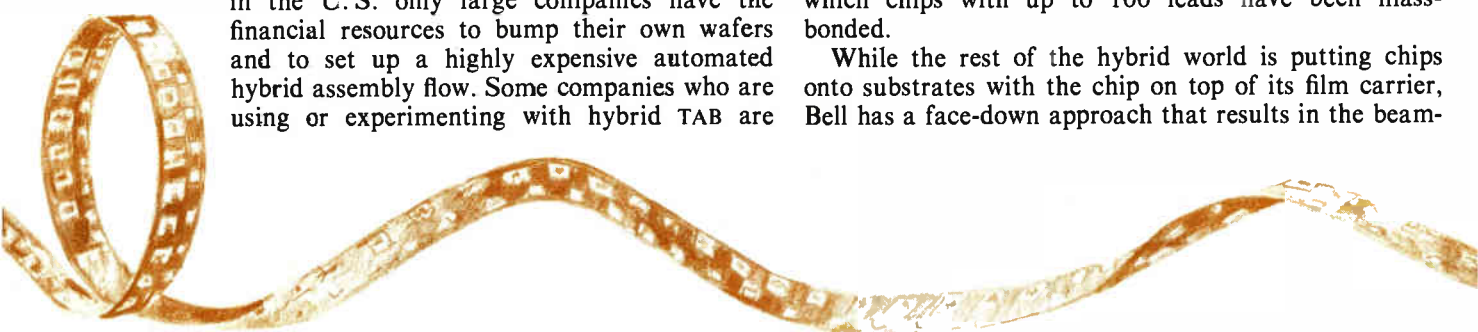
4. About-face. In most applications, tape-bonded chips are mounted on top of the tape. Bell Labs uses the face-down (chip under the tape) method shown for a beam-lead type of package with fewer assembly operations and less surface area than face-up TAB.

Honeywell, Western Electric, Bell Labs, Burroughs, Westinghouse, and General Dynamics. In almost all cases, these programs are developmental, whereas overseas hybrid TAB is in full production.

While Honeywell Information Services has concentrated on large-scale digital hybrids, the Honeywell Inc. Avionics division in St. Petersburg, Fla., has been running an extremely successful program for military digital hybrids based on thermocompression (TC) bonding of excised SSI and MSI chips to small ceramic substrates. The Avionics division bumps its own wafers and receives a three-layer tape from the HIS division. A whole variety of chips have been bumped—bipolar, complementary-MOS, Schottky, and linear. TAB chips are bonded to ceramic substrates with a Jade Massbond 34810 system that excises the chip from the tape and forms its leads.

At Bell's facility, development work is now in progress on the application of TAB chips to thin-film hybrids for telephone and telecommunications circuitry. Bell Labs has settled on a gold-plated, all-copper, 19-mm tape to which chips with up to 100 leads have been mass-bonded.

While the rest of the hybrid world is putting chips onto substrates with the chip on top of its film carrier, Bell has a face-down approach that results in the beam-



lead-like configuration of Fig. 4. In this approach, bumped chips are inner-lead-bonded to tape sites on the copper tape and the leaded chips excised from the tape. The resulting package is placed face down on the ceramic substrate and its leads are TC-bonded to thin-film pads. After bonding, the circuit is cleaned and then encapsulated in Dow-Corning RTV silicone rubber.

Face-down TAB requires fewer assembly operations than face-up TAB and takes up less surface area, as Fig. 4 shows. Bell mixes face-down TAB and beam-leaded chips on its thin-film hybrids. The all-copper tape usually prevents testing of chips on tape, though all wafers are probed.

But a hybrid program at the Westinghouse Systems Development Center [*Electronics*, June 19, 1980, p. 50] has devised a way of testing IC chips on an all-copper bumped tape. At Westinghouse, the chips are excised from the tape and bonded to a special test frame that accommodates seven standard IC sizes. The frame, an interconnection on a 35-by-19-mm piece of polyimide film, is placed in a plastic slide carrier for protection and ease of handling. It may be reused for successively larger ICs once the chip under test has been excised from it.

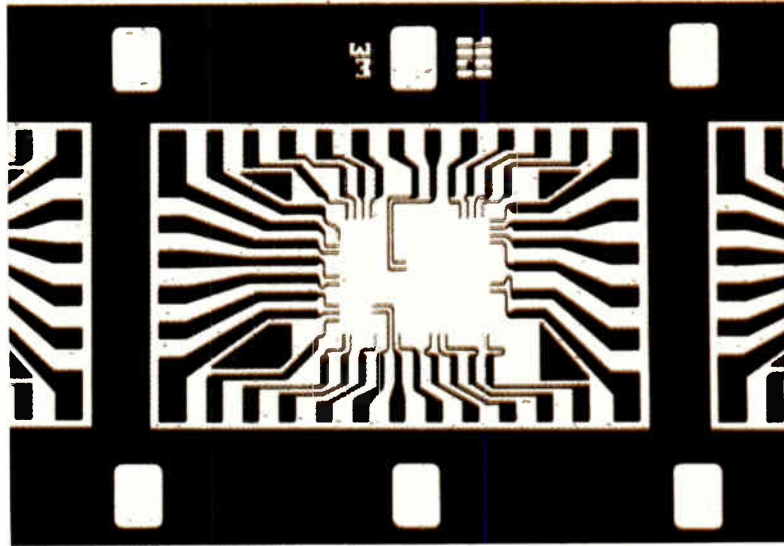
Burroughs is using TAB devices to build up packages with more than 100 leads. This company is committed to three-layer, 35-mm testable tape for its complex custom LSI and VLSI chips, which can be as large as a 160-lead device on a frame of 35-mm tape. For units with even higher lead counts, Burroughs engineers feel a wider tape format is needed. Burroughs is in a research and development phase and could eventually use its TAB devices unpackaged but protected by a drop of epoxy or else in a discrete leaded package of some type.

DIP/TAB

Though trailing in hybrid and pc-substrate TAB applications, the U. S. is the center of TAB assembly of ICs and discrete semiconductor components into plastic packages. Texas Instruments Inc., Dallas; National Semiconductor Corp., Santa Clara, Calif; Fairchild Camera & Instrument Corp., Mountain View, Calif.; and Motorola Semiconductor Group, Phoenix, Ariz., all have large automated assembly systems based on TAB. Mostek Corp., Carrollton, Texas, is now developing a TAB line. The first three of these companies jealously guard all details of tape type, format, and so on.

Motorola's Semiconductor Group, on the other hand, is quite open about its TAB operation. It uses a purchased all-copper tape for 16-lead bipolar and C-MOS devices and is planning to expand its operation to include 22- to 24-pin TAB-assembled devices. All the U. S. companies have in common that they will not sell chips on tape and they will not bump wafers for a customer's TAB facility.

One of the world's few firms that will supply chips on film directly is Siemens AG in West Germany, which bonds reels of chips onto three-layer film in four formats:



5. Inner leads. A 3M tape design concept shows a two-layer substrate with a dielectric support ring and center bridge to insulate conductors passing over the IC chip and/or accessing pinouts in the center of the device. This is a testable design.

35 mm, 16 mm, super-8, and double super-8. In fact, the firm's entire chip output is sold to outside customers, most of them in Europe and some in Japan.

Siemens has put many types of circuits on film, including Hall sensors (for automobile applications), operational amplifiers, hearing-aid amplifiers, and circuits for communication systems.

Currently the maximum number of leads for devices in production is 64. Devices with 84 and 156 pins are in preparation. In the discussion stage at Siemens are devices with more than 200 pins.

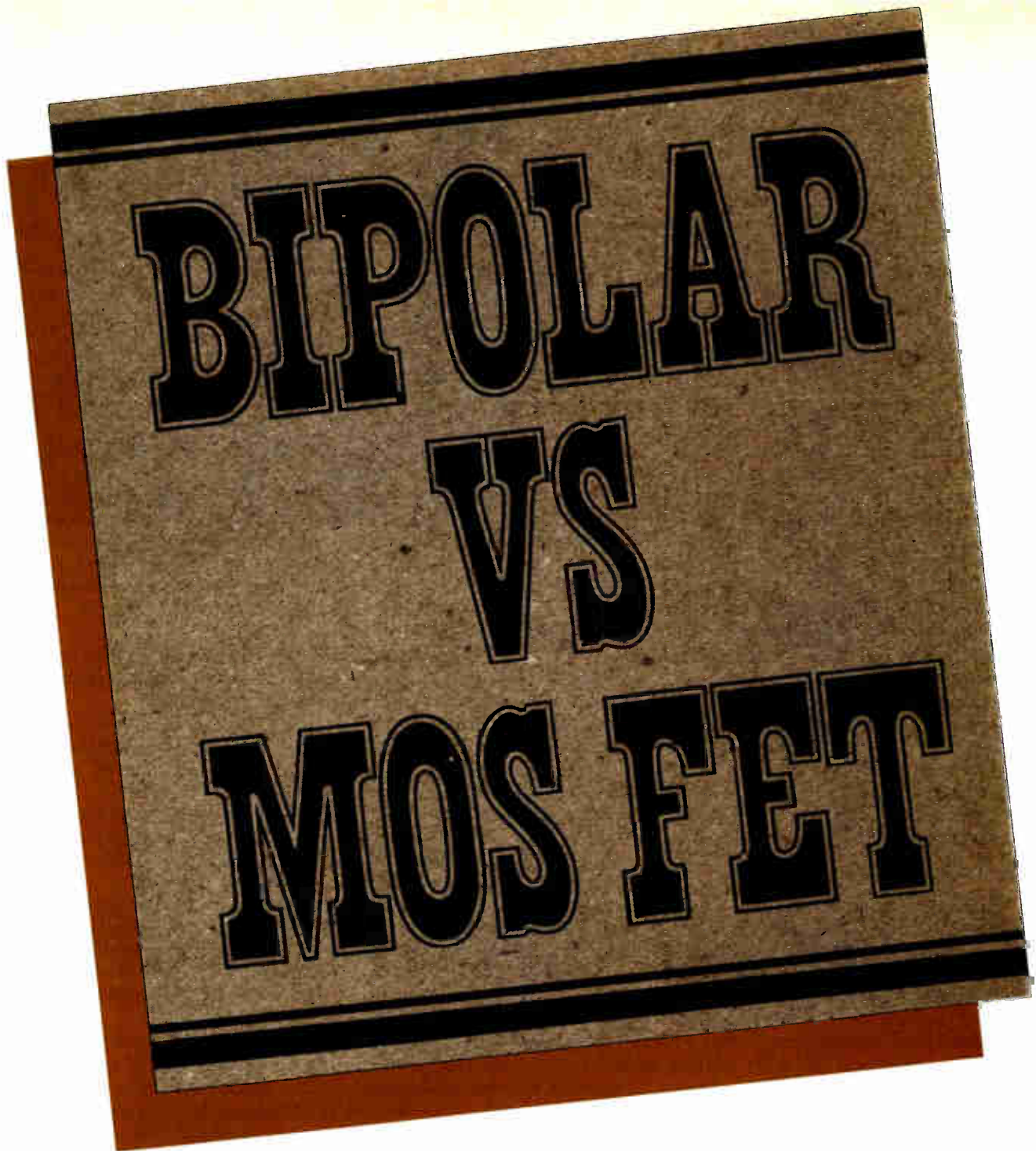
Despite the fact that only a handful of companies in the U. S. are working at hybrid TAB, this technique will become more prevalent in future VLSI applications to hybrid technology in this country. As chips with 100 to 300 leads appear, it will be almost impractical to handle them except on tape for hybrid use.

In the future, multichip tapes with more than one conductive layer will become available for special modules, where many interconnection functions of the master (motherboard) substrate can be incorporated in the multilayer tape, allowing for a simpler master board.

And finally, as chips get even more complex, it will become necessary to contact internal nodes for on-chip or on-tape testing rather than restricting contact to points on the periphery. Figure 5 shows an experimental tape of this kind from 3M. □

Reporting for this article was also done by Bruce LeBoss and Martin Marshall in Palo Alto, Larry Waller in Los Angeles, Arthur Erikson in Paris, John Gosch in Frankfurt, and Charles Cohen in Tokyo.





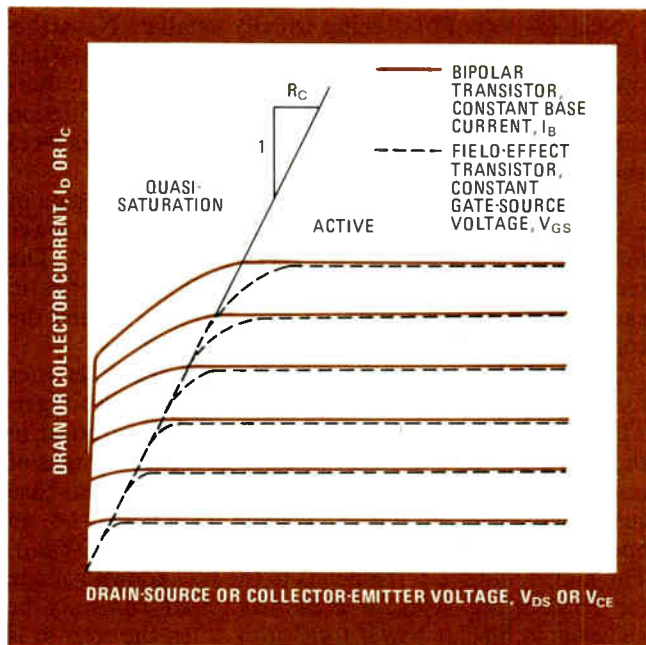
Seeing where the power lies

For switching applications requiring minimum device size, bipolar transistors are more efficient below 15 kHz

by Philip L. Hower, *Westinghouse Electric Corp., Research and Development Center, Pittsburgh, Pa.*

□ Much has been written about the advantages of MOS field-effect power transistors over bipolar devices, leaving the impression that MOS FETs have few disadvantages other than a comparatively higher price that is on the decline. A comparison of both devices, however, shows that bipolar power transistors can outshine MOS FETs in areas other than price. For example, where minimum device size is important and power is being switched at a frequency of 15 kilohertz or less, bipolar power transistors excel.

A valid comparison of both devices, which have as much in common as they have differences, can be made with regard to switching frequency, junction temperature, and current density, provided that the devices have the same die area. In addition, the costs per assembled



1. Comparison. The forward voltage drop of a bipolar power transistor is lower than that of a power MOS FET, as can be seen from the collector and drain characteristics of the devices. The difference is a result of the additional charge a bipolar device stores during turn-on.

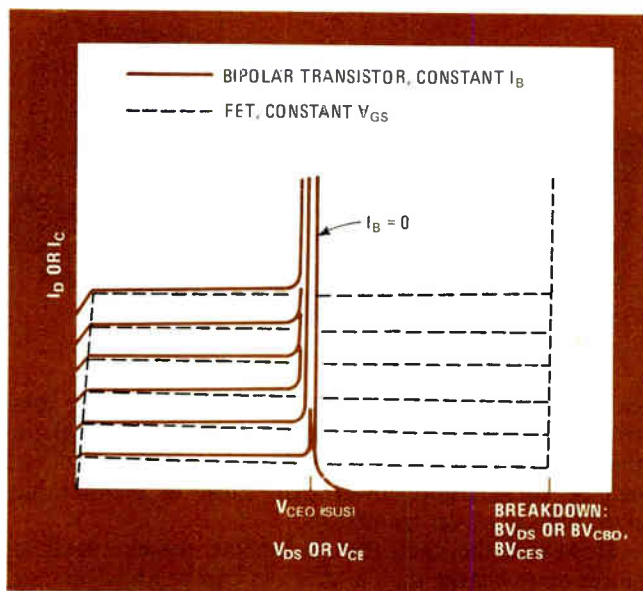
die are assumed to be approximately the same.

Besides being fabricated using the same silicon semiconductor technology, both bipolar transistors and MOS FETs are charge-controlled components. Charge is supplied to and removed from each device to achieve switching action. Both have lightly doped collector or drain regions, which are needed to block voltages while in their off-states. Another similarity of the two is that each has the same "ideal" maximum operating temperature, which is determined by thermal runaway of leakage current generated within the lightly doped region. This maximum operating temperature can be decreased in either type of device depending on the junction passivation scheme used.

Introducing charge

However, the manner in which charge is introduced and its location within each device differs. In bipolar transistors, turn-on is achieved by supplying excess minority carriers (holes in an npn device) to the base—but what constitutes the base in a bipolar transistor is subject to the operating point of the transistor's collector. When a bipolar transistor is turned on at its lowest voltage state (classical saturation), charge must be supplied in three different regions. Excess charge is first built up in the metallurgical base region. It is then supplied to the collector n region to form a current-induced base. Finally, the base-collector junction, known as a remote base, becomes externally forward-biased, thereby allowing the parasitic base-collector diode to store excess charge.

Most of the switching losses incurred in a bipolar power transistor during turn-on occur during the time needed to store charge in the metallurgical base and collector n regions.



2. Limits. At high voltage, two potentials come into play for a bipolar power transistor, whereas only one is of interest for a MOS FET. The two are the open-circuit collector-emitter (sustained) and collector-base voltages, the higher of which is the breakdown voltage.

Turning off, or removing charge from, a bipolar power transistor involves a reversal of the sequence of events described for turn-on. Charge is first removed from the remote base in what is a relatively lossless process. It is then removed from the collector n region via two different mechanisms: by a vertical back-injection of holes into the emitter from the current-induced base and by charge removal from the lateral edges of the current-induced base. This lateral sweep-out leads to a reduction in the effective conduction area and to an increase in current density.

Removal of charge from the collector n region completes the storage-time phase. During this interval, the collector current remains relatively constant, except near the end of the storage time, when current begins to decrease and the collector voltage begins to rise. When the charge from this region is nearly all removed, the collector junction begins its voltage-blocking action.

At this point, the bipolar power transistor is operating within the active region, and the applied reverse current quickly removes charges from the metallurgical base, producing a correspondingly rapid decrease in collector current. The accompanying current fall time that completes the turn-off process depends on the base transit time, the current gain, and the reverse base current. Charge removal from the metallurgical base and collector n regions is a relatively high-loss process and accounts for most of the switching losses in a bipolar power transistor.

Small turn-on charge

In contrast to bipolar power transistors, MOS FETs require only a small amount of charge for turning on. This charge is used to form the channel, reduce the width of the depletion layer (a layer that supports the off-state voltages), and charge parasitic gate-drain and gate-source capacitances. For small values of parasitic

BIPOLAR VS MOS FET

capacitances, turn-on time is rapid, because of the relatively short transit times associated with the channel and the depletion layer. Thus switching losses in a MOS FET can be considerably lower than those of comparable-sized bipolar power transistors.

However, the fact that a bipolar power transistor stores more charge than a MOS FET can be an advantage. The additional charge reduces forward-voltage drop (Fig. 1), assuming that the resistivity and thickness of the n layer for both a bipolar device and a MOS FET are the same. Furthermore, it is assumed that both devices have the same current-carrying cross-sectional areas. The latter assumption neglects a MOS FET's channel voltage drop and any resistance associated with current-spreading or junction-FET action in the drain region of the device.

Conduction may differ

An assumption of equal conduction areas for both types of device does not necessarily mean that individual die areas will be equal. The effective emitter area in a typical bipolar transistor design is about one half that of its die area. Until recently, such a ratio has not been

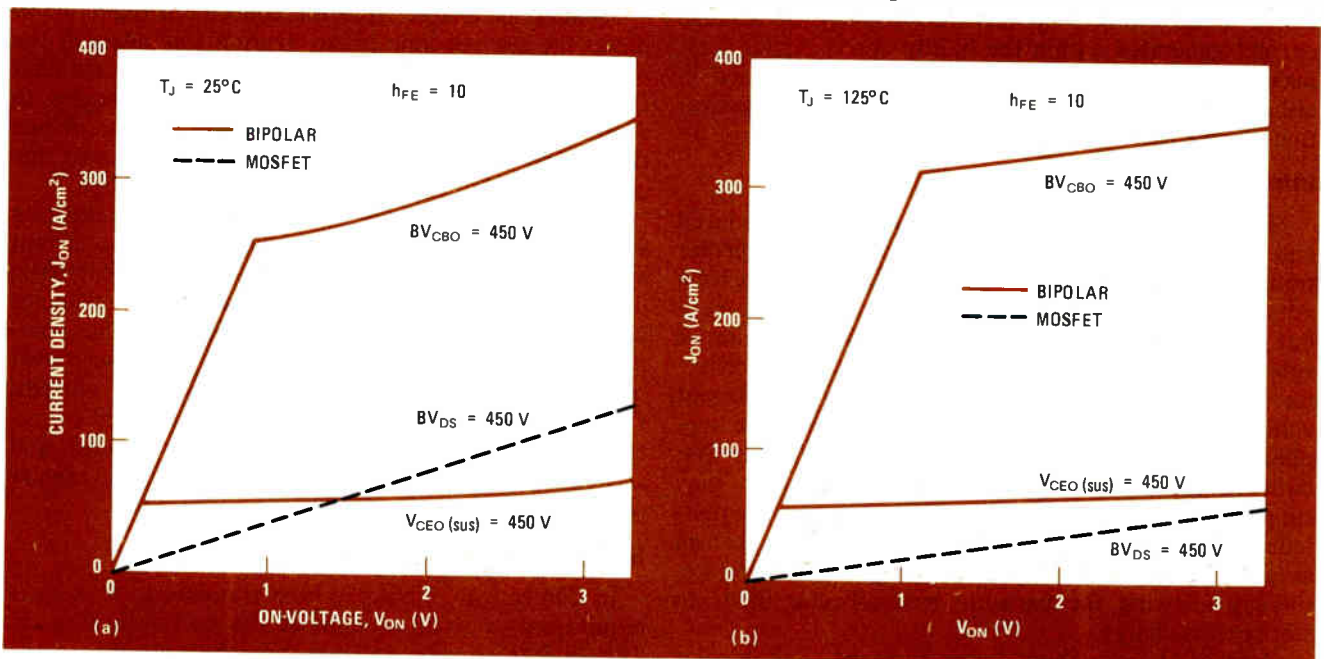
typical for MOS FETs, being usually smaller. Nevertheless, recent MOS FET design advances have made possible similar ratios. Consequently, for the purpose of the thermal calculations here, the one-half ratio of conduction area to die area will be assumed for both bipolar devices and MOS FETs.

As can be seen in Fig. 1, the quasi-saturation region of a bipolar power transistor permits operation at a lower forward-voltage drop than does that of the MOS FET. The reduction in collector-emitter voltage (V_{CE}) depends in each case on the values of the base current (I_B) and the collector current (I_C).

Figure 2 shows the collector and drain characteristics for both bipolar devices and MOS FETs at higher voltages. The major difference from the characteristics shown in the graph in Fig. 1 is that there are now two voltages of interest for the bipolar power transistor: an open-base sustaining collector-emitter voltage ($V_{CEO(sus)}$) and an open-emitter collector-base breakdown voltage (BV_{CBO}). The higher voltage corresponds to the breakdown voltage for both device types, a breakdown that can only be achieved in bipolar power transistors when the emitter is not injecting.

Don't cross

Crossing the $V_{CEO(sus)}$ line at high currents during the inductive turn-off of a bipolar power transistor is likely to initiate secondary breakdown. To avoid that, the bipolar power transistor would have to operate with a reduced off-voltage or with a snubber circuit to improve the I_C and V_{CE} turn-off loci. An alternative is to increase collector thickness and resistivity until $V_{CEO(sus)}$ is equal to the drain-source breakdown voltage (BV_{DS}) of a MOS FET. This increase in resistivity, however, brings with it an undesirable reduction in current gain (h_{FE}) within the quasi-saturation region.



3. Density. At a junction temperature of 25°C (a), large current densities arise in a bipolar power transistor if the open-emitter collector-base breakdown voltage, BV_{CBO} , is the limiting factor. If the open-base sustaining collector-emitter voltage, $V_{CEO(sus)}$, is the limit, current density is reduced by a factor of five. At 125°C (b), a bipolar transistor's behavior changes little, but a MOS FET's changes by a factor of two.

A comparison of current density (J_{on}) for MOS FETs and bipolar power devices can be made by calculating the average current density in the on-state for different on-state voltages. For the MOS FET, the calculation is relatively simple. For each BV_{DS} , an optimum n-region thickness and doping concentration exist for a minimum on-resistance. A plot of current density versus voltage for BV_{DS} equal to 450 volts for a MOS FET is shown in Fig. 3. The slope of the line corresponds to a minimum on-resistance, which in this case is 27 milliohms for an area of 1 square centimeter. The plot is taken with the MOS FET's junction temperature at 25°C.

For bipolar power transistors, calculations involve assumptions of current gain. For the curve shown in Fig. 3, an h_{FE} of 10 at a transistor junction temperature of 25°C is assumed. Since the product of h_{FE} and I_C is constant at large currents, adjustments to other h_{FE} values can be made by appropriately scaling the vertical axis of the curve in Fig. 3.

The bipolar curves are calculated for two different designs: with $V_{CEO(sus)}$ equal to 450 v and with BV_{CBO} equal to 450 v. At low voltages, J_{on} is largely determined by the contact resistance of the emitter metalization, whose resistivity value of 3.5 mΩ-cm² is used here.

Note that large values of J_{on} (more than 300 amperes per square centimeter) are possible if BV_{CBO} is the limiting voltage. On the other hand, should $V_{CEO(sus)}$ be the limit, J_{on} is reduced by a factor of five. In that case, a higher current density can be achieved for MOS FETs with on-voltages of 1.5 v or more.

Taking the heat

Increasing a power transistor's junction temperature from 25° to 125°C results in a minor change of the bipolar devices' current-density curves and greater changes for the MOS FET's J_{on} curve. The reason is that the MOS FET's on-resistance increases by a factor of two as a result of the temperature dependence of electron mobility; this behavior means that MOS FET conduction losses increase with temperature, whereas those of bipolar power transistors remain approximately constant—a fact that is often overlooked when comparing the two types of transistor.

Although the example in Fig. 3 is shown for a blocking

potential of 450 v, the relative spacing of the curves for the MOS FET and the bipolar transistors remains fixed for higher blocking voltages, save for the classical saturation voltage. This is because the respective on-current density for both devices increases approximately as $V_{CEO(sus)}$ and BV_{DS} raised to the power of 2.3.

Figure 4 shows power loss as a function of switching frequency for both types of device at a transistor junction temperature of 25°C. Note that at low frequencies, where conduction losses are dominant, a bipolar transistor has about one third the power loss of a MOS FET. This ratio corresponds to the ratio of a bipolar power transistor's on-resistivity to a MOS FET's. The base input power is included in these plots.

As switching frequency is increased, the switching losses of a bipolar power transistor increase at a faster rate than those of a MOS FET, crossing at about 15 kHz. Beyond this frequency, where switching losses dominate, a MOS FET has about a 3:1 advantage over a bipolar power transistor in terms of the amount of power dissipation per unit area.

Heating up

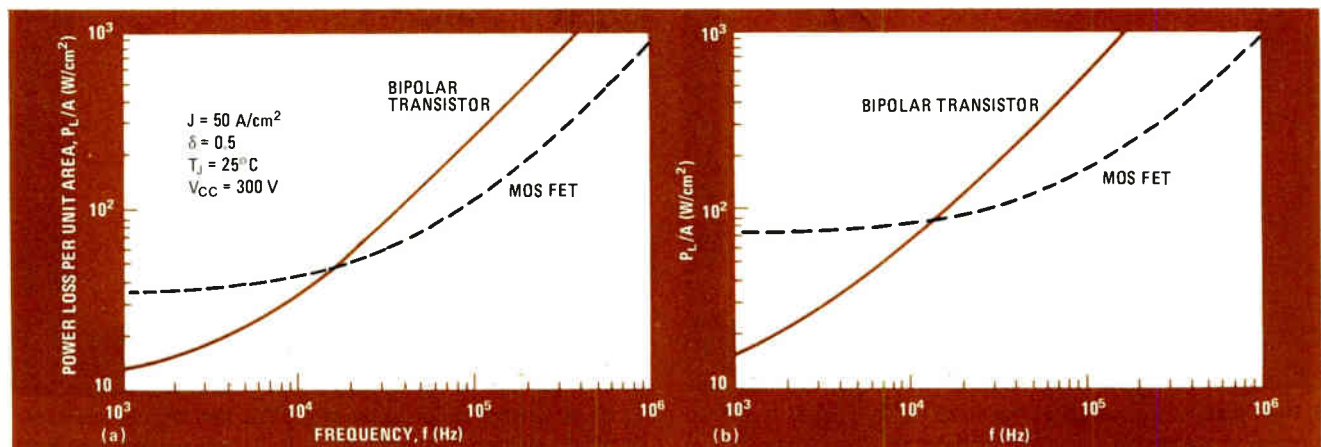
At a transistor junction temperature of 125°C, power-loss curves for both devices take on a different look. At low frequencies, the MOS FET's power losses increase even further than at 25°C, whereas those of the bipolar power transistor remain the same, further widening the bipolar transistor's advantage. However, switching losses for a bipolar power transistor increase even more rapidly with increasing frequency, again crossing over with the MOS FET's power-loss curve at about 15 kHz. At higher frequencies, the MOS FET's advantage climbs to a 6:1 ratio in terms of power loss per unit area.

The curves in Fig. 4 do not account for the practical case where heat removal becomes an important factor. In this case, the assumption of constant junction temperature may be misleading.

To account for heat flow to the ambient, a fixed thermal resistance can be assumed:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta HS}$$

where $R_{\theta JA}$ is the fixed thermal resistance, $R_{\theta JC}$ is the transistor's junction-to-case thermal resistance, and $R_{\theta HS}$



4. Power loss. At a junction temperature of 25°C (a), power loss per unit area for a bipolar transistor is one third that of a MOS field-effect transistor's at under 15 kHz. Above that frequency, the ratio reverses. Above 125°C (b), the ratio between the two is even greater.

BIPOLAR VS MOS FET

is the effective thermal resistance of the heat sink.

A reasonable value for $R_{\theta JC}$ is approximately $0.2^\circ\text{C}/\text{watt}$, assuming a 1-cm^2 area and a heat-flow cross-sectional area of 2 cm^2 . This value can be verified with a conventional TO-3 package having sides of 236 mils each and a die 6 millimeters on a side.

Reasonable values

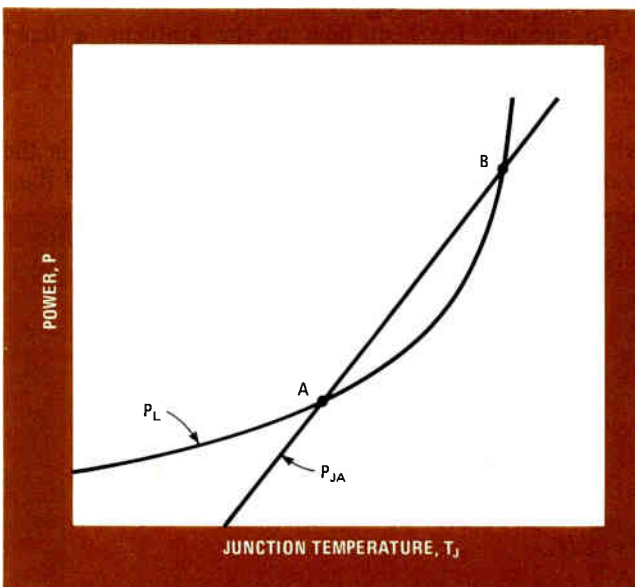
Such a package has a value for $R_{\theta JC}$ of $1.1^\circ\text{C}/\text{W}$, which is in line with the value of $0.2^\circ\text{C}/\text{W}$ cited above. $R_{\theta HS}$ is assumed to have a unit area value of about $0.3^\circ\text{C}/\text{W}$, a reasonable value with moderate-sized air-cooled heat sinks.

Heat loss to the ambient, P_{JA} , obeys the equation:

$$T_J - T_A = P_{JA} (R_{\theta JC} + R_{\theta HS}) = P_{JA} R_{\theta JA}$$

where T_J equals the junction temperature and T_A the ambient temperature.

Figure 5 shows P_{JA} as a linear function of T_J . This heat-loss-to-the-ambient curve intersects the power-loss curve at two points, A and B. Two other possibilities exist: no intersecting of the two curves or a tangential solution, where the power loss (P_L) is equal to P_{JA} at only one point. Neither of these possibilities can be consid-



5. Heat loss. In any transistor, heat loss to the ambient is a linear function of the device's junction temperature. The heat-loss curve intersects the power-loss curve at two points, only one of which (point A) is useful for calculating total device power losses.

ered, however, since thermal runaway will occur in either case.

It is well known from a simple heat-flow argument that point A will be thermally stable, whereas point B will not. It should therefore be understood that calculations of maximum power limits for different values of $R_{\theta JA}$ and T_A using data from point B are impractical.

The safe operating frequency

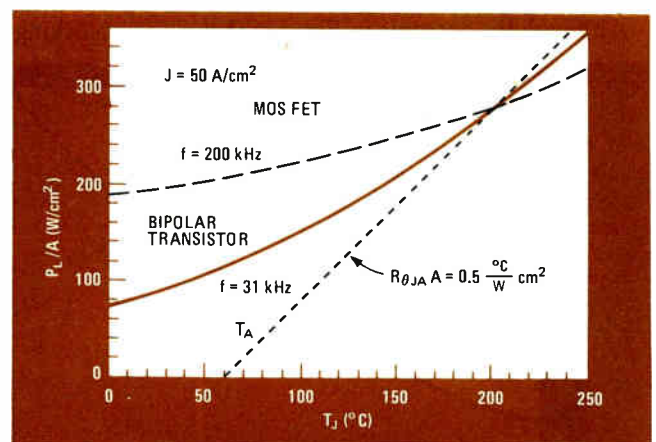
Figure 6 illustrates the case where the operating frequency (f) is selected to give a power loss equal to the heat loss to the ambient ($P_L = P_{JA}$) at a transistor junction temperature of 200°C for an assumed unit-area fixed thermal resistance ($AR_{\theta JA}$) of $0.5^\circ\text{C}\text{-cm}^2/\text{W}$. The 200°C temperature is typically used as a minimum value for silicon devices having a leakage-current limitation. As can be seen from the graph, both bipolar devices and MOS FETs are thermally stable—that is, they are of the A type in Fig. 5.

The frequency for which the junction temperature is a maximum at $P_L = P_{JA}$ is defined as the maximum safe operating frequency. Plotting current density as a function of this safe operating frequency for both bipolar devices and MOS FETs would reveal a higher current-density value for the former at frequencies under 15 kHz and a lower one at frequencies above that. At 15 kHz, the curves for both devices intersect.

For frequencies below 1 kHz, bipolar power transistors have better than a 2:1 advantage in current- and power-handling capability over MOS FETs. On the other hand, at a frequency greater than 100 kHz, MOS FETs retain at least a 2:1 advantage in this capability.

Possible trends

These calculations have been based on theoretical estimates and measurements on actual devices. As device technologies improve, changes in the switching losses per unit area can be expected. However, conduction losses are already close to theoretical limits and are unlikely to change. Thus the high-frequency portions of Fig. 4 will shift with technological advances, whereas the left-hand portions will remain fixed. □



6. Safe. At junction temperatures of 200°C or less, the maximum safe operating switching frequency for a bipolar power transistor is 31 kHz, whereas that of a MOS FET is a much higher 200 kHz. This maximum occurs at the point at which power loss equals heat loss.

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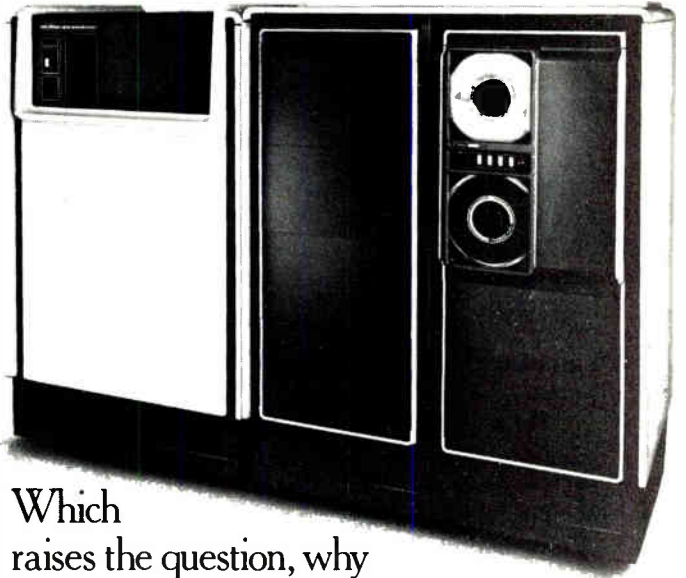
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*Fortran 77, Cobol, Basic, PL/I and RPG II

Hall compass points digitally to headings

by Gary Steinbaugh
Owens/Corning Fiberglas Corp., Technical Center, Granville, Ohio

Although the time-honored needle-type magnetic compass is very simple, inexpensive, and most efficient in terms of power consumption, two Hall-effect sensors and a few chips can be combined to make a compass with some important advantages of its own. Among them are direct digital readout of the magnetic heading, remote-sensing capability, the ability to interface with navigational computers, and the elimination of errors caused by acceleration or tuning of the body to which the compass is secured.

The general block diagram of such an instrument is shown in Fig. 1. Here, a 36-kilohertz system clock advances a 360-step counter, which in turn drives a sine and cosine digital-to-analog converter. The resulting 100-hertz outputs from the converter, $E \sin \omega t$ and $E \cos \omega t$, are then transformed into a current and introduced to the Hall-effect sensors, which are placed at right angles to each other. As a result, the output voltage of the west-east sensor is $kIB \sin \omega t \sin \theta$, and that of the north-south sensor $kIB \cos \omega t \cos \theta$, where I is the current corresponding to input voltage E , B is the strength of the incoming magnetic field, and θ is the angle of the field as measured with respect to the earth's magnetic north pole.

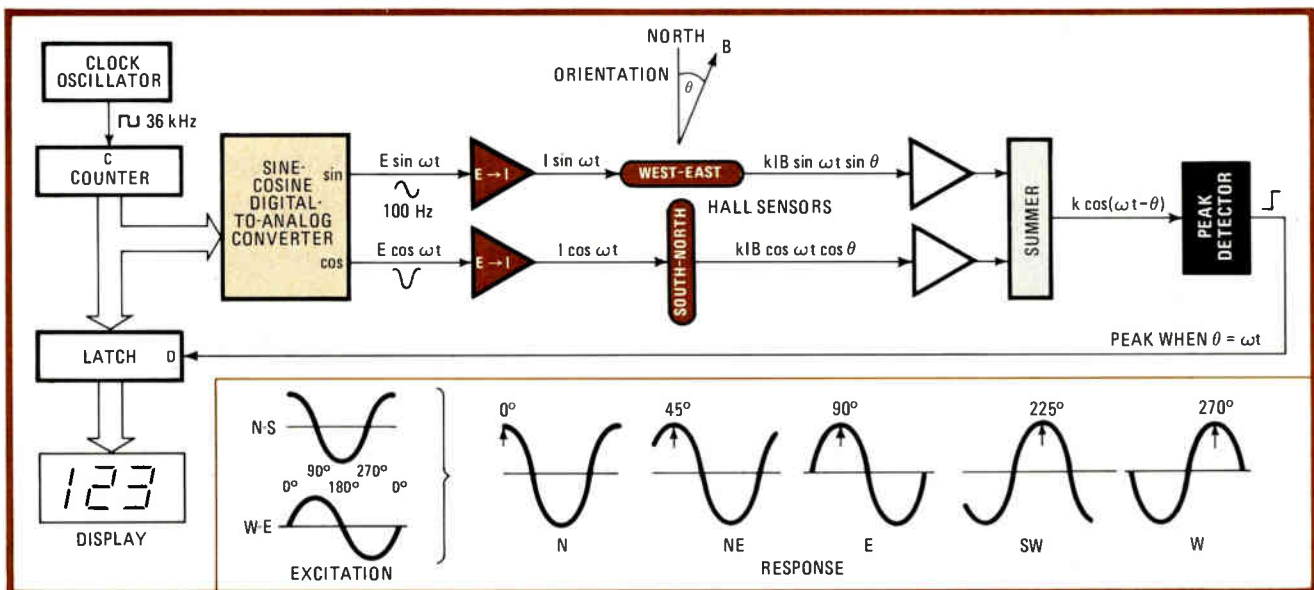
These two signals are then summed, with the result

being $kIB \cos(\omega t - \theta)$. As seen, this voltage reaches its maximum value when $\theta = \omega t$. The peak is detected and used to latch the contents of the stepped counter at that instant, yielding an indication of the bearing θ (see excitation-response curves for several representative headings).

Figure 2 shows examples of how the individual building blocks of the system may be implemented. The sine and cosine converter (Fig. 2a) has a rather low resolution, but it is easily constructed and may be sufficient for simple applications. For 1° resolution, the designer is advised to use a microprocessor-based system, using lookup tables stored in read-only memory to drive two conventional d-a converters.

The voltage-to-current amplifier block may be combined with a special Hall sensor as shown in Fig. 2b to provide superior performance. Of particular interest is the F. W. Bell BH-850 flux-concentrating Hall-effect device, which will provide ± 10 millivolts for a nominal $\pm 1/2$ gauss field (typical of the magnetic field encountered in North America), and an excitation current of 200 mA. This performance is far superior to that of the standard sensor, which will generate potentials only in the microvolt region for the same magnetic field strength. Although post-amplification with such a standard sensor is feasible, in practice the flux-concentrator type provides more linear performance and generates less noise.

The input and output leads of each Hall device must be fully isolated from each other for proper operation; this is best achieved by operating the device in the floating mode and using a differential amplifier (Fig. 2c). The input and output impedances of the Hall-effect sensors are low, and therefore a high-input impedance



1. Heading north? Flux-concentrating Hall sensors in west-to-east and north-to-south orientation, when suitably driven by $\sin \omega t$ and $\cos \omega t$ sources, combine to indicate magnetic heading. When bearing $\theta = \omega t$, peak detector latches counter to provide digital readout of θ .

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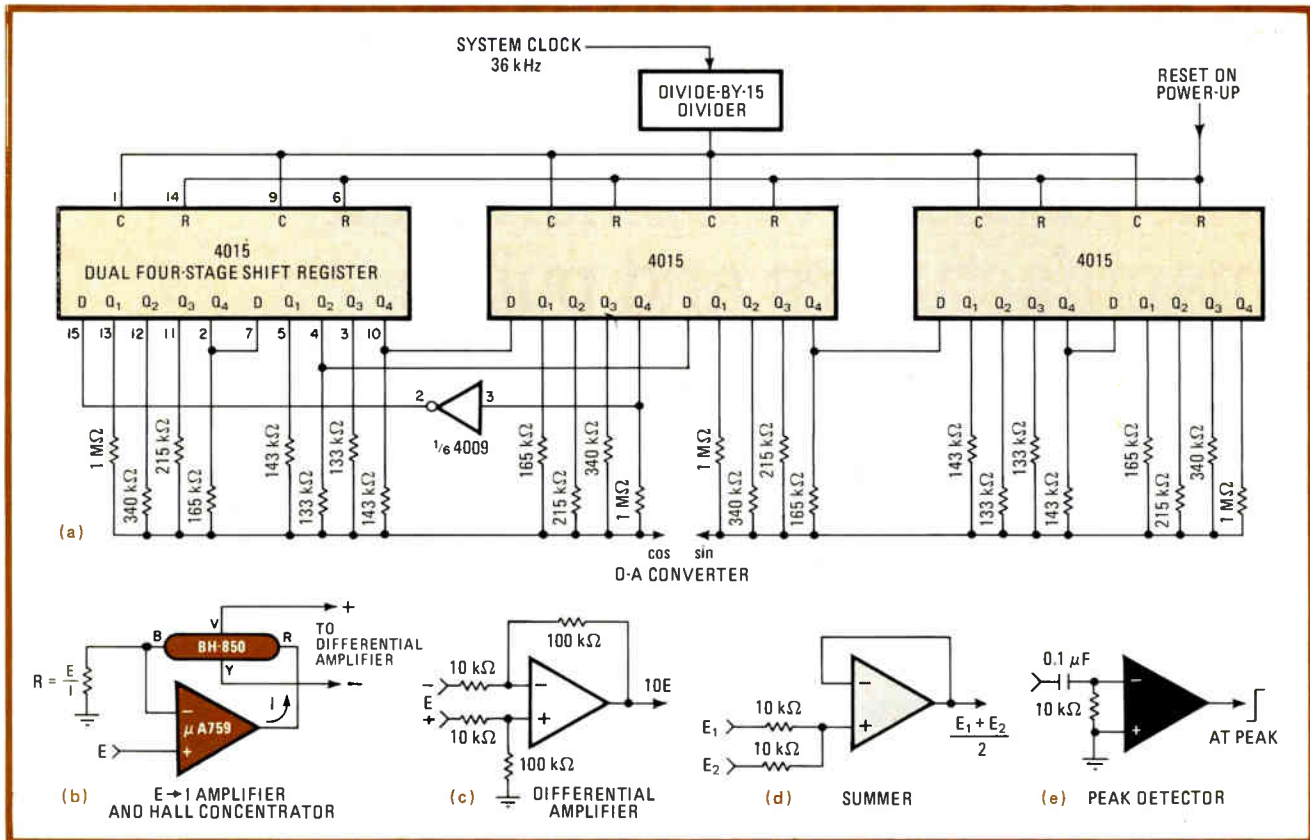
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2. Implementation. Shift-register-type counters implement circuit's sine and cosine generators (a). Sensor and voltage-to-current amplifier may be united on one stage (b), with differential amplifiers (c) following. Summer (d) and peak detector (e) are conventional.

amplifier is not required, although the amplifier's common-mode rejection should be high. A factory-trimmed instrumentation amplifier is recommended.

The summer (Fig. 2d) and peak-detector (Fig. 2e) circuits are straightforward. Note that the peak detector is actually a differentiator and zero-crossing circuit and does not hold the peak voltage level as conventional detectors do.

In operation, the sensors should remain parallel to the

earth's surface. In mobile applications, a gyroscopic platform may be required or another sensor used to permit measurement updates when the instrument passes through its level position. In fact, a third Hall sensor can be mounted perpendicular to the first two and its output used to correct the measured values for any tilt. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

Calculator notes

Codec program compands samples for μ-law simulation

by Clive McCarthy
Northern Telecom Inc., Santa Clara, Calif.

Simulating the operation of a pulse-code-modulation encoder that conforms to the industry-standard μ-255 companding law, this TI-59 program will be useful to telecommunications engineers who design or test codec circuits. The 476-step program has been designed so that it is especially easy to use.

Given a sinusoidal input signal of any amplitude, phase, and frequency, the program finds the corresponding binary output data from the following standard

approximation of a logarithmic compression curve:

$$F(x) = \text{Sgn}(x) \frac{\ln(1 + \mu|x|)}{\ln(1 + \mu)} \quad 0 \leq |x| \leq 1$$

where x = the input signal, $\text{Sgn}(x)$ = the sign of the input signal, and $\mu = 255$ for the 15-segment curve, each of whose segments has 16 steps.

A sampling rate of 8 kilohertz is assumed for solving the equation. The corresponding output data, displayed as a logic 1 or 0, with the sign bit to the left of a decimal point and the chord and step bits to the right, may be examined byte by byte or, alternatively, as a continuous stream of data if the calculator's optional PC-100 printer is available.

As an example, consider the case where an input signal at 2,600 hertz having an amplitude of 0 dBm (the zero reference digital-milliwatt level for the data channel) and a phase angle of 117° is to be sampled. Keying

Loca- tion	Key	052	PRD	106	EXC	160	GTO	214	STO	268	GE	322	0	376	X	430	÷
000	LBL	053	06	107	OP	161	LST	215	19	269	X	323	0	377	RCL	431	2
001	A	054	2	108	27	162	LBL	216	1	270	÷	324	=	378	04	432	0
002	STO	055	INV	109	LBL	163	\sqrt{x}	217	1	271	2	325	+	379	÷	433	=
003	01	057	09	111	—	165	1	219	GTO	272	5	326	RCL	380	2	434	INV
004	X	058	GTO	112	1	166	2	220	LST	273	6	327	07	381	÷	435	LOG
005	.	059	DMS	113	=	167	8	221	LBL	274	=	328	=	382	2	436	X
006	0	060	LBL	114	GE	168	=	222	—	276	19	330	07	384	=	438	1
007	4	061	—	115	X=T	169	GE	223	1	277	CLR	331	RTN	385	INV	439	5
008	5	062	RCL	116	1	170	1/X	224	0	278	LBL	332	LBL	386	FIX	440	9
009	=	063	09	117	6	171	÷	225	2	279	LST	333	E	387	RTN	441	=
010	EXC	064	INV	118	+/-	172	8	226	4	280	STO	334	OP	388	LBL	442	EXC
011	01	065	SUM	119	STO	173	=	227	=	281	20	335	25	389	C'	443	02
012	INV	066	08	120	19	174	STO	228	GE	282	.	336	(390	X	444	INV
013	FIX	067	GTO	121	1	175	19	229	SUM	283	0	337	RCL	391	2	445	FIX
014	R/S	068	.	122	1	176	1	230	÷	284	0	338	05	392	\sqrt{x}	446	R/S
015	LBL	069	LBL	123	1	177	0	231	6	285	0	339	INT	393	X	447	LBL
016	E'	070	=	124	GTO	178	1	232	4	286	1	340	X	394	2	448	C
017	INT	071	RCL	125	LST	179	GTO	233	=	287	STO	341	RCL	395	÷	449	STO
018	STO	072	20	126	LBL	180	LST	234	STO	288	06	342	01	396	RCL	450	02
019	00	073	÷	127	X=T	181	LBL	235	19	289	4	343)	397	04	451	X
020	INV	074	1	128	—	182	1/X	236	1	290	STO	344	+	398	=	452	2
021	FIX	075	0	129	3	183	—	237	0	291	0	345	RCL	399	LOG	453	\sqrt{x}
022	R/S	076	0	130	0	184	2	238	GTO	292	8	346	03	400	X	454	X
023	LBL	077	0	131	=	185	5	239	LST	293	STO	347	=	401	2	455	1
024	A'	078	=	132	GE	186	6	240	LBL	294	08	348	SIN	402	0	456	6
025	STO	079	+	133	X ²	187	=	241	SUM	295	(349	X	403	=	457	3
026	03	080	RCL	134	=	188	GE	242	—	296	1	350	RCL	404	+	458	1
027	INV	081	07	135	2	189	STO	243	2	297	÷	351	02	405	3	459	8
028	FIX	082	—	136	=	190	÷	244	0	298	9	352	=	406	.	460	÷
029	R/S	083	RCL	137	STO	191	1	245	4	299	0	353	NOP	407	1	461	RCL
030	LBL	084	06	138	19	192	6	246	8	300	0	354	SBR	408	7	462	04
031	DMS	085	=	139	1	193	=	247	=	301	0	355	IFF	409	=	463	=
032	RCL	086	FIX	140	1	194	STO	248	GE	302)	356	PAU	410	INV	464	EXC
033	08	087	07	141	1	195	19	249	Y ^X	303	SUM	357	PRT	411	FIX	465	02
034	EQ	088	RTN	142	GTO	196	1	250	÷	304	07	358	DSZ	412	RTN	466	INV
035	=	089	LBL	143	LST	197	0	251	1	305	RCL	359	00	413	LBL	467	FIX
036	GE	090	D	144	LBL	198	0	252	2	306	19	360	E	414	D'	468	R/S
037	—	091	RCL	145	X ²	199	GTO	253	8	307	+	361	R/S	415	STO	469	LBL
038	RCL	092	02	146	—	200	LST	254	=	308	1	362	LBL	416	04	470	IXI
039	09	093	LBL	147	6	201	LBL	255	STO	309	6	363	B'	417	INV	471	RCL
040	SUM	094	IFF	148	4	202	STO	256	19	310	=	364	—	418	FIX	472	07
041	08	095	X=T	149	=	203	—	257	1	311	INT	365	3	419	R/S	473	FIX
042	RCL	096	CLR	150	GE	204	5	258	GTO	312	X=T	366	.	420	LBL	474	07
043	06	097	STO	151	\sqrt{x}	205	1	259	LST	313	CLR	367	1	421	B	475	RTN
044	INV	098	07	152	÷	206	2	260	LBL	314	INV	368	7	422	STO	476	0
045	SUM	099	X=T	153	4	207	=	261	Y ^X	315	EQ	369	=	423	02	.	.
046	07	100	GE	154	=	208	GE	262	—	316	DMS	370	÷	424	—	.	.
047	LBL	101	EXC	155	STO	209	RCL	263	4	317	RCL	371	2	425	3	.	.
048	.	102	+/-	156	19	210	÷	264	0	318	20	372	0	426	.	.	.
049	1	103	GTO	157	1	211	3	265	9	319	÷	373	=	427	7	.	.
050	0	104	PRD	158	1	212	2	266	6	320	1	374	INV	428	7	.	.
051	INV	105	LBL	159	0	213	=	267	=	321	0	375	LOG	429	=	.	.

Instructions

- Key in program
 - Enter frequency of modulating signal to be encoded:
(f), A
 - Specify the signal's amplitude (dBm₀ or V_{rms}) and phase angle (°):
(A), B (φ), A'
- If amplitude is expressed in V_{rms}, the peak-to-peak reference level must also be entered in register D'. Values of dBm₀ placed in register B' will be converted into V_{rms} values. Conversely, V_{rms} quantities placed in register C' will be converted into dBm₀ values.
- Calculate the digital value of each byte:
Press E' for each byte (assuming no PC-100 printer). Press E', E to allow PC-100 to print the entire data stream automatically. PCM format has sign bit to the left of the decimal point and the chord and step bits to the right.
 - Press D to find the peak value of the PCM input signal

Sine-wave coding

0.0001101
0.0110011
1.0001010
0.0010000
0.0100100
1.0001010
0.0010101
0.0011011
1.0001001
0.0011011
0.0010101
1.0001010
0.0100100
:
:

f = 2,600 Hz
f_s = 8,000 Hz
φ = 117°

in the required data as specified in the instructions yields the data tabulated to the right of the instructions in the program listing. Note that with a sampling rate of 8 kHz, modulating frequencies should be kept below 4 kHz in order to meet the Nyquist criteria.

As seen by inspection, or alternately by pressing the D key, the peak positive value of the signal is 1.001001. Note that the chord-step information is expressed in inverted binary code, which is the industry-accepted standard. □

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The call is out to industry, university, and government computer specialists, as well as students, to compete in the first national search for ideas and inventions that will employ personal computing technology to aid the handicapped in learning, working, and adapting to home and community settings. The search is being conducted by the Applied Physics Laboratory of Johns Hopkins University, with the National Science Foundation and Radio Shack, a division of Tandy Corp., as cosponsors. **One hundred awards, among them a \$10,000 grand prize**, other cash prizes, and personal computer equipment, including training, will be presented to winners next fall at a Washington, D. C., banquet. Contestants have until June 30 to submit entries. For additional information, including applications, write to Personal Computing to Aid the Handicapped, Johns Hopkins University, P. O. Box 670, Laurel, Md. 20810.

Predicting the future for pc boards

What form will the printed-circuit board take in the coming years? A recently completed 250-page report by BPA (Management Services) attempts to answer the question. It covers such topics as high-density pc boards; discrete wiring, including stitch wiring, Multiwire, and Solder-Wrap; technologies and materials for increased density; and new packages and planar mounting. The section on technologies for increased density is particularly interesting, with complete descriptions of Lampac, porcelain-enameled steel, thick films, and polymer thick films. The report, which sells in the U. S. for \$5,200, **concludes with an analysis of the Western European market for high-density interconnections**, particularly multi-layer pc boards. For information in the U. S., write to James Welterlen, Suite 8, 7460 Girard Ave., La Jolla, Calif. 92037. In Europe, contact BPA (Management Services), Concept House, Dene Street, Dorking, Surrey RH4 2DR, England.

Are DIPs' lead size specs now outmoded?

Nowadays more than 20% of all dual in-line packages on printed-circuit boards are socketed. Yet the basic DIP was designed on the assumption that it would be permanently soldered into plated through-holes on a pc board. Consequently, a very broad lead size specification was developed that is no longer suitable for socketed applications. Dick Grubb, corporate vice president of marketing of Augat Inc., Attleboro, Mass., notes, "The IC leads of a DIP, especially in the case where a DIP is socketed, should be considered as the mating half of a connector."

Dick points out that the dimensions on the socket half are tightly held (in many cases to ± 0.0002 in.). The present Joint Electron Device Engineering Council specification is 0.015 to 0.023 in. for the lead width, 0.008 to 0.015 in. for the lead thickness, and 0.100 in. minimum for the lead length. Mating a socket with, say, ± 0.0002 -in. tolerances to a DIP's leads having much wider tolerances **subjects the insertion force, withdrawal force, and contact resistance of sockets to unnecessarily wide variations**. Grubb's solution would be to amend Jedec's integrated-circuit lead specification to 0.018 ± 0.002 in. wide by 0.011 ± 0.002 in. thick, with a length of 0.110 to 0.130 in. A broad sampling conducted by Augat indicates that over 95% of all DIP leads actually fall within this range. Thus the revised spec would not penalize IC and lead-frame firms and would save much time, effort, and cost for producer and user alike. **-Jerry Lyman**

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Circle 117 on reader service card

Roundup: 16-K byte-wide RAMs abound

With 2-K-by-8-bit static random-access memories now appearing in n-MOS and C-MOS versions, a sizable market is inevitable

by John G. Posa, Solid State Editor

Despite the tumult over the 64-K dynamic random-access memory, a growing uproar can be heard from the byte-wide 16-K static RAM marketplace. To be sure, there will be noisy clashes among makers of high-speed by-1-bit and by-4-bit organizations; but many more contestants will battle for a share of a potentially larger market for the 2-K-by-8-bit configuration.

In fact, over a dozen U. S. and Japanese manufacturers will offer 2-K-by-8-bit static RAMs built with scaled-down 3- μ m n-channel and complementary-MOS processes. As the table shows, some companies will sell both n- and C-MOS versions to

meet low-cost and low-power needs, respectively. In general, the Japanese are starting off with C-MOS and going on to n-MOS units, whereas the U. S. is beginning with n-MOS devices and will add C-MOS types as expertise allows.

The attractions of the new device are many. Of course, with cells smaller than those in previous static RAMs, cost per bit will be diminished. But in addition, as easy to use as static RAMs are, the new chips—being organized in bytes—will be even easier to interface with.

Unlike 4-K parts, the 2-K-by-8-bit RAMs are being packaged for pin-out compatibility with byte-wide read-

only memories like the 24-pin 2716 erasable programmable ROM. Thus, in a microprocessor system, if sections of RAM for data must be swapped for areas of program memory, this could be as simple as exchanging two chips. Also, if an application requires only 2- or 4-K bytes of RAM, the designer can get by with only one or two chips instead of the four or eight needed if 4-K RAMs are used. Thus, board area and power consumption, too, are minimized.

The table shows only devices now in production or slated for production by mid-1981. Motorola will bring out a C-MOS counterpart by

2-K-BY-8-BIT STATIC RANDOM-ACCESS MEMORIES

	N-channel MOS					
Company	Mitsubishi	Mostek	Motorola	Oki	Texas Instruments	Toshiba
Part number	M58725P	MK4802	MCM4016	MSM 2128-1	TMS 4016	TMM 2016P
Cell pull-up device	second-level polysilicon resistor	polysilicon resistor tied to data line	second-level polysilicon resistor	first-level polysilicon resistor	second-level polysilicon resistor	second-level polysilicon resistor
Cell area (mil ²)	1.52	1.3	1.0	1.89	≈ 1.5	1.42
Chip area (mil ²)	43,245	35,748	30,380	46,330	≈ 45,000	36,650
Access time (ns)	150/200	55 ^a /70 ^a /90 120/200	120 ^a /150 200/250	200	150 ^b / 250-450	100/150
Current consumption, active/standby (mA)	80 10	125 0.1 ^b	80 15	120 no	100 no	100-120 15
Package	24-pin standard	24-pin standard	24-pin standard	24-pin standard	24-pin standard	24-pin standard
Availability or current pricing	in production	for 100 units, 90-ns \$115.10; 120-ns \$65.50; 200-ns \$56.50	first half, 1981	for 1-24 units, \$105.60; 25-99 \$87.00; 100-999, \$72.00	fourth quarter, 1980	in production

^aFuture specification.

^bWith low-power Datasave option.

^cJunction field-effect transistor.

^dOutput enable.

^eTypical specification.

the third quarter of next year, and Texas Instruments is also considering a C-MOS spin-off. So is Mostek, but for a higher-density RAM.

Mitsubishi has described an n-channel device not listed in the table, and Nippon Electric is known to be sitting on both n- and C-MOS memories. In talking of its pin-out plan for byte-wide memories, Intel has alluded to a 2-K-byte static device, and its new C-MOS process [*Electronics*, Dec. 4, p. 39] might be just the thing.

Michael Bolan, strategic marketing manager for byte-wide memory products at Mostek, sees the 2-K-byte static RAM market as "the biggest next to the 64-K dynamic RAM's for 1981." Mostek has the capacity to build over 5 million of its MK4802s next year alone. David Ford, manager of MOS memory marketing at Motorola, puts the 1981 market for such parts at \$80 million to \$90 million, adding that it will "probably double in 1982 and then increase by at least 10% per year for the next four years."

At Hitachi America, product marketing manager Jack Mattis calls the

2-K-by-8-bit static RAM market simply "huge." He says the memory will become "the static RAM for most microprocessor systems," with the industry delivering "400,000 to 500,000 units per month by the middle of 1981 and a total of 20 million units in 1982."

As for average selling price per chip, Motorola's Ford predicts it will be in the \$30 to \$40 range for next year and around \$20 to \$30 in 1982. In his view, "customers are expecting to pay about 20% more for C-MOS versions" of the chips. But Bruce Grieshaber, product marketing manager of C-MOS chips at Harris Semiconductor, says that C-MOS could garner a premium of 30%.

Introductory pricing of the devices is in the \$75 ball park for nominal speeds and lots over 100. These will primarily replace smaller static RAMs like the 1-K-by-4-bit 2114. By about the first quarter of 1982, Mostek's 4802 will start to compete with its 8-K 4118 on a cost-per-bit basis, says Bolan. Thus, conservatively speaking, slower 2-K-by-8-bit parts "will become cost-effective on a per-bit basis by the first half of 1982."

Of course, long before that time, customers will snap up the parts to minimize printed-circuit board area requirements and to slash system power dissipation over 4- and 8-K chips. The speed of the devices will be more than adequate, because "the fastest microprocessor needs an access time of no less than about 200 ns," comments Hitachi's Mattis, and many of the chips exhibit delays of only 120 or 100 ns.

Indeed, Mostek's 70-ns 4802, which will eventually also have 55-ns speeds, is fast enough to compete for both MOS and bipolar applications. To arrive at this performance, the firm butts two high-speed 8-K RAMs together on an oblong die [*Electronics*, July 3, p. 175].

Power differences. Most pronounced of all, however, will be the differences in power dissipation of the chips and the schemes used to lower it. The majority of the devices, with the exception of the n-MOS TMS 4016 from Texas Instruments and the MSM 2128 from Oki, will feature a power-down mode controlled via the chip-enable (\overline{CE}) pin. Both companies are working on enhanced n-channel chips, though interestingly, TI will move away from its double-level polysilicon process to a single level, whereas Oki will go from one level to two.

The n-channel chips, drawing about 100 mA during active operation, will use from 5 to 50 mA on standby. C-MOS versions will consume much less active current—in the 40-to-50-mA range—but the user should always read between the lines on the data sheet. Some companies highlight superior typical specifications, especially those relating to power consumption, and hide maximum numbers.

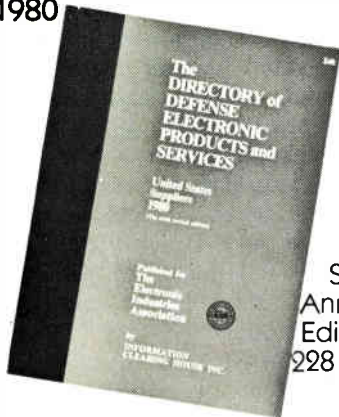
In addition, C-MOS devices usually go by two sets of numbers for power usage, depending upon input levels. Hitachi's HM6116, as a case in point, specifies a typical standby power-supply current of just 20 μ A. However, that figure only applies if \overline{CE} is within 200 mV of the power-supply potential, V_{CC} , and all other input signals are as close to V_{CC} or ground. If these conditions are not

Complementary-MOS

Harris	Hitachi	Oki	Toshiba
HM6516	HM 6116	MSM 5128	TC5516AP
second-level polysilicon resistors	buried J-FET ^c	p-MOS transistor	p-MOS transistor
n.a.	1.4	2.36	1.74
54,234	40,579	55,413	45,254
240	120/150 200	150/200 300	250
10/MHz	60-80	40	40 ^e
0.5-1	0.1-15	0.02	0.2 ^e
24 pin standard	24 pin standard	24 pin standard	no \overline{OE} ^d
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New products

met, standby dissipation can go as high as 75 mW—comparable to some n-MOS versions.

But also like the n-MOS chips, Hitachi's 6116 uses polysilicon resistors as load devices in the storage array. In contrast, when a company allots the die area for p-channel pull-up transistors in the array, power dissipation can plummet. So far, two companies—Oki and Toshiba—include p-channel loads for six-transistor all-C-MOS cells. The chips have the biggest die areas, but Oki's MSM 5128, now available in sample form, can retain data with 20 μA and Toshiba's TC5516AP stays alive on a holding current of a mere 0.2 μA .

A user does have to sacrifice some flexibility to enjoy Toshiba's super-low standby consumption. As with other C-MOS chips, its inputs must be kept near the supply rails. Also, the user must activate a second $\overline{\text{CE}}$ pin on the Toshiba chip to turn off all but the storage matrix. The spare pin replaces the output-enable pin—present on all other chips—and both $\overline{\text{CE}}$ lines must be lowered for read and write operations.

Some of the n-MOS chips will minimize power consumption through dynamic circuit techniques. The use of $\overline{\text{CE}}$ to separate active and standby modes is the simplest example (this idea, used on previous lower-density memories, is often called power-gating or edge activation).

Automatic standby. Mostek is employing what it calls address activation, a power-lowering scheme it has exploited on previous memories. The chip automatically goes into a low-power standby mode if the address lines are left idle after an active cycle. But any subsequent toggling of the addresses rouses the RAM back to action. As with power-gated parts, the address activation scheme does not rule out static, fully asynchronous operation. The user need not set aside time for on-chip node precharging, so that access and cycle times coincide.

Mostek is also offering a special low-power version of the 4802 designated the 48D02 that takes advantage of a new standby mode called Datasave. An on-chip comparator

monitors the supply voltage, and when the write-enable pin ($\overline{\text{WE}}$) exceeds V_{CC} by about 1 V, the memory matrix can be powered entirely through the $\overline{\text{WE}}$ line with as little as 100 μA —a value that compares favorably with some C-MOS specifications. A low-power bias generator also kicks in when the chip is in the Datasave mode to protect voltage margins during standby.

Synchronous vs clocked. Harris takes the concept of dynamic circuitry a bit farther in its HM6516. This memory, like older C-MOS units from the company, is said to be clocked because it employs internal precharging extensively. The $\overline{\text{CE}}$ pin, which must be used to synchronize the address signals, "is a master clock, if you will," states Charles Hochstedler, product marketing engineer at Harris.

Hochstedler prefers to call the device synchronous rather than clocked because clocking connotes nonstatic operation. But he maintains that "our device is fully static in the sense that any pin can be left in any position for an indefinite period of time." In other words, the chip does not need to be refreshed like a dynamic RAM.

The relationship between $\overline{\text{CE}}$ and address information presented to Harris's chip does subtract from ease of use, but the approach also allows the user to tailor power consumption with speed. That is the reason for the curious 10-mA/MHz specification listed in the table.

Harris Semiconductor Products Division, P. O. Box 883, Melbourne, Fla. 32901 [361]
 Hitachi America Ltd., 707 W. Algonquin Rd., Arlington Hts., Ill. 60005 [362]

Mitsubishi Electronics America Ltd., 1230 Oakmead Parkway, Suite 206, Sunnyvale, Calif. 94086 [363]

Mostek Corp., 1215 W. Crosby Rd., Carrollton, Texas 75006 [364]

Motorola Semiconductor Products Inc., P. O. Box 20294, Phoenix, Ariz. 85036 [365]

Oki Semiconductor, 1333 Lawrence Expressway, Suite 401, Santa Clara, Calif. 95051 [366]

Texas Instruments Inc., P. O. Box 225012, M/S 308, Dallas, Texas 75265 [367]

Toshiba America Inc., 2151 Michelson Dr., Suite 190, Irvine, Calif. 92715 [368]

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Components

70-W regulator handles 10 A

Chip doubles current limit of IC voltage regulators, is trimmed to within $\pm 0.8\%$

Using a new integrated-circuit fabrication structure, National Semiconductor has developed a single-chip adjustable voltage regulator capable of supplying in excess of 10 A at power levels up to 70 w. Designated the LM196, the three-terminal regulator provides twice the output of the previous IC regulator at the top of the output-current scale, the firm's own LM138.

The LM196 is fabricated with National's new Moose process, which combines standard processing techniques for linear bipolar ICs with high-power discrete transistor technology [*Electronics*, Nov. 20, p. 40]. The result is high-current transistors on half the die area of those made with standard processing, plus more efficient use of silicon for gathering high currents.

Unlike most previous voltage regulators whose reference voltage is

within 3% or 4% of specification, the LM196 features on-chip trimming of the reference voltage to within $\pm 0.8\%$. "This eliminates the need for a trimming step in production environments, which is a real potential source of trouble," states Carl Nelson, staff scientist and product designer in National's advanced linear circuits design group. Simultaneously, this feature also reduces temperature drift to a typical value of $0.003\%/^{\circ}\text{C}$, compared with a typical value of $0.01\%/^{\circ}\text{C}$ for prior IC voltage regulators.

National guarantees that the LM196 will have a maximum temperature coefficient of $0.01\%/^{\circ}\text{C}$. "The Moose process makes the temperature coefficient more predictable and relatively flat," Nelson says. The 110-by-120-mil die of the LM196 (approximately the same size as the LM138 die) is large enough for National to "consume a few mils by the addition of trim pads." Earlier IC voltage regulators were not trimmed, he continues, so temperature coefficients wandered around some.

Because of the LM196's high power dissipation, National is specifying different maximum temperatures for the power transistor and control sections. Like other IC regulators, the LM196 has a control section specified for operation over the

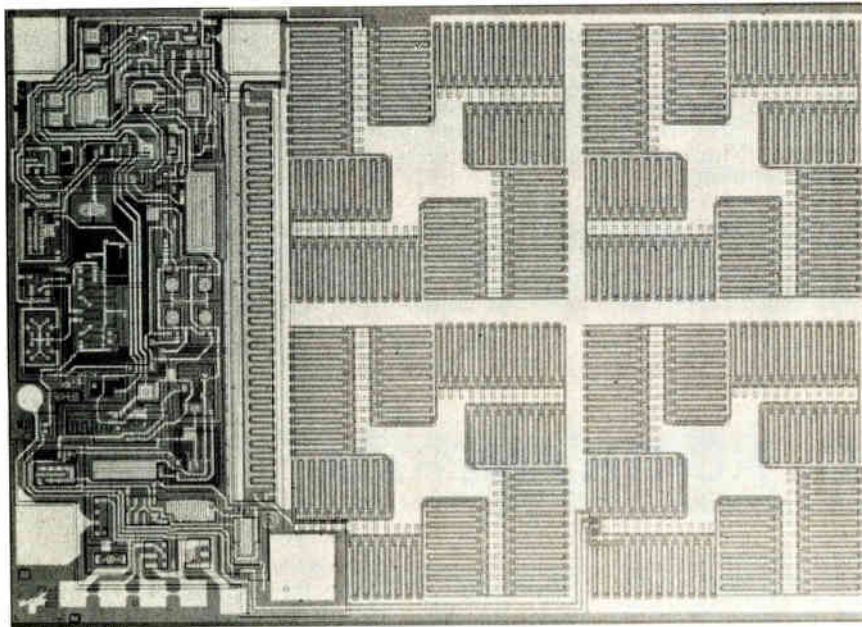
full military temperature range, -55° to $+150^{\circ}\text{C}$. "Recognizing the need for high device operating temperature when operating at elevated ambient temperature, we're specifying this new regulator for 200°C maximum junction temperature in the power transistor." This allows up to 25-w power dissipation at a case temperature of 125°C , Nelson adds, and up to 70 w can be dissipated at lower temperatures.

Safe. The LM196 features load, line, and thermal regulation to within 1% and is guaranteed to operate at a 10-A output with an input-output differential of only 2.5 v. It has all the protection features of popular lower-power adjustable regulators, including current limiting and thermal limiting, making the LM196 "immune to blowout from output overloads or shorts," even if the adjustment pin is accidentally disconnected, Nelson points out. All LM196s are burned in under thermal shutdown to guarantee proper operation of these protective features under actual overload conditions.

The output voltage of the LM196 is continuously adjustable from 1.25 to 15 v. Higher output voltages are possible if the maximum input-to-output voltage differential specification is not exceeded. A full-load current of 10 A is available at all output voltages, subject, however, to the maximum power limit of 70 w and the maximum junction temperature.

The LM196 will also be available in a commercial version specified for a 0° -to- 125°C junction temperature range for the control section and for 0° to 175°C for the power transistor. Housed in a TO-3 metal can, as is the LM196, the commercial-grade LM396 is priced at \$12.35 each in 100-piece quantities. The military-grade LM196, in like quantities, will cost about twice as much. Samples of both devices are available now, with production quantities slated to be available late this month or early January.

National will make available in 1981 two four-pin versions of the LM196. One of these will have adjustable current limiting and full output-voltage sensing capability,



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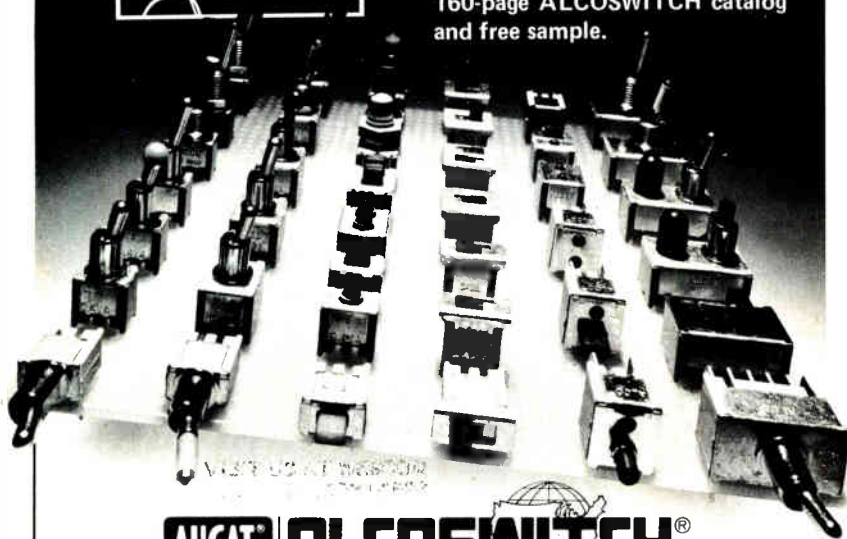


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Electronics Magazine

New products

"which a three-terminal regulator can't provide," Nelson says. The second four-pin version will be able to operate at input-output voltage differentials as low as 1 v at full load current, in addition to having output-sensing capability. Both devices will be available in TO-3 packages.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051. Phone (408) 737-5000 [341]

Converters and op amps

work at -55° to $+200^{\circ}\text{C}$

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The OPA11HT 12-MHz-bandwidth operational amplifier is specified at the wider temperature range. Input bias current is 30 nA maximum at 200°C , and the input offset voltage coefficient is $\pm 5 \mu\text{V}/^{\circ}\text{C}$ typically. The OPA12HT, on the other hand, is specified for operation at -55° to $+175^{\circ}\text{C}$. Its minimum slew rate is $80 \text{V}/\mu\text{s}$ with settling time of 200 ns typically, and its gain-bandwidth product is typically 20 MHz. Both come in TO-99 packages.

The components are slated for immediate delivery, but the company has not set their prices yet.

Burr-Brown, P. O. Box 11400, Tucson, Ariz. 85734. Phone Clay Tatom at (602) 746-1111 (344)

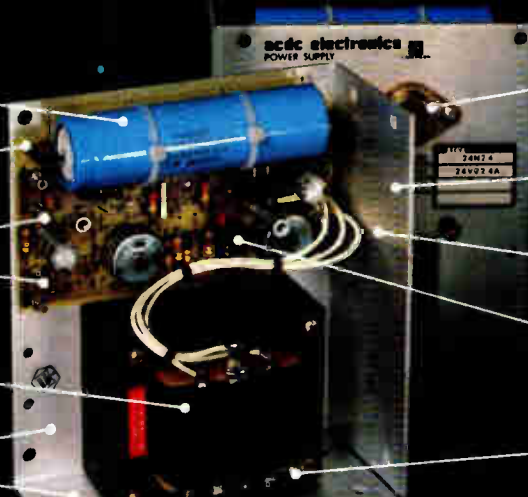
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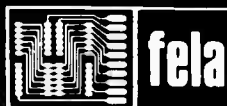
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Microwave

Analyzers cover 10 MHz to 40 GHz

Scalar network analyzers have high directivity, use desktop computer control

Using a microprocessor-controlled sweep generator for superior performance, the Wiltron 5600 network analyzers make a frontal assault on the market addressed by the Hewlett-Packard 8755P. The series is programmable via an IEEE-488 bus and is controlled by an HP 85 desktop microcomputer system, as is the HP 8755P. The HP unit, however, requires an outboard adaptor to interface with the control bus.

The six models in the series are successors to the Wiltron 5610 line. They include the 5609, which covers a frequency range of 10 MHz to 2 GHz; the 5617, which covers 10 MHz to 8 GHz; the 5647, which ranges from 10 MHz to 18 GHz; and handling the high end of the series' spectrum, the 5636 and 5640. The 5636 covers 18 to 26.5 GHz, and the 5640's range extends from 26.5 to 40 GHz.

Each system contains a scalar network analyzer, sweep generator, controller, and all required measurement components. One key feature of the 5647 system is a 40-dB directivity over its entire frequency range,

versus 26 to 38 dB for its HP counterpart. Another is its ± 10 -MHz frequency accuracy at the 18-GHz end of its spectrum. Dynamic range has also been increased by the Wiltron series, stretching to 66 dB with -55 -dBm sensitivity, compared to the 60-dB range of the HP analyzers.

Harmonics on the higher-performance members of the 5600 series are -40 dBC across the entire 2-to-20-GHz range, which compares favorably with the -25 dBC offered in the HP line. Spurious signals are down 35 dBC from 0.01 to 2 GHz and down 60 dBC on signals over 2 GHz, which compare with 25 and 50 dBC, respectively, for comparable bands on the HP 8755P.

The use of the HP-85 as a controller makes the 5600 series much simpler to operate than previous Wiltron offerings. To use the system, the operator simply inserts a preprogrammed cartridge into the controller, enters a few inputs in accordance with the interactive instructions, and then obtains computer-corrected data in tabular or graphic form.

Fundamental. The 6600 programmable sweep generator found in the Wiltron systems uses a preprocessor chip to speed and simplify the microprocessor-to-operator interface. The preprocessor separately scans and organizes all front-panel controls and displays and interfaces directly with the main microprocessor. The new sweeper also uses fundamental-frequency oscillators as a signal source rather than frequency multipliers. The result is improved specifications for harmonic output, residual

fm, and frequency accuracy.

Prices on the new line vary from \$25,520 to \$40,360. The \$40,360 model 5647 competes directly with a \$45,930 HP model 8755P. Delivery is in 90 to 120 days.

Wiltron Co., 825 E. Middlefield Rd., Mountain View, Calif. 94043. Phone (415) 969-6500 [401]

Unit generates 35-ps pulses at 10 MHz to 12 GHz

The Ailtech 95222-1 microwave impulse generator operates in a frequency range of 10 MHz to 12 GHz, with a pulse duration of approximately 35×10^{-12} s. This short pulse duration provides a broad-frequency spectral output calibrated to have an accuracy to within ± 2 dB at frequencies below 5 GHz and ± 3 dB from 5 to 12 GHz. Pulse repetition rate is 50 to 60 pulses/s, depending on power-line frequency.

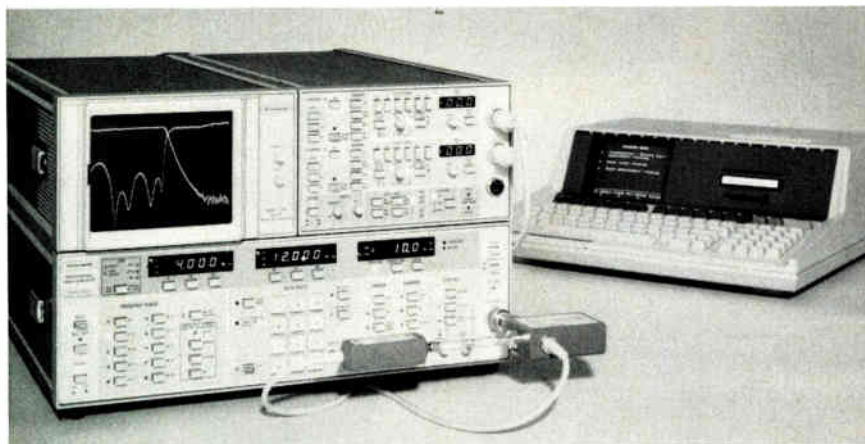
The generator is designed to provide broadband measurement capability in accordance with several military standards: MIL-1-11748 (Sig. C), MIL-1-26600 (USAF), MIL-1-6181D (USAF), and MIL-STD-461/462. It is priced at \$1,475 and can be delivered in 8 to 12 weeks.

Eaton Corp., Electronic Instrumentation Division, 5340 Alla Rd., Los Angeles, Calif. 90066. Phone (213) 822-3061 [403]

GaAs FETs handle 500-mW¹ rf input without degradation

The VSF-9320 and -9330 gallium arsenide field-effect transistors have ion-implanted channels for improved uniformity and all-gold metalization with recessed gates for increased reliability. They can handle more than 500 mW of radio-frequency input power without degradation of electrical performance.

Operating between 4 and 18 GHz, the 9320 series has typical noise figures ranging from 1.4 dB at 4 GHz to 3.0 dB at 18 GHz. At 10 GHz, the noise figure is 1.9 dB. Typical gain at 10 GHz is 10 dB, with a maximum



available gain of 12 dB. The 9330 series has slightly higher noise characteristics and lower gain.

The two devices are available as chips for use in thin-film amplifiers or in a 70-mil² hermetically sealed strip-line package. For quantities from 1 to 24, the price is \$110 each for the VSF-9320 chip and \$125 each for the VSF-9321 in the strip-line package. The VSF-9330 chips are \$65 apiece and \$75 for the VSF-9331 strip-line version. Delivery is from stock.

Varian Associates, Solid State Microwave Division, 3251 Olcott St., Santa Clara, Calif. 95050. Phone (408) 988-1331 [405]

Monitor measures radiation at 1 μ W/cm² to 20 mW/cm²

The Raham model 4A broadband isotropic radiation monitor can measure nonionizing radio-frequency power densities from levels as low as 1 μ W/cm² up to 20 mW/cm². The hand-held instrument operates over a frequency range from 200 kHz to 26 GHz with a single omnidirectional probe. It sells for \$1,495 and delivery takes 120 days.

General Microwave Corp., 155 Marine St., Farmingdale, N. Y. 11735. Phone Moe Wind at (516) 694-3600 [404]



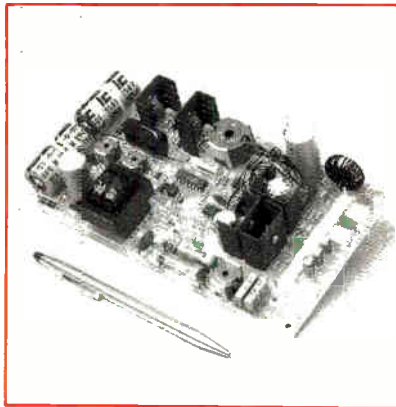
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Instruments

Unit monitors eight nodes

Cascaded one-shots are easily adjusted using real-time mode of low-cost logic analyzer

Many digital circuits require timing adjustments that can affect the operation of several successive elements. One of the more obvious examples of designs on the border line between digital and analog circuitry is a series of monostable multivibrators—one-shots—cascaded to perform complex gating functions. Adjusting the timing of one of the cascaded series often affects other parts of the circuit, and calibration, as a result, can be a tedious process of iterative adjustments.

This time-consuming process can be greatly shortened, however, with a new type of low-cost instrument developed by a startup company in Redwood City, Calif. "Using the real-time mode of our model 1010 at test sites, we have cut down the calibration time of circuits from over a half hour to just a few minutes," according to Kevin Hotvedt, founder

and president of LogaCal.

The 1010, priced at \$570 assembled and \$300 in kit form, uses an ordinary dual-trace oscilloscope to display its information. It turns the scope into a simple eight-channel logic analyzer with speeds up to 2.5 MHz and a memory of 256 bytes. But its unique feature is its real-time mode. With this mode, up to eight TTL nodes can be monitored, simultaneously and in true phase, to check responses to a single adjustment.

The instrument accomplishes this by combining the signal inputs from four traces into a single trace on the scope, with two traces representing the eight test points. The raw digital inputs from the test points are each given a different gain factor, then summed to obtain the amplitude of the trace. Inputs are not sampled, as in the logic analysis mode, but are continuously available.

On screen. "When a change in the state of the test points occurs, it shows up directly on the screen," notes Hotvedt. "Of course, the transition must be repetitive." The time from one transition to the next is then directly measurable on the scope trace. Transitions in state between different test points in the group of four test points can be distinguished, because each point gets a different scalar height factor.

To make it more obvious which

test point is switching, the 1010 has switches that can add or delete the test point signals from the display. This display allows the user to see the effects of his adjustments on eight points in the system at once. The alternative is the normal scope procedure of having to compare the analog waveforms from two test points at a time.

As a logic analyzer, the 1010 can use either an internal or external clock, and it can trigger on a rising or falling edge of either an external trigger input signal or upon the recognition of an 8-bit word. The 1010 can be set to record either all pre-trigger or all post-trigger data, but not a combination of the two. Probes are included, and they present a 10-k Ω resistance and a 30-pF capacitance to the circuit. Power is derived from the circuit under test.

Deliveries of the model 1010 are from stock to eight weeks.

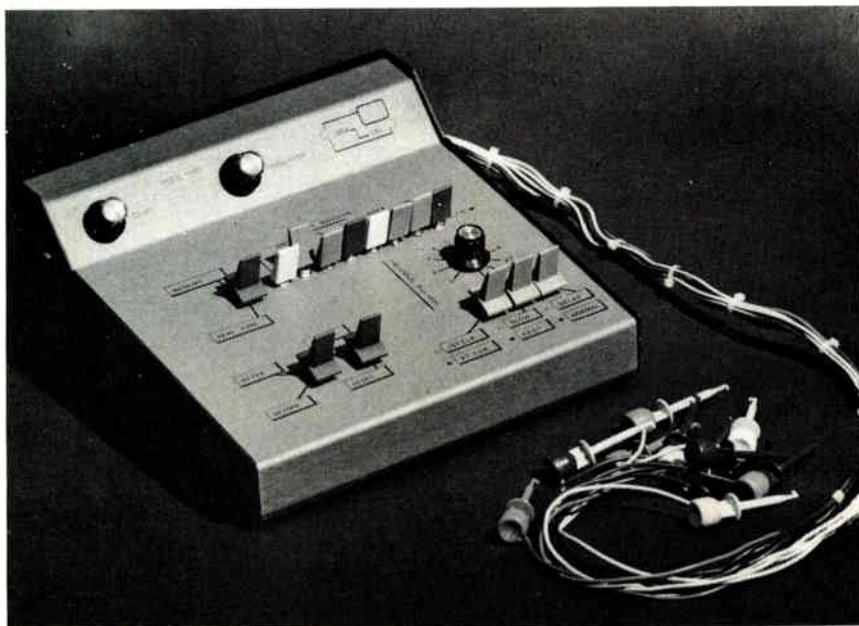
LogaCal, Box 3329, Redwood City, Calif. 94061. Phone (415) 364-5146 [351]

Automatic distortion analyzer is IEEE-488-compatible

A microprocessor-based distortion analyzer, the model 6880 is a completely automatic distortion, voltage, and frequency measurement system that is compatible with the IEEE-488 interface bus. It measures total harmonic distortion, in percentages or decibels, down to 0.003% (-90 dB), with 0.001% (0.1-dB) resolution. The instrument automatically tunes itself to the frequency of the external signal over the entire range of 1 Hz to 110 kHz. An automatic level-setting circuit presets the amplitude reference level for any input between 0.1 and 130 v root mean square. As a frequency counter, the 6880 measures and displays the fundamental input frequency from 1.000 Hz to 999 kHz. Distortion is less than 0.003% for a 1-kHz sine-wave output.

The instrument is priced at \$3,500 and is available in 90 days.

Krohn-Hite Corp., Avon Industrial Park, Avon, Mass. 02322 [355]



Microcomputers & systems

Chip controls EE-PROM bank

Microcomputer is programmed to handle subsystems having up to 32 16-K EE-PROMs

Designers with plans to incorporate Intel's forthcoming 2816 16-K electrically erasable programmable read-only memories [*Electronics*, Nov. 20, p. 50] into their products can get a leg up from the MF2801 large-scale integrated controller. Based on a popular single-chip microcomputer with a custom program in its masked ROM, it replaces as many as 40 small-scale integrated TTL packages in systems designed to read, erase, write (program), and modify (erase and write) EE-PROMs.

The 2801 takes over most of the tasks of a subsystem containing 1 to 32 of the 2816 EE-PROMs (2-K to 64-K bytes). It communicates with the host processor via an 8-bit asynchronous interface that can be set up in either a polled or an interrupt-driven configuration. Also possible is a dual-port configuration in which read cycles bypass the controller but write, erase, and modify cycles engage it.

One of the major advantages of the 2816 EE-PROM is that it can be erased and modified 1 byte at a time. The 2801 supports that capability by allowing all operations to be done either on individual bytes or on blocks of memory.

Sequence. The normal sequence of operation is for the host processor to check a status bit in the controller to make sure it is not busy and then write a command to it over the 8-bit interface. The parameters that must be passed (such as block size and the data itself) follow the command under control of a bit that notifies the host each time it is ready for the next input. When all parameters are received, the controller executes the command; it can either interrupt the host to notify it of completion or merely set a status bit to be polled by the host.

The 2801 has two on-chip buffers: one for storing input commands and parameters and another to hold output from the EE-PROMs for later transfer to the host. Several error codes, in addition to status information, are supplied to the host upon request. A novel password feature allows the user to protect the EE-PROMs from unauthorized alteration. This optional feature operates under software control; passwords may be up to 10 characters long.

The 2801 is available now for \$295. It comes in a standard 40-pin dual in-line package and runs on a

single 5-v supply.

A designer kit is also available, containing all the necessary support circuitry to implement an 8-K-byte system. A dc-dc converter is included for deriving the 24-v programming voltage from the system's 5-v supply, as are analog circuits used to deliver the programming voltage to the EE-PROMs and an Intel 8243 output-expansion port that delivers the 2801's commands to the analog circuitry. The kit, also available now, is priced at \$395.

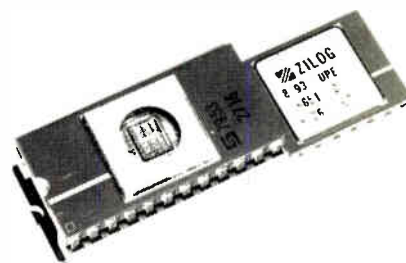
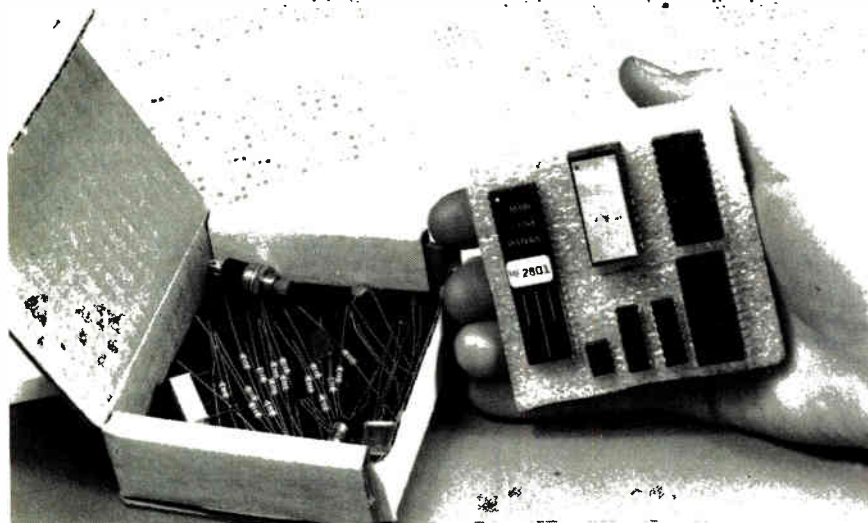
Original-equipment manufacturer discounts are available. In addition, self-source software licensing agreements are available for those companies that prefer to program their own control ROM.

Mark Five Systems Inc., 836 Fourth St., Box 1819, Ouray, Colo. 81427 [371]

Samples available of peripheral controller chip

Another of the Z8000 family of peripheral-support circuits, the Z8090 universal peripheral controller (Z-UPC) is now available in sample quantities. The intelligent device, designed for distributed processing and multitasking applications, is based on the architecture and instruction set of Zilog's Z8 single-chip microcomputer. It assumes such tasks usually performed by the host processor as arithmetic, translation and formatting of data, and control of input/output devices.

The Z-UPC features 2-K bytes of internal program read-only memory, a 256-byte register file (including 234 registers for general-purpose use), three programmable 8-bit I/O



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For more information contact RCA Customer Service, New Holland Avenue, Lancaster, PA 17604.

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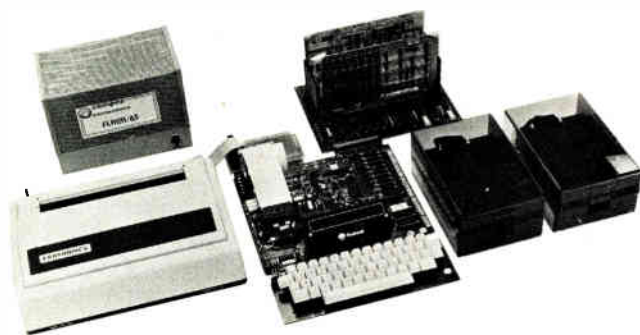
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224 SE 16th St. P.O. Box 687 AMES, IA 50010 (515) 232-8187

130 Circle 156 on reader service card

New products

ports, two programmable counter-timers, and six internal levels of prioritized interrupts. The Z-UPC controls the master processor's access to the register file and thus maintains software independence from the master. The 40-pin controller supports Zilog's daisy-chain interrupt structure.

To cover most peripheral control needs, the Z-UPC comes in four other versions: two 64-pin versions with external interfaces for up to 4-K bytes of either ROM or random-access memory and two 40-pin propack versions, each with a socket for up to 2-K bytes of either ROM or RAM. The devices are priced at \$117.36 each in sample quantities of 10 to 99.

Zilog, Exxon Enterprises Inc., 10340 Bubb Rd., Cupertino, Calif. 95014 [373]

Multuser development system supports 16-, 32-bit designs

A multiuser microprocessor development system based on the EXORmacs system supports both 16-bit and future 32-bit microprocessor designs by using the 16-bit MC68000 microprocessor. It can provide development capability for up to eight simultaneous users. The basic system hardware consists of an EXORmacs 15-slot chassis, an MC68000 memory management module, a debugging module, two 128-K-byte dynamic random-access memories, and a universal disk controller. The controller supports up to two 96-megabyte hard-disk subsystems and up to 2 megabytes of floppy-disk mass storage. It uses an MC68120 intelligent peripheral controller to handle data requests over an SMD (storage module drive) interface.

The software includes the VER-SADOS multitasking operating system, a cathode-ray-tube editor, structured assembler, linkage editor, Pascal compiler, and symbolic debugger. Peripherals include a 32-megabyte hard disk and an EXORterm 155 display console. Additional memory, display consoles, and multichannel RS-232 communi-

Electronics/December 18, 1980

cations modules may be added to accommodate up to eight users.

The EXORMacs multiuser development system sells for \$35,995.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-5714 [374]

Multichannel analog I/O boards cost under \$750

Two 10½-in.² multichannel analog input/output boards for the Intel iSBC 80/10B or iSBC 80/24 single-board computers and for the new iSBX 88/40 measurement and control computer sell for \$610 and \$750 apiece. The manufacturer claims that system designers can use a single one of these in many applications that usually require up to three or four boards.

The iSBX 311 analog-input board provides 8 differential or 16 single-ended inputs. Signal inputs can range from 20 mV full scale to 5 V full scale through the use of gain-selection resistors. Inputs can be either 0 or 5 V unipolar or -5 to +5 V bipolar, with jumper selection. The input board contains a 50-μs analog-to-digital converter with a simple programming interface allowing up to 17,000 12-bit samples/s to be stored in memory.

Users of the iSBX 328 analog-output module can independently jumper any output channel for 0 to 5-V unipolar output, -5 to +5-V bipolar output, or 4-to-20-mA current-loop output. Its digital-to-analog converter is multiplexed to eight separate sample-and-hold amplifiers to update at 1-kHz rates for eight channels and 5-kHz rates for one channel. A-d and d-a conversion resolution on both units is 12 bits and accuracy can be adjusted to within 11 bits at temperatures from 0° to 60°C.

In quantities of 1 to 10, the iSBC 311 sells for \$611, and the iSBX 328 for \$750. They will be in stock by the first quarter of 1981.

Intel Corp., 5200 N. E. Elam Young Parkway, Hillsboro, Ore. 97123. Phone (503) 640-7147 [375]

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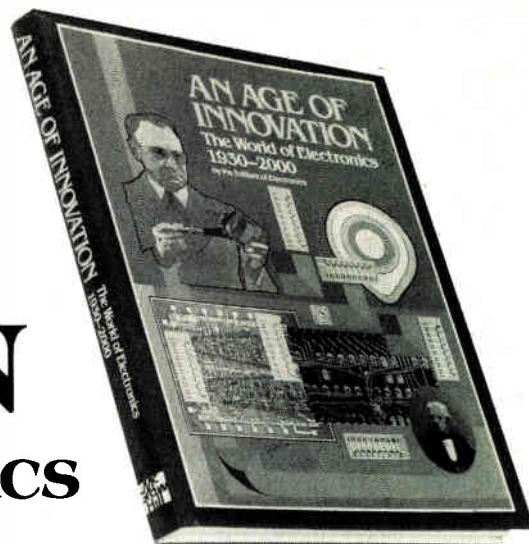
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Products Newsletter

Pascal processor joins Z80 on S-100 bus

The Pascal-100, a new two-board central processing unit, combines a Z80-type microprocessor and Western Digital's Pascal Microengine to yield 5 to 10 times faster execution times than a Pascal-programmed Z80 alone. The CPU is compatible with the S-100 computer bus and, according to its developers, Digicomp Research Inc., Ithaca, N. Y., **may be the first 16-bit Microengine to be combined with another microprocessor—in this case an 8-bit unit.** A key advantage of the dual-processor system is compatibility with existing applications software written for 8-bit Z80- or 8080-based systems or those using the CP/M operating system, as well as with new software like UCSD Pascal, which accesses the 16-bit processor's larger address space. The Pascal-100 costs \$1,485, with volume discounts running up to 33%.

Board lets Apple II run with a 6809

The coprocessor board that **supercharges the Apple II microcomputer by allowing a 6809 to run simultaneously** with it [*Electronics*, Sept. 25, p. 42] is now available from Stellation Two. At no extra charge, the Santa Barbara, Calif., company is also supplying the software routines to adapt the Flex-9 operating system, purchased separately from Technical System Consultants, Lafayette, Ind., for use with the board.

Procom II Industrial controller doubles speed

The microprocessor-based Procom II/80 coming soon from Computer Products Inc., Fort Lauderdale, Fla., **combines industrial control and data acquisition** using routines stored in erasable programmable read-only memories and written in Basic. The Procom II/80, an improved version of the Procom II industrial controller introduced in 1978, operates twice as fast as its predecessor and allows users to alter software while the system is on line controlling a process.

Nitron to make Master Logic gate arrays

Through a nonexclusive licensing agreement with Master Logic Corp. of Sunnyvale, Calif., Nitron Inc. will supply **a line of semicustom gate-array devices made with the Cupertino, Calif., firm's metal-gate complementary-MOS process.** Ranging in complexity from 100 equivalent two-input gates to 200 equivalent two-input gates with 32 flip-flops, the Nitron devices are a direct second source for the Master Logic ML100 through ML350 family of devices, as well as the MCA, MCB, MCC, and MCD gate arrays from Inter-Design Inc., Sunnyvale, another licensee.

Price changes

- **Grayhill Inc., La Grange, Ill.,** has cut prices about 10% on some 96 products in its line of switches housed in dual in-line packages, including its popular single-pull, single-throw switches.
- **Eventide Clockworks Inc., New York,** has reduced the price of its WMAP-1 memory board, which adds 128-K bytes of main memory to the Hewlett-Packard 9845 desktop computer, from \$2,900 to \$2,250.
- **National Semiconductor Corp., Santa Clara, Calif.,** has lowered prices 20% to 34% on the LH0032CG and LH0032G/883 field-effect-transistor operational amplifiers with 500-v/ μ s slew rates and on the LH0024CH 400-v/ μ s op amp.
- **General Electric Co., Norwalk, Conn.,** announced decreases of up to 40% on prices for 1,000-unit sales of its top-of-the-line optocouplers with silicon-controlled-rectifier outputs—the H11C1, -2, -4, and -5.

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Career outlook

Demand for executives grows

■ The demand for experienced executives is on the rise in high-technology industries. If companies in the area have found recruiting skilled engineers and technicians a grueling task, then the search for high-level management qualifies as a truly formidable one. According to an index developed by Korn/Ferry International, a New York- and Los Angeles-based executive search firm, the electronics industries now account for 16% of the total national demand for top-level management in the third quarter—up from 10% in the same quarter in 1979.

Although the need for these executives is growing rapidly, the pool of talented people that can be drawn upon is very small, according to Mark L. Tomchin, vice president for Korn/Ferry's New York-based electronics group. "We keep files on about 1,000 individuals in electronics and electronics-related industries, but only about 500 of those are really interesting," he comments.

Other areas of increased demand include computer-aided design and manufacturing, word processing, and overseas assignments.

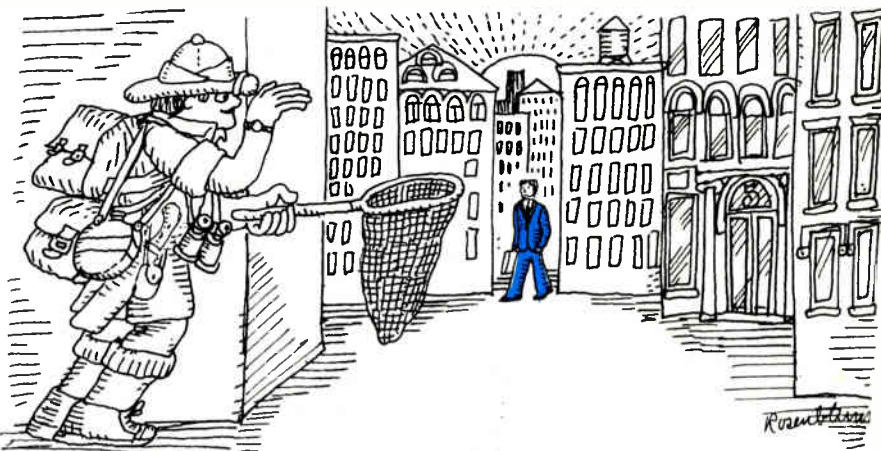
"There are significant numbers of available positions in European-based divisions of U. S. companies," notes the 39-year-old Tomchin. "But U.S. nationals don't want to go overseas. Once many of these highly technical people are away from the U. S. technology base for any length of time, it's like being out on a limb that can be sawed off." He also notes

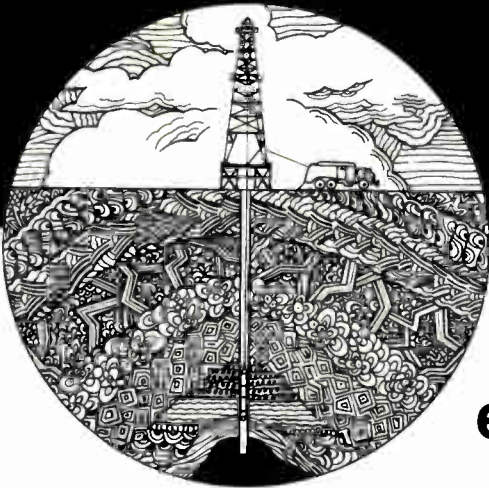
that despite some recruitment efforts by the Japanese in this country, "Americans are loathe to go to Japanese companies."

Korn/Ferry will do executive searches for company positions paying \$40,000 or more, says Tomchin. For that search, whether the firm is successful or not, a fee of one third the annual compensation for the position is charged. "We have a 92% success rate," he says, "even when we include those searches that are stopped by the company because someone is eventually promoted from within." Tomchin, who joined Korn/Ferry in 1974, has been largely responsible for setting up the electronics group, which billed about \$1.2 million last year.

At any one time, the electronics group will have about 10 clients in its portfolio. Korn/Ferry tries to avoid conflicts of interest and will work for only a few companies in any one area. For example, Tomchin notes that his people are working with three semiconductor-oriented companies; three companies in data transmission; one fiber-optics firm; and three computer companies, "two of them—one, a mainframe maker and the other, a mini maker—in excess of \$2 billion."

Tomchin observes that companies with a deep layer of middle management that often cannot be promoted to the next level are his best sources for potential recruits. "When you can offer a middle manager a vice presidency of engineering, it's often a good incentive for him to leave," he comments. **-Pamela Hamilton**





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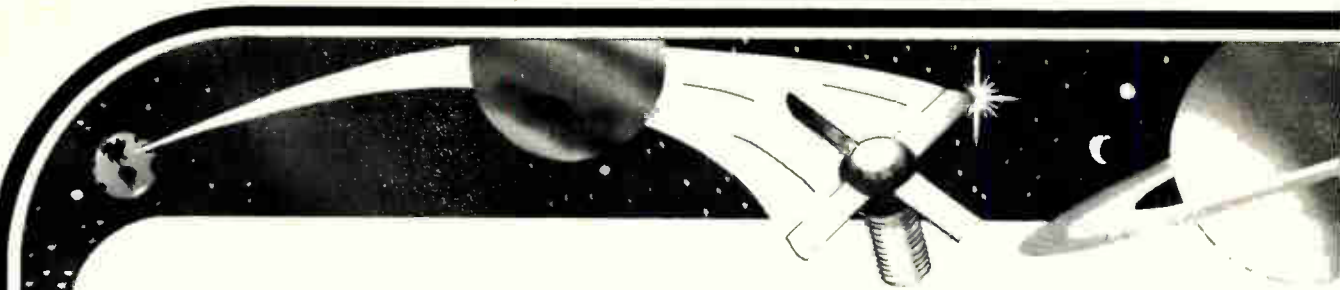
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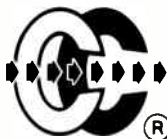
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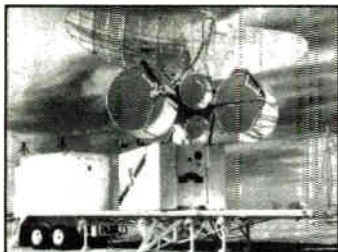
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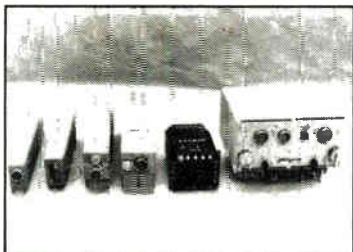
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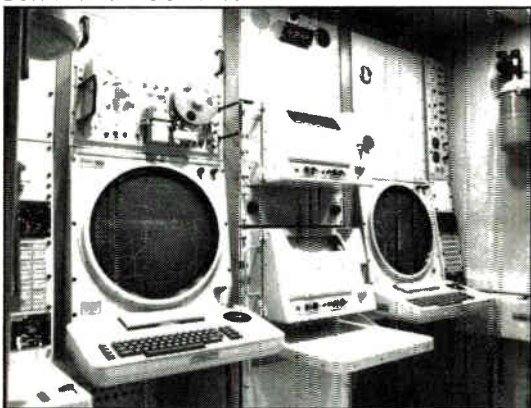
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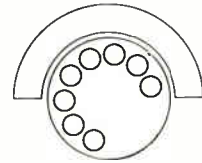
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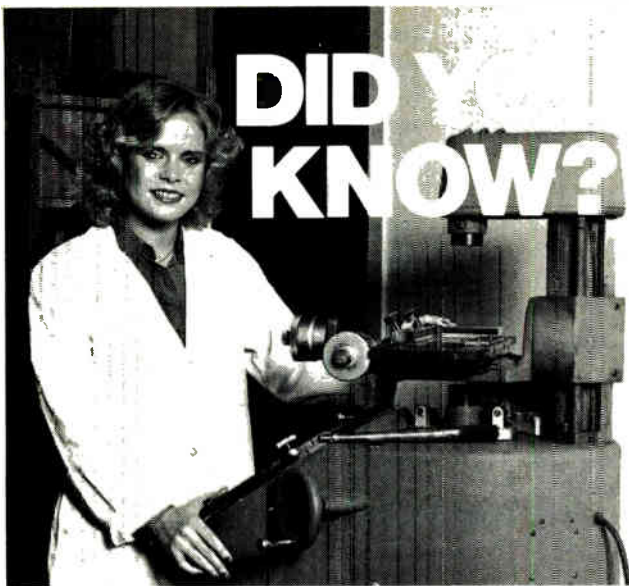
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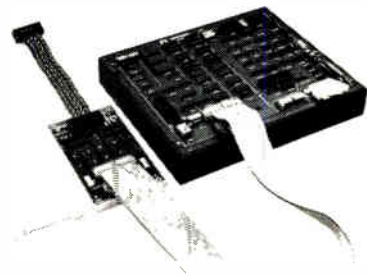
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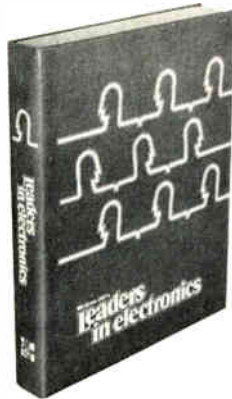
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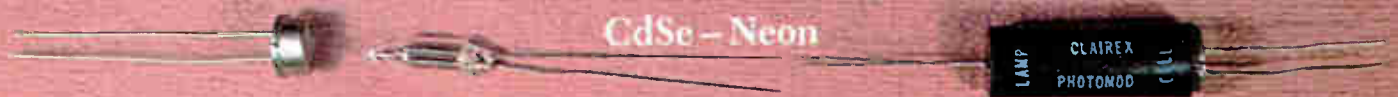
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