OCTOBER 23, 1980

ANNUAL TECHNOLOGY UPDATE ISSUE

Networks are tying together expanded processor families, the offshoots of ever-higher levels of integration/112

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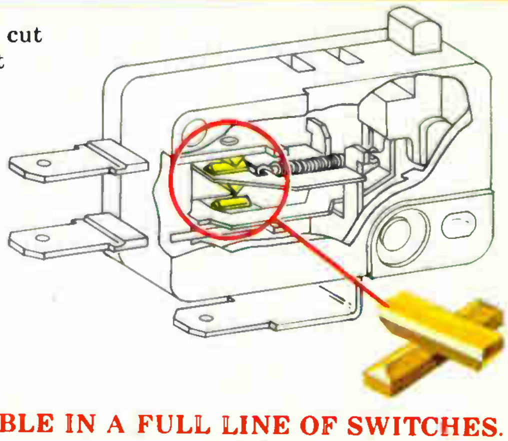

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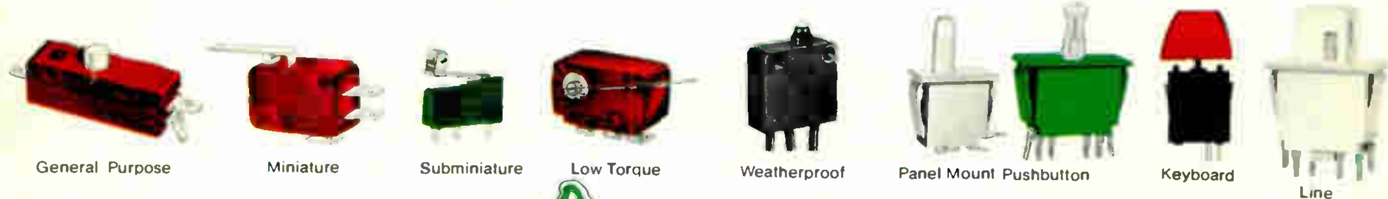

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Circle 1 on reader service card

Electronics
The International Magazine of Electronic Technology
Vol. 53, No. 23 • October 23, 1980

Highlights

Cover: The 1980 Achievement Award, 104

Electronics gives its annual Award for Achievement this year to three men who had much to do with making the fabrication of large-scale integrated circuits a reality. Perkin-Elmer's Abe Offner, Jere D. Buckley, and David A. Markle teamed up to produce the Micralign 1:1 optical projection printer. Their machine offered a way around inherently risky contact printing.

Cover is by Art Director Fred Sklenar.

Technology Update, 112

Barely out of the cradle, the 1980s has already notched several notable achievements, making it clear that the electronic technologies will not soon slacken in their rush to bring about a new Industrial Revolution.

Semiconductors, 114. Though in electronics, new is usually better, in the solid-state arena the standard technologies remain the technologies of choice. But working their way out of the labs are two extremely fast challengers, gallium arsenide and Josephson junctions.

Memories, 132. Designers have proved themselves up to surmounting the hurdles of achieving denser—and faster—memories.

Microsystems & software, 150. To be successful in the marketplace, microprocessor makers are following the example of mainframe companies.

Components, 170. Data converters, displays, even discrete devices—all are enjoying the benefits of integration.

Test & measurement, 184. Automation is a key word for what is taking place in instrumentation, with such instruments as signal generators and oscilloscopes the main beneficiaries.

Computers & peripherals, 192. Local networks blossom to ease distributed processing and office automation.

Communications, 206. A relatively recent discovery on the communications stage, fiber optics has truly emerged into professional status.

Consumer, 214. Technology's part in the leisure explosion is marked by the expansion of the television set as the center for developments in home entertainment and in information distribution.

Packaging & production, 222. The laser is a new, multitalented star in the production lineup.

The year in electronics: a chronology, 230.

And in the next issue

Two special reports: chip sensors and how electronics engineers view their career . . . a 20-bit digital-to-analog coverter . . . realizing a low-cost digital multimeter . . . a 64-K static random-access memory from Japan.

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Circle 5 on reader service card

Publisher's letter

One of the first signs of autumn around the *Electronics* editorial corridors is the quiet that falls over them as the technical editors retire to their offices, review their past year's work, and think about the year to come. Yes, they're busy on Technology Update, and the fruits of their labors will be found beginning on page 112.

Technical managing editors Al Rosenblatt and Ray Capece see to it that their reports pull together the trends that predominated in 1980 and that will be important in the year to come. Former technical editors themselves, they say it truly takes a year to produce a satisfactory Update.

To begin with, our editors travel extensively to keep up with the companies they cover—indeed, many of our readers know that, for they are accustomed to seeing *Electronics* staff members come through the door. In between trips, of course, the telephone comes into play, with calls being made to all corners of the world. Needless to say, there's a steady stream of visitors to our New York offices, and our field editors also play a role in industry watching.

So it is a year-long effort that produces our once-a-year Technology Update—and, incidentally, it has as much value for us as for you. In sitting down to refine the year's work and then to hammer out a view of the year to come, we come up with a truly precious alloy: a deeper, more comprehensive understanding of the forces at work in the industries that we cover.

And what is the story that we have wrought for you? Well, it takes better than 60 pages to set it forth, as we focus on the developments that we think most significant—and as we spotlight some of the people that have made these developments possible, both in our annual Award for Achievement and in the profiles that accompany the Update sections.

When Ray and Al talk of this Update, some of the key phrases in the conversation turn out to be: "networking," "smarter terminals," "more automation in instruments," "C-MOS strength in memories and microprocessors," "complex peripherals for the 16-bit processors," and "fiber optics." All in all, it should be another golden year.

One of the foundations of the impressive record of progress in the electronics industries is the production equipment that has made possible large-scale integrated circuits. Where, in fact, would the LSI industry be without the Micralign projection mask aligner?

If you think about the answer, you will realize why the 1980 *Electronics* Award for Achievement is going to the team responsible for Micralign: Abe Offner, David A. Markle, and Jere D. Buckley of Perkin Elmer Corp.'s Microlithography division.

"It's the backbone of the IC industry," says packaging and production editor Jerry Lyman, coauthor of the profile of the winners. "There might not have been any true LSI production without these machines, because in replacing contact aligners, they made it possible to achieve cost-effective yields."

Together with coauthor Pamela Hamilton, the New York bureau manager, Jerry spent a day talking with the team at their Wilton, Conn., laboratory. Their story, covering the history of Micralign, how it works, and the men who put it together and how they worked together, begins on page 104.

Since its optics are the heart of the machine, it's interesting to trace its provenance, which turns out to be telescopes for aerospace and satellite applications, notes Pam. "It's another case of adaptation of military expertise to solve the problems of the electronics industries," she notes.

This is the third shared Achievement Award in its seven-year history; however, it is the first time all recipients were from the same development team at the same firm.

Circle 7 on reader service card

People

Pyle will depend on a French connection

On the face of it, the formation of Alta Technology in Stamford, Conn., looks rather risky. It is a new company, 90% owned by a stranger to American shores, Compagnie Générale d'Automatisme (CGA), a French subsidiary of Compagnie Générale d'Electricité. And Alta's initial goals are to take on the likes of IBM, NCR, and Burroughs in the bank terminal market and to try to crack the near-exclusive fields of automated fare systems and automated toll-collection systems.

But 41-year-old Alta president James H. Pyle sees many advanages in the setup. The biggest plus is the availability of products from CGA that are already designed and tested in installations around the world. For instance, Alta will be able to take CGA's branch-bank check-processing terminals, alter them for U. S. applications, and go right to market. Pyle's own contacts with banks, gained as former president of Periphonics, an Exxon Enterprises Inc. affiliate in Bohemia, N. Y., are also in Alta's favor.

A third advantage is timing. "Within the next year and a half, banks will have entered distributed data processing and the CGA terminal fits this trend," Pyle says. American banks are starting what they call "check trunkation," reporting accounts without returning the canceled checks to the customer, a fact of life in Europe for years. As a result, Pyle feels that Alta is in the right place with the right equipment.

He acknowledges, however, that breaking into the transportation business in the U. S. will not be as easy. For one thing, not many mass transit systems are being built. But Pyle believes that he can impress authorities by showing them reliable, working fare systems installed by CGA in Europe and South America. Similarly, he is confident that Alta can open a wedge with turnpike authorities eager to upgrade aging toll-collection systems by showing them the ones CGA has installed.

Nouveau venu. Alta's Pyle expects his new company to win with CGA products.

Pyle is quick to point out that the CGA equipment sold by Alta will have 70% to 80% U. S. content. The microprocessors, for example, will be supplied by Intel. And he stresses that the cross-licensing agreement with CGA is a two-way street. The French company expects to acquire knowledge in the use of U. S. technology from Alta.

The new company actually came into being during Pyle's previous tenure at Periphonics. Near the end of 1977, feeling that the firm was underfinanced and finding that Exxon's purse strings were pulled tight, Pyle began negotiating with CGA. Then Exxon abruptly decided to gas up Periphonics and picked up the 20% of shares owned by Periphonics' executives. Pyle, however, remained intrigued with the potential for CGA's products in the U. S. and sold the French on forming Alta. He expects to start shipping bank terminals in the first quarter of 1981 and to reach the break-even point by the end of 1982. □

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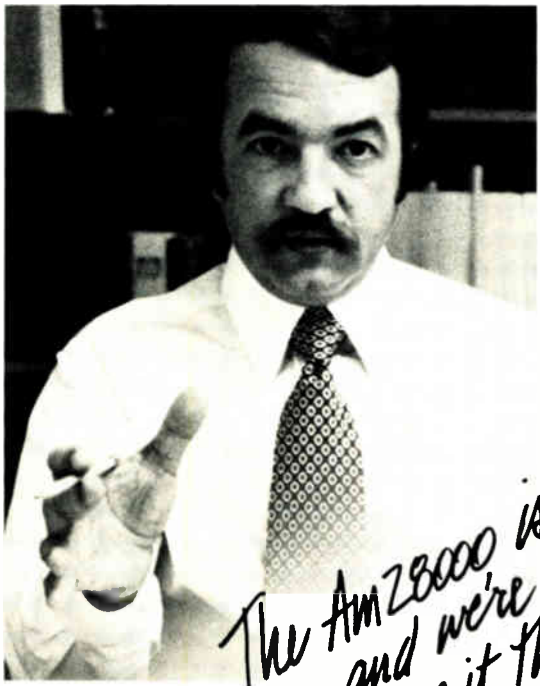

Sven Simonson, Vice President
and Technical Director,
Advanced Micro Devices

The AmZ8000 is better and we're committed to keeping it that way.

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A vote for the engineers

The engineer in the U. S. has traditionally been pictured in film and fable as the good, gray, uninspired, and uninspiring technician laboring along steadily at the workbench. The scientist, on the other hand, has been a romantic figure: given to fits of inspiration and attacks of enlightenment, he or she has been the one to discover, invent, and perfect marvels ranging from radium to the telephone. But the worm is turning.

Focusing their discontent on the role of the National Science Foundation, engineering groups are lobbying for passage of a proposal in Congress for a National Technology Foundation. The bill, H. R. 6910, started undergoing hearings last month. Its chief sponsor is Rep. George E. Brown Jr. (D., Calif.), chairman of the House subcommittee on science, research, and technology, the body that holds the purse strings for the NSF.

Basically, what the Brown measure would do is take the technological functions from some Federal agencies, like the NSF and the Commerce Department, and reorganize them as a separate agency. The Institute of Electrical and Electronics Engineers and the American Association of Engineering Societies, the two largest engineers' groups, have adopted resolutions offering three options: creation of an NTF, major changes in the NSF to enlarge the role of engineering and engineers in that body with the changes reflected by a name change that includes engineering, or establishment of a new engineering foundation.

When the NSF convened a meeting to look at itself and come up with some sort of recommendations for changes, the engineer's cause was advanced most forcefully by Karl Willenbrock, who is the dean of the School of Engineering and Applied Science at the Southern Methodist University in Dallas.

The matter of establishing an NTF raises a fundamental issue, he said. Engineers feel that they have been treated as second-class citizens by the NSF and thus have little confidence in it, he went on. "What they're saying is that the NSF has not made a contribution to engineering comparable to that which it has made in other areas," he concluded.

And Bruno O. Weinschel, at the time the IEEE's vice president for professional activities and now the institute's secretary, pointed out earlier this year that a greater issue is at stake: basic research, he noted, contributes little to the U. S. balance of payments. The key to increasing productivity is technology derived from that research. Weinschel notes that "bite-sized interim solutions to the productivity problem . . . have been suggested." Among those bills and resolutions introduced in Congress are measures dealing with:

- Investment tax credits for research and development.
- Accelerated depreciation.
- A mandatory balanced Federal budget.
- Various schemes to relax capital-gains taxes.
- Establishment of a technology division in the Department of Commerce.
- Patent law reforms.

Willenbrock, Weinschel, the IEEE, and others pushing for an engineering or technology foundation are on the right track. The recognition of engineers and their contributions to technology as equal to that of scientists is an idea whose time came quite a while ago. A National Technology Foundation to fund and nurture engineering is necessary as well as desirable—now.

Readers' comments

Taking issue

To the Editor: The article "Transparent memory ends conflicts over CRT control" by Lorne Trottier and Branko Matic [July 5, 1979, p. 136] offers an interesting approach to dual-port memory design for cathode-ray-tube displays. However, it contains several statements that could mislead the casual reader.

The article states that "the CPU is never hampered. And the method is entirely general: it does not rely on peculiar timing characteristics or a particular CPU." Buried in the next to last paragraph is the admission that the central processing unit must be able to provide wait states. In fact, under worst-case asynchronism, a wait state could occur for every CPU access to the CRT memory.

I find it hard to believe that this does not constitute "hampering" the CPU throughput. Furthermore, not all processors provide ready/wait circuitry (for example, the 6800), nor are the timings of those processors that do provide ready/wait at all similar. Some CPUs are in fact extremely sensitive to ready/wait timing. Thus the claim of being "entirely general" is exaggerated.

The next to last paragraph also states, "With 80 characters per line, this waiting time is equivalent to an access time of only 500 ns." Assuming 40 μs of active video per 63-μs horizontal line gives a CRT cycle time of 500 ns. Thus the random-access memory's cycle time will be 250 ns. If the RAM chips access in 250 ns, the RAM must use at least one full memory cycle (one-half the cell time) to serve the CPU. But under worst-case asynchronism, the CPU memory cycle start could always "just miss" ($\Delta t \rightarrow 0$) the first RAM cycle and the CPU will be required to wait through two further RAM cycles (Fig. 1). This is a worst-case access time of 750 ns.

If half of the CPU cycles are hits and half just-misses, the average access time will be 625 ns. Only the best-case time is 500 ns.

Note that this situation is made worse by decreasing the number of characters per line. Obviously, the technique described makes CPU throughput highly dependent on screen format. Also, such an irregular pattern of wait states makes system throughput hard to predict.

A better approach to the classic problem of dual-port memory contention is to make these assumptions: attached devices A and B operate asynchronously and device A—the faster of the two—has a memory-access time requirement of T_{AC}. Squeezing two port A cycles into device A's read cycle (T_{AC}) guarantees a complete asynchronous memory cycle. Only one leading edge of the sampling clock should be provided for device A's write cycle because the input latches allow memory-write cycles to be completed independently of the attached device.

This approach is truly independent of CPU timing and requires no wait states. Minimal additional circuitry and a moderate increase in RAM speed is all that is required. PBS is currently using a 1-K-byte dual-port module based on this technique in several CRT and multiprocessor applications.

Robert W. Schmidt
Public Broadcasting Service
Washington, D. C.

■ **Lorne Trottier replies:** *The statement that "the method is entirely general: it does not rely on peculiar timing characteristics of a particular CPU" was included to distinguish Matrox's method from a transparent memory technique used with the Motorola and Synertek CRT controller chips. The latter technique relies on the two-phase clock of the 6800 and 6502 CPUs and also requires that the CPU and CRT controller chip run from the same clock (difficult for board-level designs).*

It is true that the Matrox technique requires a ready line on the host CPU. I believe that most minicomputers and microcomputers should and in fact do incorporate such a signal. It is interesting to note that Motorola has added such a line to its 6800-based EXORciser bus products (at the cost of several additional TTL packages) and to its new 6800 microprocessor.

We have encountered no difficulty adapting to the ready-line timings of various CPUs. Matrox manufactures

video alphanumeric and graphic boards using this technique for the DEC PDP-11 and LSI-11 buses, Intel Multibus, S-100 bus, STD bus, and Motorola EXORciser bus.

Also, Mr. Schmidt makes an error of his own. In the example he analyzes, the best-case access time of our design is 250 ns. This leads to an average access time of 500 ns, as we stated.

Mr. Schmidt suggests a method that he claims is superior but is in fact nearly the same as ours. Both methods switch the memory at a rapid rate between the CPU buses and internal CRT scanning circuitry to give quick access to the RAM. The only real difference lies in the speed at which the switching is done. The Matrox design switches the memory at the character clock rate; Mr. Schmidt uses a second clock running at a much faster rate. This approach increases costs dramatically by requiring a second clock and also by using much faster and more expensive RAMs (2147s versus 2114s).

Finally, Mr. Schmidt states that "the Matrox technique makes CPU throughput highly dependent on screen format." That is true; however, at the fixed format of 24 lines by 80 characters for which this technique is used, this dependence poses no problem. With our new generation of software-programmable format boards, a new technique is used whereby the CPU's access time actually decreases with lower-resolution formats. The penalty of course is added circuit complexity.

Needed: a better index

To the Editor: It is indeed clear from "Japanese make quality-control pitch" [April 10, p. 81] that "Japan's quality control is better and productivity is higher." But Hewlett-Packard's data on comparative failure rates of integrated circuits is not really the "frightening set of statistics" that Richard W. Anderson claims it is. The qualification index in the last column of the HP data clearly shows that the quality from all IC vendors was not the same. The comparison of failure rates should have been made on supplies from vendors of equal rating.

Prabhakaran M. Nair
Trichur, India

MEASUREMENT COMPUTATION news

product advances from Hewlett-Packard

OCTOBER 1980

Now you can work with up to four programs simultaneously on the new HP 2626A terminal

The new HP 2626A display station makes it possible for programmers to work with several independent programs simultaneously. The terminal features display memory that can be divided into as many as four separate work areas and a display screen that can be divided into four windows. These windows make it easy to display data from different computers or from different sessions on the same computer.

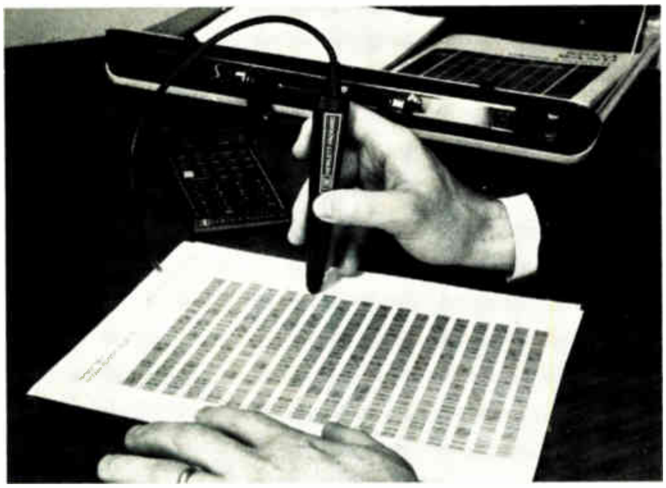
The display screen may be divided into vertical segments and as many as four horizontal segments, up to a maximum number of four windows. A programmer may scroll the data both horizontally and vertically within each window, or change the size of the window.

Dual datacommunication ports provide connections to other computers or RS-232-C peripherals. For example, while an operator is entering data into one computer, the HP 2626A could simultaneously be receiving data from a second computer and printing that data on the integral forms copy printer.

A programmer could be logged-on to the same computer twice, through the dual datacommunication ports—one session for program development, the other session for monitoring batch jobs or printing a program listing.

(continued on third page)

New peripheral for the HP-41C provides fast, inexpensive and convenient input capability



The HP Optical Wand offers fast, inexpensive and convenient input capability—an exciting and productive addition to your HP-41C personal calculator.

Last year HP introduced the HP-41C—the most powerful personal calculator Hewlett-Packard had ever designed. Now we introduce the Optical Wand—the exceptionally convenient input peripheral that permits you to load programs and data into the HP-41C quickly and easily.

When plugged into one of the HP-41C ports, the Optical Wand reads bar codes from a printed page, translates the codes into HP-41C program and data information, then automatically loads them into the calculator. The Optical Wand reduces programming time since program instructions, many of which require multiple keystrokes, can be entered, each with simply one scan of the wand.

By reading bar codes, the Optical Wand opens up a world of benefits. Bar code listings are convenient and inexpensive since most are printed on standard paper—a medium that can easily be stored, reproduced, and distributed.

The vast software library for the HP-41C is also at your fingertips. All Users Library programs and Solutions Books are printed in bar code, making them available to use with the optical wand.

Check **A** *on the HP Reply Card for details.*

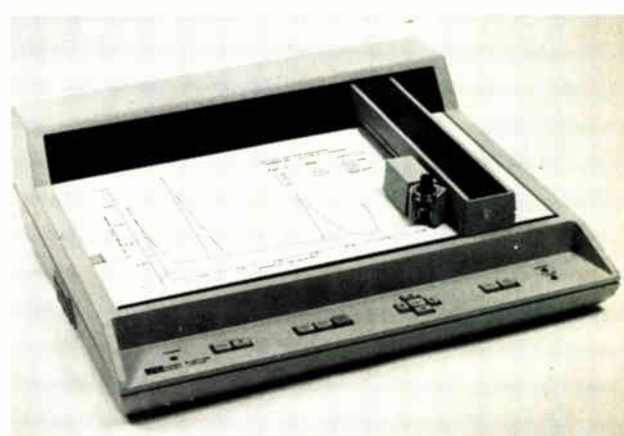
New capabilities module available to extend versatility of your DESIGNED FOR HP-IB SYSTEMS HP 7225A Plotter

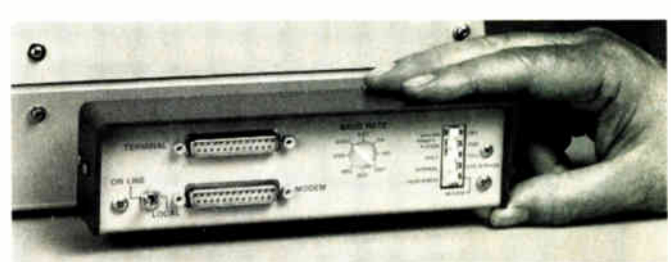
The very popular Hewlett-Packard 7225A A4-size Plotter can now be used in applications involving remote data communications. In addition, internal arc and circle generation previously available only on HP's larger 4-pen plotters is now available on the 7225A.

These new capabilities can now be a part of your 7225A plotter simply by adding HP's new 17604A Personality Module. This module provides the RS-232-C/CCITT V.24 interface for both hardwired and remote data communications and the HP-GL graphics language for easy English language programming.

Designed for OEM and end user systems, the 7225A/17604A combination provides a low-cost, high-quality plotting capability for applications requiring remote operations over a telephone line.

Check **B** *on the HP Reply Card for more information.*





ATTENTION TAPE RECORDER USERS!

If you are recording several reels per week of ½-inch or 1-inch instrumentation tape, you may be able to save thousands of dollars per year. Let us show you how.
Check **C** *on the HP Reply Card for details.*

HP introduces top-of-the-line DESIGNED FOR HP-IB SYSTEMS HP 1000 Performance/45 technical computer system

Expanded memory, new language capabilities and program optimization packages characterize the new HP 1000 Performance/45 System. Designed for applications in computation and program development, this multi-language computer system combines the HP 1000's highest-performance hardware with its highest-performance software.

New Software

The Performance/45 System is based on the HP 1000 Model 45 System which incorporates an F-Series computer, 512 kbytes of fault-control main memory (expandable to 1.8 mbytes), 19.6 mbytes of disc storage (expandable to 960 mbytes), and a graphics terminal. Included in Performance/45 are new PASCAL/1000 and FORTRAN 4X compilers, as well as new EDIT/1000 screen editing software. Performance/45 also includes the new ACCEL/1000 program profiler and microprogram development package.

PASCAL/1000 is a superset of industry-standard PASCAL, a high-level, modern, block-structured language known for its rich set of data and control structures, ease of use and maintainability. Because of these features, PASCAL/1000 helps speed up program design, debugging, documentation, modification and maintenance.

FORTRAN 4X is a superset of ANSI FORTRAN 66, with compilation speeds as high as 3000 lines per minute. FORTRAN 4X is upward-compatible with HP FORTRAN IV and features direct access I/O, double word integer data type and IF-THEN-ELSE construction. Direct access statements conform to ANSI FORTRAN 77 specifications, and allow IBM READ and WRITE statements.

EDIT/1000 is an editing package that interacts with users in line mode or screen mode. In line mode, it provides for basic text maintenance, character string search and replace capabilities, and interactive instructions. In screen mode, EDIT/1000 enables the user to take advantage of the local editing capabilities of smart HP terminals.

ACCEL/1000 is a software package that profiles program activity, showing the user precisely where execution bottlenecks exist. Often, these bottlenecks may be eliminated by rewriting that section of code in the original source language or in assembly language. For optimum performance, ACCEL/1000 also includes a microprogram development package.

HP 1000 Performance/45 basic system includes a set of microcoded CPU instructions for fast and efficient operation on matrices of data applications.

Check **D** *on the HP Reply Card.*

New terminal screen divides into four displays

(continued from first page)

User-Definable Soft Keys Ease Program Interaction and Forms Design

The HP 2626A has eight screen-labeled softkeys (function keys) which can be programmed by the user. The soft keys can be used to simplify interface to the host computer and to perform repetitive procedures, such as calling or initiating programs, generating standard statements or frequently-used formats.

Using the softkeys, the user can draw horizontal and vertical lines with single, double, or bold-line definitions. Fields, edits and display enhancements also are defined using the function keys. Programmable audio prompting on the HP 2626A can alert operators to various conditions within an application.

Integral Forms-Copy Printer an Option

A built-in, thermal forms-copy printer is an option for the 2626A terminal. The printer can reproduce dot copies of the display on the screen, line drawings, math and special-language symbols, as well as large characters.

The forms-copy printer has both a compressed-print mode that can be used to copy 132-column lines on the 8½-inch-wide paper and an expanded-print mode that produces double-size characters.

The basic HP 2626A display station can operate in block, line, line-modify and character modes. Data-communication capabilities enable operation in hard-wired, full-duplex, half-duplex and multipoint environments which are either synchronous or asynchronous. The HP 2626A is escape-sequence-compatible with the HP 2645A terminal, and supports a number of industry protocols and handshakes. It connects to any TTY-compatible port using ASCII. RS-232-C datacommunication ports are standard. A 20-mA current loop interface is also available.

Check **E** *on the HP Reply Card for more information.*

New graphics tablet simplifies system interaction

Hewlett-Packard's new 9111A Graphics Tablet allows the user to interact with displays on HP's mini, desktop and personal computer systems. This new graphics tool can be utilized in most applications requiring you to draw on a CRT display. Schematics, computer-aided design PC/IC layout, office and industrial layouts, and architecture are just a few of the variety of applications the graphics tablet can help you with. The 9111A acts as the CRT's cursor mover. As the user draws on the tablet, the picture appears on the CRT making design, diagrams and layouts virtually come alive, with room for constant on-the-spot changes.

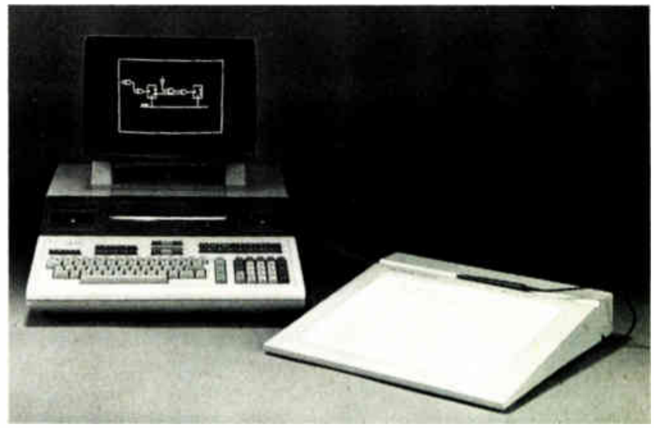
Entering data from a source document is easy with the 9111A. The single-point and continuous drawing modes allow line drawings, logos, charts, etc. to be easily traced and stored. An overlay is supplied to protect and hold down documents.

Menu Selection

As a customized keyboard, the 9111A allows you to select from the "menu" commands or data by pressing the stylus on the appropriate outlined area. Sixteen softkeys provide menu selection without requiring that you do x, y coordinate analysis. And if you need additional softkeys, your software can convert the entire tablet into a menu/keyboard for more entries. You can order and group them to suit your individual needs.

Durable and Convenient Features

Quality, durability and reliability are noticeably integrated into the 9111A. The hard ceramic platen will not easily scratch or pit. A slim, lightweight stylus and inclined working surface provide operator comfort for long periods of use. The stylus accommodates ink and non-ink refill, both of which are available through HP's worldwide supply centers.



Hewlett-Packard's new graphics tablet acts as a CRT's cursor mover in single-point or continuous drawing modes. It can draw on a CRT, trace graphics documents or pick from a menu.

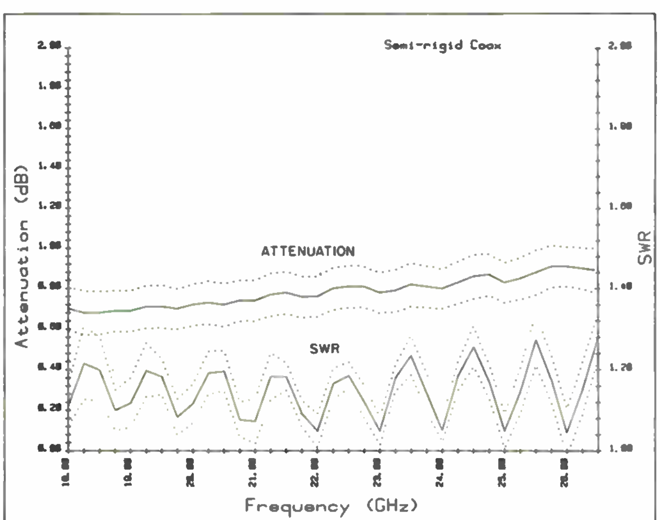
A 60-points-per-second data rate provides smooth cursor movement and can be synchronized with the refresh rate of the CRT. Optimum performance can be attained using the 9111A binary transfer capability.

A programmable beeper gives audio feedback when operations are completed. In addition, four LEDs provide visible feedback of functions being executed. Two built-in self-tests allow isolation of problems if they arise.

The 9111A utility software, Model 88100A, is available for use with the HP System 45 Desktop Computer. The software includes graphics editor, drawing utility and menu utility.

Check **F** *on the HP Reply Card for further information.*

Measure SWR, attenuation and power sensor efficiencies 18-26.5 GHz in coax



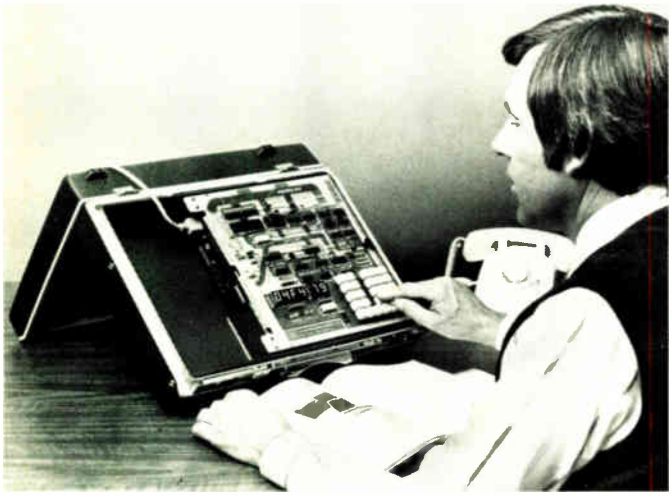
By using a K-band waveguide reflectometer with HP's new K281C APC-3.5 Adapter, and the three-power meter measuring techniques of Application Note 64-2, high-accuracy coaxial measurements can be made from 18-26.5 GHz, under automatic control.

Thanks to this combination, SWR results have an equivalent directivity of about 30 dB. And because power sensors are used for detectors, the mismatch uncertainty is low for attenuation measurements. In addition, other power sensors can be compared to a standard for calibration factor.

For complete information and a free copy of AN #64-2, check **G** *on the HP Reply Card.*

Typical plot of SWR and attenuation. Dotted lines show calculated uncertainty limits.

HP's microprocessor lab teaches digital troubleshooting



The 5036A Microprocessor Lab with optional 5004 Signature Analyzer and 5024A IC Troubleshooters Kit provide actual hands-on microprocessor troubleshooting experience.

Hewlett-Packard's 5036A Microprocessor Lab provides an aspect of microprocessor training not available in other products—microprocessor troubleshooting. What's more, it provides skill in this important area using HP's high-quality instruments and thorough documentation. The 5036A consists of a 20-lesson textbook/lab manual and a briefcase-contained operating microcomputer.

Included in the 450-page textbook are a troubleshooting tree for the lab, block diagrams, schematic, signature tables and solutions for the lab's 12 moveable, practice fault jumpers. In short, all documentation needed to completely troubleshoot the lab.

The lab's textbook, "Practical Microprocessors" culminates in four highly practical troubleshooting lessons:

- **Handheld Troubleshooting Tools**
- **Signature and Logic Analyzers**
- **Troubleshooting μP Systems**
- **Troubleshooting the Microprocessor Lab**

Detailed troubleshooting experiments on the lab using signature analysis.

For details, check **H** *on the HP Reply Card.*

Now over 1900 programs available for DESIGNED FOR HP-IB SYSTEMS IC tester

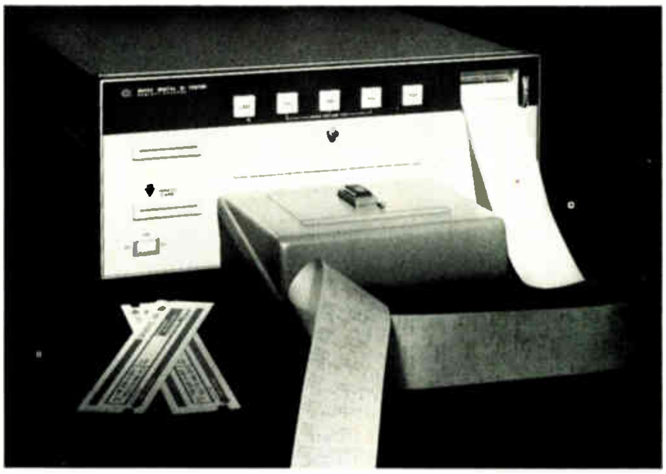
There's probably no easier way to get fast, accurate screening of your incoming ICs than with HP's 5045A Digital IC Tester. Set-up is as easy as inserting a magnetic card. The IC programs you need are almost certain to be in our growing library of over 1900 programs covering today's most used ICs from bipolar to MOS, and from gates to RAMs.

Touch a button and you get immediate pass/fail indication. Need to know more about the failure? Push another button and you get a complete printout of the test with the failure point indicated.

Customize Your Test Programs

Want to refine a test procedure? Need a test for a special IC? The HP 5046A Digital IC Test System lets you write your own custom test programs. It includes the HP 9825S Desktop Computer, a powerful computing instrument that you can also use for many other tasks, such as program storage or general-purpose computing. The 5045A Digital IC Tester also interfaces with a large variety of the major IC handlers.

For further technical data, check **I** *on the HP Reply Card.*



A simple magnetic programming card makes it a lot easier to learn about the quality of your incoming ICs with HP's 5045A Digital IC Tester.

New ease and versatility in dynamic analysis of structures and servos

HP's 5423A Structural Dynamics Analyzer provides state-of-the-art measurement, analysis, display, storage and plotting capabilities in a convenient, keyboard-operated instrument. It can quickly identify structural problem points such as maximum stress, flexure or sound transmission, and perform traditional servo analysis. Measurements include time record, power spectrum, frequency response and coherence—to name a few. Its animated, mode shape display depicts structural deformation for each natural resonant frequency. Its price is surprisingly low for such capability.

Check **J** *on the HP Reply Card for details.*

New ac/dc threshold sensing optocoupler has guaranteed input-threshold specifications

A new voltage/current threshold detection optocoupler with guaranteed input-threshold specifications and logic-compatible output has been designed by HP for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

The HCPL-3700 combines a threshold-sensing input buffer IC, an internal LED, and a high-gain photon detector to provide an optocoupler which features adjustable external threshold levels and logic-compatible output. It is recognized under the component program of Underwriters' Laboratories, Inc. (File No. E55361).

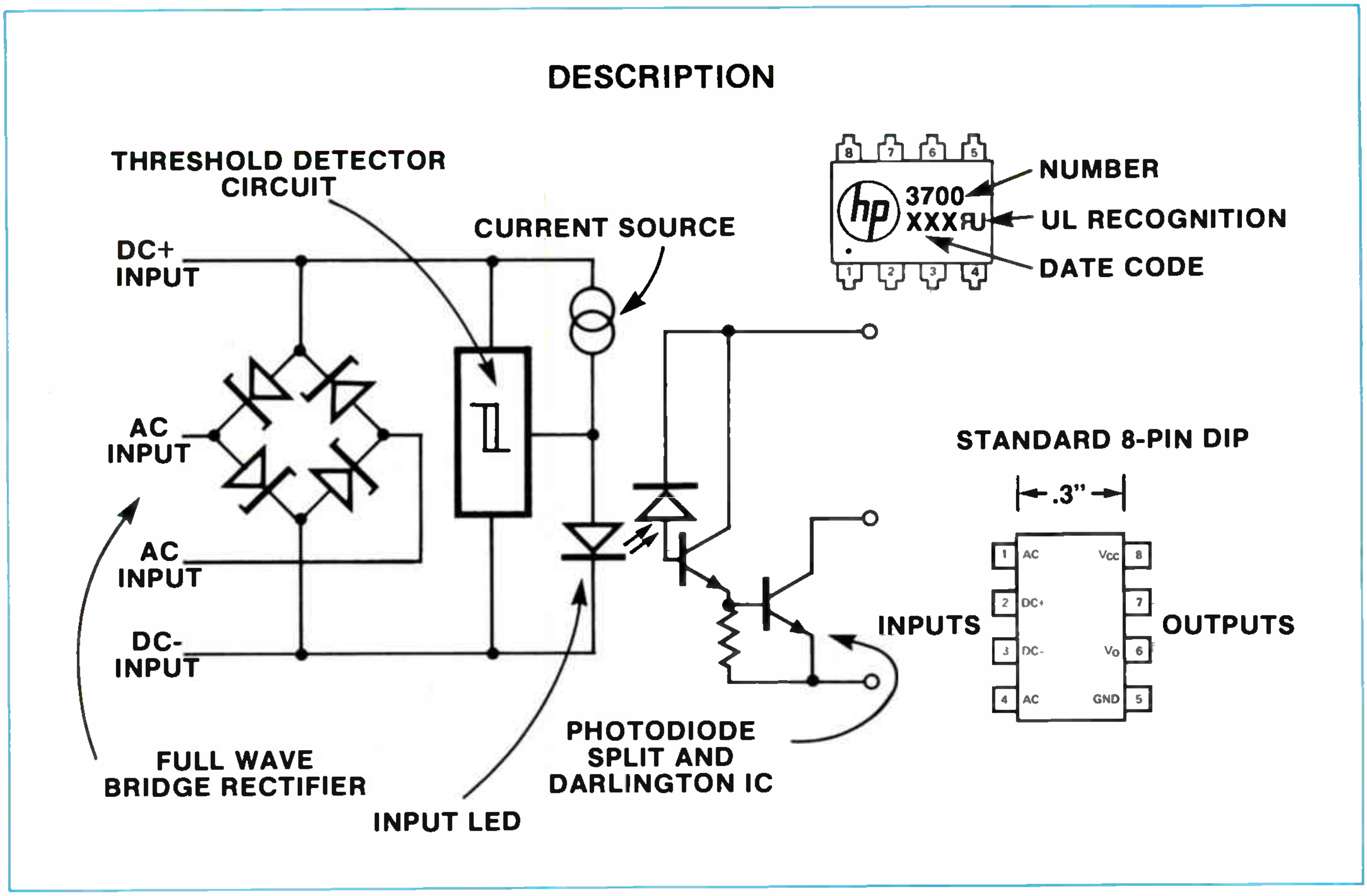
The input buffer IC contains a reference voltage circuit and a comparator that compares the input signal with the reference voltage. When the "threshold" is reached, the comparator switches and turns on current to the LED. The nominal turn-on threshold is 2.5 mA and 3.8 V, but the addition of one or more external attenuation resistors permits the user to set the HCPL-3700 threshold switching point over a wide range of input voltages and currents. Additionally, a hysteresis circuit in the comparator minimizes false LED turn-on for electrically noisy input signals.

The HCPL-3700 accomplishes threshold detection on the input side of the device, essentially eliminating gain variations as a factor in the threshold detection function. This allows for threshold specifications guaranteed over temperature and virtually eliminates problems associated with current transfer ratio degradation.

The high-gain output stage of the HCPL-3700 features a split-darlington, open collector output, providing both TTL-compatible saturation voltages and CMOS-compatible breakdown voltages. Its features make it attractive for microprocessor-interfacing applications such as limit switch sensing, low voltage detecting, 5 to 240 V ac/dc voltage sensing, relay contact and relay coil monitoring, as well as current sensing.

For ease in design applications, a full-wave bridge provides rectification of ac voltage inputs, while internal zener diodes provide clamping action to protect the HCPL-3700 from a wide range of over-voltage and over-current transients. It is packaged in a standard, 8-pin DIP and available at HP distributors.

Check **K** *on the HP Reply Card for more information.*



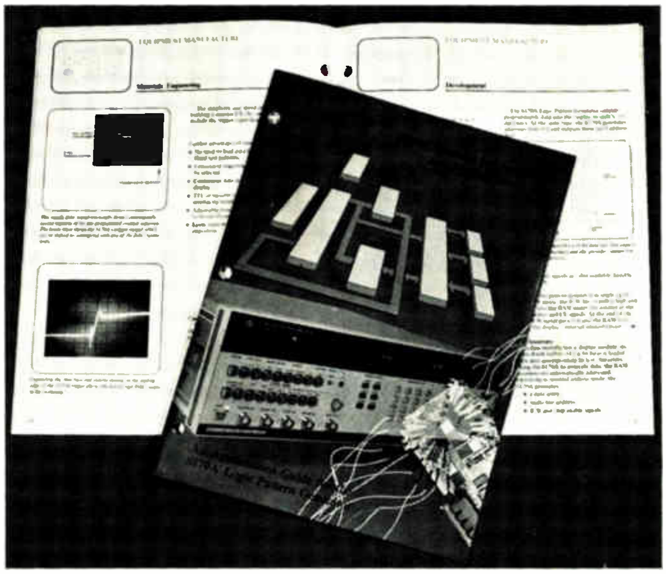
Get the right stimulus for your digital hardware test needs

Besides being essential for testing complex ICs, the environment simulation technique also gives the circuit designer and equipment manufacturer great flexibility. Independent of supporting hardware and software, this technique allows subassemblies of a product to be developed in parallel, shortening project cycle time. In system integration and troubleshooting, the same technique permits rapid identification of faulty units.

Equipment currently used depends on the device under test; switch boxes, I/O cards, processor development systems and IC testers are typical examples. However, because factors such as throughput, operator skill and equipment availability are often as significant as the actual test requirements, it is often difficult economically to match the capability to the requirement.

Promising help in this direction is a new application note, AN #296 from HP. It tells how stimulus requirements have been solved conveniently, flexibly and at a low investment. Each description includes the conditions under which the tests are made and the reasons for the choice of solution. The examples extend over a wide range of activities in the design, manufacture, and support of digital and hybrid ICs, decoders, peripherals and interface busses.

Check **L** *on the HP Reply Card for your free copy of AN #296.*



This new publication presents convenient stimulus solutions for multichannel digital devices in a wide range of design, manufacture and support activities.

New OEM modular power supplies feature 200 kHz switching

Using 200 kHz MOS power FET switching technology, Hewlett-Packard has designed a new family of 50 W power supplies featuring reduced size and weight, and improved reliability. Designers can choose from eight different models in the 65000A-Series Power Supplies specifically developed to power microprocessor-based products such as microcomputers and peripherals, communication devices and test equipment.

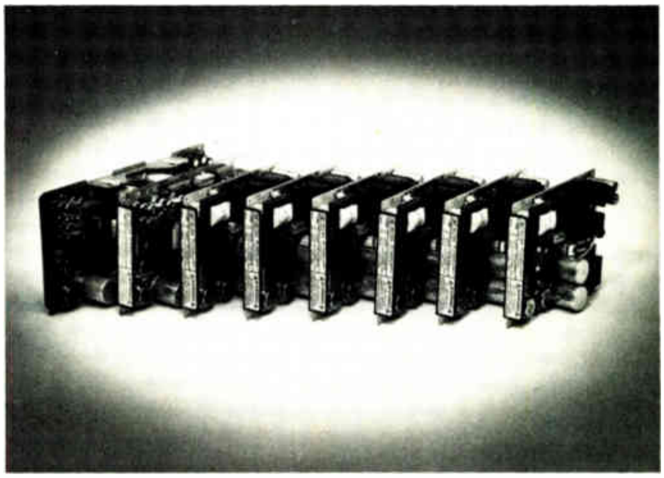
A key feature of the design is that selectable input voltage ranges make the supply adaptable to worldwide use. The supply is UL-recognized to UL487 and UL114. It is certified to CSA 22.2 No. 143 and No. 154, and also meets the requirements of VDE 0730 Part 2P and IEC 348. In addition, the supply is brownout-proof and has overvoltage and short-circuit protection. Power system management is provided by the remote shutdown terminal.

Three groups make up the family including single, triple, and five or six output models. Each group uses a different printed circuit card with a form factor that makes mounting or removing the card from the mainframe simple. Optional board-edge connectors allow the designer to choose from a variety of plug-in and screw-type terminals.

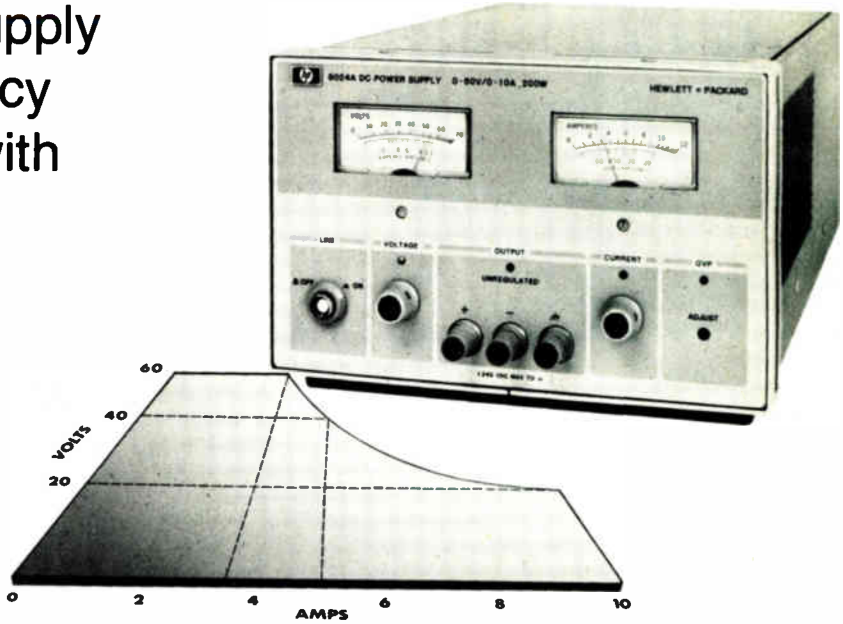
The main output in each group, V1 uses a control reactor that adjusts the operating frequency to maintain 0.1% output voltage regulation. In multiple-output models, two semi-regulated V2 and V3 outputs also serve as a source for outputs V4, V5, and V6 via discrete regulators.

Price for the Hewlett-Packard 50 watt power supply varies depending on the number of outputs and the quantity ordered. The 50-W power supplies are priced at $154 for single-output models 65105A, 65112A, and 65115A; $190 for three-output models 65312A, 65315A, and 65317A; $201 for five-output model 65512A, and $209 for six-output model 65612A. All in quantities of 1,000.

Check **M** *on the HP Reply Card.*



An advanced power supply combines high frequency switching technology with autoranging



Hewlett-Packard's new autoranging power supply is designed to meet the exacting requirements of a laboratory environment,and to have the flexibility required in automated test and control systems.

System designers who frequently need a variety of power supplies in a system to provide an adequate range of operating power or stimuli to a device under test can now have the same capability in a single instrument, the HP 6024A Autoranging Power Supply. The resulting savings in space, interface complexity and equipment expense are significant.

The 6024A provides maximum output power over a wide and continuous range of voltage and current combinations without having to manually select the proper output range. This feature, unlike conventional constant voltage/constant current power supplies (which provide maximum output power at only one combination of output voltage and current), makes the 6024A a convenient and cost-effective unit capable of satisfying many different dc requirements. For example, an engineer would need a 20 V, 10 A supply; a 40 V, 5 A supply, and a 60 V, 3 A supply to cover a range similar to that of the 6024A.

In addition to autoranging, the 6024A has many features which make it a versatile lab and system supply including mode and status indicators, adjustable overvoltage protection, two 10-turn potentiometers for high resolution control, amplified current monitor terminals, as well as voltage and current meters. A barrier strip at the back of the supply provides the necessary terminals for current monitoring, remote programming and remote sensing. The 6024A uses switching regulation which contributes to the compact size, light weight and high operating efficiency.

Optional Interface

Interface Option 002 provides a convenient, low-cost means of integrating the 6024A into a system. A single, field-installable PC board provides system designers with remote programming, status readback, remote shutdown and output bias supplies.

*Check **N** on the HP Reply Card for more details.*

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HEWLETT PACKARD

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

September/October 1980

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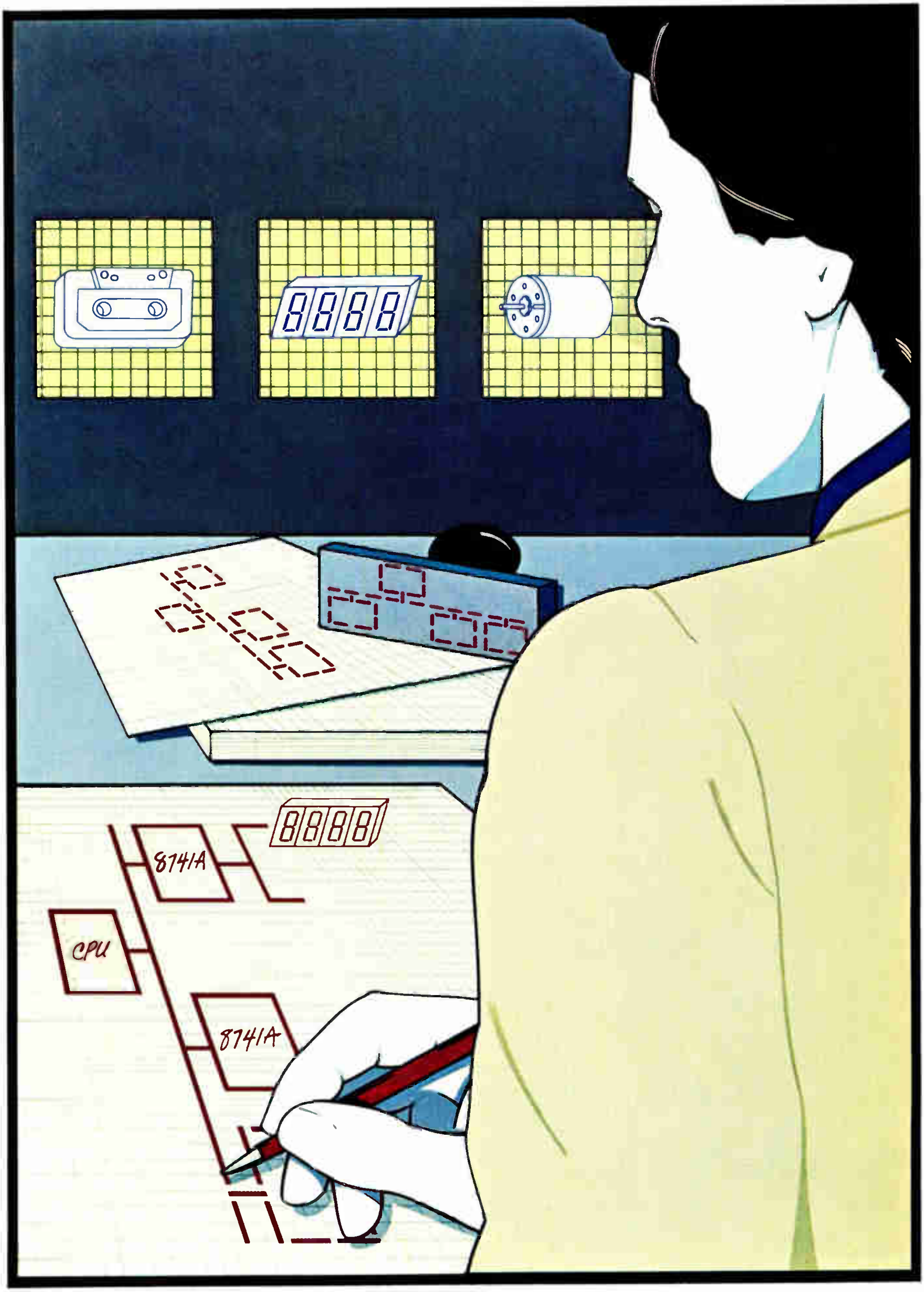

8741A
CPU
8741A

Consider the Options

Choose Intel's 8741A: the only peripheral controller with on-chip EPROM memory and unparalleled development support.

For almost any application where a system peripheral device interfaces to a microcomputer, Intel delivers the flexible design solution: our 8741A. It's the only UPI™ controller in the industry to give you EPROM memory *and* vital support that minimizes design and debug time. It's the proven peripheral controller available now . . . in your choice of ROM and EPROM versions.

Easy-to-instruct slave processor puts you in control.

If you demand more flexiblity from your controller, our 8741A delivers. The 8741A assures that everything from keyboard control to complex process control tasks within your system design can now be efficiently developed as separate projects . . . simplifying your design and making your project more manageable.

Because Intel's 8741A controller is a true slave processor, it acts under control of the host processor. And it never monopolizes the system bus. By executing macro commands from the host, our UPI controller executes from on-chip program memory . . . operating in parallel with the host CPU and freeing the host CPU to do its job.

More than just an intelligent controller, our 8741A contains an 8-bit CPU, 1K byte program memory, 64 byte data memory, clock, timer/counter plus I/O ports. But the performance features of Intel's 8741A go way beyond that.

EPROM programmable memory helps stamp out high design costs.

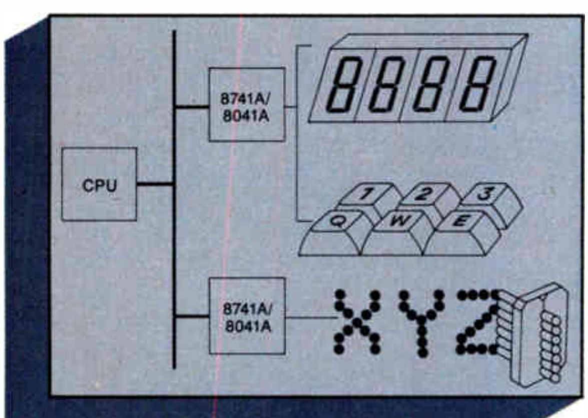
In terms of both redesign and testing, Intel's 8741A with on-chip memory offers freedom and flexibility to incorporate new features into the controller. No cost sacrifices or wasted time. Change your software as many times as necessary during development, or when new features are added to the product.

When your programs have been developed, just switch to our pin-compatible ROM version of the UPI controller, our 8041A . . . it's the economical solution for volume production usage.

A versatile controller with an easy instruction set.

If you're familiar with the instruction set for Intel's industry standard 8048, you've already made the investment in learning the instructions for our 8741A. The majority of the 8741A's instructions are control oriented, so you can easily program your controller to handle a wide range of I/O tasks.

The result? Our 8741A, a controller for peripheral devices that have no other "off-the-shelf" solution.



No other development support can serve you better.

Intel doesn't just deliver a powerful controller, we also give you powerful debug tools. With our ICE-41A™ in-circuit-emulator, Multi-ICE™ software package and Intellec® development system, you can locate design flaws and software bugs in even the most complex multiprocessor designs.

Consider Intel's ICE-41A emulator and Multi-ICE software as your direct diagnostic connection. With Intel ICE™ modules, you can debug the peripheral controller and an entire system . . . all in real time. You can also rely on Intel to deliver Multi-ICE software. This unique tool lets you have two ICE modules running in parallel, plus macro and compound command extensions to the ICE-41A software that reduce testing time, errors and inconsistencies.

The ICE-41A module lets you use English-like commands and symbolic debugging to monitor hardware and software operation. It lets you modify registers, memory locations and I/O ports. With ICE-41A modules, Intel delivers the only intelligent solution for designing intelligent controllers.

Intel's 8741A, the designer's choice.

If you want shorter design cycles, cost reduction, reliability and performance, you want Intel's 8741A. Proven in hundreds of designs worldwide, it's the best supported UPI controller you can incorporate into your design. And it's available in quantity now.

For more information, contact your local Intel sales office or distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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Military Microwaves 80, Institution of Electronic Engineers (Savoy Place, London WC2R 0BL, England), Cunard International Hotel, London, Oct. 22–24.

Integrated Circuit Quality Control Workshop, American Society for Quality Control, Electronics Division (Ralph A. Evans, IC-QC, 804 Vickers Ave., Durham, N. C. 27701), Durham, Oct. 23–24.

1980 Fall Meeting—Electronics Division of the American Ceramic Society (65 Ceramic Dr., Columbus, Ohio 43214), Sheraton Palace Hotel, San Francisco, Oct. 26–29.

10th Annual Monterey Conference, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Del Monte Hyatt House, Monterey, Calif., Oct. 26–29.

10th Annual North American Thermal Analysis Society Meeting (Robert C. Johnson, Du Pont Central Research and Development Department, Experimental Station, Bldg. 228, Wilmington, Del. 19898), Copley Plaza Hotel, Boston, Oct. 26–29.

1980 Conference on Electrical Insulation and Dielectric Phenomena, National Research Council Assembly of Engineering (2101 Constitution Ave., Washington, D. C. 20418), Parker House, Boston, Oct. 26–30.

ACM Annual Conference, Association for Computing Machinery (1133 Avenue of the Americas, New York, N. Y. 10036), Opryland Hotel, Nashville, Tenn., Oct. 27–29.

Compsac80, Fourth International Computer Software and Applications Conference, IEEE, Palmer House, Chicago, tutorials Oct. 27–28, conference Oct. 29–31.

NEC-NCF/80, 36th Annual National Electronics Conference and National Communications Forum, National Engineering Consortium Inc. (Oak Brook Executive Plaza No. 2, 1211 W. 22nd St., Oak Brook, Ill. 60521), Hyatt Regency O'Hare, Chicago, Oct. 27–29.

ICCC/80—Fifth International Conference on Computer Communication, International Council for Computer Communications (ICCC/80, Box 280, Basking Ridge, N. J. 07920), Peachtree Plaza Hotel, Atlanta, Oct. 27–30.

1980 Photovoltaic Solar Energy Conference, IEEE and Commission of the European Communities, Palais des Festivals et des Congrès, Cannes, France, Oct. 27–31.

17th Department of Defense–Association of Old Crows Electronics Warfare Symposium, AOC (15233 Ventura Blvd., P-8, Sherman Oaks, Calif. 91403), Disneyland Hotel, Anaheim, Calif., Oct. 28–30.

Fourth Annual Symposium on Computer Applications in Medical Care, George Washington University (Janice W. Eldridge, Registrar, SCAMC, Office of Continuing Medical Education, 2300 K St. N. W., Washington, D. C. 20037), Capital Hilton Hotel, Washington, D. C., Nov. 2–5.

Autotestcon '80, IEEE, Sheraton Washington Hotel, Washington, D. C., Nov. 3–5.

Midcon/80, IEEE, Dallas Convention Center, Dallas, Texas, Nov. 4–6.

Electronica 80—Components and Assemblies Trade Fair and Microelectronics Congress, MMG P. O. Box 121009, 8000 Munich 12, West Germany), Fairgrounds, Munich: Fair, Nov. 6–12; Congress, Nov. 10–12.

AEA Human Resources Symposium, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Hotel del Coronado, San Diego, Calif., Nov. 9–12.

SMPTE Technical Conference and Equipment Exhibit, Society of Motion Picture and Television Engineers (Conference Department, 862 Scarsdale Ave., Scarsdale, N. Y. 10583), New York Hilton Hotel, New York, Nov. 9–14.

26th Annual Conference on Magnetism and Magnetic Materials, IEEE and the American Institute of Physics, Dallas Hilton, Dallas, Texas, Nov. 11–14.

1980 IEEE Engineering Management Conference, IEEE, Colonial Hilton Hotel Inn, Wakefield, Mass., Nov. 12–14.

Semicon Japan '80, Semicon Japan Secretariat (4-8-19 Akasaka, Minato-ku, Tokyo 109, Japan), International Fairgrounds, Tokyo, Nov. 15–21.

Annual Meeting, Materials Research Society (102C Materials Research Laboratory, University Park, Pa. 16802), Copley Plaza Hotel, Boston, Nov. 16–20.

AEA East Coast Financial Conference, American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Radisson Ferncroft Hotel and Golf Course, Danvers, Mass., Nov. 17–19.

14th Annual Asilomar Conference on Circuits, Systems and Computers, IEEE, Asilomar Hotel and Conference Grounds, Pacific Grove, Calif., Nov. 17–19.

Autofact West, Society of Manufacturing Engineers (1 SME Drive, P. O. Box 930, Dearborn, Mich. 48128), Anaheim and Disneyland convention centers, Anaheim, Calif., Nov. 17–20.

INFO/MFG—Information Systems for Manufacturing Companies, Clapp & Poliak Inc. (245 Park Ave., New York, N. Y. 10017), McCormick Place, Chicago, Nov. 18–20.

Electro Optics/Laser 80 Conference and Exposition, Industrial & Scientific Conference Management Inc. (222 W. Adams St., Chicago, Ill. 60606), John B. Hynes Veterans Auditorium, Boston, Nov. 19–21.

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Channels: 32 data to 12 MHz,
16 data to 70 MHz
16 timing to 100 MHz
Memory: 1024 words @ 16 channels
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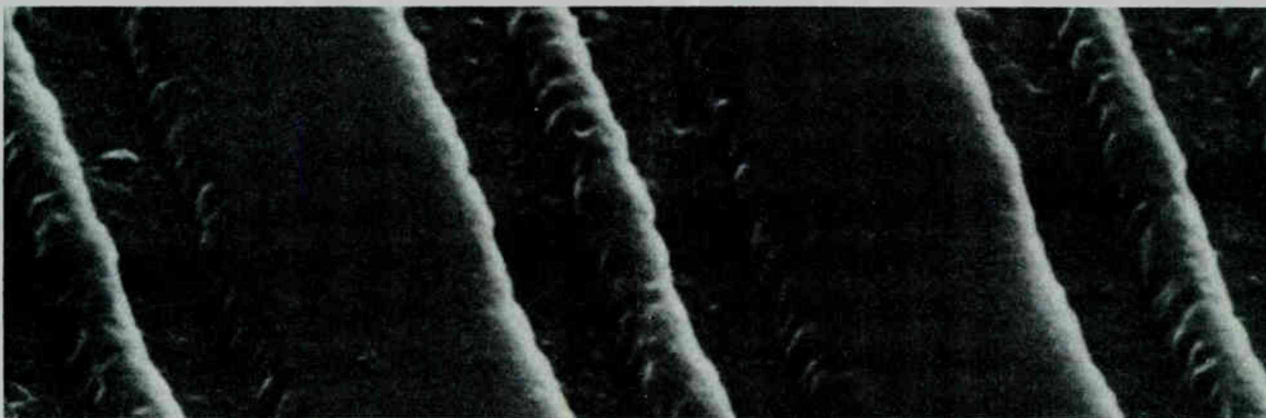

1.0 micron lines over 0.8 micron aluminum steps.

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The UV-3 option provides 1⅛ micron resolution while maintaining good process latitude and the high thruput that is characteristic of Perkin-Elmer Micralign systems.

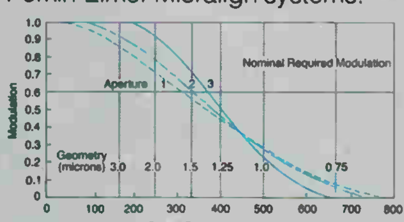

Figure 1. Model 200 (4000 Angstroms)

With diffraction-limited optical systems, resolution is inversely proportional to the exposing wavelength without a sacrifice in depth of focus. Figures 1 and 2 illustrate the improved resolution, as a function of partial coherence, of the UV-3 option as compared to a standard 200 Series exposing at the standard wavelength. The modulation for very small feature sizes is significantly improved.

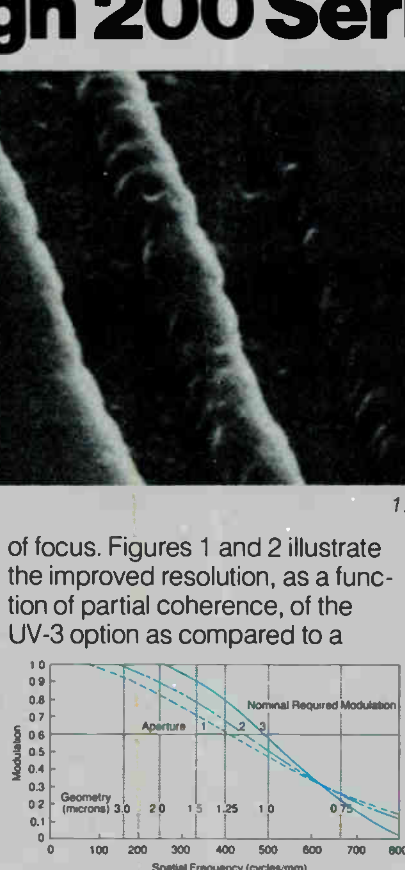

Figure 2. Model 200 UV-3 (3000 Angstroms)

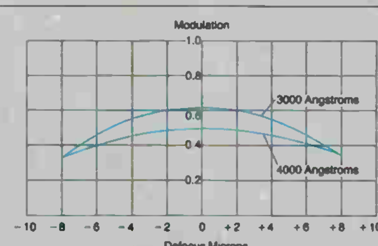

Figure 3. Diffraction-limited modulation. 1.5 micron lines and spaces (333 cycles/mm) with incoherent illumination

Figure 3 illustrates the critical fact that the use of shorter exposing wavelength to obtain greater resolution does not sacrifice depth of focus.

The UV-3 option can be ordered on any model of the Micralign 200 Series. This lets you select the correct Micralign instrument for your application.

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Responsive Technology

32-bit Vision family a year or more away at Hewlett-Packard

The long-awaited entry by Hewlett-Packard Co. into the 32-bit computer fray will be made by the Vision computer family of processors and operating systems, though the machines might not appear for another year or more. Downward-compatible with existing HP 3000 computers and operating systems, **the Vision family is being designed to eventually replace the 3000.** Although most of the Vision development will be concentrated in the new Computer Systems division, in Cupertino, Calif., the low end of the line will be developed at the Desktop Computer division in Fort Collins, Colo. HP's first software unit, the Information Systems division, will develop and market business software for the Vision line.

Electrochemical method cuts cost of substrate tests

Engineers at Sperry Gyroscope Co., Great Neck, N. Y., have come up with a major advance in the testing of complex multilayer substrates used for large-scale thick-film hybrids. The new method, described in a paper by Robert Ost at last week's ISHM 80 International Microelectronics Symposium, **allows 100% continuity testing with a much lower labor and equipment cost than current methods.** In the Sperry system, a patented electrochemical technique allows batch testing of substrates. Tagged Substrate Integrity Test Equipment, or SITE, the new system allows a known good substrate to be compared visually with those under test. A group of identical probes are positioned on the same nodal circuit of each substrate in a batch, all of which are housed in a large plastic tank. The introduction of an electrolytic solution into the tank causes a significant pulsing color change of all points connected to the node, so that comparison with the good substrate readily reveals shorts and opens.

DEC working on two additional VAX systems

Digital Equipment Corp.'s 32-bit VAX-11/750 [*Electronics*, Oct. 9, p. 33] is only one of the new VAX systems coming. Researchers are also at work on Nebula, an LSI-11 version of the VAX-11/780. It will be designed as a multichip set that is very much in the domain of very large-scale integration. The Maynard, Mass., firm is designing chips with a new composition strategy in computer-aided design that promises to be **an alternative to the gate-array approach used on the VAX-11/750.** Nebula, which will have the full 32-bit architecture of the VAX-11/780 but at one third the speed, is at least a year away from announcement and is expected to have a central processing unit that costs less than $10,000. The other VAX system under development is code-named Nova. It has twice the speed of a VAX-11/780 and is to appear in less than a year.

Instrument houses readying hand-held 4½-digit DMMs

New 4½-digit hand-held digital multimeters are being polished up by at least three firms and should be on the market soon. Data Precision Corp. will introduce its model 255, which the Danvers, Mass., firm says will offer **high accuracy, a rechargeable battery pack, and a price in the $280 range.** Also, Keithley Instruments Inc. of Cleveland should weigh in with its model 135. Shown privately at the recent Interkama Exhibition in Düsseldorf, West Germany, the meter has fewer ranges and less accuracy than the 255 but will command a lower price, probably about $225. Other firms said to be developing hand-held 4½-digit models are Beckman Instruments Inc., LaBrea, Calif., and the John Fluke Manufacturing Co., Mountlake Terrace, Wash.

Electronics newsletter

Scanning system cuts backplane flaws, speeds wire-wrapping

A new optical-scanning system may drastically cut backplane interconnection time in the wire-wrapping process, according to spokesmen for Connection Systems Inc., a subsidiary of Teradyne Inc. The Nashua, N. H., facility has developed a computer-controlled video scanner **that senses the position of pins on backplanes to within a few thousandths of an inch.** The system straightens misaligned pins and notes missing pins to be added later. Since each bent or missing pin means a stop for human aid, even a few can greatly slow operations.

Exxon cuts back at Kylex, starts up electrophoretics unit

It looks as though Exxon Enterprises Inc. may have hit a dry well at its Kylex Inc. affiliate in Mountain View, Calif., which last year announced the development of a flat-panel liquid-crystal display that uses complex multiplexing to drive its 40 characters [*Electronics*, Nov. 22, 1979, p. 46]. Exxon has chosen not to fund production of Kylex LX140S, a very thin LCD package that was to replace the initial LX140 display, no longer in production. **Instead, Kylex will halve its staff of about 100.** Meanwhile, Exxon's Electrophoretic Information Displays, or EPID of Sunnyvale, Calif. [*Electronics*, Jan. 31, p. 33], is stepping up its search for "ground-floor" managers who will set up pilot production for flat-panel displays to be implemented with n-MOS or complementary-MOS custom chips.

Polyimide tape blocks alphas on TI chips

To thwart alpha particles interfering with its 64-K random-access memory, Texas Instruments Inc., like most manufacturers, coats dice with polyimide. But instead of applying a liquid, which can yank bonds loose and leave vulnerable thin regions, the Dallas firm bakes a 3-mil-thick polyimide tape onto each chip's storage array, cutting alpha-induced errors to zero. **Ultimately, it may silk-screen liquid polyimide onto full wafers.**

TI's 64-K RAM to appear in 16-by-4-bit version

Texas Instruments Inc. will bring out a 16-K-by-4-bit version of its 64-K random-access memory, probably next year. Its present 64-K architecture lends itself to the new organization, since a one-out-of-four decoding operation is performed that can simply be eliminated. And in static RAMs, using only circuit techniques, TI **expects a 35-ns access time on a future version of the 4-K 2147** without scaling down to its second-generation high-performance MOS process. When it does scale down, it hopes to offer a 45-ns 2167 static RAM with a 35-ns speed selection.

Addenda

Dionics Inc., a supplier of power switching devices, is now entering the solid-state relay market. **Combining its DI-16V8 dielectrically isolated photovoltaic diode array chip and an infrared light-emitting diode in a single package,** the Westbury, N. Y., firm will supply the basic relay mechanism for applications requiring an output of up to 8 V and 3 μA. . . . A formidable new competitor in data communications has been formed by Honeywell Inc. of Minneapolis and SESA (Société d'Etudes les Systèmes d'Automation) SA, a French company **that has installed more than 100 message-switching and custom data-communications systems** in Europe, Africa, and North America. The combine will be called SESA-Honeywell Communications Inc. . . . Harris Corp.'s Semiconductor Group is going to add five buildings (275,000 ft^2), to its Melbourne, Fla., complex.

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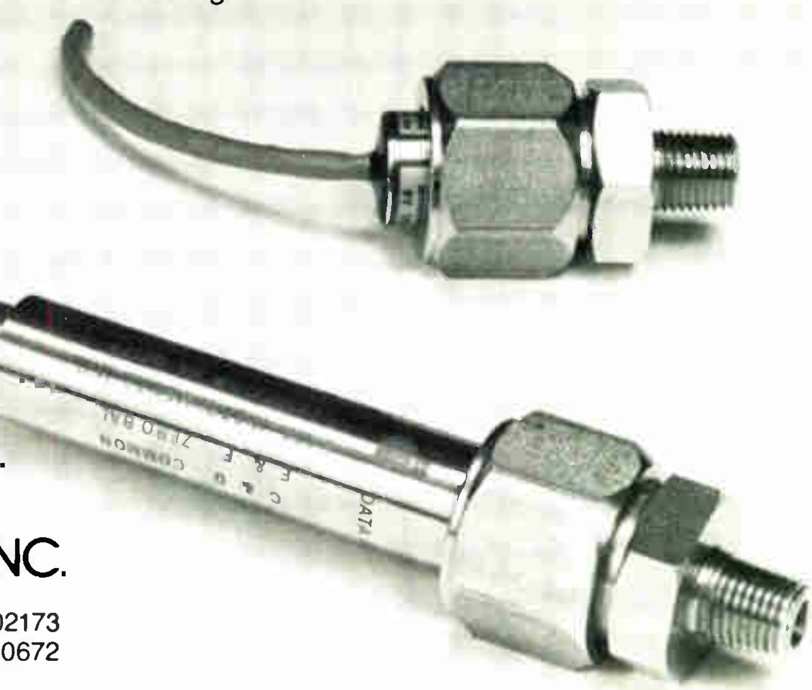

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Because the μPD 7201 allows you to select any of the most popular communications protocols just by making a simple software adjustment. You can choose async, bisync, monosync, external sync, HDLC, or SDLC.

The 7201 also offers you flexibility in transmission modes by allowing you to select character length, parity, sync characters, CRC Algorithm and transmission rates up to 880K baud rate. Each channel can be set independently, and modem control signals are provided.

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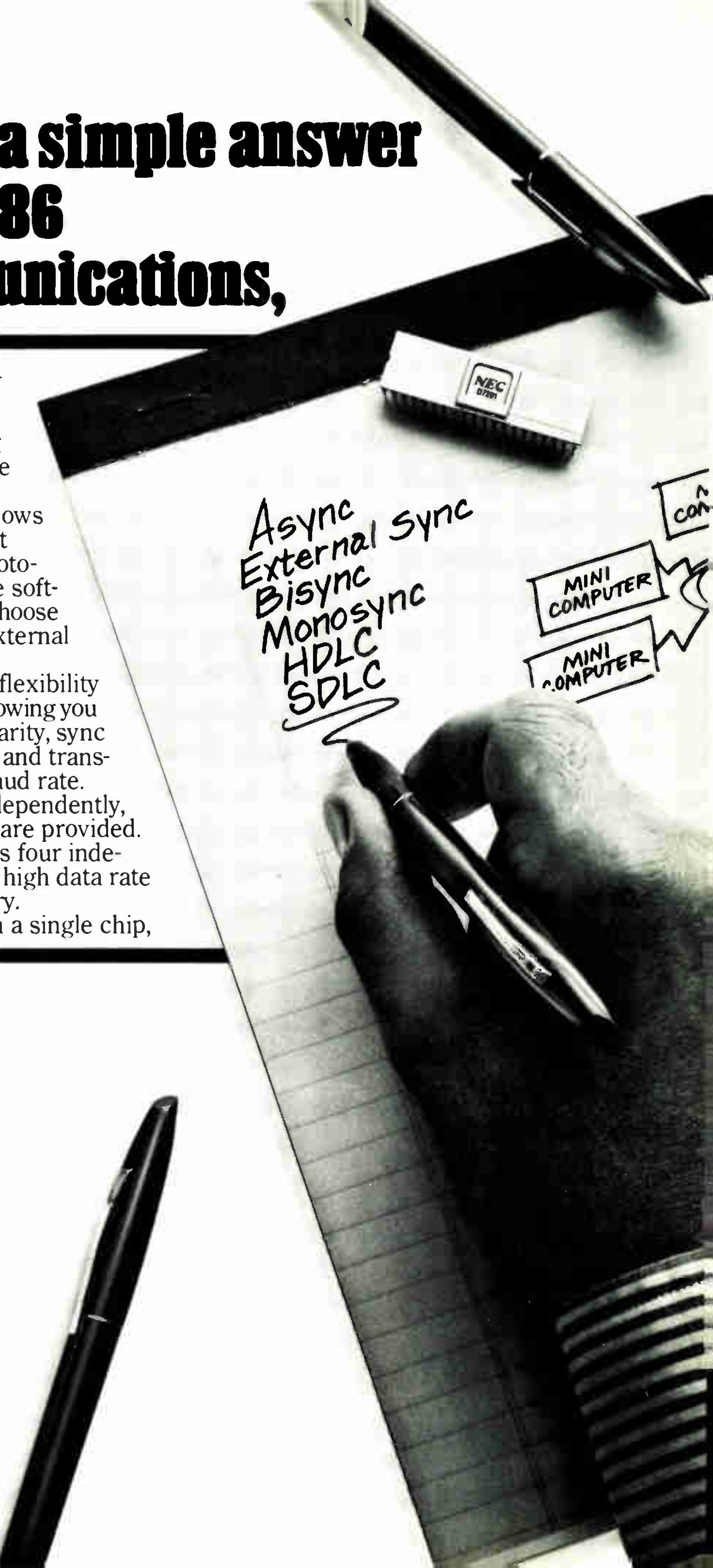


Z9000 chip to aim at easing the use of virtual memory

by R. Colin Johnson, Microsystems & Software Editor

New Zilog 16-bit processor will be speedier; refined access to virtual memory lessens risk of losing data

The second generation of 16-bit microprocessor designs is on the drawing boards, and Zilog Inc. looks to be in the lead with a successor to its popular Z8000. Pin-compatible with its predecessor, the Z9000 will incorporate added functions for easier implementation of computing systems, and it will work with an updated memory management unit for better implementation of virtual memory.

The Cupertino, Calif., subsidiary of Exxon Enterprises Inc. says the new microprocessor will run about 1.5 times faster than the 6-megahertz Z8001. In fact, it claims the Z9000 will benchmark one to one with the PDP-11/70 minicomputer when it is available in the second quarter of 1981.

As the figure shows, the new chips will eliminate much of the circuitry necessary to marry them by absorbing it on chip: each will have 5% to 10% more circuitry on a 15% smaller die. Another benefit will be elimination of the software initialization routines, because the fixed configuration of these new chips permits these functions to be hardwired.

The chief aim of the new processor and the forthcoming MMU redesign is to refine the implementation of virtual memory. Adapted from the mainframe and minicomputer worlds, the virtual memory concept lets the processor treat every memory location in the system as if it were main memory, even if it is on disk or on tape.

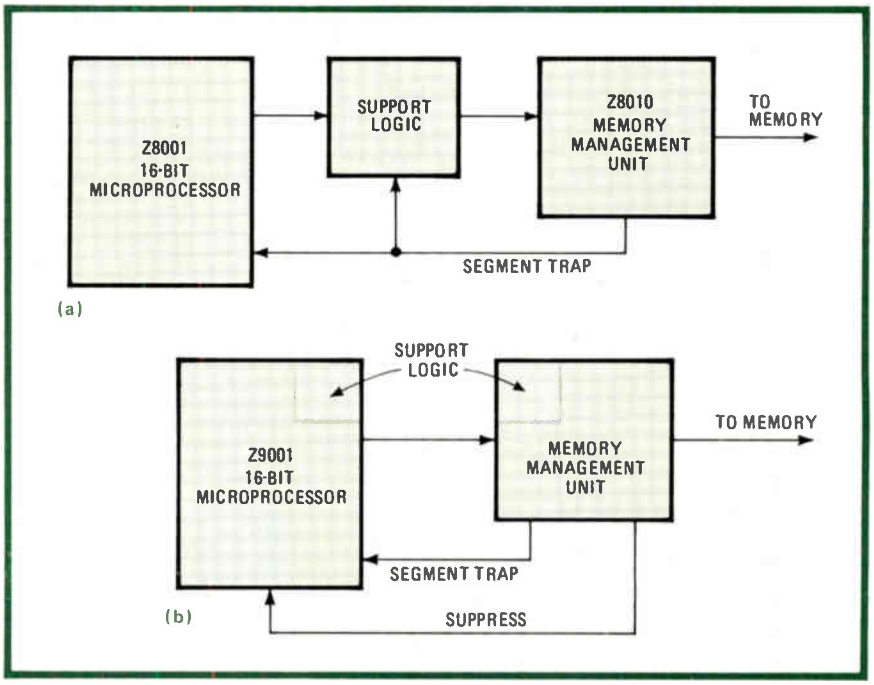
However, when a program requests a location out of main memory, the processor must abort that instruction in order to save the state of the machine until it fetches the necessary new data. Current microprocessors cannot do this, so there is the danger of losing the data associated with that instruction.

The tack to be taken by the Z9000 and by National's 16000 [*Electronics*, April 24, p. 123] when it appears next year will be to include an instruction-abort pin for backing up the processor one instruction. The new Zilog processor will use what is the no-connect pin on the Z8001.

The new MMU will retain the company's segmented approach to memory management (the Z8002 will continue as the 16-bit offering that works with a single 64-K-byte memory space). Each memory segment can store up to 64-K bytes, the precise size being programmed into the MMU by the processor.

Paging. Future versions will include an advanced paging system, similar to those on modern minicomputers and mainframes, that keeps only a page of, say, 512 bytes of the program in main memory at any one time. When execution reaches the end of a page, a new one is swapped in from disk in a mode transparent to the user.

Since paging slashes the amount



More on chip. The Z9000 and accompanying memory management unit will incorporate support logic and eliminate software initialization, thereby easing system implementation.

of main memory dedicated to any one program, it can be a boon in multiuser configurations. The Z9000 series MMU will be designed for easy implementation of paging later on.

Although virtual memory eases management of the large amounts of storage in multiuser setups, the other two major 16-bit processor makers, Intel and Motorola, have put off implementation of the concept. Intel has concentrated on peripherals for fast number crunching, typically performed in single-task systems, whereas Motorola is still designing such peripheral chips as the MMU.

Information processing

Ethernet is up to date but without surprises; local net concept has 10-Mb/s data rate

A novel combination of advanced technologies, but no surprises for the user: that sums up the long-awaited specifications for Ethernet, the local data-communications network concept being promoted by Xerox, Digital Equipment Corp., and Intel.

Ethernet [*Electronics*, Oct. 9, pp. 34 and 48] promises to allow almost any intelligent office equipment to communicate with any other, regardless of manufacturer. Backed by giants Xerox Corp. of Stamford, Conn., DEC of Maynard, Mass., and Intel Corp. of Santa Clara, Calif., its marketing clout will be of the first rank. What's more, a standards committee of the Institute of Electrical and Electronics Engineers is about to consider it as a local-net standard.

A coaxial cable system, Ethernet is set up for a data rate of 10 million bits a second, using the well-known Manchester encoding technique. The 50-ohm system will have 500-meter-long segments, although multiple segments may be interconnected through repeaters. As many as 100 transceivers per segment can be accommodated.

Packet-switched Ethernet uses the datagram concept to provide its service, and the links are controlled by contention arbitration and collision detection. If a collision is detected, there is a random interval before transmission is again attempted.

Frame. A typical Ethernet frame (see figure) has a preamble, a destination address, a source address, a type field, and a data field. Except for the preamble, all of the fields are covered by a 32-bit cyclic redundancy check.

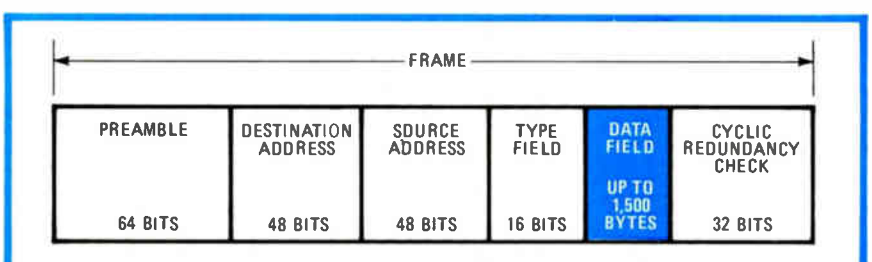
The preamble provides for bit synchronization and marks the frame boundary. The two addresses have the same format: a 48-bit field with 2^{47} physical addresses, one broadcast address, and the rest multicast addresses. The type field is a 16-bit field used to designate higher-level protocols. And, most important from the user point of view, the information field provides up to 1,500 bytes of user data per frame.

Transceivers hooking up the various data-generating and -receiving machines in the net will be designed by DEC. Intel is designing microprocessors and other chips that make up the network controllers and drivers. Both firm's offerings will go on the market for sale to original-equipment manufacturers. The concept's originator, Xerox, is, of course, interested in office equipment.

So anxious is Xerox to make Ethernet a standard that it is just about giving away the technology, which it developed over the past five years for internal use. According to David E. Liddle, vice president for systems development of the Office Products division, the data-communications community can have it at what amounts to "just the cost of furnishing the paperwork:" a one-time $1,000 fee.

The three-company effort has jumped ahead of the competition by publishing specifications and by submitting Ethernet to the IEEE for consideration as a possible standard. However, its acceptance is far from ensured, since there are many other possibilities for standards, some of them not yet announced.

Probably Ethernet will turn out to be one of several standards, depending on the type of service provided and equipment accommodated. There are too many vested interests for any one standard to do the whole job: among the concerned parties are IBM, AT&T, Exxon, Honeywell, SBS, the military, and the U. S. government. **-Harvey J. Hindin**



Frame-up. The typical Ethernet frame will provide up to 1,500 data bytes; the 32-bit CRC covers destination and source addresses and type field, as well as the data field.

IBM to interconnect local networks

Looking forward to the time when local nets are as common as computers, International Business Machines Corp.'s Federal Systems division is extending the networking concept even further into what it calls internetworking. The goal is to learn how to connect local networks without infringing upon their operations in any way.

The work is in the early stages, said Ed C. Hendricks of the division's San Diego operation at a recent IBM seminar in Yorktown Heights, N. Y. The project, he says, is simply a study of the best ways to let one network talk to another transparent to the user.

The division is giving much attention to gateways that would connect local nets. Using the datagram concept [*Electronics*, Sept. 25, p. 118], these gateways would provide such functions as addressing, protocol management, and formatting.

However, Hendricks insists that IBM is not developing a product. Still, it is clear that IBM is keeping a sharp eye on office-of-the-future requirements.

For maximum communication among the expected diversity of local nets, host-to-host protocols are required. "There are three or four major and many minor host-to-host protocols" to worry about, observes Hendricks, so that gateway design is no easy feat.

Dynamic programming. Like all packet-switched data streams, datagrams may be routed by a variety of communications modes. IBM's internetworking will therefore use dynamic programming to find the shortest available path for each internet message, says mathematician Michael Engel. What's more, there will be efficient routing procedures to transmit messages around malfunctioning gateways.

The IBM internetworking concept may be traced to the Arpanet system, to which the corporation was a prime contributor. The universities and Government agencies on the system use its packet switching for communications among their local computer nets.

During the past few years, the Arpanet community has been working on an improved gateway concept. Coherent cross-network communications would continue, while the individual local nets on a campus or within an agency could perform concurrent internal operations.

According to IBM, the new basic Arpanet functions are in operation within the Department of Defense and several participating universities. Moreover, the associated protocols have been established as DOD standards and have been submitted to the International Standards Organization. **-H. J. H.**

More chip shrinks plus C-MOS processes are Intel's game plan to stave off competition

Capitalizing on its quick-turnaround computer-aided design system, Intel Corp. is mounting a major drive to shrink and speed up its microprocessors and other logic elements, converting them to its advanced high-performance, or H-MOS, processes. What's more, to fight off low-power copies, its long-rumored high-performance complementary-MOS process will appear in 1981.

Its target is competitive integrated circuits that duplicate its popular chips. For example, Intel-type products are winning over half the market for 8-bit processors, but the Santa Clara, Calif., company receives less than half of the revenues and little recompense in royalties. So it plans to outmaneuver the competition by rapid computer shrinks.

"We have over 100 products to go through these steps," says Jack Carsten, vice president and general manager of the Microcomputer Components division. "We want to correct the image that we quit selling a product once its price drops."

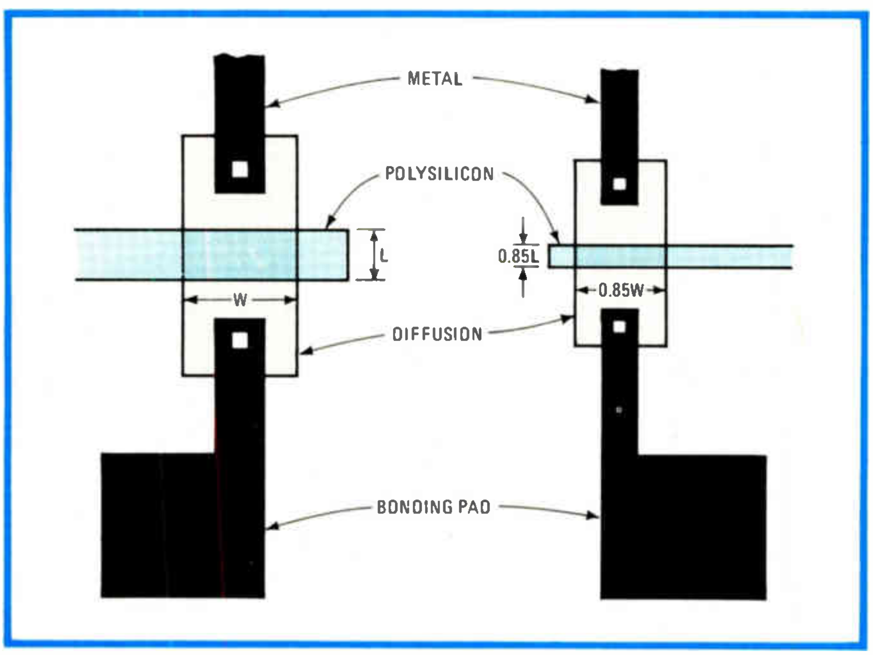
Though other companies can and do duplicate Intel's ICs, they cannot as easily duplicate the data base built up for its CAD system. In effect, Intel can simply tweak a few design variables for smaller, faster, lower-power versions of its circuits.

Savings. Carsten notes the CAD system "does not rely on optical shrinks or redesign. So what traditionally costs from $500,000 to $1 million becomes $50,000."

Moreover, the software conversion from process to process scales down only areas of interest like channel dimensions, for example, leaving bonding pads full size (see figure). A brute-force optical shrink by an imitator could cause problems like bonding pads too small to work with.

The scaled-down MOS ICs are intended to be at least one jump ahead of the competition in terms of performance and cost. However, Intel has another card up its sleeve.

"We have a C-MOS process, but



Discriminating shrink. Since Intel can use a CAD system to shrink the chips it was used to design, the firm can scale down only the areas of interest like channel dimensions.

we've been holding back on its introduction, waiting for H-MOS levels of performance and density," Carsten says. In fact, due next year is "a whole set of C-H-MOS processes. We will have to redesign a chip in C-MOS, but once there we'll be able to scale it or add erasable programmable read-only memory just as we can with n-channel MOS."

The new H-MOS campaign will benefit the 8088 microprocessor and the 8021, 8049, and 8051 single-chip microcomputer families. Although the 16-bit 8086 microprocessor and 8048 microcomputer were not designed for the CAD scaling process, their design parameters are now digitized for compatibility with the system.

Remakes. The 8-bit 8048 is a good example of what Intel is up against. Since its introduction in 1977, it has inspired more remakes than has the 8-bit 8080 microprocessor.

Building on the unit's fundamental architecture, one of the alternative sources—National Semiconductor—has an 8050 with four times the 8048's program memory [*Electronics*, Oct. 9, p. 194]. Others are recasting the 8048 in C-MOS for far superior power specifications. The 80C48 from Nippon Electric [*Electronics*, Oct. 9, p. 206], for instance, can idle on 500 microwatts, compared with the original 8048's 75-milliwatt standby consumption.

In response, Intel recently scaled down the 8048 using its H-MOS process. It got a low-power 8048L that consumes 200 mW at 4 megahertz, an H version that uses 400 mW at 8 MHz, and a selected H-1 part that hits 11 MHz, a speed that cannot be touched by others. Moreover, using an advanced H-MOS process, the chip will clock at 14 MHz in 1982.

Size reduction will be equally dramatic. Intel's 8049—an 8048 with double the program memory—now measures 250 by 199 mils. H-MOS will reduce it to 167 by 198 mils. By 1982, with advanced H-MOS, Intel expects a 134-by-158-mil die, 42% of the original's area.

Not only should competition be unable to match easily the performance of the new CAD-scaled chips, but also "reverse engineering costs go up astronomically as densities go from 10,000 to 100,000, and with a multichip family you can't just do the processor, you have to do the peripherals, too," says Carsten.

"We have a formula for beating the learning curve without having to redesign. It should generate a lot of production capacity, almost painlessly." **-John G. Posa**

Physics may cramp submicrometer rules

As Intel Corp. continues to scale down device geometries, it expects fundamental electrical limits will ultimately call a halt. And that ultimate could be just another two—perhaps three—generations of integrated circuits away, says Youssef A. El-Mansy, engineering manager at the Aloha, Ore., technology development center.

Unscaled n-channel MOS has been in use for more than five years. Then in 1977 and 1979, Intel applied scaling factors of 0.7 and 0.4, respectively, to channel lengths, oxide thicknesses, and junction depths to obtain the high-performance processes H-MOS and H-MOS II (see table).

Coming. With scaling factors of 0.3 and smaller come 1.5- and submicrometer channel lengths. But El-Mansy's results, presented at the recent International Conference on Circuits and Computers in Port Chester, N. Y., indicate that current gain tops off for a device with a scaling factor of 0.2—that is, for a transistor having a 1-μm channel length and a 200-angstrom gate oxide.

"That is very surprising," he says. "You expect that things will saturate—and they do—but then gain goes back down again." So scaling beyond this point has no effect other than to snarl processing.

Reasons for the peak in performance include velocity saturation and increased channel capacitances. As a channel is shortened, the electric field goes up and carrier speed plateaus to a value based upon scattering. Problems with capacitance arise because the inversion layer remains about 100 Å thick, even as geometries are contracted.

This inversion layer causes channel capacitance to exceed gate capacitance and, as a result, steals an increasing percentage of the gate-to-source voltage. Indeed, for a device with near-equal gate and channel capacitances (which would require 35 Å of oxide or 70 Å of silicon nitride), current is half that with no inversion layer.

Ways out. "You can't do a thing about velocity saturation or the finite inversion-layer thickness," says El-Mansy. But series resistance, which also has been rising to the detriment of performance, "can always be improved with technology." Another method of squeezing out another IC generation is to lower the power-supply voltage, which has so far been held at 5 volts for compatibility with TTL circuitry.

Then maybe a third option is "not

PROCESS PARAMETERS AND GAIN OF SCALED n-CHANNEL MOS

Process	Scaling factor	Oxide thickness (Å)	Channel length (μm)	Series resistance (Ω)	Short-channel gain ($A/V^2 \times 10^8$)
Unscaled n-MOS	1	1,000	5	20	2.35
High-performance MOS (H-MOS)	0.7	700	3.5	28.5	2.96
H-MOS II	0.4	400	2	50	4.06
Advanced H-MOS processes	0.3	300	1.5	66.7	4.35
	0.2	200	1	100	4.8
	0.1	100	0.5	200	4.73
	0.05	50	0.25	400	3.67

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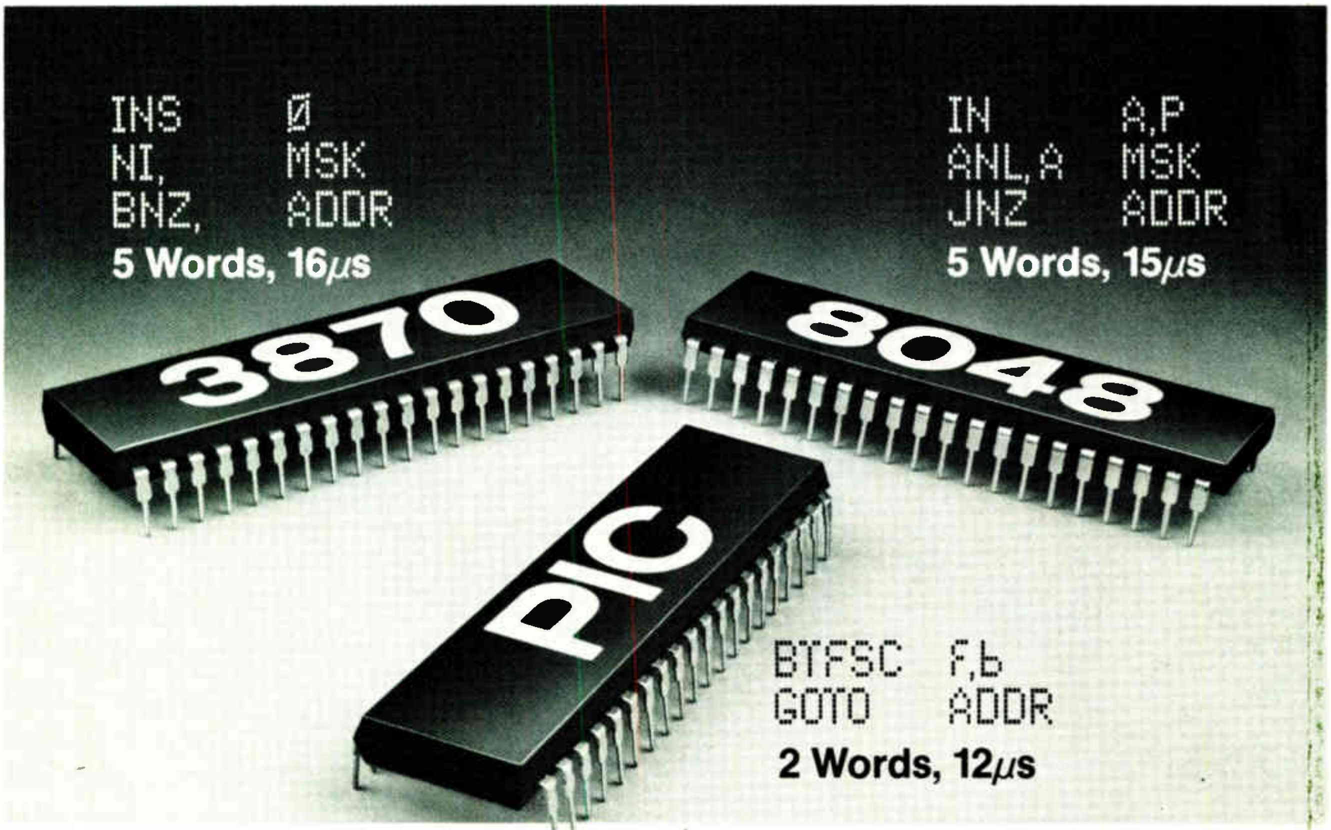

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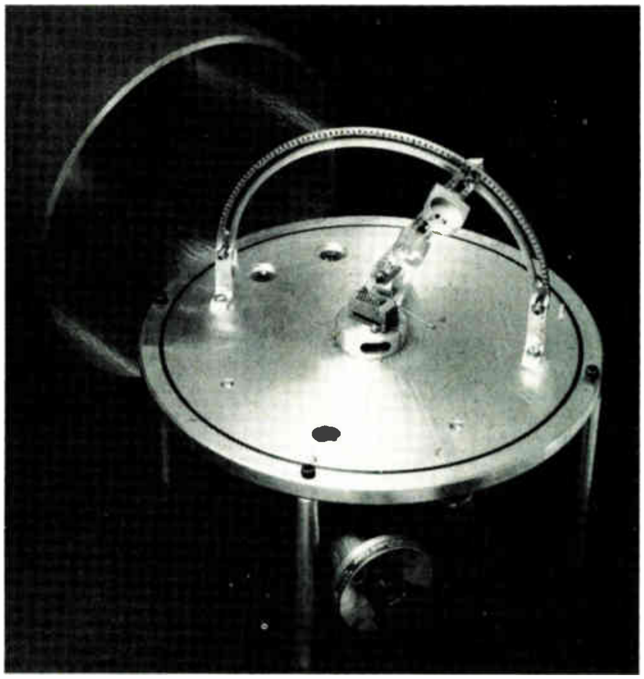
to scale the [gate] oxides so aggressively," El-Mansy continues, but to thin field oxides instead. Lateral geometries have been steadily decreasing over the years, but vertical dimensions have been staying about the same, he explains. Soon, "things will be as tall as they are narrow," and it is almost impossible to control the lithography of such structures.

El-Mansy's observations are not as pessimistic as they sound. Channel lengths of 0.5 μm or even 1 μm would allow enormously dense chips for megabit memories and 32-bit and bigger microprocessors.

However, to put such scaling factors into production would require vast investments in X-ray or electron- or ion-beam lithography. In the meantime, "we can always improve on parasitics," says El-Mansy, by lowering the resistance of polysilicon interconnections, improving chip architectures, and so on. -J. G. P.

Test equipment

Flexible fixture aids alpha-error checks



No air. When the alpha-error test fixture's vacuum cap (rear) is in place, glass-to-metal feedthroughs allow wires from the chip's socket to be brought out to an integrated-circuit tester that analyzes the data.

The unfortunate vulnerability of integrated circuits to alpha radiation is so widely accepted that IC users are beginning to demand soft-error failure-rate specifications for random-access memories and other susceptible chips. So semiconductor makers are showing considerable interest in an alpha-error test fixture developed by a small Santa Clara, Calif., supplier of nuclear instruments and systems.

Working closely with a variety of IC producers, Spectrum Sciences has turned out a fixture designed for flexibility (see photograph). The alpha energy and flux intensity may be varied; the housing of the alpha source can be moved through an arc that gives a ±80° range in the angle of incidence, and a socket holding the IC can pivot 180°.

To vary the alpha rays' energy, any of 14 elements with differing radiation outputs may be placed in the housing. The collimator on the same shaft as the housing may be used to focus the beam, with the same effect. Washers with different thicknesses of Mylar film fit into the collimator, and they absorb part of the radiation. To change the rays' flux intensity, both the pedestal under the IC's socket and the shaft to which the source housing is attached may be adjusted vertically.

Priced at approximately $3,000, the fixture must be hooked up to an IC tester that analyzes the data. Some semiconductor makers, including National Semiconductor, Texas Instruments, and Intel, have earlier versions in use.

Users react. "The fixture allows us to do experiments in a vacuum," says Earl Fuller, manager of reliability engineering for memories and microprocessors at National in Santa Clara. "Before . . . measurements were not very accurate. Overall, it makes our life much easier."

Similarly, G. R. Mohan Rao, design manager at TI's MOS Memory group in Houston, notes that the fixture's capabilities "were not conveniently available before, if at all. It's a brute-force instrument that's a little slower than we would like, but it provides us with the data we need. In terms of polar mapping data, we now have every possible angle. That was not available before."

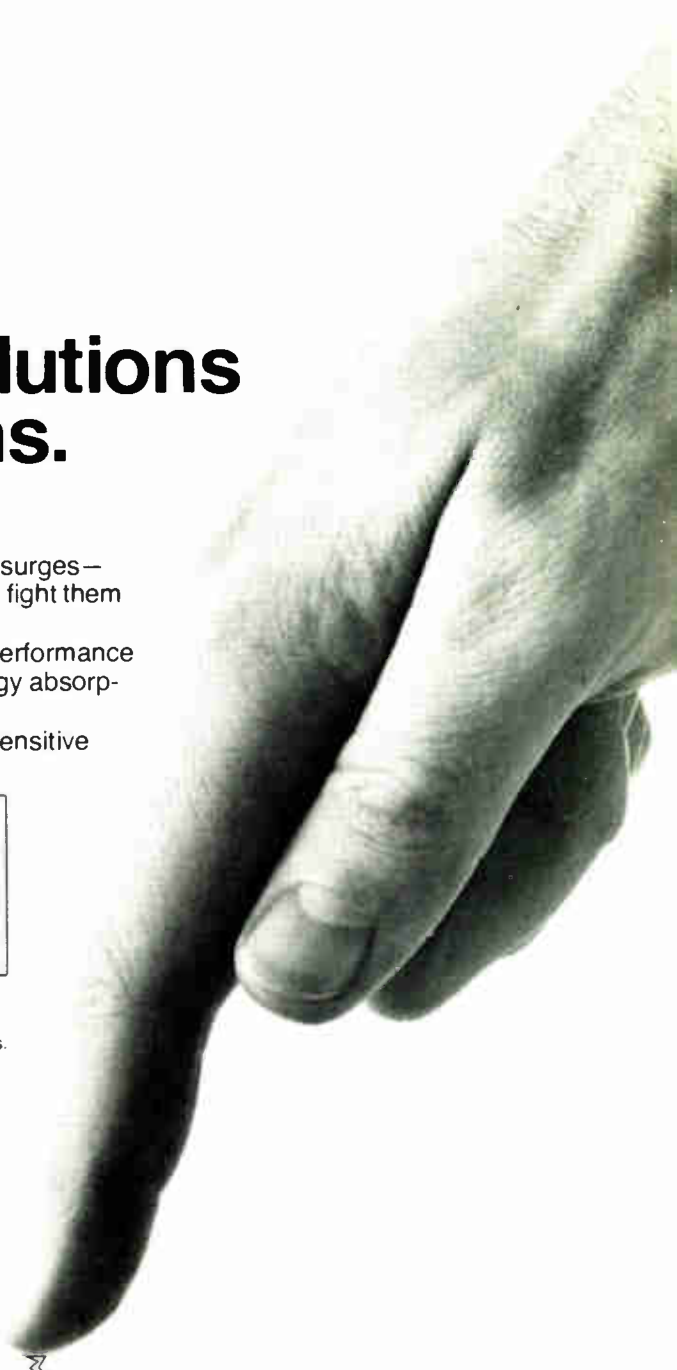
The test fixture is the latest in a series of custom developments for semiconductor manufacturers who became acquainted with Spectrum Sciences' background in nuclear physics. The first such development was for Intel Corp. in 1977, soon after engineers at the Santa Clara–based memory and microprocessor manufacturer realized that the charge used to determine bit state in dynamic RAMs could be upset and altered by alpha radiation coming in from trace elements, such as thorium and uranium, inherent in IC packaging materials. -Bruce LeBoss

Solid state

Honeywell shoots for system on a chip

Quietly building on its captive solid-state services, Honeywell Inc. is moving toward full integration of a universal computer system that can be adapted to its broad user base. "By 1986, we expect to have the entire electronics system integrated onto a single chip," says Carl Nomura, vice president and general manager of the Minneapolis company's

SIEMENS

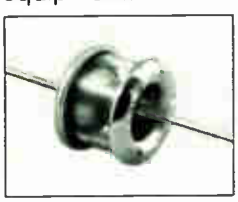


Three permanent solutions to transient problems.

Man-made voltage kickbacks or lightning-induced voltage surges—no one offers a broader range of transient protective devices to fight them off than Siemens.

Engineered to exceed REA and IEEE design criteria and performance specifications, Siemens transient protectors include both energy absorption and energy bypass (crowbar) devices.

Siemens offers three ways to protect both personnel and sensitive equipment:



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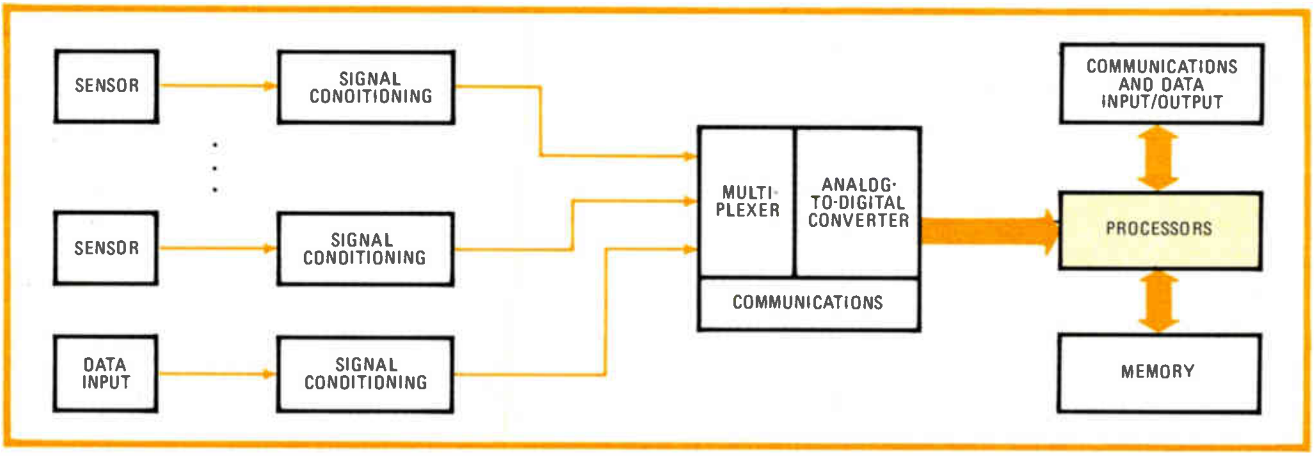

Universal. Adapting this system concept to various user needs, Honeywell Inc. is pushing its solid-state units—which include chip maker Synertek and optoelectronics leader Spectronics—to develop new technology for subsystems, in an ambitious IC effort.

Solid State Electronics Center.

More and more, large companies like Honeywell are scrambling for semiconductor expertise, since standard chips often fall short of their specialized needs. This shortfall is not expected to improve with very large-scale integration.

Honeywell's system concept (see figure) exemplifies its specialized requirements. Its goal is to meet the widely disparate needs of its users with various combinations of the subsystems. At the moment, the company is pushing integration at the subsystem level.

Already at the front end, its in-house semiconductor shops brought signal-conditioning circuits on chip for a variety of integrated sensors that use the Hall effect for magnetism and the piezoelectric effect for pressure and charge-coupled devices for visible and infrared imaging. It leads the way in growing and using mercury-cadmium-telluride crystals for night vision, reconnaissance, and thermal mapping.

Now in development are magnetic sensors that use Permalloy and moisture detectors based on zinc oxide thin films, says William T. Sackett, manager of the Corporate Technology Center. This year, Honeywell will use over 80 million of its sensors.

At the heart of its universal system are processors; for these it may tap its Synertek subsidiary. But significant processing elements have also emerged from the Phase 0 contract that Honeywell won from the Department of Defense's very high-speed IC program. For instance, it has devised a programmable fault-tolerant parallel-processing chip that will address a significant portion of the triservice needs, according to Robert J. Witham, VHSIC program manager in Honeywell's Aerospace and Defense group.

Honeywell directs its IC effort toward the requirements of its two major divisions for original-equipment manufacturers, Control Systems and Information Systems, which serve the industrial process-control and commercial data-processing fields, respectively. "Every element of these is tied to semiconductor technology," says James R. Berrett, Honeywell's corporate vice president of development.

The $4.2 billion company has the 15-year-old Solid State Electronics Center for in-house IC fabrication and the 3-year-old Corporate Technology Center for long-term plan-

TI's floppy-disk controller to bow soon

There is another contender in the IBM-compatible floppy-disk controller arena: the 9909 from Texas Instruments Inc. Though announced over a year ago, the Dallas firm's unit still ranks as one of the most advanced devices to date, allowing a floppy-disk subsystem to be implemented with very little additional circuitry.

Western Digital Corp.'s FD1771 has probably been the most popular floppy-disk controller chip available, but a boardful of additional small-scale integrated-circuit packages are needed to work with it. Even since that company's introduction of the enhanced FD1791 in 1978, several other companies have announced floppy-disk controllers that integrated more and more of that external circuitry on chip.

The controllers have undergone a painful birth, mainly because manufacturers have had difficulty in specifying which functions should be handled in hardware and which should be software-programmable. For example, Standard Microsystems Corp. has a special version of its part designed to handle hard-sectored disks, whereas with Motorola and TI that is a programmable option. Moreover, write precompensation—required by many double-density drives—is a programmable option on TI's and Rockwell's but requires external circuitry on some of the others.

Significantly absent on the 9909 is the circuitry to separate the clock pulses from the data bits on read cycles; only the SMC part includes this function, however. The +5-volt-only 9909 is actually a high-speed microcomputer (much like the company's one-chip device) that adds firmware to perform the functions of a floppy-disk controller. The 6-megahertz part handles up to four 8- or 5.25-in. floppy disks. **-R. Colin Johnson**

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ning and basic research. To these, it added two 1968 purchases: Synertek, the Santa Clara, Calif., maker of MOS chips, and Spectronics Inc., a Richardson, Texas, leader in optoelectronics.

Synertek is now an alternative source for the 6500 and Z8 processor families, and it plans a 16-bit machine and what it dubs a Super CPU (Honeywell will say no more than that). Now completing a facility in Santa Cruz, Calif., Synertek also promises a 64-K erasable programmable read-only memory, a 16-K static random-access memory, a 128-K ROM, and an electrically erasable ROM. These products will be available for sale, for Synertek's principal charter is to make money for Honeywell, says Michael Smolin, the unit's strategic marketing manager for microprocessors.

At the back end of its system, Honeywell has come up with new techniques to display information. One of these is a camera that produces real-time holograms with a reusable thermoplastic film. The holograms are viewable on a TV.

Coming is a facility with an electron-beam system for mask making and one for direct-write lithography. Already, V-groove isolation and dry etching have pushed its Schottky bipolar technology to 500 megahertz. For even higher speeds, it says, it will move gallium arsenide technology to medium-scale production within three years.-**John G. Posa**

Business systems

VW, IBM disclose more of their plans

Volkswagen and office automation are not often popularly linked, but the West Germany–based auto maker is moving to become a major element in the office-of-the-future market. A sign of its determination may be seen in the aggressively priced printer for word-processing and small-business systems that its Los Angeles subsidiary, Pertec Computer Corp., has just introduced. Cost-

News briefs

SIA sees recession affecting shipments into 1981

Sales by U. S. semiconductor manufacturers will grow this year, to $8.5 billion from shipments of $6.6 billion in 1979, reports the Semiconductor Industry Association. The current recession will slow industry growth in the second half of this year, and overall growth in 1981 will slow to 14%, or $9.7 billion, the SIA says. Integrated circuits are predicted to grow 38% this year to $6.4 billion, with memory devices the fastest growing sector in both bipolar (up 63%) and MOS (up 45%). Discrete devices will show a growth of 7% to $2.1 billion, with optoelectronics the leading growth product line at 19%, according to the forecasts.

Japan's KDD tries link of high- and low-speed data nets

High-speed data transmission is all very well, but compatibility with existing lower-rate systems can be a sticky point. To show it need not be, Japan's Kokusai Denshin Denwa Ltd. hooked up a prototype of a high-speed facsimile machine to its Venus international packet-switching system and successfully sent test faxes to the low-speed data service offered by RCA Global Communications in New York. For telecommunications users, the experiment shows that high-speed packet switching can be interfaced with a widely used, low-speed data-transmission service with extensive distribution capabilities. Through such services as RCA Globcom, a hookup could provide direct delivery of information or easy connection to other packet networks. One of the tricks that made the KDD link possible was the data compression in the prototype fax, where the 4 megabits of information on an 8½-by-11-inch document were reduced by nearly 95%.

Exxon Enterprises, Intersil mount reorganization efforts

Reorganization is the order of the day at both Exxon Enterprises Inc., the high-technology arm of the oil giant, and Intersil Inc., the Cupertino, Calif., semiconductor company noted for linear integrated circuits.

Exxon is looking to strengthen its thrust into the word-processing market by forming Exxon Office Systems Co. from three heretofore separate operating companies: Qwip, which makes telephone facsimile machines; Qyx, which makes electronic typewriters; and Vydec, which makes word processors. The move comes on top of the recent establishment of an Exxon communications group comprising Delphi Communications, which makes voice-transmission units; Periphonics Corp., which makes computer audio systems; Verbex Inc., which makes voice-recognition equipment; and Intercom Inc., which makes private branch exchanges.

Intersil's reorganization affects the Semiconductor division, which was structured along product lines in analog and digital groups. The new focus is on three teams led by Richard H. Forte, Terry Martin, and Dave Fullagar, who are responsible for operations management, process technology, and development engineering, respectively.

CSC denies charges in Federal computer services indictment

Computer Sciences Corp. maintains it is innocent of criminal charges of fraud, conspiracy, and racketeering made in a 57-count Federal indictment returned earlier this month by an Alexandria, Va., grand jury against the timesharing services company and six of its present and former officers. The indictment is the first against a nationally known supplier of technology in a continuing investigation of contracting by the General Services Administration, which has procurement responsibility for all Federal agencies for everything from computers and telecommunications services to office furniture. The indictment alleges CSC bribed a GSA contracting officer in 1972 to obtain information permitting the company to win a $100 million Government teleprocessing services contract that expired in 1977. A spokesman for CSC, which has its headquarters in El Segundo, Calif., said the company "intends to defend itself vigorously" against the charges, for which it believes "there isn't any basis."

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Semiconductors speak.

"By digitizing and compressing speech patterns the way the ear hears them, rather than the way the throat forms them, the DIGITALKER™ speech synthesizer sounds totally natural and lifelike."

One of the most exciting developments in the industry is now in production at National: semiconductors that speak.

Although the technology of digital speech synthesis is not new, it has only now become available at a low cost and with a minimal number of ICs.

In fact, techniques are now refined enough to store a large library of directly addressable words or phrases on a single ROM. Add to this a sophisticated new IC that translates and plays back these words and you've just assembled a DIGITALKER speech synthesis chip set.

However, just the availability of digital speech is not enough. Semiconductors should also speak with the same fluent quality and natural sound of a human voice. Any human voice.

This is where National's unique approach to speech synthesis totally outshines any other technique currently being explored within the industry.

Simply stated, our approach is to process and store only those speech elements that the human ear actually hears, which is significantly different from what the vocal tract actually generates.

A superior architecture. In its simplest form, DIGITALKER consists of an independent Speech Processor Chip (SPC) and one or more standard 16K, 32K or 64K ROMs.

We store speech wave patterns in the ROM that are compressed in the time domain. This eliminates a great deal of the number-crunching required by other techniques in order to reconstruct the digitized words.

In the end, you get a simpler, more straightforward SPC design that operates at slower clock frequencies relative to other techniques.

The SPC also contains an internally programmable frequency generator and a variable gain D/A converter. Together they produce the intonation and inflection that make DIGITALKER sound so incredibly realistic.

The result is that DIGITALKER can reproduce any original voice in any spoken language – male or female, adult or child – both clearly and economically.

So for the first time, you can design in electronic speech with as few as two chips. And you don't have to sacrifice any of the natural inflection, intonation and expression of the original voice.

Cutting ROM down to size. The techniques we use to process any selected speech waveform can be broken down into two basic categories: digitization and compression.

Each speech waveform to be digitized is sampled in the time domain. The sampling rate for each waveform is at least twice the highest frequency in the pattern (called the Nyquist rate).

The digitized waveform then undergoes the first of four compression schemes developed by Dr. Forrest S. Mozer. These techniques and algorithms minimize DIGITALKER's ROM storage requirements.

The first of these steps removes all redundant pitch periods and portions of certain other pitch periods. Redundant phonemes and portions of phonemes are also removed at this time. (Phonemes can be loosely defined as basic word sounds.)

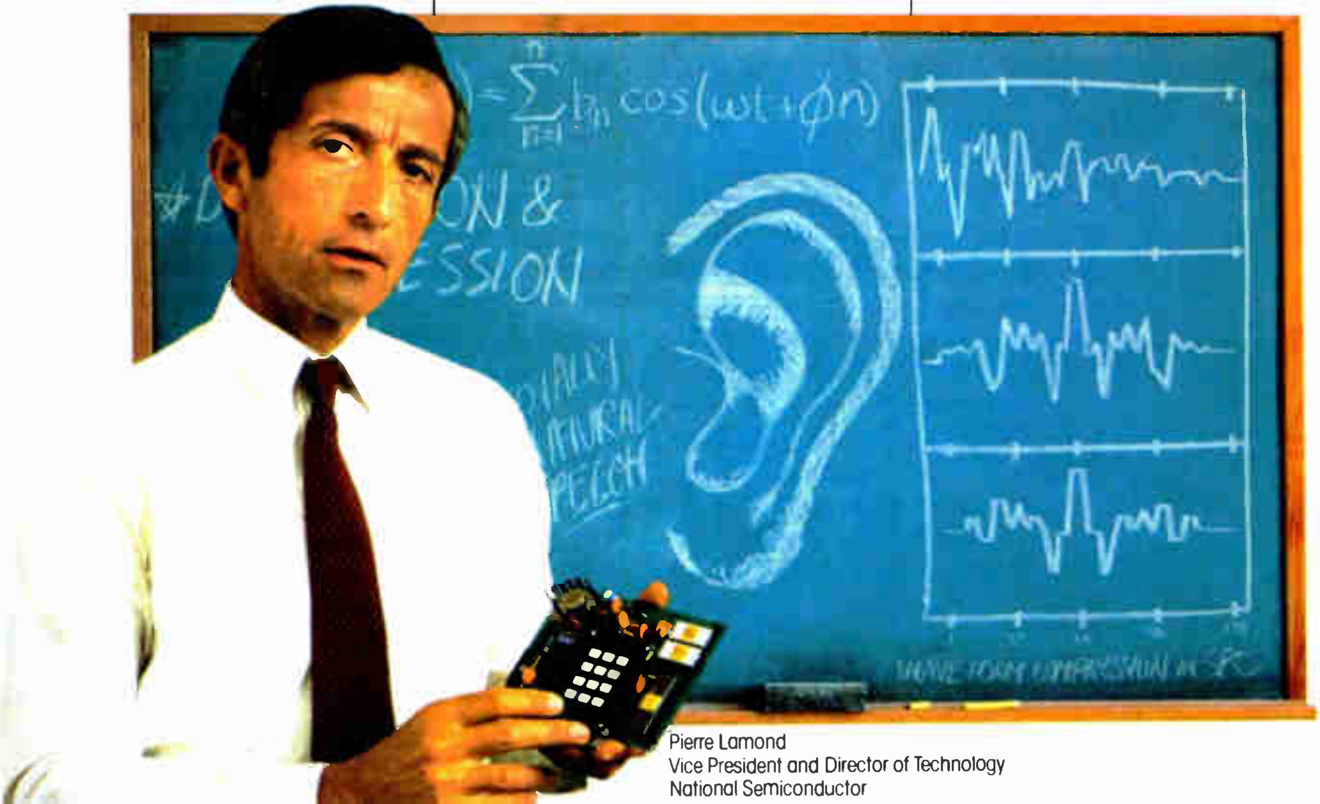
The second compression technique, called Adaptive Delta Modulation, allows us to even further minimize ROM overhead. This simply involves storing the arithmetic difference between successive wave amplitudes (which is relatively small) rather than the amplitude values themselves.

The third major compression technique removes the direction component of a speech waveform through a process called Phase Angle Adjustment. Since the ear naturally ignores this component, its removal in no way affects DIGITALKER's vocal quality.

As a final compression scheme, the low amplitude portion of a waveform is reduced to silence. This typically results in an additional 50% reduction in the amount of ROM required to store the message.

The net effect of these four data compression techniques is DIGITALKER's ability to store, reconstruct and playback high quality spoken messages in a minimal amount of ROM.

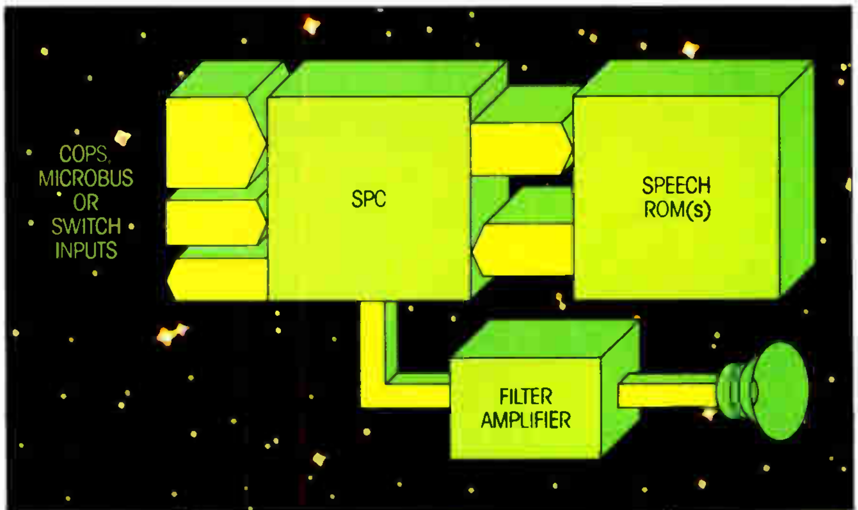
So listen to DIGITALKER. The technology speaks for itself.



Pierre Lamond
Vice President and Director of Technology
National Semiconductor

DIGITALKER™– practical in every sense of the word.

For the first time, very natural-sounding speech capability can be designed in with as few as two chips.



The Practical Wizards have come through with a versatile yet affordable application of an exciting technology.

Their new DIGITALKER speech synthesis chip set brings truly life-like speech capability to a virtually unlimited array of products.

DIGITALKER's design versatility stems from its straightforward architecture. An independent Speech Processor Chip (SPC) translates digitized and compressed expressions stored in one or more standard ROMs (16K, 32K and/or 64K, depending on the size of the vocabulary).

The SPC can directly address up to 256 expressions and 128K of ROM. Larger vocabularies may be obtained simply by cascading additional ROM.

Simplicity of application. Now, the ability to produce eloquent speech can be easily and inexpensively designed into a product using as few as two chips (for simple switch-driven devices). For more sophisticated applications, the SPC is both COPS™ Family compatible and MICROBUS™ compatible.

This is where DIGITALKER's true practicality really comes through. It functions equally well as either a stand-alone module or as a simple peripheral on a μP or microcontroller bus.

In fact, all it needs to begin speaking is a one-byte starting address and a "start" strobe. When the message is complete, it generates an interrupt.

The specially encoded customized vocabularies stored in ROM are based on tape recorded messages submitted by the customer. National processes these messages and loads them into the necessary amount of ROM.

So when it comes right down to it, the most difficult aspect of designing in DIGITALKER is deciding on what it should say. Or who it should sound like.

Have it speaking in 15 minutes. DIGITALKER is available for evaluative purposes in two forms.

The DT1000 (priced at \$495*) is a totally self-contained board that – with just a speaker and a power supply – can rattle off any desired combination of 144 words.

For those who would rather build DIGITALKER into their own evaluation designs, the Practical Wizards are also offering the DT1050 chip set (priced at \$85*). The DT1050 consists of a 40-pin Speech Processor Chip and the same 144-word ROM library that comes with the DT1000.

Both the DT1000 and the DT1050 evaluation kits are available today at the locations shown on the back page of the National Anthem.

*U.S. prices only

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The voice of things to come.

With small, low-cost speech synthesis units now easily available, is there really any limit to the number of everyday products that can and will talk?

With the advent of economical speech synthesis technology – as spearheaded by DIGITALKER – we've suddenly gone beyond the realm of simple indicators.

Because as the new technology finds its way into more and more applications, a wave of change will take place in the consumers' general attitude toward electronic products. Before long, people will not only enjoy, but will actually expect a verbal response from just about everything from clocks and computers to dashboards and gas pumps.

Questions that cannot be ignored. Since the speech produced by DIGITALKER has incredibly life-like qualities, any product that uses it immediately takes on a distinct personality. Even that of a celebrity or a familiar company spokesman.

Toys, for example, can communicate with playful children's voices in any language. A TV set might take on parental authority. An automated bank teller can be bright and cheerful. An alarm or warning signal can sound a stern but calm explanation of a problem.

The quest for the optimum product personality will undoubtedly spur a myriad of market surveys and analyses to answer such questions as: What should our product say? What should it sound like? Who should it sound like? What other products or enhancements can make good use of speech technology?

Answers to these and related questions are already becoming vital in terms of getting the most out of current and future products of all kinds.

Unparalleled cost/performance. The cost/performance benefits of designing DIGITALKER into a product application are truly substantial.

R & D costs are minimized because all of the complex speech data processing is done by National. So the engineer doesn't need to know anything about the detailed techniques of speech synthesis in order to properly design it in.

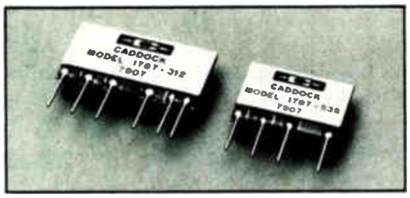
Also, if a custom vocabulary is desired, National loads the processed speech data onto the optimum combination of 16K, 32K or 64K ROMs. In this way, hardware costs are kept in line with the size of the vocabulary.

And finally, DIGITALKER's overall design versatility virtually eliminates the need for external ICs in its simplest application (except an optional filter and an amp). It can either stand alone or act as just another peripheral on a μP bus. So R & D time is cut to the bare bone.

Thanks to DIGITALKER, "speech synthesis" will soon become a household word.

Current sensing resistors for multi-range instruments.

NEW



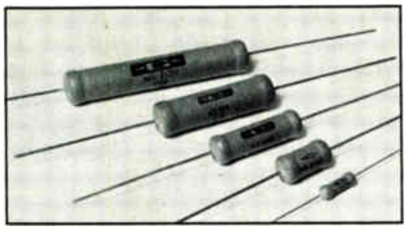
Caddock's Type 1787 Current Shunt Resistor Networks.

Absolute resistance tolerances of 0.25%, 0.1%, 0.05% and 0.02% make these 2-, 3- and 4-decade current shunt resistor networks the ideal replacement for expensive, bulky discrete resistors.

16 standard models are now available. The basic network design provides a series total resistance of 1000Ω, 100Ω, 10Ω and 1Ω. Other standard models provide commonly used variations of this basic design.

For Type 1787 data, circle Number 201.

Non-inductive precision resistors for power switching circuits.



Caddock's Type MS Power Film Resistors.

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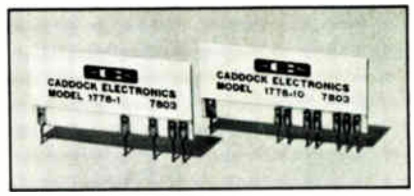

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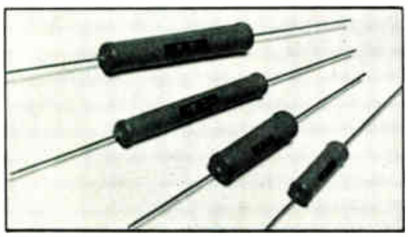

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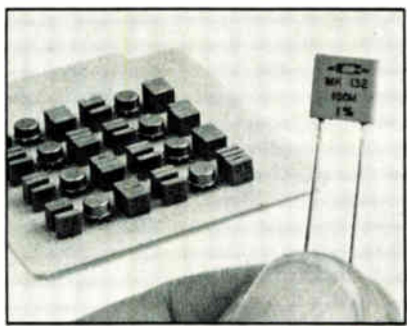

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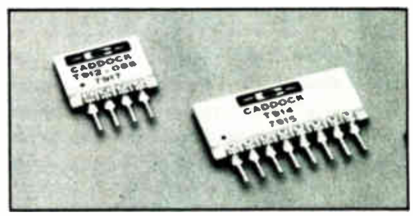

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Circle 207 on reader service card

Trade show opens China's door

For some 45 electronics companies the China trade has already begun. These were the firms that showed their wares at the recent Electronics/China 80 exhibition held at the Canton Trade center in the People's Republic of China. More than 40,000 Chinese came from every province except Tibet to crowd the 10-day-long show, according to Clapp & Poliak Inc., the show's New York–based organizer. Exhibitors not only sold all the products made available at the end of the show, but they lined up potential sales worth $15 million in China within the next 12 months. The joint sponsors, China Council for the Promotion of International Trade and the U. S.-China Trade Consultants, are already planning a follow-up exhibit in the fall of 1981.

"A large part of the success was because it was the first truly national electronics show in China," says Ned Krause, exhibition director for Clapp & Poliak. "Based on registrations for the seminars held during the show, about 40% of attendees came from outside the Canton province." And the Chinese sponsor (CCPIT) was responsible for ensuring that all attendees were actually involved in electronics. They ranged all the way from plant supervisors to the heads of large government agencies.

Exhibitors included Analog Devices, Apple Computer, Burr-Brown Research, Cal-Comp, EG&G Instruments, Fairchild Test Systems Group, Kulicke & Soffa Industries, and National Semiconductor. Krause estimates that over 80 U. S. companies will sign up for the return engagement next year. The cost of participating could range to $50,000 depending on the number of booth spaces rented, the number of people manning booths, travel expenses, and the type of products displayed. **-Gerald M. Walker**

ing $820 in volume, the daisy-wheel Stylist 360 bowed at the Info 80 information-management show in New York earlier this month.

The show also was the site of a bit of curtain-lifting by International Business Machines Corp. of its local network concept, which will be used to link office machines within the same building or site.

Pertec's pricing of the Stylist 360 sets a new price-performance standard for letter-quality printing in small systems. The printer will cost as little as half the price of competitive units.

The lower price stems largely from anticipated economies of large-scale marketing. The company is using the mechanism of an electronic typewriter made in West Germany by another Volkswagen AG subsidiary: Triumphwerke AG, and of course it expects the low price to expand the daisy-wheel market.

Nuremberg-based Triumphwerke is VW's vehicle for driving into the office automation market. Its U.S. holding company owns Royal Business Machines, an old-line typewriter manufacturer, now selling office automation equipment, and half of Omnidata Inc., the Westlake Village, Calif., computer company. All this activity last year added up to $1 billion in worldwide sales of computers and peripherals out of VW's total worldwide sales of $17 billion.

As for IBM, even as it thinks ahead on linking local networks (p. 42), it is revving up its efforts to produce its own local net concept, which it is calling the enterprise systems, to connect its word-processing, office systems, and data-processing offerings. "IBM is in the office-of-the-future business to stay, and our concept of enterprise systems is an important framework of our solution," said Allen J. Krowe, president of the System Communications division, in the keynote address at Info 80.

The firm has already revealed that it plans to offer software to link via communications the machines produced by its various divisions [*Electronics*, July 3, p. 95]. Enterprise systems will use many of the concepts found in IBM's Systems Network Architecture, used for computer-terminal communications for teleprocessing and distributed-processing applications. **-Tom Manuel**

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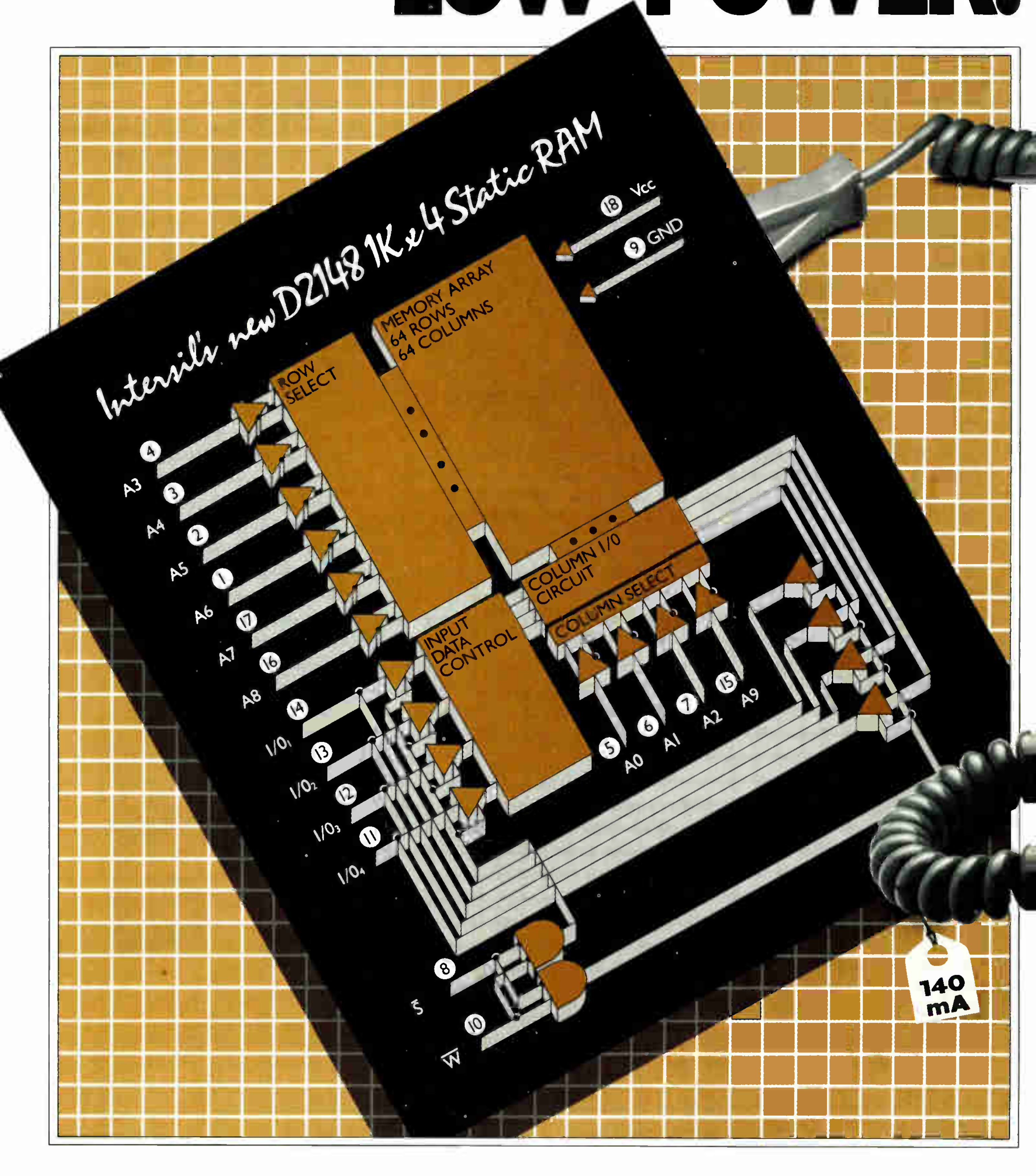

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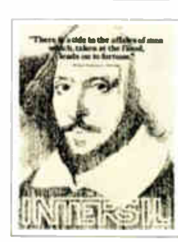

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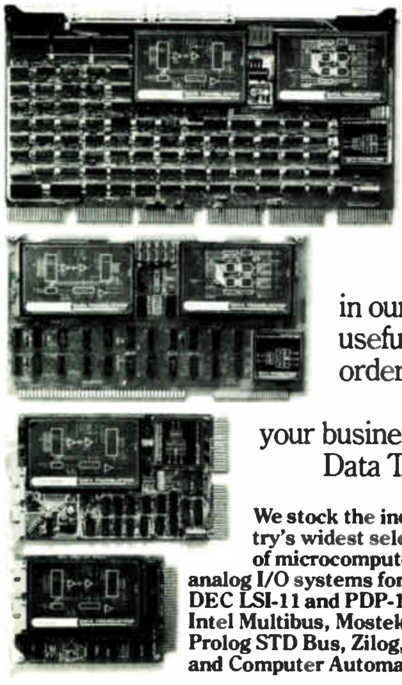

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Circle 56 on reader service card

Washington newsletter

FCC wants to open world voice, data businesses to all . . .

With five U. S. international record carriers—those that carry data rather than voice—showing both stability and strong profits, the Federal Communications Commission is considering **letting American Telephone & Telegraph Co. compete in that market and, at the same time, letting the carriers compete for AT&T's international voice traffic.** With total revenues of the international record carriers up from $89.9 million in 1964 to $397.8 million in 1978 and plant investment up from about $200 million to nearly $700 million in the same period, the FCC staff believes the earlier ruling splitting the international voice and data business, designed to protect the then-fledgling record carriers, may no longer be needed. Commissioner Joseph R. Fogarty notes that the trend toward all-digital international telecommunications—now under study by the International Consultative Committee on Telephony and Telegraphy (CCITT)—could make the issue moot. "If we go entirely digital internationally," Fogarty indicates, "it may eliminate the voice-record [services] dichotomy."

. . . as it starts international carrier profit study

The FCC also has started an examination of international record carriers' rates of return to determine if profits are too high. The formal review now being prepared by the FCC staff **will concentrate on ITT World Communications,** the largest such carrier and a subsidiary of International Telephone & Telegraph Co. The other carriers include: Western Union International, RCA Global Communications, TRT Telecommunications, and FTC Communications. Comments during the meeting of the FCC commissioners with staff members of the Common Carrier Bureau indicate that marketplace competition may itself produce a reduction in international tariffs before the new investigation can be completed.

U. S. telecomm show in China set for 1981

The Peoples' Republic of China will get its first telecommunications equipment show and seminar next year under the joint sponsorship of the Electronic Industries Association's Communications division and the National Council for U. S.–China trade. The program, scheduled for Nov. 3–13, 1981, in the Beijing Exhibit Center in the capital, is expected by Chinese estimates to draw up to 100,000 qualified registrants. Among the exhibits at the show, to be called China Comm '81, will be wire-line transmission, exchange, and station systems; satellites, microwave, broadcast, and mobile radio technologies; and switching and analog and digital terminal equipment, including data processors. **The U. S. "is playing catch-up in China," says the EIA of that potentially large market,** since other nations have already made presentations there.

Justice readies antitrust guidelines for joint research

The Justice Department says it will publish in November an antitrust guide concerning joint research ventures that will "clarify our enforcement policy and explain, in simple language, the Antitrust division's approach to analyzing the legality" of such efforts, according to Ky P. Ewing Jr., deputy assistant attorney general for antitrust. Noting that the department has challenged only three such ventures in the last two decades—on the grounds that the ventures "retarded innovation" by imposing "significant collateral restraints" on participants—Ewing told a mid-October industrial innovation meeting of the National Association of Manufacturers that **"if the project, in the long run, promotes innovations, then it will probably pass muster under the antitrust laws."**

AT&T's reorganization: decontrolled or uncontrolled?

As Jimmy, John, and Ronnie race about the nation exchanging barbs before Election Day, relatively little attention is being paid by the press to American Telephone & Telegraph Co.'s senior executives as they lay out their new competitive telecommunications strategies. That is regrettable, if only because, unlike the presidential candidates, AT&T is detailing its plans for the future with precision.

But many legal and legislative details surrounding the issue of competition in the rapidly expanding telecommunications industry—or "information industry," as AT&T president William M. Ellinghaus now calls it—remain unresolved. Congress adjourned without acting on H. R. 6121 or its Senate counterpart, and the Federal Communications Commission, the Justice Department, and the White House remain divided on whether or not AT&T can offer anything more than basic telecommunications services under the 1956 consent decree, whereby the company agreed to limit itself to these areas in settling a Federal antitrust suit.

The FCC judgment in its Second Computer Inquiry ruling earlier this year (Docket 20828) says AT&T can compete with "enhanced" services through a fully separated subsidiary. The White House agrees. The Justice Department's Antitrust division is opposed, contending that actions by either the FCC or the Congress cannot be used to set aside court rulings. Congress is split on the issue—a split that produced adjournment without legislative action.

Leaving legislation behind

Confronted with this standoff, AT&T's Ellinghaus says, "We're not going to wait." The Bell System is moving ahead to meet oncoming competition in the information industry with its own reorganization plan [*Electronics*, Aug. 28, p. 59]. As for any future rulings by the FCC, Congress, or the courts, "we'll adjust our actions later if necessary," the AT&T president told competitors at the annual meeting of the North American Telephone Association earlier this month in Florida. "The Bell System has decided that there is no part of that industry in which we intend to come in second."

At the same time, AT&T chairman Charles L. Brown spelled out for Bell System employees how the telecommunications giant intends to compete through its fully separated subsidiary "in a highly competitive retail marketplace." The regulated activities "will remain vertically integrated" and operate "as a profit center," according to Brown. The new, separated subsidiary "will be responsible for the design, development, manufacture, sales, and service of all customer premise equipment and some newly developed services."

What distresses many competitors is Brown's observation that the new subsidiary "might also become vertically integrated" and his determination that "we must employ our unrivaled assets in a manner that brings us through a hazardous period with undiminished strength."

The split within Government

Though Brown, Ellinghaus, and other AT&T leaders profess that new legislation is still needed to deregulate the information industry that now encompasses telecommunications, some competitors dispute that view. "As long as legislation is stalled," one argues, "AT&T can reorganize exactly the way it wants. Then it will have even greater leverage—political and economic—than it has now. Once AT&T restructures along its own lines, the issue of legislation could become moot."

On the other side are competitors like the one who says, "We can live with AT&T as the dominant market force provided it puts more of its procurement up for industry bids, as it seems to be doing, and as long as the customer terminal market is left completely open to competition." IBM's domination of the computer market, he argues, "does not seem to have stunted the growth of the data-processing industry in this country; AT&T could provide the same leadership in information and telecommunications. More than that, it could help the country maintain its lead against Europe and Japan."

Most world trade specialists in the Departments of Commerce and State may privately hold with the latter view, but the Justice Department clearly does not. Its antitrust suit against AT&T is scheduled for trial next year. And several industry groups—notably the Computer and Communications Industry Association—agree with the department's contention that the FCC cannot change a court order and let AT&T compete in unregulated markets and are challenging the FCC in court.

Final resolution of these critical issues should come from Congress, not the courts, but it is still not clear whether the 97th Congress will pick up the ball again when it convenes in January. And there are serious questions about whether AT&T, despite its public statement, truly wants legislation. At the moment, Ma Bell seems satisified to fill the legislative and regulatory vacuum in its own way. **-Ray Connolly**

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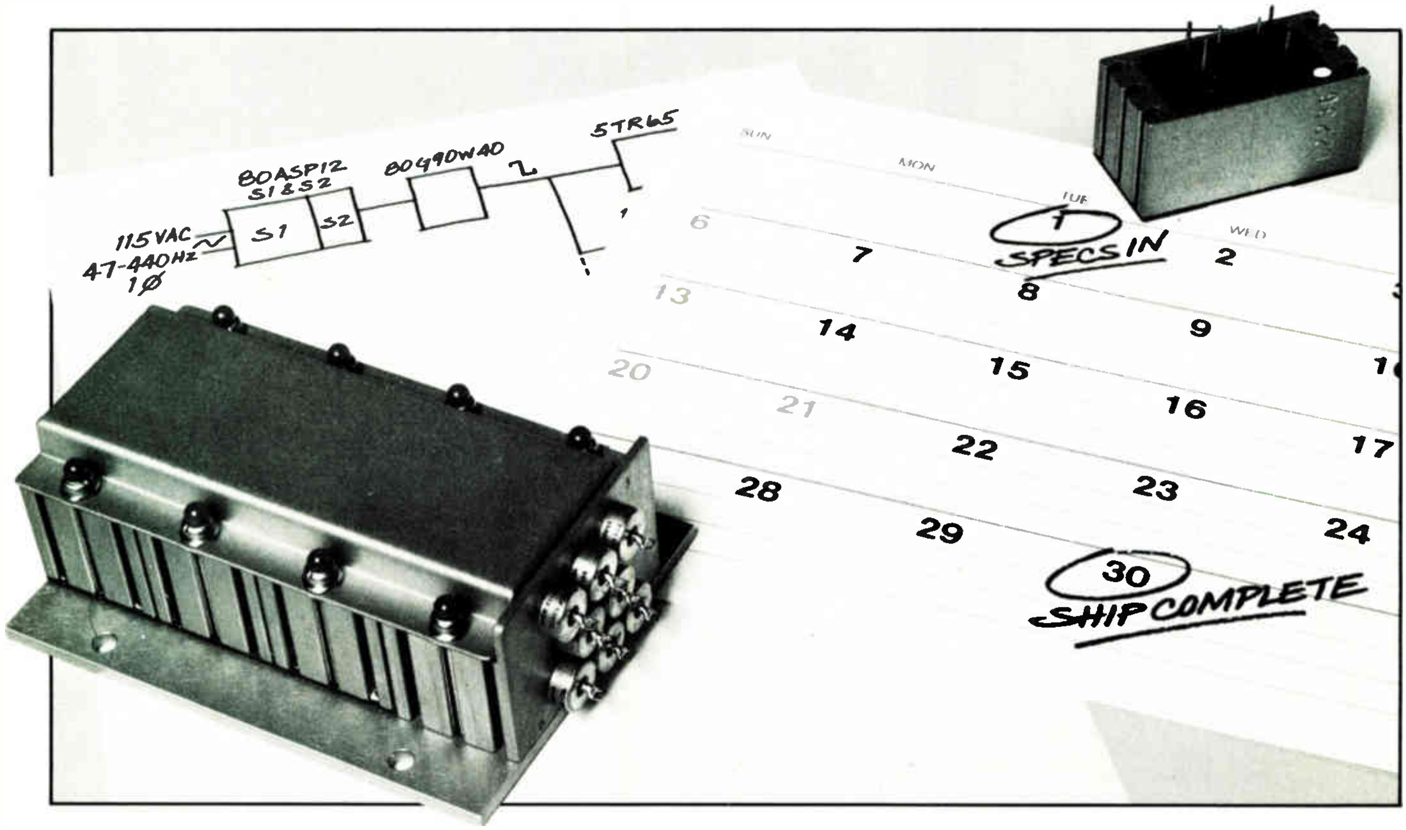

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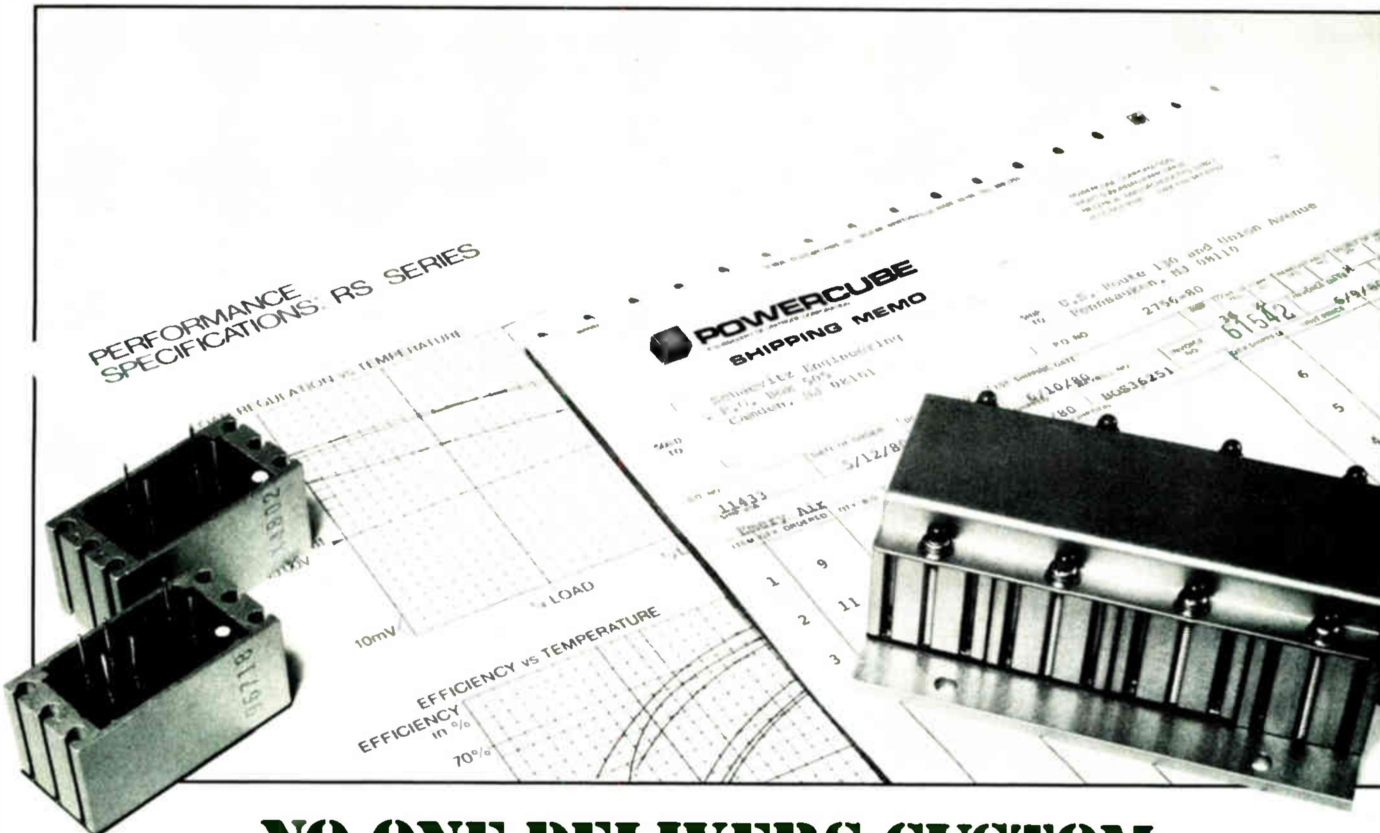

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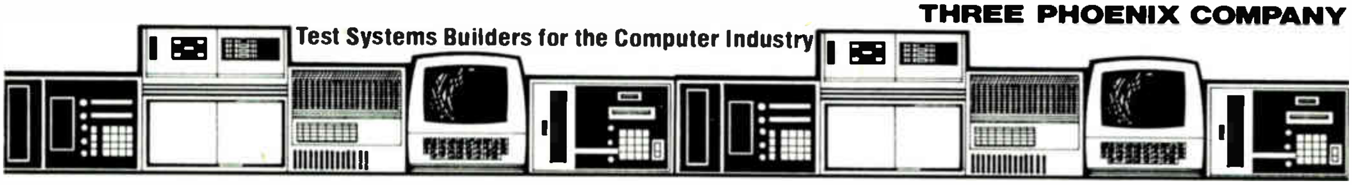

Microcassette gear for consumer stereo makes its bow . . .

Microcassette magnetic tape, the latest medium for consumer stereo, sounds amazingly good for a medium originally developed for speech only [*Electronics*, Oct. 28, 1976, p. 54]. At the 29th All Japan Audio Fair, Sanyo Electric Co. showed **a full-fledged microcassette stereo deck for $385 and a microcassette stereo player for use with headphones for $192,** while Aiwa Co. showed a stereo radio-microcassette recorder with two speakers for $206. In addition, Aiwa, Matsushita Electric Industrial Co., and microcassette pioneer Olympus Optical Co. showed prototype decks, and still others will probably hurry products to market once tape manufacturers start selling prerecorded tapes.

The microcassettes provide 30 minutes of music in each direction for most manufacturers' tapes but 45 minutes in each direction with Matsushita's metal tapes. Sanyo claims a frequency response for its deck of 150 to 14,000 Hz at 20 dB down when using metal tape; Aiwa claims a range of 150 Hz to 8,000 Hz.

. . . along with Sony-Philips audio disk at Japanese fair

Sony Corp. and NV Philips Gloeilampenfabrieken of the Netherlands have demonstrated at the Japan audio fair the latest version of what they call their compact disk digital audio system, which likely will be chosen as a worldwide standard. Philips says that a liberal licensing agreement to obtain industrywide participation would benefit all parties. Moreover, Polygram and CBS/Sony are ready to begin turning out disks.

The one-hour-on-a-side disks are only 12 cm in diameter and readily slip into a man's suit pocket. The linear velocity of the track past the near-infrared laser that plays back the recorded information is a constant 1.25 meters per second for maximum information density. Track pitch is 1.6 μm. The music is recorded at a 44.1-kHz rate and with 16-bit linear quantization to provide **a frequency response to 20,000 Hz and a dynamic range, signal-to-noise ratio, and channel separation of better than 90 dB each.**

Mobile phone system from SEL aims at military uses

West Germany's Standard Elektrik Lorenz AG, a Stuttgart-based ITT affiliate, has unveiled at the Oct. 7–9 Military Electronics Defense Exposition in Wiesbaden, West Germany, a mobile microcomputer-controlled telephone exchange system equipped with electronic components only and laid out to withstand the rough mechanical and climatic conditions encountered in military applications. In its basic configuration, the MMX 2/9 system accommodates two long-distance lines and 9 participants but is expandable to handle four or six such lines with 18 or 27 participants. It has **a semiconductor-based space-switching matrix, as well as an integrated tester that continuously monitors all functions and indicates any defective circuits.** The microcomputer, a Motorola 6802, performs all exchange and test processes. The basic system comes in a 608-by-200-by-284-mm (24-by-8-by-11¼-in.) case and weighs about 25 kg (55 lb).

British company to cash in on modular software

Though modular software is one way of containing escalating program costs, few modular application packages are available today. An exception is Trade-Winner, an integrated business system for sales and distribution developed by EMS Consultants Ltd., a small British software house based in Newcastle-under-Lyme. The company has invested four years and $1 million (partly funded by London financiers Montagu, Loebl, Stanley &

Co.) **developing a suite of 500 modules—on average, between 4-K and 8-K bytes—from which an integrated business system can be assembled to a customer's requirements.** Now the company hopes to franchise its software. The first version of Trade-Winner was written in Cobol for Honeywell's level 6 minicomputer and now a second version is being written for ICL's new ME-29 minicomputer. EMS is negotiating funding for this project from Britain's National Computer Centre. U. S. marketing rights are being negotiated with Honeywell and one U. S. software house.

Family of 8-bit microcomputers has all-European design

Watch for the Electronic Components and Materials (Elcoma) division of the Netherlands' NV Philips Gloeilampenfabrieken to announce what is the first family of microcomputers of truly European design. Developed at Elcoma's affiliate, Valvo in Hamburg, West Germany, and to be unveiled at the Nov. 6–12 Electronica components exhibition in Munich, the 8400 is a five-member family of 8-bit, single-chip n-MOS microcomputers whose special feature is **the implementation of serial inputs and outputs on the chip**—a feature that will allow loosely coupled network applications. The serial I/O has a multitransmitter capability that facilitates communication between the microcomputer and peripheral circuits or other microcomputers. The first devices of the 8400 family will be available next year.

Deep-ultraviolet photoresist optimizes optical projection

A new photoresist, a mixture of a phenol resin and a photosensitive azide compound, promises to make it possible to fabricate very large-scale integrated circuits with conventional photolithographic equipment. Hitachi Ltd.'s Central Research Laboratory says that it has developed a deep-ultraviolet-light negative photoresist with which 1-μm lines can be defined by exposure through 1:1 projection optics. The process is controllable and the walls at the edges of the pattern can be vertical or undercut as desired. The resist is highly resistant to damage during dry etching and also has the excellent stability of previously used negative resists that cannot provide the same fine pattern characteristics. Moreover, actual tests at Hitachi show that **30 seconds' exposure in a 1:1 projection system is sufficient for a 4-in. wafer.** The resist is eventually to be marketed.

TI France wants a role in new French IC plan

Texas Instruments France of Nice is making a bid for participation in the enlarged version of the French government's $180 million integrated circuits plan (see p. 100). Charles Clough, vice president and general manager for TI's European Semiconductor group, suggests that **it could second-source circuits developed by the five original participants in the plan and thereby improve those circuits' marketing possibilities.**

Addenda

Japan's Toko Inc. has agreed in principle to transfer to Motorola Inc. half its shares in MOS integrated-circuit maker Aizu-Toko Inc., which till now it wholly owned. **Aizu-Toko will be run as a joint venture.** . . . The lion's share in a combined Danish order for digital telephone exchange equipment, **to serve about 270,000 subscribers and worth initially about $100 million,** will go to Sweden's L M Ericsson and a smaller share to Kirk, the Danish subsidiary of West Germany's Standard Elektrik Lorenz AG. The Danish post and telecommunications authority, the Jutland Telephone Co., and the Funen Telephone Co. are responsible for the order.

One of these creatures is extinct...

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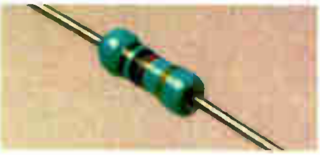

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With 20 years experience in RF instrumentation, we're driving down the cost of high performance.

The 6070A and 6071A are designed to fill a critical gap in today's signal generator market: the price/performance gap that separates $10,000 synthesizers with limited capabilities from the more sophisticated, state-of-the-art units costing $25,000 and up. As such, they represent a new generation of RF synthesizers from Fluke that deliver the industry's most-wanted features at a very affordable price.

Innovative design achieves signal purity and broad frequency coverage.

Fluke engineers developed a number of unique and cost-effective synthesis techniques for the 6070A and 6071A that deliver a high degree of spectral purity without sacrificing broadband range.

The frequency range of the 6070A is 200 kHz to 520 MHz and the 6071A extends the range to 1040 MHz. Yet both instruments have spurious output levels of 90 to 100 dB below carrier, performance equalling or exceeding the best cavity-tuned generators on the market today. Microprocessor control – which Fluke introduced to signal generator design in 1975 with the 6010A – allows precision resolution and settability you can't find from any other manufacturer.

Fluke's new approach to synthesis in the 6070A and 6071A combines several unique elements: a refined single loop de-

***Internal modulation** is fully programmable from 20 Hz to 200 kHz with 3 digits resolution. The generators can also function simultaneously as signal generators and independent audio oscillators – two instruments in one.*

***Pinpoint frequency tuning** provided by optically coupled, magnetically detented spin knob. Combines digital precision with the speed and convenience of analog control.*

***Built-in, easy-to-program IEEE-488** interface ties the signal generator capability of the instruments to the power of automated system control. Talk/listen capability provides "learn" and "teach" modes.*

***Output level adjustable** in 0.1 dB steps from + 19 dBm (13 dBm above 520 MHz) to -140 dBm – displayed in dBm or volts and in relative or absolute units.*

IEEE-488

ed technology can specify with confidence.

sign that both improves reliability and lowers maintenance costs; a Surface Acoustic Wave (SAW) device to achieve low noise performance; and a delay line discriminator in a phase-locked loop that improves spectral purity and increases the modulation flexibility of the instruments.

A major emphasis on packaging design minimizes RF leakage and insures spectral purity during servicing. Fluke's own thick film hybrids improve RF performance and keep the parts count low. And a high efficiency power supply helps reduce weight, volume and heat rise.

Versatile modulation brings you two instruments for the price of one.

AM, FM and ØM are internally selectable. Modulation frequencies from 20 Hz to 200 kHz can be selected. Modulation can be applied separately or simultaneously for frequency, amplitude or phase, and the internal signal can also be used as an independent signal source, separate from the RF output, giving the user two instruments — a signal generator and an audio oscillator — in one high performance package.

A high deviation mode of up to 1 MHz or 100 radians is provided for frequency of phase modulation. External dc coupling for AM and FM is also available.

More microprocessor benefits.

The advanced 16-bit microprocessor control of the 6070A and 6071A makes these signal generators easy to operate and a pleasure to use.

Complex functions are executed rapidly from simple, direct keyboard commands.

A remarkably fluid-feeling spin knob gives even greater precision and control by allowing you to tune around any frequency, amplitude or modulation parameter, or spin quickly to another setting: rapid-tuning convenience with digital precision.

A built-in memory for storage of front panel set-ups is provided to save time and reduce operator errors. And the 6070A and 6071A also include a relative units function that allows you to define a zero point for subsequent programming, useful in both the frequency and amplitude domains.

Both instruments are IEEE-488 programmable for complete system use. Plus self-diagnostics, error code displays, digital sweep and other special functions combine to simplify testing in any RF design application. A full line of options and accessories is available to expand the capabilities of the 6070A and 6071A.

For more information on these new signal generators, call toll free **800-426-0361,** use the coupon below or contact your nearest Fluke sales office.

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System control just got simpler: Fluke redefines the operator-ma

Fluke has good news for builders of automated test systems: instrument control just got easier. With our new 1720A, we've provided the missing link in available systems technology that gives you total control: from design, through software development, to the production environment.

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Designed with a touch-sensitive display: because your test time is money.

The first thing you'll notice about the 1720A is its simplicity. No complex controls clutter the front panel, and there's no computer-language keyboard for an operator to deal with.

Instead, the operator interacts directly with the screen on the 1720A—a soft-labelled CRT display

chine interface.

that you program according to the skill of the user and the specifics of your test procedure. Your software presents instructions, choices and even safety warnings to the operator via the display, as well as measurement data from instruments in the test system. The operator responds by touching designated areas of the display, and is able to work through even complex routines quickly after a minimum of training.

The benefits of speed, simplicity and program security.

With the operator's attention focused only on the 1720A display for all control functions—instead of being split between an assortment of devices—productivity can be improved dramatically.

Your software remains in complete control of the procedure—a guarantee that test and measurement routines will be followed to the last detail. Graphic attributes such as double-sized, reversed, highlighted or flashing characters are at your disposal to draw the operator's attention to critical items.

While our design lets you restrict operator access to the controller and application software, the 1720A does come complete with a standard computer keyboard for programming. We simply made it detachable.

A software specialist or engineer can connect this keyboard to the 1720A without taking the controller out of its rackmounted production test environment.

The real bonus: 16-bit computation power plus versatile memory and control features.

The 1720A is built around a 16-bit microprocessor with a standard read/write memory of 60K bytes and a 175K byte floppy disk; providing all the computational power of a mini-computer.

But for applications needing greater speed and larger storage, Fluke's file-structured E-Disk™ extends the 1720A's working storage to as much as 256K bytes.

IEEE-488

Rackmountable and fully compatible with all IEEE-488 bus instruments, the 1720A is equipped with two independent IEEE-488 and RS-232-C interface ports.

How to get your hands on a 1720A.

To demonstrate the far-reaching applications of this new instrument controller in ATE production testing, data acquisition and process control, Fluke is holding 1720A Systems Seminars throughout the country. To sign up, or simply get more details on the 1720A, **call toll free 1-800-426-0361**, or use the fast-response coupon below.

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TI offers these versions of popular RS422 drivers/receivers as a second source. AM26LS31/32A and MC3486/87. Ideal for high-speed differential transmissions in a dedicated system. Enable for all four channels is a big plus, too.

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SN75437, the next generation low-power quad driver with 700-mA drive capability, obtained by using unique single-saturated transistor output, features 200-mW standby (typ) and 35-V switching capability. This device is available in a 2-W copper lead-frame DIP.

UDN2841 and UDN2845 — 1.5-amp quad drivers with DTL, TTL and 5-V CMOS-compatible inputs. Switching power up to 35 V. UDN2841 sinks from a negative supply while UDN2845 sinks and sources. PNP level shifting allows operation to negative voltage. Offered in a 2-W copper lead-frame DIP.

Applications include DC motor drive, telephone relays and discharge printers, to name just a few.

The TI ULN2064 Series (2064 through 2069) and, additionally, ULN2074 and 2075, are quad Darlington drivers with 1.5-amp output current capability. Switching voltages vary from 35 to 50 V depending on the device. ULN2074 and ULN2075 employ sink or source mode outputs.

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Nixdorf enters the mainframe computer market

by John Gosch, Frankfurt bureau manager

The medium-sized 8890 that competes with IBM's 4331 will be offered in the U. S. in about a year's time

Though Europe's small-computer and terminals market has still much room for growth, the competition is getting stiffer. So one way for a firm to get ahead faster is to move into the mainframe business, and in Europe that invariably means going head on against International Business Machines Corp.

That's just the approach West Germany's Nixdorf Computer AG is taking, and the tool with which the Paderborn-based company wants to prick the U. S. giant is the 8890, a medium-sized mainframe system with IBM-compatible channel interfaces announced in Munich last month [*Electronics*, Sept. 25, p. 64]. Nixdorf is aiming the system at those of its traditional small-computer customers who want to move up in data-processing power, as well as at new customers "whom we want to offer a genuine, economical alternative to IBM systems," says Klaus Luft, Nixdorf's vice chairman. The 8890's prime targets are the models 1 and 2 of IBM's 4331. Nixdorf expects to initially sell about 100 a year and will offer it in the U. S. in approximately 10 to 14 months.

The 8890's compact, modular, and expandable central processing unit stems from two years' cooperation with Israel's Elbit Computer Ltd., a Haifa-based firm in which Control Data Corp. of Minneapolis has a 37% share. Under the licensing agreement, Elbit has contributed its know-how to the 8890 CPU's development and is now supplying vital CPU parts to Nixdorf, but system production, marketing, servicing and future 8890 modifications, are in the hands of the German firm.

A good deal. For about $200,000, buyers of Nixdorf's 8890/30 also get disks, a printer, four displays, and a magnetic-tape unit.

Vice chairman Luft considers the move into the mainframe market an important step and sees the 8890 as an "appropriate supplement to our traditional product spectrum." That spectrum encompasses work-station–oriented data-processing equipment, small-business computers, and decentralized data handlers for use at medium-sized and large organizations. The recently introduced 8860, a family of network-oriented data-processing systems [*Electronics*, Feb. 14, p. 82], is already making its mark in the field.

With this product spectrum, Nixdorf has become one of Europe's most successful and fastest-growing data systems producers, with more than 30,000 machines installed worldwide. Business this year is expected to reach 1.5 billion deutschmarks, equivalent to $830 million. That would top last year by about 20%, an annual growth rate that Nixdorf has maintained for many years. This year, the work force will grow from 12,300 to 13,000. Of note is the company's engagement in the U. S., where sales rose to around $100 million last year to make Nixdorf the strongest European contender on the U. S. computer market.

The newcomers. The new system comes in two versions, the 8890/30 and 8890/50. The basic price for the former is approximately $200,000. For that money, customers will get a configuration with a main memory capacity of 1 megabyte, fixed-disk devices with three times 70 megabytes, one line printer, four display units, and a magnetic-tape unit with a streaming-mode tape containing 1,600 bits per inch. The price for a well-equipped 8890/50 systems configuration is roughly $500,000, with the upper limit at around $1.4 million.

According to Gerhard Wagner, head of Compatible Informations Systeme/CIS, Nixdorf's marketing support and distribution organization, the 8890 boasts a number of features that should appeal to many potential customers. The microprogrammable CPU ensures a flexible expandability, because all hardware components work asynchronously and independently of each other and are interconnected via a hierarchical bus system. At the top of the hierarchy is an extremely fast central bus with a 9-megabyte/second transmission rate. The input and output buses at the second-hierarchy level work at 5 megabytes/s.

In parallel. Instead of cycle-stealing principles, the 8890 uses independently operating processors. This means that computer tasks can be solved in parallel, which in turn relieves the CPU for other functions and thus spells a high system throughput. Also, both fixed and removable disks can be used. The main memory capacity is expandable from 1 to 4 megabytes so that the 8890 may adapt to different tasks. Using multiprogramming and virtual storage techniques, the system is suitable for batch processing and dialog applications, Wagner says.

The 8890/30 works without and the 8890/50 with an instruction preprocessing unit. The IPU is capable of handling overlapped instructions. Microprogramming ensures that new or expanded instruction sets can be emulated, that additional operating system functions can easily be implemented and that, if required, parts of the system software can be shifted into the microprogram.

Like the CPU and its main memory, the input/output system is based on a modular concept. Up to six microprogram-controlled I/O processors serve both fast and slow peripherals. Direct connections and compatible channel interfaces guarantee the hookup of either Nixdorf peripherals or of external control units for special peripherals and plug-compatible devices.

Application areas. For the 8890, Wagner sees three main areas of applications—as a central computer, a distributed data-processing machine, and a dedicated system. In the central computer application, the virtual operating system with multiprogramming in 12 partitions allows combined on-line and batch processing. In a dedicated application, the 8890 can solve special problems and thus make an organization independent of other computer services and installations.

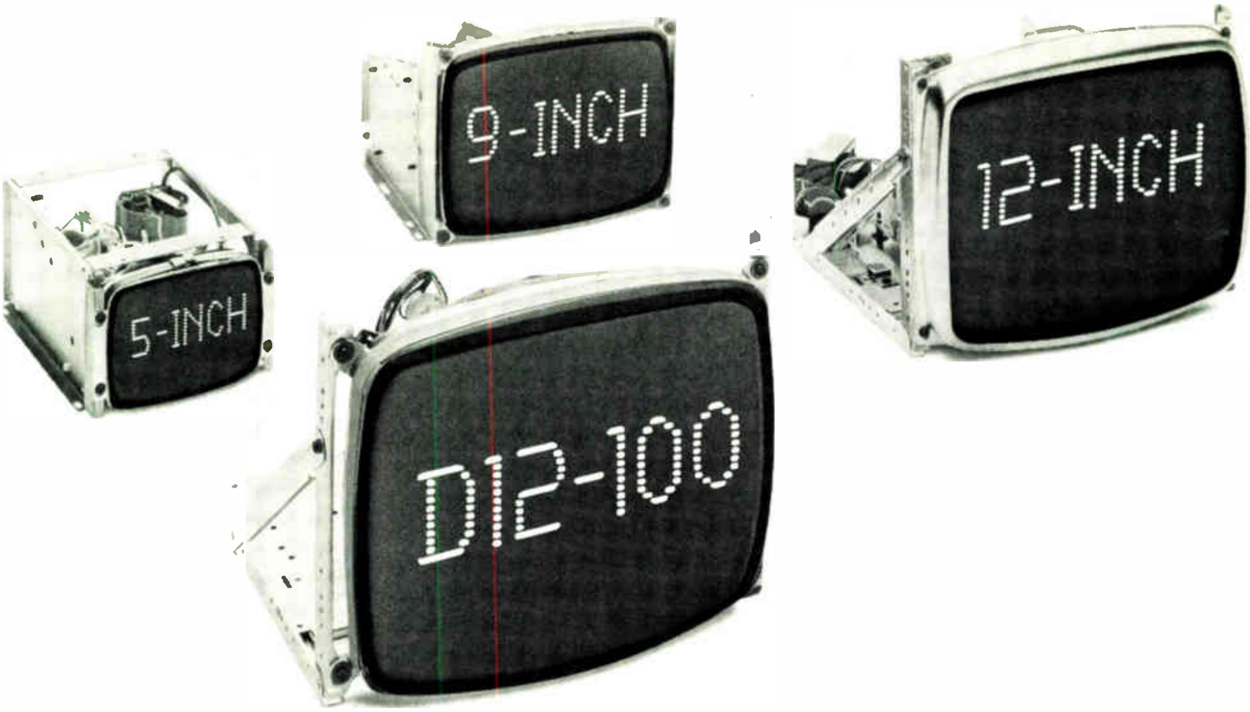
In the distributed data-processing application in computer networks, for example, the 8890 offers flexible communication possibilities. Up to 16 lines can be used for character- and bit-oriented procedures. Furthermore, the lines allow the operation of up to 32 local display-based work stations as well as communications with other computers and terminal systems.

Japan

Programmable digitizer plugs into high-resolution, sampling-rate gap

Analog signals can now be sampled with a resolution of 10 bits at rates up to 60 megahertz for subsequent display on a cathode-ray-tube monitor or as hard copy or for further processing or measurement. Initially, though, the 390AD programmable digitizer, which was developed by joint venture Sony/Tektronix Corp., will be available only on the Japanese market.

The new instrument fills a hole between a Tektronix instrument having a 200-MHz sampling frequency but only 8 bits of resolution and a Biomation unit having 10 bits of resolution but only a 10-MHz sampling frequency. It can trade its maximum sampling speed of 60 MHz and memory capacity of four kilowords (by 10 bits) for a two-channel mode in which both sampling speed and memory capacity per channel are halved. A single breakpoint allows the sampling speed to be changed at one point along the time base. Since a single time base is used, this point is the same on both channels in the dual channel mode. Pre- and post-trigger modes of operation enable



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More big ideas are coming. For further information and specifications, write: CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call (312) 773-0074.

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The quality goes in before the name goes on.

Options. The Sony/Tektronix 390AD programmable digitizer can display its output on its own digital readouts or drive external monitors or recorders.

storage of the signal before or after a trigger signal.

Built-in automatic calibration enables the instrument to maintain accuracy of gain within ±0.1% and reduces dc drift to within ±0.2% for accurate, reproducible measurements. The nominal resolution is 10 bits, or one part in one thousand, but at high frequencies the dynamic range falls from more than 8.5 effective bits at 1 MHz to more than 7.5 effective bits at 10 MHz. Furthermore, gain falls by up to 3 dB at 15 MHz. Aperture jitter, including the internal clock's, is less than 150 picoseconds.

American conversion. The instrument, like its maker, is a joint venture of sorts. Though designed in Japan for the domestic market initially and hopefully for the world market eventually, it uses hybrid analog-to-digital and digital-to-analog converters that are provided by the American parent.

The a-d process uses two 5-bit converters in a serial parallel conversion process in which the signal is first digitized into 32 levels, and then the intervening levels are digitized. The d-a converter is used between the two stages of digitizing.

The system makes extensive use of the General-Purpose Interface Bus (GP-IB) and the Tek SPS version of the Basic language for the programming needed for automatic measurement and for waveform analysis processing. Suitable control and display systems include the Tektronix graphic computer 4050 series and the firm's minicomputer CP4000 series using Digital Equipment Corp.'s PDP-11 or LSI-11.

After image. An analog output on the rear panel makes it possible to display the stored transient waveform on a cathode-ray-tube monitor as either a Y-T or X-Y display, giving the equivalent of a storage oscilloscope. The instrument can also drive chart recorders and plotters or be used in a stand-alone model by means of digital readouts on the front panel.

The 390AD's price, at today's exchange rate of 208.20 yen to the dollar, is $16,700 for the benchtop version and $16,800 for the rack-mounted version. **-Charles Cohen**

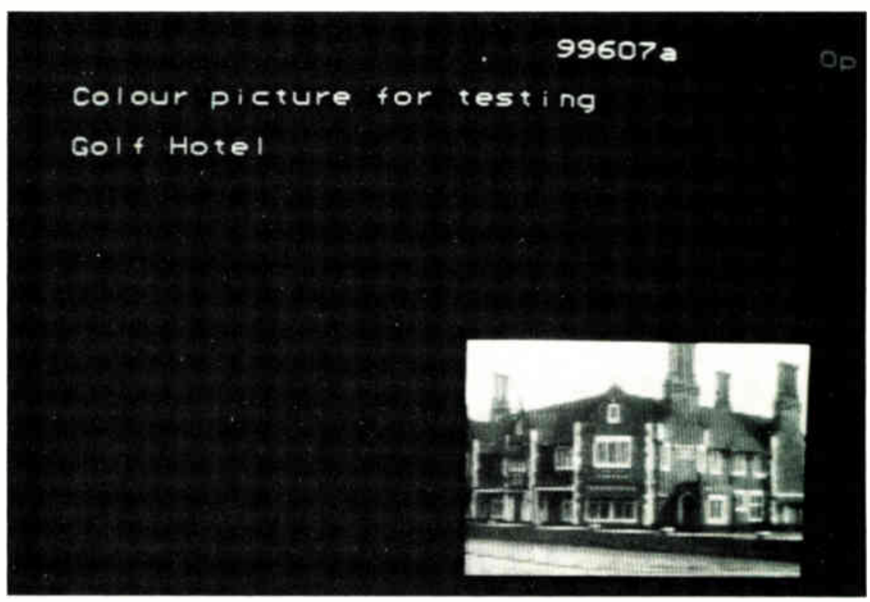
Great Britain

Prestel to transmit color photographs

Not so long ago, the display of full-color photographs on a videotext receiver linking television and telephone had been thought prohibitively expensive. But the marriage of videotext to picture-coding techniques developed initially for digital television, together with the falling cost of semiconductor memory, has completely altered the situation.

With an eye to the future of its Prestel service, in operation since March 1979, British Telecom, part of the post office, has demonstrated prototype Picture Prestel hardware. Though it has no plans for an enhanced service before decoder costs become realistic—probably around the end of the decade—it is making the technology available now to potential overseas purchasers of Prestel and to companies wishing to offer private viewdata services.

Strategic move. British Telecom's aim is nail criticism that Prestel, as the original viewdata system, is incapable of evolution. In addition, and more immediately, researchers aim



Eye appeal. To leapfrog the competition, British Telecom has developed a version of Prestel capable of displaying color photos along with text, as in this realtor's advertisement.

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It has I/O expandability: serial, parallel and S-100 Bus interface is standard. Audio-cassette recorder jacks and acoustic coupler are optional.

No sorting!

FINDEX is programmable in easy to use Business BASIC. It supports also a full ANSI FORTRAN, COBOL 74 or a BASIC compiler, as well as a MACRO assembler. APL and PASCAL can be used too. The 26k BASIC includes a comprehensive file management capability. There is no loss of time for data to be sorted. As data is typed in, it is immediately entered in its proper place in the desired order: alphabetical, zip code, price, quantity, etc. There is no loss of time for retrieving data either. The computer will access the requested data directly without going through any lengthy search.

Powerful!

The FINDEX BASIC is the most extensive Z-80 BASIC language available.

- Direct access to CPU I/O ports (INP,OUT);
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- Matrices with up to 255 dimensions;
- Error trapping;
- Fully formatted print output (tab, asterisk fill, floating $ sign, scientific notation, trailing sign, comma insertion, etc.);
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- Random files (record I/O).
- Linked keys (any string) indexed sequential files—no need for sorting!
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to improve Prestel graphics with a system called dynamically redefinable character sets, or DRS. DRS adds an inexpensive page store to a videotext terminal—basically a standard TV set with decoder—so that it may be reprogrammed with a wide range of extra symbols like those used for computer-aided design. Keith Clarke, a member of the Prestel marketing team, makes the point that Picture Prestel and DRS can both also be applied to broadcast teletext, thus sharing hardware decoder costs.

What post office engineers have in mind is a facility to insert a full-color picture [*Electronics*, April 10, p. 44], typically one third as high and as wide as the screen, into a conventional videotext frame carrying explanatory text. The hardware needed in the user's TV set, besides the conventional Prestel decoder, is a microprocessor control card with a 24-K-byte picture store.

The original picture is converted by a TV camera into its luminance and two color difference components. It is then reduced in size to cut the data storage requirement, which is further halved by the use of differential pulse-code modulation. Next the luminance and chrominance signals are multiplexed for storage and later transmission to the customer's receiver. At the receiver, the incoming data is decoded by the microprocessor and stored in the picture memory.

Compared with the simple 8-K-byte store of the Prestel decoder, the extra page memory is a lot. Yet 24-K bytes is the size of page store proposed for the Canadian Telidon alphanumeric-geometric videotext services, so that a Picture Prestel terminal could probably be provided at a comparable cost. For the moment, though, the prototype hardware with no attempt at cost reduction costs $2,000.

Time of arrival. By the late 1980s, the earliest date for Picture Prestel's introduction, memory costs will have fallen and faster data links will also be available. Prestel currently operates at 1,200 bits per second, so a picture takes a minute to build up—much too slow to be acceptable. At 4.8 kb/s—the highest data rate currently available over the public switched network—picture transmission takes 15 seconds. By late this decade an overlay System X digital network will be in place offering a basic 64 kb/s and 1-second picture transmission time or alternatively larger pictures. **-Kevin Smith**

Japan

Disk has 3 audio, 1 picture channel

Victor Co. of Japan has just unveiled a prototype of a digital audio disk system whose groove-less disks use four channels—three for stereo and one for still-picture playback on a TV set. The third audio channel drives a center speaker to give a larger stereo sound field than available with a two-speaker system. The real rather than phantom center channel makes the position of the sound sources playing the music more precise and stable.

Company engineers say that they included the extra two channels in the belief that digital audio disks should be more than just a higher-fidelity version of present records. The disk was proposed this June to the Digital Audio Disk Conference, which is in the process of selecting an industry standard from three pulse-code-modulation audio disks officially submitted to it so far. Moreover, the Audio High Density system, to give it its formal name, will be displayed amid much other audio PCM equipment at the 29th all-Japan audio fair that opens in Tokyo in mid-October.

Though the aim is to demonstrate how much three-channel improves on two-channel performance, the two-channel version is at least as good as any other, and Victor says hardware manufacturers could offer the third channel as an option. Still-picture playback can also be an option and will be expensive until the falling prices of 64-K or larger dynamic random-access memories

drive down the cost of one-frame picture memories.

However, Victor is convinced that the picture should be on the disk because today's young people have been surrounded by television since the day that they were born. One demonstration of this so-called cross-media capability showed how an amateur photographer's shots of members of a Los Angeles band were good enough to accompany and enhance the music. The actual capacity of the still channel is slightly more than one still picture a second. But Victor suggests that each picture should be left on the screen for 5 to 10 seconds if the viewer is not to be overwhelmed.

There is also another potential use of the fourth channel, though Victor is not pushing it at present. The still picture could be traded for a fourth audio channel because all four channels have the same characteristics.

Technical details. The AHD system plays back a full hour of material on each side of the disk because the disk resembles the one used in the firm's Video High Density video disk player—in fact, it could be played back by a VHD system equipped with the proper electronics. The major difference is that the audio system has a 6.14-megahertz clock rate, while the video system is analog. Thus Sharp Corp., Matsushita, GE and others who intend to manufacture VHD systems are also potential suppliers of AHD systems.

Since the AHD system is compatible with the VHD system, it uses the same 26-centimeter grooveless disks as the latest version of VHD and rotates at the same 900 revolutions per minute. The audio signal is sampled at a 47.25-kilohertz rate to provide audio frequency response to 20 kHz and furthermore guard against unauthorized copying. The 16-bit straight-line (linear) encoding has a theoretical dynamic range of 96 decibels and an actual range of about 90 dB.

The approximately complete redundancy of the recording format is said to eliminate dropouts, which are of a burst type similar to that of video tape. **-Charles Cohen**


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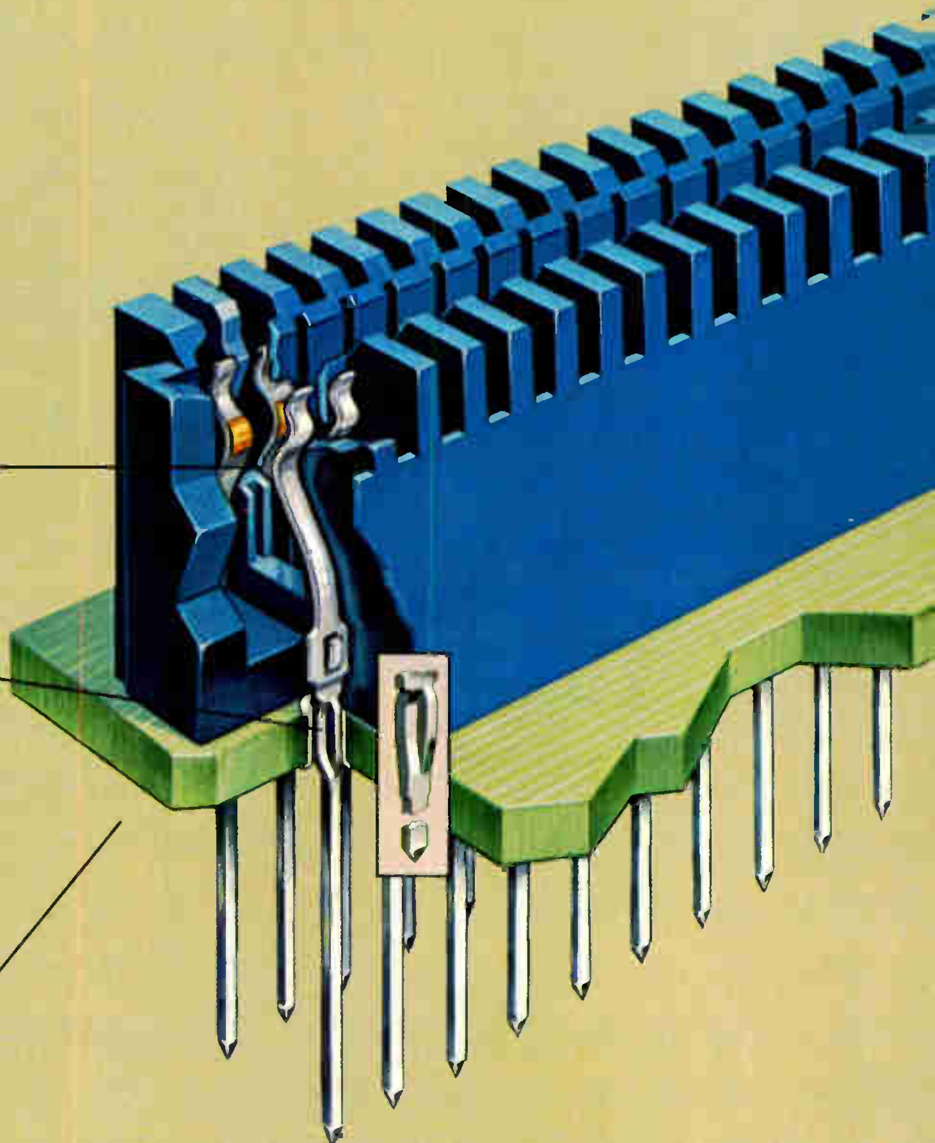

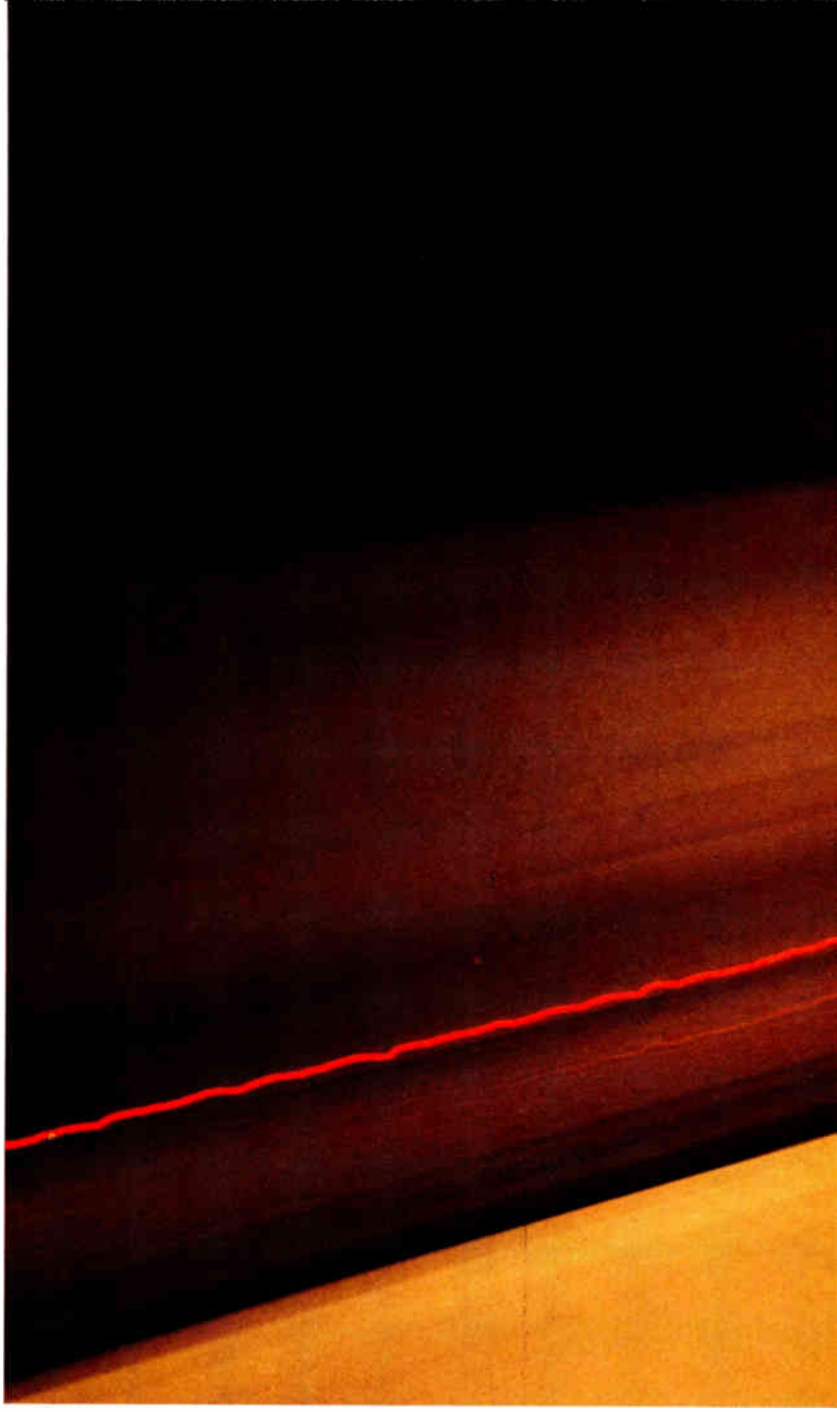

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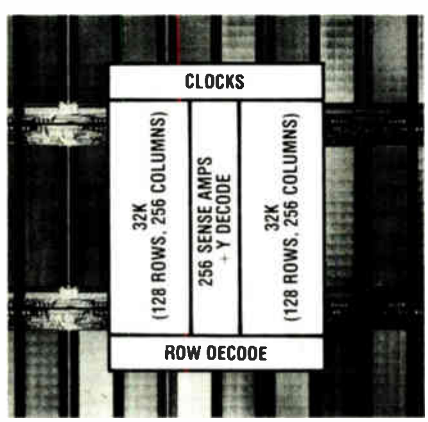

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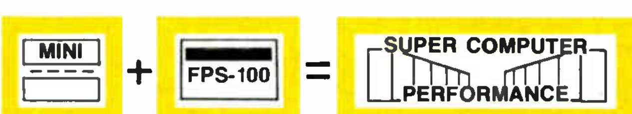

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Test Conference widens embrace

Annual meeting has become important to design engineers as well as test experts as problems gain sophistication

by Richard W. Comerford, Test, Measurement & Control Editor

For the last 10 years, October for test managers and tester manufacturers meant the annual clash at Cherry Hill, N. J., the site of their Test Conference. This year, however, the conference has moved to larger quarters in Philadelphia, at the Philadelphia Sheraton, and will take place Nov. 11–13. But more significant are changes taking place in the conference's technological focus and, indeed, the industry itself.

No longer can the get-together be regarded as the province of test engineers alone. The serious development of on-chip and on-board test structures, the sophistication of the software needed for design verification and test generation, and the effects of very large-scale integration on both vendor and user profitability have made the annual meeting equally important to design engineers. This fact, strongly evident last year, is even more obvious this year.

Three sessions are being devoted to testability, two on design at the chip and board levels and one on self-test techniques. The increasing need for better software, for both design verification and simulation and test pattern generation, is also underscored by the creation of two sessions to deal with the topic. And the universality of memory and the latest challenges in its design and testing are underscored by two sessions and an evening workshop.

Though the organizers of the conference—general chairman Edward Thomas, program chairman Joseph Tomei, and their assistants—have succeeded in focusing the conference on methodologies related to these important topics, they have left no one out. They have also provided forums for points of interest such as analog and digital component and production problems, test economics, and reliability considerations.

Attention will be directed to the major topics in session 1 by keynote speaker Lester Vadasz, vice president of Intel Corp., Santa Clara, Calif. Vadasz states that "VLSI technology continues to push the testing technology." Product features to enhance testability will help, he notes, but he also sees a sharp contrast between the need for more thorough diagnosis and the economics of high-volume testing.

Practical examples of enhanced testability will be provided in session 2, again this year under the chairmanship of International Business Machine Corp.'s Thomas Williams. In their paper on design for autonomous testing, E. J. McCluskey and S. Bozorgui-Neubat of the Center for Reliable Computing at Stanford University, Palo Alto, Calif., will describe how the 74181 arithmetic and logic unit/function generator was reconfigured to automatically partition and test itself on receipt of a test mode signal.

They will be followed by Kyushik

TEST CONFERENCE SESSIONS

	Tuesday, Nov. 11	Wednesday, Nov. 12	Thursday, Nov. 13
MORNING	SESSION 1 9:30–11:30 Keynote address and invited papers How to test VLSI – Lester Vadasz, Intel Corp.	SESSION 6 8:30–12:00 Memory testing (1) 7 8:30–12:00 Design for testability 8 8:30–12:00 Test economics	SESSION 13 8:30–12:00 Test and system hardware 14 8:30–12:00 Simulation, verification, and pattern generation (technology and techniques) 15 8:30–12:00 Integrated-circuit failure modes
AFTERNOON	2 1:30–5:15 Design for testability 3 1:30–5:15 Hardware pattern generation for memory and LSI testing 4 1:30–5:15 Analog testing	9 1:30–5:15 Memory testing (2) 10 1:30–5:15 Self-test techniques 11 1:30–5:15 Production test problems	16 1:30–5:15 Microprocessor testing 17 1:30–5:15 Simulation, verification, and pattern generation (tools) 18 1:30–5:15 Quality, reliability testing
EVENING	5 8:00– Memory test hardware workshop	12 8:00– Board test strategies workshop 12A 8:00– Digital Atlas is changing – how does it meet your needs? (workshop)	

Probing the news

Son of Digital Equipment Corp., Westboro, Mass., and D. H. Pradhan of Oakland University in Rochester, Mich., speaking on a programmable logic array designed for testability. The authors note that, in addition to stuck-at faults, programmable logic arrays "exhibit faults that are much different"—crosspoint faults (caused by missing or extra devices in the array) and bridging faults (a class of shorts). Their design approach, though it can require extra logic in addition to or instead of one pinout, permits almost perfect fault coverage. In another paper (session 14), they tell how to prevent untestable bridging faults by design.

After lunch, in session 10, Patrick Fasang of Siemens AG's Cherry Hill research staff will describe a go/no-go tester built onto the board of the circuit it tests. Called the built-in digital circuit observer, or Bidco, it is a practical application of the Bilbos (the "lb" for logic block) described at last year's meeting. Also during this session, a team from EFCIS (Société pour l'Etude et la Fabrication de Circuits Intégrés Spéciaux) and LAAS-CNRS (for Laboratoire d'Automatique et d'Analyse des Systémes of the Centre National de la Recherche Scientifique) in France will unveil a self-checking error-detecting processor built from commercially available ICs.

Concerns about design strike at the very foundations of the conference—memory testing, for instance. In an invited paper, Richard Foss, president of Mosaid Inc. of Ottawa, (see p. 124), says that the general problem of soft errors, obscured by emphasis on alpha particles, can be ascribed to inadequate internal signal margins that can be measured approximately by users in present dynamic random-access memories.

But according to a paper from a group of Intel's memory-product reliability engineers to be given in session 6, all evidence is that "soft errors due to radiation are here to stay, despite efforts to reduce sensitivity, shield devices from alpha particles, implement system-level solutions to the problems, and so on." The authors describe soft-error methodologies and a Quadraport Memory Test System they will soon use to check alpha-induced fluxes in the 2164 64-K dynamic RAM and the 2167 16-K static RAM.

For VLSI memory, they predict increased soft-error sensitivity, with ensuing use of die coatings to reduce it making system-level testing even more important. Further, cosmic rays will become a soft-error source and soft errors in nonmemory VLSI will become a reality in several years, resulting in "a testing nightmare," they claim.

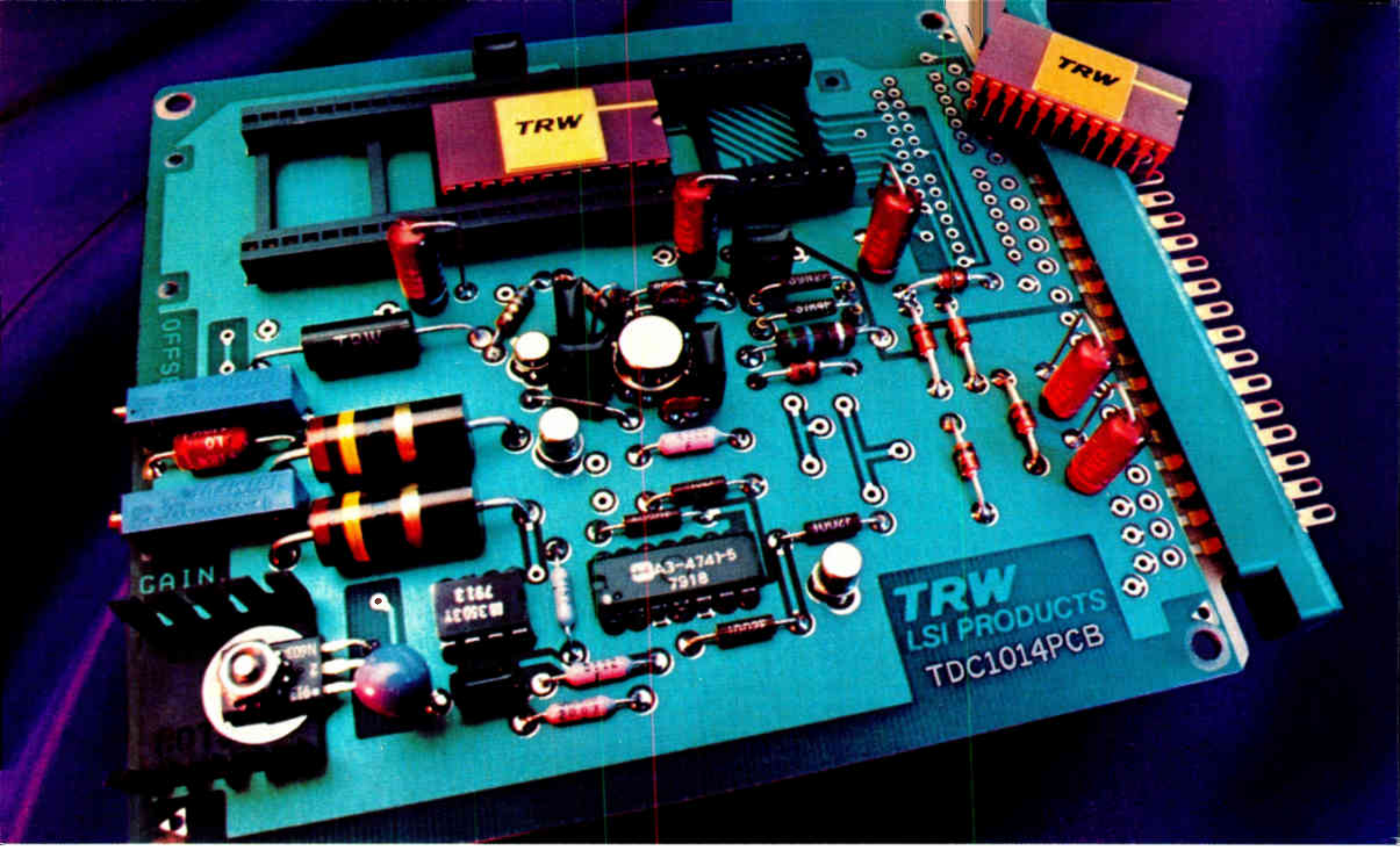
The solution to the problems that users and designers seem to be approaching, according to Edward Thompson of Comprehensive Computing Systems & Services Inc. in Austin, is an integrated environment for logic design and testing based on simulation. He notes that "with the increased role of digital simulation in the design phase, more emphasis is being placed on integrating simulation tools with the data base and then utilizing that information for testing."

Other problems. He also sees the approach as a possible solution to board design and test problems, supposing semiconductor companies to be willing to supply simulation models with their chips. While acknowledging several obstacles blocking such an approach, Thompson suggests some practical ways in which it could be accomplished. To establish the environment he calls for closer cooperation among designers, test engineers, and the developers of simulation tools.

Other important papers deal with such subjects as the pattern-generaton architectures of testers from Teradyne, Fairchild Xincom Systems, Takeda-Riken, and Adar in session 3; new approaches to codec and integrated filter testing in session 4; and test and screening methods to find failures and incipient failures in bipolar and MOS circuits in session 15. □

A second article, in the next issue, will examine new test systems to be shown at the conference.

Conference data is available from Doris Thomas, Box 3305, Wescoville, Pa. 18106; phone (215) 797-5018.



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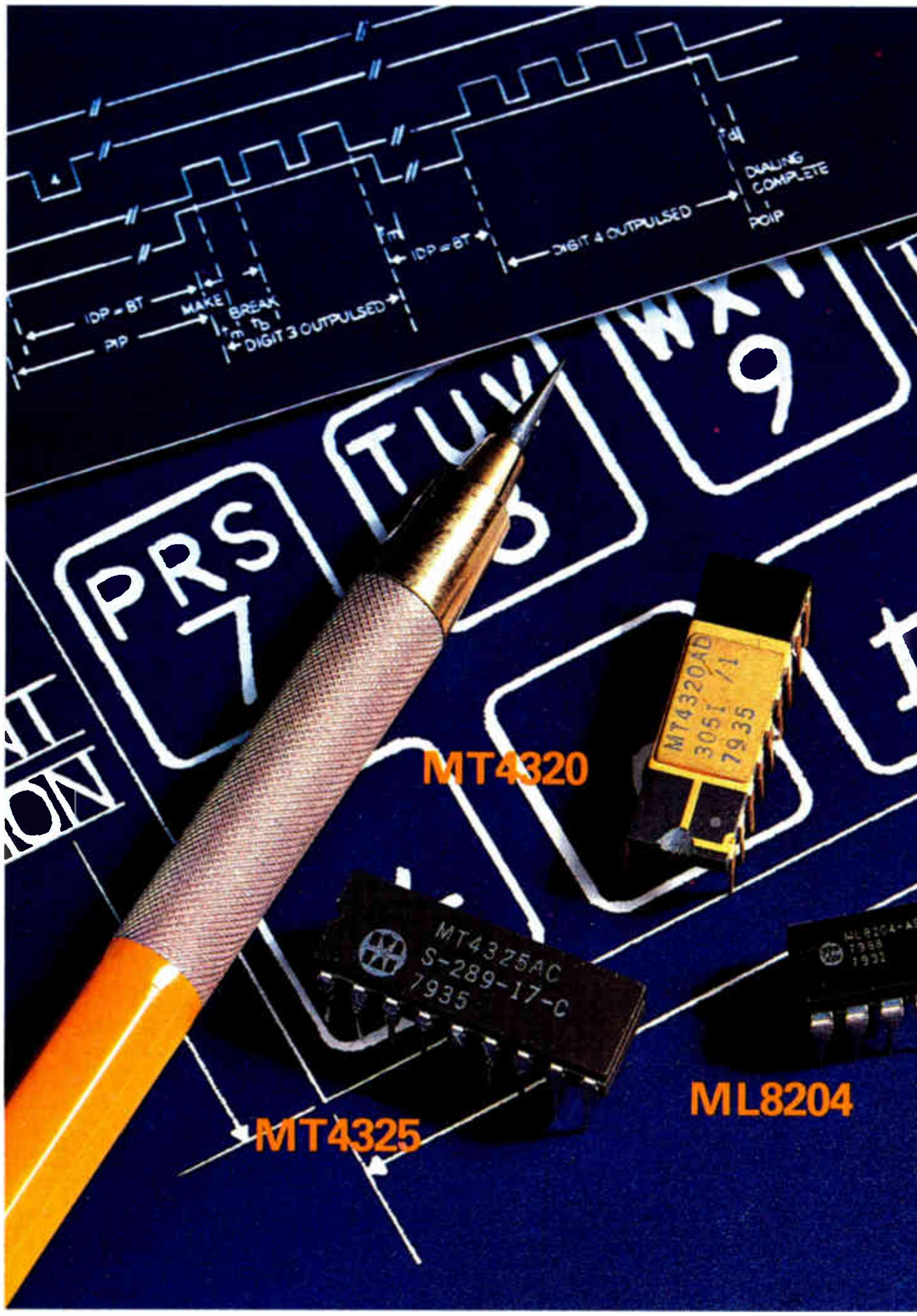

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Circle 94 on reader service card

Information processing

Document storage: a billion-dollar prize

Study says systems based on film or video disk and controlled by computer will become integral part of paperless office

by Kevin Smith, London bureau manager

Within a decade many big multinational corporations will be storing documents as well as data on jukebox-like video disks with capacities of up to 13 million pages, contributing to a total U. S. and European market for electronic document storage of $1.56 billion.

Users of these electronic document storage systems, or EDS for short, will work through high-definition cathode-ray-tube work stations on their desks to call up documents over a high-bandwidth communications link in response, say, to a telephone inquiry about an insurance claim. As the operator presses the keys, a mini- or micro-processor controller will rapidly search through an index on a fast magnetic disk before calling up and accessing the needed optical disk, itself holding up to 300,000 black and white images. Other systems on the market will use film-based storage media.

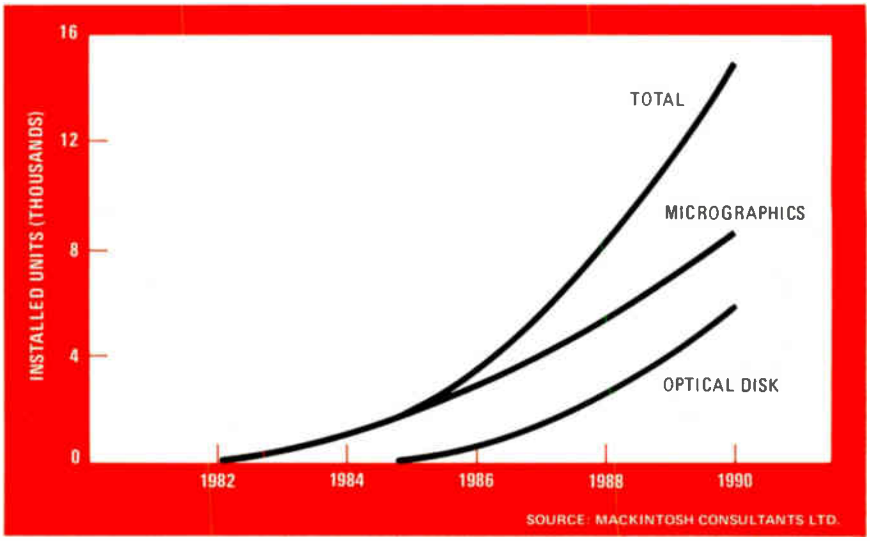
This scenario for the 1990s is conjured up in a study by the British firm Mackintosh Consultants Ltd., which was a year in preparation for 26 client companies with a real or potential interest in the EDS market. Among those companies with an interest in film-based systems are Bell and Howell, Eastman Kodak, and Fuji Photo. Video-disk manufacturers include Philips, Thomson-CSF, and Mitsubishi Electric, while contributing computer companies include Sperry Univac and Hitachi. Finally, among the companies eyeing the office of the future are Xerox, Exxon, and Nexus, the last funded by Britain's National Enterprise Board.

Though purposely restricted in scope, the report provides one more insight into the so-called paperless office of the future. Yet one of its first conclusions is that paper-based systems will not be thrown out overnight. EDS, says Ian Galbraith, who led the Mackintosh team, is at a stage now comparable to the pioneering days of electronic data processing. Stand-alone EDS systems, not cheap at $250,000 apiece, will go to the large and sophisticated users that already have a computer capability. Right now, EDS is not cost-effective for small applications, though less expensive systems will begin to appear as peripherals to large computer installations.

With paper-based office systems already under siege by electronic systems, EDS is needed because document signatures, letterheads, and graphics such as bar charts and scribbled remarks on the received document cannot be handled in any other way, says Galbraith. If documents can be easily encoded into data, he adds, they can most likely be eliminated.

The prime application for EDS is vendor records. "That's the biggest by far," says Galbraith, who points out that many documents must be kept for legal purposes. The storage of technical drawings is a second major application area; a third is in public administration.

Flexible storage. Attempts to find alternative storage media to paper are not new. Micrographics systems can reduce storerooms of filing cabinets to a shelf of microfilm, but the systems have not achieved wide acceptance. The reasons: a reader is needed, file conversion costs are high and introduce delays, and quality control is a problem. But upcoming document-storage systems onto which computer techniques have been grafted, whether based on film or video disk, will add a new flexibil-



Quick climb. Estimate of installed base of electronic document storage systems in the U. S. shows micrographic media outdistancing optical disk types because of greater capacities.

ity that outweighs these disadvantages of today.

Records held centrally can be simultaneously accessed anywhere in a building within 1 second over remote display terminals. There will be a user-friendly interface for filing and indexing, as well as retrieval guidance in the form of user prompts. And despite the disadvantages of film, it will predominate in first-generation EDS systems because of its low storage costs.

Video disks at first. Video-disk–based systems will play a key role in the mid- to late 1980s. Already they are cheaper than magnetic-disk storage and their price per bit will fall faster. Compared with film, the video disk provides both random access to data and direct read after write. But a single disk system does not have enough capacity, making automatic changers essential. By 1990, one disk will store 300,000 compressed black and white images or, if a gray scale is provided, 20,000 data-compressed images. If the characters alone are coded as in a word-processor application, one disk will accommodate 3 million pages. Mackintosh suggests that production auto changers will accommodate 40 to 80 disks.

Advances in data-compression techniques for images and in optical character recognition will help overcome initial equipment shortages. Typical facsimile algorithms, for example, give an 8:1 data reduction for a black and white standard-sized office document. Other algorithms for handling photographs and gray-scale images are not so effective. Consequently, Galbraith sees a battery of algorithms being brought into play to store documentation in the most compact way.

With a battery of new technologies under development, the danger, he says, is of putting unrealistic time scales to known developments. But with a modest market of $12 million in Europe and $20 million in the U.S. by 1982, Galbraith concludes that the real growth phase is still five years away. That, he says, gives forward-looking companies time to develop their strategies. ☐

Government

France wants bigger piece of pie

Latest five-year plan calls for accelerated effort in electronics and electronics R&D as a keystone

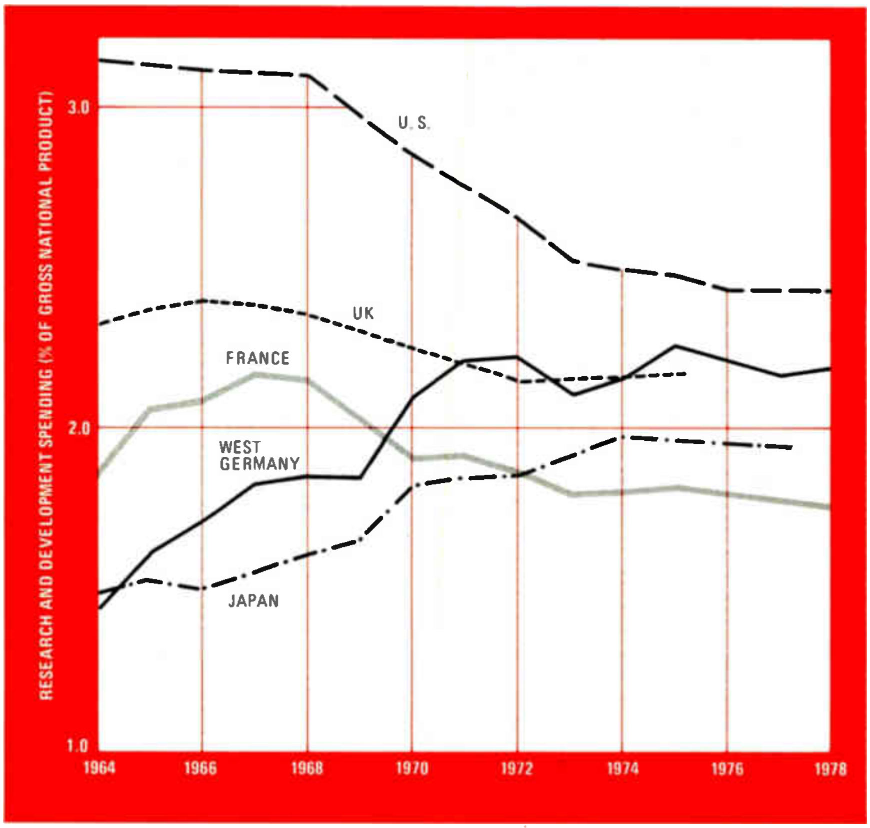
by Kenneth Dreyfack, Paris bureau

If France does not house one of the world's foremost electronics industries five years hence, it will not be for lack of government interest. Hardly a Parisian day passes without some bureaucrat or official—even the president himself—reminding the public that the cost per bit of semiconductor memory is dropping all the time.

All these officials are convinced that the country's future depends to a large extent on ensuring a substantial piece of the international action in integrated circuits, computers, data communications, and office automation over the coming five years. Thus, electronics and electronics research play a significant role in the eighth five-year economic and social plan unveiled this month, as well as in the flurry of specific government programs in varying stages of realization.

The plan foresees reinvigorating French research and development spending, in both the private and public sectors, so that it reaches 2.15% of the gross national product by 1985, a project estimated at $7.14 billion. To meet that goal, the planners suggest better management of public research projects so that more resources are devoted to actual research and less to bureaucratic activities; greater cooperation between public and private research institutions; greater interdisciplinary research; and a series of fiscal and institutional moves to encourage private industry to boost R&D spending.

Looking for more. With the percentage of France's GNP spent for R&D dropping since it reached a peak in 1968, the new five-year plan calls for an increase to 2.15% by 1985.



Key areas. Another major goal is the use of new technologies to develop highly competitive industries in six fields: new energy sources, aerospace, marine technology, biotechnology, industrial production machines, and electronics. According to Prime Minister Raymond Barre, total government spending to develop these industries will come to nearly $25 billion over the next five years. The electronics entry, which is certain to get more than a sixth of that cash, is broken down into telecommunications, data communications, data processing, integrated circuits, and office automation. In each area, a major government program is either under way or about to be launched.

The telecommunications and data-communications projects are well advanced [*Electronics*, July 5, 1979, p. 85], but the IC plan launched in 1978 has yet to bear much fruit and the office-automation project starting up this year is still more or less wrapped in secrecy. With the two new joint-venture semiconductor manufacturers set up under the IC plan—Matra-Harris Semiconductors (owned by Matra SA and Harris Corp.) and Eurotechnique SA

(owned by National Semiconductor Corp. and St.-Gobain-Pont-à-Mousson)—just set to start production early next year, the government is already worried that its original plan will fall short of its mark.

That five-year, $180 million IC project aimed at creating a positive balance of trade in the devices in 1983. Now an interministerial committee is deciding how to beef up the project financially, convinced the goal cannot be met under the current plan. Whereas originally the five companies taking part in the project were to hold the equivalent of 35% of the $265 million French market this year, the government now figures they will have only 31%.

In enlarging the plan, the government will be focusing on increasing production facilities, promoting research in technologies such as gallium arsenide and magnetic bubbles and encouraging development of wafer production equipment. Matra can surely count on substantial government aid in setting up Euromask, a subsidiary created last month to develop a wafer stepper and other microlithography equipment. Similar aid is already going to another machine maker, Cameca, the Thomson-CSF subsidiary.

Trade deficit feared. Balance of trade is also a prime consideration in the office-automation project. The French government, noting the virtual nonexistence of any office-equipment industry now, fears that the impending explosion of word processors, electronic mail, and the like will leave the country with a $2.4 billion trade deficit by 1985. To avoid that, the government plans to dole out hundreds of millions of dollars over the next two years to companies willing to work on office-automation projects.

Many of these projects look good on paper. And French industry, conditioned to relying on government help to keep it going, is generally—though not unanimously—ready to sign on the dotted line. One very real danger is that French government and industry will wander off, hand in hand, into a theoretical never-never land far removed from the realities of the fast-moving and constantly changing world of international competition.

But the most significant danger probably stems from the government's political stake in all of these plans and projects, which must succeed if the present regime is to retain credibility. This means it will use all of its very considerable economic muscle to bully French industry into making the projects succeed, at whatever cost. Indeed, some equipment makers are already concerned about government pressure to buy ICs only from companies participating in the plan. Equipment makers are justifiably worried—if such makers as Texas Instruments, Intel, and Mostek are shut out—that such restraints on their purchasing policy will leave them at a serious disadvantage in international competition for equipment sales. □

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THE 1980 ACHIEVEMENT AWARD

Developers of projection mask aligner provided basic IC fabrication tool

by Pamela Hamilton, *New York bureau manager,* and Jerry Lyman, *Packaging & Production Editor*

When Offner, Buckley, and Markle applied know-how from building a big telescopes in 1960s to optical, mechanical, electronic problems of noncontact mask printing, they not only helped provide impetus for LSI but also changed Perkin-Elmer's direction

Enthusiasm for a 10-year-old project very often wanes among its originators. Not so with the team that put together Perkin-Elmer Corp.'s projecion mask aligner nearly a decade ago. That team—Abe Offner, Jere D. Buckley, and David A. Markle—brought a great deal of individual expertise to the design of what has now become a mainstay in the semiconductor industry. And the original excitement is still there in force, with a wealth of experience backing it up.

Verve, and the attempt to accomplish what others could not, propelled the Micralign project forward at the beginning of the 1970s. Prior to 1973, Perkin-Elmer had been mainly involved in Government research and development and had not done any design of commercial products requiring large-scale production. Drawing on experience they had from their Government assignments, Offner, Buckley, and Markle tackled Micralign.

During the mid-1960s, all three men had worked on the Stratoscope II—a telescope designed by Perkin-Elmer under contract to Princeton University. That telescope used special optics and an internal guidance system to distinguish objects up to 30 inches apart at a distance of 1,000 miles [*Electronics*, Feb. 8, 1963, p. 47]. In fact, Stratoscope II was Markle's first project at Perkin-Elmer. Buckley was already doing electrical and mechanical work for the electronic subsystems of the high-powered 3-ton telescope, and Offner was concentrating on the optics.

The warmup exercise for Micralign was a contract from the Air Force's laboratories at Wright-Patterson Air Force Base in the late 1960s. Called the Microprojector, the result was a system designed to project 1:1 patterns onto wafers. Later, a similar piece of equipment was built by Perkin-Elmer for Sylvania.

"We used conventional brute force for the optics," says Buckley. "The lens system was very similar to what other people had already done, but it covered 2-in. wafers." That technique had to be refined when the

The Micralign team. Abe Offner (on the left) was responsible for the optical system—the basis for the projection mask aligner. Jere D. Buckley (in the middle) provided much of the mechanical engineering know-how needed to integrate those optics into a system. David A. Markle (on the right) oversaw the total effort as project manager, using his systems expertise to look for and solve problems.

Micralign project came onto the horizon. Offner, who joined the company in 1947, was put to work on the new optical design.

"Approaches being taken in Japan, England, and Germany weren't coming up satisfactorily at that time, so we began with the idea of making a projection aligner with broadband characteristics by making it reflecting," he recalls. "We had previously designed a refracting system at Perkin-Elmer, but didn't consider that a satisfactory solution to the problem, both from the point of view of making the machines in production, with their complexity, and from the fact that it was a monochromatic design," he adds. His solution was the system using convex and concave mirrors depicted on page 108.

The difficult part of the design came with the scanning subsystem. "At the beginning, we didn't think of the scanning part," notes Offner. "We were more or less forced into it fairly quickly when we found we couldn't cover a 3-in. wafer."

There Markle and Buckley's talents came into play. "The basic optical design was with two concentric mirrors. It was a very simple and elegant scheme that Abe came up with," Buckley says. "However, the requirements imposed on the scanning system were a little more formidable until we added the system of folded mirrors that are now used," he says. "These established the relative position of the mask and the wafer, greatly simplifying the scanning requirements. That resulted in a unique insensitivity of the system to things that ordinarily would give a great deal of trouble."

The entire task required learning about the commercial marketplace and what was needed in a product to make it sell. "Up until Micralign, we never sold more than one of anything, because the Government usually only buys one," notes Markle wryly. Suddenly, the need to manufacture the machines so that they were not extremely costly, so that they ran well in harsh environments, and so that they were easily serviced became design problems.

"The challenge was to go from the beginning idea to a comprehensive system in a manner that was as simple as possible and that made the system as manufacturable, as serviceable, and as maintainable as possible," Buckley points out. "It was a big challenge from that point of view for most of us because of our aerospace background. It's a big jump from Government business to the commercial marketplace. We all had to make that jump in the process of designing the system," he says.

Because of their diverse backgrounds—Offner is a physicist, Markle a nuclear engineer, and Buckley a mechanical engineer—the trio could approach the system as a total design problem. "At a component level, we obviously used quite a number of commercial devices. But there was nothing in the way of a consequential subassembly or subsystem that we did not create ourselves," Buckley notes. "We certainly drew on our military expertise across the board—not just in electronics. We also had to integrate mechanics and optics. It really was an ideal product in that respect to try and find a fit for our skills in the commercial marketplace," he adds.

In fact, a major problem in the design of the system was the special ultraviolet light source required for the optics. Needed was a curved capillary mercury vapor lamp, but the manufacturers of flat mercury vapor

Projection printer lighted way to lower-cost, higher-resolution ICs

The mass production of low-priced large-scale integrated circuits with minimum features of less than 10 micrometers owes a great deal to the 1:1 projection printer. Without it, IC manufacturers would have had to use contact printing to put those high-resolution patterns on silicon—an approach that is far from cost-effective.

In contact printing, an emulsion or hard-surfaced pattern mask is aligned with reference points on a resist-coated wafer, then pressed directly onto the wafer and exposed to ultraviolet light. Projection printing, in contrast, uses a complex refractive or reflective lens system to project the mask's ultraviolet image onto the wafer. Because mask and wafer do not touch, it has two obvious advantages over contact lithography: it extends mask life, and it eliminates damage to or contamination of the wafer.

The high-quality emulsion mask required for contact printing must be discarded after about 15 exposures. The expensive chrome master used to create that emulsion mask can last for about 150 contact printings. But with projection printing, the same chrome mask can make about a year's worth of exposures—some 100,000 in all.

That economy, however, comes in a poor second to the chief benefit of projection lithography: the fact that it substantially increases device yield. Its use of a chrome master—the nearest thing to a perfect mask—minimizes circuit imperfections. Totally eliminated are yield losses due to mask damage that occurs when an emulsion is stripped from the wafer or when it picks up epitaxial spikes, silicon pieces, and dust particles and prints them on succeeding wafers. As a result, projection printing has improved yield by as much as 50%.

Such printing became a production factor in 1973 when Perkin-Elmer Corp.'s Optical Group delivered its first optical projection printer, the model 100 Micralign. This manually aligned machine could expose 3-μm details on a 3-inch wafer with an alignment accuracy of within 1 μm—more than adequate for the medium- and large-scale ICs of the time. The machine was constantly improved: 4-in.-wafer coverage, an improved condenser, and automatic loading were added at various times between 1975 and 1979.

A simplified drawing of the Micralign optics is shown on page 108. In the folded optics, light is focused through a slit onto the chrome mask for an IC. The image is reflected from one portion of the primary to the secondary mirror, back to another portion of the pri-

The 1980 Achievement Award

For their development of the projection mask aligner, the basic production tool that made possible low-cost large-scale integrated circuits, Abe Offner, David A. Markle, and Jere D. Buckley have been designated by the editors of *Electronics* as the recipients of the magazine's seventh Achievement Award. Their work at Perkin-Elmer Corp. in Norwalk, Conn., is among the landmark accomplishments of the LSI era. The system they designed performs one of the most important steps in semiconductor fabrication—the task of transferring integrated-circuit patterns directly from a mask onto wafers on a 1:1 basis. There are now more than 1,000 Micralign machines in the field.

Previous winners have been: in 1974, Gordon E. Moore, president of Intel Corp. for his overall accomplishments; in 1975, the four developers of integrated injection logic, Horst Berger and Siegfried Wiedmann of International Business Machines Corp. and Arie Slob and Cornelius Hart of Philips of the Netherlands; in 1976, Robert C. Dobkin of National Semiconductor Corp. for linear-circuit development; in 1977, Charles H. House of Hewlett-Packard Co. and B. J. Moore, president of Biomation Corp., for major instrumentation innovations; in 1978, Paul Richman, president of Standard Microsystems Corp., for advanced developments in MOS technology; and in 1979, Andrew H. Bobeck of Bell Laboratories for his role in the invention of magnetic-bubble memories.

lamps were not about to make curved ones, much to Buckley's chagrin. "We set out presuming we could buy the lamps, but we quickly learned that wasn't going to work. It certainly was a key stumbling block. We just had to roll up our sleeves and do it ourselves," he says.

Another area of some concern for the team was the viewing system. "All of us were taking a hard look at the system and trying to predict where the problem areas were," notes Markle. "One of the things that gave us some trouble in our very first system was implementing a satisfactory viewing system. We ended up putting a beam splitter surface on one of the reflecting surfaces," he comments.

Offner, as a leading optical designer at Perkin-Elmer for the past three and a half decades, had worked on a variety of optical components and systems. The annular field approach he used in the Micralign design has been the basis of all Micralign family members since the original model 100.

His recent work as principal optical scientist at the Microlithography division in Wilton, Conn., includes such things as coming up with methods for applying computers to the semiautomatic design of optical systems. His preparation included undergraduate and master's degrees in physics from Case Western Reserve University in Cleveland. Among his designs are optical systems for coherent-light data processors, including a diffraction-limited multirecord side-looking radar processor optics for reconnaissance systems, a high-resolution UV lens having a focal ratio of $f/1.5$ and a 15-μm field, and optics for astronomy.

Offner, who is 71 and nearing retirement, will proba-

mary, and then to a resist-covered wafer. As the mask moves past the slit the wafer moves in unison; thus, all the mask's patterns are exposed in one fast scan. The system employs only three reflective elements and no refracting lenses. Also, there is almost no scattered light, and image quality is enhanced while ghosts are eliminated.

At the time of the Micralign's debut, the main competition to Perkin-Elmer's reflective optics were large refractive projective lens systems, some with as many as 16 lenses. Light scattering was one of their several disadvantages. It affects image quality, limits the use of negative resists, and was never satisfactorily counteracted by antireflective coatings and standing-wave effects.

The Micralign team has continued to update, upgrade, and redesign the original model 100. The model 200, which appeared in 1978, was capable of 2-μm geometries with a ± 0.25-μm alignment error. The increased resolution was achieved by isolating the unit from vibration and the ambient temperature, as well as by improving its optics. This year, a deep ultraviolet light option, employing a 3,000-angstrom wavelength, has made it possible for the same model to attain a resolution of 1.125 μm. An automatic alignment option was also offered to Micralign purchasers for the first time.

Perkin-Elmer's machine of the future is the model 500, due out next year. An automatically aligned, broadband unit (capable of both near and deep UV exposure), it will have 1-μm resolution and a ± 0.25-μm alignment error. The hourly throughput will be 125 wafers with a 5-in. diameter. The company expects the 500 to be a basic production tool until the late 1980s.

With Perkin-Elmer also heavily involved in electron-beam and X-ray lithography, is the model 500 the end of the line for the company in optical lithography? The men of the Micralign team think not.

In October 1979, David A. Markle gave a paper at the Semicon East conference in Boston on the limits of optical lithography. In it, he predicts that conventional 1:1 projection with a high numerical aperture (NA) and short exposing wavelengths (deep UV) can achieve a practical line size of 0.775 μm. Furthermore, he predicts that with an even higher NA, an even shorter wavelength, and a better photoresist, optical lithography can be pushed to 0.5 μm. Still, Markle also notes that the limits of mask-making technology will force the 0.5-μm figure to be achieved with other than a 1:1 system—probably a step-and-repeat unit based on a scaled-up reticle. -J. L.

bly be spending much of his free time at a condominium in the Virgin Islands. Discussing what he has done with Micralign, he emphasizes the technical difficulties he enjoyed surmounting. "I've really enjoyed getting into the forefront of where the problems are," he says. "The results of a Government project aren't as satisfying. There you work on something for a year or more to prove or disprove it, and that's the end of it." Not so with Micralign—Offner has been getting feedback from many customers and using that input on future designs of Micralign products.

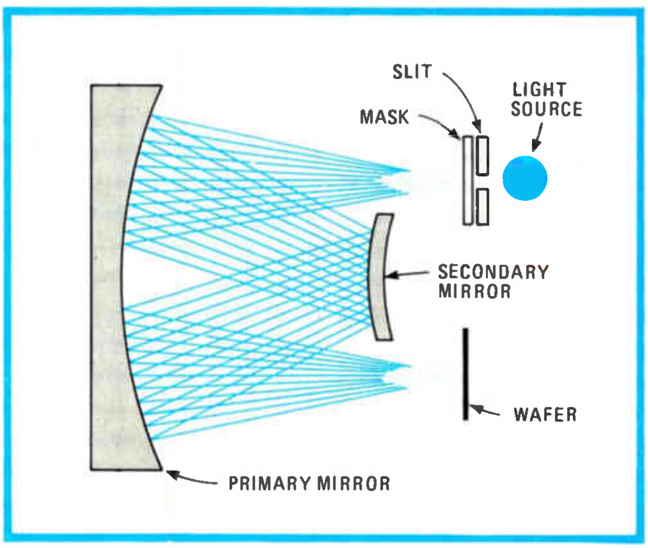
Offner was confident in handing over his innovative optics system to Buckley and Markle. "Dave's experience and his know-how are very broad," Offner says of Markle. "He can join things together very well and include optics, mechanics, and electronics in a design. It's very useful to have a person like Dave to draw an overall picture and then to know enough about all of it so that he can be critical even about the particulars," he continues.

In fact, Markle's earlier experiences at De Havilland Aircraft in Canada contributed to a large extent to his later work in optics at Perkin-Elmer. "I was studying in England and came back in 1960. In those days it was very hard to get a job in the nuclear field. I went to work for De Havilland in the infrared area, and that of course led to optics, which eventually led to Perkin-Elmer." As project manager, Markle has used many of his skills in optical design, signal processing, and thermal analysis. For the past 7½ years he has been directing the engineering and development of the projection mask alignment systems. This has included Micralign's pattern recognition and alignment system capable of 2.5-μm accuracies. He is currently director of optical lithography. A Canadian by birth, Markle, 44, now holds U. S. citizenship. He received his undergraduate degree in engineering physics from Canada's University of Alberta and his master's degree in reactor physics from the University of Birmingham in England. He also has a business degree from the London School of Economics.

"It's a little difficult to distinguish between Dave's and my participation in the Micralign project," says Buckley. "Our joint task was to take Abe's optical design and figure out how to package it." Having joined Perkin-Elmer in 1961 directly after receiving his master's degree in mechanical engineering from Cornell University, Ithaca, N. Y., Buckley was well aware what sources he could draw upon from the company as a whole when he started on the projection mask aligner design more than a decade after his arrival on the scene at the Wilton, Conn., facility.

"It was really the technical expertise we had developed as a high-technology company that was extremely helpful," he points out. "Much of what we are doing now still draws on that high-technology background in making precision optics, building sophisticated electronics, and developing complex electro-optical–mechanical systems," he adds.

Buckley, who is 43 years old, is now manager of systems engineering for standard products. In this position he is responsible for the product and systems engineering efforts associated with the Micralign program. This includes continually improving the components, the subsystems, and the total design to incorporate accessories and added features. Before the Micralign project, Buckley was the program manager for the design and fabrication of a diffraction-limited, 48-in.-aperture telescope for an aircraft application.



The optical system. The image of the master mask is produced in accurate detail by a system of convex and concave spherical mirrors arranged with centers of curvature coinciding at a single point.

Despite the major responsibility he has for the continuing success of Micralign, Buckley nevertheless finds time for his many interests—among them sailing, woodworking, and horseback riding.

All three men are quick to point out that without the support of then general manager Harold S. Hemstreet the project would have gone nowhere. "One of the keys to the success of the program was Harold, who at that time was the general manager of the Electro-optical division," says Buckley. "He was a stalwart supporter of the Micralign project in the face of less than widespread enthusiasm. I remember Harold sitting in his office and saying, 'Someday we're going to sell a thousand of these machines,' and everybody thought he was totally bananas." Hemstreet has been with Perkin-Elmer since 1959 and is currently the vice president and assistant general manager of semiconductor operations.

Offner, Markle, and Buckley are proud of the work that they have done and are pleased to note that without Micralign the U. S. semiconductor industry would not be where it is today. Their enthusiasm promises to continue into the future.

"We're a little bit unusual in that we're a true American success story," says Markle. "These days you hear all kinds of things about how the Japanese have grabbed the leadership role in automobiles, commercial products, and so on, and that they have the technical leadership. I think that in this area of semiconductor technology and processing, America's still got the leadership role. I hope we never lose it." □

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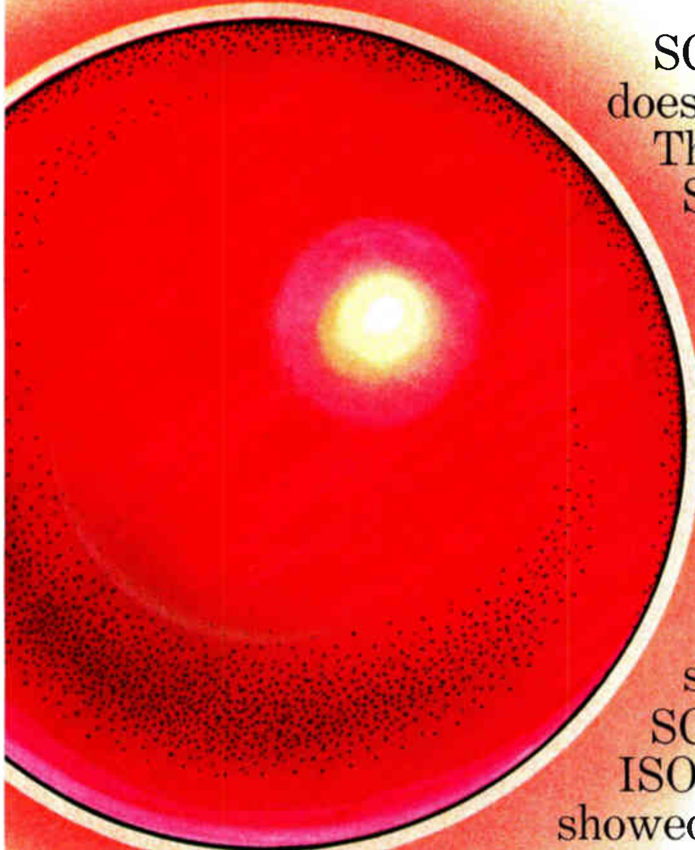

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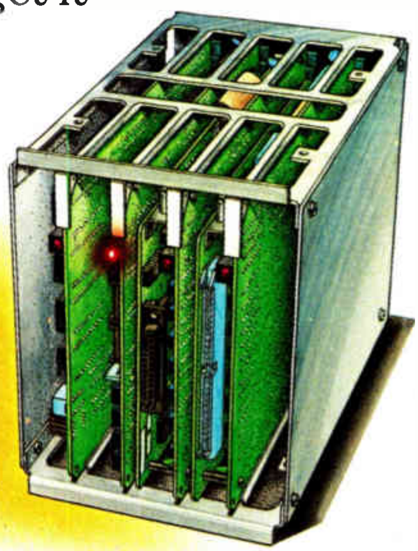

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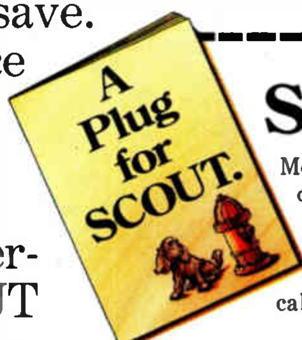

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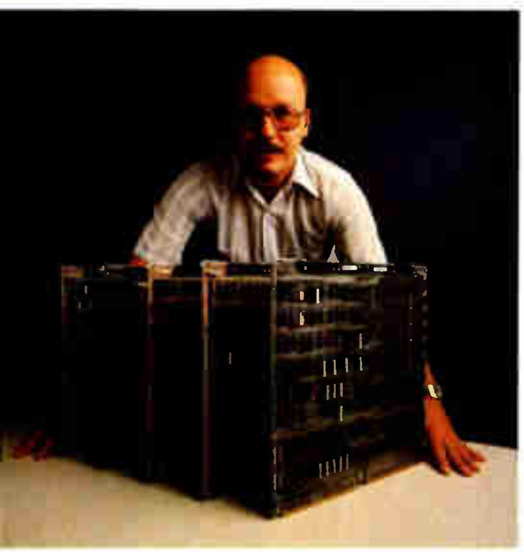
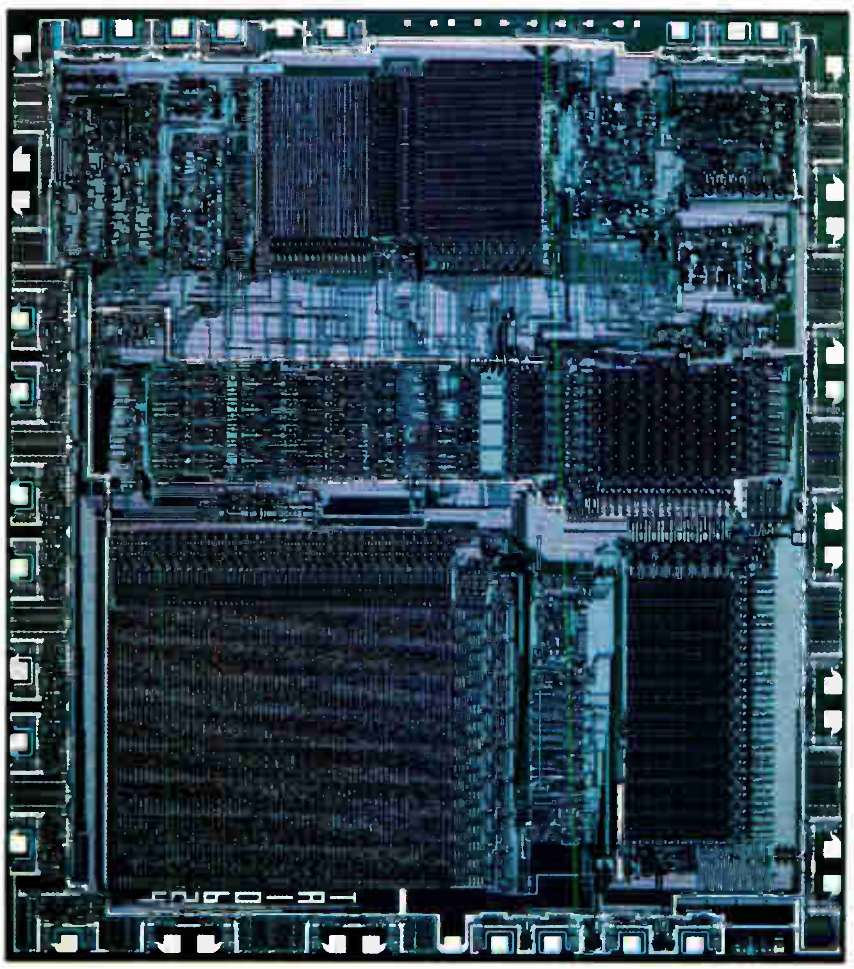
TECHNOLOGY UPDATE

The new decade is already scoring high marks for technological innovation in just about every area of electronics. Electrically erasable programmable read-only memories, for instance, are now dense enough to enable microprocessors to reprogram themselves. But the very new does not automatically triumph—the scaling down of existing MOS processes has paid off in devices with the lowest power-delay products yet attained. Meanwhile, manufacturers of 16-bit processors are showing off smart peripherals and coprocessors that will smooth the ascent to 32-bit processing. More local networks are tying together computers and peripherals. Instrument makers are automating even hand-held meters. And greater integration is upgrading mainframe computers. Clearly, the potential of the solid-state technologies is showing no signs of exhaustion.





New this year. Striving to keep things simple led Hewlett-Packard to design its 100-MHz, 1980A oscilloscope (top) with a single knob whose function is set by depressing a function key. Data General, in its first 32-bit computer, the Eclipse MV/8000 (above), fits the entire central processing unit on just five circuit boards. C-MOS is entering microcomputers like RCA's 1804 8-bit device (right) on sapphire.

SEMICONDUCTORS

Standard technologies are still cast in the leading roles as they scale down to achieve the speed and density needed for next-generation circuits, but gallium arsenide and Josephson junctions are rehearsing in the wings

by John G. Posa, *Solid State Editor,* and Roger Allan, *Components Editor*

For semiconductors, the mainstream technologies are best—that lesson continues to be driven home. Memories, with their unending need for ever greater density, have always been the proving ground for a new technology, and the recent past has shown that although charge-coupled devices and V-groove MOS may work well for image sensing and power switching, respectively, they simply will not do for general storage.

The mark of a successful technology is its ability to compete with faster or denser ones. The past has witnessed complementary-MOS put the squeeze on n-channel MOS, which now competes heavily with bipolar; bipolar, in the guise of emitter-coupled logic, can cross into the realm of gallium arsenide; and GaAs, with tiny lines and supercooling, can approach the speed of Josephson junctions—which still have no rival.

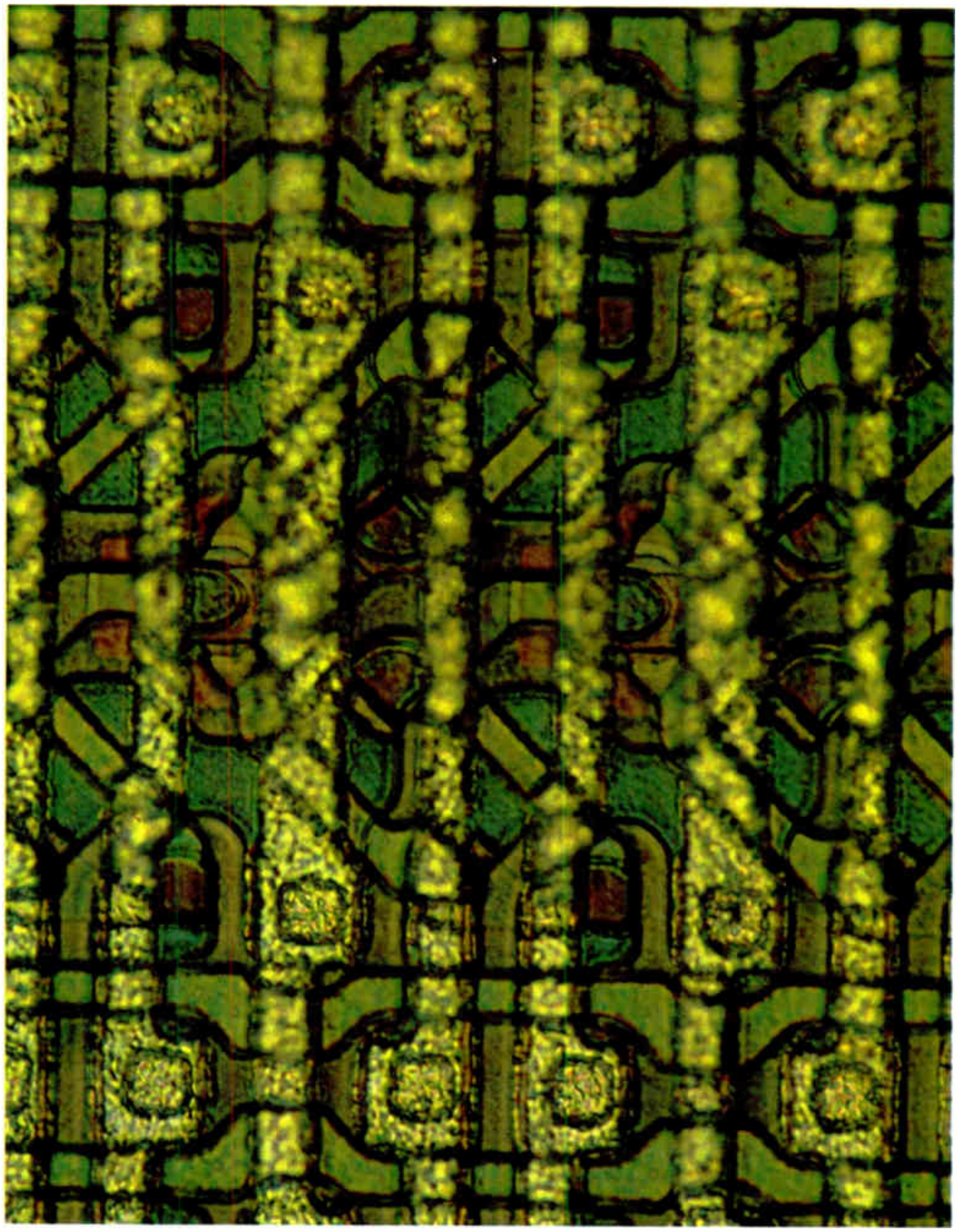
But given a winning technology, recent experience has further taught that the methods used to shrink down and speed up the transistors built with that technology must be as carefully chosen as the technology itself. For instance, it is now clear that judicious scaling down of device geometries, self-alignment, and selective oxidation for isolation pay off with low speed-power products and a process that can be gently eased into production. On the other hand, at least for the present, slapping circuits onto a sapphire substrate or melting molybdenum into polysilicon interconnections may not be the wisest moves for commercial components.

On scaling, Intel Corp. of Santa Clara, Calif., has been the teacher. Its first-generation formula for shrinking n-MOS, H-MOS—the H stands for high-performance—has been picked up, interpreted, and applied by just about every MOS maker by now. It goes by the name of X-MOS at National Semiconductor, S-MOS at Texas Instruments, and PolyPlanar at Advanced Micro Devices; but at Motorola, H-MOS is H-MOS.

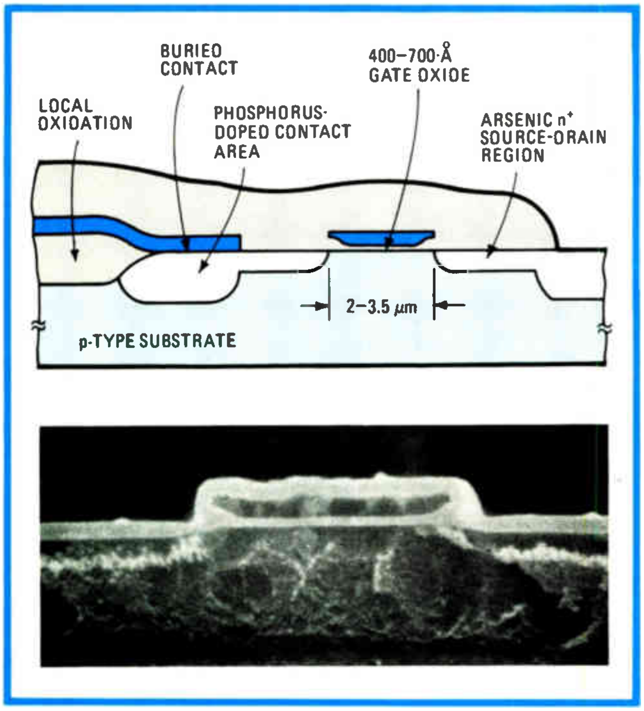
Now the competitors are turning their attention to H-MOS II, which should actually be less painful to grasp, since basically just channel lengths and gate-oxide thicknesses are trimmed down from H-MOS. Yet Intel remains the only source of H-MOS II chips. These are the 2115H and 2125H 1-K and the 2147H/48H/49H 4-K static RAMs. The 20-nanosecond maximum access time of the premium 2125H-1 and the 35-ns specification of the 2147H-1 exemplify the power of H-MOS II.

In the meantime, Intel is improving other products with high-performance MOS processing. The 16-bit 8086 microprocessor has been in H-MOS II for months, and Intel recently recast the 8048 8-bit single-chip microcomputer in H-MOS, almost doubling its 6-megahertz speed to 11 MHz. It also tapped its floating-gate process with the H-MOS wand for a variant process called H-MOS-E, which has so far turned up in a 32- and a 64-K erasable programmable read-only memory, the 2732A and the 2764, with 200-ns maximum access times—less than half that of the 16-K 2716.

The speed of H-MOS can be understood by considering its cross section. A number of factors set this process apart from older, unscaled n-MOS. One is thicker field oxides to maximize thresholds in those areas. Another is a negative substrate bias, provided on chip, to reduce



Super C-MOS. The cells in Hitachi's 6116 2-K-by-8-bit static random-access memory are powered through buried junction field-effect transistors; consequently, power-supply interconnections are not needed in the n-MOS array. Using complementary-MOS for the peripheral circuitry, the chip poses a real challenge to n-MOS technology. In this photomicrograph, taken by Mosaid Inc., 1 inch is equal to slightly more than 11 μm.



H-MOS. High-performance MOS has made n-channel technology what it is today: as fast as bipolar. The process, spearheaded by Intel Corp., is characterized by thick field oxides, on-chip substrate biasing, and channel lengths that keep growing shorter.

junction capacitances and stabilize thresholds. Deep phosphorus diffusions are used beneath contact areas, and doped polysilicon is used in lieu of the diffused regions at every opportunity in order to minimize interconnection resistances.

But of course the speed reductions of H-MOS stem from shortened channels and thinned oxides that measure about 3.5 micrometers and 700 angstroms, respectively, for H-MOS I and roughly 2.0 μm and 400 Å for H-MOS II. Delays are further minimized through nearly perfect self-alignment of the gate with the drain-source regions; the arsenic ion implants undercut the polysilicon only slightly. The sharpened edges of the gate material obtained are characteristic of the wet chemical etching used in the process.

C-MOS takes off

The same scaling principles that have given n-MOS its blinding speed are being applied to C-MOS, and with even more exciting results because of its inherently lower power drain. It has already been shown, for instance, that when the channel widths of C-MOS are reduced to H-MOS II's 2 μm, operating frequencies as high as 500 MHz are possible.

Besides Hitachi and Mitel, which are to C-MOS what Intel has been to n-MOS, American Microsystems, Harris Semiconductor, Hughes Aircraft, Intersil, Mostek, Motorola, National Semiconductor, Nippon Electric, RCA, Rockwell International, and Toshiba all have advanced C-MOS programs. Even Intel has developed a C-MOS process—to be described next year—that will accommodate H-MOS-like feature reductions.

High-performance C-MOS is arrived at in much the same way that H-MOS is: through self-aligned polysilicon gates and scaled geometries. With its n- and p-channel devices, C-MOS may seem more difficult to scale down, but that turns out not to be the case. The enhancement- and depletion-mode devices of n-MOS are laid out differently, so that when features are reduced, depletion devices get smaller widths but the enhancement devices wind up with shorter lengths. In contrast, the n- and p-type devices of C-MOS are scaled down proportionately, so that there are fewer process control problems like short-channel effects.

A related problem with n-MOS is that it is difficult to maintain a balance between the ability to pull up and pull down a transistor as it is scaled. This ratioing problem, as it is called, has not appeared in Hi-C-MOS (to use Hitachi's label). However, it should be pointed out that Hi-C-MOS does not afford the same flexibility of substrate biasing. Current work indicates that it is not impossible to achieve that flexibility, but that it is not trivial, either.

Well, well, well

In traditional bulk C-MOS processes, lightly doped p-type wells are diffused or implanted, and n-channel transistors are formed within them. Thus it is possible to form a well for each n-MOS transistor (the isolated well approach) or one large well for many (the ubiquitous well approach). Exhibiting higher speed and packing density, the ubiquitous well has become the dominant structure for C-MOS. But, of course, an isolated well can always be used if the layout dictates.

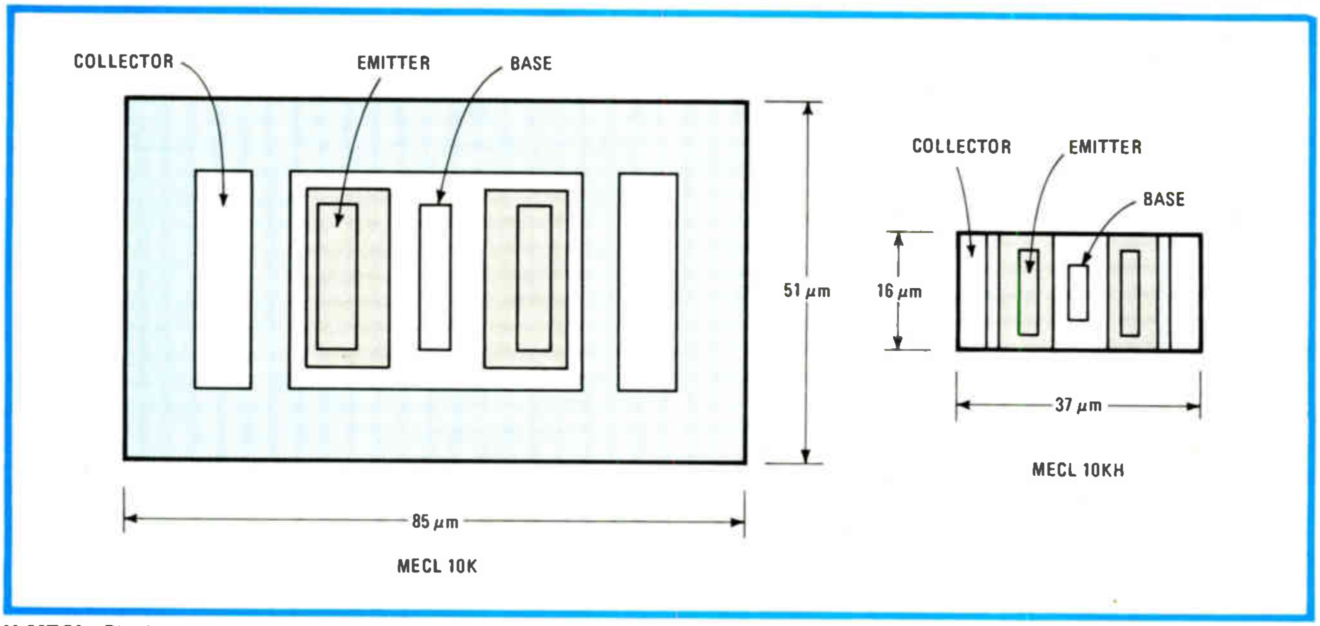
The Japanese in particular have been switching from p- to n-type wells. Matsushita Electric Industrial Co. certainly uses them, Toshiba Corp. is thought to be doing so, and Hitachi says it is. The impetus for the switch is simple. Memory-intensive chips dictate n-channel devices for their speed. It is therefore easier to start with a p-type substrate, using the n wells only for the fewer p-type devices. "It's C-MOS from an n-channel guy's point of view," comments Donald L. Wollesen, C-MOS research and development manager for American Microsystems Inc., Santa Clara.

But Wollesen does not think that n wells are here to stay. One reason is that the reverse-biased junction between p-type wells and the n-type substrate sweeps away superfluous carriers generated by alpha particles. N-type wells forfeit that key benefit.

However, a more recent idea is to diffuse both well types into a very lightly doped or intrinsic substrate so that both device types can be optimized independently. Bell Laboratories in Murray Hill, N. J., has done work in this area and has come up with a process called twin-tub C-MOS that requires only eight mask steps.

Some designers believe that the higher-resistance substrate possible with dual wells also helps to subdue C-MOS's latchup problem. This problem, which is also under scrutiny, stems from the parasitic pnpn structures in C-MOS that act as silicon controlled rectifiers under certain conditions such as an input higher in potential than the supply.

In addition to scaling down for speed, C-MOS is exploiting polysilicon for density in the same ways that



H-MECL. Bipolar processes like Motorola's emitter-coupled logic are also undergoing scaling so as to boost performance. With walled emitters and oxide isolation, the company's new 10KH family cuts propagation delays by 50% with no increase in power consumption.

H-MOS does. National, Harris, and Mitel, for instance, have already conquered double-level polysilicon C-MOS, and others have that goal in their sights. There are two ways to make use of the two polysilicon levels. One is to use both levels for gates—which is what has to be done for CCDs. The other—the route chosen by n-MOS and now C-MOS manufacturers—is to use the second level for interconnection and load resistors but not for transistors.

Back to basics

Clearly, double-level polysilicon can be beneficial to memory devices. Intel uses the upper level for load resistors and interconnections in its 2167 16-K static RAM. But two-level polysilicon is particularly advantageous to nonmemory elements such as microprocessors, where on-chip wiring of the random logic is becoming such a dominant factor.

Already, the fruits of double-polysilicon C-MOS can be seen. National Semiconductor Corp.'s P^2C-MOS process has resulted in the NSC 800 microprocessor, a blend of Intel's 8085 family architecture with the instruction set of Zilog's Z80. The Santa Clara firm expects to follow the 800 with a C-MOS version of the 8048 single-chip microcomputer and ultimately a 16-bit machine.

Harris Corp.'s Semiconductor Products division, Melbourne, Fla., will use its self-aligned junction-isolated—or SAJI—C-MOS process, upgraded with oxide isolation and double polysilicon, to improve its 6100 microprocessor, as well as to make its own version of the 8048 (and the 8748, an 8048 that contains erasable programmable read-only memory) and later, a C-MOS 8086 16-bit microprocessor. Similarly, Mitel Semiconductor Inc., in Kanata, Ottawa, Ontario, plans an oxide-isolated C-MOS, or Iso-CMOS, rendition of Motorola's 6802 (long overdue, thanks to latchup problems) and, rumor has it, the 16-bit 68000. In each of these cases, channel lengths have yet to be scaled down to H-MOS-like dimensions, but that is certainly coming.

Hitachi's 4-K and 16-K Hi-C-MOS static RAMs use polysilicon loads, but, again, the actual memory arrays in these devices are n-type. Interestingly, Hitachi did not resort to a second polysilicon level to accommodate the pull-up devices; it just made them very small, masking them with nitride while doping the remaining exposed polysilicon for interconnections.

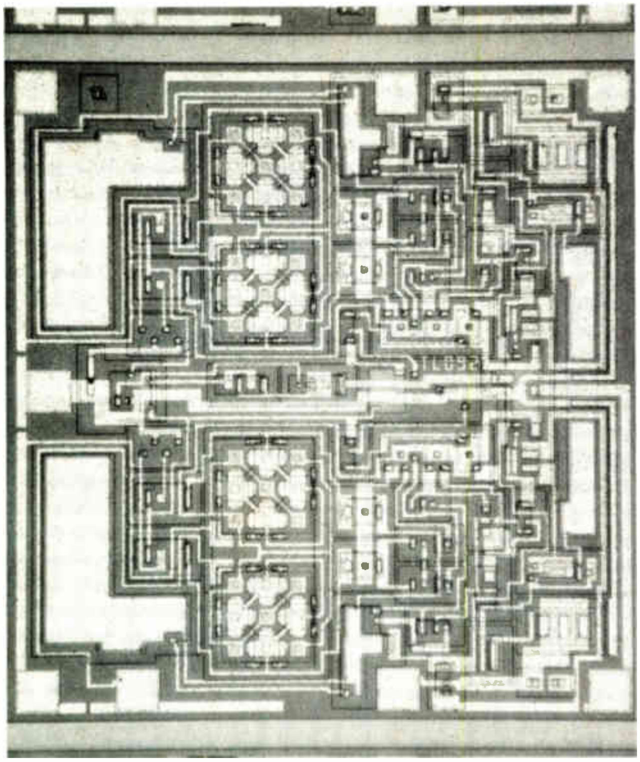
Since even in C-MOS, the load devices pull up n-channel transistors, polysilicon resistors are not inherently more difficult to define or scale down. However, the expectation is that C-MOS is going to have a lower standby power than n-MOS, so that their resistance has to be a lot higher. But resistance for a given area can be made even higher than if the polysilicon were left intrinsic, or undoped. That is because with very high-value resistances, current flow is dependent on things like trapping centers and grain size. To adjust these parameters, the entire time-temperature relationship of polysilicon must be well understood.

Better insulation

Increasingly, oxide isolation is being used for MOS and bipolar structures to cut leakage and boost speed. In bipolar processes such as Fairchild's Isoplanar, wells are etched between device sites and filled with oxide to retain a flat, or planar, surface. Another method, which the Japanese have employed, involves etching V grooves and oxidizing them.

Advanced Micro Devices Inc., Sunnyvale, Calif., is improving an Isoplanar-like process called IMOX—for implanted micro-oxide—that it is using to build 1-K RAMs, 8-K PROMs, and its new Am29116 16-bit microprocessor. Like Fairchild, AMD will scale down geometries for higher-density parts.

In bipolar technologies, if the oxide isolation extends through the epitaxial layer and into the substrate, the devices are truly isolated, because it is almost impossible for current to flow through the already present



N-FET op amp. Until now, FET-input operational amplifiers had to use p-channel devices. As a result, they could not achieve true single-supply operation. But using deep ion implants, Texas Instruments has devised the n-channel FET op amp shown above.

reversed-biased junction and then underneath the oxide. However, in MOS devices, the degree of isolation is variable and related to the depth of the oxide, since an epitaxial layer is generally not present.

Other materials

Work is also progressing on insulating substrates and on lower-resistance interconnections. The expense of sapphire as a starting material continues to limit silicon on sapphire to military and specialty applications. Texas Instruments and others have been getting promising results with laser-annealed polysilicon on silicon dioxide, however. This material may unlock the door to a low-cost insulating substrate and even three-dimensional structures, since the laser-annealed polysilicon may be oxidized, covered with polysilicon, and annealed for another level of circuitry.

The Japanese have not been afraid to admit that they use refractory metal silicides to speed up their polysilicon interconnections. The most popular metal seems to be molybdenum, which as molybdenum silicide ($MoSi_2$) has a sheet resistance of 5 ohms per square, compared with polysilicon's 40 Ω/sq. A commercial device with metal silicide gates has yet to be announced, but that could happen as early as next year. The most likely candidates are high-speed static RAMs.

Although insulating substrates would be useful only for MOS wafers, refractory metal interconnections may one day aid bipolar chips, for these, too, are using polysilicon in increasing numbers. Philips Technology Research Laboratories, Eindhoven, the Netherlands, for example, is using polysilicon films for resistors, diodes, and even transistors in its bipolar circuits.

Fairchild Camera and Instrument Corp. believes that the highest speeds will come with the all-active loads that it has planned for its Isoplanar-S technology. These loads, which will be pnp transistors, will require the use of pnp and npn transistors on the same die for a C-MOS-like bipolar equivalent. Fairchild says that the pnp loads will be employed to limit power consumption rather than die area. Without these, the Mountain View, Calif., firm says, it would be forced to add a power-down mode to large-capacity memories, just as the MOS memory makers have been doing. The first part to exploit the improved cell structure will be the 10480/100480 16-K-by-1-bit ECL RAMs.

ECL leads

As far as the development of bipolar technology is concerned, the interest has clearly been with ECL. Bipolar TTL-compatible memory and logic circuits, even if they contain ECL on the inside, are finding it increasingly difficult to compete with H-MOS and Hi-C-MOS in terms of speed and power. Even the new advanced Schottky TTL processes have been restricted to small- and medium-scale logic families like Fairchild's FAST, National's LS^2, and TI's AS and ALS series. MOS is competing even here; Mitel recently launched a series of Iso-CMOS byte-wide interface circuits that match the performance of low-power Schottky.

Heightened ECL activity can be felt around the world. In Europe, companies like RTC and Siemens are very strong; and in Japan, Fujitsu, Hitachi, and Nippon Electric are using fine-line lithography for gate delays below 5 ns in some cases. In the U. S., in addition to Fairchild and AMD, National, Motorola, and Signetics are scaling down device dimensions for more performance.

One example is the new 10KH series from Motorola Semiconductor Group, Phoenix, Ariz., which uses an oxide-isolated process called Mosaic—for Motorola self-aligned implanted circuit—to cut propagation delays in half over older, junction-isolated MECL families. This is done without increasing power.

Bipolar variations

Like TTL, integrated injection logic is having a difficult go of it as a mainstream technology. One reason is a lack of standard I^2L structures and many splinter fabrication processes with slightly different logic swings or drive requirements. I^2L does offer excellent packing density for a bipolar process, however, making it attractive for products like gate arrays. One of bipolar's advantages is that I^2L, standard bipolar transistors, ECL, and other bipolar technologies can usually be mixed on the same chip. Analog and digital functions can thus be combined for very versatile circuits. Indeed, with enough processing steps, speed, power, and operating voltage can be adjusted for just about any application.

One example of merged technologies for a specific application is the 8-bit AD558 DacPort digital-to-analog converter from Analog Devices Inc., Norwood, Mass. Its data latches are made with I^2L, and the bipolar voltage reference and control amplifier are combined thanks to

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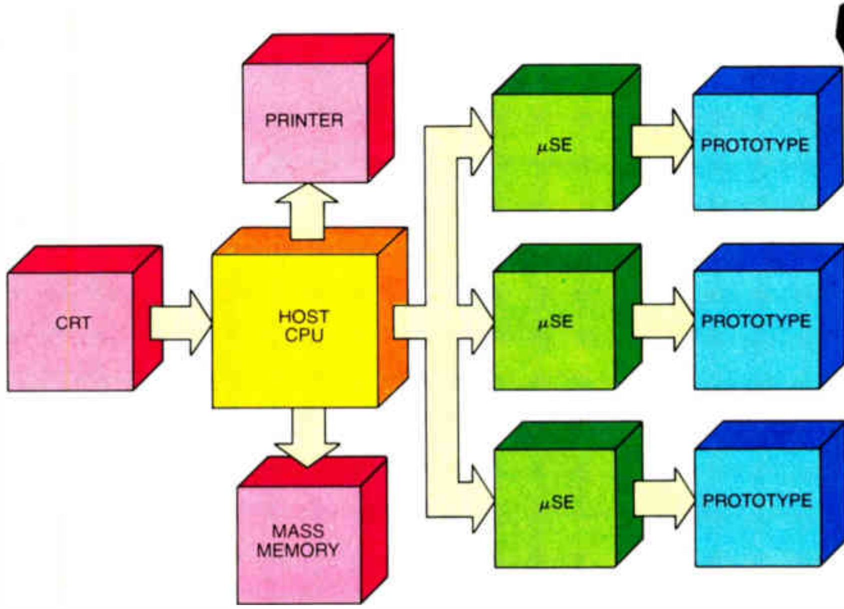

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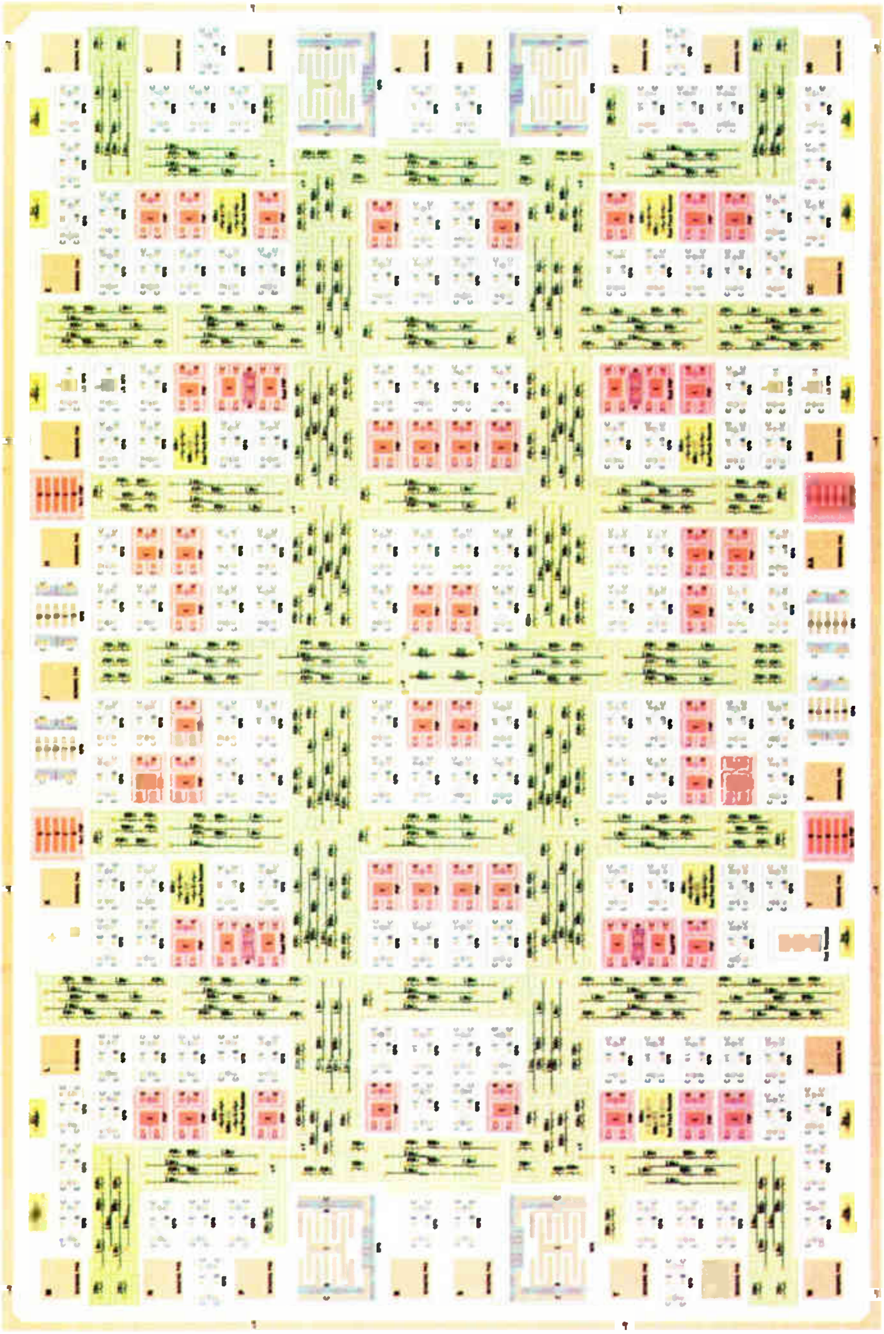

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low noise: 4	quad collector: 8	200 ohms: 60
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large: 4		900 ohms: 140
		1.8k ohms: 104
		3.6k ohms: 84
		60K ohms: 16 (pinch resistors)

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clever circuit design. In contrast to most monolithic d-a converters, which use npn transistors common to a bipolar process, the 558 uses lateral pnp transistors because they are more suitable for single-voltage operation.

Not again

As if MOS were not applying enough heat to bipolar technology along memory and digital logic lines, it is also making impressive gains in data acquisition and power control as well. C-MOS op amps are proving their worth with exciting new designs like the ICL7650 from Intersil Inc., Cupertino, Calif. The chopper-stabilized unit has a low input offset drift of just 1 microvolt/°C over the amplifier's entire operating temperature range of −55° to +125°C. Using principles similar to the firm's famous commutating auto-zero, or CAZ, amp, the 7650 does not sacrifice bandwidth for stability, as most chopper-stabilized amplifiers do: its gain-bandwidth product is 2 MHz.

Even if the inputs do not have insulated gates, junction field-effect transistors are enhancing the specifications of the latest op amps. One of the most notable advances hails from Texas Instruments Inc., Dallas, with the introduction of the first n-channel FET-input op amps. Processing innovations involving high-energy ion implantation overcame the usual contamination and noise problems that have held back the development of this type of device (conventional FET-input op amps use p-channel devices). The new units can be operated from a single negative or positive collector supply, referred to ground, whereas p-channel FET-input op amps require two power supply lines, both referred to ground.

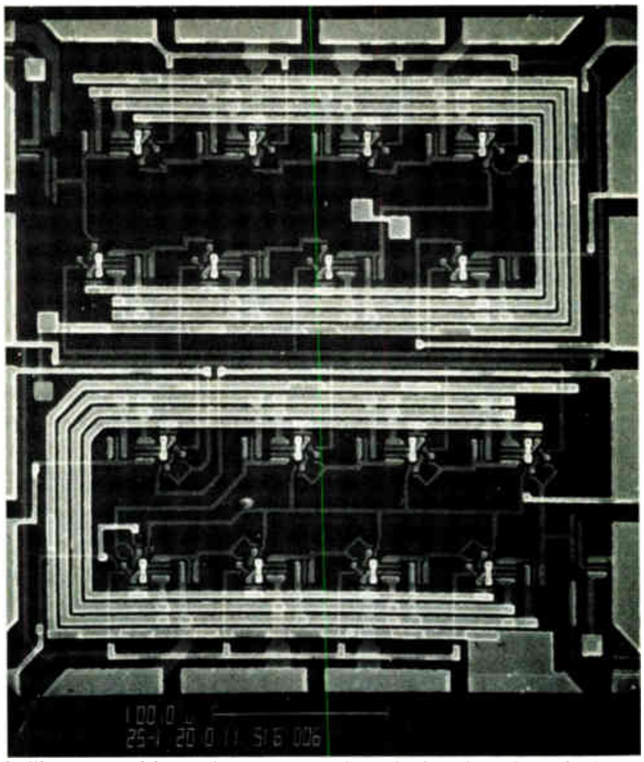
Earlier this year, the redoubtable Robert Widlar, now a consultant, designed a new bipolar op amp for National Semiconductor that challenges FET-input bipolar op amps in low input bias current, a traditional strong point of the latter. Widlar's op amp, the LM-11, features 100 μV of offset voltage, 1 μV/°C of drift, and only 20 picoamperes of input bias current.

Ever since it was discovered that the MOS field-effect transistor was an excellent candidate for high power switching just a few years back, the power transistor field has not been the same. Power MOS FETs have been relentlessly advancing in performance on all fronts and are seriously contending for sockets occupied by familiar bipolar power transistors.

Optimizing power FETs

Now a host of power MOS FET structures has arisen (for example, V-MOS, V-FET, Hexfet, T-MOS, D-MOS, Z-MOS), each with its own strong and weak points, but all offering such competitive advantages over bipolar power transistors as higher input impedances, lower drive requirements, faster switching speeds, and greater power-handling capabilities. International Rectifier Corp., El Segundo, Calif., first began drawing attention to the MOS FET with its unique hexagon-like MOS FET structures known as Hexfets. The latest geometric entries are Motorola's T-MOS and Intersil's Z-MOS, both with lower on-resistances than previous-generation devices.

Despite the years of refinement and the millions of dollars that have been pumped into silicon-based integrated circuitry, the higher speed possible with gallium arsenide logic and the Josephson junction still haunts researchers. Neither of these approaches will overtake silicon overnight. But it is no longer correct to consider either as merely a laboratory curiosity, thanks to swelling investments and expanding participation by a growing number of companies.



Gallium arsenide. With a carrier mobility higher than that of silicon, GaAs logic is leaving the lab. This parallel multiplier was fabricated by Rockwell International. Very recently, the company reported a 1,008-gate 8-by-8-bit multiplier that produces a product in 5.3 ns.

GaAs for logic

Discrete GaAs components have been around for years, but now fairly dense logic chips are surfacing. Attempts to integrate GaAs have so far resulted in depletion-mode FET logic (also called buffered-FET logic); Schottky-diode FET logic (SDFL); and enhancement-mode, or direct-coupled, FET logic (DCFL). Metal-semiconductor, or MES, FETs have been built using each approach, but DCFL has also been used to fabricate junction, heterojunction, and MOS FETs.

However, it is the depletion-mode processes—buffered-FET logic and SDFL—that have been yielding the highest densities. At Rockwell International Corp.'s Electronics Research Center in Thousand Oaks, Calif., Richard Eden and his colleagues recently reported a 1,008-gate 8-by-8-bit parallel multiplier that can yield a product in 5.3 ns. That is about 10 times faster than bipolar for this application.

Hewlett-Packard, Lockheed's Microelectronics Center, TRW's Defense and Space Systems Group, Hughes Aircraft, Thomson-CSF, and Fujitsu all have been investigating the prospects for GaAs ICs. Recently, components suppliers like Motorola and Texas Instruments have also been beefing up their efforts. Using ion implants, TI is building bipolar integrated circuits. So far, it has fabricated a 15-stage ring oscillator. In the meantime, Fujitsu is said to be building a supercomputer based on GaAs that will leapfrog the industry.

Keeping it cool

From the papers given by International Business Machines Corp., one gets the impression that it, too, is soon to release a supercomputer, but based on Josephson junctions. The firm says that it can build logic elements and memories and that it understands the packaging problems; still, no computer has yet emerged. Recently, however, it did describe a complete signal processor built from the technology, but it did not hesitate to point out that the project was experimental only.

For the longest time, IBM has been the prime mover for Josephson technology, but recently its interest has been shared somewhat by the Japanese. Earlier this year, the computer giant's Thomas J. Watson Research Center in Yorktown Heights, N. Y., reported the formation of ultrathin nanobridges made of niobium. These might allow junctionless switching. More recently, the same center announced Josephson ROMs for the first time. In fact, two cell types have been invented, one of which can be reprogrammed.

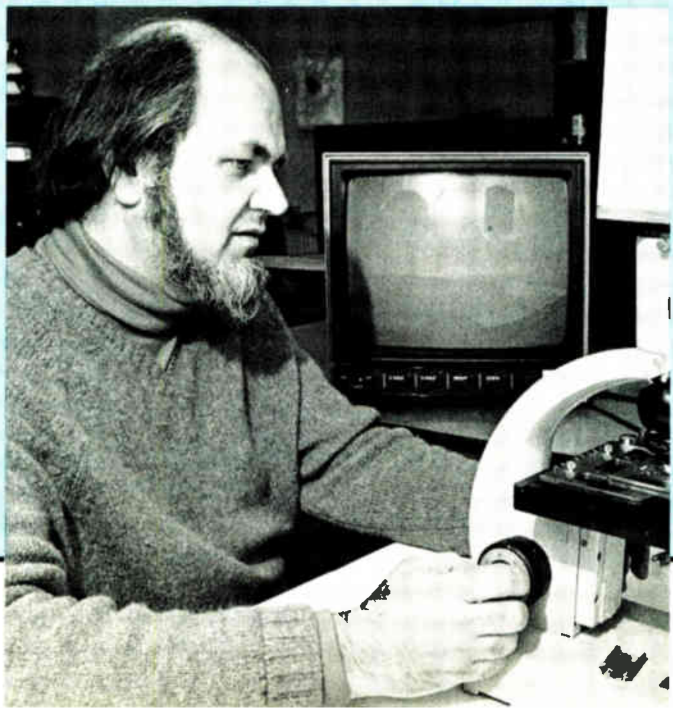
Josephson junctions are being used for demanding measurement equipment, but their role in the computer industry remains to be seen. The power-delay products achievable with Josephson logic are unbeatable, but ultralarge-scale integration must be used to circumvent delays through wiring. What's more, the packaging difficulties involved with near-absolute zero temperatures will not be overcome easily, either.

Foss: investigator of MOS circuitry

A firm can make claims about its semiconductor circuit, but it had better beware: the design might be scrutinized by the watchful eye of Mosaid Inc. For over five years, president Richard Foss and his confreres have been tearing apart memories and other MOS chips and issuing reports on what makes them tick. Although Mosaid is only six engineers and four in supporting staff, in the MOS business Dick Foss and Mosaid are household words.

Half of those who buy the reports are "users who want to know what's inside those cans and the other half are semi houses who want to know what the competition is up to," says Foss, 44 years old and born in Britain. Mosaid has dissected "every dynamic RAM in the last five years, quite a few of the static RAMs, and odds and ends like some CCD memories and one ROM from Mostek, for a total of about 30 or 40." Another of Mosaid's silicon surgeons, John Roberts, has come to specialize in complementary-MOS. Right now he is opening up Hitachi's 2-K-by-8-bit static random-access memory.

But the reports are only one of Mosaid's services. Using circuit expertise accrued over the years, the Ottawa, Ontario, firm will reverse-engineer an existing product or design one from scratch. In addition to three 4-K RAMs, "we've done four 4116 equivalents, we did one 64-K, and right now we're doing a 5-volt 16-K–64-K combined job." Most of the actual design work is handled by Robert Harland, a co-worker at Mosaid. "Bob is infinitely the better designer," admits Foss, "but I describe what it all means." Mosaid also offers a computer-aided design system, and it is soon to unveil a bench tester for RAMs.



Foss entered the semiconductor business in 1964 with Plessey Co. in England. He designed its first operational amplifiers and eventually became marketing manager of the Microelectronics division before falling out with the company in 1970.

He was caught on the rebound by the now defunct Microsystems International Ltd., or MIL, in Ottawa to set up their technical operations in Brussels. Foss traveled to Canada for six weeks, "only to discover all those things I was supposed to bring back to Brussels didn't exist." But he fell in love with Ottawa and stayed there even after MIL's parent company, Northern Electric Co., shut it down in 1975. Foss was beating the streets again with Harland, whom he had pirated away from Plessey.

Just before its closure, Harland had designed a 4-K RAM for MIL, and Foss went around "explaining how our part differed from TI's, only to find that people were more interested in the Texas Instruments schematic because they'd never seen it." So Foss and Harland concluded that "if we did a half-decent job of analyzing other people's parts—publishing the schematics, preferably with a few comments on them—there would be a business there."

Foss gets a "glow of satisfaction" to see other manufacturers adopt Mosaid's circuit techniques and reporting style. "We have tended to be the bears in this industry. We'll say, 'You're wet. You're not going to get it out on this time scale.' "

Foss received his Ph.D. in electrical engineering at Newcastle University in England, which changed its name from Durham during his residency there. He also married at school and now has two girls and two boys. He caught the older boy doing his homework on the Apple computer the other day, and that, he reports, was "not half-encouraging." **-John G. Posa**

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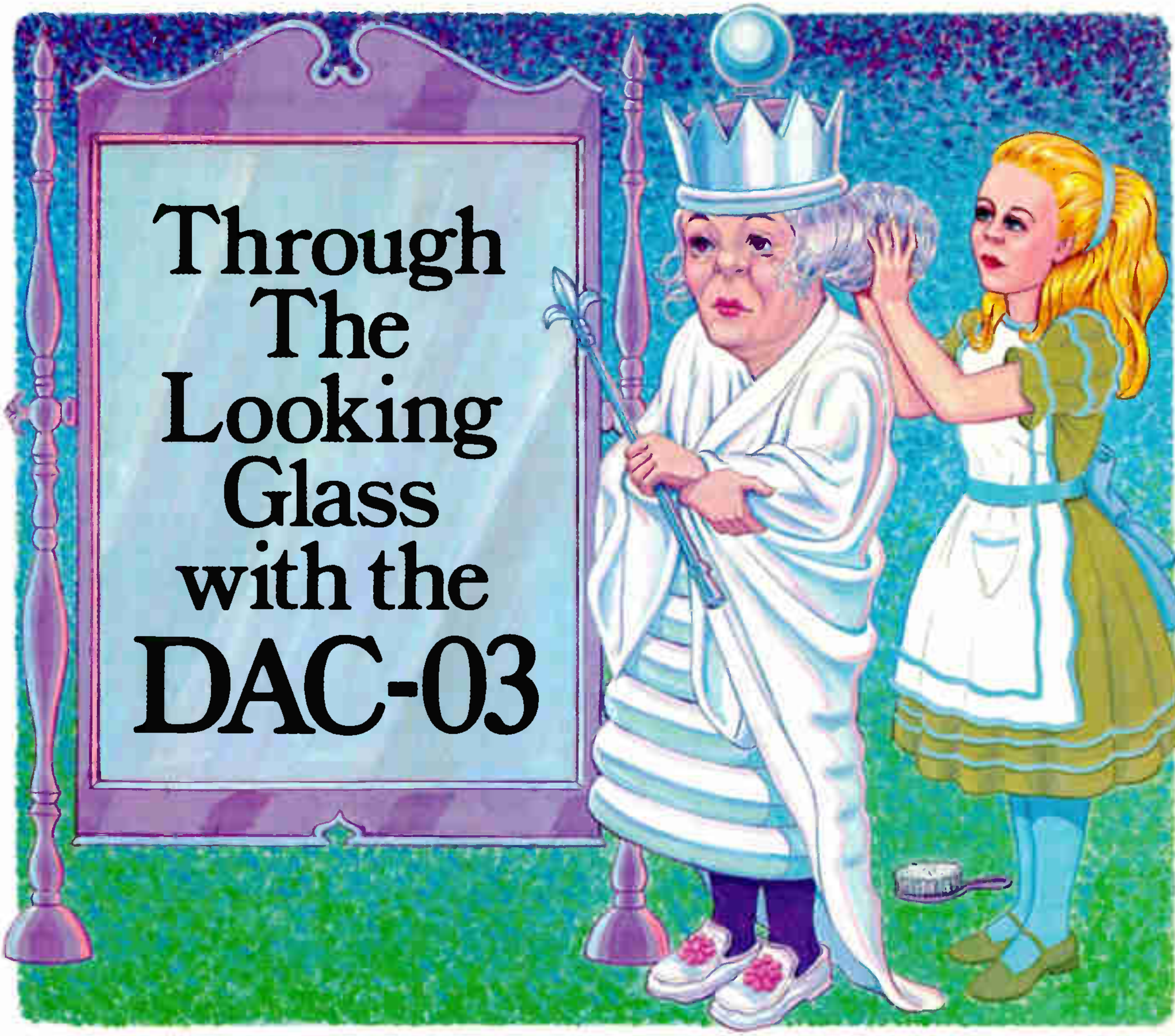


In *Through the Looking Glass*, Lewis Carroll introduced Alice to a mirror-image world where things were never what they seemed. In fact, they were just the reverse of what they should be. Punishment came before the crime; answers came before the questions.

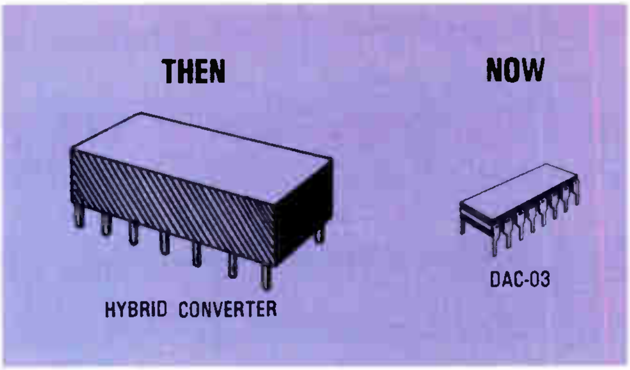
Linear Wonderland is like that sometimes, too. Salesmen spend their commissions before the purchase orders are signed. Marketing departments announce products before engineering develops them.

And at PMI, we try to develop products before anyone else realizes they're needed. We know that in Linear Wonderland, the best products create their own need.

That was how we developed the first truly monolithic D/A converter, the 6-bit DAC-01. At the time, no one thought they needed it because they were "making do" with modules or in-house designs with separate op amps and voltage references. When the DAC-01 (and the 10-bit DAC-02) came along and offered high performance specs with monolithic reliability, a lot of people suddenly found this was *just* what they needed.

PMI has another product we think a lot of engineers need: The DAC-03, a *low cost* 10-bit converter. Like the 10-bit DAC-02, it includes all the elements of a complete DAC on a single chip: precision voltage reference, current steering logic, current sources, diffused resistor ladder network, and high speed internally compensated output op amp. The DAC-03's 25°C tested and guaranteed performance and its low, low price are just what the systems engineer ordered.

The people who haven't needed the DAC-03 (until now) are all those designers who looked at our DAC-02 and decided that their system didn't justify the higher cost of wide temperature range testing.



So they turned instead to in-house designs they could build with low-cost components, or to modules and hybrids which gave them the 25℃ performance they wanted, but cost dearly in terms of space and power.

Was PMI going to let them go on forever making those trade-offs?

And will those same engineers go on using oversized $50 modules with a 1-watt power requirement and a speed of 5 μsec when they can get a DAC-03 in a DIP package which requires only 350mW, settles within 1.5 μsec to ½ LSB for a 10V step and costs as little as $7.95?

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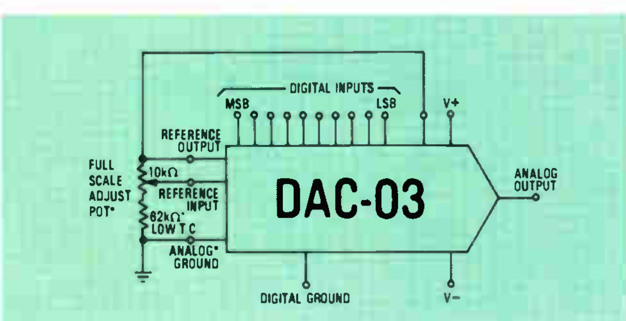
"Contrariwise! If it was so, it might be; and if it were so, it would be; but as it isn't, it ain't. That's logic!"



Logic could also convince you to be one of the first to stop not needing the DAC-03. You'll quickly develop a need for the DAC-03's guaranteed monotonic performance in four non-linearity grades. We believe you'll need not only the DAC-03's speed and miserly power consumption, but also its ability to use a wide range of power sources, from ±12V to ±18V. And knowing that it's available in either + 5V or + 10V output range versions allows you to develop a need for either. Or both.

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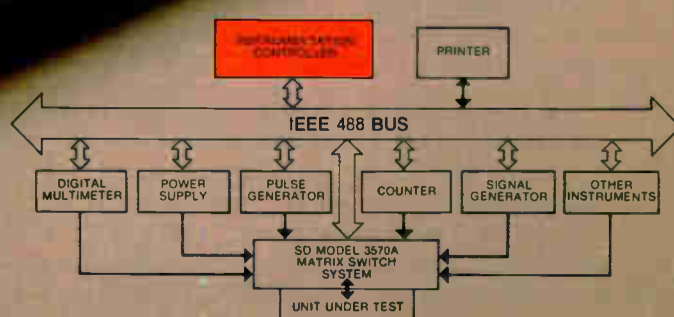

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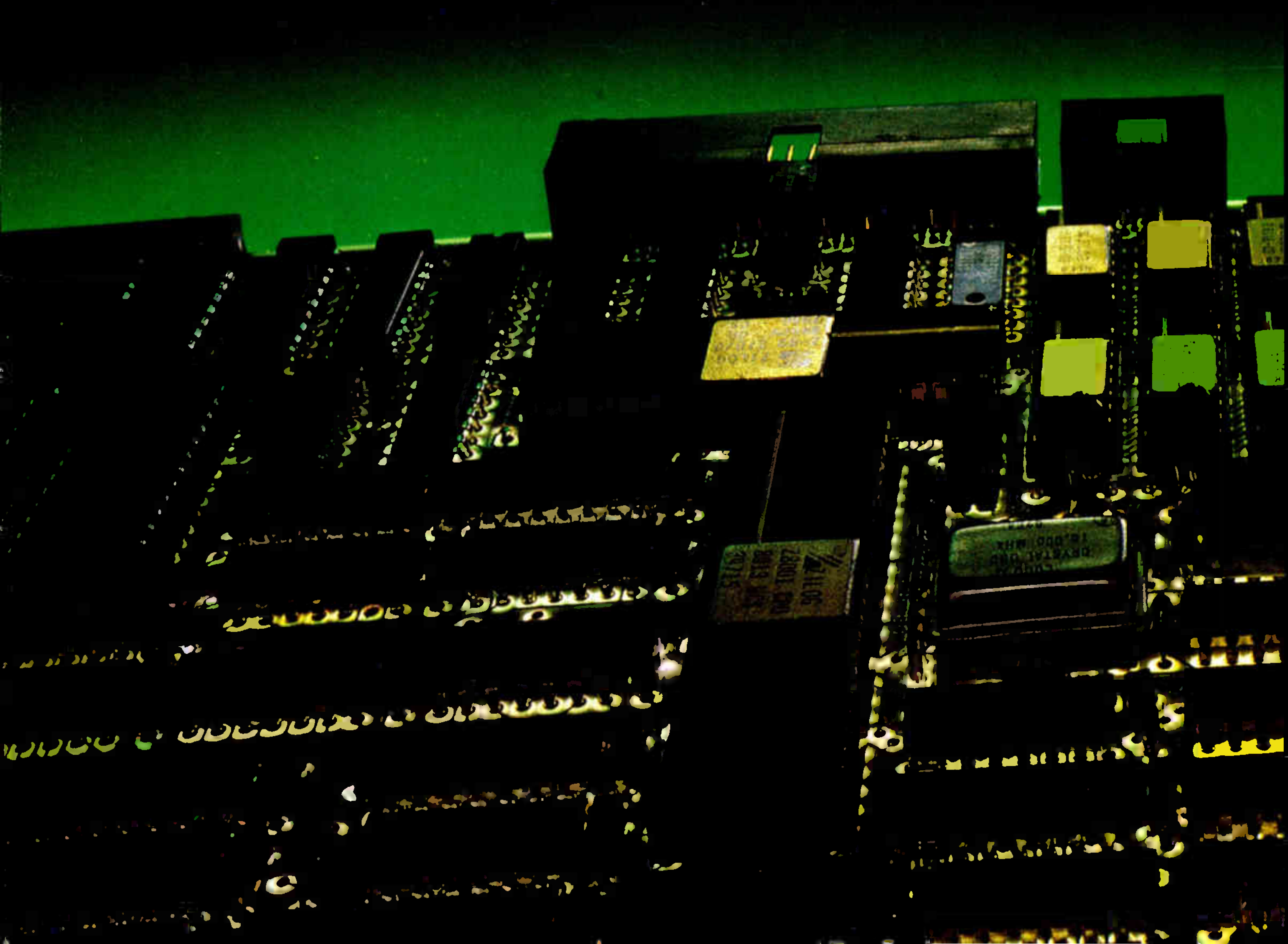


MEMORIES

Alpha particles and other obstacles notwithstanding, memories of all types continue to grow in speed and density; particularly noteworthy are the imminence of 64-K dynamic random-access memories and the existence of electrically erasable PROMs

by John G. Posa, *Solid State Editor*

Each new generation of memories brings with it untold engineering and manufacturing complexity. Density no longer doubles each year—as Gordon Moore, chairman of Intel Corp., once predicted—but design effort, equipment cost, and production intricacy surely seem to.

But if Moore's law is broken, memory designers continue to grapple with Murphy's law, which asserts that if something can go awry, it will. But they are meeting the challenge. Despite all of the technological obstacles that 64-K dynamic random-access memories present, tidings of the 256-K and 1-megabit chips can be heard. And tough as it is to get 4-K MOS static RAMs to access in 55 nanoseconds, parts with four times the density are matching that specification—even complementary-MOS memories.

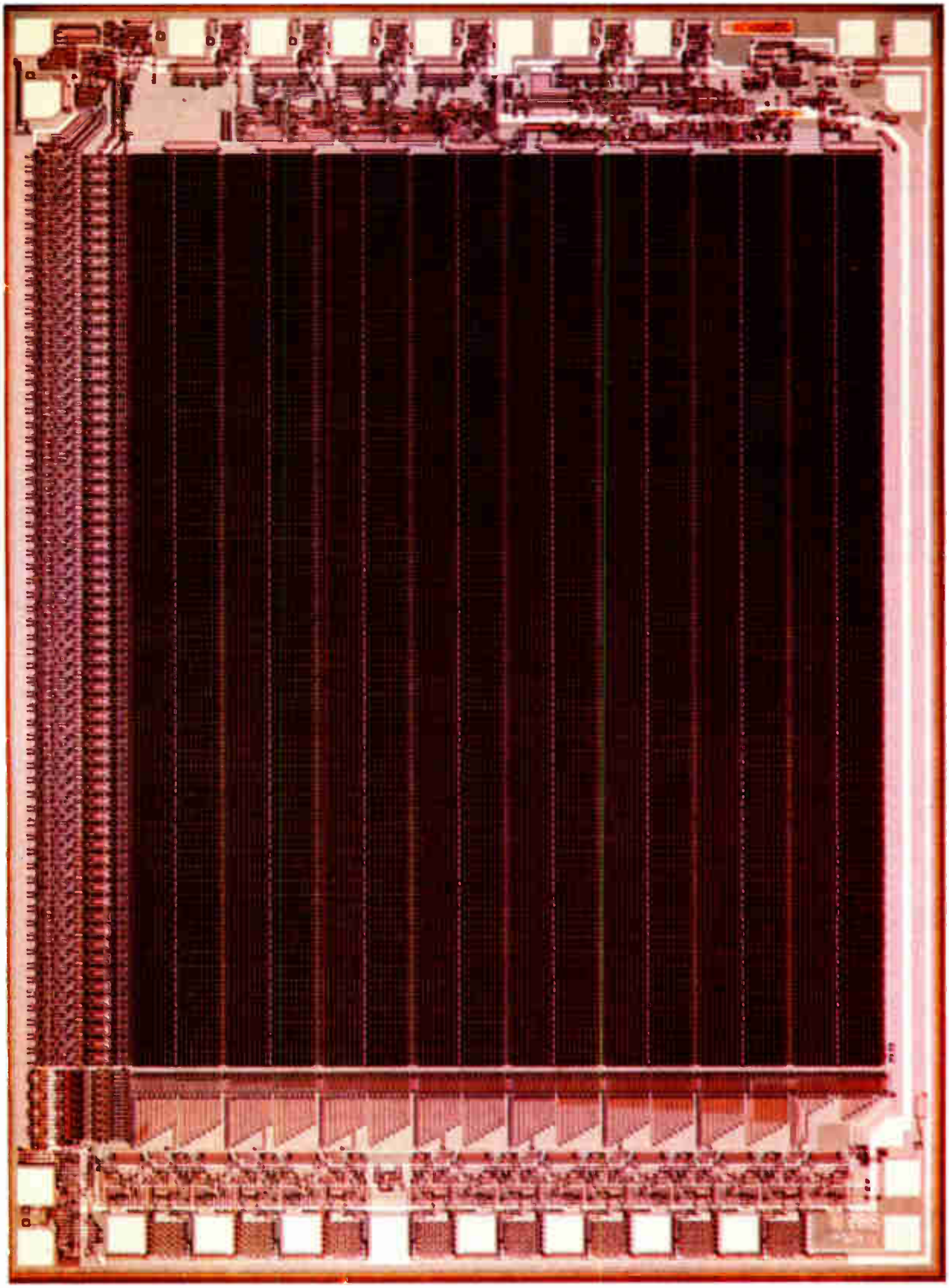
Next year will see 256-K read-only memories and 35-ns 16-K bipolar fuse-link programmable ROMs; 64-K ultraviolet-light–erasable PROMs will be produced in volume by a half-dozen manufacturers; and electrically erasable PROMs and bubble memories, having achieved respectable respective capacities of 16-K and 1 Mb, will finally usher in the wealth of new applications they have long promised.

Not without pain, MOS dynamic random-access memories have reached the 64-K threshold. Still, of the parts so far promised by 11 U. S., 5 Japanese, and 2 European companies, only one is actually on distributors' shelves, the bulk are at the design or sampling stages, and the rest are still dreams. No design has yet received the endorsement of a mainframe computer maker, but half a dozen or so are in the process of being qualified.

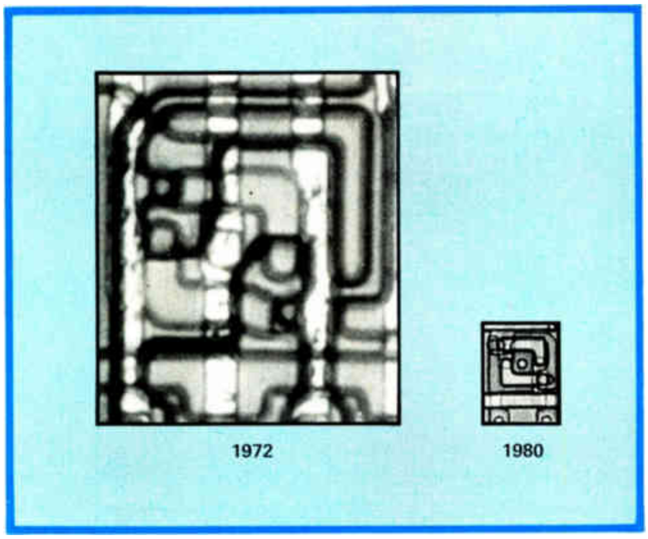
Not the simple extension of 16-K technology it was expected to be, the 64-K device turned out to be monstrously hard to build. The problem was not fashioning a cell less than 200 square micrometers in area but sheltering it from external noise. All 65,536 cells have to be able to stay charged for at least 2 milliseconds while lightning strikes the power lines in the form of a shower of alpha particles.

The techniques used by the 64-K RAM makers to establish the integrity of their parts are varied. Those designing for captive consumption—IBM Corp. and Bell Laboratories—improve yield by swapping in redundant cells and circuit elements. To quell power supply fluctuations, Japan's Nippon Electric Co., Mostek Corp. of Carrollton, Texas, and others tie their capacitor plates to ground instead of the supply voltage. To maintain the highest possible voltage level in the cell, most manufacturers capacitively boost, or bootstrap, their word lines to restore about a 7-volt level after reading or writing. Intel Corp. of Santa Clara, Calif., further bootstraps its bit lines to improve refresh margins. Sense amplifiers have become more discriminating. Intel, Fairchild Camera & Instrument Corp.'s MOS Products division, San Jose, Calif., and others use full-sized dummy-cell capacitors for a better match with the storage cell capacitors.

To increase stored charge, several approaches are being tried. The Japanese, in general, simply make their storage capacitors (and cells and chips) bigger. Mostek and Bell Labs went from diffused to polysilicon bit lines, to leave more room for capacitors. National Semicon-



Next big market. So far, Intel and Hitachi have introduced 16-K electrically erasable programmable read-only memories. Most makers of ultraviolet-light-erasable PROMs will follow suit. Intel's 2816 (shown above) is unique in that it allows bytes to be erased individually.



Emaciation. When the 1-K 2102 static random-access memory (left) was introduced back in 1972, its cells took up nearly 8 mil² each. On the right is a cell from Matsushita's new 64-K static RAM; using double polysilicon and fine lines, it measures 0.5 mil².

ductor Corp. of Santa Clara, Calif., proposes a triple-polysilicon scheme that would engulf both polysilicon capacitor plates in oxide dielectric for reduced leakage. Advanced Micro Devices Inc. of Sunnyvale, Calif., and other RAM makers say they will use the Hi-C cell that in theory will markedly increase the otherwise minuscule depletion-region component of the storage cell capacitance. According to Mitsubishi Electric Corp. of Japan, the Hi-C cell lowers the soft-error rate, too.

Also to soften the blow of an alpha particle, Japan's Hitachi Ltd. and Fujitsu Ltd., as well as Intel and Motorola Inc.'s MOS Memory Products Group in Austin, Texas, chose folded metal bit lines for their 64-K parts. These are laid out next to each other instead of being aimed in opposite directions, on the supposition that the common-mode rejection ratio of the sense amplifier is increased when the charge generated by an alpha particle is coupled to both lines. Finally, it now seems that all serious competitors will glaze their chips with an anti-alpha material like polyimide or silicone. Motorola, Hitachi, Toshiba, Mitsubishi, Fujitsu, NEC, and Texas Instruments Inc. of Dallas have all agreed to do this.

Beyond the 64-K level, the intrepid Japanese have also displayed 256-K and even larger dynamic RAMs. NEC-Toshiba Information Systems Inc. and the Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. both described quarter-megabit dynamic RAMs at the 1980 International Solid State Circuits conference, held last February. At this same meeting, members of the now disbanded Cooperative Laboratories of the VLSI Technology Research Association flaunted a 512-K RAM and insinuated that they knew the recipe for the monolithic megabit chip.

The 256-K RAMs of NEC-Toshiba and NTT are quite different. NTT's part, undoubtedly a research vehicle, had redundant circuit elements and promising but unproven molybdenum-polysilicon gates and employed slow-turn-around electron-beam direct-stepping-on-wafer lithography.

NEC-Toshiba's 256-K RAM is a different story. Architecturally, it is nearly identical to its 64-K chip, being almost a direct size reduction. NEC used direct-stepping-on-wafer processing for a 64,449-square-mil die that is only 27% bigger than its 64-K RAM and about twice the size of others' wares. At ISSCC 80, the company showed the part in a 16-pin package with the ninth address signal—A_8—on pin 1. This may be standardized by the Joint Electron Device Engineering Council's JC-42.3 MOS memory standardization subcommittee. On each of its 1,048 sense amplifiers, NEC hangs 256 cells—no more than TI or Mitsubishi do in their 64-K RAMs. Some therefore think NEC will leapfrog everyone else with this part. In the meantime, a couple of U. S. manufacturers are expected to show off their designs next year.

The noteworthy part about the 512-K and 1-megabit RAMs patterned by the VLSI Co-op Labs is not the chips but the formula used because it is capable of producing a dynamic cell measuring 2F by 3F, where F is the minimum feature. The researchers claim this is the smallest RAM cell possible, but that is to forget various proposals for cells like TI's taper-isolated design that would store data without a capacitor. However, given the need for a select transistor and capacitor, the labs' structure, which uses what it calls quadruply self-aligned MOS and vertically stacked tantalum capacitors, may be just about the ultimate.

Pseudostatic hopefuls

The quest for the smallest cell notwithstanding, the density of today's single-transistor-cell dynamic RAMs is hard to beat. Refreshing them remains a headache, though, and users still hope that somebody will invent one that appears totally static.

The attempts thus far have brought about pseudostatic RAMs— basically dynamic memories capable of refreshing their own arrays. The 2-K-by-8-bit 4816 from Mostek and the 4-K-by-8-bit Z6132 from Zilog Inc. of Cupertino, Calif., have been around for some time but their acceptance has been lukewarm, primarily because their bit densities are not quite adequate to compensate for the logic needed for the self-refreshing.

But now that the 64-K level has been reached, a crowd of self-refreshing RAMs is anticipated. In a way, the 64-K dynamic RAMs from Mostek and Motorola may be considered the first of these. Each incorporates a self-refreshing mode activated with a low signal applied to pin 1. Motorola's has a second automatic mode that continues to refresh the RAM in a battery back-up situation. AMD is also considering the idea, and Inmos Corp. of Colorado Springs, Colo., plans to give its 64-K RAM self-refreshing, activated in this case with both the row-address and column-address strobe asserted. Inmos wants to keep pin 1 free in the event that Jedec gives the pin another designation.

But these 64-K RAMs have by-1-bit organizations, and it is really the microprocessor users with their byte-wide data that need pseudostatic memories. To the rescue will come Intel, Motorola, Texas Instruments, Toshiba, National Semiconductor Corp. of Santa Clara, Calif., and others who will offer 8-K-by-8-bit devices.

Announcements may be heard as early as next year.

It remains to be seen how these designs will solve the difficulties of interfacing with the multitude of different microprocessors that now exist. For instance, if the microprocessor fails to cue the memory to refresh itself, data might die. To prevent that, the memory can begin on its own, but then a request by the processor for data might breed contention. A standard for refresh control signals is clearly in order.

The state of truly static RAMs parallels that of dynamics, albeit at a lower density level. Several manufacturers are striving to get their 16-K chips out the door and the Japanese—in this case one company—have vaunted a 64-K static RAM.

Statics on the move

But as dynamic RAMs are just beginning to get serious about self-refreshing and byte-wide organizations for the microprocessor world, MOS static RAMs, organized by 1 bit, have achieved such blistering speeds that bipolar TTL designs can barely bid for their traditional cache, high-speed buffer, and writable control-store applications. One implication is that n-MOS static RAMs will dominate at 4-K densities and higher in all but the most demanding applications, like scratchpads. There emitter-coupled-logic RAMs, with access times reaching down to 7 ns at the 1-K level, will stay in charge.

The high-speed 4-K-by-1-bit static RAM arena remains lively as Intel and Fairchild continue to punch each other out with their scaled-down high-performance MOS and bipolar processes, H-MOS II and Isoplanar-S, respectively. Using these, Intel's 2147H and Fairchild's 93F471, with their minimum access times of 35 and 30 ns, are the only TTL-compatible 4-K static devices to be had in this speed league. Only over the last year has a long list of MOS makers refined their high-performance MOS processing to the point where they could finally alternate-source Intel's 55-ns 2147.

In the fast 16-K-by-1-bit static class, Intel has allowed Inmos's IMS1400 announcement to precede that of its own 2167. Among others aiming to give Intel claustrophobia in that market are Fairchild, Mostek, and Hitachi, with Isoplanar-S, Scaled Poly 5, and Hi-C-MOS memories, respectively. Of the first two's parts, both have the maximum access time of 55 ns (Table 1). Scaled Poly 5 is a high-performance n-channel process that, among other things, scales channel lengths down to a mere 2.5 μm.

One 16-K-by-1-bit design

Inmos's IMS1400 uses two spare columns to improve yield, but that is only one of a lengthy list of innovations. Using a single-polysilicon process and 2.7-μm channel lengths (conservative against H-MOS-II's 2 μm), the IMS1400 has 1.07-mil² cells on a 30,950-mil² chip—both better than the 2167's 1.5-mil² cells on a 37,697-mil² die. Finally, whereas Intel has seen parts rolling off the line with access times of 40 ns, Inmos says that the typical access time of its device is 30 ns.

Inmos gets its dense array by using polysilicon instead of diffused tracks for the power supply lines and an n^+ diffusion in lieu of metal for ground paths. This approach makes a lot of sense because the polysilicon resistors have to be connected to V_{CC} anyway, and two diffused drain regions of each cell have to be grounded. The plan minimizes contact vias and allows metal bit lines to run right next to each other without being separated by aluminum ground lines.

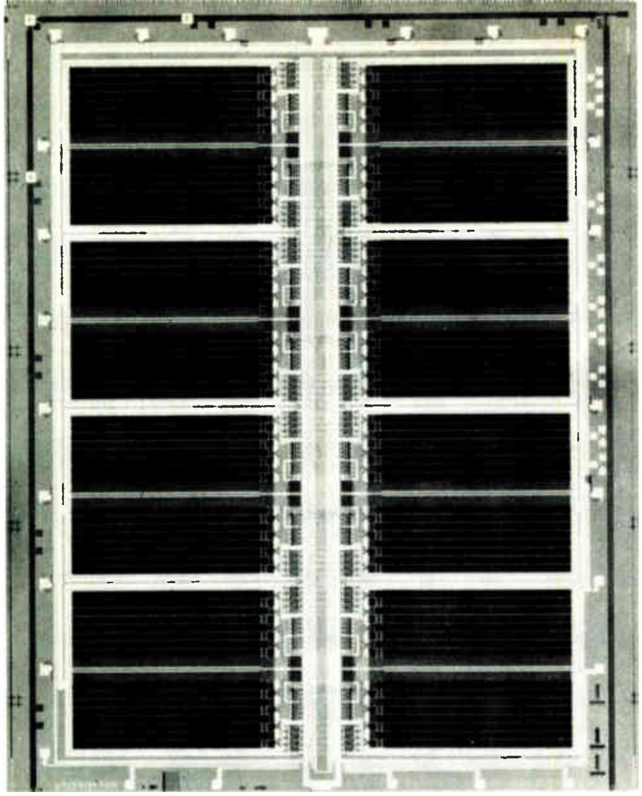
For speed, Inmos employs two key techniques. One is fast, asynchronous bootstrapping circuitry that responds to any input signal without a precharge set-up time delay. Insensitive to noise like changing address signals, these circuits do not power down with zero-threshold natural devices, which allegedly increase operating current and impair performance at high temperatures. Secondly, to sidestep word-line delay, Inmos employs bit-line equilibration circuitry: while data is being shipped out over the word lines, the bit lines are brought to a midpoint value to give the memory a head start in driving cells to their next data states.

Inmos and Intel will both bring out 4-K-by-4-bit versions of their fast 16-K RAMs next year. Inmos in fact

TABLE 1: 16-K-BY-1-BIT STATIC RANDOM-ACCESS MEMORIES

Technology	ECL	High-performance n-MOS				C-MOS
Company	Fairchild	Inmos[a]	Intel[c]	Motorola	Mostek	Hitachi
Part number	100480	IMS1400	2167	MCM 2167	MK 4167	HM 6167
Process	ECL Isoplanar-S	—	H-MOS II	H-MOS II	Scaled Poly 5R	Hi-C-MOS
Fastest access time (ns)	35	45[b]	55	55	55	55
Power dissipation, active/standby (mW)	650 / none	660 / 110	660–990 / 110–165	600 / 75	≈500 / n.a.	175 / 0.1
Cell size (mil²)	0.7	1.07	1.5	1.3	≈ 1.0	n.a.
Chip size (mil²)	20,000	30,950	37,700	38,000	28,000	n.a.
Pull-up device	pnp transistor	first-level polysilicon	second-level polysilicon	second-level polysilicon	second-level polysilicon	first-level polysilicon
1981 availability	2nd half	1st quarter	1st quarter	1st half	1st half	1st half

Notes: All chips will be supplied in 20-pin standard packages
[a]Has built-in redundancy; by-4-bit organization will also be offered
[b]Chip-enable access time; 40-ns address access time available
[c]By-4-bit organization will also be offered



Half a million. Read-only memory capacities are getting enormous. This chip from NEC-Toshiba Information Systems is programmed with an electron beam and stores 512-K. Next year will see several 256-K designs, some with on-chip encryption.

plans two by-4-bit versions, one of them without power-down—a sort of Intel 2149 at the 16-K level—that may be 10 ns faster than the 1400.

In byte-wide statics, Mostek has chased after speed harder than anyone else. It is now ramping up production of its 1-K-by-8-bit MK 4801. Scaled Poly 5 has awarded the memory a 55-ns speed selection, making it by far the fastest byte-wide MOS RAM. Mostek is also now supplying samples of the follow-on 2-K-by-8 bit 4802. Its initial 70-ns access time—to be trimmed to 55 ns by next year—is also unparalleled.

In organizing the 4802, Mostek designers essentially laid two 4801s end to end, creating a 256-by-32-bit array and an exaggerated 108-by-331-mil die. Their goal was speed: the polysilicon rails running the width of the part were not doubled. Also subtracting from access delay and power consumption is what Mostek calls address activation. With this, a transition on any of the address lines initiates internal timing without having to rely on a chip enable followed by a set-up time.

A long-sought goal with static RAMs—and dynamic ones, too, for that matter—is to remove interconnection paths from the array. The last year saw a number of ingenious new tricks for doing this. In Mostek's 4801 and 4802 the polysilicon loads are tied to one of the two data lines, depending on which side of the chip the cell lies, rather than to V_{CC}. Thus, the cell is powered through the resistors, eliminating the V_{CC} contact in the cell and the power lines. Interestingly, Motorola took a similar route in its 64-K dynamic RAM, in which each word line doubles as a capacitor plate for an adjacent row, so that only one level of polysilicon is necessary. Motorola's RAM, which was just recently analyzed by Mosaid, the MOS memory analysts of Ottawa, was called "extremely complex and masterfully executed."

Another tack to scrap power supply metalization is used by Hitachi in its 2-K Hi-C-MOS 6116, now at the sample stage. The cells are embedded in a ubiquitous p well, and an n-type island is found in each cell. A diffused p-type power line, located nearby, completes a pnp structure and the cell is powered by the resulting buried-junction field-effect transistor. This remarkable idea will surely be exploited in Hitachi's imminent 16-K-by-1-bit part.

Byte-wide static devices are also going after the lowest possible power consumption for microprocessor and battery back-up applications. Here again, Mostek has invented a unique circuit twist called data-save that will first be found in a low-power version of the 4802 called the 4802D-1. Later, it will be applied at the 4-K level to the 4147 and 4148 (Mostek's versions of the 2147 and 2148). The idea behind data-save is simple: when the user supplies a 5-V level to the write-enable pin (WE), V_{CC} can be turned off and the array, in standby, draws only microamperes.

But the lowest power can come only from C-MOS and the Japanese are relentless. Besides Hitachi's 6116, which has an n-channel array, Toshiba disclosed at ISSCC 80 an all–C-MOS six-transistor-per-cell 2-K-by-8-bit fully static RAM. Its 1-microwatt standby dissipation is noteworthy, but when it will be placed in user's hands is unclear. Harris Corp.'s Semiconductor Products division in Melbourne, Fla., has also been promising a similar IC.

Finally, there's Matsushita's 64-K static RAM, which also surrounds an n-channel array with C-MOS. But the novelty stops there; the chip looks just like Hitachi's 6147, but with cells scaled way down to 304 μm^2, using 2-μm rules, for a 48,906-mil^2 die. But it seems incredible that the company can really be about to ship a chip with 400,000-plus components.

ROMs on the rise

The demand for read-only memories is going up and up because of the storage requirements of applications like speech synthesis and high-level languages. For some time now, 64-K n-MOS ROMs have been available from various sources and lately 128-K, 256-K and even denser memories are being glimpsed. One company that has already announced a 128-K ROM is Supertex Inc. of Sunnyvale, Calif., a rising star in the C-MOS business. Its 16-K-by-8-bit CM1310 has a slow 2-microsecond access time, but 200 microamperes is all that is needed to keep this big ROM alive on standby.

In some applications—namely speech synthesis—speed does not have to be of the essence. For months, TI has been using a proprietary 128-K ROM in its Speak & Spell talking toy. Since access times for this application can be in the microsecond region, TI used simple p-channel MOS to build the part. Indeed, the slow, high-capacity ROM is one component that is breathing some life into p-MOS: the firm has even added a new fabrication line to support the demand for it, but has not said whether it will offer the device on the open market.

Mostek is gunning for speed and high density alike when it comes to ROMs; next year, it hopes to provide

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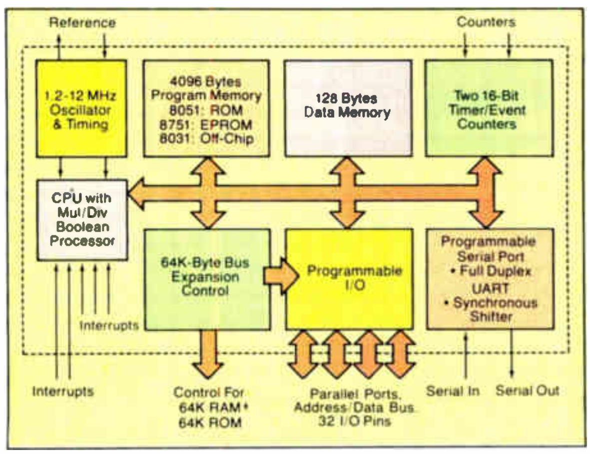
Then there's the 8051's full duplex serial I/O port, which allows it to talk to peripherals—such as terminals and UARTs—at a much higher data rate than could be achieved using software alone. At rates, in fact, from 122 to 31,250 baud. This port can also link multiple 8051s to achieve transmission rates up to 187,500 baud using standard asynchronous protocols and an address-driven automatic wakeup.

Added to that is the 8051's sophisticated interrupt system, with five sources, two priority levels, and a nested structure which allows exceptionally efficient monitoring of internal and external alarms.



Boolean bit manipulation

In addition to handling 8-bit binary and BCD arithmetic, plus 8-bit logic operations, the 8051 family offers an exclusive feature: extensive Boolean bit-handling—especially important in controller applications.

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A direct descendant of the industry-standard 8048, the 8051 family is the beginning of the new MCS-51™ series of high-performance devices. In addition to the ROM-based 8051, the other two members of the immediate family are the 8751 EPROM version, intended for prototyping and low volume production, and the 8031, which relies on external program memory.

For further details on the 8051 family and its development support, contact your local Intel sales office/distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

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Universal Instruments Corporation • Box 825, Binghamton, New York 13902 • Tel: 607/772/7522 • TWX: 510/252/1990 samples of an 80-ns 256-K chip. Other U. S. chip makers will also work on 256-K parts next year, but the Japanese, mainly because of the memory required to store and display their alphabet, have been building 1- and 4-Mb wafer-sized ROMs. Equally impressive in terms of density is NEC's 512-K ROM chip, patterned with direct-stepping-on-wafer optical lithography but programmed with an electron beam writing directly on the wafer. With ROM capacities of a quarter megabit and up, protection will have to be provided or a copycat could make off with a fortune's worth of software. So some 256-K and larger ROMs will be fitted with on-chip data encryption and decryption circuitry.

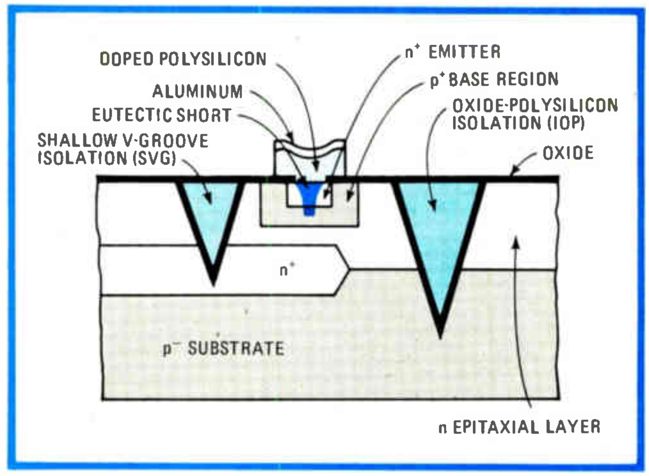
The exciting thing about a mask-programmable ROM cell is that it can literally be reduced to the crossing of two wires. AMI is working on a C-MOS 128-K ROM that proves this point nicely. Its cell is defined with a polysilicon strip overlapping a diffused region perpendicular to it and programmed by being hit with a depletion implant. Then, with that cell's bit line grounded, the word lines are consecutively pulsed low. The cell output will remain high except when a cell has the implant. AMI is expecting access times on the order of 10 to 20 μs.

Many fuse links

Although fuse-link 2-K-by-8-bit Schottky TTL programmable ROMs are available from Harris, Signetics, Intel, Raytheon Co. of Mountain View, Calif., and Monolithic Memories Inc. of Sunnyvale, Calif., the supply is limited. This situation will undoubtedly change next year when National, Motorola, TI, Fairchild, Fujitsu, and AMD see production quantities of their 16-K devices. Also by that time, Motorola will have introduced its 4-K-by-4-bit MCM7695, and Fairchild may have introduced its 8-K-by-8-bit 93F564/65. Using Isoplanar-S, Fairchild expects a die size less than 35,000 mil^2 and a typical access time of 35 ns. It remains to be seen just when bipolar PROM manufacturers will rise to the 32-K density level.

Bipolar PROMs differ in their fuse material and hence, in their difficulty of programming. There are many fuse types—AMD's platinum silicide, Intel and Harris's polysilicon, the diffused eutectic aluminum process (DEAP) of Fujitsu, and Nichrome or titanium-tungsten from the rest. Polysilicon has been in the news recently, having allowed Intel to build a 25-ns (typical), 600-milliwatt 16-K memory and Harris to construct its 6641, the first 4-K fuse-link C-MOS PROM.

Fujitsu has been receiving much attention with its DEAP process, which results in half the cell sizes and access times of conventional PROMs. The secret is two passive isolation methods called SVG, for shallow V-groove, and IOP, for isolation through oxide and polysilicon. A cell is programmed by forcing a reverse current through the emitter of its transistor. When the aluminum-silicon interface begins to melt—the eutectic temperature—it diffuses to the base region and shorts out the junction. Current flow halts, and so does any further rise in temperature. Fujitsu plans a 16-K PROM using this clever principle and has already succeeded in achieving 35-ns access times at the 4-K level with a recently improved DEAP cell.



DEAP. Fujitsu's diffused eutectic aluminum process, or DEAP, has been yielding PROMs with half the cell sizes and access times of conventional bipolar fuse-link PROMs. It is programmed with a reverse current that shorts out the base-emitter junction.

As of 1980, ultraviolet-light-erasable PROMs and electrically erasable PROMs firmly established themselves at the 64-K and 16-K levels, respectively, and competition is already fierce in both markets. Earlier this year, 64-K E-PROMs were announced by Intel, TI, Mostek, and Motorola. Battles rage over who was first to announce and whose pinout will succeed.

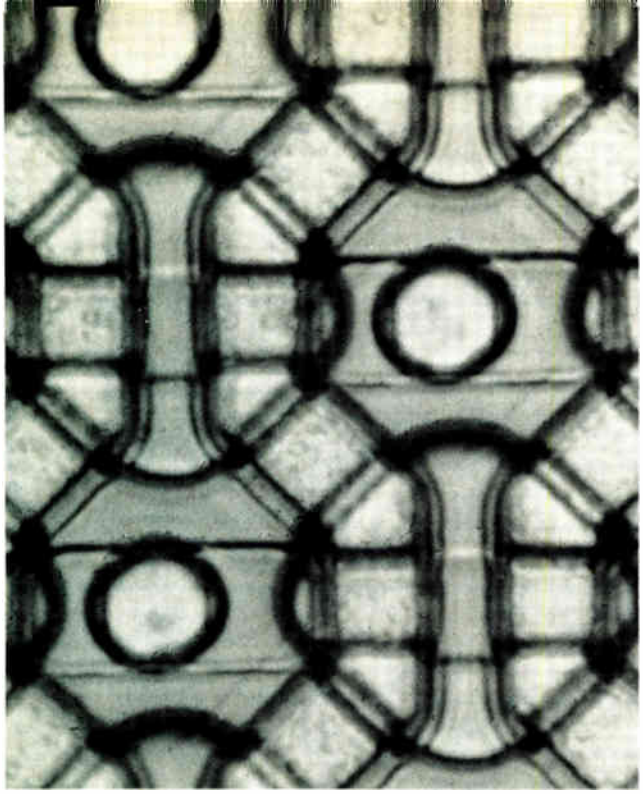
Battle of the E-PROMs

Jedec voted in the 28-pin Intel-Mostek approach, but to spite that decision, TI will try to make its slightly different 28-pin package a *de facto* standard through aggressive pricing and quick delivery. Synertek of Santa Clara, Calif., says it will go along with the Intel pinout, but National will introduce two 28-pin versions to cover both bets. Meanwhile Motorola, with a 24-pin package, will try to plug into many of the sockets created by 64-K ROMs and 16-K E-PROMs as it possibly can.

As for technology, Intel is using a variant upon its H-MOS-II technology called H-MOS-E for the smallest 64-K chip size—32,399 mil^2—and a best-case access time equal to Mostek's expected 200 ns. This is the same access time sported by Intel's new 32-K E-PROM, the 2732A. Such speeds are necessary for the latest generation of 16-bit microprocessors.

Mostek and TI are also pursuing density, using what TI calls the X-series cell, though Mostek had actually invented it for its MK36000 mask ROM. In this layout, the contact via of each column line connects to the drain/source regions of four devices, and each pair of devices shares bit and word lines. The upshot is a very dense arrangement requiring only a half a contact via per cell.

TI's present 64-K E-PROM is pretty big at 40,800 mil^2, as is Mostek's at 57,000 mil^2. But TI has yet to revamp its chip with the X-shaped cell, and Mostek's not only includes a 25% redundancy but is also built with 5-μm features. Using the X cell, TI will shrink its TMS 2564 to 33,000 mil^2 while lopping 100 ns off of the 450-ns access time. And this assumes 4.5-μm design rules; using 3.5-μm rules, TI has already built a 41,500-mil^2 128-K E-



Marks the spot. Mostek and Texas Instruments are using an X-shaped cell in their 64-K erasable programmable ROMs. These unique cells, which were first used in Mostek's MK36000 mask ROM, share source-drain regions, bit lines, and word lines.

TABLE 2: TWO 2-K-BY-8-BIT ELECTRICALLY ERASABLE READ-ONLY MEMORIES		
	Hitachi	Intel
Part number	HN48016	2816
Process	MNOS	Flotox[a]
Access time	350 ns	250 ns
Read voltage	+5 V	+5 V
Read power dissipation	330 mW	500/100 mW (standby)
Read endurance	unlimited	unlimited
Data retention	10 years	10 years
Write time	10 ms/byte	10 ms/byte
Erase time	100 ms	10 ms
Write/erase voltage	+25 V	+20 V
Write/erase endurance	10^4 cycles	10^4-10^6 cycles
Cell size	0.64 mil^2	0.85 mil^2
Chip size	28,302 mil^2	n.a.
Other comments	—	has byte erase
Availability	4th quarter, 1980	1st quarter, 1981

[a]Floating-gate tunnel oxide

PROM it is providing in sample form to a select few.

Mostek, too, plans to use 3.5-μm features to shrink its future E-PROM dice.

Mostek is pondering whether to add a third level of polysilicon to its X-shaped cell to allow electrical erasure. Details of this structure will be given in December at the International Electron Devices Meeting. Basically, the polysilicon floating gate is discharged by electric field emission to the added polysilicon layer. But more importantly, by using an adaptive erasure mechanism that senses when the cell is erased, the memory manages on a single transistor per bit—a first for a floating-gate EE-PROM.

Tunneling through

But if any one word summarizes recent progress in electrical erasability, it would have to be "tunneling." Intel probably thought the word would be Flotox, an acronym it coined for the floating-gate tunnel oxide it uses in the 2-K-by-8-bit 2816 EE-PROM launched earlier this year. That chip, and the principle behind its operation, has already had an enormous impact on the industry and more far-reaching consequences are in store.

Not long after Intel announced the 2816, Hughes Research Center followed with an 8-K C-MOS EE-PROM that also exploited electron tunneling through an oxide less than 200 angstroms thick. (Some say these layers are on the order of 120Å.) But whereas Intel uses nine transistors per byte, Hughes merges two per bit. On the other hand, Intel grew its tunnel oxide over an n^+ diffused region instead of over the channel, allowing bytes to be erased individually—a feature that Hughes will tack on to later parts. Motorola also has a series of tunnel-oxide EE-PROMs planned, and it says its cells will be significantly more compact than Flotox cells.

But Intel's byte erasure is the feature to match, for without it, a RAM buffer the size of the EE-PROM is needed to erase 1 byte. Beyond byte erasure, the next features to be added to EE-PROMs will be latches for the address and incoming data. Then EE-PROMs will be able to time out their own erasing using an adaptive-erasing feature like the one Mostek is proposing for its triple-polysilicon EE-PROM. After all this is on chip, a user will (finally) be able to write data into the EE-PROM as though it were a static RAM.

Intel says that Flotox requires only three more processing steps than H-MOS-E, the process it uses to build E-PROMs. It also says that in time the EE-PROM will overtake the E-PROM in popularity. Even though modern E-PROMs use single-device cells, packaging and testing are a large part of the cost, and EE-PROMs test faster and do not need that expensive quartz window.

Were it not for Hitachi, metal-nitride-oxide semiconductor technology would seem dead for high-density EE-PROMs. But Hitachi's 16-K HN48016, based on MNOS and on the market, does very well against the 2816 from Intel (see Table 2). It is also being priced very aggressively. What's more, the device uses two transistors per cell, so that charge need not be removed from a storage cell's gate to read that location. This gets rid of the so-called "read-disturb' problem that has muddied the reputation of MNOS memories.

The ideal EE-PROM

The ideal EE-PROM would really be a nonvolatile RAM; an EE-PROM with the fast read and write times of a static RAM. The solution proposed to this problem by Xicor Inc. of Sunnyvale, Calif., is to shadow a 250-ns static RAM with a floating-gate array on the same die that gets loaded automatically when power fails. The only drawback with this technique is a high number of devices per cell, making high bit density more difficult.

A recent development by IBM points to a true nonvolatile RAM, however. Using a dual-injector structure, it has

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written and erased in as little as 200 ns and the researchers at the Watson Research Center are looking forward to 100-ns access times and billions of cycles of endurance at 5 V or even less.

The market for bubble memories has been disappointingly slow to mature, but the availability of 1-megabit and higher-density chips promises to fuel a rapid growth in the 1980s. So far, Intel Magnetics, TI, National, Fujitsu, and Rockwell International Corp., Anaheim, Calif., have announced 1-Mb bubble memories. The ramp up to volume production of these devices has been a shallow one, however, primarily because of the numerous support elements required to make a product a success.

Millions of bubbles

The forthcoming megabit chips are similar. All are based upon block-replicate architectures, all employ swap and replicate gates, and all store redundant-loop information on chip. The announced products also have in common chevron-shaped propagation patterns made from Permalloy and external criss-crossed coils for the drive field. Work continues on replacing the Permalloy with ion-implanted patterns like contiguous disks and on replacing the coils with elements more conducive to integration.

Contiguous disks will be at the heart of the next-generation, 4-Mb chips. On the one hand, they allow two-way propagation and thus could halve access time, while on the other, they do not demand a tight-tolerance gap, as chevrons do. But replication with contiguous disks is just now being reported, and the mechanisms behind it are not yet well understood. IBM, which for the longest time pushed its wall-encoded bubble lattices, has all but dropped them in favor of implanted patterns like those of disks.

The only alternative to the bulky and speed-limiting coils is the punctured conductor sheets proposed by Andrew Bobeck of Bell Labs, who says, "We are getting ready to make a stab at a working chip." The main problem is with the detector, and Bobeck is looking into new materials for detection based upon the Hall effect.

Sud and Hardee: builders of a dynamic static RAM

Rahul Sud and Kim C. Hardee, the two-man design team responsible for the first integrated circuit to emerge from the British-backed Inmos Corp., have had some similar experiences. Both were top technical graduates at Florida universities in the 1970s. And though strangers to each other at the time, they also worked at Harris Corp.'s Semiconductor Products division in Melbourne, Fla. When they joined Inmos's operation in Colorado Springs, Colo., in early 1979, both had strong experience in most types of memory and circuit design.

But though both Sud, 27, and Hardee, 29, had designed memory circuits previously, Hardee's expertise was in static devices. While at Harris, he was the primary designer of four complementary-MOS static-RAM circuits, with densities ranging from 1-K to 16-K. Sud's experience, on the other hand, involved dynamic devices. Prior to joining Inmos, he worked with another designer at Signetics Corp. in designing a 64-K dynamic RAM and a 128-K read-only memory device.

Their combined effort at Inmos led to a static RAM—the IMS1400—that successfully incorporates performance-boosting technique such as active bit-line equilibration and bit-line precharging and bootstrapping circuitry.

Also unique to the IMS1400 design are a single-layer polysilicon cell about the same size as conventional double-poly cells; a redundancy technique that improves yield up to a factor of five yet still takes less than 2% of device real estate; and a novel, low-power substrate-bias generator producing a lower bias than that in current commmercially available circuits. Sud and Hardee now have five patents pending on aspects of their static RAM's design.

In the early going, the two recall, they designed in parallel, working individually on a particular circuit function and then exchanging work for the other's criticism. "Almost invariably, we'd find something wrong with the other guy's approach and then we'd work it out and come to a common solution," Hardee says. "Where we really had problems was when both ideas were equally good . . . in several instances it almost came down to flipping a coin, and we'd finally end up asking John Heightley [Inmos memory product vice president] to decide."

Hardee, who grew up in Florida, holds bachelor and master of science degrees in electrical engineering from the University of Florida, Gainesville, where he completed his graduate work with a perfect 4.0 grade average. Sud, a native of India, holds a B. S. in physics from the University of Delhi and an M. S. in solid-state physics from the Florida Institute of Technology—graduating first in his class in both programs—and an M. S. in electrical engineering from the University of California at Berkeley. He is also a doctoral candidate in electrical engineering at Stanford University.

Sud agrees that the IMS1400 benefited greatly from the synergistic infusion of dynamic circuit ideas. "As a matter of fact," he observes, current dynamic-RAM design techniques "could also benefit through more use of static design approaches." He fully expects a further mingling of dynamic- and static-memory design techniques as the era of very large-scale integration unfolds. **-Wesley R. Iversen**

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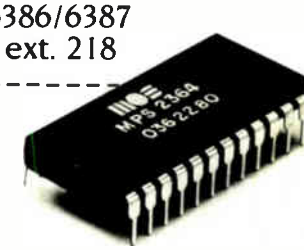

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MICROSYSTEMS & SOFTWARE

Following in the mainframe path, microprocessor-based systems are unloading their housekeeping chores onto smart support chips; lower power, faster math, and even multiprocessing options abound

by R. Colin Johnson, *Microsystems & Software Editor*

Hardware is not an end in itself—that insight is sweeping the microprocessor industry. Systems are always the final product, and the microprocessor manufacturer who wants to get ahead had better offer system support. That means taking a hard look not only at the application problems to be solved but also at how mainframe manufacturers have succeeded in solving them.

Emulating the big machines, today's microprocessors offload traffic management chores into memory management units, input/output processors, and other smart support chips. In this way very large-scale integration is truly replacing the board-level auxiliary processors of the past. In some cases the microprocessor is even emulating a mainframe or minicomputer, so dense and complex has VLSI become.

The application problems being tackled are many and varied. The need for speedier mathematical operations is pushing the development of 32-bit devices, while economy is favored by 16-bit designs that interface with standard 8-bit-wide memories. Flexibility is provided by keeping read-only memories off the otherwise single-chip processor, and low power is addressed by complementary-MOS versions of standard machines. The families of special-purpose microprocessors that make room on chip for extra elements like data converters continue to expand, as does the high-volume market for low-cost microcontrollers.

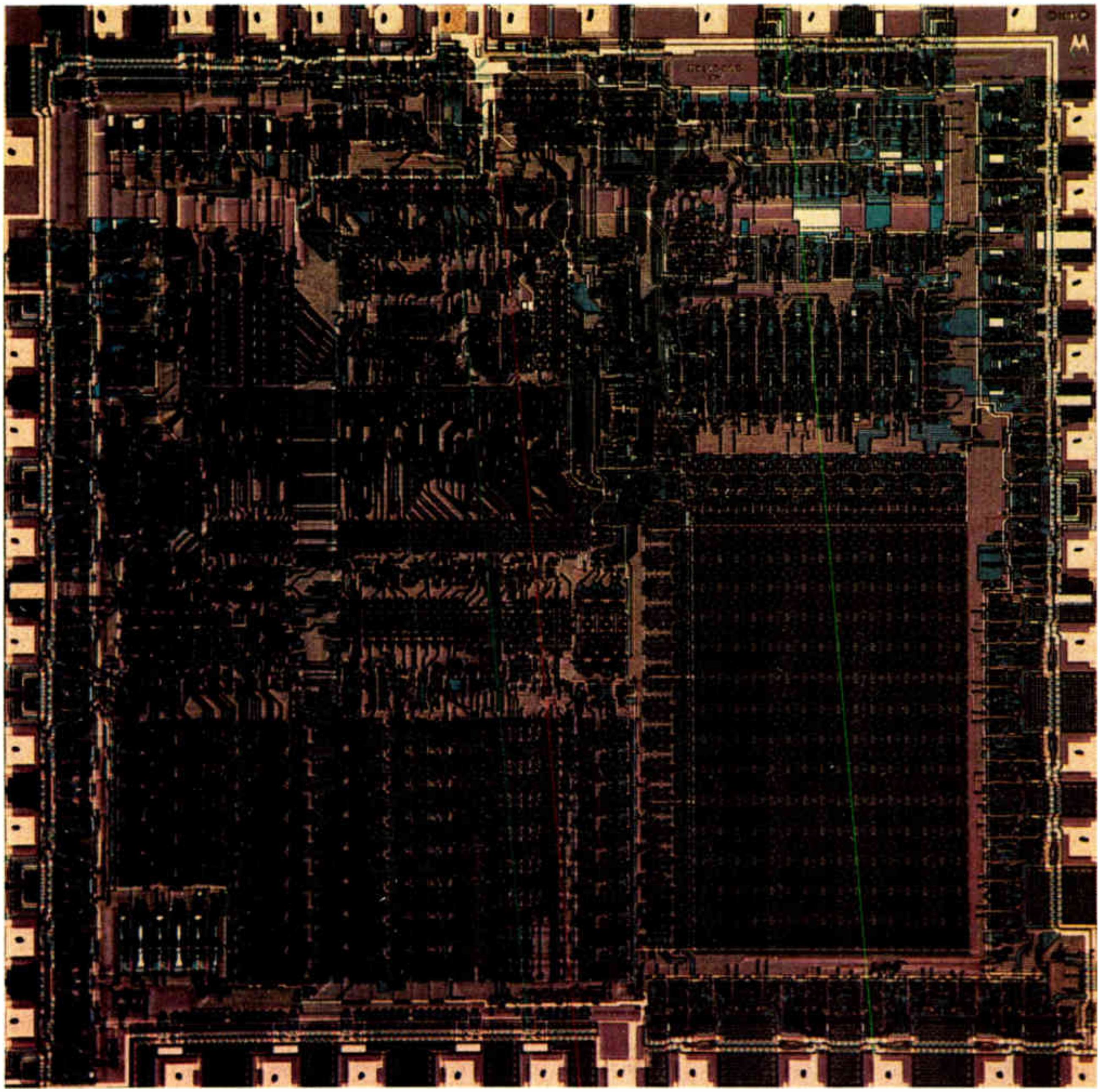
For the most complicated tasks, multiprocessing is now definitely the way to go. The logic it requires is already being designed into some microprocessors, and the standard buses are making provision for it too.

Hardware sophistication makes necessary more elaborate software development tools. Friendly operating systems and modular languages are easing this burden, as is the appearance of standard operating systems that give different microcomputers access to common programs, making for truly portable software systems. Software support for true multiprocessing will shortly realize this long-awaited capability in microsystem design.

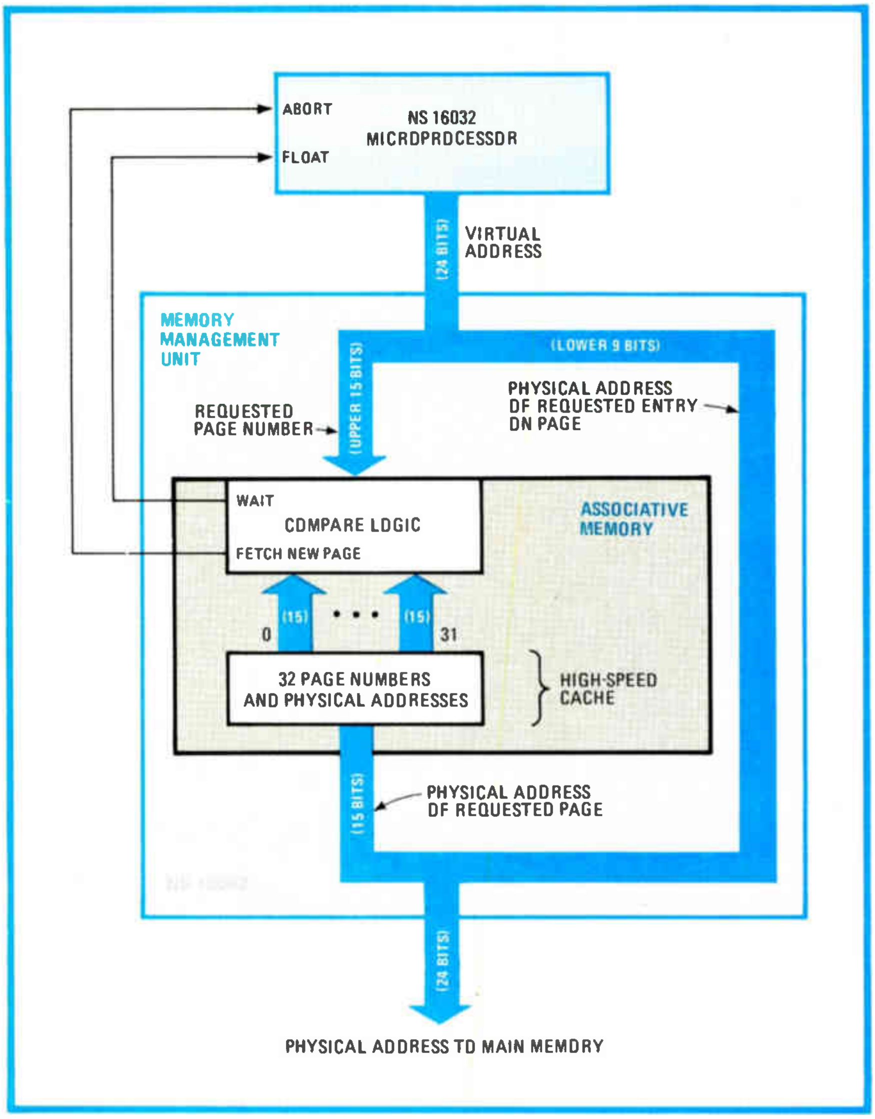
On to 32-bit power

Now that the Institute of Electrical and Electronics Engineers has adopted a standard data format, the transition to 32 bits will accelerate. That changeover will be much smoother than the one from 8 to 16 bits. It will be eased into by companion processors that add 32-bit arithmetic to present 16-bit machines, by incorporating 32-bit data paths and superset instructions into present 16-bit devices, and by reserving operation codes to be executed as software macro instructions now, but by hardware coprocessors later.

One way to make the 32-bit transition is to tightly couple a coprocessor chip to the main microprocessor. Intel Corp.'s 8087 numeric data processor does just that. The Santa Clara, Calif., company has been delivering the 8086 16-bit microprocessor for quite some time, recently in an 8-megahertz version. But speed alone is not the answer. In modern mainframes numeric operations that are often used but slow to execute in software are offloaded into special-purpose board-level coprocessors. The same approach is taken by the 8087; in effect,



C-MOS microprocessors. Since this microprocessor has all the necessary circuitry to form a microcomputer, except a read-only memory, it qualifies as a ROM-less microcomputer. It uses n-channel technology in the random-access memory cell, to save die area, and includes a wake-up timer and two power-saving instructions that allow on-chip memory to be retained while the processor is in a low power state.



Virtual memory. With each virtual address issued, the memory management unit looks up the physical address of the requested page in its high-speed cache. If it turns out not to be there, then the processor is directed to wait with its bus buffers floating.

it expands the instruction set of the 8086 to include 32- and 64-bit integer arithmetic, IEEE-compatible floating-point operations, trigonometric functions, and other number crunchers that can increase numeric throughput a hundredfold. In Intel's new nomenclature the two used together are called the iAPX 86/20.

Do it with microcode

Other major 16-bit microprocessor manufacturers have chosen to include 32-bit operations in the instruction set of the main processor. Of course, without a 32-bit ALU they require longer execution times, but this method does retain software compatibility with the next generation of 32-bit machines. For Zilog Inc. of Cupertino, Calif., 32-bit data types are a part of the Z8000's basic instruction set. These operations will eventually be offloaded into one of Zilog's forthcoming extended processing units.

An alternative solution is to reserve operation codes for 32-bit arithmetic, floating-point operations, and complex functions. The op codes can be executed as software subroutines now but eventually they will be microcoded into the basic instruction set. Thus future systems can be designed and used now, with the guarantee of both speedier execution and software compatibility later.

One way to implement this method is to use vectored software traps. Motorola Inc.'s 68000 has an extensive trap structure in which every op code vectors to a known memory location. Floating-point operations and complex functions may eventually find their way into the instruction set of the 68000. The Austin, Texas, company's immediate plans, however, are to offer a read-only memory that contains the software for floating-point operations, a method that is slower than microcode.

Texas Instruments Inc.'s 9900 series of microcomputers also employs extensive microcode as well as vectored software traps. The Dallas company is known to have optimized portions of that code in its 4-MHz version of the part; it could in addition enhance the instruction set by defining new op codes. The 990 minicomputer uses the concept of an extended operation whereby external circuitry performs a computation; this could grow downward into the 9900 family allowing auxiliary processors to be attached to the main processor.

The microcode enhancement of 16-bit machines, however, is not as fast as internal 32-bit data paths. Intel intends to use a 32-bit internal structure for its upwardly compatible iAPX-432 whose details were first revealed this year. The 432 will be a multichip solution, including a variable number of data processors, storage modules, and interface units.

Truly 32 bits

Two manufacturers have chosen to include 32-bit data paths on their present-day processors. Both the 68000 from Motorola and the 16032 from National Semiconductor Corp., Santa Clara, Calif., perform 32-bit integer arithmetic. Since the 68000 is being packaged in a chip-carrier, the data-bus interface could be extended to 32 bits. The present 64 leads plus the added 16 would bring the count to 80, eminently feasible for a chip-carrier. However, more buffers and additional control circuitry would need to be integrated on the chip.

National could do the same with its advanced processor, which was first announced this year. It is already committed to bringing out enhanced versions of its 16000 series. Its concept is to provide software-transparent slave processors that extend the series' instruction set and to integrate these functions into the basic processor in the future. Their virtual memory management unit (16082) allows programs to address 16 megabytes as if it were all contained in semiconductor memory. The unit uses a paging system that brings mass storage on line in a mode totally transparent to the programmer.

Micro mainframes

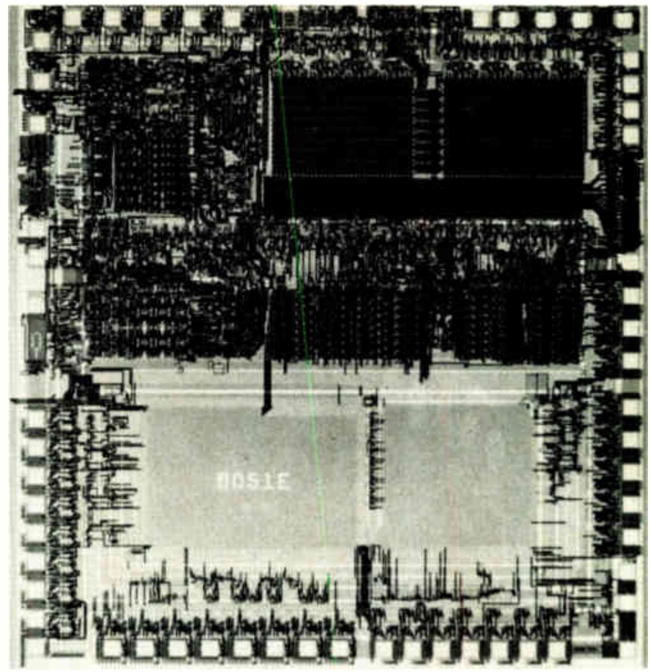
Another major development is the trend to fabricating very large-scale integrated-circuit versions of proven mainframes and minicomputers. The show-stopper this year is International Business Machine Corp.'s VLSI implementation of the processor portion of the most popular mainframe of all time, the System 370. It emulates that 64-bit-wide instruction set with an 8-bit ALU and chunks of microcode in external ROM.

Data General Corp., of Westboro, Mass., has cast its Eclipse high-performance minicomputer in silicon and Signetics Corp., Sunnyvale, Calif., is also reportedly working on a VLSI implementation of a minicomputer.

Ironically, though, peripheral support chips may become more important than the actual microcomputers. Since it is possible to build an advanced microsystem around any of the processors, designers are discovering that support chips make the difference. Zilog, Motorola, and National are all working on a comprehensive set of peripheral processors aimed squarely at their respective 16-bit machines. To the not uncommon memory management unit and input/output controllers, Zilog has added an intelligent first-in–first-out buffer memory (ZFIO) and a highly programmable universal peripheral controller (ZUPC). The ZUPC combines the instruction set of its Z8 microcomputer with two ports, plus handshaking, and a ROM for customized protocols.

More support

Intel has chosen to keep the 8086 compatible with its extensive line of 8-bit peripheral chips by segmenting memory into bytes. Its input/output processor, the 8089, takes either byte- or word-wide data, so that it will work with either the 8088 or the 8086. Intel does plan successors to both the 8088 and the 8086—the iAPX 188 and the iAPX 186, respectively—and both the 8087 and the 8089 will be offered in versions that support those updates. The company also plans to build a successor to the iAPX-186, the iAPX-286, with higher performance and an extended instruction set. It will feature on-chip memory management as well as several operating system functions in the iAPX-286/30 version. The 8089 itself is a very flexible I/O processor that can be programmed to handle anything from a slow printer to a fast disk drive. It includes two interfaces to peripherals and in many systems may be the only I/O handler necessary.



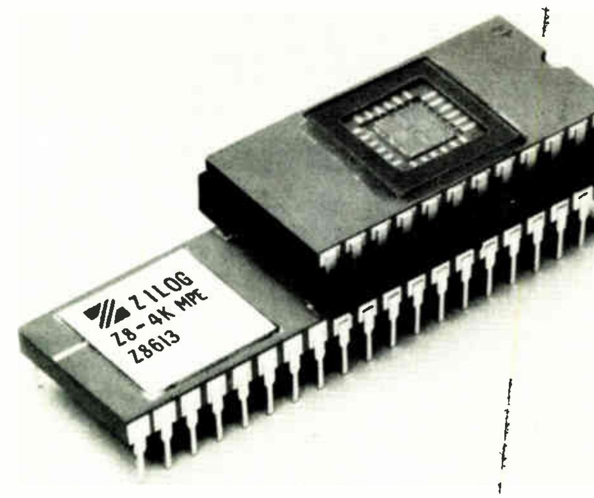
Bond-out chip. This special version of the 8051 microcomputer is designed for use in an in-circuit emulator. It brings out data lines and address lines separately so that the significantly absent program read-only memory may be simulated externally.

8-bit economy with 16-bit power

If the argument for wider data paths is their speedier number-crunching capability, then the argument for the 8-bit machines is their economy. To get the best of both these approaches, several 16-bit machines are now being offered with 8-bit memory interfaces. These allow economical use of standard byte-wide memory packages as well as saving valuable board space by decreasing the number of data bus traces. Intel's 8088 has proven to be a very popular version of the 8086.

Motorola's 6809 fits into this category since it can operate on 16-bit data types, though it is basically an 8-bit machine. It is now offered in an E-version that brings out the clock signals necessary to synchronize multiple 6809Es in a multiprocessing configuration.

TI has had the 9980 in its catalogs for quite some time. As a 9900 software-compatible processor with a byte-wide memory interface, it is joined this year by yet another version, the 9995. This processor is making a strong bid to replace calculation-intensive microcontroll-



Piggyback. The connector on top of this microcomputer allows an external erasable programmable read-only memory to simulate the normally on-chip mask-programmable ROM. Pin-for-pin compatibility simplifies emulation and shortens software development time.

ers, for it features all the on-chip logic necessary to make it a ROM-less microcomputer with 16-bit power and a fast 6-MHz clock.

The technique of adding on-chip data memory (RAM), clock generation, and I/O facilities, but no read-only memory for programs, is coming on strong. This method allows a two-chip microsystem to be formed by merely adding an external erasable programmable ROM; the buyer reaps the advantages of a single chip and is not forced to commit himself to a specific program ROM. Motorola's 6803 is offered in such a configuration, as is Zilog's Z8 and Intel's 8035.

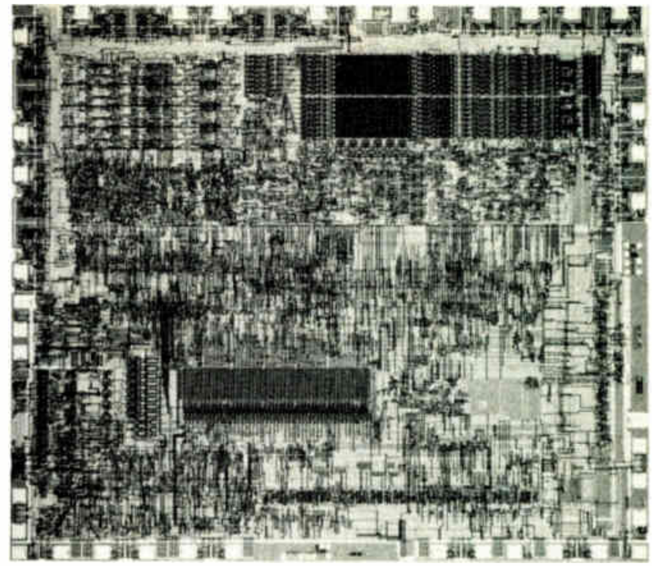
Manufacturers also like this approach since better yields on the ROM-less parts can be achieved, especially if a version with a bad ROM can be recycled and sold as ROM-less.

Another increasingly popular approach is to offer a version of the microcomputer with a piggyback socket for an erasable programmable ROM. In this way program development can be done and tested in circuit with the program being contained in an erasable memory. After the bugs have been worked out, a production run can be done with the mask-programmable ROM version.

Zilog's Z8 is offered in such a package, as are the 3870 and 3873 from Mostek Corp., Carrollton, Texas.

One-chip processors

Other single-chip microcomputers are acquiring features galore. Practically any circuit that can be used with a microcomputer is appearing side by side with it on the same chip. Motorola's 6805R2, which has an on-chip analog-to-digital converter, is a good example. Intel's 8751 includes an on-chip E-PROM, and it won't be long before electrically erasable PROM—the ultimate in nonvolatile memory—turns up on chip. With nonvolatile memories, new applications that require changing data on the fly will become microcontrolled. Also on the way are more and more special-purpose processors dedicated to specific chores such as the 2920 signal processor with on-chip analog-to-digital-to-analog conversion and an



C-MOS microprocessor. The instruction set of the Z80 is combined with the multiplexed memory interface of the 8085 to form the NSC800 from National Semiconductor. An all–C-MOS system can be built using this device with other C-MOS support chips.

instruction set optimized for its job. National is developing dedicated-function processors as well.

Advanced Micro Devices Inc. in Sunnyvale, Calif., is planning a 16-bit version of its 2900 microprogrammable processor, the 29116. This single chip takes the place of four 2900s.

Enter C-MOS versions

Probably the most activity this year has been with C-MOS microprocessors and microcomputers. The low-power solution offered by this technology has taken the industry by storm. Virtually every major 8-bit microprocessor family has at least one member cast in C-MOS, though on many of these much of the circuitry is still in n-channel MOS. The latest addition is a C-MOS version of the popular 8048 single-chip microcomputer. It is due in the first quarter of 1981 from Japan's Nippon Electric Co. and is the first 80C48 to appear, though RCA Corp. and National have similar plans.

National has its NCS800, which executes the Z80 instruction set but has a multiplexed 8080-style memory interface. In fact, this microprocessor will be offered first on an all–C-MOS Multibus-compatible board made by Diversified Technology, Ridgeland, Miss. National, of course, will follow up with a board family of its own.

Another single-chip microcomputer, the 1804 from RCA Corp.'s Somerville, N. J., division is software-compatible with the first all–C-MOS microprocessor ever offered, the 1802.

Several of Intel's original designs are now being laid out in C-MOS versions by other companies. Harris plans a C-MOS 8085 and 8086, American Microsystems Inc. of Santa Clara, Calif., is designing a C-MOS 6809, and Motorola itself has recently introduced its 146805E2, a ROM-less microcomputer that can be mated with its C-MOS ROM (65516) to form a complete low-power system.

Several other Japanese companies besides NEC plan to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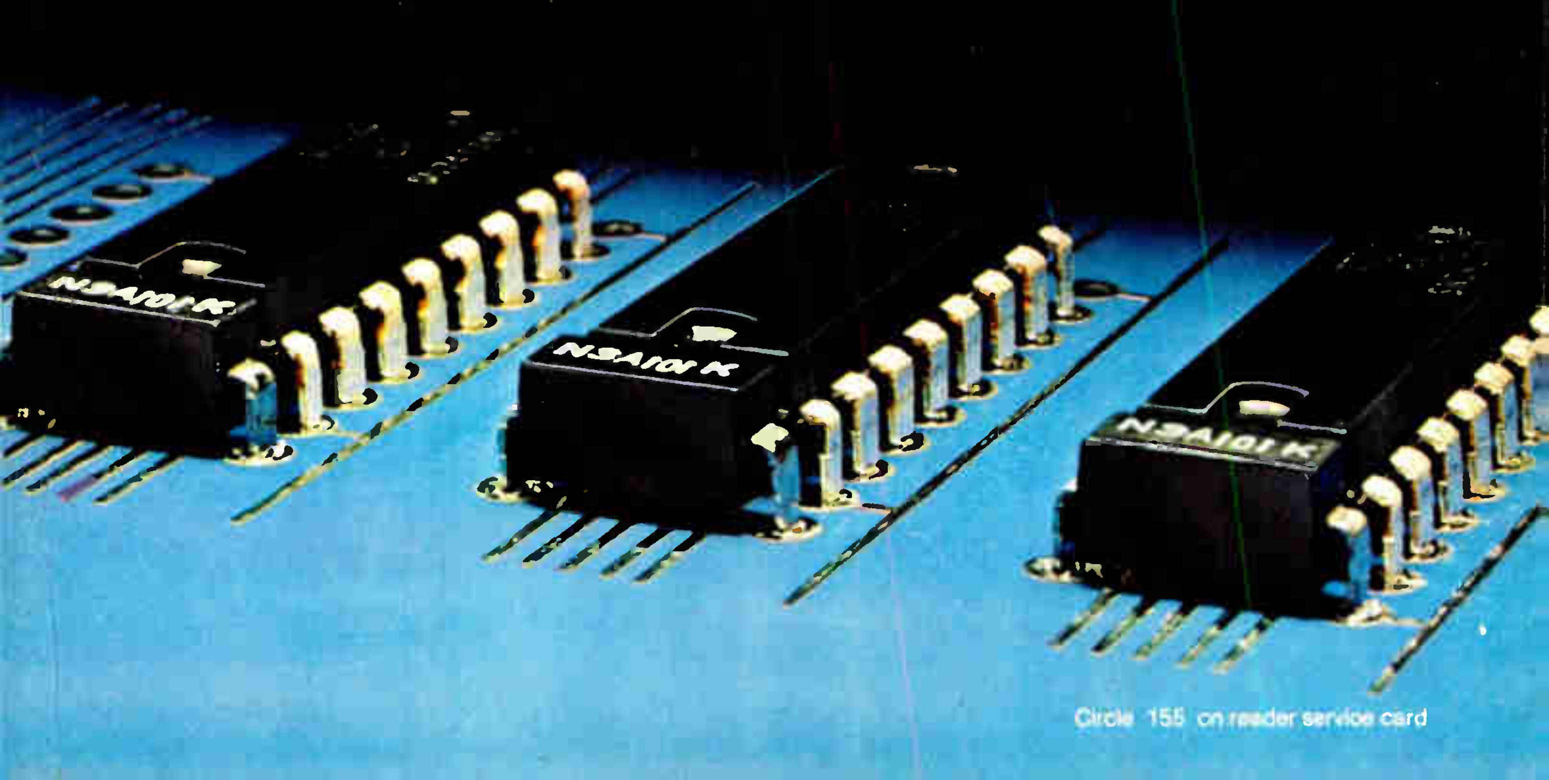
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offer C-MOS versions of American-made originals, too. Hitachi Ltd., for example, will make C-MOS versions of the 6801, 6805, and the 6805R2. Toshiba, however, plans a 16-bit C-MOS microprocessor of its own design using silicon-on-sapphire technology to operate with a remarkably fast 10-MHz clock; some of its circuitry is n-channel, however.

Mostek has announced its intention of adding a C-MOS line to its popular 3870 series of microcomputers. The first part will be the 38C70, which will be pin- and software-compatible with its n-MOS counterpart but will run at half its speed. It will also add two power-saving instructions similar to those executed by the 146805E2.

Crowds of controllers

Microprocessors are finding their way into more and more low-end applications. The 4-bit machines are selling by the million, notably TI's TMS1000 line. But several other major manufacturers are producing lines to compete in this high-volume market. Japan's Matsushita Electrical Industrial Co. is making a 4-bit machine that has several 8-bit operations in its instruction set. This allows the designer to reap the benefits of the low cost of 4-bit machines without incurring the overhead of doing double-precision operations in software.

National Semiconductor is entering this market in a very aggressive way with its COPS product line. These processors are basically 4-bit machines that are offered both with and without on-chip ROM. Their program memory is 8 bits wide for optimal program storage, whereas the other data paths on chip are 4 bits wide. They are also available in both n-MOS and C-MOS versions and can be put in a package with as few as 8 pins, when the Microwire serial interface is the only one that is needed.

In the high-speed arena Signetics is expanding its line of 8-bit bipolar microcontrollers, the 8X300 family. The additions are a Schottky TTL floppy-disk controller and an I/O processor, both compatible with the 250-nanosecond cycle time of the basic 8X300 microprocessor.

The serial bus is becoming increasingly attractive for interprocessor communication as well as in network applications. For example, the Microwire serial interface on several of National's microprocessors does the parallel-to-serial-to-parallel conversion without processor intervention, making this system very easy to use. Mostek's 3873 has a similar serial interface that features software-selectable internal or external baud-rate generation. Intel's high-performance 8051 has a full-duplex serial channel as well as extensive bit-manipulation facilities. Motorola's 6801 and Zilog's Z8 have a convenient on-chip serial interface as well.

Bus arrivals

Zilog's Z-bus, as well as all its peripheral chips, support multiprocessing. The Zilog board line for this bus is expanding almost monthly. Other buses are incorporating the necessary control lines to handle multiple masters on the same bus as well. Intel's Multibus has a well-thought-out multiprocessor control structure that has been incorporated into the IEEE 796 standard for that bus. The IEEE 696 standard for the S-100 bus, adopted this year, provides the necessary control lines to coordinate up to 16 processors sharing common memory and peripherals.

Development lab. Design and debugging of hardware and software plus real-time emulation is supported by this Tektronix development system, 8550. It supports 23 different 8-bit processors and several 16-bit processors; multiuser capability will be added soon.

A start-from-scratch standard that is planned to be processor-independent is being worked on by the IEEE's 896 committee. Not only will it provide for multiprocessor arbitration but in addition it will support a full 32-bit data and 24-bit address bus.

Motorola's Versabus supports multiprocessing and 32-bit data and will be backed by a comprehensive board line. If and when the 68000's 32-bit internal data paths become available off chip, its bus will be ready.

New software supplies

All of these superbrains will remain empty, however, unless sufficient software is developed to fill them. Several versions of the respected UNIX operating system have been trimmed down for microsystem execution. UNIX software makes available a large number of utility programs that can greatly shorten software development time. They are a part of the package that originates from Bell Laboratories and are all written in the language C, so that once a C compiler is written, the support programs are available for use. Whitesmith Ltd. of New York has an implementation called Idris on both the LSI-11- and 8080/Z80-based machines and is working on versions for the 16-bit chips as well. The Mark Williams Co., Chicago, is developing a software package dubbed the Coherent operating system. It will eventually encompass the whole C package, initially for DEC's PDP-11/34. Microsoft, Bellevue, Wash., is also working on a UNIX look-alike dubbed XENIX. It will be implemented for all the major 16-bit microprocessors as well as for DEC's PDP-11 series of 16-bit minicomputers.

Digital Research of Pacific Grove, Calif., is not resting on its popular CP/M operating system. It has been updated (CP/M 2.2) to handle the large file space available on hard disks and will soon become available for the 8086. The company also introduced extensions to handle multiuser (MP/M) and network environments (CP/NET).

Network developments

For users wanting stand-alone software development stations, with access to common mass storage, Nestar Systems Inc. of Palo Alto, Calif., is supplying the network software to link together up to 64 Apples. Avocet Systems Inc., Dover, Del., is offering a similar package for Z80/8080–based systems.

The trend toward shared resources is also evident in microprocessor development systems. The EXORmacs will support up to eight users sharing a hard disk, and Motorola plans to deliver it this quarter. Intel began delivery of its eight-user system, the model 290, in late August, along with the Intellec Series III, a 16-bit development system. In keeping with its past policy, existing Intellec systems are upgradable to the new configurations. In the wings at Intel are plans for the further interconnection of systems making use of its Ethernet local-networking expertise.

While the semiconductor manufacturers concentrate on support of their full line of processors and computer chips, others are assaulting the market by trying to provide software and emulation tools for a cross-company base of popular microprocessors. Emulogic Inc. of Westwood, Mass., for one, has introduced an LSI-11/2–based system, the ECL-3211, that supports up to 64 stations and boasts a "universal" emulator: rather than change emulator hardware when a new chip is introduced, the system requires a software change and an adapter card to emulate any processor up to 32 bits wide. Tektronix has added the 8550 to its universal development system line—this one supports 23 microprocessors.

The development system market also attracted E-H International Inc., Oakland, Calif., which first intro-

Stritter: architect of the 68000

It's hard to think of semiconductor technology as a limiting factor, when the performance of yesteryear's large mainframe computers is now contained in small pieces of silicon. But that's how Edward P. (Skip) Stritter, chief architect of Motorola Inc.'s MC68000 microprocessor, views the design and development of that 16-bit system.

For all that he considers the 68000 "the best microprocessor available today in the marketplace, in terms of performance and ease of use," Stritter is less than ecstatic about its capabilities. "From a pure computer science point of view," he states, "we did a nice, but not astounding or revolutionary, job. That will have to wait until semiconductor technology comes to the point where it's truly not a restraint," in terms of how many functions can be provided in a given amount of silicon.

Now the systems architect at Nestar Systems Inc., Palo Alto, Calif., where he is applying microprocessor technology to designing microcomputer systems and networks, the 33-year-old Stritter recalls numerous barriers and tough decisions that turned the design and development of the 68000 into a large undertaking. "The biggest barrier was the huge conflict about what one wants to do as a computer architect and what one can do with a single-chip technology," he states.

Born and raised outside of Boston, Mass., Stritter received his undergraduate degree in mathematics from Dartmouth College in 1968, where he also got his first dose of serious software development. Next he joined Bell Laboratories and was immediately whisked off to Stanford University where he received his master's degree in computer science in 1969. Returning to Bell, he spent two years developing systems software, data-base systems, and, Stritter adds, "compiler-to-compiler sorts of things, all very primitive and rudimentary compared with what's happening today." Then it was back again to Stanford for his doctorate, which he obtained in 1976. During those five years, he also worked at the Stanford Linear Accelerator Center, a computation research group consisting of computer scientists and graduate students.

Finally, in early 1977, Stritter joined Motorola's Semiconductor Group in Austin, Texas, where the MC68000 project was about to begin. "Interestingly, although Motorola had built microprocessors before," he says, "this was the first time they consciously and explicitly looked to the computer sciences community for help in designing one."

One of the many hard decisions faced by Stritter and project leader Thomas Gunter—"a hardware and MOS technologist who learned to be an excellent computer architect"—was whether to make the 68000 compatible with existing Motorola products, such as its 8-bit 6800 family, or start from scratch with a brand new design. "We chose not to make an downwardly compatible design," he says, because "at some point we and the users would have to make a significant jump to the 16- and 32-bit world. We decided to bite the bullet and make that jump so it wouldn't be more painful at a later date."

An avid skier, bicycle rider, and lover of classical music, Stritter and his wife Cynthia live in Woodside, Calif., "up in the hills away from people," he says. But his friendliness and ability to motivate people on the job has paid big dividends at Motorola. In terms of computer science, he notes, "it was tough to get the hardware people to be creative and expand their technology. However, they did a fabulous job."

-Bruce LeBoss

duced an Intellec-compatible disk drive, followed by a stand-alone emulator and finally the minicomputer-based Microsupport system with built-in Winchester disk drive. A multiuser configuration is due in the coming year.

Of note on the low-cost development scene is AMI's Phoenix. It combines a Zenith Z89-based microsystem with assemblers for 37 different microprocessors and will add emulation support shortly. Zilog has added emulation capabilities to its Z8000 development system with its ZSCAN module, as has AMD on its System 8. AMD also now fully supports the 2900 bit-slice processor with their System 29. This system, like the System 8 for the Z8000, includes an integral logic analyser with full real-time trace support.

High-level languages

The UCSD all-Pascal software package has finally emerged from litigation with a new name. The UCSD System Software, now marketed and supported by Softech Microsystems, has added a Fortran compiler and is now available for a wide variety of microcomputers. It is an integrated operating system, editor, and high-level language. Softech has also been awarded the first Defense Department contract to develop a compiler for the language Ada, though initially this compiler will be written for DEC's VAX series.

The official specification for Ada has recently emerged in a July 1980 Government document entitled "Reference Manual for the Ada Programming Language." Both the U. S. Army and the Air Force will offer contracts to implement the language, Softech's effort being for the army. That first compiler will itself be written in Ada, as will all the utility programs designed to assist in program development. Also inevitable is Ada's use in nonmilitary industrial microsystems as well as on university campuses—in fact, Ada will be the system-level language for Intel's advanced 32-bit system, the iAPX432.

As high-level languages become more standardized, they, too, will appear in ROM. Many manufacturers now offer the Basic language in silicon—in fact, National's 8073 has it in the on-chip ROM.

Concurrent execution

A pressing concern of industrial users is the real-time control of multiple processes. This has spurred on the introduction of several software packages aimed at what is termed as concurrent execution. MicroConcurrent Pascal from Enertec Inc. of Lansdale, Pa., is for Z80-, 8085-, 8086-, and 1802-based machines, with support for many other processors on the way. Mostek has produced the Multiple Independent Task Executive. That operating system allows the Standard bus (STD) to be used in an interrupt-driven real-time multiple-process-control environment.

Davis: promoter of programmer productivity

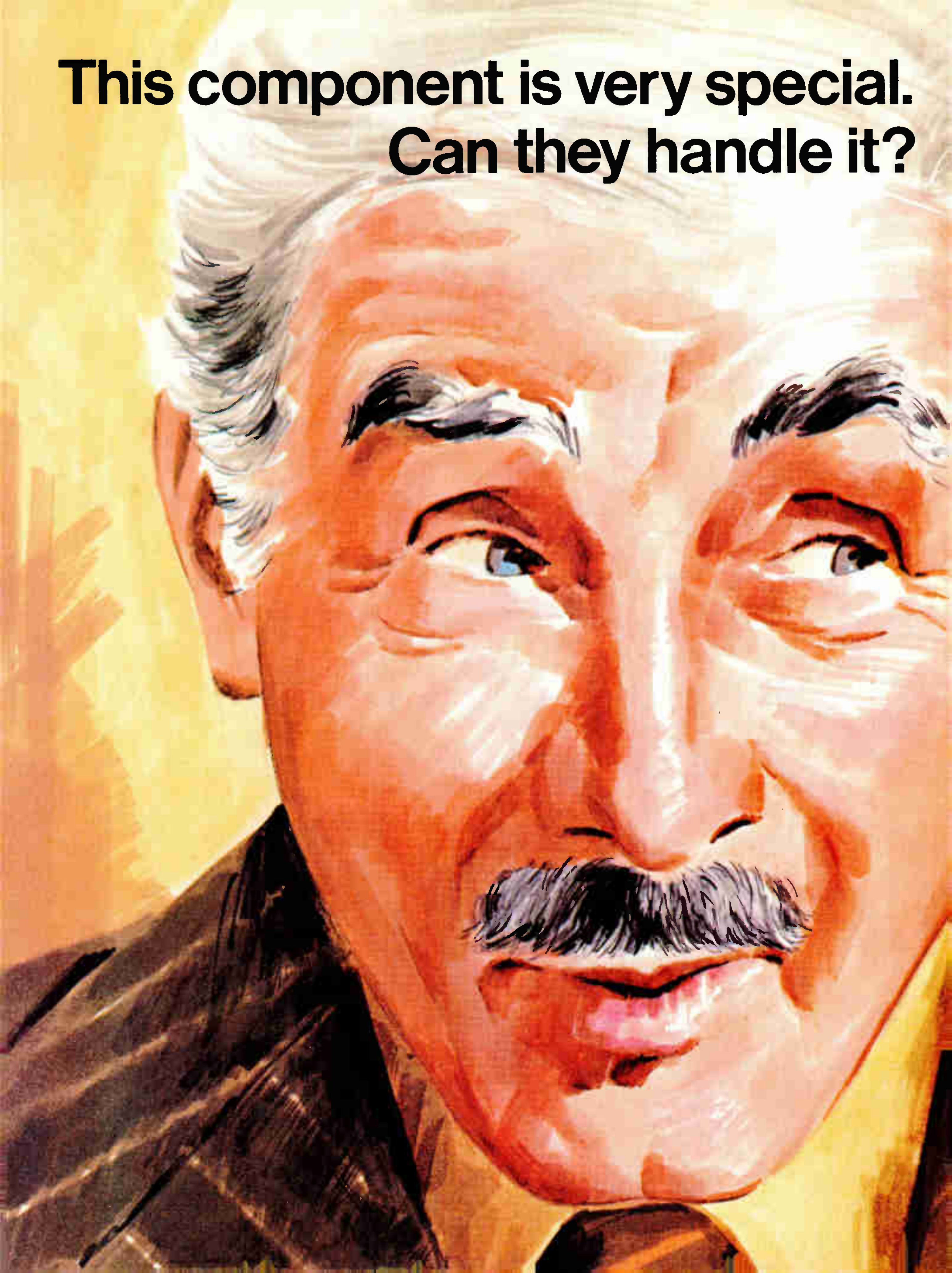
In May of last year, when American Microsystems Inc. canceled production of its ill-fated MDC microcomputer development system, a young project manager named Henry Davis was asked to come up with a low-cost alternative for its S2000 family of 4-bit controllers. He was still handling an all-Pascal software package called AMIX that turns Intel's, Motorola's, Tektronix', and Texas Instruments' development systems into universal ones, and that gave him a better idea. Since the Santa Clara, Calif., company was committed to developing all its own software anyway, why not offer AMIX on a microcomputer to form a low-cost universal development system?

Thus began the gestation of AMI's Phoenix I, a $5,495 system built around the Zenith Data Systems Z89 microcomputer that comprises a cathode-ray-tube display, a keyboard, and three minifloppy-disk drives. What really makes the system remarkable, however, is the magnitude of the software undertaking: Davis, working with a handful of programmers, has managed to produce 37 assemblers and two simulators for the Phoenix in little over a year—in all, 70,000 lines of assembly code and 200,000 lines of Pascal—some 10 times the amount generally regarded in industry as humanly possible for such a small group.

Davis's approach differed from others: "Rather than partitioning a project into smaller modules, I found the opposite far more effective," explains the 26-year-old manager of systems engineering. "What you want is one or two highly skilled people working very closely." The reason, he says, is that large groups spend too much time with communication problems.

Still, Davis will reveal little of the techniques he's used to speed software generation. Certainly, his designs don't skimp: the Phoenix, for example, boasts an elaborate screen editor whose capabilities rival that of far more expensive systems. "Research has shown that programmers spend 80% of the time editing," he maintains, "so having a fast editor speeds up software development time."

Davis has become an authority on the subject of software. He is mostly a self-made scholar who at age 16 taught his high-school teachers programming and attended two universities without ever acquiring a degree. But his unquenchable thirst for knowledge—he reads more than 100 new books, articles, and dissertations each month—keeps him on the leading edge. "Despite the alarms being raised, I don't foresee a software crisis. Though 10 times as much software will be needed by 1990, I expect to increase programmer productivity more than 10 times by then," declares Davis, who has authored three books and more than 50 papers on computer languages. **-R. Colin Johnson**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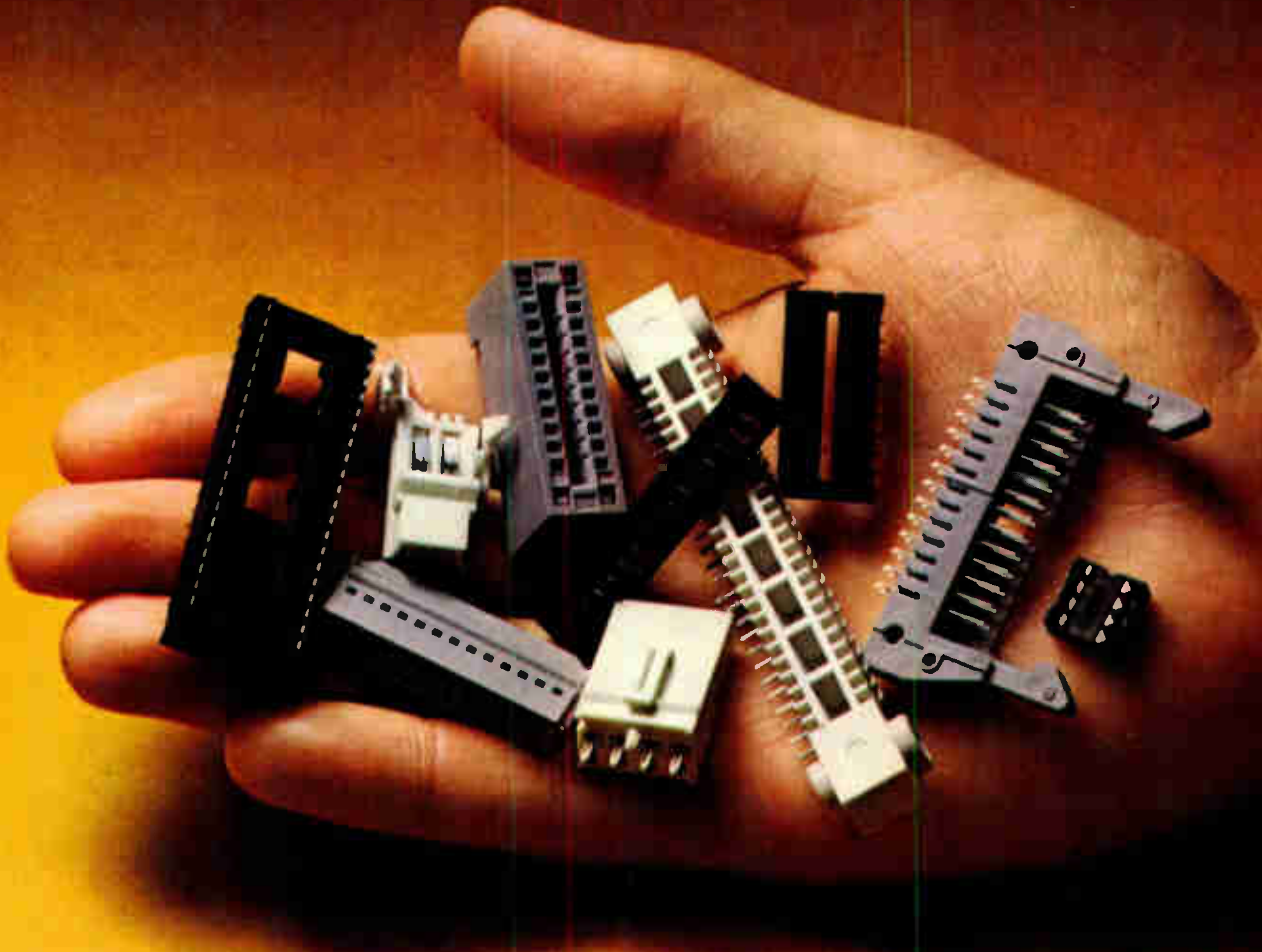

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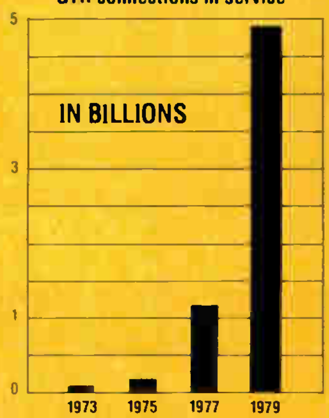

TYPICAL CONTACT RESISTANCE VALUES (Milliohms)

After Environmental Test–at Dry Circuit Levels. (Range of Values Within 99.9% Confidence Level)

Environmental Test	GTH Contacts	Conventional Geometry Contacts			
	Tin-Alloy Plate	15 Microinch Gold Flash	30 Microinch Gold Plate	50-100 Microinch Gold Plate	Tin or Tin-Alloy Plate
Initial	4.0 - 6.0	4.5 - 13.3	4.5 - 8.6	4.4 - 8.3	4.1 - 12.0
Thermal Shock	4.0 - 8.6	6.0 - 15.0	5.0 - 8.0	5.2 - 7.2	6.0 - 15.0
Humidity	4.5 - 7.0	10.1 - 31.8	5.0 - 9.0	4.9 - 8.8	5.3 - 75.1
Industrial Atmosphere	4.0 - 6.0	10.9 - 20.3	5.0 - 20.0	5.0 - 13.0	28.7 Open Circuit
Gas Tightness	4.0 - 6.5	Not Applicable	Not Applicable	Not Applicable	4.0 Open Circuit
Thermal Cycling	4.0 - 7.0	8.5 - 15.5	5.0 - 10	4.6 - 9.0	4.0 Open Circuit
Durability	4.0 - 5.5 (100 Cycles)	10.1 - 12.2 (100 Cycles)	5.0 - 9.0 (100 Cycles)	5.3 - 9.3 (500 Cycles)	13.9 - 57.9 (100 Cycles)
Vibration	4.0 - 5.5 (5-500-5 Hz)	9.0 - 15.0 (10-55-10 Hz)	4.0 - 8.0 (10-2000-10 Hz)	5.3 - 9.3 (10-2000-10 Hz)	4.0 - 15.0 10-55-10 Hz)

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interfacing problems.

Circle 169 on reader service card

COMPONENTS

The good news goes on; component performance and desnity continue to increase, with data converter ICs evolving into data acquisition systems, power MOS FETs upping their voltage levels, and displays shining brightly

by Roger Allan, *Components Editor*

Greater functional densities and higher performance levels continue to drive component technologies. Resistors, capacitors, inductors, transformers, and even sensors are being made more readily available in chip form. They sport performance levels nearly on a par with those of their larger discrete counterparts.

Monolithic data converters are not only cramming more functions on the same chip, but are evolving into miniature data-acquisition systems. And hybrid and modular data converters continue to capitalize on better monolithic data converter chips by using them for even higher-performance products.

Besides packing more power per square inch of silicon, discrete power devices, particularly field-effect transistors, are becoming more compatible with microprocessor circuits. Optimization of computer-aided designs is yielding a host of different power MOS FET geometries, each with its own combination of lower on-resistance and higher breakdown voltage advantages.

In display technology, liquid-crystal, light-emitting-diode, and vacuum fluorescent displays are showing more and brighter colors and larger characters at lower costs. Gas-discharge and ac thin-film electroluminescent displays are also gaining momentum in the market.

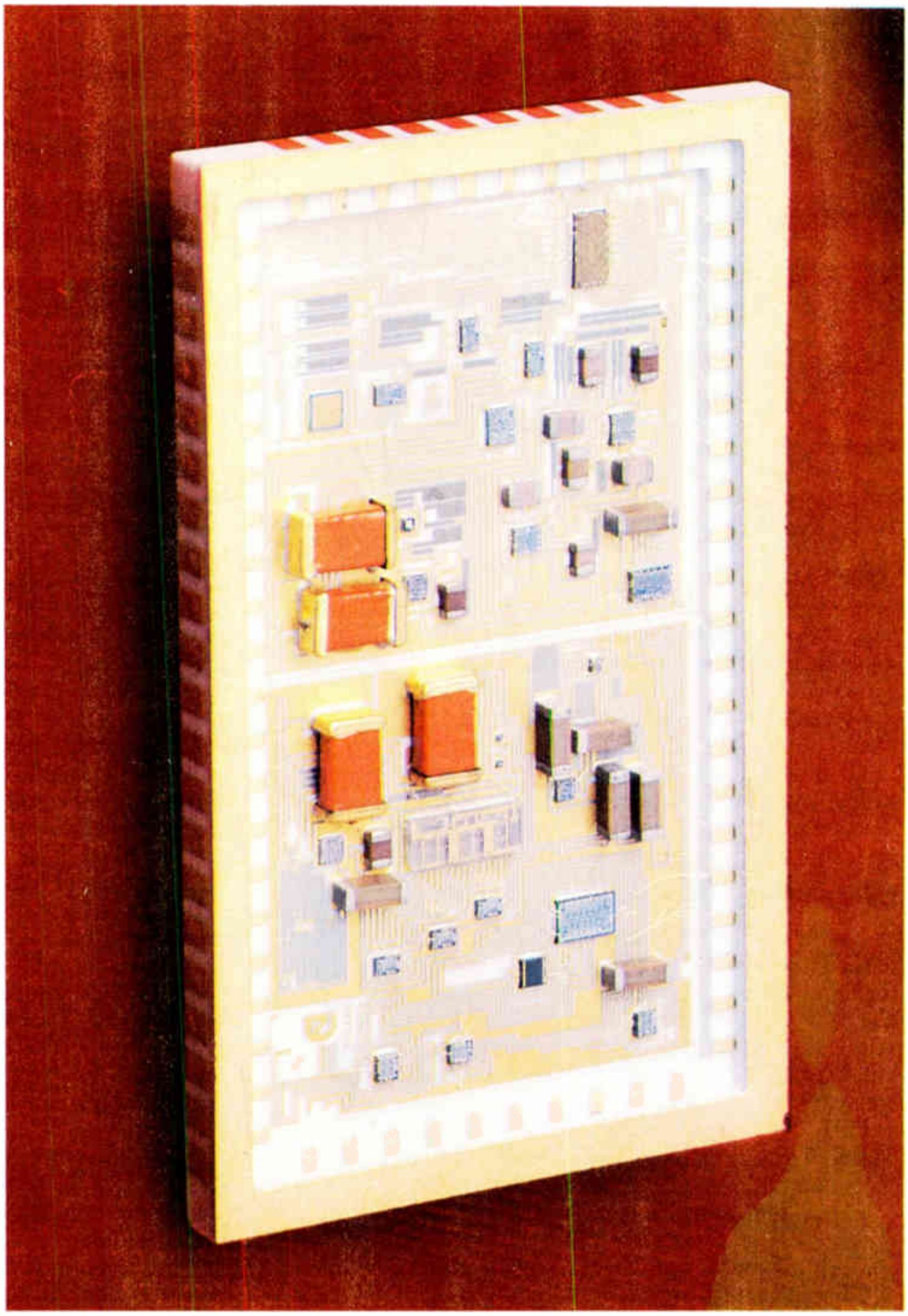
Chip components proliferating

Historically, chip components were largely limited to high-performance hybrid circuits, many of which were designed to satisfy high-reliability and space-hungry applications like those encountered in the military. This picture has changed dramatically, now that more components with wider performance ranges are becoming available as integrated circuits. Inductors, transformers, and sensors, to name a few, are being offered in chip form, albeit in limited performance ranges (values, breakdown voltages, and so on) when compared with their big-brother discrete components.

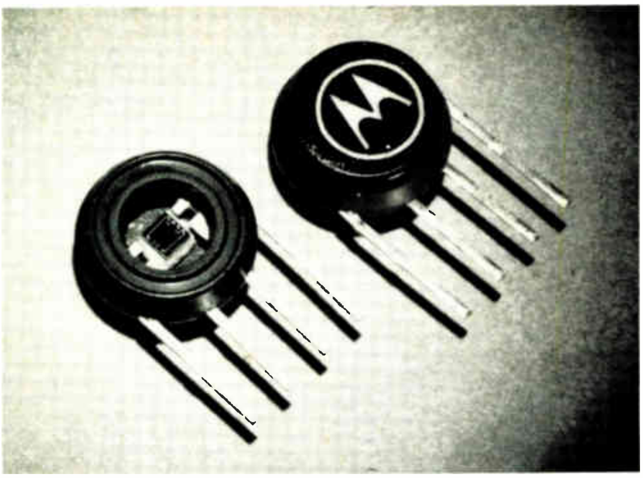
Even industrial chip sensors like the Aquamax thin-film moisture-sensing IC from Panametrics Inc., Waltham, Mass., are helping boost chip reliabilities. When placed inside an IC package, the device determines moisture variations in the package by measuring the resultant impedance changes.

Many monolithic IC manufacturers are actively working on temperature- and pressure-sensing chips for industrial, automotive, and consumer applications, although in the case of pressure-sensing chips, packaging constraints limit their availability in pure chip form. Sensor-chip packaging and testing has now been simplified (and is thus lower-priced and more widely useful) by Motorola Inc.'s Semiconductor Group, Phoenix, Ariz., with the development of the X-ducer. This monolithic sensor uses a cross-shaped sensing element, rather than a Wheatstone bridge, cutting the cost. In addition, the plastic package—really a chip-carrier—simplifies lead terminations, thereby easing testing. Although initially targeted for industrial and automotive uses, the X-ducer is foreseen as fulfilling a vast potential consumer market based on microprocessor circuits.

This year, using dielectric isolation, Dionics Inc., Westbury, N. Y., perfected an array of photovoltaic



Complete. Hybrid data-acquisition systems are being squeezed down in size, yet maintaining high-performance levels, like this HDAS-16MC from Datel-Intersil. The 16-channel 12-bit system is available in a hermetically sealed 62-pin package 2.3 by 1.4 by 0.24 inches in size. It has a minimum throughput rate of 50 kilohertz.



Practical. The X-ducer pressure-sensing silicon chip from Motorola Inc.'s Semiconductor Group has made inexpensive pressure-sensing components practical. A single X-shaped silicon element is used for sensing and is housed in a plastic package.

diode chips with an output of up to 8 volts, a vast improvement over the 0.5 V generally available from such chips. The DI-16V8 16-diode array, on a chip 35 by 40 mils, opens up potential markets for isolated solid-state switching.

Spectacular advances are being made in analog-to-digital and digital-to-analog converters, spanning the three broad areas of process technology—monolithic, hybrid, and modular. In monolithic form, d-a converters with up to 12 bits of resolution and a-d converters with up to 10 bits of resolution are routinely available.

Converter activity is hectic

One of the many examples of more-complete monolithic data converters is the 10-bit NE5020 d-a unit from Signetics Corp., Sunnyvale, Calif. Housed in a 24-pin DIP, it features 10-bit accuracy and includes the voltage reference, application resistors, input buffer, output amplifier, and data latches necessary for microprocessor compatibility.

First mentioned at this year's International Solid State Circuits Conference, Analog Devices Inc., Norwood, Mass., introduced an 8-bit monolithic d-a converter that operates from a single 5-V supply and is microprocessor-compatible. The AD558 DacPort includes a reference, data latches, and an output amplifier.

Complementary-MOS a-d and d-a units are making a bid for the monolithic converter market. The 12-bit-plus-sign C-MOS a-d converter design National Semiconductor Corp., Santa Clara, Calif., achieved this year and discussed at the ISSCC is but one indication of this trend.

Integrating-type C-MOS a-d converters have been available for several years from such companies as Intersil, Texas Instruments, NEC Microcomputers, and Analog Devices. These ICs have made possible hand-held digital panel meters that can run on small batteries. Intersil, a leader in this type of device, showed how low in power dissipation C-MOS chips can be. Its 3½-digit ICL7126 dissipates less than 1 milliwatt from a 9-V transistor-radio battery. The maximum power dissipation is 900 microwatts, and operation from a 9-V battery is for 8,000 hours (over one and a half months of continuous operation).

More recently, the Cupertino, Calif., company introduced a larger, 4½-digit unit containing nearly all the necessary parts for a total DPM, save for external reference, clock, and display with decoder-drivers. The ICL7135 features an accuracy to within ±1 part in 20,000 counts and is microprocessor-compatible.

Converter subsystems advance

As impressive as monolithic converter activity is, subsystem components like voltage references, sample-and-hold amplifiers, and comparators are establishing new performance frontiers. At this year's ISSCC, Plessey Research Ltd., Towcester, Northants., England, unveiled an 8-bit monolithic d-a converter chip with an incredible settling time of just 5 nanoseconds. Intended as a building-block component for a monolithic, successive-approximation 8-bit 15-megahertz a-d unit, it differs from conventional d-a converter subsystem chips in that it has all of the analog components needed for an a-d converter operating at video speeds: the voltage reference, output amplifier, and comparator. The comparator itself, a latched type, is worthy of note. Its propagation delay is a lightning-fast 1.3 ns.

On the subject of video-speed monolithic converters, TRW LSI Products, El Segundo, Calif., continues to be a leader in this arena, making 30-MHz a-d converters with up to 8 bits of accuracy. The firm also has 20-MHz monolithic d-a converters with up to 10 bits of accuracy and hopes to achieve 10-bit 10-MHz a-d conversion on a chip sometime this year.

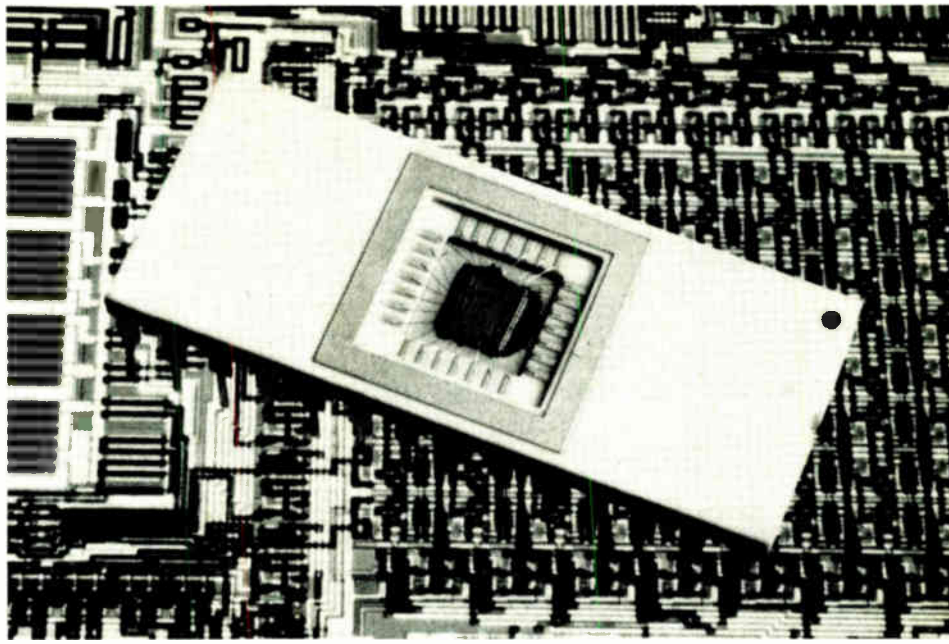
Other makers of monolithic converters either have been in this high-speed video conversion market and are now redoubling their efforts or are trying to establish a foothold. Notable are Motorola, Harris, Ferranti, and Siemens. In fact, Munich-based Siemens AG recently showed off its SDA5010, a 6-bit 110-MHz a-d chip that converts in 10 ns. The bipolar device can be paralleled for resolutions of 7 bits or more without affecting its 110-MHz sampling rate.

Motorola, which last year introduced a 10-ns 8-bit bipolar monolithic d-a converter, plans to introduce this year samples of a 7-bit a-d version, the 10317, that operates at 30 MHz. Harris Corp.'s Semiconductor Products division, Melbourne, Fla., has shown off its 50-ns HI-5618 C-MOS a-d converter. The 8-bit device is designed for accuracy to within ±¼ least significant bit over both the commercial and the military operating temperature range.

High hybrid performance

The most advanced monolithic data converters are eagerly gobbled up by hybrid converter makers (some of whom design their own chips) and put to use in hybrid circuits for even greater performance. Because hybrid converter technology is flexible—that is, a wide choice of chip and discrete components is available—individual circuit functions can readily be optimized to achieve increased performance.

The highest-performance high-speed video data converters, such as those made by Analog Devices' Comput-



Memory. The first monolithic data-acquisition subsystem to include memory is the AD7581 eight-channel unit from Analog Devices, with an 8-by-8-bit dual memory port. Interfaceable with most popular microprocessors, it also contains an 8-bit successive-approximation a-d converter and an eight-channel multiplexer.

er Labs division, Greensboro, N. C., are generally hybrid or modular in form. Units like the firm's Bare Bones 9000 series CLB1310 (13 bits at 10 MHz), MOD4100 (4 bits at 100 MHz), and MOD1205 (12 bits at 5 MHz) set the pace for the fastest video a-d converters. Recent entries from the firm are the HDO810C and the HDD1015C, hybrid 8- and 10-bit d-a converters, respectively, in dual-width DIPs for the lucrative raster-scanning cathode-ray-tube market. These devices offer rapid settling times of 10 ns to 0.2% of full scale and low-glitch energy outputs of 200 picovolt-seconds maximum. The outputs are 1-V composite-blanking signals terminated for 75-Ω impedances.

A milestone in linearity for hybrid data converters was reached when Hybrid Systems Corp., Bedford, Mass., unveiled an 18-bit d-a unit. On the DAC-370-18's alumina substrate are two chips: a custom C-MOS switch network the company designed and a laser-trimmed thin-film resistor ladder network. The part is the first of its kind to offer 16 bits of linearity and dissipate only 50 mW from a double-width DIP. Containing input latches for interfacing with microprocessor circuits, it is priced at just $210 each for orders of 100 units or more.

Among hybrid converter manufacturers offering 16-bit d-a units is Burr-Brown Research Corp., Tucson, Ariz., with its 16-bit DAC73. Introduced this year, the part exemplifies the kind of performance a hybrid design is capable of achieving: nonlinearity is just 0.0008% of full scale.

Earlier in the year, Hybrid Systems introduced a 16-bit hybrid d-a converter in a double-width 24-pin DIP with a guaranteed linearity to within 0.008% of full scale (±½ least significant bit). The two-chip 9331-16, which dissipates a maximum of 50 mW, settles in 1 microsecond and is priced at a surprisingly low $99 each for 100-lot quantities.

Micro Networks Corp., Worcester, Mass., unveiled this year a truly high-performance 12-bit hybrid d-a converter in its MN3348. The part is guaranteed for a maximum total error of ±0.075% of full scale (including errors due to gain, offset, and nonlinearity) over the operating temperature range of 0° to 70°C without any user adjustments. A military version to operate between −55° and +125°C has a maximum total error of just ±0.1% of full scale. Nonlinearity for both versions is ±0.024% and ±0.048% of full scale, respectively. Of course, should the user desire even greater accuracy, optional adjustments are available to accomplish that. Included in the converter's 24-pin package are a voltage reference, an output amplifier, a resistor ladder network, and switches.

A late entry is the MN5700, a 12-bit hybrid a-d converter from Micro Networks that operates at an ambient temperature of up to 200°C. Also in the works from Micro Networks is a 16-bit d-a converter in hybrid form with 16 bits of accuracy over the entire military temperature range of −55° to +125°C. Because of the complexity of designing and building such a part, the company does not expect to have it ready for at least two more years.

Many hybrid 8- and 10-bit a-d converters are available with speeds of under 1 μs. The successive-approximation 8-bit ADC-815 from Datel-Intersil Inc., Mansfield, Mass., is one such unit. It has a blazing 600-ns conversion time to within ±½ LSB and includes a precision reference, a clock, a comparator, registers, and a current-output d-a converter.

At the 12-bit level, many hybrid a-d converters are achieving conversion times of just a few microseconds. Analog Devices' complete 12-bit model AD578 is a multiple-chip device with 4-μs conversion time and ±0.012% maximum nonlinearity. All necessary a-d conversion components—comparator, reference, clock, and so on—are included on the DIP carrier.

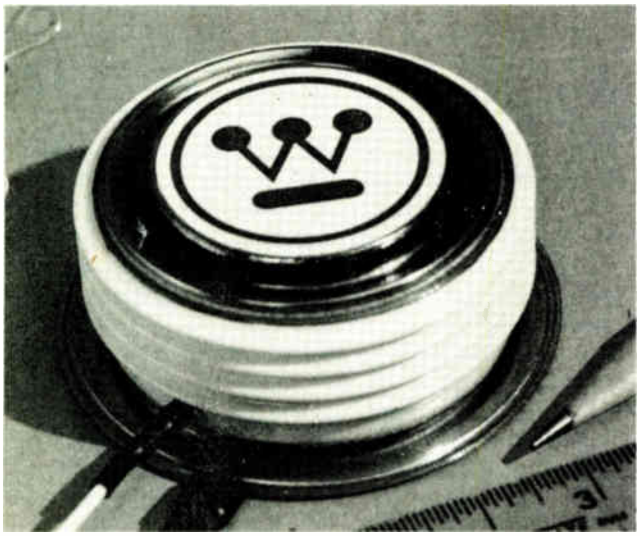
Even faster is the Datel-Intersil ADC-817 12-bit successive-approximation a-d unit. Its maximum conversion time is 2 μs over both commercial and military operating temperature ranges. According to John Donovan, product marketing specialist for data conversion products, "The ADC-817 demonstrates the maturity level hybrid converter technology has attained. The technology can now handle nearly any task asked of it."

To make even better-performing units, many data converter designers are coming up with innovative designs, some of which borrow from older conversion principles once considered impractical. Teledyne Philbrick, Dedham, Mass., for example, took the familiar successive-approximation a-d conversion technique and modified it in its model 4134 12-bit hybrid device for a typical conversion speed of 1.9 μs. Conversion time was shortened by the use of a sense-and-clock circuit that speeds up the converter's clock rate for all bits after the third one.

Innovative designs flourish

In yet another twist, Datel-Intersil recently unveiled an 8-bit hybrid successive-approximation a-d converter that uses an error-distribution scheme resulting in 12-bit linearity. Essentially the ADC-881 overcomes the effects of its own nonlinearity. It does so by scattering linearity errors over its full-scale range. By averaging out these errors over a large number of samples, a highly linear signal results. According to the company, the resultant output is more than 11 times more linear than comparable 8-bit converters. For example, integral and differential nonlinearities are just 0.0087% of full scale (0.022 LSB). The device, which has a 1.5-μs maximum conversion time, is designed for applications where analog signals are buried in noisy environments. It is part of the firm's new line of what it calls Super Modules—data-conversion products employing discrete, hybrid, and monolithic components.

As always, the highest-performance data converters can only be found in modules that use discrete components like highly precise resistors. Analogic Corp., Wakefield, Mass., introduced one such ultralinear high-performance product in its MP1926. The 16-bit modular d-a converter has the analog equivalent of 18 bits of linearity for applications in audio digitizing, where a wide dynamic range is needed and linearity levels must be very high. It converts in 3 μs and has a total drift from all error sources of less than 1 ppm/°C and a total harmonic distortion of less than 0.005%, measured with a deglitched amplifier. The worst mid-range nonlinearity is ±¼ LSB.



Powerful. This T72H silicon controlled rectifier from Westinghouse Electric Corp.'s Semiconductor division exemplifies the kind of levels power semiconductors are attaining. It handles 1,200 volts at 400 amperes and turns off in 10 microseconds.

Data acquisition booms

Nearly every data converter manufacturer, regardless of the technology it uses, is busy trying to cash in on the booming market in data-acquisition products. In fact, these subsystems are the next level upward for data converters. Many multiple-channel data-acquisition products are available in small DIPs, where the emphasis is on trying to pack more performance in yet smaller cases. This year, Harris took an unconventional approach in packaging a multichannel data-acquisition system by placing its eight-channel 50-kilohertz differential 12-bit system in two DIPs. Each package holds several leadless chip-carrier ICs. One DIP, the HI5900 analog-signal processor, has software-programmable gain and sample-and-hold amplifiers. The other, the HI5712 8-μs successive-approximation a-d converter, has a differential nonlinearity of ±½ LSB over the entire military operating temperature range. The leadless chip-carrier ICs are mounted on both sides of each DIP's ceramic substrate. The chip-mounting technique simplifies IC reworking and increases product yields by allowing individual testing of ICs before each is mounted into the chip-carrier.

Analog Devices has just unveiled the first microprocessor-compatible monolithic data-acquisition subsystem with on-chip random-access memory. Designated the AD7581, it contains an 8-bit successive-approximation a-d converter, an eight-channel multiplexer, and an 8-by-8-bit dual-port RAM.

Datel-Intersil has a 50-kHz 12-bit 8-channel differential data-acquisition system, the HDAS-8MC, in a single package. The hybrid is available in a 62-pin package with dimensions of a mere 2.3 by 1.4 by 0.24 inch. A 16-channel single-ended version, the HDAS-16MC, is available in the same size package.

As with data converters, the route to higher performance levels for data-acquisition systems is modular. One example is the 250-kHz throughput rates Datel-Intersil offers in its modular DAS250 16-channel 12-bit units.

Power devices with a greater punch

For power MOS field-effect transistors, the two major technological trends are lower on-resistances and higher breakdown voltages. These have reached the tens of milliohms and hundreds of volts, respectively. Also, the push is on to reduce the power MOS FET's comparatively higher price when stacked up against a bipolar power transistor. And prices have already descended to new levels. The VN4000A/VN4001A vertical-MOS FETs from Siliconix are selling for $9.05 and $8.60 each, respectively, in 1,000-piece lots. Such prices, according to Siliconix, a pioneer in V-MOS power FET technology, compete with those of comparable bipolar parts. The

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PM3216 35MHz Single Time Base Scope
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PM3262 100MHz Dual Trace Universal Scope
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Inset at right: PM3262 100MHz Dual Trace Universal Scope

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PM3540 10MHz Logic Analyzer with 25MHz Real Time Scope
PM3500 100MHz 16-Channel Logic State and Timing Analyzer

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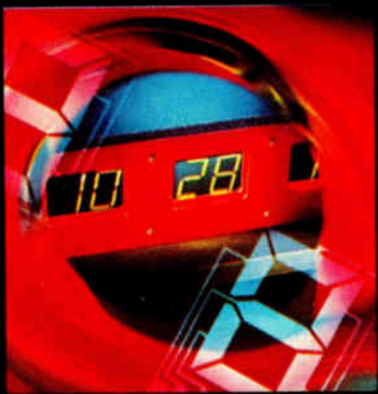
Circle 177 on reader service card



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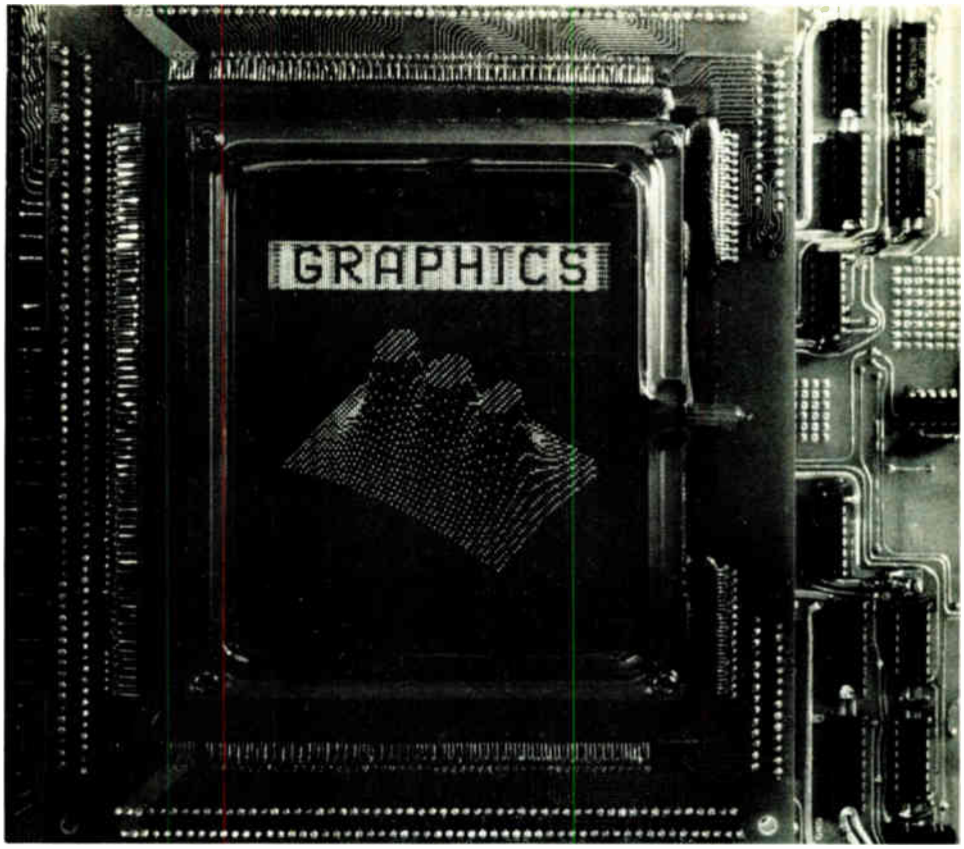

Graphics. Vacuum fluorescent displays can now deliver high-quality graphics thanks to a driving technique from Japan's Ise Electronics Corp. that increases resolution. The technique avoids the usual shadow effects that had hobbled the acceptance of such displays for graphics.

two V-MOS devices are rated for on-resistances of 1.0 and 1.5 Ω, respectively, and have a breakdown voltage of 400 V. Their continuous-current rating is 8 amperes (16 A maximum pulsed current).

Competition in power MOS FETs is also coming from overseas. This year, Siemens announced power MOS FETs made with its Sipmos (for Siemens power MOS) technology. Sipmos FETs offer on-resistances as low as 0.03 Ω and breakdown voltages up to 1,000 V. Equally important is the fact that they can be driven from 5-V TTL signals, making them more compatible with low-signal-level circuits.

Discrete power thyristor components are also getting faster and are able to handle heavier work loads. Notable is the T72H Hockey-puk silicon controlled rectifier from Westinghouse Electric Corp.'s Semiconductor division, Youngwood, Pa. The device is the industry's first SCR with a 1,200-V, 400-A (average) rating and a turn-off time of 10 μs.

A multiplicity of displays

There are now so many display technologies that either have reached maturity or are close to that point that it is difficult for a designer not to find the right technical choice for an application. The trend is into the "big picture" of flat-panel displays capable of displaying hundreds of alphanumeric and graphic characters.

In liquid-crystal displays, the activity is nothing short of frantic, with large companies consolidating their hold on the technology by buying out smaller ones. As a result of the increased competition, some LCD makers like Motorola have dropped out of the business. A large part of the competition is coming from Japan, where researchers are fast developing flat-panel LCDs, some of which are in color.

One lucrative LCD market that has yet to be tapped to any significant extent is automotive displays. However, LCD makers are feverishly trying to crack that market, now largely dominated by vacuum fluorescent displays and light-emitting diodes, by offering improved-performance dichroic color LCDs.

As for LEDs, device efficiencies are being pushed to the limit. General Instrument Corp.'s Optoelectronics division, Palo Alto, Calif., for example, showed off its Illuminator series of orange, yellow, and green LEDs (the orange can be filtered to red) earlier this year, with outputs an order of magnitude greater than offered by conventional high-efficiency LEDs. The gallium phosphide devices put out 100 millicandelas and can accept up to 0.5 watt of input power, figures comparable to those of commonly used incandescent displays.

The marriage of the microprocessor and display technology is particularly evident in LED displays, where a crop of intelligent interactive displays has arisen. Litronix Inc., Cupertino, Calif., which was the first to introduce the concept of the intelligent LED display three years ago, recently introduced the DL-3416, a four-character alphanumeric module with 0.225-in.-high LEDs. Despite their small heights, the displays can be viewed from as far back as 8 feet, thanks to an encapsulated magnifying lens covering them. The DL-3416 has a number of intelligent display functions that can be driven from a microprocessor circuit.

Another recent intelligent and interactive LED display is the BDS2724 from General Instrument Optoelectronics. The 24-character alphanumeric system is operated under the control of an on-board 8048 microprocessor or 8748 microcomputer.

Electroluminescents brighten

Despite the fact that many display researchers had practically given up on thin-film ac electroluminescent displays as impractical, some, like Japan's Sharp Corp. and Rockwell International Corp. have shown promising results. In fact, Sharp this year began offering samples of flat-panel thin-film ac electroluminescent displays. The samples feature improvements in display lifetimes and brightness levels, two key performance parameters that previously held back this technology.

A principle reason why excitement is shaping up about thin-film ac electroluminescent technology for flat-panel displays is the simplicity of the thin-film process, leading to truly low-cost large panels. Still, much work needs to be done in formulating the right kind of driver circuits, as well as in improving the display's operating lifetimes and brightness levels, before this technology can begin to take off.

The drive problem relates to the fact that most gaseous types of display require high voltages on the order of 100 to 200 V to operate, and achieving complex high-voltage drivers in IC form is difficult.

On the subject of drivers, a number of techniques are being investigated to reduce the drive complexities (and hence the costs) of LCDs and LED displays. A notable achievement in this area is AEG-Telefunken's Datacomp data-compression technique, which promises to reduce radically the number of control and address lines for both types of display. The Heilbronn, West Germany–based electrical and electronics giant feels that a Datacomp driver IC can replace five or six lines with as few as two or three. For large numbers of lines, the savings may be as high as 90%.

The data-compression techniques uses two binary states, plus an open-line state that acts as an active source of information. It is similar to the conventional three-state logic scheme; in AEG-Telefunken's technique, however, the normally passive third state conveys information.

Vacuum fluorescent display technology got a boost earlier this year from Japan: Ise Electronics Corp. described at this year's Society for Information Display meeting a driving technique that avoids the usual shadow effects found in vacumm fluorescent displays, limiting their resolution. The new technique reportedly increases resolution, making this display type suitable for graphics applications.

Fergason: pioneer in liquid-crystal displays

The fact that liquid-crystal displays are omnipresent is a credit to the inventive mind of James Lee Fergason, president of American Liquid Xtal Chemical Corp., Kent, Ohio, and frequently called the father of LCDs. It was back in 1970 that he filed for patents for a twisted-nematic device, a new kind of LCD that was to revolutionize display technology. His twisted-nematic LCD, which is the overwhelming worldwide choice of LCD makers, was in the first commercial products (watches) to use liquid-crystal displays when Fergason's International Liquid Crystal Co. (Ilixco), Warrensville, Ohio, introduced it in 1972. By then, Ilixco had perfected a practical LCD process now used by scores of other manufacturers.

In the August 1964 issue of Scientific American, Fergason wrote that, "though their existence has been known for more than 70 years, [liquid crystals] have until recently been regarded more as laboratory curiosities than as potentially useful or theoretically important subjects of study." He noted that the results of new studies pointed to a number of possible applications.

It was in that article that Fergason clarified the behavior of nematic liquid crystals, field-effect materials that react to the application of an electromagnetic field. He based his observations on studies he had performed between 1956 and 1966 at the Westinghouse Research Laboratories, Pittsburgh. He went on to become associate director of the Liquid Crystal Institute of Kent State University, Kent, Ohio, until 1970, when he formed Ilixco.

Ilixco refined twisted-nematic LCDs in 1971, developing the nondepolarizing-background concept for improved brightness and contrast levels. A year later, Fergason's team solved the problem of uneven contrast levels caused by the reverse twist and tilt phenomena of these displays. In 1974, he sold his patent rights to Basle, Switzerland–based Hoffman-LaRoche, which subsequently became entangled with Ilixco in litigation dealing with patent payment rights. The case was settled in 1976, when it was established that Fergason was the inventor of twisted-nematic LCDs and the owner of patents for them. By then, however, Ilixco had gone out of business and American Liquid Xtal had been formed in 1975.

A physicist with a bachelor's degree in physics from the University of Missouri, Columbia, in 1956, Fergason is still active in liquid-crystal material research and development. This week, for example, at the Biennial Display Research Conference, Cherry Hill, N. J., he will describe a display construction technique that allows liquid-crystal materials to respond to modulating signals in less than 50 microseconds. This development could have far-reaching consequences for LCD use as high-speed TV displays.

Married and the father of four children, Fergason proudly points out that his business is a family affair: his eldest daughter, Teresa, 22, is taking part in his firm's research efforts.

-Roger Allan

SCIENCE/SCOPE

Water levels in cooling systems of nuclear reactors may be monitored more reliably, especially during an emergency core shutdown, by an innovative metal-coated optical fiber developed by Hughes. The thin glass thread, some 1000 of which would be placed around a reactor's core, is tipped with a sapphire retroreflector. Unlike plastic-coated fibers, it can withstand the harsh reactor environment of temperatures as high as 350°C and pressures up to 1800 pounds per square inch. Compared to resistive level sensors now in use, the fiber is a model of simplicity. The sapphire tip, when dry, reflects light transmitted through the fiber; when wet, it reflects no light. Prototype sensors were developed under Nuclear Regulatory Commission sponsorship.

Nearly 25 orbit-years of flawless service have been accumulated by radiative coolers built for weather satellites in synchronous orbit. These devices are used to passively cool infrared detector arrays to less than 75K. They are far more reliable than mechanical refrigerators because they have no moving parts. They also require no power for operation. Radiative coolers built by the Santa Barbara Research Center, a Hughes subsidiary, have suffered no degradation in performance due to contamination. Since pioneering development of staged radiative coolers in 1966, SBRC has won six separate contracts to provide these devices. Designs qualified for space flight include a unit for an interplanetary mission to Jupiter and another for an earth resources satellite.

Military field technicians can test digital circuit cards containing large-scale integrated circuits with a new portable semi-automatic system. The Hughes HMC-193 Microcat, a microcomputer-aided tester, uses troubleshooting data stored on magnetic program tapes to guide a technician quickly to defective components. It uses universal adapters to route test signals and power, thus eliminating the need for unique adapters. Microcat can be taken anywhere in its shockmounted case and operated in just about any environment.

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Special uses of fiber-optics are growing with the development of a highly reliable connector that doubles the efficiency of earlier links. The device precisely aligns the ends of two laser-light-carrying fibers while maintaining a gap of only one-thousandth of an inch. (Ideally the fibers should be butted, except scratches caused by shock or vibration would reduce transmission efficiency.) The result is a coupling that is better than 70 percent efficient. The new Hughes connector also has a special seal to prevent contaminants and moisture from leaking in and impairing fiber performance.

Expanding the parameters

Design the backpanel you want with Elfab modular systems.

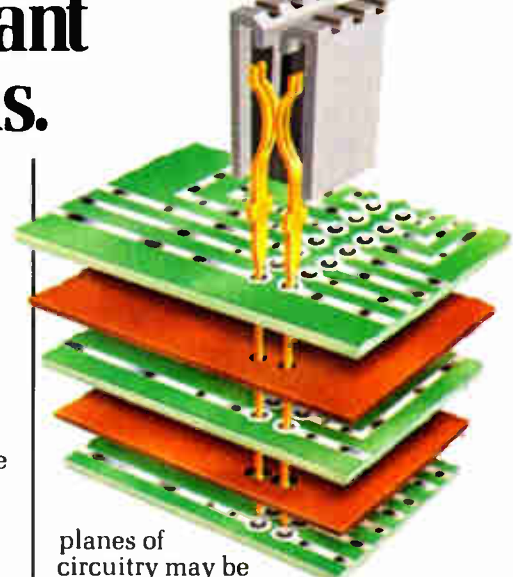
Your design flexibilty is virtually unlimited when you utilize Elfab's modular, press-fit systems. And, with press-fit technology, it's easy to stay within reasonable production budgets while you get the superb reliability demanded by today's applications.

Key to the excellent reliability of the press-fit system is the gas tight joint formed as the contact pin, with a rectangular interface section or "bullet," is pressed through a plated-thru hole in the PC Board. The diagonal of the bullet is slightly larger than the diameter of the plated-thru hole, so that the hard phosphor bronze pin deforms the softer copper, forcing the copper plating to conform totally to the pin. Four complete lines of contact asperities run the full depth of the hole. The reliability of the Elfab press-fit is proven. With more than 500,000,000 contacts now in service—and that number growing at a rate of more than 1,500,000 every day—not a single interface failure has ever been reported.

Basically, an Elfab modular system is composed of the PC board, contact pin, and insulator connector housing. You have the flexibility to interconnect to as many voltage, ground and signal planes as you need. Standard options are available in sufficient numbers to cover almost any application. But if your design calls for a special configuration, almost any adaptation can be made—and with all the reliability and economy for which Elfab press-fit systems are noted.

Let's start the design of your system with the printed circuit board. A basic system would start with a single-board, card-edge backpanel. Two layers of etched circuitry may take the place of part or all external wiring. Plated-thru holes accept the contact pins, making the board a structural part of the connector. Since no soldering of contacts is required, this system can effect savings of 5-10% over conventional soldering methods.

To achieve maximum circuit density, just stack additional boards together; all held fast by the press-fit contacts. Up to eight

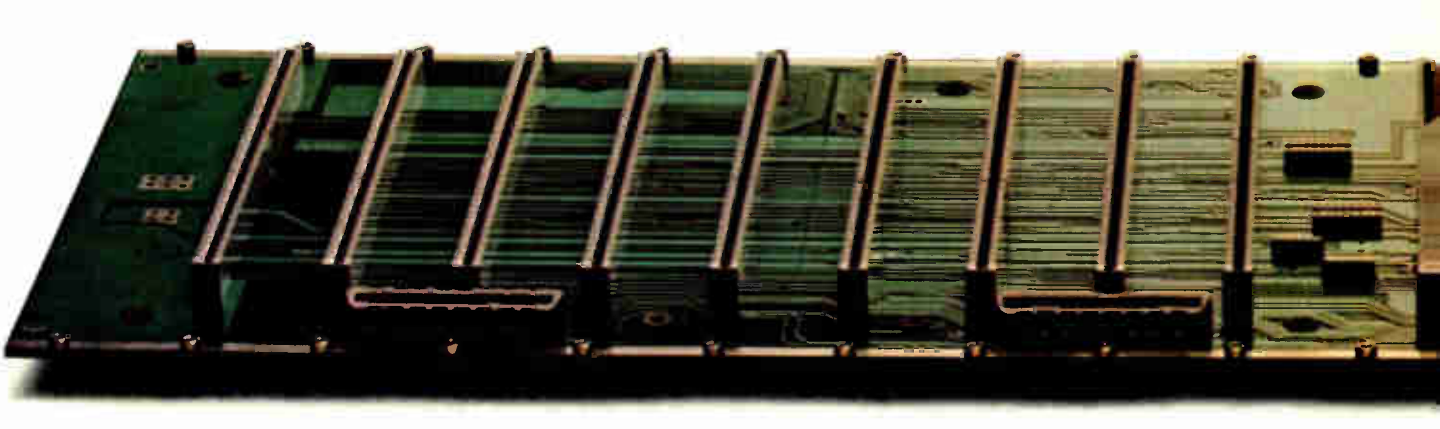


planes of circuitry may be used without any external wiring. This method is much more economical and much more flexible than the traditional laminated boards or metal plate and discrete connector assemblies.

Need extra high current capacity or positive voltage control? Make a hybrid out of the stack with pure copper insulated planes. This is excellent for today's high speed logic circuits. Select your own input/output specifications.

If electro-magnetic sensitive components are utilized, low-carbon steel sheets may be used between circuit layers for EMI, RFI shielding.

In short, whatever your circuitry



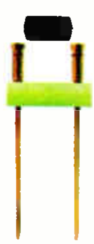
# of press-fit technology

requirements, you can get them in a compact package using Elfab's press-fit boards.

You can also select the exact contact pin to meet your requirements. Basic shapes for card-edge connectors include both cantilever and bellows contacts. The bellows contact has been made available in press-fit application by an innovation in production technique. The pin is placed in the plated-thru hole, then pulled into position to complete the gas-tight joint.

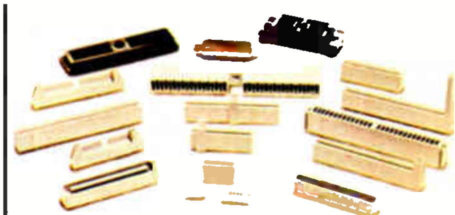
For customers with the volume to justify it, bellows contacts and insulator housings can be supplied, along with assembly equipment, so you can make your own backpanels.

Other contact pins available include: the straight post for applications which require a feed-thru I/O or access to signal or ground planes; the conventional screw machine contact for I.C. sockets; and many other contacts for specific purposes such as those for DIP sockets, "D" subminiature, etc.



A unique feature of all press-fit contacts is that they are removeable and replaceable on the board. And, growing in importance is the selective plating feature. Gold plating over base nickel is applied selectively to put the gold just where it's needed.

Insulator connector housings can be of just about any configuration you need. Standard edge-board connectors come in a choice of seven grid spacings—from .100" x .100" to .200" x .200". Modular construction makes length completely at your option with no special tooling required. Specialty configurations include: Dual In-Line packaging, "D" Subminiature, Ribbon Cable, 25 pair telephone and communications connectors, end and center connector card guides, DL connectors with "zero insertion force," and others as required.



Put these elements together, and you have the most flexible, economical and reliable backpanel system in the industry. It allows you the creative freedom to expand your own design parameters through Elfab's press-fit technology. It's what we're working for at Elfab. Write or call for application assistance.

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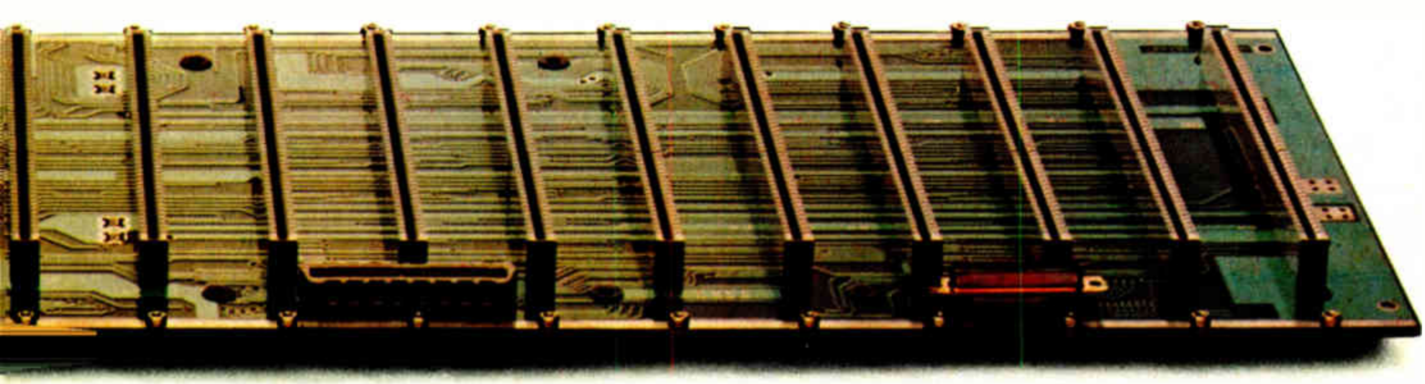


TEST & MEASUREMENT

Besides pushing speed and accuracy to new heights, instrument makers have been busy automating the measurement process, tying their equipment into multiuser, multifunction networks

by Richard W. Comerford, *Test, Measurement & Control Editor*

In their race to obtain more accurate data faster, instrument designers surged ahead on all fronts this past year. New programming and automating features were added to items like the signal generator and oscilloscope, and a host of manufacturers introduced instruments suited to the IEEE-488 bus. These included bus controllers, synchronization and network analysis gear, digital multimeters, and signal sources, as well as complete data-gathering systems.

Automatic test equipment makers were busy tying together their individual units into data-gathering networks and were also bringing forth faster systems. Microprocessor development systems were being molded into network arrangements to serve multiple users and functions. And finally, there was notable activity in the field-service area, as easier-to-use units were brought out for unsophisticated field users and as prices dropped on hand-held multimeters.

This year's most outstanding achievements in instrumentation center on automating the measurement process. Among several important instruments introduced is the 6070A radio-frequency generator from the John Fluke Manufacturing Co., Mountlake Terrace, Wash.

To provide a low-cost, programmable instrument with the spectral purity needed for off-channel receiver measurements, Fluke engineers applied technology both new—in the form of a surface-acoustic-wave device and a 16-bit microprocessor—and well established—such as cable delay lines—in innovative ways. The resultant signal generator, with its low-noise, fast-settling, major-octave generator, slashes the cost of automated receiver testing by approximately $10,000 per station.

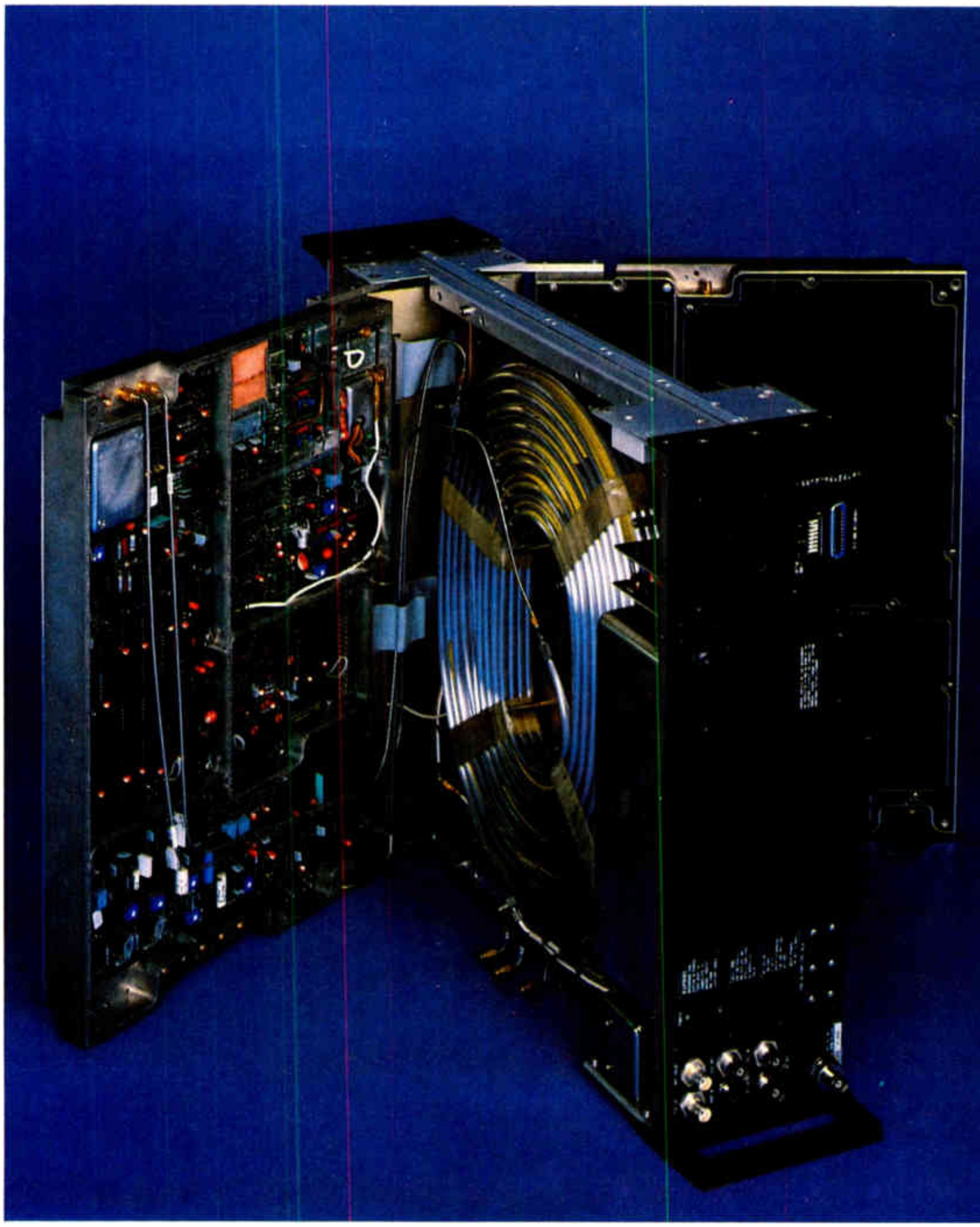
Oscilloscope operation also succumbed to automation this year—and twice at that. Driven by different views of how best to automate scope measurements, Tektronix Inc. of Beaverton, Ore., and Hewlett-Packard Co.'s Colorado Springs (Colo.) division both introduced intelligent oscilloscopes.

The 7854 introduced this past spring by Tektronix is the most sophisticated design tool to fit on an engineering bench in terms of its data-handling capability. While retaining the look and feel of a scope, it can measure some basic waveforms at the stroke of a single key. But its programmability makes the plug-in, 400-MHz unit of even greater value to the designer, who can store and manipulate waveforms using a detachable keyboard.

Hewlett-Packard's 1980A oscilloscope, on the other hand, is aimed at the non-engineer. It simplifies operation to the point where even a person unfamiliar with oscilloscopes can make measurements with little training. For example, the one-knob unit can automatically select typical measurement settings based on the input signal, making it the first autoranging oscilloscope.

System elements

An additional element that unites all three units is the fact that they can be programmed through an IEEE-488 interface. The many bus-compatible instruments now available offer the engineer a third way of automating measurement, over and above general-purpose automated test systems and dedicated, specialized testers. It is economically feasible and often desirable to put together



Interdisciplinary. Designers of the 6070A programmable rf signal generator pulled out all technological stops, both analog and digital to make automated receiver testing cost-effective. In addition to a special phase-locked loop and advanced microprocessor control, they built a custom surface-acoustic-wave device and a cable delay line (seen at center) to ensure signal purity.

a system using bus-compatible instruments as modules.

High attendance at the bus-related sessions at various technical meetings this year attests to the interest in this new option. Moreover, instrument manufacturers are increasingly addressing this new market with products uniquely tailored to it.

Systron-Donner Corp.'s Instrument division in Concord, Calif., for example, introduced its first and lowest-priced bus controller, the $795 model 3520, and Fluke also introduced its first bus controller, the 1720A. Employing both a touch-sensitive cathode-ray-tube display and a detachable keyboard, the latter controller fits both the production and lab environments.

Racal-Dana Instruments Inc. of Irvine, Calif., which last year introduced the first bus-compatible switch matrix, made it possible this year to synchronize high-speed measurements in bus systems with the series 1500 delay-pulse generator.

Wiltron Co. of Mountain View, Calif., introduced the first General-Purpose Interface Bus network analyzer, the model 560, covering a range from 10 megahertz to 34 gigahertz and in England, the Brookdale operation of EG&G Inc. introduced a GP-IB–compatible measurement system for the precise characterization of optical fibers in the 600-to-1,600-nanometer range.

Possibly the most frequently used instrument in bus systems is the digital multimeter, and this year has seen a host of system DMM introductions. Hewlett-Packard's Loveland (Colo.) division introduced the fastest-reading DMM to date, the model 3456A, able to take 270 readings with 10-microvolt sensitivity. Guildline Instruments Inc., Elmsford, N. Y., offered the 6½-digit 9576A, a unit that performs a wide variety of data manipulations that can unburden the controller. Though slower than the HP unit, the IEEE-488–compatible instrument can be used as a system by itself, according to the manufacturer, putting out data through the bus to a printer or terminal.

New wave. Through the umbilically attached keypad seen at bottom right, designers can make the processor in the Tektronix 7854 scope above it transform acquired waveforms mathematically and display them or transmit them to another unit via an IEEE-488 interface.

Fluke's 5½-digit model 3870 is IEEE-488–compatible when that option is chosen. But the unit can also serve as a bench system, with a separate, calculatorlike controller programming its memory modules to make many different measurements. And Keithley Instruments Inc. of Cleveland, Ohio, left its mark on the IEEE-488 bus not only with the lowest-priced system DMM, the 6½-digit 192 that sells for under $1,400 with bus interface and provides generic DMM functions, but also with the combination DMM and electrometer, the 619.

There was no lack of signal sources for IEEE-488–based systems either. While Fluke aimed at HP's 8662 with its 6070A and 71A synthesized signal generator, Interface Technology of San Dimas, Calif., trained its sights on HP's 8016A word generator, introducing the RS-680, which the company calls a word generator/timing simulator. The unit is able to deliver bytes at 100 MHz—twice the frequency of the HP unit—and 16-bit words at 50 MHz. Wavetek of San Diego, Calif., also aimed at HP's signal source market, in particular that for the 8165A programmable signal source, with its model 178. Trading off some of the features of the 8165A, Wavetek is able to market the unit for $3,995, half the cost of the HP unit. HP is not likely to take the competition from these companies lightly and will undoubtedly respond in the coming year.

Some bumps

Although the vast number of instruments with which to build has made this route to measurement systems extremely attractive, there are some potholes that both instrument and system builders are becoming aware of.

The smaller instrument makers who rely on chip sets from semiconductor houses to implement bus protocols were annoyed to discover bugs in the chips that the semiconductor manufacturers and larger instrument companies who helped develop them already knew about. Semiconductor manufacturers Intel and Texas Instruments have upgraded their chips, claiming that the new versions will be free of earlier problems. Still, users will be wary for some time to come, checking to see if bug lists develop.

Potential system builders, on the other hand, became aware of aspects of system configuration not addressed in the original bus standard—namely, the conventions for coding and formatting device-dependent data. While an IEEE committee tries to formalize those conventions without limiting the designers' freedom, some companies are adopting their own coding and formatting rules with an eye to the proposed recommendations.

In the meantime, instrument manufacturers are working to produce complete measurement systems that can be easily tailored to many sets of measurement tasks. Hewlett-Packard, for example, by combining its high-speed DMM with a new data-acquisition unit, the 3497A, and an HP desktop computer, can now offer a sophisticated control system, the 3054A, that is equally at home in the research laboratory and the industrial plant.

Fluke, too, is taking advantage of the bus to offer such systems. The company's model 2400A measurement and control link is offered with the 1720A controller to form a complete high-frequency data-acquisition system, and the bus controller is also employed in its new 7405 calibration system. Other instrument companies will take advantage of this philosophy in the coming year, providing measurement systems that feature their individual areas of instrumentation expertise. As the ease of configuring such systems increases, along with their capabilities, they may provide strong competition for the automated test equipment manufacturers.

ATE to the fore

But while instruments are being tied together to make test systems, automatic-test-equipment manufacturers are tying systems together into powerful data-gathering networks to revolutionize production control and efficiency. Fairchild Camera and Instrument Corp.'s Test Systems Group in San Jose, Calif., began the move with the introduction of its Integrator II, followed by Teradyne Inc.'s Semiconductor Test Systems group in Woodland Hills, Calif., with its test system administrator. This year, GenRad Inc. of Concord, Mass., introduced its first network, the daisy-chain GRnet, claiming the fastest data-transfer rate yet—a raw figure of 655,000 bits/second. With this rate, down-loading of test routines takes less time than changing tapes or disks.

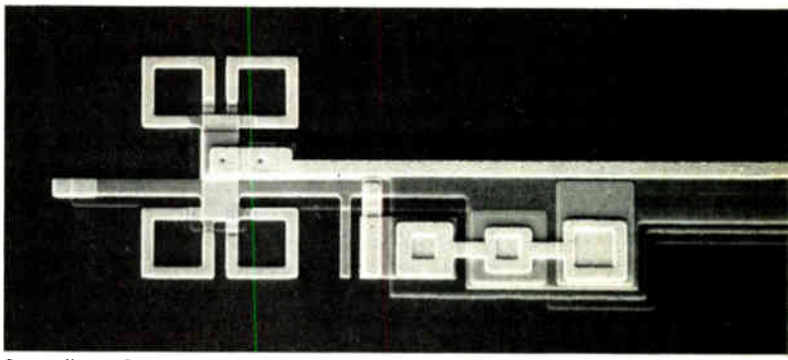
In aiming to become the No. 1 ATE company, GenRad is preparing to enter the semiconductor test system market for the first time. The company's Semiconductor Test Instrument group in Santa Clara, Calif., which has already secured a contract with IBM to provide a 100-MHz very large-scale integration test system, plans to begin deliveries of that system late next year. According to industry sources, it will be modular and a slower-speed version will debut early in 1980.

As a newcomer to this market, GenRad may have a strong advantage in not having to worry about upward system compatibility in its architecture. But Teradyne, Fairchild, and Macrodata do not plan to relinquish any portion of their market share without a strong fight.

Teradyne, for one, has clearly demonstrated its ability to provide measurements accurate enough to be meaningful for foreseeable RAMs. In its J389 RAM tester, the company is able to control placement of test signal edges with an accuracy to within 250 picoseconds. With its architecture, Teradyne can go well beyond the present 20-MHz operating speed of the system.

Teradyne is also taking a strong shot at the board-testing market where GenRad has enjoyed much success. Teradyne, in introducing the L200, may well have laid to rest the problem of whether to use functional or in-circuit testers. The new modular system can be configured to perform both types of board tests.

Another market in which GenRad was challenged this year was that for benchtop linear test systems, which it pioneered in 1979. The challenger, Analog Devices Inc. of Norwood, Mass., was new to the test system market, but the company made strong use of its converter knowledge to provide test capability for those devices, in addition to basing its design on a more powerful 16-bit microprocessor than GenRad's. That company countered Analog Devices' introduction of a-d and d-a cards at Wescon, but other companies will soon enter the market.



Superfine. Superconducting circuits like the NBS's Josephson device seen above will provide calibration laboratories with the ability to make fine-resolution measurements and thus keep ahead of the demands imposed by high-speed commercial applications.

While ATE companies move to provide networks for factories, both instrument and semiconductor companies are eyeing the design environment, planning to assist the design process by allowing development system resources to be shared. While reducing capital expenses in this manner, they are also bringing out low-cost development systems to make entry into the microprocessor design process less of an economic burden.

Better field tools

Although networks will eventually extend into the field to solve service problems, the need for immediate solutions has given rise to better portable tools in the past year. The fact that many field service people are beginning to accept signature analysis as the answer to their problems should ensure the success of the HP 5001A microprocessor exerciser. The first of a new line planned by the company, it provides not only a known stimulus for troubleshooting products in the field, but also an easy way for manufacturers to retrofit signature analysis into existing products.

The fact that several instrument makers use signature analysis techniques in the design of their own products will give rise to new signature analysis instruments from them in the next year. Already Tektronix has incorporated signature analysis capability in its model 308 data analyzer, tying it in with state and timing logic analysis and serial analysis to produce a very versatile tool.

Taking early note of both the present field service environment and the growing number of networks, Tektronix has aggressively addressed these issues in the past year by adding to its data-communication tester line the model 834, a go/no-go tester.

The analog side of the increasingly digital test world has not been ignored in the field service markets, either, this past year. Hand-held digital meters have multiplied rapidly as they replace the common analog meter once found in every technician's toolcase.

The price of 3½-digit hand-held multimeters dropped in November when Keithley introduced its first such unit, the $99 model 130. The ranging scheme—two rotary switches offset so that they can be turned with the thumb of the left hand—coupled with a large liquid-crystal display and extremely rugged packaging has made the unit popular in both the U. S. and Europe. Hickok Electrical Instruments in Cleveland, Ohio, dropped the price even more, to $89.95, with the introduction of the LX 304, which uses a slide knob ranging selector that can be moved with the probe.

The hand-held meter also got noisier as Weston Instruments Division of Sangamo Weston Inc. in Newark, N. J., introduced the Roadrunner, a beeping unit that allows the user to test continuity and to look for measurements that exceed a certain value, and Data Precision Corp. of Danvers, Mass., introduced the 936 with continuity beep.

But what may prove to be the best range-selection scheme in such meters, autoranging, was first seen this year in the model 2845 introduced by B&K Precision of Chicago. If the feature proves easy to produce, other manufacturers may adopt it. In the following months, instrument manufacturers will introduce 4½-digit units.

Even as commercial manufacturers produced a relentless flow of measurement tools to meet current demands in design, production, and the field, metrologists upped the capabilities of their research labs to handle the demands of technologies about to break.

Staying ahead

In laboratories around the world this past year several significant gains were made. A team of researchers from the U. S. National Bureau of Standards and Canada's National Research Council reached new highs in frequency measurement, directly measuring one of 520 terahertz (10^{12} hertz) in the latter part of 1979. Late last winter, in Frankfurt, Germany, workers at the Battelle Institute constructed a thin-film bolometer whose sensitivity approaches the theoretical lmit for thermal radiant energy: 1.43×10^9 cm-$Hz^{-1/2}$ watt.

This past summer researchers at both the National Bureau of Standards and IBM's Thomas J. Watson Research Center in Yorktown Heights used sampling techniques to measure signals on supercooled Josephson devices with a resolution of 9 and 2 picoseconds. Both groups are racing to apply the measurement scheme to signals piped to the Josephson chip.

Loughry, Ricci, Nelson, and Knoblock: GP-IB founders

Thanks to the IEEE-488 standard, traditional instrumentation products are now commonly applied to automatic test systems. And that standard, defining mechanical, electrical, and functional requirements for linking instruments and computers, in turn owes most of its success to four Hewlett-Packard engineers who conceptualized it, designed its important specifications, and nurtured it along its way to acceptance through a gamut of international committees and rivals in the instrumentation world. Donald Loughry (pictured below), David W. Ricci, Gerald Nelson, and Daryl Knoblock all are quick to insist that the 488 project was not theirs alone—nor even HP's—but a truly international effort. Other industry participants, however, point to these four as its founding fathers.

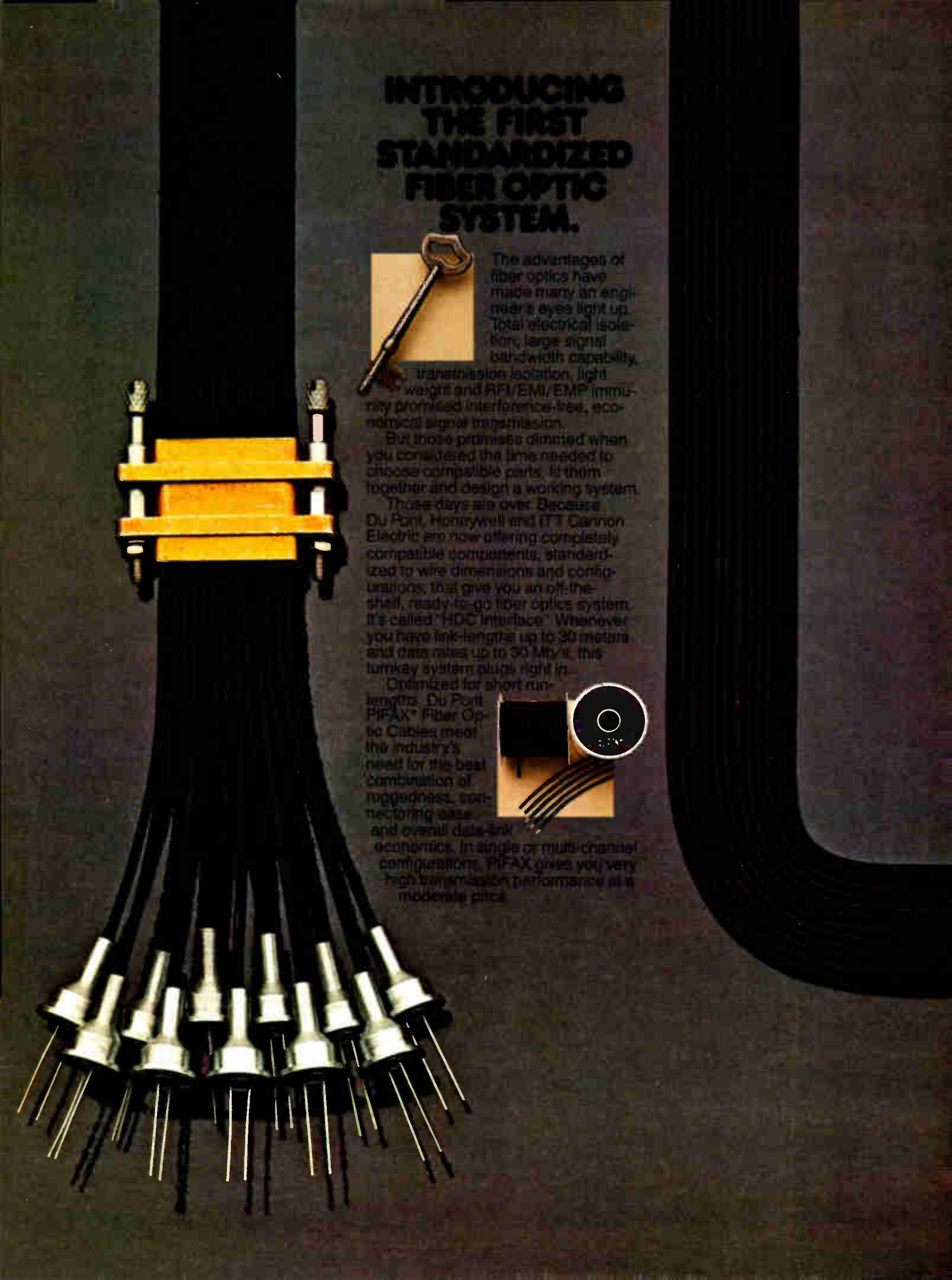
It began in 1971, when automatic test equipment engineers were still spending half their time designing interfaces instead of instruments. "We had wanted a standard set of voltage levels for instrumentation-oriented computers since the late 1960s, but 1971 was when this effort really got started," recalls Loughry, who became HP's corporate interface engineer. Two HP groups, one in the Santa Clara division under Ricci and one in the Loveland, Colo., division under Nelson, had begun similar work on specifying an interface. Loughry brought the two project leaders together on Dec. 7. By the end of the meeting, the major specifications of what later became the IEEE-488 had taken form.

"In that meeting our thoughts solidified on specs for 15 of the signal lines," recalls Ricci, now the interface engineer for HP's instrumentation group. "We agreed on the eight data lines, the four management lines, and the three handshake lines, and also to use one bus for both address and commands—an idea that came from Loveland." Later, the end-of-interval (EOI) line was added to facilitate binary records and parallel polling. The service request line (SRQ) was added even later, as the standard journeyed into international waters.

Loughry, Ricci, and Nelson were joined in the spring of 1972 by Knoblock, who wanted to use the interface for computers as well as instruments. "I suggested a number of small changes that would make it useful as a computer I/O bus, and somewhat to my surprise the other three accepted them," recalls Knoblock. Though he recognized that the interface was not the speediest possible computer bus, he saw that its adoption in HP's line would make it easy for computers to swap peripherals.

The cost of the logic to implement the interface was also a stumbling block, but the arrival of large-scale integration solved the problem. "With the coming of the HP LSI chip for the IEEE-488 in 1977, we had the best of both worlds—a low number of connections and the economies of LSI," Knoblock notes.

Standardization did not proceed without difficulty. The international community differed over whether a most significant or a least significant bit should be transmitted first, whether the standard should be product-independent, and whether polling should be serial or parallel. The most serious disagreement, however, was over choosing a 25- or a 24-pin connector. The IEC committee finally adopted both the 25-pin connector favored by the Europeans and the 24-pin version preferred by the Americans. The specs for hardware, pinouts, and voltage level were decided on in 1975 and further clarified in 1978. **-Martin Marshall**



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COMPUTERS & PERIPHERALS

Local networks sprout to handle all types of gear as peripheral devices benefit from large-scale integration and distributed processing and office automation mushroom

by Tom Manuel, *Computers & Peripherals Editor*

More than anything else, the past 12 months marks moves to new levels of utility and convenience for computers. Perhaps most noteworthy has been the attention given to ways to connect processors and peripheral devices, especially at single sites. Local networks have emerged in response to rapidly growing markets for distributed processing and office automation and in turn will open up these markets even further.

Meanwhile, peripheral devices have undergone significant changes, in large part due to the thrust of large-scale integration. For disk drives, a shrinkage from 14- to 8- and even 5.25-in. Winchester units and the application of thin-film semiconductor techniques to read/write heads have also played roles. As a result, such peripherals as disk files and color terminals that were once mere accessories are becoming intrinsic system components.

As for the machines themselves, several firms have presented interesting solutions to the challenges of LSI: getting the most of the new capabilities without sacrificing architectural flexibility or existing software.

Keeping in touch

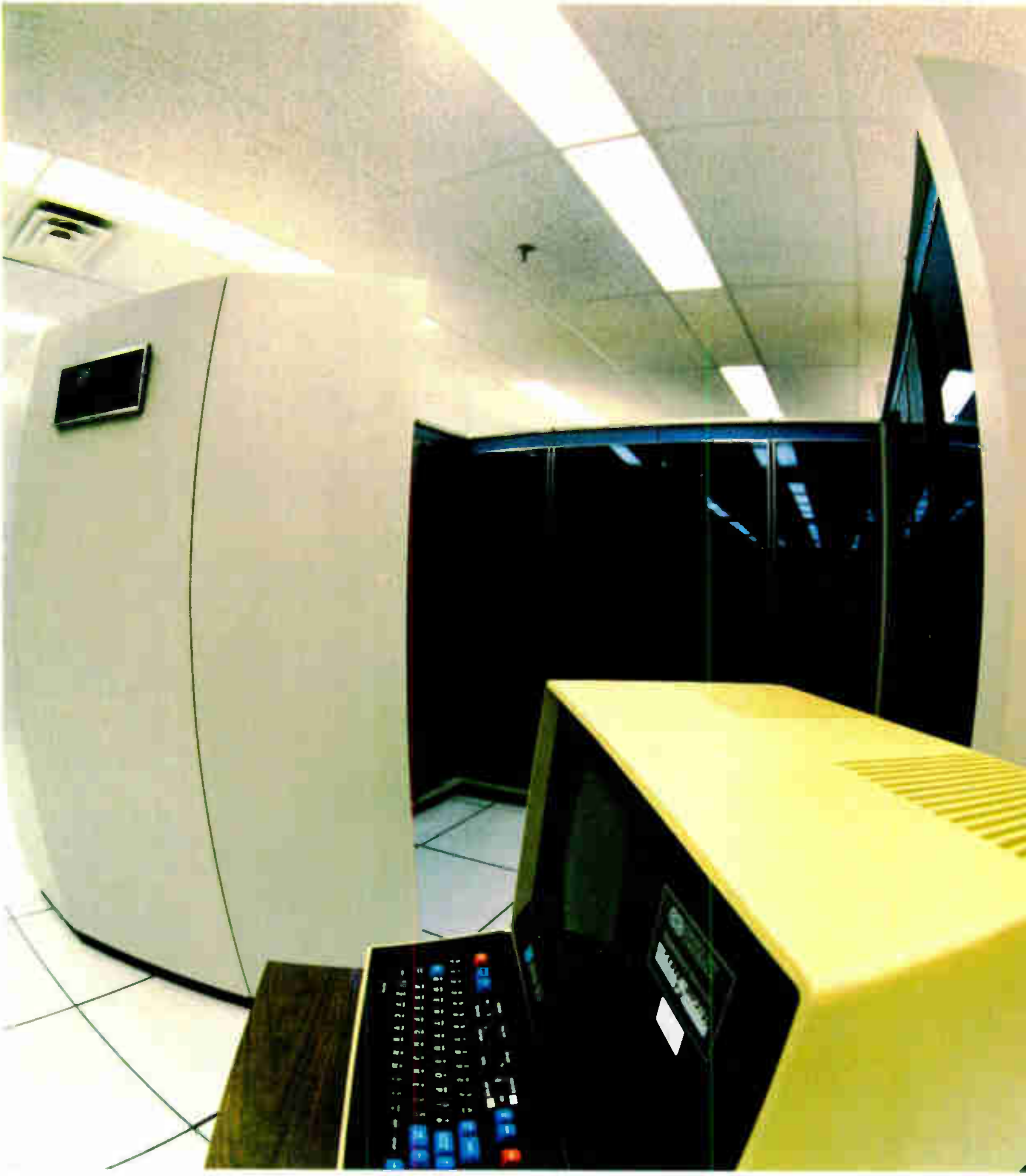
Data communications, long considered an important adjunct to computers, has become an inherent requirement of the fastest-growing applications—distributed processing and office automation. Indeed, it is becoming virtually impossible for designers to work on computers these days without a knowledge of communications.

Just coming to the forefront is local networking that can accommodate many types of gear from different makers. As its name implies, this technique is used to connect equipment together over limited distances—typically within an office building or industrial complex.

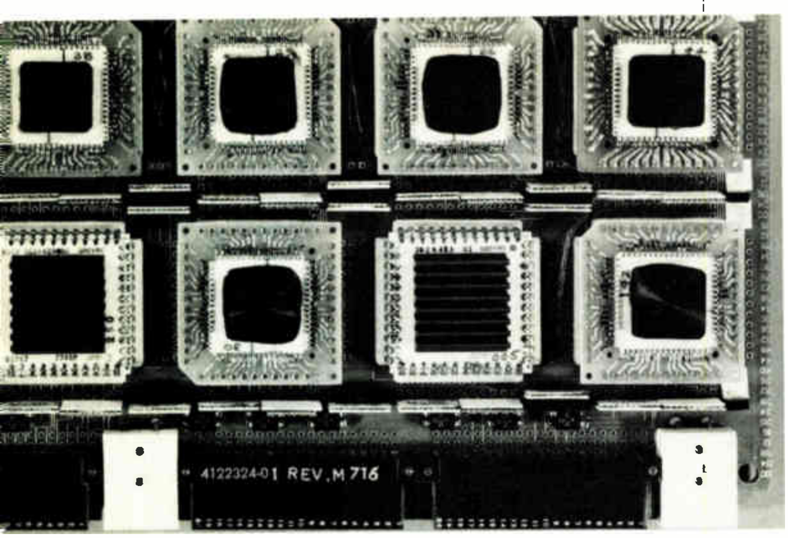
Taking a big step toward making such networks a reality, Xerox Corp., Stamford, Conn.; Digital Equipment Corp., Maynard, Mass.; and Intel Corp., Santa Clara, Calif., last May announced that they would pool their efforts to perfect Ethernet. First introduced by Xerox in December 1979, Ethernet operates at 10 million bits per second much like a party line. Each piece of equipment is attached to a coaxial cable and is given a 48-bit address. A transmitting device waits for a quiet period on the network and then broadcasts its message to all attached equipment. Only the addressed device or devices pick the information off the net. The beauty of such a system is that no central controller is needed to handle message routing, and hence there is no one piece of equipment whose failure will shut down the network.

Several other local networking schemes also came to the front last year. Newcomer Ungermann-Bass Inc., Santa Clara, last May introduced its 4-Mb/s Net/One, which also promises to interconnect locally a wide variety of computer gear. In addition, Zilog Inc., Cupertino, Calif., announced its Z-net packet-switched local network. "We're on the verge of throwing open a whole new market for communications, and it will be big enough for everybody," declares Manny Fernandez, group vice president at Zilog. "Ethernet-like communications network systems will be the local communications of the future."

From Britain came word that researchers at the Computer Laboratory of Cambridge University had devel-



Supercomputer. Cyber 205 computer from Control Data is the fastest commercially available. The CPU has two specialized units, one for vector stream (parallel) processing and the other for scalar (serial) processing. The vector processor can operate on 64-bit or 32-bit operands at the exceptionally high rates of 200 and 800 megaflops, respectively.



One-board mainframe. Using custom 8-bit-slice ECL circuits on hybrid logic modules (shown with heat sinks attached), the CPU of Sperry Univac's system 80 computer fits on a 17-by-29-in. board. The older system 90/60's CPU used 400 5-by-7-in. boards.

oped a local network based on twisted-pair cable that promises to be less expensive to operate than Ethernet. By being a closed ring, the unit also promises to be conceptually simpler than Ethernet, although it is less reliable—the failure of any element on the network breaks the ring. In any case, Logica Ltd., in London, hopes this year to start marketing the network, called the Cambridge Ring, at prices of about $2,000 per station.

In a broader sense, International Business Machines Corp. also put communications in the spotlight last year. In an unusual announcement last June that bordered on pre-announcement, the Armonk, N. Y.-based company said it would use communications to integrate its various office automation products into what it calls "single, coherent enterprise-wide solutions."

Actually, communications seems to get the industry leader out of a serious bind. Three IBM divisions—Data Products, General Systems, and Office Products—had developed three completely different product lines. Making them compatible would require the tremendous task of changing to identical instruction sets, data formats, and file structures. Instead IBM chose to use communications for the interfacing. A new "document interchange architecture" will handle the translation and emulation of communications protocols and provide a standard format for the transmission of data between systems.

Traditional communications

Meanwhile, traditional data communications was also gaining sophistication. Data General Corp., in Westboro, Mass., announced its Xodiac communications architecture. Unlike most of the proprietary data-communications structures now offered by the leading mainframe and minicomputer makers, Xodiac is based on the increasingly popular CCITT X.25 packet-switching standard.

Digital Equipment Corp., Maynard, Mass., one of the first to announce a proprietary scheme, continued to refine its offering with the introduction of DECnet Phase III. Most significant is its capability to perform adaptive path routing and to change the network configuration as line conditions change. The feature, not readily available commercially, is crucial to improving the reliability of networks.

Speak to me

Interest in how people interface with computers has heightened considerably this past year, especially in the area of voice recognition. Very few of the existing products until now have come close to recognizing speaker-independent speech that is continuous.

Threshold Technology Inc., a pioneer in the field, has perhaps done the most with continuous speech. The Delran, N. J., company has been delivering systems since 1972, and this past year it upgraded its software algorithm for voice recognition to work at almost connected-speech speeds. Labeled Quiktalk, the algorithm uses dynamic programming to match strings of sounds at a rate of 180 to 200 words or phrases per minute; it is available on the company's $16,525 model 600 voice data-entry terminal.

Verbex, formerly Dialog Systems Inc., an Exxon Enterprises affiliate in Bedford, Mass., has had a speaker-independent system on the market—the model 1800—but words are limited and must be enunciated carefully.

Other computer input/output devices were improved as well in the past year. Most noticeable, both literally and figuratively, were color cathode-ray-tube terminals. A spin-off of color television technology, color monitors and terminals have been around for several years, primarily from Conrac, Ramtek, Chromatics, and Intelligent Systems. But the additional electronics needed to handle the color display has made them too expensive for most applications and has limited their popularity. Now, however, new self-convergent CRTs and large-scale integration have combined to bring the cost of color terminals down while increasing their features.

Colorful choices

The color terminals really took off when the major computer manufacturers added color to their product lines. First was IBM, which unveiled its model 3279 color CRT terminal, ranging from $4,300 to $6,700, in December. Then in May, DEC introduced its more complex VS11 color graphics terminal, priced at $15,000. A 2901 bit-slice-based central processing unit executes software that off-loads from the host computer much of the graphics and color display details. It generates 16 basic colors that can be mixed to produce up to 256 tints.

Original-equipment manufacturers that want to add color to their systems also now have a wider selection of equipment. Chromatics Inc., Atlanta, introduced its CG3999 in May that sells for $7,997 in single units but drops to $5,995 in quantities of 100. Like most recent color terminals, it is microprocessor-based—a Z80 with 128-K bytes of random-access memory controls every dot in the 512-by-512-element display. The intention of the new displays is clear. "We intend to make black and white terminals wholly obsolete in this decade," says Chromatics' president, Terence Hughey.

For those willing to design the terminal electronics, the selection of color monitors also blossomed last year. For example, Japan's Hitachi Ltd. unveiled the HM-2619/13 and -2719/13 monitors, which feature shadow-mask CRTs with self-convergent single in-line guns. In quantities of 100, these monitors can be had for as little as $1,480 in a stripped-down 13-in. version or $2,470 for a 19-in. version ready to plug in.

Disk fever

Though not so colorful, disk drives had more than their share of excitement in the past year. Across the board, new technologies were brought to bear to lower the cost of data storage. This development was especially true at the low end, where Winchester technology was scaled down for small systems, from 14-in. disks to 8- and 5.25-in. sizes. These drives provide storage capacities ranging from 6 to 120 megabytes in packages no bigger than a floppy- or minifloppy-disk drive.

During the year, such manufacturers as Shugart Associates, Pertec Computer, Memorex, and Kennedy that had introduced 8-in. drives during 1979 began shipping their products. But as the evaluation units rolled out the door, the question of backup was persistently asked. Now that the disks are fixed inside the drive, it is impossible to remove them for safekeeping.

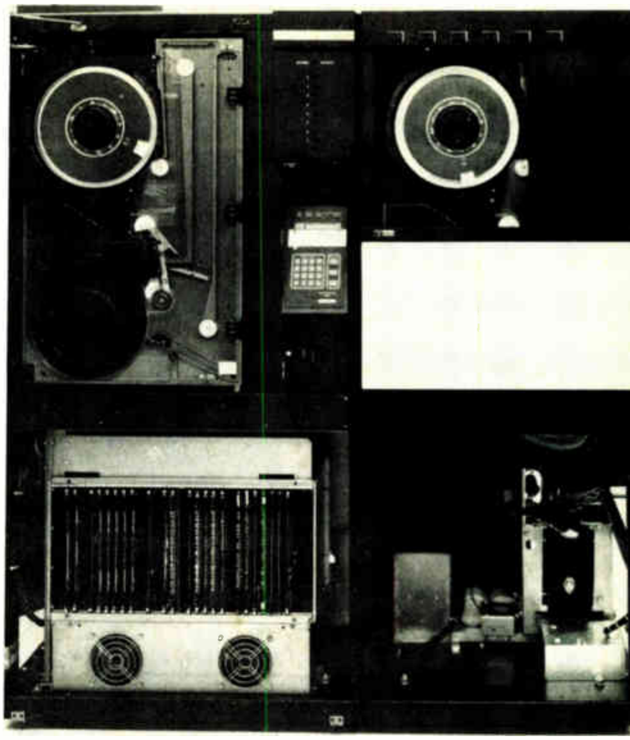
Control Data Corp., Minneapolis, proposed a system that combines Winchester technology with the best of the old disk cartridge drives. Its Lark, unveiled in June, filters the air in the removable cartridge before operation starts; then the Winchester-type heads are moved into position.

Another approach that gained popularity adds high-density tape cartridges to the system. The leading proponent and supplier of these devices, Data Electronics Inc., San Diego, Calif., introduced lower-priced OEM versions of its units that drop the drive cost to about $600.

Al Shugart, who had originally founded Shugart Associates and then sold it, returned to the disk business to start Shugart Technology Inc., which spearheaded the development of the 5.25-in. units and was the first into production at this size. Close behind were Tandon Magnetics Inc., Chatsworth, Calif., and Britton-Lee Inc., Los Gatos, Calif., whose founder Dave Britton was the pioneer of the 8-in. drives. Then Irwin International, of Ann Arbor, Mich.—founded by Sam Irwin, who was also the founder of Sycor—introduced a 12.3 megabyte 5.25-in. Winchester disk drive with a integrated tape cartridge drive for backup, to be available in May 1981.

Narrowing the gap

While existing technologies were scaled down at the low end of the disk drive spectrum, new technological ground was being broken at the high end. Borrowing a page from semiconductor fabrication, the disk drive makers were developing thin-film read/write recording heads. With photolithographic and etching processes similar to those used for integrated circuits, thin-film heads can be made having recording gaps about a quarter of the best width attainable with manually produced ferrite-core heads. Narrowing the gap increases the amount of data that can be stored on a disk.



Shrinking. Controller for Storage Technology Corp.'s model 4500 tape drive, which can handle up to eight of the drives, is small enough, thanks to custom LSI and microprocessors, to fit in a cabinet with one of the drives instead of in a separate large cabinet.

Once again, it was IBM's moves this past year that provided the impetus behind the industry's actions. When the company began delivering the 571-megabyte 3370 drive, which it had introduced in January 1979, it released specifications. The use of thin-film heads increased area recording density to 7.8 million bits per square inch—some 2.5 times that of the previous top-of-line 317-megabyte model 3350. To facilitate access to all this data, the drives also use dual actuators.

The first after IBM to go commercial was Dastek Corp. in Los Gatos, founded by former IBM disk designer Jim Koeber. The company unveiled its model 4835 drive using a thin-film head in April. Available in 200-, 300-, and 400-megabyte versions, it records at 12,772 b/in.—roughly twice the density of the model 3350, until now IBM's best ferrite-head drive. This coming year is sure to see a host of introductions using the new heads.

But no sooner did IBM begin shipping the 3370 than it surpassed itself. In June, it unveiled the model 3380, which stores a staggering 1.26 billion bytes on each of two spindles—four times more than the 3350. And with purchase prices starting at $97,650, storage costs half of what it did on the older unit.

LSI in control

In addition to improved basic recording technologies, the storage peripherals are also benefiting from the use of large-scale integrated circuits. All forms of LSI parts—microprocessors, off-the-shelf specialized peripheral controllers, and custom chips—are being employed to reduce the size and cost of the peripheral's electronics

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while increasing its features and performance.

The benefits are especially important in small computer systems. For such small systems, a plethora of new peripheral controllers became available in the past year. For example, Advanced Electronics Design Inc., Sunnyvale, Calif., unveiled its Flex family of controllers that can be programmed to work with just about any double-density floppy-disk drive. Based on a Z80 microprocessor, the controller interrogates the drive to determine its head-positioning characteristics and, once it has adapted to those, determines and adapts to the recording format used on the floppy disk.

Similarly, for the new, smaller Winchester hard-disk drives, a spate of controllers became available. Often based on microprocessors, these units generally packed all the controller functions and error-correction circuitry onto a single circuit board. Typical was the SA1400 controller from Shugart Associates, Sunnyvale. Built on a single 8.25-by-13.7-in. printed-circuit card using 2900 series bit-slice processors, it can control a mixture of the firm's 8- and 14-in. Winchester disk drives, as well as its 8-in. floppy disk, or a backup cartridge tape drive.

Other units came from manufacturers like Xylogics and Microcomputer Systems Corp. For one, Microcomputer Systems, also in Sunnyvale, crammed 75% of the control circuitry for an 8-in. disk drive controller into a hybrid 3-in.-square module called the Micromodule 9000. Using an unspecified MOS microprocessor and Schottky logic gate arrays, it handles buffering, error detection and correction, and other controller functions that are independent of the drive. Designed for internal use, it is also for sale to others.

Custom control

Some peripheral makers opted for custom circuitry. Control Data was one of the first, designing and fabricating four custom integrated-injection-logic chips for its CDC Series/1 controller. Teamed with a Z80, these four chips make it possible to construct a single controller that can attach an IBM Series/1 minicomputer to products ranging from slow devices like floppy-disk drives and CRT terminals to fast ones like hard-disk drives. Despite its versatility, the controller fits on a single 7-by-9-in. board. IBM also used custom chips in its 3370 drive and most notably in the 3880 controller that it uses with all its new disk drives. The heart of the 3880 is a custom microprocessor built from a bipolar gate array containing 1,496 gates on a chip 224 mils square.

Perhaps the most sophisticated example of the custom chip trend was the model 4500 tape memory subsystem from Storage Technology Corp., Louisville, Colo. Introduced in March, it employs a broad array of standard microprocessor parts, along with custom logic. For starters, the controller is built around a Z80. The sequencer chip, designed to process microinstructions for a bit-slice processor, is employed here instead to generate error-checking and -correcting codes for incoming data. Nine custom n-MOS chips, one for each tape channel, are used in the read electronics to replace 173 chips. These and other chips result in a controller that fits into the bottom of one of the tape drives.

LSI moves in

All this attention to peripherals is not to say that no progress was made in computer technology. Indeed, several new designs surfaced that illustrated new solutions to the problem of how best to use LSI circuits, maintain architectural flexibility, and at the same time not make existing software obsolete.

A premier example was the Eclipse MV/8000 from Data General. The minicomputer maker's first 32-bit computer, the MV/8000 maintains complete compatibility with existing 16-bit Eclipse machines yet expands the family with such mainframe features as 4.3-gigabyte virtual memory. Built around 2900 bit-slice processors, the hardware features a novel cache memory arrangement that uses separate buffers for data and instructions; a pipelined, microprogrammed CPU; a separate system-control processor; an I/O subsystem that can transfer data at rates as high as 16 megabytes per second; and an independent I/O processor that can support up to 128 terminals. Unlike other recent computers, which typically have two modes of operation—a native mode and one compatible with the existing machines—the MV/8000 has only one. To achieve this unique level of compatibility, the existing 16-bit Eclipse instructions were incorporated into the 32-bit instruction set.

No longer intent on keeping a low profile in minicomputers, NV Philips Gloeilampenfabrieken made one of the most significant European announcements when its Data Systems division in Apeldoorn, the Netherlands, unveiled three new units based on a custom 16-bit CPU chip that performs about twice as fast as the company's previous equipment. The two largest units, the P858 and P859, feature a memory management unit that provides virtual memory and gives users a real-time multiprogramming operating environment while still keeping system prices down. The smaller P853 will use bubble memory chips for peripheral memory.

Exemplifying the trend toward the use of custom circuitry by computer designers was Sperry Univac, Blue

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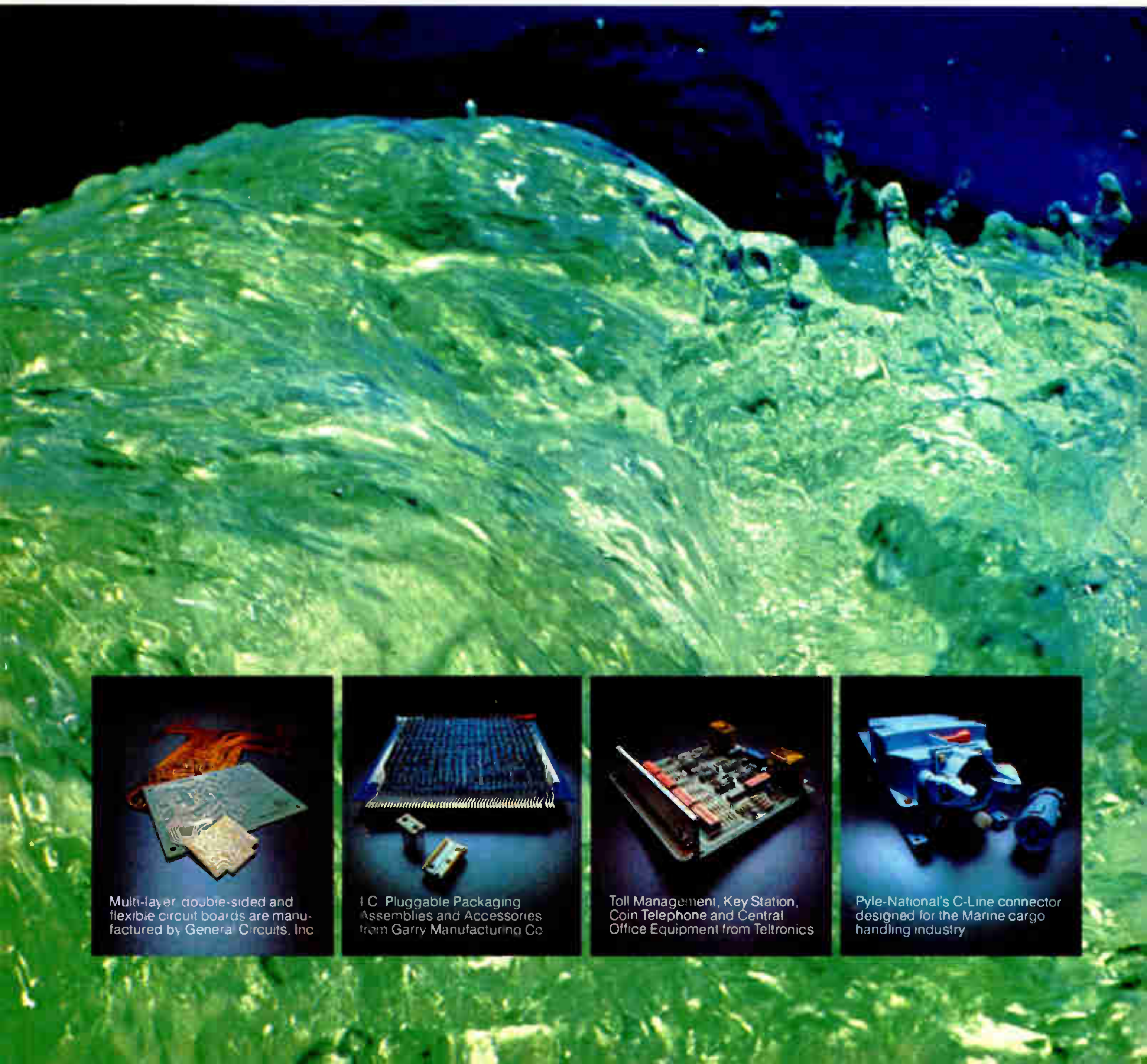

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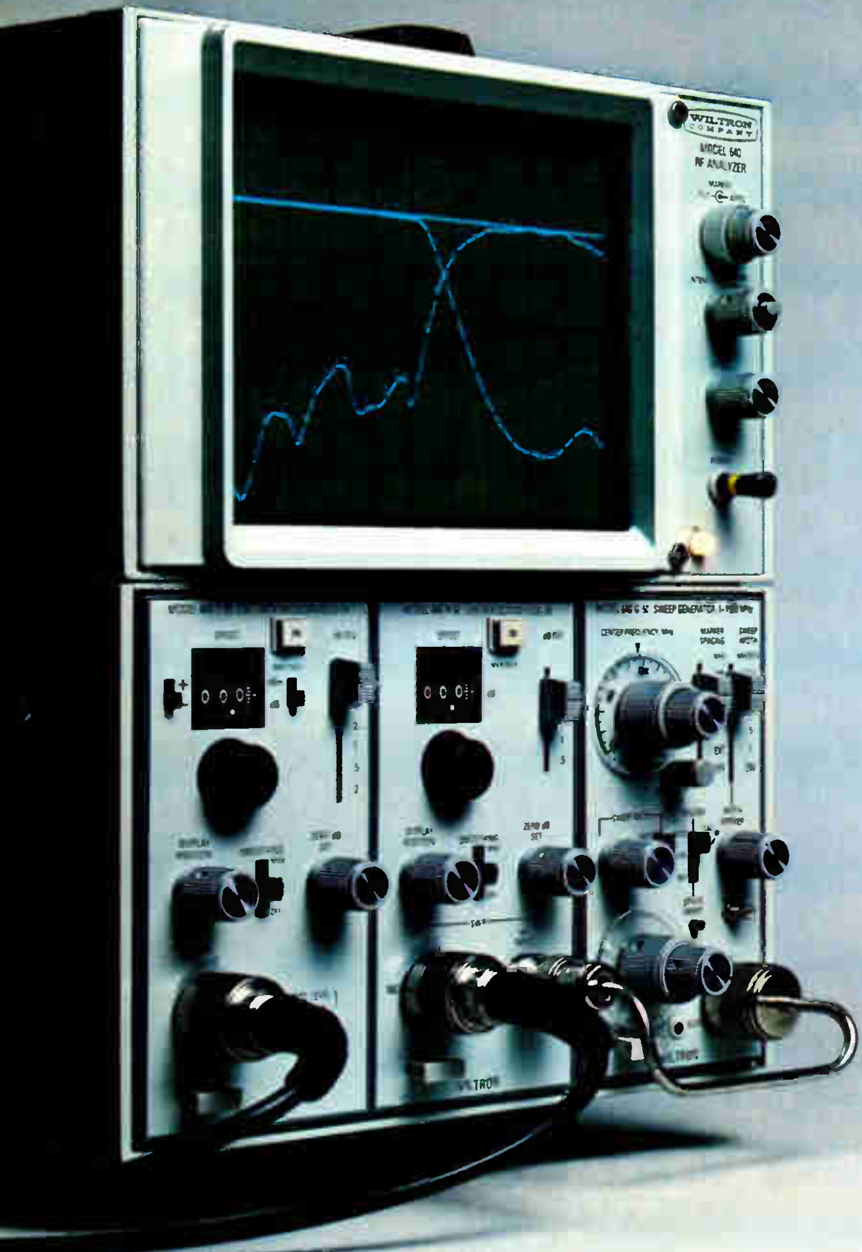

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WILTRON

Circle 194 on reader service card

Bell, Pa. Its entry-level system 80 mainframe, introduced in May, is built on a custom 8-bit-wide processor slice family developed jointly with semiconductor makers Fairchild Camera and Instrument Corp. and Motorola Inc. and fabricated with 100000 family ECL parts. The major functions of the CPU are partitioned between these chips, with one—the address and data interface unit—performing both the basic arithmetic and logic functions and the memory interface functions.

Thanks to LSI, the CPU fits onto a single 17-by-19-in. board, whereas the CPU of a comparable older system, the 90/60, used 400 5-by-7-in. boards. Rather than just milk ECL's speed, Sperry Univac chose to add error-checking and -correction features for reliability.

Relatively quiet

Compared with recent years, the past 12 months was relatively uneventful for IBM in the area of mainframe computers as it concentrated on reaching volume production with its attention-getting model 4300 processors. It added two new model groups to that series, filling the gap between the 4331 and the 4341 with the 4331 group 2 and extending the performance of the series by 80% with the 4341 group 2. At the top of the line, IBM doubled the addressable memory of the 3033 to 32 megabytes. Although the company maintained its traditional silence, industry observers became convinced that a more powerful line of processors—code-named the H series—would be announced by the first quarter of 1981.

While others were waiting for new IBM machines, the Japanese vendors continued to compete with existing IBM products, especially in the U. S. market. Hitachi, for one, brought the most powerful IBM-compatible computer to world markets through marketing agreements with Olivetti of Italy, BASF of West Germany, and National Advanced Systems of Palo Alto, Calif. Hitachi's model M-200H, using the latest in LSI, bipolar RAMs, and advanced architecture, offers 1.8 times the performance of the IBM 3033 processor.

Nippon Electric Co. expanded its Acos line to better compete with the IBM 4300 series. The Acos 350 countered IBM's low-end 4331, the Acos 450 matched the mid-range 4341, and the 550 brought the line in against the high-end IBM model 3031.

Mitsubishi Electric Corp. unveiled a new top-of-the-line mainframe, the Cosmo model 900II. Built with ECL, it had three times the performance of the company's largest previous unit. Prices were in the same range as those of IBM's 3031, but performance was closer to that of the larger 3032 machine.

Furthermore, Japanese manufacturers indicated that more product developments were soon to surface.

The uppermost end of the computing scale was unusually active in the past year. Control Data claimed it had the most powerful computer with the introduction of its Cyber 205 in June. Built from LSI ECL circuits, the unit performs 800 million floating-point operations per second (megaflops). Sperry Univac quietly entered the fray

Wallach: manager of a super-minicomputer effort

Steven J. Wallach is tired but happy these days. For more than two years, as manager of advanced Eclipse development at Data General Corp., he headed the team responsible for the firm's Eclipse MV/8000, 32-bit super minicomputer, announced last May.

In April 1978, Wallach got the task of turning management's rough product description into design guidelines. He spent four months putting together an architectural specification sprinkled with famous quotations. One from George Santayana, the philosopher—"Those who forget the past are condemned to repeat it"—was especially appropriate as the company's managers stressed the new machine's compatibility with earlier equipment.

Wallach met that goal even though his design—which he terms an asymmetrical multiprocessor—is totally different from any earlier Data General system architecture. He feels the design is so flexible that it will serve as a springboard for DG products far into the coming decade. "I believe in multiple buses and multiple specialized processors," he says. "You can get more raw performance, higher efficiency, and far more growth than with typical multiple-central-processing-unit designs."

Wallach also likes to get the processing as close as possible to the data. "If you're smart, you move the least data as seldom as possible as short a distance as possible," he says. Also, "you tailor the processor to the job. If you want floating-point operations, you don't need the features of a communications processor, and vice versa. The same is true for diagnostics, I/O management, and other tasks."

Finally, he likes the fluidity of the approach. "The MV/8000's alterable microcode lets it adopt new characteristics fast, take on instruction set augmentations easily, or take advantage of new processor modules." For example, he believes the MV/8000 is flexible enough to be used in a shared memory configuration with other, outboard processors.

Wallach received an MSEE from the University of Pennsylvania in 1969. He worked at logic and computer design at Honeywell Information Systems and at Raytheon's Missile Systems division, gaining an MBA at night from Boston University. He joined Data General in 1975 and has been with its advanced development efforts ever since.

Looking back at the development of the MV/8000, he says, "We worked 12-hour days seven days a week, and it wasn't unusual for me to get calls in the middle of the night as a team member ran up against some seemingly insoluble problem. But I think that almost everyone who stuck it out is glad to have done so. It is a huge ego boost to see a machine like the MV/8000 out there and know you had a part in making it possible." **-James B. Brinton** with an array processor attachment for its 1100/80 boosting speed to 120 megaflops.

Supercomputers

Then newcomer Denelcor Inc., in Denver, challenged the established supercomputer makers with its Heterogenous Element Processor, or HEP. This novel parallel processor—built from 1 to 16 processing modules and as many as 128 memory banks of 1 million words each—is unusual because it executes multiple streams of instructions on multiple streams of data. Most of the other supercomputer architectures, in contrast, execute only a single set of instructions that act simultaneously on multiple pieces of data.

Challenging from overseas is International Computers Ltd., in Putney, London, which delivered its first Distributed Array Processor. Consisting of an array of 64 by 64 processors, each with its own memory, the DAP can also execute multiple instructions and multiple data streams.

Heavy investments for software

Underlaying all the activity in hardware was a growing shift in emphasis to software. After a decade of talking about the problem, companies are investing heavily in new software engineering techniques, programmer training, and automated programming aids like interactive editors.

The importance of software is especially evident in that most glamorous application of computer gear, office automation. Both Datapoint Corp. and Prime Computer Inc., for example, recently expanded their office automation offerings, not with new hardware, but with new software. Recognizing the trend toward combining functions onto a single system for office use, Datapoint introduced its integrated office last December. To its existing Attached Resource computing hardware, the San Antonio, Texas, firm added new software that performs word processing, handles electronic mail, and manages voice communications, as well as performing the data-processing functions already on the system.

Most notable was an electronic file system called Associative Index Method, or AIM, that allows files of up to 12.5 megabytes to be searched for all mentions of key words, phrases, or numbers. (The first such commercial product, however, that searches by content, rather than by address, was the CAFS—for content-addressable file store—800, from England's ICL. Hardware-based, it uses key index words to access up to 14 disks of 60 megabytes each, for a total of 840 megabytes.)

In a move similar to Datapoint's, Prime, Wellesley Hills, Mass., added software in April to its 50 series minicomputers to create its content-addressable office automation system. A word-processing module lets users create, store, retrieve, and modify documents; an advanced text-management module has a dictionary for automatic proofreading, hyphenation, and multilingual translation; and a support package establishes an electronic mail system.

Martin: backer of voice recognition

"We lost money in 1980—in fact, we've lost money every year since we started in 1970." Yet the man saying this is far from worried that his company will fail in either the long or short term. In fact, Thomas B. Martin's Threshold Technology Inc. has some very big backers—Siemens AG, Xerox Corp., and Time Inc.—as well as some private investors and the public at large. On paper, the company is worth between $20 and $25 million at $12 per share, with one of the hottest products for the 1980s in its technological portfolio: voice-recognition terminals.

Martin, 45, chief operating officer and president, helped found the Delran, N. J., company, after leaving RCA Corp. There, as an electrical engineer with a Ph.D. from the University of Pennsylvania, he headed up the speech-processing group in the Advanced Technology Laboratory. Together with cofounder Marvin B. Herscher, Martin developed the logic to do feature extraction from voiced sounds and applied it in their first voice-recognition unit, the VIP 100, shipped in January 1973. Still being sold for around $17,000, it is built around a Data General Nova minicomputer and has a vocabulary of 32 words.

More recently, Threshold Technology began building its units, which must be "trained" to recognize a particular speaker, around a smaller processor—Digital Equipment Corp.'s LSI-11 microcomputer—and this year introduced a software algorithm called Quiktalk that can be used to analyze about 200 words per minute. That is virtually continuous speech. The system with Quiktalk, the Threshold 600, recognizes up to 250 words.

Martin's greatest concerns right now are product planning and marketing strategies. He wants to move from the standalone systems he has been selling to industrial end users and the handicapped into the market among original-equipment manufacturers for stripped-down terminals and even boards.

Helping in this is the acquisition last winter of Auricle Inc., a custom semiconductor design house in Santa Clara, Calif. Within a year, Martin hopes that Auricle will be turning out a speech-recognition chip for a board product that uses his original feature-extraction logic.

He is also eyeing office automation. "A manager will have powerful terminals with a lot of function keys—why not let him control them by voice?"

Then, as "there's a need for a security system when you get into communications between people and computers," he says, speaker verification will be another new market. "You may need a voice print as well as an identification number." Threshold Technology will ship its first speaker verification system sometime next year. "The deal with Siemens helped to speed up our development work a little bit," Martin admits. **-Pamela Hamilton**

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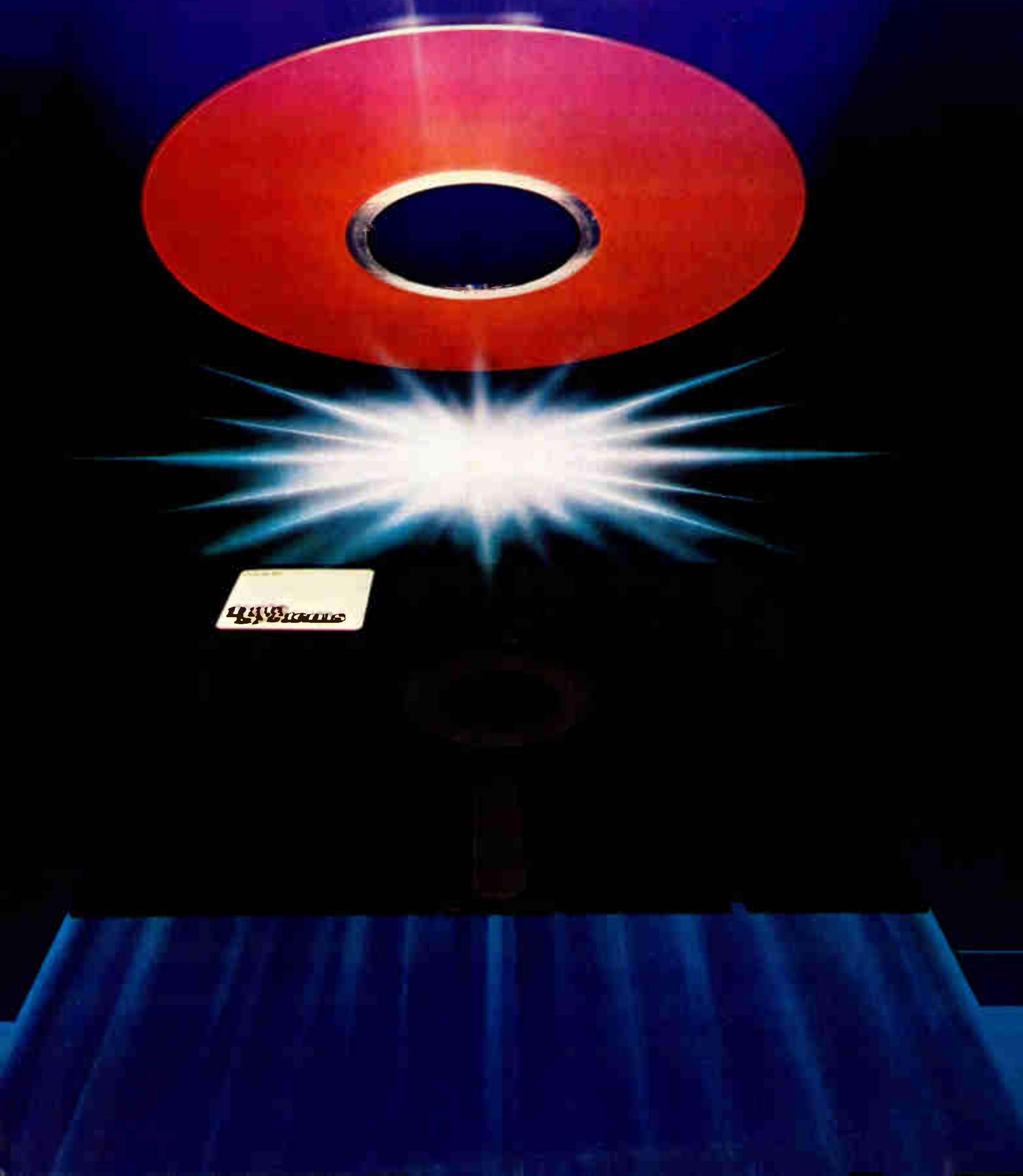

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COMMUNICATIONS

Large fiber-optic systems are at last being built or planned; coder-decoder chips are in the forefront of the invasion of telecommunications by large-scale integration; an antenna capable of dealing with several satellites at once emerges

by Harvey J. Hindin, *Communications & Microwave Editor*

Fiber optics, which gained the attention of the communications industry in 1979, held onto to it firmly in 1980, with the giant American Telephone & Telegraph Co. dominating the field. Around the world, last year's work in reducing fiber attenuation gave way to planning and building operating systems. In telecommunications, the semiconductor made further inroads, aiding the development of more cost-effective equipment, and interest in the home and office of the future continued.

Government agencies became even more involved in the industry in 1980, with activity centering around AT&T and its competitors as Bell set up an unregulated subsidiary to go into previously off-limits data-communications businesses.

Satellite technology had its dramatic moments, too. Participants at the World Administration Radio Conference agreed to disagree on orbit and frequency rulings. The first satellite able to be retrieved at the end of its useful life was launched—its retrieval depending on the fate of the long-delayed space shuttle—and a new satellite network to search for downed airplanes was designed. The year also saw important basic work in new antennas and in frequency measurements.

Put it to work

Fiber-optic technology's turn to a systems emphasis in 1980 was led by AT&T, which started development of a 611-mile system to link Boston, New York, Philadelphia, and Washington by a laser-powered lightwave system. The largest system announced so far, it will ultimately connect 19 of Bell's electronic digital switches.

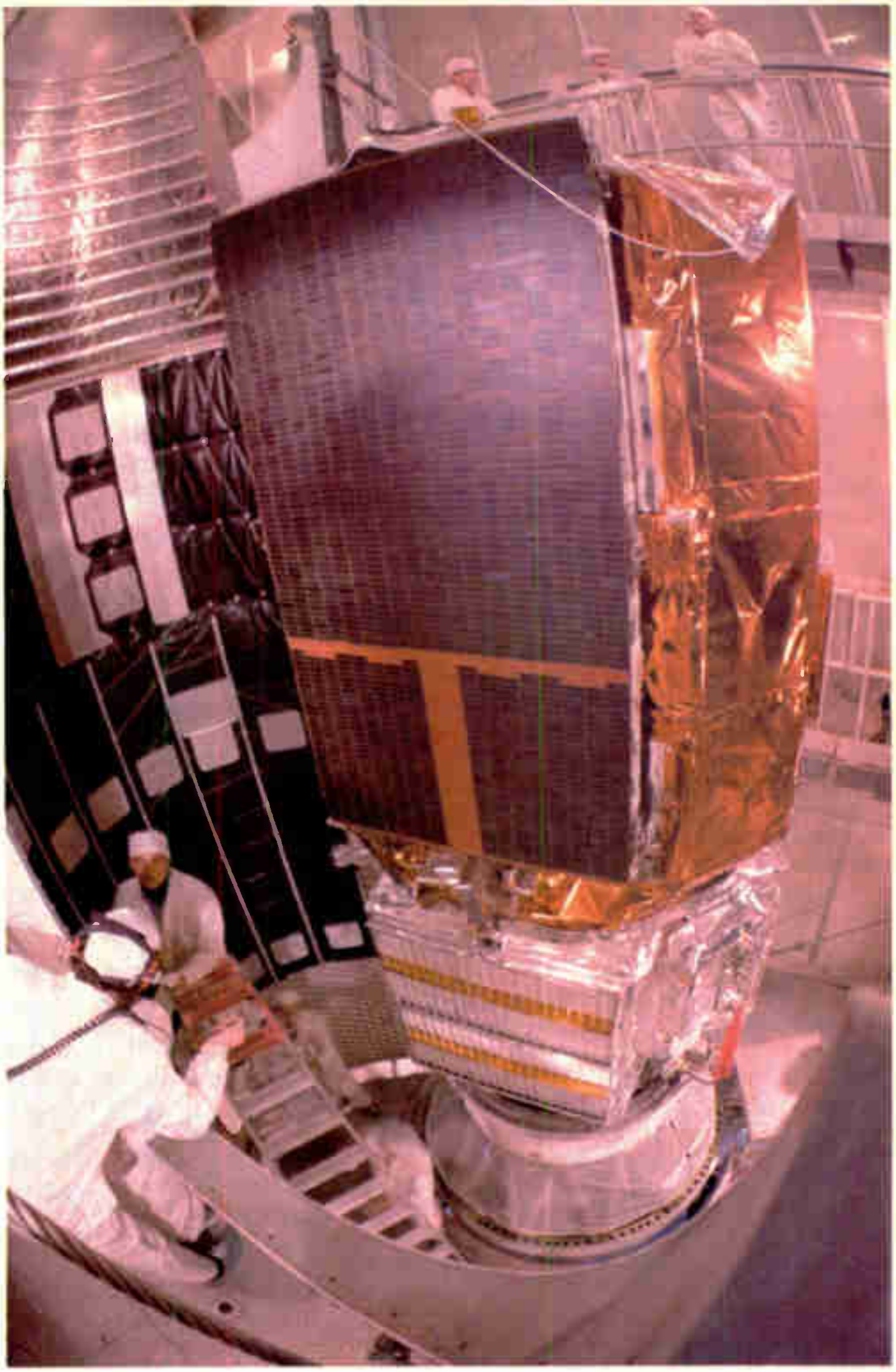
The all-digital system will let Bell carry voice, video, and data while taking full advantage of new large-scale integrated communication circuitry. It is the strongest evidence yet of Bell's commitment to a future all-digital network making extensive use of fiber-optic technology.

The first part of the link will operate at a rate of 44.7 megabits per second—fast enough to handle 80,000 calls per second on the ½-inch-diameter optical cable. Because of the long distance, the cable will have light amplifiers placed at intervals along it, but there will be far fewer of them than in a conventional electrical system. The $79 million system is expected to be extended to Chicago, Atlanta, and Miami later in the decade, with the Boston, New York, and Washington work completed by 1983.

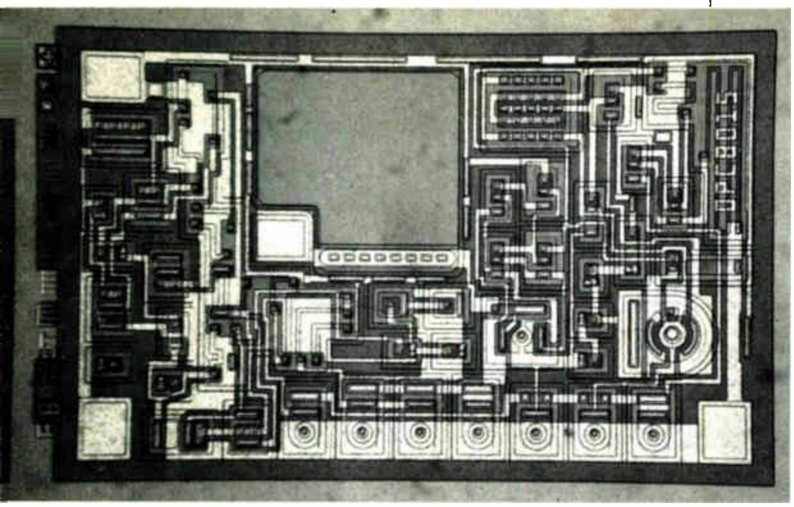
More applications

Looking even farther beyond the land link for the Boston-to-Washington corridor, Bell tested fiber-optic equipment this past year with an eye to laying a fiber-optic cable 6,500 kilometers under the Atlantic to Europe. The cable would have one fifth the cost of projected coaxial cable systems of the same capacity and one third that of today's undersea cable systems.

The system will be powered by indium gallium arsenide phosphide lasers operating at a 1.3-micrometer wavelength—a so-called second-generation system. At this longer wavelength—0.8 μm has been used until now—cable attenuation is lower. Far fewer amplifiers than for a copper-cable system need be placed under the



Retrievable. Launched from Cape Canaveral, Fla., on Feb. 14, 1980, the solar maximum mission spacecraft is the first satellite designed to observe the solar flares that are so destructive to terrestrial communications. It is also the first bird that can to be picked up by the space shuttle and reused.



Integration. Fiber-optic systems for communications are making more use of large-scale integration. Each of the integrated circuits on this TRW-Optron wafer has a photodiode, an amplifier, and a Schmitt trigger and operates as a low data-rate receiver.

sea to boost the signal; in the second-generation system they will be 35 km apart compared with 9 km for the electrical cables.

Each amplifier will have an operating laser and three standbys so the system will have a mean time between failures of eight years—an acceptable figure for submarine cables. The digital amplifiers can carry 4,032 conversations per fiber compared with 200 for copper systems. Messages will be received by p-i-n diodes, which Bell considers far more reliable than the other competitor for this chore, the avalanche photodiode. And unlike the avalanche devices, the p-i-n diodes can operate at low voltage.

Other second-generation fiber optics went into action in an experimental system in September of 1980. As part of its plans to progressively phase out copper-cable trunk telephone systems on new links, British Telecom, part of the British Post Office, transmitted optical data at 140 Mb/s over 49 km of graded-index fiber. The feat was accomplished without amplifiers, using the low-loss optical window that occurs at the 1.5-μm wavelength. A dramatic 90% drop in the fiber loss over the first generation system was achieved for a typical attenuation figure of 0.45 decibel/km. The Post Office expects the decreased attenuation to show up directly as lower-cost systems because of the fewer amplifiers needed.

Office of the future

Computer-controlled communication service became more available in 1980, although some much-heralded systems got nowhere. The Bell Telephone Company of Pennsylvania continued AT&T's move into data and information processing by offering a service delivering voice messages immediately or later, as desired, to other subscribers in the network—a form of electronic mail where the sender specifies phone number, message, and delivery time. Some form of this service will also be offered by Bell's Advanced Communications Service. Telephone-based ACS will offer digital transmission of the outputs of almost every kind of office communication equipment, though software and organizational problems continued to plague it in 1980. Xerox Corp.'s XTEN, a system with similar goals but with microwave transmission for local distribution, was likewise troubled.

The distinction between computers and communications techniques was also further blurred in 1980 by some of the private branch exchange equipment introduced by Rolm Corp. in Santa Clara, Calif.; Plessey Ltd. of Essex, England; Mitel Inc. in Ontario, Canada; and other manufacturers. These PBXs are so intelligent and have so many programmable features that they look like small computers—able to act, for example, as data-entry terminals for the user's main computer.

Home information

The feat of bringing information services into the home via a television set was dominated by the English, French, and Canadians in 1980 as they continued to test their well-developed viewdata systems. But, in a small way, AT&T finally got into the act jointly with the Knight-Ridder newspapers to test such a system in Coral Gables, Fla. There, viewers can choose from some 1,500 pages of information sent over their telephone lines and displayed on special television sets. With the present setup, there is no sound and the graphics are freeze-frame only.

While Bell gets started, Great Britain's Prestel system, available for some years now, supplies customers with up to 150,000 pages of information both in England and the U. S. through a General Telephone and Electronics Corp. license. The French system Antiope was tested, along with the competing British system, in St. Louis in 1980 by the CBS network and a test in France was slated to start near Paris late in the year. And tests of the Canadian Telidon system were announced this year for both the U. S. and Venezuela.

The various systems differ not only in their technical implementations, but in cost, the kind of services supplied, and the degree to which the viewer can interact through his keypad with the system.

The home information system and the very intelligent PBX are but a few of the products and services that AT&T may offer to the home and business community through a new unregulated subsidiary it formally announced in 1980. This event was long expected, but was the year's major news in the complicated world of lawsuits, consent agreements, and conflicts that characterize the data-processing and communications industries. It was Bell's answer to how it would compete in unregulated markets without having the advantage of its regulated operations for financial and technical support.

The dust has still not settled and Bell faces continued challenges, both political and technological, as to how the research, development, manufacturing, marketing, and financing for its new subsidiary will be carried out. Both Federal agencies and Bell's competitors for the various lucrative markets that it wants to get into will have their say.

The new organization is also expected to have a major effect on next year's congressional efforts to rewrite the 1934 Communications Act. This legislation was drawn up before certain present-day communication services could even be imagined, and all concerned parties want to see it revised in the light of today's conditions.

The semiconductor industry continued the drive to bring the benefits of large-scale integration to telecommunications equipment, with most companies introducing or further developing a wide variety of special-purpose chips.

A crowd of codecs

Codec development was a good example of this worldwide effort in 1980. These analog-to-digital and digital-to-analog converters are a major stepping stone toward cost-effective all-digital communications networks.

Besides those appearing out of almost all U. S. semiconductor houses, codecs came from both Europe and Japan. In West Germany, for example, Siemens' two-channel codec—a combination bipolar and C-MOS device, entered production. The SM610 occupies a place between the single-channel approach favored by nearly all U. S. manufacturers and the 4-, 8-, or 16-shared-channel codec made by Precision Monolithics Inc. of Santa Clara, Calif.

Not to be outdone, in February 1980 Plessey Telecommunications Ltd. of Liverpool, England, also decided that sharing is the way to go for certain communication applications. Its 30-channel two-chip device can handle more channels than any other codec.

Finally, on the other side of the world, the Japanese entered the codec market in 1980. Fujitsu Ltd. of Kawasaki was typical with a two-chip set. One chip encodes and the other decodes; both have an on-board filter. This approach eliminates transmitting and receiving crosstalk.

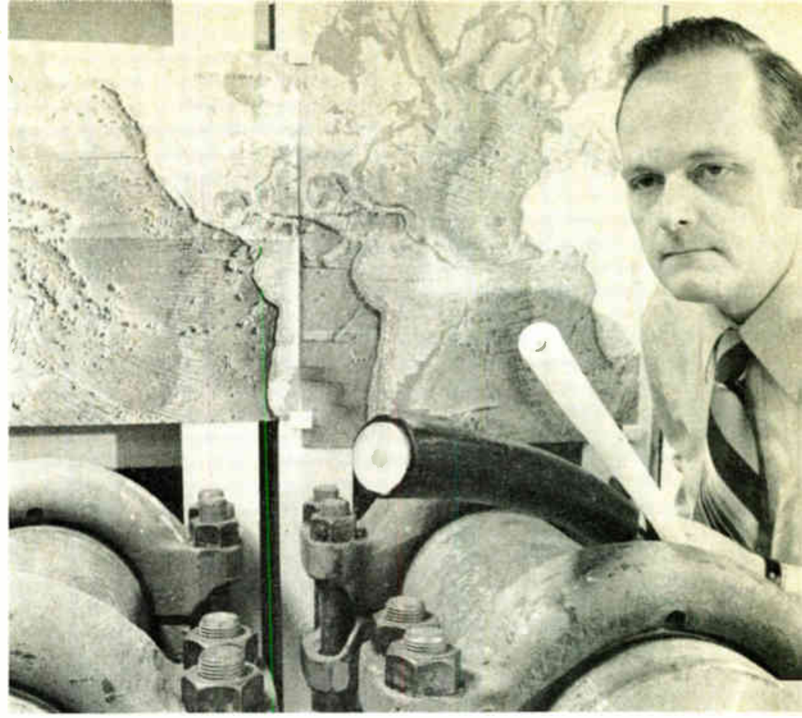
If codecs were accepted by equipment makers, users of both data- and voice-communications systems were slow to adopt another product of large-scale integration—the chips that implement the data-encryption standard. Sales for these chips, meant to ensure that no one but the intended recipient of sensitive material can read it, were slow. But the year saw another development that promised to change the way encryption is done. Software or computer programs started to show up on the market that could do the job the chips were cut out to do; a variety of programs were developed that destroyed the myth that only a hardware or dedicated-chip implementation can yield speedy encryption and decryption.

More birds flying

As more earth satellites joined those already in space, various legal questions about their orbit and frequency assignments were much debated, although few problems were solved.

The World Administrative Radio Conference, which finished several months of discussion at the beginning of the year, is a United Nations–sponsored general meeting occurring every 20 years—although there are smaller, more specialized meetings more often. The purpose of the meetings is to divide up frequencies and satellite orbits to avoid interference and so that both are used in a cost-effective way.

WARC left most questions of how to allocate old, still unassigned frequencies and new frequencies in the 14-gigahertz area still unsettled. Some countries, like Canada, even issued regulations at variance with some WARC regulations. A prime problem: the world is fast running out of synchronous-orbit parking spaces for satellites. This is especially true for North America, and some new proposals for slots filed in 1980 called for places in space that were not so desirable for ground coverage.



Smaller is better. At Bell Laboratories' "artificial ocean" in Holmdel, N. J., Robert Gleason, undersea cable design group supervisor, compares a 1-inch-diameter, 12-fiber cable with its coaxial rival. With at least twice as many circuits, the fiber cable is easier to lay.

The National Aeronautics and Space Administration launched many satellites this year, including one to study the sun. Most important for the future course of space operations, this satellite is retrievable by the space shuttle. Launched on Feb. 14 and dubbed SMM, for solar maximum mission, the bird watches for the solar flares that are peaking this year and next. Early warning of these bursts of electromagnetic noise, which can all but wipe out military and commercial communications, is vital to minimizing and compensating for outages. If the satellite is picked up by the space shuttle in 1982 or 1983 and refurbished for use, NASA says it could save millions of dollars over the cost of launching a new satellite.

Though the SMM is already in orbit, a pickup may never be made; the shuttle's timetable has continued to slip throughout 1980, largely because of difficulty in fastening heat-shielding tiles to the shuttle's skin. Consequently, several satellites planned to be launched by the shuttle were switched over to the tried and true launch-rocket approach. This includes Satellite Business Systems' bird, which is assigned a launch date in November. While the shuttle delays mount, the European Space Agency is going ahead with testing of its low-cost Ariane rocket, which it hopes will compete with the shuttle in offering inexpensive launches.

With 30% more communications satellites in orbit than two years ago, it is getting more difficult to pick up their signals efficiently with one ground antenna per satellite. So, Comsat Laboratories has further developed its multiple-beam torus antenna, deciding to incorporate it in earth stations in West Virginia, Maine, and California to serve as many as seven satellites in the 6-GHz uplink and 4-GHz downlink bands. Such birds are grouped along arcs of a geostationary orbit about 20° wide.

Several beams

The single torus-shaped reflector can generate several beams because of the overlapping illumination of its surface by a number of small, movable antenna feeds. Each beam aims at a specific bird, so that an earth station is simultaneously linked to a number of satellites.

Antennas can be designed to pick up the signals from many satellites, but satellites may also be designed to pick up and relay the signals from many ground transmitters. That is the idea behind the U. S., Canada, France, and Russia's joint project, begun this year to send up specially dedicated satellites to pick up the weak signals from transmitters on downed aircraft.

As the satellite passes over the crash site, the doppler shift of the downed plane's transmitter frequency changes. A measurement of this shift, sent to earth station receivers, will be directing rescuers by 1982.

With the available electromagnetic spectrum becoming even more crowded, all communications system designers and users must be certain they are operating exactly at their assigned frequency. A major step in ensuring this accuracy for the microwave and optical regions of the spectrum was taken this year when researchers at the National Bureau of Standards in the U. S. and Canada's National Research Council teamed up to make the highest direct frequency measurement ever made of an electromagnetic wave.

The feat, accomplished with the cesium-beam frequency standard and a chain of microwave and laser oscillators, is important because measurements based on frequency can be up to 1,000 times more accurate than wavelength checks. The researchers measured 520 terahertz (52×10^{13} hertz), which is in the visible region of the spectrum and is 50,000 times higher than the frequency of the cesium beam oscillator now used as a microwave frequency standard.

The 520-THz measurement required a chain of 14 lasers and 6 klystrons (microwave tubes) to determine the frequency of a neon laser operating near 260 THz. After this was done, a helium-neon laser from Canada's research council and a frequency-doubling crystal was used to make the 520-THz measurement.

NASA's Burr: chief of retrievable satellite project

At the National Aeronautics and Space Administration's Goddard Space Flight Center, Peter Townsend Burr is the project manager for the Solar Maximum Mission. A NASA employee for 20 years, Burr had the pleasure of seeing the successful launch of the satellite—the first ever to be devoted entirely to observing and analyzing solar flares—on Feb. 14 of this year. And it was he who had made sure the SMM met its scheduled launch date and budget—no mean feat since work started six years ago.

The SMM is now orbiting with seven instrumentation packages sending back data for U. S., English, and Dutch scientists to study. A severe sunspot cycle was predicted for 1980, and this effort was aimed at a better understanding of those massive electromagnetic eruptions 93,000,000 miles away that can wipe out both commercial and military radio communications. But, too, the state-of-the-art of solar-flare instrumentation had advanced to the point where it was the logical next step to launch a dedicated mission.

The SMM has an impressive list of design firsts for space technology. Not only is it the first satellite to be dedicated to solar flares, but it is also the first with specific mechanical and electrical design features that will let the space shuttle retrieve it. Reusable satellites that save millions of dollars have long been the dream of spacecraft engineers, who will have no trouble thinking of new experiments to perform with the money that would otherwise go toward building new birds.

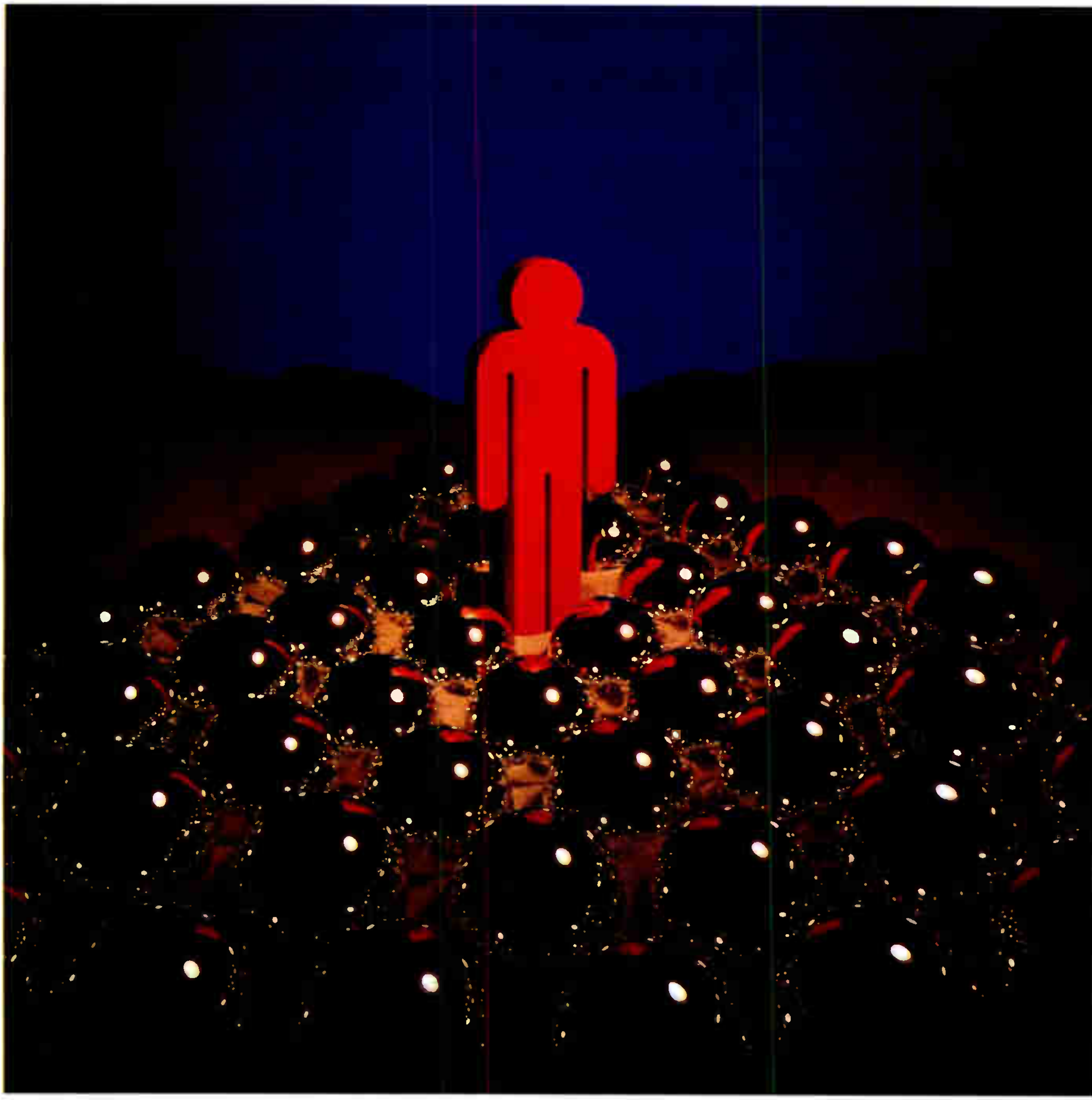
"We plan an early 1984 retrieval," says Burr, 45 years old and a University of Virginia electrical engineering graduate. But he somewhat wistfully adds that, by that time, NASA will have put him to work on some other project—probably "the Upper Atmosphere Research Satellite, which is in NASA's 1982 budget proposal."

Some folks are, by now, jaded by space firsts, but not Burr. His enthusiasm for his work is obvious as he relates that "the SMM is also the first satellite to have modular instrumentation and transmitter components designed to be serviced by the shuttle while the satellite is in orbit. It will also have an antenna on board—not deployed at present—for communicating with the first TDRS satellite when that data-relaying satellite is launched in 1982."

To make the SMM retrievable, Burr, though an EE, had to oversee a lot of mechanical engineering effort, much of it being done for the first time. The satellite's solar-array panels, for example, were designed to be ejected rather than folded up just before the bird is tucked into the shuttle's cargo bay for the return journey.

The technical stresses of the shuttle pickup were a major problem. "All of our stress analysis had to be based on shuttle load factors rather than just the classic Delta rocket launch vehicle," he says. Even more fundamental, the SMM had to be designed with a grapple system and mounting so the shuttle retrieval arms could grab it.

Satellite project management is no new task to Burr who, as he modestly puts it, "has been lucky." In a four-year period in the early 1970s, before working on the SMM, he was spacecraft manager for a series of synchronous meteorological satellites. He watched the launch of the first of those, also. **-Harvey J. Hindin**



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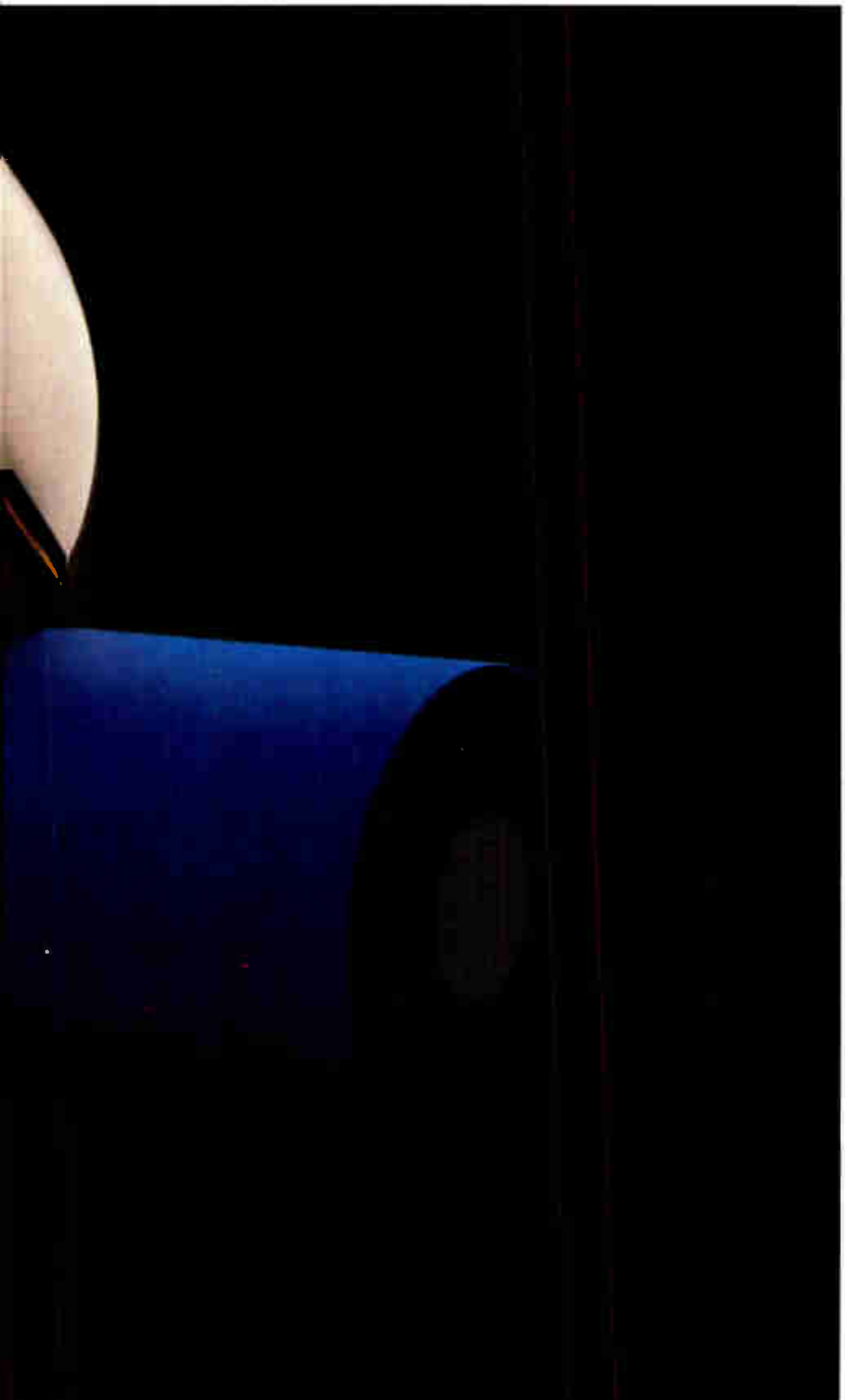

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CONSUMER

Entertaining the eye and the ear are sharper TV pictures, a choice of video disks, and more talking toys; teasing the brain are pocket computers; videotext is on the way; and automotive electronics is improving car mileage

by Gil Bassak, *Industrial/Consumer Editor*

Consumer sales of electronic products are at the opposite end of the spectrum from research and development. They are perhaps the ultimate test of R&D—its final destination on a journey that often ends with the ubiquitous television receiver.

Not surprisingly, TV pictures this year are clearer—comb filters are in place and integrated circuits have refined the art of remote control. Video disks are poised for the test of consumer acceptance as suppliers amass software and disk-stamping facilities. Video cassette recorders have recently spawned a smaller and more portable breed that threatens to supplant the 8-millimeter movie camera. And though progress for videotext in the U. S. remains stymied by a lack of industry standards, ongoing tests of numerous systems continue.

The year 1980 marked the birth of the pocket home computer, as well as the first entry by the Japanese into the U. S. personal computer market. Speech synthesis, like video disks, is gaining momentum, as myriad integrated devices promise the low production costs demanded by toy, auto, and appliance makers.

Finally, clever use of the microcomputer has plucked automobile manufacturers from the Environmental Protection Agency's grip. Detroit is going electronic both under the hood and behind the dashboard to meet stringent EPA standards without sacrificing performance.

The most significant change in television receiver design has been the widespread use of comb filters for better picture quality. The filters, which appear as discrete glass–delay-line devices as well as in integrated form, are particularly effective in separating the interlaced chrominance and luminance signals. Although these devices have been known for decades, the manufacturing cost has been prohibitive.

The integrated charge-coupled-device comb filter from RCA Corp.'s Consumer Electronics division in Indianapolis is particularly noteworthy. Unlike its glass–delay-line counterparts in some other sets, it is a single integrated component and thus is advantageous in reducing manufacturing costs. The integrated comb filter improves picture quality beyond that of the discrete glass–delay-line version since unlike that version, which operates only at the 3.58-megahertz peak of the chrominance signal, it operates across the entire 4.5-MHz baseband frequency range of the video signal. The result is enhanced vertical detail and a sharper picture.

Better remote control for TV

In other developments, integrated phase-locked–loop circuits like the MC145144 from Motorola Inc. in Phoenix, Ariz., as well as infrared emitters and detectors, have served to eliminate the expensive and noisy mechanical kludges associated with past remote-control tuning systems. In the U. S., for example, electronic tuning and remote control are in a record number of sets.

In Europe, West Germany's Grundig AG went to market last fall with a single-chassis series that has all its circuitry packaged in a dozen metal-clad modules. Top-of-the-line versions have synthesized-frequency phase-locked–loop tuners with automatic search for up to 30 preselected stations. The tuning memory, the synthesizer, and the search function are implemented with com-

Video disks. Fueling the race to develop a consumer video disk system is the lower cost of producing the vinyl disks, compared with magnetic tape cassettes. As shown here at RCA, both the grooved, capacitance electronic disk and the electromechanical pickup stylus are tested to maximize longevity and wear resistance.

conversion and a variety of compression techniques to reduce the memory requirements for storing the phrases, vastly different from TI's vocal tract model. National is selling the chip sets for about $12 in large quantities.

Finally Votrax, an old-timer in the speech-synthesis field, offers a single complementary-MOS chip that requires a minimum of memory and a simple controller. However it offers a potentially unlimited vocabulary. Since speech is formed from phonemes, or basic speech sounds, rather than previously coded words, no high-powered processing is required to develop the phrases. The Votrax SC-01 sells for $12 in OEM quantities.

Electronics moves into the car

The past year found the basic engine-control electronics needed to meet emission and gas mileage requirements, and auto makers are turning their talents to developing electronic accessories like cruise control and special dashboard displays, as well as entertainment electronics.

Some of the most advanced systems appeared in 1981 models from General Motors Corp., Detroit. GM's Computer Command Control, built around a custom microcomputer, coordinates spark advance, air-fuel ratios, exhaust gas recirculation (EGR), vapor canister purge, and air management—the control of fresh air to the catalytic converter.

One of the most exotic advances is the so-called Modulated Displacement System on GM's 1981 Cadillacs, which varies the number of cylinders operating in the engine. Either eight, six, or four will fire according to the load and speed of the car. The ability to perform this is a direct function of the engine parameters sensed and fed to the microprocessor.

GM also added built-in test equipment that lets a serviceman check for faulty subsystems. Error codes are read out either on blinking light-emitting-diode displays (for example, two blinks mean the number two) or in the Cadillac, on the climate-control temperature display.

In the passenger compartment, Chrysler, Ford, and GM hope to attract buyers with eye-catching electronic displays reading instantaneous fuel consumption, miles-to-empty calculations, and a message center for monitoring engine status.

Keizer and Clemens: inventors of RCA's video disk system

When RCA Corp. begins shipping its SelectaVision video disk system early next year, it will be in large part because of the work of two men. Both Eugene O. Keizer and Jon K. Clemens have been involved with the video disk project at RCA's Research Laboratories in Princeton, N. J., ever since its inception in 1965, and both believe that their capacitive pick-up design will be easy to manufacture, easy to use, reliable, and relatively inexpensive.

Keizer, 62, has now spent 40 years with RCA, having joined directly after receiving his undergraduate degree in electrical engineering from Iowa State University in 1940. The list of projects he has worked on includes microwave circuitry design and early radar development during the war years. After World War II, Keizer spent much of his time examining fm and television communication, putting much of that knowledge into the development of color TV over the next 10 years.

After that, he notes, "I moved into interdisciplinary projects. Around 1960, people at the labs started looking at ways of storing large amounts of information, and they reached the conclusion that the technique used to press audio records could store much more data" than magnetic media could. With his background in communications and TV, Keizer was an obvious choice for the video disk research project. He is now the staff scientist for the video disk systems research laboratory.

Clemens, 42, also joined RCA directly after leaving school; he received his Ph.D. in electrical engineering from the Massachusetts Institute of Technology in 1965 and has been with the labs ever since, working on the video disk system. At present he is the head of signal systems research. "My whole professional life, and over one third of my entire life, has been devoted to the video disk," he comments. Clemens figures his background in information transmission and his interest in electronic systems helped him to formulate a design approach to the project. "We studied all the systems—optical, pressure, even holographic—but we finally settled on the capacitive-type system," he points out. "We even gave demonstrations in some of the other technologies to higher management just to prove we could handle them. We opted for the capacitive approach around 1967–68."

Clemens has a word of caution for other research scientists like him and Keizer. "It's very tempting to go after the exotic," he observes. "But the consumer doesn't care if the most exotic component is in his system. A definition of what is best is very often 'how easy it is to operate?' or 'does the disk warp?' "

Clemens has a few thoughts on the future of video disk. "Obviously the technology we're using in the video disk can be applied in the digital audio area," he says. He notes that "multiple pick-up heads could be put on one machine to get a totally different output from either single signal." But perhaps most importantly for Clemens, "this multiple-head technology will open the door to non-FCC standards for television-type programs. If you make the player, supply the medium, and provide the programming, some very interesting technological approaches arise. It certainly will allow some room for experimentation."

-Pamela Hamilton

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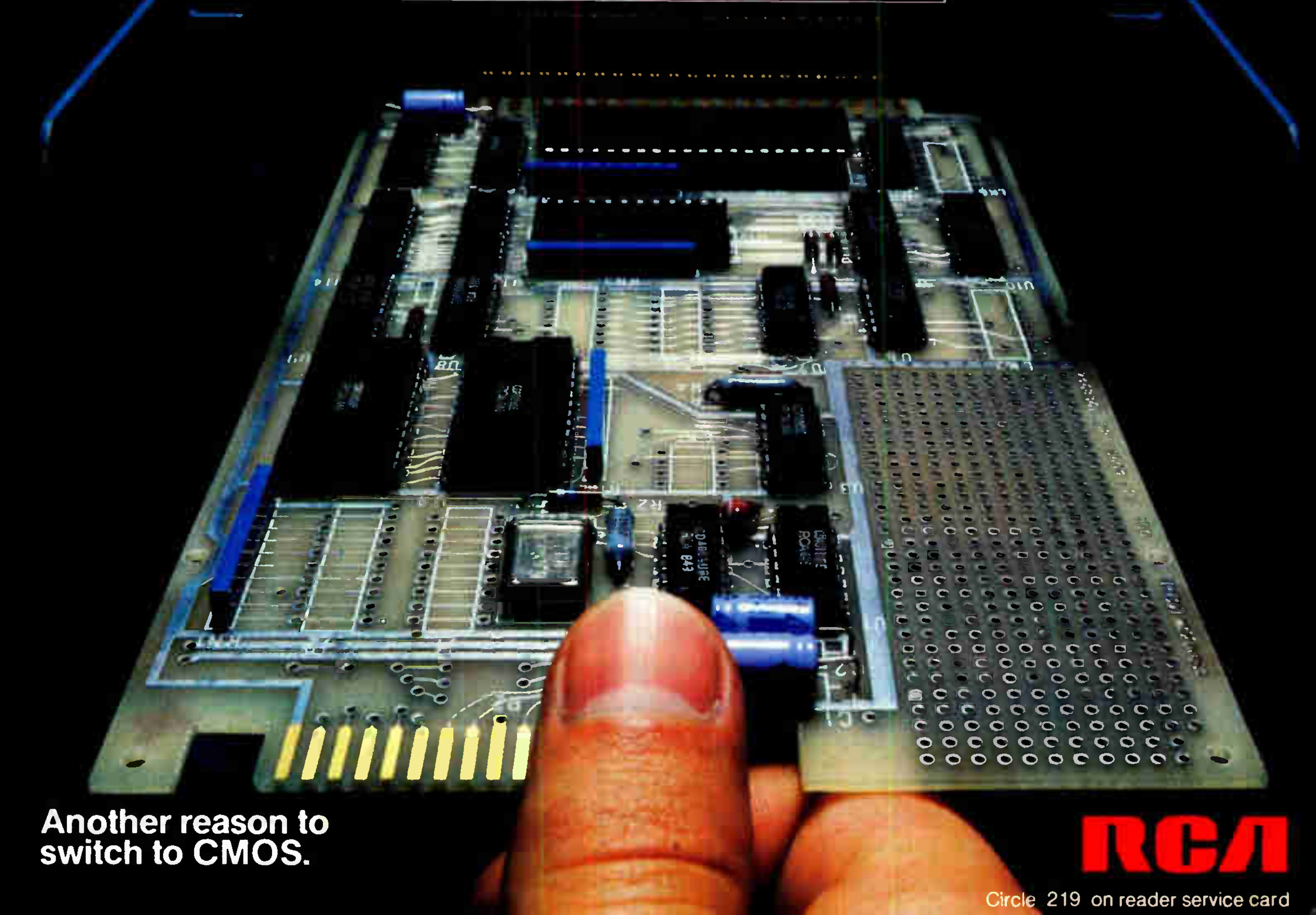
	RCA (CDP18S604)	Intel (SBC-80/04)	Mostek (MDX-CPU-1)
RAM	512	256	256
Complete with I/O	yes	yes	no
Expandable	yes	no	yes
Prices (1-9 Units)	$199	$230	$260



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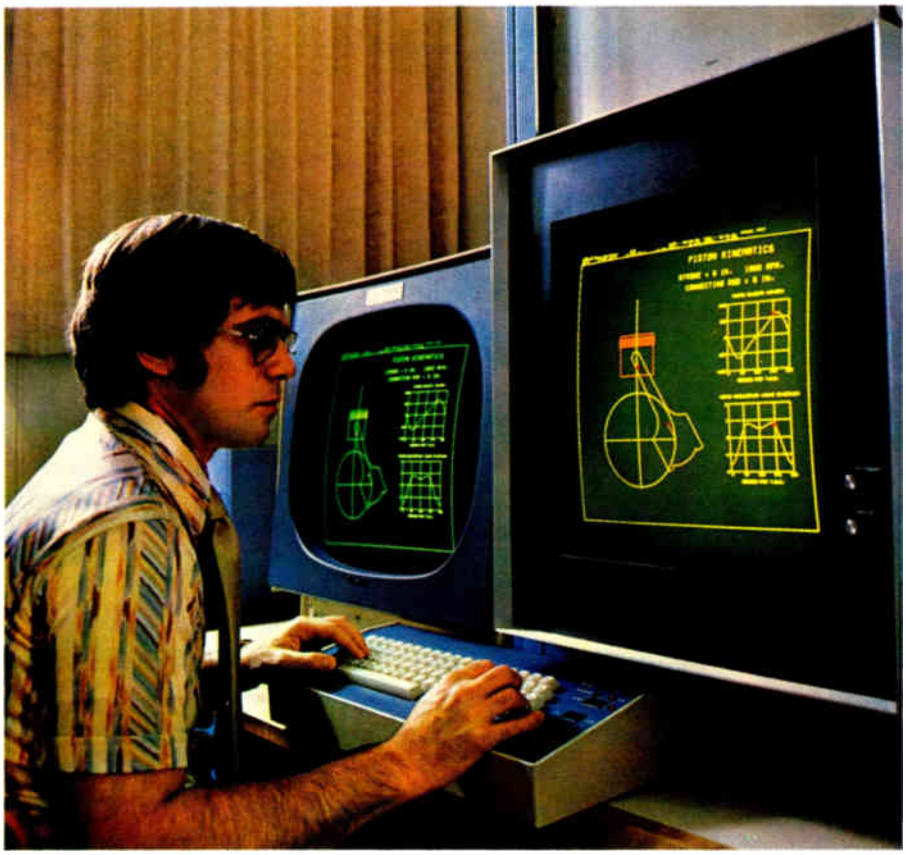

Exemplifying what state-of-the-art CAD technology can do for manufacturers, Chrysler Corporation Chief Engineer Robert Brauburger reports dramatic gains in the speed and efficiency of their design process. Above: a Chrysler engineer uses a color graphics terminal to analyze piston performance. Below: the control room at Chrysler's Technical Computing Center, where an operator monitors four interconnected Control Data® CYBER 170 systems.

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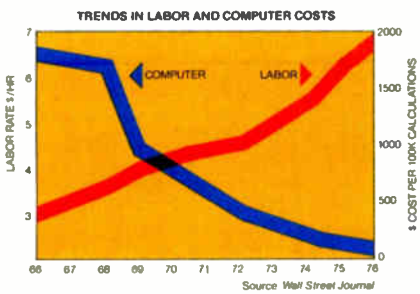

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Boeing, a long time user of Control Data computers, recently installed two CYBER 175's in a CAD/CAM center to assist in the design of its new generation of passenger aircraft.

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Circle 221 on reader service card

PACKAGING & PRODUCTION

1980's big discovery is the laser's many talents as a production tool; chip-carriers are entering the packaging mainstream and forcing circuit boards to change

by Jerry Lyman, *Packaging & Production Editor*

The laser is carving out several new careers for itself in welding and chip and board processing. Originally developed for wideband communications, the narrow beam of coherent light has long been used to scribe and mark silicon and ceramic substrates or trim thick- and thin-film resistors. Then within the past 12 months, it began annealing silicon wafers damaged by ion implantation, turning up in advanced chip processing, writing patterns on resist-covered printed-circuit boards, and also welding flexible circuits to connectors.

Accompanying the burst of laser activity were two strong trends in the chip-carrier field. This year, more and more integrated-circuit manufacturers began supplying linear as well as digital ICs either in leadless ceramic chip-carriers or in such carriers mounted on leaded ceramic motherboards. Meanwhile, the attaching of chip-carriers to plastic printed-circuit boards rather than ceramic substrates is on the increase.

The chip-carrier development has prompted several modifications in pc board design—namely, narrower lines and spaces, extra conductive layers, and the replacement of plated through-holes by solid vias, since chip-carriers are not inserted but surface-mounted.

Chip processing

LaVerne Hess, head of the laser chemistry section of Hughes Aircraft Co.'s Research Laboratories, Malibu, Calif., is enthusiastic about the potential of laser IC processing. Calling it "a revolutionary change," he says it promises "improvements in semiconductor device performance, packing density, yield, and reliability that extend beyond the reach of conventional techniques." He also sees altogether new possibilities opening up in several aspects of solid-state device fabrication.

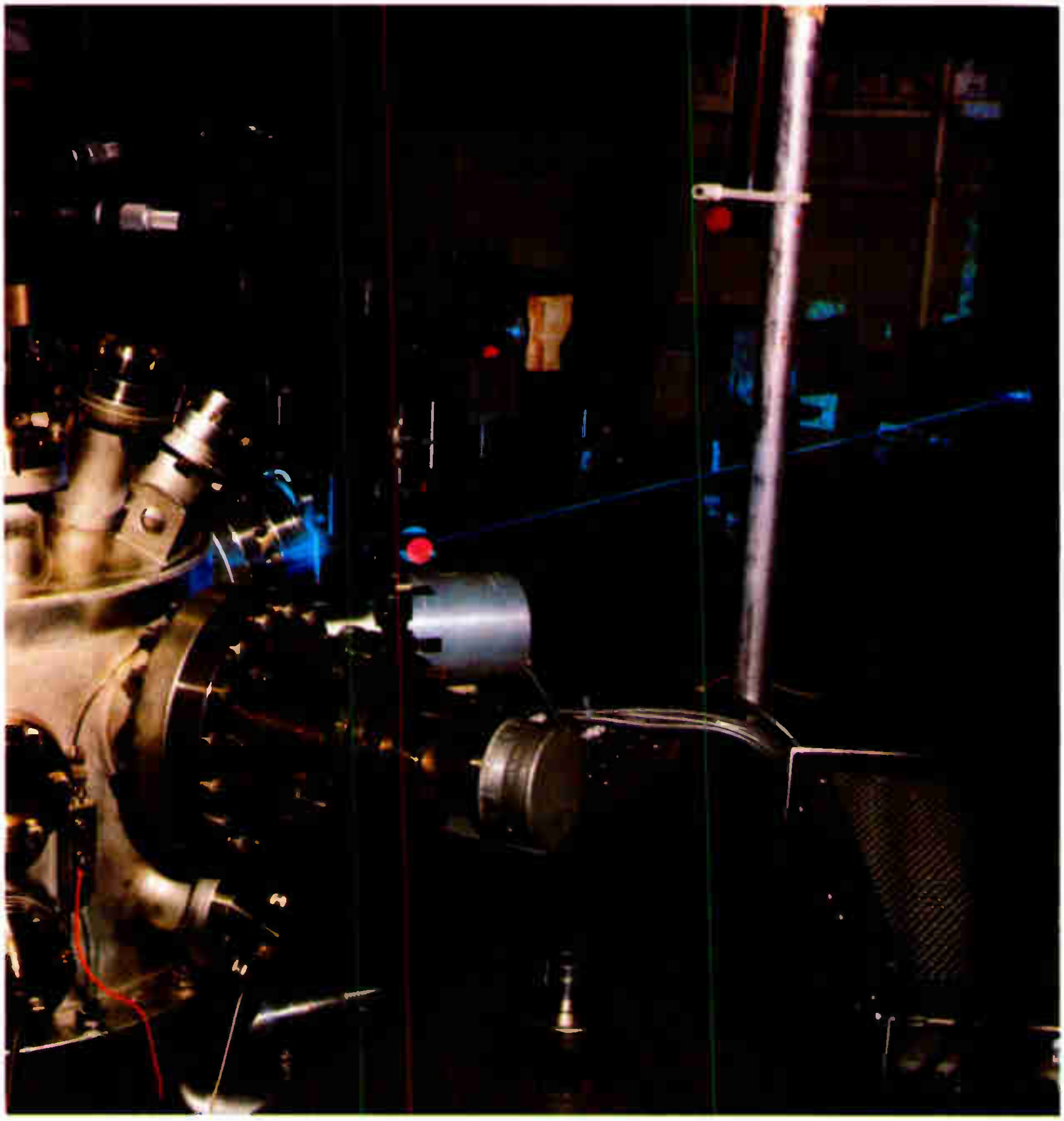
The twin strengths of laser processing are its ability to spot-heat very limited areas, for a very limited time. These attributes improve device performance by improving and even changing material properties. They also make possible new IC configurations such as stacked structures, with alternating layers of polysilicon and silicon oxides, for charge-coupled devices or random-access memories.

Already a wide range of lasers has been tried out as possible tools for IC processing. The table lists some of the more popular types and their critical parameters, such as penetration depth and pulse duration.

The first use of the laser in IC fabrication came last year with the experimental annealing of ion implantation damage on silicon wafers. By now this has become one of the more popular production applications of the laser, but many more possible uses of the device for IC fabrication are now being studied at research and development facilities here and abroad.

At Hughes' Malibu laboratory, for instance, lasers have proved adept at forming ohmic contacts, annealing polysilicon resistors, doing laser epitaxy, and annealing silicon on insulators (sapphire, silicon oxide, and silicon nitride). Other talents of theirs are reflow step coverage and backside gettering of wafer defects.

Gettering of semiconductors reduces crystalline defects in wafers by melting the silicon and allowing it to



Beaming. The laser has a bright future in IC processing to which its localized heating and small spot size contribute a high degree of control. In fact, silicon wafers can now be completely processed by various beams inside a single vacuum chamber. This experimental apparatus at Hughes' Malibu labs has an electron-beam evaporator and an ion implanter sealed inside it, plus an optical window through which a laser beam enters.

I/O pads on 50-mil centers. New types of boards are therefore either being made or in planning.

The new chip-carrier orientation produces a board with thinner pc traces, about 5 mils wide, and many more inner conductive layers interconnected by a grid of small vias on 50-mil centers. There are no through-holes because there are no component leads.

At present, two major factors are holding back the mass production of these boards. For one thing, it is hard to solder ceramic carriers to conventional laminated-plastic pc substrates because the two materials have very different coefficients of thermal expansion. However, there is an industrywide push to solve this problem and when the solution emerges, which may be soon, the via will replace the plated through-hole, since all components will be surface-mounted.

The second problem, plating 5-mil lines to a tight tolerance and plating small deep vias with a high aspect ratio, already is well on the way to being solved.

This year PCK Technology division of Kollmorgen Corp., Glen Cove, N. Y., developed an additive plating process called CC-5 that could be suitable for the densely packed multilayer boards of the future. CC-5 can put down 5-mil lines and spaces to a ±1-mil tolerance along with achieving an aspect ratio of 10:1 in plating through-holes. PCK has already used its new process to plate a grid of solid vias 20 mils in diameter on 50-mil centers on an 11-layer board—a unit typical of those carrying arrays of chip-carriers.

By the late 1980s advances in very large-scale integration may have forced even further changes in pc boards. Their makers may have to switch over to hybrid-like processes that form conductors and vias photolithographically and eliminate such operations as drilling.

Another future possibility is a substrate of the kind made by Pactel Corp., Newbury Park, Calif. Its thin layers of polymide, additively coated with copper patterns and vias, are laminated to a heat-sinking plate. A 3-in.² four-layer substrate of this type with 3-mil-wide lines and spaces and 4-mil vias can hold 48 medium-scale chips and 28 small-scale ICs all attached to it by tape-automated bonding.

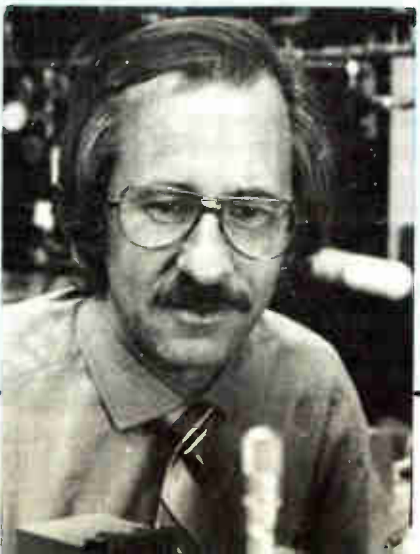
Hess: leader in laser processing

In the scramble to push semiconductor device geometries down to the submicrometer dimensions of very large-scale integrated circuits, it turns out that the much-publicized progress being made in lithography is not enough. While critical, it must be backed by concurrent improvements in other basic fabrication steps as well.

At the forefront of developing solutions, LaVerne D. Hess and associates at Hughes Aircraft Co.'s Malibu Research Laboratories, Malibu, Calif., have helped define what he calls "a new breed of fabrication activity." His generic term is "directed energy beam processing," and the Malibu group has made notable advances in annealing ICs using lasers rather than furnaces.

Hess, 46, has been at the Malibu labs since 1965, the year he received his Ph.D. in physical chemistry from the University of California, Riverside. He has been in laser research "since its inception in the early '60s," he points out. He now heads the laser chemistry section's chemical physics department.

The heart of the problem addressed by laser annealing is that high furnace temperatures (up to 900°C for a half hour) may cause ion-implanted IC-transistor source-drain regions each to "wander" as much as 0.25 micrometer. Although this works all right for present 3-to-4-μm geometries, at the 1.25-μm levels called for in the zero phase of the VHSIC program, for example, it is unacceptable. It has bad effects across the board—not only reduced device speed and variable threshold voltages, but higher current leakage that boosts power consumption.



"We have found that with laser annealing we can keep the dopants in the same position," explains Hess. As an example, he cites an n-channel MOS transistor, where a continuous-wave laser "in a few hundred microseconds, or on the order of a millisecond, activates the ions and maintains their distribution in the proper dimensions."

Experiments in laser annealing over the past year or so by Hughes have proved its importance as a new technique for fabricating submicrometer circuits, say industry sources. Underscoring its potential is the fact that several semiconductor and computer firms are either intensively studying or setting up operations to exploit it.

Even for a customarily fast-moving industry, beam processing has come on the scene quickly. Hess is the best illustration of this: he has been working with the technique only since 1977.

The approach is also very interdisciplinary, drawing on specialists with general and diagnostic materials backgrounds, as well as semiconductor experts and Hess's own fundamental science and laser experience. Hughes is in an ideal position to pioneer in beam processing because it has programs and top personnel in all the necessary areas.

Another reason for the research lab's fast pace are the attitudes of Hughes' management towards R&D, which encourage getting results out fast and widely to the scientific community. Publicizing Hughes studies "definitely helped us with good feedback," says Hess.

At present, laser annealing is the subject of a phase 3 VHSIC award, along with more of Hughes's own internal research. Also engaging Hess's attention are related, basic theoretical studies of the advantages of growing crystals with a laser heat source. A hitherto impossibly precise degree of control seems possible. To Hess, this finding shows "beam processing is just starting to evolve and lots more research is still needed." **-Larry Waller**

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CHRONOLOGY

October 1979

- Standard Elektrik Lorenz AG, Stuttgart, West Germany, attains an attenuation of 0.31 dB/km in a graded-index optical fiber, the lowest ever reported. *Oct. 11, p. 73*

November 1979

- The National Bureau of Standards performs the highest direct-frequency measurement ever made on an electromagnetic wave—520 THz. *Nov. 8, p. 12*
- Intel Corp. introduces the first high-speed 16-K static RAM, which uses overlapped implanted areas to minimize masking steps. *Nov. 22, p. 40*
- U. S. Air Force's Rome Air Development Center employs ultraviolet exposure system to fabricate submicrometer lines in SAW filters. *Nov. 22, p. 46*

December 1979

- ITT announces a single-chip 4-bit microcomputer in C-MOS, its SAA 6001, which has a dissipation of only 45 μW in standby and 135 μW in operation, the lowest thus far reported for such a device. *Dec. 6, p. 65*
- Japanese researchers from the now defunct VLSI Cooperative Laboratories describe quadruply self-aligned MOS, claiming that the process produces the smallest possible dynamic RAM cell. *Dec. 6, p. 125*
- Toshiba unveils the first all C-MOS 16-K static RAM. *Dec. 6, p. 125*

January 1980

- IBM fabricates a 30-nm-wide niobium "bridge" that suggests junctionless Josephson circuit elements can be built. *Jan. 3, p. 41*
- RCA American Communications announces that its missing Satcom III communications satellite probably self-destructed in its launch orbit. Total losses—$70 million. *Jan. 3, p. 46*
- Bell Labs announces a polysilicon fabrication process that produces ICs capable of handling up to 500 V. *Jan. 31, p. 41*
- AT&T petitions FCC for construction permit to build a 611-mile fiber-optic link between Boston, New York, Philadelphia, and Washington. *Jan. 31, p. 41*
- Motorola launches its EXORmacs development system, the first to employ a bus structure that supports 32-bit microprocessors. *Jan. 31, p. 81*

February 1980

- MIT's Lincoln Lab builds the fastest three-terminal semiconductor—a GaAs Schottky barrier transistor that can operate at 17 GHz. *Feb. 14, p. 39*
- Data General succeeds in reducing the central processing unit of its Eclipse C/350 to a single silicon chip. *Feb. 14, p. 119*
- NEC-Toshiba and Nippon Telephone and Telegraph's Musashino Lab jointly announce the first 256-K dynamic RAMs. *Feb. 14, p. 138*
- Matsushita introduces the first fully static 64-K RAM. *Feb. 14, p. 138*
- National Semiconductor designs a successive-approximation a-d converter in C-MOS, a monolithic 12-bit device having only a 50-μs conversion time. *Feb. 14, p. 146*
- Tektronix unveils the 7854, the first programmable oscilloscope capable of transmitting and receiving waveforms over the IEEE-488 bus. *Feb. 28, p. 39*
- NASA launches the sunspot-charting SMM, the first satellite designed to be retrieved by the space shuttle. *Feb. 28, p. 48*

March 1980

- AT&T announces plans for a cost-effective transatlantic fiber-optic communications link. *March 13, p. 39*
- Japan's VLSI Cooperative Labs announces the first half-megabit monolithic dynamic RAM. *March 13, p. 42*
- National Semiconductor becomes the first to supply a speech-synthesis IC, its 40-pin SPC device, to OEMs. *March 27, p. 39*
- Hybrid Systems announces the DAC 370-18, the first microprocessor-compatible d-a converter to combine 18-bit resolution and 16-bit linearity. *March 27, p. 199*

Significant developments in electronic technology reported over the past year in *Electronics*

April 1980

- MIT's Lincoln Lab designs optical a-d converters for 2, 4, and 6 bits that can perform up to 2 billion conversions per second. *April 24, p.33*
- Researchers at Thomson-CSF develop gallium indium arsenide phosphide laser that operates at room temperature. *April 24, p.80*
- Following quickly in IBM's footsteps, Dastek Corp., Los Gatos, N. M., becomes the first independent to sell thin-film disk drives. *April 24, p.201*

May 1980

- NEC develops a 512-K ROM, four times larger than state-of-the-art devices, by utilizing electron-beam, direct-writing-on-wafer lithography. *May 8, p.39*
- Data General enters the 32-bit computer market. With its Advanced Operating System/Virtual Storage, its MV/8000 is unusually compatible with existing 16-bit systems. *May 8, p. 185*

June 1980

- A new high in supercomputer performance is reached by Control Data's Cyber 205, which does a staggering 800 million floating-point operations per second. *June 5, p.34*
- Kurzweil Computer Products Co., Cambridge, Mass., announces speech-synthesizer system with unlimited vocabulary that is OEM-board–compatible. *June 5, p.42*
- Advancing the state of the disk-drive art once again, IBM unveils its model 3380, which stores 1.26 billion bytes per spindle, four times more than the 3350. *June 19, p.35*
- Hitachi introduces an EE-PROM, the HN-48016, whose 16-K capacity is the largest thus far attained with MNOS technology. *June 19, p.206*

July 1980

- AT&T initiates test of the first long-wavelength (1.3 μm) fiber-optic telephone system, in Sacramento, Calif. *July 3, p.59*
- Systems Engineering Labs, Fort Lauderdale, Fla., announces the first 32-bit single-board computer. *July 3, p.212*
- Lincoln Lab develops a programmable SAW convolver for improving jamming resistance in spread-spectrum communications systems. *July 31, p.41*
- AT&T and Knight-Ridder Newspapers Inc. launch first national test of a viewdata system in Coral Gables, Fla. *July 31, p.44*

August 1980

- First fusible-link C-MOS PROMs from Harris hit the market. *Aug. 14, p.36*
- Communications Transistor Corp. in San Carlos, Calif., comes up with a line of high-frequency high-power devices that are housed in plastic packages. *Aug. 28, p.42*
- Texas Instruments introduces the first n-channel FET-input, bipolar op amps. *Aug. 28, p.46*
- RTC–La Radiotechnique Compélec ships the market's fastest 1-K static RAM memories to its suppliers. Maximum access time is 10 ns. *Aug. 28, p.67*
- Siemens develops method for viewing undulations of SAW devices, enabling researchers to better understand the mechanisms active in such components. *Aug. 28, p.73*

September 1980

- In a process created by Photowatt International Inc., Tempe, Ariz., thick-film conductors additively plated with copper combine to cut the cost of solar-cell manufacture. *Sept. 11, p.40*
- Texas Instruments, Motorola, Hitachi, Toshiba, Mitsubishi, and Fujitsu all agree that they must protect their 64-K RAMs, using overcoats, against alpha radiation. *Sept. 11, p.41*
- AT&T announces the birth of its fully separate business subsidiary to compete in the deregulated telecommunications market. *Sept. 11, p. 100*
- Inmos announces the fastest 16-K RAM to date, the IMS1400, a 16-K-by-1-bit static device that sports a typical access time of 30 ns. *Sept. 11, p.117*
- Datel-Intersil, using an error-distribution scheme, introduces an 8-bit successive-approximation a-d hybrid converter with 12-bit linearity. *Sept. 11, p.171*
- Hewlett-Packard introduces the first autoranging oscilloscope, its 1980A. *Sept. 25, p.41*

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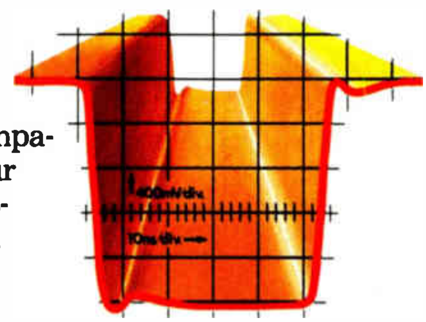

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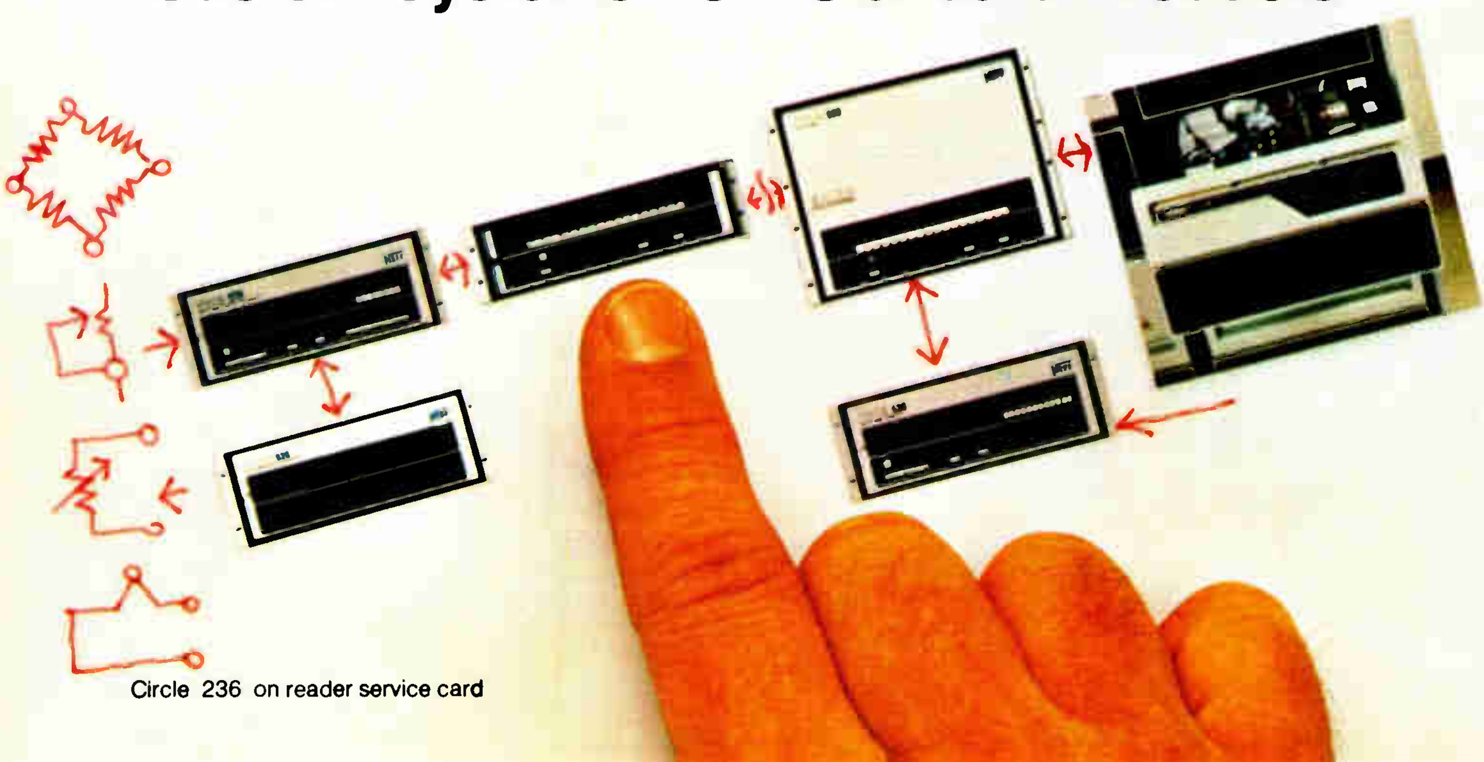

Circle 236 on reader service card

Roundup: Winchester controllers shrink

The recent proliferation of one-board controllers for 14- and 8-in. Winchester drives includes some for under $1,000

by Ana Bishop, Assistant New Products Editor

The proliferation of hard-disk drive controllers on single boards—a rare sight at this time last year—has obviously been facilitated by the availability of microprocessors. But drive makers themselves figure prominently in the current trend to offer the controllers at reduced prices and sizes.

Prices for about 20 controllers for 8- and 14-in. drives introduced since spring range between just under $5,000 to $300 (see chart on following pages), depending on number and type of drives controlled, error-correction capabilities, interfaces, the size of the computer it interfaces with and other extra features. When an 8-in. Winchester drive sells for $4,500, a controller that costs the same or more than that is hard to justify. It is even more difficult to justify if it is a two-board controller, with logic on a separate board—a controller that is perhaps twice the size of the drive.

"If you have a drive like the Kennedy 5300, which offers 42 megabytes of memory for $2,600, you can't ask $3,000 for a controller," says Allan Krosner, vice president and technical director of Distributed Logic Corp. (Dilog), "so you make a cheaper controller. Also, if you have a small computer like an LSI-11, you are really limited in size. Going to an expansion chassis is out of the question, so you go for the cost of a microprocessor board that will reduce the real estate."

"Size is the key," agrees Chris Bailey, marketing manager for boards at Piiceon Inc.'s OEM Computer Products division in San Jose, Calif. "The users of the desktop computers have the same computing needs as the big guys but lack the money and space. We have cheap computing power now and cheap video and I/O devices. What we're lacking is cheap memory."

"One objective should be a controller priced at less than half the cost of the drive," says Jim Toreson, president of Microcomputer Systems Corp. His company, Piiceon, and Western Digital Corp. seem committed to just that. Western Digital's yet to be introduced WD1000 [*Electronics*, June 19, p. 106] will operate both 8- and $5^1/_4$-in. hard-disk drives for around $350. So will Piiceon's upcoming controller [*Electronics*, Aug. 14, p. 181]. And Microcomputer Systems' MSC-9000 [*Electronics*, June 19, p. 48] packs 75% of the circuitry of a controller for a variety of drive sizes into a 3-in.-square package priced around $300 (see photo). With interfaces and additional circuitry, a complete controller would still cost under $600.

Cost. Falling prices should in time fulfill the wish of the drive manufacturers—to encourage potential OEM users to install the new drives. In fact, the drive manufacturers themselves are either developing or encouraging the manufacture of the low-cost single-board controllers. Shugart Associates, for one, introduced the SA1400 this spring [*Electronics*, April 24, p. 208], a multidrive, multimedia controller priced between $995 and $1,420. "Our main purpose in getting into controllers is to help customers integrate our disks into a system," according to Mike Kirby, product manager for hard-disk drives at Shugart Associates.

Although he feels that the future growth potential of the market for controllers is extremely large, Kirby thinks that it is difficult for new controller manufacturers to enter it. "So far, the OEM has designed his own controller. In fact, many still prefer to build their own," he points out, "so a controller manufacturer has to make his product extremely cost-effective to sell it to the system OEM."

The winning combination, according to Microcomputer Systems' Toreson, is large-scale integration applied by someone with computer systems experience—that is, someone who knows the needs of the user as well as the technology of manufacture. "The new guys are facing a technological barrier: integrated-circuit manufacturers don't have the systems experience, and the systems guys don't have the LSI experience." Toreson claims MSC has all sides of the issue covered, proof of which is its MSC-1900, which is halfway to a controller on a chip.

Nevertheless, the majority of the

ROUNDUP: THE LATEST IN SINGLE-BOARD CONTROLLERS FOR 8- AND 14-IN. WINCHESTER DISK DRIVES							
Company and model	Price/quantity	Computers and bus interface	Number and type of drives	Maximum capacity (megabytes)	Transfer rates	Error checking and/or correction	Features
Advanced Electronics Design Inc. WINC-01	$3,930/1	LSI-11; Q-bus	1 Winchester drive	20	960-K bytes/s	24-bit error-correction code	Transparent with standard RL01 software drivers, optional backup to cartridge
Computer Products Corp. Rimfire-38	disk-and-tape: $2,295/1, $1,795/50; disk- or tape-only version: $1,895/1, $1,485/50	8- or 16-bit central processing unit; Multibus	up to 5 Priam 8- and 14-in. disks and 4 tapes	150 on disk, 46 on tape	up to 1.3 MHz with enough host system memory	cyclic redundancy checking across 16 bits	streamer tape for backup, direct memory access (DMA)
Distributed Logic Corp. DQ 202	$1,592/50	LSI-11; SMD, Q-bus	2 8-/14-in. Winchesters	160	not specified	—	runs standard DEC driver software and bootstrap loader
DU-202	$1,786/50	PDP-11; SMD, Unibus	2 8-/14-in. Winchesters	160	not specified	—	bootstrap loader
Emulex Corp. SC21	under $3,500/50	PDP-11, VAX-11/780; SMD, CMD	up to 4 drives in any mix of SMD- or CMD-type removable or fixed drive	600	not specified	32-bit ECC code that corrects single-burst errors of up to 11 bits per sector, 16-bit CRC for header	models A, B, C emulate DEC RP11E, RH11, and RK611; DMA
General Robotics Corp. SMV-11	$3,000/1	LSI-11; SMD, Q-bus	1 or 2 SMD-type drives	600 on line	not specified	—	compatible with RT-11 and RSX-11 software, DMA
Microcomputer Systems Corp. MSC-1086	$2,700/1, $2,000/large orders	most minicomputers and microcomputers; Multibus	up to 4 SA4000, 4 SA850, or 1 3M HCD (may be mixed)	200	adaptable	yes	tape cartridges for backup storage
MSC-1088	$2,650/1, $2,000/large orders	small-business systems; IEEE-488	2 SA4004, 4008, or 4100 drives	over 100	adaptable	yes	verifies disk positioning and buffer data
MSC-1101	$4,850/1	PDP-11, VAX series; Unibus	SMD-type high-capacity drive, number not yet specified	not specified	adaptable	corrects single-burst errors of up to 11 bits per sector	software integration for RT-11, RSX, IAS, RSTS/E, and VAX/VMS operating systems; DMA

MSC-1102	under $4,000/large orders	PDP-11; Unibus	up to 4 SMD-type drives	80 per drive	adaptable	32-bit ECC code that corrects single-burst errors of up to 11 bits per sector	emulates RM02, DMA
MSC 1360	under $4,000/large orders	Nova, Eclipse; SMD	up to 4 14-in. hard-disk drives	200 per drive	adaptable	32-bit ECC code that corrects single-burst errors of up to 11 bits per sector	emulates 6060 family of drives, DMA
MSC-1990	$4,500/1 $3,900/26–50	TM990 models 8 through 12; SMD	up to 3 SMD-type drives	300 per spindle	adaptable	32-bit ECC code that corrects single-burst errors of up to 11 bits per sector	full-sector buffer, two 256-word buffers, DMA
MiniComputer Technology SMV-15	$3,900/1 $2,900/25	VAX 11/780; SMD	any 2 SMD-type drives	600	up to 20 MHz	32-bit ECC	DMA
EDC-22	$4,700/1 $3,800/25	Nova, Eclipse; SMD	up to 4 SMD-type drives	600 per drive	32 sectors per read/write command	32-bit ECC code that corrects single-burst errors of up to 11 bits per sector, 32-bit CRC	emulates DG 6060 Zebra disk subsystem, DMA
EDC-24	$4,900/1 $3,800/25	LSI-11; Q-bus, SMD	up to 4 SMD-type drives	600 per drive	64 kilowords transferred with one read/write command	32-bit ECC, 16-bit CRC	emulates DEC's RK06/07 and RM02/03 disk subsystems, 3-sector RAM buffer, DMA
Point 4 Data Corp. Lotus 700	$3,390/1	Point 4 and similar 16-bit machines; SMD, CMD	any mixture of 4 drives	300 per drive	1.209 megabytes/s	32-bit ECC	IRIS-compatible
Lotus 701	$1,450/1	Point 4 and similar 16-bit machines; SMD, CMD	up to 4 10-megabyte 14-in. hard-disk drives or cartridges	10 per drive	1,500 or 2,400 rpm	data error checking	transparent to IRIS operating system
Shugart Associates SA1400	$995 to $1,420/large orders	machines using the General Purpose Interface Bus	up to 4 8- or 14-in. Winchester or floppy-disk drives, plus tape cartridge	232	adaptable	32-bit ECC	data-separator logic, 1-K-byte buffer, DMA
Western Digital Corp. WD1000	about $300/100	8-bit computers; 8-bit bidirectional bus, ST500/SA1000, S-100 bus	up to 4 ST500 (5¼-in.) or SA1000	—	5 Mb/s	CRC	DMA

SOURCE: *ELECTRONICS*

controllers reaching the market now are still the single-board variety—a factor which does confirm the tendency toward smaller and smaller controllers. With the entry of floppy disks, especially the 8-in. and smaller variety, the consumer got used to seeing smaller and smaller computer systems with larger and larger capacity. Psychologically—or as Toreson puts it, emotionally—the user has gotten used to seeing his drives housed, if not within the computer, then in a very small standalone space. Hard-disk drive manufacturers have accommodated the user by going smaller.

Size reduction, of course, reduces capacity but allows installation in tighter spots. The industry has not yet settled on a standard small hard disk; 8- and 5¼-in. versions are both available. Toreson says there is little difference between what the two have to offer: "It all depends on who starts delivering first." So, MSC, Piiceon, and Western Digital have put their efforts into versatile drives that will bridge the gap between the two sizes and let the user decide.

The influence of the floppies on the system user is obvious in the capabilities offered by many of the new single-board controller makers—controllers that handle both 8- and 14-in. hard and floppy disks (see chart) as well as tapes. This may ease the transition to the smaller hard disks and may also aid in returning the floppies to their original and natural function—input/output.

This also points to one issue that remains in question: backup storage. There does not seem to be a consensus as to which way the industry will go—to floppies, tape cartridges, or streaming tapes.

"All the scrambling by controller manufacturers is preliminary to what is really going to sell in terms of backup," says Dilog's Krosner. "A streamer tape is limited in that it can't back up to selected files; you can't read what's on the tape," he says. Nevertheless Dilog offers control of the Cipher streamer as backup on a separate circuit board. "We'll wait a year or so til the dust

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settles and then go to a single-board controller with whatever backup looks promising."

Shugart Associate's Kirby feels that for backup the most useful are the floppy and the ¼-in. tape cartridge—two capabilities offered by the SA1400. "The main issue is I/O and what the floppy has to offer is that it can be removed and easily mailed," he argues.

"The business of backing up a Winchester drive is ludicrous," says MSC's Toreson. "That's merely the use of brute force, since most of the information that gets transferred in backing up has not really changed." He maintains that if the Winchester drives get cheap enough, a user can own two drives—one to have in operation, and one on standby. Then it would be a matter of switching back and forth, accessing the memory directly to make limited changes, and keeping unchanged data in the standby drive. "This is no dumber than disk-to-disk or disk-to-tape copying of entire files," he concludes. "Besides, the second drive gets free use of the same controller."

To provide system versatility, most of the controllers handle a mix of drives, or at least multiple drives. Transfer rates are usually adaptable to the drive's rates in such cases, but the manufacturers do not offer standardized specifications for these rates—a practice that would ease comparison.

In the present crop of controllers, all offer some form of error checking and/or correction, a feature that has been facilitated by the availability of chips that perform the function. The controllers also cover most standard interfaces with large and small computers, and some even offer emulation. In fact, MiniComputer Technology, which had not made emulating controllers before, found itself responding to requests from their clients to offer emulation.

Advanced Electronics Design Inc., 440 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 733-3555 [401]

Computer Products Corp., 2415 Annapolis Lane, Plymouth, Minn. 55441 [402]

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, Calif. 92643. Phone (714) 534-8950 [403]

Emulex Corp., 2001 East Deere Ave., Santa Ana, Calif. 92705 [404]

General Robotics Corp., 57 N. Main St., Hartford, Wisc. 53027. [405]

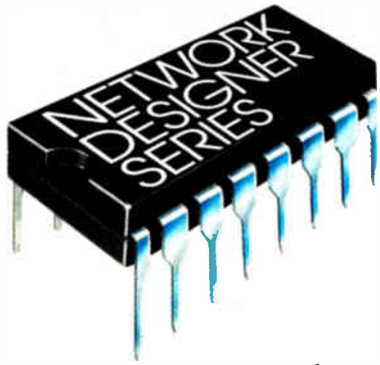
Microcomputer Systems Corp., 432 Lakeside Dr., Sunnyvale, Calif. 94086. Phone (408) 733-4200 [406]

MiniComputer Technology, 2470 Embarcadero Way, Palo Alto, Calif. 94303. Phone (415) 856-7400 [407]

Point 4 Data Corp., 2659 McCabe Way, Irvine, Calif. 92714 [408]

Shugart Associates, 415 Oakmead Pkwy., Sunnyvale, Calif. 94086 [409]

Western Digital Corp., 3128 Red Hill Ave., Box 2180, Newport Beach, Calif. 92663. Phone (714) 557-3550 [410]



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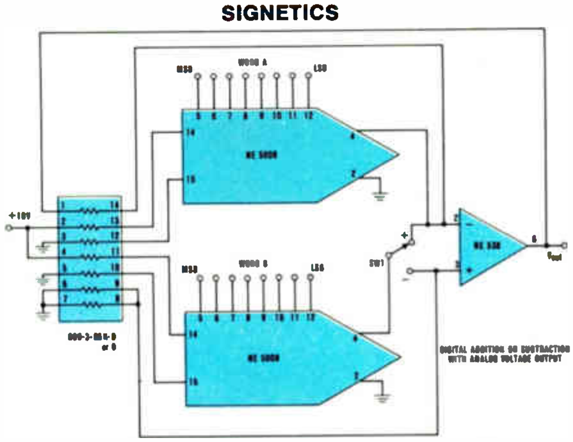
The Beckman vacuum deposition process creates consistent resistor values with typical tempco performance of 25 ppm/°C; 50 ppm maximum. More importantly, tracking tempco is only 5 ppm.

With absolute tolerances from 1% down to 0.1% and ratio matching from 0.5% to 0.05%, standard thin film networks from Beckman can boost linear circuit performance — especially when similar values or matched resistor sets are required.

As demonstrated in the digital addition or subtraction circuit below (Fig. 1), several common value resistors are supplied by a single thin film network.

SIGNETICS



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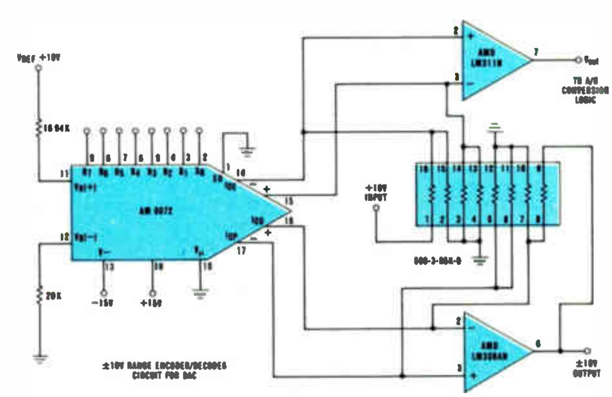
In this example, the common reference voltage drops across two inherently ratio matched network resistors, providing precise and equal reference currents to the DACs. Since the feedback resistor is part of the network, it too is ratio matched with the input resistors and tracks their movement with temperature change. The result is output stability because the input currents to the op amp track the DAC reference currents, thus the output voltage tracks the reference voltage.

Inherent Ratio Matching

The following encoder/decoder circuit application (Fig. 2), used in pulse code modulation transmission systems, again demonstrates the advantages of inherent network resistor ratio matching.

AMD



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By utilizing a series of 5K resistors with 0.5% tolerances (matched to within 0.1%) the thin film network provides stable inputs to the comparator in the encoding mode or to the op amp in the decoding mode.

The feedback resistor of the op amp tracks the input resistors to within 5 ppm, resulting in an extremely accurate gain on the output.

Additionally, a 2.5K resistor is required to tie the non-inverting input of the op amp to ground. This resistor is created by paralleling two of the 5K resistors in the network. The new value will also track the other resistors to within 5 ppm.

The precision summing amplifier circuit (Fig. 3) is an excellent example of how requirements for a matched set of resistors can be supported with a standard thin film network.

resistor networks boost performance over discretes

FAIRCHILD

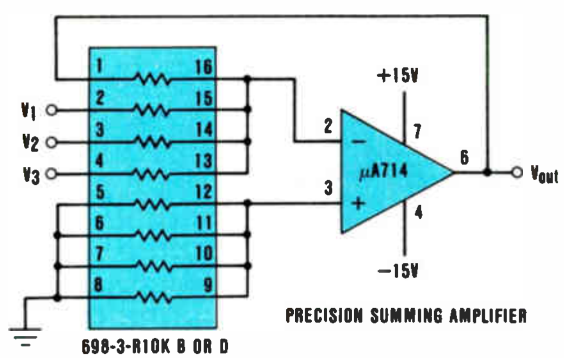

Fig. 3 Copyright © 1980 Fairchild Camera and Instrument Corp. Reprinted with permission of copyright owner.

In this application, the accuracy of the input resistors determines the common mode noise rejection. Matching the feedback resistor to the input resistors sets the accuracy of each input to the summing point. Close ratio matching is therefore essential.

The non-inverting input resistor is used in this application to cancel the effects of the bias current, and should be equal to the parallel combination of feedback and input resistors. This can be easily accomplished using the network — especially where equal weighting of the inputs is desired.

Since the amplifier error can be as low as .0015%, most of the error results from the resistors. This error can be minimized by using a standard thin film network with a ±0.1% tolerance and ratio match.

Accurate Voltage Ratios

The capability to create accurate voltage ratios which track throughout the temperature change can also be used to improve circuit performance. In the bipolar out circuit below (Fig. 4), Beckman's new thin film mini-DIP is employed to achieve a 2:1 voltage ratio between the output of the first op amp and the input from the voltage reference.

This ratio will remain stable throughout temperature change and permits a simple — yet accurate — circuit for bipolar output.

The use of the Beckman thin film mini-DIP allows the designer to gain the performance improvement of a network even in applications that require only a limited number of matched resistors.

These four applications have graphically demonstrated how Beckman standard thin film networks can improve your circuit design in the critical areas of performance, cost and versatility.

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For more information on any of these thin film applications, or to request our new Thin Film Resistor Network Catalog, contact your nearest Beckman distributor or write: Network Products Operations, Beckman Instruments, Inc., 2500 Harbor Blvd., Fullerton, CA 92634. (714) 773-8525.

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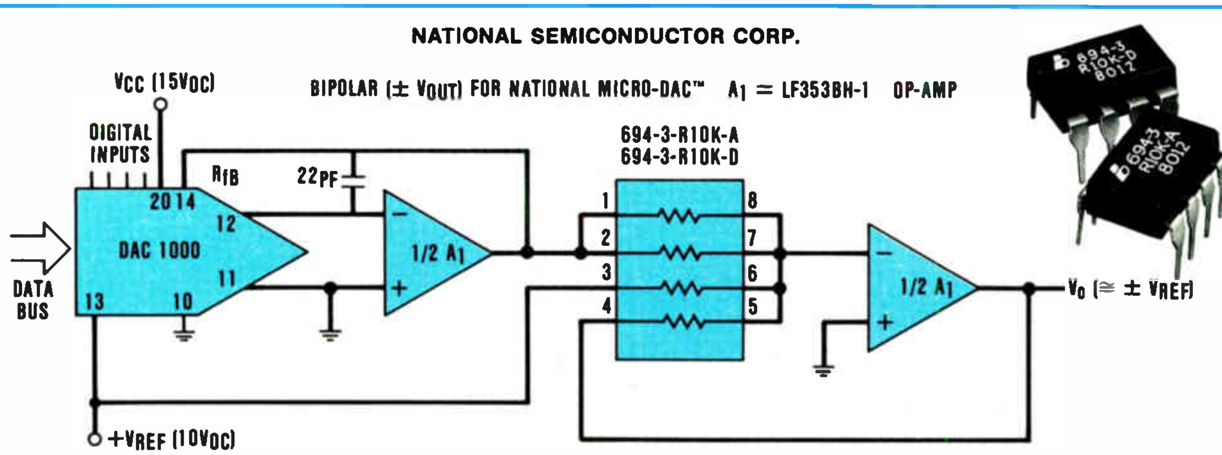

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GENERAL ELECTRIC

Circle 248 on reader service card

Board tester combines techniques

Teradyne line does in-circuit and full-board functional tests on high-density analog and digital circuit boards

by Linda Lowe, Boston bureau

Denser, more complex printed-circuit boards will increasingly tax the capabilities of board testers as large- and very large-scale integration take over in the coming decade. But Teradyne says it is ready with the first members of its new L200 series, a family of board-test systems that combine in-circuit with full-board functional testing capabilities. The testers' distributed architecture and fast modular hardware and software will pace escalating performance and throughput demands in the 1980s.

To bow at next month's Cherry Hill test conference in Philadelphia are the L230 and L260 systems, representing the low end and middle range, respectively, of the line. Teradyne will be showing off a demonstration model of the L260, which it schedules for first shipments in March 1981 and will sell for from $350,000 to $500,000. The Boston firm says it will demonstrate the L230, priced between $250,000 and $600,000, next February and begin shipping it in June.

The L260 performs analog or digital, in-circuit or functional testing in any combination using common hardware, fixturing, and programming language. Its effective test rate of 100 kHz (the time taken to load test data, run the test, and make a pass/fail decision is less than 10 μs) is 10 to 100 times faster than current testers, according to Teradyne. Its maximum clock rate for functional testing is 10 MHz. The L260's test-point capacity, expandable to 1,152 pins for functional and 2,304 pins for in-circuit testing, outstrips today's test systems. Its automatic diagnostics pinpoint multiple faults on very complex pc boards.

The L260 is built around a Digital Equipment Corp. PDP-11/44 supervisory computer, which communicates via DEC's Unibus to peripherals and to two dedicated processors controlling digital test electronics and analog instrumentation. Four different types of channel cards—one analog and three digital—are being offered initially. Users can mix them to configure the L260 for any combination of analog and digital, in-circuit and functional testing. A highly interactive Pascal-based language allows construction of modular routines that programmers can combine into test programs.

The combination of in-circuit and full-board functional testing in one test system responds to a major problem presented by increasingly complex boards, says Jeffrey R. Hotchkiss, product manager. In-circuit testing alone, which caught 98% of board problems in the era of 1,000-circuit boards, may only provide 75% to 80% now that boards are successfully packing in 10 times the circuitry, he notes. "That kind of potential failure rate demands that testers today evaluate overall board performance in a systems environment as well as checking its individual components."

Fast exercise. Programmable load pins and dual-threshold detectors permit the L260 to exercise boards at their full rated speeds, just as a final system would do. Each channel-card pin is backed up by random-access-memory chips—the number varies. The L260 performs functional tests at clock rates of up to 10 MHz; the eventual high end of the L200 family will clock as fast as 30 MHz, says Hotchkiss. In-circuit testing runs at up to 2 MHz, which allows over-drive of dynamic parts with minimum keep-alive rates. The power dissipation of overdriven parts

is controlled by keeping the duration of test bursting short.

Digital testing, whether in-circuit or functional, takes place under the direction of a digital command processor (DCP). Built with 2900-type bipolar bit-slice parts and using a direct memory access scheme, the DCP transmits test patterns directly from the PDP-11/44 to channel-card pins at a rate of 500 kHz. It directs digital drives that apply test stimuli to the board and runs tests in hardware while comparing board response with memory to make pass/fail decisions in real time. An algorithmic pattern processor for testing on-board memories at clock rates up to 10 MHz is optional; operating with standard memory-testing algorithms such as Galpac, March, and Walk, it accepts user microprogramming for more extensive custom testing.

For analog testing, an analog instrumentation processor (AIP) supervises up to 10 programmable power supplies and up to 20 forcing and measuring instruments for functional tests. The AIP switches instrumentation to each analog channel card's 24 pins over three Kelvin lines, through a full-crosspoint reed-relay matrix; software can reconfigure the matrix to six non-Kelvin lines if required. The AIP also directs an in-circuit instrumentation group that performs guarded measurements of most active and passive devices. An optional IEEE-488 bus connects to additional instruments.

The L260 test-station fixturing scheme is based on a frame that accommodates almost any kind of fixture for both in-circuit and functional testing. Vacuum beds of nails, edge-connector frames, and user-built custom fixtures all can be used. The frame interfaces directly to test electronics via zero-insertion-force connectors on the digital channel cards. Teradyne's design dramatically cuts lead lengths between channel-card outputs and a board's critical nodes to about 3 or 4 in. typically, eliminating reactance problems associated with the 18- to 24-in. leads generally found in current testers.

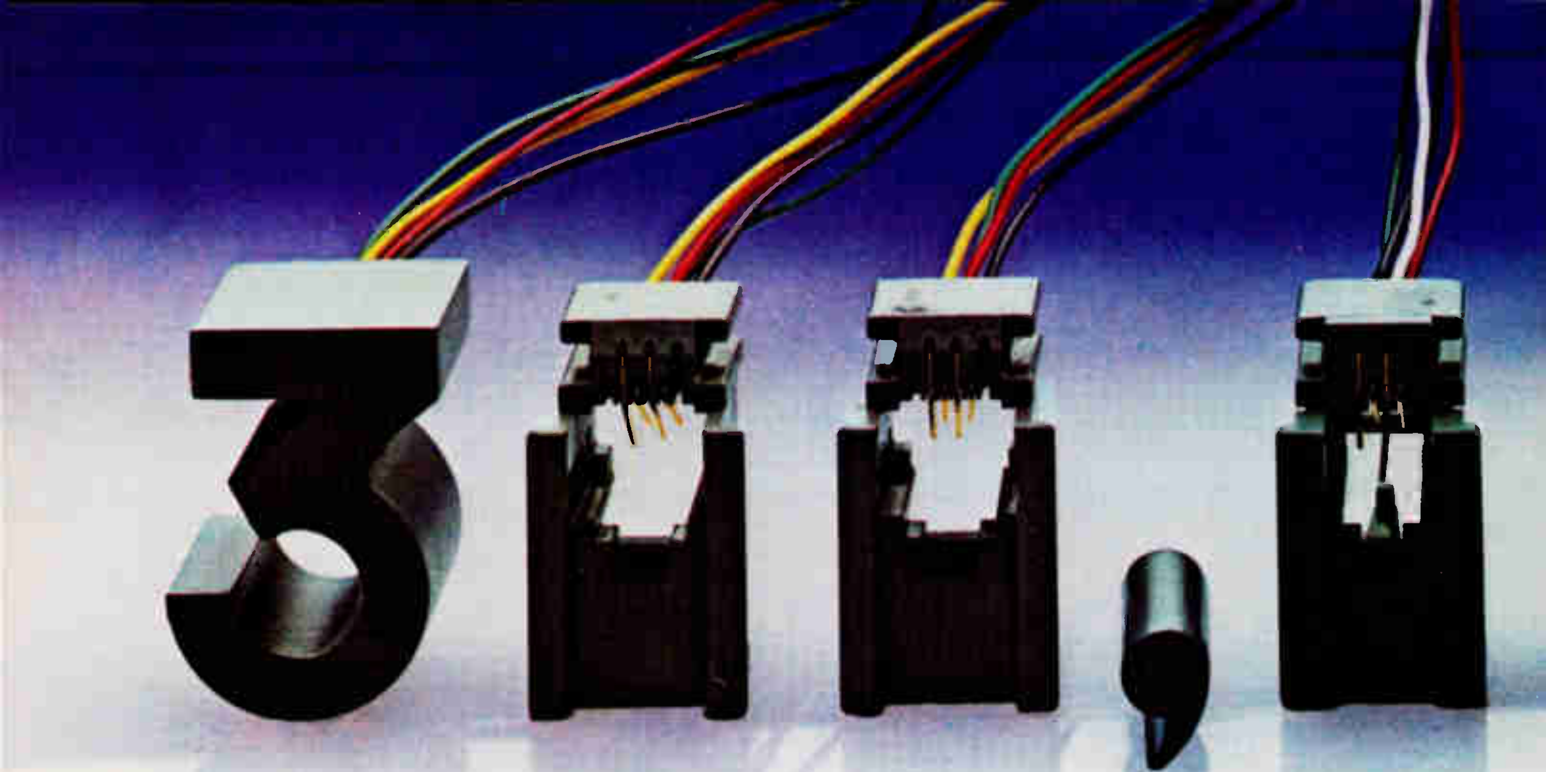
Two diagnostic software packages trace test failures to their source. Inciter, the In-Circuit Test Evaluator package, analyses even multiple in-circuit failures and diagnoses shorts, opens, and component failures. It delivers detailed diagnostic messages on a cathode-ray-tube screen or high-speed line printer as faults occur, or it summarizes faults statistically. The State-Sensitive Trace package directs automatic system probes of functional-test failures if a vacuum bed-of-nails fixture is in use or it directs an operator to probe suspect nodes and devices with hand-held probes.

Timesharing. The L260's software compiles programmed instructions automatically and allows timesharing of program generation, editing, and testing operations. An In-Circuit Composer automatically generates in-circuit test plans from a physical description of a good board and draws test data from a stored library to determine the measurement approach for each component.

Programmers compose digital and analog functional test programs using an interactive test editor that enters and automatically compiles instructions and notifies the programmer of violations as they occur. Teradyne's Lasar software is an optional package that further eases the writing of very long, very complex digital functional test sequences and can generate programs for the L260 on an off-line computer such as DEC's VAX 11/780. An Immediate-Response Debug package incrementally compiles and reloads program changes, readying them for execution typically in about 5 seconds. The package also gives programmers the power to alter program flow interactively, interrogate or modify system hardware, execute L260 language commands, and display the source program on a CRT.

The L260 comes with up to 1 megabyte of PDP-11/44 main memory, and users can add up to two 10-megabyte cartridge disk drives for primary storage and two 512-K-byte floppy-disk drives for backup storage.

Teradyne Inc., 182 Essex St., Boston, Mass. 02111. Phone (617) 482-2700 [339]



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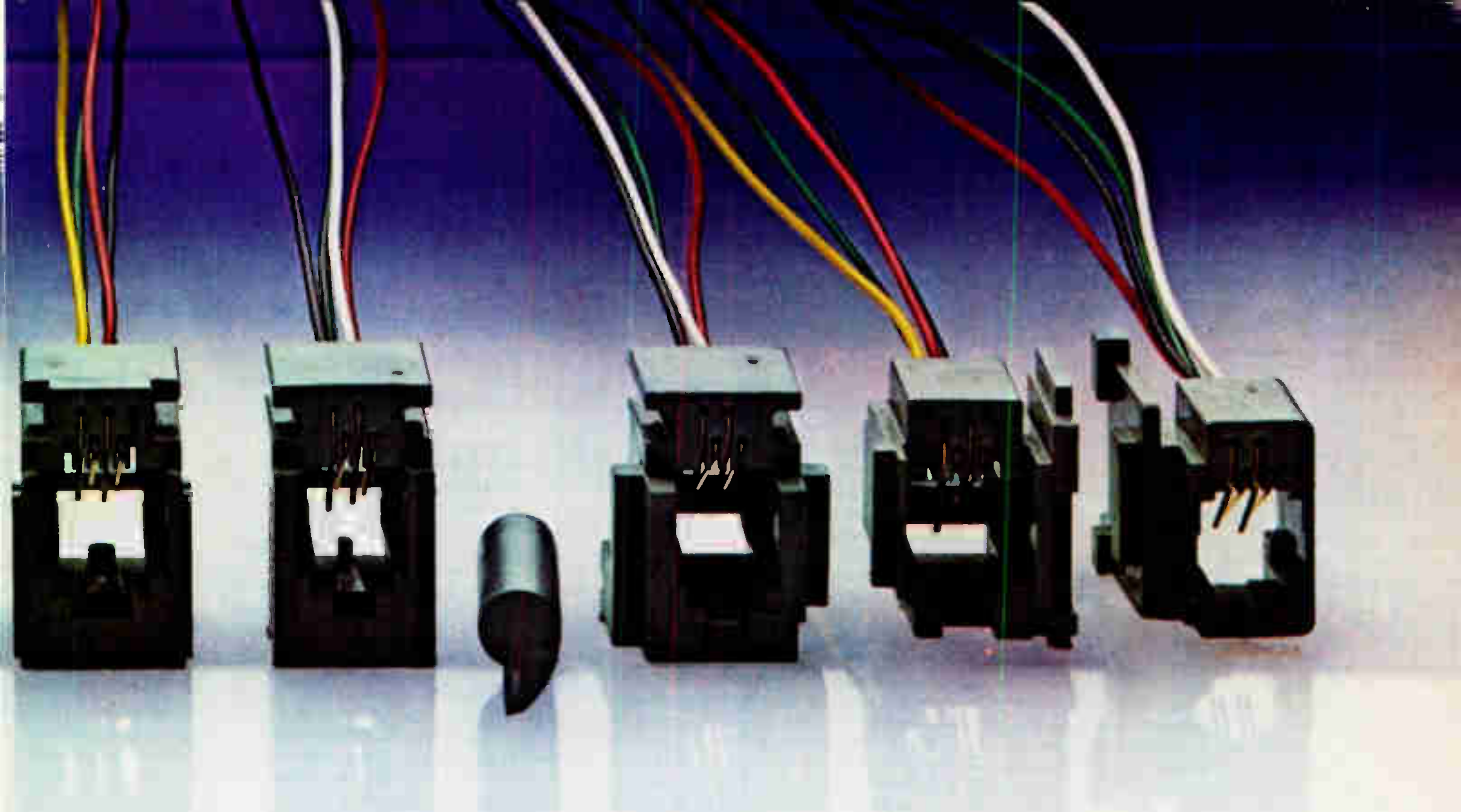

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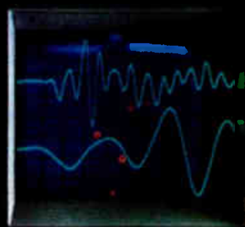

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Circle 255 on reader service card

Computer board stores ½ megabyte

The arrival of 64-K dynamic random-access memories puts HP's L-series processor in minicomputer arena

by Martin Marshall, West Coast Computers & Instruments Editor

The humble designation "option 012" marks a quantum leap for Hewlett-Packard Co.'s 1000 L computer series: the availability of 64-K dynamic random-access memories has allowed the company to offer a board that carries half a megabyte. Modifying the operating system of the complementary-MOS-on-sapphire microprocessor so that it can map memory on 64-K-byte boundaries, HP has a stout 16-bit machine on two boards for a price of $15,450 (the 2103L, with 10-slot rack and power supply). The company will not identify the two makers of 64-K RAMs it has qualified, but outside sources named Hitachi and an unknown U. S. semiconductor house.

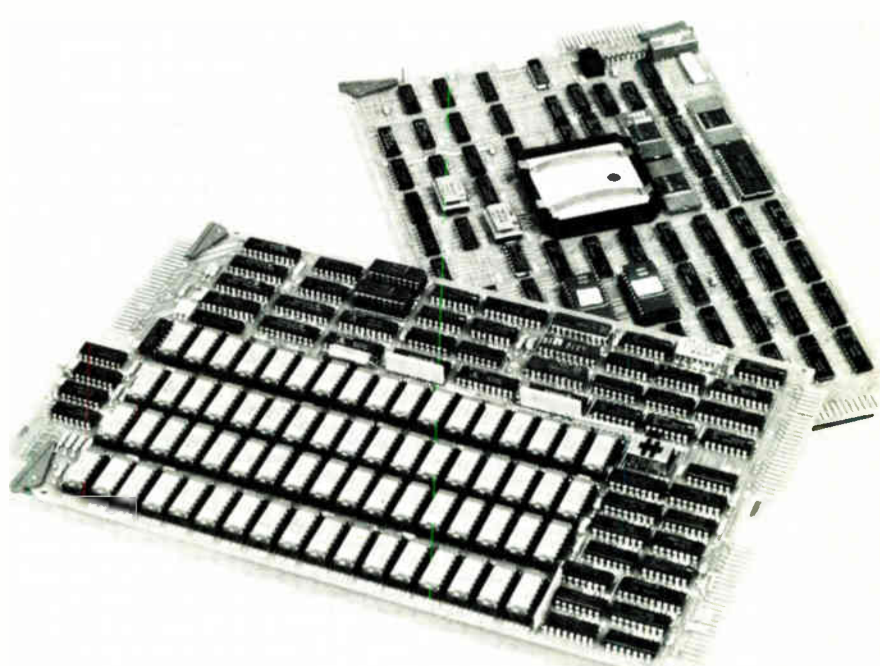
When the L series was announced in March [*Electronics*, March 27, 1980, p. 48], HP did not reveal the extent of its memory and software plans for the series. The prime components that would carry the upgrades, however, were in place. The proprietary 16-bit silicon-on-sapphire microprocessor, called the L-series processor, emulates the architecture of the bit-slice HP 1000 M series and is the backbone of the L series. Also integrated into this chip are the time-base generator, boot loaders, and self-test and memory-protection features.

Another 16-bit SOS microprocessor is used in a coprocessing role on each separate board that performs input/output functions. This coprocessor gives the L series its most outstanding characteristic—a 2.7-megabyte/s data-transfer rate, the highest for any computer in the under-$50,000 class. This I/O processor provides one channel of direct memory access per board. Versions of the I/O card can provide an IEEE-488 interface ($850), a standard serial interface ($600), and a general-purpose parallel interface ($600).

Company. HP is not the only firm to put its minicomputers onto a chip set. Digital Equipment Corp. has had great success with its LSI-11 board line, which uses a PDP-11 reduced to a chip and is at work putting its VAX-11/780 onto a chip set [*Electronics*, Oct. 9, p. 33]. With its L-series boards and their expanded memory capacity, HP is hoping to solidify the bottom end of its line just as DEC has done.

According to HP, the 512-K-byte memory represents the full implementation of the processor's direct addressing capability. Versions that contain 128- and 256-K bytes will also be made available, but these use 16-K RAMs.

The price of the 512-K-byte, two-board 2103LK option 012 is $13,250 in single units and $8,215 to original-equipment manufacturers in quantity, compared with $2,250 for a single unit of the 64-K-byte version. The additional $11,000 for the big memory ripples through the larger systems built around the two-board set. At the system level, the model 10 includes a 2103LK computer, a 16-slot card cage, a cathode-ray-tube terminal, a cabinet, a 1.2-

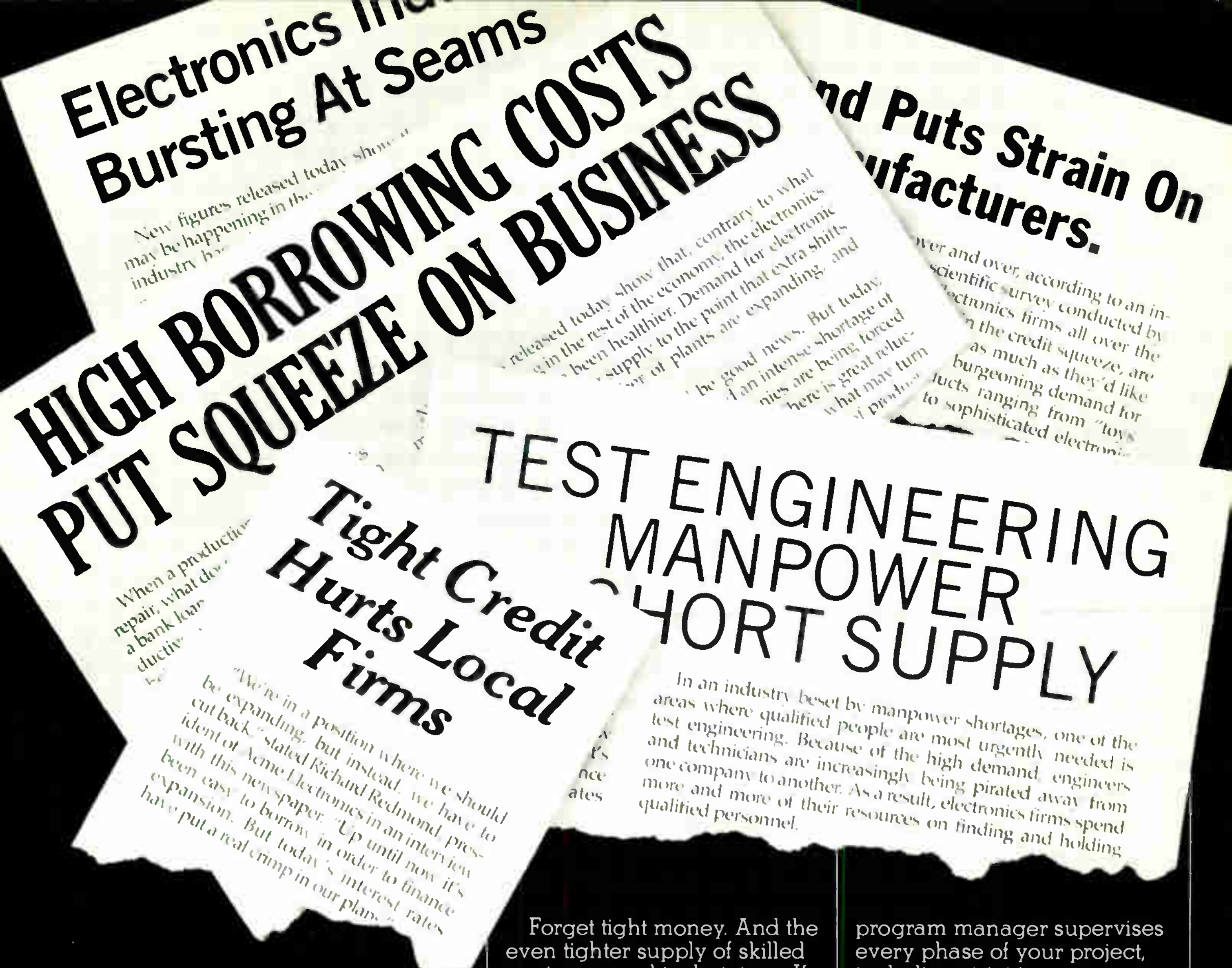


megabyte floppy-disk drive, and a 14-in. 12-megabyte Winchester disk drive; it will be priced at $32,500.

HP also revealed that the L series will be able to use the software for image data-base management, as well as the DS/1000 networking package developed for the larger HP 1000 computers. For the versions with 128-K bytes or more of RAM, HP's Query language is also available. The L series' instruction set and operating system is a subset of those used on the larger HP 1000 systems. The 512-K-byte version contains both the RTE-L real-time multitasking operating system and RTE-XL, which performs the mapping across the 64-K-byte boundaries. The L series differs from the M, F, and E series in that the larger systems run RTE-IV, which has a batch spool monitor and a session monitor as well as the ability to address 2 megabytes. The instructions on the larger machines pertaining to these features do not translate into instructions in the L series, except through emulating subroutines.

Options. The networking applications of the L series are greatly enhanced by a single I/O card ($1,800–$2,400) that contains the HP I/O processor and a Z80-based I/O subsystem. The subsystem addresses its own 8-K bytes of read-only memory and 16-K bytes of RAM and has its own serial I/O, timer, and control circuitry. It can even allow direct-memory-access transfers within DMA transfers. A similar Z80-based card can multiplex eight terminals while operating at rates up to 19.2 kb/s per terminal. It has store-and-forward capability and communicates using High-level Data-Link Control protocols. Other new I/O cards include a digital one for measurement and control applications ($1,500) and an analog input card that combines 12-bit 55-kHz eight-channel analog-to-digital conversion ($1,500) with an additional 32-channel analog multiplexer ($600). Deliveries of the new L series of computers and I/O cards are from stock to eight weeks.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304 [340]



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Circle 259 on reader service card

Components

Chip looks for 64-bit word

Correlator checks serial stream at 20 MHz for agreement with stored word

The TDC1023J is the first single-chip digital correlator. Capable of comparing a previously stored 64-bit reference word with an incoming 64-bit serial word at a 20-MHz rate, the 24-pin unit replaces several small- and medium-scale integrated packages in digital signal-processing applications, including communications, instrumentation, telemetry, radar, and medical electronics.

The device uses correlation to recognize specific signal patterns in digital form. (Correlation is a mathematical technique that allows a bit pattern of interest to be detected amidst noise.) In addition, the chip can be used to measure time delays through various media, human tissue, radio-frequency paths, and electronic circuits in general.

The device is based upon four 64-bit, independently clocked 40-MHz shift registers. Incoming data is clocked into the A register. The reference word is entered into the B register, then copied into the R register, allowing the user to load a new reference word serially while correlation occurs between the A and R registers. These registers are continually compared, bit for bit, by exclusive-OR gates whose outputs go to a digital summer via AND gates. The 7-bit output of the summer is the binary-weighted sum of those bit positions of the A and R registers that are in agreement.

The mask register, M, allows the user to adjust the word size. Since each bit in this register feeds an AND gate, any zero will prevent the corresponding exclusive-OR output from reaching the summer.

Inverted outputs can be obtained from the correlator through a control line that feeds seven other exclusive-OR outputs attached to the output of the summer. These gates in turn feed a three-state buffer, allowing the correlator to be used in bus-oriented systems.

A correlation threshold can be set through an independently clocked 7-bit register. After placing the outputs in their high-impedance state, this register is loaded via the data bus. When the sum equals or exceeds this value, the flag is set.

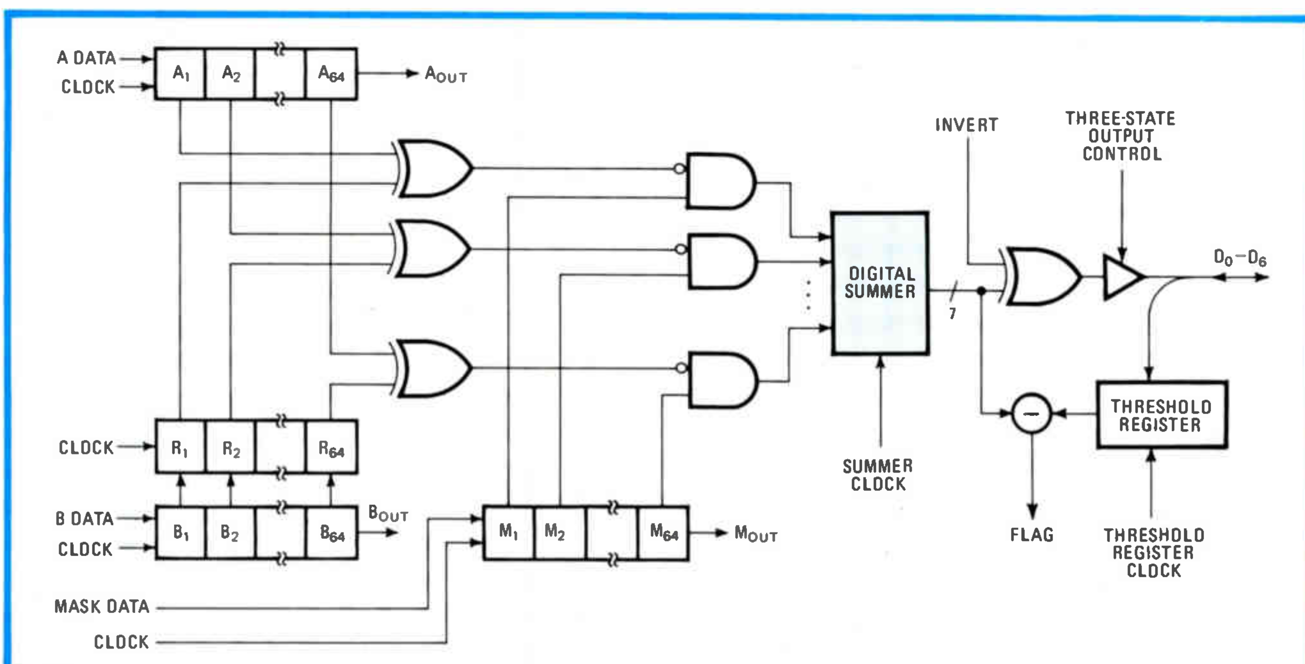
The correlation codes may be expanded in multiples of 64 bits by connecting the A_{out}, B_{out}, and M_{out} lines to the A_{in}, B_{in}, and M_{in} lines of a succeeding chip. With this multiple-chip arrangement, an external binary adder must be used to obtain the final sum. Also, an external threshold register must be used if that function is desired. The maximum number of correlators that can be used in a cascade is limited by the loading and speed of the external circuits.

The TDC1023J operates from a single 5-V supply, and all inputs and outputs are TTL-compatible. The price is $85 in 100-piece lots, with availability set for December.

TRW LSI Products, P. O. Box 1125, Redondo Beach, Calif. 90278 [341]

$2.72 C-MOS op amp has 1-μV input offset voltage

With a $2.75 price tag, the ICL7650 complementary-MOS operational amplifier has input offset voltage of



Correlator. Data clocked into A register is compared with 64-bit reference word in R register; output of summer is number of agreeing bits.

1 μV. It does not require a trimming potentiometer. Operating over −20° to 85°C, the op amp achieves a thermal drift of 0.01 μV/°C. Long-term offset drift is 1.0 μV/year. Dc input bias current of the device is 10 pA; the gain, common mode rejection ratio, and power supply rejection ratio are all in excess of 120 dB. The slew rate is 2.5 V/μs and the gain-bandwidth product is 2 MHz. Phase error between the applied signal and the chopping frequency is less than 10°.

All clock-oscillator and control circuitry is contained on the chip, which comes in a TO-99 package and is priced at $3.05 for 100 units or more. In the same quantities, a 14-pin dual in-line package version is available for $2.75. Included on the circuit is a clamping option in the feedback network to reduce gain just before maximum output is reached, plus an optional connection for an external clock. The ICL7650 is available from stock in industrial and military temperature ranges.

Intersil Inc., 10710 North Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [343]

Thyristors reach high voltage, current ratings

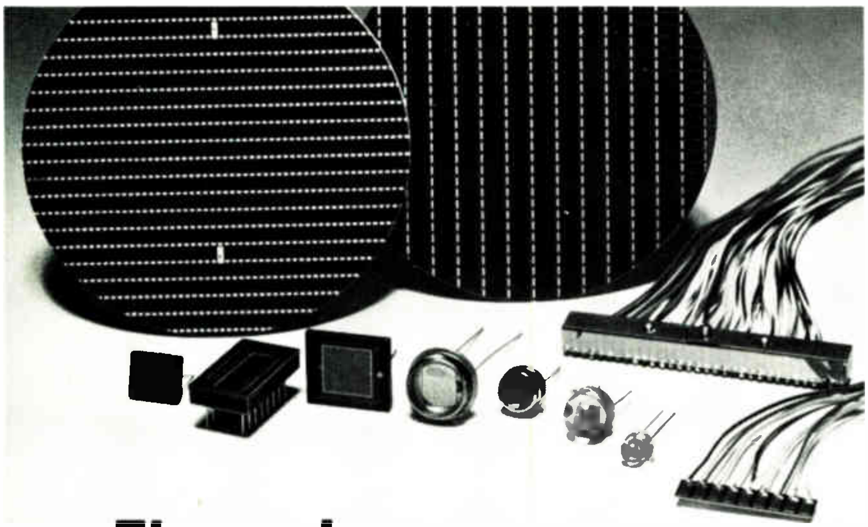
Designed for high di/dt (rate of rise of peak current) capability, the T72H thyristor has a rating of 100 to 1,200 V, 400 A average and a turn-off time of 10 μs. It can be used in chopper controls, inverters, and crowbars. It has a minimum and repetitive di/dt of 500 A/μs and a nonrepetitive rating of 1,200 A/μs. In quantities of 100, the 10-μs, 1,200-V devices are $216 apiece. Delivery is four weeks.

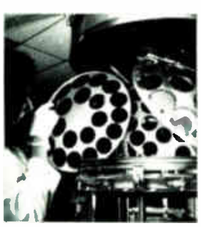
Another thyristor, the phase-control TA20, can handle currents of 1,200, 1,600, and 1,800 A and voltages ranging from 600 to 3,000 V. These high ratings minimize the need to combine several devices in parallel or series. The TA20's minimum rate of rise of peak voltage is 300 V/μs. Typical turn-off times are 250 and 400 μs. Gate current is 200 A with soft gate control; thermal impedance is 0.015°C/W, junction to case; and forward voltage drop is 1.65 V at 6,000 A for the 1,800-A device. In 100 quantities, the 1,200-A, 3,000-V devices sell for $552 apiece. Delivery is in six to eight weeks.

Westinghouse Electric Corp., Youngwood, Pa. 15697 [344]

Tuning diode has ± 1½% capacitance tolerance to 25 V

The model KV3111 precision hyperabrupt tuning diode has a ±1½%





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Intel® Military RAMs (Class B, MIL-STD-883B)

Model	Organization	Maximum Access (ns)	Current Active/Standby (mA)
Static[1]			
M2115A	1Kx1	55	125
M2115AL	1Kx1	75	75
M2125A	1Kx1	55	125
M2125AL	1Kx1	75	75
M2114AL-3	1Kx4	150	50
M2114AL-4	1Kx4	200	50
M2114A-4	1Kx4	200	70
M2114A-5	1Kx4	250	70
M2148H	1Kx4	70	180/30
M2147H-3	4Kx1	55	180/30
M2147H	4Kx1	70	180/30
Dynamic[2]			
M2118-4	16Kx1	120	25/2
M2118-7	16Kx1	150	23/2

[1]TA: −55° to 125°C
[2]TA: −55° to 85°C

For systems ranging from shipboard and ground communication systems to avionics and missile controls, these RAMs offer a way to forge ahead with cost-effective designs. And, because they're available now in volume, you can press them into service immediately.

The RAM brigade, HMOS company

Intel revolutionized RAM design when we introduced our proprietary HMOS* technology. With HMOS, power consumption and corresponding cooling requirements are drastically reduced — both critical factors in military applications. In the denser static RAMs (M2147H and M2148H), automatic power down on deselection further reduces system power dissipation — a very important power and reliability advantage in larger systems.

Furthermore, with RAMs like the M2115A, M2125A, and M2147H, you can achieve fast access times for cache memories and for systems that process data in real time.

For microprocessor applications also, you need all the performance you can muster. For those, Intel offers the low-power MOS microprocessor-compatible M2114A. Or the high-speed M2148H, suitable for fast random logic and

bipolar microprocessor designs. And for very high density applications, you can call out the M2118. It provides 16K of dynamic storage in a 16-pin package. Plus it uses only a single +5-volt supply, which reduces space requirements and increases system reliability.

The vanguard in military microelectronics

Intel's advancing line of RAMs reflects our strong commitment to military customers: to continue to deliver the broadest line of LSI devices to military systems designers. From devices like the M8080A, the first microprocessor to receive JAN approval (QPL-listed as M38510/42001), through the M8085A, the world's highest performance 8-bit microprocessor, to the first military computer-on-a-chip: the M8048. And continuing on with other MIL-STD-883B products, such as EPROMs, bipolar PROMs, and microprocessor peripherals. We've shipped hundreds of thousands of these high-performance parts to vital military programs over the past four years. Proof of our commitment to remain the leader in military microelectronics.

Our military aid program

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Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A.Varah, Wyle Distribution Group, Zentronics.

Circle 263 on reader service card

tolerance capacitance curve over the full 1-to-25-V tuning range. It allows diodes to be interchanged in tracked circuits, eliminating the problems associated with matched sets. The diode has been designed for communications and radio-frequency test equipment. Typical capacitances are 15.9 pF at 1 V and 2.125 pF at 25 V; a typical Q value is 415 at 3 V and 50 MHz. Delivery is from stock with a 100-unit price of $1.90 each.

KSW Electronics Corp., South Bedford St., Burlington, Mass. 01801. Phone (617) 273-1730 [348]

62-W op amp has 1-MHz gain-bandwidth product

The PA07 high-performance power operational amplifier has a supply voltage of ±50 V, power dissipation of 62 W, and a 1-MHz gain-bandwidth product. These specifications, says the manufacturer, constitute improvements over Burr-Brown's 3572AM, with which the PA07 has been designed to compete. The unit is basically pin-compatible with the Burr-Brown device, but the current-limiting resistors connect from the CL pins to the output rather than from the CL pins to the supply rails. This change has been made to improve stability. A new input-stage design uses a high-voltage field-effect transistor as a bias current source for the cascade stage.

The unit has a capacitive load at unity gain of 10 nF maximum. Common-mode rejection is typically 100 to 120 dB, and initial bias current is a maximum of 50 pA for the model PA07 and 10 pA for the model PA07A. The PA07A has a maximum offset voltage of ±1 mV and sells for $85.50 in single quantities and $53 each for 300 to 999. The PA07 with ±2 mV offset voltage sells for $72.50 in single quantities and for $44 each for 300 to 999. Delivery will be from stock for small volumes and four weeks for production orders.

Apex Microtechnology Corp., 1130 E. Pennsylvania St., Tucson, Ariz. 85714 Phone (602) 746-0849 [349]

You're looking at the first IC handler to solve the reliability problems of cold-handling. The model 2608C from MCT. The cold handler that operates reliably, even at testing temperatures down to −55°C.

The key to the reliability of the 2608C is its simple "dedicated" design. In competitive hot/cold handlers, mechanism failures, freeze ups, jamming and poor temperature control have been commonplace. Recognizing this problem, MCT chose to build handlers "dedicated" to a single temperature mode. First the 2608E for elevated temperature handling. And now the 2608C cold handler...built with parts made specifically to withstand cold temperatures.

But "dedicated" design isn't the whole story. The 2608C also features 5,000 DPH speed, an economical liquid nitrogen cooling system and heated input and transition gates that prevent frost.

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MCT

Micro Component Technology, Inc.

P.O. Box 43013, St. Paul, MN 55164, (612) 482-5170

Circle 265 on reader service card

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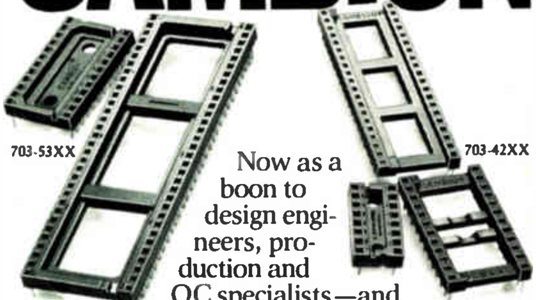

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8	.300	.396	703-5308-01-04-12	703-4208-01-04-10
14	.300	.696	703-5314-01-04-12	703-4214-01-04-10
16	.300	.796	703-5316-01-04-12	703-4216-01-04-10
18	.300	.896	703-5318-01-04-12	703-4218-01-04-10
20	.300	.996	—	703-4220-01-04-10
22	.400	1.096	703-5322-01-04-12	703-4222-01-04-10
24	.600	1.196	703-5324-01-04-12	703-4224-01-04-10
28	.600	1.396	703-5328-01-04-12	703-4228-01-04-10
40	.600	1.996	703-5340-01-04-12	703-4240-01-04-10
64	.900	3.196	703-5364-01-04-12	—

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[1]*Mounting Data:* Drill no. 67, mtg. hole dia is .032"

[2]For gold finish, specify -03 instead of -04

*Open ended for air circulation and easy access for removal of DIP.

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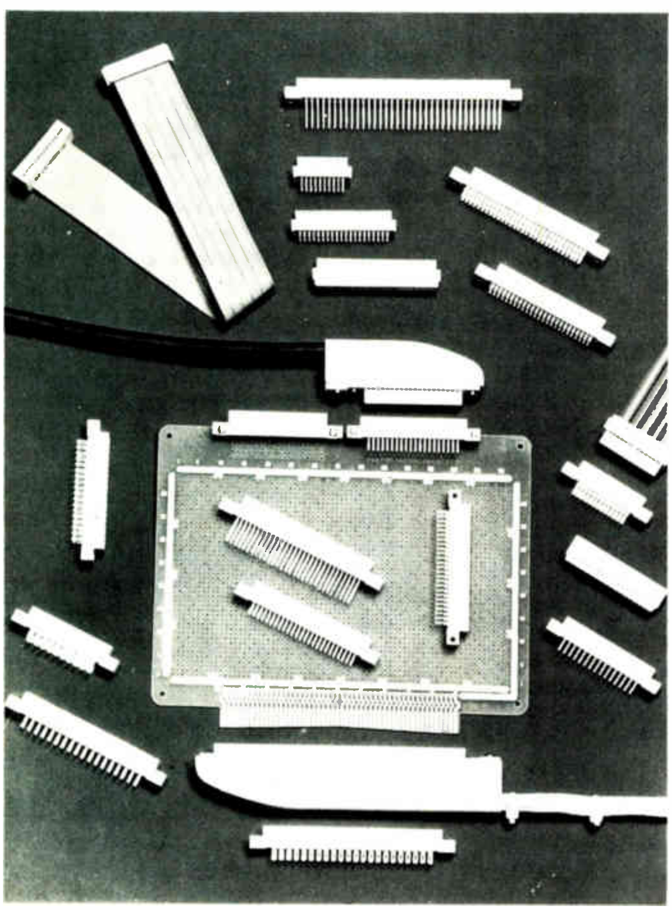

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Instruments

Logic tester handles memory

Functional board tester gets facility for testing memory embedded in complex logic

Data storage embedded in complex logic on a circuit board has left test engineers with little choice but to test the memory and logic separately, using a dedicated memory tester and a logic-board tester. But reliability suffers, for the board is not tested in an environment like the one it operates in.

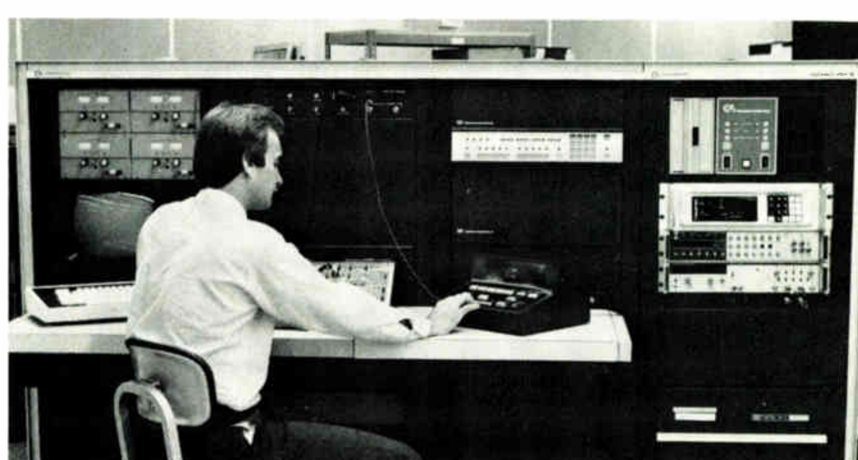
Computer Automation has married memory and logic test capabilities in the Capable 4900M. It has the features of a stored-program logic tester and a programmable hardware interface that generates memory test patterns. The system combines the real-time testing capability of the company's earlier 4900 with memory pattern generation (MPG), a hardware and software package that generates test patterns algorithmically for random-access memory arrays not not directly accessible via a card-edge connector. Memory tests can be run concurrently with logic tests.

"This means we can functionally test on a single system, without pulling off any memory, any logic board produced by the industry, including those with embedded memory," states Richard A. Garlic, director of engineering at the firm's Industrial Products division in Irvine, Calif.

According to Garlic, the combined functions provide a complete range of conditions for testing every cell of embedded memories, along with all logical functions, on a complex board at speeds equal to the board's system environment. Static tests are executed at from 1 to 10 kHz for boards with small- to medium-scale integration.

High-speed tests for boards using large- and very large-scale integration or with dynamic components requiring execution rates of up to 2 MHz are performed with timing relationships precisely like those of the system environment of the unit under test. Static and high-speed tests can be intermixed within a single test program.

Key to the MPG function are the 4900M's programmable pin interface subsystem and the algorithms that take advantage of the system's versatility. The pin interface can be defined as groups of fields—address and data—with each of up to 1,024 pins in the system representing 1 bit in the field. Although a field can be any length up to pin capacity (368 pins for the MPG function, the balance for anything else), each four-pin group has behind it a distributed microprocessor (Advanced Micro Devices Inc.'s Am2901 4-bit bipolar slice) operating on data. A system with a full complement of MPG pins



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contains 92 such microprocessors.

A specific block of bidirectional pins is dedicated to MPG control, data, and address functions, Garlic explains, while the remainder are used for logic testing. The algorithms by which data is written into the memory of the board under test and then read back by the 4900M for comparison require knowledge of the memory array size, its static and dynamic characteristics, and its accessibility through associated logic. Details are fed in using instructions that have been added to Computer Automation's test operating system (TOPS). "One application program is all that is required to test a complete board, with the system automatically switching control to MPG in the appropriate sequence of test steps," Garlic states.

Microsteps. The 4900M has the real-time subsystem (RTS) of the earlier model 4900 that was designed for dynamic tests of boards containing microprocessors and other LSI components. The RTS module is a package that features a programmable clock rate of up to 10 MHz and a test-step repetition rate of up to 2 MHz. "While 2 MHz is adequate for dynamic testing of most logic boards," Garlic claims, "higher speeds are possible from the ability to supply eight clock phases programmable to 20 microsteps that execute in 25-ns [40-MHz] increments."

To be introduced at next month's Cherry Hill test conference in Philadelphia, the 4900M is principally targeted at environments requiring board-test confidence levels of 95% and up for manufacturers of a variety of complex circuit boards who are now using both dedicated memory testers and functional board testers. It is particularly suited to producers of pipelined and array processors, word processors, telecommunications gear, and avionics systems, Garlic notes.

Priced at $119,800, the basic model 4900M tester includes a 16-bit minicomputer, 256-K bytes of RAM, 10 megabytes of disk memory, the RTS and MPG subsystems, and a floppy-disk subsystem, as well as a programmer's console with a cathode-ray-tube display and standard software and programming aids. Availability is 90 to 120 days after receipt of order.

Computer Automation Inc., Industrial Products Division, 2181 DuPont Dr., Irvine, Calif. 92713. Phone (714) 833-8830 [351]

Instrument does manual or programmed tests on relays

The RT 160 programmable relay tester is believed to be the first of its kind. The tester, which replaces largely manual test setups of scopes, meters, and potentiometers, measures up to 16 key parameters on both latching and nonlatching relays. It handles contact arrangements ranging from single-pole, single-throw to four-pole, double-throw, including diode-suppressed and transistor-driven hybrid relays. The unit either tests one parameter at a time manually or sequences automatically through an entire group test, both with preprogrammed test limits. It is designed to perform full tests to mil spec group A requirements.

Relatively unskilled test personnel can program the unit. In a group A test, for example, all applicable test steps can be done automatically in less than 10 seconds. Among the steps are pickup and dropout characteristics (voltage, current, timing, and bounce) and contact and coil resistance, along with diode and transistor performance where necessary. If a relay under test fails, the failure and supporting data are displayed. Also, pass-fail status is indicated along with the parametric data.

The unit has these maximum pull-in and drop-out limits: voltage, 40 V; current, 400 mA; and operating and release time, 40 ms. Contact resistance is 4,000 mΩ (at 10 mA per 0.6-V open circuit) whereas coil resistance is 4,000 Ω at 10 mA. Line voltage is 115 V ac at 60 Hz and the tester consumes 65 W.

The RT 160 uses an 8035 Intel microprocessor with 2,048 bytes of program memory and 256 bytes of random-access memory for data. The price of the unit is $4,995, with deliveries taking from 12 to 16 weeks. One version incorporates an inexpensive line printer for applications where data logging is required.

The Markenrich Corp., 14946-F Shoemaker Ave., Santa Fe Springs, Calif. 90670. Phone (213) 921-0250 [352]

Development system for 6500 sells for under $4,000

The Flaim/65 development system for the 6500 microprocessor family is priced at less than $4,000 but has features of processors costing over $10,000. The heart of the system is Rockwell's Aim 65, which includes a 20-character alphanumeric display, thermal printer, and keyboard.

The Flaim/65 includes an expansion motherboard with five card slots (three unused), a 5¼-in. dual disk drive with 160 kilobytes of program and object-code storage, a power supply, and a 16-K-byte static random-access memory. The entire disk operating system is contained in erasable programmable read-only memory.

The Flaim/65 software includes a ROM-based PL/65 compiler designed for the 6500 family; its output is assembler language source code. This code is passed through an A/65 RAM-based assembler to produce the

final object code. A PL/65 optimizer is also included.

A complete system is priced at $3,705 in the U. S. Availability is from stock to four weeks.

Compas Microsystems, division of Computer Applications Corp., 224 S. E. 16th St., Ames, Iowa 50010. Phone (515) 232-8187 [353]

Introducing System 716—our multi-channel system of anti-aliasing Brickwall filters, the Wavetek Rockland innovation that provides remarkably sharp rolloff of better than 115 dB per octave. Up to 16 channels of stable low-pass or high-pass filtering lets you apply our Brickwall technology to multi-channel digital signal processing and other systems use.

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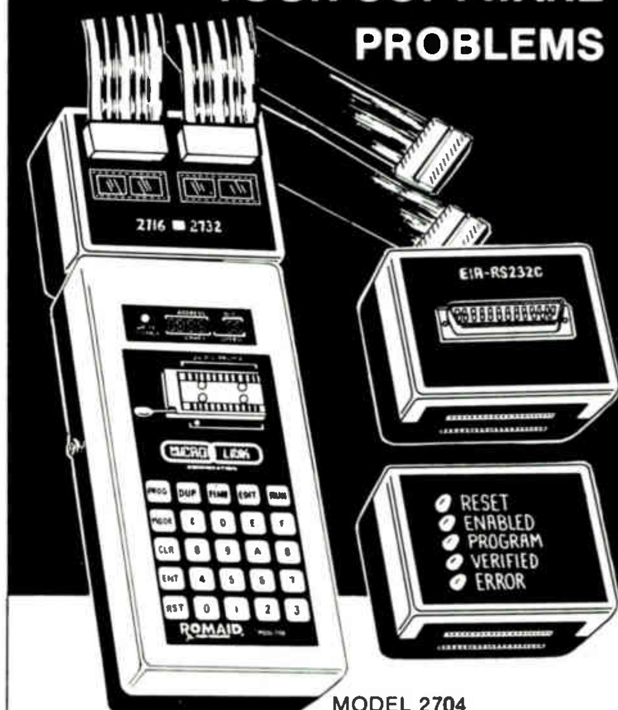

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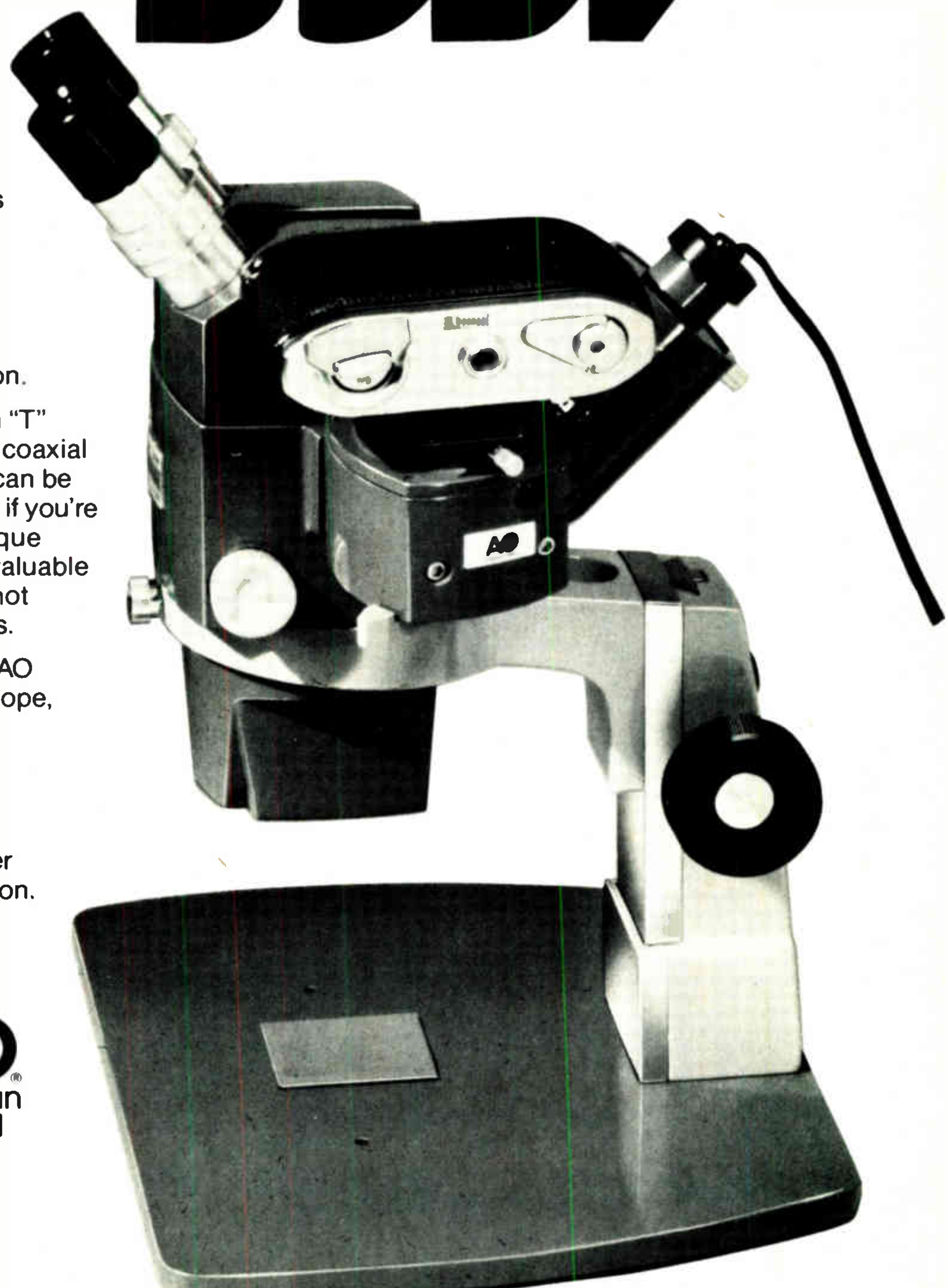

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Computers & peripherals

Unit ties port to 248 terminals

Port concentrator for Univacs allows serial port to handle mix of modems and terminals

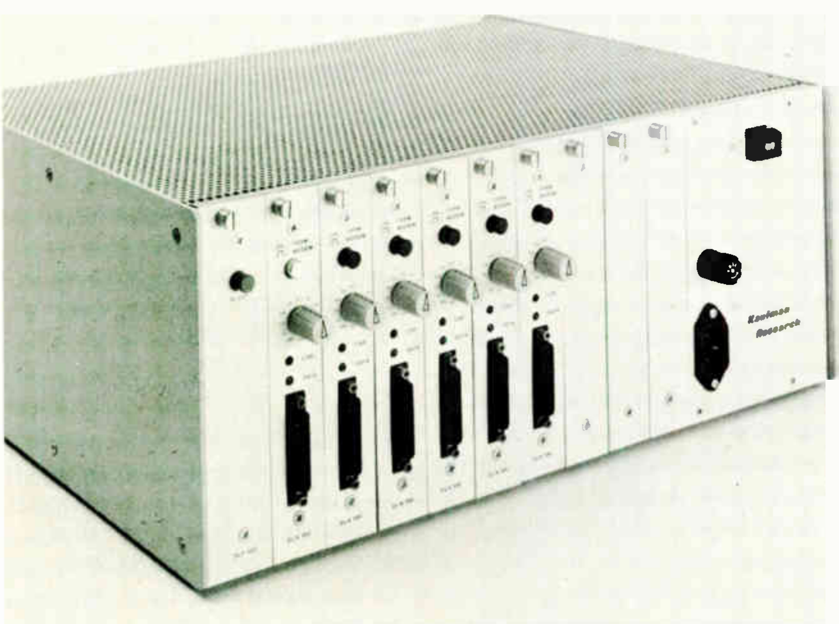
Adding ports to a computer to accommodate a large number of terminals can be an expensive proposition. But it may not be necessary with what Kaufman Research Manufacturing calls a true port concentrator such as its model 871, for use with Univac 80/60 computer systems using the protocols of the UTS 400 terminal.

Unlike time-division-multiplexing (TDM) concentrators and even most statistical-multiplexing concentrators, the 871 uses up only one RS-232-C communications port on the host computer system. On its other end, it can be servicing up to 31 nodes with eight drops each, for a total of 248 terminals (or other peripheral devices).

The 871 is similar in design to the firm's 870, which communicates through IBM's Binary Synchronous Communications (Bisync) protocol, allowing a "dumb" ASCII terminal to appear to the host computer in the same way an intelligent IBM 3270 terminal does. The 871 gives the same dumb-terminal option to users of Univac machines.

Their extensive bidirectional buffering capabilities are what separate the 871 concentrator from TDMs and statistical-multiplexing units. The usual TDM technique does not use buffering and does not compress data. It must, in fact, put characters into the data stream that represent blanks in order to keep track of the terminals sending the data. Statistical multiplexing uses buffering and compresses blank-space information to achieve increased bandwidth. However, except for the Micom series 900, which uses multidrop operation, these multiplexers are not capable of feeding into a single computer port.

Mixtures. Because of the extensive buffering capability in the line-interface modules (LIMs) of the 871, it can handle a mixture of transmission rates among the devices it services—from 300 b/s to 19.2 kb/s. It communicates with the host at similar rates. A slow and a medium-speed terminal can both communicate through the concentrator with a host computer that is receiving and trans-



mitting at a higher rate.

Each line-interface module contains its own Motorola 6800 microprocessor and its own bank of random-access memory to control and buffer the data. The modules also allow the user, for the first time, to freely mix data-terminal with data-communications equipment. Each LIM can support either a modem or a terminal.

Unlike statistical multiplexers and TDMs, the 871 can be operated remotely or locally. That means that only one unit is required for a phone hookup, rather than one on each end of the line to condense and then distribute signals.

The 871's basic price is $4,765 with one line-interface module; additional LIMs are $690 each. Delivery of the concentrator and the LIMs is 60 to 90 days.

Kaufman Research Manufacturing Inc., 175 S. San Antonio Rd. No. 217, Los Altos, Calif. 94022. Phone (415) 948-3777 [361]

5.25-in. floppies have 96-track/in. densities

Two 5.25-in. minifloppy disk drives have track densities of 96 tracks per inch. The single- (SA410) and double-sided (SA460) drives feature unformatted capacities of 500 kilobytes and 1 megabyte, respectively, using double-density recording. For improved access time, the drives incorporate a helical cam V-groove lead screw for head positioning, instead of the usual band or disk positioner.

Track-to-track access time is 6 ms; average access time to the disk is 160 ms; and average latency is 100 ms. Transfer rates for the drives are 250 kb/s for double-density recording. Recording density is 5,876 b/in. Mean time between failures is 8,000 power-on hours.

The SA410 reads disks written by the SA400, and the SA460 reads those written by the SA400, SA450, and SA410. The drives are priced at $325 for the SA410 and $400 for the SA460, when bought in quantities of 100. They are available in the fourth

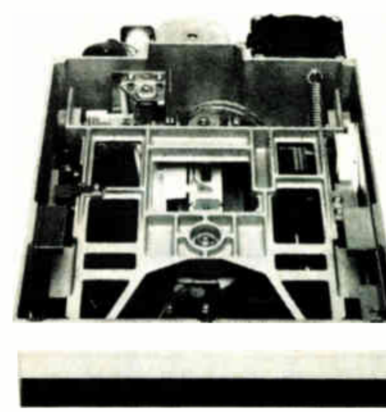
Circle 22 on reader service card

quarter of this year.

Shugart Associates, 475 Oakmead Parkway, Sunnyvale, Calif. 94086. Phone (408) 733-0100 [363]

Shock-absorbing head-loading system increases floppy life

An 8-in. flexible-disk drive features an air-damped head loading system that increases disk media life to better than 6 million passes. The model FD1160 Soft-Touch drive has a mean-time-between-failure rating of 15,000 power-on hours, about twice the industry average, says the manufacturer.



The double-sided, dual-density drive has a formatted capacity of approximately 1.2 megabytes and an unformatted capacity of up to 1.6 megabytes. Maximum track-to-track access time is 5 ms. The head-loading system used in the drive is a pneumatically controlled shock-absorbing device that minimizes media scoring and scratching.

The FD1160 is available immediately and is priced at $740 in quantities of 100.

NEC Information Systems Inc., 5 Militia Dr., Lexington, Mass. 02173. Phone (617) 862-3120 [364]

$10,900 OCR reader puts 250 pages/hour into system

The Burroughs 1205 optical-character-recognition page reader can triple the productivity of a word-

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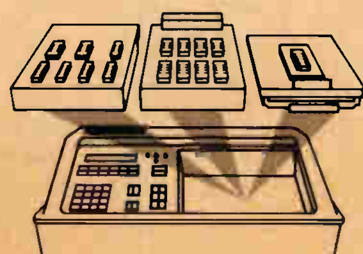


UNIVERSAL PROGRAMMING FOR PROMS & LOGIC DEVICES

New products

processing center for less than the cost of a single work station, says its manufacturer. The OCR text input device will sell for $10,900, whereas competitive OCR systems sell for from $16,000 to over $50,000, says Burroughs. The 1205 reads typed or printed documents electronically, translates the words and formats into digital form, and automatically transfers the digitized documents to a word processor or computer for final formatting. It can put 250 pages an hour into a word processor with less than one error in 100,000 characters scanned. In addition, the 1205 turns an ordinary 10-pitch, single-element typewriter with an OCR-B type font into a text entry device, so that any typist can enter text.

Burroughs will allow full-price trade-in of a model 1205 toward a more advanced OCR page reader if the transaction takes place within one year of the date of purchase. The 1205 offers 100-page feeders and interfaces to most stand-alone, clustered, or shared-logic word-processing systems. It is available for delivery in 30 days.

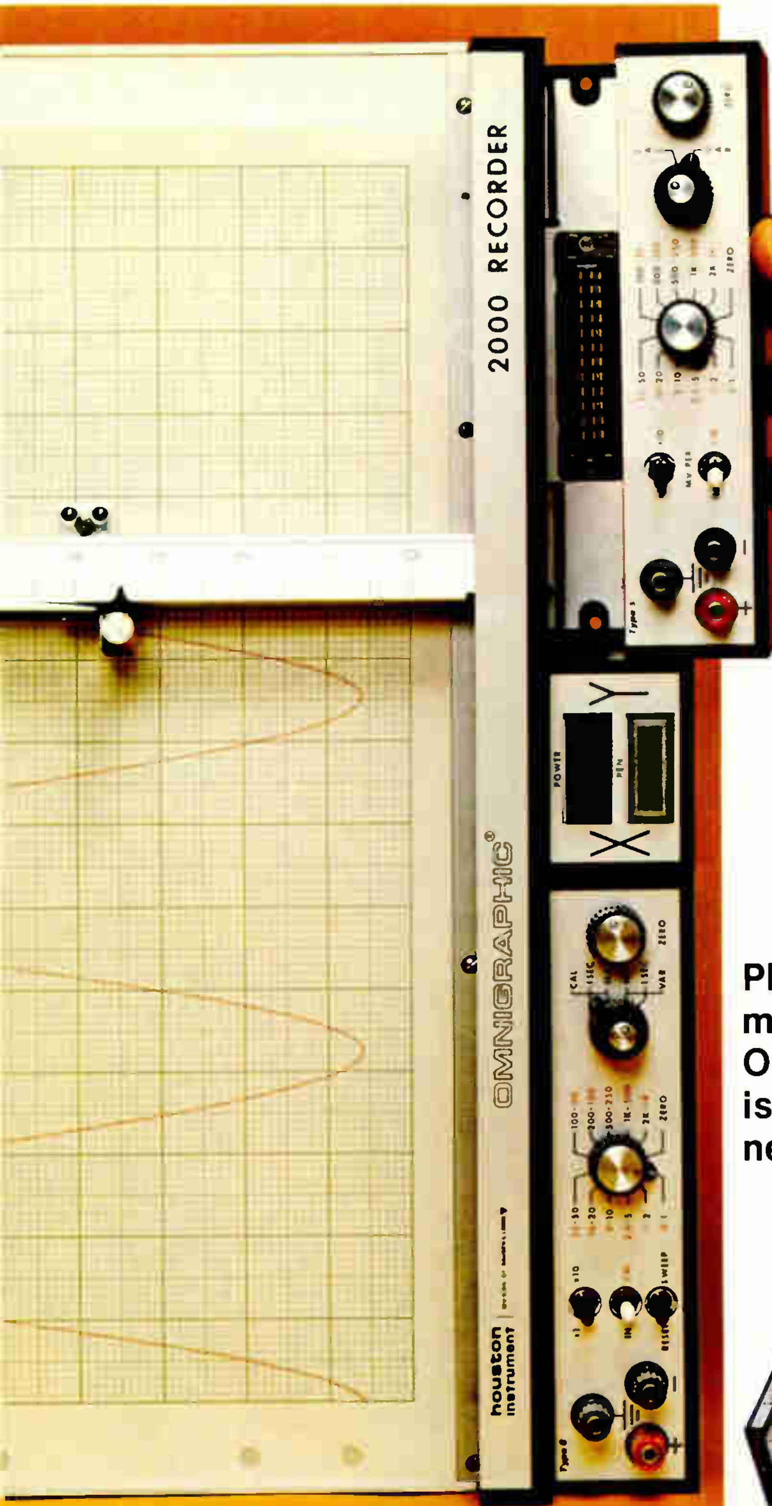
Burroughs OCR Systems, 9 Ray Ave., Burlington, Mass. 01803. Phone (617) 273-2222 [365]

8-in. Winchesters include controllers for $2,195

A single-board controller has been integrated into the shoebox-sized packages of International Memories Inc.'s 7710/7720 10- and 20-megabyte drives. With the controller, the drives have what the company says is the fastest access time for 8-in. Winchesters—35 ms average—and require only 75 W. The controller provides an asynchronous parallel interface between the drive and a central processing unit. It handles a wide range of diagnostics—from servo tests to media verification. The drive with controller sells for $2,195 in quantities of 250. Delivery is off the shelf.

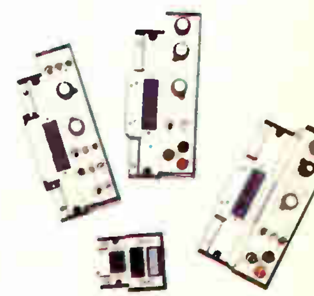
International Memories Inc., 10381 Bandley Dr., P. O. Box 880, Cupertino, Calif. 95014. Phone (408) 446-9779 [366]

When your applications change,



this recorder changes with them

Plug in your choice of modules and the Omnigraphic® Model 2000 is tailored to your need



The Omnigraphic Model 2000 is the world's best known most versatile X-Y recorder. The basic building block is a rugged die cast metal mainframe. A choice of 27 modules enables the recorder to perform in virtually any application.

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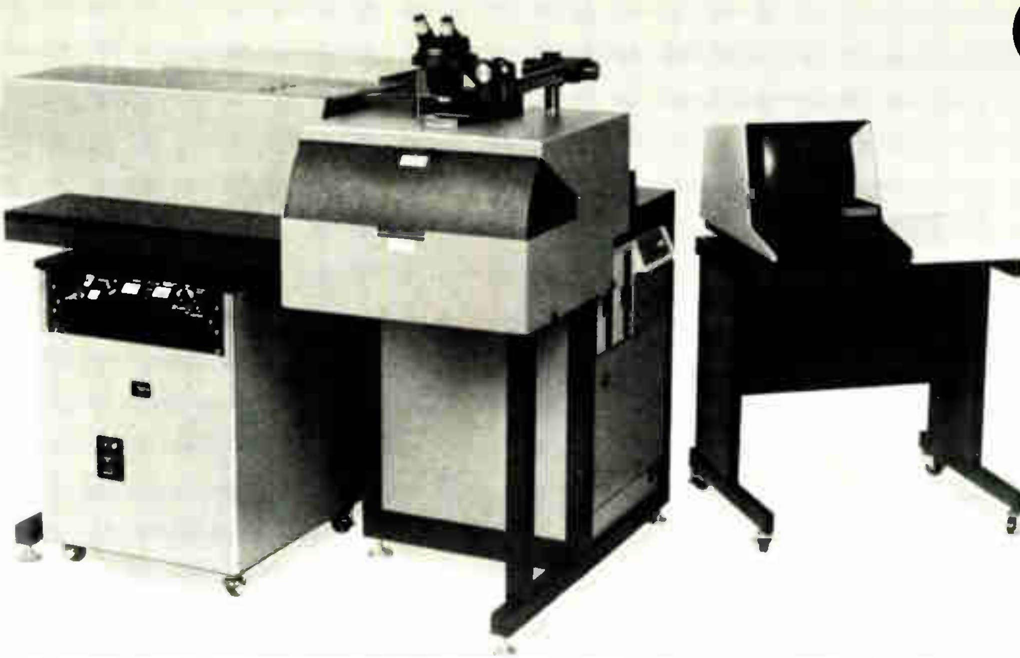
CLS 33



SIX REASONS WHY THE SMART LASER TRIM SYSTEM IS YOUR SMART BUY.

SMART is a word that defines intelligence; it can be applied to machines as well as humans. There's no better machine to apply that title to than the CLS-33 from Chicago Laser Systems. Introduced as the smartest, highest throughput laser trim system, it has proven that CLS-33 buyers are also smart.

1 Lower overhead. Reduced production costs for the high-volume user is the greatest strength of the CLS-33. Its practical design and high throughput lowers both immediate and long-term production costs of trimmed networks.

2 Design sophistication. Laser trim systems no longer need be massive monoliths of hardware and wire. In the CLS-33, engineering sophistication has overcome traditional size and complexity barriers. This achievement has not gone unnoticed by the many major network manufacturers who have become CLS customers.

3 Intelligent software. The system microcomputer of the CLS-33 is backed up by the most intelligent software operating system in the laser trim industry. Its structure frees the operator to concentrate on trimming the

product, instead of on time-consuming computer programming procedures. Programming effort is further minimized thru on-line compiling and editing and thru program de-bugging in user language. This remarkable software operating system is another CLS exclusive.

4 Maintenance ease. The CLS-33 was built to require a minimum of maintenance, but at the same time was designed to be highly maintainable. Faults can be rapidly isolated to the module level with the systematic diagnostic programs. Diassembly of the entire system, for full access to modules, requires just minutes. Efficient circuit design has reduced the total number of modules to be considered in fault finding —another time saver.

5 Free training. With every system sold, Chicago Laser provides complete training of operator and maintenance personnel at no extra cost and with no limits on time or number of operators. In addition, the easy-to-understand documentation supplied with the CLS-33 is so comprehensive that it is virtually a training course in itself.

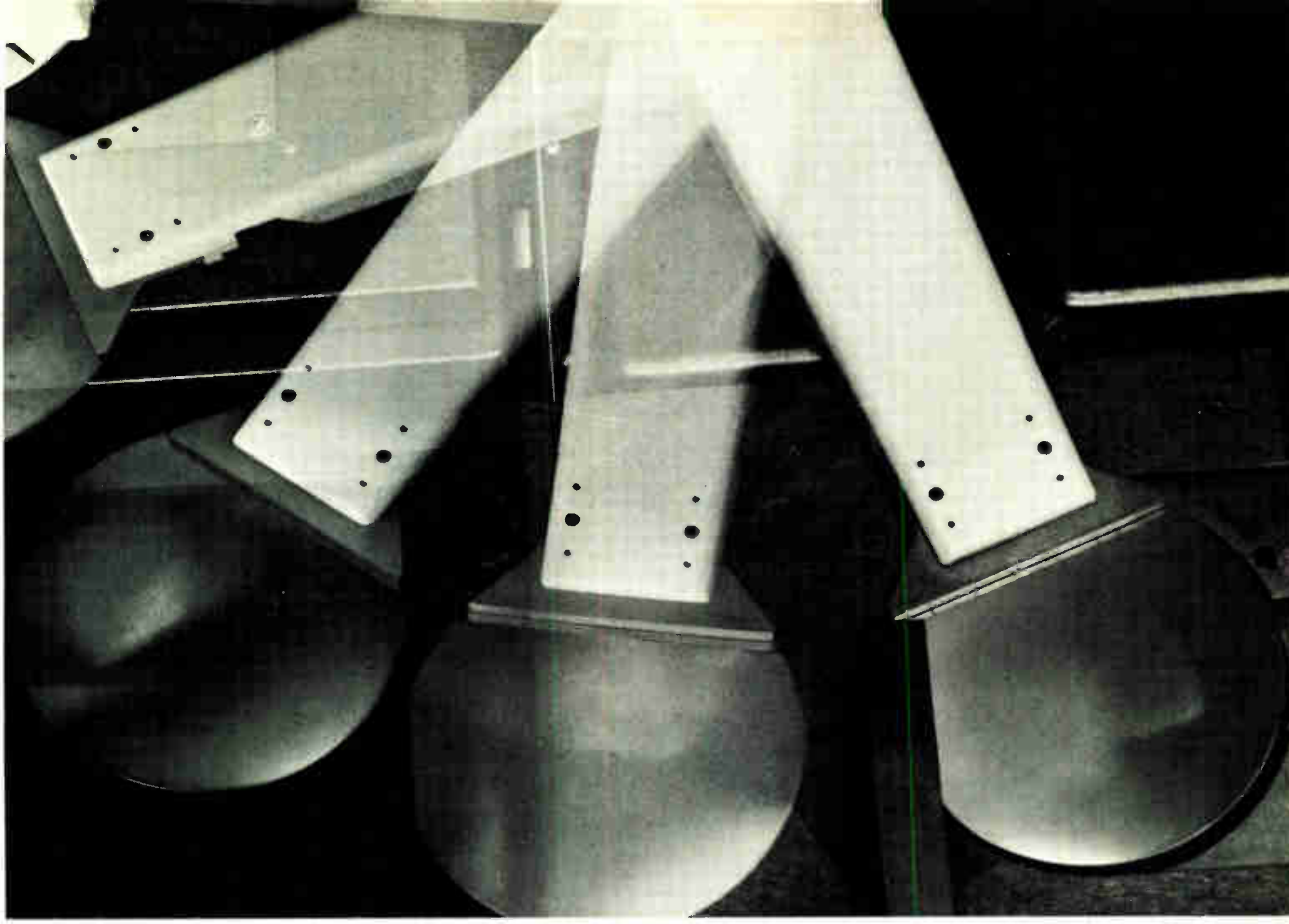
6 Adaptability. From computer program inputs to system operation, the CLS-33 is adaptable to most any production demand. For high-volume applications, an available air-bearing step-and-repeat handler allows the CLS-33 to trim an incredible 100,000 resistors per hour. A stack-load station is also available.

If you've been searching for a sophisticated yet manageable laser trim system, discover the CLS-33 and search no more. It's a system that will continue to remind others that you made a "smart buy" and selected the Smart Laser Trim System. For the complete story and a frank appraisal of how the CLS-33 can fulfill your needs, contact:

Chicago Laser Systems Inc.

4034 North Nashville Ave., Chicago, IL 60634 • Phone 312-282-2710 TELEX: 206-647

Circle 30 on reader service card



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Our DSW Wafer Stepper™ direct step on the wafer system is highly automated. So you can expect higher yields of good, small feature circuits than with any other system available.

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In short, our DSW Wafer Stepper is unmatched for automated performance and wafer imaging precision. Which is precisely what you'd expect from a Mann™ photolithographic product.

For more information, write GCA/Burlington Division, 209 Burlington Road, Bedford, Massachusetts 01730. Or call (617) 275-5400.

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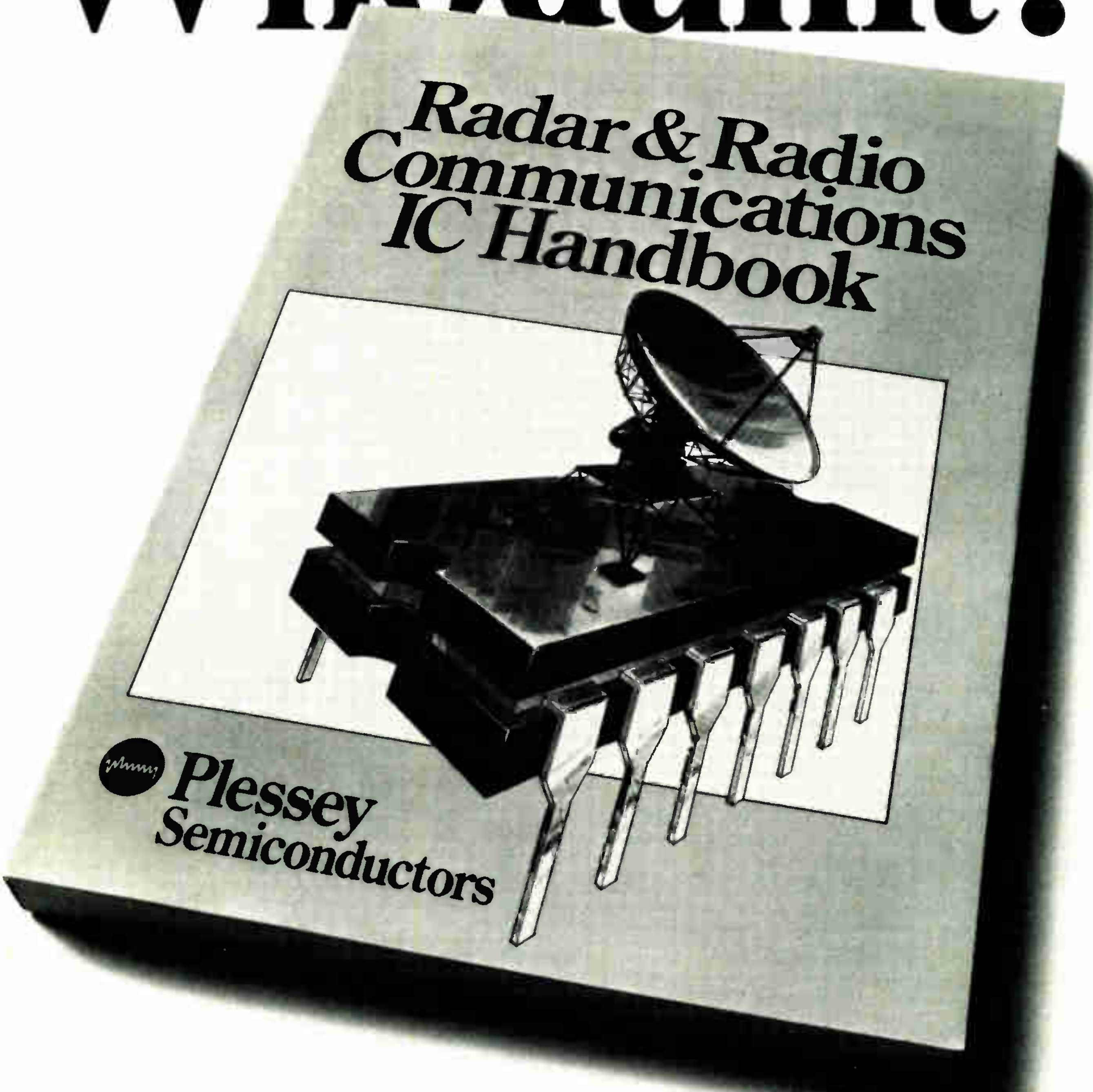

The new Plessey RADAR & RADIO COMMUNICATIONS IC HANDBOOK should be at the very top of your current reading list. It's chock-full of applications notes and design tips, a "cookbook" for all you high frequency fans that will simplify your designs, increase reliability, improve performance and lower your system cost.

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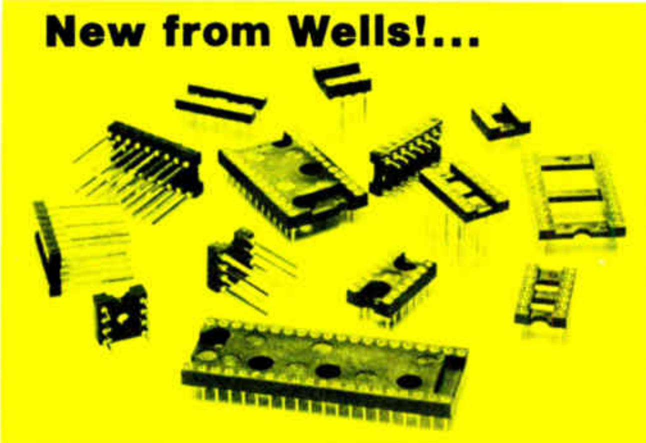

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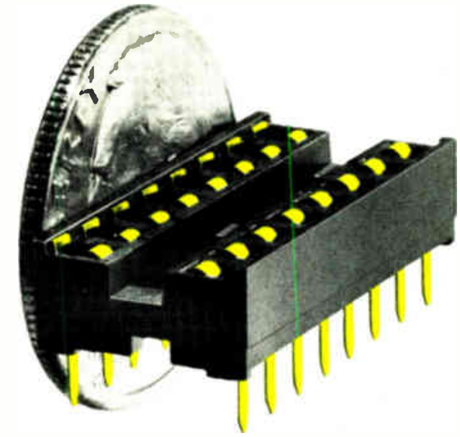

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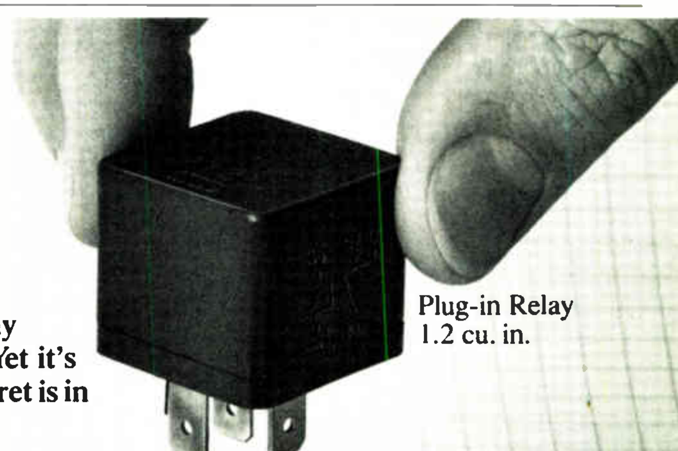
Circle 38 on reader service card

Robert Bosch announces a new Mini-Giant built to help resist moisture, dust and galloping inflation



Plug-in Relay
1.2 cu. in.

Here's a new 30-amp, 12 VDC plug-in relay engineered to do the job better than ever. Yet it's available at or below our 1979 price. The secret is in the housing of rigid polyamide plastic.

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The relay is protected by a seamless housing. Neither moisture nor dust can easily penetrate. The bottom of the unit is vented with a single hole to avoid heat buildup. But for extra heavy-duty, outdoor applications, even this vent can be closed with a Teflon plug that filters out foreign matter while allowing air to circulate.

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2800 So. 25th Avenue
Broadview, IL 60153
or phone Dave Robson,
(312) 865-5459

ROBERT BOSCH

Circle 43 on reader service card

Packaging & production

Tape delivers solder evenly

Solder delivery system cuts hand work of terminating flat transmission cables

Transmitting digital data at high speeds often calls for the use of flat transmission cable consisting of conductors 7 to 10 mils or less in diameter molded into a Teflon FEP (fluorinated ethylenepropylene) insulation layer. Signal wires are spaced on 50-mil centers with pairs of ground wires placed in between. This type of cable, with its tiny conductors, does not lend itself to insulation-piercing mass-termination techniques: soldering is necessary.

Space limitations and difficulties in heating and positioning of wires over terminals make hand-soldering the only satisfactory way of terminating these cables to a connector or a paddleboard. A highly skilled solderer with excellent eyesight is required to handle the tiny wires in the cramped space. A replacement for this difficult and time-consuming method is clearly in order.

Raychem's solution is a solder-delivery system that allows as many as 300 joints to be soldered in 1 minute. The delivery system has two components, a solder-delivery strip or tape, and a companion heating tool. The system consistently produces uniform solder joints, and it eliminates any possibility of solder bridging.

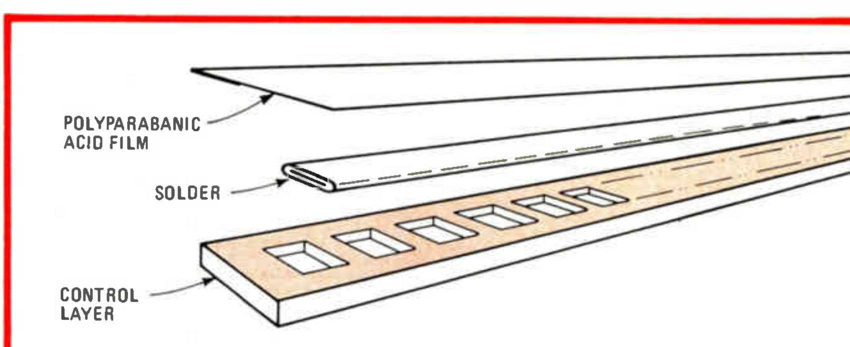
The diagram shows an exploded view of the strip, which contains soldering flux, solder, and a carrier strip. The top layer is a 5-mil thick polyparabanic acid film coated with adhesive. The adhesive holds the solder. The bottom layer is made from an irradiated cross-linked polyvinylidene fluoride sheet having windows that correspond to the spacing of the wire terminals. During solder melting, the windows divide the solder evenly between terminals. A flux coating is applied to the surfaces facing metal to be cleaned.

The components of the strip are laminated together to form a tape less than 0.020 in. thick and 0.325 in. wide. The laminate is conveniently packaged in spools and dispensed as required per connnector length.

The companion soldering tool uses twin infrared lamps in a special reflector to provide high wattage per unit length at the focus. A copper-alloy platen receives the radiant energy and conducts it to the solder-wire interface.

In a typical application, the solder-filled tape is placed over the prepared cable conductors that are to be terminated to the connector terminals and then cut to fit. A drawer-holder assembly is closed and inserted into the heater module, initiating automatically timed heating of the solder delivery vehicle. After soldering, the plastic part of the solder strip can be peeled away if necessary.

The Berg Electronics division of



Solder control. Many evenly spaced connections on flat digital transmission cables can be soldered quickly with this solder-delivery tape (shown exploded) and a heating tool.

Du Pont Co. is already applying this method for terminating its TLC connector to transmission-line cables having a pitch of 50 mils. The Raychem solder-delivery system is being used to mass-terminate signal and ground wires and selected grounding fingers on the Berg connector.

The system can be extended to other window spacings, wire terminal geometries, and layout patterns. In large volumes, the strip will cost 2¢ to 10¢ per line.

Raychem Corp., 300 Constitution Dr., Menlo Park, Calif. 94025 [391]

Wire bonder has impactless head and programmable table

A semiautomatic wire bonder designed for use with hybrid chips incorporates an impactless bonding head and a microprocessor-controlled, three-axis (X-Y-Z) table. The bonding head deforms wire uniformly. Capillary perpendicularity, tail length, search height, bond forces, and microscope focus are all kept constant by the programmable table regardless of changing bonding heights.

Bond time and bond locations on the model 2406 are programmable on a per-wire and per-die basis. The machine is programmed by stepping a device through a bonding routine and entering the positioning reference points in computer memory. The wire bonder sells for about $20,000.

Kulicke and Soffa Industries Inc., 507 Prudential Rd., Horsham, Pa. 19044. Phone (215) 674-2800 [393]

Laser imaging system cuts need for artwork

The Laser Artmaster Generator has been designed for the precise exposure of images on photosensitive media. It is driven by computer-aided-design–generated magnetic tape. A computer controls a laser scanner, which produces the images—either artwork or images that

TELESCOPE TIME AND SPACE WITH A TELECONFERENCE.

You are having your regular weekly conference with the field office.

Though you are at headquarters and your field office is a thousand miles away, it's as if you all meet in one location.

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Bell's advanced communications technology is changing ideas about how to transact business. It's becoming clear, for instance, that what we call the "conference" is one of the many aspects of information management and communications. And that's our business—the knowledge business.

For more information, call toll free 800-331-1750. In Oklahoma, call collect: 918-664-8300.

The knowledge business

go directly on printed-circuit substrates without artwork. Throughput depends on the photosensitive medium used: silver halide film, 18 by 24 in., can be exposed in 2 minutes. In contrast, the vectorized plotter method takes up to 2 to 5 hours. On printed-circuit substrates coated with certain standard film resists, 18-by-24-in. images can be exposed in 4 minutes.

The base price for the laser imaging system is $6,600. Delivery takes six to nine months.

Eocom division of American Hoechst Corp., 15771 Redhill Ave., Tustin, Calif. 92680 [395]

Hybrid assembly system has five programmable axes

The Microplacer is a computer-controlled assembly system for hybrid chips that moves along five servomotor-driven axes, each individually programmable. Tweezer-like grippers can selectively pick up as many as 60 different electronic components in any combination and place up to 200 on a substrate without changing component feeder mechanisms. The unit places 3,000 components per hour.

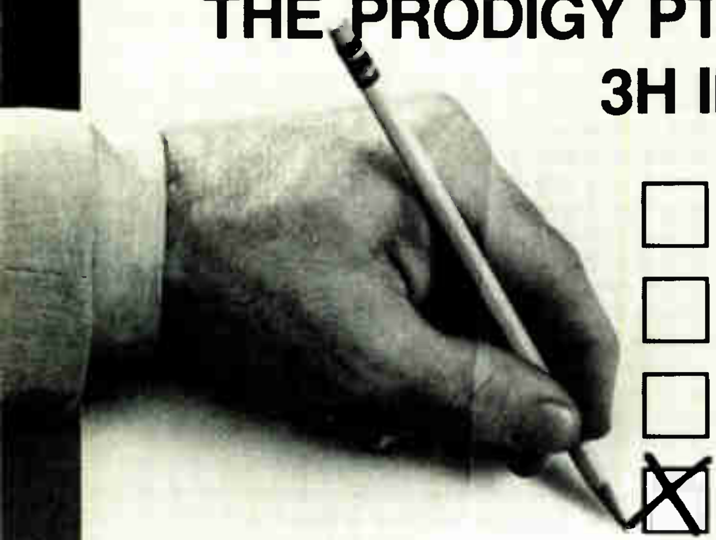
Programming is done by manually taking the gripper through each cycle. The computer calculates the most efficient series of movements from picking up the component to placing it and records that series in its memory. The entire program is retained on a floppy disk, which is standard on the Microplacer. The location of each feeder mechanism is also retained in microprocessor memory.

The system will be sold either as a complete customized hybrid assembly system with a choice of component feeders and substrate presentation mechanisms, or as a basic assembly system to which the customer will add the component feeders. The basic system starts at $95,000 and can be delivered in 22 to 24 weeks.

MTI Corp., 55 Industrial Dr., Ivyland, Pa. 18974. Phone (215) 355-3110 [396]

THE MULTIPLE CHOICE TESTER

THE PRODIGY PT900 SYSTEM FROM 3H INDUSTRIES TESTS:



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- ☐ Transformers
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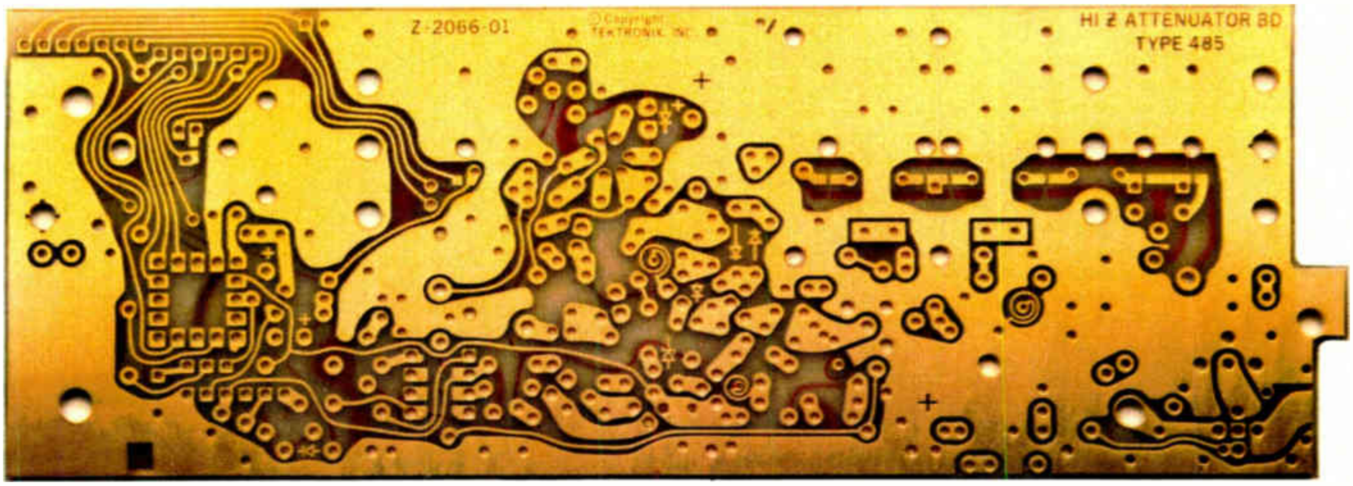
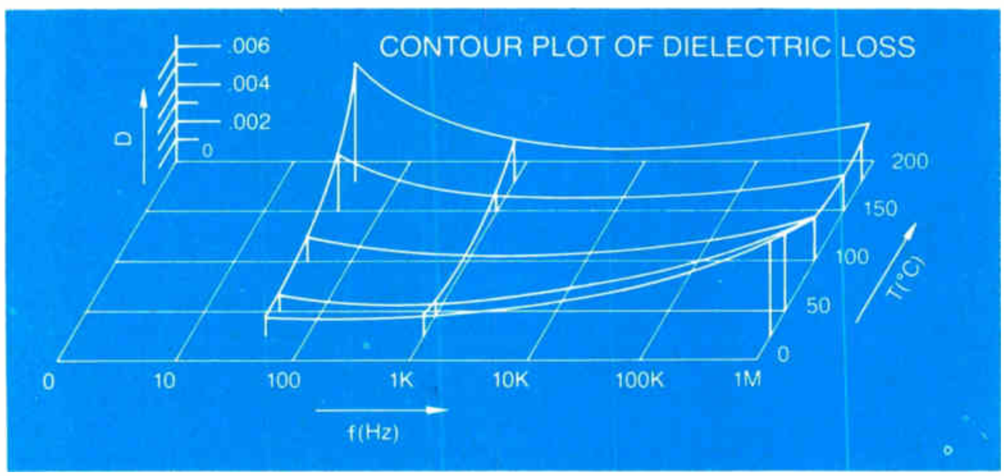
VISIT US AT CHERRY HILL-BOOTHS #119 & 120

Circle 65 on reader service card

POLYSULFONE PCB SUBSTRATE GIVES



PERFORMANCE CLOSE TO PTFE/GLASS,



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Circle 75 on reader service card

Microcomputers & systems

I/O board has four 8-bit ports

Z-bus–compatible board allows bidirectional ports to be enabled independently

The latest addition to Zilog's line of Z-bus–compatible products is a digital input/output board (DIO) featuring 32 I/O lines configured as four 8-bit ports. Separate data-strobe inputs are provided for each byte-wide port so that external devices may update the on-board latches 8, 16, 24, or 32 bits at a time.

The bidirectional ports are programmed as either an input or output by the processor. A control register serves that purpose as well as that of enabling the external strobes: 4 of the register's 8 bits determine whether the four ports will be input or output, while the other 4 determine whether input data will be latched by external strobes or upon request by the processor.

The board operates in the polled mode and has no provisions for generating interrupts. Switches in a dual in-line package determine whether the board will operate as a memory-mapped device or in a separate I/O space. The ports are buffered from the outside world by high-drive transceivers able to deliver 48 mA.

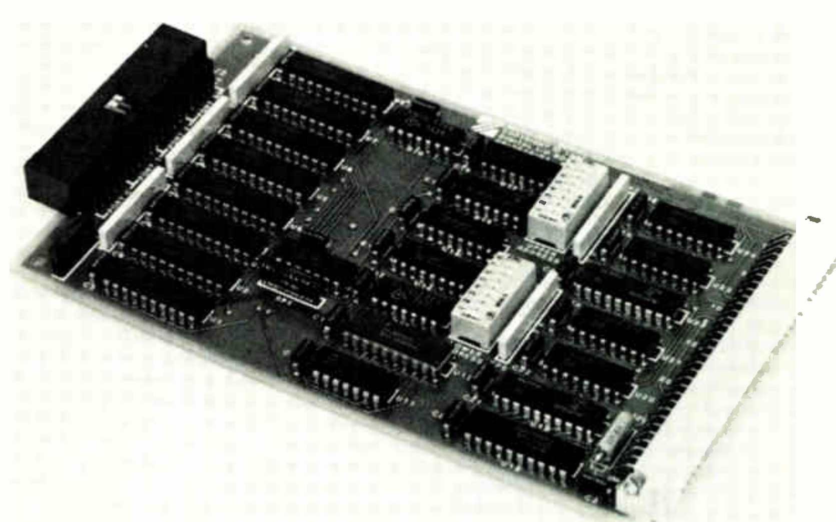
Backplanes. The DIO joins the ZCM family of Z-bus–compatible boards. The two Z-bus backplanes use either one or two 96-pin connectors, thus offering higher density and reliability than standard card-edge connectors. Only one of the connectors is used by the Z bus; the second is provided for any custom interconnections the system designed may require. The DIO is a single-width board that, like the other single-width boards, works with both single- and double-width backplanes.

Double-width boards include a Z8001 microprocessor unit featuring 32 K bytes of random-access memory and two serial ports, a Z80-based single-board computer, a 64-K-byte dynamic RAM board, and an IBM-compatible double-density floppy-disk controller.

Other single-width boards include a Z8-based single-board computer featuring the Basic language in read-only memory, a RAM/ROM module, analog input and output boards, and a controller for single-density floppy-disk drives.

The DIO uses a single +5-V sup-

Joins family. Z-bus–compatible digital input/output board's four independent bidirectional 8-bit ports can be memory-mapped or can be operated in a separate I/O space.



Make no mistake with Computrol Megabit modems

". . . We have successfully utilized thousands of them in a variety of Sanders' graphics products and systems. . . ."

W. Bernstein

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Sanders Associates, Inc., Information Products Division, produces a variety of high speed, interactive graphics products for a broad range of government and industrial uses.

1 bit in 10^{12} error rate for local networks on coaxial cable

William Bernstein, Vice President, General Manager, IPD of Sanders Associates, Inc. talks about Computrol modems. *"The Computrol coaxial cable modem was selected after a careful evaluation of alternative products and approaches, taking availability, reliability, performance and cost into consideration.*

We have successfully utilized thousands of them in a variety of Sanders' graphics products and systems.

Its flexibility gives our designers freedom to readily incorporate the modem into new systems."

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- **Operates at all data rates from DC to 2 Megabits/sec without readjustment**
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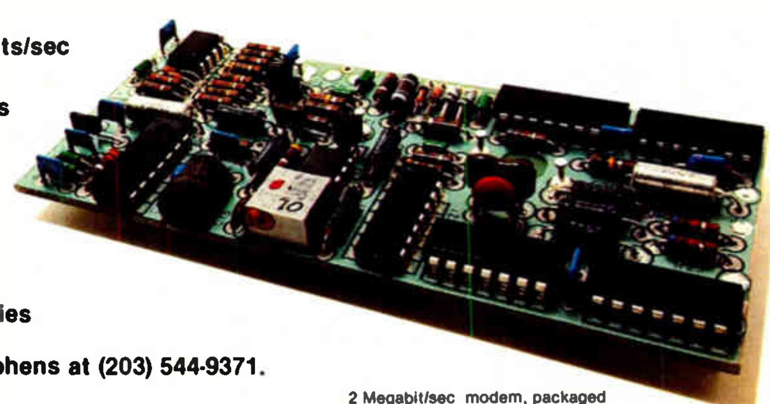


2 Megabit/sec modem, packaged for mother board mounting, measures 4.5" x 2.0" x 0.38"

computrol

15 Ethan Allen Highway
Ridgefield, CT 06877
(203) 544-9371

Circle 83 on reader service card

ply, is priced at $375 in single quantities, and will be available in January 1981.

Zilog Inc., 10340 Bubb Rd., Cupertino, Calif. 95014 [371]

Entry-level desktop computer sells for $3,695

The Vector Intelligent Partner (VIP) offers state-of-the-art word-processing and list-management capabilities and can be easily upgraded by adding disk capacity. This entry-level computer consists of an integrated video console and a single 315-K-byte minidisk drive.

The drive is housed separately so it can be replaced by a 2-megabyte diskette unit or a 30-megabyte Winchester drive or so three more 315-K-byte drives can be added. The VIP is available off the shelf and is priced at $3,695.

Vector Graphic Inc., 31364 Via Colinas, Westlake Village, Calif. 91362. Phone (213) 991-2302 [373]

Four-user microcomputer on S-100 bus costs under $5,000

In a four-user configuration, the Decision 1, a multitasking S-100–bus microcomputer, will sell for under $5,000. The processor will feature a UNIX-like operating system that runs CP/M as a subtask. The central processing unit has a 4- or 6-MHz Z80, memory management hardware, and a floating-point processor. The memory management

New products

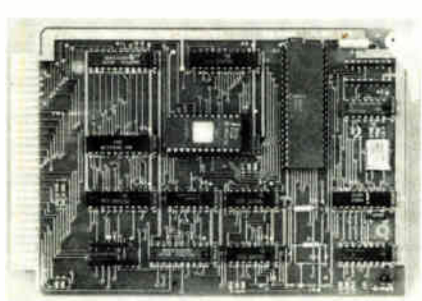
hardware includes a memory map that supports up to 16 tasks without swapping. Disk support includes dual 800-kilobyte 5-in. floppy-disk drives mounted in the mainframe, dual 1.2-megabyte 8-in. floppies, and a 26-megabyte Winchester hard disk. Decision 1 will be available through local computer stores.

Morrow Designs, 5221 Central Ave., Richmond, Calif. 94804. Phone (415) 524-2101 [374]

16-bit microprocessor is STD-bus compatible

High-performance systems like fast-Fourier spectrum analyzers can be implemented with STD components now that the DM-8800 microcomputer board has brought 16-bit processing and 1-megabyte addressing to the 8-bit bus. The 20-bit full addressing range of Intel's 8088 microprocessor is available in the DM-8800. The 1 megabyte of memory is addressed on a system with 16 address lines by multiplexing the 4 high-order address bits over the data lines at the beginning of a memory cycle. STD memory boards ignore these bits and are thus compatible with the DM-8800 if no more that 64-K bytes are used. For 2-, 4-, or 8-K bytes of memory, the DM-8800 has an on-board erasable programmable read-only memory (a 2716, 2732, or 2764) decoded at the top of the megabyte address space to leave the first 64-K bytes free for off-board memory. The DM-8800 is priced at $395 and delivery is in four weeks.

Desert Microsystems Inc., Star Rte. 1, Box 1174-D, Pasco, Wash. 99301. Phone (509) 547-3397 [376]



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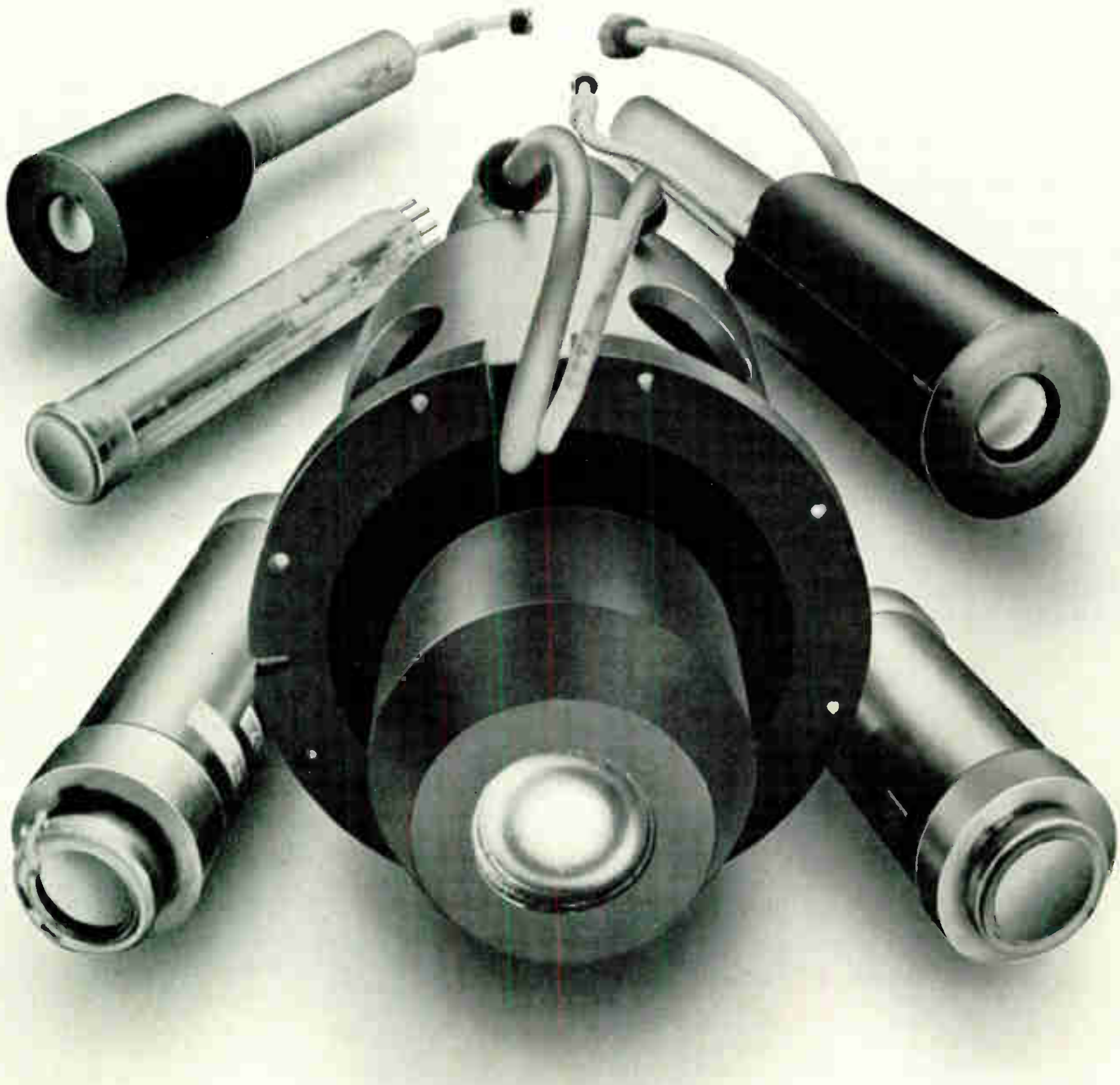

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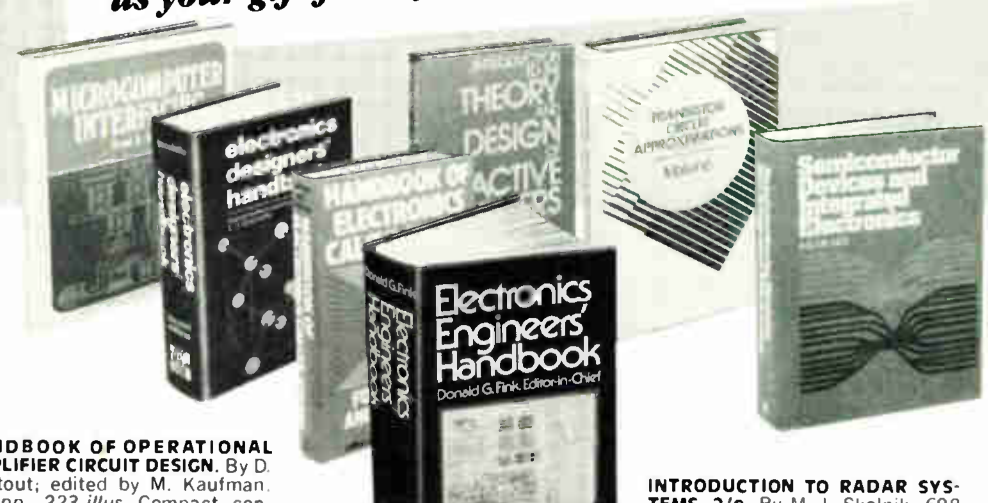

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MICROELECTRONICS: Digital and Analog Circuits and Systems. By J. Millman. *881 pp., 700 illus.* This giant book takes you step by step from a qualitative knowledge of a semiconductor, to an understanding of the operation of devices, and finally, to an appreciation of how these are combined to form microelectronic chips.
423/27X Pub. Pr., $28.95 Club Pr., $22.50

Software

Operating system shares storage

CP/M-compatible network operating system lets users share common peripherals

The ANOS/ADAY network operating system lets stand-alone computers share expensive and seldom-used resources like hard disks and line printers. What's more, it is CP/M-compatible, so that its users have a wide range of compilers, utilities, and application programs available to them.

Implemented in a star configuration, the network dedicates one computer, the hub, to handling files on mass storage devices, printing output, and communications with each satellite computer. Each satellite does its processing locally, using the network only for mass storage. Communication between satellites is restricted to sharing any data in disk files that is made public and available to all users.

The main user interface to the system is the command-line interpreter. This program provides each user with all the common disk file manipulation commands, plus arithmetic, boolean, relational, and string-handling functions that may serve as command parameters or else stand alone in a desk-calculator mode.

Illusion. Of the two major system components, ANOS is the operating system proper, residing in the hub, and ADAY consists of two monitor programs, one for the hub and one for the satellites. The satellite monitor appears to the user to be a resident disk operating system, but in fact all file accesses are performed by direct communication with the hub. The hub monitor interprets requests from the satellites, spools output requests to printers, and refers file accessing to ANOS. At present the hub processor must be a Z80, but the satellites may be 8080s.

ANOS implements a disk paging system that maintains the most often used file pages (each 1,024 bytes long) in its free semiconductor memory, thereby streamlining throughput. It also holds the input/output routines in a separate area that is easily configured for the particular hardware being used. On power-up, each user logs in via the command line interpreter using passwords that are remembered by the hub. A user may form sign-on and other procedural files that employ any combination of commands but are executed with a single directive.

Avocet, originator of several cross-assembler programs (1802, 6502, and 6800-to-8080), offers ANOS/ADAY in two configurations. An end-user version includes object code only and is priced at $400. A package for the original-equipment manufacturer includes source code, unlimited distribution rights, and six months' implementation assistance for $100,000. Both are available now for CP/M 1.4 compatibility, and in two months for CP/M 2.2.

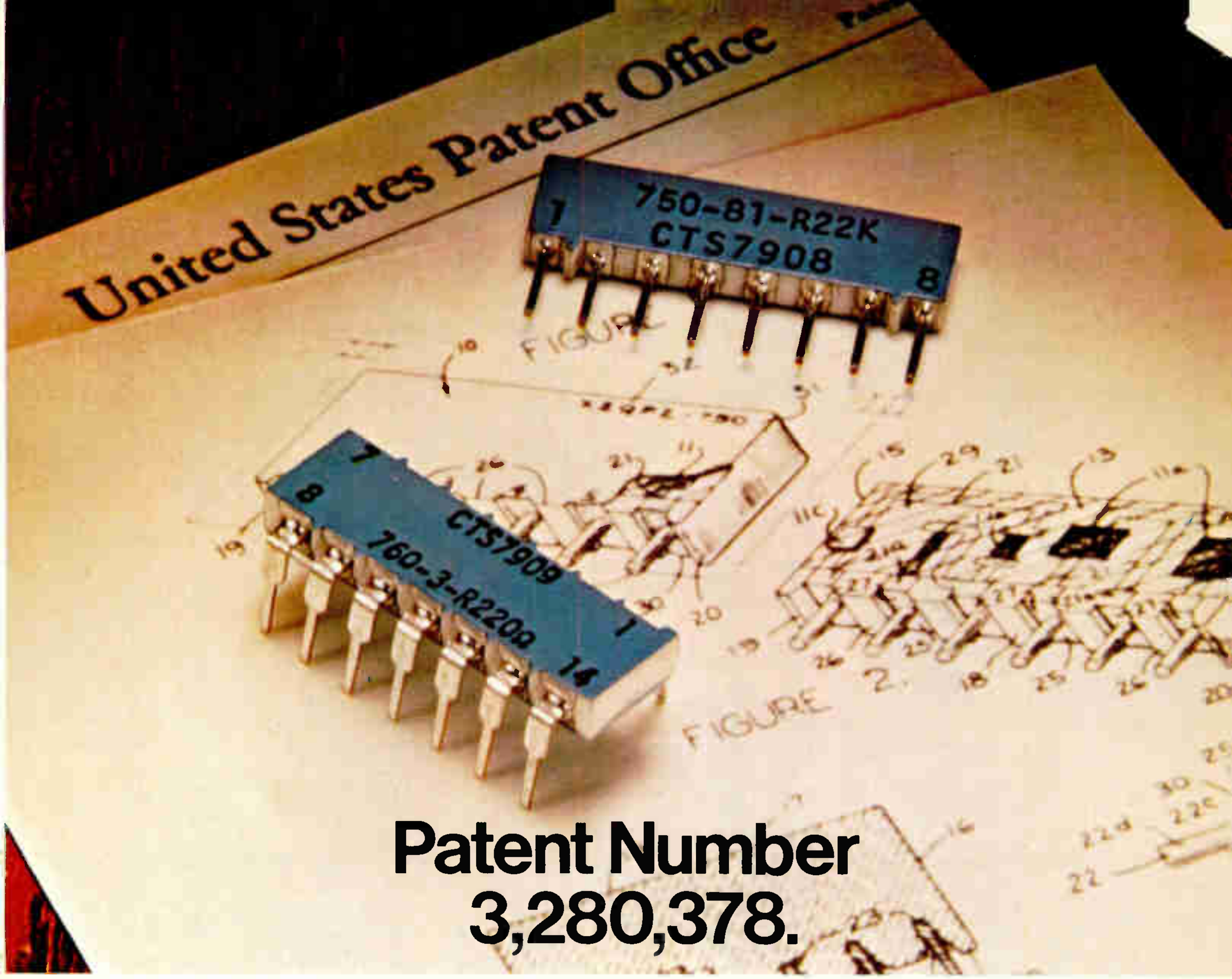
Avocet Systems Inc., 804 South State St., Dover, Del. 19901 [381]

16-bit chips get enhanced UNIX operating system

Xenix, a portable operating system for 16-bit microprocessors, is the Version 7 UNIX operating system from Bell Laboratories with several enhancements. The interactive, multiuser, multitasking system will run on all advanced microprocessors, including Intel's 8086, Zilog's Z8000, and Motorola's 68000, as well as on Digital Equipment Corp.'s PDP-11 series. Because Xenix is writen in the C programming language, it is easily transported to different microprocessors.

All of Microsoft's existing system software, including Cobol, Pascal, Basic, and DBMS, will be adapted to run under the Xenix system, and all existing software written for the UNIX operating system will be compatible as well.

The Xenix system is available



Patent Number 3,280,378.

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through an OEM license agreement, priced on a scale that depends on the number of users per system and the number of systems sold by the original-equipment manufacturer. The Xenix on the PDP-11 is available this month; Xenix-8000 for the Z8000 is scheduled for general release at the end of this year.

Microsoft, 10800 N. E. Eighth St., Suite 819, Bellevue, Wash. 98004. Phone (206) 455-8080 [385]

Report generator computes tables on 8080, 8085, Z80

The T/Maker system combines a fast, easy-to-use tabular report generator with word processing for the 8080, Z80, and 8085 processors. Using a 48-K-byte CP/M system and CBasic-2, it provides easy analysis and presentation of the numerical data and text copy used in financial modeling and report preparation. For word processing and report generation, it includes a full screen editor, while for computing tables, it has a visual two-dimensional syntax. Files can be inserted, appended, and sorted as well as created, loaded, and processed automatically. The T/Maker system, complete with documentation and reference card, is $275. Documentation alone is $25.

Lifeboat Associates, 1651 Third Ave., New York, N. Y. 10028. Phone (212) 860-0300 [384]

Cross assemblers run under UNIX system on PDP-11 series

A full line of microprocessor cross assemblers runs on the Digital Equipment Corp. PDP-11 series under Bell Laboratories' UNIX operating system. The line includes cross assemblers for the 8048, 8086, 8085, Z80, Z8000, 6809, 68000, 6502, and 9900 microprocessors. The cross assemblers are available in either relocatable or absolute versions, written in Macro-11 assembly language. UNIX versions of the Macro-11 assembler and linker are also

available. The assemblers feature upward compatibility with the DEC Macro-11 and VAX assemblers at the directive level.

Prices range from $2,000 for the 8085 cross assembler to $3,500 for the 8086 version. Delivery is one week after receipt of order.

System Kontakt Inc., 6 Preston Court, Bedford, Mass. 01730. Phone (617) 275-2333 [386]

Word-processing package includes keytops for terminal

The VTS/80 is a word-processing software package that operates on CP/M-compatible microcomputers. Designed for use by operators who have no previous computer or word-processing experience, the VTS/80 package includes a replacement set of keytops for installment on a dumb cathode-ray-tube terminal's keyboard. With the keytops, the keyboard will look like a dedicated word processor. The keytops are color-coded by function and have the commands engraved on the side.

In addition, the VTS/80 package includes a color-coded manual and a software diskette. Versions are now available on both 5- and 8-in. diskettes for any 8080, 8085, or Z80 microprocessor running under the CP/M operating system. The keytops can serve over 90% of commercially available terminals. A multi-user version of VTS/80 operating under MP/M will be available Nov. 1. The suggested retail price of the package is $549; it is available in English now and will be available in Dutch, French, German, and Spanish on Nov. 1.

National Microsoftware Producers Inc., 3169 Fillmore St., San Francisco, Calif. 94123. Phone (415) 346-7025 [387]

Software provides direct access to data files

A data-file access method named AIM (for associative index method) provides several capabilities that, according to the manufacturer, have been heretofore unavailable to data-processing users. Released with Datashare 6, the latest version of Datapoint Corp.'s Business Timesharing System, AIM is compatible with systems running under the Datashare 6 software with a minimum 120-K bytes of memory.

The software eliminates the need for index pointers, links, networks, and trees in data files by providing direct access to any or all parts of every record. AIM is a content-addressable file whose key is defined at the time of inquiry, not at the time the file is set up by the system designer. Disk space is conserved because the index file takes up only about 14% of the space occupied by the data file it indexes.

AIM software is available exclusively with Datashare 6 software and is covered by the standard Datashare 6 software licensing agreement.

Datapoint Corp., 9725 Datapoint Dr., San Antonio, Texas 78284 [388]

Networking software for HP 1000s includes HDLC

Distributed Systems/1000-IV, the fourth generation of networking software for the HP 1000 computer family, offers the High-level Data Link Control (HDLC) protocol, message accounting, dynamic re-routing, and remote peripheral assignment. It provides network support for all HP 1000 computers and their real-time executive operating systems, including the new L series. Application programs that run on DS/1000 will run unchanged on the new product.

The HDLC protocol is implemented on a family of intelligent interface cards that perform all the link-level processing needed.

An original license for the DS/1000-IV is $4,000; licenses for additional copies are $1,600 each. DS/1000 users will be upgraded without charge. The interface cards cost $1,400 to $2,000.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [389]

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In addition to providing functional equivalency and software compatibility with DEC, the quad size MDB DUP-11 and MLSI-DUPV-11 interfaces will accommodate BI-Sync and DDCMP in byte-control and SDLC, ADCCP and HDLC bit-oriented protocols, with programmable character lengths of one to eight bits for BOP and five to eight for BCP. This is performance flexibility never possible before. In addition, the MDB DUP boards feature complete error control including CRC-CCITT preset to O's or 1's, CRC-16 preset to O's or VRC odd or even. For Q-Bus users this hardware error checking saves a lot of computer time and memory over the software checking of other systems.

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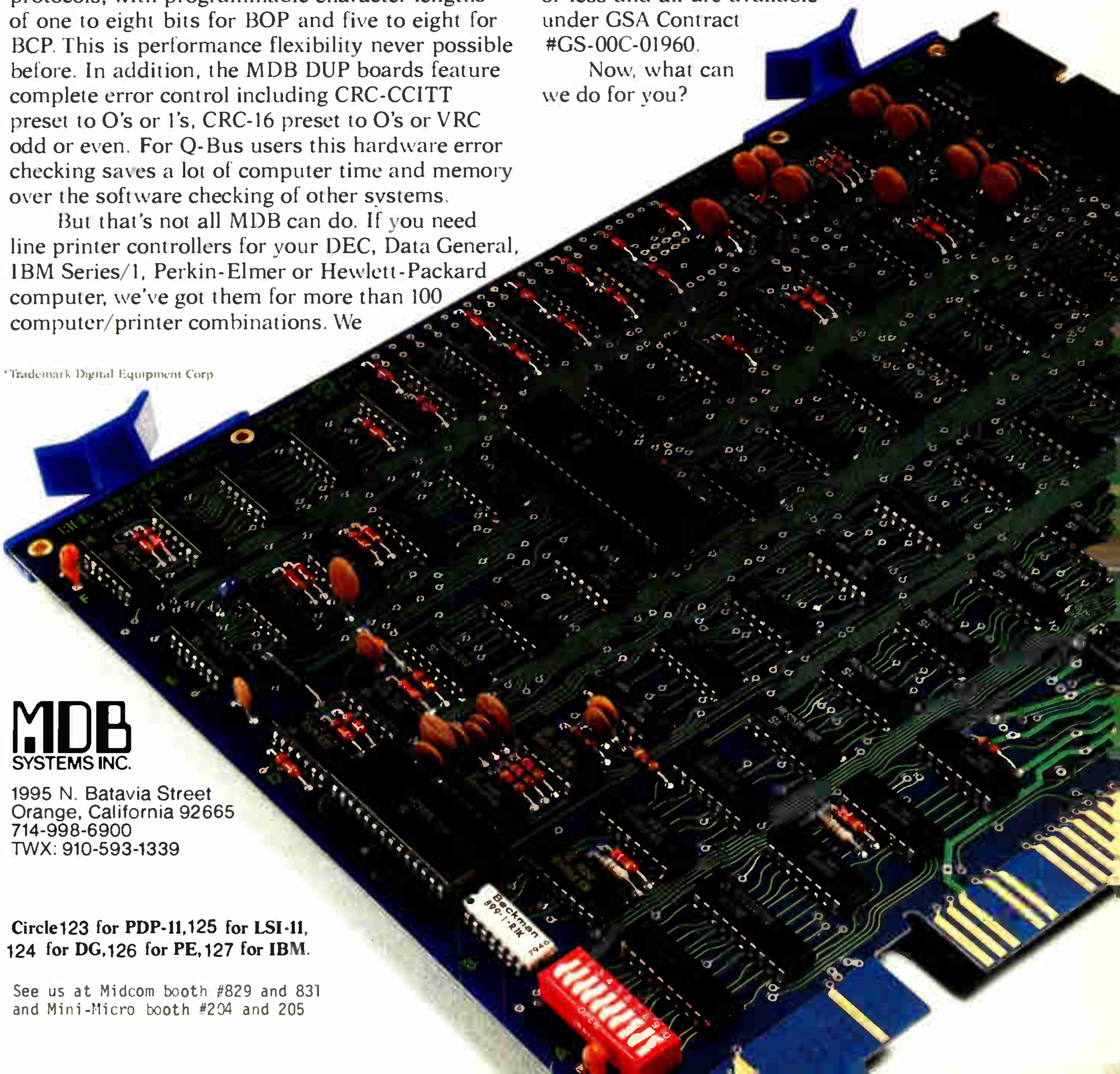

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Chip detects single- to triple-bit errors

Since the new breed of 64-K dynamic random-access memories are over five times more susceptible to alpha-particle–induced soft errors than are 16-K RAMs, Advanced Micro Devices Inc. is beginning to offer samples of a error detection and correction chip that **can correct all single-bit memory errors in a data word and detect all double-bit and even some triple-bit errors.** The bipolar Am2960 uses a modified Hamming code to boost memory reliability more than sixtyfold and detects errors in 25 ns, while correcting them typically in 40 ns. Expected to be available from the Sunnyvale, Calif., firm by the end of this year, the 2960 is flexible enough to handle word widths of from 8 to 64 bits.

Hard-disk tester scans in 40 or 60 seconds

Look for Media Test Specialists Inc., a new firm in San Jose, Calif., to introduce a hard-disk test system priced in the $100,000-to-$120,000 range, depending on options. The model 5814 is oriented toward production rather than engineering testing, **cutting test time to under 40 seconds in its fast-scan mode and 60 seconds in its normal-scan mode.** The system checks for extra bits, missing bits, modulation, and amplitudes. Mechanical adaptors allow the system to test either 14-, 8-, or 5.25-in. disks. Head positioning for track densities of up to 2,080 tracks/in. can be accommodated in 0.5-mil steps. This will enable the system to test disks using thin-film heads, as well as current disks.

Two companies find second sources

■ **International Microcircuits Inc., Santa Clara, Calif., has entered into an agreement with Supertex Inc.** for the Sunnyvale, Calif., firm to second-source IMI's two families of gate arrays, now totaling more than two dozen basic circuits. Included are a metal-gate complementary-MOS family with 50 to 550 cells per chip and a silicon-gate, oxide-isolated C-MOS family with a density of 200 to 2,000 cells per chip and a 30-MHz switching frequency.

■ **Silicon Systems Inc., Tustin, Calif., has signed a second-sourcing agreement with ITT North Electric Co.'s Microsystems division,** Deerfield Beach, Fla., for the latter to manufacture and market the SSI 201 monolithic dual-tone multifrequency receiver used in Touch-Tone telecommunications applications [*Electronics*, Feb. 15, 1979, p. 105].

Price cuts

■ In switching from its H-MOS I to H-MOS II high-performance process for its 16-bit 8086 microprocessor, **Intel Corp., Santa Clara, Calif.,** substantially increased its yield of higher-speed parts. As a result, last month's Wescon saw the introduction of the 8086-1, a 10-MHz version of the 8086 at $187.50, and now the price of its 8-MHz 8086-2 processor has dropped—from $200 to $118.75 in quantities of 100. The basic 5-MHz chip remains at $86.65 in the same quantities.

■ **National Semiconductor Corp., also of Santa Clara,** has slashed prices more than 40% on the four medium-sized programmable-array logic (PAL) devices it has been manufacturing under a licensing accord with Monolithic Memories Inc. The 100-piece price for the 16L8, 16R8, 16R6, and 16R4 goes from $55 to $32 each, with further cuts expected through 1981.

Career outlook

On the changing hybrid. A special issue of the Institute of Electrical and Electronics Engineer's Components, Hybrid and Manufacturing Technology Transactions is scheduled for publication next September. This issue will focus on recent developments in the materials, design, and application of hybrid microelectronics. The use of nonprecious metals, new substrate materials, and new techniques to build lower-cost circuits are all growing interests in the hybrid field. The IEEE is looking for papers on these subjects, as well as in the areas of interconnection techniques, device and wire bonding, reliability, automation and computer-aided design, adhesives for fabrication, thermal design, characterization, and device screening.

Abstracts are due by Dec. 1, with the final papers to be submitted by Feb. 1, 1981. The associate editor for this issue is Subash Khadpe, at Bell Laboratories, 555 Union Blvd., Allentown, Pa. 18103; the guest editor is Gerald Lorenz, TRW Inc., 401 N. Broad St., Philadelphia, Pa. 19040. Contact either one for more information.

Reliable engineering. Among the topics to be covered at the 18th annual Reliability Engineering and Management Institute at the University of Arizona, Nov. 10–14, are reliability engineering theory and practice, life-cycle costing, and product liability. The program is being given jointly by the university's College of Engineering and Honeywell Information Systems, Large Information Systems division, Phoenix, Ariz. The cost of the program is $575, and three continuing education credits will be given for attending. For more information, write to Dimitri Kececioglu at the Aerospace and Mechanical Engineering Department, University of Arizona, Building 16, Tucson, Ariz. 85721, or phone him at (602) 626-2495.

Signal analysis, digitally. Covering modern digital techniques of signal analysis with emphasis on applications to vibration and acoustics problems, "Applied Time Series Analysis" is scheduled to be presented in Cincinnati, Ohio, Nov. 17–21. A GenRad Inc. signal analysis system will be used to provide live demonstrations of specific techniques for six laboratory sessions. Sponsored by Time Series Associates in cooperation with Genrad, the course will be given by Robert K. Otnes of TSA and Loren Enochson of Genrad. The course is priced at $750, including text, materials, and lunches. Contact Robert K. Otnes, Time Series Associates, 2160 Middlefield Rd., Palo Alto, Calif. 94301 or phone him at (415) 324-1821.

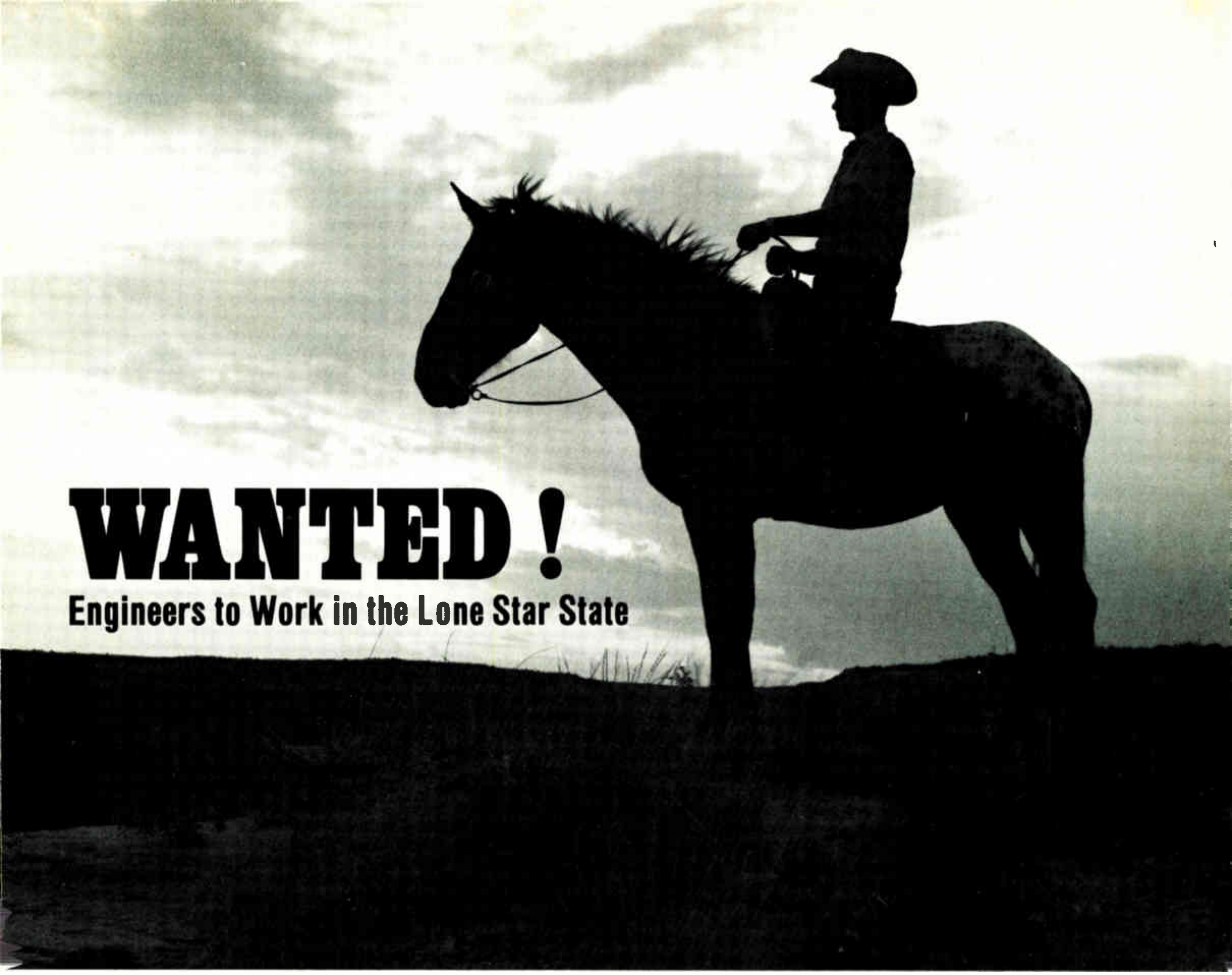
Electronics seminars. *Electronics* is sponsoring a series of two- and three-day seminars on a wide variety of topics. The first, which will be held in New York starting Nov. 10, is entitled "Applying Single-Chip Microcomputers."

Other seminars in the series, all of which will first be given in New York, are: "Microelectronics Interconnection and Packaging" (also starting on Nov. 10), "Quality Assurance for Electronics Manufacturers (Dec. 11), and "Pascal" (Dec. 15). A fifth, "Concepts of Digital Electronics," will begin on Jan. 28. The seminars will also be given in San Francisco, Fort Lauderdale, Boston, Dallas, and Chicago.

"Applying Single-Chip Microcomputers" is priced at $445. For more information, write to Pam Richards, McGraw-Hill Seminar Center, 305 Madison Ave., Room 3112, New York, N.Y. 10017, or call her at (212) 687-0243.

Fingertip pinouts. Available on floppy disk for the Apple II or Apple II+ computer, Chips is a software program designed to ease the task of locating pinouts and truth tables for over 100 TTL and complementary-MOS integrated circuits. New pinouts or truth tables are easily added to the list. Available for $49.95, the software program may be ordered from Lamar Instruments, 2107 Artesia Blvd., Redondo Beach, Calif. 90278, or by calling Maura Robertson at (213) 374-1673.

-Pamela Hamilton



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Engineers to Work in the Lone Star State

Deep in the heart of Texas there is a new and different sound. It is the energetic beat of a growing and diversified economy powered by the energy boom. To sustain this boom, business, industry, and government in the Lone Star State are avidly seeking engineers at all steps of the career ladder in avionics/aerospace, electrical/electronics, and computer science and data processing.

There is a soaring demand for professionals in these high technology fields, according to William P. Clements, Jr., Governor of Texas. He says, "Engineers are an invaluable component of the professional force in rapidly growing, industrialized Texas. Many areas of our economy draw on their creative talents, skills, imagination, and dedication. We now have a shortage of engineers that is likely to continue.

"We must support better quality education at an increasingly higher level of competency. Both undergraduate and graduate programs must be strengthened to assure that highly trained engineers are available to meet the demands of complex technology. Providing adequate laboratory equipment in our universities presents something of a problem because of rapid advances in technology."

The hot spots for the high technology professionals are clustered in the Fort Worth-Dallas area, Austin, San Antonio, and Houston. These cities are on the perimeter of what is called the Texas Triangle, with Fort Worth-Dallas at the northern end, San Antonio at the point of the western leg, and Houston located on the eastern leg. Each leg of this imaginary triangle is approximately 200 miles long.

In this triangle resides approximately four out of every five people in the Lone Star State. Because of its urban and industrial growth, Texas is attracting people from other parts of the country to live and work.

Engineers who come to Texas and want to continue their education for a master's or doctor's degree can attend some of the finest schools in the country. For example, Baylor, Rice, Southern Methodist, Texas A&M, the University of Houston, and the University of Texas are all convenient to residents of the triangle area.

Texas A&M, with the largest single engineering campus in the country, has more than 10,000 students enrolled in its engineering courses. This total includes 1,621 women engineering students, more than any other engineering school in the country.

Texas A&M is affiliated with the Engineering Experiment Station, one of its research arms. It is a state agency that is designed to meet the engineering needs of Texas and to test new concepts. The Engineering Experiment Station is funded by both government and private industry. It conducts approximately $20 million of applied research annually on a wide variety of subjects and illustrates the Lone Star State's commitment to the profession of engineering.

Both industry and government are working to solve the engineer shortage in this burgeoning industrial state. The 1970s were a decade of growth for Texas, and it is continuing in the 1980s. The state's economic boom is attracting EE engineers from all over the country, including California.

The aerospace and electronic industries have contributed to industry's growing strength. New manufacturing facilities are springing up. One Texas-based company recently came up with the latest development in silicone chip technology that will help the industry in its fierce competition with the Japanese.

Texas is also the state that has one of the most active chapters of the Society of Women Engineers in the country.

In addition to the advantages Texas offers, one must also consider the lifestyle residents enjoy. For example, the cost of living in Texas is one of the lowest in the country. Housing prices are also reasonable. As one resident recently boasted, "You can buy a darn good house in a fine community for $50,000." This is much less costly than many other areas in the country.

Another advantage is that there is no state income tax in Texas. And the state's unemployment rate, as reported in *The Wall Street Journal* last month, is 5.5%, more than two percentage points below the national average.

The climate is another attraction. The state enjoys year-round sunshine, with the average annual temperature in the lower Rio Grande Valley a pleasant 73°F. Parts of Texas can get hot, however, during the summer months.

Texas is also a land of contrasts. Its rugged desert in the western part of the state is rimmed by mountains with more than 90 peaks that reach more than a mile into the sky.

In addition, the Lone Star State has more than 23.4 million acres of forest and woodland and approximately 80 scenic state parks and recreational facilities that residents enjoy.

On its southern border, Texas meets both Mexico and the Gulf of Mexico with its 640 magnificent miles of shoreline that are dotted with a myriad of beaches that encourage swimming. The Gulf of Mexico is noted for providing some of the world's best fishing.

Inland waters comprise a total of 6,300 miles of lakes and streams that are surpassed in numbers only by the state of Alaska.

The 276,000 square miles that contain our second largest state, with approximately 7½% of our country's total land area, is also noted for its hunting and fishing. Texas is rightfully famous for its native and exotic wildlife, waterfowl and upland game birds.

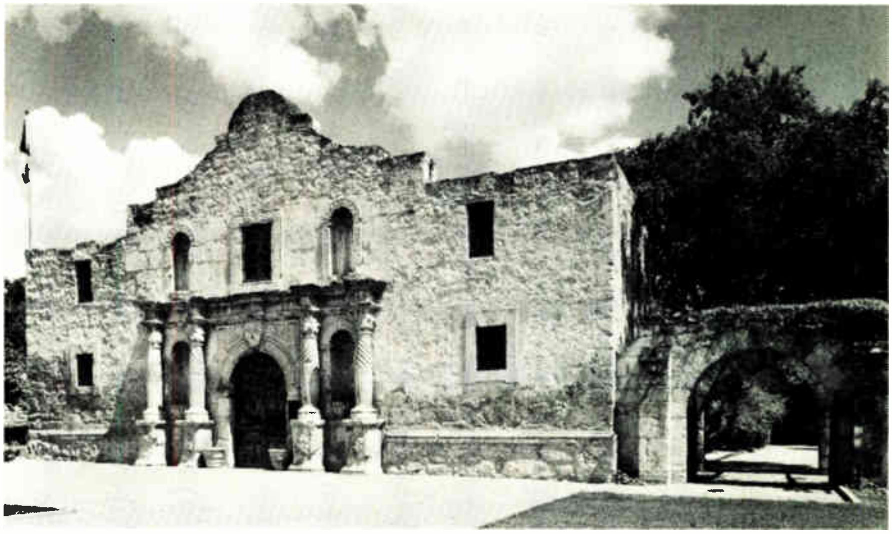
The welcome mat is out for engineers in Texas. Governor William P. Clements, Jr., says there is a shortage of engineers in the Lone Star State.

The Lone Star State is also rich in history. It has nearly 300 historical museums scattered throughout its territory. It is the home of the Alamo and frontier forts, and retains the charm of Old Mexico. It is also the home of the Astrodome and the Lyndon B. Johnson Space Center in Houston. It is the land of the cowboy and the rodeo.

Engineers who enjoy spectator sports have a wide choice of professional teams to root for in Texas. For example, the Dallas Cowboys and Houston Oilers supply the thrills for football fans. Baseball enthusiasts have the Houston Astros and the Texas Rangers to argue about. The Houston Rockets and the San Antonio Spurs cater to the needs of professional basketball fans. This fall a new basketball team, the Dallas Mavericks, are coming to town. Last, but not least, the Dallas Tornado soccer team completes the impressive roster of big-time professional sports in Texas.

The third most populous state in the union is throbbing with a frontier-like enthusiasm. Its economy is as hot as J.R. Ewing in a Dallas deal, and offers engineers the opportunity to cash in on the high technology discipline of their choice.

The welcome mat is out for engineers in Texas. If you are looking for a long and lucrative career in Texas as an engineer, turn to the following Career Opportunities section and meet some of the companies that would like to talk to you. One of them may make an offer you can't refuse. —John Brand



Texas is the home of the Alamo, one of the many historical sites in the state.

HISTORIC SAN ANTONIO IS THE SETTING FOR OUR HISTORY-MAKING RESEARCH

Southwest Research Institute is 471 acres of laboratories, test facilities, offices and workshops located in historic San Antonio, Texas. Our campus has eleven operating divisions working in a multidisciplinary approach on a variety of applied research projects. Our staff of 1800 includes internationally recognized scientists, engineers and support personnel.

DESIGN AND DEVELOPMENT OF SPECIAL PURPOSE COMMUNICATIONS SYSTEMS

The Data Systems Department is seeking a BS or MS EE with five years of diversified experience in defining, designing and developing communications networks, structures, systems, and equipment including design of concentrators and multiplexers .

ANALOG AND DIGITAL INSTRUMENTATION DESIGN FOR SATELLITE AND SOUNDING ROCKETS APPLICATIONS

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RADIO FREQUENCY PROCESS CONTROL

The Electromagnetics Division is seeking an inexperienced BS or MS EE for high level and assembly level language programming on various mini/micro systems used in radio frequency process control functions. Applicants should have an interest and aptitude in electromagnetics/radio science and be willing to travel to U.S. military locations outside the U.S.

ANALOG SIGNAL AND DIGITAL CONTROL CIRCUIT DESIGN

The QA Division is seeking a BSEE to prepare design specifications and perform detailed circuit design for both analog signal and digital control circuits. Applicants should have experience in low frequency RF work, radar or sonar signal processing and software related tasks as well as circuit design of prototype instruments.

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The QA Division is seeking a BS, MS or PhD EE or Physics major to design communication subsystems with error coding and digital filtering and digital display systems. Three or more years experience in design of prototype digital circuits is required.

VIDEO SYSTEMS DESIGN

A BS or MS EE is needed for design of video systems including automatic gain control, filtering, and video display systems. Minimum of two years experience in design of video systems having band widths up to 20 MHz required.

As our own operations have expanded, we've also been pleased to watch our community grow to be the nation's 10th largest city. Boasting near-perfect weather and a low cost of living, San Antonio has proven to be a delightful place to live as well as to work.

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THE ALAMO: Photo courtesy of the San Antonio Convention and Visitors Bureau.

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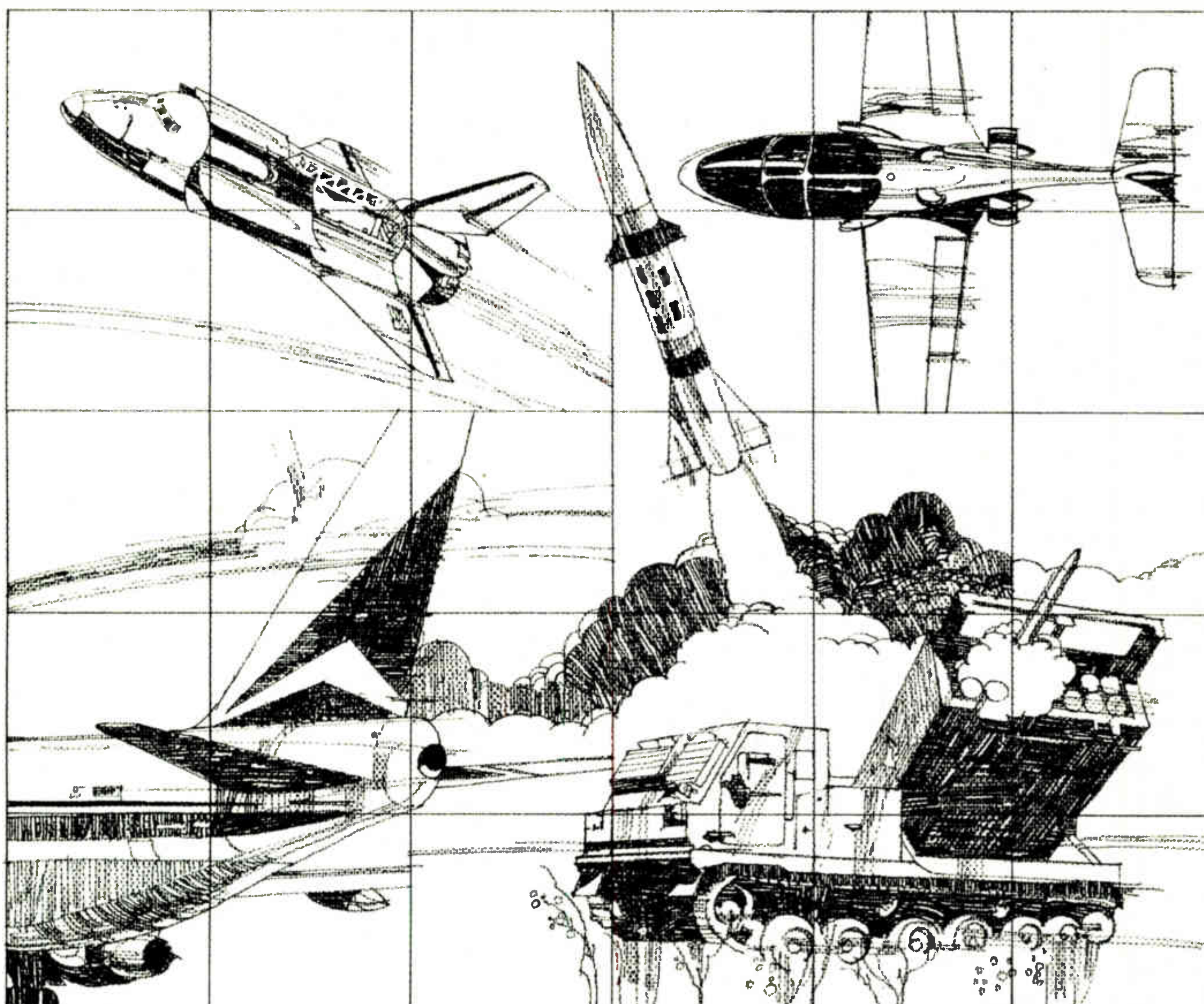

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For consideration, please call Gary Hecht at (800) 547-1164, or send resume to Gary Hecht, MS 55-033, Tektronix, Inc., P.O. Box 500, B-4, Beaverton, Oregon 97077.

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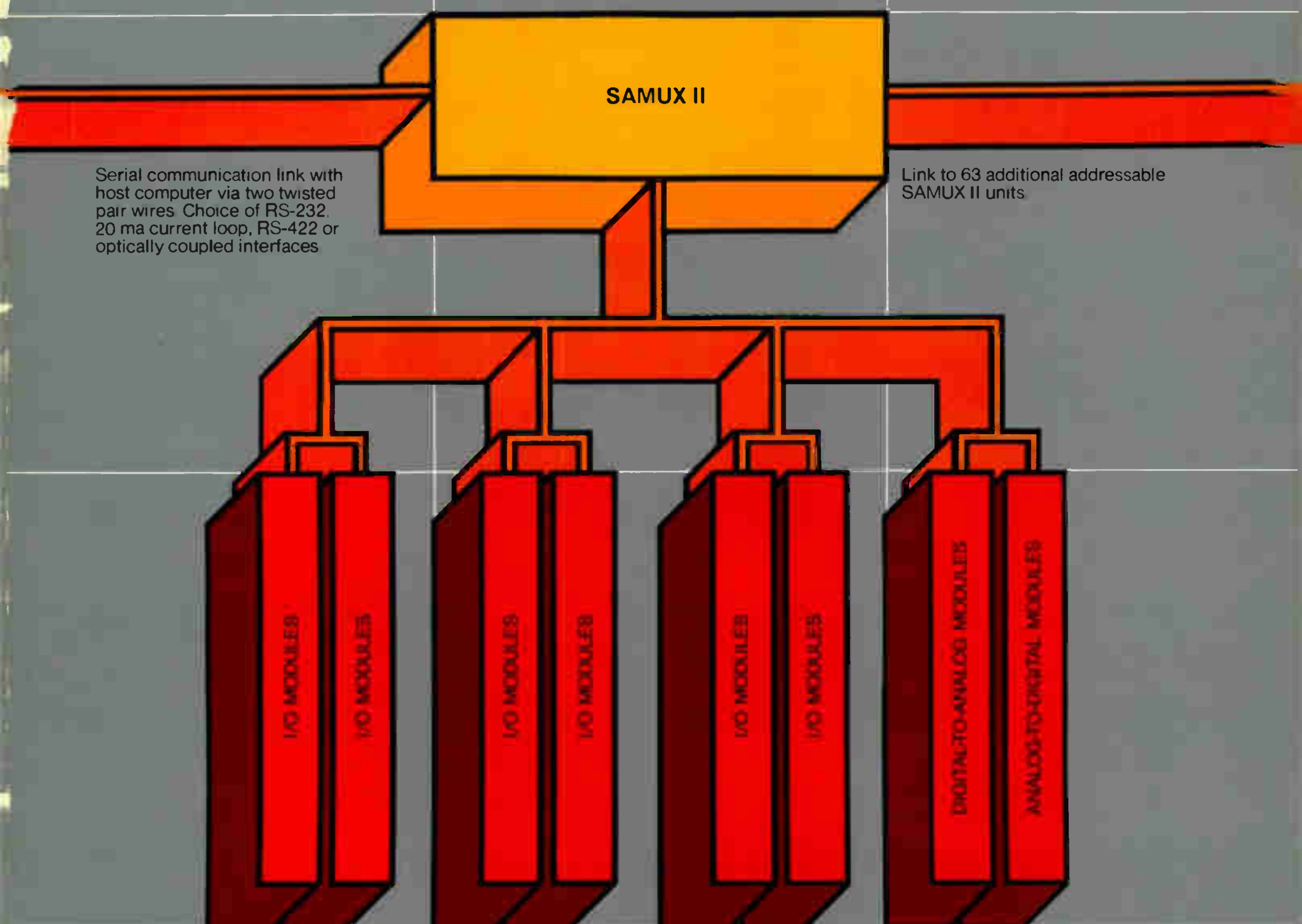

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