OCTOBER 9, 1980

**STANDARD TESTERS FOR FIBER OPTICS AWAIT MARKET SURGE/91**

Large-scale integration lightens the rf design load/ 148

Fiber-optic receivers start to integrate/ 155

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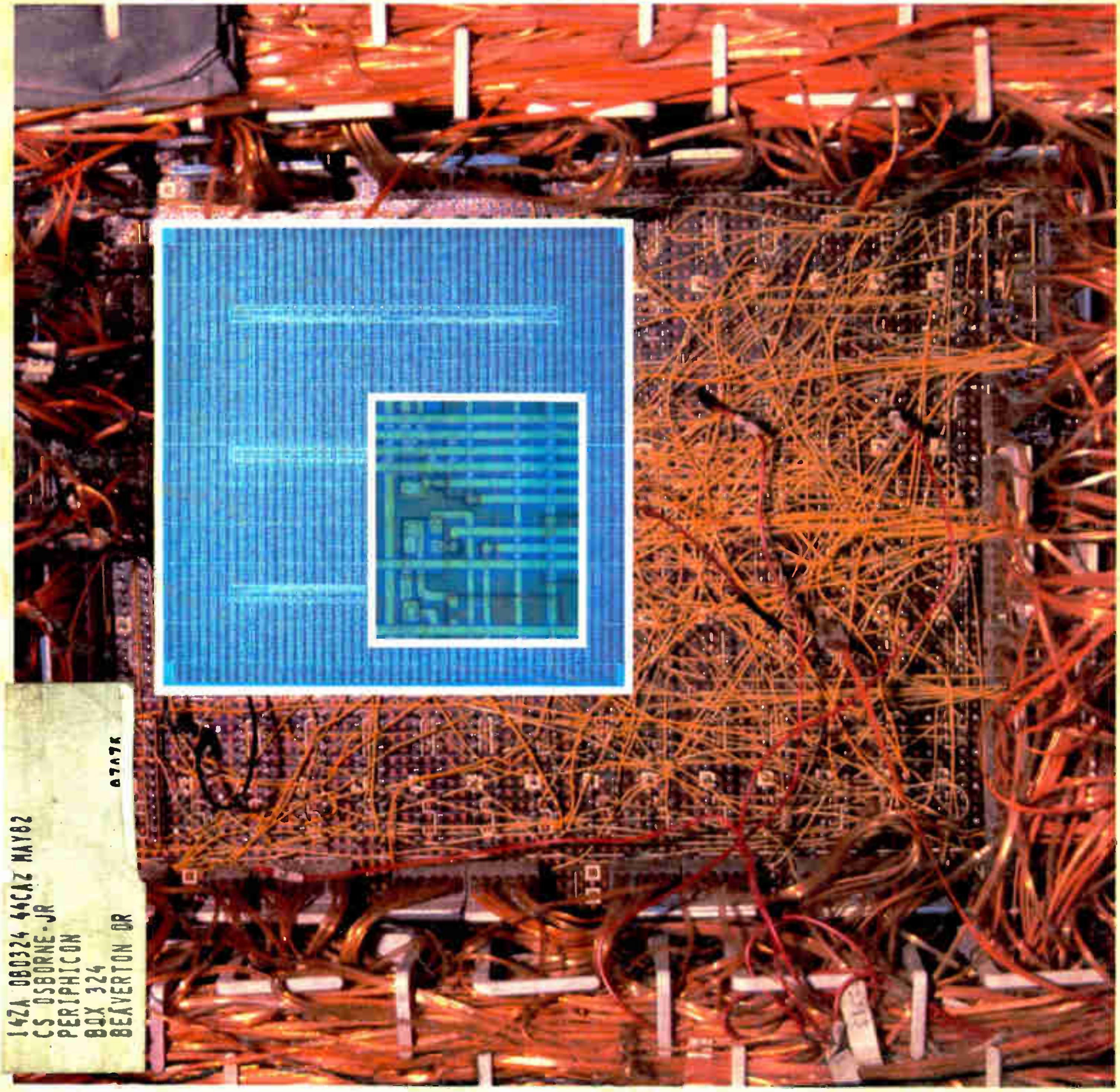
## SHRINKING A MAINFRAME CPU INTO SILICON



6. Circuit Board Testing Update/No. 6 in a series from Hewlett-Packard.

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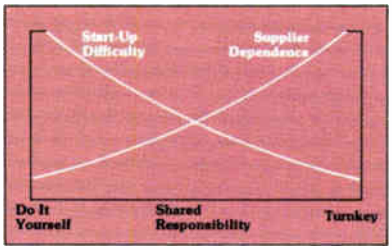


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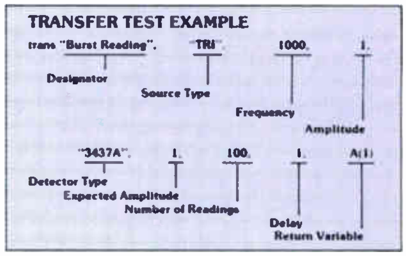


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090/46

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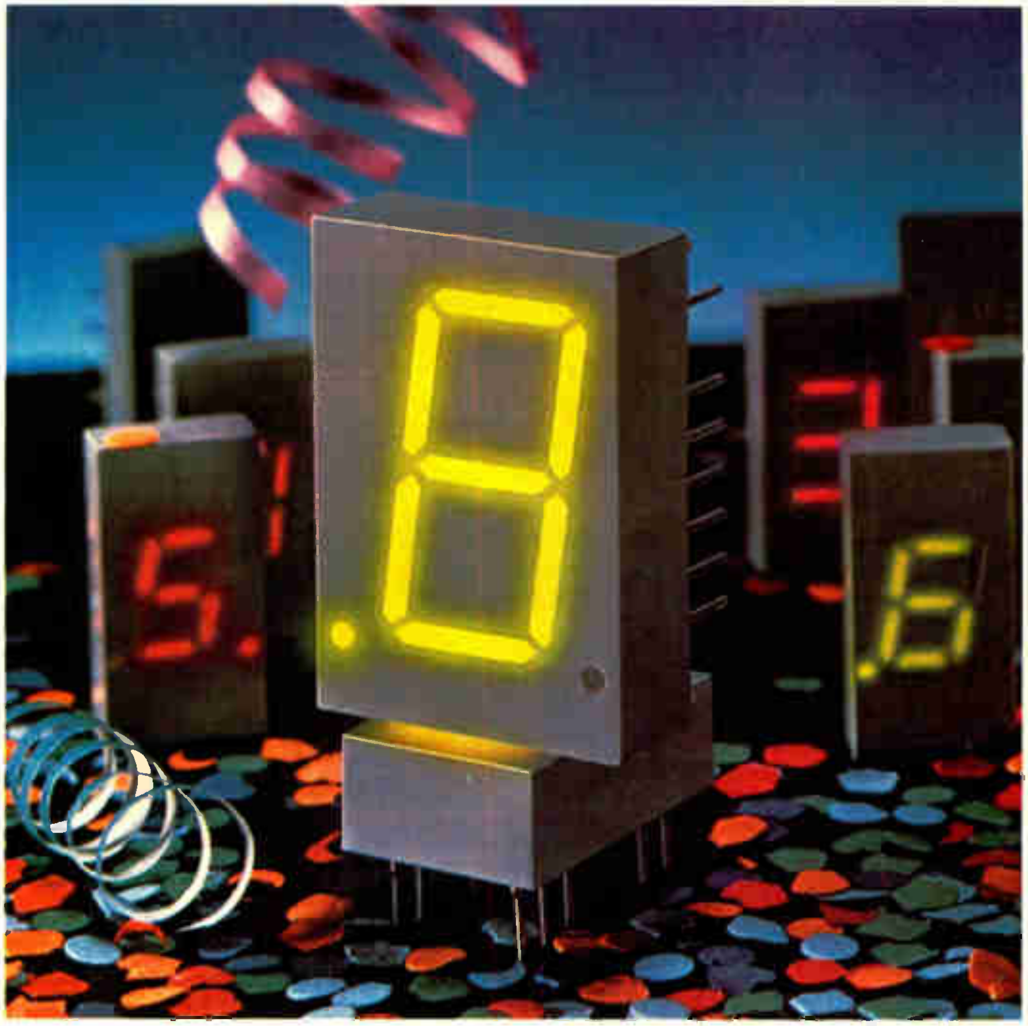

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# Electronics

**The International Magazine of Electronic Technology**

**Vol. 53, No. 22 • October 9, 1980**



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# Highlights

## Computer-aided design reduces mainframe CPU to a chip, 139

Realizing very large-scale integration is no sure thing. To find out if its automatic gate-placement and -wiring system is up to the task, IBM went about fitting the central processing unit of the System/370 mainframe computer on a single chip. Three articles reveal, respectively, how the architecture was implemented (p. 140), how the gates and wiring were placed (p. 144), and how long path delays were shortened (p. 146).

The cover design is by Art Director Fred Sklenar, the photographs by courtesy of IBM Corp.

## Market for fiber-optic measurement instruments is aborning, 91

With agreement on how to characterize fiber-optic links drawing near, instruments to specify the link's components—fibers, sources (transmitters), and detectors (receivers)—will soon be forthcoming. One indication that fiber-optic measurement is a field whose time is approaching is the Symposium on Optical Fiber Measurements. The first meeting devoted to the topic, it is being organized by the National Bureau of Standards in cooperation with the Optical Society of America and the Institute of Electrical and Electronics Engineers.

## Enlarging PLL chips' functions eases synthesizer design, 148

By putting more phase-locked-loop control functions on chip, a complementary-MOS family offers designers noteworthy performance while cutting power consumption, cost, and space, as well as design time. The chips each contain one or two programmable divide-by-N counters; for those with two, dual-modulus prescaling can be used.

## Integrated fiber-optic receivers, too, are in the offing, 155

Fiber-optic communications has emerged as a major technology, but slower to develop have been the monolithic optical receivers needed to make fiber-optic systems a commercial reality on a large scale. A few hybrid products are available, much work is being done around the world, and within five years many receiver components will be made in chip form. This special report looks at what is out and what is coming.

## One-chip computer enlists as multiprocessor, 172

Ready to take on multiprocessing assignments is a series of 8-bit single-chip computers that include the control logic required to resolve the inherent problem of bus contention. What's more, special 16-bit instructions suit the parts for word-processing chores as well.

## And in the next issue . . .

*Electronics'* annual technology update . . . the 1980 achievement award.


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# Publisher's letter

**How far can** computer-aided design, testing, and wiring procedures for gate arrays be pushed? Is it possible to put the 5,000-plus circuits of an IBM System/370 data flow on a chip? In 1978 an engineering team organized informally at International Business Machine Corp.'s Data Systems division in East Fishkill, N. Y., set out on an experiment to answer those questions.

Fascinated by the challenge, the group, representing diverse backgrounds and talents, pushed gate array design to new levels of density and complexity. It took just nine months to encode the 370 processor's logic design, automatically place and wire the logic gates, and generate verified test patterns.

A description of this project appears in the three-article cover series from IBM starting on page 139. The experiment more or less coalesced around author Claud Davis, senior engineering manager for advanced systems at East Fishkill.

As the systems expert on the team, 56-year-old Davis brought some 31 years' experience in design work on some of IBM's large computers, including the System/360. In a sense, he personifies the progress of computational power from large machines filling a room to a slice of silicon. Thinking back, Davis observes, "It's strange to realize that we can build on one chip more computing power than any machine we could make in the mid-'50s."

Equally challenged by the audacity of the project was Allan Dansky, advisory engineer in advanced applications. At 42, Dansky remembers designing chips with five circuits for the 370/145. "We've increased bipolar circuit capacity a thousandfold in 13 years," he notes. "Without computer-aided design, it could not have been done."

To Michael Feuer (pronounced "foyer"), who was responsible for the automatic placement and wiring, the project proved that the gate array has a vital place in very large-scale integration. Thirty-eight-year-old Feuer, senior engineering manager for VLSI physical design, points out that there is still a great deal more potential in the gate array.

Everyone on the project was impressed by the team work and dedication involved. In part it was the fact that the IBM 370 was the benchmark.

"No question about it, we were self-motivated. It was something special," Feuer recalls.

---

**For fiber-optic** communications to spread its hair-thin web over the world, it will become necessary to integrate the components in the systems. Of the major parts that make up a fiber-optic system, the receiver is a natural for integration.

But there are real problems to overcome. With this thought in mind, communications editor Harvey Hindin prepared the special report on fiber-optic receivers (p. 155).

Basically, the way to make p-i-n diodes for these systems is incompatible with silicon technology as we know it today, Harvey points out. Moreover, the avalanche photodiode, an alternative, is even harder to integrate and requires several hundred volts to operate. "Nevertheless," he observes, "all concerned agree that present hybrid receivers will be replaced by ones with much greater degrees of integration over the next few years."

This trend underscores the progress of fiber-optic communications from interesting concept to trial applications to operating systems. Development has been especially animated in Western Europe and Japan, so that the information from our overseas bureaus was particularly important for this report.

Considering the interest in integrating receivers, Harvey was surprised to note that, with a few exceptions, the large semiconductor houses are not addressing this market. That situation will probably change as the dollar's value begins to grow, he predicts.

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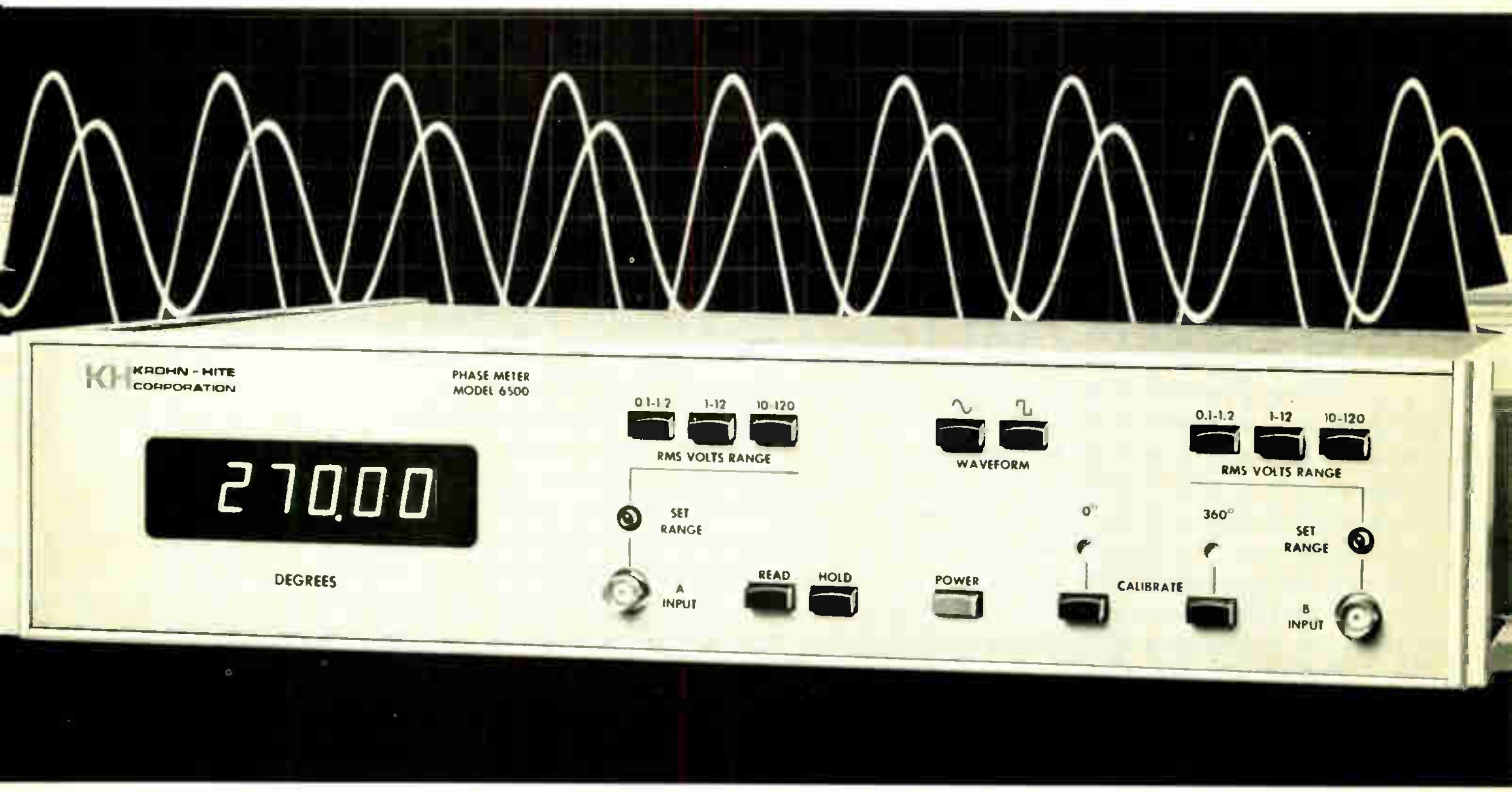


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Circle 7 on reader service card

## Readers' comments

### Not this engineer

**To the Editor:** I write in respose to Andrew Grove's "Finding tomorrow's engineers today" [Aug. 14, p. 32].

I do not intend to proselytize for the engineering profession for these reasons:

(1) Predictions of demand are notoriously unreliable. In July 1962, the Engineering Manpower Commission stated that the supply of engineering graduates for each of the next 10 years would be at least 11,000 short of the most conservative estimates of need. In February 1971, an estimated 10,000 engineers, scientists, and supporting professional workers were out of work in Massachusetts alone! Senator Brooke even announced a plan to retrain 2,000 engineers and scientists for work in urban programs.

(2) For better or worse, a person's place in this society depends as much on power as on ability. Electrical engineers have no power. We have virtually no unions and our "professional organization" is controlled by the industries that employ us. Consequently, engineering labor is a commodity. Although demand is now high, the equilibrium total income for an engineer (as for anyone whose labor is a commodity) is equal to the subsistence income plus the cost of his or her education.

George Caplan
Newton, Mass.

### Corrections

*In "Transformerless inverter cuts photovoltaic system losses" (Aug. 14), total harmonic content should be slightly over 11%, instead of slightly over 5% as given on page 124. On page 126 the 256-bit read-only memory in the figure should have a 5-bit, not an 8-bit, address line.*

*The price for the initial offering in Tektronix 8500 series (Sept. 25, p. 33) should be under $15,000.*

*Some numbers were jumbled in "Intel and NEC heat up the race in 64-K RAMs" (Sept. 25, p. 39). Intel Corp.'s 64-K RAM is the 2164, not the 4164. Mostek Corp's device is the MK4164, rather than the 4146.*

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Now Advanced Micro Devices has a bipolar dynamic memory controller for use with 16K and 64K RAMs. It's easy to use. It's flexible. And it takes care of all your $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and address problems on one chip.

The Am2964B replaces about a dozen high-speed, high-power Schottky parts. And it not only does the job faster, it uses less power.

But what about the interface to the RAM? We thought you'd never ask.

## Meet our Am2965/66 RAM drivers.

The faster you drive your memory, the faster your system. And that's where our new Am2965/66 come in. Together with our Am2964B, they achieve maximum performance and completely eliminate undershoot.

The speed is specified up to 500 pf. Min's and max's, too.

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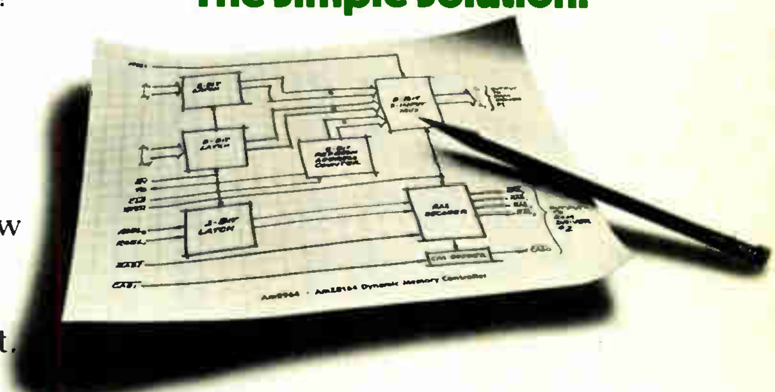
The Am2964B and Am2965/66 are the newest members of AMD's dynamic memory support family — the family that makes implementing dynamic RAM systems easier, cheaper, simpler, faster. Like all our parts, they're MIL-STD-883 for free, the highest quality parts you can buy.

Don't let driving your memory drive you up a wall. Send for all the facts on AMD's Dynamic Memory Support Family.

## Bipolar LSI: The Simple Solution.



# Advanced Micro Devices

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## News update

■ The MIT microchannel spatial light modulator will start moving towards commercialization with the signing of a licensing agreement between the Massachusetts Institute of Technology and Japan-based Hamamatsu Corp. in the next few months. Hamamatsu, which has built four MSLM units for development work at MIT, plans to approach manufacturers of scientific instrumentation with evaluation samples in about two years, says J. Ralph Eno, executive vice president of U. S. operations in Middlesex, N. J.

"Like the laser in its infancy, the MSLM is an answer looking for the right questions," says Eno. MIT researchers in Cambridge, Mass., developed the unit to speed data flow into and out of optical computers [*Electronics*, June 7, 1979, p. 41], but now foresee a number of other uses.

The MSLM is a kind of phase modulator, converting incoming images into coherent light images. Incoming light strikes a photocathode, which gives up electrons. Amplified by a microchannel plate and accelerated by an accelerator planar grid, the electrons charge an electro-optic plate, changing its refractive index. When a coherent laser beam illuminates the plate, these refractive changes induce phase changes in the laser's wave front, creating a visible readout of the original image.

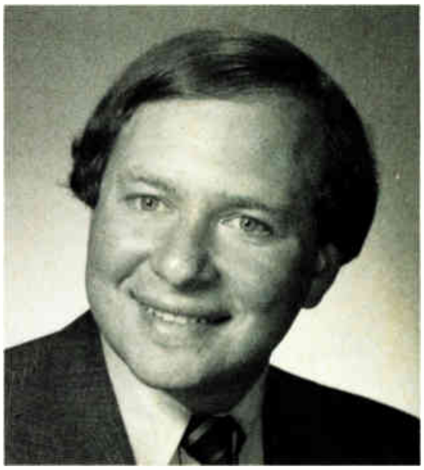
**Smart sensor.** Its real-time, image-processing abilities suggest smart-sensor applications, says team leader Cardinal Warde, assistant professor of electrical engineering and computer science. It may also make possible reception in low visibility in wireless optical communications systems, he adds.

The MIT team has made the MSLM perform a variety of sophisticated image-processing functions, says Warde. These include contrast reversal and digitization of images.

Improved materials and design will increase the MSLM's processing speed—currently 20 hertz for full modulation—and will push its spectral sensitivity further into the near-infrared, Warde believes. He reports image-storage times of up to two months. **-Linda Lowe**

# People

## Raphael wants to make modem design easier



**Think analog.** Cermetek's Raphael wants digital designers to think beyond RS-232-C.

"Two areas that are seeing the most technology innovations are microprocessors, and telecommunications and data communications. The second area is a consequence of the first," believes Howard A. Raphael. That helps explain why the former group director of microprocessor operations at National Semiconductor Corp. recently joined Cermetek Microelectronics Inc., the Sunnyvale, Calif., hybrid circuits manufacturer, as president.

The 34-year-old Raphael expects that as more equipment incorporates microprocessors, making them more intelligent and decentralized, "there will be an increasing need for data-communications capability." What's more, he continues, "the most widely available vehicle for data communications is the telephone." Thus it is clear why Raphael is excited about his new role at Cermetek, where he intends to focus the firm's hybrid microcircuits technology on supplying equipment designers with modem chips and modules that perform complete modem functions in the low-speed (300-to-1,200-bits-per-second) Bell-compatible market.

"We are looking to put modem design capability into the hands of first-time modem designers—that is, microprocessor, digital, and telecommunications engineers," states Raphael. By taking advantage of such modem modules and standard leased lines, "much equipment can be linked into a hassle-free network."

Raphael hopes that by offering components implementing the RS-232-C serial interface, among others, Cermetek not only will reduce systems cost but also, he says, "get digital designers to think beyond RS-232-C. Most just haven't dealt with analog functions before. Thus, by integrating those functions into our modem module—a digital product—we make them invisible to the digital designer."

By capitalizing on the microprocessor's acceptance and breaking new ground in other areas, Raphael expects Cermetek's volume (currently estimated at about $5 million) to grow an average of 50% annually over the next five years.

A native of New York City, Raphael holds a bachelor's degree in electrical engineering from the Rochester (N. Y.) Institute of Technology. Upon graduating in 1969, he joined Singer Business Machines Co. as an associate engineer and left five years later as its manager of process development. Prior to joining National Semiconductor in 1977, he was manager of low-end microcomputers at Intel Corp.

## Bumb sees backup memory as key to disk growth

Few would dispute that the magnetic storage media market—disks, tape, cartridges, and the like—has expanded at a dazzling 30% to 40% annual clip for several years—but can it continue? In the opinion of a 28-year veteran of the business, Frank C. Bumb, "it's still one of the most exciting growth areas, and there's a lot of gold to be mined."

Bumb stepped in as president this summer at Kennedy Co., a Monrovia, Calif., firm whose products pretty well cover the field. He takes over operating responsibility from founder Charles J. Kennedy, who remains as chairman. Acquired by Allegheny Ludlum Industries Inc. of Pittsburgh

## People

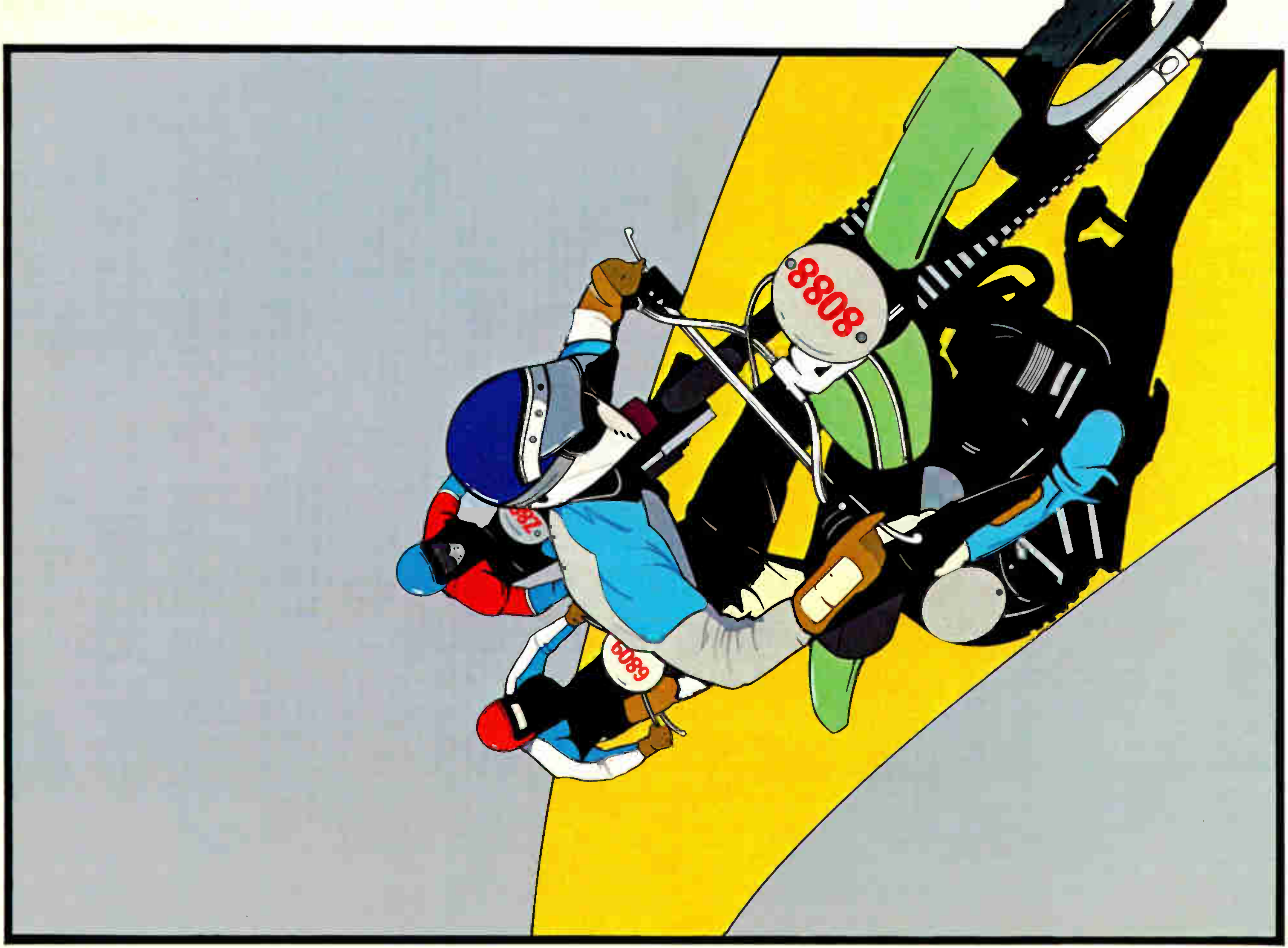
**Still digging.** Frank Bumb says there is much gold to mine in magnetic media hills.

in 1979, the company this year should see its sales approach $45 million.

Spurring such a pace is, of course, the ravenous demand for microcomputer memory. In the hottest market segment, Winchester drives, Bumb notes that "disk suppliers can't service the market today." Projected disk drive sales by independent manufacturers for 1981, of units having up to a 200-megabyte capacity, are nearly $185 million. "And this product didn't exist five years ago."

But disks are only part of it, since a clear-cut solution to the so-called backup question is still to be found. Disks must have a separate backup memory to take over in case of failure, "but the problem is a matter of price and access speed," explains the Kennedy president. The backup should not be as expensive as the disk, but it must be reliable and fairly fast. Kennedy's approach is to offer a single package, with either its 14- or 8-inch Winchester drive backed by a model 6809 tape "streamer" transport of its own or a model 640 cartridge drive. Bumb says Kennedy is the only firm selling its own package of disk drive and backup.

A graduate of the California Institute of Technology in adjacent Pasadena, Bumb held his previous job in that town as well, where he was president and general manager of Bell & Howell Co.'s Tape Products division. □


8808

# 8-Bit Champion

## In price-performance, look to Intel's powerful iAPX 88 microprocessor to leave the pack behind. Both now and down the road.

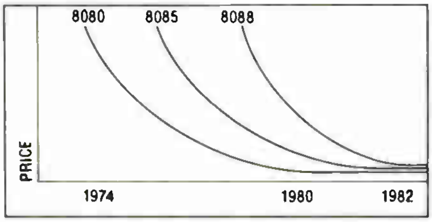
In price-performance races, the iAPX 88 is the one to beat. It's two times faster than the Z-80A and the 6809. And recent benchmark tests show that the iAPX 88, with its 8088 CPU, consistently outperforms its closest competitors in memory efficiency, ease of programming and throughput—by as much as 4 to 1. This is especially important in high-performance tasks such as block moves, character searches, word shifts, and 16-bit multiplies. All critical for applications like word processing, terminal control, scientific instrumentation and industrial control.

And because it's the only 8-bit microprocessor that addresses up to 1 million bytes of memory, the 8088 can take on large programs. Without having to slow down due to overlays or memory bank switching, like other 8-bit processors.

**Tough price competitor**

In price competition with other 8-bit microprocessors, the iAPX 88 has become the front runner.

You save dramatically on

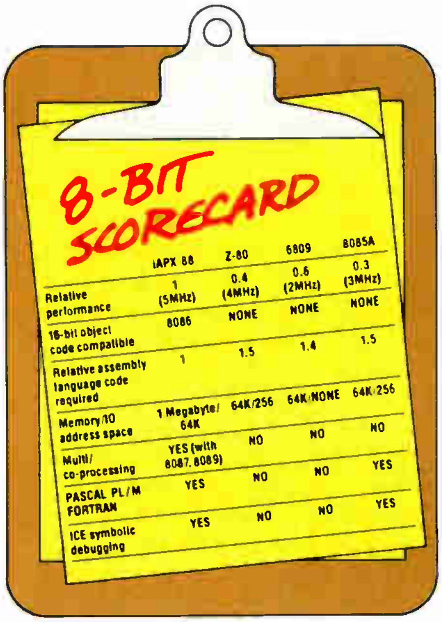



8-Bit Microprocessor Price Trends

memory chips, too. The iAPX 88 takes—on the average—30% less memory than competitors for the same programs. Then too, it allows you to use lower cost memory to get the same throughput as competitors. With a 5MHz 8088, you can use our 450ns memories and still outperform a 4MHz Z-80 requiring 250ns chips. Depending on the application, your cost savings here can be substantial.

**No contest now with new Intel software**

To unleash the new power that the iAPX 88 puts in your hands, it takes more powerful software—




| | iAPX 88 | Z-80 | 6809 | 8085A |
|---|---|---|---|---|
| Relative performance | 1 (5MHz) | 0.4 (4MHz) | 0.6 (2MHz) | 0.3 (3MHz) |
| 16-bit object code compatible | 8086 | NONE | NONE | NONE |
| Relative assembly language code required | 1 | 1.5 | 1.4 | 1.5 |
| Memory/IO address space | 1 Megabyte/ 64K | 64K/256 | 64K/NONE | 64K/256 |
| Multi/ co-processing | YES (with 8087, 8089) | NO | NO | NO |
| PASCAL PL/M FORTRAN | YES | NO | NO | YES |
| ICE symbolic debugging | YES | NO | NO | YES |

the kind only Intel delivers today. Software that produces object code directly and gives you important extensions that allow you to fine-tune the software to your application.

Software such as PASCAL-88, the block-structured application language rapidly becoming the one most widely used. With our PASCAL-88, you can do direct port I/O and interrupt handling, as well as independent program module compilation. And produce code that runs faster than other, P-code interpreter versions.

Along with PASCAL-88, you get PL/M-88, our systems implementation language, our ANSI-compatible FORTRAN, and our ASM-88 macroassembler. So with more software capability than you've ever had before, now you can choose the right language tool for each application—whatever it calls for.

**Get out in front with complete development support**

All the development support tools you need are ready to go today from Intel. Start with the Intellec® Microcomputer Development System. Add to that our ICE-88™ in-circuit emulator. Together they give you CPU emulation in real time, plus features like symbolic debugging, diagnostic commands and program trace capability. With these tools you'll get your products to market faster than by any other route.

**Looking down the road**

Best of all, with the iAPX 88, your investment in today's solution is protected. Since the 8088 is 100% object-code compatible with the 16-bit 8086—plus its future generations, the iAPX 186 and iAPX 286—you have the industry's only guaranteed headstart on the path to the future. Regardless of which language you're writing in.

So if you want to outdistance the pack, choose the iAPX 88—available today from your local Intel distributor. To get your copy of benchmark results, contact your local Intel sales office or distributor. For more information write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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Circle 19 on reader service card

# Soft sell.

We don't think software should be hard to use.

To make things easier for you, we offer software expertise as well as software.

Our Z80 assembly language comes with RAID (our memory-mapped rapid interactive debugger) which saves debugging time, and SCOPE (our screen-oriented program editor) which provides advanced word processing in a program editor. It cuts 35% of the time it takes to create new programs. What's more, ZSM is a Z80 assembler that generates files compatible with higher level languages – including CIS COBOL, PASCAL, APL, and FORTRAN.

We offer CP/M, the industry standard operating system. So transportable software developed on one system can run on others.

Vector offers a great system for developing BASIC programs with an interpreter for on-line development and an optional compiler for end-user programs.

It's the least we could do. Because we make software development a soft job.

Contact Gary Bennett, Vector Support Center, 31364 Via Colinas, Westlake Village, CA 91362. Or call 213/991-2302.

SCOPE and RAID – trademarked Vector Graphic Inc. Z80 – trademarked ZILOG Inc. CP/M – Registered DIGITAL Research Inc. CIS COBOL – trademarked Micro Focus

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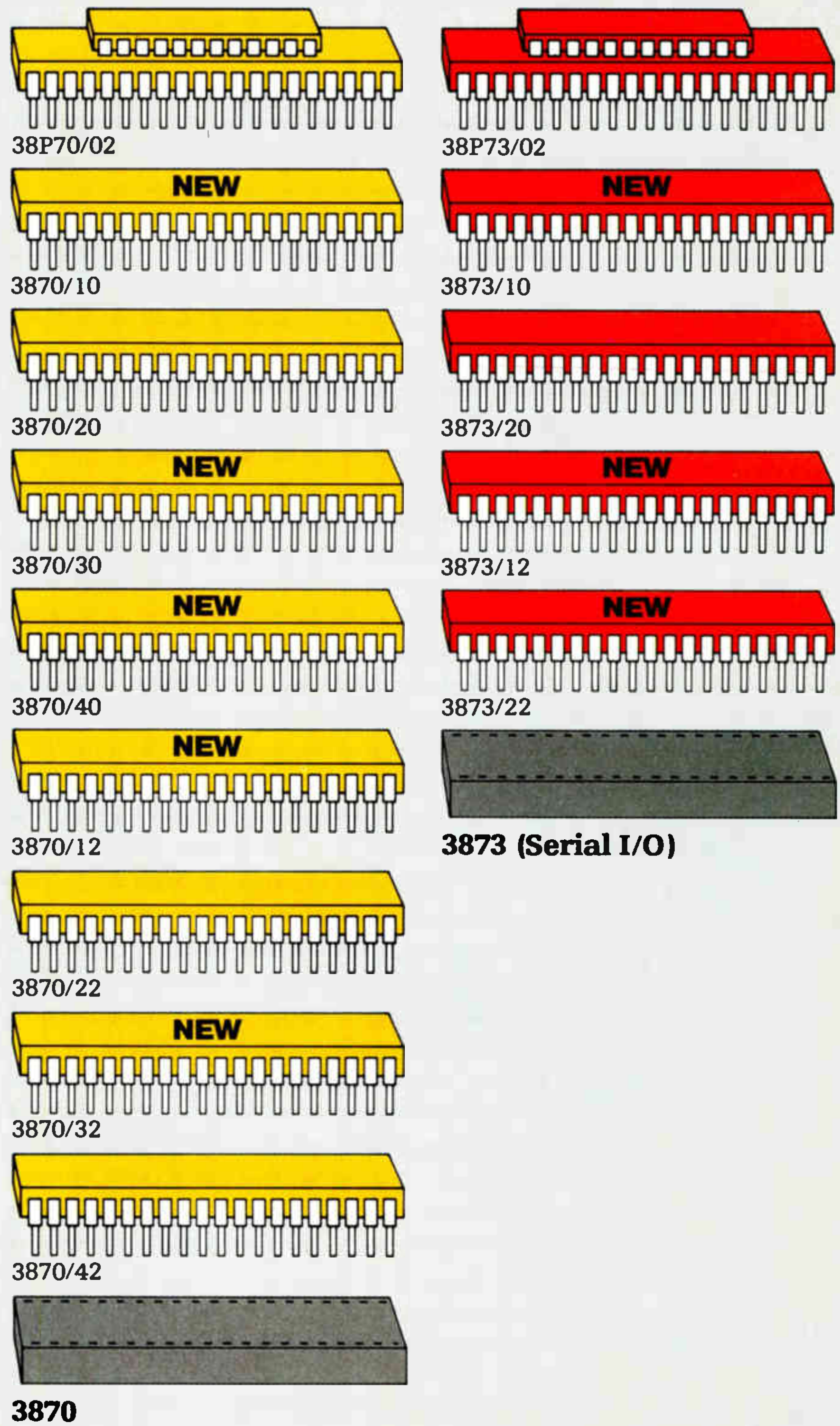
# 3870 momentum continues.

For single-chip applications, no other microcomputer family offers you more design momentum than the 3870 family from Mostek. Now there's even more momentum because eight new parts give you ROM and RAM options never before available. A total of 16 choices. You save by buying only what you need now, yet you'll also be designing in future flexibility.

That's because all our 3870 microcomputers are software compatible and basically pin-for-pin hardware compatible. So expansion or upgrading from 1K ROM to 4K ROM can be as easy as exchanging one 3870 device for another. In the same socket. There's no new architecture to learn. No retooling of artwork. No new vendors to qualify. In other words, there's no loss of design momentum.

This ongoing product line expansion is all part of our commitment and response to your unprecedented demand for Mostek 3870 microcomputers. A demand so strong for so many different applications that we literally ran out of 3870 numbers for all the variations you requested.

So to simplify identification of all our 3870 devices, we developed an expanded, easy to understand numbering system. In this system, the first four numbers designate three generic families: MK3870, MK3873, and MK3875. All three families have multiple combinations of ROM and RAM. The first slash number indicates the amount of ROM available in 1K byte increments; the second slash number identifies the amount of executable RAM in multiples of 32 bytes.



# 8 new ROM and RAM options give you 16 compatible single-chip choices.

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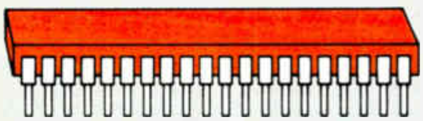
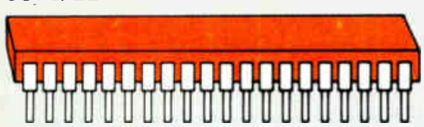
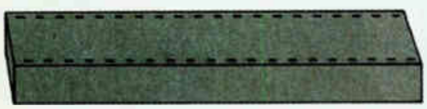


3875/22



3875/42



**3875 (Battery Back-up)**

| Designation | ROM (bytes) | Executable RAM (bytes) | Parallel I/O (bits) | Special I/O | Old Part Number |
|---|---|---|---|---|---|
| MK3870/10 | 1K | 0 | 32 | | • New |
| MK3870/12 | 1K | 64 | 32 | | • New |
| MK3870/20 | 2K | 0 | 32 | | MK3870 |
| MK3870/22 | 2K | 64 | 32 | | MK3876 |
| MK3870/30 | 3K | 0 | 32 | | • New |
| MK3870/32 | 3K | 64 | 32 | | • New |
| MK3870/40 | 4K | 0 | 32 | | • New |
| MK3870/42 | 4032 | 64 | 32 | | MK3872 |
| MK3873/10 | 1K | 0 | 29 | SI.SO. SCLK | • New |
| MK3873/12 | 1K | 64 | 29 | SI.SO. SCLK | • New |
| MK3873/20 | 2K | 0 | 29 | SI.SO. SCLK | MK3873 |
| MK3873/22 | 2K | 64 | 29 | SI.SO. SCLK | • New |
| MK3875/22 | 2K | 64 | 30 | $V_{SB}$, $V_{BB}$ | MK3876 w Standby |
| MK3875/42 | 4032 | 64 | 30 | $V_{SB}$, $V_{BB}$ | MK3872 w Standby |
| MK38P70/02 | External | 64 | 32 | | MK3874 |
| MK38P73/02 | External | 64 | 29 | SI.SO. SCLK | MK38P73 |

## 387X/XX

387X: Generic Part Type

First X: Amount of ROM in 1K increments
1 = 1K
2 = 2K
3 = 3K
4 = 4K

Second X: Amount of executable RAM in 32 byte increments
0 = 0
2 = 64 bytes

Since all our 3870 devices have 64 bytes of scratchpad RAM, that portion of the memory isn't included in the part number.

The basic Mostek 3870 microcomputer family, with 32 bits (4 ports) of parallel I/O, presently has 8 versions. ROM options range from 1K to 4K bytes with an executable RAM option of 64 bytes.

The Mostek 3873 family has 29 bits (4 ports) of parallel I/O plus a hardware serial I/O port capable of handling either synchronous or asynchronous data transfers. Two different ROM versions are currently available, and executable RAM options are coming soon.

The MK3875 microcomputer family features 30 lines (4 ports) of parallel I/O and a standby power mode to protect the executable RAM during low-power situations. Both our 3875 versions have 64 bytes of executable RAM; ROM is 2048 bytes or 4032 bytes.

Unique to the entire 3870 line are our piggyback EPROM (P-PROM™) microcomputers. Designated MK38P70/02 and MK38P73/02, these devices let you prototype and field test your software programs prior to ordering masked-ROM versions. P-PROM microcomputers are also ideal as production circuits in low volume applications.

To simplify software as well, choose our Matrix™ floppy disk development system with real-time in-circuit emulation. The Matrix system can support our entire 3870 line, including low power CMOS versions now being developed.

Three basic 3870 families. EPROM versions. And comprehensive software tools to back it up. It all adds up to more momentum. The kind of momentum that can simplify your design, and extend your product life. To find out how, call or write Mostek Corporation, 1215 W. Crosby Road, Carrollton, Texas 75006; phone 214/323-1000. In Europe, contact Mostek Brussels; phone 660.69.24.

## Editorial

### The new Sputnik: part 2

The problems facing the U. S. electronics industries in the international marketplace are in many ways the outcome of a long-time adversary relationship between business and Government. The situation was described succinctly recently by Robert Herzstein, under secretary for international trade in the U.S. Department of Commerce, when he said: "Over the years, the Government's attitude was that business is a cornucopia that will continue to pour forth benefits without needing much attention and that the role of Government is to regulate business to keep it from having undesirable social impacts. We have to start looking at the other side of the coin now and examine ways in which Government policies and programs are an excessive burden on the competitive ability of business in world markets."

Well and good. But the operative phrase here should jolt us all. *We have to start.* Herzstein's statement reflects enlightenment, but the rest of his speech is replete with suggestions for "analysis" and "evolving a new relationship" and "learning the facts." By now, the problems have been analyzed to a fare-thee-well, the need for a "new relationship" has been the cry of industry for years, and the facts have been laid before one congressional committee after another. The facts are these:

- Japan and other nations have targeted specific high-technology industries like electronics as the major growth areas of the future and are supporting them with all the resources at their command.
- Japan is outgunning the U. S. in producing engineering graduates—19,000 EEs to the U. S.'s 14,000 annually.
- The Japanese government's incentive and subsidy program makes capital available to its electronics industries at lower cost than is possible for the U. S.
- Japan restricts access to its home market while it enters foreign markets aggressively by price-cutting and absorbing the added cost of high quality to capture market share.
- With efforts like the VLSI program the Japanese are marshaling their technological resources for R&D on a national basis.
- There's evidence that other nations are embarking on industry-government partnerships.

What does U. S. industry require?

Basically, industry leaders are asking Government to restore and augment incentives that fueled the growth of the industry in the first place. They don't want direct subsidies or infusions of cash. Rather, they want to foster an environment in which the unique American system can work effectively under the new international conditions. To do this requires, as Robert Noyce, vice chairman of Intel Corp., puts it, "the setting of a new national objective—to provide a commitment to favor development of new productive and innovative industry." Noyce and others have strongly urged specific steps:

- Foster innovation by increasing R&D tax writeoffs and by channeling Government funds to applied research and R&D grants to universities on industrywide problems.
- Give tax credits to firms that support technical education.
- Offer incentives for saving in the U. S. to help capital formation—vital for expanding capacity—and incentives for new ventures.
- Allow the formation of trading companies to increase U. S. effectiveness in export markets.
- Press for equitable treatment in and access to foreign markets.

The political ramifications of some of these steps are complex and forbidding. But we must get on with them. The situation calls for a new Sputnik reaction. As Charles Sporck of National Semiconductor Corp. said recently, "The time to do something is now—not three years from now, not a decade from now, either. By then it'll be all over."

# "We asked for a high frequency counter that measures accurately in tough RF environments. We weren't disappointed."

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# Meetings

**21st Annual Symposium on the Foundations of Computer Science,** IEEE Computer Society, Sheraton Inn–Syracuse, Liverpool, N. Y., Oct. 13–15.

**Annual Meeting, Optical Society of America** (1816 Jefferson Pl. N. W., Washington, D. C. 20036), Pick Congress Hotel, Chicago, Oct. 13–17.

**27th National Vacuum Symposium and Show,** American Vacuum Society (335 E. 45th St., New York, N. Y. 10017). Detroit Plaza Hotel, Detroit, Mich., Oct. 13–17.

**Mini/Micro Computer Conference and Exposition,** Mini/Micro 80 (32302 Camino Capistrano, Suite 202, San Juan Capistrano, Calif. 92675), Brooks Hall, San Francisco, Oct. 14–16.

**1980 Japan Electronics Show,** Japan Electronics Show Association (3-23-5 Nishishinbashi, Minato-ku, Tokyo 105), International Fairgrounds, Tokyo, Oct. 14–19.

**1980 Fall Conference on Emerging Technologies—Teletext and Viewdata,** Society of Cable Television Engineers Inc. (1900 L Street N. W., Suite 614, Washington, D. C. 20036), Playboy Resort and Country Club, Great Gorge, N. J., Oct. 15–16.

**1980 Canadian Conference on Communications and Power,** IEEE, Queen Elizabeth Hotel, Montreal, Quebec, Canada, Oct. 15–17.

**First Brussels NATO Command, Control, and Communications Symposium,** Armed Forces Communications and Electronics Association (5205 Leesburg Pike, Falls Church, Va. 22041), Brussels Hilton Hotel, Brussels, Belgium, Oct. 16-17.

**ISHM 80—International Microelectronics Symposium,** International Society for Hybrid Microelectronics (P. O. Box 3255, Montgomery, Ala. 36109), Hilton Hotel, New York, Oct. 20–22.

**ISA/80—International Instrumentation Automation Conference and Exhibit,** Instrument Society of America (ISA/80, P. O. Box 3561, Durham, N. C. 27702), Astrohall, Houston, Texas, Oct. 20–23.

**PC 80 West—International Printed Circuits Conference and Exhibition,** Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215) *et al.*, Convention Center, Los Angeles, Oct. 21–23.

**1980 Biennial Display Research Conference,** IEEE *et al.*, Cherry Hill Inn, Cherry Hill, N. J., Oct. 21–23.

**Military Microwaves 80,** Institution of Electronic Engineers (Savoy Place, London WC2R 0BL, England), Cunard International Hotel, London, Oct. 22–24.

**Integrated Circuit Quality Control Workshop,** American Society for Quality Control, Electronics Division (Ralph A. Evans, IC-QC, 804 Vickers Ave., Durham, N. C. 27701), Durham, Oct. 23–24.

**1980 Fall Meeting—Electronics Division of the American Ceramic Society** (65 Ceramic Dr., Columbus, Ohio 43214), Sheraton Palace Hotel, San Francisco, Oct. 26–29.

**10th Annual Monterey Conference,** American Electronics Association (2600 El Camino Real, Palo Alto, Calif. 94306), Del Monte Hyatt House, Monterey, Calif., Oct. 26–29.

**10th Annual North American Thermal Analysis Society Meeting** (Robert C. Johnson, Du Pont Central Research and Development Department, Experimental Station, Bldg. 228, Wilmington, Del. 19898), Copley Plaza Hotel, Boston, Oct. 26–29.

**1980 Conference on Electrical Insulation and Dielectric Phenomena,** National Research Council Assembly of Engineering (2101 Constitution Ave., Washington, D. C. 20418), Parker House, Boston, Oct. 26–30.

**ACM Annual Conference,** Association for Computing Machinery (1133 Avenue of the Americas, New York, N. Y. 10036), Opryland Hotel, Nashville, Tenn., Oct. 27–29.

**NEC-NCF/80, 36th Annual National Electronics Conference and National Communications Forum,** National Engineering Consortium Inc. (Oak Brook Executive Plaza No. 2, 1211 W. 22nd St., Oak Brook, Ill. 60521), Hyatt Regency O'Hare, Chicago, Oct. 27–29.

**ICCC/80—Fifth International Conference on Computer Communication,** International Council for Computer Communications (ICCC/80, Box 280, Basking Ridge, N. J. 07920), Peachtree Plaza Hotel, Atlanta, Oct. 27–30.

**1980 Photovoltaic Solar Energy Conference,** IEEE *et al.*, Palais des Festivals et des Congrès, Cannes, France, Oct. 27–31.

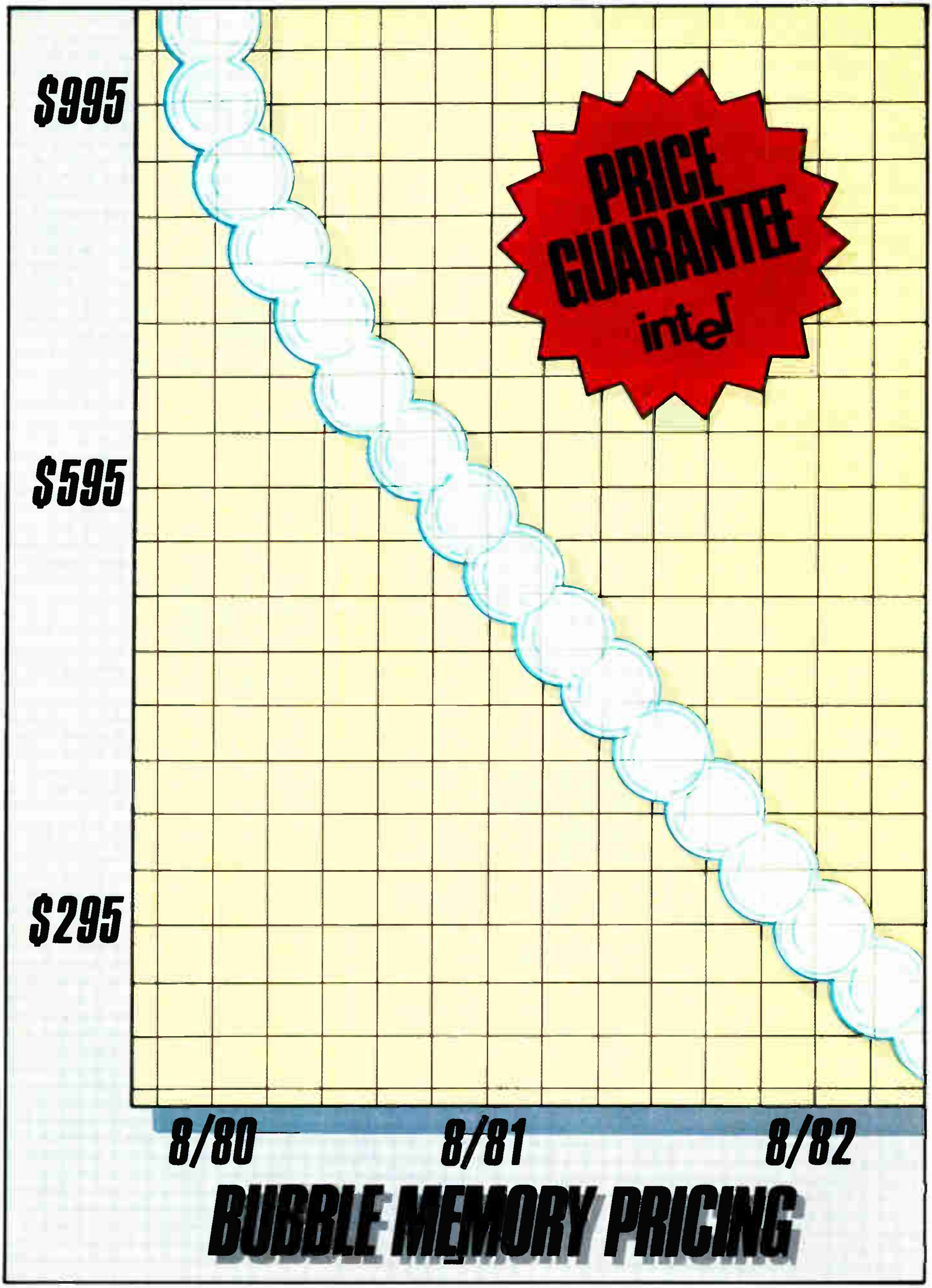
**17th Department of Defense–Association of Old Crows Electronics Warfare Symposium,** AOC (15233 Ventura Blvd., P-8, Sherman Oaks, Calif. 91403), Disneyland Hotel, Anaheim, Calif. Oct. 28-30.

**Fourth Annual Symposium on Computer Applications in Medical Care,** George Washington University (Janice W. Eldridge, Registrar, SCAMC, Office of Continuing Medical Education, 2300 K St. N. W., Washington, D. C. 20037), Capital Hilton Hotel, Washington, D. C., Nov. 2–5.

**Autotestcon '80,** IEEE, Sheraton Washington Hotel, Washington, D. C., Nov. 3–5.

**Midcon/80,** IEEE and Electronic Representatives Association, Convention Center, Dallas, Texas, Nov. 4–6.

**Electronica 80—Components and Assemblies Trade Fair and Microelectronics Congress,** MMG P. O. Box 121009, 8000 Munich 12, West Germany), Fairgrounds, Munich: Fair, Nov. 6–12; Congress, Nov. 10–12.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# Bubble Price Break

## Intel reduces prototyping prices of 1-megabit bubble memories by 40% now. And guarantees a volume price of $595 for complete component sets by August 1981.

Fast-breaking bubble technology. You've been hearing about it for years. Now Intel announces the kind of break you've been waiting for: a price break.

On August 11th, Intel lowered its 100-unit price for the BPK72 Bubble Memory Kit by 40% to $995—less than 100 millicents per bit.

By August 1981, the price of megabit bubble memories ordered in 5,000-unit lots will be an unprecedented $595. That's 60 millicents per bit. Not "projected." Not "expected." *Guaranteed.*

One year later, for 25,000-piece orders, the unit price will be $295—cutting the per-bit price in half once more. Again, we guarantee it.

How can Intel guarantee such a sharp price reduction? Simple. Intel was the first to bring production 1-megabit bubble memories to market. We've been delivering them for over a year, for a wide range of applications, and now we're moving prices down the manufacturing learning curve.

### Get more than bubbles

Intel's bubble memory is a complete set of bubble components for microprocessor-based applications. This set consists of six special support ICs: a controller, a formatter/sense amp., three packages for coil driving and a current pulse generator. It interfaces to Intel® and other microprocessor system buses via the controller, which handles up to eight bubble memory packages, and provides built-in power fail protection and error correction.

The bubble element and its small set of associated ICs can be treated as a peripheral subsystem. This allows designers to concentrate on higher level system objectives, instead of spending time learning the intimate details of bubble device interfacing. Thus minimizing expense in hardware and software development.

### Add more value to your product

With Intel's solid-state bubble memory, all that moves is the information. That means high reliability and low maintenance for your products, even in harsh or unclean environments—the kind where disks and tapes won't go. And since the memory is completely nonvolatile, your data


remains secure when the power goes off. No battery backup or replacement is necessary.

Furthermore, Intel's bubble memory system is small, lightweight and silent. By packing over 1 million bits into less than 100 square centimeters of board space, it allows you to reduce the size, weight and power consumption of your products.

As the natural mass storage for LSI microprocessor-based systems, Intel's megabit bubble memory makes it practical to design more features into your equipment. So now you can build in programmability. Portability. Reduced service and repair costs. All with ensured data integrity, even in hostile environments. Consider what that means in your applications.

### Start designing now

Everything you need to start designing your next generation product is included in our Bubble Memory Prototype Kit (BPK72), available now from distributor stock. It contains all the components necessary for a 1-megabit system, plus a printed circuit board and complete documentation.

To find out how bubble memories can give you that competitive edge in your next project—and to receive our bubble brochure, contact your local Intel sales office/distributor. Better yet, have one of our field sales engineers give you a firm quote based on exactly what you need for your next product. Write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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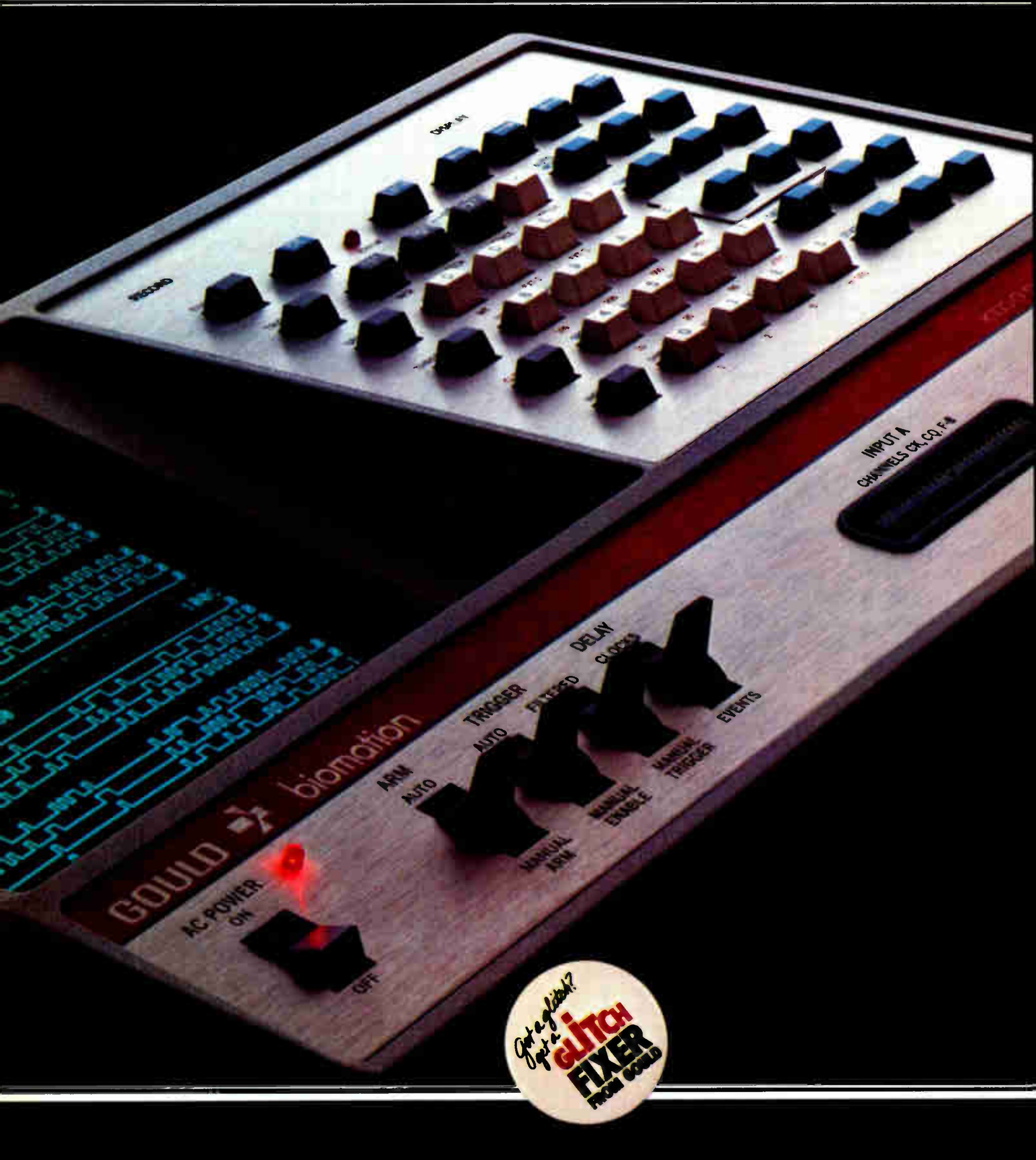
# BIOMATION K100-D



# Compare this general purpose logic analyzer with the currently accepted industry standard.

## The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

**Compare clocking speed.**

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's*. Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

**Compare capacity.**

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**DEC to unveil its 32-bit VAX-11/750**

Digital Equipment Corp.'s second 32-bit computer, well placed to compete with IBM's smaller 4300s and priced to appeal to original-equipment manufacturers, will bow Oct. 21. Originally code-named Comet, the new VAX-11/750 is compatible with VAX-11/780 software and peripherals [*Electronics*, Nov. 10, 1977, p. 36], but is slower and lower-priced. Expected to run at 650 to 700 whetstones (a measure of throughput) rather than the larger machine's 1,000 to 1,100, the 750 could be priced as low as $40,000 to $90,000 in minimal configurations. It will have a full set of commercial software, but many **industry sources expect the 750's central processing unit also to be the Maynard, Mass., firm's first entry into the 32-bit OEM market.**

The 750's low price owes much to DEC's heavy use of custom TTL large-scale integrated circuits. The resulting drastic reduction in parts count has allowed the firm to implement the 750's CPU on about six large circuit boards—about one fourth the number needed for the 780. Thus, the 750 fits almost entirely into a single 19-in. rack or a free-standing waist-high cabinet. Industry sources expect the MOS main memory to be intentionally limited in size, probably to 2 megabytes, to avoid competition with low-end versions of the 780. However, given the 750's price, the similarly priced 16-bit PDP-11/70—and, perhaps, even the 11/44—may sacrifice market share to the new machine.

The 750's introduction has been postponed repeatedly since 1979, say industry observers. Among the reasons mentioned are a desire to avoid fratricidal competition with the PDP-11 line (which is selling well and at a good profit), a large backlog for the 780, teething problems with DEC's new LSI design and production facilities, and competitive considerations.

**Hughes adds laser, sees true 3-D ICs as a possibility**

Another big jump in integrated-circuit packing density appears closer to reality after further studies into laser annealing reported by Hughes Aircraft Co.'s Malibu (Calif.) Research Laboratories. Already a leader in developing laser annealing to replace the conventional furnace heating of ICs, Hughes says its scientists, in experiments, have rigged a second laser as a real-time instrument to measure the annealing process precisely. With the setup linked to a master minicomputer, **they can monitor the growth of large-grain (25-$\mu$m) silicon crystals,** which make it possible to stack circuit structures on top of each other. The potential, according to Laverne D. Hess, who directs the Hughes work: "It gives hope for the first time of fabricating true three-dimensional microelectronic circuits."

**Bell uses LEDs as transmitters in 23-, 7-km lines**

As part of its work with long-lasting light-emitting diodes as transmitters for fiber-optic communications systems, Bell Laboratories has built both the longest and the highest-capacity line thus far achieved using LEDs. Researchers at Crawford Hill, N. J., attained **274 Mb/s on a 7-km line with no need for an amplifier.** The line can handle 4,032 telephone conversations simultaneously. The second line, 23 km long, carried 44.7 Mb/second equal to 672 conversations, without regeneration.

The main point of the work is that it appears to reduce the importance of laser diodes as components of fiber-optic systems. The LEDs are easier to construct and can be less costly, especially for the second-generation systems coming along to operate at wavelengths of 1.3 to 1.6 $\mu$m, where cable loss and dispersion are even less than in the 0.8-$\mu$m region now commonly used.

# Electronics newsletter

**RCA to design its own codec**

RCA Corp.'s Solid State division plans to introduce a codec of its own in the last quarter of 1981. The complementary-MOS device will have an on-board filter and thus enable the Somerville, N. J., operation **to leap into the codec fray, though late, with a strong entry** (see p. 41). Meanwhile, the company expects that samples of two codecs and two codec filters that it is second-sourcing from Motorola Semiconductor will be available this quarter, with production set for the first quarter of 1981.

**CP/M operating software to be extended to 16-bit systems**

Look for the introduction next month of CP/M-86, an extension of the *de facto* standard 8-bit operating system, to work on Intel's 8086 and 8088 16-bit microprocessors. Produced by Digital Research of Pacific Grove, Calif., **CP/M-86 is a single-user operating system that maintains the file format of CP/M release 2,** giving it file-structure compatibility with CP/M. CP/M-86 can also function in a slave mode in a multiprocessor networking scheme controlled by CP/Net.

**National to make boards compatible with Intel's Multimode**

National Semiconductor Corp. will attempt to capture more of Intel Corp.'s market for board-level products by producing boards compatible with Intel's Multimodule series. These are the small piggyback boards that plug into sockets provided on the Multibus series to expand their capabilities. The Santa Clara, Calif., company will ship parallel- and serial-interface and the math-processor piggyback boards by the first quarter of 1981. **National's connectors will be identical to those Intel custom-designed.**

**Ethernet specs available from DEC, Intel, Xerox**

The long-awaited specifications for Ethernet, a local-area digital communications network, have been made available by its designers: Digital Equipment Corp., Maynard, Mass.; Intel Corp., Santa Clara, Calif.; and Xerox Corp., Stamford, Conn. **Both a specification document for hardware and a protocol description are available from any of the three companies.** The documents will be submitted by the parties concerned to the Local Networks committee of the Institute of Electrical and Electronics Engineers, which meets this month in its efforts to develop a local network standard. Hewlett-Packard Co. has already said that if Ethernet is accepted by the IEEE group, it will adopt the standard (see p. 48).

**Addenda**

After eight years of development and test, GTE Products Corp.'s Sylvania Systems group, Needham, Mass., **has won a $190 million, four-year production contract** for 300- and 600-line versions of its AN/TTC-39 circuit switch and for the 50-line AN/TYC-39 message switch—both part of TriTac, the triservice tactical communications program. . . . A new family of intelligent desktop terminals from Data General Corp., based on the Westboro, Mass., firm's 16-bit microNova, **will be software-compatible with all Data General processors,** including the Eclipse MV8000 32-bit Supermini. . . . A 20-bit multipurpose computer to emerge soon from BBN Computer Corp., a Cambridge, Mass., subsidiary of consulting firm Bolt Beranek & Newman Inc., **promises faster operation than machines three times its price.** . . . Semiconductor industry pioneer **Patrick E. Haggerty,** honorary chairman and general director of Texas Instruments Inc., Dallas, is dead at 66.


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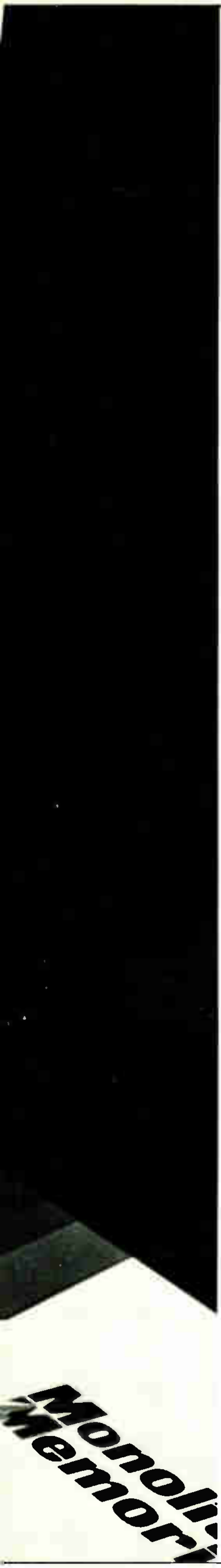

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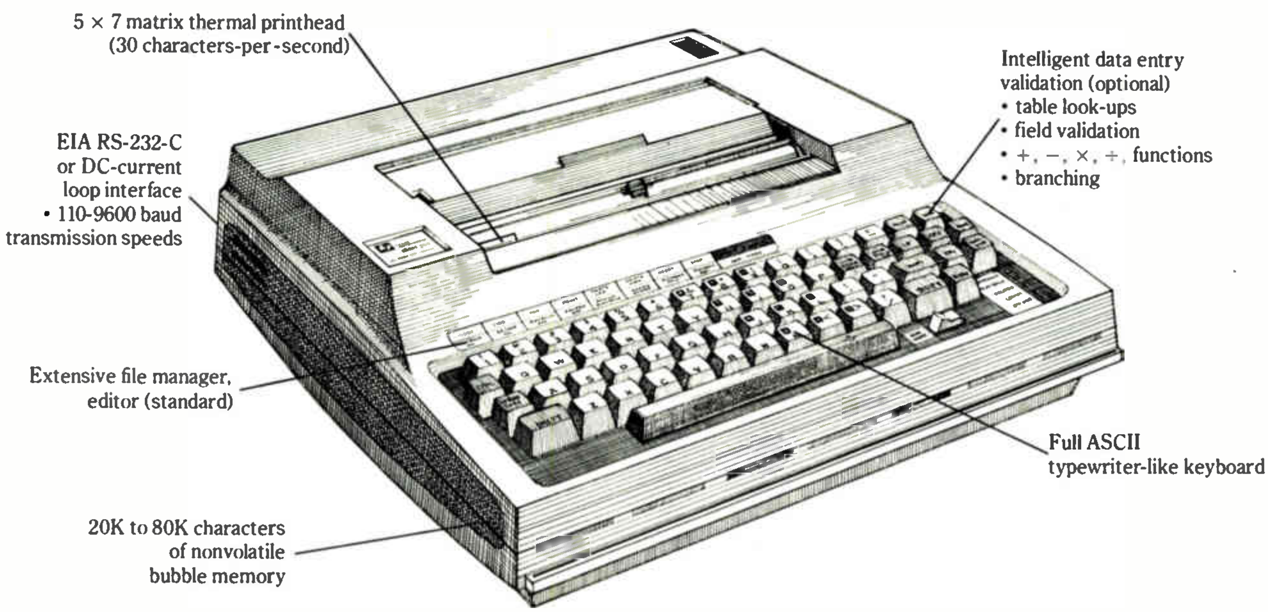


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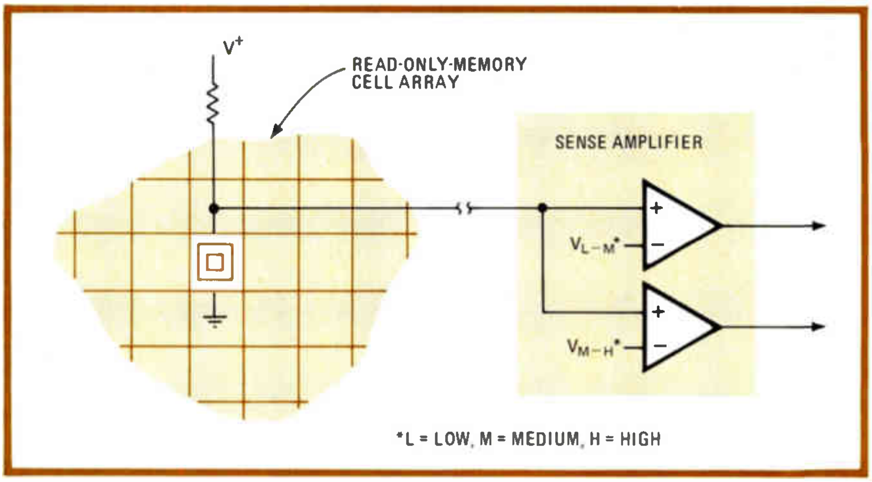
# Four-state cell doubles ROM bit capacity

*by John G. Posa, Solid State Editor*

Read-only-memory cells on two new microprocessors have three transistor sizes with varying voltage levels




**Four voltages.** On Intel's newest microprocessors, each read-only-memory cell has one of four voltage levels. Two comparators determine which output is at a given address.

**By varying the** size and resistance of the transistor—and hence the voltage level—in each cell of on-chip read-only memory, Intel Corp. is able to store 2 bits of information in the ROM cells of its latest microprocessors. Since each cell can therefore hold double the information of an ordinary cell, the Santa Clara, Calif., chip maker can multiply storage capacity without restoring to finer lithography.

The new cells, found in the 8087 mathematics coprocessor [*Electronics*, May 8, p. 114] and the forthcoming iAPX 432 [*Electronics*, May 22, p. 39], can be manufactured with the company's standard high-performance MOS, or H-MOS, process. In fact, the 2-bit cell idea is simple, almost bordering on the obvious.

**Sizes.** In a standard read-only memory, there is only one size of transistor and there is at most one transistor per bit, explains Moty Klein, engineering coordinator for Intel Israel, where the 8087 was designed. "If there is a transistor, there is a 1; if not, you store a 0. When you raise the select line, current flows if you have a transistor, and it doesn't if you don't."

The key to the new ROM is that "there are three sizes of transistor," continues Klein, "one that conducts large currents, one medium, and one small." At each cell site in the ROM array, one of these three transistor types—or no transistor at all—is placed during programming.

To determine which type of transistor is at a selected memory location, a specially designed sense amplifier is used. When a cell is chosen, it is effectively connected through a resistance to a logical high voltage. The potential developed across the cell—which corresponds to the size of the transistor—is fed to two comparators (see figure).

One comparator's second input is tied to a voltage between the two that would be generated by a small and a medium-sized transistor. The other comparator's second input has a voltage between those of the medium-sized and large devices.

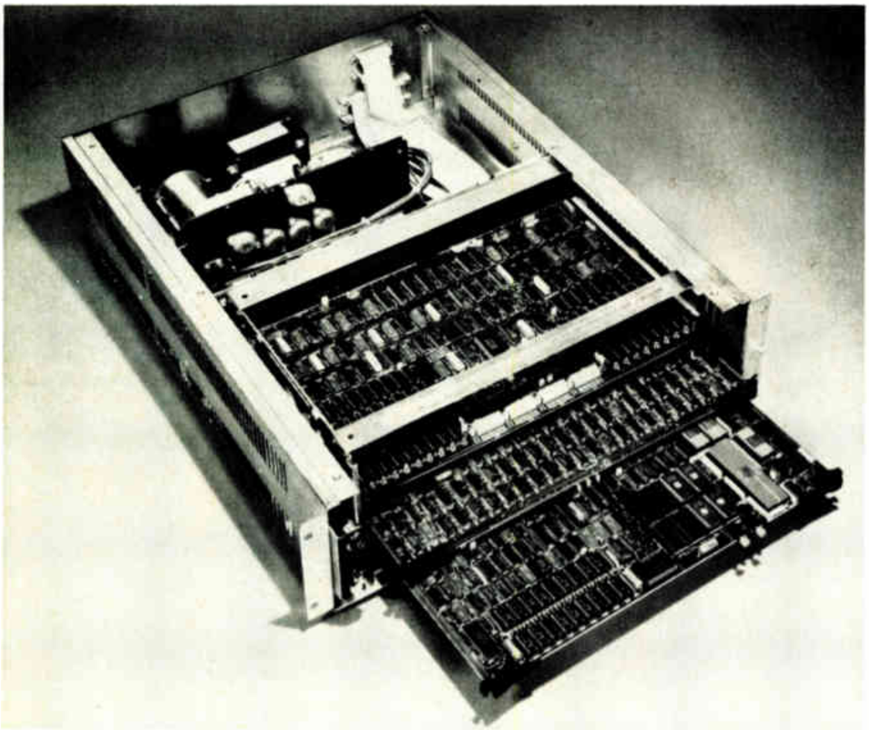
Consequently, the two outputs of the comparators will reflect which of the three voltage levels (or lack of voltage) is at that address. The sensing is done in parallel, so that there is no need to cycle through the four voltages in the sense amplifier, says Klein.

Because room must be allocated at each ROM cell for the largest transistor, even if a smaller device or no transistor is placed there, there is some wasted silicon area. However, says Klein, "it is more than made up for by not having to store the 4 states separately."

### Microsystems

## Mini makers facing another IC challenge

Another heavyweight entry into the 16-bit microcomputer board business weighed in at last month's Wescon, when Motorola Inc. announced its board computer line based on its 68000 microprocessor. A major new direction for the company's Semiconductor Group in Phoenix, Ariz., the Monoboard Microcomputer draws even more sharply the battle lines between the two camps contest-



**Caged.** Motorola's Versamodule boards include, from bottom, the 68000-based Monoboard Microcomputer, a floppy-disk controller, and 128-K bytes of random-access memory.

ing this burgeoning business.

Defending the traditional 16-bit ground are the minicomputer makers. These are led by Digital Equipment Corp., whose LSI-11 board computers hold more than half the market. The attack is coming from the chip makers, led by Intel Corp. with its iSBC 86/12A line, Texas Instruments Inc. with its TM990 line, and now Motorola. Also getting attention is Zilog Inc.'s new 16-bit board based on the Z8000.

**Powerful.** A key issue will be software—but since Motorola's entry has the high-performance 68000 going for it, it is the most powerful 16-bit hardware yet in terms of sheer throughput and flexibility, as most competitors admit.

Operating at 3 megahertz, the processor board holds 32 or 64-K bytes of random-access memory, as much as 64-K bytes of read-only memory, serial and parallel input/output circuitry, and programming counter-timers. With peripheral boards, it can be configured for mass storage, for data communications and networking, and by adding another microcomputer board, for high-throughput array processing.

What might be the typical mini maker view of a semiconductor firm's microcomputer board comes from DEC. "The hottest, niftiest chip isn't always equal to the best board," says Lloyd Fugate, planning manager for the microcomputer products group. "Building a new board is not that big a thing; software is more important in the 16-bit world."

He says operating and applications software accumulates in value, especially if it is transferable to new machines. DEC has been building its library since the LSI-II came along in 1977, and it remains for Motorola, Intel, and others to achieve such a track record, he argues.

**Coming.** For Motorola's part, it is bringing out operating software to go with the Monoboard, which sells for $1,300 apiece in volume. A memory-resident multitasking software package will be ready for first shipments of the microcomputer in November, and a disk operating system is slated for completion in 1981.

The remainder of the family—called Versamodules—will be a board with 128-K bytes of RAM, a floppy-disk controller, a multichannel communication module, a universal peripheral controller, a chassis, and a power supply. Plans for 1981 include an advanced microcomputer and a 1-megabyte bubble memory module.

Chip makers argue that they have a hardware advantage over the minicomputer makers. The Motorola board illustrates "the industry's two- or three-year technology lead," says Robert Brannon, marketing manager of Intel's OEM Microcomputer Systems division, Hillsborough, Ore.

**Upward.** He firmly believes momentum lies with the chip firms, which "represent VLSI versus LSI, multiprocessing against uniprocessing." He downplays the mini makers' software lead, claiming it will dwindle as his company and others put more programming onto chips.

However, Intel is moving to make it easier for original-equipment manufacturers by introducing soon a lower-cost, stripped-down development system that contains only the software tools necessary to write these programs. At present, the semiconductor-supplied microcomputer boards use high-ticket full-scale development systems. DEC's LSI-II, on the other hand, has a resident editor for assembling applications software as part of the board price.

**Closing.** As the two sides increasingly battle, most observers expect the semiconductor houses to close the gap. "They can give DEC and the others a run for their money," says one industry consultant. "The bottom line will be how easy they make it to write software."

Sales in this market are still fairly small—in the $100 million range for 1980—but growing, says G. S. Bushee, vice president for small computer services at Dataquest Inc., the Cupertino, Calif., market research firm. He and other market analysts agree that DEC is the clear leader and that Intel has likely overtaken TI for second place this year. Overall, the 16-bit board business is a tough one to categorize "because it is so evolutionary at the moment," Bushee says. "It's neither quite a system nor a chip." **-Larry Waller**

## Solid state

# Superconductivity at room temperature reported by Air Force researcher

The dazzlingly fast supercomputers envisioned for the 1990s ordinarily are thought of in terms of Josephson junctions, which require supercooling to near absolute zero. However, Fred W. Vahldiek, a materials research engineer at Wright-Patterson Air Force Base in Dayton, Ohio, may have stumbled upon superconductivity at room temperature.

Such a discovery could lead to uncooled computers with picosecond machine cycles, to 100% delivery of the power from generating stations without loss or heat in transmission, and to a whole world of new applications based upon extremely efficient superconducting magnets.

"It was an accident," says Vahldiek. He was trying to obtain ductility from titanium bromide crystals, ordinarily extremely brittle. "I did get the ductility after all these years. Then we looked at some other properties, and . . . the superconductivity came along as a gift."

**Materials.** Vahldiek was working with borides of titanium "because they are very good conductors, yet they have boron in there, supposedly an insulator. How do you explain a conductivity five, six, seven times better than the host metal's—titanium, in this case?"

The composition change was found by accident through deformation at room temperature under hydrostatic conditions. "The inner core of the crystals had a quite different composition—there was a change in the structure. . . . That's when I found the ductility," Vahldiek explains.

**Resistance.** He used a four-point probe to test for electrical resistance, and "in two directions the resistance appeared normal." But in the third direction, to his amazement, "the resistance was zero."

A fluke that could never be duplicated? "No, I've got 15 or 16 crystals by now," he reports. Each time, the measurements show a complete absence of resistance.

Vahldiek has patents pending both on the methods used to grow the crystal and on the deformation process. The Japanese and Russians, too, have been growing titanium bromide crystals, but not in same size and shape.

Usually, titanium boride adheres to the formula $TiB_2$ with a hexagonal or quazi-cubic structure, explains the researcher. After deformation, the ratio of boron seemed to drop from 2 to about 1.5 or 1.6, "and X-ray data show a possible orthorhombic structure, with crystal symmetry that will boggle your mind."

Vahldiek feels that this symmetry, together with the change in composition, brings about the ductility and the superconductivity. "And these borides are supposed to be very stable," he says.

As for the prospect for room-temperature Josephson junctions for future supercomputers and the like, Vahldiek observes, "That's only one of dozens of other properties that will need further investigation. I'll be busy for about six, seven months at least." **-John G. Posa**

### 'It's possible,' says IBM

Prominent among the researchers investigating superconductivity are those at International Business Machines Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N. Y., and a scientist there acknowledges that Fred Vahldiek's claim could be sound. If electrical conduction is supported by normal electron-phonon interaction, he says, the upper temperature line for superconductivity is from 30 to 40 kelvin. But if conduction is carried out by another means, such as through exciton interaction or electron-hole pairs, superconductivity could occur even above room temperature, he says.

He does warn that a superconductor must pass two tests. It must not impede current flow, of course; but it must also repel magnetic flux, a property known as the Meissner effect. Vahldiek says that he is "setting up a coil right now to test for the Meissner effect." He has already seen magnetic repulsion caused by the fields in his electron microscope, he says. **-J. G. P.**

## Communications

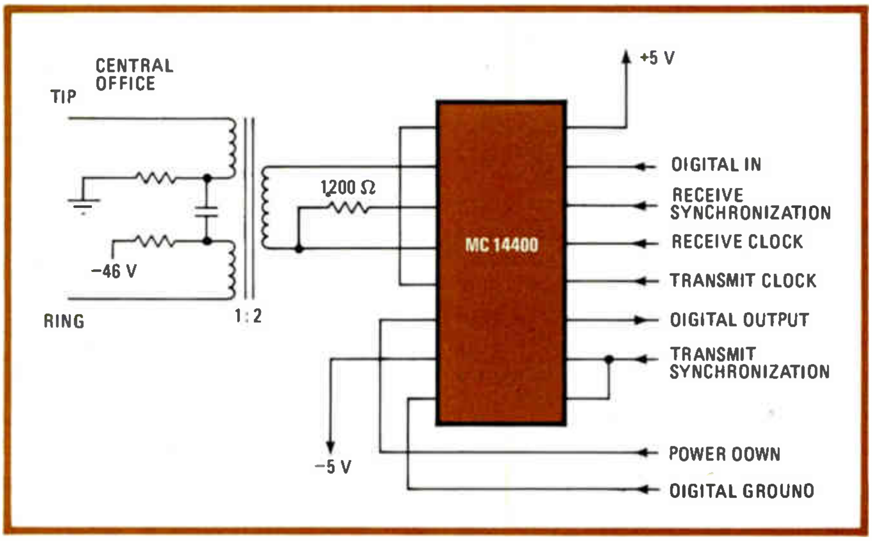
# IC makers readying codec-filter combos

Having successfully launched coder-decoder and filter integrated circuits for digital telecommunications equipment, IC makers are readying the next step: putting codec and filter, as well as peripheral functions, on the same chip. The merits of their various approaches already are sparking industry speculation and discussion.

No fewer than three major semiconductor houses—Motorola Inc., Mostek Corp., and Intel Corp.—are expected to provide samples of codec-filter ICs during the first quarter of 1981. Officials at Motorola's Integrated Circuit division and at Mostek are ready to discuss their designs, though not in detail.

Close behind that trio will be National Semiconductor Corp. and Advanced Micro Devices Inc. What's more, industry sources report that American Microsystems Inc. is already shipping samples of its single-chip codec and filter.

**Still C-MOS.** For increased density, Motorola will build the new MC14400/01/02 series in silicon-gate complementary-MOS [*Electronics*, Sept. 25, p. 34], packing codec, filter, a voltage reference, and other functions on a 30,000-square-mil IC, says Bob Karasch, product manager for standard telecommunications devices at the Austin, Texas, division. The present metal-gate C-MOS codec




**More on chip.** Motorola's forthcoming codec and filter on a 30,000-mil² silicon-gate C-MOS chip may be used in such setups as the pulse-code-modulated voice channel shown.

and filter are 35,000 and 20,000 mils², respectively.

Motorola will continue its controversial approach of offering separate chips to assign time slots to the codec [*Electronics*, June 5, p. 125]. Karasch maintains that some systems will not need time-slot assignment, and for those that do, software assignment may be the solution in some applications.

Mostek says its forthcoming codec-filter, the MK5300, will integrate the circuitry for time-slot assignment, as Intel has already done with its codec IC. However, the Carrollton, Texas, firm will also offer a 5300 chip without the assignment function, says Robert J. Paluck, vice president of data and communications products.

**N-MOS next.** Though the current MK5116 codec is fabricated in C-MOS, Paluck says the 5300 will be done in n-channel MOS for improved density and cost. Designers intend to hold down dissipation through innovative circuit techniques like those used in the MK5912, an n-MOS filter IC unveiled earlier this year.

Though final specifications are not yet available, Paluck expects typical active power dissipation on the 5300 to come in at around 50 milliwatts. Motorola is specifying a 50-mW typical active power dissipation for its combined codec and filter, half that of its two-chip set.

At Intel, "our customers continue to find time-slot–assignment circuitry to be of great value, and one should expect future Intel products to have it," says Anthony R. Livingston, telecommunications marketing manager. Although the Santa Clara, Calif., company has made great strides in reducing the dissipation in its n-MOS communications chips, it is likely that its codec-filter ICs will be available in C-MOS as well, dropping dissipation to the 50-mW range.

National Semiconductor will not disclose its approach on time-slot assignments; in fact, it will only say that its codec-filter chip will be available in samples around mid-1981. It is believed that the IC will be fabricated in the Santa Clara company's proprietary double-polysilicon C-MOS (P²C-MOS) process.

In the works at AMD is what the Sunnyvale, Calif., firm calls a subscriber-loop audio-processing circuit, or SLAC [*Electronics*, June 19, p. 35]. It will be an n-MOS codec filter with a 150-mW active dissipation.

At AMI, also in Santa Clara, a spokesman will not comment on reports that the firm will be in production with its C-MOS chip by year's end. The part is expected to dissipate 100 mW when active.

The AMI chip is said to have been developed for Hitachi Ltd. for use in a subsystem in telecommunications equipment being designed by Nippon Electric Co. AMI's initial version

## Competition already for the newest IBM 4341

Barely three weeks after its announcement, IBM Corp.'s 4341 group 2 processor has evoked a plug-compatible response. Moreover, the 4446 from IPL Systems Inc. is not only software- and microcode-compatible with the upgraded IBM machine, but it also runs 10% to 20% faster, says Stephen J. Ippolito, president of the Waltham, Mass., firm.

The 4446 executes instructions typically in 50 nanoseconds. Other specifications match those of the new 4341: 8 megabytes of maximum main memory, 16-K bytes of cache memory, and six standard channels.

Pricing is just a matter of deciding how much to undercut IBM, according to Ippolito. He expects shipments to get under way in the third quarter of 1981, soon after the scheduled first shipments of the 4341 group 2 [*Electronics*, Sept. 25, p. 51]. "We're counting on the old pattern, where a flood of orders forces IBM to announce longer and longer delivery times," Ippolito says. "The 4446 will be for customers who just can't wait for IBM."

The seven-year-old company has always been in the plug-compatible business, but in a break with the past, it will market the 4446 itself rather than through original-equipment manufacturers. Now beefing up its sales and service forces and offering remote maintenance, the firm has already begun going directly to end users with slightly modified versions of two earlier IPL processors, familiar in the U. S. as Control Data Corp.'s Omega series and sold in Europe under the Olivetti nameplate. These machines are the IPL 4443 and 4436, which are plug-compatible with IBM's 4341-1 and 4331-2, respectively. Like its predecessors, the 4446 incorporates high-speed emitter-coupled-logic circuitry, a modular, bus-based architecture, and IBM-compatible microcode control. The full line can be upgraded in the field, Ippolito says. **-Linda Lowe**

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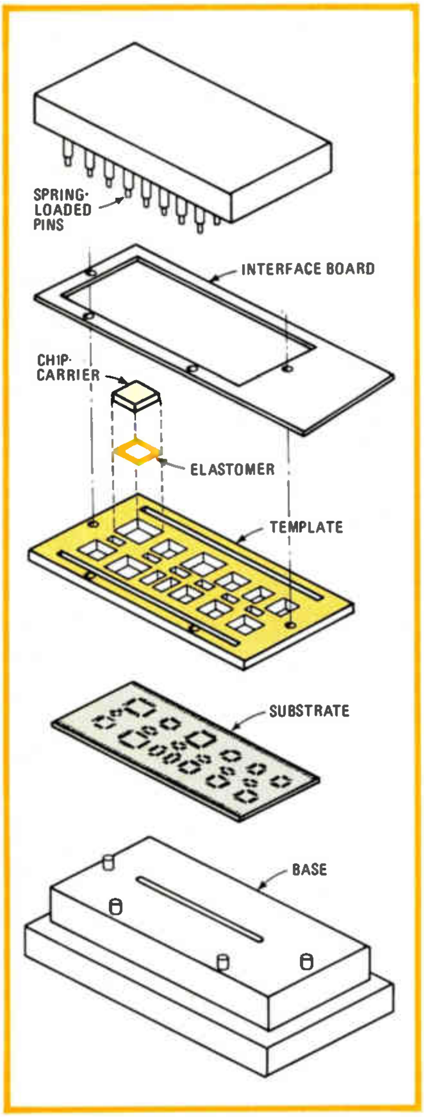
will offer the $\mu$-law companding code for the North American market and an A-law part is in design.
**-Wesley R. Iversen and Bruce LeBoss**

## Packaging

# Elastomers cushion prototype reworks

Thanks to a solderless assembly method, circuits and ceramic motherboards damaged by the breaking of soldered connections during rework may become a thing of the past. Developed by Digital Equipment Corp. for prototype work, the new technique uses conductive elastomers to make temporary electrical contact between leadless chip-carriers and the ceramic substrates.




**Easily altered.** To avoid soldering chip-carriers to prototype boards, DEC uses a temporary elastomer connection and a template to hold them in place.

The soft assembly and test approach, as it is called, makes it possible to remove and replace faulty components both quickly and safely when a module fails in testing, says George A. Katronge, senior applied engineering manager of DEC's Applied Manufacturing division in Westboro, Mass.

**Saves money.** "Until you achieve full correlation between incoming electrical test programs and a device systems application—and this can take months—[hybrid subassembly] yields run extremely low," Katronge points out. "During that period, you have to rework continually, and a lot of ruined circuits have a large impact on the cost of introducing a new product."

At such an early stage, he says, soft assembly and testing pays high dividends. "Another plus is that when you return defective circuits, the maker can't claim they don't work because you damaged them."

Elastomer materials, from companies like Tecknit and Amp, have been used as connectors in products like digital watches and calculators. Using them as connectors in prototyping with leadless chip-carriers is a notion that has been around, but only now has the need arisen as the carriers are moving into more general use [*Electronics*, July 3, p. 45].

As the figure shows, the DEC scheme uses a Teflon nonconducting template between the ceramic substrate and the chip-carriers. The template also houses the elastomer elements, which make electrical connection between the carrier's pads and corresponding substrate pads.

Strips of the same elastomer also connect input/output pads on the subassembly with those of a test interface board in an electrical test system. A cover board containing spring-loaded pins clamps the whole assembly together with sufficient force to close all connections, and the package is ready for testing as a complete module.

Unclamping and reclamping the package to replace defective parts may be repeated many times without harm to any of the components, Katronge says. When production begins, the chip-carriers can be soldered on ceramic motherboards, as DEC is doing with its LSI-11/23 minicomputer, which was the initial tryout of soft assembly and test.

Several manufacturers have approached DEC for details about soft assembly and testing, which pleases Katronge. "This is by no means a proprietary thing," he says. "The materials we use are readily available, and it's an easy matter to tool custom templates—anybody can do it."
**-Linda Lowe**

## Production

# Laser system speeds pc-board checks

Chrysler Corp.'s Huntsville (Ala.) Electronics division is teaming an automatic component inserter with a Chrysler-designed laser scanner that automatically inspects printed-circuit boards. The scanner, which the company plans to market, replaces human inspection and promises much higher throughput.

"This is the first time we have had a machine to do this kind of inspection," says Philip Geise, an engineering supervisor in the Electro-Optics Systems group at the division. Chrysler is applying the minicomputer-controlled scanner to a component inserter that stuffs boards for automobile spark-control computers. The 5-by-10-inch boards are scanned at the rate of 20 a minute.

**Setup.** As the figure shows, the system scans the bottom of each board with a 2-milliwatt helium-neon laser deflected by an X-Y moving-iron galvanometer and several folding mirrors. As each board moves off the insertion line, it is positioned to form the final side of a boxlike enclosure. The laser, inside the enclosure, scans the board and

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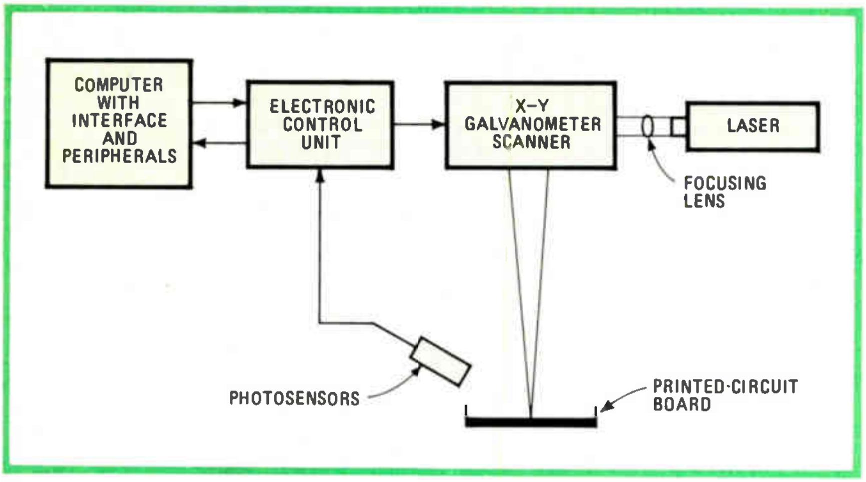



**Laser inspection.** Chrysler's Electronics division has devised an automatic inspection system that uses a laser to look for incorrect or absent welded leads on stuffed pc boards.

the reflected beam is sensed by silicon photodiodes, whose signal feeds a General Automation 16/45 16-bit minicomputer.

The beam is programmed to scan the leads of the board's components according to a pattern stored in memory. A correctly clinched lead causes a characteristic null in the reflected beam; the lead blocks the laser beam from the photodiode sensor. If the lead is clinched in the wrong direction, is the wrong length, or is missing (perhaps because the component is missing), the characteristic signal fails to appear.

**Memory sizes.** The Chrysler setup has 32 kilowords of memory, even though 16 kilowords would be sufficient to store the scan patterns expected on a board, Geise says. The system includes a magnetic-tape reader for loading a board's scan routine and a cathode-ray-tube terminal. The minicomputer will alert the operator when a failure is repeated excessively.

The system can also be programmed to detect other circuit-board faults, Geise points out. On bare boards, for example, it can check hole location, line-run separation, over- and under-etching, superfluous conductors, and copper bridges. On flow-soldered boards, it can look for solder bridges. In that case, the insides of the scanning enclosure are coated with highly reflective paint. Since the bridges are also reflective and generate glints on the reflective sides, the photosensors detect them.

Chrysler calculates its system can inspect at least 25 components or 50 component holes per second. "To reach this speed, a great deal of effort was needed to optimize the scan patterns," Geise reports. "We might not scan an entire lead, for example, but jump-scan from one to another. If a board were really bad—no leads at all, for example—it would take longer to scan than if it had no defects at all."

Right now Chrysler is completing tests of the system for the U.S. Army Missile Command, which helped pay for its development as part of its manufacturing methods and technology program. When it goes on the market, it will sell for between $80,000 and $100,000 and be built around another General Automation processor, the GA-220 microcomputer. Geise described the scanner in a paper at a Huntsville meeting last week sponsored by the Society of Photo-Optical Instrumentation Engineers.

The Army's program manager in Huntsville for the laser scanner, Robert L. Brown, is quite pleased with the results. He points out that the scanner has been better than 99% effective at detecting failures on the Chrysler production line and that this is "an impossible percentage [to achieve] with human inspectors." **-Alfred Rosenblatt**

**Business systems**

# Fujitsu office unit tests U. S. waters

Situated in an out-of-the-way corner at the recent Wescon show was what may be the tip of another Japanese iceberg: a 16-bit office business system to which Fujitsu Ltd. sought U. S. reactions. The Facom 9450 has

## Wescon encore set at Anaheim

Pleased by the turnout for the first Wescon held in Anaheim, Calif., last month, show directors have voted to bring it back for an encore in 1982. The unaudited attendance total was 63,000; though that will drop, the final figure will still be well above the 35,300 audited total for the 1978 show at the Los Angeles Convention Center.

Also important in the decision by the board of Western Electronic Conventions Inc. was how well the show came off in Anaheim's convention center, says a spokesman. "Parking, more booth space, and convenient hotel locations all played a part," he notes.

Booths for exhibits numbered 1,150 this year, up from the 921 sold in Los Angeles in 1978. Also, most of the large hotels in Anaheim are within walking distance of the center, whereas the Los Angeles arena is in a rundown central-city location.

The biggest drawback of a permanent shift to Anaheim, some 35 miles south of downtown Los Angeles, however, is that the show is farther away from the major southern California population center, observers say, though they admit that criticism would be blunted by another good attendance total in 1982. As usual, the show in odd-numbered years will continue in San Francisco, at Brooks Hall for 1981 and afterwards at a new, bigger arena slated to be completed for the 1983 gathering. **-Larry Waller**

been on sale in Japan as a terminal and is being introduced as a personal computer by its maker, Panafacom, a joint venture of Fujitsu and Matsushita. In the U. S., it is likely the new Fujitsu-TRW joint venture will market it.

For some time, industry observers have been expecting the Japanese electronics industry to jump into the U. S. very small business systems market, just as it has in consumer electronics, semiconductor memories, and the like. If the Facom 9450 is indeed the first of many such Japanese products in this market, it sets a high mark for those to follow.

**Target.** While withholding performance figures, Fujitsu says the 9450 is much more powerful than top-of-the-line U. S. personal computers, whose makers are advancing into the market for very small business systems. If so, the expected

## News brief

**Ethernet starts to grow**

Even as Hewlett-Packard Co. signaled its intention to adopt the Ethernet standard for local data networks, the protocol's originator, Xerox Corp., announced its second product that will link up with such a net: a 43-page-per-minute, laser-scan printing system for word and data processing, copying, and electronic mail. Novel in the Stamford, Conn., company's 5700, which accepts inputs from both Xerox and IBM word processors, is a touch-control screen similar in concept to the Proteus of Solid State Technology Inc. and Massachusetts Institute of Technology [*Electronics*, June 5, p. 39]. A typical system with two stations that accept input from an RS-232-C line, magnetic media, or Ethernet, plus copying facilities, forms compiler, and automatic stapler, has a purchase price of $91,050. Meanwhile, HP added its stamp of approval to Ethernet by announcing that it plans to use a controller chip designed by Intel as part of a three-company pact with Xerox and Digital Equipment Corp. [*Electronics*, June 5, p. 89]. The Palo Alto, Calif., company says, however, that it will not adopt Ethernet unless it is accepted by the committee working on standards for local data networks.

**Nestar's local net goes European**

Cluster/One model A, a local network for hooking up as many as 65 Apple 2 microcomputers, is now being offered for sale in 17 European countries. The Model A was introduced earlier this year [*Electronics*, Jan. 31, p. 43] by Nestar Sytems Inc. of Palo Alto, Calif., and is being supported in Europe by Zynar Ltd., a subsidiary of the Rank organization in England headed by Colin Crook, of Motorola Semiconductor fame. Users may communicate with one another and share both resources and files with the system, whose cost may be as low as $4,800 per station for a 10-station network.

**EE to head National Science Foundation**

The Senate has confirmed John G. Slaughter, former academic vice president and provost of Washington State University, as head of the National Science Foundation. From 1977 to 1979, Slaughter, now 46, was the NSF's assistant director for astronomical, atmospheric, earth, and ocean sciences. He has a Ph. D. in engineering science from the University of California at San Diego; a bachelor's in electrical engineering from Kansas State University; and a master's from the University of California at Los Angeles.

**E-Systems looks to digital teleconferencing**

By year-end, an E-Systems Inc. demonstration video teleconferencing setup using digital transmission will be in operation at the McLean, Va., headquarters of Satellite Business Systems Inc. The system, being developed under contract to SBS by the Dallas firm, is designed for sale to SBS customers and others with on-premise earth stations using digital satellite channels. In contrast, AT&T's Picturephone meeting service [*Electronics*, March 13, p. 12] uses land analog phone lines, and AT&T expects many users to come to its facilities in key cities, renting them on a per-conference basis.

$8,500-to-$10,000 price tag that includes a terminal, two minifloppy disk drives, and a matrix printer should be highly competitive.

The disk drives hold 320-K bytes each, and the processor addresses 128-K bytes of random-access memory, though between 26- and 56-K bytes of the RAM accommodate the operating system and utilities that Fujitsu designed. In contrast, the full 128-K bytes of RAM in the new Apple III are user-accessible.

The 9450's power lies even more in its software. It features foreground/background job processing, as well as real-time control and full-duplex communications capability over RS-232-C and IEEE-488 links. It also uses an intermediate code to separate editing, compilation, and execution modes into three clock phases that can run concurrently.

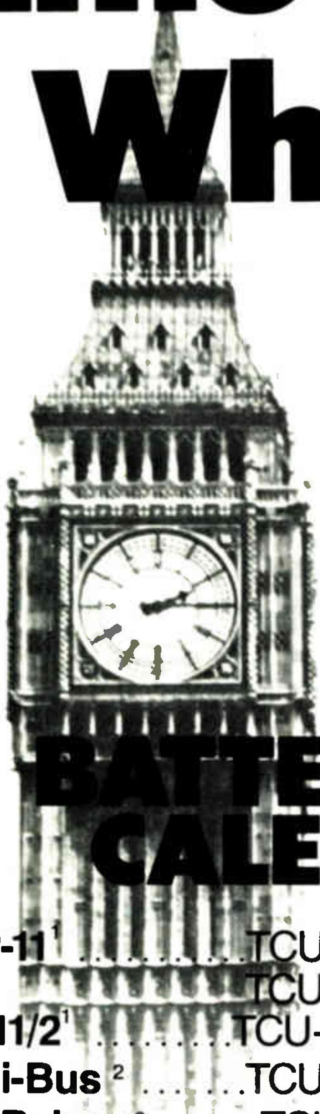
On top of this is the development software, which initially consists of business Basic and single- or double-precision scientific Basic. The software package also pays considerable attention to error detection.

**Crucial.** There are 12 user-definable keys for easy reference to often-used functions and commands, and the software is oriented towards a number of office functions, although it does not include word-processing features. In fact, application software is the crucial factor in the success of the Facom 9450 and other Japanese entries into the very small business systems market.

Already the leading American producers, notably Apple and Radio Shack, can point to impressive libraries of applications software—both their own offerings and those of software houses. They may not blanket the market, as Japan discovered IBM does with its mainframe applications software, but they already enjoy a healthy lead.

However, Fujitsu and its American partner, TRW Inc., are well aware of the importance of the applications software. TRW-Fujitsu Co. [*Electronics*, Sept. 25, p. 102] is hard at work writing the software for its initial offering, the Facom V-830 business computer aimed at the IBM System/34 market.-**Martin Marshall**

# Time is precious Why lose it?



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# DIGITAL PATHWAYS


Instrumentation
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# Washington newsletter

**AT&T to seek competitive bids for fiber-optic link . . .**

American Telephone & Telegraph Co.'s Long Lines department says it will solicit competitive industry bids in about a month for the Boston–to–New York leg of its proposed 611-mile, digital fiber-optic linking of the Northeast Corridor, pending Federal Communications Commission approval of the plan. The first leg of the net, connecting New York, Philadelphia, and Washington, D. C., will be built by AT&T's Western Electric Co. Atlanta works. AT&T's initial application for the system, filed in late January, estimated the cost of the system at $79.1 million and an **operational goal of 1983 for the Washington–to–New York and 1984 for New York–to–Boston routes.** AT&T Long Lines officials say the competitive proposal requests will specify system bids to include fiber optics and light-emitting-diode signal sources and regenerators.

**. . . as advances change plans, Long Lines says**

Innovations and advancements in lightguide technology and manufacturing since the January filing with the Federal Communications Commission led AT&T Long Lines to seek competitive systems bids for the Boston–New York link, according to Thomas W. Scandlyn, network engineering vice president. Though the initial application sought authority to use a 90-Mb/second system known as FT3LC, Scandlyn told the FCC Common Carrier Bureau at the end of September that the unavailability of that system at the time of filing led the company to plan the New York–Washington route using the 45-Mb/second FT3L with light-emitting diodes operating at 820 nm. **"Refinements in manufacturing, the quality and yield of fiber,"** Scandlyn wrote the FCC, "now permit operations at 1,300 nm, using LEDs in the 90-Mb/s regenerators. Further, we expect those innovations to be available for the initial service."

**IBM wins three key military jobs worth $127 million**

International Business Machines Corp.'s Federal Systems division won three key military system development contracts totaling more than $127 million, as awards by the services rose sharply at the end of September to beat the Federal fiscal year-end deadline. **The biggest award was $95 million** from the Air Force Space division for full-scale engineering development of the operational control system for the long-stalled Navstar Global Positioning System.

**NIOSH to research possible hazards at component plants**

A research study on potential occupational health hazards in the electronic components industry is being initiated by the National Institute of Occupational Safety and Health. NIOSH, an arm of the Department of Health and Human Services, says the effort, set for completion on Sept. 2, 1981, will begin collecting data at open meetings at 1 p.m. on Nov. 5 at the New York Academy of Sciences in New York City and at 9 a.m. on Nov. 7 at the State Office Building in San Francisco.

Project director Mark Boeniger at NIOSH offices in Cincinnati, Ohio, says the study group—assisted by North Carolina's Research Triangle Institute under a $110,000 contract—plans approximately 15 visits over the next year to manufacturing operations in California, Texas, and a northeastern belt ranging from Boston to Pennsylvania. Boeniger said when asked for examples of potentially hazardous substances that **the arsenic in dust generated during the production of gallium arsenide light-emitting diodes might be harmful.**

# Washington commentary

## Stemming the U. S. decline in R&D

Over the next several years the Department of Defense will pursue force readiness—more money for pay, munitions, spare parts, and fuel, for example—at the expense of research and development, much of it in electronics. That is the disturbing forecast of the Electronics Industries Association in its latest look at the U. S. military electronics market over the coming decade (see p. 95).

The EIA judgment is one that coincides with the Aerospace Industries Association's latest examination of the national R&D decline, a trend that could prove disastrous for the national economy overall if allowed to continue. AIA's litany of the interrelated issues is by now familiar to industry: capital investment in technological progress is down; U. S. funding of R&D is lower than a decade ago, with no substantial growth in sight; and the number of scientists and engineers in proportion to the population is down, as is the number of patents issued to U. S. citizens.

Other indicators confirm the decline, such as a drop in the productivity growth rate and an overall negative balance of trade despite the positive contributions of high-technology products. The recitation recalls "The Decline and Fall of the Roman Empire," with Edward Gibbon's pronouncement, "All that is human must retrograde, if it does not advance."

### The U. S. has no policy

The AIA's valid conclusion that the United States has no long-range policy for R&D, innovation, and technology is one that deserves more attention than it has received, like similar warnings by other groups of industrialists, academicians, and professional societies in recent years. Although some citizens are misled by the fact that Federal R&D funds have recently been increasing in terms of current dollars, the national effort is actually declining in terms of inflation-adjusted dollars.

"Constant dollar figures," AIA says of Federal R&D, "show total funding in the last 10 years (fiscal 1972–81) to be 9% below the level of the previous decade. Instead of a steady upward trend, defense R&D has actually decreased 17% and the space effort is about half the total for the fiscal 1962–71 period."

Beyond calling for the establishment of a long-range national R&D policy—as a collaborative effort between the White House Office of Science and Technology, the National Science Foundation, and the Department of Commerce—the AIA also urges Federal rules that would permit formation of industry consortiums to develop international markets with high potential, without the threat of antitrust action. On the congressional side, AIA wants "full and stable" R&D funding levels based on a national policy, plus passage of a variety of legislative incentives for R&D that are also supported by other high-technology industries. Tax credits for R&D investment are, of course, at the top of the list of incentives (see p. 24).

### What industry must do

What is refreshing to some Government officials who have examined the new AIA study of America's R&D problem is, one points out, that "it calls for positive action by industry, too, and doesn't lay everything at Government's doorstep." Indeed, AIA does urge industry to increase its own R&D outlays as well as "increase capital investment to improve productivity, encourage innovation, enhance product quality, and lower unit cost, in order to be more competitive in world markets." It also recommends that manufacturers "promote and support more imaginative job-training programs—such as internships—to attract young people."

Perhaps the only option ignored is one that a number of electronics manufacturers favor—the provision of tax-free funds for encouraging more university R&D in either separate or joint efforts with corporations. Such a program would not only turn around declining student enrollments in technology but also diminish the number of university faculty departures for better-paying jobs in industry.

On the charge that America's decline in innovation is a product of "corporate short-sightedness," AIA responds that "the general economic climate certainly offers some rationale for defensive planning. In an uncertain domestic economic and political environment, a prudent businessman is forced to invest cautiously; that undoubtedly means a trend toward short-term investments for greater low-risk profits—and a de-emphasis on basic and exploratory research."

To break that trend toward pettifogging prudence, the nation does need the long-range national R&D policy, with appropriate industrial incentives, that AIA and others are calling for. But it also needs more in the increasingly competitive global marketplace if it is to maintain leadership. It needs to cultivate "the concept of a partnership between government and industry" that does not now exist. As developments in both Europe and Japan demonstrate, the time for more study has expired. **-Ray Connolly**

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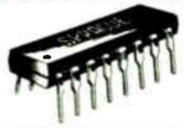
|  | UDN-6116A-2, 6126A-2 | 6 | + 60 V | 16 lead |
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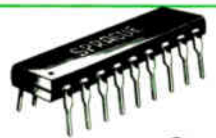
|  | UDN-6118A-2, 6128A-2 | 8 | + 60 V | 18 lead |
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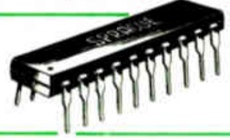
|  | UDN-6138A-2, 6148A-2<br>Split supply (+20 V, −40 V) | 8 | 60 V* | 20 lead |
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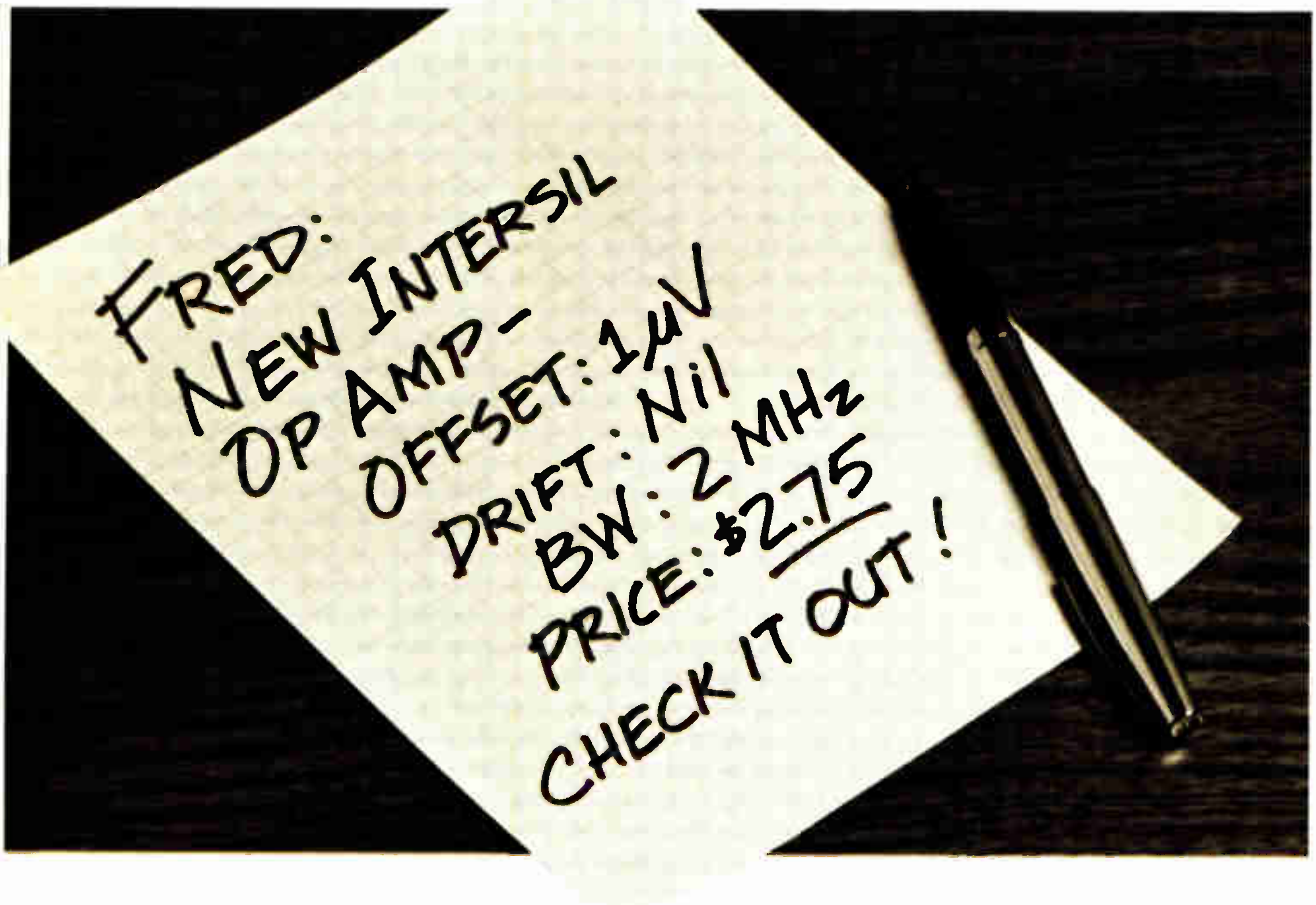


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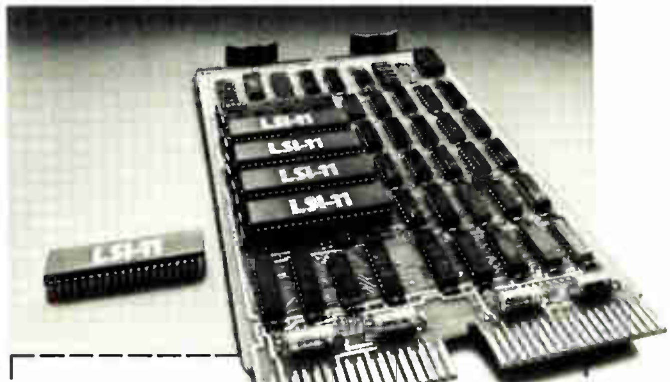


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An on-board sound generator and speaker provides aural feedback for key presses and may also be activated with escape sequences to provide an audio output.

The sealed keyboard surface, is spill proof and dust proof. This combined with high noise immunity CMOS circuitry makes the VP-3301 ideal for hostile environments.

Output is industry standard asynchronous RS232C or 20 mA current loop with six switch selectable haud rates and 8 selectable data formats.

The terminal can be connected directly to a 525 line color or monochrome monitor. Or to a standard TV set using an RF modulator.

For more information, contact RCA Microcomputer Marketing, New Holland Avenue, Lancaster, PA.

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** Available Dec. 1980

RCA

# International newsletter

**2-megabit capacity boosts yield of 1-Mb ROM from Japan**

The use of 100% redundancy has increased the yield of a 1-Mb Japanese read-only memory from 1% to more than 20%. The huge 31-by-19.2-mm (1,220-by-756-mil) device, developed by the Musashino Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp., will be used in a portable terminal that employs a 15-by-18-dot thermal head to print Chinese and other characters. Both the terminal and the ROM are made by Oki Electric Industry Co.

The ROM employs a double level of polysilicon and is programmed by the enhancement or depletion ion implantation of individual memory cells. In the memory matrix, 47 memory cells in series each share a source-drain region with an adjacent cell. The resulting device has an equivalent cell area of only 99 $\mu m^2$, dissipates only 420 mW for the entire chip, despite 8-$\mu$m design rules, but accesses in 12 $\mu$s. That slowness and its large size mean the device will probably be used only in **specialized applications like graphics displays, voice synthesizers, and dictionaries.**

**Bell Canada goes to market**

Plagued by problems with its regulatory agencies in the Canadian government and faced with strong competition by vendors selling equipment that connects to its lines, Bell Canada, much like its U. S. counterpart, has said that it is going to be an aggressive marketer. It has taken the first steps in that direction by establishing a subsidiary called Bell Communications Systems. **Customers will be able to buy new private-branch exchange and key equipment directly from the subsidiary,** which Bell says will be "totally independent and completely separate" from the parent.

**CAD begets filter-detector chip for System X**

A huge filter and detection circuit, one of the first examples of the computer-aided design of a telecommunications chip, will decode the Touch-Tone calls entering Britain's System X local exchange when it goes into operation at Woodbridge, Suffolk, later this year. Designed and fabricated by British Telecom, part of the British Post Office, at its Martlesham Research Centre, the silicon-gate MOS device uses 5-$\mu$m rules to pack 8,500 transistors into a 25-$mm^2$ (38,750-$mil^2$) area. It comes in a 24-pin dual in-line package and runs on a single 5-V supply. The second-order filter incorporates four 16-by-13-bit multipliers and is designed to handle System X's basic 64-b/s channel rate. However, **it is entirely general-purpose, as different multiplier coefficents may be programmed** into the external programmable read-only memory.

**Speech generator on a chip utters up to 32 words**

Watch for the ITT Semiconductors Group to announce at the Nov. 6–12 Electronica components exhibition in Munich a one-chip speech generator in silicon-gate n-MOS technology. Designated the UAA 1103, the device is mask-programmable for a vocabulary of up to 32 words in different languages, according to Intermetall GmbH, the Freiburg-based lead house of the group. With that vocabulary, it is **suitable for use in telephone-answering equipment, alarm systems,** and other gear to give short announcements and warnings—to car drivers, for example. By combining several complex methods of data reduction and by doing away with redundant circuitry, the Intermetall designers have accommodated 30 kilobits of memory as well as the control, decoding, and digital-to-analog conversion functions on a 31-$mm^2$ (48,050-$mil^2$) chip. The device operates off a 5-V supply and consumes about 25 mA. It will be available next year.

# International newsletter

**Spanish trains to show movies on TV screens**

Spain will be the first country to provide video-taped movies on trains. As part of its $17.5 billion 10-year modernization scheme, the Spanish National Railways (Renfe) has awarded a contract to Jusan SA, an affiliate of Rediffusion International Ltd., to install the video system on 1,000 coaches over a 5-to-10-year period. Jusan president Samuel Toledano estimates that it will cost $20,000 to equip each coach with **eight 16-in. color TV monitors suspended along the length of the aisle, plus a coupler for headphones in each armrest.** The image and sound source is a video cassette system plus audio amplifier. One prototype is now undergoing tests.

**LSI slashes cost of adapting VCR to record hi-fi music**

An adapter for recording extremely high-fidelity music in the video channel of standard consumer video cassette recorders will shortly be selling for about a third of its present $3,400 price in Japan. Hitachi Ltd. and Victor Co. of Japan cooperated on the design of a set of **five large-scale integrated circuits for pulse-code-modulation audio-signal processing,** and Hitachi has produced them. The complementary-MOS devices help cram the adapter onto a board about a fifth the previous size because they replace 500 to 600 small- and medium-scale ICs.

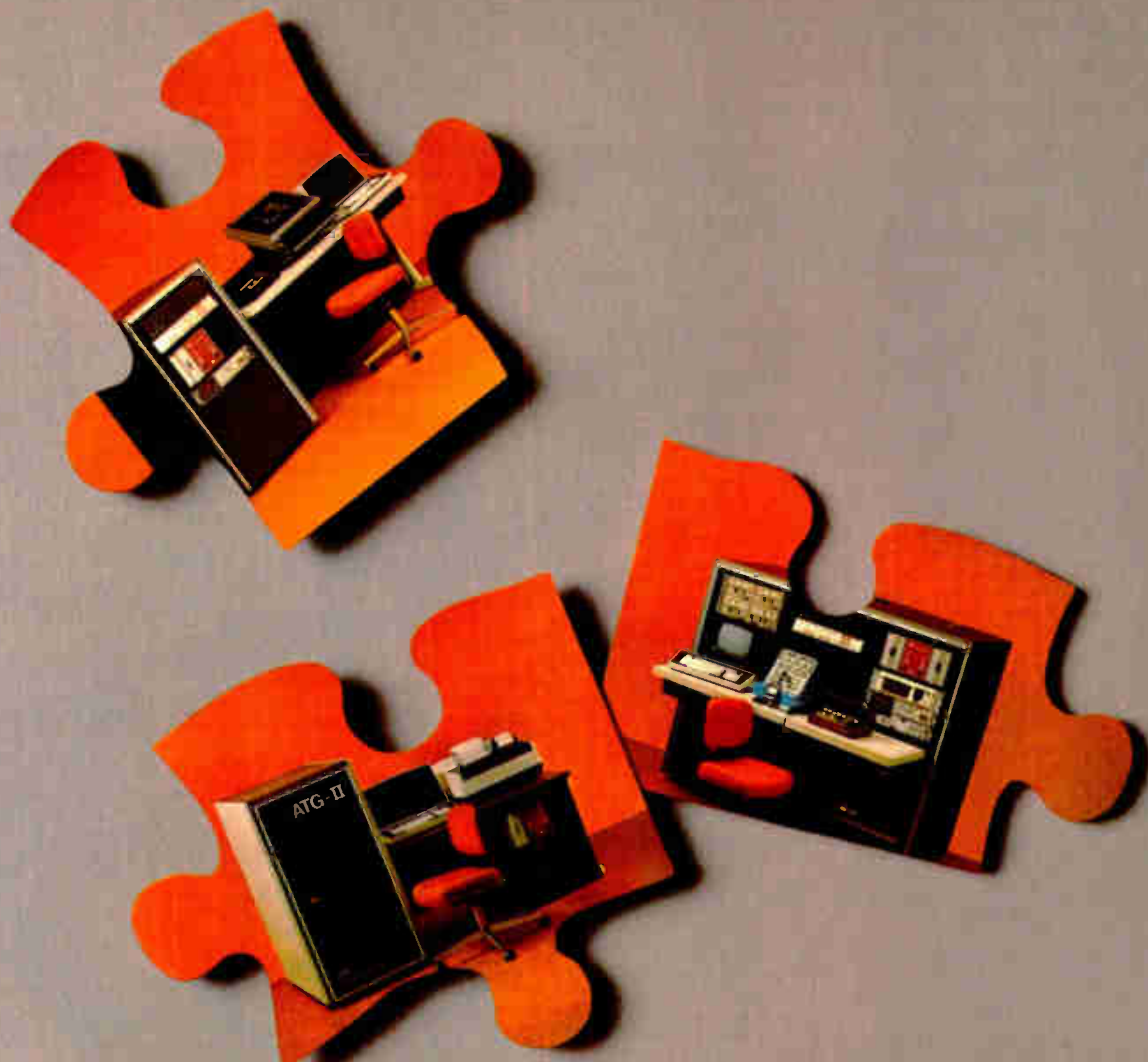
The PCM audio format standardized in Japan for video tape recording requires all this logic to compensate for the signal dropout experienced with VCRs. The technique has not been available to consumers before because it works only with a bandwidth as large as the video one.

**Flat-screen TV proves economical to manufacture**

Clive Sinclair's flat screen TV has moved a stage nearer to mass production following the successful demonstration in a pilot production line of the low-cost techniques involved in the manufacture of the miniature sardine-can–shaped cathode-ray tube [*Electronics*, July 19, 1979, p. 67]. But Sinclair's contract research company—Sinclair Research Ltd., Cambridge—has no plans to go it alone and will **likely seek a licensee to mass-produce it.** The U. S. watch manufacturer Timex Corp. is reportedly interested. The tube could form the basis of a paper-back-sized radio-TV combination with a 3-in.-diagonal black and white screen selling for approximately $200.

**Addenda**

Perhaps to enhance Japan's position in the impending talks with the U. S. on liberalizing Nippon Telegraph and Telephone Public Corp.'s procurement policies, NTT **has announced plans to buy at least 40 IBM 5280 data entry units.** Eventually it may buy up to 450 of the units, which will be imported through IBM Japan Ltd. . . . The French government is planning to enlarge its components plan, **the five-year, $180 million project designed to endow the country with a first-class integrated circuits industry.** An interministerial committee is deciding whether to add others to the five companies already involved or to boost government aid to those five. . . . **The first commercial satellite to move to the 14-GHz band** from the crowded 6-GHz one is the Canadian dual-bank Anik-B, which has just begun relaying TV programs to Quebec. . . . By adding **still-picture and slow- and fast-motion modes,** West Germany's Fürth-based Grundig AG has upgraded its version of the Video 2000 eight-hour video cassette recorder it developed with Philips. The Video 2×4 Plus, as it is called, will cost about $85 more than the earlier Video 2×4.

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Circle 67 on reader service card

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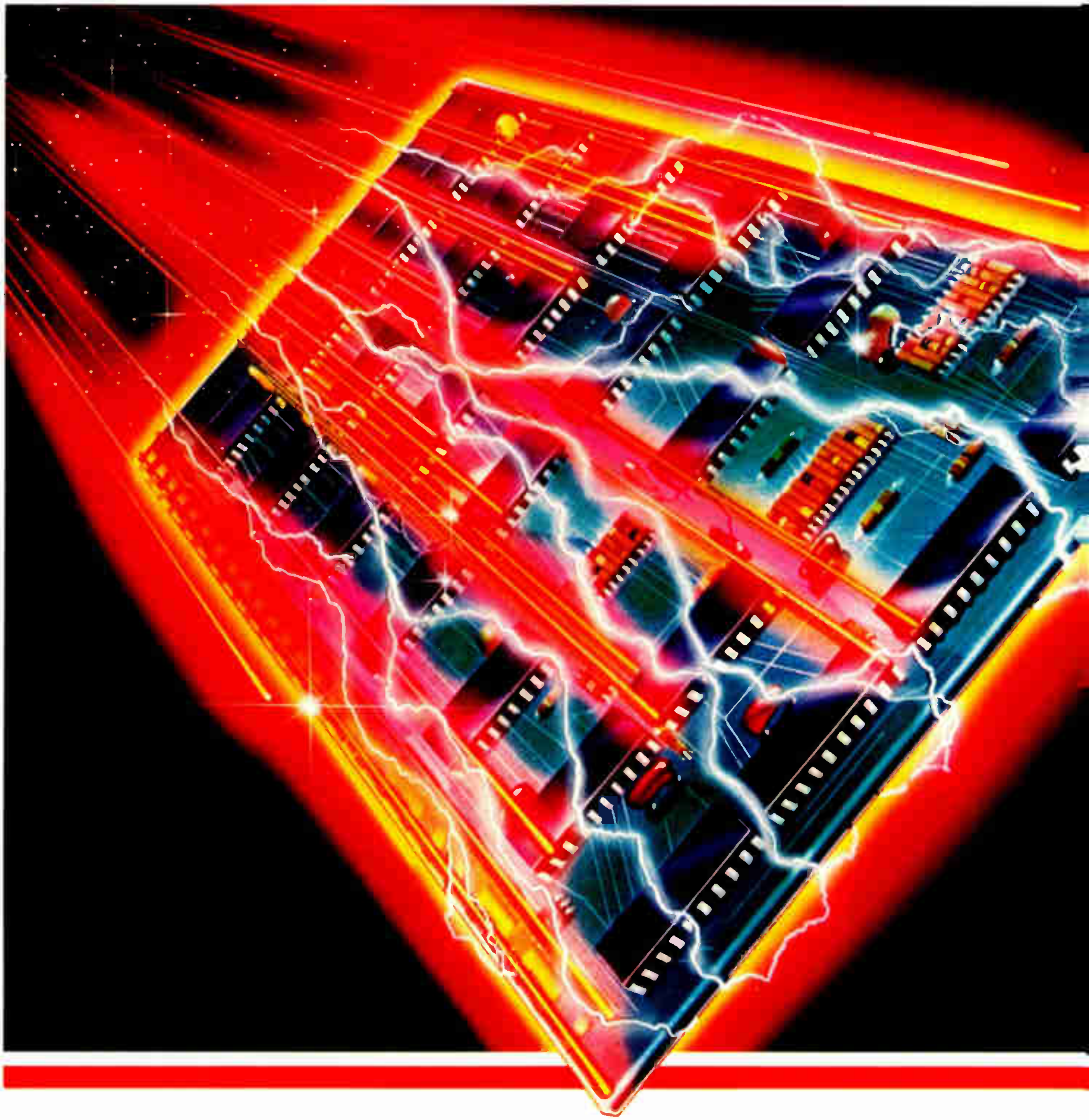

# We have the fastest circuits

# Graphics on the powerful computers: a fast way

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For example, our top-of-the-line 9800 Series System 45C includes a greatly enriched graphics language that lets you manipulate 4,913 shades of color with remarkable ease. A light pen and high-performance digitizer give you flexible options for entering data. And 3-D rotations allow you to view objects on the CRT from any desired angle.

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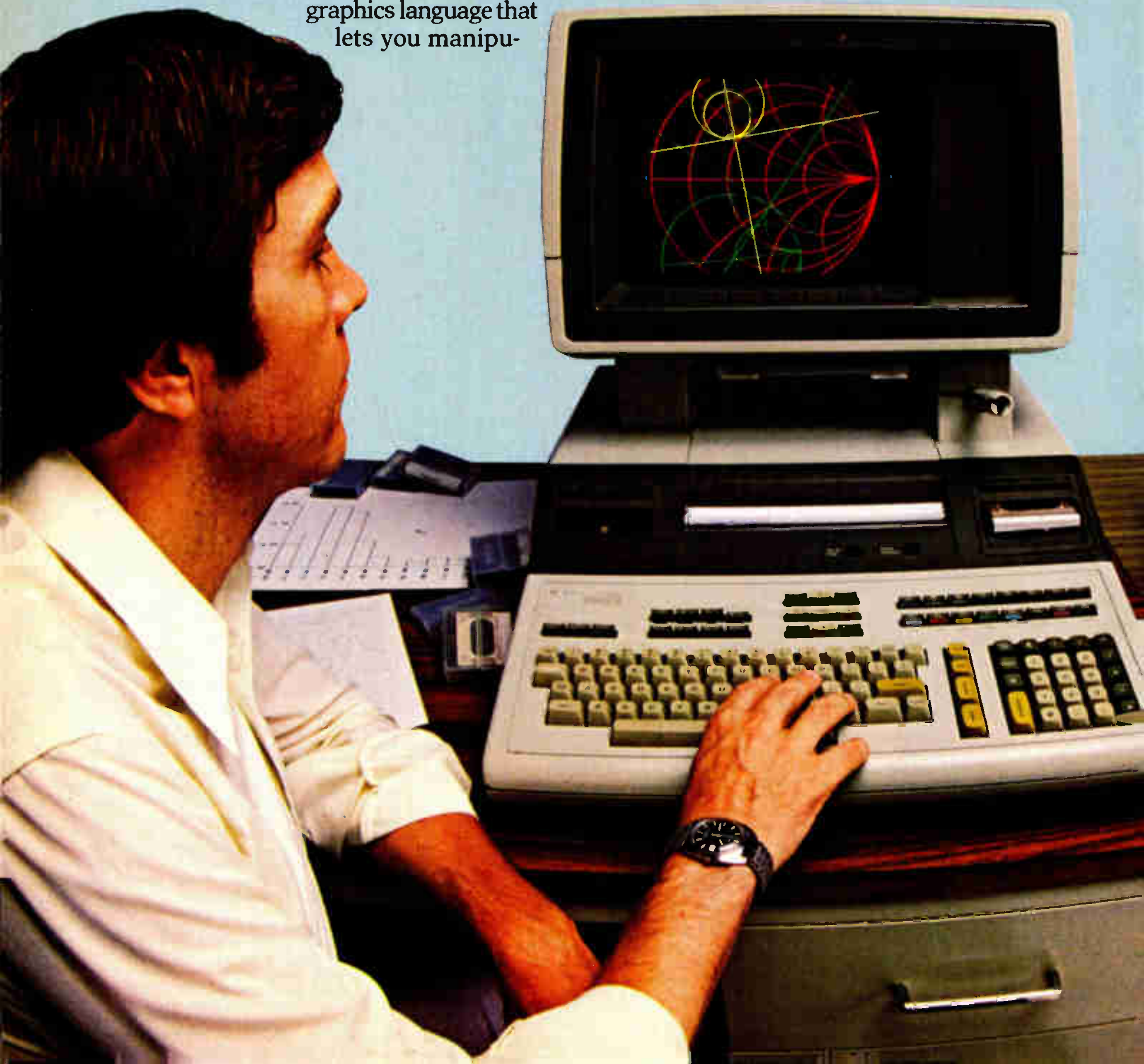

# HP Series 9800 desktop to focus on the facts.

HP 85, also provide advanced graphics software. And when you add an input peripheral and our four-color plotter, you've got a full-function graphics workstation—a completely integrated computing system that operates under your own personal control.

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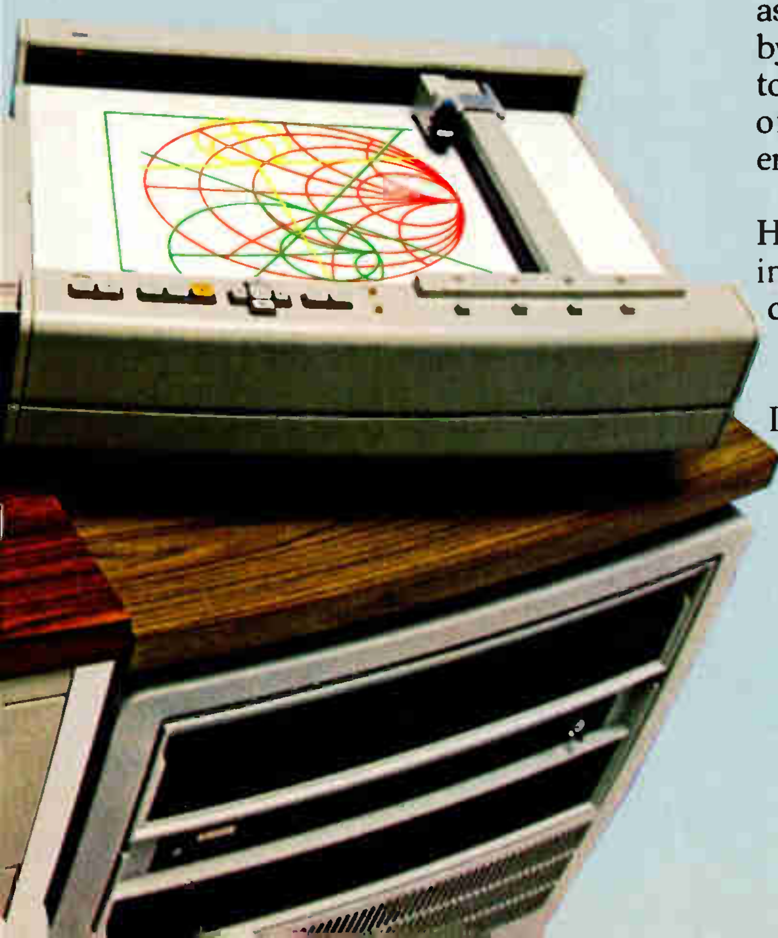
To compliment graphics capability a powerful data base management package on the disc-based System 45 models, you can store, retrieve, sort, modify and analyze large amounts of technical data—quickly and efficiently. User-addressable memories to 449K bytes give you plenty of room for complex manipulations. And hooking up to measuring instruments is a simple matter of choosing from among four protocols available: HP-IB, Bit-Parallel, BCD or RS-232-C.



## As friendly as ever.

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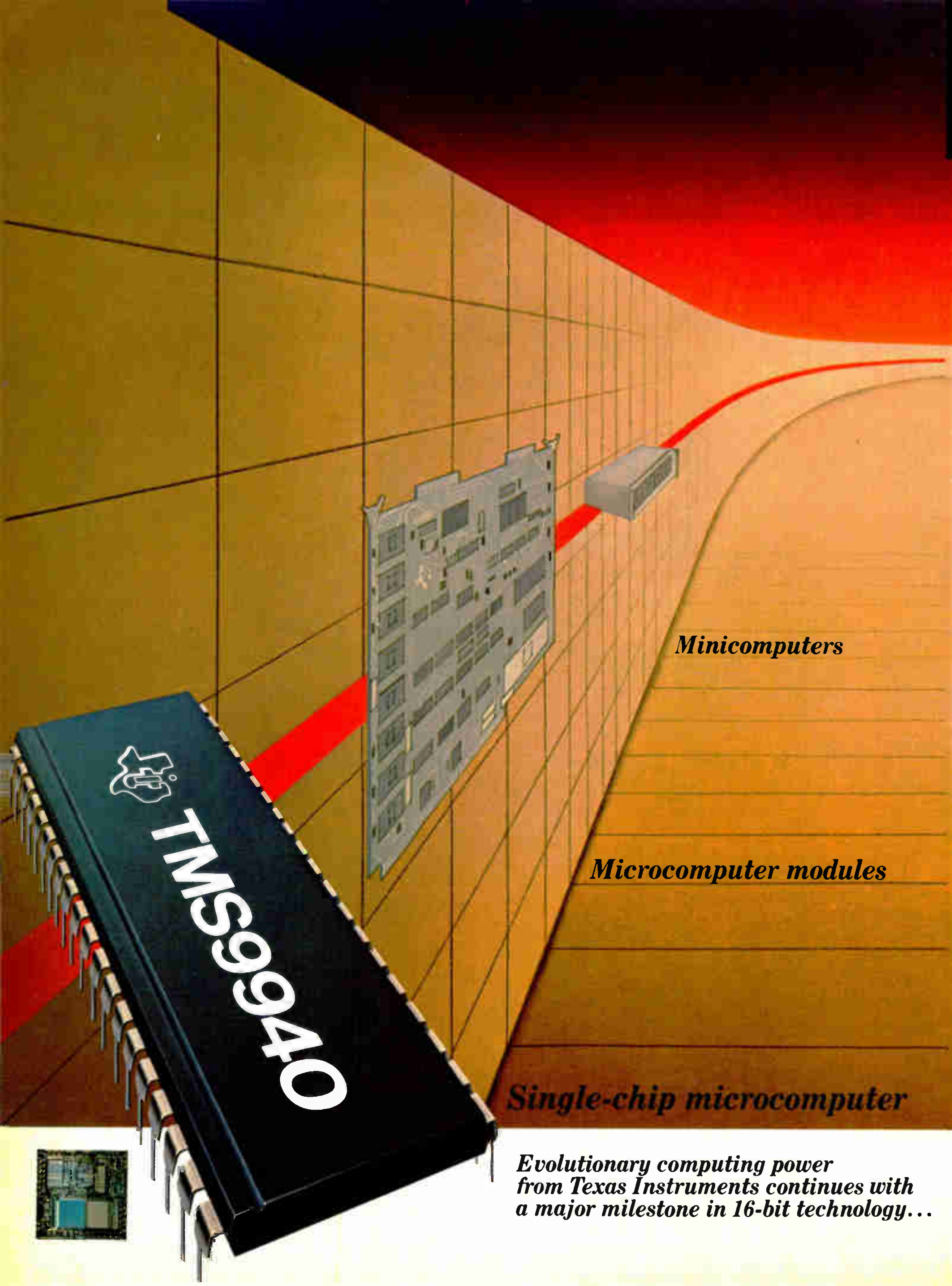
Circle 71 on reader service card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from Texas Instruments continues with
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# TMS9940
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TI's 9900 Family is the *only* family that maintains architectural and software compatibility from single-chips to multi-chips to modules to systems — all the way to the object code level.

With the TMS9940, Texas Instruments brings you high-volume, cost-effective solutions to tough system design problems, combining the computing power of a multi-chip 16-bit system with the reliability and compactness of a single-chip solution.

With its high-speed processing, bit I/O, and advanced memory-to-memory architecture, the TMS9940 offers computation power unequalled by any other single-chip product on the market, while retaining the programming ease of 16-bits.

## High-speed number crunching and bit I/O

Powerful instructions — like BCD add, BCD subtract, 16-bit multiply with 32-bit results, and compatible divide — provide a number-crunching capability unsurpassed by any single-chip product.

Thirty-two on-chip, flexible, individually configurable input/output bits are addressable for manipulation by powerful bit I/O instructions.

I/O expansion modes permit up to 256 bits of external I/O to be added, allowing easy interface to 9900 Family peripherals and most industry peripherals.

## Advanced memory-to-memory architecture

Advanced memory-to-memory architecture makes the TMS9940 ideal for interrupt-driven and extensive I/O applications.

This innovative architecture features multiple register files that provide ease of programming and unsurpassed interrupt response time.

The TMS9940 memory consists of 128 bytes of RAM and 2048 bytes of ROM. Other features include 4 levels of interrupts, plus an internal decrementer which can be programmed as a timer or event counter.

**TMS9940 — Key Features**

- 16-bit instruction word
- Instruction set includes 16-bit multiply and divide, BCD add and BCD subtract
- 128 bytes of RAM on chip
- 2048 bytes of ROM (or EPROM) on chip
- 64 general-purpose 16-bit registers
- Program execution from RAM or ROM
- 4 prioritized interrupts
- On-chip timer/event counter
- 32-bits integral general-purpose I/O bits — expandable to 256 external I/O bits
- 4 MHz crystal operation — up to 117,000 interrupts per second
- 5-volt MOS technology
- Offered in a 40-pin, 600-mil DIP

## Here-and-now availability

Perhaps just as important as the unmatched capacity for design flexibility, the 9900 Family is here-and-now and readily available. It's the lowest cost 16-bit CPU family. And proven where it counts most. In the marketplace. The choice of hundreds of companies for a wide range of systems and end products.

Microcomputers mean high volume and TI has unequalled production capacity and experience. In fact, TI is the largest supplier of single-chip microcomputers and has shipped more than the next two suppliers — combined.

## 9900 Family development tools

Reliable, available, economical development systems designed to boost programmer efficiency and cut costs.

**The AMPL* prototyping lab:** A complete set of the software and hardware development tools for the TMS9940 as well as for other 9900 Family CPUs. The AMPL system provides a real-time TMS9940 emulator and a logic-analyzer function to solve complex programming and hardware debug problems.

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## Leadership staying power

TI has paced the industry through generations of semiconductor innovation, pioneering the lion's share of major milestones.

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The continuing introduction of new, advanced 9900 Family CPUs, with TI's state-of-the-art technology and proven production resources, demonstrates TI's total commitment to 16-bit leadership.

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**For more information** about the TMS9940, or any other 9900 Family member, contact the TI field sales office nearest you. For details and specifications, write to Texas Instruments Incorporated, P. O. Box 1443, M/S 6404, Houston, Texas 77001.

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Circle 73 on reader service card

# The power is with a new 16-bit SOS microprocessor

*by Charles Cohen, Tokyo bureau manager*

Silicon-on-sapphire technology, hardware functions, two internal buses, enhance throughput

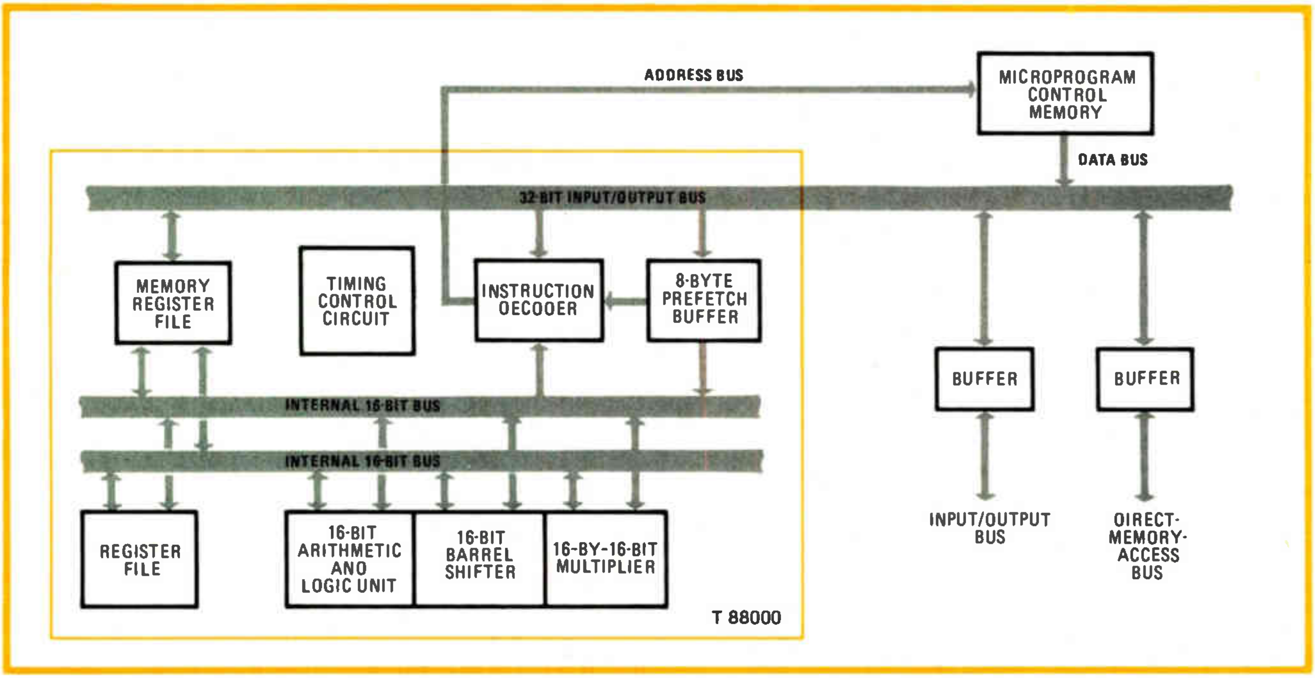
**Mixed calculations done** with three to six times the speed of Intel's 8086 or Zilog's Z8000—that's Toshiba Corp.'s claim for its new 16-bit T88000 microprocessor. The use of silicon-on-sapphire technology, which reduces the average propagation time of a gate to a mere 0.7 nanosecond, contributes to some of that computing power, and a multiplicity of hardware features supplies the rest.

Two internal parallel 16-bit buses roughly double the processing speed possible with a single bus. The 32-bit input/output bus can be used in both time- and space-multiplexed fashion to increase throughput. Furthermore, an 8-bit buffer can store instructions prefetched from main memory—a desirable feature because it makes pipeline execution possible.

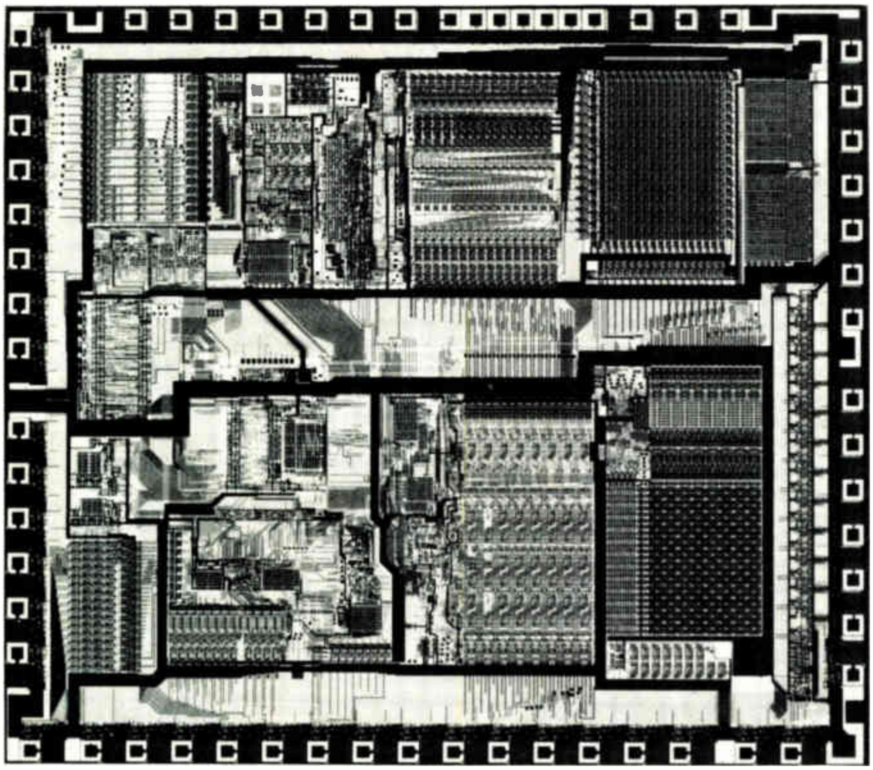
Moreover, instruction execution speed is enhanced by performing many functions not in software but in hardware, including floating-point and decimal processing. The chip features a hardware 16-by-16-bit multiplier that can perform fixed-point multiplications in 1.6 microseconds, or four machine cycles. The built-in barrel shifter provides 1-to-15-bit shifts in only one machine cycle, or 400 ns.

Moreover, because most of the 151 user instructions are completed in one machine cycle, the processor can also perform conditional branches in as little as one machine cycle, although some take up to four machine cycles.

**Lots of software.** Unlike many recently introduced microprocessors, the Toshiba device has available a large library of software, because it is compatible with the company's series 7 minicomputers. But its application capabilities go much further than the series 7's, and it will be used in a wide spectrum of other applications, including small-business computers and equipment, ter-




**Master of many trades.** Toshiba's 16-bit microprocessor owes much of its computing power to hardware features like two internal buses and a 16-by-16-bit multiplier. It is also versatile: different microprograms stored in its external ROM readily adapt it to different applications.



**Not speed alone.** Silicon-on-sapphire technology makes the T88000 easier to fabricate: 3.5-$\mu$m rules are adequate, and fewer masks are used than for bulk-silicon devices.

minals and other peripheral equipment, and industrial applications such as single-board computers.

Toshiba expects to be able to optimize the same chip for all these different applications because the T88000 is designed for microprogrammed instruction control—the microprogram resides in 80-K of standard external read-only memory. Prototype systems use six chips of 16-K capacity, but production systems will be supplied with three 32-K devices.

**C-MOS and n-MOS.** The new microprocessor has about 12,000 gates, almost equally divided among n-channel MOS gates, where speed or density is required, and complementary-MOS gates elsewhere. The high speed of the SOS process made it possible to design this device with 3.5-micrometer lithography rules and fabricate it using conventional unity-magnification full-wafer projection equipment.

For the same speed, a similar device on bulk silicon would need less-than-2-$\mu$m rules and be much more difficult to fabricate. It would require higher-precision lithography than the Toshiba device and more masks, because the SOS design requires neither channel stoppers nor p wells. Worse yet, the bulk device would probably eat up something like 3 watts rather than the 700 milliwatts of the SOS device.

The device is fabricated in a 0.6-$\mu$m-thick epitaxial layer on the sapphire substrate. To stop leakage current in the interface region, the epitaxial layer has been given a deep implantation. To achieve a higher breakdown voltage, the surplus silicon between transistors is converted into silicon dioxide.

The n-MOS transistors are given four different threshold voltages by receiving two different ion implantations, one or other of the implantations, or neither of them. Silicon gates are used, but interconnection resistance is not the problem it is in memories because long connections are made in the aluminum level of interconnection. There is also a diffusion interconnection level and a polysilicon-gate one, making three levels in all.

## France

# Gallium arsenide to yield 5-GHz divider

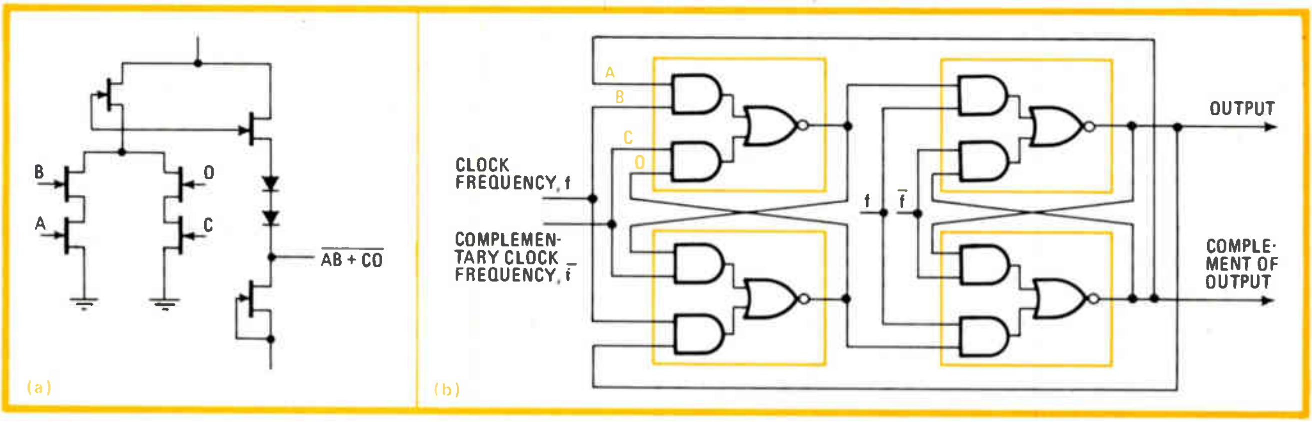
Researchers at the main Philips group laboratory in France believe they have got what may well be the fastest frequency divider around. The gallium arsenide device developed by a team at the Laboratoires d'Electronique et de Physique Appliquée in the Paris suburb of Limeil-Brévannes should prove capable of performing binary frequency division from dc up to more than 5 gigahertz. What's more, the LEP researchers have placed a clock generator and complementary clock generator on the same chip—which means that the only input needed is the frequency to be divided.

"For the moment, we have not optimized the two elements [the logic and the clock], so that the entire chip now functions at a maximum frequency of 3.5 GHz," explains Jean-Paul Hurault, scientific director for the LEP's solid-state physics department. "But we are confident we will be able to optimize the circuit up to 5 GHz."

The basic logic gate in the frequency divider differs little from the buffered field-effect-transistor logic gates developed elsewhere, notably by Hewlett-Packard (see circuit diagram). What makes the LEP version special is the fact that it has been done in planar self-aligned technology with a standard photolithographic process. The active layer is made by implanting selenium ions directly into a gallium arsenide substrate. There is no need for a buffer layer.

"Typical design rules are gate width of 1 micron, with 3 microns between source and drain," says Marc Rocchi, an engineer on the design team. Using the GaAs techniques it has devised, the lab has managed to get actual gate width down to 0.6 micrometer with 1.9 $\mu$m source-drain spacing.

The buffered-FET gate, sometimes known as a multiplexing gate, has four inputs (ABCD in the circuit




**All together now.** Basic to a frequency divider capable of handling up to 5 GHz is a buffered FET gate shown in the circuit diagram (a). Four of them, linked as shown in the logic diagram (b), fit on one gallium arsenide chip together with a clock.

diagram), and four of the gates are arranged in a gated master-slave flip-flop configuration (see logic diagram). The clock frequency is the frequency to be divided and is the input to the pair of AND gates in the master. The complementary clock frequency (f in the diagram) controls the slave. The AND gate controlled by the complementary clock frequency ($\bar{f}$) in the master ensures a correct counting sequence when the clock frequency switches from high to low.

The pair of AND gates controlled by the clock frequency in the slave fulfills the same function for the complementary clock frequency. The typical logic-gate propagation time is less than or equal to 100 picoseconds. And the power consumption is 40 milliwatts per gate, for a total consumption of 160 mW.

"We believe we could reduce dissipation to 5 mW per gate," says Rocchi, "but we would of course lose some speed." The LEP researchers feel they could build a frequency divider that would operate at 3 GHz with a total power consumption of 20 mW. "The technology is fine for medium-scale integration," comments Hurault. "But it is not good enough for very large-scale integration, because the consumption is simply too high." That explains why the LEP researchers are now turning toward a nonplanar technology—specifically, recessed Schottky gates. In fact, their first circuit using recessed gates will be a frequency divider. **-Kenneth Dreyfack**

## Great Britain

# Adaptive echo canceler helps modem run at 9,600 b/s on noisy phone lines

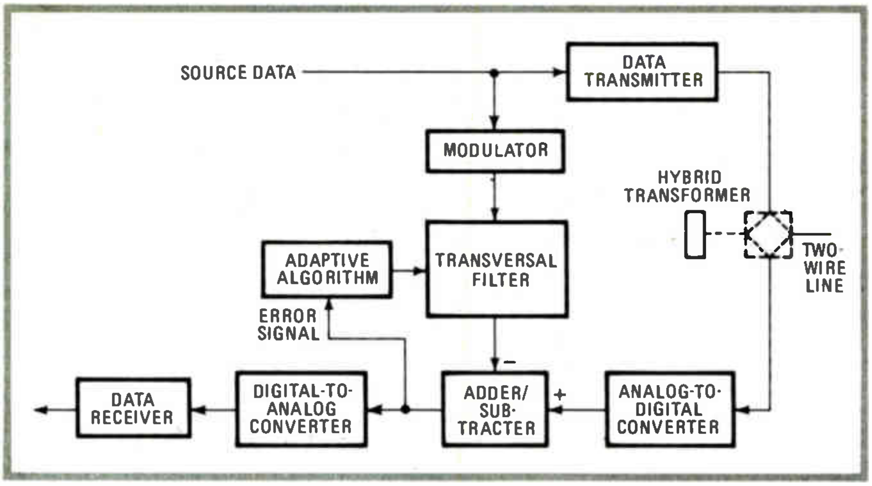
Envisioning a future abuzz with packet switching, digital facsimile, slow-scan television, and other digital services, British Telecom, part of the British Post Office, wants to be able to transmit data at high speeds anywhere over the public telephone network. To this end, its Martlesham Research Centre is developing a 9,600-bit-per-second modem that will double the data rate at present available and use large-scale integration to keep its cost low.

In terms of the two-wire 3-kilohertz standard phone connection, 9,600 b/s is a high speed, attained only by the use of advanced signal-processing techniques like adaptive echo canceling, say the center's engineers. In contrast, they note, commercially available modems with the same transmission rate require high-grade four-wire leased circuits, while those operating at 48 and 56 kilobits per second take up an entire group-band circuit from 60 to 108 kHz—enough for 16 speech channels.

The new modem incorporates an adaptive line equalizer that can compensate for poor-quality lines and prevent intersymbol interference. The technique is powerful: Plessey Digital and Network Systems Ltd. employs it in its new 16-kb/s modem for use on four-wire leased lines. But for two-wire operation and to cope with worst line conditions, adaptive echo cancelation is also necessary.

**Answering echoes.** In two-line operation, a hybrid transformer in the modem separates the transmitting and receiving paths, and discontinuities and mismatches between the transformer and the line cause talker echoes that can swamp the incoming signal. One solution is half-duplex operation, in which each end talks in turn, but that halves the data rate. The post office therefore employs an echo canceler network (see figure). The net's output models the echo response of the two-wire connection and, when subtracted from the line signal, removes the echo.

Precision digital signal processing is needed to achieve the 60-decibel echo suppression required. Conventionally enough, British Telecom employs a transversal filter that, to avoid aliasing distortion, has a sampling rate double the highest frequency present in the signal spectrum. Less conventionally, it implements the circuit in custom LSI. To cut chip complexity, the filter sampling clock is locked to the transmit clock and is a simple multiple of it. As a result, the amount of signal




**Canceled.** British Telecom's modem uses a hybrid transformer to split incoming from outgoing data. Echoes that result are copied by this circuit and subtracted from the signal.

processing may be considerably reduced by driving the canceler directly from the source data.

For use on the switching phone network, the canceler must be adaptive, and an algorithm has been developed for this purpose. The circuit can cancel echoes having up to a 20-millisecond delay.

Custom LSI appears throughout the modem. It uses the Martlesham center's 5-volt silicon-gate n-channel MOS process with 6-micrometer design rules. Samples of the first chip have already been received, and delivery of all seven LSI circuits plus two shift registers is targeted for the end of 1981.

**Good grades.** Trials have already been carried out on the phone network with a prototype system using two- and four-wire connections. They were almost entirely successful. In only 3 of the 133 line tests were there residual uncanceled echoes, and these, believes British Tele-

## Around the world

**VHS video cassette system wins another convert**

Victor Company of Japan says that its VHS video cassette récorders have been officially adopted by Standard Electrik Lorenz and will be supplied the West German firm on a private-label basis. Other non-Japanese firms that have private-label or technical assistance agreements with Victor include Saba-Werke GmbH, Norddeutsche Mende Rundfunk AG, and Telefunken Fernseh und Rundfunk GmbH in West Germany; Thomson-Brandt in France; Thorn Consumer Electronics Ltd. in the UK; Rank Industries Australia Pty in Australia; and Grupo Industrial Alfa SA in Mexico.

**Ferranti trades micropackaging for V-MOS technology**

Add another name to the growing list of semiconductor companies moving into the V-MOS power field-effect-transistor market. Through a marketing and technology exchange agreement with V-MOS manufacturer Supertex Inc. of Sunnyvale, Calif., Britain's Ferranti Electronics Ltd. is to diffuse, assemble, and test n- and p-channel discrete power FETs with a vertical double-diffused MOS structure for sale in Europe and the U. S. It will introduce its first branded parts at the Electronica exhibition in Munich in November. In the deal, which involved no transfer of money, Ferranti traded in its microminiature packaging technology for discrete devices. The technology competes with Siemen's Sipmos and International Rectifier's Hexfet proceses, among others, for high-speed, high-power applications in the industrial and consumer sectors.

com, could certainly be remedied by an improved version of the echo canceler. **-Kevin Smith**

## West Germany

# Siemens aiming to sell more ICs abroad

The opening of yet another MOS fabrication center at Siemens AG's Munich-based components division is further evidence of the West German firm's determination to become a powerful force on the international market for very large-scale integrated circuits. Right now, it rates as the No. 2 IC supplier in Europe (after Philips of the Netherlands) and as No. 10 worldwide.

The new VLSI center, together with a similar one now nearing completion at Villach in Austria, "is to help Siemens stand up to the mighty competition of Japan and the U. S.," says Friedrich Baur, head of the components division and a member of the company's managing board. More than that, he is convinced it will help shift IC market shares from those countries to West Europe. The new Munich facility is equipped to fabricate devices with 2-micrometer geometries and 150,000 components per chip [*Electronics*, Sept. 25, p. 63].

**Above average.** Adds Gernot Oswald, sales and marketing manager for ICs and head of microcomputer activities at Siemens, "We are aiming to grow more rapidly in ICs than the world average, and the additional percentage points we will have to get abroad because our share of the West German market allows only moderate gains." In 1979 Siemens had a roughly 20% share of that market and a 12% share of the West European one.

Favoring its IC sales growth in the rest of Europe, Baur believes, is steeper expected growth of the equipment production industry there, plus the fact that ICs as yet pervade systems and equipment to a far lesser extent in Europe than in the U. S. **-John Gosch**

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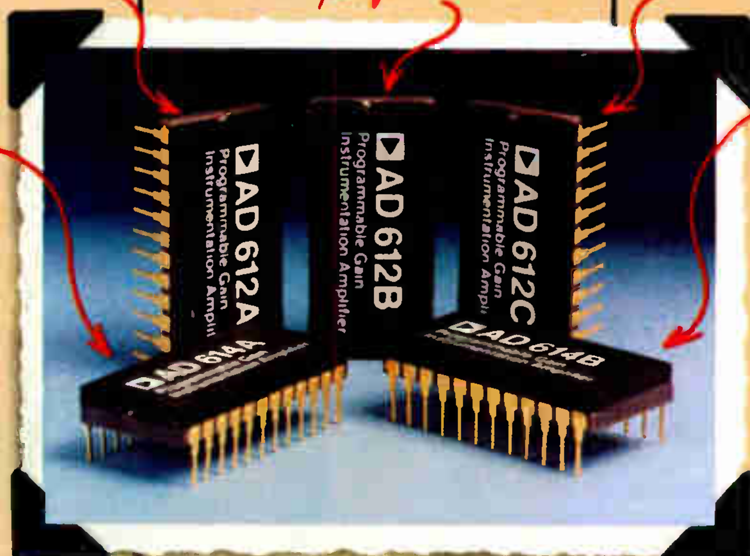


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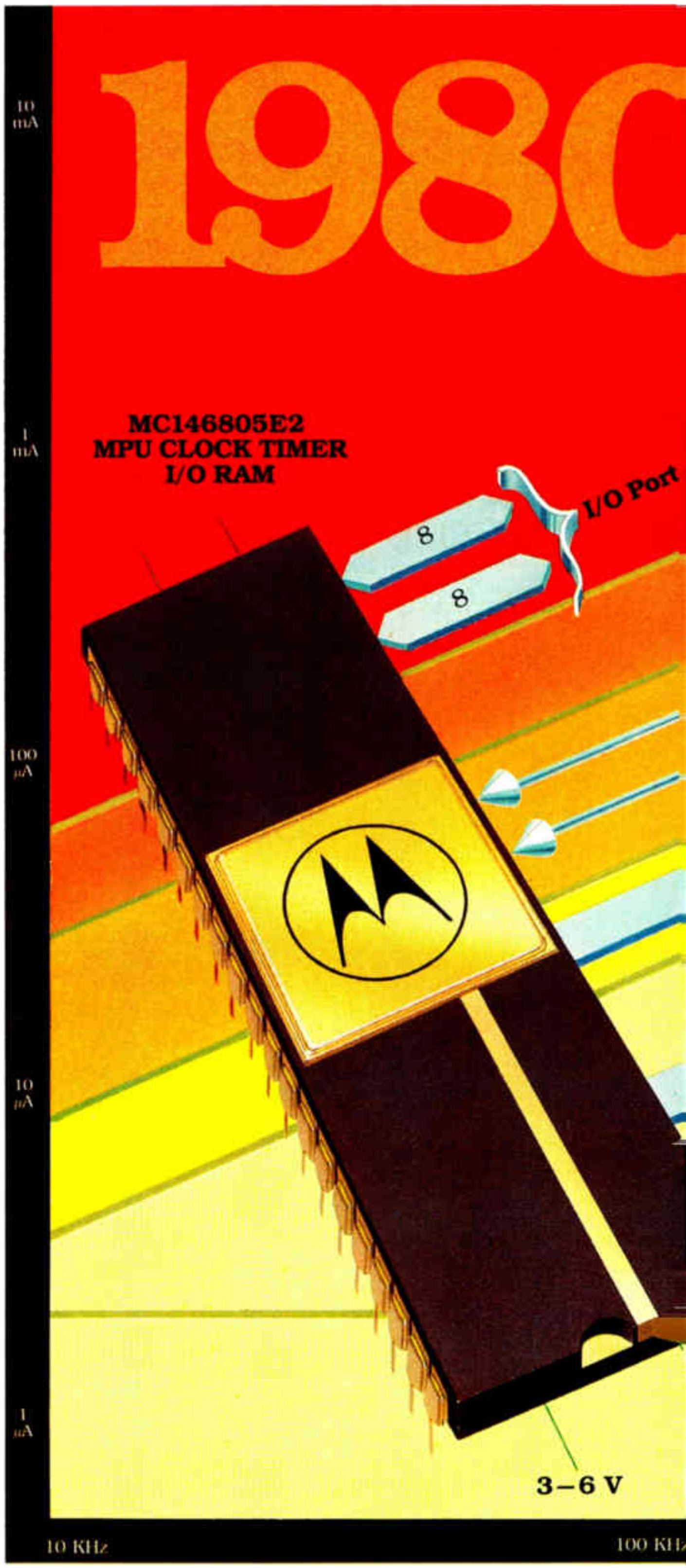


The MC146805E2 is the first CMOS microprocessor for the new era of the '80s, a merger of Motorola's strengths in microprocessors and CMOS standard logic.

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The MC146805E2 is more than a powerful 8-bit CMOS processor. Also on-chip are two 8-line I/O ports, 112 bytes of RAM, an oscillator and a programmable 8-bit timer with a 7-bit prescaler. A multiplexed address/data bus permits addressing up to 8K bytes of external memory. For implementation of real-time applications, the MPU operates with two hardware interrupts, timer underflow and an external signal, plus a software interrupt.

The MC146805E2 is fabricated in silicon-gate CMOS to match NMOS speeds— 1 MHz cycle (from 5 MHz oscillator). Power is still conserved with anticipated CMOS efficiency. Typical full-speed power consumption is less than 20 mW, and in standby is less than 100 μW.

Two power-saving, software initiated standby modes, STOP and WAIT, are used in the MC146805E2. In STOP, all internal processing and the timer are halted for the lowest possible power consumption. In WAIT, the timer is allowed to count in a normal sequence and power use is greater than in STOP, but still an order of magnitude below that of the operating mode.

Efficient use of program space, bit manipulation, memory mapped I/O and versatile interrupt handling are just a few of the programmable features of the MC146805E2. Single instructions modify any RAM bit or I/O pin. Even more unusual are single instructions which branch on the condition of any such bit. Three program-efficient indexing modes allow single-instructions access to memory tables. All of the powerful memory reference instruction functions of the MC6800 are incorporated into the MC146805E2.

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Complementing the MC146805E2 is Motorola's MCM65516 mask-programmable, byte-organized 16K CMOS ROM designed for use in multiplexed bus systems. The small 18-pin package is a tidy space saver, too. Like the MPU, the ROM also is in volume production.

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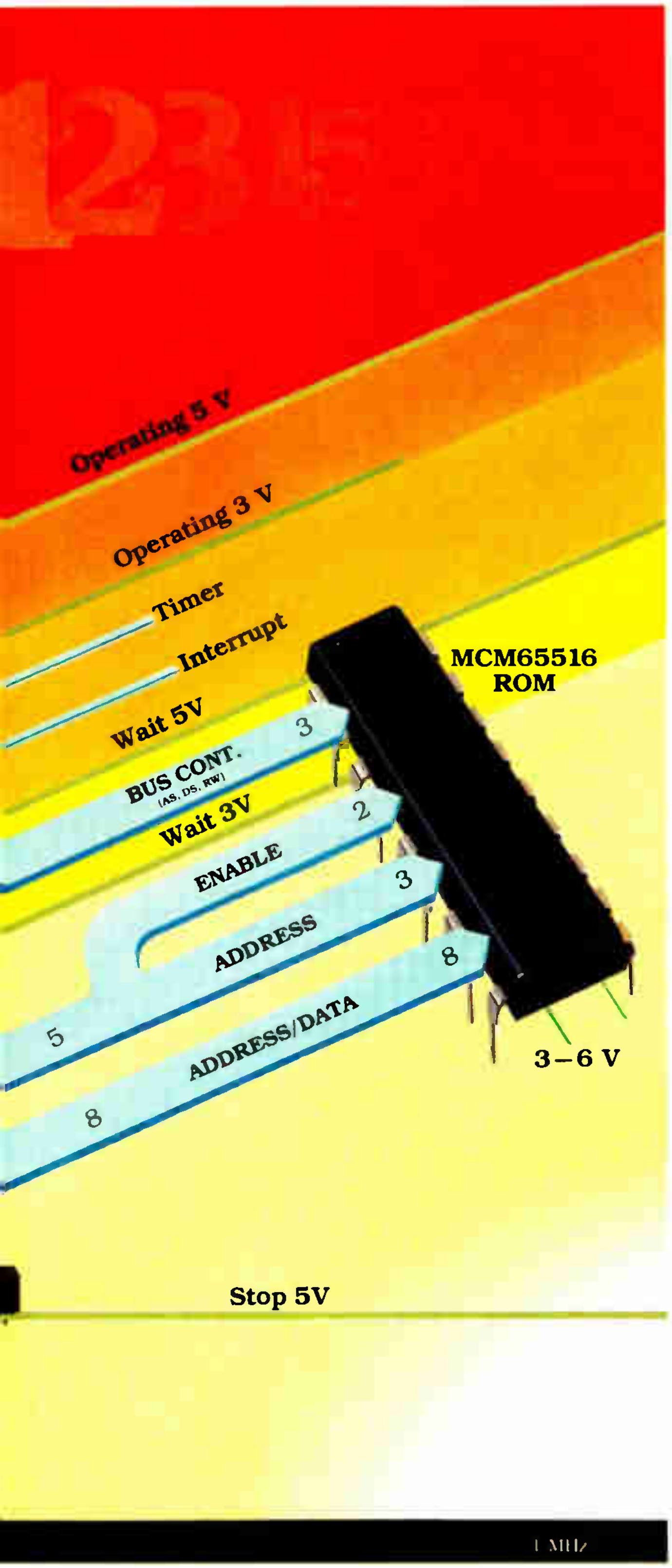


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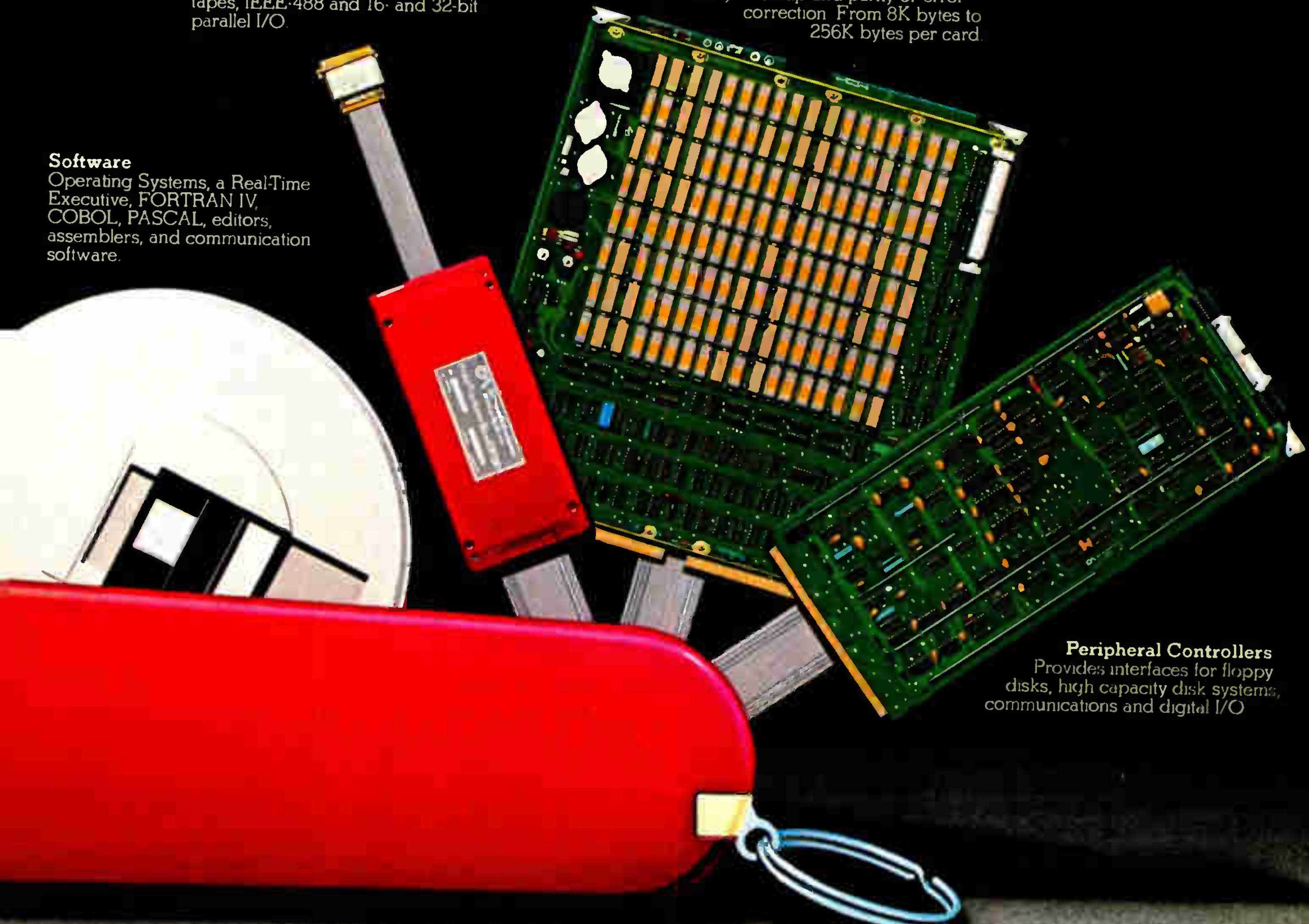


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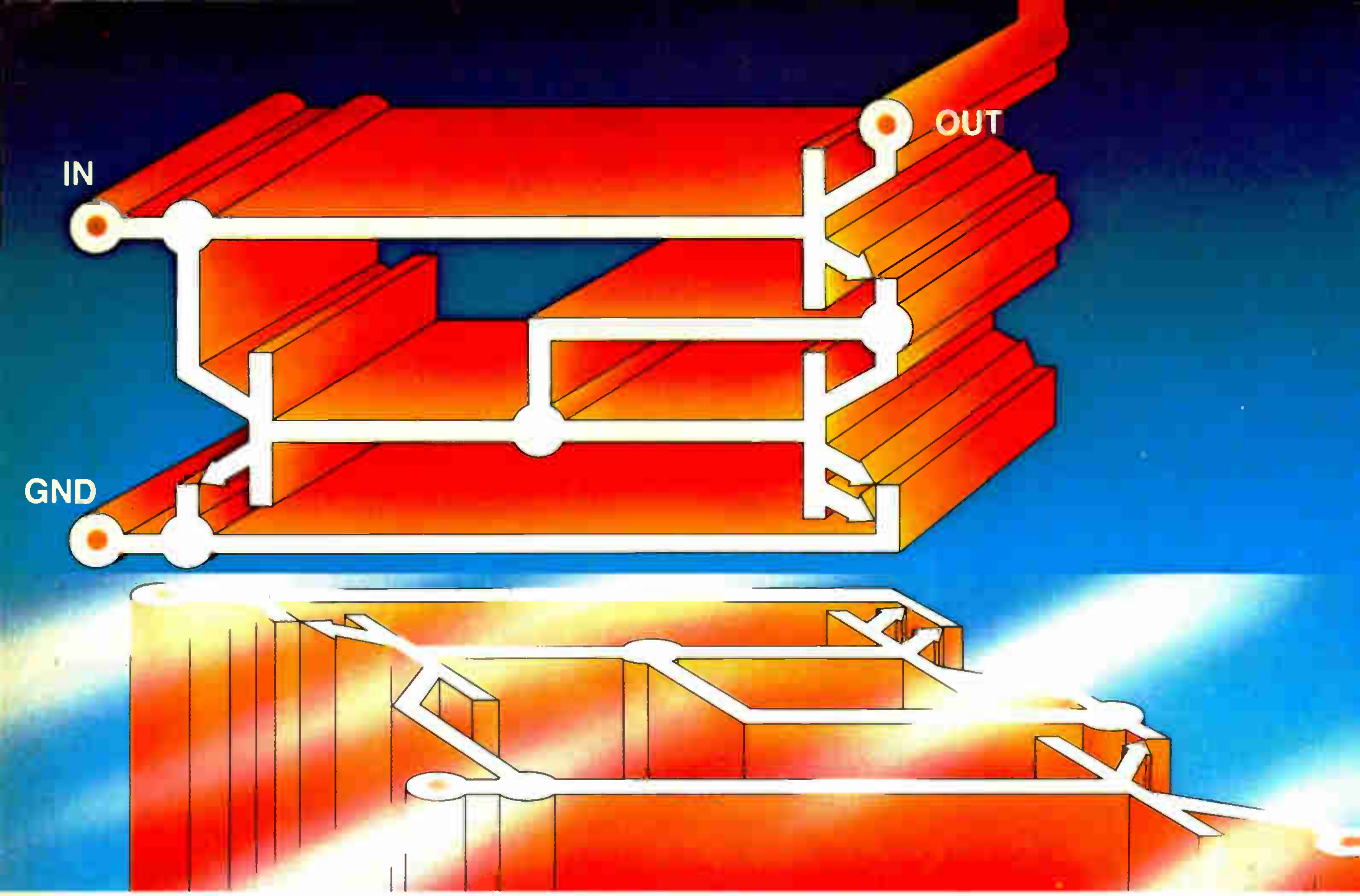


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# Meter makers see market in optics

This month's first-ever meeting devoted to fiber-optic measurement indicates that industry is finally moving toward standards

by Richard W. Comerford, Test, Measurement & Control Editor

As the **engineering** and scientific communities near agreement on how to characterize fiber-optic links, instrument makers have their antennae out. With the prospect of low-cost fibers, sources, and detectors with increased telecommunications applications, they anticipate the development of a sizable market for instruments that will measure attenuation, the ratio of incident to reflected signal, bandwidth, and possibly core diameter and numerical aperture. Indeed, some small companies have already committed themselves.

A milestone is an upcoming meeting, the first dedicated to fiber-optic measurement. Called the Symposium on Optical Fiber Measurements, it will take place in Boulder, Colo., Oct. 28–29. The organizers—Douglas Franzen of the National Bureau of Standards with the aid of the Optical Society of America and the transmission systems subcommittee on fiber optics of the Institute of Electrical and Electronics Engineers—have attracted a roster that is a who's who of telephony.

Papers will be presented by representatives of Nippon Telegraph & Telephone Public Corp.'s Yokosuka Electrical Communications Laboratory, the Netherlands Postal and Telecommunications Laboratory, British Telecom Research Laboratories, Bell-Northern Research, and Bell Laboratories. In the words of one participant, the symposium will bring together "the top people in the world in fiber optics."

These will include representatives of some of the major standards groups: the International Electrotechnical Commission, the International Consultative Committee for Telephony and Telegraphy, and the Electronic Industries Association. The upshot, says Roy Love, will be the emergence of a standard approach for measurements of multimode fibers. Love is chairman of the EIA's P6.6 group, which is working on such standards.

**Name it.** According to Love, one of the fundamental debates in fiber-optic measurement is over whether to measure waveguide properties like scattering and absorption or some other property that would yield data more vital to the user. "What we are beginning to want now," Love believes, "is just to measure a number and call it attenuation." The major criterion for that number is that if a series of cables is concatenated—or linked—the attenuations of the individual cables add up to the concatenated attenuation. "That thought may seem obvious," Love agrees, "but, though in the background all the time, it has really just begun to crystallize."

Round-robin tests conducted by the NBS on a cable resulted in different measured attenuations mainly because of differences in the angle at which the light was launched. A second round of tests is now being conducted in which launch conditions are specified in accordance with proposed EIA test procedures.

"That's all that's really at issue now," says Love, "and anyone who is knowledgeable can see where that's going"—toward a specification of launch conditions that produce the most accurate concatenation predictions. He believes that it is the small size of the market that is holding back large instrument makers, and

## Some standards already in place

The measurement standards generated by the Electronic Industries Association are included in RS-455, Standard Test Procedures for Fiber Optic Fibers, Cables, Transducers, Connecting and Terminating Devices and in addenda to it. The basic document contains three test procedures dealing with physical properties such as cable flexing, retention, and humidity effects on devices and one on insertion loss for fiber-optic bundles. Addendum 2 also deals with physical properties such as air leakage and crush resistance. Addendum 1 is still undergoing approval and addresses testing for impact, acceleration, and temperature cycling (thermal shock).

Joseph Neigh, EIA coordinator for the P6 standards group, says RS-455 "is a living document; it will change and grow as long as we have fiber optics." Therefore, rather than hold up test procedures until they can all be published, "which might be a couple of years," the members of P6 elected to use the addenda method.

Roy Love, chairman of the P6.6 subgroup, says that his unit will have a proposed test procedure dealing with attenuation measurement in single-mode fibers ready by January. This procedure will have to be approved by the entire P6 group, a procedure that can take as long as two years. But, he says, "there aren't going to be too many changes in the end from the general consensus of opinion that's emerging now."

that for field instruments—optical time-domain reflectometers that can find line breaks—the launch angle need only be adjusted.

Along with measurement practice, some basic fiber dimensions seem to be approaching standardization. A standard long-distance telecommunications fiber, one with a 125-micrometer outer diameter and a 50-μm-diameter core, is currently in the approval cycle of the EIA fiber-optics group. Love's opinion is that, given the relatively large demand in telecommunications for this fiber and related long-wavelength detectors and light-emitting-diode transmitters, many will find ways to use them in applications like process control and computer links, where noise immunity and data integrity will make them attractive.

Steve Storozum, senior engineer at McDonnell Aircraft Co., St. Louis, Mo., also sees things beginning to move. "It's starting to break out of the chicken-or-egg syndrome," he says, referring to a lack of applications due to a lack of standards and an absence of standard instrumentation due to an absence of applications. Not only is the 125/50 fiber becoming a long-distance standard, he says, but also the 140/100 fiber seems to be gaining acceptance for short distances.

However, instrument makers may not have to wait for the market to develop, according to Storozum. "I believe the fiber-optic measurement industry is ripe for *de facto* standardization," he says. If an instrument maker produces a versatile, low-priced optical time-domain reflectometer, users will start to write procedures around it, he feels.

With these properties percolating to standardization, the measurement tool market may approach critical mass in the not too distant future—as early as 1981, according to Love. The NBS's Franzen notes that already "a lot of big companies are putting a fairly large effort into it [development of fiber-optic instrumentation]—like Tektronix and Hewlett-Packard—but they are not saying anything about it publicly."

He feels that they are waiting until standards settle a bit, but more importantly, until they can accurately predict where the market is going. "The big companies are doing things, but they want to see more of what the market is, to be more certain of the success of their instruments," Franzen believes.

**Work at HP.** That a large effort is currently under way at Hewlett-Packard is a "fair statement," according to Michael Cunningham, marketing manager for a variety of microwave instruments at the firm's Stanford Park (Calif.) division. He thinks that "steps in the direction of standard fiber diameters and connectors would make the instrument maker's job as well as the systems people's jobs easier," but "test procedures will have to become more cookbooklike." In fact, he thinks that instrumentation may have to be specified, as well. As to where the market may be in the next year or so, he comments, "We've done blue-sky projections based on some ratios that traditionally apply between end system expenditures and test equipment, but it remains to be seen whether that ratio will hold if fiber optics are as reliable as they promise to be."

Tektronix Inc., on the other hand, although following developments closely, says it is not involved in a major effort. Jean-Claude Balland, a marketing program manager for the Beaverton, Ore., firm, notes, however, that there is some promotion of existing general-purpose instruments for such applications.


**On the market.** Optical meter from Photodyne resembles 3½-digit hand-held multimeter, runs for 150 hours, costs under $600.

Balland sees the market shifting away from research and development as fiber optics go into manufacturing quantities. "The plan is now toward a more manufacturing-oriented [test] system. I don't think field service will begin to emerge for two or three years," he says. Right now, he believes, fiber-optics users are looking for such instruments only as samples. "Large companies are not coming in because the market isn't enough to justify designing an instrument."

Another company that has noted the shift into manufacturing production is EG&G Inc. Earlier this year, the company's Brookdale operation in Bracknell, Berks., England, introduced a microprocessor-based system for operation by unskilled personnel, able to measure attenuation in the 600-to-1,600-nanometer wavelength band [*Electronics*, March 13, p. 63]. The $16,000 instrument is IEEE-488-compatible and so can be part of an automated test system.

**Moving ahead.** As many large companies hold back, smaller ones in the U.S. and abroad, hoping to ride fiber optics to new fortunes, are taking the risk that measurement trends will firm up. According to Dennis Horwitz, vice president of Photodyne Inc. of Westlake Village, Calif., the company predicts $1 million sales for the current year with 30% to 50% growth in the next.

The only company selling optical instruments at this year's Wescon, two-year-old Photodyne introduced a new family of fiber-optic tools aimed at field service, the XE series. The series—two optical power meters and a fiber-optic power source—resembles 3½-digit hand-held multimeters. They can run for 150 hours, are autoranging, and display power in decibels relative to a milliwatt—a measurement that fits well with the current view of such measurement.

Among Japanese companies, Anritsu Electric Co.'s instruments are directly aimed at fiber-optic communications. The company has a fault locater that will likely go to market in another year or so. □

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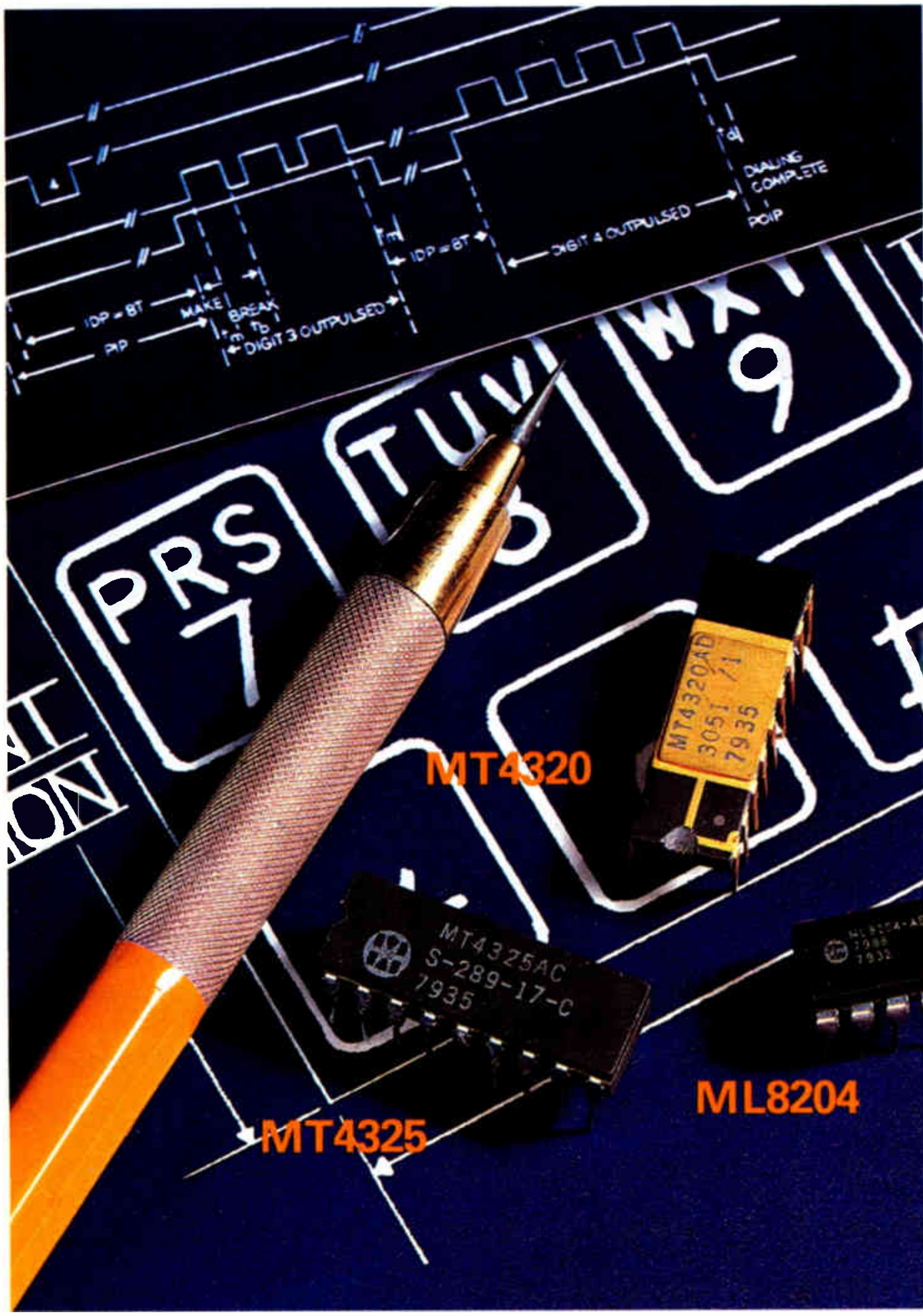


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Circle 94 on reader service card

Military electronics

# Military purchases to slow

## EIA study shows that system startups will be cut and inflation will outpace increases in R&D funding

*by Ray Connolly, Washington bureau manager*

**Regardless of who** occupies the White House next year, the military spending scenario is already set for the foreseeable future, and defense electronics contractors view it as one that limits the growth of their market to 2% per year after inflation.

The picture, says the Electronic Industries Association, is a grim one in which military leaders and Congress are pushing improvements in force readiness—including better training and salaries—at the expense of new weapons starts and an upsurge in strategic offensive systems at the expense of tactical requirements.

Military electronics research and development looms as the biggest loser over the next decade as budget increases are offset by an annual inflation rate ranging upward from 7%—perhaps as high as 10%—according to EIA's 10-year forecast of the military market (see table).

After interviews with 30 senior Pentagon and service officials, as well as with members of Congress and the Office of Management and Budget, the Washington, D. C.-based association's Government division presented its forecast during a Los Angeles symposium Oct. 7–9.

Nevertheless, the outlook is better for military electronics than for the defense industry overall. The reason: emphasis on readiness will call for product improvements of existing weapons platforms in lieu of multiple new starts—improvements with a high electronics content, according to EIA forecaster Jim Lee of Hughes Aircraft Co., Culver City, Calif.

Tactical aircraft upgrades are a prime example of where electronics firms will benefit, explains Lee, even though the aircraft industry itself will be "the most depressed area" because of the lack of new starts.

Using fiscal 1981 dollars, the EIA's figures indicate that the $25.4 billion available in the new fiscal year that began this month will be nearly 15% greater than the $22.1 billion for fiscal 1980's total for R&D, procurement, and operations and maintenance. But in fiscal 1982, the market will grow only 7% to $27.2 billion, slipping further the following year to 6.2%. Moreover, the largest slippage in percentage growth from prior years will come in monies for research, development, testing, and engineering rather than procurement.

The biggest single dollar share in the EIA's forecast goes for what the association calls E&C, for electronics and communications, which the analysts define as hardware "not dedicated to the support of one single weapons system or not classified elsewhere." For example, a system peculiar to a single type of weapon, like an aircraft or missile, is included

**U.S. DEFENSE ELECTRONICS: R&D AND PROCUREMENT**
(Total obligational authority in billions of dollars)

| Fiscal year | Aircraft | | Missiles | | Space | | Ships | | Ordnance | | Electronics and communications | | Other | | Operations and maintenance* | Overall total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | R&D | Proc | R&D | Proc | R&D | Proc | R&D | Proc | R&D | Proc | R&D | Proc | R&D | Proc | | |
| 1981 | 0.6 | 4.6 | 1.8 | 2.2 | 1.1 | 1.3 | 0.2 | 1.7 | 0.3 | 1.3 | 2.5 | 3.1 | 0.4 | 0.5 | 3.8 | 25.4 |
| 1982 | 0.5 | 4.8 | 1.9 | 2.7 | 1.2 | 1.4 | 0.3 | 1.8 | 0.3 | 1.5 | 2.6 | 3.3 | 0.4 | 0.5 | 4.0 | 27.2 |
| 1983 | 0.5 | 4.9 | 2.0 | 3.2 | 1.3 | 1.6 | 0.3 | 1.9 | 0.3 | 1.6 | 2.8 | 3.4 | 0.4 | 0.5 | 4.2 | 28.9 |
| 1984 | 0.5 | 5.0 | 2.1 | 3.4 | 1.3 | 1.8 | 0.3 | 2.1 | 0.3 | 1.9 | 2.9 | 3.5 | 0.4 | 0.5 | 4.4 | 31.4 |
| 1985 | 0.5 | 5.1 | 2.0 | 3.7 | 1.4 | 1.9 | 0.3 | 2.2 | 0.3 | 2.1 | 3.0 | 3.7 | 0.4 | 0.5 | 4.5 | 31.6 |
| 1986 | 0.5 | 5.2 | 2.0 | 3.9 | 1.4 | 2.1 | 0.3 | 2.4 | 0.3 | 2.3 | 3.1 | 3.9 | 0.4 | 0.6 | 4.6 | 33.0 |
| 1987 | 0.6 | 5.3 | 2.0 | 4.2 | 1.6 | 2.2 | 0.3 | 2.6 | 0.4 | 2.5 | 3.2 | 4.1 | 0.4 | 0.6 | 4.7 | 34.7 |
| 1988 | 0.6 | 5.4 | 1.9 | 4.4 | 1.7 | 2.5 | 0.3 | 2.7 | 0.4 | 2.7 | 3.3 | 4.4 | 0.4 | 0.6 | 4.8 | 36.1 |
| 1989 | 0.7 | 5.6 | 1.9 | 4.5 | 1.9 | 2.7 | 0.3 | 2.8 | 0.4 | 3.0 | 3.4 | 4.7 | 0.5 | 0.7 | 4.9 | 38.0 |
| 1990 | 0.7 | 6.0 | 2.0 | 4.7 | 2.1 | 3.0 | 0.3 | 2.8 | 0.5 | 3.2 | 3.5 | 4.8 | 0.5 | 0.7 | 5.0 | 39.8 |

*No R&D funds

SOURCE: ELECTRONIC INDUSTRIES ASSOCIATION under that weapon's category. On the other hand, the EIA explains, items that are "unique or used as a building block for several systems"—say, a command center, navigation and guidance, or electronic warfare—fall into the E&C category. Funds for E&C are forecast to grow by only 5% in fiscal 1982 from the current year, which reflects a 12% growth from just ended fiscal 1980. And that percentage growth rate in the decade's later years will slip even more, according to the forecast.

**Missile drain.** Modernization of strategic missiles is seen as constraining spending for tactical forces despite the political controversy and uncertainty still surrounding the Air Force's costly MX intercontinental ballistic missile and replacement of the old, liquid-fueled Titan ICBM force with solid-fueled D-5 versions. To the EIA analysts, the tradeoff between strategic and tactical priorities raises questions about the Pentagon's widely advertised Rapid Deployment Force. They question whether the RDF effort to move a tactical force into small conflicts quickly is not largely a "cosmetic" effort. In any case, the RDF is seen as offering few electronics opportunities compared with the program's need for new large cargo aircraft and ocean transports.

In the tactical ground forces area, the EIA's analysts see continuing heavy investment in antitank systems—with good potential for IMAAWS, the Infantry Man-portable Anti-Armor Weapons System, now initially contracted to Honeywell Inc.—and the possibility of development of a lightweight tank for large-scale production at relatively low cost. The army sees such a tank, as well as a "high-mobility multiple-use vehicle" as candidates for airlifting.

**Copter felled.** For tactical air systems, however, the forecast describes as "dead" the prospect for an advanced Aerial Scout Helicopter (ASH), long pushed by Hughes Aircraft, to extend the reconnaissance range. Similarly, the Air Force is showing little interest in a two-seat version of the A-10 ground attack aircraft. However, the analysis also shows that the F-15 fighter may resurrect the need for a new electronics warfare tactical system using that airframe. Another tactical air loss for U. S. producers will the Asraam—Advanced Short Range Air-to-Air Missile—which is to be produced by North Atlantic Treaty Organization partners in Europe, although the medium-range version, Amraam, will stay in the U. S. (For an examination of NATO program opportunities, see p. 104.)

Avionics makers will face a big Air Force push for integration and standards development in the coming decade, the EIA says. It is an issue that some producers say they have mixed feelings about, with one company's Washington representative noting that "it is an old story, of course. Everyone wants standards provided that those adopted are his."

Tactical naval forces still face a "numbers problem"—not enough ships—says the EIA. It notes that the lead entry is the DDGX/Aegis class, a ship smaller than the existing DDG-993 destroyer but equipped with the Aegis air-defense system. This employs phased-array radar and automated fire-control systems using an upgraded Standard Missile, the SM-2, that has a longer interception range and is more lethal than its predecessors.

**Gold watch.** In the area of $C^3I$—command, control, communications, intelligence—the EIA sees the Air Force still pushing hard for approval of JTIDS, the Joint Tactical Information Distribution System for triservice combat use by air, ground, and naval forces, even though Congress cut funds for the program in the fiscal 1980 appropriations. After several years in R&D, the spread-spectrum JTIDS uses frequency hopping in the 960-to-1,125-megahertz band to prevent jamming. The EIA calls it an Air Force "gold watch"—a needed and wanted program to which the service regularly attempts to overcome congressional objections by annually resubmitting it for funding. The EIA's forecast sees "lots of gold watches this year," noting that the Patriot and Stinger tactical air defense missiles were the only gold-watch survivors of the fiscal 1980 budget process. □

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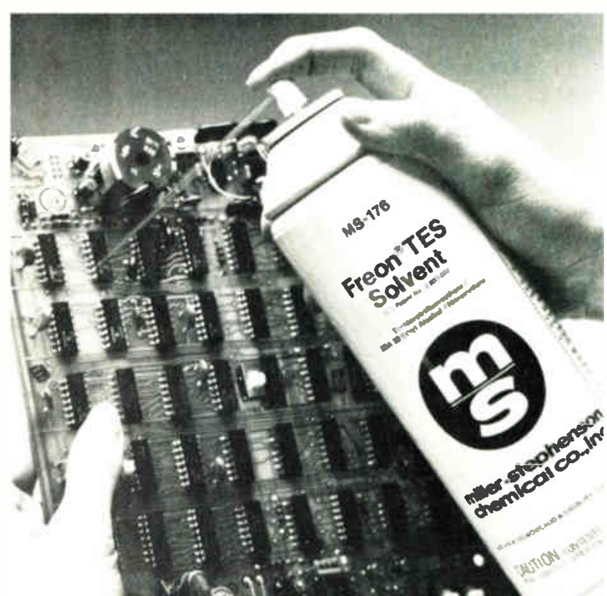


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Components

# European components outlook is dim

Inflation, energy, unemployment woes dampen market growth as manufacturers prepare for next month's Electronica

*by John Gosch, Frankfurt bureau manager*

**"It's going to** be a very tough year." That prediction, from Gernot Oswald, sales and marketing manager for integrated circuits and head of microcomputer activities at West Germany's Siemens AG in Munich, pretty much sums up how Europeans feel about the components business in 1981.

Thus, despite all the fanfare over new product introductions at the Nov. 6–12 Electronica components exhibition in Munich, apprehension will be the prevailing mood among the nearly 1,700 companies preparing to display their wares.

The causes for their concern are numerous. The continuing high rate of inflation, the nagging unemployment problem, and the climbing fuel prices in Europe's major economies are all directly or indirectly affecting Western Europe's $10 billion–plus components markets. Compounding the problems are the uneasiness over current world affairs and the protectionist tendencies in some countries, which could stifle free trade, and the uncertainty about whether the U. S. economic rebound is a real upswing. Taking the outlook for components, particularly semiconductor markets, on a country-by-country basis, the pervasiveness of concern is apparent.

Among the West German marketing people for example, there will be no arguing at Electronica over where one major problem for components producers lies: stagnating sales of color TV sets, traditionally the biggest single outlet for everything from electromechanical devices to integrated circuits.

As a result, semiconductor sales to the entertainment sector will creep upward only 2% to 3% in 1981, predicts Hans de Haan, market research administration manager at Texas Instruments GmbH in Freising, West Germany. The moderate business with entertainment equipment makers will partly be compensated for by brisk semiconductor sales to original-equipment manufacturers—10% over this year's level, according to de Haan. Overall, he sees West Germany's 1981 semiconductor market going up 5% to 10%. Considered separately, ICs will do better, 12% to 15%, he says.

Rüdiger Karnatzki, marketing director for continental Europe at ITT Semiconductors Group in Freiburg, is a bit more sanguine about next year. Semiconductor sales should rise at least 15%, he says. Behind the growth will be the OEM sector, with telecommunications providing particularly strong impulses.

**French fog.** "Right now, business is very good in France," says Michel Brunet, research and development director at RTC–La Radiotechnique-Compélec, a components-making subsidiary of the Philips group. "But there is a fog hanging over the end of the year." As far as semiconductor devices are concerned, he sees the biggest question mark for standard ICs. "Everyone is wondering how consumers will act at Christmas time," he says.

Data processing, however, is one area where industry watchers expect continuing healthy growth. "Overall, the market is in good shape, largely because of the pressure for distributed data-processing equipment, especially minicomputers and terminals," explains André Rivière, deputy general manager for Paris-based CII-Honeywell Bull.

**British layoffs.** In the UK, the recession's effect on semiconductor


**Looking ahead.** With Electronica opening next month in Munich, European producers are wrestling with problems in their respective economies. The scene is from 1978's show.

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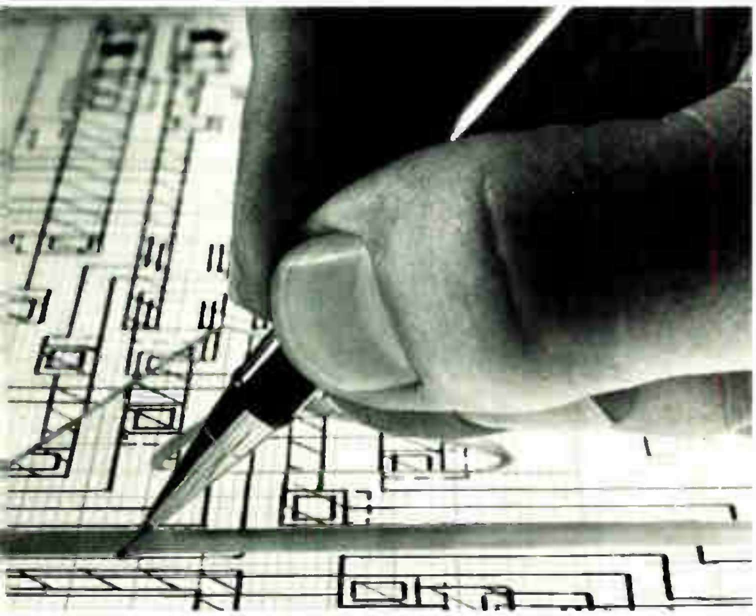

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sales has been patchy. Deliveries of color TV sets have stood up well in the first half of this year, while the total unit market for black and white receivers is the highest since 1972. But a truer picture may be coming from the audio sector. There, Philips, Grundig, and Rank all have announced layoffs or closures in the UK, and other companies have shown signs of distress.

Telecommunications, led by a modernization program undertaken by the British Post Office's British Telecom, is still a strong growth sector, but government borrowing limits may eventually affect this program and slow components purchases. The cash limits have also led to a damaging moratorium on military purchases and distress to Britain's instrument makers, according to Colin Gaskell, managing director of Marconi Instruments Ltd., St. Albans. The computer sector, normally a bright spot, is showing its first signs of trouble, though the full impact has not yet shown up in component deliveries.

**Italy is vague.** The immediate future for the Italian components market is difficult to pin down. Prospects for the next six to eight months depend on a number of imponderables, many of them outside the influence of producers. Angelo Teli, secretary of the National Electronics Industry Association in Milan, explains the Italian state telephone company's long-discussed plans for a $550 million investment program have finally been given the go-ahead on paper but that producers have yet to see the first order.

Teli adds that the video and audio sectors have been in a slump since April but, he says, producers are now hoping for a pre-Christmas lift. However, even if business picks up, sales during the final months of this year will only keep the components market stable, according to Enrico Villa, international sales and planning manager at SGS-ATES Elettronici SpA in Agrate, near Milan. The only really bright spot for Italian components makers, then, is the industrial sector. There, consumption is growing at 15% to 17%. □

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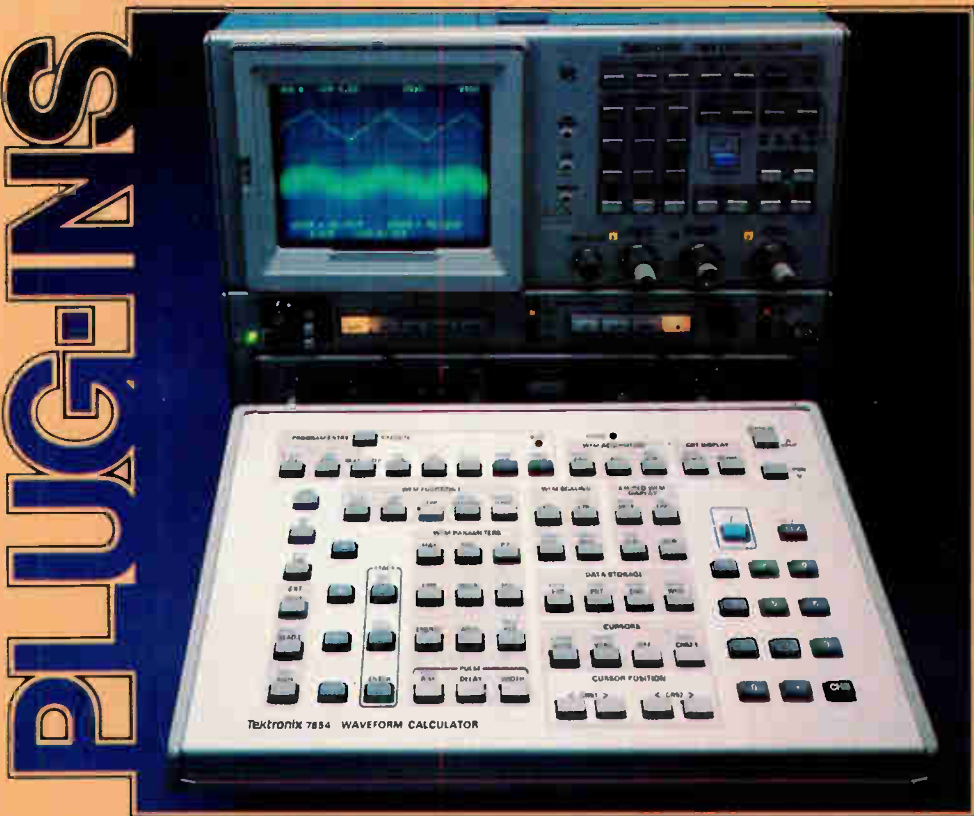


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Military electronics

# NATO dollars are flowing

American firms continue to pick off prime contracts despite the unhappiness of their European rivals

*by James Smith, McGraw-Hill World News*

**Despite European concerns** that U. S. firms are walking away with too many prime high-technology contracts, opportunities for electronics business with the North Atlantic Treaty Organization have never been better. If funding requests to be submitted to defense ministers next December are approved, NATO will probably lay out $1 billion over the next five years for fresh programs and updates of existing communications and military command and control systems. And spending will continue apace into the 1990s.

Among the projects:

- ACECCIS (Allied Command Europe Command and Control Information System), an update and partial automation of present manually operated information systems.
- Ongoing modernization of Nadge (NATO Air Defense Ground Environment) through replacement of radars, addition of computer capacity, and updating of control centers.
- ACCS (Air Command and Control System), a new system and part of NATO's long-term defense program. It can be considered a subsystem of ACECCIS, incorporating both Awacs (Airborne Warning and Control System) and the updated Nadge.
- A mammoth 15-year modernization of NICS (NATO Integrated Communications System), the basic communications network for the organization's civil and military authorities. It uses satellites, national telephone links, and NATO's own transmission facilities.

**Bundle for Britain.** Contracts for the programs are rolling in. Last month a consortium consisting of Hughes Aircraft Co., Plessey Co., and Marconi Radar won a $240 million contract to update Britain's air defense system. This award comes on top of a $150 million contract to modernize the West German air defense network awarded exclusively to Hughes last summer.

The U. S.'s General Electric Co. sold two radars worth $20 million to the UK last month, and Hughes, Plessey, and the French firm Thomson-CSF are competing for two others. Burroughs Corp., Computer Services Co., and Hughes are bidding on a $60 million command and control system (eventually part of ACECCIS) for NATO's northern region, Denmark and Norway. Also, last month the NATO infrastructure committee awarded Ford Aerospace Corp. a $90 million contract for a so-called Gap Filler communications satellite to bridge the time gap between the existing NATO Satcom 3 program and Satcom 4.

Some of the biggest programs will hit their stride after the 1980–85 funding period. Planning for the new ACCS system is only getting under way with establishment of a management agency. There is as yet no system architecture. But NATO military experts think procurement will start by 1985 and perhaps earlier.

**NICS dollars.** In addition, procurement for the 15-year phase 2 NICS modernization, the cost of which has now been increased from $1.5 billion to $2 billion, will start in earnest in 1985–86. If requests for an additional $3 billion in infrastructure funds are met by NATO ministers in December, the organization will probably spend about $500 million on NICS over the next four years. This sum will include some funds for additions to the first-phase program, which is now expected to cost nearly $1.1 billion and to be operational in

## Americans' success annoys NATO partners

European firms are unhappy about the growing dominance of U. S. electronics and aerospace firms successful in snatching choice North Atlantic Treaty Organization business. For example, practically all key prime contractors for NICS 1, the NATO Integrated Communications System, were Americans, exceptions being Siemens AG and AEG-Telefunken of West Germany. There has also been what some Europeans find a disturbing tendency for U. S. rivals to obtain repeat business.

One of these, Hughes Aircraft Co., which was system contractor for the Nadge (NATO Air Defense Ground Environment) consortium in the late 1960s, not only has piled up $230 million in British and West German Nadge updates this year, but has also won contracts for integration of Awacs (Airborne Warning and Control System) with Nadge ground stations—not part of the Nadge program but closely associated with it. Also, Ford's Aerospace Corp. Gap Filler award came on top of its Satcom 3 business.

Much of the U. S. firms' success, of course, comes from greater cost competitiveness, especially on systems being produced for the U. S. military. But another key reason appears to be their greater willingness, compared with Europeans, to meet NATO's often highly complicated specifications, even though it means increased development costs. -J. S.

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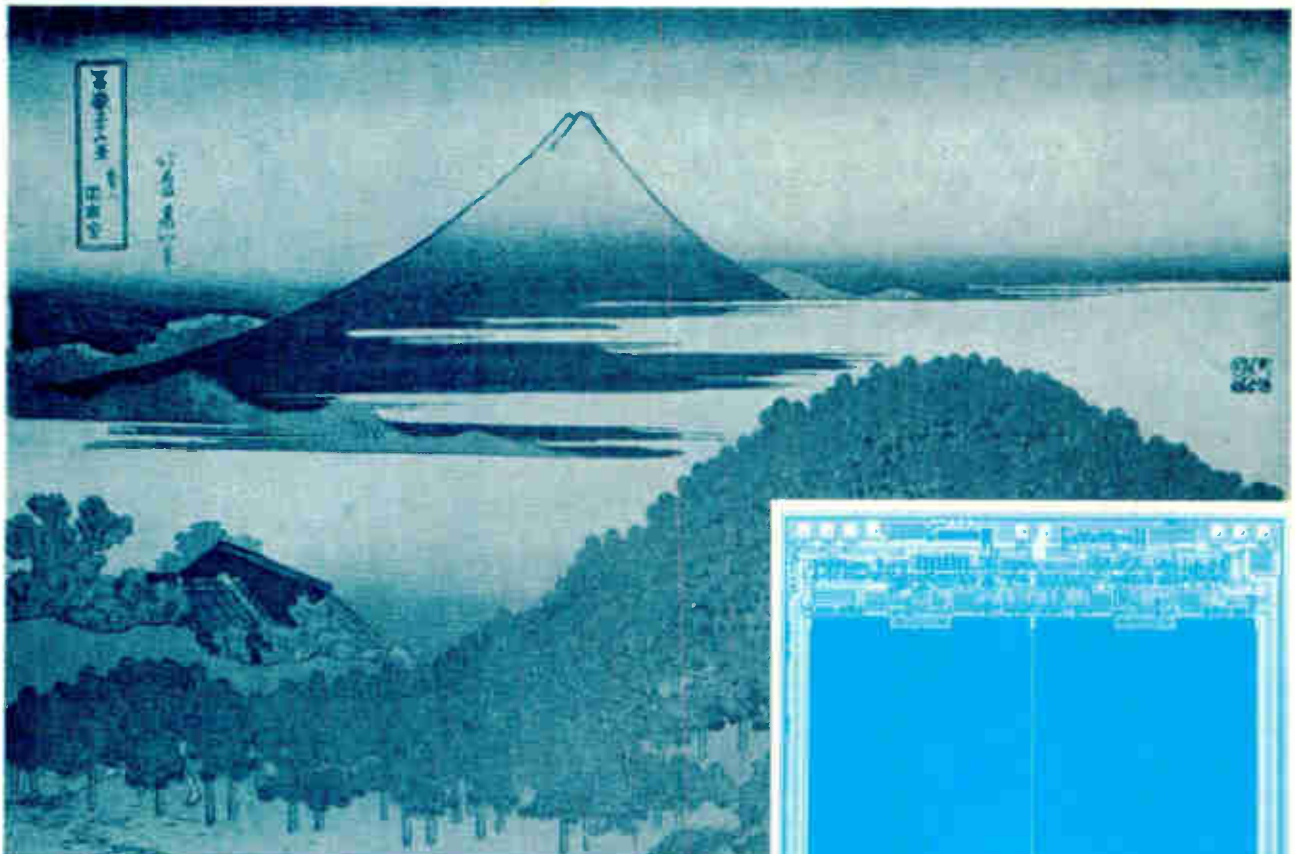
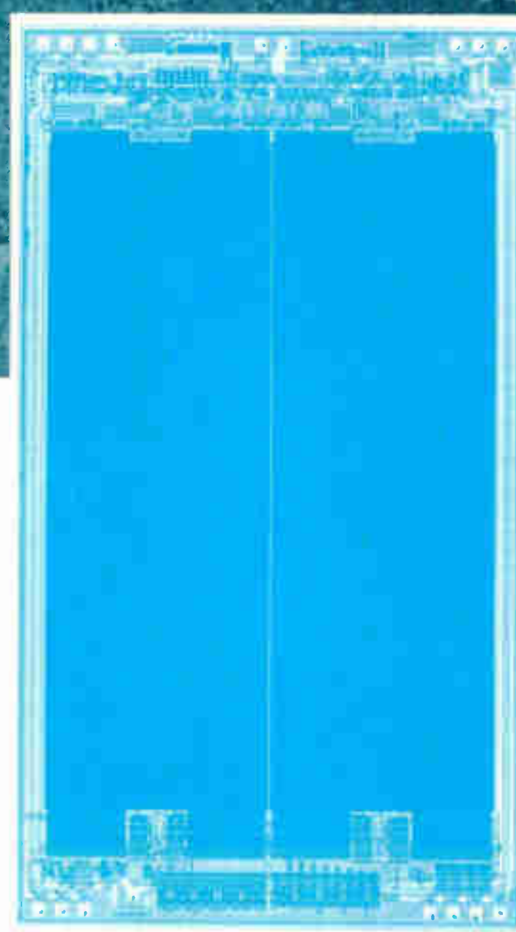
One of the problems spotted quickly in NICS planning—in the early 1970s—was the technical difficulty of obtaining nodal switches capable of accommodating the jumble of subsystem interfaces. These included analog, digital 64-kilobit/second pulse-code modulation, and digital 16-/32-kb/second delta modulation, as well as interfaces for narrowband speech-processing terminals and for emerging data services. It was decided to settle in stage one for separate voice and data systems—the IVSN (Initial Voiced Switched Network) being installed by ITT North Electric Co. and TARE (Telegraph Automatic Relay Equipment) by Litton Industries Inc. The third major subsystem, three Satcom 3 satellites, was launched by Ford Aerospace, which is installing 21 ground stations and modifying 12 others.

**Questions.** The upcoming debate over transition strategy will treat several critical questions, including how much of the NICS 2 system will eventually be scrapped and how much updated, and what technologies NICS should aim toward. NATO experts are divided between two switching technologies—16-/32-kb/second continuous-variable-slope delta (CVSD) modulation, the standard toward which NATO tactical military systems are moving, and 64-kb/second PCM, the direction of the European national telephone authorities. CVSD standards are already written into the NICS architecture and are also being defined for national tactical communication systems for the 1990s.

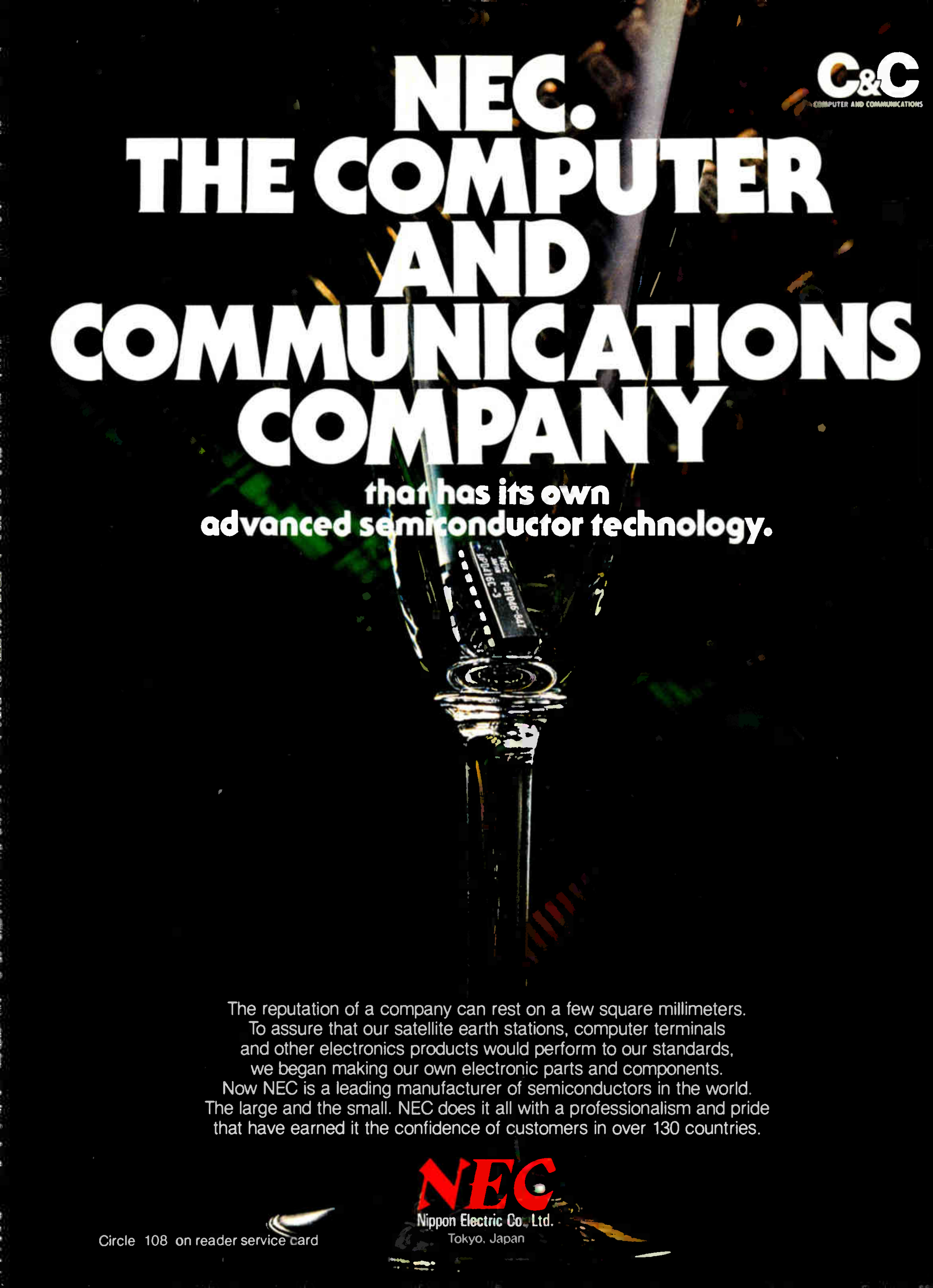
If NICS moves in this direction, some U. S. and British suppliers will probably be in a good position with CVSD hardware that will become available during the NICS 2 procurement period: the New U. S. unit-level switch TCC 42 and Britain's Ptarmigan tactical communications system. However, there are growing concerns that CVSD technology may be becoming dated and that NICS modernization could be more economically ensured by an evolutionary growth based on PCM. □

# HIGH-TECHNOLOGY ELECTRONICS IN JAPAN





## A LOOK AT ITS ORIGINS, ITS PRESENT STATE, ITS FUTURE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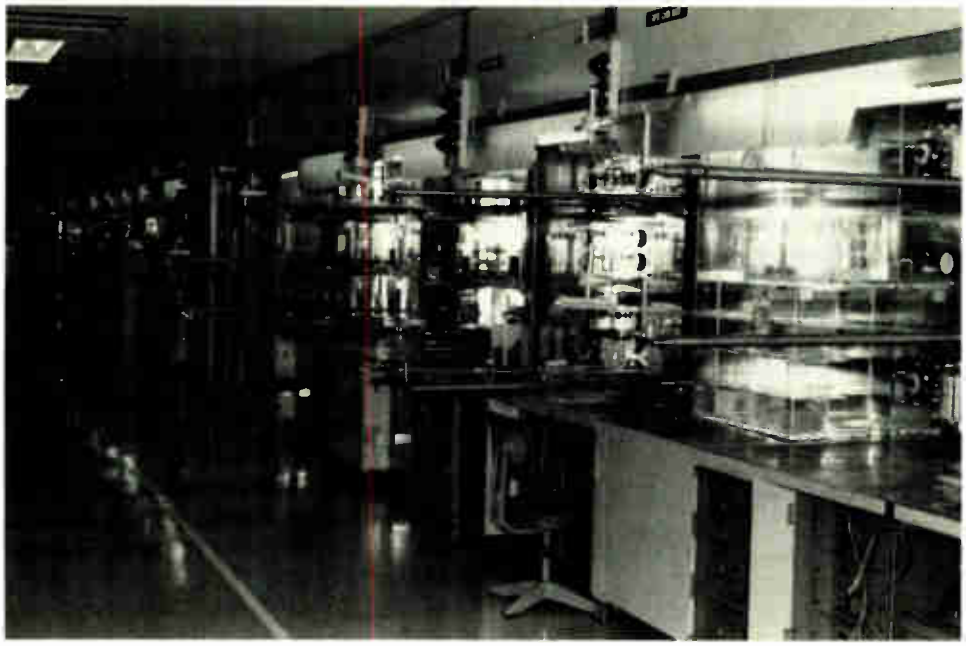


Kyushu Nippon Electric Co.

# GROWTH HAS ITS REASONS

*By Yumi Murakami*

*The dynamism and potential of the Japanese electronics industries is almost without parallel. Last year, these industries achieved a total production figure of $32.5 billion, which means they expanded 3.7 times during the past 10 years and registered an average growth rate of 12.6%. Japan's total economy grew at an unprecedentedly high rate during the 1970s, too, primarily because of its electronics industries, which profited by an upgrading of component quality, reliability, and production.*

*Unlike developments in other countries, the electronics industries' progress in Japan is attributable to specialization in consumer appliances. The introduction of merchandise like TV sets that appeals to the needs of consumer households worldwide and continuing innovative technology following the successful marketing of the transistor radio in the 1950s are factors in the growth.*

*Also, Japan's concentration on consumer electronics development, rather than on military reseach and development, is important. Whereas the industrial electronics industries in Europe and the U.S. developed with the support of large government projects, the Japanese electronics industries did not. For example, technological advancement by the American industrial electronics industry—including the development of integrated circuits—was largely supported by an enormous U.S. budget for R & D in such areas as national defense and space exploration. Until recently, development of industrial electronics technology, requiring huge advance investment for large projects, was not required in Japan.*

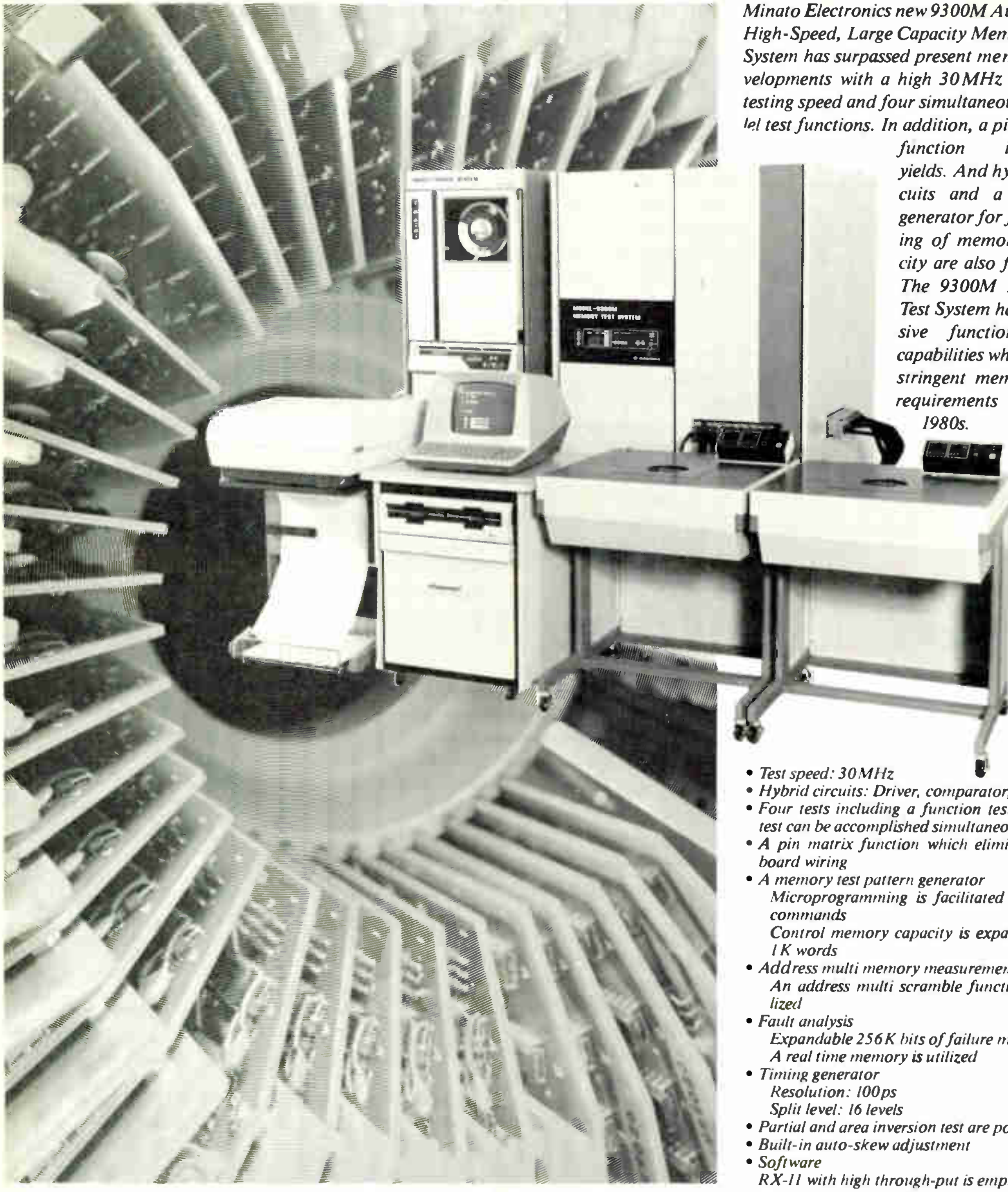
*Another contribution was Japan's high economic growth between 1960 and 1970, combining with the substantially increased income levels to create a demand for leisure goods. Unlike the trend in Europe and the U.S. toward widely varied leisure activities, Japanese households fixed on consumer electronics for leisure activities.*

*The growth of the Japanese electronics industry faced a turning point in the mid-1970s. Because of the saturated domestic market and import restrictions by developed countries, a high growth in production volume was not to be expected. Furthermore, the driving force of developing countries' industries was a potential threat to the competitive strength of Japan.*

*In response, Japanese industries introduced products with high value added. They achieved further growth, accompanied by an increase in nonprice-competitive strength, through the application of production and management techniques. In the future, the consumer electronics industry, which has reached substantial maturity, will probably not experience further rapid growth. High technology definitely will be the key to the expansion of electronics applications from consumer products to industry usage.*

*Certainly, integrated-circuit technology represents the leading edge of the development of the electronics industries in Japan, as in any industrially developed country. What follows is a look at the semiconductor industry in Japan, with particular attention to the industry's quest for mass-production volumes and high-quality products. Components are important too, and a discussion of a very important class—tubeless electronic displays—follows the section on the semiconductor industry.*

# An Advanced Memory Test System for the 1980s.



*Minato Electronics new 9300M Automatic High-Speed, Large Capacity Memory Test System has surpassed present memory developments with a high 30MHz memory testing speed and four simultaneous parallel test functions. In addition, a pin matrix function increases yields. And hybrid circuits and a pattern generator for free testing of memory capacity are also featured. The 9300M Memory Test System has extensive functions and capabilities which meet stringent memory test requirements of the 1980s.*

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- *Hybrid circuits: Driver, comparator, etc.*
- *Four tests including a function test and DC test can be accomplished simultaneously*
- *A pin matrix function which eliminates test board wiring*
- *A memory test pattern generator*
  *Microprogramming is facilitated with 700 commands*
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- *Address multi memory measurement*
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  *Expandable 256K bits of failure memory*
  *A real time memory is utilized*
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# SEMICONDUCTOR INDUSTRY MOVES BEYOND HIGH TECHNOLOGY

There are two major national semiconductor industries, but they are very different. It is not surprising that the *modus operandi* of the Japanese semiconductor industry should differ from that of the U.S. The development of any industry usually differs from country to country, due to differences in the availability of skilled labor, capital, and technology and, at other times, due to the competitive situation and economic environment of a given nation. In any case, it is not necessary for a country that learned the methodology of a new industry from another country to structure its own development process identically to that of the place of origin.

If we compare the structures of the American and Japanese semiconductor industries, we find some clear differences between "starter" and "follower." The semiconductor industry in the U.S. developed as a typical technology-intensive effort. The most important factor was technology to produce pure crystalline silicon and to design accurate and efficient circuits.

If a new U.S. company had the technology to develop a new product, it could sell the product at a price that not only absorbed the cost of production, but also created profits. This is one reason why many excellent technical experts could start business ventures. Furthermore, many investors were attracted to these businesses because of their high profitability and need for relatively small amounts of capital.

The Japanese, who have more recently entered the semiconductor market, must insure that the industry is more than simply a high-technology operation. The Japanese manufacturers of semiconductors, of necessity, must put great effort into lowering production costs and developing the highest-quality products, since they face stiff American price competition.

To compete in the world market, the Japanese had to build large facilities in order to receive increasing returns of scale. As is well known, the technological revolution in the semiconductor industry is moving at a very rapid pace, thereby causing technology, products, and facilities to become outdated quickly. In order to survive, then, it is necessary for semiconductor manufacturers to receive reasonable returns on their investments by selling products as quickly as possible and by reinvesting money in research and development and in new and updated production facilities.

This pace makes the business quite risky. In 1974, for example, the investment of Japanese manufacturers in R&D was approximately 22% of sales, and the investment in their facilities was approximately 21% of sales.

It is a special kind of Japanese company that enters the semiconductor business. It is not a venture company as in the U. S. The Japanese companies that entered the business are big corporations that have stable internal demands for integrated circuits and that also have other highly profitable divisions, namely, telecommunications, computers, and consumer electronics. They have survived their startup periods in the highly competitive semiconductor market by investing profits from their telephone, microwave, television, and other businesses, at the same time that they benefited from in-house demands for their new products. This distinctly different environment that surrounded Japanese semiconductor manufacturers at the beginning has influenced their competitive stance.

Controversy between the Japanese and American semiconductor industries started about 1977. The most extreme criticism against the Japanese IC companies was raised by semiconductor manufacturers in the areas around Boston and Santa Clara, Calif. Their criticism focused on the strategy the Japanese used in their R&D.

The arguments were that the Japanese manufacturers copied

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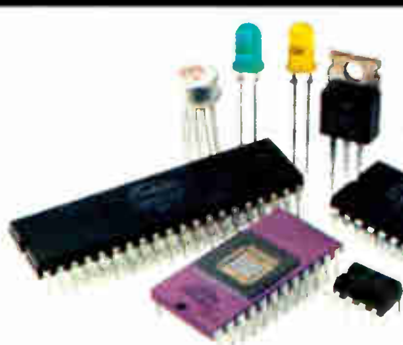
- steel & paper mill equip.
- air conditioners
- VTRs/TV cameras/ video tuners
- hi-fi components



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American technologies and received aid from the Japanese government in order to develop their own technology. Thus, the argument went, it is not fair for American corporations to try to compete with Japanese corporations in the same market. Therefore, U. S. semiconductor houses reasoned, that the Government has some obligation to assist the American companies so that they can compete with the "Japanese alliance of corporations and government."

It is well recognized by many people in the U. S. that the purposes of these arguments are not only to criticize the strategy of the Japanese corporations, but also to obtain some assistance from the American government. As a matter of fact, one of the main reasons why the position of a venture company has weakened in the U. S. market is that the semiconductor industry has developed into a capital-intensive industry that utilizes mass production. It is no longer at the stage of being a technology-intensive industry.

This is also apparent in Japan, where development of very large-scale integration is dominated by five big corporations; other smaller companies are concentrating on specialized IC products. Therefore, American semiconductor companies' positions in the U. S. market were weakened by the entry of corporations that have mass-production and mass-distribution systems; that the new entries are foreign companies is a secondary consideration.

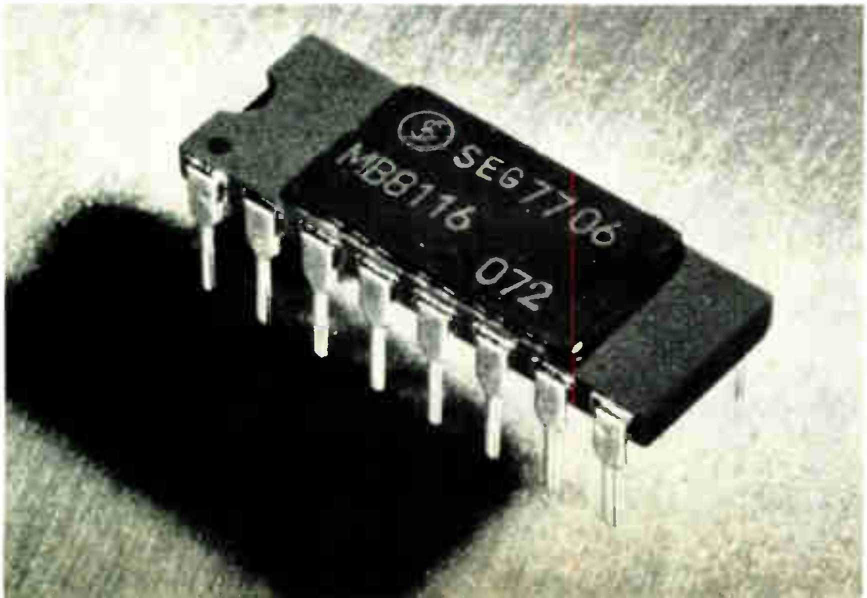
The competitive conditions in the semiconductor industry, which has become very highly developed, are quite similar to those in the consumer electronics industry. One of the important factors allowing a corporation to compete successfully in this market is its ability to offer a product of high quality at a low price. To satisfy these conditions, a company should have a mass-production technology that also can produce high-quality products. Moreover, it should have a strong mass-distribution system in order to market these products. It is equally important for a corporation to acquire technology that can develop semiconductor products, applied semiconductor products, or both for user needs. Thus a big company, which has integrated its production system from semiconductors to some finished goods based on ICs, will have a stronger competitive position in the marketplace.

As mentioned above, companies in Japan that satisfy these conditions are enjoying good positions in the market. It is not an overstatement to say that, along with the development of the industry, competitive conditions changed—and this change unexpectedly created greater demand for Japanese semiconductors. Also, needless to say, American corporations that satisfy these conditions are enjoying great success in the market, even as difficulties increase for the venture companies that achieved success with their technological excellence but with small amounts of capital.

The technological development of the semiconductor in Japan can be seen in such products as the one-chip microcomputer and the random-access memory. If a system of many ICs is replaced by a single-chip microcomputer, the resulting design would be smaller and sell at a lower price at the same time that some complicated functions could be added. When products are redesigned to exploit these functions, many kinds of mass-produced products such as consumer electronic equipment, office equipment, automobiles, etc., are able to sell more competitively. This is important for the Japanese makers of these products, and so the demand for microcomputers has a high growth potential, especially since mass production is the strongest point of Japanese technology.

Another market expected to grow rapidly is that for the RAM. Lowering the cost of information units by increasing memory density gives more options for a computer memory. For example, many systems can be organized so that parts of their memories can be used as a buffer—increasing necessary microcomputers, and, therefore, the number of multipurpose ICs. This is a strategy that lowers the cost of existing products, rather than developing ground-breaking new products. Of course, the added demand for the ICs increases production efficiency for their makers.

Looking over the revolution in random-access memories, we see the greatest demand in the RAM market is for the 16-K part, which is expected to reach its peak in popularity in 1980. Technologically, it is possible to begin the mass production of 64-K RAMs by then. However, the return on investment in 16-K products has not been sufficient, so their life cycle should be extended. Because of this, the production of 64-K chips is




**Since denser integration means more and more memory bits can be fitted into a RAM package, the popularity of these chips continues to grow.**

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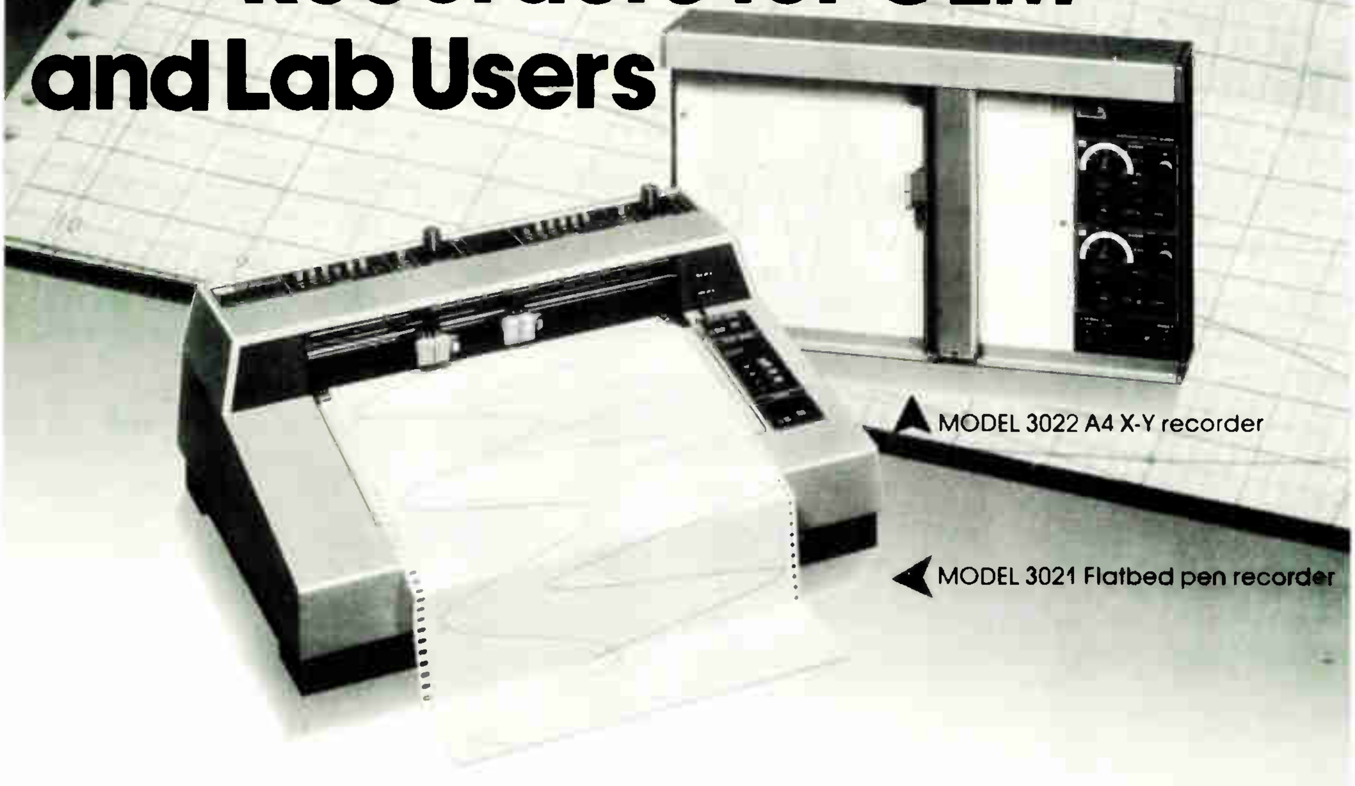


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limited to very special-purpose products, which makes the cost of these memories still higher.

However, the 64-K RAM is expected to begin replacing the 16-K part in 1981 and 1982 and to reach its peak in popularity in 1984. It is expected that the 128-K RAM will reach its peak in popularity by about 1988. Furthermore, a prototype of a 256-K memory has been presented, but it will take some time to develop it to the production stage.

Production technology has played an important role in increasing RAM densities. Ultraviolet light was utilized for photolithographic patterns in LSI memories; however, there is a limit of 1 micrometer for each pattern feature. It is necessary to use electron beams or X rays instead of UV rays in order to draw a pattern with less-than-1-$\mu$m features. For instance, the 256-K RAM developed by the Nippon Telegraph and Telephone Public Corp. utilizes electron beams.

What is more, a 1-megabit RAM cannot be produced by making a photolithographic mask and transcribing a circuit pattern on a silicon wafer by using beams. So it is necessary to develop a method for directly transcribing a pattern on a wafer with electron beams. This technological development has been pursued by a VLSI research group, the national project group that has contributed in finishing the fundamental research into this technology. Now each manufacturer is researching utilization of the technology.

As mentioned, the mass-production technology of semiconductors is the major strength of the Japanese semiconductor industry in this very competitive market. Of course, one of the most important impetuses for the development of mass-production technology is lowering the cost of the product.

One of the methods many American corporations used to lower cost was to move their assembly lines to Southeast Asian countries. In the case of Japanese manufacturers, however, this strategy was not taken. They tried, instead, to automate their assembly lines by improved mechanization.

For example, they have developed automatic machines for installation of chips and wire bonding in their assembly lines, and they utilize these newest machines in their factories in order to reduce labor requirements. This automation of the assembly line has contributed not only to improving productivity, but also to increasing the reliability of the products by minimizing human error.

There are generally two ways to increase the reliability of products. One is to eliminate inferior products by strict inspection and screening. Another is total quality control in order to prevent inferior products.

The first method makes the cost of products higher by adding the costs of the inspections, screening, and loss of rejected products. On the other hand, the latter method increases the yield of products and reduces the cost of inspections. Therefore, it produces more reliable products at lower costs and has been utilized by most of the Japanese manufacturers, including those in the semiconductor industry.

Thus reliable mass-production technology is supported by the automation of production and by high quality control, which is as important in design as in production. To begin with,

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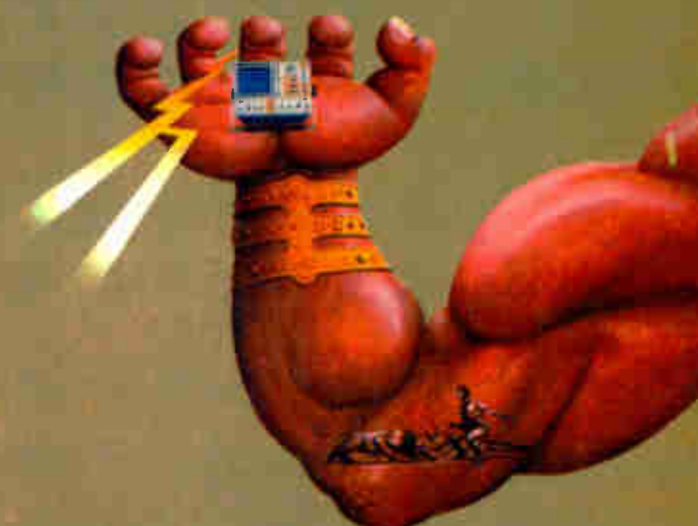

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designers are often encouraged to learn new ways of increasing the reliability of products. After the design has been finished, they meet with related departments like engineering and quality control. The engineers in charge of engineering and production try to prevent any trouble on the production lines and to increase production capability. The engineers in charge of design try to make designs that are well fitted to the production process.

The second step is trial production. Any abnormality is completely analyzed through statistical and physical methods. Products that could not reach the necessary level of quality are eliminated at this point.

The last step is mass production. Many kinds of faults found in this step, such as dirt on products, directly affect the yield rate and reliability of products. It is imperative that production processes give close attention to prevention of dirt contamination. Furthermore, data on the yield of products is periodically checked to improve the stability of the production process.

As part of this quality control, a very important factor is education for the workers. A wide variety of education is offered, ranging from specific production problems to the building up of morale. A QC circle, which is a small-group activity, is especially effective in strengthening morale.

For the realization of this highly reliable mass-production technique, the operations of the inspection system during the manufacturing process must be given close attention. The inspection of photomasks, for example, has been performed visually by microscope. This method, however, can hardly be applied to the current complicated mask patterns of a 2-to-3-$\mu$m minimum feature width.

Automatic inspection equipment has been developed and is being widely utilized in Japan and to some degree in the U. S. This equipment enables automatic inspection by the combined use of a TV camera, a processor, and display equipment. When a flaw is detected in a mask, automatic correction is carried out by a laser adjustment device which is directly connected to the equipment. Alternatively, flaw information is initially stored in the memory and later corrected by a separate adjustment device that has received input flaw data.

Today there are several detection methods that can screen a minimum flaw size of 1.5 to 0.75 $\mu$m at speeds between 15 and 60 seconds per square centimeter. This highly efficient automatic detection system plays a significant role in the achievement of a mass-production technique that continuously yields highly reliable products.

We have been discussing the present situation in the Japanese semiconductor industry. Now let us turn the discussion to its future, concentrating on new applications that represent increased use of ICs.

Needless to say, the major new application area is in computer products. One kind of computer development will be to shrink the computer while speeding up information processing at the same time that memory size is increased. As a result, the capability of computers will be enhanced.

Another development will be to make the computer simpler to use. For instance, it could be programmed in the spoken and

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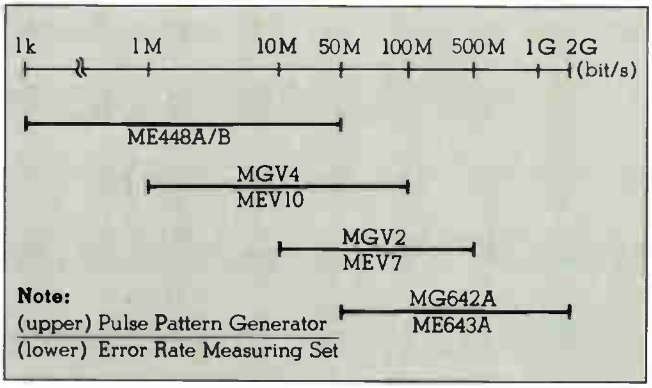


In addition, the models listed above are designed for testing PCM transmission systems.

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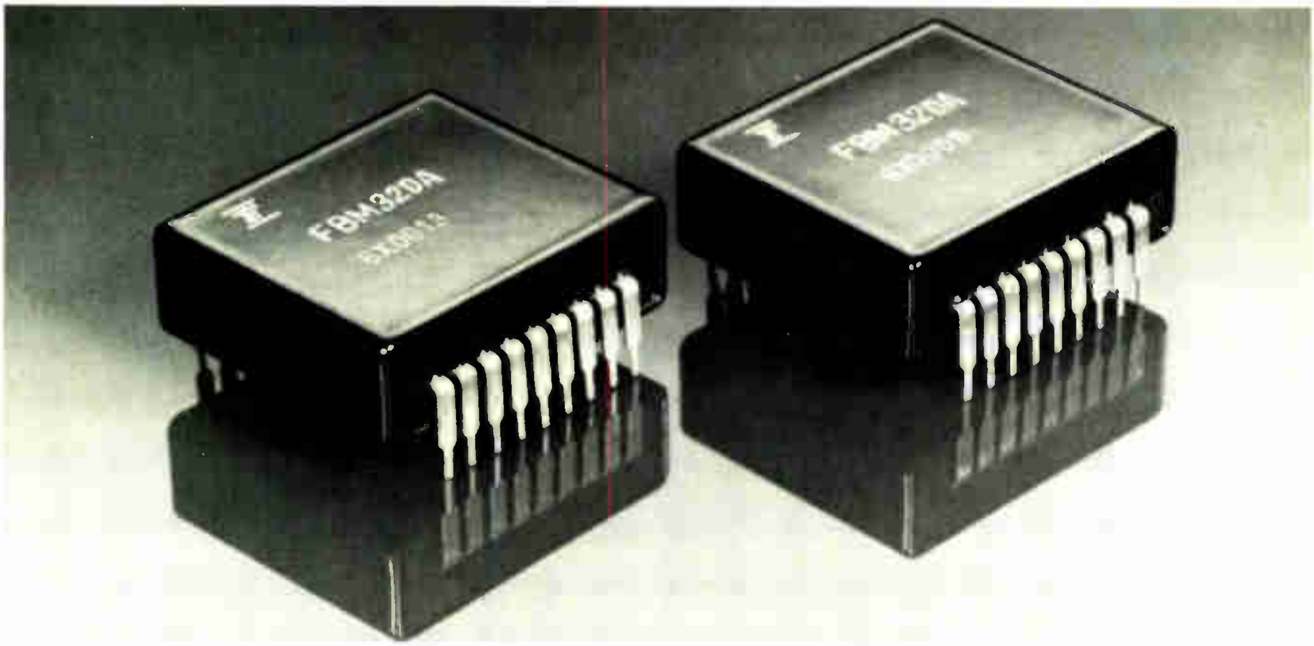
Circle 121 on reader service card




**Nonvolatile magnetic bubble memories are finding a slot between magnetic disk and core memories and the IC memory.**

written languages of people rather than programmed in computer languages and with keyboards. What's more, the computer output could be in natural voice, common alphanumeric characters, or both. The latter development, especially, could extend the usefulness of the computer to office and home users. This we consider to be very important.

In order to develop these new uses, we have to produce a computer that has such functions as running a very complicated program, recognizing patterns and voices, and synthesizing voice. It will be necessary to have high-density ICs, and this is the area on which VLSI designers should concentrate.

In software, we should develop systems that can recognize alphanumeric characters, understand the meaning of sentences, and fulfill the potential needs of users. The Japanese, who have such a complicated language, have a special interest in developing this kind of software. It also is the key for corporations seeking to win the Japanese market, which is potentially the second largest in the world.

For computer memories, the IC is related to the system's internal memory. In addition, the system has an external memory that files and stores input data in accordance with their usage. Relatively large and voluminous magnetic components like a hard disk, core system, floppy disk, or a cassette tape, have been commonly used for external memory. However, in anticipating the whole computer system reduced in size with a larger memory capacity for broader functions, it is inevitable that these external memories be minimized in size.

For this purpose, a promising medium is the magnetic bubble memory. Following its announcement by Bell Laboratories in 1967 in the U. S., research and development has been conducted in many countries to achieve higher integration and a larger memory capacity. The objective is to minimize the diameter of the magnetic bubble that controls the overall memory capacity.

In the past 10 years, the diameter of the magnetic bubble has been reduced from 50 to 100 $\mu$m to 2 to 3 $\mu$m. This reduction also led to a change in the memory structure from multi-chip to single-chip. The majority of magnetic-bubble memory systems presently manufactured around the world have a 64-K capacity. However, those with a 256-K capacity are also in the marketplace, and a few 1-megabit systems can be found.

The bubble memory is a highly integrated external system of compact size and broad capacity. It is a nonvolatile memory that permits easy replacement and alteration of data. Different from the conventional file memory, it is a complete solid-state system having no detachable sections, which means strong mechanical and environmental durability. Its compactness enables direct application to a printed-circuit board. Benefits of low electrical consumption also are a factor.

In a sense, this memory system is a medium-speed medium-capacity memory located between the conventional magnetic-disk or magnetic-core memory—those with large capacity but slow speed—and the IC memory—those with relatively small capacity but very high speed. It may be possible to boost capacity, and it is anticipated that demand by users of medium-speed systems will increase.

In light of the recent increases in demand for numerical control, computer terminals, minicomputers, and office computers utilizing cassettes and floppy disks, the production of bubble memory systems will increase. Furthermore, developments such as mass production, cost reduction, and higher integration are expected through future R & D. In two to three years, the 1-megabit chip will be a major product, while a 10-megabit chip will be achieved in the future.


Stand-Alone In-Circuit Emulation Probe?
IN-CIRCUIT DEBUGGER
ICD-178/Z80*
● debugs your objects by simply inserting its probe, instead of the microprocessor (Z80*) CPU chip.
● debugs, stand-alone, when combined with TTY, CRT or MC177 microcommunicator (another of our products)—big advantage in field maintenance and on production lines.
● may also be used as in-circuit emulation probe by combining it with a higher level machine, such as minicomputers or microcomputers.
Z80*
IN-CIRCUIT DEBUGGER 178
FEATURES
● Compact and light. ● 48K memory: mapping ICD and target at a 1K byte block. ● All 256 I/O ports can be used. Each serial port is equipped with 2 channels as standard (RS232C/Current Loop/TTL).
SPECIFICATIONS
● Dimensions, weight: 300(W) × 210(D) × 80(H)mm, 3.2kg ● Processor: Z80* (10kHz to 4MHz) ● System memory (for OS): 6K byte Debugger OS, 8K byte Option (self-assembler, etc.), 1K byte System RAM, 1K byte Memory Map, I/O ● User memories: 48K byte built-in (dynamic RAM), 1K byte block mapping possible (EXT for connection of static RAM) ● Communication ports: RC232C/20mA current loop/TTL × 2CH/110 to 9600BPS in 8 increments ● Break points: Hardware 2 points, Break modes: Instruction fetch/memory read-write/I-O read-write/external signals ● Trace: Real time/branch/1-step ● Memory mapping mode: 1) All memories of ICD 2) All memories of targets 3) 1K byte block mapping
* TM of Zilog, Inc.
APPLICATIONS:
● Microcomputer system development 1→3
● Microcomputer system maintenance 1→2
● Cross-debugging of high level machines 1→4→6, 7; 1→5→6, 7
RS232C
1) Model 178/Z80*
2) Microcommunicator Model 177II
3) TTY
4) FDOS system
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Circle 122 on reader service card

# TUBELESS DISPLAYS GROW

The story of tubeless electronic displays and their uses illustrates various trends in the highly technological electronics industries of present-day Japan. In fact, the display market has grown as the applications for advanced electronic components have grown.

In 1979, the market for tubeless displays experienced sudden and rapid expansion, and the demand for several types, including the light-emitting-diode, liquid-crystal, plasma, and fluorescent displays, increased by more than 50%. It is anticipated that the markets for the products utilizing these parts will exhibit substantial growth.

An important factor is that the technological development of these electronic displays was closely interrelated in the past with the development of integrated circuits. Until recently, production shortages of large-scale integrated circuitry created problems in expanding the electronic-display markets. However, it is expected that these problems will be alleviated.

Let us review 1979. The primary items on the market quickly shifted from electronic calculators in the first half to watches at the midyear and to diversified products at year-end. Such rapid shifts in demand and the diversification of display types for various purposes have created good results for manufacturers. These developments formed sound bases for further diversification in the 1980s. A glance at products like calculators and watches supports this conclusion.

To take electronic calculators as an example, the type of the display has varied from the gas-discharge tube to fluorescent and liquid-crystal displays (LED displays are common). Watches employ LED and liquid-crystal displays, and electrochromeric displays have been introduced quite recently to the market.

Technological developments in the use of large-scale integrated circuits and electronic displays in watches and calculators are at present expanding the scope of these components. Moreover, since the microcomputer first made its appearance, the display market has been growing at a rate of 30% to 50% annually, a rate similar to that of the microcomputer market (including other LSI chips).

Conventionally, the cathode-ray tube is employed as the display for computers. For the new small applications of computing power like point-of-sale terminals and personal computers, however, use of the LED, liquid-crystal, and fluorescent displays is relatively widespread. The




Circle 123 on reader service card

power consumption, the size, and the high-voltage requirement of the CRT militate against its use, especially when displaying large amounts of information is unnecessary. Yet, the tubeless displays are technologically inferior to the CRT as large-capacity information displays, although they function adequately when applied to microcomputers.

To develop effective demands for various tubeless displays, segmenting the market is effective to a certain degree. For example, the U.S. automobile industry is expected to become a major market for fluorescent displays since they are considered most appropriate for the electronic and digital car clocks and dashboard panels. Liquid-crystal manufacturers, at the same time, are strengthening their sales activities in order to find new applications that can ignore the material's limited temperature range, which hinders their use in such areas as automobiles. Manufacturers of LEDs are maintaining a relative calm even though there is need for several LED technological improvements, such as brightness.

Requirements in future displays include a wider range of colors and multicolored panels. Developments here have been advanced by individual manufacturers, and some have introduced products. However, the realization of full-scale practical applications is expected in the latter half of the decade.

In regard to multicolored designs, it is expected that the problems still remaining, such as quality of displays, brightness of the light-emitting type, and prices of elements, will be solved in the near future. It is certain that multicolored units will play a significant role in the development of display markets.

Japan produced 866,788,000 LEDs in 1979—an increase of 75% over the previous year. In monetary terms, a value of $85 million was recorded—a rise of 64% from the previous year. An analysis of this substantial growth was carried out by major manufacturers, and some of their conclusions follow.

The rapid increase in applied products is regarded as having contributed to the growth. Improvement and sophistication in certain products are considered to have increased demand for LEDs. Appli-

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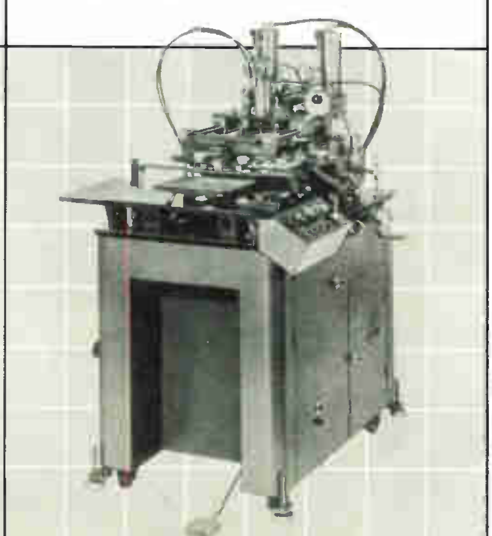
- Squeegee speed: 0 ~ 4 in. sec. (0 ~ 100 mm sec.)



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Circle 125 on reader service card

cations in home appliances, sound equipment, and industrial products will become major markets. The resulting growth rate is expected to exceed that of last year.

It is rather difficult to forecast the next major market from the above. However, it is most likely that the automobile industry will develop into a significant market. At the same time, display manufacturers will increase their efforts to promote the application of light-emitting diodes. That market, on the whole, is expected to grow at a higher rate than those of other tubeless displays.

In regard to the problem of brightness, some improvements were made by the manufacturers, who have announced that LEDs are able to compete with other light-emitting displays. Aided by improvements in the output power of LSI chips, light-emitting diodes have found their way into automobile clocks and digital displays of car radios. The expansion of applicable fields, attributable to the improvements in brightness, permits custom production according to user specifications, although it indicated unfavorable trends in standardization.

Liquid-crystal displays are most frequently seen in calculators and watches. Major advantages of LCDs are low power consumption and relatively low operating voltage. Moreover, their nonemissive characteristics avoid problems resulting from lack of contrast under sunlight, due to insufficient brightness. In fact, the brighter the ambient light becomes, the more readily a high contrast is obtained.

The demand for LCDs has increased substantially in recent years because of growth in calculators and watches and remarkable increases in their application of liquid-crystal displays. Although the LCD industry had at one time encountered some problems due to shortages of ICs, the demand for liquid-crystal panels has been stable.

Many LCD manufacturers are confident that calculators and watches will continue to use many liquid-crystal displays. However, the majority of these manufacturers have reached the conclusion that the makers of both products already have established their LCD sources. Therefore, new fields of application will be sought.

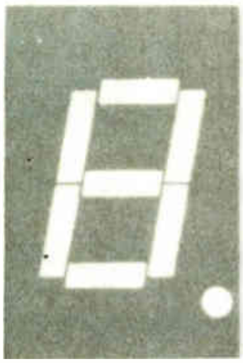
One application is in portable electronic games, which have a high degree of variation in display patterns. These LCD panels are rather larger than conventional panels and are capable of providing the most appropriate display patterns to meet the respective game requirements. It is predicted that LCD panels made for this purpose will undergo an increase in growth rates over the next few years.

Dot-matrix panels were developed for wider applications, including cash terminals at banks, ticket reservation terminals, and electronic translators. Most of these applications used CRT displays in the past. However, it is expected that LCD panels will rapidly replace CRT displays, since they are better suited to deal with restricted power and physical space. Additionally, extensive use of color will be rapidly demonstrated in the future.

In June and July of this year, the Eighth International Liquid Crystal Conference and the Liquid Crystal Exhibition were held at the Kyoto International Conference Hall. Eighteen Japanese and European companies that have establishments in Japan participated. Their exhibits included dot-matrix LCDs with three or four rows of 20 to 40 characters, game panels, and many experimental automobile dashboard panels with multicolored displays.

In a separate conference sponsored by the Society of Automotive Engineers, practical automobile dashboard panels with LCDs were viewed as a likely trend. This indicated the appropriateness of applying liquid crystals to automobile displays. Not emitting light, they do require alternative lighting sources at night. LCDs are brighter than light-emitting displays in the daylight.

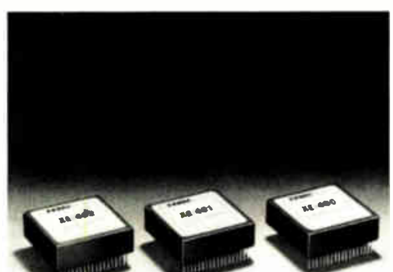
The application of liquid-crystal displays to portable TV displays has been tried by sandwiching liquid crystal between glass plates and a silicon substrate with transistors manufactured by IC technology as a switching component. Certainly, LCDs have gained a firm position through use in watches and calculators. Further developments are expected to multiply their fields of application.



*Stanley Electric Co.* uses temperature-difference liquid-phase epitaxial growth to produce its Superbright light-emitting diodes for seven-segment numeric displays. With character heights of 10, 15, and 25 mm, the displays come with red, green, yellow, or amber LEDs. They feature low current drive with extremely high light-emitting efficiency, and they are excellent for dynamic driving applications because of the nearly linear characteristics of the GaAlAs red diode in the current vs. brightness tradeoff. (501)

*Jepico Corp.* offers the UT series of miniature switches, which can be mounted on printed-circuit boards. Developed for dry-circuit applications, the switches have contacts and terminals that are 1.3-$\mu$m gold or silver plate over 3 $\mu$m of nickel. Case material is Valox/94V-O U/L. (505)

*Minato Electronics Inc.'s* Z-80-equipped model 1860 programmer for programmable read-only memories can be used with single MOS and bipolar PROMs. Personality modules adapt it to different memories, and the microprocessor gives a wide range of functions. (502)

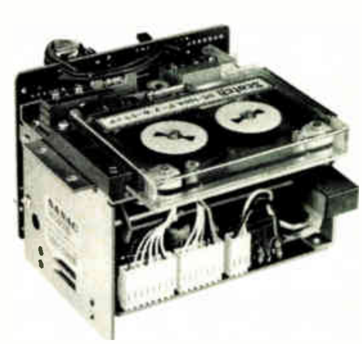


*Xebec Co.* converts linear signals into nonlinear and vice versa using a piece-wise linear-approximation method in the XE-400 series function converter modules. Ease of use comes from the simple, independent adjustment of the various settings, such as overall span. (504)

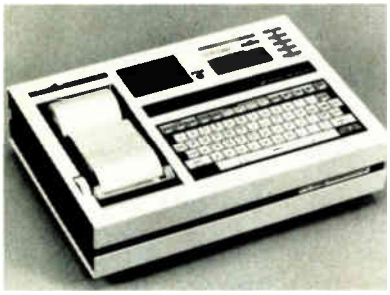

*Toyo Corp.* employs ball bearings in its ac and dc miniature fans, giving an operating life of at least 15,000 hours. Intended for office equipment, computer peripherals, medical equipment, and the like, the fans come with a variety of performance specifications. (506)

The 1961 PROM programmer from *Minato Electronics Inc.* can gang-program as many as eight MOS memories. It has a 16-kilobyte memory capacity. Like the model 1960, it has parallel and serial interfaces and check functions, such as memory test and improper-circuit test. (503)

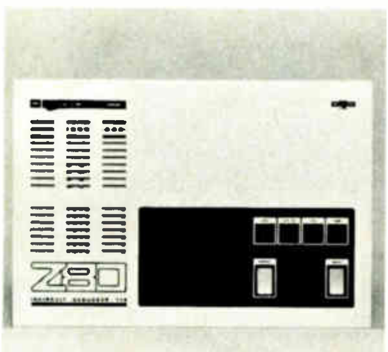
*Sankyo Seiki Manufacturing Co.* makes its double-sided flexible disk-head assembly to exceed required drive life expectancy. The assembly is designed to operate at zero penetration, and the gimbal upper fixture maintains head stability during load and unloading. (507)



The STC-8000-2A read-after-write cartridge drive from *Sankyo Seiki Manufacturing Co.* operates from a single supply, consuming less than 700 mA during normal running and less than 2 A during start/stop/reverse. It has an inter-record gap of less than 0.7 in. nominal. (508)



*Bell Corp.* offers a portable computer terminal, the Microcommunicator 177 Mark II, that is compatible with Teletype's ASR 33. With an ASCII full keyboard, a 32-digit printer, and a 16-digit display, the MC 177 II has built-in RS-232-C and current-loop interfaces. (511)


The ICD 178/Z80 in-circuit debugger offered by *Bell Corp.* is a portable in-circuit emulator that is essentially a low-cost, compact microprocessor development system for debugging, field service, etc. The Z80 ICD is available now; coming are models for the 8085 and 6809. (512)

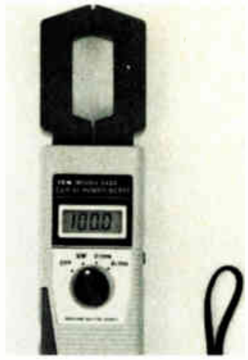
*Anritsu Electric Co.* combines optical power meters and sensors for the ML93A digital meter shown and the ML94A analog meter, both with wavelength ranges of 0.4 to 1 $\mu$m or 0.75 to 1.7 $\mu$m and with a variety of measuring ranges that go as low as $-90$ dBm up to $+10$ dBm. (513)

*Sharp Corp.* fits its ultra-compact liquid-crystal-display clock module into a 19.8-by-9.8-by-4.7-mm package. The LX-3101X micro-digital clock operates from a single 1.5-V power supply and incorporates a complementary-MOS large-scale integrated circuit on a thin-film-carrier substrate. It features simple time setting with two buttons and signals the passing seconds by flashing the colon between the hours and minute digits. It is intended for consumer applications, such as pendant clocks and ball-point pens. (509)

The ML442A selective-level meter from *Anritsu Electric Co.* covers a wide frequency range from 200 (20) Hz to 30 MHz with a $\pm 0.1$-dB level-measuring accuracy and a 70-dB intrinsic distortion. A microprocessor plays a role in level measurement, autoranging, etc. (514)

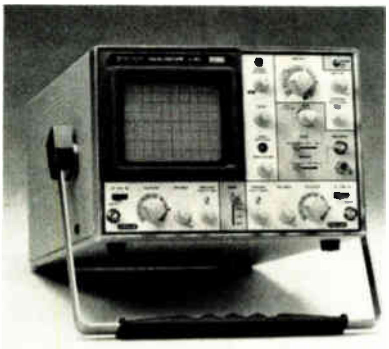
*Ando Electric Co.* has developed its AE-4100 series microprocessor system analyzers for use in development, product inspection, and maintenance of hardware and software of setups using the 8080A, 8085A, and Z80 processors and their equivalents. The AE-4100 performs tests directly on the processor, and, in addition to its monitor functions, it tests units while controlling them, permitting reading and writing to and from registers and memories. It is easy to operate, since all required functions may be performed with the 16-key function and numerical keyboards; also, it may be connected through its trigger output to an oscilloscope or logic analyzer for detailed analyses. Available options include an input/output interface card, a keyboard printer, and a user-mode random-access memory. Clock rate is 0 to 3 MHz. (510)

*Yokogawa Electric Works Ltd.* employs an interactive programming system with a built-in cathode-ray-tube display in the 3848 universal data logger. The result is simplified operation through menu programming. The 3848 also provides comprehensive computational ability. (515)



The 2433 ac power meter from *Yokogawa Electric Works Ltd.* measures true rms voltage, current, and power in single-phase or balanced three-phase circuits—without interrupting service. Voltage range is 20 to 600 V; power ranges are 2 to 200 kW and 0.2 to 20 kW. (516)


*Nippon Electric Co.* offers two read-only memory options in its µPD8048 family of single-chip 8-bit microcomputers. The µPD8048 has 1 K by 8 bits of maskable ROM, and the µPD8035L uses an external program memory. Both microcomputers are compatible with standard 8080A/8085A peripherals, which may be used, for example, for the µPD8035L's ROM. Their n-channel MOS technology requires only a single +5-V supply, and cycle time is 2.5 µs. Of the 96 instructions, 70% take 1 byte; the rest take 2. The two microcomputers each have a 64-by-8-bit random-access memory, an eight-level stack, 27 input/output lines, an interval time/event counter and an internal clock generator. They function efficiently in control, as well as arithmetic applications, and the flexibility of their instruction set allows direct set and reset of individual data bits within the accumulator and I/O port structure. Standard logic-function implementation is facilitated by the variety of branch and table look-up instructions. (517)



*Hitachi Denshi Ltd.'s* V-352 dual-trace portable oscilloscope has a vertical sensitivity of 1 mV/division and a frequency range of dc to 35 MHz. A companion V-202 scope has a dc-to-20-MHz range. They offer high-accuracy voltage and time axes set at ±3%. (518)

The KP-500 color video camera from *Hitachi Denshi Ltd.* uses solid-state MOS sensors, giving greater sensitivity than charge-coupled-device sensors, which drop in transfer efficiency in dim light. Also, each picture element is larger for a given image area, aiding sensitivity. (519)

Carrousel Type
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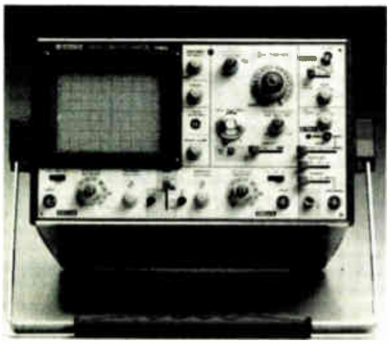
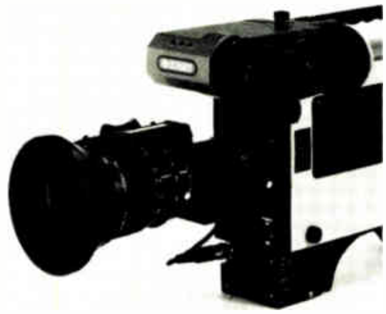
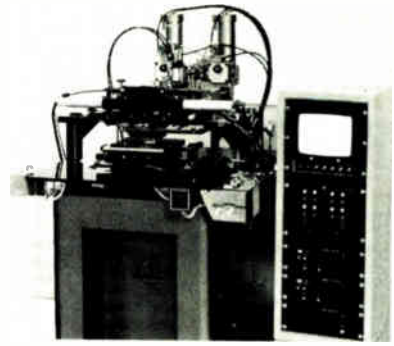


*Hitachi Denshi Ltd.* provides oscilloscope users with a delayed sweep, variable trigger hold-off, and automatic focus correction in its V-550B 50-MHz dual-trace scope. Other features include a single-sweep mechanism and third-channel display. Sensitivity is 1 mV/division. (520)



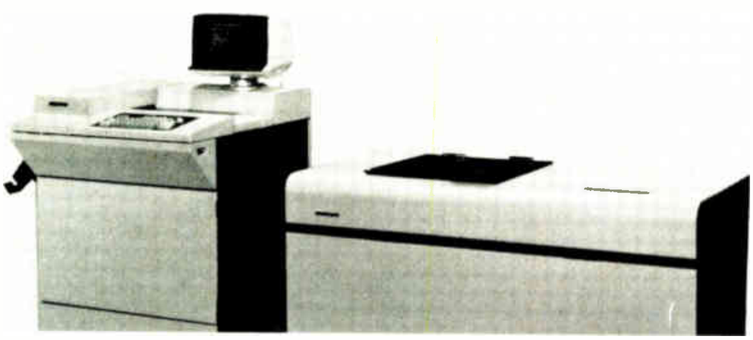
The SK-91 color video camera from *Hitachi Denshi Ltd.* weighs only 4.4 kg and runs for over two hours on a rechargeable battery belt. A new F1.4 prismatic beam splitter, together with low-noise preamplifiers, provides high sensitivity and an excellent signal-to-noise ratio. (521)



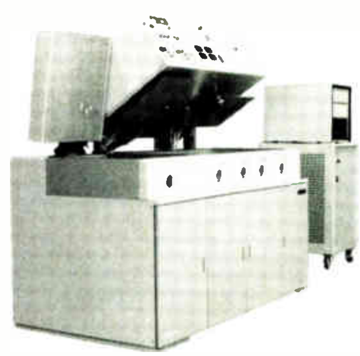
*Newlong Seimitsu Kogyo Co.* combines a TV monitor with its screen printer in order to let users check mask alignment and make the necessary adjustments. Since the monitor is then set to the right alignment, placing subsequent wafers in the right position is easy. (524)


*Hakuto Co.* exports the model 1861 gang programmer for programmable read-only memories. The unit can program the Intel 2716 and 2732 and Texas Instruments TMS 2532 PROMS and equivalents and has RS-232-C and 20-mA current-loop interfaces. Among its check functions is a system check that tries out the 1860 to see if it is working properly, as well as checking to see that the PROMS are programmable. Data inputs for the programming may come from a master device, a computer program, or a paper-tape reader. (522)

*Ulvac Corp.* designed its System 1200 vacuum deposition and evaporation unit to process, at one time, 78 3-in. or 51 4-in. wafers under fully automated control. A high-capacity electron gun and a planetary jig provide excellent step coverage and uniform film thickness. (525)



*Toshiba Corp.* incorporates laser-beam technology in its document filing system, which easily and speedily records and reproduces printed image information. There are four parts to the system: a laser scanner that converts input information into electric signals; an optical disk memory that permanently records the signals; a laser printer that reproduces the data on plain paper; and a microcomputer-controlled operation and control unit. Capacity is 10,000 pages per 30-cm optical disk; random-access time is 0.5 s; read and record time is 3.5 s; and reproduction and output time is 10 s. Resolution in reading and output is 8 lines/mm. (523)



The MLH-6000 high-rate sputtering system from *Ulvac Corp.* consists of a loading/unloading chamber and a sputtering chamber. As one tray of substrates is being sputtered, the previous one may be unloaded and the next one loaded, contributing to the high sputtering rate. (526)

# High Performance on Display
# From Hitachi, the Reliable Performer

## High-resolution Color Display Tube

**Features**
- High-resolution in-line electron gun
- Fine pitch dot type screen
- Self-convergence, preset deflection yoke

**Applications**
- Character and graphic display, picture monitor

**Main Specifications**

| Size (in.) | Type No. | Spot Dia. (mm) | Brightness (fL) | Anode Voltage (kV) | Beam Current (μA) | Dot Trio Quantity (K pair) | Character Numbers |
|---|---|---|---|---|---|---|---|
| 14 | 370JYB22 | 0.5 | 50 | 23 | 450 | 750 | 3000 |
| 14 | 370JSB22 | 0.8 | 70 | 23 | 700 | 380 | 2000 |
| 20 | 510XJB22 | 0.8 | 26 | 27.5 | 450 | 1,350 | 6000 |
| 20 | 510XTB22 | 1.2 | 55 | 27.5 | 1,000 | 600 | 4000 |

Note: Monochrome display tube is available.

## Liquid Crystal Dot Matrix Display Module


**Features**
- Alpha-numeric display module having 5 x 7 dots/characters with cursor
- Compact and slim design
- 1-chip control C-MOS LSI (HD43160A) which has 160 characters (ROM) and character memory (RAM) is available.
- Easy-to-use TTL or C-MOS level interface
- Suitable for battery drive and portable use

**Applications**
- Small-sized terminal displays, microcomputers, measuring instruments, POS terminals, telephone receivers, machine translators

**Main Specifications**

| Module | Number of Characters | Module Size (WxHxD),mm,max. | Power Supplies, V | Power Dissipation, mW | Weight, g |
|---|---|---|---|---|---|
| H2532A | 16x1 | 84x44x15 | +5, −5 | 2 (typical) | 40 |
| H2535 | 16x2 | 84x44x15 | +5, −5 | 2 (typical) | 40 |
| H2538A | 40x1 | 220x53x15 | +5, −5 | 2 (typical) | 100 |
| H2539 | 40x2 | 220x53x15 | +5, −5 | 2 (typical) | 100 |
| H2555 | 40x1 | 227x38.5x15 | +5, −5 | 2 (typical) | 90 |

Note: The Hitachi LC display module can be manufactured to meet special design specifications. Please contact Hitachi for special modules.

HITACHI

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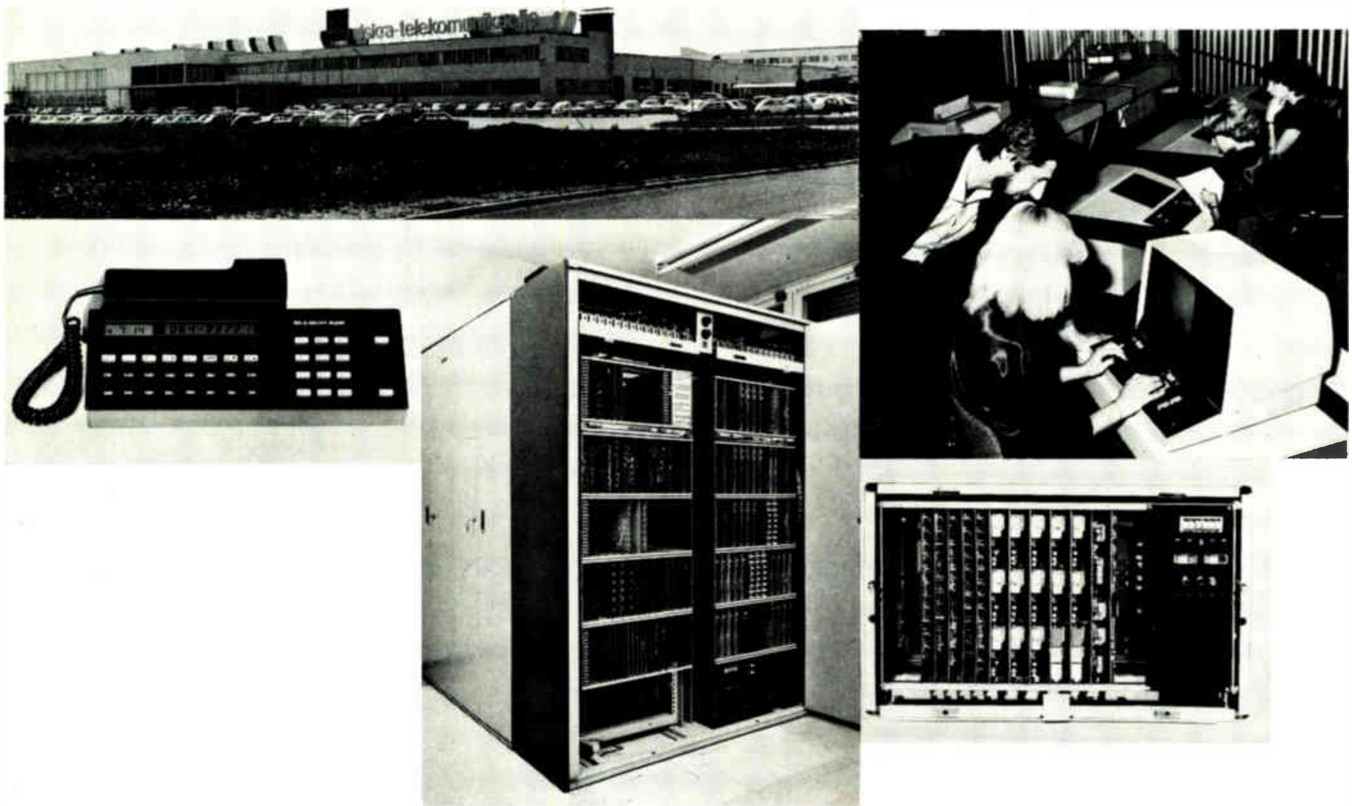
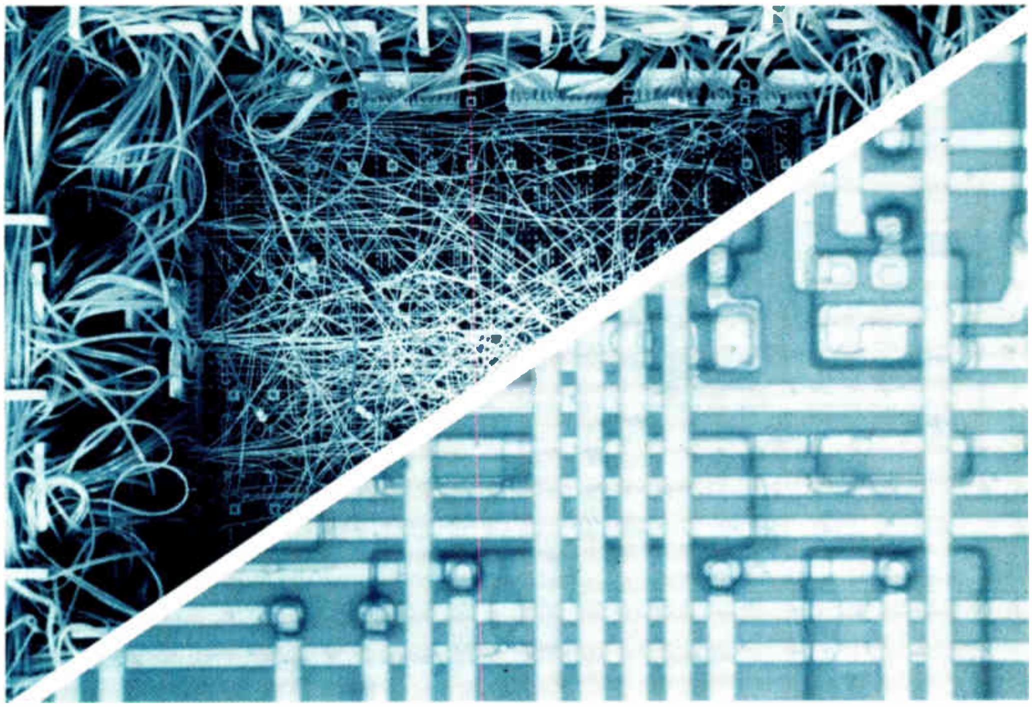




# The System/370 processor chip: a triumph for automated design

Programs for wiring up a complex gate array surmount the challenge of very large-scale integration

*☐ In the fall of 1978, a team at International Business Machines Corp.'s Data Systems division in East Fishkill, N. Y., mobilized to reduce the central processing unit of the System/370—the most prominent computer in the mainframe class—to a piece of silicon. In other words, the group was asked to position and wire nearly 5,000 logic gates on a master slice measuring 7 millimeters (276 mils) on a side. The gates comprise over 45,000 components on what might be the most complex bipolar integrated circuit built to date.*

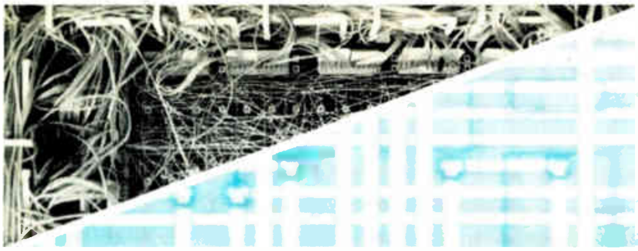
*This audacious experiment was undertaken to assay the effectiveness of IBM's automatic placement and wiring system for gate arrays by pushing it into the realm of very large-scale integration. The company wanted to know if this was a reasonable way to build an advanced microprocessor.*

*The three articles that follow outline the proceedings of that trial. To be sure, the undertaking was a success; but the jury is still out about the degree. One criterion is the definition of central processing unit, for IBM points out that its VLSI processor embodies only the data flow portion of the CPU. The accomplishment is nevertheless remarkable.*

*The first article in the series describes the architecture of the machine—that is, the paths over which the data flows between registers and arithmetic units. The second describes the automated design process used to position and interconnect logical blocks in the array. The third deals with the array's physical characteristics. It describes the internal cell and shows how such cells and the input receivers and output drivers are arranged on the die. This article also tells how the speed and power of the internal cells were adjusted to compensate for long on-chip interconnections.*

*The technology here is impressive, though it had really been proven previously—albeit with fewer gates and larger geometries. The points to ponder are that only nine months was required for logic entry, computer-assisted cell placement and interconnection, and test-pattern generation and verification; that these steps were carried out on a System/370, the same architecture that was being cloned; and that future turnaround time will be markedly reduced now that the CAD tools are in place.*

*Overall, this achievement is reassuring to everyone in the U.S. semiconductor industry who wants it to retain its position of technological leadership.* **-John G. Posa**



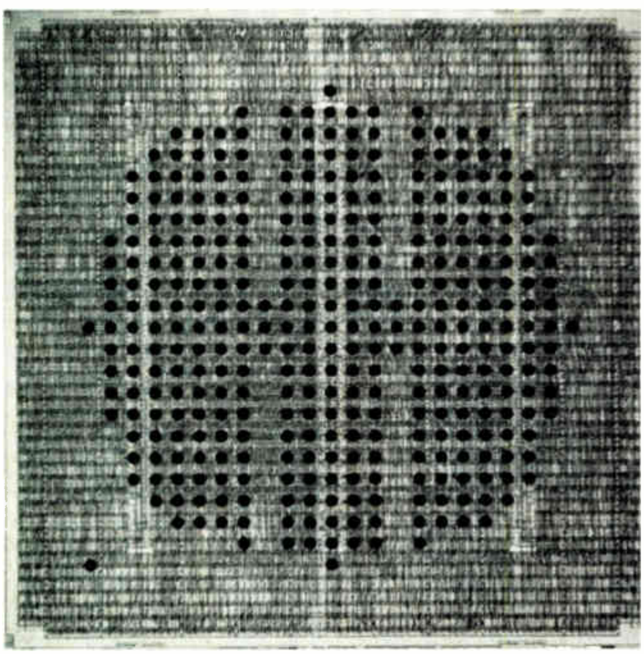
# Gate array embodies System/370 processor

by C. Davis, G. Maley, R. Simmons, H. Stoller, R. Warren, and T. Wohr, *IBM Corp., Data Systems Division, East Fishkill, N. Y.*

The central processing unit of a System/370 mainframe computer now sits on a single chip (see Fig. 1). The goal was to see if the computer-aided design of gate arrays could meet the challenge of very large-scale integration, and it can—only nine months were required to encode the processor's logic design, automatically place and wire the logic gates, and generate and verify the test patterns. No commercial production of the device itself is planned, however.

### On the chip . . .

Figure 2 shows how the chip connects to other system components, and Figs. 3 and 4 explain the chip architecture. A circuit count of nearly 5,000 and a 2.2-nanosecond NAND circuit—conservatively clocked at 4 ns—gives the machine a cycle time of 100 ns. The rich instruction set of the IBM System/370 requires a weighted average of 50 machine cycles for each instruction, resulting in a system performance rating of 200,000 instructions per second.



**1. Master mainframe.** Along 1,405 wiring channels and through 33,516 vias, 4,923 Schottky bipolar gates out of a possible 7,640 were automatically interconnected. The third and final metal level on the 7-by-7-millimeter (75,950-mil²) die ties to 200 I/O solder dots.

An 8-bit arithmetic and logic unit is all that can be permitted if hardware assists such as program relocation are to be included. A shared incrementer/decrementer (I/D) is used rather than counters, because sequential circuits can be difficult to test.

### . . . and off the chip

An off-chip control store, assumed to be read-only memory, provides overall control of the processor (see Fig. 2). The ROM word is 54 bits wide, including 3 parity bits. On the assumption that up to a quarter of a million bits of ROM would be required, a full 2 bytes of ROM addressing, gated off the CPU chip, is provided.

Enough pads (200) were supplied on the master slice to allow horizontal microprogramming. This means that system resources are controlled by microcode bits directly, without the need for vertical microprogramming. The directness of such an approach should reduce timing and logic errors, while its horizontal nature should lessen the testing problem and in general add to the flexibility of the chip.

The System/370 architecture requires many active registers that could not fit on the chip, so an off-chip high-speed local store is instead used for this purpose. Given the performance of the bipolar processor chip, this local store complies nicely with the requirement for a 100-ns machine cycle time. (The access time of the register bank is 60 ns.)

### Data flow

The 8-bit ALU, incrementer/decrementer, and both off-chip memories are controlled by the 54-bit microcode word, as shown in Figs. 3 and 4. The microcode is also responsible for its own sequencing.

The ALU performs its arithmetic and logic operations on two 8-bit binary numbers, producing one 8-bit binary result with carry and overflow signals. It can also perform the same operations on two packed 4-bit binary-coded decimal numbers or on 8-bit binary numbers that represent alphabetic characters. It produces negative numbers in the 2's complement form.

Its three 8-bit logical operations are OR, AND, and exclusive-OR. Its arithmetic operations may be controlled directly from a microcode ROM field or indirectly through a bit located in the status register, S. This indirect control allows microprogramming routines to be shared for adding and subtracting operations.

The output of the ALU is connected to a bus that is used to pass the data to a series of machine registers. As for the input, two registers, A and B, each hold a byte for the ALU. Fields in the ROM word decide how the contents of the A and B registers are presented to the ALU. This gating is important to decimal operations because it gives easy access to each of the two 4-bit hexadecimal digits in each byte. The two hexadecimal digits in the A register can also be swapped—a feature that is very useful for the packing and unpacking instructions required by the System/370 architecture.

The incrementer/decrementer is really a 24-bit binary arithmetic unit having limited capabilities. It can perform only eight arithmetic operations: add or subtract the values 0, 1, 2, and 3. The primary input to the I/D comes from the 24-bit memory-address register. A ROM field selects which of the eight arithmetic operations is to be performed, as well as which set of registers is to feed the memory-address register (MAR) and thus the I/D. The output of the I/D is always returned to the same set of registers that feed the MAR.

A 24-bit shifter with a very limited number of complex instructions is connected in parallel with the I/D. The shifter primarily handles the 12-bit address field used for page addressing in a virtual storage system.

**Memory control**

Twenty-four address lines from the processor chip address 16 million bytes of main storage—another requirement of the System/370 architecture. The chip can accept or transmit memory data in either 1- or 2-byte increments. For reasons of performance, however, a 2-byte interface is preferred and is assumed here.

The parity of each data byte from the main store is checked by the chip. Parity generators affix a parity bit to each memory data byte leaving the chip, and these bits are tested when the bytes return.

The two main memories with which the chip works can have different speeds. Since they share the same address and data buses, they cannot be referenced on the same cycle. Two independent signals, generated by a ROM field, leave the chip and select either memory or neither memory. This arrangement allows I/O devices to be affixed to the same set of address and data lines as the main memories.

The CPU will operate at almost any memory speed, since the memories are asynchronous with it. Any memory reference causes the processor to enter a wait state that lasts until a data-valid signal is received from the referenced memory. A separate control line from the chip requests a read or write operation.

A 16-bit ROM address is generated very early in each machine cycle to ready the next 54-bit microcode word (see Fig. 3). Thus, while one word controls the chip, the next word is being fetched. As the generation of the next ROM address requires 25 ns, the access time of the microcode ROM must be 75 ns for the 100-ns machine cycle time.

**ROM addressing**

The CPU generates 2 low-order bits of ROM address by examining conditions internal to the chip. Two fields in the ROM data word, one field for each bit, dictate which internal conditions the CPU is to consider. This technique provides a four-way conditional branch that appears to be adequate for a 1-byte CPU.

The next-higher 6 bits of the address are taken directly from a 6-bit field in the ROM data word, thereby enabling the ROM programmer to read any one of 64 words without consideration of the 2 branch bits. By setting each of the 2 branch bits to 0 or 1, a programmer can read any of 256 words without branching.

The memory address register is 3 bytes wide (refer to Fig. 4). Any bit pattern in this register will appear on the 24 address lines from the chip. The immediate source of the data to be placed in either the high-speed local store or the main memory is derived from one of four pairs of registers. Any of the 2-byte R, G, L, or H register pairs may be used as a memory-data register (MDR), significantly reducing the need for data transfer among registers. The G register pair has special ROM branching capabilities that dictate its use as an operation-code register.

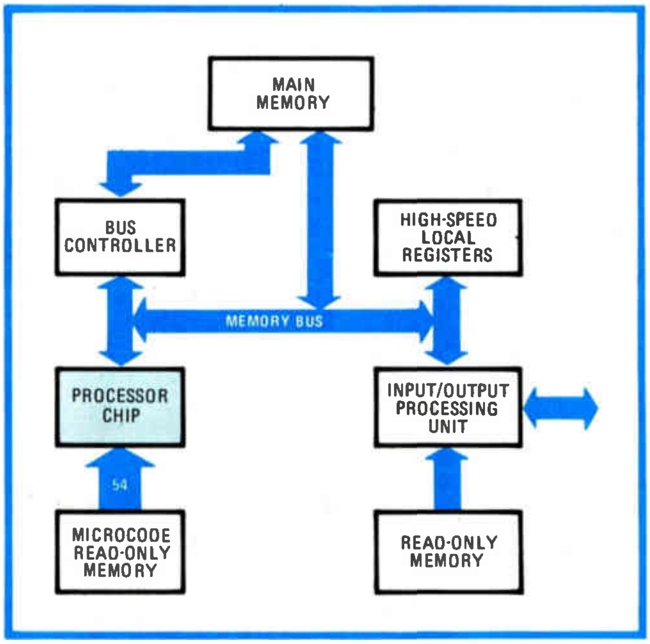
A 3-byte instruction counter (the I register) is updated by having its contents passed through the I/D. Another 3-byte register, U, serves as an operand-address register for main store; it, too, can be updated by the I/D. The 2-byte T register is used for addressing local store, limiting the size of the local store to 65,536, or 64-K, words. Although this feature is not shown in Fig. 4, the I, U, T, and R registers can pass 2 bytes of data—with or without displacement information—among themselves to aid in implementing the virtual storage requirements of the System/370 architecture.

**More registers**

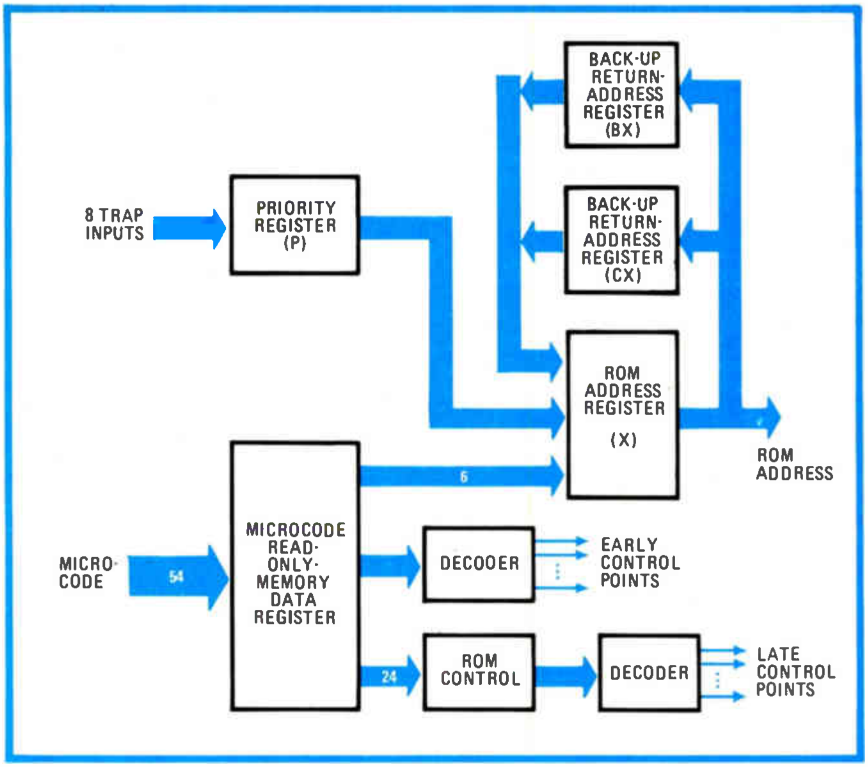
As mentioned, the S register is a CPU status register. The microprogram uses it for branching by altering the 2 low-order bits of the ROM address generated by the chip. The higher-order byte of the S register can be set and reset by external inputs.

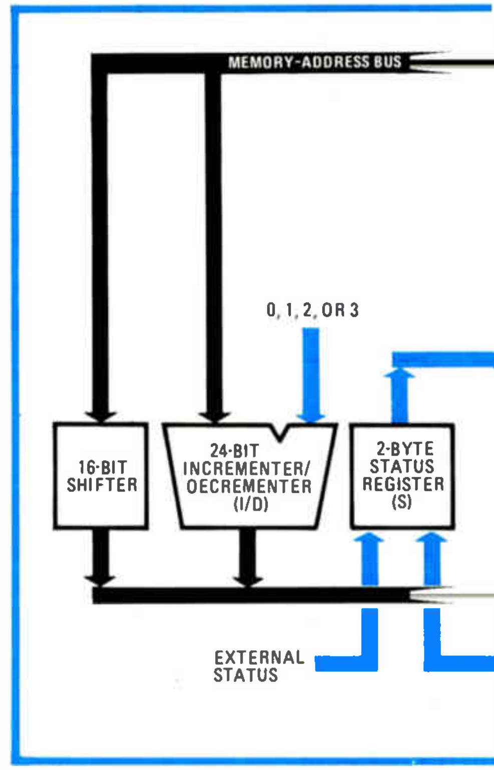
The 1-byte F register is for interrupts, and all 8 of its bits may be set in accordance with external conditions. The response to the setting of these bits is under control of the microprogram, and action is usually delayed until the end of a System/370 instruction. This delay time can therefore vary from a few to hundreds of machine cycles.

The execution of some System/370 instructions may require hundreds of microinstructions. It is therefore




**2. In its place.** To complete the System/370 architecture, the processor chip talks to main memory, a high-speed local store, and a separate I/O channel processor over a multiplexed memory bus. Microcode is brought in directly over a separate 54-bit bus.




**3. Decoding.** The 54-bit microcode gets divided up for control and sequencing of the microcode ROM itself. The next address is based upon bits from the ROM, from trap inputs, and from backup registers holding return addresses if a trap was taken.

advantageous to provide a hardware-forced micropro-gram-entry, or trap, system to transfer control between microprograms on a microinstruction boundary rather than on a macroinstruction boundary. Once included, this hardware can be expanded to solve other difficult control problems such as the handling of parity errors, push-button interrupts like those generated through a front panel, and memory wraparound.

## Eight trap levels

The processor chip incorporates eight trap levels, each of which forces a different address onto the ROM address lines. The eight levels are executed in the following order:

- Parity errors.
- Initial program load (IPL) request.
- Page overflow (virtual storage operation).
- Memory wraparound.
- Memory-protect violation.
- Stop request.
- I/O control.
- I/O control.

The last two levels are intended to handle high-speed I/O devices that cannot wait until the end of a System/370 instruction.

Once a trap has been taken, a latch is set and all future trapping is suspended until a microinstruction is executed to reset the latch. In addition, each of the seven low levels (all below parity error) can be individually masked off. As shown in Fig. 3, the ROM address register has two backup registers to save return addresses when a trap instruction is in progress.

No macrocircuits are used in the physical design of the logic. Every logic function on the chip—whether a register, latch, or one-shot—is created exclusively out of NAND gates.

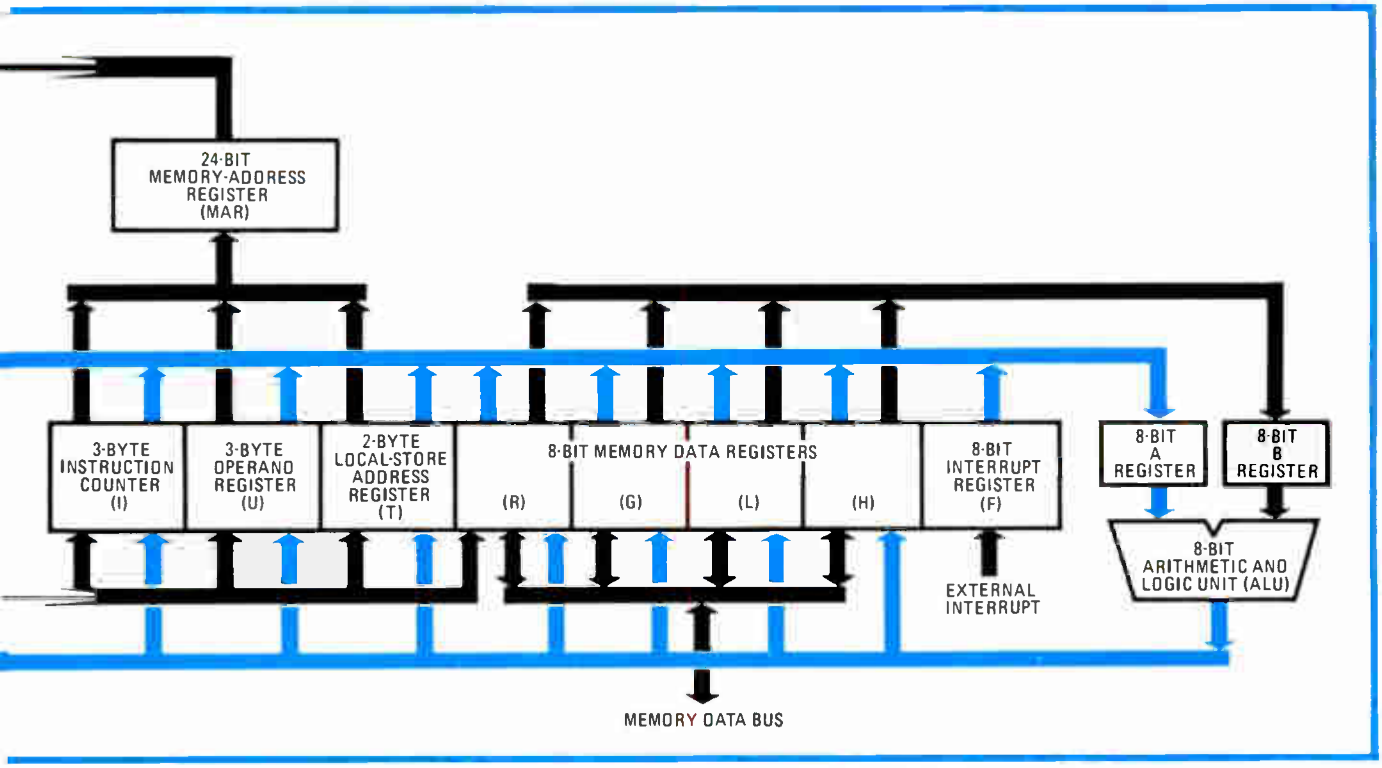
Furthermore, every function was designed so that the placement program could locate the component NAND blocks anywhere on the chip. For example, the latches were designed to operate even if the four NAND blocks comprising the network were located at each of the corners of the chip. This approach was adopted because it gave maximum flexibility to the automatic placement and wiring programs.

Redundant logic can improve performance and reliability. Unfortunately, it cannot be used if high test coverage of stuck faults is desired.

Performance enhancement was therefore achieved without redundancies. For instance, clock timing was used to eliminate logic glitches (noise). In addition, for easier testing, all clock lines can be activated by test input signals, allowing data to be flushed through the registers. As a result, the entire chip becomes one large combinatorial—rather than a sequential—network. Moreover, all registers may be loaded directly from input pads and read directly from output pads, which further enhances testability.

## Testing details

Manually generated test patterns were used to test the microprocessor chip. The initial objective was to select reasonably good chips from the first fabrication run through flush testing. Chips that passed this preliminary screening would then be mounted on modules and functionally exercised. The exerciser would clock the chips at full speed while executing test microcode.




**4. Architectural details.** An 8-bit arithmetic and logic unit adds and subtracts, ORs, ANDs, and exclusive-ORs. The 24-bit memory address register feeds a 16-bit shifter and a 24-bit incrementer/decrementer that is actually an ALU with limited functions.

A limited number of flush tests caught 40% of the stuck faults. Close to 100% may be caught by exercising the registers and propagating the stuck faults through the sequential circuits. Some test patterns could cause the chip to oscillate or lock up. These were spotted by means of a simulator and avoided.

The fault simulator produces an updated listing of the untested fault conditions. In working with this list, new test patterns are generated to cover the untested faults. Thus any degree of test coverage may be obtained.

## The physical design

In the case of this gate array, 4,923 circuits had to be placed within 7,739 cells and 10,605 interconnections had to be wired on a 800-by-600-channel grid.

Two placement methods were pursued: fully automated placement and iterative structured placement. The automatic method ignored the functionality of the logic and instead grouped and placed the logic blocks on the basis of the interconnection matrix. This was possible because the basic logic gate had been designed to operate independently of the position of its constituent NAND blocks. Since not all the cells of the chip had to be used, rows of horizontal cells were kept clear of NAND blocks in order to provide avenues for additional horizontal wiring channels.

Three different automatic placement passes were made, and the most promising was chosen for automatic wiring. Each placement pass required approximately three hours of IBM System/370 model 168 data-processing time, as well as several hundred cylinders of disk space.

The structured, iterative placement method was pursued as an alternative in case the fully automatic method was unsuccessful. In addition, this method gives the designer greater control during failure analysis and greater freedom to correlate the physical placement of a set of NAND blocks and their logical function.

The same automatic wiring program was used on placements resulting from both methods. The best fully automatic placement was wired with only 68 overflows. Wiring for the best structured method produced over 200 overflows. The detailed printout of the wiring required a plot measuring about 4 by 5 meters. Using this printout, and with the aid of a card input language to describe the wire additions and deletions, the 68 overflows were imbedded manually.

## Few errors

After wiring, a sophisticated pattern-recognition program for checking circuit shapes was used to test for ground-rule (geometry) violations and for logical and physical errors. The first pass through this program ferreted out just five errors in a total of 750,000 shapes involved in the design. Two of the errors were in the definition of the gate array and the other three were wiring violations.

The second pass was error-free. The shape-checking procedure required about four hours of processing time on the IBM System/370 model 168 and several hundred cylinders of disk space.

The physical design took about three months to complete. Allowance should be made for the fact that this was the first time that this array and automatic placement and wiring programs were used. A second-pass design would take much less time. ☐

# Computer-aided design wires 5,000-circuit chip

by M. Feuer, K. H. Khokhani, and D. Mehta
*IBM Corp., Data Systems Division, East Fishkill, N. Y.*

Automatic design aids that work well at one level of chip complexity may not succeed at a much higher level. Gate-placement and -wiring programs are crucial to the success of gate arrays much less complicated than the one needed to realize a System/370 microprocessor. Fortunately, with relatively minor modifications, the same design aids proved capable of organizing the logical elements into a 7-millimeter-square area.

Experience at IBM in the design of gate arrays dates back 10 years to the layout of 130-circuit bipolar chips and extends through the design automation of the 700-circuit logic chips in the System/38 and 4300 series to a 1,500-circuit bipolar gate array used in microcontroller applications. With its 5,000 gates, therefore, the System/370 processor chip quadruples the number of circuits and connections to be placed and wired. This adds a valuable empirical data point to a plot of the data-processing times required for the automatic placement and wiring of increasing numbers of circuits.

### Wirability analysis

The feasibility of wiring so many circuits was tackled from many angles. Various master-slice elements and cells were evaluated in terms of the difficulty of wiring them. Overall wiring requirements were estimated from a wirability model. At meetings with chip designers, the details of cell topology were optimized. A test chip, one quarter the size of the proposed chip, was described to an automatic design system and the gates of a small microprocessor were placed and wired. Finally, a wiring analysis tool, consisting of simplifed automatic placement and global wiring programs, was used on an early version of the logic to estimate how hard it would be to wire. In each case, the results confirmed the wirability of the proposed System/370 processor.

The various activities involved in designing and developing a gate array overlap considerably. The design and verification of the logic for this device began before the definition of the gate array and continued to within two months of its final layout. The wirability analysis was performed concurrently with both the design of the gate array and the coding of the data into the computer-aided design system. Necessary CAD programming changes began before the gate array data coding was completed, and these changes were tested on preliminary logic when the gate array data became available.

In parallel with the CAD programming changes, a special test chip was both designed and manufactured to verify the electrical characteristics of the gate array. In the end, with the design system and the gate array both in satisfactory condition, a final version of the System/370 microprocessor logic was placed and wired. By that time a stockpile of gate array wafers had collected, awaiting the metalization patterns that were all they required for completion (see figure).

### Automatic placement and wiring

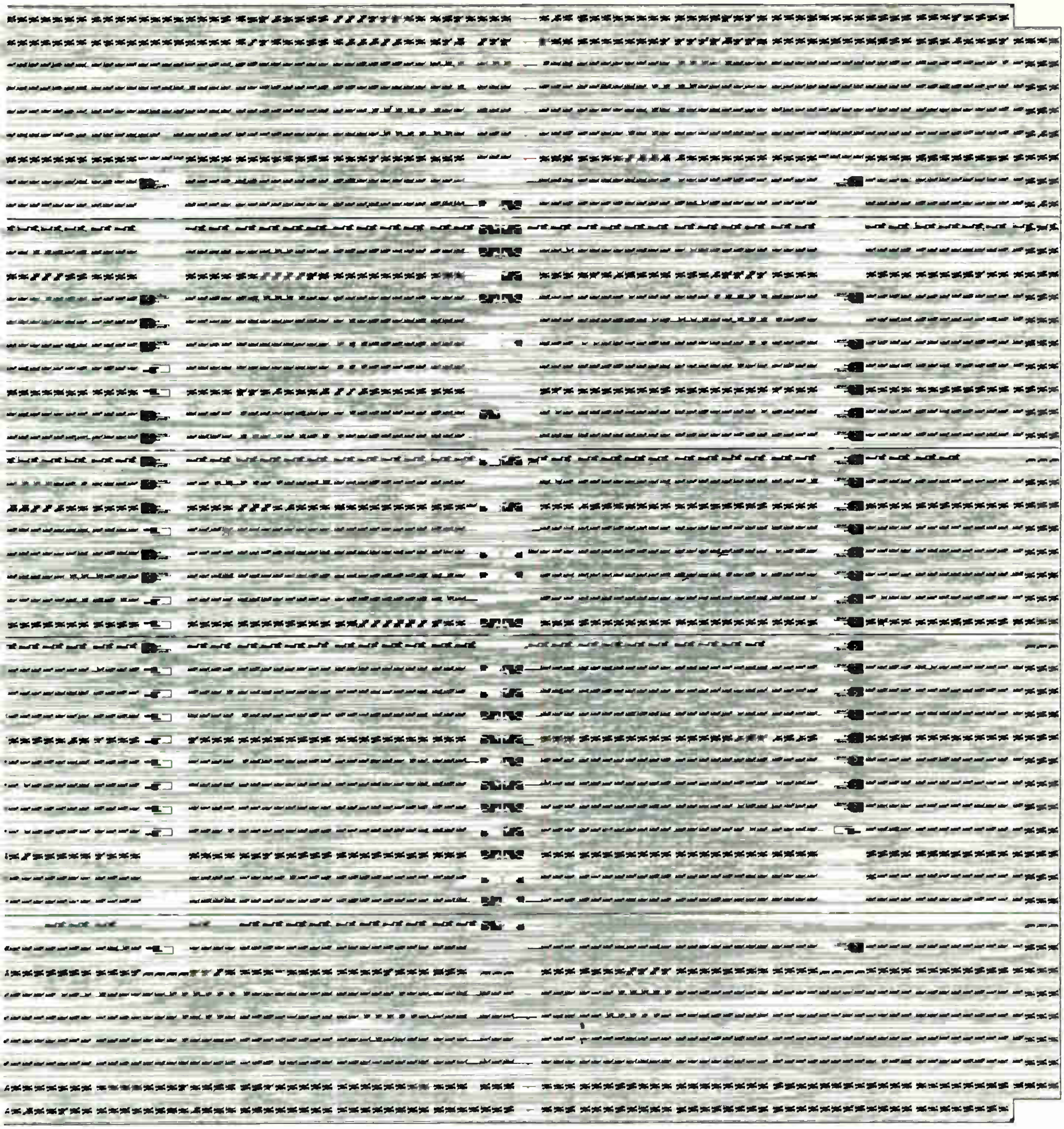
The design process consisted of the following 11 steps, of which all but the tenth were automatic:

- Clustering. The 5,000 circuits were clustered into 144 supernodes of highly interconnected gates.
- Constructive placement of supernodes. The supernodes were assigned in sequence to various regions of the chip, called supercells, according to the degree of their connectivity to neighboring supernodes.
- Supernode interchange. Pairwise exchanges of supernodes were evaluated and accepted if they decreased the number of wires crossing supernode boundaries.
- Supernode decomposition. Each individual logic gate was placed in sequence in, or as near as possible to, the region to which its supernode was assigned.
- Iterative interchange. Initial placement was improved through several efficient interchange techniques. Interchange algorithms were used to balance horizontal- and vertical-channel utilization, improve channel crossings of boundaries, reduce total conductor length, and attempt to reduce congestion of wires by moving gates from crowded into uncrowded zones. The iterative process ended when a highly wirable layout was generated.
- Global wiring. Wires were assigned to groups of channels to produce a feasible overall wiring pattern.
- Vertical assignment. The entry points of vertical wire segments into horizontal channels were determined.
- Horizontal line packing. A channel router wired the horizontal segments.
- Clean-up maze runner. A local maze runner, which exhaustively searched a small region of the chip for all possible routes, completed special unwired connections.
- Manual wire embedding. The remaining wires were routed manually.
- Checking. A series of topological and electrical tests was performed.

The final logic became available on June 15, 1979. Automatic placement and wiring were completed roughly one month later for all except 68 of the 11,000 connections. Manual wire embedding of these 68 and checking was completed on Aug. 15, 1979. The elapsed time of two months is long, compared with production schedules. Even so two months compares favorably with the time needed to design a VLSI chip manually.

The running time for automatic placement (the first five steps in the design process) was 208 minutes on an IBM System/370 model 168, and wiring time (the next four steps) was 87 minutes.

These placement and wiring running times, $T_p$ and $T_w$, in relation to the number of circuits involved, C, can be



**Complex.** This is just the first layer of metal wiring on the System/370 processor chip. If the individual segments were laid end to end, they would span 2.4 meters. The second metal layer is even more complex; it would stretch 3.4 m. The third level is used for power and ground.

combined with the experience gained from previous chips to yield the empirical scaling formulas:

$$T_p \propto C^{1.2}$$
$$T_w \propto C^{1.1}$$

Evidently then, the hierarchical nature of the placement and wiring algorithms leads to only a mild increase in running time with increasing chip complexity, given constant intrinsic wirability. The overall running times could be greatly reduced if more wiring channels were provided, but then chip size and manufacturing costs would be adversely affected.

The versatility and rapidity of designing with gate arrays has been proved yet again. Continuing advances in hierarchical automatic design tools, the inclusion of memory arrays, and technological advances that provide more wiring channels will further ensure this design style's future in very large-scale integration. □

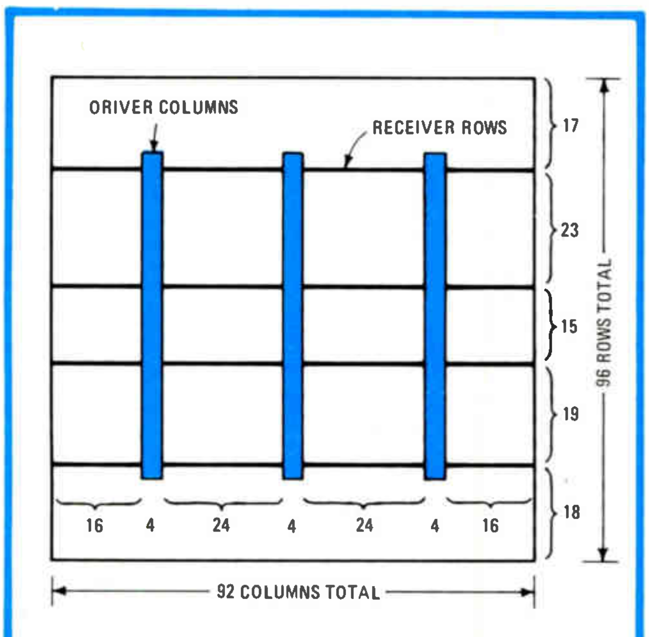
# Halving load resistances shortens long path delays

by A. H. Dansky
*IBM Corp., Data Systems Division, East Fishkill, N. Y.*

Long interconnections spell a high capacitance that can damage the performance of a very large-scale integrated circuit. In the case of the chip version of the System/370 central processing unit, some of the 5,000 logic gates are linked by interconnections more than 7 millimeters long—an unavoidable consequence of large functional chips. The microprocessor comprises 45,000 components at a density of 110 circuits per square millimeter.

To compensate for a long path's high capacitance, the drive capability of the basic logic circuit may be increased by lowering its output load resistance. This technique must be applied judiciously, however, as it also raises the gate's power dissipation.

It was to combine maximum performance at low power with minimum area that Schottky-clamped TTL was chosen for the basic CPU logic circuit. The circuit resembles the one used in the IBM 4300 computer series, except for the fact that it consumes less power.




**1. Arrangement.** The array has 96 rows, 4 of which contain receiver circuits, and 92 columns, including 12 for drivers. Three metal levels provide interconnections. Only about 65% of the internal logic gates are used, but the unoccupied cells provide extra wiring channels.

In fact, the semiconductor process used for the System/370 gate array is virtually identical to the one developed for the bipolar random logic chips contained in the 4300 series [*Electronics*, March 15, 1979, p. 105]. Its main features are a 2-micrometer-thick epitaxial layer, recessed oxide isolation, and three levels of metal for interconnections. For this chip, however, the circuit geometries have been scaled down from 3 to 2.5 $\mu$m.

The gate array consists of a matrix of 96 rows by 92 columns of basic cells (Fig. 1). Each cell may accommodate one circuit—either the internal logic gate or a driver or receiver circuit for input and output. As Fig. 1 shows, these drivers and receivers are interspersed with the internal logic gates, with the drivers arranged in 12 columns and the receivers in 4 rows.

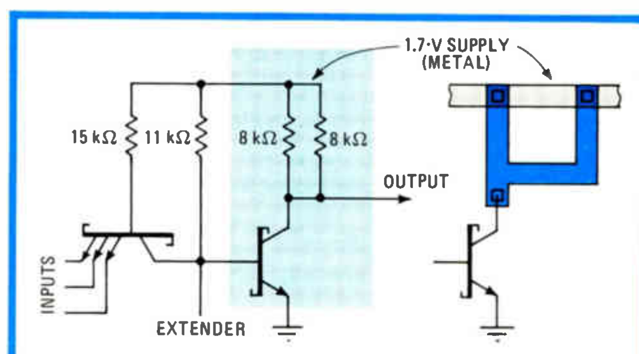
Altogether there are 7,640 internal cells, but only about 65% of them will be occupied by circuits. The unoccupied 35% of the internal cells provides additional wiring channel capacity. Each occupied cell provides 5 horizontal channels on the first level of metal and 10 vertical wiring channels on the second metal level. An unoccupied cell supplies an additional 4 horizontal channels, since no contacts to it are opened. The third metal level is used mainly for power distribution and I/O.

## Wiring statistics

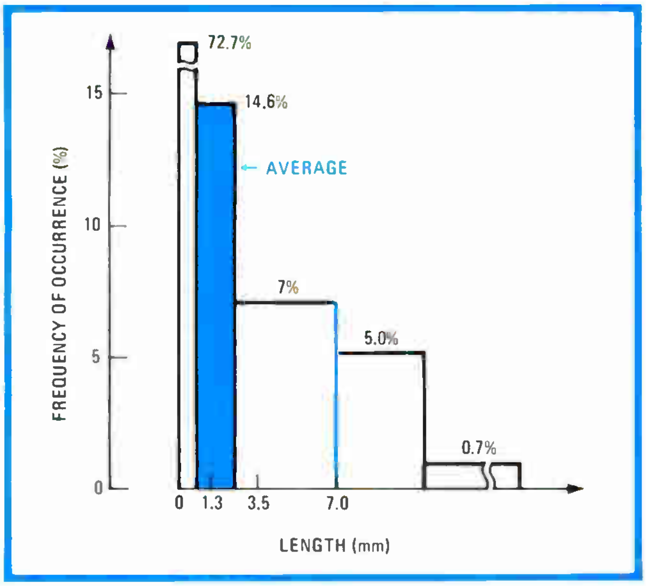
There are 1,404 wiring channels available on the chip after placement. This equals 80 columns of 10 vertical channels per column, or 800, plus 56 occupied rows of 5 horizontal channels per row, or 280, plus 36 unoccupied rows of 9 horizontal channels per row, or 324. Simulations and logic diagrams used logic macros such as registers and parity trees to simplify the logic description. But the physical design used only single circuits for maximum flexibility of placement and wiring.

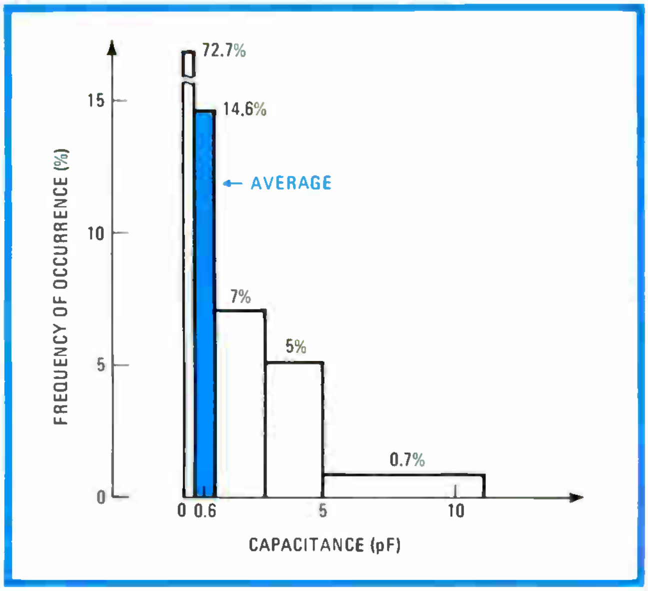
The basic internal logic gate shown in Fig. 2 has a speed-power product of 0.7 picojoule and requires a low power-supply voltage of 1.7 volts. The receivers and drivers for off-chip data, however, require a higher supply voltage of 3.4 V to cope with the greater external voltage swings. The total nominal power dissipated by the chip's 5,000 or so circuits is 2.3 watts, of which 1.6 W is consumed by the logic gates.

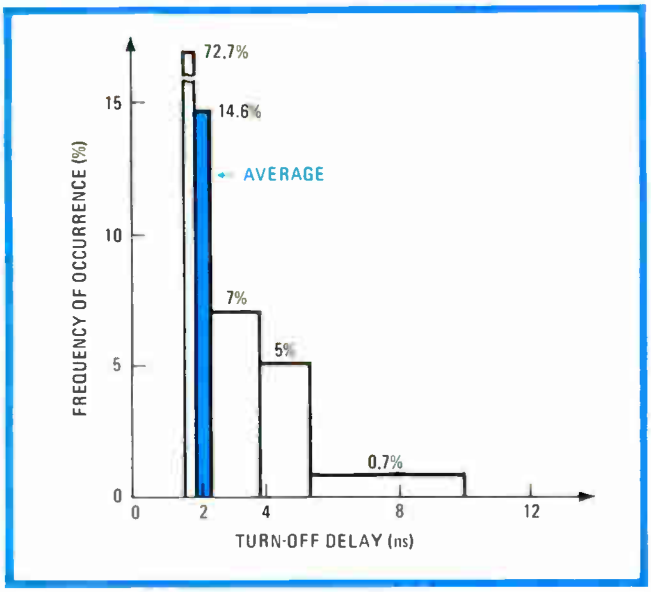
The total interconnection length is 5.8 meters, com-




**2. Ohm's law.** About 13% of the paths on the chip exhibited capacitive loading in excess of 1 pF. To circumvent speed degradation, two load resistances were given to the cells. When both are wired in, the pull-up value is halved and drive increased.




**3. Histograms.** One of the advantages of computer-assisted design is that statistical information is conveniently generated. It was decided to judiciously alter some load resistances in the circuit for more speed. Yet power consumption increased by only 0.1 W.

pared with the 2.2 m (typical) for the 704-circuit gate array used in the 4300 System/38. The average length of an interconnection path is then equal to 5,800/4,437 m, or 1.3 mm. To design for an optimum speed-power product, it is necessary to know not just the average but the distribution of path lengths also, since lengths significantly greater than the average increase the turn-off delay and degrade system performance.

The automatic placement and wiring programs were used to calculate the length, including stubs, of each of the 4,437 routes. As Fig. 3 shows, almost 6% of the paths exceed 7 mm.

The next step was to translate path length into total interconnection capacitance, so the distribution of circuit delay could be calculated. Given a single active load on a path, the sensitivity of the turn-off delay to load capacitance works out at 1.5 nanoseconds per picofarad for $R_L$ = 8 kilohms and 0.75 ns/pF for $R_L$ = 4 kΩ.

## Estimating capacitance

Using a wiring capacitance of 0.63 pF/mm for the first level of wiring and 0.2 pF/mm for the second, a capacitance histogram was calculated from the path-length histogram. The step height of this histogram is the same as for the length histogram, and it also has a long tail, with 6% of the paths, or 265 of them, having a total wiring capacitance greater than 3.0 pF. Such a high capacitance, if not counteracted, would slow down those 265 paths and degrade performance.

In fact, in this design, long paths with capacitance values of almost 10 pF occurred in the output bus of the arithmetic and logic unit, which drives 19 working registers. So these circuits were powered up by reducing the collector pull-up register from 8 kΩ to 4 kΩ (Fig. 2). In fact, all 13% of the circuits exhibiting a capacitive load greater than 1 pF used the 4-kΩ pull-up resistor.

Figure 3 gives the distribution of turn-off delay for all of the circuits on the chip. The delay variation includes only the difference in turn-off delay due to the load capacitance that each internal circuit must drive on chip. Even with the 4-kΩ pull-up resistor, 6% of the circuits have a turn-off delay more than twice the average. But, if the 8-kΩ pull-up resistor had been used exclusively, the turn-off delay for 6% of the paths would be greater than three times the average. In sum, then, the turn-on delay distribution is narrower, since its sensitivity to load capacitance is less.

The increase in average power for the 13% of the circuits utilizing the 4-kΩ pull-up is 0.17 milliwatt. Thus, total chip power increases by only 4.5%—0.13 times 4,700 times 0.17 mW, or 0.1 W. The selective use of the 4-kΩ pull-up resistor, therefore, gives a good power-performance gain. ☐

The three articles presented here are based on papers prepared for the Institute of Electrical and Electronics Engineers' International Conference on Circuit and Computers '80 (Oct. 1-3). The papers are "Bipolar Circuit Design for VLSI Gate Arrays," by A. H. Dansky; "System/370 Bipolar Gate Array Microprocessor Chip," by C. Davis *et al*; and "The Layout and Wiring of a VLSI Microprocessor," by M. Feuer *et al*. The copyrights to the papers belong to IEEE.

# Adding to PLL chips' functions speeds rf synthesizer design

## Programmable phase-locked-loop ICs contain reference oscillator and divide-down counters, offer dual-modulus prescaling

by John Hatchett, *Motorola Inc., Semiconductor Group, Phoenix, Ariz.*

☐ A new family of large-scale integrated circuits is now available to provide those designing rf synthesizers with breakthroughs in performance, power drain, cost, and space. Each chip in the family provides large blocks of phase-locked-loop circuitry, thus reducing the effort in designing all kinds of radio-frequency equipment. By using complementary-MOS technology, this family of circuits has the added appeal of drawing a minimum of power over a wide range of supply voltages.

Applications abound for these easily implemented phase-locked-loop ICs. They include avionics, navigation and communications equipment, mobile radio transceivers, marine radio and sonobuoys, amateur radios, scanner receivers, cable and broadcast television tuning systems, and a-m/fm radios.

Each member of the MC145100 family of PLL synthesizer chips contains a reference oscillator, a selectable reference-frequency divider, a digital phase detector with a lock-detection output, and at least one programmable divide-by-N counter.

Some of the chips have a dual-modulus prescaling capability for extended frequency range (see "Dual-modulus prescaling"). With the loop filter, voltage-controlled oscillator, and suitable dual-modulus prescaler needed to complete the PLL circuit, these ICs can synthesize frequencies to over 500 megahertz.

Frequency is selected by programming the divide-by-N and, where applicable, the divide-by-A counters with either a serial bit stream, a fully parallel word (14 or 16 bits wide), or coding on a 4-bit bus. The family's variety of frequency-selection schemes and other on-chip features allow the designer to minimize the need for additional components for an application (see Table 1).

Highlights of the synthesizer family are:
- 30-MHz input capability (typical at 25°C, 5 volts dc).
- Operation at 3 to 9 volts dc.
- Low power drain.
- −40° to +85°C operating temperature.
- Linear detector response.
- Low input drive level (500 millivolts peak to peak).
- On-chip latches and shift registers for serial and 4-bit-bus designs.

Interfacing the frequency synthesizers with microprocessor or microcomputer controllers is best accomplished employing the chips offering serial or 4-bit-wide inputs: the parallel-programmed devices interface best with mechanical switches, diode matrixes, and programmable read-only memories. The parallel input designs are housed in 0.6-inch-wide, 28-pin packages, and the other units come in narrow-lead-frame, 0.3-in.-wide, 16-, 18-, or 20-pin packages.

There are seven chips in the family. Each of the three programming methods (serial, parallel, and 4-bit data bus) is represented by both a single- and a dual-modulus

TABLE 1: FEATURES OF THE MC145100 FREQUENCY-SYNTHESIZER CHIP FAMILY

| Programming method | Features | Part number | Modulus | Number of pins |
|---|---|---|---|---|
| 4-bit data bus | • latches<br>• enable/chip-select<br>• software-programmed reference divider | MC145144 | single | 16 |
| | | MC145145 | single | 18 |
| | | MC145146 | dual | 20 |
| Fully parallel | • pull-up resistors on all programming lines | MC145151 (receive/transmit shift function) | single | 28 |
| | | MC145152 | dual | 28 |
| Serial bit stream | • shift registers<br>• latches<br>• enable<br>• latched outputs for use as system switching functions | MC145155 | single | 18 |
| | | MC145156 | dual | 20 |

## Dual-modulus prescaling

Dual-modulus prescaling, used with three of the MC145100 family of large-scale integrated circuits, is a well-established method for designing high-performance high-frequency synthesizers. The technique allows the relatively low-frequency programmable counters on the synthesizer chip (the divide-by-A and divide-by-N functions of the MC145156, -52 and -46 devices) to function as a single high-frequency programmable counter. Actually, the lower-frequency counters on these ICs are used to control external high-speed chips called dual-modulus prescalers. The prescaler consists of one or sometimes two ICs made for this purpose. This control is done with the aid of special logic on the LSI chip for selecting one of two prescaler division values, either P or P + 1.

The division control signal generated by the synthesizer chip is supplied to the prescaler in a specific, timed format: the division value is P + 1 while A is counting down and P when A has stopped and N is counting the rest of the way down. Thus the low-frequency on-chip counters control the high-frequency prescaler. Note that $N \geq A$ is a requirement for using dual-modulus prescaling.

The greater the total system division value, $N_{total}$, the higher the output frequency of the synthesizer. $N_{total}$ is a function of three input values: the prescaler division value, P; the value of A, programmed into the divide-by-A counter; and the value of N, programmed into the divide-by-N counter. The relationship is:

$$N_{total} = NP + A$$

To see how this equation is applied, consider the problem of tuning a radio receiver. A maximum resolution over the widest possible frequency range is desirable. For the minimum frequency increment, N is therefore held constant and A is varied between 0 and P − 1 in integral steps. N is then incremented to N + 1 and A is again incremented sequentially from 0 to P − 1. In effect, the system performs tuning in two stages—first coarse, then fine. The procedure is used over the entire $N_{total}$ range. The actual tuning increment is equal to the reference frequency, $f_R$. Without dual-modulus prescaling—that is, with fixed prescaling—the tuning increment is $P' \times f_r$, where P' is the division value for the fixed prescaler.

A dual-modulus prescaler can operate up to the speed capability of the prescaler chip without sacrificing system resolution or performance, which would occur if a fixed (single-modulus) divider was used for the prescaler. High frequency is achievable because the dual-modulus prescaler must divide by only two different values (P or P + 1) and can therefore be designed for high operating speeds comparable to those of fixed dividers.

Motorola's dual-modulus prescaler chips, off-the-shelf parts, offer speeds to over 500 megahertz. They are used individually or in some cases combined with an additional counter IC to provide a variety of P and P + 1 values to best serve the application at hand. Figures 4 and 5 (pp. 153 and 154, respectively) show two examples.

The 145156, -52, and -46 chips can control prescaler division values that range from 3 and 4 through 128 and 129 (for the -56 and -46 devices) or 3 and 4 through 64 and 65 (for the -52).

version, and chips with 4-bit-wide data input include an extra single-modulus version designed specifically for television tuner applications, bringing the total number of chips to seven. Figure 1 depicts the internal functions of the chips, the variations available, and the external components required to complete the PLL. Table 2 sum marizes the chips' basic characteristics.

### Dual-modulus requirements

The MC145156, -52, and -46 are for use in synthesizers that employ the dual-modulus prescaling concept. Each contains the circuitry for all the lower-frequency functions, along with the modulus control signal for operating the prescaler in the divide-by-P or divide-by-P + 1 mode in the properly timed format for performance to over 500 MHz.

Synthesizing high frequencies using the dual-modulus concept requires a special high-speed counter, or prescaler. By matching a synthesizer chip with one or more of the ICs that make up the prescaler (Motorola makes a series of them), a designer may tailor a system to meet a variety of speed, performance, and cost goals.

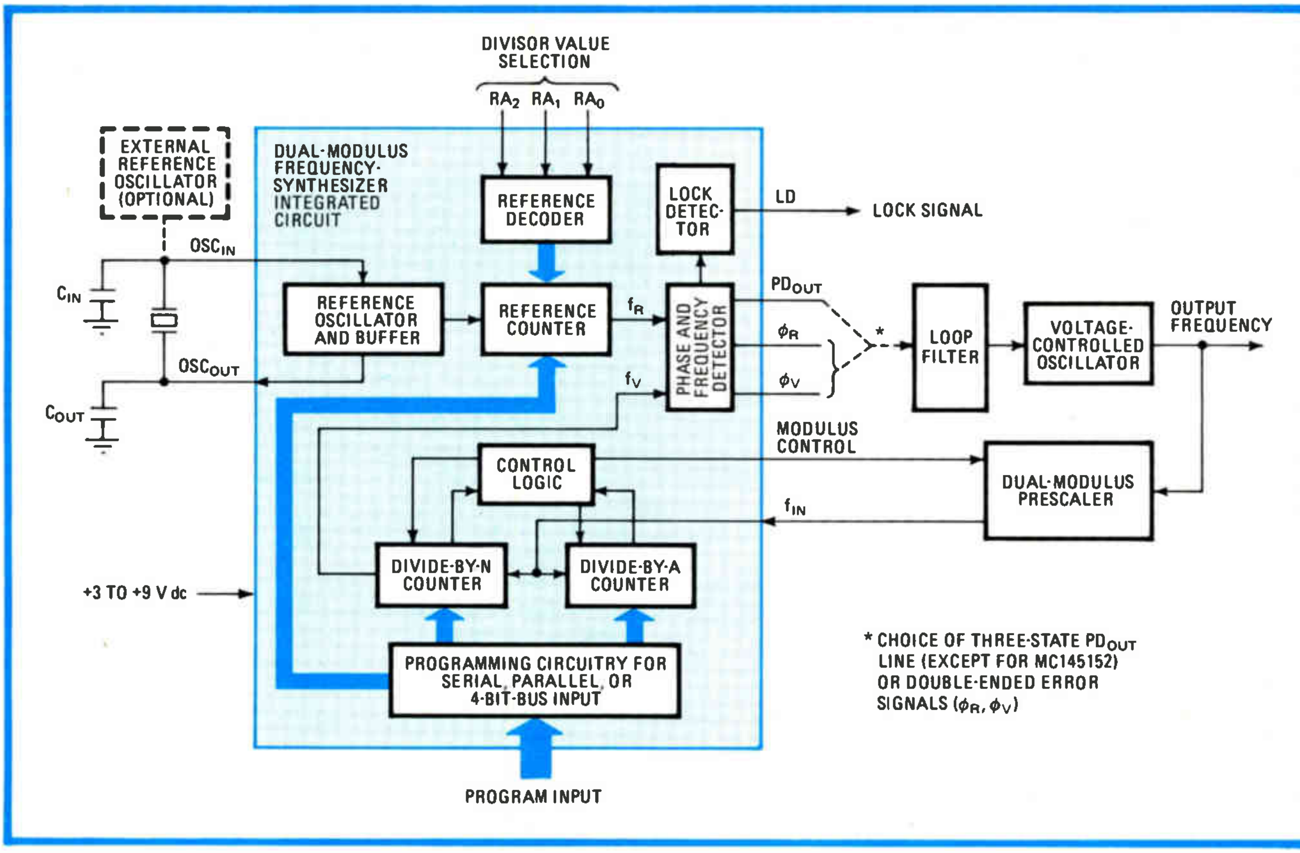
The MC145156 and -46 contain 10-bit divide-by-N and 7-bit divide-by-A counters and can control prescalers having division values (P and P + 1) ranging from 3 and 4 through 128 and 129. Depending on the prescaler selection, a range from 9 to 131,199 in steps of unity can be achieved for the total system division value, $N_{total}$. The availability of only 6 bits in the MC145152's divide-by-A counter restricts it to controlling prescalers having division values of 3 and 4 through 64 and 65. In this case, the upper $N_{total}$ limit is limited to 65,599.

The other four devices, the MC145155, -51, -45, and -44 are used when programmability at higher frequencies using dual-modulus prescaling is not required. Since a modulus control signal is not generated, these ICs employ a single counter for the divide-by-N function. Except for the MC145144, the counter contains 14 bits and can be programmed to divide by 3 through 16,384. The 145144, although similar to the -45, is optimized specifically for TV tuning system designs and employs a fixed divide-by-256 prescaler.

Typical frequency characteristics are given in Fig. 2. As shown in Fig. 2a, the use of high-amplitude drive levels will have little effect on the maximum operating frequency for drain supply voltages, $V_{DD}$, less than about 5 V. However, for higher $V_{DD}$ levels, high drive levels can increase the maximum frequency significantly.

Current drain is predominantly set by the counters and the driving-signal frequencies. Except at extremely low frequencies, the other on-chip functions will produce only secondary current-drain effects. This results in about the same total drain current value, $I_{DD}$, for all members of the family under the same operating conditions. From Figs. 2b and 2c a characteristic plot of $I_{DD}$ as a function of voltage and frequency can be drawn to determine the current requirements with large-amplitude (rail-to-rail) input signals.

With low-amplitude drive levels (500 mV p-p), the current will remain essentially as shown in Figs. 2b and




**1. Integrated.** The MC145100 family of C-MOS frequency synthesizer chips contain the bulk of the circuitry needed to implement a phase-locked-loop design. Dual-modulus prescaling for higher-frequency operation is optional on three of the family's seven members.

2c for a $V_{DD}$ of 3 V. For the 5- and 9-V conditions and for operating frequencies in excess of a few hundred kilohertz, higher current drain results.

The reference oscillator and buffer on each chip is used for developing a crystal-controlled reference signal by connecting an external fundamental-mode crystal that is parallel-resonant at the desired operating frequency and by loading the crystal with two capacitors, $C_{in}$ and $C_{out}$, to ground (see Fig. 1 again).

The acceptable loading capacitance, $C_L$, seen by the crystal depends upon the oscillator frequency. For a $V_{DD}$ of 5 V, $C_L$ should not exceed 32 picofarads for frequencies up to approximately 8 MHz, 20 pF for frequencies in the range of 8 to 15 MHz, and 10 pF for frequencies above 15 MHz.

These guidelines for $C_L$ take into account IC-capacitance drive capability, variations in stray and IC input/output capacitance, and realistic crystal load-capacitance values. The load capacitance, $C_L$, presented across the crystal can be estimated to be a $C_{in\,total}$ in series with a $C_{out\,total}$, where:

$$C_{in\,total} = C_{in} + C_{in\,IC} + C_{in\,stray}$$
$$C_{out\,total} = C_{out} + C_{out\,IC} + C_{out\,stray}$$

with $C_{in\,IC}$ and $C_{in\,stray}$ representing the capacitance to ground at $OSC_{in}$ contributed by the integrated circuit and stray circuit effects, respectively. Similarly, $C_{out\,IC}$ and $C_{out\,stray}$ apply to the $OSC_{out}$ pin. $C_{in}$ and $C_{out}$ are capacitors that are added to achieve the proper $C_L$ value. They should be chosen to make $C_{in\,total}$ and $C_{out\,total}$ approximately equal. In practice, $C_{in}$ and $C_{out}$ will be nominally equal. The oscillator can be trimmed to frequency by making a portion or all of $C_{in}$ variable.

The 145156, -55, and -45 provide a buffered oscillator output, $REF_{out}$, for use in other system functions. For the 145152, -51, and -46, the oscillator signal can also be obtained by lightly coupling to $OSC_{out}$. This can be done by using a capacitor-tap impedance-transformation network for $C_{out}$.

An off-chip reference source can also be used to drive the oscillator input. The reference signal is applied to $OSC_{in}$ and the crystal, and $C_{in}$ and $C_{out}$ are omitted. The oscillator circuitry now behaves as a buffer amplifier. The external reference signal will typically be ac-coupled to $OSC_{in}$, but for high-amplitude signals (standard C-MOS logic levels), dc coupling may be used.

### The reference counter's role

The reference counter divides down the high-frequency reference signal to the desired comparison frequency, $f_R$, which is fed into the phase detector. When using the 145156, -55, -52, and -51, the user chooses one of eight possible division values with a 3-bit code applied to division-value select pins $RA_0$, $RA_1$, and $RA_2$.

The reference counters in the 145146 and -45 are fully user-programmable for integers 3 through 4,096 with a 12-bit binary code. Typically, the desired division value is selected by software through a microprocessor or microcomputer interface with the synthesizer's 4-bit-bus programming structure.

The digital phase-frequency detector on the synthesizer chips compares positive-going edges of its two phase-compared input signals ($f_R$ and $f_V$) and generates output error signals $PD_{out}$, $\phi_R$, and $\phi_V$ as pulses of varying widths whenever the $f_R$ and $f_V$ edges are not in alignment (Fig. 3).

The error signals are filtered by the loop filter and thus establish the control voltage for a voltage-controlled oscillator. Except with the 145152 and -44, the user is provided a choice of either double-ended ($\phi_R$, $\phi_V$) or single-ended ($PD_{out}$) error information. The -52 offers only $\phi_R$ and $\phi_V$ and the -44 only $PD_{out}$.

Outputs $\phi_R$ and $\phi_V$ are well suited for use with loop filters that provide common-mode rejection and summing properties such as those employing operational amplifiers. $PD_{out}$ is a three-state output and presents a high impedance and a minimum of error-signal energy to be filtered when the loop is locked—in other words, when $f_R$ and $f_V$ are equal in frequency and phase.

Previous detectors for frequency-synthesizer applications have typically exhibited large changes in gain (sometimes changing by an order of magnitude) near the zero, or phase-lock, point. This can result in many system design difficulties and compromises in loop performance. The detector used in the 145100 chips produces a linearized response that provides a relatively constant detector gain through the phase-lock region and synthesizer performance better than that of previous designs.

The user can maintain some flexibility in indicating an in-lock or out-of-lock condition by using the lock-detection output. When the loop is locked, a lock-detection pin, LD, is high except for a narrow low-level pulse (normally 100 nanoseconds wide for a $V_{DD}$ of 5 V). When the loop is not locked, LD pulses low during the time an error signal of either polarity is generated (see Fig. 3 again). Typically, output LD is integrated and used to bias a transistor switch on and off. In this way, the user can assign the point when a phase-lock condition is actually to be indicated.

### Programmable counters, too

The 145155, -51 and -45 contain a single 14-bit counter for the divide-by-N function. Those that control an external dual-modulus prescaler—the 145156, -52, and -46—must have this function made up of two separate counters. This is implemented using a 10-bit counter, designated divide-by-N, and either a 7-bit or 6-bit (145152) counter, designated divide-by-A. In addition, a fully programmable 12-bit reference counter is provided in the 145145 and -46. The division value of each counter corresponds to the number (in binary code) applied to the counter's programming inputs. The only exceptions are when binary codes having a value of less than 3 are applied to the divide-by-N and reference counters. For these cases, a binary zero code gives a division value of $2^b$, where b is the number of bits of the counter. Division values for binary codes of 1 and 2 are not specified.

All the counters are preceded by buffer stages to allow the use of low-amplitude inputs (500 mV p-p) when ac coupling is used. If a large-amplitude signal is available (standard C-MOS logic levels), dc coupling may also be used. For optimum performance when ac coupling is employed, input signals should be symmetrical.

**TABLE 2: CHARACTERISTICS OF THE MC145100 FAMILY OF FREQUENCY-SYNTHESIZER CHIPS**

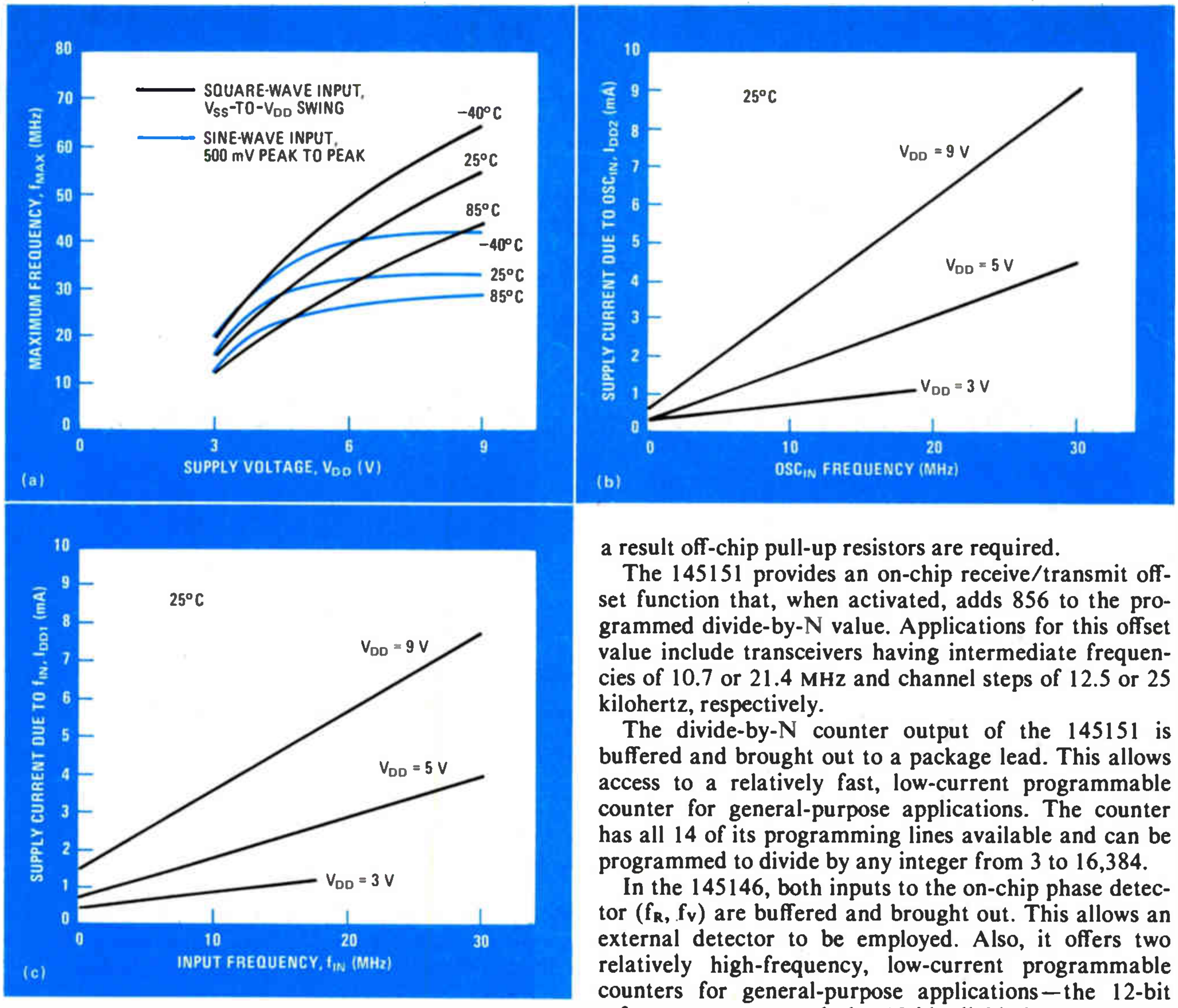
| | |
|---|---|
| Operating voltage | 3 to 9 V dc |
| Typical current drain, with $f_{IN}$ = $OSC_{IN}$ = 10 MHz and $V_{DD}$ = 5 V, at 25°C | 4 mA dc |
| Operating temperature | −40° to +85°C |
| Maximum $f_{IN}$, with 500-mV peak-to-peak sine wave and $V_{DD}$ = 5 V | 15 MHz minimum |
| System frequency | > 500 MHz |
| Dual-modulus prescaler range<br>MC145156, -46<br>MC145152 | <br>divide by 3 or 4 through 128 or 129<br>divide by 3 or 4 through 64 or 65 |
| Maximum total division value ($N_{TOTAL}$) with dual-modulus prescaling<br>MC145156, -46<br>MC145152 | <br>131,199<br>65,599 |
| Time required to generate modulus control signal, at 25°C, with $V_{DD}$ = 5 V | 50 ns typical, 100 ns maximum |
| Divide-by-N range, MC145145, -51, and -55 | 3 through 16,384 |

The control logic generates the modulus control signal. This signal is used to establish the divide-by-P and divide-by-P+1 format of an external dual-modulus prescaler and therefore allows the 145156, -52, and -46 to function in dual-modulus prescaling modes.

The modulus control is dc-coupled to the prescaler's control input and will interface directly with most existing dual-modulus prescaling ICs. The prescaler should divide by P for a high signal on its control line and by P+1 for a low signal. The prescaler's output should make a low-to-high transition after each group of P or P+1 input cycles to the prescaler. This action provides the proper interface to the positive-edge–triggered divide-by-A and divide-by-N counters, maximizing the time available for generating the modulus control signal and thus optimizing system frequency capability.

The modulus control signal is low at the beginning of a count cycle and remains low until the divide-by-A counter has counted down from its programmed value, A. At that time, the modulus control signal is set high and remains high until the divide-by-N counter has counted the rest of the way down from its programmed value, N. This will be N − A additional counts, since both divide-by-N and divide-by-A counters are decrementing during the beginning of the cycle. The modulus control signal is then set back low, the counters are preset to their respective programmed values, and the sequence is repeated. This order of timed events results in a total programmable divide value for the system defined by $N_{total}$ = $N \times P + A$, where $N \geq A$.

When using dual-modulus prescaling, the maximum input frequency, $f_{in}$, for the 145156, -52, or -46 is usually not limited by the speed capability of the divide-by-A or divide-by-N counter, but is dictated by the propagation time through the prescaler (period a), the prescaler's control-input setup or release time (period b), and the




**2. Performance.** Maximum operating frequency (a) is achieved by increasing both supply and drive-signal voltages. Current drain is primarily a function of reference oscillator frequency (b) and input frequency (c). The total current is the sum of $I_{DD1}$ and $I_{DD2}$.

time required for the LSI synthesizer to generate the modulus control signal (period c).

The $f_{in}$ signal must be low enough in frequency so that its period is greater than the sum of periods a, b, and c. Two of these factors (a and b) are determined by the user's dual-modulus prescaler implementation. Period c is a factor determined by the LSI device and is typically 50 ns for a $V_{DD}$ of 5 V (see Table 2 again).

For added flexibility, both the 145155 and -56 provide two latched open-drain outputs, $SW_1$ and $SW_2$, for system switching functions. These functions are controlled by the first 2 bits in the serial data stream used to program the ICs and may be used in any way to aid the designer or enhance the system.

A logic 1 in the control bit causes the respective switch output to assume a high-impedance state, and a logic 0 causes the output to sink current and provide a low impedance. Both switches use an open-drain configuration capable of controlling dc levels to over 15 V, and as a result off-chip pull-up resistors are required.

The 145151 provides an on-chip receive/transmit offset function that, when activated, adds 856 to the programmed divide-by-N value. Applications for this offset value include transceivers having intermediate frequencies of 10.7 or 21.4 MHz and channel steps of 12.5 or 25 kilohertz, respectively.

The divide-by-N counter output of the 145151 is buffered and brought out to a package lead. This allows access to a relatively fast, low-current programmable counter for general-purpose applications. The counter has all 14 of its programming lines available and can be programmed to divide by any integer from 3 to 16,384.

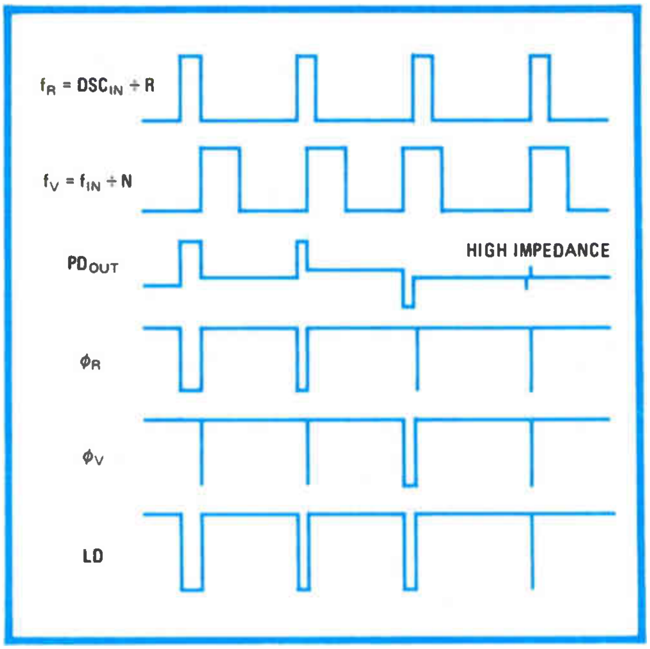
In the 145146, both inputs to the on-chip phase detector ($f_R$, $f_V$) are buffered and brought out. This allows an external detector to be employed. Also, it offers two relatively high-frequency, low-current programmable counters for general-purpose applications—the 12-bit reference counter and the 10-bit divide-by-N counter. Both are programmed using a 4-bit data-bus structure.

## Programming the counters

The serial and 4-bit–bus devices are typically used in systems employing a microprocessor or microcomputer for the programming interface. The parallel units can serve in these applications also but are frequently at a disadvantage because they require a large number of interface connections.

For the serial devices, the 145155 and -56, programming involves only three interface lines: the data, clock, and enable lines. Programming is accomplished by clocking data serially into the on-chip shift registers and then transferring their contents into latches with the enable line. Each low-to-high clock transition causes the registers to shift right 1 bit as each data bit is shifted in on the data pin at the time of the clock transition. (As mentioned, the first 2 bits control the two open-drain switch outputs, $SW_1$, and $SW_2$, instead of programming the counters.)

An inhibiting feature, activated by holding enable low, allows new data to be entered without affecting the previously programmed information. The programming




**3. Phase-locked.** When the divided-down frequencies of the reference oscillator and the input are locked in phase, the detector output assumes a high-impedance state; the double-ended outputs and the lock-detector ouput are reduced to narrow slivers.

interface can be reduced to only two lines, the data and clock lines, by holding the enable line high. However, under this condition all program changes are continuously transferred to the latches and counters, resulting in erroneous information being entered during the programming time-frame. Depending on the application, such errors may or may not be acceptable.

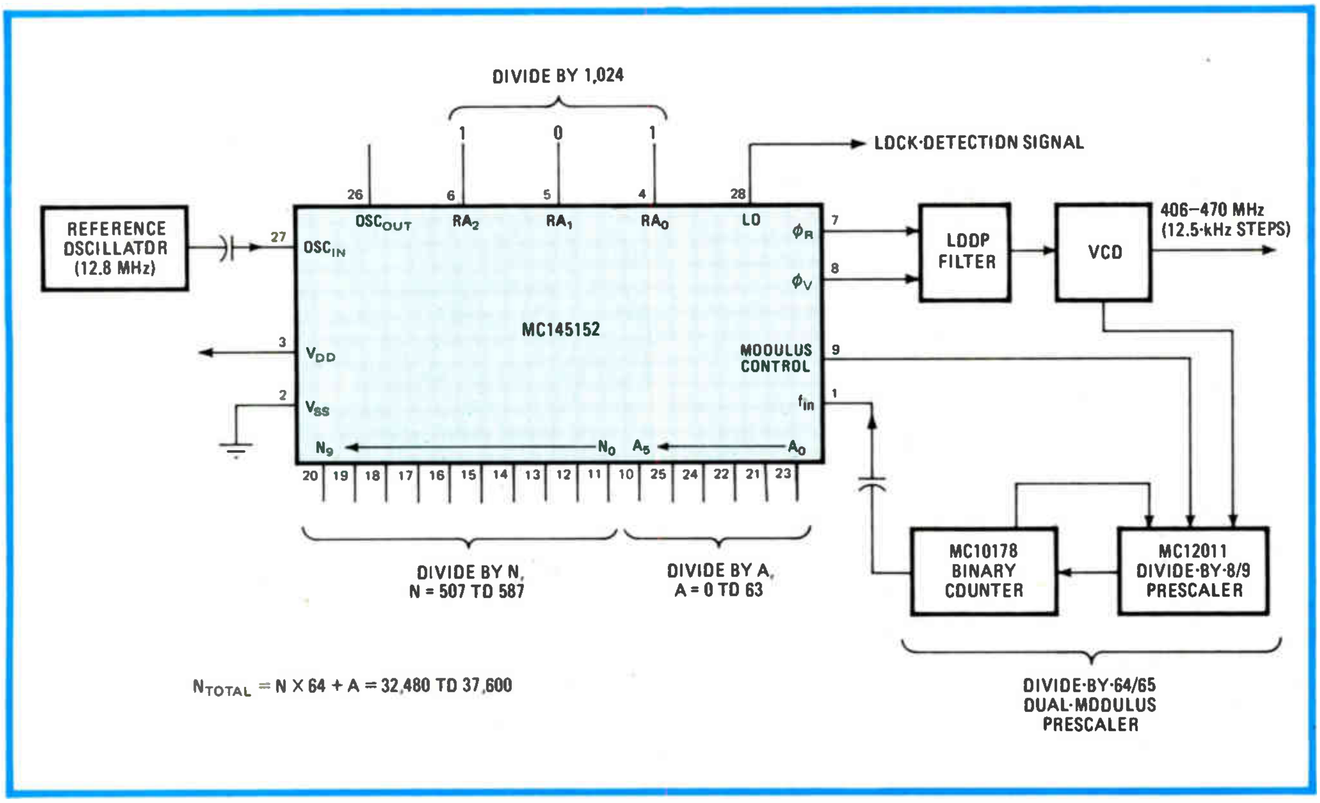
### A fully parallel input

For parallel devices 145151 and -52, all counter programming points are brought out to the package pins. Programming is accomplished by taking the appropriate pins high or low. There are 14 programming lines for the MC145151 (14-bit divide-by-N counter) and 16 for the -52 (10-bit divide-by-N and 6-bit divide-by-A counters). In applications in which lines will not be changed, they can be hardwired to the appropriate level. Built in pull-up resistors are provided on all the programming inputs.

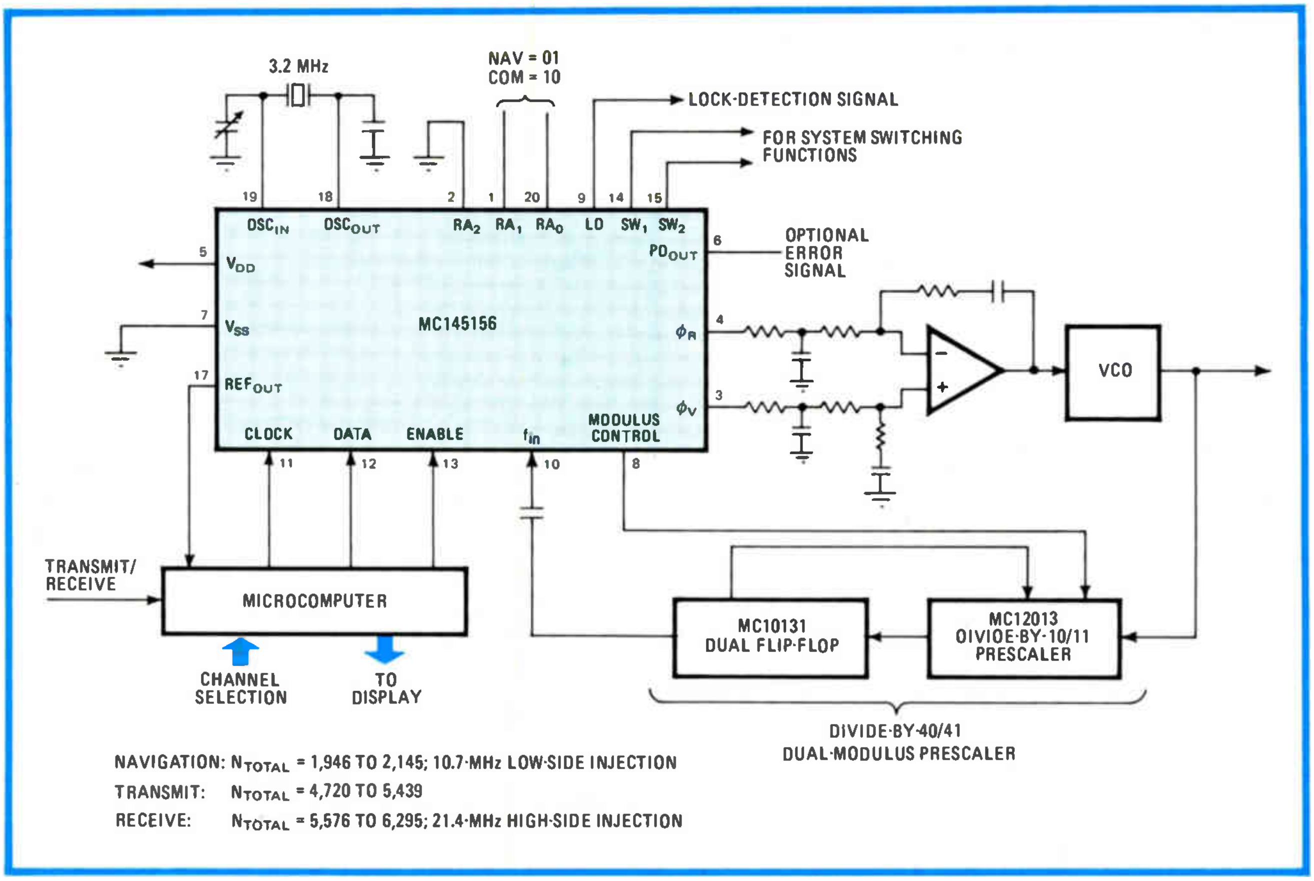
Finally, for the 145145 and -46, which use 4-bit data buses, programming is done using eight interface lines—four for the data word, three for the address that directs data to one of eight latches (seven for the -45), and one for an enable/chip-select function. Although eight lines are involved, only the chip-select line, ST, must be dedicated to the synthesizer chip. The remaining seven can share the bus with other system functions, since they assume an inactive, high-impedance state when ST is held low. They need to be activated only when programming changes are made.

Three data words program the reference divider. Five data words are used to program the divide-by-N and divide-by-A counters in the 145146, and four words program the divide-by-N counter in the -45. The addressable on-chip latches store the information between program changes.

The 145100 chips can be used in a variety of synthe-




**4. Uhf.** Good tuning ability is easily implemented at ultrahigh frequencies. With the reference-divider code inputs $RA_0$, $RA_1$, and $RA_2$ set as shown, the reference oscillator division value is 1,024. Frequency can be stepped in 12.5-kHz increments for the 12.8-MHz oscillator shown.




**5. Multifunction.** Both navigation and communication functions are incorporated in a single synthesizer. Different tuning increments are programmed into the reference frequency divider and a microcomputer serially programs the division values of the counters.

sizer designs. Figures 4 and 5 show samples of some possible implementations. Any of the three programming methods discussed can usually be chosen without major concept changes.

## Applications

Figure 4 illustrates an approach for a high-frequency synthesizer employing dual-modulus prescaling intended for an ultrahigh-frequency mobile radio. As with all PLL frequency synthesizers, a comparison, or reference, frequency is compared in phase with the output of a voltage-controlled oscillator, and any difference generates a corrective signal that is fed to the VCO.

The countdown circuits discussed earlier allow the output frequency of the VCO to be many multiples of the comparison frequency. The exact multiple equals the effective division value of the countdown circuits between the phase detector and the VCO. Thus, changing the division value changes the output frequency, making the circuit tunable in discrete increments. Using the dual-modulus prescaling technique as shown in Fig. 4, the VCO tuning-increment resolution is equal to the comparison frequency, $f_R$, fed into the phase detector—in this example, 12.5 kHz.

Dual-modulus prescaling ICs with a maximum-frequency specification in excess of 500 MHz over the temperature range of −55° to +125°C are available. These devices may be used individually or combined with an additional divider to increase the prescaling divide factor and thus lower the input frequency, $f_{in}$, to a value within the specifications of the LSI device. The MC10178 and MC10131 emitter-coupled-logic ICs in Figs. 4 and 5 perform this function.

For the navigation or communication synthesizer in Fig. 5, it is also possible to use a TTL device for the dual–flip-flop function in the prescaler. To facilitate this, an on-chip ECL-to-TTL translator is available in some dual-modulus prescaler ICs such as the MC12009, -11, and -13. In the circuit shown, the VCO's output ranges from 97.300 to 107.250 MHz in 50-kHz steps; for communications transmission, it is 118.000 to 135.975 MHz in 25-kHz steps; and for reception, it is 139.400 to 157.375 MHz, also in 25-kHz steps.

The 145145 and −46 synthesizer chips provide the user with the access to fully program the 12-bit reference divider for values from 3 to 4,096. This feature can be used to obtain divide-by-R values not available with other family members. Selecting a divide-by-R value allows the frequency of the reference oscillator to be chosen to serve multiple functions, such as the injection signal for a receiver's second mixer stage.

Another feature of these two chips is that they require only one dedicated program line. This is because four data lines and three address lines can share the data-bus system with other ICs. This sharing makes multiloop synthesizer designs more practical. Three or even more loops may be controlled without undue complexity at the programming interface. □

# Integration is on the way for fiber-optic receivers

The slow takeover from hybrid designs will occur first in low–data-rate systems

by Harvey J. Hindin, *Communications & Microwave Editor*

☐ Fiber-optic communications systems have won acceptance as a practical technology, but before they make it big in the marketplace, costs must drop. In particular, systems designers are looking for the makers of optical receiver parts to move beyond the present hybrid designs to monolithic implementations.

Such efforts are already under way, with some products offering varying degrees of integration available for systems with low data rates. Since fiber-optic technology has spread around the world, these efforts are taking place in many countries. Within five years, say industry participants, many receiver components will be implemented monolithically: integrated transmitters will lag because of the difficulties in producing laser or light-emitting diodes in this way.

With the first generation of integrated receiver components available or in the design stages, designers and users of both digital and analog optical communications systems can foresee industry trends for low–data-rate systems by looking at the state of design around the world. Some attention to hybrid designs of receivers is also valuable, for these receivers are likely to predominate for some time in high–data-rate systems where maximum performance is a must.

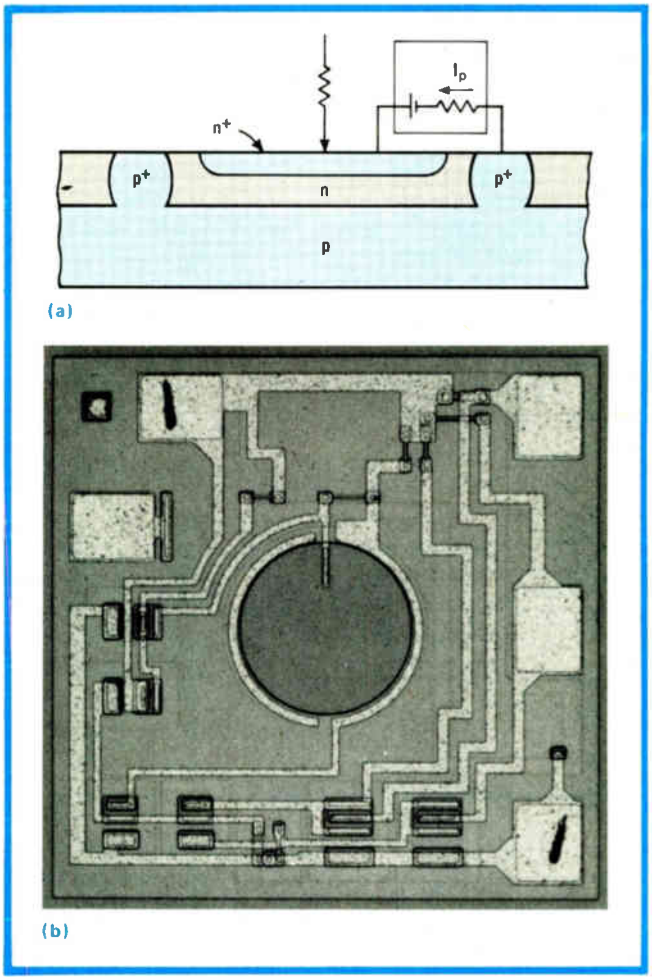
## No one path

However, discerning trends is complicated by the fact that there is no one path to receiver integration. Just what can be achieved is a complex interaction between the intended system's data rate or bandwidth, digital bit-error rate or analog signal-to-noise ratio, modulation scheme, and other electrical parameters. Thus what may work in one application may fail in another.

Furthermore, state-of-the-art technology problems are only part of the story. Engineers may merrily combine more and more circuits on an integrated circuit, but just how far they may go can depend on competitiveness with the cost and electrical performance of the hybrid approach to receiver design.

For the engineer wanting some form of integrated optical receiver, there are but a few choices today. Motorola leads the field, with Spectronics and TRW/Optron right in behind. Other efforts in the U.S., in Europe, and in Japan are still in the early stages but they do indicate the direction the technology is taking.

Perhaps the most sophisticated integrated receiver available comes from Motorola Inc.'s Semiconductor Group, which offers several types of p-n detectors integrated with preamplifiers (Fig. 1). One has a 35-megahertz bandwidth and a 5-millivolt-per-microwatt sensitivity; another has a 10-MHz bandwidth and a 25-mV/$\mu$W sensitivity, says Patrick O'Neil, a principal engineer at the Phoenix, Ariz., group, which has other




**1. Special detector.** In the MFOD403F Motorola monolithic fiber optic receiver, a 10-mil-diameter collector-substrate diode (a) performs the functions of a p-i-n diode. Complete receiver chip (B) contains diode detector (circle) and preamplifier, minimizing noise.

## Optical receivers: light from within

The receiver is the key element in the design of a fiber-optic system, as important in long-distance communication as in busing data over short distances, and at low as well as high data rates. It detects the incident light and converts it into an electrical signal containing the information impressed at the transmitting end of the system.

The design goal is to minimize the amount of optical power that must reach the receiver in order to achieve a predetermined bit-error rate for digital systems or signal-to-noise ratio for analog systems. The minimization is necessary since neither transmitter power nor low-attenuation glass fiber comes cheap.

This minimum power level, the receiver sensitivity, is a complex function of the parameters of the design. There are other design considerations, and practical receivers have less than optimum sensitivity. For example, sensitivity may be traded off with receiver dynamic range, a measure of just how much the receiver input signal may vary and still provide usable outputs.

**Essential components.** As the figure shows, an optical receiver consists of a photodetector that acts as an optical-to-electrical converter, a low-noise preamplifier and post amplifier that convert the detector's weak signal into a usable level, and filtering to remove extraneous signals and noise. The design may be adapted to either digital or analog signals by adding such specialized circuits as decision logic to the digital device and demodulation to the analog.

The photodetector and preamplifier incorporate semiconductors and present problems for the designer who wishes to integrate them into one or two chips. Still, this front end is receiving most of the attention in the drive to integrate. The postamplifier can follow, and in any case, it does little to influence receiver sensitivity since it operates at an already high signal level. Next will come the filters, but as passive devices, they present few problems.

The photodetector may be either a p-i-n or an avalanche diode, although in present first-generation designs, it is more likely a p-n diode. Also, research is under way on other structures like field-effect phototransistors. Today, the diode is made from silicon, which provides a spectral match for the 0.8-to-0.9-micrometer wavelengths emitted from the aluminum-gallium-arsenide transmitters that are commonly used in fiber-optic systems.

However, other options are being studied, notably GaAs FETs that have better noise performance than their silicon equivalents, but introduce a second substrate into a silicon world. It is likely that future receivers will take advantage of the lower fiber attenuation in the 1.3-to-1.6-$\mu$m region of the spectrum and be made from materials absorbing in this spectral region, which include several GaAs compounds.

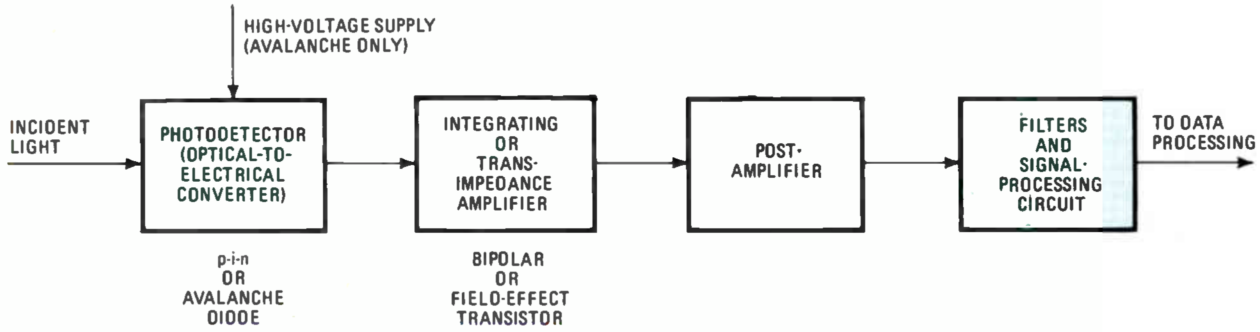
**Choice.** For now the choice is between a p-n or p-i-n diode or an avalanche device. For its part, the p-n or p-i-n diode merely converts the optical into an electrical signal. In contrast, an avalanche device adds internal current gain but requires applying several hundred volts to make it function. Such voltages are undesirable if the goal is to integrate the avalanche detector on a substrate with other important devices.

The current generated by the photodetector must be converted into a usable signal level for further signal processing by the receiver. It is critical that the preamplifier do this with a minimum amount of noise added to the system—since the lower the noise, the more sensitive the receiver. So the first stage of the amplification is performed by either a FET or a bipolar transistor. As is the case with the photodetector, the choice depends on the application at hand. In digital systems, for example, high data rates favor a bipolar device since its noise performance is better.

Whether a FET or bipolar device is used, there are two choices for the preamplifier configuration: either the high impedance (integrating) version that is a current amplifier or a transimpedance amplifier that is a current-to-voltage converter. Either type, with its associated circuitry, may be integrated onto a silicon substrate.

The integrating amplifier reduces all sources of noise to an absolute minimum. However, each receiver has to be tuned and temperature-compensated individually, making integration difficult. In addition, the dynamic range of such a design is limited. However, where the ultimate in sensitivity is required, this amplifier is the preferred approach.

The transimpedance amplifier is the most common design for either the hybrid or the monolithic approach. It can provide wide bandwidths and a greater dynamic range than the integrating amplifier approach, though its noise performance is somewhat inferior.




versions with still different specification tradeoffs.

System design is eased by an input fiber strand fed through a specially designed connector and leading to the light-sensitive area of the IC. The connector is a joint development of Motorola and Amp Inc.

The most common approach to a fiber-optic receiver is the combination of a p-i-n photodetector diode or variant like a pn detector and a transimpedance preamplifier (see "Optical receivers: light from within," p. 156). Such a design is relatively easy to implement and can be made with specifications almost as good as the more exotic alternative devices: avalanche detectors and integrating preamplifiers.

In the Motorola design, an emitter-follower amplifier is included with the transimpedance preamp so that the receiver's output voltage is available from a low-impedance source. Thus the receiver can easily match and drive other signal-processing circuitry. What's more, this approach yields an output voltage directly proportional to the incoming light power over a wide range of input levels—the already mentioned sensitivity measured in millivolts per microwatt.

**Benefits anticipated**

Most engineers in the fiber-optic receiver industry believe that the integrated detector-amplifier will cost much less in large quantities than the hybrid components. However, it is too early in the game to make exact comparisons. Costs for both types are strongly dependent on specifications and quantities, and experience in producing large numbers of these parts is lacking.

However, the systems designer will find his or her task simplified by the integrated offerings. For one, the design of a transimpedance amplifier is a tough nut to crack, but it need not worry the user of an integrated detector-amplifier. For another, this integrated receiver front end comes enclosed in a shielded container, eliminating difficult-to-do and expensive shielding of printed-circuit boards.

Another design problem that the integrated front end can solve is electromagnetic and radio-frequency interference. The key here is a short lead length—the Motorola design has an equivalent detector lead length of only about 0.25 millimeter in the connections on the IC.

Both emi and rfi are problems for p-i-n diode receivers because they have high impedance. The shortest of leads will act as a pickup antenna, and the energy coupled into the receiver is amplified by the high-gain transimpedance preamp. Thus the shortest possible lead lengths are highly desirable in the fiber-optic receiver.

Such noise problems in the receiver are particularly frustrating to the system designer, who may be attracted to an optical transmission scheme because the dielectric fiber is totally free from emi or rfi pickup (unlike metal cable or wire). Worse yet, the interference tends to be random, so the only compensation is increasing the signal or transmitted power to maintain a satisfactory bit-error rate or signal-to-noise ratio.

**The U. S. effort**

After Motorola, the two manufacturers furthest along the integrated path are TRW/Optron, one of TRW Inc.'s Electronic Components divisions, and the Spectronics Inc. subsidiary of Honeywell Inc. Both manufacturers have already made their moves toward establishing an industry position.

The basic strategy at Optron in Carrollton, Texas, is a step-by-step integration of the signal-processing elements in the preamp stage, varying the elements integrated with the diode detector to determine the mix customers need. The company expects that the first true monolithic receiver will combine the detector with two or three of the amplifier's building blocks, such as threshold detectors, comparators, linear amplifiers, automatic gain control, and phase-locked loops.

**2. Lots of modules.** TRW/Optron is preparing for the advent of monolithic fiber-optic receivers by developing a line of integrated devices. Here engineers Ben Wagner and Joel Van Antwerp check photo mask artwork for accuracy on a light table.

"By 1983 or 1984 the technology will be available for production of a very large-scale integrated fiber-optic receiver, but it will take until 1985 for these to become commodities," says Michael F. Ehman, vice president of materials technology and development. "Probably three of the modules [the building blocks] will be integrated with the detector. If you go much beyond three, the circuit is going to be too complex for the business/computer systems market. The dice would be too big and the yield would be reduced to a point where nobody could afford them."

**A beginning**

Optron introduced an IC family this year (Fig. 2) that features a threshold detector on a chip with a photodiode. But it is used for optical switching applications, not in fiber-optic receivers yet. The company plans to integrate other amplifier modules with a detector, eventually including several of the modules in a package designed specifically for fiber-optic receivers. Ehman expects the package's detector will be a p-i-n device (see "No rush to integrate an avalanche photodiode," p. 158) for low-performance systems in the industrial-control, office-of-the-future, and automotive markets.

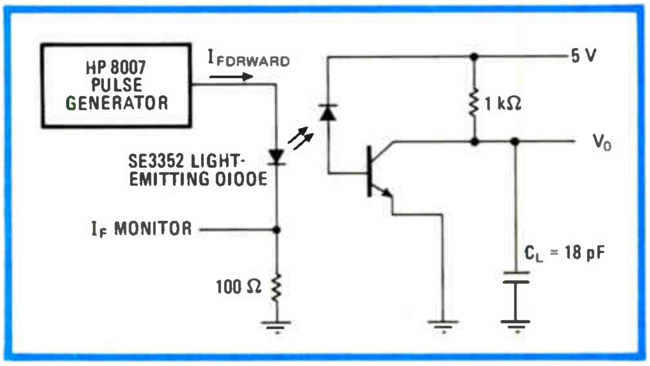
Such low-performance systems are the only area where integration of the receiver will take place quickly, says J. R. ("Bob") Biard, chief scientist of Spectronics in Richardson, Texas. For systems needing 5-MHz speed or more, the basic incompatibility between high-speed

## No rush to integrate an avalanche diode

Avalanche photodetectors, superior to p-i-n diodes in several respects, are being ignored in the race to integrate the fiber-optic receiver. The industry view is that, for the foreseeable future, they will not be seen on chip with other circuitry.

"The complexity of the avalanche photodiode process is so far away from the integrated-circuit processes of today that the two don't appear to be really compatible," says Michael F. Ehman of TRW/Optron. "The materials processes needed to fabricate avalanche devices and integrated circuits are going in opposite directions. Avalanche photodetectors tend to be high-sheet-resistance devices, while low sheet resistance is needed for integrated circuits."

Texas Instruments' Shaun Shaunfield says flatly that "avalanche and IC technology just don't mix." Furthermore, the high voltage needed to make the avalanche function is an insurmountable stumbling block for Spectronics, whose Bob Biard sees no hope of integrating it into an IC. Add to this the device's problem with voltage control and temperature compensation (since the avalanche gain varies strongly with voltage and temperature), and it appears that the fiber-optic receiver designer can forget about it for now in integrated designs.




**3. Check it out.** The Spectronics fiber-optic photodiode with integrated preamplifier is checked for both optical and electrical parameters. Data obtained depends on such fiber parameters as cable diameter and numerical aperture, as well as the diode characteristics.

detector and IC processes is going to require hybrid implementation "for a long time to come," he says.

Like Motorola, Spectronics actually is producing integrated detector and amplifier products. One part, the SD3323 (Fig. 3), incorporates a photodiode with a transistor as a first-stage amplifier. It comes in a metal or plastic can and can be used to directly drive a TTL output if a short fiber line and a large-diameter cable are used.

The SD3323 sells in the $10 range for the metal-can version. "Due to compromises in detector performance that had to be made in relation to the IC technology needed to put everything on the chip, the bandwidth is specified at 2 MHz," says William F. Stephen, the company's product manager. "This is significantly lower than our discrete devices."

Spectronics also offers what it calls a fiber-optic Schmitt-trigger detector. This chip integrates a photodiode, a preamplifier, and a Schmitt threshold and output compatible with TTL or complementary-MOS logic. The IC is made with what Biard calls a linear complementary bipolar process and is available in a plastic can or a metal can suitable for direct coupling to a fiber. The low speed of 200 kilohertz is a tradeoff for a better response than in the 2-MHz SD3323.

As in the Motorola offerings, the integrated Spectronics designs do not use a p-i-n device for the detector diode. In the case of the 3324 Schmitt trigger, the detector is formed at the junction between the epitaxial layer and the substrate.

"For the IC epilayer technology, the substrate is fairly high resistivity p-type material," Biard says. "You grow on it the epilayer that forms the collector of all the transistors on the circuit. That epilayer is the cathode of the photodiode and the substrate is the anode. So it really is just an n- or p-type diode. This has to be done because there just isn't any way to make a true p-i-n diode compatible with silicon IC technology."

This procedure makes the receiver slow to respond and only suitable for low data rates. "Since it is a p-n diode it has a fairly small depletion-layer width at the bias voltage that is available for it on the chip," Biard says. "So a lot of the response of the photodiode is from undepleted material. Those carriers have to diffuse to the junction before current flows in the external circuit, and that makes the detector slow."

The inherent bipolar collector's substrate junction is used as the photodetector in the Motorola devices, points out semiconductor industry consultant Lawrence A. Murray of Murray Consultants, St. Louis, Mo. "This is neither a low-capacitance approach nor highly efficient insofar as conversion efficiency is concerned, but meets the needs of low–data-rate baseband or computer links," he says.

Spectronics says the demand for these low-end integrated receivers is very strong for process-control and instrumentation applications. It adds that 50,000-unit production projections bring integrated devices to half the price of the discretes.

### A dissenting view

Not all U. S. makers of optical receiver components embrace integration enthusiastically. "While there is a trend toward integrating signal-processing circuitry with the detector in a fiber-optic receiver, there is no particular urgency," says W. N. ("Shaun") Shaunfield, manager of electro-optical components at Texas Instrument's Optoelectronics department in Dallas.

"TI has no specific program under way right now to integrate detectors on chip with circuitry elements," he says. Cost is a major factor, he adds. "Since detectors are likely to take up large portions of a chip, it's not economical to use valuable wafer real estate that could be used for more complex functions. It would probably be cheaper to process the simple two-to-three-mask detectors separately and go the hybrid route."

The fundamental physics is a problem too, Shaunfield says. He notes that integrated p-i-n diodes do not collect all the light incident on them, because their active regions are on the surface half mil or so and the incident light goes down several mils. The resulting efficiency problems might degrade responsivity as a function of wavelength by a factor of four or five.

Still, Shaunfield admits the integrated receiver will come along—especially for short fiber runs where lower performance is more acceptable. But five years from now such parts will be hard-pressed to capture as much as 30% of the market and will probably have to settle for something like 15% or 20%, he says.

**Overseas action**

With lead lengths causing grief over noise, it is no surprise that, as the receiver community investigates pure monolithic designs, it is attacking the lead-length problem with other clever approaches. Typical is the Hitachi Ltd. design consisting of a discrete p-i-n photodiode and a two-transistor integrated monolithic transimpedance amplifier (see Fig. 4). It can provide a 30-MHz bandwidth with a sensitivity of −35 dBm at the commonly used 0.83-micrometer wavelength.

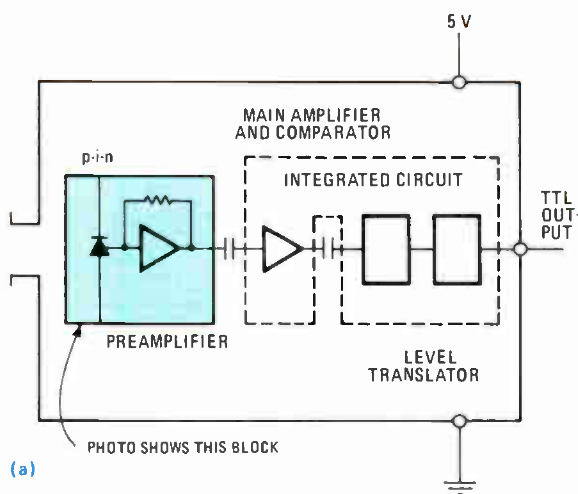
The lead length is only 2 mm, so noise is no problem as long as the metal can is used. "The design might prove usable up to a bandwidth of several hundreds of megahertz," says its designer, Mitsuo Tanaka, senior researcher at Hitachi's central research laboratory in Tokyo. It has already been employed in a 4.2-kilometer, 10-megabit-per-second data highway that carries signals controlling a continuous casting steel mill, he says.

Not to be outdone, another Japanese group has built an IC with six p-i-n diodes as part of its effort to construct a compact receiver. The Yokoshuka Electrical Communications Laboratory of the Nippon Telegraph and Telephone Public Corp. built the array to match an experimental six-conductor fiber cable. Researchers there say that the lead lengths are such that there are no special problems with reduced frequency response or noise. Their experiments have been carried out at the 6.3-Mb/s rate used in Japan for transmission and at the 8.2-Mb/s rate used between telephone exchanges.

In another experiment the Yokoshuka group built a receiver front end with a silicon field-effect transistor mated to a p-i-n detector. The 6.3-Mb/s part has a 25-dB dynamic range and a sensitivity of −46.7 dBm. A gallium-arsenide FET would be more attractive for the amplifier's first stage because of its low noise—but its incompatibility with silicon causes integration problems.

However, GaAs fiber-optic receiver work is going on all over the world. For example, the Thomson-CSF Corbeville Laboratories near Paris have developed a fiber-optic transceiver dubbed EROS for emitter-receiver optical system (see "A timely conference for receiver fans," p. 160). A discrete GaAs diode functions both as a receiver and transmitter in a half-duplex scheme. The lab is far from having any prototypes of integrated fiber-optic receivers, a spokesman says.

The French are, however, busy in fiber-optic receiver integration, as they see its potential for more efficient, less expensive, and noise-free systems. At the Thomson-CSF Lignes Télégraphiques et Téléphoniques subsidiary in Paris, a group headed by Michael Eve has started to investigate the integration of a p-i-n detector with a FET amplifier, both being GaAs devices. So far "the problem is getting the device capacitance low enough for suitable amplification," Eve says. It will be as much as two years before anything is ready to market, he adds.





**4. Two in one.** In one Hitachi experimental fiber-optic receiver, a discrete p-i-n diode is mounted alongside a two-transistor monolithic transimpedance amplifier (a). Both are enclosed in a metal case (b), so that electrical noise is not a problem.

Even further away from a product is the effort at Compagnie Générale d'Electricité. The word from its central research laboratory in Marcoussis near Paris is that engineers are starting to look into an all-silicon photodetector and amplifier combination, but they will have nothing to report until 1981.

Meanwhile, West Germany's Siemens AG has been busily developing integrated photodetector amplifiers at its Munich operation, but it has not devoted much effort to the fiber-optic integrated receiver. Instead, the company has chosen to go after the now more lucrative market for camera exposure meters, electronic flashes, and the like. Its TFA 1001 W is typical: an IC with

## A timely conference for receiver fans

Designers and users of fiber-optic receivers, whether integrated or in hybrid form, will find much to ponder in presentations recently at the FOC-80 fiber optics and communications conference in San Francisco. The conference offered three papers directly concerned with receivers and others that touched on the subject.

The French EROS hybrid transceiver was discussed by its authors L. d'Auria and P. Richin of Thomson-CSF. They emphasized a description of the discrete module system. National Semiconductor Corp. sent Eric M. Miller to tell the audience he designed a hybrid fiber-optic receiver for medium performance because such general-purpose units have been ignored in the past.

For its part, Motorola's Semiconductor Group presented two papers on the system use of its integrated fiber-optic receivers. Also, Lawrence A. Murray of Murray Consultants presented his prediction of the evolution of the fiber-optic receiver business.

photodiode and an amplifier. The technology has enough in common with the requirements for integrated optical receivers so that Siemens will probably introduce a line of monolithic receiver products when the time is ripe.

In England, development of integrated fiber-optic receivers is also in the beginning stages. Researchers are devoting their efforts to optimizing hybrid designs with the experience gained being transferable to integrated designs. Typical is a hybrid p-i-n photodiode plus gallium-indium-arsenide FET receiver operating at the high data rate of 140 Mb/s [*Electronics*, Sept. 25, 1980, p. 73].

The p-i-n diodes were fabricated at Plessey Co.'s Allen Clark Research Center in Caswell. The system itself was put together by the Post Office research center in Martlesham Heath and has sensitivities at the 1.3-$\mu$m wavelength of $-44.2$ and $-40.1$ dBm for 140- and 280-Mb/s data rates respectively. A system bit-error rate of $10^{-9}$ is maintained. Such second generation fiber-optic systems are important because they exploit the lower fiber attenuations available at the 1.3-to-1.6-$\mu$m wavelengths. Thus longer fiber runs between repeaters are possible.

### Still life in hybrids

The pace of worldwide development is such that it will be three to five years before the integrated approach takes over from the hybrid receiver designs running the show now. As well as fundamental technical reasons, the size of the markets the receivers serve and their cost are factors.

The important technical factor is that "you can't do monolithic photodetectors right now for the high bandwidths," says David B. Medved, president of Meret Inc., a Santa Monica, Calif., maker of fiber-optic components and subsystems. He defines this as 30 MHz and up and sees hybrids as the answer for the next two or three years, at least. "Nobody has found a way to put a high-speed p-i-n photodiode onto low-resistivity silicon," he explains.

Dennis Haynes, marketing manager for analog products of Burr-Brown Research Corp. in Tucson, Ariz., agrees that the detector-amplifier integration is the hard part. "What has held back the development of integrated fiber-optic receivers is disappointment by manufacturers with the slowness of the fiber-optic market to become important," he adds. Only as the market matures will research and development into integration pick up its pace, he believes.

Burr-Brown, Meret, Spectronics, and other manufacturers have lines of hybrid receiver components available. They cost $100 or more, depending on specifications and quantities. These prices are high because the sales volumes are not yet enough to attract the mass semiconductor producers, says consultant Lawrence Murray, although he expects a change in the next few years [*Electronics*, July 17, 1980, p. 44].

Furthermore, "a push toward integrated fiber-optic receivers will require expertise that the small suppliers of hybrid devices just don't have," he says. Only a few of the six dozen suppliers of optical receiver parts could do an integrated receiver he says, mentioning TI, RCA, Hewlett-Packard, Hughes, Motorola, Spectronics, and Optron. However, only the last three companies will admit to ongoing R&D programs in integrated optical receivers.

### Costs may tumble

Murray points out that a standard discrete p-i-n silicon diode is made with three masks on a 50-by-50-mil substrate and may sell for $7. "This is twice the selling price of a 200-by-200-mil chip with thousands of transistors, so there is certainly room for prices to fall, especially when you consider that the larger device has much tighter tolerances."

That inexpensive integrated fiber-optics receivers will first make their mark in low–data-rate systems is clearly the industry viewpoint. For example, Eric N. Randall, vice president of engineering and director of optical communications products for Galite Inc., a Wallingford, Conn., division of Galileo Electro-Optics Corp., says that he suspects that integrated devices will be especially well suited to the sort of short links that exist in minicomputer setups or between computers and peripherals where maximum bandwidth is not a problem. In fact, "widespread availability of monolithic detectors with an amplifier stage would make the short link market even more active than it is now."

While agreeing with Randall's assessment, Stephen C. Lang, senior marketing specialist at systems maker Valtec Inc. in West Boylston, Mass., says the key question is not price but reliability. He says that Valtec's discrete optical modulator-demodulators have mean times between failures in the field of more than 100,000 hours and "we wouldn't consider retreating from that to save a few dollars." □

*Inputs to this article came from* Electronics *staff members Arthur Erikson, James B. Brinton, Charles Cohen, John Gosch, Wesley R. Iversen, Kevin Smith, and Larry Waller.*

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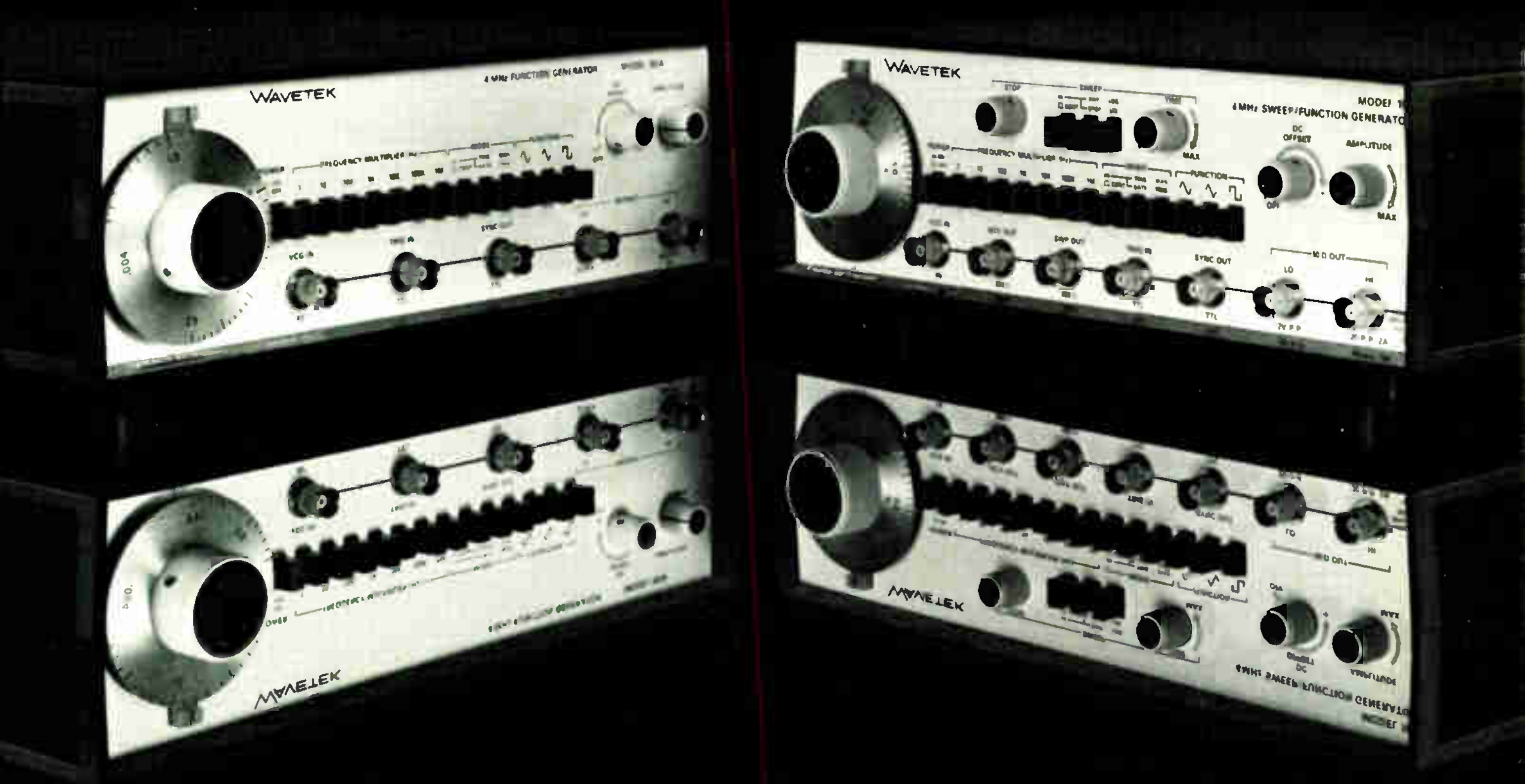


# Opto-isolated line monitor provides fail-safe control

by Eric G. Breeze and Earl V. Cole
*General Instrument Corp., Optoelectronics Division, Palo Alto, Calif.*

Because of the degree of isolation they provide, optically coupled ac-line monitors serve well as a small, reliable low-power interface in ac-to-dc control applications, where status information of the ac line is crucial. When a type is used that is TTL- and microprocessor-compatible—like the MID400, which performs the basic monitoring function on a single chip—a circuit can be built that ensures fail-safe control under the most difficult monitoring assignments. And when combined with a 555 timer, the monitor will have improved drive capability, more precise control of the turn-on and turn-off delay times, and better noise immunity than units that are typically available.

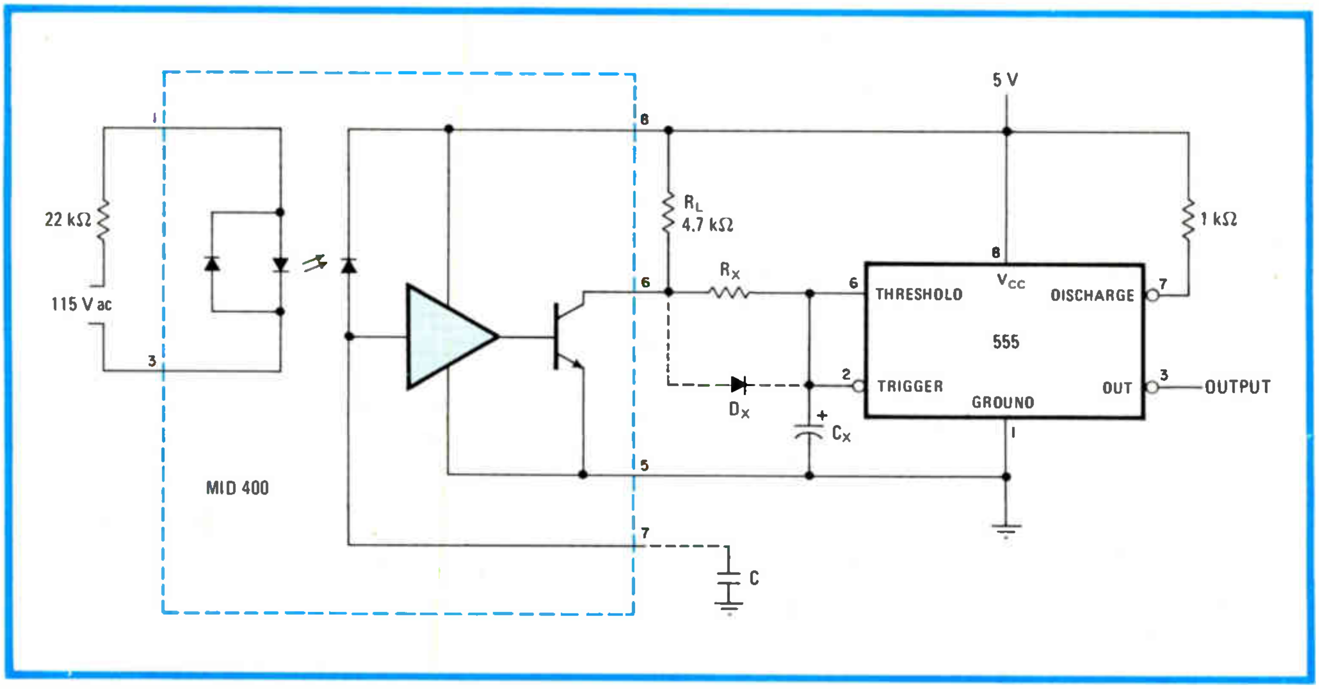
As shown in Fig. 1, two gallium arsenide infrared-light-emitting diodes connected back to back and optically coupled to an integrated photodiode and high-gain amplifier make up the MID400, which is encased in an eight-pin dual in-line package. In operation, each LED conducts on alternate half cycles of the ac-input waveform, together producing 120 pulses of light per second. Thus the photodiode periodically conducts, causing the amplifier to drive the npn transistor at the output to its on state. As the amplifier's switching time has been designed to be slow, it will not respond to an absence of input voltage lasting a few milliseconds; therefore it will not respond to the short zero-crossing period that occurs each half cycle.

The MID400 operates in one of two basic modes: saturated or unsaturated. It operates in the saturated mode when the input signal is above the minimum required current of 4 milliamperes root mean square and the photodiode pulses keep the output of the MID400 low. It operates in the unsaturated mode if the input current drops below 4 mA rms. Under these conditions, a train of pulses will appear at the output. In this way, a clean clock generator, devoid of power-line transients because it is isolated, may be realized.

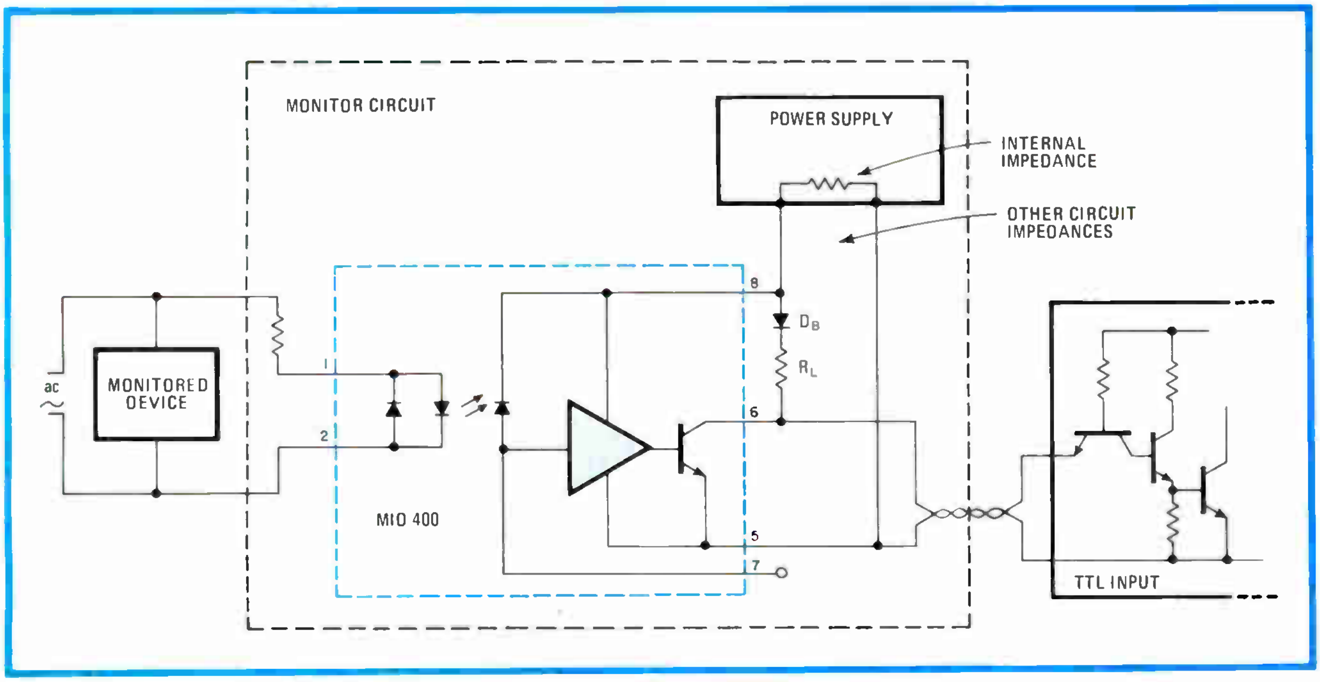
If the input current drops below 0.15 mA, the device turns off. This causes the output of the MID400 to remain high.

Adding an external capacitor, C, to pin 7 of the device produces a time-delay circuit. The amount of delay on power-up is short because the photodiode has a low impedance when conducting. When ac is removed, however, the delay is long because the capacitor must discharge through the leakage resistance of the amplifier and photodiode. The larger the capacitor, the longer the delay.

In lieu of capacitor C, the use of a 555 timer also provides pulse shaping by yielding faster rise and fall times at the output. Here, the 555 is used as a Schmitt trigger with well-defined thresholds, the high state being ⅔ $V_{cc}$ and the low state being ⅓ $V_{cc}$. Besides providing




**1. Control chip.** Opto-isolated power-line monitor on single IC provides hash-free driving signals for ac-to-dc control applications. When united with 555 timer, circuit provides precise control of on and off delay times, improved driving capability, and good noise immunity.




**2. Immune.** Monitor is easily modified for fail-safe control tasks, such as are required in industrial applications. Diode prevents component failures from creating output glitches. MID400's output circuit design inherently prevents generation of glitches caused by supply anomolies.

noise immunity, use of the 555 also minimizes oscillations that might occur if a TTL device were to drive a minicomputer.

Timing elements $R_x$ and $C_x$ set the delay. With appropriate choice of the time constant, the circuit can be made to respond to, or to ignore, one or more ac input cycles. Diode $D_x$ permits the fast charge and slow discharge of $C_x$ or, if the diode's polarity is reversed, the slow charge and fast discharge of the capacitor. The actual delay time will depend on the operating mode of the MID400.

For industrial, military, or medical applications in which fail-safe operation is important, the circuit's response must also be considered for the cases where either the ac input or the MID400 supply is removed. Fortunately, the MID400 has been designed so that its output transistor is on (low) only when both the ac input voltage and the supply voltage are present, thus simplifying the problem of providing a valid fail-safe control signal. Consider the case where the MID400 is powered by a separate 5-volt supply and the monitor drives a TTL-compatible interface through a twisted-pair line (Fig. 2). Normally, the inherent truth table of the device will prevent an erroneous output to the TTL interface circuit. Should $R_L$ fall below 1 kilohm for one reason or another, however, and the power supply be off, the TTL input of the minicomputer will appear low because of excessive current flow through $R_L$. Diode $D_B$ in series with $R_L$ blocks any reverse current, eliminating the problem. □

# Three-level inverter conserves battery power


by Geert J. Naaijer
*Laboratoires d'Electronique et de Physique Appliquée, Limeil-Brévannes, France*


Converting 12 volts dc into a well-regulated 220 V ac at high efficiency is especially desirable when the input power source is derived from solar cells or a car battery. Often, too, output harmonics generated by the conventional square-wave inverter must be reduced to a point where it does not create other practical drawbacks. These design requirements are met with this inverter, which maintains efficiency and reduces harmonics at all power levels by ensuring that the driving current is almost linearly proportional to the output power and by producing a three-level output waveform that more closely approximates a sine wave.

As shown, the CD4013 dual flip-flop generates a 100-hertz pulse train (duty cycle is ⅙) and a 50-Hz square wave (the oscillator is easily modified for 60 Hz), both of which are independent of input voltage and load variations. The AND gates formed by the diode-resistor networks at the output of the flip-flops apply these signals to the power transistor drive circuitry (BC548, MJE801, etc.), which, configured in a two-phase switched-mode arrangement that sends a pulse through the primary of the line transformer every quarter cycle at 50 Hz, generates a three-level waveform.

Because the positive and negative output swings each last one third of a cycle, separated by sixth-period intervals at the zero crossings, third-harmonic attenuation is theoretically reduced to zero. By appropriate modulation

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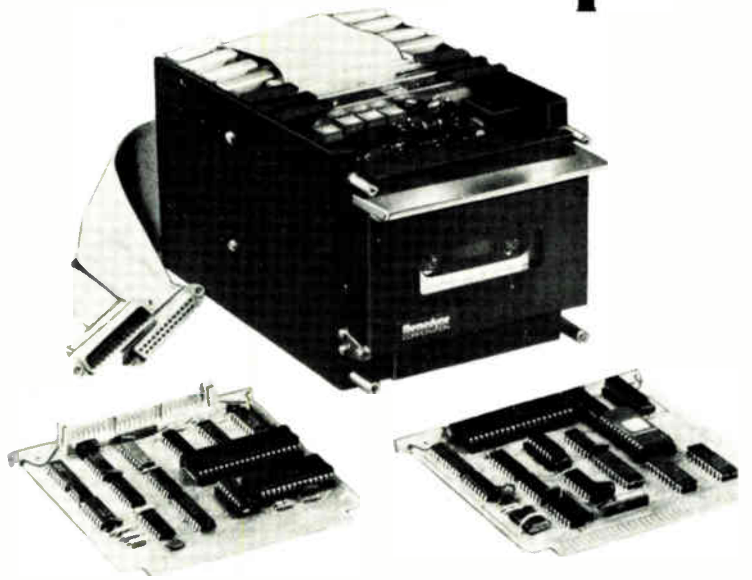

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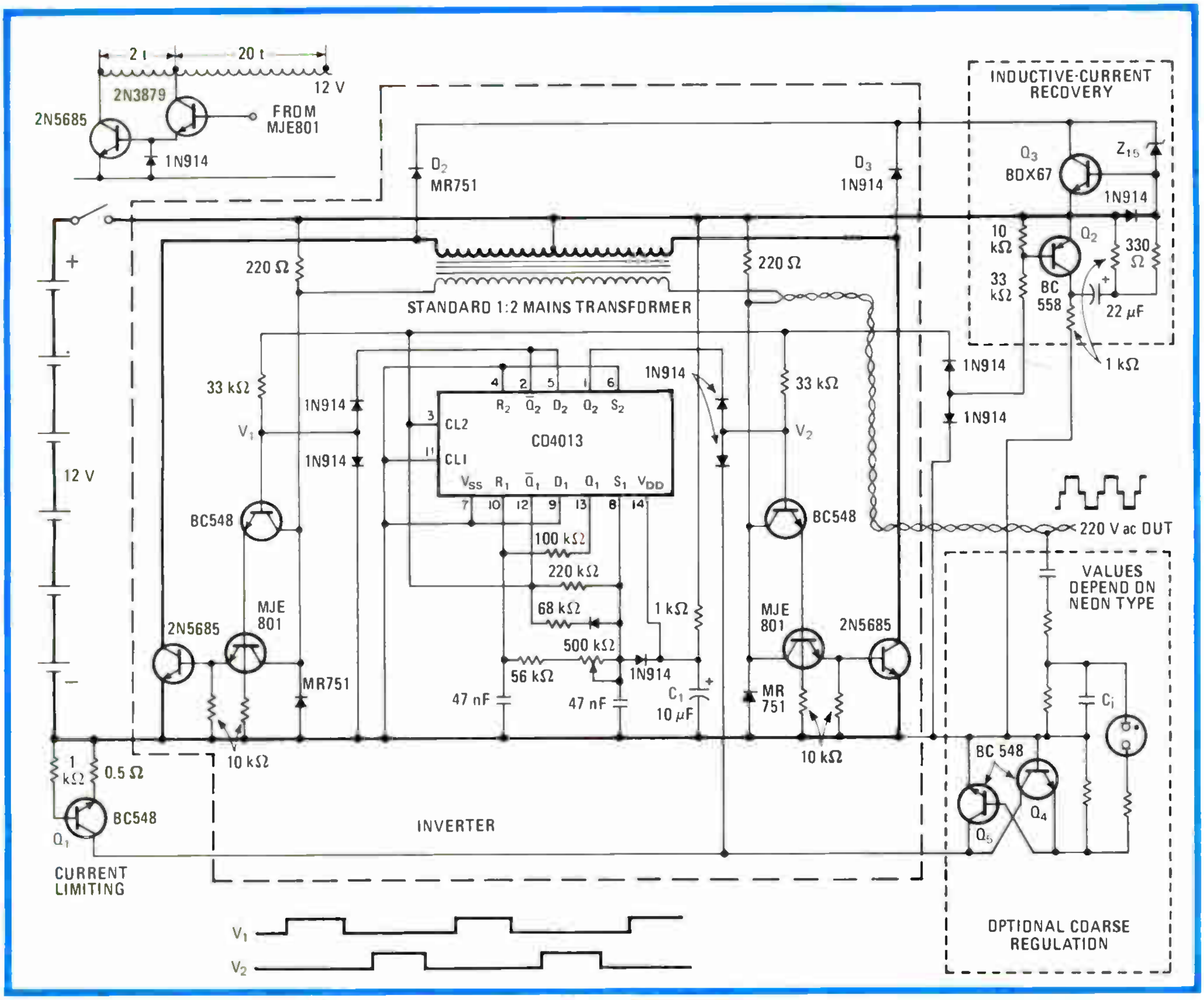


**Cell saver.** Switched-mode inverter attains high efficiency and low harmonic distortion over a wide range of power levels, thus conserving solar cells and batteries. Output frequency is independent of input fluctuations. Current limiting and voltage regulation are provided.

of these zero-voltage intervals, good regulation is achieved at low loss without reintroducing excessive third harmonic energy. Although this method is not as elegant as the transformerless method of summing phase-shifted square waves or stepped sine waves,[1] it is much simpler.

$D_1$ and $C_1$ ensure reliable startup. Current limiting is provided by $Q_1$, which diverts drive current if output current soars. Output impedance is kept virtually constant during all parts of the cycle, including zero-voltage periods, where $Q_2$ saturates $Q_3$, thus feeding an inductive current back into the battery via diodes $D_2$ and $D_3$. The zener diode provides spike suppression. A neon lamp or similar symmetrical-breakdown device allows simple voltage regulation. When $V_{out}$ soars, $C_i$ attains breakdown before the normal zero-voltage period, and $Q_4$ or $Q_5$ diverts current.

Because this is a switched-mode inverter, efficiency is excellent at nominal output power. But, in contrast to other inverters, its high-efficiency characteristic extends down to very low output-power levels. This is achieved by forcing output current to flow not only through the transformer's secondary, but also through the base-emitter junctions of the 2N5685 power transistors. Thus, base drive closely tracks the output power requirements. As long as the transformer winding ratio is compatible with the gain needed to saturate the power transistors, significant power can be saved at the lower power levels. Efficiency exceeds 88% at 120 volt-amperes, 75% at 175 VA, and 50% at 15 VA. No-load loss is only 12 watts.

Still better performance can be obtained by adopting the power Darlington configuration, as shown at the upper left. Using the Darlington, the inverter's efficiency will be 89% at 150 VA, 70% at 225 VA, and 50% at 15 VA. Lower transformer step-up ratios further improve performance, because the output transistors switch more totally into saturation. Thus, 12-V dc-to-110-V ac and 24-V-dc-to-220-V-ac designs are more efficient than this 12-V-dc-to-220-V-ac circuit. □

**References**
1. Geert J. Naaijer, "Transformerless inverter cuts photovoltaic system losses," *Electronics*, Aug. 14, 1980, p. 121

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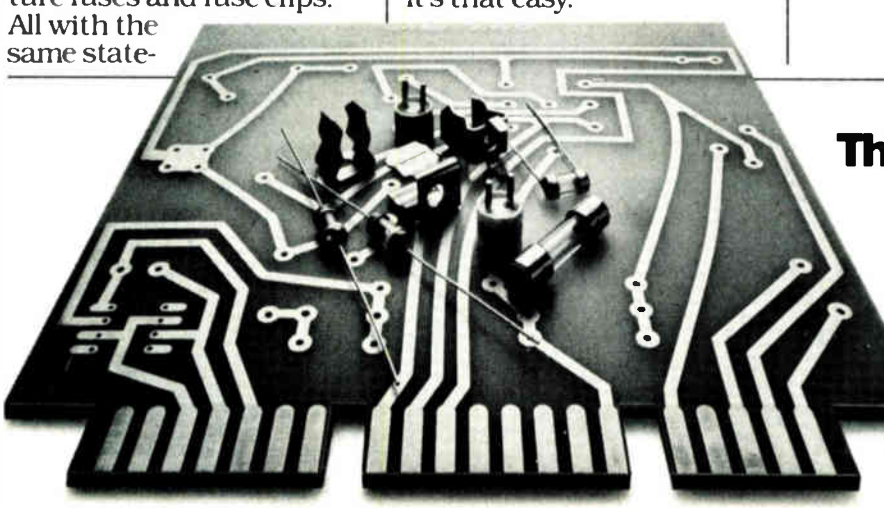

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# High linearity and video speed come together in a-d converters

Digitally corrected subranging in analog-to-digital converters ensures high precision at no loss in speed

by William J. Pratt, *Analog Devices Inc., Computer Labs Division, Greensboro, N. C.*

☐ Conversion speed is obviously paramount for analog-to-digital converters meant to operate in the 1-to-20-megasample/second range. But linearity is also a most important parameter. Unfortunately, a tradeoff must usually be made between top speed and maximum conversion precision in the design of such converters. The result is a less-than-ideal transfer function.

Increasing the resolution of the first encoder in a conventional subranging a-d converter is the basis of a digital error-correction technique, called digitally corrected subranging, that extracts superior performance from 9- to 12-bit a-d converters. As a bonus, this better performance can be achieved with components that are less accurate, smaller, and dissipate less power than those needed in conventional designs, since less attention need be paid to system errors. Examples of a-d converters using the DCS approach include the 10-bit, 20-megahertz MOD-1020 and the 12-bit, 5-MHz MOD-1205, both from the Computer Labs division of Analog Devices Inc.

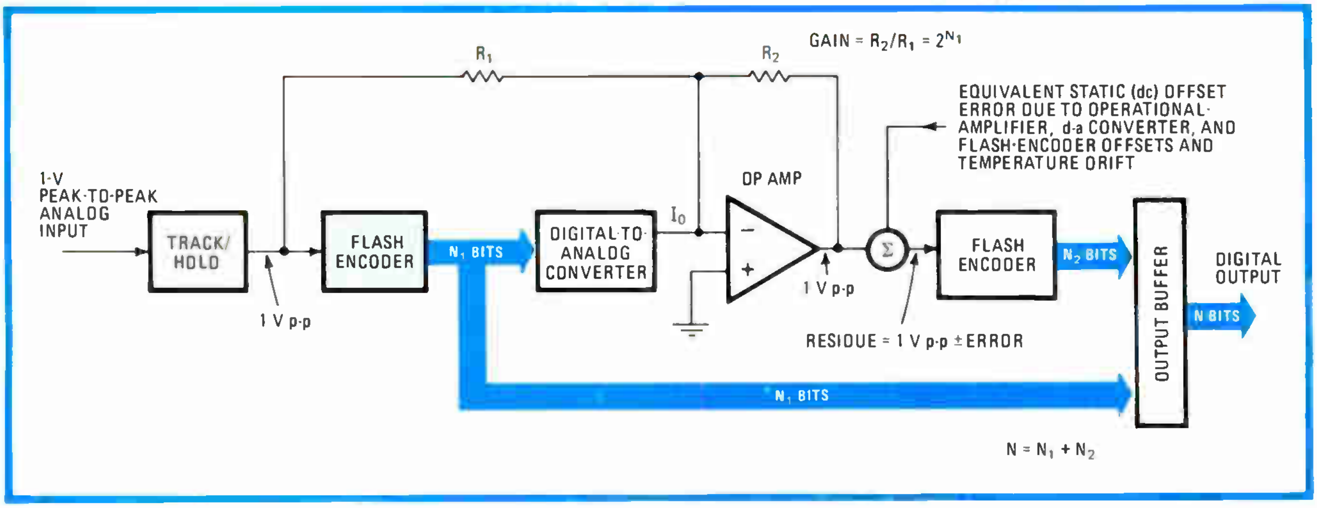
Subranging a-d converters are widely used at conversion rates of 1 megasample/second and higher and for resolutions of 9 to 12 bits. The conventional subranging a-d converter circuit (Fig. 1) employs two encoders, connected in series with one another. The encoders quantize the analog input signal and produce a binary output. They can be flash (parallel) or Gray (foldback amplifier) encoders. The digital error-correction scheme described here is useful only for subranging a-d converter circuits. As such, it is best understood by a closer examination of the error factors in a subranging a-d converter circuit.

## Encoder accuracy

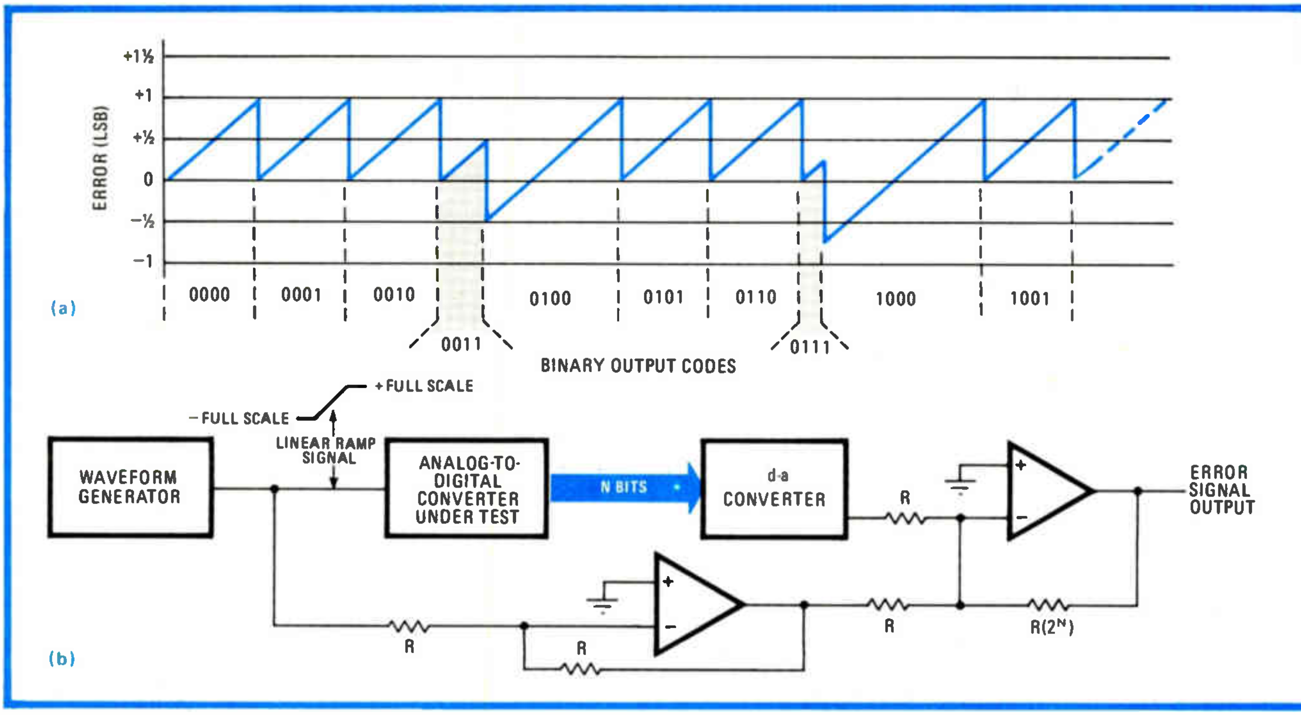
A conventional subranging a-d converter produces a binary output with a resolution of $2^N$, where N is the total number of converter binary bits, or $N_1$ plus $N_2$, the respective resolutions of the first and second encoders.

The first encoder must be at least as linear as the converter is overall, even though its resolution may be much lower. For example, a 10-bit subranging a-d converter with 10-bit linearity must have a first encoder whose minimum linearity is 10 bits, even though its resolution may be, say, 8 bits. A closer look at the circuit reveals why this is so.

The first encoder quantizes the analog input signal. The resulting digital word drives the digital-to-analog converter, whose output is subtracted from the original analog input signal and the difference amplified by the operational amplifier. The op amp's output is a composite signal, consisting of a "residue," or unquantized portion of the original analog input signal, plus any




**1. Subranging.** A conventional 9-to-12-bit analog-to-digital converter operating at rates of 1 megasample/second and higher uses a subranging conversion circuit. A common variation is the use of a Gray code (foldback amplifier) encoder in place of the first flash encoder.

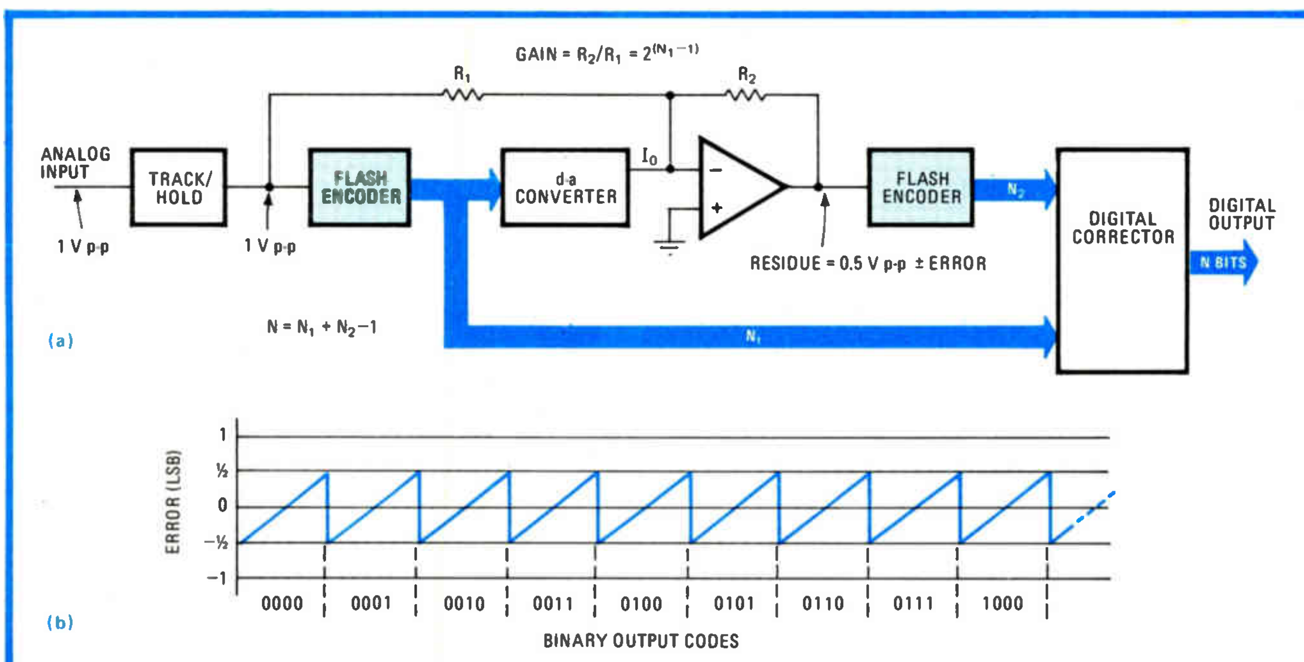



**2. Errors.** In a conventional 4-bit subranging a-d converter using two 2-bit flash encoders, the error at 0011-0100 is due to static offset effects, while the error at 0111-1000 is due to bias effects as well (a). The test circuit (b) measures converter input-signal linearity.

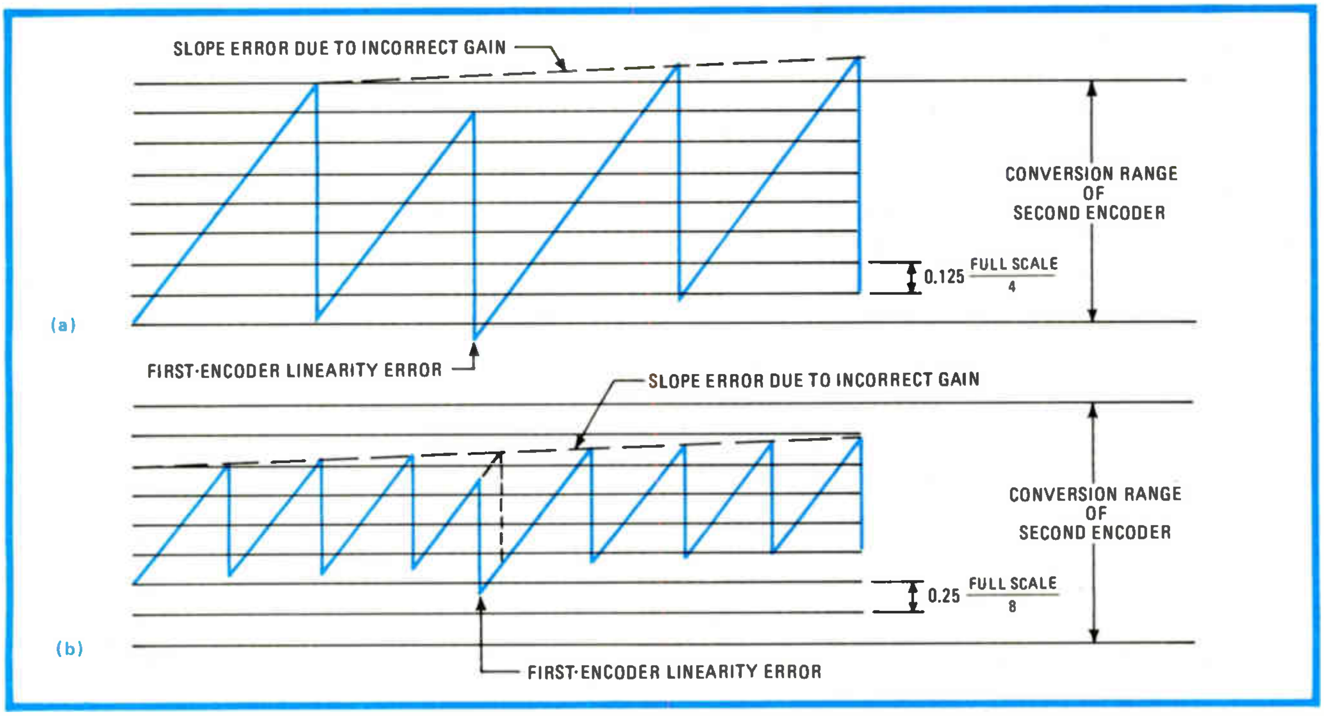
errors resulting from nonideal behavior of the encoding circuitry. These errors must be removed from the output signal if a low-accuracy (and thus low-cost) encoder is to be used. The second encoder quantizes the composite signal, producing an output byte that is combined with the digital output of the first encoder to form the final output of the a-d converter.

The circuit works much like a successive-approximation a-d converter circuit. The difference is that more than 1 bit at a time is encoded and the input to the d-a converter digital is in parallel. Such an arrangement allows operation at much higher speeds.

The required resolution can be provided only if the input range of the second encoder is equal to one quantization step of the first encoder and if the residue signal at the input of the second encoder is always within that encoder's input conversion range. Should the residue signal exceed the limits of the second encoder, signal




**3. Elimination.** Digital correction (a) can be used to eliminate conventional subranging a-d converter linearity errors. Note the error reponse (b) of the conventional circuit in Fig. 1 is within at least ±½ least significant bit, after the use of digital error correction.




**4. Residue.** When second-encoder input range is exceeded by residue and error signals in a conventional subranging a-d converter, information is lost (a). Digital correction improves signal linearity in the presence of the same signal errors and residue (b).

information is lost. On the other hand, a smaller residue signal than what the second encoder can handle results in the encoder's underutilization and subsequent loss of resolution. Consequently, the range of this encoder is set after amplification exactly equal to the ideal quantization error of the first encoder. Any other error causes the residue signal to exceed the bounds of the second encoder's input range. Irrevocable a-d conversion errors result and signal information is lost.

## Sources of error

The linearity of a conventional subranging a-d converter must generally reflect the sum of all the error sources in the design, including those contributed by the second encoder.

Figure 2a shows typical output errors of a conventional subranging a-d converter, as measured in the test setup of Fig. 2b. Those errors include:

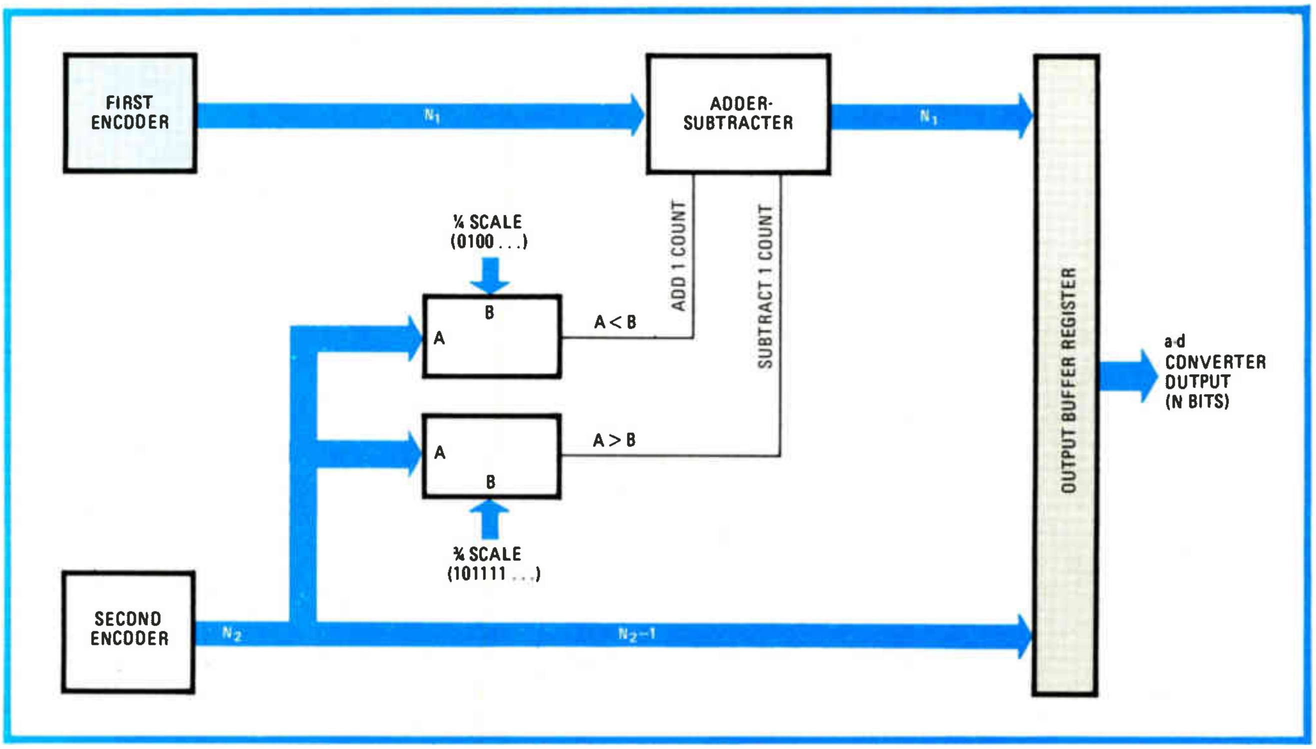
- Track/hold droop errors (dV/dt during hold time).
- First-encoder gain error.
- First-encoder offset error.
- First-encoder linearity error.
- Operational-amplifier offset error.
- D-a converter offset error.
- Second-encoder offset error.
- Operational-amplifier gain error.
- D-a converter gain error.
- D-a converter linearity error.
- Second-encoder gain error.
- Second-encoder linearity error.
- Noise generated by all components.
- Inadequate-settling-time errors due to the d-a converter and operational amplifier.

The first seven of these error sources can be ignored with the digital error-correction scheme to be described.

A digitally corrected subranging a-d converter circuit (Fig. 3a) is similar to the conventional subranging converter, save for the first encoder. An error-free, or ideal, waveform would appear as in Fig. 3b. In the digitally corrected circuit, the first encoder has 1 more bit of resolution. The residue input to the second encoder consists of the same elements as in the conventional circuit, but the quantization error is halved because of the doubled resolution. Figure 4a shows the residue signal for a conventional subranging a-d converter, and Fig. 4b, the results of adding another bit to the first encoder. Note that since the same error sources will not cause the residue signal to exceed the input range of the second encoder, provided that they add up to less than half the maximum input range (the other half is needed to quantize the ideal residue of the first encoder), no signal information is lost. Errors can be corrected by measuring them and subtracting their digital effect from the digital output. Error measurement is performed by the second encoder, which also provides its normal function of increased resolution for the a-d converter.

The digitally corrected circuit permits the existence of errors that, in a conventional design, would cause gross nonlinearities at the a-d converter output, at the cost of only 1 extra bit of resolution in the first encoder. Furthermore, the linearity of both the first and second encoders need only be commensurate with their resolutions.

Since component tolerances and accuracies are significantly relaxed in a digitally corrected design, monolithic flash encoders with conventional accuracies of within 0.2% may be used, reducing design costs, power dissipation, size, and failure rates. A flash encoder—of any resolution—for a conventional 12-bit a-d converter, for example, must be accurate to within 0.01%. Such a




**5. Digital correction.** This circuit can be used to correct linearity errors of conventional subranging a-d converters. In practice, the circuit can be simplified further by inserting an offset error at the first-encoder's input, so that its output is always less than ideal.

converter cannot be built without precision resistors, comparators, and potentiometers.

Furthermore, the accuracy of conventional designs is difficult to maintain in harsh environments; frequent recalibrations are needed. No such constraints hobble digitally corrected designs since their errors are completely corrected.

## Making corrections

The output of the digitally corrected converter's second encoder provides the additional resolution required to meet the converter's specification. It also contains a quantization of the linear and nonlinear errors that must be identified and corrected.

Linear errors include gain and offset errors, as well as track/hold droop. They appear as additive signals (in other words, they shift the output of the second encoder but do not cause linearity errors), provided the residue signal stays within the bounds of the second encoder. These errors (the first seven listed above) are rendered relatively harmless in a digitally corrected subranging design, appearing in the output as an equivalent dc offset that is easily adjustable to zero with a single offset control at the a-d converter input. No digital processing is required to correct these errors.

Nonlinear errors contributed by the first encoder—incorrect digital words at the encoder's output—require some digital processing. The digital-to-analog converter must be as linear as the overall a-d converter to ensure that the first encoder's nonlinearity is measurable. Hybrid d-a converters are available that take care of this aspect. Correcting the output bits of the first encoder simply involves subtracting the error from the output digital signal.

The nature of the digital processing can be seen most easily for the case where gain and offset errors are zero, and first-encoder linearity error is as shown in Fig. 4. It is assumed that the digitally corrected circuit is biased such that a perfect first encoder produces a residue signal ranging from ¼ to ¾ scale on the second encoder. If the residue signal is less than ¼ scale, the first encoder's output must have changed state too soon because of the error, that is, two of its transition zones are too close together and its output code should be one count less than it is when the residue signal is less than ¼ scale. When the residue signal returns above ¼ scale, the output code is correct again. It is at this point that the first encoder should have changed state. The binary output codes are always correct, then, if left unchanged, except when the second encoder produces an output of less than ¼ scale (when one count will be added to the first encoder's output) and when the second encoder produces a result in excess of ¾ scale (when one count must be subtracted from the binary output of the first encoder).

## Some modifications

Correction is implemented with the circuit of Fig. 5. This circuit may be simplified further by introducing an offset error at the input of the first encoder such that the encoder's output will always be less than ideal. Thus the circuit need never perform subtraction. Leaving the bits unmodified or adding them suffices.

In a further modification, the range of the second encoder is offset so that only its most significant bit is used to indicate whether or not a count is to be added to the first encoder's digital word. In practice, the correction circuit involves one or two adder chips. □

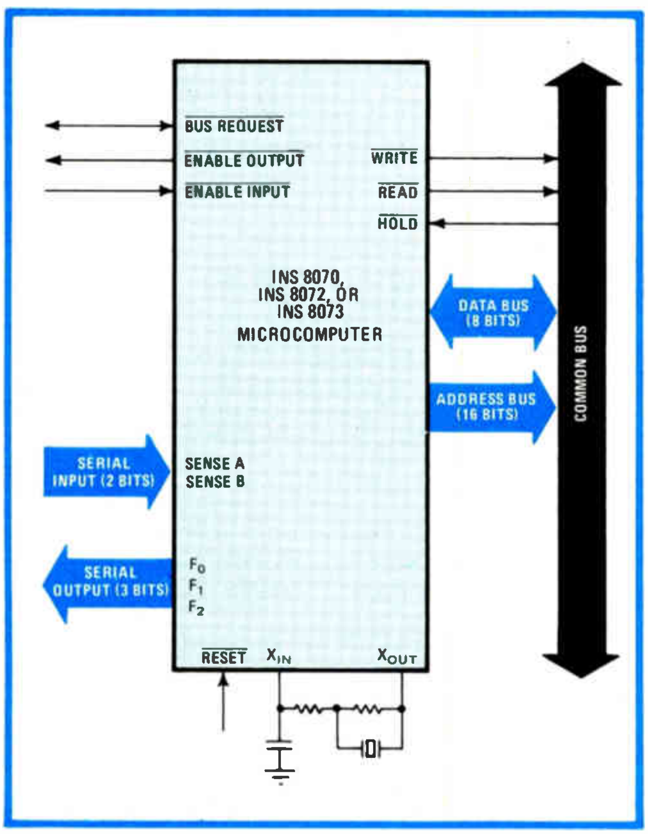
# Single-chip computer aims at multiprocessing

## 16-bit instructions also help bring word processing, personal computers, and smart terminals within reach

by Phillip Hughes, Thomas Dugan, James Handy, and Ronald Pasqualini, *National Semiconductor Corp., Santa Clara, Calif.*

☐ Many single-chip microcomputers aim only at low-end control applications, a high-volume market where they have found wide-ranging success. But as more memory becomes available on chip because of increasing semiconductor densities, they can set their sights higher—at terminals, personal computers, word processors, and even machines that speak only a high-level language.

Perhaps the most exciting openings lie in multiprocessing applications, in which several processors operate simultaneously on different programs while sharing common memory and peripherals. With their on-chip program and data memory, microcomputers are admirably suited to these situations because they seldom need to use the common bus and consequently all run at nearly full speed.




**1. Single-chip solution.** Series 70 microcomputers have identical pinouts. These govern the data, address, and control lines that make up the bus common to all multiprocessors as well as serial inputs (SA and SB), serial outputs ($F_0$, $F_1$, and $F_2$), and the bus priority control pins ($\overline{BREQ}$, $\overline{ENIN}$, and $\overline{ENOUT}$) essential for multiprocessing.

To serve this emerging market, National Semiconductor has developed its series 70 of 8-bit microcomputers, complete with on-chip read-only and read/write (random-access) memory. More distinctively, the devices include the control logic needed for handling the bus contention problem that is a part of multiprocessing. In short, they are ideal for applications requiring the economy of a single chip, the flexibility of multiprocessing, and the power and convenience of special 16-bit arithmetic instructions (Fig. 1).

### Multiprocessing purposes

In a multiprocessing application the data, address, and control lines of several processors are tied together, so that they form a common bus. However, only one processor at a time is allowed to use the bus, the other processors meanwhile keeping their pins in the high impedance state.

Ordinarily a substantial amount of extra hardware is needed to prioritize use of the bus and to ensure that no two processors attempt to use it simultaneously. On the series 70 microcomputers only a single additional pull-up resistor is needed on the bus request line ($\overline{BREQ}$), no matter how many processors happen to be sharing the bus (Fig. 2). That is made possible by the control logic built into the chips.

The enable output ($\overline{ENOUT}$) of the higher-priority microcomputer is connected to the enable input ($\overline{ENIN}$) of the one next in priority, thus forming a daisy chain of bus priority. Whenever a processor wishes to use the bus, it first checks to see if the ($\overline{BREQ}$) is active. If it is not, then it pulls $\overline{BREQ}$ low and checks to see if $\overline{ENIN}$ is active as well. If no other processor has made a bus request during the same clock cycle, then it receives control of the bus. Other processors that subsequently wish to use the bus will delay issuing their request until they observe $\overline{BREQ}$ going high.

However, it is possible for more than one processor to make a bus request simultaneously, especially if they have all been waiting for $\overline{BREQ}$ to go high. In this case, they will be granted use of the bus in the order determined by a hardwired priority scheme.

To illustrate, the top processor in Fig. 2 has the highest priority in the system because its $\overline{\text{BREQ}}$ line is connected to its $\overline{\text{ENIN}}$. It will maintain a high level on its $\overline{\text{ENOUT}}$ line until it has finished using the bus, and by passing this $\overline{\text{ENOUT}}$ signal along down the daisy chain of $\overline{\text{ENOUT}}$s to $\overline{\text{ENIN}}$s, it will prevent any other processor from attempting to use the bus.

When the highest-priority processor finishes with the bus, it releases its hold on $\overline{\text{BREQ}}$ and drives the $\overline{\text{ENOUT}}$ low. That output propagates to and enables the processor next in priority that is requesting use of the bus. This action continues down the daisy chain until all the processors that have simultaneously requested the bus have been granted its use. When the last of these processors releases $\overline{\text{BREQ}}$, the pull-up resistor brings it high, signaling to the ones that have been waiting that the bus is now available for them to issue their own bus requests, and the cycle repeats.

In this way no processor is locked out of using the bus even though it may have a low priority as determined by its position in the daisy chain. Regardless of priority, all waiting processors that issue their requests simultaneously will be serviced before any new requests are allowed.

## The architecture

Fabricated with a standard silicon-gate n-channel MOS process and requiring only a single 5-volt supply, members of the series 70 family include the INS8070, with 64 bytes of on-chip RAM for data and no program ROM; the INS8072, which adds 2.5-K bytes of ROM; and the INS8073, with a Basic interpreter stored in the 2.5-K bytes of ROM.

Each contains an 8-bit arithmetic and logic unit and an 8-bit accumulator (with an 8-bit extender for double-precision arithmetic). Also on the chip are four 16-bit registers for storing addresses—a program counter, a stack pointer (SP), and two other pointers ($P_1$ and $P_2$)—as well as a temporary register (T), used in multiply or divide operations, and a status register (Fig. 3).

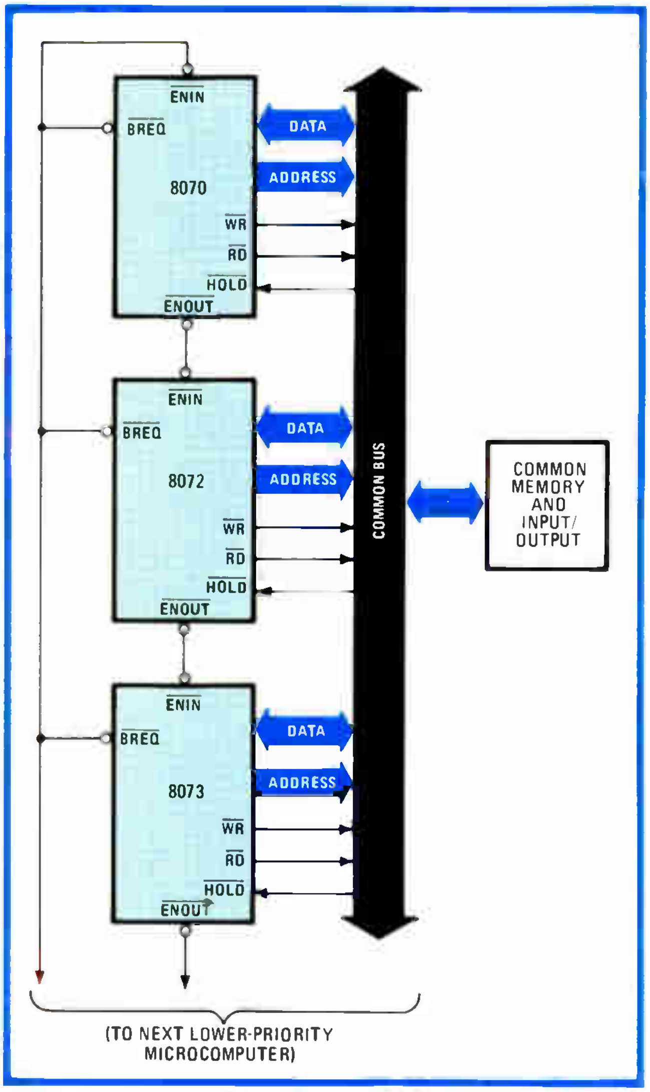
The series 70 instruction set contains several specialized instructions, two of which are especially helpful in word-processing applications. The SSM instruction, used to search and skip if a character is matched, scans memory for the character that matches the one being held in the accumulator. It searches the 256 bytes above one of the pointer registers and skips the next 2 program bytes if a match is found. This is handy for searching an ASCII file for an end-of-line marker, usually a carriage-return code. Since the instruction uses indexed addressing, the pointer register will be left pointing to the next character after the end-of-line marker when the match is found; nothing could be more appropriate for processing the next line in a text file.

Another ASCII-oriented instruction (BND) tests the character present in the accumulator and converts it into its BCD equivalent, if there is one. If it is not a valid ASCII decimal numeral, then a conditional branch is executed to a user-supplied service routine. Word-processing applications can employ this instruction for doing ASCII-to-BCD conversion while simultaneously checking for valid decimal characters.

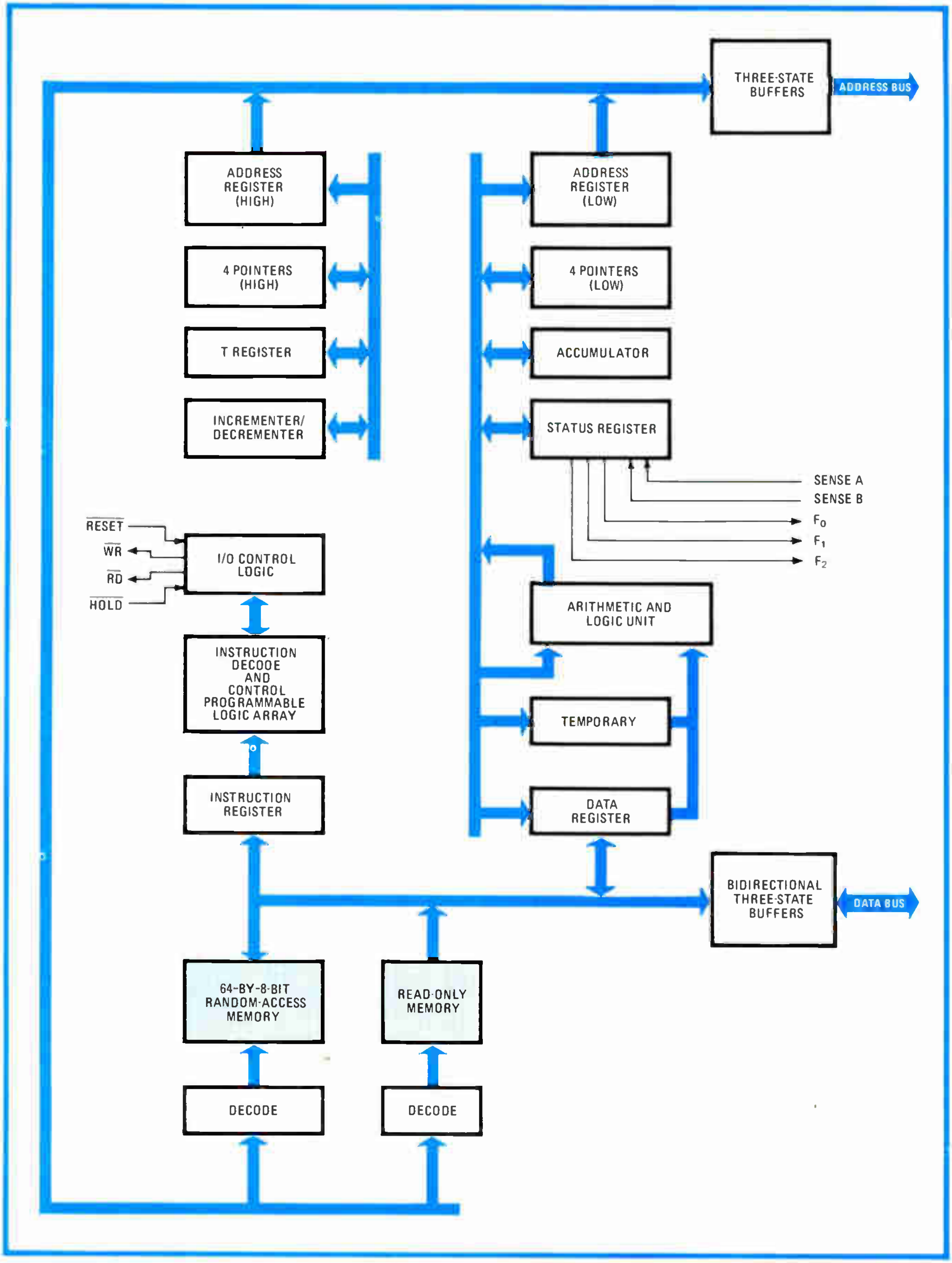
For multiprocessing, the ILD and DLD instructions are especially useful. The former increments the contents of any memory location while the latter decrements, thus in effect performing a read-modify-write operation. In multiprocessor applications, several processors may perform these operations on the same flag (memory location) in order to determine the next task to be performed and/or which processor will execute it. In order to ensure that tasks are correctly assigned, the ILD and DLD instructions retain the bus throughout the complete read-modify-write period.

## Multiplying fast

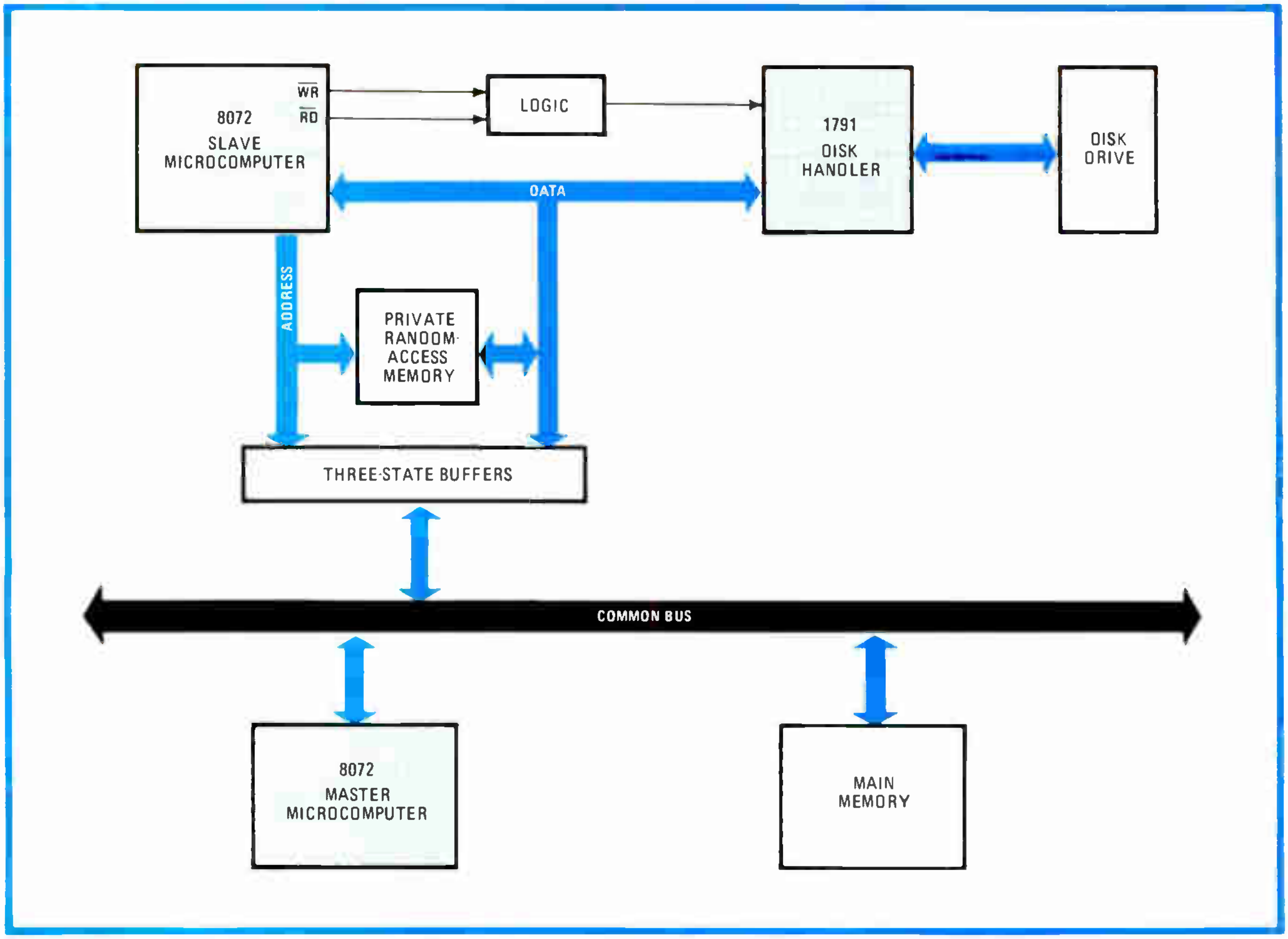
In applications that are number-intensive, the slow process of performing double-precision multiplication and division in software has been a bottleneck for 8-bit microcomputers. The series 70 processors have therefore been equipped with instructions that multiply and divide 16-bit integers directly. With a 4-megahertz clock, multiplying two 16-bit integers to obtain a 32-bit result can




**2. Multiprocessing made easy.** Several series 70 microcomputers may be connected to a common external bus quite conveniently. Bus use priority is a hardwired function built into the chips and needing only a pull-up resistor on the bus request line. The enable outputs are daisy-chained to the enable inputs of the various processors.




**3. Architectural features.** An 8-bit accumulator combines with an extension register for 16-bit operations; the temporary register assists with the multiply and divide instructions. Four 16-bit registers are supplied as well for convenient storage of addresses.




**4. Smart slave.** An intelligent disk controller may be formed by complementing the Western Digital 1791 disk handler with a series 70 microcomputer. The processor handles disk formatting, track and sector assignment, and file management, freeing the main processor.

be done in a fast 37 microseconds. A similar division takes 42 $\mu$s. Such speeds are comparable with those of many 16-bit microprocessors.

The key to the high speed achieved by these processors lies in their use of a programmable logic array acting as the internal microprogram that specifies the cycles necessary to execute each instruction. The speed of a PLA is, for all practical purposes, independent of the complexity of the logic equation that it realizes. In contrast, the speed of random logic implementations is usually inversely proportional to the complexity of the logic equation realized. Comparatively, then, the PLA makes faster work of the complex operations that many of the instructions mentioned above perform.

Ordinarily with these parts, input/output is memory-mapped so that all processors may use the memory reference instructions to communicate with the common peripherals. However, serial I/O may be performed directly, without using the common bus, by utilizing the two input pins, sense A (SA) and sense B (SB), along with the three output pins ($F_0$, $F_1$, $F_2$). In this way private serial I/O channels can be readily implemented, under software control, to communicate with devices like teletypewriters, terminals, and modems.

The series 70 microcomputer family has been designed to be especially effective in applications where high-level processing needs to be coupled with a low parts count. A case in point is a dumb terminal, which can be implemented with as few as 16 extra TTL packages. Intelligent terminals and personal computers need only the addition of external memory and mass storage interfaces.

## Another application

In fact, another series 70 device could be used as an intelligent controller acting as a slave for the main processor. An intelligent floppy-disk controller, for example, can be economically designed by adding a Western Digital 1791 (Fig. 4). While the 1791 actually handles the floppy drive, the slave processor can be performing the necessary housekeeping tasks such as diskette formatting and track and sector assignment, as well as general file management. Since the main processor is free to execute programs and released from the need to handle interactions with the disk, and since data transfers between host and slave are being carried out through direct access to common memory, system throughput is greatly increased.

Stand-alone applications, such as home appliances, often require that the processor communicate with untrained human operators in a high-level English-type language. The large ROM of these processors (up to 2.5-K bytes) suits them to these applications as well. □

## Transistor probe simplifies solid-state gaussmeter

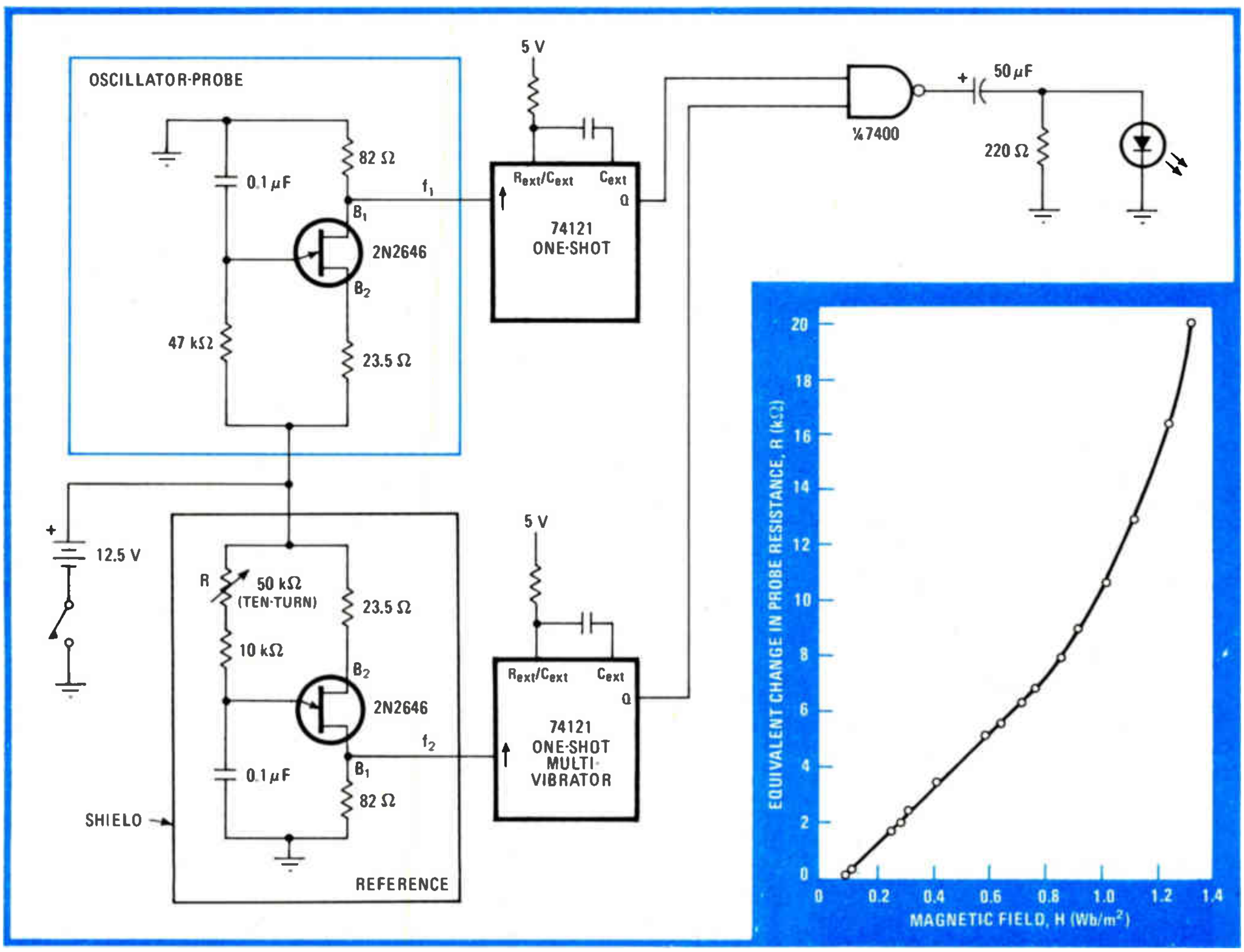
by Shanker Lal Agrawal and Rama Swami
*Banaras Hindu University, Department of Physics, Varanasi, India*

As a result of the subatomic energy exchanges that take place in many semiconductors because of particle-wave interaction, the electrical characteristics of the unijunction-transistor oscillator can be significantly changed by an external magnetic field. This property makes the low-cost unijunction transistor ideal for use as a probe in a gaussmeter or other flux-measuring instrument. Although it is not as linear, is not as easily calibrated, and does not provide the readout precision of some of the more elegant designs,[1] this circuit is simpler, just as sensitive, and virtually as accurate.

As shown, the gaussmeter is based on the comparator technique, wherein the frequency of the relaxation oscillator-probe is matched against a reference whose nominal frequency is about 400 hertz. Both generate positive-going spikes, which are lengthened by the pulse-stretching 74121 one-shot multivibrators. The NAND gate serves as a digital comparator, turning off the light-emitting diode when frequency $f_1 = f_2$.

In operation, the frequency of the reference oscillator is adjusted by resistor R until $f_2$ equals the free-running (free-field) frequency of the probe. Placing the oscillator-probe within the field to be measured will cause its frequency to change; potentiometer R in the reference must then be adjusted until the difference between $f_1$ and $f_2$ is minimized. The change in resistance of R from its nominal position may then be related to the strength of the magnetic field with the aid of the unit's individual calibration curve, which is shown at the right side of the figure.

As for calibration, at least three standard magnets will




**Flux finding.** The low cost of the rudimentary unijunction transistor, which is sensitive to externally applied magnetic fields, makes it ideal for use in comparison-type gaussmeters. The circuit range is 0 to 1.5 $Wb/m^2$, with circuit response linear to 1.0 $Wb/m^2$.

be required over the range of 0 to 1.5 weber per square meter, which is the range of the instrument. The circuit response is not likely to be linear above 1.0 $Wb/m^2$, and depending on the particular UJT used, the standard-marker points will vary considerably as a function of R. Still, the circuit will hold calibration and will serve well in most general-purpose applications. □

**References**

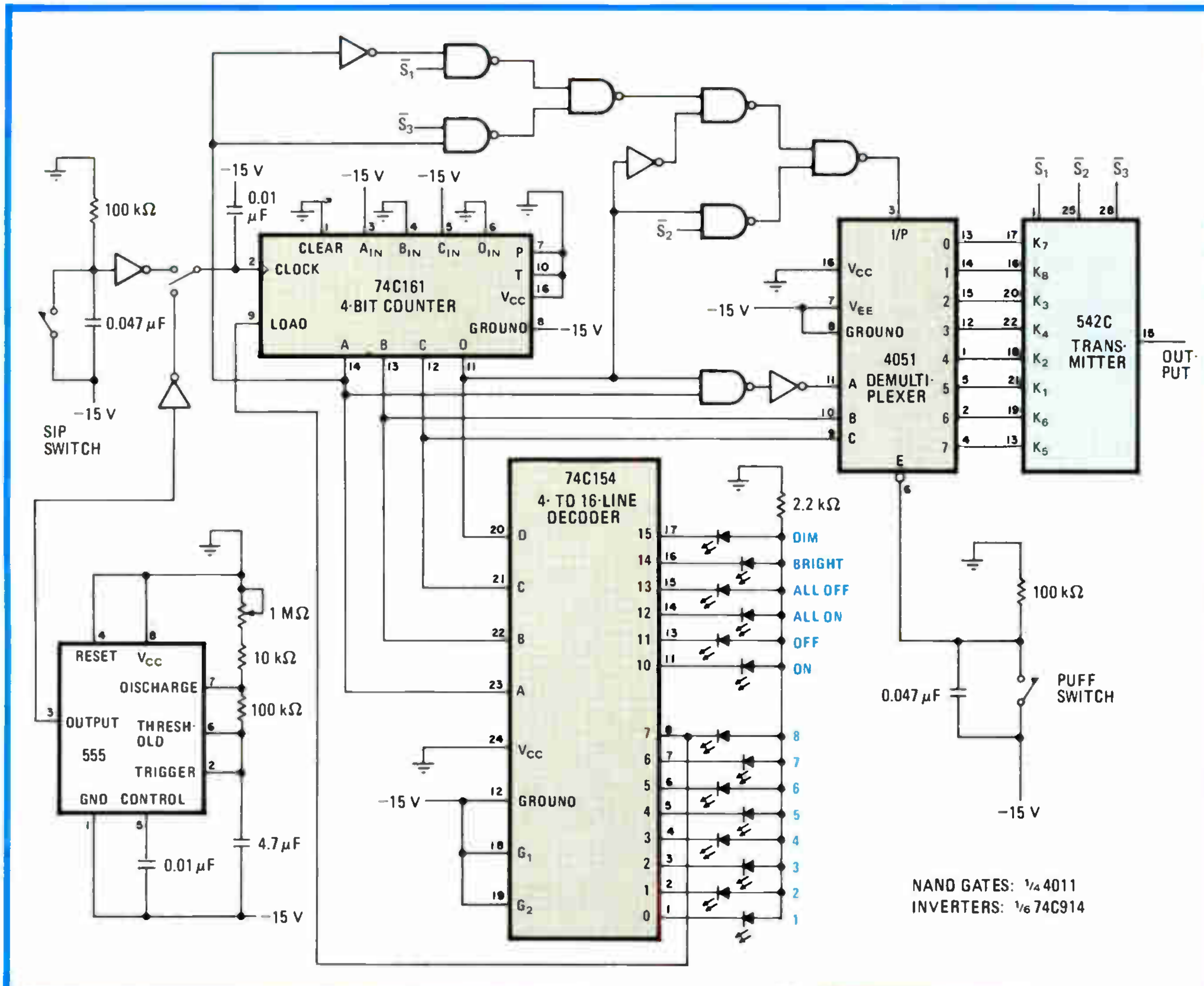
1. Henno Normet, "Hall-probe adapter converts DMM into gaussmeter," *Electronics*, Jan. 3, 1980, p. 179.

# Appliance-controller interface aids the paralyzed

by David Rye
*BSR (USA) Ltd., Blauvelt, N. Y.*

The popular BSR System X-10 controller, which serves so well in home-security systems, can be easily adapted for use by the paralyzed with this interface, whose puff-and-sip switches enable the handicapped to turn on appliances. Here, the switches are used to activate the desired output device via a stepped counter, instead of the push-button console normally required. Light-emitting diodes provide the visual feedback to the user.

The heart of the X-10 controller is BSR's 542C chip, which transmits a common-carrier code on the ac power line corresponding to the user-defined location of the desired appliance in the system, when it is appropriately addressed. The control signal is then decoded by plug-in modules connected to the individual appliances. This standard scheme is modified by adding circuitry to accommodate the sip switch, which is used to select the desired appliance, and the puff switch, which is used to




**Handy.** BSR X-10 controller, the heart of the Sears Home Control System, is easily adapted for the physically handicapped with interface that uses tongue-depress, head-activated, or sip and puff switches. Eight appliances can be activated. Eight additional commands provide all-on and all-off functions, light-dimming duties, and so on. Light-emitting diodes supply user with required visual feedback of controller's state.

**TRUTH TABLE: CONTROLLER FOR USE BY THE MOTION-HANDICAPPED**

| Count | Counter | | | | 4051 | | | 4051 O/P | K | S | Code sent |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | A | B | C | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $K_7$ | $\bar{S}_1$ | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $K_7$ | $\bar{S}_3$ | 2 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 2 | $K_3$ | $\bar{S}_1$ | 3 |
| 3 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 2 | $K_3$ | $\bar{S}_3$ | 4 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 4 | $K_2$ | $\bar{S}_1$ | 5 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 4 | $K_2$ | $\bar{S}_3$ | 6 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 6 | $K_6$ | $\bar{S}_1$ | 7 |
| 7 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 6 | $K_6$ | $\bar{S}_3$ | 8 |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | $K_7$ | $\bar{S}_2$ | * |
| 9 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $K_8$ | $\bar{S}_2$ | * |
| 10 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2 | $K_3$ | $\bar{S}_2$ | on |
| 11 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 3 | $K_4$ | $\bar{S}_2$ | off |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 4 | $K_2$ | $\bar{S}_2$ | all on |
| 13 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5 | $K_1$ | $\bar{S}_2$ | all off |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 6 | $K_6$ | $\bar{S}_2$ | bright |
| 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7 | $K_5$ | $\bar{S}_2$ | dim |

transmit the corresponding code onto the power line.

The modification is made with the aid of a 74C161 4-bit counter for stepping and a 4051 demultiplexer for code selection, as shown. In this configuration, the address lines of the 4051 are controlled by the divide-by-16 counter, whose outputs step through a count of 0 to 7 twice in each 16-count cycle when advanced by the sip switch, which serves as a clock (see truth table). The eight K inputs of the 542C will therefore be selected in sequence, twice for each complete cycle of the counter. The circuit is wired so that numbers 1 to 8 corresponding to the numbered wall module are transmitted during the first eight clocked states of the counter. The D output of the counter is low at this time, and odd numbers are sent when $\bar{S}_1$ is at logic 1. Even numbers occur during the time that $\bar{S}_3 = 1$, meaning that $\bar{S}_1$ or $\bar{S}_3$ can be selected by the A output of the counter, which is high on odd counts and low on even counts.

Alternatively, the 555 timer can be used for the clock to yield automatic code selection. This eliminates the need for the sip switch, making the controller easier to operate. An external potentiometer is included to set the scanning speed to the user's preference and ability.

In either case, outputs 0 to 7 of the 4051 are enabled in sequence. Note that each is connected to the K inputs of the 542C in such a manner as to ensure that the transmission of numbers is in the correct order. It is seen that the proper sequence can be transmitted by using the counter's A output to select $\bar{S}_1$ or $\bar{S}_3$, using the D output to disable the A input of the 4051 so that only even-number outputs on the multiplexer are enabled, and connecting the four even-numbered outputs to the appropriate K inputs of the 542C.

Eight additional functions can be sent on the second eight counts, including the off, on, all-off, all-on, bright, and dim commands. The D output of the counter is set high during this time. $\bar{S}_2$ is selected when D = 1. Under this condition, the input to the 4051 is a binary number that steps from 0 to 7, and all its outputs will be enabled in sequence.

Note that during counts 8 and 9, the 542C transmits invalid codes. It is therefore suggested that these states be avoided. To achieve this, it is necessary to preset the counter to 10 after count 7 is decoded.

The 4-to-16-line decoder (74C154) monitors the state of the counter. Fourteen light-emitting diodes indicate the function addressed, thus providing the user with the necessary feedback information. □

## Calculator notes

# TI-59 inverts Laplace transforms for time-domain analysis

by Kin-chu Woo, *Texas A&M University, Department of Electrical Engineering, College Station, Texas*

Performing quick mathematical inversion of Laplace transforms so that they may be instantly analyzed in the time domain, this short program will be highly useful to engineers engaged in network design. Many transforms can thus be converted and evaluated, with the only restriction being that of the user's ability to express the terms with the limited set of key functions available.

Taking the given Laplace transform, F(s), the program finds the function's corresponding value for any specified time, t, from the following equation derived by Gaver:[1]

$$f(t) = \frac{\ln 2}{t}\sum_{i=1}^{10} V_i F\left(\frac{\ln 2}{t} i\right)$$

where the set of $V_i$ coefficients are constants, and it is assumed that f(t) is suitably bounded and well behaved.

As for the mechanics of introducing the functions,

## TI-59 PROGRAM FOR REAL-TIME ANALYSIS OF LAPLACE TRANSFORMS

| Location | Code | Key | Location | Code | Key |
|---|---|---|---|---|---|
| 000 | 76 | *LBL | 028 | 71 | SBR |
| 001 | 11 | A | 029 | 16 | A' |
| 002 | 35 | 1/x | 030 | 65 | × |
| 003 | 65 | × | 031 | 73 | RCL *Ind |
| 004 | 53 | ( | 032 | 00 | 00 |
| 005 | 02 | 2 | 033 | 85 | + |
| 006 | 23 | ln x | 034 | 43 | RCL |
| 007 | 54 | ) | 035 | 12 | 12 |
| 008 | 95 | = | 036 | 54 | ) |
| 009 | 42 | STO | 037 | 42 | STO |
| 010 | 11 | 11 | 038 | 12 | 12 |
| 011 | 25 | CLR | 039 | 97 | Dsz |
| 012 | 42 | STO | 040 | 00 | 00 |
| 013 | 12 | 12 | 041 | 12 | B |
| 014 | 01 | 1 | 042 | 53 | ( |
| 015 | 00 | 0 | 043 | 43 | RCL |
| 016 | 42 | STO | 044 | 12 | 12 |
| 017 | 00 | 00 | 045 | 65 | × |
| 018 | 76 | *LBL | 046 | 43 | RCL |
| 019 | 12 | B | 047 | 11 | 11 |
| 020 | 53 | ( | 048 | 54 | ) |
| 021 | 43 | RCL | 049 | 91 | R/S |
| 022 | 11 | 11 | 050 | 76 | *LBL |
| 023 | 65 | × | 051 | 16 | A' |
| 024 | 43 | RCL | · | · | · |
| 025 | 00 | 00 | · | · | · |
| 026 | 54 | ) | · | · | · |
| 027 | 53 | ( | · | 92 | INV SBR |

| Registers | |
|---|---|
| $R_1$ | 0.0833333333 |
| $R_2$ | −32.08333333 |
| $R_3$ | 1279.000076 |
| $R_4$ | −15623.66689 |
| $R_5$ | 84244.16946 |
| $R_6$ | −236957.5129 |
| $R_7$ | 375911.6923 |
| $R_8$ | −340071.6923 |
| $R_9$ | 164062.5128 |
| $R_{10}$ | −32812.50256 |

**Instructions**

- Key in program and place equation coefficients $V_i$ in registers 1–10
- Enter the desired Laplace transform in the program subroutine:

  *GTO *A', LRN, (enter function), INV SBR, LRN*
- Specify the time for which the function is to be evaluated:

  *(t), A*

  The calculator will display the corresponding value of the function.

**EVALUATION OF $1/s^4 \longleftrightarrow t^3/6$**

| t (s) | True value (t function) | Calculated (s function) |
|---|---|---|
| 1 | 0.1667 | 0.1657 |
| 2 | 1.3333 | 1.3254 |
| 3 | 4.5000 | 4.4732 |
| 4 | 10.6667 | 10.6030 |
| 5 | 20.8333 | 20.7090 |
| 6 | 36.0000 | 35.7852 |
| 7 | 57.1667 | 56.8256 |

they are entered via a subroutine, with the keyboard functions serving to represent the operations performed on the variable *s*. A large class of functions containing the expressions $s^{1/2}$, $s^n$, and $e^s$ may thus be represented with little difficulty, with the only precaution being that the user appropriately isolate the terms of the function, especially the variable s, by using parentheses keystrokes. For example, with $F(s) = (1/s^{1/2})e^{-2/s}$, the exponential term is first entered with STO 13 ((RCL 13) × 0.5), 1/x, ±, INV ln x, ×. Then, for the remainder of the function, ((RCL 13) √x), 1/x, =. Note that the programming of a function always begins with the variable s (specified by the program itself) and that it is usually advantageous to store it in a register (for example, STO 13), as shown.

Consider the simple example where the short-term output voltage of a network is given by $V_o(s) = 1/s^4$. This function can be simply expressed with the key sequence 1/x, $x^2$, $x^2$. Entering this sequence into the subroutine as instructed and specifying the times over which the function is to be evaluated yields the results shown in the table. The results compare favorably with the equivalent time-domain function, $t^3/6$. □


**References**

1. D. P. Gaver, "Observing Stochastic Processes and Approximate Transform Inversion," Operational Research, Vol. 14, No. 3, 1966, pp. 444–459.

# Engineer's newsletter

**Check out data encoding with new tests**

Want to find out if your data-encryption chip is working properly? Unfortunately, it is not easy to know if something is going wrong, since determining if an encryption is as good as it might be is laborious. The National Bureau of Standards has come to the rescue, however, with **four readily applied in-service tests that are fast enough to test the chips in actual operation.** Send $2 for Stock No. 003-003-02225-0 to the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. The 29-page publication tells how to make sure that unclassified data transmission is secure.

**Keep your LCD warm**

With winter coming, there's word that existing printed-circuit heaters can help protect liquid-crystal displays used in cold environments. With the heaters, for example, LCDs can replace mechanical counters and light-emitting-diode readouts in gasoline pumps. In fact, when the devices are placed behind the LCD, high-contrast digital readouts are possible at temperatures as low as −45°F. Only low voltage is needed, and **the etched-foil heaters consume a low 2 to 5 W.**

High-volume prices are approximately $1 for heaters measuring 1 in. wide and 4 in. long. They are made from Kapton, silicon rubber, and neoprene dielectric material and can be applied to the LCD using pressure-sensitive adhesive or liquid adhesives. Alternatively, they can be simply held in place with a pressure mounting.

The heaters are designed to custom requirements and can be supplied with an integral thermistor for temperature sensing. Information can be obtained by writing Sierracin/Thermal Systems, 13920 South Broadway, Los Angeles, Calif. 90061, or calling (213) 321-4350.

**Connector standard extended to 75 Ω**

If you're a microwave or radio-frequency engineer concerned with the new generation of standard 14-mm rigid precision coaxial lines and associated hermaphroditic precision coaxial connectors, you'll want the new International Electrotechnical Commission standard on such devices. An updated version of IEC Publication 457-3 (originally issued in 1974 and covering only connectors with a characteristic impedance of 50 Ω), the latest edition has been extended to cover connectors of the same design but with a characteristic impedance of 75 Ω.

**The standard describes mechanical, electrical, and environmental specifications of the 14-mm precision connector,** the reflection coefficient and attenuation of which has to be measured up to 8.5 GHz for 50 Ω and to 9.5 GHz for 75 Ω. For a copy, write to the IEC at 1 rue de Varembé, 1211 Geneva 20, Switzerland. The 13-page document costs 18 Swiss francs.

**Make a precision pot decision**

A small but mighty slide rule offered gratis by Beckman Instruments' Helipot division **allows design engineers to select standard single-turn and multiturn potentiometers easily.** The desktop reference guide gives vital information on Beckman's standard line of pots, consisting of some 44 model numbers. Among the specifications included are number of turns, starting and running torque, resistance ranges, linearity, tolerance, power rating, ambient temperature ranges, and rotational load life. The slide rule also is an aid in comparing Beckman pots with those of the competition.

Write Beckman Instruments Inc., Helipot Division, 2500 Harbor Blvd., Fullerton, Calif. 92634, or phone (714) 773-8355. **-Harvey J. Hindin**

# The most advanced one-now user-programmable.

Motorola's new MC68701 is the user-programmable version of the industry's most advanced single-chip microcomputer in production today, the MC6801.

The MC68701 microcomputer has all the power, speed and design flexibility of the MC6801, and the original combination of on-chip functions, too. But where the MC6801 has mask-programmable ROM, the MC68701 provides 2K bytes of MCM2716-equivalent EPROM.

This on-chip EPROM adapts the MC68701 especially well for prototyping, because the control program is easily evaluated and changed during development. User programmability also makes the MC68701 ideal for low-volume systems where factory programming isn't practical, for initial production field test units of a user's system, and for systems that require reprogramming in the field.

Filling out the powerful complement of MC68701 on-chip functions are, of course, the high-efficiency, enhanced MC6800-type CPU, 128 bytes of RAM, 29 parallel I/O lines, a serial communications I/O port, a clock and a 16-bit programmable timer.

## User-selectable operating modes.

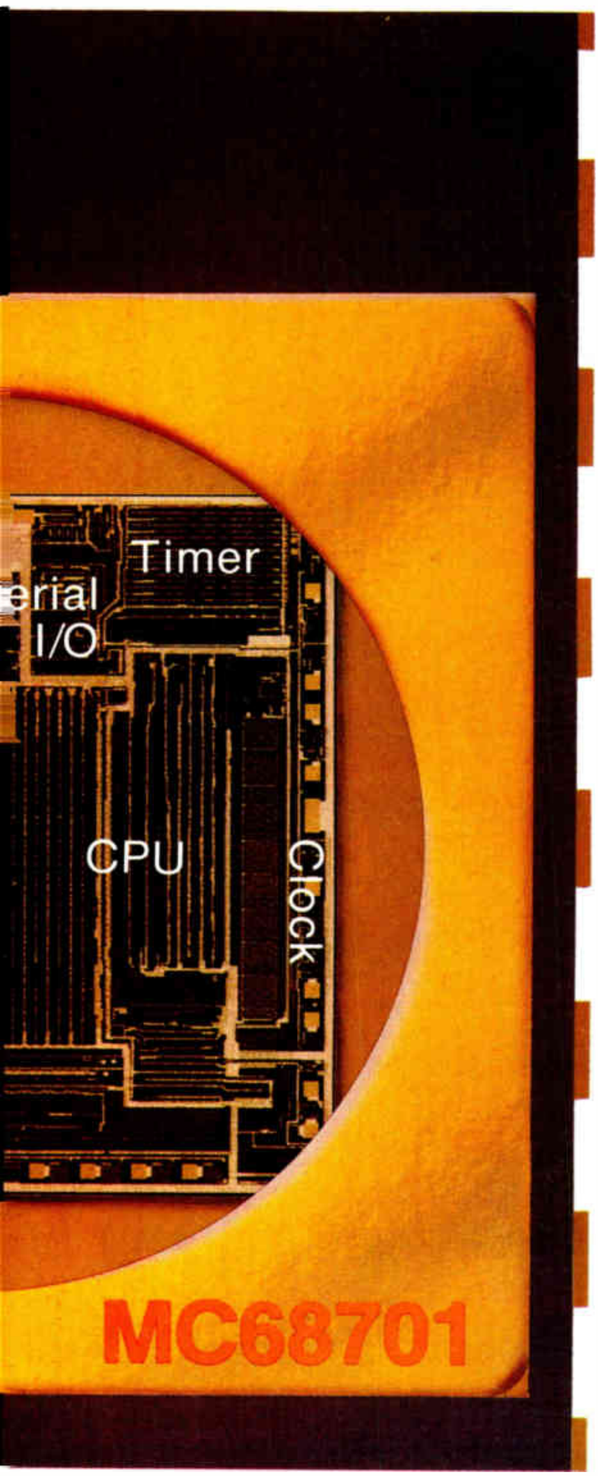
The unique flexibility of the MC6801-MC68701 is rooted in the wide range of built-in, user-selectable operating and test modes. Among them are the three basic operating modes.

In the single-chip mode, all ports are configured for I/O–29 I/O and two control lines. The expanded multiplexed mode enables an impressive 64K-byte addressing capability. And, in the expanded non-multiplexed mode, no external logic is required to directly address 256 external locations, including any and all M6800 Family peripherals. Thirteen to 20 I/O lines are still available.

Additional modes permit testing and other special operations. In all modes, the 16-bit timer can count or time events and generate or measure pulses. The complete combination represents an unparalleled advance in design convenience.

The on-chip, fully-buffered Serial Communications Interface (SCI) offers operation at four baud rates—full duplex asynchronous formats. The SCI operates at over 75K baud, and other special features—such as wake-up capability, NRZ and biphase—promote efficient multiprocessor system configuration.

# chip microcomputer is Motorola's MC68701.




The MC6801-MC68701 CPU is an enhancement of the highly-capable MC6800 which puts seven addressing modes at the designer's disposal. An MC6800 machine-code-compatible instruction set is expanded by 16-bit instructions, including a 10 μs hardware multiply. Execution time of most instructions has been reduced by reducing the instruction cycle count to increase throughput.

Compare the MC6801-MC68701 to any other general-purpose, single-chip microcomputer for on-board functional capability, programming ease and system performance. We believe the MC6801-MC68701 can get you to market faster, with more competitive designs.

## Total hardware, software and training support.

Motorola fully supports the MC6801-MC68701 in every way. The entire, fully-compatible M6800 Family provides a broad range of microcomponents and memories for system expandability. One of the highest VLSI production capabilities in the world and the Motorola training course curriculum back up the product. EXORciser® development systems and Motorola development software support all M6800 Family units, including MC6801-MC68701.

For additional information, contact your Motorola sales office or authorized distributor, or write to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

Motorola's MC6801-MC68701 is the world's most versatile single-chip microcomputer, representative of Motorola's dedication to product excellence.

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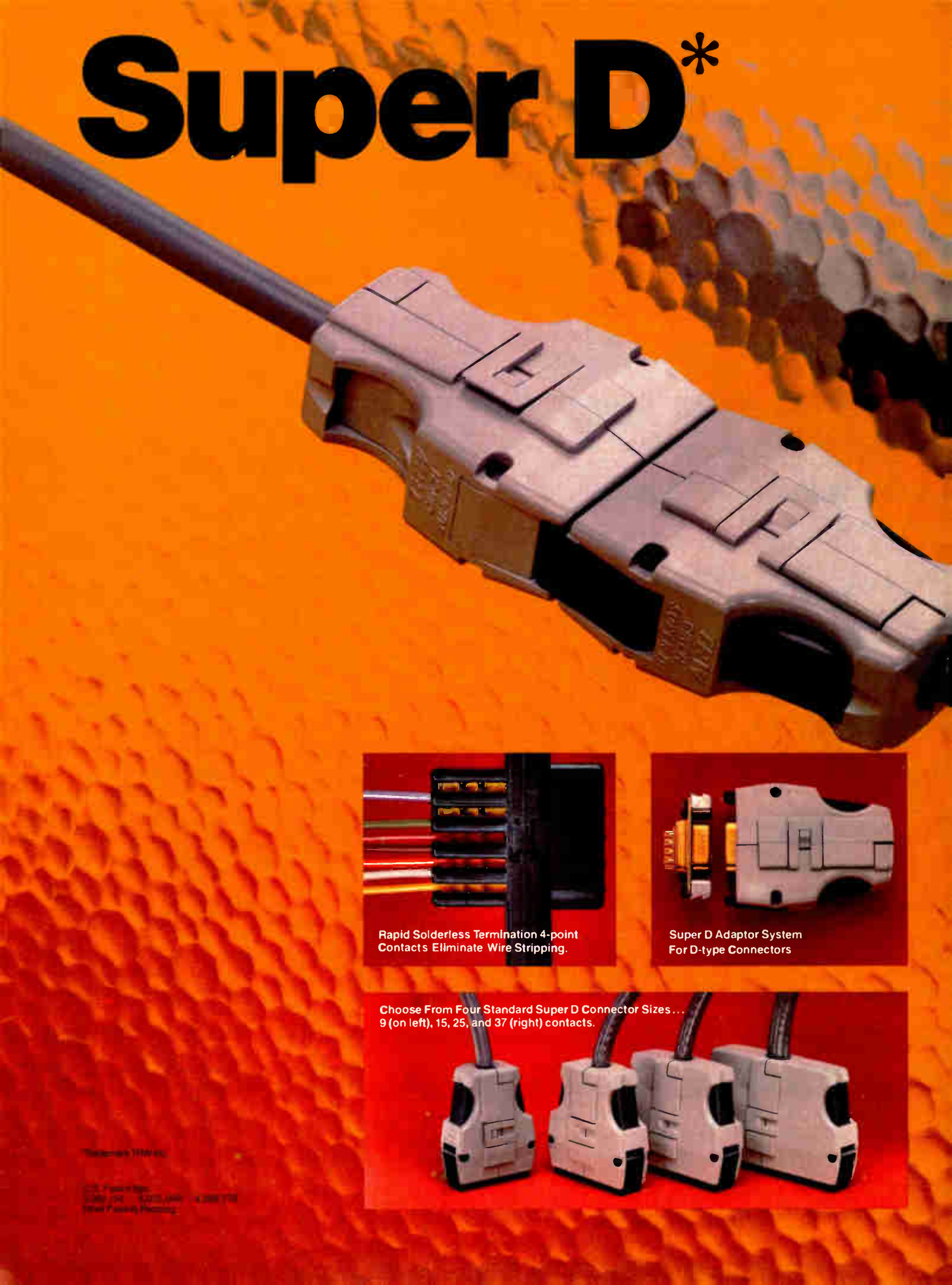

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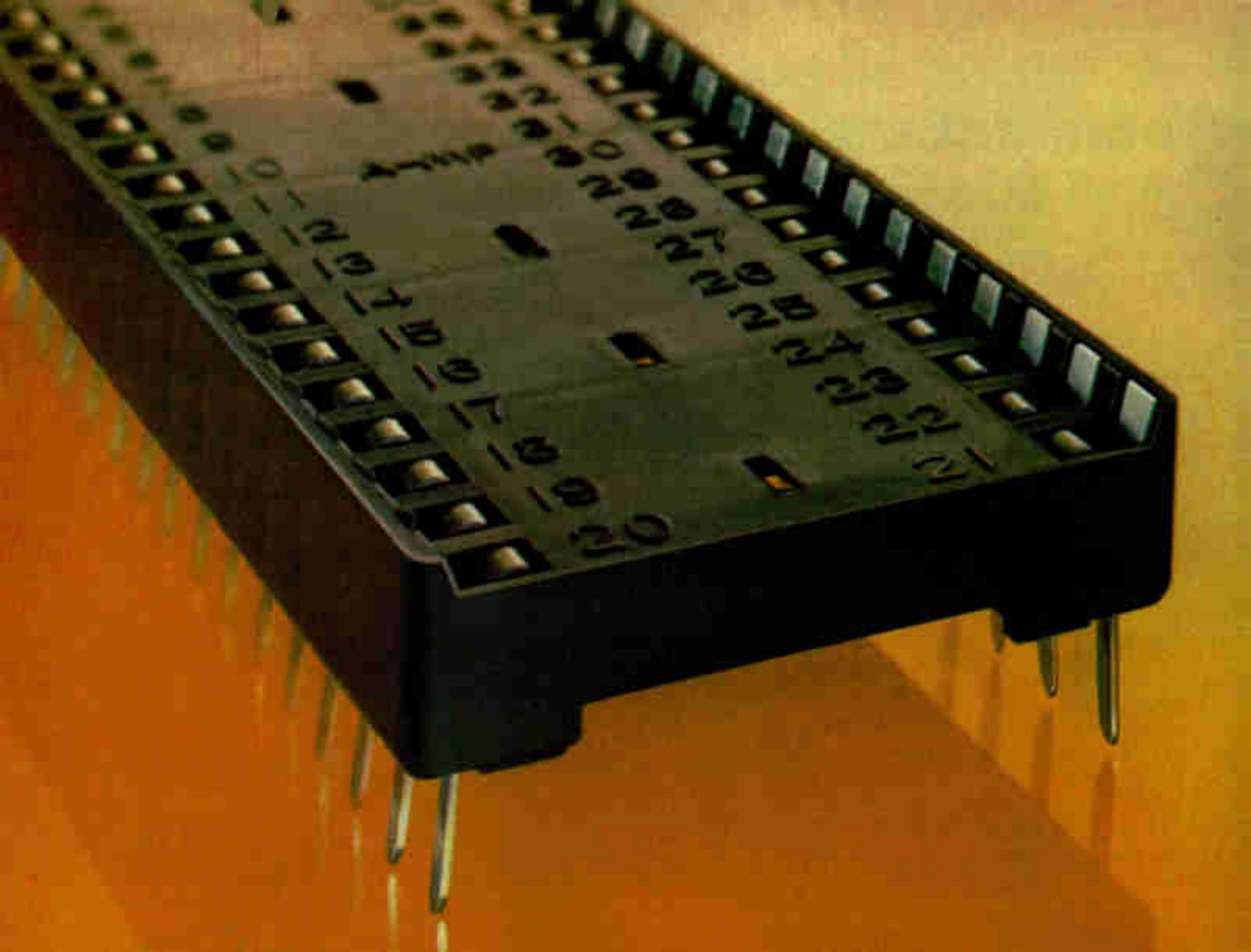

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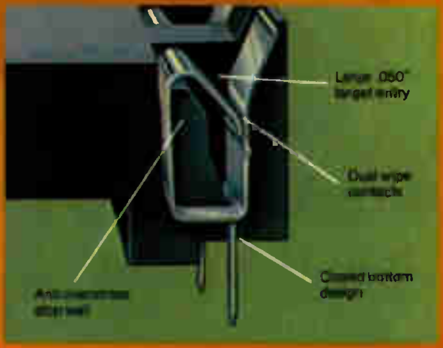

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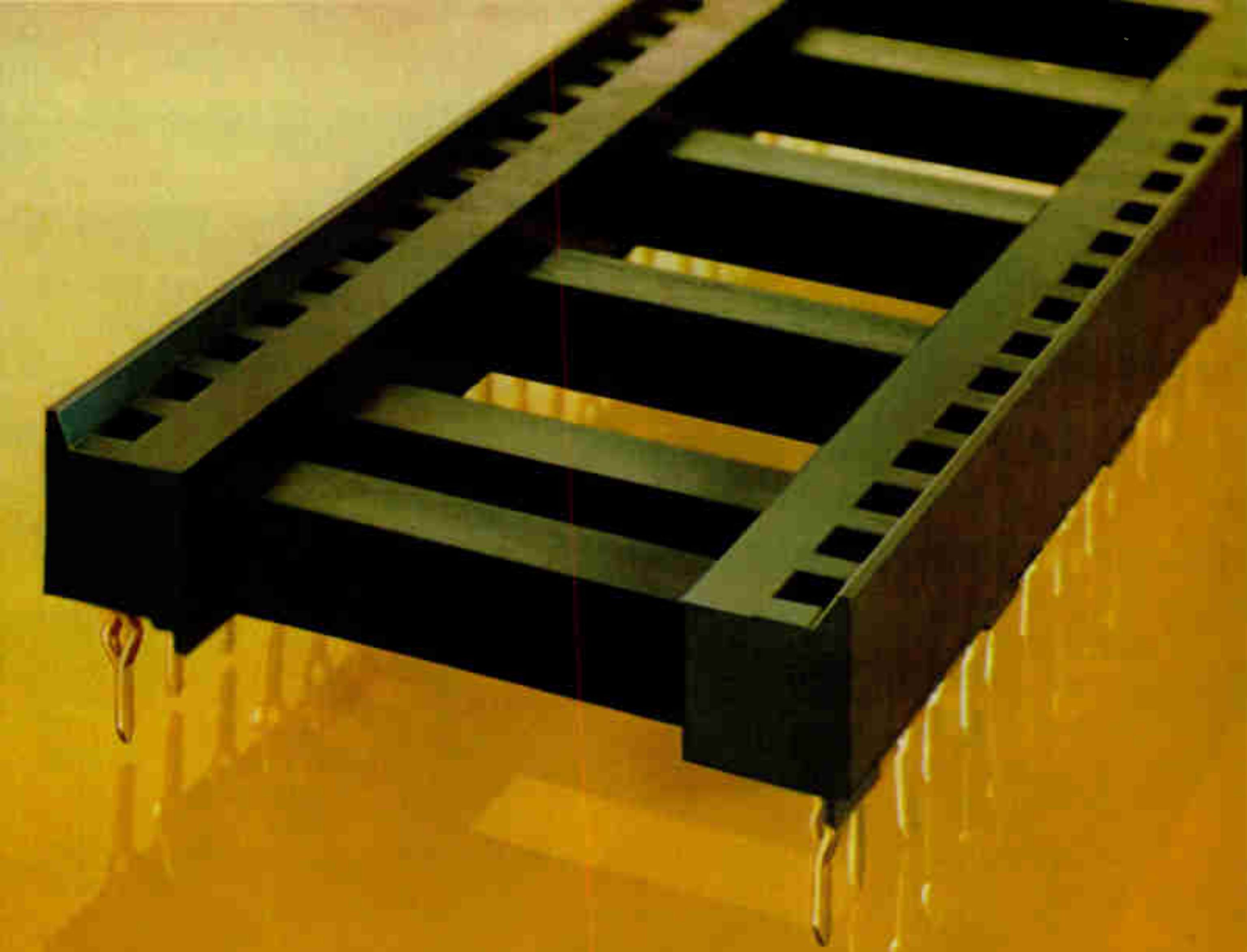

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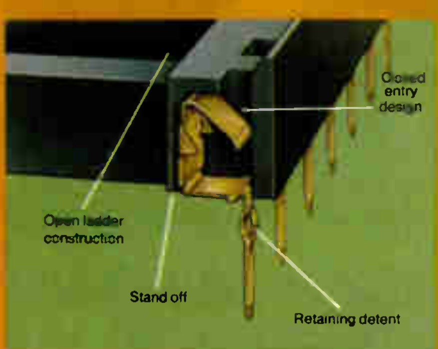


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# Storage scope samples at 50 MHz

Special CCD helps digital oscilloscope achieve sampling rate without expensive high-speed analog-to-digital converter

by John Gosch, Frankfurt bureau manager

**Many oscilloscope makers** have beaten NV Philips Gloeilampenfabrieken to the punch with digital storage scopes, but the Dutch electronics giant is determined to make a virtue of its tardiness. By biding their time while the Philips components specialists developed their new scope's key element, a so-called profiled peristaltic charge-coupled device ($P^2CCD$), designers at the Eindhoven-based Scientific and Industrial Equipment division have leapfrogged the competition with a dual-channel digital storage scope that offers higher performance at a lower price.

The PM 3310 has a sampling frequency of 50 MHz and an analog bandwidth of 60 MHz. Repetitive signals with frequencies up to the analog bandwidth limit can be stored, as well as single-shot events that occur at frequencies within the Nyquist-criterion limit. The scope will sell for about $5,900 in the U. S., less than the price of other digital scopes with lower sampling rates.

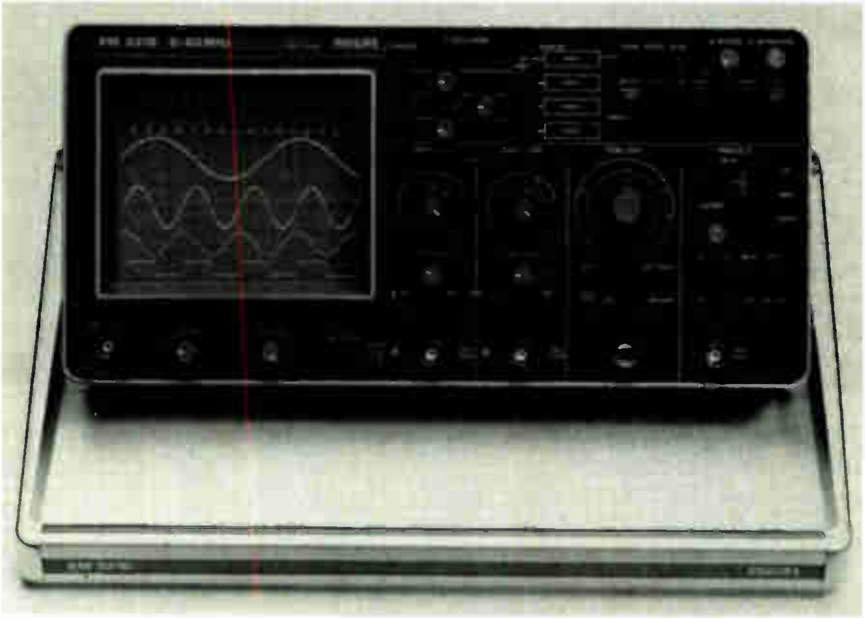
The new instrument, from the division's Test and Measuring Equipment group, is being shown for the first time at Interkama, the international instrumentation and automation exhibition being held in Düsseldorf, West Germany, Oct. 9–15. It can be had in small quantities in Europe and the U. S. right after that event, "with larger numbers available early next year," says Rob van der Werf, the group's product manager for oscilloscopes.

The $P^2CCD$ used in the scope evolved from a purely experimental component in the Philips research labs a few years ago [*Electronics*, Sept. 4, 1975, p. 53 or 5E] into a product ready for commercial use at the company's Electronic Components and Materials division. "This is another example of a development in one division having a stimulating effect on equipment design at another," van der Werf notes.

**In a name.** The $P^2CCD$ is called profiled because the charge-transfer layer includes an extra surface-transfer layer on top: a thin, heavily doped region over the less-doped bulk layer. Charge packets are transferred down the line in peristaltic movements reminiscent of the alternating waves of contraction and dilation that move food through the digestive tract—hence that part of the name. The $P^2CCD$ can operate at a higher clock rate and higher transfer efficiency than conventional charge-coupled devices.

The new device replaces the expensive high-frequency analog-to-digital converters used in other storage oscilloscopes—converters that can cost as much as $1,000. The $P^2CCD$ is effectively an analog shift register with a short transfer time and large charge-handling capacity. The signal is fed in as a high-frequency series of charges; it is read out at a much lower frequency, yielding a signal typically at 78 kHz. A low-cost, low-frequency a-d converter can then be used to change the signal into digital form for storage in solid-state memory. The contents of the memory are reconverted into analog form for display as discrete dots on the screen.

"The savings achieved by employing a $P^2CCD$ were partly passed on to the customer and partly used to provide the PM 3310 with some special features," van der Werf says. The instrument has a remote-control



facility, four separate 2-K (2,048-bit) banks of random-access memory for storing digitized waveforms, an output for X-Y and chart recorders, and pre- and post-triggering extending from −9 to +9,999 divisions. A roll mode for analyzing slow-moving phenomena allows samples to be taken every 0.2 s; at that rate, 40 hours' worth of data may be stored.

In addition to those of a conventional analog scope, the prime applications of the PM 3310 are in analyzing single-shot events that may be encountered in destructive tests and in investigating multiple-shot events like spikes occurring at unknown intervals in power supplies.

**Single shots.** The PM 3310 provides a good representation of single-shot signals up to 5 MHz with virtually no loss of information and a reasonably good representation of such signals up to 12.5 MHz with only a small loss of information. Single-shot bandwidths up to 25 MHz can be handled with computer analysis. The scope feeds the data via its IEEE-488 or IEC-625 bus interface to the data-processing system.

Either or both inputs to the dual-channel instrument are stored in the four memories as needed—by manually selecting the signal from the first accumulator memory for guarding in one of the other three or by automatic transfer in sequential fashion until all memories are filled.

The contents of all four memories can be displayed simultaneously, with each occupying one fourth of the 8-by-10-cm screen. The display is a 250-by-250-dot matrix for the content of each memory bank, or a 250-by-1,000-dot matrix (1,000 dots in the vertical dimension) for the whole screen. In the scope's dot-join mode, the dots are linked to give a continuous and clear display of the waveform.

Separate light-emitting-diode displays indicate the attenuator and time-base settings at the time of recording of each stored waveform.

NV Philips Gloeilampenfabrieken, Scientific & Industrial Equipment Division, TQ III-4, Eindhoven, the Netherlands [351]

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# Microcomputer has 32-K ROM on chip

Fully pin– and op-code–compatible with the 8048, the single-chip 8050 has four times as much memory

*by Bruce LeBoss, San Francisco regional bureau manager*

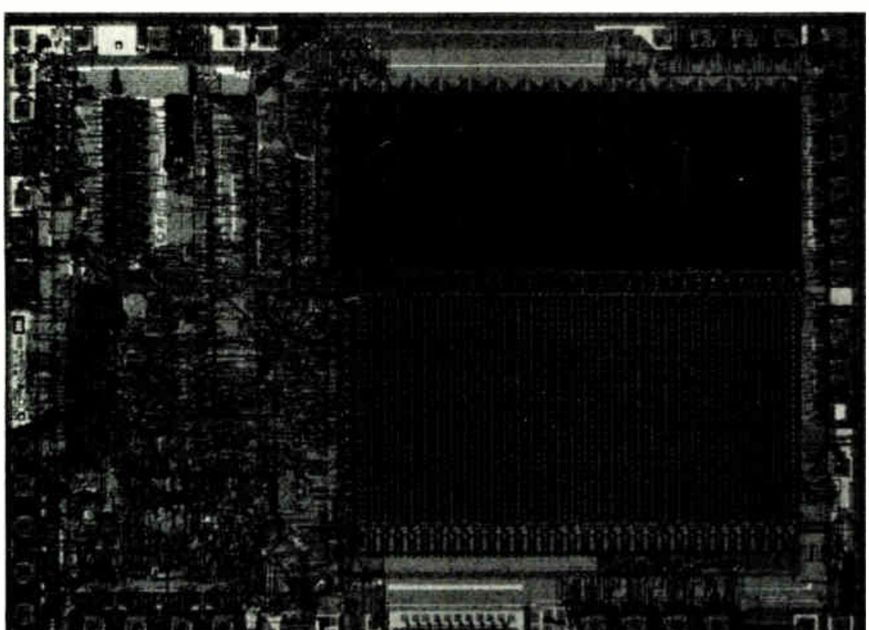
**The 8048 microcomputer** has been a favorite with designers for several years, ever since Intel Corp. introduced the 8-bit chip with 1-K byte of read-only memory. Now National Semiconductor Corp. has built a version with four times the program and data memory, which is bound to dramatically reduce systems costs.

With the INS 8050, which carries 4-K bytes of masked ROM and 256 bytes of random-access memory, "complex applications requiring large amounts of program space can now be implemented on a single chip," claims Tom Dugan, the firm's product marketing manager for single-chip microcomputers. For such jobs, users would previously have had either to use multichip processors or add external ROM, RAM, and latches to their one-chip system.

Fabricated with National's proprietary X-MOS technology—a scaled-down n-channel MOS process with single polysilicon loads and 3-μm spacing—the 8050 has a die 35% bigger than National's own 8048 design.

The 8050 is also a cost-effective alternative for multipattern 8048 users. It is possible, Dugan says, to put up to 10 8048 programs into one 8050, including routines for displays, keyboard controls, input/output, mathematics, and self-diagnosis. Thus when large production runs of the 8048 are not justified, the 8050 may be ordered in volume instead, and routines called up for specific market needs.

Many users have a lot of engineering time and money invested in 8048 software. Unlike Intel's recently introduced 8051, an extension of its MCS-48 family with 4-K bytes of ROM and 128 bytes of RAM, the 8050 does not require a separate converter to use 8048 assembly source code; it is both operating-code– and pin–compatible with the 8048. In-circuit emulation of the 8050 is available on National's Starplex development system.



The 8050's 8-bit central processor has an internal register and stack array, three programmable 8-bit I/O ports, eight control and timing lines, a programmable counter/timer, priority interrupt controls, and a system clock generator. It can operate as a byte processor or a binary or binary-coded decimal arithmetic processor, with RAM and ROM independently addressable and expandable.

The 8050 executes one of the 96 instructions in its set in 2.5 μs, typically, when operating at a 6-MHz clock rate. That is about half as fast as the 8051, which is tailored to higher-speed applications, executing most instructions in 1 μs when using a 12-MHz clock. However, National does plan to have an 11-MHz version of the 8050 available by year's end. Operating off a single 5-V power supply, total supply current of the 8050 is 75 mA maximum, 25 mA typical, at 6 MHz.

Available from stock to 30 days after receipt of order, the 8050 is priced at approximately $19 each in quantities of 1,000, packaged in a standard 40-pin dual in-line package. A version without ROM, designated the INS8040-6N, sells for $21.55 each in lots of 100. Both are available in ceramic packages for approximately $3 more each.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051 [338]

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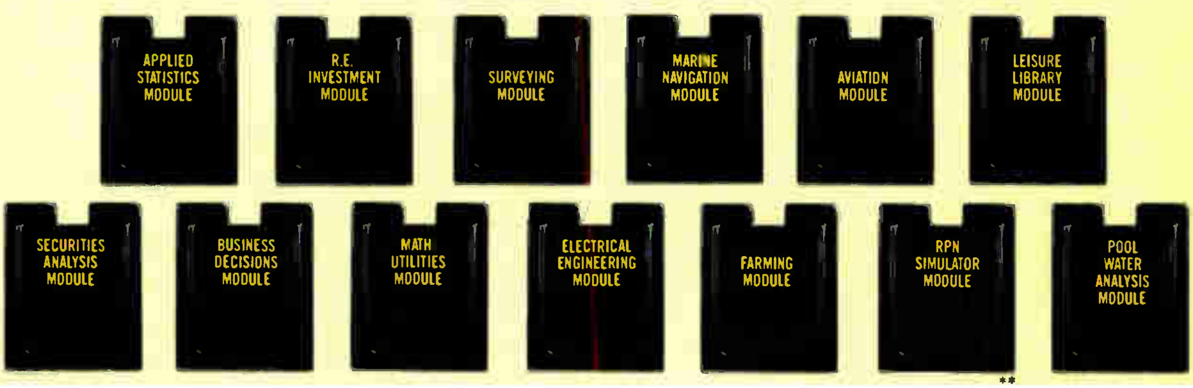


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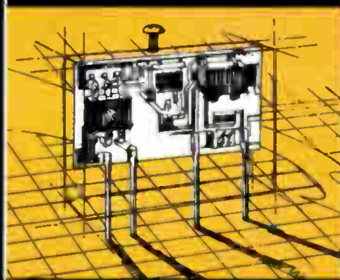

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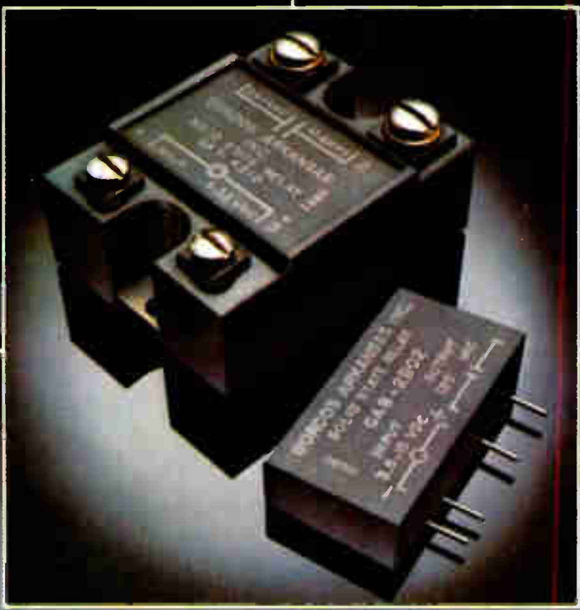

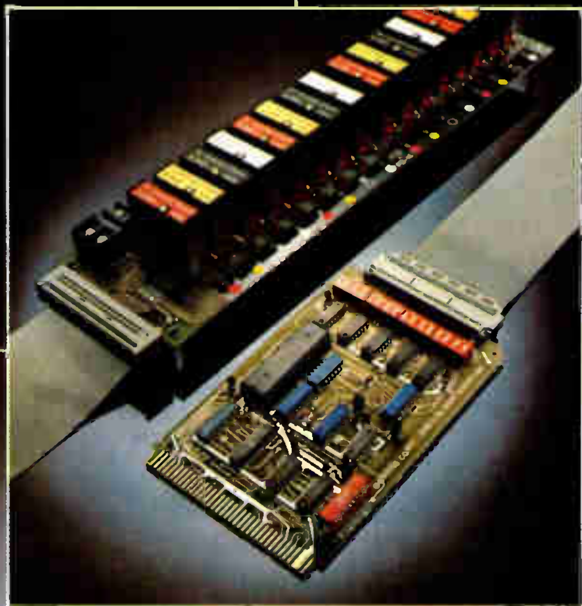

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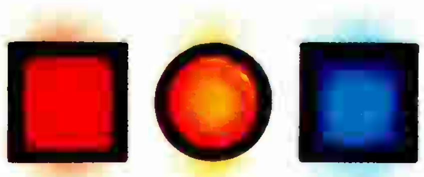

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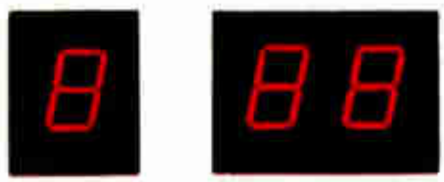

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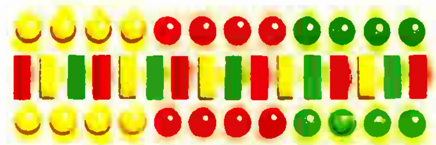

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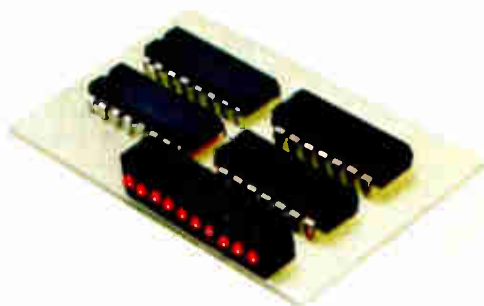

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# 16-K MOS ROM accesses in 80 ns

Read-only memories made with selective-oxidation process are as fast as bipolar PROMs but use less power

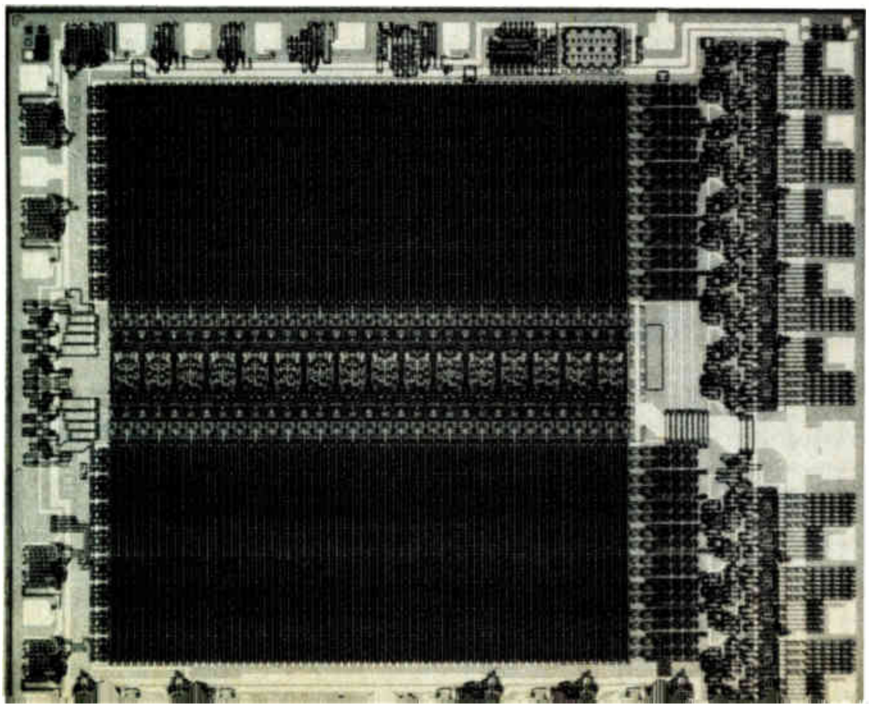
*by Bruce LeBoss, San Francisco regional bureau manager*

**Makers of** MOS random-access memory have been able to challenge the performance of their bipolar counterparts with high-performance MOS technology. Now Intersil is applying its H-MOS technology to read-only memories, reducing cell size and improving performance.

Two basic ROMs, available in 1-K-by-8-bit and 2-K-by-8-bit configurations and designated the 82HM-181 and 82HM191, respectively, are fabricated using the company's Selox selective-oxidation arsenic-diffusion process, which has a single layer of polysilicon and 3-$\mu$m geometries. With it, the company can "provide ROMs that operate at sub-100-ns access times, equivalent to that of industry-standard bipolar PROMs," while using "only 75% of the power," claims Bob Gardner, director of product marketing for large-scale integrated digital products.

Whereas the standard 82HM181 has an access time of 70 ns when operating off a 5-V ±5% power supply at 175 mA, the standard 82HM191 accesses in 80 ns maximum when operating at those voltage and current levels. Each of the 24-pin devices consumes a maximum of 965 mW. The inputs and three-state outputs of the ROMs are TTL-compatible and, Gardner notes, allow direct interfacing with common bus structures. Three chip-select inputs ease memory expansion.

Using the Selox process, Gardner claims, the MOS ROMs have a 50% smaller die area than their bipolar counterparts. The reduced size contributes to high-speed performance and results in "close to an order of magnitude improvement in yields." That is largely because the Selox H-MOS process reduces, by about one fourth, the number of mask steps used in producing bipolar programmable ROMs and, he adds, "because we are able to avoid the tough front-end [epitaxial growth] and back-end [metalization] problems normally associated with bipolar processing."



The yield improvements have led Intersil to offer the H-MOS ROMs at approximately 10% to 20% less than equivalent bipolar PROMs. For example, the 82HM181 and 82HM191 will be priced under $10 each and under $40 each, respectively, in lots of 10,000, when all are to be delivered over a 120-day period with at least 2,000 pieces per code mask.

However, "the total cost savings to the user will be on the order of 30%," Gardner says, because a PROM needs to be tested and programmed, among other things. With a ROM, "the user has got a finished part that's programmed, marked, and burned in where appropriate, ready to use in his equipment," he points out. In large-volume applications, for which the H-MOS ROMs are tailored, the user gets a part that "falls right into a bipolar socket." Faster turn-around times are possible when reordering ROM code.

Intersil also plans to offer an 82HM141, a 4-K (512-by-8-bit) version of the 82HM181. Eventually, it will also produce the 82HM185, a 2-K-by-4-bit ROM, and the 82HM-137, a 1-K-by-4-bit part as fallout from the 16-K ROM. Later, "we will produce 32-K [4-K-by-8-bit] and 64-K [8-K-by-8-bit] versions of those parts," says Gardner.

The availability of both the 82HM181 and 82HM191 is 8 weeks for prototypes, 16 weeks for production quantities, with reorders expected to slip to about 6 weeks by the second quarter of 1981.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [339]

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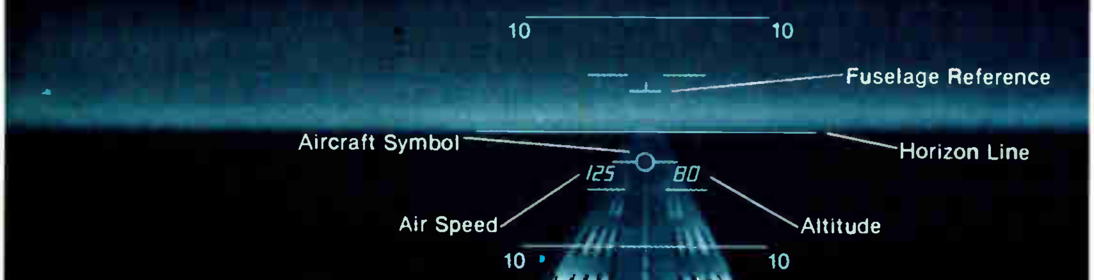


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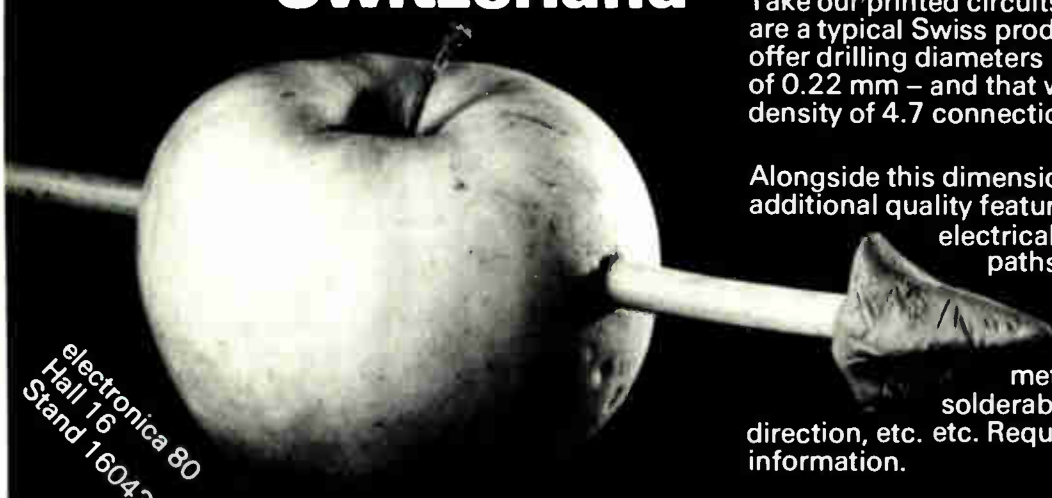


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Microcomputers & systems

# C-MOS 8048 uses 10 mA at 6 MHz

## Power-saving NEC version needs only 1 mA when halted, operates at −40° to +85°C

Although the chip remains essentially nonexistent, many circuit design engineers nonetheless know what an 80C48 is: a complementary-MOS version of the popular and widely sourced 8048 single-chip microcomputer. The designation is familiar because at least two U. S. semiconductor companies have promised C-MOS 8048s. But they have so far been unable to muster production volumes. Now Japan's Nippon Electric is crashing into that market with its μPD80C48, a part that it will ship in quantity by year's end.

Architecturally, the C-MOS counterpart is nearly identical to the original n-channel MOS microcomputer with its 8-bit central processing unit, 1-K byte of read-only memory, 64-byte random-access memory, and 27 input/output lines. Also like the n-channel device, the 80C48 features an internal timer/event counter, two interrupt modes, over 90 instructions, and bus compatibility with the wealth of peripheral chips that have been designed for the 8080 and 8085 microprocessors.

But, of course, the key difference here is power consumption. Of the three new high-performance MOS, or H-MOS, cousins of the 8048 recently introduced by the originator of the part, Intel Corp., the lowest-power version—the 8048L—draws an active current of 40 mA at 3 MHz and just 4 mA on standby—admirable for n-MOS.

However, NEC's chip draws a maximum of 10 mA at a full 6 MHz. Through an added halt instruction ($01_{16}$), this can be taken to 1 mA. "In addition, for further power conservation, there is a stop mode," beams Dwain Aidala, manager of the product at NEC Microcomputers Inc., the Wellesley, Mass., marketing and sales connection for NEC in the U. S.

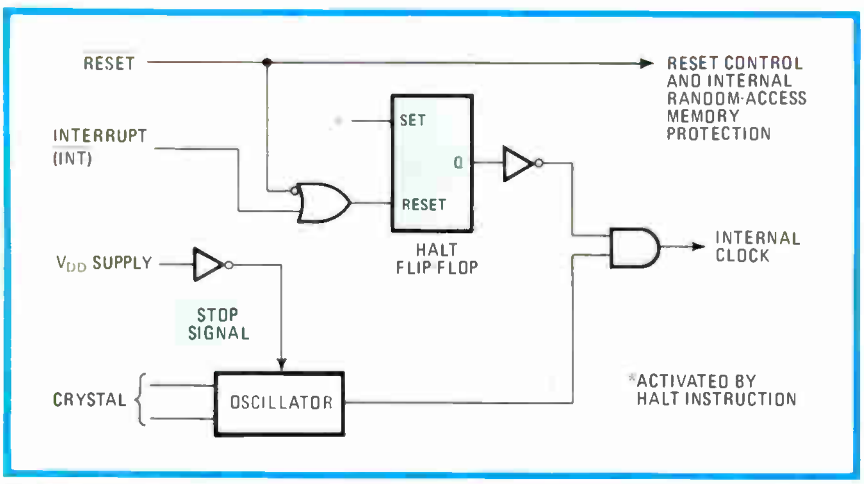
Upon reaching the halt instruction, the μPD80C48 keeps its on-chip oscillator running but denies clocking to internal logic. Either the interrupt or the reset pin on the 40-pin package can be lowered to bring the chip out of its halted state. The stop mode is initiated by reducing the supply voltage to the chip to about 2 V. This anesthetizes all but the RAM. Restoring 5 V on the supply pin will rouse the oscillator, and after a short stabilization period a reset will restart program execution at address zero. The block diagram depicts the standby control logic.

Besides being power-conscious, the C-MOS microcomputer offers other benefits. The clock can be slowed right down to dc, unlike the n-channel chip, which "will go down to a little under 1 MHz," Aidala comments. The 80C48 also operates at −40° to +85°C, compared with the 8048's 0° to 70°C.

Like the n-MOS 8048, the μPD-80C48 carries a ROM-masking fee. It is $1,000. For this reason, development versions of the chip have become important. So NEC will also produce, in C-MOS, the ROM-less version of the chip, the μPD80C35, and the erasable programmable ROM version, the 87C48, is also planned, says Aidala, adding that there is no reason why development cannot be done on an n-MOS 8035 or 8748.

Pricing is not yet firm, but Aidala expects the unit price to be below $20 in 1,000-piece lots. Orders will be taken in December for 12- to 14-week deliveries.

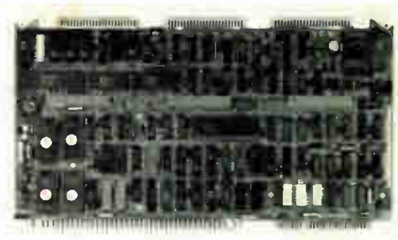
NEC Microcomputers Inc., 173 Worcester St., Wellesley, Mass. 02181. Phone (617) 237-1910 [371]




**Full stop.** In its halt mode, the 80C48's oscillator runs on, and the chip draws 1 mA. Dropping the supply to 2 V shuts down all but RAM, saving even more power.

## Industrial controller handles 16 control loops in 200 ms

The iSBC 88/40 measurement and control computer based on the 8088 16-bit microprocessor is Intel's first single-board computer designed for industrial and laboratory applications such as real-time process control, production monitoring, supervisory control, and data acquisition. The board can concurrently process and update 16 control loops in 200 ms using a traditional proportional-integral-derivative (PID) control algorithm. Analog input capability consists of 32 single-ended or 16 differential channels. In addition, the board has 24 programmable parallel



input/output lines.

The on-board dual port and 4-K bytes of static random-access memory, in conjunction with Multibus system bus-control logic, enable the iSBC 88/40 to function as a stand-alone, multimaster, or intelligent slave analog preprocessor. The board also has support for electrically erasable programmable read-only memory; sockets for up to 32-K bytes of E-PROM; and a 12-bit analog-to-digital converter that works at 20 kHz and has programmable gain and multiplexed inputs.

Intel will introduce the computer board at the Instrument Society of America's ISA/80 conference and exhibit, Oct. 20–23 in Houston, but the unit can be ordered now for deliveries starting in March 1981. From then on, it will be available from stock for the U.S. price of $2,000.

Intel Corp., 5200 N. E. Elam Young Pkwy., Hillsboro, Ore. 97123. Phone (503) 640-7147 [373]

## MC6809 processor rides the S-100 bus

The ADS 6809 S-100 single-board computer brings the capabilities of Motorola's MC6809 to the S-100 bus. The board features provisions for 2-K bytes of random-access memory; 4-, 8-, or 16-K bytes of erasable programmable read-only memory; RS-232 serial communications with switch-selectable transmission rates; parallel input/output ports; and simulated 8080-type I/O.

A monitor 2-K bytes in size called Adsmon allows the examination and modification of memory and registers, as well as the testing of memory, the calculation of relative offsets, and the setting and display of breakpoints. The ADS 6809 S-100 computer is sold as a silk-screened solder-masked printed-circuit board, with a comprehensive manual included. The price is $69.95, plus shipping.

Ackerman Digital Systems, 110 N. York Rd., Suite 208, Elmhurst, Ill. 60126. Phone (312) 530-8992 [374]

## Microprocessor supports 16 users on S-100 bus

The CSSN system 1000-MP is a multiprocessor microcomputer system that supports up to 16 users on an S-100 bus. It provides each user with an independent operating system to eliminate response degradation and to simplify debugging. The Z80A-based system is expanded by adding single cards that contain a processor, memory, and a dual-port memory window. Special cards for high-speed communications are also available.

The system 1000-MP supports up to four 8-in. Winchester hard disks with a maximum storage of 96

megabytes and with file backup on cartridge tape drives. The PDOS hard-disk operating system offers large-scale file management facilities and user and file security. PDOS is upward-compatible with CP/M 1.4 and can run a variety of industry-standard languages and applications. With four users and 24 megabytes of storage, the 1000-MP is priced at $25,000. It is available as a desktop or 19-in. rack-mounted model.

Computer Service Systems Network, 120 Boylston St., Boston, Mass. 02116. Phone (617) 482-2343 [376]

## 6800-based controller needs only power supply, terminal

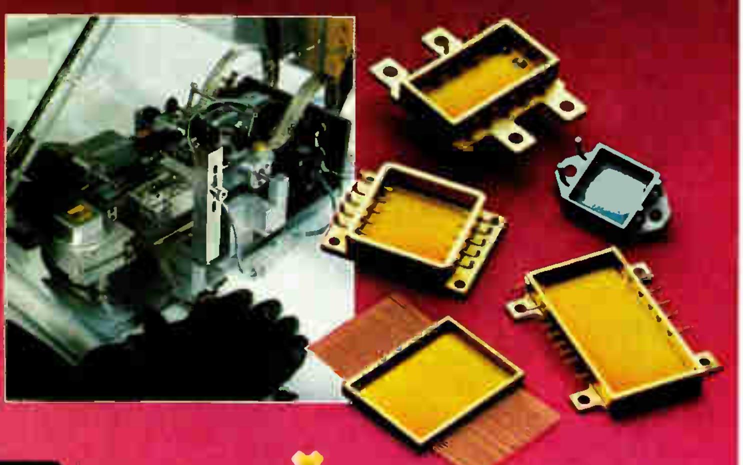
The applications controller series 12 single-board computer features the Motorola 6800 microprocessor family and requires only a power supply and terminal to operate. The ACS-

12-PRO provides two programmable 16-bit timers, software-controlled asynchronous communications interface adapter/modem interface on an RS-232 serial port, and two 8-bit or one 16-bit parallel port with handshake control.

The computer contains up to 4-K bytes of static random-access memory and 6-K bytes of programmable read-only memory. The ACS-12-PRO is supplied with 4-K-byte D-Forth software, a task-driven operating system that is a derivative of Forth. A 6-K-byte D-Forth version includes a 6800 assembler and a line editor. The 4.5-by-9.6-by-0.5-in. board's STD bus interface provides the user access to a large selection of input/output devices. With 1-K byte of static RAM, the 4-K-byte D-Forth, and a manual, the ACS-12-PRO lists at $495 from stock. The ACS-12-OEM lists at $395.

Datricon Corp., 7911 N. E. 33rd Dr., Suite 200, Portland, Ore. 97211. [377]







## Signetics' IFL family can be programmed in one step

By using the 950-0800 Logic Programming Pak, logic designers can prepare programming data for Signetics' 28-pin Integrated Fuse Logic (IFL) in a single step. The Pak is to be used in Data I/O's System 19 programmable read-only memory programmer. It accepts logic-variable data expressed as input- and output-state combinations. Integral software translates the data into the programming format for Signetics' IFL devices. The programming sequence, including a blank check, an illegal-bit check, and an array verification, takes from 3 to 15 seconds, depending on the device. Once a design is completed and tested, the

fuse-logic devices can be programmed using a master device or other memory as a data source.

The 950-0800 is priced at $1,050, with a delivery time of six weeks. Users of Data I/O's existing Signetics' IFL Programming Pak, the 919-1542, may add the new data-preparation capabilities by ordering an update kit, 960-0800, for $750. Delivery for the kit is seven to nine weeks.

Data I/O Corp., 1297 N. W. Mall, Issaquah, Wash. 98027. Phone (206) 455-3990 [378]

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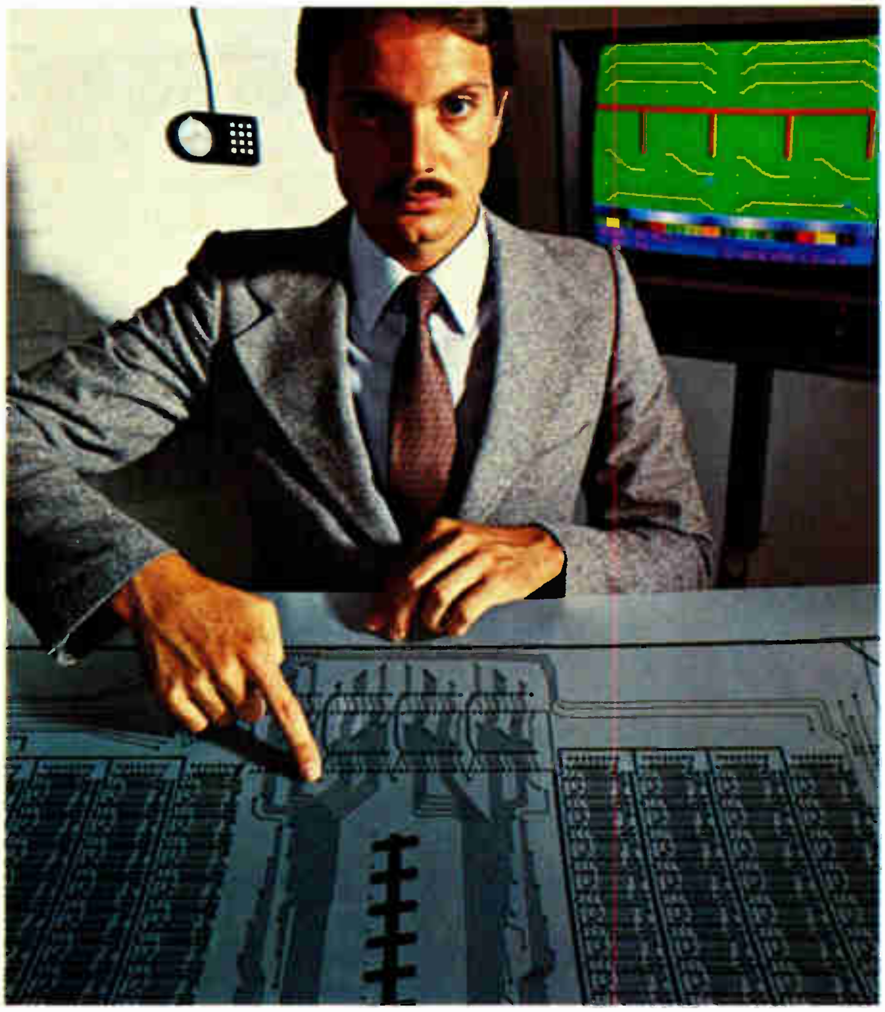

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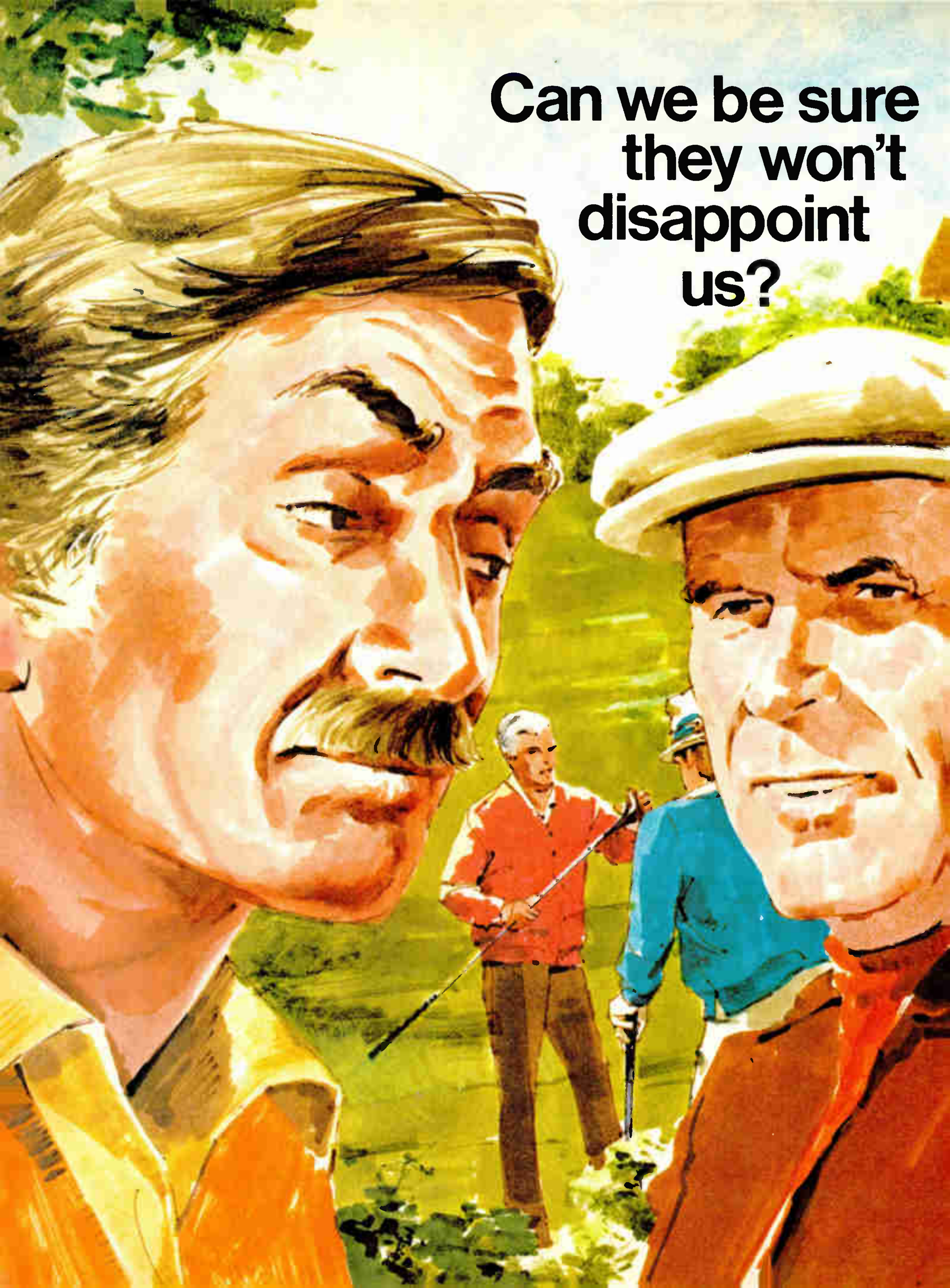
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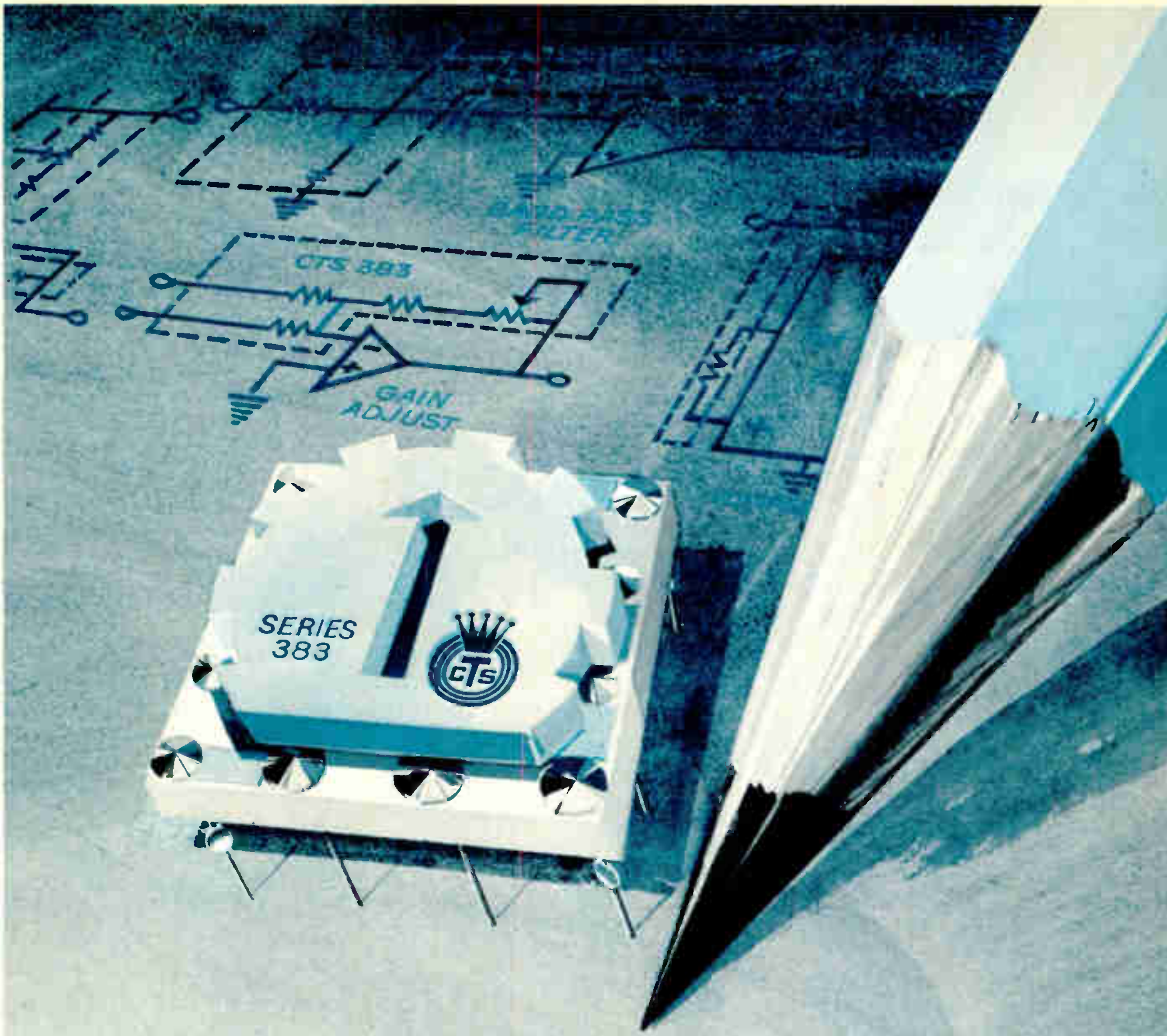
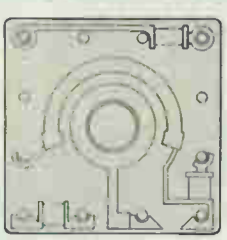



# Specifying both resistors and trimmers? Here's a single solution from CTS.



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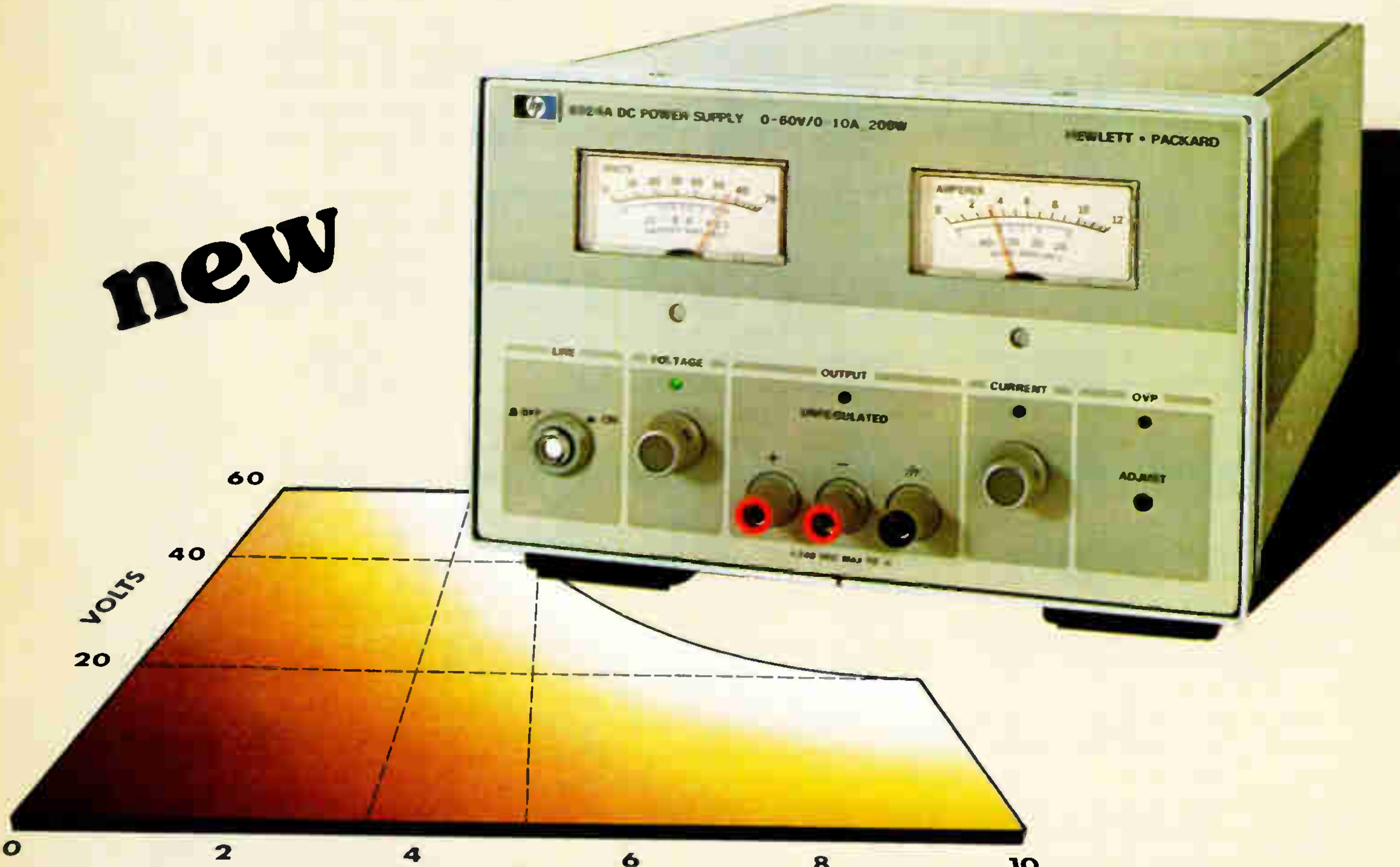


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## Small PROMs access in 45 ns

### 1-, 2-K bipolar PROMs have titanium-tungsten fuses; low-power parts are coming

At a time when manufacturers of bipolar programmable read-only memories are concentrating on supplying devices with 4,096 bits or more, at least one firm aims to quench the market's still considerable thirst for smaller PROMs—and with some performance improvements at that. Monolithic Memories Inc. is making available two families of bipolar PROMs with titanium-tungsten (TiW) fuses that access more quickly and dissipate less power than PROMs using nickel-chromium fuses.

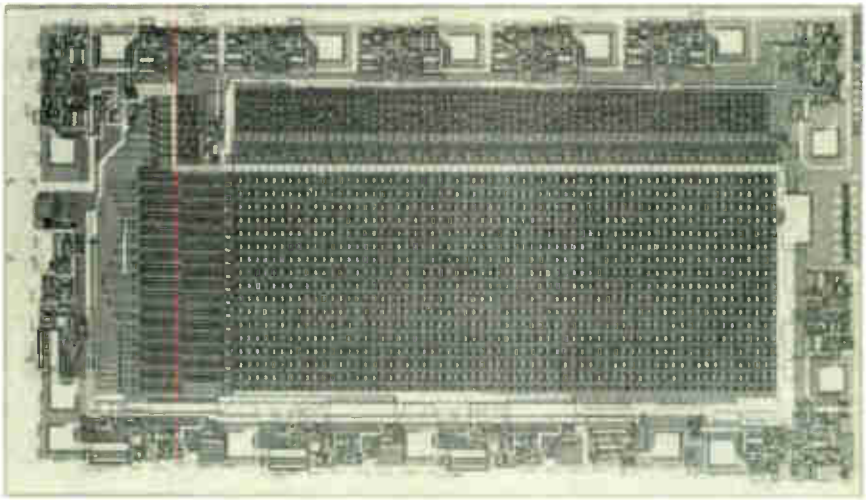
MMI's new Schottky (S) and low-power Schottky (LS) families are fabricated with a new platinum silicide process that, claims Shlomo Waser, manager of product planning and applications, "allows designs with the highest speeds over operating temperature ranges." The high-performance PROMs use a new programming technique that does not require a separate programming pin as in standard PROMs with NiCr fuses. The TiW fuses store a logical low and are programmed to the high state.

Initially available in 1-K (256-by-4-bit) and 2-K (512-by-4-bit) configurations, both the S and LS families have pnp inputs for low input current, full Schottky clamping, and three-state (suffix: 1) or open-collector (suffix: 0) outputs. Additionally, they are specified for operation over the commercial (prefix: 63) as well as the military (prefix: 53) temperature and voltage ranges. Thus, the two new families comprise a total of 16 devices.

**Real-time switching speed.** According to Waser, the S family of memory devices consumes the same amount of power (0.65 W) as do MMI's earlier NiCr-fused PROMs, but their 45-ns switching speed, he notes, represents a 25% speed improvement over the 60-ns rate of the older devices. Such switching speeds, he continues, are being demanded by "minicomputer manufacturers and some others who are building systems to perform real-time signal processing."

Furthermore, Waser points out that PROMs, if fast enough, can be used as programmable logic elements. "The majority of random logic can be replaced by PROMs if these devices are fairly fast. At 45-ns switching speeds, that becomes a viable approach."

In contrast, the LS family of devices maintains the 60-ns switching speeds of MMI's earlier PROMs with NiCr fuses, but they "nearly



halve power consumption" (0.35 W compared with 0.65 W) of the older devices. "The need for such low-power PROMs," Waser says, "is basically in two market areas: the telecommunications industry, which normally doesn't push speed to extremes; and the military, which needs low power for airborne systems," among other applications.

Waser expects the new devices to alleviate what he calls a worldwide shortage of bipolar PROMs. Furthermore, because of the limited capacity to make such devices, he adds, many companies have stopped supplying smaller PROMs and instead are manufacturing 4-K and larger PROMs, with the 8-K bipolar PROM being the most popular at present. Thus, those bipolar PROM users that have designed smaller PROMs into their systems, Waser says, "are having difficulty in getting them."

Pin-compatible with standard Schottky PROMs, the new 16-pin devices from MMI will cost more. For example, the 63S140/1 commercial 1-K PROM will be priced at $5 each in lots of 100, whereas their counterparts with NiCr fuses are priced at $3.50 each in like quantities. Similarly, the 63S240/1 commercial 2-K device will be priced at $7.50 each, as compared with $5.83 each for 2-K NiCr PROMs in the same quantities. The LS family of bipolar PROMs will be priced "slightly higher" than the S series.

Small quantities of the S family are available off the shelf from distributors; large quantities (up to 5,000) are delivered 12 weeks after receipt of order. The LS family will be available by the end of this year.

Monolithic Memories Inc., 1165 E. Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 739-3535 [411]



## TI 92-K bubble memory system and kit available

Texas Instruments has two new 92-K single-board magnetic-bubble memory systems that are compatible with the STD bus—the TBB7090 and TBB7091. In addition, the company is offering two kits—the TIBK090 and TIBK091—for engineers who prefer to do their own board layout.

The TIBK091 kit contains the parts required to construct one minimum memory system and consists of one 92-K bubble memory, a sense amplifier, two coil drivers, a function driver, two diode arrays, one thermistor, one function-timing generator, and one controller. It sells for $191. The 090 kit contains all these parts except for the function-timing generator and controller. It sells for $151.

The completely assembled and tested single-board memories—TBB7090 and 7091—are supplied with one, two, three, or four 92-K

TIB0203 bubble memories for 11.5, 23, 34.5, or 46 kilobytes of storage. The 7090 contains 11.5 kilobytes of nonvolatile memory storage and all the necessary support circuits. The 7091 is designed to expand the storage capacity of the 7090 to a maximum of 104 kilobytes. Each 7091 contains up to 46 kilobytes of memory. Both boards are compatible with such microprocessors as the 8085, 6800, and Z80. They are available in two temperature ranges: from 0° to 50°C, and from 0° to 70°C. Depending on memory capacity and temperature range, they sell for $610 to $1,580 and are available within four weeks after receipt of order.

Texas Instruments Inc., P. O. Box 225012, M/S 308, Dallas, Texas 75262 [413]

## 2-K C-MOS E-PROM dissipates 20 mW

The CDP18U42C complementary-MOS 2-K (256-by-8-bit) erasable programmable read-only memory is erased with ultraviolet light (2,500 Å typical). The E-PROM is useful for asynchronous ROM applications and will interface directly with the CDP1802 microprocessor. It has common data inputs and outputs and utilizes a single 4- to 6.5-V supply during read operations. Three chip-select inputs are provided. Access time is a maximum of 1 $\mu$s and programming usually takes 5 seconds. The E-PROM dissipates 20 mW typically during read operations. It comes in a 24-lead hermetically sealed dual in-line ceramic package and sells for $38.70 apiece in 100-unit lots. It is available from stock.

RCA Solid State Div., Box 3200, Somerville, N. J. 08876 [414]

## Real-time clocks are Microbus-compatible

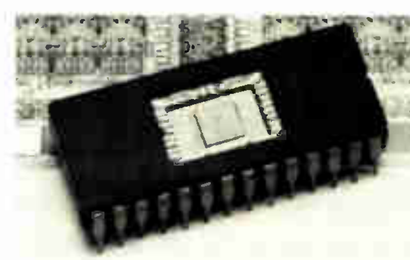
Designed with a bidirectional data bus in order to facilitate interfacing with microprocessor systems, the MM58167 and MM58174 real-time clocks are Microbus-compatible. Both devices feature addressable real-time counters. The 174 measures from tenths of seconds through months and includes a write-only register for leap year calculation; the 167 measures thousandths of seconds through months and has corresponding addressable latches for alarm functions. Each counter and latch is divided into 4-bit words. The two chips' time bases are generated with 32,768-Hz crystal-controlled oscillators. The model MM58174 is housed in a 16-pin dual in-line package and is priced at $8.50 in quantities of 100. The MM58167 comes in a 24-pin DIP and is priced at $9.25 in the same quantities. Both devices are currently available from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [415]

## 250-ns 64-K E-PROM comes in Jedec-approved 28-pin DIP

The Intel 2764 64-K erasable programmable read-only memory with a 250-ns worst-case access time conforms to the new industry standard for high-density byte-wide memories. The E-PROM's 28-pin configuration matches the one recently approved by the JC-42 MOS memory standardization committee of the Joint Electron Device Engineering Council. This format permits two-line control to assure proper system operation at high speed. It can be used as a universal pinout for all byte-wide memories, including ROMs, E-PROMs, and random-access memories of 2-, 4-, 8-, 16-, and 32-K size to be interchanged in the same 28-pin socket.

Intel claims that by applying its HMOS-E process technology to nonvolatile memories it has made the 32,400-mil$^2$ 2764 the smallest 64-K E-PROM currently in production. The process has 3-$\mu$m channel lengths. The 2764's speed eliminates the need for wait states in a central processing unit's program, so the CPU's performance is maximized, the company points out. Faster and slower versions, the 2764-2 and -3, are available with worst-case access times of 200 and 300 ns. The U.S. price for the 2764 is \$163 each for 100-piece purchases. Volume shipments will begin in the first quarter of 1981.



Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051. Phone (408) 987-6742 [417]

# New iSBX™ Multimodule™ boards

## Intel® introduces a whole new dimension in configuring single board computer systems.

Intel pioneered the concept of flexible microcomputer *system* design in 1976, with our family of iSBC™ single-board computers interfaced via the Multibus™ system bus—presently accepted as the industry standard.

Now we've extended this well-accepted concept to *board*-level design: A new generation of Multimodule boards interface to iSBCs via the new iSBX bus. So now you have a second design option. You can expand systems in large increments with Multibus boards. Or in smaller, more economical increments with Multimodules.

### The key to configuration flexibility

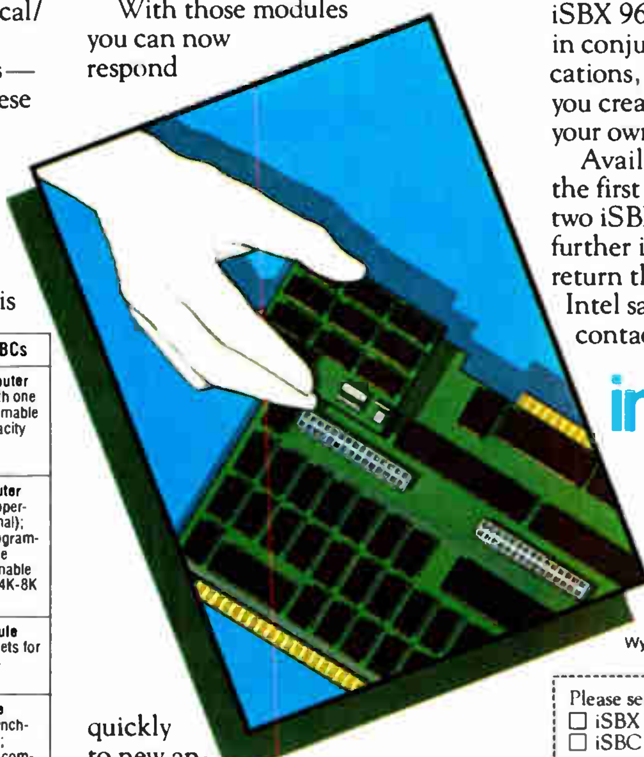
The iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems—assures compatibility between these systems and the emerging Multimodule product line.

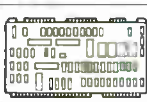
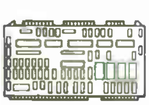
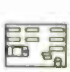
Present on all future Intel single-board computers, the iSBX bus saves design time and space, and facilitates fast, easy upgrading. System performance is also improved because Multimodules tie directly to the iSBC internal bus. Connection to the iSBX bus is made with a set of rugged connectors—one on the iSBC board, the other on the Multimodule itself.

### The new Multimodule family

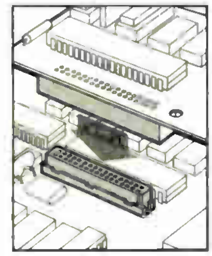
Multimodules represent a whole new family of plug-in expansion boards. They allow you to add a variety of special performance features to your existing iSBC system. Currently available add-ons are shown below. Soon you'll also be able to add other Multimodules for D-to-A and A-to-D conversion, communications, peripheral interfaces—and more.

With those modules you can now respond quickly to new applications opportunities. Examples? Take data acquisition or industrial control: to add extensive I/O processing power, you simply plug in the iSBX 350 board. Or consider communications networks. Now there's no need to add entire USART boards; just use the iSBX 351 unit. In laboratory control applications, instead of an independent math processor, now you can choose the more economical iSBX 331 or 332 math modules.



| New Multimodules and iSBX Bus-compatible iSBCs | |
|---|---|
|  | **iSBC 80/10B Single Board Computer** 8080A-based microcomputer with one iSBX bus connector; 48 programmable I/O lines; one USART; timer; capacity for 1K-4K bytes RAM; up to 16K EPROM |
|  | **iSBC 80/24 Single Board Computer** 8085A-2 based microcomputer operating at 4.8 MHz (2.4 MHz optional); two iSBX bus connectors; 48 programmable I/O lines; one USART; three programmable timers; programmable interrupt controller; capacity for 4K-8K bytes RAM; up to 16K EPROM |
|  | **iSBX 350 Parallel I/O Multimodule** 24 programmable I/O lines; sockets for inverting and noninverting transceivers |
|  | **iSBX 351 Serial I/O Multimodule** Programmable synchronous/asynchronous communications channel; standard RS232C or RS449/422 compatibility; software-selectable baud-rate generation; two programmable 16-bit BCD or binary timers/event counters |
|  | **iSBX 331 Fixed/Floating Point Math Multimodule** Fixed point single- (16-bit) and double- (32-bit) precision arithmetic; floating point single- (32-bit) precision functions; floating-to-fixed and fixed-to-floating point conversions; transcendental functions |
|  | **iSBX 332 Floating Point Math Multimodule** Single- (32-bit) and double- (64-bit) precision arithmetic; compatible with proposed IEEE format and existing Intel floating point standard. |

### New Multimodule-compatible iSBC boards



iSBX 960-5 Connector

Intel's new 8-bit iSBC 80/10B and 80/24 single-board computers are the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved versions of widely used iSBC boards. (See table).

### Custom tailoring, too

For users who want to design their own Multimodule boards, Intel offers iSBX 960-5 connectors. When used in conjunction with the iSBX specifications, this set of connectors lets you create modular boards that meet your own unique requirements.

Available from Intel today are the first four iSBX Multimodules and two iSBX-compatible iSBCs. For further information, or to order, return this coupon or call your local Intel sales office or distributor. Or contact Intel at the address below.

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Please send information on:
☐ iSBX Multimodules ☐ iSBC 80/10B
☐ iSBC 80/24 ☐ Configuration Guide
☐ Other ______
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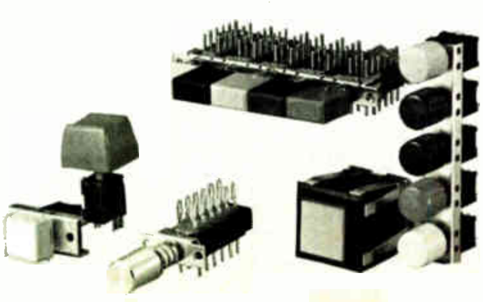
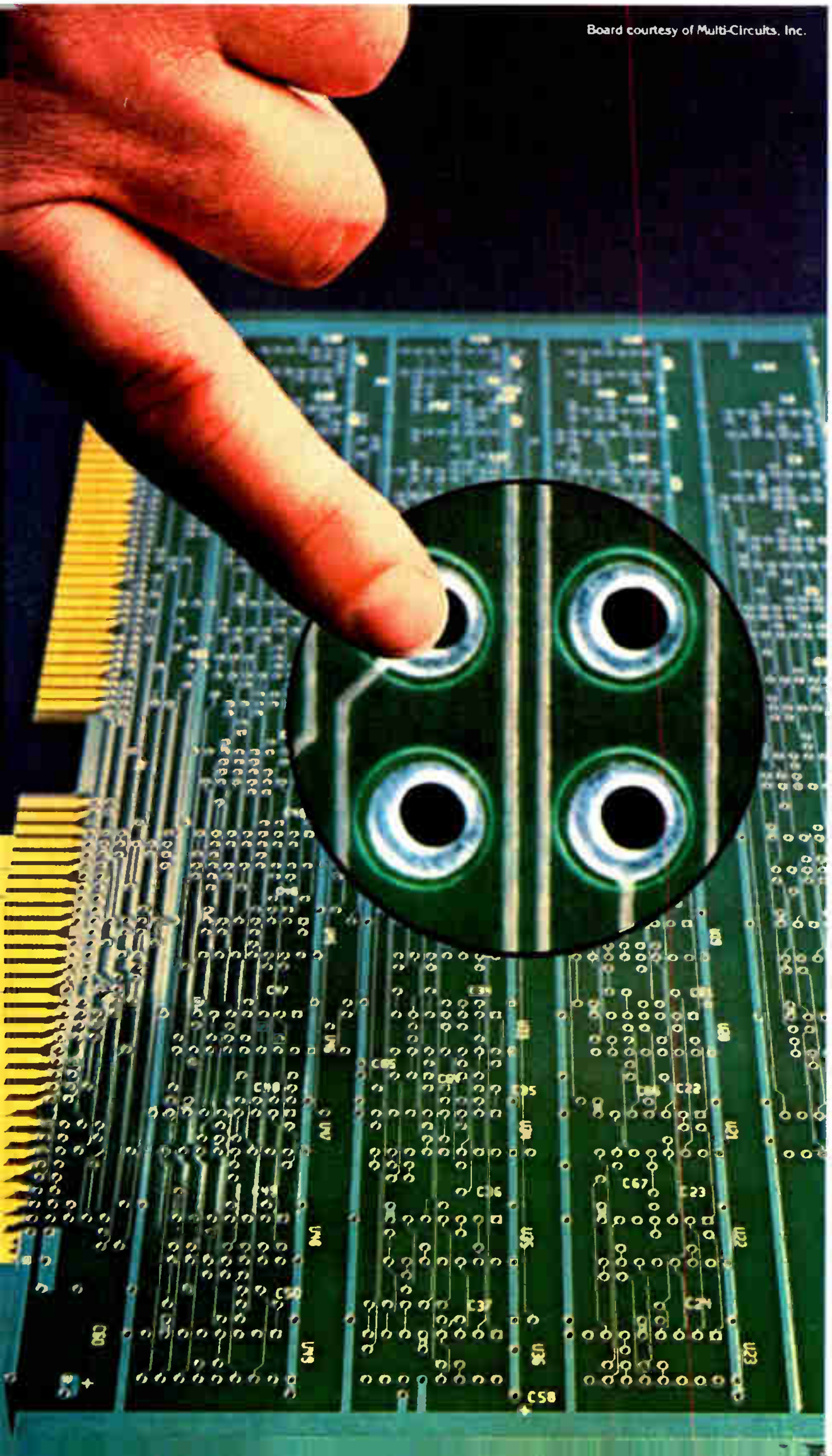


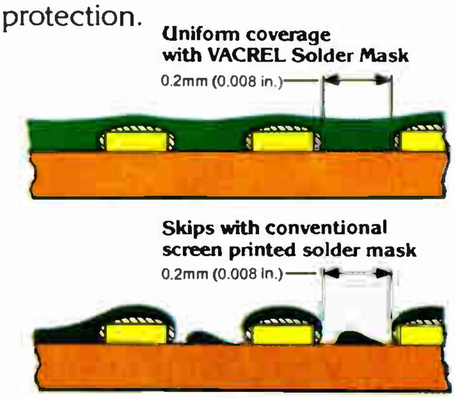
# When you design circuitry this tight, you need the protection of VACREL™.

DRY FILM SOLDER MASK




Fine line printed circuit board designs call for tight conductor spacing. And with spacing tolerances of less than 0.3mm (0.012 inch), you need circuitry protection beyond the capability of ordinary screen printed solder mask. You need VACREL dry film solder mask.

In the cross sectional illustration below, VACREL uniformly covers the circuitry with no skips. It provides *maximum protection* of fine line circuitry, even below 0.2mm (0.008 inch) conductor spacings, resulting in electrical, environmental and mechanical protection.




Conventional screen printed solder mask has limited utility in the protection of fine line circuitry.

Interested? Ask us to show you how VACREL dry film solder mask can protect your tightest circuitry designs. Write: VACREL Solder Mask, RISTON® Products, DuPont Company, Rm. 38014, Wilmington, DE 19898.

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Circle 227 on reader service card

Data acquisition

## 18-bit d-a unit contains reference

### Hybrid converter also includes op amp, latches, as do low-cost 16-bit parts

Only 18 months ago, Hybrid Systems introduced its first 18-bit digital-to-analog converter, the DAC 374-18, packaged in a dual-width, 32-pin dual in-line package [*Electronics*, April 26, 1979, p. 180]. Claimed at the time to be the first hybrid of this resolution in such a small package, the DAC 374-18 has since been followed by units with fewer parts and improved price-performance ratios.

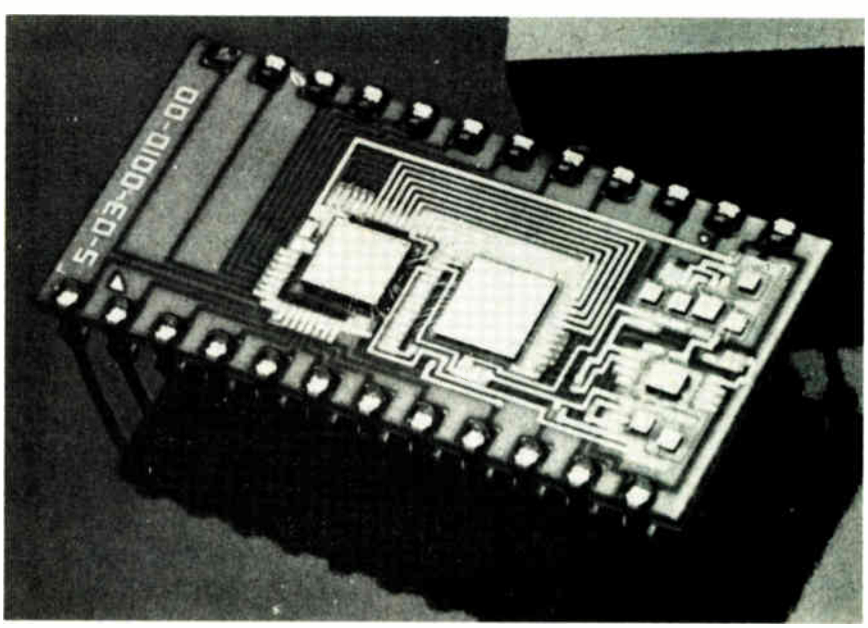
Now the firm is introducing two more converters, the 18-bit DAC 377-18 in a 28-pin hermetic package suitable for military environments, and the DAC 9377-16 (shown in photo), a 16-bit unit in a low-cost 24-pin package aimed at commercial sockets; they are available from stock. Both are equipped with an operational amplifier for voltage-output applications; both contain a variable-feedback 10-V reference with a 5-ppm/°C temperature coefficient; and both have latches, or input registers, for interfacing with mini- or micro-computers.

Both converters use the large-scale integrated converter circuit introduced in the DAC 370-18 [*Electronics*, March 27, p. 199]. This complementary-MOS chip contains all converter electronics except a laser-trimmed resistor network, voltage reference, and operational amplifiers. Thus the parts count has dropped to about a quarter that of the DAC 374-18.

**Analog LSI.** The chip contains 29 tightly matched dual field-effect-transistor switches, 29 latches and drivers, 18 exclusive-OR gates, 16 decoders, and temperature-compensating electronics. All this packed into a single chip adds up to low price: for example, the DAC 9377-16, in 100-unit lots, costs $65.

Much of this low price is due to Hybrid's proprietary glass-filled epoxy package, said to save the firm up to 95% of the cost of other commercial packages. The level of monotonicity achieved also affects the price: the $65 figure applies to units with 14-bit monotonicity. Units with 15-bit monotonicity go for $94 in the same quantities, while 16-bit monotonic units cost $129 in hundreds.

DAC 377-18s are monotonic to 16 bits and are offered in two price and

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Circle 229 on reader service card

temperature ranges. For units operating over the 0°-to-80°C range, the 100-unit price is $199, $11 less than Hybrid's own six-month-old DAC 370-18, a current-output device with no voltage reference. For the −55°-to-+125°C military temperature range, the 377-18 sells for $520 in hundreds. Much of the difference results from manufacturing to MIL-STD-883 reliability specifications and from the cost of documentation.

Both the 9377-16 and the 377-18 are expected to sell for so-called insurance applications: the 9377-16 to users who need a dependable 12 or 14 bits of resolution and the 377-18 to those needing a sure-fire 16 bits. User plans already are said to include high-resolution radar, sonar, and automatic-testing applications.

Both units accept either binary or offset-binary inputs and are compatible with diode-transistor-logic, TTL, and complementary-MOS. Input leakage current is rated at about 1 μA maximum. Output is 0 to 10 V with current compliance of ±5 mA and output impedance less than 1 Ω.

Relative to full scale, the scale factor is 0.1% and initial offset is ±0.05%. Integral linearity for 377-18 and for the 16-bit-monotonic version of the 9377-16 is to within ±0.0008%. Differential linearity typically is about half that figure.

Major-transition settling time (to 0.006% of full scale) is 20 μs—faster than for most 16-bit converters and quite respectable for a voltage-output device. Power-supply requirements are a standard ±15 V dc ±5%. Power dissipation varies with model from a typical figure of 400 mW to a maximum of 500 mW, with most power going to the reference and output operational amplifier.

Hybrid Systems Corp., Crosby Dr., Bedford, Mass. 01730. Phone (617) 275-1570 [381]

## 16-bit a-d unit digitizes analog signal in 2 μs

The ADC-1600 16-bit analog-to-digital converter will digitize an analog input signal in a maximum of 2 μs. The converter can be configured

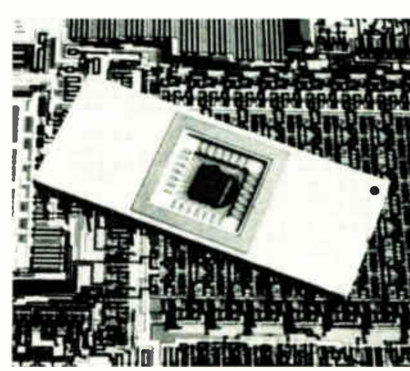
## New products

with either single-ended or differential inputs in its basic form, offering conversion times of 2 or 4 μs. It comes with sample and hold inputs, and options include either a 2- or a 5-μs sample-and-hold in a single-ended input configuration. Temperature coefficients are ±7 ppm/°C and maximum nonlinearity error is ±½ least significant bit. All inputs are diode-transistor-logic– and TTL–compatible. In quantities of one to nine, the ADC-1600 is priced from $2,050; delivery is from stock to 12 weeks.

Intech Function Modules, 282 Brokaw Rd., Santa Clara, Calif. 95050. Phone (408) 727-0500 [383]

### Monolithic data-acquisition system includes RAM on chip

A monolithic data-acquisition system includes on-chip random-access memory. The AD7581 contains an 8-bit successive-approximation analog-to-digital converter, an eight-channel multiplexer, an 8-by-8-bit dual-port RAM with address latches,



# Cost Effective Systems for the Microcomputer OEM.

Ohio Scientific has been building small business microcomputers and personal computers since the beginning of the microcomputer revolution. Most Ohio Scientific products incorporate a bus architecture utilizing modular circuit cards mated to a multi-slot backplane. Ohio Scientific's 48 signal line bus is designed to effectively marry the versatility and modularity of bus architecture with the economies of consumer products producing an ultra-low cost yet reliable system. Many industrial users of microcomputers recognize the economy and versatility of Ohio Scientific's modular computer boards and utilize these boards and subsystems as well as customers who purchase complete computer systems on an OEM basis.

### Ohio Scientific's New OEM Program

Ohio Scientific now recognizes the importance of the OEM marketplace and is introducing a complete program for the board level OEM user as well as the system OEM. The program starts with our standard products including three CPU boards, a broad range of static and dynamic memory boards, mini and 8″ floppy disk controllers, printer controllers, multiple RS-232 port boards, a hard disk controller, and video interface with optional keyboard. Backplanes with two, four, eight or sixteen slots are available. These standard products are now being supplemented by a broad range of products specifically for the OEM user including:

- New universal telephone interface board which has auto-dial capability, auto-answer capability, tone encoding and decoding, answer and originate 300 baud modem and voice I/O via tape recorder or optional phonetic voice output system.
- New calendar-clock with several month battery backup capability which can be programmed to automatically restart the computer or shut off the computer at set times. The circuit board also includes automatic power-fail restart capability.
- Instrumentation quality high speed, 12-bit analog A/D – D/A module with a 16-channel input multiplexer and two 12-bit D/A converters.
- A large range of parallel interface options including circuit cards containing 48 parallel I/O lines.
- New solderless prototyping board which connects to the computer system and allows rapid prototyping of new interface ideas.
- System PROM blaster which accepts 8K through 64K bit industry standard EPROMS and a universal EPROM-ROM card.
- A card edge extender, bus analyzer and bus compatible breadboards.

### Documentation

All of Ohio Scientific major circuit boards are now fully documented by Howard Sams (the originator of the Sams Photofact series for Consumer Electronics) servicing manuals which include block diagrams, schematics, detailed pictorials, parts placement diagrams and parts lists providing the designer, systems integrater and serviceman with detailed hardware information. Ohio Scientific is offering qualified OEM users its principal disk operating system (OS-63D V3.2) which supports multiple languages, mini-floppies, 8″ floppies, printers, modems and other accessories in documented Source Code and machine readable form which can be reassembled on standard OSI computers. This gives the product developer the ultimate flexibility in integrating these components into his total system design.

### Best of all is the Price

Because of Ohio Scientific's hundreds of thousands of boards per year volume for the consumer and small business market, these products cost a mere fraction of the corresponding LSI-11, SBC or S-100 bus boards. This economy allows you to utilize a floppy subsystem in your product at a total cost typically less than an EPROM based system from other vendors.

Ohio Scientific's reasonably priced universal telephone interface and voice output capabilities allow you to integrate advanced telecommunications, remote control capabilities and/or unlimited vocabulary voice response in your systems at the same price as a "bare bones" implementation with other bus architectures.

### Easy to Start With

Getting started with the OSI bus architecture is now easy with documentation, off the shelf availability, and economical computer systems for in-house software development using Assembler, BASIC FORTRAN or PASCAL. Ohio Scientific's new OEM contract provides easy to start with terms and generous volume discounts.

**For more information and the name and phone number of your local Ohio Scientific OEM representative call 1-800-321-6850 toll free. Please specify your interest as an OEM user.**

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Circle 233 on reader service card

## New products

control logic, comparator, and three-state buffers. The system connects directly to the 8080, 8085, Z80, 6800, and other microprocessors; the converter is transparent to them. Input channels are scanned sequentially and continuously, averaging 680 $\mu$s for eight channels. On-chip logic provides interleaved direct memory access.

Six versions are available, all in 28-pin dual in-line packages: the JN, KN, and LN grades are specified for the 0°-to-70°C temperature range and come in a plastic DIP; AD, BD, and CD grades are specified for the −25°-to-85°C range and are housed in a ceramic DIP. Differential nonlinearity is ±¾, ±⅞, and ±1⅞ least significant bit maximum over the specified temperature ranges for LN and CD, KN and BD, and JN and AD versions, respectively. Relative accuracy is to within ±½, ±¾, and ±1⅞ LSB maximum within given temperature ranges. The AD7581 sells for $13.90 in 100s and large quantities can be delivered 90 days after an order is received.

Analog Devices Semiconductor, 804 Woburn St., Wilmington, Mass. 01887. Phone (617) 935-5565 [385]

### 15-bit sample-and-hold has 300-ps aperture uncertainty

The model 1569 is a digital gain-controlled differential-input sample-and-hold amplifier suitable for up to 15 bits of resolution. Really two separate differential sample-and-hold amplifiers contained on one printed-circuit board, it exhibits low offset and drift characteristics in both sample and hold modes. Its low aperture uncertainty time of less than 300 ps permits the acquiring of analog data containing high frequencies while the unit maintains high accuracy. The model 1569 has been designed for installation into the TEC A/D x-1500 Data System and is available from stock. The fixed-gain model is priced at $200 per unit and the programmable-gain version at $250.

Tustin Electronics Co., 1431 E. St. Andrews Place, Santa Ana, Calif. 92705 [384]

  


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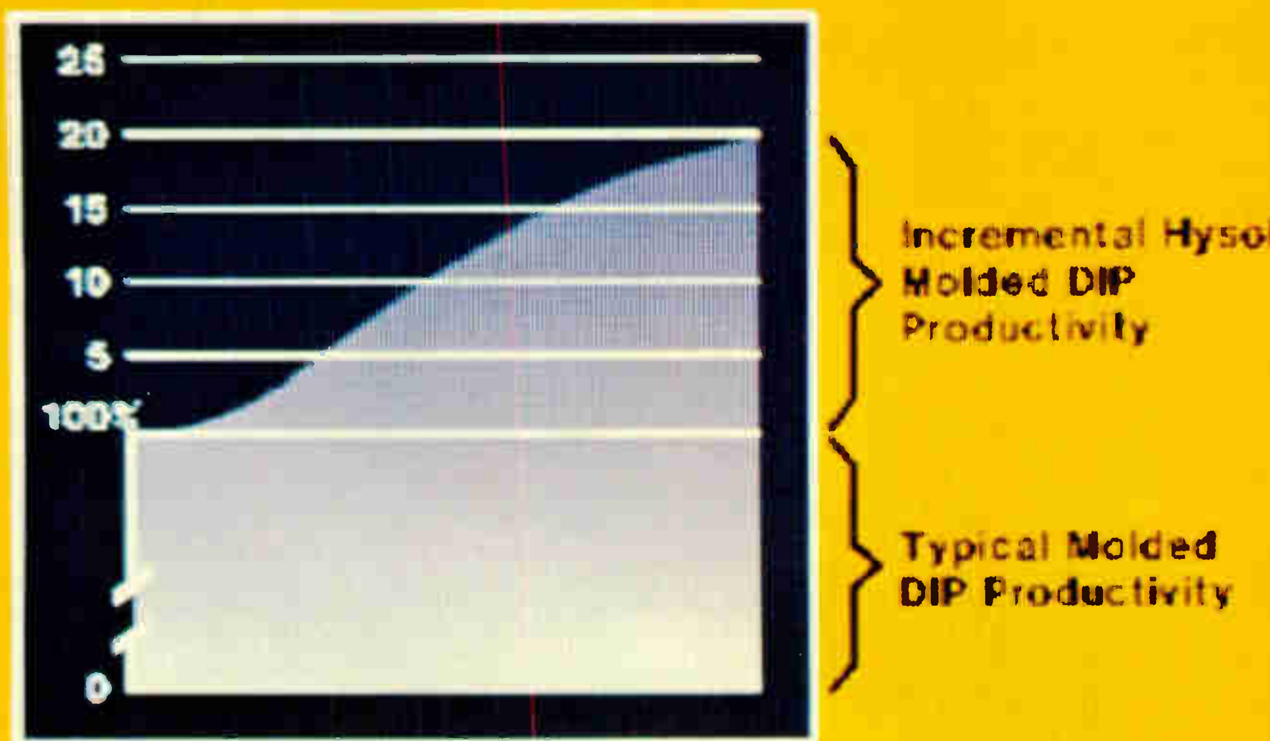


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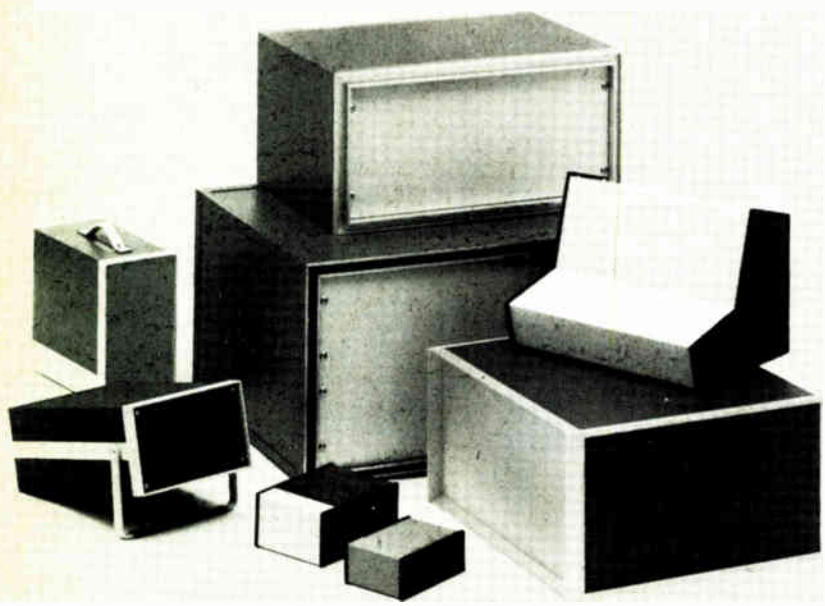

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*St. Louis Arch in background. "The Gateway to the West."

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Materials

# Chip-processing chemicals become 1,000 times purer

The materials used in making semiconductors, especially fine-line large- and very large-scale integrated circuits, must be kept fanatically clean. Allied Chemical's new line of chemicals caters to that need. The Particu-lo low–particle-grade, low-mobile-ion processing chemicals are filtered and packaged to deliver a purity 1,000 to 10,000 times greater than that of products currently on the market. They are virtually free from many of the particles found in other low-mobile-ion–grade processing chemicals and are already in use in the fabrication of devices with 2-$\mu$m geometries, reports Gary J. Clancy, manager of marketing for electronic chemicals in Morristown, N. J.

A 30% hydrogen peroxide solution will typically have about 8.3 million 1-$\mu$m or larger particles per liter if it is classified as a low-grade, low-mobile-ion substance. The same chemical when processed to Allied's Particu-lo standards will contain only 10,000 particles/l maximum, 5,000 typically.

The line runs the gamut of processing chemicals for etching and cleaning and includes sulfuric acid, hydrogen peroxide, and isopropyl alcohol, as well as a variety of stripping solutions. Altogether nearly 30 chemicals are being offered. "Any product that would be used in a semiconductor processing line is available in the Particu-lo line, with the exception of photoresists," notes Clancy.

The chemicals may be completely substituted for any products now being used, according to Clancy, with no changes needed in the manufacturing process. "We recommend that tanks and process vessels be kept as clean as the wafers are kept, however," he advises. The products are available in 2.2-l glass bottles, 3.8-l amber glass bottles, and 3.8-l polyethylene bottles, depending on the particular chemical. The bottling is done in a controlled, clean atmosphere, and each filled container is wrapped in two plastic bags to protect its exterior.

Clancy estimates that the Particu-lo products sell, on average, for about three times the price of low–mobile-ion-grade chemicals. For example, sulfuric acid now sells for about $5 per 2.2-l bottle, whereas the Particu-lo product will sell for about $19 for the same size bottle. A 3.8-l bottle of isopropyl alchohol sells for about $5 now, and the Particu-lo product will sell for about $16. He notes that for most semiconductor manufacturers, a yield increase of up to 10% will often offset this additional expense.

Particu-lo products are now available in sample quantities for production use.

Allied Chemical Corp., Chemicals Co., P. O. Box 1139R, Morristown, N. J. 07960 [476]

## Thick-film resistor material ranges to 1 MΩ per square

The 1800 series of thick-film resistor compositions developed for potentiometers and trimmers includes eight members, ranging in value from 1.5 Ω per square to 1 MΩ/sq. The Birox 1800 materials exhibit low contact resistance variation even in the low-resistivity compositions. The temperature coefficient ratio for the 1-kΩ/sq

through 1-MΩ/sq materials is ±50 ppm.

Du Pont Co., Electronic Materials Division, Wilmington, Del. 19898. Phone (302) 774-2358 [477]

## Substrates feature high dielectric constants

Sapphire, quartz, and alumina substrates for microwave and microelectronic applications feature high dielectric constants. From $10^4$ to $9 \times 10^9$ Hz, sapphire has a 9.3 to 10.3 constant perpendicular to the optical axis, 11.5 to 13.2 parallel to the optical axis. From 0 to 30 GHz, quartz has a 3.7 to 3.8 constant, and from 60 Hz to 25 GHz, alumina has a 9.8 to 10.1 constant. The substrates are parallel within 1 mil and provide tolerances of ±1 mil on length and width and 10 waves/in. on flatness.

Sapphire substrates range from ¼ in. per side to 2 by 1½ in. (5 to 25 mils thick); quartz goes from 1 to 3 in. per side (5 to 25 mils thick); and alumina ranges from 1 to 4 in. per side (10 to 25 mils thick). Standard finish is 1 μin./side, but sapphire and quartz are also offered with one side chemically polished to be scratch-free. Small quantities of the substrates can be delivered in three to six weeks.

Adolf Meller Co., 120 Corliss St., Providence, R. I. 02940. Phone (401) 331-3717 [478]

## Copper-nickel-tin alloy comes in three versions

A copper-nickel-tin alloy, marketed as spinodal 770, was developed for use in high-performance connector applications. The alloy consists of 77% copper, 15% nickel, and 8% tin. Two other compositions of the alloy are also available: spinodal 850 with 85% copper, 9% nickel, and 6% tin; and spinodal 920 with 92% copper, 4% nickel, and 4% tin. The spinodal alloys have unusual properties of strength, formability, and electrical conductivity as well as excellent spring and resistance to stress relax-

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ation, says the manufacturer. Other advantages the company claims are better corrosion resistance and fatigue strength than beryllium-copper alloys, good joining characteristics, and nontoxicity.

Handy & Harman, Industrial Products Division, 850 Third Ave., New York, N. Y. 10022. Phone (212) 752-3400 [479]

## Conductive adhesives offer high performance, low cost

Four Eccobond conductive adhesives offer high performance at a reasonable cost. One, 57C, is a silver-based solder that cures at room temperature to a typical volume resistivity of $6 \times 10^{-4}$ Ω-cm. With bond strength in shear of over 700 lb/in.² (49 kg/cm²), it is priced at about $350 per pound. Solder 72C is about $108 per lb; its resistivity is $6 \times 10^{-3}$ Ω-cm.

A one-component carbon-based adhesive, 60C, sells for about $15.50 per pound and provides a volume resistivity of 50 Ω-cm. A two-part 60L is similarly priced but resistance through a thin film of it is less than 5 Ω, whereas through the 60C it is less than 1 Ω.

Emerson & Cuming, W. R. Grace & Co., Canton, Mass. 02021 [480]

## Sprayable acrylic emi shield satisfies FCC requirements

An acrylic coating that provides effective shielding against electromagnetic interference for consumer, commercial, and industrial electronic products can be sprayed on. Electrically conductive, the Enforcer complies with FCC and VDE requirements for electrical components housed in plastic. Offering a surface resistance of less than 2 Ω/sq, it withstands continuous-use temperatures from −54° to +82°C. When coating approximately 35 ft²/lb to a thickness of 2 mils, it dries tack-free in 30 minutes and is fully dry in 2 hours at 65° to 82°C.

Chomerics Inc., 77 Dragon Court, Woburn, Mass. 01888. Phone (617) 935-4850 [481]

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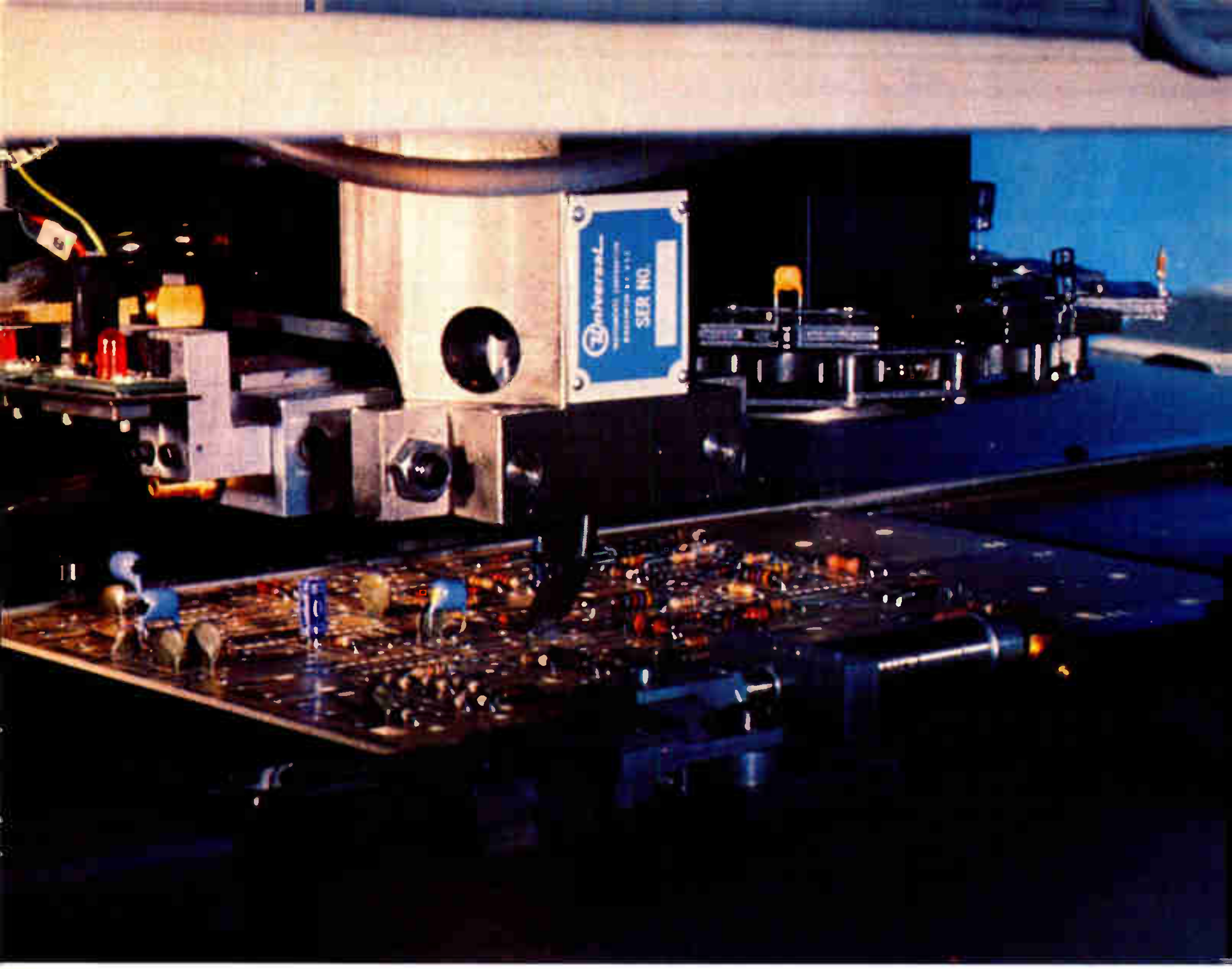



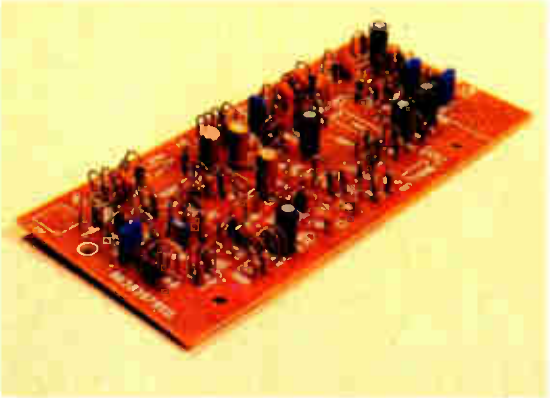

# Products Newsletter

**Precision trimmer potentiometer sells for $2.92**

Vishay Resistive Systems Group of Vishay Intertechnology Inc. is ready to market **a ¾-in. precision trimmer potentiometer at $2.92** each in 100-unit quantities. The 1280 features a temperature coefficient of resistance of less than 15 ppm/°C between −55° and +125°C and can be set to within 0.05%. The group in Malvern, Pa., says that the 1280 "has all the critical characteristics of a precision trimmer at an economical price."

**Digital scope stores four times more data**

The need to retain more data on the low-frequency phenomena that are investigated by digital storage oscilloscopes may be met with Gould Inc.'s OS 4020. The latest addition to its scope line, to be introduced in November by the firm's Cleveland, Ohio, instruments division, will feature a **4-K-by-8-bit memory that holds four times more waveform data than other portable digital scopes.** It will be priced at about $5,500.

**Microprocessor prevents auto theft**

A microprocessor and a programmable read-only memory packed into an automobile's starter can protect the vehicle from theft. When activated, the Phantom system from Elpac Automotive Systems Inc. of Santa Ana, Calif., prevents engine startup unless the car's key is turned to the ignition position the number of times required by the unit's **factory-programmed three- or four-digit code.** Phantom sells to original-equipment manufacturers for $45 to $50 and retails for $299.

**Teledyne Philbrick second-sources military LH0032**

Teledyne Philbrick claims that its version of the military-grade model of National Semiconductor's LH0032 operational amplifier, the model TP0032, has **more consistent performance over the full temperature range of −55° to +125°C.** Though most specifications tally with the LH0032's, the TP0032 has typical power-supply and common-mode rejection ratios of 75 dB and a typical dc open-loop gain of 85 dB, versus about 60 and 70 dB for the original, says the Dedham, Mass., firm. The TP0032 costs about $50 in lots of 100 or more.

**National cuts prices for 8-bit a-d converters**

National Semiconductor Corp., Santa Clara, Calif., is slashing prices **as much as 45% on its microprocessor-compatible 8-bit analog-to-digital converters.** For example, the ADC0806, an eight-channel multiplexing a-d unit with a maximum error of 0.5 least significant bit is going from $17.95 to $9.96 apiece in 100-piece quantities. Also, the ADC0801, a single-differential converter with 0.25-LSB maximum error, is reduced from $16.90 to $12.25.

**NTC thermistors come in the form of ceramic chips**

Monolithic ceramic negative-temperature-coefficient (NTC) thermistors have been developed by Sierracin/Western Thermistor, Oceanside, Calif., **in two diameter ranges: 0.010 to 0.025 in. and 0.050 to 0.100 in.** Designed for a temperature range of −50° to +150°C, they feature sensitivities from −3%/°C to +0.7%/°C. They are available with tolerances of ±0.05°, ±0.1°, ±0.2°, ±0.5°, and ±1.0°C.


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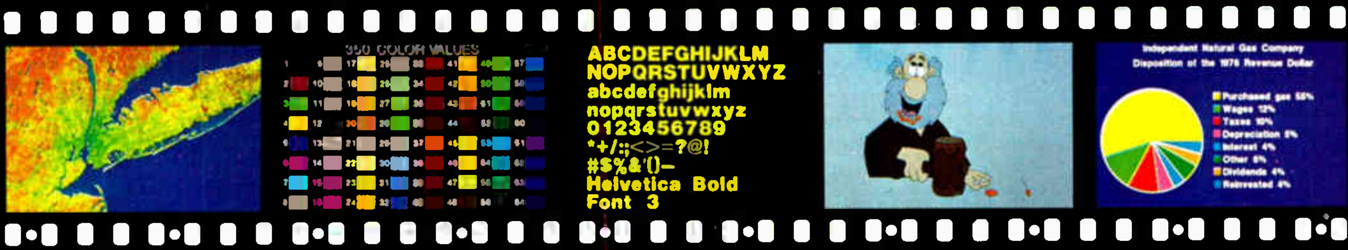


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# Career outlook

**Government fellowships.** The National Science Foundation plans to award nearly 550 fellowships in the spring of 1981 for advanced study to help meet the continuing national need for qualified scientific personnel. Included will be 400 graduate fellowships, 50 minority graduate fellowships, 50 postdoctoral fellowships, and 50 North Atlantic Treaty Organization postdoctoral fellowships. Application materials for all programs are now available.

Open to all qualified citizens and nationals of the U. S., the awards will be made on the basis of merit in all fields of science, including interdisciplinary and multidisciplinary areas. The application deadline for the graduate fellowships is Nov. 26, 1980, and for the postdoctoral, Nov. 3, 1980.

For more information on the three NSF fellowships, write to the Fellowship Office, National Research Council, 2101 Constitution Ave. N. W., Washington, D. C. 20418. For the NATO fellowship, write to the NATO Fellowship Program Office, Division of Scientific Personnel Improvement, National Science Foundation, Washington, D. C. 20550, or call (202) 282-7154.

**Computers and the law.** A special two-issue set of the Computer/Law Journal will be published in early 1981, and a call for papers has been issued. The set, "Law and Information Policy," will contain papers on all areas of information processing, from the legal aspects of fact gathering to those of information storage, retrieval, and transmission. Topics include privacy, protection of data bases, cryptography, and antitrust polices in the telecommunications industry. Articles about international information law and policy are of particular interest.

Authors who wish to submit papers should write to Dr. Jon Bing at the Norwegian Research Center for Computers and Law, Oslo University, Karl Johans Gt. 37, Oslo 1, Norway; or to Michael Scott, Editor-in-Chief, Computer/Law Journal, 530 West Sixth St., 10th floor, Los Angeles, Calif. 90014.

**Hybrid tutorial.** For those able to attend the International Society for Hybrid Microelectronics technical symposium later this month in New York who have no solid grounding in hybrid technology, a one-day course is being offered. Aimed at executives, engineering professionals, technicians, and students, "Introduction to Hybrid Technology" will give a fundamental understanding of the field.

Robert J. Ost, hybrid technology group leader for the Sperry division of Sperry Corp., Great Neck, N. Y., will outline what is currently available in production equipment, materials, and components, as well as the latest assembly and quality assurance techniques in both thick- and thin-film microelectronics. Emerging technologies will also be covered.

Enrollment will be limited to 120 people; the registration fee for the tutorial is $30 per person or $15 for full-time students. The course will be held on Oct. 21, from 9:00 am until 5:00 pm. Additional information is available by writing ISHM Headquarters, P. O. Box 3255, Montgomery, Ala. 36109, or by calling (205) 272-3191.

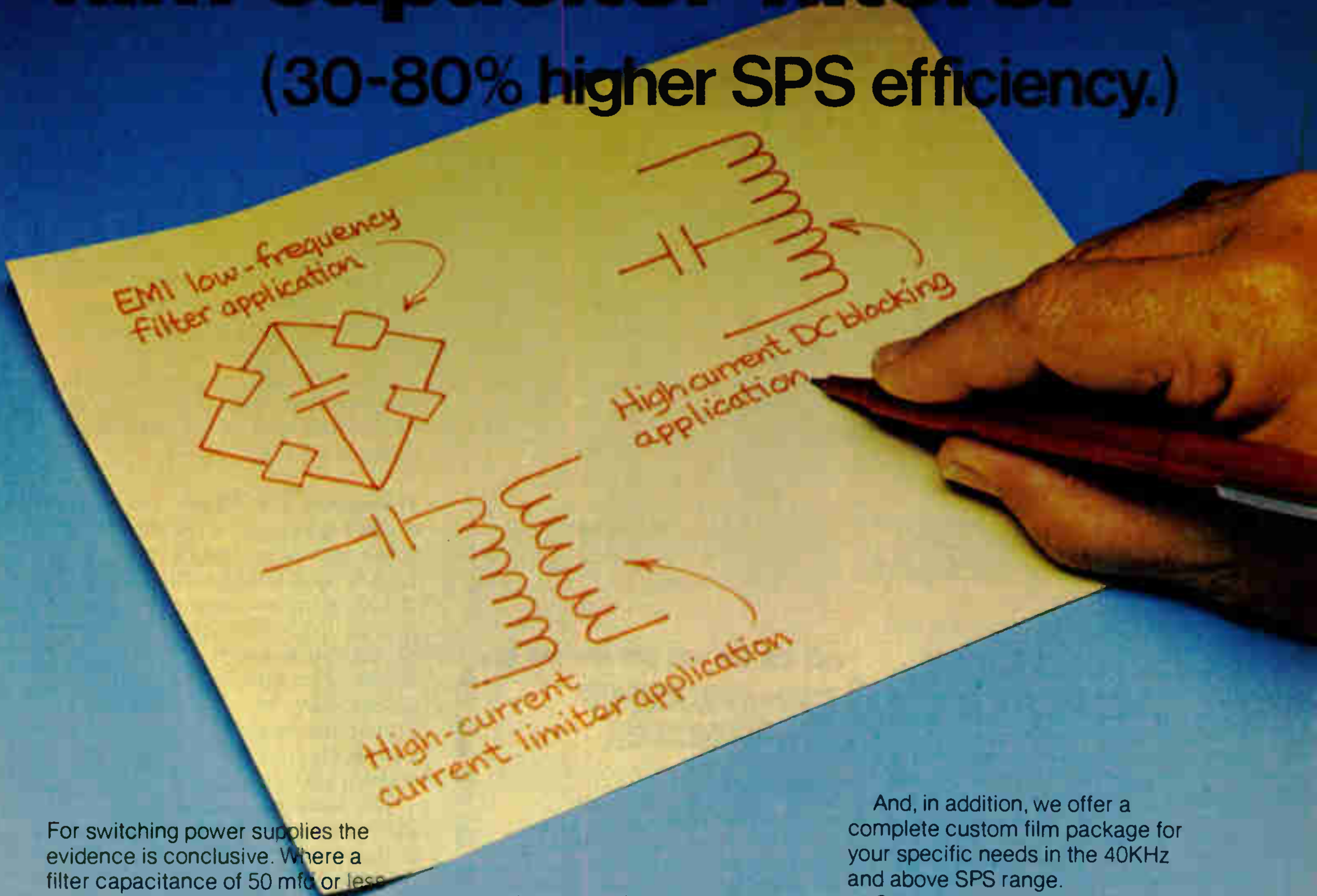
**Considering the ergonomics.** A special session at the Eastern Design Engineering Conference—to be held this year Oct. 28–30 at the New York Coliseum—will focus on the relationship between machines and the people who operate them. Entitled "The Human Factor in Design," there will be four presentations in the session: "Human Factors Considerations in Computer-Aided Design of Mechanical Parts," "Integrating Human Factors Engineering into Product Design: A Case Study," "Practical Applications of Human Factors Engineering," and "Human Factors in Control System Design: From Simple Machines to Large Processes."

For more information on this session, or on the conference, write to Clapp & Poliak Inc., 245 Park Ave., New York, N. Y. 10017.

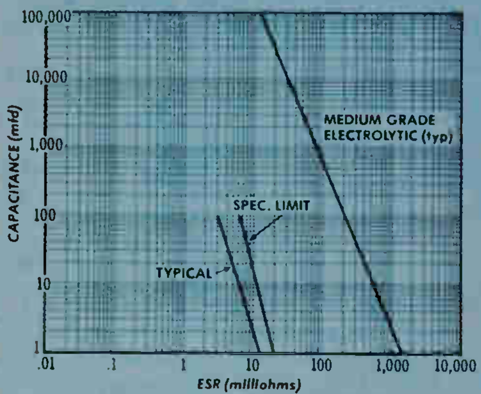
**Cryptology as a practiced art.** The need to protect data by coding or

# Why the switch is on to film capacitor filters.

## (30-80% higher SPS efficiency.)




For switching power supplies the evidence is conclusive. Where a filter capacitance of 50 mfd or less will do, metallized polypropylene (film) capacitors far surpass electrolytics in impedance characteristics.

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Here's why:

At resonance, ESR for a film capacitor is less than *one-tenth* that of an electrolytic. The film's capacitance won't dwindle at higher switching rate frequencies, so you can design with a lower value cap.

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## Career outlook

ciphering is becoming more necessary as computer crime escalates. A one-day seminar for executives and managers responsible for data processing, telecommunications, corporate operations, security, or planning is being given Oct. 20 in Los Angeles and Nov. 10 in Palo Alto, Calif. "Cryptology and Data Security" is normally a three-day seminar, but this shortened version is intended to give the executive a perspective on the types of threats companies are facing in these areas, the countermeasures that may be taken, and the costs of these measures.

For more information, write to Hellman Associates, 299 California Ave., Palo Alto, Calif. 94306, or phone (415) 328-4091.

**Prototyping the future.** For those design engineers who cannot wait to begin prototype work on Intel Corp.'s soon-to-be-available family of single-chip microcomputers made with its HMOS technology, the EM-51 emulation board is now being offered. The functional and electrical equivalent of the 8751, the EM-51 may also be used for development work calling for the 8051 and 8031 microcomputers.

The board plugs directly into the 8751 sockets without a cable. It includes sockets for 2716 or 2732 erasable programmable read-only memories, which substitute for the on-chip memory during prototyping.

The EM-51 sells for $950, with delivery in six to eight weeks. For more information, write to Intel Corp., 5200 N. E. Elam Young Pkwy., Hillsboro, Ore., 97123.

**Boston job fair.** A specialized career open house for technical and professional people in the fields of electronics and commercial data processing will be held in the Boston area, Oct. 27–28, at the Northeast Trade Center. More than 50 companies are expected to participate.

Contact Jim Peck, Managing Director, Technical Job Mart, Northeast Trade Center, 100 Sylvan Rd., Woburn, Mass. 01801, or call him at (617) 935-8090, for more information.

# Hardware Engineers and Software Engineers: MAKE YOUR RESERVATION NOW.

Take your place with the Strategic Systems Division engineering staff. In 1981, we'll be occupying a new 300,000 square foot design and development facility in Westborough, Massachusetts. This suburban location, conveniently close to Boston, will be the new home of the talented professionals responsible for the MX $C^3$ and Minuteman programs.

Our MX $C^3$ program, as well as the continuing development of the Minuteman System, is creating new roles for those who are capable and ready to accept them. MX $C^3$ will involve the world's largest fiber optic cable network, over 15,000 Kilometers; a radio communications system incorporating over 600 VLF, MF, HF, VHF, UHF and SHF radios; a hierarchy of over 5000 computers; and one of the largest software communications networks ever developed.

By joining us now, you reserve your place in a program that offers all you're looking for...and more.

You're looking for the excitement-charged atmosphere of a really new project? Our MX program is venturing into advanced areas most engineers only read about. The term "state-of-the-art" takes on new meaning here.

You want flexibility? You can work in any or all of the areas listed below, as your interests change. We'll give you the freedom to explore every function, every discipline, every one of your strengths.

You like the visibility of a small work environment? Our engineers cluster in balanced teams, for maximum creative interaction. Those who join us now will always play a crucial role in our activity.

You're looking for technical growth? The intense involvement, front end development, advanced techniques, and exceptional talent associated with this program make one or two years here worth many times that anywhere else. And to enhance your growth you can participate in in-house training and instructional programs.

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If you have what it takes, you're already interested. So make your reservation now to join us...GTE's Strategic Systems Division.

# ENGINEERING MANAGER PRODUCT DEVELOPMENT

## To Become A Part Of Our Management Team.

We are an advanced technology company with a substantial R & D Budget, dedicated to designing and manufacturing electro-mechanical systems for the military. Technology involves lasers, radar, navigational systems & integration with weapons & delivery systems.

We need a director for our applied R & D effort. The challenge is two fold. First, develop new products or advanced versions utilizing new combinations of state-of-the-art electronics. Second, perform business planning with presentations to top management & contractors, for a multi-million dollar program.

This position is located in suburban St. Louis, reports to a senior vice president, and is a member of the Strategic Management Team. Salary will be around $50,000 depending on qualifications, plus substantial benefit package.

The successful candidate will probably have a degree in EE, Physics, or ME. Experience will consist of 10 or more years designing military hardware involving advanced technology. Component or systems background is desirable. Specific experience with microprocessors computers, software, lightweight mechanical devices, automatic test equipment, electronic warfare, and vehicles would be helpful.

**Please forward resume to P-2859, Electronics Class. Adv. Dept., PO Box 900, NY, NY 10020**

All replies will be received by our personnel consultants and none revealed without your permission after a preliminary review of mutual interests.

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The individuals we seek will formulate, design and program automatic test systems for avionic products, as well as evaluate production test performance and automatic test equipment for radar (color displays) data navigation production.

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Tektronix Laboratories has need for an experienced professional in the area of advanced silicon IC process technology. The individual will be responsible for contributing to and leading (5 to 10 engineers) a growing research effort in new materials and advanced IC structures and circuits. Primary focus will be high power laser processing techniques. Background must include significant R & D experience in all aspects of device oriented materials and processing. A well equipped research oriented IC cleanroom facility is available for R & D work as well as others for engineering development and manufacturing. We feel this position represents an excellent opportunity for someone to join a respected company that has been developing and manufacturing high performance custom IC's for over 13 years in the Portland metropolitan area.

For consideration, please call Gary Hecht at (800) 547-1164, or send resume to Gary Hecht, MS 55-033, Tektronix, Inc., P.O. Box 500, B-4, Beaverton, Oregon 97077.

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**Engineers: Electrical-Civil-Mech.** Nationwide openings—all levels—$15-60K Energy, Environment, Chemical, Power, Oil/Gas, HVAC, Piping etc. Send resume w/salary requirements to: Engrg/Mgmt Recruiting Services—416 E. Downs, Stockton, CA 95204. "Mitch" (209) 529-8145—All Fees Paid.

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## RESUMES

**Resumes—Complete instructions** and examples; $4, Consultants, Box 567—J. Bergenfield, N.J. 07621.

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# ENGINEERS

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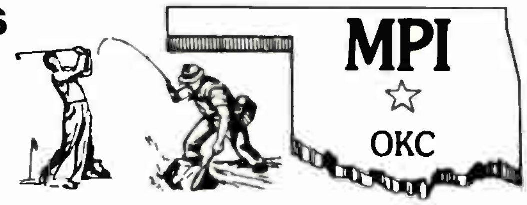


If you have been thinking that 1980 might be your year for a change in the direction of your career, we invite you to investigate the technical careers available with us in Oklahoma. We have immediate opportunities for

### ELECTRICAL ENGINEER (3 required per "A", "B" & "C" below)

"A" Design of phase locked loop, closed loop systems and linear phase filters and amplifiers. Prefer familiarity and experience with LSI design for disk products or similar technology background. BSEE required or MSEE preferred and 4-9 years experience or equivalent experience.

"B" Design of analog and digital circuits. Ability to analyze problems and develop practical solutions. Experience in the area of read amplifiers required. BSEE degree required or MSEE preferred plus 9 years experience.

"C" Ability to handle all phases of design on rotary positioning systems, including electro-mechanical design of positioning motor and all electronics related to 8" rigid disk design. BSEE required or MSEE preferred. A minimum of 9 years design experience or equivalent required.

### ELECTRICAL ENGINEER (2 required as per "D" and "E" below)

"D" Analyze, design and develop analog circuits required for new products. Involves servo mechanism circuit design; A/D and D/A techniques; optical, ultrasonic, and magnetic transducers; bar code and character reading; ink jet circuitry; and use of micro processors as related to above. BSEE required; MSEE desirable plus 9 years design experience emphasizing analog circuit design.

"E" Project Engineer responsible for the design and development of test equipment and test systems. Will include Design and Design Leadership; Project Planning, Scheduling and Monitoring; and Development Coordination for a group of Engineers and Development Technicians. BSEE or BSME required plus 6-9 years of equivalent experience.

### MANUFACTURING ENGINEER — PLATING & PAINTING

Knowledge of paint and plating processes; must include electro-plating of zinc on steel anodizing aluminum and paint systems.

### DESIGNER

Create, design, and prepare layouts of products from written or oral information. Should be creative and well-versed in drafting techniques, as well as engineering and manufacturing processes and procedures. Should have 6-9 years related experience.

### MECHANICAL ENGINEER

Mechanical design, development, evaluation, manufacturing release and continuation of new flexible disk drive products. Experience in cost reduction programs desired. BSME required; MSME preferred plus 6 years related experience or equivalent experience.

### SENIOR SYSTEMS ENGINEER

Responsible to develop systems requirments and specifications for new non-impact printer products as well as analyze and propose potential hardware/software design approaches. You will be a project leader for custom and special customer interfaces. Requires three (3) years of logic/system design experience in the field of minicomputers or mainframes with knowledge of disk/tape/terminal controller design and operation and knowledge of IBM or Honeywell operating system. A BSEE or BS Computer Science degree or equivalent is desired with MS degree preferred.

### MANUFACTURING ENGINEER — MECHANICAL ASSEMBLY

Mechanical Assembly Tool Designer. Will design small to medium tools and fixtures for Mechanical Assembly. Minimum of three (3) years tool design experience preferred and drafting techniques are required.

### QUALITY ENGINEERS — INSPECTION

Responsible to develop and evaluate quality plans and inspection procedures. Will investigate component part problems and initiate corrective action. May provide supervision of assembly inspection personnel. Good communication skills essential. Should have BS degree in technical discipline plus minimum of 3 years quality control experience, especially in high-volume precision electro-mechanical devices.

### AUTOMATION ENGINEERS

Experienced in design, creation and implementation of automation tooling, systems and methods. Strong background in mechanical, hydraulic and pneumatic applications in design of sophisticated assembly devices for automatic assembly of electro-mechanical devices. Desire experience in design of machines to assemble small linkage mechanisms and experience in tool and die design or control systems background using microprocessor controllers in automatic assembly equipment. Desire technical degree with 6 or more years related experience.

### MANUFACTURING ENGINEER — SHEETMETAL

Delineate sheetmetal process instructions. Tooling justifications, work planning revision update and problem solving.

### MANUFACTURING ENGINEER — PWA TEST

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