SEPTEMBER 25, 1980

**SPECIAL REPORT: GATE ARRAYS STAKE A CLAIM AS LOGIC REPLACEMENT/145**

C-MOS microprocessor teams with versatile ROM/123

Electron devices meeting to emphasize 3-d structures, VLSI/89

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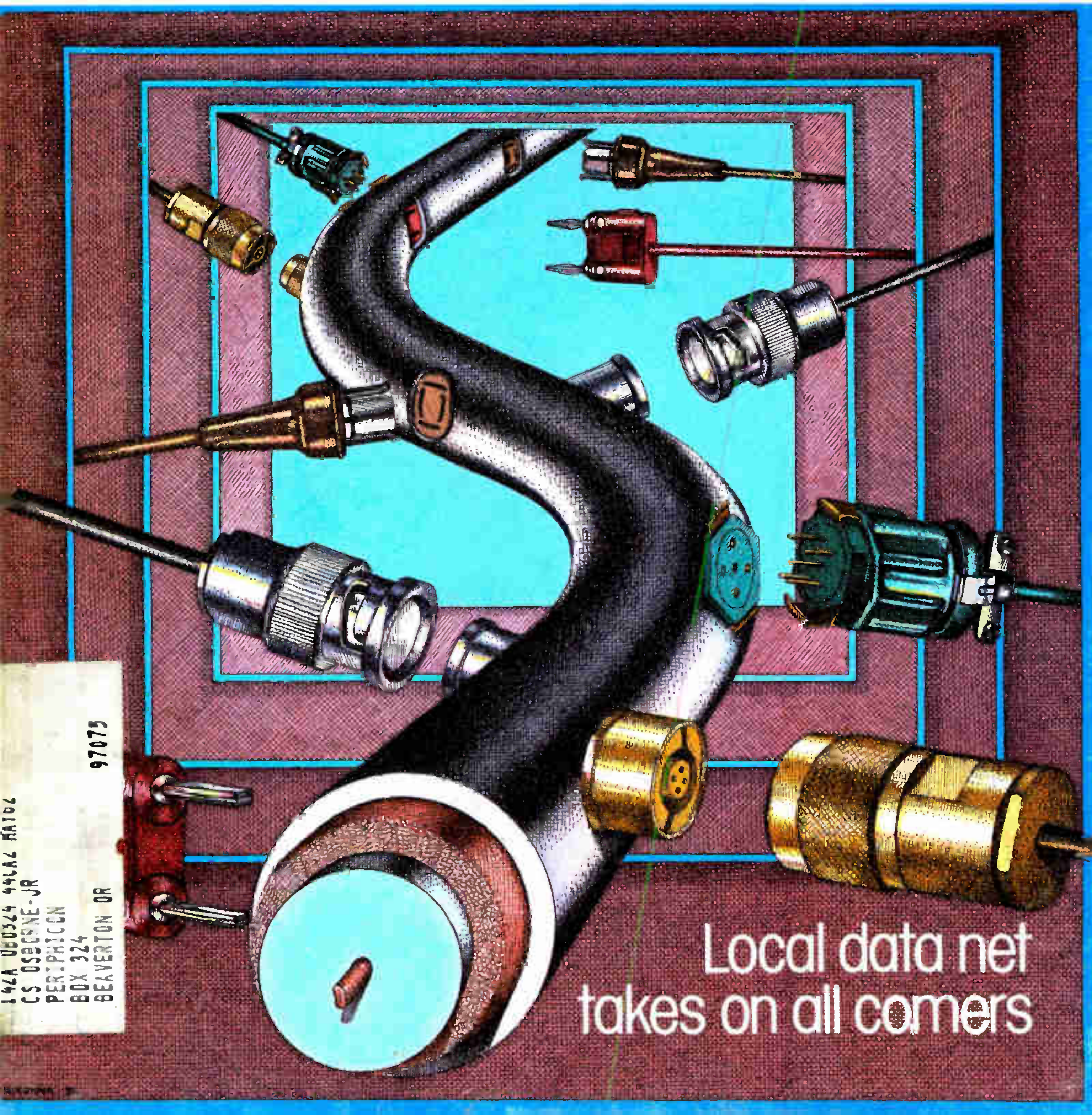

# Pushing performance to the physical limits, yet versatile and easy to use. HP's new 3456A DVM.

Performance well beyond what you expect in a DVM. That's what HP's new 3456A offers. You get standards lab accuracy under many test conditions, with quiet, repeatable 100 nanovolt resolution on the 100 millivolt range. What's more, the inherent noise rejection of integration is enhanced by an advanced A to D converter to give you 48 readings per second with useable one microvolt resolution. That's performance approaching theoretical limits.

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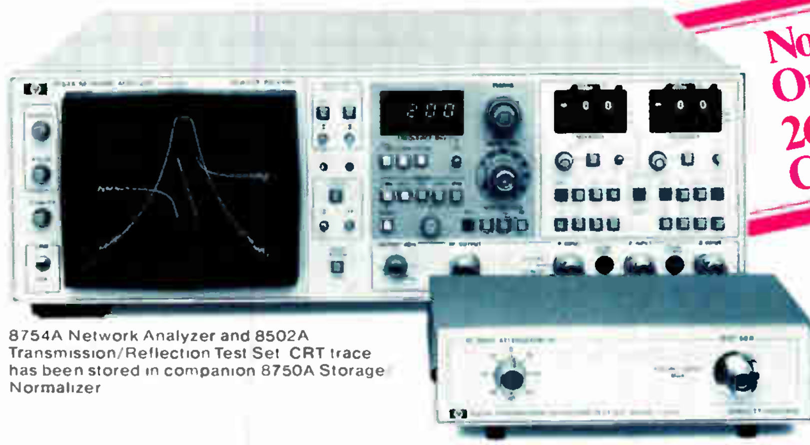

8754A Network Analyzer and 8502A Transmission/Reflection Test Set. CRT trace has been stored in companion 8750A Storage Normalizer

## HP's 1300 MHz Network Analyzer. It brings speed and convenience to RF measurements for only $12,400.

The HP 8754A consists of:

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Just add the appropriate test set and you can make thorough and accurate measurements quickly and easily. Such as:

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Measure loss, gain and phase shift using the 11850 Power Splitter ($675). Completely identify filter passbands and skirt characteristics without misleading harmonic or spurious responses.

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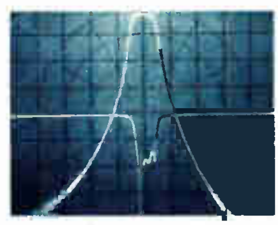
Measure and display impedance in polar form, with crystal markers to give precise frequency data. Test sets are available for both 50 and 75 Ω systems.

### Simultaneous Transmission and Reflection.



Use the 8502 Test Set ($2250) and see the trade offs between transmission gain/loss and input match in a single setup. For two-port characteristics of networks, including transistors, an S-parameter test set is available.

### Storage/Normalizer increases the 8754A's capabilities.

Add the 8750A and you can automatically remove system frequency response variations also make comparison measurements easily. Digital storage permits flicker-free displays even for measurements requiring slow sweep rates.

A call to your nearby HP field sales office is all you have to do to get more information, or write 1507 Page Mill Road, Palo Alto, CA 94304.

Domestic US prices only.

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Electronics
The International Magazine of Electronic Technology
Vol. 53, No. 21 • September 25, 1980

## 114 Technical Articles



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## 89 Probing the News



## 173 New Products



### Departments



### Services

# Electronics



# Highlights

### Cover: Local network ties in all types of gear, 114

No matter what manufacturer or protocol is involved, literally thousands of devices—computers and peripherals—can now communicate over a single local network. By means of programmable interfaces, Net/One accommodates any unit using the RS-232-C serial or a TTL-level parallel interface. It also offers unmatched control of distributed data-processing resources.

Cover illustration is by Ron Chironna.

### IEDM: where the elite of solid-state devices meet, 89

More than any other conference, the International Electron Devices Meeting develops a picture of the underlying technologies and process enhancements that will deliver tomorrow's circuit techniques. This year's meeting, to be held in Washington, D. C., Dec. 8–10, gives a good deal of attention to materials—polycrystalline and amorphous silicon, gallium arsenide, and metal silicides—for both discrete devices and very large-scale ICs.

### Microprocessor makes the most of C-MOS, 123

A low-power microprocessor takes a double-barrelled approach to bettering n-channel designs. It adds such features as an oscillator, a timer that can stimulate vectored interrupts, 16 bidirectional input/output lines, and 112 bytes of random-access memory. But that's not all. It rides its complementary-MOS technology for the most mileage it can, including an orderly power-up and -down sequence and special instructions that further cut its already low power consumption.

### Taking the heat off semiconductors, 135

Never a factor to be slighted, thermal design of electronic equipment is growing more important as ever-larger power semiconductor devices come onto the market. In addition to a device's maximum operating junction temperature, its thermal resistance and the heat sink's, the type of cooling, mechanical factors, and the thermal environment must be weighed.

### Gate arrays arrive, 145

Semicustom logic offers a way out of the mass production–dedicated function dilemma facing very large-scale integration, and gate arrays have emerged technically and commercially as one viable type. This special report takes a comprehensive look at both MOS and bipolar arrays.

### And in the next issue . . .

A mainframe central processing unit on a chip . . . a special report on integrated fiber-optic receivers . . . digital error-correction technique boosts the performance of 9- to 12-bit subranging analog-to-digital converters . . . a family of monolithic phase-locked-loop frequency synthesizers.


*September 25, 1980 Volume 53, Number 21 103,113 copies of this issue printed*

Electronics (ISSN 0013-5070). Published every other Thursday by McGraw-Hill, Inc. Founder: James H. McGraw 1860-1948. Publication office 1221 Avenue of the Americas, N.Y., N.Y. 10020; second class postage paid at New York, N.Y. and additional mailing offices.

Executive, editorial, circulation and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 997-1221. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

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| Mid Range | LO-RF | 45 | 30 |
| | LO-IF | 40 | 25 |
| Upper Band Edge to | LO-RF | 35 | 25 |
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Circle 5 on reader service card

**Gate arrays have** quietly become a major factor in the industry's design arsenal. Not only have the companies that originally developed arrays come out with new products, but what's more, new companies have entered the field.

This movement, described by solid state editor John Posa in the special report starting on page 145, underscores the advances in technology that now make it possible to build very large-scale integrated arrays. New, more sophisticated computer-aided design programs offer the opportunity to achieve high density—up to 5,000 gates on a chip—so that users are now replacing entire mainframe logic or entire disk controllers with arrays. John adds, "I was impressed, too, with how far oxide-isolated complementary-MOS arrays have come. They're now competitive with fast bipolar technology."

John points out that the Europeans were early supporters of arrays. "I credit the Europeans with insight. They identified the need for and applications of arrays," he observes, "and they stuck to their support even though interest declined in the U. S. during the '70s."

Japan, on the other hand, has not made much of a move in this area—so far. There are indications that this situation could change, because the Japanese have described some arrays in conference proceedings.

Although the report highlights the growing success of arrays, these products appear to have a finite market—to replace existing logic. "A computer designer doesn't usually embark on a logic design with a gate array in mind," John states. Yet, he adds, it could happen in certain situations because with CAD simulation it is now possible to design an array economically for small-volume uses.

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**For three years** *Electronics* has augmented its information services to readers with an organized program for publishing books and editorial reprints. Now we are getting set to expand that effort.

Starting this fall *Electronics* plans to hold a series of short, intensive seminars for people who need a quick fix in specific subjects. The first batch covers four especially important topics:

- Applying Single-Chip Microcomputers. The seminar leader will be Joseph Willhide, a pioneering inventor of nonvideo electronic games using single-chip microcomputers. He is associate professor of systems and computer engineering at Boston University.
- Microelectronics Interconnection and Packaging. Leading this seminar will be Daniel I. Amey, engineering manager of packaging techniques for Sperry Univac at Blue Bell, Pa.
- Quality Assurance for Electronics Manufacturers. This timely conference will be led by C. L. Carter Jr., Dallas-based director of quality, reliability, and safety in the southwestern region for the consulting firm of Rath & Strong Inc., Lexington, Mass.
- Pascal. Heading this seminar will be Herbert L. Dershem, who has been a consultant specializing in software for many years. He is currently chairman of the department of computer science at Hope College in Holland, Mich., and is the author of "Computer Exercise for Elementary Statistics."

Coordinated by special projects manager Janet Eyler, these seminars are the beginning of an ongoing series. Others being planned for next year will cover various aspects of designing and interfacing with microprocessors.

Most of these seminars will be available for in-house courses as well. Arrangements can be made to send an instructor to hold a seminar at a company if enough are interested in the topic.

For a complete description of these seminars, the dates, and the locations, contact Janet Eyler, *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020.

# Readers' comments

## Alive and kicking

**To the Editor:** Your editorial about the demise of the reform movement among engineers [Aug. 14, p. 12] is, like Mark Twain's reported death, premature. What is true is that the reform efforts undertaken by the Institute of Electrical and Electronics Engineers' Professional Activities Committees are dead; indeed, they never existed. That is because the various IEEE vice presidents for professional activities, selected by the board of directors, have been either academics or corporate executives. They simply will not do anything to correct the chronic oversupply of engineers. Out low incomes are sufficient proof for the existence of a glut of engineering manpower.

But our own activities continue unabated. Consider our efforts to:

- Alert the U. S. Department of Labor to violations on the part of ITT and others in recruiting foreign nationals to work here (successful).
- Convince the American working engineer that the profession of a college professor is not the same as the profession of a working engineer (partly successful).
- Alert the Department of Defense to violations by their contractors of the Age Discrimination in Employment Act as it affects recruitment advertising for engineers (partly successful).
- Convince the IEEE that engineering "degrees" from phoney colleges pose a threat to the legitimate, hard-earned degrees of the majority of its members (unsuccessful). It must be noted that at least two former members of the IEEE's board of directors have phoney doctoral degrees.

As to my cardiac condition. I am still very active; I still write and publish a monthly newsletter; I have not changed.

Irwin Feerst
Committee of Concerned EEs
Massapequa Park, N. Y.

## Up and running

**To the Editor:** AMI has been supplying samples of 64-pin plastic S9900 devices for the last five months and sold the technology for the 64-pin plastic package to Texas Instruments in a technology-exchange program. We are, in fact, the only company in the last five months that has had a working 64-pin plastic packaging process in house.

Therefore I was surprised to read in the Aug. 14 Products Newsletter [p. 181] that only TI offers the TMS 9900 in plastic, 64-pin dual in-line packages.

Frank Toth
Manager, Product Marketing and Applications
Microprocessor Group
American Microsystems Inc.
Santa Clara, Calif.

## One-eyed Big Brother?

**To the Editor:** Reading the recent article concerning the British Open University's development of a system called Cyclops ["Cyclops will equip TV sets to receive and send color or monochrome graphics," July 31, p. 66], I wondered if 1984 wasn't a bad prediction for the year of "Big Brother."

I also wonder how many readers are aware of the implications of installing equipment in the home capable of not only receiving a wealth of information but sending it as well. The technology is available to not only turn your living room into a "remote classroom" but into a laboratory capable of being monitored 24 hours a day.

Let us not be too hasty to hail the advance of technology in an area with such a potential for abuse to individual privacy. Without careful safeguards, devices such as the Cyclops might be used to control our lives to an intolerable degree.

G. Tim Schlaile
Pasadena, Texas

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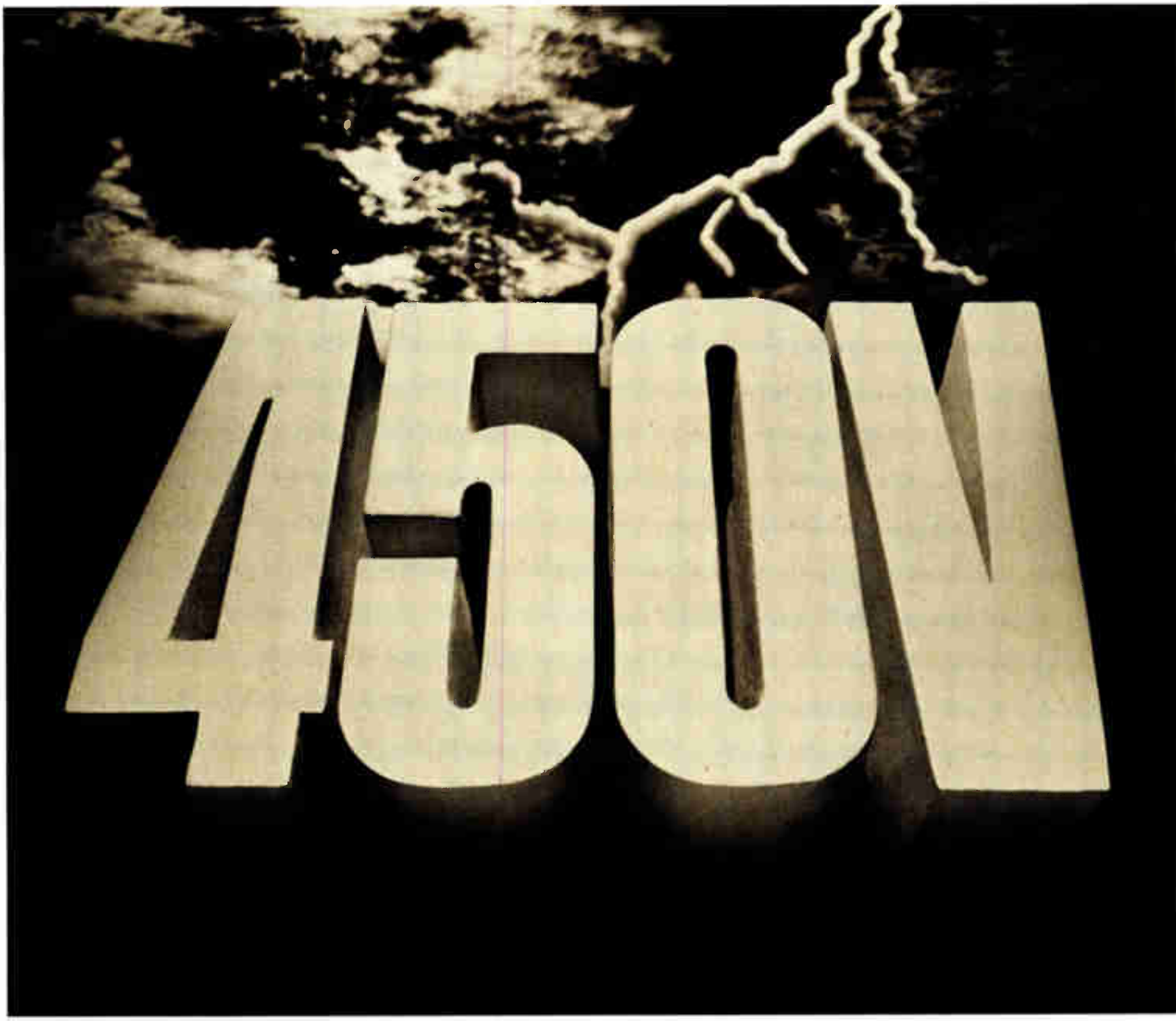
## Corrections

*In "Cyclic redundancy routine tracks data-stream errors," (July 3, p. 163) location 200D should read LDA B LCHK instead of LDA A LCHK.*

*The fund for the joint Japanese government and industry drive in optoelectronics (Aug. 28, p. 76)—which will end March 31, 1987—will total $2.8 million. The monies quoted as appropriated so far are from the Ministry of International Trade and Industry.*

# POWER MOSFETs




## A better power MOSFET.

Announcing a major new family of power MOSFETs: the IVN6000 series. Using an improved DMOS process that provides better transconductance, reliability and high-voltage performance. Now producing a power MOSFET with 450V breakdown voltage and 10ns switching speed!

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If your application operates directly from an ac line, a 400V power transistor can be risky. When you consider the effects of high line voltage, stray inductances, momentary surges and the change in $BV_{DSS}$ with temperature—you need 450V.

And that's why the IVN6000 is the answer for a whole spectrum of uses: Switching power supplies, voltage converters and inverters, pulse amplifiers, lighting and motor controls, rf applications, on and on.

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## Goodbye bipolars.

Bipolar power transistors are no longer a good deal. This comparison chart shows why power MOS designs have fewer parts, smaller size, less weight, less cooling and higher overall reliability.

| | Power MOS | Power Bipolar |
|---|---|---|
| Switching Speed | 10 ns | 1 μs |
| Input Current | 100 nA | 300 mA |
| Secondary Breakdown | No | Yes |
| Drive Circuitry | Simple | Complex |
| Device Paralleling | Yes | No |
| Integral Reverse Diode | Yes | No |

## Check these specs:

- Breakdown Voltage:
  IVN6000KNT = 450V, Min.
  IVN6000KNS = 400V, Min.
  IVN6000KNR = 350V, Min.
- Switching Speed:
  10ns, Max.
- On Resistance:
  3.0Ω at 1A, Max.
- Continuous Drain Current:
  2.25A, Min.
- Peak Drain Current:
  7.5A, Min.

## Priced right. Ready to go.

Intersil's DMOS process also provides some significant manufacturing advantages. Its smaller die sizes mean lower prices. So the 100-piece price for the 450V IVN6000KNT is only $10.95.

For the 400V part, it's $10.25. For the 350V part, it's $9.50. All in TO-3 packages. Not a bad deal.

Also, since our DMOS is very manufacturable, you won't have to worry about getting parts. The company that's introducing new highs in power MOSFETs is also introducing new lows in power MOSFET delivery times.

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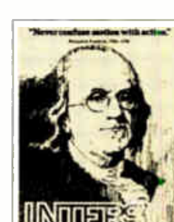
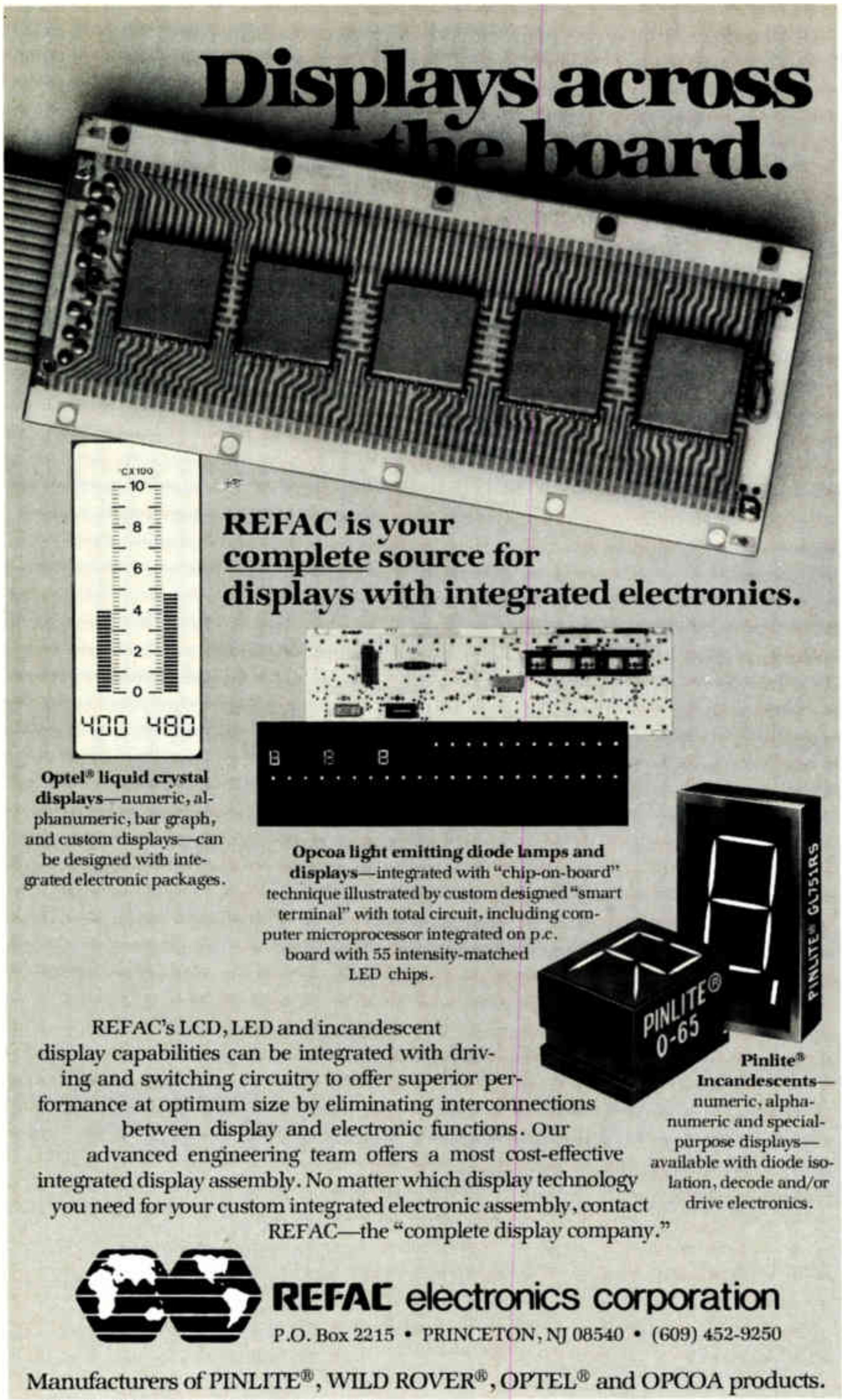





Circle 12 on reader service card



## News update

■ The key contestants in the bubble memory business are quietly perfecting their 1-megabit chips and support circuits for the battle that looms. Having traded its 68000 16-bit microprocessor expertise for Rockwell International's bubble know-how, Motorola Inc., too, will be in that race. At the 1-Mb level, it will be competing with Texas Instruments, Intel Magnetics, National Semiconductor, and Rockwell, for that matter.

As a result of the trade [*Electronics*, June 21, 1979, p. 33], Motorola is building support circuits like the sense amplifiers and coil predrivers; Rockwell is building the n-channel controller; and each will have rights to the other's circuits. In addition, both are building their own megabit chips. Rockwell is already building samples of its 1-Mb chip and Motorola expects to be sampling everything else—including its memory—by the first quarter of 1981.

**256-K.** Motorola also received complete plans for Rockwell's 256-K bubble part, which it is building in limited quantities. This design does not have swap gates, which allow data for reading to simultaneously change places with data for writing. Nor does it have boot loops, which store redundancy information—the location of the bad loops—without having to keep track externally, as in a programmable read-only memory.

"We feel the market requires both of these features, and our megabit chip will have them," says Leonard M. Call, Motorola's market development manager for bubble memory systems. Although an earlier 1-Mb Rockwell chip did not have these elements, its newest part does.

**Megabits.** Both chips will have block-replicate architectures, seen from the outside as 1 million by 1 bit. This resembles National's plans, but contrasts with the long folded loops of Intel's chip and the 512-K-by-2-bit organization of TI's.

Motorola expects an access time of 10 to 12 milliseconds. All development work is under one roof, the Motorola Integrated Circuit Applications Research Laboratory, or Mi-carl, in Mesa, Ariz. **-John G. Posa**

# People

## Apple's Lawrence predicts sales boom in Europe

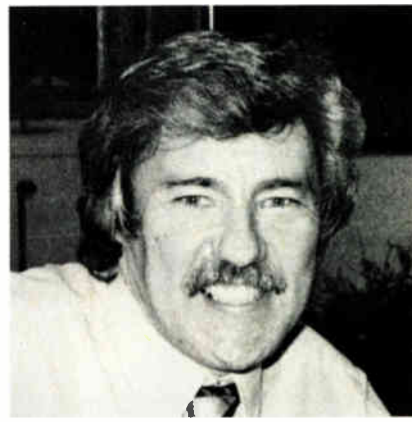
Explosive growth seems sure for personal computers in Western Europe during the coming decade and that explains in large measure why the apple of Thomas J. Lawrence's eye now starts with a capital A. Although Europeans so far have not taken to personal computers the way Americans have, that is fast changing. And as the new general manager for European operations of Apple Computer Inc., the 47-year-old American aims to make the sales totals on his turf comparable to those in the U. S. for the Cupertino, Calif., company.

This long-term aim is ambitious, certainly. Europe at the moment acounts for only 20% of the Apples sold and the U. S. for most of the rest. But Lawrence and his European crew will have going for them a burgeoning market for "one-on-one" computers (as he sometimes describes them), a market better structured for growth in a sense than in the U. S.

"There is practically no hobby market in Europe," Lawrence explains. He singles out single-owner businesses as the major market segment, 50% of the total. Partnerships add another 15%. Thus the market will be driven, he reasons, by hard-headed people buying computers with which to earn more money rather than to have fun. Consumer whim, then, will not condition sales curves, but sound business decisions will.

Before he started working for Apple on Sept. 1, Lawrence headed Intel Corp.'s operations in Europe for six years. "Apple will be as innovative in software as Intel was in silicon," he maintains. He is convinced that getting effective business software packages on the market will be crucial to growth.

And Apple will go native with its software as much as possible. "Our French distributor has invested $200,000 to translate operating manuals into French and has prepared French versions of Pascal and



**Eye on the Apple.** Thomas J. Lawrence is out to boost Europe's 20% of Apple sales.

an accounting package," he points out. He plans to push for similar investments in native-language software elsewhere, particularly in West Germany and the Scandinavian countries.

"It's like coming home again," sums up Lawrence of his return to the computer business. After taking bachelor of science degrees in electrical engineering and mathematics at the University of Michigan in Ann Arbor, he went on to a master's in computer sciences at Stanford University in Palo Alto, Calif. Prior to joining Intel, Lawrence worked in the computer divisions of the Singer Co. and RCA Corp.

## Sandhu leads GI toward three process pathways

A master in the art of semiconductor processing, Jagtar S. Sandhu is now perfecting those processes that will carry General Instrument Corp.'s Microelectronics division through to the middle of the 1980s. As vice president of technology, the 43-year-old Sandhu is narrowing his pursuit to three design and process innovations that may well affect the entire device output from GI's plants in Hicksville, N. Y.; Chandler, Ariz.; and Glenrothes, Scotland.

"For the next three to five years, we'll be looking at three fronts processwise," says Sandhu, who works at the division's headquarters in Hicksville. "We're looking at the

## People

**Looking ahead.** Jagtar S. Sandhu is looking at advanced process for General Instrument.

most advanced technology for silicon-gate n-channel MOS, silicon-gate complementary MOS, and n-channel [electrically erasable programmable read-only memories] made using both metal and silicon gates," he notes, adding "the silicon-gate MOS will be used for ROMs and microprocessors, and the silicon-gate C-MOS will be used for telecommunications devices as well as microprocessors." Until now, all of GI's EE-PROMs have been made with a p-channel MOS process.

Sandhu, who has his undergraduate and master's degrees in chemistry from Punjab University in Chandigarh, India, received his Ph.D. in chemistry from the University of Southern California. This, together with work experience at IBM Corp. as manager of thermodynamics and kinetics studies and later as part of a team that set up Cogar Corp.'s technology division, established Sandhu's credentials for the position he took at GI in 1972 as manager of process engineering.

Previously responsible for both the development and production of GI's n-MOS and EE-PROM processes, Sandhu is now "shooting for very dense circuits using design and thin-line dimensions," he says. "We're heavily involved with X-ray lithography, which will really come into the picture below 1 micron. As soon as lab-scale equipment is available, we'll be buying it." Sandhu is aiming for fully automated processing, which he says will be practical in the next three to four years. ☐

# Ask us anything about SerenDIP® Solid State Relays.

An SSR in a DIP package? Certainly. All have logic compatible inputs. Some feature zero voltage switching for AC applications. Some are rated to switch 1.5 amps at 250 VRMS. Others are rated to 400 ma DC. Did you expect anything less from the people who introduced hybrid micro-circuits to SSR design?

But you probably have other questions about this little relay and how to use it. So go ahead. There are no dumb questions.

- ☐ How can an SSR switch both AC and DC?
- ☐ How will SerenDIP® solve my low power AC switching needs?
- ☐ Are speed, long life, and bounce-free operation the only SerenDIP advantages?
- ☐ How can I get prototype quantities quickly?

Sorry. You missed my question. Here it is. ____________________

Name ____________ Title ____________

Company ____________ Phone ____________

City ____________ State ____________ Zip ____________

**TELEDYNE RELAYS**

Ask us anything. There are no dumb questions.

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# BIOMATION K100-D

# Compare this general purpose logic analyzer with the currently accepted industry standard.

## The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

**Compare clocking speed.**

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's*. Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

**Compare capacity.**

The K100-D's 1024 word memory is *four times as deep as the 1615A's*. This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

**Compare your productivity.**

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

**The final analysis.**

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

**Hewlett-Packard 1615A**
**A very good logic analyzer**

Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data, or 24 data

**Biomation K100-D**
**The industry's finest logic analyzer**

Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data, or 32 data

**GOULD**
An Electrical/Electronics Company

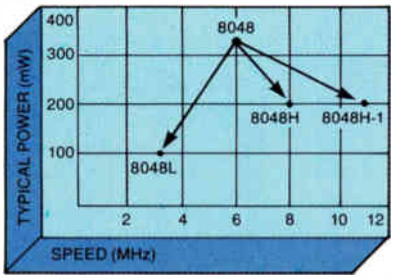
Circle 19 on reader service card


8048

# Watt Watchers

## Introducing three power saving 8048H microcontrollers and improved support tools for trimmer product development.

For years Intel's 8048 has been the industry standard 8-bit single-chip microprocessor for control applications. Now we're offering a wide selection of high-performance HMOS 8048s, suitable for expanded applications—all consuming less power than before, and all backed by extensive development support.




### New 8048Hs put on strict power diets

Our three new microcontrollers—the 8048H, 8048H-1, and 8048L—cut power consumption from 40 to 70%. Maximum operating currents for the first two are 80 mA; for the third, just 40 mA. In fact, for those applications requiring RAM-stored data to be retained, consumption at power-down falls to just 8 mA for the 8048H and 8048H-1, and to a mere 4 mA for the 8048L. These power economies are an especially important consideration when you're designing portable, battery-powered equipment. And they help cut power supply costs as well.

Because they're produced with Intel's high-reliability HMOS* technology, these new direct-replacement devices boost performance to dramatically higher levels, too. With these three new versions—operating at 3.6, 8, and 11 MHz—cycle times are reduced to less than 4.2, 1.9, and 1.4 microseconds, respectively, with performance specified over the full operating range. At 11 MHz, that's almost twice the processing speed of the original 8048. And since these units are totally compatible with existing 8048s, you can easily upgrade your current products, as well as create new designs.

### Reduce your development cycle with Intel support

In microcontroller system development, time is money. To save you both, Intel offers the most advanced microcontroller support, including real-time debugging to 11 MHz. Our Intellec® Microcomputer Development System and new microcontroller development tools can speed your product from concept to production line months ahead of your competition. And dramatically reduce your bottom-line development costs.

At the Intellec console you can write and edit application programs

quickly, using 8048 assembly language, and then have the system translate them into highly efficient machine code. Our ICE-49™ In-Circuit Emulator also enables you to debug your programs—in single steps or in real time—using high-level English-like instructions

**8048 Family—Commercial Grade****
(0° to 70°C)

| Model | Program Memory (Bytes) | Data Memory (Bytes) | Cycle Time (μsec) |
|---|---|---|---|
| 8021 | 1K ROM | 64 | 8.38 |
| 8022 | 2K ROM | 64 | 8.38 |
| 8048H | 1K ROM | 64 | 1.88 |
| 8048H-1 | 1K ROM | 64 | 1.36 |
| 8048L | 1K ROM | 64 | 4.16 |
| 8748 | 1K EPROM | 64 | 2.5 |
| 8035 | (External) | 64 | 2.5 |
| 8049 | 2K ROM | 128 | 1.36 |
| 8039 | (External) | 128 | 1.36 |

**Industrial Grade: I8022, I8035L, I8039, I8048, I8049, I8748
Military Grade: M8035L, M8048, M8748

and symbolic address references. Your software can even be executed and debugged in your prototype or production unit, with full control and monitoring from the Intellec console. There's just no more effective way to use your company's engineering resources. And no better way to reduce your development cycle.

### The Intel way to product fitness

With Intel's expanded family of HMOS 8048s and Intellec support tools, your next generation of microcontroller-based product—and sales—can now be the picture of health. To find out how, write for our Success Manual for Single Chip Microcomputer Users and the new 8048H data sheet. Or call your local Intel sales office/distributor, or Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

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Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

Circle 21 on reader service card

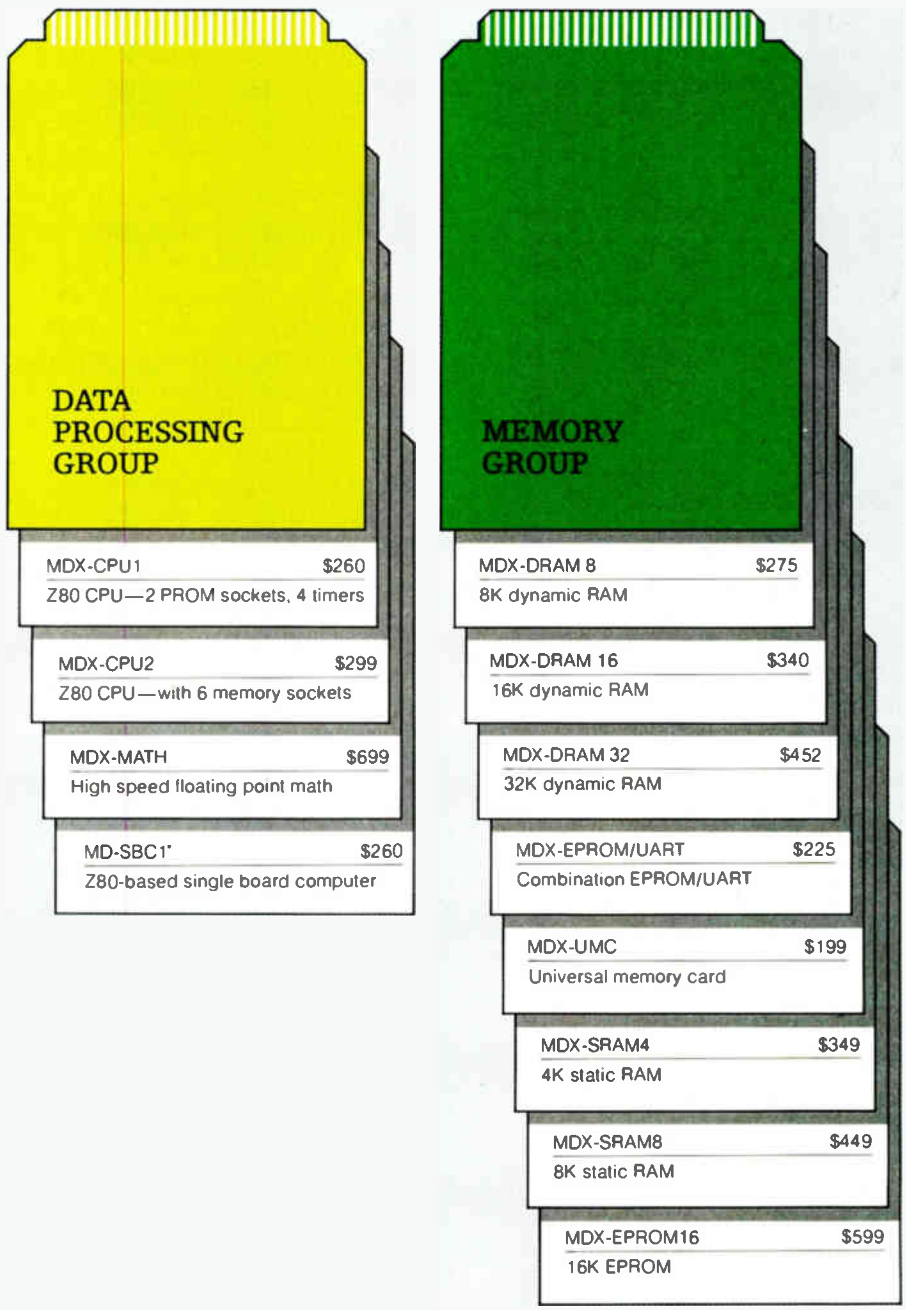
# MD SERIES MICROCOMPUTER BOARDS

With the Mostek Z80-based MD Series,™ building a custom microcomputer system is as simple as it is economical. The compact (4.5" X 6.5") boards—fully assembled, tested and debugged—virtually eliminate any hardware design effort. And since each MDX module is so specialized, the unneeded functions and subsequent higher costs of large multi-purpose boards are also eliminated.

Upgrades are simpler too, because the MD Series uses the expandable STD-Z80 BUS. As a result, design options are nearly limitless. Using either 2.5 or 4.0MHz versions, you can choose from more than 30 MD Series boards to design, customize or modify your system.

To make all of it even easier, there's a full range of powerful software development systems. Including the low cost MD PROTO kit with board level ROM-based firmware. The Matrix 80/SDT, a low cost disk-based Software Development Tool. Or our Matrix 80/SDS dual floppy disk Software Development System with optional in-circuit emulation.

For fast delivery and more information, contact your Mostek distributor listed on the opposite page. Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; (214) 323-1829. Or Mostek Brussels 660.69.24.



## The new Sputnik: part I

The word "Sputnik" is surfacing again—this time as a symbol of serious concern about the potential loss of U. S. leadership in electronic technology. When the Soviet Union launched Sputnik, the world's first orbiting satellite, in 1957, the shockwaves reverberated throughout the scientific and Government community. They served as a catalyst to the U. S. space program, caused a reexamination of technical education in this country, and resulted in the explosion of technology that we have witnessed in the last two decades.

Now some observers are calling for the same sort of shocked response to the challenge of Japan for market share and technological leadership in electronics. A recent report of a Congressional trade subcommittee concluded that Japan's rate of industrial progress and its stated economic goals "should be as shocking to Americans as Sputnik. And as with Sputnik, we should be shocked into responding to the challenge."

It is encouraging that this kind of sentiment should come from a Government source. As a matter of fact, there are portents of a growing realization on the part of Government that the increasing stridency with which the semiconductor industry, for example, is calling for help is not just the pleas of another business lobby coming to Washington looking for special privilege.

It's about time. The Japanese, by virtue of the industry-government partnership that characterizes their thrust into electronics, have captured as much as 40% of the market for such products as 16-K dynamic random-access memories and have set their sights on other high-technology market goals as well. They have accomplished this by adroitly targeting their efforts and mobilizing their resources on a national scale. And by virtue of fundamental differences between U. S. and Japanese economic systems and policies, they enjoy advantages in the market that U. S. industry has not as yet been able to counter. And it won't, without some help from Washington.

Japan's industrial policy combines a coordinated package of tax incentives, guarantees, loan subsidies, cartels, tariff rates, government procurement, and strict control of foreign activity in the Japanese market. In the U. S., there is no national industrial policy worthy of the name and our trade policies, although undergoing some changes, are still largely products of a world that no longer exists.

The old story of the farmer clobbering his mule with a two-by-four comes to mind: it's nice to be getting the Government's attention, but action on the problem is urgently required. At a recent conference convened by the Semiconductor Industry Association, Margaret Truver, deputy executive director of the U. S. Japan Economic Relations Group, warned that "U. S. industry and Government must begin to question whether or not this country can maintain its economic strength and security when it is faced with competition from foreign industries which are increasingly managed and rationalized in close government-industry cooperation." And she pointed out that such policies are not restricted to the Japanese. The French and West German governments are on a similar course.

The situation is complex. It calls into question our most basic, long-cherished traditions of a free marketplace. But the reexamination must be made—with the urgency required by another Sputnik.


# The most capable universal counter HP has ever offered.

Add it up—we think you'll find that HP's 5335A has universal counter capabilities you can't get anywhere else at any price. First, it gives you superb resolution in frequency and time interval measurements. Then, at the touch of a few keys, it will automatically measure phase, slew rate, duty cycle, rise/fall times, or do statistics. Built-in calculations and Hewlett-Packard Interface Bus operation are standard, too. And surprise, it costs just $2950*.

Naturally, the HP 5335A gives you all the frequency, time interval and totalizing measurements you usually get in a universal counter. But this counter goes on to give you remarkable performance and operating features.

For example, its automatic interpolators and reciprocal-taking frequency measurement technique give you a constant frequency resolution of 9 digits per second up to 200 MHz (or even to 1.3 GHz optionally), and a time interval resolution of 2 ns for single shot events.

You get four modes of triggering. Included is a new auto preset trigger mode that tracks variations in dc offsets. So, when offsets vary, there's no need to fiddle with trigger controls or to reprogram them in automatic systems use. And digital readout of trigger level and gate time is standard.

There's more. Six modes of arming give you outstanding versatility when measuring frequency bursts, profiles or similar dynamic parameters. The display can be smoothed by weighted-averaging for a stable readout. The built-in calculator lets you apply math (+, −, ×, ÷) to any measurement. RFI and EMC are excellent. Options include a built-in, integrating, floating DVM for $275* and a 1.3 GHz, 10mv sensitivity, C channel for $450*.

The new 5335A is truly a remarkable instrument at a remarkable price. Get the full story from your nearest HP sales office today or write, Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

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*Domestic U.S. prices only.

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02003

HEWLETT PACKARD

## Meetings

**Info 80—Information Management Conference and Exposition,** Clapp & Poliak Inc. (245 Park Ave., New York, N. Y. 10017), New York Coliseum, Oct. 6–9.

**Eighth World Computer Congress,** International Federation for Information Processing (U. S. Committee for the Eighth World Computer Congress, c/o Bowery Savings Bank, 110 East 42nd St., New York, N. Y. 10017), Tokyo, Japan, Oct. 6–9; Melbourne, Australia, Oct. 14–17.

**The Defense Electronics Market—Forecast for the 80s,** EIA (2001 Eye St. N. W., Washington, D. C. 20006), Hyatt House Hotel, Los Angeles International Airport, Oct. 7–9.

**Military Electronics and Defense Exposition,** Industrial and Scientific Conference Management Inc. (222 W. Adams St., Chicago, Ill. 60606), Rhein-Main Halle, Wiesbaden, West Germany, Oct. 7–9.

**12th National SAMPE Technical Conference,** Society for the Advancement of Material and Process Engineering (P. O. Box 613, Azusa, Calif. 91702), Red Lion Inn, Seattle, Wash., Oct. 7–9.

**21st International IEEE Symposium on Electromagnetic Compatibility,** IEEE, Baltimore Union Hotel, Baltimore, Oct. 7–9.

**Semicon/Southwest 80,** Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Market Hall, Dallas, Oct. 8–9.

**13th Annual Connector Symposium,** Electric Connector Study Group Inc. (P. O. Box 167, Fort Washington, Pa. 19034), Benjamin Franklin Hotel, Philadelphia, Oct. 8–9.

**Interkama 80—International Congress and Trade Fair for Instrumentation and Automation,** Nowea (D-4000 Düsseldorf 30, Box 320203, West Germany), Fairgrounds, Düsseldorf, Oct. 9–15.

 


# Innovative design brings new values in universal counters for systems, bench and field use.

This is much more than just another family of 100 MHz universal counters. An innovative design using a microprocessor and HP's Multiple Register Counter IC give you remarkable performance and versatility for the money: 7 digits of frequency resolution per second; continuously variable gate times; dual-mode input conditioning that optimizes both frequency and time interval measurement; input filter and time interval delay for noisy inputs; very low RFI/EMC and excellent versatility when measuring frequency bursts.

Remarkably, at their low prices, these counters use the reciprocal measurement technique, which measures the input waveform's period and inverts the result to display frequency. This gives you full resolution for all frequencies without the use of long gate times or phase-locked multipliers.

You get a full complement of universal counter measurements: frequency and frequency burst to 100 MHz (1 GHz optional), frequency ratio, time interval with resolution of 100 ns single shot and 10 ps averaged, period average and totalizing.

There are three models to select from. The new 5316A counter gives you full Hewlett-Packard Interface Bus (IEEE-488) capability including remote digital setting of trigger levels. It is metal-cased and rack mountable. And, at $1500* it is our lowest cost systems counter. The 5315B is similar to the 5316A, but without HP-IB. It costs only $1050.* The HP 5315A portable version has a rugged polycarbonate case and carrying handle. It costs $875.* Options: battery pack (5315A only), $225;* 1 GHz C channel, $250;* Offset/Normalize Module (divides and/or adds numbers to Model 5315B or 5316A measurements), $650;* higher stability time base (TCXO), $100.*

All three of these counters have the quality you've come to expect from HP— at truly remarkable prices. For the full story just call your nearest HP sales office or write, Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

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02004

HEWLETT PACKARD

# It's time to revitalize engineering

**by Bernard M. Gordon,** *chairman and technical director, Analogic Corp., Wakefield, Mass.*

Despite self-congratulatory exclamations by some industry spokesmen and predictions of uninterrupted growth for high-technology electronics companies, the long-term view is not so optimistic. Consider, for example, that much of our consumer electronics industry has been lost to foreign competition for reasons related not primarily to price, but rather to inferior quality and lack of reliability.

Many electronic products being delivered today are poorly engineered and unreliable under varying operating conditions. The problem even extends to military equipment, which is often conceived by committees and requires inordinate time to get into production.

Despite the fact that our technical colleges and universities have increased their number of graduates by over 50% in the last decade, qualified engineers who can conceive, design, and supervise in detail the development of complex products encompassing a range of technologies have become a rarity. To a large extent electrical engineers have found that their education and later apprenticeship in industry did not properly prepare them for assuming broader responsibilities in a long-term career. Instead, they have found that after engaging in a narrow specialty they are too confined to adapt to the demands of design engineering leadership.

Today even modestly complex development projects, once staffed by one or two junior engineers under the supervision of a senior engineer, require a substantial number of people. So-called project managers are confounded as development programs move forward haltingly with constant redirection instead of proceeding along well-defined paths blazed by broadly educated, self-disciplined engineers. The reasons for this situation are varied, but the result is an alarming decline in engineering productivity. Moreover, many engineers lack verbal and written communication skills, do not have a firm grasp of basic physics and mathematics, and do not even understand the meaning of leadership.

We in industry must assume strong leadership roles in the rebuilding of national design-engineering standards. We can contribute significantly to this goal both from within and outside our organizations.

In our own companies we can:

- Reject the permissiveness and complacency with which we sometimes view the breakdown or lack of engineering discipline.
- Assign product engineers responsibilities consistent with their experience and their abilities; provide structured career ladders and diverse experience, in both hardware and software, so that engineers will be able to grow in their technical knowledge, leadership, and understanding of the competitive demands put upon the product engineer.
- Explain, particularly to the young, the attention to detail and commitment to the total job required to produce a reliable product.

In our relationship with schools and with government institutions, we can:

- Work with curriculum committees to set measurable goals of knowledge, skills, and most important, attitudes that our industry should expect of the engineering graduate; help schools define requirements for mathematics, physics, basic electronics, hardware and software design processes, communication skills, and documentation.
- Recognize that the leaders in education must also have a commitment to providing well-grounded graduates in tune with the notion that education is a continuing process.
- Offer constructive criticism of well-meaning government-sponsored programs such as those that attempt to boost productivity by trying for greater quantity without better quality.

In the past, when our society has recognized danger, we have always worked together to overcome the threat. Our present problems have been decades in developing and will not be solved overnight. But, if we do not start now, it will take longer to cure. And it might be too late.

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*This is a condensed version of a lengthier text that is available upon written request from: Opinion, Analogic Corp., Wakefield, Mass., 01880.*


intel SERIES 90
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INTEL MEMORY SYSTEMS

# Packaged Memories

## Intel's Series 90 Memory System. The only one that combines system-level standardization with custom-built features.

If you're a system designer responsible for memory-intensive products, you know the problems of starting every project from scratch. Extended design cycles. Constant specification changes. Cost overruns. Component testing/integration hassles. Late documentation. Seemingly endless schedule slippages. And even when the design is finally complete, reliability remains a question mark.

These are all problems you had to put up with to get the custom-built features that would precisely match your requirements. But no more.

**Head start in memory design**

Now you no longer need to start from scratch in memory system design. Instead, start with Intel's standard Series 90 Memory System.

The Series 90 is a family of memory modules and intelligent controllers, interfaced via Intel's standard BXP™ memory bus. It eliminates the time and cost formerly required to design a special memory for each new system or performance/density upgrade.

The Series 90's family of compatible memory modules plug into the BXP bus, allowing you to choose exactly those word widths, cycle times, and memory technologies you need. Each system is factory-assembled from off-the-shelf components, and fully tested at the IC, board, and system level. So you know the system will perform according to specification, and reliability is assured.

And just as importantly, you know exactly what the system costs and when it will be delivered. No guesswork. No surprises. Just the confidence you gain from reliable, field-proven Intel® memory products.

**Flexibility for the future**

For future requirements, the BXP bus will easily accommodate Intel's new technologies as they become available. Even then, you won't have to redesign. The result? Shorter memory system design cycles plus longer life for your products.

Also with each Series 90, you can address up to 2 billion bytes of memory, with or without an ECC option. So whether you're adding more of today's memory technology or upgrading to higher density components in the future, the BXP bus stays with you.

**Performance to spare**

To give your memory systems the competitive edge, we incorporate our highest performance semiconductor memory components in the Series 90. Static memory modules using leading edge HMOS* technology to provide cycle times of 100 ns. Or our family of dynamic memory modules.

And for faster data transfer rates, our BXP bus allows you to interleave modules. Or combine both static and dynamic memory in the same system. However you configure, the Series 90 lets you achieve the highest speeds with performance to spare.

**What's in store**

We've recently upgraded the Series 90 by adding new performance categories for both static and dynamic memory boards.

So the next time you need a memory system, we urge you to compare your usual design choice with the advantages of a standardized, off-the-shelf Series 90 alternative. For assistance in making that comparison, contact your local Intel sales representative. Or return the coupon below.

*HMOS is a patented Intel process.

☐ My memory system requirements are attached. Please show me how the Series 90 can best meet these.
☐ I'll figure it out myself. Please send me:
☐ Series 90 technical information.
☐ Your handy Configuration Guide.
☐ Series 90 Application Profiles.

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# Take the Z80, 6800 or 8085 route to cost-effective STD BUS design . . .

**. . . with Pro-Log's Series 7000 STD BUS cards. By the designers who gave you the STD BUS.**

Our economical STD BUS cards are designed and built with the same expertise and commitment that led us to develop the industry standard STD BUS.

Unlike other manufacturers who limit you to one microprocessor, Pro-Log lets you design with Z80, 6800 or 8085 CPU cards. Choose from modules designed specifically to meet your system's needs: battery back-up CMOS RAM card, dedicated timer/counter card, dual UART card, 24-slot card rack, and many other system modules. We also have support hardware, manuals and design courses—all totally unbundled, so you can pick only what you need.

**Second-source designed in for reliability.**

We use only industry-standard, second-sourced parts with proven reliability. Buy 250 of any card and we give you free manufacturing rights, photo-ready artwork, parts list and assembly prints, so you can build your own cards if you wish, relying on Pro-Log as your second source.

**Send for our STD BUS technical information.**

See how easy and cost-effective microprocessor design can be. Write for our STD BUS Technical Manual, Microprocessor User's Guide, and a schedule of our design courses and free half-day micro processor economics seminars. Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940, phone (408) 372-4593.

PRO-LOG CORPORATION

**Microprocessors at your fingertips.**

Circle 32 on reader service card

# Electronics newsletter

**Tek's 8500 development aid ready to bow**

Tektronix Inc. plans to set in place next month the first block of the new, modular microprocessor development system called the 8500 series. The Beaverton, Ore., instrument maker will initially unveil **a single-user system consisting of two major parts**—one for software development and in-circuit emulation and one for managing up to 2 megabytes of floppy-disk files—that will sell for less than $1,500. In 1981, the company plans to expand the series to include a multiuser system based on the LSI-11/23, a hardware-software integration station, and support for 16-bit processors.

**Medical potion cures electronic ills**

An antistatic and bacteriostatic liquid, used for years in medical environments to prevent the buildup of static electricity, has a chance to make it big in electronic production. Called Staticide, the water-soluble liquid is being sprayed at ITT Courier Terminal Systems Inc. of Tempe, Ariz., onto bare printed-circuit boards that are to be stuffed with components and then wave-soldered. The result, says John L. Scovern, senior engineer in the test engineering and special projects group, **"is to reduce solder faults 75% and increase board yields 10%**—and that adds up to 50,000 boards a year at the rate we are making them." The liquid is manufactured by Analytical Chemical Laboratories, Elk Grove Village, Ill.

**IBM's ROM cell could serve as nonvolatile RAM**

An MOS EE-PROM that has the potential to be written into and erased so quickly that it could function as a truly nonvolatile random-access memory has been developed at International Business Machines Corp.'s Thomas J. Watson Research Center. Scientists at the Yorktown Heights, N. Y., facility have neared that elusive goal with a device that is similar to a floating-gate, avalanche-injection MOS read-only memory but adds a dual electron-injector structure to yield important performance payoffs and eliminate the need for a separate shadow array. The approach is so new that only nonoptimized single memory cells have been tested, **but data-retention time already is impressive: a computed 5% charge loss per 10 million years.**

**Intel to use own chips in special computer . . .**

Watch for Intel Corp.'s OEM Microcomputer Systems division in Hillsboro, Ore., to unveil soon a measurement and control computer on a single Multibus module that will be the **first in-house application of some key Intel chips.** The iSBC 88/40 board will use such parts as the 8088 microprocessor, the 8087 mathematics coprocessor, and the 2816 2-K-by-8-bit electrically erasable programmable read-only memory. The 8087 will reside on a smaller module, the iSBC 337, to plug into the microprocessor's socket, and an on-board 22-V supply will be used in programming the EE-PROM. The computer will be provided with a 16-channel analog-to-digital converter, as well as three multimodule expansion sockets for more plug-in cards.

**. . . and shows chip set to go into Ford's mid-1980s autos**

Saying that standardized large-scale ICs are the correct direction for semiconductor makers to take in developing automotive electronic systems, Intel Corp., Santa Clara, Calif., has introduced a chip set that will go into Ford's engine-control system in the mid-1980s. The set consists of an 8061 custom 16-bit microprocessor with a 200-ns cycle time and a read-only memory. Both are 5-V parts and are fabricated in HMOS, its high-speed n-MOS process. In announcing the development at the Institute of Electrical and Electronics Engineers' Convergence '80 show in Dearborn, Mich., Intel vice chairman Robert Noyce enumerated the virtues of standard large-scale integrated circuits as **portable software, superior quality, high reliability, and uniformity in testing and maintenance.** He lobbied for a pool of programmable circuits to serve engine control and other automotive functions.

**French mini users told that DEC may soon offer X.25**

Though it is the world's largest minicomputer maker, Digital Equipment Corp. has been a longtime holdout against the X.25 protocol for packet-switched networks springing up around the world. But now users of Transpac, France's public system that conforms to X.25, are quietly being told that the Maynard, Mass., firm may offer appropriate software this year. Little else has been heard except for hints that **DEC's approach will be regional, with its product aimed at the specific needs of X.25 users in different countries.**

**TI to purchase its voice-recognition system, firm says**

A voice-recognition system that employs some unique software techniques developed by a small Denton, Texas, company called Scott Instruments Corp. [*Electronics*, July 17, p. 154] is drawing attention from the firm's big neighbor from Dallas, Texas Instruments Inc. Though TI refuses to discuss the matter, **Scott officials report they have a signed contract under which the Dallas company will purchase about 60** of Scott's $895 Vet-2 systems, with an option to purchase a nonexclusive license to use the Scott technology in TI products.

**Codec and filter IC from Motorola scheduled for 1981**

Monolithic devices that integrate the codec and associated filter functions on the same chip represent the next step for MOS manufacturers pursuing the digital telecommunications market. Initial samples of one such chip are expected to emerge during the first quarter of next year from Motorola Inc.'s Integrated Circuit division in Austin, Texas. Though compatible with the company's current line of metal-gate complementary-MOS telecommunications devices, **the new chip will be fabricated using a denser, silicon-gate C-MOS process.**

**Addenda**

Harris Corp.'s Semiconductor Products division in Melbourne, Fla., and National Semiconductor Corp. of Santa Clara, Calif., have signed **a major cross-licensing agreement covering telecommunications products.** Initially, Harris will supply details of its bipolar subscriber-loop interface circuit technology, National its complementary-MOS codec technology. . . . Conrac Corp.'s System West division in Duarte, Calif., has supplied the New York Futures Exchange with an electronic display system featuring a unique mosaic arrangement called Macrofont: **30 23-in. industrial cathode-ray-tube monitors are stacked in three rows of 10 each,** displaying 1.5-in.-high characters. . . . The General Electric Co. acquisition of Intersil Inc. [*Electronics*, Sept. 11, p. 34] has been approved by the directors of both firms. The deal would be for $235 million. At the same time, **Gould Inc. has agreed to purchase Systems Engineering Laboratories Inc.** in an exchange of stock worth about $150 million.

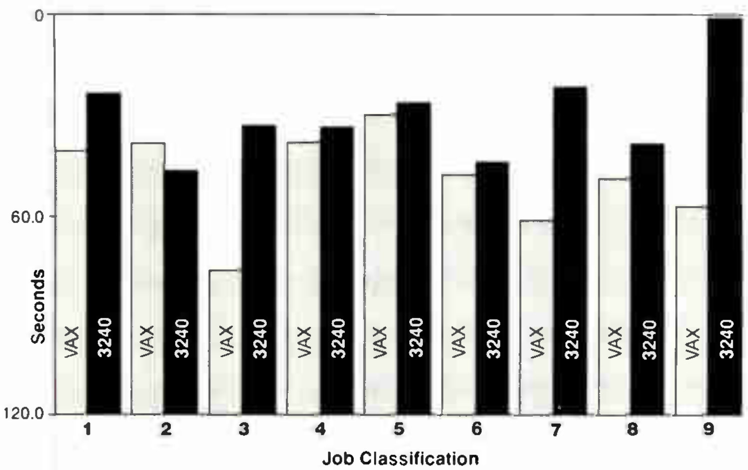
# The benchmarks prove it...

## 1. Performance Measurements

| Benchmark Name | VAX 11/780 CPU time | Perkin-Elmer 3240 CPU time | Performance Ratio* |
|---|---|---|---|
| PMS0154 | 1.140 | 0.907 | 1.26 |
| PMS0254 | 4.710 | 4.485 | 1.05 |
| PMS0354 | 9.160 | 8.990 | 1.02 |
| PMS0454 | 43.610 | 43.451 | 1.00 |
| PMS0554 | 86.420 | 86.123 | 1.00 |
| PMS0664 | 1.610 | 1.350 | 1.19 |
| PMS0764 | 7.040 | 6.679 | 1.05 |
| PMS0864 | 13.730 | 13.370 | 1.03 |
| PMS0964 | 66.830 | 66.068 | 1.01 |
| PMS1064 | 132.920 | 129.727 | 1.02 |
| PMS1124 | 1.520 | 1.306 | 1.16 |
| PMS1234 | 2.470 | 2.424 | 1.02 |
| PMS1324 | 1.310 | 1.618 | 0.81 |
| PMS1407 | 251.560 | 37.327 | 6.74 |
| PMS1507 | 50.260 | 57.657 | 0.87 |
| PMS1674 | 22.440 | 23.005 | 0.98 |
| PMS1724 | 52.550 | 53.133 | 0.99 |
| PMS1807 | 50.180 | 34.766 | 1.44 |
| PMS1907 | 32.020 | 34.679 | 0.92 |
| PMS2007 | 17.720 | 20.264 | 0.87 |
| PMS2107 | 13.450 | 20.242 | 0.66 |
| PMS2202 | 33.311 | 26.352 | 1.26 |
| PMS2324 | 121.610 | 137.997 | 0.88 |
| PMS2402 | 0.940 | 0.539 | 1.74 |
| PMS2502 | 0.720 | 0.562 | 1.28 |
| PMS2624 | 122.920 | 227.689 | 0.54 |
| PMS2708 | 4.850 | 0.961 | 5.05 |
| PMS2809 | 103.770 | 0.006 | 17295.00 |
| PMS2934 | 0.660 | 0.414 | 1.59 |
| PMS3009 | 0.230 | 0.006 | 38.33 |
| PMS3103 | 0.610 | 0.398 | 1.53 |
| PMS3202 | 4.740 | 3.923 | 1.21 |
| PMS3307 | 2.470 | 1.959 | 1.26 |
| PMS3407 | 39.190 | 7.774 | 5.04 |
| PMS3507 | 5.580 | 2.587 | 2.16 |
| PMS3607 | 156.540 | 20.077 | 7.80 |
| PMS3701 | 4.480 | 1.621 | 2.76 |
| PMS3802 | 4.060 | 2.874 | 1.41 |
| PMS3903 | 6.050 | 3.864 | 1.57 |
| PMS4002 | 9.330 | 5.505 | 1.69 |
| PMS4102 | 76.290 | 77.764 | 0.98 |
| PMS4202 | 118.490 | 125.039 | 0.95 |
| PMS4301 | 110.650 | 75.569 | 1.46 |
| PMS4403 | 1.990 | 0.739 | 2.69 |
| PMS4584 | 219.990 | 189.081 | 1.16 |
| PMS4603 | 18.640 | 16.939 | 1.10 |
| PMS4701 | 0.350 | 0.077 | 4.55 |
| PMS4802 | 0.830 | 0.880 | 0.94 |
| PMS4934 | 0.340 | 0.050 | 6.80 |
| PMS5008 | 0.430 | 0.168 | 2.56 |
| PMS5108 | 98.950 | 55.419 | 1.79 |
| PMS5208 | 0.900 | 0.917 | 0.98 |
| PMS5308 | 0.330 | 0.029 | 11.38 |
| PMS5408 | 2.080 | 1.697 | 1.23 |
| PMS5502 | 1.130 | 2.180 | 0.52 |
| PMS5602 | 207.140 | 198.685 | 1.04 |
| PMS5703 | 585.170 | 254.545 | 2.30 |
| PMS5824 | 18.740 | 18.194 | 1.03 |

*Performance Ratio = VAX 11/780 CPU time / Perkin-Elmer 3240 CPU time

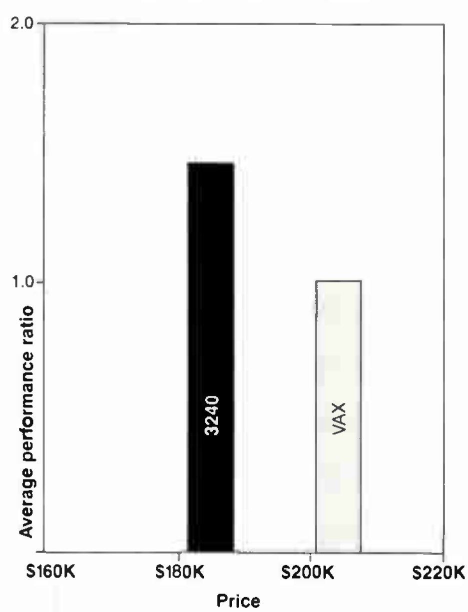
## 2. Perkin-Elmer 3240 vs. VAX* Average Time by Job Classification




1. Integer
2. Single-precision
3. Double-precision
4. Math functions
5. Single-precision whetstone timings
6. Double-precision whetstone timings
7. Arrays
8. Job mix
9. Compiler technology

*VAX is a trademark of Digital Equipment Corporation

## 3. Proven Price/Performance




The configurations tested were 2 MB of memory, 67 MB disc, 75 ips tape, Floating Point Processor, CRT terminal, battery backup, and system software. The 3240 had a Writeable Control Store and Fortran Enhancement Package, while the VAX 11/780 had a Floating Point Accelerator.

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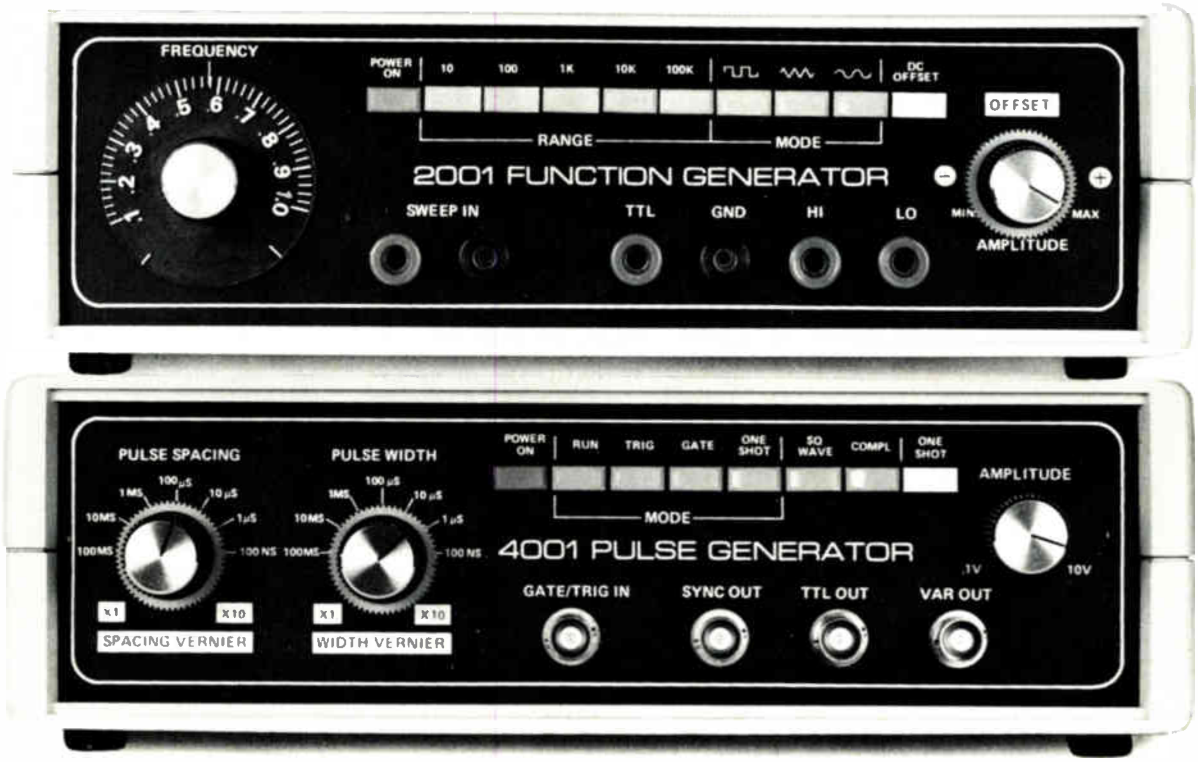


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# Intel and NEC heat up the race in 64-K RAMs

*by John G. Posa, Solid State Editor*

New chips have big areas as their makers aim at easy manufacturability and relaxed operating margins

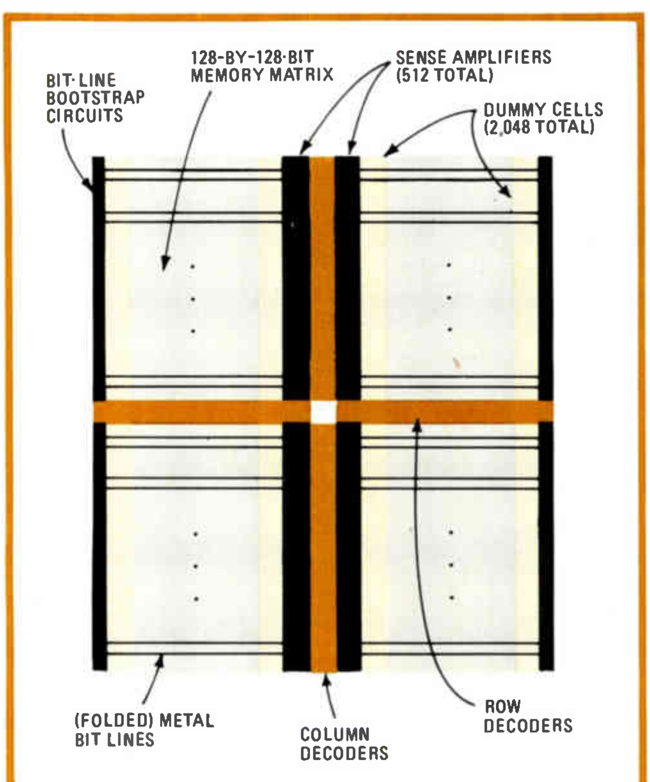
**The 64-K dynamic** random-access memory race is heating up now, with two anxiously awaited arrivals—from Intel Corp. and the Nippon Electric Co.—about to enter. In addition, other manufacturers like Mostek Corp. are realizing significant yields on long over-due chips.

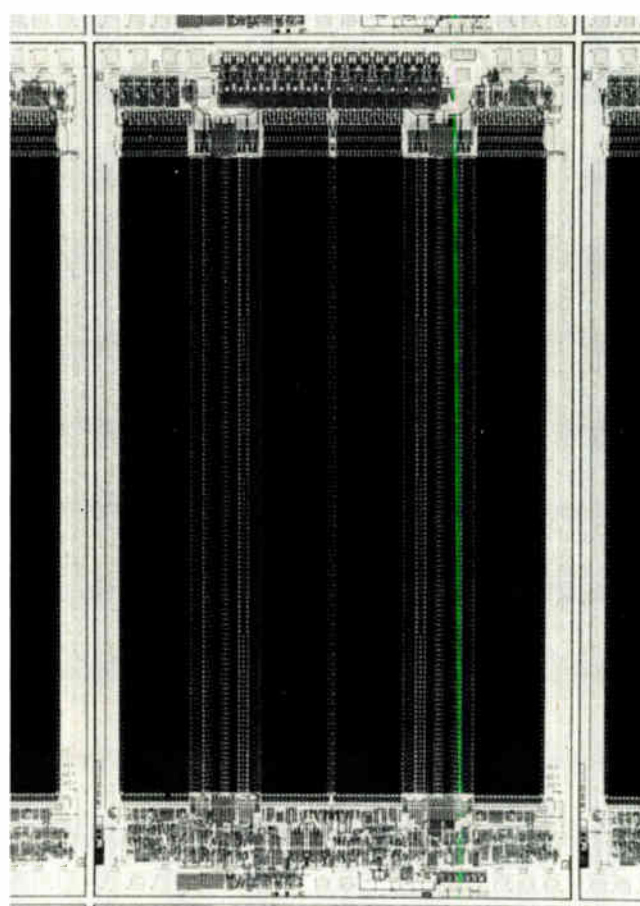
Unlike the opening round of 64-K RAM announcements, which stressed "being first" and "having the smallest die," the latest buzz words are "most manufacturable" and "highest margins" on internal operating specifications. Indeed, though the earlier companies might have been loath to disclose a chip size in excess of 40,000 square mils, Intel's 4164 is 47,000 mil², and NEC's μPD4164 a whopping 50,920 mil².

"We feel we have done everything we could do—within reason—to maximize the margins on the part," submits Sunlin Chou, Intel's manager of dynamic RAM engineering and memory components. "Power dissipation will be on the high side," admits Kirk MacKenzie, strategic marketing manager of memory components in Aloha, Ore. "We've done that to improve quality and reliability." The 335 milliwatts maximum is more than most 64-K RAMs'.

Intel's 64-K part, like Motorola's

**New dice.** The 64-K RAMs of Intel (below) and NEC (right) stress producibility. Intel goes for bootstrapping and full-sized dummy cells. NEC chooses conservative layout and an anti-alpha coating.



[*Electronics*, Feb. 15, 1979, p. 141], uses folded metal bit lines and is partitioned into four quadrants (see figure, p. 39). Its double-polysilicon cells, however, are more akin to Hitachi's [*Electronics*, July 31, 1980, p. 103]. To increase margins, the 4164 includes active bit-line bootstrapping and full-sized dummy cells.

As do most RAM makers, Intel boosts—bootstraps—its word lines above the power supply voltage ($V_{DD}$) to store more charge. But it further bootstraps the 4164's bit lines to restore a $V_{DD}$-plus level to the cells after a refresh. "It takes a couple of transistors and a capacitor at the end of each bit line that theoretically could be chopped out at the expense of margins," says Bob Abbott, 4164 program manager.

For a more solid sense-amplifier reference, Intel moved to full-sized dummy-cell capacitors, and "to track alignment with the storage cells, we have dummy cells on each side, and we select the one that is facing the same direction as the storage cell," Abbott says.

**Noise.** Alpha-particle noise is one reason designers are building in higher margins. The present specification for soft errors is 1 in $10^6$ per hour. Intel says that it "has the option to get down to this level," hinting at an anti-alpha overcoat. Motorola, TI, and others have recently disclosed that they will employ polyimide coatings to shield against alpha particles [*Electronics*, Sept. 11, p. 41].

NEC is using a silicone coating over 100 micrometers thick on its 64-K RAM (see photograph, p. 39), aiming at surpassing the industry alpha-error specification. Also, NEC is conservative with layout for a high bit-line-to-cell-capacitance ratio of 9:1, further guarding against noise. The architecture looks like that of a 256-K RAM that the company recently described [*Electronics*, May 22, 1980, p. 129].

NEC also grounds the upper plates of the storage capacitors in its array—instead of tying them to the power supply—to subdue power fluctuations. Mostek does the same thing in its 64-K RAM.

**Delay.** The Mostek MK4146 was announced over a year ago, "but margins and specs weren't there, so we went through an iterative process," says Sam Young, the Carrollton, Texas, firm's strategic marketing manager of memory products. Other Mostek insiders attribute the tardiness partly to the loss of key people like Paul Schroeder to a recent startup, Inmos Corp.

Now "we have working devices in house and consistent yields," states Young, who says that a fourth-quarter introduction is in store, followed by volume production next year. Like Intel, Mostek is bootstrapping its bit lines for more signal strength.

In addition, Young points to "a unique, revolutionary sense amplifier that is far more sensitive than what we've done in the past." In fact, "we don't plan on coating the part right now—through design, we have enough signal," he says. "We will be the only manufacturer to initially offer [the RAM] in plastic."

## Business

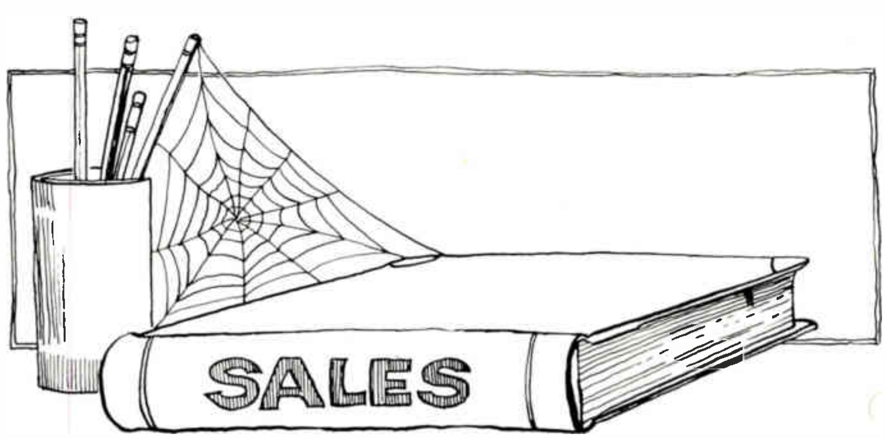
# Recession reaches electronics sector as distributors' midyear sales drop

Amid mounting signs that the U. S. recession is finally hitting the electronics industries, distributors around the nation are reporting that their sales started to fall sharply in the spring. The last month has seen some improvement, but few officials are ready to predict reigniting of the boom their industry has felt ever since the 1974–75 recession ended.

What has hit the distribution industry is the almost simultaneous occurrence of all the ills that can plague the business in a downturn—"cancellations, stretchouts, and price declines," sums up Sidney L. Spiegel, chairman of the Wyle Distribution Group, El Segundo, Calif. While distributors are feeling the effects of increasing supplies of hard-to-get parts, even more they are experiencing a drop in demand.

One eye-opener is that firms operating in the supposedly recession-resistant Southwest felt the decline perhaps more than other areas. In Texas, for example, Joseph Semmer of Hall-Mark Electronics Corp. reports April was the last month when the key book-to-bill ratio held above 1:1. The ratio has edged up from under 0.8:1 in June to about 0.96:1 now, says Semmer, the director of semiconductor business development for the Dallas firm.

**West.** In Los Angeles, Jack F. Darcey, president of Kierulff Electronics, a national firm that is strong in the West, calls July sales a "disaster," dropping nearly 15% below July 1979. Other western distributors agree; an exception is giant Hamilton/Avnet, whose nationwide sales are more than triple those of its



competitors.

Bookings for July and August actually ran ahead of the same period a year ago, claims William C. Cacciatore, executive vice president for worldwide operations. Top officials at other firms, however, doubt that Hamilton/Avnet's sales were ahead, pointing out that booking an order does not mean it is solid.

**Ratios.** What distributors report should be felt among both their suppliers and their customers. However, semiconductor manufacturers have remained tightlipped about their sales. The Semiconductor Industry Association does report that its member firms have book-to-bill ratios of about 0.75:1. The ratio, however, is an imperfect measure, since there is no standardization on how orders and shipments are reported.

On the user end, minicomputer makers are reporting big production cutbacks because of sharp order falloff. Such a slowdown is bound to ripple back to distributors and to integrated-circuit makers.

Unlike the 1974–75 downturn, there has been little of the double ordering that greatly inflates backlogs and subsequently hurts suppliers when cancelled. Rather, shortening lead times from months to weeks on hard-to-get parts has had two adverse effects.

First, it chops out months of backlog that were counted as a cushion. Second, distributors' customers themselves carry much smaller inventories because they are able to get quicker deliveries. Many officials think that decreased inventories are the dominant factor in this slide in distributor sales.

**A price drop.** On top of slower sales, price declines in previously short-supply large-scale integrated memories, which make up perhaps 20% of distributors' volume, are forcing them to run harder to stay even. How tough a job that can be is noted by Hall-Mark's Semmer, who says an order booked today for 16-K random-access memories is worth only a third of its value three months ago.

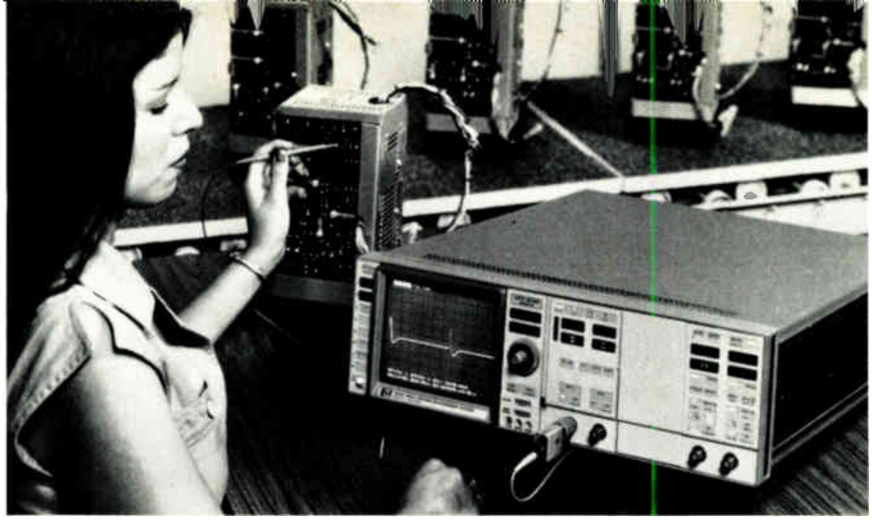
He and others hope price pressures do not spread to other parts. But the history of the semiconductor business during recessions hints otherwise, they admit.

For all the rapidity of the downturn, most distributors maintain an optimistic outlook, although none sees a fast return to 30% growth rates. If a consensus exists, it foresees flat to slightly increased sales for the rest of the year and softness (defined by Kierulff's Darcey as a 10% increase) through the first half of 1981.

These forecasts are based on hopes that the decline bottomed in midsummer and that customer inventory rebuilding, which seems to be stirring in early September, will lead the way. The distributor officials see current troubles as temporary, with a new fast-growth track opening up in late 1981. **-Larry Waller**

**Instrumentation**

## Microprocessor paths diverge for scopes



**Easy to run.** Hewlett-Packard's two-channel 100-MHz 1980A scope uses an 8085 to simplify operation for the unskilled user.

Thanks to the microprocessor, that most analog of instruments—the oscilloscope—is steadily getting smarter. One path to take is found in Hewlett-Packard Co.'s just-introduced 100-megahertz 1980A scope, which goes for simplified all-digital controls and automatic ranging.

In contrast, Tektronix Inc. uses the processor in its 400-MHz 7854 to enhance scope performance greatly. Whereas HP's Colorado Springs (Colo.) division opted for the 8-bit 8085 to simplify setup for less sophisticated users, Tektronix chose the 16-bit TMS 9900 to permit extensive waveform manipulation by the engineering designer.

HP product manager Wayne Gutschick sees the 1980A "growing into traditionally nonelectronic industries, such as the auto industry, where people who may never have seen a scope will have to use them." Tektronix, on the other hand, maintained much of the analog circuitry and traditional appearance in the 7854 [*Electronics*, Feb. 28, p. 39] so as "not to shock the user" with an instrument "unrecognizable as an oscilloscope," says Val Garuts, principal designer of the Beaverton, Ore., company's scope.

**One knob.** The contrast is immediately evident on the face of the 1980A (see photograph). Gone are the multiple knobs and push buttons to which most engineers have become accustomed. Instead, there is a single control knob whose function is determined by which of the function keys is pressed.

The digital design also allows HP to offer autoranging. When the autoscope key on the front panel is pressed, the 8085 examines the input for vertical amplitude, horizontal sweep speed, and position and selects settings to produce display.

**Autoranging.** Certain functions that the user may want to select, such as input coupling and triggering, can be entered and preserved during the autoscope sequence. Although the autoranging feature is particularly beneficial to an unskilled operator, its attraction to any scope user cannot be denied.

By means of commands sent to them through an IEEE-488 interface, both scopes can display text telling a user how to perform measurements. However, only in the 1980A may all settings be programmed through the interface. It can also transmit some measurement data to a computer.

**Storing.** But the unit cannot currently store, send, and receive waveforms as can the 7854, an important feature for a system scope. HP plans to add waveform digitizing and transmission in the first quarter of 1981, using two field-installable cards that provide about 2-K of random-access memory. As that RAM capacity is less than in the 7854, it will not store as many waveforms.

Additional measurement routines will be added to the 1980A through 4-K read-only memories, of which the unit can accept four. At present, just one is offered—a $500 sequence ROM that lets the user program up to 25 front-panel inputs and recall them in sequence.

Whereas the $10,500 7854 mainframe requires plug-in function modules to be operational, the $8,500 1980A comes ready to run. Still, users of Tektronix' popular 7000 series most likely have many such plug-ins on hand, and the company offers a wide range of them—the 7D02 logic analyzer is the most recent. HP has set aside a single front-panel slot for adding enhancement modules; at present it offers a $2,000 plug-in that adds another two channels to make the 1980A into a four-channel unit. **-Richard W. Comerford**

## Microsystems

# Coprocessor board supercharges Apple II by harnessing the power of new 6809E

Users of the Apple II personal computer will soon be able to harness the power of the 6809E microprocessor to perform multiprocessing. A recently formed Santa Barbara, Calif., company, Stellation Two, is introducing a plug-in board holding the new Motorola processor and all the interface logic that add up to a true multiprocessing system.

The 6809E, designed for just such setups, can execute programs much faster than the Apple II's 6502. "If we figure the average Apple user has $3,000 invested in his system, then for an additional investment of about 10% he can have a processor that is twice as fast," says James A. Hinds, president of Stellation Two and a founder of Nestar Systems Inc., the Palo Alto, Calif., networking software house.

**Upgrade.** When Stellation Two's board becomes available in limited quantities late this year, Apple II users may find that they have processing power equal to or exceeding that of the recently introduced Apple III. Making this possible is the 6809E, part of Motorola's ambitious plans for the 6809 family [*Electronics*, May 8, p. 48] and formally unveiled at last week's Wescon show.

In the Stellation Two system, the 6809E acts as the bus master while the standard Apple processor uses the common bus during the time slices when the 6809E is doing internal operations. In this way the processors run simultaneously.

The E version of the 6809 has several features that facilitate coprocessing. External clock inputs to the chip allow it to run off the Apple clock circuits, ensuring that the two processors operate in synchronization. Also, an advance-valid-memory-address pin notifies the 6502 that the 6809E will need the bus during the next clock cycle; when that line goes active, circuitry on the Stellation Two board takes the 6502 off the bus so that the coprocessor will have access to common memory and input/output channels.

**More.** Other multiprocessing features of the 6809E include a pin that signals that the processor is performing internal computations; one that puts the address, data, and control pins in the high-impedance state; and one that notifies the external world that the next cycle will be an operation-code fetch.

The board allots 80% of the bus time to the Motorola chip. However, it does let the 6502 interrupt, should it need access to the bus for a time-critical task. An on-board read-only memory stores the reset vectors for both processors, as well as the multiprocessing software.

There is at least one other plug-in

### 16-bit/8-bit machine lacks only ROM

Another 16-bit microprocessor has found its way into an 8-bit package. The TMS 9995 from Texas Instruments Inc. is software-compatible with the 9900 family of 16-bit processors but has an 8-bit interface with memory. The 8-bit data bus and separate 16-bit address bus allow the use of byte-wide read-only memories, which, along with the 9995's other features, makes possible a complete 16-bit computer with only two chips.

The 9995 executes all the regular 9900 instructions but at a much faster rate, as a result of the 6-megahertz clock and internal optimizations. It also adds four instructions, including a signed multiply/divide. In addition, it contains 256 bytes of random-access memory, clock-generation circuitry, and prioritized interrupts, all features that qualify it as a ROM-less microcomputer. As a 16-bit chip with an 8-bit data bus, it joins the 9980, Intel's 8088, and Motorola's 6809, which differs from the others in being a scaled-up version of an 8-bit processor. However, only the 9995 has the on-board features that make possible a two-chip system.

Since the 9995 uses the memory-to-memory architecture of the 9900 family, it keeps its registers in general memory, which is usually slower than on-chip registers. The longer register-access time is the reason that the architecture has been regarded as inherently slower than those using on-chip registers. However, the 9995 can avoid the penalty of off-chip registers by using the on-chip 256-byte RAM for registers. **-R. C. J.**

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processing card for the Apple II. However, the Z80-based board from Microsoft in Bellevue, Wash., does not operate in parallel with the Apple II's 6502, as does the Stellation Two offering. Thus one of its processors will be idle while the other is using the bus.

However, Microsoft does offer extensive software options: Basic, Fortran, and soon Cobol, as well as the proven CP/M operating system. Stellation Two's coprocessor board initially will be offered with only the low-level software necessary to coordinate the multiprocessor synchronization—although Hinds says negotiations for system support are under way with some 6809 software houses. -R. Colin Johnson

## Components

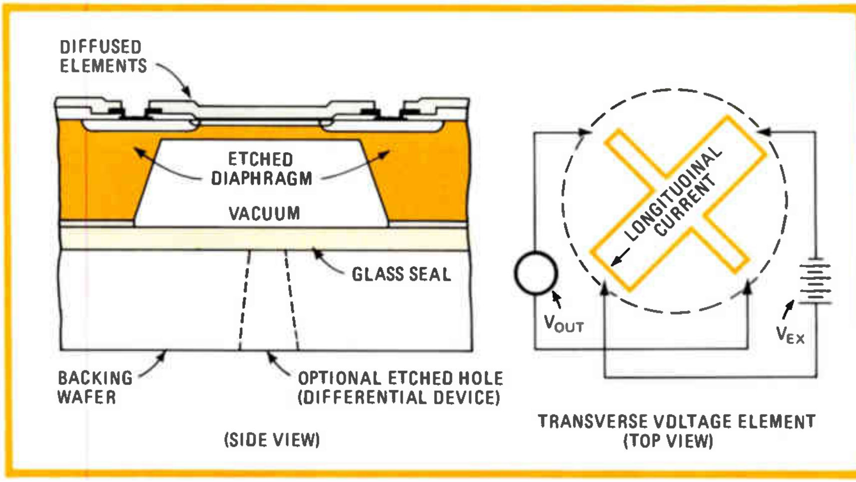
# X-shaped sensor simplifies transducer

Bringing down the price of monolithic silicon pressure sensors has proven a tough problem to tackle, but Motorola Inc.'s Semiconductor Group thinks it is set to score a touchdown. Engineers there have sidestepped the cost problem by devising a simpler piezoresistive element that fits into an inexpensive plastic package.

The Phoenix, Ariz., group's new offering is a single-element strain-gage transducer pegged to sell for $2 to $5, depending on quantity. The next cheapest comparable monolithic pressure transducer costs around $50, Motorola says.

**Others.** While other makers of transducers acknowledge they are working on simpler monolithic units, none is willing to talk about an approach that so deeply cuts the cost. Much industry attention is going toward perfecting packages that would fit many applications and thus allow a uniform testing procedure. Here, too, Motorola is set to make its mark with the new part.

All silicon pressure transducers are piezoresistive devices, producing a change in output voltage when a sensing element's resistance changes. In the conventional pressure sensor, the sensing element is one of four resistors in a Wheatstone bridge circuit.




**A cross, not a bridge.** Motorola Semiconductor has devised a monolithic silicon pressure transducer with a simple cross-shaped sensing element (shown in top view at right).

In the Motorola part (see figure), the sensing circuitry is a single p-type silicon element that is cross-shaped, giving rise to the part's name, X-ducer. A constant current passes through the element's longitudinal axis, generating a transverse voltage across the latitudinal axis. When pressure is applied, this output voltage changes.

**Orientation.** In the traditional approach, the piezoresistive element is oriented to maximize the diagonal term of the electric field vector and to minimize the nondiagonal terms, thereby minimizing transverse voltage changes. Acting on a 20-year-old proposal for simple sheer-stress pressure measurements, the Motorola engineers orient their sensor for maximum nondiagonal terms.

The resulting X-ducer produces a 65-millivolt maximum output at 1 atmosphere of differential pressure when excited by a 3-volt dc source. Its sensor is much cheaper to make than the traditional device, says James Herman, marketing manager for sensors and fiber optics.

"With the Wheatstone bridge approach, you must generally match resistor temperature coefficients to within 0.1%, since silicon has a nominal TCR of 1,000 parts per million per °C," he says. "This is cumbersome and costly," because it requires laser trimming or exacting ion implantation to balance the resistors.

A bonus of the new design, contributing to the low price, is its simplified packaging, which also leads to easy testability, says John Gragg, the group's operations manager for sensors. "The plastic package used, which is really a chip-carrier, provides simple terminations of the transducer's leads, simplifying testing by automatic equipment," he points out.

Gragg acknowledges that the plastic limits the X-ducer's pressure range. But he hastens to add that automotive and process-control applications use pressures in the 3-to-15-pound-per-square-inch range.

Motorola also points to the good performance of its new offering. The part is nearly free of hysteresis, with a worst-case repeatability of within ±1% and full-scale temperature coefficient of −0.2%/°C. It has a maximum zero pressure offset of 35 mV and a sensitivity of 3.42 mV per square inch. -Roger Allan

## Peripheral equipment

# Compact Winchester packs features in

Twelve years ago Sam Irwin built a better mousetrap when he pioneered the intelligent terminal at Sycor, and

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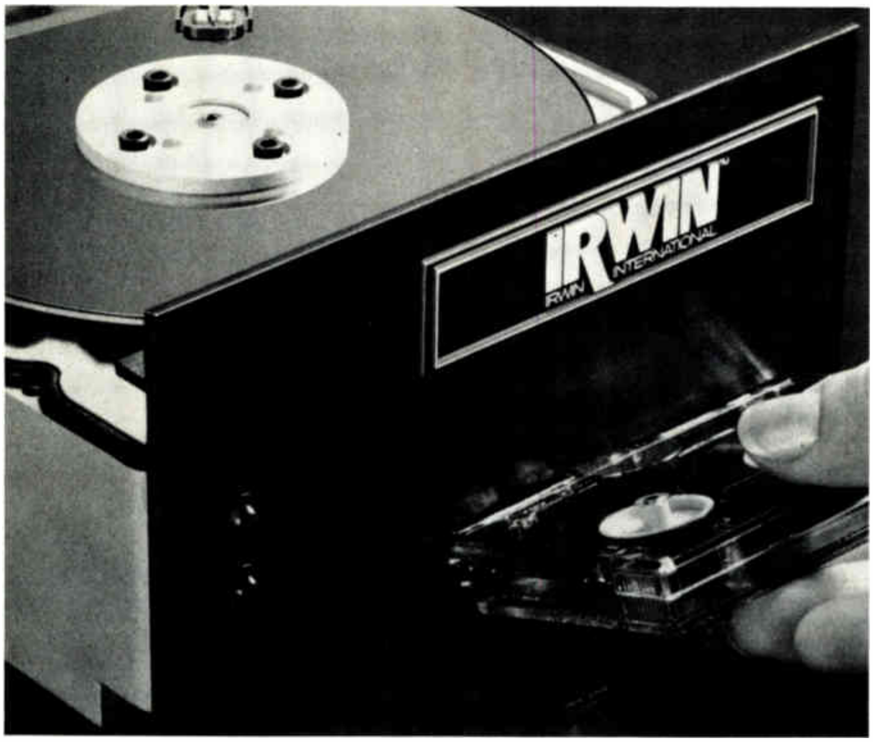
*—Anthony Schiavo, President*


Circle 45 on reader service card




**Two in one.** The Irwin 5-1/4-in. Winchester disk drive includes a cartridge backup and has twice the storage capacity of other micro-Winchesters and much faster access times.

now he may have done it again. The mousetrap this time is a 5¼-inch Winchester disk drive with an integrated tape cartridge backup.

From his new company, Irwin International, Ann Arbor, Mich., he is announcing a product with four major features that will, for now, put it out front in the market in small disk drives. It has twice the storage capability of the other 5¼-in. Winchester drives, the first integrated tape cartridge backup to be found in a 5¼-in. Winchester, much faster access times, and a per-kilobyte price competitive with the 8-in. Winchester drives.

**Storage.** The Irwin 510's capacity is 12.3 megabytes, unformatted. The integrated tape backup will hold the entire 10-megabyte formatted capacity on one cartridge. It will read or write the total cartridge in less than four minutes.

The average access time of the disk is 25 milliseconds, half that of 8-in. Winchesters and about seven times faster than that of the first 5¼-in. drive, Shugart Technology's ST506. The price, at $1,500 for quantities of 500 (unit price is $2,500), results in a cost per kilobyte of 12.2¢, compared with 14.5¢ for the ST506 and a range of some 9¢ to more than 15¢ for the 8-in. drives.

**Microprocessors.** The Irwin 510's designers achieved the high density and fast access of both disk and tape in part by a generous application of microprocessor control. The fast positioning of the disk head boosts speed, and because it is highly accurate, tracks can be closer together.

Irwin will not specify the type or number of microprocessors that are used at least to control the disk head and tape head servo positioners and the rotation speed of the disk and tape spindles. The result is the highest track density yet announced in a small disk—900 tracks per inch.

Irwin is no stranger to computer peripherals, since he built Sycor into a leading supplier of intelligent data-processing terminals. In 1978, that company was bought by Northern Telecom Inc.

The micro-Winchesters, as the 5¼-in. drives are called, will fit into the space of a 5-in. floppy-disk drive and should see applications in small computer systems. There is considerable interest in the technology of these small units [*Electronics*, June 19, p. 104], but only two other manufacturers have announced products: Shugart Technology and Tandon Magnetics Inc.

The new Irwin product draws some admiration from competitors—and some caveats, as well. "It sounds like a very high-performance product with pretty aggressive pricing," says Finis Conner, executive vice president of Shugart Technology.

**Caveat.** However, Conner argues, state-of-the-art technology sometimes has timebombs. "Shugart Technology's philosophy is not to take advantage of the very latest in magnetic and drive technology at the sacrifice of maintainability and manufacturability," he remarks.

Similar praise for the impressive specifications of the Irwin drive comes from Dave Britton, president of the drive designers Britton-Lee Inc. and himself the designer of the first 8-in. Winchester drive on the market, International Memories Inc.'s 7710. He also sees another stumbling block.

"If you have the team that can design a good product, do you also have the team that can put the product into production and also the team to market it?" he asks. "This is the same problem everyone in the Winchester business faces," especially production, because the drives difficult to manufacture.

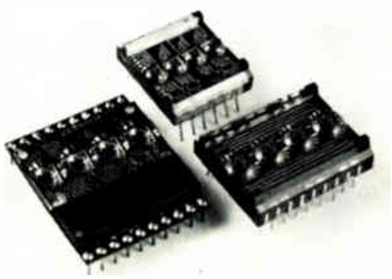
Irwin International's response is to schedule delivery of evaluation producton units for early 1981, with production set for May at the latest. The company expects to be manufacturing 300 of the drive a week, all spoken for by users, by the end of next year. **-Tom Manuel**

## Business

# Next 20 years to see fiber optics flower

Tumbling component prices in the next two decades will bring an explosion in demand for fiber-optic systems. The market is expected to soar

# The revolution in Intelligent Display.™



We live in a world of machines, and most of them can communicate to us only in rudimentary terms: a flick of a needle, a lamp, a gauge.

The microprocessor provided the brains for more sophisticated man/machine communications. But prohibitive costs have limited alpha-numeric readouts to the CRT's of larger systems.

The Litronix Intelligent Display* will change all this.

Thanks to low cost, the Intelligent Display makes it practical for all kinds of machines to talk to us in *our* language. Litronix' Intelligent Display has started a revolution in product design which is just now gathering momentum.

### What is the Intelligent Display?

The Litronix Intelligent Display is basically an alpha-numeric readout with built-in random-access write-only memory, built-in character generator (ROM), multiplex circuitry, monolithic LED chips, and all the display-driving circuitry.


ACTUAL SIZE OF THE DL-1416 AND DL-2416

Interface the Intelligent Display just like a RAM, which means it is compatible with any known modern computer. In addition, it requires just a 5v power supply.

*Intelligent Display is a trademark of Litronix.

### How it simplifies your system.

There are two basic reasons to consider the Intelligent Display: (1) you want to use alpha-numeric displays where they are not now being used, or (2) the alpha-numeric displays now in use involve too much drive circuit complexity and cost.

The Intelligent Display simplifies your system by reducing the total number of individual parts and inter-connections needed. Compared to a typical dot matrix display, the Intelligent Display is a system designer's joy. You don't need additional PROM, RAM, interface circuitry, decoders, digit drivers, segment drivers, etc.

The Intelligent Display is bright, highly legible, and offers solid state reliability.

Total cost of the Intelligent Display system is substantially less than other approaches. Savings of over 50% are frequently possible. This is where the revolution begins. Because the Intelligent Display now makes it practical to use alpha-numerics where none were practical before.

### Machines that talk.

Virtually any machine that uses a microprocessor is fair game. This includes process control machinery, test instrumentation, and consumer products of all sorts.

Consider the automatic phone dialer. Using the Intelligent Display, you could store literally hundreds of numbers and activate any one simply by typing in any five letter sequence. This sequence might be a person's initial and the first four letters of his last name. If you have ten numbers to call, the machine could be programmed to try them all in sequence...and display the entire name of the first person who answers.

The Intelligent Display is infinitely flexible. It is as versatile as the software which controls it.

Another use is on future automobile dashboards. One Intelligent Display can serve as a multiple warning indicator, reporting on every condition in the car...from the status of your brakes to whether all your tail lights are on. Multiple failures could be shown sequentially or by priority. Other functions can be added later with only a software change. No change in panel layout or wiring is necessary.

In the consumer field microwave ovens, stoves, washing machines, and dozens of other appliances can display directions and status reports in simple English.

### The Intelligent Display is available now.

Litronix currently has a growing family of 4-character Intelligent Display modules. One recent addition, the DL-1414, has 112-mil high characters and draws only 6 ma per character. A 20-character line is only 3½" long...ideal for hand-held, battery powered devices.

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**THE LIGHTS FANTASTIC**

Circle 47 on reader service card

from its existing $275 million level to $6.5 billion by 1990 and to $40 billion by 2000, according to a forecast by Gnostic Concepts Inc.

North American production will supply slightly more than half this accelerating demand—led by such firms as Corning Glass Works, International Telephone & Telegraph Co., and Western Electric Co. The remainder will be supplied by competition in Japan, Western Europe, and elsewhere, according to Jeff D. Montgomery, president of the Electronics division of the Menlo Park, Calif., market researchers.

Montgomery and co-author Frank W. Dixon are to address the four-day meeting of the Society of Photo-Optical Instrumentation Engineers that begins Sept. 29 at the Huntsville, Ala., Von Braun Civic Center. The market estimates in 1980 dollars include an inflation factor of about 300% for the 20-year period.

**Impact.** Montgomery likens the impact of future fiber-optic systems on telecommunications to that of semiconductors on vacuum tubes in the 1960s. As spectrum congestion increases in the 1980s, limiting the expansion of satellite communications and terrestrial microwave systems, fiber-optic links will begin to replace them, becoming a major market factor by 1990.

Lower charges for broadband transmission circuits made possible by fiber optics should rapidly expand markets for private facsimile networks, electronic mail, and video telephones, according to Montgomery. Facsimile transmission times using copper cable are now measured in minutes, for example, but broader fiber-optic bandwidths should drop these to seconds and ultimately tenths of a second.

**Optical ICs.** Another spinoff of the market boom, says the study, will be optical integrated circuits already "being pursued by dozens of major laboratories, with a cumulative total of about $50 million invested to date," including over $15 million in Federal funding. Major applications for these ICs, in addition to cable systems, will come in optical signal switching and data processing after

## News briefs

**Datapoint extends content addressing to office systems**

Datapoint Corp. is extending the capability of the content-addressable file-access feature designed for use in its integrated electronics office package. The San Antonio, Texas, supplier of small-business systems is adding that capability to data-processing files as well. The Datapoint software feature known as AIM, for associative index method [*Electronics*, Dec. 6, 1979, p. 44], is included as part of Datashare 6—the newest version of the company's business timesharing system. Requiring a 14% memory overhead, AIM allows files to be searched on a free-form basis for all items containing user-specified combinations of key words, phrases, or numbers. It thereby eliminates the need for complex query programs or the maintenance of multiple-index record keys that are required by traditional access methods.

**National imports big Hitachi mainframe**

Sporting a performance rating about twice that of an IBM 3033, the AS/9000 IBM-compatible mainframe computer was unveiled by National Advanced Systems Corp. of Santa Clara, Calif. It had been introduced in Japan earlier this year as the Hitachi M-200H, and word was out that the National Semiconductor unit would sell it in the U. S. [*Electronics*, Aug. 28, p. 68]. The price of $4.52 million for the 16-channel, 16-megabyte memory version gives it about a 40% price-performance edge over the IBM mainframe. The AS/9000 has a 40-nanosecond machine cycle time and 64-kilobyte cache buffer storage and can use IBM's latest disk drives, the 3375 and 3380. National picked up the Hitachi mainframe line last year after acquiring Itel Corp.'s Data Products group. The Itel unit, which also sold IBM-compatible computers made by National, suffered heavy losses after IBM introduced its 4300 series.

**C-MOS memory module fits STD bus**

Pro-Log Corp. of Monterey, Calif., will expand its line of memory cards compatible with the STD bus to include complementary-MOS modules. Its model 7701 cards will be loaded with up to 16 kilobytes of either n-channel or complementary-MOS random-access memory or pin-compatible programmable read-only memory. The 16-kilobyte C-MOS RAM version, costing $940, has buffered STD bus lines. The C-MOS card with static RAMs of the 6514-2 type has an access time of 275 nanoseconds. Another C-MOS RAM card, the 7703, provides similar access times and has a lithium backup battery for a minimum data retention of two years. Both the 7701 and 7703 lines operate from a single 5-volt power supply, and the 7703 line has automatic memory protection on loss of power.

**Israeli firm looks for openings in U. S. consumer market**

Determined to double its exports to $12 million in the coming fiscal year, Amcor Ltd., of Tel Aviv, is mounting a push to penetrate the U. S. consumer market. The company is a broad-based producer of consumer electronics products and electrical appliances, but because these markets are already crowded, it is looking for less competitive openings. The first offerings introduced are Freshen Aire, an ionizer that cleans room air, and a line of electronic insect exterminators. Amcor is also planning to sell particle ionizer modules to makers of TV sets and air conditioners.

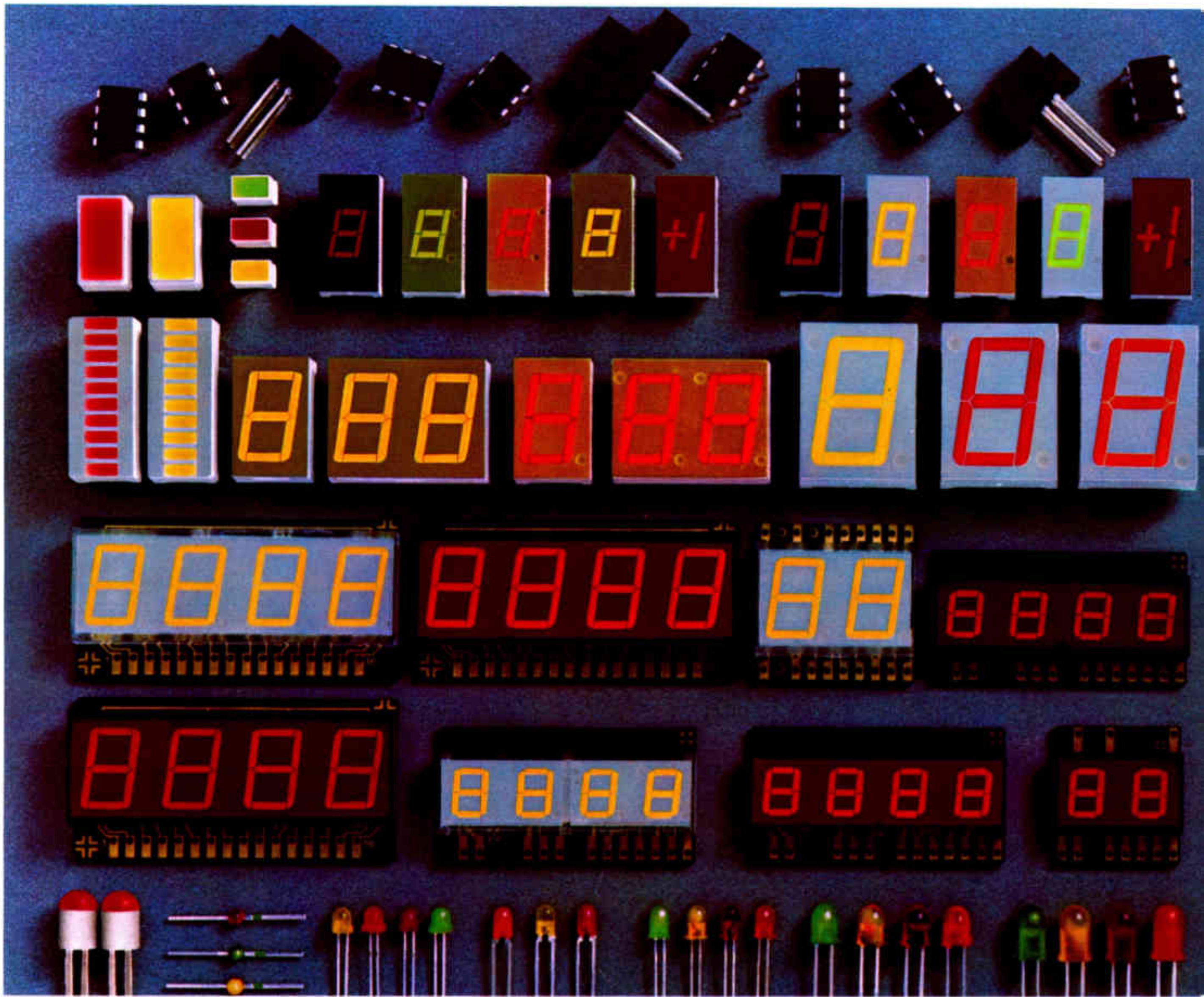
**SIA renews executive director's contract.**

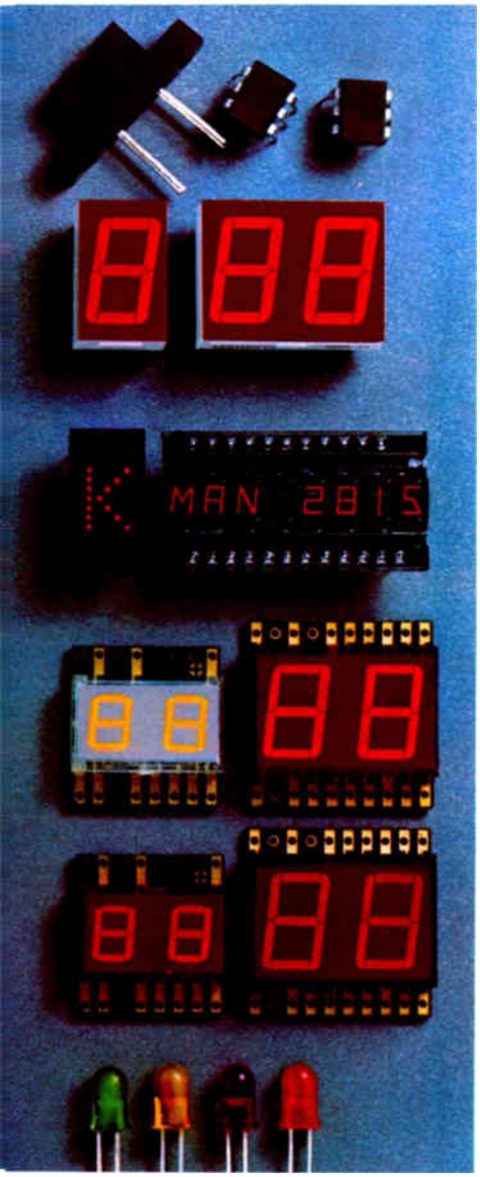
The Semiconductor Industry Association has approved a new three-year contract for executive director Tom Hinkelman. The approval by the board of directors represents a confirmation of the programs and activities under Hinkelman's direction, says John R. Welty, senior vice president of Motorola Inc. and SIA board chairman. The trade association has grown from 7 U. S. semiconductor makers at the time Hinkelman assumed the directorship in 1977 to 42 members.

# Is General Instrument big in optoelectronics?

# Here's our line...

# ...actual size.






General Instrument is one of the biggest names in optoelectronics today.

Our line proves it.

It includes 4 different sizes of lamps, single digits in 4 sizes, .6" double digits, high performance sticks in 2 sizes and a variety of shaped lamps.

All in high efficiency color.

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**4. LAMPS:**
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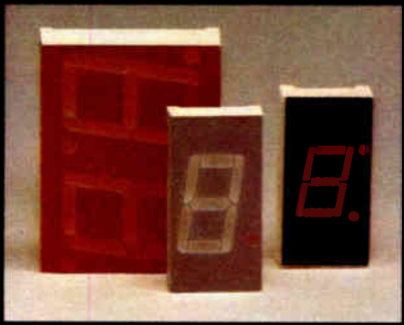

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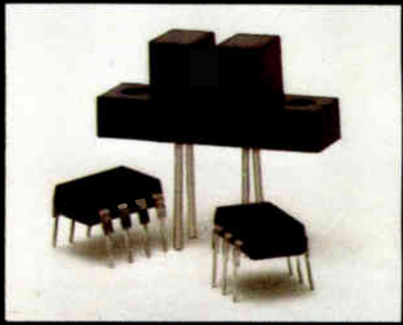
Displays share in General Instrument's work to further improve the performance of current high efficiency materials. So today and tomorrow, expect brilliant displays from General Instrument.



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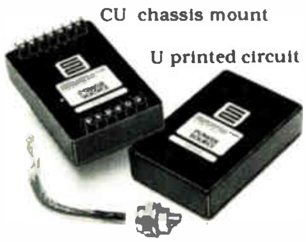

We do . . . because we know what you're up against!

We know your operational problems are complex. That's why we combined a host of innovations into our U and CU series of 25W dc/dc converters.

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Great innovations. Great choices. Both series are available with single, triple, or quadruple outputs. The shielded cases are designed for mounting convenience and noise-free operation. And like *all* the power supplies we make, our U and CU lines require *no derating from −25° to +71°C*. Converters are 10-piece-priced at $157 for single output (5V or 12V), $228 for triple outputs (±5V, +12V, or +5V, ±15V), and $228 for quadruple outputs (±5V, ±12V).

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the circuits begin to emerge from labs about the middle of the decade. By the year 2000, the market could approach $1 billion annually, according to the forecast.

A shift to longer wavelengths—to 1.3 to 1.6 micrometers by the mid-1980s and possibly 2.5 $\mu$m for the 1990s—will be coupled with improved fibers dispersing less light. Thus, data-transmission rates of graded-index fibers for commercial use should rise to 10 gigabits per second, Montgomery forecasts, a sharp advance over today's rates of 2 Gb/s. The capacity of the more costly single-mode step-index fibers, already at the 10-Gb level, will pass the 50-Gb level.

For lower data rates, however, future systems costs can be cut by increasing repeater spacing to 50 kilometers, achieving transmission rates of 1 Gb/s in single-mode fibers, or 200-megabit/s rates in the graded-index variety (see p. 73). The result, Montgomery says, "will eliminate repeaters in virtually all except transcontinental and intercontinental links."

**Laser diodes.** Solid-state light emitters used with fiber-optic systems are expected to continue the marked gains they have made in the last five years in lifetimes, power outputs, linearity, radiation pattern, and efficiency, the study concludes. Guaranteed lifetimes for lasers, now of over 10,000 hours, will rise in another decade to 100,000 hours—more than 11 years—for routinely available production devices. Again, the move to longer wavelengths will contribute to this advance.

As for power outputs, the forecast says that stripe double-heterostructure laser diodes will jump to about 7 or 8 watts by 2000, compared with less than 1 W today, while the output for low-cost hemisphere light-emitting diodes used in laboratory devices will rise to about 0.5 W, compared with present levels well below 0.1 W. **-Ray Connolly**

## IBM, Burroughs expand mainframe offerings

U. S. mainframe manufacturers are stepping up the pace in medium-scale systems. IBM Corp. is giving its 4300 series a new top end, while Burroughs Corp. is making a new attack on the medium- and large-sized market by offering a new entry-level system.

IBM is introducing the 4341 group 2 processors, which are 1.5 to 1.8 times faster than the group 1 processors. Maximum main memory has been increased from 4 to 8 megabytes, along with a doubling of high-speed cache memory from 8 to 16 kilobytes.

At the same time, Burroughs of Detroit, Mich., has announced the B5930 computer, the first of a B5900 series. The 1.5-megabyte system—expandable to 6.2 megabytes—will use the same system software as the large B6000 and B7000 series systems.

It represents a new path to Burroughs' family of large computer systems. The performance of the B5930 is rated at approximately 50% of the B6900 system, falling roughly between the IBM 4331 and 4341 systems.

IBM is obviously trying to keep its customers in the fold when they need expanded computer power and is jabbing at its plug-compatible competitors again by making another improvement in the price-performance ratio for medium-scale computing. Burroughs is making it easier to enter the Burroughs family and stay there all the way to the top.

The surprise is that IBM did not cut the price of the 3031 large-scale system now that the top of the 4300 line will outperform it by about 50% and only cost half as much, argues the analysis group at the research firm, Advanced Computer Techniques Corp., New York. They expect a lower priced, reduced-performance 3033 model soon.

The IBM 4341 model group 2 processors are priced at $385,000, $416,000, and $479,200 with 2, 4 and 8 megabytes of main memory, respectively. The Burroughs B5930 with 1.5 megabytes of memory is priced at $200,000. Both offerings are scheduled for delivery beginning in the second quarter of 1981. **-Tom Manuel**

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We actually design reliability into Digital's micro products.

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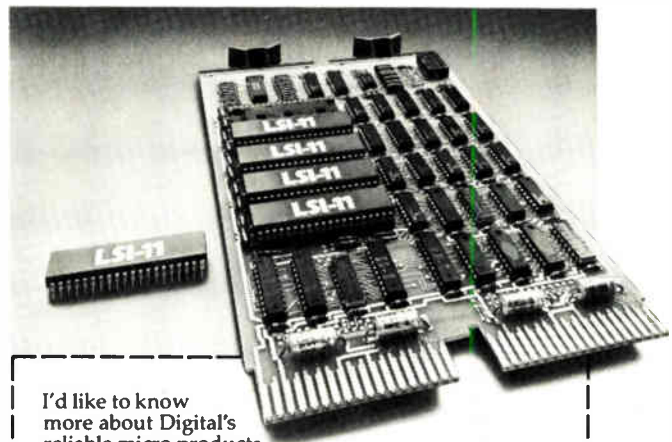


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DEC-C-149 N-9-25-0

# It took the minicomputer company to make micros this easy.

digital

# SCIENCE/SCOPE

Microelectronic chips that contain nearly a half million circuit elements and are hundreds of times faster than currently available devices are being developed at Hughes for a wide range of military uses. The first VHSICs (very high-speed integrated circuits) will be made using photolithography and have device geometries (jargon for the smallest dimension on the chip) as small as 1.25 micrometers. Chips in the mid-1980s will be made with electron-beam lithography and will boast device geometries with submicron dimensions. Applications for VHSIC chips include processors for multimode radars, communication systems, sonars, electro-optical systems, and advanced multimode "fire-and-forget" missiles. The major program goal is to develop common military chips and to limit the number of custom-built and special circuits used.

A spacecraft designed for a variety of missions will carry the most versatile propulsion module ever developed. The new Hughes module will be installed on NASA's Multimission Modular Spacecraft (MMS), which starting in the mid-1980s is to be used for a wide range of communications and scientific missions. In addition to new electronic controls and support structures, this compact module contains a unique monopropellant hydrazine thruster that requires no heater. Conventional thrusters, if used on certain proposed MMS missions, would need extra equipment to heat their catalyst beds to avoid reductions in performance or a complete loss of power.

A new series of PIN photodetectors uses high-purity intrinsic silicon for high responsivity. The devices operate over a broad wavelength range spanning the entire visible spectrum from 400 to 1100 nanometers. At 900 nanometers, responsivity is .63, and quantum efficiency is 87 percent. Applications include computed axial tomography, instrumentation using lasers, and fiber-optic communication and data links. Hughes HPIN diodes are available in single and multi-element arrays in standard or special configurations.

The Manufacturing Division of Hughes Missile Systems Group in Tucson has many immediate openings for engineers. These career opportunities require expertise in designing test equipment for advanced major electronic and missile system programs. Openings range from digital logic, analog, and IF/RF circuit design to electro-optical and IR system design. Also needed are industrial engineers and manufacturing production engineers. For immediate consideration, send resume to Engineering Recruitment, Hughes Aircraft Company, P.O. Box 11337, Dept. SE, Tucson, AZ 85734. Or call (602) 746-8484. Equal opportunity employer.

Field-effect transistors are emerging as strong contenders for microwave switch applications in communications satellites. Gallium-arsenide FETs are likely to replace PIN diodes in satellites due to advantages like higher speeds and lower power consumption. Using arrays of FETs, Hughes researchers built an 8x8 switch matrix for time-division multiple-access applications at 4 GHz. The device achieved a 1-nanosecond transition time at 10 milliwatts drive control power.

# Washington newsletter

**U. S. computer exports peak at $3.5 billion in first half . . .**

Worldwide exports of U. S. computers hit an all-time high of $3.5 billion in the first half of 1980, a 40% gain on the comparable 1979 period and more than seven times the $524 million recorded in imports, which rose 6.8% from the year before. New Commerce Department figures show that exports of other U. S. office equipment rose nearly 25% to $450 million, pushing total business equipment exports to nearly $4 billion, a 35% gain. **That raised the total U. S. trade surplus for all categories to $2.8 billion**—a $1 billion gain from a year ago—despite a $21 million deficit in business-machine trade, where imports totaled $664 million, up 10%.

**. . . as Japan's 25% dip in U. S. shipments is offset by other gains**

U. S. computer imports from Japan slipped 25% to $90.1 million in the first half of 1980 compared with the same period in 1979, while American exports to that country rose by one third to $277.5 million, says the Commerce Department's Bureau of Industrial Economics. However, the decline in imports, attributed by Government experts to the failure of various deals to materialize between Japan's Hitachi and Fujitsu and such American corporations as Amdahl, was more than offset by U. S. imports of Japanese electronic calculators, accounting machines, word processors, and electric typewriters. These categories raised Japan's total exports to the U. S. to nearly $404 million. **Japan is the only nation with which the U. S. has a trade deficit in business machines and computers.**

**Ericsson exploring military version of Millicom transceiver**

Representatives of LM Ericsson, Sweden's largest telecommunications producer, confirm they are exploring with Millicom Inc. the possibility of developing a military version of the New York–based company's **proposed broadband cellular transceiver, a lightweight, hand-held unit.** Millicom recently filed for Federal Communications Commission approval to install and test its system in the Raleigh–Durham, N. C., area, saying the low-cost hardware is being developed by E. F. Johnson Co., a mobile-radio maker in Waseca, Minn., using supervisory and control software and hardware to be develped by IBM Corp.'s. Florida operations [*Electronics,* June 19, p. 61].

**Boeing gets funds to quadruple size of photovoltaic cell**

Boeing Aerospace Corp. has picked up another $503,000 from the Department of Energy to quadruple the size of its 9.4%-efficient thin-film photovoltaic cell made from a combination of copper indium selenide and cadmium sulfide. The two-year contract from the department's Solar Energy Research Institute calls for Boeing to **increase the size from 1 $cm^2$ to 4 $cm^2$ while retaining the high efficiency level** that comes closest to the department's goal of 10%.

**Air Force licenses Z8000 instruction set**

Establishing a beachhead in the military market for 16-bit microprocessors, Zilog Inc. has licensed the U. S. Air Force to use the instruction set of its Z8000 microprocessor in defense-related computer systems. Under the agreement with the Cupertino, Calif., firm, the Armament division of the Air Force Systems Command may use it in **16-bit computer-based embedded systems developed by either the divison or its contractors.** The pact is believed to be the first licensing of a commercially available instruction set to any part of the armed services.

## Ada comes of age

The military computer user's dream—a single language that will run on any computer on or off the battlefield for communications, air traffic control, avionics, or missile guidance—moved closer to reality early this month as the Defense Advanced Research Projects Agency unveiled the first standards for its new high-order language, Ada. It is the result of five years of study by the Department of Defense's High Order Language Working Group and a $6 million investment, including multiple competitive design contracts and inputs from 14 computer makers and software specialists from nine foreign countries. Ada's final form was developed in approximately one year at Honeywell Inc.'s French affiliate, CII-Honeywell Bull, under a team headed by Jean Ichbiah.

Ada evolved through five HOLWG definition studies—Euclid, LIS, MESA, Modula, and SUE—plus smaller contributions from Algol 68 and Simula and research languages such as Alphard and Clu. Darpa's William E. Carlson, Ada program manager, says that the transition to use of the machine-independent language in the mid-1980s should save the military services hundreds of millions of dollars annually by eliminating the duplication of costs for maintaining software, for training, and for making compilers and programming tools available.

### Opening to praise

Ada got a positive acceptance from the estimated 400 software specialists invited to its debut by the defense research agency early this month in Washington, at which Ichbiah spent two days detailing its design and operation. Bolt Beranek & Newman Inc.'s Arthur Evans, describing himself as a long-time critic of the Ada effort, said at the conclusion of the sessions that he was "very impressed by the excellence of the language and its performance."

As Ada is modular, programs can be composed of one or more units of three types: subprograms (defining executable algorithms), packages (defining collections of entities), or tasks (defining concurrent computations). In each unit the specification is separated from the implementation, which therefore may be replaced by a new, more efficient one or even by a functionally equivalent hardware chip without affecting any programs that use the unit. The design emphasis was on program readability over ease of writing, and efforts were made to keep Ada as small as possible, Ichbiah says.

Compilers for Ada are being developed at several universities and manufacturers, Carlson says. SofTech Inc., Waltham, Mass., will complete a basic validation capability for these compilers in October. The DOD expects to have an Ada compiler validation facility operating in the autumn of 1981 to test and certify all independent compilers for use with Ada. Carnegie-Mellon University is working with Intermetrics, runner-up in the competition to develop Ada, on the largest compiler development effort under way, says Carlson; another is being funded by the West German Ministry of Defense at the University of Karlsruhe. The use of Ada's parallel processing features on a multiprocessor is being explored at Stanford University.

### New applications compilers

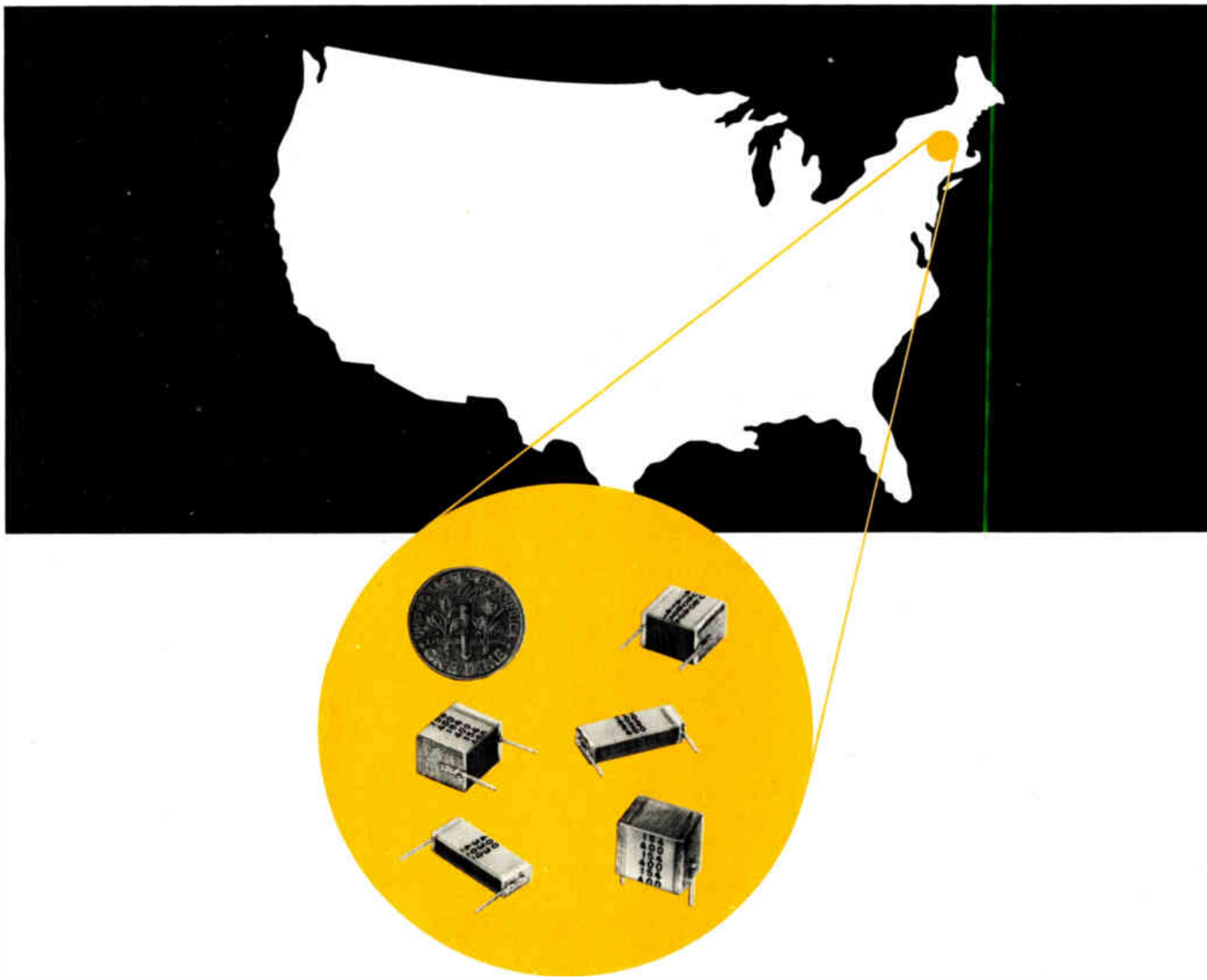
An Army Electronics Command compiler, set for 1982 delivery, is being developed by SofTech to run initially on a VAX 11/780 computer. The Army is pushing the Ada program for its new battlefield computer family.

The Air Force's Rome Air Development Center is striving for compiler code generators for programmers developing or maintaining avionics software and advanced communications processors. It has a 1983 target for a portable system for an IBM/370 and Interdata 8/32.

Intermetrics has also been funded by Darpa to create an experimental compiler to run a DEC-20 by June 1981, using the test translator the company developed in the Ada Phase 2 design competition and combining it with the Carnegie-Mellon University code-generation software. The effort, Carlson explains, is designed to encourage use of Ada for advanced development projects before validated production compilers become available.

Ada still has some way to go before becoming an operational tool for the military. For example, it must gain acceptance from the American National Standards Institute, where manufacturers' biases abound. Nevertheless, the DOD is sufficiently confident in Ada that it is taking program management away from Darpa and funding a new operational support organization for the language under the aegis of its Management Steering Committee for Embedded Computer Resources. As for Ada's principal designer, Jean Ichbiah, he has left CII-Honeywell Bull to head a new company in Versailles called Apsys—for Applications et Systèmes–Ada Programming Systèmes—in which his older employers hold an interest of about 15%. The company was formed in mid-1980 to develop and market software using advanced technology, including the Ada language. **-Ray Connolly**

# Metallized stacked-film capacitors from a NEW prime source: Sprague.



## Type 451P standard design now available for automotive, EDP, telecommunication, TV, instrumentation, and industrial control.

There are good reasons for using metallized polyester stacked-film capacitors: high volumetric efficiency, low self-inductance, and high voltage stress capability—*plus* great suitability for printed wiring boards. Small base dimensions and unencapsulated construction keep size to a minimum, while insulating plates provide mechanical protection. Type 451P capacitors are available with capacitance values ranging from .001 $\mu$F to 2.2 $\mu$F and with voltage ratings of 100, 250, and 400 WVDC. Capacitance tolerance of $\pm$10% is standard . . . $\pm$5% can be ordered at a modest premium.

***For detailed technical data, write for Engineering Bulletin 2460 to Technical Literature Service, Sprague Electric Co., 35 Marshall St., North Adams, Mass. 01247.***

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# engineers gate arrays. decide?

themselves are far faster and more versatile than they were a few years ago. We're delivering 2,000 gate-cells per chip now, looking at about 4,000 soon and forecasting nearly 10,000 in '82. Three years ago we were offering less than 500 gate-cells per chip.

It's not a sudden boom. It has been building for several years and we have done more than 400 circuits during that time.

*Orhan Tozun, Director of Engineering*

## How do we interface with you? How do we get started?

Our engineering department talks with your designer and evaluates your logic to make sure it's do-able on one of our many gate arrays. The next step is a firm quote to let you evaluate the economics of our solution. That includes both development and production costs. We can do it because our CAD system gives us consistency and our years of experience provide projectable yield information that lets us cost your job accurately in advance.

## Then we send you our logic, right?

Right. We take it through a logic restructuring and minimization, block out the functions from our CAD library and lay out the interconnections between logic blocks. Then we check it. And re-check it. Only then do we commit to fabrication.

*Rick Picard, Director of Operations*

## How do we minimize risk with gate arrays?

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**2. Functionality.** We use CAD to convert your logic into silicon. And we have only one layer to get right. Everything else is proven. We spot any problems fast. **It will work.**

**3. Reliability of supply.** Gate array technology lets us inventory pre-processed, ready-to-be-personalized wafers. We keep plenty of wafers on hand to support our customers' orders both for development and for production. Personalization, packaging and test are all performed in-house. We can promise 4–6 week delivery for production quantities. And costs of $.02 a gate or even lower.

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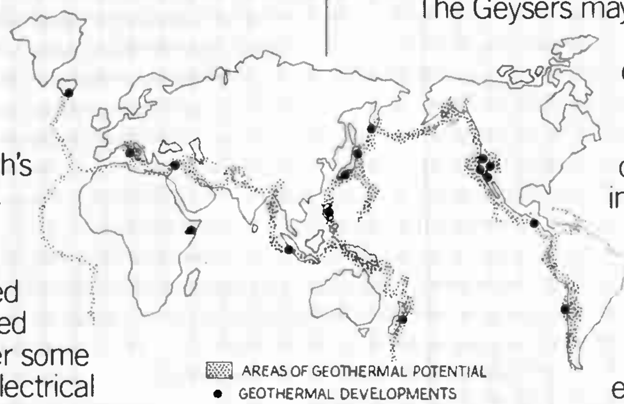
INTERNATIONAL MICROCIRCUITS INCORPORATED
Gate Array Leadership

# MOTOROLA HELPS GET ENERGY FROM

In northern California, the natural heat of the earth is being harnessed to serve the energy needs of man. Natural steam, heated by the molten rock below the earth's crust, is being tapped, extracted and piped to power some of the electrical generators that help light up San Francisco, 90 miles to the south.




The place is called The Geysers, and it's part of a pioneering effort by Union Oil Company of California to make geothermal energy a practical alternative to expensive imported oil.

The Geysers may be an unorthodox power source, but it has one thing in common with every other branch of the energy industries: the need to maintain good, reliable communications, no matter how remote or primitive the site.

At The Geysers, as in many places around the world, the solution to that problem is Motorola communications.

### ELECTRONIC PROBLEM-SOLVING.

One problem at The Geysers, for instance, was the rolling terrain and steep, narrow canyons, among which conventional high-frequency radio signals could get diffused and lost. Motorola solved that one with ingenious simplicity: a low-band two-way radio system that, as one engineer put it, "gets into the nooks and crannies."

### ELECTRONICS EVERYWHERE.

But this is merely the tip of the iceberg of Motorola's experience in energy-industry communications.

One of America's largest oil refineries has 35 Motorola

# THE EARTH, THE SEA AND THE SUN.

systems and subsystems, among which are pagers that tell a man he's wanted on the phone; closed-circuit video monitoring systems; and alarm and control systems that not only tell when something is going wrong, but also when everything is working right.

In the North Sea, a Motorola microwave system will provide a data and voice-communication link that will help one person control six unmanned oil-production platforms. He'll be able to check pressures and flow rates, regulate meters, pumps and motors, all by touching a few buttons.

Some of the Motorola equipment on the Alaska Pipeline is so sophisticated that a hard-hat worker in the field can talk directly to an executive in an office a thousand miles away.

In Canada, specially designed Motorola equipment is in use at an oil mine, an extraordinary strip-mining process for extracting petroleum from tar sands.

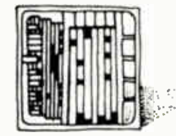
Motorola has made the apparently impossible happen by taking radio communication underground into deep-shaft coal mines.

And in solar energy, Motorola has gone beyond communications to actual energy development. Our engineers are producing photovoltaic systems that convert sunlight into electricity.

## ELECTRONICS AND PEOPLE.

Motorola's preeminence in energy-industry communications is as much a matter of people as of technology. We made an early and total commitment to solving energy-industry communications problems, not merely as suppliers but as participants.

Microelectronics is at the heart of the matter, as it is in many of the things we do today. But if there are similarities among communications devices, there are none at all among the communications systems that the energy industries need in all their activities.



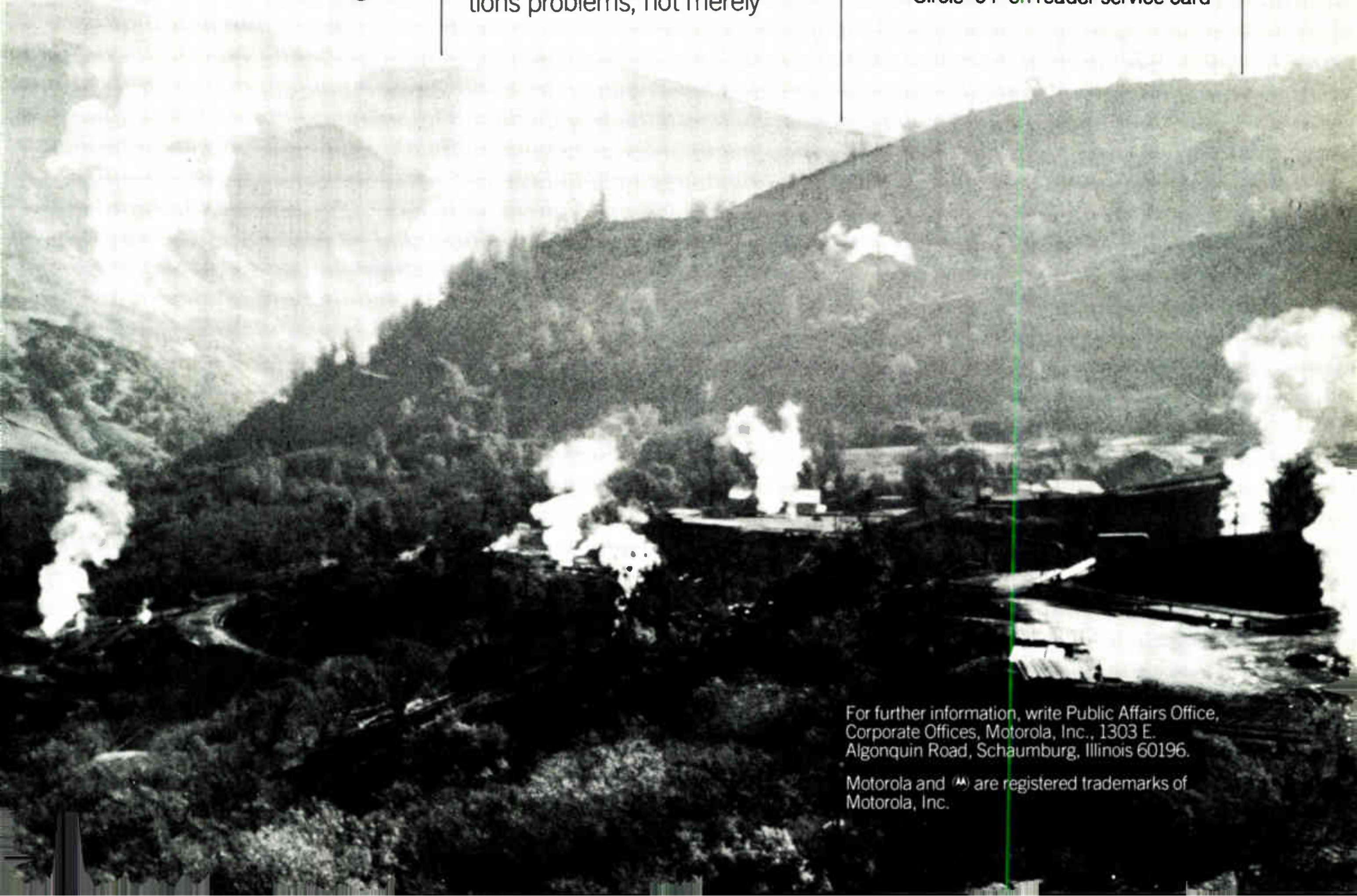
*A microcomputer, drawn larger than life.*

In designing these systems, Motorola brings to bear a combination of expertise and enthusiasm that helps us keep expanding the limits of what's possible in electronics.

**MOTOROLA**

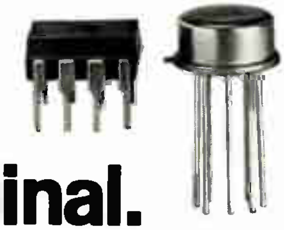
**Making electronics history.**

Circle 61 on reader service card



For further information, write Public Affairs Office, Corporate Offices, Motorola, Inc., 1303 E. Algonquin Road, Schaumburg, Illinois 60196.

# BiMOS vs. BiFET op amps: The RCA alternate source for TI's 080 outperforms the original.



Our new CA080 BiMOS series is a pin-for-pin compatible alternate source for the TL080 BiFET family from Texas Instruments.

But that's where the similarity ends. When it comes to specs, in many cases the RCA device outperforms the original.

Our version has both lower input bias current and lower input offset current. This superior performance can save you money.

Your filter circuits will cost you less because you can increase resistor values and use less expensive, lower value capacitors.

The lower input bias and input offset currents of our devices also let you design circuits with input signal currents in the picoamp range.

Other features of the new CA080 series are: low power consumption, wide common mode input voltage range, fast slew rate, 5.0 MHz (typical) bandwidth, low distortion, and large output voltage swing.

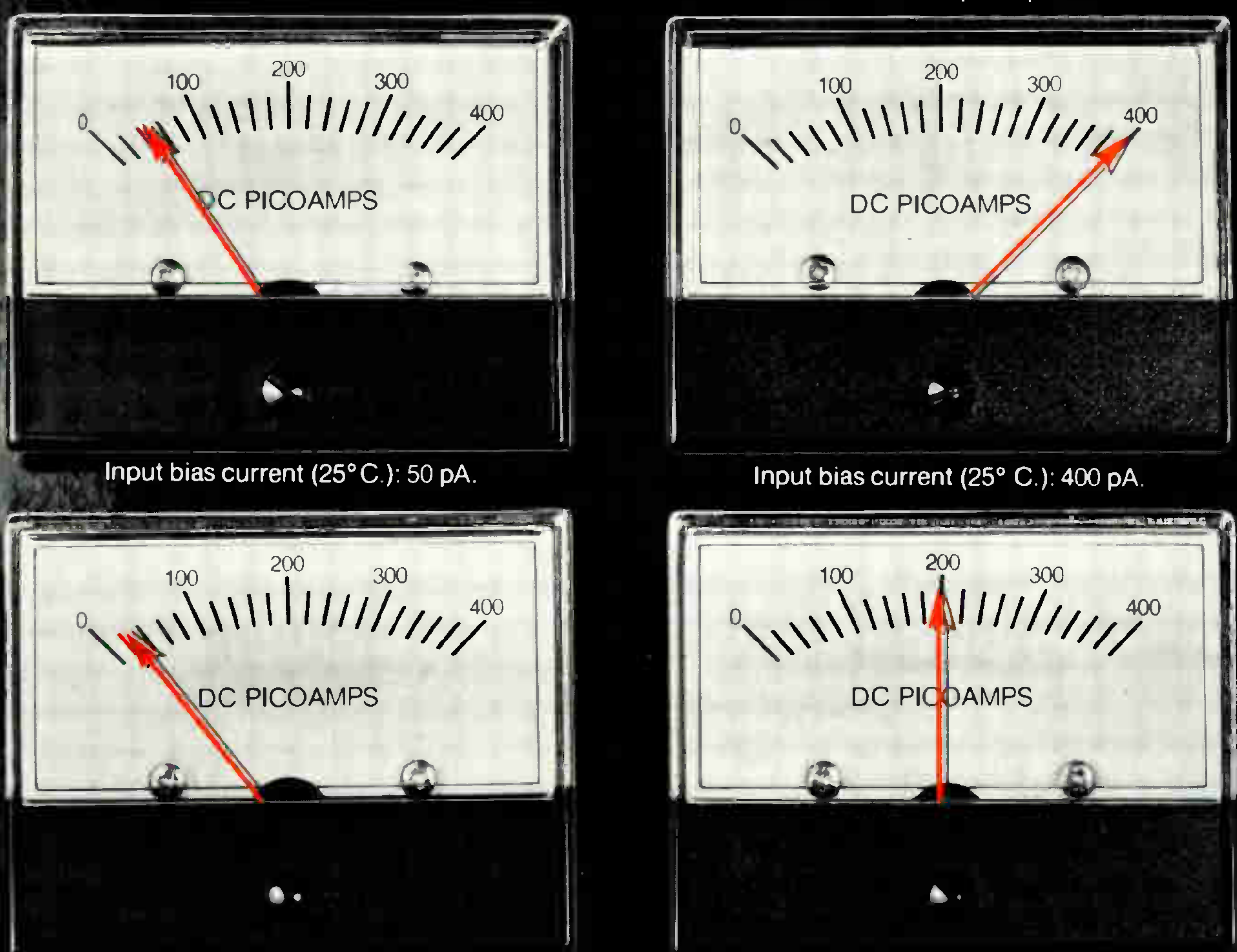
The CA080 and CA081 single devices are available in quantity now. Our CA082 and CA083 duals will be available by mid-1980.

For more information, contact your local RCA Solid State Distributor.

Or contact RCA Solid State headquarters in Somerville, New Jersey. Brussels, Belgium. Tokyo, Japan.

RCA BiMOS op amp:

TI BiFET op amp:




Input bias current (25° C.): 50 pA.

Input bias current (25° C.): 400 pA.

Input offset current (25° C.): 30 pA.

Input offset current (25° C.): 200 pA.

RCA

Circle 62 on reader service card

# International newsletter

**First video camera with solid-state imager reaches consumers**

Video cameras built around a single solid-state sensor are officially on their way to the consumer. Hitachi Ltd. has become the first company in the world to announce a product with a firm price and a date for start of sales. Its VK-C1000 will **go on sale in Japan in April for $1,666.** Consumers will be able to preview the product, though, at the Japan Electronics Show '80 in October. Production will start at about 1,000 cameras a month.

Hitachi's image sensor is an MOS device that has 485 elements vertically by 384 laterally on a 10-by-8.5-mm substrate that reads out two lines simultaneously. Active area is equal in size to the target of a ⅔-in. vidicon. A repetitive, quad color filter provides high utilization of scene illuminance because all four filter elements pass green. Minimum scene illumination is 100 lux; resolution is 260 TV lines horizontally by 350 vertically; and signal-to-noise ratio is 46 dB in good lighting.

The camera measures only 58 by 100 by 155 mm (2.3 by 3.9 by 6.1 in.), exclusive of its electronic viewfinder and lens. With the standard six times *f*1.4 zoom lens, it weighs 1.1 kg; the electronic viewfinder adds another 0.5 kg. **Exports should start somewhere between April and December 1981.**

**British modem sends 16 kb/s over unconditioned line**

The high-speed norm for transmitting digital data over conventional, unconditioned telephone lines is currently 9,600 b/s, but Plessey Digital and Network Systems Ltd. at Taplow, Bucks., has upped this by 66% with a newly introduced modem that transmits data at 16,000 b/s. Under sponsorship from Britain's Royal Signals and Research Establishment in Malvern, the modem was initially intended to transmit digitally encrypted speech. It overcomes the telephone line's limited 3.4-kHz bandwidth by using quadrature-amplitude modulation (QAM), in which **two 1,700-Hz tones, phase-separated by 90°, can each take any of eight peak values.** The receiver is enabled to discriminate between the eight levels by microprocessor-based adaptive line equalization and filtering techniques developed initially at Loughborough University. First deliveries are scheduled for January 1981.

**Siemens opens advanced VLSI facility**

In an effort to strengthen its position in the market for MOS integrated circuits, West Germany's Siemens AG has started up a new production center for such devices featuring structures down to 2 $\mu$m. The $17 million facility, at the company's Munich-based Components division, is laid out to produce very large-scale ICs on 4-in.-diameter wafers that contain some 150,000 elements on a 25-mm$^2$ area. **Encompassing two ion-implantation plants as well as the latest photolithographic projection equipment and wafer steppers,** the center will initially fabricate the Intel-derived SAB 8085 and SAB 8086 microprocessors plus 16-K and 64-K dynamic memories and custom VLSI circuits.

**Toshiba builds 16-bit microprocessor on sapphire**

Silicon-on-sapphire large-scale integration has enabled Toshiba Corp. to implement on a single 6.66-by-7.46-mm (262-by-294-mil) chip its T88000 16-bit microprocessor, which is **suitable for a super minicomputer that can directly access a 16-megabyte memory.** The processor features a 10-MHz clock with one machine cycle of four clock periods, or 400 ns (most user instructions take only one machine cycle). Despite the high performance, the inherent high speed and high density of SOS make for ease of fabrication and high yields because the device can be built with 3.5-μm-rule masks and a 2.8-μm effective channel length.

The device uses both complementary-MOS and n-MOS circuits for the optimum combination of speed and power. It operates from a single 5-V power supply and dissipates 0.7 W.

### Nixdorf announces its first large computer

Living up to the promise it made earlier this year, West Germany's Nixdorf Computer AG has taken the second step in moving into the mainframe business. After acquiring the Computer Software Co. of Richmond, Va. [*Electronics*, May 22, p. 33], whose software products enable users of IBM systems to improve the performance of their machines, Nixdorf has announced its first mainframe system, the 8890, **a medium-sized computer comparable to the lower-end models of in the 4300 series** from the U. S. computer giant. To build it, Nixdorf is cooperating with Elbit Computer Ltd. of Haifa, Israel, which supplies data-processing systems know-how and is producing 8890 parts under a licensing agreement with the German firm. Paderborn-based Nixdorf initially expects to sell about 100 of the 8890s a year and will be offering them in the U. S. in 12 to 15 months.

### Video camera cassette recorder from Hitachi vies with Sony's VCR

A camera with a compact built-in cassette that can record up to 2 hours of picture and sound is Hitachi Ltd.'s entry into the standardization sweepstakes for video cassette recorders started by Sony Corp. [*Electronics*, July 17, p. 48]. Despite its machine's radically different specifications, Hitachi hopes that the industry can reach a consensus in time for it to start sales in about two years.

Besides providing six times longer recording time, Hitachi one-upped Sony by developing a method of multiplexing a frequency-modulated stereo signal with a frequency response to 18 kHz onto the video signal. Other features include **still, slow-motion, and high-speed playback, as well as dubbing.** The format also puts audio and control signals on the edges of the ¼-in.-wide tape, as in present VHS video recorders. The video recording method is standard.

Although only a prototype, Hitachi's Mag camera is producible because it uses the same image sensor as the firm's video camera (see p. 63). The weight is 2.6 kg, including a nickel cadmium battery that will power the unit for 30 minutes, size is 237 by 192 by 76 mm without the 4× zoom lens. A big difference from Sony's scheme is that **the combination plays back tapes directly rather than requiring a table-top adapter.**

### Addenda

A throughput of 29 million instructions per second distinguishes the bigger of two models of Nippon Electric Co.'s Acos 1000, **the world's largest general-purpose computing system.** The new machine could prompt modifications in IBM's upcoming H series. . . . France's Compagnie Générale d'Electricité is **moving to improve its access to MOS technology.** CGE's Parisian subsidiary, CIT-Alcatel, is acquiring 25% of Semi Processes Inc., a two-year-old Santa Clara, Calif., manufacturer of custom semiconductors created by former Intersil vice president Robert Freund.

# What if Isaac Newton had discovered Monochips™ before gravity?

It's too bad Monochips™ weren't around in Isaac Newton's day. If they had been, Sir Isaac might have designed tools to defy gravity in addition to discovering it...or a radar unit to warn people about falling apples. He might even have designed a computer to help people use his new calculus. Because Monochips bring out the genius of great thinkers.

Monochips are semi-custom IC's. They give you all the benefits of full-custom development without the lead time or the expense. That's because Monochips' circuit components — the first five layers — are already in place when you start designing. All you do is connect them to make the circuit your application requires.

Working from your layout, we etch the sixth layer and deliver prototypes in 8 weeks for $5,000 or less. When you approve them, we produce 1,000 to 500,000 parts for you.

Make a great discovery yourself — Monochips. Our Monochip Design Kits make it easy for you to design your own custom IC — linear, CMOS, NMOS, CML, or bipolar — for only $25 to $59 per kit. Put your genius to work. Call us today to order your kit or for more information. Interdesign, 1255 Reamwood Avenue, Sunnyvale, CA 94086. (408) 734-8666.

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# Introducing the F6856 Protocol Controller.

At Fairchild, we've been working on ways to help you better understand the world of protocols. As a result, we've just developed the first in a new series of advanced telecommunication circuits that will put you worlds ahead. The F6856 Protocol Controller.

## We speak your languages: SDLC, BISYNC, HDLC, DDCMP, ADCCP and more.

Now that the F6856 is here, your equipment can be designed to handle virtually any synchronous protocol. That includes SDLC, BISYNC, HDLC, DDCMP, ADCCP and other bit-oriented or byte-control protocols. This eliminates the incompatibility problem you've encountered up until now.

And, as another major advantage, the F6856 is compatible with all major 8 and 16-bit microcomputer buses.

## A single-chip solution to multi-protocol problems.

Most of the competitors' products use either two or more chips, or provide very rudimentary protocol functions; which requires extensive programming in the host computers.

The F6856 performs the bulk of the communications protocol functions on one chip, including the complete BISYNC. That means there's less programming and design time involved. So your entire system overhead cost, in time and dollars, is going to be reduced.

## We bring world communications closer together.

When you need to be on speaking terms with the whole world of protocol, write or call Fairchild Microcomputer at Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, California 94042. Telephone: (408) 224-7106.

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# on speaking terms.



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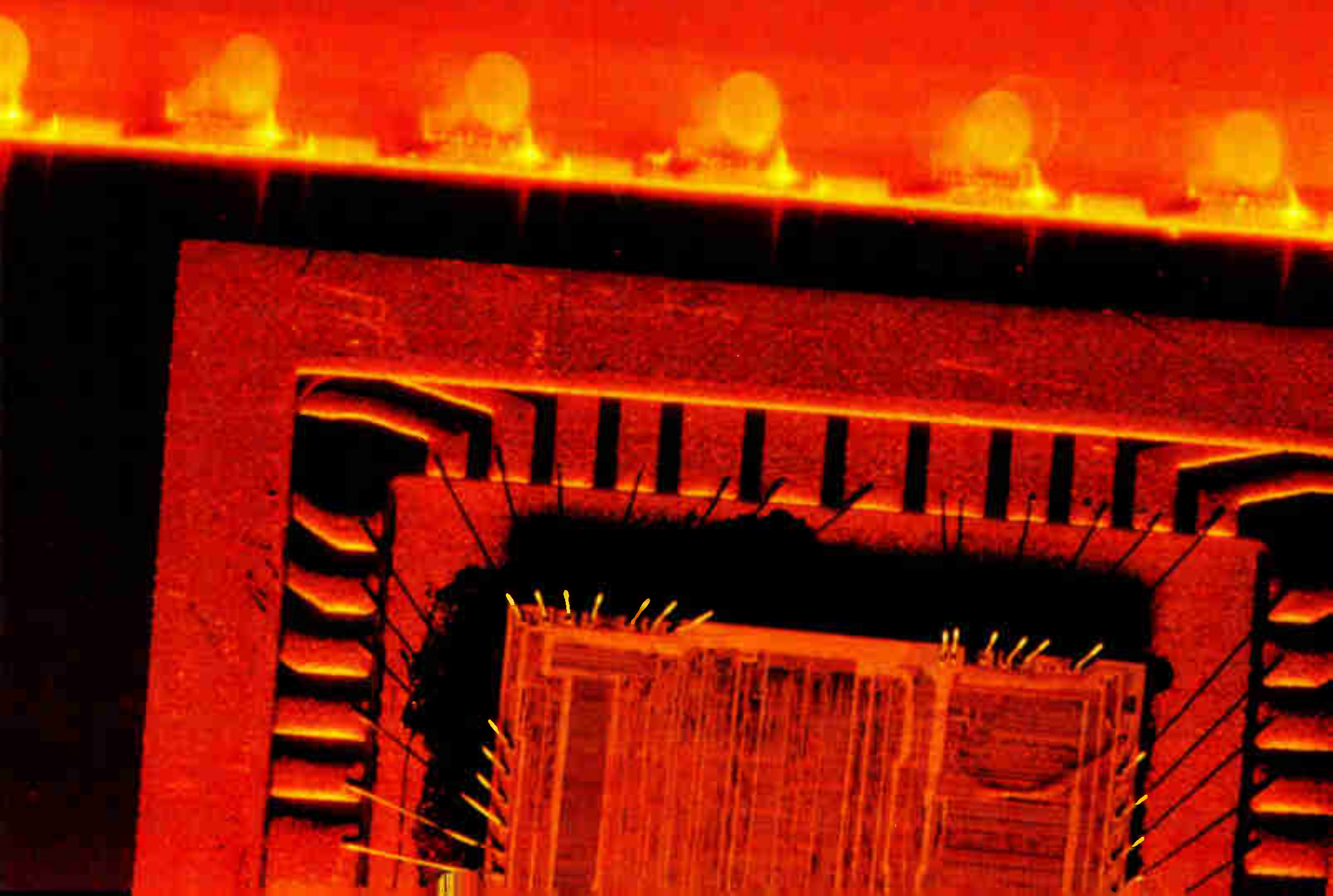


HI-5900
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SAMPLE AND HOLD
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D/A
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ANALOG TO DIGITAL CONVERTER
HI-5712

*Harris Technology at Work*

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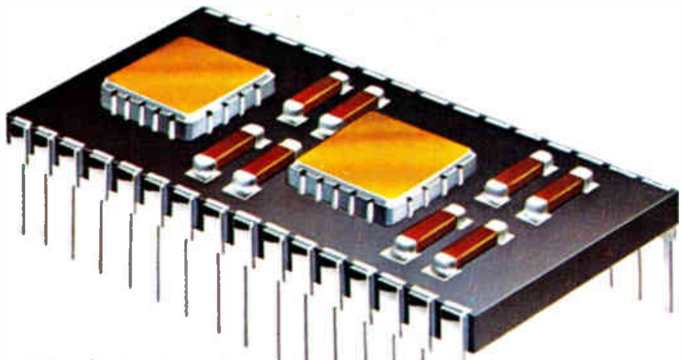

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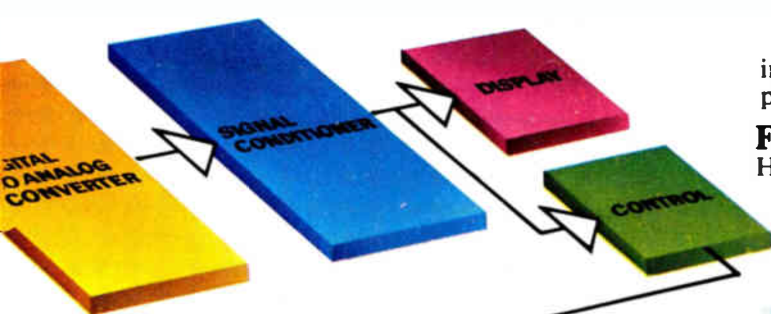


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# UK to install second-generation fiber-optic links

*by Kevin Smith, London bureau manager*

Success with InGaAs-based detectors encourages move by post office to less costly, longer-wavelength systems

**Plans by British** Telecom, part of the British Post Office, to progressively phase out copper-cable trunk telephone systems on new links in favor of second-generation fiber-optic systems from 1985 onward have been given a boost by successful laboratory experiments at its Martlesham Research Centre. In the experiments, optical data was transmitted at 140 megabits per second over 49 kilometers of graded-index fiber in one hop using the low-loss optical window that occurs at the 1.5-micrometer wavelength [*Electronics*, Sept. 11, p. 67].

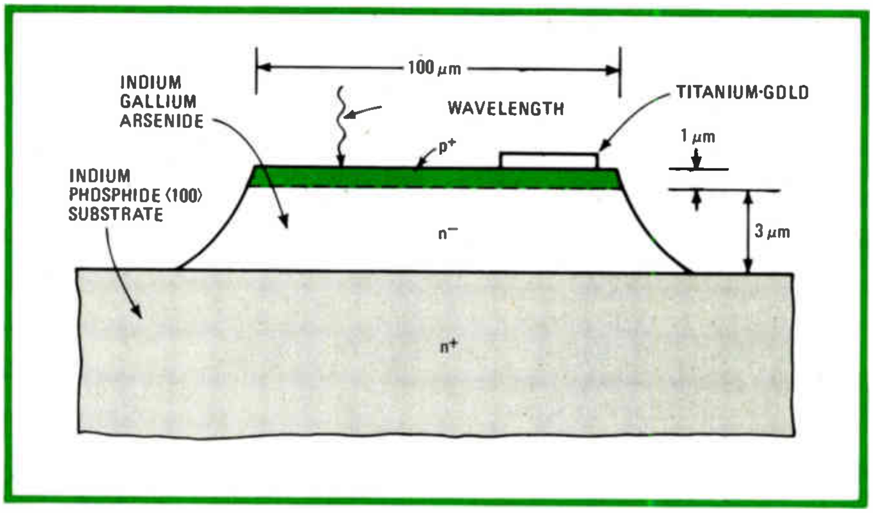
In first-generation systems operating at 0.85 μm—the first of which was cut over to routine public service last week—repeaters are spaced every 10 km. By moving to 1.3- or 1.5-μm windows, fiber losses drop dramatically to 0.45 decibel/km typically, a 90% decrease. But the move has awaited the development of optical transmitters and receivers capable of operating at these longer wavelengths.

**Striped.** British Telecom's planning department used a newly developed stripe laser from Standard Telecommunications Laboratories Ltd. and group III–V p-i-n diodes developed by Plessey Co.'s Allen Clark Research Centre and its own laboratories. Plessey also has a 1.3-μm light-emitting-diode source. The planning department's specification 4 requires that, for fiber-optic systems to oust cables, repeaters should be spaced every 30 km on 1.3- or 1.5-μm-wavelength, 140-Mb/s trunk systems, and post office experiments at both wavelengths demonstrate that these targets can be comfortably met. Last year, British Telecom ordered its first fiber systems for routine use—15 of them operating at 8, 34, and 140 Mb/s—and is shortly to place follow-on orders that will be twice the size of the first so-called shop-window contracts.

At a wavelength of 1.3 to 1.5 μm, silicon-based devices are past optimum sensitivity. Commercially available germanium detectors have a good response, but characterization at British Telecom's Martlesham labs found that they were noisy and had a high leakage current. The alternative was to move to group III–V compounds such as gallium, indium, and arsenic, but when operated in the high-gain avalanche mode these, too, proved noisy.

An alternative approach uses a group III–V p-i-n photodiode detector. This device has only unity gain, but by combining it with a high-impedance field-effect-transistor preamplifier in a hybrid package, a theoretical performance comparable to that of the avalanche device can be achieved. The resulting system also has the advantage that it can be manufactured more reliably than avalanche devices, works at a lower voltage of 10 to 15 volts, and needs no additional circuitry to control gain.

**Two options.** Two detectors have been developed for this purpose, one by Plessey and the other by British Telecom, optimized for operation at the 1.3- and 1.5-μm windows, respectively. Both are zinc-diffused homojunction devices with mesa-defined active areas. In the Plessey device, an InGaAs epitaxial layer is grown on a GaAs substrate and




**Economical.** To space repeaters 49 instead of 10 km apart along a fiber-optic link, British go to 1.3- or 1.5-μm wavelength, detect latter signals with aid of 1.5-μm diode (above).

incorporates a constant composition layer and a highly doped graded region that buffers crystal mismatches between substrate and epitaxial layer.

In order to optimize peak response at 1.3 or 1.5 μm during manufacture, electronically controlled flow regulators provide accurate and reproducible control of the indium-gallium ratio.

The resulting device has a low input capacitance of less than 0.2 picofarad, a dark current of less than 1 nanoampere, and a quantum efficiency of more than 50% without optical coating. For operation up to 1.67 μm, the BPO-developed InGaAs p-i-n diode (see figure) is formed on an indium phosphide substrate. Quantum efficiency is 45% to 50%. The active area of 100 μm in diameter gives an input capacitance of 0.3 pF at a 10- to 20-V bias, and leakage current is 10 to 20 nanoamperes. Commercial development of the device will be likely left to Plessey.

Either diode matches into a GaAs metal-semiconductor FET preamplifier, and the two are mounted on a thick-film hybrid substrate soldered into a dual in-line package that comes complete with a fiber pigtail. The resulting receiver sensitivity, says British Telecom in a paper presented at the Sixth European Conference on Optical Communication in York, Sept. 16–18, shows at least a 4-dB improvement over results reported for long-wavelength avalanche photodiodes. The gain is sufficient to render negligible the noise from following amplifier stages, according to Ray Hooper, a member of the Telecom research team leading the development.

## East Germany

# Leipzig fair spotlights liveliness of East German consumer electronics

Rudyard Kipling notwithstanding, East and West do meet—at least Eastern and Western Europe—and one place where the twain often come together is at Leipzig, East Germany. There, at the sprawling Saxon metropolis, firms from the Capitalist West and the Socialist East meet twice each year during the city's big spring and fall fairs—to display their wares and to assess each other's products.

For many Western observers, Leipzig is as much a place to compare technologies as to get a reading on how business in East Germany's electronics sectors is going. From the just-ended fall fair (Aug. 31–Sept. 6), they came away with a strong feeling that for all their emphasis on industrial electronics, East German economic planners have not neglected the entertainment sector. In fact, East Germany, which boasts the highest standard of living in the Socialist Bloc, is generally considered to lead its Comecon partners in the level of both the penetration and the technical sophistication of many of its entertainment products.

**State-owned.** Like almost everything else it makes, East Germany fabricates such products at state-owned enterprises. Responsible for equipment ranging from small portable radios to color TV sets and large community antennas is VEB Kombinat Rundfunk und Fernsehen. The combine encompasses 19 production centers throughout the country and employs some 21,000 people. Part of the organization are several distribution centers and well over 1,000 service shops with another 6,000 or so employees.

Headquartered in the 800-year-old town of Stassfurt, just east of the Harz Mountains, the combine produces nearly all of what Kansas-sized East Germany, with its 17 million people, consumes in the way of electronic entertainment gear. Annual consumption is pegged at about $1.3 billion. Imports—some color receivers from the Soviet Union and portable sets from Japan—are "not very high and intended mainly to round out the sales program," one industry official says.

As is the case in many Western countries, color TV is the industry's main pillar, "with 24-inch and 26-inch sets predominating," says Johannes Gläser, head of market research for the combine. Of the half a million units it produces annually,

**For the Socialist consumer.** This Colorett 3006/3007 color television set is manufactured by East Germany's major set manufacturing facility, located in Stassfurt.

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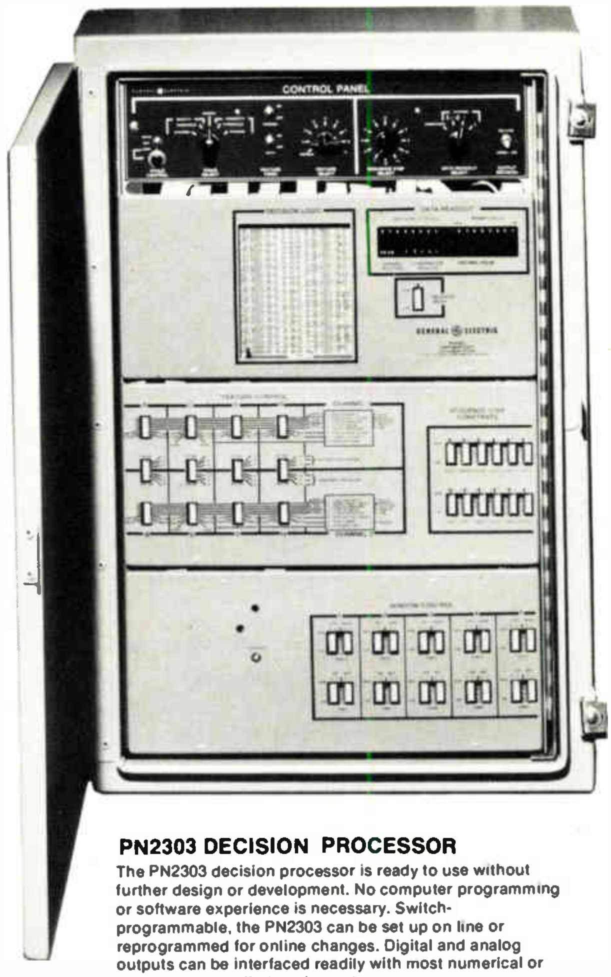


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about three quarters are color sets. "We sell them as they come off the production line," Gläser notes, hinting the industry has none of West Germany's inventory problems.

**Penetration.** Surprisingly, since the start of color broadcasting in the late 1960s, the color set penetration into East Germany's 6.4 million households has already reached the 55% level, which puts the country on a par with, or even ahead of, some West European countries. The total penetration—of both color and monochrome sets—is at the near saturation level at about 92%.

For many Westerners, the high color set density is all the more surprising given a receiver's relatively high retail price—between $2,200 and $3,300 for a set capable of receiving not only East Germany's Secam-standard programs but also PAL programs from West Germany. That price range amounts to four to six times the monthly wage of an average East German factory worker. But industry officials are quick to point out that many basic necessities of life—housing, public transportation, and medical care, for example—are very inexpensive or even free, thus offsetting the high prices for manufactured goods.

Though color sets are slowly becoming a standard household item, high-fidelity and stereo equipment still has some way to go. Gläser estimates the stereo set penetration at about 35%. Somewhat higher is the figure for households with sets hooked to community antennas—40% to 45%—which is delighting environmentalists, for whom small rooftop antennas are an eyesore. Some community antennas, Gläser says, accommodate up to 50,000 subscribers.

**Imports.** For East Germany's entertainment electronics industry, it makes little economic sense to produce everything on its own. Reel-to-reel tape equipment, for example, is imported from other Socialist countries, as are some low-priced car radios. Besides, all the color TV tubes consumed by East Germany come from either the Soviet Union or France, the latter supplying tubes with a precision in-line gun configuration. Audio cassette recorders, higher-priced a-m and fm car radios with automatic station-search facilities and traffic radio decoders, as well as hi-fi equipment, are made domestically.

A quick look at color sets at the Leipzig fair revealed that in many aspects of receiver design East German engineers are closely following their Western counterparts. Testifying to that are video games, remote control by infrared-light beams, and other features. In using integrated circuits to enhance set performance, "we are up to international standards," Gläser states. The ICs applied are mainly East German, "but we are also sampling what other Socialist countries are offering," Gläser adds.

A top-of-the-line model in East Germany's arsenal of color receivers is the Colorlux 3010/3011. It uses a 110° 26-in. precision in-line tube. With IR remote control, implemented with ICs, up to eight programs can be selected. Further, the on-off function, the volume, brightness, and contrast control, and some other functions can be performed remotely. **-John Gosch**

## France

# SLIC chip will adapt to every switch

Philips' main telecommunications equipment subsidiary in France is finally taking some of the wraps off what is touted as a "truly universal" monolithic subscriber-loop interface circuit, or SLIC. Controlled by a digital data bus, the circuit was designed by Télécommunications Radioélectriques et Téléphoniques (TRT), based in the Paris suburb of Le Plessis-Robinson, and is being put onto silicon by Harris Corp.'s Semiconductor Products division in Melbourne, Fla. [*Electronics*, June 5, 1980, p. 126].

Both partners boast that it will be fully compatible with existing digital switching exchanges, be they public or private, and will also be versatile enough to fit into more sophisticated switches of the future. Test samples are expected late next year.

As described at the mid-September International Symposium on Subscriber Loops and Services (ISSL) in Munich, West Germany, the device is designed to operate over a wide range of voltages and impedances while maintaining immunity to longitudinal line currents and an exemplary balance to ground—knotty problems in SLIC design. Balance to ground never gave much trouble in conventional line interface circuits because they were made from passive components.

**Amps.** In the TRT-Harris chip, a pair of symmetric push-pull amplifiers, controlled by two delta-modulation decoders, constitute an internal programmable ringing-signal generator. The amplifiers can be powered by a 48-volt battery, an auxiliary positive power supply, or a combination of the two. The stream of data into the decoders permits a ringing voltage anywhere from the negative battery voltage up to the positive voltage provided by the auxiliary supply. Since the delta decoders operate at a relatively high frequency, 100 kilohertz, they produce a smooth sinusoidal ringing signal.

The internal generation of ringing signals means that the signal frequency can be easily modified to conform to a wide variety of standards, notes Gilbert Ferrieu, technical manager of the SLIC circuit design for TRT. What's more, the same data stream can control the ringing voltage for all of the subscriber lines in a particular grouping.

Though the SLIC is traditionally conceived to fulfill what telephone specialists call (and spell) the Borsht functions—battery feed, overvoltage protection, ringing, signaling, and two-to-four-wire hybrid and test functions—Ferrieu suggests that a second "t" could be added to the acronym to stand for "transmission." Providing a specified impedance and good balance to ground for ac signals are among the most difficult requirements an electronic SLIC must meet, he explains. In the TRT-

Harris device, counterreaction circuits both ensure that its dual push-pull amplifiers balance their impedance to ground and render them insensitive to current reversals due to longitudinal currents.

**Details.** The currents flowing to or from the two outputs from the SLIC to the subscriber line are fed into a summing circuit, where a current proportional to the sum of the two SLIC output currents is calculated. At the same time, the voltage drop created by this current on any given impedance with respect to ground is measured. A routing device creates two voltages, one equal to the voltage drop and the other to 48 V. Being controlled by the two delta-modulation decoders mentioned above, the routing device can direct the voltage drop and its complement voltage to the dual push-pull amps.

This summing circuit provides one way in which the SLIC can handle changing impedances in the transmission line connected to it. The circuit both sums the SLIC's output currents and calculates its own proportionality factor from the result and finally multiplies the sum by the factor. The change in current simulates a change in impedance. Alternatively the delta-modulation controllers may be programmed to vary the impedance with respect to ground. Thirdly, these two methods may be combined.

The accuracy of the summing circuit is a crucial point, and Harris's dielectric isolation process is said to be particularly well suited to the job.

**44 tests.** The same serial data bus used to control the delta decoders provides the data for a series of switches that control current injectors for test purposes. A multiplexer gives access to eight internal points in the SLIC, where a set of loop conditions are created by combining multiplexer and current injector configurations. All told, 44 different conditions can be measured, and the results sent via the exchange itself to a remote maintenance facility.

Though reluctant to cite specifications at this early stage, Ferrieu believes the SLIC will provide common-mode suppression of better than 60 decibels, have a maximum power dissipation of 1 to 2 watts, and thanks to a pair of clamping diodes, offer overvoltage protection of 1 kilovolt. The chip itself is expected to measure 2.5 by 2.5 millimeters (98 by 98 mils) and contain the equivalent of roughly 100 transistors and diodes. **-Kenneth Dreyfack**

**Japan**

## Electron-beam and optical lithography combine to enhance VLSI throughput

Is it possible to fabricate a very large-scale integrated device combining direct-stepping-on-wafer optical lithography and direct-electron-beam-on-wafer lithography? As part of Japan's now-complete four-year VLSI project, researchers working out of Nippon Electric Co.'s Central Research Laboratories in Kawasaki have done just that.

They did it in two versions of the same 512-K read-only memory. The results indicate that it is practical to use 10:1-reduction direct-wafer-stepping optical lithography for high throughput for most masking processes on the chip and follow it with direct-electron-beam-on-wafer lithography for the critical fine dimensions of high-density chips, including the upcoming generations of 256-K and 1-megabit random-access-memory chips. The same production approach could also be used for fast turnaround time on a wide variety of custom and semicustom chips.

The original ROMs were designed for kanji (Chinese character) pattern generators for cathode-ray-tube displays. But the same memory could find other applications.

The Japanese team reached the combined procedure in two install-

Circle 118 on reader service card

ments. The first version of the 512-K ROM used direct-electron-beam-on-wafer lithography for all pattern steps [*Electronics*, May 8, p. 39]. While conceding that use of electron-beam lithography for every step is not really practical because the throughput is too slow, the developer points out that the result does establish the feasibility of using this procedure on any masking step.

The second version, which was reported on at the 12th Conference on Solid State Devices held in Tokyo late last month, proves the electron-beam system can be aligned on the pattern previously exposed by the optical system.

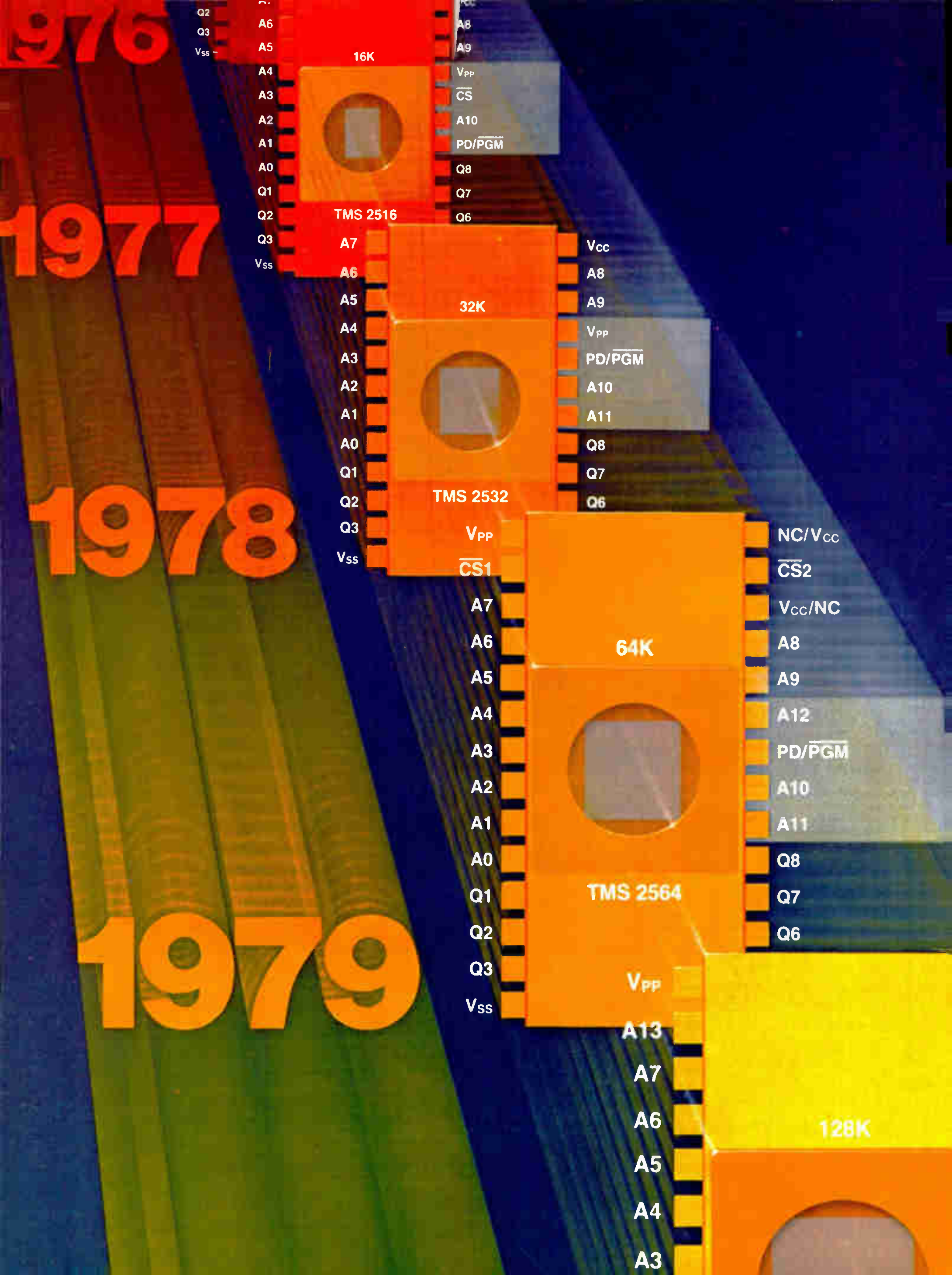
**Down the drain.** In this particular application, electron-beam lithography is used to personalize the ROM by opening a contact hole to the drain region just prior to the final metalization. This approach would make for short turnaround time. NEC engineers claim that such a fabrication method is also suitable for customization by maskless electron-beam exposure of pattern levels having lines rather than contact holes. In fact, the production process is expected to give line definition much the greater emphasis.

During the direct stepping exposure, cross marks for aligning the electron-beam system are delineated and later etched to a depth of 1.5 micrometers. They enable correction for wafer rotation and field. As a result, the average overlay error of both the stepper and the electron beam is less than 0.3 $\mu$m. The average exposure time for the 81 chips on a 4-inch wafer by the optical stepper is 80 seconds per wafer, while the average electron-beam system time for exposing contact holes is about 60 seconds per chip.

Each ROM chip is organized as eight 64-K blocks, and eight single-bit outputs are read out in parallel. Design rules include a polysilicon gate length of 1.8 $\mu$m and metal line width of 3.2 $\mu$m.

The 512-K ROMs operate from a single 5-volt power supply with TTL logic levels; access time is 400 nanoseconds and power dissipation is 800 milliwatts. **-Charles Cohen**

Circle 81 on reader service card


1976
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A9
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TMS 2532
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TMS 2564
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CS2
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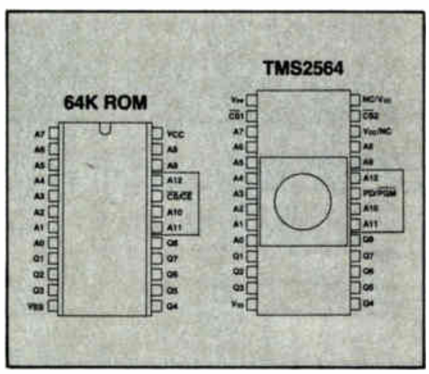


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|---|---|---|---|---|---|
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| TMS25L32 | 32K | 5 V | 325 mW | 50 mW | 450 ns |
| TMS2532 | 32K | 5 V | 400 mW | 50 mW | 450 ns |
| TMS2516-35 | 16K | 5 V | 285 mW | 50 mW | 350 ns |
| TMS2516 | 16K | 5 V | 285 mW | 50 mW | 450 ns |
| TMS2508-25 | 8K | 5 V | 250 mW | 50 mW | 250 ns |
| TMS2508-30 | 8K | 5 V | 250 mW | 50 mW | 300 ns |
| TMS2716 | 16K | +12, ±5 V | 315 mW | — | 450 ns |
| TMS27L08 | 8K | +12, ±5 V | 245 mW | — | 450 ns |
| TMS2708 | 8K | +12, ±5 V | 690 mW | — | 450 ns |
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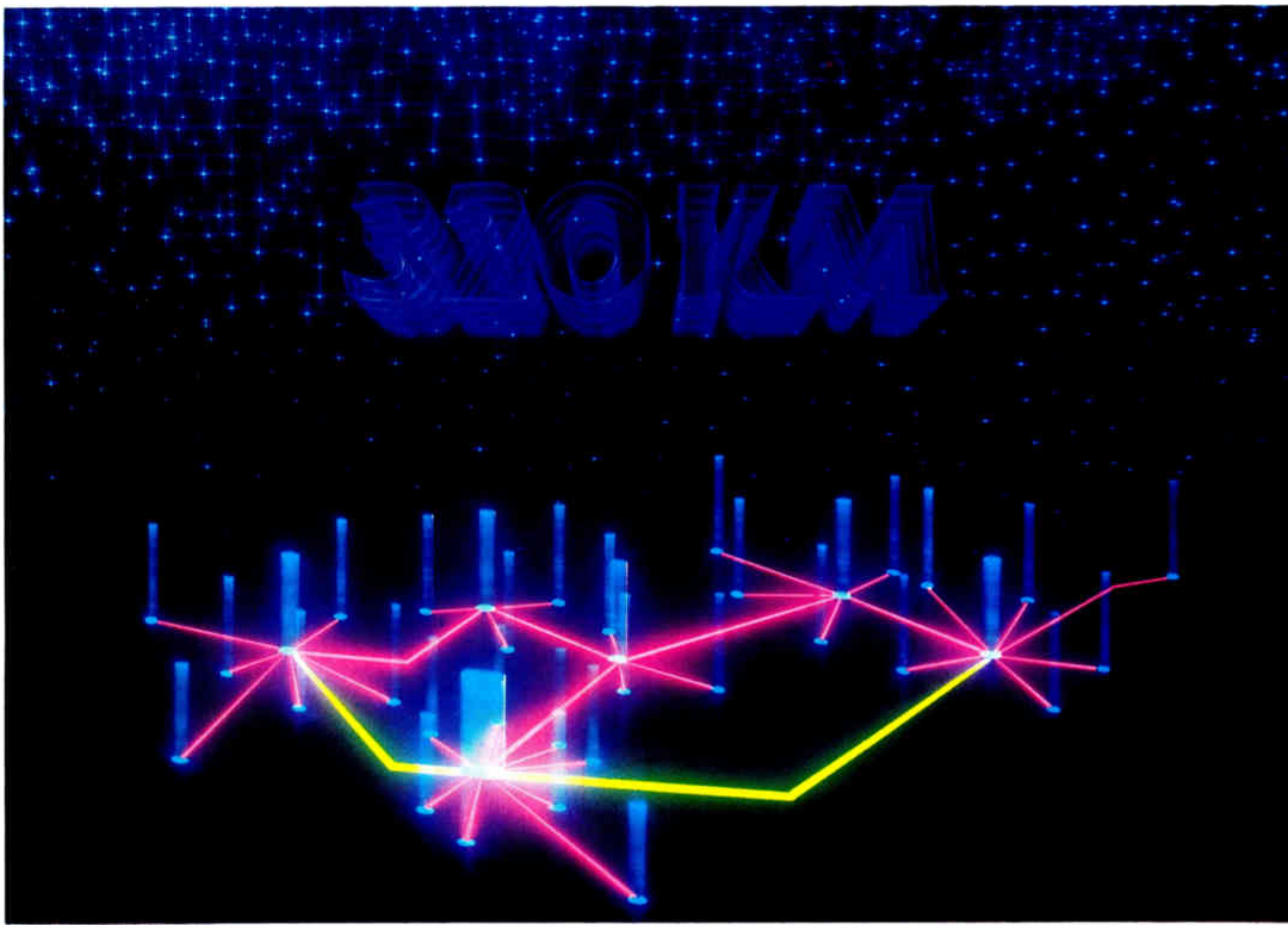



# 320-KM FIBER OPTICS DIGITAL TELEPHONE SYSTEM FOR BUENOS AIRES

NEC will soon start constructing an ultra-modern telephone network in Buenos Aires under the terms of a contract recently signed with ENTEL, Argentina's national telephone authority.

The system will be the largest digital switching network ever to be built in a single city and will incorporate high-capacity fiber optics transmission systems, also the largest of their kind.

The new digital telephone network will have 6 tandem exchanges and about 60 telephone offices interconnected by means of large-capacity transmission lines. Each tandem exchange will have circuits equivalent to 80,000 subscriber lines and will be provided with a NEAX61 digital switching system.

A 140 mbps (1,920 telephone circuits) fiber optics transmission system will be used to interconnect the tandem exchanges. A 34 mbps (480 telephone circuits) fiber optics system will be employed to interconnect the tandem exchanges and telephone offices. The length of these optical systems will be 80 and 240 kilometers, respectively. The transmission links will be backed up 100% by an advanced, fully solidstate digital microwave system operating at 11 GHz. Cut-over date is scheduled for the end of 1981.

## WORLD'S LARGEST-CAPACITY FPLA.

NEC has introduced the world's first 9,216-bit bipolar field programmable logic array. The new product, called µPB450D, can bring about tremendous reductions in the size, cost and power consumption of electronic digital control systems while improving availability, turn-around time and design flexibility.

The new product has 9,216 programmable points in the form of AND- and OR-arrays, as well as 16 J-K flip-flop feedback loops. Flexibility is an outstanding feature of the device which allows the customer to achieve any kind of sequential logic by programming the 9,216 points arbitrarily.

It is contained in a 0.6-inch width, 48-lead, dual-in-line package with 24 inputs, 16 outputs and 6 control terminals. It works in TTL levels with a single 5-volt power supply; power consumption is 600mW typ. (1.1 watts max.); input-to-output time delay is

100 nsec typ. (200 nsec max.).

A medium-speed device, µPB450D is highly suitable for microcomputer-control circuits. Applications include both industrial and consumer electronics. The range goes from peripheral and terminal equipment to TV games and electric washing machines.

Circle 87 on reader service card

## MNC-80A PORTABLE CAMERA FOR ACTION TV.

TV audiences are demanding more dynamic and varied programs. This, in turn, creates a need for versatile, high-performance cameras that can be used with equal ease in the studio or out on location. NEC has been responding to this need with a growing line-up of advanced television cameras.

The latest offering is the MNC-80A series fully self-contained portable color camera. Light enough for hand-held operation, it is engineered for maximum stability and reliability both in the studio or out in the open air.

The MNC-80A weighs only 4.5 kg and measures 260mm (h) x 100mm (w) x 293 mm (d). Yet it produces pictures of astounding clarity, and because its circuitry is based on extensive use of LSIs, the MNC-80A consumes significantly less power than comparable cameras. In fact, it runs on a mere 24 watts.

The MNC-80A series comes with a wide range of accessories; models are available for NTSC, PAL, PAL-M and SECAM standards.

Circle 86 on reader service card

## NEAX61 SYSTEMS IMPROVE PHONE SERVICE IN RURAL IRAQ.

NEC has won a major contract to improve telephone services in rural districts of Iraq with ultra-modern digital switching systems. Under the terms of the contract, NEC will manufacture and install a total of ninety NEAX61 rural digital switching systems, plus a digital radio communications system to interconnect the new switching network.

The NEAX61 rural digital switch is capable of accommodating 50 to 1,500 subscriber lines. It is a smallish version of the popular NEAX61 for central office use.

The digital radio system will consist of 30-station 28 microwave links using PCM 240/480-channel equipment, and 86-station 62 UHF links using PCM 60-channel equipment.

To lower the construction cost and hasten installation, most of the telephone offices will house their switching systems and radio equipment in container-type shelters. Some offices located in deserts will be unattended, and controlled and maintained centrally.

NEC plans to complete Iraq's new digital telephone network in 1982.

NEC
Nippon Electric Co., Ltd.
P.O.Box 1, Takanawa, Tokyo, Japan

# IEDM: progress report on tomorrow

26th annual meeting will lift the lid on materials, technologies, and processes for parts ranging from discrete devices to VLSI circuits

*by John Posa, Solid State Editor, and Roger Allan, Components Editor*

**Each year, those** attending the International Electron Devices Meeting walk away convinced that the device designers have outdone themselves: there is simply no way they can top their performance for next year's edition. But each year they do.

This, the 26th annual meeting, will be held Dec. 8–10 at the Washington (D. C.) Hilton hotel. And once again the program's 200-plus papers—a third from overseas—spotlight the new tricks that device designers have taught electrons.

Very large-scale integrated circuits are approached in terms of submicrometer lithography and multiple self-aligned structures that promote miniaturization. Novel random-access and nonvolatile memory cells are presented; complementary-MOS and bipolar technologies are each awarded more than an entire session apiece. Higher-power, yet more easily activated, thyristors are introduced, as are clever new ways to sense and display information.

Unlike a circuits conference, which emphasizes finished ICs, the IEDM emphasizes the underlying process enhancements that will spawn the next round of faster, denser circuits. So materials technology is important, and new light is shed on the properties and uses for polycrystalline and amorphous silicon, gallium arsenide, and refractory metal silicides.

On memories, Mitsubishi tells how the Hi-C dynamic RAM cell helps ward off alpha particles, Nippon Electric shows off a RAM cell that is half the size of present ones, and Toshiba has a fast 2-K-by-8-bit static RAM up its sleeve.

In the nonvolatile memory area, Fujitsu has an electrically erasable read-only memory cell with more efficient electron transfer and retention. Using a 5-nanometer tunnel oxide, Hitachi built an EE-PROM that programs in 50 nanoseconds. By adding a third polysilicon level, Mostek realizes an EE-PROM having just one transistor per bit. IBM electrically alters a programmable logic

HIGHLIGHTS OF THE IEDM

| SESSION | PAPER | SOURCE |
|---|---|---|
| **Monday, Dec. 8** | | |
| 2.1 | VHSIC Technology Barriers | U.S. Navy |
| 2.5 | E-PROM Programming at Reduced Dimensions | Toshiba Corp. |
| 3.1 | Polycrystalline Bipolar IC Devices | Philips Research Laboratories |
| 3.2 | Bipolar Memory with Polysilicon Loads | Toshiba Corp. |
| 3.4 | Symmetrical Bipolar Structure | IBM Watson Research Center |
| 3.6 | Complementary Transistor for Analog ICs | Nippon Electric Co. |
| 4.3 | FET-Controlled Sipmos Thyristor | Siemens AG |
| 5.1 | 30-GHz Gallium-Arsenide FETS | Toshiba Corp. |
| 6.1 | Laser-Programmed Vias for VLSI | MIT Lincoln Laboratory |
| 6.2 | Self-Aligned Contact Technology | Nippon Electric Co. |
| 6.3 | Self-Registering MOS Transistor | Hewlett-Packard Co. |
| 8.6 | Polycrystalline SIS Solar Cells | Colorado State University |
| **Tuesday, Dec. 9** | | |
| 9.2 | Multilayer Polycrystalline Structures | Stanford University |
| 10.1 | Bulk Silicon Versus SOS for C-MOS VLSI | Mitel Semiconductor Inc. |
| 10.2 | Latchup-Free C-MOS | Bell Laboratories |
| 10.3 | The Parasitic SCR in Bulk C-MOS | Harris Semiconductor |
| 10.5 | Parasitic Capacitance in C-MOS SOS | Rockwell International Corp. |
| 13.6 | CCD for 2/3-in. Color Camera | Toshiba Corp. |
| 14.1 | Lasers Grown with Molecular-Beam Epitaxy | Bell Laboratories/Western Electric Co. |
| 15.1 | Bipolar–JFET–$I^2L$ Process | University of California at Berkeley |
| 15.2 | 1-GHz Multicollector ECL | Toshiba Corp. |
| 15.5 | GaAs Bipolar Integrated Circuits | Texas Instruments Inc. |
| 16.5 | Status of X-ray Lithography | IBM Corp. |
| 16.7 | Electron-Beam Direct Writing | NTT Musashino Laboratory |
| 17.2 | Advanced Processing for GaAs ICs | Hughes Aircraft Co. |
| 17.3 | GaAs IGFET for High-Speed Digital ICs | Wright Patterson Air Force Base |
| 20.4 | Recent Advances in GaAs Solar Cells | MIT Lincoln Laboratory |
| 20.6 | High-Efficiency Amorphous Solar Cells | Energy Conversion Devices |

SOURCE: *ELECTRONICS*

array, and Toshiba says just how small an ultraviolet-light–erasable ROM cell can get.

Other papers describe how polysilicon is laser-annealed to serve as an insulating substrate and doped to form active and passive elements—now in bipolar circuits, too. Polysilicon also turns up in three-dimensional devices; in different sessions, models are presented for these silicon sandwiches. Amorphous silicon is employed both for solar cells and for integrated inverters. For the first time, gallium arsenide is used to build bipolar circuits and insulated-gate field-effect-transistor counters and dividers.

Some authors put complementary-MOS on bulk silicon, others put it on sapphire, and still others compare the two approaches. To match the n- and p-channel devices in C-MOS, Bell Laboratories adopts an eight-mask "twin-tub" approach. Similarly, in bipolar technology, NEC uses 10 steps to match npn and pnp transistors in analog ICs. And IBM constructs lateral pnp and vertical npn transistors that conduct current in both directions.

Unique constructions will also merge technologies in new ways to exploit their synergism. Siemens AG combines power MOS and bipolar processes. The University of California at Berkeley mixes bipolar technology with junction FETs and integrated injection logic for faster circuits.

**More FET news.** Not only are FETs handling high voltage and currents better, but new structures such as Sipmos (for Siemens power MOS) FETs and Resurf junction FETs will also be unveiled. In particular, look for an interesting discussion from Siemens researchers on how they apply their Sipmos power FET technology to functionally integrated MOS and to FET-controlled thyristors. The Resurf JFET is a lateral power device from Philips Research Laboratories in Eindhoven, the Netherlands, that can handle higher currents than conventional JFETs.

On thyristors, one of the more interesting papers is on a 6-kilovolt, 1.5-kiloampere light-activated thyristor from the Hitachi Research Laboratory in Japan. In another paper on a light-activated thyristor, researchers from Brown Boveri Research Center in Baden, Switzerland, propose a solution to the thorny problem of optically turning off thyristors. Noteworthy is a paper from the Soviet Union's Physics Technologic Institute, Leningrad, on a high-power subnanosecond switch. Currents of 30 to 40 amperes were switched in less than 0.2 nanosecond at voltages of more than 2 kV.

**More sensors.** The proliferation of microprocessor technology is hastening the development of sensors to serve as the eyes, ears, and nose of microprocessor-based circuits—one session has no fewer than eight papers on this topic. Included are discussions of a silicon microtransducer for measuring the magnitude and direction of a magnetic-field vector, a micromechanical accelerometer integrated with MOS detection circuitry, and an MOS chip for monitoring IC package moisture and IC surface impedance. Still other sensors discussed include an IC infrared thermopile detector and thin-film pyroelectric anemometers for flow measurements.

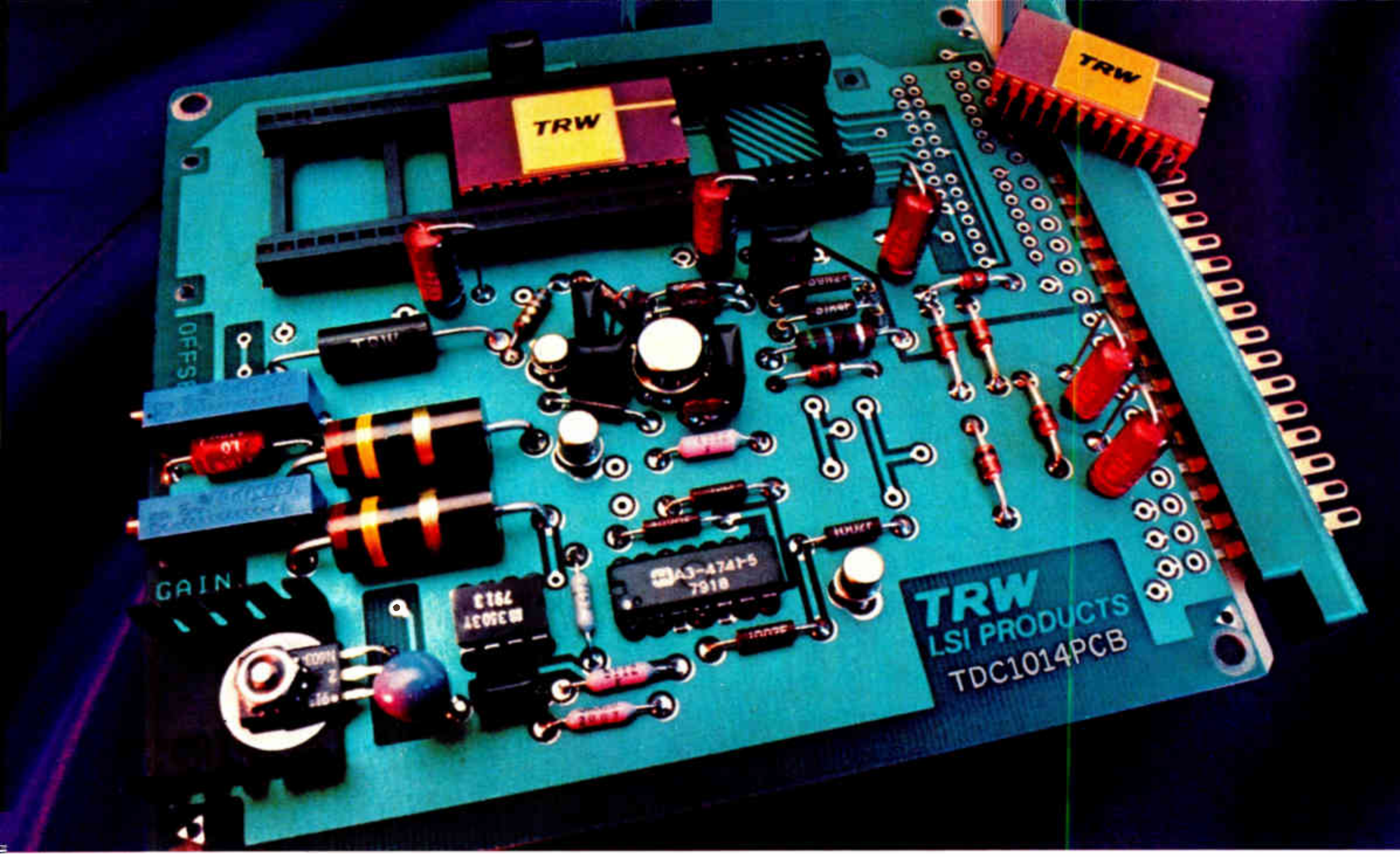
One hot topic is display technology. Researchers from Fujitsu Laboratories in Japan and the Rockwell Electronics Research Center in California disclose their feelings on ac thin-film electroluminescent displays, a technology suitable for large flat panels. The invited paper is on how to matrix-address flat-panel displays, at present a complex problem, and is written by Larry Tannas Jr. of Aerojet ElectroSystems Co., a well-known authority on flat-panel displays.

To register for the IEDM, contact conference manager Melissa Widerkehr at (202) 296-8100. □

**HIGHLIGHTS OF THE IEDM** (continued)

| SESSION | PAPER | SOURCE |
|---|---|---|
| **Wednesday, Dec. 10** | | |
| 22.1 | Laser-Recrystallized Silicon-on-Oxide | Texas Instruments Inc. |
| 22.2 | Silicon-on-Oxide MOS FETs | Texas Instruments Inc. |
| 22.3 | Thin Oxynitride Gate Dielectrics | MIT Lincoln Laboratory |
| 22.4 | Defect-free Oxidized Polysilicon | Toshiba Corp. |
| 23.1 | Soft Errors and the Hi-C Structure | Mitsubishi Electric Corp. |
| 23.2 | New Dynamic Cell for VLSI Memories | Nippon Electric Co. |
| 23.3 | High-Speed 2-K-by-8-Bit Static RAM | Toshiba Corp. |
| 23.4 | EAROM with Graded-Energy Band Gap | Fujitsu Ltd. |
| 23.5 | 50-ns 15-V Nonvolatile Memory | Hitachi Ltd. |
| 23.6 | Electrically Alterable Logic Array | IBM Corp. |
| 23.7 | Triple-Level-Polysilicon EE-PROM | Mostek Corp. |
| 24.1 | Permeable-Base Transistors | MIT Lincoln Laboratory |
| 25.2 | 6,000-V, 1,500-A Light-Activated Thyristor | Hitachi Ltd. |
| 25.4 | Gate-Turnoff Structures | RCA/NJIT |
| 25.7 | High-power Subnanosecond Switch | Physics Technologic Institute |
| 26.1 | Discrete and Integrated Optoelectronics | Rockwell International Corp. |
| 27.1 | Matrix-Addressed Flat-Panel Displays | Aerojet ElectroSystems Co. |
| 27.3 | 68-line Multiplexed Liquid-Crystal Display | Bell-Northern Research |
| 27.5 | Thin-film Electroluminescent Display | Fujitsu Ltd. |
| 29.1 | Twin-Tub C-MOS for VLSI | Bell Laboratories |
| 29.2 | Buried-channel MOS FET with Implanted Oxide | NTT Musashino Laboratory |
| 29.3 | Totally Self-Aligned MOS Transistor for VLSI | Rockwell International Corp. |
| 29.5 | Electron-beam Lithography for VLSI | Texas Instruments Inc. |
| 29.6 | Electron-beam Lithography for VLSI | Bell Laboratories |
| 29.7 | Electron-beam Lithography for VLSI | Texas Instruments Inc. |
| 30.4 | The Junction-MOS Transistor | Hewlett-Packard Co./Dortmund |
| 30.7 | Amorphous Silicon Inverter Circuit | Tokyo Institute of Technology |

SOURCE: *ELECTRONICS*

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Instruments

# At Interkama, the beat is lively

Survey made on eve of West German show predicts worldwide instrumentation and automation sales in 1980 of $56 billion

by John Gosch, Frankfurt bureau manager

**In good times** or bad, makers of control and automation equipment have something going for them. If it is not their customers' drive to boost productivity by automating manufacturing operations, it is industry's need to make better use of energy and raw materials by optimizing production processes. And if it is neither of those, the control systems market gets a lift from governmental and public clamor for cleaner air and rivers.

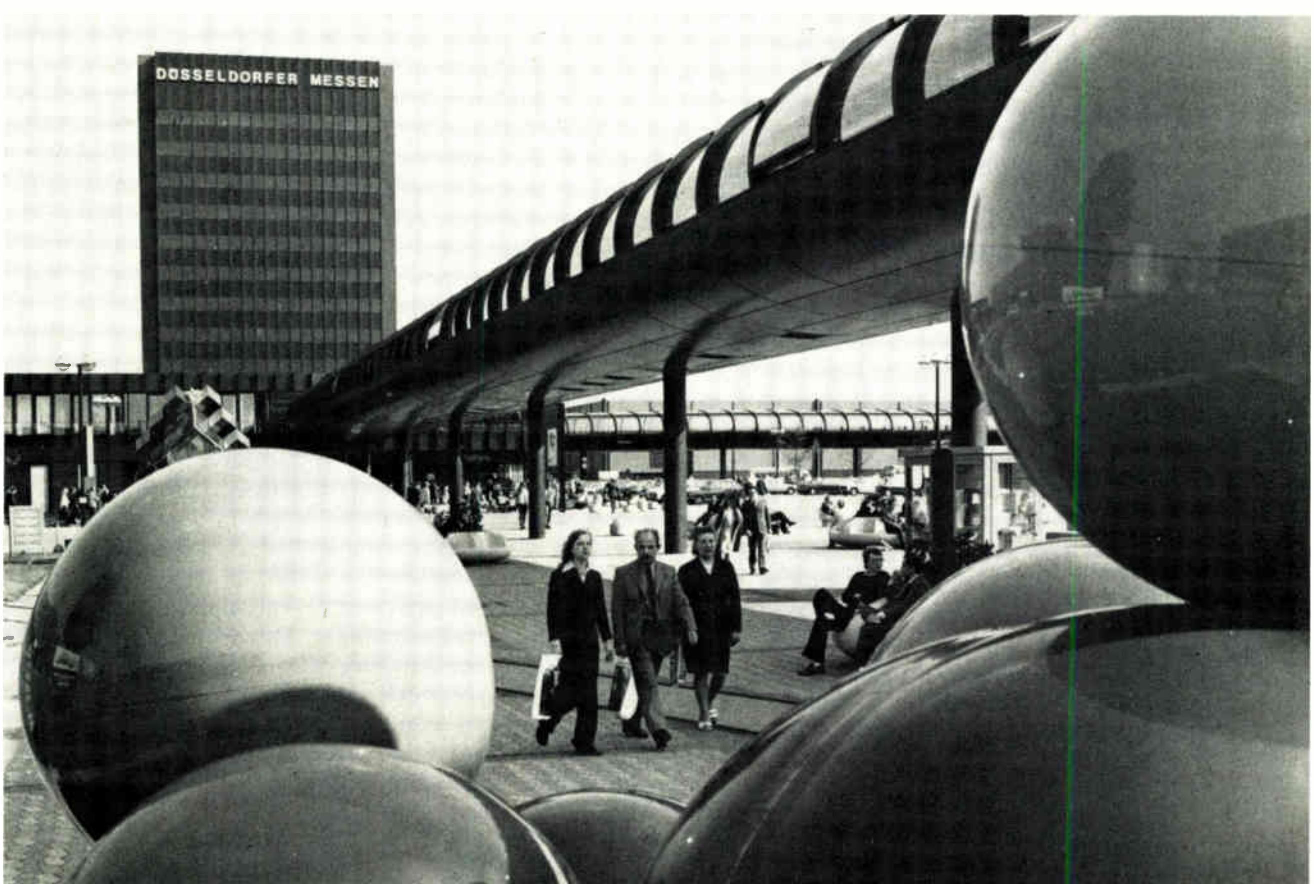
It is little wonder, then, that equipment makers will be in a buoyant mood at the Oct. 9–15 Interkama Exhibition in Düsseldorf, West Germany. Staged in the bustling North Rhine–Westphalian capital every three years and devoted solely to instrumentation and automation gear, Interkama has become the world's largest exhibition in this field since it was launched in 1957.

But Interkama is more than a forum for new equipment. What also makes the event a mecca for control engineers is the concurrently held scientific congress, where topics range from new sensing devices to process analyzers, weighing technology, quality control, and the structure of complex automation systems. Adding to the show's appeal are applications-oriented seminars and a side exhibition on applied research.

This year's show is expected to draw more than 100,000 persons to Düsseldorf's sprawling fairgrounds along the shores of the Rhine River. Spreading their wares over roughly half a million square feet will be over 1,000 firms from 25 countries. About one third of the visitors and more than one fifth of the exhibitors will come from abroad.

Equipment suppliers and their systems-designing customers will flock to Interkama as much to get a look at what's new on the stands as to get a fix on the instrumentation and automation market. In a nutshell, that market, unlike some others in electronics, is doing very well and is

**Making instrumentation news.** That is the reputation of Interkama, the big triennial show in Düsseldorf, West Germany, that underlines instrumentation and automation advances. The world's largest show in its field, it will take place Oct. 9–15 at the city's fairgrounds.



expected to continue the steady climb it has enjoyed during the past two decades or so.

For the first time, the experts have made a truly global assessment of that market. Three West German industry groups—the Central Association of the Electrotechnical Industry, the Association of German Machine Builders, and the Association of the German Precision Mechanical and Optics Industry—have included the Eastern Bloc, something most others exclude.

Their estimates: the 1980 worldwide business in instrumentation and automation could reach about $56 billion. This figure not only encompasses the cost of hardware (including process computers and industrial robots), but also software, engineering, hardware installation, maintenance, and repair.

**Software up.** Of note, the West Germans point out, is the rising cost of software. For an average instrumentation project, the software cost currently accounts for half the total investments, whereas hardware claims only a 20% share. The remaining 30% is for installation and checkout.

Turning to growth, the experts peg the average worldwide rise for instrumentation and automation sales at about 9% a year for the near term. There are noticeable regional differences, of course. Although in some dynamic developing nations like Saudi Arabia and other oil-exporting countries the market is spurting ahead at well over 15%, in most industrialized nations, including the U. S., it is climbing at a respectable 12%.

Today, several factors combine to keep the market growing vigorously. Besides the industry's ongoing push to cut labor costs and thus to achieve higher productivity, "there is now a strong need to optimize production processes with a view toward keeping the cost for energy and raw materials low," says Pieter W. van der Wal, manager for industrial automation at the Scientific and Industrial Equipment division of NV Philips Gloeilampenfabrieken in the Netherlands. And with the energy and materials costs constantly on the rise, that need becomes all the more pressing. Also buoying the market is the drive to eliminate human error in production processes "in an effort to increase both product quality and yield," van der Wal points out.

Horst Kaltenecker, scientific consultant in the control systems development group at Siemens AG in Karlsruhe, sees the drive to humanize the work place as another market stimulus. "The more intelligent the means at his disposal, the more the human controller's job of reaching a decision is eased," he says. Aids in the decision-making process are intelligent information-handling and -analyzing systems, as well as sophisticated monitors and other display devices.

**Pollution control.** Still another factor in market growth is the environmentalists. Although industry feels that outlays for pollution control should not come at the expense of plant expansion or modernization, most people still seem to want a better environment.

Aside from providing a fix on where the market is going and what is influencing it, Interkama is also a good place for spotting technological trends in instrumentation and automation. Probably the most significant trend visitors will note this year is that toward more microprocessor applications. Such devices may well be the prime topic at the show as more and more control-systems designers become aware of what they can do in measurement, analytic, control, and test equipment.

Says Kaltenecker of Siemens, "The big price reduction in microelectronic functions that can be performed with microprocessors allows designers to apply such devices economically and have them solve tasks that are difficult to handle by analog means." The low cost per function also makes it possible to distribute intelligence in an automated plant and use microelectronic devices redundantly. "That makes for more systems reliability," Kaltenecker points out.

Another trend picking up steam is the application of fiber optics. Optical couplers and transmission links, including complete fiber buses, are already in use. The big advantage of fiber links is their immunity to electrically noisy environments in which control equipment must often operate. However, Philips' van der Wal does not see a significant breakthrough in the use of optical components coming for another five years or so.

Also coming to the fore are microprocessor-oriented distributed-processing computer systems for handling all automation functions, including open-loop and closed-loop control, but allowing centralized operation and supervision of the controlled processes. Such distributed systems, which in a sense constitute a symbiosis of computer and controller, do not necessarily mean a move away from the superimposed process computer. The computer still retains its key role, although the hierarchical structure of process-controlled automated plants will move more and more in the direction of decentralized subsystems. □

## Microelectronics moving into machines

Fueling the optimism being generated by a forecast of the global market for instrumentation and automation gear made by three West German industry groups, one of them, the Association of German Machine Builders, points out that the use of microelectronics in machines is still in its infancy. According to the association, of the 1,300 different machine types it has investigated, about 37% still incorporated electromechanical components, 22% electronic circuitry, 17% purely mechanical controls, another 17% hydraulic and pneumatic gear, and only 5% microelectronic devices.

"But the 5% does not reflect the significance machine designers attach to microelectronics," an association official says. Of the machine-building firms it has surveyed, 46% are just getting acquainted with microelectronic devices, 30% are planning to use such components, and another 30% are already designing with them. What it boils down to is that only 7 out of 100 firms have not yet concerned themselves with microelectronic applications, the association says.

-J. G.

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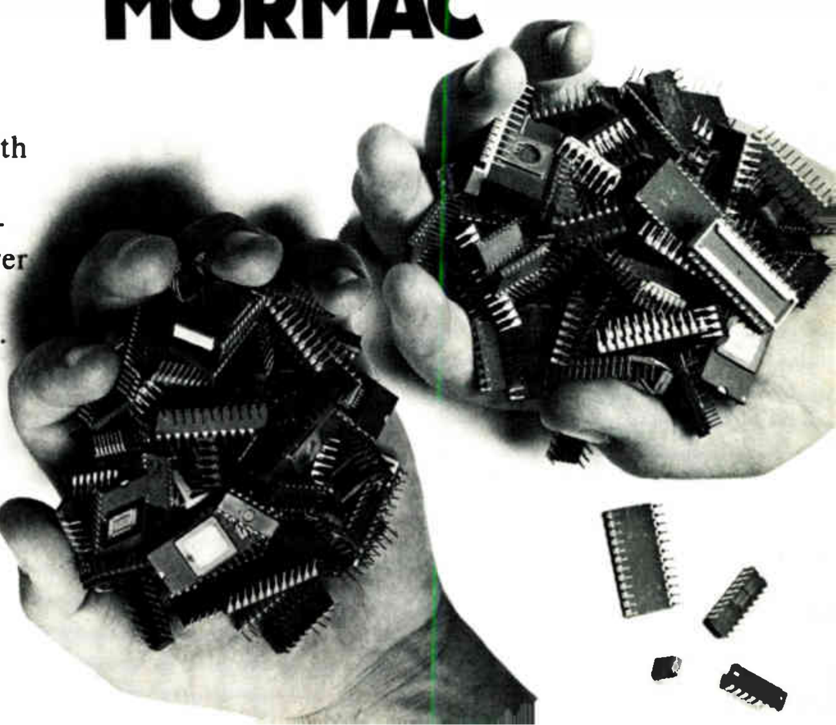

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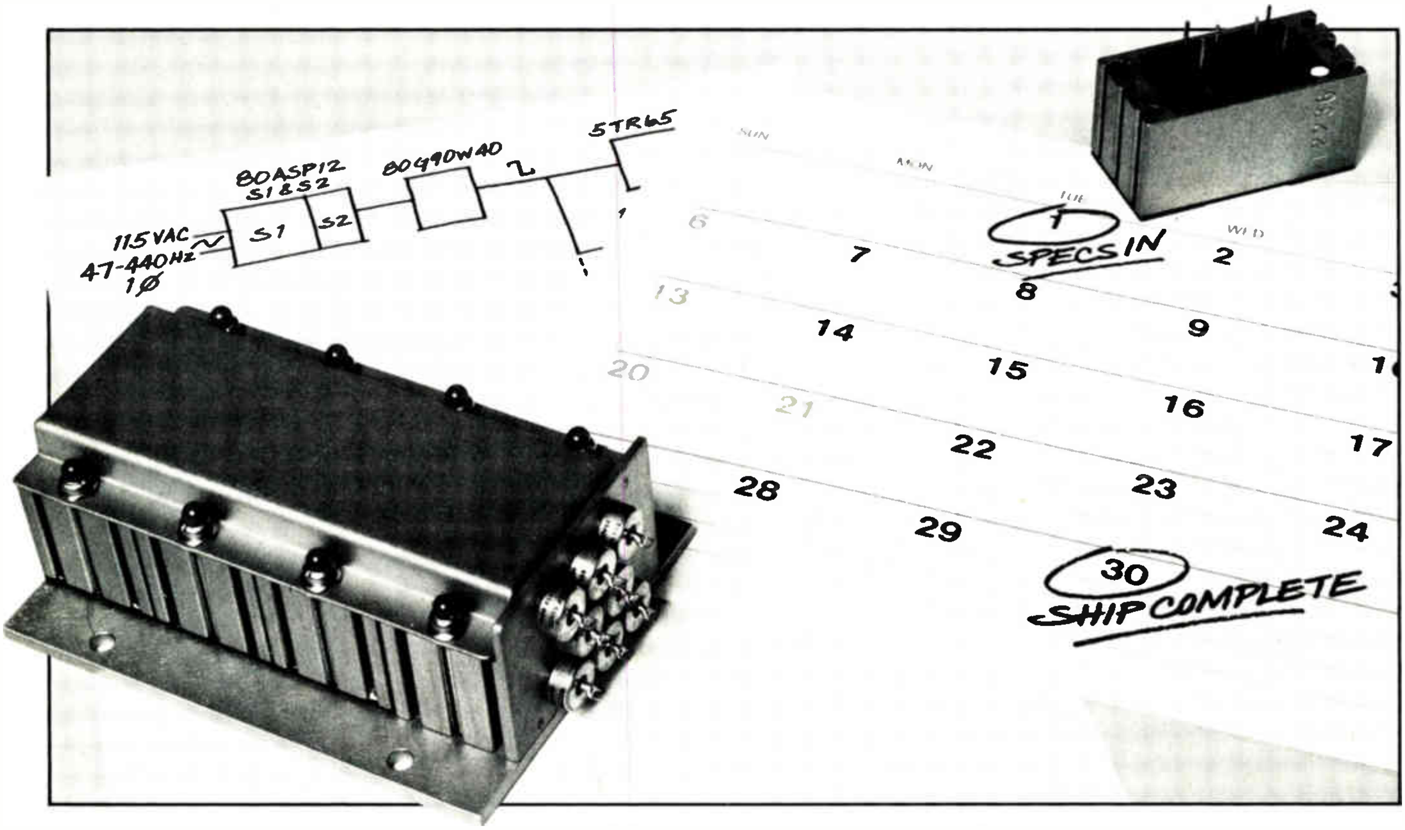


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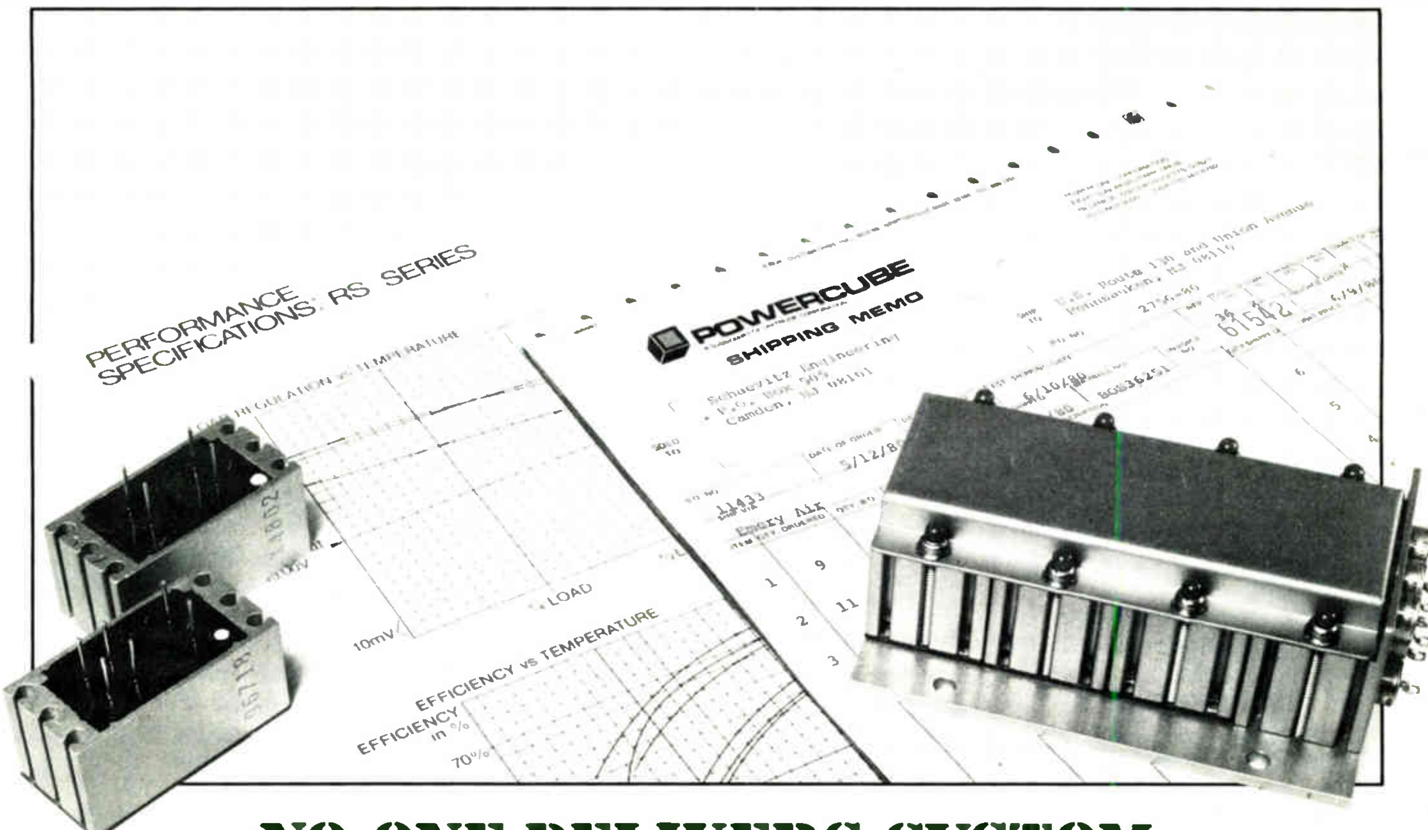


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Microcomputers

# IEEE readies backplane standard

'Future bus' for 16-, 32-bit machines leaves processor makers cold, but independents and Europeans are expected to use it

by Martin Marshall, West Coast Computers & Instruments Editor

**The instruments have** changed, but the tune is familiar. When 8-bit microcomputer systems began selling, they came with almost as many different backplane packaging and arbitration proposals as there were microprocessor makers. Now, before much the same thing can happen to 16- and 32-bit systems, the Institute of Electrical and Electronics Engineers has attempted to come up with a processor-independent standard for backplane bus configuration and arbitration.

But the task is not an easy one. Microprocessor makers like their own schemes for the backplane, which is a fixed number of conductive paths into which a printed-circuit board can be plugged. Since it serves as the major bus for data communication between boards in any piece of equipment, a manufacturer can tailor the backplane to the architecture of the individual microprocessor and lock the customer in to his unique criteria for processor configuration and control.

However, even if none of the major semiconductor manufacturers produces microcomputer, memory, and peripheral boards that conform to the proposed IEEE P896 standard, there are likely to be independent board and system manufacturers that will. One reason is that the proposed standard uses double-Eurocard form factor and 96-pin DIN 41612 connector for its boards. European manufacturers are eager to use this format, but they have yet to develop common arbitration protocols for bus control and interrupt vectors. A potential International Electrotechnical Commission standard for these protocols, as well as for data-transfer specifications, would go a long way toward popularizing the Eurocard approach to 16- and 32-bit multiprocessor systems.

The P896 is referred to as the "future bus" by industry participants because it provides for 32-bit microprocessors that have not yet been announced. The IEEE committee, which includes both American and European groups, has proposed standards for a 32-bit–address, 32-bit–data backplane, and for a 24-bit–address, 16-bit–data subset. Moreover, its proposal accommodates both multiplexed and nonmultiplexed versions of these address-and-data combinations. The committee defines the function of the backplane bus as the transfer of bus control, program control (via interrupts), addresses, and data.

Understandably, the committee's chairman, Andrew Allison, a microcomputer consultant in Los Altos, Calif., is enthusiastic about the proposal. "This could do for microcomputers what the IEEE-488 standard has done for instrumentation," he says.

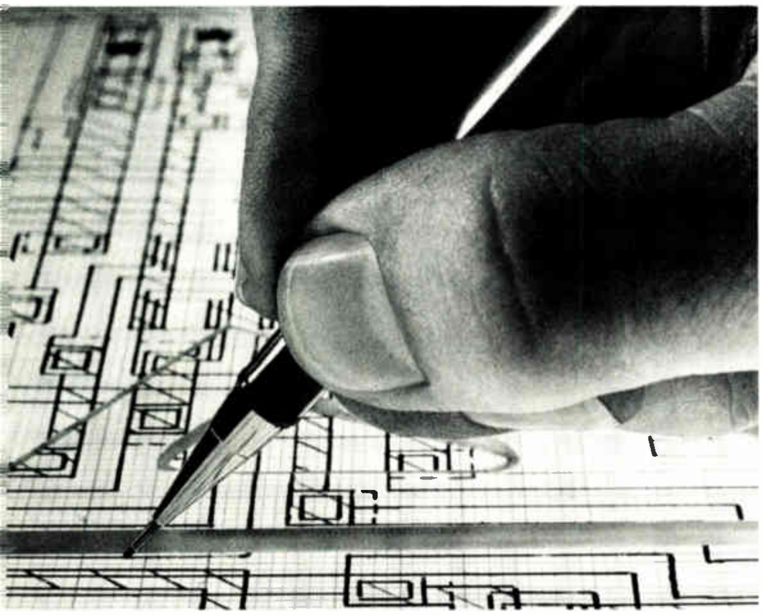
**Built for speed.** The proposed standard does have some technical advantages going for it. For one, it is designed to operate at rates of over 10 megahertz, while Intel Corp.'s Multibus (now formalized as IEEE P796) operates in real systems with rates of about 1 MHz. For another, it would allow the mixing of different processor boards within the same multiprocessor system. "The different processors could each address their own local memory, but they could also share global memory. They could even all be running the same transportable language and execute commands out of the same memory," notes Rollie Linser of Monolithic Systems Inc., Englewood, Colo.

The future bus, if it becomes an IEEE and IEC standard, will enter a field that is already populated with competitive buses produced by the U. S. semiconductor manufacturers. Intel's Multibus, which supports the architecture of the 8086 and 8088, is already the dominant 16-bus structure. It even dominates the Eurocard configuration in Europe. However, the Multibus is currently defined only for 20-bit–address, 16-bit–data configurations, and there is some question of how it can be expanded. Next come two 32-bit–address, 32-bit–data structures, the Versabus

## Something for the designer

The proposed standard suggests specific backplane pin assignments, as well as error detection and correction techniques, but it leaves to the designer the task of figuring out how to balance the speed and load characteristics of a large system built around the proposed backplane. Those who use the proposed standard will probably consider speed-load tradeoff to be secondary, however, and they will surely be grateful that the committee has presented them with a common set of arbitration procedures. It should be noted, however, that the bus proposal must still go through the slow process of review before becoming standard. **-M. M.**

# "Every time we ask a MOS/LSI company about their custom experience, they change the subject."



That's no surprise. Most MOS/LSI companies take on custom work only when market conditions force them to. And, no matter how big they may seem, they're usually only willing to handle a few limited jobs. So they really don't have much custom experience worth talking about.

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**Expansion-minded.** As it happens, a Multibus expansion has been the prime focus of the IEEE's P796 committee, which is further along with its work than the P896 group and will publish its specifications next month. According to committee member Rod Allen of Microbar Systems Inc., Palo Alto, Calif., those specifications will reveal the assignment of four new address pins to the Multibus, bringing its total to 24 address bits and 16 data bits. Allen also notes that the committee has decided to reserve up to 24 additional pins on the P2 connector of the Multibus for expansion. If 8 of those pins are used for address and 16 for data, then it is possible that the Multibus could be extended to 32 address bits and 32 data bits.

Intel, which is sensitive about commenting upon bus structures produced elsewhere, is reluctant to speculate about the chances of the future P896. A company spokesman would note only that "Intel prefers creating standards to following them. The company has no plans to use the P896 specifications."

Motorola and Zilog similarly say they have no product plans, but both leave the door open should the future bus take hold. Richard Lyman, Zilog's engineering manager for original-equipment manufacturer products, comments: "There will be some companies that will produce cards for the future bus, but I don't think it will really take off until someone develops an LSI chip that performs the bus interface. The fact that the Europeans are involved in the future bus, however, gives it additional clout." Lyman, who is Zilog's observer on the committee, believes that it has come up with a good bus arbitration scheme, but that it is still a bit vague about handling interrupts. "To implement the interface would at present take several SSI TTL chips. That is why the LSI chip is needed," he observes.

**Practical view.** Motorola's observer on the committee, Thomas Balph, a systems specialist in the microsystems strategic marketing group, takes a pragmatic view: "If it gains a wide acceptance, we would have to create some support for it." □

## Equal chance for all

The arbitration scheme of the "future bus" envisioned by the proposed IEEE P896 standard is certainly more egalitarian than existing backplane schemes, because its bus priority is not a function of slot location. Instead, the proposed standard provides a bus arbitration scheme in which up to 64 bus masters can command equal access to the bus. Priorities are hardwire-selected, but the scheme also provides a way to keep one high-priority module from hogging the bus. It allows a small class of bus-requesting modules to protest failure to win an arbitration by raising their priority status for the next arbitration. According to the standard-writing committee, this scheme prevents the monopolizing of either the bus or interrupt facilities.

Multitasking control on the future bus is facilitated by two modes of operation in the interrupt-priority arbitration scheme. One mode first determines which bus master has the highest-priority interrupt, then places that bus master's number and the level of the interrupt's priority on the interrupt vector line. A second mode schedules future tasks by determining the priority and locations of the highest-priority pending task and matching it to the lowest-executing task. Up to 1.024 interrupt priority levels are provided in the proposed standard.

The proposal calls for bus arbitration to be carried out independently and in parallel with other bus operations. The arbitration is initiated on the falling edge of the bus clock, and it must be completed within one bus clock cycle. Specified as active-low open-collector lines are the bus request line, bus busy line, and bus priority lines. In order to execute indivisible bus operations, a local lock signal is also provided. This lock prevents the release of the bus for as long as a particular processor takes to complete the operation. The interrupt arbitration scheme uses serial polling. **-M. M.**

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Computers

# TRW-Fujitsu venture has the potential

New joint company helps each partner, as TRW gets aid for POS gear and Fujitsu gains entry to U. S. market

*by Larry Waller, Los Angeles regional editor*

**If TRW Inc.** and Fujitsu Ltd. can make a go of their fledgling joint venture aimed at cracking the U. S. data-processing business, its success should have some far-reaching effects. A thriving TRW-Fujitsu Co. would immediately approach major status in the world's No. 1 marketplace for such equipment and services. In the longer run, the unique arrangement, which amounts to a true joint enterprise—unlike largely one-sided ventures that previously had little impact—could point up a better way to channel foreign investment into high-technology U. S. operations.

The venture, announced in May after months of ticklish negotiations [*Electronics*, May 22, p. 48], brings together the largest Japanese computer manufacturer (1979 sales of $2.1 billion) and a firm that for more than 20 years has made passes at getting into this business (see "Looking for a way in," p. 104). Under the agreement, Fujitsu contributes cash, computer products already proven in Japan, and technology. For TRW's part, it provides the marketing and distribution organization (mostly its existing Communications Systems and Services division). Not included are TRW's profitable service operation, which, however, will work for the new firm, nor its manufacturing operation, which still turns out terminals for financial and retailing customers and point-of-sale (POS) equipment.

**$100 million deal.** During the first years Fujitsu will sink some $50 million into the effort, for which it gets a 52% interest. Total investment for both sides therefore approximates $100 million.

Judgments on the venture so far focus on the good fit between the partners and the potential. "It's likely to be pretty successful, since it helps both," says computer industry financial analyst Wolfgang Demisch of New York's Morgan Stanley and Co. Besides future payoff, it gives Fujitsu what Demisch calls "a semi-reasonable beachhead" in the U. S. He also says that it "relieves a drain on TRW," referring to plans eventually to shift manufacturing to Fujitsu and to profitability troubles TRW suffered from its terminals and POS equipment.

Even more optimistic about TRW-Fujitsu's chances is J. Garrett Fitzgibbons, who as vice president and general manager runs the venture from its Los Angeles headquarters. Among advantages, he names "cheap startup, with minimum cash from both sides, and keeping the venture's American name in the forefront while we get started." Fitzgibbons has already hired 50 persons to go with the 500 or so TRW already had. Most are engaged in what he and other officials see as top-priority jobs writing programs and assembling operating software packages for introduction of TRW-Fujitsu's initial products, Fujitsu's V-830 small-business computer and its terminals. Plans call for their U. S. debut early next year, with installations to start in the third quarter.

**Sweet tooth.** General manager Fitzgibbons calls new partner "candy shop of products."

**American touch.** The nub of this task is what anyone bringing Japanese products into the U. S. faces: customizing for U. S. users. Though the products are proven, their operation will be somewhat different by the time they get their finishing touches, predicts Fitzgibbons.

Watching the TRW-Fujitsu venture with particular interest is Akira Takei, who heads the U. S. computer subsidiary of archrival Mitsubishi Electric Corp. Not only will the TRW-Fujitsu small-business machine knock heads with his model 18, already being sold in the western U. S. and slated for national distribution in coming months, but what's more, computer veteran Takei ran a Japanese-based joint venture between TRW and Mitsubishi in the 1960s.

His opinion: "Any kind of joint venture is difficult and for small computers very difficult." Takei diplomatically slides over well-documented problems of U. S.–Japanese cooperative efforts but notes that the small-computer business is so competitive and fast-moving it could be the hardest marketing nut for the new kid on the block to crack. Even large computers are an easier target, he thinks.

Sitting at the helm of the new venture, Fitzgibbons holds a post he helped carve out in the protracted negotiations with Fujitsu. The native Georgian was responsible for coming to terms with the operating agreement for the venture, which takes in all-important product planning and manufacturing. As he says, "The intent all along was for me to end up running it." The business and financial side of the agreement was handled by others, especially Fitzgibbons' boss, J. Sidney Webb, now president and chief executive of the joint venture as well as vice chairman of TRW.

After weeks in Japan, where Fitzgibbons and TRW-Fujitsu staff members immersed themselves in the study of Fujitsu's products, both present and planned, and its basic technology, the executive is even more enthusiastic about the potential of the alliance. "It's a candy shop of products and a wealth of technology," he says. "Our primary mission is to bring them to the U. S."

Uppermost is getting Japanese reliability into the venture's new products. This is a particularly touchy point for TRW, whose equipment has had more glitches than desirable in the retail marketplace, where computer-based equipment cannot stand much down time. Its impact is such that TRW's 1979 annual report mentioned high costs and soft demand for POS equipment as a cause for lower profits in its electronics business. This situation played a big part in TRW's determined push for the link with Fujitsu, knowledgeable sources hold.

On this subject, Fitzgibbons observes that Fujitsu's failure rate for such gear "is an order of magnitude better than what we're used to." For example, a controller in TRW equipment now requires 8 to 12 service calls a year, a rate that quickly eats up profits. But its proposed replacement based on Fujitsu designs has a failure rate of only one in three years, dramatically reducing service costs. However, Fitzgibbons notes, such quality control does not come cheaply. "To get it costs money spent on hardware and software designs that have to be extremely reliable," he says.

While the years-off future looks rosy for the combine, Fitzgibbons and others admit to some immediate problems. Chiefly, they worry that current customers will hold off buying TRW equipment during the transition, waiting instead for advanced units. Some evidence of this indeed is showing up in volume figures, which Fitzgibbons puts at about $40 million annually, down from some $60 million less than a year ago.

Morgan Stanley's Demisch also notes this, but sees it as short-term. "Fujitsu intends TRW-Fujitsu as a stepping stone for the long term, and they're willing to throw money into it for at least three years," he says. □

## Looking for a way in

Like many successful technology-oriented U. S. firms, TRW Inc. long has searched for entry into the computer business. Spurred by such top scientists as Simon Ramo, retired vice chairman, and Dean Wooldridge, also retired, TRW about 20 years ago marketed the first major line of digital process-control computers to a broad cross-section of industry. Technically advanced programming and custom applications proved too expensive to make them profitable, so they were spun off into a separate Bunker-Ramo Corp. "We were way ahead of our time," recalls an executive. These machines, however, got TRW into various joint ventures, including one with Mitsubishi Electric Corp., all phased out in the 1960s. Since then the firm again has edged closer to computers through its terminals and point-of-sale gear, now a part of the TRW-Fujitsu joint venture. **-L. W.**


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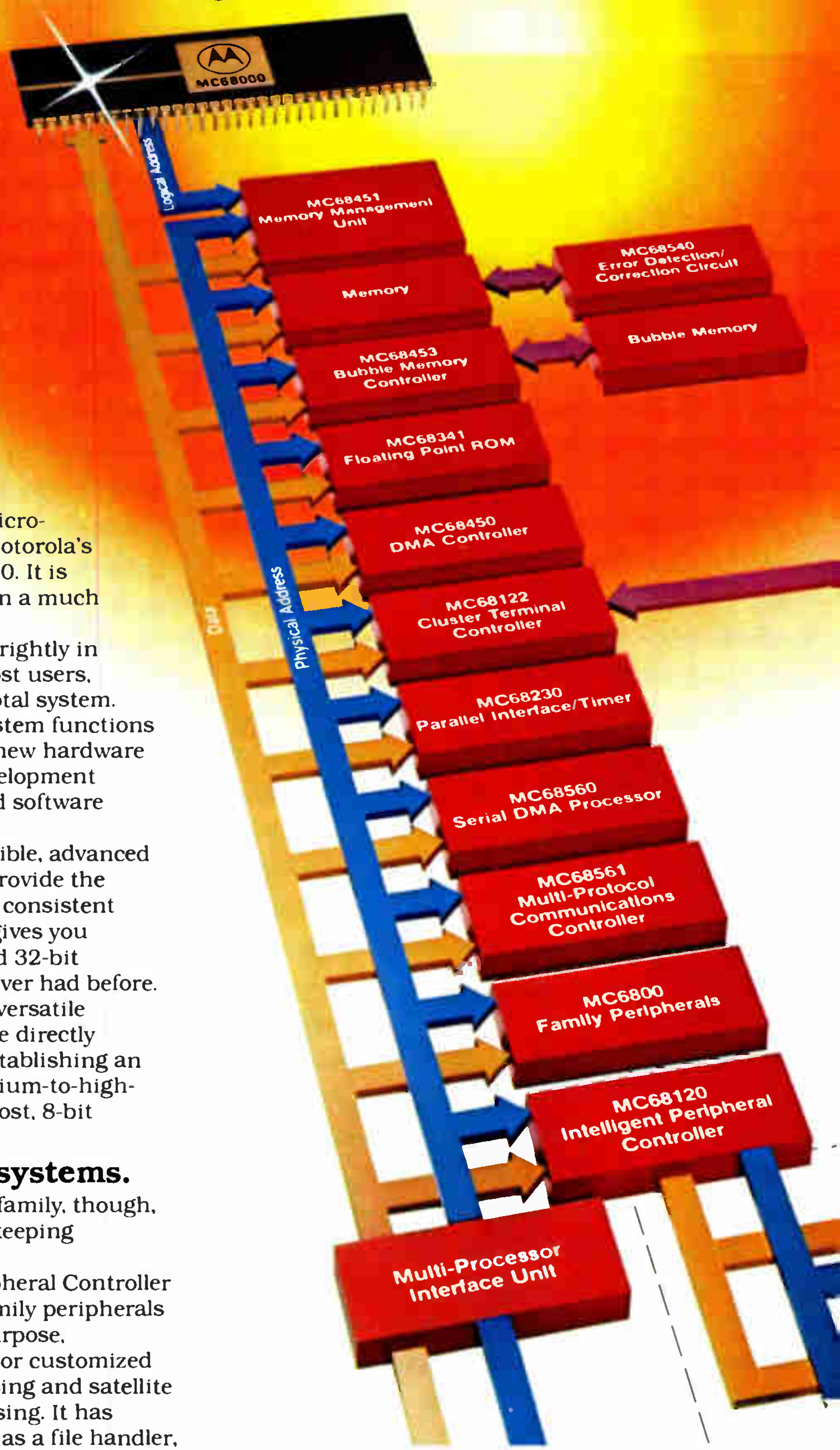


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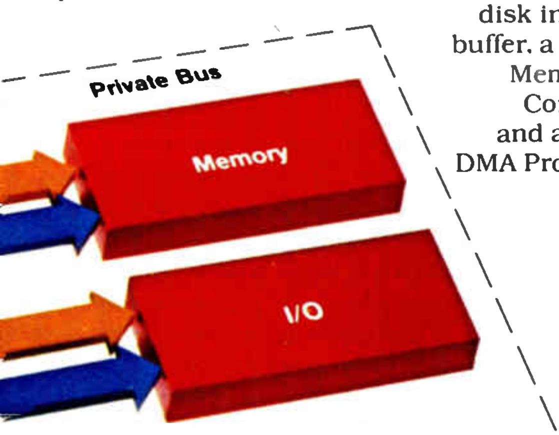


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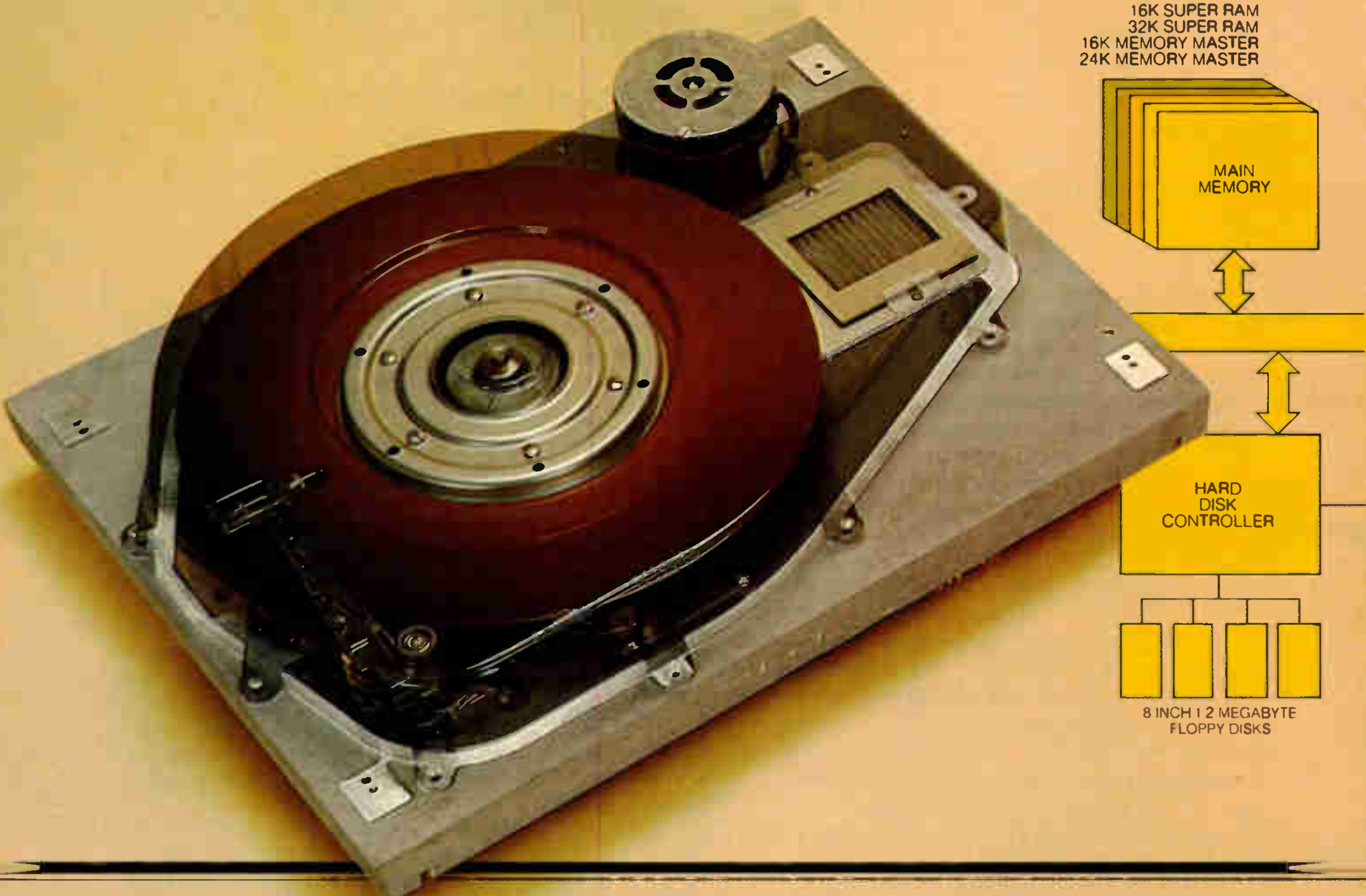


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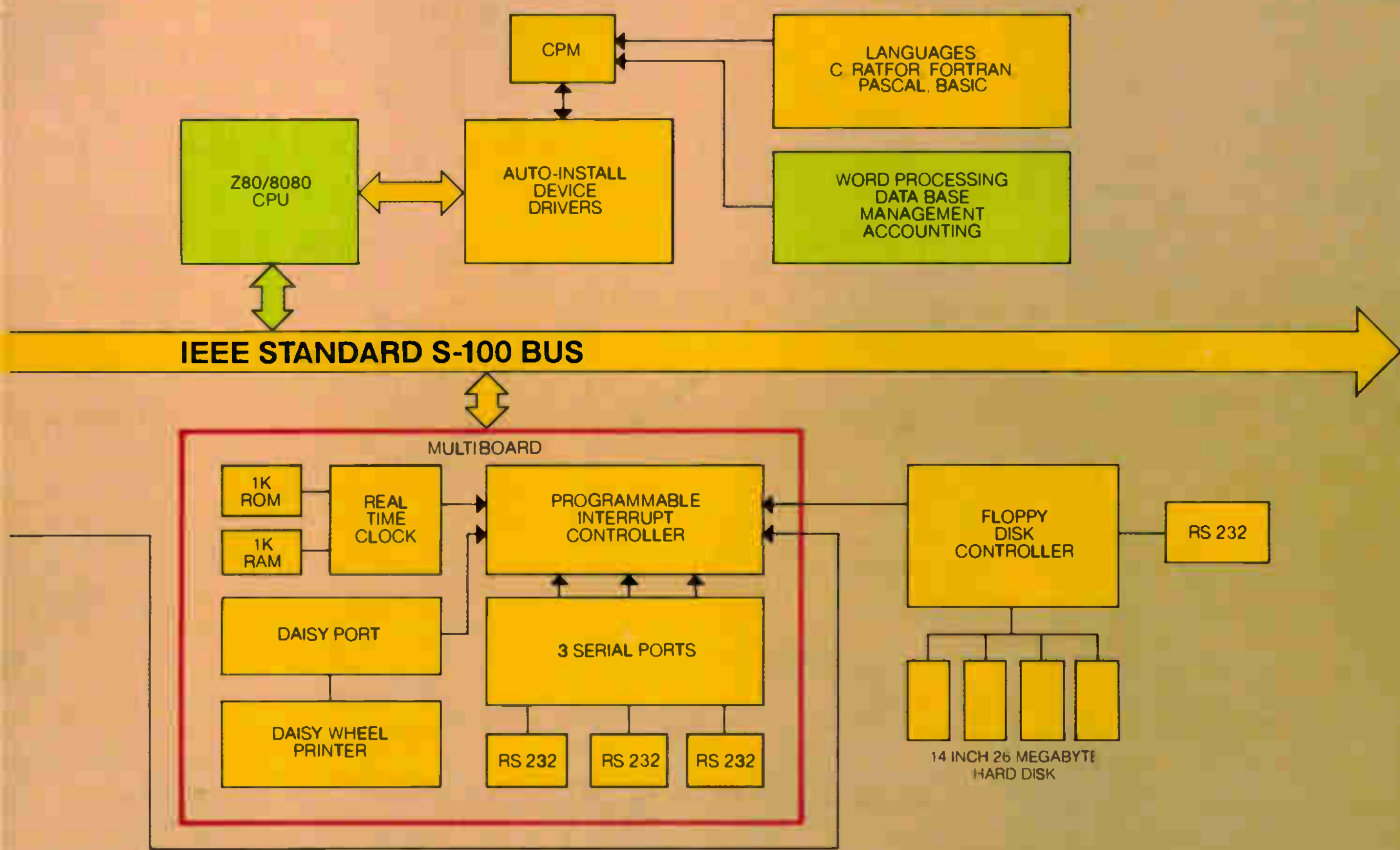


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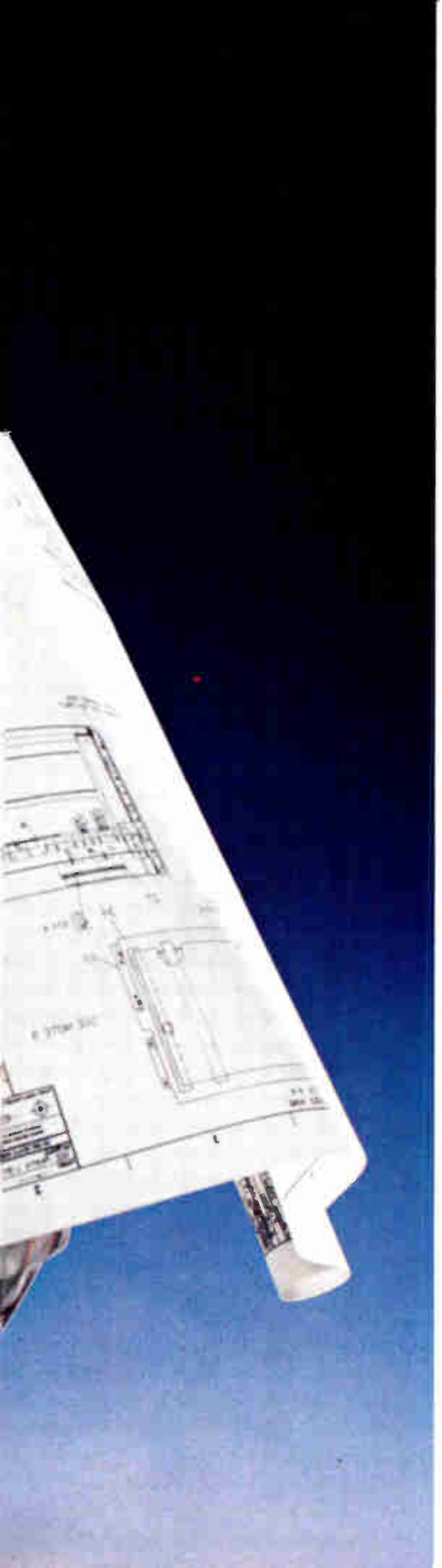

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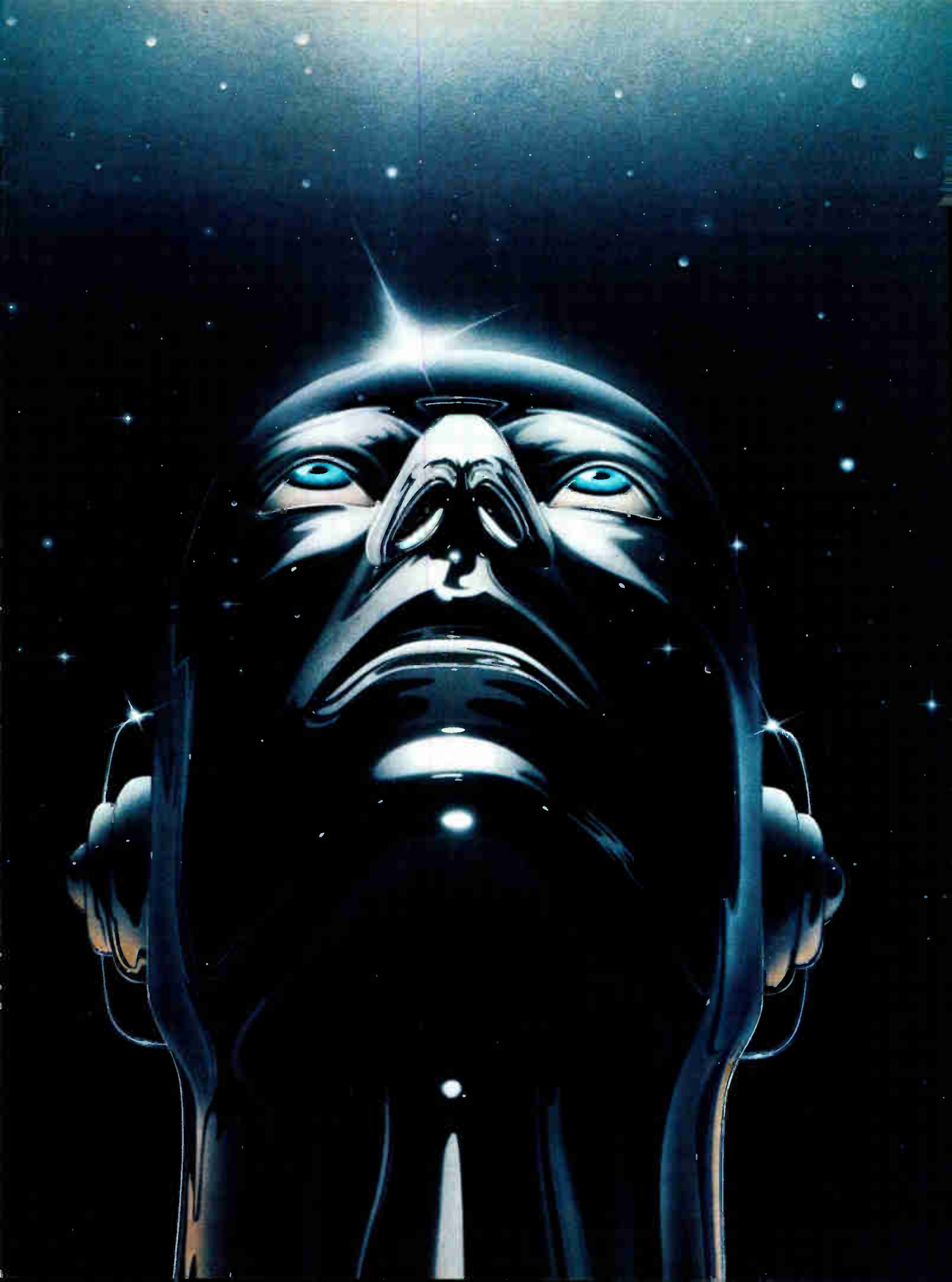

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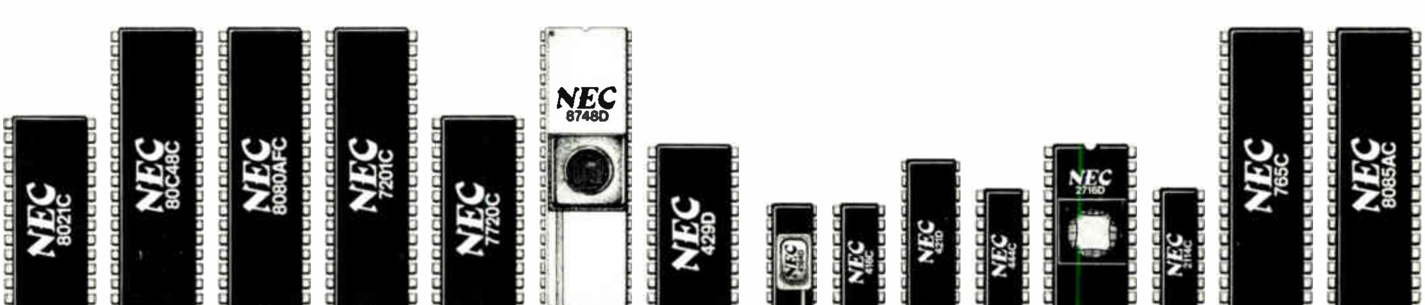



™*Multibus is a trademark of Intel Corporation.

Circle 113 on reader service card

*Companies in the computer and data-communications business have always furnished their customers with proprietary local networks. These networks allow a single vendor's data-generating and -receiving equipment to be hooked together. Thus the benefits of a common data base and the efficient allocation of resources such as printers can be realized. A good local network is, in fact, the heart of an efficient distributed-processing system.*

*As distributed processing has grown into a multibillion dollar industry, the proprietary local network has been found wanting—there are just too many data-processing systems that are incompatible. The trend in the data-communications industry for the 1980s will therefore be to design local networks that will hook up any manufacturer's equipment. Such local networks are only now becoming available.*

*The Net/One local network from the Ungermann-Bass organization in Santa Clara, Calif., is the first to be compatible with the offerings of most manufacturers of data-processing equipment. It is a good example of what can be done with state-of-the-art large-scale integration, clever software, and classic, inexpensive coaxial cable. It is just now starting to be shipped to customers.*

*Local networks such as Net/One are being welcomed by users and manufacturers of distributed data-processing systems because they eliminate problems at every level of the system. For example, they remove from consideration such incompatibilities in equipment as different electrical interfaces, code sets, signaling methods, data rates, and data-base access methods.*

*Of course, there is another way around incompatibility. If the user is willing to design a*

# Local network gives new flexibility to distributed processing

## Bus-architecture, coaxial-cable–based system handles 250 nodes, thousands of incompatible terminals

by Charlie Bass, Joseph S. Kennedy, and John M. Davidson, *Ungermann-Bass Inc., Santa Clara, Calif.*

☐ In the variegated world of computer communications, protocols multiply as the number of equipment vendors grows. Terminals in the accounting department often cannot communicate with those in payroll, a word-processing system in customer service must maintain customer files separate from those maintained in sales, and one mainframe is underutilized while another is overburdened.

Most proprietary local computer networks are dedicated to just one vendor's equipment and therefore cannot solve these problems. The newly available Net/One, however, interfaces with a wide variety of equipment—anything with either the industry-standard RS-232-C serial interface or a TTL-level parallel interface.

Because it reconciles protocols of various devices by means of programmable interfaces, the thousands of devices that may be connected to Net/One—intelligent terminals, data bases, microcomputers, multiuser mainframes, or whatever—can all be made to communicate with each other regardless of their manufacturer. Net/One also supplies a hitherto unattainable control of distributed data-processing resources. Its user can switch terminals between hosts or share expensive peripherals, application programs, and data-base management systems with other users or even gain access to the facilities of a remote Net/One.

### Four building blocks

The packet-switching network is designed specifically for data distribution at high speeds (up to 4 megabits per second) within a single, relatively confined facility, the kind in which studies have found over 60% of all computer communications takes place. A minimal Net/One setup requires only a length of coaxial cable, some passive transceivers, and several model 1 Network Interface Units handling four peripheral devices each. The *custom interconnection network, he can do so. Unfortunately, a significant amount of software and hardware development is necessary. This is complicated, since few LSI devices are designed to deal with local interconnection problems.*

*IBM, Honeywell, Hewlett-Packard, Digital Equipment, Wang, Four Phase, Data General, Datapoint, and others in the data-processing business have made local networks available. However, these offerings are, in general, specific to one brand of equipment, although there are degrees of flexibility.*

*Of course, these companies are not going to be left behind in developing greater flexibility in their networks. IBM, for one, is modifying its centralized, hierarchical System Network Architecture to be more flexible than currently available versions. And Xerox is working hard on its Ethernet system, although it is not yet generally available. Just how flexible these and other systems will be will be known when they become more completely specified. In the meantime, there are still other systems coming out. For example, Zilog has developed a local network dubbed Z-Net that will be the subject of a technical article in an upcoming issue of* Electronics, *and in Britain the Cambridge Ring is attracting the attention of companies there* [Electronics, *Aug. 28, p. 80*].

*The use of local networks in the office lags behind their use in the factory because the need has taken longer to develop. Such organizations as Ford, General Motors, Citibank, and various Government agencies have had local networks for varying lengths of time. None of these, however, uses a general-purpose design like Net/One; all are custom approaches.*

**-Harvey J. Hindin**

model 2 NIU has greater processor capability and can handle more equipment. A Network Development System may be added if the user wants to design his own software, and a Network Administrative Station keeps tabs on the events in a large and complex network.

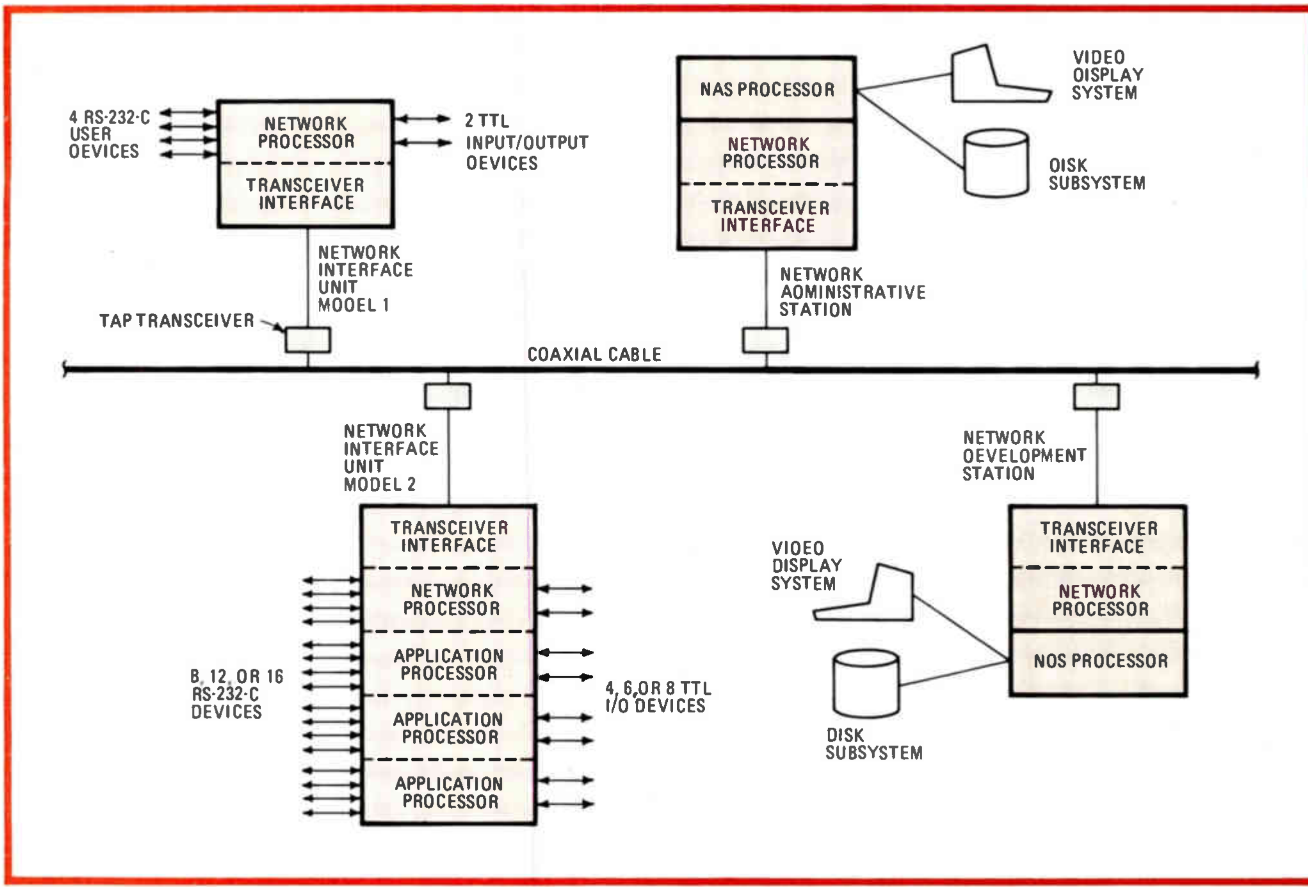
As each of these four types of stand-alone interface unit has its own intelligence, communications between them are controlled not by a central computer but by the network processor in each unit (Fig. 1). Thus only four building blocks can interconnect, customize, and monitor a distributed-processing network of almost any size.

The human engineering of Net/One makes it exceptionally easy to use. The complexities of message and data transfer are handled by preprogrammed microcomputers in each Net/One node. Thus, the Net/One system user never needs to know what it takes to get from point A to point B—he simply indicates the desired destination through simple commands. The NIU takes it from there: formatting the data in packets, handling any speed conversions, and routing the data to the specified destinations. Likewise, for receiving data, the NIU manages all handshaking and the converting of packet data into device-formatted data.

### The link

All the NIUs are connected by means of standard RG-8A/U 50-ohm coaxial cable, which provides high bandwidth, low cost, and easy installation. In fact, it may be possible to use the cable already installed in most new office buildings. Of course, the cable may be installed in an existing facility.

A single such cable segment may be 4,000 feet long. If that is not enough, extra segments may be connected by means of repeaters. Also, requirements for greater geographic coverage can be accommodated by making NIUs serve as gateway stations for linking local networks.




**1. Basic modules.** Depending on the application, four different modules can be combined in various ways to make up a Net/One local network. Up to 250 of the Network Interface Units can be accommodated by one 4,000-foot length of coaxial cable.

Connection to the cable is made through a nondestructive tap with an integral, passive, baseband transceiver. Because the tap is nondestructive, connections can be added to or removed from Net/One without interrupting network operation. Up to 200 taps separated by a minimum of 10 feet may be placed on a single cable segment. The passive nature of the transceiver prevents the network from being affected by an inactive or malfunctioning node.

### A busy interface

The transceiver drives data onto and receives it from the cable at 4 Mb/s using the modified Manchester encoding technique. It also converts the cable's baseband signals into the logic levels required by the NIU, and vice versa. It is connected to the NIU by a nine-conductor cable that may be up to 80 ft long.

The operation of the transceiver itself is controlled by the NIU's transceiver interface, which has the jobs of address recognition, error detection, packet retransmission, and packet framing (Fig. 2). The receiver portion of the interface provides logic for recognizing the NIU address (selected at the time of manufacture), as well as a special broadcast address. It may also be programmed to receive all packets concerned with diagnostics and statistics or performance measurement.

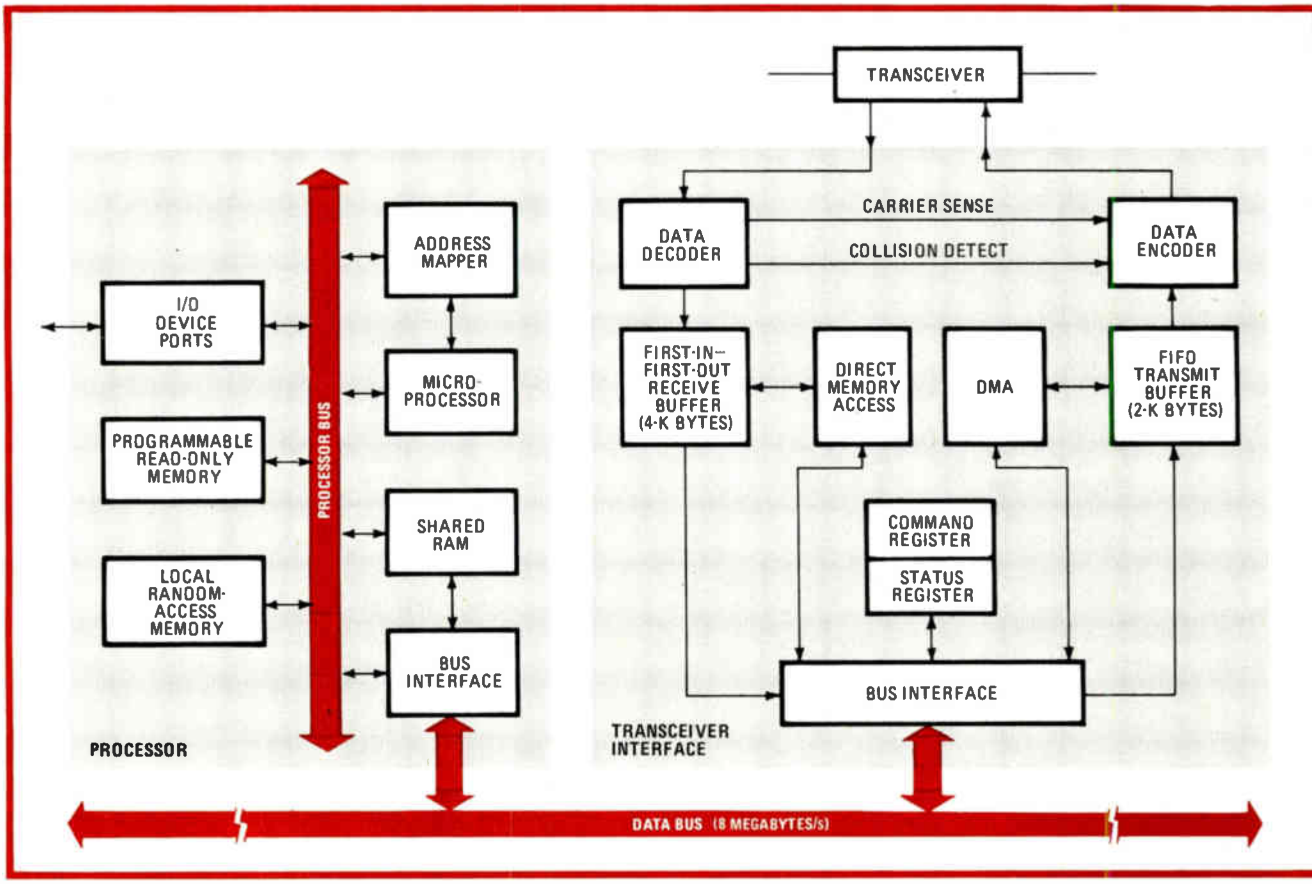
When an appropriately addressed packet is recognized, it is received into 4-K bytes of buffer random-access memory, organized as a first-in–first-out receive queue. When the complete packet has been received, a cyclic redundancy check (CRC) is performed to validate the packet contents. Invalid packets are automatically removed from the FIFO buffer.

Upon reception of a complete valid packet, an interrupt is generated for the NIU's network processor, which may then retrieve the packet through programmed input/output or direct memory access. Typically, the processor first retrieves the packet header and examines it to determine its local destination. The remainder of the packet is then retrieved via direct memory access directly into the memory of the network processor or an application processor.

### Just the opposite

Packet transmission is the converse. Typically, the packet header is built by the NIU network processor and submitted to the 2-K-byte FIFO transmit buffer. The remainder of the packet is submitted directly from a message buffer in the NIU processor or, if appropriate, directly from the memory of an application processor.

As might be expected, actual packet transmission is closely coordinated with receiver information. Before transmission, the receiver examines the state of the network to determine if the line is quiet. Transmission is delayed if network activity is sensed. When the network is available, the transmitter interface encodes the packet and shifts it via the transceiver onto the network. For its part, the receiver continues to monitor the state of the




**2. Two interfaces.** The model 1 Network Interface Unit has a built-in transceiver interface that couples to the passive transceiver tapped into the coaxial cable backbone of the Net/One system. It has one network processor that can connect four data terminals.

network, and if it detects invalid encoding (indicating another NIU's attempt at simultaneous transmission or some other interference), it signals the transmitter that a collision has occurred.

On detection of a collision, the transmitter sends a signal onto the network to notify the other node (or nodes) that such an event has taken place. Each transmitting NIU then computes a variable, randomized time interval and attempts retransmission only after the computed delay period. (Transmission is again delayed if the line is not quiet.) It is this mechanism that allows broadcast use of the transmission medium without the necessity of a central master node. It also provides orderly recovery in the event of simultaneous access to the channel by more than one node.

## Interface control

While the transceiver interface ties the NIU to the network, its network processor provides an intelligent interface to locally attached peripheral equipment. The two elements—transceiver interface and network processor—communicate via a high-speed, 8-bit parallel bus operating at 8 million bytes per second. The model 2 NIU adds one to three application processors to extend the NIU's I/O capabilities or to provide a more powerful, user-programmable interface to locally attached devices.

The network processor operates independently of the other processors on the data bus and can therefore take advantage of future technology without compromising investments in application processor software. Similarly, the design of the transceiver interface will accommodate any transceiver and transmission medium. Thus, fiber-optic and other transmission media may readily be used in place of coaxial cable.

Each NIU executes software that coordinates its activities with other NIUs on the network. Thus, each NIU can participate in a variety of cooperative netwide operations, such as statistics acquisition, fault isolation, and network configuration and access control. In addition, it can execute diagnostics that isolate faults in its operation to the circuit-board level.

NIU power-on diagnostics are invoked at system reset and verify the ability of the NIU to transmit and receive data. Thereafter background-mode diagnostics continue to monitor operation and verify software integrity. More extensive diagnostic information may be gathered by setting the NIU into the test mode. All NIUs in this mode establish communication with each other to implement a distributed diagnostic and network exerciser.

## Controlling the network

The network processor is the heart of the NIU and performs such functions as controlling traffic over virtual circuits to other nodes (see "Making the connection," p. 118), processing commands from local terminals and other devices, and servicing requests from other NIUs on the network. The network processor contains a Z80A microprocessor, 64-K bytes of random-access memory,

## Making the connection

In a local network, connections are made only when they are needed. In Net/One, data traffic is controlled by either a two-way or a one-way connection between two or more devices on the network. The first serves lengthy transfers of data between various devices and is described as a virtual circuit because to the devices, the network appears to be a full-duplex nonswitched dedicated line. The second serves brief messages and is called a datagram. Either of these approaches may be chosen at the discretion of the system operator. His choice will depend primarily on the nature of the message, its length, the number of recipients.

During a data-transfer session, a virtual circuit is established between devices, data is exchanged, and the circuit is disconnected. Throughout, the network activity is transparent, allowing the devices to exchange data in their native code, using their native protocol, totally unaware of the underlying network mechanisms. These devices need not be intelligent terminals or a host computer since no special programming is necessary—the devices communicate in their native mode unaware of the fact that their data is being carried by packets on a local network.

To establish a virtual circuit, one of three procedures may be used. First, a circuit may be set up when the system is designed. This approach ensures, for example, that a circuit will be established between devices without the user's intervention. Alternatively, a circuit may be established by a command from a Network Administrative Station. This method controls access to the network: virtual circuits can be set up only through requests to network administrators.

The third and most flexible way of setting up a circuit is through network commands issued by the terminal operator. The actual syntax of the commands is also configurable by the user, allowing installation flexibility, relative device independence, and a friendly operator interface. For example, the NIU could be configured to recognize SIGNON as "Connect this terminal to host A." If more than one host computer is available, the desired host may be identified within the same message—SIGNON HOST B could be interpreted as "Please connect this terminal to host B."

Which method is chosen to establish a virtual circuit depends on the resources available to the system operator. For example, if the Net/One setup does not have an NAS, the second procedure cannot be used.

All resources within the network may be identified by a user-specified symbolic name rather than by a fixed address. A resource may be any device or service the user wishes to identify to the network—terminals, host computers, printers, disks, application programs, or compilers. Thus, instead of identifying a particular host computer, a user requiring an accounts-payable application program could request it with LOGON ACCTSP. This gives operations personnel the flexibility to move application programs from one host to another (in case one host is "down" or to balance work loads) without affecting the terminal operators.

Net/One resources may also be identified with secondary generic names. For example, a printer subsystem may be primarily known as PRINTER 5, but also identified as PRINTER and 900LPM-PRINTER. Thus a user at a word-processing station may specifically request PRINTER 5, any available printer (PRINTER), a high-speed printer for rough draft printing (300LPM-PRINTER), or any available typewriter-quality printer for final copies (FINAL-COPY-PRINTER).

In contrast to virtual circuits, transaction-oriented data may be exchanged between two host computers or intelligent terminals using a single packet of information—a datagram. In this operation, each packet is individually addressed. Whereas a virtual circuit can be thought of as a telephone connection, where the destination is dialed, a two-way information-exchange session takes place, and both parties hang up, datagrams are more like telegrams. In this approach, an addressed unit of information is sent to the destination in a single, one-way transmission. A response, if required, may be sent with another transmission.

Because datagrams involve little overhead, they are ideally suited to host computers and intelligent terminals needing short information-exchange transactions, rather than a long-term circuit session. For example:

Host A: "To Host B: Find account balance for customer 123456."

Host B: "To Host A: Here is the requested account balance."

Datagrams also allow the user to make maximum use of the multi-access, broadcast technology of Net/One. Flexible packet-addressing modes provide the capabilities necessary for a fully distributed resource-sharing system. For example, datagrams may be addressed to a specific destination:

To Disk Subsystem 2:
Find accounts payable record 11932.

Or they may be broadcast to all devices:

To all nodes:
Report your status.

They can also be broadcast to a specific group of devices at all locations:

To all disk subsystems:
Do you have accounts payable record 11932?

Finally, they can be broadcast to a group of devices at a specific location (on a specific NIU):

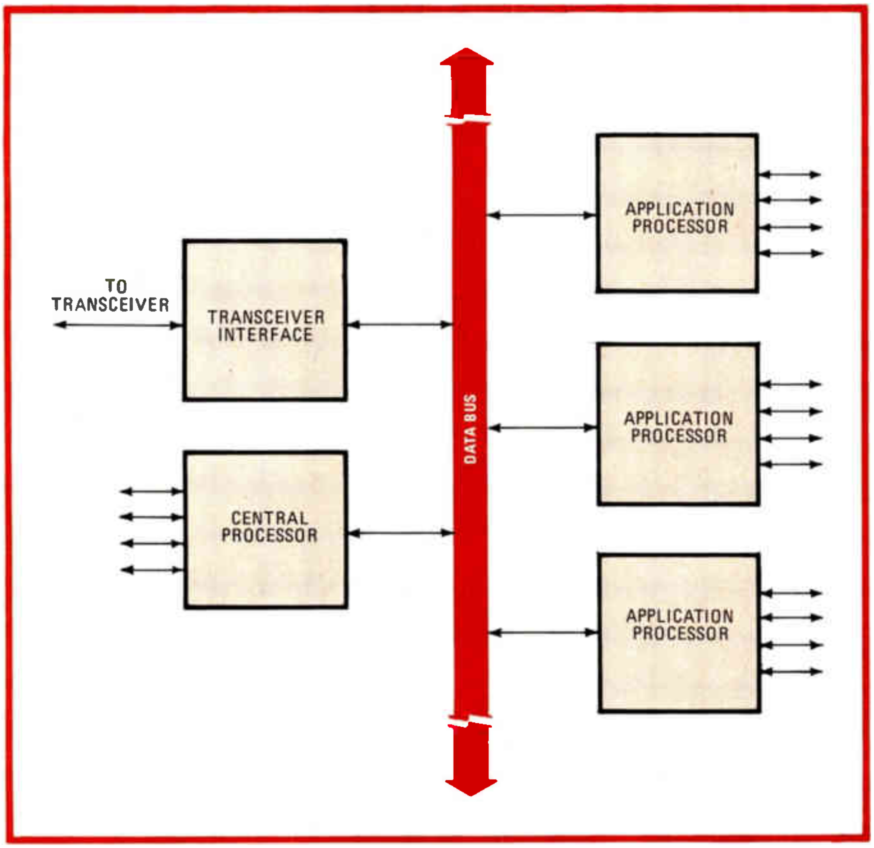
To all disks in accounting:
Do you have accounts payable record 11932?

---

4- to 16-K bytes of programmable read-only memory, memory-mapping logic, two 8-bit parallel I/O ports, and four serial (RS-232-C) I/O ports. All components communicate via an 8-bit bus, internal to the processor and independent of the data-bus link to the transceiver interface (see Fig. 2 again).

By design, 16-K bytes of the 64-K RAM are dual-ported and accessible to the high-speed NIU data bus. This arrangement permits high-speed memory-to-memory transfers and direct access to network processor memory from the transceiver interface or from application processors.

The memory-mapping facility extends the network processor's addressing capabilities to over 1 million bytes. The mapper makes it possible to address both internal memory (PROM, local RAM, and shared RAM) and external shared RAM contained on other processors, giving the network processor the ability to directly




**3. Still better.** The model 2 NIU has up to three applications processors, in addition to the network processor of the model 1. Each of these can interface up to four user terminals with Net/One at a time while handling protocol conversion and complete device management.

address buffer memory in the application processors in its own or another NIU.

The 4,096-byte PROM contains power-on reset diagnostics and bootstrap (initial program load) logic. The PROM controls the processor after a reset condition, which can occur from power-on, from operation of the NIU reset switch, or by command from the Network Administrative Station (via the network). The reset condition clears the memory mapper, executes the power-on reset diagnostics, and causes a broadcast message to be sent requesting "down-line-load" (bootstrapping). When the NIU software has been completely loaded, the 4-K PROM is mapped out of the processor's address space to allow the NIU software full addressability to the 64-K RAM.

The two parallel I/O ports provide the commonly required TTL-level interface for a wide variety of peripheral devices. Each port includes eight input or output data lines with simple strobe/ready handshake lines.

The four serial I/O ports are RS-232-C–compatible, full-duplex interfaces provided to connect the NIU with such interfaces on data terminals, host computers, or (via a modem) remotely located equipment. Each port can be configured to appear either as a modem to terminal equipment or a host computer or as a terminal in order to connect to a modem. Transmission modes may be either asynchronous or synchronous, with data rates of up to 19,200 bits per second. Asynchronous characters may be 5, 6, 7, or 8 bits in length, with 1, 1.5, or 2 stop bits and even, odd, or no parity. The synchronous mode supports one or two sync (flag) characters, CRC-16 binary character checker (BCC) generation and checking, and for bit-oriented protocols, automatic zero insertion and deletion.

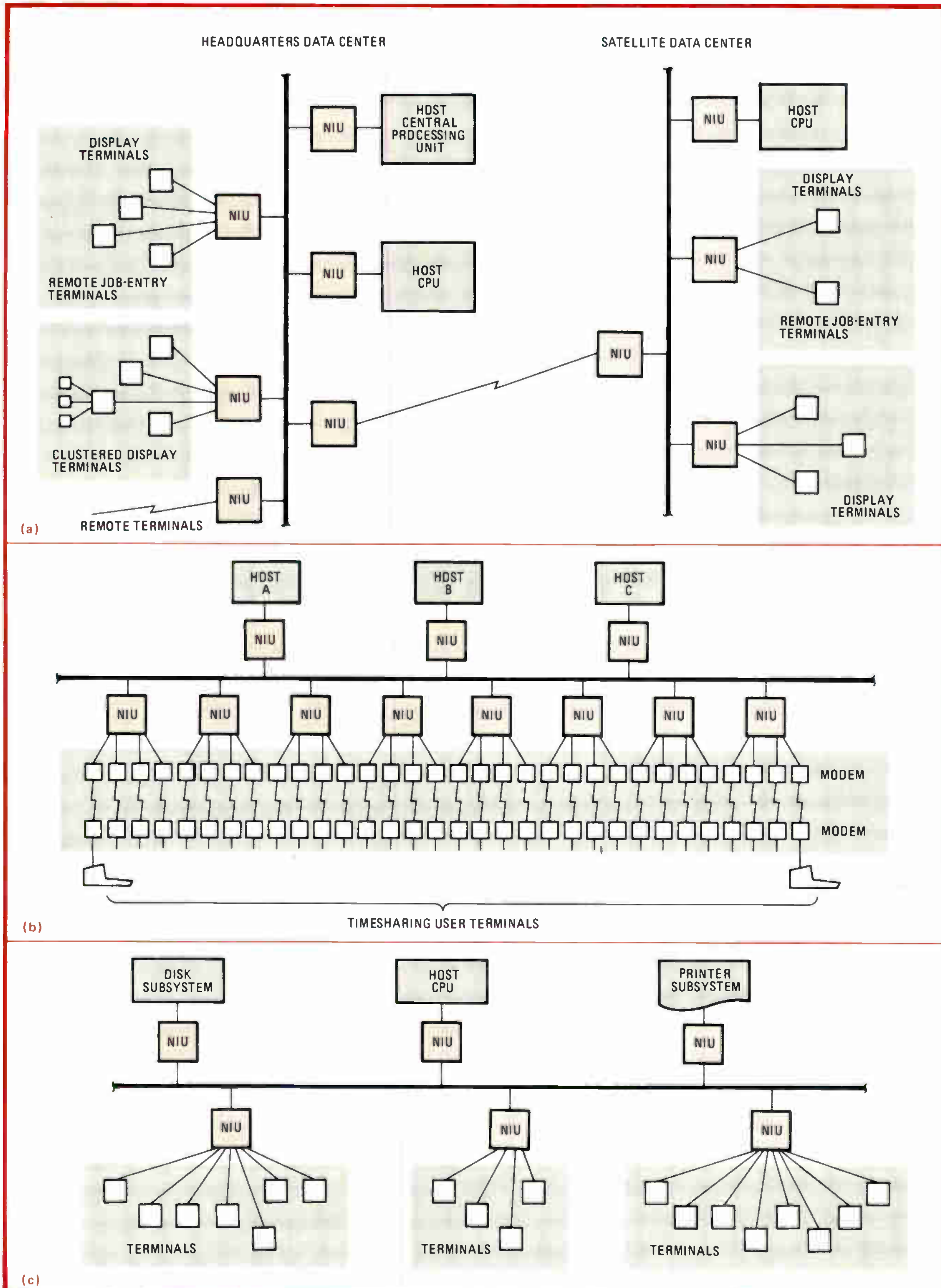
Up to three extra processors may be added to the model 2 NIU, providing a user-programmable interface capable of performing complex device management and data manipulation functions (Fig. 3). For example, such an application processor could be programmed to act as an intelligent controller for a disk subsystem, processing data-base requests from terminals and hosts on the network. Alternatively, being functionally identical with the network processor, an application processor may be added to the NIU simply to obtain four extra serial I/O ports and two extra parallel I/O ports.

In the model 2 NIU, the network processor controls all protocol activity and manages packet traffic, relieving the application processor of this overhead. Network packets are sent and received by direct memory access between the application processor's shared memory and the transceiver interface.

## Developing software

To develop custom application software for the network, the Network Development System provides all the software development tools needed—from editors to structured high-level languages. Application execution is facilitated by a multitasking control program resident in the application processor. Programs may be written in Z80 assembly language or structured high-level languages designed specifically for efficiency in microprocessor applications.

In reality, the NDS is an NIU to which has been added a video display terminal, disk storage, and a computer



HEADQUARTERS DATA CENTER
SATELLITE DATA CENTER
NIU
HOST CENTRAL PROCESSING UNIT
DISPLAY TERMINALS
REMOTE JOB-ENTRY TERMINALS
HOST CPU
CLUSTERED DISPLAY TERMINALS
REMOTE TERMINALS
(a)
HOST A
HOST B
HOST C
MODEM
TIMESHARING USER TERMINALS
(b)
DISK SUBSYSTEM
PRINTER SUBSYSTEM
TERMINALS
(c)

**4. Flexible connections.** There are almost no limitations on how Net/One may be configured. In (a) two separate local loops are linked; in (b) three host computers are linked to 32 timeshared terminals; and in (c) a flexible shared-resource system is illustrated. Both intelligent and dumb terminals may be mixed as desired, since the Network Interface Units are programmable.

system programmed to provide the services of a program development station. Development tools include a disk operating system, a program editor, a macro assembler, and structured high-level languages. Furthermore for ease of use there are a linker/loader (linkage editor), and file utilities.

The NDS also provides the administrative services necessary for program debugging and testing. These include download bootstrap of NIU software, interactive debugging of a remote NIU and diagnostic loading and error reporting. All these tools allow the system management function to be performed with little or no grief.

### Watch the show

Finally, all data transfers between devices on the Net/One network can be monitored through a network operator's console—the Network Administrative Station. Besides having a display keyboard for operator control and a disk for program storage, the Network Administrative Station contains the necessary performance-monitoring and diagnostic software to analyze activity on the network. With the station, for example, the user can monitor how many packets are being transferred per second on the network or who is receiving the messages, or he can trace a network malfunction to a particular NIU and then to the malfunctioning board of that NIU.

The Network Administrative Station also helps establish and modify the network configuration. With it, the user can specify what type of devices are attached to each NIU, what type of data each NIU may handle, and what symbolic name each NIU will be called.

### Finding errors

Inherent in the design of the Net/One distributed architecture are extensive error-detection and -recovery features. As noted, each NIU has carrier-sense multiple-access hardware to prevent it from transmitting data when another NIU is already transmitting. In addition, its collision-detection circuitry immediately detects an attempt at two simultaneous transmissions and the data is retransmitted automatically. Beyond that, the NIU's CRC block check polynomial circuitry detects and recovers garbled transmissions.

All these error-checking procedures apply to both the transmission modes that the Net/One system can furnish. These are the two-way virtual circuit and the one-way datagram (see "Making the connection," p. 118). Using a virtual circuit, any data-generating or -receiving device can communicate directly with any other such device. The virtual circuit is established by software command rather than by physical connection, so that the connection is switchable by the user. It resembles a two-way telephone connection in having all the advantages of simple, point-to-point communications for large-volume, session-oriented data transfers.

With datagrams, transaction-oriented data may be broadcast quickly from one intelligent device to one or more intelligent devices. Like a telegram, the datagram is a one-way transmission containing the message and the destination address. It can be broadcast to one device, to a group of devices, or to all devices on the network. Consequently, it provides the message-transfer techniques necessary for a fully distributed, resource-sharing system.

Whatever the transmission technique used, the effort required to attach a device or a host to the net is variable. A dumb device such as a cathode-ray-tube terminal or a printer can take advantage of a virtual circuit service with no alteration in its normal operation. A more intelligent host, such as a word-processing station, can use the datagram service by simply enclosing its data in an appropriate protocol envelope and handing it to the NIU. But it does need software changes to support this datagram capability, depending on the form of distributed processing that the host wants to participate in. Such changes might be as simple as providing device drivers for the serial and/or parallel ports that interface with the NIU, with packet construction and packet interpretation being provided within application programs.

### Apply the system

A key feature of Net/One is its versatility in making individual connections and the practically unlimited number of different configurations it provides. These configurations handle both dumb and intelligent terminals, since the Network Interface Units are programmable.

Starting with the NIU and the serial or parallel access it provides, a network community can be configured from processors and various I/O devices. For example, by connecting a number of user terminals and a single processor, a conventional multiuser system can be achieved.

The software requirements in this bus topology (see "Choosing a topology," p. 122) are essentially the same as they would be for a multiuser system with a conventional CPU star topology. An existing multiuser operating system could be used without change by attaching each of the host's terminal ports to a distinct NIU port.

By connecting directly to the data bus of the NIU, more complex and sophisticated host equipment interfaces can be achieved. For example, a disk or storage module may be attached to an NIU to provide a shared-peripheral and associated file storage system. Alternatively, an assortment of printers may be attached to an NIU. Combined with the disk facility, files to be printed may be pooled and scheduled for an assortment of printers or other devices. Alternatively, the NIU may provide access by means of a high-level protocol such as X.25 to another processing system.

### Two separate networks

Moreover, the NIU can serve as a gateway between the local environment and another local network or a long-haul network. For example, suppose a manufacturing company has a central data-processing facility with two

## Choosing a network topology

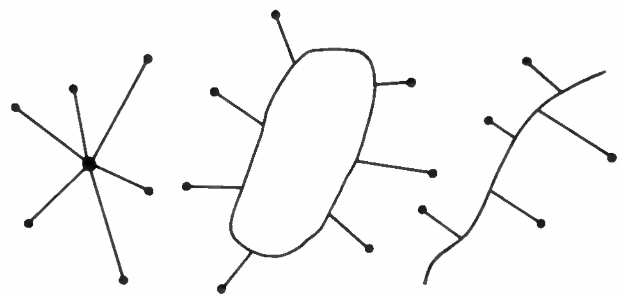
The first decision to make in designing a local network is whether to use a star, ring or bus topology (see figure).

A star arrangement connects each user to a central facility responsible for managing all communications. Both the advantages and disadvantages of this arrangement stem from this centralization. Although communications and resource management can be efficiently handled, the limitations and reliability of the central unit determine all network performance characteristics. In addition, connecting the central host to each individual user is often costly because so much cable is required.

Compared with a star organization, the ring architecture is a simpler and therefore less expensive way of connecting processors and other network elements and also eliminates the central facility bottleneck. But overall network reliability now depends on the reliability of each connection. A break in the ring at any point disables it because messages circulate in only one direction. Consequently, each connection to the network is complex because hardware is required to keep the network functioning even when a node fails.

The bus approach—the architecture of choice for Net/One—has roughly the same topological simplicity as a ring. By using passive connections, it alleviates the reliability issue. In addition, simpler transmission hardware can be used to access the bus. Consequently, this architecture allows the simplest, least costly, and most reliable implementation.

Though the topology selected determines many network issues, it is basically independent of the choice of the transmission medium. Ultimately, local networks will use an assortment of whichever media are technologically appropriate to a given application. They will include optical-fiber as well as coaxial cable and twisted-wire pairs, and eventually cable television, radio, and infrared transmission as they show promise.




large mainframe computers located at its headquarters, plus a satellite data center located at a remote distribution center (Fig. 4a). Each location services a variety of local and remote terminals performing data entry, inquiry, and update functions. A local network at each location interconnects the host computer(s) as well as the various terminals. The two separate networks are connected with gateway nodes via a high-speed leased-line communications channel, thus creating a single network. The separate parts of this network may be thousands of miles apart, depending on the communications channel chosen.

All terminals in such a network have a direct link to any of the host computers; operators can easily access any data base or any application program in the system. For example, the headquarters' accounting department can retrieve a customer's order backlog from the satellite's data base and a satellite order-entry operator can retrieve a customer's credit history from the headquarters' data base. Since the network resources are accessed by name, rather than by physical address, application programs and data can be moved freely from one host computer to another or even from one location to another. Host computers that are down and resource shuffling resulting from production loads have no effect on the terminal operators.

### Share the system

Direct computation needs are also readily served. Suppose a timesharing company has several large mainframe computers servicing a mix of leased-line and dial-in users. Net/One provides a high-speed link interconnecting the host computers and services all of the incoming lines. Each incoming line is serviced by a model 2 NIU that includes one application processor (Fig. 4b). When a call comes in, the NIU answers it, establishing the physical connection to the network. The application processor is programmed to ask the terminal operator what kind of service is desired (Fortran, Cobol, or a user application program).

Once that is determined, the application processor might broadcast a message to all of the hosts requesting the desired service. Any host capable of providing the service is programmed to send an acknowledging response, including in the response an estimate of the performance to be expected from it in light of its job backlog and similar factors. The application processor chooses the best available host and then establishes a virtual circuit between it and the dial-in terminal.

This dynamic balancing of incoming traffic ensures optimum response for the company's users. At the same time it allows the movement of resources from one host to another with no disruption in service. The local link of course can handle a wide variety of terminal equipment of the kind a university or factory might acquire over a period of many years. The terminals operate with various speeds, line protocols, and character codes. Net/One provides a common base of compatibility so that the terminals may communicate with each other, as well as with the facility's host computer (Fig. 4c).

Students and instructors or supervisors make use of Net/One's compatibility base and full connectivity to exchange messages, class schedules, notices, and data, as well as to access the host for word processing, program editing, and so on. Instructors make use of virtual circuit sessions to advise students and to provide individual tutoring. Supervisors file reports, modify processes, and check the progress of operating processes as required. □

*Because of the extremely low power consumption of complementary-MOS random-access memories, they have been adopted for many battery-operated applications, including remote data collection, hand-held calculators, and backup memory for computer-system power failures. However, the total low-power system requires additional hardware and software to ensure, for example, that the information stored during power-down is returned to the locations from which it was taken. But casting all the components in C-MOS would greatly simplify the design of such low-power systems.*

*A complete low-power microcomputer system can be built from two C-MOS integrated circuits: the MC146805E2 microprocessor, described in the article below, and the MCM66516 read-only memory, detailed in the article following. Both chips are fully static devices and operate at frequencies of from 1 megahertz down to dc. What's more, their designs stave off the usual manufacturing problems of large-die C-MOS chips, borrowing heavily from dynamic n-MOS circuit techniques.*

*This minimum system uses a multiplexed address and data bus whose lines can drive one TTL load and 130 picofarads of capacitance. It dissipates 45 milliwatts while running at full speed (1 MHz at 5 volts) and a mere 100 microwatts in a special standby mode.* **-R. Colin Johnson**

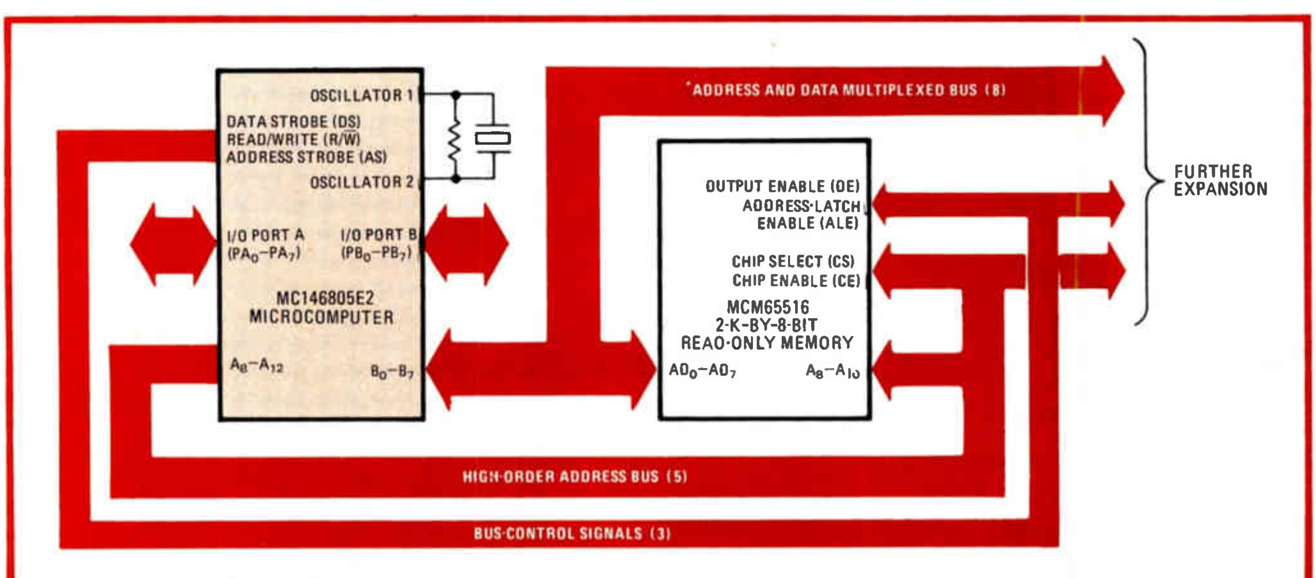
# C-MOS microprocessor wakes itself up

## Special instructions shut down processor, timer awakens it; on-board RAM permits complete system in two chips

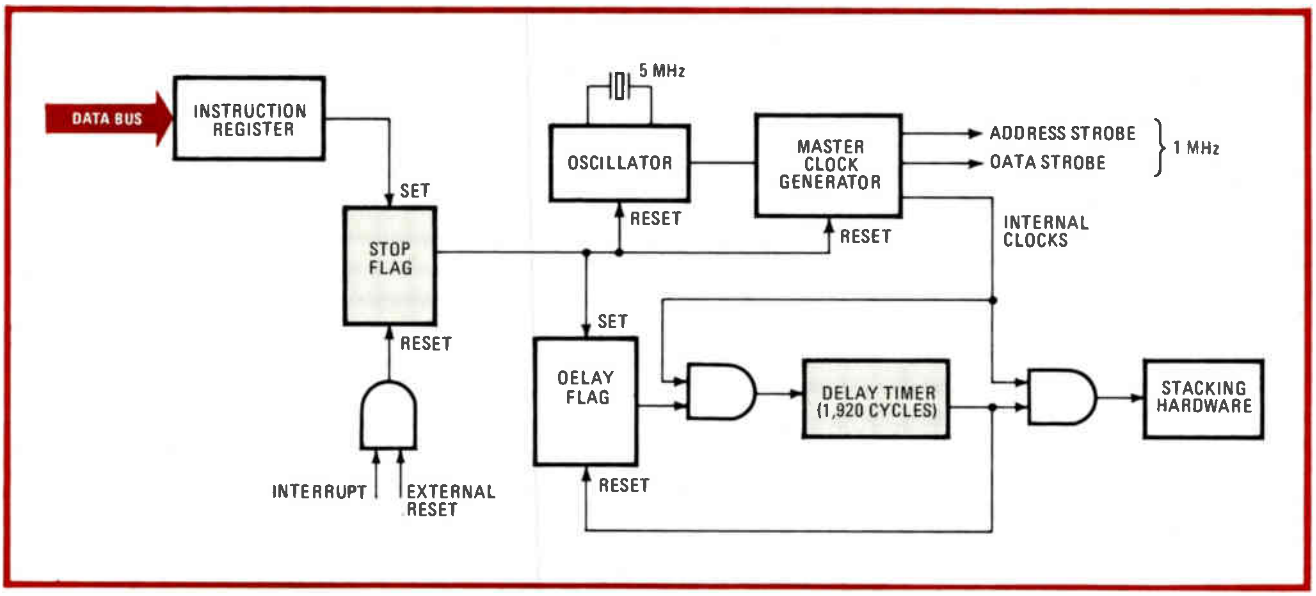
by Philip Smith, K. Raghunatan, and Jerry Hewell, *Motorola Semiconductor Products Inc., Austin, Texas*

☐ The 146805E2 microprocessor improves on the usual n-channel MOS processor designs by including features like an oscillator, the ability to recognize pulsed interrupts, a timer that can stimulate a vectored interrupt, 16 bidirectional input/output lines, and 112 bytes of random-access memory. But more important, the part is C-MOS and makes the most of it, adding, for example, an orderly power-up and -down sequence and special instructions. Running at full speed (1 megahertz), the 146805E2 dissipates only 20 milliwatts; but even this low figure can be reduced to the microwatt range by two instructions—a boon to battery life in mobile systems.

The wait instruction sets the microprocessor in a mode that shuts down unnecessary internal and external processor signals and has it await an interrupt from the internal timer or the external world. The oscillator continues to function while the microprocessor's state is preserved, all registers and on-board memory retain




**1. Two-chip C-MOS system.** This minimum yet complete system stores programs in the 65516 read-only memory, data in the 146805E2 microprocessor's on-chip random-access memory. The system can be expanded as necessary for more complex configurations.




**2. Stop the system.** Whenever a stop instruction is loaded into the instruction register, the 146805E2's oscillator and clock generator are shut down. Then, when a reset or interrupt occurs, the delay timer counts down before it enables the service vector to be fetched.

data, and ports maintain their I/O configuration and continue to provide output drive, but power dissipation drops some 85%. The processor draws 3 milliwatts.

As with any C-MOS chip, the least amount of power is dissipated while in the quiescent state. To achieve quiescent operation, a stop instruction is provided. In this mode, all internal switching functions, including the oscillator, are shut down; as a result, the processor consumes a meager 50 $\mu$W. As in the wait mode, drive remains at the I/O ports and data is retained in memory.

## Stopping the processor

Figure 2 shows the implementation of a stop instruction inside the microprocessor. Once the corresponding operation code has been loaded into the instruction register, the stop flag is set and the interrupt mask cleared. To allow an orderly stop, the processor waits till the end of the next valid-data strobe to shut down both the oscillator and the master clock generator.

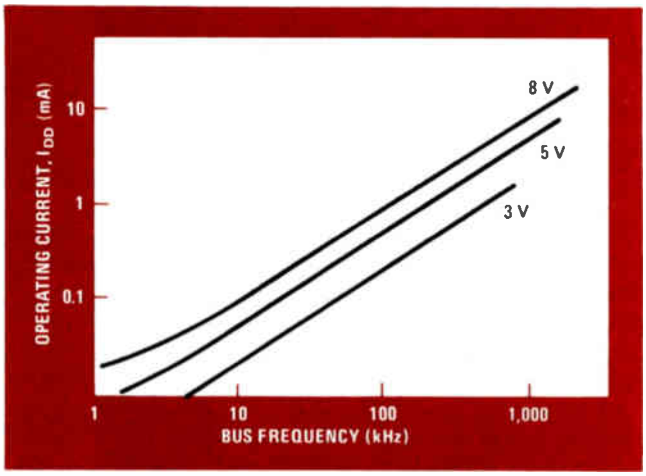
The processor will remain indefinitely in the stop mode pending the reception of an external reset or interrupt to retrigger operation. When either of these signals is detected, the stop flag is cleared, enabling the oscillator to start up and initializing the 1,920-cycle delay counter. The delay allows all signals to settle before processing resumes.

The delay counter is also activated whenever power is applied to the chip. This amounts to a power-on reset delay of about 2 milliseconds (with a 1-megahertz clock). If a longer delay is needed for some external device, the reset pin should be held low to extend it.

## Trading off

As with other C-MOS chips, power-supply current can be traded off for operating speed (Fig. 3), a prime consideration in hand-held applications. Of course, since the processor is fully static and can be operated at any switching frequency from 0 to 1 MHz, a much wider choice of speed versus supply current and voltage exists when compared with processors cast in other technologies. The table compares the 146805 with its n-channel MOS counterpart, the 6805 microcomputer.

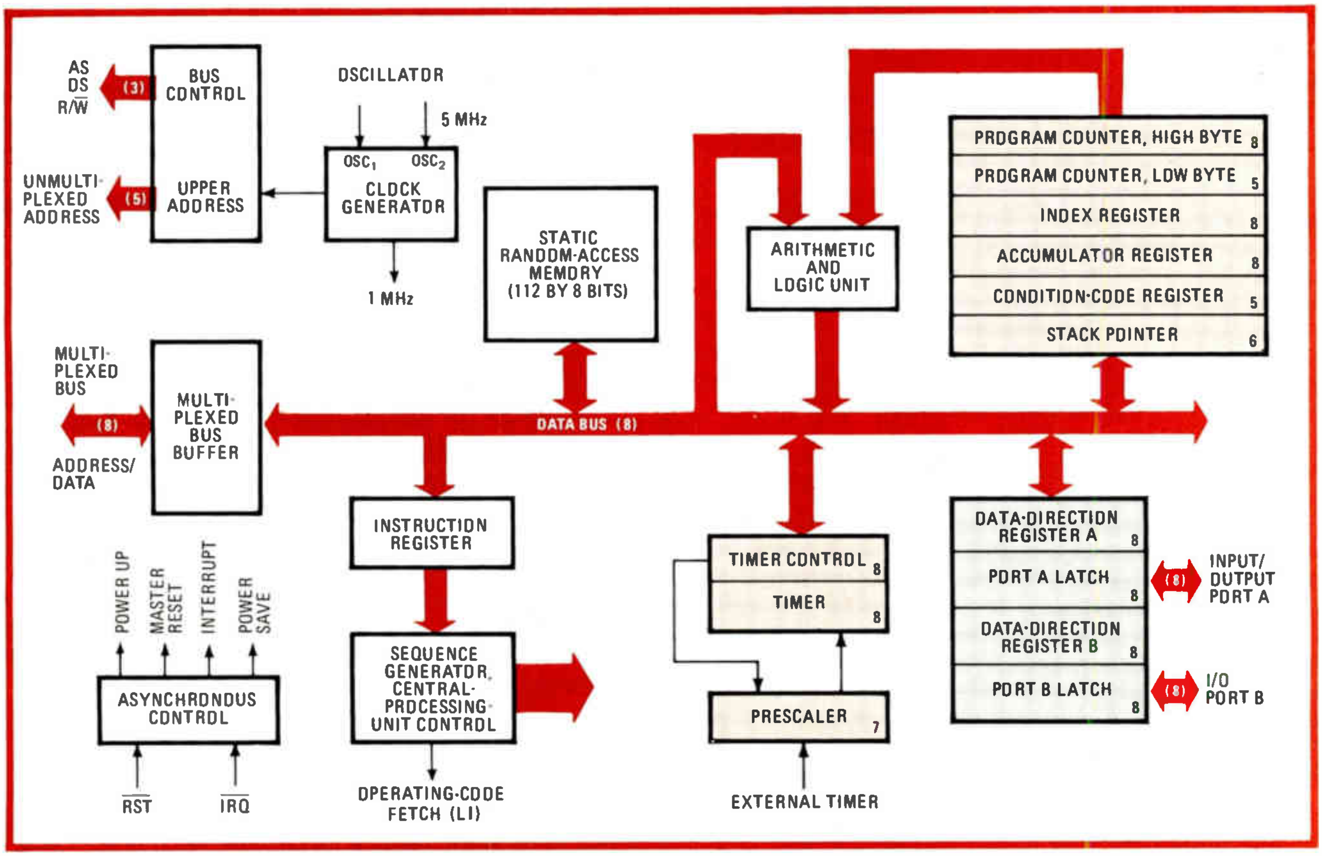
The architecture of the 146805E2 is similar to that of




**3. Power considerations.** A wide range of voltage, current, and operating-frequency combinations are possible with the 146805E2. These can be optimized for long battery life in portable systems, high speed in time-critical situations, or any tradeoff in between.

THE HMOS-C-MOS TRADEOFFS

| | MC6805 HMOS | MC146805 complementary-MOS |
|---|---|---|
| Power dissipation | 300 – 500 mW | 0.5 – 50 mW |
| Standby power | no standby mode | 0.1 – 5 mW |
| Voltage range | 4.75 – 5.75 V dc | 3.0 – 8.0 V dc |
| Cycle range | 100 kHz – 1 MHz | 0 Hz – 1 MHz |
| Cycles/instruction | 5.36, average | 4.02, average |
| Noise immunity | good | better |
| Price | lower | low |




**4. Architecture.** The 146805E2's register file holds the program counter, accumulator, index register, and stack pointer. Other features include on-chip RAM, a timer with prescaler, 16 latched I/O lines, and an instruction-fetch pin for single-step operation.

the 6800 microprocessor, with the addition of some specialized memory-mapped registers (Fig. 4). These registers load, read, and control the I/O ports and the on-chip timer.

It includes two general-purpose 8-bit registers (an accumulator and an index register, ACC and IXR, respectively); a program counter using separate high and low bytes (PCH and PCL); a 6-bit hardware stack pointer (SP) to facilitate nested subroutines and interrupts; and a 5-bit condition-code register (CCR) to reflect the state of the processor.

An on-chip timer has become a standard feature of mid- to low-range microcomputers. The 146805E2 timer consists of an 8-bit down counter whose clock frequency is controlled by a 7-bit software-selectable prescaler, which in turn is driven either from an external time base or from the on-board 1-MHz source. Four software-programmable modes allow for internal timing, external event counting, pulse-width measurement, and timer freezing. Management of the timer system is done through the timer-control register.

### Keeping time

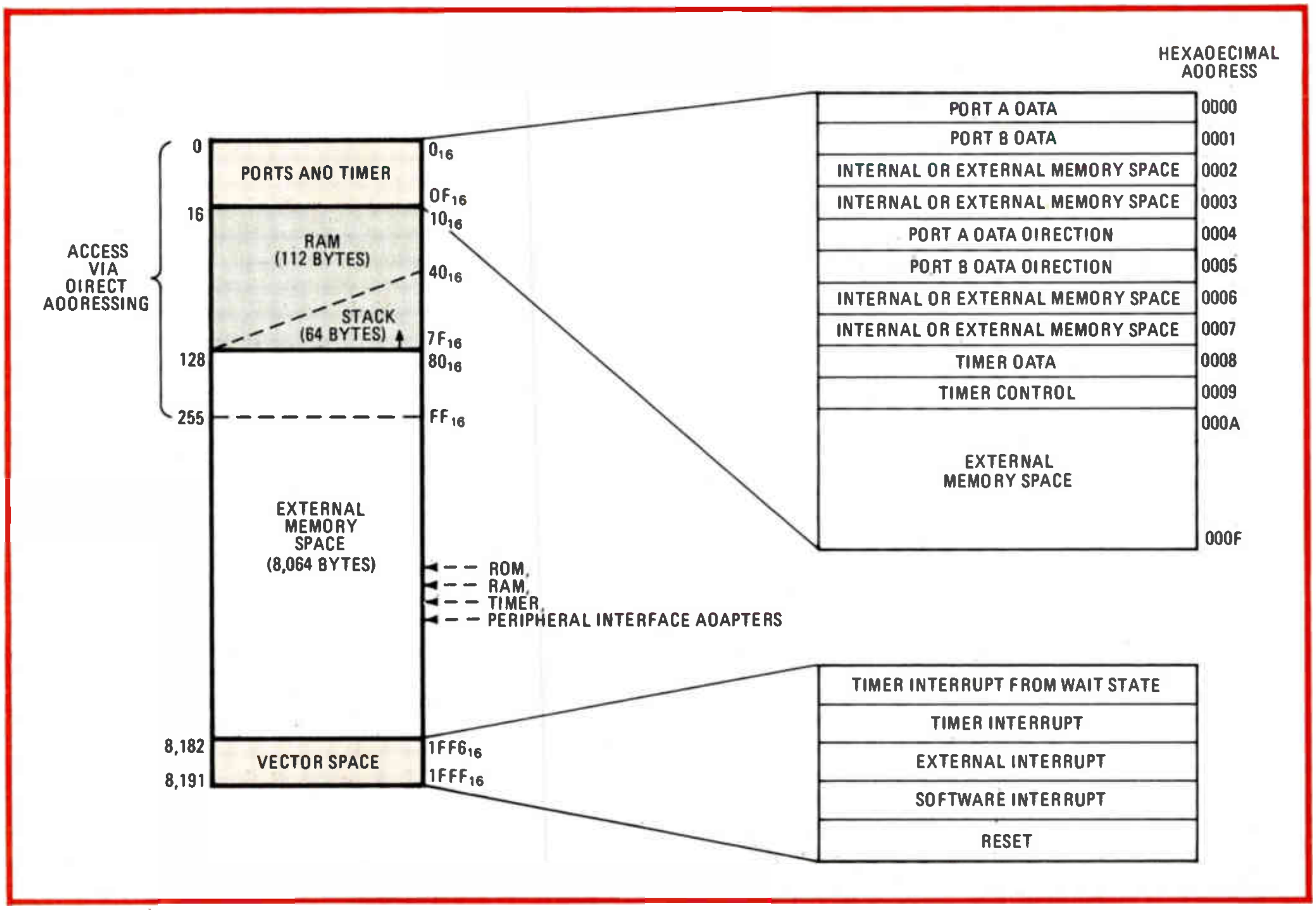
The counter may be read at any time by the processor without disturbing the count. Whenever the counter reaches zero, a timer interrupt will occur if the timer mask and processor mask bits are clear. The timer continues to count past zero, allowing the software to determine the number of clocks since the timer interrupt flag was set.

I/O ports A and B are 8-bit memory-mapped registers, both of which may be read out of or written into by the processor. The data-direction registers (DDRs) let the user define the individual port pins as either input or output. Selecting a bit as an output allows the value of the corresponding bit in the port latch to appear on the external pin. A reading of an output bit obtains its value from the port latch; a reading of an input bit, from the external pin. During power-on reset or external reset, all port pins are configured as inputs.

### Addressing and instructions

The 13 address bits allow users a total memory space of 8,192 bytes, which is segmented into several different functional areas, (Fig. 5). The 10 highest memory locations are reserved for the five interrupt vectors (2 bytes for each: reset, software interrupt, hardware interrupt, timer interrupt, and wait interrupt). The lowest 16 locations correspond to the two memory-mapped I/O ports, the timer register, and their associated control registers (the unused locations may be treated as external memory, as indicated in the figure). Of the remaining 240 bytes of directly addressable memory, 112 are internal RAM (of which 64 may be used as the stack) and the final 128 are addressed as external memory.

It must be noted that the internal memory area is dual-mapped. Any information written into an internally mapped location is reflected externally; a read issued by the processor will access only the internal memory area, ignoring any external data at the pins.




**5. Address map.** The total memory space of 8,192 bytes includes the ports and control registers in the lower 16 locations. Above these is the on-chip RAM, 64 bytes of which can be used for stacking. The top of the space holds the five interrupt vectors.

The 146805E2 has 61 basic instructions of from 1 to 3 bytes in length and utilizing 11 address modes, with an average execution time of four machine cycles. They are very similar to the 6800's and should be easily learned by programmers already familiar with that device.

A welcome feature not found on the 6800 is bit-manipulation instructions that let the user set, clear, and test each bit of the first 256 bytes of memory. The instruction specifies both the bit position and its set or clear function, and the next byte defines the memory location. The test-and-branch instructions allow a program to test the state of any bit and branch relative to the offset contained in the third byte. Simultaneously, the tested bit is loaded into the C flag of the condition-code register.

A unique feature of the processor's interrupt logic is that it recognizes either levels or pulses on the interrupt-request line. It is capable of responding to three different kinds of interrupts as well—one software instruction (SWI) and two hardware (external and timer). When any interrupt occurs and the mask is clear, normal processing is suspended at the end of the current instruction execution, and the contents of the program counter, index register, accumulator, and condition-code register are pushed onto the stack. The appropriate interrupt vector is then fetched and loaded into the program counter.

The 146805E2 is fabricated using a 5-micrometer channel, shallow-diffusion, silicon-gate C-MOS process. It requires only a single level of polysilicon and benefits from the use of dual-polarity buried contacts.

A chip size of approximately 41,000 square mils is achieved partly by using a purely n-MOS memory cell that employs undoped polysilicon resistors for static operation. A saving of 60% in area is gained over the conventional six-transistor C-MOS cell.

## Debugging and development

A versatile software debugging feature has been implemented by providing an op-code fetch pin (LI) and a unique op code ($88_{16}$) that allows easy single-stepping.

In addition, a development system package, the MEX146805, is available to help designers build a system around the processor. It consists of an EXORciser-compatible plug-in control module, a microprocessor module, an operating system, and an interconnecting cable. The software supplied with the package provides over 40 debugging commands, like breakpoint and trace.

Two of the support chips that are planned are the MC146818, which contains a real-time clock capable of producing a programmable interrupt signal, 50 bytes of RAM, and a 2-hertz-to-32-kilohertz square-wave generator; and a C-MOS peripheral interface adapter, the MC146823, which will provide three software-programmable ports with handshaking. In addition, a complete microcomputer, the MC146805G2, will add two I/O ports and 2-K bytes of ROM. □

# C-MOS read-only memory mates with a host of processors

16-K part connects directly to processors whether read request is active high or low

by Bill Donoghue, *Motorola Semiconductor Products Inc., Austin, Texas*

☐ The read-only memory is a cost-effective method of permanent program storage. When cast in complementary-MOS, the advantages of low power dissipation are made available as well. The MCM65516 is a 2-K-by-8-bit ROM that can be combined with a C-MOS microprocessor (like the MC146805E2 discussed in the preceding article) to form a complete microsystem that is ideal for battery powered applications and was shown on page 123.

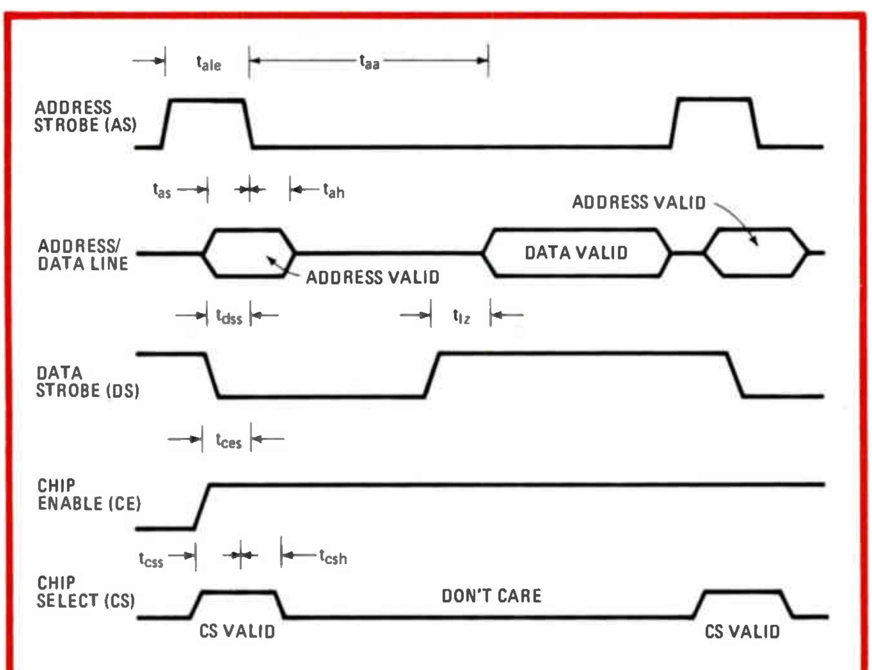
The 65516 has several unusual characteristics, one of which is its multiplexed operation. Since the address and data lines are shared, the package size is reduced from the standard 24 pins used for n-channel MOS ROMs to 18 pins. The savings in size and bus lines allows much greater board densities—which is desirable for hand-carried systems.

## Motel mode

A unique feature allows the part to work with microprocessors from different manufacturers. The problem in achieving compatibility is that some manufacturers indicate a valid read cycle with an active-low read-request signal and some use one that is active high. The 65516 operates with either signal, using a mask-programmable feature called the Motel mode that works as follows. Since the address and data lines are multiplexed, an address strobe (AS) must be supplied to latch the address into an internal register on the chip (Fig. 1). This strobe also latches the state of the read-request signal (here called the data strobe, DS), thereby memorizing its state. The outputs are then enabled when the data strobe changes state. In this manner, the data-strobe input works with either polarity signal as long as the signal toggles during the read cycle. If the data strobe remains either high or low (in other words, does not toggle), the outputs remain off.

Thus, in the Motel mode, this memory is compatible with many microprocessors from different manufacturers. Use with the Motorola 146805E2 was illustrated on page 123; Fig. 2 illustrates how it can be used with National Semiconductor Corp.'s NSC800.

The data-strobe line has two other operating modes. These are the standard static select modes (either high or low), where a dc level not synchronous with the




**1. Timing.** The address strobe latches the valid address into the on-chip address registers. Since the data strobe must toggle after the falling edge of the address strobe to enable the output buffers, the 65516 can accept an active-low or -high strobe.

| TYPICAL TIMING REQUIREMENTS FOR THE MCM65516 READ-ONLY MEMORY | |
|---|---|
| Parameter | Typical value |
| Address-strobe pulse, $t_{ale}$ | 70 ns |
| Access time, $t_{aa}$ | 280 ns |
| Address-setup time, $t_{as}$ | 10 ns |
| Address-hold time, $t_{ah}$ | 10 ns |
| Data-strobe on time, $t_{lz}$ | 85 ns |
| Note: Tests performed at $V_{CC}$ = 5 V, $V_{IH}/V_{IL}$ = 2.4 V/0.8 V, and load capacitance $C_L$ = 60 pF. | |

address strobe turns the outputs on or off.

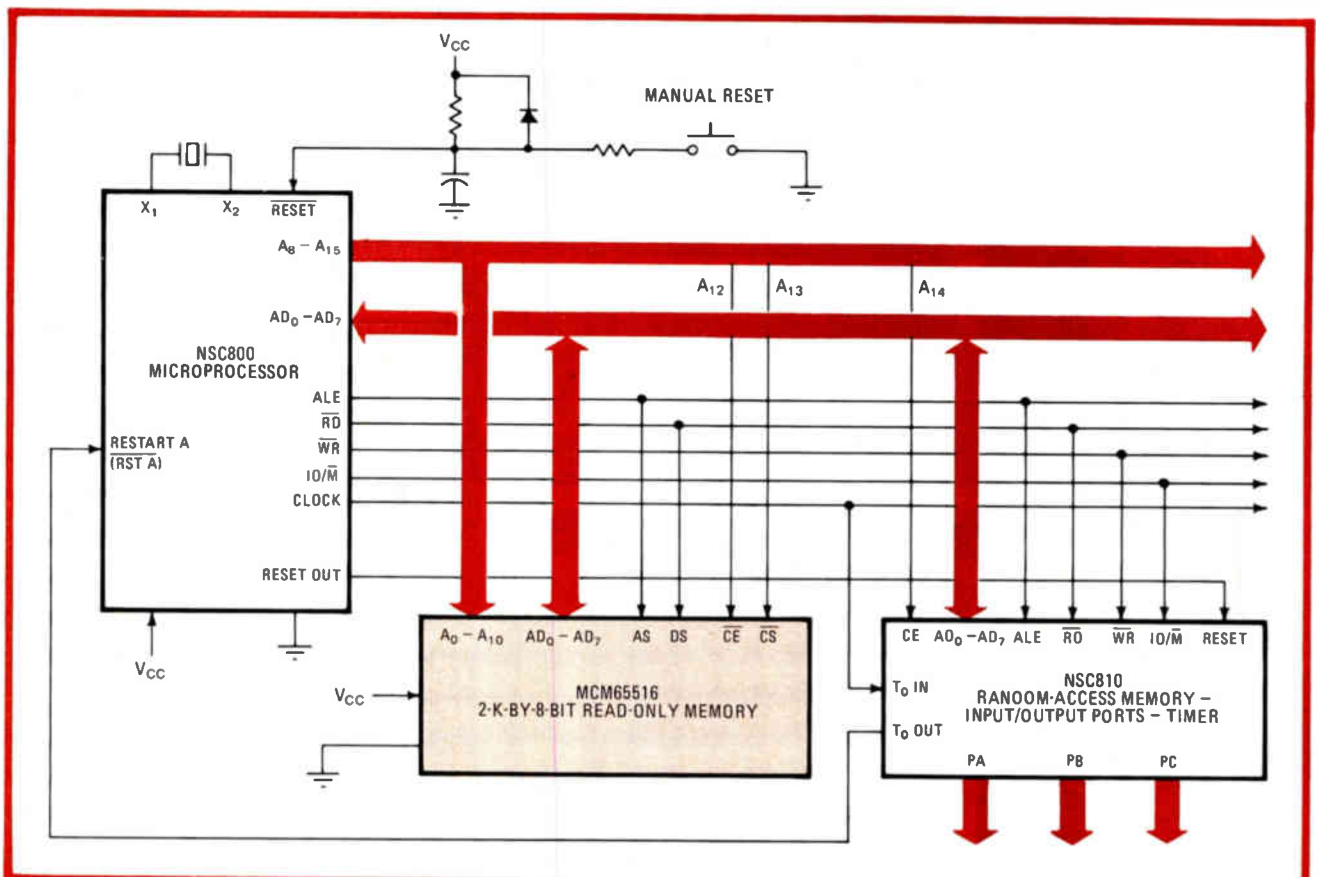
The chip-enable and chip-select inputs are mask-programmable to be active high or low. The chip select acts as an additional address bit and is latched on the trailing edge of the address strobe. When the chip is not selected, its output drivers are disabled (in a high-impedance state). The chip-enable inputs put the chip into a standby mode that saves substantial power. However, they are not latched by the address strobe and must remain stable throughout the read cycle.

The table summarizes timing requirements for the 65516. The address strobe has a minimum pulse-width requirement, since the circuit is internally precharging during this pulse and is set up for the next cycle only on the trailing edge of that signal. Access time is measured from the negative edge of the address strobe; a typical value is 280 nanoseconds.

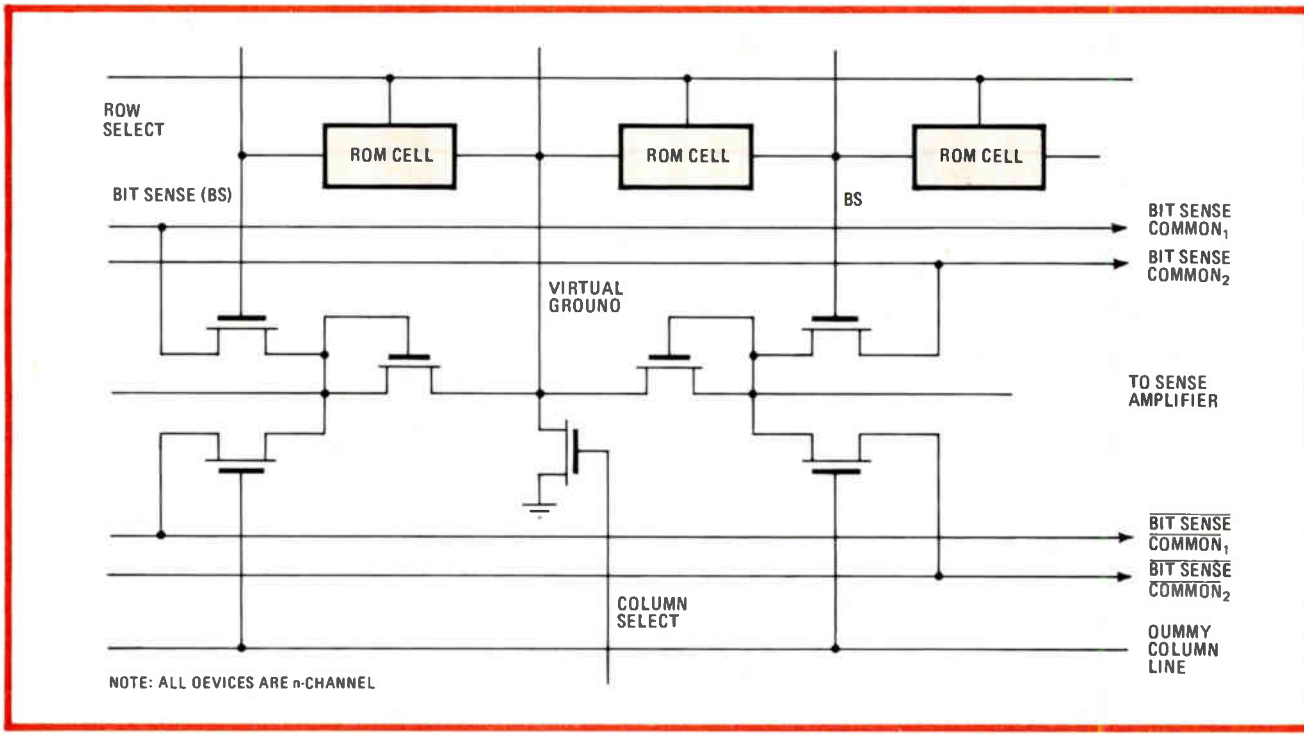
### Virtual grounds

This part is built using a silicon-gate C-MOS process that has been simplified for ROMs. It requires 10 mask steps and uses self-aligned guard bands. Designed to dissipate 600 microwatts when active and 15 $\mu$W in standby (with a 3-volt supply and operating at a rate of 100 kilohertz), it achieves those goals by a virtual-ground approach that offers a smaller cell size than a standard grounded array. With this approach, only eight lines are decoded and discharged during a read cycle (Fig. 3), whereas in a standard configuration all ground lines to the array are discharged. The lines not selected remain precharged to $V_{dd}$, saving power during reads.

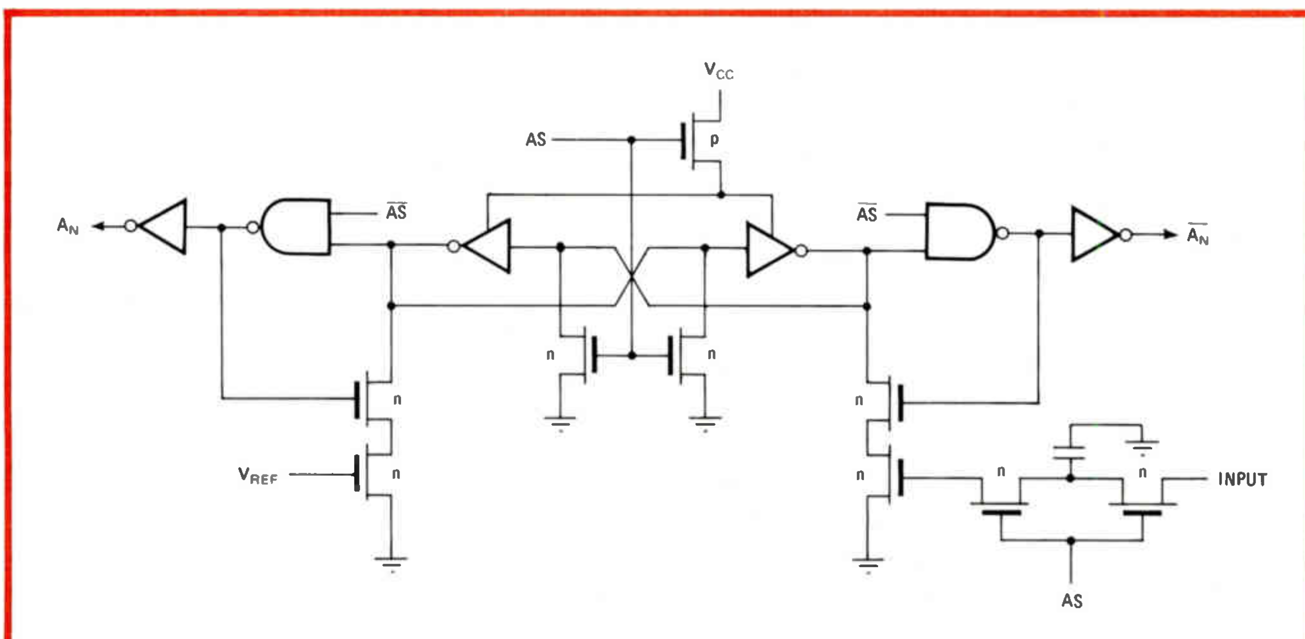
This circuit also limits the amount of voltage discharge on the selected bit-sense lines. Sensing is initiated by a clock signal that occurs whenever the bit-sense lines have discharged by approximately 15% of $V_{dd}$. When this signal is detected, the data from the cell is latched into the sense amplifier and the circuit is put back into the precharging mode. That action prevents the complete




**2. Impartial.** The 65516 ROM may also be used with National's NSC800 microprocessor—even though the data strobe from that part is active low—thanks to the Motel operating mode. Also shown is the NSC810, a combination RAM, I/O, and timer chip.




**3. Virtual-ground operation.** Because only eight select lines are activated during a read (rather than all of them, as with conventional circuits), power is saved during active cycles. Another virtue of the virtual-ground approach is that it results in a smaller cell size.




**4. Address-select logic.** The design used here for the 65516 is more like that for n-MOS dynamic RAMs than for the standard C-MOS ratioed-inverter inputs. It offers shorter propagation delays, no static current paths, and higher yields with process variations.

discharge of the bit-sense lines, returning the circuit to standby for a portion of the cycle, both to save power and to speed up the cycle time (by shortening the address-strobe period).

The address- and chip-select input buffers (Fig. 4) are similar to the address inputs used in n-channel dynamic RAMs and are designed to provide lower power for TTL-level inputs than the standard C-MOS ratioed-inverter inputs.

In addition, the address- or chip-select input buffers act as a latch that is triggered by the address strobe. These buffers have no static current paths and minimal propagation delays and short address-setup and -hold times. The input levels to the circuits are compared with a reference voltage level of 1.4 V (at $V_{dd}$ = 5 V). The reference voltage level tracks the supply voltage and device threshold voltage; therefore the part has stable input levels over process variations. □

## Divider sets tuning limits of C-MOS oscillator

by Henno Normet
*Diversified Electronics Inc., Leesburg, Fla.*

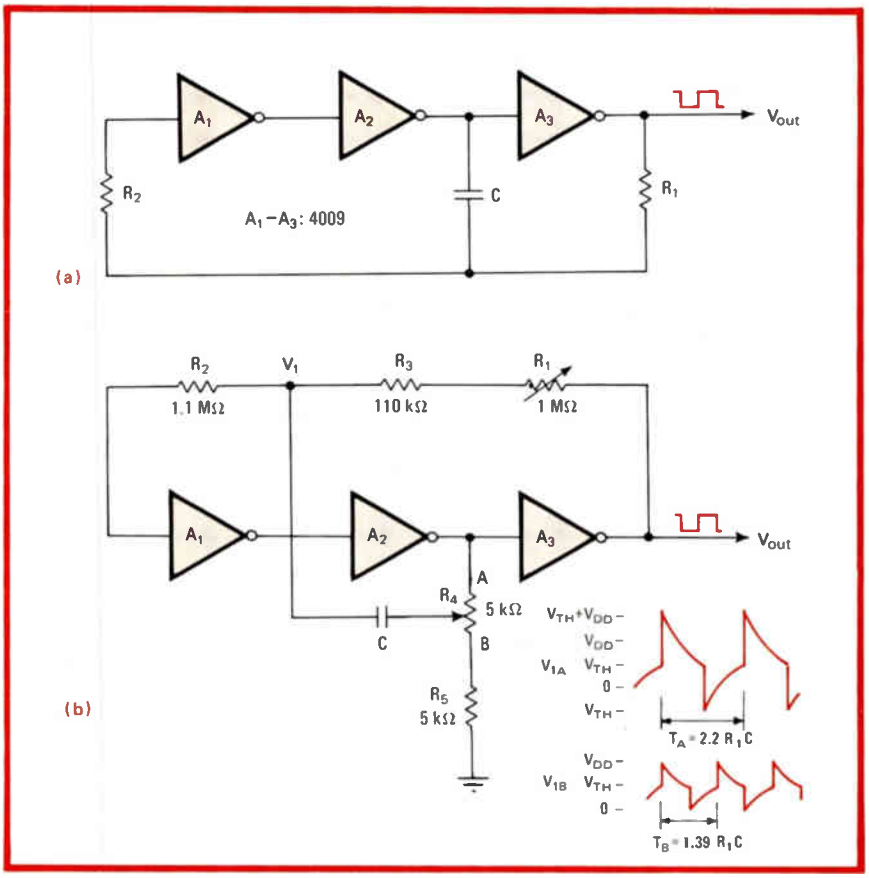
Useful as it is, the square-wave RC oscillator implemented in complementary-MOS has one shortcoming—setting its maximum and minimum frequencies of oscillation independently while also maintaining accuracy is extremely difficult. By placing a voltage divider in the feedback loop of the conventional three-gate circuit, however, a one-time trimming adjustment can accurately set the maximum and minimum frequency excursion and will force the ratio of the upper to the lower limit of oscillation to approach a value virtually determined by the resistors used in the same divider.

The standard RC oscillator generates a frequency of $f \approx 0.482/R_1C$, where $R_1 = R_2$, as shown in (a). Generally, it is not practical or economical to use a variable capacitor for C. A potentiometer could be substituted for $R_1$ to tune the frequency, but slight differences in integrated-circuit parameters will preclude predicting the maximum and minimum frequencies of oscillation with any degree of accuracy for a particular chip. The only other method for setting the upper and lower frequency limits is to parallel several capacitors across C, a tedious procedure at best.

Alternatively, $R_1$ can be a potentiometer that is placed virtually in parallel with voltage divider $R_4$–$R_5$ through C (b). In this way, capacitor C is no longer charged from the fixed-voltage output of the middle gate in (a), but from the voltage divider across the output. $R_1$ is thus used to change the circuit's time constant without affecting the potential that is applied to C.

The upper and lower limits of oscillation are determined by the position of $R_4$'s wiper arm and by the values of $R_4$ and $R_5$. With the tap at point A, the circuit will oscillate at a frequency given by $f = 1/2.2R_1C$. With the wiper at point B, the frequency will be $f = 1/1.39R_1C$. The frequency ratio to be expected is thus $2.2/1.39 = 1.6$. The actual frequency change measured with the particular chip used for breadboarding was 56%, which is thus very close to the intended value. The ratio will increase as $R_4$ is made larger with respect to $R_5$.

The circuit has only one small disadvantage—the load presented by $R_4$ and $R_5$ does increase the power-supply drain by approximately 0.5 milliampere. □




**Calibrate.** IC anomalies, inherent circuit imbalance, and the expense of making C variable preclude setting upper and lower oscillation limits of typical RC oscillator (a) with any accuracy. Placing $R_1$ virtually in parallel with voltage divider (b) through C gives circuit one-knob frequency control, with upper-to-lower oscillation ratio in effect determined by $R_4$ and $R_5$.

# Digital comparator minimizes serial decoding circuitry

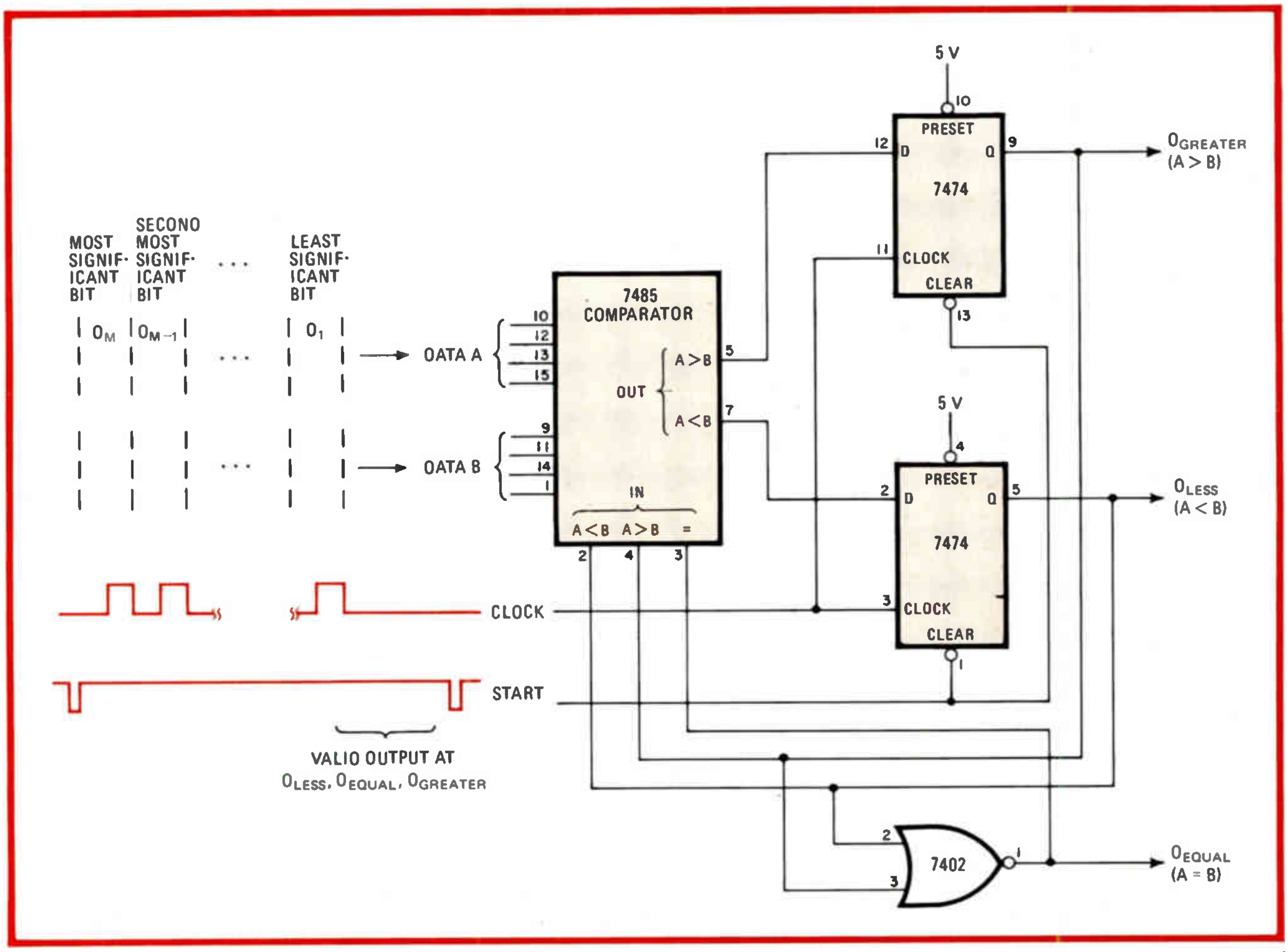
by Harland Harrison
*Memorex Inc., Communications Division, Cupertino, Calif.*

Using significantly fewer chips than the comparator proposed by Patil and Varma[1], this two-word, 4-bit comparator offers other advantages as well—it accommodates any word length and is more easily modified to handle any bit width. The control signals needed to facilitate the comparison can also be more conveniently applied.

The circuit outputs are first cleared with a negative-going pulse from the start signal. This sets outputs $O_{LESS}$ and $O_{GREATER}$ low. $O_{EQUAL}$, derived from $O_{LESS}$ and $O_{GREATER}$, goes temporarily high. At this time, the numbers can be presented to data buses A and B for comparison, with the least significant bit pair introduced first. As a consequence of the configuration, any number of bit pairs per word can be compared without modifying the circuit at all. The data buses each accept up to 4 bits, but this number may be expanded simply by cascading 7485 comparators.

The result of each bit-pair comparison is then latched into the 7474 flip-flops by the $D_i$ clock pulse, with the results of each bit-test being fed to the cascade inputs of the 7485. As a result, the comparator keeps track of the previous bit-pair check while continuing to update its results as each succeeding bit pair is introduced. Thus, the need for additional memory and logic elements is eliminated. The final result becomes valid after the $D_m$ clock pulse, where m is the word length in bits, and remains valid until the next start pulse. □

**References**
1. V. L. Patil and R. Varma, "Digital comparator saves demultiplexing hardware," *Electronics*, Aug. 14, 1980, p. 129.




**Less memory.** Circuit performs 4-bit comparison of two numbers with minimal circuitry. 7485 comparator replaces large numbers of flip-flop–type memories and logic elements by keeping track of previous bit-pair checks in real time as each pair is introduced. Circuit accommodates any word length; bit width is expandable simply by cascading 7485 comparators.

IMMEDIATE DELIVERY

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## 820 RO

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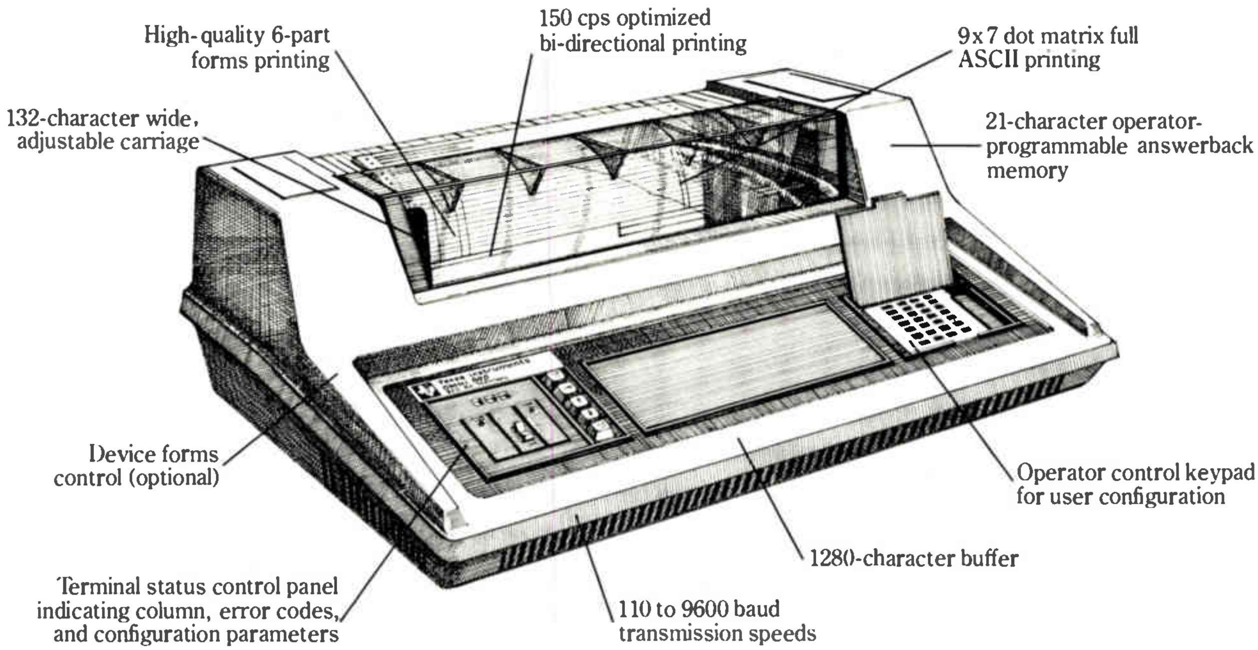


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# TEXAS INSTRUMENTS

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# Voltage-controlled resistance switches over preset limits

by Chris Tocci
*Halifax, Mass.*

Using two field-effect transistors as switches, this voltage-controlled resistor network can order up any value of resistance between two preselected limits. It is unlike other circuits in that it does not employ the drain-to-source resistance of matched FETs, whose $R_{ds}$ characteristics are usually proportional to a control voltage. As for circuit linearity, it will far exceed that of conventional networks using a single FET in various feedback configurations.[1]

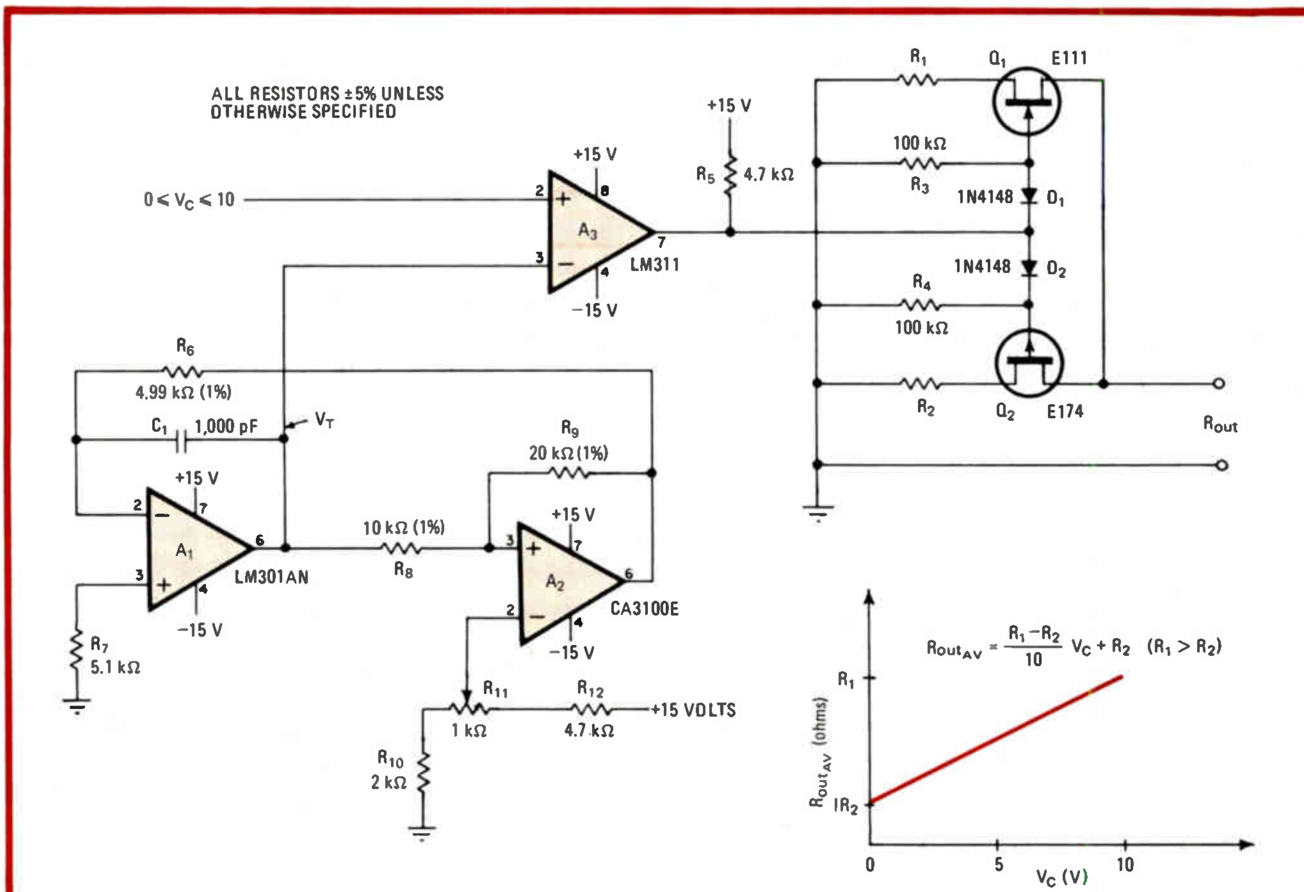
In operation, oscillator $A_1$–$A_2$ generates a 0-to-10-volt triangle wave at 100 kilohertz, which is then compared with the control signal, $V_c$, at $A_3$. During the time that the control exceeds switching voltage $V_T$, FET $Q_1$ is turned on, and resistor $R_1$ is placed across resistance $R_{out}$ (disregarding the $R_{ds}$ of $Q_1$). At all other times, FET $Q_2$ is on and resistor $R_2$ is placed across $R_{out}$. Thus $R_{out}$ is equal to an average value proportional to the time each resistor is placed across the output terminals, with the actual resistance given by $R_{out} = (R_1 - R_2)V_c/10 + R_2$, for $R_1 > R_2$. This relationship will hold provided any potential applied to the $R_{out}$ port from an external device is less in magnitude than the supply voltages; that any signal processing at $R_{out}$ be done at a frequency at least one decade below the 100-kHz switching frequency; and that the upper and lower resistance limits, $R_1$ and $R_2$, are much greater than the on-resistance of $Q_1$ and $Q_2$, respectively.

Potentiometer $R_{11}$ adjusts the baseline of $V_T$ to zero so that with $V_c = 0$, $R_{out}n = R_2$, where n is a constant. Further calibration can be carried out by trimming $R_1$ and $R_2$ to precise values.

This circuit is readily adapted to many applications, such as a one-quadrant multiplier. This is achieved by connecting a voltage-controlled current source into the $R_{out}$ port to build a dc-shift amplitude modulator whose carrier frequency is the switching frequency. The audio information or data is taken from $V_c$, but with the signal offset by 5 volts. Thus the dynamic range of the circuit will be 10 V. □

**References**
1. Thomas L. Clarke, "FET pair and op amp linearize voltage-controlled resistor," *Electronics*, April 28, 1977, p. 111.






**Ohmic linearization.** FET switches in voltage-controlled resistor network place maximum-minimum resistors $R_1$ and $R_2$ across $R_{out}$ so that the resistance is proportional to the average time each is across output port. Switching technique ensures piecewise-linear operation. This circuit lends itself to many applications, such as a-m modulator, by placing voltage-controlled current source across $R_{out}$.

RCA

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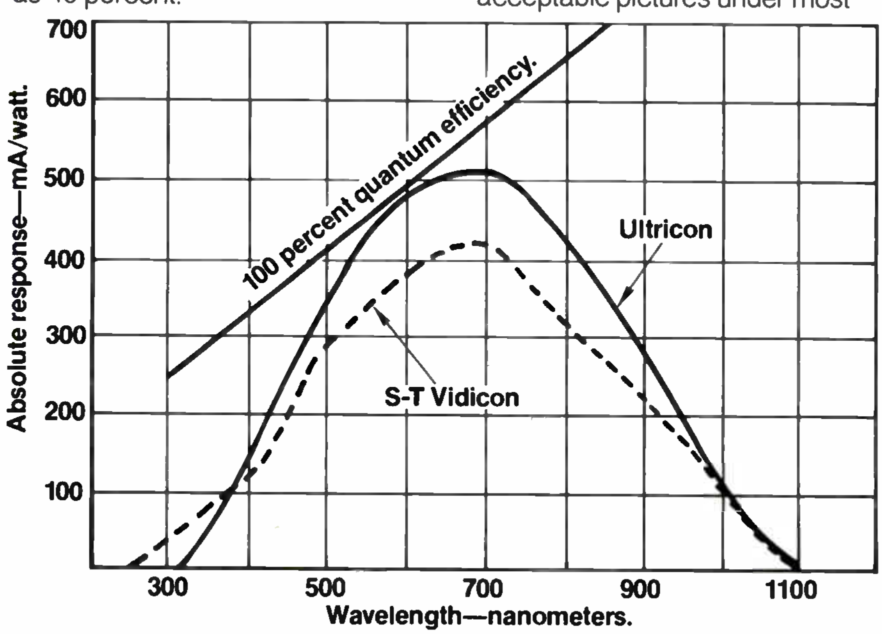


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# Thermal management techniques keep semiconductors cool

Heat-dissipation requirements depend on device and heat-sink thermal resistance, type of cooling, maximum junction temperature, mechanical factors, and the thermal environment

by Greg Owen, *International Electronic Research Corp., Burbank, Calif.*

☐ The thermal design of equipment is as important as its electronic design when it comes to reliability and performance. Yet semiconductor thermal management—the technique of controlling the devices' operating junction temperatures—becomes more crucial as larger and larger power semiconductors appear.

The operating junction temperature directly affects reliability in semiconductors. The power dissipated is lost as heat, which thermal management aims to remove safely, efficiently, and economically. Figure 1 shows the improvements in component reliability to be expected by lowering junction temperatures in junction transistors.

The best thermal management requires a preliminary design analysis of which semiconductors will be subjected to high temperatures and what is required to cool them. The optimized circuit-board layout can then make room for heat dissipaters if necessary.

### The thermal circuit

Heat generated in a transistor is the product of the voltage drop across the emitter-to-collector junction multiplied by the current flow through it. Maximum power at this junction depends on semiconductor material and how the generated heat is dissipated.

Most germanium devices can operate at a junction temperature of no more than 100°C. Silicon devices can operate at junction temperatures of between 150° and 200°C. Before considering heat transfer, some basic parameters should be established.

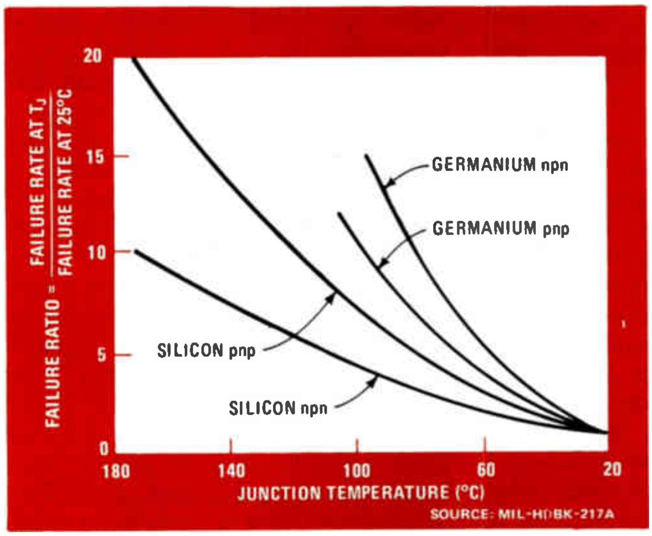
Thermal resistance (Θ) is defined as the quotient of the temperature drop (ΔT) between two points and the heat flux (Q), or power, passing between them under steady-state conditions:

$$\Theta = \Delta T/Q \quad (1)$$

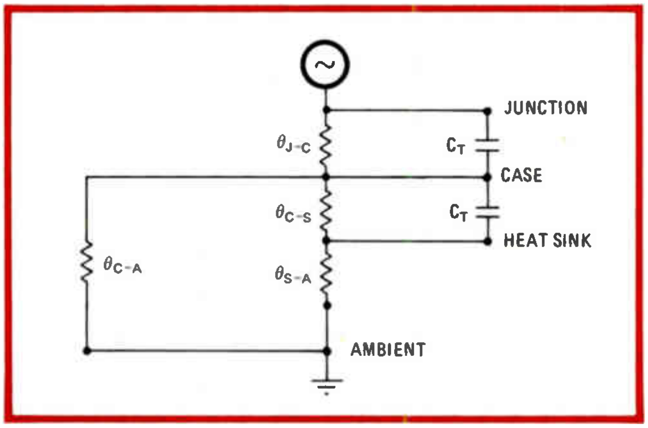
The temperature drop is usually measured between the point of heat generation (semiconductor junction) and some reference point (the case or the heat sink, for example) allowing the junction temperature calculation. Several thermal resistances are in series between the heat-generation point and the ultimate heat sink, typically ambient air.

The heat flow or thermal resistance problem may be analyzed in terms of the electrical analog of Fig. 2, where:

- ΔT (temperature drop) is analogous to voltage drop.
- Θ (thermal resistance) is analogous to resistance.
- P or Q (power generated or dissipated in the semiconductor business) is analogous to power.
- K (constant of thermal conductivity) is analogous to




**1. Heat kills.** As the junction temperature of a transistor rises, its failure ratio goes up. For instance, a silicon npn transistor has about a 7.5 times higher failure ratio at 140°C than at 20°C. Germanium types have even higher failure rates at elevated temperatures.




**2. Thermal circuitry.** The thermal circuit of a transistor mounted to a heat sink can be analyzed in terms of this equivalent electrical analog. Thermal resistance, Θ, is analogous to ohmic resistance, and $C_t$, heat capacity, is analogous to electrical capacitance.

| TABLE 1: THERMAL RESISTANCE, JUNCTION TO CASE, $\theta_{j-c}$ (°C/W) | |
|---|---|
| Case | Thermal resistance, junction to case |
| TO-18 (glass header) | 130 – 220 |
| TO-5 (glass header) | 30 – 50 |
| TO-5 (metal header) | 20 – 40 |
| TO-3 (typical: 2N3055) | 0.5 – 6.0 (1.5 max) |
| TO-66 (typical: 2N3054) | 1.5 – 15 (7.0 max) |
| TO-36, TO-6 (typical: 2N174) | 0.5 – 1.0 (0.5 max) |
| TO-63 (typical: 2N4210) | 0.4 – 2.0 (1.0 max) |
| TO-61 (typical: 2N5678) | 0.5 – 2.0 (1.0 max) |
| TO-8 (typical: 2N1483) | 1.5 – 15 (7.0 max) |
| DO-4 (typical: 1N3879) | 2 – 7 (2.5 max) |
| DO-5 (typical: 1N1195A) | 1 – 1.5 (1.2 max) |
| TO-126 (typical: 2N4921) | 4 – 15 (4.15 max) |
| TO-127 (typical: MJE3055) | 1 – 2 (1.39 max) |
| CASE 152 (MOTA) (typical: MPSU01) | 11 – 18 (11 max) |
| TO-220 (typical: G.E. D44C8) | 1.7 – 5 (4.2 max) |
| TO-116 (kovar frames) (copper alloy frames) | 59 – 91 30 – 40 |
| TO-202 (typical: G.E. D40D8) | 15 – 25 (20.0 max) |
| TO-92 | 175 – 200 |

electrical conductivity.

■ $C_t$ (heat capacity) is analogous to capacitance.

The effect of $C_t$ will be discussed in the section on pulsed-power operation.

Figure 2 can be summarized mathematically as:

$$\Theta_{j-a} = \Theta_{j-c} + \Theta_{c-s} + \Theta_{s-a} \quad (2)$$

where:

$\Theta_{j-a}$ = thermal resistance, junction to ambient
$\Theta_{j-c}$ = thermal resistance, junction to case
$\Theta_{c-s}$ = thermal resistance, case to heat sink
$\Theta_{s-a}$ = thermal resistance, heat sink to ambient

The following equation also derives from Fig. 2 and determines heat-sinking requirements:

$$\Theta_{c-a} = \Theta_{c-s} + \Theta_{s-a} \quad (3)$$

where $\Theta_{c-a}$ = case-to-ambient thermal resistance.

Outward heat transfer (or flow) from the heat-generating junctions begins inside the semiconductor and depends on a number of factors, including the thermal conductivity and geometry of the semiconductor die; the bond between the die and its mount; the thermal conductivity of the mount material; the geometry of the mount; and the thermal resistance of the interconnection lead.

The circuit designer has no control over these factors and must therefore rely on the manufacturer's junction-to-case thermal resistance ($\Theta_{j-c}$) rating. However, since semiconductor circuits are available in many package shapes (TO-3, TO-66, TO-220, and so on), each with different thermal characteristics, temperatures can be lowered by changing packages. Table 1 lists approximate $\Theta_{j-c}$ for typical semiconductor packages.

## Case-to-sink thermal resistance

The first thermal resistance outside of the semiconductor is through the interface of the semiconductor and heat sink. Thermal control measures taken here have a major impact on operating junction temperatures.

For example, a TO-3 transistor case-to-sink interface can range from a low of 0.1°C per watt (for an interface with no insulator and with thermal joint compound) to a high of approximately 2°C/W (with a dry insulator). With a power dissipation of 15 W, the TO-3 case (and also the junction) would be 15 W (2.0° to 0.1°C/W), or 29°C hotter in the latter case.

Thermal resistance across any interface is a function of cross-sectional contact area, surface finish and flatness, applied load between the surfaces, and the thermal conductivity of the material filling small gaps in the interface area.

Brazing or soldering the surfaces together would provide the lowest thermal resistance across these joints by giving the interface a metallic filler with high thermal conductivity. This is usually not feasible because of the varying coefficients of different metals. Rather, the following guidelines should be observed:

■ The surface should be kept flat and smooth.

■ The maximum possible surface contact area should be maintained.

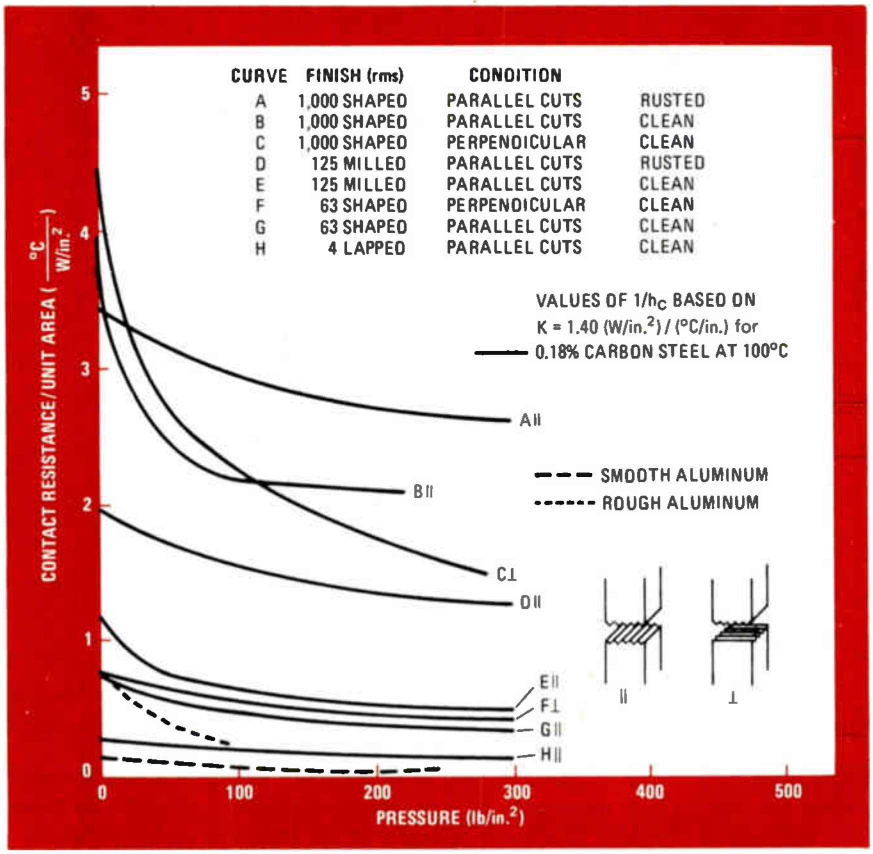
■ Where practical, thermal joint compounds should be used.

■ Where bolts, studs, or screws are used for mounting, torque should be set to the manufacturer's recommended values. Increased torque yields higher contact pressure within allowable stress limits.

In most applications, surface finishes are in the 63-to-125-microinch root-mean-square range. It can be very expensive to produce surface finishes smoother than 63 μin., so improvement in this area is often uneconomical. The interface thermal resistance can be reduced by filling in the small voids between surfaces that are not perfectly smooth with thermal contact fluids, or joint compounds, having a higher thermal conductivity than the air. The fillers generally consist of fine metal or oxide particles suspended in a carrier fluid and typically have 10 to 100 times the conductivity of air. Table 2 lists the thermal conductivities of various materials.

In addition to their finish, the flatness of the two surfaces is also important. Flatness is expressed in inches of total indicated reading (TIR) per inch of surface length. This generally falls within a range of from 0.005 to 0.008 TIR. Achieving flatness under 0.005 in. requires a special machining operation, which increases cost.

The geometry of the surface is as important as its absolute flatness. Attempting to flatten surfaces that are




**3. Thermal contact.** Thermal contact resistance is a function of pressure and surface flatness. Increasing clamping torque lowers thermal resistance. Surface smoothness also has a large effect, as a comparison of rusted and clean surfaces of a similar heat sink indicate.

concave to each other will yield a large air gap, whereas surfaces that are convex will tend to flatten each other as pressure is applied, yielding a tight, efficient interface. Air gaps are common in stamped metal heat sinks of thin material, but become less noticeable in extruded heat sinks, where the material at the mounting interface is thicker and more resistant to bending. Semiconductor packages are designed to be slightly convex on the mounting surface, where two screws are used (such as the TO-3 and TO-66) to take advantage of this characteristic. Stud mount packages are usually slightly concave but will flatten out as torque is applied. On single-screw–mounted packages the geometry is less important because of nonuniform pressure distribution.

When an electrical insulator is required between the semiconductor and heat sink, the insulation must have the lowest possible thermal resistance.

When a hard insulator such as mica or one of the harder plastics is used, it becomes even more necessary to use a thermal joint compound. These insulators do not flow as well as the rubberized types and so leave air gaps. Also, there is now thermal resistance in the two interfaces (case-to-insulator and insulator-to-sink) as well as in the insulator itself, so control of the interfaces is a major consideration. Table 3 illustrates typical case-to-sink thermal resistance for some common insulating materials.

The torque of all mounting hardware should be set to the manufacturer's recommended level in order to achieve maximum contact pressure between the surfaces. This greatly reduces interface thermal resistance, especially in the lower contact pressure ranges (10 to 100 pounds/in.$^2$) common in mounting semiconductor devices (see Fig. 3). One of the most cost-effective measures in reducing interface thermal resistance, it is easily controlled and allows repeatable thermal resistance values.

Often overlooked is the need to reset the torque of the mounting hardware after a flow or wave solder operation, when the entire circuit board has been heated and then cooled. This usually reduces the torque. Where solder lands are present, solder melts and can flow out from under the mounting hardware because of the pressure, giving the hardware substantially lower than recommended torque. These factors can cause the hardware to be substantially below the rated torque after soldering even though it was properly torqued prior to soldering.

## Heat sink thermal resistance

There is no single thermal resistance value for a heat sink; the value changes with conditions. As Fig. 4 illustrates, heat sink thermal resistance decreases with a rise in operating power. Air flow also has a significant impact in reducing thermal resistance, even at low velocity, by increasing the heat transfer efficiency from the sink to the air.

The best way to determine a heat sink resistance value is from a graph of rises in case temperature above the ambient versus the power dissipated for the heat sink. The designer can thus determine the case temperature rise for a given power dissipation. Heat sink dissipation is a result of the three distinct modes of heat transfer—conduction, radiation, and convection.

In the first mode, heat is conducted through the heat

TABLE 2: THERMAL CONDUCTIVITY CONSTANTS OF FREQUENTLY ENCOUNTERED HEAT SINK MATERIALS

| Material | K (Btu/h/ft²/°F/ft) | K (W/in.·°C) |
|---|---|---|
| Still air | 0.016 | 0.0007 |
| Alumina (99.5%) | 16 | 0.70 |
| Beryllia (99.5%) | 114 | 5.00 |
| Silver | 242 | 10.6 |
| Diamond | 364 | 16.0 |
| Gold | 172 | 7.57 |
| Epoxy | 0.114 | 0.005 |
| Thermally conductive epoxy | 0.45 | 0.02 |
| Aluminum alloy 1100 | 128 | 5.63 |
| Aluminum alloy 3003 | 111 | 4.88 |
| Aluminum alloy 5052 | 80 | 3.52 |
| Aluminum alloy 6061 | 99 | 4.36 |
| Aluminum alloy 6063 | 111 | 4.88 |
| Copper alloy 110 | 226 | 9.94 |
| Beryllium copper 172 | 62 – 75 | 2.7 – 3.3 |
| Brass alloy 360 | 67 | 2.95 |
| Stainless steel 321 | 9.3 | 0.41 |
| Stainless steel 430 | 15.1 | 0.66 |
| Steel, low-carbon C1040 | 27 | 1.19 |
| Titanium | 4 – 11.5 | 0.2 – 0.5 |

sink material from the transistor interface area to the sink's major heat-dissipating areas, which are either fingers or fins. The failure to optimize the material and heat-flow geometry can result in the case running hotter, and the sink cooler, than anticipated.

At steady state, conduction of heat through a length of material follows Fourier's law:

$$Q = KA\Delta T/L \qquad (4)$$

Heat conduction is directly proportional to the thermal conductivity of the material (K), the cross-sectional area of the flow path (A), and the temperature differential (T) along the material. It is inversely proportional to the length (L). Variation of K with temperature can be neglected within the limits of environmental conditions relevant to electronic packages. This equation can also be used to determine $\Theta_{c\text{-}s}$ where a filler of known thermal conductivity is used.

For optimum heat transfer by conduction, materials that have the highest thermal conductivity (consistent with good structural considerations, price, and availability) should be used. $T_2$ (where $\Delta T = T_1 - T_2$) should be kept at as low a value as possible and the thermal path as short as possible.

Table 2 lists the thermal conductivities for materials typically used in heat-transfer applications. Epoxy, even thermally conductive epoxy, is a poor conductor. Copper is the most conductive of available heat-transfer materials, but aluminum, because of its lower material cost, weight, and ease of fabrication, is most frequently used. Aluminum's conductivity is directly affected by alloying elements. But factors like strength, environmental resistance, and cost are important in choosing an alloy.

In space applications, conduction may be the only form of thermal transfer open to the designer. Here, heat is conducted from the semiconductor to the card-racking structure, chassis, or other point of high thermal mass. It is important to keep the thermal path as short as possible, a factor to consider in the layout of a circuit board.

### Heat radiation

In most situations, the heat sink or the heat dissipater transfers the unwanted energy to the ambient air by radiation or radiation with convection. Thermal radiation is the transfer of heat by electromagnetic radiation (primarily in the infrared wavelengths). It is more difficult to analyze than heat transfer by conduction, since the rate of heat flow by radiation is a function of the emissivity of the surface, the surface area, and the fourth power of the absolute temperature differential.

The Stefan-Boltzmann law states that the total energy radiated by a perfect blackbody radiator is proportional to the fourth power of the absolute temperature differential. This usually takes the form of:

$$Q_{rad} = SA_{\sigma}[(T_1)^4 - (T_2)^4] \qquad (5)$$

In this equation:
S = shielding factor
A = area of the radiator
$\sigma$ = Stefan-Boltzmann constant ($0.003710^{-8}$ in the watt-per-square-inch–kelvin system)
$T_1$ and $T_2$ = temperatures of the hot and cold bodies, respectively, in kelvin.

The emissivity ($\epsilon$) is a derating factor for surfaces that are not blackbodies. It is defined as the ratio of the emissive power of a given body to that of a blackbody for which the emissivity is unity. Some bodies, such as lampblack, approach unity very closely and are consequently called black. The term has little to do with color in the optical sense; bodies of any color can have high emissivities and be referred to thermally as blackbodies. (For example, the emissivity of anodized aluminum is

| TABLE 3: TYPICAL INTERFACE THERMAL RESISTANCE FOR INSULATORS | | | | |
|---|---|---|---|---|
| Material | Thickness (in.) | Device | Torque (in.-lb) | Case-to-sink interface thermal resistance (°C/W) |
| Beryllium oxide | 0.1132 | TO-3 | 8 | 0.22 |
| | 0.1132 | TO-66 | 6 | 0.45 |
| | 0.1132 | TO-220 | 3 | 1.4 |
| Mica | 0.0057 | TO-3 | 8 | 0.8 |
| | 0.0057 | TO-66 | 6 | 1.6 |
| | 0.0057 | TO-220 | 3 | 5.2 |
| Plastic (Kapton) | 0.002 | TO-3 | 8 | 0.8 |
| | 0.002 | TO-66 | 6 | 1.6 |
| | 0.002 | TO-220 | 3 | 5.2 |
| Insulube 448 | 0.0039 | TO-3 | 8 | 0.9 |
| | 0.0039 | TO-66 | 6 | 1.8 |
| | 0.0039 | TO-220 | 3 | 5.9 |
| Filled elastomers | 0.010 | TO-3 | 8 | 0.4 – 1.0 |
| | 0.010 | TO-66 | 6 | 0.8 – 2.0 |
| | 0.0095 | TO-220 | 3 | 2.6 – 6.5 |
| Silicone rubber | 0.012 | TO-3 | 8 | 1.2 |
| | 0.012 | TO-66 | 6 | 2.4 |
| | 0.012 | TO-220 | 3 | 7.9 |
| Bare device | – | TO-3 | 8 | 0.15 – 0.25 |
| | – | TO-66 | 6 | 0.35 – 0.45 |
| | – | TO-220 | 3 | 0.55 – 0.65 |

Note: Thermal joint compound used except for filled elastomers and silicone rubber.

the same if it is dyed black, red, blue, and so on.) A matte or dull surface, however, will be more radiation-efficient than a bright, glossy surface. The surface emissivity of a heat dissipater is largely dependent on its surface finish. Table 4 lists some common surface emissivities of typical heat dissipaters.

The area term, A, must usually be derated by the shielding factor, S, to yield the effective surface area. In many designs, and extrusions in particular, the radiant energy emitted by one fin is often reabsorbed by an adjacent fin because radiant energy flows on a path perpendicular to the surface. This energy flow will continue until air molecules or another surface absorb it. Thus, closely spaced fins have little effective radiation area because they merely bounce the radiant energy back and forth, and S is consequently small in value. S increases as the fins are moved apart and more air molecules absorb energy. S equals 1.0 and all area is effective when there is no reflecting surface such as a flat plate suspended in air.

This fact should figure in the layout of circuit boards. When a high-temperature component is located near a heat dissipater, that dissipater will absorb some energy, causing it to run hotter than it normally would.

A designer can take maximum advantage of radiation by using a heat sink that affords maximum surface area for a given volume. Care should be taken here that no surfaces of the same heat sink in close proximity are radiating to each other. Surface finishes should be kept as highly emissive as possible, so that they radiate thermal energy and do not absorb it from other hotter bodies. Heat sink materials should be used that conduct the thermal energy to the dissipating surfaces as fast as possible to keep a high temperature differential between dissipating surfaces and air.

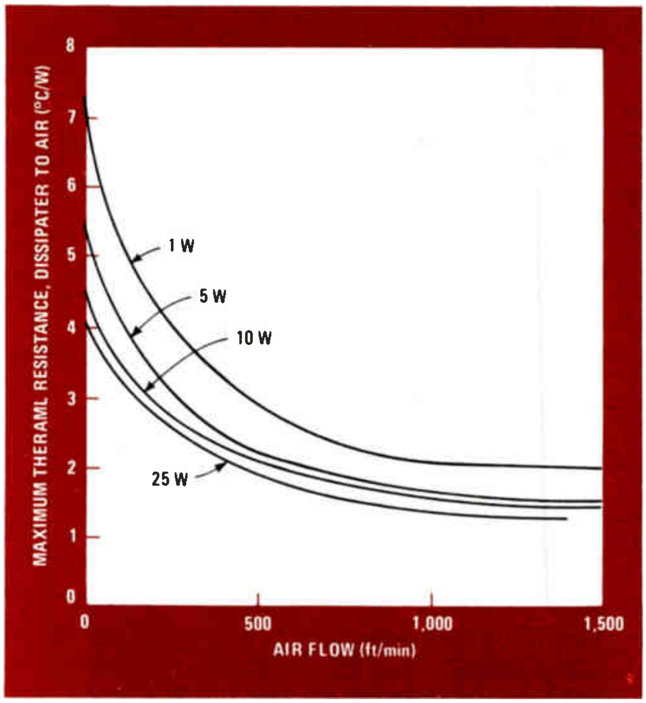
## Convection complexities

Convection is the most complex heat-transfer mode, involving the mixing of fluids. The rate of heat flow by convection from a solid surface to a fluid is a function of the area of the solid in contact with the fluid, the temperature differential between the fluid and the solid, and certain properties of the fluid.

The contact of any fluid—air, for instance—with a hotter surface reduces its density and causes it to rise. Circulation resulting from this phenomenon is known as free or natural convection. Since convection heat transfer is closely related to fluid motion, an understanding of the effects of laminar and turbulent flow, and their differences, is helpful.

In laminar flow, the air moves in layers, each molecule following a smooth and continuous path called a streamline. The molecules in each layer remain in orderly sequence and do not appreciably mix across the streamlines. A boundary layer of air exists along a hot surface and heat is transferred between the air layers primarily by radiation from the warm molecules and by conduction between molecules that come into contact.

In contrast, turbulent flow is characterized by the random motion of the air molecules. Heat transfer from layer to layer is aided by innumerable eddies that carry the air molecules across the streamlines. These molecules carry energy and transfer heat by mixing with other air particles and by breaking up the boundary layer so




**4. Thermal resistance variation.** These curves plot the variations of a typical heat sink's thermal resistance with airflow and power dissipated. As power dissipation increases, thermal resistance decreases. Increasing airflow also decreases thermal resistance.

cooler air molecules come into contact with the heat sink more frequently, increasing the temperature differential. Any increase in turbulence will increase the rate of heat flow by convection. Either natural convection or forced convection with fans or blowers can create the airflow.

The general equation for convection is usually written:

$$Q_{conv} = hA(T_{surface} - T_{fluid}) \quad (6)$$

Here A is the area of the heat sink and T is the temperature. All other variables that affect convection efficiency are considered in the derivation of h (coefficient of convection), or heat transfer per unit area; h is a function of the fluid, flow velocity, and flow path.

Heat transfer by forced convection with a properly designed forced-air heat sink can be as much as 10 times more efficient than natural convection. Turbulent airflow usually begins to occur at velocities of approximately 3 feet/second with a concurrent increase in heat transfer. As Fig. 4 shows, there is as much reduction in thermal resistance by going from still air to 200 feet/minute as there is from 200 ft/min to 1,000 ft/min. Also, it has been found that velocities in excess of 1,000 ft/min do not significantly reduce heat sink thermal resistance. Forced convection is more expensive than natural convection and should be resorted to only at extremely high power-density levels.

In forced convection, the effect of heat transfer by radiation is greatly minimized. At sea level, with a well-designed natural convection heat sink, heat is transferred by approximately 70% natural convection and 30% radiation. When forced convection is used, transfer by radiation can be reduced to only a 2%-to-7% contribution because of lower heat-sink temperatures and greater convection efficiency. In forced-air designs, heat transfer by radiation is frequently disregarded because of its small contribution. When a heat sink is specifically designed for forced-air applications, the fins can be moved much closer together since radiative heat transfer is no longer a factor.

Other application factors that should be considered to maximize the advantages of convective cooling are:

- In natural convection, mounting the heat sinks so that the maximum length of convection surface is in the vertical plane.
- Mounting heat sources low on the heat sink. An exception here would be in the case of high-power devices on the same heat sink with low-power, temperature-sensitive devices. In this case, the low-power devices should be towards the bottom of the heat sink and the high-power devices farther up.
- Providing enclosure ventilation to ensure the natural convection of the air.
- In forced convection, keeping low-power components upstream, with devices generating higher heat downstream.
- Providing ducts for equipment that properly maintain optimum pressure heads throughout, ensuring higher velocities and more efficient heat transfer.
- Where flat-finned heat sinks are used, making sure that the height, length, and spacing of the fins can handle the amount of airflow. Where possible, spines should extend into the airflow to create turbulence.

## Altitude and ambient effects

As discussed previously, convection and radiation are the principal means of transferring heat to ambient air. At high altitudes, the convection becomes less effective as the air becomes less dense; at 70,000 feet, 70% to 90% of heat dissipation is by radiation. This factor is crucial in aircraft installations and greatly affects heat dissipator design and function. Figure 5 shows typical heat transfer degradation with altitude and can be used to derate heat sink values determined at sea level.

Since air density is directly proportional to temperature, convective heat transfer is less efficient at higher ambient temperature, where the air molecules thin out. As with altitude, adjustment to anticipated convection cooling should be taken into account if equipment must operate over an extreme range of ambient air temperatures.

At ambient temperatures up to approximately 50°C, there is usually no need to derate heat-sink values derived at 25°C, but the effect of the increased ambient temperature must still be directly applied when finding semiconductor case or junction temperatures (as $T_{amb}$).

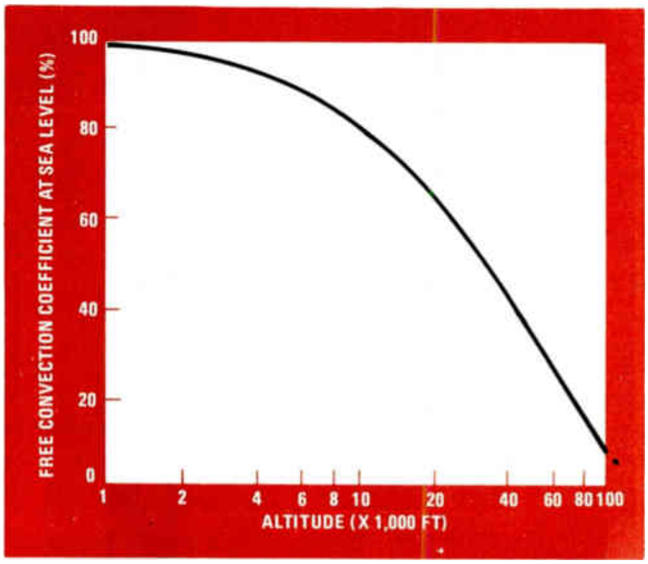
An ambient temperature that is realistic for the entire lifetime of the equipment should be selected. Setting it too high means an overly large heat sink; setting design ambient too low can mean very high device temperatures should it be exceeded.

A design ambient of 50°C (122°F) is frequently specified in commercial applications. Military requirements usually require design ambients of up to 71°C (160°F).

With high dissipation levels, either liquid cooling or vaporization (ebullition) cooling must be used. These

**TABLE 4: NORMAL EMISSIVITY OF VARIOUS SURFACES**

| Material and finish | Emissivity |
|---|---|
| Aluminum sheet, polished | 0.040 |
| Aluminum sheet, rough | 0.055 |
| Anodized aluminum, any color | 0.80 |
| Brass, commercial | 0.040 |
| Copper, commercial | 0.030 |
| Copper, machined | 0.072 |
| Steel, rolled sheet | 0.55 |
| Steel, oxidized | 0.657 |
| Nickel plate, dull finish | 0.11 |
| Silver | 0.022 |
| Tin | 0.043 |
| Oil paints, any color | 0.92 – 0.96 |
| Lacquer, any color | 0.80 – 0.95 |
| Insuluble 448 | 0.91 |




**5. Convection vs altitude.** This is a plot of the major effect of altitude on free convection heat transfer on a ½-inch-by-2-foot side fin. At 70,000 ft, convection is only about 30% effective, with the most of the heat being transferred by radiation.

will not be discussed in detail.

The amount of heat generated by a semiconductor is directly influenced by its mode of operation as well as by its power level and efficiency. Choosing a steady-state mode over a pulsed mode can affect heat dissipation requirements significantly.

## Steady-state conditions

Power dissipation under steady-state conditions ($P_{ss}$) depends on the sum of thermal resistances from the junction to the ultimate heat sink, the maximum allowable junction temperature, and the ambient temperature. Stated mathematically:

$$P_{ss\,(max)} = (1/\Theta_{j\text{-}a})(T_{j(max)} - T_{amb}) \qquad (7)$$

To determine the maximum dissipation of a semiconductor/heat-sink system the following inputs are needed: From the transistor manufacturer's data sheet:

$\Theta_{j\text{-}c} = 1.5°C/w$ (for a TO-3 in this example)
$T_{j\,(max)} = 200°C$

From the heat dissipater manufacturer's data sheet:

$\Theta_{s\text{-}a} = 2.5°C/w$

Assuming $\Theta_{c\text{-}s} = 0.3°C/w$ (for a TO-3 mounted with thermal joint compound and no insulator) and $T_{amb} = 50°C$, then:

$$\Theta_{j\text{-}a} = (1.5 + 2.5 + 0.3)°C/w = 4.3°C/w$$

To determine maximum allowable power:

$$P_{ss\,(max)} = (1/4.3)(200 - 50)\text{ w} = 34.9\text{ w}$$

To maintain junction temperatures below the rated maximum for greater reliability, the maximum design junction temperature should be substituted for $T_{j\,max}$ in the equation. The temperature of a device operating at a known power in a heat sink system can be predicted by rearranging the steady-state equation (Eq. 7) to:

$$T_{j\,(max)} = P_{ss\,(max)}\Theta_{j\text{-}a} + T_{amb} \qquad (8)$$

With a dissipation of 20 w, $\Theta_{j\text{-}a} = 4.3°C/w$ (above) and an ambient of 50°C yield:

$$T_{j\,(max)} = (20\text{ w})(4.3°C/w) + 50°C = 136°C$$

When a transistor is operated in a single, nonrepetitive, short-duration pulse-power mode, the maximum allowable dissipation is substantially greater than in the steady-state case.

## From the curve

Before the maximum power dissipation of a transistor in the previously specified thermal system in response to a single 1-millisecond pulse can be determined, the thermal characteristics of the transistor must be known. These are obtained from the maximum-operating-area curve in the form of a normalized power multiplier (M).

The graph of Fig. 6 shows that for a 1-ms pulse, the normalized power multiplier for a 2N3055, with a case temperature of 25°C, is 3. At higher case temperatures, the power multiplier must be linearly derated to zero at $T_{j(max)}$. The temperature-derating factor (TDF) is determined as follows:

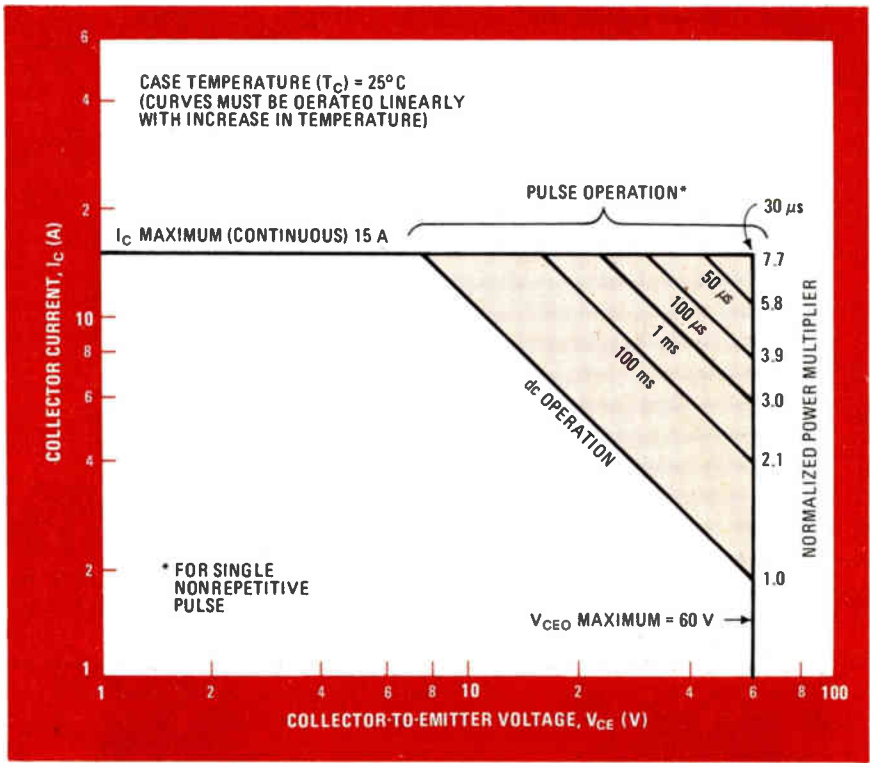
$$\text{TDF} = 1 - (T_c - 25°C)/(T_{j(max)} - 25°C) \qquad (9)$$

In this example, the heat sink's thermal capacitance is so large that its temperature rise from the 1-ms pulse will be negligible. Case temperature is the same as the ambient (50°C). This information and the maximum steady-state dissipation rating ($P_{max} = 115$ w and $T_c = 25°C$) can be used to find maximum power dissipation for a single 1-ms pulse ($P_{sp}$) as follows:

$$\begin{aligned} P_{sp} &= M(\text{TDF})(P_{max}) \qquad (10)\\ &= M[1 - (T_c - 25°C/T_{j(max)} - 25)](P_{max})\\ &= 3[1 - (50 - 25)/(200 - 25)](115)\\ &= 296\text{ w} \end{aligned}$$

## Repetitive-pulse operation

For a transistor operating in a repetitive-pulse mode, the previous analysis must be modified to take into




**6. Pulsed operation.** A family of curves displays maximum operating areas for a 2N3055 silicon power transistor. Using these curves and the device's junction-to-case thermal resistance, maximum power dissipation for single and repetitive pulse operation can be calculated relatively easily.

In this situation, it may be assumed that the transis- account the rise in case temperature caused by the average power dissipation. It is assumed that the transistor operates in response to a series of 1-ms pulses at a repetition rate of 100 Hz with the same thermal conditions specified for both steady-state and single-pulse operation.

For repetitive-pulse operation, the average power dissipation ($P_{avg}$) follows from the following relationship:

$$P_{avg} = P_{pk}d \quad (11)$$

where $P_{pk}$ = peak pulse power and d = duty cycle.

The effective $T_c$ that results is:

$$T_{c(eff)} = T_{amb} + P_{avg}\Theta_{j\text{-}a} \quad (12)$$

Note that the effective case temperature is based upon thermal resistance from junction to ambient, which takes into account thermal capacitance or inertia. Heat flow from the junction is "off" due to the built-up temperature differential created by its operation. The equation permits conservative design by assuming that case temperature equals junction temperature.

Substituting Eq. 11 into Eq. 12 yields:

$$T_{c(eff)} = T_{amb} + P_{pk}(d)\Theta_{j\text{-}a} \quad (13)$$

If $T_{c(eff)}$, as defined by Eq. 13, is substituted for $T_c$ in Eq. 10, the following expression is obtained for the maximum allowable power dissipation ($P_{rp}$) for repetitive pulses:

$$P_{rp} = \frac{M(T_{j(max)} - T_{amb})P_{max}}{T_{j(max)} - 25 + MdP_{max}\Theta_{j\text{-}a}} \quad (14)$$

The junction-to-case thermal resistance of a semiconductor whose maximum power is rated at a 25°C case temperature may be expressed by:

$$J_{j\text{-}c} = (T_{j(max)} - 25)/P_{max} \quad (15)$$

If the relationship expressed by Eq. 15 is used, Eq. 14 can be simplified to:

$$P_{rp} = M(T_{j(max)} - T_{amb})/(\Theta_{j\text{-}c} + Md\Theta_{j-a}) \quad (16)$$

For the numerical example considered, the following values were previously assumed:

$d = (1\text{ ms})(100\%)/10\text{ ms} = 10\%$
$T_{j(max)} = 200°C$
$T_{amb} = 50°C$
$\Theta_{j\text{-}c} = 1.5°C/W$
$M = 3$
$\Theta_{j\text{-}a} = 4.3°C/W$

When these values are substituted in Eq. 16, the maximum power dissipation under repetitive-pulse conditions is

$$P_{rp} = [3(200 - 50)]/[1.5 + 3(0.1)4.3]\text{ W} = 161\text{ W}$$

### Irregularly shaped repetitive pulses

For a conservative design when a transistor is subjected to irregularly shaped repetitive pulses, the maximum average power for the irregular pulse is calculated on the basis of the pulse width ($t_p$), the period between the leading edges of successive pulse (t), and the maximum steady-state dissipation $P_{ss(max)}$, as follows:

$$P_{avg} = P_{ss(max)}(t_p)/t \quad (17)$$

This equation can be substituted into Eq. 13 to give the following:

$$T_{c(eff)} = T_{amb} + P_{ss(max)}(t_p)/t\Theta_{j\text{-}a} \quad (18)$$

This equation can in turn be substituted for Eq. 10 as described above, in order to determine $P_{irp}$ or $T_j$. □

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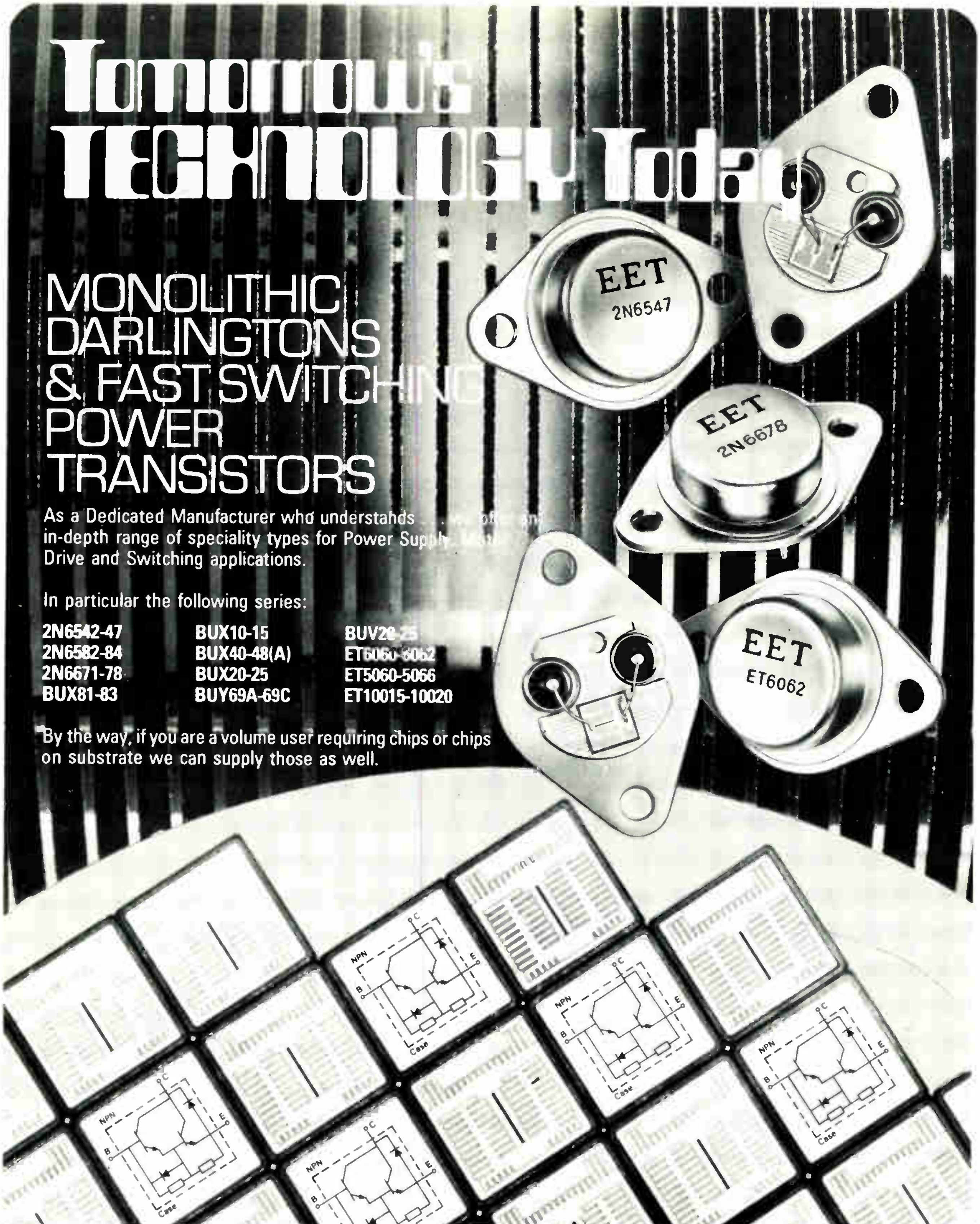
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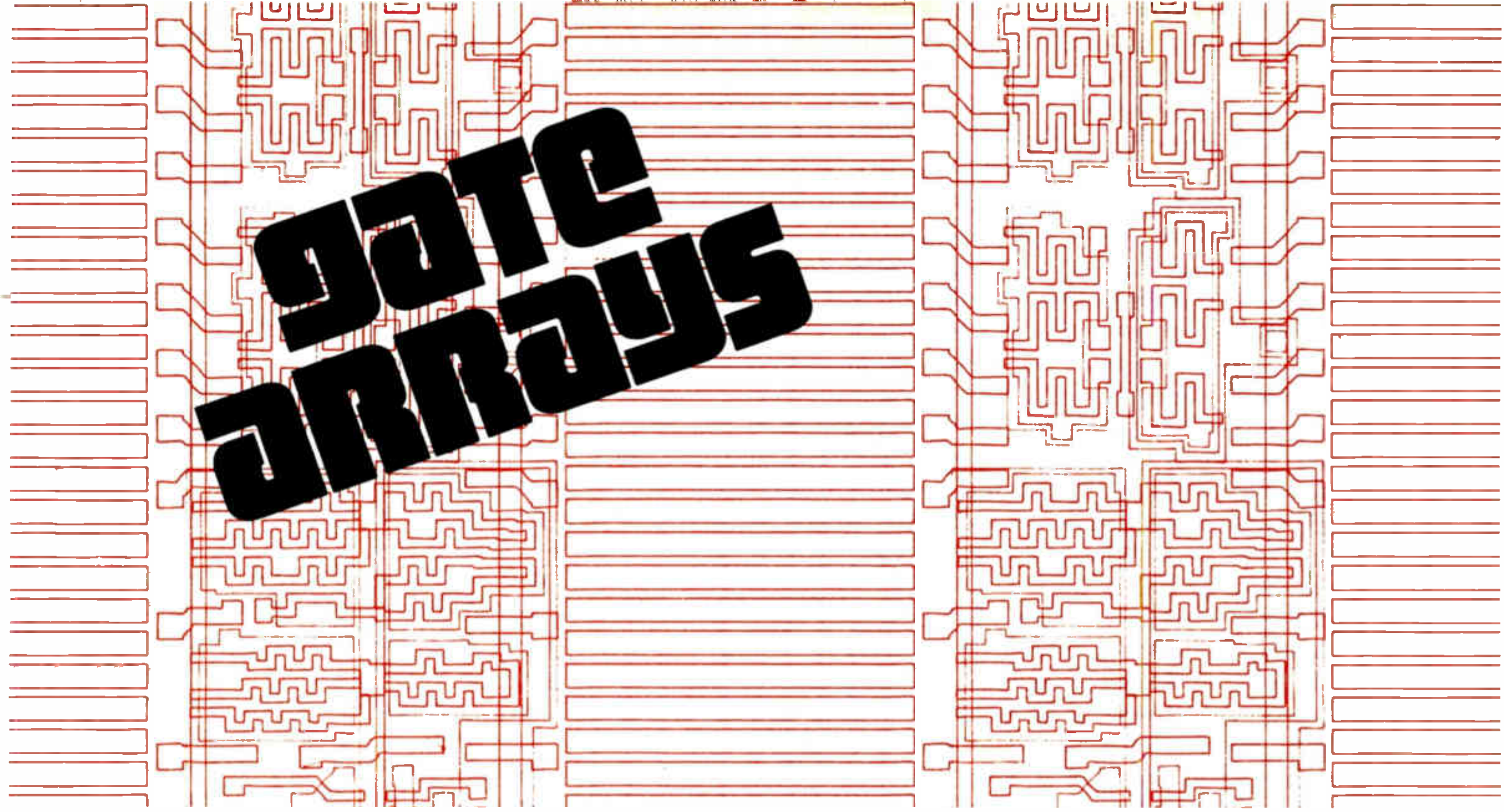



# A special report

Arrays have rushed in to fill the vacuum between high-volume standard parts and costly custom chips; now their growth depends on new resources for layout, testing, and packaging

by John G. Posa, *Solid State Editor*

☐ The concept of preprocessing an integrated circuit up to its final stages for later differentiation via fuse links or metalization patterning has been kicking around since the mid-1960s, but it has taken over a decade for this semicustom approach to IC fabrication to turn a profit commercially. Now nearly every major semiconductor manufacturer is jumping into the business and the market is exploding in the U. S., Europe, and Japan.

The semicustom logic rubric actually covers a number of techniques intended to provide a continuum of options falling between high-volume, low-cost standard logic chips and expensive, handcrafted custom ICs. These complementary approaches are easily distinguished when they are grouped according to cost and capability and when some of the myths about the semicustom industry are dispelled.

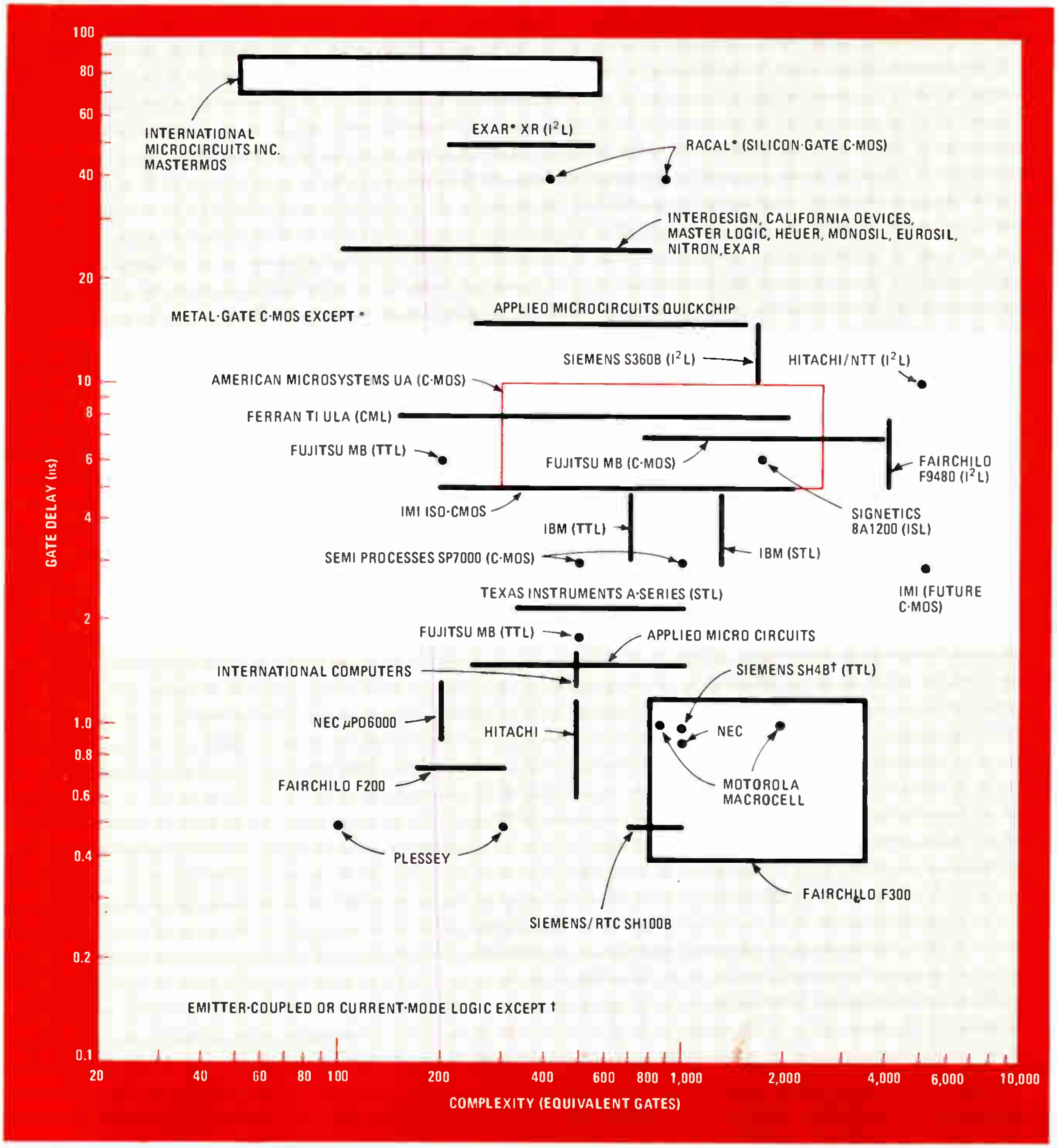
There are basically three forms of semicustom logic. They are, in increasing cost, density, and development turnaround time:

- Field-programmable ICs like the programmable array logic (PAL) chips from Monolithic Memories Inc. and its alternative sources, and the field-programmable logic arrays that were pioneered by Signetics Corp. and later adopted by others.
- Gate arrays or master slices produced by numerous commercial concerns and by computer companies for captive consumption.
- Standard-cell or polycell approaches such as the Microcells from Plessey Semiconductors and those used in the Composite Cells espoused by Signetics.

This report will concern itself only with gate arrays and standard cells, however, because of the involvement of so many more companies, technologies, and techniques than with field-programmable products. Also, the role of computer-aided customization—an important consideration not common to field-programmable devices—is transforming integrated circuit fabrication, with an almost complete demise of fully custom designs as one possible consequence.

## CAD is key

A growing availability of computer-aided-design software in the form of placement and routing algorithms is not the only reason for the resurgent popularity of gate arrays. As very large-scale integration squeezes more and more functions onto silicon substrates, the chips produced become less and less general. This does not mean that the users of electronics will be any less inter-




**1. A market divided.** Speeds of about 1 and 10 nanoseconds separate today's arrays into application areas. Lower-density metal-gate complementary-MOS slices do not compete with complex emitter-coupled logic. All points will shift down and to the right with time.

ested in integration. But it does imply that an increasing number of logic chips will be produced in lower volumes and—without automation—prohibitively high costs. That scenario does not, of course, apply to memory.

"As density rises, the uniqueness of the function goes up and so volume goes down," comments Joe Kroeger, director of marketing for International Microcircuits Inc., a Santa Clara, Calif., manufacturer of master-slice chips. "The microprocessor broke the back of that curve in the early '70s, so we bypassed the issue for some 10 years." The industry is back on that curve, according to Kroeger. In addition, "it turns out that anything you do in a microprocessor is slow. Dedicated logic, even in a slower technology, can usually outperform it."

Beyond memories and microprocessors, it is difficult to define a VLSI circuit with enough appeal to warrant the volumes necessary for a price below, say, $10. For instance, it will be interesting to chart the cost curves for some of the forthcoming sophisticated VLSI microprocessor-support circuits—the mathematics coprocessors, the memory management units, and so on.

Of course—particularly with VLSI—device price is only part of the grander goal: to reduce cost per function. Practically any IC will do this, even those high-class peripheral chips. The problem that is growing more acute is the definition of functions to integrate. If a company has a specific requirement that will demand a large enough volume, maybe it can stand the expense of developing a fully custom IC. But that's not so for those caught in between with a need for fewer parts—a need that cannot be filled with a microprocessor.

More and more customers will be shopping for semicustom logic. Dataquest Inc., a market research firm in Cupertino, Calif., believes that with such sales currently below $50 million, the market for semicustom logic is virtually untapped. But by 1985, says Dataquest, the global market for semicustom logic could amount to one third of that for all of bipolar digital logic. Indeed, some suppliers are reporting sales growth rates in excess of 100%. "I see gate arrays as being a major portion of the logic TAM [total available market] for the 1980s and beyond, quite frankly . . . it's the next-generation mainstream logic vehicle," adds L. R. "Gib" Gibson, manager of the gate array program for Texas Instruments Inc. in Houston.

Although gate arrays are another way to consolidate random logic, they do not really compete with the now ubiquitous microprocessor. After they were initially used to integrate discrete logic, "users figured out that the microprocessor was a lot more powerful than a board full of TTL," comments Justin Rattner, principal engineer at Intel Corp.'s Special Systems operation in Aloha, Ore.

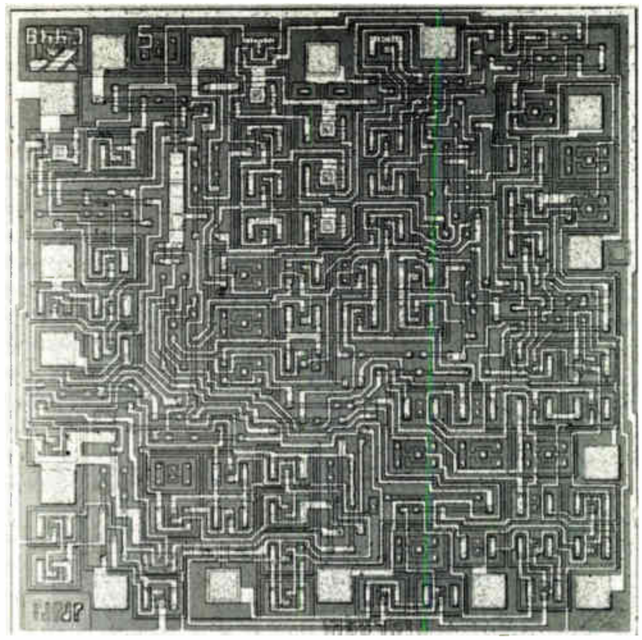
"What were ostensibly logic replacement applications began to take on a new intelligence through programming," continues Rattner. In contrast, gate arrays appear destined to remain in the realm of logic replacement. "And if the application is to build a computer—if that's the logic you're replacing—then after designing and verifying the logic you still have to write programs," Rattner avers. That is why computer companies can afford to upgrade existing architectures with arrays.

### Different markets

There are many different types of master-slice chips, and it is incorrect to treat them as though they were all competing for the same sockets. For the most part, the devices in the following categories address entirely different markets:

- Linear master slices. Built with standard, diffusion-isolated bipolar processes, these small chips are used to integrate amplifiers, oscillators, and other analog functions. CAD is not used to prepare these devices, nor is it really appropriate.
- Medium- and high-speed digital gate arrays. Technologies here include n-channel MOS, complementary-MOS, integrated injection logic (and its derivatives), and TTL, usually Schottky-clamped.
- Very high-speed emitter-coupled- and current-mode-logic arrays. With gate delays often below 1 nanosecond, these arrays are almost exclusively intended for mainframes and large minicomputers.

One reason why these products are confused is that



**2. Linear master slice.** This is not a gate array. In place of gates, this analog semicustom chip from Exar Integrated Systems Inc. has uncommitted bipolar transistors, diodes, and resistors. They are wired to form amplifiers, oscillators, filters, and so on.

some overlap does exist. For instance, there are arrays combining analog and digital circuitry; Exar Integrated Systems Inc., Sunnyvale, Calif., offers an I²L array called the XR-400 that has 57 linear transistors and 256 digital gates. Similarly, the C-MOS arrays, though considered digital, can also be connected to form operational amplifiers, comparators, voltage references, and so on.

In addition, some market overlap does exist between the high-speed C-MOS and Schottky bipolar arrays and the emitter-coupled-logic arrays. Although ECL can dip below 1 ns, the oxide-isolated process—which in part allows such speeds—has also been applied to silicon-gate C-MOS and non-ECL bipolar processes to achieve gate delays well below 10 ns. Figure 1 plots gate delay versus gate complexity for some of the currently available digital arrays.

### Linear arrays

At present, the perceived leader in analog master slices is Interdesign Inc., a Sunnyvale company acquired by Ferranti Ltd. in 1977 (see "Ferranti: the British array pioneer," p. 151). Interdesign is also the leader in diversity of technologies. After its bipolar master slices—which it calls Monochips—were introduced in 1972, it went on to offer an n-channel MOS gate array in 1977 and C-MOS arrays in 1978. In 1978 it also began marketing Ferranti's bipolar gate arrays and this year it took on Ferranti's high-speed current-mode-logic arrays.

Interdesign stocks 10 linear Monochips. Seven of them are also available from Exar, and two of them from Cherry Semiconductor Corp., Cranston, R. I.

These linear arrays contain npn and pnp transistors, diodes, and diffused and higher-value pinch resistors built with standard junction-isolated bipolar technology (see Fig. 2). Development starts with breadboarding of

## Who's Charlie Allen?

When the metal-gate complementary-MOS arrays designed in California's Silicon Valley are appraised, the apparent similarity of the designs is striking. One reason is that many were designed by Charlie Allen. So who's Charlie Allen?

Charles A. Allen is president of a small Sunnyvale, Calif., gate array supplier, Master Logic Corp. The metal-gate C-MOS arrays offered by International Microcircuits Inc. (IMI) of nearby Santa Clara bear a family resemblance to his arrays, because he was one of the founders of IMI. The C-MOS arrays of Interdesign Inc. of Sunnyvale and Heuer Microtechnique AG of Brugg, Switzerland, are identical to his, because he has license agreements with both firms. He is currently concluding agreements with other potential suppliers, including Monosil Inc. of Santa Clara, Exar Integrated Systems Inc. of Sunnyvale, Nitron Inc. of Cupertino, Calif., and Eurosil of Munich, West Germany.

**Standardization.** Some of these companies will be fabricating identical wafers, whereas some will purchase their preprocessed wafers from common silicon wafer foundries, like Semi Processes Inc. of Santa Clara and Supertex of Sunnyvale.

Asked if he is helping his competition by licensing arrays of his design to potential competitors, Allen says: "No, I'm trying to create a viable industry out of the gate array concept. There is no advantage to a proprietary array, because the large customers demand a second source. And without these large customers, we will remain a cottage industry."

Prior to his involvement in the gate array business, Allen was employed by Cogar Corp. in upstate New York along with Frank Deverse and Robert Lipp. When Cogar Corp. folded, Allen and his cohorts landed in Silicon Valley in 1972. "We saw what Interdesign had done in linear arrays and decided to do something similar in digital MOS," recalls Allen. Deverse continued on as president of IMI, and Lipp formed California Devices, another small C-MOS gate array supplier in Santa Clara.

Allen has recently completed the design of mask sets for 500- and 1,000-gate arrays to be manufactured by SPI. Deverse and Lipp are hotly contesting the market with arrays of their own. Allen believes this battle will be decided on the basis of consistent, reliable wafer supply, and he is betting on SPI.

Allen thinks that these dense, fast Iso-CMOS arrays will finally be successful in capturing the attention of the computer companies. "They have the resources to finance the software for automatic gate placement, wire routing, and test pattern generation," Allen says. "We need a total package like that to make this industry really expand. I believe that such programs will become available early next year."

the circuit by the customer, preferably with parts supplied by the manufacturer to insure compatibility with chip components. Next the user pencils in the design on a layout sheet supplied by the chip maker, who then uses this to tape together the single metal mask used for customization. The design cycle lasts from 6 to 18 weeks and tooling charges range to $5,000.

### Digital slices

Many gate-array manufacturers prefer C-MOS. But there are really not that many different C-MOS arrays. Several companies have licensed the metal-gate arrays designed by Charles A. Allen, now president of his own gate-array design shop, Master Logic Corp. of Sunnyvale, Calif. (see "Who's Charlie Allen?" at left).

The cells in most C-MOS arrays are characterized by two or three n-channel MOS field-effect transistors—connected in series—adjacent to two or three p-channel counterparts, also in series. Between the rows of transistors are diffused $p^+$ underpasses with contact openings at their ends; some also have an additional contact opening near their center.

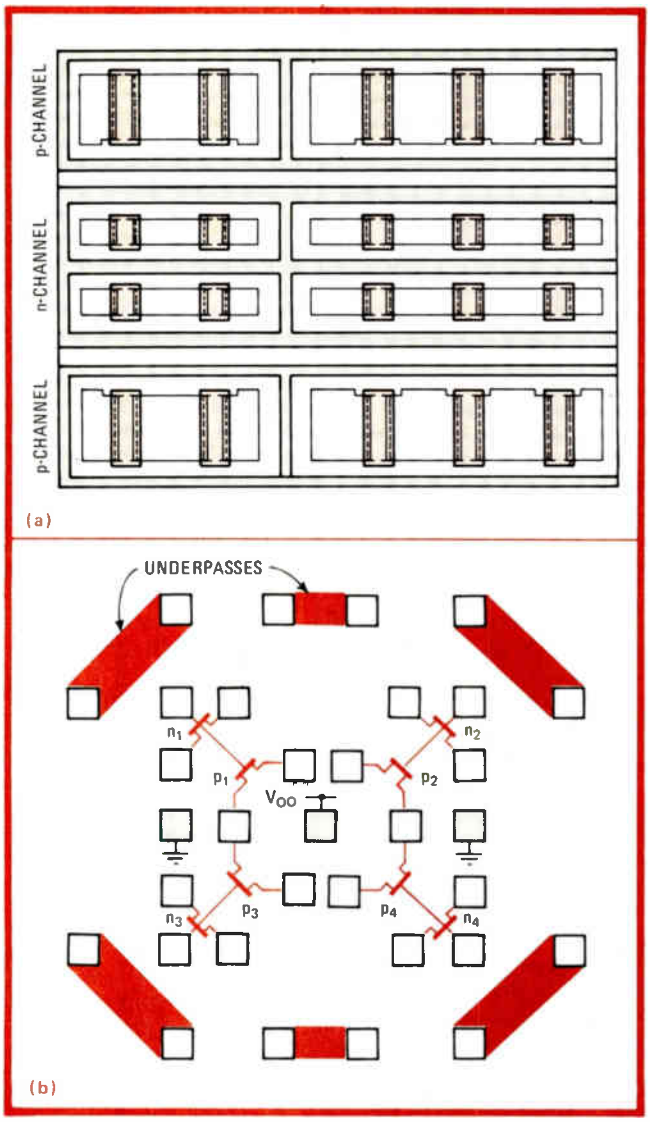
The bulk of those companies using metal gates will probably go on to offer faster, denser, oxide-isolated silicon-gate C-MOS arrays with cells similarly arranged. International Microcircuits already has the jump on the competition with its Iso-CMOS parts [*Electronics*, July 3, 1980, p. 119]. The silicon foundries now supplying these companies with wafers will also turn around and offer arrays themselves. Supertex Inc., for instance, will become an alternative source of IMI's Iso-CMOS arrays. This second source is important for IMI, since Allen has sold a design of an incompatible dielectrically isolated array to Semi Processes Inc., Santa Clara, Calif. [*Electronics*, Sept. 11, 1980, p. 33].

IMI will beef up its product line later this year with a 5,000-gate array exhibiting gate delays below 3 ns. To meet this goal of speed and density, IMI will move from 5-micrometer design rules to 4 $\mu$m, and it will employ a double-level metalization system. Double metal will allow IMI to scrap the diffused underpasses to shrink the array and improve performance.

Although double-metal interconnection is common among bipolar circuits—indeed, some medium-scale integrated TTL chips use it—such a technique for MOS is relatively untried. So IMI will probably adopt an approach that appears to be working for IBM: sputtering the insulating oxide rather than growing or reflowing at high temperature.

Again, these C-MOS arrays are basically wired by hand. The companies do, however, keep libraries of overlays on hand for common functions such as flip-flops, exclusive-OR gates, and so on. These overlays, which the companies refer to as "pasties," are nothing more than self-adhering decals containing an optimized metalization pattern for the function or gate of interest, which the chip maker sticks on the layout sheet before photoreduction.

International Microcircuits is one company migrating in the direction of CAD. Its arrays are digitized, and the user places and interconnects the gates using a cathode-ray tube, albeit still by hand. However, the mere digiti-



**3. C-MOS cells.** A cell from a C-MOS array built by Applied Micro Circuits Corp. is shown in (a). Its rows of n- and p-channel devices typify metal-gate C-MOS chips. Racal's silicon-gate C-MOS cell (b) is claimed to have layout efficiencies up to 90%.

zation of the array is a step in the right direction. IMI can call up its macros from a data base, saving paper work, and it can take advantage of the printed-circuit-board wiring algorithms that are available for the Calma and Applicon graphics machines that it is using.

"I can't understand why the other guys aren't doing it this way," states IMI's Kroeger. "Most of the people we know are doing it [laying out their arrays] by hand. You can't really go beyond 400 or 500 gates that way," he says. IMI's densest array, for which it has contracted six designs thus far, contains 2,000 gates.

## Others' arrays

An oxide-isolated C-MOS array that invites CAD is the 288-gate chip designed by the Hughes Aircraft Co.'s Industrial Electronics group in Newport Beach, Calif., for internal use. Hughes has left space between the bonding pads on two sides of the chip for a shrink to 3-$\mu$m geometries and about 1,100 equivalent gates. Hughes has also put some arrays on sapphire, as has RCA Corp.'s Solid State division in Somerville, N. J.

RCA will describe one of its C-MOS-on-sapphire arrays next month at the first international conference on circuits and computers [*Electronics*, Aug. 14, 1980, p. 96]. The paper's authors, from RCA's Camden, N. J., facility, will present an 840-gate master slice that they call an automated universal array because customization is handled entirely by an automatic placement and routing program. So competent is the software that utilization of internal gates exceeds 90%, the authors claim. RCA has also designed metal-gate and silicon-gate C-MOS arrays with complexities of 200 to 1,000 gates.

In Hughes' array, the ratio of routing channels to gates is higher than in older C-MOS arrays like the early ones designed by Allen. Hughes also staggers the polysilicon underpasses so that their ends are between cell connecting points. This allows interconnections to get by with two feedthroughs compared with the three needed in other C-MOS arrays.

In addition to the metal mask, Hughes also customizes the metal-to-polysilicon contact-via mask. This allows metal paths to be routed perpendicularly over the underpasses the entire length of the chip. (In designs that customize only with the metal mask, not all of channel metalization can run this far before being interrupted by a precut via.) Customizing with the contact mask also allows Hughes to run metal right over unused cells.

## Dedicated cells

Hughes has also added some dedicated flip-flops to its array. Some designers do not believe in this approach, saying that it cuts down on the generality of the matrix. On the other hand, if the flip-flops are needed, packing density is much more efficient. Interdesign has also added flip-flops to one of its arrays, the MCD Monochip.

Western Digital Corp. of Newport Beach, Calif., specializes in a new n-MOS array. The 20-pin chip, which Western Digital only uses internally for such designs as its Pascal MicroEngine board computer [*Electronics*, Oct. 12, 1978, p. 155] contains 32 2-input NOR gates, 16 2-input NAND gates, 4 3-input NAND gates, 9 D-type flip-flops, 7 drivers, and a dynamic 4-bit binary synchronous up-down counter. A logic diagram, drawn on a layout sheet created by Western Digital, is digitized and an Applicon system generates the contact-via and metalization masks. The company has completed only two codings so far and is working on a third for an upcoming multiuser version of the MicroEngine.

Taking the hardwiring idea the farthest is Applied Micro Circuits Corp., a San Diego, Calif., company formed last year by Howard Bobb and Joe Mingione, both from American Microsystems Inc. Its Q400 Quickchip, now in development, has a functional equivalent density of 1,500 C-MOS gates, but the die is partitioned into four quadrants, three with digital cells and one with linear C-MOS components. Other devices in the Quickchip family will feature different combinations of analog and digital quadrants.

Each analog quadrant on the chip will contain the following resources:

- 4 internally compensated operational amplifiers.

## Computer makers push European arrays

European designers of computers, leading-edge telecommunications gear, and complex test instruments do not have to look very far from home for their logic arrays. Some of the fastest arrays on the market turn up in the catalogs of European semiconductor houses, and the variety is impressive. Ferranti alone boasts 17 types.

So far, the demand for master slices has primarily been generated by native mainframe computer makers; CII Honeywell Bull (CII-HB) in France, International Computers Ltd. (ICL) in the UK, and Siemens AG in West Germany. All three have opted for emitter-coupled logic and high density so that time is not wasted along the relatively long interconnection paths between large numbers of integrated-circuit packages.

The European gate-array market is just now starting to blossom. The first computers to have ECL arrays—upgraded models in Siemens' 7500 series—will wind up in the hands of end users next year. Fritz Gütter, product marketing manager for computer ICs at Siemens, warns that in-house suppliers make the size of the gate array market hard to peg; nonetheless, he guesses that the world market for arrays runs "at a seven-digit figure for unit production with annual growth at a two-digit figure." The pace in Europe should not lag behind.

**Untapped.** Though the market in Europe remains relatively untapped, the potential is there, according to Michel Blanchard, international marketing manager of ECL products for RTC-La Radiotechnique-Compélec, the French semiconductor house of the Philips Gloeilampenfabrieken group. He puts the world market for 100000-family ECL LSI circuits at roughly $5 million for 1980, predicting that it will more than double again in 1981.

Because the performance of their next-generation machines depends in large part on how clever they are with large-scale integration, none of the three companies dares leave its array circuit development to a lone semiconductor supplier. Siemens is a major semiconductor supplier as well as a mainframe maker so there exists an in-house partnership.

CII-HB worked closely with RTC to develop cell arrays with current-mode logic (CML), a low-power implementation of ECL. And ICL already has a small pilot production unit to turn around logic arrays in a hurry.

CII-HB has long had the computer-aided know-how to conceive large-scale CML circuits. Jack Petersen, a general director of the company, says it may one day fit itself out with production metalization equipment and "a fast turnaround facility" to truncate customization time. The decision has yet to be made, but the investment would be a heavy one, suggests Petersen.

The ECL at ICL is compatible with 10000-family logic and the arrays pack in as many as 400 triple-level-metal gates in a 64-pin package. ICL's circuit designers can call up functions from a library of some 50 different cells. This library also includes test patterns for each cell that can be used in simulations. Interconnections between cells are basically laid out by hand, though some computer-aided-design routings are available to speed up layouts and to spot logic-level mismatches.

With its pilot unit, ICL can get a mask-pattern tape about two weeks after it has spelled out the chip's specifications. Samples appear after another four weeks unless there is a real rush for the part; when there is, an express route trims the turnaround time to one week. Fast turnaround, as well as simulation to check out logic designs, is essential for LSI design, ICL believes.

**Speedy.** The ribbon for European arrays should be awarded for the 24- and 36-cell ECL chips having 0.5-nanosecond internal gate delays developed by Siemens and second-sourced by RTC. "The technology is different," says RTC's Blanchard, "but otherwise theirs and ours are the same. The metalization masks are interchangeable." What is more, a third source—in the United States—looks likely, Blanchard hints.

Siemens calls its chips SH100B/type 0 for the 24-cell version and type 1 for the 36-cell part; the nomenclature at RTC is MLA 24 and 36. Either way, the logic cells contain 42 transistors and 16 resistors. In addition to the basic 24 or 36 cells, there are 30 or 42 input cells and 38 output cells.

For practical purposes, this adds up to a possible complexity of 500 maximum equivalent gates on the 28-square-millimeter 24-cell chip and 800 maximum on the 36-mm² 36-cell chip. Both are packaged in 64-pin flat packages or 68-pin leadless carriers. The cell library at RTC includes some 40 basic circuits and about 20 input/output cells. Typical power consumption for the smaller chip is 1.8 watts and for the larger one, 2.3 W. Metalization is aluminum on two levels.

Siemens actually still has a third version of its 100000-family-compatible ECL cell array. The SH100B/type 2 incorporates a 4-by-32-bit random-access memory on the chip (see photograph). Another array in the Siemens lineup is an integrated-injection-logic part, the S340B, with a longer internal gate delay—typically 15 ns—but very low power consumption, just 15 microwatts per gate. This is a 30-mm² chip with some 2,600 components.

The last part in the firm's arsenal of bipolar arrays is a 1,000-gate TTL-compatible master slice, the SH4B. With a 1-ns internal gate delay it is the fastest in its class, Siemens' Gütter maintains. The device sports a power dissipation of 0.6 milliwatt per gate, needs only a single 5-V supply, and integrates 3,100 components on a 36.6-mm² chip. Its high speed—faster than Schottky, Siemens says—makes the chip just right for fast bit-slice computers. Production starts next year.

RTC has additional array chips in mind though it just got into production of the MLA 24 and MLA 36 this spring. Blanchard says the market seems to need a 2,000-gate chip with some 100 input/output pads. The gate propagation delay should run about 0.3 or 0.4 ns and the power dissipation, less than 8 W. The chip size would be something like 40 mm². The main problem for such a chip, in Blanchard's view, is designing a package with so many I/O pads.

There is a market for smaller fast arrays, too, figures

- 1 comparator.
- 2 programmable logic arrays.
- 8 40-kilohm resistors tapped every 5 kΩ.
- 105 0.75-picofarad capacitors.
- 15 bipolar npn transistors (with collectors grounded).
- 11 diodes.
- 3 zener diodes.
- 14 single-pole, double-throw transmission gates.

Plessey Ltd., a UK heavyweight in telecommunications gear. The company will go to market soon with 0.5-ns ECL dual quad-input gates and a dual flip-flop intended to fill in where large uncommitted arrays are underutilized or too slow. Plessey will follow up these parts with 100- and 300-gate ULAs with 0.5-ns internal gate delays.

Ferranti Ltd., first to market with ULAs in the UK, faces increasingly heavy competition at home in the form of C-MOS gate arrays based on the dielectrically isolated process—Iso-CMOS—championed by Mitel Semiconductor Inc. of Ottawa, Canada.

Racal Microelectronic Systems Ltd. now sells two arrays with 448 and 880 two-input gates, respectively (see p. 153). Before year end, Smiths Industries Ltd. in Cheltenham will offer an array with 2,000 equivalent gates, to be available in 64-, 48-, and 180-pin versions. Chip sizes will range from 250 to 180 mils (6.35 to 4.57 mm) on a side using 4- to 5-$\mu$m geometries.

By 1982, the company will introduce a ULA with 5,000 equivalent gates. Ian Pierson, who heads up Smiths' Microelectronics division, will not say whether each cell will contain an array of components or a prewired gate, however. The gate arrays will be backed by a custom layout service so that proven array designs can be further reduced in size with little additional effort for high-volume production runs.

Both Racal and Smiths will stockpile prediffused wafers from Mitel and do the final metalization and testing themselves. General Electric Co. Ltd. (GEC) and Plessey, however, plan to produce their own wafers under license from Mitel. GEC already builds a ULA using a C-MOS-on-sapphire process. The part has 512 AND and OR cells on a chip measuring 5.4 by 5.7 mm. The typical delay per cell is 10 ns at 5 V, and 5 ns at 10 V.

**Pilot facility.** British Telecom, the telecommunications wing of the British Post Office, will also set up an Iso-CMOS pilot production unit at its Martlesham facility. Semicustom circuits based on ULAs—and possibly standard cell custom circuits—will be used extensively in the Mark II version of System X, Britain's all-digital main phone exchange program, and in other telecommunications gear.

"The uncommitted logic array is a natural method of exploiting the power of Iso-CMOS technology," says Bill Holt, manager of the integrated circuit division at Plessey's Allen Clark Research Center in Caswell.

A novel twist to the gate array concept is being developed by S. L. Hurst of the School of Electrical Engineering at Bath University. He has come up with the concept of a universal logic gate. With appropriate input connections, it will perform a range of logic functions, unlike AND/NAND gates which can only perform their designated function.

Custom designer Silicon Microsystems Ltd. in Malmesbury plans to launch a ULA based on the concept next year along with a more conventional ULA using second-generation C-MOS technology. It claims that chip utilization with the universal gate will be one to two times better than with ordinary gates. **-*Electronics* European staff**

- 2 current generators.
- 1 4:1 p-channel current mirror.
- 8 input/output pads with optional input protection.

Each digital quadrant holds 24 basic digital cells, each

## Ferranti: the British array pioneer

Ferranti Semiconductors was one of the world's first semiconductor companies to recognize the commercial potential of the uncommitted logic array: it introduced its first 187-cell ULA in 1973. Buying the Sunnyvale, Calif., custom integrated-circuit design house Interdesign in 1978, Ferranti launched the product in the United States alongside Interdesign's complementary Monochip array system for linear circuit designs.

The company has broadened its product portfolio to include 17 different arrays, blanketing the performance and applications spectrum. The family now extends from small 100-gate arrays with excellent linear capability to 2,000-gate chips having a 20-megahertz clock rate and excellent interfacing capability. The product line also includes low-power versions with a 0.4-microwatt dissipation per gate.

**Dense and fast.** Ferranti's ULAs exploit its collector-diffused-isolation bipolar technology, a derivative of the process developed by Bell Laboratories back in the 1960s. CDI, says Ferranti, has attributes that render it ideal for ULA applications. Its simple five-mask process offers the functional density of MOS and the speed advantages of bipolar. Further, the ability to distribute power within bulk silicon enables the power rails to be removed from the top interconnection plane, so customization is carried out in the final masking stage. The highly doped collector-isolation diffusion is of sufficiently low resistivity to enable supply connections to be made without metal, and the p-type epitaxial layer on a p-type substrate makes direct ground connections possible.

When Ferranti first capitalized on CDI in 1972, few technologies could offer the same combination of features, but now integrated injection logic and dielectrically isolated complementary-MOS processes threaten Ferranti's total available market. In response, the Lancashire-based company is moving from 4- to 3-micrometer features and a washed-emitter process.

The Ferranti group is now readying a 990-cell array having a 2,000-gate complexity and a gate delay of 6 nanoseconds. This gives a power-delay product of 0.5 picojoule, since it operates from a single 5-volt supply. The 64-pin ULA1D000 array is scheduled for production in 1981. The array, less than 200 mils square, promises high yields, says the company.

**Hints.** The 3-$\mu$m CDI process has also been applied to 256-cell power arrays that operate on a typical current of 200 microamperes from a supply voltage of between 1.0 and 5.5 V. That still cannot quite match upcoming high-density Iso-CMOS processes but, points out Alan Williamson, product marketing manager of ICs at Ferranti, such processes require many more masking stages. "We are very mindful of the situation," he says, hinting at a new process that Ferranti has in the works. This might be a derivative of CDI, perhaps with pinch-off field-effect-transistor load resistors or other MOS features, or it could be a new C-MOS process.

In all recent arrays Ferranti uses the same cell structure comprising five transistors (one of which is used as a dual current source), three resistors, and three crossunders. These components can be configured to form two two-input current-mode-logic gates. This compact gate structure was first used in the company's F100-L 16-bit microprocessor. A specially designed interface cell accompanies each bonding pad of the array. **-Kevin Smith** containing 10 n-channel and 10 p-channel devices (see Fig. 3a), 10 static D-type flip-flops, and 19 I/O pads with the following options: input protection, pull-up or pull-down resistors, three-state output, latching and multiplexing for liquid-crystal display driving, or bidirectional circuitry for interfacing to two-way buses.

In addition to the devices in the analog and digital sections, AMCC's C-MOS Quickchip contains an on-chip crystal oscillator, 2 18-state dynamic shift registers with a nonoverlapping clock generator, 4 high-current (28-milliampere) n-channel drivers, 8 high-current (8-mA) p-channel drivers, 8 voltage-level shifters, 4 dynamic D-type flip-flops, and 8 high-impedance resistors.

### Shift registers for testing

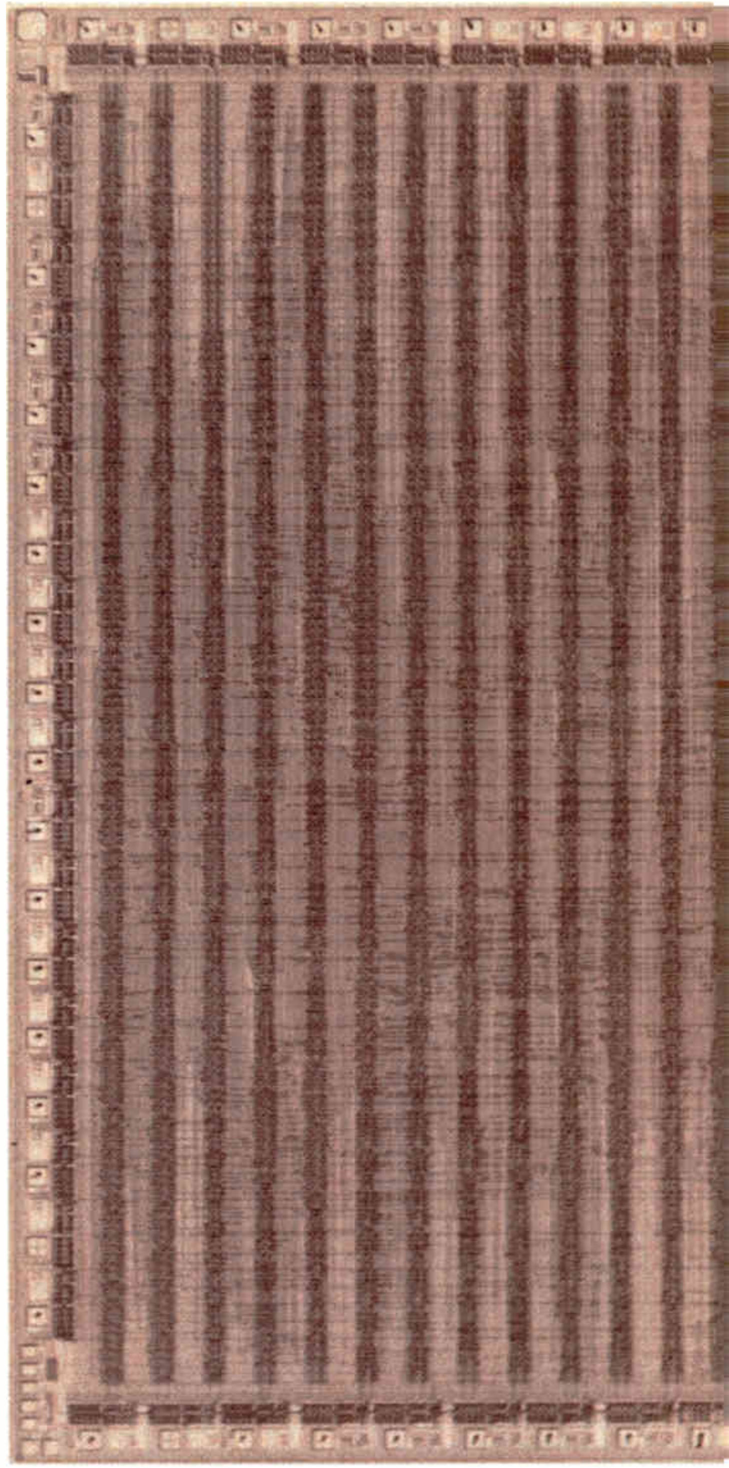
"It's like a designer's tool kit," smiles Dan Yoder Sr., AMCC's vice president of sales. Although the dynamic shift registers on the chip can be for any purpose intended by the user, AMCC really added them to enhance testing—a growing bottleneck in most array designs. Although test points have to be wired to the shift registers, once attached, the signals can be shifted out in serial fashion. Hughes says that its larger future array "will very likely have shift registers for testing." The idea of serializing test information in this way is not new, having being implemented by IBM for the gate arrays and boards in recent computers like its System/38. IBM calls this level-sensitive scan design, or LSSD [*Electronics*, March 15, 1979, p. 108].

Another company now getting into the C-MOS gate array business is American Microsystems Inc. of Santa Clara, Calif. It has six oxide-isolated arrays with densities ranging from 300 to 1,260 equivalent gates in the advanced development stage. AMI is also building up a library of functional overlays for complex gates, flip-flops, and so on. It even has an overlay for a 4-bit binary-coded decimal counter that consumes 27 gates.

AMI already has a lot of software in place for its custom business that it can fall back on for its gate arrays. This software is currently partitioned into a front end that produces a validated logic diagram, an intermediate stage for placement and routing, and a back end for mask generation that goes by the acronym SIDS, for symbolic interactive design system.

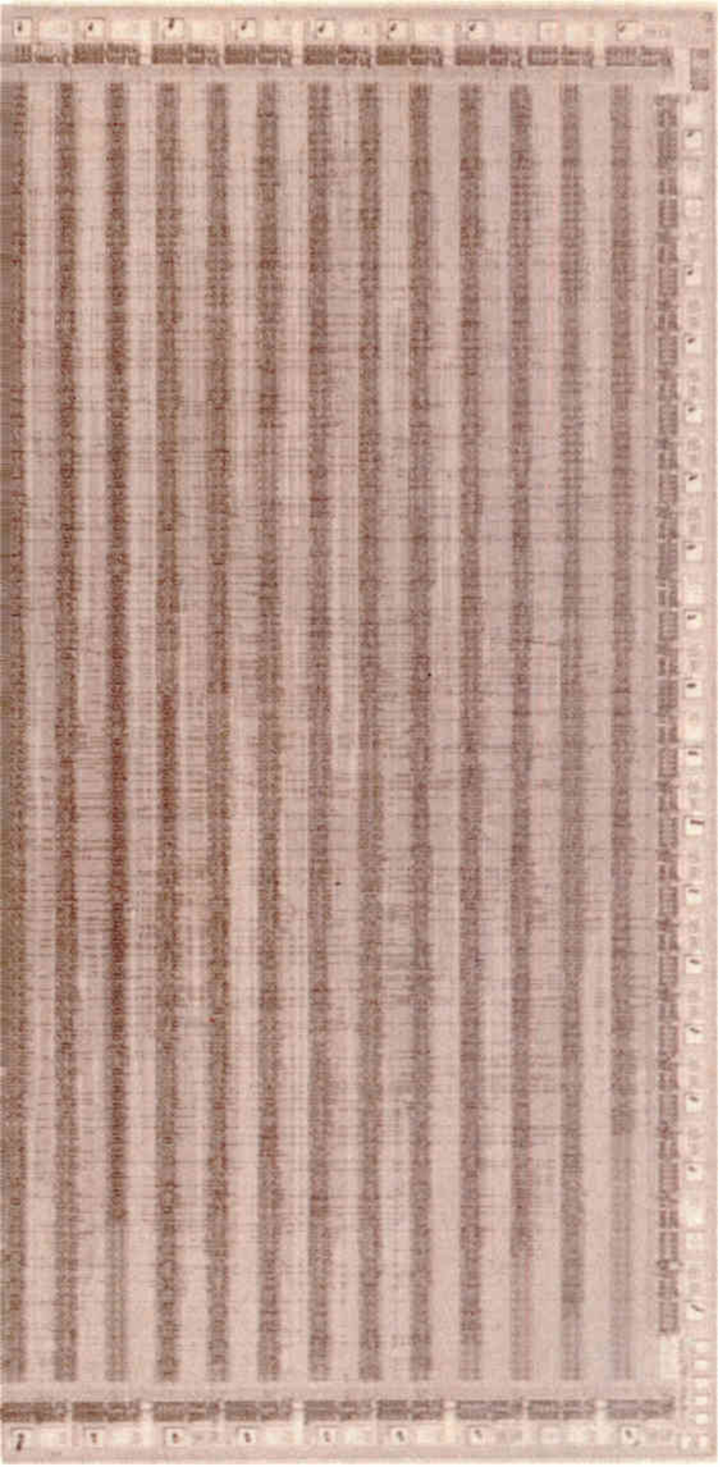
The software liaison between logic simulation and mask generation contains a set of routines called layout planning aids, or LPAs, comments Bruce Bourbon, AMI's department manager of technical information services. "LPA uses interactive placement and routing to create a topological plan that is then used in the mask design," he explains. It is here, in LPA, that provisions will be incorporated for gate arrays. "There will be two versions of the software, with gate arrays being the special case," says Bourbon.

AMI also sees the need for automatic test-vector generation for its custom and semicustom logic. It is evaluating a program called Lasar, which Bourbon believes was originally developed under Department of Defense sponsorship. "The early versions were terrifically expensive because they take all the logic and transform it into NAND equivalents. Then forward and backward tracing techniques are used to generate the [test] vectors."

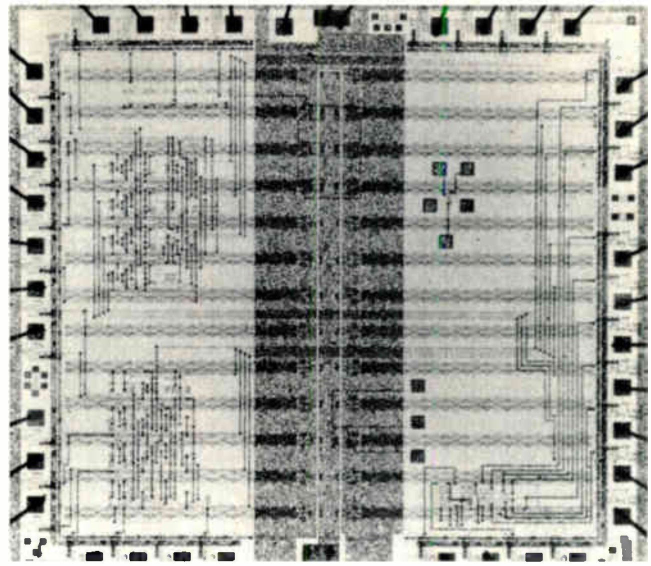


Bourbon mentions that Teradyne Inc. of Boston acquired Lasar and recently got it up and running on a Digital Equipment Corp. VAX minicomputer system. "We're evaluating the claim that the run time has been substantially improved." There is some question as to how efficiently it handles bidirectional transfer gates, a logical circuit element peculiar to MOS. "It looks like it explodes them into a fair number of NAND equivalents to get a decent simulation and fault model," says Bourbon.

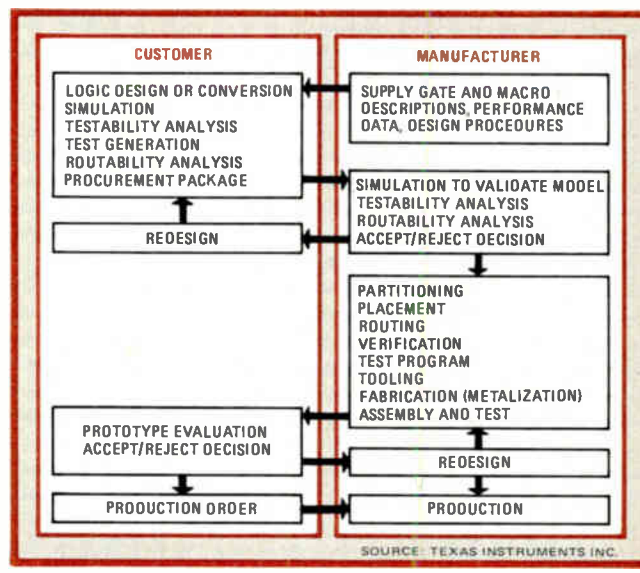
All of the C-MOS arrays discussed thus far are based on rows of transistor pairs. Racal Microelectronic Sys-



**4. Huge.** This state-of-the-art 3,900-gate C-MOS gate array from Fujitsu Ltd. hints at where things are headed for that technology. This is the largest C-MOS array offered commercially thus far, though International Microcircuits Inc. promises an even denser chip.



**5. Go-between.** Between moderate-speed C-MOS and super-fast ECL is a host of chips made with TTL, integrated injection logic and various Schottky processes. This 1,200-gate integrated Schottky logic chip from Signetics contains an evaluation circuit.




**6. Info flow.** TI's gate array design utility software illustrates what a complex package of routines should contain. In time, some of the programs on the right may be given to the customer, while some of the responsibilities now on the left may be taken on by TI.

tems Ltd., Reading, Berks., England, uses the unique cell shown in Fig. 3b (see also "Computer makers push European arrays," p. 150). Although wiring efficiencies with parallel lines of devices are only around 75%, says Racal, its layout allows connection efficiencies approaching 90%.

Racal reasons that C-MOS devices are invariably used in pairs so the four n- and p-channel pairs in its cells can share a common polysilicon gate. Power-supply connections are brought up from the substrate so they need not be wired. Six cross-unders are provided that allow two metal tracks to pass parallel to the side of a cell and three tracks to emerge from each corner at an angle. The cell is designed on a grid with a metal pitch equal to 4.8 μm. (Pitch is the width of a line plus the width of the spacing to the next line, divided by 2.) This allows easier layout without a knowledge of design rules. Racal configures cells both manually, with overlay decals, and automatically, with cells stored in a CAD library.

As for density, the biggest C-MOS chip to be offered thus far is the 3,900-gate job shown in Fig. 4. The array

## Japanese build for themselves

Fujitsu Ltd. is the only major Japanese semiconductor company now aggressively selling semiconductor gate arrays. It is supplying devices that cover all but the fastest applications; its complementary-MOS devices with up to 3,900 gates have an average propagation delay of 7 nanoseconds; its TTL devices with up to 500 gates have an average propagation delay of only 1.8 ns. Fujitsu also has emitter-coupled-logic gate arrays that it uses in its largest computers and communications equipment.

**Families.** Nippon Electric Co. of Tokyo has three families of ECL gate arrays, two of which it developed jointly with the Musashino Electric Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. One of these, developed for use in telephone exchanges, is sold to a limited number of outside customers, including Takeda Riken [*Electronics*, Feb. 3, 1977, p. 2E or 66, and Oct. 11, 1979, p. 46]. Japan's other electronics exchange suppliers—Fujitsu, Hitachi Ltd., and Oki Electric Industry Co.—also produce functionally equivalent versions of the 200-gate device. The other jointly developed array, with 1,200 gates, is used in NEC's medium-sized computers and is not made by the other three firms. NEC is willing to supply it to others but does not expect many takers because of the nonstandard power supply voltage of −3.3 volts, used to hold down power consumption [*Electronics*, Aug. 30, 1979, p. 63].

Hitachi Ltd. has ECL devices with 550 gates and TTL devices with 500 gates, both of which are used in house. The ECL devices were designed to be compatible with Fairchild F100 devices to enable company engineers to easily use both standard and custom devices in the same computer. The TTL devices are said to have performance similar to Fujitsu's 1.8-ns type.

Mitsubishi Electric Corp. has for two years been using gate arrays with diffusion self-aligned (DSA) MOS as a replacement for entire boards of low-power Schottky TTL [*Electronics*, Oct. 12, 1978, p. 67]. When the company first announced the devices it said it had great hope of selling the devices to a wide variety of customers and that it would provide quick turnaround through CAD layout and test-pattern generation. Since then the company appears to have pulled back from the market and is using them mainly in house.

Mitsumasa Ashida, manager of the custom IC engineering department at Fujitsu, says that industrial users will use gate arrays wherever possible for most requirements. They are not suitable, though, where it is necessary to get the highest possible performance from the technology, where memory is included, where there are very special requirements, or where the amount of logic is huge. Furthermore, VLSI will continue to be custom, he predicts.

Fujitsu's C-MOS gate array family comes in four versions with gate densities of 3,900, 2,000, 1,275, and 770. The largest chip is 9.7 millimeters square; the next largest is 7.2 mm². But because of the space that must be provided for wiring channels, only about 30% of the chip is utilized for transistors. The average delay per gate is 7 ns, though this varies widely depending on fanout. Average power dissipation for the largest chip is about 50 milliwatts in data-processing applications and around 100 mW in high-speed communications applications, where shift registers and the like draw power by running constantly. If the devices were implemented in n-channel MOS the dissipation would be at least 1.0 to 1.1 watts and the speed would have to be limited to keep power use down. With C-MOS technology it is not necessary to worry about power dissipation.

Fujitsu's p-well C-MOS process uses 3.6-micrometer patterning. It is essentially one step behind the processes used for memories, but this is the best course for random logic. For memories it is possible to redo a design many times, changing it for best performance and yield. But with random logic there are many components connected in various configurations and a fairly large margin is needed. The largest devices have 72 bonding pads, even though they are mounted in 64-pin packages.

The basic cells, all 3,900 of them, contain two p-channel MOS transistors and two n-MOS transistors that can be connected as a two-input NAND or two-input NOR gate. The peripheral cells contain sufficient elements for connection as a three-state input/output buffer or as simple input or output gate only. Because the propagation time of C-MOS is affected by fanout and wiring capacity, CAD is needed to manage variations in delay time as well as to lay out the wiring of the chips. Although it is possible to utilize much more than 90% of the internal cells, attempts to use higher ratios might result in a lack of wiring routes.

**Library.** A standard library for these devices includes 66 types of internal logic blocks and 5 types of I/O functions. Fujitsu requires from its customers a logic drawing and test data. The first CAD task is to check that these documents match. Delivery of engineering samples is approximately 14 weeks after design validation. Fabrication includes four custom masks—contact, first aluminum, vias, and second aluminum. The mask that opens windows on the bonding windows after glass passivation is standard. Fujitsu says that the 3,900-gate devices are economic in lots of 500 or more, and the smaller devices become reasonable in lots of 1,000 or more.

In bipolar, Fujitsu makes a low-power Schottky chip with 208 internal three-input NAND gates and 26 input/output buffers that can be encapsulated in any standard 16- to 28-pin dual in-line package. The internal gates have a propagation delay of about 6 ns and consume less than 2 milliwatts each. Although this is a relatively simple design with a small number of gates, it can replace about 30 small-scale integrated TTL packages. Use of washed

comes from Fujitsu (see "Japanese build for themselves," above).

Various bipolar technologies are being tried for gate arrays. Integrated injection logic in one form or another is being used by Exar, Harris, Signetics, Texas Instruments, and Fairchild. Although $I^2L$ can achieve power-delay products comparable to C-MOS, C-MOS gate array manufacturers criticize $I^2L$ on two grounds. One is that too few companies are pushing the technology, and of those that are, each uses a different version. Another complaint is that if the gates do not have enough outputs, they are hard to wire. "If you only have two outputs and you need eight, you have to add three more gates," says Hughes' W. E. Armstrong, assistant manager of operations in its Solid-State Products division.

But the firms choosing $I^2L$ cite its excellent packing emitters and other advanced processing help keep speed high while operating at low power. Typical input to the 2.6-by-3.27-mm chip is 500 mW.

The library includes 50 types of cells. Like the C-MOS devices, the customer need only supply a logic diagram and test pattern. Turnaround time on a design is usually only 8 to 10 weeks after confirming that the logic and test pattern match. This device differs from the C-MOS devices in that it does not require a contact mask—only three masks are required.

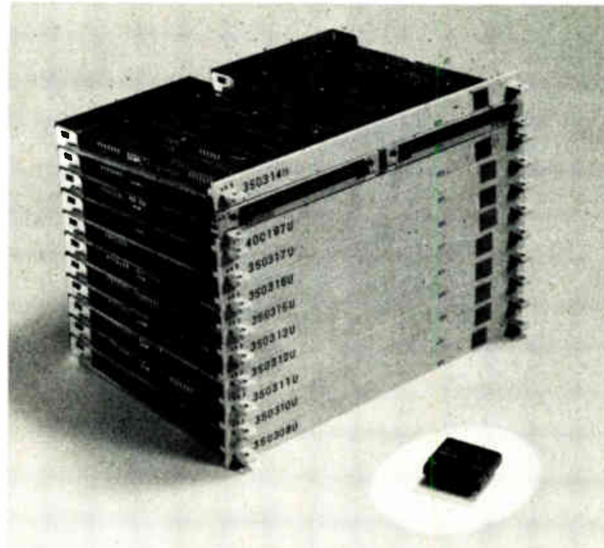
**Three masks.** Fujitsu also has a high-speed bipolar chip with 512 two-input NAND gates, 60 input buffers, and 48 output buffers. The advanced Schottky low-power design provides high performance; internal gates have a propagation delay of 1.8 ns per gate at a power dissipation of 2.3 mW. Typical input to this 4.9-by-5.1-mm chip is 800 mW, 1.2 watts maximum. Either a 42-pin DIP or a 64-pin square package can be used. The same type of documentation as is used for the 200-gate devices suffices and only three masks need be generated, but turnaround time is still 10 to 12 weeks.

Nippon Electric's first gate-array product was a set of 4 emitter-coupled-logic chips whose development started in 1973, with the largest chip having 200 gates. About 40 different devices have been built using the same four basic chips. CAD is not practical with these chips because wiring channel areas are too small, wide metal lines are used to carry high currents, and power supply and ground connections are not standardized.

At Hitachi the computer group has its device development center right in the firm's main semiconductor plant. Yuichiro Oya, department manager of the device development center, says that for the past several years there has been almost no custom bipolar work done—it is either standard devices or gate arrays. The complexity and the large number of masks required for bipolar devices, together with the generally short production runs, mean that custom bipolar devices represent too great a loss of manpower. (MOS is something else because there are fewer masks and quantities are huge.)

Oya further says that there is no hurry in starting to sell gate arrays to customers outside of Hitachi because he does not see much business coming from Japanese companies. Large-scale demand would normally be for computer applications, but all major Japanese computer manufacturers have their own semiconductor operations. Thus volume sales would have to be directed overseas.

Surprisingly, Oya says that in these devices there is more loss of yield in the wiring than in the diffusion. He says that in bipolar devices the minimum dimension of 3 micrometers is only used for the emitters, which are small and only take up a small percentage of the area of the chip. But the connections, with similar dimensions, are long and run parallel to each other. He also says that an electron-beam pattern generator is used for fast turnaround time.



**Consolidator.** The 3,900-gate complementary-MOS array from Fujitsu (see Fig. 4) is shown with the disk controller unit it replaces. It can supplant 400 packages.

At Hitachi the users have access to the same CAD system as the device fabricators, so normally device fabricators receive two tapes—one for the pattern generator and one for the device tester.

Hitachi's high-speed device for its fastest computer is an ECL gate array with the equivalent of 550 gates. Actually there are only 352 internal circuits—three-input OR/NOR cells—and 64 OR/NOR buffer cells. But the use of wired-ORs and dotted-collector ANDs gives the larger gate count.

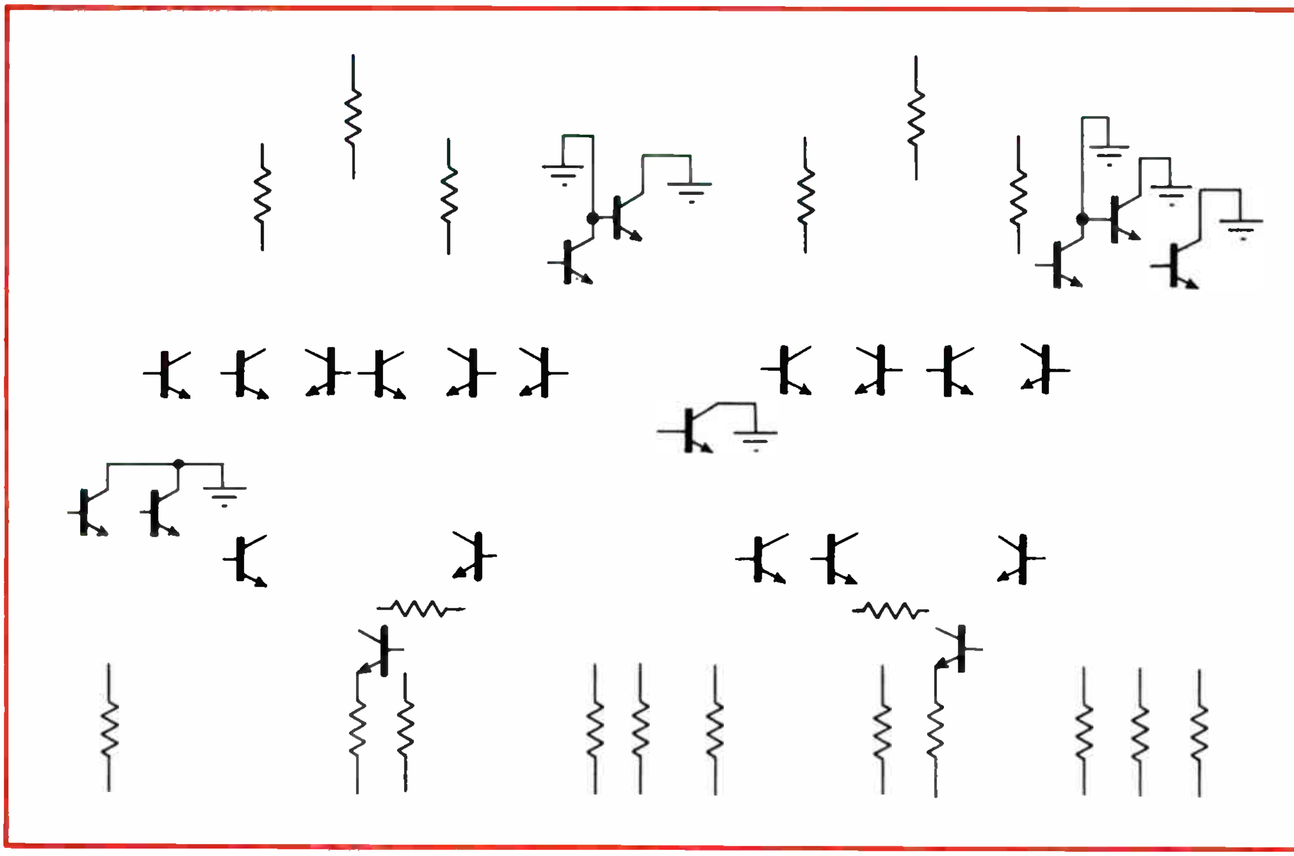
**Pins proliferate.** The internal circuits operate at a power-delay product of 5 picojoules; they have a delay of 0.6 ns at one load and average 1.2 ns at three loads. The 5.7-$mm^2$ chip is sealed in a 108-pin package, but many grounds are needed, so there are only 88 signal pins.

Hitachi also has an advanced low-power Schottky TTL circuit similar to Fujitsu's larger TTL device. It consists of 378 three-input NAND gates and 54 output buffers on a 5-$mm^2$ chip in a 72-pin package with 68 signal pins. It differs from Fujitsu's device in not being intrinsically designed for three-state operation, although internal gates can be used to obtain this kind of output. The device is used mostly in computer peripheral circuits. Hitachi is now developing a 1,500-gate TTL device with more than 100 pins.

**-Charles Cohen**

density. Exar is one of the only companies using pure $I^2L$. Signetics uses Schottky-barrier diodes on each output; this it calls integrated Schottky logic, or ISL (see Fig. 5). Harris and Texas Instruments use Schottky transistor logic (STL). ISL and STL both use Schottky barrier diodes to isolate their outputs; STL goes on to add a Schottky clamp on the cell's internal npn transistor. Different metalization systems are employed so that the barrier heights on the transistor and the outputs differ by about 200 mV. Ten masking steps are required for ISL, 12 for STL. Harris' approach is to build ISL cells and add the extra STL steps if the higher speed is a must.

TI is getting serious about gate arrays with 250-, 500-, and 1,000-gate STL arrays that have 40, 64, and 112 bonding pads, respectively, and extensive automatic placement and routing software. This is a long time



**7. Uncommitted.** ECL gate array cells are usually shown in this kind of exploded view so that connections can be penciled in. These particular components belong to the F300 array from Fairchild. Other chips in this family will include scratchpad random-access memory.

coming, considering that the Dallas company helped get the gate array idea started with its Master Slice flip-flops of the late 1960s. TI has also had for some time an $I^2L$ array, the SBP9600, for use with the SBP9900 $I^2L$ version of the TMS 9900 16-bit processor. Its new arrays will use triple-level metalization, requiring five custom masks. The third metal level will be used for power and ground. This all smacks of IBM.

## Speeding customization

"If gate arrays are to be effective, then the turnaround time on the part must be fast," TI's Gibson notes. "Less than 12 weeks is acceptable for starters, but we can see the capability of going down to 3 weeks. This, of course, will require a high degree of automation."

TI will release in stages what it calls gate array design utility software. First it will offer documentation that will allow a user to design for a TI array using his own manual methods or CAD techniques. This documentation will fully describe HDL, a hardware description language, and TDL, a test description language, which together will drive TI's automated gate array system.

TI expects to have remote job-entry terminals in its Chicago, Los Angeles, and Boston regional technology centers by the end of this year for the purpose of gate array specification. By 1982, it hopes to have this software in a transportable form for loading into a customer's machine. The package includes an HDL compiler, a logic simulator, a test pattern grader, a logic design rule checker, a testability analyzer, a routability analyzer, an HDL macro library of STL functions, and various utilities.

After analysis and a decision to go ahead with it, the logic description will be fed into TI's automatic layout system, which includes major phases for partitioning into gates, cell placement, gate placement, and intracellular routing. After routing, a logic verification routine is executed to pinpoint errors and a pattern generation tape is issued. Figure 6 shows the flow of information between the user and TI during gate array design. TI says that initially it will take about 10 working days to accomplish the automatic layout and six weeks to produce the parts using photolithography. It hopes to trim the layout time down to about 4 days by the end of this year and the production time to about 5 days in 1982 using an electron beam to write directly on the wafer.

International Business Machines Corp.'s experiences with gate arrays date back 10 years with the layout of a 130-gate bipolar chip, through the automated design of 700-gate arrays in its System/38 and 4300 series computers, to a 1,500-gate slice used in microcontroller applications. It has recently completed a 5,000-gate chip that it has used to successfully implement one of its popular mainframe computers [*Electronics*, Aug. 14, 1980, p. 96].

Another one of its most recent master slices contains 3,425 six-output STL gates, measures about 22 $mm^2$, and has 122 flip-chip solder dots. A set of the customized circuits for the array that IBM calls books are stored in IBM's Engineering Design System, or EDS, a sophisticated software system that allows simulation and physical wiring of an IC at a remote station.

Interestingly, no area is allocated for wiring on this particular chip; rather, books are simply not placed over cells where wiring is needed. After completing the physical design with EDS, the data is processed for mask making or electronic-beam processing. To ease diagnostics, LSSD techniques are used and several test sites are located on each wafer to monitor process and device characteristics.

IBM will be using this master slice as an I/O controller for its System/38 computer. This version of the IC will contain an 8-bit microprocessor driven by an 18-bit instruction word. There are also two 13-bit control-store address registers, a 6-bit program status register, a 9-bit selector register, and random control logic. The controller array uses 1,626 of the internal cells and the wiring, if laid out in a straight line, would be 172 centimeters or about 68 inches long.

Fairchild Camera & Instrument Corp., Mountain View, Calif., has two aggressive gate array programs, one using Isoplanar $I^2L$ (its $I^3L$) and another using ECL. At this month's Wescon show, two very dense, fast chips will be revealed: the 4,000-gate F9480 $I^3L$ array and the subnanosecond F300 family of ECL arrays.

The cells in the 9480 consist of four npn and four pnp transistors arranged so that four first-layer and three second-layer metal channels pass above without interfering with intracell connections. There are 16 rows, each with 62 cells for a total of 992 or 3,968 gates. Programmable current-setting resistors, running the length of the array, allow for adjustment of each horizontal current injector.

Fairchild is developing a macrocell library for the 9480 containing D-type flip-flops, adders, latches, and many other standard functions. Depending upon the randomness of the design, typical gate utilization rates will vary from between 50% and 80%, says Fairchild. The array can be laid out and digitized in much the same way that IMI does with its Iso-CMOS arrays. But Fairchild's short-range solution is to use the Computervision CAD system and PC-ES software for automated placement and routing. Its long-range goal is to automatically place and route on a mainframe computer. It also hopes to automatically generate test vectors for its Sentry system.

## The fastest

Other companies producing ECL arrays are Motorola, AMCC, and various European and Japanese companies. When it comes to speed, ECL is on top with subnanosecond gate delays. As mentioned, many of the ECL arrays wind up in mainframe computers.

Amdahl Corp. of Sunnyvale, Calif., is one such user. Its 470/V6 machine uses 110 parts made with the same master slice, which is supplied by Motorola and Fujitsu. Its newer /V7 and /V8 computers use 130 of the chips, which contain a five-by-five array of four-gate cells that can take on 17 or 18 different configurations.

"If you're going to design a high-performance processor, you're going to wind up with a lot of random logic," states Amdahl's director of corporate planning and business development, David L. Anderson. "For our purposes it is cheaper to use master-slice LSI when you consider the overall picture such as board area and power dissipation. It is considerably more reliable," he adds.

**MOTOROLA BIPOLAR GATE ARRAY TECHNOLOGY**

| | 1974 | 1979 | 1982 | 1985 |
|---|---|---|---|---|
| Gate count | 150 | 750 | 2,100 | 6,300 |
| Gate delay, ns | 1 | 0.75 | 0.50 | 0.20 |
| Gate power, mW (logic switch with emitter follower) | 8 | 4 | 2.8 | 2.4 |
| Gate area, $mil^2$ | 225 | 100 | 30 | 15 |
| Technology | junction isolated | Mosaic* I | Mosaic II | Mosaic III |

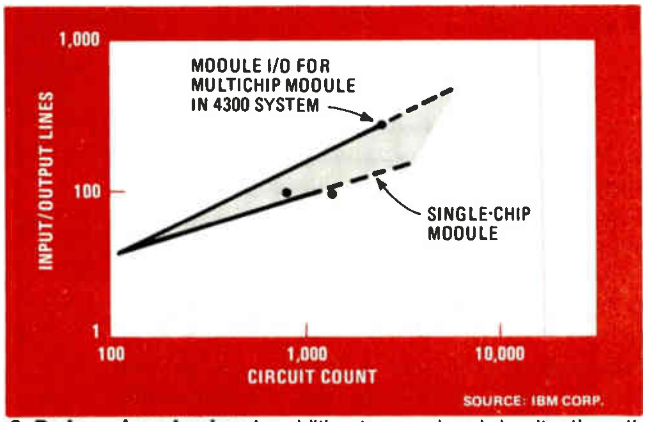
*Motorola oxide self-aligned implanted circuit

Anderson does not see too much overlap in store between high-speed C-MOS arrays and higher-speed bipolar slices. "In the mid-1980s I expect C-MOS arrays to be below 1 ns. But we'll be down into the 100-to-200-picosecond range. My suspicion is that C-MOS will never make it for the highest-performance applications. Instead, maybe we'll shoot for gallium arsenide arrays and, who knows, maybe Josephson junctions." But then Anderson would not be surprised to see a mix of technologies, "with ECL arrays at the heart and C-MOS arrays for such things as console I/O."

As Amdahl's current line points up, many of the ECL arrays now in use are low in density. But it will be no surprise to see larger arrays in upcoming computers. To give an idea of the capabilities of Fairchild's new F300, Tom Goodman cites the Cray-1. Goodman is bipolar product manager at Fairchild in charge of gate arrays. "The Cray-1's got 225,000 GCO-1s," Goodman begins. The GCO-1, made by Fairchild, has two five-input ECL gates. "So there's somewhere on the order of 450,000 gates [in the Cray-1]. Assuming we use 3,000 gates in the F300, we could make that thing with about 150 parts." The power dissipation would be lower and it would run faster, he predicts.

Motorola's principal Macrocell array product at present, the MCA-1, has about 1,200 equivalent gates [*Electronics*, Feb. 15, 1979, p. 113]. About five months off is a 600-gate mini-array that consumes half the power of the bigger part: 2 watts versus 4. Next year, Motorola will recast its 1,200-gate array in low-power Schottky and, in the second quarter, an advanced low-power Schottky array will be introduced. Motorola also intends to prove the economy of the Macrocell array with standard parts; it is selling an 8-by-8-bit multiplier, for instance [*Electronics*, April 24, 1980, p. 204].

ECL arrays are a different breed in more ways than just raw speed. They run hot. The F300 dissipates from 2 to 20 W; above 6 W, liquid cooling is almost a must. Also, the cells in an ECL array usually contain both transistors and resistors, positioned so that common functions are




**8. Pads and packaging.** In addition to speed and density, the ratio of gates in an array to the number of input/output pads, too, is an important number. If this ratio is near 10:1, as it is in some IBM arrays, packages with more pins should be developed.

easily wired up. Motorola and Fairchild both take this tack. The components in a quarter cell of the F300 are shown in Fig. 7.

The F300 family is at present slated for seven members with 100 to 500 quarter cells. The latter has a gate equivalent of 5,000-plus, says Goodman, and gate delays will be as short as a half nanosecond. Motorola's Macrocell array contains just over 1,000 equivalent gates but it is projecting much higher densities using Motorola oxide self-aligned implanted circuit, or Mosaic, processing (see table).

Fairchild is taking a noteworthy step by adding specialized blocks to certain members of its F300 family. Just as the C-MOS people are adding dedicated flip-flops, three of Fairchild's F300 chips will have programmable logic arrays and all but the biggest device will have random-access memory, which Goodman says will be valuable for a scratchpad. All of the macro layouts under consideration by Fairchild will offer, as an option, level-sensitive-scan inputs. Goodman admits this adds some area overhead, "but not if you choose not to use it."

Fairchild's plan sounds similar to TI's. Indeed, a trend is brewing whereby large companies will one day be able to call up semicustom logic from across the globe and get finished parts shipped for their specific application. There will be heavy exchange between huge corporations and the semiconductor houses acquired for captive consumption. Doubtless Schlumberger will be using Fairchild in this way.

An even better example concerns the recent announcement that Mostek Corp. will be primed with at least $20 million by parent company United Technologies Corp. to construct a microelectronics center in Colorado Springs, Colo., for the express purpose of designing gate arrays [*Electronics*, Aug. 28, 1980, p. 109]. Mostek and UTC decided on C-MOS and array sizes ranging from 200 to 4,000 gates.

## Other considerations

Without doubt, future gate arrays will have more cells. But perhaps more important than the number of gates is the ratio of gates to wiring channels or the ratio of gates to input and output pads. Some manufacturers, IBM included, have discovered than an efficient gate-to-I/O-pad ratio is about 10:1; that is, an I/O pad for about every 10 gates (see Fig. 8). This high ratio will dictate more expensive packaging like 100-plus–pin leadless chip carriers and quad in-line packages for the high-density arrays.

Testing problems also threaten to limit the growth of the gate array business because even with automatic layout, testing algorithms are usually still best generated manually. "Gate arrays don't create new testing problems," stated John Birkner of MMI at Wescon 80, "they just move the old testing problems from the printed-circuit board onto the chip."

The problem, states Birkner, arises because the physical realization of an array is quickly outpacing the ability to test it. "For a single systems design, a few engineers can create as many as 200 new and unique gate array patterns," he says, but "this translates into four years of test engineering time." The solution, he suggests, is to get the chip designers more involved in the testing of the arrays. This could be accomplished by developing more computer-aided tools like simulators that could be passed on to the customer.

## Standard cells

A discussion of gate arrays is really not complete without some mention of standard cells. These are called up from a library and are positioned in their entirety on the silicon—they are not built from preprocessed gates, so an entire mask set must be generated for standard-cell ICs. So standard cells fall somewhere between gate arrays and fully custom chips.

Only two companies now advertise a commercial standard-cell service. Signetics Corp. of Sunnyvale, Calif., offers Composite Cell logic (CCL) and Plessey Ltd., Microcells. Signetics' system can be used to create chips with densities ranging to 1,000 gates. Cells are chosen from two libraries: a low-threshold library and an extended-performance library. Also, these Schottky logic libraries will soon be accompanied by an integrated Schottky logic (ISL) library.

Unlike Signetics' Composite Cells, Plessey's Microcells are MOS, so they are slower. But Plessey claims 1,500-gate chips are easily realized. Signetics asks the customer to tape the layout on gridded Mylar, indicating bottom- and top-level metal interconnections with red and blue pencils. Signetics then digitizes from this worksheet using in-house CAD tools. With Plessey's system, the designer's schematic diagram is entered into a Calma graphics system via a specially designed button menu. From the digitized schematic, the six mask layers for the process are generated.

An exciting prospect is in store for gate arrays: electrically programmable cells. If mask programming could be supplanted by electrical programming—and erasure, for that matter—the chip makers could produce a truly universal part with outstanding appeal. This idea is not as blue-sky as it sounds; as IBM Corp. will describe a nonvolatile programmable array at the International Electron Devices Meeting in December. □

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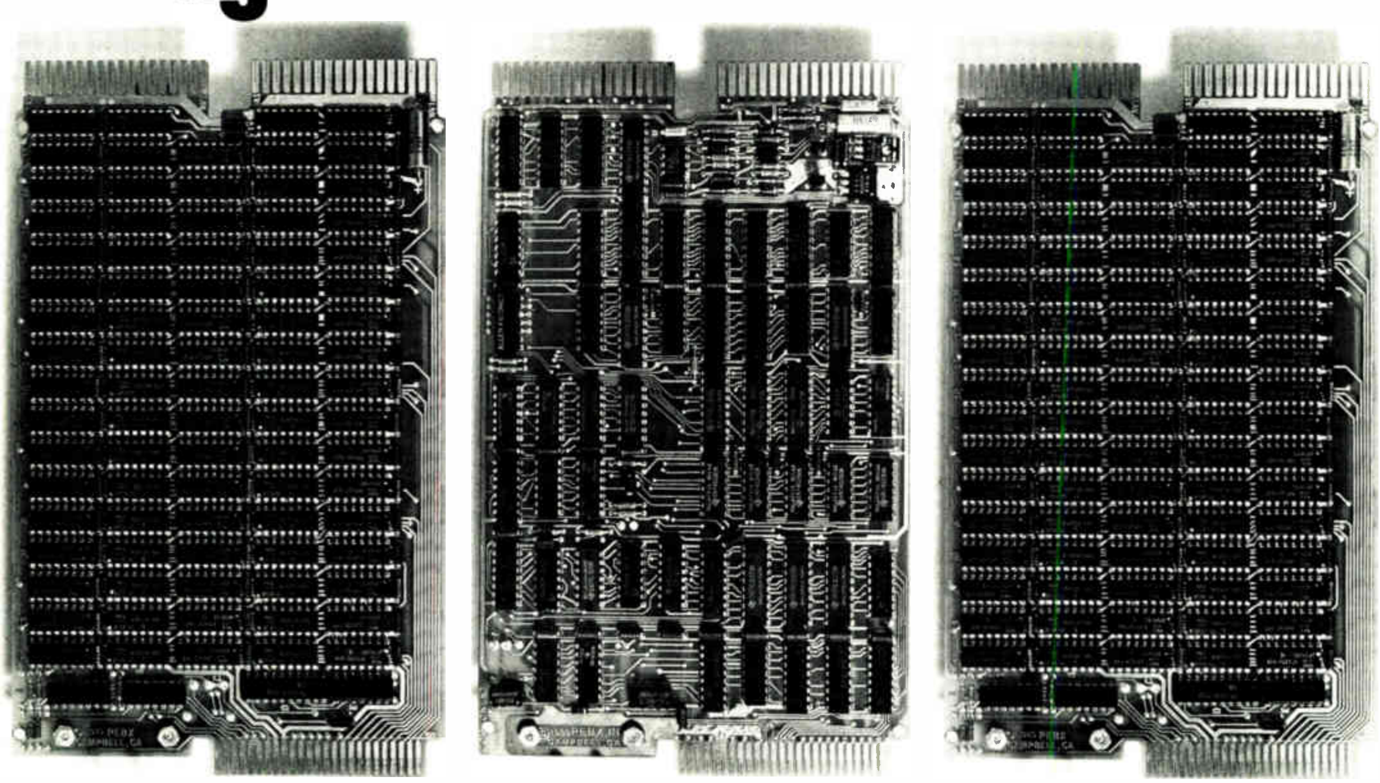
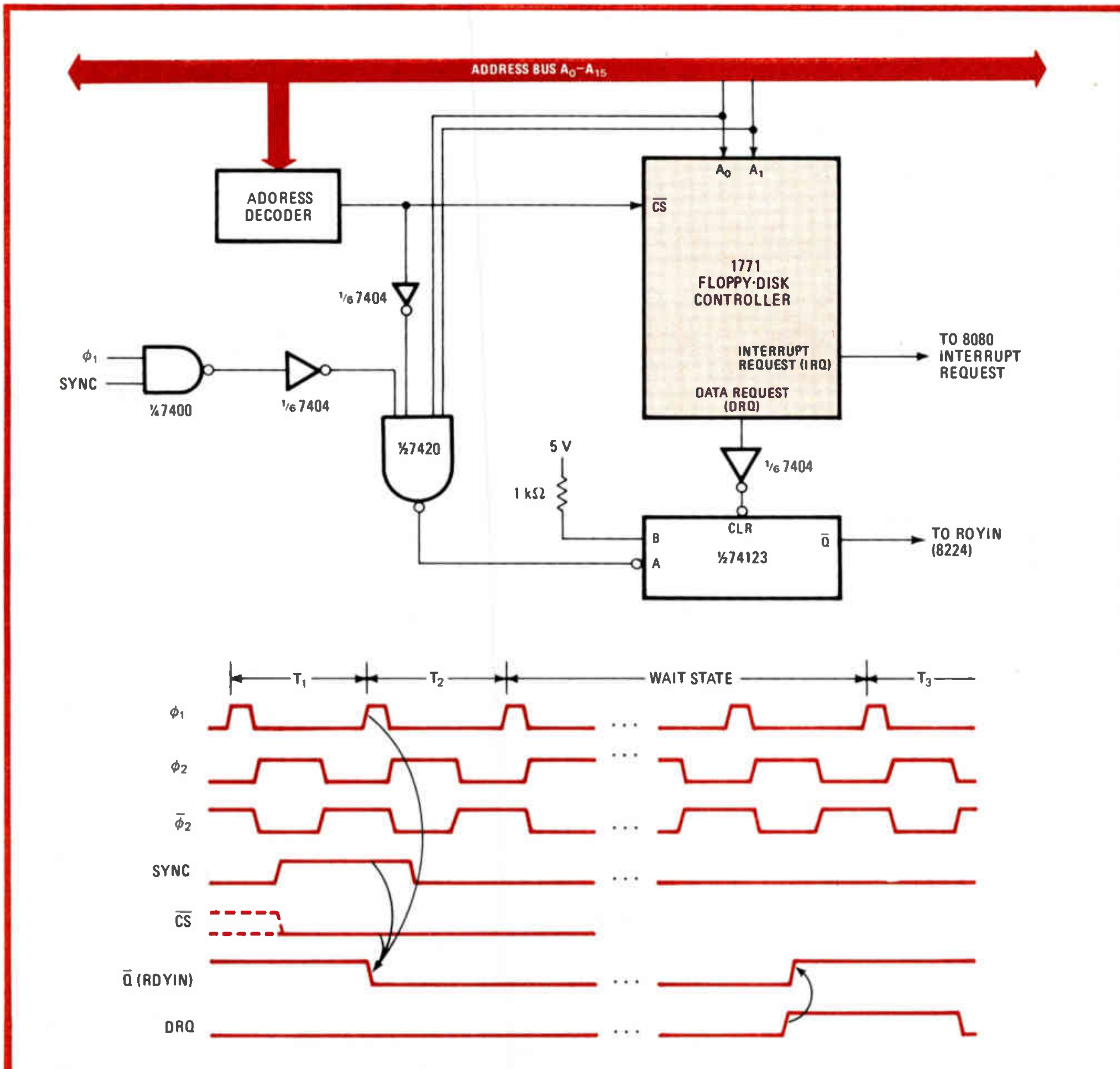


*LSI-11 is a registered trademark of Digital Equipment Corporation.

## Speeding floppy data transfer under program control

by S. Shankar
*Sangamo Weston/Schlumberger, Energy Management Division, Atlanta, Ga.*

The transfer of data between a floppy-disk drive and memory is normally carried out through a microprocessor's direct-memory-access (DMA) port—a bit of overkill, considering that the disk drive's data rate is relatively slow (1 byte every 32 microseconds) while the DMA's write time is less than 1 μs. Still, using DMA represents one of the best ways to process the data because other methods, such as input/output or interrupt control, are just not fast enough to accommodate the floppy. But data can be transferred under program control, while avoiding the time-consuming test-flag and jump steps that are so much a part of the aforementioned methods, if the processor's read and write operations are synchronized with the rate at which the floppy handles data.




**Synchronous.** Software-based controller minimizes processor-to-floppy-disk data-transfer time by ensuring that processor's read and write operations are synchronized with floppy's data rate. Scheme works with any processor having the ready and wait facilities.

| 8080 PROGRAM FOR DATA TRANSFER BETWEEN MICROPROCESSOR AND FLOPPY DISK | | |
|---|---|---|
| Label | Source statement | Comments |
| | LXI H, FDCRGG | Set up (H,L) to point to FDC data register |
| | LXI B, BUFFER | Set up (B,C) to point to buffer area where data is to be stored |
| | — — — — — | |
| | — — — — — | |
| | — — — — — | Set up 1771 for Read |
| | — — — — — | |
| | — — — — — | |
| | JMP READ | Go to READ |
| | ⋮ | |
| READ | MOV A, M | Move byte from FDC Register to 8080 accumulator. The 8080 goes into WAIT until data becomes available. |
| | STAX B | Store contents of accumulator in buffer area. |
| | INX B | Increment (B,C) |
| | JMP READ | Go back for more |
| | ⋮ | |
| RSTX | — — — — — | Interrupt Service Routine for IRQ. Routine is executed on completion of READ |
| | — — — — — | |
| | — — — — — | |

The implementation is shown for the Western Digital 1771 floppy-disk controller working with an 8080 microprocessor. As seen with the aid of the program, the processor initially generates an output command to the floppy-disk controller to start the data-read operation. It then proceeds to the read routine and attempts to read a data byte from the floppy's data register.

The data register is accessed when $A_0 = A_1 = 1$ is placed on the data bus and CS = 0. Then the 74123 monostable (one-shot) multivibrator is triggered on the occurrence of the synchronizing signal, forcing the processor into the wait state.

When the floppy disk is ready to generate a data byte, line DRQ goes high and clears the one-shot. The processor comes out of the wait state and reads the byte. It then loops back and repeats the operation.

The read loop could go on indefinitely. To afford some flexibility, however, provision is made for interrupt control. Because the IRQ command is always generated on completion of a read-command execution, the processor can never hang up.

The same technique is used to write data into the floppy. The only difference is that the processor writes data into the disk each time a DRQ signal is generated.

The total time required to transfer one byte of data with this method is 29 machine cycles, or 14.5 μs using a 2-megahertz clock. The method should work just as well with double-density floppy disks where the rates are twice as fast. □



# Programmed comparator finds loss in optical fiber

by J. T. Harvey and G. D. Sizer
*AWA Research Laboratory, North Ryde, NSW, Australia*

This circuit simplifies the job of finding an optical cable's quality for systems that use time-domain reflectometry (TDR) to measure transmission loss. The novelty of the circuit is that it is used as a programmable comparator to determine the times (and thus the cable length) corresponding to preset levels of the optical backscatter signal generated by the system, instead of to sample the amplitudes of the signal at preset times, as is normally the case. Consequently, circuit complexity is minimized and the measurement procedure is made significantly easier. Although the measurements will not yield results as accurate as could be achieved in the lab, they are adequate for most field applications—typically, to within 0.2 decibels per kilometer of the true cable attenuation.

In the TDR technique, the backscatter signal, which is derived from the fiber's reflection of an infrared pulse generated by the system's laser pulser, is detected by a photodiode amplifier and introduced to the vertical input

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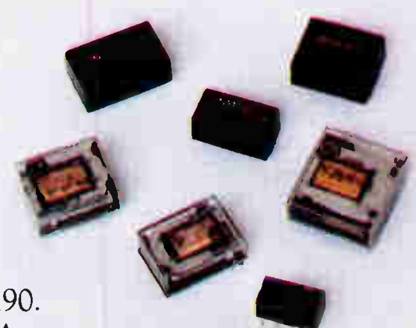

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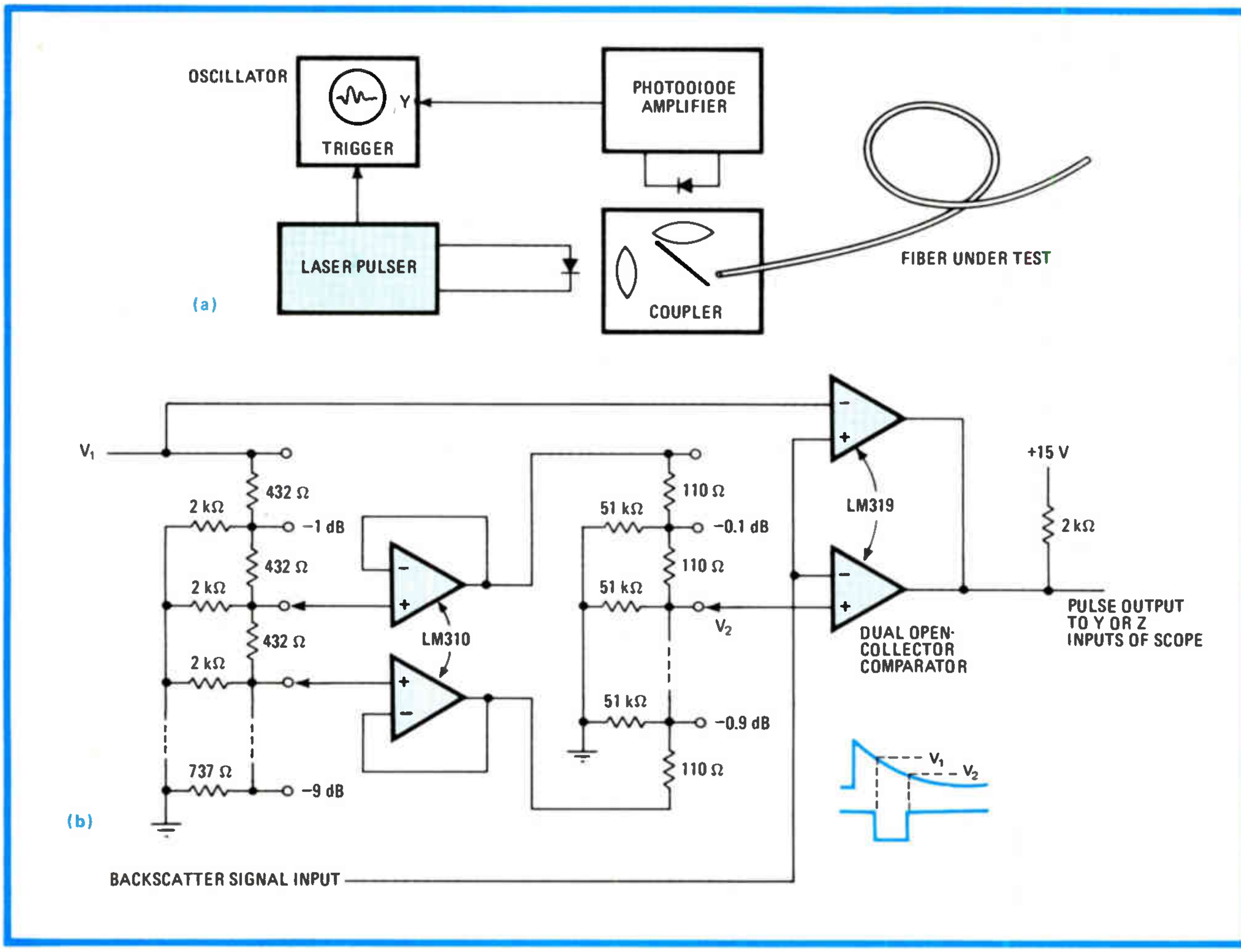


**Simplified.** Comparator determines the threshold crossing times corresponding to preset levels of an infrared backscatter signal so that loss in optical cable can be found directly. Accuracy of system is to within 0.2 dB of true value for fibers having 3 to 6 dB/km of loss.

of an oscilloscope. The laser pulser triggers the scope periodically as shown in (a) so that the profile of the backscatter signal can be sampled and the resulting cable loss calculated. Sampling, averaging, and computation are done in a variety of ways[1,2], often requiring a rather complex digital timekeeper to coordinate the measurement activities and a scope reading for estimating cable loss.

The slope of the backscatter signal (actually, the log of the slope, as it is exponential for a cable having constant loss per unit length) can be found easily with the circuit shown in (b), which uses a variant of a two-point sampling technique described in reference 2. There, the backscatter signal is sampled at two set times and the samples digitally processed to yield the loss between sample locations. With this circuit, however, the sample levels are set and the propagation times (and cable loss) corresponding to them are found.

Essentially, the circuit is a window detector that generates a pulse width corresponding to the time it takes for the backscatter signal to cross two preset thresholds. The first threshold is continuously variable, being set by voltage $V_1$. The second threshold is selectable in 0.1-dB steps from 0 to 9.9 dB by means of the resistive ladder, which is designed so that the voltages corresponding to those steps are given by 5 log $V_2/V_1$. This response matches that of the typical square-law photodetector and optic cable system.

The circuit can be used in several ways. One convenient way to measure cable loss is to set $V_1$ to initiate a pulse edge on the incident laser pulse and to adjust the second threshold so that the end of the pulse terminates 10 $\mu$s later. (This is the time taken for a double transition of a pulse through a 1-km fiber with a refractive index of 1.499, which is within 1% of the value expected in commonly available optical cables.) The cable loss, in dB, is then found from direct readout of the tapped resistive ladder.

The resolution of the measurement will be within 0.1 dB/km for a cable having a loss of from 3 to 6 dB/km. The estimated error in setting the pulse trigger time for a 1-km cable corresponds to a length deviation of about 30 meters, due largely to jitter on the laser pulse. The overall measurement error is thus 0.2 dB/km for cables having a low to medium loss—more than adequate for field use. □

**References**
1. M. K. Barnoski and S. M. Jensen, "Fiber Waveguides: A Novel Technique for Investigating Attenuation Characteristics," Applied Optics, Vol. 15, No. 9, Sept. 1976, pp. 2112-2115.
2. A. J. Conduit *et al.*, "An Optimized Technique for Backscatter Attenuation Measurements in Optical Fibers," Optical and Quantum Electronics 12, 1980, pp. 169-178.

**NBS issues standards for I/O interfaces**

The National Bureau of Standards has published its first set of four Federal input/output interface standards for computer equipment. The four, printed as Federal Information Processing Standard publications (FIPS PUBS), are No. 60, "I/O Channel Interface Standard"; No. 61, "Channel Level Power Control Interface"; No. 62, "Operational Specifications for Magnetic Tape Subsystems"; and No. 63, "Operational Specifications for Rotating Mass Storage Subsystems." **Equipment must be verified by the NBS as being in conformance before it will be accepted for use by Federal agencies.** Manufacturers that will be able to deliver equipment conforming to the standards in time for acceptance and that can meet individual benchmarking requirements will be able to submit bids to supply medium-sized and large computer systems.

Prospective suppliers wishing to have equipment verified should first submit documentation detailing the equipment's interfacing specifications directly to the NBS. For further information, contact John P. Riganati, chief of the System Components division, Institute for Computer Sciences and Technology, National Bureau of Standards, Washington, D. C. 20234, or call (301) 921-2705.

**Seminars prepare technicians for IC processing**

In response to the need of semiconductor manufacturers to train and augment the industry's supply of technicians, Varian Associates has announced an expansion of its East and West Coast training programs, which, according to a spokesman, can take a good assembler or technician and within one week of intensive training give him a strong start in becoming a vacuum-system or coater specialist. Varian offers several courses for maintenance and process technicians, including "Basic Vacuum Technology" and "Leak Detector Operation." On the West Coast, where Varian manufactures its coater systems, it offers hands-on training in system operation and maintenance. In addition, courses on the operation of ion-implantation systems and electron-beam lithography will be conducted by Extrion division personnel in both Woburn and Gloucester, Mass.

The cost of the seminars ranges from $280 for a two-day course to $700 for a five-day course, including materials. **Classes are kept small, and instruction includes the extensive use of audio-visual aids.** For schedules and registration information, call Mimi Wong, (415) 493-4000, ext. 2295, or write her at 611 Hansen Way (Mail Stop D-106), Palo Alto, Calif. 94303.

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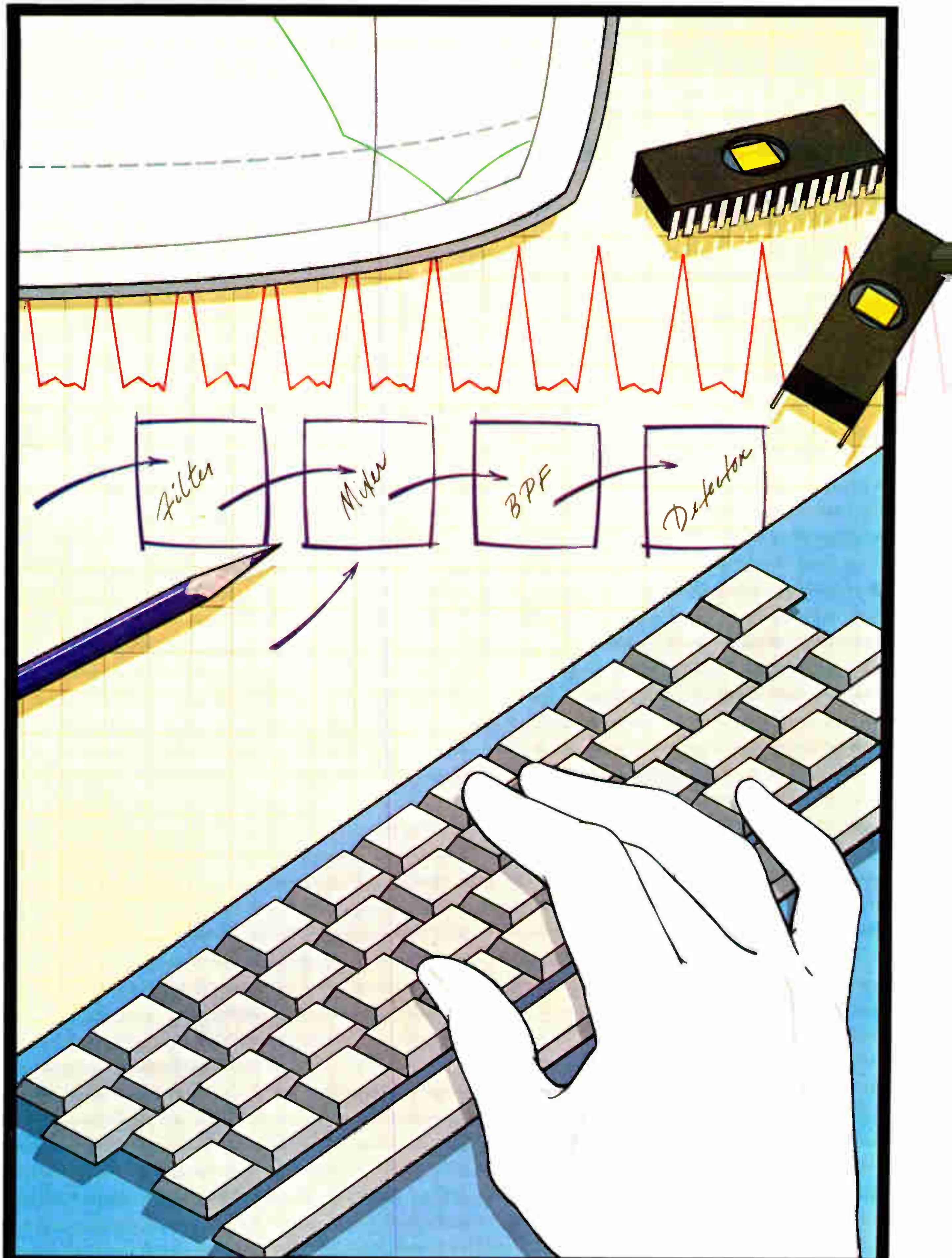
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## Analog systems can now be built with cost-effective digital LSI tools: Intel's 2920 Signal Processor and Intellec® Development System.

In analog design, Intel's new 2920 Signal Processor support package puts the speed and power of *Programmability* literally at your fingertips.

A complete signal processing system, the 2920 consists of a 9-bit A/D converter, integral high-speed processor, and D/A converter—all on a single chip. For virtually any analog system in the DC to 10-kHz range, the 2920 can make a world of difference. It's the first intelligent digital LSI chip powerful enough to process analog signals in real-time.

Because it's programmable, the 2920 can be used for a variety of applications, and is therefore being manufactured in high volumes. This has already enabled prices to be significantly reduced. And with the ROM version, you'll be able to save even more—implementing complete functions such as a modem for under $20.

But just as importantly, a complete development support system is available for the 2920. So now you can solve analog design problems in *software*—taking just a fraction of the time it once took. And reducing fixed labor costs, because a multitude of design solutions are readily available. Solutions for applications like these:

- Telecommunications
- Speech processing
- Process control
- Laboratory instrumentation
- Seismic/Sonar signal processing
- Industrial automation
- Guidance and control

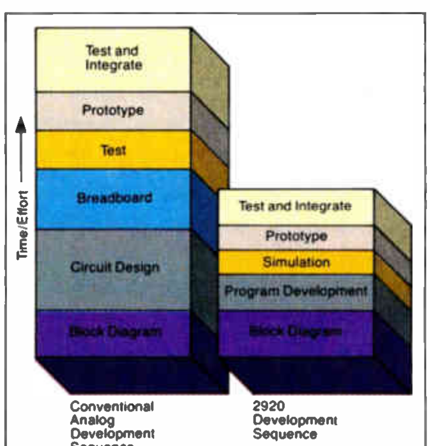
### Reducing Risks in development

The key to streamlining the design cycle with the 2920 is Intel's 2920 Software Support Package and time-tested Intellec® Microcomputer Development System. Software tools included in this package are the Signal Processing Applications Software compiler, assembler, and simulator.

Using these tools, the typical 2920 design sequence is quite straightforward. Working from the Intellec terminal, you specify for the system those analog functions and parameters required. The system compiles, assembles and simulates the desired analog function for the 2920—all without any actual breadboarding. When your design is complete and tested in software, it is quickly transferred to the 2920 chip via the Universal PROM Programmer, for final real-time testing with the hardware.

### Time is money

As shown here, the 2920 approach can significantly reduce




development time—and thus costs. Because it eliminates breadboarding, the 2920 approach is much less labor-intensive than conventional analog design. And since you work with the same elements for each new design project, the learning curve effect makes subsequent projects go even faster. Which helps you get to market more rapidly than ever, with products that are simpler, more easily reproduced, and more reliable. For many applications, that means a single development cost savings—plus the competitive edge and improved reliability you gain—may justify your entire investment in the system.

### Total solution advantages

The 2920 total solution approach now offers you a real competitive edge in the analog design world. In shorter development cycles. In vast new product opportunities. In lower overall development costs. To begin designing your next generation of analog system products with that competitive edge, it's essential that you act today.

Your keys to faster analog design are now on distributors shelves and in demonstration centers. For a demonstration of our 2920 and development system capabilities, or to order, call your local Intel sales office/distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080. We'll also be happy to send you our complete information package including a schedule of Intel's world-wide 2920 Design Workshops, on request.

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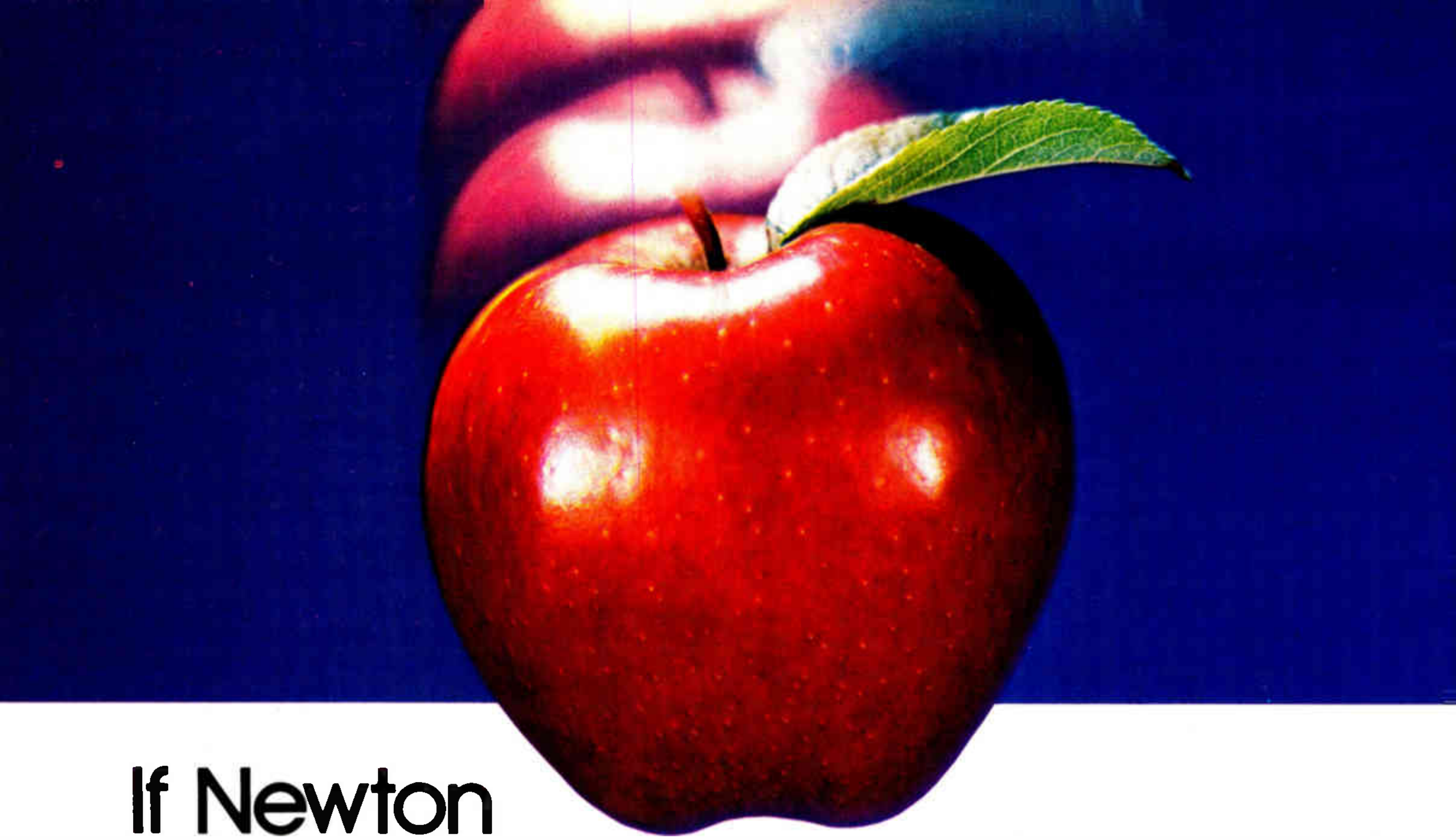

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Schenectady, New York 12345

**GENERAL ELECTRIC**

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# $125 12-bit a-d unit converts in 3 μs

Analog-to-digital converter selling for $124.50 in 100s includes internal clock and 10-V reference

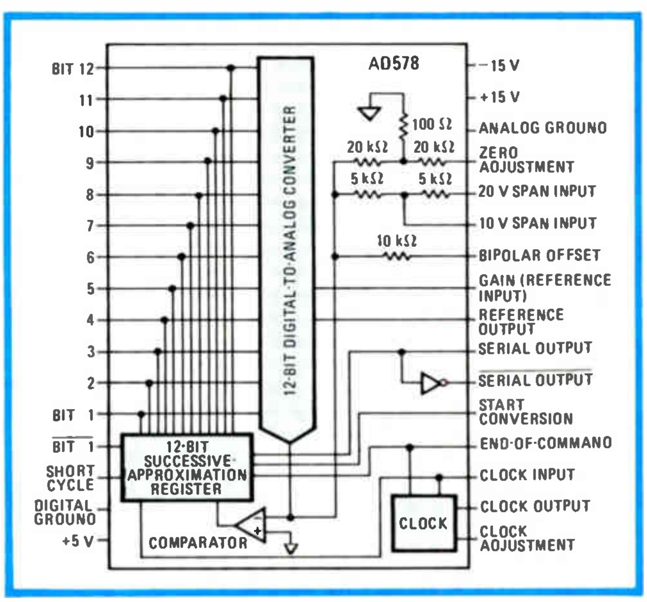
*by James B. Brinton, Boston bureau manager*

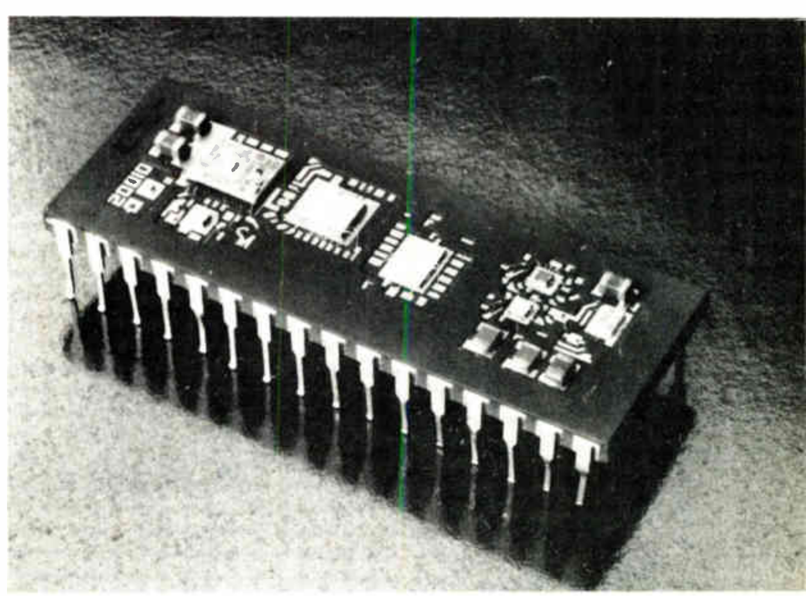
**The AD578L,** a complete 12-bit analog-to-digital converter, is faster than most of its competition [*Electronics*, July 17, p. 107], offers a list of convenience features, and—at a 100-unit price of $124.50—costs from $50 to $170 less, says David W. Kress, manager of new product marketing at Analog Devices' Semiconductor division.

The converter comes in a 32-pin double-width dual in-line package and contains a successive-approximation a-d converter, a 10-V reference, and a clock. Both of the latter can be used as system references; their outputs are available at package pins for use in applications where a common voltage or timing reference is useful, as in data-acquisition systems. The conversion time of the AD578's L version is typically 3 μs, though the unit is offered in two slower, lower-priced versions with speeds of 4.5 μs (the K version at $99.50 in 100s), and 6 μs (the J version at $85 in 100s).

Both clock rate and word length are adjustable, making possible faster or slower conversions at 12-, 10- and 8-bit resolutions. Shorting the appropriate pins turns a 578 into either a 10- or an 8-bit converter with 2- and 1.4-μs conversion times, respectively. Clock-rate adjustment is a simple matter of inserting either a resistor or capacitor of the necessary value between appropriate package pins. The 10-V buried-zener reference, which is accurate to within 0.1%, can be quickly trimmed to accuracy within 0.01%—equivalent to about 13 bits of absolute accuracy. The reference has a 15-ppm/°C temperature coefficient. And an outboard reference can supplant the AD578's internal one. This adds up to a good deal of applications flexibility, notes Kress, who adds that Analog Devices' goal was to enter the market with a unit having "no-compromise specifications" and significant price and convenience advantages.

Compared with similar converters, the only tradeoff of note is in speed, says Kress. Analog Devices' own HAS1202, for example, costs about $50 more and converts only 0.2 μs faster than the 578. At least one competing unit is as much as a full microsecond faster than the 578, but Kress feels that, for many, the 578's one-third lower speed will be offset by its 50% lower price. The converter's power dissipation, says Kress, may be the lowest of any competing unit, at 775 mW typical and 1.2 W maximum. Kress claims that the



**All in one.** In a 32-pin double-width DIP, the AD578 contains a 12-bit successive-approximation analog-to-digital converter, a 10-V reference, and clock. The outputs of the reference and clock are available at the pins for use when a common voltage or timing reference is needed.

competitive state of the art is closer to 2 W maximum—a factor that could be important to users with power-supply limitations. Supply requirements for the 578 are ±15 and +5 V, both ±10%. A ±12-V model also is available.

Scaling resistors allow the unit to operate over a variety of input ranges. Analog inputs of ±5, ±10, and 0 to +20 V all are accommodated at input impedances of 5 to 10 kΩ. The resistors are included on the 578's monolithic converter chip and will therefore track each other well with changes in temperature.

The unit's low power dissipation and consequent low operating temperature, plus the location of its scaling resistors, make possible some respectable temperature coefficient specifications, notes Kress. Gain temperature coefficient is ±15 ppm/°C typically and ±30 maximum. Unipolar offset is ±3 ppm/°C typically, ±10 maximum; the bipolar offset tempco is put at ±8 ppm/°C typically, ±20 maximum. The differential linearity tempco is ±2 ppm/°C typically.

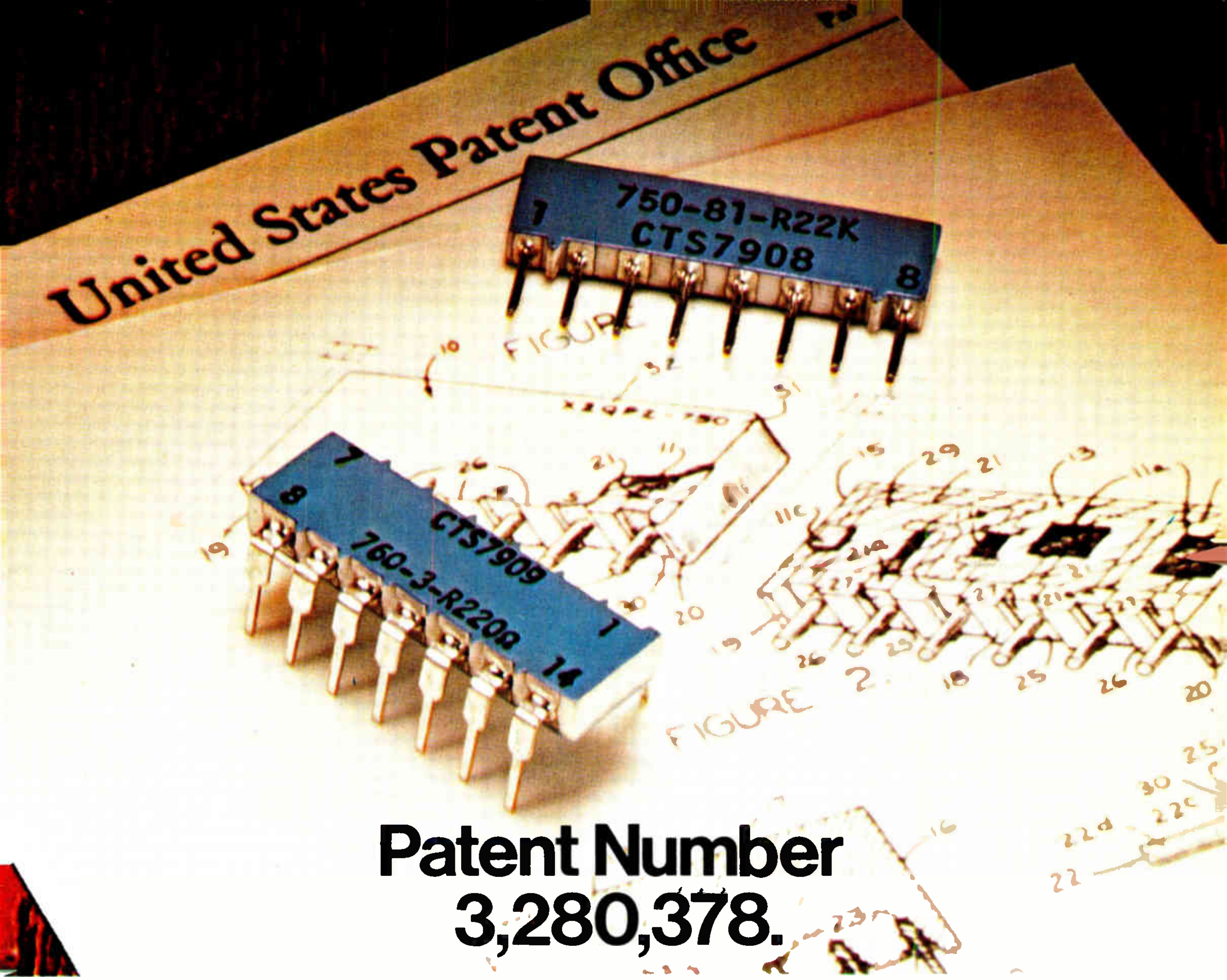
Both unipolar and bipolar, serial and parallel outputs are available from the 578, and in a variety of codes; binary, offset binary, 2's complement binary, and complementary-offset binary. The converter's output stage can drive the equivalent of five TTL loads.

Maximum nonlinearity of the device is specified as 0.012%. The firm guarantees no missing codes for 12-bit conversions at standard speeds over the 578's full operating temperature range of 0° to 70°C.

A ceramic dual in-line package is employed for all models, but users may choose a polymer seal for use in nonhostile environments or a solder seal for harsh applications. The latter is due in two or three months at a $7 to $10 premium.

All units are available from stock. Single-unit prices are $127.50 for the AD578J, $149.50 for the AD578K, and $186.50 for the AD578L.

Analog Devices Inc., Rte. One Industrial Pk., Norwood, Mass. 02062. Phone (617) 329-4700 [338]




# Patent Number 3,280,378.

## Termination strength is the key to network reliability— patented CTS Anchor Lock Terminations are the key to strength.

The secret? Our superior process forcefully drives the leads into tapered holes in the substrate, cold forming the lead to the substrate and wedging it tightly in place prior to soldering. Try pulling out a CTS lead; you'll see how much assurance our 5 lb. pull strength gives you. Then try it with a competitive product! You'll see what we mean.

Why risk a loose termination that can alter the resistance value of your network? CTS, and only CTS, can deliver the superior mechanical and electrical reliability qualities of Anchor Lock terminations. The same exclusive insertion process applies to both CTS Series 750 SIP and Series 760 DIP style cermet resistor networks.

Reliability has been our key to success. With more than one billion element hours of extended load life testing, CTS resistors have exhibited a failure rate of only 0.00041%/1,000 hours @ a 95% confidence level. Each SIP and DIP network is 100% value and tolerance tested before shipment.

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TL094
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# Introducing NFET. Single supply FET op amps. High impedance. Low distortion. More linear leadership from TI.

The high input impedance of BIFET *plus* single supply operation. That's NFET. An evolutionary advance in op amp circuitry that combines N-channel junction FETs with bipolar circuitry on a monolithic chip.

The result? *The first N-channel FET devices ever.* FET op amps that operate on a single supply voltage of 3 to 36 V.

The difference? NFET technology allows the op amps to process signals at or near ground. With no negative power supply required.

Compared to other single supply devices, TI's new TL091 Family has significantly better distortion characteristics. *And, the high input impedance of BIFET.* Imagine the possibilities. For applications never before possible with any single supply system. For automotive, telecommunications and instrumentation applications. With big savings in cost, design time and board space.

## Quads here now Singles, duals on the way

The TL091 Family of JFET input op amps share these common features:

- a wide range of supply voltages — 3 to 36 V
- class AB output stage
- high input impedance — N-channel JFET input stage $10^{12}$ ohms (typ)
- internal frequency compensation
- short circuit protection
- input common mode range includes $V_{CC-}$
- low input bias current — 100 pA (typ)
- low input offset current — 50 pA (typ)

Slew rates are typically 0.6 V/$\mu$S, bandwidths are 1 MHz open-loop and a typical noise of 34 nV/$\sqrt{Hz}$ at 1 kHz.

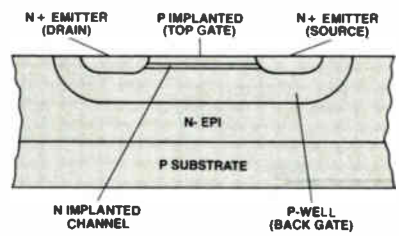
TL094 (quad) NFET op amps are available now at a 100-piece price of $1.97*. Singles (TL091) and duals (TL092) will join the family soon.

## New NFET comparator, too

The TL311 comparator uses new NFET processing, allowing us to offer you features like:

- first true single supply FET input comparator
- common mode input voltage range includes $V_{CC-}$
- pin-compatible with popular LM311
- high input impedance — $10^{12}$ ohms (typ)
- low input bias current — 100 pA (typ)
- low input offset current — 50 pA (typ)
- strobe capability
- input offset voltage — 2 mV (typ)
- supply current — 2.5 mA (typ)
- response time — 165 ns (typ)
- TL311 comparator 100-piece price $1.37*

### NFET technology ... a capsule summary

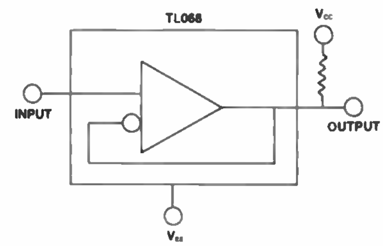



NFET is the result of advanced process and design techniques. Techniques that allow the combination of N-channel junction FETs and bipolar devices on a single chip. So, for the first time, you can get FET input performance and single supply operation. Our new NFET devices are capable of providing input sensing at ground level, output voltage swings to ground and significantly improved harmonic distortion yields.

## Family portrait

The new TL091 NFET Family joins the industry's broadest BIFET line. A line of general purpose (TL081), low noise (TL071), low power (TL061) and low input offset voltage (TL087/TL287) BIFET op amps. Eighteen products available in singles, duals and quads.

### TL068 BIFET buffer




TL068. An industry first. A JFET input unity gain voltage follower amplifier featuring high input impedance, wide bandwidth, low bias current and low quiescent power dissipation, plus:

- high slew rate — 7 V/$\mu$S (typ)
- low power — 3.5 mW (typ)
- 3-terminal "LP" package
- TL068 BIFET buffer 100-piece price $0.43*

## Imagination unlimited

Just as BIFET spawned a whole new generation of improved products, so too, the bright promise of NFET augurs much the same. A generation of products not previously technically acceptable. Until now.

The powerful, positive thrust of the new NFET technology is twofold. For us, it's another strong commitment to linear leadership. For you, it's the assurance of product design support at the leading edge of the state-of-the-art.

TI's new NFET Family and BIFET products are available now at your nearest authorized TI distributor.

**For a free brochure on TI's NFET and BIFET products,** write to Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.

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|---|---|---|---|---|---|---|
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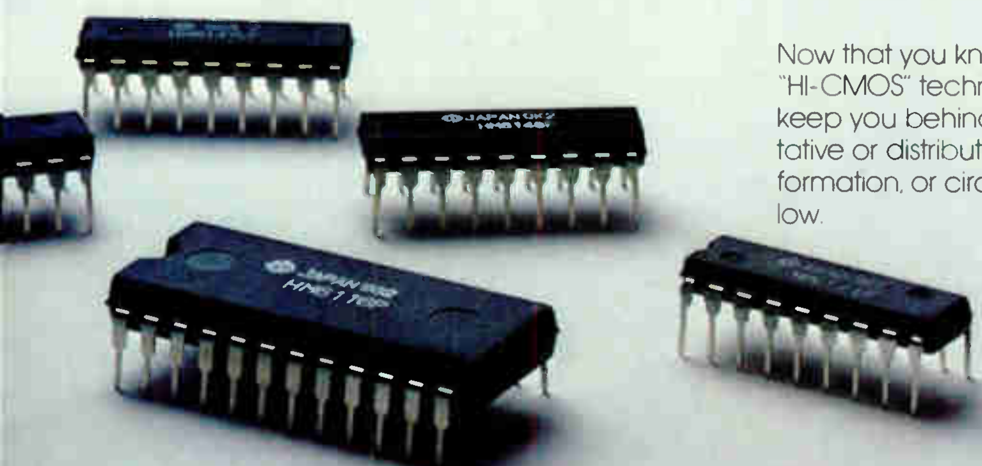
| HM 6147 | 4K x 1 | 55/70/85ns | 75mW | 60mW | 0.5mW | Now |
| HM 6148 | 1K x 4 | 55/70/85ns | 150mW | 60mW | 0.5mW | Samples |
| HM 4334 | 1K x 4 | 300/450ns | 20mW | 5mW | 0.5mW | Now |
| HM 4315 | 4K x 1 | 450ns | 20mW | 5mW | 0.5mW | Now |



Now that you know more about Hitachi "HI-CMOS" technology, don't let NMOS technology keep you behind. Call your local Hitachi representative or distributor sales office for complete information, or circle the reader service number below.

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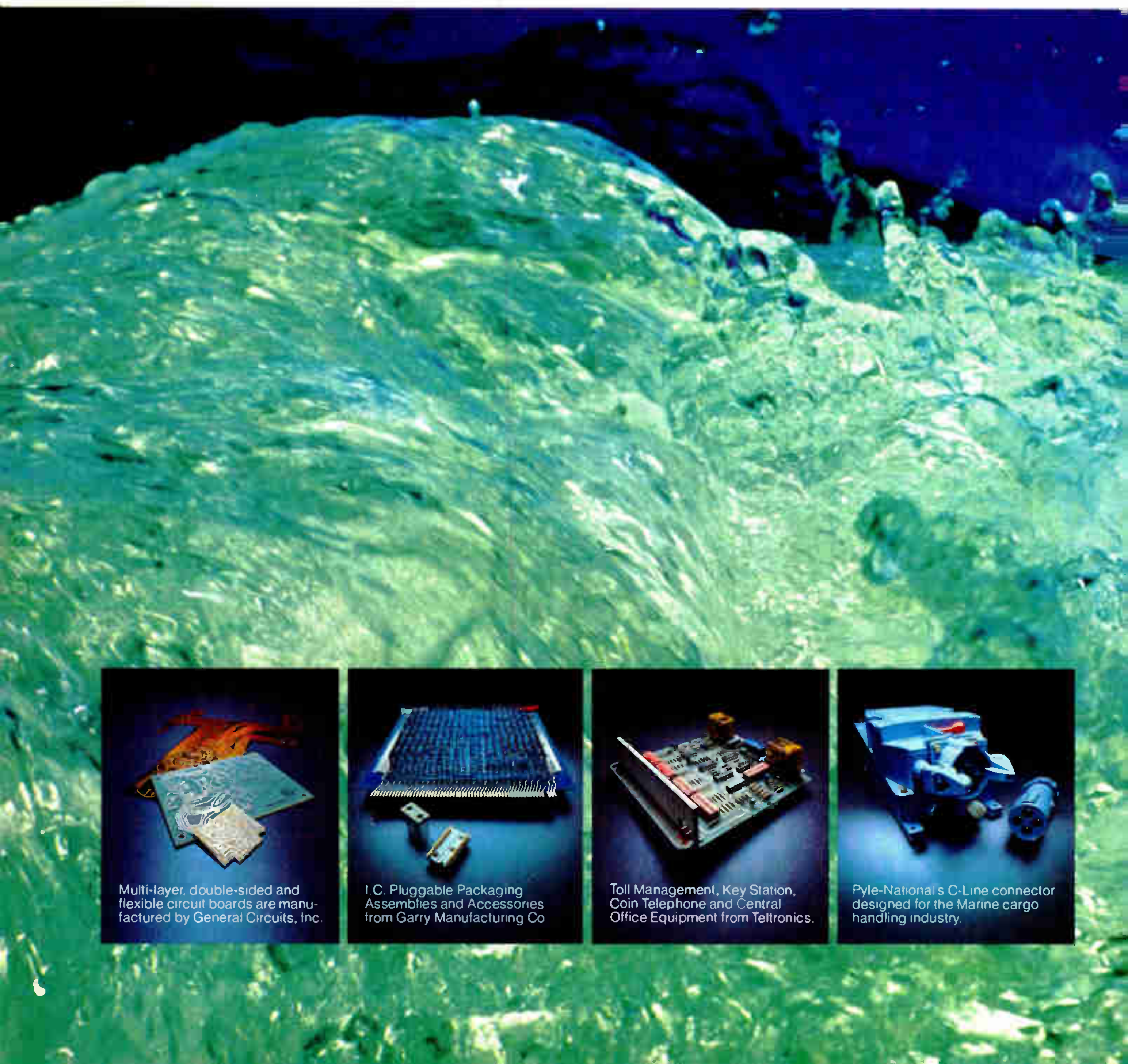

Multi-layer, double-sided and flexible circuit boards are manufactured by General Circuits, Inc.

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Data acquisition

# DPM chip has high accuracy

## 4½-digit a-d converter counts to ±20,000 to within ±1 count

Single-chip integrating analog-to-digital converters have made possible an entire generation of small and inexpensive digital panel meters and voltmeters. On the other hand, higher-precision DPMs and DVMs have for the most part relied on multichip a-d converter systems, thus becoming limited to larger sizes and higher prices.

Intersil has now changed this picture with what it claims is the first single-chip 4½-digit a-d converter offering a ±20,000-count (2.0000-V full-scale) display, yet requiring only an external reference, a clock, and a display with decoder-driver to make it a complete DPM system. With a multiplexed binary-coded-decimal output and six auxiliary input/output lines for interfacing with universal asynchronous receiver-transmitters and microprocessors, the ICL7135 offers flexibility as well as accuracy to within ±1 count. And it is economical, being priced at $22.50 each for single quantities, and $15 each for 100-lot quantities.

**Star qualities.** The ICL7135 has a number of high-performance features. It includes autozeroing and autopolarity, a guaranteed zero reading for a 0-V input, a true differential input, and true polarity at zero count for precise null detection. The chip requires a maximum of 1 pA of input bias current and exhibits less than 1 μV/°C of 0-V drift, while providing under- and over-range signals for autoranging. Also, the complementary-MOS device has TTL-compatible outputs.

Several of the dual in-line package's 28 pins have been reserved to allow it to be used in sophisticated measurement systems. For example, the pins for strobe, overrange, underrange, run/hold, and busy on the ICL7135 allow it to interface easily with such popular microprocessors as the 6800, 6500, MCS-43, 8080, and 8085, as well as with UARTs.

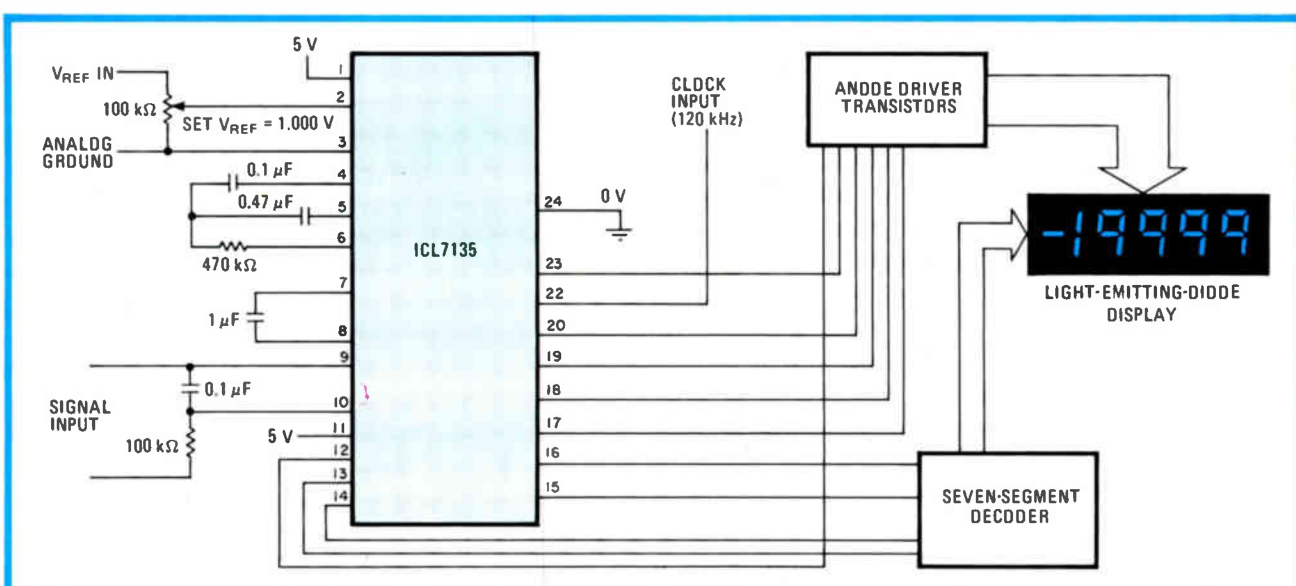
The ICL7135 requires ±5-V supplies, drawing a maximum of ±3 mA. However, where the input signal can be referenced to the center of the common-mode range of the converter and where that signal is less than ±1.5 V, a single +5-V supply suffices. The maximum clock frequency at which the dual-slope a-d converter operates is 1.2 MHz.

Two versions of the ICL7135 are available: the plastic ICL7135-CPL and the ceramic ICL7134-CDL. Both are designed to operate over the commercial temperature range of 0° to 70°C. Power dissipation is 1 W for the ceramic DIP and 0.8 W for the plastic part. The devices are available from stock.

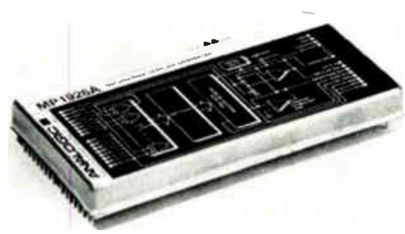
Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [381]

## $100 audio d-a unit has 18-bit linearity at zero crossover

Priced at less than $100 each in 1,000-unit quantities, the MP1926A 16-bit audio digital-to-analog converter module provides 18-bit linearity (±4 parts per million) for small signals in the zero-crossover region on a bipolar scale. With this converter, such complex analog waveform-reconstruction systems as digital audio playback systems can restore signals from digital data with better than −86 dB harmonic distortion and with less than 15 μV of noise injected into the audio band. Two models are currently available: the




**Complete.** With the ICL7135 4½-digit analog-to-digital converter, all that is needed to form a ±20,000-count digital panel meter with ±1-count accuracy are an external reference, a clock, and a display with decoder-driver. The unit interfaces with popular microprocessors.



MP1926A, which will settle in less than 3 μs to within 0.01% of a 5-V code-step input; and the MP1926S, which settles to 0.01% for a 5-V step input in less than 40 μs. The S model has a maximum range and offset temperature coefficient of ±5 ppm of reading/°C and of 0.5 ppm full-scale range/°C. Both units are available for delivery in 30 days.

Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617) 246-0300 [383]

## A-d converter chip runs a year on one 9-V battery

An analog-to-digital converter chip operates for 8,000 hours—nearly a year—on a single 9-V battery. The model ICL7126 is a lower-power version of the industry-standard ICL7106, a 3½-digit a-d converter that is the heart of a wide variety of hand-held digital multimeters, voltmeters, and thermometers. Based on complementary-MOS technology, the new converter includes seven-segment decoders, display drivers, reference, and clock. It interfaces directly with a liquid-crystal display and includes a backplane drive.

The device features guaranteed zero reading for 0 V on all scales, and has true polarity at zero for precise null detection. Autozero is less than 10 μV; zero drift is less than 1 μV/°C; input bias current is 10 pA maximum, and rollover error is less than one count. The device also features true differential input and reference.

The ICL7126's noise is less than 15 μA peak to peak and its power dissipation is guaranteed to be less than 0.9 mW. The converter is available from stock in 40-pin plastic or ceramic dual in-line packages, at a 100-unit price of $11.30 for the epoxy package.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [384]

## 8-bit data-acquisition chip with 16 channels costs $37.50

The DAS-952R is a single-chip, 16-channel, 8-bit data-acquisition system that costs $37.50 in quantities of from 1 to 24. It allows any one of 16 single-ended channels of analog information to be selected and digitized to 8 bits of resolution at a throughput rate of up to 17.5 kHz. The system is designed to inferface easily with microprocessors.

Monolithic complementary-MOS technology allows this system to be fabricated on a single chip and contained in a 40-pin plastic dual in-line package. It requires an external reference, clock, and connection to a power supply of +5 V at 1 mA maximum. The maximum unadjusted error for the system is ±½ least significant bit.

The unit's input multiplexer allows direct access to any of 16 single-ended analog inputs and provides the necessary logic for expanding the number of channels. Connection of the multiplexer output to the a-d converter input is by external pin connection. This permits easy input-signal conditioning.

Analog-to-digital conversions are performed on a ratiometric basis, the analog input signal level being digitally expressed as a fraction of the converter's full-scale voltage range. The full-scale range may be selected to go from 0.512 to 5.25 V and resolution may go from 2 to 20.5 mV. Latched and decoded channel address inputs, latched three-state TTL data outputs, and microprocessor-compatible control logic permit easy interfacing to microprocessors. The DAS-952R, says the manufacturer, features excellent performance over the −25° to +85°C temperature range. Delivery is from stock.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [385]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We start you off with a base salary that compares with any in the oil industry.

We also give you a cost-of-living differential in Saudi Arabia so that the higher costs of things like food come out of our pocket, not yours.

The best part is our premium for overseas employment. This is *fully* sheltered from all taxes.

We pay you a 40 percent premium on the first $30,000 of base pay—plus a 20 percent premium on the next $20,000. Maximum is $16,000 per year.

### Tuition and board anywhere in the world for high schoolers

High school students get their educations in Europe, the United States, anywhere. We pay 80 percent of all tuition and board (up to $4900 annually) for three years of high school.

We also pay air fare for high schoolers visiting parents in Saudi Arabia—three trips per year. (The same goes for air fares for college students but they get fewer trips.)

Youngsters from kindergarten through the ninth grade attend our American-style schools in Saudi Arabia.

### Free trip home every year—long vacations

You get 40 days of paid vacation every 12½ months — plus an average of 12 holidays every year—plus weekends.

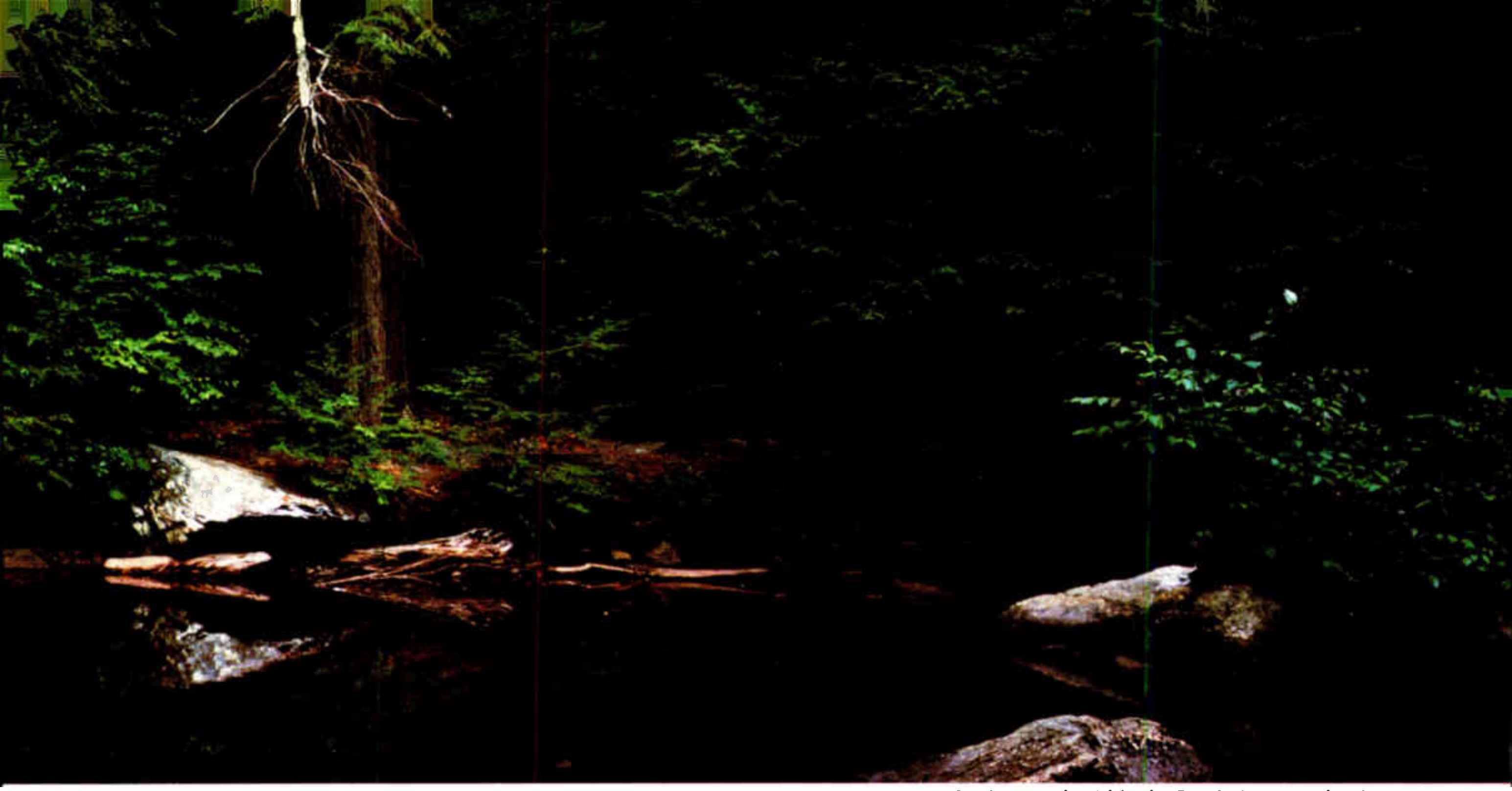
You get a travel allowance every year, too. This is equal to the economy round-trip air fare between Saudi Arabia and the U.S. or Canadian city where you were hired. Good for you *and* your family. Every year.

Where you go is your business. Is it any wonder that so many Aramco people get to see Europe, the Orient, the *world* on their annual leaves?

### Free life insurance and health care

You're automatically covered with a life insurance policy the day you join Aramco. No cost to you.

You can also buy extra insurance up to thirty times your monthly salary for about 34¢ a month for every thousand dollars.



*Will your retirement home be near some mountain greenery, or farther south within the Sun Belt, or on the shores of the Pacific? Aramco's big bundle of benefits will help you secure it sooner than you think. See below.*

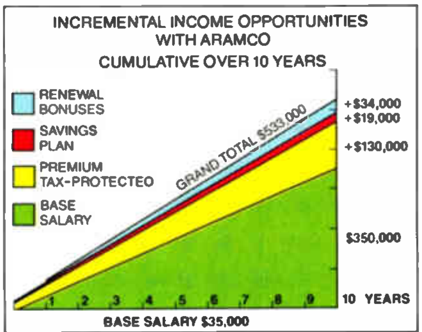
All your medical needs are free while you are in Saudi Arabia — even your prescriptions.

Unlike medical care, dental care is not free for Aramco employees. However, the costs are comparable to what you'd expect to pay back home.

### A chance to save huge sums of retirement money

We can only give you a bare idea of how the money can multiply over a 10-year span. For the sake of illustration, let's add up the fortunes of an engineer working for Aramco in Saudi Arabia making $35,000 U.S. in base pay, with no raises for the 10 years (not likely!). Remember this is just a hypothesis.

Right off, you see that our imaginary engineer in Saudi Arabia can gross




*This is not an offer or an indication of wage scales. It is merely a hypothetical example of how your gross income can accumulate dramatically when you work for Aramco in Saudi Arabia. Employees are not fully vested in the savings plan until 60 months of continuous service. All projections subject to change.*

around $183,000 more. The amount saved out of that grand total is strictly up to the individual.

But look at that $130,000 premium. Whatever the dollars work out to in your case, please remember that this is the bundle which is *totally* tax-protected.

This graph doesn't show what you save on medical expenses, it doesn't show the allowances on your children's education, it doesn't show the travel allowances which cut down on vacation costs, it doesn't show the retirement benefits you may accumulate.

What it does show is that you have the chance of a lifetime to save a really important amount of money.

### A sensible way to check out the new lifestyle

Everyone in Saudi Arabia lives within the letter of the local law. (No alcohol, for instance.)

But the Americans and Canadians eat steak and french fries, they go golfing and sailing and water-skiing, they tend their nice suburban houses.

While the lifestyle is easy, sometimes living so far away from relatives and friends can be difficult for some. That's why we've begun a new policy. The Aramco overseas tryout.

If you don't want to move your whole family over at once, come and work for us on bachelor status for one year. We'll fly you home three times so you can keep the family informed about your adjustment to life in Saudi Arabia. Then at year's end or sooner all of you can decide whether the life is for you or not.

### Take on job challenges you thought you'd never see again

Aramco is the world's largest oil-producing company. So the job opportunities for experienced engineers are boundless. You can stay within your specialty — or you can expand into new territories.

Here are the engineering job categories we're interviewing for right now.

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Inspection
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Resources Planning
Maintenance

(P.S. Our job opportunities are open to qualified engineers of *all* ages.)

*Interested?* Send your résumé in full confidence or write for more information to: Aramco Services Company, Department ELT092580MCLA
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**ARAMCO**
SERVICES COMPANY

Circle 187 on reader service card

# Introducing PMI's "On-The-Shelf" Hermetic, Ceramic Mini-dips

## *The Shelves are Always Well-Stocked in PMI's Linear Wonderland Stores*



"What is it you want to buy?" the Sheep said at last, looking up for a moment from her knitting.

"I don't quite know yet," Alice said. "I should like to look all round me first, if I might."

The shop seemed to be full of all manner of curious things—but the oddest part of it all was that, whenever she looked hard at any shelf, to make out exactly what it had on it, that particular shelf was always quite empty, though the others around it were crowded as full as they could hold.

Shopping for linear circuits in low-cost ceramic packages offers designers the same frustration Alice felt in this curious store in the Looking Glass world. No matter how many manufacturers say they have them "off-the-shelf," when you go to reach for them, that's exactly where they are. *Off* the shelf.

PMI has solved the problem with its new "Z-package." A ceramic mini-dip package at prices lower than TO-99 packages, into which we've put many of our most famous linear circuits, including both operational amplifiers and comparators.

Of course many people package linears in *plastic* mini-dips, for all those time-conscious Wonderlanders who want to save assembly time (and costs) by using automatic component insertion equipment. Thanks to our shelves *full* of the new Z-packaged mini-dips, now you can enjoy the speed of automation and still have the proven performance of PMI's products in **hermetic** packages. And we've got a lot *more* products to come in **hermetic** mini-dips.

You get auto-insertion capability, but also our famous triple passivation technique, the ease of storing and handling **hermetically-sealed** packages, elimination of the metal on top of other packages, which can cause shorts, and, not to be forgotten, prices so low you'd almost think the shelf was marked wrong!

Here's our latest inventory of circuits—including military—available right now *on the shelf* at all PMI Linear Wonderland outlets.

## OP AMPS

**OP-01-Z** *High Speed*—slews at 18V/μsec, settles to 0.1% in 1μsec.

**OP-02-Z** *Premium 741 Replacement*—offest voltage drift is low (10μV/°C); noise is less than 1μV, p-p (0.1-10 Hz.)

**OP-05-Z** *Superlative Low Signal Level Performer*—low drift (less than 1μV/month; less than 4.5μV/°C) without trimming.

**OP-06-Z** *Very High Voltage Gain*—an improved replacement for all 725 types; low drift (0.8μV/°C) coupled with minimum voltage gain of 1,000V/V.

**OP-07-Z** *Ultra-Low Offset*—offset voltage is less than 250μV (from 0°C to 70°C) without trimming.

**OP-14-Z** *Dual-Matched Pair*—enhanced version of the *1458/1558* types, it is pin-for-pin compatible, with matched $V_{OS}$ and CMRR, low noise and drift.

## COMPARATORS

**CMP-01-Z** *Fast Precise Response*—response time typically 100nS; input slew rate, 92V/μs.

**CMP-02-Z** *Low Input Current*—bias current less than 50nA; input offset current less than 1nA.

Now that you know how we stock our shelves at PMI, order a sample of the ceramic mini-dip linear you're looking for. Just fill out the "ON-THE-SHELF" order form below.

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Microcomputers & systems

# 8X300 family gets peripherals

## Controller and sector buffers for floppy-disk drives and I/O register array added

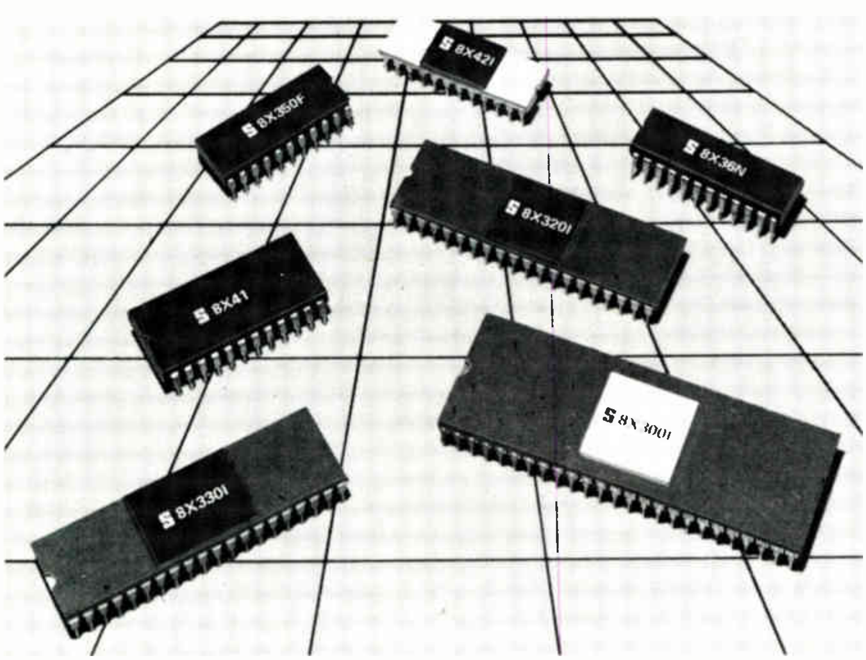
In the five years since Signetics introduced the first single-chip bipolar microcontroller, the 8X300, the trend toward intelligent input/output processors and serial data transmission has grown beyond the expectations of many. Attempting to keep pace with that growth, the company's Bipolar LSI division is expanding its 8-bit 8X300 family with a group of peripheral devices that includes a controller and a sector buffer for floppy-disk drives and an I/O register array.

Made with low-power Schottky TTL technology, the 8X300 is a fast (250-ns cycle time) fixed-instruction-set microprocessor that can perform 4 million operations per second and thus compares favorably with more complex bit-slice processors [*Electronics*, June 23, 1977, p. 113].

In such applications as magnetic-media controllers, high-speed modems, and data-communications controllers, the 8X300 reduces package count by half or more, as compared with other microprocessors and with small- and medium-scale TTL design approaches, notes Stan Bruederle, division marketing manager. The basic 8X300 has an 8-bit bus. Up to 512 devices can be selected using an additional left- or right-bank signal.

To exploit the capabilities of the 8X300, Signetics has developed the 8X330, a floppy-disk formatter and controller that uses integrated-Schottky-logic (ISL) technology and includes some unique features, Bruederle claims, "to give users a competitive edge in both simple and complicated disk-controller designs." The competitive advantage, he adds, is measurable in terms of system parts count, error-correction capabilities, and applications-oriented design concepts.

Except for an operational amplifier to act as a low-pass filter, "the 8X330 contains all the processing circuits and the required control logic to encode and decode double-density and single-density codes based on the IBM format," states Mike Janak, new products manager, standard products. "To permit the most flexible controller design," he continues, "we put into the 8X330's hardware those functions that are fixed and very fast, and all the things needed to enhance the flexibility are stored in the microprogram of the 8X330 microcontroller."




For example, modified frequency modulation (mfm) and modified mfm ($m^2fm$) encoding and decoding are stored in the 8X300's program, as are such ideas as the coding of address marks, the data-transfer rate, and the sector length. Built into the 8X330 is a data separator, precompensation and write logic, a phase-locked loop, a byte counter, and a cyclic-redundancy-check generator that includes software-controlled error correction for bursts up to 11 bits long.

Additionally, the 8X330 has 16 bytes of scratchpad random-access memory provided for storage of various control and status parameters. This small, general-purpose RAM can be accessed directly by the 8X300 and, Janak explains, is used to store system variables such as track address, sector address, and other necessary parameters. The device's 16 8-bit registers, he continues, "provide sufficient on-chip memory to accommodate a minimum of two disk drives."

Signetics also is making available a bus-interface register array, the 8X320, which is a dual-port RAM designed for use between a host and a peripheral processor, Bruederle says. Specifically, the input/output register array "provides a convenient and economical interface" between the 8X300 microcontroller (secondary port) and a user's host system (primary port), which can be almost any bus-oriented device.

In addition to containing two three-state bidirectional ports, the 8X320 array also provides simple handshake control via two 8-bit flag registers. What's more, it contains logic to facilitate direct-memory-access transfers for an 8086, an LSI-11, or other processors, and a write-protection feature for the primary port in both byte and word modes of operation.

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## New products

after receipt of order, the 8X320, 8X330, and 8X350—a 256-by-8-bit sector buffer RAM for floppy-disk drives—are priced at $26.10, $56.90, and $50 each, respectively, at the 100-piece level. All are available in 40-pin packages, and all operate from a single 5-V power supply.

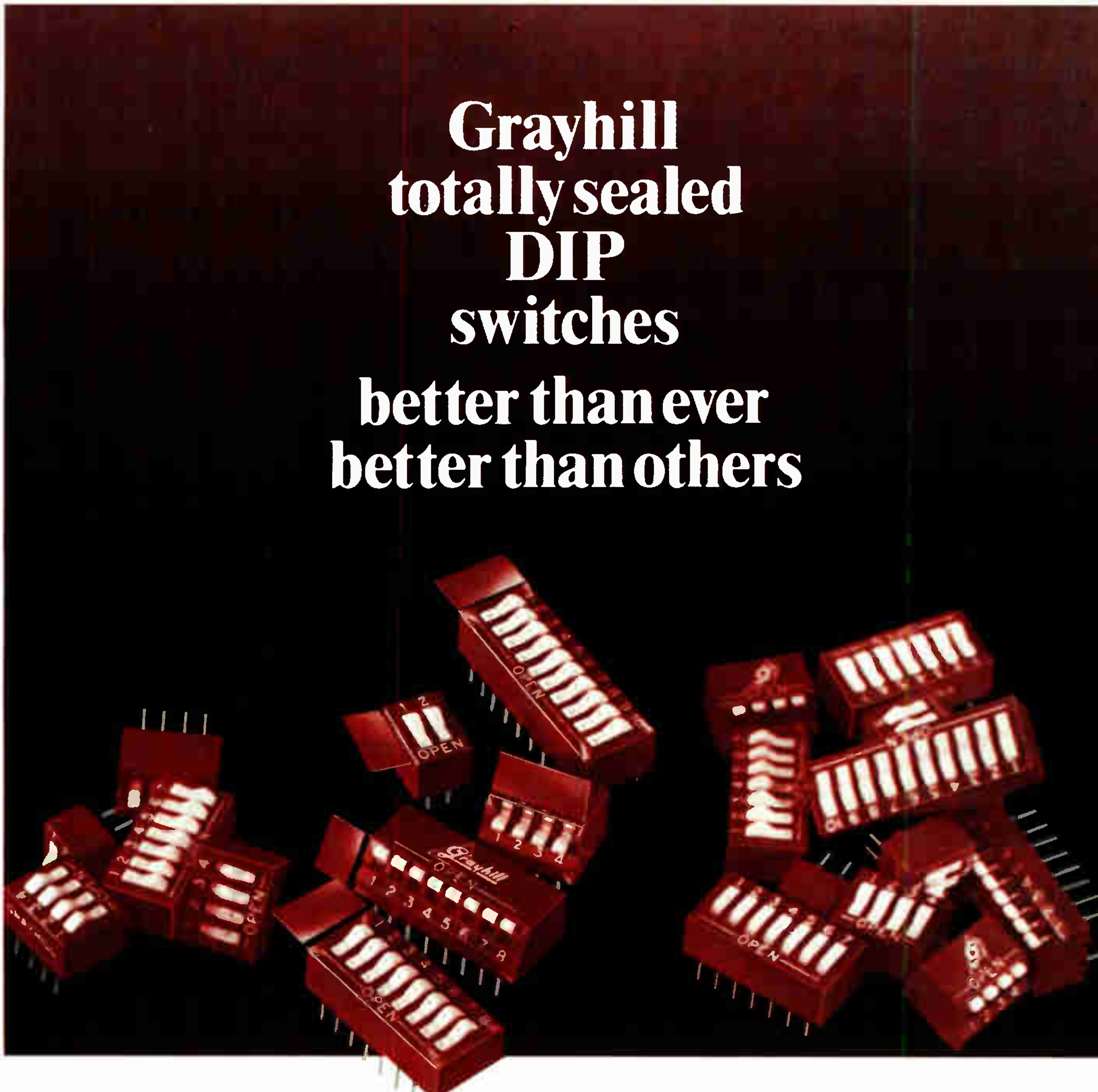
Signetics Corp., 811 East Arques Ave., P. O. Box 9052, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [371]

### Processing terminals stand alone or share store

Members of a line of four intelligent cathode-ray-tube terminals called video processing units can be tied together in daisy-chain fashion to share a central hard-disk file. One of the CompuStar terminals has no floppy-disk drive and so cannot stand alone, but the other three have from 350 kilobytes to 1.5 megabytes of floppy-disk storage capacity, and these units can perform on their own as microcomputer systems. All four have an internal microprocessor and 64-K bytes of dynamic random-access memory. An 8-bit parallel interface allows data transfer to and from a central disk at 1.6 Mb/s.

Three central disk storage systems are offered: a 10-megabyte 8-in. Winchester drive and cartridge module drives from Control Data Corp. with 32 or 96 megabytes of total capacity. Each central store system includes Intertec's disk controller and multiplexer circuitry that ties individual terminals into the common system. Single-unit terminal prices range from $2,495 to $4,995; the Winchester drive is $3,995.

Intertec Data Systems, 2300 Broad River Rd., Columbia, S. C. 29210. Phone (803) 798-9100 [373]

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## New products

### Multiplexer, interface, and software enhance microNova

Three new communications products enhance the flexibility and hardware support of the microNova MP/100, MP/200, and microNova board computer line. An asynchronous/synchronous line multiplexer (model 4336-S) has four serial-communication lines with modem control.

Each line is independently programmed and supports either character-controlled synchronous protocols (including IBM Bisync) or asynchronous communications. The multiplexer can operate at 19,200 b/s in either mode. It sells for $750. A four-line asynchronous interface (model 4336-AS) sells for $600; its RS-232-C lines have fully programmable characteristics and operate at a maximum transmission rate of 19,200 Mb/s.

The third product is the MP/OS synchronous communications software package, which supports up to eight synchronous communications lines, as well as the multiplexer on microNova computers and the SLM, ULM, and CSI communication products in the Nova 4 product line. Initial license is $500, with $100 for run time. All products are on a 90-day delivery schedule.

Data General Corp., Rte. 9, Westboro, Mass. 01581. Phone (617) 366-8911 [374]

### Math card adds fixed-point, transcendental functions

The iSBX 331 fixed- and floating-point math card joins Intel's family of Multimodule options for its single-board computers [*Electronics*, April 10, p. 135]. Running at 4 MHz with an on-board crystal clock, the 331 performs a 32-bit floating-point multiplication in 42 μs, compared with the iSBX 332's 50 μs, and adds 16-bit and 32-bit double-precision fixed-point math and transcendental functions—trigonometric, logarithmic, and exponential. The 331, how-

ever, does not meet the proposed IEEE floating-point math standard, as the 332 does.

Consuming only 2.73 W, the 6.35-by-9.40-cm (2.5-by-3.7-in.) card plugs into the iSBX bus connector on such microcomputer boards as the iSBC 80/108 and 80/24, increasing the computer board's height by 2.86 cm (1.13 in.). It uses Intel's 8231 arithmetic processing unit, a chip fabricated in the firm's high-performance HMOS process. The card's U. S. price is $415 in quantities of 10 to 24.

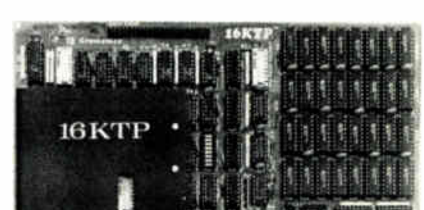
Intel Corp., 5200 N. E. Elam Young Pkwy., Hillsboro, Ore. 97123. Phone Mary Slamp (503) 640-7147 [375]

## Two-port boards store high-resolution images

Two two-port memory boards have been designed for use with Cromemco's SDI color graphics interface. This interface can be used to display images with a resolution of 754 by 482 points on a red-green-blue monitor. Storing 16-K bytes (the 16KTP) or 48-K bytes (the 48KTP), the memory boards have two sets of address and data lines so they can process the SDI's memory-refresh requests while the central processor simultaneously and independently executes a user program.

Full utilization of all options of the company's graphics software package requires two pages of 48-K bytes each. The two-board SDI interface is priced at $595; the 16KTP and 48KTP cost $795 and $1,785, respectively. The graphics software is $295 on floppy diskette.

Cromemco Inc., 280 Bernardo Ave., Mountain View, Calif. 94043. Phone (415) 964-7400 [376]



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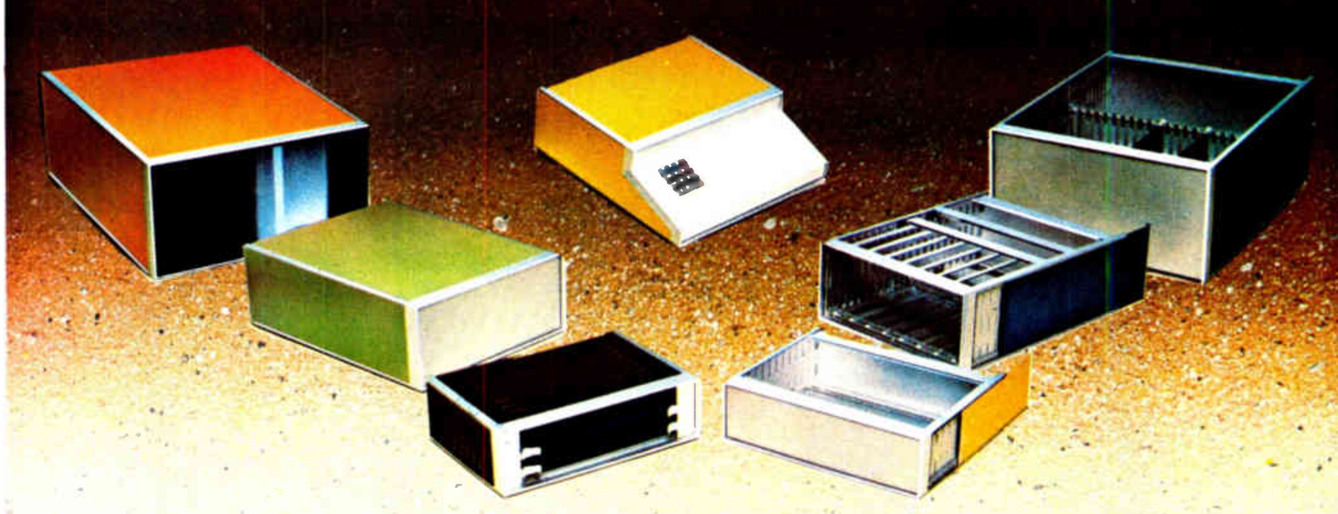

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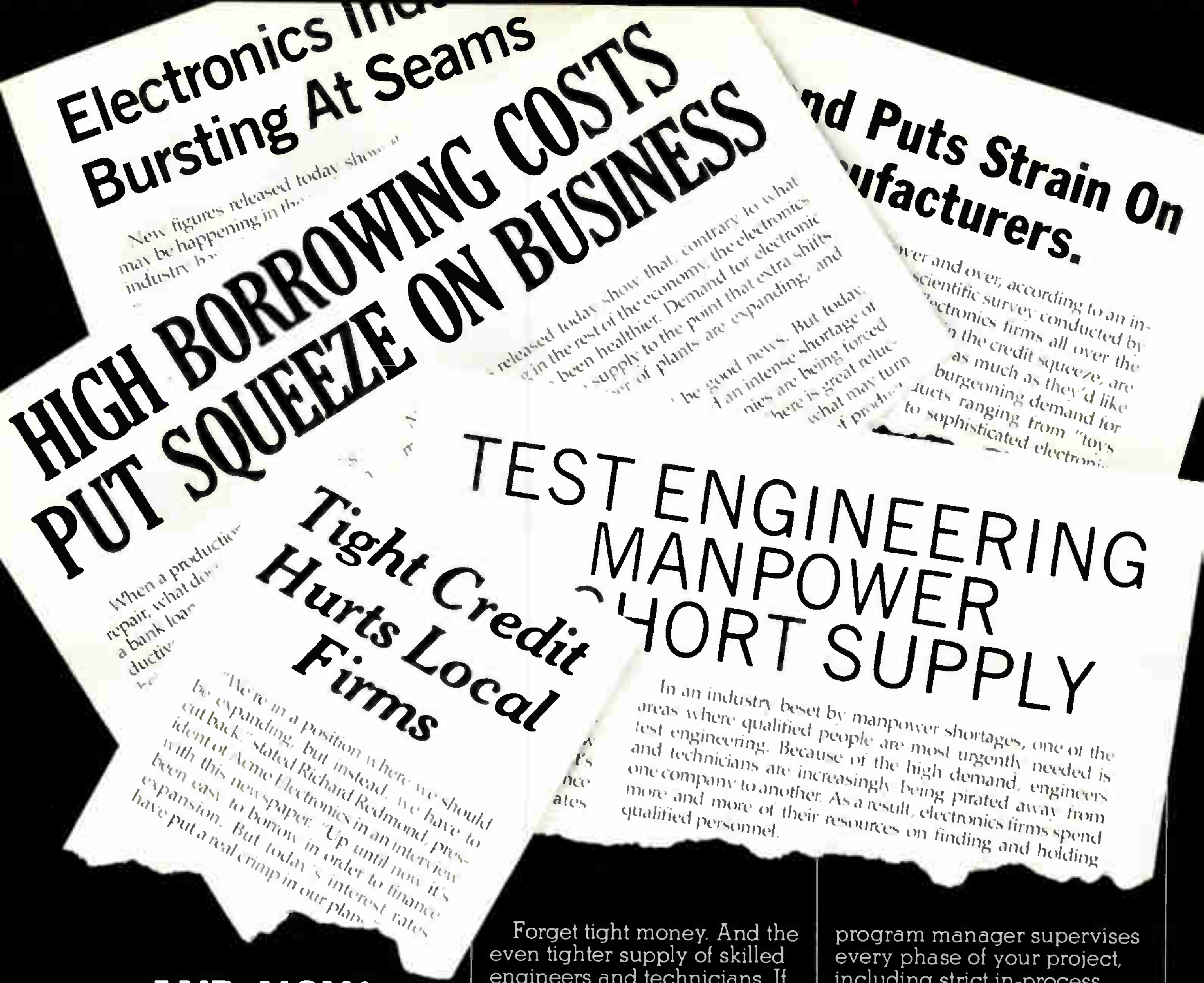


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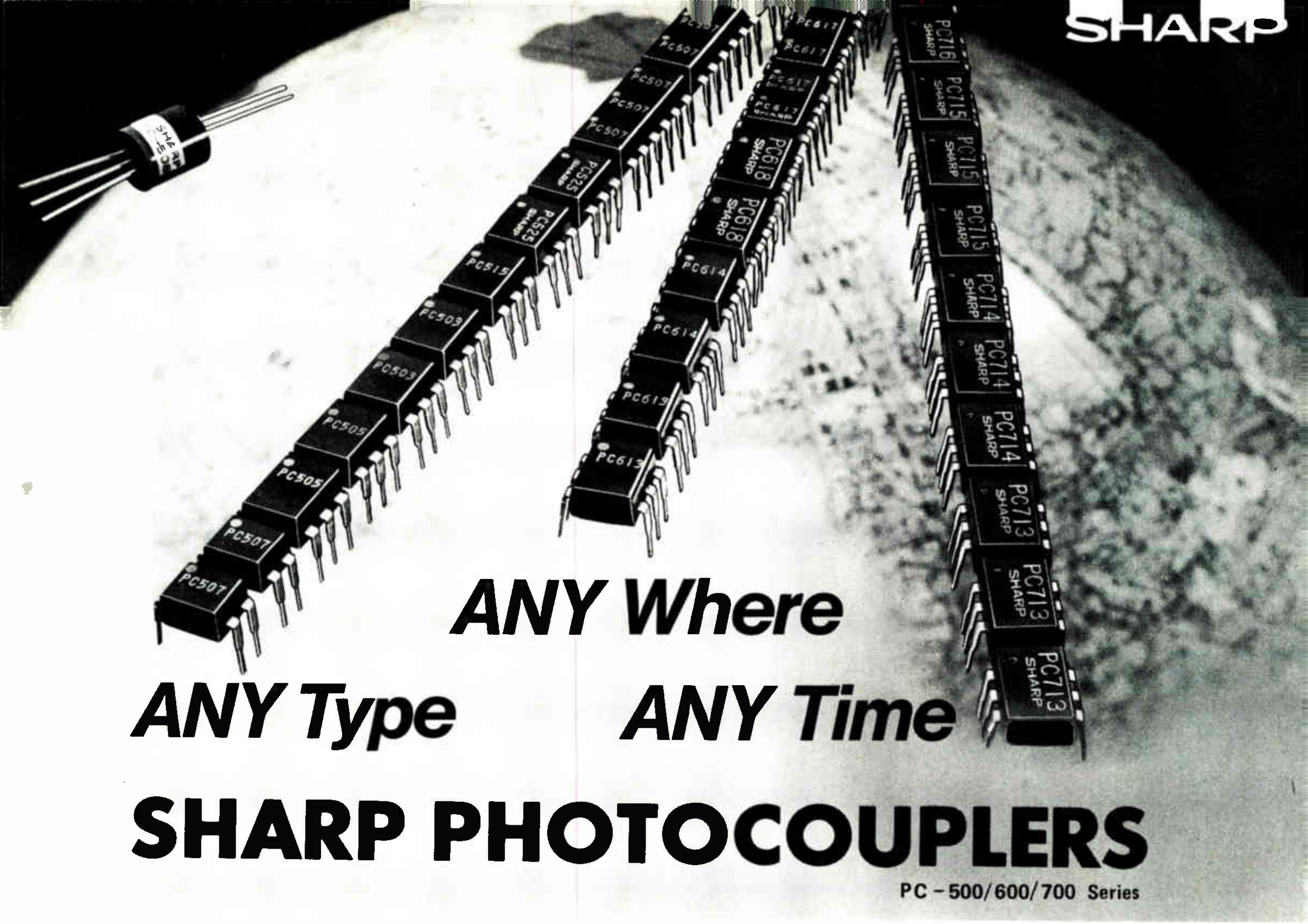

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| | | IF (mA) | $V_{CEO}$ (V) | $P_{tot}$ (mW) | $V_{ISO}$ (kV) | (%) TYP. | $V_{CE}$ (V) | $I_F$ (mA) | tr (μs) TYP. | $I_C$ (mA) | $R_L$ (Ω) |
| PC-508 | Tubular 5P (base) | 50 | 45 | – | 5.0 | 67 | 5 | 30 | 6.0 | 1 | 100 |
| PC-525 | DIP 6P (Darlington) | 70 | 200 | 350 | 1.5 | 600 | 2 | 5 | 25 | 20 | 100 |
| PC-627 | DIP 8P (2 ch) | 70 | 35 | 200 | 2.0 | 120 | 5 | 5 | 4.0 | 2 | 100 |
| PC-637 | DIP 12P (3 ch) | 70 | 35 | 200 | 2.0 | 120 | 5 | 5 | 4.0 | 2 | 100 |
| PC-713 | DIP 6P | 50 | 35 | 170 | 5.0 | 100 | 5 | 5 | 4.0 | 2 | 100 |
| PC-714 | DIP 6P | 50 | 35 | 170 | 5.0 | 100 | 5 | 5 | 4.0 | 2 | 100 |
| PC-715 | DIP 6P | 50 | 35 | 170 | 5.0 | 1,600 | 2 | 1 | 60 | 10 | 100 |
| PC-716 | DIP 6P | 50 | 35 | 350 | 5.0 | 3,000 | 2 | 1 | 130 | 20 | 100 |
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Communications

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## Microwave generator and digital receiver can cover 3,600 telephone channels

The latest generation of white-noise measuring sets from W&G Instruments takes much of the tedium out of testing the linearity and intermodulation performance of microwave radio-link systems in telecommunications—normally time-consuming and boringly repetitive procedures.

Moreover, by offering a frequency bandwidth from 6 kHz to 25 MHz, the RK-25 and RKS-25 become the only sets of their kind capable of testing the newer microwave radio systems whose basebands go beyond the previous 13-MHz upper limit. In fact, with its broad frequency range, the units cover up to 3,600 telephone channels, giving them reserve capability for additional baseband requirements in systems yet to come. They and their filters conform to the latest Intelsat, AT&T, CCITT, and CCIR recommendations.

Intended for use by operators of both telephone and military microwave radio systems, the automated units are also useful in the computer-controlled manufacture of radio systems. They are programmable by the IEEE-488 bus. Mathematical computations are all done within a measuring set, not by the operator, as is the case with other such systems. Also, the traditional analog meter display is replaced by a digital readout that further simplifies the measurement procedure for manual operation.

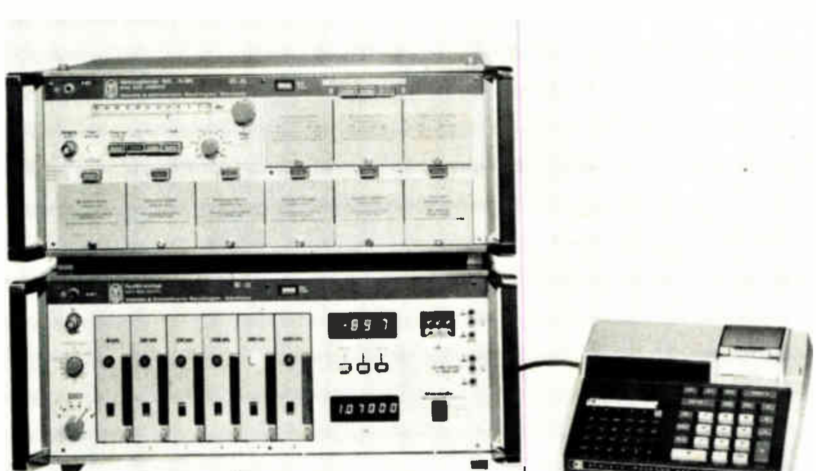
The RK-25 programmable white-noise measuring set consists of the RS-25 white-noise generator and the RE-25 white-noise digital receiver. The two units can be connected and operated as slave and master. There is a push-button choice of noise display (dBmOp, dBrnCO) or of the noise-power-ratio (NPR) display. Also, an option is available that allows noise power to be read out directly in picowatts as well as decibels. For NPR measurements, the generally needed reference alignment is done automatically after the push button has been depressed.

The RK-25 white-noise measuring set may be interfaced with Hewlett-Packard's HP 97S preprogrammable and printing desktop input/output calculator using W&G's RKS-25 test program. Used this way, the measuring and indicating modes, channel and band-limiting, and "send" levels are automatically selected and sequenced. There is also provision for recording the measured data and the I/O reference values.

For noise measurements, the RK-25 ranges from −89.8 to −30.1 dBmOp or from 0.1 to 59.8 dBrnCO. The range of NPR measurements is from 20.1 to 79.9 dB (or optionally from 1 to $10^6$ pW). All measurements are made to 0.1-dB resolution. Relative power may be measured over −69.8 to −10.1 dBr and the reference level can be set from −79.9 to −20.0 dBmOp.

The basic RK-25 measuring set package starts at $13,000; the RKS-25, which includes the HP 97S and software, costs an additional $4,600.

W&G Instruments Inc., 119 Naylon Avenue, Livingston, N. J. 07039. Phone (201) 994-0854 [401]



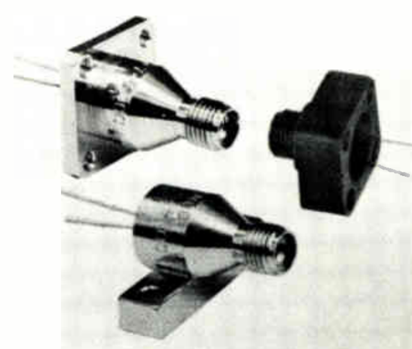
## Errorless modem lets terminals operate on unconditioned lines

The Micro5000 high-speed modem series lets minicomputers and asynchronous dumb terminals operate error-free at 2,400, 2,800, or 9,600 b/s on standard, unconditioned leased telephone lines without any changes in existing hardware or software. It provides automatic retransmission on error and can deliver error-free transmission on telephone lines with error rates worse than 1 in $10^4$ and through line outages of several seconds. The 10-lb modem is designed for easy installation and troubleshooting by untrained personnel. Prices range from $5,500 for the 9,600-b/s model down to $1,500 for the 2,400-b/s unit. Quantity discounts are available, and delivery takes 60 days.

Micom Systems Inc., 9551 Irondale Ave., Chatsworth, Calif. 91311. Phone (213) 882-6890 [403]

## Emitters and detectors have rise times of 10 to 200 ns

The E-1000 series of emitters consists of diodes that emit light in the visible and infrared regions, with rise times ranging from 200 to under 10 ns. The infrared light-emitting diodes come in a slow version with 200-ns rise time and a medium-speed, 15-ns version. A visible-red



LED has a rise time of 15 ns, and a 1.06-μm-wavelength LED's figure is under 10 ns. The LEDs are mounted in SMA or AMP connectors, optically centered for direct interfacing with fibers or bundles of from 200 μm to 2 mm in diameter.

The E-5000 series of detectors also consists of four devices: a low-noise, low-speed p-i-n diode with 50-ns rise time and another with 10-ns rise time; a photo-Darlington transistor; and a germanium photodiode with a 20-ns rise time for use in the IR region up to a wavelength of 2.0 μm. Also available in either SMA or AMP connectors, the series will mate with fibers or bundles from 65 μm to 2 mm in diameter. Prices for most units in single quantities are under $30; in 100-unit quantities prices are usually under $20.

Math Associates Inc., 6 Manhasset Ave., Port Washington, N. Y. 11050. Phone (516) 944-7050 [404]

## Extended-interaction amp puts out 1 kW at 95 GHz

An extended-interaction amplifier—the VKB-2400T—delivers a 1-kW minimum peak power output with a 30-dB minimum gain at 95 GHz. The 90-in.$^3$, 15-lb amplifier provides excellent phase stability, according to its manufacturer, and has demonstrated up to 2.3 kW of peak power at 95 GHz. Its operating life is expected to exceed 5,000 hours, although the unit is guaranteed for 1,000 hours of operation.

The amplifier was developed for military requirements. It has a 200-MHz (3-dB) instantaneous band-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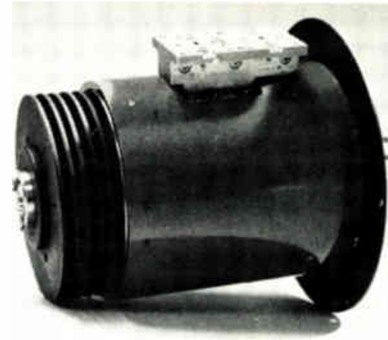

width and a mechanical tuning range of 1 GHz. Nominal pulse length is 10 $\mu$s, with a pulse voltage of 13 kV. Beam voltage is 21 kV; peak beam current is 650 mA. The VKB-2400T is priced at $55,000 per single unit, and delivery takes eight to nine months.

Varian Associates, Electron Device Group, Varian Canada Inc., 45 River Dr., Georgetown, Ontario, Canada L7G 2J4 [405]

## Multiplexer and modem handle 8 synch/asynch channels

A data-transmission system, model MTS-1, combines the Timeplex series II Microplexer statistical multiplexer and a 9,600-b/s modem in a single compact package that can multiplex up to eight asynchronous or synchronous channels. The series II Microplexer, introduced last year, transmits and receives data from up to 24 asynchronous or bisynchronous sources. The MTS-1 permits parameter programming on a per-channel basis, so that many different types of terminals, printers, and other peripheral devices can share a single telephone line.

The transmission system allows local and remote diagnostics at both the channel and data-link levels. It features functional displays and, in the event telephone-line degradation prevents operation at higher rates, it falls back to 4,800 b/s. The system is available in a four-channel configuration for $7,350 and in an eight-channel version for $7,950.

Timeplex Inc., One Communications Plaza, Rochelle Park, N. J. 07662. Phone (201) 368-1113 [406]

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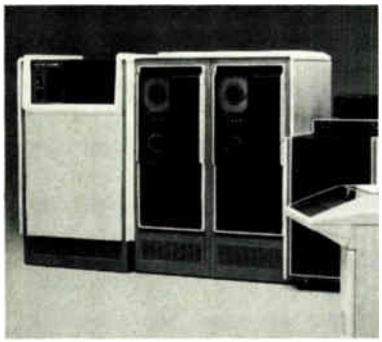

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Semiconductors

# SPI makes own power MOS FETs

## Hexagon-structured devices feature breakdown ratings of 350, 450, and 500 V

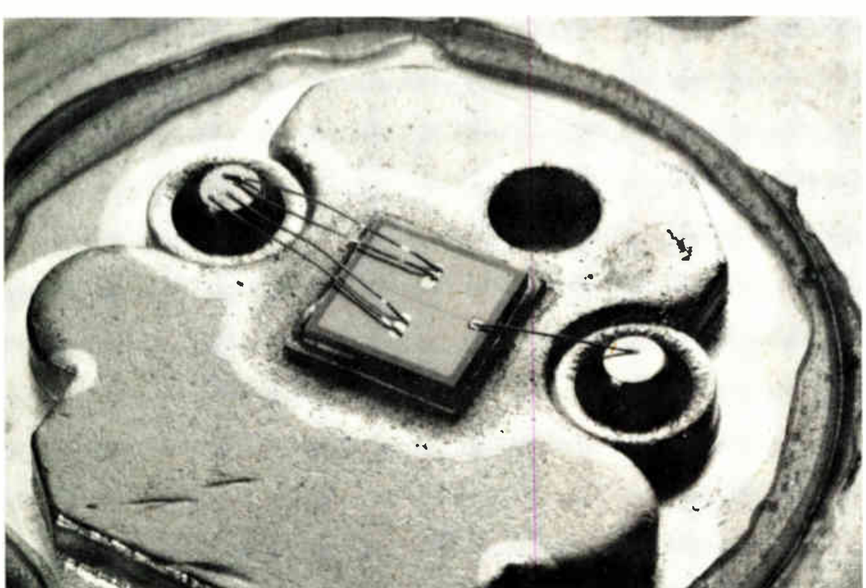
Traditionally a supplier of custom wafer-processing services, Semi Processes Inc. recently put a toe into the semiconductor-device waters when it began second-sourcing Signetics' double-diffused MOS product line [*Electronics*, Jan. 31, p. 129]. Now, apparently pleased with the temperature, the firm has plunged in, having developed a group of proprietary D-MOS products. The first are three families of high-power field-effect transistors for power switching, regulating, and amplifying applications.

The new families of power MOS FETs are fabricated with a silicon-gate, self-aligned vertical D-MOS process that, according to Thomas P. Cauge, D-MOS product manager at SPI, is not much different than others, with one major exception. "We have optimized diffusion profiles to minimize secondary breakdown effects," he explains. Among other things, the process changes the thickness of the epitaxial layer and thus its resistivity in order to produce devices with "much lower on-resistance and with higher current," he claims.

**A hex on it.** Furthermore, the basic channel geometry of the n-channel, enhancement-mode devices, designated the SD1000, SD1100, and SD1200 series, is a hexagon structure, similar to the Hexfet design pioneered by International Rectifier Corp. [*Electronics*, Dec. 20, 1979, p. 126]. However, Cauge says, "we use a different method of current flow, and different channel spacing [than the Hexfet] to minimize parasitic resistance and optimize breakdown voltage."

In addition to the 350- to 450-V power FETs it is developing, SPI is also focusing its attention on higher-voltage (500-V and up) devices with less demanding performance specifications, for which "there are markets with more immediate application opportunities," Cauge says. For example, the SD1200 series has a specified breakdown voltage of up to 500 V, a drain-source off leakage current ($I_{DSS}$) of up to 30 mA, and an on-resistance of less than 500 Ω.

"There are many high-voltage applications where current drive and on-resistance are not important, and these areas have been overlooked," he explains. Such applications include high-voltage test equipment and high-voltage drivers for electrostatic printers and other low-current, high-voltage peripherals.



The 1200 series, which includes the 1200 and 1201, with breakdown ratings of 500 and 450 V, respectively, also can be driven by standard TTL devices. Because of this logic compatibility, Cauge sees the series replacing "journeyman bipolar devices." The principal advantages over bipolars are that "the D-MOS devices are simpler to use because they require less drive circuitry," and, he says, "they are a more reliable part because they won't latch, as will bipolar devices, if breakdown does occur."

The SD1100 series is also specified with a breakdown voltage of up to 500 V, but with an $I_{DSS}$ of up to 1.0 A and an on-resistance of less than 10 Ω. It is targeted at the telecommunications market, in particular, but also at medical electronics applications, notes Cauge. The resistance and voltage values were "chosen with relay replacement in mind, particularly reed relays, as well as replacing some solid-state relays or being used in them," he states.

**Telephone target.** One of the power devices, the SD1101, has a specified breakdown voltage of 300 V that is expected to satisfy the needs of domestic telephone companies that use an 80-V ringing voltage and a 48-V battery backup. For the higher-voltage needs of the European telephone markets, as well as domestic phone companies and medical electronics manufacturers concerned about surge-protection circuitry, SPI offers another device, the 1100, specified at 450 V minimum breakdown voltage and 500 V typically.

Finally, SPI's SD1000 is aimed at the switching power-supply market. Specified at 450-V breakdown, this MOS FET can handle up to 10 A and offers an on-resistance of less than 1.0 Ω—typically 0.7. "Other suppliers offer D-MOS power FETs with lower voltage and higher on-resistance specifications that generally are good for power supplies of 1 kW or less," Cauge points out; the SD1000 "allows us also to get into the market


We speak connectors.




for power supplies greater than 1 kw."

The SD1000, available in a TO-3 package, is priced at $9.50 apiece in 100-piece quantities. In like amounts, the SD1100 costs $3.00 each in a TO-39 (medium-power) package, and $2.85 in a TO-18 (small-signal) package; the 1101 in those same packages is priced at $2.40 and $2.25, respectively. The SD1200 and 1201, available in TO-18 packages only, cost $1.05 and 90¢, respectively. Availability of all parts is 30 days after receipt of order.

Semi Processes Inc., 1885 Norman Ave, Santa Clara, Calif. 95050. Phone (408) 988-4004 [411]

## C-MOS circuit assigns time slots

The MC14418 is a programmable time-slot–assigner circuit incorporating features the manufacturer says will simplify hardware design for central-office and private-branch-exchange digital switching. The line-circuit control device is intended to operate at rates up to 2.56 MHz, to handle 0 to 64 time slots per frame, and for use with a 5- to 16-V power supply. Some of the control functions offered include ring enable, ring trip, power down, and tone and data control. The unit requires 60 mW maximum active power and approximately 1 mW when powered down. The MC14418 in a standard 22-pin ceramic dual in-line package is $8.80 each in quantities of 100 and more. A plastic version is available for $7.50.

Motorola Inc., MOS Integrated Circuit Division, 3501 Ed Bluestein Blvd., Austin, Texas. Phone (512) 928-6237 [415]

## Counter/timer-I/O chip matches patterns too

The Z8036 Z-CIO device, a general-purpose peripheral circuit that combines counter/timer, parallel input/output, and interrupt controller functions, is now available in sample quantities. The CIO contains three I/O ports—two independent, double-buffered, bidirectional 8-bit ports and a special-purpose 4-bit port. Sophisticated pattern-matching logic designed into the ports makes them useful for interrupt generation. The chip also has three independent 16-bit counter/timers, each with up to four external access lines.

Two versions of the CIO allow interfacing with virtually any microprocessor. The model Z8036 is designed for multiplexed address-and-data bus structures such as that of the 16-bit Z8000; the model Z8536 is intended for nonmultiplexed microprocessors such as the 8-bit Z80.

Samples are priced at $29.25 each in quantities of from 10 to 99. Production quantities will be available next month.

Zilog, 10340 Bubb Rd., Cupertino, Calif. 95014. Phone (408) 446-4666 [414]

## Controller handles data links for 8-bit microprocessors

The S6854 advanced data-link controller for S6800 and other 8-bit parallel-bus microprocessors performs communication link functions for the Advanced Data Communication Control Procedure (ADCCP), High-Level Data-Link Control (HDLC), and Synchronous Data-Link Control (SDLC) standards. The S6854 provides the data-communications interface for primary and secondary transmitting stations in stand-alone, polling, and loop configurations. Among the controller's functions are automatic flag detection and synchronization; zero insertion and deletion, extendable address control, logical control-field generation, variable–word-length (5- to 8-bit) field provision, and automatic frame-sequence generation and checking. The device also detects and transmits an abort or idle control bit when the first-in–first-out transmitter register is empty. Data-transmission rates as high as 1.5 megabits per second are possible with the S6854


# 48 TO 96

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Our LAM 4850 is the only logic analyzer that won't force you to buy, borrow or add-on to expand your analyzing capability to 96 channels. The power is already there. The flexibility is there. With a new channel expansion probe, the world's first 48-channel logic analyzer can be easily extended to an unrivaled 96 channels.

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For more information circle #129

For a demonstration circle #215

operating at a 1-MHz clock rate. The S68A54 version has a 1.5-MHz clock rate. U.S. pricing in quantities of 100 to 999 in 28-pin plastic packages is $17.40 each.

American Microsystems Inc., 3800 Homestead Rd., Santa Clara, Calif. 95051. Phone (408) 246-0330 [416]

## Sample-and-hold amplifier is accurate to within 0.015%

The SMP-11, a data-acquisition sample-and-hold amplifier, features accuracy to within 0.015% and a low combined offset voltage and step-transfer error of 0.45 mV. The device employs a diode-bridge switch design that minimizes charge-transfer errors. Typical acquisition time is 3.5 $\mu$s and slew rate is typically 10 V/$\mu$s. A transconductance amplifier enhances the diode-bridge switch during acquisition by providing up to 50 mA of charging current to the hold capacitor. It turns off as the sample-and-hold amplifier acquires the signal, charging the hold capacitor with minimum noise.

Because it uses a bipolar Darlington amplifier input stage, the SMP-11's droop current decreases for temperatures up to 70°C or more. The unit has a 50-ns aperture time, holding-mode settling time of 1.5 $\mu$s, a sample-current–hold-current ratio of $1.7 \times 10^8$, and compatibility with diode-transistor logic, TTL, and complementary-MOS logic.

In 100-piece quantities, the SMP-11 ranges in price from $4.50 to $17.50 in a commercial version and from $22.35 to $42 in a military version. Availability is from stock.

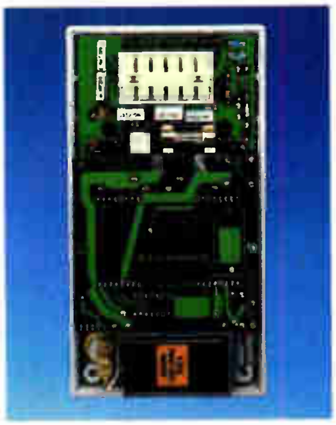
Precision Monolithics Inc., 1500 Space Park Drive, Santa Clara, Calif. 95050. Phone (408) 246-9222 [417]


# Beckman's new digital multimeter is ready to handle any job you are.

Continuity checks. High current measurements. In-circuit resistance measurements and semiconductor tests. Whatever the job, if a multimeter is called for, call for a new Beckman digital multimeter.

There are three models to choose from with a price tag as low as $140.

All three feature Insta-Ohms™ quick continuity indicator, (exclusive to Beckman digital meters), 10-amp current ranges, in-circuit measurement capability in all six ohm ranges, a dedicated diode test function, and up to two years normal operation from a common 9V battery.



The Model 3020 has seven functions, 29 ranges, and 0.1% Vdc accuracy for just $170.

For just $140, there's the Model 3010 which has all the features of the 3020, but with Vdc accuracy of 0.25%.

Or, for measuring noisy, non-sinusoidal signals, there's the Model RMS 3030. It features true RMS (ac and dc) voltage and current measurement capability with 0.1% Vdc accuracy for only $200.

And every Beckman meter uses band-gap reference elements, thin-film resistor networks, gold switch contacts and custom designed CMOS LSI chips to assure long-term accuracy and reliability.

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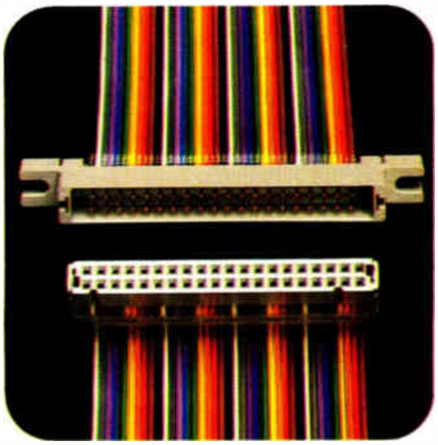
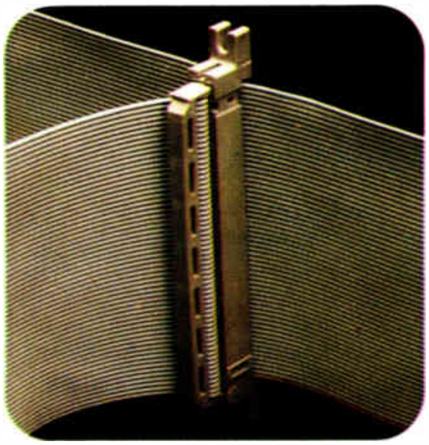
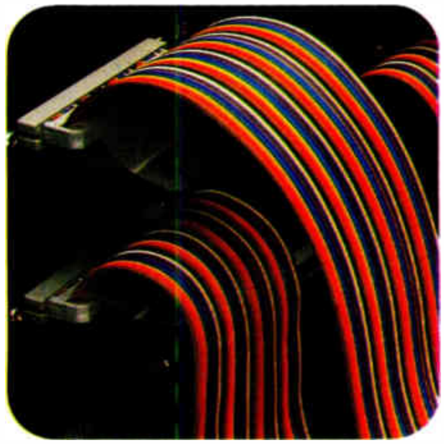

Scotchflex® brand plug connectors bring the proved labor-saving of mass termination to T-taps, splices and I/O interfaces. Designed to give you pin configuration continuity in both mid-span and rack and panel applications, Scotchflex plugs are compatible with all socket connectors in the complete Scotchflex line.

**Positive polarization.**
The design of Scotchflex plug connectors includes two channels in the sidewall. When our polarizing keys are inserted, the plug may be mated one way, and only one way, with its corresponding Scotchflex socket. So you get positive polarization, without the loss of an electrical position. Excellent socket retention. And you eliminate the possibility of equipment damage due to misalignment.


**Now up to 60 positions.**
To meet your specific design needs, Scotchflex plug connectors are available in 10, 20, 26, 34, 40, 50 and 60-pin sizes, with mounting flanges for panel mounting or without for T-tap or splice applications. Strain relief clips are also available.

**There's only one source.**
The 3M Scotchflex line offers you the widest choice of mass terminating connectors, cable and system components. Plus proven reliability. Off-the-shelf availability through a nationwide network of distributors. And the unmatched experience of the people who pioneered the concept of electronic mass termination.

Scotchflex connectors are recognized under the component program of Underwriters Laboratories, Inc.

"Scotchflex" is a registered trademark of 3M.

## Scotchflex® systems from 3M. The source.

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Circle 221 on reader service card

Instruments

# Bare-board tester can change tunes

## Modular hardware, software adapt to many boards and test environments

With increasingly dense multilayered printed-circuit boards making visual inspection a thing of the past, Teradyne Inc. is launching a bare-board tester that is intended to be flexible enough to fit nearly any test environment. Modular hardware and software adapt the N221 system to a host of different boards, test parameters, fixturing schemes, and testing loads, says Roger S. Saylor, manager of interconnection-verification products for the Boston, Mass., company.

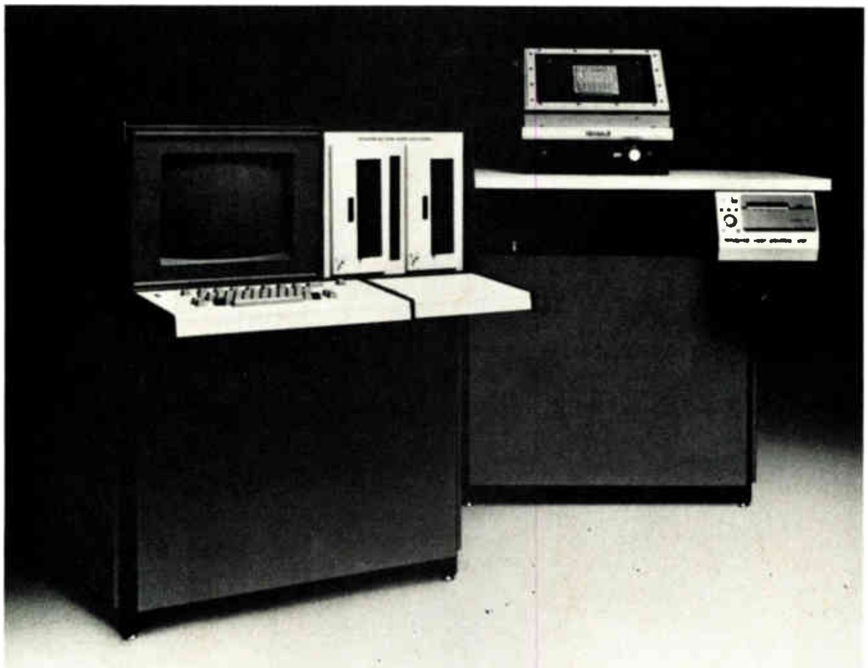
At the center of the system is the test-administration and system-control center, which contains an 8-bit microprocessor-based single-board computer with up to 192 kilobytes of random-access memory. Also incorporating a 15-in. cathode-ray-tube console and dual floppy-disk drives for storage of operating software and test plans, the center can handle eight test plans at a time and can supervise four test stations.

**Test site.** Test-station hardware includes Teradyne's H697 control unit, through which an operator can start and stop testing or read status indicators during automatic test sequences. A thermal printer is standard; up to five high-speed line printers—Centronics' 703S or Dataproducts' 2260S—may substitute where lengthy detailed printouts accompany testing.

Test and measurement electronics include fixture cards of 120 or 128 test points each. Maximum system capacity will reach 64,000 test points, well in excess of current pc-board requirements, which may top 40,000 points today, Saylor says.

Complementary-MOS switches handling 0- and 10-V signal levels, along with parallel addressing of test points and high-speed algorithms, speed continuity verification to better than 2,000 points per second. The system has a standard 5,000-ohm test threshold for opens and shorts; users can set their own threshold levels to test for leakage paths.

Operating software for the N221 presents users with menus containing the full range of choices available for creation of test plans, setting of measurement levels, and dictating of the contents of error messages for printout. Identifying test points for diagnostic descriptions can take place automatically in several variations of user selection.



**Variations.** In low-volume runs, the system itself will identify test points and provide a lookup table for interpreting error messages. By keying in directions, users can dictate specific names for each point; group points into appropriate pin, group, or family tables; or define X-Y coordinates and direct the system to name points within the grid.

The N221's software also has several ways of handling programming of correct test-plan interconnections. Once test points have been identified, the system can program itself using a board known to be good. Alternatively, an operator can program a list of interconnection points, or an optional RS-232-C communications port can bring in board layouts from a data base.

Other routines ease editing of existing test plans, queue test operations for multiple test stations, and perform self-monitoring and diagnostics. They also compile statistics on yield, error frequency, operator efficiency, and system utilization.

Each test station comes with a vacuum-fixture base or with a special fixture using point-to-point wiring or ribbon cable to interface with in-house or commercially available standard-grid pneumatic fixtures. The N221 system accommodates test heads containing bed-of-nails interfaces for boards as large as 20 by 24 in.

**Custom.** The company will also custom-build board heads for system users. The N221's standard head comes with a minimum of 1,920 points and can expand initially to a maximum of 4,020 points.

Teradyne will introduce the N221 at the PC/80 conference scheduled for Oct. 21–23 in Los Angeles. The firm will concentrate first on telecommunications-equipment and computer manufacturers.

The company expects to be in full production by the second quarter of

# Silent Partners.

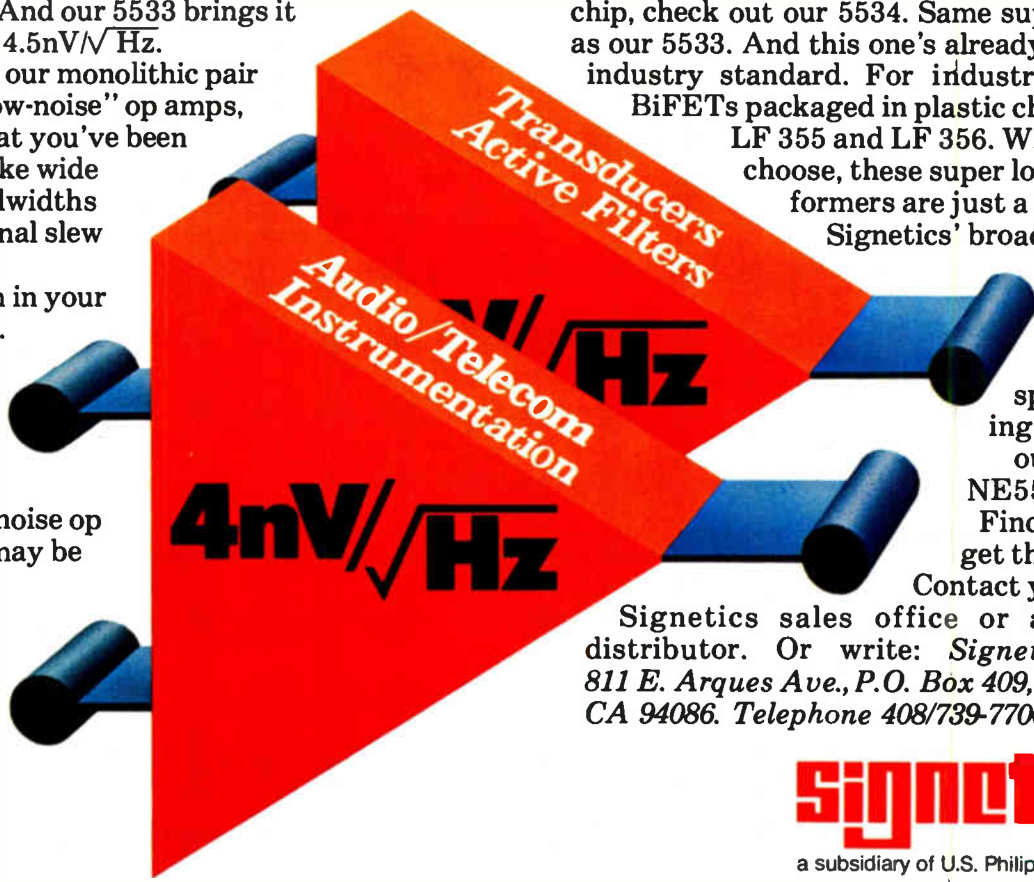
## Signetics' new dual op amps. Team them with your design for the industry's lowest noise.

Now the instrument OEM can specify op amps that deliver precision performance *and* low noise operation.

Our new duals combine the industry's lowest spectral voltage with a $600\Omega$ output drive capability. The Signetics 5532 really shines at $6nV/\sqrt{Hz}$. And our 5533 brings it all home at $4.5nV/\sqrt{Hz}$.

Compare our monolithic pair to other "low-noise" op amps, and see what you've been missing. Like wide power bandwidths at exceptional slew rates.

Use them in your new design. Or specify them as superior replacements for not-so-low-noise op amps you may be using now.




Both devices give you a small-signal bandwidth of 10MHz, and high output drive capability. *By "high," we mean 10V rms into* $600\Omega$ *at* $V_s = \pm 18V$. Great for active filters or low-signal transducers.

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| **Part Number** | **Key Specifications** |
| NE5532* | Low Noise: $6nV/\sqrt{Hz}$ (max.); internally compensated; 140kHz power BW @9V/μsec slew. |
| NE5533 (dual) | Low Noise: $4.5nV/\sqrt{Hz}$ (max.); 200kHz power BW @13V/μsec slew. |
| NE/SE5534* (single) | Low Noise: $4.5nV/\sqrt{Hz}$ (max.); 200kHz power BW @13V/μsec slew. |

*industry-standard pinouts, and available processed to MIL-STD 883B too!

To: Signetics Publication Services, 811 E. Arques Ave., MS 27, P. O. Box 409, Sunnyvale, CA 94086

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Company ______________ Division ______________

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E9/25

1981, according to Saylor. Though pricing is still tentative, he estimates an average turn-key system with a vacuum-fixture base and one test station will cost about $45,000.

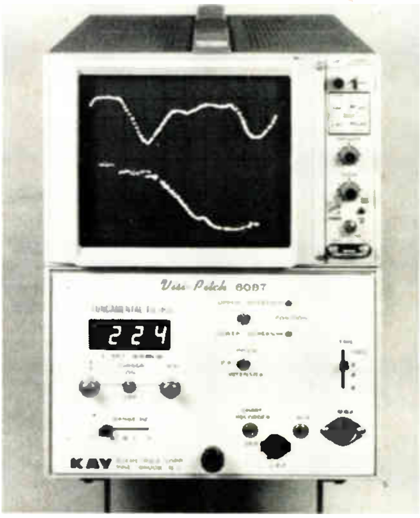
Additional test stations will be in the neighborhood of $5,000 each, and customized board heads will be priced on the basis of $1.75 to $2 per wired test point. Delivery time will range from 12 to 16 weeks.

Teradyne Inc., 183 Essex St., Boston, Mass. 02111. Telephone (617) 482-2777 [351]

## Instrument extracts frequency changes from cycle to cycle

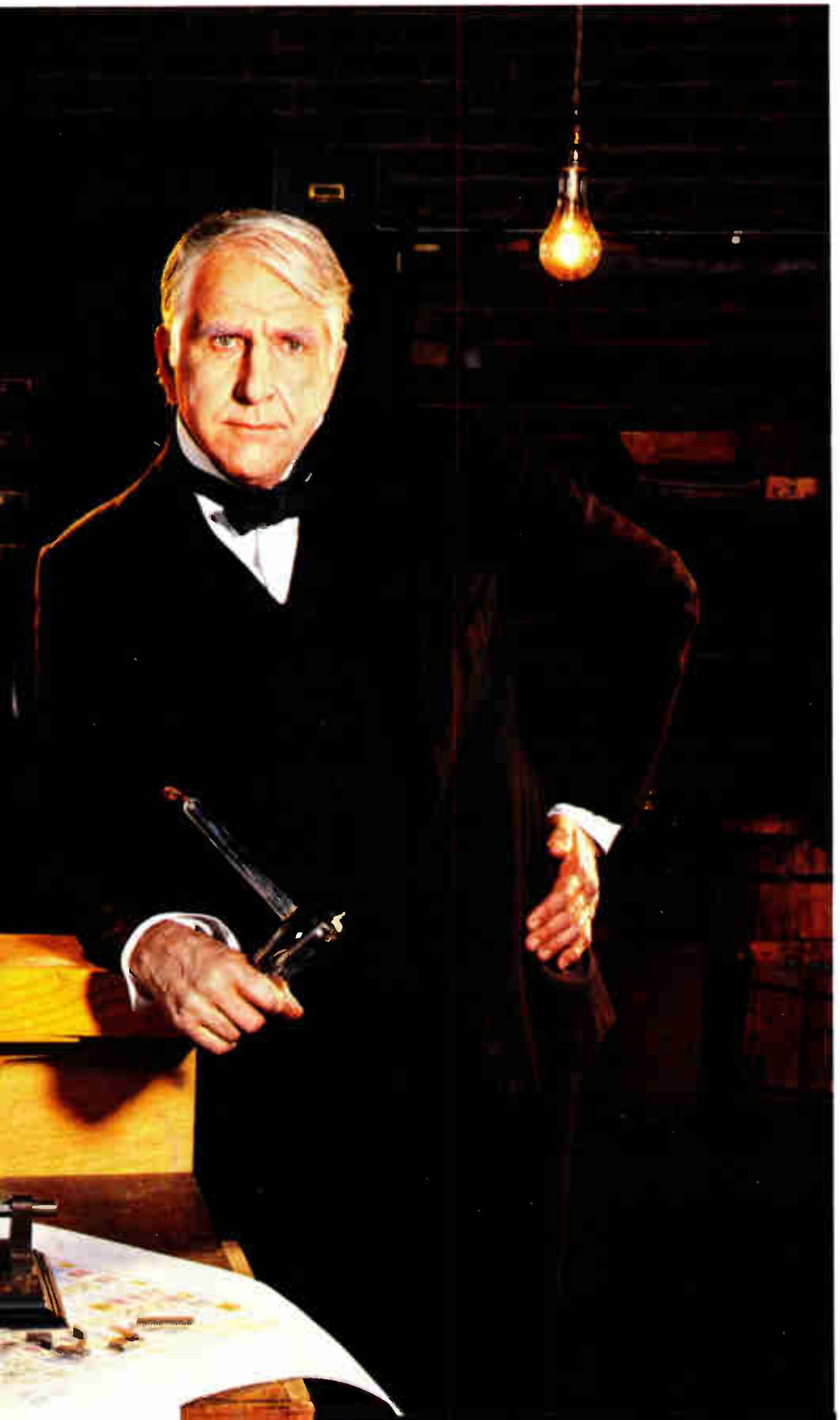
The Visi-Pitch is a portable instrument that extracts and measures fundamental frequencies in real time. It measures up to 1.6 kHz in four bands—50 to 300 Hz, 130 to 535 Hz, 200 to 800 Hz, and 400 to 1,600 Hz. The fundamental frequency can be displayed on a Tektronix 5000 series scope, which the Visi-Pitch plugs into (see photo). The pitch can also be displayed on a strip-chart recorder.

The manufacturer is uncertain of applications for the instrument, although the most obvious ones are in speech recognition and synthesis. The instrument displays a relative amplitude trace, either separately or simultaneously with pitch. An interfacing option allows transferral of frequency or period information



# *If Thomas Edison had used a Monochip,™ think how far he could have gone...*

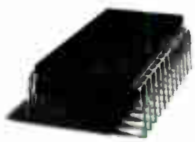


If Thomas Edison had used a Monochip,™ his electric pen might have been a color copy machine. His lightbulb might have been a laser. And his phonograph might have been a stereo system. Why? Because with Monochip, IC turnaround time could have kept pace with the speed of his imagination and the limitations of his budget.

Monochip is the semi-custom IC. That means its circuit components—the first five layers—are already in place when you start designing. All you do is tell us how to connect them to make the circuit your application requires. Working from your layout, we etch the sixth layer and deliver prototypes in only 6 to 8 weeks for $5,000 or less. Once you've approved them, we'll make production runs of 1,000 to 500,000 parts. It's that easy. Monochip Design Kits are only $25 to $59 each, and include everything needed to develop your own custom linear, CMOS, NMOS, CML or bipolar IC.

There's no telling what Edison might have designed if he could have used a Monochip. Now, just imagine how far *you* can go. Call or write for more information. Interdesign, 1255 Reamwood Avenue, Sunnyvale, CA 94086. (408) 734-8666.

**Interdesign**



Monochip:™ the semi-custom IC.

Interdesign is a Ferranti Company.

Circle 225 on reader service card

from the instrument to any 8-bit parallel-input computer or microprocessor. The plug-in instrument sells for $1,550 and can be obtained complete with scope for $2,195 more. Delivery takes from two to four weeks.

Kay Elemetrics Corp., 12 Maple Ave., Pine Brook, N. J. 07058. Phone (201) 227-2000 [353]

## 8-digit counter/timer measures 15-ns pulses

An 8-digit, 150-MHz multifunction counter/timer measures frequency, period, average period, and elapsed time and counts and totals events. In addition to measuring sine-wave frequency, the model 5845 also measures and resolves pulses occurring as close as 15 ns apart. The instrument has a sensitivity as low as 10 mV rms for sine waves, or 30 mV peak to peak for pulses. It will accept signals as large as 250 V. It features a switchable 100-kHz low-pass filter to maximize noise rejection when measuring low-frequency square-wave or pulse signals. The instrument's time base is a 10-MHz crystal oscillator with accuracy to within ±4 ppm per year.

The 5845 is priced at $325. A

field-installable input/output option that puts out full binary-coded decimal data and status and has provision for an external 10-MHz clock input sells for $125. Availability is from stock to 30 days.

Data Precision Corp., division of Analogic Corp., Electronics Avenue, Danvers, Mass. 01923. In Massachusetts phone (800) 892-0528; in other states call (800) 343-8150 [354]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Packaging & production

# Mercury lamps are toughened

## New design and materials produce a highly reliable ultraviolet source

If a mercury lamp that is the light source for a critical piece of integrated-circuit processing equipment—mask aligners in photolithography—goes out, wafer flow is slowed. In fact, if it blows out, the explosion also destroys the associated reflective optics. To cover such contingencies, Optical Associates is introducing a series of 200-, 350-, and 500-W lamps whose performance and reliability allow the company to offer an extended warranty on the lamps.

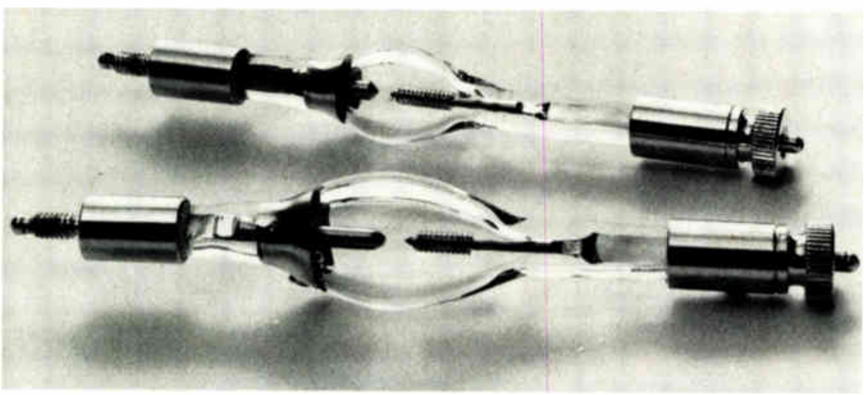
When used with any OAI lamp system (light source and power supply), the lamps are expected to last between 600 and 800 hours. "This, of course, depends on the operating conditions and controls provided by the original manufacturer of the aligners," says company president George A. Lee. If an OAI lamp used with a light source and power supply from OAI explodes, OAI will provide the end user with a significant discount (20% to 40% off) on replacement optics and lamp. This, again, depends on the length of time the lamp has been in use, and other ambient conditions.

A major objective is to "open the door for us to negotiate what could be an industry-standard contract," explains Lee. He adds that manufacturers of lamps for photolithography lack industry-wide standards for price, specifications, and warranty. "Different OEMs are willing to trade off certain specifications for the sake of others, and the lamp makers often end up making practically custom lamps."

Short arc lamps, the type OAI is introducing, approach an ideal point source, employing an arc discharge to provide high radiant intensity and luminance. Such intense conditions have sometimes resulted in explosions of ordinary lamps. The OAI lamps' ellipsoid envelope is manufactured from a very high-grade, optically clear (water-free) fused quartz. The envelope's thick walls survive the internal operating pressure, approximately 40 atmospheres, making the lamps virtually immune to catastrophic failure, says the firm. Short radii have also been eliminated from the quartz envelope to reduce stress concentrations.

The lamp's electrodes are formed from specially treated tungsten. The anode serves as a large thermal sink, enhancing heat dissipation, and contributing to long life. After assembly, each envelope is filled with triple-distilled mercury.

The lamps employ gold-plated anode and cathode bases to ensure reliable contact interfaces. Due to the corrosion resistance of gold, the electrical connections to the lamp bases are virtually immune to contact degradation—a common problem when lamp sources lack a noble-metal base contact.



Every lamp is pretested for ease of starting, electrical specifications, and output intensity. A single lamp lists for $50 and up, but since they sell in larger quantities and vary in configuration, final pricing depends on individual contract arrangements. The lamp series is available now from distributors' stock in the United States, Europe, and Japan.

Optical Associates Inc., 3300 Edward Ave., Santa Clara, Calif. 95050. Phone (408) 988-6900 [391]

## Module equips Wafertrac to develop positive resists

Users of the Wafertrac wafer-processing system now can develop positive resists using a new spin-processor module. The model 9110 was developed to meet the need of users of projection aligners and GCA's DSW Wafer Stepper system. The module is capable of clearing 2.5 μm lines and spaces with a uniformity of ±0.05 to 0.1 μm on 100-mm wafers. The unit's dispenser head and wafer chamber were designed to avoid water-vapor and salt buildup. A special nozzle and liquid-feed system provide accurate low-pressure control, says the company; they also eliminate condensation drip.

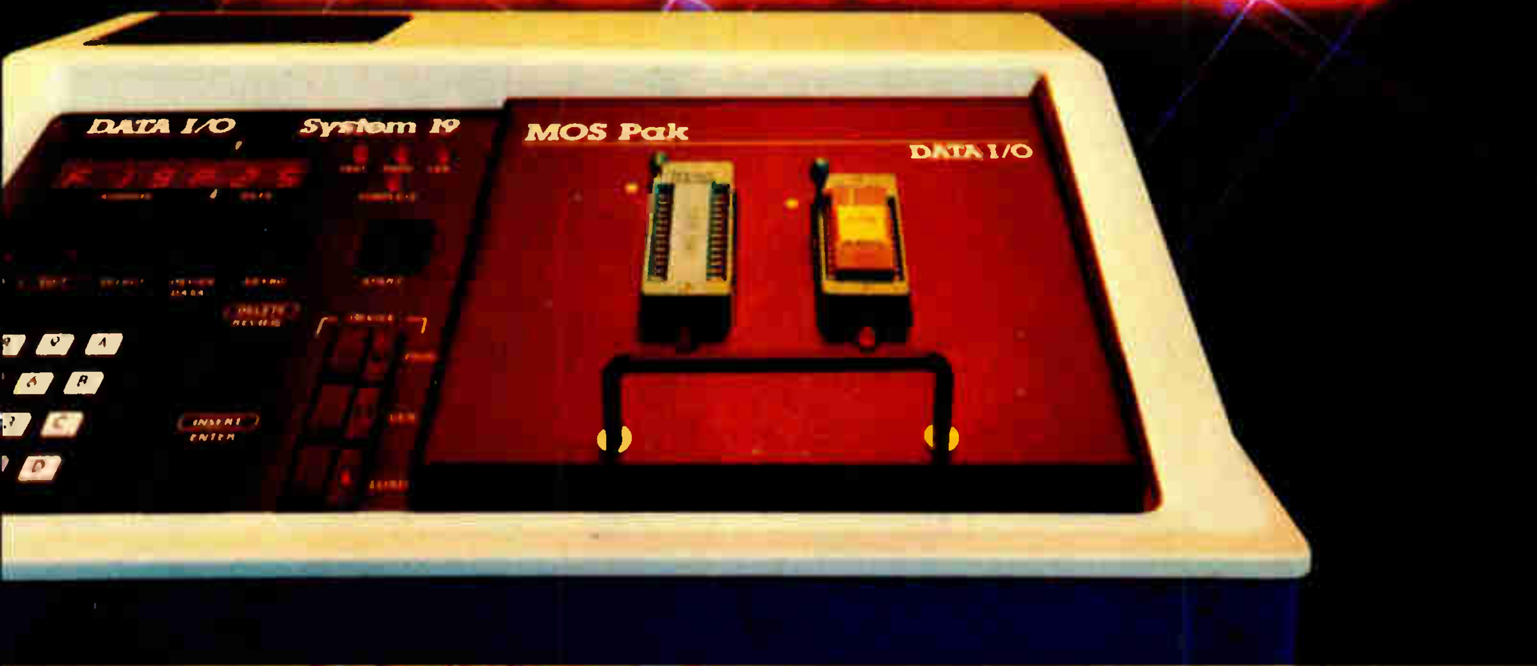
The module is built on a 9-by-36-in. side-rail frame that can be incorporated into a new Wafertrac system for a total system price starting at $35,000. It can also be retrofitted to systems already in use for $9,000. The Wafertrac systems have a backlog of 12 months, but retrofitting in the field can be done in only three to four months.

GCA Corp., California Operations, 214 Humboldt Ct., Sunnyvale, Calif. 94086 [393]

## Insulated shorting jacks have 0.030-to-0.032-in. diameters

Insulated shorting jacks measuring 0.030, 0.031, and 0.032 in. in diameter can be used for switching or shorting on any printed-circuit board that uses the same-diameter pins

# DATA I/O INTRODUCES A UNIVERSAL MOS EPROM PROGRAMMER FOR PEOPLE WHO THINK AHEAD.





**System 19/MOS Pak programs all of today's EPROMs and offers plenty of room for future growth.** MOS Pak lets you program all currently available EPROMs including the 2704, 2708, 2758, 2508, 2516, 2716, 2532, 2732, 2732A, 2564, 2764, 68764, and the new Hitachi 48016 EEPROM.

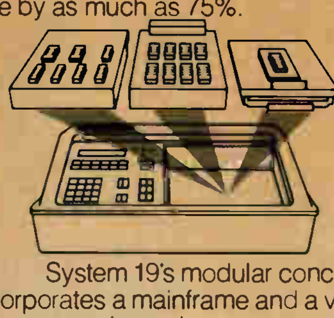
And what about the future? Simple software changes to the MOS Pak will enable you to program new devices as they're developed—even if you decide to design a 128K EPROM into your product.

**Semiconductor manufacturers' approval provides user security.** System 19/MOS Pak is the first "MOS only" programmer to meet the high programming standards set by the semiconductor industry. Programming algorithms and waveforms have received written approval from all of the manufacturers.


Approval plus Data I/O's unique built-in calibration system assure you of high reliability and device yield.

**System 19/MOS Pak is self-contained and easy to use.** System 19/MOS Pak goes where you need it: engineering lab, service department or in the field. It requires only ten seconds to set up and begin programming. Simply key in a four digit code for the particular type of EPROM you want to program. A lighted LED on the MOS Pak will tell you which socket to use.

And the MOS Pak's new programming algorithm for 64K devices can shorten programming time by as much as 75%.



System 19's modular concept incorporates a mainframe and a variety of programming paks.

**With the System 19/MOS Pak, Data I/O now offers three great ways to program MOS EPROMs.**

*For EPROMs*

- –MOS Pak programs single MOS devices
- –Gang Module programs eight EPROMs at once
- –Unipak programs more than 200 MOS and bipolar PROMs

*For individual PROM and logic families*

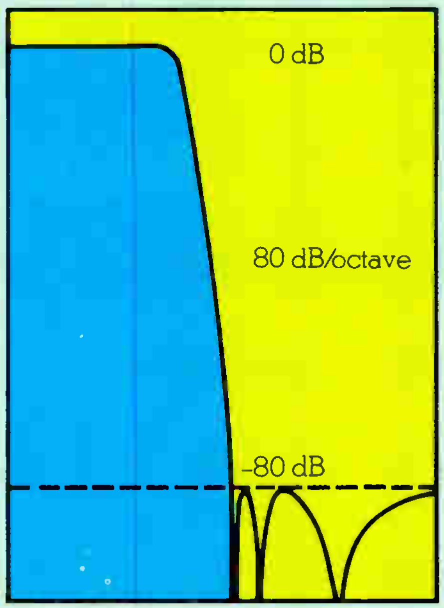
- –More than 40 approved programming paks

**Let us show you the future.** The Data I/O MOS Pak is available now. To make arrangements for a demonstration or to get your free copy of our MOS programming brochure, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. Phone 206/455-3990 or Toll Free 800/426-9016.

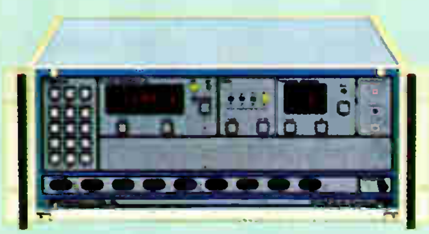

**DATA I/O**

Circle 231 on reader service card

# BEGONE CURSED ALIAS




**Precision 616**
124 programmable cut-off frequencies.



**Precision 636**
Two models: 4092 or 6141 cut-off frequencies.

**Precision 416**
Combined filter and amplifier. 62 cut-off frequencies.

You want analog data to come clean for digital conversion.

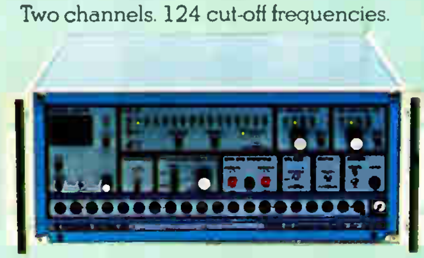
We keep extending the Precision ways to do it with signal conditioners, amplifiers and filters.

All Precision anti-alias filters have elliptics with 80 dB/octave attenuation. All come with time delay filters superior to Bessel. All have typical phase match of ½°.

All Precision instruments are programmable. All interface with mini, micro or GPIB. All have 16 channels, except the 602.

**Call Don Chandler,**
607-277-3550, for detailed specifications.

**Precision 602**
Two channels. 124 cut-off frequencies.



**Precision 216**
16 channel automatic/programmable gain amplifier. 300kHz bandwidth.

**Precision 316**
Calibration and conditioning for charge, voltage and strain inputs.

## PRECISION FILTERS, INC.
303 W. Lincoln, Ithaca, N.Y. 14850

Circle 232 on reader service card

mounted on 0.100-in. centers. The jacks mate with the 0.032-in.-diameter (±0.001 in.) pins used in Cambion's 470-2101/2102 switching blocks. The 0.120-in.-diameter hole in the body of the jack's insulated portion permits the use of a hooklike tool to help extract the jack when space is limited.

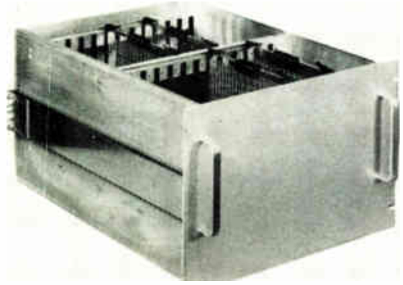
The jacks come in black, red, and blue, and the insulating material is polypropylene. They are priced at 28¢ each in 100-piece quantities and at 25¢ each in 1,000-piece lots. All are available for delivery from stock.

Cambion, 445 Concord Ave., Cambridge, Mass. 02238. Phone (617) 491-5400 [394]

## Drawer for 19-in. cabinet has connector backplane, slides

A fully assembled drawer comes complete with connector backplanes, slides, and handles. The backplanes are slotted between each connector to allow air movement. The slides allow the drawer to pull out of a 19-in. cabinet and pivot up and down for easy access to the backplanes or panels. The drawer packages up to 26 of Mupac's 324-class wire-wrappable panels and printed-circuit boards that are designed around the company's 108-pin connector. The card guides supplied with the drawer are on 1.200-in. spacing. The blank, 0.125-in.-thick aluminum front and back panels allow the mounting of hardware such as input/output connectors, switches, and light-emitting diodes. The overall drawer size is 23.82 by 19 by 12.220 in. The price for one to nine units is $1,408.56. Delivery takes four weeks.

Mupac Corp., 646 Summer St., Brockton, Mass. 02402. Phone (617) 588-6110 [395]



## Dual-channel cable replaces two single-channel assemblies

A fiber-optic dual-channel cable and connector assembly, the HFBR-3100 duplex cable consists of two single-fiber cables extruded together and surrounded by a common black polyurethane jacket, forming what the maker calls an "easy-slit zip cord." Where two-channel transmission is required, the dual-channel cable can be used in place of two HFBR-3000 single-channel assemblies. It weighs 17 g/m and measures 6.35 by 3 mm. Connectors are factory-installed and -tested for mechanical strength and optical quality. Temperature performance is characterized to −40°C, and the cable is flame-retardant.

Cable lengths up to 5 km are $4.50 per meter in the U.S., plus $45 per termination for up to 19 connectors. Delivery is from stock.

Hewlett-Packard Co., Inquiries Manager, 1507 Page Mill Rd., Palo Alto, Calif. 94304 [397]

## Programmable burn-in board loader inserts 3,000 DIPs/h

A programmable burn-in board loader has insertion rates of 3,000 dual in-line packages per hour. The CS-301 automatic DIP inserter has 15-by-18-in. travel and positions at a speed of 900 in./min. The insertion head, which accepts virtually all packages, combs bent leads. The unit also recognizes defective sockets that have been painted and automatically skips over them.

Instead of a conventional on-line sequencer, the CS-301 uses a single-tube input. It also uses a paper-tape reader to enter programs into memory. The programs consist of simple descriptions of the board geometry indicating DIP row and column spacing. The loader's microcomputer generates coordinates on the fly. The complete unit is $19,000.

Contact Systems Inc., Miry Brook Road, Danbury, Conn. 06810 [398]

# There's no body like our new ZOOM BODY

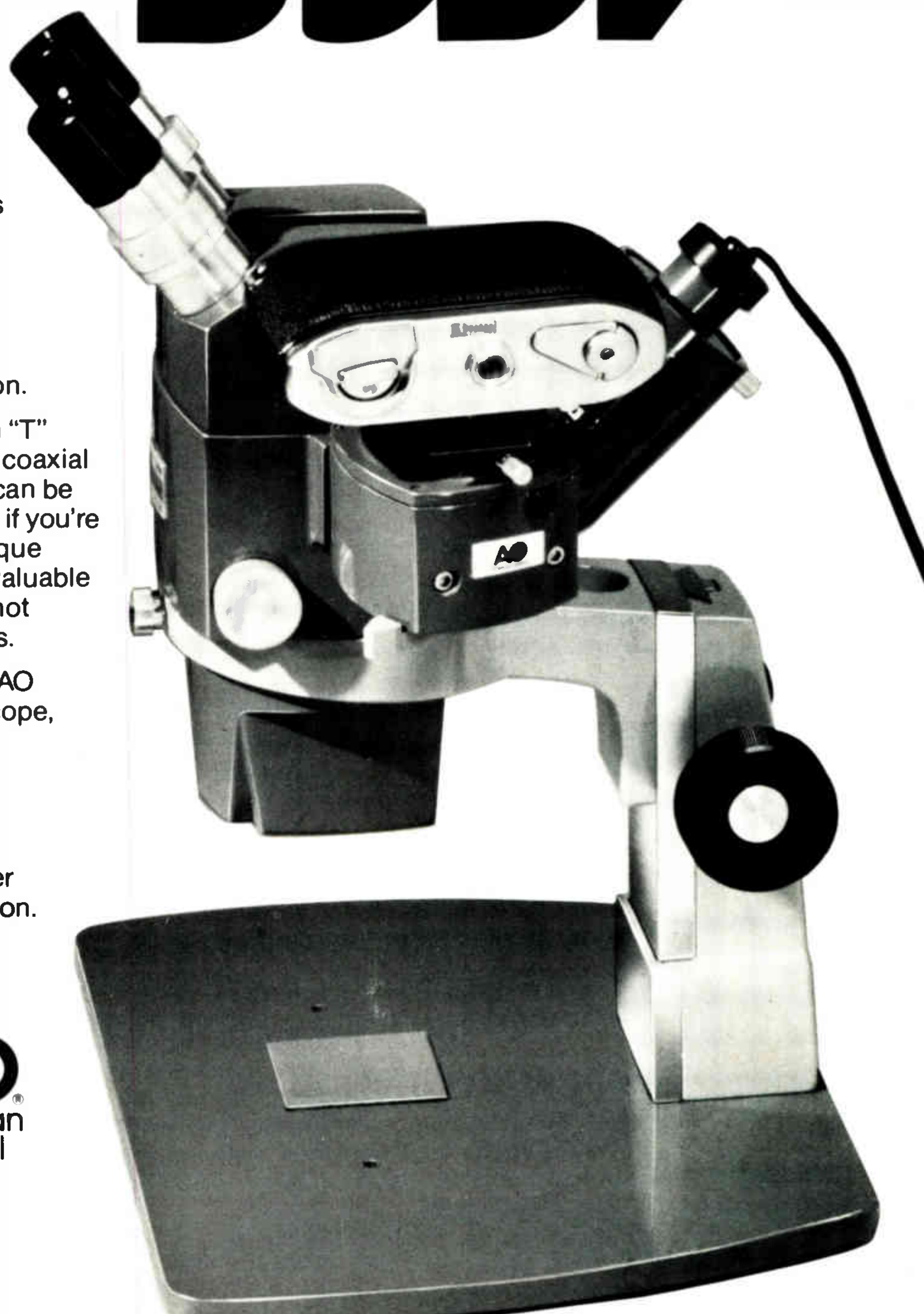
The new AO STEREOSTAR® Zoom "T" microscope features the "T" zoom body with coaxial illumination and photo capabilities. It may be just what you need to boost output in your production, assembly or inspection department.

The Zoom "T" gives you a constant 4" of working room. It has a 1x - 6x magnification range, and with auxiliary lenses and eyepieces it offers a total range of 5x - 300x. Magnification can be conveniently changed with controls on both sides of the body. No matter what magnification you're working with, you get crisp, sharp image definition.

Modular in construction, the Zoom "T" can be ordered with or without the coaxial illuminator. In fact, any accessory can be simply added at any time. However, if you're working with highly reflective opaque surfaces, coaxial illumination is invaluable because it gives contrast without hot spots, glare, reflections or shadows.

We invite you to compare the new AO STEREOSTAR Zoom "T" microscope, feature by feature, with any other competitive microscope.

We're confident you'll immediately see that it offers the outstanding value in its field. See your AO dealer or representative for a demonstration. Or write for a detailed brochure American Optical, Scientific Instrument Division, Box 123, Buffalo, NY 14240.




AO® American Optical

# TWO NEW FOILS FROM GOULD WILL HELP YOU DESIGN MORE RELIABLE PRINTED CIRCUIT BOARDS.

**TCS™ foil.** The growing use of multilayer laminates has placed a premium on the reliability of the printed circuit board.

Thermal z-axis expansion of multilayer laminates during the solder operation can induce strains in the copper foil near the edge of plated thru holes. Gould TCS foil has been developed to help withstand this thermally induced strain. That means added reliability in the circuit board.

**Double treated copper foil.** TC/TC™ double treated copper foil is used in the manufacturing of the copper clad inner layers of high density multilayer printed circuit boards. TC/TC double treated foil eliminates the need for the oxide treatments currently in use. The foil is uniformly treated on both drum and matte sides with a TC treatment to enhance the bonding strength.

Add an extra dimension of reliability to the circuit boards you design. Specify TCS foil and double treated copper foil from Gould.

For more information, write Mr. Frank Zust, U. S. Marketing Manager, Gould Inc., Foil Division, 17000 St. Clair Ave., Cleveland, Ohio 44110.

**GOULD**

*An Electrical/Electronics Company*

# Products Newsletter

**$10,900 OCR system aims to enter word-processing market**

The model 1205 optical character-recognition system from Burroughs OCR Systems, Burlington, Mass., could be the wedge that OCR has needed to penetrate the word-processing market. At $10,900 and with **a throughput of up to 300 pages per hour,** the 1205 is expected to challenge low-priced, manual-entry word-processing stations, which rarely exceed 10 pages/h. The 1205's specified error rate is less than 1 in $10^5$. It includes a 100-sheet automatic paper feed and is programmable. It also offers editing and formatting capabilities.

**National Semiconductor quadruples memory of 8048 microcomputer**

National Semiconductor Corp., Santa Clara, Calif., has started offering samples of an expanded version of the industry-standard 8048 single-chip 8-bit microcomputer. The INS8050 n-MOS chip **has 4-K bytes of masked read-only memory and 256 bytes of random-access memory** on board. That's four times the program and data memory on Intel's 8048 and twice as much RAM as its addition to the MCS-48 family, the 8051, which, unlike the National chip is neither pin– nor operation-code–compatible with the 8048. Volume production of the 8050 is slated for early in the fourth quarter of the year.

**MMI's PAL gets mask-programmed**

Monolithic Memories Inc., the Sunnyvale, Calif., firm that developed the programmable array logic (PAL), has come up with **a mask-programmed version, termed a HAL, for hard array logic.** A HAL's relationship to a PAL is similar to that of a mask-programmed read-only memory to a programmable ROM. The first standard HAL products are not expected to surface until next year.

**Sample-and-hold network acquires data in 1 μs**

The 4857 hybrid sample-and-hold network from Teledyne Philbrick combines a 1-μs acquisition time with **a 0.1-μV/s droop rate.** An internal comparator maintains performance despite fluctuations in digital ground from 1.5 to 7 V, and an uncommitted buffer amplifier offers either inverting or noninverting gain. The 4857 costs $98 in lots of 100. Delivery by the Dedham, Mass., firm takes 12 to 16 weeks.

**Digital bridge betters performance at minimal cost**

At $4,950, the 1687B 1-MHz Digibridge from Genrad Inc. costs only $565 more than its predecessor, the 1687A, but offers a new 10-mV-rms probe for semiconductor tests and can make **twice the number of measurements with twice the accuracy.** Users of the Concord, Mass., firm's new digital bridge can break down complex impedances in passive and active component systems, reading each vector's value on twin alphanumeric displays. The 1687B makes three to seven measurements per second and includes automatic self-testing, diagnostics, and battery backup. Genrad claims that similar systems cost about $6,000.

**P-channel devices added to Hexfet power MOS FET line**

International Rectifier Corp.'s latest p-MOS power field-effect transistors are especially suited for reverse-polarity applications. In addition, the new MOS FETs have the **voltage control, high gain, fast response,** and other standard features of the El Segundo, Calif., company's existing n-channel Hexfets. For 100-unit lots, prices range from $6 each for the IRF9523 60-V devices to $14 each for the IRG9130 series of 100-V devices.


I SPEAK FOR GERMANIUM!
"FRIENDS, ENGINEERS AND BUYERS! I come to praise Germanium, not to bury it: there's too much life in the old technology yet,"
says Oliver O Ward, President, Germanium Power Devices Corp.
"For high power devices, you can't beat Germanium.
For example, GPD makes the only single-chip 100A transistor on the market.
"For battery-operated instruments, Germanium is still the best, with its excellent VSAT characteristics and low current drain.
"And even where there are alternatives, it is not worth the time and expense of redesign, as long as you are sure of your source.
We at, GPD, will be making Germanium devices from 150mW to 100A, as long as you the customer need them.
"Long live Germanium!"
"Germanium Power for the future!"
"I promise never to forget the small-signal Germanium user!"
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## Career outlook

### Group seeks software ideas

■ Formed to look into software-related controversies, the Commission of Software Issues in the '80s is now grappling with problems that may well be of interest to the electrical engineering community at large. Late last month the commission—which was started in April and now comprises some 17 member associations—set up four task forces to investigate software taxation, the education and training of computer professionals, software standards, and software protection.

"We're trying to recruit recognized experts and people who may have worked in one or more of these areas," notes Steven J. Jost, secretary for the commission. "We'll be soliciting papers, and ultimately we'll prepare a draft paper from each task force. The commission will take those draft papers and issue white papers eventually."

In the software taxation area, the task force will be looking at, among other issues, whether software is a tangible or intangible item. If tangible, it is subject to a sales tax at the state level; if intangible it might qualify for Federal investment tax credits. In establishing software standards, the commission hopes to determine prerequisites for machine compatibility and product integrity. "We want to set down guidelines for determining if a software product really is what the supplier says it is," says Jost. The software-protection task force will be researching copyright and patent issues as the first order of business.

Other areas that the individual task forces will be investigating include software crime and the economics of software, although these areas may acquire their own task forces at a later date.

Included in the list of member associations to date are the Computer Law Association, DPMA, Adapso, the computer society of the Institute of Electrical and Electronics Engineers, and the American Electronics Association. Although individuals may not join the commission as members, Jost emphasizes that anyone with something to contribute may participate at the task-force level. "We're going to be making some pretty complex and far-reaching decisions and we want all the input we can possibly get," he observes. "Some choices are going to have to be made fairly soon, or government will be in charge of all the regulation. And I don't think anyone wants 51 different policies at the state and Federal level."

For more information, Steve Jost can be reached at 1301 20th St., N. W., Suite 116, Washington, D. C.; (202) 887-0337.

**Laser short courses.** The Laser Institute of America is offering a series of five-day courses in the areas of optical-fiber communications, laser fundamentals and systems, laser applications in materials processing, and laser safety. The first course on communications starts Oct. 6 in Santa Fe, N. M., and will cover the areas of design fabrication, test and applications of information-transmission systems using optical fibers. The second, to be held Oct. 20–24 in Washington, D. C., will look at the principles and techniques of laser operation, pulse generation, output characteristics and measurements, classes of lasers, and applications in materials processing, communications, medicine, holography, and data processing.

The third will further explore applications in materials processing for manufacturing engineers in Boston starting Oct. 27. The last course—to begin Nov. 3 in Anaheim—will evaluate hazards as well as standards, control measures, and laser safety program management. The cost for each course is $600. For more information, write to the Laser Institute of America, Short Course Director, P. O. Box 9000, Waco, Texas 76710.

**Futuristic technology.** A one-day seminar will be held Sept. 30 by Arthur D. Little Inc. on current and future developments in high technology and communications. "Status Report: Ten Hot Topics in Information Technology" will highlight evo-

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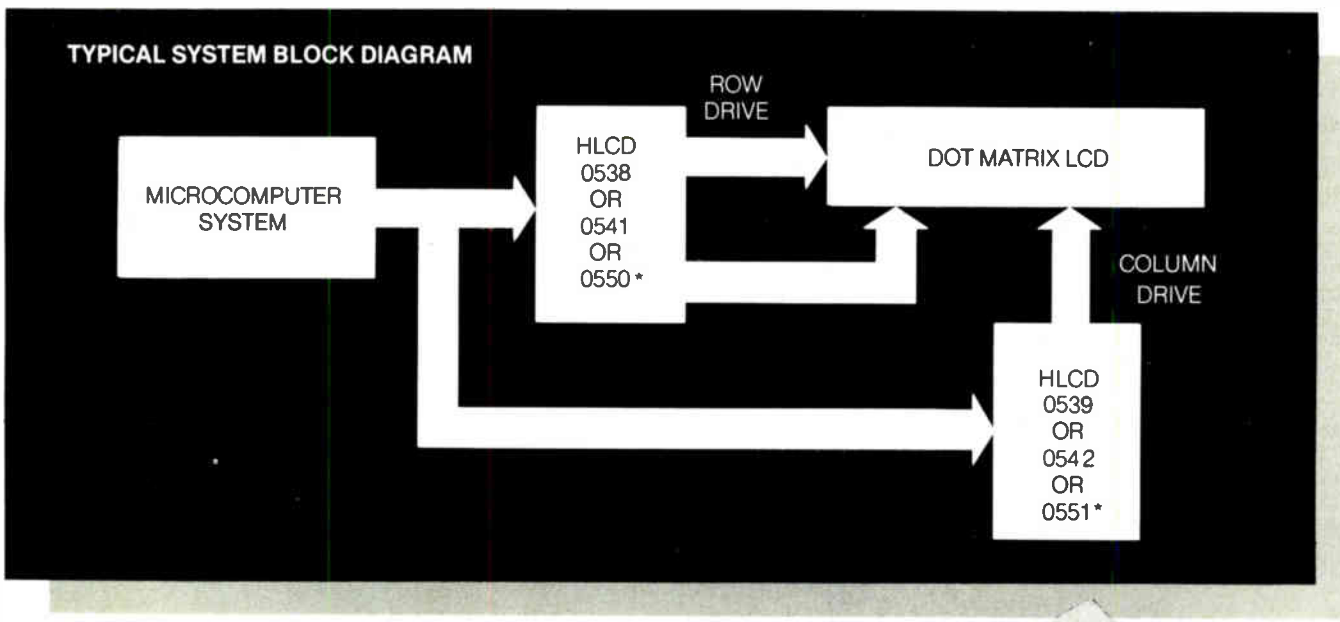


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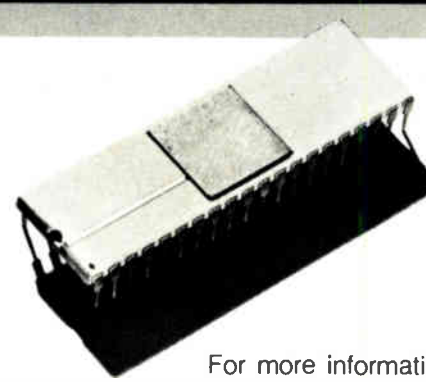

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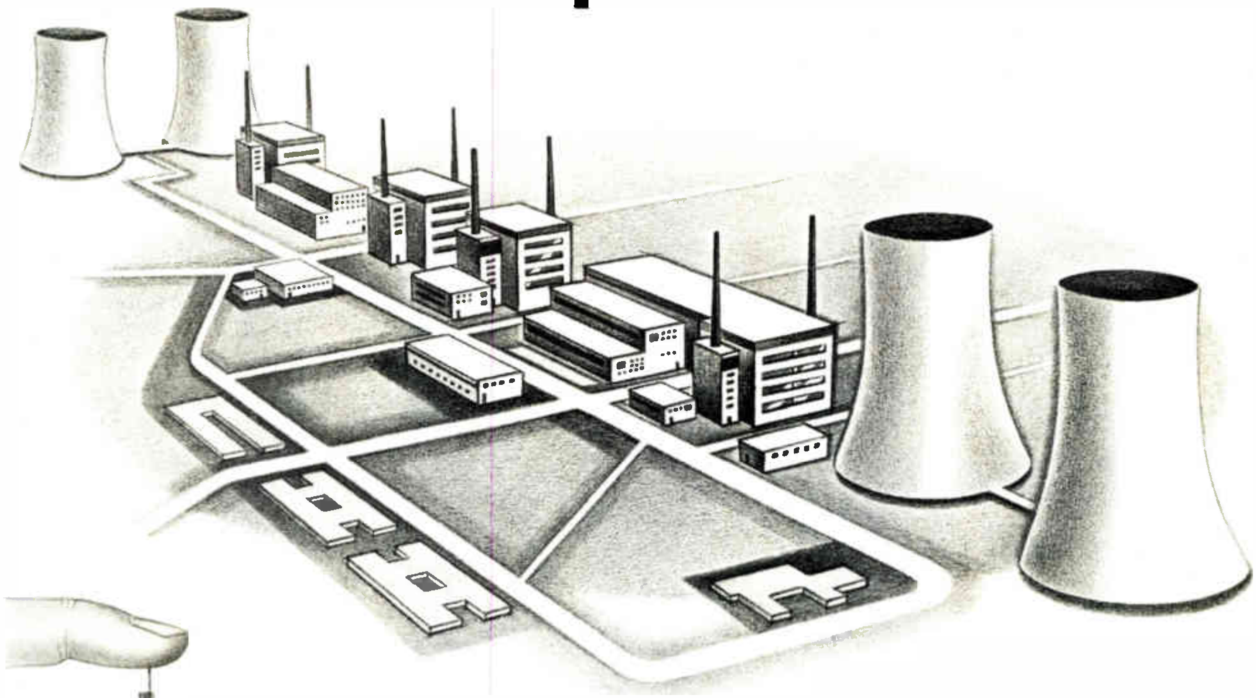
## Career outlook

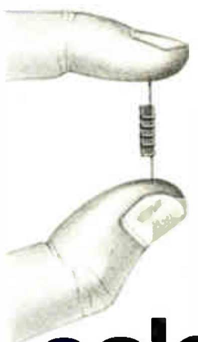
lutionary developments in semiconductors, personal computers, home terminals, office automation, intelligent copiers and robotics. Frederic D. Withington, an ADL vice president, will be heading up the presentation, which will also examine areas of voice recognition, video disks, novel computers, and artificial intelligence. The attendance at the seminar will be limited, and the fee is $500. For more information or to make reservations, please write to Dusty Rhodes, Arthur D. Little Decision Resources, Acorn Park, Cambridge, Mass. 02140, or call her at (617) 267-3456.

**Digital video.** The Society of Motion Picture and Television Engineers (SMPTE) has just published its third volume on digital video. The book is entitled "Digital Video" and contains 24 papers that were presented at the SMPTE Television conference held in Toronto this past February. Such papers as "Integrated Circuits for TV in the Digital Decade," "Digital Video Processing—1980," "Architecture of the French LSI Set for Antiope Teletext Decoders," and "Video Recording in the 625-line System" are included in the book. Edited by Richard Marcus, Rombex Productions Inc., the volume is priced at $20. It may be obtained from SMPTE Books, 862 Scarsdale Ave., Scarsdale, N. Y. 10583, or call (914) 472-6606.

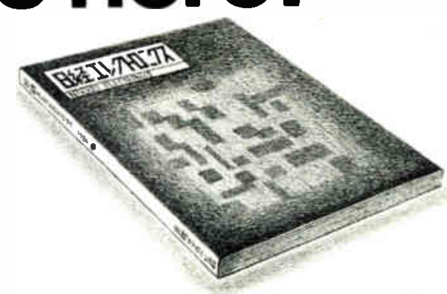
**Personnel changes.** A new chairman of the electrical engineering department has been named at Lehigh University. Donald M. Bolle joins the Bethlehem, Pa., faculty from Brown University. He has a BSEE degree from Kings College, Durham University, in England and a Ph.D. in electrical engineering from Purdue University.

Also at Lehigh, Richard B. Streeter has been named the director of the office of research to encourage awareness of potential sponsors of research. Streeter joins Lehigh from Portland State University, where he was director of sponsored research activities, as well as an assistant dean. **-Pamela Hamilton**









# Massachusetts

## The state of technology for engineers



Massachusetts is the state of technology and a land of opportunity for engineers. The beautiful and historic Bay State has a dire need for engineers to fill positions in high technology companies that specialize in avionics, computer science, electric/electronics, and data processing.

The demand is so great that the Massachusetts High Technology Council, a business organization that represents 89 companies in the high technology field, says the state will have to find 3,500 new engineers every year for the next three years. When you consider that Massachusetts colleges graduate approximately 850 EE and computer science specialists each year, the grave shortage of engineers in the state is obvious. The need includes both entry-level and experienced engineers. If you are a qualified engineer in the disciplines mentioned, your talents are wanted and welcome in Massachusetts.

The dominant influence in the Massachusetts employment picture is high technology and the companies that serve it. Not only are these companies among the nation's fastest growing, with annual growth rates of 15% to 40% a year, they are among the few companies in the nation that are bucking the inflation spiral. These companies comprise nearly 40% of all manufacturing in Massachusetts and account for almost 30% of total state employment.

The main indicator of future growth in employment is the birth of new high technology firms. Massachusetts and California are the two strongest states in this category. The proportion of companies that were founded in this field after 1970 is 57% for California and 93% for Massachusetts. It is important to note that states that do not generate new companies or new branches have a limited growth potential.

Massachusetts is making it happen with incentives to encourage engineers to live and work in the state.

For example, in February 1979 in what is called a social contract Massachusetts Governor Edward J. King and the High Technology Council, which represents more than 100 chief executives of high technology companies, agreed to work together to create 60,000 new high technology jobs plus 90,000 new jobs in manufacturing and support services by 1983.

In addition, a new 4% tax cap (ceiling)

and subsequent reduction of property taxes was imposed in 1979. In the first year of the tax cap, 60% of the state's cities and towns reduced their property tax rates and another 10% remained stable.

Personal income taxes were reduced by increased exemptions.

The capital gains tax is being reduced 60% over a three-year period.

These are noteworthy achievements in a state noted for high taxes. Massachusetts is continuing its efforts to reduce taxes paid by individuals as well as taxes in such areas as real estate, capital gains, auto excise, and inheritance.

The tax benefits to be derived from the new jobs created under the social contract are a $2 billion annual increase in personal income by 1983 and $300 million annual increase in state and local tax revenues to fund state and local tax rate reductions and to support worthy social goals.

It must also be pointed out that the long-term economic indicators for Massachusetts are optimistic. For example, the latest list of Fortune 1000 companies shows that of the newcomers to the list, 21.7% came from Massachusetts, more than any other state. The newcomer list represents growing, up-and-coming companies. California had 16.6% and New York 11.9%.

Another plus for Massachusetts is that it has the lowest unemployment rate among the ten largest states. In March of this year, for example, the seasonally adjusted employment rate for the state was 4.9%.

The real estate picture in Massachusetts is another bright spot and many incoming engineers have a pleasant surprise in store. Housing is available and prices are lower than in most of the concentrated electronic areas in other states.

Massachusetts also had the largest increase in per capita income of the six New England states from January of 1979 to January of 1980. Personal income in the state increased 33% more than the national increase, and was 16.4% above the average for New England States.

Inflation in Boston in 1979 was lower than any city except Chicago and Saint Louis. Inflation rates in major cities in the South and Southwest ran well ahead of their northern counterparts.

In addition to its growing economic strength and job opportunities, Massachusetts offers engineers an above average lifestyle. The state's educational, cultural, historic, and recreational facilities are second to none.

Photos courtesy of Massachusetts

Saling off Cape Cod, part of Massachusetts' 2,000 miles of shoreline, is a popular sport. The Bay State also has 36 ski areas, 143,000 acres of state forest, and 100 state parks.

Massachusetts Governor Edward J. King encourages business in his state and is working to create more jobs.

Recently James F. Carlin, Commissioner of the Massachusetts Department of Commerce, summarized some of the advantages its residents enjoy. For example:

Massachusetts is unequaled for engineers who want to continue their education. The state boasts 123 public and private colleges and universities, with the highest concentration of higher learning institutions in the country. Massachusetts has more than 100 private and secondary schools—almost 25% of all such schools in the United States.

Cultural activities in this lovely centerpiece state of New England include 23 orchestras and 175 museums—more per capita than any other state. There is also opera and ballet, the Boston Symphony, and the Pops, made famous by the late Arthur Fiedler.

Massachusetts also has more historic sites listed in the National Historic Register than any other state.

When it comes to recreation Massachusetts has it all. The state has 2,000 miles of magnificent shoreline, 36 ski areas, and close to 300 golf courses. More than 70% of the state is forestland, with 143,000 acres of state forest and 100 parks.

Sports-minded engineers have four professional teams to root for—the Boston Bruins, the Boston Celtics, the Boston Red Sox, and the New England Patriots, plus the famous Boston Marathon that draws 5,000 runners every year from all over the world and more than a million spectators.

It is also interesting to note that Massachusetts has the largest concentration of scientists in the United States. There are more than 1,000 industrial research laboratories and more than 35,000 scientists who live in the Bay State.

To sum up, Massachusetts offers engineers well paying jobs, a growing economic climate, and an envious lifestyle. Says George S. Kariotis, Secretary of the Executive Office of Economic Affairs, "Our growth industries, particularly the high technology sector, are keeping us afloat in this recession. That and the improved business climate give us real hope for a continued sound and growing economy."

If you are an engineer looking for a job that offers the opportunity to advance, and a virtually guaranteed future, don't miss the following Career Opportunities section featuring topnotch companies that want and need engineers with your specific talents. —John Brand.

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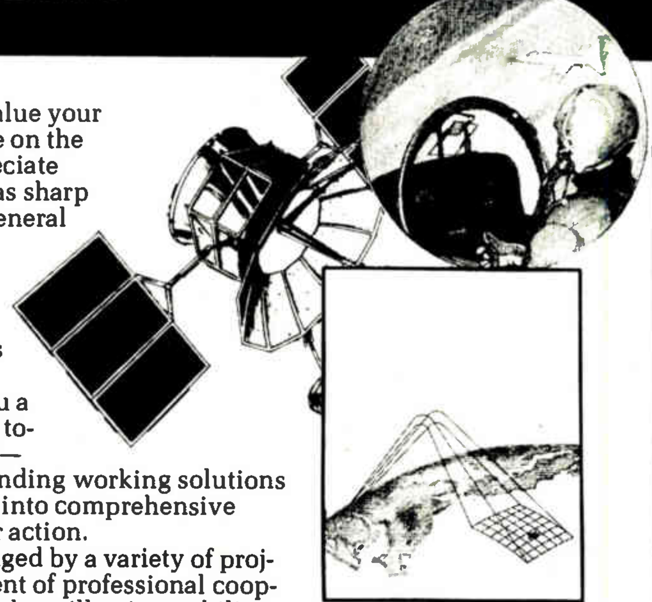

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- Analog Design
- Frequency Synthesizers
- Digital Radio
- Digital Signal Processing
- Fiber Optics Interfaces
- Electronic Surge Arrestors
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- I/O Controller Design
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## Software Engineering

You will have your choice of working in one, some, or all of the following areas:

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- Real-Time Simulation
- Diagnostics/ATE
- Operating Systems and Compilers
- Microprocessor Development

Your involvement will be in all phases of state-of-the-art development:

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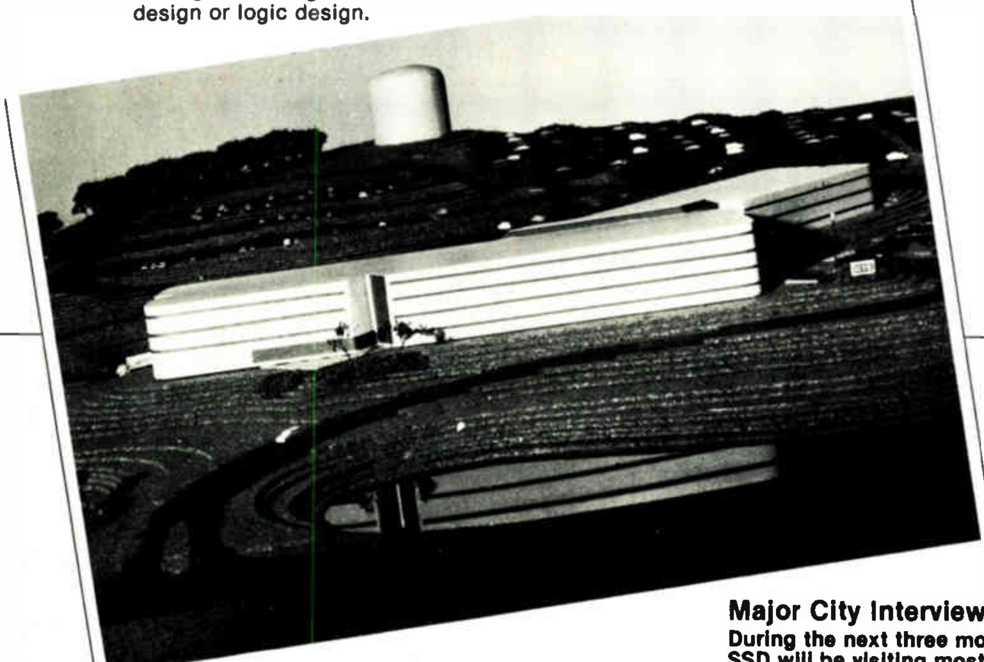
- Specifications
- Design
- Implementation

You should have anywhere from 2 to 10 years experience, be a self-starter, with the relaxed attitude and sense of humor that works well with others, under pressure. Your background should include real-time software engineering, preferably with minis and micros.



### Major City Interviews

**During the next three months, representatives of SSD will be visiting most major high technology cities throughout the country. Professionals interested in exploring career opportunities with Strategic Systems are invited to phone or forward a resume to pre-arrange a convenient appointment in your area. Or if you prefer, you can arrange an appointment to meet with us at our current facility in Needham, Massachusetts. *Phone Jim Poe toll free at 1-800-225-3956, In Massachusetts call 617-449-2000, Ext. 400 or forward your resume to Jim B. Poe, Sylvania Systems Group, Strategic Systems Division, 189 "B" Street, Needham, MA 02194.***

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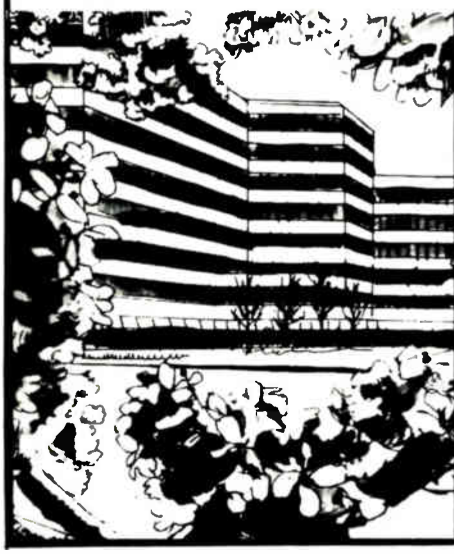

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### Engineering Technician

Layout, build, test prototype digital and analog circuits. Troubleshooting experience a must as well as ASEE or equivalent.

### Electro-Mechanical Designer

Prepare layouts of new products and modifications to existing products as well as perform various tasks related to R&D projects.

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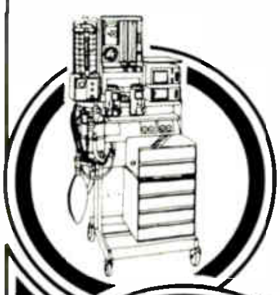

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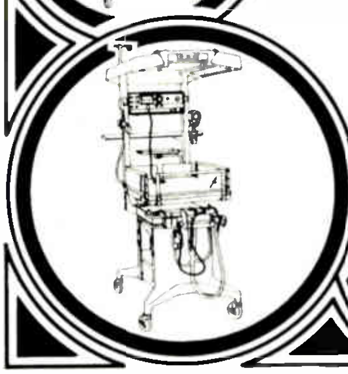

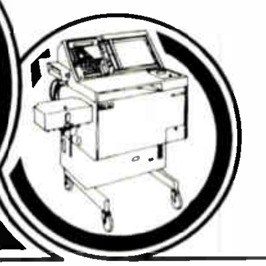

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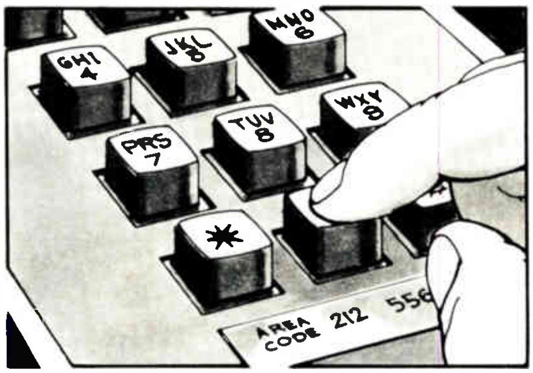


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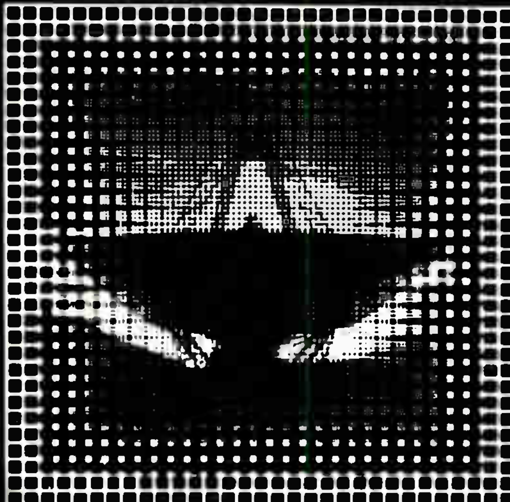

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