AUGUST 14, 1980

A GRAD SCHOOL DESIGNED FOR SOFTWARE ENGINEERS/92

Achieving E-PROM reliability: a two-part article/132

Stepped–sine-wave inverter cuts photovoltaic system cost/121

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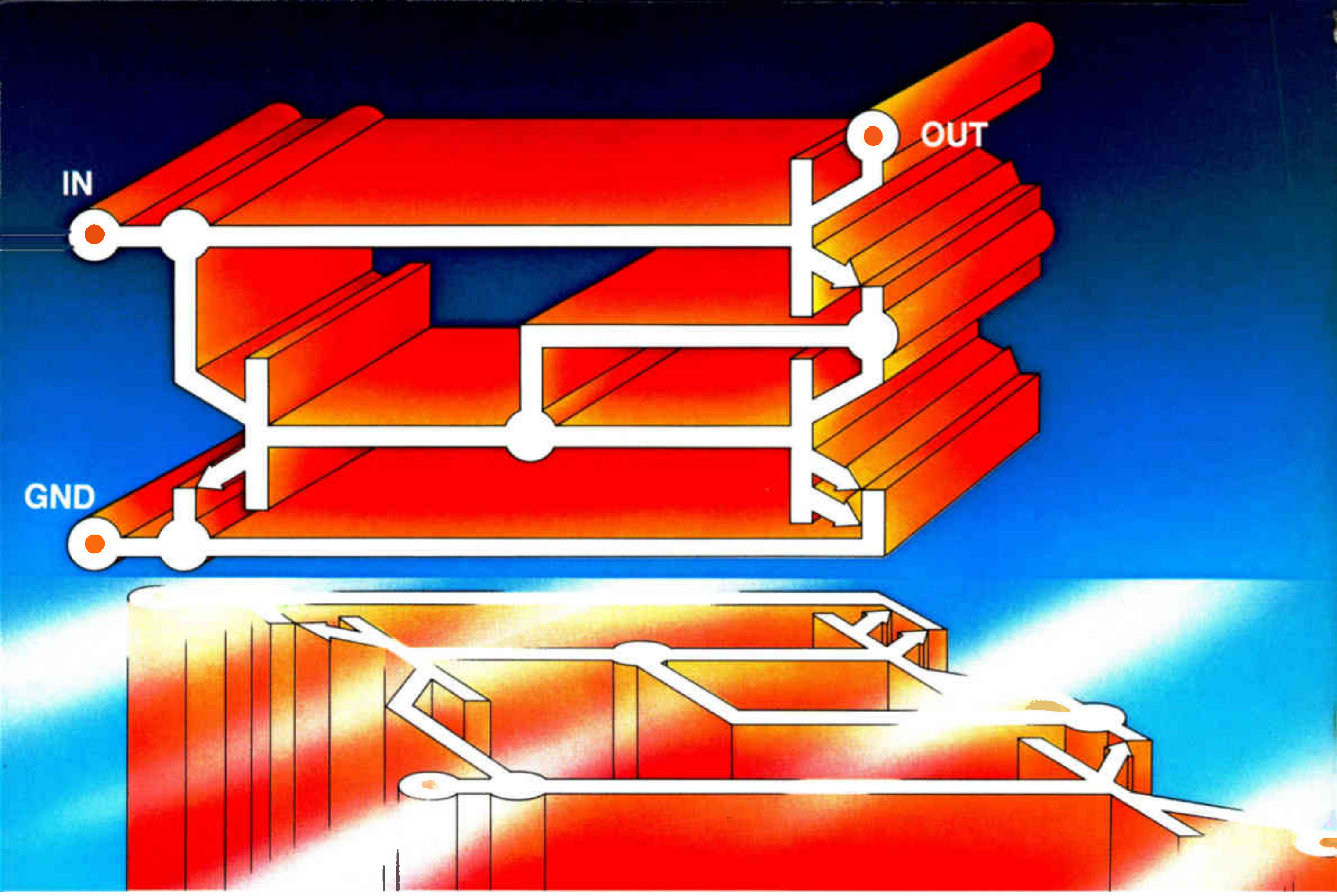

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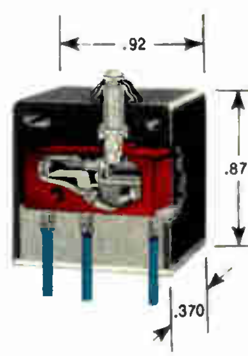

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Electronics

The International Magazine of Electronic Technology

Vol. 53, No. 18 • August 14, 1980

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Highlights

Cover: Delay generator schedules fast tests, 111

A new type of bus-compatible instrument has emerged to join the other forms of instrumentation brought about by the IEEE-488 interface standard: a delay pulse generator, to manage the timing and synchronization of events for automated test and measurement systems. Not only does this programmable unit replace a combination of gear, but it does so at roughly one sixth the cost.

Cover design is by Gabor Kiss.

Software engineers get own grad school, 92

For some time now a matter of concern in the electronics industries, the shortage of software engineers has led to the establishment of the Wang Institute of Graduate Studies near Boston. Offering students a master's degree in software engineering, the school is the creation of An Wang, chairman and chief executive officer of Wang Laboratories.

E-PROMs: their structure and reliability, 132

Ultraviolet-light–erasable programmable ROMs have reached their majority, now that manufacturers have answered the difficult processing questions they posed. These enormously popular read-only memories are the subject of a two-part article written by the firm that led in their design. Part 1 (p. 132) describes the floating-gate memory cell and how it is programmed and erased. Part 2 (p. 136) discusses the various failure modes of E-PROMs and the tests and screening procedures that can be used.

Inverter design rejects transformer to reduce losses, 121

In an attempt to bring photovoltaic power systems for the home closer to reality, French engineers have taken a new tack: they have designed a stepped–sine-wave inverter. The lack of a transformer means the elimination of the iron-core losses that occur during the long low-load periods common in residential use. Solar-cell area requirements are substantially lower, too, thanks to the increased system efficiency.

Peripheral control chip unburdens 8- or 16-bit processors, 143

A universal peripheral controller takes on complicated input/output tasks for 8-bit or 16-bit systems. Based on the Z8 one-chip microcomputer, it adds bus interfacing for multiplexed or nonmultiplexed address and data lines.

And in the next issue . . .

A programmable rf signal generator . . . family controls all types of single- and double-density floppy-disk drives . . . using large-scale integration for pulse-code-modulation repeaters . . . molecular-beam epitaxy nears commercial use.

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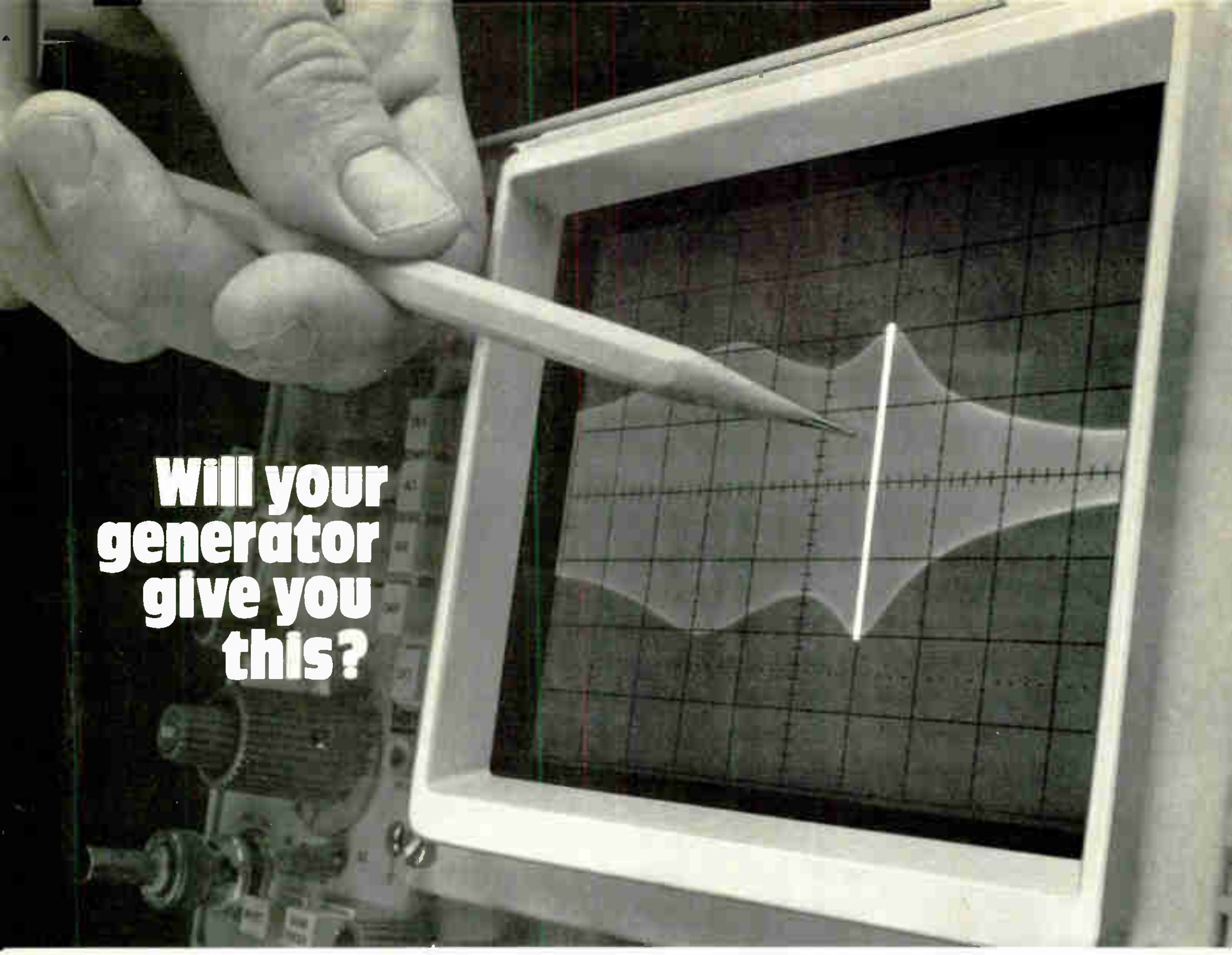

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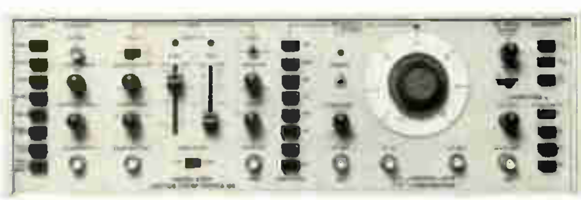

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An excellent example of the crucial role that reliability assurance plays in today's semiconductor industry is the two-part article on the reliability erasable programmable read-only memories that starts on page 132. Part 1 is by Murray Woods, manager of process reliability for Intel Corp. in Santa Clara, Calif. Part 2 is the work of Stuart Rosenberg, who is now manager of quality assurance for Intel's Microcontrol Operation, which is located in Phoenix, Ariz.

The article stresses that reliability is an intrinsic part of a successful semiconductor process. It means investigation into the very heart of a device to understand the physics of a process and thereby pinpoint the failure modes and mechanisms.

Both Woods and Rosenberg have been immersed in reliability and quality assurance. Woods is well remembered for his pioneering work that led to the observation of the effects of alpha particles on memory operation. He has long been interested in nonvolatile memory and was particularly intrigued by the reliability challenges presented by the E-PROM.

"Because we are concerned with reliability in the preproduction stage of a product, it is necessary to learn how a device works in detail—to understand failures and develop screening procedures," Woods notes. "That's what we have done for the E-PROM, but the work won't stop there. For every new product, as speed and density increase, we have to look at new requirements and new environments. We have to start all over every time."

Like many people involved in reliability assurance, Rosenberg came by the job unexpectedly. A 1974 graduate of the University of Wisconsin with a degree in physics, he had hardly heard of reliability until his job interview at Intel. He took a position and has been involved in reliability ever since.

Rosenberg expanded his horizons during a two-year stint at Intel's European quality center. There he spent most of his time working with overseas customers such as Philips and Siemens, an important aspect of reliability assurance. On returning to Santa Clara, he plunged into Intel's HMOS development and later moved into work on the company's E-PROM program.

To Rosenberg, there are fundamental aspects of the E-PROM that set it apart from other memories. "With the floating-gate process, it is necessary to store a finite number of electrons for a long period. Charge integrity is critical. So even the screening tests for E-PROMs are different," he observes.

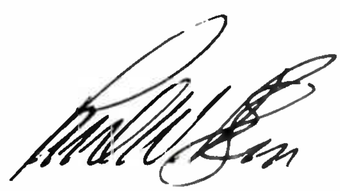
The speed at which the Wang Institute of Graduate Studies (WIGS) moved from conception to fruition is remarkable. According to Linda Lowe of our Boston bureau, who prepared the story on the institute (p. 92), it took only 16 months to organize and ready the school.

This rapid action underscores the urgency and importance that An Wang, chairman and chief executive officer of Wang Laboratories, and the WIGS staff attribute to the project. The campus was in place, albeit as a former seminary. WIGS occupies a 200-acre estate, complete with New England woods and pond.

"I was a little skeptical about the school at first, thinking it might be a promotional maneuver by the company," Linda admits. "But I did a turnaround. The objectives and the organization make me believe that WIGS is the way to go."

The main objective is to have a school that specializes in graduate training in software and that is responsive to the needs of industry. "They don't expect the graduates to go into teaching," says Linda. "The curriculum is organized to reflect what's going on in industry."

Despite all the planning that went into the institute, one thing was overlooked—choosing a mascot for the new school. But Linda has a nomination. How about R2-D2?



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Readers' comments

RCA's rebuttal: SOS part of LSI strategy

To the Editor: I was shocked to read your Probing the News article, "RCA sets SOS aside" [July 31, p. 82]. The headline is totally misleading and absolutely false. The article itself conveys an erroneous impression of RCA's position regarding silicon on sapphire. RCA has not set SOS aside. The article conveys the impression of being the result of an in-depth personal interview and has placed in jeopardy significant present and future business opportunities for RCA. The text, in fact, contains judgments and supposed facts never mentioned in the interview.

As was clearly stated to the interviewers during their visit to RCA, we have chosen a strategic direction for our work in large-scale integration. This strategy is not new to RCA Solid State but, in fact, was fully delineated in an Aug. 16, 1979, memo entitled "RCA MOS LSI Strategy," by R. H. Pollack, executive vice president, RCA Corp. To quote directly from the Pollack memo:

"In the optimization of [complementary]-MOS for packing density, chip size, power consumption, radiation tolerance, cost, etc., it is appropriate to develop and employ more than one process. RCA will compete in the MOS LSI business with a dual technology approach: C-MOS/SOS and bulk silicon C-MOS. We will pursue the development of sapphire background material, and at the same time refine and advance our technology for realizing C-MOS in bulk silicon.

"SOS products will feature performance advantages difficult or unlikely to be achieved with bulk devices. These bulk C-MOS products will serve a very broad market and will be employed where the density/performance/cost tradeoffs are appropriate to the particular application requirement."

The wisdom of this dual approach is compelling and not hard to grasp, but it surprisingly escaped comprehension by the *Electronics* interviewers. Although Carm Santoro has been on our staff only a short time, he has fully embraced our C-MOS LSI strategy. He has summed up the Pollack memo as simply and properly stating that the continued exploration of the right technology for the right product at the right time will be the commitment of integrated-circuit management. I completely support this position.

From the standpoint of its impact on customers and potential customers, the above-stated policy affects two major market segments, Government and commercial applications. RCA Solid State division and the RCA Solid State Technology Center are currently deeply involved in more than 20 Government programs requiring the performance advantages of SOS ICs. The 100 custom and commercial chips being developed for these programs are at all stages ranging from design to production. In many cases—in meteorological satellites, for example—the systems are already in service.

These Government programs offer excellent opportunities for the application of SOS's unique characteristics such as high density, high voltage breakdown, higher speed, and transient radiation hardening.

For commercial applications we currently have in production five random-access memory configurations, an erasable programmable read-only memory, and two high-speed level shifters. Our near-term plans call for faster RAMs and ROMs and larger E-PROMs. For example, we are currently in prototype production of an HDB-3 telecommunications circuit, a 6-bit analog-to-digital parallel (flash) converter, and the CDP1804/05 microprocessor configurations. This commercial posture is consistent with our policy of using the best available technology for a given application.

R. S. Pepper
vice president and
general manager
RCA Solid State Division
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■ Electronics *regrets the false impression conveyed by the article. We mistook RCA's aggressive program in bulk C-MOS LSI for a complete de-emphasis of SOS.*

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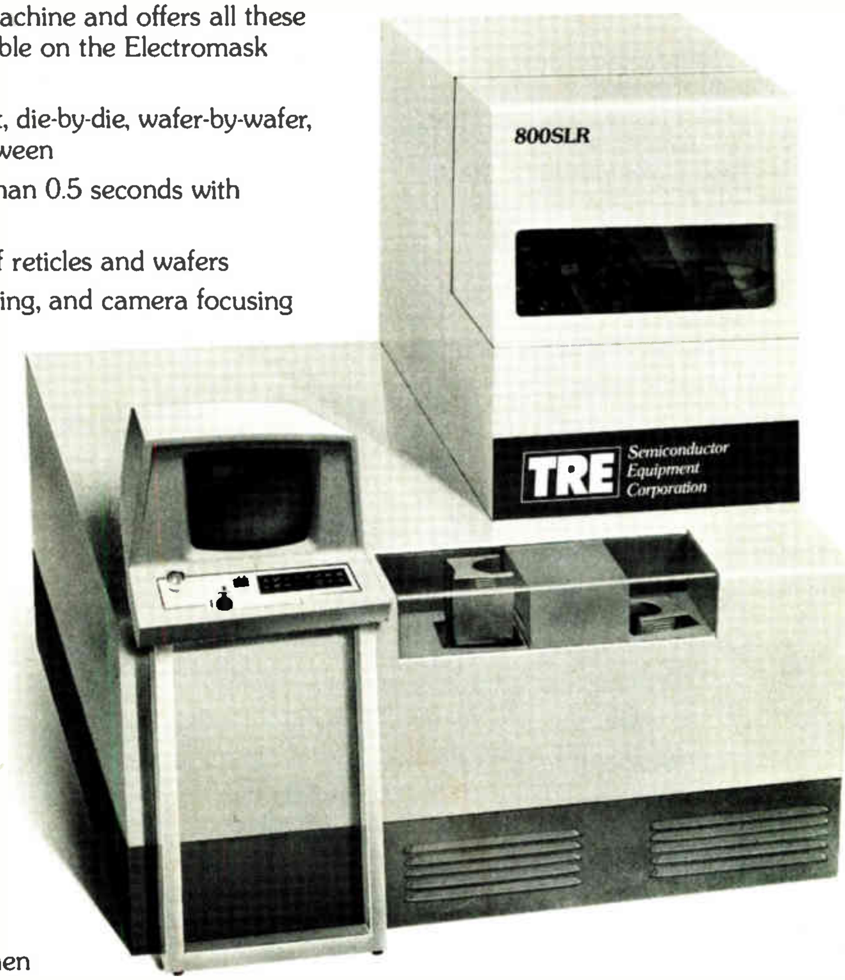

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Editorial

RIP: the reform engineers

It has been noticeable for some time now, the gradual fading of the spirit of reform and restitution that fired the engineering ranks during the mid-1970s. It seems good times have put out the light that burned inside the militants of the last decade. The signs are clear:

Item: For the first time in years, the board of directors' candidates for president and executive vice president of the Institute of Electrical and Electronics Engineers are running unopposed. True, the perennial challenger Irwin Feerst is now on the sidelines with a cardiac condition. But there are no other reform candidates on the horizon.

Item: Also for the first time in years, there is no grass-roots–inspired amendment to the IEEE constitution on the ballot. In the past, a few of the most active sections organized petitions to change the institute's election system, its dues-increasing powers, and other procedures. This year, there's nothing.

Item: The Professional Activities Committees of the IEEE regional sections have fallen silent, while on the national level the Professional Activities Board has drifted off into programs that support careers only indirectly.

The reason for all this quiet is obvious—apathy has once again crept over the EE. Never well-organized or well-led in career programs, the engineering fraternity is easily lulled to sleep by good times.

Priorities have changed. Thus, for example, the call for a lifetime career heard in the 1970s has been softened by those who espouse lifetime employment, as in the Japanese system. The difference here is crucial. In the former, the EE was at the forefront, still an individualist united with other EEs in the pursuit of career goals. In the latter, the employer is asked to assume responsibility for the career plan. We still believe that you get what you work for. Let us hope that it will not require another series of economic shocks to reawaken true professional aspirations.

Opening Europe's telecommunications markets

Britain's telecommunications equipment makers will be stimulated by one of the Conservative Party's latest proposals—to ease the British Post Office monopoly on telecommunications services.

Letting outsiders sell handsets (except the one supplied with the line), private exchanges, and the like to telephone subscribers will parachute innovation into a traditionally staid market. With phone users rather than post office bureaucrats selecting the hardware, the winners in the upcoming open market will be the companies that can transform high technology into equipment with features that people want at prices they are willing to pay.

True to their free-trade beliefs, the Tories will give foreign firms a shot at the subscriber-equipment market after an initial period of about three years of competition between the BPO and the British suppliers. But the British government has set a condition that makes uncommon good sense: imports can come only from countries that allow reciprocal fair access to their own telecommunications equipment markets. That shuts out Japanese suppliers, who for once will not be able to crash into an export market while enjoying a well-protected home market.

Indeed the electronics industries in other countries should use this example to convince their trade officials to take the same stance as their UK counterparts. Reciprocity in foreign trade, especially for high-technology products, is a reasonable demand. Free trade fosters technological innovation and thus is essential to the industries' growth. But this truth should not obscure the fact that free trade is never a one-way avenue.

People

Optron's Ehman to guide advanced optics to market

Capitalizing on the anticipated boom in optoelectronics and fiber-optic systems will require not only improvements in technology but also sound business planning. As the new vice president of materials technology and development for the Optron division of TRW Inc., Michael F. Ehman has a job encompassing both.

Joining Optron last February following nine years of materials-related engineering and management experience at Rockwell International Corp., the 35-year-old Ehman is overseeing completion of a new 5-micrometer TTL production line scheduled for startup next month at the firm's Carrollton, Texas, headquarters.

Replacement. The new line will replace a 10-μm process, providing significantly increased capacity and improved ability to integrate photodetectors with logic circuitry, Ehman notes. As a $6 million investment, it also demonstrates TRW's plans to support the Optron operation, acquired by the Cleveland, Ohio-based industrial conglomerate in early 1979.

The Texas manufacturer of infrared optoelectronic devices and assemblies has been growing at about a 54% pace, with projected sales this year of about $33 million. "My job is to help the firm through the transition from a small company to a large corporation," Ehman says. His twofold assignment involves injecting advanced technology into the company and providing the marketing guidance to maximize the effectiveness of TRW's capital investment.

He reports that the new TTL line will provide an ion-implantation capability that will permit the production of faster photodetectors to keep up with today's faster microprocessors. Eventually, it will turn out avalanche protodetectors.

Emitters. On the emitter side of the optoelectronic equation, Optron is looking at gallium aluminum arsenide LEDs, moving on from its present GaAs light-emitting diodes. Further away, the company hopes to get into laser technology with injection laser photodiodes.

Opportunity. Michael Ehman plans for the growth of optoelectronic devices.

With a Ph.D. in solid-state chemistry from Pennsylvania State University and his broad process and materials experience at Rockwell, Ehman is well suited for the technical portion of his job. To strengthen his management skills, he is pursuing a degree in the executive master of business administration program at Southern Methodist University in Dallas.

Space shuttle will change satellites, says RCA's Wright

The age of the space shuttle is imminent, and it will usher in the next generation of satellites, believes Paul E. Wright, division vice president and general manager of RCA Astro Electronics. What's more, what the U. S. makes of the new age may well decide whether American manufacturers maintain a dominant role in the satellite business.

"For years we have played this [satellite] business as a one-shot game," says the 47-year-old Wright, who has headed up RCA's space development center since last fall. "The space shuttle is big enough to carry many satellites at once. That's going to change the economics of putting a communications satellite into orbit. It might cut the total cost of ownership by from 15% to 20%."

"We have to realize the strong

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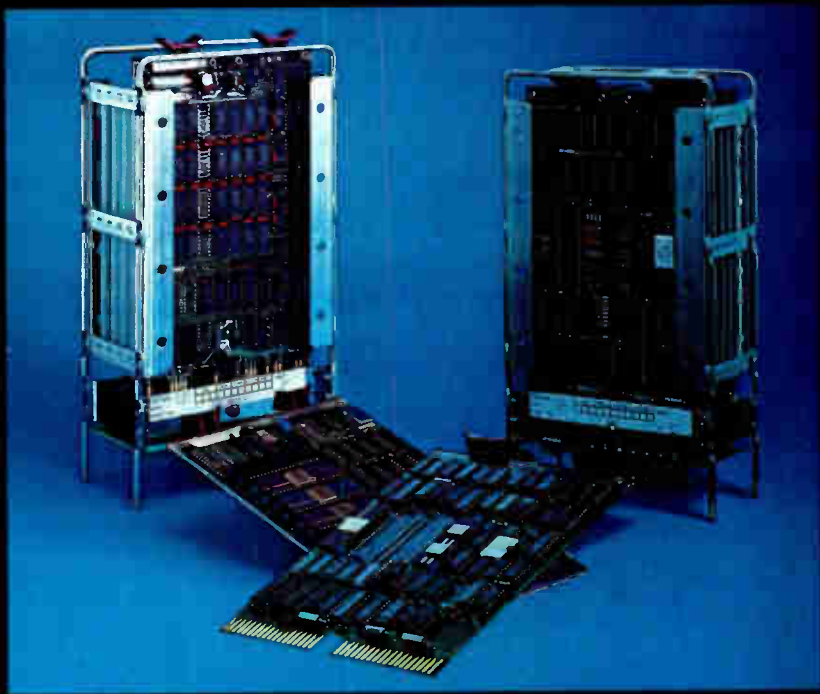

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People

More. RCA's Paul Wright forsees new satellite technology, thanks to space shuttle.

position we have now with the space shuttle. It will be a wasted investment unless we design satellites to take advantage of it," he feels.

Watch out. But, he warns, "we've got to continue to accelerate our productivity in the space business. Productivity has to have a much broader meaning, or in 1990 we'll find that Japan or West Germany is the dominant maker of satellites."

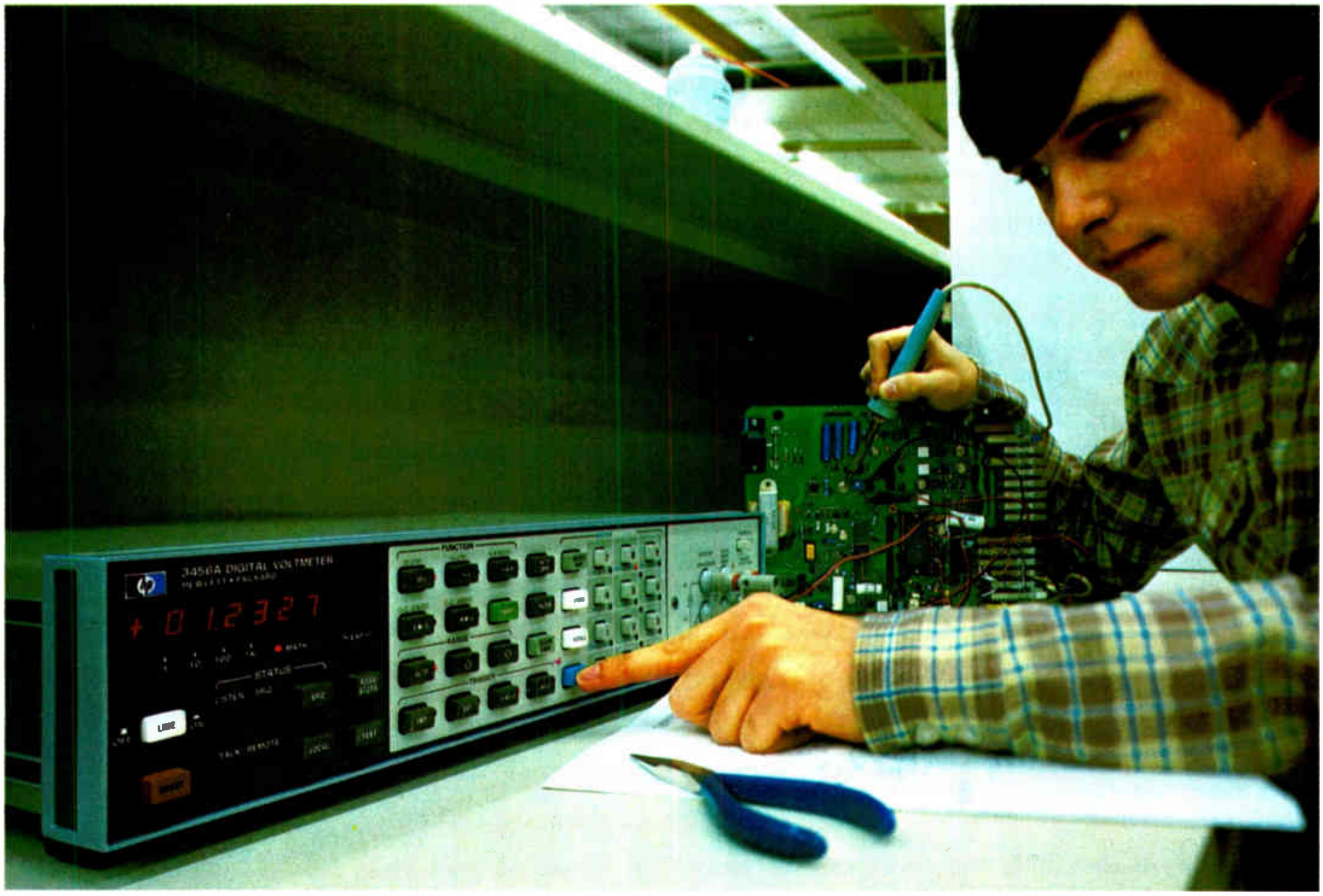
Wright has had a deep involvement in RCA's space program during his 22 years with the company. He can quickly sketch the shape of satellites to come from Astro Electronics, a Princeton, N. J., operation of the Government Systems division.

Sending the satellites up in the space shuttle means that no longer are there such stringent geometric or weight limitations, he says. But because satellite engines now may be running on standby during the space shuttle ascent, "you have to take into account temperature control, outgassing, and thermal idling because of the shuttle crew—as well as new boundary considerations because several satellites will be housed in the shuttle."

According to Wright, three problems influence productivity in the satellite business today. One is finding enough qualified engineers to design and build the product. Another is implementing advanced technology concepts in practical designs. The last is trying to get U. S. vendors to deliver satellites quicker in order to capture a large share of the growing communications market. □

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

AUGUST 1980



Obtain outstanding precision and speed in your measurements with HP's new DMM

You don't have to compromise measurement accuracy, noise or resolution to get fast DMM readings. Hewlett-Packard's new integrating 3456A 3½ to 6½-Digit Multimeter for bench and system use allows you to choose the best speed, or the best accuracy or resolution for a particular application, simply by pushing a button.

An important key to this flexibility and nearly uncompromising capability is the 3456A's selectable integration time, ranging from 0.01 to 100 power-line cycles. If reading rate counts, an operator can select up to 330 readings per second for high-speed bursts or one reading every 15 minutes for periodic measurements. When accuracy is more important, stretching the integration time increases the accuracy. You can also select resolution of 100 nV at up to 48 readings per second (6½ digits) or 10 μV resolution up to 330 readings per second (3½ or 4½ digits).

This fully-guarded, microprocessor-based DMM also provides a wide repertoire of other features. Its dc voltage capability extends from 0.1 to 1000 V in five ranges and it measures up to 700 V of calculated true-rms on four ranges, over 20 Hz to 250 kHz. In addition, the 3456A offers resistance measurements, mathematical calculations controlled from the front panel (statistics, null, percentage error, dB, limits, scaling), and a built-in memory of up to 1400 bytes.

A technique called Offset Compensated Ohms is incorporated in the 3456A to correct resistance measurements for undesirable thermal offsets generated by bimetallic junc-

(continued on third page)

HP's lowest priced synthesized signal generator now available for 0.1 to 990 MHz applications

Full HP-IB programmability under microprocessor control makes the new HP 8656A Signal Generator particularly well-suited for automatic test stations as well as for manual testing in the lab and in the field.

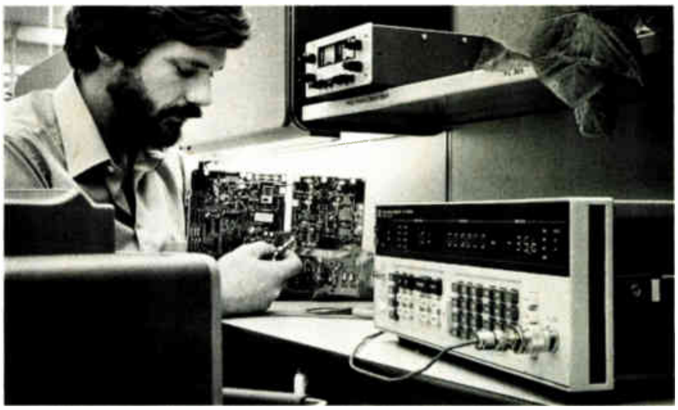
For manual applications, the 8656A has been designed to minimize the time required to set up desired signal conditions of frequency, output level, and modulation. All signal conditions are keyed-in directly in the units desired, such as MHz and dBm. What's more, the microprocessor permits keying in of non-traditional units such as dBμV (dB referenced to a microvolt) useful in broadcast stereo work. For high impedance loads, the output can be calibrated in EMF.

An important advantage to repetitive testing is the 8656A's store/recall mode. It can remember 10 complete, front panel, signal set-ups and recall each at a touch of two keys. In production test, the 10 conditions can be sequenced with a rear panel contact closure to ground, connected to a foot switch.

Output frequency covers a very broad application range from long range navigation (100 kHz) to beyond cellular telephone (990 MHz). Resolution is 100 or 250 Hz while stability results from an internal 2 ppm per year time base. Intended primarily for in-channel receiver tests, the single sideband phase noise is <-122 dBc/Hz at a 20 kHz offset at 225 MHz.

Calibrated output level from +13 to −127 dBm has an absolute accuracy of ±1.5 dB, resolution of 0.1 dB, harmonics <-25 dBc, non-harmonic spurious <-60 dBc, and reverse power protection of 50 W.

AM from 0-99% is available at internal rates of 400 and 1000 Hz. FM ranges up to 99 kHz peak deviation (depending on carrier frequency) at 400 and 1000 Hz rates. For calibrated external AM or FM (at rates up to 25 kHz), two limit lights indicate proper input amplitude of 1 V peak.



HP-IB programming is standard in HP's new 8656A Signal Generator. In that mode, fequency switches in less than two seconds (to be within 100 Hz).

All display values can be incremented with up/down keys and increment sizes are set in the same fashion as other function data by the keyboard. Holding down an up/down key causes continual step "tuning" and replaces the need for knobs.

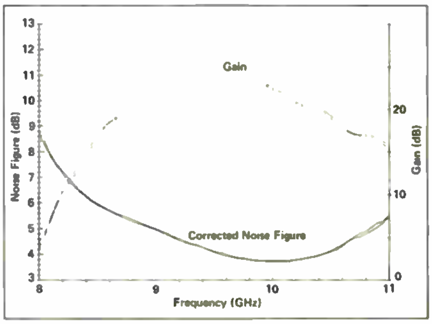
Check B *on the HP Reply Card.*

New application note describes how to make accurate repeatable noise figure measurements 10 MHz to 18 GHz

Application Note 64-3, *Accurate and Automatic Noise Figure Measurements*, details how to use the HP 436A Digital Power Meter, under desktop computer control, to measure Y-factor and compute noise figure. This new, high-accuracy technique depends on the implementation of the new HP 346A 10 MHz - 18 GHz Noise Source which reduces measurement uncertainty because of its low SWR.

Demonstration software routines in AN 64-3 include techniques for measuring noise figure and gain of microwave components. Further, the note covers use of the computer to correct second stage noise figure, ambient temperature, and ENR (excess noise ratio) variation vs. frequency.

For a complimentary copy of AN 64-3, check C *on the HP Reply Card.*



Corrected noise figure and gain of an X-band Amplifier shows good repeatability.

How to select the right RF signal generator

A new, colorful, 8-page Selection Guide for RF Signal Generators and Sources is now available. It describes HP's signal generator capabilities between 10 kHz and 2600 MHz. Specification comparisons are made for nine different generators ranging from the manually-tuned 8654A L-C type to the high-performance 8662A Synthesized Generator.

The application selection chart compares critical parameters required for nine separate measurement applications ranging from L.O. substitution to the stringent out-of-channel radio test procedure. A single-sideband, phase noise comparison chart for five generators appears for the first time, as well as a glossary of terms to round out the user-oriented information in this brochure. Capsule descriptions of each generator are provided.

For a free copy check D *on the HP Reply Card.*

Extend MLA test capability to RF

The new 3730B Down Converter offers extended frequency coverage and many new features to improve measurement accuracy.

The new 3730B Down Converter is a replacement for the now obsolete 3730A model and offers many outstanding new features. It provides RF to IF conversion, permitting an RF interface capability for Microwave Link Analyzers (MLA's). The extended RF range, 1.7 to 14.5 GHz, is accommodated by a series of broadband, plug-in RF Modules.

In addition to extended RF coverage and a much improved residual performance, this latest down converter provides a special tracking AFC and recovered sweep facility which causes the local oscillator in the 3730B to track the incoming swept RF signal. Because of the effective sweep compression of the IF signal, the 3730B allows measurements with conventional MLA's over bandwidths of up to 250 MHz.

Lengthy runs of RF cables between the down converter and the RF test point may generate ripple responses which can mask the true measurement response. To avoid this problem, it is possible to remove the down converter plug-in and mount this directly onto a waveguide test point. The plug-in is then connected to the 3730B mainframe by an umbilical cable, which carries only IF signals.

Other new 3730B features are: upper/lower sideband operation to eliminate difficulties when comparing MLA responses between microwave radio repeater stations; provision for incorporating an RF Input Isolator to improve noise figure, input VSWR, and local oscillator leakage; and interface capability with 70 or 140 MHz IF MLA's.

Check E on the HP Reply Card.

New "SC" crystal-cut and efficient electronics provide superior quartz oscillator performance

These two new, high-performance oscillators were designed for instruments, communication and navigation equipment, and precision timekeeping systems.

If your equipment requires a compact, rugged precision frequency source with fast warmup, high stability, or low phase noise, consider HP's two new oscillators, the 10811A/B. Both can be built into your equipment to provide the following key specifications:

Output frequency: 10 MHz (10.23 MHz on special order).
Aging Rate: <5 parts in 10^{10}/day
Phase Noise: >160 dBc at 10 kHz offset
Warmup: Within 5 parts in 10^9 of final frequency in 10 minutes.
Time Domain Stability: 5 parts in 10^{12} for a 1-second averaging time.
Power consumption: 2 Watts.

They are plug-compatible with HP's other compact quartz oscillators, the 10544A/B/C. Models 10811A and B differ in 1) the methods of making electrical connections and, 2) model B has provisions for shock mounting.

*Check **F** on the HP Reply Card.*

Have your speed and accuracy too with this new DMM

(continued from first page)

tions. This allows the user to select any kind of metal for the test leads, without worrying about the metal on the resistor leads.

Standard on the 3456A is an isolated HP-IB (IEEE-488) I/O for the systems operation. The front panel indicators on the 3456A display range, function and HP-IB status during remote operation. Also on the front panel is a SRQ (Service Request) button which can be used to flag or interrupt a computer. When combined with the 3456A's program memory and reading storage capability, system programmers and operators need to use only one desktop or minicomputer to control numerous test stations.

Another system feature of the 3456A is its hardware scanner advance capability. As soon as the 3456A's measurement cycle is complete, a TTL signal is available to trigger an HP 3495A Scanner or 3497A Acquisition/Control Unit to advance to their next channel. Up to 330 channels can be scanned per second without computer interaction.

With a 2 PPM stability, the HP 3456A is a true transfer standard with its 100 nV sensitivity and 0.001% accuracy. A statistics function key (STAT) enables the operator to improve the 3456A's sensitivity, resolution and accuracy by averaging.

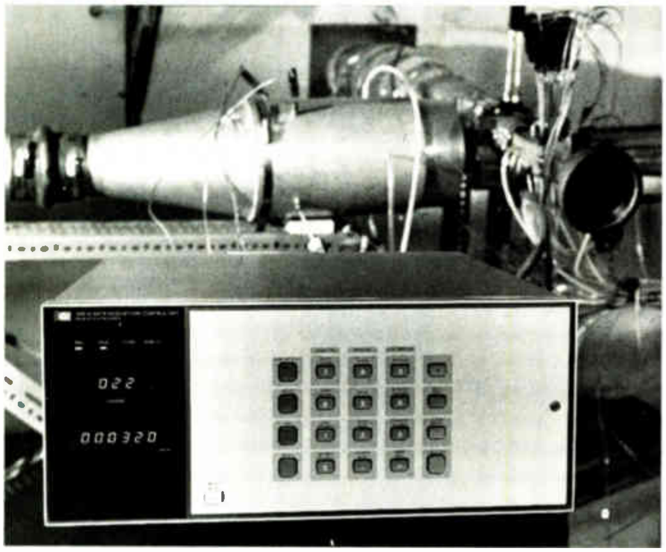
Calibration of the HP 3456A is fast and convenient since all routine adjustments are accessible from a concealed door in the front panel.

*Check **B** on the HP Reply Card.*

HP introduces a low-cost solution to data collection in a variety of applications

If you've been looking for a low-cost solution to data collection problems in applications such as component and production test, environmental monitoring, production process monitoring, and evaluation and quality assurance, consider HP's new 3497A Data Acquisition and Control Unit.

A powerful tool that's easy to use, the 3497A consists of a clock/timer, front-panel keyboard and display. Optional plug-in assemblies enable the user to customize the 3497A for a specific data logging/acquisition application.



Dedicated keys such as "Current Source" or "Voltage Source" can be programmed from the front panel, making it ideal for system configuration and troubleshooting.

Friendly and Powerful Keyboard

The simple front panel keyboard with dedicated keys makes the 3497A easy to understand and operate. Should the operator wish to observe a particular analog channel or digital slot without disturbing running measurement, all that is required is to press a "Viewed Channel" or "Viewed Slot" key. Keyboard control also lets the operator evaluate different 3497A configurations before writing a program. After a program is written, the operator can quickly verify system configuration or troubleshoot.

Standard in the 3497A is a non-volatile quartz reference clock-timer. Complete timing from months to seconds can be programmed from the front panel. It can monitor elapsed time (stopwatch) or interrupt at a pre-set time (alarm clock).

Options for your flexibility

A number of optional, plug-in, multiplexer assemblies are available for scanning inputs. The maximum of 1000 analog channels and 1360 digital lines is available when using HP's 3498A Extenders with the 3497A. An optional, plug-in, 5½-digit integrating DVM assembly provides one μV resolution, 0.0005% best-case accuracy, auto-ranging with maximum reading rates to 300 per second (3½ digits) and memory storage up to 100 readings.

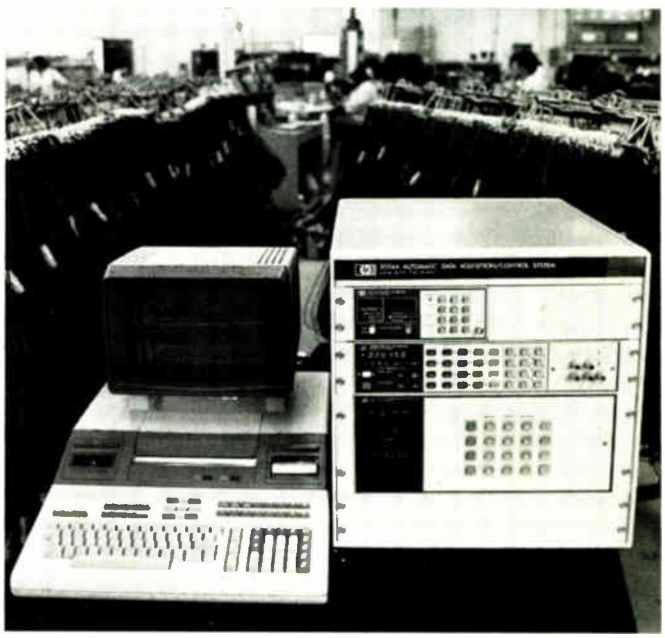
Check **H** *on the HP Reply Card.*

Powerful, new data acquisition system gives you high speed at low cost per channel

A powerful, new data acquisition system with full computation and analysis capabilities now makes available impressive speed and accuracy at an economical rate.

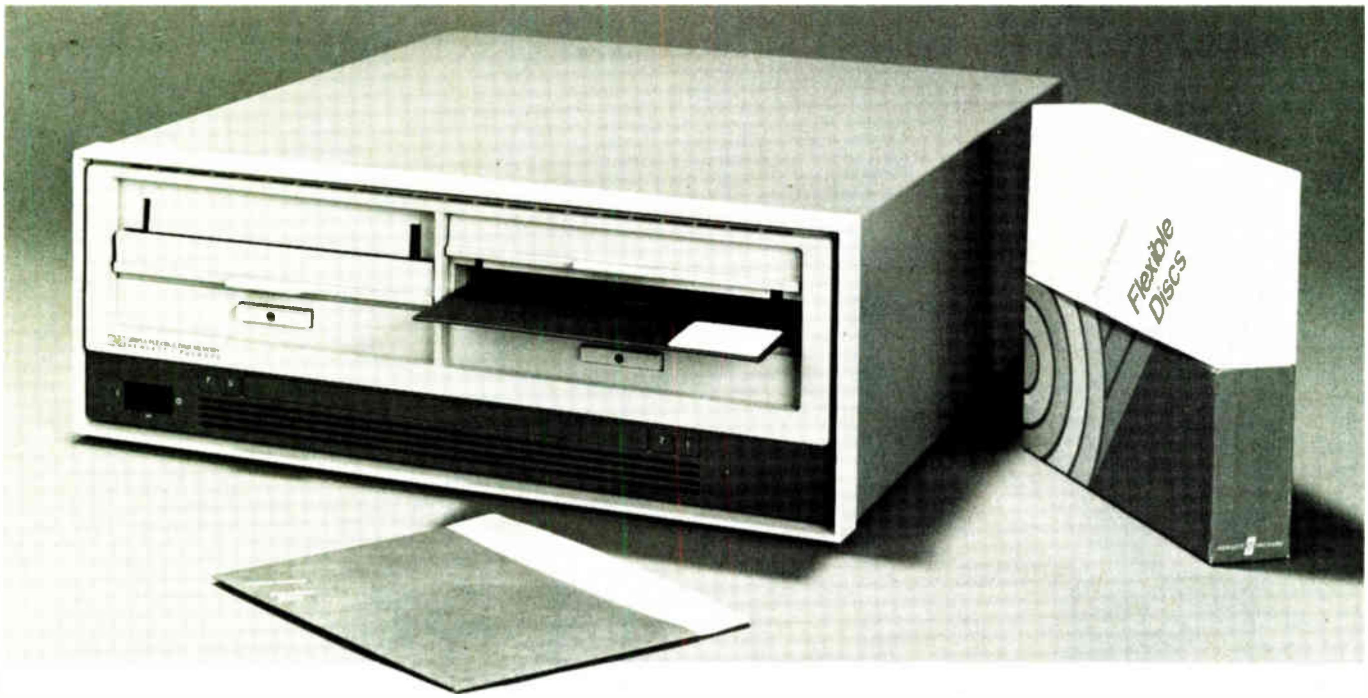
This new HP 3054A system offers a range of features to deal with your needs in process control development, transducer measurements, production testing, research and development, and signal analysis. Consisting of an HP desktop computer, an HP 3497A Data Acquisition/Control Unit, and HP's 3437A and/or 3456A Voltmeters, the 3054A system also accommodates a number of options to further augment its performance and versatility. The 3437A Digital Voltmeter gives this system the flexibility of very fast (5,000 readings per second) measurements, with waveform characterization.

Powerful system software, including instrument driver routines, data analyses and presentation programs, instrument verification routines, and application programs are provided with the 3054A system which uses HP's 85A, 9825T, 9835S or 9845T Desktop Computers. Each of the computers has different capabilities so you can choose the level of performance that your application demands. For example, read/write memory ranges from 32K bytes in the 85A up to 449K bytes in the 9845T



For complete details,check **I** *on the HP Reply Card.*

New, double-density flexible disc memory provides increased personal mass storage



Hewlett-Packard's new, double-density 9895A Flexible Disc Memory offers up to 2.36 million bytes of formatted, mass storage capacity for the HP System 45B Desktop Computer and the HP 1000 Minicomputer series.

The Hewlett-Packard 9895A Flexible Disc Memory provides a convenient way to store and retrieve up to 2.36 million bytes of additional mass storage for your HP 45 Computer and HP 1000 minicomputer series.

The increased storage capacity offered by the 9895A lifts the storage constraints you may have experienced with tape or single flexible disc drives, without the expense of hard discs.

Each of the two drives in the HP 9895A reads double-sided, double-density format on HP-qualified, flexible discs. The drive can store up to 590,000 bytes of formatted data per side, for a total of 1.18 million bytes per disc.

Price/Performance Flexibility

A total storage capacity of up to 4.72 million bytes can be provided through an optional dual-drive slave unit (without controller). This is one of several options designed to provide you price/performance flexibility. A single-drive slave offers an extra 1.18 million bytes of storage, and the dual-drive slave provides an additional 2.36 million bytes. For 1.18 million bytes capacity, the 9895A can also be ordered with one drive installed with controller. You can easily upgrade these options to full 9895A capability at a later date if you choose.

Single-Drive Compatible

The built-in controller enables the 9895A to recognize whether a disc has been recorded on one or two sides. This capability allows it to read single-sided discs written by the HP 9885M or 9885S flexible disc memories, making it convenient for present 9885 owners to convert to the new drive. The 9895A can also write on any 9885 single-sided disc, and the 9885 will be able to read the disc. (A 9885 cannot read 9895 double-sided flexible discs, however.)

The IBM Exchange

Many of today's applications call for both data exchange with IBM mainframes or use of data that has been generated on IBM products. HP designed the 9895A, enabling it through its built-in controller, to conveniently and reliably recognize if a disc is written in IBM 3740 single-density or in HP's double-density format. Software available for HP System 45 also allows the user to easily read and write IBM discs.

Stand-Alone Reliability

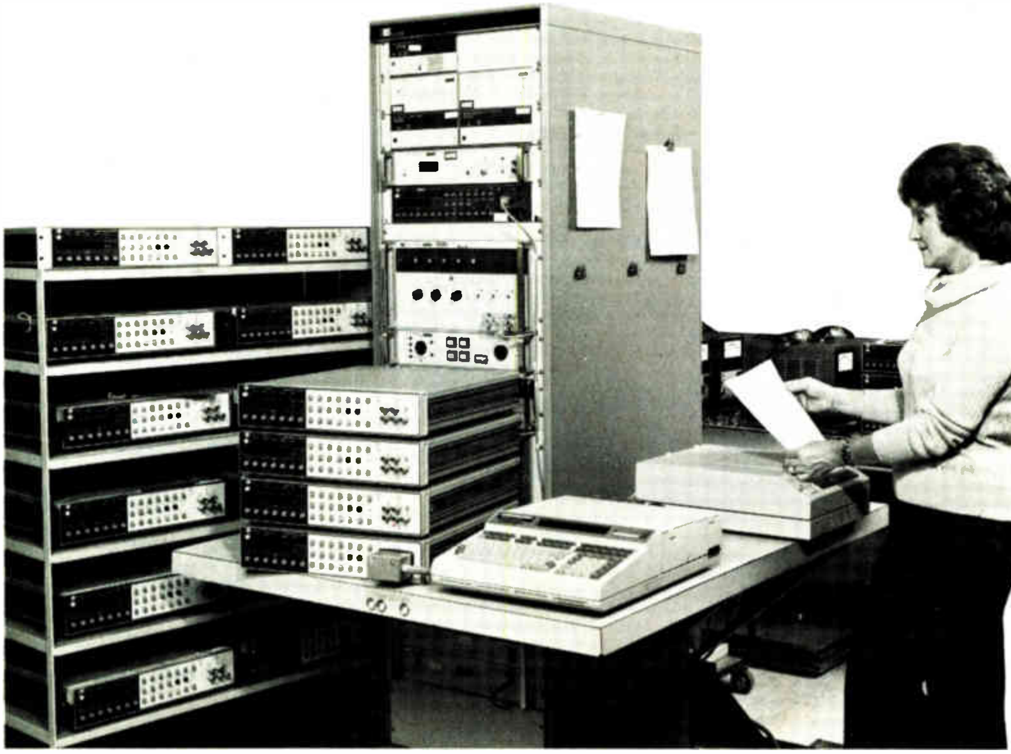
The 9895A is patterned after similar flexible disc drives currently integrated into other HP business and technical computers—the HP 250, HP 300, and HP 3000 Series 30 and 33. The 9895A also has extensive self-test capabilities which are accessible to the host controller. A hardware self-test is initiated and reported at powerup. Read/write tests can be initiated manually by the operator or remotely through HP-IB using the host computer. The 9895A's intelligent controller can detect and mark bad tracks, as well as renumber good tracks sequentially to maintain organization in a logical manner.

Quality Media

You are assured of approved, quality media thanks to Hewlett-Packard's extensive QA testing, selection and control over its flexible discs. These HP qualified discs bring out the most reliable performance in the 9895A disc drive and are among the full line of HP computer supplies readily available for your convenience through local HP sales offices, and distribution centers located both in the U.S. and Europe.

Check J on the HP Reply Card.

HP's fastest desktop controller now has twice the memory



A 25T Desktop Computer controls the automated testing of digital voltmeters, acquires test data and prints out results on an HP 9876A Printer.

The HP 9825 Desktop Computer is now available with up to 62K bytes of read/write memory, with no loss of the speed on which the 9825 built its reputation.

Two Models

Reducing the physical size of the memory inside the 9825 and devising a hardware block-switching scheme have made possible the introduction of the two new models, the 9825B and the 9825T. Both are completely compatible with programs written for the 9825A or S.

The 9825B has 23K bytes of read/write memory and internally integrated ROMs (read-only memories) for many functions that were previously available only as plug-in options. These internal ROMs are: Strings, Advanced Programming, Plotter, General I/O and Extended I/O.

The 9825T has 62K bytes of read/write memory, all the built-in ROMs contained in the 9825B, and, in addition, a built-in Systems Programming ROM. This internal Systems Programming ROM in the 9825T can be used concurrently with the Matrix ROM. Due to addressing limitations, this is not possible in the 9825A, S, or B.

The Systems Programming ROM is still available as a plug-in option for the 9825B. The Matrix ROM and the 9885 Flexible Disc ROM are available as options for both the B and T models.

In addition to the read/write memory and ROM changes, the 9825B/T includes the improved typewriter keyboard that was introduced on the 9825A/S several months ago. It provides higher reliability and a familiar, typewriter-like feel that makes entry faster and more comfortable.

Easy Upgrade from 9825A/S

An upgrade kit is available to convert any 9825A or 9825S into a 9825T. Local HP sales office personnel can install the kits at either the HP sales office or at customer locations.

The upgrade kit provides 62K bytes of read/write memory, built-in option ROMs, option ROM compatibility and software compatibility. And an upgraded 9825T will operate with all the speed it did when it was a 9825A or S.

HP's Premier Desktop Controller

The 9825 is HP's fastest desktop computer for data acquisition, instrument control and computation. It can perform direct memory access at up to 800K bytes per second, fast read/write at up to 70K bytes per second, and formatted read/write at up to 16K bytes per second.

The 9825 has three I/O slots (expandable to 14) and four ready-made plug-in interface cards are available: HP-IB (IEEE-488), 16-bit parallel, bit-serial (RS-232C) and binary-coded decimal (BCD). An optional real-time clock can also be plugged into one of the I/O slots.

A complete line of peripherals is available to complete any 9825 system—page printers, plotters, flexible disc, magnetic tape cartridge drive, digitizer, paper tape and card readers and a paper tape punch.

The 9825's usefulness grows every year as the number of available HP-IB instruments increases. There are now well over 100 available from Hewlett-Packard and hundreds more from other manufacturers.

Check K on the HP Reply Card.

HP-85 personal computer gets advanced I/O capability and three I/O ROMs

The combination of I/O ROMs and HP-IB module enable the HP-85 to control a large number of instruments in data acquisition applications.

Hewlett-Packard's HP-85 personal computer for professionals is now even more powerful and versatile. This additional capability is made possible by the HP-IB interface module and three I/O ROM's, all of which can be plugged into the HP-85's ports.

The HP-IB interface module is a complete implementation of the IEEE-488 standard. It enables the HP-85 to communicate with up to 14 instruments plus a variety of peripherals, such as plotters and printers.

ROM's enable the user to get maximum benefits from the peripherals and instruments by providing additional BASIC language commands. The I/O ROM provides statements to configure, control, pass data and check the status of devices in the system. The Plotter/Printer ROM extends the basic graphics commands in the HP-85 while the Matrix ROM allows extensive, one-and two-dimensional array manipulation.

Twelve application pacs in science, engineering and finance make the HP-85 an adaptable tool that the technical or business professional can use immediately to solve problems.

Check A *on the HP Reply Card.*

New, easy method permits quick retrofitting for signature analysis

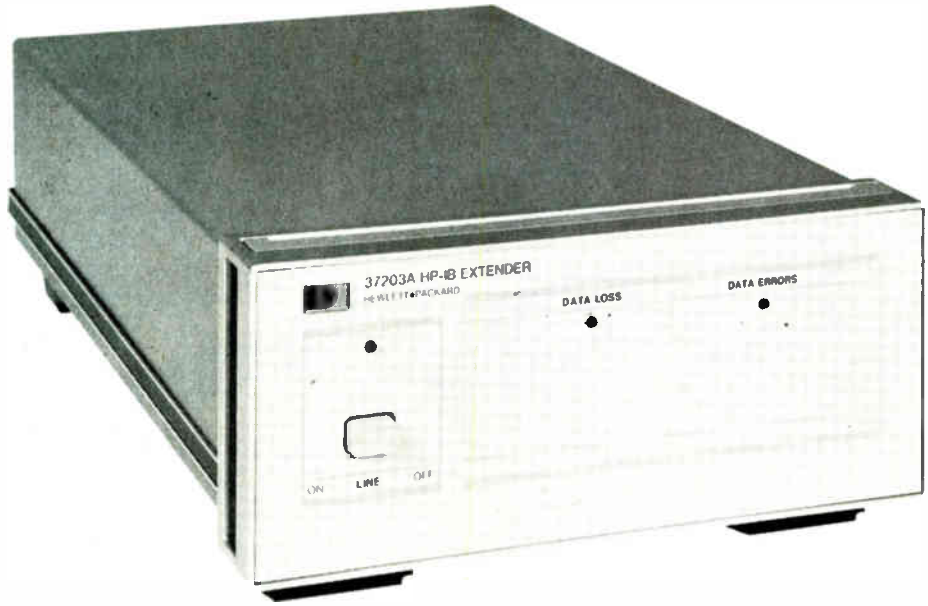
Just plug your product's 6800 microprocessor into HP's new 5001A Microprocessor Exerciser, plug the 5001A cable into the now vacant microprocessor socket, and the major hardware and software part of your retrofit for Signature Analysis (SA) is done. It's that simple and it costs less than providing test stimuli through incircuit emulation techniques.

The 5001A Exerciser takes control of your product's buses and runs test stimulus programs from its own ROM while you use an HP 5004A Signature Analyzer to take signatures at designated circuit points for each test stimulus. These signatures help you pinpoint malfunctions right down to the component level. This saves you time and money compared to the hit-or-miss, board exchange, troubleshooting method.

For 5001A/5004A details, check L *on the HP Reply Card. For an index to signature analysis publication, check* M.

Now you can troubleshoot your microprocessor-based products quickly and economically through Signature Analysis—even if you didn't design it in.

DESIGNED FOR HP-IB SYSTEMS New, fast HP-IB extender operates over coaxial cable or fibre optic link



The new 37203A lets you extend operation of your HP-IB systems up to 1000 metres using coaxial cable or a fibre optic link.

HP's new 37203A HP-IB Extender provides a high-speed, low-cost solution for HP-IB extension up to 1000 metres. Operating in pairs, each 37203A serializes the HP-IB information and transmits it over coaxial cable or a fibre optic link to a remote 37203A which reconverts the serial data to parallel HP-IB format.

The 37203A is fast — providing information transfer at rates up to 50k bytes/second. It is also inexpensive and the basic unit is designed to operate over a single, low-cost coaxial cable. An optional fibre optic interface is also available which allows HP-IB Extenders to operate over a dual fibre optic link up to 1000-metres long.

Integrity of HP-IB extension is assured by isolating the data from electrical interference — the fibre optic link provides complete immunity to electro-magnetic pick-up and even the coaxial cable interface is optically isolated. A further measure of protection is provided by a simple error detection/correction algorithm which automatically identifies and corrects any transmission errors.

The 37203A is easy to use, and no special programming is required. It is transparent to HP-IB operation and suports the full range of HP-IB procedures including Pass Control and a form of Parallel Poll.

Check N *on the HP Reply Card.*

East-4 Choke Cherry Road, Rockville, MD 20850, Ph. (301) 258-2000
South-P.O. Box 10505, 450 Interstate North Pkwy., Atlanta, GA 30348, Ph. (404) 434-4000.
Midwest-5201 Tollview Dr., Rolling Meadows, IL 60008, Ph. (312) 255-9800.
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HEWLETT PACKARD

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

July/August 1980

New product information from

HEWLETT-PACKARD

Editor:
Bojana Fazarinc

Editorial Offices:
1507 Page Mill Road
Palo Alto, California, 94304 U.S.A.

00084

Meetings

The 12th Conference on Solid-State Devices, Japan Society of Applied Physics (3–5–8 Shiba Koen, Minato-ku, Tokyo 105), Tokyo Chamber of Commerce & Industry Building, Aug. 26–27.

10th Symposium on Electromagnetic Theory, Verband Deutscher Elektrotechniker (D-6000 Frankfurt 70, Stresemannallee 21, West Germany), Munich Technical University, Aug. 26–29.

The 15th International Conference on the Physics of Semiconductors, Physical Society of Japan (Hiroshi Kamimura, Department of Physics, Tokyo University, Tokyo), Kyoto International Conference Hall, Kyoto, Sept. 1–5.

Electronic Business Communications Conference, Electronic Industries Association (2001 Eye St. N. W., Washington, D. C. 20006), Las Vegas Convention Center, Las Vegas, Sept. 3–5.

Second International Colloquium on Reliability and Maintainability, Centre National d'Etudes des Télécommunications and Centre National d'Etudes Spatiales (CNET Reliability Center-Lannion B, B. P. 40—22301 Lannion, France), Perros-Guirec and Trégastel, Brittany, France, Sept. 8–12.

Oceans/80, Ocean Engineering in the 1980s, IEEE and Council on Oceanic Engineering, Seattle, Wash., Sept. 8–10.

10th European Microwave Conference 80, Association of Polish Electrical Engineers (Microwave Exhibitions & Publishers Ltd., Temple House, 36 High Street, Sevenoaks, Kent TN13 1JC, England), The Palace of Culture and Science, Warsaw, Sept. 8–12.

Electrical Overstress/Electrostatic Discharge Symposium, Illinois Institute of Technology Research Institute (IITRI Symposium, RADC/-RBRAC, Griffiss Air Force Base, Rome, N. Y. 13441), Town and Country Hotel, San Diego, Calif., Sept. 9–11.

Convergence-80—30th International Congress on Transportation Electronics and Vehicular Technology Society Conference, IEEE and Society of Automotive Engineers, Hyatt Regency Hotel, Dearborn, Mich., Sept. 15–17.

Essderc 80—1980 European Solid State Device Research Conference, Institute of Physics (47 Belgrave Sq., London SW1X 80X, England), University of York, York, England, Sept. 15–18.

Sixth European Conference on Optical Communication, Institution of Electrical Engineers (1 Savoy Pl., London WC2R 0BL, England), University of York, Yorks., England, Sept. 15–19.

Euromicro 80, Institution of Electrical Engineers (L. R. Thompson, Hawker Siddeley Dynamics, Manor Road, Hatfield, Herts. AL 109 LP, England), Imperial College, London, Sept. 16–18.

FOC 80: Fiber Optics and Communications, Information Gatekeepers Inc. (167 Corey Road, Suite 111, Brookline, Mass. 02146), Hyatt Regency, San Francisco, Sept. 16–18.

Wescon/80, IEEE, Anaheim Convention Center and Disneyland Hotel, Anaheim, Calif., Sept. 16–18.

Eusipco: European Signal Processing Conference, IEEE *et al.*, Swiss Federal Institute of Technology, Lausanne, Switzerland, Sept. 16–19.

ACM Symposium on Small Systems, Association for Computing Machinery (Liza Loop, 3781 Starrking Circle, Palo Alto, Calif. 94306), Hyatt Rickey's, Palo Alto, Calif., Sept. 17–19.

30th Sicob—Salon International de l'Informatique, de la Communication, et de l'Organisation de Bureau, (6 Pl. de Valois, 75001 Paris, France), Init—Paris La Défense, Sept. 17–26.

Circle 27 on reader service card


SERIAL I/O
PARALLEL I/O
iSBX
MATH
iSBC

One Step Beyond the iSBC™ System

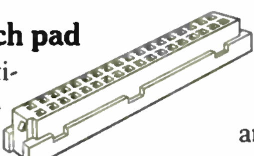
Introducing iSBX™ Multimodule™ boards. A whole new dimension in configuring single board computers.

Intel pioneered the concept of flexible microcomputer *system* design in 1976. That's when we began introducing iSBC™ systems, a family of single board computers. These are expandable via the Multibus™ interface, presently accepted as the industry standard for microcomputers.

Now Intel has extended this well-accepted concept to *board*-level design—with Multimodule™ boards and the iSBX™ bus. With this new line of plug-in modules, you can now expand iSBC systems simply and efficiently at the board level. Without making any demands on the system structure. And all at much lower cost than was previously possible.

Multimodules let you add special performance features today to your iSBC host board—features like high-speed math functions. And serial or parallel I/O. Soon you'll also be able to add Multimodules for D-to-A and A-to-D conversion, communications, and peripheral interfaces—and more. With these modules, you'll be able to precisely tailor hardware configurations to your application, and cut down critical development time.

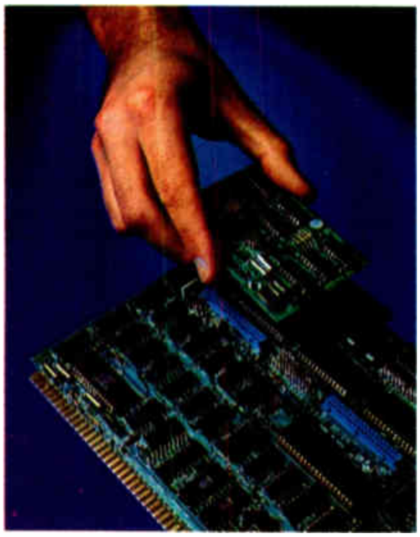
The iSBX™ launch pad



The key to Multimodule flexibility is the iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems. Available on all future Intel single board computers, the iSBX bus assures you of compatibility between iSBCs and the emerging Multimodule product line.

You can also count on improved system performance. Since Multimodules tie directly into the iSBC's internal bus, you get faster, more efficient memory access and I/O operation than is possible with full expansion boards.

For those who want to explore their own expansion module designs, Intel also offers iSBX 960-5™ connectors. These let you create custom Multimodule boards to meet your own unique requirements.



Two new iSBC™ command modules

Intel's new 8-bit iSBC 80/10B™ and iSBC 80/24™ single board computers are just the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved, iSBX-compatible versions of popular single board computers.

Backed by life-support equipment

To support your implementation efforts, Intel provides an extensive set of hardware development tools. Such as the Intellec® system, with ICE™ in-circuit emulation. Or high-level programming languages like PL/M, BASIC, and FORTRAN. And the RMX/80™ real-time software.

A small step for microcomputers

Intel's new iSBX bus and family of Multimodules represent a small step for incremental design of micros. But a giant step toward making you and your iSBC system more productive. Available from Intel today are the first three Multimodules, and our two iSBX-compatible single board computers. The next step is up to you.

For more information, or to order, return this coupon or call your local Intel sales office/distributor. Or contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

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ELEX

Please send information on:

- ☐ iSBX Multimodule package
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BIOMATION K100-D

Compare this general purpose logic analyzer with the currently accepted industry standard.

The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's*. Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

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The K100-D's 1024 word memory is *four times as deep as the 1615A's*. This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

Compare your productivity.

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

Hewlett-Packard 1615A
A very good logic analyzer

Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data, or 24 data

Biomation K100-D
The industry's finest logic analyzer

Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data, or 32 data

GOULD
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Circle 31 on reader service card

Finding tomorrow's engineers today

by Andrew S. Grove, *president and chief operating officer, Intel Corp., Santa Clara, Calif.*

Over the years, the limiting factor in the development of an industrial society usually has been the availability of the skilled people who provide the momentum for progress. Historically, the pace of change has been slow enough so that the training and educational processes of a particular society could respond to the need. In this way, education has become like a free market, with supply responding to the changing demand.

The efficiency of any free market, however, depends on the ease with which information flows so that the news of changing demand reaches the producers of goods. If the information flow is not good, despite their best intentions manufacturers may flood the market with the wrong product and take away the resources for the development of others.

Electronic technology is penetrating our society at an accelerating rate, creating a dramatic change in the supply and demand for technically trained people. The need for the inherent technical capabilities provided by electronics is eminently clear in our society, faced as it is by declining productivity coupled with crippling inflation. It is also clear, however, that for this electronic wave to continue to advance, craftsmen and users (the latter also knowledgeable in the ways of electronics) must be readied in similarly increasing waves. Based on the annual output of electrical engineers in the U. S., this increase clearly is not happening.

Assuming that the number of equipment designs incorporating electronics will increase 30% per year and that the difficulty of implementating these designs will double in the next 10 years (it increased approximately 10 times in the last 5), an estimated 1 million software engineers will be needed in the U. S. alone by 1990 to apply the available technological capabilities. In contrast to this requirement, the National Center for Educational Statistics estimates that the total number of U. S. electrical engineers graduated in 1979 was under 17,000.

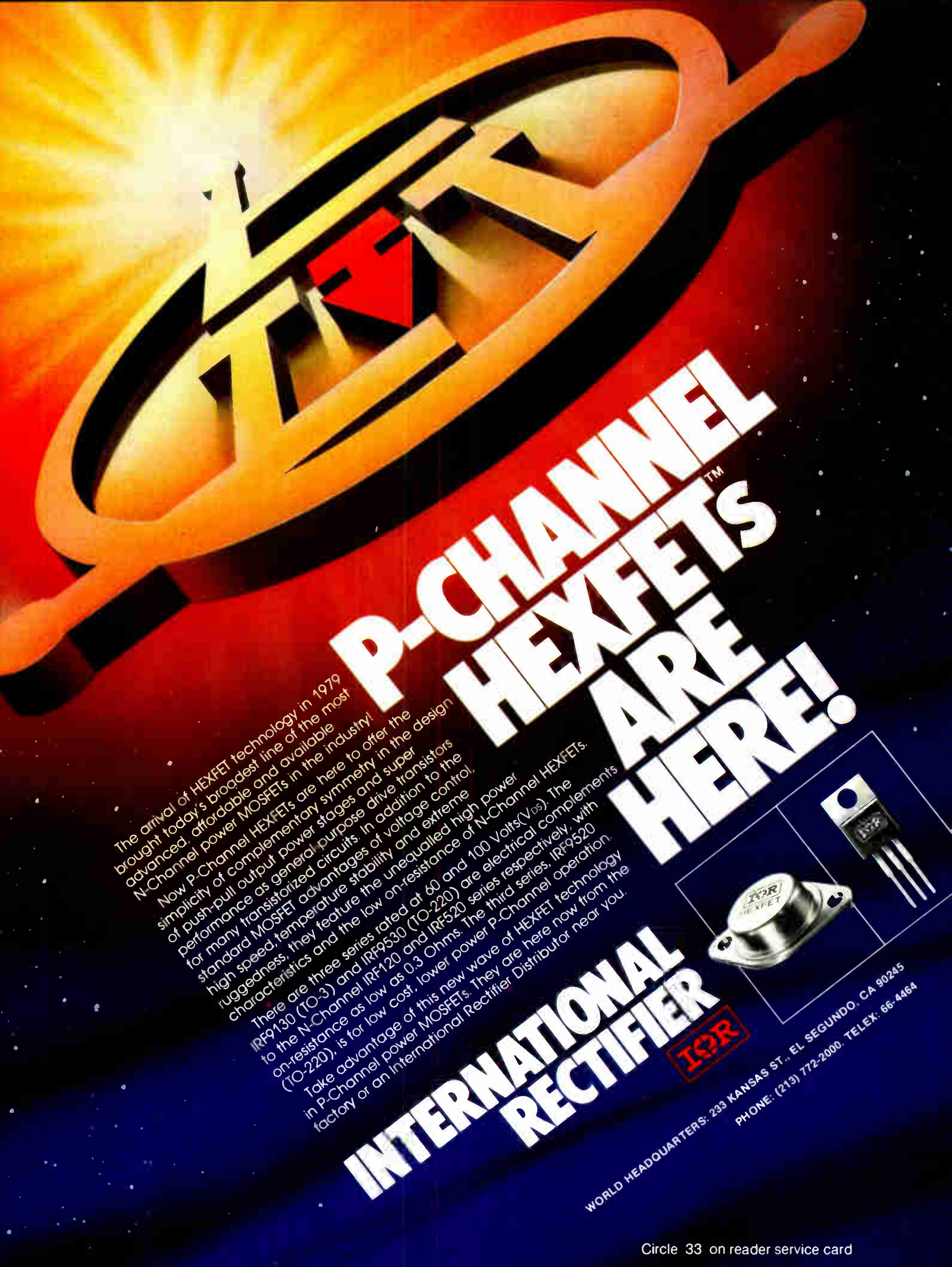
Considering these numbers, I cannot help but wonder how efficient our educational free market really is. As the father of teen-aged children, I have a sense that it is not efficient at all, because in my view the educational system does virtually nothing to convey to this generation of students (my children and their friends) the enormous market for technical talent that will exist throughout their working lives. Our secondary educational system leaves the choice entirely to the students, seemingly oblivious to the fact that without adequate knowledge free choice cannot take place.

To be sure, these children are exposed to computer terminals at school, but in no more enlightening a fashion than they are exposed to them in a supermarket. They are tested—by computer, of course—to match their aptitudes to possible occupations, with extremely superficial results.

So what we have is a distressing combination of two factors: a pace of change that is faster than it has been historically and a free market that is inefficient because information about demand—and especially future demand—does not reach the "producers."

Plaintive comments like this tend to end with a plea for some kind of Government action. I believe, in this case, that a Government program is neither called for nor desirable. No segment of society understands the problem better than we engineers or is better qualified to proselytize for the profession. We are dispersed; we have contacts with schools and, through them, potentially with students all over the country. I think we collectively should undertake to tell our story. There are a lot of us; we can have an almost immediate impact, and in this age of "pyramids," the rapidity with which individuals can start a grass-roots movement has been amply demonstrated.

The goal is clear: it is the continued eminence and leadership of our American technological society. Participation by the best of our young people will determine its long-term viability far more than superficial Government programs that come and go on the tides of politics. The action that is required of us is also clear. We must all begin to do our part to bring the very best into our field.



Circle 33 on reader service card

Inside this general purpose memory is the right mix for any match.

The right mix.

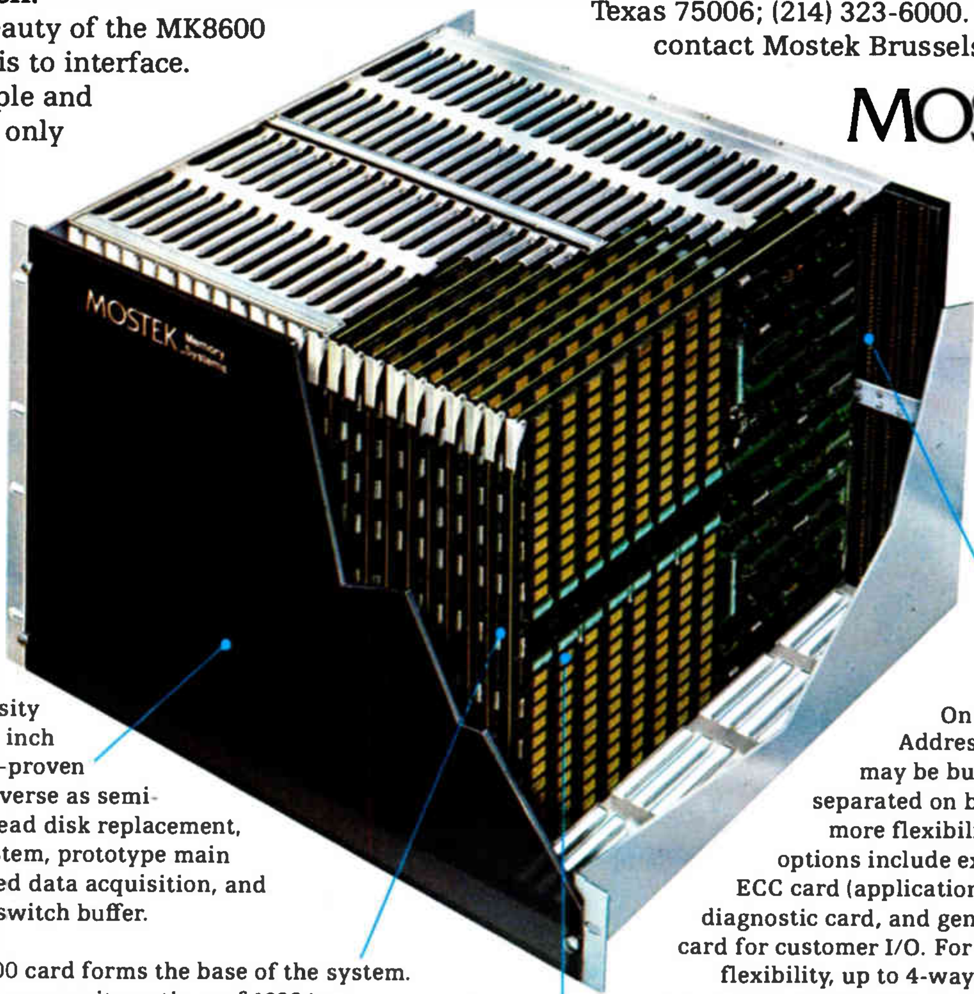
With the MK8600 add-on memory system, you can get up to 6 megabytes capacity in a compact 12¼ inch chassis. Configure it 768K × 72, 2304K × 16 or any other way you want to complement your existing system. It's that versatile.

For any match.

But the real beauty of the MK8600 is how easy it is to interface. The I/O is simple and direct because only minimal control signals are required for any data transfer. This lets you quickly integrate the MK8600 into your system.

Before you specify your next add-on memory system, make sure it has the capacity and interface flexibility to meet your requirements. To be sure, make it the MK8600 add-on memory from Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; (214) 323-6000. In Europe, contact Mostek Brussels 660.69.24.

MOSTEK®



Six megabyte density in a compact 12¼ inch chassis with field-proven applications as diverse as semiconductor fixed head disk replacement, video memory system, prototype main memory, high speed data acquisition, and digital telephone switch buffer.

On the MK8600, Address, DI and DO may be bussed, but are separated on backplane for more flexibility. Available options include extender card, ECC card (application dependent), diagnostic card, and general purpose card for customer I/O. For even greater flexibility, up to 4-way interleaving within a single chassis is also available.

MK8000 card forms the base of the system. Features capacity options of 16384 to 131072 words up to 24 bits in length on a 15.4 × 11.75 inch P.C. card. Complete timing control and addressing logic self-contained on each board. Other features include customer-specified timing options, inverting or non-inverting data, and byte control.

All RAM memory is the industry standard Mostek MK4116 16K dynamic RAM with typical system speed at 250ns access and 450ns cycle time, with faster speeds available for applications requiring high throughput.

Circle 34 on reader service card

Electronics newsletter

Intel shakes up bubble market with price guarantees

In what appears to be an unprecedented action, Intel Magnetics Inc. is guaranteeing prices for future production-quantity purchases of its BPK72 bubble memory kits. These contain the 7110 1-Mb bubble memory module, the 7220 bubble memory controller, and five other large-scale integrated support chips. The guaranteed prices are **$595 each for 5,000-piece orders beginning in July 1981 and $295 each for 25,000-piece purchases starting a year later.** In the interim, the Santa Clara, Calif.–based subsidiary of Intel Corp. is reducing prices of its bubble memory subsystem components and boards by more than 40%. Effective immediately, the 100-piece price of the BPK72 drops 42%, from $1,710 to $995, or 100 millicents per bit. Also, the one-piece price of the firm's iSBC 250 board drops 26%, from $4,750 to $3,500.

New entries in IBM-compatible race from Cambex

The Cambex Corp., formerly Cambridge Memories Inc., is announcing three new mainframe computers in competition with IBM. Software-compatible with the IBM 4300, 370, and 360 series, the Waltham, Mass., firm's Cambex 1600 claims 30% to 35% advantages in price-performance ratio. **The emitter-coupled-logic machines cycle in 50 ns, use up to 144 kilobytes of microcode, and have error-correcting main memories of from 4 to 8 megabytes.** Microprogrammed and bus-oriented, the machines are modular, and according to Cambex executives, they should be almost indefinitely field-upgradable. The Cambex 1636 is said to have about 15% more throughput than an IBM 4331 Group 2, but costs $50,000 less at $125,000. The 1641 claims performance equivalent to IBM's 4341 but costs $75,000 less at $190,000. Both machines can be upgraded—for an added $92,000 for the 1636 or $160,000 for the 1641—to a claimed performance level 50% greater than the IBM 4341, a configuration Cambex calls the 1651.

Raynet system lifts data-handling capability

A new Multibus-compatible multiprocessor is the heart of Raytheon Data Systems Co.'s Phase Two Raynet data-communications system, to be announced this week. **The Norwood, Mass., firm's RDS 7500 outboard communications multiprocessor and its new Preemptive Communications Operating System aim at more reliable and efficient handling of multiple tasks in large, diverse data networks than that offered by the Phase One Raynet.** Raytheon claims that with Raynet Two not only are most mainframes off-loaded from communications processing tasks, but also internodal communications are more rapid than in Raytheon's earlier Raynet systems. Finally, the RDS 7500 PCOS switches operations from one control processor to another in the event of failure so that line concentration, message switching, store-and-forward processing, and other operations can continue uninterrupted. A typical RDS 7500–based Raynet Phase Two system capable of handling 63 high-speed lines would sell for $360,000.

N-channel op amps work from ground

Texas Instruments Inc., Dallas, has modified its Bidfet process—which combines bipolar, double-diffused MOS field-effect, and junction field-effect transistors—to produce n-channel single-supply monolithic J-FET operational amplifiers. Unlike conventional p-channel single-supply J-FET op amps, which can only be powered by 3 V referenced to a negative collector-supply voltage, **the n-channel units can have either side of the**

collector-supply input (+V_{CC} or $-V_{CC}$) referenced directly to ground. Single-, dual-, and four-channel op amps are being offered. The same modified Bidfet process is also being used to make high-speed n-channel J-FET comparators, bi-FET (combining bipolar and FET devices) buffer amplifiers with low power dissipation, and current mirrors. All will be available shortly.

Harris readies 4-K C-MOS PROM using fusible links

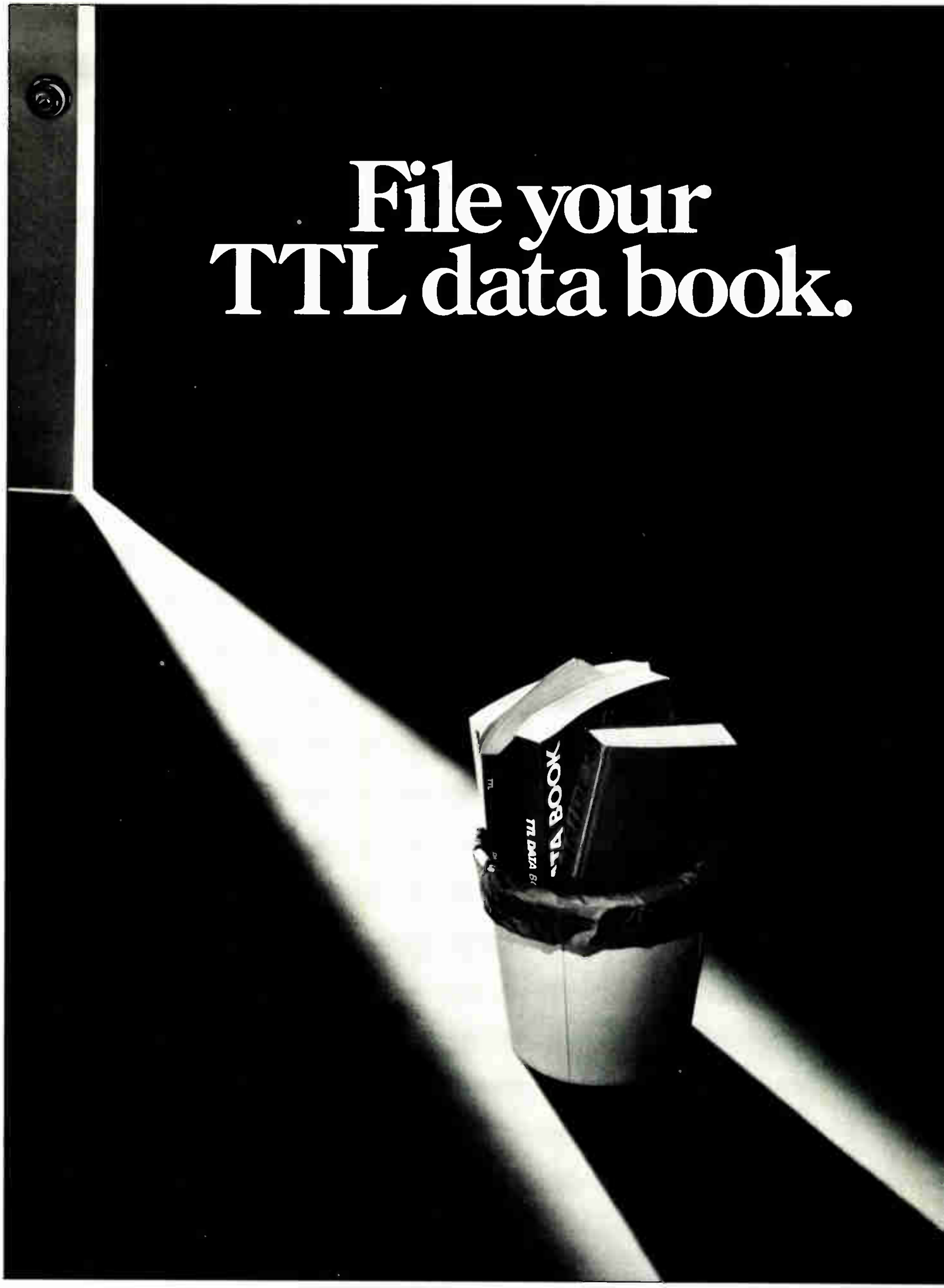
What is said to be the first 4-K complementary-MOS programmable read-only memory using fused-link programming could be in distributors' hands this month. The 6641 from Harris Corp.'s Semiconductor Products division, Melbourne, Fla., **is about 5% larger than 4-K Harris mask-programmable parts, but includes on-chip address latches for microprocessor interfacing.** The 6641's three-state output is TTL-compatible and its power dissipation is typically 5 μW in standby at room temperature or a maximum of 500 mW active at maximum military temperatures.

Wafer processor opts to add gate-array ICs

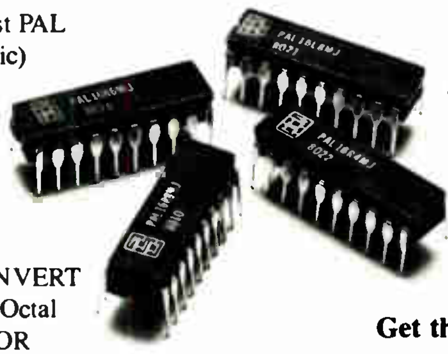
Monosil Inc., Santa Clara, Calif., is entering the market for predesigned gate-array integrated circuits, the first of which will be a family of complementary-MOS metal-gate types ranging from 50 to 550 gates. By year end, **the custom wafer-processing firm hopes to offer an array family using a high-speed C-MOS process.** Its array process will be called Monologic, whereas its predesigned array devices will be labeled Unichips.

Addenda

Semiprocesses Inc., Santa Clara, Calif., which has a second-source agreement for Signetics Corp.'s entire double-diffused MOS (D-MOS) lines, is about to unveil some proprietary D-MOS developments of its own. **Three families of high-power D-MOS field-effect transistors are due**—one, an n-channel type, will feature a breakdown voltage of at least 500 V . . . . **Look for a speedier version of the 1802 8-bit microprocessor from RCA Corp.'s Solid State division in Somerville, N. J.,** sometime in October. The 1802A will operate at 4 MHz, up from about 3.2 MHz. . . . The high-end Eptak programmable controller line from Eagle Signal Industrial Systems division of Gulf & Western Industries Inc., Davenport, Iowa, is about to be upgraded. The Eptak 700 will still rely on an 8080A microprocessor but it will incorporate as standard the heretofore optional arithmetic processing unit built around the Advanced Micro Devices 9511 calculator chip. . . . Technicolor Audio Visual, Costa Mesa, Calif., is marketing a 7-lb battery-powered video cassette recorder and a companion color camera, both made in Japan. **The recorder, priced at $995, is a ¼-inch unit made by Funai Ltd. of Osaka.** The camera, which sells for $950, is supplied by Hitachi Ltd. . . **Qume Corp., San Jose, Calif., will ring out two new printers to supersede its Sprint 3 series.** The company is also understood to be developing a very sophisticated terminal-based printing system that could arrive in the second half of next year. . . Xicor Inc., the firm that made a name with its 5-V-only nonvolatile random-access memories, **is building a fabrication facility in Santa Clara, Calif.,** to produce the parts that Ebauches Electroniques SA of Switzerland has heretofore been making for Xicor. The Sunnyvale, Calif., company intends in addition to fill out its line with 64-by-4-bit devices and 256-by-4-bit devices.


File your
TTL data book.

Four new PAL® devices join the family that's making TTL logic obsolete.



They're here. Our 4 newest PAL (Programmable Array Logic) devices make a total of 13 in the instant custom logic family that replaces up to 90% of the entire 54/74 *S* and *LS* series logic. Meet PAL16L8, an Octal 16 Input AND/OR/INVERT Gate Array, PAL16R8, an Octal 16 Input Registered AND/OR Gate Array, PAL16R6, a Hex 16 Input Registered AND/OR Gate Array, and PAL16R4, a Quad 16 Input Registered AND/OR Gate Array. And soon MMI will introduce two additional PALs with arithmetic functions.

PAL—The Programmable Solution™ —saves you space, time and aggravation.

A single PAL 20 pin SKINNYDIP™ can replace from 4 to 12 TTL devices. But pc board space isn't all you save. Lower system cost, smaller inventory requirements, reduced parts count and high-volume, off-the-shelf, multiple sourced availability,* make PALs the most cost-efficient logic devices on the market. And every PAL can be programmed by any PROM programmer with a PAL personality module.

Get the *right* data book. Free.

For your complimentary copy of the new Bipolar LSI Data Book and further information on the revolutionary PAL logic family, contact your local MMI stocking distributor or sales representative. Monolithic Memories, Inc., 1165 East Arques Avenue, Sunnyvale, California 94086.

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Monolithic Memories MMI

Beat-the-heat hybrids ready to go to market

by Linda Lowe, Boston bureau

Teledyne Philbrick works on materials and structures to push operation above 200°C; other firms also active

The first contenders in a U.S. Department of Energy race to develop very high-temperature data-acquisition and -transmission circuitry for geothermal exploration are beginning to appear commercially with many applications. Teledyne Philbrick is first out of the gate with two hybrid circuits to be introduced at next month's Wescon; close behind are General Electric, with a high-temperature hybrid multiplexer, and Harris Corp.'s Semiconductor Products division, with a complementary-MOS monolithic quad operational amplifier.

Hybrids. Teledyne Philbrick's 2115 voltage regulator has a guaranteed operating temperature of 275°C, and its 4160 analog-to-digital converter is good for 200°C [*Electronics*, July 17, p. 34]. The Dedham, Mass., firm says these hybrid parts are the start of a whole new product range and expects geothermal exploration to be just one of many markets it will address.

So does Harris Semiconductor, also under contract to the DOE's geothermal energy division. "This is an exercise in creating a market," predicts Paul S. Smith, manager of linear products at the Melbourne, Fla., division. He sees great commercial potential in harsh process-control and -monitoring environments, among them nuclear power plants and jet engines.

Harris is developing a C-MOS quad operational amplifier IC for operation at 300°C. It already offers a number of analog circuits that can operate at 200°C.

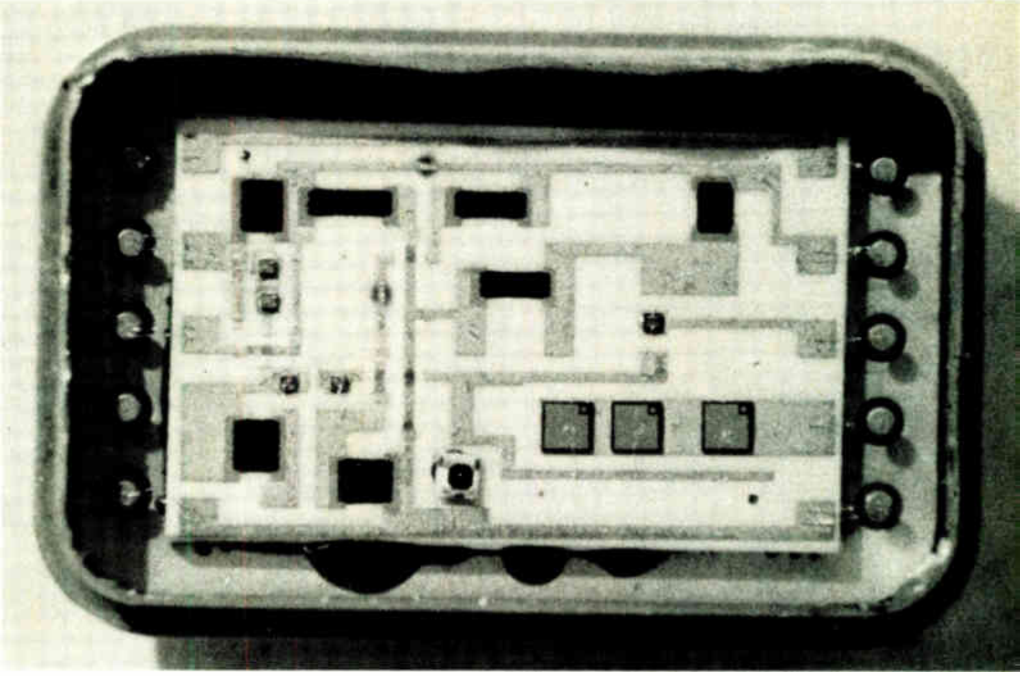
Teledyne Philbrick put much of its development effort into perfecting materials and structures that could take operating temperatures above 200°C, reports production engineering manager Michael G. Reagan. It developed special epoxies and solders that would not fracture or melt and substituted aluminum bonding for gold to ensure that connections would hold despite the heat.

No single vendor's thick-film system was adequate to maintain stability at high temperatures, adds Reagan; much experimentation was needed to come up with a multivendor combination that could do the job. Expensive heat-resistant Pyrolin had to be used for printed-circuit boards to test the parts, since fiberglass would disintegrate and burn.

Multiplexer. In Houston, the technical supply services operation of General Electric's Space Systems division has a high-temperature multiplexer in the works. The company plans to market the part sometime after the conclusion of its DOE contract at the end of this year, according to Marion M. Ringo, manager of design engineering.

Special fabrication and testing will make high-temperature elec-

Tropical hybrid. Teledyne Philbrick's new voltage regulator hybrid has a guaranteed operating temperature of 275°C. Other firms also are working on very high-temperature parts.



tronics "somewhat more expensive than comparable military-grade products," he notes. "But cost will not be the major consideration if components can reliably do jobs that have not been possible before."

At Harris, the biggest problem was the current leakage that occurs in ICs as temperatures rise, causing severe noise and input-offset currents. Up around 300°C, says Smith, "this is enough to render conventional semiconductors useless."

Answers. The engineers compensated by dielectrically isolating each discrete device in a C-MOS semiconductor, eliminating the p^--to-n^- junctions that are the largest source of leakage. Other design techniques include increasing quiescent-current levels to accommodate leakage current and using emitter resistors to stabilize matched pairs in applications like current sources and current sinks. Use of C-MOS parts, Smith adds, ensures that what leakage remains is complementary.

Sandia National Laboratories, the Albuquerque, N. M., research facility managing the high-temperature project for the DOE, is experimenting with other semiconductors. The most promising heat-beaters right now look like gallium arsenide and gallium phosphide, says Anthony F. Veneruso, supervisor of Sandia's Geothermal Technology division. Gallium phosphide parts have been tested successfully at 400°C.

The DOE has set a goal of generating 20,000 megawatts geothermally by the year 2000, compared with 610 MW now. "We're quietly trying to stir up a revolution that will produce the technology we need to advance," Veneruso says.

Communications

Compact ground stations for SBS has gallium arsenide amps, powerful TWTs

With its first communications satellite going aloft, Satellite Business Systems is getting set to put ground stations in place. SBS will take delivery later this month of the first ground stations, from Hughes Aircraft Co. and Nippon Electric Co., with several advanced features over earlier ground terminals, including amplifiers based on gallium-arsenide transistors and powerful new traveling-wave tubes.

Spurring developments is the move of SBS into higher communication frequencies of from 12 to 14 gigahertz (or K band), up from 4 to 6 GHz (C band) where commercial satellites now operate. The higher band takes the first U. S. all-digital satellite communications system away from terrestrial microwave interference, but the penalty comes from attenuation, particularly during bad weather.

Challenge. So the challenge for the terminals, and the satellites, is to boost power to overcome the attenuation, without sacrificing reliability, all at reasonable cost. "We're plowing new ground in commercial earth stations, all right," observes Richard D. Brandes, manager of the Commercial Systems division at Hughes' Space and Communications Group.

K-band. Hughes ground station for Satellite Business Systems' customers comes with a 7.7-meter antenna (shown) or with a 5.5-m antenna for rooftop locations.

The Hughes division and NEC each have contracts for 100 ground stations (and Hughes is building the satellites). Neither of the firms—nor SBS—will talk prices, which may well be at bargain-basement levels in anticipation of orders to come.

One factor in reorders may be the field performance of the two company's products. However, the two types of ground stations share most of the same advanced technological features. One major difference is the higher degree of integration in the Hughes circuitry.

Changes. Chiefly, the improvements are in the low-noise amplifiers, where GaAs field-effect-transistor units replace the conventional parametric amplifiers, and in the development of upgraded 250-watt parallel helix TWTs.

The big edge GaAs FETs offer is price, with performance close to that of parametric amplifiers. They make possible a $2,000 amplifier, compared with the $35,000 parametric amp. The noise figure of about 3 decibels is close enough to the parametric amplifier's 2 dB to guarantee system performance.

The 250-W TWTs combine to provide the required 500 W of radio-frequency output for the modulated signal transmitted to the satellite. If one TWT fails, output is reduced 3 dB, which is still sufficient for uninterrupted operation, says Hughes.

The low-noise amps are in the subsystem that converts the K-band signal down to the intermediate-frequency band; the TWTs convert the i-f into the desired radio frequencies for the transmitter. Antennas come in 5.5- and 7.7-meter sizes, for roof- and ground-mounting, respectively.

Both Hughes and NEC have virtually the same design, including microprocessor-controlled switching to backup modules in case of failure. Prototypes from both firms pass initial tests, says Irving Dostes, SBS director of development engineering. "We think we got super terminals from both," he says.

A major difference is size of terminal electronics, he notes. Hughes' fills two open racks, each 6 by 4 by 3⅓ feet, but NEC's total package volume is some 50% more.

Hughes has a higher level of circuit integration, particularly in frequency converters. Though space is not at a premium in the SBS stations, Hughes believes that squeezing circuitry into smaller integrated designs should improve cost-effectiveness and reliability.

The firm's Commercial Systems division plans to kick off an entire line of ground terminals based on the SBS equipment. So it sees a longer-term advantage in compactness.

So far, SBS has signed up only eight customers for its dedicated service, where terminals will be installed at various facilities throughout the country. Recession effects no doubt are complicating sales of the point-to-point voice, high-speed data, facsimile, and teleconferencing service. **-Larry Waller**

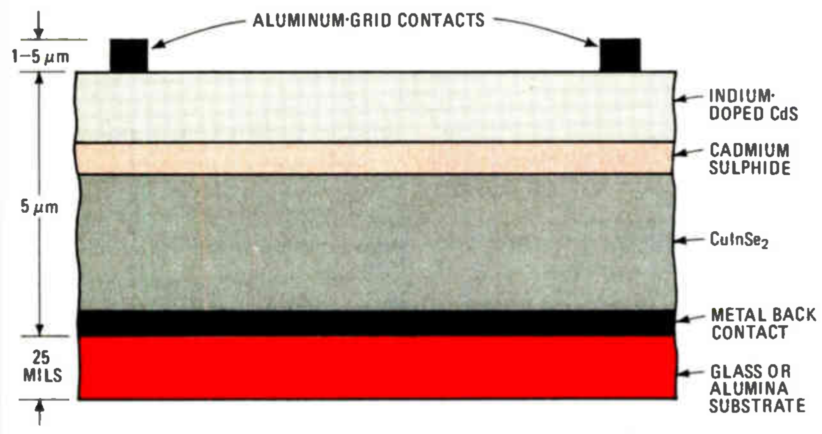
Photovoltaics

Deposition drops cost of thin-film CdS cells

Low-cost thin-film cadmium sulfide solar cells are moving towards commercial realization at Boeing Aerospace Co. Researchers at the Seattle, Wash., company have developed a photovoltaic cell whose junction is manufactured entirely by vacuum deposition and sputtering techniques, omitting the usual chemical bath and thus reducing costs over previous versions.

The cells have reached a 9.4% energy-conversion efficiency. The Solar Energy Research Institute, which is funding Boeing, says that a fully optimized design should top 10%—the 1980 goal set by SERI's parent, the Department of Energy, for thin-film devices.

Cost. Boeing and SERI think the new cell also puts the DOE goal of 15¢ to 50¢ per peak watt in 1990 well within reach. Although single-crystal silicon cells can achieve efficiencies of 16%, they cost about $15 per peak watt—at least so far [*Electronics*, July 19, 1979, p. 105].



Cheaper. Forming layers for Boeing's cadmium suflide cell by using thin-film deposition techniques exclusively reduces materials use and manufacturing costs.

The appeal of thin-film cells is that they are easy to manufacture and use relatively small amounts of material, compared with thick-film cells. As a result, research with thin-film cadmium compounds continues in several areas using zinc, copper, and selenium traces. Boeing's copper indium selenide CdS cell is the most recent addition to this family of thin-film devices.

Both Boeing and SERI are reluctant to discuss the process details until the issue of patents has been settled. However, two critical factors are the ability to use evaporation techniques to build all the layers (see figure) on a low-cost substrate in one diffusion chamber, plus elimination of the difficulties associated with the chemical baths used to lay down the compounds in other forms of CdS solar-cell manufacture.

Long-term stability, a problem for other cadmium sulfide thin-film designs, is within reach, Boeing says. Its design appears to be less prone to oxidation and moisture, problems requiring hermetic sealing of other CdS designs.

For the past three years, Boeing has received about $200,000 annually in SERI contracts for photovoltaics. In the last year, the current cell has undergone efficiency improvements from 6.7% to 9.4%, a figure verified by the National Aeronautics and Space Administration's Lewis Research Center.

Next. For the Boeing researchers, Wen S. Chen and Reid A. Mickelsen, the next step is to optimize the aluminum contact grid lacing the top of the cell. Mickelsen believes that the 8% shadowing caused by the grid can be reduced to 3%.

"The design of the top grid structure is critical," he explains, noting that the aluminum lattice must be sparse enough to pass light to the cell, yet sufficiently low in resistance to serve as an efficient electrode.

Further work is also needed to increase the 1-centimeter-square cell

IEEE funded for photovoltaic standards

The Institute of Electrical and Electronics Engineers has been awarded a $25,000 contract to help establish photovoltaic standards. From the Solar Energy Research Institute, the contract should defray the administrative costs associated with developing the voluntary standards. The work will be undertaken by the IEEE's standards coordinating committee on photovoltaics, directed by David Redfield of the David Sarnoff Research Center, RCA Laboratories, Princeton, N. J. **-Pamela Hamilton** size, perhaps to the 3- and 4-inch diameters of silicon cells—"but not right away," says Richard Burke, a branch chief at SERI's photovoltaic division. "We need to increase the efficiency first and do a cost analysis and see what's involved in scaling up." -Gil Bassak

Peripheral equipment

Membrane keyboards adopt raised keys

Makers of flat-panel keyboards are beginning to reintroduce keys, because they find that the keyless panel that serves so well for hand-held calculator runs into operator resistance in data-entry applications. Thus Oak Technology Inc.'s new FTM (full-travel membrane) keyboard features keys—but the Crystal Lake, Ill., company says it has refined membrane-switch technology for improved reliability and faster, lower-cost production.

As the photograph shows, the FTM offering looks to the user like a keyboard employing capacitive, mechanical, or Hall-effect technology. The membrane is, in effect, a flexible circuit board, and it reduces parts counts, gets rid of costly gold contacts by using carbon-silver conductive inks, and simplifies manufacturing—a plus for fast turnaround on custom keyboards for original-equipment manufacturers.

Automated. "To design a keyboard that we could custom-design and turn around cheaper and faster than anybody else in the industry, we realized we had to go to completely automated manufacturing. And in designing such a keyboard with computer aids, we came up with several technological breakthroughs," says Willis Larson, vice president of product development at Oak.

The breakthroughs Oak claims include the membrane material and conductive inks. Since patents are pending on all of these, Larson would not elaborate. The new membrane, a second cousin of Teflon, will operate over a wider temperature range than the polyester-based membrane used by other companies.

"Since in most cases, keys will be in contact with the membrane, this will give us an edge," Larson says. "The film retains its elastic properties even at high (85°C) temperatures, a capability superior to polyester—100 million cycles per key."

Such a reliability figure, double that claimed for other membrane-based keyboards, approaches the specifications quoted for solid-state Hall-effect switches. With no physical contact necessary, the Hall-effect keyboards offer unquestioned reliability, and OEMs have been willing to pay the price for this.

Oak says it will be delivering large quantities of its FTM keyboards for from $25 to $30 apiece, about half the cost of the Hall-effect keyboards. The Oak price range is similar to that of the Fastype Series 1, a membrane-based full-travel keyboard line recently introduced by Chomerics Inc., the Woburn, Mass., inventor of membrane keyboards [*Electronics*, July 7, 1977, p. 42].

More. Of the Oak entry, Robert A. Rothenberg, president of Chomerics International, says: "This is the second company Chomerics is aware of that has entered the membrane alphanumeric keyboard market [his being the first], and we are reasonably certain that two new companies will soon be entering this same market. The interest of all these other companies only supports our contention that this is the only direction that alphanumeric keyboard design can take."

The response from the Hall-effect people is tight-lipped. Edward C. Leibig, marketing manager for keyboards at the Micro Switch division of Honeywell in Freeport, Ill., says, "We are aware of the Oak full-travel keyboard, and we have no comment at this time." -Ana Bishop

Back to keys. Although membrane-switch technology lends itself to flat keyboards, for data-entry applications, it is being combined with raised keys because users prefer them.

Consumer

CBS stepping out for French teletext

Bypassing the stalled efforts of the Electronic Industries Association's subcommittee on teletext, CBS Inc. has endorsed the French-developed Antiope teletext system as a U.S. standard. The capacity to support future technological growth was the major reason cited by the New York–based owner of CBS-TV in its recommendations to the Federal Communications Commission. Anti-

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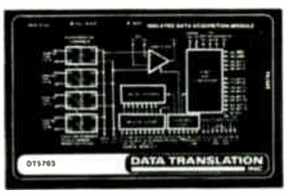

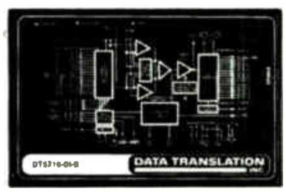

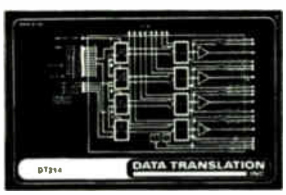

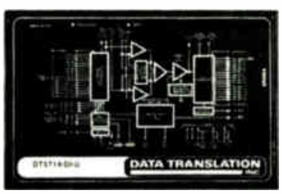

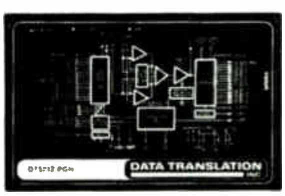

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Free-form. An added feature of the Antiope teletext system is the transmission of free-form graphics, which translates wand's path into the geometric primitives of line and polygon.

ope is flexible and more easily adapted to U. S. TV, according to CBS, which has conducted over-the-air testing of both British and French teletext systems. Field tests at KMOX-TV, St. Louis, Mo., began in March 1979, when the network-owned station exercised the British Ceefax/Oracle and the Antiope systems.

Software. Antiope [*Electronics*, June 19, p. 80] is a software system with its data stream formulated independently of the transmission mode—line-for-line synchronization with the broadcast TV signal is not necessary. So it can more easily accommodate the almost certain changes in technology.

The British systems employ a character-transmission format that is more dependent on hardware, adding to the costs of updating each TV set's decoder. It has similar alphanumeric and graphic capabilities to Antiope's, since both use the same display format and page store.

The software-based French system already can send a wide variety of data. Examples include encrypted messages sent simultaneously and decoded only by the designated recipients and free-form graphics (see photograph).

Also, Antiope is carried via Didon, a packet-based transmission system conforming to the International Standards Organization X.25 protocol for data communications. Thus, CBS argues, Antiope would best meld into existing and developing communications networks.

Each Antiope packet contains 8 service bytes followed by up to 32 bytes of display data. The packet organization is designed to permit transmission at data rates varying from 2 to 4 megabits per second and to permit operation with PAL, Secam, or NTSC TV broadcasting systems. Antiope's packet transmission also can be used for viewdata.

One advantage of a variable format such as Antiope's is that of "parallel" attributes, where character features like color, extended size, and flashing do not occupy any display space. Ceefax and Oracle require serial attributes, transmitted along with the information to be displayed and thus generating blank spaces next to each character.

Hybrid. The British have devised a hybrid teletext format, Polyglot C, which resembles Antiope's variable format, and CBS acknowledges that it could theoretically accommodate changes as the technology develops. However, in the words of Joseph Flaherty, vice president of engineering and development, it sees Polyglot C as "a system of workarounds," which "could pose problems and be more error-prone than the straightforward method."

Telidon, a Canadian teletext system [*Electronics*, April 10, p. 44], has some features in common with Antiope, such as a software-based character format, but it requires more memory and this would be reflected in the cost of the decoder. CBS did not test Telidon because its Canadian promoters did not have equipment available at the time.

All the systems tested by the network are transmitted during the vertical blanking interval of a broadcast signal, a characteristic of teletext. Antiope can also be transmitted continuously on a TV channel, pouring out hundreds of pages of data a second. Viewdata, a two-way, telephone-accessed information system [*Electronics*, July 31, p. 44] was not included in the tests.

Stalled. Although a recent EIA vote suggested that the British system was favored, the traditional 75% majority was not reached. The subcommittee on teletext, composed of TV broadcasters and manufacturers, is stalled, according to observers, because the TV manufacturers are reluctant to add anything that will increase the cost of their product.

The CBS report argues that, even though the Antiope decoder might be a little more expensive at first, it is essential that parallel attributes be available in any teletext system.

The British say the fight is far from over as they believe some U.S. television manufacturers favor their system. Zenith, in fact, has hardware based on British chip designs [*Electronics*, July 3, 1980, p. 59]. British sources dispute CBS's technical arguments in favor of Antiope, stressing that their system's decoder is inherently cheaper and that its heavy error-protection system is better adapted to the noisy broadcast environment.

The network, which first suggested to the EIA that it examine the issue of teletext and come up with a standard, has grown impatient with the committee it helped form, warn-

ing that "adoption of teletext rules and standards is essential at this time." Though CBS intends to participate in future activities of the subcommittee, its director of transmission engineering, Robert O'Connor, has resigned his chairmanship of the EIA unit. -Gil Bassak

Instrumentation

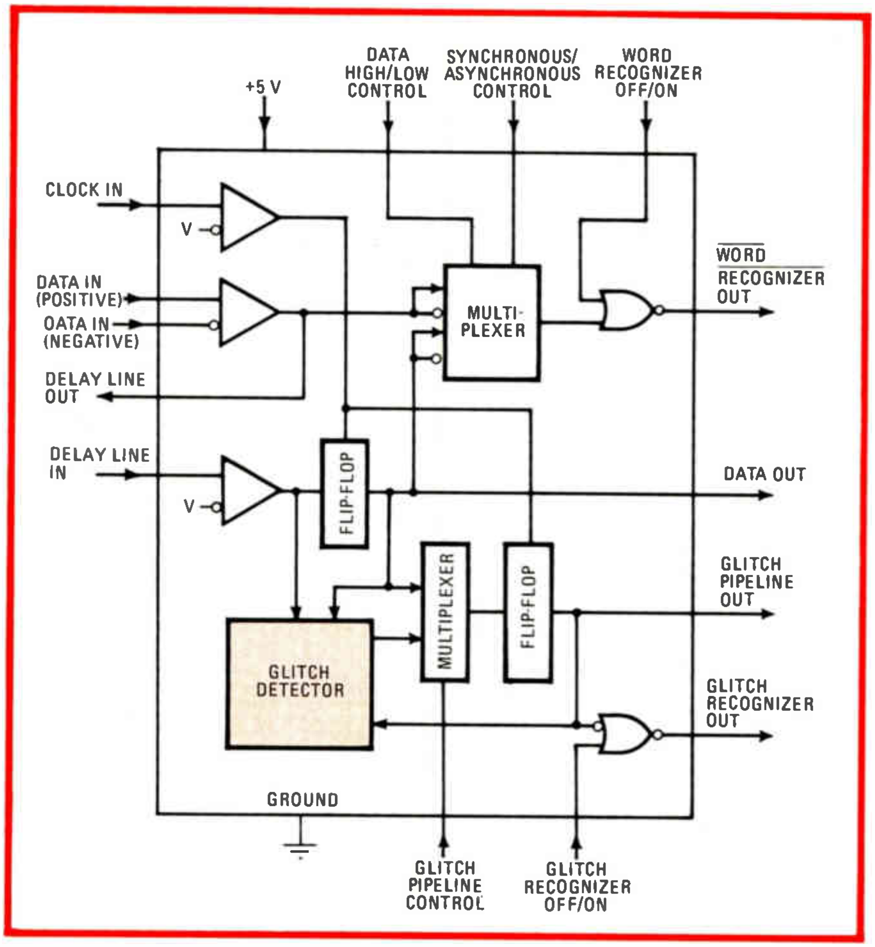
Logic analyzer design is miser on power

Power consumption is a great design headache when updating an existing instrument design especially when the basic mainframe is several years old. Add to that the problem of fitting the plug-in module into limited space, and it's easy to see that Tektronix' logic-analyzer designers faced down some tough problems in their update of the 7000 series.

The new 7D02 module [*Electronics*, July 31, p. 127] is definitely up to date—it can analyze the logic state of 16-bit microprocessors using decoded mnemonics and offers up to 44 channels. Optionally, it also provides asynchronous analysis of eight channels, along with detection of fast waveform glitches.

Providing this capability meant using only the power that the early mainframe could supply. So the designers had to keep a close eye on the power budget, while putting the design on the fewest number of printed-circuit boards.

"It was quite a challenge," says Robin Teitzel, hardware design project manager for the new analyzer module. "We had 49.5 watts to play with and we counted every milliwatt." Keeping power down meant playing a lot of tricks with the standard logic parts used in the state machine to minimize design risk.



Glitch catcher. Replacing eight chips with one, Tektronix' bipolar multilogic IC is the heart of a timing option subsystem in the new 7D02 logic analyzer designed to be power-thrifty.

Building the state machine that way gave the designers the freedom to use custom logic for the timing option chip, which Teitzel describes as "one of the best things we've ever done." The chip is built with the Beaverton, Ore., company's SHF II (super-high-frequency II), a monolithic bipolar fabrication process developed for high speed. Tektronix' latest process, SHF III [*Electronics*, June 21, 1979, p. 131] was still experimental at the time the module design began.

The chip, which uses emitter-coupled, current-mode, and diode-transistor logic, allows the glitch-catching timing option to fit on only two pc boards—one-quarter the space it took up in the earlier 7D01 analyzer module intended for 8-bit machines. Here, too, chip designer Keith Taylor says, "the thing was to get the glitch detection capability into the power constraints of the box."

Detecting. To do that, Taylor came up with new glitch detection schemes and folded what were essentially eight integrated circuits into one. The unit can catch two or more transitions in a short period of time without any dead time for resetting, as in other schemes.

Actually, there are two glitch detectors—one for negative polarity and one for positive—in one. Each time the incoming signal makes a transition from one level to another, a flip-flop is set.

In effect, the flip-flop settings are examined to see whether there are two zero crossings between clock edges. "Really, it's a push-pull scheme. We've filed a patent on it, but it's a little too early to give out too much detail on it," the reticent Taylor explains.

Though most of the remaining design is not patentable, it took a good deal of creative thought. "We did a lot of engineering on the [module's] power supply itself," Teitzel recalls. A switching supply, it is 80% efficient at minimum, and 84% typically—high even for a switcher.

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News briefs

Intel goes lower in development systems
Intel Corp., Santa Clara, Calif., is introducing a low-priced development system for its 8048 and 8080A/8085 microcomputer families, as well as a high-speed emulator for single-chip microcomputers. The new model 120 Intellec series II is a single-package development system with a built-in cathode-ray-tube display and a floppy-diskette drive. With resident software for either microcomputer system, it is priced at $6,990, or at least $4,000 less than other Intellec models. The model 120 can be used with the new 11-megahertz emulator, the HSE-49, that emulates the 8048 and 8049 microcomputers in single-step and real-time modes. Its price is $1,950 with 2 kilobytes of random-access memory.

HP to make floppy disks, tape drives
Hewlett-Packard Co. has formed a new division that will produce floppy-disk memories and subsequently computer tape drives. The Greeley division will initially be at HP's Fort Collins, Colo., site but will eventually occupy a plant near Greeley, Colo. Thomas L. Kelley, manager of peripherals operations at HP's Desktop Computer division in Fort Collins, has been named general manager.

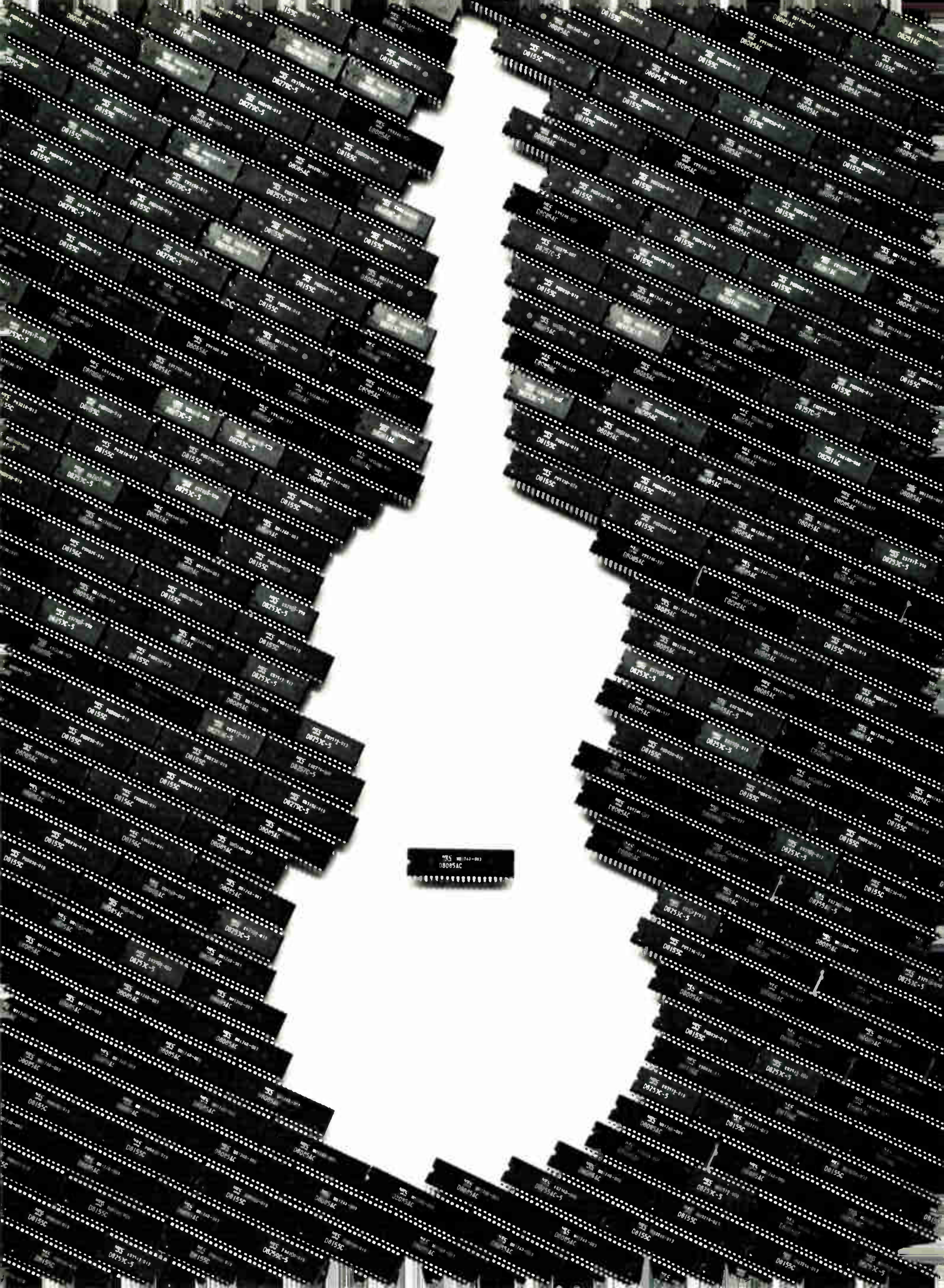
Radio Shack expands its TRS-80 family
Tandy Corp.'s Radio Shack division proved late last month that it has no intention of resting on its laurels as the volume leader in personal computer sales. As expected [*Electronics*, July 31, p. 33], the Fort Worth, Texas, company unveiled three computers aimed at supplementing its TRS-80 family. Two of the three machines come in at the low end. The TRS-80 pocket computer, a hand-held unit that houses 1.9 kilobytes of random-access memory, will sell for $249.95. The TRS-80 color computer, priced at $399, includes 4 kilobytes of main memory and a 53-key alphanumeric keyboard with modulator for use with a standard color or black and white TV receiver. The TRS-80 model III, despite its name, is positioned between the original $499 model I introduced in 1977 and the $3,450-to-$9,000 TRS-80 model II brought out last year. With the same basic architecture as the model I, it is directed toward professional and scientific use and is offered in three versions priced at $699, $999, and $2,495.

GE putting microelectronics center in North Carolina
General Electric Co. is moving technology southward. With a planned initial expenditure of $55 million, the Fairfield, Conn., corporation is setting up a microelectronics center in North Carolina's Research Triangle Park near Durham. Research, development, and production of custom components for many of GE's product lines will be carried out in cooperation with the corporate research and development center in Schenectady, N.Y. The company hopes to have the plant fully operational by early 1982.

certain amount of luck as well as work, the designer notes. Originally the design called for a rod inductor in the supply's output, but it was found that it acted like a broadcast antenna, causing noise to show up on the mainframe's cathode-ray tube. This caused a switch to a toroid, cutting the interference and increasing the power-supply efficiency, thereby providing an extra 100 milliwatts of power.

"We watched a lot of stuff like that and we played a lot of tricks—for example, we don't run the TTL ICs at 5 volts. We run it down a bit, at 4.85 V," Teitzel discloses.

Though the 150 millivolts does not seem like much, the end result is a power saving of 700 milliwatts. Teitzel points out that the savings would actually have been greater if he had used "garden-variety discrete TTL, LS163-type stuff. But I had to do everything with ICs because I didn't have the board space, so it meant that the circuit actually consumed more power." **-Richard Comerford**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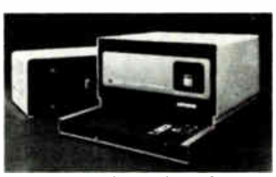

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Washington newsletter

Motorola leads in a-m stereo re-review FCC insiders say . . .

Motorola Inc. is leading its four competitors at the start of the Federal Communications Commission's expected second look at its earlier recommendation that Magnavox Consumer Electronics Co.'s a-m stereo radio broadcast be selected for national use [*Electronics*, July 17, p. 54]. **Also to be reevaluated are the proposals of Belar Electronics Laboratory Inc., Harris Corp., and Kahn Communications Inc.** But FCC insiders say that Motorola's early lead with its entry—called C-QUAM, for compatible quadrature amplitude-modulated signal [*Electronics*, April 14, 1977, p. 82]—could change by the time the commission completes its new comments and reply schedule at the end of the year.

. . . but Magnavox cites system adaptability in drive to hold on

The disappointment of Magnavox in the FCC's decision to take another look at its a-m stereo recommendation was somewhat softened by the commission's refusal to withdraw its initial recommendation of the company's technique until it gets more data. The company is trying to reinforce the original FCC recommendation by reporting that it has successfully converted a Kahn Communications a-m stereo exciter used by broadcasters and produced the Magnavox broadcast signal. Robert Streeter, inventor of the Magnavox system, **made the conversion in "about two hours,"** the company said, "simply by removing 13 components from the printed-circuit boards and adding some jumpers." Indeed, FCC engineers noted that the relatively simple engineering approach used in the design of the Magnavox system "makes conversion of other systems to it quite easy."

Flight simulator market boosted by FAA ruling

The market for advanced flight simulators will get a major boost following a Federal Aviation Administration ruling that airline pilots may now use simulators for increased training, checking, and certification. However, simulator manufacturers will need to upgrade present systems. In the first of the program's three phases, existing simulators may be used for periodic proficiency checks of pilots, copilots, and flight engineers, the FAA says. **The second phase—which will require substantial simulator improvements—will permit additional training to upgrade pilots to larger aircraft.** Simulator improvements required will include programming for crosswind and wind-shear effect, a variety of runway conditions, brake and tire failures, and six-axis motion systems, plus the addition of visual systems to simulate dusk and night scenes. The more complex third phase which will permit simulator use for nearly all pilot training and flight checks, including initial training in new aircraft types, "will require additional development by manufacturers of equipment that can duplicate virtually every aspect of the real world of flight," the FAA says.

Now Mexico heads U. S. color TV import markets

U. S. color TV receiver imports are changing dramatically, with shipments of incomplete units rising and imports of complete receivers declining, according to new Commerce Department figures. **Imports of incomplete receivers—usually lacking only a picture tube—rose 24.8% to more than 750,000 units in the first 1980 quarter from the year before,** while imports of complete units dropped more than 50% to less than 209,000 units. Mexico, which accounted for nearly 60% of the 2.5 million incomplete receivers imported in 1979, registered a first-quarter increase of 11.1% over last year with shipments of 389,000 units, mostly from subsidiaries to their U. S. parent companies.

Automation delays on the D. C. subway

Technology has a bad name among Washingtonians these days. The name is Metro, the multibillion-dollar subway system with its chronically faulty Automatic Fare-Collection System built by Cubic Western Data Corp. In fact, with 60 miles of its 101-mile system operating, the Washington Metropolitan Area Transit Authority is now contemplating scrapping the $51.6 million system and replacing it with more reliable turnstiles and tokens.

Despite recent fixes made to the automatic equipment—originally touted as an improvement on the one developed for San Francisco's Bay Area Rapid Transit—Metro general manager Richard Page leans toward scrapping Cubic's System. But Page also acknowledges that this decision is complicated by the fact that the WMATA board comprises representatives from the three separate government jurisdictions that Metro serves—the District of Columbia and adjoining counties in suburban Maryland and Virginia.

An image problem

Metro's fare-collection system received much attention when Cubic got the contract in 1975. Breakdowns and malfunctions since then have attracted substantially more attention. Local television news programs have competed vigorously for stories on the fare-collection problems. The bad publicity certainly has offset Cubic's corporate image ads touting "technology that makes America a better place to live."

Page's latest financial assessment of the choice between automation and turnstiles got a lot of attention when he declared that the cost of going to turnstiles for the whole 101-mile system would still be cheaper even if AFCS in the existing 60 miles was replaced and the millions already spent were written off. Moreover, annual maintenance costs would be more than halved. A complete AFCS package with improvements, he says, will cost $80.4 million versus $21.4 million for turnstiles with token vendors. Annual AFCS operating costs would be $25.4 million versus $12.1 million for turnstiles.

From where Page sits, the basic issues are "financial and political, not technical." But they are indeed technical for U. S. electronics companies anxious to develop new markets and cultivate their image as makers of quality products. The fundamental issue is one of product design. "Cubic's problem," contends one Metro engineering task force member, "is that it came up with a product that failed to factor the operating environment—the fine dust and dirt that exists in a subway—into its design. These produced most of the breakdowns, and still are producing them desite all the fixes" [*Electronics*, March 27, p. 57]. Others agree.

That design failure, according to one California-based executive who served as an advisor to San Francisco's BART, is a product of American management's failure to assign its best engineering talent to new market areas whose dollar volume and profit margins are uncertain. His contention is that "your best engineers come from the top 10% of any university graduating class. The same numbers apply in industry. And those people get assigned to the big dollar programs with the highest payoff potential."

Cubic rejects those arguments, of course, although it concedes both its failure to recognize that passenger traffic far heavier than original estimates would generate the extra dust and dirt that led to equipment breakdowns and its failure to tell Metro management in 1977 and 1978 to order spare parts for maintenance. Though the company has larger contracts, a Cubic spokesman contends that the Metro system got the attention of the company's top management because the initial 1975 contract award for $54 million was the largest of its kind the firm had ever received. Its complex automatic system represented "state-of-the-art technology in 1975," Cubic says, but notes that the technology "has advanced by leaps and bounds since then"—advances that Cubic says led it to invest an out-of-pocket $5.5 million in changes at one heavily used downtown station to bring hardware to a 99% reliability level. Nevertheless, the damage to the image of good engineering and its potential in an emerging market has already been done.

Demands of new markets

What Metro's problems with Cubic demonstrate is that engineers dealing with a first-time customer for a new application of technology must recognize that the customer often cannot define his own operating environment, much less product performance specifications. And corporate managers must recognize that when they seek to displace old and proven technologies—in this case turnstiles—with something they insist is better, the manager must allocate the company's best engineering talent to the problem at the beginning.

Metro's program to make its new subway system a model for the nation did not seem overly ambitious at the start. Nevertheless, its major technological segment has flopped. And the image of U. S. electrical engineering has suffered as a result. **-Ray Connolly**

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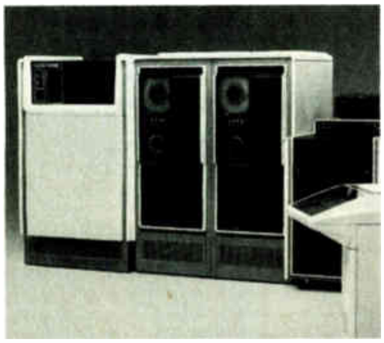

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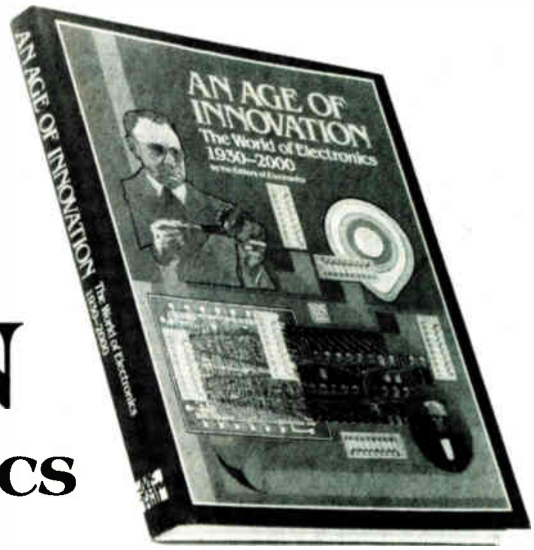
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RCA

Circle 64 on reader service card

International newsletter

Japan hopes to build world's fastest computer

Japan's Ministry of International Trade and Industry may set out to build the world's most powerful scientific computer next year if it can win approval from the Finance Ministry and the Diet. It would be based on either gallium arsenide or Josephson junction devices and have **a speed of several tens to several hundreds of billions of floating-point operations per second.** Thus it would be several tens to several hundreds of times more powerful than the computer the U. S.'s National Aeronautics and Space Association is developing in collaboration with Burroughs and Control Data Corp., which in turn is much more powerful than the CDC Cyber 205 to be completed next year.

The eight-year project would kick off at the beginning of the 1981 fiscal year, which starts on April 1. **Its total budget would be on the order of $88 million to $133 million.** The project would most likely be managed by the ministry's Electrotechnical Laboratory, with much of the work contracted to the nation's mainframe manufacturers in the manner of the last large-scale computer project [*Electronics*, May 24, 1971, p. 41].

Inmos British plant gets go-ahead

After a delay of more than seven months, the British government has given Inmos Ltd. the go-ahead for a UK production unit at a cost of $58 million. It will be located in South Wales close to the Bristol microprocessor design centre, where it will also qualify for both regional aid and European Economic Community grants. The decision follows appraisals by two U. S. consultants who found Inmos well advanced with technically competitive 16-K static and 64-K dynamic memories—under development at its Colorado production unit—while competitors had been slower than projected in entering the market. **Inmos projects sales of $345 million by 1984,** with the British production unit to provide 1,630 jobs by 1985.

Toshiba making CCD filter for deluxe TV sets

Japan's Toshiba Corp. is manufacturing the charge-coupled-device–based comb filter chip with which RCA Corp. vastly improves the picture in its top-of-the-line limited-edition Color Trak TV sets [*Electronics*, Dec. 6, 1979, p. 96]. RCA's own semiconductor plant in Somerville, N. J., will be the second source as soon as it can make the parts, which the company's Princeton laboratory designed around a CCD analog delay line. Now that it can supply RCA's requirements, Toshiba has started a sales campaign among other customers. Therefore probably one or more Japanese companies will be upgrading deluxe TV sets in time for year-end sales by means of the chips—at present around $4.30 each in quantity.

Since its work for RCA is on a custom basis, Toshiba **is saying nothing about the similar but different parts that both companies have undoubtedly developed for video disk players,** in which comb filters are essential to the separation of luminance and chrominance signals.

West Berlin installs fat fiber-optic cable

Standard Elektrik Lorenz AG has installed a fiber-optic cable that the Stuttgart-based ITT subsidiary says is the fattest yet produced. The half-mile-long cable, which is part of a telephone communications network in West Berlin, **consists of no fewer than 320 fibers, each with a 50-μm core and a 125-μm outer diameter.** With a bandwidth of more than 100 MHz, each fiber has enough spare capacity to handle not only phone communications but also video telephone and other broadband services that the West German post office may offer in the future.

International newsletter

West Germany developing digital phone switches

West Germany's post office has given contracts to three communications houses—Siemens AG, Tekade GmbH, and the ITT subsidiary Standard Elektrik Lorenz AG—to develop digital telephone switching systems for a one-year comparative test starting in early 1983. Each firm is to develop **a small and a large system for 1,200 and 4,000 subscribers,** respectively. The results of the test are to show which company's version will be used as a standard for future local exchanges. The introduction of a standard digital system will begin in 1985.

Packet-switching service starts in 7 Japanese cities

Nippon Telegraph and Telephone Public Corp. finally started the packet-switching service of its direct digital exchange service at the end of July with 15 customers. Packet switching is now available in 7 Japanese cities—Tokyo, Yokohama, Nagoya, Osaka, Fukuoka, Sendai, and Sapporo—with the service area **scheduled to be broadened to include altogether 30 to 35 cities by March 1983** and eventually the entire nation.

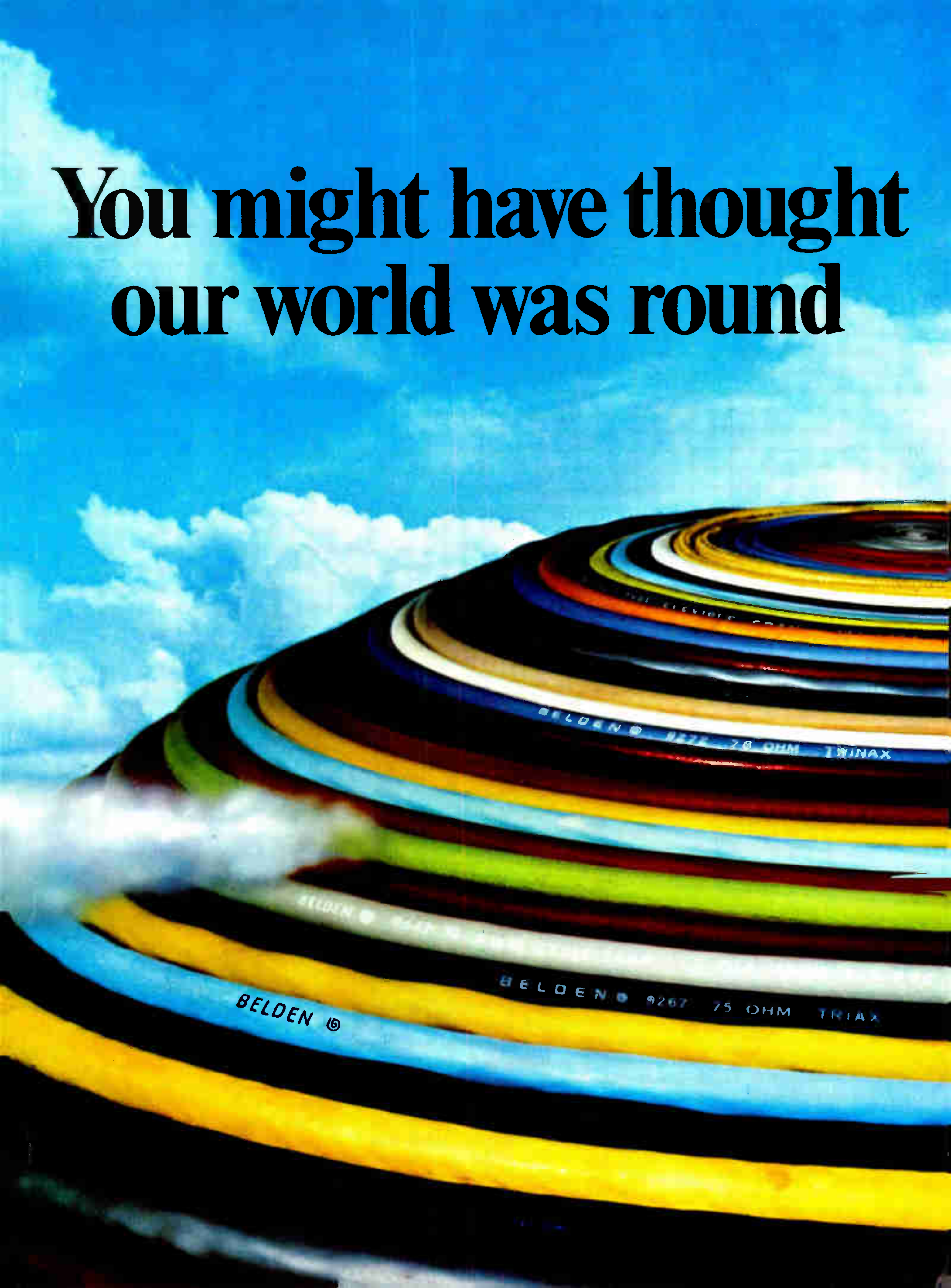
British industry, lobbyists reserved about new citizen's band channel

A discussion paper outlining British government proposals for a new mobile-radio channel received a guarded welcome this week from lobbyists and manufacturers alike, who criticized a suggested operating frequency above 928 MHz—far higher than the 27-MHz frequency currently used in the U. S. The government says that this frequency band, by limiting reception in open country to 10 miles and in cities to less than 3 miles, will minimize disturbance to other services. But potential users will be disappointed by the ranges, and manufacturers argue that **the choice of a virgin frequency band will push the set price up to $700 or more,** depressing the likely market. The government anticipates annual sales of 150,000 of these open-channel sets with an eventual population of 3 million sets. Instead of the suggested frequency, Pye Telecommunications Ltd., the UK's largest mobile-radio manufacturer, would like to see the 200-MHz or 400-MHz band used, so that economies of scale could be achieved by adapting existing mobile-radio equipment.

Speech synthesis hears from Mitsubishi

Mitsubishi Electrical Corp. is now the fourth Japanese company to offer a speech-synthesizer chip set, which it will start shipping in October. It follows Hitachi and Matsushita in using the partial autocorrelation method developed by NTT's Musashino Electrical Communication Laboratory; Sharp has its own scheme. Included in the p-channel MOS set are the M58817P synthesizer and the M58818-XXXP 128-K mask-programmable read-only memory, as well as the M58819S interface chip, which interfaces the synthesizer with standard erasable programmable ROMs for evaluation during system development. Also needed is a controller, which may be any standard 4- or 8-bit microprocessor.

The speech synthesizer can provide either male or female voices and operates at either 1,960 or 3,920 b/s. At the low bit rate, one 128-K ROM can "speak" for 100 seconds, **the maximum of 16 ROMs for 26 minutes.** The synthesizer and ROM chips sell for $6.20 and $7.10 respectively in lots of 10,000; the interface chip costs $17.70 in 1,000 lots.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CIRCLE NUMBER 222 ON THE READER SERVICE CARD.

Direction finder helps ships steer with only ±0.1° error

by John Gosch, Frankfurt bureau manager

Error-compensating design infers bearing from phase angle between signals derived from radiotelephone system

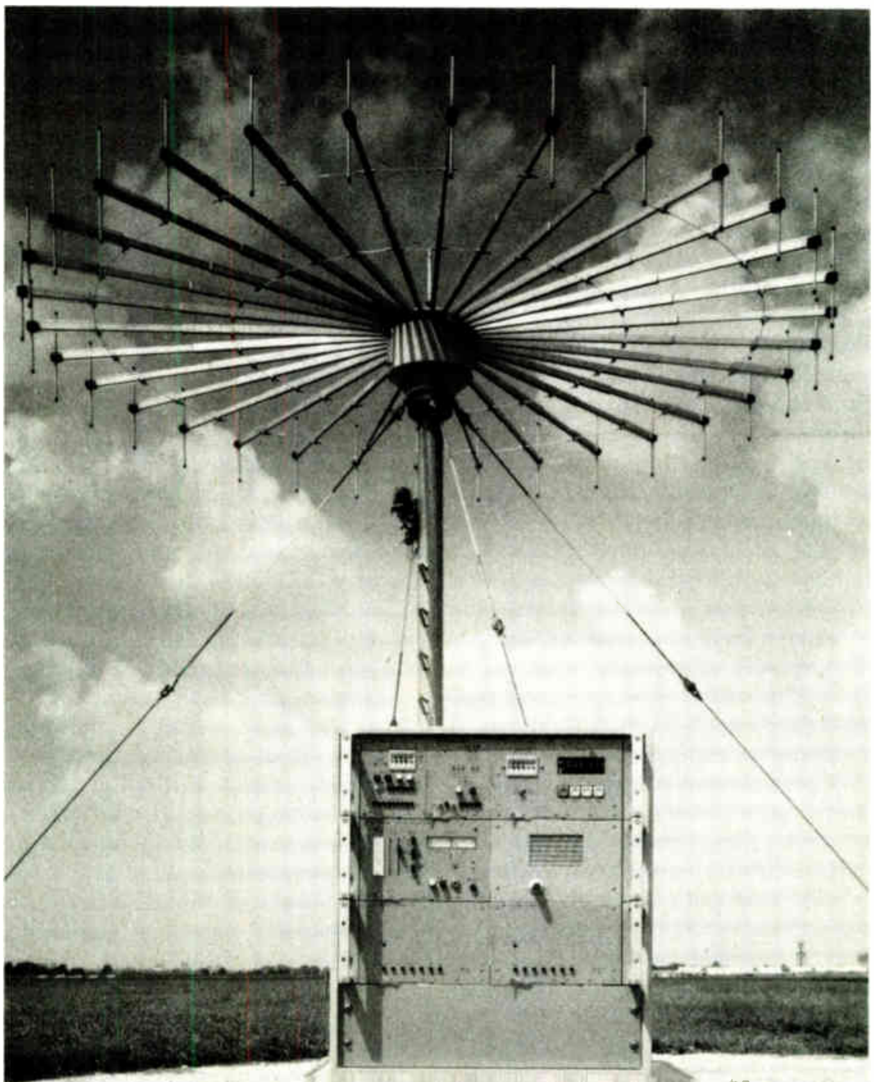
The sun, reflecting surfaces, and the laws of trigonometry gave an ancient Greek a fix on ships approaching the shore. For higher accuracy, however, modern men have turned to electronic direction-finding systems, among the latest of which is the PA 001 from West Germany's Rohde & Schwarz. Intended for maritime applications, it can determine the azimuth, or bearing, to a ship with an accuracy of within ±0.1° [*Electronics*, July 17, p. 67].

The Munich firm's high-precision direction finder (DF), which has just completed tests off Germany's North Sea coast, measures bearings by using the signals from a ship's very high-frequency radiotelephone transmitter. With its antenna installed at a sufficient height and given the system's high DF sensitivity of 10 microvolts/meter, it can determine the bearing of ships as much as 80 kilometers (48 miles) away to within 100 milliseconds.

The requirement. "With our equipment we are not simply aiming to set a new accuracy record but to meet the requirements of the maritime authorities," emphasizes Bernhard Henkel, the chief engineer involved in the PA 001 project. The authorities' concern, he says, is to guide ships safely down the center of an 80-km-long, 300-meter-wide channel cutting through the shoals of Jade Bay and leading to the port of Wilhelmshaven—not an easy task, particularly when wide-bodied, hard-to-maneuver vessels like tankers are involved. It is to be able to tell the pilot exactly how far his ship is off the channel's center line that the authorities are demanding a system accuracy of within ±0.1°.

The system owes that figure principally to a special DF antenna and the use of the phase-delay error-compensation method. As the photograph shows, the antenna has a large number of vertical dipoles—32 in all—arranged along the perimeter of a horizontal circle 6 meters in diameter. To ensure good reception of a ship's vhf signals, the antenna is mounted on a mast typically 70 meters high.

The dipoles are successively



Static rotation. Direction-finding accuracy of within ±0.1° is achieved in part by this 32-dipole antenna; successive cw and ccw scans simulate one moving dipole.

scanned for 10 rotations alternately in the clockwise (cw) and counterclockwise (ccw) directions. Controlling this operation is a signal from a unit at the center of the antenna. This scanning-control unit also supplies a signal that determines at which dipole the scanning direction is to change.

Simulation. The successive scanning of the dipoles simulates, in effect, the rotation of a single dipole. And since the dipole moves away from the vhf source during one half rotation and toward that source during the next half, the received signals are doppler-frequency–modulated. Thus, the antenna delivers an output that is modulated by two doppler-fm signal trains, one resulting from the cw and the other from the ccw rotation. The phase angle between the two signals is a measure of the bearing to the ship.

Contributing the most to the accuracy, Henkel says, is the phase-delay error-compensation technique. In the DF receiver, the two fm signals undergo the same processing steps in their common or separate circuit branches. Any errors caused in these branches by phase-delay variations are the same for both signals. But since they have opposite signs, the errors are completely canceled, or compensated.

Also adding to the accuracy are the antenna's large number of dipoles and the relatively big, 6-meter-diameter antenna base. These factors, Henkel says, make any errors due to dipole design negligible. Any torsional vibrations to which the antenna may be subject during a storm have no effect on system accuracy because their frequency is higher than the bandwidth of the intermediate-frequency DF filters employed in the receiver.

Output. The measured bearing is fed to the receiver's four-digit display. It is also put out in the form of a binary-coded decimal code for digital processing and transmission to other facilities such as monitoring centers. The system, of modular design, can easily be expanded into a larger one with several simultaneously operating DF channels.

The authorities' plans call for completing a network of five PA 001 systems along Jade Bay by 1982. Upon the pilot's request, the ship's position will be determined at a navigation control center in Wilhelmshaven by standard triangulation methods using the results of several bearing measurements. Operators at the center will then phone the pilot to say where the ship is is relation to the channel's center line.

In a second project phase—its completion date is not yet determined—the position of ships will be fixed by cyclic scanning of a vessel's transmitter about every 30 seconds. The result will be radioed to the ship and automatically indicated on a display in the pilot room.

West Germany

$4,000 node interconnects everything from mainframes to microprocessors

A microcomputer-based node costing a mere $4,000 can link any mainframe, mini-, micro-, or personal computer into an extensive data-processing and -communications network. Called Compunet, it is now going to market in Europe and will be available in two to three months from the Redwood, Calif., subsidiary of one of its developers, Kontron Elektronik GmbH.

The unprecedentedly low price, according to Peter Blomeyer, head of Kontron's Microcomputer division, is due both to "a sophisticated software architecture from [codeveloper] Softlab, which requires only a minimum of supporting microcomputer hardware, and our expertise in implementing that hardware at low cost." Softlab GmbH is located in Munich, Kontron just outside in the town of Eching.

Blomeyer notes that the node also reduces peripheral equipment costs, since a single set of peripherals like hard disks and high-speed printers may be accessed by any computer in the network.

Modules. Compunet's software combines a multitask operating system with different modules assigned to the stations connected to the node. It runs on a Zilog Z80A microprocessor with an operating speed of 4 megahertz. Up to 16 kilobytes of read-only memory store the operating system, and 16 kilobytes of random-access memory serve as a data buffer.

As many as 16 stations, consisting of either a computer or another node, can be linked by the node's 16 bidirectional asynchronous or synchronous serial data-communication interfaces. The node routes data from station to station in accordance with messages contained either in the source protocol or in the data in the form of control instructions. In order to ensure flexibility, the node converts all data from the source protocol into an internal protocol and then from the internal into the destination protocol.

Several data streams can be transmitted at the same time, their number being limited only by the protocol being used and the node's maximum transfer speed of 80 kilobits per second. At this speed, the node can handle eight simultaneous 9,600-bit/second streams. Two buffers provide each stream with full-duplex functions.

Among the software modules readied thus far is the BSC, which serves the IBM/370 or Siemens 7000 mainframes and their associated batch processors, such as the IBM 3780 or the Siemens Transdata. Other modules are for interconnecting small computers and peripheral equipment such as consoles and printers.

Numerous uses. Compunet's many possible applications point up both its versatility and its cost-cutting capabilities.

For example, a laboratory employing several microcomputer development systems for the same or differ-

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Q. *Is that so? How does* that *work?*

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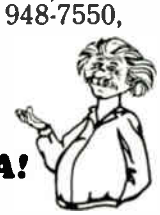

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Circle 73 on reader service card

ent microprocessors can integrate the units into a single universal system by means of just one node. Only one set of peripheral units may then be needed, and the cost of software engineering is greatly reduced, since a hard disk with a centralized program library may be accessed by all development engineers.

Another user might be the organization that has to transfer data between several mainframes at different locations and normally optimizes its use of computing time by equipping each machine with a batch processor. The same function can be supplied by only one Compunet system costing about the same as one or two months' rent for the batch terminals, according to Blomeyer.

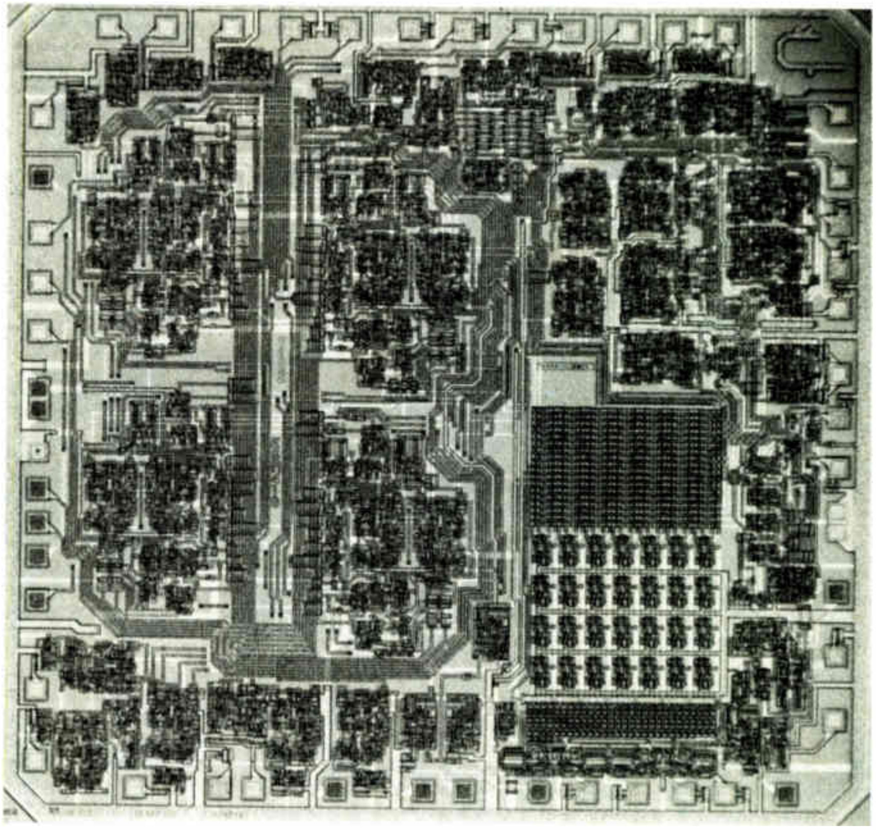
Given such low-priced versatility, Blomeyer is sanguine about Compunet's market potential. For West Germany alone, he pegs sales at well over 100 units during the first year and then an annual doubling of sales for the near term. Compunet comes as a stand-alone unit for mounting in a 19-inch rack—for use as a protocol converter or a concentrator, for instance. It is also available built into Kontron's PS180 personal computer. -J. G.

France

Seven ICs shrink Mirage computer

Ordinarily, a computer built around a bipolar bit-slice processor chip has a lot of TTL packages in its components count. But TTL packages will be noticeable by their relative absence in the airborne computer that the Avionics division of Thomson-CSF has developed for the Dassault-Breguet Mirage 2000, the next-generation French high-performance fighter. Instead, the 2900 family processors on its tightly packed circuit boards will be flanked largely with custom peripheral packages and memory chips.

Given the production rush for military airborne computers, the custom packages, seven in all, will never be best sellers, but they signify a lot to Thomson-CSF's Semiconductor division, which fabricates them. The batch of chips are the beginning of the payoff from a circuit-concept program that the semiconductor people, based in the Paris suburb of Courbevoie, have been working on for some three years.



One of seven. This 30-mm² chip replaces numerous TTL packages formerly needed to control the registers and status bits of a 2900 processor central to an airborne computer.

Efficient. In essence, the program makes it possible for logic designers in Thomson-CSF's equipment-building divisions to lay out large-scale integrated circuits. That frees the Semiconductor division's own circuit designers to work on chips for volume markets—the money spinners.

At the moment, the Courbevoie crew has some 60 basic functional cells—gate arrays, shift registers, bus drivers, and the like—that equipment division computer designers can interconnect on two levels to obtain peripheral chips to go with 2900 family bit slices. (Thomson-CSF fabricates the slices as a second source to Advanced Micro Devices Inc. of Sunnyvale, Calif.). A computer-aided-design program checks the interconnections specified.

Using the library of chips and the CAD backup, the average design time for a custom circuit some 30 square millimeters (46,500 square mils) in area has been cut from well over a year to under a year. "We are aiming to cut that to six months," says Georges Grunberg, deputy director of the Semiconductor division. The technology for the chips is classic low-power Schottky TTL with 5-micrometer design rules and propagation speeds of between 5 and 10 nanoseconds. A 30-mm² chip consumes about 1 watt.

Because the production runs will be small, Thomson-CSF does not plan to put the seven circuits devised for the airborne computer in the catalog. "We would have to price them at something like $200 or $300 each," Grunberg explains. But there is no ironclad policy against selling the chips to outsiders.

The roster of chips for the Mirage

2000 computer lists a 12-bit microsequencer, a status-bit and register controller (see photo), a direct-memory-access chip, a bus interface, a slow-to-fast-bus coupler, a bus controller, and a clock circuit. The first five have been fabricated. The other two should be ready by October. Except for the AMD 2910 sequencer, which AMD put on the market after Thomson-CSF had its own design worked out, there is no counterpart available for any of them, Grunberg believes. **-Arthur Erikson**

Great Britain

ICL chooses international standard as basis for its computer network architecture

Backing its belief that all computers will one day be able to converse freely with each other over open data-communications networks, London-based International Computers Ltd. has adopted the International Standards Organization's packet-switched open systems interconnection (OSI) model as the basis for its computer networking philosophy.

In launching its information-processing architecture, or IPA, ICL is among the last computer companies to announce its strategy for making the data-processing and telecommunications technologies converge, yet it is one of the first to commit itself totally to an international standard as an alternative to IBM Corp.'s proprietary Systems Network Architecture. CII-Honeywell Bull in France, though, is thought to be working in a similar direction.

Goal. IPA will eventually allow a user to connect any computer system through a public packet-switched network—there are plans for 12 national systems in Europe alone—through privately leased lines or local data networks like the Cam-

ICL's first five network facilities

From a user's viewpoint, the benefits that ICL's newly announced information-processing architecture will bring are contained in five new standard software facilities that between them meet most likely applications in a distributed computer network. They are:

- The remote session access (RSA) facility, which enables a user to employ more powerful, central machines to develop programs or financial models or to consult data bases. Since the user normally signs on for a long session, heavy handshaking protocols are employed to establish the "most intimate contact" between terminal users and mainframe.
- The file transport facility (FTF), which permits the transfer of files between machines under operator or program control. Examples include transferring updated prices to local depot machines, central distribution of programs, transmitting central reports out for local printing, collecting daily transactions for local printing or for central analysis, and collecting diagnostic and performance data.
- The distributed applications facility (DAF), which is for use in shops, banks, and other environments employing terminal operators of only limited experience. This facility allows the program itself to enter into a dialog with programs at another site with no need for operator intervention. On submission of a stock enquiry, for example, some items will always be handled locally, others centrally.
- The distributed message router (DMR) facility, which is similar to the DAF but more flexible at routing messages according to source, message type, message content, or user-written program.
- The applications data interchange (ADI) facility, which allows a user to create a dialog between application programs in separate computers. **-K. S.**

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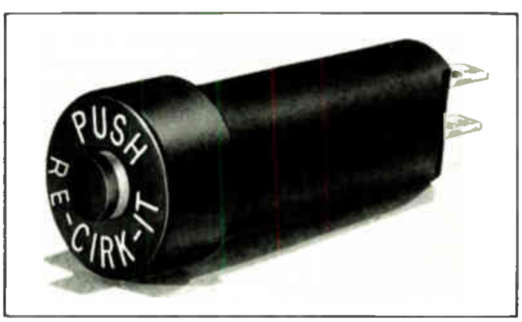

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bridge Ring or Ethernet, using packet-switching protocols and hardware where appropriate. ICL at present is actively considering its choice of local networks.

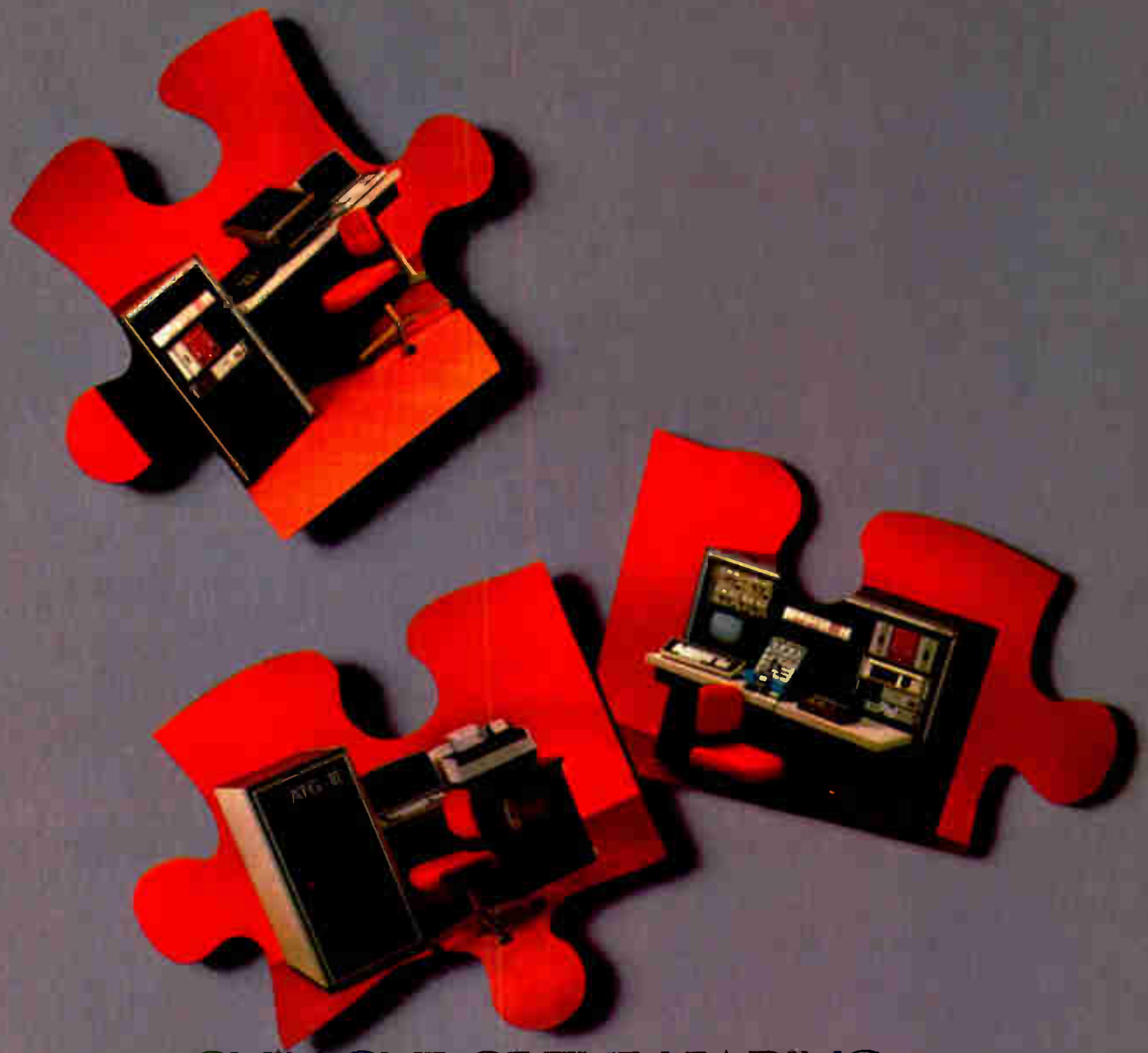
To start with. The company is kicking things off with a package of five software facilities that will support every major type of distributed-processing network in operation today. Together they supply users with the tools for interchanging data records, for accessing nonlocal system services, and for communicating between application programs running in different environments (see "ICL's first five network facilities").

IPA brings other benefits, too. For instance, it is one factor in the improved interactive performance that ICL is currently achieving with its ICL 2900 series mainframes thanks to a considerable reduction in communication code sizes. In simulations on a big 2972 machine owned by the British Gas Corp., the computer handled 1,000 terminals sustaining rates in excess of 10 messages per second, with typical response times of 2 to 3 seconds.

The new network architecture will run on ICL's recently launched ME29 [*Electronics*, April 10, p. 70] using its TME operating system and on the 2900 series using its VME/B and VME/K operating systems. In addition, all future ICL hardware will incorporate IPA facilities where appropriate.

Restructuring. Preparations for the release were laid well in advance and "involved a complete restructuring of our communications software," according to John Chatterton, a marketer who has been deeply involved in the project for the past four years.

"The IPA project group has swept away an accretion of different protocols built up over many years and many company mergers and begun again from the ground up using the OSI standard," he explains. In addition, ICL engineers have contributed extensively to the definition of OSI, gaining much of their experience on the British Post Office's experimental packet-switched network first specified in 1973. **-Kevin Smith**



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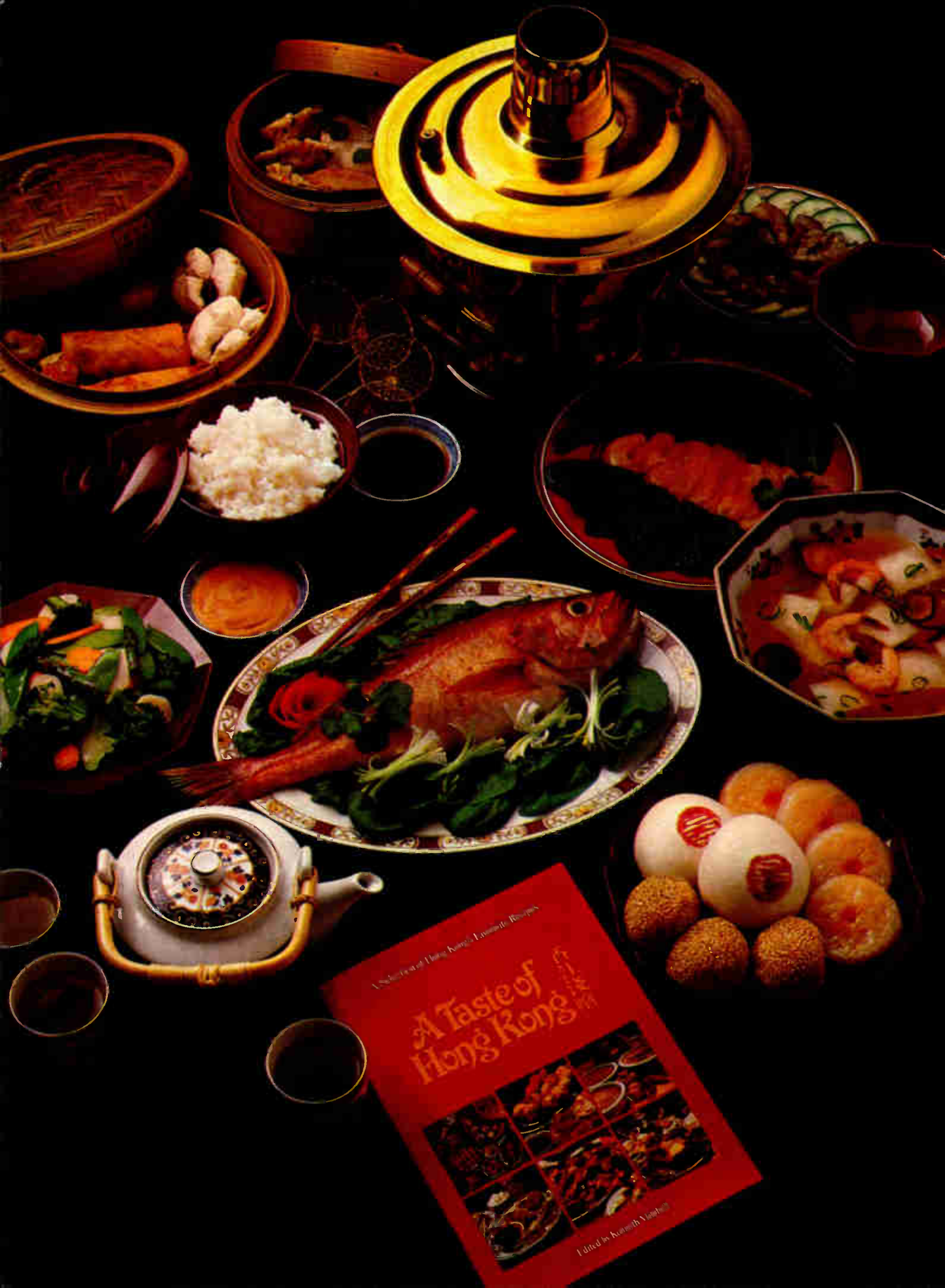
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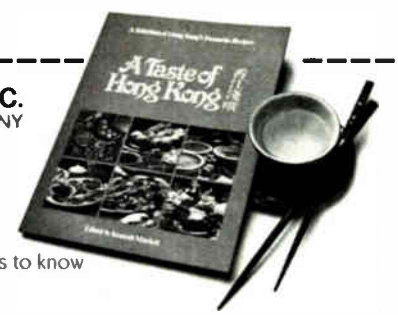

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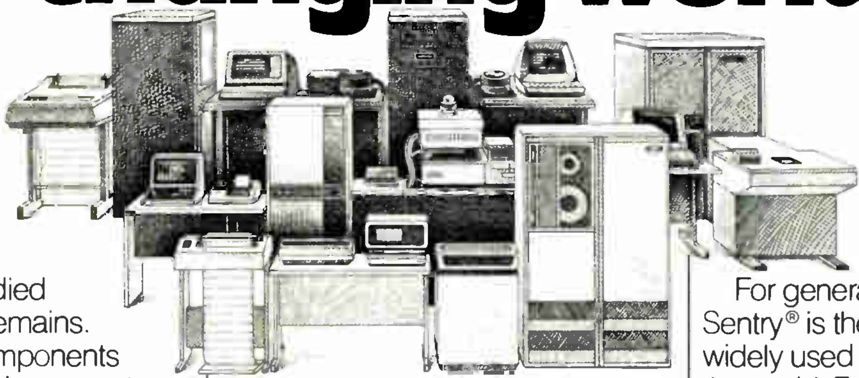

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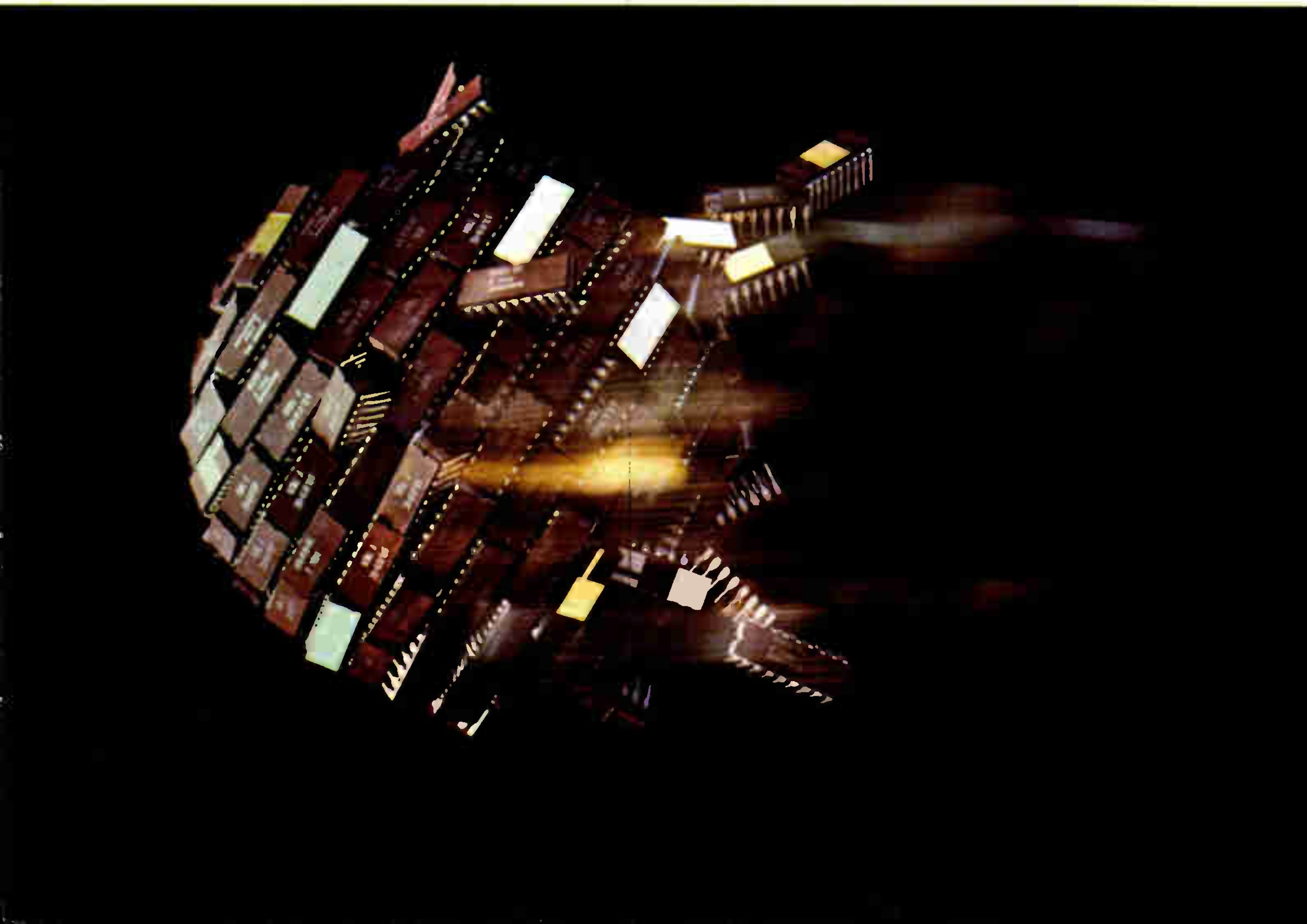

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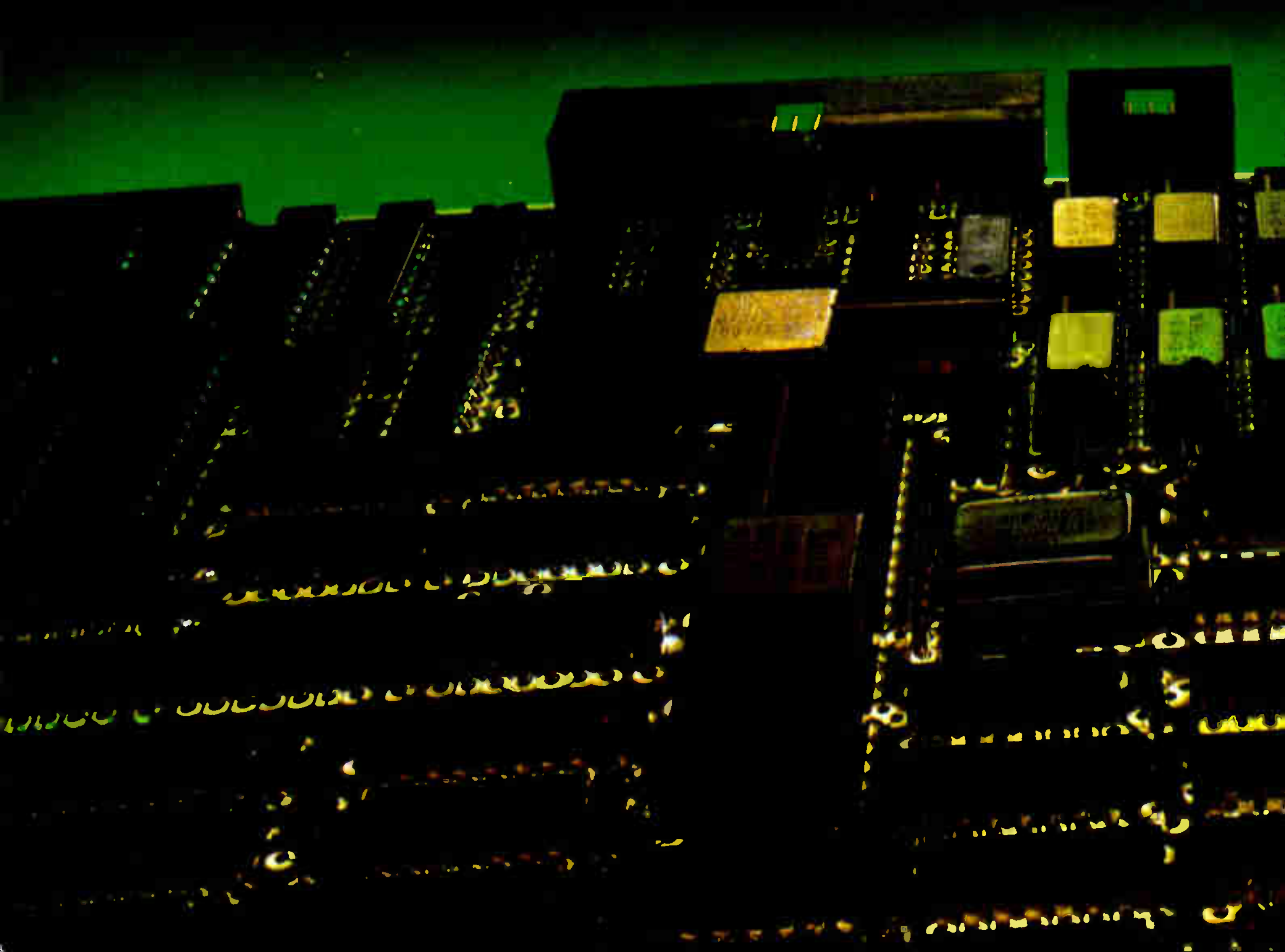

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ECL starts to move

Carried along by computer applications, emitter-coupled logic is now speeding toward growing military and communications uses

by Bruce LeBoss, San Francisco regional bureau manager

Despite the speed offered by emitter-coupled logic (ECL), its performance in the merchant market has been something less than breathtaking. However, things are changing. The few large mainframe computer makers who have driven most, if not all, of the demand for ECL are being joined by numerous others.

As a result of a rapid acceleration in requirements for ECL devices, and the more lucrative sweepstakes to be shared, many semiconductor manufacturers are either revving up their ECL activity or preparing to enter the race.

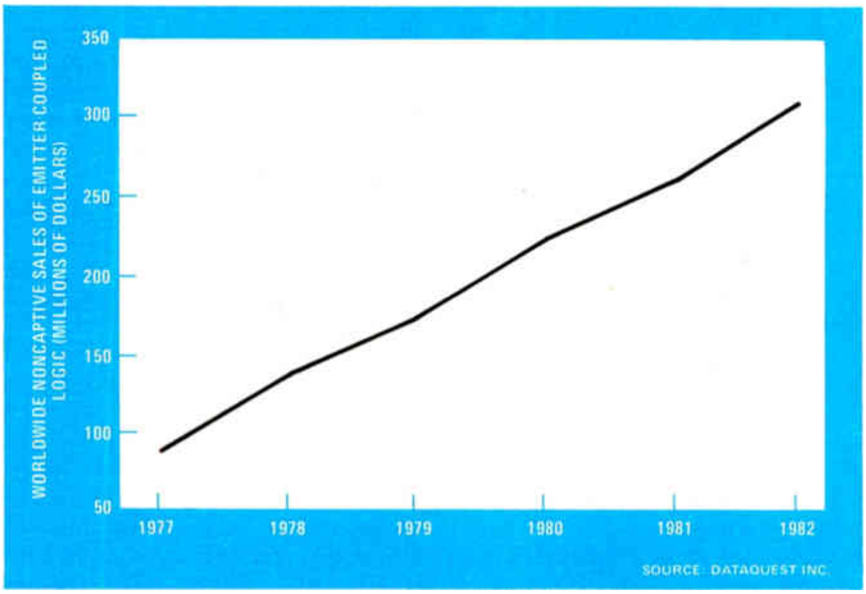
"There was a time when ECL was planned for every single big processing system and some minicomputers, as well," notes Mel H. Eklund, vice president of Integrated Circuit Engineering Corp., Scottsdale, Ariz. That, of course, has not occurred, he states, because "some ECL vendors shied away from the market, reluctant to supply custom parts needed in relatively low volume by few users. Thus there were not many vendors to pick from, and computer manufacturers either forgot about using ECL or built it themselves."

Fragmented. Further slowing ECL's acceptance, Eklund says, was the split in the market by the vendors—specifically, Fairchild Camera and Instrument Corp., with its 100,000 (100K) family of temperature- and voltage-compensated devices, and Motorola Inc., with its uncompensated 10,000 (10K) family. "Market acceptance of ECL would have been much greater had the vendors not split up into two incompatible product camps," he states.

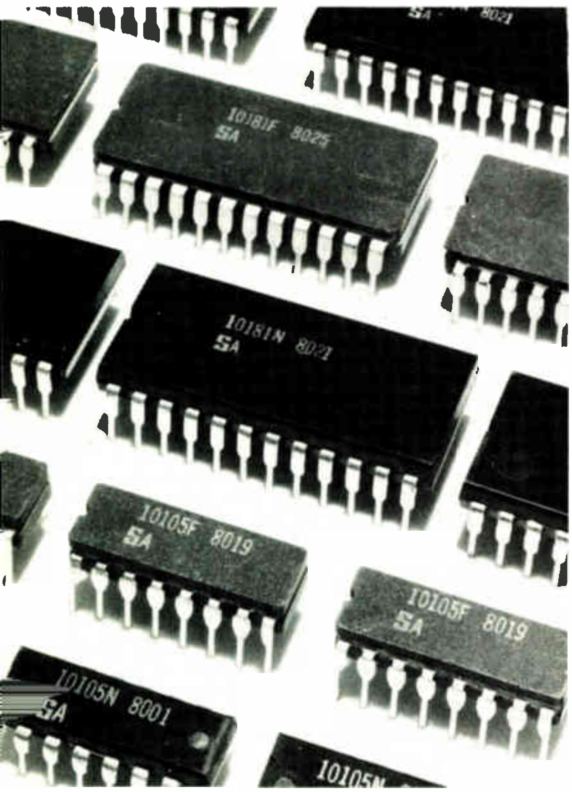
Although ECL accounts for a mere 3% market share of worldwide integrated circuit product sales, according to ICE estimates, the demand and interest in ECL devices is so high that forecasts are for the ECL sector to top the semiconductor industry's rate of growth at least for this year and next. According to Daniel L. Klesken, vice president and director of semiconductor industry service at market researchers Dataquest Inc. of Cupertino, Calif., "The worldwide ECL market will grow in excess of 30% this year, from $175 million in 1979, to $230 million [see chart]."

Computer uses. Much of the activity in ECL is, as before, coming from the large mainframe manufacturers. IBM, for example, is using ECL and closely related current-mode logic (CML) circuits in its 4300 series and System 38 computers and is understood to have designed a CML gate array with upwards of 1,500 gates per device. Other mainframe manufacturers, most notably Amdahl Corp., Burroughs Corp., Honeywell Inc., Control Data Corp., Cray Research Inc., and Sperry Univac division of Sperry Corp. are using ECL and CML circuits in their latest computers [*Electronics*, Oct. 25, 1979, p. 44, and April 24, p. 39].

Many of the computers built around ECL are targeted at the military market, according to John D. Shea, an ICE vice president. "The fast response time and expanded numerical calculation capability that is inherent in high-speed ECL makes it ideal for airborne, as well as shipborne and ground-based support systems," he states. In signal processing applications, for example, ECL "allows a variety of inputs to be taken, and the numbers to be crunched, in



Fast-growing. High-speed circuit applications have made ECL popular with mainframe companies. But sharp growth is expected from additional converts.



Marching along. More semiconductor companies are getting into the ECL race, such as Signetics Corp., which is introducing both 10K and 100K devices (above).

real time so as to make an instant threat analysis and determine what countermeasures or evasive actions to take."

Dataquest's Klesken notes, "Communications people are pushing for ECL, as well. They are talking about 1-gigabit-type logic for switching high-speed data streams."

New contenders. It is not surprising, then, that many semiconductor manufacturers are expanding their ECL efforts or getting right into the action. Signetics Corp.'s logic division in Sunnyvale, Calif., which has been quietly alternate-sourcing a few of Motorola's MECL 10K devices, is now launching a major offensive into the ECL arena. It has just disclosed plans to manufacture more than 80 ECL devices that cover more than 95% of the ECL devices considered industry standards.

According to division marketing manager John Tammel, Signetics not only plans to expand its 10K offering, which includes a number of interface chips, flip-flops, and counters, along with more complex medium-scale ICs, but also will make a move into the smaller race in faster 100K parts by alternate-sourcing a majority of the Fairchild series.

Signetics' 10K devices, because of their 300-megahertz operating speed, typical gate delay of 1.5 nanoseconds, and high noise immunity, are expected to be "widely used in high-speed CPUs, digital communications, computer peripherals, and instrumentation (test systems and counters with ECL prescalers)," Tammel predicts. In the 100K market, which Signetics expects will grow 10 times as fast as the 10K market, the firm will offer parts with a 750-picosecond gate delay and an operating speed in the 400-to-500-MHz range.

Fast race. Not content to sit back and watch Signetics, or any other supplier, win a share of the ECL prize money without a battle, several semiconductor makers are loosening up on the reins. Motorola's bipolar division in Mesa, Ariz., the industry leader with an estimated 30% share of market, is developing a new high-performance family of 10K devices. Dubbed MECL 10KH, they "will offer twice the speed at the same power" of the firm's current 10K family, says Robert Liggett, product planning manager, bipolar digital logic products.

Meanwhile, Motorola also plans to introduce, later this year, a scaled-down version of its ECL macrocell array, which differs from other ECL gate arrays in that it is split into functional blocks, rather than individual gates [*Electronics*, April 10, p. 46].

National Semiconductor Corp., Santa Clara, Calif., signed an agreement with Motorola late last year that will allow National to make and sell bipolar very large-scale integrated circuits derived from the Motorola macrocell array. Pierre Lamond, National's vice president and technical director, says his firm will go into early production on array-derived circuits for its own computer production lines and will also accept orders from external customers for custom circuits using the array concept. National also is understood to be readying an ECL offering of its own design.

Neighboring Advanced Micro Devices Inc. of Sunnyvale, which has been making several bipolar random-access memories with ECL innards and TTL-compatible on the outside, as a spokesman puts it, will put both feet into the ECL market.

AMD's first all-ECL part will be a 1,024-bit RAM that will be offered as both a 10K and 100K device in early 1981. The new ECL devices, the spokesman continues, will be fabricated in AMD's new oxide-isolated process, called IMOX.

More to come. Fairchild is following up its 100K family with its F200 ECL arrays having an equivalent gate complexity of 200 to 250 gates and a typical propagation delay of 750 ps per gate for the higher-power (4-W) version. Power dissipation is in the 2-W range for a soon-to-be-available low-power version, F201, that has gate delays of 1 ns.

More recently, the Mountain View, Calif.-based firm disclosed development of an F300 array that incorporates the latest photolithographic techniques and Isoplanar-S (for scaled) processing to address both the high-speed and the high-density applications simultaneously. Slated to be available in the second quarter of 1981, the F300 has an equivalent complexity of 2,000 gates. Total array power ranges from 8 W down to 2 W, and typical gate propagation delays range from 1.5 ns to as little as 500 ps.

Japanese stables Fujitsu Ltd., Hitachi Ltd., and Nippon Electric Co. also are expected to run for a larger share of the ECL purse. Interestingly, Texas Instruments Inc., Dallas, Texas, is "essentially withdrawing from the ECL race," as a TI spokesman puts it, but threatens to make a comeback with a horse of a different color. "We had one remaining ECL product that we were selling as recently as late 1979. It is a long drawn out process of getting out of the business. Thus, only now are we fulfilling commitments." However, "there are some other (undisclosed) products under development at TI that will fulfill those needs of high-speed computers that are now served by ECL," adds the spokesman, setting the stage for a "dark horse" entry. □

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- New solderless prototyping board which connects to the computer system and allows rapid prototyping of new interface ideas.
- System PROM blaster which accepts 8K through 64K bit industry standard EPROMS and a universal EPROM-ROM card.
- A card edge extender, bus analyzer and bus compatible breadboards.

Documentation

All of Ohio Scientific major circuit boards are now fully documented by Howard Sams (the originator of the Sams Photofact series for Consumer Electronics) servicing manuals which include block diagrams, schematics, detailed pictorials, parts placement diagrams and parts lists providing the designer, systems integrater and serviceman with detailed hardware information. Ohio Scientific is offering qualified OEM users its principal disk operating system (OS-63D V3.2) which supports multiple languages, mini-floppies, 8″ floppies, printers, modems and other accessories in documented Source Code and machine readable form which can be reassembled on standard OSI computers. This gives the product developer the ultimate flexibility in integrating these components into his total system design.

Best of all is the Price

Because of Ohio Scientific's hundreds of thousands of boards per year volume for the consumer and small business market, these products cost a mere fraction of the corresponding LSI-11, SBC or S-100 bus boards. This economy allows you to utilize a floppy subsystem in your product at a total cost typically less than an EPROM based system from other vendors.

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Getting started with the OSI bus architecture is now easy with documentation, off the shelf availability, and economical computer systems for in-house software development using Assembler, BASIC FORTRAN or PASCAL. Ohio Scientific's new OEM contract provides easy to start with terms and generous volume discounts.

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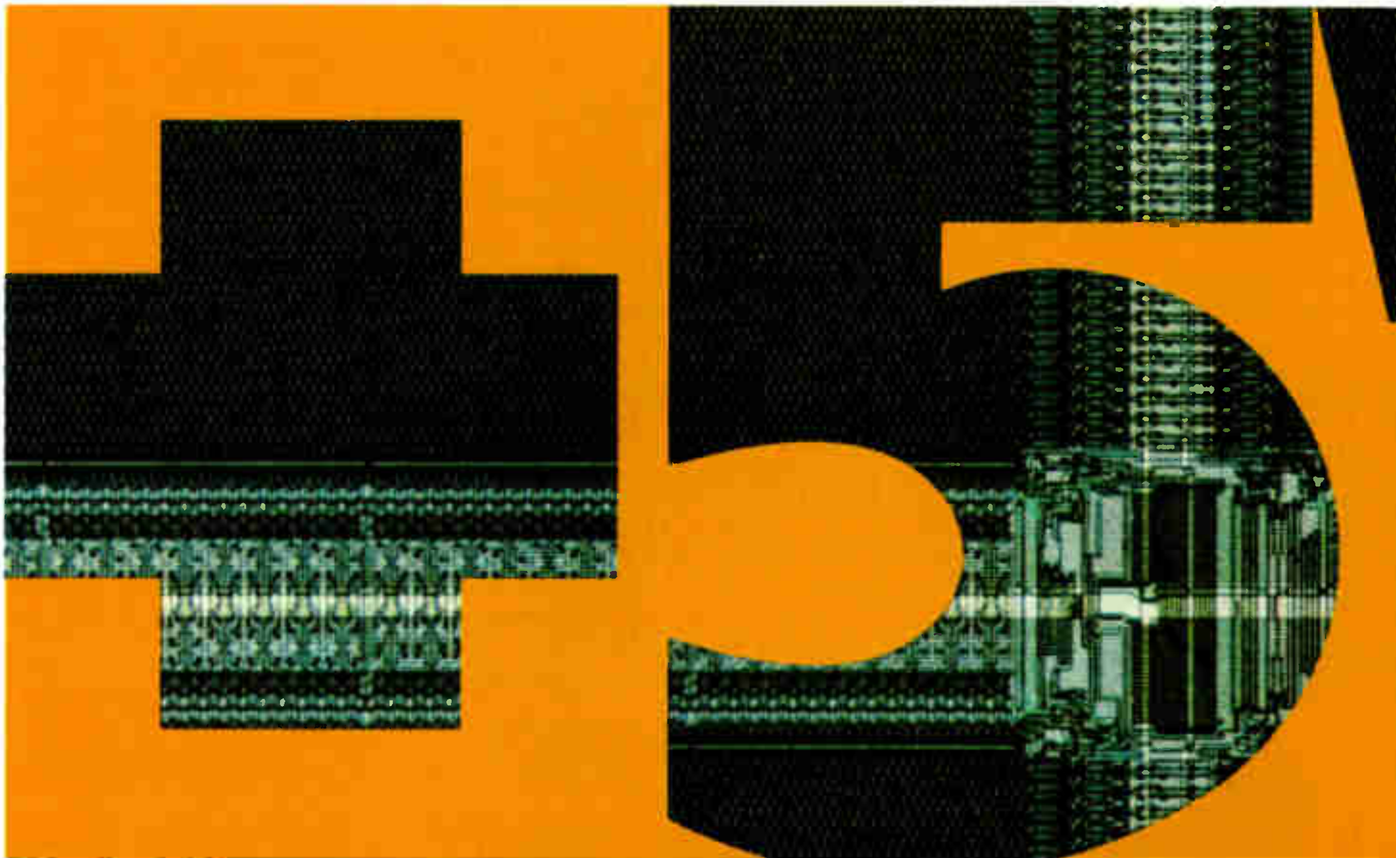

The industry's most complete single +5 V supply dynamic RAM family

Density	Device	Self/Auto Refresh	Power Supply	Access times (ns)
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32K 32K	MCM6632 MCM6633	✓ –	+5 V, ±10%	150, 200
16K 16K	MCM4516 MCM4517	✓ –	+5 V, ±10%	120, 150, 200

V dynamic RAM family today, from Motorola.

V_{CC} Supply Current-Max Active/Standby mA*	Price* 100/pc.
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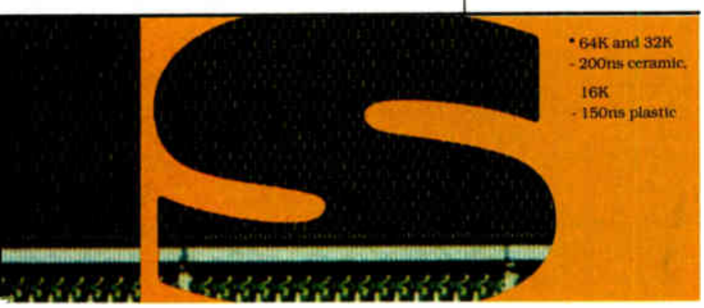

For the first time, a complete family of single-supply +5 V dynamic RAMs from 16K through 64K is available in production quantities. You can get them now, from Motorola.

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The single-supply 16K RAMs also are available now in production quantities from the factory and distributors. Completing this family of totally upward-compatible 16-pin RAMs are the +5 V 32Ks, for intermediate memory system densities between 16K and 64K. They're also available now direct from the factory.

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Motorola's +5 V 64K RAM was the first in volume production. Now, two versions are available. The original MCM6664 has the leadership Pin 1 self-refresh and auto-refresh functions. The MCM6665, without Pin 1 refresh, is now also in volume production.

Our 16K and 32K single-supply dynamic RAMs are designed with and without Pin 1 refresh, too. The 32K MCM6632 (with Pin 1 refresh) and MCM6633 (without) are both in production, as is the 16K MCM4517 (without). The 16K with Pin 1 refresh, MCM4516, will be available later this year.

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Circle 91 on reader service card

Careers

Grad school tackles software

Emphasis at the new Wang Institute is on developing software engineers for industry's needs

by Linda Lowe, Boston bureau

Moving along the halls of a former religious seminary in Massachusetts next month will be students concerned not with the spiritual nature of the life hereafter, but with the development of software for here and now. This new school in Tyngsboro is the Wang Institute of Graduate Studies, an independent, nonprofit institution offering a master's degree in software engineering.

The brainchild of An Wang, chairman and chief executive officer of Wang Laboratories Inc., Lowell, Mass., the institute's dual mission is, first, to prepare software architects and first-line project supervisors to meet the demands of industrial software development and, second, to attract technical people to a region that badly needs them. As such, Wang's new school could become as significant to the industry as any of his hardware.

WIGS, which is about 50 miles northwest of Boston near the New Hampshire state line, should have a significant impact on the region, thinks Howard P. Foley, executive director of the influential Massachusetts High Technology Council. "Massachusetts schools produce too few graduate-level engineers, so in terms of adding to the talent pool, the institute comes as good news indeed," he comments.

Down to earth. Backed by a $3 million endowment from the Wang family, WIGS may reside in a former religious seminary, but it will be no monk's retreat, says Caroline Wardle, the assistant dean. She stresses that the institute's program is a professional one that will specialize in software technology and technical management and emphasize actual

Getting a head start

"Start 'em while they're young" might well be the motto of Project Access, a program to teach high school students programming skills and acquaint them with career opportunities in software engineering. Originally begun as a "general-purpose, philanthropic gesture" by Raytheon Data Systems Co., Project Access has proven so successful that it is now an important part of the company's manpower planning, says its director of human resources, Daniel P. Mulkeen.

Project Access got under way last summer when mathematics teachers from four high schools near the Norwood, Mass., firm attended a six-week, intensive computer-science course at RDS. In particular, they learned to work with RDS equipment and its Macrol language. What they learned became part of the school-year curriculum for 283 high school seniors at the four schools. The company donated and installed equipment for the courses—including RDS 1200 processors, terminals, and printers—as well as additional technical training sessions for the teachers carried on at Raytheon throughout the year.

Last April, RDS recruited two students from each school for part-time co-op jobs at the company. Working about 20 hours a week, the students tackled routine coding projects under the supervision of RDS software engineering managers. "This was a real test balloon," reports Mulkeen. "Coding is generally assigned to new engineering graduates to break them in, and while the work often is below their developing capabilities, we wondered how high school kids could handle the job."

But, Mulkeen adds, the kids did just fine. "The response from our engineering managers was very favorable and very enthusiastic." As a result, RDS now plans to increase the number of co-op students next year to 12 and eventually to include more high schools in the program.

Participating students also have been enthusiastic about Project Access, and some, Mulkeen says, have told him it was the major factor in their decision to pursue an engineering career. He notes that RDS hopes to have some of these students back in summer jobs during their college years. And those who return as graduates familiar with Raytheon and its products can sidestep the training and breaking-in period that is usually required for new engineers.

Another bonus for RDS is that using co-op students to do coding frees up the company's younger engineers to do some higher-level jobs. That, says Mulkeen, alleviates "the boredom factor," which he believes is a common problem in the industry and accounts for the high turnover rate among younger software engineers.

So Project Access promises a means not only of cultivating technical talent in the early stages, but also of allocating existing human resources better, and it looks to be an ongoing investment on the part of RDS, according to Mulkeen. The firm modeled Project Access on a similar program it conducts at the college level. That program, now going into its third year, has produced a number of graduating engineers recruited by RDS for full-time work. -L. L.

work experience in its curriculum.

The influence of industry out in the real world will be felt. For instance, team projects will replace the traditional master's thesis or individual programming assignment and deal with problems "donated" by private companies. Students might work on improving a compiler or on developing new applications software enhancements, and the grades they receive will reflect how well their work meets industry as well as academic standards.

The institute also will use a variety of mid-sized computer systems that graduates will most likely encounter on the job. The WIGS laboratory initially boasts Digital Equipment Corp.'s VAX 11/780, Prime Computer's 750, and Wang's VS systems, plus remote access to an IBM 3033 and a terminal for each student. Working with several different, commonly used systems will make for a breadth of practical experience, Wardle believes.

On its own. The multivendor approach also "assures companies that this will be no mere 'Wang Prep,' but rather an institution serving the whole industry," notes Joseph F. Cashen, engineering vice president of Prime Computer Inc. "That assurance is responsible for the good will and support Wang has elicited from companies like Prime." The Wellesley Hills, Mass., firm donated its 750 system to WIGS and may enroll some of its engineers there this fall, Cashen adds.

The decision to start an independent school rather than give funds to an existing technical school or university reflects a determination to give private industry more say in the content of professional education. "Even specific, industry-funded programs have a way of drifting from the original intent and serving the needs of the university that administers them," comments Jack R. Bohlen, vice president of development for the institute.

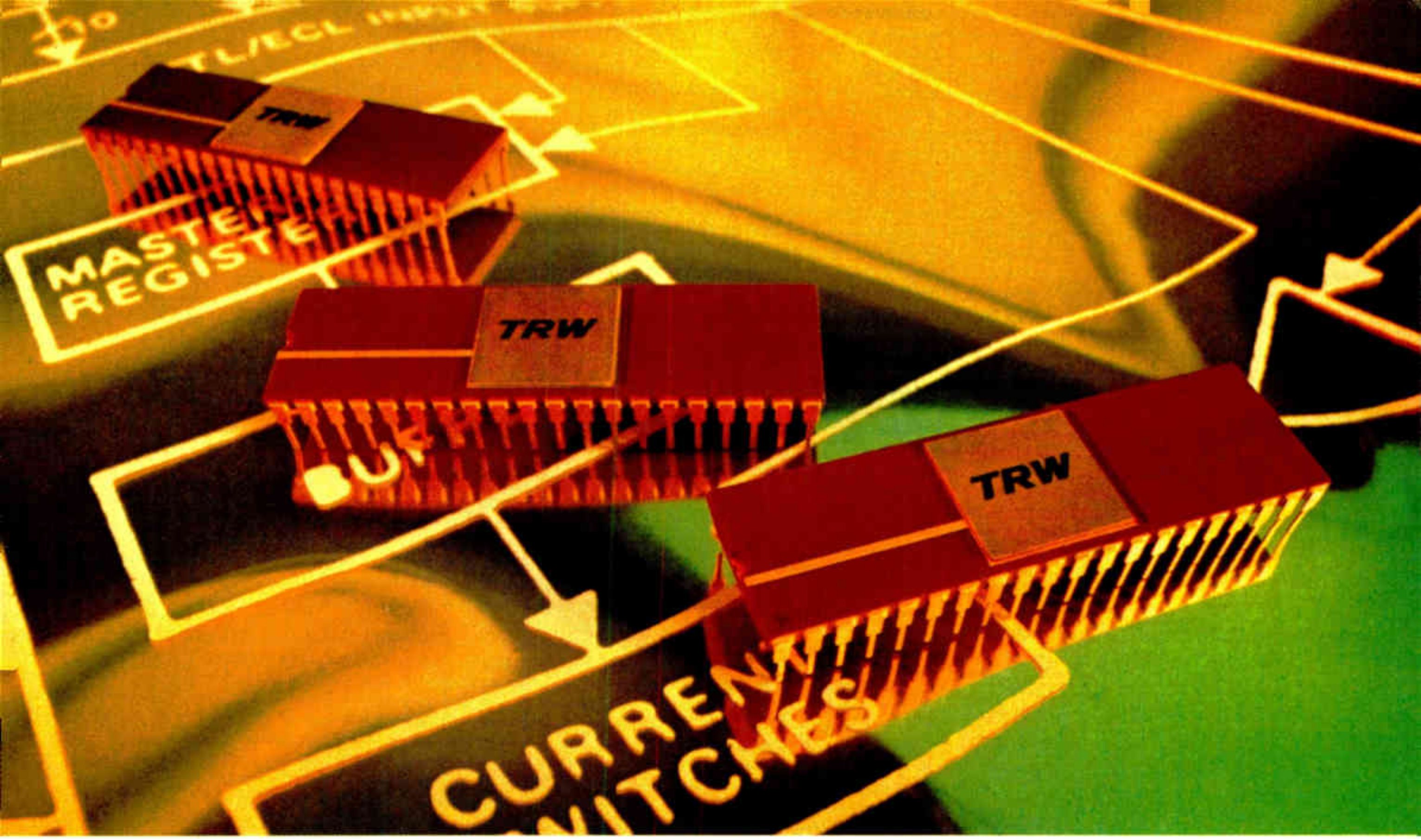
That is just the problem that WIGS will be addressing, says Wardle. Though the institute's two advisory committees include strong academic representation, its training approach will respond to the needs and realities of industry.

The core curriculum will include many courses offered only as electives by most conventional graduate programs, she points out. It will ground students in management skills applying to all phases of designing and running software-development projects, as well as in programming methodology, the application of formal methods, systems architecture, and software engineering techniques. Elective courses will encourage specialization in areas like compilers, operating systems, and data-base management. Common themes running through the course work will include professional standards and ethics, organizational and industry perspectives, and human relations. The goal is to produce graduates ready for industry.

WIGS applicants must have an undergraduate degree in science, mathematics, or a computer-related discipline, plus a minimum of two years' work experience. Full-time students can complete the program in a year, but with tuition costing $5,600 annually and no scholarship plan yet in place, most students probably will take the two-year part-time route to their degree under the sponsorship of the companies employing them. The faculty is headed by Ugo Gagliardi, who is on leave from Harvard University, where he is Gordon McKay professor of the practice of computer engineering. Besides assistant dean Wardle, who is from Boston University, Wang also recruited professors from Michigan State University and the Purdue University.

The first class will probably number some 25 to 30 students, Wardle projects. She hopes to see that number increase to over 100 in three or four years and represent an even split between full- and part-time degree candidates. Comments An Wang: "There is no hurry. We prefer to start small, take our time, and do it right."

His concern is as much for the example WIGS will set as it is for the institute itself. "A lot of people are watching what we do very closely," says Wardle, "and if our experience inspires the creation of similar schools, we'll be very pleased." □



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Solid state

New conference homes in on VLSI

Merging circuit and system design, the first ICCC blankets all aspects of very large-scale integration

by John G. Posa, Solid State Editor

Does the electronics industry need another solid-state technology conference? Some may not think so, but ICCC 80, the first international conference on circuits and computers for large-scale systems, makes a strong argument for itself. It is to be held at the Rye Town Hilton Inn in Port Chester, N. Y., during the first three days in October.

To be situated near IBM Corp.'s East Fishkill facility and its Yorktown Heights Watson Research Center, it is no surprise that the computer giant dominates the program. Indeed, one of the highlights of the conference will be a three-part presentation by IBM on a very large-scale integrated microprocessor.

One of the papers will describe the design of the bipolar gate array used to implement the processor; a second paper will address the architecture of the processor; and the final paper will unveil the automatic placement and routing system and software used to wire the array.

But IBM will not be the only heavyweight on the program. One of the panel discussions, for example, concerns the impact of VLSI on hardware and software in the 1980s. If any group of individuals is prepared to assess the impact of VLSI, it should be these panel members: Gordon Bell of Digital Equipment Corp., Erich Bloch of IBM Corp., Kaneyki Kurokawa of Fujitsu Corp., Bernard List of Texas Instruments Inc., Thomas Longo of Fairchild Camera and Instrument Corp., Joachim Saehn of Siemens AG, Leslie Vadasz of Intel Corp., and John Welty of Motorola Inc.

Merger. ICCC 80 will merge VLSI circuit design with large-scale system design. It is jointly sponsored by the computer society of the Institute of Electrical and Electronics Engineers and its circuits and systems society. In all there will be 58 sessions and 300 papers from all over the world.

The program, listed in the table, blankets all aspects of VLSI, from pure technology to titanic systems. Papers will be given on the prospects

SESSIONS OF THE FIRST INTERNATIONAL CONFERENCE ON CIRCUITS AND COMPUTERS

Day				
Wed., Oct. 1	am	*Session 1:* Memory circuits	*2:* Computer communications	*4:* VLSI placement algorithms
			3: VLSI logic design	*5:* Design automation
	pm	*12:* VLSI logic arrays	*13:* Large VLSI systems	*15:* Systems routing algorithms
			14: Distributed processing	*16:* C-MOS/SOS computers
Thur., Oct. 2	am	*21:* VLSI technologies	*22:* VLSI architectures	*23:* VLSI design aids
				24: Lithography
	pm	*31:* Bipolar VLSI microprocessor	*33:* Fault-tolerant computing	*35:* Fault detection I
		32: VLSI circuit design	*34:* Multiprocessor systems	*36:* VLSI layout
Fri., Oct. 3	am	*42:* Analog circuit techniques	*44:* Software/hardware systems	*45:* Test generation and evaluation
		43: Josephson technology I		*46:* Design verification and simulation
	pm	*51:* Josephson technology II	*53:* Logic and arithmetic unit design	*54:* Computer packaging and interconnection
		52: LSI applications		*55:* Fault detection II

for integrated injection logic, on scaling MOS devices for VLSI (by Intel Corp.), the potential of bipolar devices in LSI gigabit-per-second logic, and the design of LSI analog circuits. The present and future problems of X-ray lithography will be reviewed, as will software for electron-beam VLSI lithography.

Mitsubishi Electric Corp. will outline the boons of the high-pressure oxidation process that has already improved the refresh characteristics of its 64-K random-access memory. IBM will consider MOS devices and integrated circuits at liquid nitrogen temperatures and, in another paper, it will impart yield studies for VLSI chips with projections out to the year 1990.

Josephson too. IBM will also disclose much about its Josephson-junction technology, with its Watson Research Center furnishing three papers. One will present a new ultra-high-speed latching memory element having a 3.5-nanosecond cycle time. A second paper on Josephson LSI circuits will introduce programmable logic arrays and functional-loop logic built with the junctions; the loop logic deals with optimization of complex logic blocks.

The third paper from Yorktown Heights shows off an integrated Josephson system that includes all of the necessary elements to power latching Josephson logic. Speaking of speed, Richard Eden and his collegues at Rockwell International Corp.'s Electronics Research Center in Thousand Oaks, Calif., are forging ahead with super-fast LSI gallium arsenide circuits. They will demonstrate fast, low-power GaAs ICs having gate counts up to 560.

In Session 1, on memories, V. L. Rideout of IBM will present a paper on future directions of MOS RAMs and K. W. Hoffmann of Siemens AG will suggest present and future trends of dynamic MOS memories in general. Siemens will also give a paper on two fast bipolar RAMs and another on a 256-K RAM with selectable operating conditions.

The sessions on logic and processing elements stress the large-scale difficulties of VLSI. As in the user community, a shift in focus from hardware to software is also being embraced by chip designers. Semicustom logic in the form of gate arrays is being tried in lieu of costly custom chips. These arrays are personalized through final mask patterning.

Software. ICCC 80 has scheduled a wealth of talks that concern automatic placement and wiring of such arrays. RCA Corp., for instance, will deliver a series of papers on silicon-on-sapphire technology: one will illustrate the first complementary-MOS SOS gate array to have interconnections routed entirely through automatic algorithms.

In addition to IBM's VLSI microprocessor, TRW Inc. and Amdahl Corp. will also describe VLSI computer architectures. Siemens AG will disclose a fascinating method for testing microprocessor chips using an electron beam. With a scanning electron microscope in the voltage-contrast mode, Siemens is able to record micrographs of logical states and sequences using an 8085 microprocessor as a specimen.

Networking, multiprocessing, and communications will also be given equal time. Mitre Corp., Bedford, Mass., will show how throughput can be improved in packet-switching networks. Fiber optic communications will be the subject of a Bell Labs paper. Another delivery will suggest the use of electric power distribution lines as a communications network. And Nippon Telegraph and Telephone will reveal new C-MOS digital communications chips. □

6: Numerical algorithms	*8:* Panel on large-scale systems	*10:* Large-scale systems
7: Large system decomposition	*9:* Network flow problems	*11:* Linear systems and fast computation
17: Latency and macromodeling	*18:* Large computers and queuing networks	*20:* Dynamical systems
	19: Telecommunications systems	
25: Computer-aided design	*27:* Approached to VLSI design	*29:* Large dynamical systems
26: CAD in Europe I	*28:* Graph theory for large systems	*30:* VLSI panel discussion
37: Panel on VLSI circuit optimization	*39:* Graph theory and combinatorial networks	*40:* Network design and reliability
38: Nonlinear circuits		*41:* Steady-state CAD
47: Numerical device modeling	*49:* Large-scale transportation and communication networks	*50:* CAD for VLSI circuits
48: Large-scale computation		
56: Circuit optimization	*58:* Digital signal processing	
57: CAD in Europe II		

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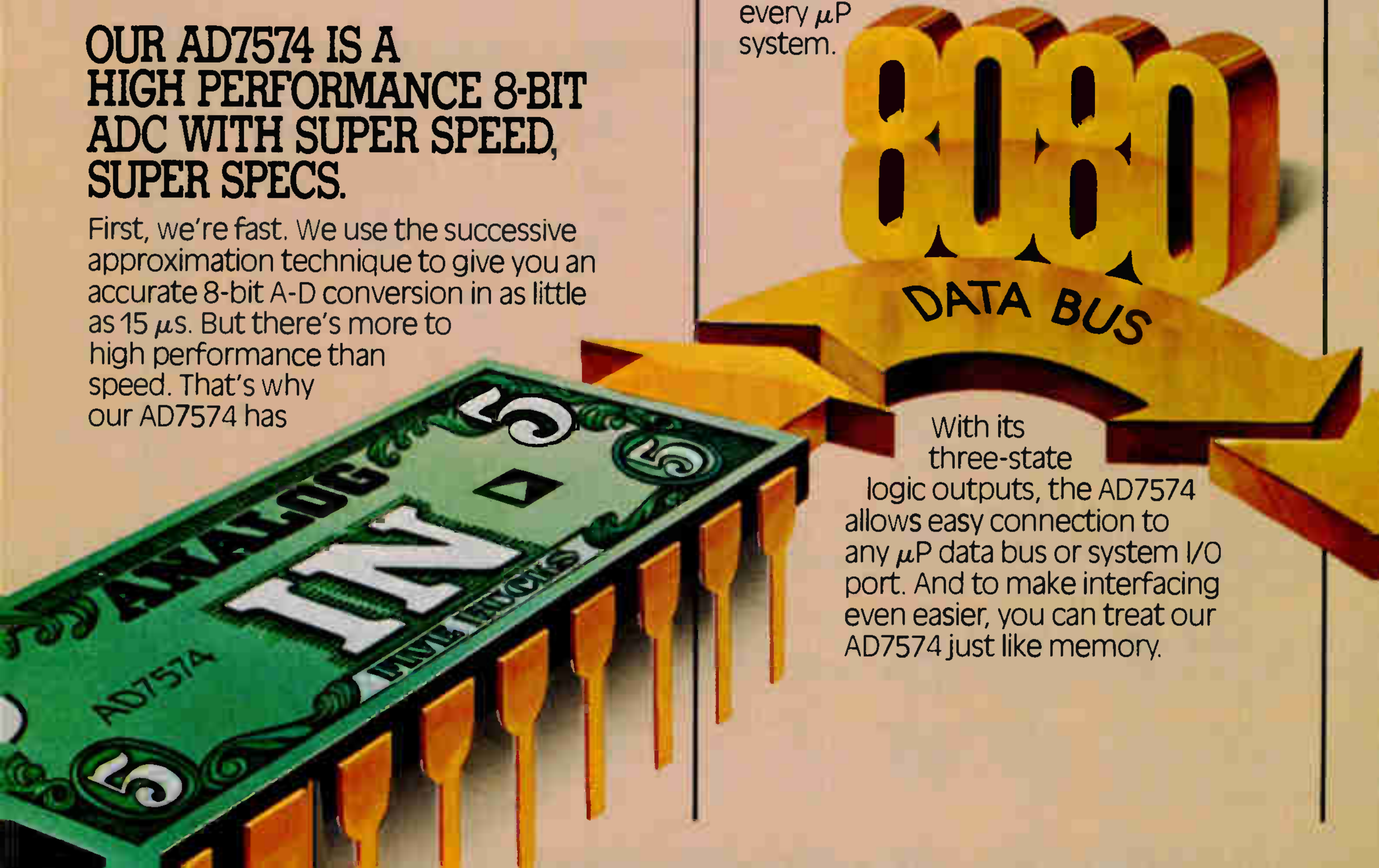

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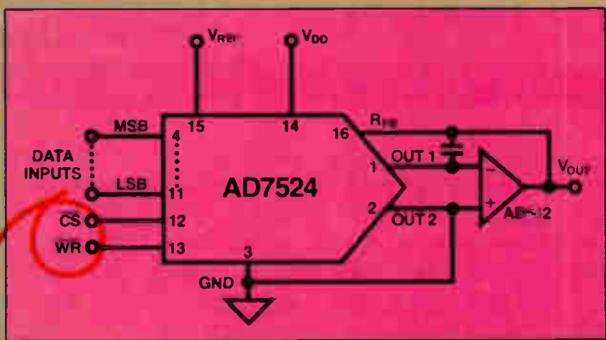

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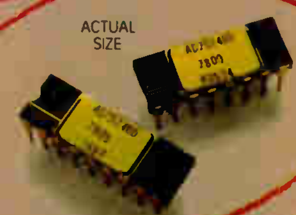

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Circle 99 on reader service card

Computers

Fixing faults by phone

Mainframe companies are finding that remote troubleshooting saves time and money while serving customers better

Fixing computers by telephone is a service technique that has been around for some time, but these days cost-conscious computer manufacturers are turning more and more to this alternative to on-site repair. In the past few months several companies have increased their investments in remote maintenance, indicating a fundamental change in the way computers are serviced.

Expectations are high. Manufacturers want to cut down on expensive, labor-intensive, and time-consuming on-site service calls, especially the exploratory visit to diagnose the cause of a computer malfunction. At the same time they want to provide better service for their customers, who are increasingly dependent on their computers.

Giving impetus to the current popularity of remote maintenance is the improved electronics technology that makes the extra remote diagnostic modules more economical than ever before. In addition, a major boost came last year, when the big name in service, computer giant International Business Machines Corp., endorsed this technique by opening remote service support centers for its new 4300 models.

Since then, Honeywell Information Systems has installed remote modules on its larger systems, and other manufacturers, including Sperry Univac, NCR, Data General, and Digital Equipment Corp., have introduced or expanded their remote service capability. But most observers agree the industry is just beginning to scratch the surface of this capability.

The doctor is in. Working at one of the stations of Honeywell's Technical Assistance Center (TAC) for large computer systems, in Phoenix, Ariz., this technician uses the telephone and a terminal to diagnose malfunctions remotely, saving the time and cost of a service call.

Inflation fighter. Of course, the manufacturers' interests are also well founded in bottom-line profits. While service has steadily been contributing to manufacturers' revenues, the operating costs—inflation-sensitive because of labor intensity—have been spiraling upward. Even the big manufacturers, who are usually the last to feel the pinch, are reporting these trends.

For instance, IBM's gross income in 1979 from machine rentals and service increased 8.7%, while the costs of these rentals and services increased 10.8%. Since hardware prices are dropping, service costs must have contributed significantly to that difference. IBM attributes the lower earnings for this sector to the "rapid growth of services." At Honeywell, the service and maintenance business has almost doubled since 1973 and now accounts for about 20% of total revenue.

Call for help. Fortunately, selling customers on remote maintenance is not difficult. It has an immediate reward for the user—up time—and the added bonus of lower service costs. Honeywell estimates it can save a quarter man-year, amounting to $10,000 a year, per large mainframe site—a savings that can be shared with the user. Data General says sales for its remote service terminal are picking up after an initial lag, and DEC estimates that about 50% of its customers now use its remote diagnostic service.

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using a toll-free number, a technique the company estimates solves 67% of the software problems. For hardware problems, the self-diagnostic capability in the 4300 provides the user with a code that is called into a service center, but a service engineer must still come to the site. If the engineer requires assistance, he can then connect the 4300, with the customer's permission, to a remote service center for a run-through.

When a user experiencing technical difficulty phones toll-free to Honeywell's 24-hour Technical Assistance Center (TAC), an up-to-date maintenance profile of the computer is pulled from a data bank. This profile is given to a specialist at the center in Phoenix, Ariz., who then discusses the problem with the user to determine if it concerns hardware or software or is operational in nature.

If necessary, with the customer's permission the specialist can connect into the system for further analysis. He can then get statistics on error rates for the central system controls and peripheral devices, as well as perform diagnostic tests to determine hardware malfunctions.

"Ninety percent of software problems can be handled remotely by field engineers," according to Sy Kraut, Honeywell vice president and general manager, field engineering operations. "The rate is not as high for hardware malfunctions, but many cases can be solved by the operator."

In addition to saving time and money, the new technique allows small original-equipment manufacturers to compete for a larger share of the computer market.

For example, Bankmatic Systems Inc., a small OEM in Portland, Ore., in business less than a year, has found that Data General's Dasher remote maintenance terminals have been instrumental in the company's ability to operate its business. Bankmatic supplies computer services to five community banks, located an average two-hour drive away from Portland, and is considering expanding out of state.

Gene Morgan, software systems supervisor for Bankmatic, calls the remote capability "the best of both worlds." He continues: "We couldn't afford to have a staff running all over the countryside. That would have meant people being out of the office, travel time, and expenses."

Bankmatic does not have exact figures on the cost savings, but Morgan thinks the system has more than paid for itself. "Our first bank customer was 3½ hours away. A maintenance call was an overnight trip. It doesn't take too many of those to pay for the terminal."

Looking at the long-range impact of remote maintenance, Honeywell's Kraut says, "I don't see remote diagnostics eliminating people. It means that for most of the future we may not need as many more people as we would otherwise." □

Reporting for this story was provided by Deborah Williams, McGraw-Hill Publications Co., and Anthony Durniak, formerly of *Electronics*.

Facts from Fluke on low-cost DMM's

Conductance: What it is, and what it can do for you.

We've often referred to conductance as the "missing function" in DMM's — the capability so many of you have wanted in a DMM but couldn't find until we introduced the 8020A Analyst.

Since its introduction, the Fluke 8020A has become the world's best-selling DMM. And four more low-cost models with conductance ranges have been added to our line. But you'll still find this function only on Fluke DMM's.

Simply stated, conductance lets you make resistance measurements far beyond the capacity of ordinary multimeters. Until the 8020A, there was no way to make fast, accurate readings from 20 MΩ to 10,000 MΩ — ranges typically plagued by noise pickup. Yet, measurements at these levels are vital in verifying resistance values in high-voltage dividers, cables and insulators.

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Here the 8020A is being used to check leakage in a teflon pcb. With a basic dc accuracy of 0.1% and an exclusive two-year warranty, this seven-function handheld DMM has made hundreds of new troubleshooting techniques such as this possible, and more are being discovered every day.

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☐ Please send 8020A specifications.
☐ Please send all the facts on Fluke low-cost DMM's, including the conductance application note.
☐ Please have a salesman call.

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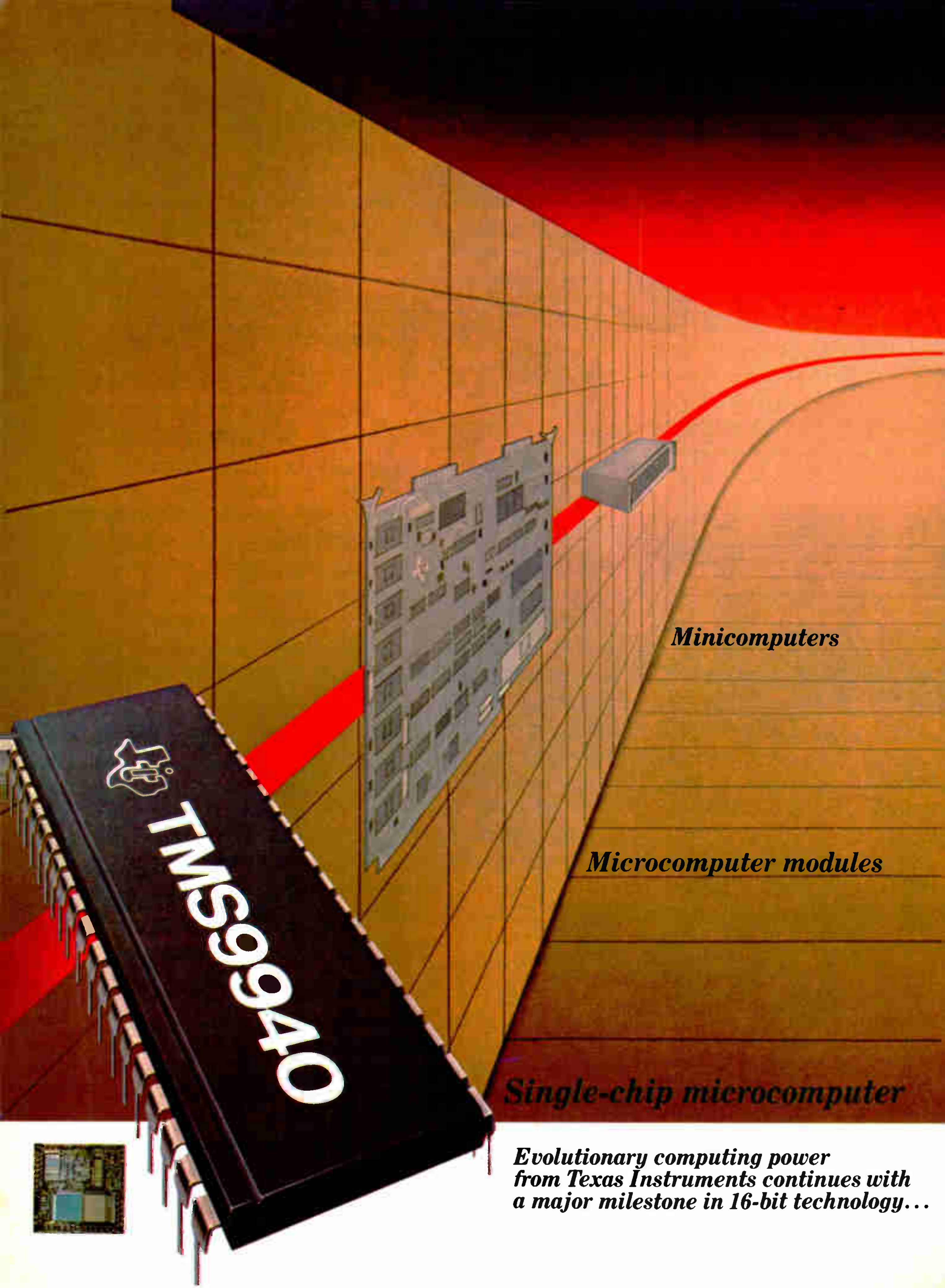
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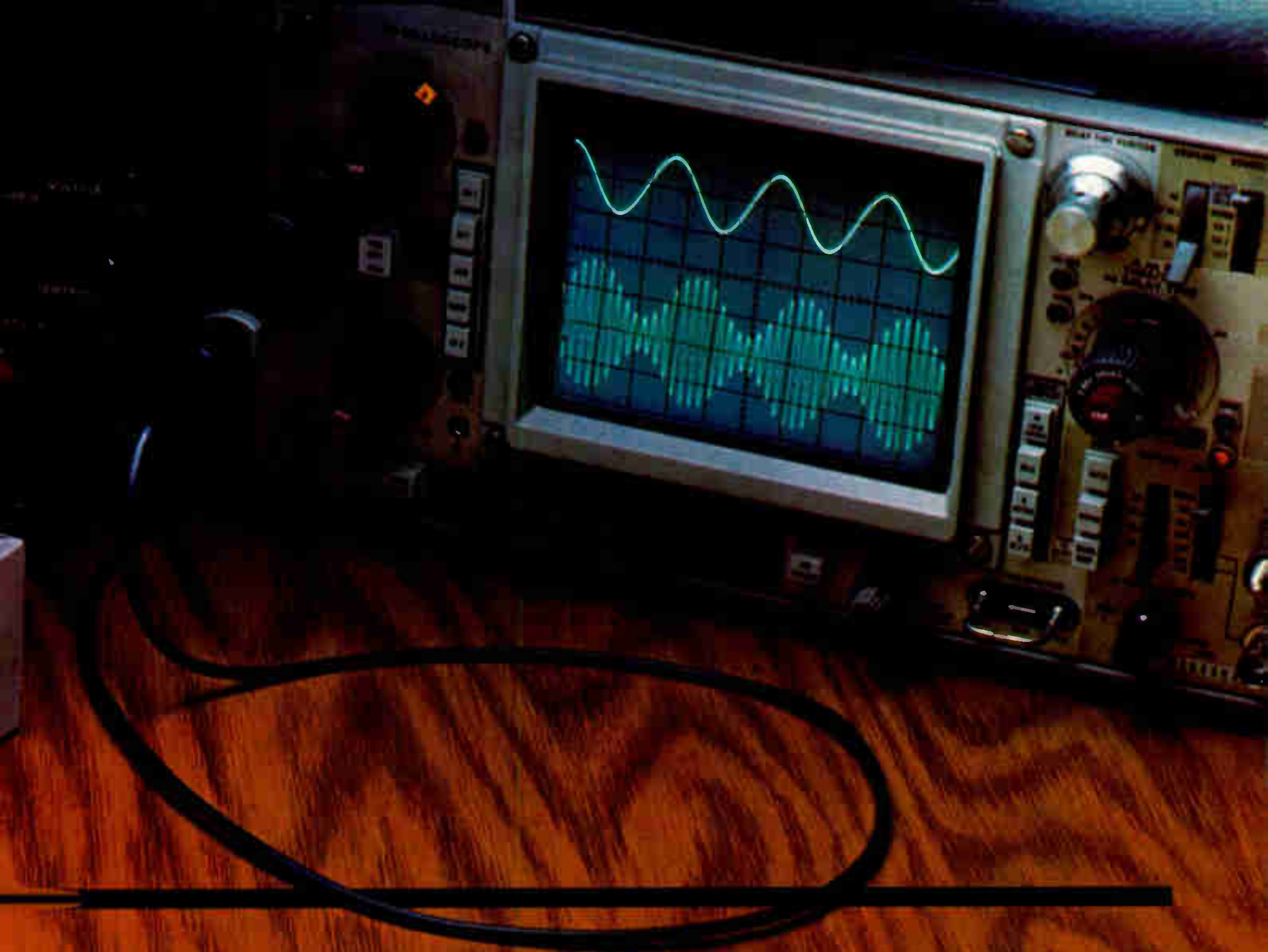

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XR-B100	69	12	16	191	24	YES
XR-C100A	22	8	6	71	14	YES
XR-D100	50	16	0	126	16	YES
XR-F100	96	36	0	296	24	YES
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	YES
XR-J100	[illegible]	12	0	116	[illegible]	YES

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Circle 107 on reader service card

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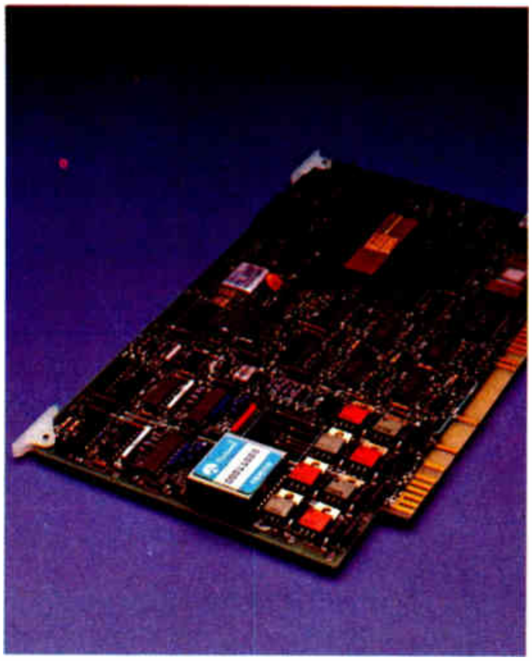

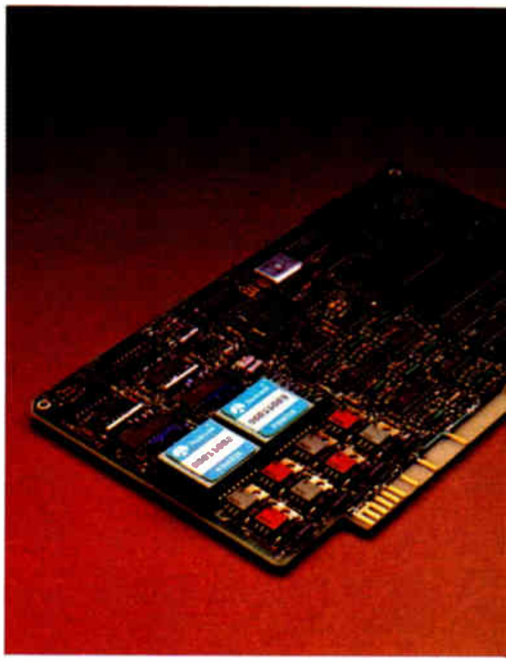

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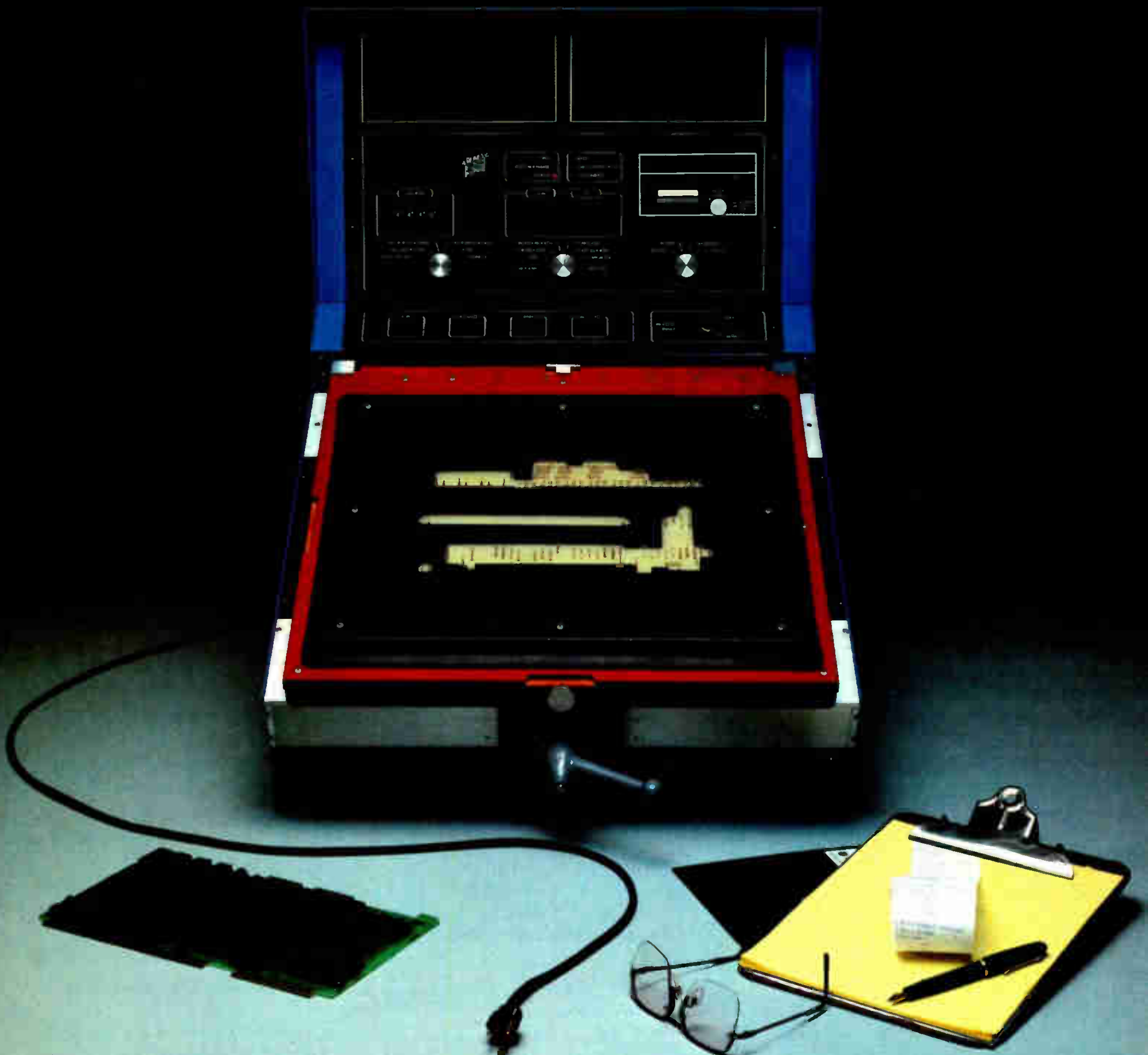

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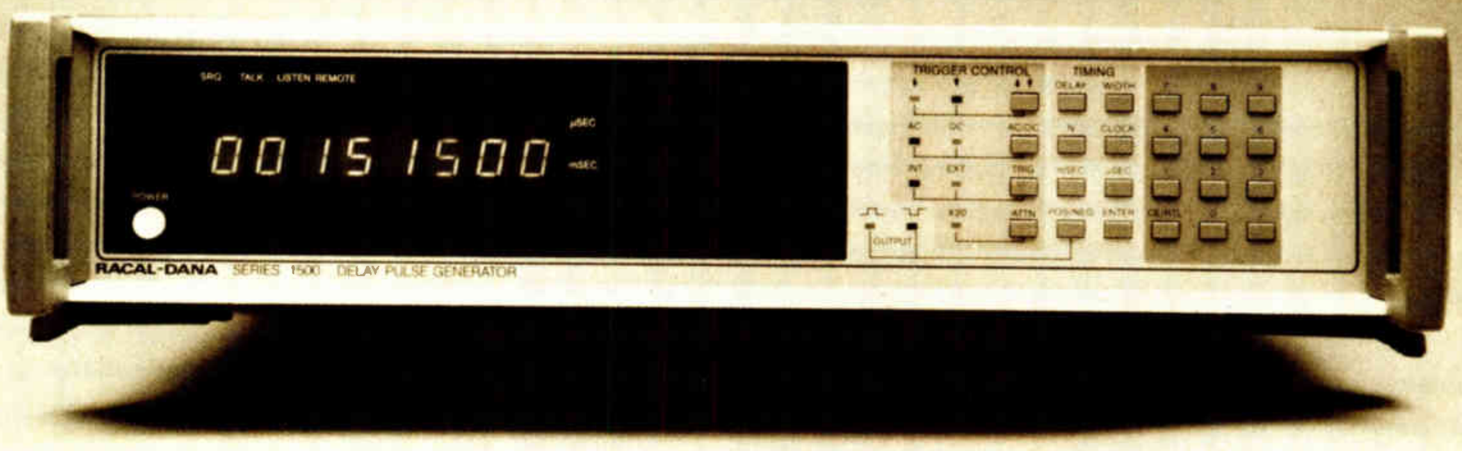


Low-cost programmable delay generator for IEEE-488 systems triggers with 10-ns resolution, takes over timing and synchronization of events

by Nelson Urdaneta, *Racal-Dana Instruments Inc., Irvine, Calif.*

☐ The application of the IEEE-488 interface standard to the construction of automated test and measurement systems has already created new forms of instrumentation, such as the bus-programmable switching matrix and dedicated bus controllers. But amidst the plethora of IEEE-488 instruments, none for management of timing and synchronization of such systems has so far emerged. Now, however, a new type of bus-compatible instrument, the series 1500 delay pulse generator, has been designed to solve these problems.

In its full configuration the unit can operate as a digital delay generator to permit fine-resolution timing of measurements, as a real-time clock to measure software execution times, and as a time-code generator for recording system events in days, hours, minutes, and seconds. Because of the way the series 1500 resolves time intervals, it does not require many costly counting elements. The basic model (without an internal clock) can be offered for about $2,500, so it is cost-effective in manual test systems. It also provides functions that are needed for automated systems at roughly one-sixth the cost of previous approaches.

Before the series 1500, builders of in-house automatic test equipment generally turned to a combination of equipment to synchronize and time system events. For synchronization, they would employ programmable pulse generators costing $6,000 or more each. Though more than adequate as stimuli for a unit under test, they often could not provide the timing accuracy or resolution needed to synchronize measurements in high-speed systems, nor was their performance free enough from jitter to ensure repeatability.

Besides the pulse generator, a system clock and time-code generator were often needed to measure and record elapsed time and the time various system functions and measurements occur. These separate elements increased cost and took up more of the address space of the general-purpose interface bus, limiting the number of other system elements that could be added.

Two solutions

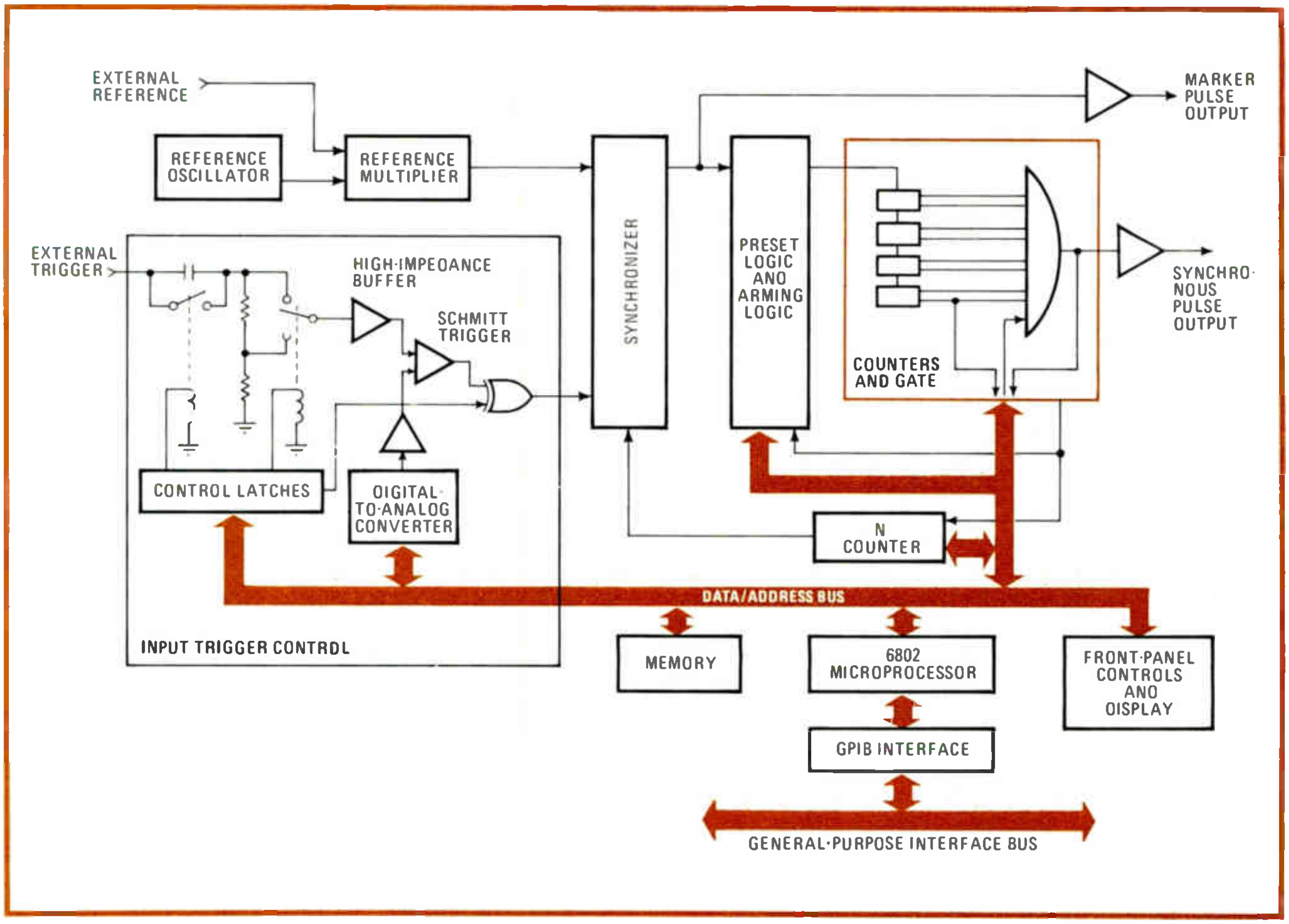
The series 1500 tackles these needs with two models. The model 1515, with internal clock, combines all three system requirements in a single instrument. The model 1510, without internal clock, does not provide time-code generation or system timing but—like the 1515—can be used for synchronizing and triggering. A user can choose the model that most economically fulfills system requirements. The series' specifications are given in the table.

For triggering or synchronizing tests, either model

CHARACTERISTICS OF SERIES 1500 DELAY PULSE GENERATOR				
Function	Specification			
	Range	Resolution	Accuracy	Other
Pulse delay and width	100 ns – 1 s	single pulse: 10 ns multiple pulses: 100 ns	± 10 ns ± oscillator error	jitter: ±2 ns, referred to marker output
Time interval	10 ns – 10^4 days	10 ms	same as oscillator	–
Time-of-day clock	100 days	1 s	same as oscillator	–
Interrupt timing	10 ms – 100 s	–	± 10 ms	–
Trigger level	± 2.5 V ± 50 V	10 mV 200 mV	–	sensitivity: 150 V peak to peak for 2.5-V range
Reference oscillator functions (switch-selectable)	Frequency	Aging	Temperature stability (20° – 30°C)	Other
Internal input	10 MHz	± 1.5 x 10^{-5}/year	± 5 ppm	–
External input	10 MHz	–	–	amplitude: 1 V rms

generates two outputs after receiving an external signal from the system hardware or unit under test or a software command from the system controller. The first output from the generator after it is triggered is a marker pulse.

The marker pulse output is a single pulse that occurs less than 100 nanoseconds after the trigger input is received. Its rise time marks the point from which the delay time set by the user is measured. Because the instrument can be programmed to begin operation only after a variety of input conditions are met—for example, after the input signal has reached a certain voltage level



1. Say when. In the series 1500, the input-trigger control circuit at left is set for various user-specified conditions. After a trigger and the reference oscillator have been synchronized, the 1500 begins the delay count in the counter circuit shown at right.

either on the rise or fall—the marker pulse can be used as a well-defined trigger for the system. It is, in effect, a system trigger derived from a complex waveform. The marker pulse has a minimum pulse width of 20 ns.

The second ouptut is called the synchronous pulse output, and its form—pulse width, number of pulses, and delay between pulses—is determined by the user. If no more than one pulse is needed, the delay time can be resolved to 10 ns; for multiple or continuous pulses, resolution is to 100 ns.

New microprocessor application

Achieving these resolutions at a price one-sixth that of earlier instruments meant rethinking the ways delay times could be measured and propagated. As a result, the microprocessor found new application. Microprocessors have been widely used in programmable pulse generators, but primarily for automation of front-panel control and internal configuration, with analog techniques still employed for the desired delays and pulse widths.

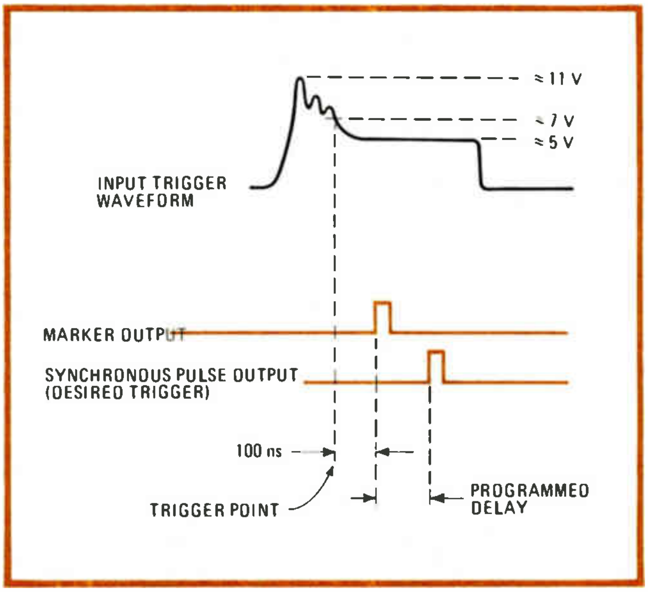
In a digital approach, three to six decades of counters are needed normally to count out time with fine resolution. Where low jitter and high accuracy requirements are essential, synchronous counters are most often used. Though these are more expensive than ripple counters, they permit counts to change only in accordance with a master clock pulse, so the propagation delay of the carry pulse from one counter decade to another is closely regulated and does not vary as it tends to do in ripple counters. One method of eliminating this variance is using very fast propagation circuits. Indeed, to achieve with traditional techniques the performance that the 1500 series offers, both synchronous counters and fast-carry propagation circuits would be needed—hardware six times as expensive as that used in the series 1500.

Timing shared

The series 1500 avoids these expenses by using the counting circuit shown in the overall functional diagram in Fig. 1. It comprises an inexpensive ripple counter, the 6802 microprocessor, and an AND gate. The output of each counter decade is tied to an AND gate input, as is a line controlled by the microprocessor.

The job of counting clock pulses to measure the delay period is shared by the ripple counter and the microprocessor. The counter circuit handles all periods up to 1 millisecond with a resolution of 10 ns, a six-decade range. The microprocessor handles all timekeeping in excess of 1 ms.

When a delay time is entered, either at the front panel or through the general-purpose interface bus, the processor retains that portion of the entry in excess of 1 ms as a multiple of 1 ms and initiates the counter for the remainder. For example, if the synchronous pulse output is to occur 10.11111 ms after the marker pulse output, the processor stores the multiple 10 in memory. It then presets the ripple counter by the complement of the remainder less one—in this instance, 0.88888. After the unit is triggered and the marker pulse generated, the ripple counter begins a count at 88888. As each decade of the ripple counter reaches a terminal count of nine, it puts out a logic 1, so at the end of the first 10,000 counts



2. Clean trigger. Generator's trigger conditions—delay, voltage level, and slope direction—are programmable, letting a system pulse be derived from complex signal, as shown. Such triggering can prevent system from reacting prematurely, for instance.

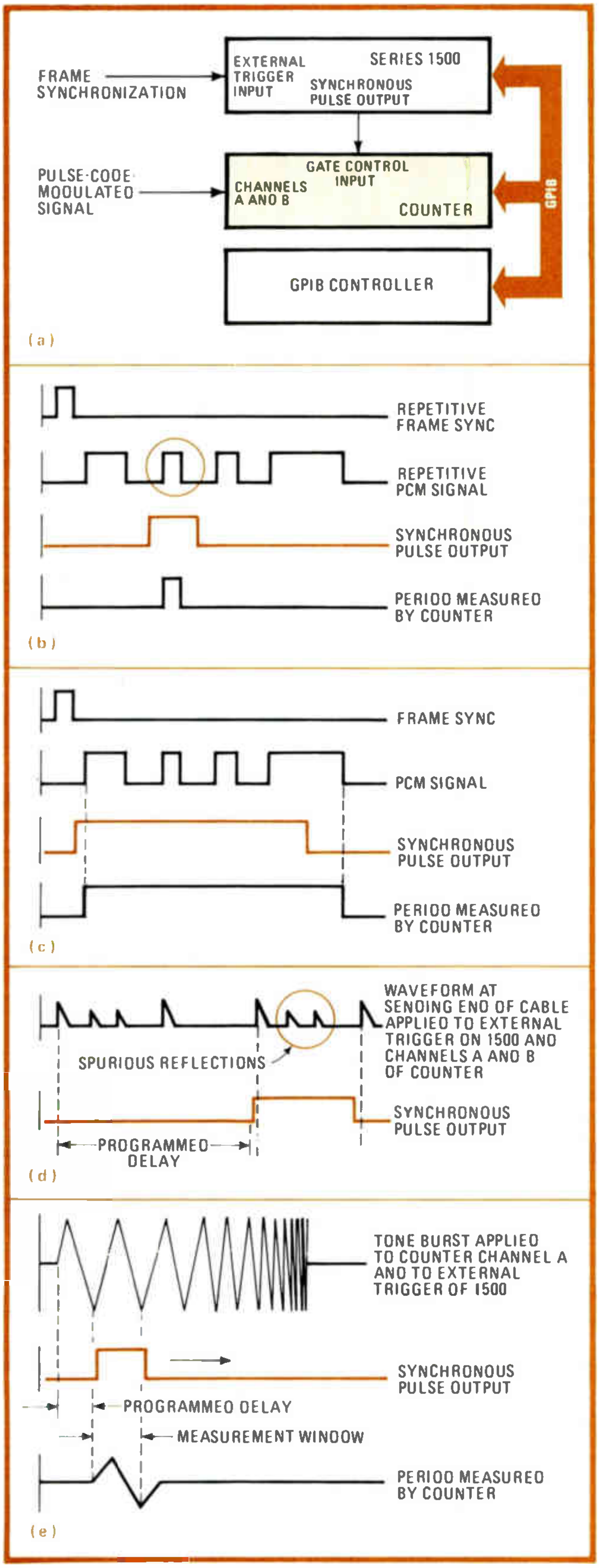
the output of the most significant decade is a logic 1.

In addition to being tied to the AND gate, the output is sent to the microprocessor. The processor executes an interrupt routine each time it receives this signal, accumulating the number of interrupts already received from the counter since initiation and comparing it with the multiple stored when the desired delay was entered—in this instance, 10. When the most significant decade has generated a number of interrupts equal to those stored—that is, when the ripple counter has gone through that number of cycles—the processor causes its line to the AND gate to go high.

At this point, the ripple counter will have counted to 99,999 nine times and the count will stand at 90,000. The output to the AND gate from both the microprocessor and the most significant decade is a logic 1. As each lesser decade reaches a terminal count of nine, its output to the AND gate also becomes a logic 1. Finally, the ripple counter's least significant decade reaches terminal count and—since all AND-gate inputs are now logic 1—the signal propagates to the synchronous pulse output port.

Task allocation

This scheme reduces overall system cost significantly by intelligently allocating counting tasks to those elements that can most efficiently and economically perform them and by reducing the number of elements necessary to achieve high accuracy. By letting the microprocessor keep track of counts above 1 ms, the scheme effectively extends the counting chain into inexpensive, low-speed, random-access memory. Most of the decades in the ripple counter need not operate at high speeds, either. Since all but the least significant decade in the ripple counter reach terminal count and put out a logic 1 at least nine clock cycles before the least significant decade, it is that decade alone which, in the end, allows



3. Transmission check. At the 1500's command (a), a counter can measure the period of one pulse (b) or an entire frame (c). In (d), the generator lets the counter ignore spurious reflections from a cable, while in (e) the periods of different portions of a tone burst are read.

the signal to propagate. Therefore, the uncertainty of the final output will be no more than the propagation delay of the first flip-flop in that decade. The other decades can be progressively slower and less expensive than the critical least significant decade.

The series 1500's timing scheme could prove useful in universal counter/timers, so it is fitting that the series 1500 borrow something from those instruments. And it does—in the form of the fully programmable trigger input, which is also seen in Fig. 1. By controller or front panel, the instrument can be set for dc or ac coupling, positive or negative slopes, and trigger levels in the range of ±2.5 V with a resolution of 10 millivolts or of ±50 V with a resolution of 200 mV. This triggering capability combines with timing facilities to permit creation of a defined timing signal from a complex waveform, such as that shown in Fig. 2.

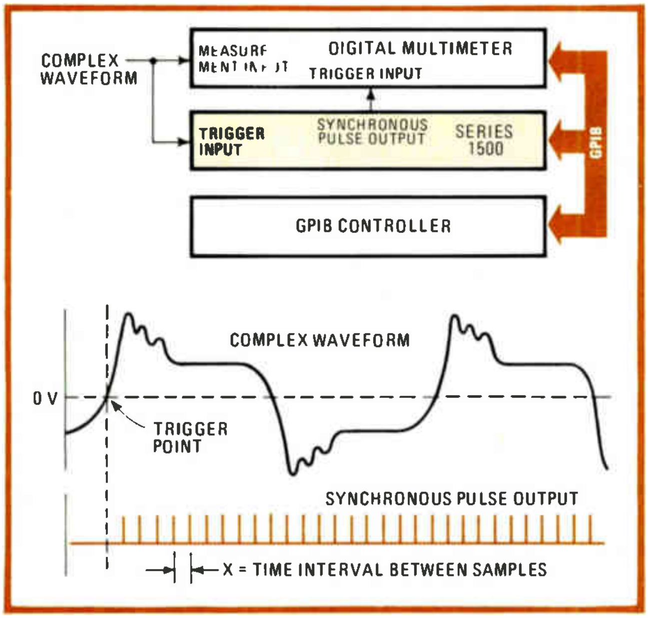
Besides synchronizing and triggering capabilities, the model 1515 can act as a real-time clock and time-code generator. Both abilities are realized by a software time-keeping routine performed by the 1515's 6802 microprocessor. As a real-time clock, the 1515 can be programmed to generate service-request (SRQ) interrupts at user-specified time intervals or after a user-specified delay. These interrupts can direct the system program to a measurement subroutine or initiate a series of measurements. It may measure a single interval or accumulate time over multiple start and stop commands. This permits timing of software routines.

Operating as a time-code generator, the clock in the model 1515 will display and put out through the bus either the elapsed time or the time of day. Data is put out in either of two user-definable formats: DD:HH"MM"SS, or DDHH.MMSS, where DD stands for day, HH for hour, MM for minute, and SS for second.

At work

The advantages of the series 1500 can be seen in its use in systems for measuring the parameters of pulse-code-modulated signals and in its ability, with a digital multimeter (DMM), to form a waveform digitizer. PCM signal parameters—such as pulse-to-pulse timing, rise and fall time, and pulse width—can be measured automatically with the series 1500, a universal timer/counter, and a system controller arranged as in Fig. 3a.

In this setup, the frame-synch pulse from the PCM system under test is used to trigger the series 1500. The total delay and the pulse width of the 1500's synchronous pulse output is here programmed by the controller to create an arming pulse for the counter during the time the desired pulse appears. The counter, at the same time, may be programmed to measure the desired pulse parameter, such as rise or fall time. The counter will ignore all pulses except the one that occurs during the synchronous pulse output, as shown in Fig. 3b. By increasing the pulse width of the synchronous pulse output, the same configuration can be used to measure the length of a word, as shown in Fig. 3c. Using two pulses in the synchronous pulse output to arm the counter, the series 1500 permits measurement of pulse-to-pulse time measurements even where the pulses, as in



4. A-d converter. For digitizing repetitive signals, the delay generator can recurrently trigger an inexpensive digital multimeter to catch readings at a precise time. The digitized values, taken at regular intervals as shown below, can then be fed to the GPIB controller.

radar simulation, are not necessarily contiguous. Adding a pulse microwave counter to the system lets it measure most parameters of a radar system, including the profile of the microwave frequencies within the output burst.

The same setup can be used to measure cable length, using the reflection time of an input signal, even in the presence of spurious reflections, as seen in Fig. 3d. Then too, the configuration can be used to obtain frequency profiles of tone bursts and low-frequency sweeps, as seen in Fig. 3e, where period measurements are made within a window and converted into frequency by taking their reciprocal. By programming the width of the synchronous pulse output of the 1500 to a time shorter than the smallest period in the burst and then incrementing the delay along the length of the burst, the entire burst or sweep can be measured on a cycle-by-cycle basis.

Low-cost waveform digitizer

The 1500's multiple pulse output can be used to make a waveform digitizer out of a high-speed DMM. Using a test configuration such as that shown in Fig. 4, digitized waveforms can be sent to the system controller where peak and root-mean-square values, linearity, frequency, and harmonic distortion can be computed.

To digitize a waveform such as that shown in Fig. 4, the external trigger input of the series 1500 is programmed for ac coupling, 0 V, and positive slope. The synchronous pulse output is then programmed for the minimum width required for the DMM trigger input; the number of pulses and the delay between them programmed by the user determines how many samples will be taken at what intervals.

For very low-frequency waveforms, this burst triggering of the DMM allows rms values to be obtained more quickly than by traditional methods such as thermal transfer techniques. For the controller to compute the rms value, it need only calculate rms using the formula:

$$\text{rms} = (R_1^2 + R_2^2 + \ldots R_n^2)^{1/2}/n$$

where R_n is one of the digitized readings.

Using the single pulse mode of the series 1500, these same measurements can be accomplished with lower-speed digital multimeters containing sample-and-hold circuits. After the first reading is taken, the delay is incremented to 2X, another reading is taken, and the delay is incremented to 3X. This process is repeated until all points on the repetitive waveform of interest have been obtained. Care should be taken that the waveform slew rate does not exceed the capabilities of the DMM.

The ease with which these and other measurements can be taken was a primary goal in the design of the series 1500. To that end, independent push buttons are used for the selection of each programmable function. Coupled with the light-emitting–diode annunciator, this permits operation of the unit with practically no training. A 3-by-4-key pad is provided for numeric entries.

The same concern is evident in the GPIB interface of the unit. Programmable from the bus for any of the trigger modes that can be established through the front panel, the series 1500 accepts data in either fixed, floating point, or exponential format. Ignoring leading spaces and 0s, it forgives any idiosyncrasy within the controller's program message.

Ease of use

Further facilitating the use of the instrument are its self-checking, troubleshooting, and calibration features. At power-up, the microprocessor goes through a self-checking sequence that tests all read-only and random-access memory. If an error such as a bad bit is detected, a message indicating the nature of the fault is displayed on the front panel.

Once the operation of the basic circuitry associated with the microprocessor is verified, troubleshooting is facilitated by setting switches on the motherboard. Setting these switches causes a repetitive digital signal to be sent to the untested hardware for the purposes of troubleshooting using signature analysis, transition counting, or oscilloscope observation of circuit nodes.

Binary switches are used for storing calibration corrections in the series 1500. At the time of calibration, voltage offsets in the trigger signal conditioners are compensated for by setting internal binary switches to the measured offset. The microprocessor then uses this value as a compensating factor when it sets the trigger levels.

Calibration of timing accuracies is accomplished in the same manner: actual delays are measured during calibration and a correction factor is dialed in on a binary switch. Whenever a new timing parameter is programmed when the instrument is in use, the microprocessor applies the stored correction factor automatically. This procedure permits timing to be trimmed to its 10-ns resolution.

With its maintenance and calibration concepts and its reduced component count, the series 1500 demonstrates a significant improvement in reliability and reduction in mean time for repairs over traditional approaches to GPIB system timing. □

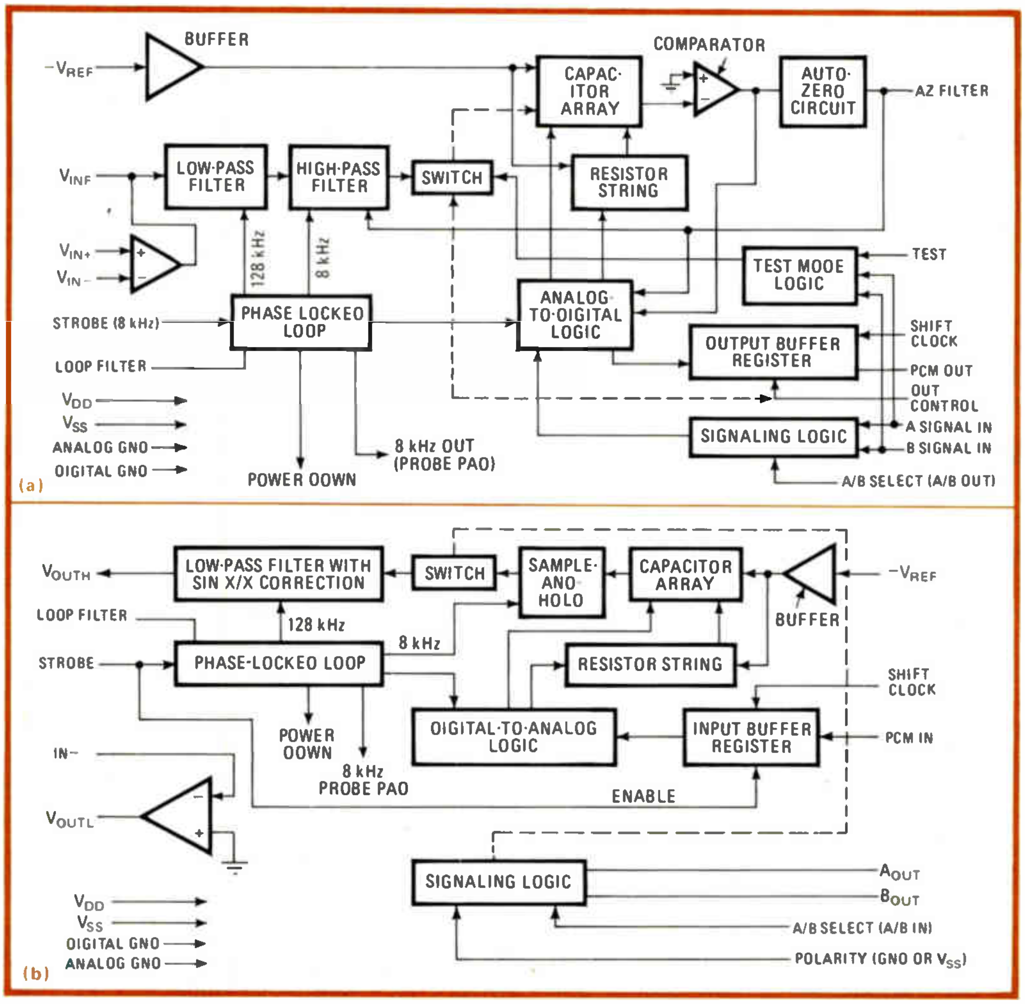
Encoder-decoder chip pair eliminates system crosstalk

C-MOS logic anticipates future telephone signaling schemes; partitioning gives codec more design flexibility

by Yusef Haque and Victor Godbole, *American Microsystems Inc., Santa Clara, Calif.*

☐ Codecs with a variety of architectures are now available for use in communications equipment. In looking for optimal, cost-effective solutions to high-level integration of telephony functions, a number of "best answers" have been claimed. Putting the entire codec on one chip has obvious face-value attraction, but there are strong arguments—notably design flexibility and zero crosstalk—for a two-chip implementation with receiving (decoding) and transmitting (encoding) functions on separate chips.

Like other codecs, the complementary-MOS S3501 encoder and S3502 decoder together form a subsystem for encoding analog signals into a pulse-code modulated (PCM) digital data stream and for decoding received PCM data, returning it to analog form [*Electronics*, May 22, 1980, p. 202]. Each chip carries filtering circuitry for its associated (transmitting or receiving) channel. The two chips can be used in a central telephone office to allow more efficient digital signal-switching to be used (see "A complete central office system," p. 117); they can be used in a telephone to put the signal in digital form before it goes out on the transmission line; and they



1. Partitioned. In the AMI codec pair, both the encoder (a) and the decoder (b) have on-board filters. The chips are packaged separately to eliminate system crosstalk and to allow the user to purchase only what is necessary for a particular application.

A complete central office system

The major elements of a typical line-interface circuit used in a private branch exchange or central office are a two-to-four-wire converter, transmit and receive filters, analog-to-digital and digital-to-analog converters, and circuitry for line supervision and control. The two-to-four-wire converter—generally implemented by a transformer-resistor hybrid—provides an interface between the two-wire subscriber termination and the transmit and receive paths of the time-division-multiplexed pulse-code-modulated data highway. It also supplies the battery feed to the subscriber telephone.

The transmit filter performs the band-limiting function needed for the 8-kHz-sampling system and the a-d converter encodes the band-limited analog signal into 8-bit PCM data words at the 8-kHz sampling rate. Typically, data words from 24 channels are multiplexed to form a PCM transmit highway.

On the incoming signal side, the d-a converter decodes the 8-bit PCM data words from the PCM receive highway into analog samples at the 8-kHz rate. Then the low-pass receive filter smoothes these samples to reconstruct the original analog signal. The line-supervision and control circuitry provides off-hook and disconnect supervision and ringing and rotary-dial pulse decoding, as well as supplying signaling bits to the a-d converter for transmission within the PCM data words.

The S3501 and S3502 provide both the a-d and d-a conversion with its associated filtering. Programmable attenuator blocks in the transmit and receive portion are needed to provide attentuation—typically in increments of 0.1 decibels over the range from 0 to 6.3 dB. This is required to overcome variations in losses in office wiring. The codec filters have zero gain, but further gain adjustments can be implemented at the input of the encoder amplifier stage or at the output of the decoder output-amplifier stage.

can be used in private branch exchanges to bring the benefits of digital switching into the office.

Partitioning the codec function into independent transmitting and receiving sections eliminates any possibility of channel crosstalk due to either sharing of the conversion circuitry or leakage between on-chip components. It also means that the two chips can be operated either synchronously or asynchronously.

When half is enough

In applications that require either analog-to-digital or digital-to-analog conversion but not both, such as digital signal processing or tone receiving, this partitioning lowers costs because only the equivalent of half a codec need be purchased and because certain auxiliary chips that may be needed to make a full codec perform are made unnecessary. Two-chip partitioning also permits the use of 16- or 18-pin packages, which are machine-insertable.

The choice of C-MOS was dictated by the desire to keep power consumption low—always a consideration in central telephone offices where many thousands of codecs are used at once. The C-MOS pair typically dissipates but 125 milliwatts in the active mode.

The choice of C-MOS also means that only two noncritical and non-tracking power supplies (+5 and −5 volts typical) are needed. The third supply (+12 V) needed for some circuits made in n-channel MOS is also eliminated.

For a given supply voltage, C-MOS gives more dynamic range than n-MOS in the codec's linear circuit elements, such as its operational amplifiers. Since these amplifiers use complimentary symmetry in their output structure, typical design voltage swings close to the maximum +5- and −5-V power supply levels are obtained in typical designs, making useful the maximum possible dynamic range of codec input signals.

C-MOS technology has one further advantage. Since a vertical npn transistor is available, the output amplifier in the decoder filter can directly drive the 600-ohm transformer in the subscriber-loop interface circuit connected to the codec. Up to +9 dBm of power is furnished for this task, plenty for all applications.

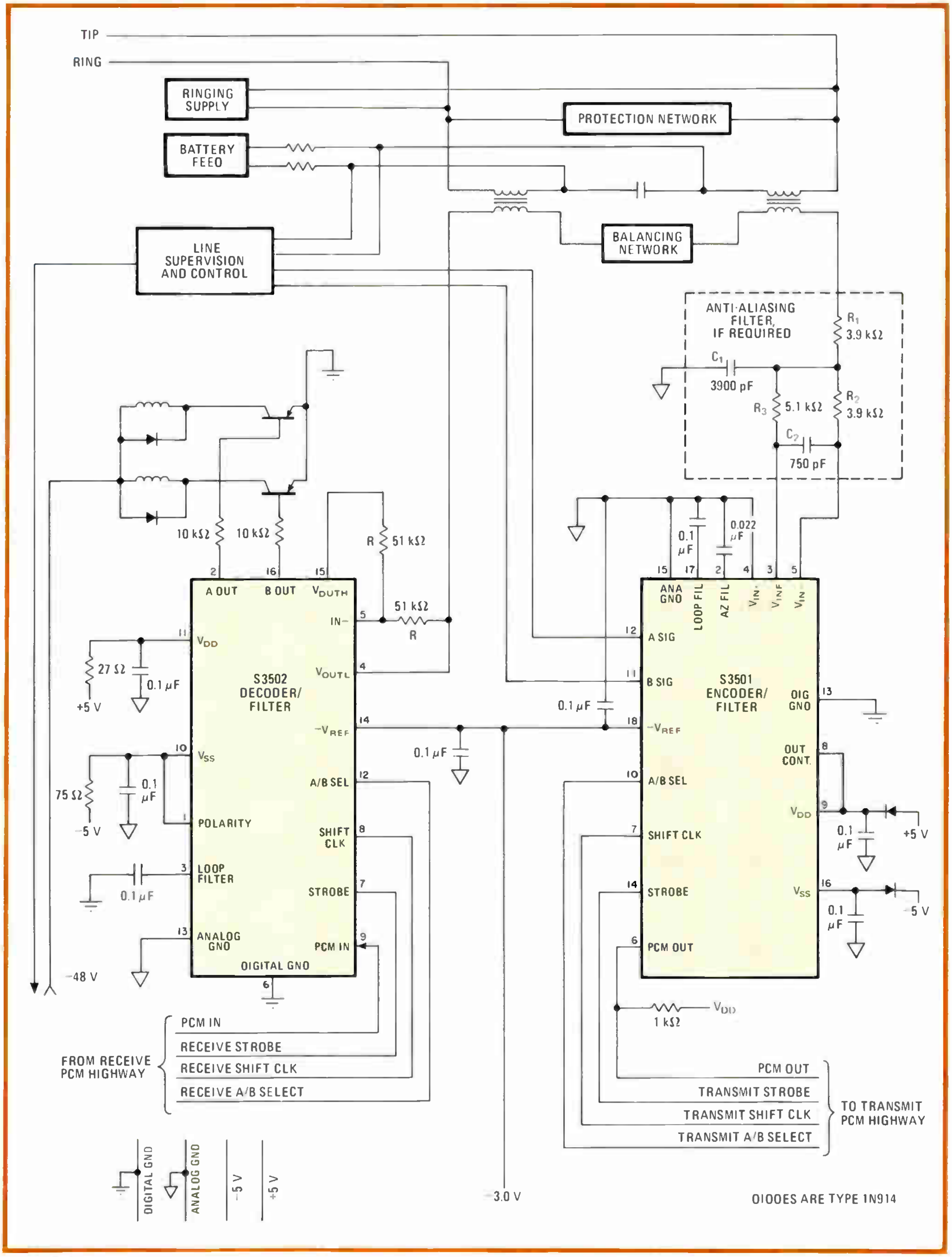
Both the S3501 and S3502 require an externally supplied −3-V reference voltage for the a-d and d-a conversion circuitry. This shortcoming is not as bad as it seems at first glance. Due to the high input impedance presented at the reference input, input current is only 100 nanoamperes, and multiple-chip sets can be supplied by one voltage reference. In fact, all codec sets in a standard 24-channel PCM system can easily share a single reference source. Commercial low-cost bipolar references with the required long-term stability and temperature coefficient (better than 100 parts per million/°C) are readily available and the cost per 24 channels for this shared reference is negligible.

On-board filters

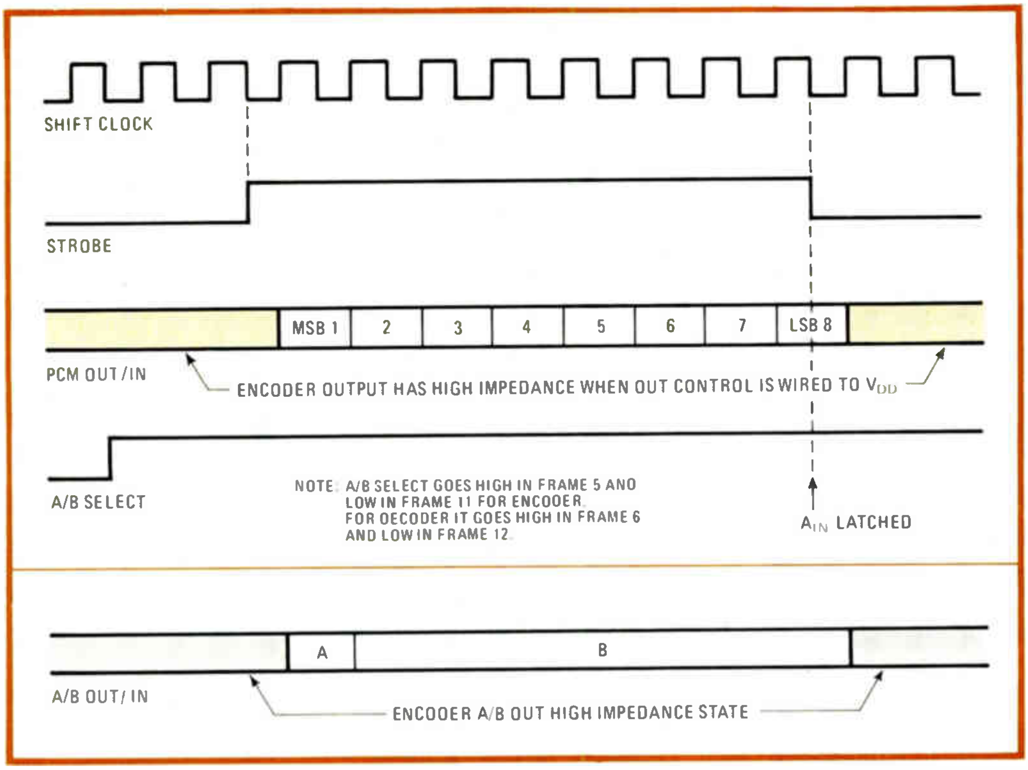
The filters that codecs require for the transmitting and receiving channels have traditionally been implemented by active circuitry using either discrete components or hybrids. These filters require component trimming to achieve their frequency-response characteristic. Recent design advances in monolithic switched-capacitor filters have made possible monolithic realizations of these filter functions with no external components or frequency-response adjustments. Many manufacturers have made monolithic filters available, but few have done so on the same chip as the d-a or a-d converter. AMI and others have integrated the encoder and its filter on one chip and the decoder and its filter on another because the approach has considerable advantages in addition to the reduction of system chip count.

With an integrated filter, a phase-locked loop can be used to generate all timing signals for the filter and conversion circuitry from the system's 8-kilohertz sampling strobe signal. If this is done, the filter clocks and the a-d and d-a conversion clocks have an exact harmonic relationship with the 8-kHz strobe signal. This eliminates the need for a smoothing filter between the transmit filter and the a-d converter.

Furthermore, since such a timing scheme means the sample-and-hold function in the encoder can be elimi-



2. Central office. The S3501 encoder and S3502 decoder are connected in a central telephone office much as are one-chip codecs; antialiasing filter is needed if 128-kHz noise is present. Both present and anticipated A/B signaling formats are taken into account.



3. Waveforms. In a typical pulse-code-modulation multiplexed telephone system, the codec's TTL-compatible strobe input is driven by an 8-kHz signal. When a logic 1 level appears on the strobe line, 8 PCM bits are encoded or decoded at the data highway's shift-clock rate—between limits of 56 kHz and 3.2 MHz for the S3501/S3502.

nated, its contribution to the codec group delay is eliminated, improving an important system specification. It is also important to remember that with this approach the a-d and d-a conversion rate is based on the 8-kHz strobe only and is independent of the PCM data rate. So any arbitrary data rate from 56-kHz to 3.2 megahertz may be used. This increases the codec's range of applications.

The use of a phase-locked loop to derive all timing signals has one more advantage. A simplified power-down scheme can be implemented by simply gating off the 8-kHz strobe signal when the channel is idle. The phase-locked loop then detects the unlocked condition and powers down all the active circuitry. Total power dissipation is reduced to less than 25 milliwatts in this mode of operation.

Other system design improvements have been incorporated in the chip architecture. They can be immediately used in a typical central-office telephony application (Fig. 2). For example, to minimize the noise induced in the codec circuitry by nearby power lines, the low-pass filter in the encoder is followed by a third-order Chebyshev high-pass filter. This filter provides attenuation of at least 25 decibels below 65 hertz. And, for further noise immunity in the codec, its operational amplifiers and comparators have 75- to 85-dB rejection of power-supply noise. Because of the codec's good noise rejection, 0.1-microfarad bypass capacitors are sufficient for power-supply decoupling in most applications. Idle-channel noise of 14 dBrnC or better has been obtained for the full channel using the S3501 and S3502.

There is yet another source of noise that is of concern since the switched-capacitor filters are sampled-data filters. Any extraneous signal or noise components at the input of the transmit filter in the vicinity of the filter sampling frequency (128 kHz) fold back into the filter passband. In most cases these components are negligibly small so that no external filtering at the input is necessary. However, if extraneous signal or noise in the vicinity of 128 kHz is significant, an external two-pole RC filter (formed by R_1, R_2, R_3, C_1, and C_2 in Fig. 2) should be added. This is used in conjunction with the uncommitted on-chip input amplifier to provide sufficient attenuation for these undesired-frequency components. This second-order filter can readily be designed to have negligible impact on the codec passband characteristics. Transmit-channel gain adjustment can also be accomplished by changing the gain of this filter.

A similar antialiasing filter is not necessary at the output of the decoder since the transformer has band-limiting characteristics and the received signal is sent to the subscriber connection of the system.

Simplified timing

The internal design of the codec chip set allows for a simple solution to an ambiguity problem in codec system timing. Unless the codec is timed with the proper edges of the clock signal, the user cannot be sure that the eighth data bit is not shortened or the first data bit is not lengthened. To ensure that this timing is accomplished properly, data is shifted out of the encoder on the positive edges of the shift clock.

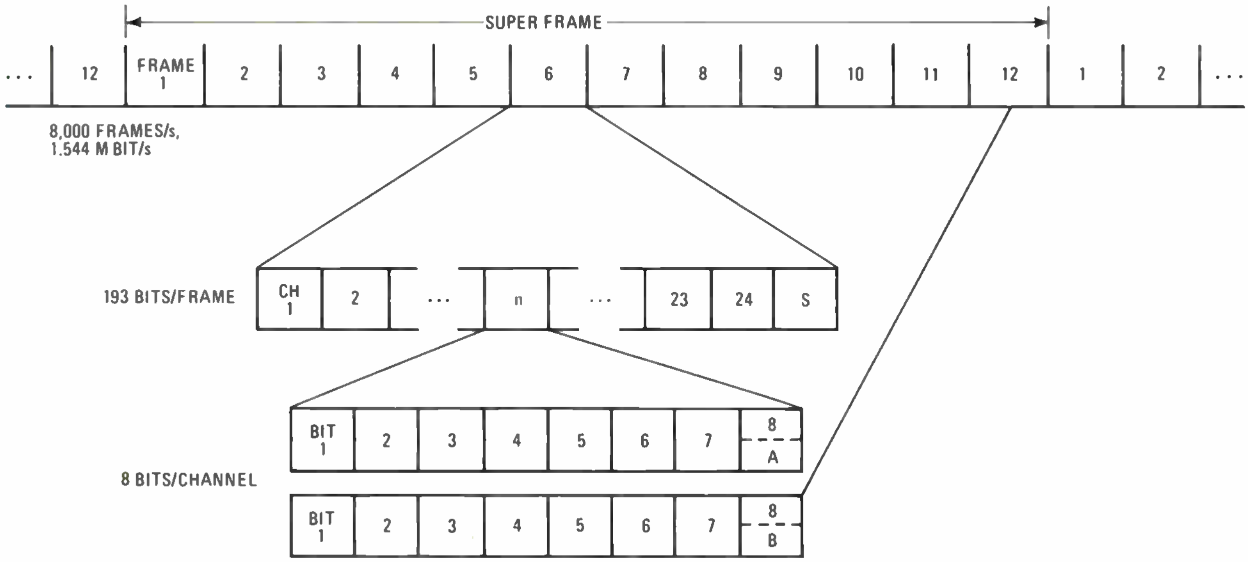
At the same time the 8-kHz sampling strobe is synchronized to the negative edges of the shift clock. In the absence of the strobe signal, the encoder output goes into a high-impedance state, in coincidence with the positive edge of the shift clock. With this timing approach, all 8 data bits on the PCM highway must occupy equal time. This permits the logic to sample data bits (synchronized with the negative edge of the shift clock) at the center of the bit "on" time, avoiding any chance of ambiguity

Sending the signal

In American Telephone & Telegraph Co.'s T1 Carrier PCM format, A/B signaling is used to convey channel signaling information. This information varies with the service requirements and according to whether the application is subscriber, direct, toll-connecting, tandem, or intertoll. It might include the on- or off-hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, or ring ground.

Usually, provision is made to send two signaling conditions—A and B—per channel, giving four possible signaling states per channel repeated every 12 frames. This requires a sampling period of 1.5 milliseconds per signaling condition. The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling condition is sent in frame 12. In each frame, bit 193 (called the S bit) performs the terminal framing function and serves to identify frames 6 and 12 (see figures).

Use of the bit 8 in the PCM channel word for signaling causes a slight degradation in the signal-to-quantizing-distortion ratio and increases idle-channel noise. The D2, D3, and D4 channel bank formats allow for future use of common-channel interoffice signaling (CCIS), which multiplexes signaling for all 24 voice channels onto a separate signaling highway. The S3501A/S3502A codec set is designed to accommodate a separate A/B signaling highway and facilitate the CCIS scheme.



(Fig. 3). The decoder uses a similar scheme for reception of PCM data.

The S3501 and S3502 are designed to simplify the signaling interfaces (see "Sending the signal," p. 120). For example, the A/B-select input pin is transition-sensitive: it selects the A signal input on a positive transition and the B signal input on a negative transition. A common A/B-select signal can thus be used for all 24 transmit channels in a channel bank instead of two separate select signals.

Encoding signaling data

The A/B-select input is internally synchronized with the strobe input and thus each individual encoder in such a bank is able to derive its own A/B-select input in the proper time slot. The A/B-select input must go high at the beginning of frame 5 and low at the beginning of frame 11. The encoder logic then puts out the A signaling bit at the time slot of bit 8 in frame 6 and the B signaling bit similarly in frame 12.

A similar scheme is used for receiving the A and B signaling bits in the decoder. There is, however, one difference. The A and B signaling bits are latched to the output in the same frame where the A/B-select input makes a transition. With this approach, the A/B-select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

The received A/B signaling bits are usually used to control A and B signaling relays. It is common practice to use 48-V relays that operate from the −48-V supply available in the central office. The decoder's signaling-output logic was designed to facilitate this relay driving with a pnp transistor interface. In this approach the decoder logic latches the received A and B signaling bits and performs a level translation that provides an output voltage swing from −5 to +5 V dc for the signaling-bit change from logic 1 to logic 0.

Thus, with the received signaling bit equal to a logic 1, the signaling output is −5 V dc. This supplies sufficient base drive to the pnp transistor to turn the relay on. At the same time, when the signaling bit is a logic 0, the output voltage changes to +5 V dc. This allows reliable shutdown of the grounded-emitter transistor and turns the relay off. For relay drive capability, the polarity pin on the decoder is connected to the V_{ss}, or power-supply, pin. TTL compatibility at the signaling outputs can be achieved by connecting the polarity pin to digital ground. In this connection there is no inversion of the signaling output level with respect to the received bit polarity. □

Transformerless inverter cuts photovoltaic system losses

Design eliminates the iron-core losses that hurt efficiency during long low-load periods

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☐ The eventual viability of photovoltaic power systems for the home depends on more than the development of efficient solar cells. Any losses that can be eliminated from the system reduce solar-cell area requirements, making the system more competitive.

One place in the power system where significant losses occur is the dc-to-ac inverter. Iron-core losses in a typical inverter's transformer can impair a solar power system's efficiency during the long off-peak hours of a daily load cycle. Thus a transformerless inverter design was developed to boost the efficiency of a photovoltaic system and reduce its solar-cell area requirements substantially [*Electronics*, Dec. 6, 1979, p. 69].

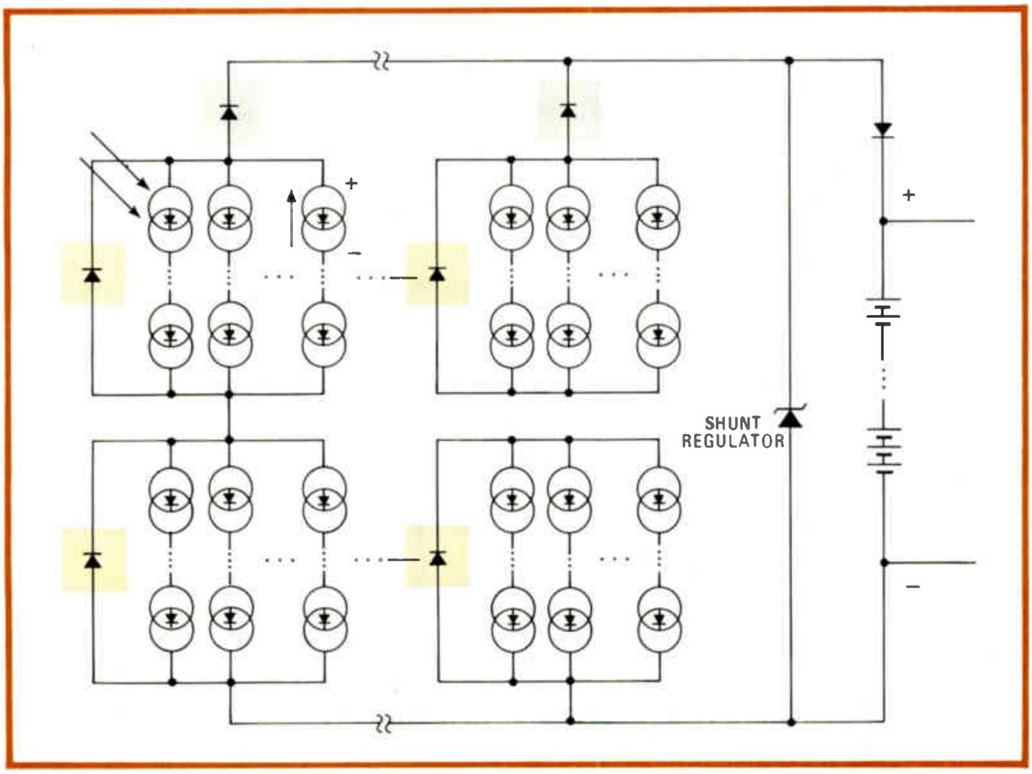
The 2-kilovolt-ampere prototype stepped-sine-wave inverter described here is the result of approaching the classic problem of dc-to-ac conversion in a new way. A 2-kVA production version will be marketed this fall by OMERA (Société d'Optique, de Mécanique, d'Electricité et de Radio) in Argenteuil, France, a subsidiary of NV Philips Gloeilampenfabrieken (as are the Laboratoires d'Electronique et de Physique Appliquée).

This design yields a conversion efficiency that is high on the average because its no-load losses are low. The following example demonstrates the importance of reducing no-load losses in a photovoltaic system.

A solar-powered house

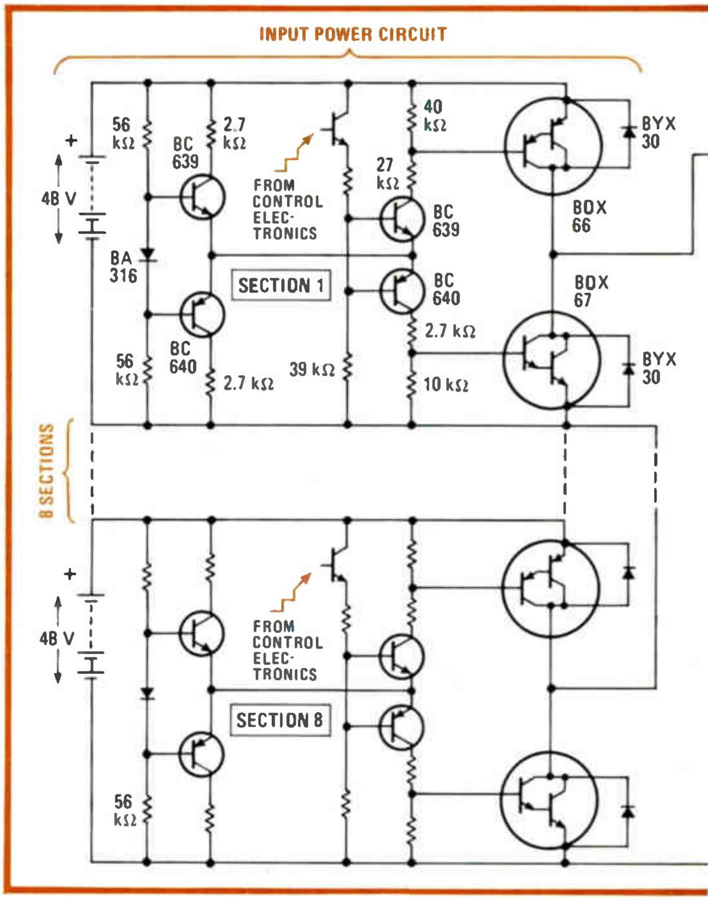
It is reasonable to assume that with thermal collectors providing central heating and hot water, a family of four could live comfortably using about 10 kilowatt-hours of electrical energy per day. This example also assumes a sunny climate such as that in the south of France, a 5-kilowatt peak photovoltaic array, and 200 kwh of backup battery storage.

If inverter losses are considered negligible, 70 square



1. Diode protection. Stacked arrays of photocells require protective diodes if the array is large. Parallel diodes across series cells prevent excessive power dissipation should the accumulated voltage reverse-bias a weak cell. Series diodes between parallel arrays further isolate the branches and reduce the chance of damage.

2. Switched on. Eight separate battery modules are switched onto the bridge circuit in a sequence dictated by the control electronics. Output voltage is determined by the number of modules on line; the bridge section adds polarity reversals. Part numbers are European.



meters (84 square yards) of silicon photovoltaic panel are required. A typical commercial photocell module measures 38 by 102 centimeters (15 by 40 inches) and generates 33 watts peak at about 16 volts. Each module contains 36 monocrystalline silicon cells in a clear silicone resin sandwiched between two glass plates.

The 5 kW required would be produced by 150 such panels. The array of cells would constitute a major part of the system cost. Yet by using an off-the-shelf inverter with a 90% full-load efficiency, photovoltaic array requirements would double.

The reason is that in this application, the inverter will operate, on the average, at a power level less than one-tenth of what it is rated to handle. This is similar to the situation faced by the utility companies, which must meet peak power demands and then run their generators underutilized for a large portion of time. As a result the no-load, or fixed, losses of the inverter become an important factor in determining the overall system efficiency, and hence the cost. For example a 10-kWh daily demand, an average demand of only 417 watts, would nevertheless require a 7.5-kW inverter—large enough to handle the possible simultaneous load demands from a washing machine and other heavy equipment. In fact, the inverter would need to withstand occasional transient demands as high as 10 kVA.

To determine the losses, recall that efficiency, η, is given as:

$$\eta = P_{out}/P_{in} = P_{out}/(P_{out} + \text{losses})$$

where P_{in} and P_{out} are input and output power, respectively. If η is 90% and P_{out} is taken as 7.5 kW, losses work out to 833.3 W, or 11.1% of the nominal output. Assuming for the example that fixed losses and proportional losses are equal at full load, then each constitutes 5.5% additional input power required, and the total input energy required to supply the 10-kWh demand can be derived.

Continuous 24-hour operation of the inverter is also assumed, so the daily fixed losses are 24 hours × 417 W, or about 10 kWh, and daily proportional losses are 0.055×10 kWh = 0.550 kWh.

The total daily input energy to supply a 10-kWh demand is then 20.55 kWh, and overall system efficiency is therefore about 50%. Furthermore, demanding only 10 kWh from an inverter that is designed to supply 180 kWh per day is wasteful. The total energy could be supplied only by increasing the number of photovoltaic panels from 150 to 300, doubling the investment in arrays of photovoltaic cells.

No-load losses

The major contributors to no-load losses in power inverters are transformer magnetizing currents, hysteresis, and eddy currents. In contrast, proportional losses are due to semiconductor voltage drops, switching losses, and IR drops and have relatively little impact on overall system efficiency; for practical purposes they can be neglected. The key to efficient low-power inverter operation rests, therefore, in the reduction of iron losses.

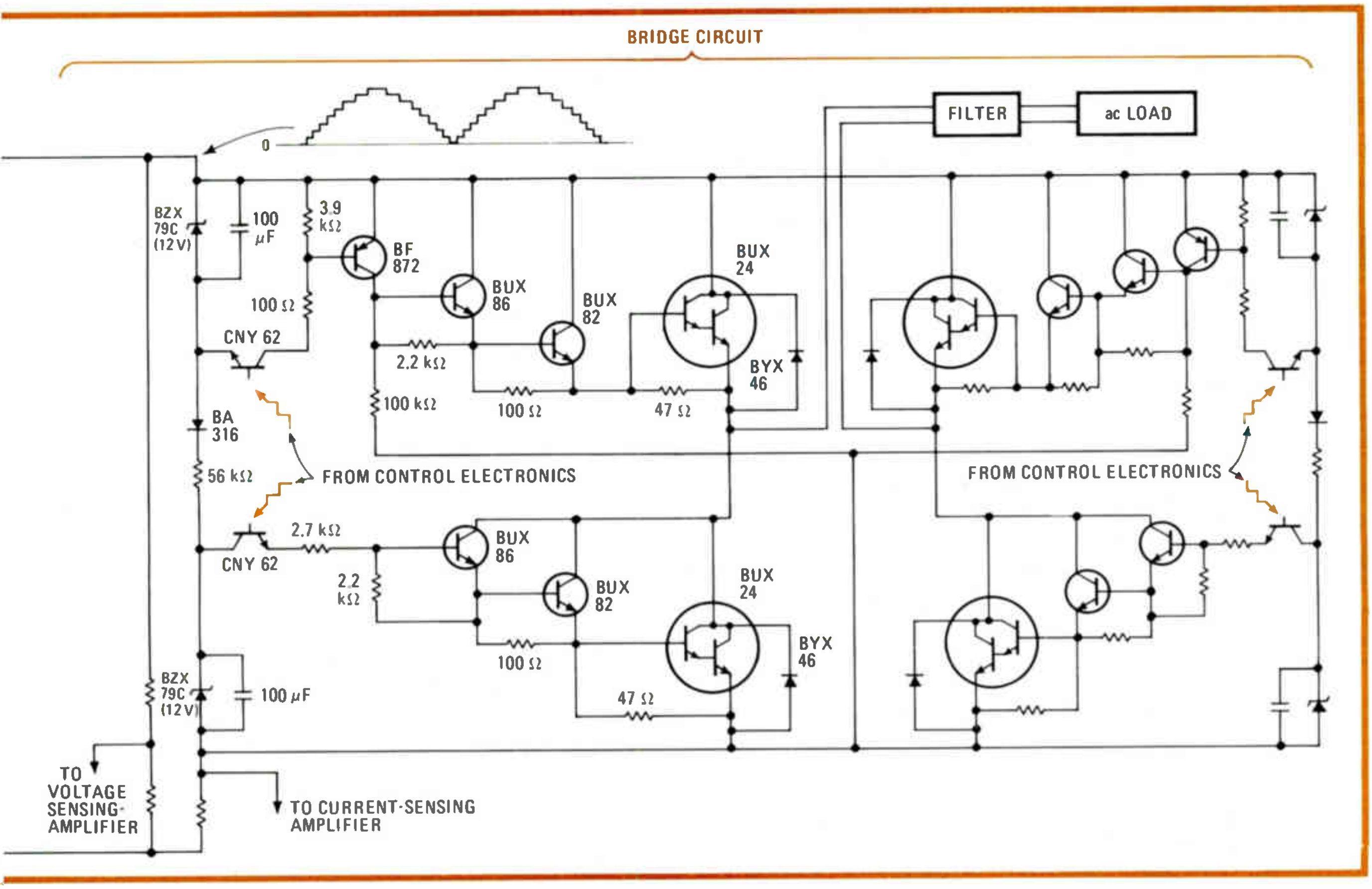
Before abandoning the transformer-based power inverter, however, several solutions that do use the device should be considered, since the inherent limitations of these alternatives are the stepped–sine-wave inverter's justification in the first place.

To sidestep the imposing fixed losses of conventional ac power inverters for widely varying loads, a system designer could:

- Automatically cut off the inverter when there is no electrical demand.
- Provide two or more inverters of different rated power, for example, 4, 2, and 1 kVA, and provide an automatic circuit for selecting the most appropriate combination at any given time.
- Assign a high-power inverter for high-demand equipment and a smaller one to low-demand appliances.
- Impose a particular time schedule on the use of various equipment in order to have the inverter always operating near its optimum working point.
- Assign an inverter to each piece of equipment.
- Install a mixed ac and dc electrical distribution network, using dc wherever possible.

Each of these alternatives adds expense, and some are not very effective. It is clear that with a transformerless inverter design it would be possible to obtain much higher efficiencies, especially at output power levels well under the rated maximum.

The stepped–sine-wave inverter differs from more common designs not only by eliminating the power



transformer. It also exploits a feature peculiar to photovoltaic power plants, that of modularity.

The stepped-sine-wave inverter develops an ac output from an array of dc sources, in this case batteries, photocells, or both. The output voltage is varied by rapidly changing the connections between each source in the array into different series and parallel circuits. The output is stepped higher and lower, positive and negative as the interconnecting switches rearrange the connections between sources.

Actually the output is not a pure sine wave, but a staircase function simulating a sine wave. By smoothing the edges of the staircase with filters and providing a sufficient number of steps, a sine wave, for all practical purposes, is produced.

Multiple dc inputs

Unlike conventional transformer-equipped inverters with two input lines to accept dc and two output lines supplying single-phase ac, the stepped-sine-wave device accepts a multisource, reconfigurable arrangement at its input. This is what most photovoltaic power plants with stacked solar panels look like.

There are limitations on the stacking of photovoltaic panels beyond which protective measures should be taken. Protective diodes must be strategically placed in series and parallel, as shown in Fig. 1, to prevent damage and breakdown.

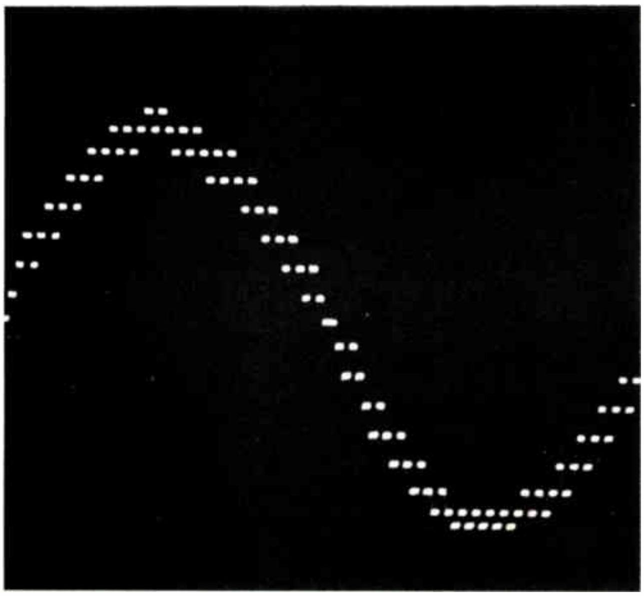
Parallel diodes are placed across series-connected photocell branches because, as the total series voltage accumulates in the string, single cells may become reverse-biased, causing excessive local power dissipation. Also, in parallel-connected photocell branches, sometimes one or more branches become a load for the others, again dissipating excessive power. This is prevented by isolating the interconnected solar panels with series diodes.

Typically, the unprotected array is safe for up to 10 branches connected in parallel, with each branch at a nominal voltage of 48 v for battery loads. If a higher voltage is desired, subassemblies of photocells or batteries may be connected in series. For example, 10 36-v assemblies connected in series are sufficient to drive the input of a transformerless power inverter capable of delivering 220 v ac.

Rapid electronic commutation of voltage sources is the basis of the stepped-sine-wave inverter. However, even relatively slow, time-dependent commutation of array interconnections can prove very useful. Being able to modify the interconnection of separate arrays allows the system to adapt to changes in photocell output.

Consider as an example the application of six photocell subassemblies to the task of charging a battery. Two parallel rows of three subassemblies each would be configured in series at high light levels and reconfigured as three parallel rows of two for low light levels. Note that judiciously adding steering diodes to the network reduces the complexity of the array wiring.

Another case of stepwise commutation of a photocell array is one where its output is defined over a period of one day. The array might be used, for example, to match the output variations of a nontracking photocell array to loads such as pumping and irrigation systems where it is



3. Many possibilities. A hybrid waveform incorporating staircase and pulse-width modulation is one of an infinite variety of simulated waveforms possible with the stepped-output inverter. The 50-hertz wave shown has peak-to-peak voltage of about 700 volts.

preferable not to use batteries. If, for instance, the pump is a lift type with a constant torque and the motor a dc type with a permanent magnet needing constant-current drive, a commutation scheme could be used to give near-constant current at optimum power output while the available light impinging on the cells goes through daily half-wave sinusoidal variations. In this case, the output voltage of the photocell array will show daily variations very close to a half-wave–rectified sine wave.

The concept of varying the wiring configuration of individual voltage sources is the principle behind the stepped–sine-wave inverter. By speeding up the commutation and using semiconductor switches, any waveform can be synthesized, including a 60-hertz sine wave.

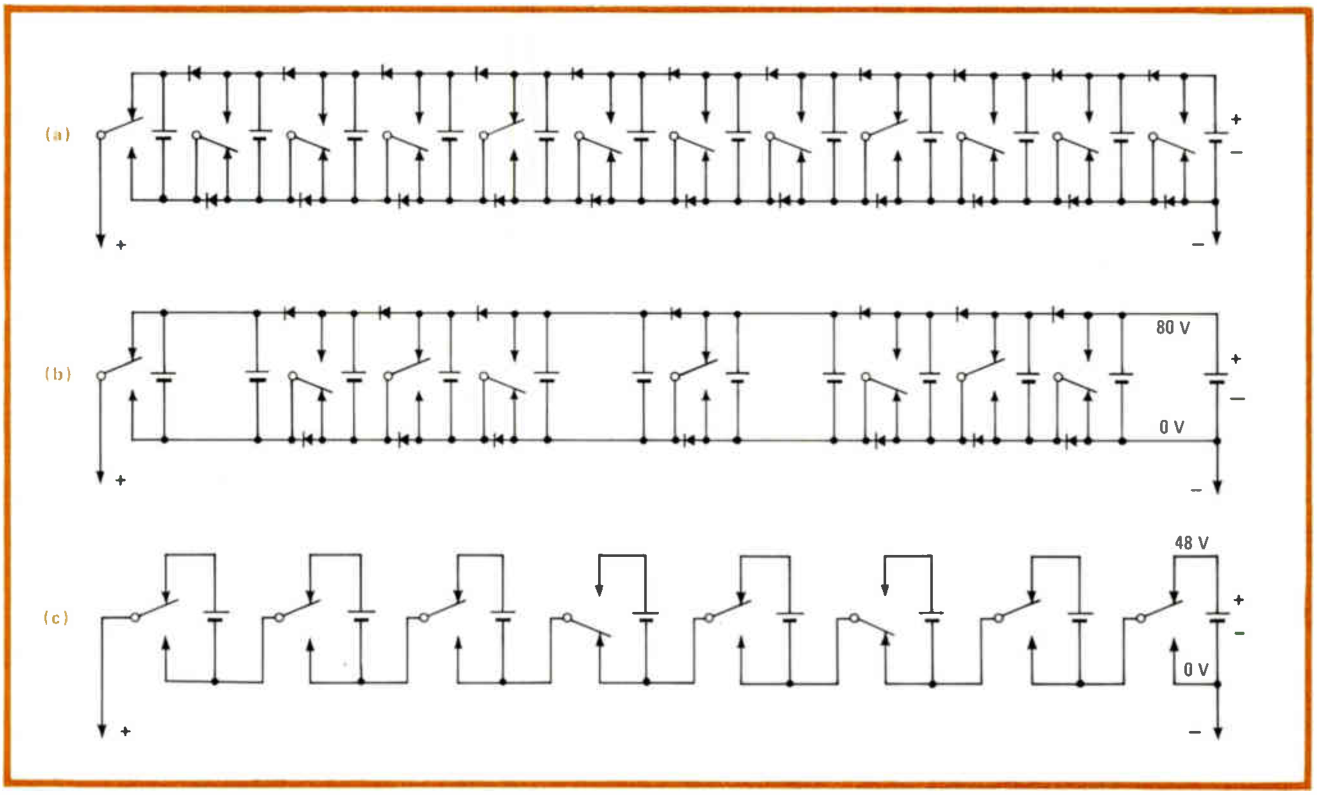
Power circuit

Figure 2 illustrates the power section of the inverter. The contents of a read-only memory within the control electronics defines the position of the solid-state switches. This memory is addressed by a clock-driven counter. The switch positions are changed rapidly, connecting the photocell/battery modules to produce the stepped 60-Hz output.

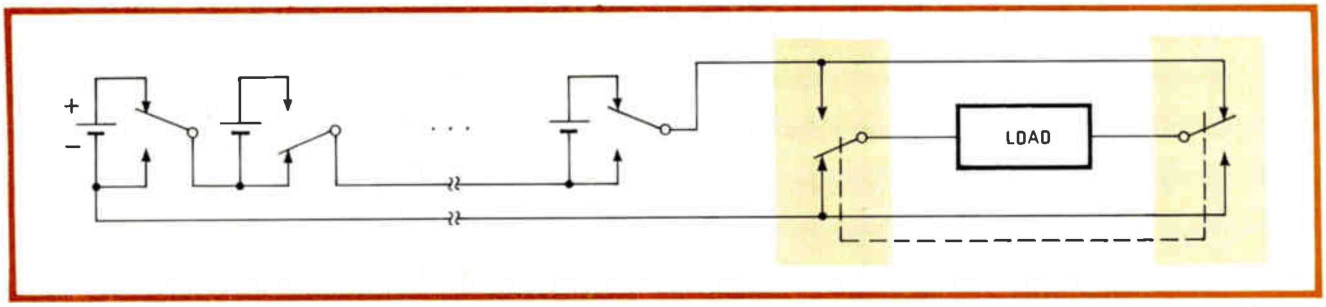
The ROM stores the code for many cycles of the sine wave. In this way, the source commutation can be varied to guarantee equal average discharge of the batteries. The zener diodes protect the batteries from being overcharged, the bypass capacitors isolate the photocells from high frequencies, and a low-pass filter reduces the radio-frequency content introduced by the switching. Figure 3 depicts the waveform obtainable with this circuit. The total harmonic content is slightly over 5%.

Regulation of the voltage is desirable not only from the standpoint of a changing load, but also because of the variations in battery voltage, which can swing from 20% above to 10% below its nominal value.

One way to achieve regulation is to modulate the commutation angles, which will increase slightly the total harmonic distortion. Another way is to pulse-width-



4. Commutation schemes. The general form for wiring sources (a) can be simplified, giving fewer combinations of series and parallel connections (b) but retaining equal discharge rate for each source. Further simplification is possible (c), but the equal discharge rate is lost.



5. Polarity reversal. Bridge circuit operation is depicted here by the load switches (tinted), which alternate to produce the positive and negative excursions of the sine wave. In the actual circuit, optically coupled silicon switches are driven by the control circuit.

modulate the voltage steps so that particular steps dwell around the ideal sine curve. Both methods require some feedback arrangement, but it need not be complex.

In comparison with conventional PWM switched-mode power supplies, transient amplitude and commutation frequencies are lower. These lower frequencies ease the tasks of filtering and of reducing iron losses in the filters.

The basic operation of the inverter in Fig. 2 can be understood by considering Fig. 4a. A multiple-source arrangement is shown wherein each battery connects to a single-pole, double-throw switch and is coupled to adjacent batteries by diodes.

Flexible switching

A special simplified case of this general structure was described in the example of the commutated photocells, using subarrays with values that are not necessarily equal and with fewer, simpler switches. With 12 identical 80-V batteries, the circuit in Fig. 4b allows six different output voltages through the use of appropriate switching combinations, namely, 0, 80, 160, 240, 320, and 480 V. In the configuration shown, batteries are discharged at an equal rate, obviating the need to keep track of different levels of charge in each battery. Other configurations may result in unequal discharge rates. However, since the circuit is reconfigurable, periodic changes can be made to balance the overall discharging of each battery.

The point is that there are numerous ways to configure an array of voltage sources to make stepped changes in output voltage. In fact, almost any waveform can be generated. It is this concept of time-dependent commutation from which the design of the stepped–sine-wave inverter is drawn.

The circuit of Fig. 4c omits all diodes and uses eight identical 48-V batteries. This allows output steps of $n \times 48$ V, where $n = 0, 1, 2, 3, \ldots 8$, and is the circuit on which the 2-kVA prototype stepped–sine-wave inverter is based. Cyclic commutation of the batteries ensures equal average discharge of all batteries. Going one step further, it is possible to monitor the batteries and electronically reconfigure them according to need or to isolate bad cells entirely from the system.

But these circuits simulate only positive- or negative-going waves, not both. To simulate a full sine wave, the voltage output must go positive and negative, and this can be accomplished in at least two ways. A complete sine wave may be synthesized using two sets of batteries and switches, so that positive and negative battery assemblies are switched at 60 Hz. Alternatively, a single bank of batteries and switches can be switched by an electronically controlled full-wave bridge circuit (Fig. 5). The latter technique was selected for the prototype.

Isolation between the prototype inverter's control electronics and its power circuitry is achieved with optical couplers (Fig. 6). The power switch associated with each battery consists of complementary Darlington power switches shunted by power diodes that bypass inductive spikes. The bridge that performs the polarity reversals has four identical power Darlington transistors, each shunted by power diodes. All power for the switching and bridge circuitry is drawn directly from the source voltage, and no auxiliary power supplies are needed.

Feedback resistors sense the output voltage and current. This information is compared with the reference signal generated in the control electronics and is used for error correction in the power switches.

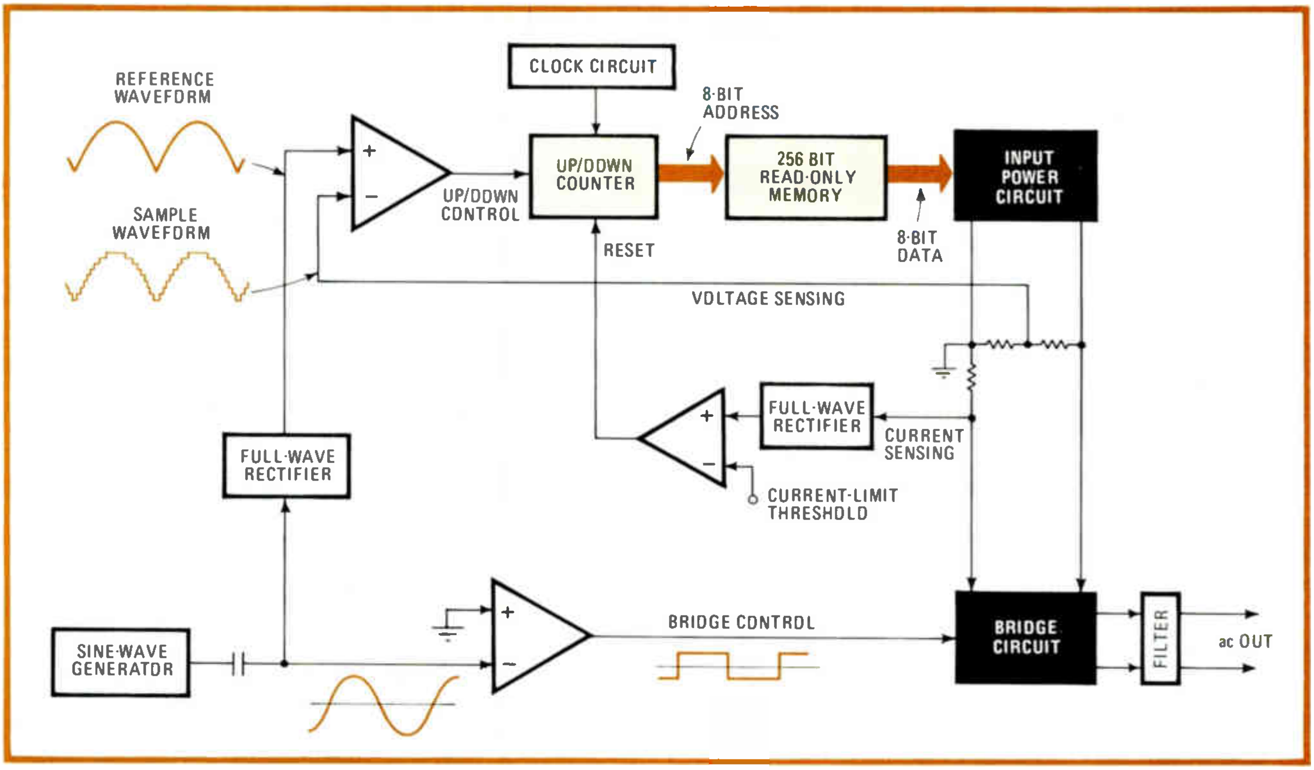
The control electronics are very simple and contain less than 10 common integrated circuits such as LM339 quad comparators, LM324 quad operational amplifiers, complementary-MOS gates, one-shots, an up-down counter, and a 32-byte ROM controlling the optical couplers. The clock frequency applied to the counter is on the order of several kilohertz. The counter's output addresses the ROM, whose output controls the optical couplers and therefore drives the power circuitry that determines the output voltage.

Comparison of the actual inverter output voltage with the reference sine wave generates a control signal that determines the operating mode of the up-down counter. The up-down counter is also controlled by feedback from the output current of the inverter. If the current exceeds a preset threshold, the counter is made to decrement rapidly, bringing the output voltage to zero. Regulation is excellent and the waveform is clean enough to run a color television receiver.

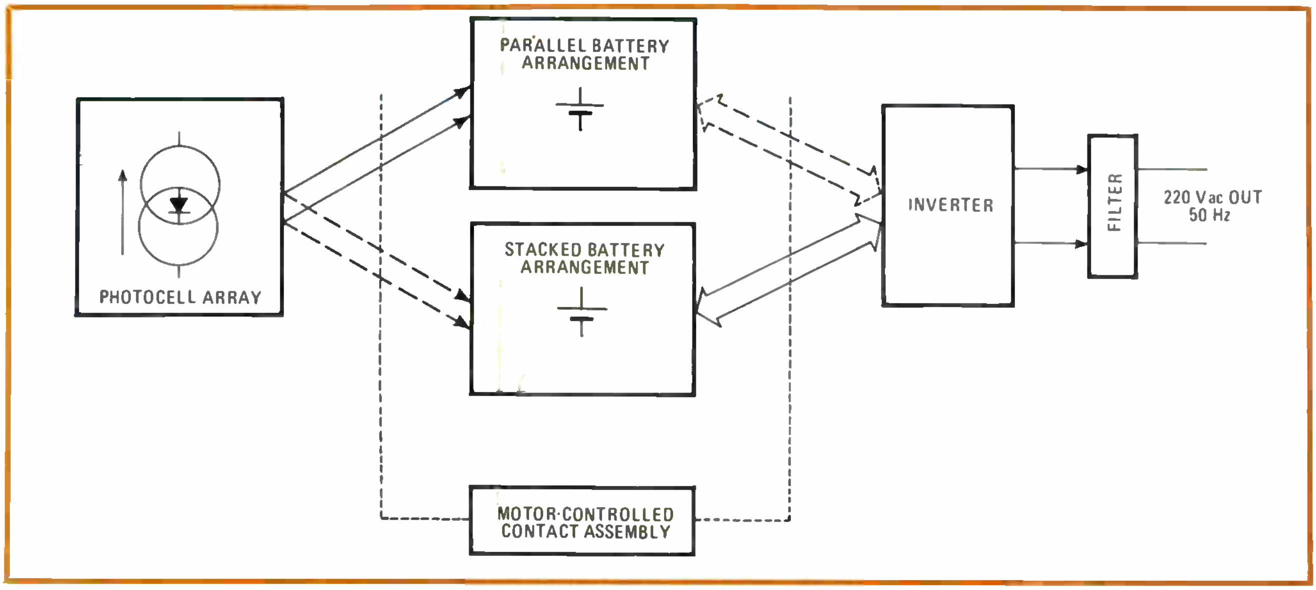
Efficiency is also excellent. At full load, it exceeds 93%. At a 100-VA output, 5% of rated output, efficiency still exceeds 90%. No-load power consumption is just 5 W and would not be much higher for a similar 10-kVA design. Total harmonic distortion is under 15%, typically 12% without any filtering.

Potential for photovoltaics

In a system for providing sun-generated electricity, the dc photocell array and ac inverter output can be isolated by splitting the battery assembly into identical halves, each capable of supplying power for prolonged



6. In control. The power circuit receives switching commands from a read-only memory coded for the desired waveform. Polarity reversals are triggered by a reference sine-wave generator but may also be in ROM. Voltage- and current-sensing taps guard the output limits.



7. Tapping Sol. If the battery modules are separated into two blocks, one may be charged by photovoltaic cells while the other powers the inverter load. The two halves exchange roles when a block approaches either an upper limit of charge or a lower limit of discharge.

sunless periods. As one half is charged by the photocells, the other is connected to the load via the inverter. When either bank is close to its upper limit of charge or to its lower limit of discharge, the halves are switched. Automatic commutation can be performed at night during low-load conditions by a motor-driven contact assembly.

Such a twofold battery arrangement (Fig. 7) simplifies battery inspection, maintenance, and replacement. Since each half will have several days' capacity, daily commutation will ensure practically identical states of charge for the two banks, and sufficient reserve capacity is available to bridge maintenance periods. As batteries are kept at nominal voltage levels (between 1.85 and 2.05 V per cell), regulation is held within ±5% without additional feedback circuitry.

If necessary the inverter can also operate as a battery charger supplying power from the main power lines. Additional flexibility and built-in functions may be implemented by replacing the ROM in the inverter with a microprocessor. □

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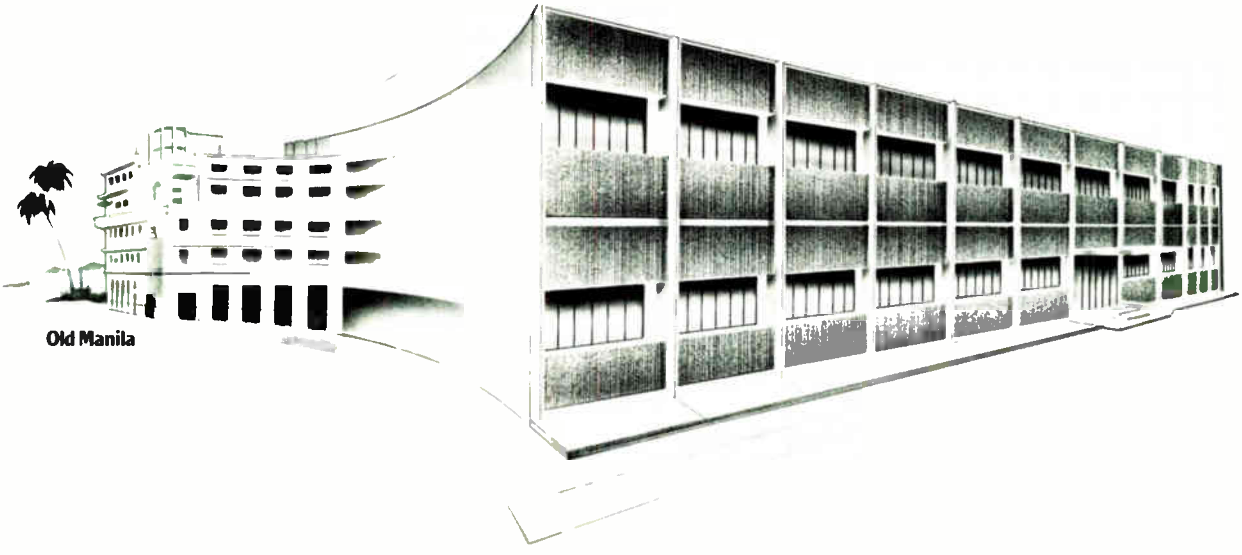

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Designer's casebook

One-chip DVM displays two-input logarithmic ratio

by David Watson
Intersil Inc., Reading, Berks., England

The popular ICL7106 series of analog-to-digital converters that serve so widely nowadays as one-chip digital voltmeters can be easily converted to display the logarithm of the ratio between two input voltages, making them useful for chemical densitometry, colorimetry, and audio-level measurements. Only slight wiring modifications at the device's input and integrating ports are required.

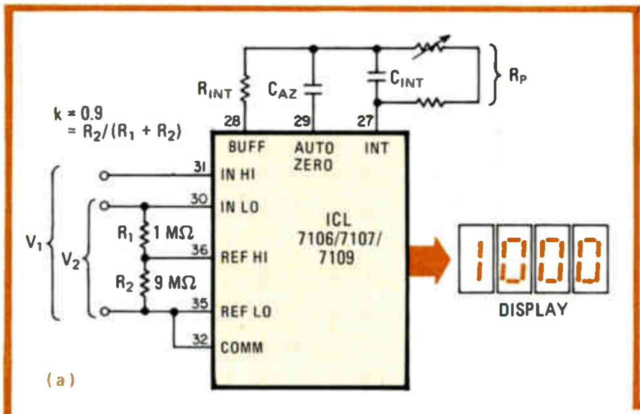
Shown in (a) is the new configuration. The modifications from the standard a-d converter connection include the addition of a resistive divider, R_1–R_2, at the reference inputs, and the placing of resistor R_p in parallel with the device's integrating capacitor.

As shown with the aid of the timing diagram in (b), the time constant of the integrating network is given by $\tau = C_{int}R_p$, with the asymptotic endpoint voltage of the integration voltage being $V_{as} = R_p(V_1 - V_2)/R_{int}$, where V_1 and V_2 are the input voltages to be measured. The final integrator voltage therefore becomes $V_{int} = R_p(V_1 - V_2)(1 - e^{-T/\tau})/R_{int}$, where T is the fixed integration period.

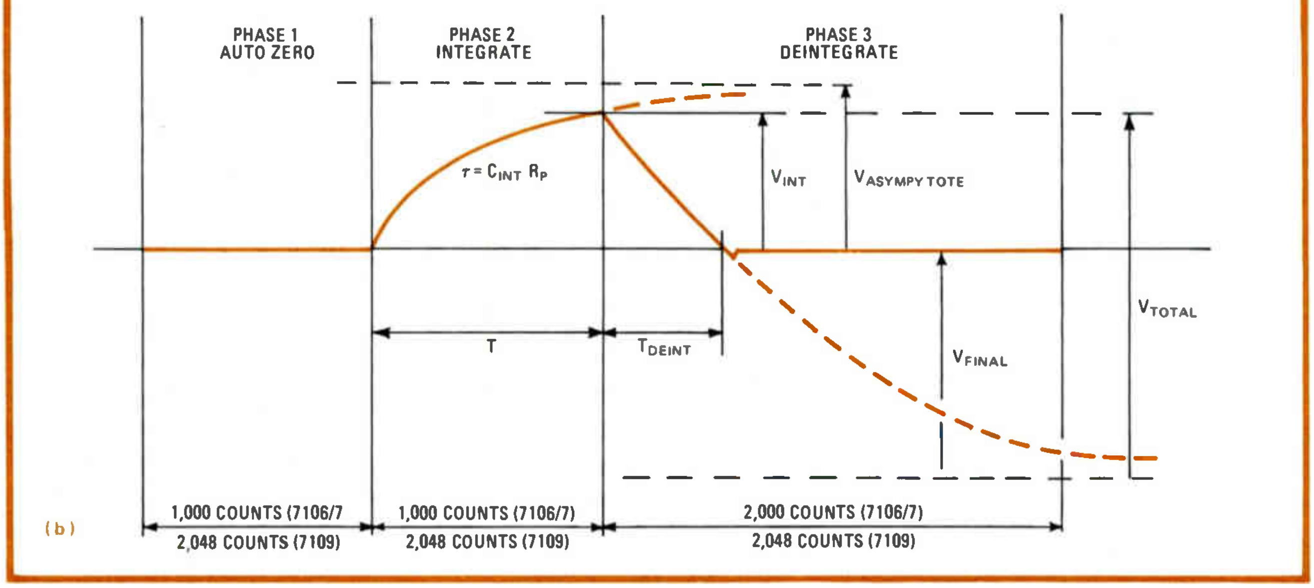
During the deintegration portion of the cycle, the exponential decay moves toward the total voltage, V_{tot}, which equals $V_{int} + V_{ref}(R_p/R_{int})$. But $V_{ref} = kV_2$, where k is set by the resistive divider, so that $V_{tot} = R_p(V_1 - V_2)(1 - e^{-T/\tau})/R_{int} + R_pkV_2/R_{int}$. The integrator voltage actually crosses zero when the exponential waveform reaches $V_{final} = V_{ref}R_p/R_{int} = R_pkV_2/R_{int}$.

As seen, the time needed to reach the zero crossing is given by $T_{DEINT} = \tau\ln(V_{tot}/V_{final})$. Making $k = (1 - e^{-T/\tau})$ and $\tau = T/2.3$, it is realized that $T_{DEINT} = T\log_{10}(V_1/V_2)$. For this condition, k = 0.9, which is achieved by making R_1 = 1 MΩ and R_2 = 9 MΩ.

Theoretically, the system's full-scale output voltage is reached when $\log_{10}(V_1/V_2) = 2$, but noise will probably limit the range of the converter. Note also that the accuracy of the system is no longer independent of passive component variations. The simplest way to ensure that k = 0.9 is to use a pretrimmed divider. The system is calibrated by making $V_1 = 10V_2$ and by adjusting R_p until the display reads 1.000. □



Log converter. ICL7106 analog-to-digital converter may be used to measure the logarithmic ratio of two input voltages. Modifying converter's input circuit (a) and integrating network and selecting suitable time constants ensure that its output is proportional to $\log_{10}(V_1/V_2)$. Timing diagram (b) clarifies circuit operation.



Digital comparator saves demultiplexing hardware

by V. L. Patil and Rahul Varma
Central Electronics Engineering Research Institute, Pilani, India

Comparing two *m*-digit numbers, where each digit comprises *n* bits, by conventional means requires the services of a demultiplexer for separating the data into two corresponding sets, $2mn$ storage elements that convert the data into bit-parallel, digit-parallel form, and *m* magnitude comparators for performing the actual comparison. The demultiplexing can be simplified, however, and the number of storage elements reduced to $3m$ with this technique, which utilizes strobed memory elements in the form of D flip-flops and combinational logic to ascertain the relationship of the two numbers.

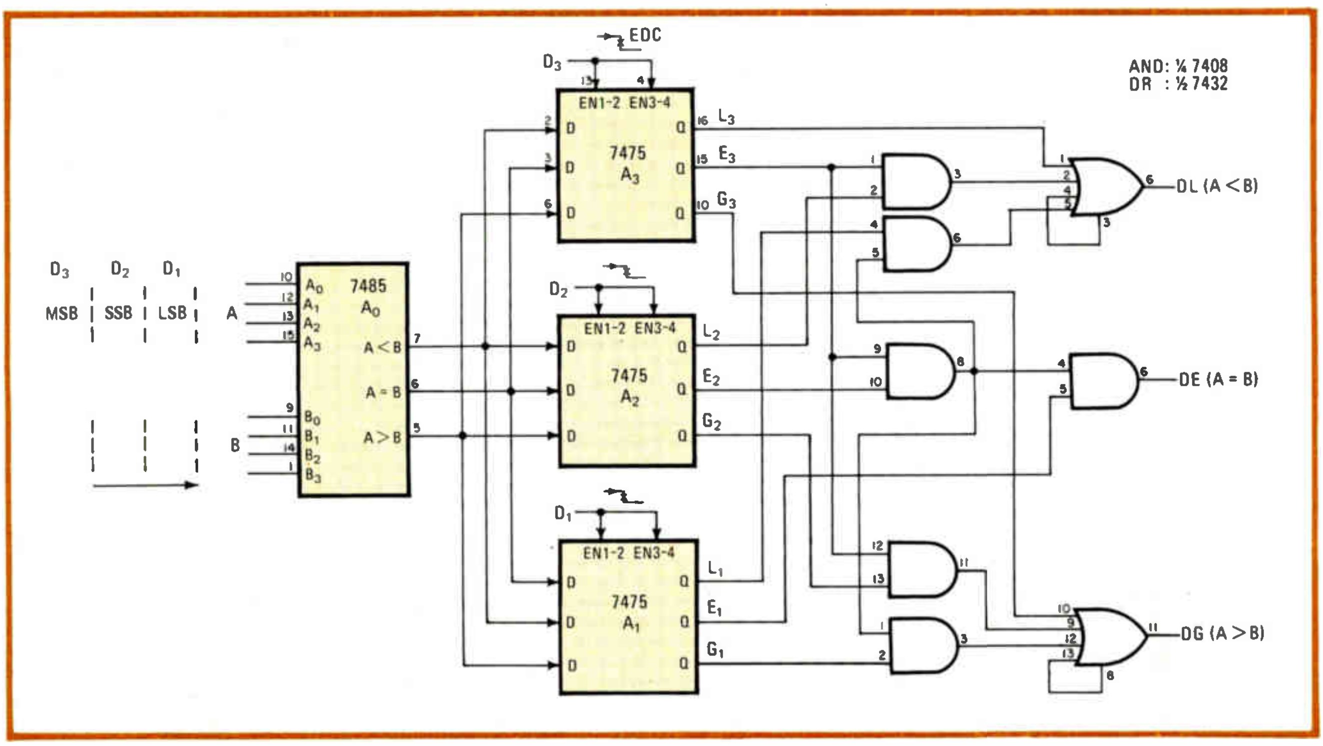
The method is illustrated for an example where two 4-bit, 3-digit numbers are compared. As seen, the corresponding digits of both numbers are simultaneously introduced to the 7485 4-bit comparator, A_0, with the least significant bits being introduced first. The result of the comparison is then strobed into the 7475 quad latch, A_1, by digit strobe D_1.

Similarly, the second-most significant bits (SSB) and the most significant bits are then strobed into A_2 and A_3, respectively, by strobes D_2 and D_3. The combinational logic that follows then evaluates the three-digit (MSD, SSD, and LSD) comparison from:

$$OL = L_3 + E_3L_2 + E_3E_2L_1$$
$$OG = G_3 + E_3G_2 + E_3E_2G_1$$
$$OE = E_3E_2E_1$$

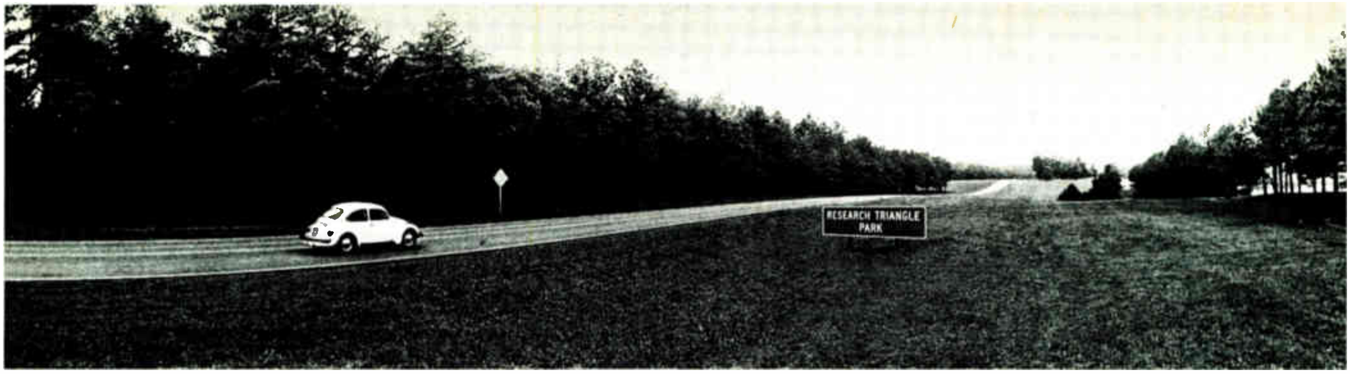
where $OL = 1$, $OE = 1$, and $OG = 1$ signify that $A < B$, $A = B$ and $A > B$, respectively, and L_i, E_i, and G_i are the individual corresponding outputs of flip-flops A_i.

The truth table outlines circuit operation. □



MSD			SSD			LSD			OUTPUT		
G_3	E_3	L_3	G_2	E_2	L_2	G_1	E_1	L_1	OG	OE	OL
>	=	<	>	=	<	>	=	<	>	=	<
0	0	1	X	X	X	X	X	X	0	0	1
0	1	0	0	0	1	X	X	X	0	0	1
0	1	0	0	1	0	0	0	1	0	0	1
1	0	0	X	X	X	X	X	X	1	0	0
0	1	0	1	0	0	X	X	X	1	0	0
0	1	0	0	1	0	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0	0	1	0

Reduction. Circuit performs n-bit, m-digit comparison of two numbers without a conventional IC demultiplexer, reduces number of memory elements normally required. Simplified decoding technique utilizes combinational logic. Truth table outlines circuit operation in comparing most, second-most, and least significant digits.



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Tracking filters demodulate two audio-band fm signals

by Stephen Barnes
Center for Bioengineering, University of Washington, Seattle

Because of the way in which they retrieve recorded data, many systems designed for monitoring biomedical functions have to demodulate two closely spaced fm carrier signals in the audio-frequency band. The original data signals could be recovered with low-pass filters, but they are an expensive solution since their cutoff must be sharp to prevent cross modulation, signal blocking, or undue limiting of the bandwidth needed by one or both signals. The low-cost solution shown here, however, uses a dividing phase-locked loop to demodulate one signal and to provide the clock signal for a tracking notch filter that recovers the other channel of data.

The advantages of the circuit may be seen for a typical monitoring case in which a 30-hertz electrocardiogram signal (having a frequency too low to be recorded directly on cassette tape) is placed on a 9-kilohertz carrier. This signal is applied to the LF356 amplifier along with a 0-to-6-kHz signal from an ultrasonic doppler flowmeter that provides data on blood circulation.

Block A, the dividing phase-locked loop module, oscillates at a free-running frequency equal to $8f_m$. It is here that the 9-kHz carrier is directly demodulated. Also included in block A is a 74C193 divide-by-8 counter in the PLL's feedback loop, which provides the driving signals for the CD4051 multiplexer in block B. This block contains the sampling filter which passes frequencies equal to 1/8 the sampling frequency, $8f_m$, and its harmonics. Thus the doppler data is notched out by the sampling filter. But signal $\vec{f}_m$ is subtracted from the original input signal $\vec{f}_o + \vec{f}_m$ by the differential amplifier in block C. Therefore, only signal f_o will appear at the output.

Resistor R_Q, which is in the PLL's feedback loop, controls the width of the notch, which is given by $B = 1/8\pi R_Q C_Q$, where B is the width defined by the filter's upper 3-decibel frequency minus its lower 3-dB frequency. Potentiometer R_B is used for balancing the differential amplifier by nulling the 9-kHz feedthrough signal.

When the circuit is in the locked state, the minimum attenuation of the fm signal will be approximately 33 dB for input signals ranging from 540 millivolts to 8 volts peak to peak. Below signal levels of 540 mV, feedthrough from the multiplexer will reduce the attenuation.

Because the filter is a sampling device, it is subject to aliasing if any input-frequency components approach the Nyquist limit of $4f_m$, so that precautions should be taken to prevent this. Spurious output components that are higher harmonics of the 9-kHz fm signal or the clock signal can be removed easily.

Phase jitter in the PLL should also be minimized, for it causes narrow noise sidebands centered about the 9-kHz fm signal and separated from it by a frequency equal to the loop bandwidth of the PLL. The amplitude of these noise sidebands in a properly adjusted circuit should be down at least 33 dB from the level of the fm signals at the input. □

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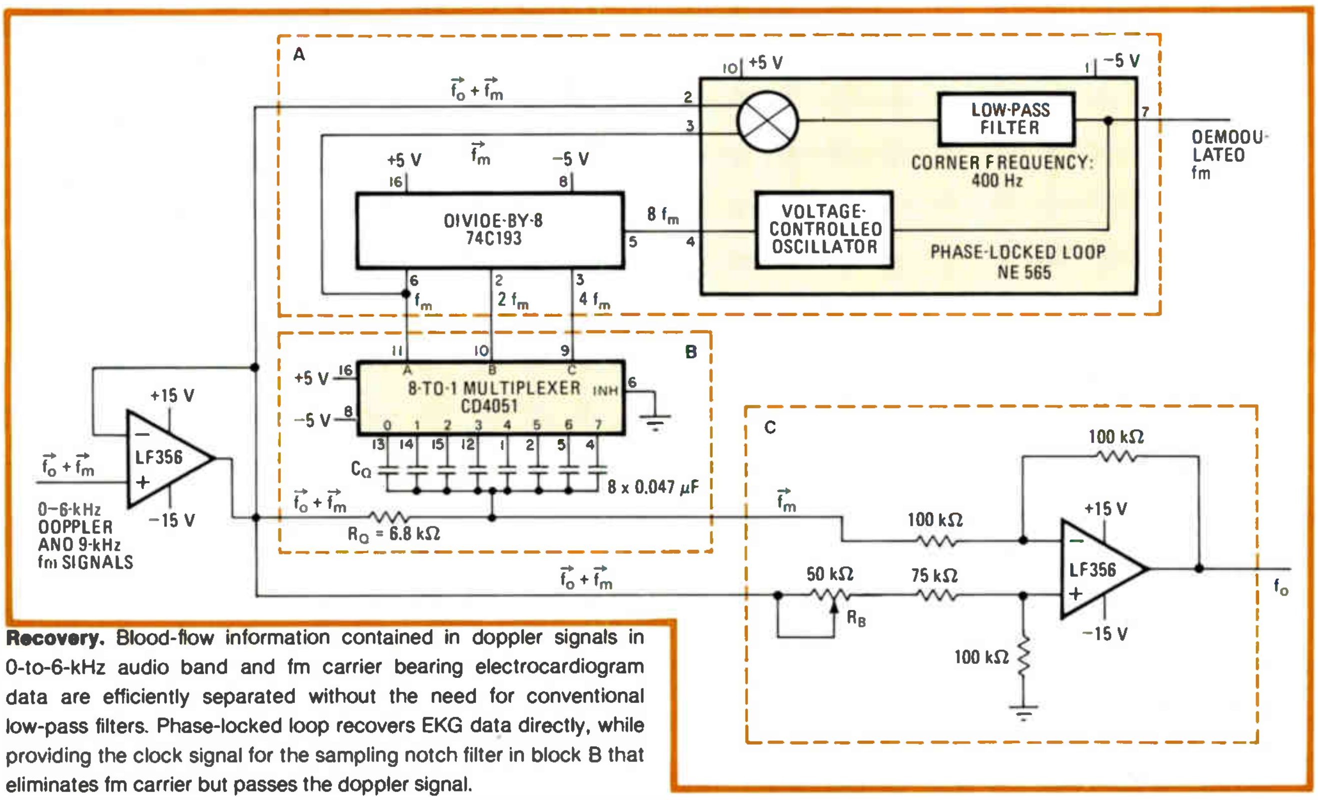


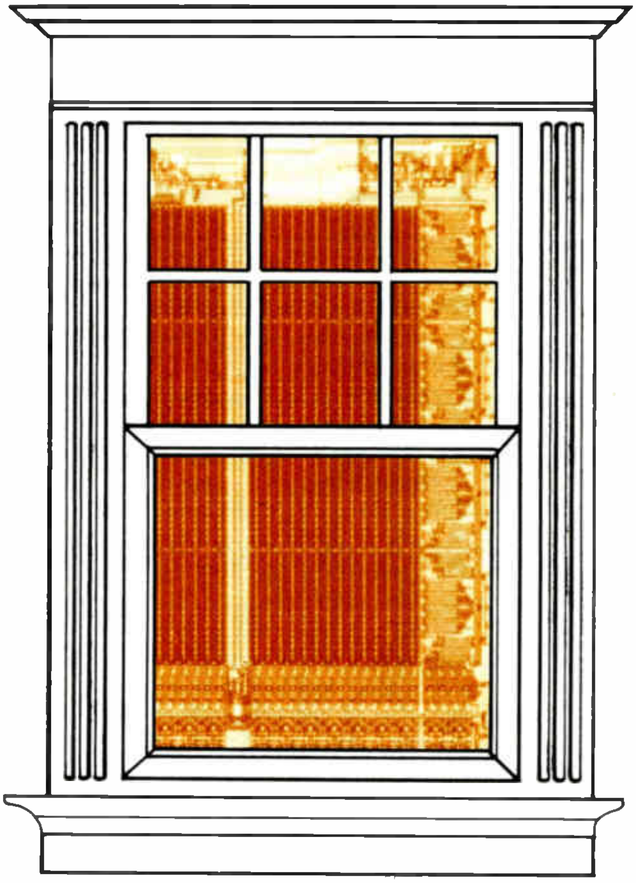
Recovery. Blood-flow information contained in doppler signals in 0-to-6-kHz audio band and fm carrier bearing electrocardiogram data are efficiently separated without the need for conventional low-pass filters. Phase-locked loop recovers EKG data directly, while providing the clock signal for the sampling notch filter in block B that eliminates fm carrier but passes the doppler signal.

The same quartz window that lets in the ultraviolet light for erasure also permits the user to see the actual silicon chip. Maybe this has something to do with the enormous popularity enjoyed by the E-PROM, or erasable programmable read-only memory. But more likely responsible is its attractive combination of field programmability, high density, and low power consumption when compared to bipolar fusible-link memories. Many an E-PROM has been shipped in end equipment because of these desirable features.

The same company that pioneered the E-PROM in the early 1970s wrote this two-part tutorial on its fabrication and reliability. Part 1 reviews the structure of the E-PROM's floating-gate memory cell and the mechanisms of its programming and erasure. As this section notes, electrons accelerated in the channel of the memory transistor gain enough energy during programming to penetrate an oxide dielectric and to cling to a floating gate, made attractive with an overlapping, capacitively coupled control gate. These captive electrons scatter from the floating gate, however, when hit with a flood of UV radiation.

The E-PROM structure and operation give rise to some special reliability considerations (part 2). For example, the oxide insulator surrounding the floating gate must have the integrity to hold charge yet be thin enough to pass electrons and light. Various failure modes of the E-PROM are introduced and discussed in relation to the lifespan of the chip. Specific reliability data is presented for the 16-K 2716 E-PROM, and screening procedures are outlined that can be used to weed out bad devices and estimate total failure rate for each batch.

-John G. Posa



E-PROM reliability: part 1

An E-PROM's integrity starts with its cell structure

A practical understanding of avalanche injection, floating gates, and UV erasure has led to predictable device behavior

by Murray H. Woods, *Intel Corp., Santa Clara, Calif.*

□The ultraviolet-light–erasable programmable read-only memory has matured, and its processing become rather routine. This situation was long in arriving. For years, in fact, the right sequence of fabrication steps was elusive because of the E-PROM's many potential failure modes. Owing to the unique structure of the E-PROM, these afflictions can strike during programming, erasing, or reading.

The E-PROM transistor resembles an ordinary MOS transistor, except for the addition of a floating gate, buried in the insulator between the substrate and the ordinary select-gate electrode (Fig. 1). As a result, in an E-PROM, the select-gate voltage must be capacitively coupled in series with the floating gate rather than directly to the underlying channel. Charge stored on the floating gate alters the threshold voltage of the device as seen by the top or select gate.

Figure 1 also shows why very high densities can be achieved with E-PROM cells: the floating storage gate and the select gate are both directly above the transistor's channel. Even higher densities are obtained by self-aligning these two gates and the source and drain regions. This vertical stacking allows the functions of storage and reading—which normally require separate devices—to reside within the space a single field-effect transistor occupies.

The cell is programmed by charging the floating gate via the injection of so-called hot electrons from the drain's pinch-off region (Fig. 2a). It is erased through internal photoemission from the floating gate to the top gate and substrate. The ultraviolet light gives electrons on the floating gate enough energy to surmount the energy barrier between the floating gate and the insulator surrounding it (Fig. 2b).

The charge on the memory cell's floating storage gate changes the threshold voltage of the select gate by an amount $\Delta V_t = -\Delta Q_{FG}/C$, where C is the capacitance between the floating gate and the select gate and ΔQ_{FG} is the change in charge on the floating gate. The drain current versus select-gate voltage transfer characteristics for the programmed and erased states are parallel to each other (Fig. 3). The select-gate voltage during reading lies between these two curves and results in a drain current that reflects the cell's state, the nonconducting programmed state (storing a 0), or the conducting erased state (storing a 1). When the E-PROM cell is programmed, the negative charge on the floating gate causes the floating-gate-to-source voltage to be negative. This turns the cell off, even with a positive reading voltage applied to the select gate.

Since the floating gate is not tied to a power supply, its voltage is determined by its charge and by capacitive coupling to the voltages of the select gate, the drain, the channel, and the source. The difference between the floating-gate voltage and the voltages of these other cell areas can be used to determine the electric fields in the various oxide regions of the device.

Although the voltage applied to the chip during programming is high—25 volts—the fields across the gate oxide directly above the channel are relatively small, about 2 megavolts per centimeter at the onset of programming and less than 1.5 MV/cm afterward. During all other operations, even when the floating gate is fully charged, this field is $\leq$0.7 MV/cm. This is a typical operating field for a high-performance MOS device.

Programming

The hot electrons get their energy from the voltage applied to the drain of the E-PROM cell. They are accelerated along the channel into the even higher fields surrounding the drain depletion region. While traversing the channel, the electrons enter a region where the electric field in the substrate is about 10^5 V/cm or greater. At this point the rate of energy gained from the electric field can no longer be described by the temperature of the silicon; hence the term "hot." Once these electrons gain sufficient energy they can surmount the energy barrier of about 3.2 electronvolts between the silicon substrate and the silicon dioxide insulator. Because energy loss due to phonon emission increases at higher lattice temperatures, it is actually easier to obtain hot electrons at lower operating temperatures.

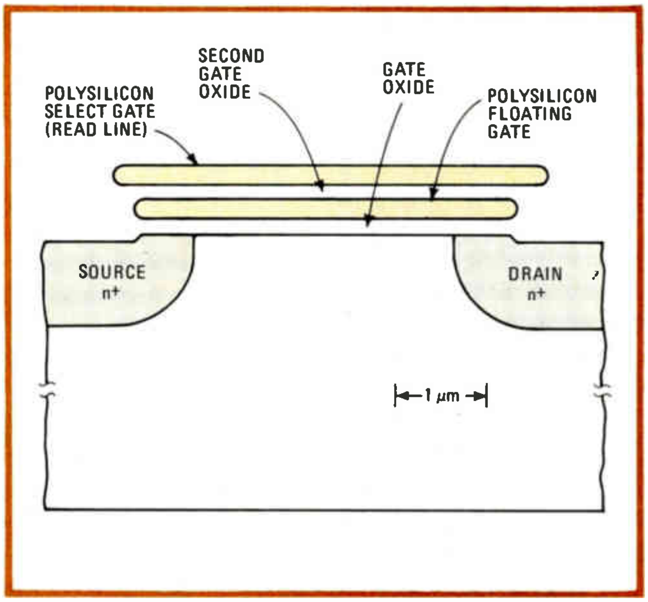
In addition to phonon emisson, hot electrons with energies above about 1.8 eV may give up some of this energy in another way: through electron-hole pair creation resulting from impact ionization. This phenomenon is observed in ordinary MOS transistors as the cause of the onset of substrate current at high drain voltages. However, in the case of the E-PROM, significant current multiplication produces substantial substrate current even before a large enough drain voltage is reached to produce hot-electron injection into the oxide.

With positive drain and channel voltages, electrons injected into the oxide of an n-channel E-PROM return to the substrate unless a high positive select-gate voltage is applied to pull the electrons toward the floating gate. Not only does the floating gate have to be positively biased with respect to the source, it must also be positive with respect to the point along the channel where hot-electron injection occurs.

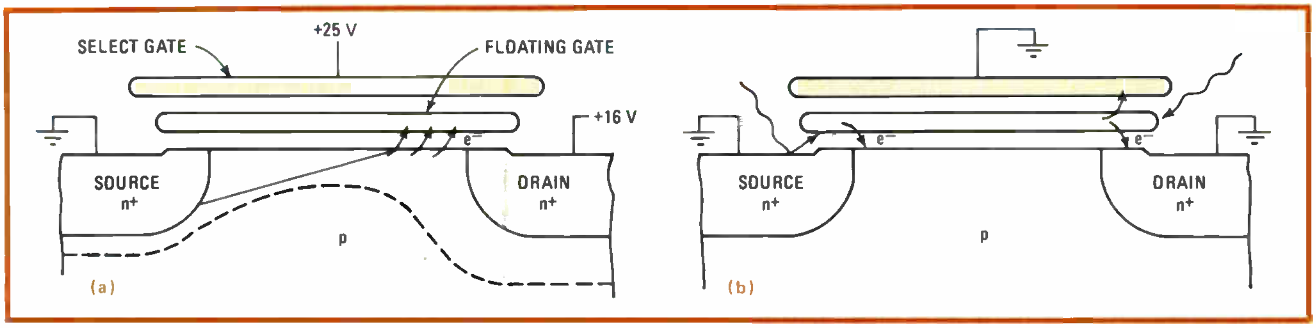
Near the beginning of the injection process, the inversion layer extends almost all the way to the drain, and the field in the oxide is attractive except for a small portion very near the drain (see Fig. 4). Current begins to flow through the oxide at the point where the electrons are their hottest and where the oxide field is most favorable. As the floating gate charges up, the floating-gate-to-source voltage drops and the drain's pinch-off region moves towards the source. The surface field near the drain intensifies and more hot electrons are produced in the substrate.

However, as seen in Fig. 4, in the region where the electrons are their hottest, the oxide field is least favorable for injection and so the injected-electron current begins to subside. Thus, fortunately, the electron injection process is self-limiting. The charging of the floating gate reduces the number of electrons that can be accelerated in the high-field region. As the floating gate becomes fully charged, the oxide current is reduced almost to zero because the oxide field is now repulsive to the electrons injected into the high-field region.

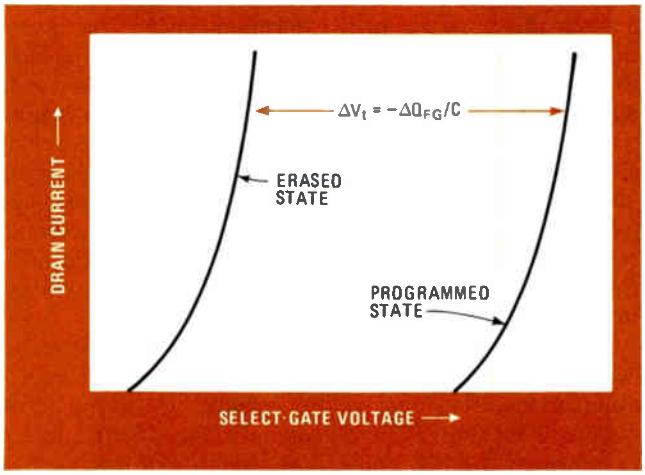
Since the reducing electric field between the floating gate and channel is responsible for shutting off the oxide



1. Vertical. In the erasable programmable read-only memory, a floating storage gate and a select gate are directly above a MOS FET's channel. The floating gate assumes the select-gate potential during writing. The 1-micrometer scale applies to the 2716.



2. To and fro. During programming of the E-PROM cell, electrons are injected onto a floating polysilicon gate (a). During erasure the same electrons receive enough energy from ultraviolet radiation to enter the surrounding silicon dioxide layer (b).



3. Sensible. An E-PROM cell's threshold voltage determines whether it is sensed as a logic 0 (the nonconducting programmed state) or 1 (erased). The change in threshold corresponds to the shift shown in the select-gate voltage to drain current transfer characteristic. This shift depends on the difference in charge on the floating gate in the two states (ΔQ_{FG}), as well as the intergate capacitance (C).

current, the saturated threshold-voltage shift of the floating gate tracks the select-gate voltage during programming on a volt-per-volt basis. The floating gate charges to the same value relative to the source and the channel. An increase in the select-gate voltage during programming merely increases the charge on the floating gate necessary to abort the injection of hot electrons. The drain voltage does not in general have a major effect on the final programmmed voltage of the floating gate. However, it does affect the speed at which the device is programmed, since injection exhibits an exponential dependence on the electric field in the channel.

The reliability of programming

The high-voltage E-PROM programming process is not without its reliability problems. A major concern is electron trapping in the oxide after several programming cycles. Trapped electrons decrease the rate of programming because the electrons that flow through the oxide now encounter locally repulsive fields.

Owing to their small optical cross section, electrons can easily remain trapped in the oxide even after UV erasure of the floating gate. Therefore, as a result of the field around them, trapped electrons also locally raise the threshold voltage of the channel. Indeed, the erased threshold voltage can, through trapping, rise to a point where cell states are sensed incorrectly. This condition is avoided by proper growth of the first gate oxide to reduce the density of electron traps.

Another programming problem may arise when the select-gate voltage is raised high for a device in a row that contains another device that has already been programmed. This produces the highest field in the upper, or second, gate oxide during any time of operation. The average electric field in the second oxide is only about 1 MV/cm, but pointed asperities on the first polysilicon layer can substantially increase the local electric field to the point where partial erasure of the floating gate occurs. This field emission effect can be eliminated by the right combination of process steps, including the temperature used to form the gate structure.

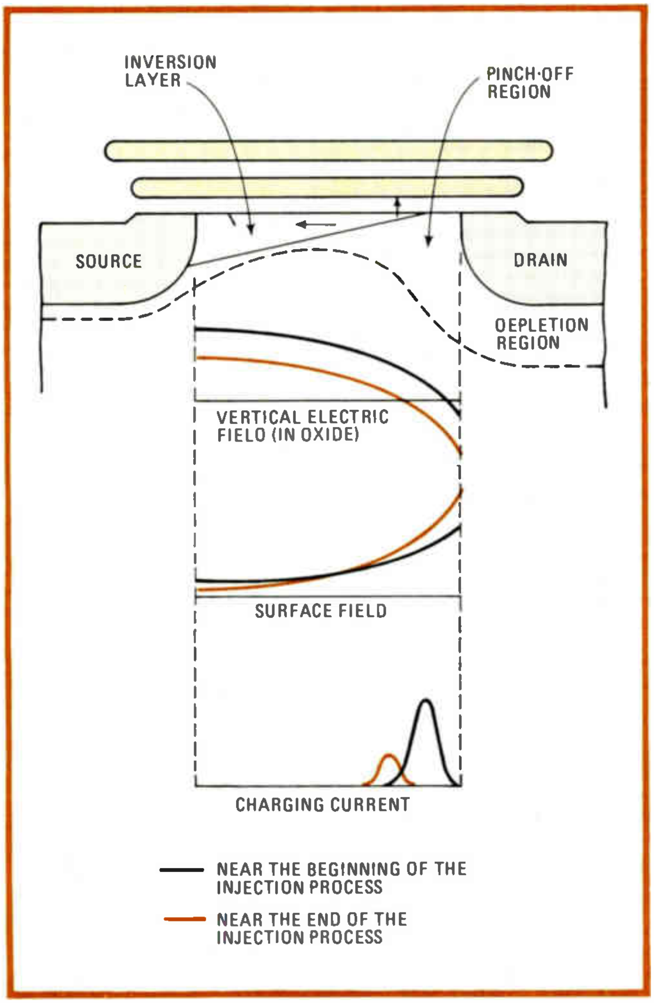
Another case of erasure through field emission may occur when a column is raised high to program a device in another row. The drains of the unselected programmed cells in that column will rise in voltage to create a field of approximately 2.5 MV/cm in the first gate oxide, that between the drain and the floating gate. Fortunately, the bottom of the polysilicon floating gate has a smooth surface so tunneling (Fowler-Nordheim emission) of electrons from the floating gate to the substrate is negligible.

Erase conditions

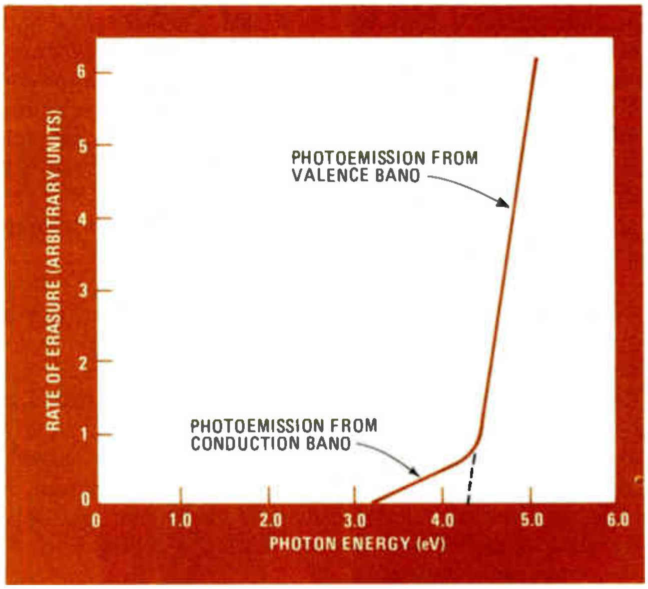
Complete erasure of an E-PROM is required before the device can be reprogrammed. This is accomplished by exposing the entire array to UV light. Typical sources for erasure are quartz-jacketed mercury arc lamps and mercury vapor lamps, which emit strong radiation with a wavelength of 2,537 angstroms (4.9 ev).

The photons are absorbed by electrons in the conduction and valence bands of the polysilicon floating gate; at this wavelength, most are absorbed within 50 Å of the oxide interface. The excited electrons leave the polysilicon floating gate, enter the oxide, and are swept away to the select gate or substrate by the local field. During erasure, the select gate, source, drain, and substrate are all near ground potential.

With an n-type polysilicon floating gate, electrons can be excited from either the conduction band or the valence band into the oxide. Excitation from the conduction band requires only 3.2 ev, while the barrier height from the valence band is 4.3 ev. Even for heavily doped n-type material there are many more electrons available



4. Injection. With a positive floating gate, electrons leave the drain and are accelerated along the channel,. They gain enough energy to hop the thin oxide and cling to the attractive floating gate (as implied by the fields shown). This avalanche injection is self-limiting.



5. Erase rate. Two distinct threshold energies are apparent when erasing an E-PROM cell. The first, at 3.2 eV, corresponds to photoemission from the conduction band of the floating gate. The second point, at 4.3 eV, is associated with the valence band.

from the valence band of the polysilicon floating gate than from the conduction band.

The quantum yield and the erasure rate per incident photon follows the square-law dependence upon photon energy shown in Fig. 5. Two distinct threshold energies are apparent. The first, at 3.2 ev, is associated with the photo-excitation of electrons from the conduction band. Its slope is much shallower because of the lower density of electrons. The 4.3-eV threshold corresponds to the onset of photoemission from the valence band. The much steeper slope is indicative of the much higher density of valence-band electrons.

Unlike earlier p-type floating-gate E-PROMs, the fact that there is a significant density of electrons on the floating gate introduces the potential reliability problem of spurious erasure. Even with atmospheric filtering, sunlight photons having energies as high as 4.1 ev can reach the earth's surface. Also, fluorescent and incandescent lamps emit a minimum wavelength of about 3,000 Å, which corresponds to 4.1 ev. Erasure rates in sunlight or normal room light are much slower—1,000 times or more—than erasure under intense UV exposure because of the lower intensity of illumination and low density of electrons in the conduction band of the floating gate. However, care must still be taken so that programmed E-PROMs are not subjected to prolonged exposure from either sunlight or ordinary room lighting.

Ultraviolet rays are so strongly absorbed that they do not get past the top select gate and the photons can only make their way to the floating gate from the side. In modern self-aligned structures, the edge of the floating gate is directly exposed to the radiation. But in earlier n-channel structures in which the floating gate completely overlaps the select gate, erasure is accomplished as the photons travel through the field oxide, under the select gate, and to the floating gate where they are absorbed. This wave-guiding effect is efficient because the reflectivity of silicon to 2,500-Å light is roughly 65%.

An interesting exception exists for very energetic X rays and gamma rays, which can readily penetrate the select gate and then be absorbed throughout the gate oxides, the floating gate, or the substrate. However, a broadband flux on the order of 10^{13} photons per cm from an X-ray tube operated at 100 kiloelectronvolts with a tungsten target is necessary to fully erase an E-PROM; hence X rays are not regarded as a special reliability concern for E-PROMs.

Finally, single ionizing events due to the passage of a cosmic ray or an alpha particle cannot cause spurious erasure because not enough charge is created in the gate oxides around the floating gate to neutralize the charge stored there.

Reading and storage

During reading, the E-PROM cell operates like an ordinary transistor except that the normal gate capacitance is replaced by the series capacitance of the floating-gate structure. Though it might be suspected that some low-level programming could occur during a read operation, as read voltages are applied to both the gate and drain, this has not been observed. One reason is that hot-electron current is an exponential function of drain voltage and the drain voltage used for reading (approximately 3 V) is much lower than that used for programming (over 20 V). In addition, the requirement for electric fields greater than 10^5 V/cm to generate hot electrons—and an energy barrier of greater than 3 eV for injection into the oxide—make spurious programming nonexistent at normal reading voltages.

The key issue for nonvolatile memories is just how well they retain their data. For E-PROM, the answer hinges on how well the charge on the floating gate stays put over the lifetime of the part. The advantage of floating-gate memories is that the gates are surrounded by high-integrity silicon dioxide. This oxide is a nearly ideal insulator because it has a wide bandgap, a very high barrier with reference to silicon and aluminum, a relatively low surface-state density on silicon, low bulk trapping densities and electron trapping levels, and no structural polarization.

For ordinary electric fields from the floating gate to the select gate and substrate encountered during reading and storage, electron emission is negligible. Therefore any charge leakage that occurs must be due to oxide defects. Since this leakage is due to a thermally activated hopping mechanism having an activation energy of 0.6 eV[1], its rate can be accelerated under high-temperature biasing and/or baking conditions. For example, programming all bits and then subjecting the device to a high temperature (150°C) rapidly determines the ability of each floating gate to maintain charge. Additionally, a high-temperature biasing of unprogrammed bits screens out oxide defects that cause current leakage to the floating gate.

By taking advantage of these high-temperature and/or voltage accelerating factors, production screens have been developed that successfully weed out those parts with defective oxides. These screens are the subject of part 2 of this article. □

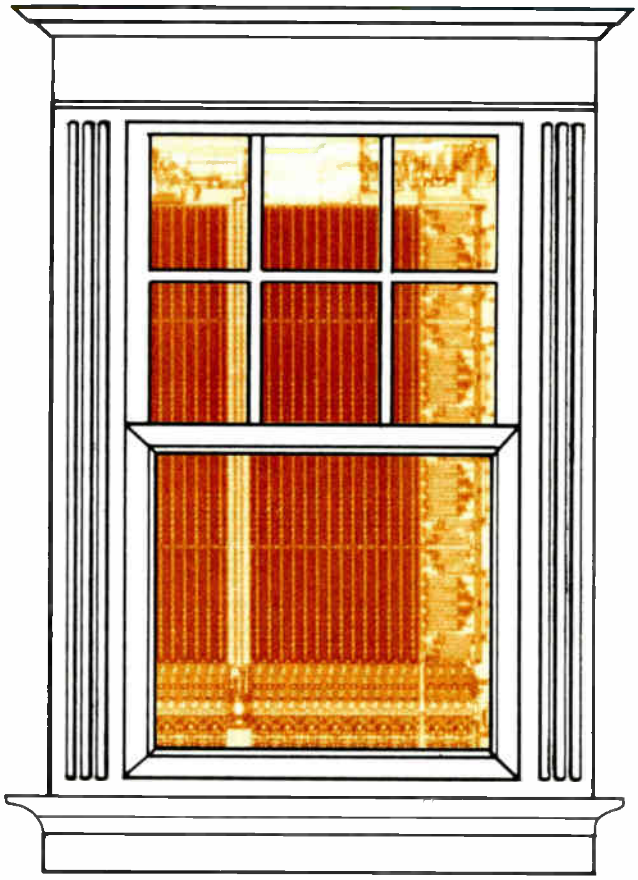
References

1. R. E. Shiner, J. M. Caywood, and B. L. Euzent, "Data Rentention in E-PROMs," 18th Annual Proceedings, Reliability Physics Symposium (1980).

E-PROM reliability: part 2

Tests and screens weed out failures, project rates of reliability

by Stuart Rosenberg, *Intel Corp., Phoenix, Ariz.*



□ To determine the failure rate of a group of erasable programmable read-only memories—or any integrated circuit, for that matter—various short cuts must be employed or the testing time would become intolerable. Some E-PROM failure modes only occur after the device has been working properly for years (proper operation of an E-PROM is described in part 1 of this article). Obviously, production testing cannot afford this kind of time, so the aging process is accelerated with high temperatures and extreme supply voltages. This form of testing, called screening, will both pinpoint bad chips and help determine the overall failure rate that can be expected for a batch of devices.

The purpose of reliability testing is to quantify the expected failure rate of a device at various points in its life. Fundamental principles of reliability engineering predict that the failure rate for a group of devices will follow the bathtub-shaped curve depicted in Fig. 1. This curve is divided into three regions: infant mortality, random failures, and wear-out failures. All classes of failure mechanism can be assigned to one or more of these regions.

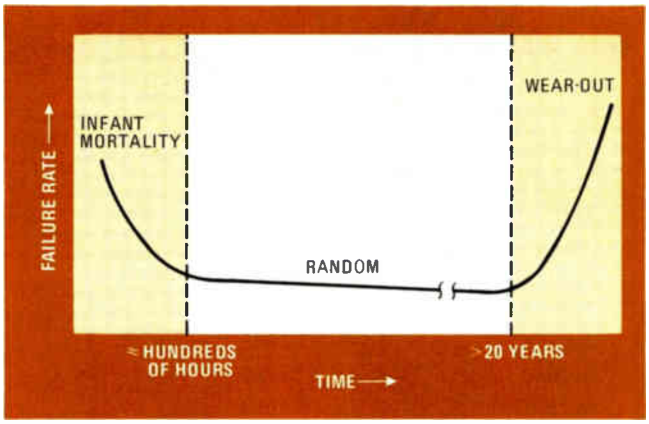
Infant mortality, as the name implies, represents the earliest failures in a device's life and is usually associated with one or more manufacturing defects. After a time, usually in the high tens to low hundreds of hours, the failure rate approaches a constant low value where it remains for a period of hundreds of thousands to millions of hours (for integrated circuits), depending upon temperature, applied voltages, and other operational and environmental factors.

This random-failure region of the curve represents the useful life of the device. During this period there is a slight decline in the failure rate as potential random failures are weeded from the general population. Wear-out failures are characterized by a rapidly rising failure rate with time as the devices wear out both physically and electrically.

Characterizing a given device type in the shortest possible time requires tests that simulate accelerated aging. To choose the right acceleration factor, it is first necessary to understand what makes E-PROMs fail in each region of Fig. 1.

Table 1 lists the common failure mechanisms for n-channel MOS E-PROMs. The table also shows the region of the bathtub curve most affected by each mechanism, as well as the thermal activation energy (E_a) of the mechanism. The thermal activation energy indicates the effect that increased temperature has on the frequency of the failure; the higher the activation energy, the greater the effect. For example, a temperature rise from 70°C to 125°C increases the failure rate resulting from oxide-hopping conduction (E_a = 0.6 electronvolt) by a factor of 16.5. This same temperature rise causes oxide rupture failures (E_a = 0.3 eV) to increase by only a factor of 6.

A detailed explanation of each mechanism is beyond the scope of this article, but charge loss, oxide-hopping conduction, and hot-electron injection are responsible for the majority of failures. A buildup of electrons trapped in the oxide layer mentioned in part 1 commonly causes devices to wear out.



1. Failure tub. The reliability of an integrated circuit follows a bathtub-shaped curve. Infant failures happen right after the chip is made. Wear-out failures do not start until after 20 years, a time span representing the useful life of the device.

Charge loss from the floating gate is due to thermal emission. It affects most E-PROM cells to some degree over their 20-year life, and typically amounts to less than 10% of the charge stored on a cell.

Failure modes

Oxide-hopping conduction between the floating gate and the silicon substrate is typically less than 10^{-19} ampere, or about one electron per second. The electrons flow onto or off the floating gate depending on bias conditions, so they may cause bit errors on either stored 0s or 1s. Oxide-hopping conduction is related to manufacturing defects and does not occur in most devices. Thus, this failure mechanism affects the random and infant portions of the bathtub curve most strongly.

Undesirable hot-electron injection occurs when an MOS transistor is in saturation. Accelerated electrons in the pinch-off region may be scattered or attracted because the gate field is perpendicular to the silicon-oxide interface.

As covered in part 1 of this article, cell programming

TABLE 1: E-PROM FAILURE MECHANISMS

Mode	Lifetime region affected (in Fig. 1)	Thermal activation energy (eV)	Primary detection method
Slow trapping	wear-out	1.0	high-temperature bias
Surface charge	wear-out	0.5–1.0	high-temperature bias
Contamination	infant/wear-out	1.0–1.4	high-temperature bias
Polarization	wear-out	1.0	high-temperature bias
Electromigration	wear-out	1.0	high-temperature operating life
Microcracks	random	–	temperature cycling
Contacts	wear-out/infant	–	high-temperature operating life
Silicon defects	infant/random	0.3	high-temperature operating life
Oxide breakdown/leakage	infant/random	0.3	high-temperature operating life
Hot-electron injection	wear-out	–	low-temperature operating life
Fabrication defects	infant	–	high-temperature burn-in
Charge loss	infant/random/wear-out	1.4	high-temperature storage
Oxide-hopping conduction	infant/random	0.6	high-temperature storage/burn-in

TABLE 2: INFANT MORTALITY EVALUATION FOR THE 2716

Month (1979)		Burn-in results (number failed/number stressed)
January		3/1956
February		2/964
March		6/4085
April		4/3813
May		9/3602
June		7/3822
July		9/2995
August		7/3055
September		3/1893
October		8/5025
November		2/1726
December		13/3321
	Total	73/36,257 = 0.2% failure rate

Failure analysis:
- 33 charge-lose failures
- 34 charge-gain failures
- 3 decoder failures due to oxide breakdown
- 2 ac failures from slow trapping or contamination
- 1 dc parametric failure from contamination

TABLE 3: 2716 DYNAMIC LIFE TEST DATA AND RANDOM-FAILURE RATE EVALUATION

Month started	Results at 125°C		
	168 hours	500 hours	1,000 hours
Before 5/79	5/3983	7/3874	3/3969
5/79	0/128	1/128	1/127
6/79	0/128	2/128	0/126
6/79	0/286	0/286	0/286
6/79	0/29	0/29	0/29
6/79	0/299	0/299	0/299
7/79	0/192	0/192	0/192
8/79	0/64	0/64	0/64
8/79	0/99	0/99	0/99
8/79	0/102	0/102	0/102
8/79	0/102	0/102	0/102
8/79	0/100	0/100	0/100
8/79	0/100	0/100	0/100
8/79	0/128	0/128	0/128
9/79	0/64	1/64	0/63
10/79	0/75	0/75	0/75
10/79	0/31	0/31	0/31
Cumulative	5/5894 (A)	12/5065 (B)	6/5055 (C)

FAILURE ANALYSIS

(A) 5 single-bit hopping conduction (0.6 eV)

(B) 11 single-bit hopping conduction (0.6 eV)
1 double-bit charge retention (0.6 eV)

(C) 5 single-bit hopping conduction (0.6 eV)
1 single-bit fabrication defect (0.3 eV)

FAILURE RATE CALCULATION

Failure-mode activation energy (eV)	Actual device-hours at 125°C	Equivalent device-hours at 55°C	Number of failures	Failure rate at 60% confidence level (% per 1,000 hours)
0.3	5.2×10^6	2.7×10^7	1	0.007
0.6	5.2×10^6	2.2×10^8	22	0.011

Total failure rate: 0.018% per 1,000 hours

of an E-PROM is accomplished through hot-electron injection. During a programming cycle, as electrons travel to the floating gate, a small percentage of these carriers may become trapped in the thin gate oxide. Since ultraviolet radiation is relatively ineffective at removing these trapped electrons during erasure, repeated programming and erase cycles may result in a build-up of charge. These trapped electrons may, in turn, cause significant degradation in the operating margins of the device and, ultimately, device wear-out.

Measuring mortality

To measure the infant-mortality failure rate, a 48-hour dynamic burn-in at 125°C is used. Depending on the failure mechanism, the test correlates with 240 to 2,000 hours of operation at 55°C. To perform such a test, E-PROM samples are gathered on a weekly basis, programmed with a checkerboard pattern, and burned in. Results of infant mortality tests done on the Intel 2716 E-PROM for 1979 are shown in Table 2. The data reveals an average infant-mortality failure rate of 0.2% for the year, with failures heavily dominated by hopping conduction (67 of a total of 73 failures).

To best characterize the random portion of the bathtub curve, burned-in E-PROMs that no longer exhibit infant mortality are used. Long-term failures are measured with 1,000-hour 125°C life tests; results for the 2716 are shown in Table 3, along with the failure analysis. There were 23 failures in 5.2×10^6 device hours for a failure rate of 0.4% per 1,000 hours at 125°C.

With more than one failure mode, and with different thermal activation energies, the effect of operation at 125°C varies for different devices. It should also be pointed out that since failures occur at the die level, any extrapolations must be made from junction, and not ambient, temperatures. Thus a 125°C to 55°C ambient derating corresponds to a derating of junction temperatures from 130°C to 65°C for a 2716.

Although there are many ways to compute a 55°C failure rate, only one is realistic: by simply calculating the rate due to each mechanism and then adding them up. In another method, one that yields overly optimistic results, a single thermal activation energy is chosen to represent all failures in the population. A common choice is 0.7 eV since this value is used in military testing procedures. Based upon the number of device-hours in Table 3 (5.2×10^6) and this activation energy, the acceleration factor from 130° to 65°C corresponds to 48:1. This acceleration factor was read off an Arrhenius plot (Fig. 2).

For this scheme the equivalent number of device hours at 55°C works out to 2.5×10^8. At a 60% confidence level with the tabulated number of failures (23), the 55°C failure rate becomes 0.01% per 1,000 hours. The pitfall of this method is that the acceleration factor is determined independently of the failure types and their corresponding activation energies. Unless all the failures are

0.7 eV, which is not generally the case, the extrapolation has little meaning.

Accurate results are given at the bottom of Table 3, where a 55°C failure rate of 0.018% for 1,000 hours is calculated. The first method's failure rate, 0.01%, is two times too optimistic.

Testing for wear-out

There are two failure mechanisms by which E-PROMs wear out that significantly affect reliability. These are charge loss and stress from program-erase cycling.

Since charge loss has a high thermal activation energy (1.4 eV), a test involving storage at a very high temperature (250°C) can determine where on the bathtub curve devices begin to wear out. So units with a high percentage of programmed bits (typically more than 90%) are placed in storage at 250°C for up to 1,000 hours. Intermediate data is taken to determine the shape of the failure-rate curve.

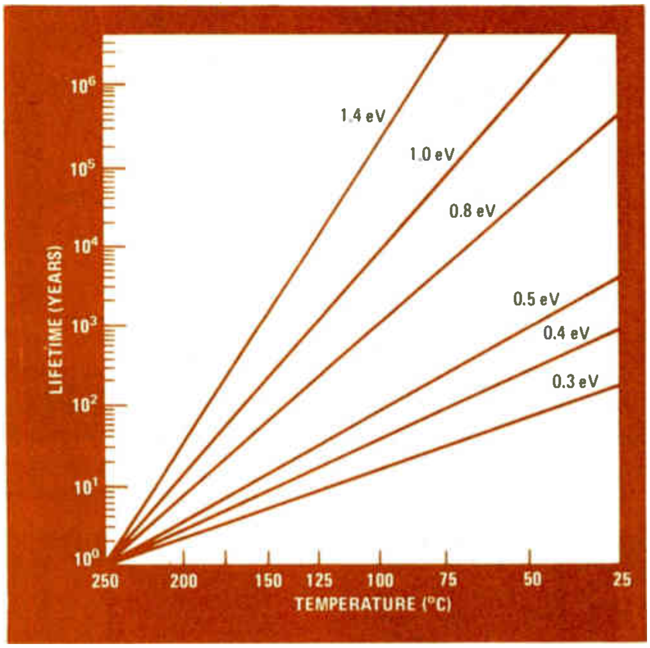
Figure 3 illustrates the cumulative percentage of failures versus time for the 2716 after a storage test at 250°C. This graph is based on data from more than 1,000 units, taken over a period of more than six months. This curve shows no sign of an increase in failure rate, indicating that the failures are defect-related and symptomatic of the infant and random failure regions. No indication of wear-out resulting from intrinsic charge loss is seen at 1,000 hours at 250°C. This corresponds to 1,950 years at 125°C or 1.3 million years at 70°C.

To evaluate the effect of program-erase cycling on device wear-out, supply voltage maximum and minimum measurements (V_{CCmax} and V_{CCmin}, respectively) are made after subjecting an E-PROM to multiple programming and erasing cycles. V_{CCmax} is the greatest supply voltage that will support proper operation, and V_{CCmin} is the lowest value. Each cycle comprises programming of the E-PROM with more than 90% 0s; measuring V_{CCmax}; erasure via UV light with an intensity of 10 watt-seconds/square centimeter; programming to a pattern with more than 90% 1s; measuring V_{CCmin}; and erasure.

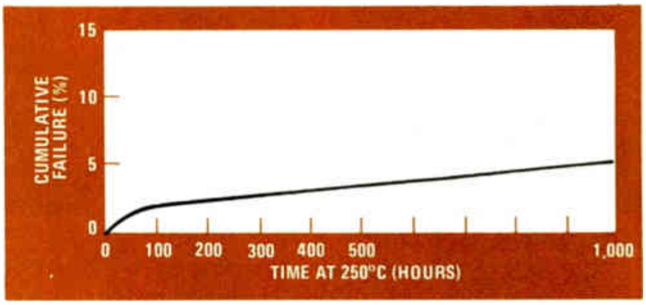
The results of 225 program-erase cycles on 48 2716s showed only one failure, which occurred after 56 cycles. The cause of the failure was determined to be partial oxide breakdown due to high field stressing during programming. Figures 4a and 4b show the 10%, 50%, and 90% points for program and erase margins (the cell's threshold voltage after programming and erasing) versus the number of program and erase cycles for the remainder of the sample. No appreciable shift can be seen in either the program or the erase margin and, for the 2716, degradation of operating margins due to hot electron injection did not occur.

Achieving acceptable reliability

To produce reliable E-PROMs, it is necessary to know the types of failures that may afflict the device and then devise tests to weed out those parts with latent defects. These tests are called failure-mode screens because they are effective only on those E-PROMs with latent defects due to a particular failure mechamism or mode. Figure 1 shows that infant mortality and wear-out failures each have an order of magnitude greater effect on reliability



2. After Arrhenius. The Arrhenius plot shows the extent that an increase in temperature will accelerate a failure mechanism. Using the thermal activation energy for the failure mode of interest—see Table 1—a device's life is deduced from a temperature differential.

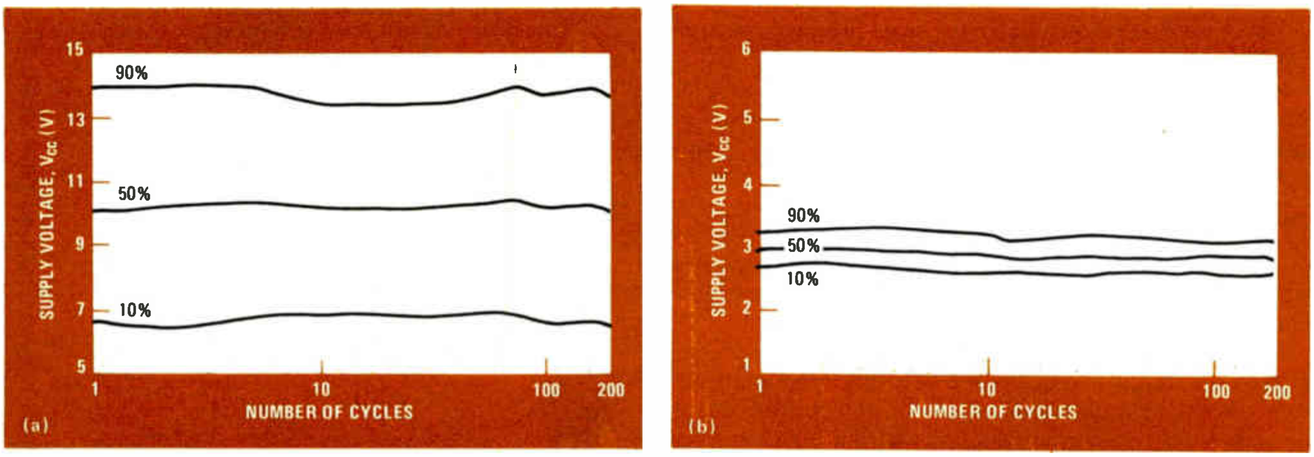


3. In sum. The cumulative percentage of failures is charted against time after storage tests done at 70°, 100°, and 250°C. The data was gathered from more than 1,000 units over a period of more than six months. Charge loss is not seen for an extended period of time.

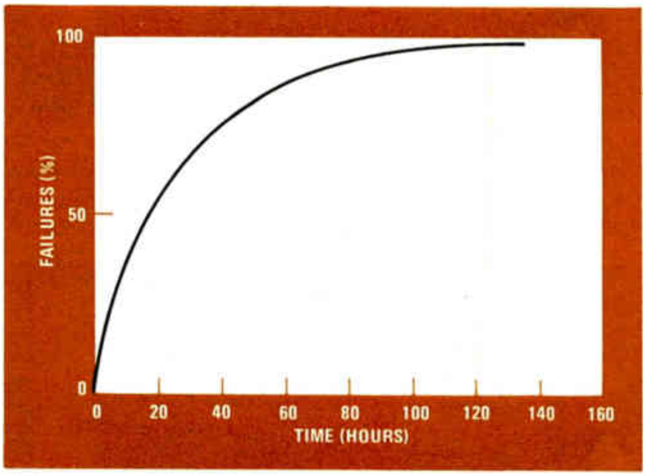
than do random failures. For this reason, failure-mode screens are designed to isolate mechanisms that strike in these two regions of the bathtub curve.

Screens are also region-specific, so two different screens are needed to reduce failures during both the infant mortality and wear-out periods. Although the infant-mortality screen does not lower the random-failure rate, it does reduce the cumulative failure rate, thereby improving overall reliability.

Infant-mortality screens reduce a population's early-life failure rate by prematurely aging each part just beyond the first change in slope of the bathtub curve. If the manufacturer can eliminate most parts with latent defects before they leave the factory, the balance of each shipment should be error-free until the parts begin to wear out. Wear-out screens attempt to extend the random-failure portion of the curve further to the right, extending useful device life. Infant-mortality screens have a negligible impact on the wear-out failure rate because of the relative time scales; premature aging of a



4. Good margins. To evaluate the effect of program-erase cycling on wear-out, a V_{CCmax} test is done after multiple programming cycles (a), and a V_{CCmin} test is done after numerous erasures. The near-horizontal lines indicate no degradation in program or erase margins.



5. Charge-loss screen. A lot of 10,000 2716s was screened for 72 hours at 150°C, then burned in for 48 hours to check for charge-loss failures. The optimum duration for such a screen corresponds to the curve's leveling out; this happens after 72 hours.

part—even by two months—means little after 20 years.

When faced with a raw population of E-PROMs whose reliability is to be improved by screening, the first step is thorough reliability life testing, followed by a detailed analysis of the failures. Once the dominant failure mechanisms have been identified and a failure rate computed, the number of screens and their types must be settled on.

Avoiding screen overkill

Screens cost money, though, because of the time and equipment needed to implement them. Overkill is a measure of the number of parts that fail a screen but that would never have failed in the field. A good screen has little overkill yet still lowers the failure rate. Ideally, screens should be part of a normal test program and should take less than a second to perform. A screen may be put into production to combat a new failure mode with little regard to overkill or complexity. Once the failure rate is under control, the screen can be modified to optimize its cost with respect to its effectiveness in improving reliability.

Two infant-mortality screens—one for defect-related charge loss and another for charge gain (both are manifestations of oxide-hopping conduction)—were developed for the 2716. The combined objective of those screens was to reduce the total early-life failure rate to less than 0.2% of the population. To measure the effectiveness of the screens, it was decided to follow each with a dynamic burn-in at 125°C for 48 hours—a typical infant-mortality period.

Charge-loss screen

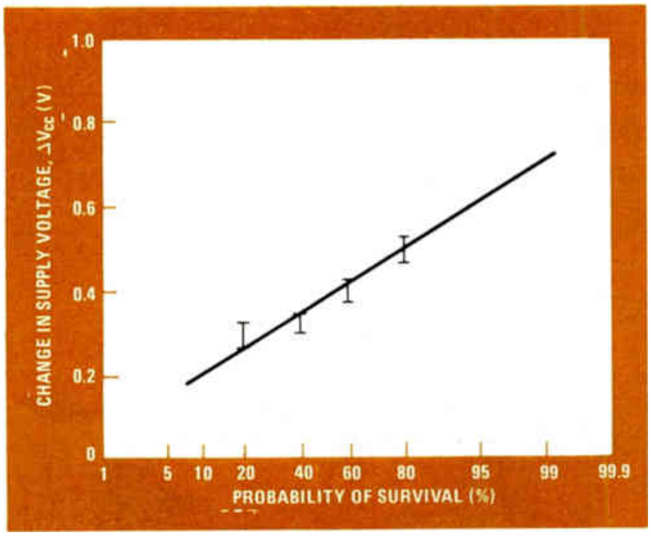
The charge-loss screen was devised only after an analysis of indicators of latent manufacturing defects, as these are most responsible for charge-loss failures. Though indicative of the number of electrons on the floating gate, ease of programming and erasure and programming margin were evaluated—but without success, in this case.

The next step was to examine the effect on charge loss of bias voltage and temperature. Earlier work with E-PROMs showed charge loss to be more than two orders of magnitude greater at 150°C than at 55°C, so a high-temperature bake was selected as the basic screen. To determine whether bias voltage affected the charge loss, programmed cells with and without bias were compared, but found to be similar. Therefore, it was decided to make the screen an unbiased high-temperature bake, for reasons of simplicity.

The final step was to determine how high in temperature and how long in duration the screen should be. Since it was intended for production runs of 2716s in tin-plated ceramic packages, temperatures were limited to 150°C to prevent severe lead oxidation. To determine the optimum bake time, the screen was applied to known charge-loss rejects with pass/fail tests every 20 hours. The results (Fig. 5) indicate that about 72 hours would be sufficient to weed out the majority of charge-loss rejects.

To confirm this time estimate, a 10,000-piece lot of 2716s was first screened for 72 hours at 150°C and then dynamically burned in for 48 hours. Approximately 0.1% of the parts that passed the charge-loss screen failed the burn-in. This percentage of charge-loss failures compared favorably with an overall infant-mortality failure rate of 0.27%.

Unlike charge loss, a well-known failure mechanism in



6. Wear-out. Wear-out screening should guarantee at least 99% of all parts will not fail during a specified lifetime. Both elevated temperature and maximum V_{CC} were used to screen for charge-loss wear-out. For a 1% failure rate, V_{CC} had to be increased 0.7 V.

TABLE 4: RESULTS OF DATA-RETENTION MONITOR			
Month	Number of devices	Data-retention failures	% fail
1/78	293	14	4.7%
2/78	200	0	0%
3/78	300	4	1.3%
4/78	100	3	3.0%
5/78	300	1	0.3%
7/78	165	1	0.6%
8/78	260	3	1.1%
9/78	323	11	3.4%
10/78	176	4	2.2%
11/78	323	11	3.4%
12/78	535	9	1.6%
This test was run for 168 hours at 250°C			

older designs, charge gain seemed unique to advanced E-PROMs. Earlier work at Intel hinted at a relationship between supply voltage and charge gain, so a biased, dynamic burn-in for 48 hours at 125°C became the first screen attempted.

The temperature was later raised to 150°C when it was decided to run the screen on 2716s in their power-down mode. During power-down, all select gates are driven to V_{CC} and are stressed more effectively. By running the screen in power-down, the burn-in temperature could be safely raised to 150°C.

The supply voltage was the final parameter to be determined. Since the failure rate increases linearly with the stress voltage for charge gain, a V_{CC} level greater than 5 volts was desirable for the screens. But a conflict arose because the power-down mode at an elevated V_{CC} supply is also the programming mode. Fortunately, computer simulations of the 2716 revealed that 7.5 V could be used without going into the programing mode. Because of the increased voltage, temperature (150°C), and duty cycle, the screening time was reduced to six hours. The final result: a charge-gain screen done at 150°C for six hours at 7.5 V in the power-down mode.

With screens devised for both charge gain and charge loss, data was collected and measured against the 0.2% infant-mortality goal. Samples pulled weekly from an inventory awaiting shipment were subjected to a dynamic 48-hour burn-in at 125°C. Results for 1979 showed 72 failures out of 35,783 units stressed, or an infant mortality rate of 0.2%.

Wear-out can have a dramatic impact on reliability if it occurs in an operating piece of equipment. To minimize wear-out resulting from intrinsic charge loss, another type of screen was called for. As opposed to infant-mortality screening—where a small freak population must be eliminated—wear-out screening should insure that at least 99% of all parts will not fail during a specified lifetime.

It was known that temperature aggravates charge loss and that no external bias is necessary to induce charge loss in programmed cells. A good method for identifying charge-loss wear-out was found to be a 168-hour bake at 250°C. Using known acceleration factors from Arrhenius plots, this correlates with more than 220,000 years at 70°C. The acceptable percentage of failures for this test is 5%, which corresponds with 2×10^{-4}% failures due to charge loss in 10 years. If this rate is not exceeded, then wear-out has not yet begun.

Monitoring margins

Through the logging of cell programming margins (based on V_{CCmax}) at the beginning and end of the 168-hour bake at 250°C, an average degradation was determined. This was fed into the standard manufacturing test sequence—where cell programmability is checked—to insure that all parts have sufficient margin to weather a normal lifetime.

To determine a value for V_{CCmax}, experiments were conducted to discover the change in V_{CCmax} for 99% of the 2716s tested. Although the target for failures was 5%, a 1% ceiling was considered more appropriate to account for normal statistical variations in the small 50-piece sample.

The changes in V_{CCmax} for the 168-hour 250°C bake are plotted in Fig. 6 against the probability of seeing a given change in V_{CC}. From this plot, a ΔV_{CC} of 0.7 V corresponds to the 99% pass criterion. Thus, to insure that all 2716s have sufficient margin to withstand normal life, the standard manufacturing testing sequence includes a test with ΔV_{CC} set to +0.7 V.

By incorporating the screen in the normal product flow there is a minimum of disruption and no increase in testing time (the screen takes less than 1 millisecond to perform). The final test of this wear-out screen is its effectiveness. Results through the first 11 months of 1979 pinpointed 100 failures in 3,800 devices stressed. This works out to a failure rate of 2.5%, well below the target of 5% (see Table 4). □

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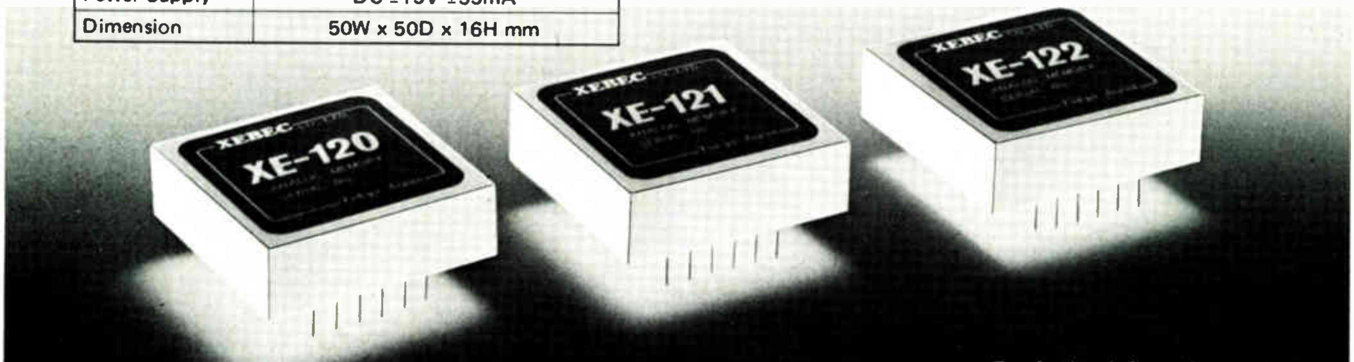

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Based on one-chip-microcomputer architecture, universal peripheral controller comes with either multiplexed or nonmultiplexed address and data lines, provides ROM-less and prototyping packages for product development

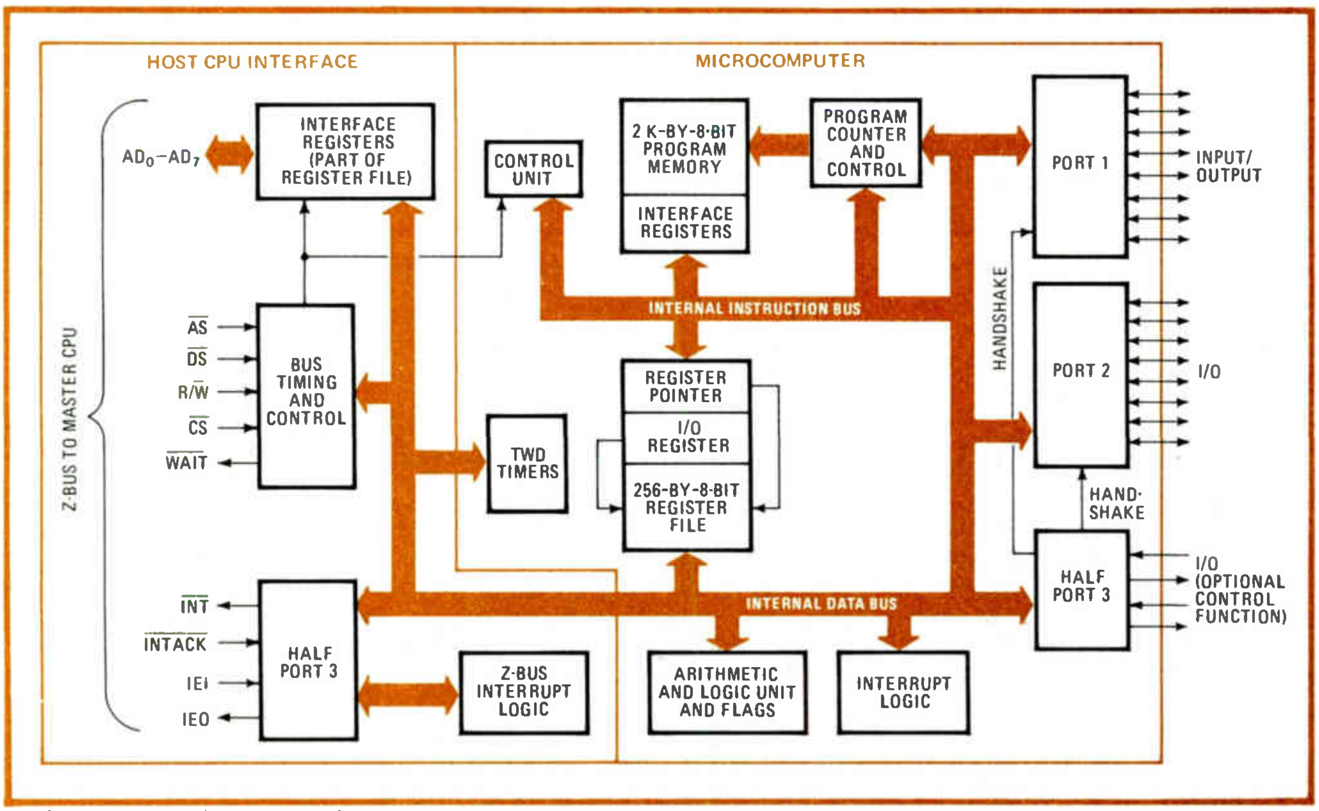
by John Banning and Pat Lin, *Zilog Inc., Cupertino, Calif.*

□ The growing power of high-end microprocessors and the complexity of peripheral devices attached to them has given rise to a need for general-purpose distributed processors to handle increasingly complicated input/output activities. As such, these devices must themselves have respectable processing and I/O-manipulation abilities while being able to interact efficiently with high-end microprocessors. Ideally, they would also communicate with 8-bit midrange microprocessors and be low in cost.

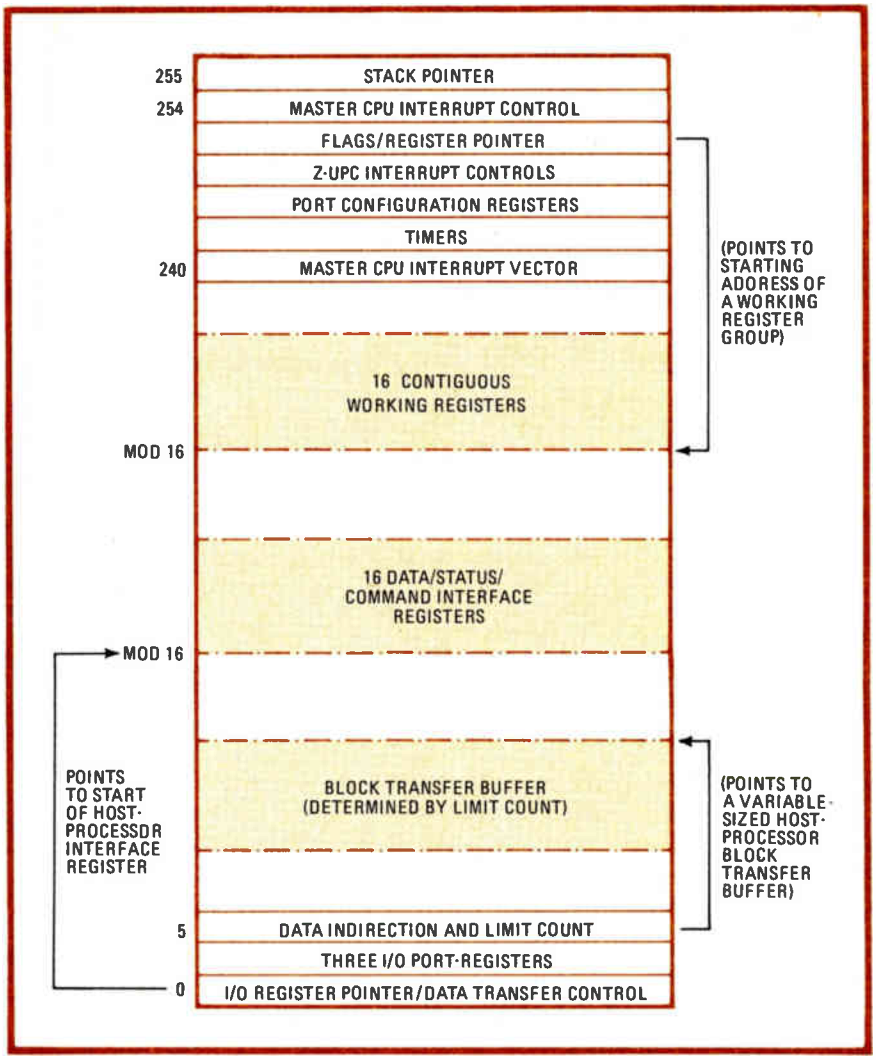
Just such a processor has been based on the Z8 single-chip microcomputer. The Z-UPC universal peripheral controller combines the instruction and I/O capability of the Z8 with two versions of bus interfacing: the Z-UPC offers the Z-BUS interface found on the Z8000, and the Z-UPC/U provides a Z80-compatible interface. The Z-BUS interface allows flexible connection to larger microprocessor systems and control of distributed I/O peripheral functions by means of a multiplexed address and data bus. The Z80-bus interface provides easy interfacing with 8-bit microprocessors and others that employ nonmultiplexed address and data buses.

A logical organization

The UPC is partitioned into two functional blocks: the logic for interfacing with the host-processors, and the core microcomputer (Fig. 1). In the multiplexed (Z-BUS) version, communication between the host and the UPC takes place over the Z-BUS, which provides an 8-bit bidirectional address and data port (AD_0–AD_7) and a set of control lines ($\overline{AS}$, $\overline{DS}$, $R/\overline{W}$, $\overline{CS}$, $\overline{WAIT}$). Also, under UPC program control, an optional daisy-chain interrupt structure—using request ($\overline{INT}$), acknowledge ($\overline{INTACK}$),



1. Microcomputer plus. The Z-UPC universal peripheral controller bases much of its architecture on the Z8 chip, to which it adds circuits at left for interfacing with a host processor. Shown is the Z-BUS–compatible version with multiplexed address and data lines.



2. File in. Of the UPC's 256-byte register file, 234 are general-purpose and can function as accumulators, buffers, pointers, or stack or index registers. The other 22 are specific pointers and registers, as well as status and control registers for the UPC's I/O facilities.

enable input (IEI), and enable output (IEO) lines—can be implemented. The microcomputer portion is based on the Z8 microcomputer architecture, whose central processing unit executes instructions averaging 2.2 microseconds each using a 4-megahertz clock source. The CPU's memory comprises 256 bytes of register-file random-access memory (which can be accessed directly by the host processor and the UPC), plus 2,048 bytes of read-only memory for program storage; other features include three I/O ports for device control, two timer/counters, and six vectored interrupts.

In addition to the standard 40-pin version (with 2-K bytes of ROM), there are two 64-pin versions of the Z-UPC: a ROM-less version and a RAM version, both of which have the program address, data, and control lines buffered and brought to external pins. The version with no program ROM on chip is intended as a development tool. The RAM version, which has 36 bytes of vestigial bootstrap ROM on chip, is intended as a controller whose program is downloaded from the host processor.

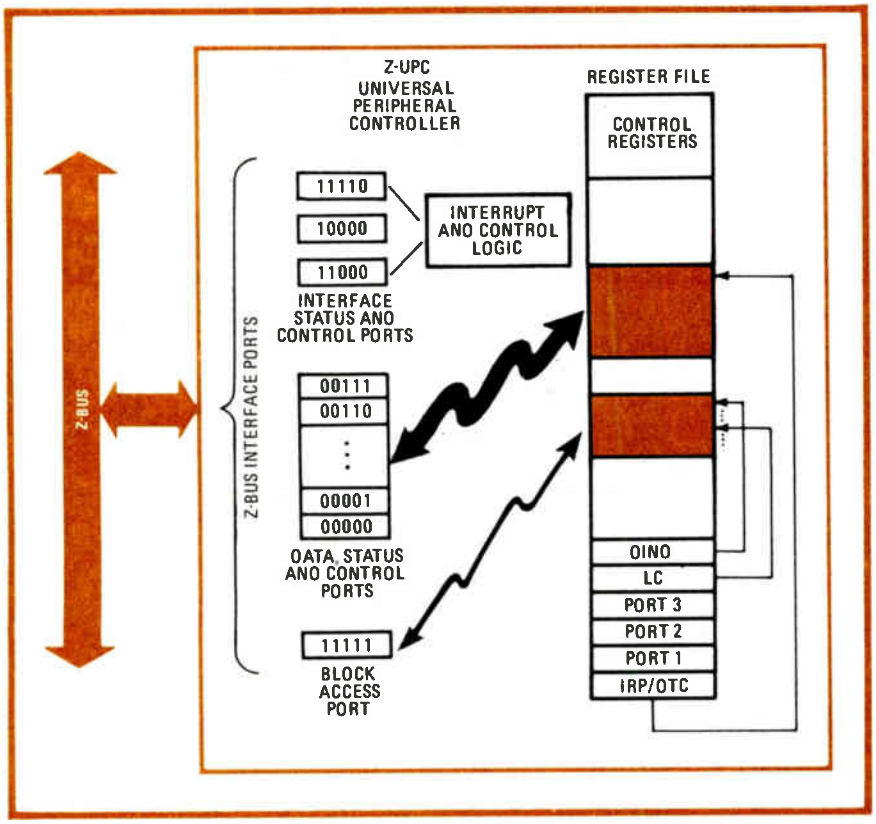
All three of these configurations are available with either the nonmultiplexed bus or the multiplexed Z-BUS interface to meet the needs of 8-, 16-, or even future 32-bit systems.

The UPC processor is organized around a 256-byte register file (shown in Fig. 2). Besides storing data and control and I/O functions for the processor, the register file serves as buffer storage for communication between the UPC and the host CPU.

In addition to 234 general-purpose registers, the register file contains 19 control registers for configuring and controlling the Z-UPC's I/O facilities and three parallel I/O ports. The control registers both specify how the hardware is configured and should function and provide status information for it as well.

A multipurpose register file

All of the general-purpose registers can function as accumulators, data buffers, address pointers, and stack or index registers. All ports and control registers can be accessed by UPC instructions like any other register. Instructions can access the registers directly or indirectly with an 8-bit address field. However, a 4-bit addressing scheme, which makes use of a register pointer, can save memory and execution time. In this scheme the register file is divided into 16 register groups, each containing 16 contiguous locations. The register pointer determines which group is being accessed, and a 4-bit address field specifies the register within the group. This capability is especially useful to speed context switching.



3. Control. The 20 control registers in the UPC are divided into three groups: 3 for the interface status and control; 16 for data, status, and control (mapped by the I/O register pointer); and 1 block-access register for the transfer of data to or from a buffer file that is set up by the UPC.

Programs running on the UPC may communicate with those running on the master processor in a number of ways: under interrupt control (either by the UPC or master); by transfer of byte data through data, status, and command registers; and by transfer of blocks of data to and from the UPC's register file.

Three groups

The host CPU can directly access the 19 interface registers through the Z-BUS interface. As illustrated in Fig. 3, the registers are separated from the UPC's internal registers and divided into three groups:

- Those for interface status and control, which the master processor can access to control UPC–generated Z-BUS interrupts, to interrupt the UPC, and to control message transfer over the Z-BUS.
- Those for data, status, and control, which are mapped into 16 registers by the I/O register pointer, controlled by the UPC. That arrangement gives the master processor direct access to 16 registers and allows transfer of data, status information, or control commands between the UPC and master processor.
- Those for block access, used by the master to transfer blocks of data into or out of a buffer in the UPC's register file. The UPC has complete control over the placement and size of the buffer in its register file.

Each of the three types can be read or written by the master processor. Because the UPC software has complete control over how these register groups are mapped into the register space, the layout of data in the registers is independent of the host processor's software and protected from it.

The UPC and the master processor can operate completely independently of each other. The UPC can ignore the data transfer request from the master by setting a bit in its master-processor interrupt control register. Any attempt to transfer data from the master when this bit is set causes an error flag, which will cause an interrupt to the UPC (if interrupts are enabled).

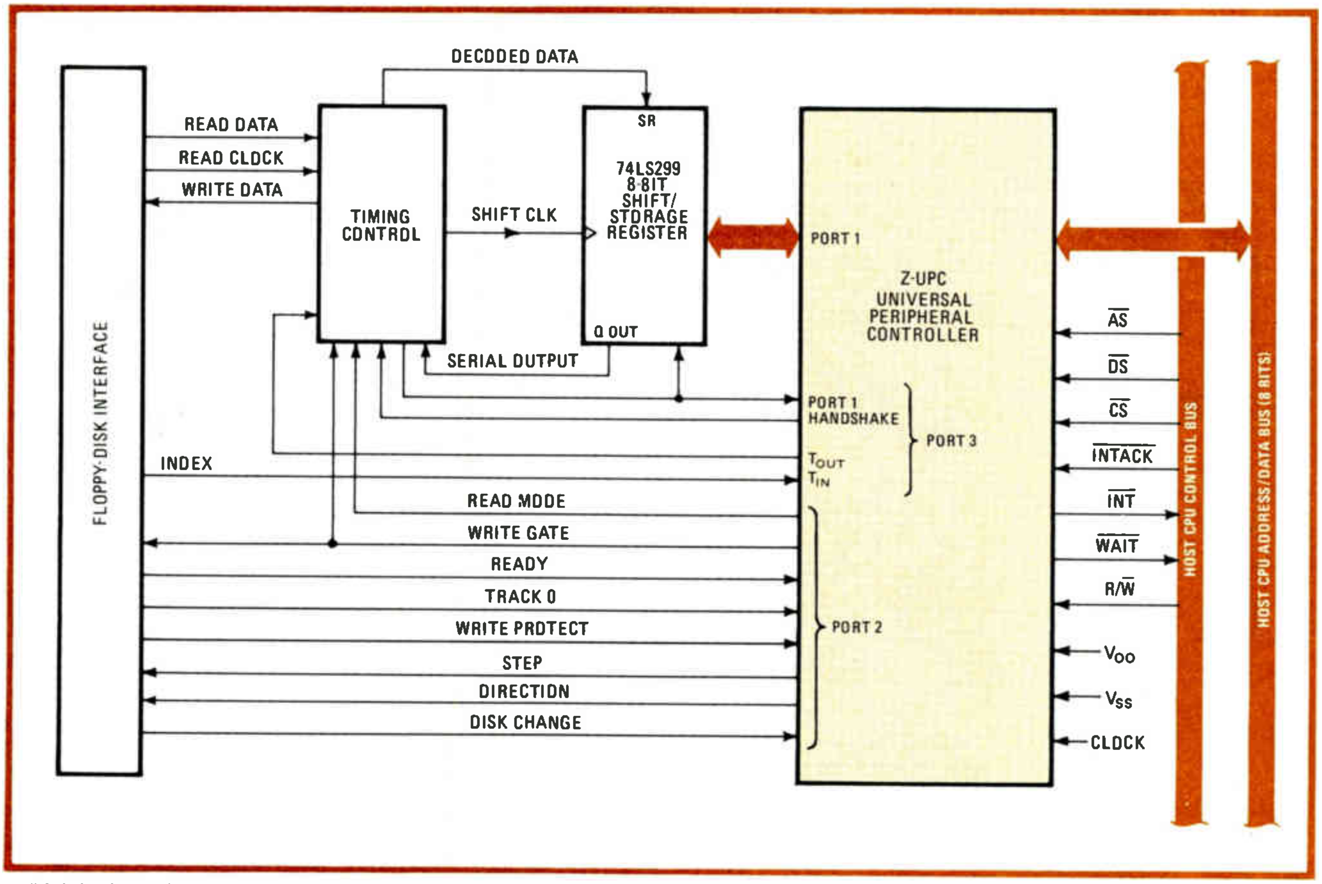
I/O lines by the dozen

The UPC has 24 lines dedicated to input and output that are grouped into three 8-bit ports. Since the ports are mapped into the register file, I/O data can be directly manipulated by any instruction. Each port has a mode-control register, which allows the port functions to be changed during program execution; for example, each line of port 1 and port 2 can be individually configured as input or output under program control. Each port can have its output lines defined as push-pull or as open-drain drivers.

Port 3 is a multifunction port. It has four input and four output lines that can be used for I/O or control functions. The control functions available through this port include interlocked handshake lines for ports 1 and 2, interrupt request inputs, timer input and output, and Z-BUS interrupt control.

Timing and counting

To support timing and counting requirements of software routines, the UPC provides two 14-bit timer/counters, T_0 and T_1. Among the timer/counter functions that are easily implemented by the UPC are; interval delay timer, time-of-day clock, watchdog timer (as for refreshing dynamic memory), external event counting, variable pulse-train output, duration measurement for external



4. Disk jockey. The UPC makes a controller for a floppy-disk drive that actually stores the file system on chip. The host has only to specify the file name and the function to be performed. The 74LS299 shift register converts serial into parallel data, which enters port 1 on the UPC.

events, and automatic delay after an external event.

Each timer/counter is divided into a 6-bit prescaler and an 8-bit counter and is driven by the internal UPC clock, divided by four. The internal clock for T_1 may be set up for gating or triggering by an external event, or it may be replaced by an external clock input. Each timer/counter may operate in either a single-pass or a continuous mode, so that after the last count either counting stops or the counter reloads and continues counting. The counter and prescaler registers may be altered individually while the timer/counter is running; software controls whether the new values are loaded immediately or when the end of count (EOC) is reached. The two timer/counters may be cascaded using the timer-input lines on port 3.

Interrupting the controller

To serve host or I/O-device requests quickly, the UPC provides six interrupts from eight different sources: three from ports, two from timer/counters, and three from the host-processor interface. All six interrupts may be individually or globally disabled. The interrupts are prioritized, with the interrupt-priority control register providing 48 different priority schemes for handling concurrent interrupts. What's more, the masking and prioritizing of the interrupts may be dynamically modified under program control.

The UPC's interrupts are vectored. When an interrupt occurs, the program counter and flags are pushed onto the stack, and control passes to one of six predetermined interrupt-handling routines. The routine is pointed to by an address that has been stored in the first 12 bytes of program memory. All of the interrupts are disabled after an interrupt is accepted. Interrupts can be nested by enabling them during the interrupt service routine; they are automatically enabled during the return from the routine.

The Z-UPC instruction set is compatible with the Z8 microcomputer instruction set (though the UPC's load-external-memory instruction is only available in the 64-pin RAM version of the Z8). This instruction set, comprising 129 instructions of 43 basic types and using six main addressing modes, speeds program execution and achieves byte efficiency. The types of data that it allows to be used include bits, binary-coded decimal digits, bytes, and 16-bit words.

Z-BUS support

The UPC can support the full Z-BUS interrupt structure, including daisy-chained priority resolution and vectored interrupt acknowledge. Using the interface control and status ports, the master processor has the full range of Z-BUS mechanisms for enabling or disabling Z-UPC interrupts, marking interrupts as being under service, clearing interrupts, setting interrupt vectors, and disabling interrupts from lower-priority devices.

A program running on the UPC can start the normal Z-BUS interrupt sequence (assuming interrupts are enabled) by setting the interrupt-pending bit in its master-processor interrupt-control register. Once that is done, the UPC hardware automatically handles the Z-BUS interrupt protocol—including output of the interrupt vector, which is held in a separate control register.

The master can generate an interrupt to the UPC by setting the end-of-message flag in the master-processor interrupt-control port. In addition, UPC interrupts are generated from the master when an error condition, such as transferring a block of data that is too long, occurs.

Block transfer within limits

The UPC's block-access port is ideally matched to the block-I/O instructions of the Z8000 microprocessor. With a single block-I/O instruction the Z8000 can address the block-access port and transfer a string of bytes into or out of the UPC. Each access by the Z8000 to the block-access port causes a series of actions in the UPC involving its data-indirection register and limit-count control register. The data-indirection register points to the UPC register that is read or written when the master reads or writes the block-access port. After each such read or write, the data-indirection register is incremented and the limit-count register decremented. When the limit count reaches zero, any further transfers through the block-access port will abort and cause a length-error interrupt in the UPC.

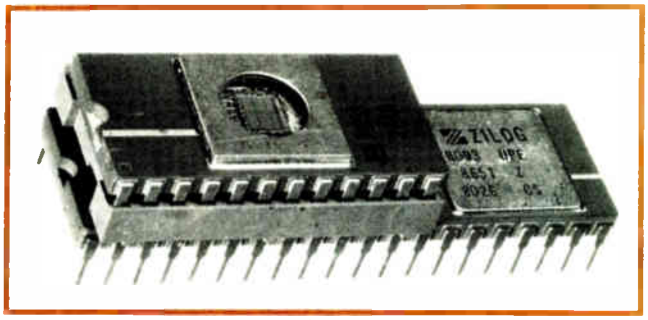
Ideas for application

The intelligence and flexibility of the UPC make it suitable for a wide variety of applications and allow it to offload the host computer in several ways. The UPC is capable of doing intensive off-line calculations, for example, such as those for data encryption. Also, it can perform the various code conversions and data formatting that are usually required in processor-to-device and device-to-device communications. Furthermore, it can buffer the data and generate controls for I/O devices such as printers and keyboards.

Figure 4 illustrates the UPC's application as a disk controller. Here, a file system can actually be implemented in the controller itself. The host processor has only to specify the file name and the function to be performed on the file. Depending on the sector size, either the register file or the external RAM in the 64-pin RAM version can be used as for data buffering. The serial-to-parallel conversion is done by a 74LS299 shift register, and the data is transferred using handshake logic in and out of port 1. Also, cyclic-redundancy error checking can be done by the UPC.

A UPC software package is available for Zilog's PDS8000 development system that includes an assembler (PLZ/ASM), a linker, and an imager. PLZ/ASM is a free-format assembler that generates relocatable and absolute object-code modules. It makes provision for external symbolic references and global symbol definitions. Data declarations, control structures, and DO loops between them supply a structured approach to the task of assembly language programming.

A development board, similar to the one that is now available for the Z8, will also be available. It uses the 64-pin version of the UPC to prototype a UPC-based system. The code thus developed can later be transferred to the ROM in the mask-programmable 40-pin version of the UPC, or it can be made available in image form for downloading to the RAM version.



5. Prototyping. The ROM-less version of the Z-UPC, called a Protopack, is available in a special 40-pin package with a 24-pin socket on its back. Suitable for prototyping and preproduction use, it accepts a 2716 E-PROM for its first 2-K bytes of program memory.

Two serial RS-232-C interfaces will allow the 11-by-14-inch board to be used alone with a cathode-ray-tube terminal or to be connected to one of Zilog's PDS or ZDS-1 series development systems. Cable connection to such a host system will permit the transfer of software from the host—where it is developed—to the board for testing. Included on the board is a 64-pin Z8, which serves as a program monitor for the UPC.

The board also contains 4-K bytes of 2716 erasable programmable ROM (for the monitor/debugger program) and 4-K bytes of 2114 static RAM. For the user who wishes to test a ROM-based version of his code, it also offers a socket for 4-K bytes of 2716 E-PROM that may be used in place of the RAM. The monitor/debugger software, comprising a terminal handler, a debugger, command interpreter, and an upload/download handler, provides the various commands necessary for control, I/O, and debugging.

A wrapped-wire area of 40 square inches accommodates additional customer interfaces or special application circuits. This arrangement allows for wide range of user applications.

Aid in prototyping

The Z-UPC Protopack—the ROM-less version of the standard Z-UPC, housed in a pin-compatible 40-pin package (Fig. 5) that carries a 24-pin socket to accommodate a 2716 E-PROM—is used for prototype development and preproduction of mask-programmed UPC-based applications. The 24-pin socket is equipped with 12 ROM address lines, 8 ROM data lines, and the necessary control lines for interfacing with the E-PROM for the first 2-K bytes of program memory.

Pin compatibility allows the user to design the printed-circuit board for a final 40-pin mask-programmed UPC and, at the same time, allows the use of UPC Protopack to build prototype and pilot-production units. When the final program is established, the user can then switch over to the 40-pin mask-programmed UPC for large-volume production. The Protopack is also useful in applications where masked ROM setup time and mask charges are prohibitive and program flexibility is desired. □

Sequencer plus PROM step three motors independently

by Vikram Karmarkar
Hindustan Computers Ltd., New Delhi, India

Using a 4-bit bipolar microprogram sequencer and a 32-word-by-8-bit programmable read-only memory as a storage element, this processor easily meets the frequent requirement for multiple, independent stepping of up to three motors in either open-loop or servo-type control systems. The software approach makes possible the building of a compact and extremely flexible position controller.

The Am2911 program sequencer provides dynamic control for each motor, which in turn is dependent upon the information residing in the 6311 PROM. Here, forward- and reverse-step sequences are stored (that is, the sequence to be taken for a specified direction), as well as the individual motor selection/disable codes and a 3-bit-wide instruction field for the sequencer. Note that each motor has separate step-sequence codes in PROM so that it is not necessary for all three stepping motors to be of the same type.

Information for setting the actual direction of each motor is introduced to the program sequencer through lines FWD1–FWD3 of the 74LS153 multiplexer, with FWD = 1 specifying the forward condition. The active state of each motor is determined by the $\overline{\text{MOT1}}$–$\overline{\text{MOT3}}$ lines, with $\overline{\text{MOT}}$ = 0 denoting the on condition. The system is clocked at a rate dependent upon system requirements and the capability of the stepping motors.

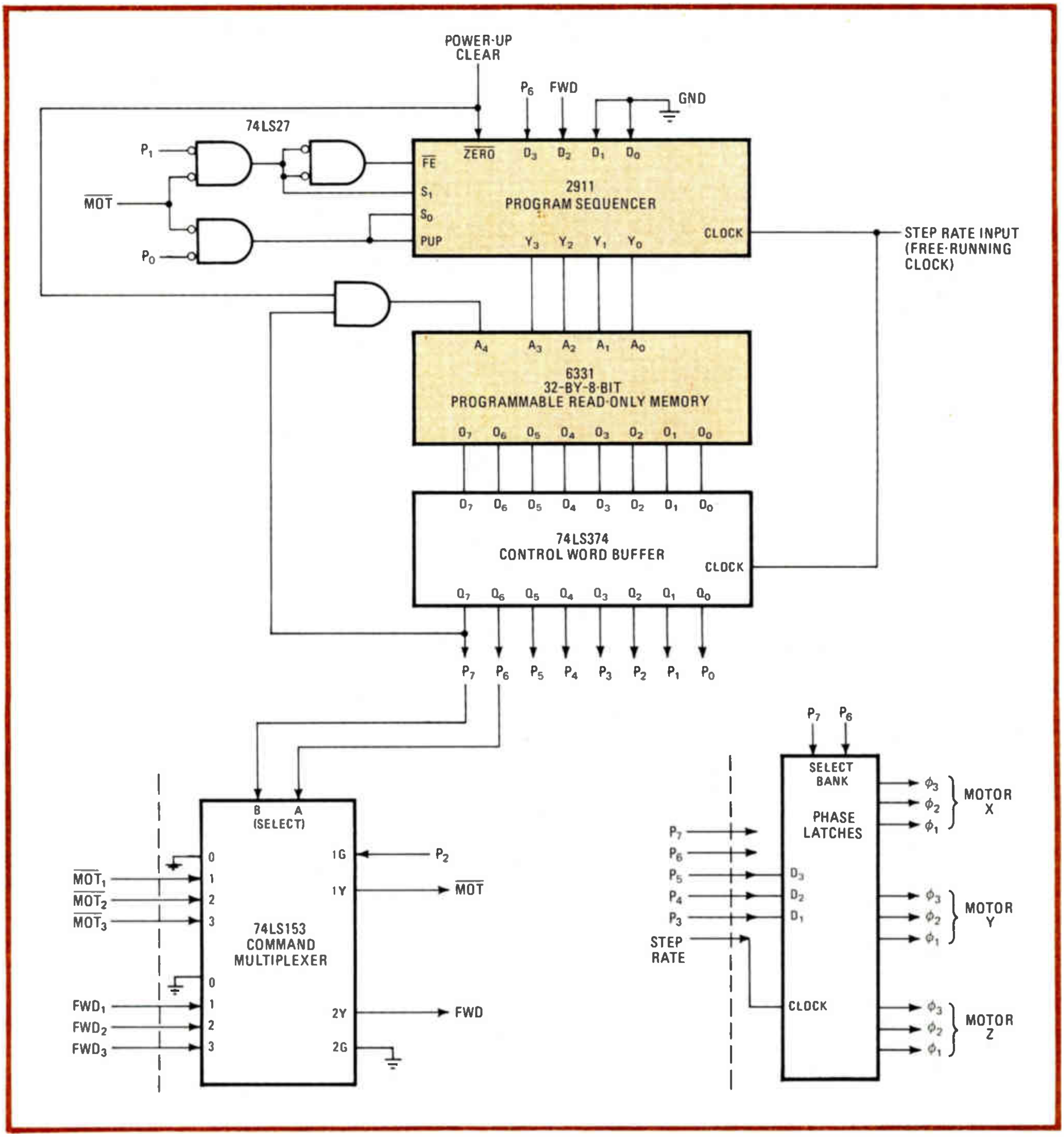
As for the software (see table), the main control loop, which occupies locations 00 to 04, handles all vectored subroutine calls. After each individual step sequence, program control returns to this main loop. Three no-operation instructions separate the control loop from the body of the program that samples each motor's status. Sampling of the $\overline{\text{MOT}}$ line of each motor determines whether the program control will branch or bypass a particular motor's subroutine. It may be observed from the notational shorthand that BR specifies an unconditional jump to the address presented to the Am2911 and that BRC is a branch to a given subroutine if its $\overline{\text{MOT}}$ line is at logic 0. PC specifies a step to the next address, and RTN commands return to the main program.

A typical sequence map for three motors is shown, where the forward sequence for any motor is 011, 101, 110 (3, 5, 6 in decimal). The reverse-direction modes are 110, 101, and 011 (6, 5, 3 in decimal). □

TYPICAL SEQUENCE MAP IN PROM

Address	Motor code P_7, P_6 (decimal equivalent)	Step output P_5, P_4, P_3 (decimal equivalent)	Next address instruction P_2, P_1, P_0	Hex code
00	0	0	PC	07
01	1	0	BRC	40
02	2	0	BRC	80
03	3	0	BRC	C0
04	0	0	BR	04
05	X	X	X	X
06	X	X	X	X
07	X	X	X	X
08	1	6	PC	77
09	1	5	PC	6F
0A	1	3	PC	5F
0B	0	0	RTN	05
0C	1	3	PC	5F
0D	1	5	PC	6F
0E	1	6	PC	77
0F	0	0	RTN	05
10	2	6	PC	B7
11	2	5	PC	AF
12	2	3	PC	9F
13	0	0	RTN	05
14	2	3	PC	9F
15	2	5	PC	AF
16	2	6	PC	B7
17	0	0	RTN	05
1B	3	6	PC	F7
19	3	5	PC	EF
1A	3	3	PC	DF
1B	0	0	RTN	05
1C	3	3	PC	DF
1D	3	5	PC	EF
1E	3	6	PC	F7
1F	0	0	RTN	05

BR: unconditional jump to address at D_2 of Am2911
BRC: branch to subroutine if $\overline{\text{MOT}}$ = 0
PC: continue to next address
RTN: return from subroutine



Simultaneous stepping. A microprogram sequencer and 32-word-by-8-bit PROM control the individual directions and stepping sequences of up to three servo motors. Its software approach gives the position controller great flexibility, as stepping sequences are ordered in PROM to suit particular applications. The servo-control system provides direction information through FWD1–FWD3 lines.

Synchronous pulse catcher snares narrow glitches

by Marian Stofka
Bratislava, Czechoslovakia

Positive and negative glitches are easily detected by this pulse catcher, which costs less than $5. It is especially useful in synchronous data systems, since it is capable of indicating if the glitch has been detected on the positive or negative level of the system clock. As a consequence of using clocked flip-flops, the unit snares pulses as narrow as 7 nanoseconds—a tenth of the width caught by conventional low-cost units built with monostable

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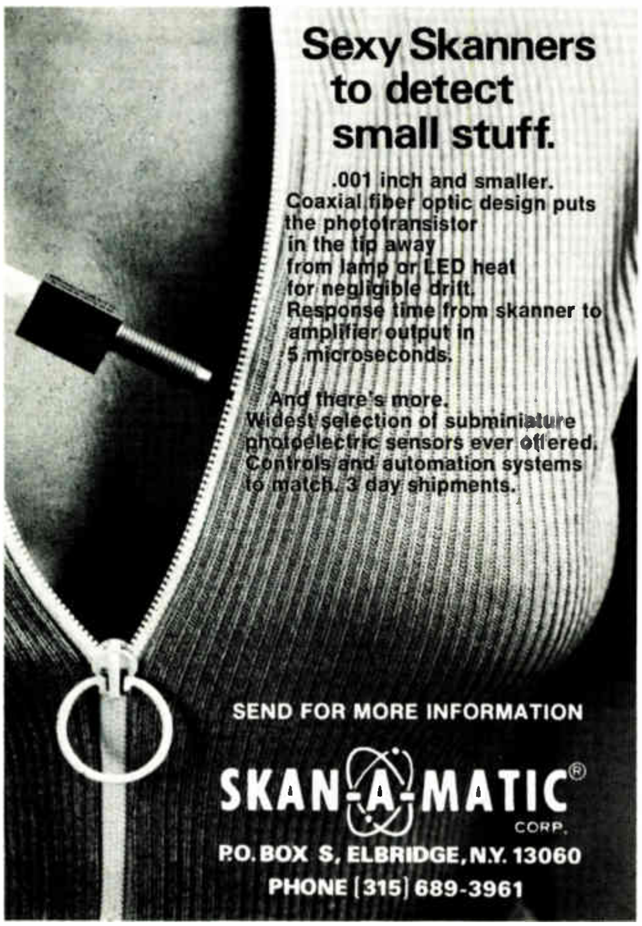

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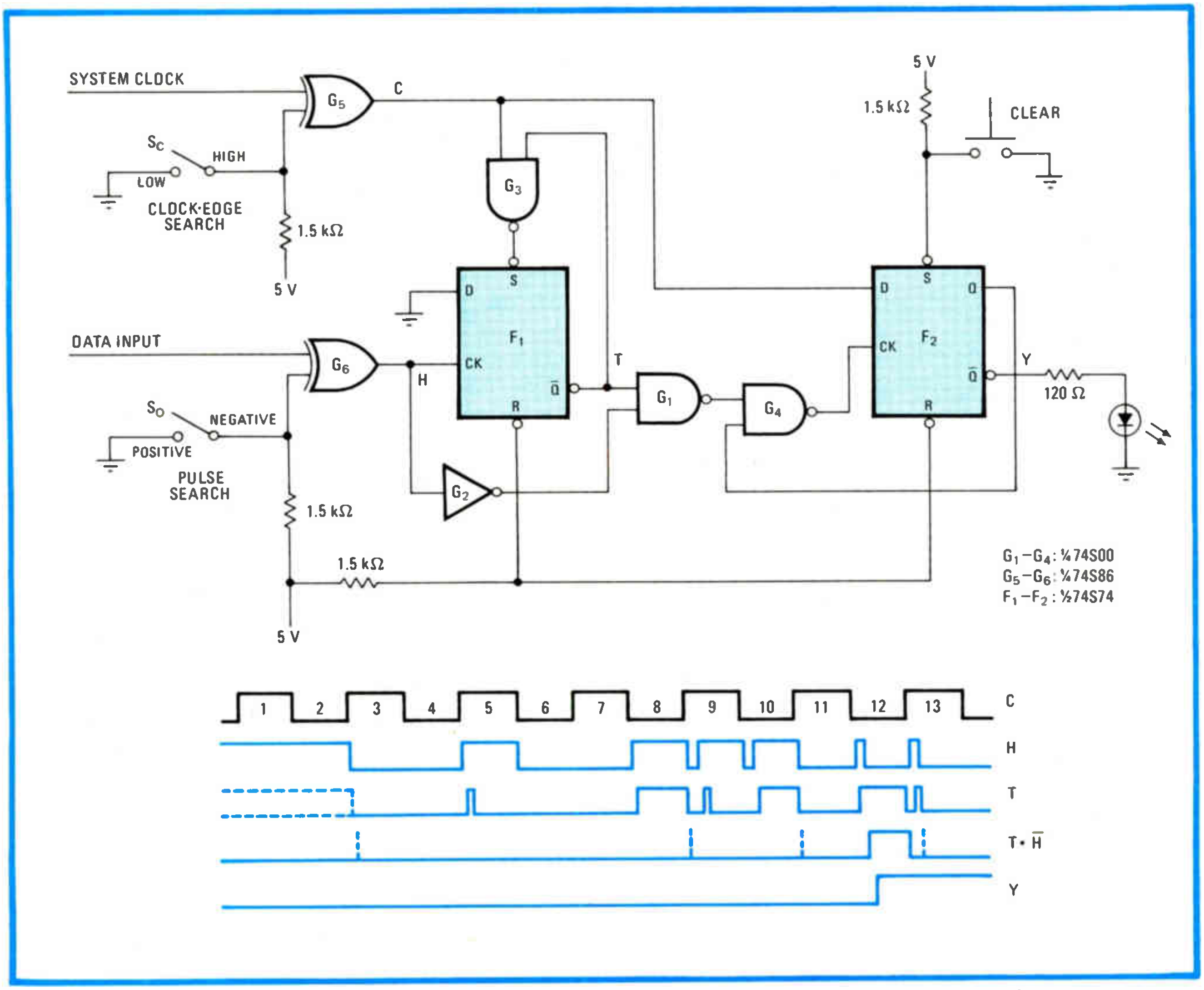

Glitch grabber. Synchronous pulse catcher detects narrow positive- or negative-going glitches on either 0-to-1 or 1-to-0 transition of system clock. Width of shortest pulse detected is determined by minimum width of clock needed to drive flip-flop F_1—in this case, 7 ns, which is well beyond the capabilities of conventional pulse catchers. LED serves as the output indicator. Timing diagram details circuit operation.

multivibrators and rudimentary logic.

Circuit operation is based on the principle that true data signals create only one input transition for a 0-to-1 or 1-to-0 system clock cycle; more than one data-input transition constitutes a glitch. Generally, data is stored in the 74S74 flip-flop, F_1, as shown, and compared with the input signal already stored at NAND gate G_1. If these data signals differ, flip-flop F_2 is triggered and the light-emitting diode at the output is turned on, indicating a glitch has been detected.

The operation of the circuit is subdivided into the search ($C = 0$) and prepare phases, which alternate with the logic state of the clock. The search and prepare phases can be inverted by selecting the initiating clock cycle's edge polarity that is desired (switch S_c). Similarly, a search for either positive or negative glitches can be selected (switch S_D).

As seen with the aid of the timing diagrams, whenever a positive data transition occurs during a 0-to-1 clock cycle, the Q output of F_1 is set high. Slightly before this time, the output of inverter G_2 has gone low, however, and so there is no logic-race condition at comparator G_2.

During the search phase, the set input of F_1 is released because G_3 is disabled by $C = 0$. The input data, once high ($H = 1$) must remain so within the present search phase. Otherwise the output of inverter G_2 will go high and the comparator G_1 will produce a pulse that triggers glitch-memory F_2. Selection of a search for positive and negative glitches by simple inversion of the input data is made possible by the fact that F_1 is edge-triggered. Gate G_4, connected to the clock input of F_2, prohibits loss of information once a glitch is detected. The LED will then light and remain on until the circuit is manually cleared.

During the preparatory phase, the ability to catch glitches is lost, but F_1 is set for next search because it is cleared during this time. F_1 clears itself through G_3, rather than directly. Thus there is no dead time during which a glitch might slip through. Short false-pulse indications may still appear if input-data transitions immediately follow the clock signal, however. To ignore these indications, the D input of F_2 is driven by G_5, which serves as a buffer for the clock. □

Engineer's newsletter

Interface book covers transducer uses and connections

Bridging the information gap between electronic measurement system designers and the growing number of engineers engaged in monitoring temperature, pressure, force, level, and flow, Analog Devices' new Transducer Interfacing Handbook describes the most popular kinds of transducers available for such measurements and the components used with them, as well as how to connect these devices. Covered are such subjects as transducers as circuit elements, using bridges, eliminating interference, using amplifiers and ways to implement signal translation, and offsetting and linearizing. **Eight of the fifteen chapters are devoted to applications,** including discussions of thermoswitches, thermocouples, resistance temperature detectors, and semiconductor temperature transducers, and separate chapters on interfacing pressure, force, and level transducers, as well as flowmeters.

Edited by Dan Sheingold, manager of technical marketing, the 266-page hardbound text costs $14.50. Copies may be ordered from Analog Devices Inc., P. O. Box 796, Norwood, Mass. 02062.

Fiber-optics exchange lights the way

A little-known source, the Navy's low-profile Fiber Optics Information Exchange serves as a major bibliographical reference for highlighting the latest happenings in light-wave communications and technology. The organization's aperiodic listings are available free of charge to the general public, **representing, for the most part, little-known work of a highly diverse nature done for various governmental agencies.** The latest listing is a healthy 39 pages. Contact the Commander, Fiber Optics Information Exchange, Code 825, Naval Ocean Systems Center, San Diego, Calif. 92152, for more information.

Thermal seminar puts heat on semiconductors

A concentrated one-day course, "Thermal Characterization and Evaluation of Semiconductor Devices," sponsored by the University of California Extension, Berkeley, will be presented at three locations across the nation in October. The sites and dates are: Scottsdale, Ariz., Oct. 13; Cambridge, Mass., Oct. 15; and Dallas, Texas, Oct. 17. **Intended for engineers and engineering managers involved in the manufacture and use of semiconductors,** the course will cover thermal impact on performance, heat-flow concepts, thermal analysis, and measurement techniques and associated problem areas. Almost all types of semiconductor devices—among them low- and high-power transistors; field-effect transistors; rectifier, optical, and microwave diodes; integrated circuits, including logic arrays and microprocessors; and digital and analog hybrids—will be discussed.

The course instructors, Bernard S. Siegal and David A. McGreenery, are president and marketing applications manager, respectively, at Sage Enterprises, Mountain View, Calif. Their firm specializes in the manufacture of semiconductor measurement and test systems.

The price of registration at any of the three locations is $150, including lecture notes and lunch. Enrollment is limited and advance registration is mandatory. For a brochure containing a detailed program description and registration information, write to Continuing Education in Engineering, University of California Extension, Berkeley, Calif. 94720, or call (415) 642-4151.

-Vincent Biancomano

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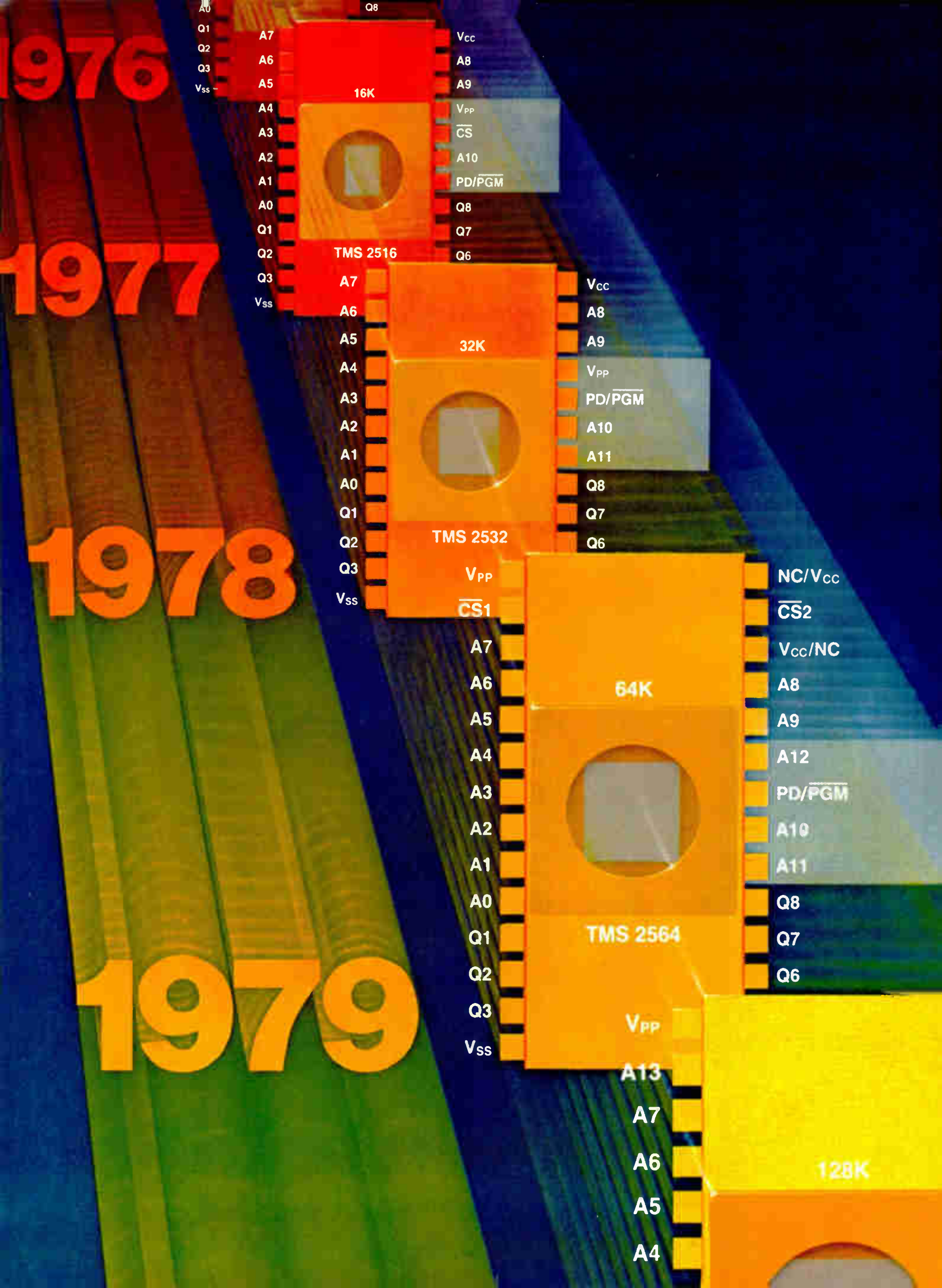

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PD/PGM
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128K
VPP
A13
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A6
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A4

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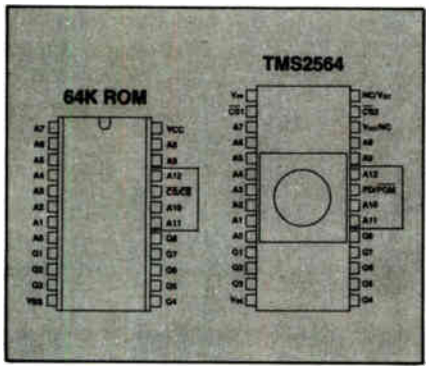

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TMS25L32	32K	5 V	325 mW	50 mW	450 ns
TMS2532	32K	5 V	400 mW	50 mW	450 ns
TMS2516-35	16K	5 V	285 mW	50 mW	350 ns
TMS2516	16K	5 V	285 mW	50 mW	450 ns
TMS2508-25	8K	5 V	250 mW	50 mW	250 ns
TMS2508-30	8K	5 V	250 mW	50 mW	300 ns
TMS2716	16K	+12, ±5 V	315 mW	—	450 ns
TMS27L08	8K	+12, ±5 V	245 mW	—	450 ns
TMS2708	8K	+12, ±5 V	690 mW	—	450 ns
TMS2708-35	8K	+12, ±5 V	690 mW	—	350 ns

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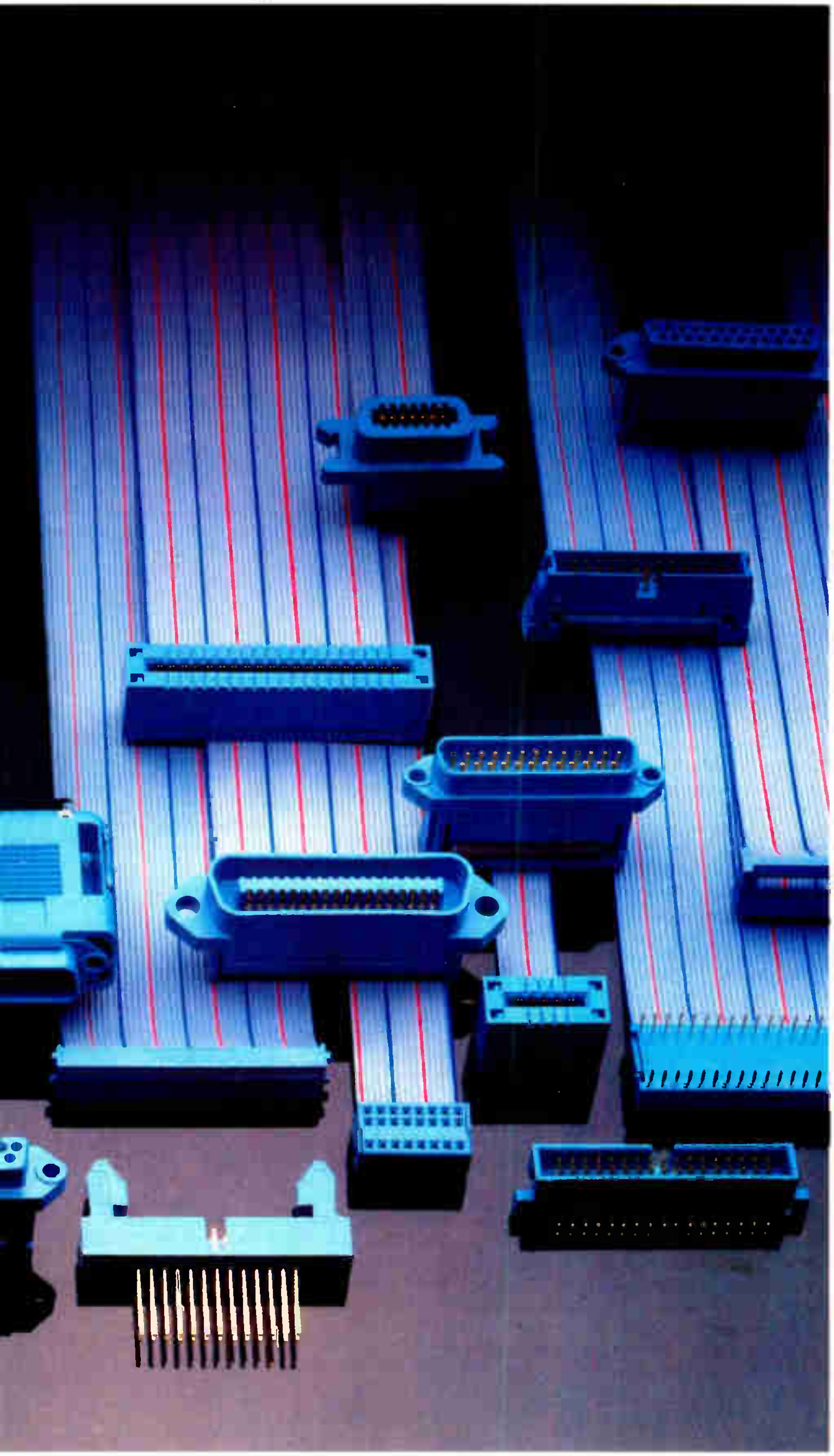

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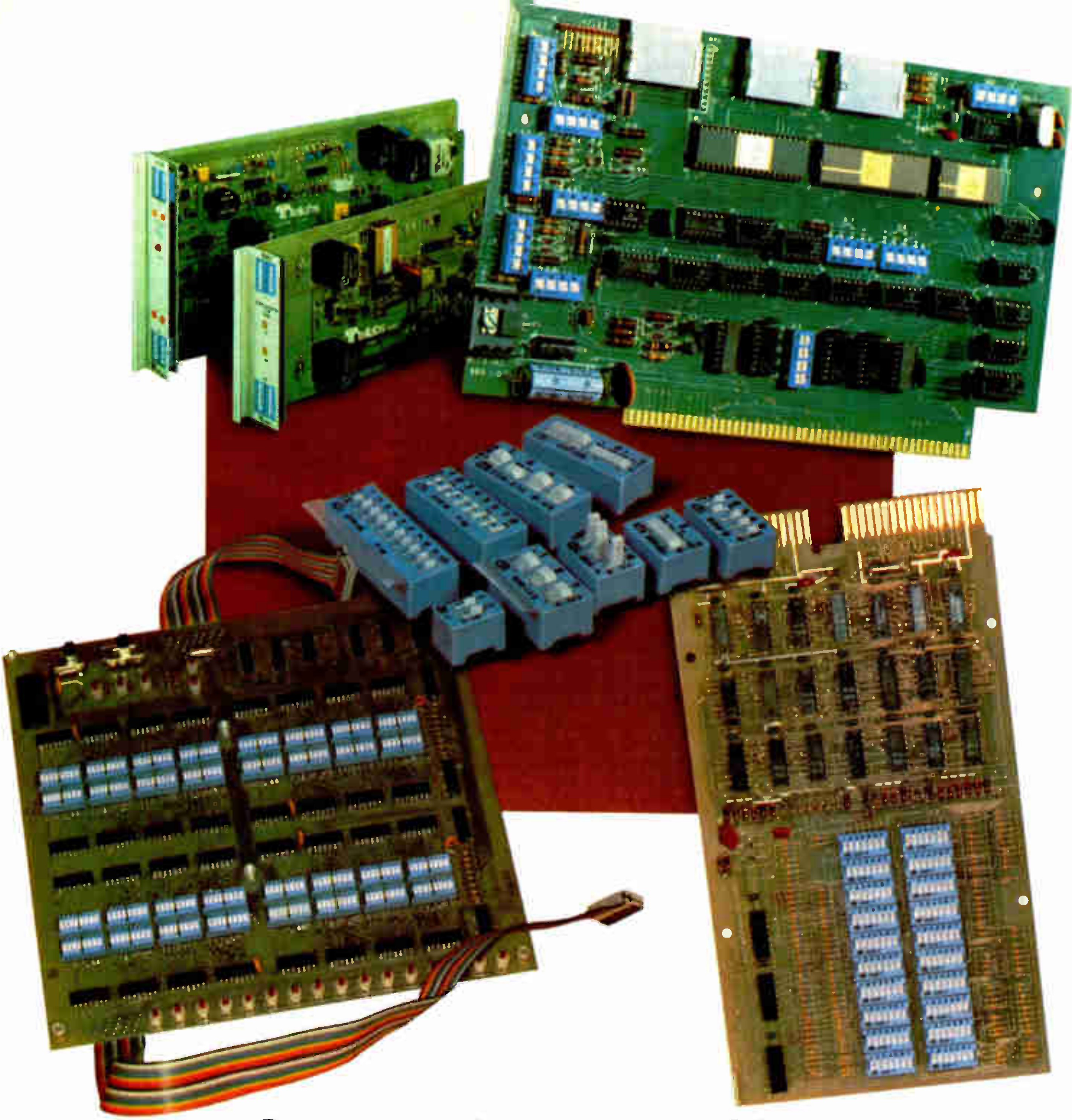

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New products

6½-digit DMM is priced at under $1,000

For bench or systems, a new design offers programmability and direct connection through separately controlled inputs

by Alan Serchuk, New Products Editor

High-performance, smart digital multimeters that are equally at home on the work bench or installed in a system normally cost a few thousand dollars. But Keithley Instruments is now introducing one that sells for less than $1,000.

In a nutshell, the model 192 programmable DMM provides a number of features not often found in instruments in this price range. These include:

- Display of 5½ digits (6½ with extended resolution).
- Accuracy to within 0.0005%.
- Up to 35 readings per second on the IEEE-488 bus.
- Sensitivity of 1 μV with autozeroing and automatic calibration for stability.
- Input impedance of 10 GΩ up to 20 V with a 120-dB common-mode rejection ratio.
- Math functions and data storage.

Behind the unit's low cost and high performance is a careful mixture of clever digital and analog design. For example, an intelligent digital filter is used in place of a costly RC filter to minimize input noise. The filter tracks slowly varying inputs but switches itself out when a large signal change is sensed. The result is a settling time to within 6 digits of only 250 ms for a step change.

On the analog side of the design, the company uses a novel input circuit that provides the high input impedance and CMRR needed for many industrial and lab applications. A bootstrap circuit, it permits the input amplifier's power supply to float with the input. The resultant 10-GΩ is 100 times larger than that found in other DMMs.

Also, Keithley incorporated low-leakage junction field-effect transistors as input multiplexers. Because they exhibit less than 1 pA of leakage current, it was possible to connect nine of the components to the input amplifier, resulting in simpler and lower-cost switching circuits compared with the relay and ganged FET switches usually used. And to improve the instrument's performance in making microvolt-level measurements, the J-FETs have copper leads to minimize thermal offsets.

Storage. The 192 stores up to 100 readings; speed ranges from a high of 35 per second to 1 per hour, making possible data accumulation over a four-day period. Front-panel controls permit selection of 10 reading intervals; data may be read back through the unit's display or transmitted over the IEEE bus using an optional interface. (The transmission rate over the bus depends primarily on the speed of the system controller.)

The integrating analog-to-digital converter of the 192 combines high normal-mode rejection (60 dB at 50 and 60 Hz) for a 5½- or 6½-digit display with 4½-digit reading rates of up to 35/s. At 5½ digits the 60-Hz reading rate slows to 10/s; additional filtering provides 6½-digit resolution at the same conversion rate.

New products

Operating in the triggered mode, the first byte for a 5½-digit display is available 39 ms after a trigger. That means, for example, triggered 5½-digit conversions may be made at the rate of 25/s.

Separate input ports allow direct cabling from test points to the 192. This permits additional flexibility not obtainable with single-input instruments. For example, dc measurements can be made while waiting for a new input to the ac terminals to settle. Switching costs may also be significantly reduced, since independent switching may be used for dc and ac voltage and resistance. Often, this means that switching for one or more functions can be eliminated. However, if an application requires a single-port input, an optional rear-panel port is available.

The ranges. Five dc voltage ranges (200 mV and 2, 20, 200, and 1,200 V) allow measurement from 1 μV to 1,200 V. For an additional $175, those same ranges will cover ac voltages in an averaging mode; the option can be added at the factory or installed later by the user. There are also six ranges from 200 Ω to 200 MΩ to cover resistance measurements.

Several math programs are also part of the 192 DMM. These include scale factor and offset modifications according to the formula $y = mx + b$. Other programs cover percentage deviation from an entered nominal value, storage of minimum and maximum readings, and high- and low-pass limits.

Full control of range, function, and zero controls can be transferred to a remote location through the IEEE bus using the optional interface, which is priced at $395. The same arrangement provides remote access to stored data and permits remote programming of trigger mode, data terminators, and reading rate.

The model 192 programmable digital multimeter is priced at $995 and is available with 60-day delivery.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, Ohio 44139. Phone (216) 248-0400 [338]

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Books of special interest to our readers

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Rf sources suit design and production

Two microprocessor-controlled signal generators bring the performance once limited to design-quality instruments to production testing

by Bruce LeBoss, San Francisco regional bureau manager

Signal generators suited to receiver design have been inappropriate for production testing because they were too expensive, too slow, or could not be programmed for system automation. Conversely, inexpensive generators suited for production testing generally do not have spectral purity adequate for design work. Two new microprocessor-controlled synthesized rf signal generators from John Fluke Manufacturing Co. now make possible receiver testing and design using the same instrument.

Designated the 6070A and 6071A, the new units differ only in frequency range: 200 kHz to 520 MHz and 200 kHz to 1,040 MHz, respectively. Bob Hightower, product marketing manager at Fluke's Precision Instruments division, says that the instruments' spectral purity "equals that of most cavity-tuned generators."

According to Hightower, the instruments make it easier for engineering and production to produce data of the same high quality. They allow off-channel tests (of adjacent channels, for example) to be done during production, improving the receiver's performance and reliability and cutting the warranty costs resulting from rejected and returned products. "What's more," he notes, "engineering and production instruments can be interchanged as necessary."

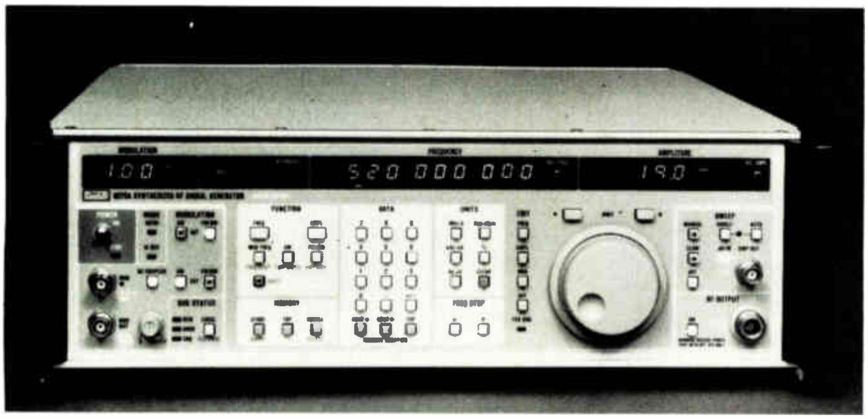
Synthesis techniques. To achieve their broad frequency coverage while limiting spurious output levels to about 90 to 100 dB below the carrier (dBc), Fluke engineers developed several cost-effective synthesis techniques, among them the use of a Fluke-designed and -built surface-acoustic-wave (SAW) device, and a delay-line discriminator, or interferometer, explains Fred Telewski, an engineering manager. In addition, the designs include the use of advanced phase-locked synthesis techniques and sealed rf compartments, he points out.

In their noise performance, the two new units "are comparable to the best generators available today," claims Telewski. For example, the broadband noise floor is −150 dBc/Hz, and single-sideband phase noise is typically −140 dBc/Hz at 20 kHz offset. By contrast, the performance of on-channel–only signal generators is typically −50 to −70 dBc, with SSB noise at −80 to −110 dBc at 20 kHz offset. Off-channel–type signal generators typically limit spurious output levels to −90 to −110 dBc, and phase noise to −130 to −150 dBc. Typical flatness of the 6070A/6071A output is ±0.2 dB from 0.2 to 520 MHz and ±0.3 dB from 520 to 1,040 MHz for the 6071A only. Resolution is 1 Hz below 520 MHz; 2 Hz above.

Each of the two new instruments relies on a 16-bit microprocessor, Texas Instruments Inc.'s TMS 9900, to provide special instrument functions, including control via an IEEE-488 bus interface, and perform a variety of self-tests. Among the complex functions that can be executed from simple commands—a stroke of a "shift" key followed by two numerics—are dcfm (dc mode frequency modulation), high deviation, fixed range, sweep speed and sweep symmetry, narrowband-wideband reference, modulator oscillator output, and amplitude correction.

When the new instruments are turned on, the microprocessor in each enables them to automatically perform a functional self-check, then go to programmed safe power-up settings. A nonvolatile memory option also enables the instruments to turn on at power-down settings. Other special functions, under control of the 9900, allow the user to test the instrument's displays and annunciators and do a pattern-sensitivity random-access memory check, as well as run a check of the nonvolatile memory and set or reset the status-request line.

Furthermore, the internal self-check mode is provided with a variety



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of diagnostics and error codes. If a user incorrectly programs the instrument, the entry is rejected and an interrogate button can be pushed to display the appropriate error. Codes with explanations and other operating instructions are found on a pull-out card located beneath the front panel.

The 6070A and 6071A each contain a built-in memory that allows up to nine (50 with the nonvolatile memory option) commonly used front-panel setups and test sequences to be stored and recalled. Test sequences may be stepped through one memory location at a time, and editing features allow the insertion or deletion of program steps during development. In all, each instrument contains 32 kilobytes of program read-only memory, 2 kilobytes of scratch-pad RAM, and a like amount of calibration memory stored in erasable programmable ROM.

The new signal generators have three display sections: a three-digit display that indicates modulation frequency, a-m depth, and a-m or phase deviation; a 9½-digit display of carrier frequency, shifted function parameters, status information, and frequency error messages; and a 4½-digit display of dB, dBm, volts, mV, and μV, as well as amplitude error codes.

According to Hightower, the new instruments "retain all the popular features of manual signal generators," like the analog tuning knob, which uses a long-life magnetic detent and an optoelectronic phase-sensing rotation detector. This combination, he explains, "eliminates mechanical drag" and "gives a smooth analog-like feel with digital precision for adjusting frequency, amplitude, or modulation."

To be introduced domestically at next month's Wescon '80 in Anaheim, Calif., as well as at the subsequent Automatic Test Equipment Conference in Paris, the 6070A and 6071A are priced at $15,000 and $17,000, respectively. Availability is 90 days after receipt of order.

John Fluke Manufacturing Co. Inc., P.O. Box 4310, Mountlake Terrace, Wash. 98043. Phone (206) 774-2211 [339]

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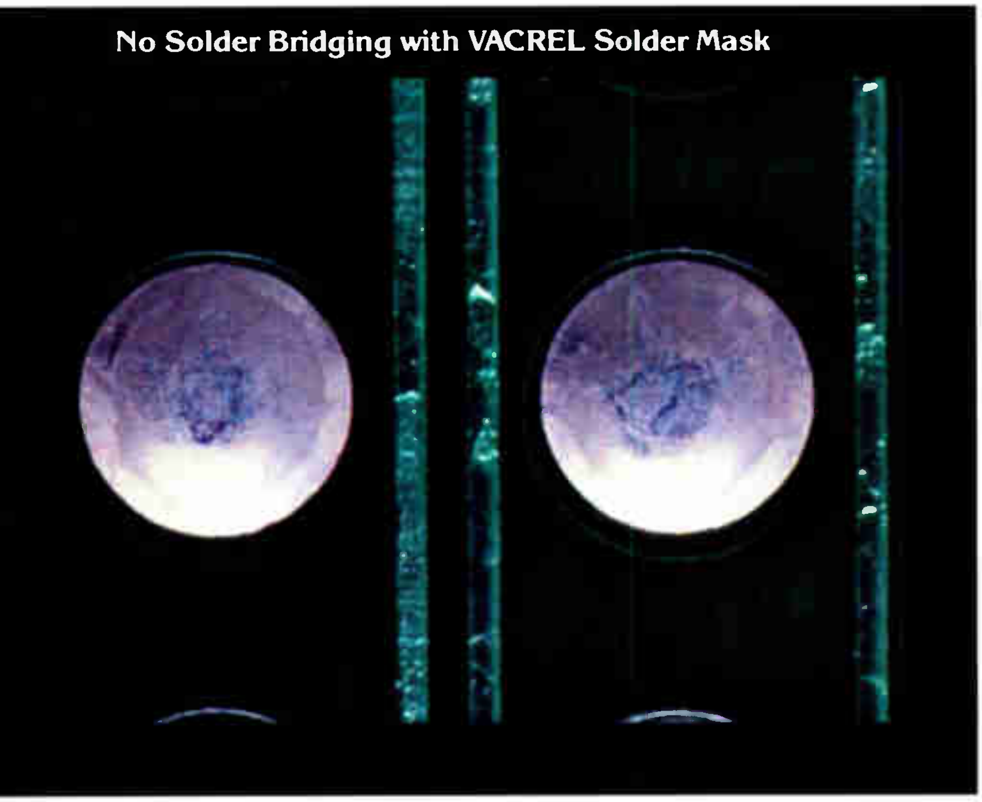

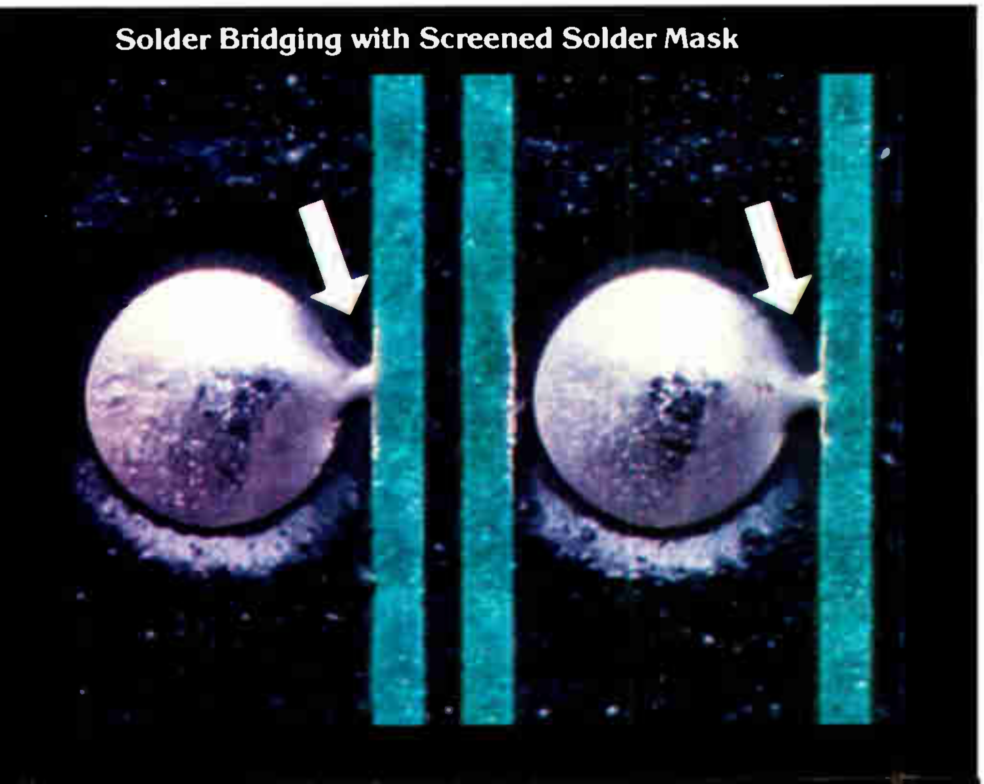

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Microcomputers & systems

4-bit controllers dissipate 50 μW

C-MOS technology results in low standby rating; active power dissipation is 4 mW

National Semiconductor Corp. may have hit a new "low" in the 4-bit microcomputer marketplace. The four latest units of its COP (control-oriented processor) family of single-chip microcontrollers are the first members to be fabricated using complementary-MOS technology [*Electronics*, July 31, p. 34]. One result is what is believed to be the lowest power dissipation available for 4-bit microcomputers.

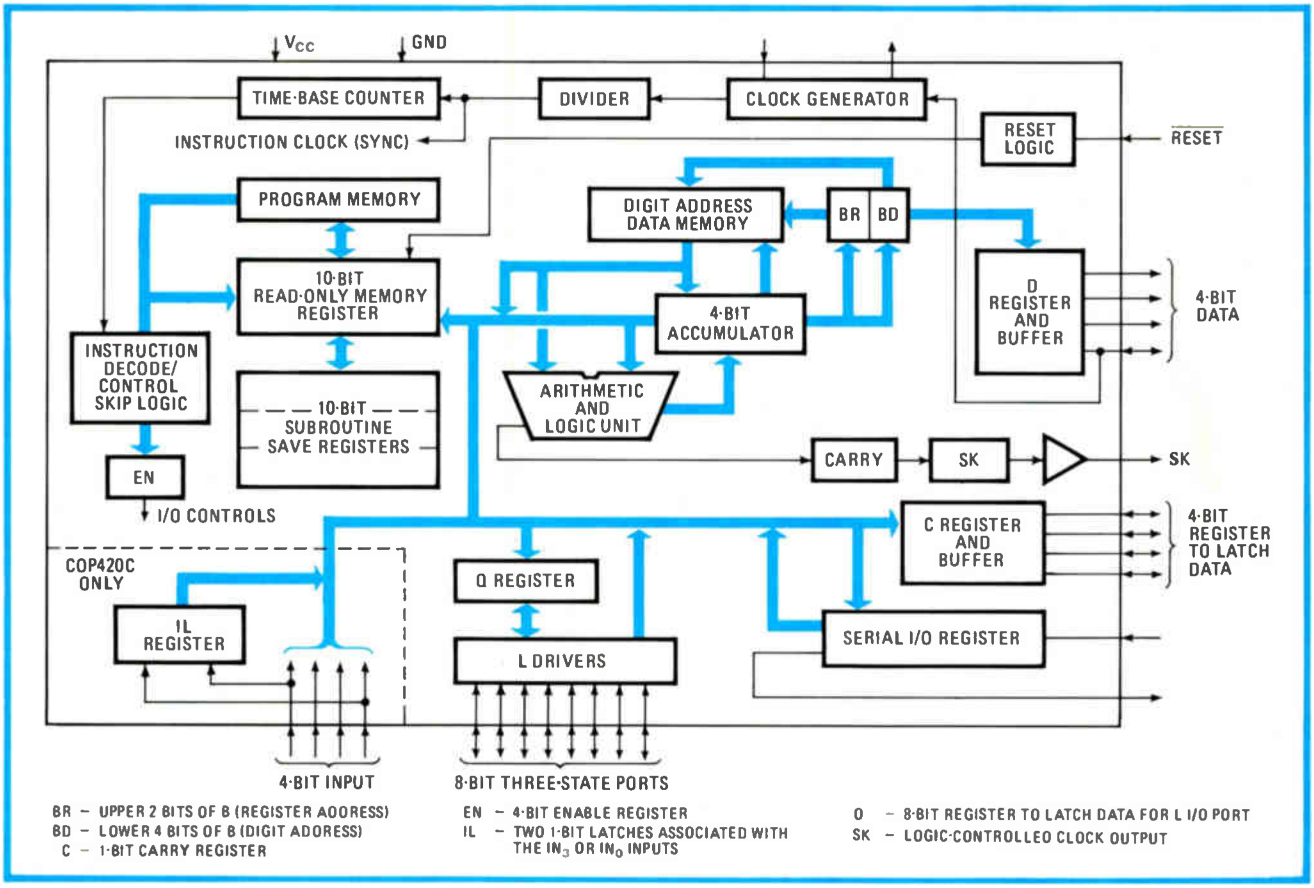
Designated the COP420C, COP-421C, COP320C, and COP321C, the additions are complete microcomputers containing all system timing, internal logic, read-only memory (8-K bits organized as 1,024 by 8 bits), random-access memory (256 bits organized as 4 by 64 bits), and the input/output facility necessary for dedicated control functions.

Except for having 4 fewer I/O lines (19 instead of 23), the 421C is identical to the 420C. Both operate over the 0°-to-+70°C temperature range. The 320C and 321C are extended-temperature-range (−40° to +85°C) versions of the 420C and 421C, respectively.

Typical power dissipation of the four microcontrollers when idle is 50 μW (with a 32-kHz clock and a 2.4-V supply). In the operating state, dissipation rises to 4 mW typically (500-kHz clock and 5-V supply). In comparison, the earlier, n-channel MOS members of the COP family typically dissipate 3 mA at 3.3 V.

In addition to the power-saving idle state, the new units also include software control of power-up and power-down, notes product marketing manager Tom Harper. In a power-loss situation, he adds, the devices can turn off, then turn back on, "taking up where they left off," using a backup battery.

The vectored interrupt, plus restart, and three-level subroutine stack featured in the new devices, Harper claims, "allow the user to achieve program efficiency unattainable in other microcontrollers." The C-MOS units employ the same instruction set, pinout, and architecture as other members in the COP family, he says, "enabling users to incorporate them into systems without the need for extensive retraining. Also, the programmability of the I/O ports, featured in the entire COP family, reduces the amount of external hardware required and provides drive characteristics compatible with



Microcontroller in C-MOS. The C-MOS versions of National's family of control-oriented processors include two (the COP420C and the extended-temperature-range 320C) with four extra pins that form a 4-bit input port (left). Two of the lines carry signals to a latch register.

Multiwire* Optimizes ECL.

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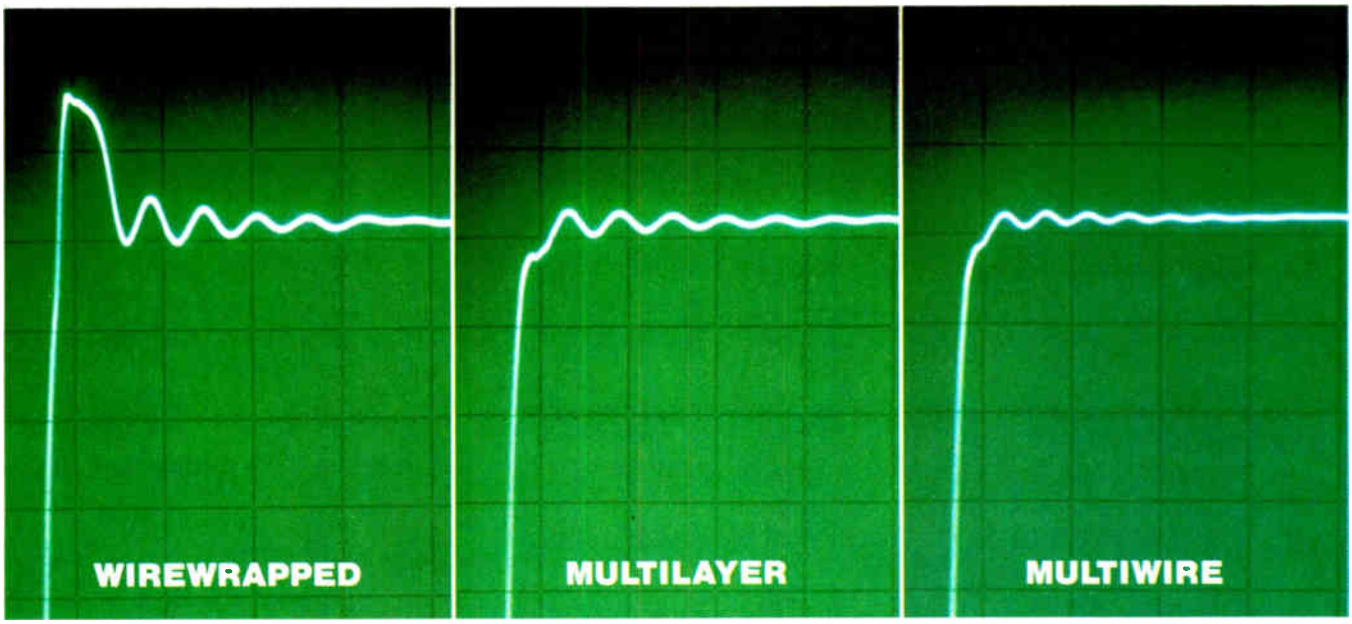

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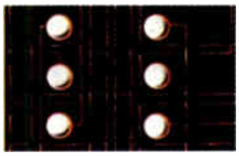

A typical example of the circuit density achievable with Multiwire circuit boards.

Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307

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the user's external circuitry."

As with other COP members, the new devices are Microbus-compatible, allowing them to be used as peripheral microprocessor devices, receiving and transmitting data and commands from and to a host microprocessor in less than 1 μs. They are also compatible with Microwire, National's standard three-wire bus interface, he notes, a feature that enables the end-user to add several peripheral devices.

Tailored for applications in telecommunications, automotive, and security systems, among others, the four microcontrollers operate from a single power supply (2.4 to 6.0 V), and contain an internal time-base counter for real-time processing.

The COP420C and 320C are housed in 28-pin dual in-line packages, and the 421C and 321C come in 24-pin DIPs. Available nine weeks after receipt of customer programming, the four are priced in the $20 range in 1,000-piece quantities and in the $5 range in high volume (about 100,000 pieces).

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [371]

Timesharing system compiles PL/M languages for 8086s

The National CSS timesharing service is offering a PL/M software development system for the Intel 8086. The PLM/S86 compiler accepts 8086 mnemonics and produces relocatable object modules that take advantage of the power and address space of the 8086. It also provides syntactic debugging facilities by detecting errors and producing messages as well as variable cross-reference lists. Error messages include statement, line number, and diagnostic information. The modules may be linked and down-loaded into the user's system over the National CSS telecommunications network.

Charges are determined by usage, and average less than $30 per hour.

National CSS Inc., 187 Danbury Rd., Wilton, Conn. 06850 [373]

Communications

500-W amplifier works to 35 MHz

Completely solid-state circuit shows gain of 60 ± 1 dB across all load impedances

High gain-bandwidth product in an all-solid-state class A amplifier operating up to 35 MHz seems unlikely given the properties of radio-frequency transistors. Therefore the model A500 amplifier, which generates 500 W between 30 kHz and 35 MHz, is a notable accomplishment.

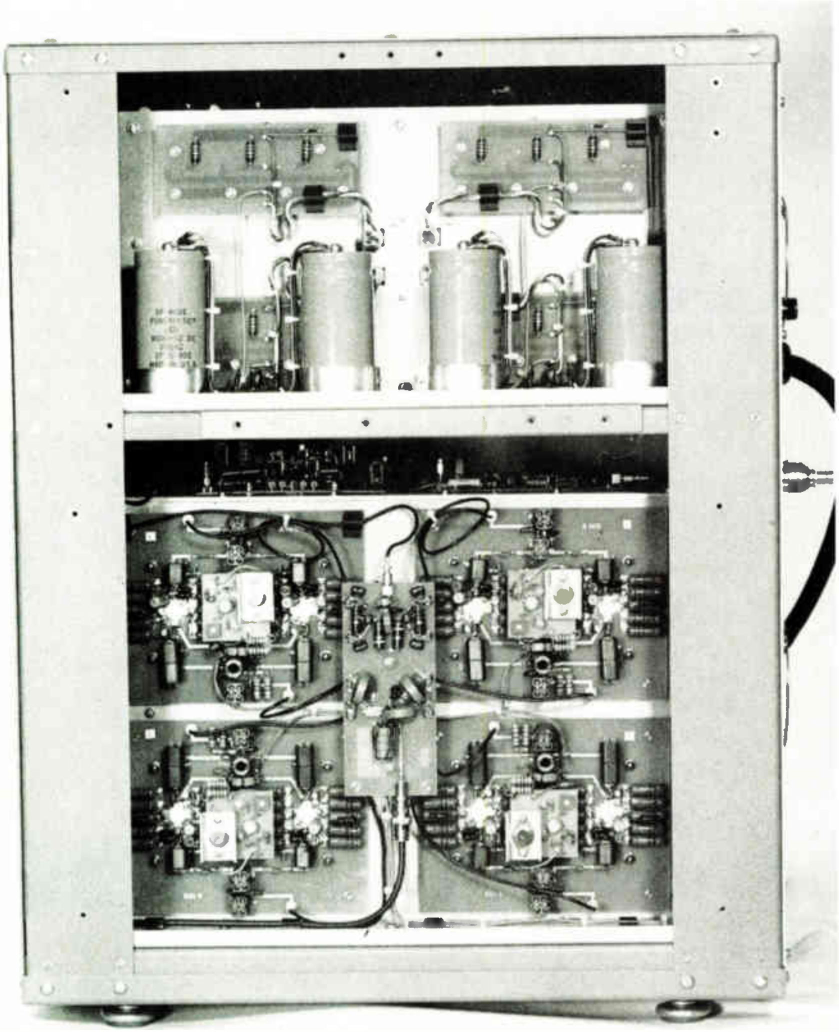
The problem with rf transistors is that they must use relatively small junction areas to achieve their frequency response. The smaller the junction area, the lower the thermal-power-handling capability. As a result, high bandwidth and gain are generally incompatible in the same device.

This dilemma can be resolved by combining the outputs of low-power transistors. However, parallel connections are usually impractical, since the transistors are often different from one another and their outputs do not combine in phase properly. Series adding circuits and push-pull designs generally suffer the same limitations.

The classic hybrid circuit—a 3-dB divider with phase quadrature on the outputs, often used in telephone repeater coils and microwave signal combiners—offers a solution to this dilemma. Electronic Navigation Industries has used this four-port device to electrically isolate the individual transistors in its A500 power amplifier so that the outputs add properly.

Many applications. According to Leonard M. Salmen, vice president of ENI, the A500 is especially suitable for use in high-frequency transmitters and electronic-countermeasure equipment. Other applications include driving linear accelerators, plasma and sputtering equipment, ultrasonic systems, and nuclear magnetic resonance gear and in general laboratory use.

The unit has an extremely flat gain of 60 ± 1 dB, making it compatible with any commercial synthesizer and signal or sweep generator. The wide frequency range and linear phase response of the A500 enable it to amplify amplitude- or frequency-modulated, single-sideband, or pulse-code-modulated signals with harmonic distortion held 25 dB below the fundamental frequency at a 400-W output. Furthermore, the unit delivers its rated power to any load impedance. In fact, it withstands 100% reflected power continuously without suffering damage or shutdown due to reactive loads or short circuits.



An output meter indicates the average output voltage (calibrated in root-mean-square values) and the output power when connected to a 50-Ω load. A power supply and a ducted forced-air cooling system are built in.

Designed for ease of maintenance, the A500 consists of modular assemblies, subassemblies, and printed-circuit cards. All major subassemblies are easily accessible for replacement or testing without the need for special tools.

The amplifier is suitable for mounting in a 19-in. rack or cabinet. Rack-mounting adapter units and slides are available as options.

The A500 is priced at $8,950. Delivery takes 60 to 90 days.

Electronic Navigation Industries Inc., 3000 Winton Rd. South, Rochester, N. Y. 14623. Phone (716) 473-6900 [401]

Switches combine waveguide and coaxial assemblies

The WR-137 dual-waveguide switches for the 5.925-to-6.425-GHz band were made to help designers use the least number of components within satellite communications systems. The dual switches offer a 1.05:1 maximum voltage standing-wave ratio, a maximum insertion loss of 0.025 dB, and minimum isolation of 90 dB. The waveguide portion of

the switch can handle a maximum of 10 kW clockwise and has a 1.25:1 maximum VSWR. The coaxial portion has a 0.3-dB maximum insertion loss and 60-dB minimum isolation. The switches range in price from $850 to $1,100 in small quantities. Delivery is from two to eight weeks.

Logus Mfg. Corp., 22 Connor Lane, Deer Park, N. Y. 11729. Phone (516) 242-5970 [403]

Fiber-optic units handle 290-nm to 2.5-μm sources

The A-5000 and A-5100 series of input and output assemblies for use with optical fibers can handle wavelengths ranging from 290 nm through 2.5 μm at continuous power levels exceeding 100 W. The A-5000 input assemblies may be used with virtually any light source. Light input over a narrow angle gets converted into a converging beam that matches most fibers having a numerical aperture of 0.22 or more. The A-5100 output assemblies produce a collimated, converging, or diverging beam. Efficiencies for both types of assembly may reach over 90% when they are used properly.

Prices range between $135 and $275, depending on which unit is chosen. Both series are available from stock to three weeks.

Math Associates Inc., 6 Manhasset Ave., Port Washington, N. Y. 11050. Phone (516) 944-7050 [404]

Termination-insensitive mixer covers 1 to 7 GHz

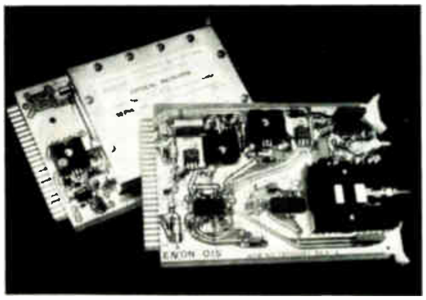
A biasable termination-insensitive mixer operates at 0-dBm local-oscillator drive and covers the 1-to-7-GHz region of the spectrum. The model MD-163 exhibits a conversion loss of 7 dB typically, 9.5 dB maximum. The mixer also has a 1-dB compression point of −2 dBm and a third-order intercept of +8 dBm.

The MD-163 is available with flatpack or SMA connectors for $550 or $630, respectively. It is delivered from stock.

Anzac Div., Adams-Russell Inc., 80 Cambridge St., Burlington, Mass. 01803. Phone (617) 273-3333 [405]

Electro-optical set transmits, receives at 150 megabytes/s

Without using repeaters, the 5100 series of emitter-coupled-logic–compatible electro-optical transmitter-receiver sets communicate data at 150 megabytes/second over 5-km-long standard fiber-optic cables. What's more, they do so with bit-error rates that are better than 1 in 10^9. The solid-state devices operate over 12 km at 50 megabytes/second at the same error rates, and even further if a higher error rate is tolerable. The 150-megabyte/second rate, made possible by the use of



semiconductor lasers, is compatible with the maximum required output rate of most data-concentrating and -formatting computers used in distributed-processing networks.

The transmitter's modulated optical power is greater than 1 mW peak to peak, with rise and fall times of less than 1.5 ns. The receiver comes in two versions, with sensitivities of either −21 or −35 dBm at the maximum data rate. A complete set sells for $2,500, and delivery is from stock to five weeks.

Optical Information Systems, Exxon Enterprises Inc., 350 Executive Blvd., Elmsford, N. Y. 10523 [406]

GaAs FET amps limit output to ± 1.00 dB

Designed for signal-processing applications in the 1-to-2-GHz band, the AML-2000 series of gallium arsenide field-effect-transistor amplifiers are output-limited devices whose output power can be centered anywhere between +6 and +12 dBm and remain constant to within ±1.0 dB over a 35- or 43-dBm range of input signal levels. The pulse rise time is 25 ns.

Designated AML-2004 and AML-2005, respectively, these devices' limited-output power capability ensures the correct drive level to virtually any instantaneous-frequency measurement discriminator or other signal-processing subsystem. Both amplifiers offer a maximum signal-to-noise figure of 4.0 dB and ±1.0 dB flatness. They sell for under $1,500 in small quantities. Delivery takes 120 days after receipt of order.

Avantek Inc., 3175 Bowers Ave., Santa Clara, Calif. 95051 [407]

The foremost solution
to monolithic capacitor performance with disc economy...

Ultra-Kap® Ceramic Disc Capacitors

from

CENTRALAB

When you're selecting capacitors for low-voltage, high-frequency applications, Centralab's Ultra-Kap ceramic disc is the economical alternative to more expensive film, tantalum and multi-layer ceramic types. Look at the specs and you'll find that when you can't afford the performance characteristics of an X7R monolithic, but your circuit demands better stability than a hi-K dielectric ceramic disc, the Ultra-Kap is the answer. It will provide the stability and ceramic reliability you need at a reasonable price.

With Ultra-Kap, you get a non-polarized, temperature-stable capacitor with excellent high frequency characteristics and a small package size. You get the kind of ceramic reliability that's been proven in many types of severe environmental and other demanding applications.

They're available in a wide variety of lead configurations and are offered with your choice of tape and reel packaging for automatic insertion. Standard sizes and values are stocked for off-the-shelf delivery by over 200 Centralab Industrial Distributors.

Discover the foremost source for your ceramic capacitor requirements. Call your Centralab Representative, Industrial Distributor or write Centralab, Inc., a North American Philips Company, 5855 N. Glen Park Road, P.O. Box 2032, Milwaukee, Wisconsin 53201.

Circle 174 on reader service card

Packaging & production

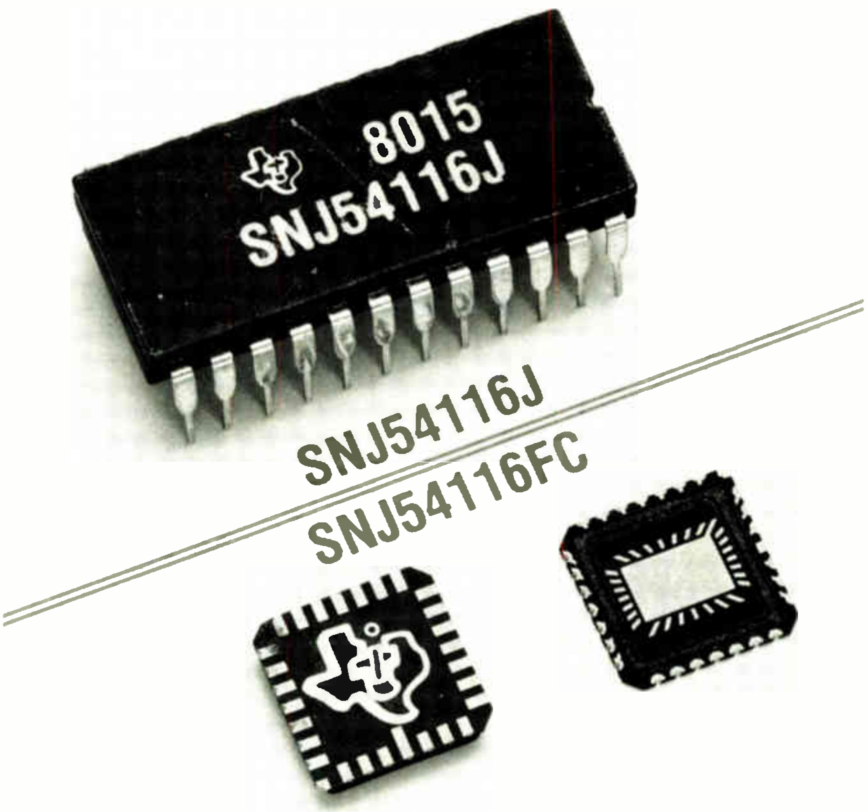
Chip-carriers meet new Jedec spec

Broad range of devices available in volume should bring cost down rapidly

By the end of the decade, leadless chip-carriers are expected to replace today's standard dual in-line package as the dominant packaging form for integrated circuits [*Electronics*, July 3, p. 45]. The driving forces include smaller size, less weight, and potential cost savings associated with chip-carriers. Smoothing the road is the growing unwieldiness of DIPs as very large-scale integration carries pin counts beyond the 40 to 68 required for today's most complex devices. And to add impetus, last April the Joint Electron Device Engineering Council approved a standard footprint for chip-carriers with input/output terminal-pad counts ranging from 16 to 156.

Among the first of the IC manufacturers to make a broad product offering in the new Jedec-approved package is Texas Instruments. The company, a major participant in Jedec activities aimed at establishing the chip-carrier standards, now offers its Schottky, low-power Schottky, advanced Schottky, and advanced low-power Schottky product lines in Jedec-standard ceramic chip-carriers.

In all, some 2,000 products are offered mounted in either the 20- or the 28-terminal-pad version of the Jedec leadless type C ceramic chip-carrier, says Dennis Gaetano, field sales marketing manager in TI's military products department. Compared with equivalent DIPs, the chip-carriers save space and weight. For example, a 24-pin DIP measures 1.25 by 0.6 in., occupies a 0.75-in.[2] board area, and weighs 1.37 grams. The 28-pin chip-carrier that houses 24-pin circuits measures 0.45 by 0.45



in., takes up 0.203 in.^{2} on a board, and weighs only 0.13 g.

Savings. Whereas a DIP contains two parallel rows of pins that have centers 100 mils apart for socketing into standard printed-circuit boards, TI's chip-carrier is leadless and square, with terminal contacts on all four sides that are designed for direct attachment via reflow soldering. The type C version offered by the company is one of four leadless Jedec carrier types that have 50-mil-center contact spacing with a footprint aimed at compatibility with 100-mil-center pc boards. The Jedec standard also covers some leaded 50-mil-center chip-carriers, as well as a family of 40-mil-center packages intended to meet the military's need for the highest possible packing density. The 40-mil-center chip-carrier designs, however, are not suited for easy use with conventional 100-mil-center board applications.

Though leadless chip-carriers are designed for direct surface mounting, the differing thermal expansion coefficients between .the ceramic used in the package and the epoxy surface of today's conventional pc boards could cause stress on solder joints. This difference could result in unreliable connections or, in the extreme, soldered packages popping off the board.

Other materials. A number of firms are looking for more cost-effective board materials having a closer thermal match that would allow direct soldering of ceramic carriers. But in the meantime, Gaetano expects that most users initially will attach chip-carriers to a small ceramic motherboard, which will in turn plug into a pc board in single or dual in-line fashion.

As a new, still low-volume packaging technology, ceramic chip-carriers are significantly higher-priced than equivalent DIP circuits. Current TI carrier pricing on gate and flip-flop devices is typically eight times higher than the same circuit in DIPs, says Gaetano; simple and complex medium-scale integrated circuits are lower, but still about three times more costly.

However, company officials are quick to predict that ceramic chip-carrier costs will fall rapidly as demand increases. Pricing should reach parity with Cerdips by 1985, they feel, with savings at the system level coming much sooner than that as a result of reductions in the number of boards required. For applications not requiring a hermetic seal, the expected introduction of plastic carriers conforming to the Jedec footprint will likely further cut costs.

About 65 types of Schottky and low-power Schottky circuits are available in chip-carriers off the shelf from TI. In 100-piece quantities with standard −55°-to-+125°C hermetic levels, these products are priced at $5.65 each for gates, $7.06 for flip-flops, $8.19 for simple MSI designs, and $9.10 for complex MSI units.

Texas Instruments Inc., P. O. Box 225012, Mail Station 911, Dallas, Texas 75265. Phone (214) 995-4553 [391]

Wrapped-wire panel accepts most DIPs

The model 347 universal wrapped-wire panel can hold nearly any dual in-line package in use, according to the manufacturer. Up to 469 devices can fit on a panel area measuring 15.85 by 14.90 in. The panel handles devices with leads on 0.300-, 0.400-, 0.500-, 0.600-, 0.700-, and 0.900-in. centers. It has two voltage planes plus ground and uses five 108-pin connectors for high-density input and output. The version with gold-plated pins sells for $1,193.83; with tin plating, it sells for $984.61. Both prices are for from one to nine units. Delivery is from stock to two weeks.

Mupac Corp. 646 Summer St., Brockton, Mass. 02402 [393]

System expands capabilities for LSI in-circuit testing

The Data Director is intended for tests of complex large-scale integrated devices that require sequential stimuli of enable, clock, and other control lines, as well as manipulation of data and address buses. The tester is designed to be used in conjunction with the Troubleshooter 800 in-circuit inspection system. Testing flexibility is attained through a high-level language that allows the programmer to talk to a

device with its own mnemonic instructions. The programmer uses the Data Director to design and implement tests at a level understandable to the user.

The Data Director consists of a controller and an operating system, plus one or more driver-receiver cards. Each card supports eight data lines and eight control lines to allow the Director to segregate control and data functions. The basic price of the Data Director is $10,000 plus $2,000 per 16 pins (8 for data, 8 for protocol). Delivery is scheduled to begin in early 1981.

Plantronics/Zehntel, 2625 Shadelands Dr., Walnut Creek, Calif. 94598. [394]

Components

1,400-V SCR unit switches at 50 kHz

10-μs turn-off time and 200-A peak current should benefit power inverters

The 20-kW switching power supplies used by industry for a variety of applications such as resistance welding, ultrasonic equipment, and 400-Hz uninterruptible power supplies might be far more efficient and economical if they could be connected directly to the 220- or 480-V ac line, through a semiconductor inverter. By doing away with the usual bulky step-down transformer, the size and weight of the supply would be greatly reduced, along with its cost.

Unfortunately, inverters fast enough to work with high-power switching supplies have not been available. The best components, typically silicon controlled rectifiers, have the 1,200-V reverse-breakdown rating needed, but their generally slow turn-off times of 10 seconds or longer do not make them compatible with the needs of high-frequency switching power supplies.

General Electric seems to have licked this problem with an SCR that operates asymmetrically to achieve turn-off times of 10 μs. A gate-assisted turn-off device, the CA386 operates between 10 and 50 kHz. Capable of passing 200-A peak currents when switching at 20 kHz (at a 50% duty cycle and 85°C case temperature), it is intended for use with switching power supplies that operate at 20 to 50 kHz.

Specs. Seven versions are available, each with a different blocking-voltage rating. The highest-rated device is the CA386PD, with a blocking voltage of 1,400 V; the lowest is the CA386N, with an 800-V rating. Between are five others with blocking voltage ratings in 100-V increments. All have repetitive peak reverse ratings of 10 V.

Turning on the SCR requires a 5-V (peak) source having a 1-μs rise time. When switched at a 20-kHz rate, the CA386 dissipates a maximum of 400 W, assuming the use of an RC snubber network of 5 Ω in series with a 0.05-μF capacitor.

Other parameters include a di/dt rating of 800 A/μs (nonrepetitive) and 500 A/μs (repetitive) and gate power dissipation of 25 W. Further, the unit operates over the temperature range of $-40°$ to $+125°$C.

Like most SCRs, the CA386 should be coupled with a diode in an antiparallel arrangement when applied as an inverter. The diode handles reactive load currents and limits voltage ringing. The A393 fast-recovery diode is supplied for those purposes as a companion component.

The CA386, with the A393 diode and a mounting hardware kit, sells for $200. A mounting force of 800 lb is required to heat-sink the Hockey Puk–type device properly. Availability is from stock.

General Electric Co., Semiconductor Products Department, Electronics Park, Syracuse, N. Y. 13221 [341]

Charged particle preamp has 1-ns rise time

Measuring only 2 in. in diameter by 1 in. high, the H242 charged-particle preamplifier has a rise time of 1 ns. The manufacturer says the unit is about one third the size of previous models and its rise time is about five times faster than that of conventional preamps. It is intended for silicon surface-barrier detectors and sells for $660. Delivery time is 60 days, though this time is expected to shorten in the future.

EG&G Ortec, 100 Midland Rd., Oak Ridge, Tenn. 37830 [344]

Optocoupler unit operates from $-55°$ to $+100°$C

The H11G is an optoelectronic device that consists of an epitaxial gallium arsenide infrared-light–emitting diode optically coupled to a Darlington-connected phototransistor. Operating over the temperature range from $-55°$ to $+100°$C, it has a breakdown collector-to-emitter voltage of up to 100 V with a 2,500-V root-mean-square isolation capability. Ten mA of the IR diode current will switch a load of 100 mA in the Darlington. The H11G can switch solenoid loads from low-level inputs. It sells for 77¢ each for 1,000 units.

General Electric Co., West Genesee St., MD-14, Auburn, N. Y. 13021 [345]

Instruments

System DVM is complete in itself

6½-digit unit has store for multiple measurement routines

The term "system DVM" usually applies to a high-accuracy digital voltmeter intended for use in a larger system. While the latest DVM from Guildline Instruments Inc.—the Datastore 9576A—fits that description very well, it also is a complete measurement system in itself. On its own, it can perform preprogrammed measurement manipulations for which other units require a separate controller. "With all the data-processing capability we've put into the unit," says Ed Nemeroff, Guildline vice president of sales, "the user doesn't need anything else."

The 6½-digit unit is the next step up from Guildline model 9576. Like the earlier model, it has 26 preset routines that the user can call at the press of a button—routines that do statistical analysis, offset subtraction, thermocouple linearization and temperature conversion, and various common ratios such as power, to name a few. And like the 9576, the 9576A has a basic dc voltage accuracy of ±0.0004% of reading on the three lowest of its six ranges (10 and 100 mV and 1, 10, 100, and 1,000 V) and it can take ac voltage and resistance readings as well.

What gives a big boost to the power of the new unit is a memory facility and a new preset routine. The memory facility stores the latest 50 displayed readings automatically, gives an extra 25 locations for use as a scratchpad, and provides 5 more locations for program store. The new preset routine, polynomial evaluation, permits selection of four constants for a standard third-order polynomial ($c_0x^3 + c_1x^2 + c_2x + c_3$) and each of those constants can be the output of one of the preset routines or a user-entered number.

A measured value or constant can be stored in any of the 25 scratchpad locations. For example, the offset of a strain gage can be measured and stored in the scratchpad. Later, when strain readings are taken, this value can be applied to the measurements by the offset routine.

The DVM can be set to automatically take, for example, 10 readings at 1-second intervals and apply to them a program string of up to three preset routines with stored constants. Once initiated, the meter will take and manipulate the readings and store them in one of the five program locations that the user has selected. A separate program or program string can be used to enter data into each of the five locations, and the results can be recalled and examined later. "Effectively," notes Nemeroff, "you have five different instrument systems in one."

The basic unit, which sells for $4,995, can also be equipped with a $995 interface option that provides both RS-232-C and IEEE-488 ports. Using either of those ports, the unit can be attached to a dumb printer so that all the displayed readings are automatically recorded.

For building even more sophisticated systems, a scanner—the Minate 7010 is also offered. The $2,195 unit has 16 analog input channels, each consisting of four terminals plus a guard, which can be selected individually by the operator or scanned sequentially.

Deliveries can be made from stock to 30 days.

Guildline Instruments Inc., 2 Westchester Plaza, Elmsford, N. Y. 10523. Phone (914) 592-9101 [351]

Active low-pass filter is versatile, costs $299

A $299 active low-pass filter for laboratory and field applications offers a comprehensive choice of functions that can be selected from the front panel. The model 901F, an active eight-pole Butterworth filter, has corner frequencies variable from 0.1 Hz to 29.9 kHz. Three rotary dials set the first three digits of the frequency, and a fourth dial multiplies by a scale factor of 0.1, 1, 10, or 100. One unusual feature of the unit is a differential input amplifier to eliminate long-line ground-loop problems.

New products

The instrument is available in a line-powered version, but a battery option with an internal charger that provides uninterruptible power is also available for an additional $100. The 901F is available within eight weeks after the receipt of an order.

Frequency Devices Inc., 25 Locust St., Haverhill, Mass. 01830. Phone (617) 374-0761 [354]

Hand-held DMM selects range automatically

Using its microcomputer to provide autoranging, the 3½-digit model 2845 multimeter offers a basic accuracy of within 0.1% on its four dc measurement ranges—±1, ±10, ±100, and ±1,000 V, with automatic polarity indication—±1 least significant digit. On the ac ranges, accuracy varies depending on voltage and frequency. In the 1-to-100-V range it is to within ±0.5% between 50 and 500 Hz, to within ±1.0% between 500 Hz and 1 kHz, and to within ±12% between 1 and 5 kHz. For measurements in the 1,000-V range and between 50 and 500 Hz, accuracy is within ±1%. For ac, resolution is ±3 least significant digits.

The input impedance on ac and dc ranges is 10 MΩ. Resistance measurements cover five ranges—1 kΩ, 10 kΩ, 100 kΩ, 1,000 kΩ, and 10 MΩ—accurate to ±0.3% ± 1 least significant digit for the 1-kΩ through 1,000-/kΩ ranges and ±0.6% ± 1 LSD on the 10-MΩ range. Circuit protection is ±1,000 V to −450 V dc or 300 V ac.

Delivery is from stock at $175 each.

B&K-Precision, Sales Department, 6460 W. Cortland St., Chicago, Ill. 60635. Phone (312) 889-9087 [358]

Pπceon promises controller for 5¼-in. hard-disk drive

A low-cost single-board controller for 5¼-in. hard-disk Winchester drives is in the final stages of development at Pπceon Inc.'s OEM Computer Products division in San Jose, Calif. Designated the D-100, the controller board is expected to be available in the first quarter of 1981 and have the flexibility for **controlling both 8-in. and 5¼-in. drives.** The board will interface the drives via the S-100 bus with Z80, 8080, 8086 and Z8000 microprocessors for about half the price of the drive, which sells in the $700-to-$750 range.

AMI readies C-MOS uncommitted logic arrays

American Microsystems Inc., Santa Clara, Calif., has almost completed development of a line of complementary-MOS uncommitted logic arrays, the first of which may be brought to market by the end of this quarter or early next quarter. The ULA family will be offered in six configurations, with circuit complexities equivalent to **as few as 300 and as many as 1,260 two-input gates.** The C-MOS process used for these devices is AMI's 5-μm oxide-isolated, silicon-gate approach [*Electronics*, Sept. 13, 1979, p. 116], which offers dense circuits with high performance, in addition to all the other conventional advantages of C-MOS.

Report lifts veil on Hitachi's 4-K C-MOS RAM

Well-known for its analytical reports on n-MOS random-access memories, Mosaid Inc. has expanded its services to include advanced complementary-MOS parts. Its latest report, on Hitachi's HM6147, contains **a complete circuit diagram of the 4-K-by-1-bit C-MOS static RAM** with transistor dimensions pointed out, a process analysis, and a commentary on the validity of the circuit concepts used. Copies of the report are available from the Ottawa, Canada, company for $3,000 each or as part of an annual subscription service that costs $15,000.

TI offers TMS 9900 in 15% cheaper plastic DIP

Texas Instruments Inc. has begun selling its 16-bit TMS 9900 microprocessor in a plastic 64-pin dual in-line package, offering a 15.8% savings over the Dallas company's standard 64-in. ceramic DIP. **The standard 3-MHz machine, designated TMS 9900NL, is housed in plastic and sells for $26.30** in 100-unit quantities. The 4-MHz part, designated TMS 9900NL-40, is priced at $42.10 in plastic. Cerdip versions go for $31.25 and $50, respectively, at the 100-unit level. TI already offers the 8-bit data-bus version of the 9900—the TMS 9980—in a plastic package.

Honeywell raises computer sales, rent, and service prices

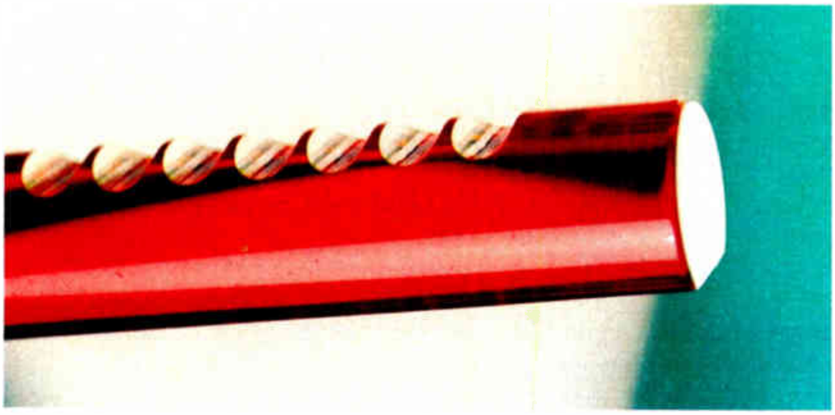
Price increases ranging from 5% to as much as 19% have been posted by Honeywell Information Systems Inc., Waltham, Mass. The firm is implementing **5% increases on its level 62 and 64 and series 60 large computers** and related equipment, as well as on most of its data-net front-end processors. Leases and rentals for DPS 8 add-on memory subsystems will rise by 10%, as will monthly costs for maintenance of peripherals for these systems and system engineering for all Honeywell computer products. On-call field engineering services will cost from 12% to 19% more. Finally, some software package prices have been upped by 10%.

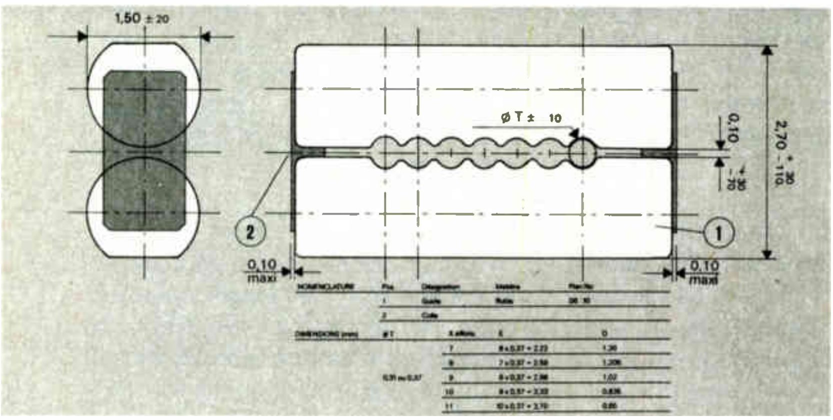
New product, lower cost

Seitz

Seitz, c'est sûr !

Wire-guide bars for printing heads





All kinds of material have been tried out for the manufacture of wire-guide bars. The corundum in single crystal structure ($Al^2 O^3$) still remains the best one. Seitz knows it and uses it in an economic and intelligent way.

The form: a cylindrical bar, which means reduction of friction, improvement of the ribbon guiding, elimination of the wear of the head.

Application: in every type of head, thanks to the rigorously respected dimensions and tolerances.

Seitz is the pioneer of wire-guides and is furthermore the most important manufacturer of this product. Seitz has created and fixed its norms.

Seitz wire-guide bars: A technical and economic solution.

Design Borel

Seitz SA, CH-2416 Les Brenets, Tél. 039/321112, Télex CH 35505 SEITZ

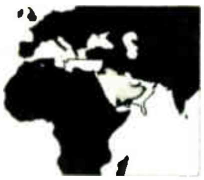
Circle 182 on reader service card

Pierres Holding, Faubourg du Lac 6, CH-2501 Bienne
Téléphone 032 / 22 65 11. Télex 34 566

Abqaiq, Saudi Arabia

No baseball, no morning paper, no pizza, no autumn leaves.

But here's the great life that makes Aramco people stay on and on.



If you never considered working in Saudi Arabia because you think it's all sand and hardships, consider this.

3,900 Americans like you work for Aramco in Saudi Arabia now. Ask them why they stay and they'll tell you that, besides money, it's the casual lifestyle, American-style hometowns, top-notch schools, and vacation travel they used to only daydream about.

Where on earth is Abqaiq?

Located close to the world's largest oil-field (Ghawar), Abqaiq is the center of a giant oil-gathering and processing system that handles 60% of all the oil produced by Aramco, the world's largest producer.

Does Aramco's paycheck justify living in a desert kingdom?

Yes! You get a base salary competitive with top U.S. oil firms. We compensate you for overseas cost-of-living differences.

On top of that, Aramco pays an **incentive of up to 40%** for overseas employment, and you are reimbursed for any foreign or U.S. Federal income tax on the premium. So your premium is tax-protected.

Another benefit: employees overseas participate in Aramco's Retirement Income Plan on an **accelerated** basis.

With this financial package, no wonder 3,900 Americans like you work for Aramco in Saudi Arabia today.

What can you do with all that money stuck out in the desert?

Aramco people use 40-day paid vacations (every 12½ months) and 12 paid holidays (average) to visit fabulous places like the Pyramids, Greek Islands, Mt. Everest, the Serengeti Plain, Hong Kong.

Aramcons vacation in Asia, Africa, the Middle East and Europe

Doesn't a child's education suffer so far away?

No! Aramco has a modern American school system. Teachers are primarily American and more than 75% of them have master's degrees. The teacher-student ratio is 1 to 15 in grades 1 to 6; 1 to 20 in grades 7 to 9.

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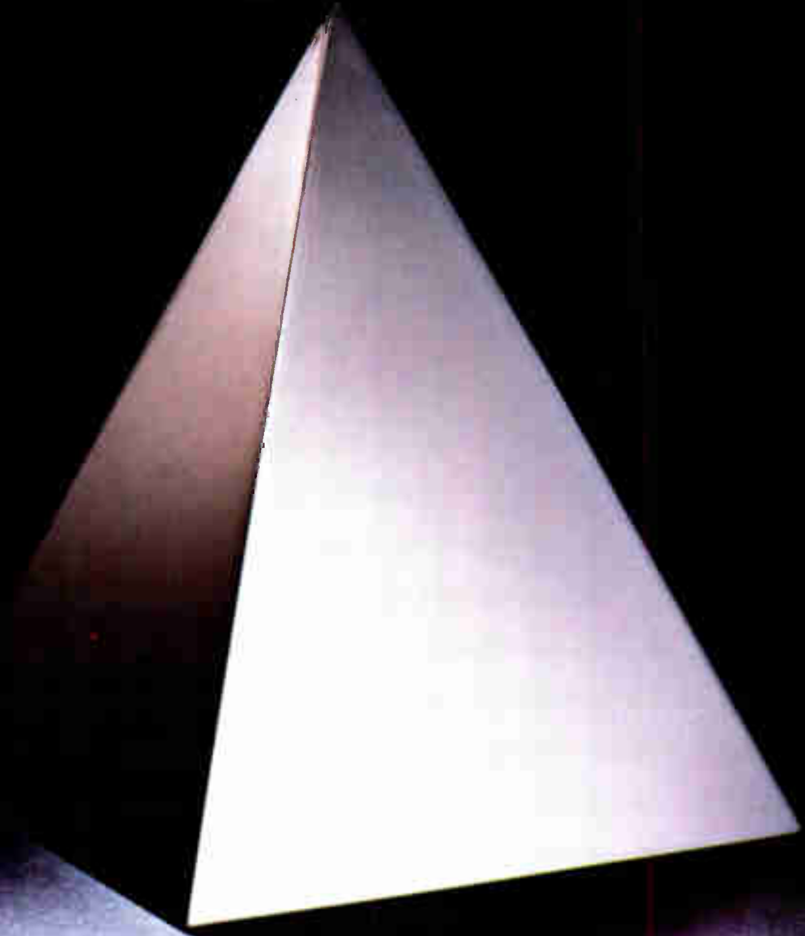

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