JANUARY 31, 1980

FLAT-PANEL DISPLAYS FINDING THEIR NICHE/67

Programmable controller fits many peripherals/93

Analog microcomputer chip tackles speech synthesis/102

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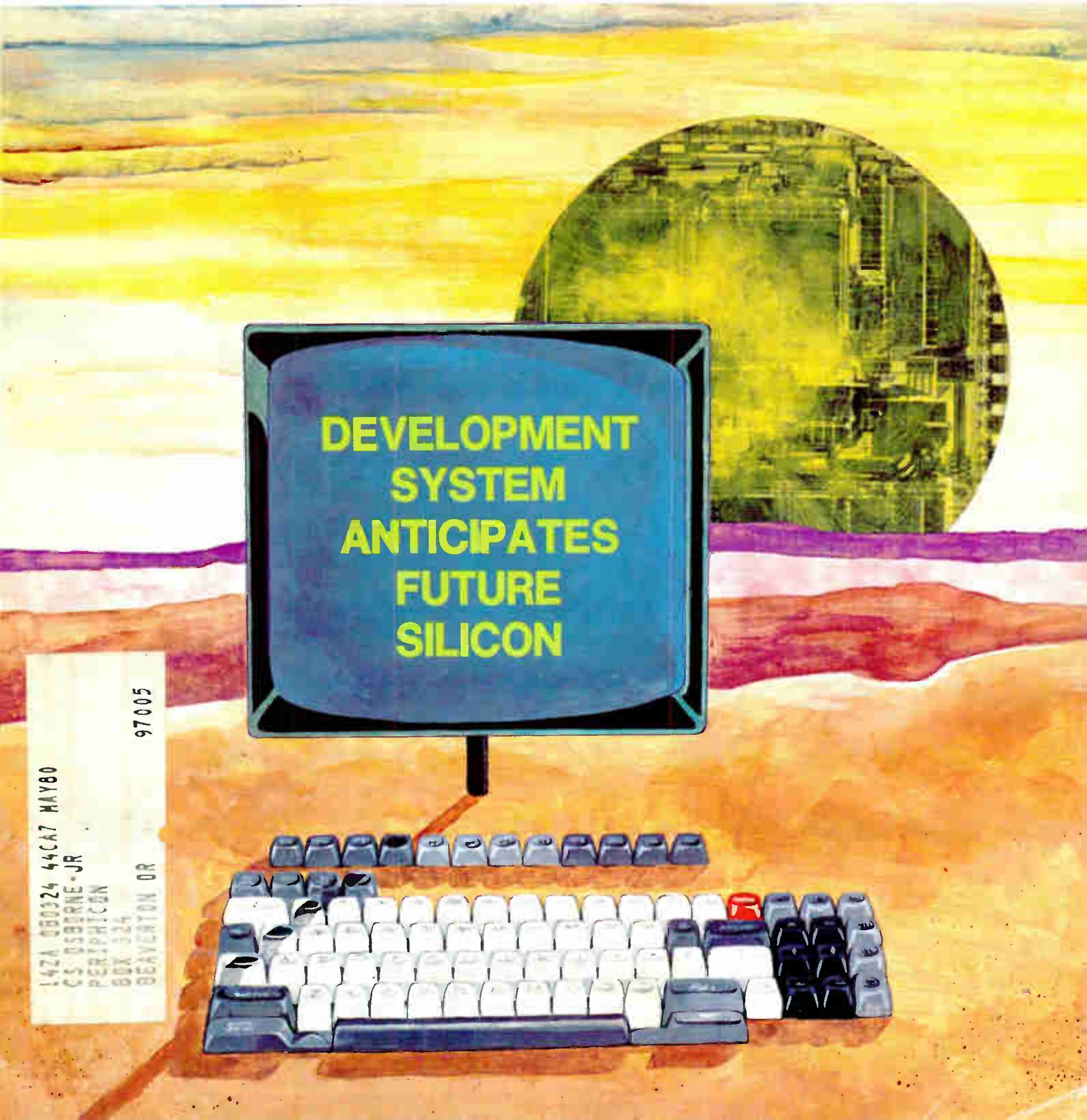

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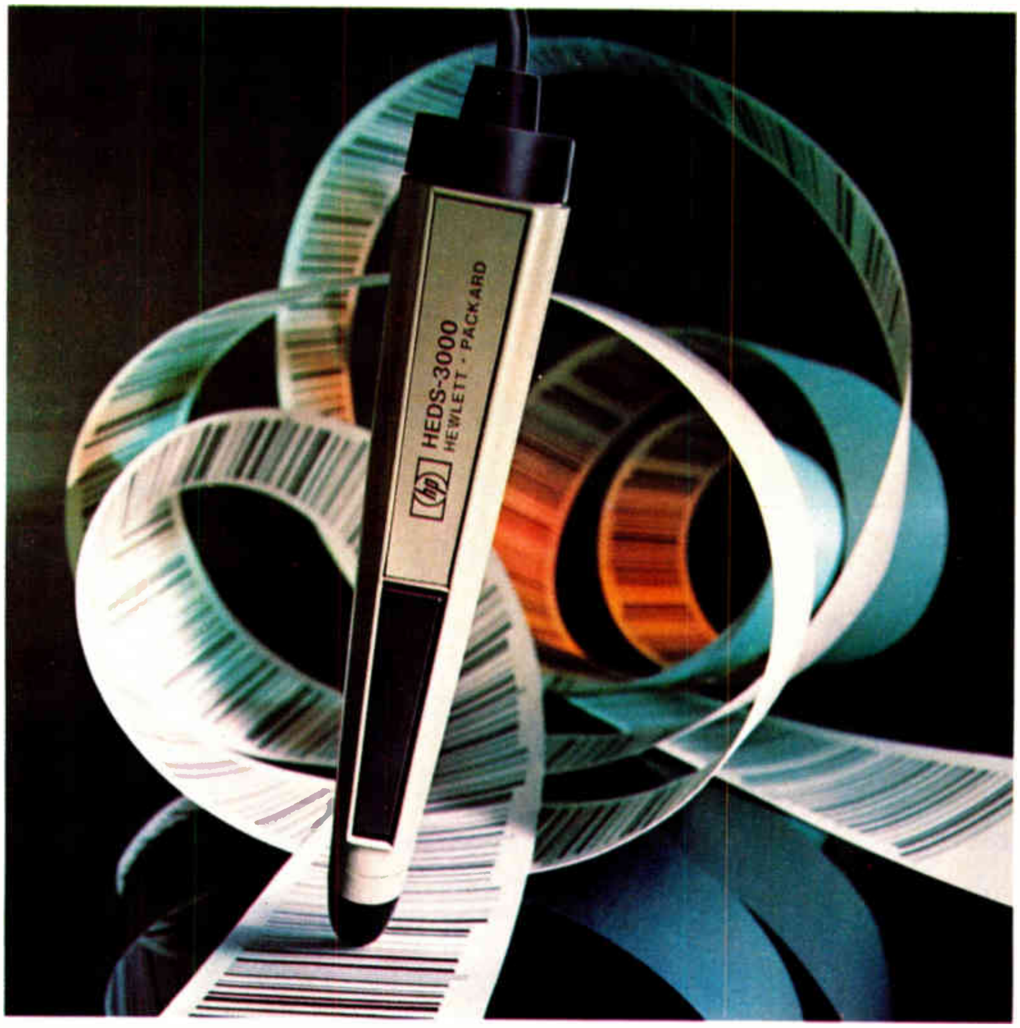

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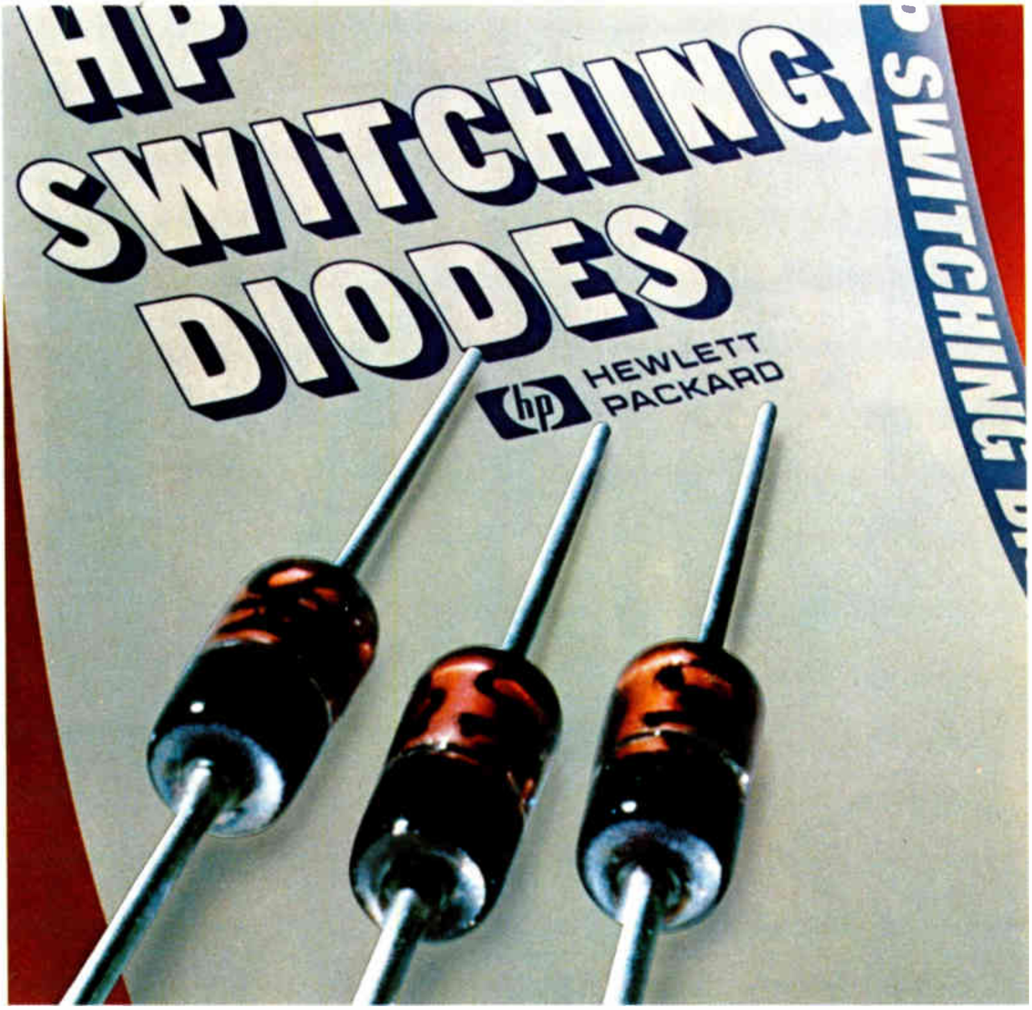

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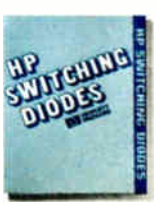

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Electronics

The International Magazine of Electronics Technology

Vol. 53, No. 3 January 31, 1980

Electronics

Highlights

Cover: Development system stands ready for 32-bit chips, 81

With the dust still settling from the electronics industry's first march into 16-bit microprocessor territory, advance scouts are bringing back reports of powerful new chips. Motorola's 68000 processor has 32-bit internal buses, and it won't be long before improved packaging schemes allow the wide buses to emerge from their silicon confines. The company is getting the jump on development system needs by introducing an EXORmacs system that's ready for the next generation of processors.

Cover is by Art Director Fred Sklenar.

Will 1980 be the year of the home computer? 70

A number of prognosticators said it would happen in 1979. It didn't. Now some of the same voices are reverberating with predictions that the consumer market for small "personal" computers will quadruple in 1980. Significant new entries in the field might encourage such optimism, but other small-machine makers are getting out.

E-PROM rides piggyback on emulation aid, 89

One-chip microcomputer prototypers impatient with the compromises and clumsiness of using emulation boards in the field may have found just what they've been looking for. It's a version of the microcomputer, with operating characteristics matching those of the final chip, packaged with a socket on top for erasable programmable read-only memory.

Crowded peripheral controller resorts to I²L, 93

Peripheral makers aren't far behind computer manufacturers in the application of large-scale integration. So that it might occupy a slot in a specific minicomputer, a programmable peripheral controller has been made with four custom integrated-injection-logic chips, a microprocessor, and a dense 7-by-9-inch printed-circuit board.

There are ways to make a microcomputer talk, 102

Specialized speech-synthesis chips are stoking demand for talking consumer electronics, but they're not the only slices of verbal silicon around: the 2920 microcomputer's speed and analog input/output make it an able speaker, given suitable software.

. . . and in the next issue

Systems on chips, enormous memories wow ISSCC attendees . . . a one-chip processor emulates a high-end minicomputer . . . how to build a 60-watt switching power supply for $37 . . . a contact temperature probe's design affects its accuracy . . . a dual-processor measurement system raises the art of interruption to new heights.

January 31, 1980 Volume 53, Number 3 102,650 copies of this issue printed

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Circle 5 on reader service card

Publisher's letter

Dallas bureau manager Wes Iversen was born and raised in Council Bluffs, Iowa. But darned if he isn't starting to sound and act more like a Texan every day. His Letter from Dallas appears on p. 69.

This letter is the first in a continuing series of regional reports on the electronics industry to be written by our bureau editors.

Wes does some Texas-style bragging about how this region is fast becoming a major electronics center not only for semiconductor producers, but for computer hardware companies as well. Judging from the employment statistics, these observations may be more than just bragging.

The lure of wide open spaces, favorable tax policies, and moderately priced housing have made Texas a prime location for electronics firms. Not to be overlooked in the stampede of newcomers is that the oldest electronics tenant on the range, Texas Instruments, has also been expanding, and attracting hard-to-hire engineering talent to what Wes calls "silicon prairie."

The eyes of Iversen have been upon Texas electronics firms since he joined the staff a year and a half ago. In that time his beat has become busier and busier as major firms have joined the enterprises already growing on the scene. Therefore doing his first letter on this expansion was a natural.

Designing a microprocessor development system for a microprocessor that has not yet been developed poses some problems. As Jack Kister, manager advanced computer support systems for Motorola Inc.'s Semiconductor group in Phoenix, Ariz., puts it: "The difficulty is that there is no development system for the development system. We had to invent new tools, improvise, and use simulation techniques."

Kister, who is co-author of the cover article on Motorola's new EXORmacs development system (p. 81), had another thing going for him when he began work on the project. He had spent two years at Motorola's microprocessor operation in Austin, Texas, as an applications engineer working with the people who were designing the 16-bit MC68000 chip. Being in on the ground floor in Austin was an advantage when it came time to design the development system in Phoenix.

"For the first six months of the project there were no chip characterizations available. We designed the development system without knowing the final ac characterization of the chip," Kister recalls. "It was a big help to be able to call the people I knew in Austin and ask them how things were coming along. It's good to have this cross breeding from the chip to the systems level."

Because there was considerable interest in the 68000 among potential users, a number of them went through Austin to learn about the processor, then went through Phoenix to pass along suggestions on the development system to Kister and his group.

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Circle 7 on reader service card

Readers' comments

More costly circuits

To the Editor: I enjoyed Ernst Wall's article on the Hamming code [Nov. 22, 1979, p. 103]. Wouldn't it be easier, however, to use TI's SN74LS630/631 16-bit parallel error-detection and -correction circuit instead of the circuits the author proposes?

Clinton Jones
Tucson, Ariz.

The author replies: *I would like to comment that, first, the TI chip (74LS630) will only become available this January (we designed the system described in* Electronics *over one and a half years ago); and second, the estimated small-quantity cost of the TI chip is about $55.00. To implement a 16-bit system of the kind described in the article would cost about $30.00 and an 8-bit system about $20.00.*

Who's racing whom?

To the Editor: I am seldom moved to write letters but "Europe races to catch up" [Nov. 8, 1979, p. 94] gave me an incentive. Who is racing to catch whom? It seems to me that the Europeans and Japanese have led the U. S. for years in applying electronics to automobiles, under the hood and elsewhere. They are always faster to apply a new technology than the U. S. auto industry.

I own a 1969 Volkswagen, Type 3, a mass-produced auto that has an electronically controlled fuel-injection engine. What U. S. auto could I have bought in 1969 with any type of fuel injection, much less electronic?

Loy M. Bloodworth
Ellicott City, Md.

Canada's first fiber optics

To the Editor: On page 56 of the Dec. 20 issue, due credit is given to Silma Ltd., Nippon Telegraph and Telephone Public Corp., and Thomson-CSF for their accomplishments. But the absence of any reference to the Canstar division of Canada Wire and Cable Ltd.'s having provided Canada's first industrial fiber-optic link at General Motors of Canada Ltd. is conspicuous.

Brigitte M. Gauthier
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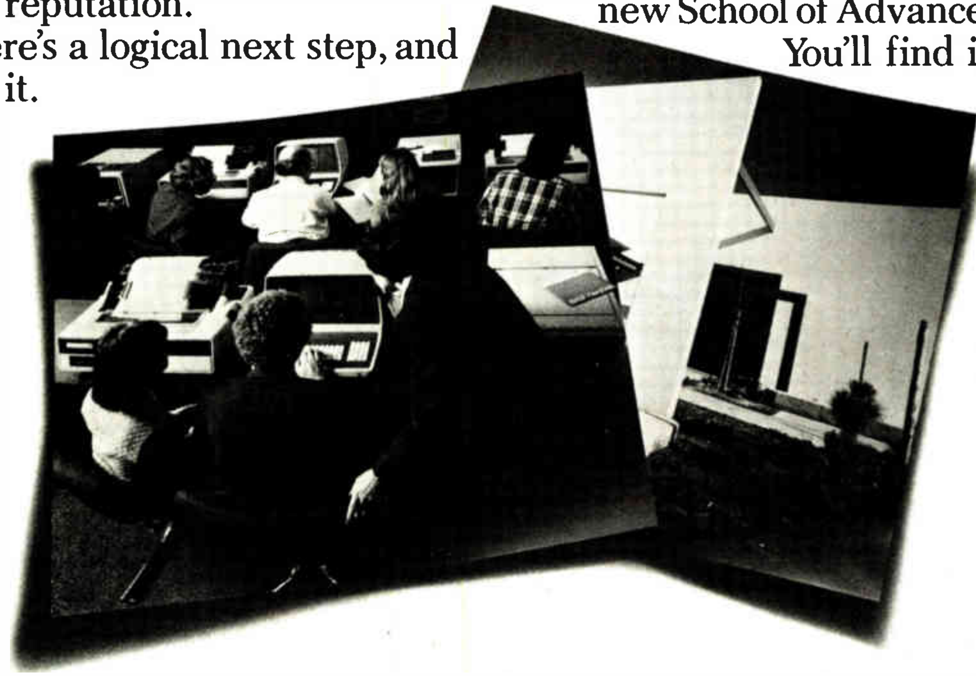

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News update

■ Solid-state electrochromic displays are a tempting target for researchers. Their attractions include completely passive display operation once written into and a pleasing appearance, with deep blue characters being formed on a white ceramic background. Thus, while such displays have yet to emerge from the laboratory, progress is being made at research installations around the world.

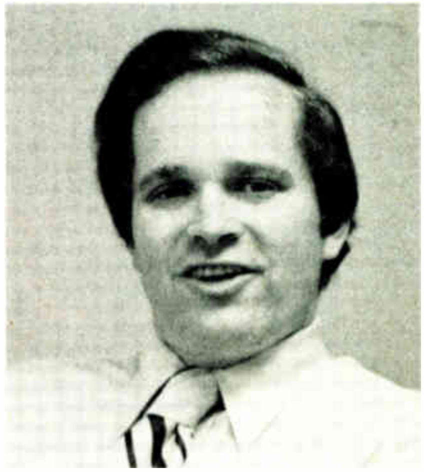
One of the foremost workers in the field is Mino Green, who heads a small team plugging away at the Department of Electrical Engineering of London's Imperial College [*Electronics*, Jan. 18, 1979, p. 67]. A year ago, Green thought he could have a working seven-segment display within 12 months, a development that truly would be a landmark. However, no display has emerged, and "pray God we get around to making one in 1980," says Green. The trouble is that "we are only a small operation, not a big industrial enterprise," he explains, adding that he puts a higher premium on understanding basics. "But I do not see any basic fabrication problem," he says.

In the past year, says the researcher, "we have developed a more detailed knowledge of how these things work," and this has added to his confidence that the technology will ultimately work. "Test cells on life tests have now clocked 10 million operations with no problem at all," he discloses, "and the technology is less power-hungry than we thought: writing takes 2 milliamperes per square centimeter at 0.6 volt."

Read/write time varies from 1 second at room temperature to a tenth of a second at 55°C—a speed that is adequate for line and character display, though it could be improved, says Green. The problem is that the speed is highly voltage-sensitive, but Green believes that difficulty can be solved by finding electrolytes with a lower resistance and by improving the mobility of the sodium ions as they penetrate the tungsten trioxide chromic compound that forms the cell's outer layer, turning it blue. **-Kevin Smith**

People

Kalb brings Silicon Valley outlook to DG engineering



New perspective. Jeffrey C. Kalb will involve semiconductor more in DG plans.

His colleagues agree that Jeffrey C. Kalb, Data General Corp.'s new vice president of engineering, looks like the right man in the right place at the right time.

Kalb comes to the headquarters of the Westboro, Mass., firm from his position as head of its Sunnyvale, Calif., semiconductor operation. Now he will have the sole responsibility—from the mechanical side of peripheral devices to the software needed to make systems run.

Kalb replaced Carl D. Carman as DG's engineering czar, and he says that he will probably impose a somewhat more structured style on engineering management. "That doesn't mean a clampdown," he is quick to point out. "I like the multidisciplinary team-engineering approach already in use. With so much of life-cycle cost coming to consist of software and support, that seems to be the best way to approach computer systems design. But though I want to allow engineers maximum flexibility and room to innovate, at some point their efforts have to tie into corporate goals."

Thus, "I suspect we will see more product reviews, program definitions, market analyses, etc.," says Kalb, adding, "in fairness to Carl [Carman], I will probably need more of this than he might have; he had a feel for product development based on years of experience."

But the system is different today from when Carman took the position. "He started in when there were less that 100 engineers aboard; now there are more than 500, and many are doing different sorts of things. That simply takes a different form of management. The challenge, as I see it, is to keep engineering productivity high while DG goes through what some are calling a period of growth through change."

The change is nothing more than the company's posturing itself for the new sorts of markets it will face in the 1980s. And with one key trend pointing toward higher-complexity solid-state devices, Kalb, with his Silicon Valley background, seems truly to be a good match for the time and the circumstances.

And, sure enough, he plans to "involve DG's semiconductor group more in the future. Many engineering decisions dealing with architecture, components, and so on relate to semiconductor technology. In some firms, impressions of what is possible are gained only through vendors, and sometimes those impressions are not too accurate. Our Sunnyvale operations will be able to give our East Coast engineers a better feel for realities and the 'what if' impacts of new technology on potential hardware and software."

Young wants IEEE's voice to be a million strong

On Jan. 4, the Association of American Engineering Societies met for the first time to discuss the problems affecting engineers of all disciplines. Representing electronics engineers at that meeting was Leo Young, 53, recently elected president of the IEEE. Young has taken the IEEE into the AAES, in the face of some rank-and-file resistance, because he believes sheer numbers will eventually help get engineers' problems publicly aired and solved. "For instance, if the IEEE is anxious to get something done—say, about pensions—and we

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People

Joiner. President Leo Young feels IEEE will be stronger in new alliance.

say we speak for 150,000 electrical engineers, people listen. But if we say we speak for 1 million engineers and scientists, they will listen a lot harder," he says.

Young, who collected signatures to get on the last IEEE ballot, won on a platform of many planks, all of them supporting the policy that the IEEE has to serve the professional needs of the engineer. "If I could condense everything into one phrase, it would be 'career maintenance'," Young says. "The IEEE is not there just to publish technology—although this is a logical extension of its work. Its emphasis and focus should be on careers, of which technology is the biggest, but not the only, part."

As well as taking the IEEE into the AAES and continuing the fight for pension rights, Young wants to obtain a closer interaction between the various societies within the IEEE, hoping to establish technical cross-ties to give the engineer more flexibility in his career path. "We're going to let the Computer Society run with the ball at first. This technology is more pervasive than others, so we'll see what the computer needs are in some of the other societies," Young observes. "The IEEE has become a bit too compartmentalized. We need connections across the society's boundaries." It looks as if the IEEE will be crossing some boundaries of its own under Young's direction over the next year.

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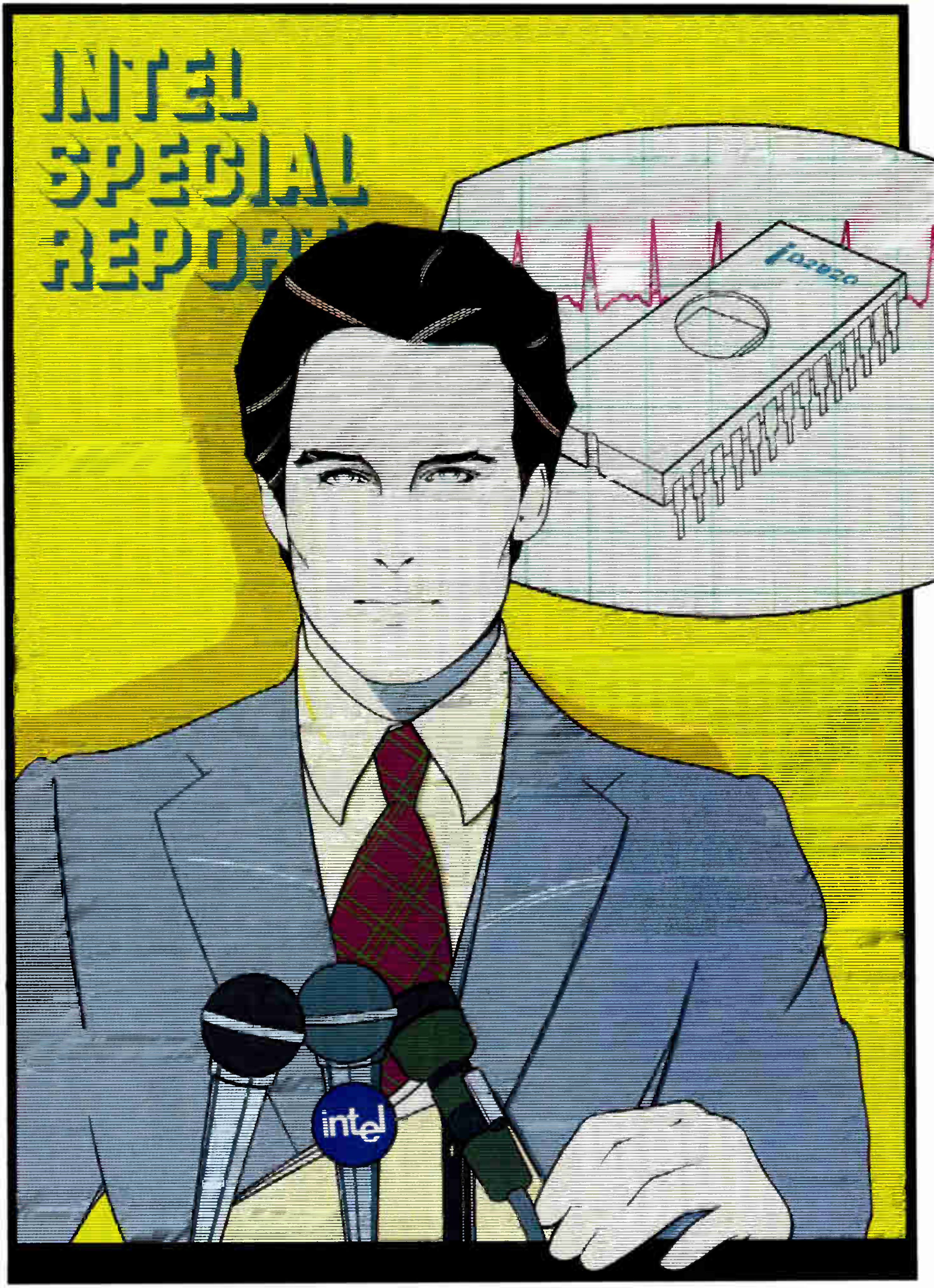

INTEL
SPECIAL
REPORT
intel

LSI Breakthrough for Analog

Intel announces the 2920 Signal Processor, first general purpose, real-time system on a chip.

Good news for analog designers. Intel breaks a new barrier in microelectronics: The first intelligent chip powerful enough to process analog signals in real time. Plus a computer-aided development package to help speed your systems to market faster than ever before.

Intel's 2920 is a complete, micro-sized signal processing system that packs the equivalent of over 18,000 transistors on a single chip. It operates hundreds of times faster than current digital processors. And best of all, the 2920 allows designers to *program* system values quickly, instead of having to match and tweak components.

A revolution in analog design

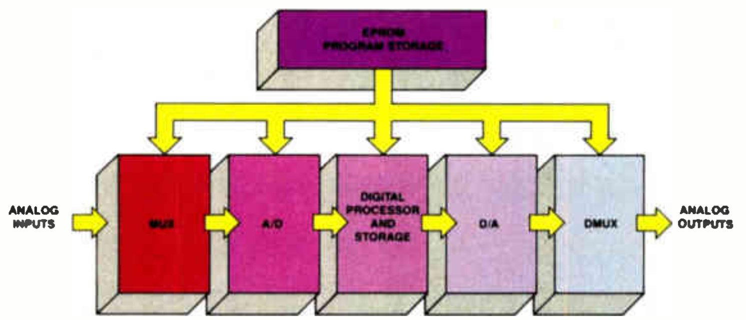
From the beginning, LSI technology has helped designers achieve dramatic improvements in product size, design cycles and manufacturing economics. But until now, the speed and complexity of analog processing has stood in the way of general purpose, single chip solutions for real-time applications.

Today, Intel's 2920 Signal Processor brings the power and flexibility of LSI to the analog world. Because of its size, the 2920 can fit in spaces too compact for traditional analog solutions. Because the 2920 is programmable, product development and time-to-market are speeded significantly. Finally, because the 2920 is a solid state device produced with Intel's proven NMOS process, reliability and manufacturing repeatability are assured to a degree not possible with previous methods.

Micro-processing for the real world

Applications for the 2920 are as broad as your imagination. Since analog designers can program the 2920 processor to perform a large number of standard building block functions, the chip can be used as an entire subsystem. Implement such functions as complex filtering, waveform generation, modulation/demodulation, adaptive processing, and even non-linear functions. This broad capability makes the 2920 an ideal single chip solution for virtually any application in the DC to 10 kHz range.

And like the digital microprocessor, the 2920 is destined to create entirely new classes of applications: products that are smaller, simpler, and less costly to produce. It gives a competitive advantage to companies in such areas as process control, test and instrumentation, guidance or control systems, telecommunications, speech processing, and seismic or sonar signal processing.



Functional Block Diagram of the 2920 Signal Processor

How the 2920 simplifies system development

Programming Intel's 2920 Signal Processor is fast and easy to learn—far less complex than the component matching it replaces. Most importantly, Intel provides the complete support tools and design workshops you need to start designing 2920 systems today.

Our SP20 Support Package and Intel's Intellec® Microcomputer Development System allow you to develop and debug by simulating your system in software. Just program functions according to your system schematic, then specify input and operating values. Together, Intel's development aids let you see how your system will work before you even build a prototype. Best of all, because you develop in digital code, your prototype system will be duplicated precisely in manufacturing.

Start making news with your product

Everything you need to begin designing a new generation of real-time analog processing systems is here today: Intel's 2920 Signal Processor, SP20 Support Package, and the Intellec Development System. For detailed information, including our new 2920 brochure, plus a schedule of Intel's nationwide 2920 Design Workshops and Seminars, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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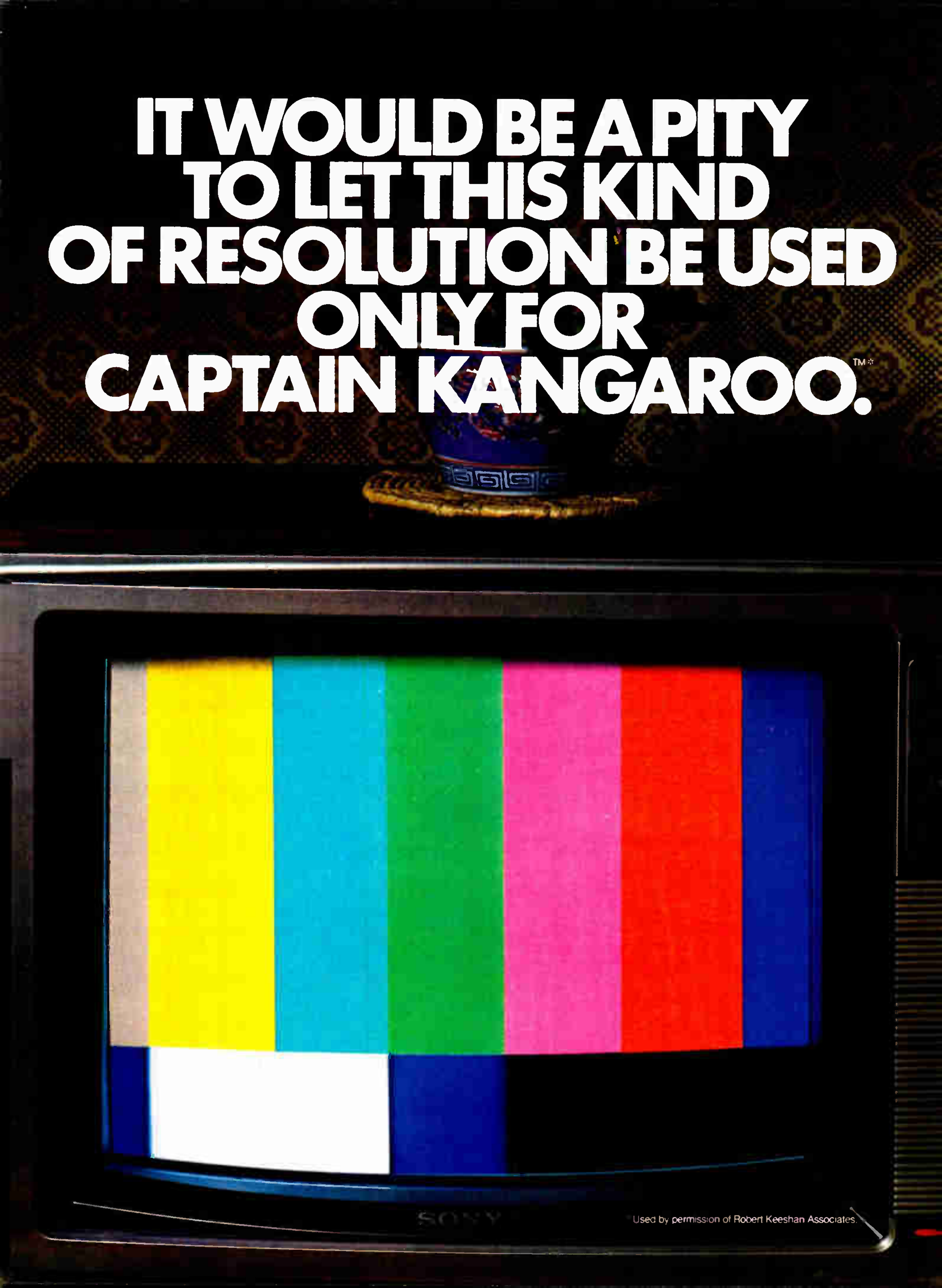
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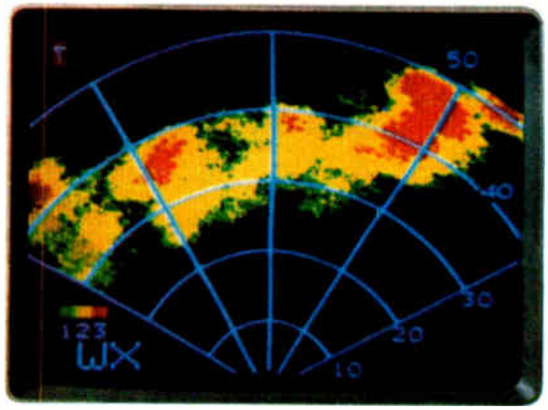
Sony color picture tubes are now available for avionics use.

The same Sony picture tubes that many believe to produce the clearest, brightest, sharpest color television pictures available today.

The same patented one-gun Trinitron tubes that can be found in almost every television station in America.

If you're in the process of designing avionics systems, the uses of Sony Trinitron tubes should be obvious.



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Everyone knows, for example, that color radar is only as accurate as the color. What better tube to use than Sony? (Leading manufacturers already use Trinitron tubes in their color radar systems.)

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Sony Trinitron color tubes can be incorporated into the next generation of avionics and air-route traffic-control systems to display en-route NAVAID information, aircraft position, approach plate data, and flight routings. And because their quality is so abundantly evident (all you have to do is look), they'll make any color display system easier to sell.

As you'd expect, Sony tubes meet very high standards for durability and shock absorption.

USED IN ONBOARD NAVAID SYSTEMS, A SONY TRINITRON TUBE CAN MAKE EVEN THE MOST COMPLICATED APPROACH PATTERNS EASIER TO USE.

More importantly, they meet the standards of Sony. A company whose reputation for quality control is second to none.

For more information about the avionics applications of Sony Trinitron tubes, write on your company letterhead to Michael Schulhof, President, Sony Industries, 9 West 57th Street, New York, N.Y. 10019.

Better still, go to any store that sells television sets and witness the superiority of Sony Trinitron tubes for yourself.

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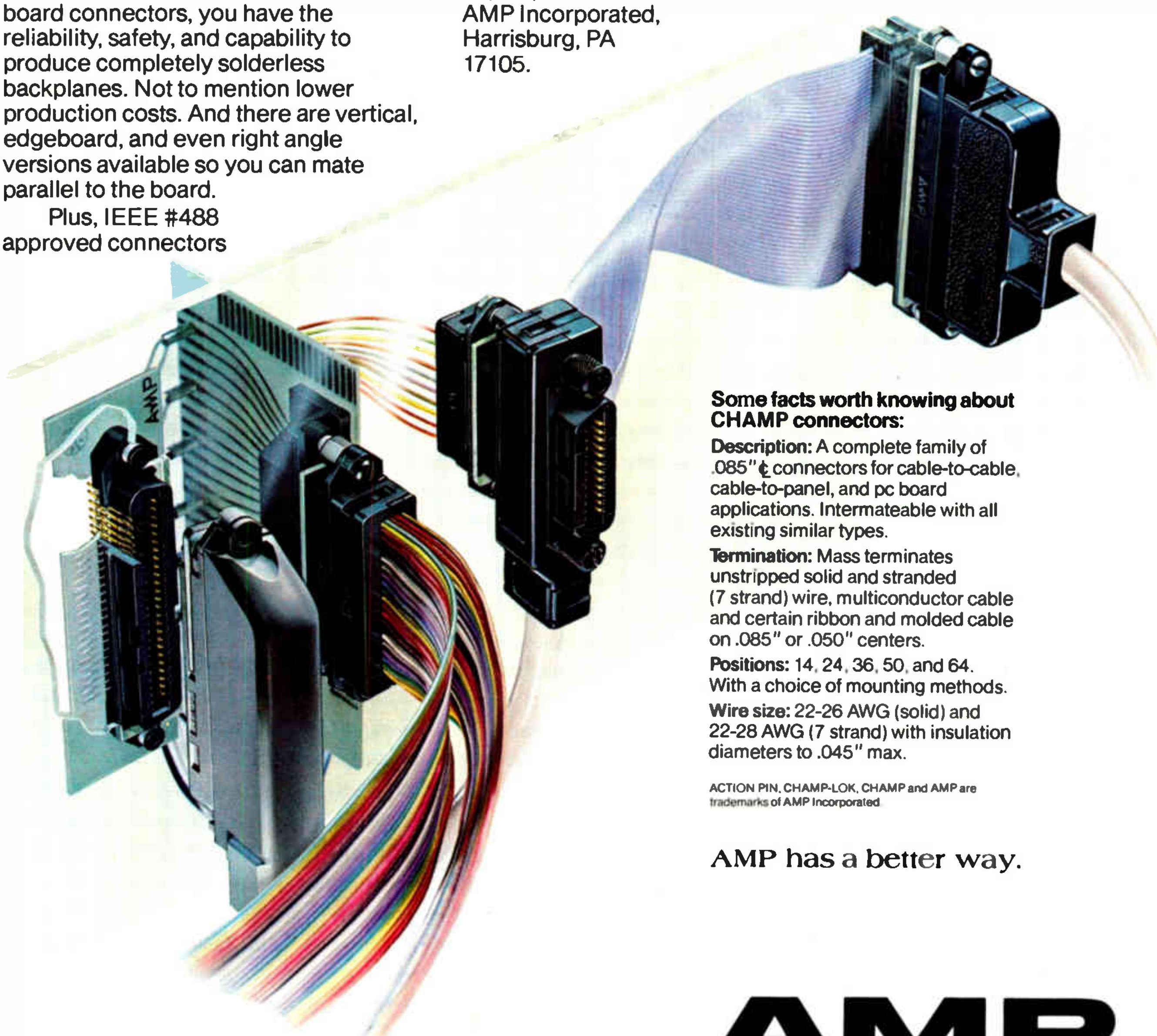

Some facts worth knowing about CHAMP connectors:

Description: A complete family of .085" ℄ connectors for cable-to-cable, cable-to-panel, and pc board applications. Intermateable with all existing similar types.

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A signal from the Government

President Carter and his multitude of challengers are not falling all over themselves to explain to their fellow Americans why silicon may have as important a role in the economy as grain sales to the Soviet.

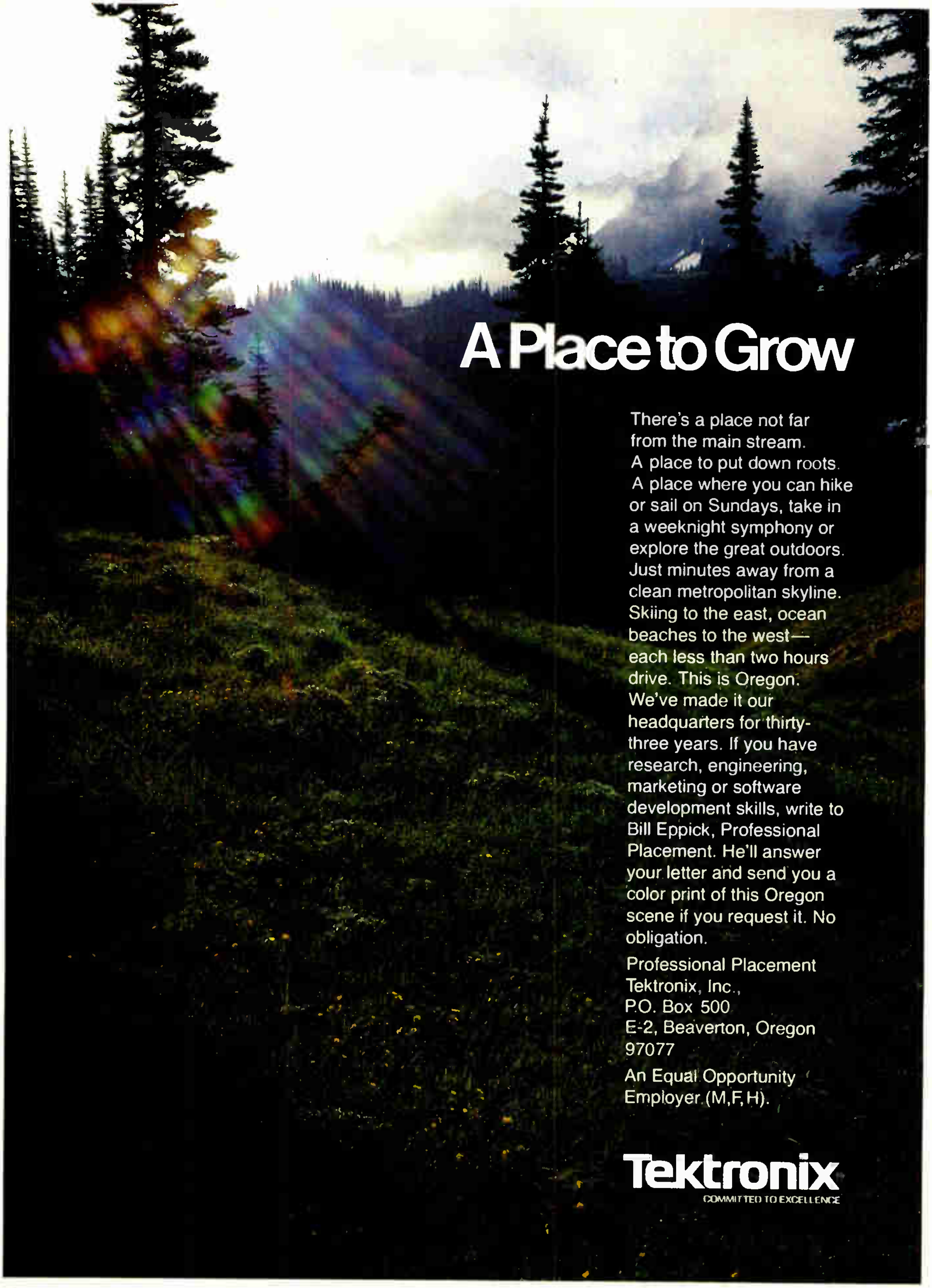
Sen. Adlai E. Stevenson III, for one, is known to lament that reality, and so does the staff of the Illinois Democrat's subcommittee on international finance. But that does not alter the fact that Stevenson was the only legislator to turn out for mid-January hearings that seek to shape a national policy on trade in electronics and other high technologies. "Issues like these unfortunately lack the sex appeal of an embargo on grain sales to Russia," admits one Stevenson staffer, "and never get broad media coverage." The trade press reports them, of course, but readers of these reports are aware of these issues already. For the public in general, however, such issues as trade in integrated circuits are too ambiguous, mysterious, and plagued by statistics to warrant attention.

That attitude compounds the problems of a vigorous and growing IC industry unwilling to stand by while what it sees as unfair foreign competition undermines its leadership position in its own domestic markets. It was a point made clear to a sympathetic Stevenson by such industry leaders as Intel Corp.'s Robert N. Noyce, testifying on behalf of the Semiconductor Industry Association, and Motorola Inc.'s John Welty, who spoke for the International Business Council of the Electronic Industries Association.

The fact that their concerns were supported by the White House Trade Representative's office was probably the most encouraging sign of the session. "In trade policy development, we must not, and will not, overlook the legitimate trade problems of an expanding successful industry simply because it has unorthodoxly [*sic*] approached the Government in health, rather than in serious injury," declared Robert Hormats, who carries the rank of ambassador and functions as deputy to U. S. trade representative Reubin Askew.

This signal by the Government that it is now ready to support one of its leading industries in gaining access to European and Japanese markets equal to others' access to U. S. markets is indeed encouraging. But it is certainly not enough.

What U. S. manufacturers of ICs and other high-technology products must do is take their case to a broader segment of the U. S. public than they are now reaching. Beyond Adlai Stevenson are 99 other members of the Senate and 435 members of the House. Beyond them are the voters who must be awakened to the fact that products made from silicon will be just as critical as products made from corn and wheat to the long-term economic future of the nation.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Meetings

The Automated Office, American Institute of Industrial Engineers, (P. O. Box 3727, Santa Monica, Calif. 90403), Twin Bridges Marriott Hotel, Washington, D. C., Feb. 11–13.

Third International Business Computing, Word Processing and Information Management Exhibition and Conference (Info '80), BED Exhibitors Ltd. (Bridge House, Restmor Way, Wallington, Surrey SM6 7BZ, England), Cunard International Hotel, London, Feb. 12–15.

The IBM Evolving Network Strategy, The Yankee Group (Box 43, Cambridge, Mass. 02138), Hyatt Rickey, Palo Alto, Calif., Feb. 13–14, and the Harvard Club, New York, March 25–26.

ISSCC '80, International Solid State Circuits Conference, IEEE and the University of Pennsylvania, San Francisco Hilton Hotel, San Francisco, Feb. 13–15.

Southwestern Tool and Manufacturing Engineering Conference and Exposition, Society of Manufacturing Engineers (P. O. Box 930, Dearborn, Mich. 48128) and National Tool, Die and Precision Machining Association, Albert Thomas Convention Center, Houston, Texas, Feb. 19–21.

Alternate Energy Sources of the 1980s Conference, IEEE, Town and Country Hotel, San Diego, Calif., Feb. 20–22. (For information, write to George Seebeck, San Diego Gas & Electric Co., San Diego, Calif. 92101.)

First International Conference on Bubble Memory Materials and Process Technology, American Vacuum Society (2030 Alameda Padre Serra, Santa Barbara, Calif. 93103), Santa Barbara Riviera campus, Feb. 20–22.

Word/Text Processing, American Institute of Industrial Engineers, (P. O. Box 3727, Santa Monica, Calif. 90403), Ambassador West Hotel, Chicago, Feb. 20–22.

Software Quality Assurance and Configuration Management Seminar, American Institute of Aeronautics and Astronautics (P. O. Box 91295, Los Angeles, Calif. 90009) *et al.*, International Inn, Washington, D. C., Feb. 21–22.

Computers in Manufacturing Conference, American Institute of Industrial Engineers (P. O. Box 3727, Santa Monica, Calif. 90403), Airport Park Hotel, Inglewood, Calif., Feb. 25–27, Ambassador West Hotel, Chicago, March 19–21, and New York Statler, New York, April 30–May 1.

Compcon80, IEEE Computer Society (999 N. Sepulveda Blvd., Suite 410, El Segundo, Calif. 90245), Jack Tar Hotel, San Francisco, Feb. 25–28.

Diamond Jubilee Exhibition, Society of Automotive Engineers (400 Commonwealth Dr., Warrendale, Pa. 15096), Cobo Hall, Detroit, Feb. 25–28.

Conference on Industrial Investment Opportunities in Morocco, Moroccan Industrial Development Office (821 U. N. Plaza, Suite TM-606, New York, N. Y. 10017), Rabat, Morocco, Feb. 25–29.

13th International Instruments, Electronics and Automation Exhibition, Industrial and Trade Fairs Ltd. (Radcliffe House, Blenheim Court, Solihull, West Midlands B91 2BG, England), National Exhibition Centre, Birmingham, Feb. 25–29.

Conference on Laser and Electro-Optical Systems/Inertial Confinement Fusion, IEEE, Optical Society of America (200 L St. N. W., Washington, D. C. 20036) *et al.*, Town and Country Hotel, San Diego, Calif., Feb. 26–28.

Short courses

Printed-Circuit Boards Update, Holiday Inn Center Park, San Jose, Calif., Feb. 19–21. Write to Society of Manufacturing Engineers, P. O. Box 930, Dearborn, Mich. 48128.

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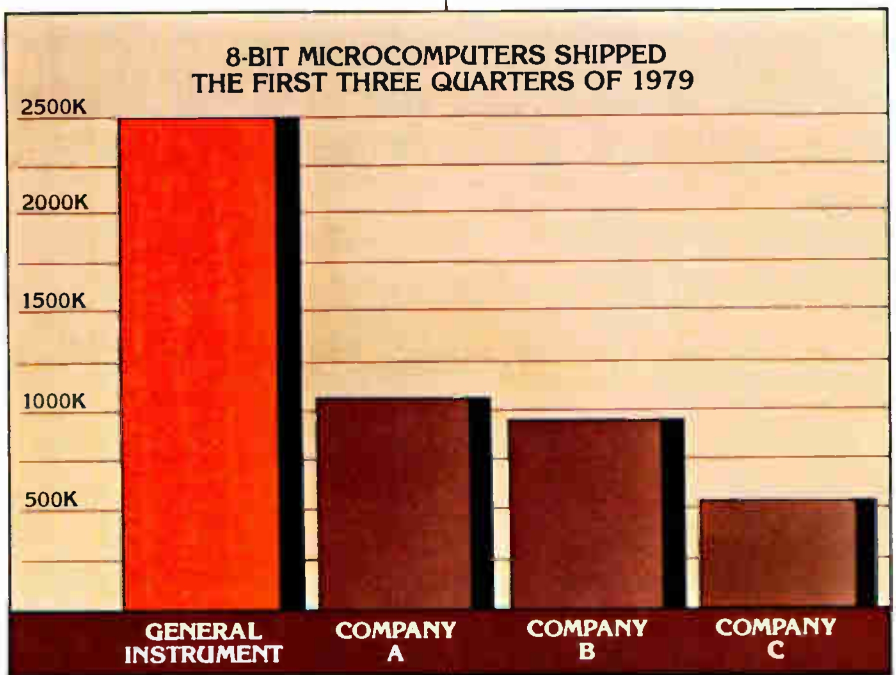
The record speaks for itself. An independent survey revealed that during the first 9 months of 1979 General Instrument had topped all rivals by delivering over two and one-half million 8-bit microcomputers. That's more than twice as much as our nearest competitor.

While it is a most impressive record, to be sure, it's a direct reflection of the success and acceptance of General Instrument's philosophy: To provide products of consistent high quality, backed by comprehensive support and customer service, at competitive prices. Simply stated, we deliver more 8-bit microcomputers, because our microcomputers deliver more to our customers.

Specifically, our popular PIC family consists of the PIC 1650A with 512, 12-bit words of Read-Only-Memory, 32, 8-bit bytes of RAM, 32 I/O lines, real-time clock counter and two-level stack, packaged in a 40-pin DIP. The PIC 1655A is a reduced I/O version, 20 I/O lines, packaged in a space-saving 28-pin DIP. Another version, the PIC 1656, has both external and internal interrupts, three-level stack and 20 I/O lines in a 28-pin DIP. A development microcomputer, without the ROM, is also available.



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All PIC series chips feature a powerful 12-bit instruction set, instead of the usual 8-bit instruction word offered by other manufacturers, which allows applications with far less ROM.

So much for what we make. What our customers make of it is something else again. Our 8-bit microcomputers have proven them-

top by just delivering microcomputers.

selves in a wide variety of applications, including vending machines, consumer appliances such as washing machines and vacuum cleaners, electronic games, keyboards, display drives, TV/radio tuning systems, industrial timers, motor controls, security systems and automotive dashboard instrumentation. And as long a list as we may come up with, it still isn't long enough, because even as you're reading this, someone is designing a PIC into yet another challenging product application.

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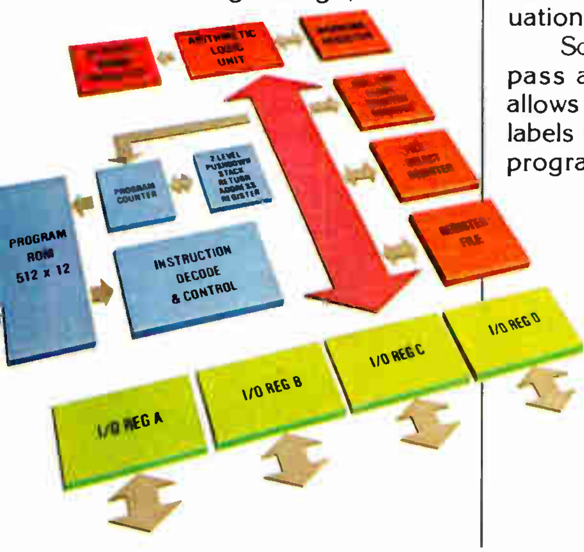

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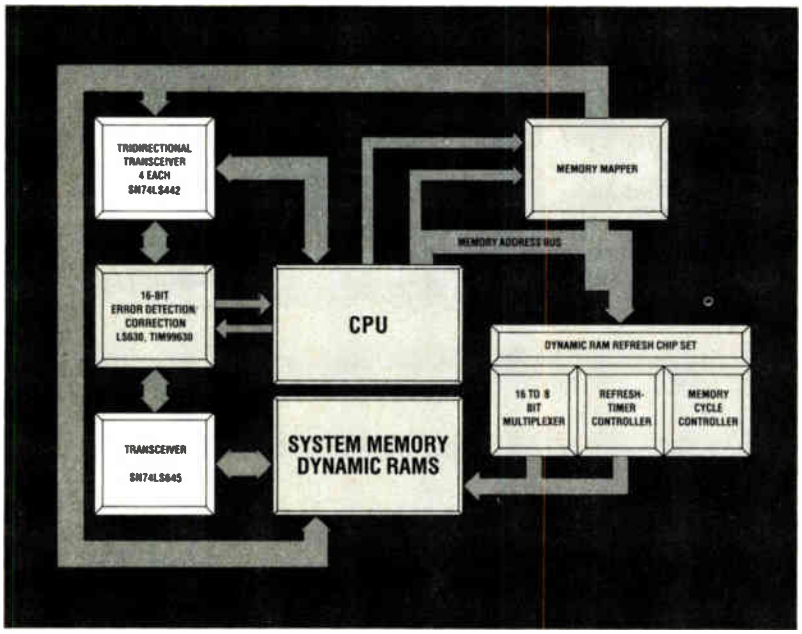
22 new bus transceivers. First quad tridirectionals ever. More octal bidirectionals too.

Low-Power Schottky innovation from Texas Instruments.

Here's a new line of bus transceivers from Texas Instruments that offers a choice of true or inverting logic in 3-state or open-collector outputs — plus, the industry's first quad tridirectional transceivers.

Among the new quad transceivers are tridirectionals (LS440 through LS444, LS448) and bidirectionals with individual direction controls (LS446, LS449). The new octal transceivers, all bidirectional, include some with local bus-latch capability (LS620 through LS623), expanded versions of the popular LS245 (LS640 through LS645) and some with input D registers (LS646 through LS649).



This is the second in a series of innovative Low-Power Schottky devices TI is introducing over the next few months. Watch for the new Memory Mapper announcement and find out how you can replace 26 components with one 40-pin package.

Features common to all device types include: asynchronous communication between data buses; on-chip bus selection decoding; input hysteresis for improved noise margins; control function implementation for maximum timing flexibility; operation over full commercial and military temperature ranges.

For the first time the designer has a choice of selecting inverting, non-inverting, or a combination of inverting and non-inverting data paths with either 3-state or open-collector outputs.

The direction of data transmission for all devices is controlled by the logic level at the direction control input. The enable input may be used to disable the devices so that the buses are effectively isolated.

Just examine the options and you'll see how flexible the new line of transceivers from Texas Instruments can make your next design job.

An additional option on the LS640 through LS645 devices is the ability to sink 48 mA instead of the conventional 24 mA. Parts with this capability are designated with a "-1" following the standard part number.

Like all TI Low-Power Schottky circuits, these new devices are low-cost and feature less heat generation, increased densities and improved system performance.

TI's continuing commitment to innovative Low-Power Schottky technology means that you can continue to design with confidence — tapping the industry's broadest product line.

For every low-power, high performance application — whether it's military systems, data processing, telecommunications, process control — and much more.

And there's much more on the way from TI. In addition to those devices already introduced, over the next few months we'll be introducing more new devices in the Low-Power Schottky Family.

You'll want to watch for them. Because, like the new bus transceivers, and the proven performance of TI's existing Low-Power Schottky line, they'll go a long way toward making your design job easier.

For the widest range of effective bipolar state-of-the-art solutions, turn to the leader. Turn to Texas Instruments for more Low-Power Schottky innovation.

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Electronics newsletter

Fiber optics shows mettle in watery application for Navy

Fiber optics continues to be the transmission line of choice for harsh environments. The latest example: ITT's Electro-Optical Products division in Roanoke, Va., has installed a six-channel 4-km cable underground in what it refers to as a "generally water-filled duct." **Though such immersion might be sudden death for a conventional electrical cable,** the fiber, made of dielectric material, is not bothered. More than 10 Mb/s can be handled by the installation at the Navy air station in Norfolk, Va.

Electrophoretic display occupies new Exxon venture

According to Webster's, "electrophoresis" is the movement of suspended particles through a fluid by an electromotive force. But it also describes a technology around which Exxon Enterprises Inc. has formed a new electronics venture that is expected to yield its first fruits for only year or more from now. Called Electrophoretic Information Displays, or EPID, the new division is understood to be engaged in the **research and development of a new display product, possibly flat-screen.**

Analog Devices joins ATE race with benchtop unit

The potentially rich automated test equipment market these days has tempted a New England company to broaden its diet. Hybrid component maker Analog Devices Inc. of Norwood, Mass., is going after **its first slice of the ATE pie with a benchtop linear IC tester slated for delivery at the beginning of May.** The tester will be built around a 16-bit TMS 990/100M microcomputer from Texas Instruments Inc. and offer IEEE-488 bus control, two RS-232-C interfaces, and disk program store.

Mostek to unveil its versions of 8086 and controller

Initial samples are expected around midyear of Mostek versions of the 16-bit 8086 microprocessor and associated 8259A interrupt controller. The two devices, which the Carrollton, Texas, subsidiary of United Technologies Corp. will build as a licensed second source to Intel Corp. [*Electronics*, Nov. 23, 1978, p. 46], will be available concurrently late in the second quarter or early in the third quarter, Mostek officials say. Also definite now are **Mostek plans to produce a second-source version of the 8088,** an 8-bit implementation of the 8086, about six months later.

New firm lists Pascal compilers for Intel devices

Language Resources Inc., the Sunnyvale, Calif., software company founded by former Intel Corp. employees, will make available native code Pascal compilers for Intel's 8080 8-bit and 8086 16-bit microprocessors during the second quarter. **The first compiler will execute on Intel development systems, and later versions will execute as cross compilers on large machines.** These products will include a compiler for standard Pascal, a macro-assembler, binding software, and library support.

Word processor based on disk to enter market

Exidy Data Systems Inc. of Sunnyvale, Calif., will introduce a disk-based word-processing system this April. The system will use full-sized disks and will accept both single- and quad-density floppy disks. It is an expansion of the firm's existing Sorcerer system. Exidy will enter the already crowded field with what are expected to be two advantages: **a keyboard that provides for single-stroke commands; and a price that is aimed at the lower end of the market,** less than $4,000 for the basic computer system, word-processing package, disk drive, and printer.

Electronics newsletter

V-MOS FETs take price down to bipolar level

Siliconix Inc. of Santa Clara, Calif., is about to take the wraps off two new high-voltage (400-V breakdown) V-MOS power field-effect transistors that are expected to herald the arrival of such devices at bipolar prices. What's more, the devices will be the first at Siliconix to use **a new high-density process that enables the firm to price them about an order of magnitude less** than comparable currently available V-MOS parts.

Engineers in the '80s: the ultimate scarce resource?

According to figures projected for employment needs and engineering graduations, New England, and perhaps the entire country, may be **as much as 50% short of engineers and computer professionals by 1982–83.** The data, just released by the Massachusetts High-Technology Council, appears to indicate that "there is **just no way we can get enough engineers into the educational pipeline fast enough** to offset this shortfall."

Low-cost gyros to improve breed, broaden markets

Responding to increasing demand for medium-performance inertial guidance and control systems, the C. Stark Draper Laboratory Inc. has established a new operation to develop and produce miniature gyros and accelerometers with high parts commonality and innovative materials and production techniques. The Cambridge, Mass., lab already has built a pilot run of molded plastic gyro systems with high price-performance ratio and is **experimenting with automated and robotic assembly techniques.** The effort, partly sponsored by the Air Force, would first be applied to tactical weapons systems. However, the low-cost inertial sensors might be inexpensive enough for private aircraft and vessels and remotely piloted vehicles.

Motorola joins list of makers of 5-V 16-K RAMs

Samples are scheduled to be available later this quarter of the MCM4516, a 16-K dynamic random-access memory from Motorola that requires only a single 5-V power supply. The device, organized as 16-K by 1 (bit), is built with the same HMOS process as that employed in Motorola's 64-K RAM, the MCM6664. Single-supply 16-K RAM devices—which offer improvements over traditional three-supply 4116-type devices—are also **planned or announced by several other U. S. manufacturers, including Intel, Mostek, National Semiconductor, and Advanced Micro Devices.** In Japan, Hitachi is also believed to be planning one.

Addenda

Look for the Motorola Semiconductor Products Group to introduce a data-encryption chip at the end of March. The single-chip device—dubbed the MC6856—will handle 400,000 b/s in a 24-pin package that **is compatible with either the 6800 or 8080 microprocessors.** It is based on the one available in Motorola encryption systems that have previously been available [*Electronics*, June 21, 1979, p. 107] and will have secondary key capability. . . . The on-again, off-again **merger of Sanders Associates Inc. of Nashua, N. H., and California Computer Products Inc. of Anaheim, Calif., is on again,** and this time it looks as if it will stick. Proxy materials have been sent to stockholders and they will vote on the merger at meetings Feb. 15 and 16. . . . Nippon Electric Co. has developed a 1-K random-access MOS memory **with 8-ns access time.** . . . **Clarence W. Spangle will become president and chief executive officer of Memorex Corp., Santa Clara, Calif., in March.** He now heads Honeywell Inc.'s information systems operation in Minneapolis.

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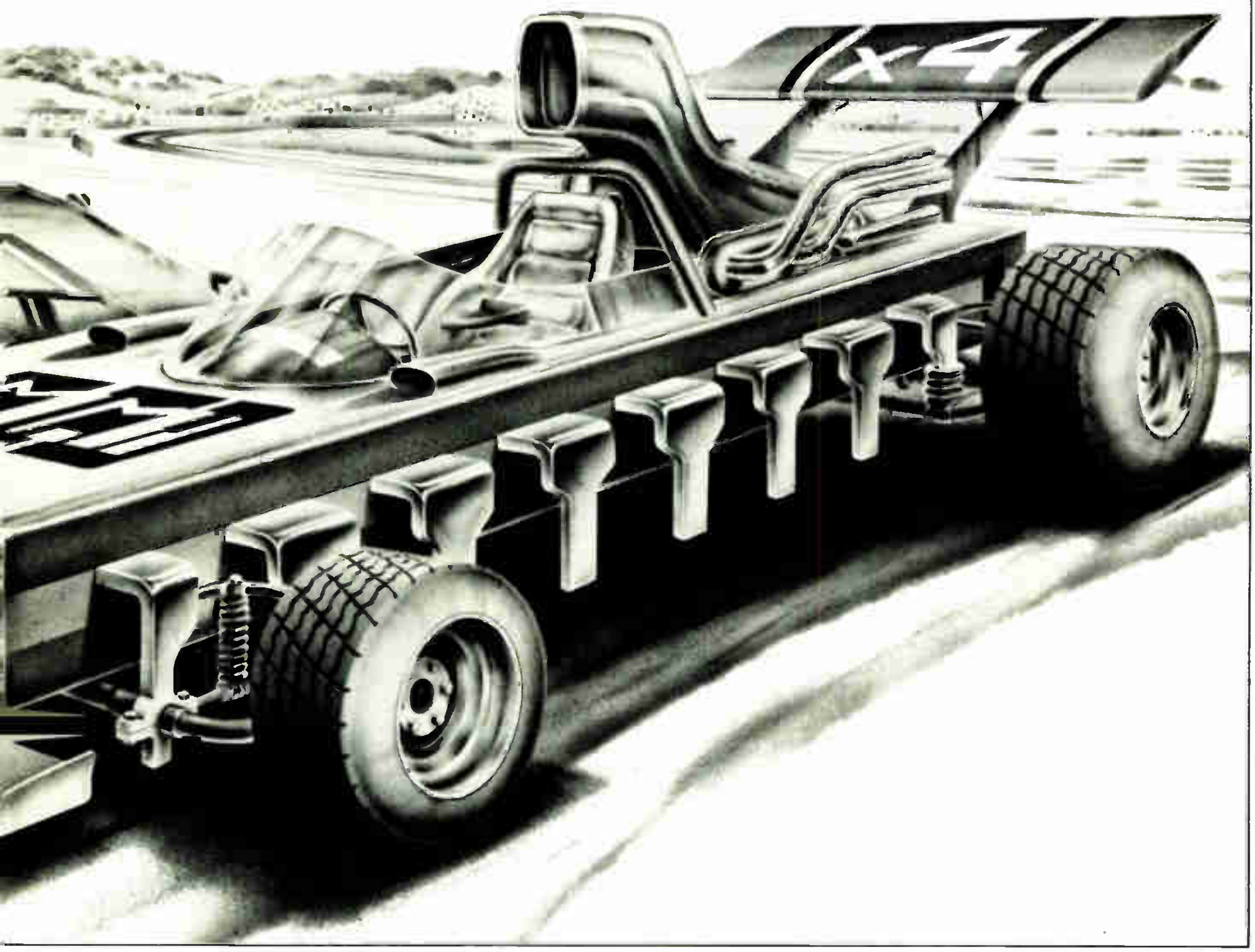


Instrument makers score unannounced bugs in GPIB chips

by Martin Marshall, West Coast Computers & Instruments Editor

Complaints cover design idiosyncracies in instrument-bus ICs known to their makers

Semiconductor makers have a good thing going in their general-purpose instrument-bus chips because the GPIB integrated circuits simplify the interconnection of instruments with the IEEE-488 bus standard. However, users report that virtually every one of these ICs comes complete with bugs—design idiosyncracies that require care during system design so that the chips will implement the bus interface correctly.

Designing around these bugs is not made easy for small instrument manufacturers by secrecy at the IC houses. "Designers from small instrument makers find themselves in the position of rediscovering some of the bugs when prior knowledge could save a lot of effort," notes Bert Forbes, president of Zia Tech Corp., San Luis Obispo, Calif. "When they call up a manufacturer, he will acknowledge the bug that the designers found, but then he won't tell them about the other bugs."

More complaints. Forbes is not alone. The bugs and the secrecy of the bug lists were a hot topic among designers at the Automatic Test Equipment Seminar and Test Instruments Conference held earlier this month in Pasadena, Calif.

What kinds of problems crop up with the GPIB chips? A sampling includes:

- The interpretation of the end-of-interval signal on Intel Corp.'s 8291 talker/listener and 8292 controller. They can act on the EOI message asynchronously, which can lead to a false data-valid message unless the designer is very careful in timing the sending of the data.
- The TMS 9914 will let information flow into an instrument faster than the buffer of the latter's central processing unit can handle it. Thus other means have to be used to control the not-ready-for-data line.
- A more recent entry, the Signetics HEF4738 bus interface, may have a problem with the unlisten message in at least one application. Valhalla Scientific Inc. of San Diego reports UNL is not telling an instrument to go into standby. Thus it stays on the bus and responds to commands intended for other instruments; although Valhalla does say the problem may be in its system.
- With the Motorola 6848 GPIB chip, an EOI signal leaves an end message in the buffer, which then goes out in the first byte of a new message. Also, there are ghost interrupts produced by the byte-out command followed by an attention message or by an interrupt of a serial poll.

Lists exist. Generally, such idiosyncracies are well known to the chip makers. In fact, designers at the Pasadena meeting complained that the makers will provide lists of GPIB bugs to large users, such as Hewlett-Packard Co., Tektronix Inc., and John Fluke Manufacturing Co., but not to low-volume users.

Intel says it has indeed given bug

Conferees look at logic analysis techniques

Signature analysis looks to be the digital service technique of the 1980s, according to a panel at the Automatic Test Equipment Seminar and Test Instruments Conference. Ease of use in the field by unskilled technicians is the primary reason, they say.

The panel on logic analysis techniques included representatives from Hewlett-Packard Co., which introduced the measurement technique [*Electronics*, March 4, 1977, p. 89], and from Tektronix Inc. and Millennium Systems Inc., both offering signature-analysis gear. Also present were equipment manufacturers who are implementing signature analysis.

HP is perhaps the leader in implementing of signature analysis in their wide range of products, but other manufacturers are reported to be using the technique. Among them are Leeds & Northrup Co., Lanier Business Systems Inc., Eastman-Kodak Co., and Racal-Dana Instruments Inc.

The technique is desirable for field servicing because the field technician need only probe nodes in a circuit and check the signatures obtained with those on a schematic. However, implementing the technique does require extra design time on the part of the maker, and, of course, documentation of the proper signatures is no small task.

When it comes to design development or production-line testing, logic analysis and in-circuit emulation come into play, the panel agreed. Signature analysis is almost entirely excluded from the design area because it does not disclose the qualitative program-oriented information designers need. **-M. M.**

lists to at least two major GPIB chip users. "Yes, we have given bug lists to HP and Tektronix, but that was because they helped us develop the chips," reports William R. Schillhammer, product marketing manager of data-communications peripherals in Santa Clara, Calif.

Marketing glitch. A spokesman at another semiconductor company, who asked for anonymity, says "We don't like to publish errata sheets because we feel it would give our competitors an unfair marketing advantage. They could run ads citing the problems with our devices without mentioning the bugs involved in their chips."

The chip makers also say that the information on the bug list is available—to the right people. "Designers should be able to get that information from our field applications engineers," asserts Don Phillips, peripheral products marketing manager at Intel. "The people we won't give that information to are those who have no commitment to the chips but are just shopping around."

On the other hand, "the month delay in updating field applications engineers can turn into a 2½ month delay if the timing of the bug discovery is wrong and if it takes a while for the engineer to read the update," notes Gerald K. Mercola, president of ICS Electronics Corp., San Jose, Calif. -Martin Marshall

Photovoltaics

Arco pact gives Ovshinsky up to $25 million for development of his amorphous cells

The oil industry's high-roller mentality may be starting to shake the photovoltaic cell business, in which so many of its companies have invested. In mid-January, Atlantic Richfield Co. granted a $25 million contract to Energy Conversion Devices, Troy, Mich., to develop amorphous silicon solar cells.

Besides the amount, which intrigued industry sources say is the largest nongovernmental one of its kind yet, the contract raises some questions. "Presumably, for $25 million there's some solid technology behind it," says a photovoltaic veteran, "So what do they know that we don't?"

Little to say. But answers are hard to come by at Los Angeles–based Arco, partly because of recent changes in the management of Arco Solar Inc., its Chatsworth, Calif., solar panel firm. A corporate spokesman says Robert R. Chambers, who ran Arco Ventures Co.—a subsidiary that acquired and kept track of Arco Solar—no longer heads it. But he is mainly responsible for the $25 million award, of which Energy Conversion Devices received $8 million at the contract signing.

Chambers will not discuss the details that led to the award except to say "it's entirely for research and development" and to call its head, Stanford R. Ovshinsky, "a good research man." A source familiar with the award, however, cautions, "Don't assume it's all for solar cells or that a lot of progress was made to justify it." Arco will not get actual devices from the Michigan firm.

Skepticism. Indeed, Department of Energy and industry officials remain skeptical about any technology advances in amorphous cells by Energy Conversion Devices. "It's an exciting area, and there's nothing wrong with it, but they have a long way to go," says one.

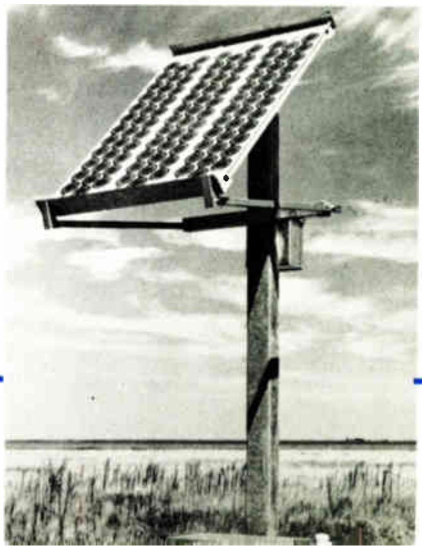
Amorphous silicon's random molecular structure, which can be built up in thin film, should be cheaper than crystalline silicon. However, the conversion efficiency of sunlight to electricity has been below 6%, perhaps as low as 4.5%—and the break-even point is 8%.

Ovshinsky says his amorphous cells have a conversion efficiency of about 10%, compared with the 10% to 14% of crystalline silicon cells. He also claims that the cost of electricity from production volumes of his cells will be about 5¢ per kilowatt-hour—residential electricity now costs about a penny less, and present photovoltaic energy costs are about 14¢/kW-h.

However, technical details on Ovshinsky's work are scanty. Also, his

Arco promotes crystalline cells, too

Whatever happens with amorphous cells, Arco Solar is aggressively pushing its panels using conventional crystalline cells, such as this 7-kilowatt array. Located in the Four Corners region where New Mexico, Arizona, Utah, and Colorado meet, it has a row of 10 of Arco Solar's new 33-watt panels, four of them wired in series to produce 48 volts dc and the rest in parallel. It is used for cathodic protection by a pipeline company, a technique that keeps pipes from rusting and deteriorating in the ground. Other applications include powering a 300-kilometer communications link (a secure phone line from Jedda, Saudi Arabia, to the Sudan) and providing power to part of the Winter Olympics communications system at Lake Placid, N. Y. Prices of Arco Solar panels run about $7 a watt. Some competitors see that tab as deliberate underpricing to grab a market share: the industry price structure at the moment is around $10/W. -L. W.



company is target of a suit by United Nuclear Corp., which had invested $500,000 in the amorphous work in a 1976 agreement. The long-term commitments in the accompanying contract are in dispute.

In 1978, Ovshinsky announced the development of photovoltaic cells from amorphous materials. But DOE officials and other sources say RCA Corp.'s Semiconductor division gets the credit. RCA reported its work in 1976 and remains "first and best," says a competitor.

The problem is pushing conversion efficiency high enough to make amorphous cells feasible, compared with more costly crystalline structures. Amorphous devices can drive low-level calculators and watches and can convert fluorescent light. But, say solar cell experts, they are not good enough yet for significant power applications. **Larry Waller**

Telecommunications

Polysilicon gives high-temperature chips; crosspoint arrays may cut need for codecs

Coming from Bell Laboratories is an integrated-circuit polysilicon technology that produces ICs capable of withstanding up to 500 volts, some 10 times higher than the typical chip. Moreover, the lab's high voltage IC design group has used it to develop a monolithic crosspoint array that could significantly cut the anticipated need for coder-decoder chips.

The new circuit could be used to reduce the high cost of providing battery feed, ringing, codec, and other interface functions for each phone line. It can do this because an array of them can function in a digital central-office switching system as a space-division concentrator or as a multiplexer of, say, 80 subscriber lines to 10 interface circuits.

Fewer codecs. Thus 10 sets composed of codec, filter, and associated circuitry could do the work of 80 sets, and the potential market for these components may be reduced by a factor of 10. Such a reduction is over and above the sharply lower codec market estimates coming from International Telephone and Telegraph Corp. [*Electronics*, Jan. 3, p. 90, and this issue, p. 76].

The crosspoint array is a replacement for the electromechanical switches that classically have been used as line concentrators. These switches have been the only way to withstand the ±500 V that a telephone loop switch must block—to say nothing of handling surge currents on the order of an ampere and the interruption of the direct current generated by the 48 V that powers the telephone loops.

Theoretically, the electromechanical crosspoint arrays could serve as the multiplexers for the codecs. But they would not be a cost-effective solution in the coming all-digital phone network.

No details. Bell Labs is keeping close wraps on its technology because it is the subject of a paper at next month's International Solid State Circuits Conference in San Francisco. However, the key to the circuit is what is known as a gated diode switch. Two of them are connected back to back with a common gate to produce bidirectional blocking and conduction in the concentrator circuit.

The new high-voltage polysilicon technology makes it possible for these switches to withstand up to 500 V. It is important to note that the technology can be the basis for IC use in applications outside telecommunications—switching, for example. **-Harvey J. Hindin**

Bell plans 611-mile optic link

Charging for the lead in the worldwide race to put fiber optics to real use, American Telephone and Telegraph Inc. has petitioned the Federal Communications Commission for a construction permit for a 611-mile system. To link Boston, New York, Philadelphia, and Washington, the laser-powered lightwave system will be wholly digital and will ultimately hook up 19 of Bell's ESS-4 electronic digital switches.

The all-digital system will enable Bell to carry voice, video, and data while taking full advantage of new large-scale integrated telecommunications circuitry. Also the plan must be viewed as the strongest evidence yet of Bell's commitment to a future all-digital network.

The first link will use the standard FT-3 44.7-megabit-per-second design. Ultimately, it will be able to handle 80,000 calls per second on its ½-inch cable, which for most of the 611 miles will be put in existing ducts. Because of the distance, the cable will have light amplifiers placed at intervals along it. But there will be far fewer amplifiers than in a conventional electrical system.

According to Robert W. Kleinert, president of AT&T's Long Lines Department, studies are already under way to extend the system to Chicago, Atlanta, and Miami later in the decade. The Boston-to-Washington system will be constructed in segments, with New York connected to the capital by 1983, assuming all regulatory barriers are overcome expeditiously. Installed cost for the segment is estimated to be $79 million. **-H. J. H.**

Government

Budget may flood defense contractors

Where will the engineers come from? Aerospace and electronics industries are all asking that question as the implications sink in of President Carter's record high budget proposal for the fiscal 1981 year beginning Oct. 1. Economists examining the spending proposals of close to $620 billion overall want to know how the plan can be implemented without giving the nation's chronic

Plain-paper copier does halftones

A fiber-optic lens array plus an innovative image-development system gives Canon USA a desktop copier that can use plain paper. The 134-pound, 10½-by-20¼-by-21¼-inch NP-200 uses a microprocessor and infrared sensors to control the copying process, says the Lake Success, N. Y., affiliate of Japan's Canon Inc.

A fiber-optic array obviates the need for a bulky lens and mirror combination and is increasingly evident in new copiers. Though plain-paper units have till now required a wet carrier for the toner, which adds components, the NP-200 uses an insulated dry toner that needs no carrier to convey it to the photosensitive drum on which images are formed. The negatively charged toner particles are picked up by an ac-biased magnetic roller, for transfer in well-proportioned amounts to the positively charged image-forming areas of the cadmium sulfide imaging drum and thence to the paper.

The result, says Canon, is perfectly formed images, even of halftones, on any type of paper. Though other dry-toner copiers can reproduce a halftone on special paper, the quality is low.

The $3,995 copier will automatically adjust to paper up to 11 by 17 in. in size. A light-emitting diode and phototransistor monitor the length of the incoming original and transfer the information to a 16-bit microprocessor, which adjusts copy length. The microprocessor also monitors and controls the entire copying process. **-Pamela Hamilton**

inflation spiral another spur.

The proposed fiscal 1981 Defense Department expenditures are $142 billion, 3% more (corrected for inflation) than the fiscal 1980 defense budget. Some 30% will go for weapons production and their research and development. That comes as no surprise in light of the USSR's military moves in the Middle East, but the size of increases in domestic social programs caught much of Congress off guard despite their election-year predictability.

"The programs themselves don't surprise me; their number and dollar values do," explains one House Appropriations Committee source. "I thought the country was supposed to be preparing itself for a little economic austerity."

No recruiting relief. A rising demand for engineers and technicians as several new weapons move into production is one that troubles corporate electronics leaders who have been recruiting in an already tight market. They see no relief in sight in view of Carter's five-year defense plan to provide real funding increases that average more than 4½% a year after inflation, confirming an earlier report [*Electronics*, Nov. 8, p. 57].

Proposed electronic upgrading of existing tactical weapons, notably Air Force and Navy attack aircraft, missiles, and army helicopters, will push electronic systems funds higher than in most other industries, officials say. They cite goals to develop a "quick reaction" strike force as speedily as possible.

One such upgrading is the Air Force's decision to equip its General Dynamics F-16 multimission fighter with the Navy-developed airborne self-protection jammer. Fitting the F-16 with the ASPJ being competitively developed by teams from Northrop Corp. and Sanders Associates and from ITT and Westinghouse "will mean a multi-year buy of more than 800 more units and should guarantee its adoption by the North Atlantic Treaty Organization," says one program leader.

Another major Air Force spending proposal is in new air-to-air and air-to-ground missiles for tactical strikes that will boost demand for radar-homing, infrared, and laser guidance packages. They will also accelerate the transition from development to production of such programs as the advanced medium-range air-to-air missile known as Amraam, follow-on to the Sparrow.

The Carter budget proposal also calls for accelerating the production start this year of the USAF air- and ground-launched cruise missiles, as well as the Navy's Tomahawk version. All three, operating with either nuclear or conventional warheads, can be employed with strategic or tactical forces. Cruise missile countermeasures and its navigation and guidance package using terrain correlation matching [*Electronics*, July 21, 1977, p. 69] have pushed unit production costs well beyond the $1 million target price, accounting for about 40% of the system.

Air and ship transports for quick-reaction forces will boost funding for a new USAF transport known only as C-X (until it gets a numerical designation) and ships like those of the Litton-built LHA class used in amphibious and helicopter assaults. These, plus funds for another new carrier, will eat up much of the Navy increases in equipment funds in fiscal 1981, if Congress adopts the Carter Administration proposal.

Electioneering? Capping the military electronics boosts, says one White House advisor, are proposals for "huge increases" for purchases of computers for educational institutions, plus significant gains for the upgrading of civilian air traffic control by the Federal Aviation Administration. "These will be criticized as election-year political buys, I know, but they are not," he contends. "They are part of needed programs to support university R&D and the President's recognition that the nation's air traffic control and landing systems require a lot of work to improve safety levels."

Beyond the problems of technical staffing, industry representatives in Washington are concerned with funding the capital requirements of additional plant space and production equipment that the accelerated spending program will need. As one military electronics executive says of the Carter program, "there is so much new money in here, it is very appealing, but I am not sure that Congress will provide all of it. Nor am I sure that industry can handle it given the present [inflationary] economy and money supply," he adds skeptically. **-Ray Connolly**

Solid state

EE-PROM merges write and erase devices, shrinks cell size eightfold

By shrinking the cell in its electrically erasable programmable read-only memories to an eighth of their original size, Texas Instruments Inc.'s French design center can now make large-capacity EE-PROMs. To do it, TI went to n-channel technology for its dual-injection floating-gate MOS, so that Difmos cells can now use two merged devices for writing and erasing and a sharply reduced area for bootstrap capacitance.

The first products to benefit from the improved Difmos process will be 8-K EE-PROMs and TI's popular TMS 1000 4-bit microcomputer, which will be offered with on-chip nonvolatile memory later this year. The company is not renowned in the U. S. as a supplier of EE-PROMs, but in Europe it has sold tens of thousands of 1-K and smaller parts for all-electronic TV tuning.

These parts have been built with p-channel and even complementary-MOS versions of Difmos [*Electronics*, Aug. 19, 1976, p. 26]. The cells have been rather large, but as such applications ask for no more than a kilobit of storage, die size and yield have both been reasonable.

The new Difmos technique will enable TI to break away from modest-capacity memories to compete in the ultraviolet-light-erasable PROM market. Technological problems have kept EE-PROMs from competing with these E-PROMs, but besides TI, Intel and Xicor are solving the problems, and others like General Instrument Corp. will join the race.

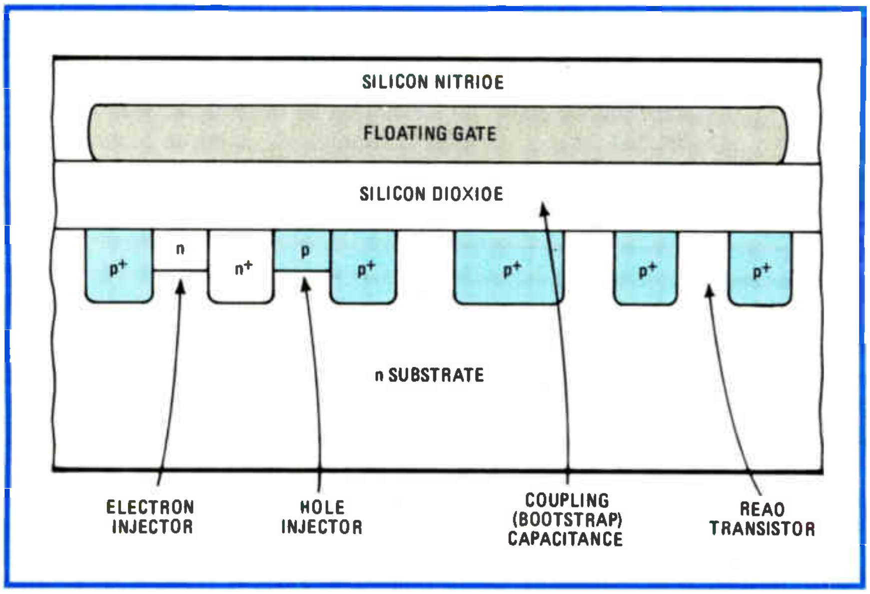
Similarities. Difmos cells are similar to floating-gate avalanche-injection MOS (Famos) cells pioneered by Intel Corp. for E-PROMs. In both structures, electrons generated in the channel of an MOS transistor muster sufficient energy to penetrate a thin gate oxide and become lodged in a floating gate. While Famos devices absorb UV radiation for erasure, a second transistor in the Difmos cells generates holes that cross the gate oxide to neutralize and erase the floating gate.

The n-channel Difmos uses a single merged injector (see diagram) to inject both electrons and holes into the floating gate, explains Jean Lesieur, manager of integrated circuits research and development for TI France in Villeneuve-Loubet.

The merged structure also allowed the TI engineers to reduce the cell's bootstrap capacitance without affecting its ability to help the holes jump the gap to the floating gate. The positive holes need to see a floating gate at a voltage of about −30 V, and the bootstrap capacitance pumps it up to that level just prior to erasure. In the old cells, this capacitance ate up a significant amount of area, about one third of the 1,000-square-micrometer total.

Gate changes. Whereas the older devices used aluminum floating gates, the new ones use a completely insulated polysilicon gate that enhances the efficiency of the bootstrap action. Moreover, some of the charge intended for the floating gate always goes into the substrate. But with the merged layout, the substrate under each cell is eight times smaller, so much less is lost.

The new memories and the TMS 1000 with nonvolatile storage may not be marketed in the U. S. The technology has been pursued by TI France, and all the resulting products have so far served European markets—about 75% of the TMS 1000 applications are in telecommunications. The word from Dallas? "No comment." **-Kenneth Dreyfack**



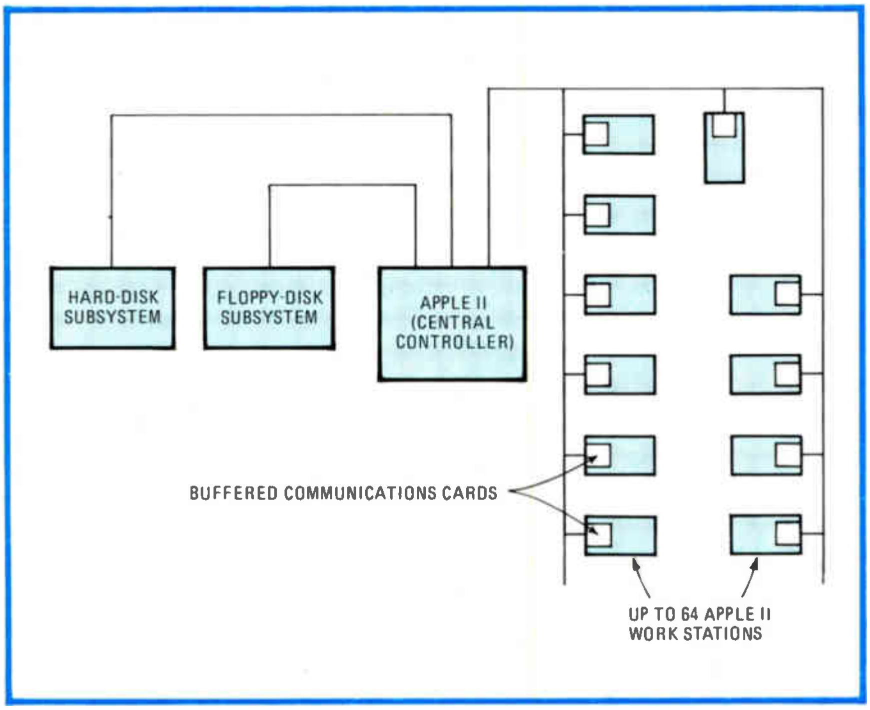
Small cells. By going to a p-type substrate, TI France can merge the two charge-carrier injectors (left) with a shared n⁺ region. The result is much smaller EE-PROM cells.

Personal computers

Network links units, includes mass store

A new world of applications is opening up for personal computers now that time-sharing and distributed-processing procedures are being added to their repertoires. Much of the groundwork for these additions is coming from a small California firm, Nestar Systems Inc.

The Palo Alto company last year developed personal computer cluster—several machines time-sharing a large program library—that is



Apple network. A hardware-software package from Nestar Systems organizes as many as 65 Apple II personal computers into a low-cost network with sophisticated communications.

finding a niche as a limited-function, local network in classrooms and laboratories. Now Nestar is following up with a network having greatly expanded storage and far more sophisticated communications.

New affiliations. Whereas the initial Cluster/One system allows as many as 30 personal computers access to a central program library, it did not provide communications between terminals or a means of maintaining an on-line data base. Now that those functions are available in the model A, personal computers can be expected to vie with small business computers in many existing office-system applications, among them word processing and electronic mail, and to make computer nets affordable for lower-level applications. In a 10-station network, the cost per work station would be less than $2,800, or about one third that of existing communicating word processors.

Intended also for the educational market, the new hardware and software link as many as 65 standard Apple personal computers—one serving as a central mass storage manager—into a high-speed computer network (see figure). The model A allows users transparent access to programs, files, and data resident in the central processor.

According to Harry Saal, president of the 1½-year-old firm, message blocks can be transmitted at 120 kilobits a second directly from work station to work station. Each station can connect to a central memory able to store up to 33 million bytes. "It allows for the ultimate combination of personal computers and central resources, because it moves applications based in an 8-inch disk into a network for multiple users to access," says Saal.

Controller. In the model A network, a standard Apple computer with 48 kilobytes of random-access memory functions as a dedicated central controller and mass-storage manager with connections to storage subsystems and other Apples that serve as user stations. All stations share access to a common read-only library of programs and data and can have their individual data bases simultaneously updated.

Basically, Nestar's model A offering consists of a 10-by-20-by-29-inch metal package with a read-only library of two double-sided 8-in. floppy disks having a formatted storage capacity of 1,260 kilobytes; the necessary electronics that plug into the central controller to provide communications and mass-storage control; the ClusterBus communications card; the communications cards required for each Apple station; and the necessary software. The communications cards for each station contain a 1-kilobyte RAM for transparent buffering and 2 kilobytes of read-only memory for network interface routines, as well as all necessary bus electronics.

The software includes protection to preserve data and prevent unauthorized access. A "lock" command permits a primary user to update a specific data base unhampered.

The model A has a gateway feature that, Saal says, allows users to interconnect two or more networks. One work station in each network has two communications cards, each linked to a different network. Users can write programs in one network requesting programs or data from another. **-Bruce LeBoss**

Trade

U. S. to press Japan on 'targeting' charges

The campaign of U. S. semiconductor manufacturers to galvanize Government action against foreign competition is beginning to bear fruit. A key U. S. trade negotiator told a mid-month Senate hearing that the Carter Administration is preparing to take a tougher line with Japan on internal policies there that affect foreign trade.

What's more, Robert Hormats, deputy U. S. trade representative, observed that the semiconductor industry is suffering from foreign competition (see p. 24). As they have in other such forums, the semiconductor houses wheeled out some big guns to testify: Robert N. Noyce, vice chairman of Intel Corp., and John Welty, general manager of Motorola Inc.'s Semiconductor

Products Group. Appearing on behalf of the Electronics Industries Association of Japan was H. William Tanaka, its counsel.

Hormats said the U. S. trade representatives engaged in continuing negotiations with their Japanese counterparts will argue that Japan is targeting specific U. S. electronics markets, such as that for 16-K random-access memories. "Targeting" is singling out export markets for specific products and then helping domestic industry compete through vast government financial resources and close relationships with private banks. The negotiators also will continue to push for an end to Japanese restrictions on foreign investment and participation in domestic trade.

Hormats stopped short of saying that restriction by foreign governments of overseas competition will be met with equivalent U. S. action. But he did say the negotiators "will actively assert our trade rights in this sector."

The occasion for the hearing before the Senate international finance subcommittee was the International Trade Commission's report on competitive factors in world trade in integrated circuits. [*Electronics*, Dec. 6, p. 41]. The ITC prepared the report for the committee.

That report has already run into flak from the Semiconductor Industry Association [*Electronics*, Dec. 20, p. 43]. Testifying for the SIA, Noyce challenged some of the report's statistical judgments and called for Government negotiations "to neutralize target industry policies."

A major SIA indictment of Japan has been on targeting. Noyce continued this attack by focusing on capital investment in the U. S., Europe, and Japan.

Tight money. He argued that U. S. companies face a "leverage gap" that could slow their relative growth and lead to loss of market share to "aggressively growing, government-subsidized foreign companies, which have assured resources of capital and thus can price their products without concern for current earnings."

To bolster his case, he presented the subcommittee chaired by Sen. Adlai E. Stevenson III (Dem., Ill.) with SIA data drawn from corporate annual reports and Moody's Investment Services. Although the 1978 profitability of U. S. producers was double or triple that of Japanese and

Space heaters look to digital control

Digital electronics control is coming to another consumer product: electric space heaters, where business is undergoing a modest boom as central heating systems get more expensive to operate. However, the space heaters tend to have a wide margin of error in maintaining a steady output of heat—and that is where solid-state electronics comes in.

At this month's Chicago housewares show, Arvin Industries Inc. unveiled a solid-state controlled space heater. Both the Columbus, Ind., company and its chief competitor say they are working on microprocessor-based programmable controls.

Arvin applied some of the solid-state knowledge it has accumulated in its private-label audio products division, says Gene Knott, engineering vice president. A custom quad comparator from Hitachi Ltd. receives signals from a thermistor, compares them with the desired temperature level, and sends instructions to triacs controlling the two heating elements and a fan. It controls the output temperature to within ±1°F, whereas electromechanical controls have a ±15°F range of error.

Both Arvin and the Edison division of McGraw-Edison Co. are working on microprocessor-controlled space heaters, in which the user will be able to program an operating temperature sequence. However, the $5-to-$6 price tag for a microprocessor package is too high: the cost-effective level is around $2.50, says Ed Irelan, manager of human factors engineering at Edison in Columbia, Mo.

He says he is stymied over the cost, despite extensive developmental help from General Instrument Corp. and Texas Instruments Inc. But he and Knott expect the learning curve to drop their way. "It's just too early in the game for us," Irelan notes.

-Larry Marion

1978 FINANCIAL RESULTS

	After-tax return on equity (%)	After-tax earnings (as % of sales)	Debt (as % of equity)
U. S. companies			
Texas Instruments	16.6	5.5	2.3
Motorola	14.6	5.6	22.4
Fairchild Camera and Instrument	12.0	4.6	45.2
Intel	21.6	11.0	0
Mostek	15.8	7.1	25.0
National Semiconductor	17.1	4.6	1.1
Average	16.3	6.4	16.0
Japanese companies			
Nippon Electric Co.	8.1	1.2	485.0
Fujitsu	8.8	2.4	191.0
Hitachi	13.0	2.5	144.0
Toshiba	2.1	1.6	562.0
Average	8.0	1.9	345.0
European companies			
Siemens (Germany)	9.8	2.5	36.8
Philips (Netherlands)	9.0	2.2	57.6
Average	9.4	2.4	47.2

Source: Semiconductor Industry Association

News briefs

Computer makers raise prices
Long noted for its continually decreasing prices, the computer industry is showing signs of succumbing to the pressures of inflation. Honeywell Information Systems, Waltham, Mass., raised computer prices January 21 by 7 per cent, while boosting systems and application software prices as much as 20%. Amdahl Corp., Sunnyvale, Calif., plans to raise prices some 6% to 9% on two- and four-year leases on its 470 series of large-scale mainframes on March 15. Storage Technology Corp., Louisville, Colo. is raising domestic purchase, rental, and maintenance prices between 5 and 15% for its line of data storage products effective April 1. All follow a decision at the end of 1979 by IBM Corp. to raise prices about 5% practically across the board. IBM's year-end results suggest that pricing was too aggressive and was hurting profits. Its 1979 earnings were down 4% to $3,011 million even though revenues had increased nearly 8.5% to $22.863 billion.

Zilog to add specialized 16-bit processor
Zilog Inc. of Cupertino, Calif., plans to introduce a companion processor for its 16-bit Z8000 microprocessors in the second half of 1980. The new processor, called an "Extended Processing Unit", will relieve the central processing unit of specialized tasks such as floating-point arithmetic, database search and maintenance operations, network interfaces, and graphics support functions. The EPUs will use six new Z8000 operation codes to form an extended instruction set, which expands the Z8000 instruction set by more than 256 instructions for each EPU added to the system.

Honeywell mid-level computer replaces two models
Honeywell Information Systems Inc. is replacing two of its earlier Level 64 mid-range computers with a single unit of minimal design and packaging differences. The new Level 64/DPS-330, with 512 to 2,048 kilobytes of main memory, spans the memory range—and exceeds by about 10% the power range—represented by the earlier models, DPS-320 and DPS-350, which the Waltham, Mass., computer maker introduced only last spring [*Electronics*, April 26, 1979, p. 190] to compete with IBM's 4331. The DPS-330, attended by some upgraded peripherals and some new software capabilities, does use main-memory and firmware chips four times larger than its predecessors'. Base price is $79,675, and deliveries will take 90 to 120 days.

Philips Instruments adds a general manager
Completing management changes that began last summer at Philips Test and Measuring Instruments Inc., Robert C. Joseph is becoming general manager of PTMI. Until his new appointment, he was general manager of Ailtech, the microwave instrument subsidiary of Eaton Corp. His major responsibility will be the line of low-frequency oscilloscopes that Philips began to assemble in the U. S. PTMI is a subsidiary of Philips Electronic Instruments Inc., a U. S. operation of the multinational giant NV Philips Gloeilampenfabrieken of the Netherlands.

National unveils five computers
National Advanced Systems, Palo Alto, Calif., has launched an assault on the IBM-compatible computer market with five systems. Aimed at the low and middle portions of the market are the AS/3000 and AS/3000N, priced at $425,000 and $325,000, respectively. The entry-level 3000N is said to provide performance equivalent to that announced for IBM's 4341 processor and the 3000 has 20% to 30% more performance or equivalent to that of IBM's 370/158-3. The processors are manufactured at parent National Semiconductor Corp.'s San Diego Computer Products group. Also introduced are three general-purpose computers, targeted at the middle and upper end of IBM's 303X series. Designated the 7000 family, the processors are made by Hitachi Ltd., under a recent accord. Deliveries begin immediately for the 3000 series, in the second quarter for the 7000 series.

European competitors, the latter have higher debt-to-equity ratios (see table on p. 45). "Easy access to capital permits our foreign competitors to finance access to our market, which presently constitutes more than half the world market," Noyce argues.

Testifying for the Electronic Industries Association, Motorola's Welty rejected the ITC's conclusion U. S. losses to Japan of IC market share stem from American underinvestment after the 1975 recession. "The U. S investment in plants and equipment has steadily increased, except for the flat year of 1975, when Japanese investment declined," he says.

The soaring U. S. market demand in 1976–78 exceeded forecasts of "moderate to healthy sales increases," while Japan's home markets did not—so excess Japanese chip-making capacity filled the U. S. shortage, he says.

VLSI program. Welty also contends that Japan's government-funded and -coordinated $250 million Very Large-Scale Integration Program made possible the 1977 introduction of 16-K RAMs by six companies "in five quarters or less." That was half the time it took the same firms to develop the simpler 1-K RAM, he says.

The VLSI effort was defended by Tanaka, who argued that the Pentagon's $210 million Very High-Speed Integrated Circuits effort [*Electronics*, Jan. 3, p. 81] could be called a Government subsidy by using the logic the U. S. producers have applied to Japan.

"In spite of alarms sounded by the SIA," Tanaka argues, "Japan accounts for only about 6% of U. S. semiconductor imports and only 1.6% of annual consumption. In the absence of sustained shortages in the [U. S] domestic supply, these percentages would, of course, be substantially lower."

Tanaka also pointed to "a significant negative trade balance of semiconductors with the U. S." In 1978 imports totaling $230 million against exports to the U. S. of $74 million, he says. -**Ray Connolly**

Only TEAC makes both on-site and in-lab cassette data recording equipment.

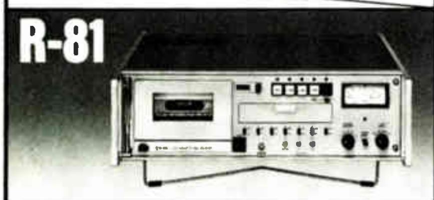
Have you been going to one manufacturer for your portable data recorders, and to another for recorders for your lab? TEAC makes things easier for you by offering a complete line of data acquisition equipment including both portable and lab models. Complete compatibility allows you to collect data in the field with a convenient portable recorder and bring it back to the lab for analysis on a full-feature lab recorder.

Of all our models, you'll find that our cassette-format recorders are the most convenient. The R-60, R-61 and R-61D portable cassette data recorders have proven extremely popular because of their ruggedness, stability of operation and light weight. They can record four channels of data in a choice of DR or FM format.

Back in the lab, the R-80 and R-81 provide big-recorder performance and features without using up a big amount of space or budget. Both can be mounted in standard E.I.A rack panels if desired.

These five cassette data recorders are part of a complete line of data acquisition equipment. Only TEAC can handle *all* your data acquisition needs.

Feature Comparison Chart

Model / Feature	Channels	Record System*	Tape Speed	Freq. Response	Power	Weight
R-81 	7	FM (DR: option)	4 speeds (7½, 3¾, 1⅞, 15/16ips)	FM: DC – 5k Hz at 7½ips	DC Car Battery (AC with AD-80)	12kg approx.
R-80 	4	FM (DR: option)	4 speeds (7½, 3¾, 1⅞, 15/16ips)	FM: DC – 5k Hz at 7½ips	DC Car Battery (AC with AD-80)	12kg approx.
R-61 	4	Ch-1: FM/DR Ch-2: FM/DR Ch-3: FM Ch-4: FM	1 speed (1⅞ips)	DR: 50 – 8k Hz FM: DC – 625 Hz	DC Car Battery with CL-61 (AC with PA-2)	4.7kg approx.
R-61D 	4	Ch-1: DR/FM Ch-2: DR/FM Ch-3: DR Ch-4: DR	1 speed (1⅞ips)	DR: 50 – 8k Hz FM: DC – 625 Hz	DC Car Battery with CL-61 (AC with PA-2)	4.7kg approx.
R-60 	4	FM	1 speed (1⅞ips)	FM: DC – 625 Hz	AC	6.5kg approx.

* Noise Comp. & Memo capable

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Digital service will need 110 MHz Xerox tells FCC

Xerox Corp. says that from the year 1990 to 2000 market demand for competitive digital termination systems (DTS), like that for its proposed XTEN telecommunications network, will require a larger frequency allocation from the Federal Communications Commission—an extra 20 MHz for shared use in local metropolitan service areas, in addition to a 90-MHz allocation for DTS national service, will be necessary. Xerox counsel and former FCC chairman Richard Wiley says the commission's proposed initial allocation of 60 MHz in the 10-GHz band, with 30 MHz held in reserve, **"will not be sufficient to meet the public need" for national DTS service.** The company says 1990 market needs will require a transfer rate of 105 Mb/s in the busy peak hour, rising to 160 Mb/s by 2000.

Although the National Telecommunications and Information Administration supports the FCC's proposed 60-to-30-MHz split and wants allocation quickly [*Electronics*, Jan. 17, p. 55], the docket 79-188 issue **may be stalled by a developing dispute between the FCC and state regulators** (supported by American Telephone & Telegraph Co.) concerning the FCC's assumption of jurisdiction over DTS.

Commerce forecasts 1980 growth for EDP and systems . . .

Large backlogs will help carry strong growth in 1980 shipments of the aerospace, computer, and electronic systems and equipment industries. **But a softening national economy will produce slippage in sales of electronic components and calculators.** Those are the forecasts of the Department of Commerce in its new 548-page "U. S. Industrial Outlook 1980" published at January's end by the Government Printing Office. Aerospace shipments—including aircraft, missiles, spacecraft, engines, and parts—rose 34% last year to an estimated \$55.2 billion, and are expected to reach \$68.9 billion this year, reflecting the steady rise in commercial air transport orders. Shipments of computers and related equipment for 1979 will total an estimated \$20.9 billion, a 22% gain on the year before, and will add 10% more this year, rising to \$23.2 billion. But industry shipments of calculators and accounting machines, expected to show a rise in 1979 to \$1 billion, will slip back 3% to \$970 million this year, with cuts coming largely in the low end of consumer lines as the economy softens.

. . . with components expected to drop 4% to \$19 billion

Electronic systems and equipment shipments, the bulk of them custom tailored for the military, Federal aviation, and space agencies, are expected to climb 11% to \$20.1 billion this year on top of a 12.6% rise last year from 1978's level of \$16 billion. Telephone and telegraph equipment shipments this year are expected to rise 10% to close to \$10 billion following an 11% rise from the 1978 level and to continue rising at a compound annual growth rate of 9.1% to \$13.6 billion in current dollars in 1984.

Components industry shipments, however, are expected to dip 4% to \$19.4 billion from the 1979 high of \$20.3 billion—a rise from the year before. Unlike the somewhat more stable commercial, military, and industrial markets, the components downturn is expected to result from a weakening consumer electronics market. Integrated circuit shipments, which the Commerce Department estimates soared 29% last year to reach nearly \$5.1 billion, are projected to drop 5% to \$4.8 billion in 1980. A better long-term outlook for components is projected, however, for the annual average real growth is expected to be 9.4% through 1984.

Washington commentary

H.R. 6121: another disaster for Van Deerlin?

The hue and cry against Rep. Lionel Van Deerlin's latest bill to rewrite the Communications Act of 1934 is louder than ever as the staff of his House Interstate and Foreign Commerce communications subcommittee continues to flip-flop on key issues of deregulation and the future role of American Telephone & Telegraph Co.

Though the California Democrat's 1978 bill called for open competition and would have required AT&T to spin off its Western Electric manufacturing operations as a subsidiary, it was weak on means of implementation despite 20 months of hearings, studies, and analyses [*Electronics*, June 22, 1978, p. 58]. The bill's problems were compounded by the fact that it tried to put deregulation of two vastly different industries—telecommunications and broadcasting—into one legislative document.

That effort, largely the product of subcommittee counsel Harry M. Shooshan III and his staff, failed badly. It was not helped by the fact that virtually none of the other 14 subcommittee members was consulted as the draft was proposed.

The search for consensus . . .

Realizing his error, the subcommittee chairman called for a complete rewrite of the bill dropping broadcasting deregulation to concentrate on telecommunications. Subcommittee staffers were also required to come up quickly with a new bill that would represent a subcommittee consensus. That is now H. R. 6121, and Van Deerlin is anxious to push it to passage before Congress adjourns early for the election campaign. But Van Deerlin may again be disappointed, despite President Carter's call this month for reform of telecommunications regulation this year.

Van Deerlin's December rewrite has become January's horror story for competitors of AT&T, whose vice chairman James Olson has called the bill "probably the best piece of telecommunications legislation to be produced thus far." That is because the draft rewrite is much softer on AT&T. Not only would it lift the 1956 antitrust consent decree to permit AT&T to compete in nontelephone markets, but it would leave AT&T, Western Electric, and Bell Laboratories intact under one financial roof, requiring formation of new subsidiaries only to market new services and products of the parent.

Like its predecessor, the draft rewrite is incomplete and so sloppily written that it is producing criticism from almost every quarter. Federal Communications Commission Chairman Charles Ferris put his as diplomatically as he could in a letter to Rep. Harley Staggers (D., W.Va.), chairman of the Interstate and Foreign Commerce Committee and Van Deerlin's subcommittee overseer. "It is essential that there will be a full delineation of the bill's practical effect on AT&T structure—and its consequent economic impact on various telecommunications markets in which AT&T has such a dominant role. These organizational and competitive effects are not fully apparent on the face of the bill," Ferris contends.

The challenges of the Ad Hoc Committee for Competitive Telecommunications are more straightforward. Composed of eight large and small intercity transmission companies, ACCT told Van Deerlin his draft reflects "confusion about the relation between competition and deregulation" that "could easily have anticompetitive effects" by giving "AT&T a new license to try to thwart or eliminate the limited competition which has been slowly developing during the last decade." ACCT's members include GTE Telenet Communications, Graphnet, MCI Telecommunications, Midwestern Relay, RCA American Communications, Satellite Business Systems, U. S. Transmission Systems, and Western Telecommunications. Van Deerlin is also getting strong criticism from the Consumers' Union, the Computer and Business Equipment Manufacturers Association, Control Data Corp., and a team of four trade associations: the Computer and Communications Industry Association, the Independent Data Communications Manufacturers Association, the North American Telephone Association, and the Association of Data Processing Service Organizations.

. . . and for clarity

Control Data complains that H. R. 6121's language contains "many new words and phrases" without defining them, making each "a potential source of litigation." CDC's examples of such key words: competition, intra-exchange, interexchange, network, terminal equipment, market or submarket, data processing, and shared use. CCIA chief Jack Biddle agrees that the bill's vague language could "take the courts 20 years to untangle."

The response of Van Deerlin's staff at January's end was to unveil some 70 pages of amendments of H. R. 6121 to clarify and perhaps correct the bill's weaknesses. Capitol Hill is still in process of reacting to those amendments. But if past performance is a valid measure, they still have a long way to go before H. R. 6121 becomes the law of the land.

-Ray Connolly

Racal moves to acquire some Decca operations

A major new British electronics merger with combined sales of $933 million a year is in the offing if Racal Electronics Ltd. of Backnell, Berks., succeeds in its bid to take over part of Decca Ltd.'s operations. **Decca, of London, has already spun off its ailing television manufacturing and audio recording businesses,** leaving the industrial and commercial interests, which include radar and navigation systems, for Racal. In an earlier consolidation, Thorn Electrical Industries Ltd. took over EMI Ltd. to form an enterprise with $4.32 billion a year in sales.

Italy wants in on Franco-German satellite project

Italy's minister for Post and Telecommunications, Vittorino Colombo, recently **lambasted the joint French and German decision to exclude outside participation in a direct-broadcast television satellite project** [*Electronics*, Dec. 6, 1979, p. 66]. The Italian minister, calling himself a "good European," suggested after talks with his counterpart in Germany that the Franco-German decision to handle the project alone would confer on the two countries an advantage in television exchange that "should be shared" with other major European nations. Colombo also argued that Italy's experimentation with ultrahigh-frequency transmission could be beneficial to both its European neighbors.

Retrieval controller finds 10 heads better than one

To speed data retrieval from large stores, International Computers Ltd., London, has introduced a content-addressable file store (CAFS) using an old technique with a new wrinkle. The CAFS 800 allows 10 times as many simultaneous inquiries as conventional, software-based information retrieval systems, according to ICL. **To accomplish this, the company uses 10 read heads that search the disk surfaces simultaneously.** One CAFS 800 controller can handle up to 14 disks with a capacity of 60 megabytes each for a total of 840 megabytes.

Bell Canada hooks laser-source fiber optic link to radio

The latest fiber-optic technology development by Bell Canada is the placing of a fiber-optic cable for the first time as an "entrance link." **This link connects the switched telephone network with an 8-GHz microwave radio system used for long-distance transmission.** The 8-km fiber cable is in Kitchener, a city 109 km southwest of Toronto.

The light sources in the trial are 5-mW injection lasers. They send data at a 44.7-Mb/s rate, the equivalent of 672 voice conversations on each fiber pair. This is a change for Bell Canada, which until now has used light-emitting diodes.

Matsushita, Victor to cooperate on VHD video disk . . .

Japan has taken a big step toward a video disk standard with the announcement that Matsushita Electric Industrial Co. and Victor Co. of Japan will promote Victor's VHD (Video High Density) disk as a standard. The move is significant because Matsushita is the nation's leader in television; also, **it deals a blow to whatever hopes are entertained by RCA Corp. and Philips of the Netherlands that the winner of their video disk battle in the U. S. would also pick up Japan by default.**

Although Matsushita owns a 50.2% equity in Victor, the two are competitive. They have cooperated in the past, though, on the VHS (Video Home System) video cassette recorder first developed by Victor and with Sony Corp. on its U-matic VCR. As for which way Sony will go on video disks—a decision that could hold the key to success of the Matsushita-Victor system—the company will say only that it is studying the situation.

. . . as Matsushita lightens the load of portable VCR

At the same time, Matsushita has taken steps to make its VHS portable video cassette recorder lighter, smaller, less energy-hungry, and less expensive than previous models. It has also added a 6-hour play mode. **Size, weight, and power consumption are about 60% that of the former portable,** and power demand of 5.6 W means a battery pack weighing 1.5 lb instead of the former 2.9 lb for the same 1-hour recording time. The recorder itself now weighs 11.7 lb and measures 11.8 by 4.5 by 9.8 in.

UK software house gets GSA approval for Cobol system

With an eye to the future role that microprocessor-based systems will play in U. S. government data-processing activities, the British software house, Micro Focus Ltd., London, has obtained General Services Administration approval for its high-level microprocessor-based Cobol compiler. **The certification is for Federal low intermediate, which combines ANSI Level 1 and Level 2 and is typically implemented on minicomputers.** The software, called CIS Cobol—for Compact Interactive Standard—is a portable system for compiling, debugging, and executing Cobol programs and is sold in off-the-shelf packages available for Intel 8080, Intel 8085, Zilog Z80, and DEC LSI-11 chips. The company sees a total market for its product of $27.36 million over the next three years.

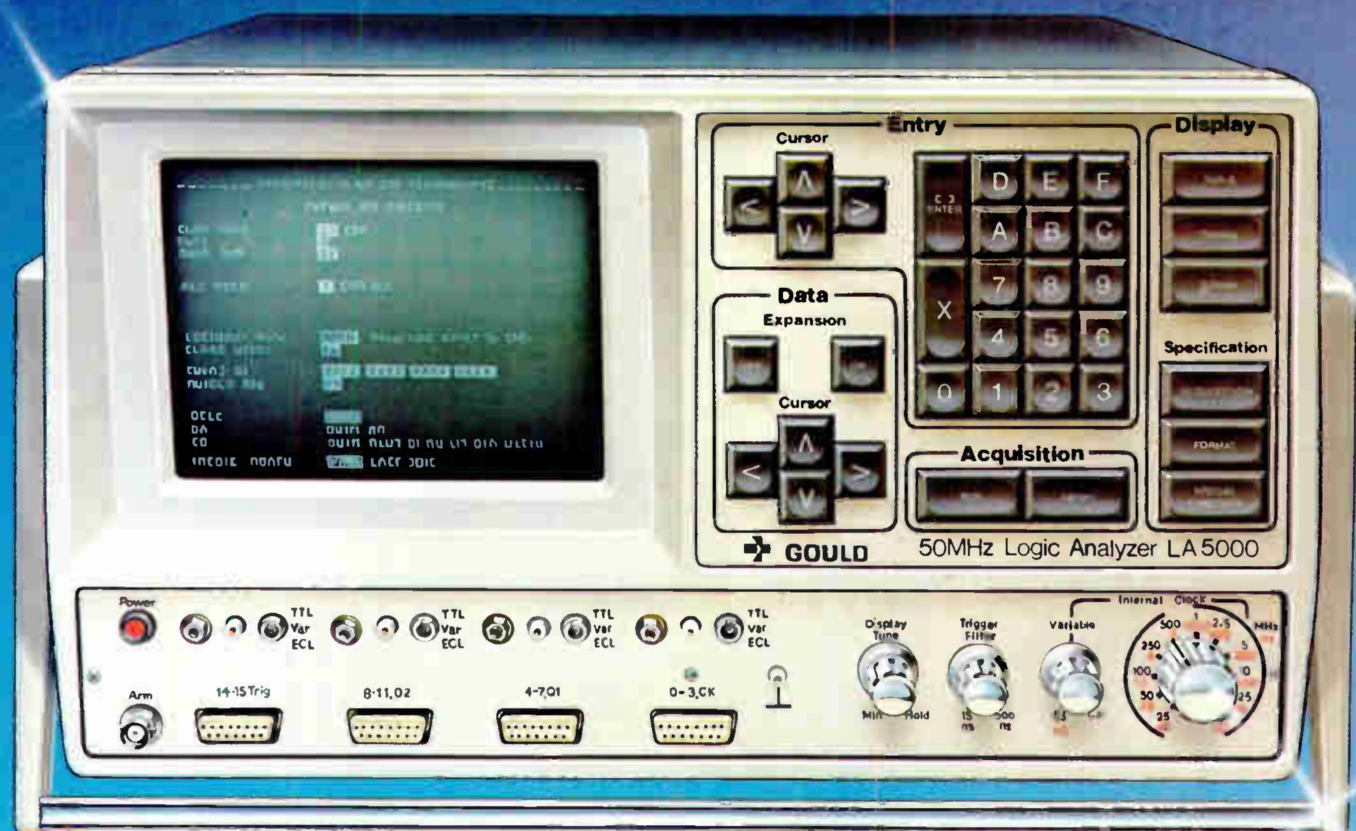
CII-HB plans own IC lab for VLSI chips

Worried about turnaround delays in development of VLSI semiconductors, computer maker CII-Honeywell Bull is starting up its own integrated circuit development lab. The work, to be done at the Franco-American company's research center in the Paris suburb of Louveciennes, will focus on n-channel MOS technology. **The company intends to use ion implantation and/or plasma etching to get at least to the prototype stage** for circuits in which transistors will have channel lengths of less than 1.5 μm and oxide gates about 400 Å thick.

Addenda

Thomson CSF of France has put all its computer-related activities and its scientific instrument subsidiaries under the wing of a holding company—Thomson CSF Informatique. **The dozen companies in the new grouping had sales of some $430 million,** about two thirds of which came from hardware, some 20% from software and systems service, and the balance from scientific instruments. . . . Tong Yang Nylon Company Ltd. in Seoul, Korea, will in March start turning out **a licensed version of Hitachi's HITAC L-320 intelligent terminal,** which the Japanese company designed for distributed processing in billing applications. The two companies concluded a seven-year agreement last year that calls for Hitachi to send engineers to Korea and provide information to the Korean company's engineers who visit Japan. . . . The U.S. Postal Service has bought a DP-100 voice-recognition system from Nippon Electric Co. for its parcel post facility at Rockland, Md., where it will be used for sorting. **The system can recognize strings of words said without pause** [*Electronics*, April 13, 1978], giving it an advantage over competitive systems.

MICROPROCESSOR GLITCHES: MEET YOUR FIXER.



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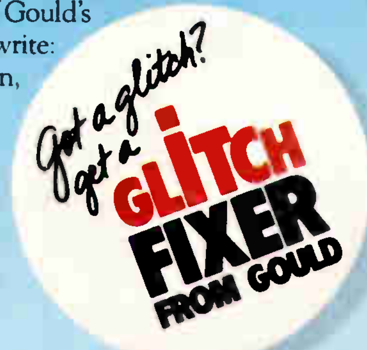

Circle 57 on reader service card

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by John Gosch, Frankfurt bureau manager

Iodine vapor deposition works at low temperatures, virtually eliminating diffusion effects

Low growth temperatures and highly selective silicon deposition are the hallmarks of a silicon epitaxial process developed by AEG-Telefunken. Called Locep (from "local epitaxy"), it could have a big impact on device fabrication.

Because there are virtually no diffusion effects with either the silicon or the dopants, very abrupt pn junctions can be made. Consequently the process lends itself to producing extremely thin epitaxial layers such as may be needed for very large-scale integrated circuits, says Peter Braun, the developer of Locep.

Cooler. Developed at AEG-Telefunken's semiconductor facilities in Heilbronn, West Germany, the process works at temperatures as low as 600°C, a big drop from the up-to-1,200°C levels of standard methods. And since the process allows stable thermodynamic equilibrium conditions to be maintained, silicon deposition can be highly selective.

The key is the use of iodine to transport silicon to the silicon substrates for deposition there. Iodine reacts with silicon at a much lower temperature than do other halogens, such as chlorine, normally used in vapor deposition.

The very abrupt pn junctions that can be made permit the fabrication of, say, zener diodes with sharp breakdown curves. "It's even possible for Locep-made zener diodes to have voltage ratings down to 2 volts," Braun says.

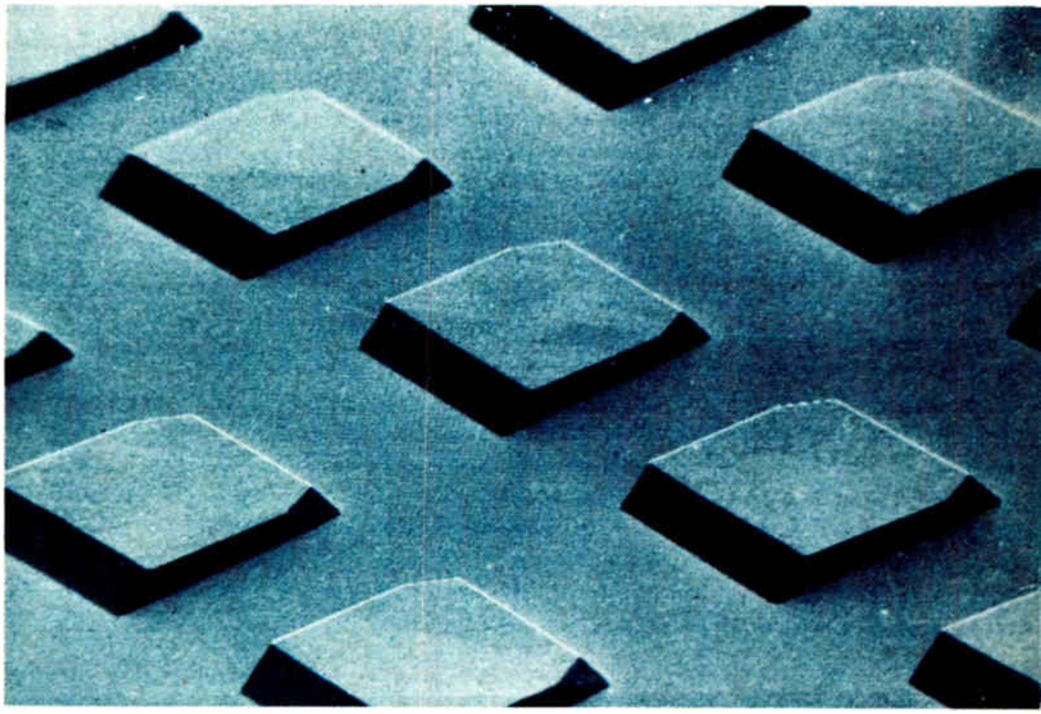
Further, because silicon deposition is so selective—that is, highly restricted to nonmasked substrate areas—sharply defined mesalike structures with very smooth surfaces can be made (see photo). Such structures could find use as collectors or emitters in certain types of transistors or ICs.

Well-defined. The process also allows the deposition of layers as thin as 2 micrometers and featuring an even, controlled distribution of dopants. With conventional processes, however, the dopants may penetrate the substrates.

On the face of it, the Locep process seems to resemble an iodine-based method worked out at France's Sescosem some years ago. But this method apparently does not reach down to 600°C. Neither does it seem suited for producing very thin layers or zener diodes with voltage ratings as low as those achievable with the Locep technique.

In implementing the process, Braun and co-worker Wolodymyr Kosak use a quartz tube about 100 centimeters long and 7 cm in diameter. Inside the tube is a solid source of silicon and dopant at one end and a number of silicon substrates at the other. Crystalline iodine is put near

Smooth work. Deposited with AEG-Telefunken's Locep process, the mesalike epitaxial areas show no growth disturbances other than border faceting.



the silicon source. After loading, the tube is evacuated, sealed, and inserted into a diffusion furnace, Braun explains.

The furnace heats the source up to 100°C more than the substrates, causing the now gaseous iodine to transport the silicon (and dopant) from the source to the substrates.

Although silicon can be grown expitaxially at about 600°C, practical devices need at least around 700°C, Braun says. The reason: as the temperature decreases, epitaxial growth becomes more sensitive to the substrate surface conditions. Nonstandard surface cleaning methods would have to be used, and that would drive the costs up.

Available. The deposition rates are about 1 μm per hour at 700°C and roughly 15 μm per hour at 900°C.

AEG-Telefunken is already using its process for low-voltage zener diodes with sharp breakdown curves. High deposition selectivity reduces the number of fabrication steps notably, Braun points out. Rated at 400 milliwatts or 1 watt and at voltage levels below 6 volts, the diodes are now being marketed.

A disadvantage of the Locep process, Braun says, is the need for a quartz tube for the transport system. But that, he adds, is more than compensated for by the advantages of high device yield and reliability that the process affords.

Present work at the Heilbronn facilities is aimed at producing selective collector and emitter areas on transistors. Also being investigated are Locep-based power zeners covering high voltage ranges, as well as silicon deposition over large areas for VLSI use.

Japan

Multilayer process yields ferrite chip inductors for automated installation

Hybrid-circuit manufacturers now have a new monolithic device. TDK Electronics Co. has started making monolithic ferrite inductors by a process like the one it uses to fabricate multilayer chip capacitors. The new devices are the same size as the chip capacitors and can be installed with the same automatic equipment [*Electronics*, Jan. 17, p. 63].

Because their figure of merit, Q, is on the order of 10 to 30, they are suitable for use mainly as chokes for color TV, video recorder, and video camera circuits; for television tuners; and for noise filters in microcomputers for automatic applications. However, the company expects to develop similar inductors with Qs several times as large for use as peaking coils and resonant circuits.

Alternating. The monolithic chip coils are fabricated of alternate layers of ferrite and conductor only—no other materials are used—with ferrite layers at the top and bottom of the device. Ferrite also surrounds the outer edges and fills in the center of the coil, creating a closed magnetic path that minimizes leakage flux. The coil itself is made of silver paste, with palladium covering the two end-terminal connections to protect them during soldering.

The coil is more difficult to fabricate than a capacitor because it consists of a continuous helix with adjacent turns insulated from each other. Four depositions are required for one turn: slightly more than half a turn of conductor, then half a layer of ferrite insulator, slightly more than half a turn of conductor, and finally half a layer of ferrite. The half turns are connected at their overlaps during the depositions to form the coil.

High volume. Although many operations are required, they can be automated and a large number of devices fabricated in each batch. Thus TDK says that when produced in high volume the chip inductors will be competitive in price with discrete devices, as well as being more convenient to use.

Two sizes will be available, with a wide range of inductances. The smaller chips are 3.2 millimeters long by 1.6 mm wide by 0.6 mm thick and have an inductance of 10 nanohenries to 2.4 microhenries. The larger ones are 4.8 mm long by 2.4 mm wide by 1.1 mm thick and initially will be available within an inductance range of 2.4 to 50 μH, which will be increased to 220 μH.

The firm says that production capacity is limited because the inductors are manufactured with the same equipment as its capacitors. It does not know when it can start exports. -Charles Cohen

Great Britain

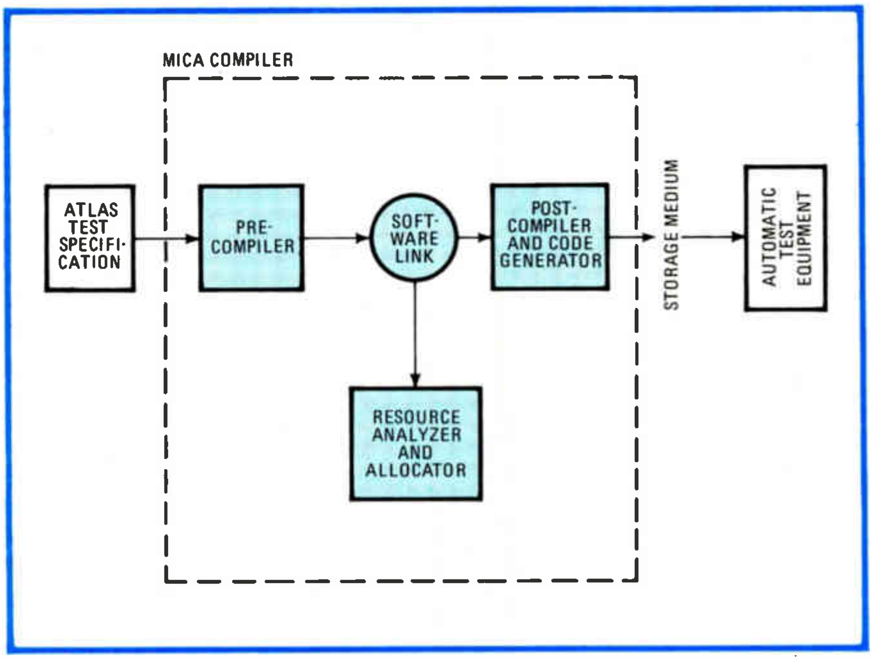
Compiler translates Atlas for minis

Atlas was conceived as a high-level programming language for expressing equipment test procedures in both man- and machine-readable form. But it has generally succeeded only in the first of these objectives—when setting up automatic test equipment, Atlas programs have to be interpreted manually or at best semiautomatically.

Now a small British software company has cracked the considerable intellectual difficulties in the way of developing an Atlas compiler. It has delivered its first commercial software systems to LM Ericsson, the Swedish telecommunications manufacturer, and the British Aircraft Corp.

Needed. The company, Warren Point Ltd., calls its compiler MICA, for Machine Independent Compiler for Atlas. It has invested 50 man-years in its development, funded in part by Britain's Ministry of Defence, which sees a major logistics need for the compiler.

Because the potential market is limited compared with commercial data-processing software, the Stevenage, Herts., company aimed to make MICA run on as many machines as possible. The software was therefore written in Cobal 66, a



Holding up Atlas. The Machine Independent Compiler for Atlas (MICA) designed by Warren Point Ltd. is organized to put all the machine-dependent parts in one program segment

high-level language for real-time performance that is well supported with compilers available for several machines.

Additionally, says John Mansfield, MICA project manager, "we have put all the machine-dependent parts of the compiler in one program segment, so to tailor the system we only have to make changes in that area." Some 85% to 90% of the software is standard, he adds.

Right now, the compiler runs happily on a host DEC PDP-11/34 under the RSX-11M operating system, and, says Mansfield, portability has been demonstrated for five target ATE systems. Furthermore, a compiler is being developed by the Royal Signals and Radar Establishment for the GEC 4080 computer, and Warren Point is to develop others for Texas Instruments' 990 minicomputer and also for Computer Automation's LSI-2 if the software can be fitted in.

Impetus for Atlas came during the 1960s from the airlines, which faced a huge problem testing and maintaining avionic systems internationally. Through Aeronautical Radio Inc., or Arinc, the international air standards committee, they defined a high-level computer language for expressing test procedures unambiguously in English-like statements.

Wordy. Designed to meet these needs, Atlas began with a large vocabulary of 200 words but quickly expanded to a huge one of 440 words. In contrast, says Leo Rhodes, a company executive associated with MICA from its beginning in 1973, a high-level language like Fortran has a vocabulary of 40 words.

A typical Atlas statement, for example, is: APPLY, DC SIGNAL, VOLTAGE 10V ERRLMT "−0.1V, CURRENT MAX 0.2A, SNX HI J1 LO J2 $ ("Apply a dc signal of 10±0.1 volts and not more than 0.2 ampere between high pin J1 and low pin J2").

But the task of automatically translating these abbreviated statements into the machine's limited instruction set has proved formidable. The problem is posed by the semantic and syntactic rules governing them, since in English the meaning of a word can depend on its position in a sentence. "We are beginning to face some of the problems encountered in automatic language translation," Rhodes says.

To overcome these difficulties, Warren Point adopted a three-stage compilation process. First, a test program is entered into the host computer and a precompiler checks for syntactic and semantic errors, after which an intermediate code is produced.

In a second pass through the host computer, the intermediate code is acted on by a resource-analyzer program. This program describes the capabilities of the target ATE system, checks that its resources—such as measuring instruments—are available, and allocates these resources to the statements calling them up.

Thus modified, the intermediate machine code is acted on by a postcompiler to produce machine code for the target system. Filed on floppy disk, paper tape, or other storage medium, the compiled program is normally executed directly by the ATE hardware. The result, says Geoff Evans, managing director of Warren Point, is "a complex piece of software, challenging and elegant."

The cost for a complete MICA software system depends on the user's requirements, with subsets available for digital or analog testing. But, says Mansfield, most systems work out at about $200,000.

The availability of a proven low-cost Atlas compiler will help to boost all-automatic testing, Evans believes, and he predicts a big increase in the use of Atlas. This trend has already begun in the defense sector, where it is a standard language for contractors and government agencies in the U. S. and many parts of Europe. But the biggest market will prove to be for industrial and commercial systems. -Kevin Smith

Japan

Chip sensor shrinks color video camera

A new single-chip color video sensor for use in video cameras boasts higher sensitivity, better resolution, and a lower tendency toward blooming than present devices. Matsushita Electric Industrial Co., which developed the device, says it will be ideal for cameras designed for the con-

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Circle 63 on reader service card

Around the world

Siemens aims hi-fi equipment at ailing Japanese market . . .
Even though the Japanese audio market is not exactly robust, Siemens-Electrogeräte GmbH is banking on the increasing popularity of European-designed equipment in the island nation and is introducing high-fidelity equipment in Japan. A household-goods subsidiary of Munich-based Siemens AG, the West German firm will have its equipment built and distributed by Sanyo Electric Trading Co.

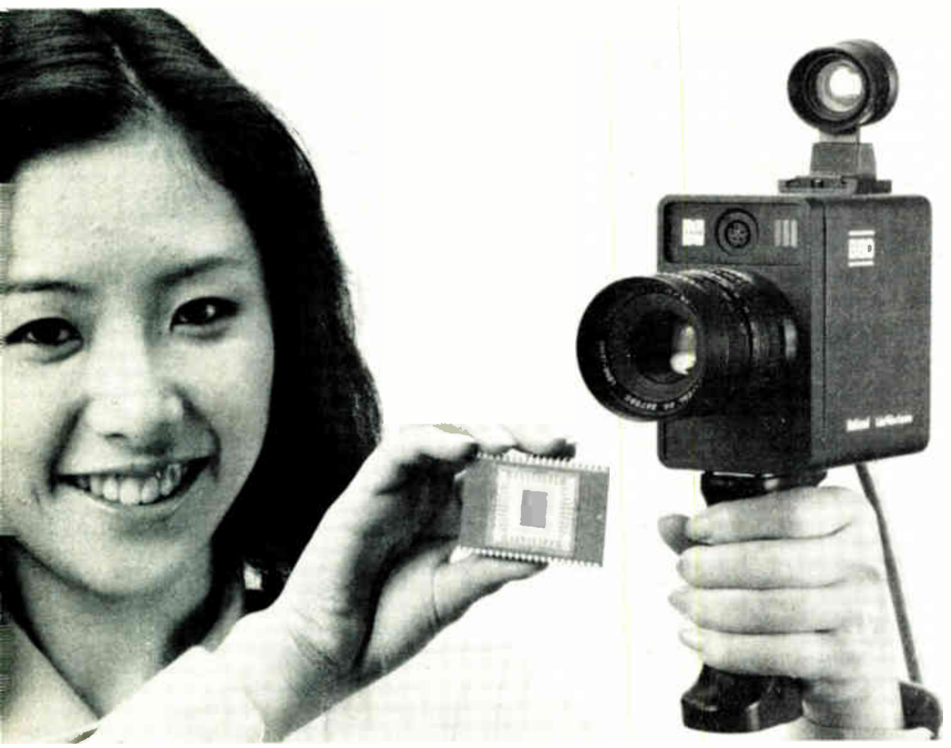
. . . and eyes U. S. power transistor facility
Continuing its drive to become more active on the U. S. semiconductor market, Siemens AG is bidding to take over the semiconductor activities of Chicago-based FMC Corp. The deal would involve only the power transistor business, which is said to have been worth $20 million in 1979.

Japanese fax goes to British firm
The British National Enterprise Board–backed Nexos Ltd. will expand its automated office equipment line by adding a high-speed facsimile system from Japan's Oki Electric Industry Co. The London-based company is also discussing possible areas of collaboration with Plessey Office Systems Ltd. Talks are likely to center on the latter company's PDX all-digital private branch exchange, which Plessey sees as central to its automated office system strategy.

sumer market because it will make for products that are compact, light, and easy on their batteries.

The firm says that its prototype camera is only one third the volume and one half the weight of those using image pickup tubes. It is 10 centimeters high, 5 cm wide, and 11.5 cm deep. With a 6× zoom lens, it weighs 1.2 kilograms.

Reduced. New color video sensor chip enables Matsushita to make a phototype video camera one third the volume of those using image pickup tubes.



In addition, power requirements are down because the chip and its peripheral circuits work with low voltage and current. Also, they do not need the power-hungry deflection yokes or dc-to-dc converters that image pickup tubes do.

The sensitivity of the chip, which will be discussed at next month's International Solid State Circuits Conference in San Francisco, is higher than that of previous types because the entire front surface is a photoconductive layer for converting the image photoelectrically. It is also higher because this layer, a thin-film zinc selenide–zinc cadmium telluride heterojunction for vidicon-type tubes, is more sensitive to blue light than silicon photosensors.

Scan. Image signals are transported for vertical scanning by bucket-brigade-device circuits in the silicon chip underlying the photosensor. Horizontal scanning is performed by charge-coupled-device circuits also on the same chip. In contrast, in monolithic semiconductor devices the area is divided between the sensing and transport functions; since only a portion of the area is available for image sensing, sensitivity suffers.

Matsushita claims that the mosaic color filter laminated onto its device has higher resolution than previous filters having the same number of elements. The chip is 13.0 millimeters (512 mils) vertically by 17.0 mm (669 mils) horizontally, with a photosensitive area of 10.3 by 13.5 mm (407 by 531 mils). This area has 470 pixels vertically by 375 pixels horizontally.

The company says that resolution is 280 TV test-pattern lines horizontally by 480 lines vertically and that the signal-to-noise ratio is at least 43 decibels for a scene illumination of 500 lux when the lens aperture is *f*/2. Blooming, though, is suppressed for highlight areas up to 120 times as intense as the saturation signal.

Consumers will have to wait until Matsushita gears up for mass production and gets costs under control. In the meantime, the Osaka firm expects to sell a limited number of cameras later this year at about $4,000 each. **-Charles Cohen**

Flat-panel displays find special jobs

Instead of trying to force CRTs out of business, designers seek applications where size, power, and capacity are factors

by Roger Allan, Components Editor

After 25 years of futile attempts to replace the cathode-ray tube, researchers working on flat-panel displays have abandoned that goal. They are concentrating instead on applications where the CRT—because of its bulk and high power dissipation or its information-handling shortcomings—is less than ideal or cannot do the job at all. Taking that design tack, a number of companies using different technologies are enjoying considerable success.

Major flat-panel display technologies competing for special applications are thin-film electroluminescence, gas-discharge or plasma panel, and liquid-crystal displays. Light-emitting-diode display panels have also surfaced in some applications.

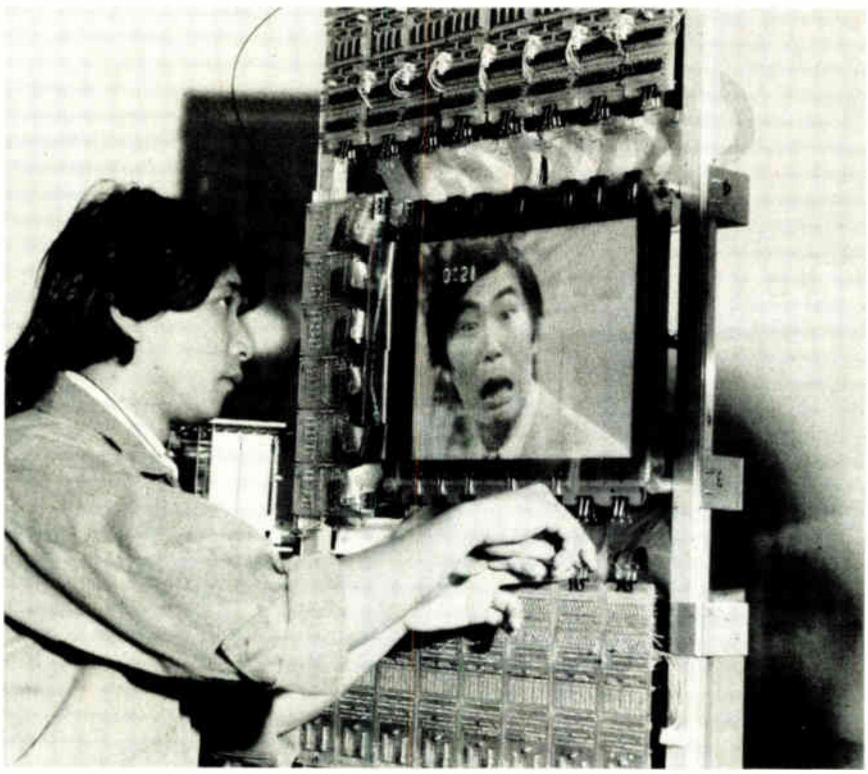
Most successful over the past four to five years have been ac plasma panels. On the other hand, fast-moving developments in LCDs and dc plasma panels promise some radical changes in large-screen flat panel displays within the next year or two, with many coming from Japan.

The many major companies turning out large numbers of ac plasma panel displays make it clear that this is a mature technology. Though the technology for making large-screen flat-panel ac plasma displays able to show thousands of characters is here, it is limited by the high cost of the driver electronics, which also tend to be bulky and complex. And colors are limited to orange and green.

Two companies that spun off the original Digivue effort of the University of Illinois and Owens-Corning Corp. have been selling ac plasma panels for special applications. One of these, Photonics Technology Inc. of Luckey, Ohio, has developed with Science Applications Inc. of La Jolla, Calif., the world's largest ac plasma panel, a 24-inch-diagonal unit that can display over 21,000 characters. Used by the military, the glass panel has a 1,024-by-1,024 addressable matrix and a resolution of 60 picture elements per inch. The active display area is 17 by 17 in. and overall panel thickness is 0.5 in. The firm is developing a 39-by-39-in. panel with resolution of 50 to 60 lines/in. Plasma ac panels are not inexpensive. The Photonics 24-in. panel, for example, costs $45,000 for quantities of less than five. And a dozen or more other companies make dc panels.

The other spin-off is Electro Plasma Inc. of Millbury, Ohio, which is partly owned by A-T-O Inc. of Willoughby, Ohio. To complete the tie, another A-T-O subsidiary, Interstate Electronics Corp. of Anaheim, Calif., has marketed some of Electro Plasma's panels.

Dc plasma displays are also popular. Burroughs Corp. in Plainfield, N. J., sells the dot-matrix Self Scan and formed-character Panaplex panels. Others like IEE Inc., Van Nuys, Calif.; Cherry Electrical Products Corp., Waukegan, Ill.; Dale Elec-



Making a face. NHK's planar positive-column flat panel display is said to offer better luminance, luminous efficiency, and video quality than conventional dc plasma panels.

tronics Inc., Columbus, Neb.; and Beckman Instruments Inc., Scottsdale, Ariz., also sell dc plasma panels. Some of the largest dc plasma panels like Burroughs' 12-row 40-character Self Scan II show up to 480 five-by-seven-dot-matrix characters. IEE sells a similar panel known as the Argus.

The stumbling block for dc plasma panels has been the difficulty producing a panel with a large number of characters at a low enough price. But it costs less to drive dc plasma panels than ac models, and dc panels have more color capability.

One manufacturer of displays that believes it has licked the problem of high cost in a large multicharacter dc panel is Lucitron Inc., Northbrook, Ill. It was founded in June 1978 by a group of scientists when Zenith Radio Corp. closed its research and development facility. Lucitron has been working jointly with GTE Laboratories, Waltham, Mass., on a large-screen dc plasma panel, and will have samples of a 10.5-in.-diagonal color dc plasma panel by the middle of this year. The panel will be 3 in. thick and will use glass 0.125 in. thick. Its aspect ratio will be about 4:3. As explained by Lucitron's president Joseph Markin, "It is not a question of producing such panels, but of producing them using low-cost materials for a low selling price."

Lucitron bases its optimism on its patented extensive multiplexing technique. In addition, it is confident that it can keep tooling costs for the new display low. "We'll do better than one-half the tooling costs of the Shadowmask CRT," says Markin. He adds, "Our patented multiplexing schemes allow economy, efficiency, and high brightness levels. We're sure that we can do better than 100 foot-lamberts of brightness and luminous efficiency of 1 to 10 lumens/watt."

One of the interesting aspects is that a full-color Lucitron panel would require less than 100 driver circuits, regardless of panel size. The company will set up a pilot production line this year.

Japanese view. Fujitsu Ltd., NHK (Japan Broadcasting Corp.), and Hitachi Ltd. have all demonstrated 10-in. diagonal dc plasma panel color displays. NHK and Fujitsu have done work on planar positive-column panels. The technique is said to provide better luminance, luminous efficiency, and video quality than conventional dc panels. NHK and Hitachi have both demonstrated 10-in. diagonal panels for portable TV systems, though the picture quality has been poor. Despite that, some display experts feel that the pace of their work gives Hitachi and NHK a shot at producing practical color dc plasma panels for large-diagonal displays.

The Japanese also want to make LCD panels. Matsushita Ltd. and Seiko Denki Co., as well as Hitachi, have made experimental LCD panels for portable TVs. Matsushita, for example, has demonstrated an LCD panel about 1.4 by 1.9 in. with about 240 by 240 picture elements. Hitachi has shown a 3-in. diagonal LCD panel with 240 by 380 picture elements.

The two biggest drawbacks to LCD panels are the material's slow response, particularly in cold temperatures, and its limited color capability. At least in the area of limited-color capability, LCD panels for portable TVs can prove to be acceptable.

American researchers have not neglected LCD panels. Westinghouse Electric Co. in Pittsburgh and Hughes Aircraft Co. in Carlsbad, Calif., have also developed flat LCD panels, the former using thin-film transistors for the drive circuitry. In addition, among other companies that market LCDs with a limited number of characters, Kylex Inc. of Mountain View, Calif., recently succeeded in developing a 40-character LCD with a patented multiplexing scheme [*Electronics*, Jan. 3, p. 151] that significantly advances LCD multiplexing state of the art. Multiplexing is a major problem, particularly for large numbers of characters.

One U. S. firm that is bullish on LCD technology for panel displays is Integrated Display Systems of Montgomeryville, Pa. It is developing dichroic LCD panels that require no polarizers, making them less expensive than conventional LCDs that require polarizers. The largest one developed is a 4-by-9-in. panel with densities on the order of 40 dots/in. A 3-by-7-in. LCD prototype panel is currently being used in Volkswagen automobiles and, says IDS president Thomas Saldi, will be in U. S. automobile dashboards by 1983.

In addition to all the technologies on the market, every major U. S. laboratory is working on thin-film electroluminescent ac panels. Sharp Electric Co.'s U. S. subsidiary, Hycom Inc. in Irvine, Calif., is also developing such panels. Hycom is sampling a 240-by-320-element dot-matrix display made from ac thin-film electroluminescent technology. The sample panel is rated at 1,000 foot-lamberts and a 10-year lifetime to half-brightness levels. □

Big picture. Largest ac plasma panel has 24-in.-diagonal picture and can display over 21,000 characters. It was developed by Photonics Technology with Science Applications Inc.

Letter from Dallas

Companies plug in to Texas

Lower housing costs, availability of labor, and high esteem for the work ethic combine to make Lone Star State attractive

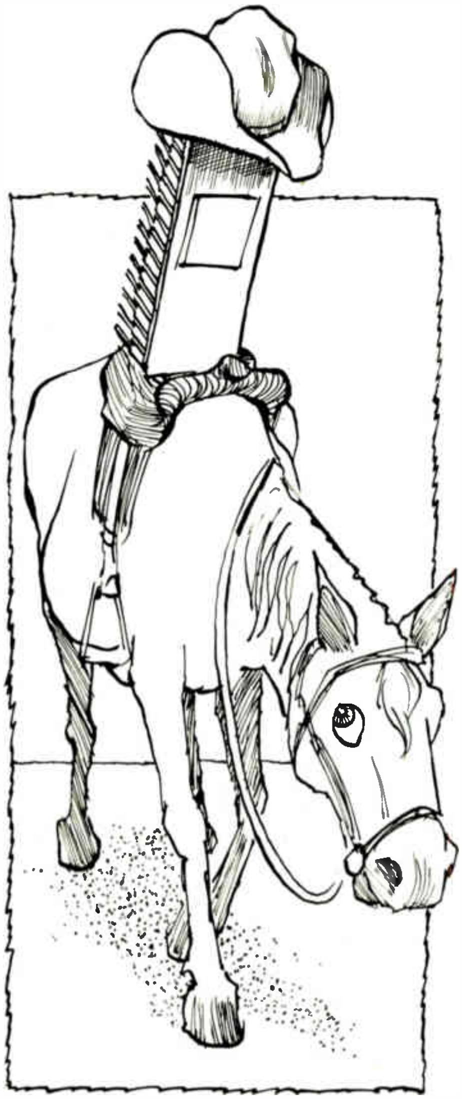
by Wesley R. Iversen, Dallas bureau manager

Nobody wants to sound like a braggart. But in Texas these days it's not hard to find engineers and managers who are willing to talk pretty tall about the Lone Star State's future as a premier electronics center during the 1980s. Not that Texas is going to overtake California's Silicon Valley in terms of sheer concentration of semiconductor companies. The "silicon prairie"—as some are beginning to call it—is much too spread out.

But the availability of land is one of the attractions that Texas touters cite. Also, labor shortages and high housing costs in Santa Clara Country have taken some of the glow off California. Bay Area firms, when they expand, are beginning to seek out other locales. Computer makers and other electronics manufacturers, too, are beginning to spread out geographically. With all this dispersion going on, a lot of folks figure that Texas cities such as Dallas and Austin are likely to benefit the most, given their own already growing momentum.

Texas Instruments Inc., of course, makes more semiconductor devices than anybody else in the world and runs wafer-fabrication lines in Houston, Lubbock, and Sherman, as well as at its Dallas headquarters. But there is a growing recognition here that TI is no longer the only electronic game around. According to figures supplied by the Texas Employment Commission, "electrical and electronics" companies account for the largest number of manufacturing jobs in the 11-county Dallas-Fort Worth area, employing 50,000 as of last October.

Based on the number of new firms moving in and pace of expansion by existing manufacturers, that figure looks likely to keep growing. IBM Corp. recently bought a big chunk of land, and other firms that have started operations in the area recently include Hitachi Ltd., NEC America, and Boeing Electronics Inc., a new subsidiary of Boeing Aerospace Corp. In addition to TI, Mostek Corp. also processes silicon at Carrollton and is currently bringing up its fifth wafer-fabricating line there.



Capital investment. In Austin, the state capital and another budding electronics center, with a population of about 350,000, Data General Corp. and Advanced Micro Devices Inc. are among the most recent to bring major operations to town. The city's three largest industrial employers—in order, IBM, Texas Instruments, and Motorola—plan major expansions. Motorola completed an additional 230,000-square-foot facility last year, bringing total space occupied in Austin to more than 500,000 ft², including two wafer-fabricating lines. Ground was broken recently in Austin for two more Motorola wafer-fabricating modules. And AMD—in its new 100,000-ft² Austin facility—is bringing up a wafer-fabrication line with plans to produce 16-K random-access memories initially, augmenting the current Texas position as the leading producer of high-volume MOS memory.

The growing electronics activity is making Texas much more attractive to career-conscious engineers. "It's just so easy to talk to people now about moving in this direction," beams one TI recruiter. "We get a lot of comments about the quality of homes and the amount of floor space for the dollar. And best of all, we're still viewed as having a work ethic here that's very desirable. People want to come to Texas to raise their families." □

This is the first in a continuing series of reports from *Electronics* bureaus relaying the talk of the electronics industries in their regions.

Computers

1980 could be year of the consumer

Personal computers for the home expected to quadruple sales even as industry sees some makers fall by the wayside

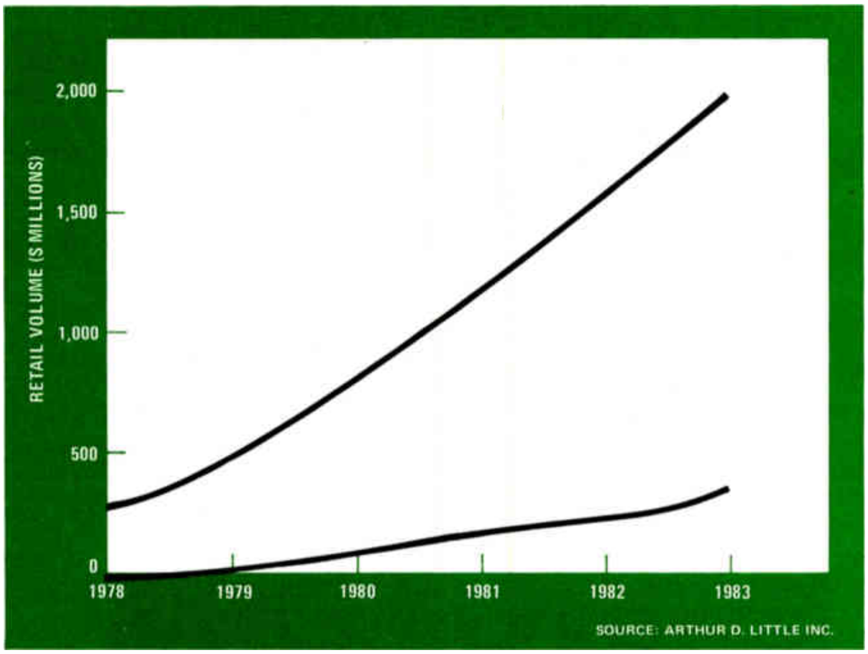
by Bruce LeBoss, San Francisco region bureau manager

The personal computer industry is less than five years old, but already it seems to be entering adolescence. With retail sales of personal computers expected almost to double this year, and the consumer segment forecast to quadruple and make 1980 the long-awaited year of the consumer, it appears that the industry has nothing but a bright future. However, while some suppliers are targeting one or more market segments to exploit, others are expected to become industry dropouts.

The picture for the personal computer industry, in particular for those serving the consumer market, was notably brightened at the Winter Consumer Electronics Show in Las Vegas earlier this month, where conferees heard projections that retail sales of personal computers will reach $950 million and 600,000 units this year, up from $500 million and 350,000 units in 1979. That forecast, made by Bill Meserve, a member of the Information Systems Group of Arthur D. Little Inc., Cambridge, Mass., further points out that the consumer segment of the market will show the most significant gains. Sales to consumers, he says, will rise from $30 million and 50,000 units last year to $120 million and 200,000 units in 1980.

Oddly, the projection is not far from the one made a year earlier for 1979 when, according to Meserve, the consumer market "did not take off, as many industry observers had predicted." What happened, he explains, were "production difficulties caused by a lack of chips. Many units were not shipped around June, when expected, but closer to the November-December time frame."

However, "the industry as a whole did well, showing a 67% increase in sales over 1978," Meserve says, "thanks to a strong showing from the other major segments—the very small-business users and the traditional technology-based segment." Spurring the overall growth last year, he adds, were several factors, including the appearance of new suppliers, among them Digital Equipment Corp., Texas Instruments Inc., and Atari Inc. Also, distribution channels expanded with the introduction of factory-owned stores, most importantly DEC's chain of stores aimed at the small-business user. Furthermore, mass retailers such as Sears, Roebuck and Co., J. C. Penney Co., and Montgomery Ward & Co. also came into the picture. That, coupled with a host of new products, prodded industry growth and laid the groundwork for 1980, says Meserve.



Upswing. This forecast shows uninterrupted growth in personal computer market, both home and small business. Consumer segment (top line) could reach $950 million in 1980.

Dropping out. Although the personal computer industry is "alive and well and continuing dynamic growth of better than 50% a year," he projects a shakeout among industry participants that is still a few months out. Last year saw some of the first casualties when firms such as Imsai, Polymorphic, and Xitan dropped out of the personal computer business for a number of reasons, one of them being the inability to make the transition from the hobbyist market to the small-business or high-technology segments. Others, such as MITS/Altair—purchased by Pertec Computer Corp., which was itself bought by a West German affiliate of Volkswagen AG—are disappearing from the market, he notes.

Those storm clouds, coupled with Meserve's projections that the industry in 1983 will be "consuming some 2 million units worth $2 billion," did not dampen the enthusiasm of personal computer suppliers at the Las Vegas show. This was particularly true of vendors to the consumer market, which the market research and consulting firm says will reach 1.3 million units worth $330 million in 1983. According to Sy Lipper, president of APF Electronics Inc., New York, "the personal computer in the home will start mushrooming this year." He cites one research organization's forecast of a $5 billion personal computer market in 1985.

But while the home market is expected to boom this year, at least one personal computer supplier, Hewlett-Packard Co.'s Corvallis (Ore.) division, is shying away from the home market. Instead, HP is targeting its new HP-85 personal computer [*Electronics*, Jan. 17, p. 46] primarily at business and technical professionals, such as engineers, scientists, accountants, and investment analysts.

Market aid. Apple's Stock Quote Reporter shows current prices, permits bid to be made, ascertains closing price, high and low price for the day, and current volume of a stock.

No place like home. But Apple Computer Inc., for example, believes "the home is potentially the greatest untapped market for personal microcomputers" and expects that "personal computers will be purchased and used in the home as commonly as TV sets, stereo systems, or microwave ovens." However, the Cupertino, Calif., firm has shipped over 25,000 of its Apple personal computers to the business, scientific, and professional marketplace, adds Steven P. Jobs, vice president of product marketing.

According to Jobs, Apple sees an opportunity to contribute in the scientific-industrial and business-professional marketplaces by making hardware and software offerings that perform, for example, word processing, general ledger, accounts payable, and accounts receivable applications. And these markets, he adds, "are gobbling up" the firm's personal computers for other than home use. Apple's apparent success has come even though the firm "just kicked off a concerted thrust in these markets last October," notes A. C. (Mike) Markkula, chairman and marketing vice president.

Also making an apparent bid for the market is Commodore Business Machines Inc., the Santa Clara, Calif., firm whose sales of Pet personal computers perhaps make it the No. 2 supplier in the field behind Radio Shack, suppliers of the TRS-80. Commodore previewed at Las Vegas a prototype of an 80-character screen system, the 8032, with 32 kilobytes of memory, that it will make available after introduction at an office products show in Atlanta in March. Also shown was a prototype of one of four disk-based systems Commodore reportedly is developing. Designated the 8050, the system is based on a Micropolis 1-megabyte disk. Both offerings "obviously are not aimed at the beginner," says Chuck Peddle, vice president for systems technology.

Looking up. Other suppliers of personal computers for the home market apparently have an eye on the business and technical professional market segments, as well. For example, Texas Instruments Inc., Dallas, which entered the personal computer field at the summer consumer show in June 1979, took the wraps off five peripherals that expand the power and capability of its TI-99/4 home computer. The additions include: a mini-floppy disk system, which includes a controller with up to three disk drives; an RS-232 interface; an acoustic modem; a speech synthesis module; and a thermal printer. Although TI's thrust is the home market, according to Rex Naden, manager of the product customer center, he expects approximately 20% of the 99/4's sales to be split between professional and small-business applications.

Atari, in Sunnyvale, Calif., also is making a move with its personal computer line into the business arena. The Warner Communications Inc. division earlier this month signed a licensing agreement with Control Data Corp. to market eight computer investment-applications programs developed by CDC. The programs, designed to help users make financial investment decisions with their Atari personal computers, include: bond yield, bond price and interest, bond switch, stock rate of return, stock dividend analysis, stock charting, mortgage analysis, and portfolio analysis.

Similar accords are anticipated as existing suppliers of personal computers look to broaden their base into other than the hobbyist market, which, says Greg. R. Leveille, director of the distributed-data-processing division of Creative Strategies International, "has pretty much plateaued and might even be on a decline." □

Electronics abroad

Italy seeks yet another solution

GNP may rise only 1.5% this year, although electronics industries will do better as computers, communications lead

by Arthur Erikson, Managing Editor, International, and Jeff Ryser, McGraw-Hill World News

No matter how precarious the economic outlook for Italy has seemed in recent years, the country has always managed to find some sort of "Italian solution," a mix of make-do, insouciance, and ingenuity that would provoke disaster anywhere else in Western Europe. Still another "solution" will be needed this year, and it is harder than ever to divine whence it might come.

As before, the ruling coalition is fragile. The minority Christian-Democratic government of Prime Minister Francesco Cossiga is hanging on mainly because neither the Communist nor the Socialist Party—each for its own reasons—wants to topple it at the moment. Meanwhile, Cossiga cannot get the legislation he needs to govern effectively through the parliament.

Inflation continues to accelerate while economic growth dwindles. After a poor 1978, Italy's Gross National Product rebounded to show a reasonable 4.3% gain last year. It now looks set to backslide to about 1.5% in 1980. Inflation by the end of the year could top 20%.

To be sure, electronics markets figure to fare better than the economy does overall—particularly in communications and computers, where pervasiveness is the goal. At first glance, the figures in *Electronics*' forecast do not look too bad. They predict equipment markets will rise 11% this year to reach $4.58 billion. However, the estimates are made at current prices and therefore must be discounted for inflation. What's more, they are based on a survey that was made last fall, before the latest round of oil-price hikes sent forecasters back to their computers to adjust their growth figures downward.

Computers. Whatever the adjustments, computers will rank as the fastest-growing electronics hardware market in 1980. The forecast: a climb of 11.8% to $1.61 billion. The heaviest push is likely to come from the lower bands of the equipment spectrum. Sizable numbers of small firms remain that still have to acquire their first data-processing hardware, and they will obviously start small. Also, many medium-sized companies are shifting to distributed processing, and that means minicomputers. Large Italian companies for the most part have what they need—large systems. The same can be said for the central administration of the Italian government. The upper bands of the market, then, figure to lag behind. As for word processing, "that is still too advanced for Italian companies," according to a market researcher at a large-computer manufacturer.

The major mainframe makers like Honeywell Information Systems Italia, IBM Italia, and Sperry-Univac will presumably keep a closer-than-usual watch this year on Ing. C. Olivetti & Cie., the country's leading office-machine maker, with headquarters at Ivrea, near Turin. For one thing, the firm plans to get back into the mainframe computer business and has set up a subsidiary, Olivetti Computer SpA, to market medium-sized and large systems bought outside—possibly from a Japanese producer.

For another, it wants to step up automation at its major plants and trim its work force in Italy by some 4,500, a move the unions are fighting

ITALIAN ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1978	1979	1980
Total assembled equipment	3,621	4,131	4,584
Consumer electronics	1,326	1,477	1,605
Communications equipment	502	575	633
Computers and related hardware	1,226	1,435	1,605
Industrial electronics	394	456	529
Medical electronics	86	95	109
Test and measurement equipment	55	60	68
Power supplies	32	33	35
Total components	737	779	824
Passive and electromechanical	349	375	393
Discrete semiconductors	87	99	111
Integrated circuits	92	107	124
Tubes	209	198	196

(Exchange rate: $1 = 830 lire)

Note: Estimates in this chart are consensus estimates of consumption of electronic equipment obtained from a survey made by *Electronics* in September and October 1979. Domestic hardware is valued at factory sales prices and imports at landed costs.

to forestall. Its success—or lack of it—at boosting productivity will give other high-technology companies a reading on what they might be able to do to lower their production costs.

Finally, Olivetti figures to be a candidate for a substantial chunk of the government's $605 million package of loans and subsidies to boost research and development in computers, telecommunications, and semiconductors [*Electronics*, Aug. 3, 1978, p. 84]. The plan, funded nearly two years ago by the parliament, is "now set to go," according to Giancarlo Lizzeri, the Ministry of Industry official who headed the special commission that drew up the plan. "All that is left to be done is for the respective companies to enter the maddening bureaucratic maze of procedures laid down by the plan," Lizzeri maintains.

Communications. Additional government largess looks likely for telecommunications producers. They had good news in mid-January from Vittorino Colombo, the minister for posts and telecommunications. He announced then that because of added income from a rise in telephone rates, the government-controlled telephone agency, Societá Italiana per l'Esercizio Telefonica PA (SIP), was preparing to spend $400 million over the next three years to upgrade the country's network.

Part of the money will go for time-division switching systems, the Proteo hardware developed by Societá Italiana Telecommunicaziono Italtel, like SIP a unit in the government's telecommunications holding company, STET. Already, some 8,000 lines of Proteo switching gear have been installed in intercity trunk exchanges. The figure is expected to bounce up to 33,000 lines by 1982 and to 200,000 lines by 1985. Meanwhile, Italtel will be striving to sell Proteo systems abroad. The most likely market is Brazil.

Although the money SIP plans to spend will not filter down this year to suppliers like Italtel (better known inside Italy as SIT-Siemens) and Telettra SpA, a subsidiary of the Italian auto maker Fiat, they can expect to hold their own, according to *Electronics*' survey. The communications sector will rise to $630 million this year, a 10.1% hike over last year's estimated $575 million. Discounted for inflationary price rises, that translates as flat.

Consumer. TV set makers are almost surely in for a poor year. Household consumption in Italy climbed some 3.8% in 1979 and this year will edge up only 1.5%, according to Bruno Brovedani, an economist for a major Italian bank. At the same time that consumers' affluence is on the wane, the market for color-TV sets is beset by a heavy inventory. Although the Olympic Games thus far triggered sales spurts in countries where color receiver saturation was low—the case for Italy at the moment—the 1980 games (if they are actually held) may not be enough.

Electronics' survey predicts color set sales of $900 million or a little better this year, up just under 8% over the 1979 level. And as goes color TV, so goes the consumer electronics business: a comparable percentage rise to $1.605 billion from the 1979 level of $1.477 billion.

Components. As for components markets, the total figures are hardly inspiring—a rise of 6.3% this year to $824 million. Passive component suppliers cannot even count on that much—the rise forecast for them is less than 5%. For tube suppliers, the heavy inventory of color-TV sets means a low-growth year and a tough market for picture-tube people. To make matters worse, Italian passive-component suppliers will not be able to offset slower sales in their home market by boosting exports, as they have in past years.

The semiconductor sector, though, is something else. According to the forecast, integrated-circuit sales will surge nearly 16% to $124 million, and discretes show a solid rise of slightly better than 12% to $111 million. SGS-ATES Componenti Elettronicci SpA, the only major Italian semiconductor house and still another company under STET's wings, figures it can repeat this year the 30% rise in sales it managed for 1979. But SGS-ATES' fortunes depend heavily on export markets—the company does only a quarter of its business in Italy. □

Fourth in a series examining European markets.

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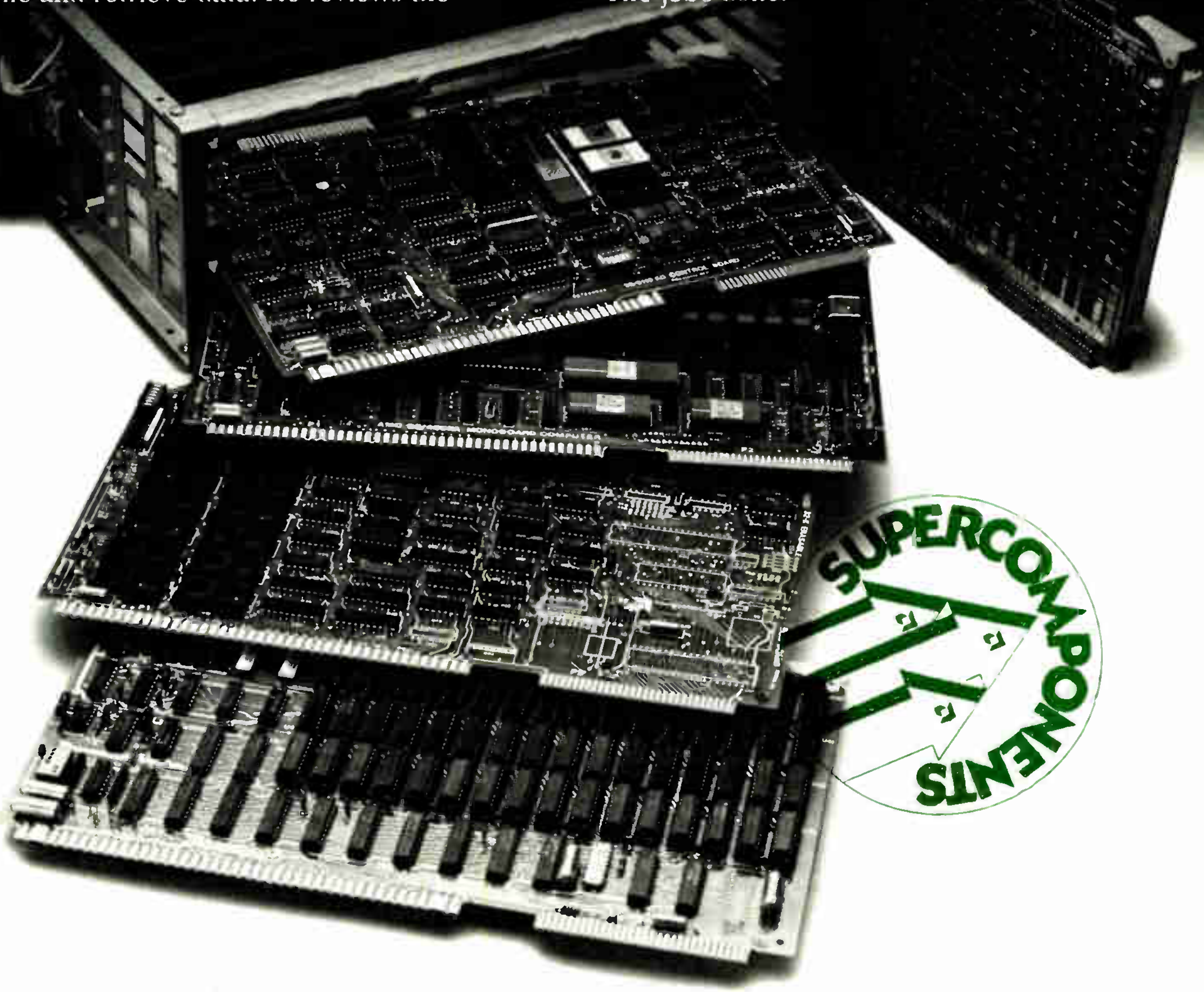

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Communications

ITT off base, say chip makers

Semiconductor marketers say telecommunications giant has ignored segments of market in calling estimates of potential overblown

by Harvey J. Hindin, Communications & Microwave Editor

International Telephone and Telegraph Co. may think that the makers of integrated circuits for the telecommunications market have overestimated its size. But the semiconductor industry is sticking to its guns, even casting some doubt on ITT's credentials as a digital expert in this area.

Most industry leaders concede that ITT's figures [*Electronics*, Jan. 3, p. 90] for the central office and private branch exchange markets are sound, although the number of lines that will be "captive" is debated. On the other hand, they feel that ITT has underestimated or ignored the market for the chips in other segments of the domestic communications market. And, they say, all aspects of the foreign market have been wrongly evaluated by the multinational telecommunications giant.

For instance, Robert W. Peters, marketing manager of the Consumer and Communications Products Group of American Microsystems Inc. in Santa Clara, Calif., says, "I generally agree with [ITT's Tim] Smith and [Wil] Riner that the immediate domestic central office market is limited." However, "they did not cover the whole somewhat more complicated story—there is a far greater market for codecs and associated pulse-code modulation components in private branch exchanges and channel banks not only in the U. S. but in Japan and Europe."

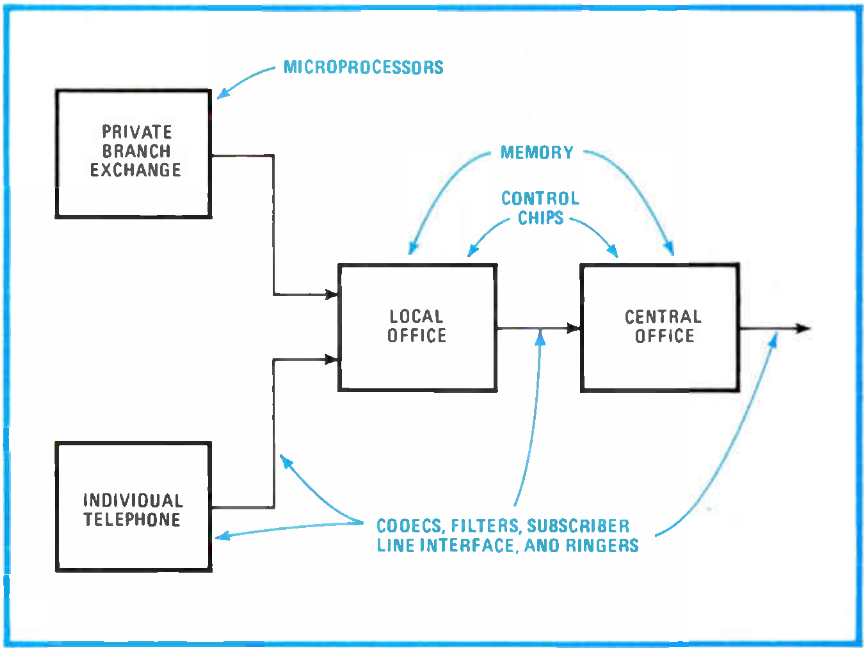
More forcefully, Tom Reynolds, industry business manager for telecommunications of National Semiconductor Corp., also in Santa Clara, believes that "the billion-dollar market quoted by the two ITT spokesmen is not that far off if you look at total semiconductor utilization and do not try to relate the figure to specific semiconductor circuits such as codecs and subscriber-line interface circuits."

Always up. The fact is that the use of chips in the transmission function, as part of the connections between switching offices, as well as in all parts of the telephone system, is constantly increasing. This is noted by the semiconductor manufacturers as a major segment of the market ignored by ITT.

Another such segment they repeatedly mention is the growth of memory and microprocessor consumption in network control and the other control functions. As Reynolds puts it: "This is massive—it is standard product and is not committed to line cards only." Thus, the chip makers evidently feel that the number of opportunities cannot be measured by the number of line interfaces or even specific components.

Even ITT's estimate of just the codec and filter market comes in for its share of criticism. Tony Livingston, telecommunications marketing manager for Intel Corp., Santa Clara, believes that ITT understates the size of that market by 1985 "by a factor of four or so."

Livingston bases his opinion on the tremendous growth expected for digital technology. Even Bell, which has been a laggard in that area, has by now started to move solidly in that direction. It will have the ESS-5—a small digital switch—ready by



Lots of chips. Both sides of the discussion about the market agree that as the network becomes more digital, and stored program control the method of choice, chip usage will rise.

the early part of this decade. It is also under tremendous pressure to introduce a digital private branch exchange in about the same time because it is losing that market to the independents. Furthermore, it has gone so far as to qualify Canada's Northern Telecom as a supplier of digital switches—at least one—for Bell's operating companies.

Chances abound. These Bell moves could mean more opportunity for the semiconductor people if Bell proves unable to supply its own needs. As Dick Pieranunzi, strategic marketing manager for telecommunications of Motorola Inc.'s Semiconductor Products Group in Phoenix, puts it, "It will be somewhat like the shortage of memory right now in the automotive market and IBM going more and more to the outside marketplace." He also adds, "Western Electric does not have offshore facilities to bring the cost of its chips down. So you have to ask if the telephone companies will want some outside supply for the components they will be using. I think they will, and while the total market won't be in the billion-dollar range it may well triple or quadruple within the next five years."

This sentiment is echoed by Frank Schneider, vice president and general manager of the Automotive and Telecommunications division of Signetics Corp. in Sunnyvale, Calif., who says, "The demand is going up very fast and Bell and ITT will not be able to keep up with it. It will be like what happened to the IBM market. I get the impression that ITT's figures are only extensions of past trends rather than estimates of what will really happen."

Late start. Some semiconductor marketing people also argue that as ITT didn't address the digital switch market until late in the game, it may not have the best view of where the industry is going. It certainly cannot be considered to be an innovator in the digital communications market, whereas Northern Telecom is consistently singled out by the chip marketers as the industry leader. The Canadian company is called an aggressive manufacturer and the epitome of how growth can come from early innovation in the use of digital telecommunications.

The ITT forecasters are called to task also for their estimates of the foreign market. As for the U.S. market, however, specific opposing figures were hard to come by. National's Tom Reynolds puts it this way: "The fact that only 30% of the phone market is taken up in France is a positive rather than a negative factor. This can make a major contribution to future industry growth." He believes that none of the industrialized countries can afford to leave a gap between itself and the others, and he deduces that the telecommunications market, insofar as the central office line interface is concerned, is therefore greater outside the U.S. than within.

As for ITT's claim that it is difficult, if not impossible, to sell to foreign telephone companies, it is worth noting that many U.S. semiconductor companies have cross-licensing agreements with foreign companies to help them gain access to those markets. Motorola's Pieranunzi asserts, too, that "if the product is right, they will buy. They buy memories they need to be competitive on a worldwide basis, and if they see they will end up behind in the telecommunications market if they don't, they'll buy more memories."

Moreover, Pieranunzi adds, countries like France and West Germany are very concerned with their balance of payments. "They cannot export a low-labor product. Nor can they ship raw materials like oil. The only thing left is high technology, and a major factor here is telecommunications. The recent major contract for them to redo Egypt's telephones bears this out."

One last point that drew fire: ITT said the chips on a line-interface card cost $12, but the industry consensus is that up to $20 is more likely for the present.

If there is unanimous agreement between ITT and the semiconductor makers about anything, it is regarding the need for the chip suppliers to equip themselves with personnel who know telecommunications, the difficulty in obtaining specifications for systems, and the need for special hardware and software for design and testing. However, no one views any of those as insurmountable problems. □

VAX Virtual Memory. Ask any user.

"We were looking for large program capacity. And VAX ran circles around the competition."

Skip Little,
Supervisor of Systems Analysis and Systems Programming,
VAX Computer Group,
Woods Hole Oceanographic Institution,
Woods Hole, Massachusetts

Scientists at the Woods Hole Oceanographic Institution gather massive amounts of data about the earth's oceans. But until recently the only way they could analyze much of that data was by sending magtapes to and from a giant Cray 1 computer located 1800 miles away.

So the Institution decided to buy its own VAX from Digital.

Here's what Skip Little, Supervisor of Woods Hole's VAX Computer Group, has to say about VAX program capacity: "Some of the smaller versions of Cray modelling programs can actually be run on VAX. That's remarkable because the Cray 1 computer is the world's most powerful commercially-available system."

Now the problems they had in doing large data analysis and timesharing simultaneously are a thing of the past. Says Little, "We're able to lock our biggest jobs — like synthetic seismogram generation and fluid dynamical modelling — into VAX's main memory, while other timesharing users can be handled by the virtual memory system."

And Little has found that program conversion is a breeze: "We've converted programs from practically every kind of computer you can imagine with great ease."

"With VAX's virtual memory, there isn't a PC board around that's too large for LASAR to handle."

Fred Grant,
LASAR Product Manager,
Teradyne, Inc.,
Boston, Massachusetts

"Without Digital's VAX, our specialized design work just wouldn't be as cost effective."

Stephen Tritter, Senior Principal Engineer,
Engineering Computer Facilities,
E-Systems, Inc., ECI-Division
St. Petersburg, Florida

Teradyne, Inc. makes a wide range of automatic test equipment including computer-based systems for testing printed circuit boards. To help their customers program the most complex of these PC board test systems, Teradyne developed a sophisticated software package called LASAR.™

But until Teradyne looked at Digital's VAX-11/780, LASAR was only available to customers through a timesharing service on a large batch-oriented mainframe. The software package was just too big for anything less.

Now with LASAR running on VAX, Teradyne will have the program capacity they need, in a system their customers can afford to purchase.

"When you reach the limit of main memory, VAX automatically puts the program into virtual memory," Grant says. "That's a key factor in our LASAR development work. Test programmers can develop more complete programs without being limited by memory size."

Has Teradyne sacrificed performance by switching from the mainframe?

"Definitely not," says Grant. "In our benchmarks, VAX matched up one-to-one with the mainframe. That really impressed us."

And VAX's interactive capability should be a big plus for Teradyne's customers: "Several people can program on VAX simultaneously, and they can monitor the progress of their programs as they work.

"There's more programmer involvement with VAX, and more efficiency too."

The ECI Division of E-Systems, Inc., designs high-technology electronics and communications equipment for the U.S. Government. And that requires huge computer programming space.

So virtual memory capability was an important factor in the E-System decision to buy a VAX.

"We're doing a lot of work now that we couldn't have done without Digital's VAX," says Steve Tritter, Senior Principal Engineer.

"For example, we use the VAX to help us design our own LSI integrated circuit chips. That means keeping track of thousands of points, each with several different characteristics. It's a big job.

"And while that analysis is running, other people are performing high-frequency radio propagation studies using as many as 210,000 memory locations, or running Fast Fourier Transforms with up to 8,000 points."

Tritter says that ECI regularly has 10 to 12 engineers working interactively on VAX at a given time.

"We're very happy with VAX system performance," he adds. "We expect to add more memory, and eventually service 50 to 60 simultaneous users."

Digital's VAX-11/780, with its 4 billion bytes of virtual memory, has set a new standard for program capacity. This means you can run large programs easily on VAX, with a potential for growth that's unmatched in the industry.

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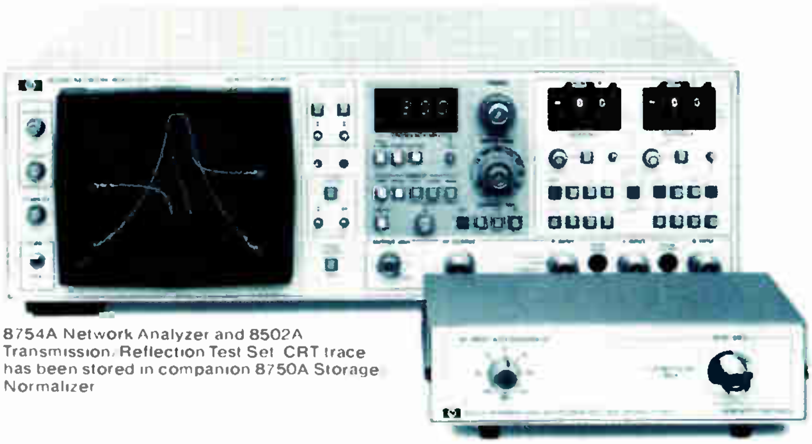

8754A Network Analyzer and 8502A Transmission/Reflection Test Set. CRT trace has been stored in companion 8750A Storage Normalizer

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Add the 8750A and you can automatically remove system frequency response variations also make comparison measurements easily. Digital storage permits flicker-free displays even for measurements requiring slow sweep rates.

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HEWLETT PACKARD

Development system supports today's processors—and tomorrow's

Present hardware modules and software tools emulate 68000; future enhancements will include a multi-user operating system

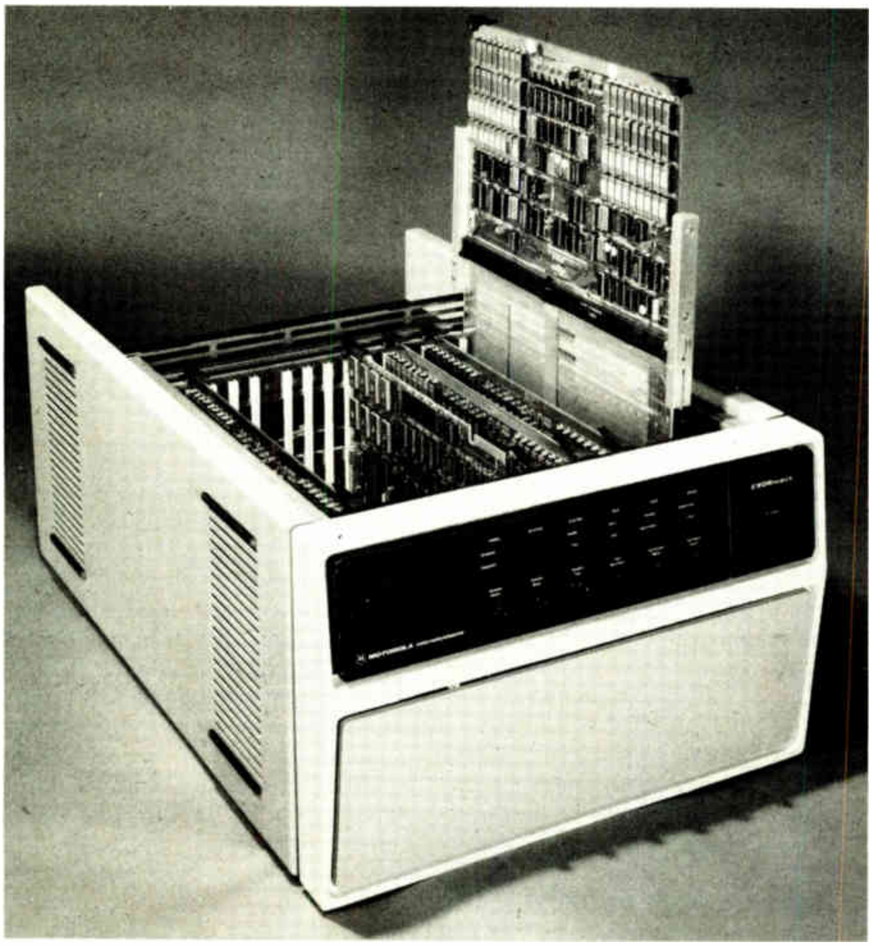
by Jack Kister and Irwin Robinson,* *Motorola Inc., Semiconductor Group, Phoenix, Ariz.*

☐ The EXORmacs development system is intended to aid in the design of systems based on the MC68000 16-bit microprocessor. But it is also compatible with previous development tools and microprocessors and, more importantly, is designed to support future processor chips.

In readiness for those yet unannounced devices, EXORmacs incorporates a new, 5-megahertz bus structure called VERSAbus that 32 address and 32 data lines (see "A 32-bit bus system," p. 82). On this bus reside the modules that constitute the system hardware. Besides the 68000, the central-processing-unit board contains memory management logic to smooth software development. A bus arbiter module allows multiple processors to share the system bus. Portions of these and other modules will be integrated into dedicated peripheral chips at a later date in order to further boost system performance.

The system is loaded with new software, too, including a real-time, multitasking operating system, a resident Pascal compiler, and a macro-assembler. A secondary memory map optionally provides unrestricted use of the

*Now with Graphtek Inc., Phoenix, Ariz.



1. Thinking ahead. The EXORmacs development system is designed to support the 16-bit 68000 microprocessor, but its 32-bit address bus and 32-bit data bus are intended for future versions of this and other microprocessors. The system incorporates memory management and bus arbitration logic for multiprocessing and, later this year, multiple users. The hardware and software self-test their own integrity.

A 32-bit bus system

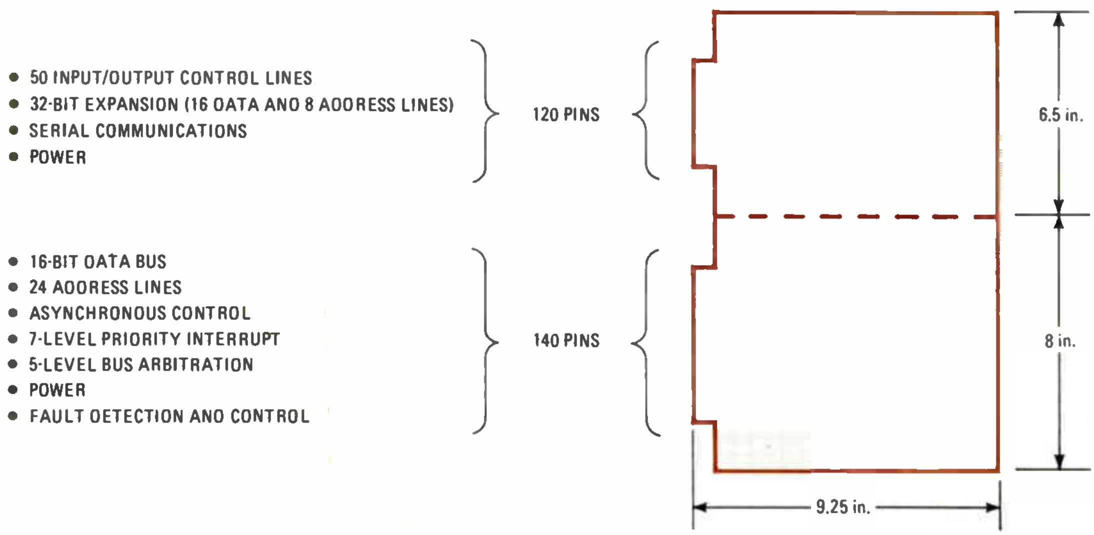
VERSAbus is designed to serve as a comprehensive foundation for 8-bit to 32-bit microprocessor architectures having 5-megahertz data transfer rates. It is specifically intended to serve industrial control, communications, and general-purpose business applications and to allow for system architectures involving multiple processors. A final objective of VERSAbus is to exploit to the fullest the latest computer and semiconductor technologies but without sacrificing ease of use.

To satisfy these objectives, the following features are provided by VERSAbus:

- ☐ A very fast bus cycle time.
- ☐ Asynchronous, bidirectional operation.
- ☐ 8-, 16-, or 32-bit data transfers, with single-byte designation possible in 16- and 32-bit data transfers.
- ☐ 32 address lines for direct access to 4 billion words of memory.
- ☐ Direct memory access and multiprocessor support.
- ☐ Seven-level priority interrupt control.
- ☐ Five-level daisy-chained bus arbitration.
- ☐ Up to 50 peripheral input/output lines with mating ground returns.
- ☐ Standard +5-V and +12-V power for logic as well as +15 V for process control and standby power support.
- ☐ Serial communications.
- ☐ Distinct I/O mapping.
- ☐ Bus error and retry signals.
- ☐ Separate analog ground.

To accommodate the signal lines required for these features, VERSAbus uses 260 pins in two connectors, as shown in the diagram. Why should a microprocessor bus be so large? First, as densities increase in semiconductor devices, greater amounts of memory and peripherals will be controlled from a microprocessor and wider data widths will be required.

Secondly, since one of the goals of VERSAbus is to provide a comprehensive basis for future microprocessor systems, it must be capable of supporting the largest envisioned applications and single-board designs. Because of the two distinct connectors, systems may be designed using board sizes of 8 inches wide by 9.25 inches high. Such small-sized boards may be plugged into full-width systems for development purposes, or they could serve as a more economical means of providing functions that do not occupy the full-sized module. Entire 16-bit, 16-megabyte systems with full priority interrupt and bus arbitration could in fact be implemented on the half-sized boards.



68000's supervisor and user modes. Moreover, to enhance the reliability of the system, a complete self-test is executed at powerup and the operating system incorporates diagnostic routines. Later this year, the operating system will be upgraded and an intelligent communications controller and hard disk unit will be added to support multiple users.

A good start

EXORmacs represents phase three of the 68000 support that began (before the 68000 chips) with a cross assembler and cross simulator in 1978. The second phase started with the introduction of the 68000 device and the 68000 design module [*Electronics*, Oct. 11, p. 118].

The introductory EXORmacs system consists of a 68000 microprocessor–memory management unit (MPU-MMU) module, debug module, 128-kilobyte dynamic random-access memory module, 32-kilobyte static RAM module, floppy-disk interface module, and 68000 user system emulator (USE) module (Fig. 1).

The central intelligence of EXORmacs is provided by the 68000 MPU-MMU module that, besides the 68000, also contains a four-segment memory management unit and diagnostic firmware. The memory management unit allocates memory for tasks and allows the multitasking operating system to protect user programs. The real-time multitasking operating system speeds program development by allowing tasks to be run concurrently. For example, an assembly requires the printer but leaves the display console free for editing other modules.

Designed to help the operating system execute concurrent tasks, the floppy-disk controller is itself driven by an

MC6801 microcomputer. The operating system need only request sectors of information from the controller, and the 6801 will initiate a transfer, set up the direct memory access controller, and provide error correction. This distributed processing increases performance and makes possible a standard input/output interface that allows substitution of different types of storage devices without software modifications.

Both the static and dynamic RAM modules increase system performance by offering byte parity generation and detection within a 500-nanosecond read cycle. The boards can request re-execution of a bus cycle to correct soft errors or terminate bus cycles if hard errors occur.

For development on time-shared software systems, EXORmacs provides two RS-232 serial ports. One would be connected to the user's cathode-ray-tube terminal, the other to the time-shared computer. The resident firmware, MACSbug 2.0, provides a transparent mode whereby the terminal is connected directly to the time-shared system for program development. Then, a down-load command may be used to transfer the program into EXORmacs for execution.

Supervisor and user maps

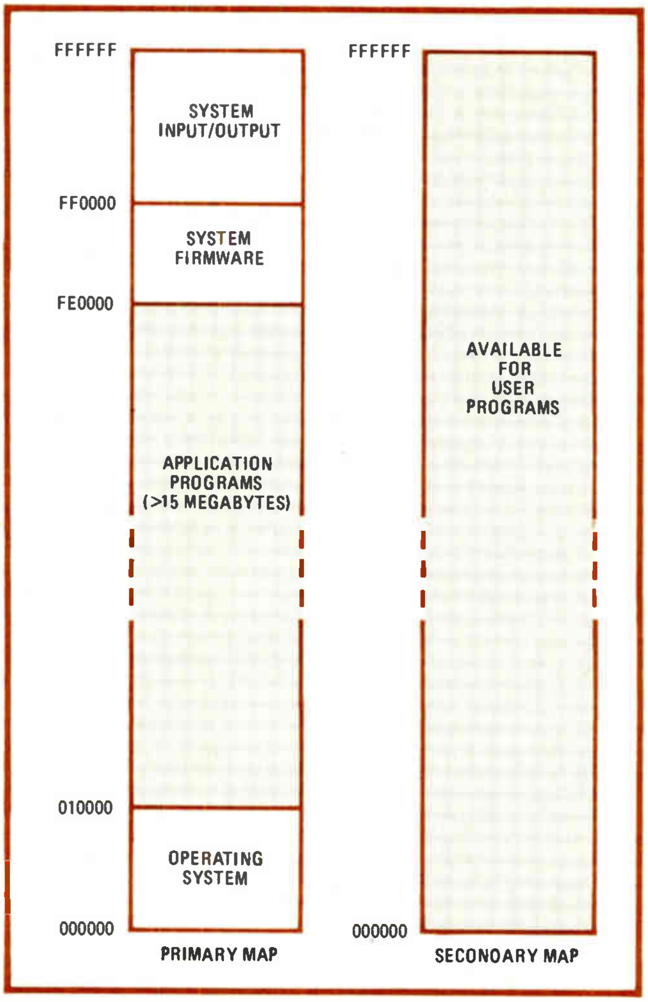
EXORmacs overcomes some unusual problems. At first glance, it would seem that the 16-megabyte address space of the 68000 processor would be more than adequate for a development tool; however, it was found necessary to expand the address space of the system. This requirement can be understood by examining the 68000. Within the processor there are two modes of operation: supervisor and user. In the supervisor mode, programs may perform any operation without restriction, whereas in the user mode certain privileged instructions are off limits. In a typical 68000 computer application, the operating system executes in the supervisor mode and the user's applications programs execute in the user mode.

Paradoxically, EXORmacs cannot always restrict users to executing in the user mode. A good example is a designer who wishes to develop a general-purpose computer. As such, the system should use the supervisor mode for executive routines and I/O handlers, plus the user mode for application programs.

In designing such a system it is often necessary to test the system at real-time speeds. This is especially important for interrupt handlers and I/O routines. In order to provide the user with a development system and yet still give unrestricted use of the 68000 processor, it was necessary to duplicate the entire address space of the processor (Fig. 2).

Users wishing to execute code without restriction at full processor speed are assigned to a secondary memory map. System software resides in the primary map, completely separated from the user's programs. The transfer of control from the secondary map is performed by the execution of an "illegal" instruction. When this occurs, the EXORmacs operating system is awakened from its dormant state to service the user's program.

Not all the software on the EXORmacs development system needs to use the primary and secondary map scheme for program management, however. Assemblers, compilers, and editors, as well as many user programs, may not need the special environment of the secondary map. Such programs execute in the primary map, using the facilities of the operating system to manage interrupts, task swapping, and I/O.



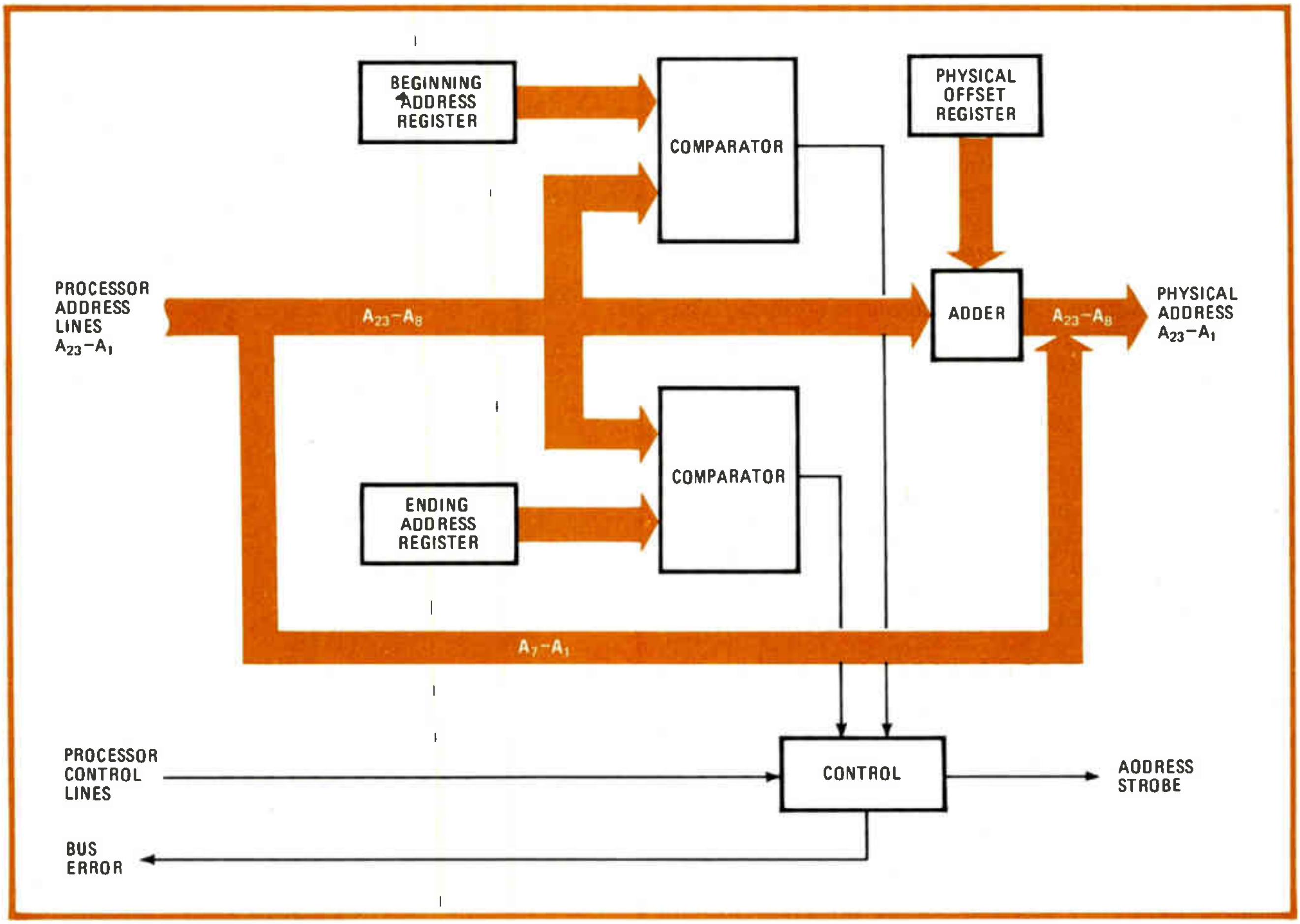
2. Two maps. In EXORmacs the entire 16-megabyte address space has been duplicated. This allows the user to perform real-time emulations while continuing to provide complete support for the operating system, which uses part of the primary map on the left.

In the primary map it is necessary to protect the operating system from software failures that naturally occur in a development system environment. A common error of this type might stem from an incorrect last address, such as too large or too small an array subscript. This can accidentally change operating system code or device tables or even cause a device to perform an unwanted function.

Memory management

In EXORmacs the operating system is protected by the memory management unit. This arrangement is not used like the memory management units of minicomputers to expand the amount of available memory; rather, its purpose is to enhance the usefulness of memory and to ease the creation and execution of programs.

In addition to protecting the operating system from inadvertent tampering, the unit also relocates programs



3. Managing. With each memory management scheme, the upper 16 address lines are compared with each segment's beginning and ending address register. If between the two, the physical address is generated by adding the processor's address to the physical offset register.

automatically, translating memory accesses from a logical or program address into a physical or hardware address. The physical address may be located at a completely different place in memory from the one the logical address would imply. By translating the addresses of user programs, the operating system and protected I/O can be removed completely from the address map seen by the user. Any attempt to read or write memory outside of the user's assigned address space causes the processor to abort the user's program.

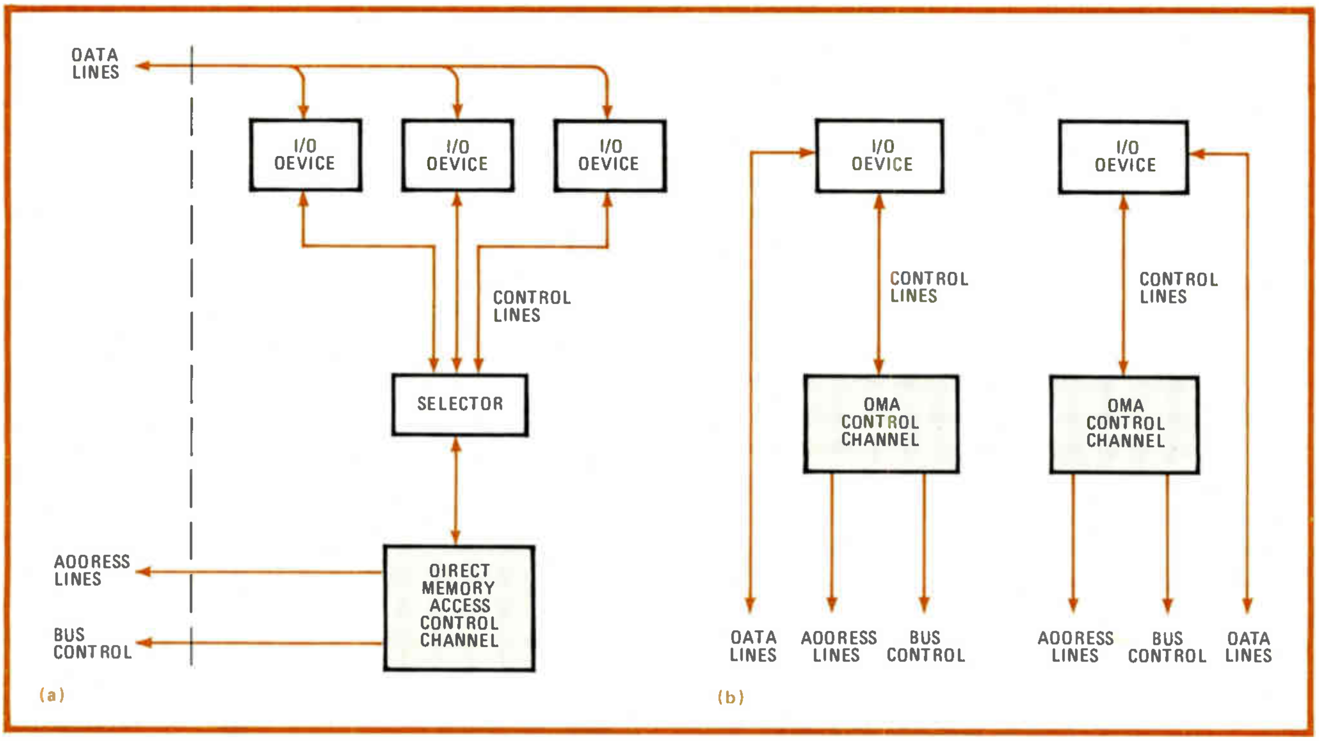
Through this address translation process the unit provides another very important function. Since the physical location of a user's program in memory is not related to the program's internal addresses, all user programs may be located anywhere in physical memory, regardless of their origin. This enables the operating system to utilize all the memory without the need to relocate programs as they are loaded. That is, tasks that execute under control of the operating system may be moved or placed anywhere there is space available.

The EXORmacs memory management unit has four physical segments, each of which may represent up to 65,536 pages of 256 bytes. These segments each contain a beginning and an ending address register, a physical offset register, and a control register (Fig. 3). When a program executing in the user mode performs a memory access, the address generated by the processor is compared to the beginning and ending address of each segment. If the processor's address falls between the beginning and ending address registers, the address is added to the physical offset register using 2's complement arithmetic. The resulting sum serves as the physical bus address.

Within the control register, segments may be designated read-only or disabled. Any attempt to write to a protected segment or to select simultaneously two or more segments flags a bus error and terminates the cycle. However, memory accesses that are performed in the supervisor mode bypass the memory management unit; processor addresses are put directly on the bus without translation.

Both DMA types

As the creation of a memory system is complicated by the need for a versatile development tool, so also is the process of performing DMA transfers. As shown in Fig. 4, there are two basic methods for providing DMA in a system: centralized and distributed. A centralized or pooled DMA system uses one or more DMA controllers as a common resource for many devices. When a device needs to transfer data, a DMA controller is assigned through software to the device. Upon completion of the transfer, the DMA controller is freed and returned to the central pool.



4. Both. Rather than choose one type of direct memory access to support, the system supports both. In the centralized scheme (a), one channel may perform I/O for several devices. With distributed DMA in (b), a channel is dedicated to each device.

In a distributed DMA system, controllers are permanently assigned to devices. With single-chip DMA controllers the distributed approach has gained popularity because of its simplicity. However, the centralized DMA scheme is still quite commonly used. Within the EXORmacs system, DMA controllers may be centralized on one board or distributed. A set of control lines, designated by the user, may be used to communicate to a centralized DMA controller.

Closely associated with DMA control is the topic of multiprocessor systems. To provide for the creation of a multiprocessor system within EXORmacs, it was necessary to make a fast and powerful bus arbitration scheme available. In designing the bus it was concluded that memory transfers are best accomplished in blocks to avoid the excessive overhead in arbitrating for each cycle. To complement this philosophy, a simple arbitration scheme using bus requests and chained bus grants is employed, similar to that found in the 68000 processor.

Arbitration

Arbitration is performed on a highest-priority basis, unlike many schemes that use a first-request algorithm. That is done by delaying the issuance of a bus grant until the last cycle of the current bus master. In this way devices of the highest priority are serviced before devices of lower priority, regardless of which device first requested the bus. Individual devices may also dynamically increase their priority by asserting higher-priority bus requests if the occasion arises, as in the case of a pending data-late error on a disk drive. The arbiter generates a signal called bus clear to inform devices on the bus that a higher-priority device needs servicing.

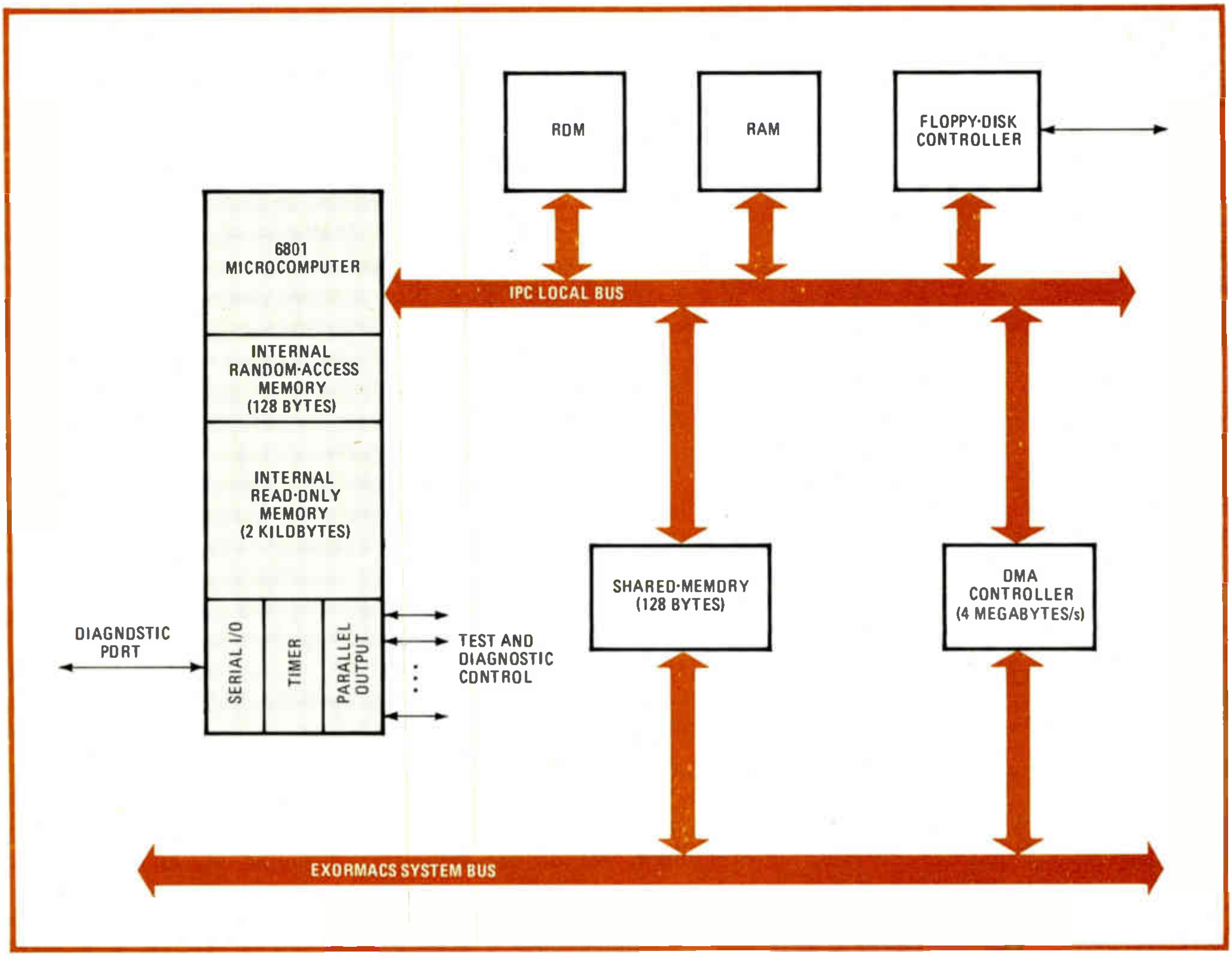
Because a development system is used to test unproved hardware, it is sometimes necessary to interrupt the system and regain control. Even in a nondevelopment environment, certain events, such as a power failure, can require the immediate attention of the system. To provide for such necessities, another line—bus release—is asserted by a device to command all bus masters to relinquish the bus and turn over control to the host processor. That allows the host processor to service pending interrupts regardless of the priorities of other pending bus masters.

State of suspense

Another important attribute of a multiprocessor system is the ability to suspend the state of all the tasks being executed. Through a system-pause line, the system may be single-stepped at a process level. When the processors in the system—whether they be emulators or user-designed hardware or both—recognize the system pause line, they suspend their current processes and release a line called system-pause acknowledge. When all the processors have released the acknowledge line, the system pauses and can be examined.

To provide for testability, the system has been designed to perform a complete self test. Upon powerup the processor, bus, memory, and I/O channels are functionally tested and their status displayed on the front panel. In the event of an error, a status condition is shown on the front panel and the processor is forced into a diagnostic monitor for the user or field-service personnel. If the processor board or an I/O channel fails the test, a lamp is lit on the faulty board.

The I/O driver boards, called intelligent peripheral controllers (IPCs), utilize an on-board 6801 microcomputer for test and diagnostics (Fig. 5). By choosing a



5. Smart I/O. EXORmacs I/O is controlled by intelligent peripheral controllers, or IPCs. On-board 6801 microcomputers process the commands found in 128 bytes of shared memory. Data is transferred directly into main memory through a 4-megabyte/s DMA channel.

microcomputer with complete internal read-only and random-access memory and input/output, the ability to diagnose faults is retained with a minimum of parts.

Besides the power-up functional test, the IPC is capable of device-level fault isolation. This function is provided through the serial and parallel I/O ports of the 6801 microcomputer. Through the serial port, service personnel may attach a terminal and interface to a simple monitor through which memory may be examined and changed, programs executed, and breakpoints set. The monitor also provides an interface to internal signature analysis routines. The parallel I/O ports of the processor are used for factory testing as well as in the signature analysis routines.

Advanced software

To complement the hardware of EXORmacs, a totally new and advanced software system has been designed. This system includes the real-time, multitasking operating system and a macro-assembler, a Pascal compiler, and complete set of editors and debuggers. The package is supported by both floppy-disk–based software and resident firmware. The operating system and supporting software are designed to allow expansion to a multi-user, hard-disk configuration, to be available later this year.

The macro-assembler and Pascal compiler generate efficient and cost-effective code for the 68000. The macro-assembler allows conditional assembly, complex expressions, and position-independent code generation. Pascal for the 68000 is a superset of the currently proposed standard. Calls to executive directives, I/O routines, and assembly language routines ease its use in EXORmacs. Pascal for the 68000 also supports absolute addressing and interrupt handling. Finally, a set of cross software, including the macro-assembler, Pascal compiler, and a 68000 simulator, is available for the IBM 370, PDP-11, and 6800 EXORcisor.

The heart of the EXORmacs software is the multitasking operating system. This system is designed to support sophisticated multiple-task systems through resource sharing, intertask control, and communications. Users may interface to the facilities of the operating system interactively, as with batch jobs or with programs using executive directives. The file and I/O system of EXORmacs can be controlled through simple device-independent commands. EXORmacs also provides the ability to communicate to a remote computer for off-line program creation and downloading.

The operating system uses a layered approach that allows the software to be modular and easily expandable. A foundation, or kernel, contains the basic executive and a set of executive extensions. This is surrounded by the I/O management system, the user-session management system, and complete set of user interfaces that provide for intertask communication and scheduling. The net effect is somewhat like a target, with the executive forming the bull's eye and with the user tasks occupying the outermost ring.

The executive is the smallest unit of the operating system and is designed to be completely self-sufficient. Within the executive is a task controller, an intertask communication facility, a memory management facility, and an initialization section. The executive also has the ability to load the remainder of the operating system. This feature allows the basic executive to act as a foundation for extended functions that are added later.

The majority of the executive is called the task management system. This system is responsible for coordinating the scheduling of tasks and allocating memory. In a real-time multitasking executive, provisions must be made for intertask communication and dynamic task scheduling. These facilities are provided through the use of semaphore flags, asynchronous service queues, and shared memory segments. Any task within the system has the ability to affect the status of any other task through the use of executive directives. These directives can pass information, create tasks, suspend executing tasks, and so on. Tasks may also be affected by interrupts, traps, and scheduled events.

In addition to task management, the executive is also capable of dispatching interrupts and traps to the executive's simulators for floating-point operations and strings as well as for special service routines. The operating system's I/O management system is also attached to the dispatcher.

I/O management

The next level above the executive and its extensions is the I/O management package. Its routines execute as a system task to process all I/O requests. When a task operating in the system wishes to perform an I/O function, the executive queues the I/O request for execution by an I/O management task. This task then verifies the request and directs the appropriate intelligent peripheral controller, or data control, to perform whatever has been requested. Upon completion of the I/O transfer, the requesting task is resumed.

The I/O management system also automatically spools output files. When the file is completed it is then despooled from the disk and printed. This procedure allows several tasks to share the printer without unnecessarily delaying a task.

The outermost level of the operating system is the user session management system. It interfaces a terminal user to the operating system. Through the user session management system the user may initialize multiple, concurrent batch processors yet remain in an interactive mode, editing, compiling, or executing a user program. Each terminal may have the complete set of facilities normally associated with a system console. Users may be identified as privileged or restricted according to their identification code.

To debug and maintain the EXORmacs operating system, a special set of diagnostic routines has been built in. These routines provide for on-line error detection and status indication. Errors within the executive hardware or software are detected through the use of checksums and entry flags. Before the operating system enters a routine, a status indicator is set on the EXORmacs front panel. If an error is detected or if the processor halts due to a failure, the status can aid in diagnosing the problem.

To aid in the development of dedicated microprocessor products, the kind that contain just enough performance to satisfy the requirements of the system, EXORmacs provides a series of pre-built development modules. These contain I/O devices such as parallel interface adapters, serial communication adapters, timers, and universal adapter modules. All come with a VERSAbus interface and Wire-wrap space that allows the board to be easily customized. In addition, an interface module is available that adapts EXORcisor development system modules and micromodules to the VERSAbus. This permits immediate availability of many additional peripheral boards such as relay drivers, analog-to-digital and d-a converters, arithmetic modules, and so on.

EXORmacs of the future

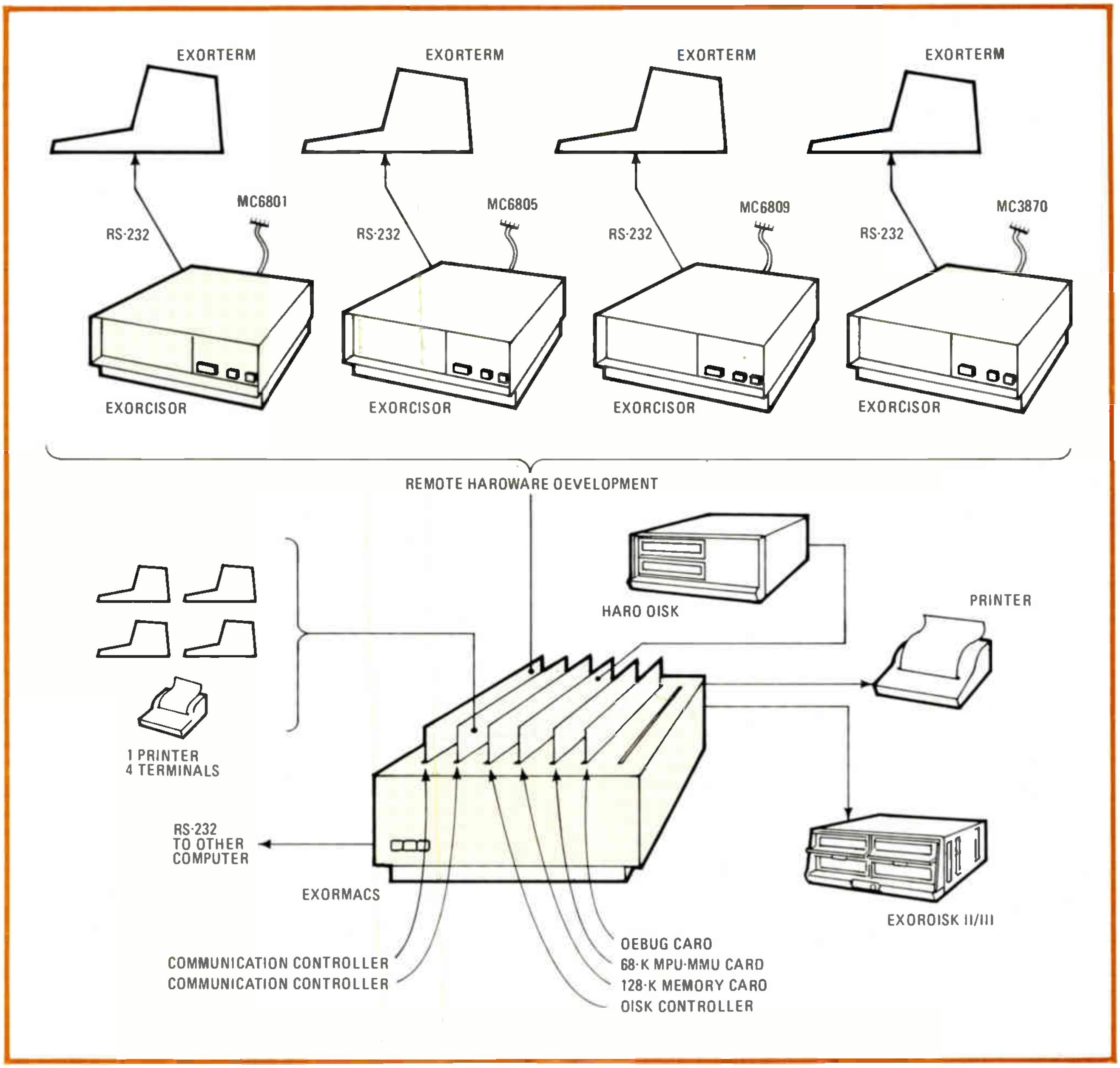
Phase four of the 68000 support is the multi-user EXORmacs, now in development to be introduced this summer. The multi-user system will consist of the basic EXORmacs plus an intelligent serial communications controller, an intelligent hard-disk controller, and up to 1 megabyte of memory.

When introduced, the multi-user operating system will support eight users. It utilizes the memory management features of the hardware as well as software interlocks in order to prevent unplanned interaction between the individual users.

Each task is uniquely identified to the executive by a combination of session number and task name or ID. A task or a group of related tasks that communicate do so under a session number. A program with a task name may be concurrently executing under multiple sessions; for instance, an assembler might be concurrently operating for several users.

Session number assignment can be used to facilitate intertask communication or to provide security against it. Multiple tasks executing with the same session number need not know the session number; only the task name is required to communicate. For tasks with different session numbers to communicate, the task name, as well as the called task session number, must be known. Session No. 0 has a unique property in that it can communicate with any session number, but it is protected from communication from any and all other tasks. Thus, an on-line, real-time control may be totally protected from software development.

Software is developed under the multi-user system by creating a session control task for each user after a request for service is initiated at a terminal. A new session number is generated for each user to uniquely



6. To come. EXORmacs is not just some temporary solution for the development of the 68000. Phase 4 of the project is the multi-user system, which will feature a hard-disk controller and an intelligent serial controller that will link up several other development stations.

identify the concurrent usage of the software development and utility program (tasks) supplied. The session control task acts as a monitor during the session and until the session is terminated by the user by invoking a LOGOFF command. Another function of the session control task is to request commands, decode them, create a task for the execution of the requested program, initiate the execution, and take over when the requested program aborts or terminates.

The multi-user file system provides protection and isolation for files associated with a given user. Normally, all files are considered private and may not be accessed by anyone other than the owner of the file. An optional file password may be used to make a file available to other users equipped with the password, or a file may be marked as public to allow unrestricted read access to it.

Figure 6 depicts multi-user EXORmacs in use as a central software development system with additional EXORcisors (or EXORmacs systems) being used for hardware development. The separate development chassis provides each user with a dedicated bus and full control of his system and the resources of the host system. Each remote chassis can support a parallel development activity on any of the wide range of microprocessors.

EXORmacs will complement the existing family of support hardware by extending its range into the high end of the performance market. Many new VLSI chips will be introduced in the 1980s and EXORmacs will support these advanced chips both before and after their introduction. Additional advanced tools to aid the designer in developing multiprocessing systems will also be introduced in the future. □

Package piggybacks standard E-PROM to emulate one-chip microcomputer

24-pin socket on processor's back accommodates 2716 or 2732 E-PROMs, replaces external pc boards for better emulation of 3870 family

by Steve Gerson, *Mostek Corp., Carrollton, Texas*

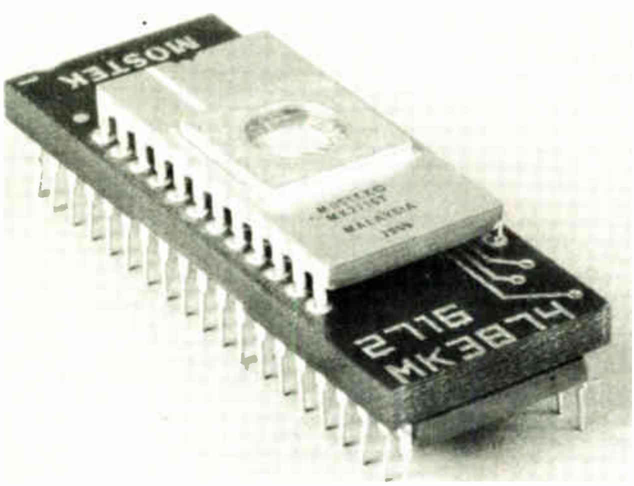
□ "Why didn't I think of that myself?" is a question engineers often ask themselves when they see a particularly neat and simple solution to a problem. The problem for Mostek's integrated-circuit designers was emulating a one-chip microcomputer. Using all existing components—a standard socket, substrate, and small printed-circuit board—they came up with an emulator (Fig. 1) that is a 40-pin IC with an integral on-board 26-pin socket allowing a standard family of ultraviolet-erasable read-only memories to be plugged in.

In traditional methods, program storage, which in the final microcomputer design is to be on chip in ROM, must be emulated off chip on a circuit board as either random-access memory or ROM plus extra circuitry. In the new compact design, the 40-pin IC is replaced by the actual single-chip microcomputer with a masked on-chip ROM by simply plugging the microcomputer into the emulator's position on the system pc board. The result, trademarked the MK 3874 P-PROM emulator, is especially designed for its MK 3870, a single-chip 8-bit microcomputer.

Before the new dual-in-line-package-sized emulator appeared, three methods of microcomputer emulation were in general use, each with weaknesses. One method involves building a microprocessor system from a compatible multichip family, if one exists. Emulation of the MK 3870 was usually done in this manner. There are, however, some difficulties with this approach. Although the software can be fully verified, some characteristics of the emulated processor cannot be exactly simulated with the multichip configuration. Also, the physical size and power requirement differences between the emulator board with its collection of DIPs and the final single 40-pin DIP severely restrict field prototyping of the final design.

A second general approach is used for single-chip microcomputers that add memory with off-chip addressing capability. On these circuits, pins used in the final design as input/output ports have address, data, and control functions during emulation. This presents the new problem of having to add circuitry on an emulator board to replace those I/O pins lost as a result of the memory expansion. As in the previous case, the final emulation product consists of a pc card that is awkward for field use in low-volume applications.

A third approach combines the microcomputer and the E-PROM on the same chip—an example is the 8748 E-PROM version of Intel's 8048 one-chip microcomputer. This solves problems caused by increased size and power requirements, but it creates new ones. Specialized PROM



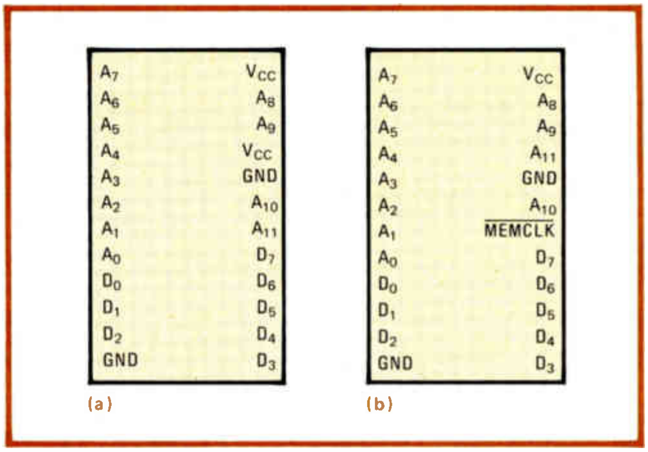
1. Double-DIP. Mostek's MK 3874 P-PROM has the following three parts: a leaded ceramic substrate with a modified 3870 bonded onto it, a small printed-circuit board that serves as an E-PROM socket, and an E-PROM that plugs into this socket.

TABLE 1: 3874-COMPATIBLE PROGRAMMABLE READ-ONLY MEMORIES

Programmable read-only memory	Memory size	3874 pinout option	3870 series device emulated
2732	4 K × 8	No. 2	3872
2532	4 K × 8	No. 1	3872
2716	2 K × 8	No. 1	3870, 3876
2758	1 K × 8	No. 1	—
82S2708	1 K × 8	No. 1 or No. 2	—

TABLE 2: MK 3870 SERIES SINGLE-CHIP MICROCOMPUTERS

Part	Read-only memory	Scratchpad random-access memory	Executable RAM
MK 3870	2,048 × 8	64 × 8	—
MK 3872	4,032 × 8	64 × 8	64 × 8
MK 3876	2,048 × 8	64 × 8	64 × 8
MK 3874	up to 4,032 external	64 × 8	64 × 8
Multichip F8	up to 65 K external	64 × 8	up to 65 K external RAM/ROM mix



2. Socket variations. The 3874 P-PROM emulator accepts five different MOS and bipolar E-PROMs. Pinouts for the 2716, a 2-K-byte E-PROM, require socket option (a) on the 3874, while the 2732, a 4-K-byte E-PROM, requires socket option (b).

programming equipment must be purchased, adding to the cost of the final design. In addition, only a moderately sized E-PROM can be integrated onto a microcomputer circuit while still retaining a manufacturable die size. For example, the die size of a single-chip microcomputer with 4-K bytes of E-PROM such as would be needed to emulate Mostek's MK 3872—a device with 4,032 bytes of ROM—would make the circuit unproducible with today's technology.

Additionally, the E-PROM process with which the entire chip is fabricated is not optimal for the processor section of the die. Many dynamic circuit techniques typically used in the processor circuitry must be avoided for the device to function properly when exposed to ambient light through the quartz lid needed for a UV-programmable E-PROM.

Circuitry compatible with the E-PROM process can, of course, be designed to perform the processor function, but it requires significantly more area than the high-performance process, resulting in a still larger die. Because it is not exactly like the high-performance process on the ROM version, there will still be subtle dc differences between the two versions.

Replacing the ROM

An optional approach to emulating a 40-pin single-chip microcomputer would consist of an integrated circuit with pins for external addressing capability in addition to the 40 original pins. Such a circuit, with memory address and data lines to access an external program, has been developed for the MK 3870. The MK 3874 was created by removing the ROM from the 3870 and placing address and data-bus buffers on the circuit in its place. This allows the emulation of a 3870 series device to be made using a circuit whose dc, timing, and process characteristics will match those of the final masked ROM parts.

Development of an external addressing 3870 would not by itself eliminate the problems associated with bulky pc cards now used for emulation purposes. To that end, Mostek has designed a new type of package that can house both the 3874 and a standard E-PROM.

The 3874 die is mounted on a 40-pin ceramic motherboard, with a small board of ceramic or phenolic board on top of it. This small pc has a 24-pin socket that accepts a standard E-PROM.

The entire module occupies the same board area as the final ROM-based part, facilitating its use in field prototyping and low-volume applications. The E-PROM can be removed for reprogramming and then reinserted as many times as desired.

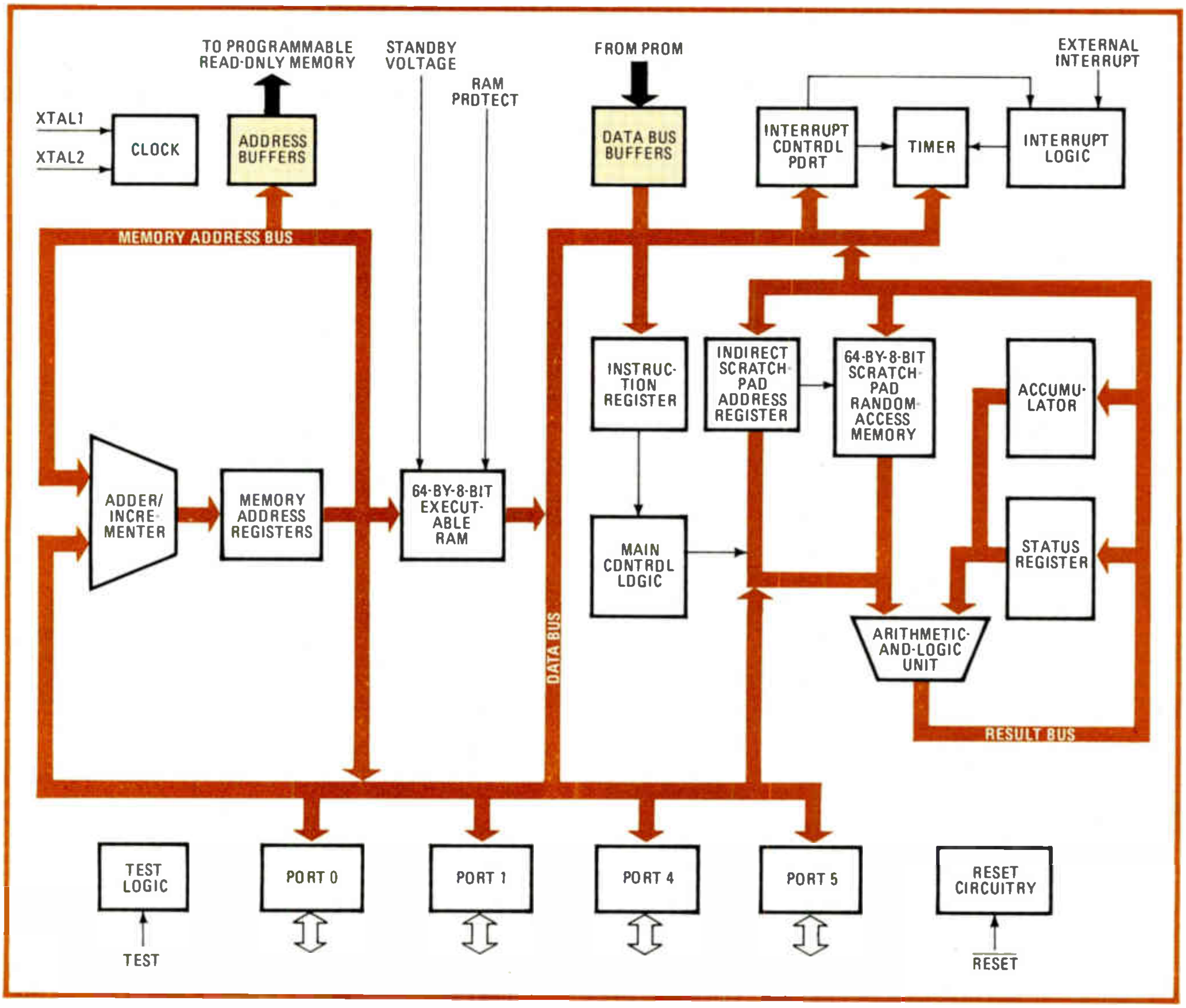
Mostek has a patent pending on two embodiments of this packaging design—the two-piece package, capable of surviving restricted environmental applications pictured in Fig. 1, and an industrially durable one-piece application package containing socket pins plus the 3874 chip, to be commercially available in 1980. Mostek's package will let the low-volume user enter into industrial applications with an environmentally durable design.

The 3874 P-PROM is designed to interface with standard, single-supply E-PROMs (see Table 1). All E-PROM timing- and single-level requirements are handled inside the 3874 so that the designer has the flexibility to select the PROM size that is correct for his application.

Some E-PROM signals, like address and data lines, must come from signals on the 3874 die, whereas others like power-supply inputs can come directly from the power-supply input pins on the 40-pin package. For the 2716 2-K-byte E-PROM (Fig. 2a), the output enable signal, pin 20, is tied to ground (pin 12) and the V_{pp} input (pin 21) is tied to V_{cc} (pin 24). The chip enable input, which could be tied to ground since this is a static part, is instead tied to A_{11} from the 3874 to allow insertion of a 2532 4-K-by-8-bit E-PROM. The 2716 will thus reside in the lower 2-K 3874 memory space, which is where it should be for 3870 emulation.

To interface the 3874 with the 2732 4-K-by-8-bit E-PROM (Fig. 2b), a revision of the socket board was required because of a change in pinout from the 2716. Pin 21 now becomes the signal A_{11} and pin 18 becomes a memory clock signal generated within the 3874. The two different socket board pinouts are shown in Figs. 2c and 2d and a list of 3874-compatible E-PROMs is given in Table 1.

Table 2 shows the memory configuration of each device in the 3870 family. The 3876, like the 3870, has



3. ROM-less. A block diagram of the 3874 shows address and data-bus buffers in place of the normal internal ROM of the 3870. This modification lets pluggable E-PROMs emulate ROM's program and dc characteristics, eliminating the need for large pc board emulators.

2-K bytes of ROM at locations 0-7FF$_{16}$. The 3872 has 4,032 bytes of ROM at locations 0-FBF$_{16}$. All parts have 64 bytes of scratchpad RAM, while the 3872 and 3876 each have an additional 64 bytes of RAM located at RC0-FFF$_{16}$. A mask option is available to give this extra RAM low-voltage standby power capability at the expense of two port pins. The 3874 contains this RAM and will be available with either the standard or the standby power option.

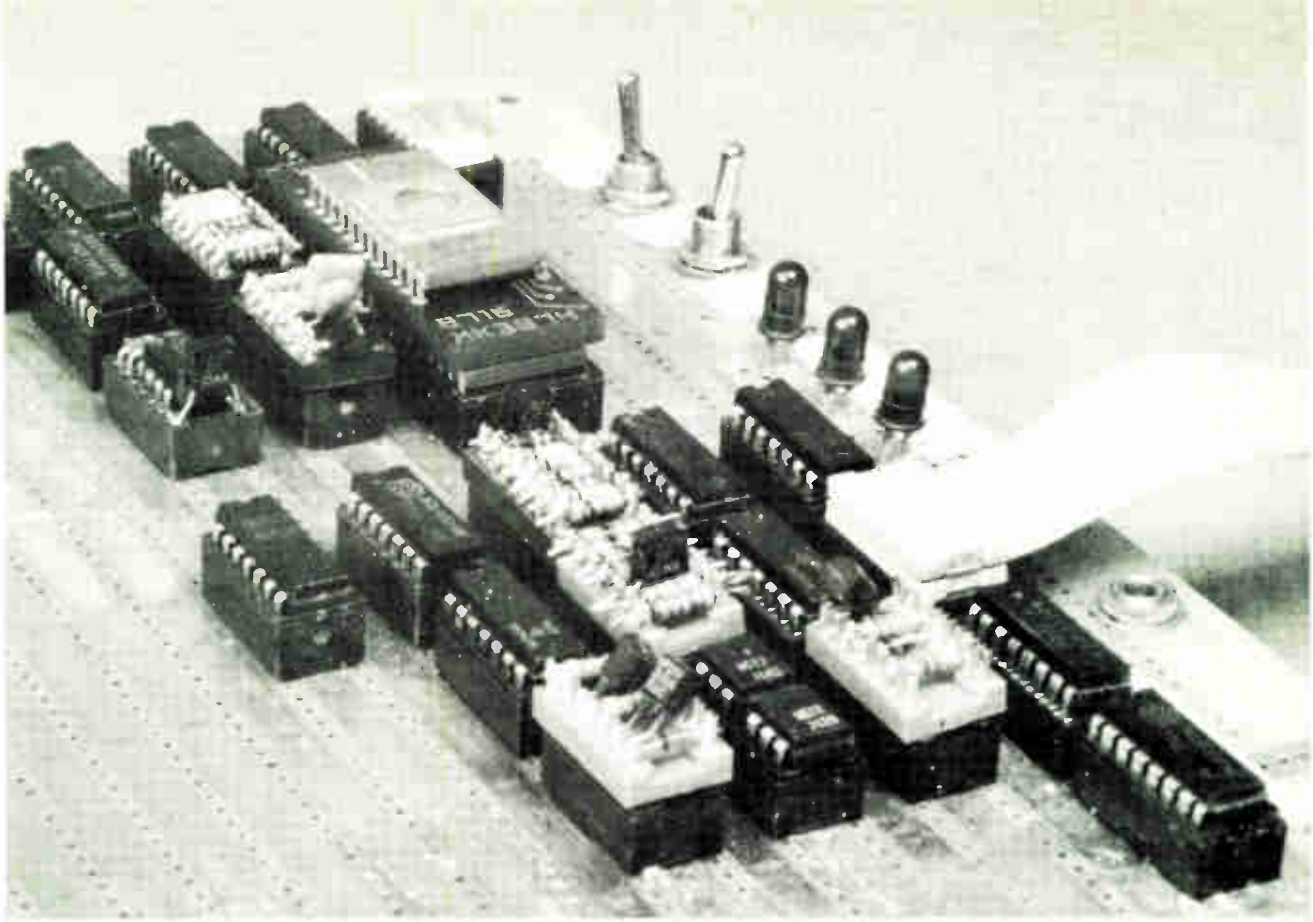
The socketed PROM of the 3874 P-PROM is addressed by either of two internal registers (Fig. 3). The program counter accesses op codes and immediate operands while the data counter is used to address data. Both of these registers are 12 bits wide on the 3874 and can address 4,096 bytes of memory. However, any access attempted from the upper 64 bytes of this memory space will address the internal RAM, not the external PROM.

The 3874 contains 32 lines (or 30 with the standby RAM option) of bidirectional input/output organized as four 8-bit ports. This chip has a built-in timer with a programmable prescaler, and vectored interrupts are provided for both the timer and external interrupt pin. The master clock can be derived from an external source, a crystal, a resistor, or an inductor. In addition, the 3870 architecture permits very efficient use of the scratchpad RAM and arithmetic and logic unit.

More available memory

The special capability of addressing up to 4-K bytes of program storage enables the 3874 to support a variety of applications that require more memory than is available on any other single-chip microcomputer. The large pluggable E-PROM is suitable for a variety of data table functions in place of computing an f(x) by a slow recursive algorithm. Also, requirements for mass data storage in character generation and display applications can now be met with this augmented program storage.

The standby-power option that was discussed previously is very useful in many applications where certain variables are to be saved when the main power supply is removed. Because the standby voltage ranges between 3.2 and 5.5 volts, only three nickel-cadmium



5. **On-board emulation.** With the 3874, emulation can be done on the system printed-circuit board. For low volume, the system can be shipped with the 3874 in place. In production, the actual microcomputer in a 40-pin dual in-line package can replace its emulator.

4. **Off-the-board emulation.** This microcomputer circuitry on a wire-wrapped integrated-circuit socket panel is being emulated off the board by a software development system and an application interface module (a printed-circuit board providing an in-circuit emulation of the microcomputer chip). The application interface module is cabled into the actual microcomputer socket.

cells (typically 3.7 V) in series are needed.

Software development begins on a machine such as Mostek's Matrix, a floppy-disk–based computer used for software development. This system provides tools for program development such as a text editor, assembler, and relocating linking loader, as well as a sophisticated peripheral management program.

Complete hardware/software debugging capability is obtained through the addition of an application interface module (AIM) to the Matrix development-system emulator instruments designed by Mostek. The AIM card is a pc board providing a real-time, in-circuit emulation of the 3870 family of microcomputers. Because the AIM card is an exact functional emulation of the MK 3870, it may be directly cabled to the 3870 socket in the target system (Fig. 4).

The program under development is stored in RAM on the AIM card where it can be examined and modified. Other debugging features are breakpoint insertion, register display and modification, and single stepping.

Storage convenience

The next phase of system design begins when the software is developed enough to facilitate the programming of specific E-PROMs. With one of these, the 3874 can be inserted into a wire-wrapped configuration of the microcomputer system for more extensive hardware and software debugging and system characterization as shown in Fig. 5. The small size of the 3874 permits field prototyping of the system in its final package configuration. For low-volume, quick-turnaround applications, the 3874 with PROM can be shipped as part of the final system. For high-volume applications, the final code, developed with the aid of the 3874, would then of course be integrated into a mask-ROM 3870.

Multiple program alternatives can be examined in the field without the limitations of bulky emulation boards. In addition, applications where the final volume does not justify mask-ROM parts are solved by using the MK 3874 with a standard MOS E-PROM or bipolar PROM. In fact, the MK 3874 gives the low-volume microcomputer user an inexpensive method of building a 4-K system. □

Peripheral controller turns to I²L

Four chips and a Z80 microprocessor make controller programmable for a variety of peripherals

by Jeffrey M. Wisted and David E. Tetzlaff, *Microcircuits division,*
and Fred B. McAleer, *Peripheral Products Co., Control Data Corp., Minneapolis, Minn.*

□ What's good for the goose is good for the goslings, makers of computer peripherals are discovering. Just as central processors have dwindled in size under the influence of large-scale integration, so too are peripheral controllers. Peripheral manufacturers are right behind the computer companies in bringing component counts down through increased use of custom LSI chips.

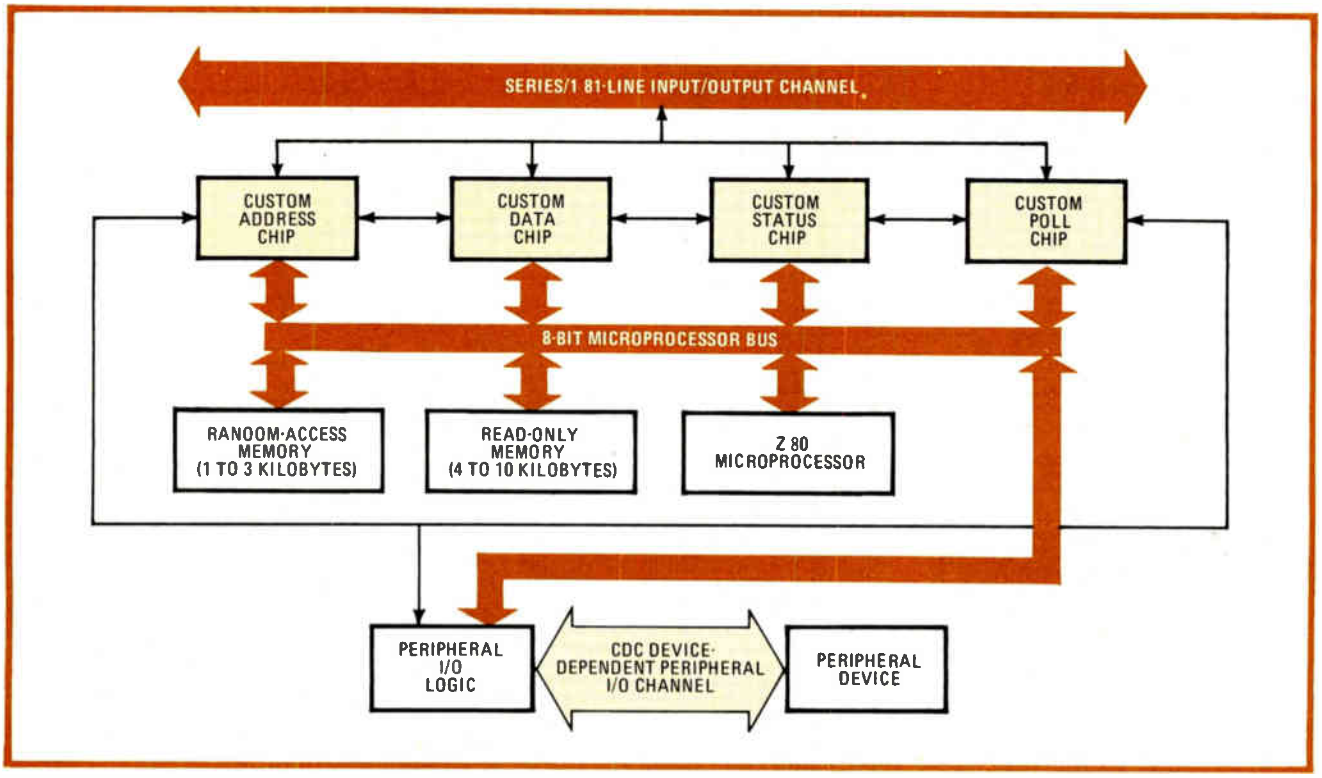
CDC was the first peripheral maker to design and even fabricate its own custom LSI logic for a peripheral controller. Earlier controllers occupied several printed-circuit boards or an entire cabinet. But thanks to CDC's four custom integrated-injection-logic chips and a Zilog Z80 microprocessor, the CDC Series/1 controller resides on a single 7-by-9-inch board.

This early entry to the growing single-board programmable controller market is compatible with International Business Machines Corp.'s Series/1 minicomputers. It plugs into a slot in the minicomputer chassis to control a variety of peripherals.

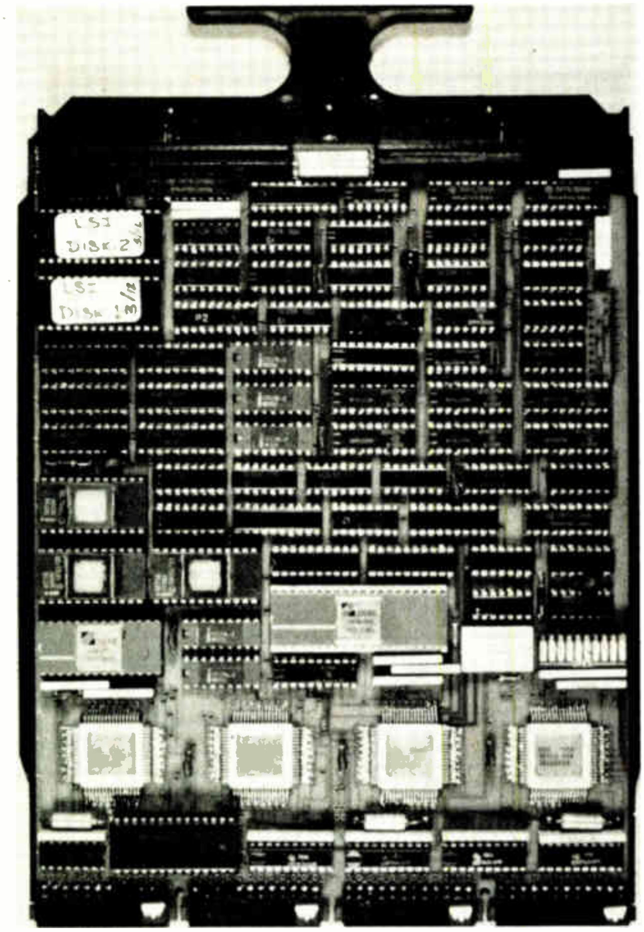
The microprocessor's programmability makes it possible to tailor the board to control a variety of devices with only minor modifications. It can handle low-speed devices such as flexible-disk drives, cathode-ray-tube terminals, and line printers and high-speed devices such as hard-disk drives.

The various peripheral types are connected to the controller through a device-dependent peripheral input/output channel (Fig. 1). The peripheral control logic, made up of standard TTL small- and medium-scale integrated circuits, is the portion of the board that must be adapted to the various peripheral devices.

The 8-bit Z80 microprocessor controls the peripheral using programs stored in read-only memory. Between 4 and 10 kilobytes of ROM can be mounted on the board,



1. Versatile I/O. The four custom integrated-injection-logic chips, working with a Z80 microprocessor, make a one-board controller that can be tailored to a variety of peripheral devices. Only the peripheral control logic and peripheral input/output channel need be modified.



2. Compact. The high levels of integration achieved on the custom I²L chip set make it possible to squeeze the entire controller onto a 7-by-9-inch board. Flat packs were used for the custom chips to save space; they are located close to the Series/1 bus connector.

using 2-K-by-8-bit Intel 2716 chips. The microprocessor also uses between 1 and 3 kilobytes of random-access memory. The Z80's 8-bit bidirectional bus is the central path for exchanging of instructions and data with the rest of the board.

The four custom chips interface the peripheral controller to the 81 lines of the input/output channel on the IBM Series/1 minicomputer. These chips allow the controller to emulate completely, and hence replace, IBM's input/output attachment feature. This allows a system designer to purchase a complete peripheral subsystem from one vendor and have it plug directly into the IBM Series/1 cabinet.

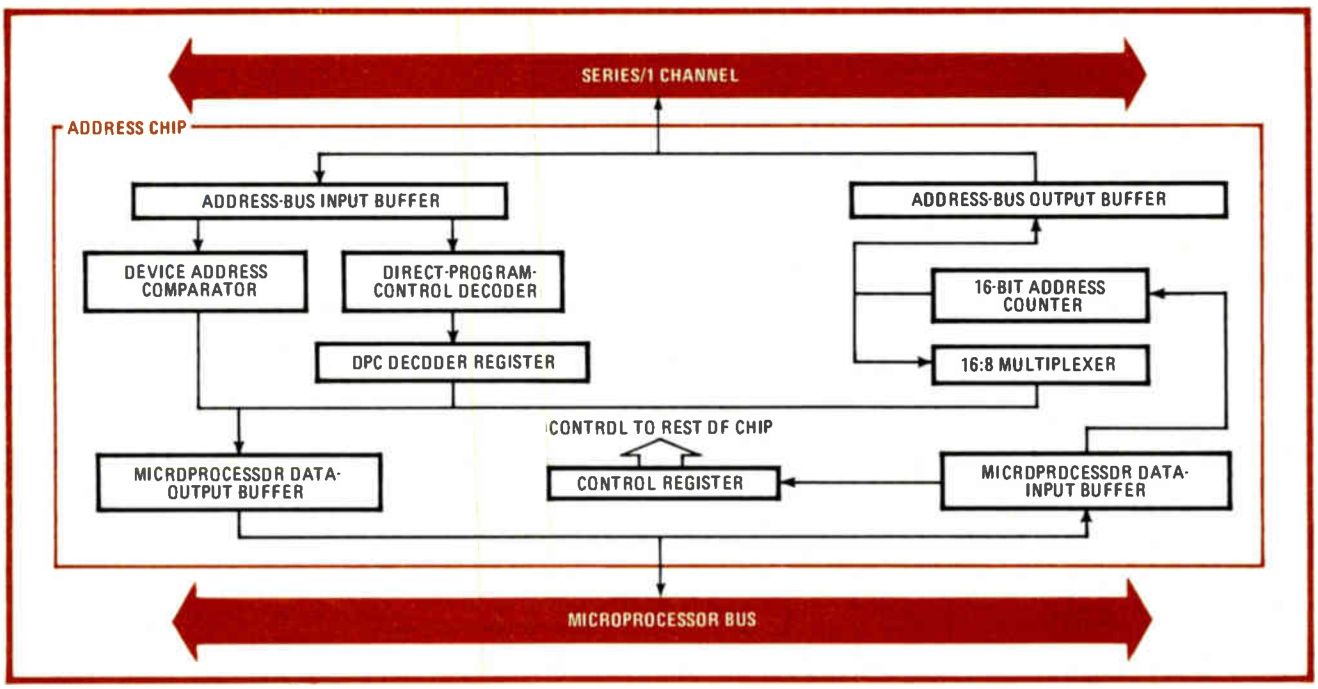
Space limitations

In order to plug directly into the IBM cabinet and backplane, it was necessary that the controller fit onto a 7-by-9-in. board. LSI circuits and a six-layer printed-circuit board were used to accomplish this. To pack the devices tightly on the board, fine 5-mil line widths with 7.5-mil spacing were used on the board.

The four custom chips, mounted in ceramic flat packs, are placed next to the IBM channel connector because most of the 81 channel pins are connected to these chips (Fig. 2). Next to them are the Z80 microprocessor and its associated RAM and ROM. The lower third of the board contains over 75% of the total logic in the controller and is common to all peripheral applications.

The custom chip set performs four general control functions—address and data control, status indication, and polling—that essentially give the controller its IBM-compatible personality. The operations of the four chips are controlled by the Z80 according to the firmware stored in ROM.

The custom chip set contains a total of approximately 2,600 gates. Integrated injection logic was used to



3. Microprocessor support. A counter on the address chip helps the Z80 perform direct memory access in the cycle-stealing mode by keeping track of addresses. When the peripheral is under direct program control by the minicomputer, this chip decodes instructions.

Immunizing I²L

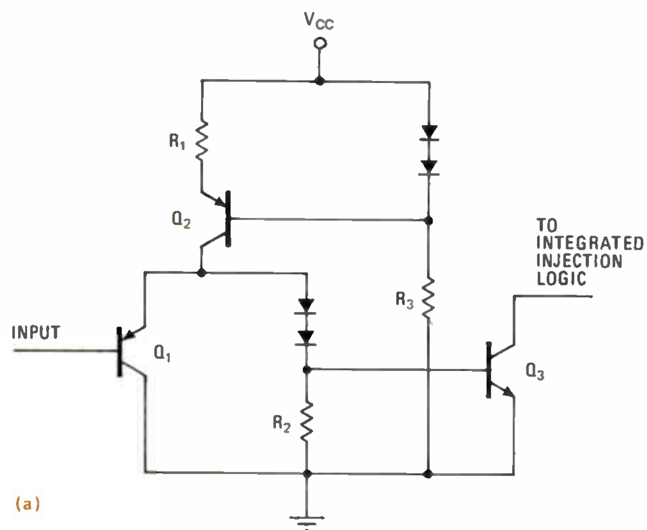
The custom large-scale integrated circuits designed and fabricated by CDC for its Series/1 peripheral controller use integrated injection logic for the sake of its speed, density, and low power dissipation. But because the I²L circuitry operates at such low voltages, it is rather susceptible to noise interference. Furthermore, it is not compatible with the TTL voltage levels used by the Z80 microprocessor and the rest of the controller's circuitry. To solve the noise problem and make interconnection easier, all inputs and outputs of the custom chips were buffered to make them TTL-compatible.

For the input buffer (a), the basic current mirror approach was used because it meets several needed performance parameters. First, the current source for the buffer's switch has voltage compensation built in. As the supply voltage (V_{cc}) varies, R_1 has a relatively constant voltage maintained across it to provide 1.5 milliamperes. The reference is simple yet may connect to several current sources. The main switch is compatible with the 1.4-volt threshold of TTL, as the current will change its path when the voltage at the emitter of Q_1 reaches 2.1 V, which is one diode drop above the input level.

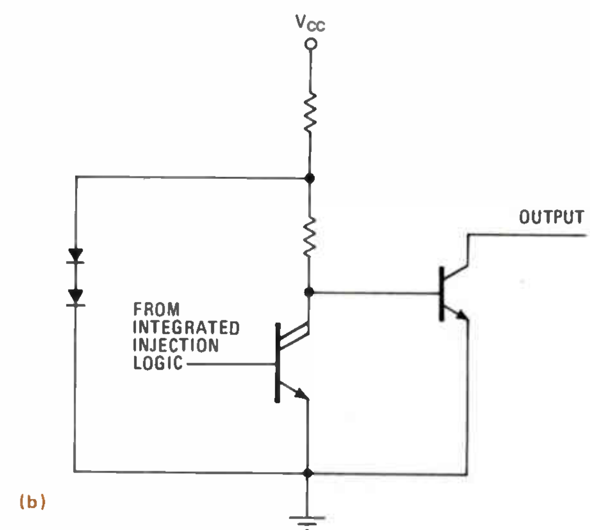
In the high state, the pnp input allows only leakage currents to flow, so it is a high-impedance load. In the low state, the current drawn is a function of transistor Q_1's beta and its collector current. Typically, input current in the low state is 100 to 150 microamperes. Thus it is ideally suited for applications requiring a heavy fanout. Q_3 is the first I²L transistor in the circuit. It is a special case in that it requires no injector current source: it gets its drive from the buffer-switch network.

The output buffer (b) is designed as an open-collector translator with an external pull-up to allow connection to a common bus. Where necessary, an internal pull-up was added to avoid extra external components. This design also provides bidirectional buffer capability because the output can be directly coupled to the pnp input transistor of an input buffer. A two-collector I²L device directly drives the final isolated npn transistor with the base drive coming from a relatively simple biasing network.

The requirements of the output driving device called for a collector-emitter saturation voltage of less than 0.4 V at 6.0 mA, a collector-base breakdown voltage of 20 V, a collector-emitter latch voltage of 7 V, and beta ranges from 60 to 150 at a 4-mA collector current. To provide additional noise immunity, the buffer's ground connections are made to a bus that is separate from the I²L circuits' ground line.



(a)



(b)

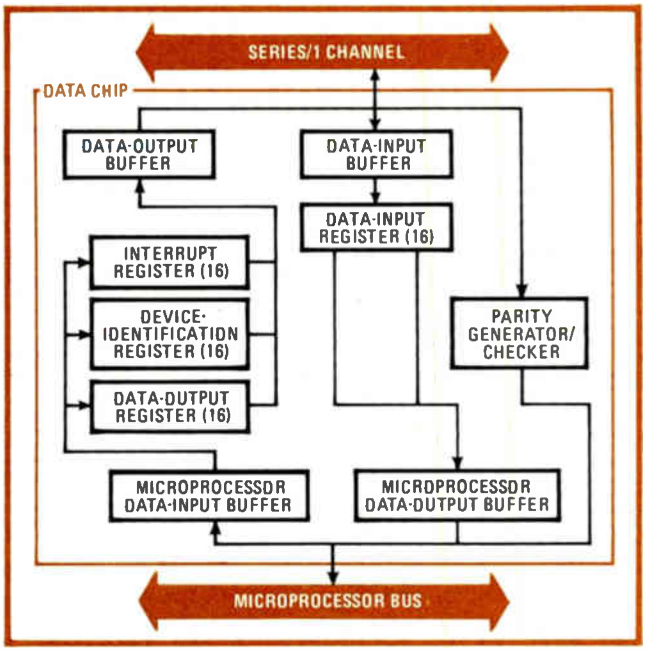
achieve this high circuit density, as well as for its low power dissipation and high speed. But to increase the custom I²L's noise immunity and to make chip interconnection easier, all the chips' inputs and outputs are buffered to be fully compatible with low-power Schottky TTL signal levels (see "Immunizing I²L," above).

So that the controller may fully emulate the IBM input/output attachment feature, the custom chip set allows operation in either of the two data-transfer modes used by IBM in the Series/1 minicomputer: direct program control (DPC) or the cycle-stealing mode. When a peripheral is under direct program control, the Series/1 central processing unit controls the peripheral device directly and must be interrupted to conduct the I/O operation. In cycle-stealing operation, the controller's microprocessor handles the I/O operation and sets up a direct-memory-access channel to the minicomputer's main memory. Instead of interrupting the CPU to complete the data transfer, the controller steals memory cycles to perform the DMA and only signals the central processor when the operation is complete.

Self-diagnostics

The custom chips include self-diagnostics that check out all major sections of the controller when the system is powered up without affecting the Series/1. All registers on the chips can be written into and then read back out for diagnostic purposes. These self-diagnostic features also simplify system debugging and wafer testing considerably.

Communication between the custom chips and the microprocessor via the microprocessor's 8-bit bidirec-



4. Store and forward. The data-circuit chip holds data on route from the central processing unit to the peripheral in an input register, and the other three registers store interrupt information from the Z80 for the CPU. A parity generator and checker maintains data integrity.

tional bus does not require any additional interfacing chips. This helps hold down the number of pins on the custom circuits—an important design concern (see "One chip or four?" p. 97). Eliminating interface circuits also reduces the number of interconnection paths on the circuit board.

The first and largest of the four chips is the address circuit that assists in controlling the flow of data from the CPU's memory to the peripheral. Of several functional logic blocks on this LSI chip, four—the microprocessor data-bus input and output buffers and the Series/1 system address-bus input and output buffers (Fig. 3)—interface the internal I^2L circuitry to the external TTL at its higher voltage levels.

The control register receives instructions from the Z80 and in turn determines the direction of flow on the chip's internal buses. Related to the CPU's address bus are the device-address comparator and the DPC decoder and register. The DPC decoder is used in the direct-program-control mode to execute simple instructions that do not require the use of the microprocessor. In this way the Series/1 CPU maintains control of information flow at all times during this mode of operation. The comparator looks for the address of the peripheral device that is attached to the controller and determines when the CPU is sending it data or instructions.

Address counter

The largest single portion of this circuit is the 16-bit synchronous storage-address counter. Its main purpose is to allow for sequential accessing of the Series/1 CPU's memory under control of the microprocessor during the cycle-stealing mode. Designed for either byte- or word-sequential transfer, the counter employs a parallel load feature as well as look-ahead carry in the counter stages.

The primary function of the data-circuit chip (Fig. 4) is to hold data temporarily and then transfer it either to and from the CPU memory or to and from the microprocessor bus. Four 16-bit registers hold the information for transmission. The input register receives 16 bits of data from the CPU. It then forwards the information 8 bits at a time to the output register that is connected to the Z80 microprocessor's bidirectional bus. Associated with this data register is a parity generator and checker to verify data integrity.

Registers report to CPU

The other three registers report to the CPU. An interrupt register reports with an interrupt information word upon completion of an operation. The device-identification register transmits a 16-bit word during a request for identification by the CPU. The data-output register is used for programmed DMA writing to the Series/1 memory under control of the microprocessor in the cycle-stealing mode. Containing about 800 gates, the data-circuit chip measures 170 by 190 mils.

The microprocessor uses the status chip to relay information concerning the condition of the peripheral subsystem to and from the minicomputer. Some of these reports are interrupt-condition codes that indicate the nature of the interrupt, such as normal or abnormal end of operation. An associated interrupt mask bit allows the interrupt mechanism to be turned on or off.

There are also several read-only status reports that indicate the state of the CPU and are obtained from the IBM channel. A 4-bit status-bus register is continuously monitored for information on the current CPU state; it indicates such conditions as power-on reset, system reset, and halt/machine check for proper operation on the Series/1 channel. The status chip measures 160 by 160 mils and contains 450 gates.

The final chip of the four is the poll circuit, which has primary responsibility for obtaining the CPU's attention to service the peripheral (Fig. 5). It also keeps track of the CPU's response to such requests so that the microprocessor can tell if the CPU is ready for data transfer.

Requests and responses

There are four diagnostic registers on this chip that the microprocessor may read from or write into. These registers hold multiple-byte data-transfer requests like cycle-stealing or burst requests and an interrupt request, which is generally used to simplify the start or completion of a data-transfer operation.

The poll chip also contains four status registers that are loaded by the CPU and are only read by the microprocessor. They report the current state of the CPU with bits indicating bad status, cycle-steal capture, and cycle-steal enable. These registers provide information about the status of cycle-stealing operation to the microprocessor. The poll chip measures 155 by 185 mils.

The largest of the four chips, the address chip, is a good example of the levels of integration achieved. Measuring 180 by 190 mils, it contains some 800 gates. The buffers that make the I^2L circuitry TTL-compatible are located on the chip's periphery. Two layers of metalization are used, with all the power buses on the second

One chip or four?

The custom logic used in the CDC Series/1 peripheral controller contains only 2,600 gates, a number suggesting single-chip integration. This level of integration has been achieved in other applications, but the nature of integrated controllers precludes a one-chip implementation given the current state of the packaging art.

A peripheral controller must retain as much information as possible concerning the current status of all system components. This typically requires many data inputs and control outputs. In the case of the Series/1 input/output controllers, the required lines include 81 for communication with the minicomputer channel, 33 for communication with the microprocessor system, and 27 for communication with the peripheral itself, a total of 141 lines.

This high pin count prohibits implementing the entire system on one chip; the largest commercially available package at the time of design had an insufficient number of pins. Of course, in a partitioned system, more pins are required to interface the separate chips. Thus the system required about 250 pins in the final four-chip version. The chips are mounted on 64-pin ceramic flat packs, which were chosen primarily because of the limited real estate on the board. Four dual in-line packages would never have fit, nor would other package types that require sockets.

layer and 95% of the logic interconnections on the first layer. Extensive use of resistive underpasses for logic interconnections was a significant factor in achieving the chip's density.

Compact I²L layout

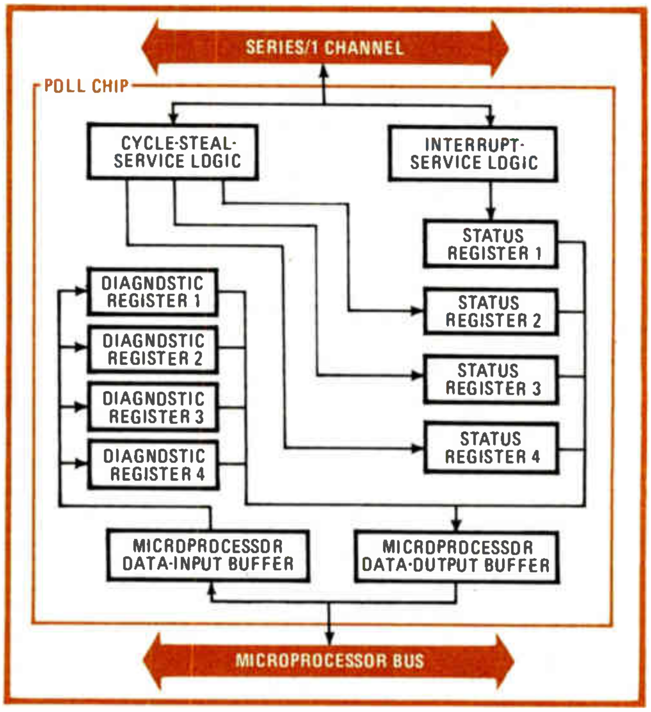
The I²L section is implemented with four-collector gates with standard bar geometry. Generally, the structure for this internal switch is two gates fed by a common lateral pnp injector. The position of the base contact is completely flexible, as are the collector positions, allowing a custom interconnection pattern. This flexibility makes possible a more compact layout than a gate-array structure with fixed collector and base positions. The minimum feature size is 2.5 micrometers on the I²L collector contacts and the underpass interconnection contacts.

The n^+ collar surrounding the gates improves beta readings for higher yields over process variations. Although the circuits operate at 150-microampere injector currents in this application, successful operation of test switches in the lab have been demonstrated in the ½-nanoampere range. Gate delay is in the 18- to 20-nanosecond range at 150 μA.

The basic transistor structure of the I²L device is built upon a p-type substrate. An n^+ buried layer provides a low-resistivity common-emitter region, and n-type epitaxial layer is the foundation for the transistor. The deep n^+ ring also serves as an excellent ground bus connection. The base p^+ diffusion has a resistivity of 100 ohms per square. An n^+ collector diffusion finishes the device profile. Collector latch voltages of the npn transistor are typically in the 5.0-volt range with I²L beta up in the range of 3 to 10. The change in beta from the collector nearest a base contact to the collector farthest from the base contact is typically 10% to 15%.

Computer-aided design

A very important part of the design process was the use of computer aids at various stages. While the buffer interfaces were being designed, for example, extensive simulation was performed to ensure that all design parameters were being met over specified voltage and temperature ranges. The program used the Ebers-Moll mathematical transistor models and allowed variations in component values to home in on the best design.



5. Hey, CPU! The poll-circuit chip gets the CPU's attention to service the peripheral. Its four diagnostic registers are either read from or written into by the microprocessor; the four status registers are read by the microprocessor and written into by the minicomputer.

The I²L truth table was verified by another computer program, which simultaneously produced a logic-design simulation. Given the characteristic I²L parameters of gate delay versus loading or collector position, this program picks out any flaws in the logic design or truth table before the design is implemented. The layout design rules were enforced and checked using various options in the automated layout system. These checks helped to minimize problems when the completed wafer was probed and helped avoid the costly redesign cycle. Computer-operated wafer testing using the previously verified truth table allows a final check to find the functional dice quickly.

The end result was a savings in both time and money. In only 10 months, all four custom circuits were taken from initial design to completely functioning chips satisfying the original specifications. □

Foldback limiter protects high-current regulators

by A. D. V. N. Kularatna
Ratmalana, Sri Lanka

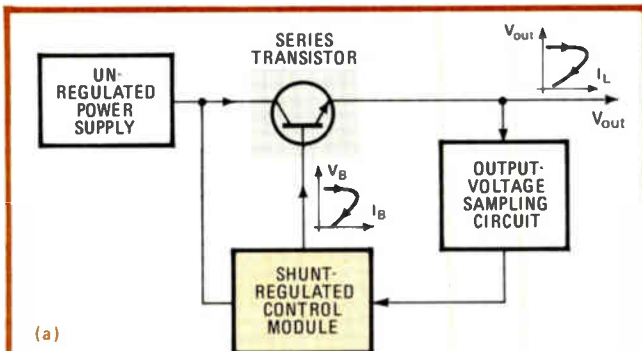
This circuit provides foldback protection for a series-regulated source that has to deliver high current. Because it requires no current-monitoring resistor, the circuit achieves wide dynamic response at good efficiency. It draws only 2% of maximum load current and its cost is reasonable.

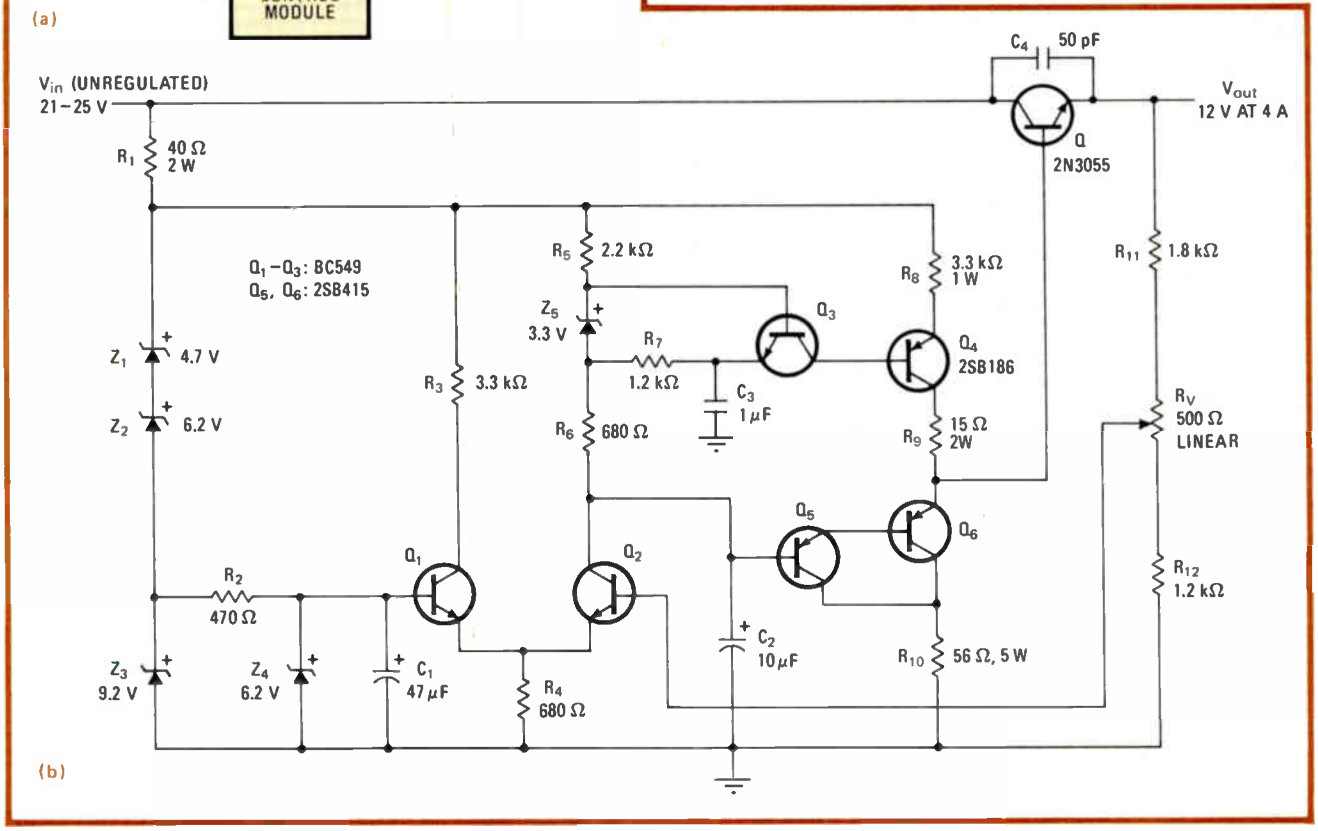
Here, a low-current shunt-regulated module (a) provides the overload protection. This module is configured into the conventional regulator system to work as a switch, in which role it quickly turns off a series-pass transistor when the load current exceeds some predetermined value.

The circuit details are explained with the aid of the diagram (b) for a representative regulator designed to deliver 12 volts at 4 amperes. Transistors Q_1 and Q_2 form a differential amplifier, which compares a 6.2-V reference to a potential derived from the 12-V output through potentiometer R_V. Shunt elements Q_5–Q_6 act to maintain the potential at the base of Q constant for any load condition by taking up the difference between the set and the actual base drive.

It is necessary that the current source Q_3-Q_4 be set to I_L/h_{fe} for proper tracking, where I_L is the maximum load current and h_{fe} is the current gain of Q. The value of the constant current, I, is $h_{fe\,Q4}\,(V_{Z5} - V_{be\,Q3})/R_7$, so that the current is most easily set by adjusting resistor R_7.

The module requires a current of 70 to 80 milliamperes under maximum load conditions. The short-circuit output current is less than 200 mA, because the drop in





High handling. Low-current shunt regulator (a) provides foldback limiting for high-current power sources at good efficiency and reasonable cost. Circuit (b) for 12-V regulator uses differential pair Q_1–Q_2 for detecting differences in reference and output voltage, Q_3–Q_6 for maintaining output potential by suitably controlling base drive to series pass transistor Q. Z_1–Z_3 minimize output ripple.

output voltage switches transistor Q_2 off. The voltage across zener diode Z_5 is then reduced to a very low value, and this action in turn lowers the voltage at Q_6 and cuts down the base drive to Q.

Zener diodes Z_1–Z_3 were added to improve the ripple characteristics of the supply. As configured, the source has an output ripple of 6 mV peak to peak.

The shunt regulator module can be easily configured for any output voltage mainly by selecting the appropriate zener-diode values. □

Remote controller sets universal motor's speed

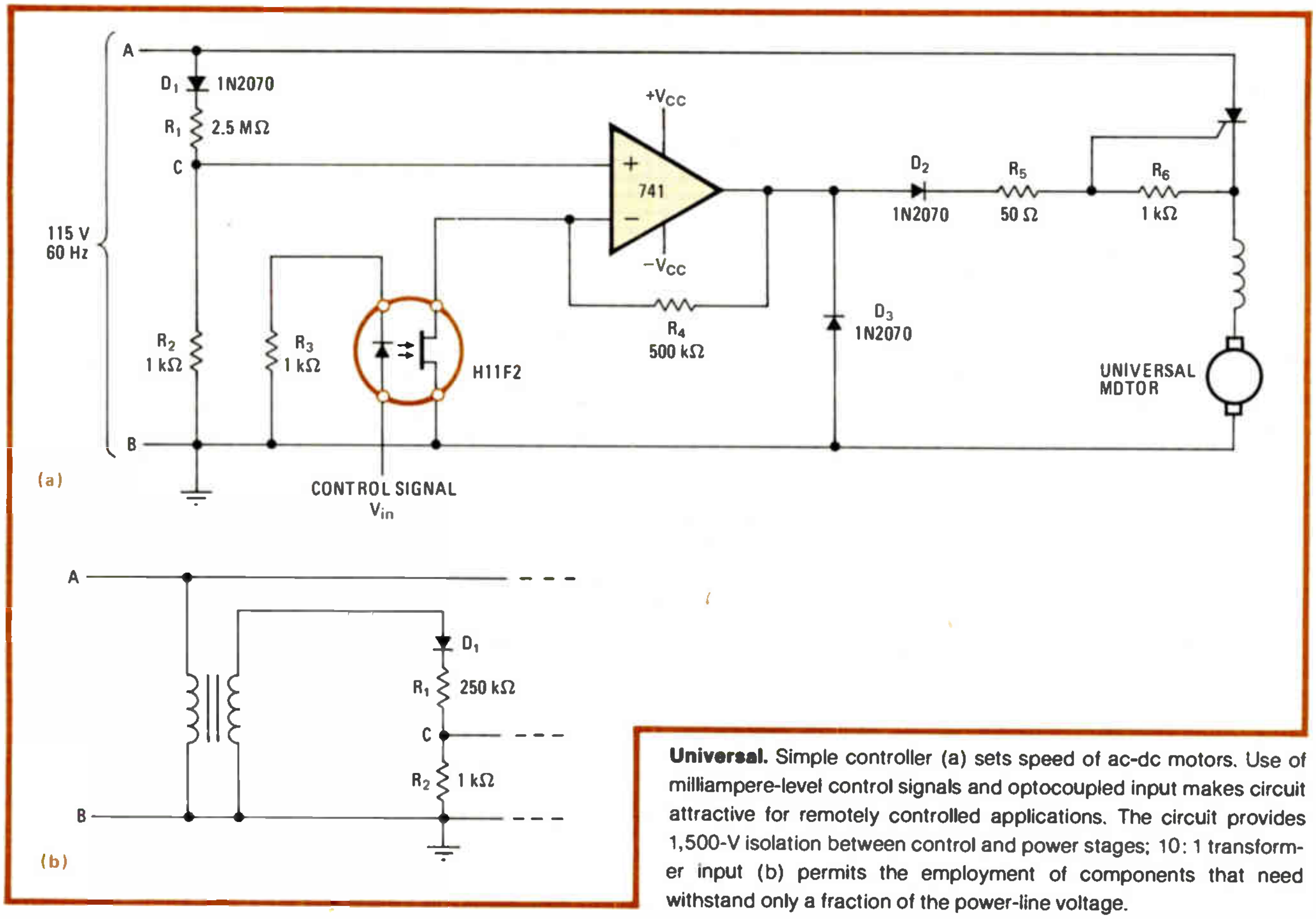
by Hari Herscovici
Cordis Corp., Miami, Fla.

The speed of an ac-dc motor is easily set with this circuit. Millivolt-level input voltages drive its variable-speed control amplifier through an optocoupler that is isolated from the rest of the circuit to permit its use in remotely controlled applications.

Control signals in the range of 0 to 3 volts are applied to the optoisolator (GE H11F2) as shown (a). The resistance between the drain and source of the device's field-effect transistor varies with input voltage V_{in}, and so the gain of the 741 operational amplifier, which amplifies the rectified 60-hertz power-line input, is controlled accordingly.

When the instantaneous output of the op amp is greater than the motor's counter electromotive-force voltage, diode D_2 conducts and thus the silicon controlled rectifier is switched on. Power is thereby applied to the motor. The greater the difference between the op amp's output and the counter emf voltage at any instant, which indicates motor speed is lower than programmed, the earlier in the cycle the trigger pulse to the SCR occurs.

Diode D_1 and resistors R_1 and R_2 have been selected so that the circuit will withstand a reverse voltage of 200 V. If a transformer-based input circuit (b) is substituted, however, it is only necessary for D_1 to have a reverse-breakdown value of 20 V. □



Universal. Simple controller (a) sets speed of ac-dc motors. Use of milliampere-level control signals and optocoupled input makes circuit attractive for remotely controlled applications. The circuit provides 1,500-V isolation between control and power stages; 10:1 transformer input (b) permits the employment of components that need withstand only a fraction of the power-line voltage.

High-voltage regulator is immune to burnout

by Michael Maida
National Semiconductor Corp., Santa Clara, Calif.

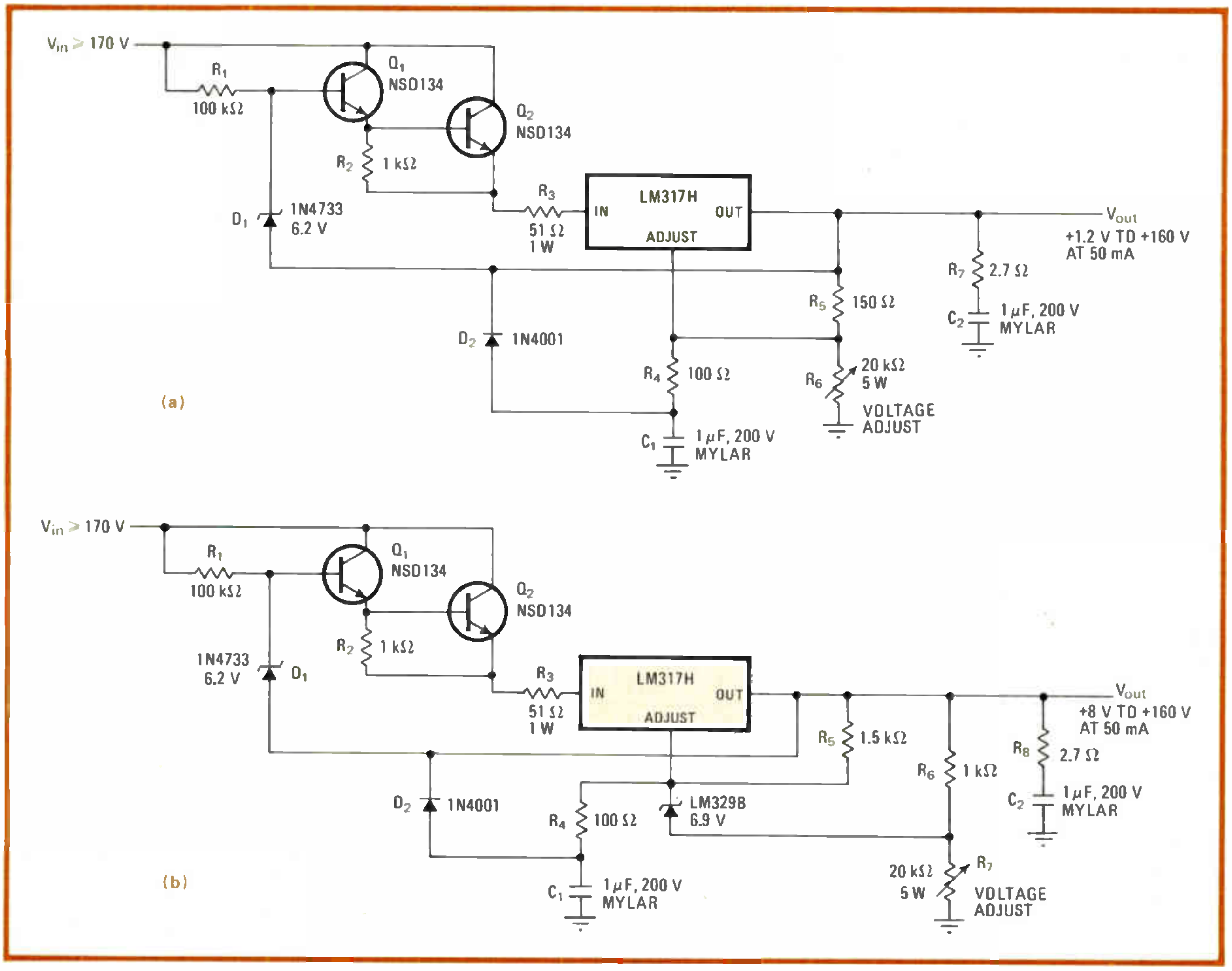
The floating-mode operation of adjustable three-terminal regulators in the LM117 family make them ideal for high-voltage service. Because the regulator sees only the input-output differential—40 volts for the LM117—its voltage rating will not be exceeded for outputs in the hundreds of volts. But the device may break down if the output is shorted unless a circuit can be developed for withstanding the high voltage typically encountered and the output current is limited to a safe value in the event of a dead short.

The circuit surrounding the regulator will serve to solve the problem. Zener diode D_1 maintains a 5-V input output differential over the entire range of output voltages from 1.2 to 160 V. Because high-voltage transistors inherently have a relatively low β, a Darlington arrangement is used to stand off the high input potentials.

The zener diode's impedance will be low, so that no bypass capacitor is required directly at the regulator's input. In fact, no capacitor should be used if the circuit is to survive a short at the output. Resistor R_3 limits the short-circuit current to 100 milliamperes. The RC network at the output improves the circuit's transient response, as does bypassing the adjustment pin. R_4 and D_2 protect the adjustment input from breakdown, if there should be a short circuit at the output.

The approach shown in (b) will serve well in precision regulator applications. Here a LM329B 6.9-V zener reference has been stacked in series with the LM317's internal reference to improve temperature stability and regulation.

These techniques can be employed for higher output voltages and/or currents by either using better high-voltage transistors or cascoded or paralleled transistors. In any event, the output short-circuit current determined by R_2 must be within Q_2's safe area of operations so that secondary breakdown cannot occur. □



Skirting shorts. Three-terminal regulator (a), configured for high-voltage duties as a consequence of operating in the floating mode, is protected by appropriate circuitry against burnout due to shorts. LM329B zener (b) and minor changes improve stability and regulation.

Software makes a big talker out of the 2920 microcomputer

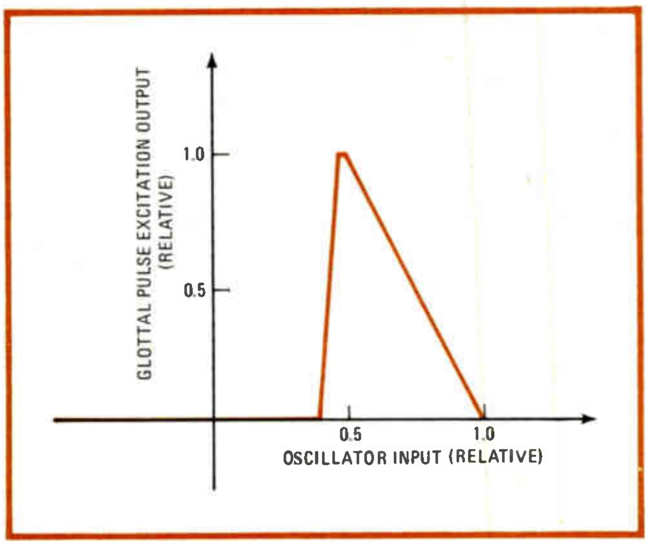
One-chip device's analog I/O and high speed suit it for a variety of speech-synthesis techniques

by M. E. Hoff and Wallace Li, *Intel Corp., Santa Clara, Calif.*

☐ The continuing advances of solid-state technology, coupled with the development of software analogs of human speech, have made possible the handful of speech-synthesis integrated circuits now incorporated or being designed into several consumer products. As a result, interest in such a capability has boomed, but so far only specialized chips could do the job.

The recently introduced model 2920 microcomputer, however, designed for signal-processing applications [*Electronics*, March 1, 1979, p. 105], readily lends itself to speech synthesis because of its analog input and output and its high speed. Through the use of appropriate software algorithms, it can implement a variety of speech-synthesis techniques.

A detailed explanation of all the useful algorithms would be out of place here. The software information that is provided, however, can be used as building blocks and developed further by users of the 2920. The primary emphasis of this information is on the modeling of formants, the characteristic components of speech sound.



1. Glottal pulse. The human vocal tract's glottal-pulse response can be synthesized by a piece-wise linear approximation of a nonlinear transfer function. The resulting triangular waveform contains the desired nonlinear characteristics, caused by overflow saturation.

Memory limitations

Speech-synthesis circuits depend heavily on the use of memory, because every part of human speech, right down to the smallest inflection, requires corresponding memory, whether that part is synthesized from the ground up or called up from storage. For example, the Speak & Spell teaching aid from Texas Instruments [*Electronics*, June 22, 1978, p. 39] requires a 128-K memory for a vocabulary of about 200 words. Obviously, the greater the number of points processed to approximate speech, the faster must bits be transferred out of memory and hence the more memory needed.

As a result, a major design goal for synthesis software is a reduction in the rate memory bits are transferred by the microprocessor from memory storage to the synthesis circuit. On the other hand, too low a bit-transfer rate can result in unnatural-sounding speech. The lowest rate practical therefore minimizes the amount of memory needed while still allowing continuous natural-sounding simulation of human speech.

Although direct recording of telephone-quality speech generally requires approximately 64 kilobits per second, that rate is too high to be of any practical use in speech-synthesis circuits. Fortunately, other techniques have been developed, like linear predictive voice encoders (vocoders), that can provide synthesized speech of adequate quality at 1,200 to 2,400 b/s. There are even formant-modeling methods being investigated that might some day make it possible to synthesize acceptable-quality speech at 600 b/s.

Most approaches to synthesizing speech using a low bit rate involve modeling of the human speech tract. In human speech, there are two basic sound sources, a buzzing tone produced by the vibrations of the vocal cords and noise produced by air turbulence. These basic sounds are modified by the characteristics of the human speech tract—the throat, mouth, and nasal cavities. To reduce the bit rate, the bandwidth is compressed in modeling so that the rate of change of the filters and generators used is relatively slow when compared with the rate of change of the bandwidth of the resulting

TABLE 1: GLOTTAL PULSE GENERATOR					
Oscillator to produce sawtooth waveform. Frequency = PV ÷ sample rate/32.					
SUB	OSC,	PV,	R05		Update sample of oscillator.
LDA	DAR,	OSC,	R00		Move to DAR to test sign.
ADD	OSC,	KP4,	L01,	CNDS	Restore to positive value if negative.
Modify waveform as follows:					
LDA	GPE,	KM6,	R00		Initialize dc value.
ADD	GPE,	OSC,	L01		Add 2xOSC value.
ADD	GPE,	GPE,	L02		Multiply value by 5 to produce saturation.
SUB	GPE,	OSC,	L01		
ADD	GPE,	KP4,	R01		Correct for dc and clip top.

sound. Instead of samples of the sound waveform as in synthesis based on recording and storing actual speech, samples of the parameters of the model are saved for later delivery to the synthesizer.

There are three basic ways to model the human speech tract for synthesized speed. All three simulate the pulse periods of the vocal cords and the noiselike sound produced by air turbulence in the vocal tract.

Viewing the human speech tract in terms of a physical model provides a better understanding of how these techniques simulate human speech. An extremely simple one is that of a tube with varying widths. These variations in width cause deflections of the air passing through the tube, resulting in the production of several resonant frequencies.

Three basic synthesis methods

In one method, the tube is approximated by a lattice filter containing a series of fixed-delay elements wired in cascade, with a reflection coefficient defined for each stage. Because the filter coefficients may be derived by linear-prediction techniques, this synthesis structure is often referred to as a linear-predictive vocoder.

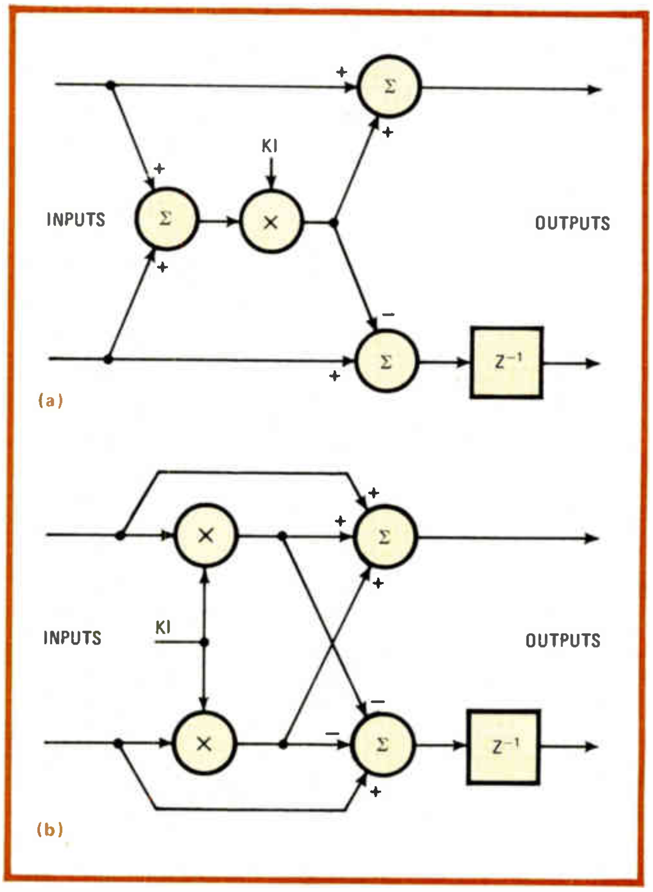
A second approach uses an array of narrow band filters that cover the speech spectrum. The gain of each filter is controlled in such a manner as to imitate the transmission properties of the human speech tract. This technique is used in channel vocoders.

A third method consists of modeling the speech tract as a variable filter, typically as a cascade of second-order recursive sections. Each filter section's center frequency (and in some cases bandwidth) is varied. Such filters are used to simulate the resonances (formants) observed in the human speech tract, which carry the primary information content of speech. Despite the fact that the extraction of formant data from sampled speech is extremely difficult to do, this method has the potential for using the lowest memory bit rate.

Speech excitation

The main source of speech excitation is a series of glottal pulses produced by variable constrictions in the speaker's throat. These pulses can be modeled as somewhat asymmetrical triangular pulses, each lasting approximately one half the pulse period.

The pulse rate for male speakers is roughly 100/s; for female speakers, it is about 200/s. Although these rates can be synthesized by the use of an impulse-train generator driving a filter whose impulse response resembles that of the glottal pulse it is trying to reproduce, this technique could produce some alias distortion.



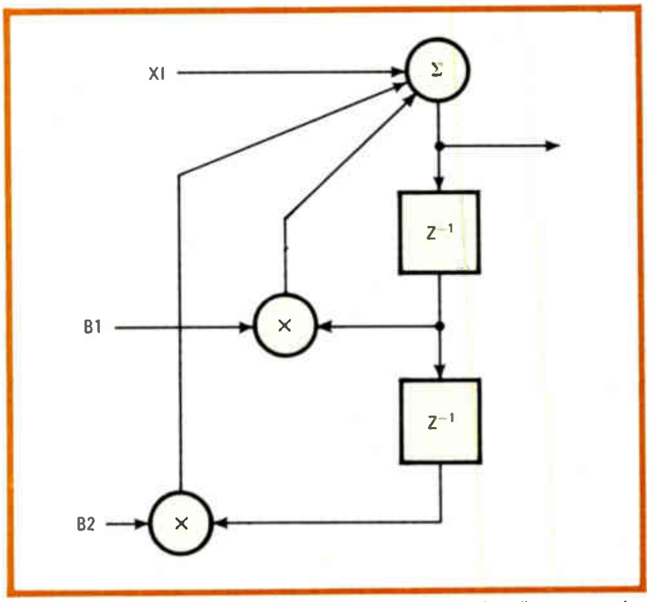
2. Lattice filters. These lattice-filter structures simulate human speech-tract behavior. Their parameters must vary with time to properly model the changes in frequency response of the tract. Each filter stage may require one (a) or two (b) multiplications.

Because an impulse train is a wideband signal, if it is not exactly a submultiple of the speech sample rate, its components may interact with the speech sample rate and produce undesirable audible beat notes.

Another approach is to take a nonlinear transfer function and linearize it by piece-wise approximation. The

TABLE 2: NOISE GENERATOR ROUTINE

Random-noise generator using feedback shift register. Register length is 17 bits. First, test for all 0s condition – ensure proper start. TEMP is a temporarily used variable, and NGEN is the generator output.				
LDA	TEMP,	NGEN,	L1	Test subtraction. Negative result implies need for initialization.
SUB	TEMP,	KP1,	R13	
LDA	DAR,	TEMP		Move to DAR for sign test.
LDA	TEMP,	KP4,	CNDS	Initialize if DAR is negative.
Next, fetch the 17th bit, test, and move to DAR as follows:				
LDA	TEMP,	KP1,	R13	
AND	TEMP,	NGEN,	L1	
SUB	TEMP,	KP1,	R13	Test subtraction to convert bit to sign.
LIM	DAR,	TEMP		Set DAR = +1.0 for 1, −1.0 for 0.
Next bit of shift register is XOR of bit 17 and bit 5. Generate in DAR as follows:				
XOR	DAR,	NGEN		
Shift register right and fill in new value as follows:				
LDA	NGEN,	NGEN,	R1	Shift right
ADD	NGEN,	KP4,	CNDS	



3. Recursive filter. A basic second-order recursive filter can also model the human speech tract. The filter's frequency characteristics are varied by variables instead of constants. When combined with a single 2920 microcomputer, a formant synthesizer results.

linearized function is then used to convert a sawtooth waveform to the desired glottal waveform. The harmonic content of such a synthesized waveform is much lower than that of an impulse-train synthesized signal. That means that distortion due to interaction with the speech sample rate is sufficiently suppressed to render the undesirable components negligible.

Writing the 2920's programs

The 2920 contains an erasable programmable read-only memory capable of storing up to 192 instructions of 24 bits each. It executes all of the instructions in sequence—the only jump allowed is from the program's end to the beginning. These programs usually consist of a series of sections each simulating the behavior of some analog circuit. All of the programs are executed repeatedly at a rate that establishes the 2920's system sampling rate.

Each of the programs shown here makes use of assembly language. Each program line or statement consists of an operation code, a destination location, a source location, a source-scaling code, and an optional condition or input/output code, in that order. Source and destination codes rate symbolic names that refer to random-access memory locations or to certain special registers. RAM locations are automatically assigned by the assembler to symbols defined by the user.

RAM locations consist of 25-bit 2's complement binary numbers. These numbers have an imaginary binary point just to the right of the sign bit. Any variable X can thus fall in the range $-1.0 \leq X < +1.0$, with a resolution of 1 part in 2^{24}. The largest positive value for any variable is $+1.0-2^{-24} = 0.99999994$, which is equal to $+1.0$ for all practical purposes.

Operation codes and meanings are:

ADD	add scaled source to destination
SUB	subtract scaled source from destination
LDA	load scaled source to destination
ABS	load scaled absolute magnitude of source to destination
ABA	add scaled absolute magnitude of source to destination
LIM	load limited value of source to destination
XOR	exclusive-OR scaled source with destination
AND	AND scaled source with destination

The operand LIM produces a value of +1.0 if the source operand is greater than or equal to 0. Otherwise, it produces a value of −1.0.

Scaling codes are designated L2, L1, R0, R1, ... R13, for binary shifts of left 2, left 1, and so on, through right 13 and correspond to a multiplication of the source operand by 4, 2, 1, ½, etc., through 2^{-13}.

Special register codes include DAR for the I/O register that communicates with the analog-to-digital conversion circuitry and an array of constants KM8, KM7, ... KM1, DPO, KP1, ... KP9, that correspond to values −1, ⅞, ... −⅛, 0, +⅛, ... +⅞, respectively.

If the operand is ADD or LDA and the I/O field contains a code of the form CNDS, CND7, ... CND0, the arithmetic operation is executed on the condition that the DAR bit of the I/O register is tested. If the selected bit is 0 (CNDS selects the sign bit, CND7 the next higher-order bit, and so on), no operation takes place. If it is a 1, the designated operation occurs. The conditional SUB command is used for division. Other I/O field codes control input sampling, analog-to-digital conversion, and the output.

It starts with a triangular wave

The first portion of the glottal pulse-train synthesis routine is a triangular-wave oscillator—that is, a program that computes at each pass a value equivalent to a sample of a sawtooth waveform at the pulse frequency. Each sawtooth wave sample is passed through a nonlinear transformation for conversion into a series of asymmetrical triangular pulses. The program for the glottal pulse synthesizer is shown in Table 1.

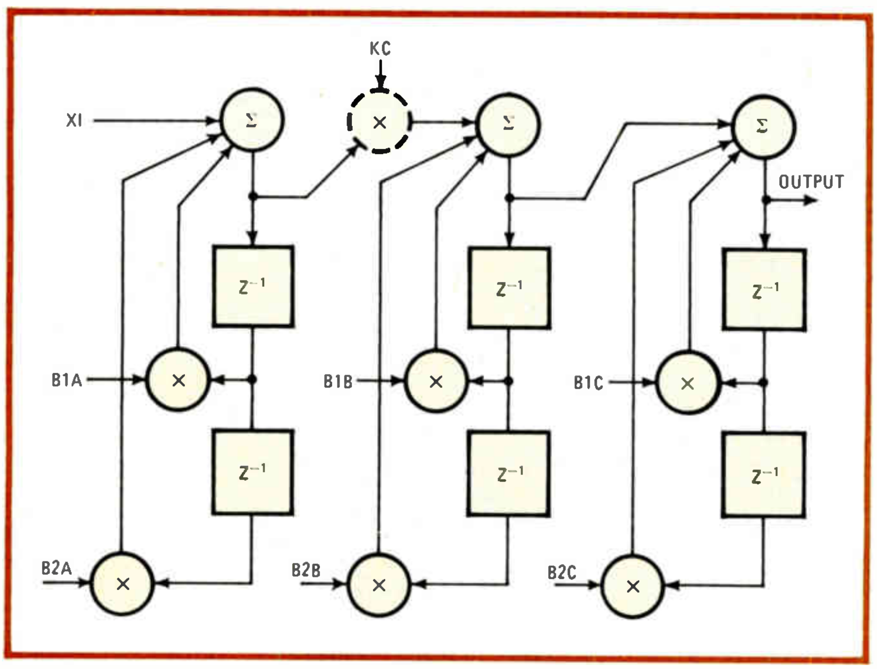
The first portion of the program is the sawtooth oscillator. PV (standing for "pitch variable") is a random-access memory location that controls speech pitch, or frequency, and OSC is a RAM location where samples of the sawtooth oscillator are computed. The oscillator produces a sawtooth waveform having a peak value of + 1.0 and a minimum value of 0.

At each pass of the program, or sample interval, the value representing the frequency (designated by the variable PV) is subtracted from the contents of OSC and scaled down such that when PV = 1.0 and the sample rate is 8 kilohertz, the oscillator runs at 250 hertz. The oscillator sample is passed to the DAR register and tested for a sign. If subtraction of PV produces a negative result, the OSC sample is restored to a positive result by the addition of + 1.0 by the conditional ADD instruction.

The second portion of the program is for nonlinear transformation. This transformation is accomplished by taking the sample value from the oscillator and converting it to a new value (represented by the variable GPE) that approximates the glottal pulse excitation. The transformation, which is represented by the transfer characteristics shown in Fig. 1, is made possible by overflow saturation that produces the desired nonlinearities. Because the oscillator sawtooth waveform runs from + 1.0 to 0, the transform of Fig. 1 appears to be a mirror image of the glottal pulse waveform as it would appear

TABLE 3: PROGRAM FOR LATTICE FILTER

Inputs are designated XI, YI, and outputs are XO, YO. Control parameter is KI. Input to delay stage is designated YID. Delay realization is accomplished by:			
LDA	YO, YID		
Set up multiplier. TMP1 and TMP2 are temporary locations.			
LDA	TMP1, XI		Generate RI + YI in TMP1.
ADD	TMP1, YI		
LDA	DAR, KI		Load multiplier into DAR.
LDA	TMP2, KPO		Clear product area.
Execute multiplication sequence, 9-bit KI resolution, in 4 quadrants as follows:			
ADD	TMP2, TMP1, R1,	CND7	
ADD	TMP2, TMP1, R2,	CND6	
ADD	TMP2, TMP1, R3,	CND5	
ADD	TMP2, TMP1, R4,	CND4	
ADD	TMP2, TMP1, R5,	CND3	
ADD	TMP2, TMP1, R6,	CND2	
ADD	TMP2, TMP1, R7,	CND1	
ADD	TMP2, TMP1, R8,	CND0	
SUB	TMP1, TMP1, R1,		Optional if KI is positive.
ADD	TMP2, TMP1, R0,	CNDS	
Compute outputs as follows:			
LDA	XO, XI,		
ADD	XO, TMP2,		
LDA	YID, Y1		
SUB	YID, TMP2		



4. Cascade. When a cascaded second-order recursive-filter structure is used to model the human speech tract, the filter's pole positions may also influence the system's overall gain. As a result, a gain-compensation stage (dotted line) may be necessary.

TABLE 4: VARIABLE-FREQUENCY FILTER STAGE

Program for variable frequency filter.
Input is XI, output is YO, intermediate values are Y1 and Y2.
B1 coefficient is an 8-bit positive variable, stored as half value in location designated HB1.
B2 is realized by successive additions/subtractions and has the value −0.9375, corresponding to a bandwidth of approximately 82 Hz, when the sample rate is 8 kHz.
Propagate through delay stages as follows:

LDA	Y2,	Y1,	R00	
LDA	Y1,	YO	R00	

Generate B2 ÷ Y2 in 40 as follows:

LDA	YO,	Y2	R4	+ 1/16 Y2 in YO
SUB	YO,	Y2	R0	

Set up for multiplication as follows:

LDA	DAR	HB1	R0

Perform multiplication and add to YO as follows:

ADD	YO,	Y1,	R0, CND7
ADD	YO,	Y1,	R1, CND6
ADD	YO,	Y1,	R2, CND5
ADD	YO,	Y1,	R3, CND4
ADD	YO,	Y1,	R4, CND3
ADD	YO,	Y1,	R5, CND2
ADD	YO,	Y1,	R6, CND1
ADD	YO,	Y1,	R7, CND0

Add input to filter, scaled to prevent overflow for setting above 300 Hz, as follows:

ADD	YO,	Y1,	R7

Filter range is 0 to 2,000 Hz. Center frequency resolution is 5 Hz at 2,000 and 22 Hz at 300 Hz.

on an oscilloscope displaying the sawtooth.

The noise generator may be simulated by a pseudo-random number generator. Its software program, listed in Table 2, is implemented by a feedback shift register that uses only one variable location. The exclusive-OR operation (XOR) is used to generate the bit that is entered into the shift register.

Modeling the response with filters

The outputs of both the noise generator and the glottal-pulse generator are modified by filters whose parameters must vary in time to model the changes in frequency response of the speech tract. Two filter types that have been used to model speech-tract behavior are lattice and time-variable recursive filters.

Figure 2 is a block diagram of two lattice filters. Each filter stage may require one or two multiplications of the input values by a variable coefficient. Since adequate speech synthesis typically requires about 10 lattice-filter stages, a single 2920 microprocessor may not suffice for an entire synthesis structure.

Table 3 shows a typical program for a single lattice-filter stage equivalent to that of Fig. 2b. The variable KI represents the control parameter, which is different for each stage. A typical speech synthesizer would require two 2920s, the first for the excitation generator and the first few stages of the lattice filter and the second to make up the remaining stages of the lattice filter. The results from the first stage must be passed to the second stage by transmitting analog or digital data between each of the 2920's analog ports.

Although a lattice filter usually requires two 2920s, a formant synthesizer may be made with a single 2920. Here, the speech tract is modeled by a cascade of second-order recursive sections, whose basic configuration is shown in Fig. 3. The frequency characteristics of this filter are varied by the use of variables instead of constants for one or more of the coefficients B1 and B2. If the format bandwidth remains fixed, only coefficient B1 is varied. For adequate synthesis, at least three stages must generally be cascaded; in other words, at least three formants must be realized.

Cascaded

When a cascade structure such as that shown in Fig. 4 is used to model the speech tract, the position of the poles of the filters may influence not only the frequency response but also the overall gain of the filter system. Gain compensation may therefore be necessary. One approximation for such compensation involves measuring the difference between the B1 coefficients for the first and second stages of the filter and generating the factor KC, which is proportional to this difference.

Table 4 shows the program for one stage of a fixed-bandwidth variable-frequency filter. As can be seen, resolution is limited at 300 Hz to 22 Hz per step. Finer resolution could be obtained by reducing the control range of the filter or by extending the multiplication precision. To reduce the control range, the coefficient B1 may be separated into fixed and variable components, with the variable component scaled down to cover a smaller range.

For each of the filter structures discussed, one or more variables were used as control parameters for a synthetic-speech output. As previously noted, these control parameters must be provided to the speech-synthesis circuit at a rate that is adequate to model the physical changes of the vocal tract during speech. Shifting digital data into a 2920 input port at 1 or 2 bits per sample time is adequate if the data is properly distributed into the various random-access memory locations where it is required. The program shown in Table 5 allows 10 parameters of 8 bits each to be delivered 100 times per second when an 8-kHz sample rate is used. During each pass through the sample program, 1 bit is entered and shifted into a holding register, designated SR. A portion of the program is used to produce two oscillators, one of which divides the sample rate by eight to produce the word rate for data entry.

Two ways to transfer

Two methods are shown in Table 5 for distributing the data assembled in the input shift register SR to the final parameter locations. One method provides simultaneous transfer of all parameters; the other behaves more like a commutator. The latter technique uses a ring counter for the second oscillator.

Part (a) of Table 5 shows the input program, and

TABLE 5: SERIAL DIGITAL DATA INPUT AND DISTRIBUTION

(a) Serial data input routine

Serial data input routine – low-order bits first. Part 1 is a single-bit a-d conversion, which may be overlapped with filter or transformation processing.

```
                      INO    Sample input – 6 INs used here.
                      INO
                      INO
                      INO
LDA   DAR,   KP4,     INO    Set input threshold.
                      INO
                      NOP
                      CVT7   Set bit 7 of DAR to reflect input value.
```

Next, transfer the tested bit into the input shift register. SR is the variable allocated to the shift register.

```
LDA   SR,   SR,    R1     Move data in register to right.
ADD   SR,   KP4,   CND7   Add tested bit.
```

(b) Data distribution – simultaneous transfer

Program to route data from shift register SR–10 values at 8 bits each. Oscillator set at 1/8 sample rate–designated CTR1.

```
ADD   CTR1,  KM1
LDA   DAR,   CTR1
LDA   CTR1,  KP7,          CNDS
```

A set of delay stages to hold input words is defined in locations TH0, TH1, . . . TH9. Transfer takes place each time oscillator CTR1 cycles.

```
LDA   TH9,   TH8,          CNDS
LDA   TH8,   TH7,          CNDS
LDA   TH7,   TH6,          CNDS
LDA   TH6,   TH5,          CNDS
LDA   TH5,   TH4,          CNDS
LDA   TH4,   TH3,          CNDS
LDA   TH3,   TH2,          CNDS
LDA   TH2,   TH1,          CNDS
LDA   TH1,   TH0,          CNDS
```

Data assembled in the input shift register JR is loaded, and then SR is cleared for the next input.

```
LDA   TH0,   SR,           CNDS
LDA   SR,    KP0,          CNDS
```

A second oscillator runs at 1/80 of the sample rate (1/10 the word rate).

```
ADD   CTR2,  KM3,   R2,    CNDS
LDA   DAR,   DTR2
LDA   DTR2,  KP7,          CNDS
```

This oscillator controls transfer of data from the holding register to the first control parameter locations (designated CP0, CP1, . . . CP9).

```
LDA   CP9,   TH9,          CNDS
LDA   CP8,   TH8,          CNDS
....
etc.
```

(c) Data distribution–sequential transfer

Program for distribution of 10 values at 8 bits each. If nonsimultaneous transfer is acceptable, a sequential data-distribution technique can be used. One oscillator, CTR1, runs at 1/8 sample rate. A second oscillator, CTR2, operates with a circulating 1. Divide-by-8 oscillator is as follows:

```
ADD   CTR1,  KM1
LDA   DAR,   CTR1
LDA   CTR1,  KP7           CNDS
```

Set up mask area to all 1s if oscillator cycles. Otherwise set to all 0s.

```
LDA   MASK, KP0
LDA   MASK, KP4,    L1,    CNDS
```

Ring counter oscillator; cycle length is 10 instructions.

```
LDA   CTR2,  CTR2,  R1             Shift right.
LDA   DAR,   CTR2,  L2             Test for shift past 10th bit.
SUB   DAR,   KP4,   R7
LDA   CTR2,  KP4,          CNDS
```

Combine ring counter and mask to generate control mask.

```
AND   MASK, CTR2,
```

Move to DAR to test first 8 bits.

```
LDA   DAR,   MASK
```

Using mask in DAR, conditionally load control parameters.

```
LDA   CP0,   SR,           CND7
LDA   CP1,   SR,           CND6
LDA   CP2,   SR,           CND5
LDA   CP3,   SR,           CND4
LDA   CP4,   SR,           CND3
LDA   CP5,   SR,           CND2
LDA   CP6,   SR,           CND1
LDA   CP7,   SR,           CND0
```

Now, shift remaining 2 mask bits to the left and test. Prevent overflow by first clearing all but the remaining 2 bits.

```
AND   MASK, CP3,    R7
LDA   DAR,   MASK, L2
```

Finish transfer of last two values.

```
LDA   CP8,   SR,           CND1
LDA   CP9,   SR,           CND0
```

parts (b) and (c) show the two distribution programs. An output signal should be provided for either distribution method to externally synchronize data transfer to the 2920. Generation of such an output is not shown.

Many of the instructions listed in part (a) contain no arithmetic operation. These instructions might be combined with some other portion of the program that does not use any I/O field instructions. In this way, the number of instruction words used can be reduced. Both of these input routines require data at a continuous 8-kHz rate. A conventional single-chip microcomputer may be used to accept commands from a host computer at a lower rate and generate the data stream for the 2920's input.

Bear in mind that even though the 8-kHz data rate used here is high for a formant vocoder synthesis circuit, the use of a microprocessor allows a further reduction in the data rate. The software program presented here is only a first cut. Interpolation techniques can be applied between data sample sets and the 2920's program modified accordingly to make the rate reduction possible. □

8085 performs PSK modulation for data-line transmission

by F. B. Chawdhury and J. Das
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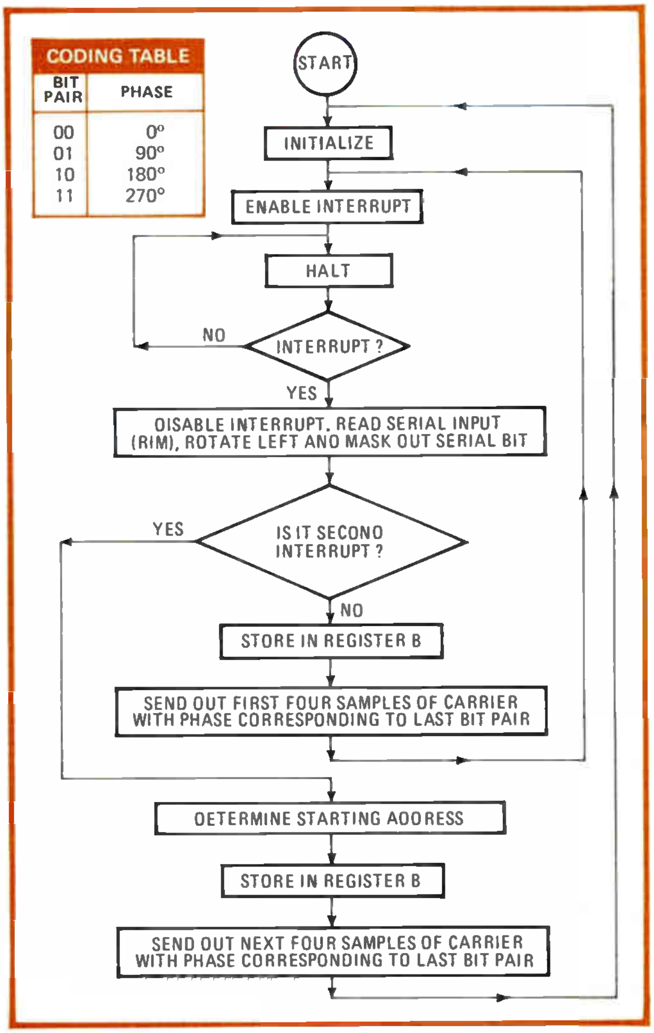
A reliable and flexible four-phase phase-shift–keyed modulator can be built using an Intel 8085 microprocessor. The quality of the modulation produced by this system is sufficient to send data over a voice-grade telephone channel.

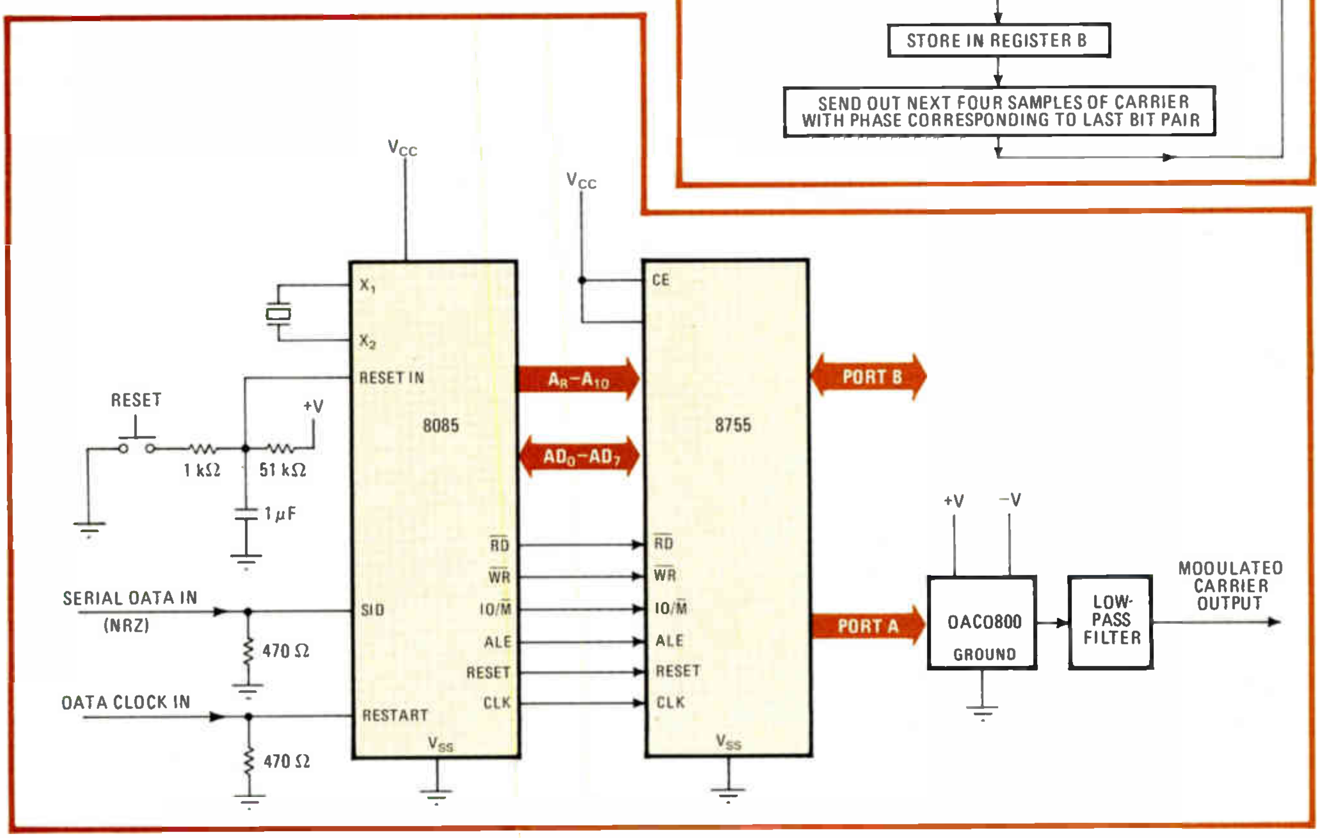
The modulation process has two steps. First, the nonreturn-to-zero input data stream used to modulate the carrier is sampled. In the second step, 8 bits corresponding to the sample value of the carrier are transmitted, their phase defined by a coding table.

Use of the 8085 makes it possible to build a modulator with minimum hardware. In this particular case, several peripheral-interface units can be eliminated. Only one

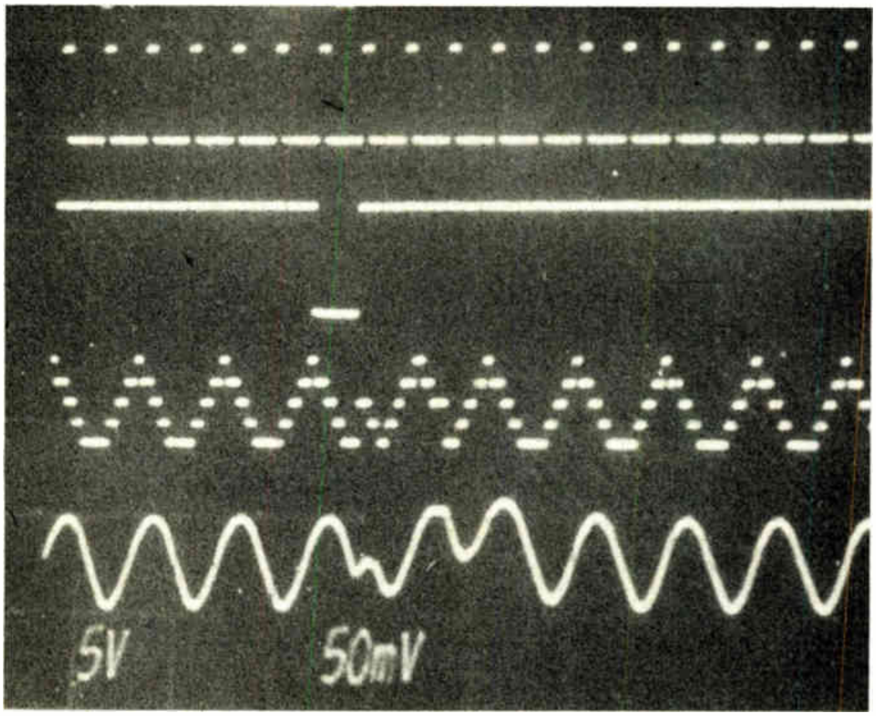


CODING TABLE

BIT PAIR	PHASE
00	0°
01	90°
10	180°
11	270°



1. Processor phasing. 8085 microprocessor needs little support circuitry to perform four-phase phase-shift–keyed modulation. Using only one interface chip, a d-a converter, and a filter, system executes a short program to produce a 2,400-baud PSK data stream of sufficient quality for telephone-line transmission.



2. Response. System pulses (top) clock in serial data (second trace) that is to modulate 2.4-kilohertz carrier signal. Digital-to-analog converter provides sampled-data output (third trace); the signal is suitable for transmission after passing through the low-pass filter (bottom).

support chip, the 8755, is needed. The 8755 is a 16-K erasable programmable read-only memory with two bidirectional input/output ports; it stores the modulation routine.

The software is designed to handle 4,800 bits per second, as the modulator operates at a 2,400-baud rate for a 2,400-hertz carrier signal. This is well within the capabilities of the 8085, which has a cycle time of 1.2 microseconds. The typical instruction will require two to four machine cycles.

The program begins with a sequence that sets up the coding table and the I/O-port direction and initializes the stack pointer and the interrupt-mask register (see flow chart). On receiving an interrupt, the processor reads the serial-input-data (SID) line by executing the read-interrupt-mask (RIM) instruction, and the data is latched at bit 7 of the accumulator. This data bit is then masked, rotated, and temporarily moved to register B of the 8085.

The 8085 now executes a data-output routine in which data obtained from the table is transmitted. The starting address is determined by the last bit pair received and is preserved in a working register. After sending out the 4 low-order bits corresponding to the carrier phase of the sample processed, the microprocessor waits for another interrupt.

On receiving the interrupt, the 8085 performs a similar operation on the sampled data. First, the data is rotated and logically ORed with the earlier data set stored in register B. This result is then added to 80 to yield the starting address of the table that stores the sample values. The microprocessor next executes the data output routine and sends out the 4 high-order bits of the sample before returning to the interrupt routine once again.

Thus 8-bit samples are continuously generated at port A. After digital-to-analog conversion and adequate low-pass filtering, the output becomes a PSK waveform. The filter's output is shown in the photograph (see bottom trace). □

Calculator notes

TI-59 solves fifth-order differential equations

by Andrzej Nafalski and Jan Guz
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The large memory of the TI-59 calculator, which enables storage of this 278-instruction program, and the use of Heun's numerical method (recognized as a second-order Runge-Kutta approximation) combine here to solve linear or nonlinear differential equations of up to the fifth order in a relatively short time. When given the differential function expressed as a set of state equations (Cauchy form):

TI-59 PROGRAM FOR HIGH-ORDER DIFFERENTIAL EQUATIONS

Locations	Keys
000 – 005	*LBL EE *A X RCL 13
006 – 011	= STO 03 INV if flg 1
012 – 017	STO *B' X RCL 13 =
018 – 022	STO 04 INV if flg 2
023 – 028	STO *C' X RCL 13 =
029 – 033	STO 05 INV if flg 3
034 – 039	STO *D' X RCL 13 =
040 – 044	STO 06 INV if flg 4
045 – 050	STO *E' X RCL 13 =
051 – 056	STO 07 LBL STO RCL 13
057 – 062	SUM 14 RCL 15 STO 08
063 – 068	+ RCL 03 = STO 15
069 – 074	INV if flg 1 SUM RCL 16
075 – 080	STO 09 + RCL 04 =
081 – 086	STO 16 INV if flg 2 SUM
087 – 091	RCL 17 STO 10 +
092 – 096	RCL 05 = STO 17
097 – 102	INV if flg 3 SUM RCL 18
103 – 108	STO 11 + RCL 06 =
109 – 113	STO 18 INV if flg 4
114 – 119	SUM RCL 19 STO 12 +
120 – 125	RCL 07 = STO 19 *LBL
126 – 131	SUM *A' X RCL 13 =
132 – 136	SUM 03 INV if flg 1
137 – 139	RCL *B' X

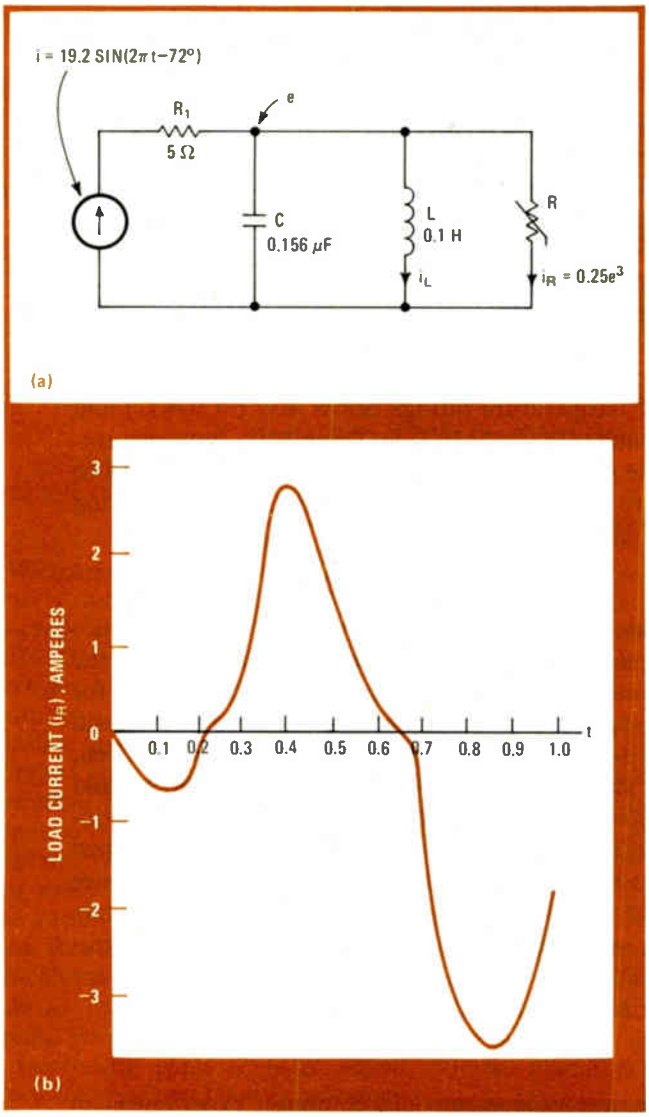
Locations	Keys
140 – 142	RCL 13 =
143 – 147	SUM 04 INV if flg 2
148 – 153	RCL *C' X RCL 13 =
154 – 158	SUM 05 INV if flg 3
159 – 164	RCL *D' X RCL 13 =
165 – 169	SUM 06 INV if flg 4
170 – 175	RCL *E' X RCL 13 =
176 – 181	SUM 07 *LBL RCL RCL
182 – 187	÷ 2 + RCL 08 =
188 – 193	STO 15 INV if flg 1 =
194 – 198	RCL 04 ÷ 2 +
199 – 204	RCL 09 = STO 16
205 – 210	if flg 2 = RCL 05 ÷
211 – 215	2 + RCL 10 =
216 – 221	STO 17 INV if flg 3 =
222 – 226	RCL 06 ÷ 2 +
227 – 232	RCL 11 = STO 18 INV
233 – 238	if flg 4 = RCL 07 ÷
239 – 243	2 + RCL 12 =
244 – 249	STO 19 *LBL = dsz 1
250 – 255	EE RCL 14 R/S GTO EE
256 – 260	*LBL A (CE –
261 – 266	x ≷ t 1) STO 02 *LBL
267 – 272	st flg st flg IND 02 dsz 2
273 – 277	st flg x ≷ t R/S GTO EE

Instructions

- Key in program
- Enter state equations corresponding to the nth-order differential equation, beginning at location 278
- Clear all data memories
  Press *CMs
- Enter initial conditions, incremental value of time for which equations step to determine new values
  (t), STO 14, (x_{10}), STO 15, (x_{20}), STO 16, (x_{30}), STO 17, (x_{40}), STO 18, (x_{50}), STO 19, (h), STO 13
- Initialize the program
  (N), A
  The program will display N, the number of state equations representing the nth-order differential equation
- Press R/S to execute program
  The state equations will be evaluated for a given t_i. The values of each x_i variable, as well as all desired circuit variables, may be displayed by addressing their appropriate register or user-defined memory location (user key).
- Press R/S as required to update variables
  If m has been entered into register R_1, the calculation will proceed through the execution of m steps before the program is halted

Keys
A initialize
A'1st equation
B'2nd equation
C'3rd equation
D'4th equation
E'5th equation

Registers	
R_1	m
R_2	N
R_3-R_{12}	in use
R_{13}	h
R_{14}	t_i
R_{15}	x_{1i}
R_{16}	x_{2i}
R_{17}	x_{3i}
R_{18}	x_{4i}
R_{19}	x_{5i}



Stated solution. TI-59 solves differential equations of up to the fifth order, either linear or nonlinear, in order to find any branch current or voltage. When supplied with state equations of typical network, program provides point-by-point plot of the desired variable.

$$dx_i/dt = f_i(t_1 x_1, x_2 \ . \ . \ . \ x_i) \qquad (1)$$

where i_{max} corresponds to the order of the equation and f_i is an algebraic collection of terms, the program yields a point-to-point solution of any desired circuit variable with an accuracy sufficient for all but the most demanding applications.

The algorithm utilized is:

$$x(t_o + h) = x(t_o) + \frac{1}{2}\{h\, f[x(t_o), t_o] + h\, f[x(t_o) + f_a(t_o + h)]\} \qquad (2)$$

where $f_a = h\, f[x(t_o), t_o]$, t_o is the initial time at which the function x is defined, and h is the increment that t is stepped to so that $x(t_o + h)$ can be evaluated. Equation 2 is stepped from t_o to t_m, where $t_m = t_o + mh$ and m is the required number of plotted points. Note that with Heun's method only the initial conditions are required to evaluate t_i; a knowledge of t_{i-1} is not needed.

NONLINEAR NETWORK PROGRAMMING	
Locations	Keys
278 – 283	*LBL *A' (10 X
284 – 289	RCL 16) INV SBR *LBL *B'
290 – 295	RAD (((2 X
296 – 300	π X RCL 14 −
301 – 306	1.26) SIN
307 – 312	X 3.84 +
313 – 317	(RCL 16 x² ÷
318 – 323	4 + .2) X
324 – 329	RCL 16 + / − − RCL 15
330 – 336	) X 6.41)
337 – 342	INV SBR *LBL B (RCL 16
343 – 347	x² X RCL 16 X
348 – 354	.25) R/S GTO EE

As an example of the program's usefulness, consider the simple second-order circuit shown in the figure. Load resistor R has a known nonlinear voltage-current characteristic of $i = 0.25e^3$. Finding i_R, however, is normally a very tedious procedure in circuits of this nature, and a quick method of solution is desirable.

The required state equations are first written:

$$di_L/dt = e/L \qquad (3)$$
$$de/dt = -i_L/C - e/(CR_1) - e/(CR_n) + i/(CR_1) \qquad (4)$$

where $x_1 = i_L$, $x_2 = e$, and $R_n = e/i_R = e/0.25e^3$. Substituting for L, R, and C and simplifying where necessary results in:

$$di_L/dt = 10e \qquad (5)$$
$$de/dt = [\{\sin(2\pi t - 1.26)3.84 - (e^2/4 + 0.2)e - i_L\}6.41] \qquad (6)$$

The right side of Eqs. 5 and 6 are now entered into the memory at location 278, following the main program (see programming box). Note that each equation is separated by an appropriate label (A′ for x_1, B′ for x_2, etc.) and partitioned by the instruction INV SBR. The desired variable to be monitored (in this case, i_R) is retrieved by calling out $i_R = 0.25e^3$ starting at location 338.

Initializing the calculation with $t_0 = 0$, $h = 0.02$, and x_{10} to $x_{50} = 0$ as per the program instructions and executing the routine yields the curve as shown in the figure. Calculation time for each point is approximately 14 seconds. Current i_R is found by addressing label B after each program halt. Displayed initially after each halt is the time, t, that corresponds to that current. The value of all other variables are found in their assigned registers A′ to E′.

If the value of a particular variable is required for only one specific time, the calculation can be made to proceed through the execution of m steps before a program halt by entering the number m in register 1. The program will step in increments of h thereafter. ☐

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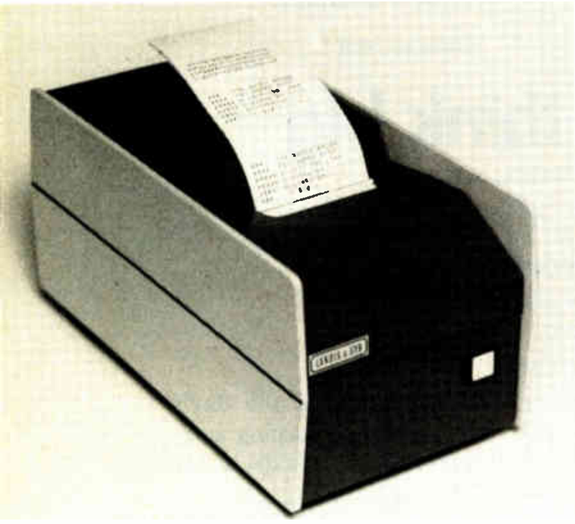


Convenient. The 21-column model 0533 from Sodeco has a snap-in ribbon cartridge. It prints line segments from a drum—what Sodeco calls bar-matrix impact printing.

Corp.'s 80-column nonimpact printers sells for under $600, and Computer Printers International Inc. (Comprint) is now offering an optional interface that will make its 80-column model 912 compatible with most home and small-business computers.

The competition with 80-column printers for the home computer market does not scare Ernie Campbell, director of marketing at MPI in Salt Lake City, Utah, who sees a bright future for small printers. "There will always be a need for 40-column printers for instrumentation, testing, and production," he says. Although MPI has been pushing more and more into the 80-column market, its commitment to the low-cost 40-column variety is apparent in its intention to introduce one in the $380 range this year.

As if in agreement with MPI, most of the manufacturers of the new small printers featured here did not restrict their product to the personal computer marketplace. The focus is on instrumentation, as it has been for several years. Even those companies such as LRC and Interface Electronics that have aimed at the small computer are enjoying good business in instrumentation applications.

Major printer manufacturers like Anadex Inc., Axiom Corp., Centronics, and MPI have all had under-40-column stand-alones for a while and some are adding more models: Datel/Intersil recently expanded its printer' line to include a panel-mounted thermal printer of 20-column width [*Electronics*, Oct. 25, 1979, p. 317], and United Systems Corp., also known as Digitec, has a new stand-alone [*Electronics*, Jan. 3, p. 218].

Newcomers. Coming on the market now are the following:

- The LRC model 7000+ is a 40-column dot-matrix impact printer that sells for $389. The stand-alone unit prints 1.25 lines/s unidirectionally. Although the unit is designed for small business and home computer systems, the manufacturer says that the housing for the printer will withstand an industrial environment. It is 6.5 in. in height by 10 in. in width by 12.5 in. in depth.

The interfaces of the 7000+ include TRS-80 and Apple parallel, RS-232-C, IEEE-488, and current loop, so it can be readily interfaced to any home computer or instrument system. The 7000+ accepts the full ASCII character set and can print in both a single- and double-width font. Among the options available are a 120-character buffer and a version that prints 64, 40, 32, or 20 characters per line, selectable under software control.

- Model 0533 from Sodeco Industrial Products division of Landis & Gyr Inc., prints 21 columns of alphanumeric information using the company's bar-matrix, impact-print mechanism. The bar-matrix impact printer is like a drum printer, but instead of having complete characters on the drum, it has line segments that are put together to construct individual characters. A snap-in ribbon cartridge permits easy ribbon replacement.

The stand-alone unit measures 13.5 by 1.5 by 6.9 in. and contains a power supply and an ASCII-compatible interface controller to perform all printer functions. Printing at 90 lines per minute (approximately 1.5 lines/s), the unit also slews paper up to 10 lines/s. The unit sells for $495 in single-piece quantities, but discounts for original-equipment manufacturers are available. Delivery is 8 to 10 weeks.

- From Durant Digital Instruments comes the Century System 6070 printer, which the company says has been built to industrial specifications for long life in rugged environments. The 32-column stand-alone unit prints the standard 64-character ASCII set. Logic-controlled printing produces the characters within a five-by-seven-dot matrix, averaging 40 characters/s—about 1.25 lines/s. The unit prints on conventional

Fast. Interface Electronic's Model 100 dot-matrix impact printer puts out 27 columns per line at 2.4 lines/s. It contains a C. Itoh/Epson model 210 printing mechanism.

Rugged. The Century System 6070 32-column printer has been built by Durant Digital Instruments to industrial specifications. The printer also self-tests.

adding-machine paper.

The 6070 features serial asynchronous interfaces compatible with either the teletypewriter or EIA RS-232-C standards offered by most computer manufacturers. It also provides parallel 7-bit ASCII and binary-coded decimal interfaces. The serial interfaces can sustain a continuous 300-baud data rate. The printer has a self-test print capability to test basic logic, electrical, and mechanical functions.

The list price of the 6-by-10.5-by-14-in. printer is $645, with quantity discounts available. The unit is available for immediate shipment from stock.

■ The dot-matrix impact printer model number 100 from CCC's Interface Electronics division prints 27 columns per line at 2.4 lines/s. The stand-alone unit incorporates a C. Itoh/Epson model 210 printer, a microprocessor-based single-board printer controller, and a modular power supply. It measures 6 by 6.5 by 11 in. The model 100 can print the 96-character ASCII upper- and lower-case set under software control, in either black or red.

The parallel input is TTL/Centronics-compatible, and the serial input accepts 20-mA current loop or RS-232-C signals at selectable rates of 110 to 9,600 bauds. The printer sells for $545. Delivery is from stock.

■ Rank Numbering Machines Inc. is introducing to the U. S. an electrosensitive matrix printer made by English Numbering Machines Ltd. that can operate on a 12-V dc battery supply, making the printer suitable for mobile applications. The 4.2-by-8.2-by-8.4-in. unit prints 40 columns per line at 1.3 lines/s. Since it has options for other printing fonts, the speed varies according to what column width is specified, but the printing rate usually approximates 80 full lines/min. The ESP40 printer produces the 96-character ASCII set, generating a nine-by-five-dot matrix.

Portable. The ESP40 is an electrosensitive dot-matrix printer just introduced into the U. S. by Rank Numbering Machines Inc. The unit operates on a 12-V dc supply.

The unit's interface is bit-parallel character serial, and it has serial inputs available to suit both RS-232 and current-loop connection. Besides being used with a battery, the unit can be optionally supplied with an integral transformer for direct connection to a 100-to-200-V or 210-to-250-V supply. Other options include a self-test unit and a keyboard input port. The ESP40 printer sells for $500 a unit in lots of 100; the housing is extra.

■ The SP308 ticket printer from Syntest Corp. prints on flat stock—such as credit-card receipts and automatic-testing forms. The dot-matrix impact unit prints 1.5 lines/s using the ASCII character set, printing 40 characters per line. The printer has RS-232 or 20-mA loop interfaces or a parallel interface. The 11.75-by-7.25-by-9.25-in. device runs on 115 or 230 V at 50 or 60 Hz. It hooks up to a microcomputer or to a point-of-sale terminal. The SP308 sells for $678 each in quantities of one to nine printers. It is available from stock within 30 days.

LRC, Eaton Corp., Technical Research Park, Riverton, Wyo. 82501. Phone Daniel Mitchell at (307) 856-4821 [341]

Sodeco Div. of Landis & Gyr Inc., 4 Westchester Plaza, Elmsford, N. J. 10523. Phone R. M. Banzaca at (914) 592-4400 [342]

Durant Digital Instruments, Eaton Corp., 901 South 12th St., Watertown, Wis. 53094. Phone Thomas Ackerman at (414) 261-4070 [343]

Interface Electronics Division of Capitol Circuits Corp., 24 Denby Rd., Allston, Mass. 02134. Phone Dick Hubbell at (617) 787-2030 [344]

Rank Numbering Machines Inc., 411 East Jarvis Ave., Des Plaines, Ill. 60018. Phone J. M. Campbell at (312) 297-7720 [345]

Syntest Corp., 169G Millham St., Marlboro, Mass. 01752. Phone (617) 481-7827 [346]

14-bit s-d converter gets smaller

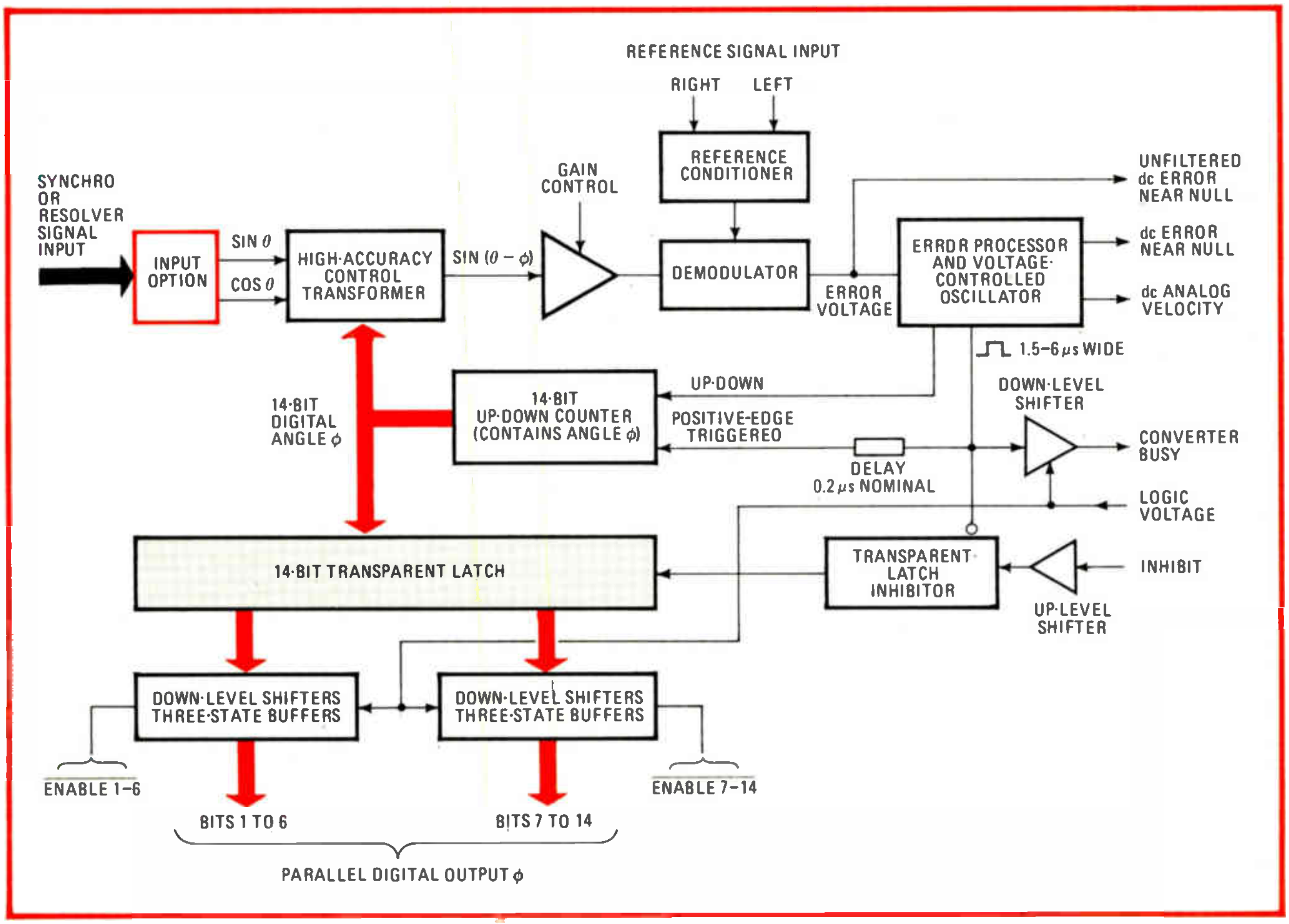
Synchro-to-digital converter uses two custom LSI chips and four standard ICs in a double-width dual in-line package to miniaturize hybrid design

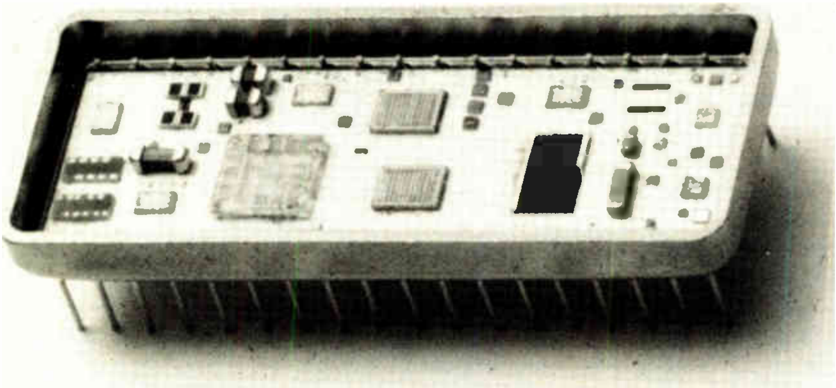
by Pamela Hamilton, New York bureau manager

Making smaller converters for the synchro/resolver-to-digital marketplace is ILC Data Device Corp.'s latest engineering direction. Already a major supplier of high performance hybrid s/r-d converters, the company is branching out with a 14-bit s/r-d converter housed in a single, 36-pin double-width dual in-line package [*Electronics*, Dec. 6, 1979, p. 36]. Processed to MIL STD 883, the 8915 promises to be most useful in places where environmental conditions are harsh.

Monolithic design. Key to the size and performance of the 8915 are two custom-designed monolithic circuits, which greatly reduce the parts count in the hybrid package. The complementary-MOS LSI chips were designed in house at DDC and are the beginnings of a Monobrid series of s-d, d-s, analog-to-digital, and digital-to-analog converters the company hopes to introduce in the upcoming months. "We're designing the kind of chips we can't buy," says Stephen A. Muth, director of marketing. The hybrid circuit also uses four standard chips as well as several thin-film resistor networks.

The 8915 is available with a maximum error of ±4 minutes, ±0.9 least significant bit (equivalent to ±4 LSB in 14 bits), or ±2.6 minutes (±2 LSB in 14 bits). This inaccuracy includes the quantizing error and is maintained under static and dynamic conditions at speeds of up to





±2 revolutions/second. The converter will accept broadband inputs of either 360 to 1,000 Hz (400 Hz nominal) or 47 to 1,000 Hz (60 Hz nominal). The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric.

The digital output of the converter is through a transparent latch that allows the converter to keep tracking while an inhibit command is being applied. The three-state output is in 2 words, one 8-bit and the other 6-bit. "The latches and three-state outputs have been designed into the custom chips," notes Seymour S. Lanton, R&D manager for synchro conversion products. "It's flexible as to how the digital interface is configured." The output angle is in natural binary code, with parallel positive logic. The output is compatible with diode transistor logic, TTL, and complementary MOS. Analog outputs include angular velocity and also error voltages.

Low power. A single +15-V power supply is all that is required for the converter, and the voltage may vary from +11 to 16.5V with no degradation in performance. All logic inputs and outputs are buffered to handle any external TTL or C-MOS signals between ±4.5 V and the +15-V supply level. Lanton also notes that the converter's reliability has been greatly enhanced over earlier models. "It's about 4½ times more reliable than the [two-package] HSDC 14 that it's replacing," he says. The 8915 also consumes less power—about 0.5 W vs the 0.75 to 1 W other models needed—which will open up new applications for synchro converters, speculates Lanton.

Among those applications are satellites, where low power is essential. "Another application is in oil drilling," notes Lanton, "where the farther down you go, the hotter it gets." More mundane applications might include bus multiplexing and areas where an interface between synchros and microprocessors is required. The 8915 is also well suited for harsh industrial, military, and avionics environments.

Operating between −55° and +125° C, the 8915 has no lag error for speeds up to 2 rps. For a 179° step change at 400 Hz, the settling time is 200 ms typically to 1 LSB, or 250 ms maximum to final value. At 60 Hz, with a 179° step change, the converter has a settling time of 350 ms typically to 1 LSB and 400 ms maximum to final value.

Lanton also notes that the 8915 has a maximum differential nonlinearity of 1 LSB, making it monotonic. The converter is also jitter-free. The company has a patented algorithm for the control-transformer circuitry used in the converter, which also contributes to the accuracy of the output; the total algorithmic error is 0.03 s.

The 8915 will sell for about $450 is single quantities with delivery from stock to six weeks.

ILC Data Device Corp., Airport International Plaza, Bohemia, N. Y., 11716. Phone Ken Baker at (516) 567-5600 [339]

Computers & peripherals

32-bit computer aimed at OEMs

OEM and end-user versions use microcode and have 80-ns bipolar cache memories

Although they exist, 32-bit computers for the original-equipment manufacturer are rare. Feeling that there was more than enough room in the world for another entry, especially one with a low price-performance ratio, Prime Computer Inc. has introduced its model 150—a 50-series machine with such throughput-boosting features as extensive use of microcode and a high-speed cache memory. At the same time, the Wellesley Hills, Mass., firm is announcing a new computer aimed at end users—the model 250.

Architecturally, both machines are similar to Prime's flagship model, the 750. Common characteristics include hardware-stack-oriented organization and the throughput-boosting features mentioned earlier. The 50 series also includes relatively large error-correcting MOS main memory; segmented and paged virtual-memory management; hardware-controlled memory protection; the Primos embedded time-sharing operating system; firmware-resident business and floating-point instruction sets; multichannel direct memory access, control, and transfer; and burst mode input/output capability with data rates to 8 megabits per second in some machines.

Within this description, the 150 has a basic 256-kilobyte main memory, an 80-ns bipolar cache, a virtual control panel with remote diagnostics capability, a 32-megabyte Winchester disk system, and an eight-line asynchronous controller.

Five units is the minimum order Prime will accept on the 150, according to Russell C. Planitzer, vice president for marketing development. In small lots, he says, the 150 goes for $49,000. But Planitzer adds that "aggressive discounting" brings this price well down well below $40,000 at a 25-unit-per-year order rate.

Planitzer says that the 150 is aimed at mainframe-oriented customers with evolved software capabilities who want to develop and implement dedicated or distributed processing systems, but with the ante raised to 32 bits. Prime's approach to this market, he says, is not simply to make longer words and larger memories available to OEMs, but to emphasize upgradable hardware as well. Prime's market research tells it that more than 50% of systems builders upgrade their systems within two years by going to more capable mainframes. This makes software compatibility within a product line a major plus, he feels, noting that all other machines in the 50 series—six of them at present—are software-compatible. Thus, programs for smaller machines like the 150 and 250 are subsets of programs used on the Prime 750, a machine now competing in the market with Digital Equipment Corp.'s VAX-11/780.

So Prime's strategy is to cut the entry price to its line, according to Planitzer, and to reap the benefits of the upgrading trend. For some, it will not even be necessary to buy a new mainframe to upgrade; users of the 150 will be able to boost computer power to that of the model 450 through a central-processing-unit board swap. While this will cost roughly $20,000, it should be a bargain as the 150 is only about 60% as powerful as the 450.

Prime had formerly tried to address the OEM sector with the more powerful, more costly 450, but found it was selling into other markets. Still, says Planitzer, experience with the 450 showed Prime that there was more to the OEM market than price; "communications and networking capabilities, good implementation languages, indexed sequential file management, and query language software were frequent necessities for systems builders." Plantizer says that the 150 offers all that, plus software compatibility, and at a price which brings it into competition with less powerful 16-bit minicomputers.

The 250 is end-user-oriented. Like the 150, it can run 32-megabyte programs; it also can support up to 16 users simultaneously through its embedded Primos operating system. The smallest 250 has a 512-kilobyte main memory, Primos, floating-point and business firmware, 2 kilobytes of 80-ns cache, virtual control panel, 32-megabyte Winchester disk, CRT terminal, and eight-line asynchronous controller.

Priced at $59,500 and up, the 250 is specifically aimed at two user classes: first, network customers that want highly capable nodes of preprocessors, but at relatively low cost; second, the small-company end of Prime's traditional market, the technically sophisticated end user. Planitzer figures that the 250 has just about the right price-performance ratio to attract companies that are computer-bound with available 16-bit machines, but which find it hard to justify the outlay needed for a typical, large mainframe.

Most of the advantages claimed for the 150 apply to the 250, he says, including software compatibility, and upgradability. Prime will also offer a CPU board swap for the 250, upgrading it to the level of the 40%-more-powerful 550.

Prime supports all its 50-series computers with software like the Primnet communications and networking system. Primnet is compatible with a variety of protocols including X.25, CDC 200UT, Univac 1004, ICL 7020, and IBM Bisync for HASP and 2780. There also are the more typical offerings such as Fortran and Cobol packages; plus, Planitzer adds, any user-developed program for one 50-series machine operates on any other with the necessary memory and peripherals.

Deliveries of the 150 and 250 will begin in June.

Prime Computer Inc., 40 Walnut St., Wellesley Hills, Mass., 02181. Phone: (617) 879-2960 [361]

96-track/in. floppy-disk drives store 480 kilobytes

Two floppy-disk drives that read or write 96 tracks/in. can store 480 kilobytes on each side of a 5.25-in. disk and have a track-to-track access time of 5 ms. The model 91 is a single-sided disk drive, and the model 92 is double-sided. The drives have a proprietary split-band head-positioning device that is driven directly by a stepper motor. The head assembly for the model 92 consists of a fixed bottom head with a gimbaled top head.

Both drives have an automatic disk positioning and ejector mechanism to preposition the disk over a spindle hub before the clutch-centering device is engaged. The mechanism also partially ejects the disk for easy removal when the door is opened. The drives accommodate frequency-modulation, modified fm, and modified mfm encoding. Prices of single units for evaluation by original-equipment manufacturers will be $450 for the model 91 and $550 for the 92.

Micro Peripherals Inc., 9754 Deering Ave., Chatsworth, Calif. 91311. Phone (213) 709-4202 [363]

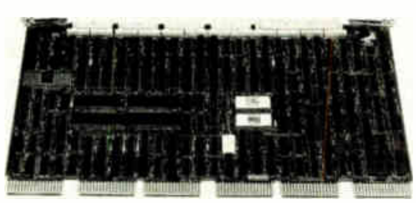
SMD controller is compatible with PDP-11

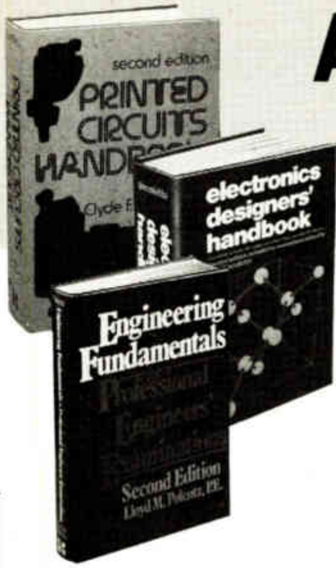
Dataram Corp.'s S33/A is a single-board controller that is software-compatible with storage-module drives used with Digital Equipment Corp.'s PDP-11 minicomputers. The S33/A is completely software-compatible with DEC's RM02 input/output drives, so it can operate with DEC's RSTS/E and RSX11-M operating systems and RM02 diagnostics. The microprocessor-based unit will also operate with Control Data Corp.'s 9762 SMD drive and other such drives like those from Ampex, Ball, and Century Data Systems. It also offers media compatibility with the RM02 storage-module drive supplied by DEC.

The S33/A can drive up to four 80-megabyte SMDs to provide a maximum storage capacity of 320 megabytes, unformatted. Internal self-test is a standard feature. A 2-kilobyte (four-sector) bipolar buffer eliminates data-late errors. The S33/A has a 32-bit error-correction code for data, so a single 11-bit error burst can be corrected. It also has a 16-bit cyclic redundancy checking for header error detection.

In single quantities, the S33/A is $4,900. Delivery is 30 days after the receipt of an order. The unit has a one-year warranty.

Dataram Corp., Princeton-Hightstown Road, Cranbury, N. J. 08512. Phone John Gilligan at (609) 799-0071 [365]





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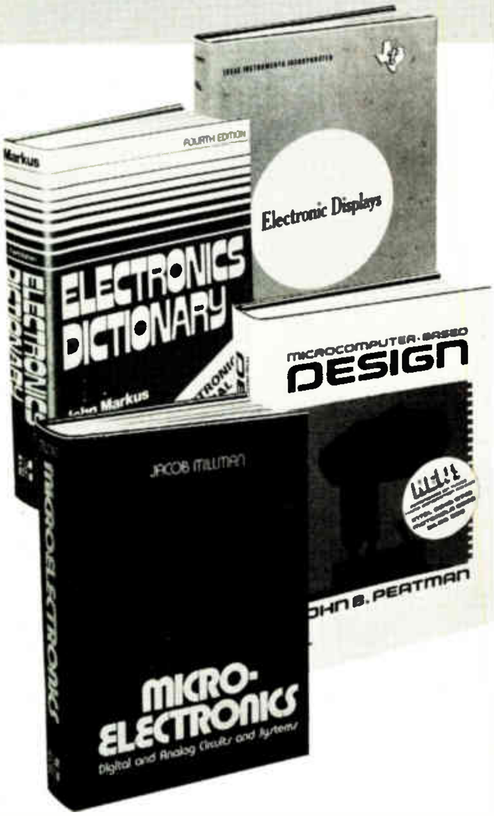

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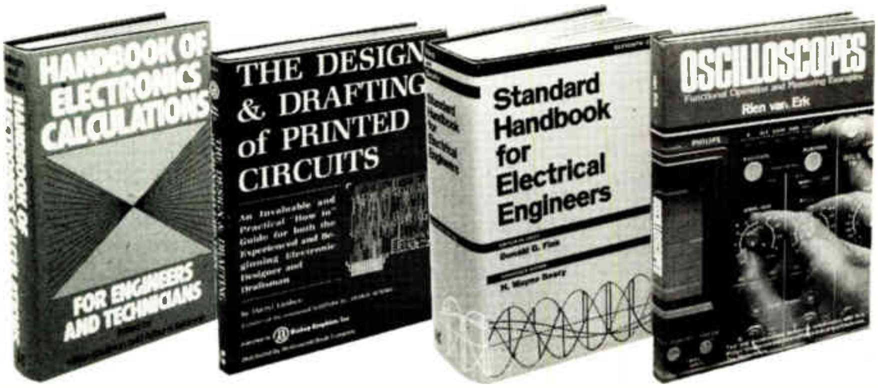

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New products

Data acquisition

Small converter has big specs

Fast 16-bit d-a unit fits in a DIP, yet offers true 16-bit linearity

Although there are more than a dozen 16-bit digital-to-analog converters on the market, not all of them provide true 16-bit performance. The ones that do have full 16-bit linearity tend to be the bulky board or module types, which are costly and power-demanding as well as large. Typically, the converters available in dual in-line packages have no better than 14-bit linearity.

Now Hybrid Systems Inc. is attempting to change the picture with its 9331-16—a two-chip hybrid device in a double-width 24-pin DIP. This d-a converter is guaranteed linear to within half a least-significant bit (0.008% of full scale), consumes a maximum of 50 mw (typically 20 to 30 mW), settles to within ½ LSB in 1μs, and sells for $99 each in lots of 100 or more ($169 in small quantities).

Graceful interfacing. Input storage registers in selectable 8- or 16-bit segments allow the 9331-16 to interface gracefully with most microprocessors. Also, it is compatible with complementary-MOS circuitry operating from 5 to 15 V dc and works with TTL and DTL as well.

Although part of the unit's low power consumption is due to its C-MOS design, part comes from its lack of an on-board reference and an output op amp. The current-output converter requires either a +10-V or a −10-V reference supply and, for voltage-output applications, an operational amplifier. Over its 0°-to-70°C operating range, both its temperature coefficient of gain and its nonlinearity tempco are 1 ppm/°C.

There are two primary reasons for the 9331-16's attractive price-performance ratio, according to G. James Estep, Hybrid's director of advanced development. First, he explains, it is built around a custom monolithic chip, which includes the storage registers and the switch set. Second, it uses an extremely rugged but inexpensive package made of glass-filled epoxy.

The chip will not be used only for the 9331-16, so its development cost can be spread over a number of products, lowering the unit cost. The circuit can be configured to contain 4 to 16 decoders, 18 exclusive-OR gates, 29 latches, 29 drivers, 29 dual FET switches, and a variety of other circuits. Its 65-pad pinout gives an idea of its complexity. For the present application, the chip is overdesigned; according to Estep, its specifications suit it to 18-bit applications.

The plastic package is claimed to withstand environmental extremes usually associated with military-type hermetic housings, but at much lower cost. Hybrid is patenting the package. Meanwhile, Hybrid engineers are loading various circuits into the package and cooking them in a pressure cooker. Almost all of the circuits last two hours, says Estep, and most of them manage to last four [*Electronics*, Sept. 27, 1979, p. 168].

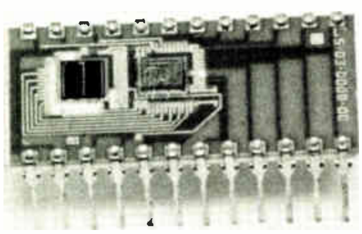
The 9331-16 has both two- and four-quadrant multiplier capability, making it suitable for precision synchro applications as well as use in medical electronics, sonobuoys, radiosondes, and other power-sensitive areas.

Delivery time for the converter is stock to two weeks.

Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 01730. Phone (617) 275-1570 [381]

Scott T transformer is less than 0.3 in. high

A Scott T transformer for converting synchro signals into resolver signals to be used in synchro to digital conversion has a maximum height of 0.3 in. The low profile of the model 13530 is comparable to that of other printed-circuit board components, making close board-to-board spacing possible. The total size of the 13530 is 0.63 by 1.25 by 0.3 in. With a three-wire synchronous input of 11.8 V rms, 400 Hz, the unit will provide an output of 1 V rms sine and 1 V



rms cosine. Accuracy is to within 1 arc minute. The unit operates over the full temperature range of −55° to +125°C. The manufacturer says that since toroidal construction is used, interference and pickup are minimized.

The 13530 is priced at $27 apiece in 1,000-unit quantities. Delivery is 12 weeks, but samples can be delivered in two to four weeks for evaluation reports and customer drawings.

Magnetico Inc., 182 Morris Ave., Holtsville, N.Y. 11742. Phone Harold G. Eicher at (516) 654-1166 [383]

12-bit integrating a-d board is LSI-11, -11/2–compatible

A 12-bit integrating analog-to-digital converter that is compatible with Digital Equipment Corp.'s LSI-11, LSI-11/2, and PDP-11/03/23 series of microcomputers gives a common-mode rejection of 126 dB and handles common-mode voltages of up to 250 V rms. This board—the model ST-LSI-RLY—has an overall system throughput time of 36 ms, sample to sample (28 samples/s). The low speed is especially useful in industrial environments, where low voltages from sensors have to be carefully sought lest they be obscured by high-voltage common-mode noise.

Analog input signals ranging from ±10 mV to ±1.0 V or 10 mV to 2.0 V full-scale are processed by a programmable-gain amplifier. A diagnostic program on paper tape checks out system performance. A-d conversion is accomplished by the company's 12-bit ADC-EK12, a complementary-MOS integrated circuit. The programmable-gain amplifier, whose circuit is autozeroed, is controlled by a 2-bit program word for gains of 1, 2, 5, and 10 times.

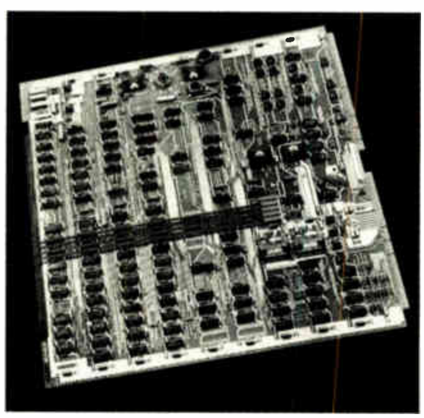
The ST-LSI-RLY board fits DEC's half quad spacing. Operating temperature is from 0° to 70°C, and power requirements are +5 V dc at 1.5 A maximum; +12 V dc ±5% at 70 mA maximum. The boards sell for $695 apiece and are available four to eight weeks after an order is received. Large-quantity discounts are available.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone Ted Petit at (617) 339-9341 [384]

Sensor input/output subsystem sells for $2,000

A $2,000 analog signal converter complements Data General Corp.'s Nova and Eclipse computers and controls laboratory and industrial processes. The Analog Data Subsystem (ADS) is a 15-in. board with 32 single-ended or 16 differential analog inputs, two analog outputs, and a Z-pulse for oscilloscope control. Data transfers through each of the two independent interfaces can be made with either programmed input/output or data channel (direct memory access). The resolution is 12 bits in four different voltage ranges, and analog-to-digital throughput is 22 kHz.

Software support is provided by a Sensor Access Manager (SAM), which runs under the company's own real-time disk operating system (RDOS). SAM allows sensor input/output applications to be programmed in the Fortran IV, Fortran



5, and Assembler languages with a minimum effort.

The subsystem may be delivered 90 days after the receipt of an order, and discounts for large-quantity purchases are available.

Data General Corp., Rte. 9, Westboro, Mass. 01581. Phone (617) 366-8911 [388]

Industrial

A-d converters sample for $299

Fully integrated 14- and 15-bit analog-to-digital converters include a sample-and-hold unit

Until the introduction of Analogic Corp.'s ADAM-824 and ADAM-825 14- and 15-bit sampling analog-to-digital converters, designers had essentially two choices: buying inexpensive sampling a-d converters with accompanying low performance levels or paying premium prices for high-performance units that more than likely had features that were too fancy for the application intended. Now, thanks to Analogic's new units, the designer's choice is wider, as the ADAM-824 and -825 are optimized for performance at moderate frequency ranges, yet are low in price.

Each 2-by-4-by-0.44-in. module combines an a-d converter with a sample-and-hold amplifier, eliminating interface problems that frequently arise when separate converters and sample-and-hold amplifiers are integrated.

The performance of each unit is impressive, considering the low price of $299 each in single quantities. Each sampling a-d converter features a 20-kHz throughput rate that includes both sampling and conversion time, a maximum differential nonlinearity of ±0.002% of full scale (±0.003% for the ADAM-824) at 25°C, and a low differential nonlinearity temperature coefficient of ±0.002 ppm/°C of full scale (±0.003% for the ADAM-824). Each unit contains a programmable-gain amplifier and bus-controllable three-state outputs with latched registers.

High performance is ensured by a low, ±3 σ noise specification of 50 μV for the a-d converter (75 μV for both the converter and the sample-and-hold amplifier). Each unit is guaranteed to be monotonic and includes all of the signal-conditioning and support circuitry needed for operation. These include a precision reference supply, a trimming potentiometer, bypass capacitors, and timing circuitry. A single start pulse is all that is required to control the entire data-acquisition and -conversion process.

Each of the sampling converters dissipates approximately 1 W of power and requires ±15- and +5-V supply lines for operation. Pin-programmable input ranges of 0 to 5, 0 to 10, ±5, and ±10 V are available. The input impedance is 100 MΩ in parallel with 5 pF. A choice of digital outputs includes unipolar binary, offset binary, and 2's complement.

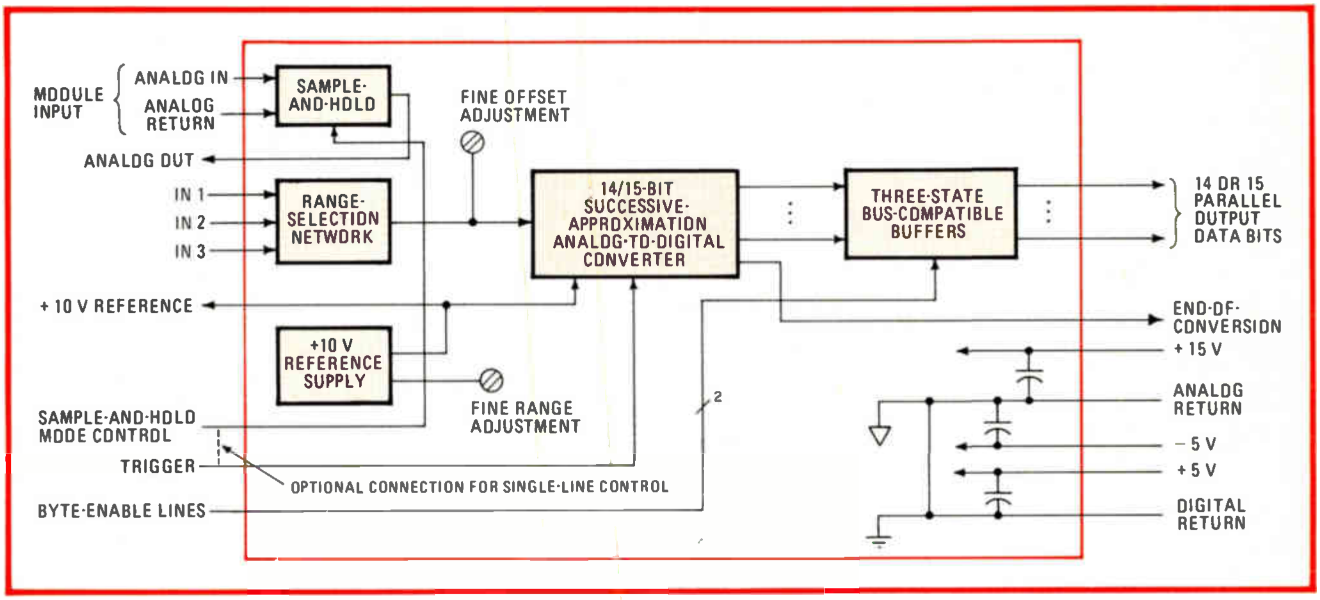
Additional specifications include an input bias current of 1 nA maximum (at 25°C), calibrated absolute accuracy within ±0.006% of full scale (traceable to the National Bureau of Standards), quantizing error of ±½ least significant bit, and a gain temperature coefficient of ±8 ppm/°C. The sample-and-hold aperture delay time is 50 nanoseconds, and the aperture uncertainty time is ±1 ns.

Feedthrough rejection is −90 dB (measured with a 20-V peak-to-peak 10-kHz sine wave across the input terminals). The droop rate for the sample-and-hold amplifier is 0.2 μV/μs (at 25°C). Power-supply sensitivity is ±0.001% for every 1% change in the supply voltage.

The ADAM-824 and -825 are designed for operation from 0° to 70°C and are electrostatically shielded against electromagnetic interference.

Applications include precision data-acquisition systems, automatic test equipment, portable seismic instrumentation, materials testing, and process control. Availability is from stock, so the sampling converters can be delivered in two weeks.

Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617) 246-0300 [371]



0.2-in.² accelerometer has 7-mV/g sensitivity

The model 811A Picotron miniature accelerometer measures 0.2 in.² and weighs less than 0.5 gram. The unit has a flat upper frequency response of 25 kHz at the +5% point and a sensitivity of 7 mV/standard gravity. This output from such a small package makes the Picotron useful where small size and weight and high resolution and frequency response are important. Patented low-impedance integrated circuits should eliminate the need for special low-noise cables, the maker says. The unit's temperature range extends from −195° to +135°C.

The Picotron 811A sells for $410 each. Delivery is made from stock or takes four weeks.

Kistler Instrument Corp., 75 John Glenn Dr., Amherst, N.Y. 14120. Phone Ronald F. Lochocki at (716) 691-5100 [356]

Power-factor motor control is based on semiconductors

The ES-1 line of power controllers for industrial single-phase ac induction motors uses semiconductor technology to reduce voltage whenever the motor is operating at less than full load. The voltage is cut to maintain the motor's rated speed, at the same time reducing power consumption and therefore operating costs. Actual savings depend upon the motor's design, the power requirements of the application, operational on-time compared with load time, and the cost of electrical energy. However, the maker reports typical savings of 25% to 45% for motors that are oversized or operate lightly loaded.

Six models of the ES-1 are offered for direct wiring with 120- and 240-V single-phase motors. They cover a power range of 0.33 to 3.0 hp and 7.5 to 20 A. Motors do not need to be modified. The 4-by-6-by-4-in. units have a cast-aluminum wall-mountable enclosure.

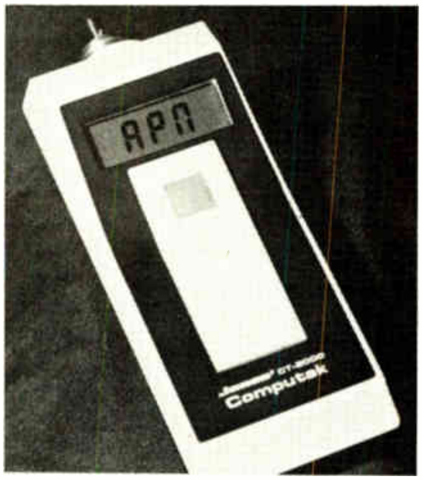
Options include an integral cord set for direct wall receptacle use and a pilot light that indicates voltage variations. List prices range from $127 to $154 for each basic unit. Delivery is from stock to two weeks.

Nordic Controls Co., 155 N. Van Nortwick Ave., Batavia, Ill. 60510. Phone (312) 565-1200 [359]

Hand-held tachometer measures 0.25 to 50,000 rpm

Computak, a microprocessor-based digital hand-held tachometer, can be programmed to compute any of 13 standard units of measurement across a wide range of speeds—from 0.25 to 50,000 rpm. The ranges of the device are: 0.25 to 200 ± 0.01, 200 to 2,000 ± 0.10, 2,000 to 20,000 ± 1.00, and 20,000 to 50,000 ± 10.00 rpm. Computak is available with either an English measuring-system program (model CT2000) or a metric system program (CT2100). In the English system, the tachometer computes revolutions, inches, feet, yards, or miles per minute, second, or hour. In the metric system, it computes either revolutions or meters per time unit. The device features a liquid-crystal digital display, memory recall, and quartz-crystal accuracy. The CT2000 sells for $265, the CT2100 for $275. Both are in stock.

Jones Instrument Corp., 430 Fairfield Ave., Stamford, Conn. 06904. Phone John Walsh at (203) 327-6440; [358]



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Products newsletter

National selling sample 256-kilobit bubble memory

National Semiconductor Corp. has begun selling sample quantities of a 256-kb bubble-memory device, the NBM2256. At an operating frequency of 100 kHz, the new memory **has a data rate of 100 kb/s and an average access time to the first bit of a random block of 7 ms.** Typical power dissipation is 750 mW.

The memory, which has a 1.1-by-1.1-in. footprint, will be supported by four additional circuits: the INS82851 controller, the DS3615 function driver, the DS3616 coil driver, and the DS3617 sense amplifier. The three DS-series circuits are scheduled to be available this summer, but the INS device will not be ready until late in the year. Until the complete set of support circuits is available, National will be selling an evaluation board that performs all the basic functions, using standard integrated circuits where necessary.

Unit-quantity pricing on the NBM2256 memory is $500. The NBS100 evaluation board, which will be offered in the second quarter, will be priced at $1,300 in units. All the bubble-memory products are available through National's Santa Clara, Calif., factory.

Fast d-a converters to debut in April

ILC Data Device Corp. in Bohemia, N. Y., is designing a **monolithic 14-bit digital-to-analog converter to incorporate into two superfast hybrid units** that will be available in sample quantities by the middle of April this year. One unit is an extremely low-glitch emitter-coupled-logic device that settles within 30 ns. The other is a TTL converter that has little glitch and settles in less than 100 ns. Both units are current-output converters with on-board references.

DDC is also developing **a 14-bit multispeed and multichannel synchro/resolver-to-digital converter** system based on Texas Instruments' 9900 16-bit microprocessor. The unit will have wide operating flexibility and will use DDC's model 8585 analog-to-digital converter.

SPI to supply SD5000 quads

Semi Processes Inc., Santa Clara, Calif., kicks off its recent second-sourcing agreement with Signetics Corp.'s Analog division [*Electronics*, Dec. 6, 1979, p. 50] by making **the SD5000 quad analog switch array family available from stock.** SPI will make, and eventually market, the Sunnyvale, Calif.–based division's entire double-diffused MOS product line, including the new 60-V SD220 series. SPI also intends to develop higher-power (above 300 V) switching applications for the D-MOS technology. Single and 100-piece prices for the SD5000N, in a plastic package, are $4.40 and $3.60 apiece, respectively.

Modicon upgrades programming panel

Gould Inc.'s Modicon division in Andover, Mass., has upgraded its P180 programming panel **to offer an optional ladder-listing feature and to make it compatible with many RS-232-C or current-loop display terminals and printers.** The option in the Deluxe P180 provides hard-copy listings of relay ladder programs resident in any Modicon 484 industrial process controller. The Deluxe version is priced at $1,895; the basic P180 can be updated in the field to offer the Deluxe's features.

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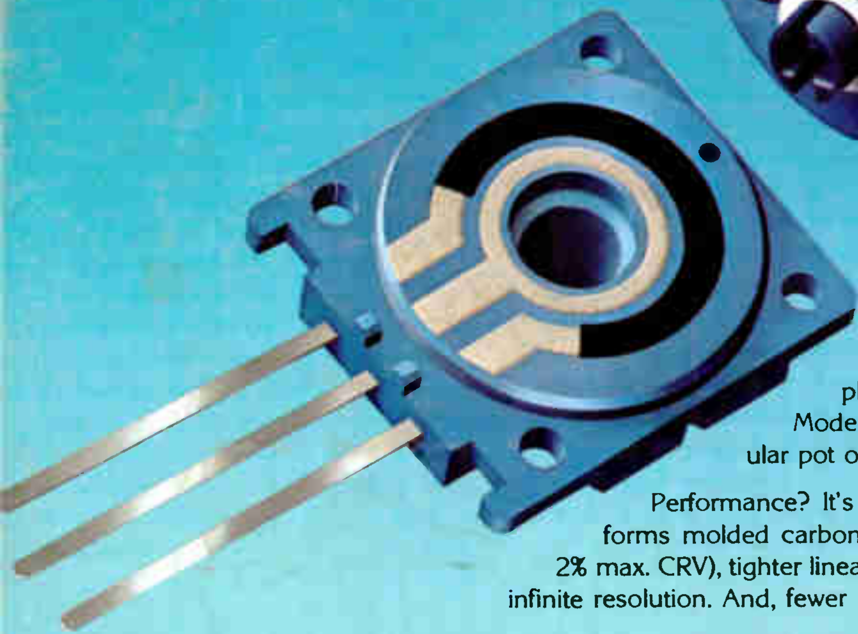

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