NOVEMBER 22, 1979

EIA FORECASTS PENTAGON COMPUTER PUSH/88

C-MOS microprocessor matches n-channel performance/111

D-a converter provides bit-slice processor with fast analog output/140

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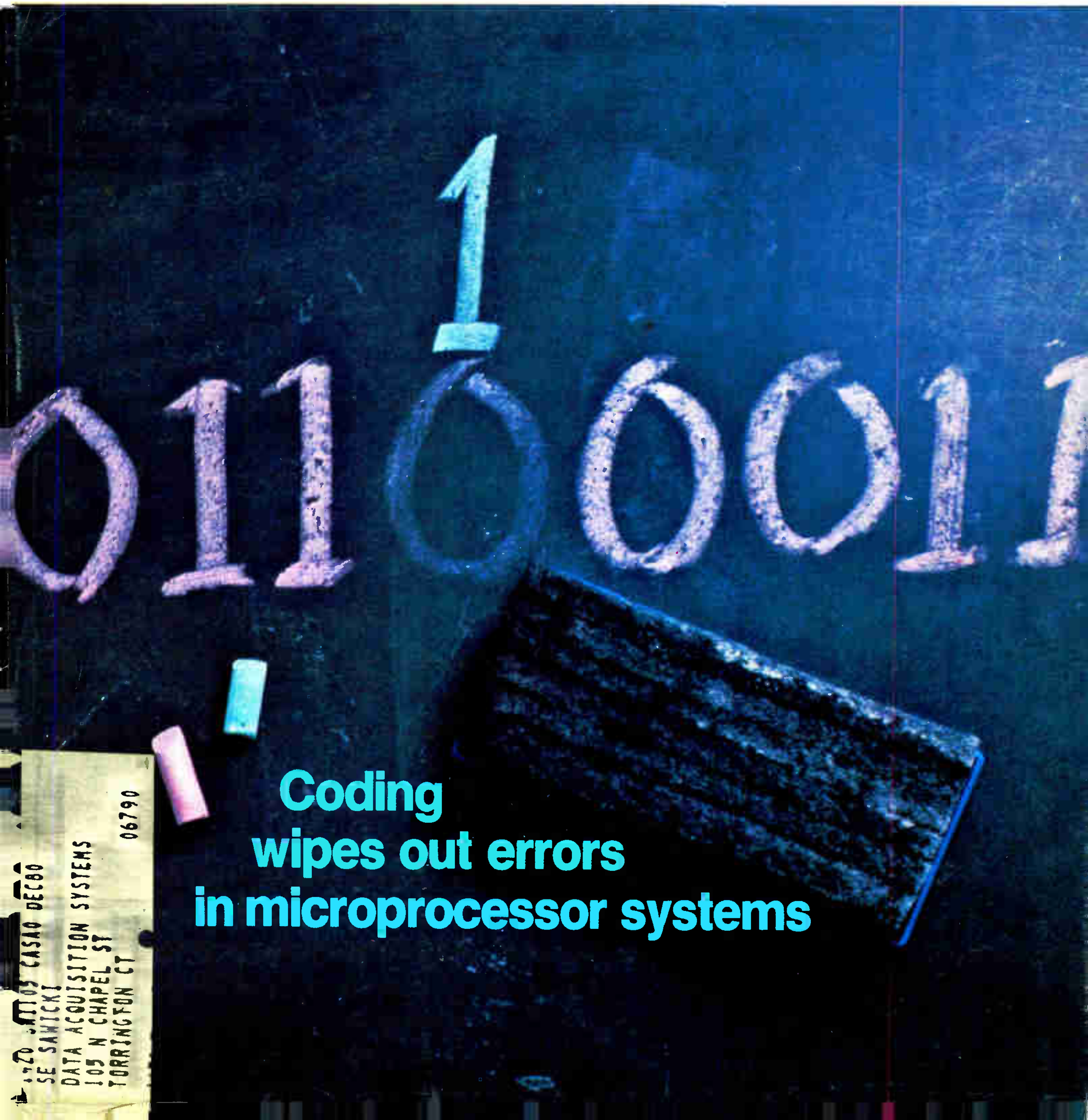

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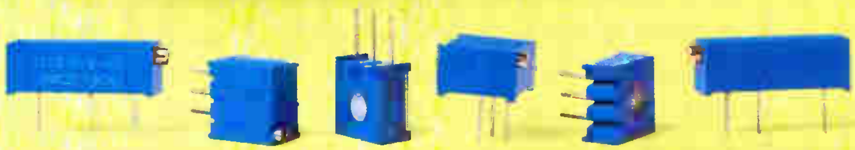

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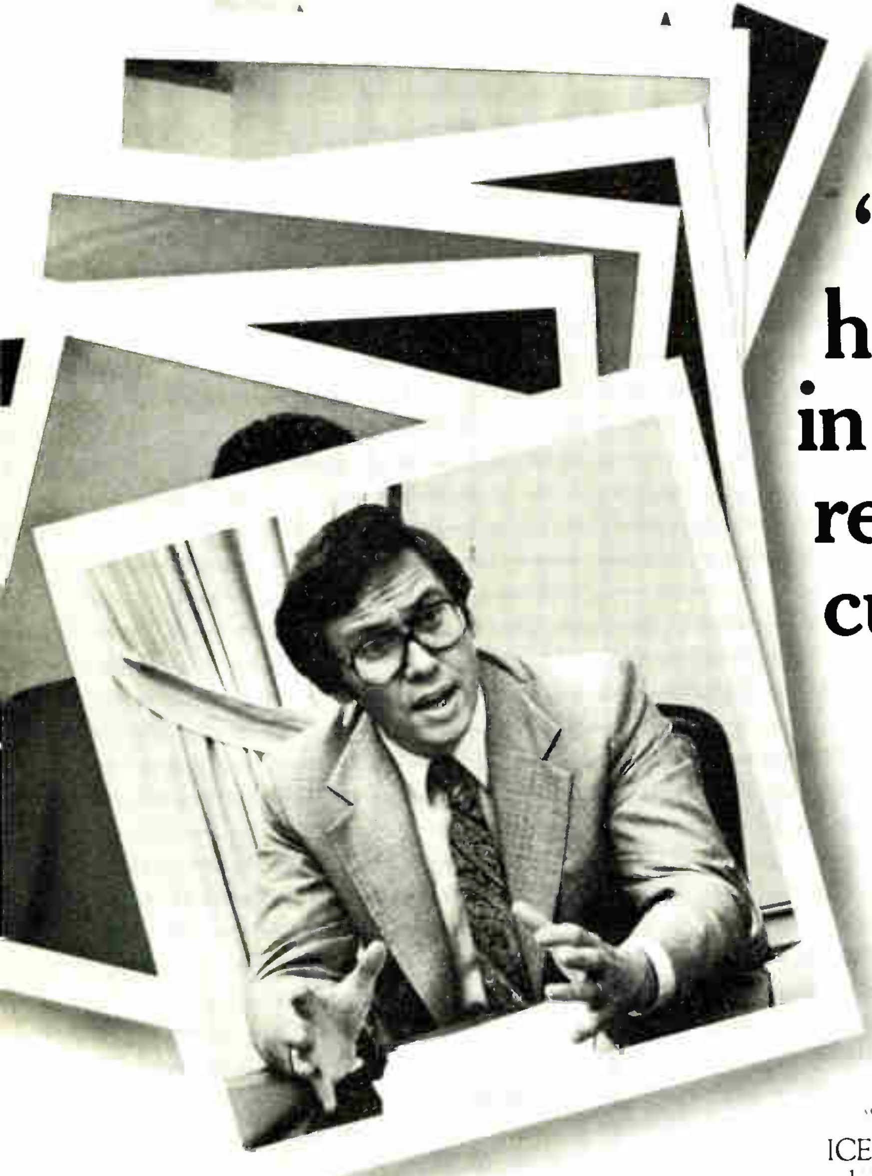

"We and Intel have something in common–responsiveness to customer needs."

I. Gary Bard, President,
Aydin Controls.

I. Gary Bard: "We've carved out a dominant position in the video graphics marketplace by listening carefully to our customers and giving them the features and capabilities they need. To do that, though, we need to take advantage of the leading edge of microcomputer technology.

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Electronics
The International Magazine of Electronics Technology
Vol. 52, No. 24 • November 22, 1979

Highlights

Cover: Hamming for microprocessors, 103
Circuit specifics show how the pervasive algorithm for error detection and correction worked out by Richard Hamming is being used in 8- and 16-bit systems
Cover is by Art Director Fred Sklenar.

Vertical-MOS gains in power market, 85
V-MOS field-effect transistors, with their inherently high gain and switching-speed characteristics, are threatening to take the discrete power transistor market away from bipolar devices.

Fast C-MOS process challenges n-MOS, 111
A complementary-MOS process using two levels of polysilicon interconnections brings n-MOS speed and C-MOS power frugality together in a microcomputer family.

A-d conversion: catching the drift, 123
Digital and analog techniques are combined to combat temperature-induced linearity and offset errors in the analog-to-digital converters of data acquisition systems—inexpensively.

. . . and in the next issue
Electronics industry executives look at the year ahead . . . an overview of this year's International Electron Devices Meeting . . . a scaled-down process for bipolar memories.

Publisher's letter

Like more than a few of today's circuit designers, Ernst L. Wall, member of the technical staff of ITT's Telecommunication Technology Center in Shelton, Conn., got into the field by happenstance. He is actually a trained physicist (BS, University of Georgia; MS, University of Florida) who became involved in semiconductor research and eventually gravitated to design work.

Even the assignment to design the Hamming code circuits described in the cover article (p. 103) was unexpected. "Serendipity is the story of my life," Wall remarks.

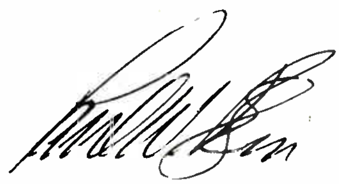
He went to work at the ITT center as a "liaison" man and was only peripherally involved in processors. When the need for a high-reliability processor for telecommunications switching equipment came up, he looked into Hamming code and suggested a design. His idea went over and he got the assignment.

However, the opportunity did not open up as accidentally as he modestly tries to convey. There was a lot of hard work and study preceding this project. In a sense, Wall is an example of turning continuing education into a career opportunity.

During "a streak of unemployment" in the early 1970s, he decided to get up to speed on microprocessors and microcomputers. While his wife brought in a salary as a teacher, Wall invested some $3,000 for equipment and dug in to learn digital-circuit design. Later he took a course in compiler theory.

By the time he arrived at ITT, he was well grounded in microprocessor design. Since completing the Hamming code circuits, he has been working on other projects, including a tone generator and filtering systems. He is comfortable in circuit design now and wants to stay with it.

"I'm a grease-under-the-fingernails type at heart," says the 41-year-old physicist-turned-engineer. "In digital logic design, if you learn the fundamentals and then do some work in it, you've got 90% of the problems licked."



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Readers' comments

Another pioneer

To the Editor: As a designer of monolithic digital-to-analog converters, I read with great interest your "Monolithic approach bears fruit in data conversion" [May 10, p. 105]. In general, I found the article well researched and presented. However, I did find disappointing the lack of mention of one monolithic d-a converter manufacturer who has pioneered precision film resistor processing—Micro Power Systems in Santa Clara, Calif.

The article credits the AMD Am-6012 with being the first single-chip 12-bit device that gives 12-bit accuracy without individual trimming of resistors. In fact, Micro Power Systems has been offering a monolithic complementary-MOS d-a converter (MP 7621) for some time in 12-bit linearity grades with no resistor trimming. This particular design is based upon a straight film-resistor R-2R ladder approach.

The article perhaps overemphasizes the significance of AMD's new 12-bit design. The Am6012, though very innovative, has limitations as a 12-bit converter. Aside from not being accurate to 12 bits (accurate to within ±0.05%), it suffers from no on-board application resistors and lacks low-temperature-coefficient film-resistor processing.

Your article mentions that the Harris 562 is faster than the Analog Devices and PMI models. Although the Harris product is indeed faster than the original Analog Devices part, it has optimized speed at the expense of power dissipation. The Harris part has been designed around a 5-mA full-scale current and typically dissipates 660 mW with ±15-V supplies. The AD, PMI, and Micro Power designs all maintain a 2-mA full-scale current with dissipations of 525 mW, 375 mW, and 120 mW, respectively.

In all fairness, Analog Devices' AD 566 12-bit converter achieves the 12-bit accuracy at 180 mW of dissipation at speeds comparable to that of the Harris design.

Donald T. Comer
Los Gatos, Calif.

News update

■ A battlefield computer system called Wavell is about to go into production after a prototype spent 1978 in the British army undergoing field tests. Intended as a front-line aid to commanders and their staff in making decisions, Wavell will offer information on troop dispositions, combat strengths, orders of battle, and intelligence reports via cathode-ray-tube displays [*Electronics*, Aug. 4, 1977, p. 56 or•3E]. Its developer, Plessey Defence Systems Ltd. in Addlestone, Surrey, has received a first $22.5 million production contract.

Wavell works with any internationally standardized trunk communications network to distribute information among headquarters but eventually will be mated with the Ptarmigan digital switching system that will become operational in the early 1980s [*Electronics*, Aug. 19, 1976, p. 73]. The computer on which it is based will have a magnetic-bubble memory backup from Plessey Microsystems Ltd. **-Kevin Smith**

■ Despite the fact that tests are still going on to determine the interference of large windmills with television reception [*Electronics*, Sept. 13, p. 96], residents of Rhode Island's offshore Block Island have no doubts about the problem. Neither apparently does the U. S. government, which will spend upwards of $600,000 to enable them to watch TV programs without the picture shaking.

The action is mandated by the law that says Federal projects may not interfere with the environment. On Block Island, it represents the cost of a coaxial system to homes within a mile or so of the island's new wind turbine, a project of the Department of Energy and the National Aeronautics and Space Administration.

The turbine, or windmill, generates electricity for the Block Island Power Co. But its large rotating metal blades cause interference, producing extraneous modulation of the electromagnetic waves now carrying the television signals.

-Harvey J. Hindin

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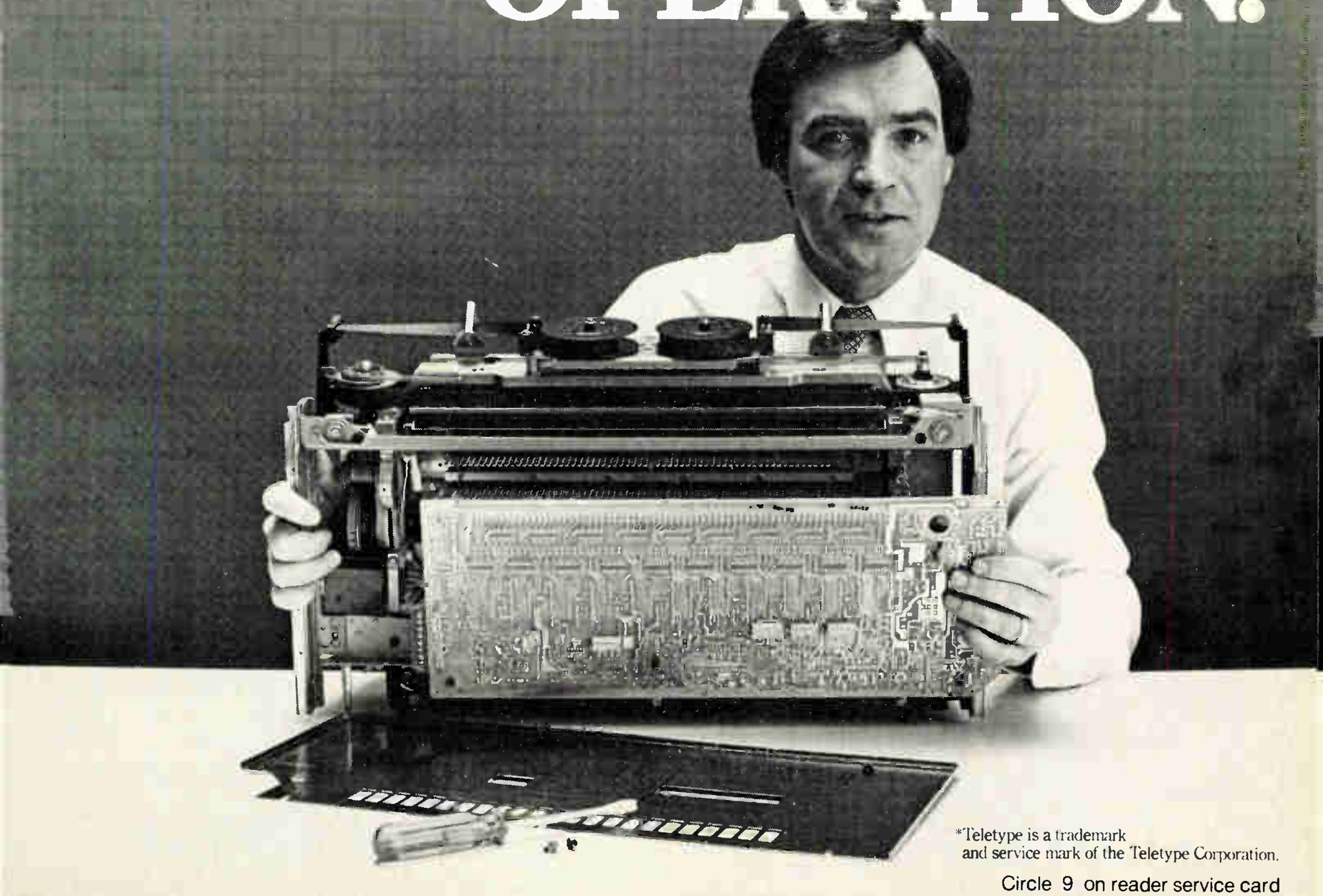

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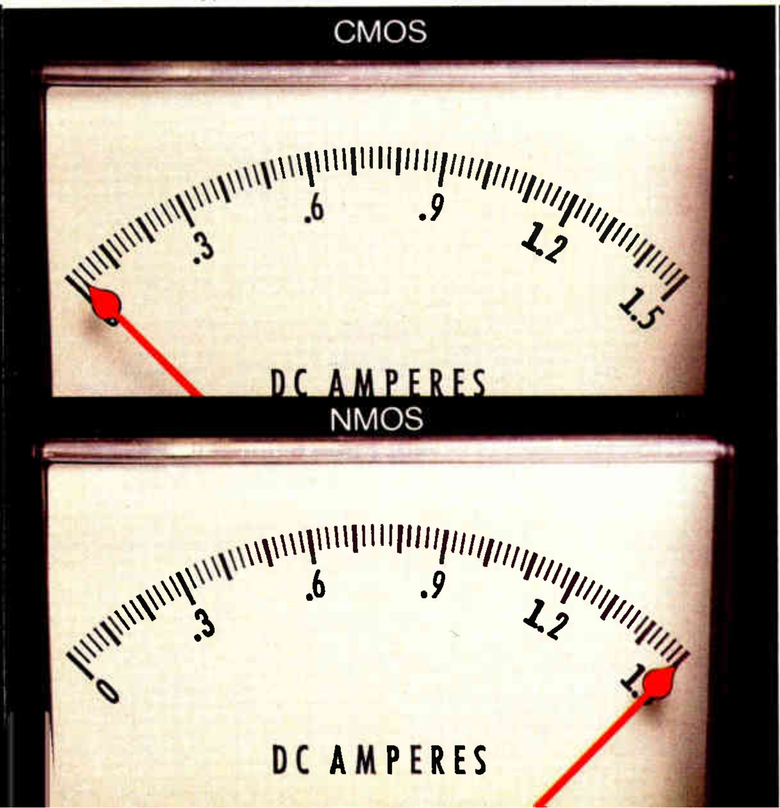

(2) Low operating temperature. NMOS boards can get very hot. Our CMOS boards generate little heat. So cooling fans are totally unnecessary.

RCA introduces Microboards with CMOS technology. At competitive prices.

And for your design, this could very well be the end of NMOS. Just glance at the illustrations below and judge for yourself. You'll find that CMOS Microboards (based on the COSMAC 1800 Series Microprocessor) can do more jobs in more different environments than any other single-board computer on the market.

The "go anywhere" board.

Ordinary NMOS boards consume lots of power and give off lots of heat. That calls for bulky power supplies, large cabinets and fans to keep the whole package cool.

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Plus our microboards consume so little power, they can run on built-in batteries. Which makes them particularly suitable for just about any portable application.

In noisy environments like industrial process control, RCA Microboards are the logical choice. Like CMOS logic, CMOS Microboards can withstand voltage noise spikes three times higher than NMOS boards.

The introductory line.

For starters, the RCA Microboard line includes two basic single board computers, three memory boards, a UART interface board, a combination memory and I/O board, a 5 V power supply, a five card chassis.

And there's more in the design stage: I/O boards, D/A and A/D boards, plus additional computer and memory boards.

All boards measure 4.5 × 7.5 inches. So you get a very compact system, even when you use expandable memory and I/O with the single board computer.

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We've designed our BUS to help save you hardware headaches. Any board plugs into any slot in the backplane, any time. No need to hand wire backplanes or breadboards.

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Another design feature—none of those annoying "wait states" to hold up your design.

Full design support products.

To make prototyping easy, we're offering a low cost fully assembled prototyping system containing a Microboard computer, power converter, control/display module, technical literature, and all the nuts and bolts you need to get to work on your design.

Microboards are also plug-in compatible with all the RCA COSMAC development tools. Such as our COSMAC D.O.S. Development System (CDP18S007). So integration and checkout of software and hardware is a snap.

Free color brochure.

We've put together a 12 page color brochure giving full technical data on RCA's CMOS Microboards.

To get your free copy of the brochure, use the reader service card or contact your local RCA Solid State Distributor.

Or contact RCA Solid State headquarters in Somerville, New Jersey. Brussels, Belgium. Tokyo, Japan.

RCA

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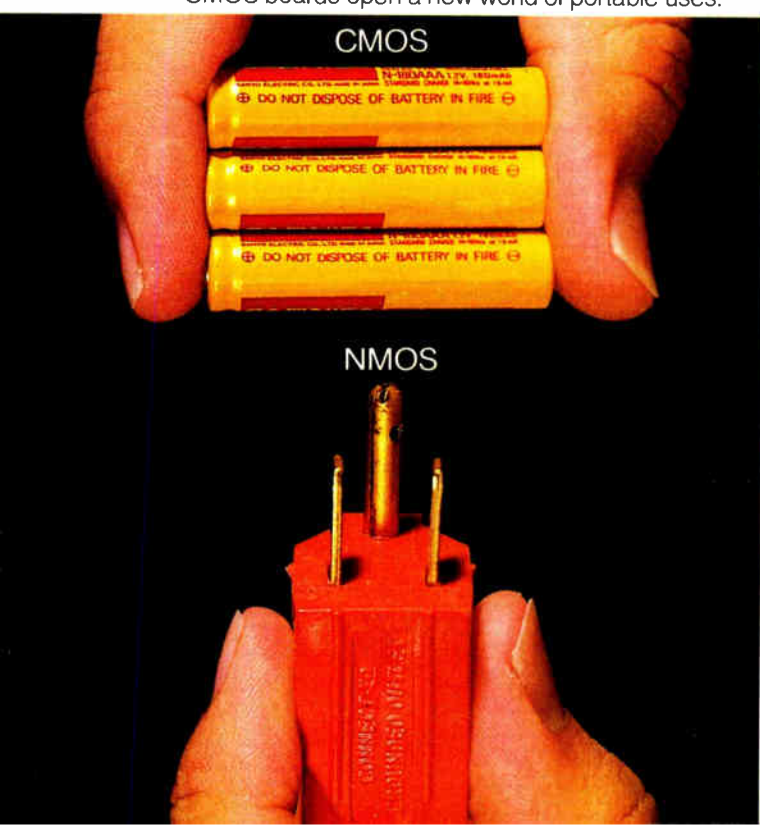
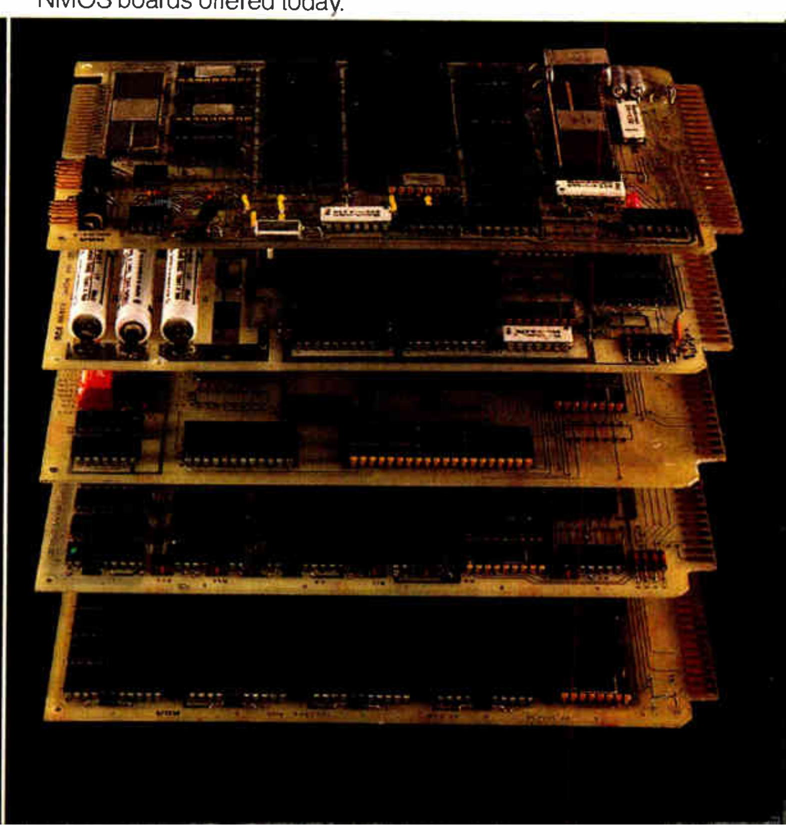
(3) Portable operation. NMOS boards are normally operated off power lines. Battery powered CMOS boards open a new world of portable uses.



(4) A lot in a little space. RCA Microboards measure 4.5 × 7.5 inches. Compare this to most NMOS boards offered today.



People

Champine decries increases in cost of innovation in U. S.

"The challenge for the country today is to restore profitability to technical innovation," says George Champine. He is in a good position to know, since managing technological development—and keeping it profitable—is his job as director of research for Sperry Rand Corp.'s Univac division in Blue Bell, Pa. Although appointed to the position just last month, Champine is no newcomer to research and development in electronics, having been associated with Univac's computer operations for over 20 years.

Cost-conscious. Champine keeps an eye on the rising cost of technical innovation.

A number of factors makes meeting that challenge harder now than ever before. To begin with, "the current tax structure has taken the profitability out of innovation," he says. And the financial aspects of research are becoming more critical because, Champine continues, "the sophistication of technology makes the equipment needed to develop it very expensive. Yet without that equipment you can't compete."

This rising price tag on research is already causing a centralization of research efforts. As a result, Champine, who runs the central research lab at Blue Bell, coordinates the efforts of Univac's other labs: a semiconductor facility in Eagan, Mich., one devoted to terminal research in Salt Lake City, Utah, and another concentrating on rotating memory at Univac's ISS subsidiary in Cupertino, Calif. In addition, he works closely with Sperry's corporate research facility in Sudbury, Mass.

In addition to making research more expensive, technology is gaining sophistication faster and product development time is shorter. Champine says choices of basic technology must be made as much as seven years before a product is ready.

Besides contributing to this fast pace and rising costs, large-scale integration is forcing computer manufacturers to change the type of research they do. "As chip density increases, chip specialization increases and we need less," Champine notes. That translates to low-volume requirements, so "all computer makers must do their own logic chip design, mask making, testing, and prototyping." And Champine, despite the litany of difficulties, looks forward to positioning Univac in the forefront of those sectors.

Watson plans a firm hand on software R&D

Even before it became apparent to most that Computer Automation Inc.'s fiscal 1979 would be a losing season (nearly $4.2 million), management at the Irvine, Calif., minicomputer manufacturer began looking ahead to future campaigns. One of its more important moves was to hire Gordon M. Watson, a hardware and software executive, out of TRW Electronics.

Now, as the newly appointed vice president for engineering at Computer Automation's Naked Mini division, the 43-year-old Watson heads a new engineering team. The team represents a redefinition of the firm's approach to the development and production of computers for original equipment manufacturers, as well as added emphasis on parallel software work for all products.

With prior experience including a

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People

Watchdog. Watson believes bad management, not bad technology, causes failure.

seven-year stint at Varian Data Machines where he became vice president for engineering, responsible for all hardware, firmware, and software development, Watson says he is totally convinced that engineering operations most often fail because of a lack of management—"and not the lack of technology or skill in performing the trade." He is determined to see that such failures do not occur.

"When I arrived, I found that the software activity, for example, lacked leadership, and that there was zero gray hair in the engineering organization. They had used first-time people to do things and, as a result, they had a low probability of success." Thus, Watson is trying to build structures with good, journeyman managers, "those with proven track records, who are compatible, team-type people that I've known. Also, he says, "I don't see any mystique in software." Watson, whose background as a practicing engineer was 70% software, believes "you can build software as successfully as hardware. It just takes half again more management attention."

From a hardware standpoint, Watson plans to move Computer Automation much closer to the forefront of technology. Whereas the firm typically built and sold low-cost systems and used low- to medium-performance devices, "we will broaden our line and have more high-performance, high-ticket items," he states, like the upcoming Protos. □

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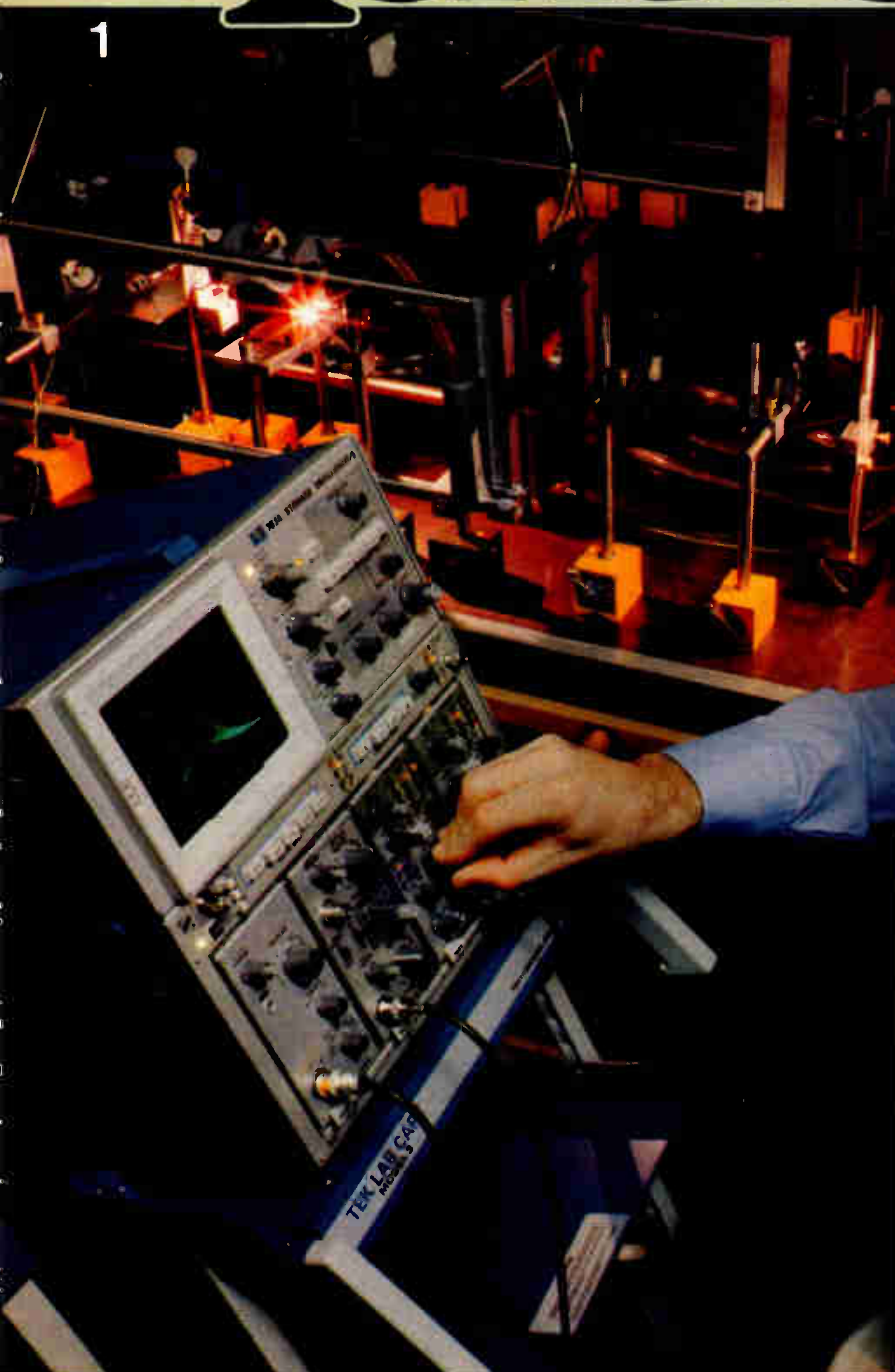

Tektronix offers 15 storage scopes and the widest selection of storage modes. Here is how just a few of those scopes are being used today.

1 The FAST storage mode of the 7834 being used to capture high speed laser pulses.

2 The extremely bright display provided by the 466 in variable persistence mode makes it easy to view low rep rate switching performance.

3 The TM 500 with an SC 503 bistable storage plug-in being used for audio maintenance.

4 The highly portable 214 at work in system troubleshooting.

5 The long view time provided by bistable storage in the 5111 is useful for the study of pain threshold data.

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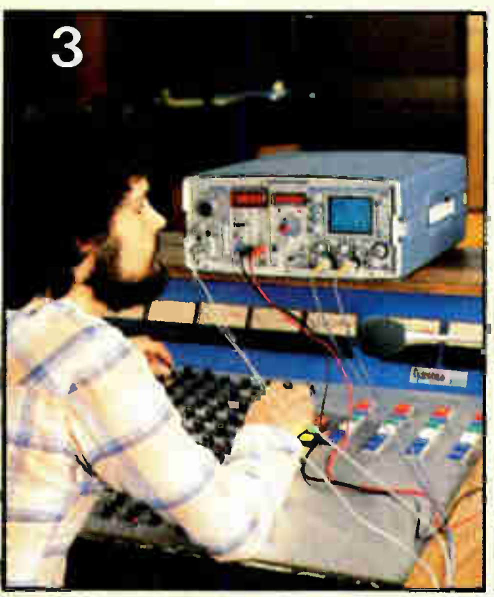

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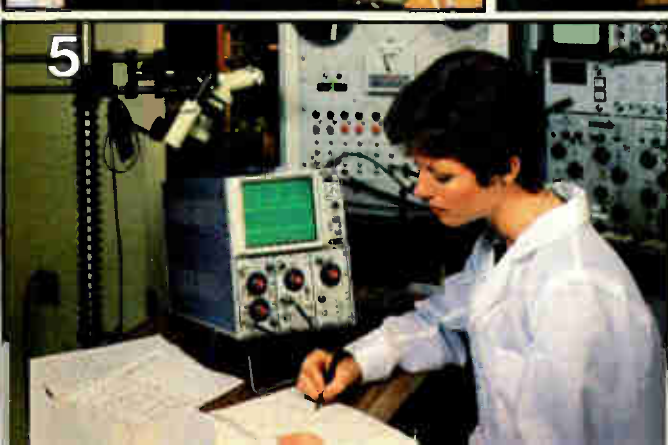

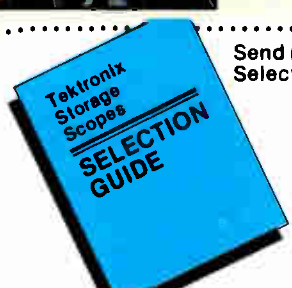

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Mr. Carter's feeble R&D initiatives

When Jimmy Carter sent his new program for spurring American industrial research and development to Capitol Hill early this month, the specifics failed to support the President's press conference rhetoric. Mr. Carter proposes to "unleash America's creative genius" by adding some $55 million to the Federal R&D pot—an increase of 0.002% on fiscal 1979's obligations of $28 billion.

But those pathetic numbers are less important to innovators in industry than the President's failure to address the issue of tax law changes that would encourage increased private R&D investment by permitting some of it to be tax-deductible. Much of the Federal R&D budget—one half of it spent by the military—goes for specific products that have limited appeal to many innovators. Under most Government programs, a company must respond to an agency's needs rather than the demands of the marketplace.

The President offers short rations for new small companies—which history shows have been responsible for most advances in electronics and other high technologies. He advances no plan to encourage capital investment, nor does he make mention any capital-gains tax changes that would permit the use of limited stock options to attract new engineering talent.

What might have been a couple of good points—changes in patent policy and relaxation of antitrust rules on R&D collaboration between companies—are weakened by their vagueness. A proposal to grant exclusive manufacturing rights to a company whose product would use a Federally owned patent has little appeal since the Government would retain ownership of the patent.

White House domestic policy chief Stuart Eizenstat, the man behind the rewrite that watered down the stronger draft initiatives first advanced by the Department of Commerce, says the missing tax incentives may show up separately in the fiscal 1981 budget. But Eizenstat's credibility at the moment is at a new low in view of his performance on the long-awaited initiatives. They do not provide significant help to industry, much less unleash its creative genius, and they certainly have not helped Jimmy Carter.

It's time to be heard

Talk about silent majorities—about 53% of the eligible membership failed to return ballots in this fall's Institute of Electrical and Electronics Engineers election. Of course, that percentage differs little from earlier—in fact, about as many votes were cast as last year, but there was a smaller base from which they were drawn. Still, the continued apathy is nothing to cheer about.

It is possible to speculate at length on the reasons for this apathy, but it is more important to shake it. Why? Because the concerns of the IEEE are crucial to the well-being of the individual engineer, of the electronics industries, and of the great world beyond. With electronics clearly the dominant technology for at least the next century, engineers must prepare for influential new roles in society.

No better vehicle exists for this than the IEEE. Indeed, the long-standing controversy about the extent to which the organization should engage in member-oriented professional activities stems from a recognition on both sides that the IEEE can be a powerful group.

Of course, this election hardly settles that controversy, but neither should the dispute over professional activities shroud the importance of technical activities. The IEEE must fill both roles, and it must constantly evaluate how well it is meeting the needs of the members and the rest of the world. It is time to get involved—in fact, it is past time.

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Meetings

VHSIC—A New Era in Electronics, American Institute of Aeronautics and Astronautics (Box 91295, Dept. VHSIC, Los Angeles, Calif. 90009), Washington, D. C., Dec. 6–7, and Boston, Jan. 21–22.

Electronic Component and Telecommunications Apparatus Industry Show, Ente Fiera—Mostra di Componenti Elettronici (Viale degli Scaligeri—C.P. 805, 36100 Vicenza, Italy), Vicenza fairgrounds, Dec. 8–10.

Electronic Mail in Tomorrow's Office, Institute for Graphic Communication (375 Commonwealth Ave., Boston, Mass. 02115), Highlands Inn, Carmel, Calif., Dec. 9–11.

Second International Symposium on Mini and Microcomputers in Control, International Society for Mini and Microcomputers (P. O. Box 2481, Anaheim, Calif. 92804), Galt Ocean Mile Hotel, Fort Lauderdale, Fla., Dec. 10–11.

Distributed Data Processing, Data Communications and Networks, and Minicomputers Conference, American Institute of Industrial Engineers, (P. O. Box 3727, Santa Monica, Calif. 90403), Jack Tar Hotel, San Francisco, Dec. 10–12.

Computer Networking Symposium, IEEE Computer Society (Box 639, Silver Spring, Md. 20901) *et al.*, National Bureau of Standards, Gaithersburg, Md., Dec. 12.

Conference on Decision and Control, IEEE, Galt Ocean Mile Hotel, Fort Lauderdale, Fla., Dec. 12–14.

Winter Consumer Electronics Show, Electronic Industries Association, Convention Center, Hilton and Jockey Club Hotels, Las Vegas, Nev., Jan. 5–8.

Sixth Semiannual ATE Seminar and Exhibit and First Annual Test Instruments Conference, Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215), Convention Center, Pasadena, Calif., Jan. 7–10.

Second Design and Finishing of Printed Wiring and Hybrid Circuits Symposium, American Electroplaters' Society (1201 Louisiana Ave., Winter Park, Fla. 32789), San Francisco Hilton, Jan. 15–17.

TV Mex, the TV Microelectronics and Microprocessing Exhibition, and IDEA, the International Domestic Electrical Appliances Exhibition, Montbuild Ltd. (11 Manchester Sq., London W1M 5AB, England), National Exhibition Centre, Birmingham, England, Jan. 15–17.

Advanced Semiconductor Equipment Exposition, Associated Ad-Ventures Inc. (Suite V, 4546 El Camino Real, Los Altos, Calif. 94022), Convention Center, San Jose, Calif., Jan. 22–24.

Annual Reliability and Maintainability Symposium, American Society of Mechanical Engineers, IEEE *et al.* (for information, contact N. H. Kutner, Burroughs Corp., Burroughs Pl.–5F48, Detroit, Mich. 48232), San Francisco Hilton, Jan. 22–24.

Communication Networks '80, The Conference Co. (60 Austin St., Newton, Mass. 02160), Sheraton Washington, Washington, D. C., Jan. 28–30.

Fifth Topical Meeting, Integrated and Guided Wave Optics, Optic Society of America (Suite 620, 200 L St. N W., Washington, D. C. 20036) and IEEE, Hyatt-Lake Tahoe, Incline Village, Nev., Jan. 28–30.

11th International Symposium for Mini and Microcomputers, International Society for Mini and Microcomputers (P. O. Box 2481, Anaheim, Calif. 92804), Asilomar Conference Grounds, Pacific Grove, Calif., Jan. 30–Feb. 1.

Eighth Semiannual Conference on Federal ADP Procurement: New Departures, American Institute of Industrial Engineers (P. O. Box 3727, Santa Monica, Calif. 90403), Shoreham Americana Hotel, Washington, D. C., Feb. 4–6.

Micralign® 200 Series... Higher throughput than step-and-repeat at a much lower price.

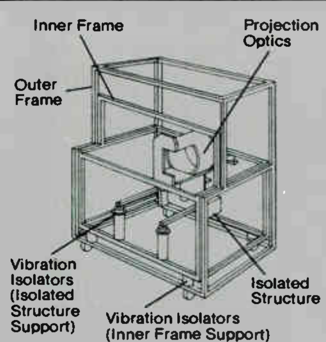
Perkin-Elmer designed the new Micralign Model 200 to be the most cost-effective projection mask aligner available. In performance, it achieves 2-micron geometries or better in production, distortion/magnification tolerance of 0.25 micron, and 4 percent uniformity of illumination. Options available include automatic wafer loading and automatic alignment. Soon to be available: deep UV optical coatings for still smaller geometries.

Compared to the leading step-and-repeat aligner, the Micralign Model 200 delivers outstanding performance for not much more than half the cost. It takes about a quarter of the floor space. It provides consistently higher throughput regardless of die size.

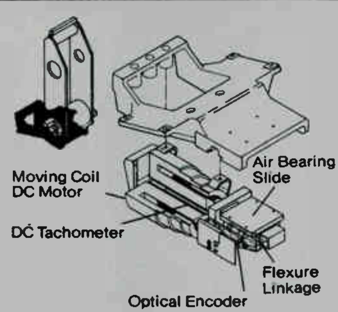
The Model 200's remarkable performance is the result of a number of major innovations.

Improved optical design and fabrication
We improved the optical design to provide increased resolution and depth of focus. Optical manufacturing tolerances are five times tighter to ensure precise overlay from aligner to aligner.

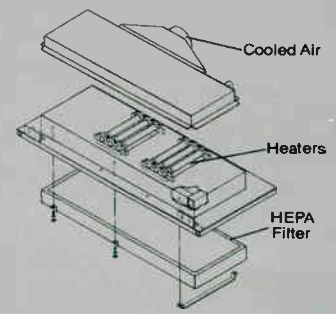
Near-zero vibration
We minimized vibration. We constructed the Model 200 with two frames—one inside the other. The inner frame, which carries the projection optics and carriage drive, is completely isolated from the outer frame.



We incorporated a superb linear motor carriage drive with air bearing slide. This drive does more than eliminate vibration. With the air bearing feature there's no contact and no wear. And no limit to carriage drive durability.



Built-in environmental control
We provided the Model 200 with a built-in environmental chamber. External air, supplied by you or from our optional air conditioning system, is blown through a HEPA filter and heating elements built into the Model 200 top cover. A positive-pressure, class 100 environment is carefully controlled to better than 1 °F.



We included a separate thermal control for the mask, to compensate for mask run-out.

No mask contamination
We designed a sealed mask carrier for the Model 200. You put the mask in the special carrier right in the mask department. Seal it. When you load the sealed carrier in the Model 200, the cover plates are automatically removed. After use, the cover plates are automatically replaced.

Proven production capabilities
Perkin-Elmer, the leader in projection mask alignment systems, offers six years of proven production capability, with an excellent training and service record.

Get all the facts
These are just a few of the features that make the Micralign Model 200 Series a completely new concept in projection mask aligners. Get more details on how these and other improvements in design can translate into improvements in your production. For literature, write Perkin-Elmer Corporation, Microlithography Division, 50 Danbury Road, Wilton, CT 06897. Or phone (203) 762-6057.

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Circle 27 on reader service card

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When you buy a Fluke system, you join the ranks of companies like IBM, Philips, and Olivetti. In fact, our customers include the top electronics manufacturers throughout the world. Why do these companies choose FAS? Because our systems offer solutions backed by years of experience in solving tough test problems. And because we've reduced their testing costs by one-third.

A close look at testing.

Deciding when to test is as important as how. With an overall goal of high end-product turn-on rates, PC board functional testing is the best approach. It offers comprehensive testing to locate faults across the entire fault spectrum, from production faults to dynamic operational errors.

Deciding how to test comes next. You need to consider a wide range of factors including PC volume, board types, test yield, production yield and anticipated new products. You also need to take a look at the true costs of the system including initial capital expense, programming and diagnostic costs and the kind of service you'll get when every moment of downtime costs thousands.

Take a close look at Fluke Automated Systems. You'll find some surprisingly simple answers to these complex questions.

Making every dollar count: time proven techniques.

We pioneered the concept of reference board testing. Over the years, it has proven to be the fastest, most economical means of board testing, producing higher throughput and superior test confidence.

FAS systems are designed to make test program generation fast and easy to learn. Over 700 automatic stimulus patterns can be selected with the push of a button. For sequential logic, our high level language uses efficient data compression techniques, allowing a user to quickly generate massive stored sequence stimuli. Both techniques can be interleaved "on-the-fly" gaining the advantages of each.

The key to testing is comprehensive test programs. Fluke's test techniques enable exhaustive test sequences to operate at real-time speeds. Extensive test response patterns are data-compressed into a single output signature. Consequently, operation is not limited by disk capacity or access times — problems that plague simulator-based systems.

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Production throughput with a FAS test system is increased by a full spectrum of diagnostic methods. They range from 12 manual aids (including Faultrack® and a built-in logic analyzer for LSI) to a powerful computer diagnostic package called Autotrack®

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We use the very latest teaching techniques, including videotape and programmed learning courses, in addition to live lectures and demonstrations. Our average instructor has a minimum of seven years of experience. We have trained over 8,000 customer personnel in the past seven years.

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The key to effective applications support is making sure your Fairchild system does everything it can to meet your specific testing requirements. We maintain a worldwide team of applications engineers to help you get your system up and running. We also have a software library containing hundreds of ready-to-run device test programs for standard ICs, almost every known microprocessor, I/O chips, bipolar RAMs, MOS RAMs and a number of support circuits. These programs would cost you tens of thousands of dollars if you had to develop them yourself from scratch.

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NTT to look at Motorola's pagers in test

In the first step in the open-door procurement policy sought by the U. S., Motorola Corp.'s Communications Systems division, Schaumburg, Ill., will ship about 150 pagers to the Nippon Telegraph and Telephone Public Corp. next summer as part of a qualification test to enter the Japanese home market. **The cost of the test units will be comparable to the $300 price tag for pagers linked to telephone systems or specialized common carriers in the U. S.,** but Motorola will modify them to meet NTT's specifications.

Exxon's Magnex ready to market thin-film heads

Magnex Inc., an Exxon Enterprises Inc. business venture formed in September 1977 to develop and manufacture thin-film magnetic recording heads for computer disk and tape drives, is about to begin volume production of what it calls the integrated slider. This thin-film head is fabricated like an integrated circuit. **Hundreds of magnetic circuits are deposited on a wafer,** which is then diced and machined to form hundreds of one-piece head and slider units with the tightest tolerances, highest densities, and lowest costs to date.

Semiconductor test, fabrication systems linked

Semiconductor manufacturers will soon be able, for the first time, to buy test and fabrication systems that can be tied together easily **to make a totally integrated facility tailored to their own needs.** The Macrodata memory test line and the Kasper Instruments line of wafer-processing, ion-implantation, and mask-alignment systems will be offered in the third quarter of 1980 with hardware that lets them communicate with any host computer from the PDP-11 family. The move reflects the thinking of Macrodata and Kasper Instruments. Both were acquired by the Eaton Corp. of Cleveland when it took over their parent, Cutler-Hammer.

Voice system fits Multibus

A single-board automatic Voice Recognition Module that is Multibus-compatible was announced by Interstate Electronics Corp., an Anaheim, Calif., subsidiary of A-T-O Inc. of Cleveland. Various models, with single-quantity prices ranging from $1,650 to $2,090, recognize 40, 70, or 100 words or short phrases with better than 99% accuracy. **After spectral analysis, all processing—including pattern recognition—is done digitally.** Also, using a patented algorithm, all words and phrases are compressed into 128 bits. Although this system is speaker-dependent, Interstate intends ultimately to design speaker-independent systems using custom integrated circuits.

RCA video disk to be unveiled on Dec. 6

It's official: on Dec. 6, RCA Corp., New York, will at last announce its 1980 marketing strategy for its video disk player. Although competitor Magnavox will be selling its Philips-developed VLT system nationwide by year-end [*Electronics*, Oct. 25, p. 72], **RCA will sell its capacitive system nationally right from the start through retail television outlets.** Backing the player will be an array of 300 or so disk titles, with 10 to 15 introduced every month during the first year. RCA has trimmed the weight of its system to less than 20 lb, eliminated many of the discrete components in favor of integrated circuits, and hiked the original retail price estimate from less than $400 to about $500.

Electronics newsletter

Datapoint adds word, message features to ARC

Look for Datapoint Corp. to join the rapidly growing list of companies with new products targeted at the automated office of the future [*Electronics*, July 19, p. 8]. Late this month, the San Antonio, Texas, firm plans to offer **word-processing and electronic-message capabilities that may be integrated with the data-processing and voice-communication management** already available on Datapoint's Attached Resource Computer (ARC) network system.

Among other features of the new package is believed to be a content-addressable access system, by which files can be searched for all documents containing user-specified key words or sets of words. Also expected is the announcement of a unique short-distance communications device using modulated, noncoherent infrared light.

VW to purchase Hall-effect sensors from Micro Switch

Honeywell Inc.'s Micro Switch division in Freeport, Ill., has concluded an agreement with Robert Bosch GmbH of West Germany to supply 1980 Volkswagen automobiles with Hall-effect ignition timing sensors (to replace mechanical breaker points). Micro Switch has been supplying Chrysler with Hall-effect devices for the ignition systems in Omni and Horizon automobiles since 1977, when these cars were introduced.

DEC unveils PDP-11/44 and DECsystem 540

The Digital Equipment Corp. has introduced what is probably its successor to the PDP-11/34. The Maynard, Mass., firm's new PDP-11/44 is said to have **twice the performance of the former unit but costs $23,900—only about 20% more.** The new 11/44 uses the instruction set of the larger PDP-11/70 computer, offers MOS main memory expandable from a basic 256 kilobytes to 1 megabyte, uses an internal 8-kilobyte cache memory to speed operation, and includes ASCII interface and programmer's consoles—both under microprocessor control and the latter with built-in diagnostics. DEC is simultaneously announcing the DECsystem 540. Based on the 11/44, the business-oriented system includes an enhanced Cobol compiler that DEC claims makes the system 50% faster than any of its earlier mid-range systems.

Bell underestimates software job for data network

"We underestimated the software job" is how AT&T chairman Charles L. Brown explained the company's decision at the beginning of the month to postpone its Advanced Communications System. Speaking last week at a meeting of New York security analysts, Brown said that, in the interim, **the company would "leapfrog" itself by going to new technologies in the all-digital data-communications network.** Meanwhile, the telecommunications giant is upgrading its existing network, to create what Brown called the "network of tomorrow," by installing new electronic local office equipment at the rate of one per working day and adding 21 more electronic switching systems to the long-distance network during 1980.

Addenda

Maurice R. Valente has been named president of RCA Corp. He succeeds Edgar H. Griffiths, president since September 1976, who becomes chairman while continuing as chief executive officer. Valente, 50, has been executive vice president of International Telephone & Telegraph Corp. . . . Meanwhile, Harold S. Geneen says he will **step down as ITT chairman at year's end.**

MICROSOFT. FANTASY ISLAND FOR MICROCOMPUTERS.

Microsoft is fulfilling the ultimate fantasy of microcomputers with excellent, reliable, tested software. Not just one or two items for certain computers, but a complete, integrated line of system software for all major microprocessors. Isn't it nice to know you can find a little island with such a big array of software? To microcomputers everywhere, we're a dream come true.

BASIC-86 and BASIC-80 Interpreters. BASIC for the 8086 and 8080/Z80. Both support the extensive language features that have made Microsoft™ BASIC the world standard—including PRINT USING, PEEK and POKE, RENUMBER, WHILE/WEND, CHAIN with COMMON, long variable names, protected files, error trapping, double precision arithmetic and dynamic string space allocation. Disk BASIC-86 for Intel SBC 86/12, $600. Disk BASIC-80 for CP/M, ISIS-II or TEKDOS. $350.

BASIC Compiler. With the same extensive language features—plus fast, relocatable object code—the Microsoft™ BASIC Compiler is ideal for all types of commercial applications and microcomputer development systems. This single pass compiler performs extensive optimizations that maximize speed and minimize space of the object code. Available for CP/M or ISIS-II operating systems. $395.

COBOL-80 Compiler. Indisputably the best compiler for powerful use of disk files, data manipulation facilities and interactive ACCEPT/DISPLAY. COBOL-80 is an ANSI-74 standard COBOL that supports indexed and relative files, including DYNAMIC access, FILE STATUS, START, READ NEXT, DELETE and REWRITE. In versions for CP/M or ISIS-II. $750.

FORTRAN-80 Compiler. More 8080/Z80 computers are using FORTRAN-80 than any other FORTRAN in the world. With good reason. Microsoft™ FORTRAN-80 is the most complete micro FORTRAN you can buy. It has all of ANSI-66 FORTRAN (except COMPLEX data), plus unique enhancements for use in the microcomputer environment. An extensive library of single and double precision scientific functions, too. Available for CP/M, ISIS-II, OASIS or TEKDOS. $500.

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Circle 35 on reader service card

Three questions about digital in-circuit test systems other ATE companies hope you won't ask.

Introducing GenRad's enhanced 2270—the first analog/digital in-circuit test system with all the right answers.

Our new system is so unique, so advanced, so accurate, it begs to be compared with every other system on the market.

To make your comparison a little simpler, we'll give you the three toughest questions you can ask about any test system.

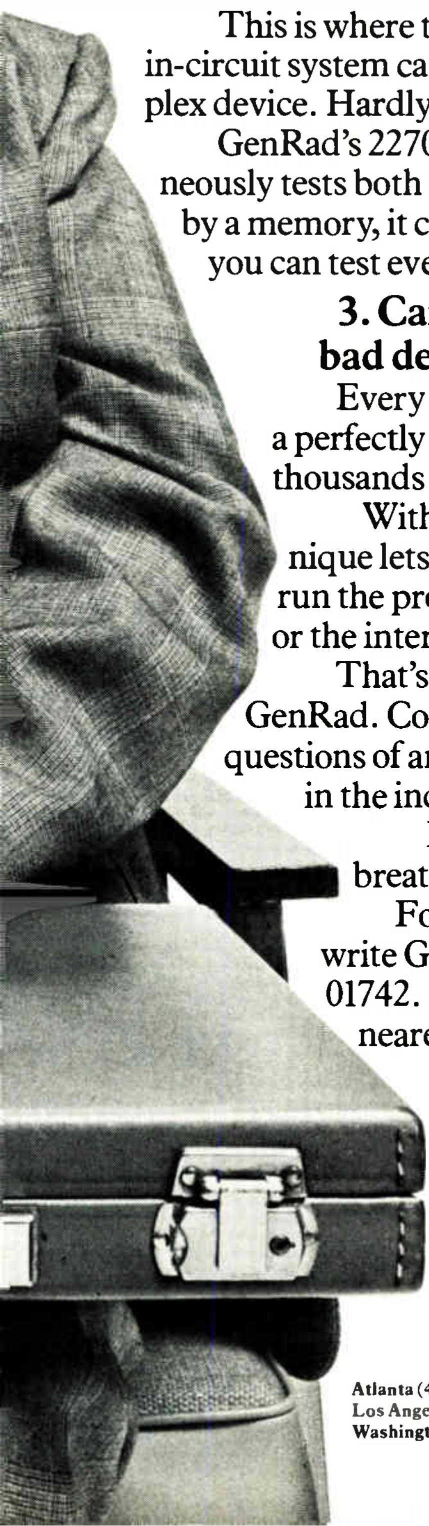
1. Can your system test MSI and LSI boards?

This simple question will weed out quite a few systems right off the bat. Most systems can power an MSI or LSI, but that's it. GenRad's 2270 accurately verifies the functionality of a device.

2. Can it test each device comprehensively? Simultaneously?

This is where the competition starts dropping by the wayside. Almost every other in-circuit system can only test a single pin at a time. That's hardly the way to test a complex device. Hardly the way to test a board quickly and efficiently.

GenRad's 2270 uses a new technique called "parallel stimulus/response." It simultaneously tests both the inputs and outputs of each device. And since each pin is backed by a memory, it can deliver a complete stored pattern sequence in a burst. That means you can test every device comprehensively. Efficiently. Simultaneously.



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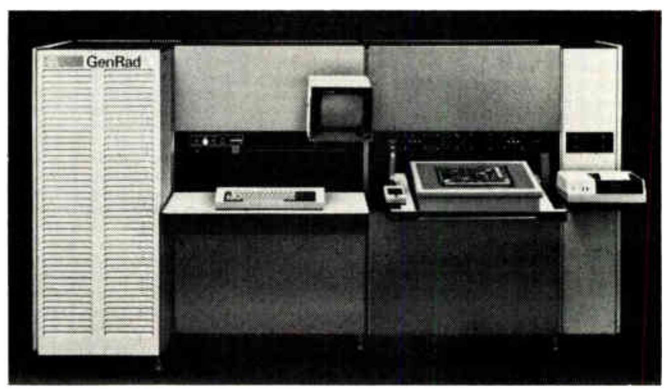

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Circle 37 on reader service card

All-silicon devices will match SOS in performance

by John G. Posa, Solid State Editor

Laser anneals polysilicon on silicon dioxide; technique could lead to three-dimensional ICs

Researchers at Texas Instruments Inc.'s Central Research Laboratories have succeeded in fabricating MOS devices in laser-annealed polysilicon on silicon dioxide. Not only will the devices have the speed and density of those fabricated on sapphire, but the all-silicon construction could lead to true three-dimensional circuitry.

A paper by the Dallas lab will be one of the highlights of the International Electron Devices Meeting in Washington, D. C., Dec. 3–5 (see also the following story). The TI researchers say they have fabricated both enhancement- and depletion-mode n-channel MOS field-effect transistors with various width-to-length ratios, as well as 7- and 11-stage ring-counter circuits. Eventually very large-scale integrated circuits may use this technique.

Effect on sapphire. With performance comparable to silicon on sapphire, cheap and easily grown oxide may replace SOS. The excellent isolation of the sapphire substrate has inspired large but as yet unavailing efforts to reduce the cost of materials for commercial devices.

Another more subtle implication stems from the fact that, unlike metal, polysilicon supports further growth of silicon dioxide. Entire circuits fabricated in annealed polysilicon may be covered with oxide and a subsequent layer of polysilicon can be deposited atop this for another level of circuitry, and so on.

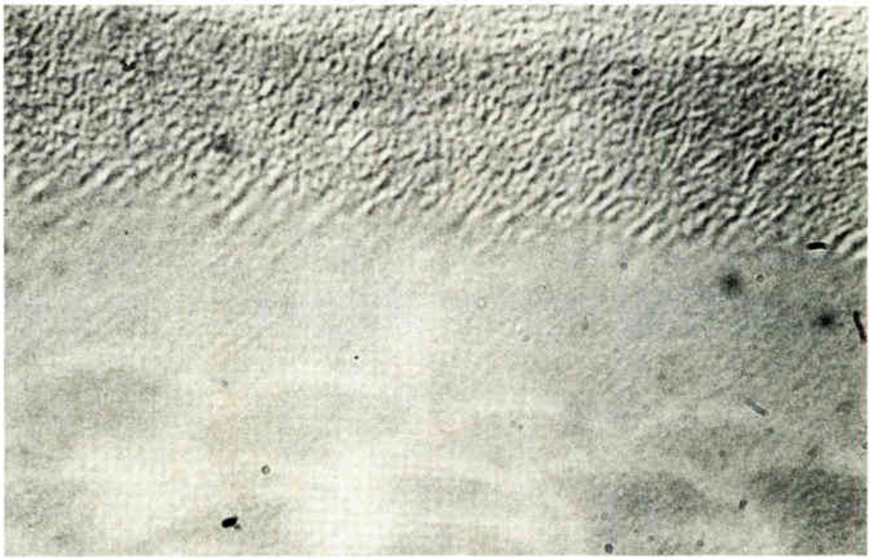
Therefore, while single-crystal silicon made possible the two-dimensional integrated circuit, polysilicon may be responsible for truly three-dimensional ICs. Al F. Tasch Jr., manager of the lab's VLSI technology branch, acknowledges that such a prospect "is entirely possible."

Unannealed polysilicon is made up of randomly oriented crystal grains on the order of 500 angstroms across. Carrier flow is impeded at each grain-to-grain boundary and the resulting low mobility would yield a poor device at best.

Armed with a pulsed frequency-doubled neodymium-yttrium-aluminum-garnet laser, TI scans the polysilicon surface to induce localized melting. The grains recrystallize with much larger dimensions so the number of interfaces is reduced and mobility is enhanced. With this setup, researchers have observed grains as large as 10 micrometers across (see photograph).

To build what it calls silicon-on-insulator MOS FETS, TI begins with a single-crystal p-type silicon substrate. On this, it grows a 1-μm-thick oxide layer and then deposits a 0.5-μm film of undoped polysilicon film. The samples then go onto an X-Y translation stage, which is heated to 350°C while a stepping motor moves it in synchronization with the pulsed laser.

Implantation. Then the polysilicon is selectively etched down to the oxide level to isolate islands for each transistor. Boron ions are implanted to form the channel, which is covered with a thermally grown 500-Å gate oxide. A polysilicon gate is deposited on the gate oxide and implanted with phosphorus. It also is used for a self-aligned



All silicon. Depositing polysilicon on silicon dioxide (top) and then annealing the deposited material (bottom) gives TI a large-grain film with improved mobility.

arsenic ion implantation of the source and drain.

The researchers discovered that the highest mobilities were obtained when a square grid pattern was plasma-etched into the oxide before polysilicon deposition. The square, 11 μm on a side and 0.1 μm deep, encouraged more uniform recrystallization of the polysilicon.

TI also annealed previously implanted polysilicon and will report the results in another IEDM paper. Implanted silicon doped for gates and interconnections also has a small-grain structure, so it too can stand recrystallization for mobility improvements—especially as design rules are scaled down. By laser-annealing, sheet resistance was lowered up to three times more than it was by thermal annealing.

Memories

Intel to disclose 16-K static secrets and to release soft-error data

Clearly one of the highlights of this year's IEDM presentation will be Intel Corp.'s disclosures about its 16-K n-channel MOS static random-access memory, a design that will become a product next year. Though discussed at the International Solid State Circuits Conference in Philadelphia [*Electronics*, Feb. 15, p. 122], Intel designers will be much more specific this time.

In fact Richard Pashley, manager of static RAM design and development of the Santa Clara, Calif., chip maker, nervously admits that "more will be said about Intel's static RAM technology than ever before." Moreover, his company will release soft-error reliability data.

Such an exposé is dearly sought. The company's hustle has netted it a one-to-two-year lead in fast n-channel technology. It enjoys a corner on the market for such parts—and several other MOS houses, poised to pounce on that commanding position, are eager to know just how Intel does it.

To obtain 16-K densities, Intel designers were forced to replace the depletion-mode load transistors used in the cells of their 1- and 4-K fast static memories with doped polysilicon resistors. The transistors simply consume too much real estate.

Speed. Unexpectedly, the change did not extend the access time. "The polysilicon loads do not affect speed," says Pashley. Indeed, using rather conservative 4-micrometer design rules, the memory sports a respectable 40-nanosecond typical access time, while consuming 0.5 watt.

Two self-aligned levels of polysilicon give device density at least double that achievable with single-level polysilicon. The added upper level of the Intel RAM is implanted with arsenic to form the high-resistance pull-ups, but it is also selectively doped for low-resistance interconnections. The second level makes a self-aligned direct connection to the first polysilicon layer, which, as usual, forms gates. Projection printing with a 2-μm misalignment tolerance is used throughout the process.

Two implants. Smart money is betting that Intel uses multiple ion implantations for the 16-K static, and it wins. In fact, the company needs only two threshold-adjusting channel implants to build the four transistor types listed in Table 1.

The chip's power-down feature is made possible by one of those types, a zero-threshold switching transistor. Driven by the chip-select buffer, the switch turns off nonessential blocks of internal circuitry and power use is cut to one seventh, about 70 milliwatts, with no penalty in access time.

As for errors, a modern depletion-load static RAM can expect no alpha-induced errors in 1,000 hours of operation, given the layout rules implied in Table 2. Alpha hits are more easily assimilated with depletion loads because cell holding currents and capacitance are higher.

The soft error rate for the polysilicon-load 16-K memory has been held to less than 0.05%/1,000 hours. The chip was also stressed to predict threshold shifts due to the trapping of hot electrons in the gate oxide, and it was found that it would take almost 60 years for a 5-millivolt shift to occur. **-John G. Posa**

TABLE 1: COMPARISON OF TRANSISTOR TYPES

	Channel implant	Threshold voltage (V)	Circuit application
Enhancement-mode	boron	0.7	pulldown device
Depletion-mode	arsenic	−3.0	high-performance load
Depletion-mode	arsenic, boron	−1.5	low-power load
Zero-threshold	none	−0.2	power-down device

TABLE 2: RELIABILITY AND RELATED FACTORS

	Single polysilicon depletion load (1979)	Double polysilicon resistor load (1979)
Soft error rate	0%/1,000 hr	< 0.05%/1,000 hr
Cell size	3.0 mil²	1.5 mil²
Cell node capacitance	~ 12 fF	~ 50 fF
Range of load resistance	5–10 MΩ	50–200 MΩ

Solid state

Silicon nitride cap keeps implants in place on gallium arsenide

Working towards the goal of a single-chip X-band receiver, TRW Inc. has developed an improved method of doping gallium arsenide integrated circuits. So confident is the firm that it has licked a major problem associated with the highly temperamental material that it predicts it will have its IC receiver in about a year.

The GaAs material is desirable for its inherent low-noise characteristics and its frequency limit of 30 to 40 gigahertz, which is well above the 5.2-to-10.9-GHz boundaries of the X band where the U. S. Navy plans to use the single-chip receiver. Moreover, TRW anticipates that its implantation technique will make possible digital logic, as well as the analog devices found in the receiver.

"We have already fabricated and successfully operated the basic on-chip building-block circuit," says Thomas G. Mills, referring to a four-quadrant analog multiplier. Mills is senior scientist at TRW's Microelectronics Center, in Redondo Beach, Calif., part of the firms's Defense and Space Systems Group.

Ion implant. The key to the metal-semiconductor field-effect-transistor configuration is the ion-implantation method the center devised for GaAs. The precisely controlled introduction of impurities possible with ion implantation can provide a variety of circuit elements on a single IC—and the X-band chip must pack in many different receiver circuits.

However, there is a stumbling block in ion-implanting GaAs wafers. "Any time you implant wafers with ion energy, you get damage—especially on the surface with gallium arsenide," says Mills. "Silicon can be annealed at 800°C, but that's not the case with GaAs," which dissolves at 350°C.

As Mills describes the problem, the catch is not so much repairing the crystal damage as sealing the surface of the wafer so that implants remain where they are supposed to. For this sealing, he and his fellow scientists have developed a cap of plasma-deposited silicon nitride.

Benefits. Among other advantages, Si_3N_4 adheres well to GaAs and can be deposited at low temperatures. Also, its 90% doping efficiencies approach those of silicon—that is, 90% of the performance possible from the amount of implanted impurities is actually realized.

Mills claims that the plasma deposition process permits reproducible performance characteristics, as in ion-implanted silicon. In the analog multiplier, for example, the contemplated low noise figures can be maintained, he says. Tests at 8 GHz (the middle of the X band) show losses of only 3 decibels.

In an area of only 40 to 50 mils, the multiplier has operated at up to 10 GHz, says Mills. The researchers are working on improved performance through such changes as moving sources closer to gates for faster response time. They also are tweaking the circuit to get better gain—"in the neighborhood of going from a few decibels' conversion loss to a few decibels' conversion gain," Mills explains.

At the same time, they are designing the other receiver elements, including amplifiers, oscillators, modulators, and demodulators. In mid-1980, all the components will come together on a single chip, Mills predicts, giving the Navy the low-noise receiver that an IC configuration promises. -Larry Waller

IEEE

President seeks support from 1980 board that 1979 group denied to his candidacy

As the first petition candidate to win the IEEE presidency, Leo Young may now have to build support from the 1980 board of directors that he did not get from the 1979 board for his candidacy. In addition, in order to accomplish anything, he will have to establish a close working relationship with the executive committee, which will be chosen in New Orleans this weekend.

At this point it is not clear if the new president will enjoy the full support of that committee, which plays a crucial role in the development of policy. Although as executive vice president he currently holds the No. 2 elective position, Young was challenging the IEEE establishment simply by running for president as a petition candidate. As a result, his standing in the institute's hierarchy is unclear.

Nor do the results offer much of a mandate to guide the executive committee. Young, a staff consultant at the Naval Research Laboratory, won decisively enough—22,947 to 18,544 for board candidate Burkhard H. Schneider, vice president for divisions at Detroit Edison—but the total vote represents only 27½% of the ballots.

Moreover, the two constitutional amendments, which Young supported, went down to defeat. They provided for direct election of the vice president for professional activities and of members of the Nominations and Appointments Committee, and neither approached the two-thirds majority needed for passage; in fact, neither received a plurality.

Member-oriented. Nevetheless, the amendments represent the kind of thrust that Young wants to introduce into the IEEE's policies—what might be termed member-oriented professional activities [*Electronics*, Aug. 30, p. 90]. Schneider represents a more conservative approach, close to that reflected by the board of directors and its executive committee. Similarly, the unopposed board candidate for executive vice president, C. Lester Hogan, a former Fairchild Camera and Instrument Corp. executive, is typically cast as a conservative.

List. Already the Nominations and Appointments Committee (itself appointed by the board) has a list of two candidates each for the various vice presidencies that compose the executive committee. The board's elected members—the heads of the regions and the technical divisions, the new president and vice president and the two immediate past presidents—will be considering that list in New Orleans, although they are free to bypass the suggested candidates and choose their own. One well-positioned observer calls chances for a slightly more liberal executive committee a tossup.

Young agrees with incumbent president Jerome J. Suran on the relative powerlessness of the office. "The president does not have the power to set major policy without the approval of the board, and approval of the executive committee is needed for implementation," Suran notes.

However, Young has long been active in IEEE professional and technical affairs, and he speaks hopefully of his ability to be persuasive with the board members and to unite the feuding factions within the general membership when he takes office Jan. 1. He sees one way of reconciliation being *ad hoc* groups representing the spectrum of membership, including the establishment. These groups would be charged with fairly specific assignments by the board, he says. **-Benjamin A. Mason**

What happened to Feerst?

Low turnouts are hardly a surprise in IEEE elections, but one factor that did surprise observers this year was the slight effect Irwin Feerst apparently had on the returns. A petition candidate in several recent elections, Feerst entered this year's campaign, but a heart attack forced him to withdraw.

The causes with which he associates himself are distinctly on the liberal side of IEEE politics, yet he endorsed the more conservative of the two remaining candidates—board nominee Burke Schneider. However, he was unable to deliver his constituency to Schneider.

Working through his newsletter, the Committee of Concerned EEs, Feerst mounted a strong *ad hominen* attack on the successful candidate, Leo Young. Since Young's positions are closer to his than are Schneider's, it may be that he simply confused his followers, who then sat out the election. It is also possible his endorsement drove some conservatively oriented IEEE members out of the Schneider camp because his stamp of approval is outright anathema to them.

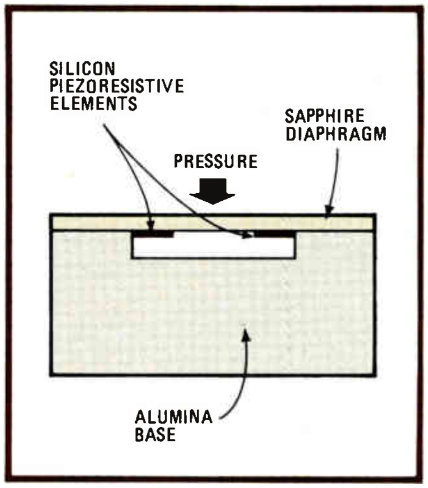
Not that Feerst agrees with such assessments. He characterizes the election as a battle between two political machines and speculates that his constituency simply is so disillusioned that it did not vote. "I did get on the ballot," he notes, and his illness meant not only that he had to withdraw his nomination but "I also was not as vigorous in the campaign as I might have been." He plans to continue his activities. As for entering next year's campaign, he says simply, "I don't know—we'll see."

Components

Transducer sports SOS diaphragm

A new role for silicon on sapphire is about to appear in the commercial arena. Conrac Corp.'s Systems-West division has developed an SOS transducer whose impressive temperature range and high sensing accuracy are the result of the material's good electrical isolation, low power dissipation, and high thermal stability.

SOS has been largely relegated to use in semiconductor memories and logic and microwave integrated circuits. The Conrac development may open up applications where high performance is needed in hostile environments.



Precious stuff. For a high-performance transducer, Conrac has developed a sapphire diaphragm with epitaxially grown p-type silicon strain gages. The unit's upper temperature limit is 475°F.

An outgrowth of a military development, the series 4720 transducer has a patented sensing element that consists of a sapphire diaphragm with silicon piezoresistive strain gages grown epitaxially (see figure). The diaphragm is glass-bonded to an alumina base.

There are two versions, both offering several pressure ranges between 0 and 1,000 pounds per square inch absolute and an output of 50 ±2 millivolts. Both have an extremely wide temperature range of −65° to +475°F, with one offering very high accuracy of within ±0.3% of full-scale value over a 375°F compensated temperature range and the other accurate to within ±4%.

Better. The upper temperature limit is more than 200°F higher than that of typical transducers using an all-silicon diaphragm, and the accuracy shows similar improvements. Silicon units are limited to about 250°F by large thermal drifts caused by diode leakage. Thermal expansion also has been a problem, necessitating complicated graded seals between the diaphragm and the stainless-steel casing. The excellent insulating quality of sapphire eliminates the diode leakage in the 4720 up to about 500°F. Because the

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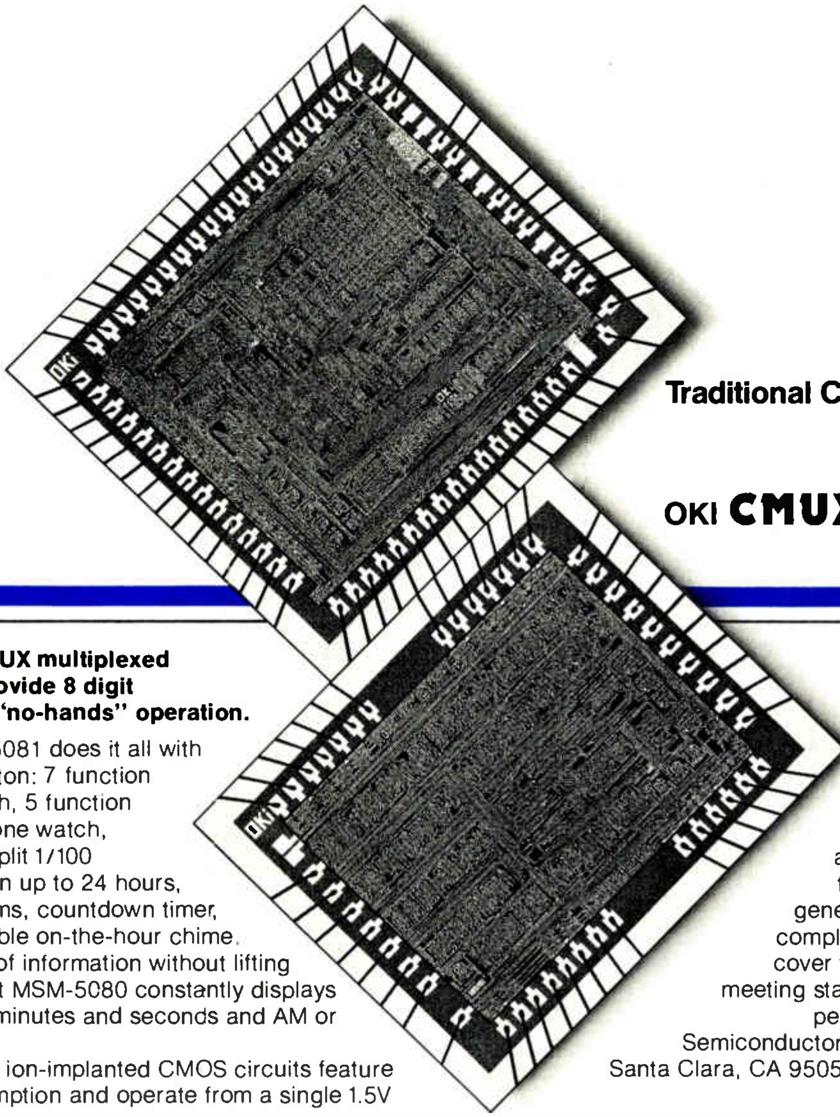

Two new OKI CMUX multiplexed watch circuits provide 8 digit multifunction or "no-hands" operation.

The 8 digit MSM-5081 does it all with the touch of a button: 7 function primary time watch, 5 function secondary time zone watch, with stopwatch split 1/100 second information up to 24 hours, two separate alarms, countdown timer, and a programmable on-the-hour chime.

And for a lot of information without lifting a finger, the 8 digit MSM-5080 constantly displays date, day, hours, minutes and seconds and AM or PM information.

Both of these ion-implanted CMOS circuits feature low power consumption and operate from a single 1.5V supply.

OKI's new CMUX circuits reduce assembly costs and improve reliability.

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Circle 43 on reader service card

OKI

material is so stable thermally, it is relatively unaffected by large thermal expansion in the adjacent p-type silicon gages.

There are additional benefits in using SOS. The monolithic construction imparts a high degree of insensitivity to shock and vibration. Also a factor is the high strength-to-weight ratio of sapphire, about twice that of steel. The resulting error is given as less than 0.004% per gravity of vibration up to 20 g.

To keep output well within the linear portion of the stress-strain curve of the diaphragm, the transducer is designed so that the 50-mv full output is produced at only 5% of the sapphire's ultimate yield strength. Repeatability, hysteresis, and creep—all functions of the level of stress—are therefore minimized, says the company.

Low stress, of course, means longer transducer life. Conrac says test units cycled 1 million times at 300% of the rated pressure ranges showed no effect on performance. In fact, the manufacturer is confident enough of the pressure-range capability to be prepared to offer custom versions handling up to 6,000 psia.

Initially intended for fuel- and oil-pressure monitoring, the device also will be aimed at the process-control market. Of course, superior performance does cost: in 100-lot quantities, the more accurate version costs $1,900 each and the other $1,200 each. **-Roger Allan**

Aerospace

Do cosmic rays spell death for VLSI?

Cosmic radiation could cause major obstacles to the use of very large-scale integrated devices in space, a U. S. Air Force researcher contends. Analysis shows that rays will cause device failure, as well as soft errors like those caused by alpha particles, says Patrick J. Vail, project scientist at Rome Air Development Center.

"One thing is clear: without a major breakthrough in circuit hardening, many systems now on the drawing board will have to abandon VLSI for space applications," Vail said in a paper at a digital avionics conference in Forth Worth, Texas, this month. However, other scientists dispute this contention, arguing that the redundant circuitry possible with VLSI will lead to solutions.

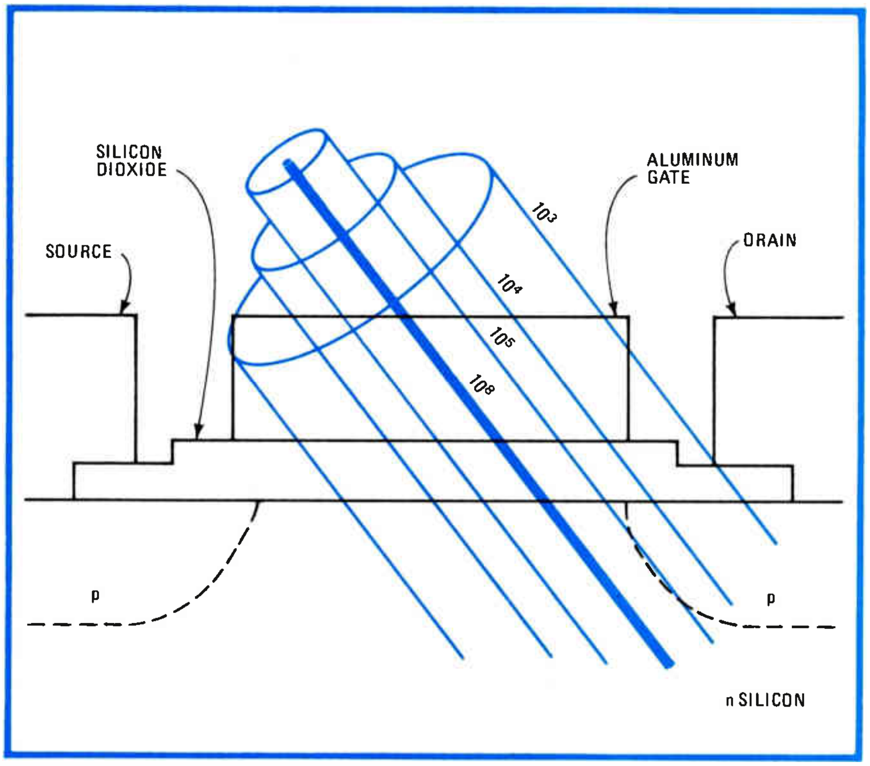
Vail maintains that shrinking VLSI geometries are the crux of the problem. A cosmic ray in space that might pack a 10^8-rad wallop at its core (see figure) could exceed sensitive VLSI design tolerances and produce hard errors in the form of destroyed transistors.

Since VLSI transistors will operate on reduced switching margins, they will also be more vulnerable to soft errors, he says. It takes fewer ionized electrons to cause a spurious change of state in a VLSI device compared with LSI and larger devices.

Coauthor John H. Bradford, also at the development center at Hanscom Air Force Base, Mass., provided an analysis that permits Vail to predict as many as 25,000 soft errors and 50 or more hard errors per year in a megabit memory with 0.5-micrometer geometries—all caused by cosmic rays. A comparable LSI system would experience 3,650 soft errors, he says.

Not all in the research community share Vail's pessimism, however, not even at IBM Corp.'s Watson Research Center where at least one researcher has warned of cosmic-ray damage [*Electronics*, May 10, p. 34]. "Whether you're talking space or earth, the [cosmic-radiation] error rates are going to be very, very small and are the kinds that can easily be coped with by using error-correction techniques," declares John Armstrong, director of physical science at the Yorkstown Heights, N. Y., center. He adds that the hard errors are still a theoretical issue.

Fault tolerance. Vail agrees that his analysis is theoretical and that fault-tolerant techniques possible with an abundance of VLSI circuitry holds the most promise for coping with cosmic rays. However, he notes, his analysis is based only on one type of error caused by heavy cosmic ray ions like iron. Other yet uncharac-



Strong dose. A cosmic ray passing through a silicon device with channel lengths of less than 0.6 μm would have its strongest radiation at its center and "cylinders" of lesser strength.

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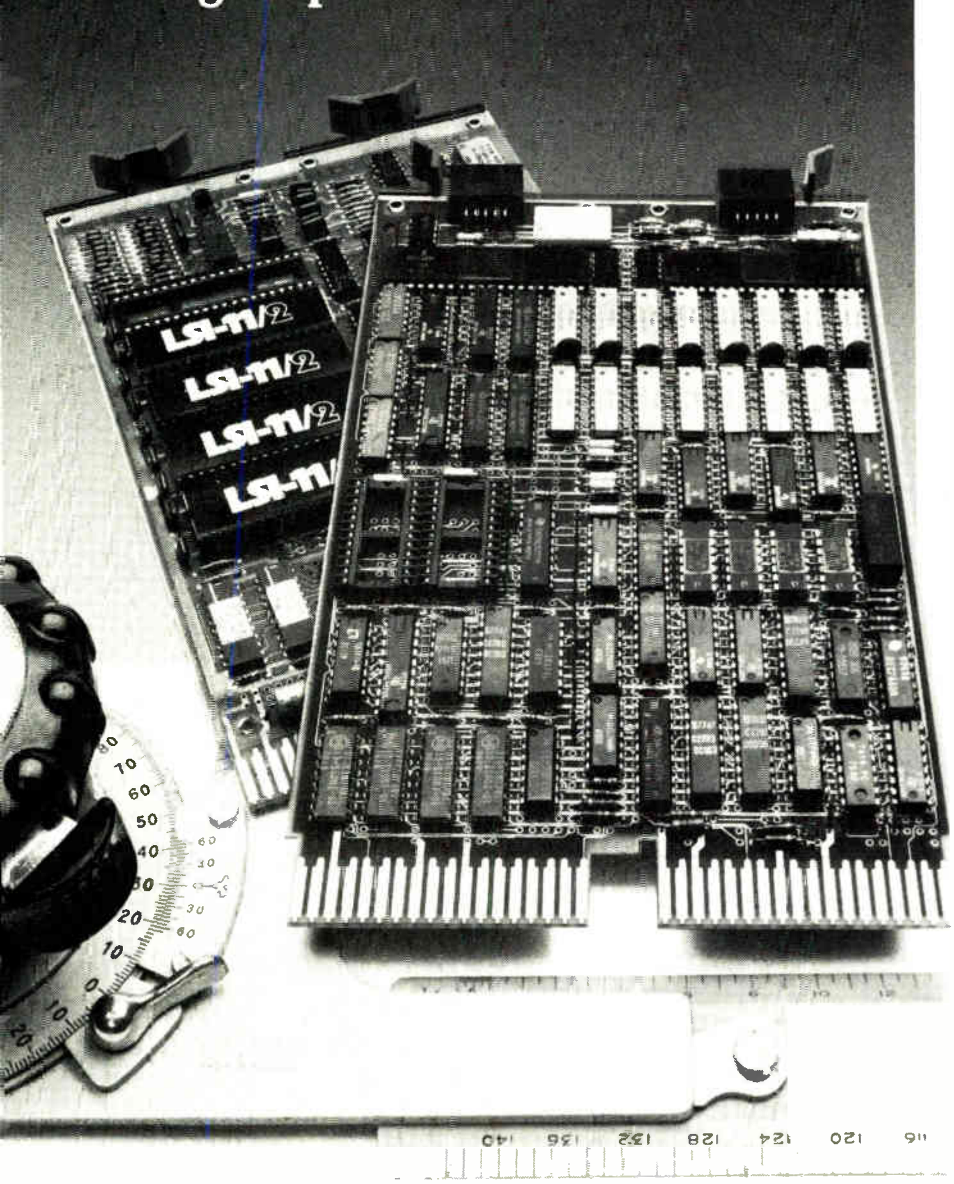

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It took the minicomputer company to make micros this easy.

Circle 45 on reader service card

digital

terized failure mechanisms could crop up, he warns.

Although heavy ions make up less than 1% of cosmic rays, today's circuit-hardening techniques are ineffective against their heavy doses, he says. Shielding might work, but it also would slow down the light, highly energized protons that otherwise would zip through a VLSI device without causing a cell upset that results in a soft error.

Yet another possible corrective approach lies in the circuit-design tricks of the kind that combat alpha radiation emitted from package materials in LSI devices. Vail, however, doubts that such techniques alone will prevent VLSI errors or failures in space. **-Wesley R. Iversen**

Displays

40-character LCD is made like ICs

Inside. Forty-character LCD unit uses polyimide flexible circuit that connects display and six custom driver ICs and meets all system-bus requirements.

Borrowing a leaf from the book of semiconductor makers, a new firm specializing in liquid-crystal displays is about to enter production with a flat-panel 40-character device. The LX140 from Kylex Inc. is fabricated with precision photolithographic techniques that give a five-by-nine-dot matrix, thereby achieving better visual definition of the characters than five-by-seven-dot LCDs.

The new display, from the Mountain View, Calif., unit of Exxon Enterprises Inc., uses complex multiplexing to drive its 40 characters. It also incorporates a custom complementary-MOS driver chip that simplifies interfacing in microprocessor-based applications—its intended marketing target.

Most LCDs are patterned using screen printing. By employing photolithography, Kylex achieves clearly defined dots separated by less than 0.002 inch. The closer the dots, of course, the more the characters look as if they were formed from solid lines. Also, the two extra rows of dots in the matrix give the full ASCII character set, including lowercase descenders. As with five-by-seven-dot LCDs, there is another line of dots for underlining (see photo).

As in semiconductor wafer fabrication, "the process is readily adaptable to automation," notes Terry Leeder, marketing manager. He anticipates that the LX140 will lend itself to high-yield production and will drop considerably in price as the company moves down the semiconductor learning curve.

Available in evaluation quantities on a six-week basis, the LX140 costs $299, or $199 in 100-unit lots. It operates from a single 5-volt supply and has a typical power drain under 400 milliwatts. It is aimed at word-processing applications where only a single 40-to-80-character line need be displayed.

Chip. For direct interconnection with microprocessors through one of the popular peripheral interface chips, the display has a custom C-MOS integrated circuit, called the LCID for liquid-crystal integrated driver. Six are in each display.

In its 174-by-204-mil area, the LCID packs a data input/output buffer, character- and row-address decoders, 35 waveform generators for the necessary 35 column or address outputs, seven 5-by-10-bit random-access memories for the characters, and seven 5-bit data buffers. On-chip refresh circuitry provides continuous sequencing of the row addresses, thereby giving continuous refresh of the RAM data to the display.

The boost in character count over the usual four to six in the typical LCD application does exact a price. Kylex president Garrett Stone points out that the LX140 has had to forsake direct-drive techniques for matrix multiplexing.

A square-wave pulse train is time shared among the display's rows and columns. Where the scanning voltage equals an element's threshold voltage, that element switches on.

New materials. Time-sharing a driving voltage among many characters results in short duty cycles, and the more characters the shorter the cycle. The root-mean-square voltage that activates each element is smaller, so Kylex developed new liquid-crystal materials to respond to these small rms voltages.

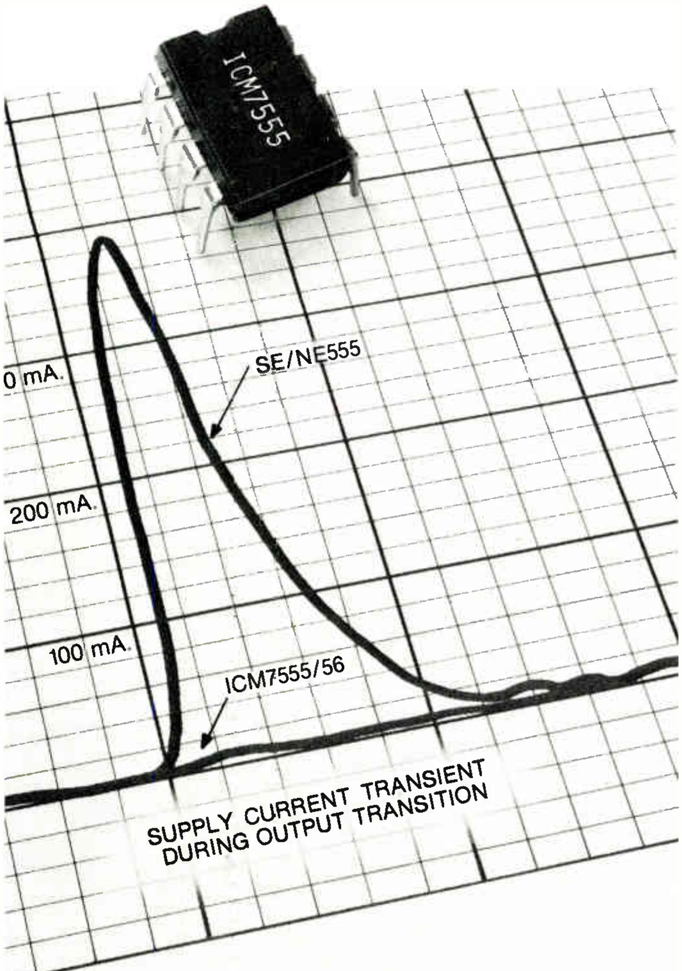
Other companies also are looking into multiplexing setups for LCDs. But a major question with such complex multiplexing schemes is whether they limit applications to single and double lines of characters. Going to more than 40 characters in a line or adding lines of characters might require a tough tradeoff: weighing additional power sources versus even more fiendishly complicated multiplexing with a single source. **-Bruce LeBoss**

Packaging & production

UV exposure system goes submicrometer

A line width of 0.425 micrometer in a surface-acoustic-wave filter's interdigital transducer is achievement enough in any league. However, these lines are the product of what amounts to off-the-shelf photolitho-

"WHY DOESN'T SOMEONE BUILD A CMOS 555?"



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Guar. Max. Osc. Freq.	500KHz	150KHz
Operating Temp Range	−20° to +70°C	0° to 70°C
Output Risetime	40ns	100ns

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The ICM7555/56 single and dual precision timers are function-for-function, socket-for-socket replacements for the SE/NE 555/556 timers in 95% of all applications. And, they require no power supply decoupling or voltage decoupling capacitors.

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City _______________ State _______________ Zip _______________ graphic equipment using an ultraviolet light source.

To fabricate the SAW filter (below), researchers at the U. S. Air Force's Rome Air Development Center fitted a garden-variety step-and-repeat mask-making system with a broad-band UV light source, a 365-nanometer filter, and a 10× reduction lens. Some private companies' laboratories are taking the same tack as RADC, and are achieving submicrometer lines also.

Pushing the specs. That the combination went so far below the 1-μm minimum dimension usually attributed to UV equipment suggests that performance specifications have been conservative, says Jose M. Silva, engineer in charge of the project at Hanscom Air Force Base, Bedford, Mass. "I don't believe that 0.425-μm lines are the end of the story. We're going to keep pushing that limit, so stay tuned."

Of course, a SAW filter presents no registration problem since its features are defined by a single mask, and the key to production-line submicrometer dimensions is alignment of successive layers. Also, Silva points out that his system requires wafers with less than 2-μm deviations from a plane because of limitations in its depth of focus. He suggests that several sophisticated refocusing devices recently put on the market may be the means of sidestepping this limitation.

Arguing that depth of focus will limit optical lithography's usefulness in semiconductor production is Philip D. Blaise, supervisor of semiconductor processing technology at Westinghouse Electric Corp. in Pittsburgh. Like RADC, Westinghouse is using an old D. W. Mann step-and-repeat system. The primary modification is a company-designed, highly collimated light source, whereas RADC uses a Tamarack Scientific Co. source.

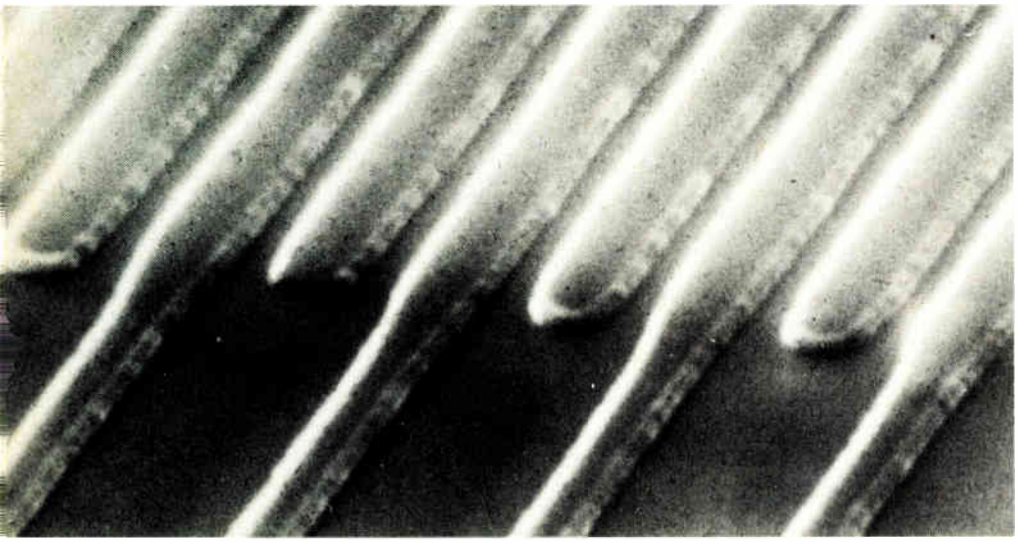
Operated largely as a contact printer, the Westinghouse setup has produced 0.7-μm line widths. However, maintaining focus across textured semiconductor substrates "gets to be pretty tortuous," says Blaise, who does not think the problem is going to be resolved.

No choice. Still, with electron-beam and X-ray lithographies still in their infancy, semiconductor makers "have no alternative" but to invest in advanced optical equipment to stay competitive, he says. Westinghouse has four such machines on order, he adds.

Another group using a fine-line UV optical system is at the United Technologies Research Center, East Hartford, Conn. Engineer Robert A. Wagner says the center designed an optical system around the same Tamarack illuminator Air Force researchers adopted but used a Nikon lens instead of a Tropel lens.

Wagner says his system has produced good-quality 0.7-μm lines for SAW filters. Under consideration, he says, is the addition of a laser interferometer to aid in positioning and registration. **-Linda Lowe**

Going down. A careful combination of available elements gave Air Force researchers a UV lithography system that produced a SAW filter with a minimum line width of 0.425 μm.



Commercial

Accuracy questioned in stress analyzers

Controversy over accuracy has not stopped lie-detector manufacturers from bringing voice-stress analyzers out of police interrogation rooms and into personnel offices. Now solid-state technology has brought the analyzers within reach of the average consumer—some can be mail-ordered for as little as $149 and an inexpensive wristwatch version is in the works.

Unlike polygraph machines, voice-stress analyzers work without having to wire up the person being questioned. Operating under the assumption that voice stress indicates untruth, they look for imperceptible changes in the frequency modulations or harmonics in the voice that signify stress.

However, not everyone familiar with the operation of the machines agrees that they work [see "Do they tell the truth?"]. Nor will the companies marketing them identify the integrated circuits used.

Ads. For example, advertisements for a mail-order "truth machine" in major newspapers and magazines (including *Electronics*) say, "When you ask a direct question you deserve a straight answer." However, getting a direct answer out of the company marketing the device, Telestar Inc., also known as Microtronics, is not so easy.

The Wormleysburg, Pa., company's ads claim that a solid-state voice-stress analyzer can tell whether what you are hearing is "less than the truth." The company will not disclose who is manufacturing the

No. 2

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

What's new in BIFETs™?

MIL-TEMP AND GUARANTEED DRIFT.

MICRO-DAC™ D/A converters get you off the bus easy

Wickersham on ROMs

What is a wizard

Wisdom of single-minded COPs

Microcomputers for the real world

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NATIONAL ANTHEM

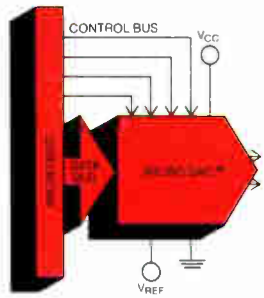
New MICRO-DAC™ Series is the easiest way to get from D to A.

National's DAC 1000 is the first of a series of four quadrant multiplying D/A converters which easily interface to a μP.

The DAC1000 is the only microprocessor-compatible 10-bit DAC that is truly μP-compatible without the need for any support chips. In fact, it looks like a memory location or I/O port with all control functions right on the chip. So you get easy interface with any 8 or 16-bit data bus.

The "Best Straight Line" Myth. The competitions' linearity spec is based upon a "best straight line," which doesn't correspond to real world applications, and can mean several adjustments to find the "best straight line." The competitors benefit by shipping these lower accuracy devices. You lose.

With National's "end point" linearity spec only two adjustments are needed – Zero and Full Scale; set these, and the linearity specification is met. Thus, National's linearity specifications ease calibration of the system. In addition, where low reference voltage or reference voltage changes are required, linearity is maintained even with a 10 to 1 reduction.



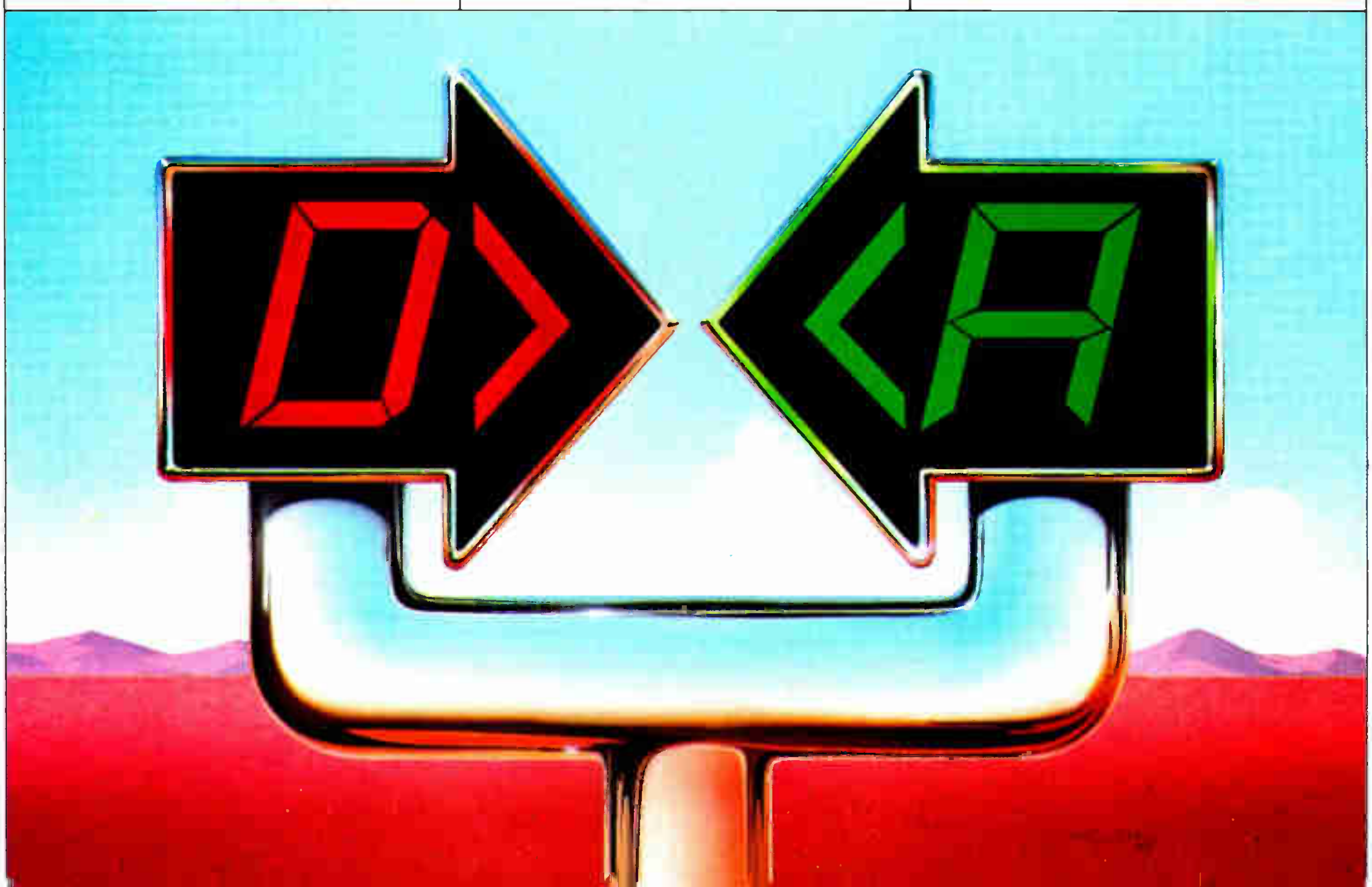
It fits into a lot of places and takes up a lot less space. The MICRO-DAC1000 Series is used primarily for building D/A conversion systems. But these DACs can also be used as building blocks for digitally controlled amplifiers, alternators, active filters, and even oscillators. They're also more flexible than any DACs around – 4 quadrant multiplying, double buffered, single supply operation from +5V to +15V, right or left justified data format, micro power operation (2mA max.), and output current mode setting time of 500ns.

In the 20 pin package they're only .3" wide compared to .6," so they're easily inserted and use a lot less space.

If you don't need μP interfacing, National's still got you covered. The DAC1020 and DAC1220 are 10 and 12-bit DACs without all the μP interfacing. And they still offer application flexibility along with improved linearity.

If you're already using AD7520, AD7521, AD7530, AD7531, or AD7533, National's DACs are direct replacements. They're also priced at least 30% lower and, in some cases as much as 300% lower. These inexpensive DACs start at $4.00 at 100 pieces, and because of National's volume capacity, no one can sell for less.

The MICRO-DAC Series opens up a whole new world for design engineers. Because National's D to A's are better from A to Z.



New Military Temperature Range BIFET™ Op Amps inducted into National service.

The inventors of BIFET Op Amps are in the military with the LF151, LF151A, and LF153.

In 1975, National Semiconductor invented BIFET technology. Because of their low bias current and high-speed performance, these op amps quickly became the new industry standards. But while the competition continues to imitate what National introduced, National has moved on.

Their latest offering is three new low-cost, high-performance military temperature range op amps – the LF151, LF151A, and LF153.

A single op amp. A lot of features. The LF151 and LF151A were designed to fill a long-vacant price/performance gap between the LF156H workhorse and the top-of-the-line LF156AH. And both models come with a solid list of guarantees over the −55° to +125°C temp range.

For example, the LF151A comes with a maximum input offset voltage of 2mV and a maximum input offset voltage drift of less than 20 μV/°C. You also get a minimum slew rate of 10V/μ sec and a bandwidth of 3MHz minimum. These parameters are 100% tested, including temperature drift, and are guaranteed with no exceptions, qualifications, asterisks, or footnotes.

Two into one equals a dual. For those who need a dual op amp, there's the LF153, simply two LF151's in the same package. Although National doesn't guarantee a maximum input offset drift spec, they do guarantee that the input offset voltage won't exceed 7mV over the full military temp range. Couple that with low bias current and high speed, and you have a very capable pair of op amps in a single 8-pin package.

The bottom line. Perhaps the most appealing features of these three new op amps, however, are their price and availability. All three models are available now – for as low as $3.25 for the single and $6.00 for the dual (100 unit price). For further information, call your local National distributor or sales engineer.

They'll show you how the people who invented BIFETs just made it easier to own them.

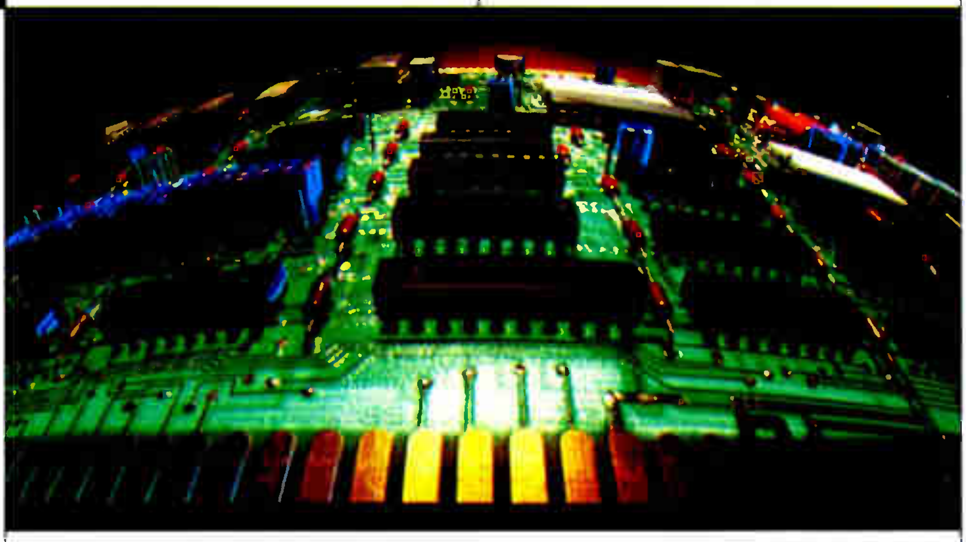
COP402 eliminates microprocessor overkill.

National's COP402 microcontroller handles little control processing jobs better than complex microprocessors. Granted, most microprocessors can do a lot very well, but when it comes to doing very little, it's a different story. In fact, those repetitive job applications like weather data transmitters, levelers for farm harvesters, transponders for divers, plastic extruders, asphalt mixers, egg sorters and even chicken pluckers being handled with microprocessors are really cases of overkill.

So National introduced two additions to their COPS family: the COP402 and COP402M. Each features a RAM right on the chip, direct I/O instructions, direct LED drive, easy interface to COPS peripherals (like the COP470), binary and BCD operations, direct KBD scan, and built-in address decoder.

In addition, the COP402 can scan switches, maintain real time, display in LED or VF, use external data from a read/write memory, and even function as a computer peripheral.

Considering all this, it's no wonder some people are wondering why they used a complex microprocessor in the first place.



BLC-8737 analogue I/O board simplifies MULTIBUS designs.

National's new BLC-8737 analog I/O board lets your MULTIBUS computer live in the real world of analog. It provides easy interface with that real world, because its built-in intelligence takes care of the analog functions automatically.

The BLC-8737 eliminates time spent writing conversion routines and the possibility of messing them up. Because onboard intelligence handles the complete analog conversion and scanning control. So you save considerable development cost and get to market quicker.

This analog I/O board is National's newest addition to its already broad line – over 75 different MULTIBUS compatible products in the family now. The line features CPUs, memories, controllers, analog and digital I/Os, peripheral controllers, rack-mounted systems, card cages, power supplies, cables, and other accessories.

Every BLC product also comes with a warranty four times longer than the competition's: a full 12 months.

National's MULTIBUS-compatible boards aren't just simpler. They're simply better.

National is seriously in the ROM business and is committed to capturing the major share of the market.

"At National Semiconductor, we're in the ROM business in a big way. We've made a major, no-holds-barred commitment to ROM production, and our fabrication lines are now ROM exclusive – not shared.

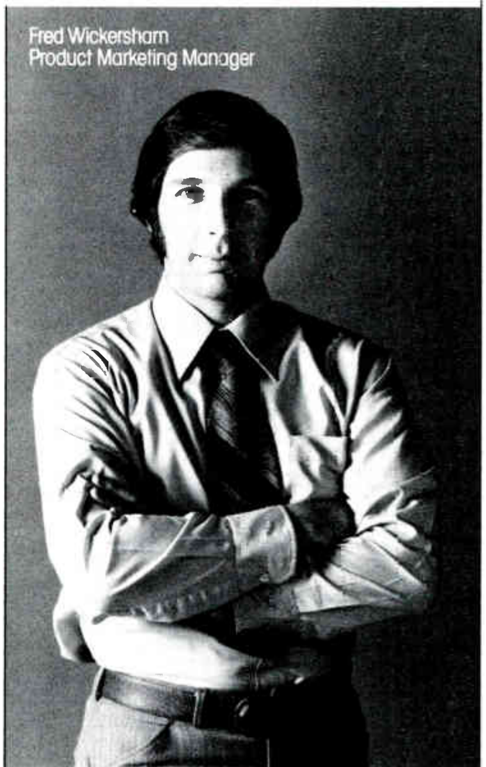
"And we're committed, also, to delivering every ROM we make on time. Without exception, thanks to our increased capability for volume deliveries. Which means no missed deadlines for our customers.

"With the number of products we offer, we're truly a first source company, and intend to stay that way. Our line features the MM52116, MM52132, and MM52164 ROMs, 16K, 32K, and 64K respectively. All are 2716 PROM-compatible, fully static, single ±5V products.

"Every model in our line has good, stable circuits which meet and, in many cases, exceed applicable specifications. Our prices are truly competitive, too,

"With the addition of a geared-up, production commitment to ROMs, National becomes a supplier for all your needs. We have focused our manufacturing capabilities on ROMs, no ifs, ands, or buts, and fully intend to dominate the marketplace.

"Call or write us here at National today and let us show you how committed we are."



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Just exactly what is a practical wizard? A practical wizard helps people. With his knowledge, his expertise, and his level-headed, sensible approach to solving problems. He is exceptionally gifted or clever at a specified activity, and uses his expertise for the benefit of others. He is, quite simply, the embodiment of "wizardry made practical."

This is the type of individual who works for National Semiconductor. And it's reflected in a broad line of semiconductor and semiconductor-related products. The wizards at National make everything from micros to mainframes, forgetting nothing in between. Be it digital, discrete, hybrid, linear, memory components, microprocessors, MOS/LSI, or optoelectronics, National has it.

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- 009 ☐ ROM MM 52116 Data Sheet
- 010 ☐ ROM MM 52132 Data Sheet
- 011 ☐ ROM MM 52164 Data Sheet
- 012 ☐ DAC 1000 Data Sheet
- 013 ☐ LF 151, 151A, 153 Data Sheet
- 014 ☐ New Data Acquisition Products Brochure

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The Practical Wizards of Silicon Valley

Do they tell the truth?

"Americans have deep faith in lie detectors, as in Santa Claus," says David Lykken, professor of psychiatry and psychology at the University of Minnesota's psychiatry research unit in Minneapolis. But using any of the devices is "equivalent to flipping coins," he adds. "For years, there was no evidence of accuracy—for or against the machines. Now there is some evidence, and it's negative."

"The only stress analyzers to have been subjected to impartial testing are those that measure frequency modulation," says Lykken, "and the published literature concludes that they cannot discriminate between stress and nonstress situations. Even if the tests could detect stress, one could not assume that stress indicates lying. Speaking the truth under stressful circumstances would typically show up as stress in these machines."

Lykken points as an example to rape victims who have to undergo lie detector tests before a case is allowed in court in some states. "70% of those rape victims flunk the test, not because they're lying, but because questions on the rape itself produce anxiety in the victims."

"No physiological response has been found to be unique to lying," says Frank Horvath, associate professor of criminal justice at Michigan State University in East Lansing. Horvath, who heads the state's polygraph licensing board, has conducted two studies comparing the accuracy of a popular stress analyzer with that of a polygraph machine. Under controlled circumstances using volunteers asked to lie about the value of numbered cards shown to them, the stress analyzer detected lies 38% and 20% of the time, compared to a polygraph machine's record of 92% and 76%. Horvath notes that the stress analyzer tested gives a printed readout, but "these new machines do not even provide a permanent record of the analysis," he says.

units for them or what integrated circuits are used, saying that patent rights have to be ironed out.

CCS Communication Control Inc., a New York City–based retailer of security and surveillance equipment, is almost as secretive about its voice stress analyzer—the 6-by-3-by-2-inch VSA VIII A. The unit filters and measures harmonic changes in a selected subject's voice.

Stress, not lies. CCS does not claim that its device can detect lies. "All our machine can do is detect stress," says Carmine Pellosie, vice president of the firm. "We encourage customers to take a course in interrogation techniques included in the $199 price of the machine. With the course and further experience, you can have as high as 85% accuracy detecting stress. Without the course your chances are 50-50," no better than guessing.

"The interrogation techniques are almost more important than the machine," says CCS chief engineer Sid Appleman. The operation of the VSA VIII A is quite simple.

The user must first adjust the circuitry to recognize the fundamental frequency range of the voice of the person under test. While talking to that person under nonstress conditions, the user tunes the analyzer with a one-knob control, until the number 20 registers on the light-emitting-diode display.

That number signifies that the machine is locked into the individual's fundamental voice frequency range. Appleman says that when a person experiences stress, normal harmonics disappear from the voice—that is, they shift so that they are no longer integral multiples of the fundamental.

A sensor/filter, possibly a tuned circuit programmed to anticipate those harmonic changes, measures their duration and intensity. The LED display indicates stress by a rise in the numeric value it displays.

The VSA VIII A has a built-in microphone, or it can be connected to an external mike or to a telephone. Powered by four AA batteries, it uses five ICs. The company says it is negotiating with another firm on an inexpensive watch version that would use hybrid circuitry.

However, the new machines may add fuel to an already raging fire. Increasingly, personnel departments of many businesses are using the earlier suitcase-sized models with strip-chart readouts to screen applicants. As a result, several bills banning the machines are before Congress, and related measures are pending or already in place in many states. **-Ana Bishop**

Military

Tropospheric radio uses digital circuitry

Another link in the U. S. armed services' evolving Tri-Tac tactical communications network is entering its developmental test. It's the TRC-170 tropospheric scatter communications system, funded by the Air Force Electronic Systems division.

Three versions of the TRC-170 are being tested at Fort Huachucha, Ariz. Key features that will be evaluated closely are portability, fast erection, and compatibility with the rest of the multiservice digital Tri-Tac system [*Electronics*, March 15, p. 90]. The digital system is intended as a replacement for an analog design in use since the mid-1950s.

Different ranges. Designated the V1, V2, and V3, the three systems have ranges of 200, 150, and 100 miles, respectively. The Air Force says the digital circuitry employed gives 30% greater range than comparable analog systems, plus three times the channel capacity, lower radio-frequency background noise, and—partly as a result—lower error rates. Electrical power requirements also are lower. At about 25 kilowatts, they make for a small generator system. Tripod-mounted dual antennas not only go up swiftly, but also appear to be sturdier than earlier units. The Air Force claims that they will survive 130-knot winds and continue to operate in 100-knot winds.

The largest of the three TRC-170 models, the 10-kw V1, can be transported in a single mobile shelter with one pallet. Its crew of three can raise its two 15-foot parabolas and be on the air within 4 hours. The smaller V2 and V3 use 9.5-ft dishes and lighter-weight 2-kw klystron (microwave-tube) transmitters—two in the V2, one in the V3—and should get on the air within an hour.

The TRC-170 features some built-in test capability, including sensors to help the crew aim the antennas

News briefs

SIA now sees 36% hike for 1979

Based upon third-quarter shipments and early fourth-quarter data, the Semiconductor Industry Association estimates that shipments of U. S. semiconductor manufacturers will reach $6.3 billion in 1979, a record increase of 36% over 1978. Third-quarter shipments of $1.7 billion were 37% higher than year-earlier levels. Integrated-circuit shipments for the quarter totaled $1.2 billion and are expected to reach $4.5 billion for the full year, topping 1978 shipments by 40%. The Cupertino, Calif.–based association previously forecast a growth of 11% for 1980, based on the impact of a recession late in 1979 and early next year. While it has yet to revise that forecast, SIA executive director Tom Hinkelman notes that current backlogs and order rates now point to strong business activity into the first quarter of 1980.

Sales of television and radio sets slide

That bellwether of the home entertainment industry's economic health, color television, dropped in sales in October for the third straight month. The Electronic Industries Association says the 882,758 TV receivers sold to dealers are 3.4% fewer than in October 1978. Monochrome sales registered their first decline of the year, off 0.2% to 560,373 units. As for radios—a-m, fm (or combination), and auto—sales dropped 17.8% from October 1978 to just under 2.8 million. However, sales of video cassette recorders did jump 8.6% to 61,389 units in October, up 19% for the year.

Fairchild, Allen-Bradley report top management changes

Acting with a dispatch that caught industry observers by surprise, Schlumberger Ltd. has catapulted one of its executives into the presidency of its recently acquired subsidiary, Fairchild Camera and Instrument Corp. in Mountain View, Calif. Thomas C. Roberts will also become chief operating officer, replacing president and chairman Wilfred J. Corrigan, who will continue on as chairman but only until February. Roberts was vice president and chief financial officer. Departing from the Allen-Bradley Co. is Stanley J. Kukawka, president and general manager of the electronics division in Milwaukee. "Personal reasons" is the only explanation given.

Tandy, Datapoint to make peripherals

In a move that will break new ground for both Texas companies, Tandy Corp., Fort Worth, and Datapoint Corp., San Antonio, plan a joint manufacturing venture for production of computer peripheral equipment: Texas Peripherals. Neither Tandy, a $1 billion–plus consumer electronics retailer owning Radio Shack, nor Datapoint, a $200 million–plus manufacturer of business computer systems are saying what products will be built. However, disk drives and printers may be early on the agenda. Initial production could begin within a year at an unspecified Texas site. Datapoint makes some peripherals; Tandy has made none.

Paris components show to feature U. S. pavilion

The U. S. Department of Commerce is looking for 40 electronics firms to exhibit at the pavilion it will sponsor next spring at the Composants Electroniques show in Paris. The department promises "a comprehensive Government promotion program" aimed at European buyers and "Government market research on the French electronic components industry." To be held March 27 through April 2, the show is one of the most important annual exhibitions in Europe.

and keep them aimed. Pointing error degrades transmission quality, so these sensors operate continually as part of a performance-monitoring system.

Other than the antenna and transmitter subsystems, the three units are identical. All use a thermoelectrically cooled gallium arsenide field-effect-transistor preamplifier to boost sensitivity and keep the noise figure to a respectable 2 decibels. The preamp and receiver subsystems are broadband, covering the 4.4-to-5.0-gigahertz tropospheric band without tuning.

Common modem. The units also share a digital adaptive modulator-demodulator built for the high multipath environment characteristic of tropospheric operations. To boost transmitting efficiency and shrink bandwidth, the modem uses a dual-frequency time-gated waveform, which helps prevent the confusion among pulses usually caused by parts of a signal arriving at slightly different times. On the receiving side, an adaptive filter demodulator also reduces the effect of what is called pulse smearing.

In the field, the TRC-170 would usually be connected with other digital units. For communication with analog units, there is a built-in two-way conversion facility. This subsystem uses the Tri-Tac digital group multiplexer, a unit capable of serving as many as 30 subscriber loops in a variety of formats and a variety of bit rates—from 128 to 2.048 kilobits per second. The TRC-170's channel capacity is 60 channels at 32 kb/s or 120 channels at 16 kb/s.

The Fort Huachuca tests by the division, based at Hancom Air Force Base, Mass., are aimed at seeing whether the TRC-170 can perform as specified in the field, in various weather and transmitting conditions. At the conclusion of these tests next April, the Defense Department will decide whether to go into production on the equipment. If the decision is go, Raytheon Co., Sudbury, Mass., would stand a good chance of getting the production contract, since it won the $18.2 million development award. **-James B. Brinton**

PHILIPS

BEAMWRITER

VECTOR SCAN LITHOGRAPHY SYSTEM

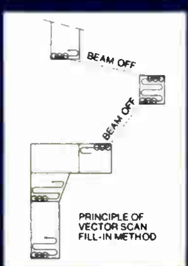
The Best Production EBL You Can Buy

Choosing an electron beam lithography system is a difficult task. Your selection will depend upon your specific requirements; however, throughput, uptime, precision, flexibility and minimum feature size are the most relevant factors in the majority of applications. That's why Philips designed the Beamwriter Lithography System to excel in each of these areas:

Throughput

In a production environment, the number of masks, reticles or chips produced per hour determines the cost effectiveness of the equipment. Throughput is critical. Philips' Beamwriter system gives you highest throughput for most applications by using vector scan technology and high dose rates.

Vector Scan



Philips' Beamwriter system is the only commercially available production oriented vector scan EBL. You achieve higher throughput with vector scan than raster scan because the beam wastes no time scanning unnecessary areas. This makes vector scan especially efficient in the production of reticles.

High Dose Rate

The efficient electron optical design of Philips' Beamwriter system gives you an exposure dosage twenty times greater than other commercially available EBL systems. This enhanced dosage enables a faster maximum writing speed and a wider choice of resists.

Uptime

Three main factors affect uptime — reliability, serviceability, and service response:

Reliability

The Beamwriter system's exceptional reliability results from Philips' 30 years experience in building dependable electron microscopes. Offstage drives are mounted in the main working chamber. By eliminating the need for bellows, the Beamwriter eliminates the possibility of downtime due to bellows failure. The stage utilizes ball bearings coated with a molecular layer of lubricant, which eliminates bearing wear. This specially chosen lubricant does not contribute to any column contamination.

Serviceability

Designed for serviceability, the Beamwriter incorporates a lifting jack within the column for quick separation of parts. This gives you access to the X-Y table in 10 minutes. Recalibration is rapid because of the unique assembly configuration of the X-Y table and the electron optics column.

Service Response

Philips has more than 3000 electron microscopes installed around the world with an experienced team of over 250 service engineers to maintain them. No other microscope or EBL manufacturer has a service organization that comes close to this in numbers, experience or dedication.

Precision

Electron Beam productivity requires alignment accuracy. The Philips' Beamwriter system eliminates drift due to thermal effects. All lenses and lens reference power supplies are water cooled. The rigidly-built working chamber utilizes special materials which have low coefficients of thermal expansion. The working chamber is also temperature stabilized. Consequently, the Beamwriter offers you overlay accuracy twice as good as other commercially available systems.

Flexibility

The Beamwriter system is built for direct writing as well as mask making. The unique substrate height sensor, standard in the Beamwriter, enables block by block refocusing of the beam to compensate for wafer distortion. Four backscatter detectors offer optimum alignment on topographical markers.

Minimum Feature Size

The Beamwriter system has a minimum beam diameter 10 times smaller than other commercially available production EBL equipment. Furthermore, vector scanning provides the potential for proximity correction, necessary to achieve narrow geometries. The Beamwriter's variable clock rates capitalize on this potential.

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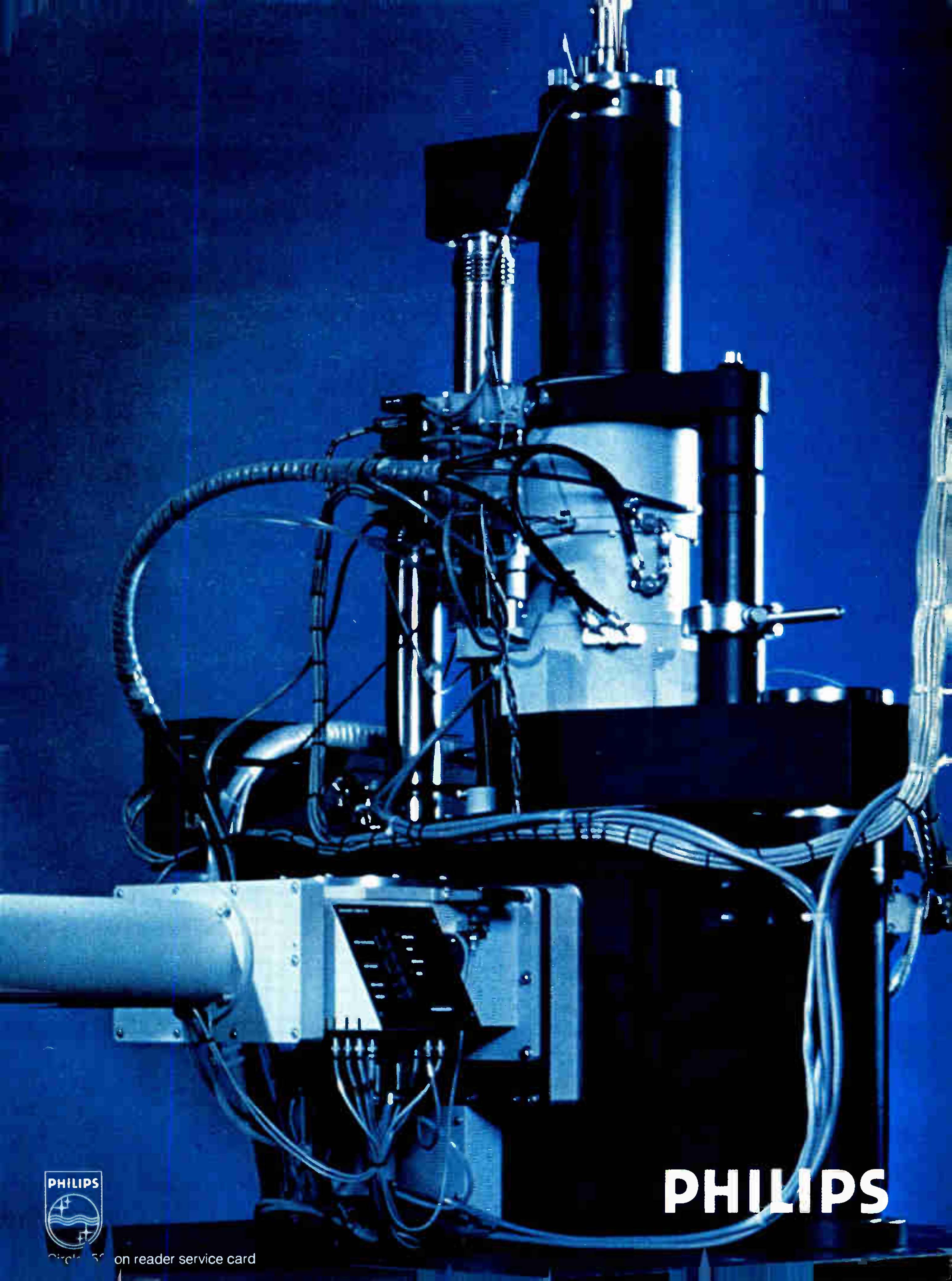
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NASA revitalizes satcom R&D at Lewis Center

The National Aeronautics and Space Administration is moving to regain a leadership role in satellite communications technology with a program at its Lewis Research Center in Cleveland aimed at launching a sophisticated third-generation system in 1985–86. The new mandate to Lewis, which led the joint U. S.-Canada project to develop the Communications Technology Satellite, **calls for using high technology for increased and more effective use of the radio-frequency spectrum in geostationary satellites.** The Cleveland center will work closely with the Pentagon, other NASA centers, and private industry. The loser in the decision is NASA's Goddard Space Flight Center at Greenbelt, Md., which sought the assignment after the National Academy of Engineering recommended two years ago that the space agency get back into the business. NASA's satellite communications research and development budget at that time had dropped to $10 million from a 1973 high of $60 million [*Electronics*, April 14, 1977, p. 57].

TI, others engage lawyers to protect Army IR&D data

Companies like Texas Instruments Inc. are hiring special lawyers in case they have to fight **to keep AT&T from gaining access to data on independent research and development** on file with the Army's Materiel Readiness and Development Command (Darcom). AT&T wants to invoke rights of discovery to the IR&D telecommunications files to help prove its antitrust case argument that it is not a telecommunications monopoly [*Electronics*, Oct. 25, p. 58].

Plan to reduce color TV dumping assessments hit

The U. S. Customs Service is being accused of rushing to slash color TV dumping duties against 10 Japanese manufacturers before the stiffer rules of the 1979 Trade Agreements Act take effect in January. Compact—the Committee to Preserve American Color Television—denounced the Customs Service's decision earlier this month to "allow some of the adjustments claimed" for costs, discounts, rebates, sale, and services by protesting importers to reduce the amount of dumping duties assessed. **Compact claims this could cut the assessment to as little as 9% of the backlog of $400 million to $600 million.** Customs says it is recomputing the dumping duty liability on a company-by-company basis and expects to have new figures before the end of the year.

NATA forecasts 1980 sales drop for PBX, key systems

After more than four years of rapid growth, dollar volume of independent telecommunications terminal sales in 1980 will drop about 12% to $639,800, says the North American Telephone Association. **However, the total 1980 income for the independent interconnection industry is expected to grow slightly,** NATA forecasts, as the decline in key systems, automatic electronic private branch exchanges (PBXs), and computer branch exchanges (CBXs) is more than offset by increased income from maintenance and system add-ons, moves, and changes.

Sales of key systems are forecast to drop 20% from the 1979 high of 15,000 to 12,000 next year before rising again in 1981 to 15,800. Similarly, sales of PBX and CBX systems will slip 10% from this year's 6,800 systems to 6,100 next year before recovering to 6,600 in 1981. NATA bases its PBX calculations on an average of 102 instruments per system priced at $800 each. Key systems are calculated at 13 instruments per system priced at $900 apiece.

Solar power and the voting machine

Last June, after an extensive review of domestic policy the year before, President Carter got extensive mileage in the media out of his proposal to support the development of solar energy as a counterweight to U. S. dependence on foreign oil. No one cheered louder than the Solar Energy Industries Association when the President announced "a national goal of meeting one fifth of our energy needs with solar and renewable resources by the end of the century." Enthusiasts began comparing the announcement with John F. Kennedy's challenge to the nation to put American astronauts on the moon.

Nearly five months later, Carter's legislative initiatives have failed to match his oratory, and the SEIA's cheers have turned into jeers. The Administration is charged with "political exploitation of the solar industry." Providing only "lip service to one of the major solutions available to him," according to Sheldon Butt, SEIA president. The association supports its charges with an analysis of the 11 segments of the Domestic Policy Review presented to Carter, as well as the three options within each segment, and finds that in nearly every case the President has opted for the least promising program.

The majority leader's message

Since the SEIA presented this blistering critique of Carter at its annual meeting in the capital at the end of October, the Iranian student takeover of the U. S. embassy in Tehran, the President's cutoff of imports of Iranian oil, and subsequent events seem to have awakened the American public to the need for the nation to achieve greater energy independence.

House majority leader Jim Wright has been trying to focus national attention on that need for some time. At the SEIA meeting, the Texas Democrat got the members' attention by quoting one passage from a White House report that goes like this: "We find the existing situation to be so dangerous that unless corrective measures are taken immediately this country will face both a military and civilian collapse. [The crisis has come as a result] of procrastinations, indecisions, conflict of authority, clashes of personalities, lack of understanding, delays . . . [and the] failure to build a greater stockpile of crude. . . . The naked facts present a warning that dare not be ignored."

The report was delivered 37 years ago to Franklin Roosevelt by a task force headed by Bernard Baruch to assess U. S. efforts to create a synthetic rubber industry using petroleum as a base. "Three years after this report," recalled Wright, "the industry had been built and the Allies rolled into Germany on rubber made by that industry." He is convinced that "the sleeping giant that is the American will, when once aroused, can triumph just as gloriously over our present crisis" in energy.

As SEIA's applause for Congressman Wright subsided, one executive in the photovoltaics industry observed, "Sounds great, except he didn't say anything about money. We might be out of business before we get to share in that glorious victory."

Similar sour comments about President Carter's failure to propose and support significant increases in Federal funding of photovoltaic technology and tax credit incentives for its use are common among most of the small businessmen in the industry—those who have provided most of the technology breakthroughs in the past. They are now beginning to feel the credit crunch as sources of new capital dry up and interest rates continue to soar.

In the absence of increased Federal support, more and more photovoltaics manufacturers are selling shares in their operations to the major oil companies, who recognize a cheap, good investment when they see one—particularly if it represents a potential threat to their market. In that context, it is truly puzzling to find the President pushing hard to curb the growth of oil company conglomerates on the one hand while failing on the other to spur the development of an independent and potentially competitive new energy source.

The fallout from Iran

By the Department of Energy's own estimate, the photovoltaics market will experience "explosive growth" when array costs per peak watt come down to $1. The DOE's goal for its limited program is $2/W by 1982 and 50 cents/W by 1986. However, in the wake of the Iranian oil cutoff and the petroleum price hikes that it is expected to generate elsewhere, some DOE officials believe photovoltaics may become price-competitive even sooner.

All of ths suggests that conditions are ripe for a different kind of "political exploitation of the solar industry" by President Carter. Carter's new approach would capitalize on the political momentum of an aroused nation, as well as please the solar energy industry, by putting money and legislative programs behind his promises of last June 20. The price tag need not come close to that of putting Americans on the moon, although the President might find it sufficient to help him remain in the White House beyond 1980.

-Ray Connolly

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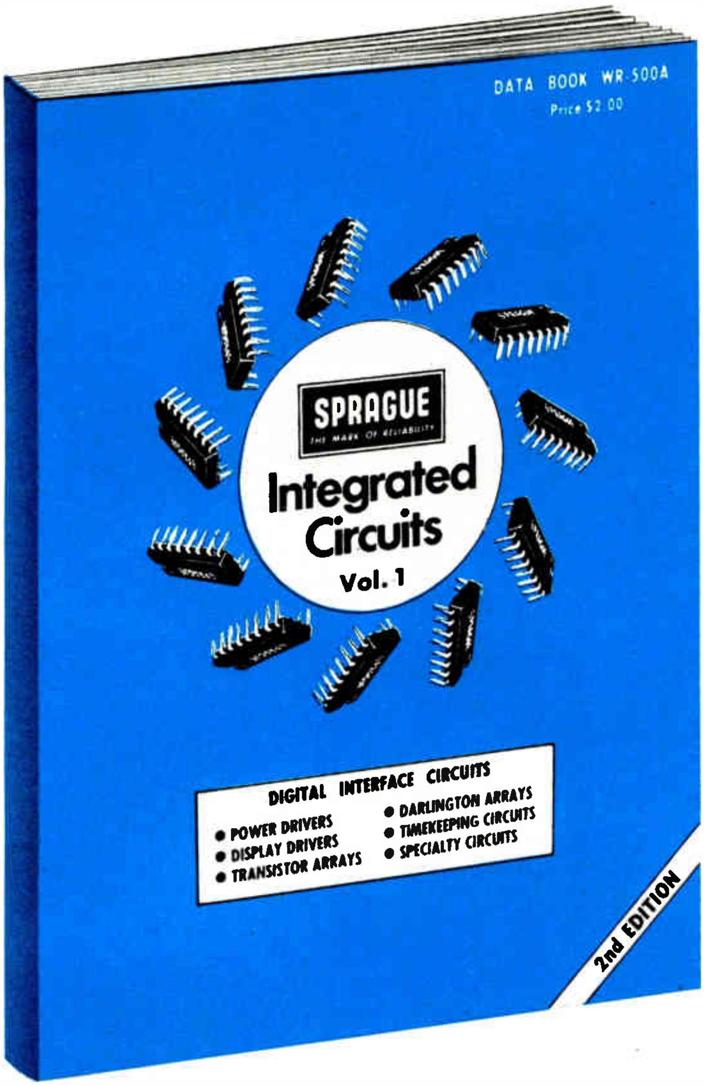

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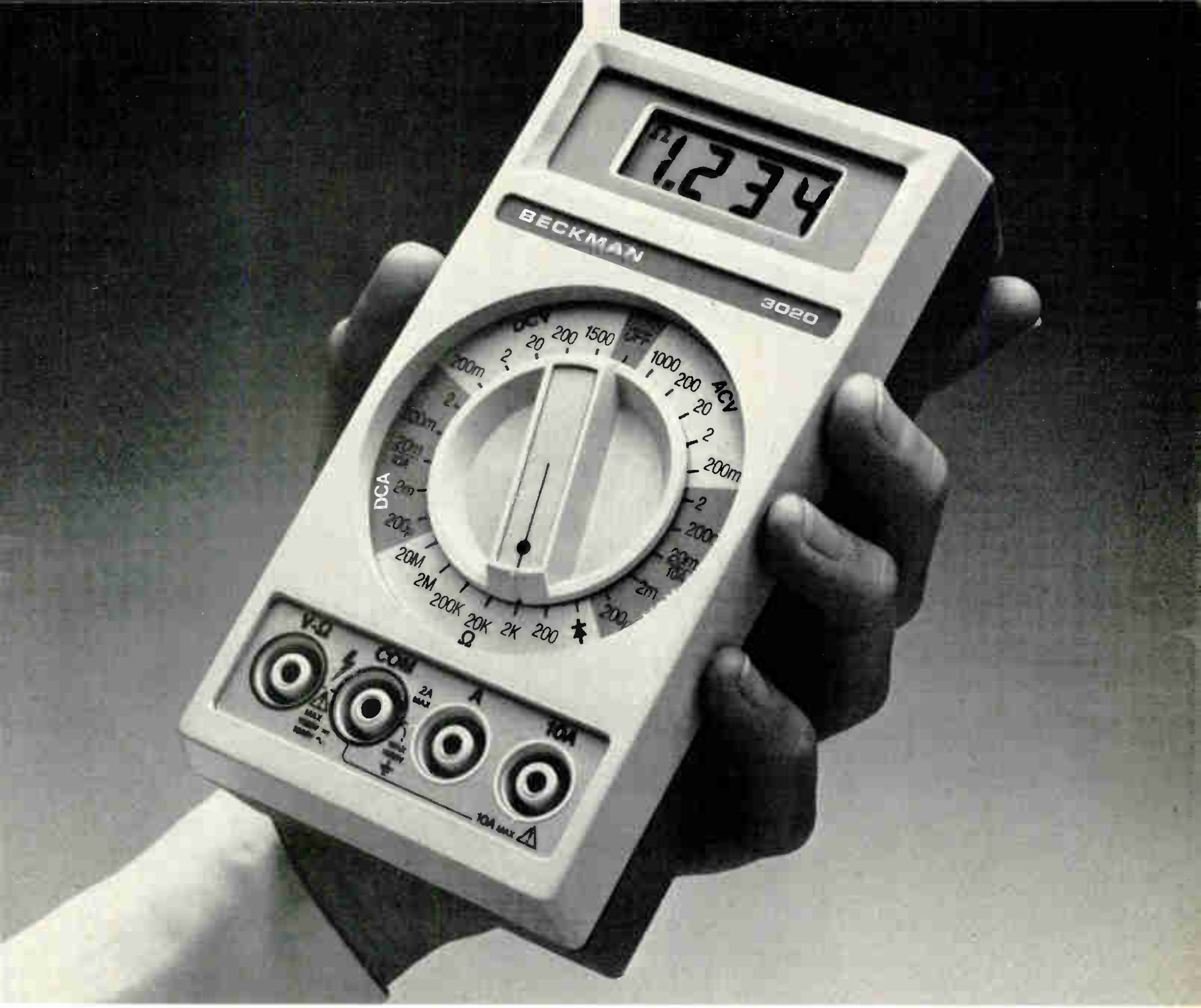

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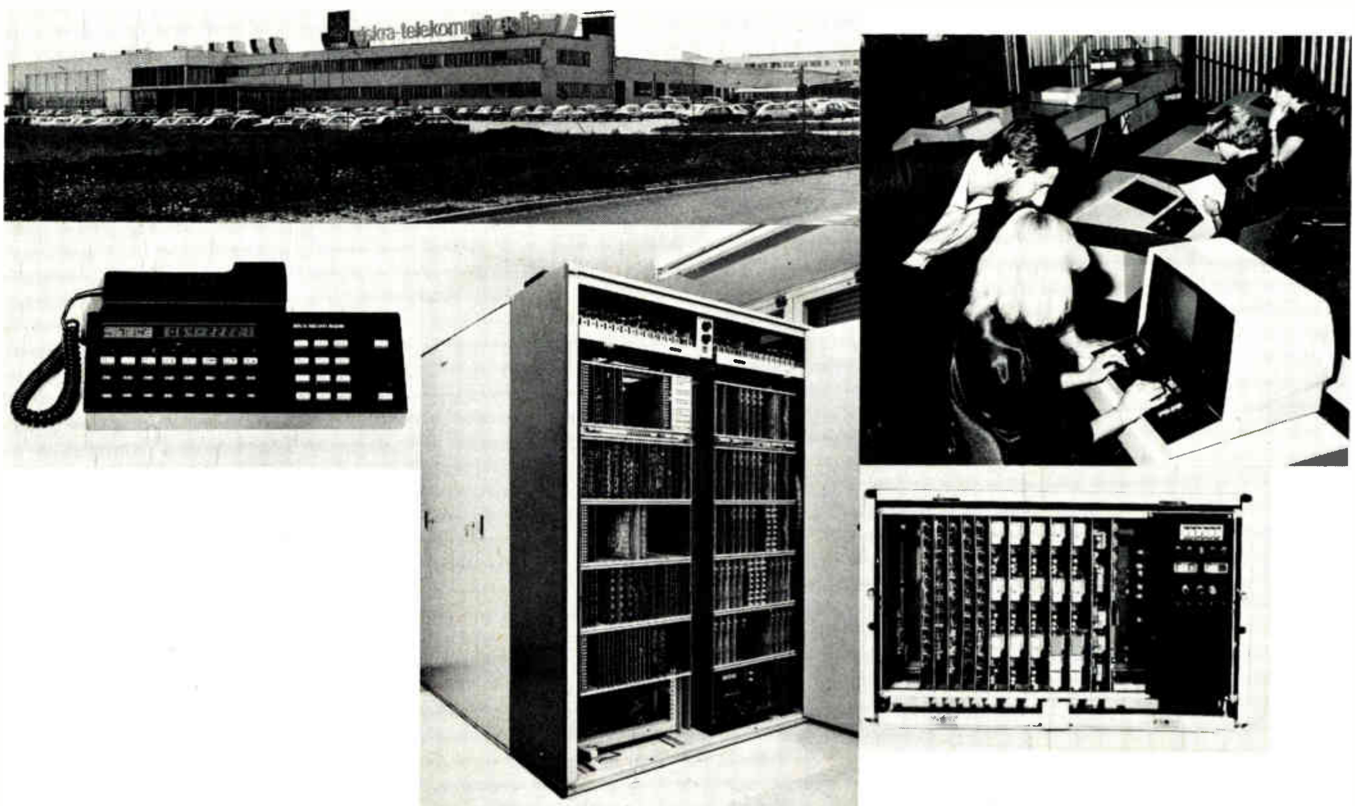

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Toshiba applies looped video tape for data-file storage

A continuous-loop video tape from Toshiba Corp. will find its first commercial application as the storage medium in a data file—the Tosfile 1000. Similar to the consumer prototype the firm showed earlier this year [*Electronics*, March 15, p. 72], **it is teamed with a laser scanner and a laser printer having scanning densities of 8.5 lines/mm.** Each cassette, which has had the tape length shortened to 36 meters for faster access and tape speed reduced to 5 m/s, **can store an average of 3,000 metric A-4 page (8.4 by 11.9 in.) facsimile images.** Toshiba says it will start sales in Japan next October at a price of $28,000. It expects to sell 5,000 units over a five-year period. Modified Huffman coding is used for redundancy reduction of the signal [*Electronics*, Nov. 8, p. 85], which is transferred at a rate of 1.5 Mb/s. The system will include a 2-Mb buffer memory, but the average page length is said to be about 0.5 Mb. Input or output requires an average of about 8 seconds.

Compromise likely at WARC on high-frequency band

After nearly two months of work on noncontroversial technical problems, the delegates from more than 140 countries to the World Administrative Radio Conference in Geneva are finally getting down to the sensitive political and economic issues overhanging the 10-week session [*Electronics*, Sept. 13, p. 87]. A compromise is being worked out between developing countries seeking continued use of the high-frequency band for point-to-point fixed communications and developed countries looking for expanded international shortwave broadcast frequencies. But **there is no movement so far on the developing countries' demands for reserved positions for geostationary orbital communications satellites.** The conference is due to close Nov. 30.

CII-HB plans bank card that uses microprocessor

CII-Honeywell Bull will announce early next month its intention to commercialize a microprocessor-equipped bank card, designed for use in an off-line electronic funds transfer system. Although the Paris computer firm already has a prototype of the card, based on a Mostek 3872 microprocessor and a 2716 electrically programmable read-only memory, **it is apparently seeking a customer to help with the $1.5 million development costs** needed to bring the project to fruition. Several other French companies, including Thomson-CSF, Schlumberger, and Transac, a subsidiary of the large Compagnie Générale d'Electricité, are also experimenting with an "intelligent" credit and bank card, but based upon a PROM combined with about 100 simple logic gates rather than a microprocessor.

Philips upgrades minicomputer series with one-chip CPU

The Data Systems division of NV Philips Gloeilampenfabrieken is about to announce an upgraded version of its P800 minicomputer series. One item making the series more powerful and faster is a 16-bit central-processing-unit chip. About 57,600 mil^2 (36 mm^2) in size, **it replaces the 40 integrated circuits on a 6.4-by-8-in. (16-by-20-cm) board currently used.** The Dutch company has dubbed its new microprocessor FAST, for "Fontenay Apledoorn Sunnyvale technology," a name indicating that the device was designed by two Philips data-systems development groups, in Fontenay-aux-roses in France and Apeldoorn in the Netherlands, in collaboration with the Philips subsidiary Signetics corp. in Sunnyvale, Calif.

Hybrid alerts car drivers to aquaplaning risk

Alfred Teves GmbH in Frankfurt, Europe's biggest automobile brake manufacturer and an ITT subsidiary, has developed a system that warns a driver of the risk of aquaplaning, or skidding on a wet road. **The heart of the system is a printed-circuit board the size of a cigarette pack fitted with components from various ITT subsidiaries.** Wheel-mounted sensors register the slower rotation of wheels losing their grip on a slippery surface, and an acoustical or optical warning alerts the driver. Teves says it is about to deliver sample systems to interested car makers for testing.

Japanese moving monochrome TV production offshore

Japan's consumer electronics industry is being forced to drop domestic production of less sophisticated products in the same manner as was its U. S. counterpart, albeit with a time lag. Hitachi Ltd. has announced that it is phasing out the production of black-and-white TV, even those for sale under its name in Japan. **It will shift production to two subsidiaries, Hitachi Television (Taiwan) Ltd. in Taiwan and Hitachi Consumer Products (S) Ltd., in Singapore.** It is also ending the production of black-and-white picture tubes in Japan. Toshiba Corp., for one, already imports its monochrome sets from a subsidiary in South Korea.

In an unrelated development, the company says that downstream assembly color picture tubes has begun at a joint venture, Hitachi Electronic Devices (Singapore) Ltd., in which it has 70% of equity, the Singapore government 30%. The plant will produce color picture tubes from start to finish, beginning in April. The tubes will be sold mainly in Southeast Asia.

Thin-film pulse amps to go aboard U. S. Jupiter probe

Rohde & Schwarz GmbH is making what it says is a major contribution to the Jupiter space probe that the U. S.'s National Aeronautics and Space Administration will launch early in 1983. The Munich-based firm will supply **some 30 thin-film pulse amplifiers for identifying and measuring the distribution and energy of the particles trapped in Jupiter's strong magnetic field.** Designated the PA-200, each pulse amplifier is only 0.5 $in.^2$ (3.25 cm^2) in size and weighs 1.6 g. To meet NASA's exacting quality demands, the substrate, made of high-purity aluminum oxide, carries high-quality nickel-chromium resistors and pure-gold printed conductors. The amplifiers are connected by aluminum wires 25 μm in diameter. Fitted in metal flatpacks and hermetically sealed, they are designed for low power consumption and fast rise times and use ruggedized thin-film technology developed by R&S.

Plato comes to Great Britain

Computer-assisted learning is becoming big business. Control Data Corp., Minneapolis, one of the pioneers in the game, is taking its Plato computer-based educational system abroad, with a first $10.7 million investment in the UK to establish learning centers in four cities during 1980. They will be serviced from a dual Cyber 730 in North London. The development of Plato began at the University of Illinois in 1962, and now 60 U. S. cities have CDC learning centers. **One of the first courses to be offered—at the instigation of the Department of Industry—is a 60-to-80-hour program designed to train technicians and engineers in the basics of microprocessor technology.** The computer, says the firm, allows a student to work at his own pace and check his progress at every stage of the course.

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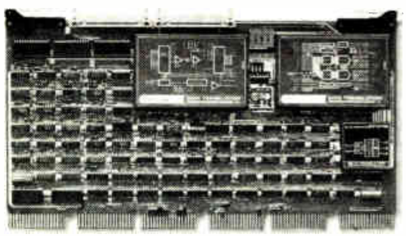

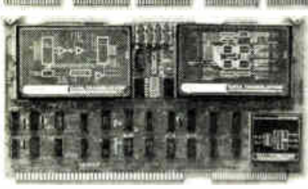

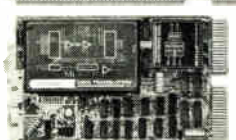

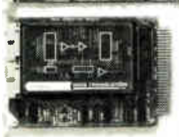

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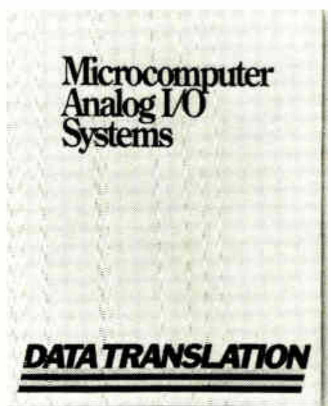

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Ultrasonic fuel injector is simple, promises greatly reduced cost

by Kevin Smith, London bureau manager

Piezoceramic transducer and ball valve offer reliability, lessen need for tight engineering tolerances

Ultrasonic injectors may soon be squirting precisely metered fuel into the cylinders of U. S., Japanese, and European cars if the ambitions of Barry James Martin, managing director of Plessey Automotive Products Ltd., are realized. Martin heads a small team of development engineers at the Romford, Essex, firm who are trying to sell the world on a new form of low-cost fuel injector that's been 12 years in development.

Now, in the wake of the energy crisis and increasingly stringent anti-pollution legislation, their device may be about to hit pay dirt. Fuel injection systems provide a cleaner burn, better performance, and greater fuel efficiency than carburetor systems. Their greater complexity and the needed micrometer-level engineering tolerances, however, have restricted their use for the most part to top-of-the-line models.

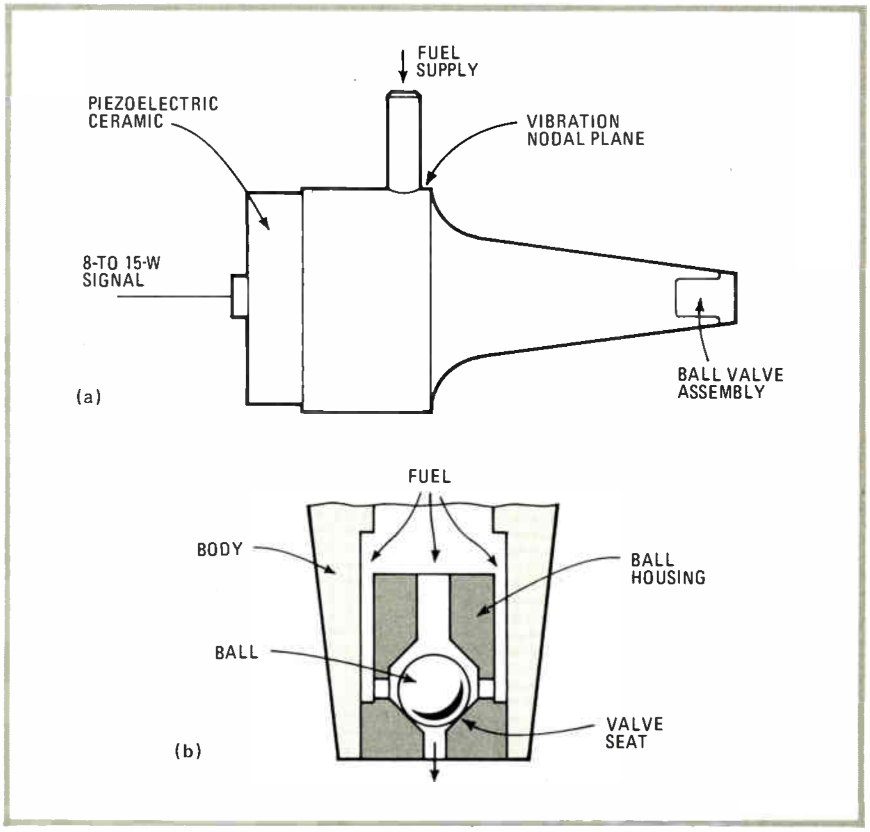
More for less. One answer to these drawbacks is a simple ultrasonic fuel injector that Martin discussed at the recent Second International Conference on Automotive Electronics in London [*Electronics*, Nov. 8, p. 94]. The device, says Martin, "offers improved performance over electromechanical fuel injectors at under half the cost—and serious value engineering has not even begun." Furthermore, he believes, a single injector could be used to replace the carburetor in engines with a displacement of up to 2.5 liters.

Plessey has no plans to manufacture the device. "We are not really in the automotive business," Martin says, explaining that his small group exists only to license the injector to other firms.

The group got involved in this area while looking for applications of piezoceramics, then a new class of oven-manufactured materials that are far cheaper than piezoelectric crystals. The ultrasonic fuel-metering device is the end product of this program, and now the group is talking to a key customer in each of the principal world markets—the U. S., Japan, and Europe. Next, says Martin, is volume manufacturing.

Simple shape. The injector is the essence of simplicity—a tapered steel body whose length is equal to one-half wavelength at 60 kilohertz so that maximum motion occurs at the tip. A piezoceramic disk is bonded to the broad, low-amplitude end, and a metering ball valve is situated at the narrow, high-amplitude end (see figure).

The valve is usually held against



Bouncing ball. Simple ultrasonic fuel injector from Plessey Automotive Products (a) uses piezoceramic transducer to shake loose ball from valve opening (b).

its seat, which has an opening 0.4 millimeter in diameter, by the fuel pressure. But when commanded by the control unit, the drive oscillator output excites the injector body into resonant vibration. The valve seat vibrates, shaking the ball from its closed position and thus allowing fuel to pass through and be atomized. Metering accuracy is not affected by contamination, as the value seat is continually cleaned by ball contact against it.

Reliability is excellent, too. "The only parts that can wear are the ball and its seat," explains Martin, "but as the ball is roughly 100 times lighter than the moving parts of the electromechanical injector, the reasons for the exceptional lifetime characteristics can easily be seen."

Driving. The injector is driven by an oscillator operating at 60 kHz, the resonant frequency of the injector. Its signal is amplified to an 8- to 15-watt level, depending on the flow rate, but improvements in driver-circuit efficiency will reduce this requirement. Since the transducer is voltage-driven, a transformer is needed and full integration is not possible. "This requirement adds a few cents to the driver circuitry," says Martin, "but the overall cost of the injector is dollars less."

The injector is pulsed at about 100 hertz, and the quantity of injected fuel is controlled by pulse-width modulation, with the relationship between fuel flow and pulse width linear. The flow is independent of pipeline pressure.

Learning time. Though the system is not mechanically complex, it took 12 years to develop. "One reason," Martin says, "is that it took that time to understand the physics of what was going on. The first injector we made worked the first time, but after that we could not get repeatability."

Now the group reckons they know what the critical parameters are and can monitor them at an early stage in production to check that the finished product will be within performance tolerance. The final hurdle is to persuade a customer to prove their groundwork in volume production.

West Germany

PCM audio disk proposal offers simple tracking mechanism, record production

Although audio records and playback systems using pulse-code modulation have already been demonstrated, it won't be until the second half of the 1980s before such equipment goes to market. The reason, the experts say, is that the industry wants to scrutinize the various proposals with a view toward reaching a worldwide consensus on a standard to prevent a hodgepodge of incompatible systems from fragmenting a market that could amount to billions of dollars a year in the decades ahead.

The latest proposal for a PCM audio standard comes from AEG-Telefunken and the record producer Teldec GmbH, a joint venture of Telefunken and Britain's Decca Ltd. based in Hamburg. Not surprisingly, the two West German firms are convinced they have something special to offer. Their proposal envisions a system for which records are simple to produce, whose player needs no elaborate tracking mechanism, and whose error-correction scheme can easily be implemented.

AEG-Telefunken recently demonstrated such a system that could eventually retail for about $550, "a price roughly the same as that of average hi-fi equipment and low enough to spawn a mass market," says Klaus Welland, head of research and development at the company's entertainment electronics division in Hanover. The records would cost no more than conventional ones with the same playing time.

The two firms propose a polyvinyl chloride disk only 13.5 centimeters, or roughly 5.3 inches, in diameter and hence called the Mini-Disk. Recorded on both sides, the disk has a playing time equivalent to that of four long-playing records. It spins at 300 revolutions per minute.

For the record. Proposed PCM audio disk from AEG-Telefunken and Teldec is 13.5 centimeters in diameter and comes housed in a protective cassette (not shown).

Playback. Sound information is read mechanically by a piezoelectric pickup device running along the disk's grooves. There are some 600 grooves per millimeter, a groove density 50 to 60 times greater than that of an LP record.

Disk wear is no problem, Welland says, because the forces bearing on the disk are negligible. "The disk will last a lot longer than the number of times that people will want to listen to it," he claims.

The proposal specifies a value of better than 85 decibels for the dynamic range, as well as for the signal-to-noise ratio and crosstalk attenuation. The frequency response is essentially flat over a range of 20 hertz to 20 kilohertz, and the distortion is less than 0.05%.

To record, the system uses 14-bit linear coding with a sampling frequency of 48 kHz. A 14-bit resolution, Welland explains, is enough to provide the 85-dB dynamic range, which is more than adequate for any

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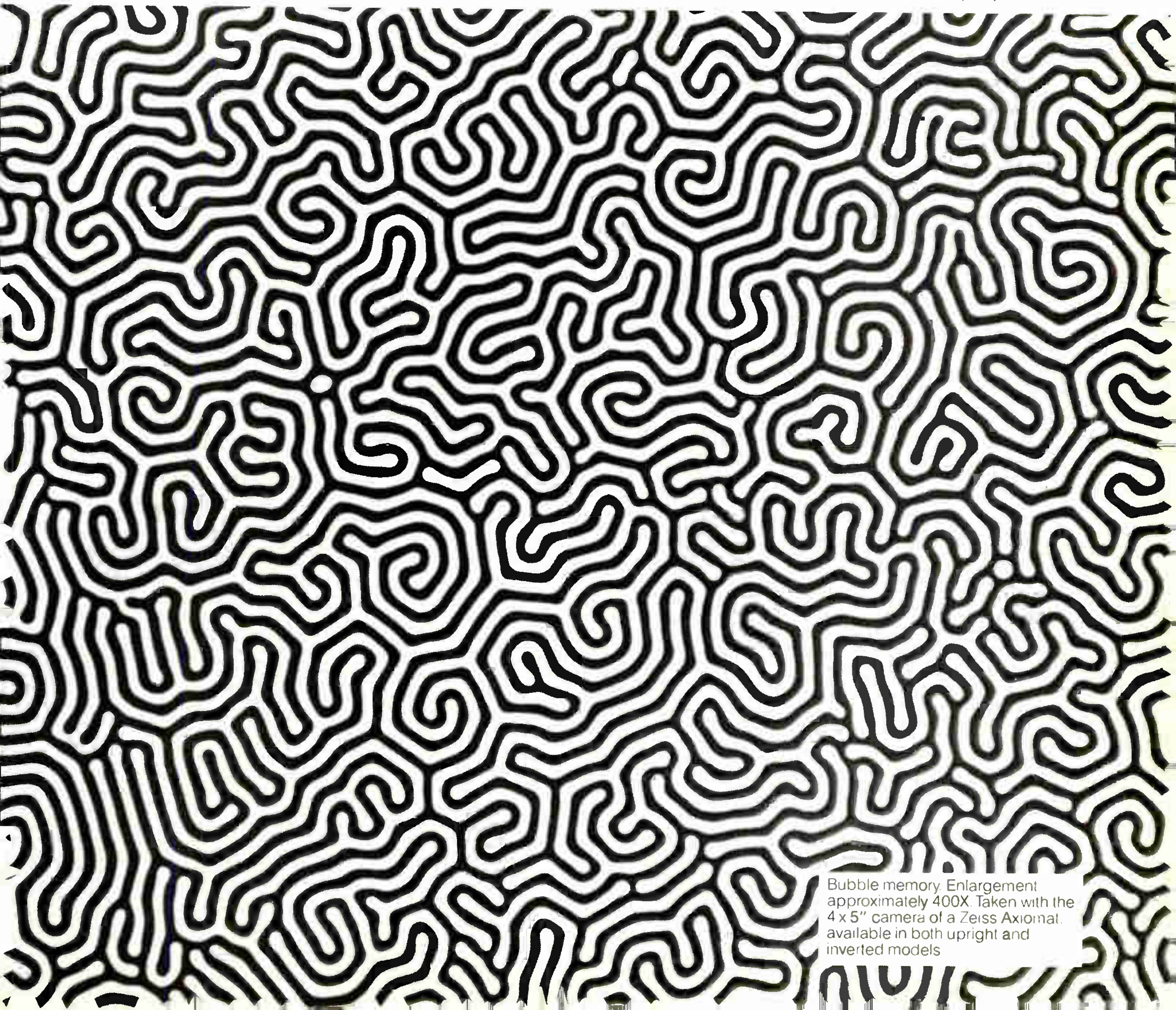

Bubble memory. Enlargement approximately 400X. Taken with the 4 x 5" camera of a Zeiss Axiomat, available in both upright and inverted models

PCM vs analog audio recording

Audio recording and playback using pulse-code modulation marks a radical departure from conventional techniques, techniques based on analog phonographic principles almost a century old. During that time, significant advances have been made in reproduction fidelity, playing time, equipment price, and market penetration. More than 200 million record players are estimated to be currently in use worldwide and about 1.5 billion records to have been sold in 1977 in industralized countries in the West alone.

For all the advances made, however, the quality of analog systems still leaves much to be desired. System noise continues to be a problem, as does crosstalk between stereo channels. Clicks and crackling sounds on the record are another shortcoming. But PCM digital techniques promise relief. They provide a high dynamic range and a better signal-to-noise ratio. Furthermore, PCM gets rid of crosstalk, reduces distortion to negligible levels, and eliminates noise spikes through the use of error correction.

Before PCM records and players become a commercial reality, though, the industry wants to agree on a standard, just as it has on the 45- and 33⅓-rpm long-playing records. The equipment market is simply too big to let it be broken up by different standards and the resulting incompatibility of players and records.

The introduction of standard PCM systems will not spell the immediate demise of analog systems, however. Given the number of record players and records sold each year and the enormous amounts of money the industry has tied up in manufacturing equipment and production lines, "analog systems will exist alongside PCM audio for some 15 to 20 years," says Klaus Welland, head of research and development at AEG-Telefunken's entertainment electronics division in Hanover, West Germany. **-J. G.**

room in which the equipment would be used. By the time a standard is agreed upon, he adds, "the necessary 14-bit digital-to-analog and analog-to-digital converters will be available at prices so low as to be attractive for consumer equipment."

The proposal meets the basic requirements that a PCM audio disk system should fulfill, Welland says. The code chosen satisfies high quality and reproduction fidelity standards. What's more, the system's Mini-Disk meets the need for a recording medium that is compact and provides a long playing time. In addition, the system can be built relatively inexpensively.

Picking up. Although many of the proposed parameters agree with those suggested by other firms [*Electronics*, Nov. 24, 1977, p. 78], the new system differs in one crucial aspect: the mechanical information pickup, which is really the key to a low system cost and to simple disk production.

In disk manufacture, the information is put directly onto a metallic plate that serves as a master in mass-producing the disk—the same method used for producing conventional records. In contrast, optical disks (based on laser scanning) are relatively expensive to make, as each disk must be covered with a metallic layer after pressing and then coated with a protective plastic layer.

The mechanical pickup also allows the use of a simple tracking mechanism. Coarse tracking is provided by tangential scanning, in which a motor drive system guides the pickup arm. The grooves themselves effect fine tracking.

Error correction is also simple to achieve. It is done by cyclic redundancy checking, a scheme whereby digital circuitry compares the information bits with the CRC bits to catch errors.

To prevent dust particles, fingerprints, and scratches from impairing scanning, the disk comes in a normally nonremovable protective stiff-paper cassette. When inserted in the player, the disk is partly removed from its cassette and scanned, with the disk rotating freely in the cassette. After the scanning, a mechanism in the player reinserts the disk into the cassette and pushes the latter through a slot so that the user can remove it. **-John Gosch**

France

Fast signal analyzers use analog memories

Responsible for designing and building instruments for France's nuclear defense program, the Special Instrument Applications (ASI) department of Thomson-CSF has traditionally limited its activities to classified government work. But having persuaded French military authorities several years ago that the instruments themselves need not be top secret, but only the measurements they help supply, the department is expanding into civilian markets.

At Mesurcora, the triennial measurement and automation exhibit to be held in Paris, Dec. 10–15, it will be showing off ultrafast, fully programmable, microprocessor-controlled transient-signal analyzers. Paired with other new high-precision instruments, including a four-digit voltmeter accurate to within 0.1% from 1 to 15 kilovolts, and a 100-picosecond chronometer, the equipment makes possible a fully digital test bank for nuclear fusion experimentation, lightning measurement, and high-voltage installation tests.

Analog store. The signal analyzers use a series of analog memories to store samples of the signal to be analyzed before digitizing it and storing the data in a semiconductor memory, explains Etienne d'Humières, technical director for the department, located a mile outside the Paris city limits in Malakoff. The analog memories are serial analog devices, each containing 100 capacitors, supplied by Reticon Corp. of Sunnyvale, Calif. One of the analyzers, the TSN 693, contains 10 such memories, for a total of 1,000 points. The other, the TSN 694, contains 50, to handle 5,000 samples.

The minimum input voltage for

the 693 is ±1 millivolt. For the two-channel version of the 694, it is ±2 mV, and for the five-channel version, it is ±4 mV. All three can take a maximum pulse of 500 volts for 1 microsecond. The bandwidth is 50 megahertz for the 693 and 100 MHz for the 694.

The analog memories operate at a maximum speed of 10 megahertz, which means 100 nanoseconds between entries. They are strung together in parallel and fed sequentially to improve overall performance. With 10 memories, the sampling interval of the TSN 693 is 10 ns; for the TSN 694, the 50 memories means the interval is 2 ns.

Signal sampling and storage in analog memory are synchronized by a 10-MHz clock. After storage, the clock is slowed down to 100 kilohertz to allow the data to be transferred into a 12-bit, 10-μs analog-to-digital converter. From there, the samples are stored as 8 bits in standard digital memory.

The instruments each contain two microprocessors, an Intel 8080 to supervise the sequencing of operations within the instrument and an 8047 for input/output control. One of the 8080's jobs is to direct a test signal to each and every analog memory cell before a reading is taken. It then compares the signal as it is read out of the memory with the test signal and calculates a correction factor to account for any variations between the two. The correction is applied to the readout from each cell when the reading is taken. With 1,000 or 5,000 memory cells to be tested and then calibrated, the speed with which the microprocessor carries out its operation is crucial to the overall speed of the instrument.

Slow down. "The 8080 is just not very fast," says d'Humières, "which means there is a time lapse ranging from several seconds to several dozen seconds, depending on the precision required, before the instrument is again ready to receive data." That is no problem for one-shot measurements, but it is for repetitive high-speed data acquisition. He says Thomson will use Intel's 8085, a faster version of the 8080, in future models, but this will not do much to remedy the problem.

D'Humières says Thomson's approach differs from that of its principal competitor, Gould Inc.'s Biomation division in Cupertino, Calif., in the use of an input memory. Biomation achieves a 2-ns sample rate feeding its samples directly into an a-d converter, but d'Humières points out that those samples are expressed in 6 rather than 8 bits, rendering the results less precise.

The ASI department has developed also a transient-signal analyzer for military applications that operates at 2 gigahertz and provides 10-bit data conversion of a maximum of 20 signal samples. To improve performance and follow up on the civilian market, researchers are now trying to develop an analyzer capable of sampling between 50 and 200 points at a speed of 5 GHz without decreasing the 10-bit conversion. To reach those goals, d'Humières says, they are looking into the feasibility of using gallium arsenide integrated circuits in an a-d converter, which would do away with the need for an input memory without lowering precision. **-Kenneth Dreyfack**

Around the world

Olivetti, Soviet Union make a deal

Ing. C. Olivetti & Co's chief executive officer, Carlo De Benedetti, and the Soviet minister for automation and business equipment and production, Konstantin N. Rudnew, have signed an accord for combined economic, technical, and scientific cooperation for advanced office-organization and information-handling systems. Ivrea-based Olivetti estimates that the accord could give the company a stake as high as $120 million in the Soviet Union's five-year plan. The umbrella agreement follows negotiations between Olivetti and the Soviet government for supply of data-processing products and office machines and a wide-ranging plan for industrial cooperation. The latter would involve two projects for the production of Olivetti equipment in the USSR for domestic and Comecon markets.

Western European sensor market to pass $500 million, says Siemens

Western Europe's market for microcomputer support products, like sensors, actuators, power supplies, and displays, will amount to nearly $1.9 billion in 1985. That is the main conclusion of a market study for such devices prepared by Munich-based Siemens AG. Significantly, the largest chunk—more than $0.5 billion—will be for sensors, with automobiles and household appliances gobbling up about 70% (by value) of such devices sold in 1985. Measuring and control systems will account for 12% and communications equipment for about 5% of the sensor market. Pressure sensors will be the most common type, accounting for roughly 35% of overall sensor sales in 1985, Siemens says.

France's AOIP to vote on sale of telecommunications

The 4,500 worker-stockholders of France's Association des Ouvriers en Instruments de Précision (AOIP), a workers' cooperative formed in 1896, are to vote in early December on the proposed sale of the company's public telecommunications activities to CIT-Alcatel and Thomson-CSF, the two giants in the French telecommunications industry. After months of negotiations, the three parties agreed that Alcatel and Thomson would split the acquisition 64/36, with each forming a new company out of its share. Telecommunications is the cooperative's largest sector.

Fairchild offers its figures for automotive semiconductors

Fairchild Camera and Instrument (Deutschland) GmbH estimates that in 1980 semiconductor products in automobiles will account for 1% of the vehicles' total value. The figure for 1985 should be 4%, it says. Fairchild puts worldwide consumption of semiconductor products by the automobile industry next year at about $259 million and pegs it at roughly $1.2 billion in 1985. (For related estimates, see *Electronics*, Nov. 8, p. 94.)

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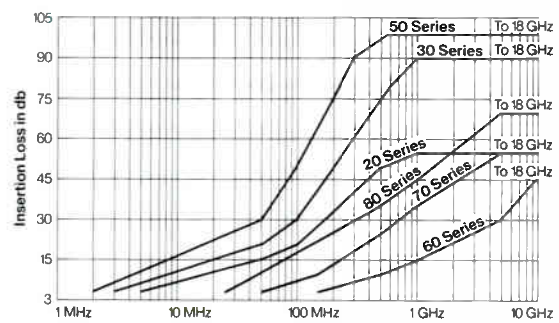

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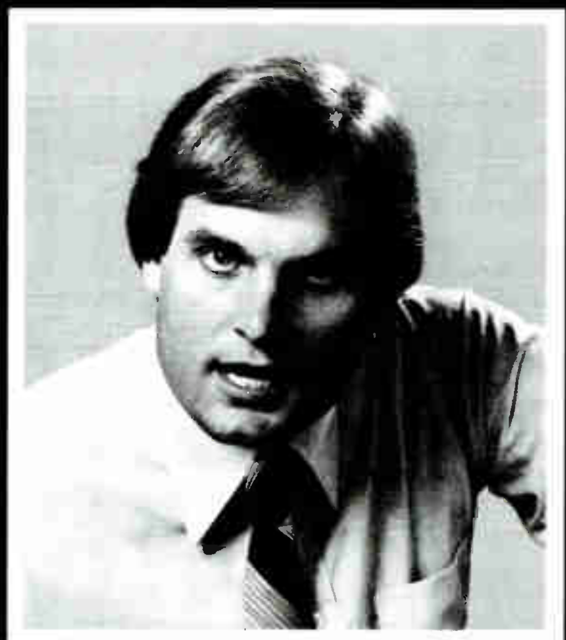

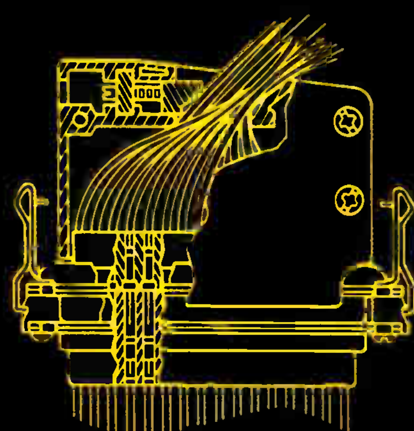

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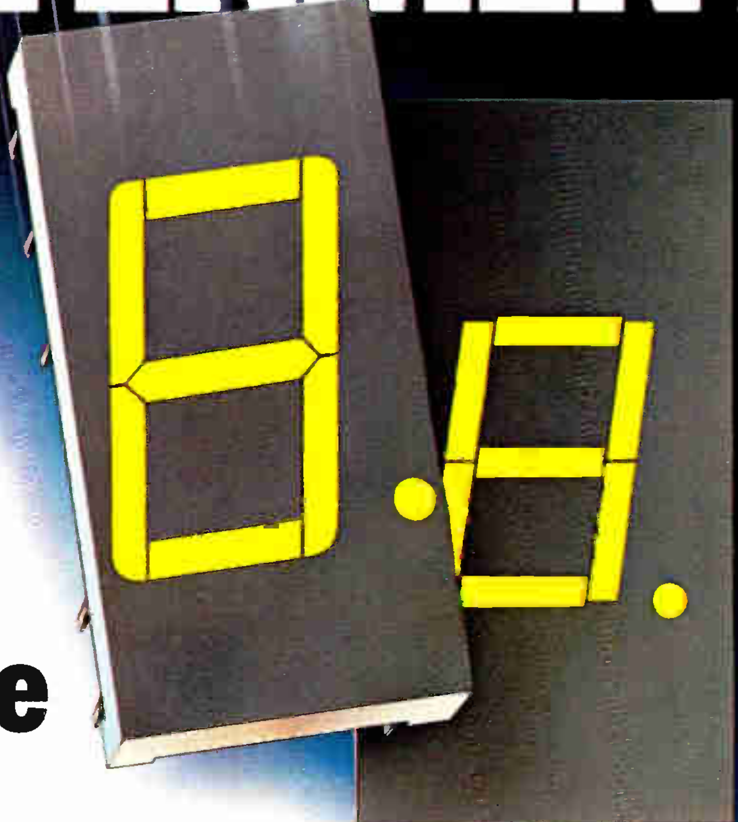

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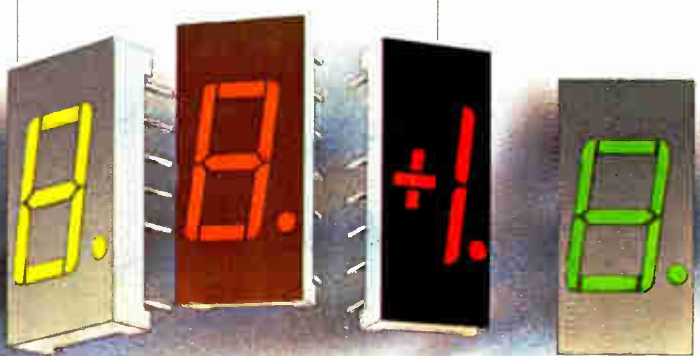

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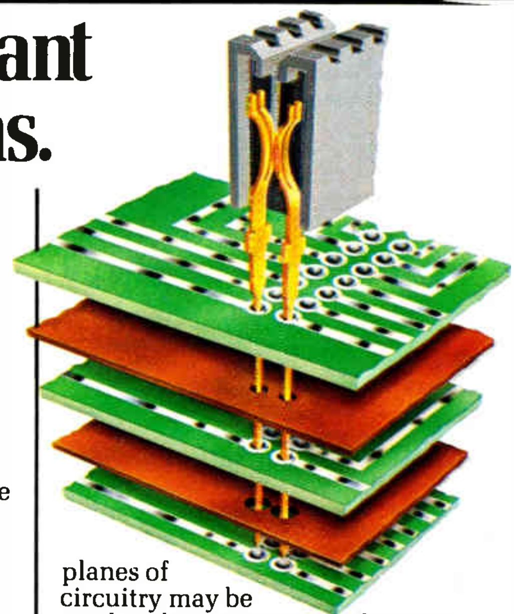

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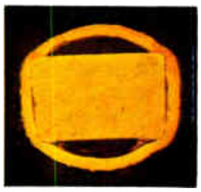
Key to the excellent reliability of the press-fit system is the gas tight joint formed as the contact pin, with a rectangular interface section or "bullet," is pressed through a plated-thru hole in the PC Board. The diagonal of the bullet is slightly larger than the diameter of the plated-thru hole, so that the hard phosphor bronze pin deforms the softer copper, forcing the copper plating to conform totally to the pin. Four complete lines of contact asperities run the full depth of the hole. The reliability of the Elfab press-fit is proven. With more than 500,000,000 contacts now in service—and that number growing at a rate of more than 1,500,000 every day—not a single interface failure has ever been reported.



Basically, an Elfab modular system is composed of the PC board, contact pin, and insulator connector housing. You have the flexibility to interconnect to as many voltage, ground and signal planes as you need. Standard options are available in sufficient numbers to cover almost any application. But if your design calls for a special configuration, almost any adaptation can be made—and with all the reliability and economy for which Elfab press-fit systems are noted.

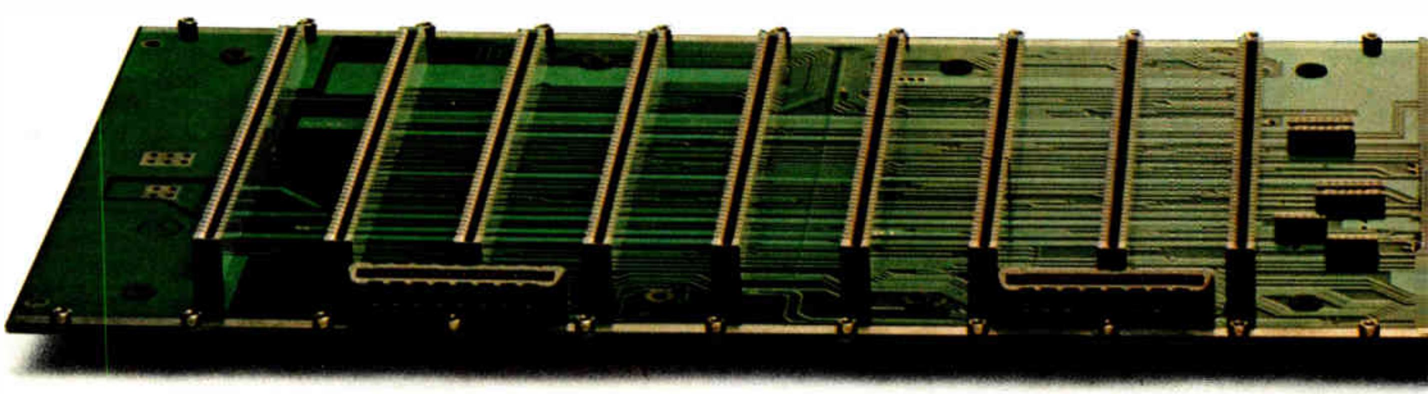
Let's start the design of your system with the printed circuit board. A basic system would start with a single-board, card-edge backpanel. Two layers of etched circuitry may take the place of part or all external wiring. Plated-thru holes accept the contact pins, making the board a structural part of the connector. Since no soldering of contacts is required, this system can effect savings of 5-10% over conventional soldering methods.

To achieve maximum circuit density, just stack additional boards together; all held fast by the press-fit contacts. Up to eight planes of circuitry may be used without any external wiring. This method is much more economical and much more flexible than the traditional laminated boards or metal plate and discrete connector assemblies.

Need extra high current capacity or positive voltage control? Make a hybrid out of the stack with pure copper insulated planes. This is excellent for today's high speed logic circuits. Select your own input/output specifications.

If electro-magnetic sensitive components are utilized, low-carbon steel sheets may be used between circuit layers for EMI, RFI shielding.

In short, whatever your circuitry



# of press-fit technology

requirements, you can get them in a compact package using Elfab's press-fit boards.

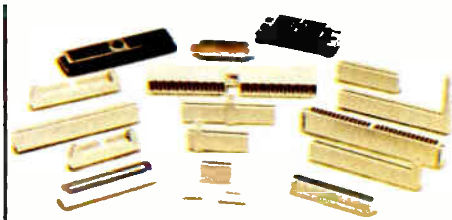
You can also select the exact contact pin to meet your requirements. Basic shapes for card-edge connectors include both cantilever and bellows contacts. The bellows contact has been made available in press-fit application by an innovation in production technique. The pin is placed in the plated-thru hole, then pulled into position to complete the gas-tight joint.

For customers with the volume to justify it, bellows contacts and insulator housings can be supplied, along with assembly equipment, so you can make your own backpanels.

Other contact pins available include: the straight post for applications which require a feed-thru I/O or access to signal or ground planes; the conventional screw machine contact for I.C. sockets; and many other contacts for specific purposes such as those for DIP sockets, "D" subminiature, etc.

A unique feature of all press-fit contacts is that they are removeable and replaceable on the board. And, growing in importance is the selective plating feature. Gold plating over base nickel is applied selectively to put the gold just where it's needed.

Insulator connector housings can be of just about any configuration you need. Standard edge-board connectors come in a choice of seven grid spacings—from .100" x .100" to .200" x .200". Modular construction makes length completely at your option with no special tooling required. Specialty configurations include: Dual In-Line packaging, "D" Subminiature, Ribbon Cable, 25 pair telephone and communications connectors, end and center connector card guides, DL connectors with "zero insertion force," and others as required.



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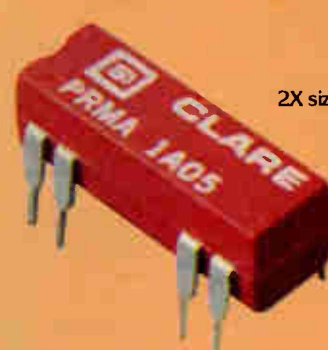

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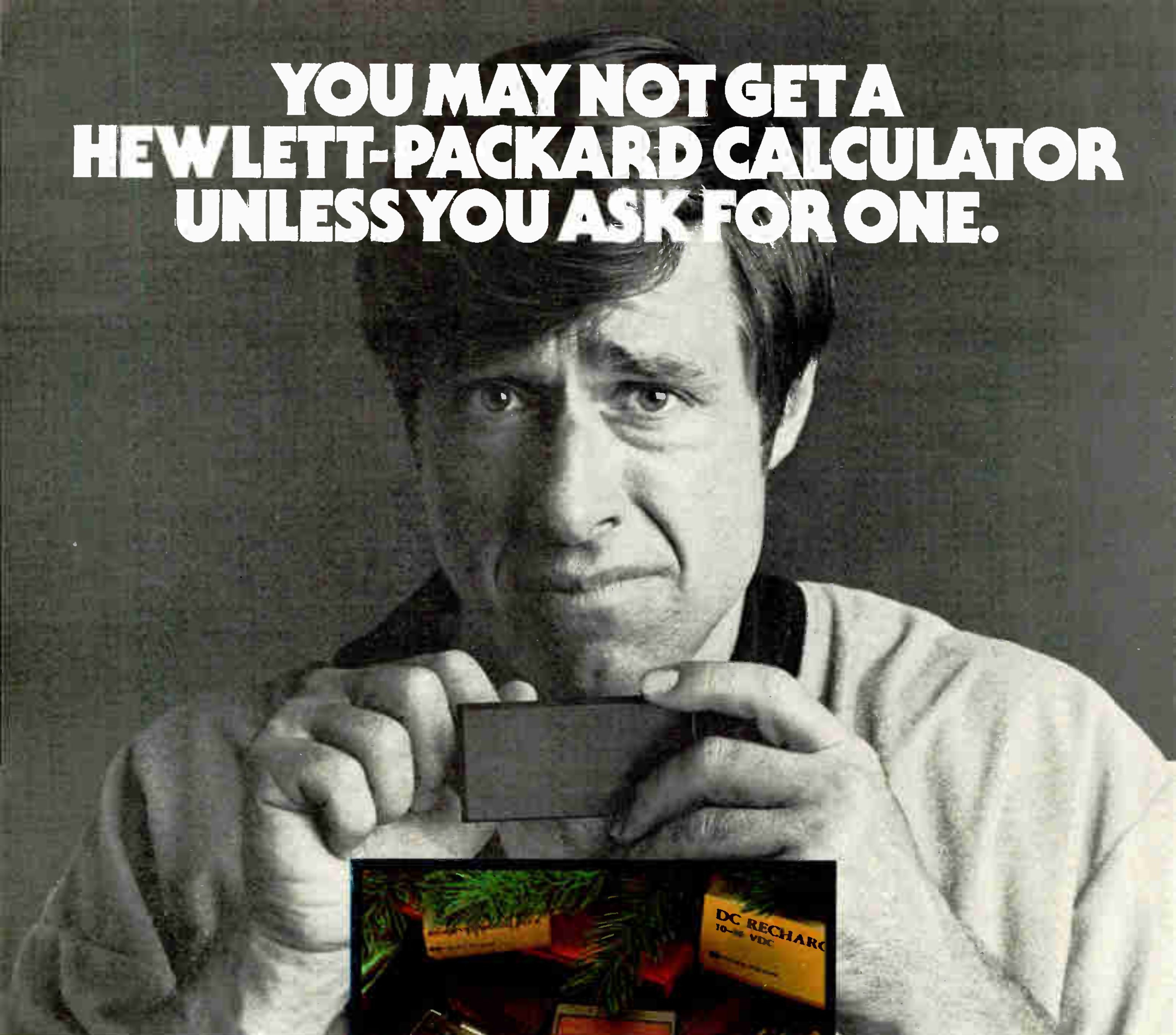

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V-MOS outstrips bipolar for power

V for V-groove MOS logic may be out of the ballgame, but V for vertical power MOS FET is headed for victory

by Bruce LeBoss, San Francisco regional bureau manager

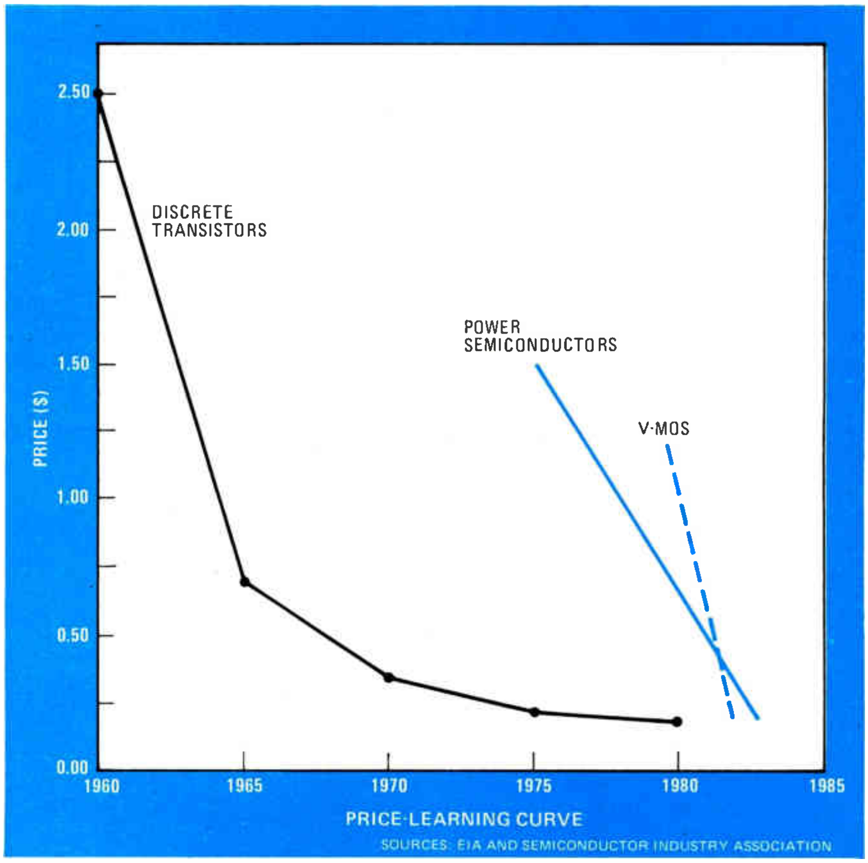
The high hopes once held for V-groove MOS technology as a mainstream logic technology have faded [*Electronics*, Oct. 11, p. 43], but the V might mean victory elsewhere. For it now seems that V (as in vertical) MOS, a more widely applicable technique, is going to be a winner in at least the power field-effect transistor market.

Some suppliers of V-MOS power FETs predict these devices may just eliminate bipolar versions in the next five years. Other semiconductor makers, particularly those with a vested interest in the bipolar market, are less optimistic. Nonetheless, the rush to the V-MOS power FET field by a growing number of suppliers, among them Texas Instruments, Motorola, RCA, Siliconix, Solitron Devices, and Intersil, suggests that such parts will replace the bipolar transistor in many applications. The lure is improved performance and many new circuit opportunities nonexistent with bipolar technologies.

These other manufacturers of V-MOS power FETs are not necessarily using the same process as AMI. V-MOS is actually the generic name for a power FET structure that allows the current to flow vertically from the source on top of the chip to the drain on its backside, whereas the "V" in AMI's process referred to a device with truly V-shaped grooves, which decreased active area and boosted packing density.

Adding to the confusion is the fact that several suppliers of V-MOS power FETs do, indeed, build their devices with V grooves. For example, Siliconix Inc. of Santa Clara, Calif., the acknowledged leader in the field, employs a V groove, as does TI for certain V-MOS power FETs it is now producing in prototype quantities. Intersil Inc. of Cupertino, Calif., which entered the V-MOS power FET field this summer, employs a groove with a distinctive flat bottom to eliminate certain electrical and mechanical stresses associated with conventional V grooves.

Whereas both TI and Intersil are using variations of the V groove for low-voltage power FETs, both are adopting a vertical D-MOS (double diffused MOS) process for higher-voltage (typically 400 V and above) power FETs. Intersil is calling its process Z-MOS while TI says it is not ready to talk about its particular high-voltage structure, except that it has to do with gate-source spacing on the surface of the chip. Motorola Semiconductor Products Group in Phoenix is about a full quarter away from introducing products that use a vertical structure it calls T-MOS. And then there is the Hexfet, a planar technique with vertical current flow pioneered by International Rectifier



Convergence. As V-MOS power FETs come down the price-learning curve, their price premium should approach 10% in two to three years and be 10% or less in three to five years.

Corp. It has hexagonal-shaped p regions on the surface of the chip to lower on-resistance.

RCA moves in. RCA Corp.'s Solid State division in Somerville, N. J., has a "very active power MOS FET program" and has looked at several competitive structures from which it will pick one, says Dale Baugher, manager of power applications. "In the next six months, we will be in a position to sample," he adds. RCA finds that overlay structures like International Rectifier's to be most attractive because "you have separate independent devices everywhere on the pellet." What's more, he continues, "because the cells are small, you can achieve a high current-handling capability and a low on-resistance."

Though V-MOS represents a small segment (about $6 million, or less than 1%) of the $700 million discrete power market, compared with about $200 million for bipolar power devices, expectations that it will capture virtually all of the discrete power sockets in less than a decade are understandable. "We had been in the bipolar power transistor business for about five years, and had become well established in it, but we could see a tremendous future potential for V-MOS power FETs," states Brian Pelly, vice president of applications engineering at International Rectifier Corp.'s Semiconductor division in El Segundo, Calif. "They are clearly a superior device to bipolars in a number of ways," he says.

One inherent advantage of the V-MOS parts, Pelly notes, is that they have a much higher gain. Theoretically, the MOS FET device has an infinite gain compared to a relative finite gain for bipolars. "But typically, a MOS FET has a gain on the order of 10^9 whereas the equivalent bipolar part has a gain of 10^2 or 10^3," he adds.

Secondly, MOS FETs have very high switching speeds, "an order of magnitude faster than bipolar," says Tom Daly, V-MOS product marketing manager at Siliconix. For example, typical V-MOS devices switch in nanoseconds, while bipolars do so in milliseconds, he says.

Furthermore, V-MOS devices do not suffer secondary breakdown. "They can operate at full rated currents and voltages," unlike bipolars which would be destroyed, points out Daly. What's more, V-MOS devices have a positive temperature coefficient and do not exhibit thermal runaway. By contrast, he continues, "bipolar transistors draw more current when they heat up. With V-MOS you can parallel parts without having to use protection devices to prevent them from hogging, or conducting, more current."

Not surprisingly then, some suppliers expect V-MOS power FETs to take no less than a 20% share of the marketplace for new designs in two to three years, and 40%, if not "a leading share of the market within five years," in the words of Siliconix' Daly. "What will tip the lion's share of the market away from bipolars to power MOS FETs in the end will be pricing," adds International Rectifier's Pelly. He doesn't think V-MOS power FET prices will ever get "quite close to bipolar levels. Users will always pay a premium."

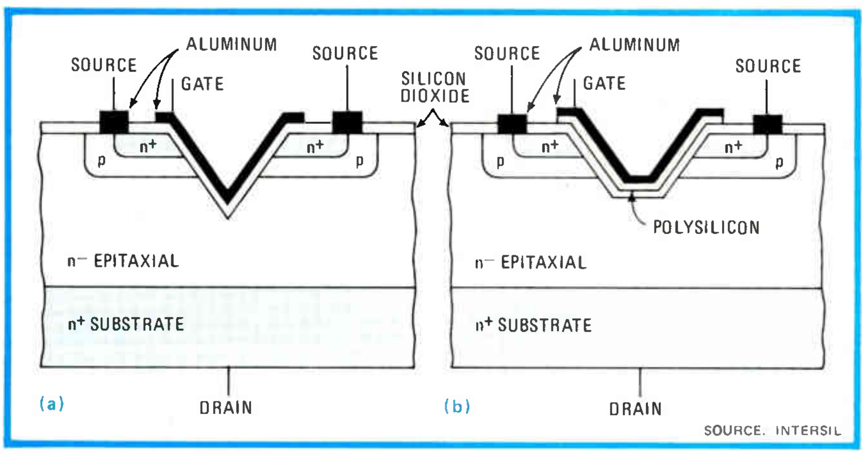
However, Daly believes "there's nothing to prohibit V-MOS prices from getting below bipolar levels." Pricing will go down, "even if we have to push it down. It is too big a market to ignore, and, if we have to, we will push our pricing down to meet our growth objectives."

V-MOS power FET users are paying an artifically high premium over comparable bipolar parts at higher voltage ratings, "as much as 10 times more," notes International Rectifier's Pelly. By comparison, there's "about a 25% to 50% premium at the low-voltage range," adds TI's Frank Taylor, manager of market planning for power products. As power FETs go down the learning curve, the price differential "should be a lot closer, perhaps, approaching 10% within two to three years, and 10% or less in three to five years. Intrinsically, it doesn't cost that much more to make power FETs."

Although Taylor forecasts that V-MOS FETs should average a 40% to 50% annual growth rate for the next five to eight years, he still sees bipolar power devices growing 10% to 15% yearly.

"Don't count bipolars out. We don't feel the day of the bipolar is gone. While V-MOS has some advantages, it is not a panacea," he adds. "Power FETs have some catching up to do with bipolars with respect to voltage and current." The automotive, consumer, industrial and peripheral equipment markets, Taylor continues, "will support growth of bipolars while allowing new technologies, such as V-MOS power FETs, to grow at an even faster rate."

The high-voltage area (250 V and up) is where Motorola is concentrating its V-MOS power FET activity. "We think their forte will be in power switching, and that implies higher voltages," states Tom Ruggles, manager of power products planning in Phoenix. "Power FETs will be competitive with bipolars at the high-voltage end, but in low-voltage applications they will have a tough row to hoe economically against bipolars." □



Getting the point. At left is the conventional metal-gate V-MOS structure, while the Intersil version, at right, sports a flat bottom groove and an additional layer of polysilicon.

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For technical data circle no. 87

E2 11/79

Military electronics

EIA sees good news at Pentagon

Electronics spending seen growing from 21% of budget to 26% over next decade; microprocessors and computers top the list

by William F. Arnold, Electronics

Take away salaries, pensions, and military construction and housing—the housekeeping portion of the defense budget—and the percentage of remaining expenditures devoted to electronics will rise from 21% in the 1980 fiscal year to 26% in fiscal 1989. That is the conclusion of a forecast of the Defense Department's budgets by the Electronic Industries Association (EIA). It adds up to some cheering news for electronics companies, although it could bring some gloom to those firms on the hardware side of the business. The message for electronics companies: modify and upgrade.

Leading the way on the military expenditure list will be data-processing equipment, as the EIA expects the Defense Department to embrace microprocessors and computers in a big way. "If I were a computer house, I'd have every salesman out on the street tomorrow," observes Henry Bourgeois of Singer Co., who was one of the industry officials to present the EIA forecast at a San Francisco meeting last month.

Basically, the EIA estimates that the overall Pentagon budget will rise slowly from $137 billion in fiscal 1980 to $151.3 billion in fiscal 1989 measured as total obligation authority in constant 1980 dollars. Defense electronics, spread out among programs in research and development, procurement, and operations and maintenance, will grow $19.2 billion to $26.6 billion over the same 10 years. In percentage terms, the electronics content of R&D will rise from about 39% to almost 46%, indicating the introduction of all kinds of hot technological development. The percentage in procurement will rise from the low to the high 30s during the same period.

Economy pressure. The Defense Department wants an annual 3% increase—in real terms (on top of inflation)—to meet its expanding hardware needs and fund an arsenal of new programs. That sounds good, but "I don't see how they will get 3% to 4% real growth after inflation once the election is over and SALT II [Strategic Arms Limitation Treaty] is signed," declares Frank Forthoffer, senior business planner in the new business planning operation at Lockheed Missiles and Space Co., Sunnyvale, Calif., who was the keynote speaker at the San Francisco meeting. "There will be pressures to hold down spending," he adds. "It looks as if none of the services will be able to buy what they want."

Worse, "the number one problem in the Defense Department is affordability," declares James L. Lee of Hughes Aircraft Co., who also presented parts of the EIA's forecast. "In the next decade, cancellations could well exceed new starts," he says, pointing out that the number of R&D programs standing by in the pipeline exceeds what is available in the budget to pay for them by a factor of three or four. And, after subtracting pay and housing costs from the forecast, money for R&D, procurement, and operations and maintenance rises only from about $91 billion in 1980 to $101 billion-plus 10 years later.

Another dampening factor is that

DEFENSE SPENDING FIGURES (in billions of 1980 dollars)

	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989
Research, development, test and engineering, total ($)	13.8	13.6	13.4	13.6	13.8	14.0	14.1	14.3	14.5	14.7	14.9	15.1
Electronic content ($)	4.9	5.1	5.2	5.5	5.7	6.0	6.1	6.3	6.4	6.5	6.8	6.9
Electronic content (%)	35.5	37.0	38.8	40.7	41.3	42.9	43.3	44.1	44.1	44.2	45.6	45.7
Procurement, total ($)	36.5	34.8	35.3	35.9	36.0	36.1	36.6	37.1	38.2	39.4	40.6	41.9
Electronic content ($)	11.0	10.6	11.0	11.5	12.0	12.2	12.7	13.1	13.9	14.6	15.5	16.2
Electronic content (%)	30.1	30.5	31.2	32.0	33.3	33.8	34.7	35.3	36.4	37.1	38.2	38.7
Operation and maintenance, total ($)	42.0	41.7	42.6	42.8	42.8	42.9	43.1	43.3	43.6	43.9	44.2	44.5
Electronic content ($)	2.9	2.9	3.0	3.0	3.1	3.1	3.2	3.2	3.3	3.4	3.4	3.5
Electronic content (%)	6.8	6.9	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	7.8	7.9

SOURCE: EIA

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For technical data circle no. 88

E2 11/79

Probing the news

Defense Department must absorb some large programs that further squeeze the budget. Among them are such major projects as the proposed mammoth MX missile project, various fighter programs for the Air Force and Navy, the Army's new tank, and the Navy's new aircraft carrier.

On the aircraft side, for example, the real opportunities are in electronic upgrading to enhance the capabilities of existing airframes, according to Nathan L. Higginbotham, manager of government market research at McDonnell Douglas Corp. in St. Louis, who also is pessimistic about any real hardware growth.

But the industry researchers for the EIA, after picking their way through the more than 1,000 line items in a typical Pentagon budget and talking to key executives in government and industry, pinpoint a host of promising electronics technology areas besides computers. These include software, large-scale integration, night vision, millimeter waves, noncooperative identification of friend or foe, signal processing, and sensors in a variety of forms such as new-generation infrared and nonacoustic for undersea, land, and air use.

In addition, the EIA forecast identifies three areas that are especially promising for electronics companies: electronic warfare; tactical command, control, communications, and intelligence; and combat simulators and other training aids.

Electronic warfare procurement in fiscal 1980 already totals more than $1 billion. Modification of existing systems is the real growth area, and R&D spending among the three services totals $400 million in 45 program elements. Money here goes for such things as multipurpose sensors, advanced self-protection jammers, radar warning receivers, electro-optic processing equipment, and software management.

Countermeasures. Also promising in this area is counter command, control, and communications—also called command and control countermeasures—for which the Pentagon has drafted a policy this year. It should go from a $4.5 billion market in this fiscal year to $5.5 billion in fiscal 1989. R&D, now $1.5 billion, will show no real growth and may actually decline to $1.4 billion in fiscal 1989. All three services have such countermeasure programs.

The simulator segment should grow markedly with training programs driven by rising fuel costs and increasingly affordable computational technology. The EIA forecasts an $8 billion market over the decade. That expenditure will not be just for airframe simulators, but for training in electronic warfare, alpha radiation detection and the operation of such items as guns, missiles, and trucks. □

SPENDING BY CATEGORY (in billions of 1980 dollars)

	1980	1981	1982	1983	1984	1985	1986	1987
RDT&E and procurement								
Aircraft	4.4	4.4	4.3	4.2	4.2	4.2	4.2	4.2
Missiles	2.9	3.2	3.6	3.9	4.3	4.6	4.8	5.0
Space	1.6	1.8	1.9	2.0	2.1	2.2	2.3	2.6
Ships	1.6	1.6	1.6	1.6	1.6	1.5	1.6	1.7
Ordnance/vehicles/ other weapons	0.4	0.5	0.5	0.5	0.5	0.6	0.6	0.6
Electronics and communications	4.6	4.8	5.1	5.3	5.4	5.6	6.0	6.3
Military science, other, management and support	0.7	0.7	0.7	0.7	0.7	0.8	0.8	0.8
Operation and maintenance	3.0	3.0	3.1	3.1	3.2	3.2	3.3	3.4
TOTAL DEFENSE ELECTRONICS	19.2	20.0	20.8	21.3	22.0	22.7	23.6	24.6

SOURCE: EIA

Climb. Increases in electronic content of weapons programs are greatest, on a percentage basis, for missiles and space.

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Word processing

IBM widens office beachhead

Introduction of 5520 system fills hole in its text-editing capabilities and sets up interdivisional competition

by Anthony Durniak, Computers & Peripherals Editor

International Business Machines Corp. is preparing an across-the-board attack on the office of the future. The latest, and perhaps most competitive, weapon is the model 5520 Administrative System.

A shared-logic word-processing system that can support up to 18 work stations, the model 5520 was introduced by the company's Atlanta-based General Systems division earlier this month [*Electronics*, Nov. 8, p. 33]. The product, IBM's first shared-logic system, offers refinements necessary for text editing, including a larger 1,920-character display and a more sophisticated software package, that had been missing from its earlier machines.

"It's the first decent word-processing system they've put out," notes William Becklean, an industry analyst with Bache Halsey Stuart Shields Inc.'s technology group in Boston.

Available in five models, the 5220 lets its 18 work stations share the computer necessary to implement the word-processing functions, as well as up to 130 megabytes of fixed disk storage, 23 megabytes of on-line diskette storage, and 12 printers.

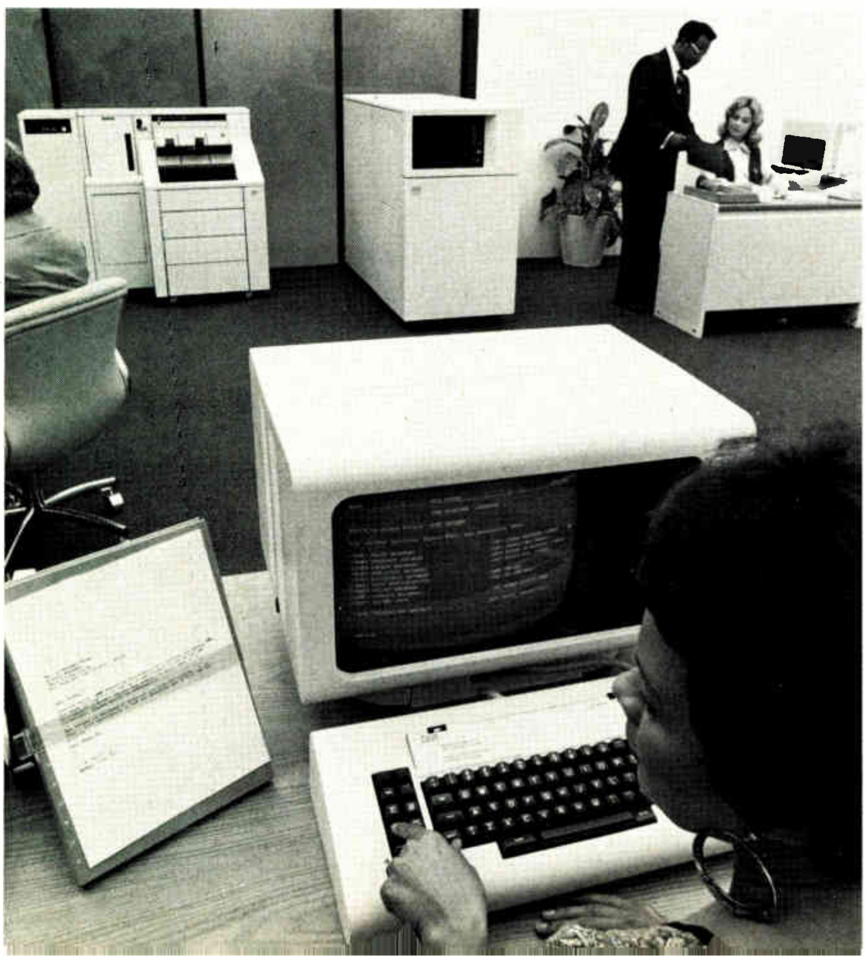
No details. The unit has what appears to be an interesting hardware configuration that couples between two and five 16-bit processors to provide the necessary power. But IBM will not reveal any details about the processors, how they are interconnected, or the size and type of main memory they employ. The company confirms, however, that the units use its 8-inch Winchester disk drives for the fixed-disk storage.

The Administrative Processing Program software necessary on the new machine provides more sophisticated text-editing features and an on-line Help facility that assists operators by guiding them through menus of available tasks and tutoring them on menu parameters and keyboard functions.

This software will also support electronic mail functions, such as automatic initiation and reception of calls to or from another 5520 and unattended storing and forwarding of documents. These calls can be programmed to be made at a certain time of day or when a certain quantity of documents accumulates, and they can be distributed according to routing lists in the system.

February start. Initial system shipments are scheduled for February 1980, but the full-blown systems will not be available until next November. Prices range from $64,351 for a low-end 5-station set up to $175,753 for one with 15 work stations and the maximum disk configuration. Software monthly license fee is $245.

But competitors, who have been aggressively eating into IBM's market share by offering many of those features on technically sophisticated



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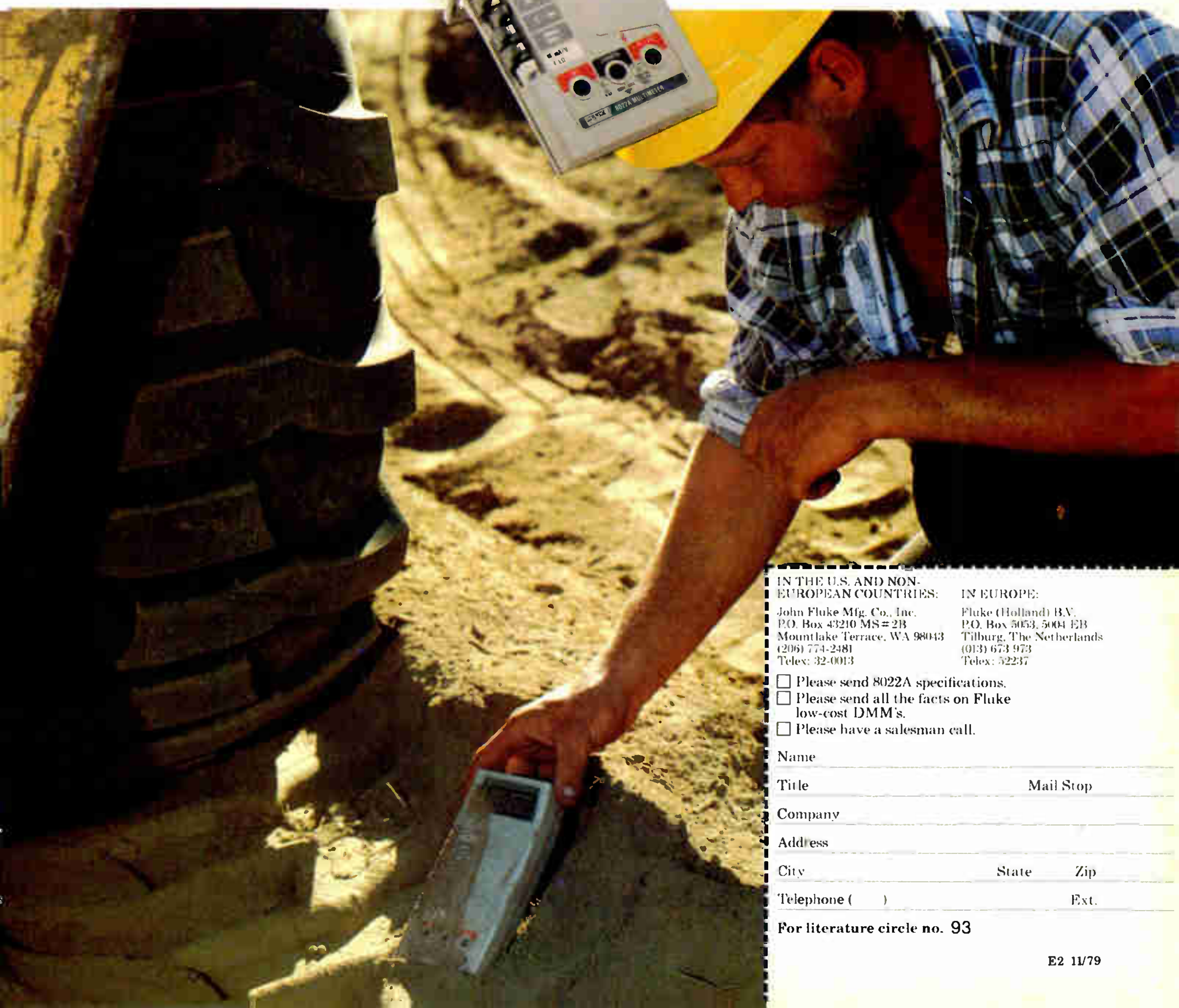

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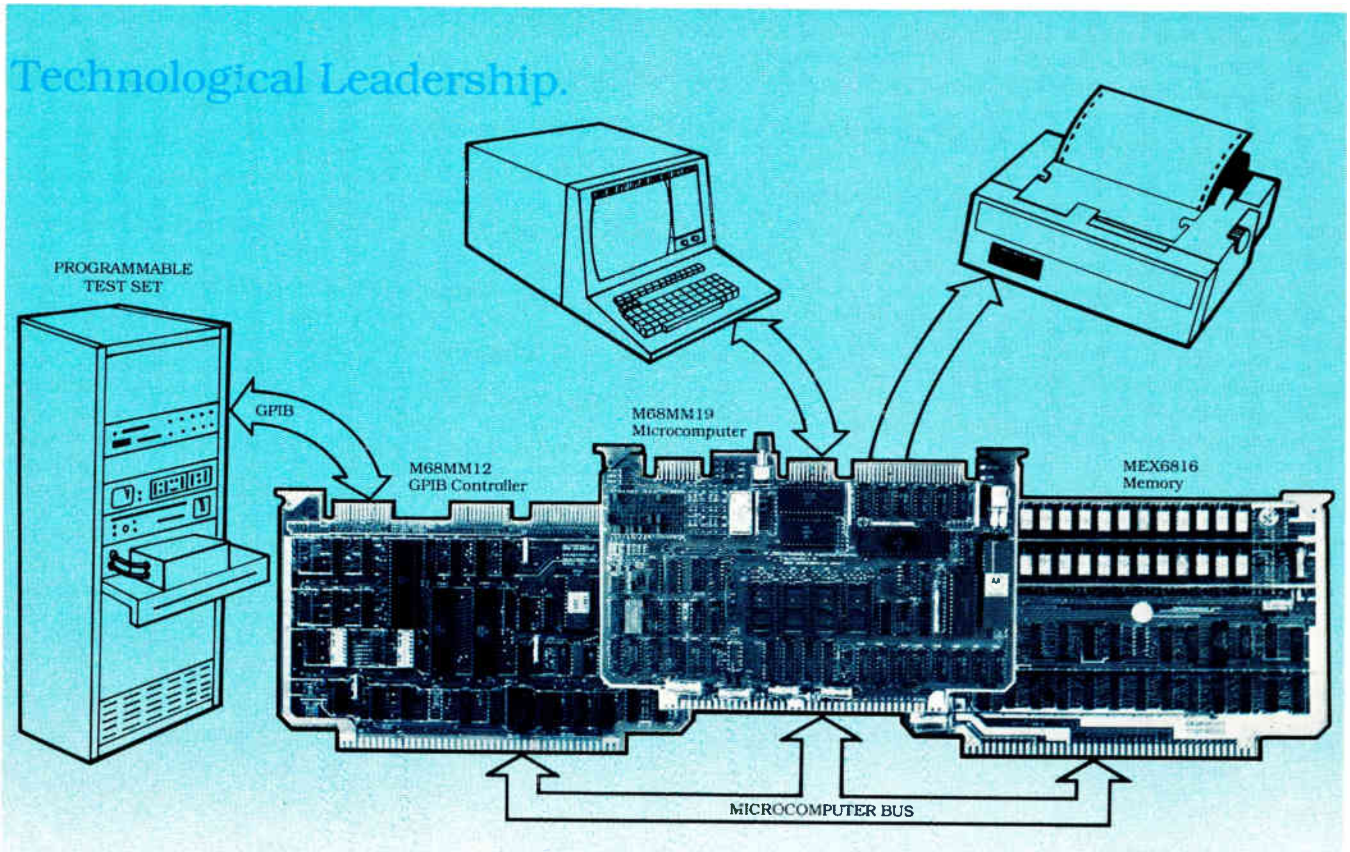

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Probing the news

products for the past few years, do not appear worried.

"The new 5520 is priced at between $15,000 and $16,000 per work station, and that's about a 30% premium over us," says John Cunningham, executive vice president for Wang Laboratories Inc., Lowell, Mass. Cunningham points out that Wang's Integrated Information Systems, introduced last June [*Electronics*, May 24, p. 34], offer additional capability, since they merge data- and word-processing functions on a single set of machines—something IBM is yet to do on the 5520.

Like others, Cunningham is surprised by the fact that IBM chose the General Systems division, its small-business computer maker, to sire the new product. Up to now the Office Products division, Franklin Lakes, N. J., which essentially created the word-processing market with its magnetic-tape typewriters in 1964, has been IBM's contender.

Now, though, all three divisions have word-processing capability. In addition to GSD and its 5520, the mainframe-marketing Data Processing division, White Plains, N. Y., has the model 3730 Distributed Office Communications System, introduced a year ago.

"We're seeing the emergence of a new marketing strategy from IBM," Beeklean notes. "Now there's a lot of product overlap and the divisions will compete."

Despite what might be market competition, the products can be very friendly once they are installed, a feature that may give IBM a leg up when it comes to fully integrating an office. The model 3730 is designed to operate with up to 12 work stations, linked to either a stand-alone controller or one attached to a System/370 host computer. When attached to the host computer, centralized electronic document filing, retrieval, and distribution can be performed, the company notes. The stand-alone Office System/6 from OPD can communicate with other machines in its family and communicating magnetic-card typewriters.

Talkative. The new 5520 can talk to all of these at speeds of up to 9,600 bits per second as well as IBM's innovative model 6640 ink-jet document printer and model 6670 information distributor—a nonimpact printer based on xerographic copying techniques. □

IBM unit types and talks

While International Business Machines Corp.'s General Systems division was entering the office equipment field, one formerly the exclusive preserve of the Office Products division in Franklin Lakes, N. J., the New Jersey group bolstered its line with a unique talking typewriter. Called an audio typing unit, it produces synthetic speech from typed information, thus enabling blind typists to "proofread" their own copy. The unit attaches to any of four IBM magnetic-media typewriters. A keypad allows the typist to select a variety of operating modes—from hearing the audio response for every key stroke to hearing the text in review.

An audio console contains 44 kilobytes of memory for the unit, of which 24 kilobytes holds language-dependent codes that change the text representation into phonetic representation and send prompts to a voice synthesizer. The synthesizer is a custom chip developed for IBM by the Votrax division of Federal Screw Works in Detroit. But IBM declined to elaborate on the chip's details or on marketing arrangements with Votrax.

The software for the audio typing unit includes preprogrammed pronunciation rules and discrete speech sounds, called phonemes. The voice synthesizer produces and blends the phonemes to form continuous speech. It also spells, sounds out punctuation and spacing, and indicates the typing position on the page. In addition, it verifies the mode and type size the typist has selected.

The unit was developed and is being manufactured at IBM's facility in Austin, Texas, and will sell for $5,300 or lease for $150 to $170 a month. It will be available in the U. S. and the United Kingdom for delivery by early 1980.

-Ana Bishop

Consumer electronics

Santa Claus feels chip pinch

Shortage may cause game deliveries to fall 20% below order level, as manufacturers generally remain loyal to IC suppliers

by Larry Marion, Chicago bureau

The stratospheric rise of popular interest in electronic games spells trouble for retailers and toy assemblers this Christmas, because chip suppliers will not only fail to meet demand, but will also renege on their commitments. Letters from Mattel Electronics Inc. of Hawthorne, Calif., and other assemblers are now going out to retailers with the bad news that deliveries of finished games may fall 20% short of the orders accepted only six months ago [*Electronics*, June 21, p. 42].

The shortfall comes at an awkward time for retailers. Sears, Roebuck and Co. of Chicago predicts that revenues from electronic game sales this year will represent the bulk of its 1979 toy dollars, a significant milestone for a product line that did not exist before 1977 but should gross $400 million or more this year.

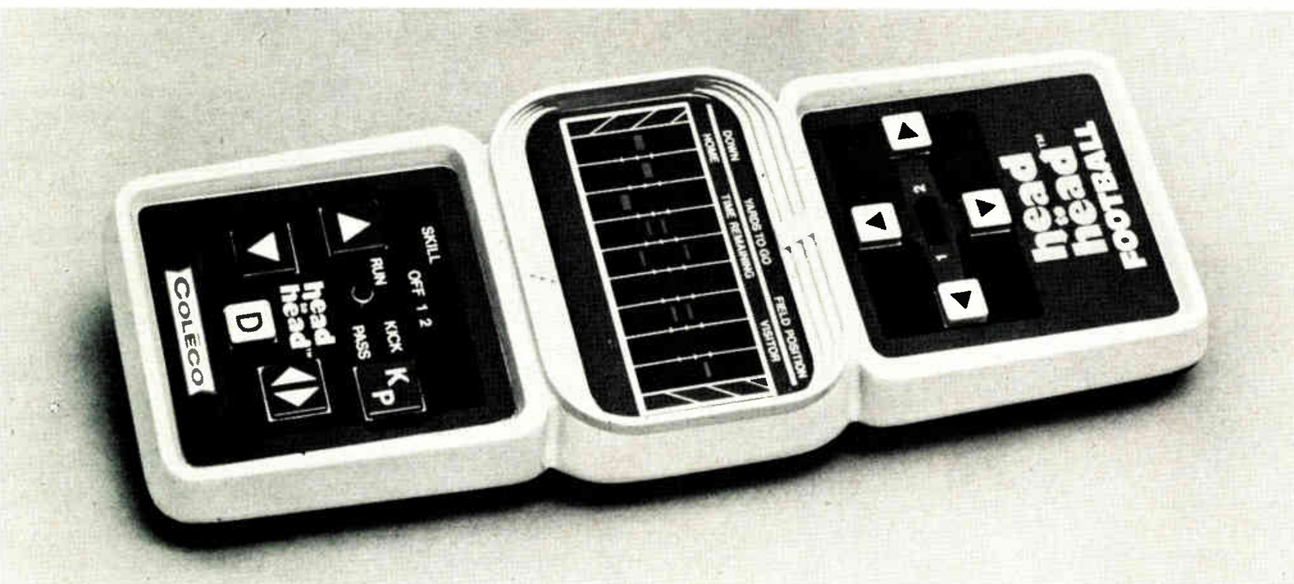
Michael J. Moone, vice president and manager of Milton Bradley Co.'s game division, Springfield, Mass., says a shortage of memory chips and the Texas Instruments 1000 family microcomputer will force shipments 15% to 20% below the size of its order book. "And it could get worse," he says, depending on the size and condition of mid-November deliveries: "We have seen some decline in the quality of chips delivered." Milton Bradley, like other toy manufacturers, usually limits itself to two chip suppliers (TI and Intel Corp.), but may add suppliers next year. "We're pursuing every avenue at this point," Moone adds.

Hanging in. Over at Mattel, "all large-scale integrated circuits are tight," laments Edward M. Krakauer, senior vice president and general manager. Rather than look elsewhere, Mattel is maintaining its "good relationships" with suppliers Rockwell International Corp. and National Semiconductor Corp., despite canceled shipments.

Although finding additional sources is a tempting prospect, toy makers are reluctant to spread themselves among multiple sources. Many of their toys require custom masks for the special features.

For example, Bradley's Big Trak tank is a programmable robot toy. Although the company uses comparatively low-level microprocessors such as the 4004 from Intel, it still cannot find loose supplies. "We would buy other chips if they were available," says Moone.

Krakauer of Mattel says he is unwilling to turn to other sources because of the expense and time necessary when custom products are



The appeal of electronics. Youngsters across America are turning electronic calculator-like games into a craze. Sears Roebuck expects them to make up the bulk of its 1979 toy sales, and the prediction is that total U. S. retail sales will come to about $400 million.

Shortfall. Michael J. Moone of Milton Bradley Co. says shortage of memory chips and microcomputers will cut shipments.

Fantasy. Electronic toys are gaining complexity. This is Mattel's Big Bird, a simulated fighter spacecraft with sound.

involved. Also, since the toy companies rely on outside semiconductor expertise more than a General Motors or a Ford, assemblers like Mattel do not want to betray their friends. "They're doing the best they can," say a sympathetic Krakauer.

Retailers, though, may not remain as calm when they learn that Mattel will drop at least one product from its fall delivery schedule and switch its supplies to higher-priced toy lines. "We will try to meet demand equitably," says Krakauer.

Some satisfied. Meanwhile, Parker Bros. Inc., the Beverly, Mass., toy subsidiary of General Mills, is in similar shape. In fact, it will go to second sources next year for almost every product, says Ronald Jackson, marketing vice president. Parker ranks behind electronic game leaders Mattel and Bradley.

All sides are reluctant to blame the others, because major toy assemblers and their suppliers this year boosted product plans two- or threefold. The heavy demand for semiconductors from the auto industry and the more traditional buyers is no help. Moreover, the popularity of electronic games last year—many leading products were sold out a month before Christmas, and a black market developed—led several more assemblers, including importers, to enter the market recently.

Some retailers are confident that they will receive, and sell, what they ordered. Major retail marketer K-Mart Corp., Troy, Mich., says, "there's no problem getting what we need."

Emphasis hit. But one electronic toy assembler sharply criticizes enthusiastic retailers like Sears. "They're paying too much attention to electronics, and not enough to the basics." Another assembler defends the principle, though she questions the timing, too: "We think that, eventually, electronics will be bigger" than the current champion, board games. Meanwhile, Sears' Christmas catalog includes 15 pages devoted to electronic football, baseball, and educational games, including Speak & Spell from TI.

Assemblers, already worrying about last-minute deliveries, are even starting to talk about a shakeout in the industry. "How many of seven football games can sustain themselves in the marketplace?" questions Moone of Milton Bradley. Adds Krakauer of Mattel, "I'm amazed at the number of products out there." To prevent its advertising from helping sell the me-too products of smaller competitors—customers looking for a sold-out advertised product will settle for an electronic product without a brand name—Bradley and Mattel are already pulling some advertising away from electronic products and increasing their plugs for traditional games. "Our greatest concern is if the consumer does not find our product available," says Moone. □

Meetings

Midcon sets attendance mark

17,000 attend Chicago show, 60% more than at first running two years ago; exhibitors say they're enthusiastic

by Roger Allan, Components Editor

Its sponsors had predicted—and hoped—that the third annual Midcon would be better than the other two, and they were right. Some 17,268 individuals passed through the doors of the O'Hare Exposition Center last month in Chicago to indicate that at least one segment of the economy, the electronics market, is still growing strong. The attendance was up 60% over the figure for the 1977 Chicago show, when the convention made its premier showing. Midcon alternates annually between Chicago and Dallas.

According to Midcon director James Ralston of the Allen-Bradley Co., Milwaukee, "The attendance was better than anything we expected. So was the professional program."

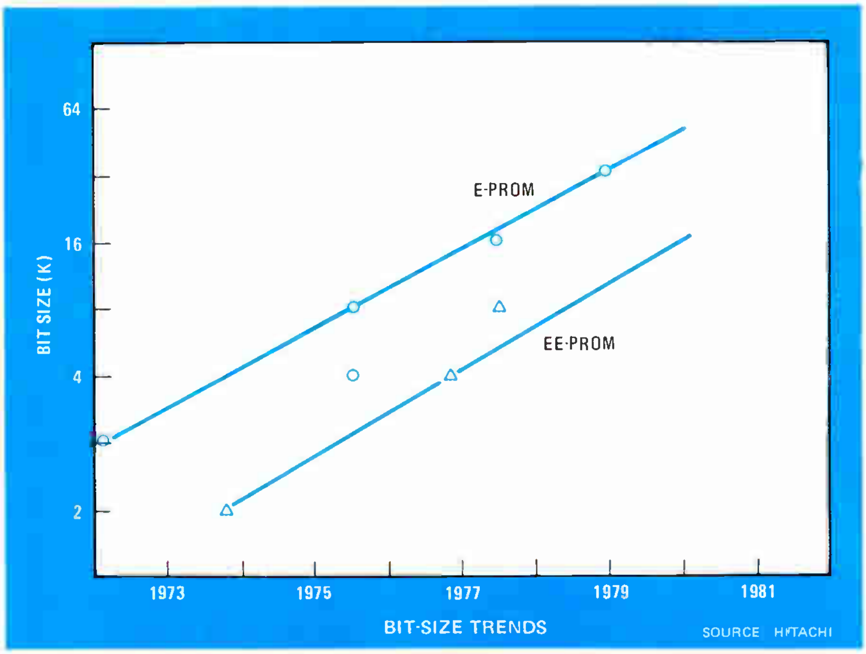
In fact, it was the right combination of a record number of exhibitors and a strong professional program that did the trick [*Electronics*, Oct. 25, p. 90]. Some 350 exhibitors occupied 535 booths, compared with 260 in 401 booths in 1977.

Exhibitors interviewed at random had nothing but praise and good marks for this year's show; many of them indicated that they would like to be back in Chicago in 1981. Dennis King, regional sales manager for Data Precision Corp., Danvers, Mass., said that "it was a good show. The quality of the leads was equal to that of Wescon and other major shows we've been in. We certainly might be back in two years."

Echoing his remarks was Frank Goodenough, technical promotion manager for Analog Devices Inc., Norwood, Mass. "An excellent show. The quality of the people stopping by our booth was as good as anything I've seen. We will be in Dallas next year," he said.

Some, such as Ernie Lutfy, sales manager for Krohn-Hite Corp., Cambridge, Mass., were surprised at the showing. "It's a pleasant surprise to us. The quality of the leads is high. We might be back in Chicago in two years," he said.

Two of the nation's largest integrated-circuit manufacturers, Intel and Texas Instruments, were exhibiting. Both of them plan to be in Dallas next year. Notably absent were instrument giants like Hewlett-Packard, Tektronix, Systron-Donner, and Dana Laboratories, although others like John Fluke and GenRad were present.



Getting bigger. Trend lines for E-PROMs and EE-PROMs show rapidly increasing size. A 32-K E-PROM is now available, and it appears that a 16-K EE-PROM will arrive very soon.

Varied program. Midcon's sponsors this year scrapped the traditional distributor-marketing seminar and keynote speech in favor of a more solid and varied professional program. The 29 technical sessions were sufficiently varied to attract virtually every type of engineer. For example, there were sessions reporting not only on exciting digital and analog IC developments, but also on advances in consumer, industrial, military, medical, manufacturing, energy, communications, instrumentation, and management areas.

About one third of the professional program dealt with device and device-related subjects that included analog-to-digital and digital-to-analog converters, microprocessors, control ICs, semiconductor memories of all types, and their system design considerations. As for the microprocessor, software is receiving greater attention than hardware. Anyone attending the session "Advanced Software Tools for Microprocessor-Based Systems" could see why as new-generation software languages and development systems were discussed. Mark Krieger of Whitesmiths Ltd., New York, explained what the C language for Z-80- and 8080-based microprocessor systems was like. He predicted that by next year C will be available on some 16-bit microcomputers as well as on the IBM System/mainframes.

Also from Whitesmiths was P. J. Plauger, who reported on the development of a UNIX-like minicomputer operating system called Idris. (UNIX was developed at Bell Laboratories in the early 1970s.) Although it is similar to UNIX, Idris was designed from the ground up. According to Plauger, it is pin-for-pin compatible with UNIX on some popular minicomputers like the PDP-11 and microcomputers like the LSI-11.

Skip Stritter and Don Weiss of Motorola Inc.'s Austin, Texas, facility described how Pascal was used for the firm's 6809 and 68000 microprocessors. Also discussed was an extension of Pascal to support commercial and industrial microprocessor uses.

Count. Ever wonder how many electrically erasable programmable read-only memories, or EE-PROMS, there are in use in the field? Over 6 million, according to John Wunner of General Instrument Inc., Hicksville, N. Y., who gave a paper on the many applications of these devices in a session titled "Future Trends in Nonvolatile Memories."

Yokichi Itoh of Hitachi Ltd.'s Central Research Laboratory, Tokyo, reported on his firm's efforts to develop a 16-K EE-PROM with a 200-nanosecond read-access time. Expected to be ready in sample quantities by the first quarter of next year, this metal-nitride-oxide-semiconductor device is not word erasable. ☐

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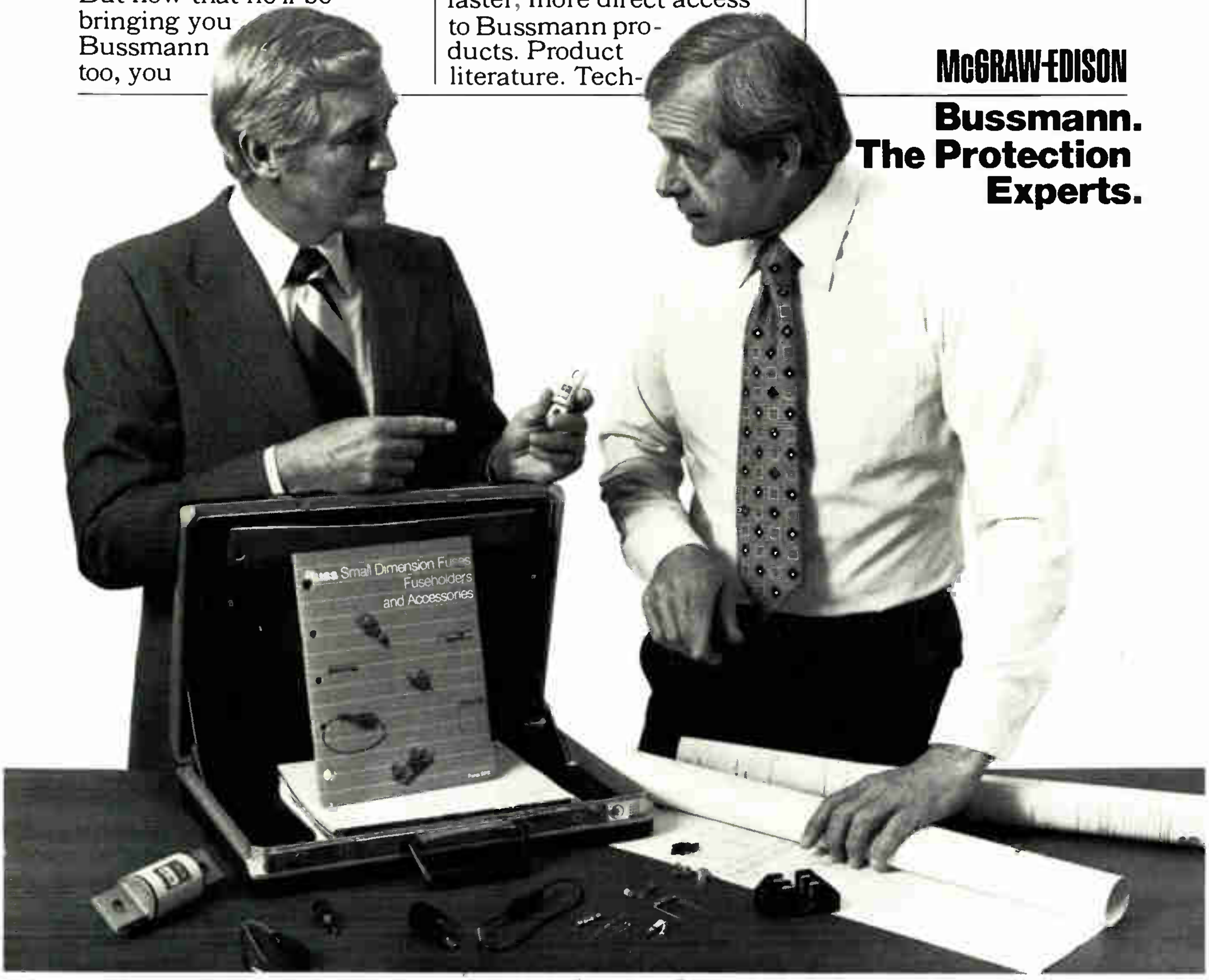


Applying the Hamming code to microprocessor-based systems

Three practical circuits automatically detect and correct bit errors in 8- and 16-bit machines

by Ernst L. Wall, *International Telephone and Telegraph Corp., Telecommunications Technology Center, Shelton, Conn.*

☐ For years, digital communications systems, unattended data-gathering equipment, and computers have used special codes to detect and correct errors in data words. The Hamming code, first proposed back in 1950, has generally been employed in systems with few errors and would be ideal for many microprocessor-based applications. But information on the circuits that implement the code has customarily been regarded as proprietary.

The detail in which the following three circuits are discussed is therefore particularly valuable. The designs were developed specifically to assure the accuracy of 8- and 16-bit microprocessor applications.

Two of the circuits detect and correct single-bit errors in 8- and 16-bit words, in real time, for a minimum delay in program execution. They use hardware only. The other, which will be described first, is an 8-bit circuit that does not function in real time. Its data- and address-capture latches are read by software and this data is used to correct single-bit errors and also detect double-bit errors. It is less practical than the real-time circuits for unattended locations because it does not correct errors without immediate interrupts during program execution.

In addition to the required TTL overhead, there is an

APPLYING HAMMING CODE TO A 16-BIT DATA WORD

BIT CONTENT		H_0	H_1	D_0	H_2	D_1	(D_2)	D_3	H_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	H_4	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
BIT POSITION		1	2	3	4	5	(6)	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
POINTER WORD P_0 →	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
(P_1) →	0	0	1	1	0	0	(1)	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
(P_2) →	0	0	0	0	1	1	(1)	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
P_3 →	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
P_4 →	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

← 16-BIT PROCESSOR ONLY → (D_{11} to D_{15})

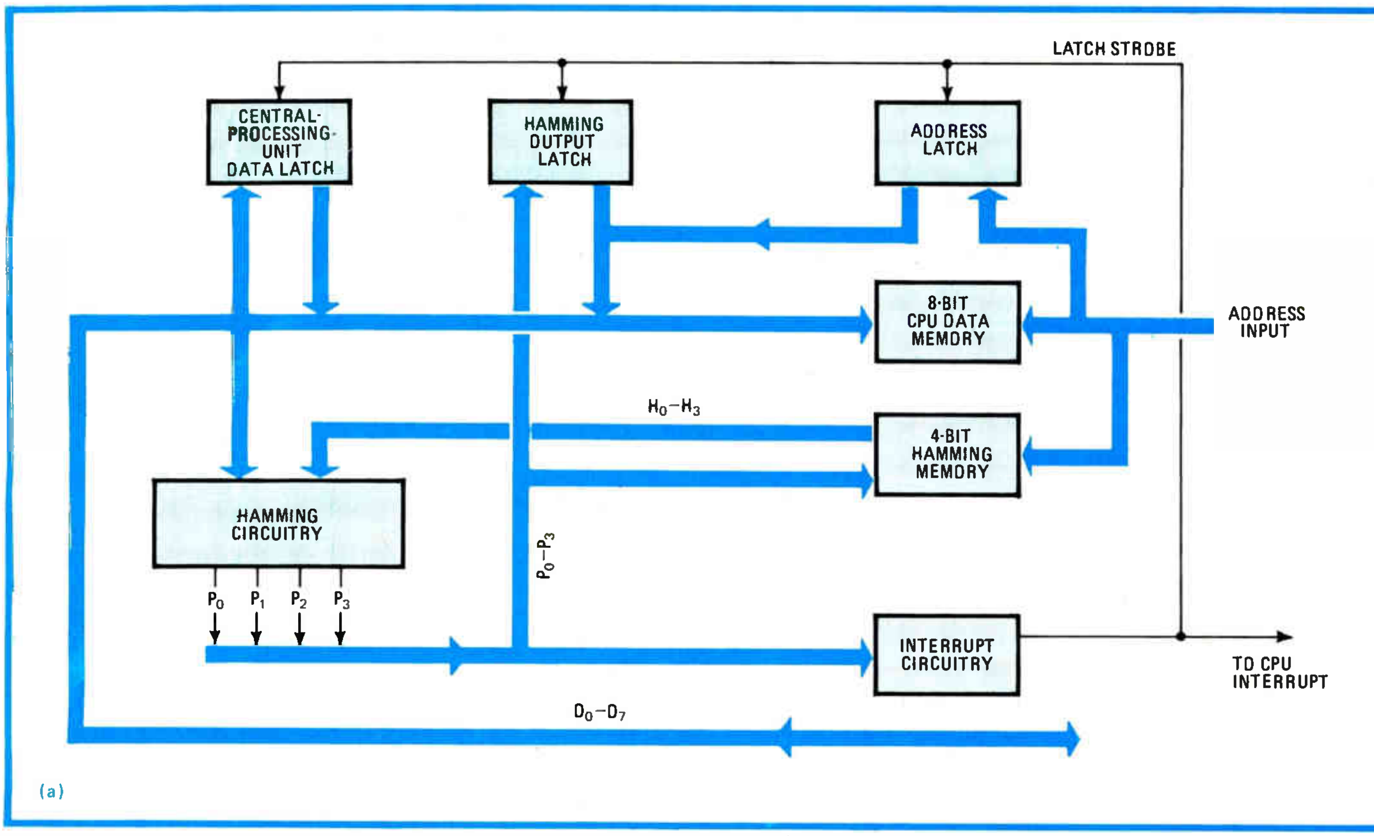
$$P_0 = (H_0 \oplus D_0 \oplus D_1 \oplus D_3 \oplus D_4 \oplus D_6) \oplus D_8 \oplus D_{10} \oplus D_{11} \oplus D_{13} \oplus D_{15} = 0$$

$$\textcircled{P_1} = (H_1 \oplus D_0 \oplus \textcircled{D_2} \oplus D_3 \oplus D_5 \oplus D_6) \oplus D_9 \oplus D_{10} \oplus D_{12} \oplus D_{13} = \textcircled{0}$$

$$\textcircled{P_2} = (H_2 \oplus D_1 \oplus \textcircled{D_2} \oplus D_3 \oplus D_7) \oplus D_8 \oplus D_9 \oplus D_{10} \oplus D_{14} \oplus D_{15} = \textcircled{0}$$

$$P_3 = (H_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7) \oplus D_8 \oplus D_9 \oplus D_{10} = 0$$

$$P_4 = (H_4 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} = 0$$



1. Software, too. If there is an error, the timed interrupt circuit interrupts the 8-bit processor and pulls the latch-strobe-out line low (a), trapping address, data, and parity in latches B–E (b). Chips G–J solve the Hamming equations; K and O sum the overall parity.

extra memory overhead: 5 extra Hamming code bits are added to an 8-bit machine and 6 bits to a 16-bit machine when both single-bit correction and double-bit detection are used.

A choice

All three circuits operate at the same speed but the circuit of Fig. 1, the 8-bit software and hardware approach, is slightly faster than the 8-bit real-time approach (circuit 2) because there are fewer TTL propagation delays. The non-real-time approach also requires that the correction program be stored in a memory array that is much more reliable than the memory array that is being checked. Otherwise, an error in the correction program could produce incorrect results.

The Hamming parity-checking circuitry of course increases the propagation time of the signals in all three. But in the real-time approach, the additional propagation delays inherent in these circuits could necessitate adding "wait" states to a fast processor, thus slowing it down. On the other hand, in applications such as telecommunications, disrupting a control processor at random times to correct errors could cause considerable difficulties.

What's the code?

How the Hamming code works can be explained in terms of Table 1.

The top row, labeled "bit content," shows the structure of a 16-bit data word in which Hamming bits have been inserted. The 5 H_i bits are parity, or Hamming, bits, and the 16 D_is are the data bits. Beneath each bit

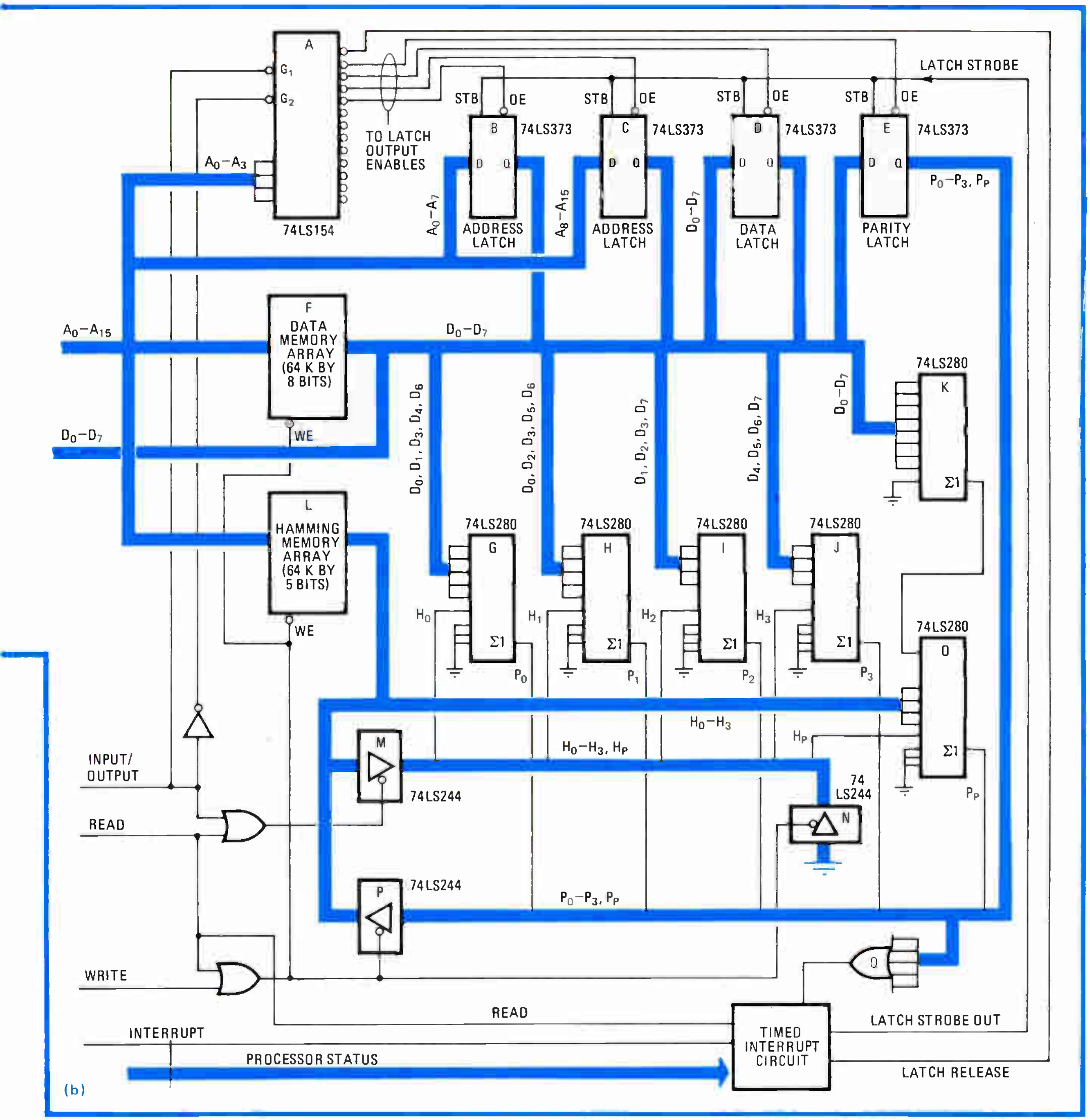
Hamming is still showing the way

According to the citation in his latest award from the Institute of Electrical and Electronics Engineers, Richard W. Hamming, the inventor of the Hamming code, has been a leader in the "introduction of error-correcting codes and [has] done pioneering work in operating systems and programming languages and the advancement of numerical computation."

This is the wording in the 1979 Emanuel R. Piore Award given to the 69-year-old Ph.D. mathematician at the computer conference, Compcon Fall, in September in Washington, D. C.

Hamming has been with the faculty of the Naval Postgraduate School since 1976, following a 30-year career with Bell Laboratories in Holmdel, N. J. There, he worked on applying computing theory to military and telephone research. He published his first Hamming code paper in the Bell System Technical Journal in 1950. It supplied the basis for the error-detecting and -correcting codes today found in almost all data-communications and computer systems and remains perhaps the most important of his publications, which include several books and over 100 other technical papers.

-Harvey J. Hindin

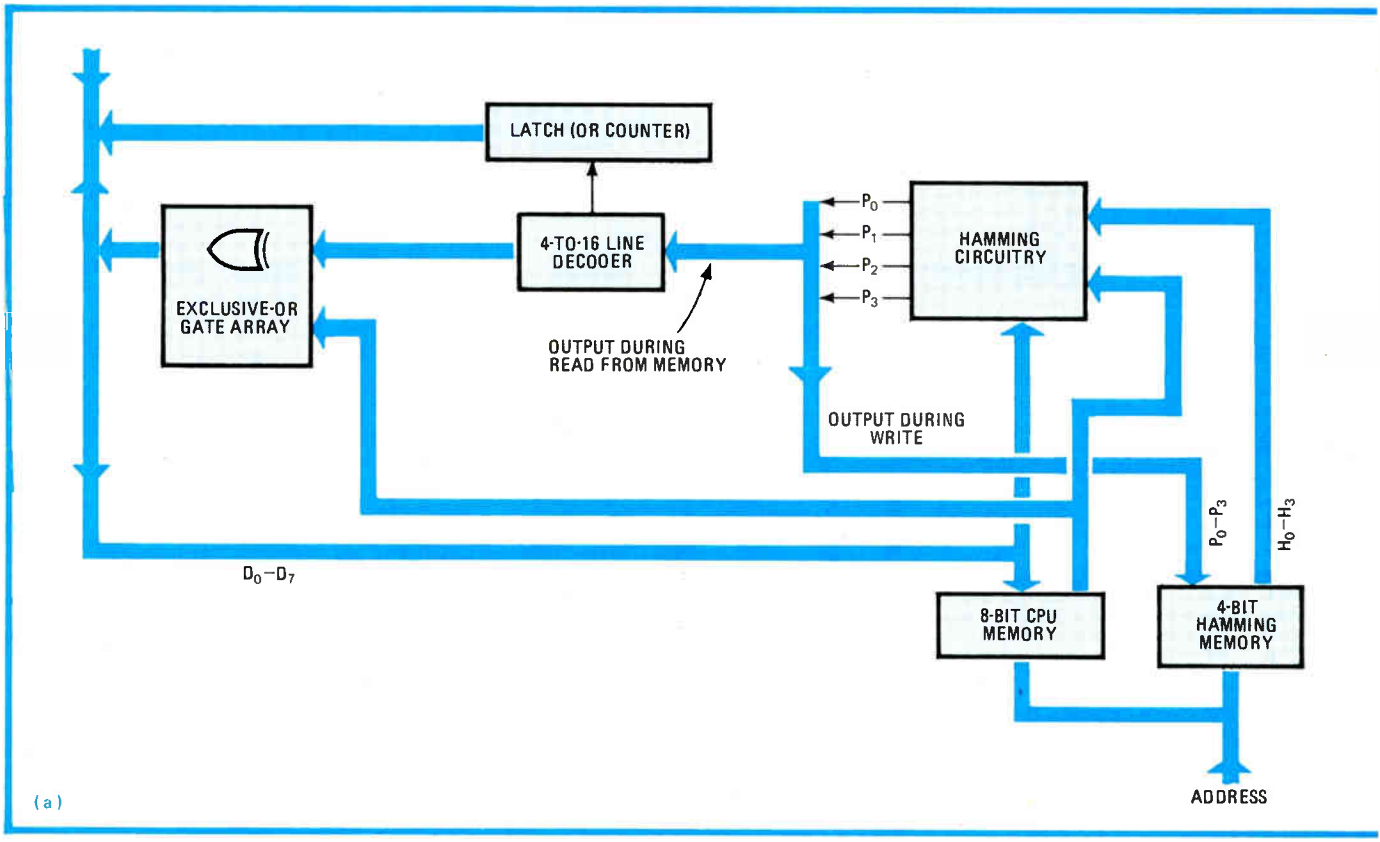


position number, shown in base 10, is a column containing a 5-bit binary number, which is equal to the bit position number and is called a pointer word. (The uppermost bit is the least significant, the bottom one the most significant.)

Table 1 and the equations below it are based on Hamming's work. The latter are exclusive-OR combinations of the data and the Hamming bits. Note that each Hamming bit occurs in only one of the equations and is associated with a different combination of data bits. It is generated as the even parity of the data bits in its equation—that is, it rounds out the sum of the data bits to an even number by being set at 0 or at 1.

Thus, when summed with their associated data bits during a read from memory, the Hamming bits yield either 0 (if there is no error), or 1 (if a data or Hamming bit is in error). (See "Computing Hamming bits," p. 110). In the latter case, the five P_j equations taken together yield one of the 16 5-bit pointer words in Table 1. In other words, any single-bit error produces a 5-bit pointer word that indicates its position in the word and may be used to trigger either hardware or software to correct the erroneous bit by inverting it.

A standard, fixed order is used to insert the Hamming bits that is invariant regardless of data-word length. Thus the 2 Hamming bits needed to check a 1-bit binary



2. Real time. In this 8-bit circuit and block diagram, if there is an error, the parity outputs P_0–P_3 select the appropriate output of chip I, which inverts the data bit that was wrong. One error can be detected and corrected, but two errors cause failure.

data word precede the first data bit; the extra Hamming bit that would be needed to check a 2-, 3-, or 4-bit data word follows the first data bit and precedes the second; the fourth Hamming bit needed to check 5-through-8-bit words follows the fourth data bit and precedes the fifth, and so on.

This invariance has two important—and elegant—consequences. First, it makes it possible to arrange the equations so that, when a bit is in error, they yield the binary equivalent of that bit's ordinal position in the word. Second, the user's task is simplified: he or she just chops the sequence of Hamming and data bits (and the accompanying equations) off at the point that includes the number of data bits in his or her word, thereby using the fewest possible number of Hamming bits needed to detect 1-bit errors.

To detect a double error, a simple parity check over all bits—Hamming and data—can be added to the procedure. An odd number of bit errors will generate an odd parity, a zero or an even number of bit errors will generate an even parity. A single-bit error in a word can be detected and corrected; a double-bit error can only be detected. The probability of having no more than two errors may reasonably be assumed for many systems. However, it is a necessary assumption here, for the scheme actually breaks down for three errors.

Why all the fuss?

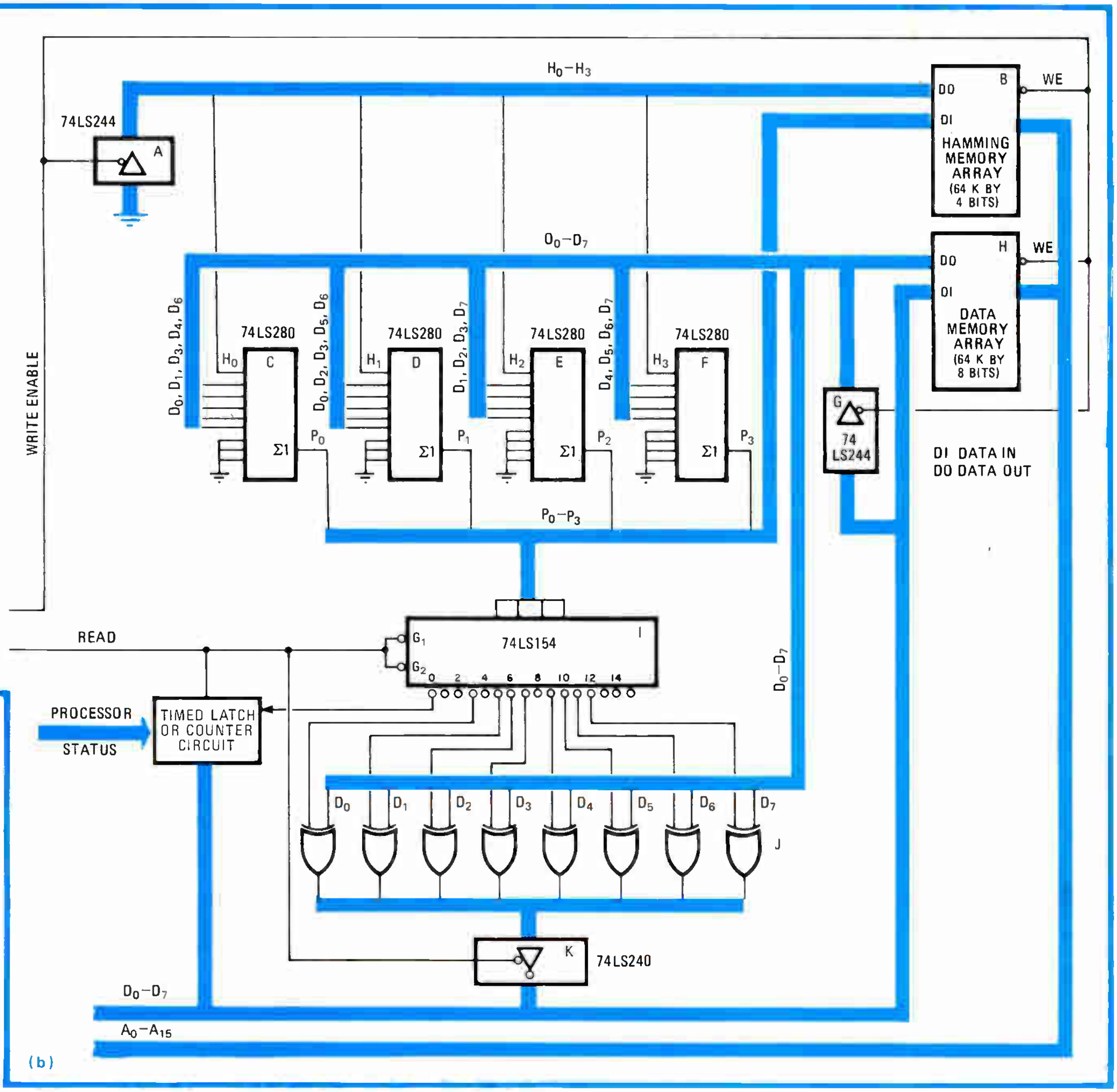
No longer an optional luxury, error-detection and -correction codes are becoming standard on most computer systems as hardware costs come down and system complexity goes up. Semiconductor memories particulary need the codes, being more prone to errors than the older magnetic-core designs.

But now increased chip densities makes the use of these codes even more critical. The denser memories are especially susceptible to single-bit errors induced by alpha particles hitting the semiconductor. As the semiconductor manufacturers discuss chip densities of 64 and 256 K, the computer makers are looking towards new schemes that go beyond the Hamming code to detect as many as 3 failing bits and correct up to 2-bit errors. **-Anthony Durniak**

Invoking software

A practical circuit for error detection and correction for an 8-bit processing system does several things. First, of course, the special Hamming circuits determine if there has been an error by generating the four equations. Latches immediately latch or trap the addresses of an incorrect word, the word itself, and the Hamming data. Finally, the processor is interrupted.

The block diagram of Fig. 1a gives an overall indication of the sequence of events. First, the circuit's address bus selects an 8-bit location in the central processing unit data block and a corresponding 5-bit location in the Hamming block. While 8 data bits are being written into the CPU memory block, the Hamming circuitry generates a 4-bit Hamming word and 1 overall parity bit and stores it in the Hamming memory blocks. Subsequently,



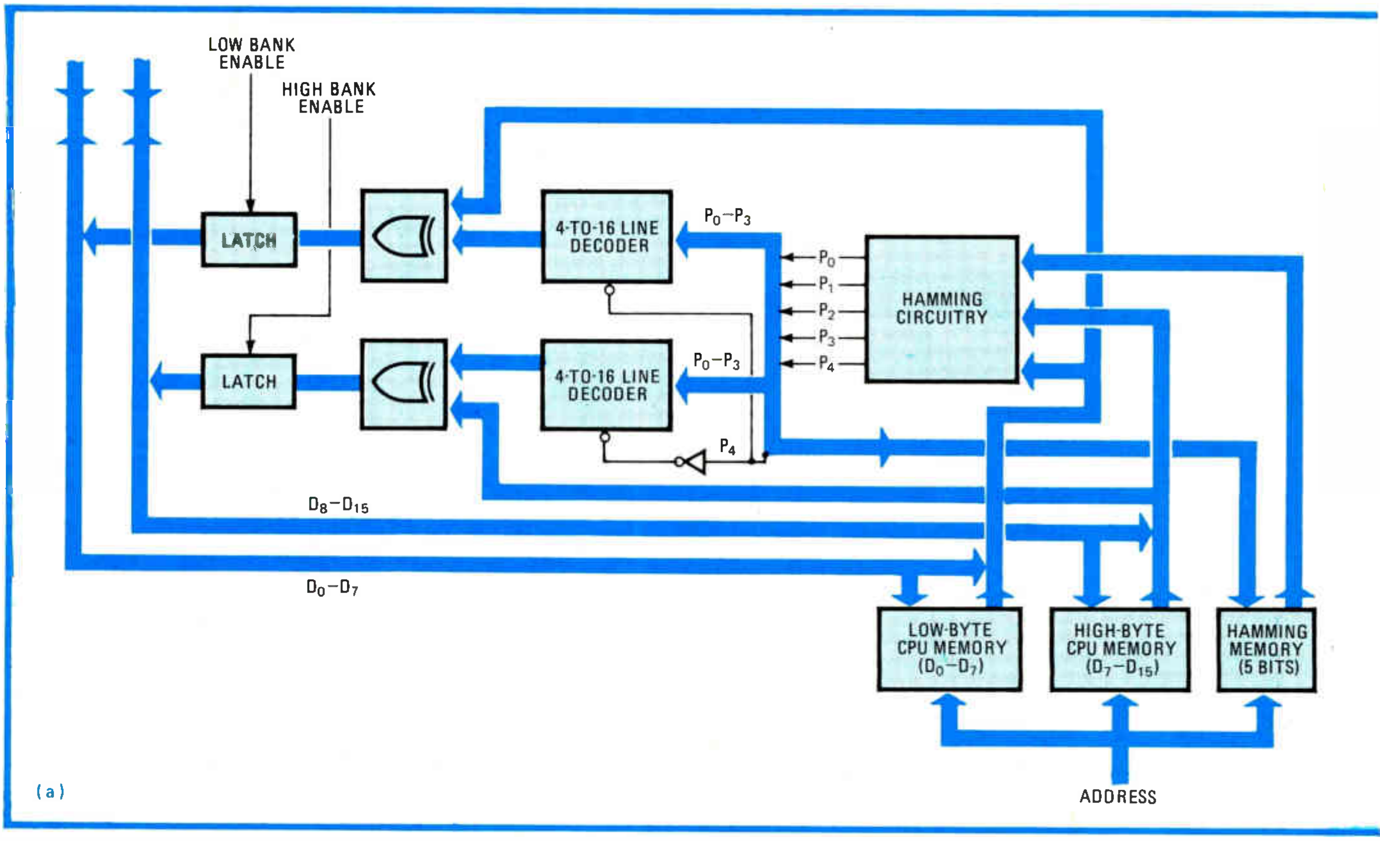
(b)

when the data bits are read from CPU memory, the Hamming circuitry compares them with the Hamming memory data. If there is an error, one or more of the output parity lines P_0–P_3 go high. This event causes the interrupt circuitry to store the current word's address, the CPU data, and the Hamming output data in their respective latches and to alert the CPU. The CPU then retrieves the data from the latches, corrects it, and rewrites it into memory.

Figure 1b gives the details of the circuit. More specifically, when data is being written into memory, the H_0–H_3 and H_p (overall parity) lines are disabled from memory by the three-state buffer M and grounded by the three-state buffer N, whereas the parity lines P_0–P_3 and P_p are enabled to memory by buffer P. Each of the parity chips G–J then sums the parity of the pertinent data with its respective Hamming bit set equal to 0. Note, however, that while chips K and 0 sum the total parity of D_0–D_7 and H_0–H_3, chips G–J solve the Hamming equations O_0–P_3. The P_p variable is the simple overall parity that is used to determine if there is a single or double error.

While data is being read from memory, the parity lines P_0–P_3 and P_p are disabled from memory, whereas the Hamming lines H_0–H_3 and H_p are disabled from ground and enabled to memory. Now the parity chips G–J each sum the parity of the appropriate data and Hamming bits for equations P_0–P_3. If there are no errors, the CPU data bits give an even parity, or 0, for P_0–P_3 when summed with the Hamming parity data. Chips K and O provide the overall simple parity.

But if there is an error, one or more of the parity outputs will go to 1 and there will be an output from gate Q. A timed interrupt circuit, or strobe, responds to this



3. Sixteen bits. Operation is similar to the 8-bit real-time circuit but all five complete parity equations must be solved. P_4 enables the lower decoder chip P for errors in data bits less than D_{11} and enables the upper decoder chip Q for errors in data bits D_{11} and above.

output by enabling the four latches B–E, so as to trap the address, data, and parity bits, and by sending an interrupt to the processor.

The processor thereupon instructs a software routine to read the data from the latches. These latches are each output-enabled in turn by the 4-to-16-line decoder chip A, which is addressed as an I/O port. The software then corrects the data and writes it back into memory (provided of course that there was only one error). Finally, the latch strobe from the timed interrupt circuit will be released by a strobe from the decoder chip A, and the interrupt circuit itself will be reset.

Points to remember

The details of the operation of the timed circuit vary with the timing signals from the particular processor being used. They also depend on the access time of the memory array and the propagation time through the parity chips. Time must also be allowed for the data to stabilize before the interrupt is enabled, for otherwise false interrupts will occur.

This hardware/software circuit has been verified in an ITT laboratory by a computer simulation but was not constructed because a real-time circuit was more appropriate for use in unattended systems. Instead, a real-time 8085-based single-board telecommunications control processor was built and successfully tested.

Real-time error correction for the 8-bit microprocessor is perhaps simpler to implement, since it uses hardware only. In this circuit, the memory array has separate data-in and data-out lines as in typical 16-K dynamic random-access memories. The same Hamming circuitry is used as in the previous circuit, but there are neither latches nor an overall parity check for double errors. Instead, a 4-to-16-line decoder and an exclusive-OR gate array perform the error-correction functions.

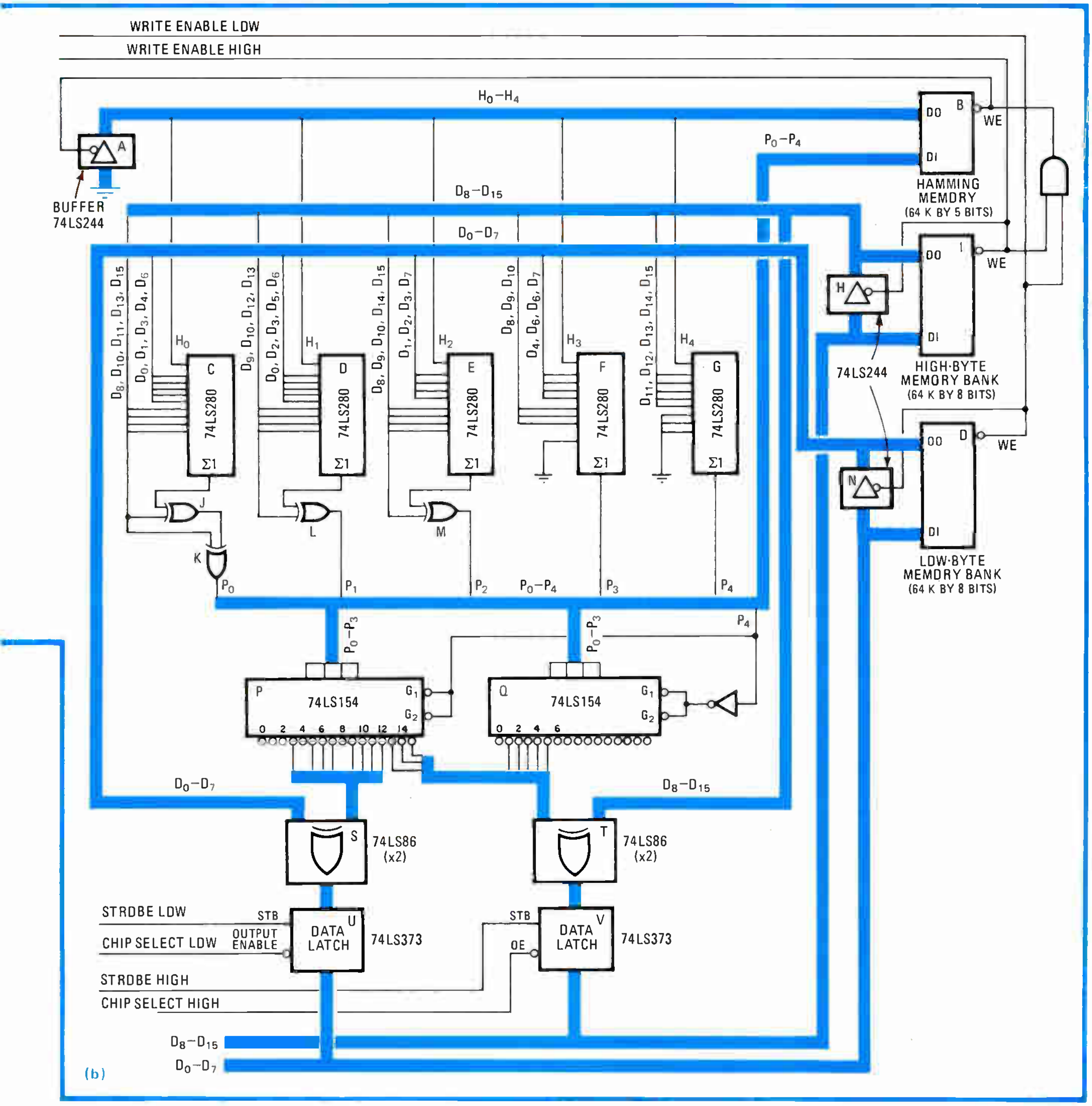
The circuit design assumes that each word will be either accessed at least once or scanned for errors in a period of time much shorter than the mean time between failures. This is the usual mode of operation.

If an error is encountered while the memory is being read, it is corrected before it can reach the processor bus and trip a latch or counter. This latch or counter can be periodically checked for errors. If an error has occurred, it is necessary to read each word in memory (thus correcting it) and then rewrite it.

Because of this frequent access, it is assumed that the probability of double errors, though finite, is negligible, so no overall parity is taken. Again, this is a reasonable assumption for practical systems.

Figure 2a outlines the operation of this circuit. As before, the address bus selects an 8-bit CPU data location and a corresponding 4-bit Hamming data location; the Hamming circuitry generates Hamming code from any 8-bit CPU data being written with memory and stores P_0–P_3 in the Hamming memory.

While data is being read from those locations, the Hamming circuitry compares data from the CPU memory and the Hamming memory. If there is an error, one or more of the lines P_0–P_3 go high, causing the latch (or counter) to trip for later reference, while the 4-to-16-line decoder's outputs are combined with the CPU memory



data via exclusive-OR gates to correct the erroneous bit. If there is no error, the data is unchanged.

The circuit's detailed operation may be understood from Fig. 2b. During writing, the Hamming lines H_0–H_3 are grounded by buffer chip A, and the data being written into memory is admitted to the parity chips C–F by the three-state buffer G. As with the combined hardware and software approach, this permits the parity of the data alone to be summed and stored in the Hamming memory via lines P_0–P_3. During a read operation, P_0–P_3 form a pointer word that points at a specific data bit by means of the 4-to-16-line decoder chip I.

The exclusive-OR array J combines each output line of the decoder chip with its respective set of data bits in accordance with the error positions of Table 1. Note that since the output of the decoder is active low, it is necessary to invert the result by using an inverting three-state buffer at chip K. Otherwise, a noninverting buffer would be used.

As in the hardware and software approach, time must be allowed for the data to be accessed and propagate through the circuitry. Otherwise, propagation skew would indicate errors falsely. For this circuit, the propagation time is about 150 nanoseconds.

In the telecommunications control processor in which this circuit was tested, the Hamming circuitry can be

Computing Hamming bits

It is simple to correct any error in a stream of binary data: the value of any bit known to be erroneous is simply inverted. But there's the rub. How can the transmitting device tell the receiving device which bits are wrong?

The Hamming code was the first of many techniques for manipulating data streams so as either to detect or to detect and correct errors. It depends on a clever interweaving of the data bit stream with another bit stream composed of Hamming (or check, or parity) bits. The values of the Hamming bits are determined by the values of the data bits and their positions are fixed in relation to the data bit positions according to equations developed by Richard Hamming. Since the receiver knows how the transmitter does this, it can infer the existence of a bit error from any discrepancy between the Hamming the and the data bits.

For instance, to ensure the detection and correction of any single-bit errors in a 4-bit data word, a transmitter would interleave the 4 data bits, D_1–D_4, with 3 Hamming bits, thus: H_0, H_1, D_0, H_2, D_1, D_2, D_3. It would derive the value of each Hamming bit from a different combination of 3 data bits, thus: H_0 from D_0, D_1, D_3, H_1 from D_0, D_2, D_3, and H_2 from D_1, D_2, D_3. The premise is that the sum of the 3 data bits plus the Hamming bit must always come out even; in other words, each Hamming bit provides even parity for its associated data group by being set at 1 when the sum of those 3 bits in base 2 arithmetic ends in 1 and at 0 when the sum ends in 0.

In this example, if the data bits are 0101, logic circuitry in the transmitter calculates the Hamming bit as 010, and the word 0100101 is transmitted. Then if some noise on the line changes the second data bit (D_1) from 1 to 0, the logic circuitry in the receiver gets 0100001, computes the pointer bits as 101, deduces D_1 is in error, and corrects it. Then it strips out the Hamming bits and passes the corrected 4-bit word, 0101, to the next part of the system for further processing.

Hamming set up similar structures for data streams of various lengths. Roughly speaking, the longer the data word, the lower the ratio of the Hamming to data bits, and the less the data-transmission efficiency is affected.

Moreover, his work pointed the way to even more powerful codes that could detect and correct multiple errors. However, many of those codes are not only complex to analyze, but require so many parity bits to be added to a data word that they drastically lower the effective data transmission rates. They are therefore used for special-purpose applications requiring a few or zero errors. For example, the Hagelbarger code will correct up to six consecutive errors, at the price of using as many check bits as data bits and thus creating 100% redundancy on the transmission line.

locked in or out of operation. This was done, by means of software-controlled latches, for maintenance and evaluation purposes.

In typical tests, data was written into memory with the Hamming circuitry active. Following this, the Hamming circuitry was locked out, single-bit errors were written in, and the Hamming circuitry reactivated. A check on the memory locations with the errors showed them to have been corrected.

Sixteen bits

The 16-bit real-time processor was designed for an 8086-based system but has not yet been fabricated. It is a more complicated version of the 8-bit real-time machine. To begin with, it has five Hamming equations to be solved instead of four. In addition, the processor's operation is more complex, since it can either access the word's upper and lower 8 bits (high and low bytes) separately or access the entire 16-bit word. In the case of a write operation to a single byte, the data in the other byte must be corrected, combined with the new CPU data, and new Hamming data generated.

Figure 3a is clearly an expansion of Fig. 2a. For a given memory location in this circuit, there is a low byte (D_0–D_7), a high byte (D_8–D_{15}), and a 5-bit Hamming word. The CPU may write data into both memory banks simultaneously with the Hamming circuitry functioning as in the 8-bit real-time machine. Alternatively, it may write to the high byte or low byte individually with the other corrected byte being first generated by the Hamming circuitry from all of the old data stored at that memory location. This corrected byte is stored in a latch and combined with the other byte from the CPU. The new Hamming data is derived from those combined data, and all three data groups are written into their respective locations.

When data is being read from memory, the Hamming data goes to the Hamming circuitry where any errors cause one or more of the lines P_0–P_4 to go high. The output from one of the 4-to-16-line decoders then combines with the data in the exclusive-OR gate to correct any single incorrect bit.

This arrangement permits writing to each bank separately. For example, suppose it is desired to write data into the high bank but not the low one. First, the memory is accessed, but an arbitrator circuit disables the write-enable signal, causing the data to be read into the latches U and V (Fig. 3b). The output of latch U is then enabled causing the low byte to be read from memory onto data lines D_0–D_7. However, the output of latch V is not enabled.

The write signal is then enabled so that the high byte from the processor is written to the high memory bank while the low byte from the latch is written to the low bank. At the same time, the lines H_0–H_4 are grounded by three-state buffer A, and both the high- and low-byte data are admitted to the parity chips C–G via buffers H and N. The parity outputs P_0–P_4 are then written into the Hamming bank.

One further detail must be remembered. Since the 74LS154 will point at only 16 bits, two of them are required for this circuit. P_4, when 0, selects the high-bank point chip P. P_0–P_3 then select the appropriate output line on the enabled chip.

As with the previously mentioned time-interrupt circuits, the specifics of the circuit used to arbitrate this sequence depend on the timing the user requires for a specific processor and memory. □

P^2C-MOS microcomputer family attains n-MOS performance

Double-polysilicon C-MOS process drops power consumption; CPU combines best attributes of 8085 and Z80

by George Simmons, Rich Burnley, Chuck Seaborg, and Keith Winter, *National Semiconductor Corp., Santa Clara, Calif.*

☐ If there were an ideal mid-range microcomputer, it would probably take the best features of current 8-bit n-channel MOS devices—high speed and density, a multiplexed address- and data-bus scheme, a sophisticated register structure, and an instruction set that is compatible with today's popular software—and implement them with a complementary-MOS process for the low power and high noise immunity that only C-MOS can offer.

The NSC800 microcomputer family comes the closest yet to that ideal. It provides designers of microprocessor systems with the advantages of low C-MOS power levels and the speed of existing n-MOS processors. It also combines the best features of Intel Corp.'s 8085—its multiplexed data and address bus—with those of Zilog Inc.'s Z80—its register structure and instruction set.

The family

The NSC800 family currently contains three members and a host of support circuits:

- The NSC800 central processing unit, which is capable of 1-microsecond instruction cycles yet dissipates only 5% of the power of comparable n-MOS CPUs.
- The NSC810 RAM-I/O-timer, which combines 128 bytes of random-access memory with 22 input/output lines and two counter-timers.
- The NSC830 ROM-I/O, a dedicated peripheral chip comprising 2-K bytes of mask-programmable read-only memory and 20 I/O lines.
- In addition to these components, National offers a full family of P^2C-MOS and standard C-MOS peripherals, including memories, auxiliary components, general and dedicated peripherals, and analog-interface devices.

This article is the fifth in a series on the new large-scale integration processes. The previous articles appeared in the Sept. 13 issue, pp. 109, 116, and 124, and in the Sept. 27 issue, p. 141.

The 40-pin CPU's multiplexed address/data bus structure is shared in the 810 and 830 dedicated memories, both of which incorporate on-chip logic to demultiplex the bus. The three devices make possible an efficient, highly integrated design system for low-end and mid-range applications that significantly reduces chip count, as well as power; and they do so without compromising performance, which remains equivalent to that of n-MOS systems.

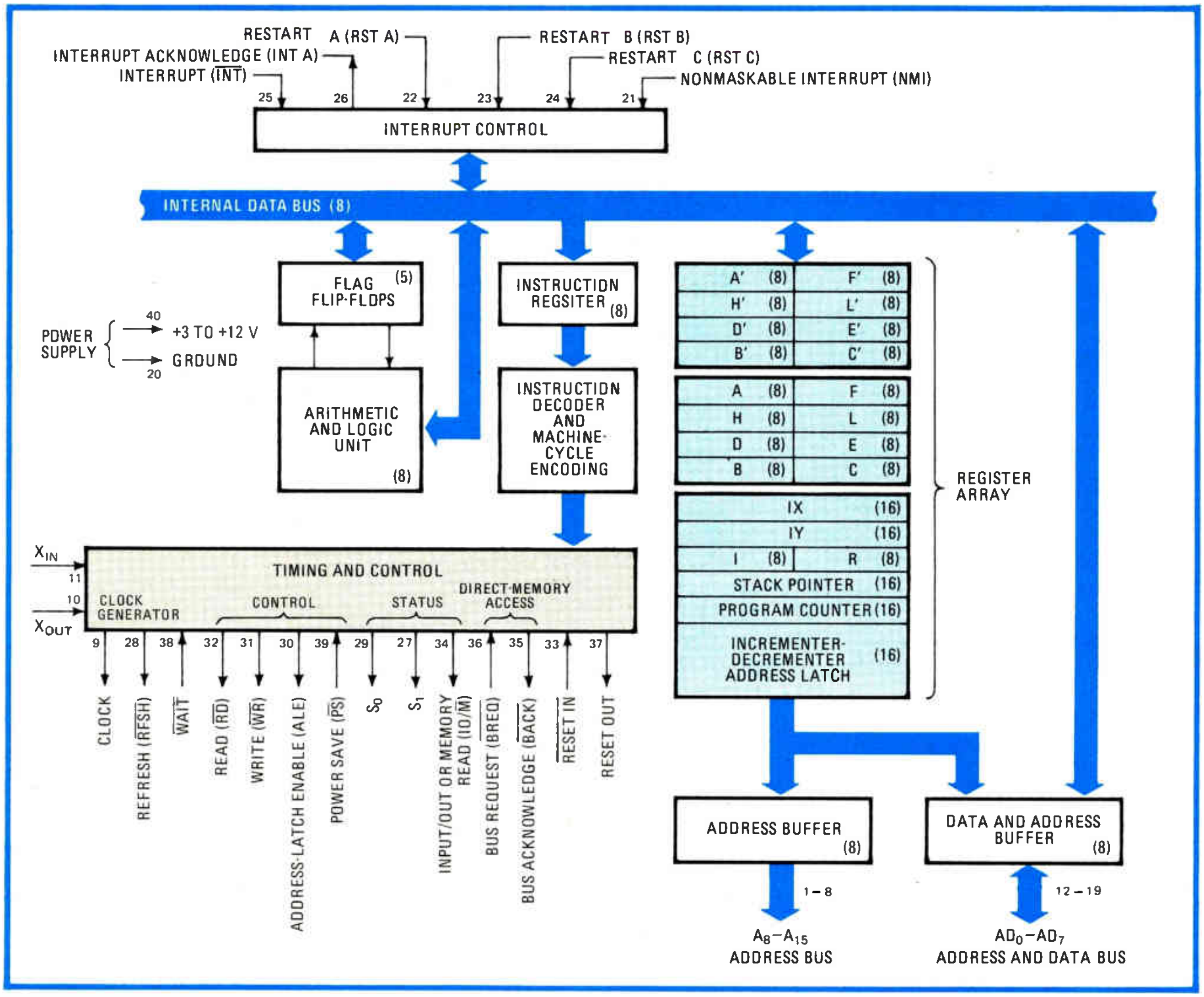
Battery backup

Systems that must be powered by batteries or that require battery backup are natural candidates for the NSC800 family. Also, the family excels in noisy electrical environments, since it offers broader operating-voltage range and signal-level tolerances than n-MOS devices. Finally, the NSC800 family can operate over an extended temperature range.

Because all devices in the family operate with a single

TABLE 1: GENERAL FEATURES OF THE NSC800 AND COMPETITORS

	8080	8085	Z80	6800	1800	NSC800
Technology	n-MOS	n-MOS	n-MOS	n-MOS	C-MOS	P^2CMOS
Power supply (V)	+12, +5, −5	+5	+5	+5	+3 to +12	+3 to +12
Cycle time (μs)	0.48/0.32	0.32/0.20	0.40/0.25	1.0/0.5	0.31/0.16	0.40/0.25
Instruction execution time (μs)	1.92/1.28	1.28/0.8	1.6/1.0	2.0/1.0	5/2.5	1.6/1.0
Bus structure (lines)	16 address, 8 data	8 address, 8 address or data	16 address, 8 data	16 address, 8 data	8 multiplexed address, 8 data	8 address, 8 address or data
Mil-spec components	yes	no	no	no	yes	yes
Memory refreshing	no	no	yes	no	no	yes



1. Hybrid. The NSC800 central processing unit combines the best features of the Intel 8085 and the Zilog Z80 CPUs. It borrows the multiplexed address/data bus scheme of the 8085, yet has the register structure and instruction set of the Z80.

TABLE 2: MEMORY ACCESS TIME FOR THE NSC800

Operation	Access time (ns)	
	At 2.5-MHz clock	At 4-MHz clock
Op code fetch	475	250
Op code fetch with wait state	875	500
Memory read	675	375
Input/output read or memory read with wait state	1,075	625

supply ranging from 3 to 12 volts, only an inexpensive, loosely regulated power source is needed. That means a lower cost per watt of supply. More noteworthy is the fact that compared with the power consumption of an n-MOS microprocessor system, the total power-supply costs for the NCS800 are dramatically reduced. Moreover, additional savings can be realized because the lower power consumption means less heat generated, and the greater component density thus possible reduces the package size. Further, lower heat dissipation and fewer parts lead to increased system reliability.

The NSC800 family members are fabricated with a new C-MOS process called P²C-MOS (see "Inside the NSC800," p. 113). The key feature of this process is that it allowed a C-MOS microprocessor family to match for the first time the density and speed of a state-of-the-art n-MOS one, while preserving the power and noise-immunity advantages of standard C-MOS. Although the process is new, the individual steps have been done before in one form or another. In fact, everything that has been learned about increasing density and improving performance with present n-MOS technology has been applied to P²C-MOS to enhance performance.

In the NSC800, P²C-MOS makes possible a standard execution time of 1.6 microseconds. A faster version of the CPU, the NSC800A, offers 1-μs execution as the norm. In a comparison of the general features 800 with those the n-MOS 8080, 8085, and 6800 microprocessors—as well as with the C-MOS 1800 microprocessor—the P²C-MOS CPU comes out on top (see Table 1).

Architecturally, the 800 CPU represents an excellent

Inside the NSC800

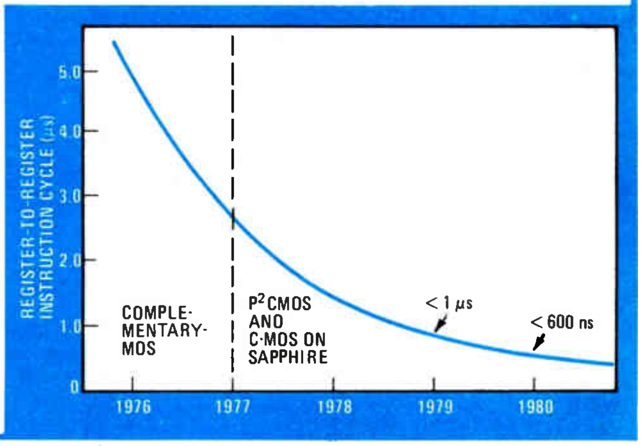
P^{2}C-MOS is a silicon-gate complementary-MOS process with two levels of polysilicon interconnection to give the NSC800 maximum density. The double polysilicon, in fact, enables P^{2}C-MOS to compare well in density with current standard (nonscaled) n-channel MOS processes. Moreover, P^{2}C-MOS uses fairly conservative geometries—5-micrometer lines and spaces—though the process is well suited to finer lithography. The 5-μm geometry was chosen to ensure that P^{2}C-MOS in its first iteration would be a producible process.

When applied to microprocessor architectures, P^{2}C-MOS results in significant performance improvements over standard C-MOS processes. As the chart below shows, a register-to register instruction for a C-MOS processor using 1977 techniques required 3 to 5 microseconds. With the development of new processes like C-MOS on sapphire and P^{2}C-MOS, greatly improved speeds in low-power microprocessors are possible. But there is an important distinction between the two: whereas the former is an expensive, revolutionary process development, the latter is an evolutionary extension of process techniques already tested and used in high-density n-MOS products.

The cross section of a typical P^{2}C-MOS structure is shown at the right. A ubiquitous-well (oxide-isolated) process with selective field oxidation is used. Field-surface doping extends the operating-voltage range without the need for the usual C-MOS guard rings; as a result, it affords improved layout density. A doped layer of polysilicon forms the self-aligned gates over a gate oxide less than 1,000 angstroms thick. A second layer of polysilicon interconnection improves design flexibility and layout density. Combining those features with carefully controlled source-drain diffusions and special metalization yields a C-MOS process comparable in density and performance with n-MOS.

The P^{2}C-MOS process employs state-of-the-art fabrication techniques, including ion implantation, dry plasma processing, and noncontact printing on 4-inch wafers using electron-beam–generated masks.

During the development of P^{2}C-MOS, considerable forethought was given to evolving a basic C-MOS process that can be readily scaled down in the future to provide improved device performance and circuit density. Of course, the process is reliable, since it evolved as an extension of widely used techniques.



compromise between the multiplexed bus approach of the 8085 and the nonmultiplexed, register-oriented structure of processors like the Z80. As shown in Fig. 1, it incorporates an 8-bit data and 16-bit address bus that can directly address 65,536 bytes of memory plus 256 locations in a separate memory space for I/O.

Architectural compromise

Within the CPU, an 8-bit bus provides communication among the register array, the arithmetic and logic unit, and the status registers, as well as between the data and address buffers and the instruction register. The processor's 22 registers, all of which can be used by the system designer, are divided into three main groups: the first and second groups each comprise eight 8-bit registers (A, B, C, D, E, H, L, and F, and their primes); the third group has two 16-bit index registers, one 16-bit stack-pointer register, and one 16-bit program-counter register. In addition, two 8-bit registers store an interrupt vector and the next refresh address for dynamic RAMs.

The processor's internal clock rate—2.5 megahertz for the 800 and 4 MHz for the 800A—is half the basic oscillator frequency. This buffered signal is available on a pin (CLK) for use as a clock for peripheral circuits; as such, it cannot be interrupted by the CPU.

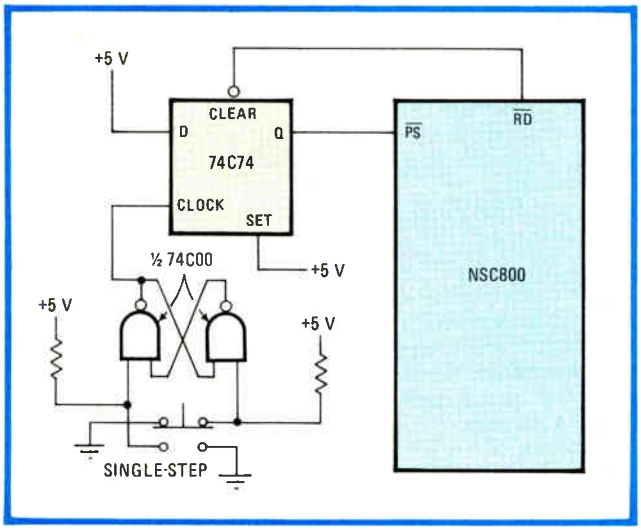
The NSC800 instruction set is completely compatible with that of the Z80 down to such details as the block-I/O and memory transfers; bit sets, resets, and tests; and indexed addressing. The 800, however, breaks down instruction cycles into several basic subcycles.

One basic subcycle is an operation-code fetch, which defines an M_1 machine cycle comprising four cycles of the clock output, or T states. Throughout an M_1 cycle, cycle-status outputs S_0 and S_1 indicate the fetch cycle. A memory-read machine cycle is a basic subcycle that comprises three T states. Here, the S_0 and S_1 outputs indicate a read status during the entire read cycle. The I/O-read and -write cycles are similar to the memory-read and -write cycles except that they extend an additional T state.

Easy operation

The NSC800 design eases interfacing with peripherals. For example, although it places certain timing requirements on ROMs, RAMs, and peripheral devices (see Table 2), a wait input supplied on chip can relax access-time specifications. Moreover, the user can add extra wait states. The wait input is sampled on the falling edge of the clock during the second T state of an M_1 cycle (the M_1T_2 state); if it is active low when sampled, an extra T state (T_W) is inserted to stretch all strobe signals. Thus, a widely varied mixture of fast and slow memories and peripherals can function within any NSC800-based system.

The NSC800 provides a unique low-power mode through its power-save ($\overline{PS}$) pin. The $\overline{PS}$ input is sampled at the last T state of the last M_1 cycle of an instruction. If a low level is detected on $\overline{PS}$, the CPU stops its internal



2. Power miser. The NSC800 has a power-save ($\overline{PS}$) pin that can shut off all circuits but the oscillator and system clock to allow timing functions to continue. Here, $\overline{PS}$ allows single-stepping of the CPU through instructions with a minimum of external hardware.

TABLE 3: COMPARING THE NSC800, 8085, AND Z80 PROCESSORS

	NSC800	8085	Z80
Power-supply requirements			
Voltage range (V)	3 to 12	5	5
Power consumption at 5V (mW)	50	850	750
Bus-drive capacity (100-pF TTL load)	1	1	1
Dynamic random-access memory refresh counter	8-bit	no	7-bit
Automatic wait state on I/O	yes	no	yes
Number of instruction types	158	80	158
Number of registers accessible to programmer	22	10	22
Block I/O and search	yes	no	yes
On-chip clock generator	yes	yes	no
Minimum instruction execution time (μs)	1	0.8	1
Number of on-chip vectored interrupts	5*	5	2*
Early read/write status	yes	yes	no

*INT interrupt has 3 modes

clocks, thereby reducing power dissipation, yet maintaining all register data and the internal control status. The only power consumed in the power-save mode is that required by the oscillator and the system clock.

The power-save input can also provide a single-instruction-cycle feature, useful in debugging programs, that requires a minimum of additional hardware. In the setup shown in Fig. 2, the CPU executes one entire instruction for each push of the button. When stopped, the CPU sends out the next instruction address.

Multiplexed bus

The NSC800's 16-bit address bus shares its lower 8 bits with the 8-bit data bus on lines AD_0–AD_7. The multiplexed bus holds several advantages over a nonmultiplexed one. For one, it frees pins on the CPU and peripheral packages for other purposes, like status outputs, direct-memory-access (DMA) control lines, and multiple interrupts, reducing system component count considerably. For another, since in most applications fewer bus lines are required to interconnect devices—16 lines, as against 24 for a nonmultiplexed configuration—it reduces circuit-board complexity.

The address-latch-enable (ALE) output strobe demultiplexes the bus information. The higher 8 bits (A_8–A_{15}) of the bus are not multiplexed and remain valid through the end of a read or write strobe. During an input or output cycle, address lines A_8–A_{15} duplicate the address appearing on lines AD_0–AD_7 and therefore can simplify chip-select logic.

Read ($\overline{RD}$) and write ($\overline{WR}$) control signals are generalized active-low strobes used in both the memory-address space and the I/O-address space. The $\overline{RD}$ strobe is used during op-code-fetch cycles, as well as during memory- or I/O-read cycles; it is suppressed during interrupt-acknowledge cycles. The $\overline{RD}$ strobe, which must not overlap onto the refresh time, is the narrowest during an op-code-fetch cycle, since dynamic RAM refreshing takes place during the second half of that cycle. During memory- or I/O-read cycles, there is no refreshing and the $\overline{RD}$ strobe is lengthened accordingly.

The $\overline{WR}$ strobe has a different width for memory-for I/O-address spaces, since the CPU automatically adds a wait state when accessing I/O-address space to accommodate slower peripheral devices. The I/O- or memory-select output (IO/$\overline{M}$), in conjuction with $\overline{RD}$ and $\overline{WR}$, fully decodes the selected operation and wait state.

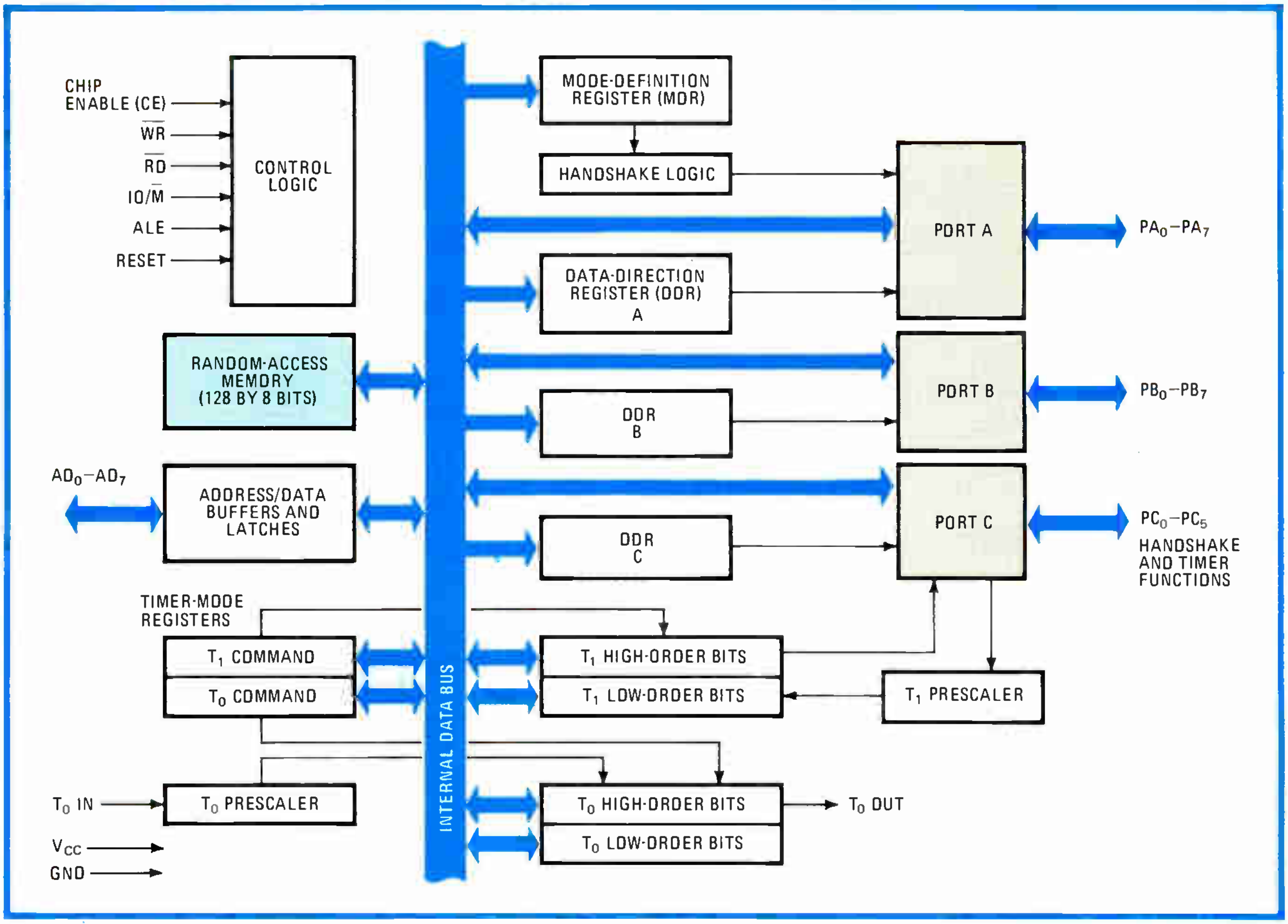
Built-in refreshing

The CPU refreshes memory during the third and fourth T states (T_3 and T_4) of every M_1 op-code-fetch cycle. During that time, the CPU is busy decoding the last op code fetched and cannot access the bus. The refresh output goes low to indicate a refresh operation. Table 3 indicates the major advantages of the 800 CPU over the 8085. In its bus structure, the 800 is similar to the 8085: both use a multiplexed data/address bus with nearly the same timing relationships. Unlike the 8085, however, the 800 guarantees that output data on AD_0–AD_7 is valid during both the leading and trailing edges of the $\overline{WR}$ strobe signal.

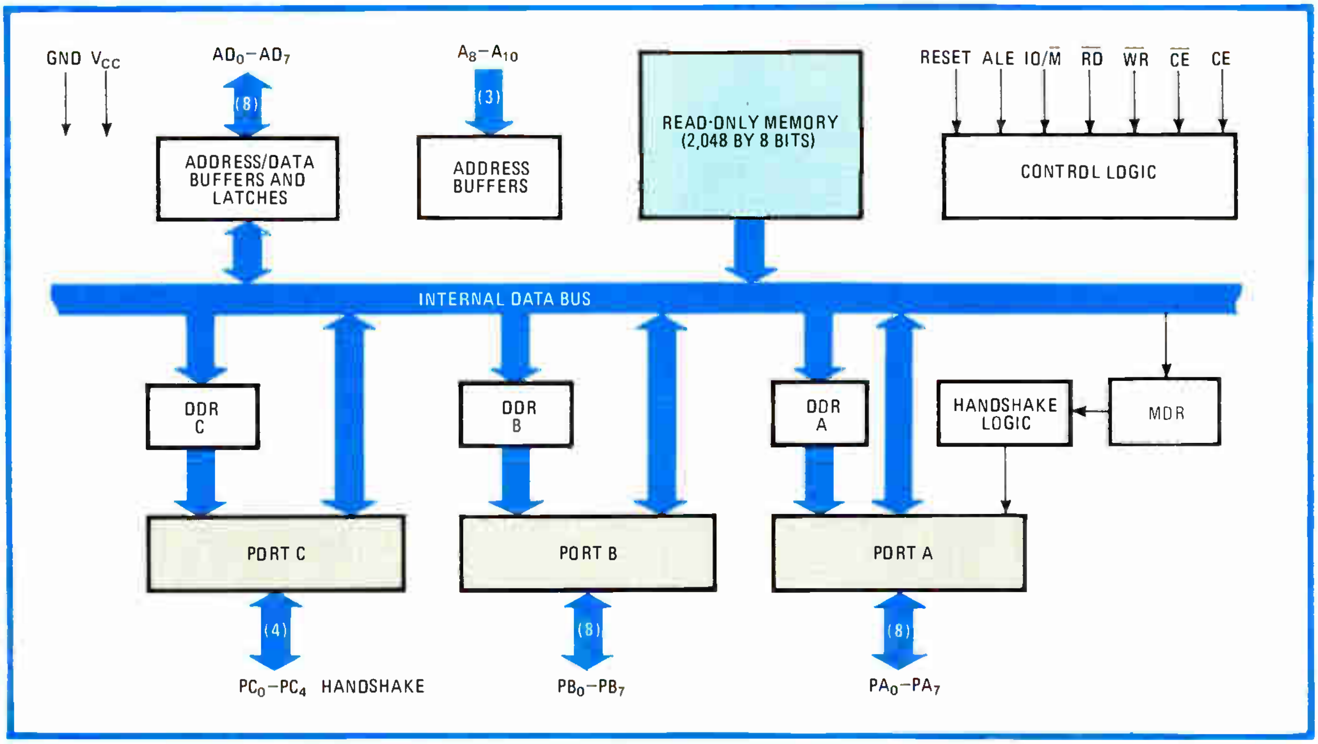
Status signals produced by the 800 are the same as those of the 8085: ALE, S_0, S_1, and IO/$\overline{M}$. In the 800, as in the 8085, the lower 8 address bits are guaranteed valid on the data bus at the trailing edge of the ALE signal. When all the components in a system are members of the NSC800 family, all of which contain on-chip demultiplexers, ALE simply connects to all the enable inputs. If other components are used, ALE should connect to the enable input of an internal 8-bit latch to demultiplex the bus information.

The machine-status lines of the NSC800 and the 8085 are similarly identical. Decoding status bits S_0 and S_1 in conjunction with the IO/$\overline{M}$ line will indicate the ensuing machine cycle.

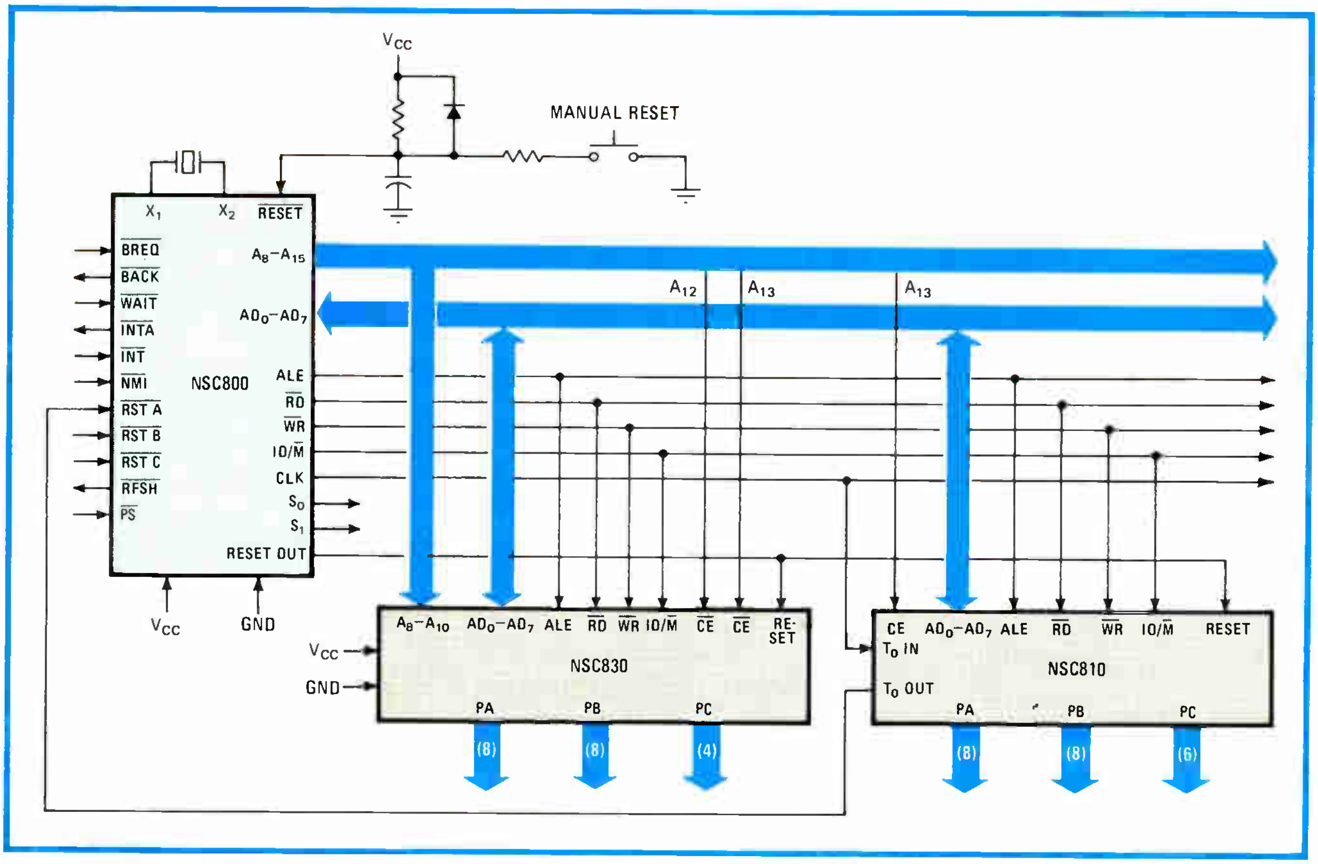
Direct-memory-access bus-request ($\overline{BREQ}$) and bus-acknowledge ($\overline{BACK}$) control signals on the 800 perform the same functions as $\overline{HOLD}$ and $\overline{HLDA}$ on the 8085. The 800 allows simple ORing of bus signals by these active-low DMA control lines. A low signal on the $\overline{BREQ}$ line, tested during the last T state of the current M cycle, initiates a DMA condition. The 800 then responds to a



3. RAM and more. The NSC810 supports the NSC800 with 128 bytes of random-access memory, two 16-bit counter-timers, and 22 input/output lines. Also built with P²C-MOS, the 810 has the same wide power-supply and operating-temperature ranges as the CPU.



4. Additional support. Providing 2,048 bytes of mask-programmable read-only memory, as well as 20 input/output lines, the NSC830 ROM-I/O peripheral chip supports the NSC800. The 830, like the 810 RAM-I/O-timer chip, has on-chip latches to demultiplex the bus.



5. Minimum system. Tying the NSC800 to the NSC810 and to the NSC830 builds a minimum microprocessor system that can serve low-end to mid-range applications. It offers the performance of an 8085- or Z80-based system while dissipating far less power.

low-going $\overline{\text{BACK}}$ signal by driving address, data, and control buses to the high-impedance state and by notifying the interrupting device that the system bus is available for use.

Differences

There is, however, a difference in the timing relations of the DMA bus-request and -acknowledge signals between the two processors. The 8085 responds with an HLDA signal half a T state after it recognizes HOLD, whereas the 800 responds with $\overline{\text{BACK}}$ a full T state after it recognizes $\overline{\text{BREQ}}$.

Another difference exists in the I/O cycles for peripherals: the 800 automatically inserts a wait state, which reduces the external hardware required for slow peripherals; the 8085 does not. When wait states are needed, the 8085 user must add hardware to do the job. When more than one wait state is required, they can be added to the I/O cycles in similar manners for both the 800 and the 8085: on the 800, that is accomplished by bringing the wait control signal low during T_2 of an I/O or memory cycle; on the 8085, it is controlled in the same way but using the ready line.

The NSC800 does not support the read-interrupt-mask (RIM) and set-interrupt-mask (SIM) instructions of the 8085, but it can emulate them with I/O instructions. The 800 substitutes two pins, a refresh (RFSH) output and a power-save ($\overline{\text{PS}}$) input, for the serial-output-data (SOD) and serial-input-data (SID) lines on the 8085. RFSH is a status signal that indicates the presence of an 8-bit refresh address on the address/data bus. The 800's internal refresh counter, which is incremented after each instruction cycle, is useful for dynamic RAM refreshing. The $\overline{\text{PS}}$ input, when activated, not only stops all internal clocks at the end of the current instruction, but also leaves all buses unchanged. Power consumption of other C-MOS parts in the system is thereby reduced, since C-MOS dissipates minimum power when the state remains unchanged. All internal registers and status conditions are maintained, and when $\overline{\text{PS}}$ subsequently goes high, the op-code-fetch cycle begins in normal fashion.

NSC800 vs Z80

Table 3 shows the major advantages of the 800 over the Z80. The 800 contains the same complement of internal registers as the Z80 and maintains instruction set and op-code compatibility. Machine-cycle timing for the standard-speed version of the 800 is comparable to that of the Z80; for the high-speed version, the 800A, it is comparable to that of the Z80A.

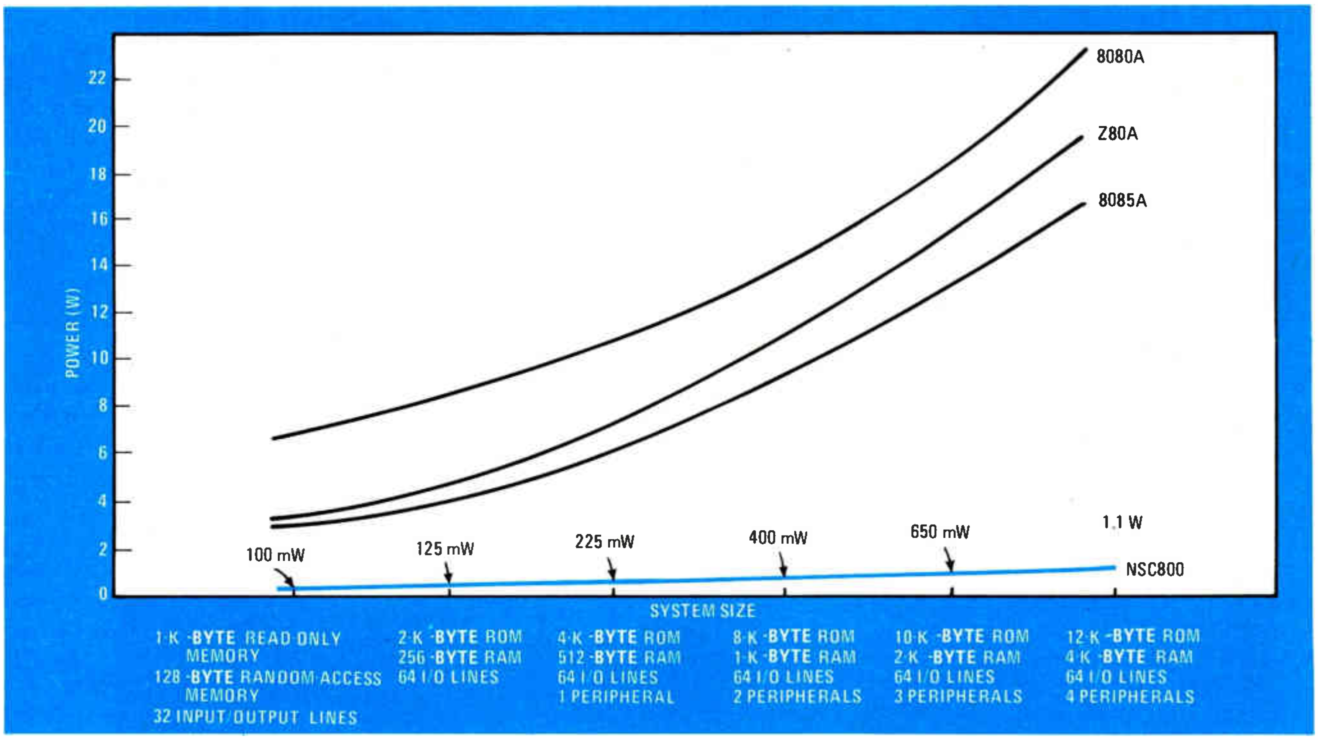
Although the software execution speeds of the 800 and Z80 are about equal, the 800 offers a number of architectural advantages over the Z80. In addition to the multiplexed data/address bus structure, these include:

- An 8-bit refresh counter on the 800, which allows refreshing of all 64-K dynamic RAMs and future devices using 256-cycle refreshing schemes; the Z80 has only a 7-bit counter. Except for that, the refresh timing of the 800 is functionally identical to that of the Z80.
- On-chip clock generation, which reduces system

TABLE 4: COMPARING MINIMUM SYSTEMS

Features	8080	8085	Z80	6800	1800	NSC800
Chip count	6	3	6	6	8	4
Power dissipation (W)	4	2.8	2.5	2.7	0.1 (at 5 V)	0.1 (at 5 V)
Memory address (bytes)	64 K	64 K	64 K	64 K	64 K	64 K
I/O address	256	256	256	0	7	256
Interrupt/restart inputs	1	5	2 (3 modes)	2	1	5 (3 modes)

NOTE: Minimum system defined as a central processing unit, 256 bytes of random-access memory, 2-K bytes of read-only memory, and 32 I/O lines



6. Compare power. The advantage in power dissipation of the NSC800 family over an n-MOS family increases with system size. For a typical medium-sized system an NSC800-based version dissipates almost one twentieth the power of an n-MOS one.

component count. In place of an external clock-generator chip, the 800 requires only a crystal or an RC circuit to produce the system clock.

- The availability on the 800 of three hardware interrupts not found on the Z80: restart A (RSTA), restart B (RSTB), and restart C (RSTC). These give the 800 five levels of vectored, prioritized interrupts without external logic. The general-purpose interrupt (INTR) and the nonmaskable interrupt (NMI) are identical to those in the Z80. INTR also has the same three modes of operation as it does in the Z80—modes 0, 1, and 2. Upon initialization, the 800 is in mode 0 to maintain compatibility with the 8080 code. Unlike the Z80, interrupt acknowledge ($\overline{INTA}$) on the 800 is provided on a dedicated output pin and need not be decoded externally.
- With the status outputs S_0, S_1, and IO/$\overline{M}$, early read/write information is available on the 800 that cannot be derived on the Z80.

Building a system

The NSC810 (Fig. 3) supports the 800 CPU. It includes 128 bytes of fully static RAM, two 16-bit binary counters or timers with prescaling, three programmable I/O ports (two 8-bit and one 6-bit), address and data buffers, and latches for interfacing with the multiplexed system bus. The NSC830 (Fig. 4) includes 2-K bytes of ROM and three programmable I/O ports.

A minimum three-chip system (Fig. 5) uses the 800, 810, and 830 and requires no external components. The system incorporates 2-K bytes of ROM, 128 bytes of RAM, two counter-timers, five interrupts, and 42 I/O lines, yet dissipates a maximum of only 100 milliwatts. A comparison for a more typical configuration—CPU, 256 bytes of RAM, 2-K bytes of ROM, and 32 I/O lines—is shown in Table 4 for the 8080, 8085, Z80, 6800, and NSC800 systems.

As illustrated in Fig. 6, low-end systems configured with NSC800 family components typically dissipate only 5% the power of n-MOS processors, with roughly comparable speed. At the high end—closely equivalent to an Intel type iSBC 80/20 microcomputer board, which has 12-K bytes of ROM, 4-K bytes of RAM, 64 I/O lines, and four peripherals—the difference is even more startling. Whereas the n-MOS devices dissipate anywhere from 15 to 20 watts, an NSC800-based system consumes a mere 1.1 W—again, with no sacrifice in performance. □

Designer's casebook

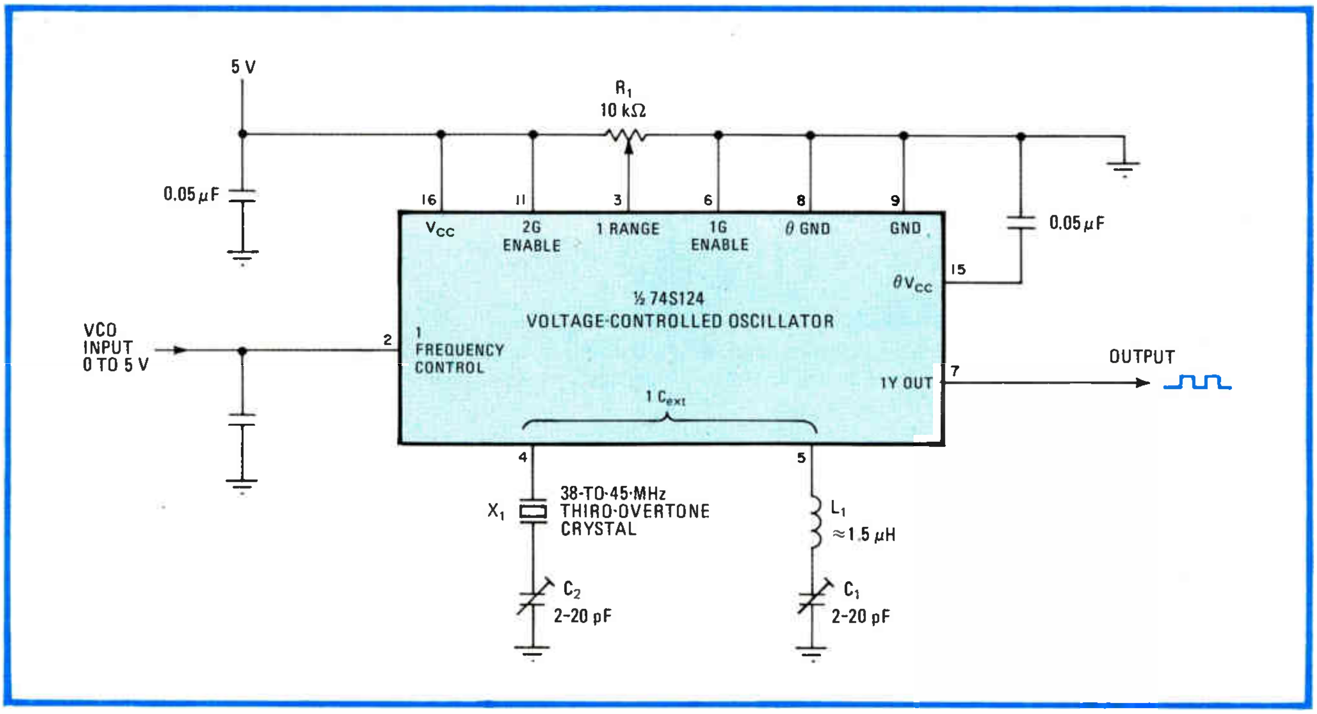
LC network adapts PLL for crystal-overtone operation

by R. J. Athey
National Research Council, Ottawa, Canada

Although Texas Instruments' popular 74S124 oscillator serves reliably in most instances as a crystal-controlled phase-locked loop, problems arise when overtone crystals are utilized for high-frequency (20 megahertz and above) operation. The difficulties may be overcome by adding an LC network in order to retain adequate system gain for oscillation at the required overtone and dampen oscillations at the fundamental frequency. This technique thereby forces the loop to lock onto the crystal's third-order output.

Although the range over which the PLL responds will be limited to about 1 kilohertz for a 0-to-5-V input signal, the method affords repeatable results and will enable use of the 74S124 beyond the normal limits imposed by fundamental-mode crystals. As shown in the figure, L_1 and C_1 are selected to be series-resonant at the desired overtone frequency. Assuming L_1 is 1.5 microhenries, a C_1 value of 2 to 20 picofarads will be adequate for tuning over the range of 38 to 45 MHz required in this particular application. The Q of both L_1 and C_1 should be reasonably high.

C_1, along with R_1, serves as a gross frequency control. Unfortunately, the setting of R_1C_1 will be rather critical. Although the range over which R_1 is effective as a tuning element for a given C_1 is narrow, a miniature carbon potentiometer will have sufficient resolution for making adjustments. C_2 provides an offset for the desired third-overtone frequency. In general, the circuit will work satisfactorily for crystals working to 60 MHz. □



Order of oscillation. Addition of L_1C_1 adapts TI's voltage-controlled oscillator for use as a high-frequency phase-locked loop utilizing an overtone crystal. LC network eliminates crystal's strong fundamental response, forces loop to lock onto slab's third-order output.

Tone detector sharpens digital filter's response

by Steve Newman
Los Angeles, Calif.

Using digital techniques to set the center frequency and the passband, this circuit will serve as a precision tone detector or as a control (transmission) gate for digital bandpass or band-blocking filters. The circuit elements can be easily cascaded to provide as great a degree of selectivity as required.

The general scheme is outlined in (a). Up counters A_1 and A_2 are preprogrammed to generate a carry signal after N or M input pulses of f_{in}, respectively, where N is equal to or less than 16 and N is greater than M. The period of the reference signal f_{ref}, which is t_{ref}, determines the time each counter is enabled.

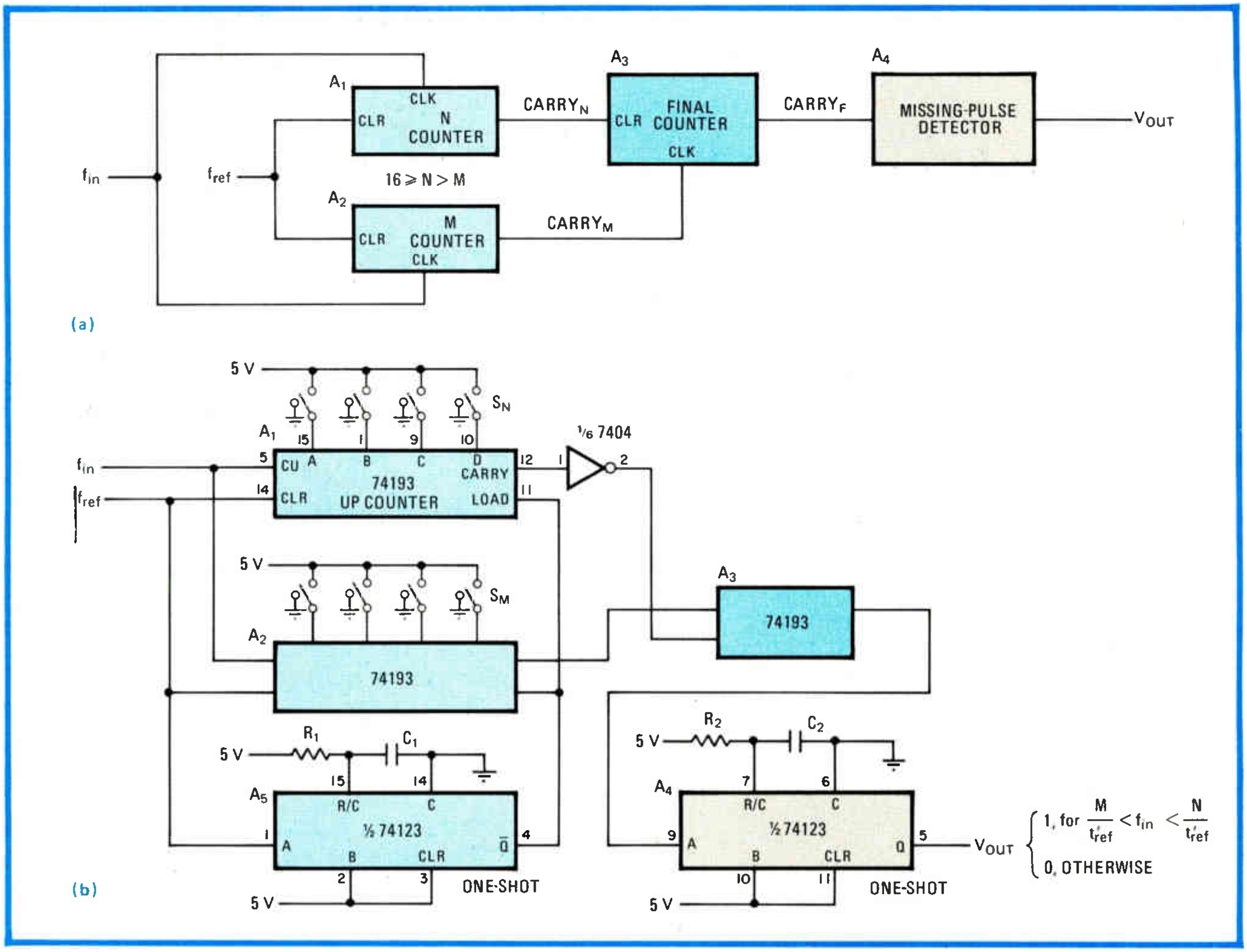
The output of the M counter clocks the presettable counter A_3, while the output of the N counter is connected to its clear input. Thus if M or more pulses occur during the time $\frac{1}{2}t_{ref}$, hereafter called t'_{ref}, the final counter generates carry pulses periodically (this circuit is intended to detect tones of fairly extended duration only). As a result, the output of the missing-pulse detector, A_4, can be forced high.

If, on the other hand, the incoming frequency is greater than N/t'_{ref}, presettable counter A_3 is always reset before it can produce a carry pulse. Thus A_4, which requires a steady stream of pulses to keep it active, is forced low. If f_{in} is less than M/t'_{ref}, A_3 again cannot produce a carry pulse because there are no clock pulses from the M counter. Thus, V_{out} will be high only for the case where $M/t'_{ref} < f_{in} < N/t'_{ref}$.

The actual circuit is shown in (b). A_1 and A_2 are enabled at the instant f_{ref} moves low. A_3 and A_4 assume the same functions described in (a). If the detection process must be sped up, A_3 can be preset so that it generates a carry for every Pth pulse from A_2, in the range 1 to 15. In general operation, however, A_3 is not preset.

At the start of the measurement cycle, f_{ref} initiates the process whereby one shot A_5 presets A_1 and A_2 to their switch-programmed values (switches S_N and S_M are active low). The reference frequency is selected in conjunction with S_M and S_N to provide almost any desired passband.

For example, if a frequency between 9.5 and 10.5 kilohertz (f_{in}) must be detected, M can be arbitrarily selected to be 9 and N = 10. A t'_{ref} = 0.95 millisecond is then required (f_{ref} = 526 hertz at 50% duty cycle). Note the time constant R_1C_1 must be much less than t_{ref}.



Logical boundaries. Tone detector sets limits of desired frequency range digitally. Using counting technique, circuit rejects tones whose frequencies are too high or low. Detector generates output only for $2M/t_{ref} < f_{in} < 2N/t_{ref}$, where f_{in} is input frequency, M and N are the Mth and Nth pulses that generate a carry from the M or N counters, respectively, and $t_{ref} = 1/f_{ref}$, where f_{ref} is the reference frequency.

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R_2C_2 must just exceed $240/f_{in}$ to cover the case where M = 15 and N = 16, whereupon as many as 240 input pulses are required to detect the tone. Under these conditions, however, the bandpass will be only 3% of the center frequency, f_o.

If greater selectivity is desired, a pair (or more) of 74193 up counters can be simply cascaded without upsetting the basic operation of the M and N counter chains. With two counters in each chain, the range of M and N can be expanded to 256, whereupon a bandpass of only 0.2% of f_o can be selected. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.

D-a converter simplifies hyperbolic clock

by R. H. Riordan
Cybec Electronics, Bentleigh, Australia

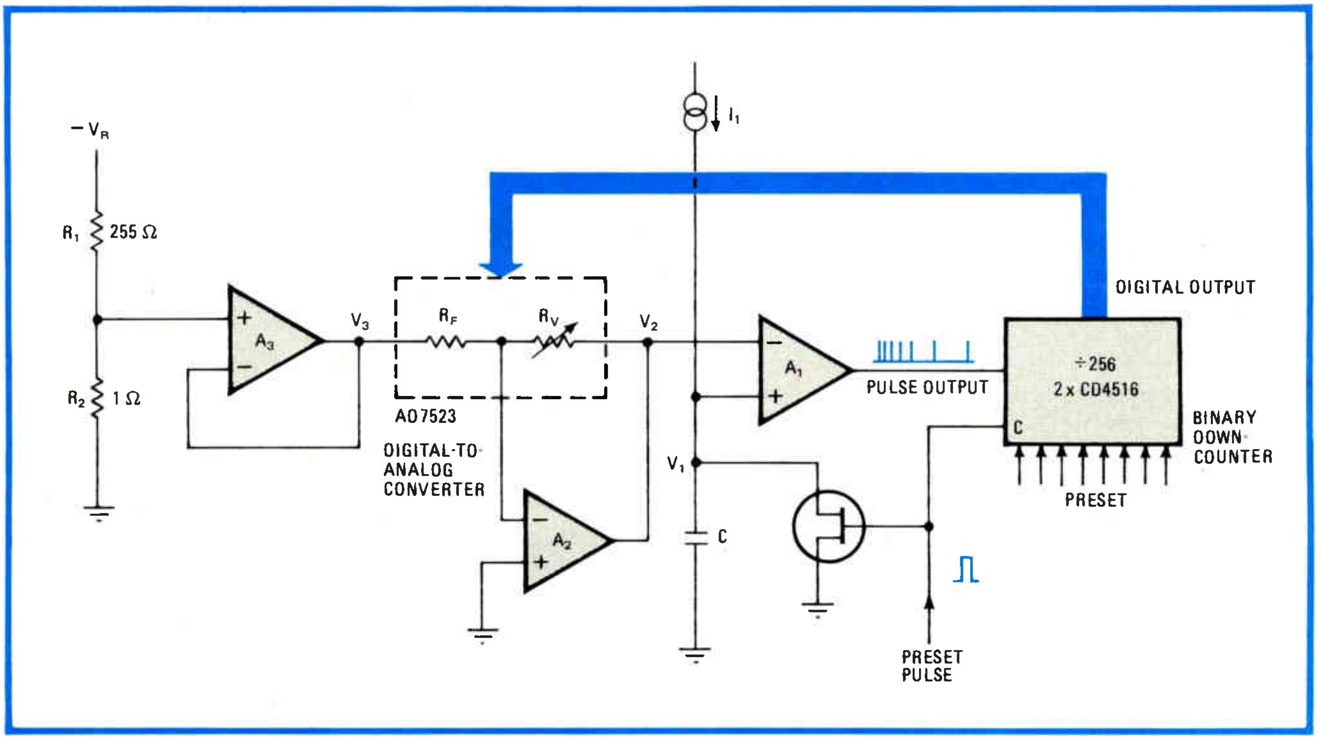
The hyperbolic clock circuit proposed by Baxter [*Electronics*, July 5, p. 132], which transforms a time function, t, into units of 1/t in order to measure rate, can be made more compact by employing a one-chip digital-to-analog converter. Using the converter's monolithic ladder of 255 equivalent resistors in place of Baxter's discrete network for scaling provides greater resolution for a circuit of a given size and is easily modified for applications requiring a decimal output.

Initially, voltage V_1 is set to zero and the 8-bit binary counter formed by cascading two C-MOS 4516 chips is preset to a count of 255. The converter is equivalent to a fixed resistor R_f and a variable resistor R_v, where $R_v/R_f = 256/N$ and N is the output count of the 4516. The converter is connected in the reverse of the normal configuration, so that $V_2/V_3 = -R_v/R_f = -V_3(256/N)$. But $V_3 = -V_{ref}/256$, so $V_2 = V_{ref}/N$.

At first, $V_1 = 0$ and $V_2 = V_{ref}/255$. At $t = 0^+$, current generator I_1 starts to charge capacitor C_1, and V_1 begins to rise linearly with time. Whenever V_1 climbs above V_2, comparator A_1 generates a clock pulse, decrementing the counter and causing V_2 to rise above V_1 again. For any given count N, a clock pulse will be generated at a time t when $V_1 = I_1t/C = V_{ref}/N$. Thus, until the counter reaches zero, the count at any instant will be proportional to the reciprocal of the elapsed time.

This circuit, as well as Baxter's, has a potential weakness in that if a single-step cycle does not result in V_2 rising above V_1, a lock-up condition will occur. This danger is eliminated if a separate clock signal is provided for the counter, with A_1 used only to enable the 4516s.

If decimal timing signals are required, it is a relatively simple matter to replace the d-a unit and the counter with their decimal-output equivalents. If a different step range is required, it can be selected accordingly by changing only R_1 and R_2. R_1 and R_2 are also used to set the desired count range. □



Turnabout. Clock inverts time function, t, in order to measure rate. D-a converter's ladder network, driven by counter, generates stepping function that is compared to ramp voltage V_1 at A_1. V_1's linear increase and V_2's monotonic rise are almost equal initially, but rates of rise diverge hyperbolically, so that counter is stepped at 1/t intervals. R_1 and R_2 set step size; I_1 sets scaling factor.

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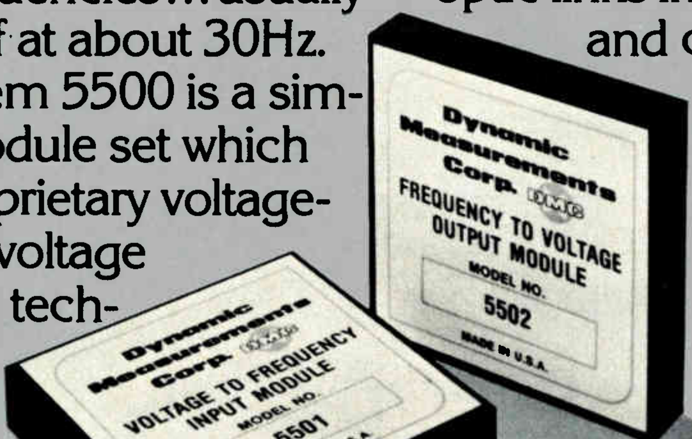

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Correcting errors digitally in data acquisition and control

Using a microprocessor in addition to analog techniques optimizes the compensation of gain and offset errors

by Paul Prazak and Andrij Mrozowski, *Burr-Brown Research Corp., Tucson, Ariz.*

☐ The accuracy of a data-acquisition or -control system can fall off rapidly as the ambient temperature varies and the circuit components age. An analog-to-digital converter, the heart of a data-acquisition system, may have 12-bit accuracy at room temperature yet be accurate only to 9 or even 8 bits over its entire operating temperature range.

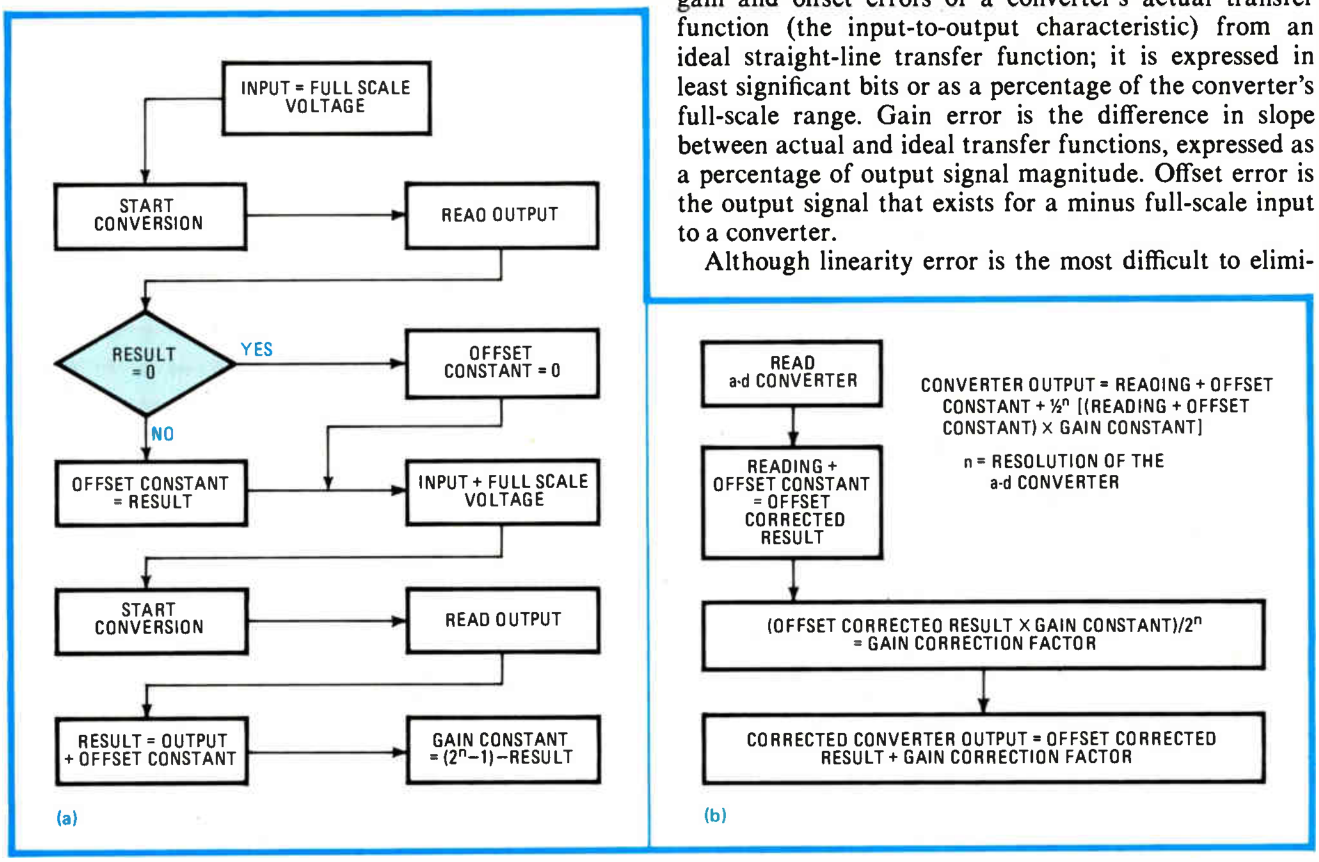
The analog-drift compensation techniques typically employed to counteract such errors at the 12-bit level and above have limitations, are costly, and require periodic recalibration. A more effective and less expensive drift-compensation method for data-acquisition systems is possible by combining a digital technique with an analog approach. All that is needed is a microcomputer or controller, a stable reference voltage, and two spare analog input channels. Furthermore, since all these elements can be found in many data-acquisition applications, the cost of implementing this digital and analog approach is quite low.

Breaking down the errors

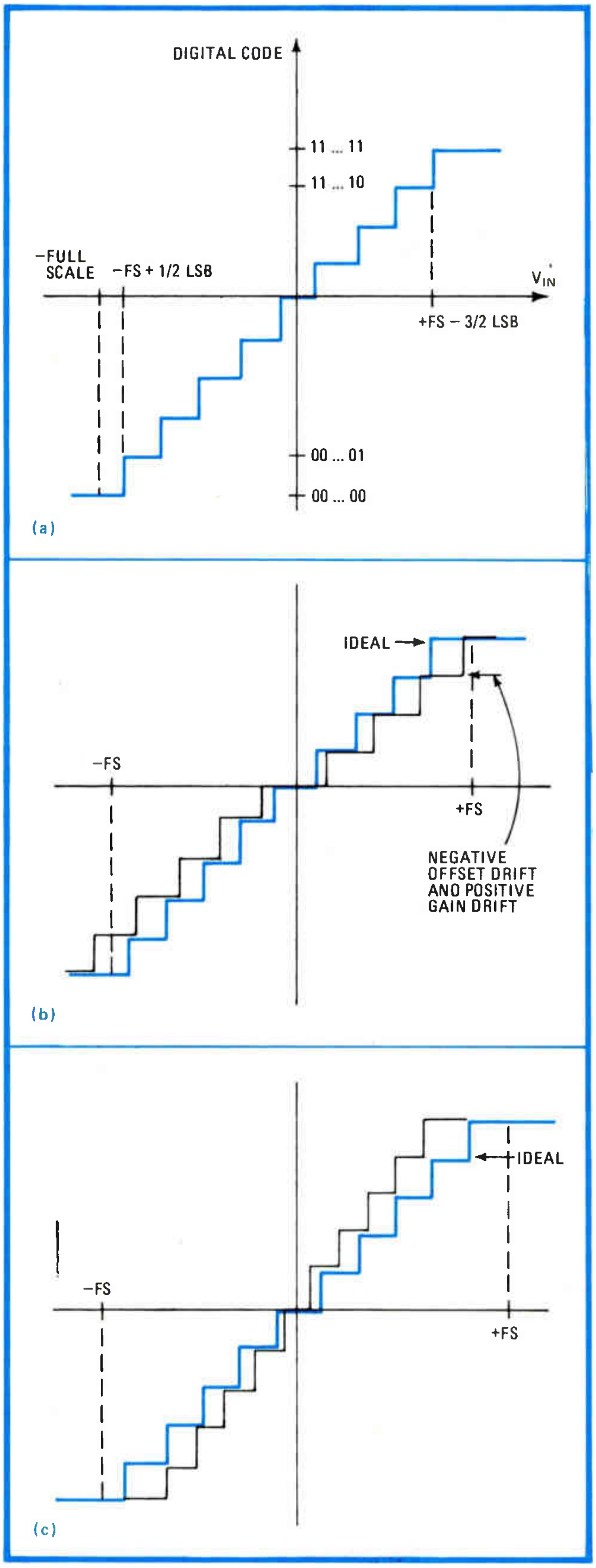
A better understanding of how digital drift compensation is accomplished is afforded by a closer examination of system errors, most of which result from the data-acquisition system's a-d converter.

A data-acquisition or -control system's total error derives primarily from errors in linearity, gain, and offset. Linearity error is the maximum deviation at zero gain and offset errors of a converter's actual transfer function (the input-to-output characteristic) from an ideal straight-line transfer function; it is expressed in least significant bits or as a percentage of the converter's full-scale range. Gain error is the difference in slope between actual and ideal transfer functions, expressed as a percentage of output signal magnitude. Offset error is the output signal that exists for a minus full-scale input to a converter.

Although linearity error is the most difficult to elimi-



1. Error algorithms. Gain and offset errors in a data-acquisition or -control system can be computed by the use of one algorithm (a) and removed by means of another (b). Error removal is accomplished in (b) by the use of the offset and gain constants computed in (a).



2. Transfer function. An ideal a-d converter transfer function (a) can be compromised by negative offset and positive gain drifts (b). Alternatively, the converter's ideal response can be compromised by positive offset and negative gain drifts (c).

nate by external adjustment, it is the easiest to control during a converter's manufacture. It is a function of how closely the base-emitter voltages (V_{BE}) and current gains (betas) of a converter's transistors as well as its ladder resistors are matched to track each other. Linearity errors of under ±0.01% (±½ LSB for a 12-bit a-d converter) are possible over a wide temperature range.

Gain and offset errors, on the other hand, not only depend on the closeness of converter transistor and resistor ladder matching and tracking, but also on the absolute accuracy of the reference voltage, the comparator's offset voltage, and the offset voltages of the operational amplifiers used. It is simple enough to null out such errors initially by external potentiometers. It is quite another matter to prevent such errors from occurring as the temperature changes.

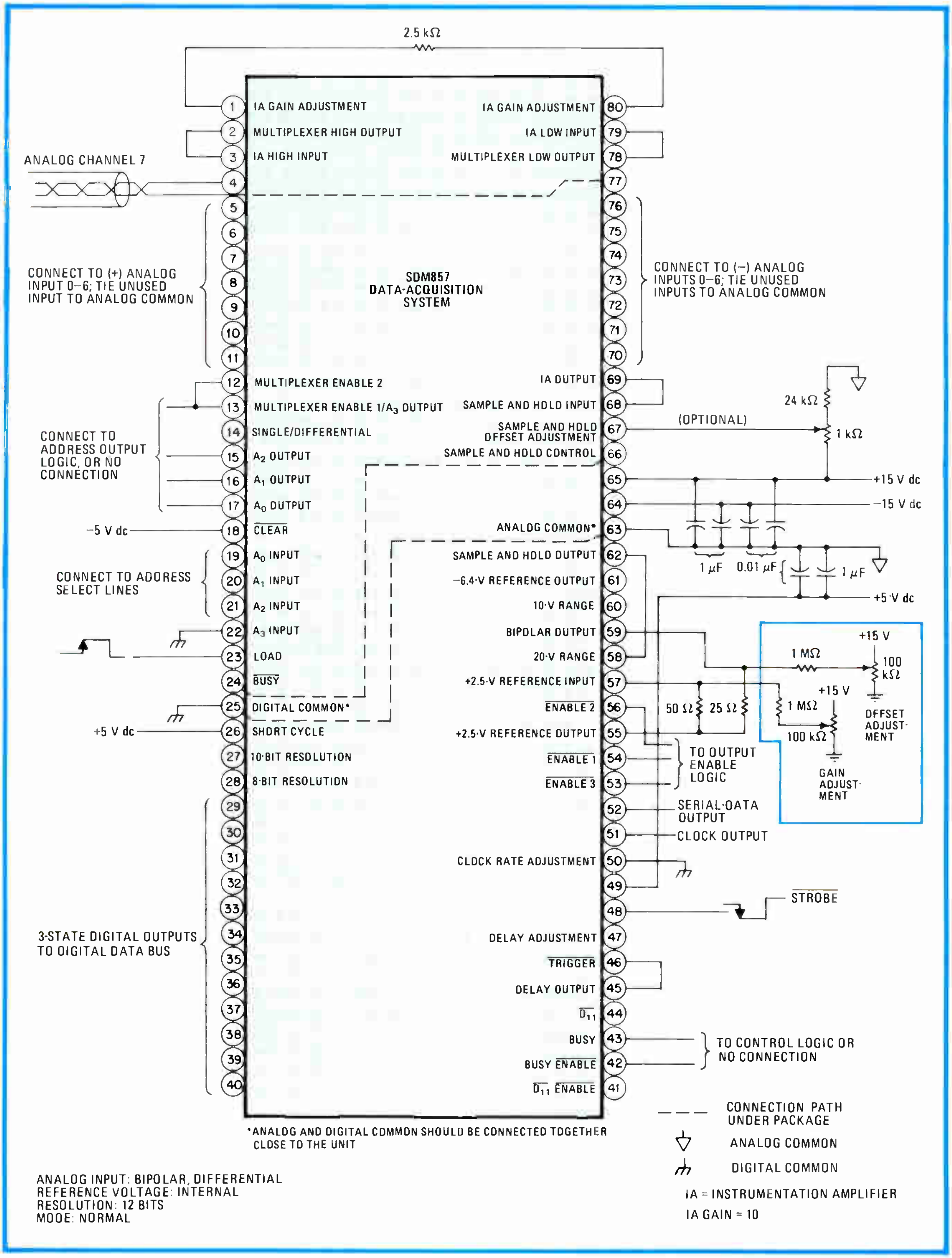
To illustrate, most commercially available 12-bit data-acquisition systems have specified gain and offset temperature coefficients ranging from 20 to 50 parts per million per °C (gain and offset tempcos are the changes in gain and offset with temperature changes). This means that a 12-bit system can exhibit an error of as much as ±0.1% over only a 20°C range and thus be only 9 bits accurate. When a typical operating range of 0° to 70°C is considered, even worse errors are possible.

In the commonest method of compensating for such errors, the converter is subjected to a known temperature change, its gain and offset drift calculated, and this drift canceled by adding a component to the converter with an equal but opposite temperature coefficient—for example, a silicon diode, which has well-defined drift characteristics. This technique, for all its usefulness, has several drawbacks. For each data-acquisition system to be compensated, the temperature coefficient must be determined individually. The temperature coefficient is also assumed to be linear over the full temperature range, whereas in fact it is generally linear only to within a few ppm/°C over a 0° to +70°C range and is almost never totally specified by a converter manufacturer. Finally, the effect of component aging on gain and offset errors is ignored.

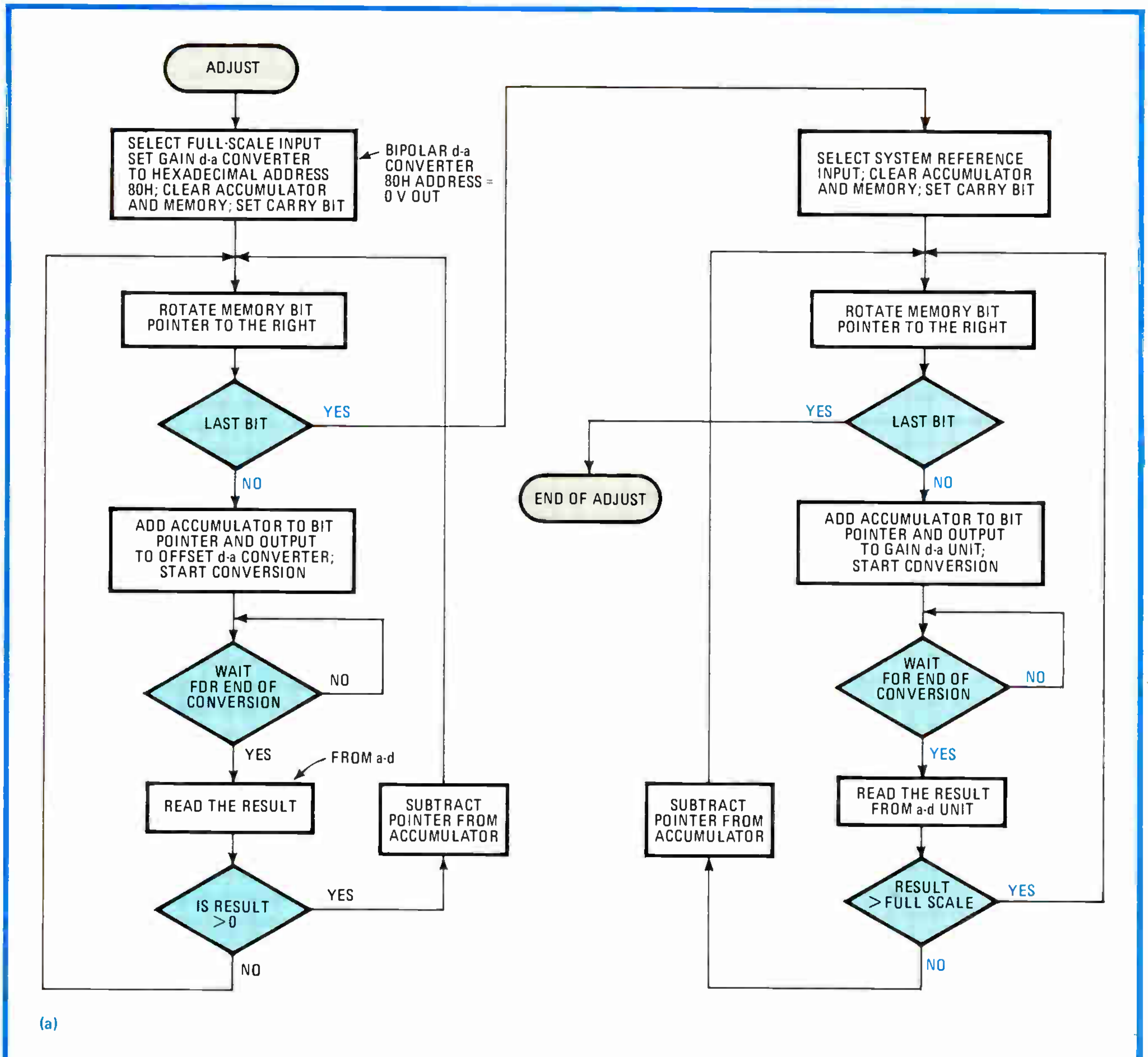
Automatic compensation with a microcomputer

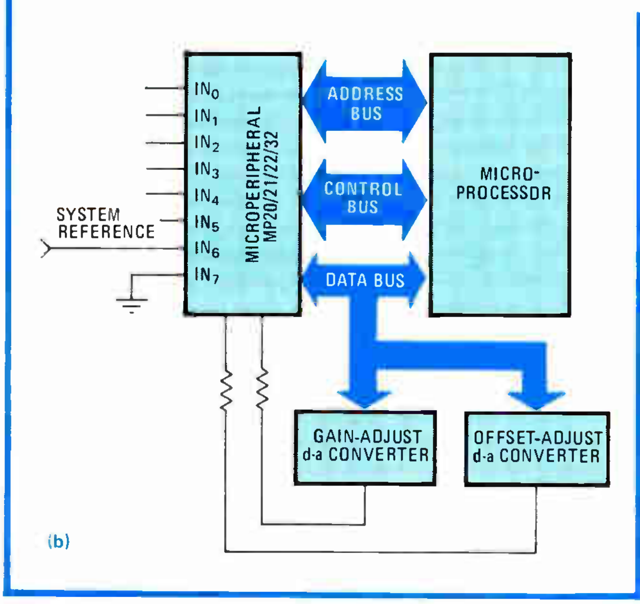
A purely digital compensation technique is not perfect, either. Admittedly, it is simple. The ideal output is known in digital terms and from it data-acquisition system gain and offset errors can be computed. These errors can be stored in memory according to the algorithm of Fig. 1a. They are derived by taking two spare analog-input channels of the data-acquisition system and connecting one to the system reference voltage and the other either to analog common (for a unipolar system) or to a minus full-scale voltage derived from the system reference voltage (for a bipolar system). With the use of a microprocessor, and with the relatively simple algorithm of Fig. 1b, gain and offset errors can then be removed from each of the system's digital output codes. The gain and offset factors can be updated as often as necessary to account for parameter variations due to time and temperature. Although this approach is straightforward, its exclusive use has some limitations.

Consider the ideal a-d converter transfer function



3. Adjustments. Gain and offset errors can be adjusted out of a data-acquisition system (such as the Burr-Brown model SDM857) with the external circuitry shown. Similar external-adjustment circuitry can be used for other data-acquisition systems.





4. Digital potentiometers. Low-cost 8-bit d-a converters can be used to remove gain and offset errors in a data-acquisition system (b) with the use of the algorithm in (a). Converter resolution and reference stability are the limiting factors in this situation.

shown in Fig. 2a. Note that for each digital output code there is a 1-LSB uncertainty as to the actual value of the analog input voltage. This is the inherent quantization error of an a-d converter. Only the analog input voltages that cause a transition from one digital output code to the next are unique. In an ideal a-d converter, the transition from a condition where all output bits are in an off state to one in which only the LSB is on should occur with an analog input voltage of minus full-scale value plus ½ LSB. Any deviation in this transition voltage is an offset error. A minus full-scale analog input voltage (or a voltage near the minus full-scale value) produces an output digital code with at most a ½-LSB uncertainty. The same analysis can be applied to the plus full-scale transition voltage. Since these quantization errors are not additive, the worst-case uncertainty in gain and offset errors at any input voltage is a matter of only ±½ LSB. However, the aforementioned digital compensation technique cannot correct this error, which is equivalent to the error caused by a 12-bit data-acquisition system that drifts ±2.7 ppm/°C over a 0° to +70°C temperature range.

Another limitation occurs when the input reference voltages are too close to the minus or plus full-scale voltage values. Figure 2b shows the effect of a negative offset drift and a postitive gain drift on the a-d transfer function. This type of error can be corrected if minus and plus full-scale values are used as reference voltages. If, however, the offset drift is positive and the gain drift is negative, as shown in Fig. 2c, the algorithm of Fig. 1a will not detect an error. This is because the digital output codes obtained for a minus or plus full-scale input voltage will always be correct. This limitation can be avoided, however, by the selection of reference voltages that are several LSBs greater than the minus full-scale voltage (and also, of course, several LSBs less than the plus full-scale voltage).

Still another limitation of the digital technique is that it cannot be used to remove the gain and offset errors from d-a converters or complete analog-output systems.

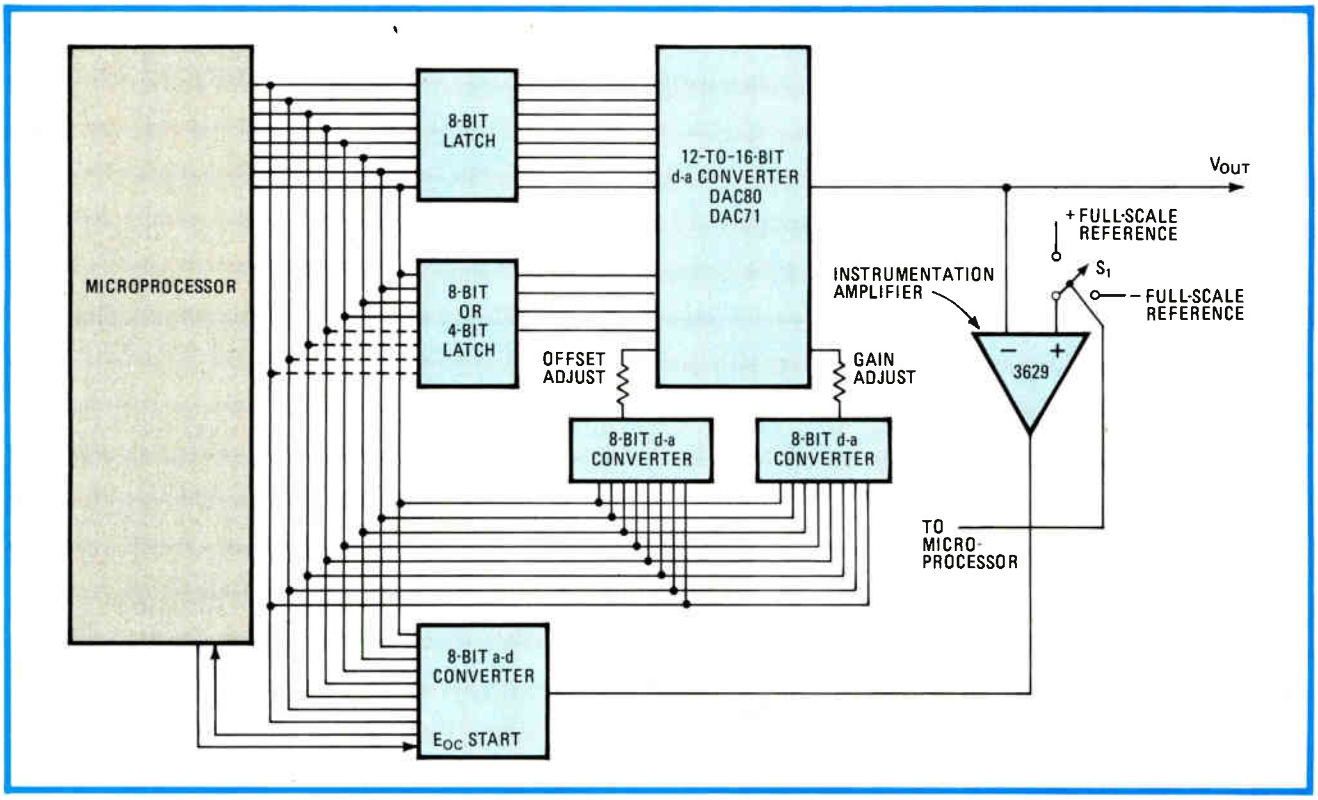
Combining digital and analog methods.

A combination of analog and digital techniques provides the optimum method of removing gain and offset errors in data-acquisition systems. Figure 3 shows the gain and offset adjustment circuitry recommended for a Burr-Brown SDM856/857 hybrid data-acquisition system. Similar external-adjustment circuitry is recommended for most commercially available data converters. The standard adjustment procedure for an a-d converter or any analog-input system is as follows:

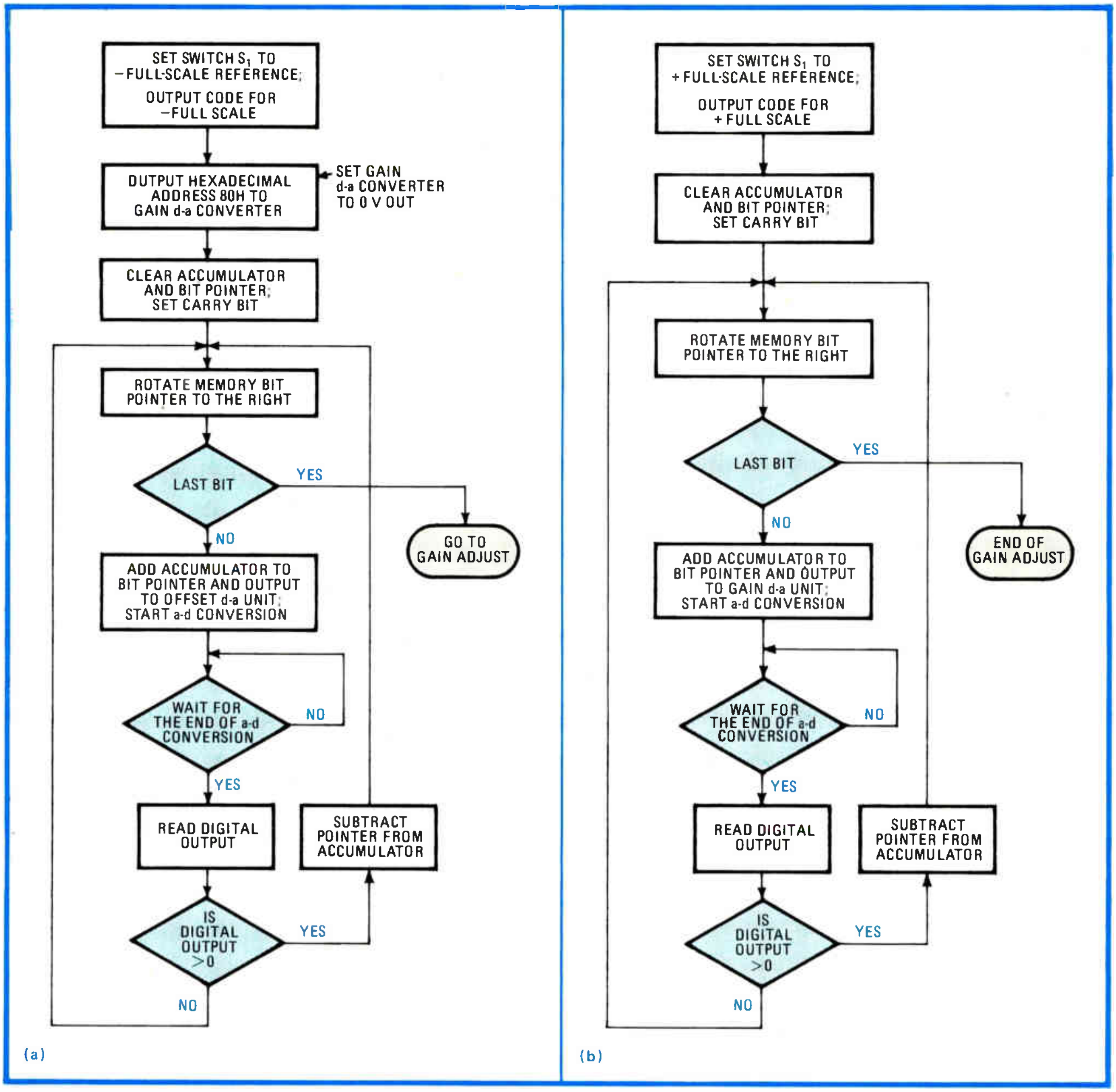
- Apply an input voltage whose magnitude is minus full scale plus ½ LSB.
- Adjust the offset potentiometer until the digital output varies between the condition where all output bits are off and only the LSB is on while continuously converting.
- Apply an input voltage of plus full scale minus ³⁄₂ LSB.
- Adjust the gain potentiometer until the digital output varies between the condition when all bits are on and only the LSB is off. Voltages above or below plus or minus full scale can be employed with only a small degree of interaction between the gain adjustment and the offset adjustment.

The replacement of the analog potentiometers with digital ones (also known as d-a converters), as shown in Fig. 4b, and the connection of two of the analog input channels to minus the full-scale voltage plus ½ LSB and plus the full-scale value minus ³⁄₂ LSB, respectively, produces very precise gain and offset correction when the algorithm shown in Fig. 4a is used.

The accuracy of this technique is limited only by the resolution of the adjustment d-a converters and the stability of the reference voltages. If the data-acquisition system has a maximum gain and offset error of ±0.4% (including the effects of initial error, temperature, and time), then the adjustment resolution obtained with an 8-bit d-a converter will be ±0.4%/128 = ±0.003%, which is about ±1⁄10 LSB for a 12-bit system. This technique can be easily expanded to equipment that



5. Multiple DASs. Gain and offset errors in a d-a converter or an analog-output system can be adjusted digitally. The analog output is amplified, then converted into a digital signal for proper error determination. A microprocessor can be used for multiple systems.



6. Error algorithms. Analog-output system gain and offset error removal can be accomplished by algorithms (a) for a single output system and (b) for multiple systems. Inexpensive microperipherals are available to implement this algorithm.

happens to contain more than one analog-input system.

Adjusting gain and offset errors for a d-a converter or an analog-output system requires more hardware when done digitally than when done by analog means. This is because the analog output signal must be converted into digital form to determine if any error is present. A circuit for accomplishing this task is shown in Fig. 5. A low-cost instrumentation amplifier is used to amplify the difference between the actual analog output signal and the plus or minus full-scale reference signals, respectively. This error signal is then converted into digital form with a low-cost 8-bit a-d converter. If the d-a converter has a maximum gain and offset error of ±0.4% (including the effects of initial error, temperature, and time), then the instrumentation amplifier gain should be equal to 128 to give a maximum output signal of ±10 volts. The 8-bit a-d converter then provides a resolution of about ±0.0003%, or about ±1/10 LSB, for a 12-bit d-a converter. The algorithms for performing offset and gain corrections for an analog output system are shown in Fig. 6a.

This technique can also be easily expanded to systems with multiple analog outputs, as shown in Fig. 6b. In this case, it is very economical to use the Burr-Brown MP20 or MP21 analog-input microperipherals to perform the a-d conversion. Each of these systems contains an 8-channel differential (or 16-channel single-ended) multiplexer, an instrumentation amplifier, an 8-bit a-d converter, an address decoder, and all the necessary logic to interface to most microprocessors. □

Weather forecast outlook for your investments in

Bavaria: bright and sunny

General climatic conditions
In every respect Bavaria offers an ideal climate for business initiatives. The political and economic stability which this West German state has enjoyed for many decades helps to safeguard your capital investments. The profound confidence placed in Bavaria's economic and political development is reflected in the high level of foreign investments: DM 3.7 billion since 1962.

No dark clouds over the labor market
Bavaria's well-trained workers are good partners who will give you a square deal. They are known for their reliability and loyalty to the firms in which they work. Statistics show that strikes are few and far between. The large number of qualified young people coming to work in Bavaria shows that the state is a magnet for highly skilled personnel.

Infrastructure helps to generate a favorable investment climate
Bavaria's infrastructure meets the exacting requirements of a modern industrial state. (Note that the Federal Republic of Germany has the most extensive network of autobahns or superhighways in Europe.) The international airports in Munich and Nuremberg and many strategically located airfields throughout the state link Bavaria to Europe and the world. The sources of available energy range from natural gas to nuclear power. Industrial sites with utility connections are laid out in all parts of the state.

Bavaria's economy basking in bright sunshine
Take advantage of Bavaria's dynamic economic growth. For example,
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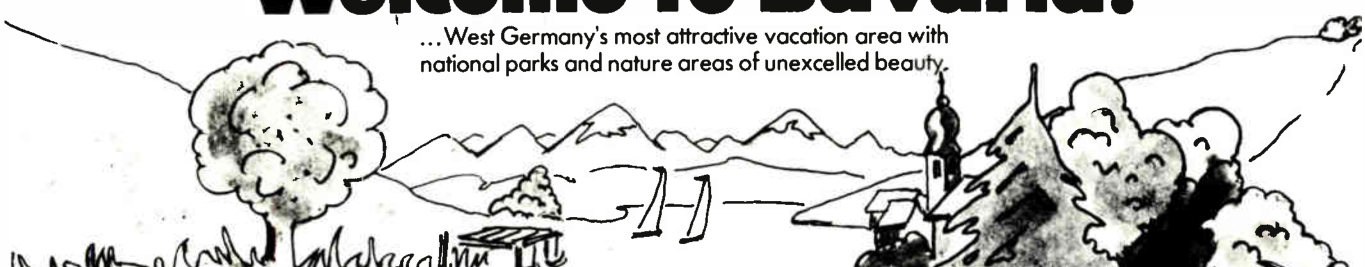

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EL 79/2

Microprocessor adds flexibility to television control system

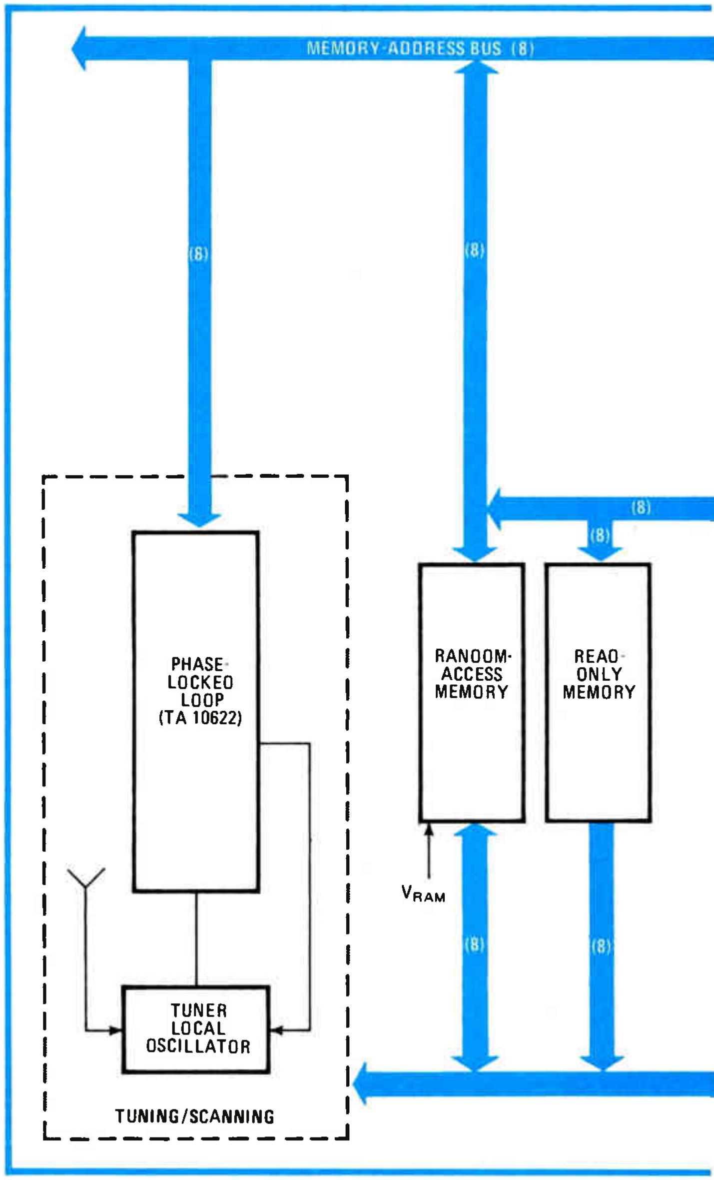
Programmable TV prototype synthesizes channel frequencies; features can be added easily through software modifications

by Kaare Karstad, *RCA Corp., Solid State Division, Somerville, N. J.*

☐ The television receiver is poised to enter an era of microprocessor control. Useful and sophisticated features will appear that could not be implemented in sets controlled by standard medium-scale integrated circuits or even custom large-scale ICs: the microprocessor's stored program opens up possibilities limited only by the designer's imagination and his budget.

Microprocessor control lends itself to modular design. Essential functions such as tuning and channel selection can be implemented first and other features can be added or existing ones modified. Features can be added for different markets simply by software changes; the expense of custom LSI development is avoided.

The prototype microprocessor-controlled color TV set described in this article has been designed, built, and successfully tested for a European customer. Constructed around one of RCA's 8-bit microprocessors (the CDP 1802), the prototype features control and channel selection from one of two keyboards, one on the set proper and another on a cordless hand-held remote unit (Fig. 1). Tuning is done using a custom LSI phase-



1. Computerized TV. Commands from two keyboards, one remote and cordless and another on the set, are executed by an 8-bit CDP 1802 complementary-MOS microprocessor supported by external read-only and random-access memory. The controller communicates with the viewer via a six-digit light-emitting-diode display.

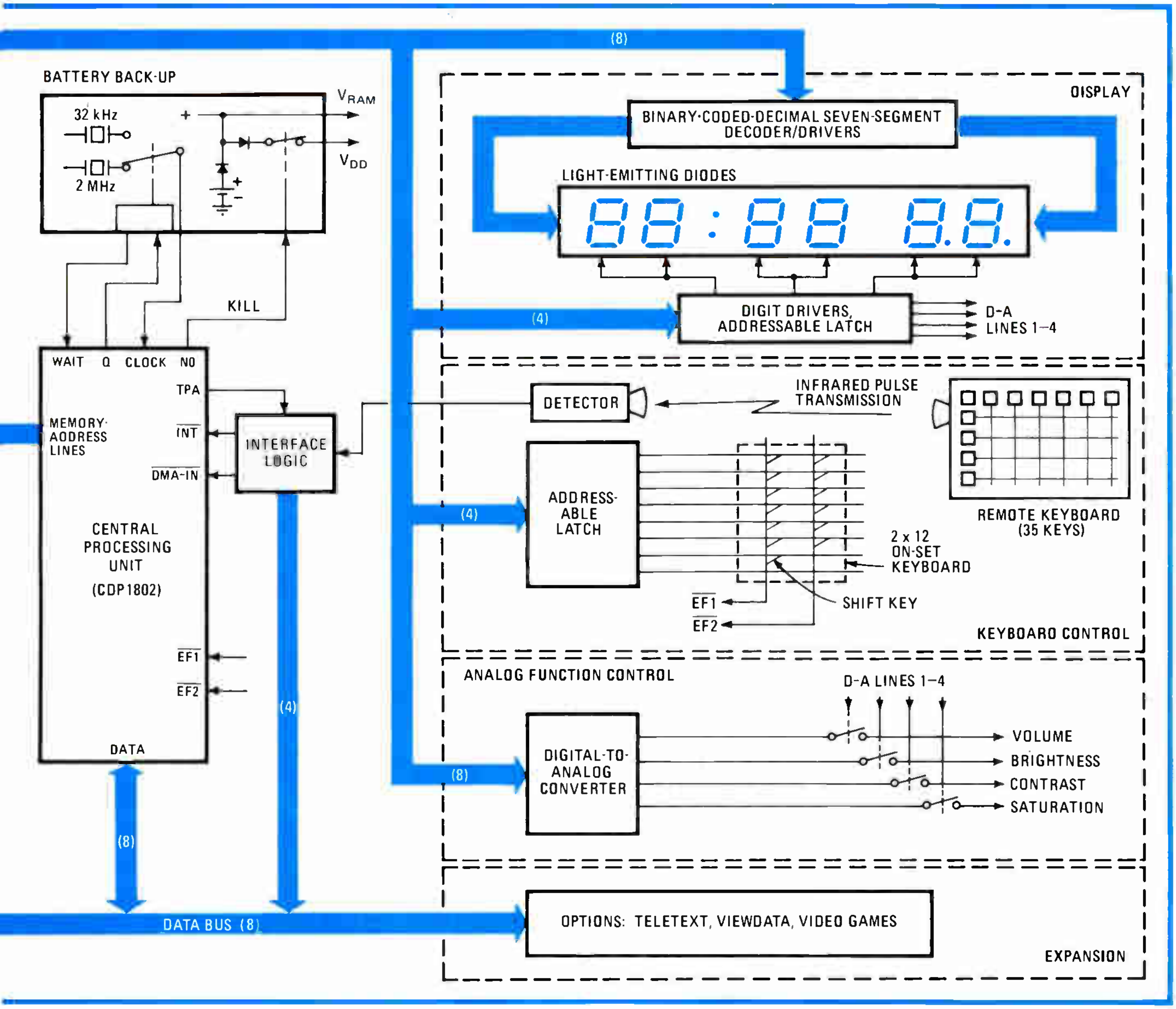
locked-loop (PLL) chip with controlled scanning and channel preprogramming. A real-time clock implemented in the complementary-MOS 1802-based microcomputer design allows the set to turn itself on or off or to switch channels in a sequence and at times chosen by the user. A six-digit light-emitting-diode display reads out time, channel, and other information. A two-level battery backup scheme using nickel cadmium cells maintains proper time for a week and keeps stored information intact for months if the power is cut off.

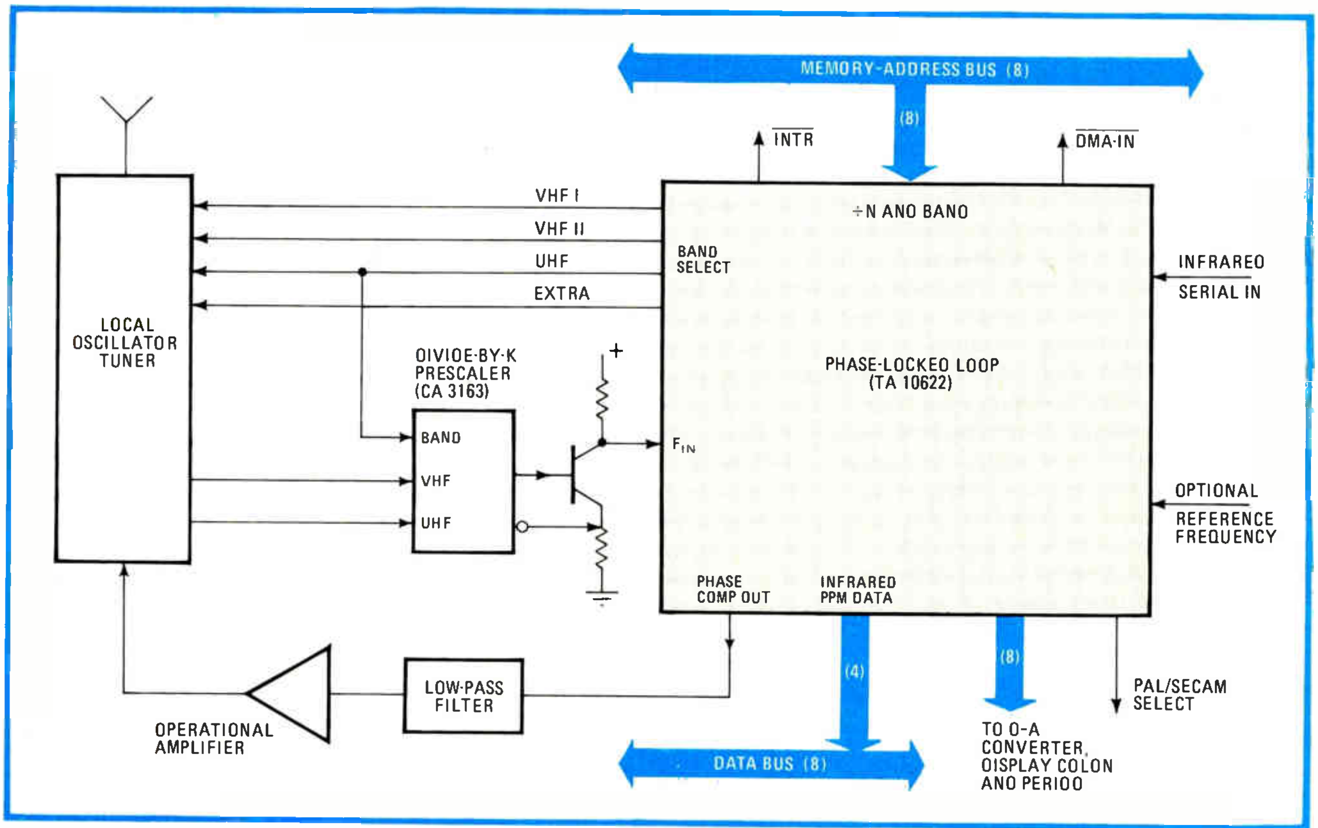
Locked in

This set's electronic tuning is done by frequency synthesis. The PLL chip and microprocessor compose a closed-loop frequency synthesizer. The entire PLL (Fig. 2), except for a prescaler made with emitter-coupled logic, a low-pass filter, and an operational amplifier, is integrated on a single custom C-MOS chip (TA 10622). The signal from a reference oscillator is compared with a signal from the local oscillator that has had its frequency divided by two counters. The first counter is the ECL prescaler, which divides the frequency of the local oscillator by either 64 (for very high-frequency channels) or 256 (for ultrahigh-frequency channels). This counter, whose dividing ratio is defined as K, brings the signal into a frequency range suitable for the low-frequency C-MOS circuits of the PLL chip.

The second counter is a user-programmable divide-by-N counter on the PLL chip. Any channel number from 1 to 99 punched in on the remote keyboard is translated into a 14-bit code for N according to international channel allocations by a ROM look-up table. At phase lock the tuner's local-oscillator frequency is $N \times K$ times the reference frequency.

This section uses a 16-bit–word data format. The 16 bits are sent out over the 8-bit memory-address bus with only one instruction, using register-based output. The 2 most significant bits are decoded to select one of four bands (designated vhf I, vhf III, uhf, and extra). The remaining 14 bits are the binary representation of the number (N) for a specific channel. These 14 bits give sufficient resolution to place the local-oscillator frequen-





2. Frequency synthesis. A custom large-scale phase-locked-loop integrated circuit fabricated in C-MOS handles tuning chores in conjunction with the local oscillator. The PLL chip contains a divide-by-N counter, phase comparator, and a reference-frequency divider.

cies as little as 25 kilohertz apart for vhf. This makes it possible to select any channel in the world, as well as unassigned channels used in cable-TV installations.

Because the prototype television was designed for a European customer, it was provided with the ability to preprogram or scan for network transmissions. A given country may have more than one network; these are designated in a European country by "program numbers." A given network (or program) is broadcast on different channels in different locations, just as the U. S. networks (ABC, CBS, and NBC) are.

Channel scanning

The prototype television can be programmed with a network number: 16 memory locations set aside for networks can each be assigned a channel. Tuning can then be done by keying in the desired network number from 1 to 16. This preprogramming technique requires that the channel frequency be known. If it is not, the receiver may be programmed by scanning the TV bands.

Starting at an available channel, a scan key is pressed to look for the next available actively broadcasting station up the band. If the scan button is released at this point, the channel is automatically assigned to the current network number. Each push of the scan button makes the tuning system search for the next available carrier. If no station is found, the scan wraps around and stops on the frequency where the search started.

In addition to the channel scan, a similar network scan is also part of the automatic tuning. This scan searches the 16 network storage locations for active stations.

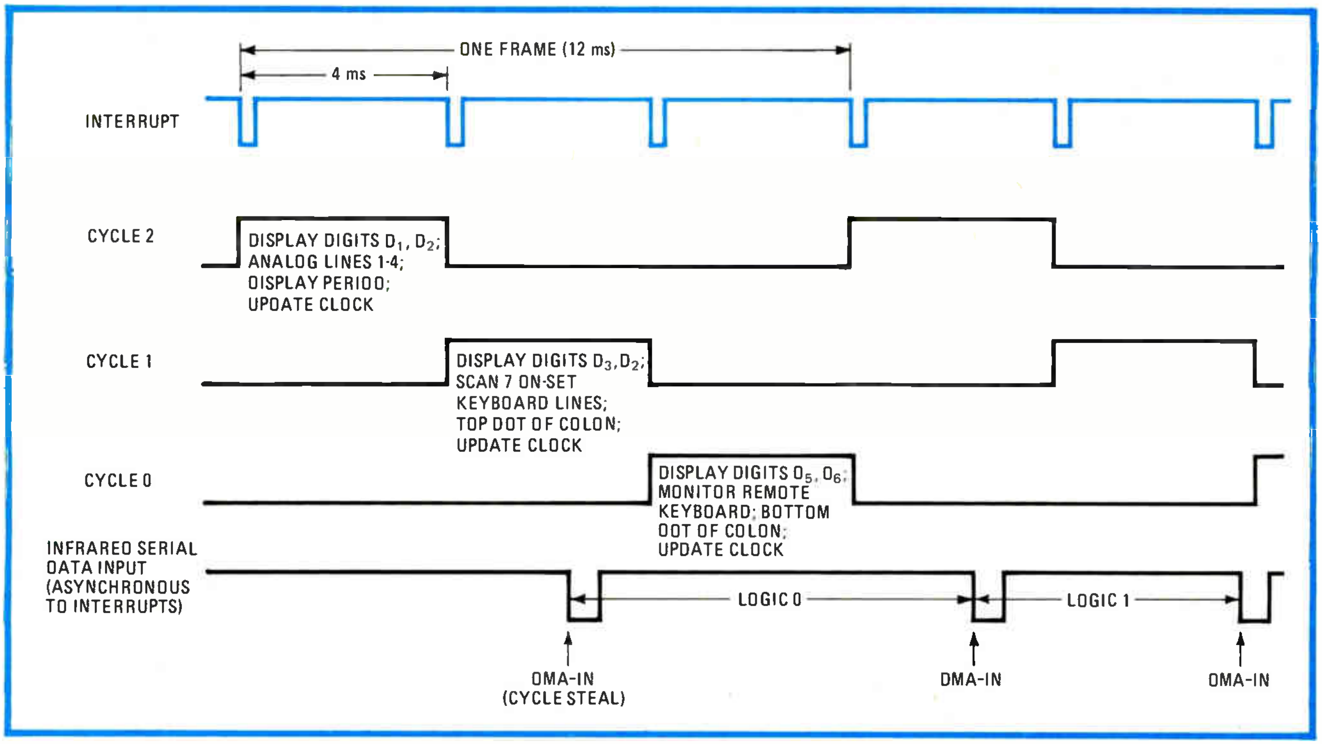
A viewer interacts with this TV through the on-set and remote keyboards. The LED display allows the user to monitor time, channel and network numbers, and memory storage locations. The normal display mode displays time (four digits) and network number (two digits) continuously. Upon request from a keyboard, both channel and network numbers are shown, the channel displacing the time display. In the network scanning mode, the channel numbers assigned to network numbers are also shown.

The on-set keyboard has 12 keys plus a shift key that allows it to handle 24 tasks, including network selection, scanning, muting, clock setting, turning the set on or off, and changing the values of the analog functions.

The 35-key master keyboard is a remote unit that communicates with the control system over a cordless infrared link. The 35 keys are necessary to handle the same functions as the on-set keyboard plus such extra functions as list, clear, channel scan, program event, cancel, viewdata, teletext, fine tuning, and others.

Command entry

Each depressed key on the remote unit generates a unique 7-bit code in a pulse-position-modulated (PPM) pulse train. A specific distance between pulses is defined as a logic 0, and a 1 is another defined distance. This pulse train, an asynchronous event with respect to any other processor task, is processed by the direct-memory-access (DMA) channel of the CPU chip. This allows the processor to give the random real-time event (the user pushing a button) its required priority over other tasks



3. Interrupt timing. Three interrupt cycles (2, 1, and 0) are derived from the system clock, and each is assigned certain service-routine tasks, such as refreshing display digits and analog-function channels, monitoring the keyboards, and updating the real-time clock.

initiated internally by the system software.

The analog functions—volume, brightness, contrast, and saturation—are changed continuously up or down while the appropriate key of either keyboard is held down. The current value of each of these functions is represented by a 6-bit word in RAM, which provides 64-step resolution. When the appropriate key is held down, this value is read out at a predetermined rate and incremented or decremented by one step each time. A sample-and-hold multiplexing technique makes it possible to use one digital-to-analog converter to serve the four different functions.

Sorted event list

The six-digit display and the 24-hour clock make it possible to preprogram and monitor events. An event can be defined as specific television material broadcast during a specified time period. This applies for a period as long as 24 hours. An arbitrary number of memory locations—eight in this design—are reserved for event programs. The user, while watching the display, simply punches in the desired time for the set to turn itself on (or switch channels if already on) and the network number to which it should tune.

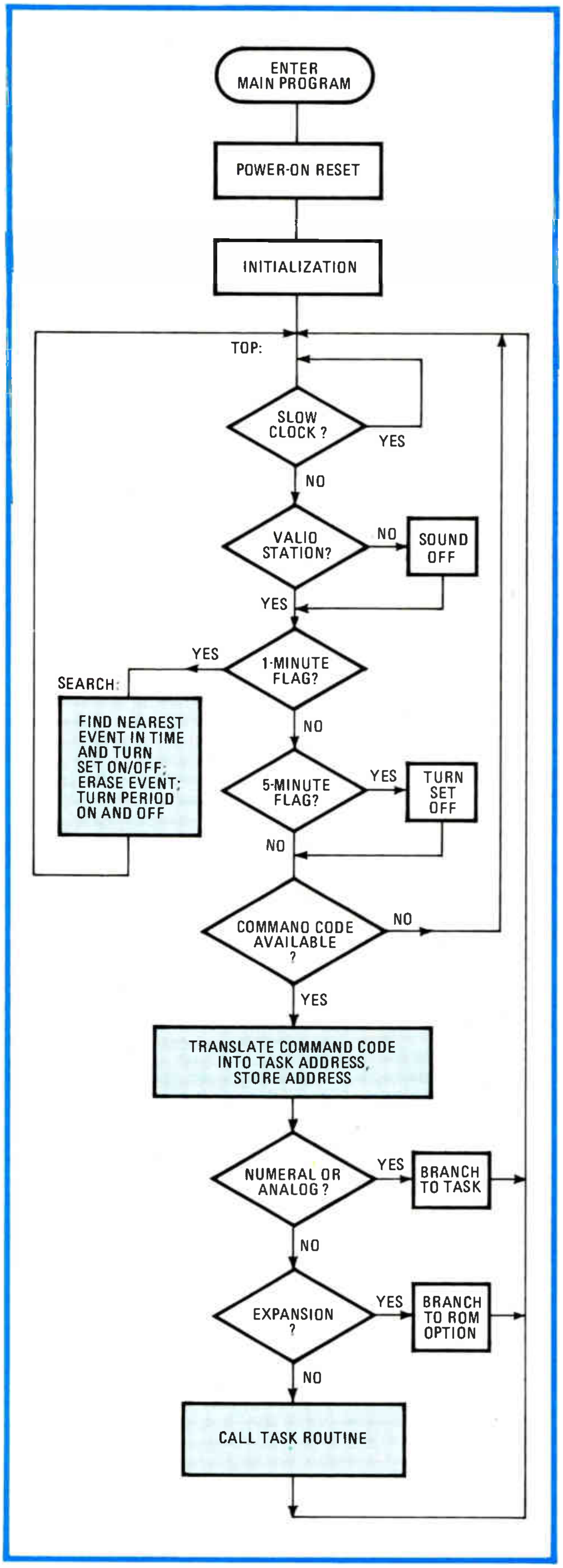
The software sorts the list of user-programmed events into a time sequence so that the event nearest in time always is on top of the list. The software then checks every minute to see if an event is to be executed; if so, the command is carried out, the executed event is erased from the list, and the next in time is moved up. One of the decimal points on the LED display, if lit, indicates that an event is pending. After the event is executed, the decimal point blinks until the viewer acknowledges the event by pushing any key. If no acknowledgement is received within five minutes, the set turns itself off.

The modular structure of the software makes it possible to add options by adding ports connected to the data bus and segments of code to the software. Teletext, viewdata, and video games are future options.

The microprocessor, through its software, must control the timing and data routing of the entire system. This includes multiplexing the six display digits, multiplexing the four analog channels, updating the clock, monitoring the two keyboards, and executing the tasks called for. The display must be refreshed at a rate high enough to avoid flicker—at least 50 to 60 hertz. The analog functions must also be refreshed steadily at a rate high enough to maintain a direct-current signal without excessively large filter constants. Keyboards must be checked frequently enough to catch any key depressions.

These overlapping and partially conflicting requirements are met by an interrupt-driven system together with the DMA channel used for the remote keyboard. Figure 3 shows the timing of the software interrupts. The interrupt pulse, derived from the CPU clock, interrupts main-program execution every 4 milliseconds.

To divide the processing load on the CPU, an interrupt frame of 12 ms is created and divided into three separate cycles (2, 1, and 0). A different set of tasks is performed by the interrupt service routine during each cycle. Cycle 2 refreshes LED digits D_1 and D_2, multiplexes the analog-function data, and updates the clock. Cycle 1 updates D_3 and D_4, scans the on-set keyboard, and updates the clock. Cycle 0 refreshes D_5 and D_6, monitors the remote keyboard, and also updates the clock. Note that serial data from the remote keyboard is asynchronous to the interrupt timing. The three cycles comprise a complete frame and are sequentially serviced. After 12



ms, a full interrupt service frame repeats.

When an interrupt occurs, the sequence of events is as follows. The last digit pair on the display is turned off and the next pair is turned on. Then the four analog channels are multiplexed and refreshed and the clock is updated. Control now returns to the main program. At the second interrupt, the last digit pair is turned off and the next one on. The clock is updated again but in this cycle the local keyboard is also scanned for key closure. At the third interrupt, the last digit pair is handled and the service routine checks to see whether a character is being received from the remote keyboard and processes the command. Once more the clock is updated and the main program resumes execution.

A key closure on the remote keyboard generates a bit string of pulses and for some commands a long character string. These pulse trains, which occur randomly and sometimes last for long periods, are received without tying up the processor and neglecting other real-time events since the pulses are fed into the DMA input. The data is conveyed to the CPU through a cycle-stealing process and for all practical purposes without slowing or interfering with the CPU's current operation.

The interrupt service routine in each 4-ms time slot may vary in length according to which cycle it is and how much of the clock-updating routine is required at a specific moment. Nevertheless, the processor is idle for the major part of the time slot, giving it time for background processing in the main program.

When control returns to the main program in each time slot, the program simply checks to see if a command was received from one of the keyboards. If so, that task (say, increase brightness) is executed. If no command has been received, the CPU is essentially idle until the next interrupt. In most cases the free time in one of the three cycles is ample for processing any task in the main program; if it is not, the next interrupt simply postpones the background processing into one or a few more time slots. This is not apparent to the user.

An interrupt can occur at any point in the main program (Fig. 4). Most of the time the main program goes through the loop at the top of the flowchart if no keyboard command has been received. A few other tests are also regularly made. Every minute, it searches for pending event commands. The program also checks to see if an event was executed but not acknowledged, if power has failed, or if the tuned station is on the air.

Time, display, and analog-function data is stored in RAM; this data is routed over the memory bus under control of the interrupt software to the correct circuit in the proper sequence.

For instance, four locations in RAM are allocated to the four clock digits. As shown in the flowchart of Fig. 5, a seconds counter is incremented at every interrupt. Later, in the update routine, this counter is tested for 1 second and an update buffer is loaded.

Another buffer in RAM, the display buffer, contains

4. The main event. The main program follows a loop at the top of the flow chart unless a keyboard command is received, in which case the corresponding task routine is called and executed. The TV set's audio output is automatically muted if it is not receiving a valid signal.

binary-coded-decimal data for the six display digits. The update routine transfers data for the four clock digits from the update buffer. The display buffer also contains addresses for the digit pairs, the seven scanning lines for the local keyboard, and the four multiplexed d-a lines.

The configuration of the data in the display buffer is closely related to the hardware scheme shown in Fig. 6. LED segment data for a digit pair is fed from two separate latch/decoder circuits (CD 4511s). An 8-bit addressable latch (CD 4099) selects the digit pair or the d-a channel to be sampled. Another addressable latch (also a CD 4099) provides scan addresses for testing key closures on the on-set keyboard. The required 16 bits of data are assembled in one 16-bit CPU register and read out over the memory-address bus with one instruction.

Four RAM locations store the 6-bit data for the analog functions. It is read out before the d-a channels are sampled. The latched data is smoothed by the R/2R network shown in Fig. 6. No great precision is required.

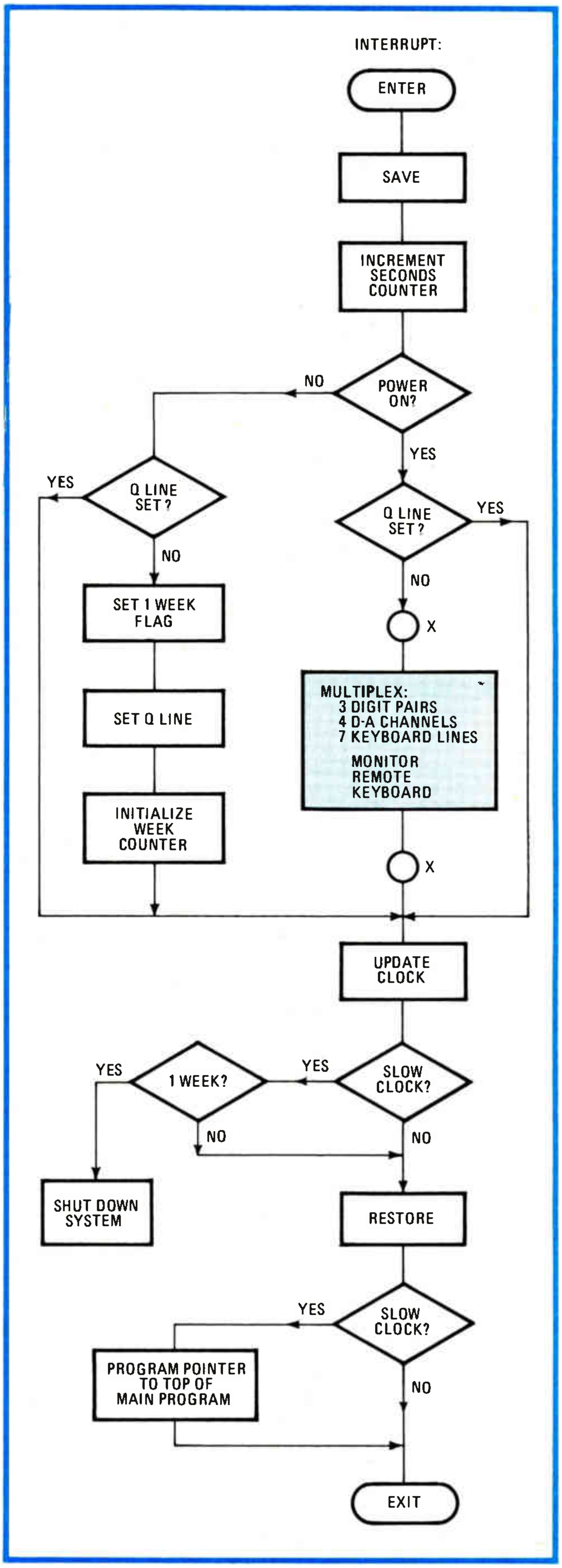
The software section of the interrupt routine that interacts with this hardware turns off the last select line for a digit pair and tests to see if the program is in cycle 0. If the answer is yes, a new frame of interrupt events is about to begin and the display pointer is reset to the top of the display buffer. Segment data for the next digit pair is read out and the pair is selected.

For example, if the answer to testing cycle 2 is yes, the four d-a channels are sampled in a burst mode, after which the program branches to the update routine. At the next interrupt, since it was not cycle 0, the program turns on the next digit pair. The program finds itself in cycle 1 and the on-set keyboard routine is activated. Finally, at the third interrupt (cycle 0), the remote keyboard routine is executed.

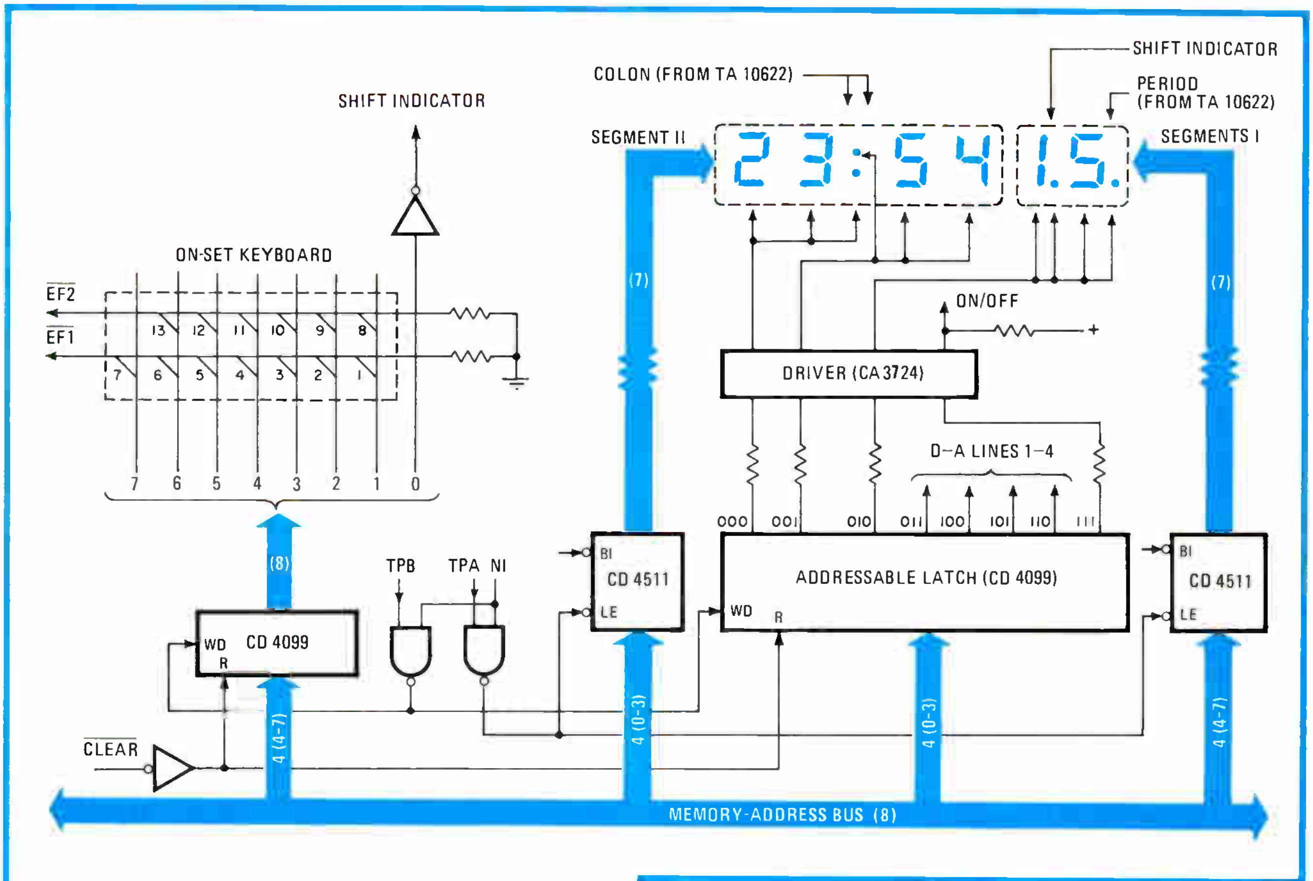
A key depression on the local keyboard is translated into a command code and stored in memory for the main program to process. The sequence of events is as follows: one of the output lines from the addressable latch is activated and the CPU tests the first flag line (EF1) for key closure (Fig. 6). If the output line is number 4 and flag-line 1 is tested (defined as row 0) then a possible key closure is identified and marked as key number $4+0 = 4$. Next the CPU tests line 4 and flag-line 2 (EF2, defined as row 7). A key closure is here identified as key number $4+7 = 11$.

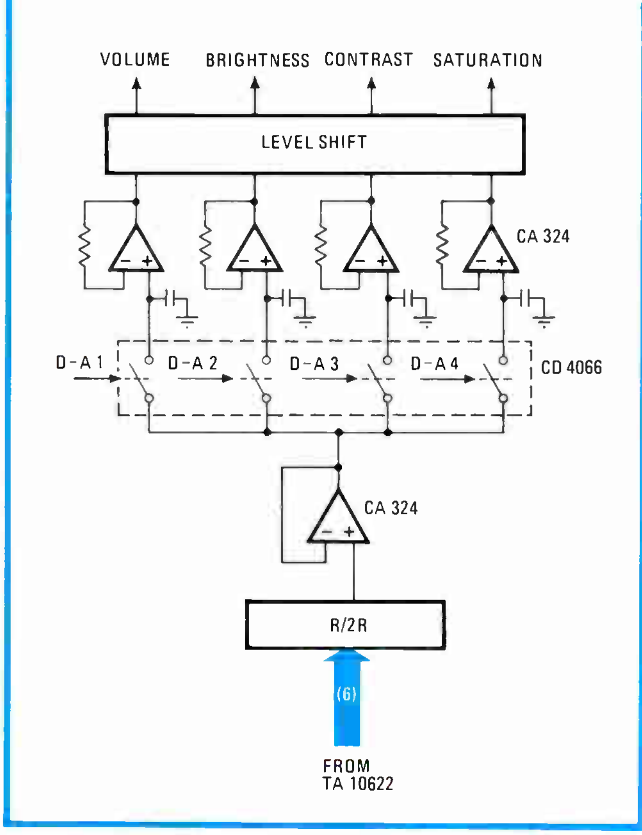
The received and detected infrared PPM pulse stream from the remote unit is composed of 6 bits plus 1 parity bit for each character. The software checks for the presence of a bit stream, measures the time between pulses (thereby discriminating between 1s and 0s) and assembles the information into a character that represents the actual command code. Finally, the program tags the received command code with its type—a single command (on/off) or a repeat command (increase volume) for the duration of the key depression.

A 4-bit counter is clocked by a 10-kHz signal. The contents of the counter are read at the beginning of each



5. Interrupt tasks. The interrupt service routine increments a seconds counter and updates the real-time clock. It also initiates refreshing of the display and analog-function channels and switches to a slower system clock and backup battery power if power fails.





6. Multiplexing. A compact 16-bit-word data format ties the LED display, the four analog-function channels, and the on-set keyboard together. An 8-bit addressable latch (the left-hand CD 4099) selects the proper display-digit pair or analog channel to be refreshed.

infrared pulse, whereupon it is restarted. Hence the number of clock pulses counted represents the time interval between the last two infrared pulses. As the infrared pulse itself activates the DMA input line, the time count is automatically read into a memory location.

The DMA pointer of the CPU advances in readiness for another input byte, which occurs at the next infrared pulse. Hence the 7 bits in a command, represented by seven counts, are automatically stored in memory.

A battery backup system is implemented to avoid losing track of the time or losing stored data during power failure. The outage may last from seconds to hours or indefinitely. Due to an all-C-MOS circuit design, continuous operation is possible with four small rechargeable nickel cadmium cells.

A two-stage battery mode is used in this prototype. The CPU senses a power failure; the batteries automatically take over and run the whole processing system for a predetermined period of one week (Fig. 5).

Upon detecting a power failure, the CPU automatically switches from its 2-megahertz crystal to a low-frequency 32-kHz crystal in order to conserve power. The switching takes place during a wait state a few milliseconds long, which the CPU also enters upon detecting power failure. If power is not restored within a week, the CPU turns itself off after shutting down the whole system with the exception of the RAM programmed by the user.

Battery power is sufficient for approximately three months of storage. If power returns before three months have passed, operation resumes as normal with stored information intact. □

10-ns monolithic d-a converter keeps bipolar drive circuits hustling

Teamed with fast ECL microprocessor, 8-bit converter produces wide variety of high-resolution output waveforms

by Bill Blood and Loren Kinsey, *Motorola Inc., Integrated Circuits Division, Mesa, Ariz.*

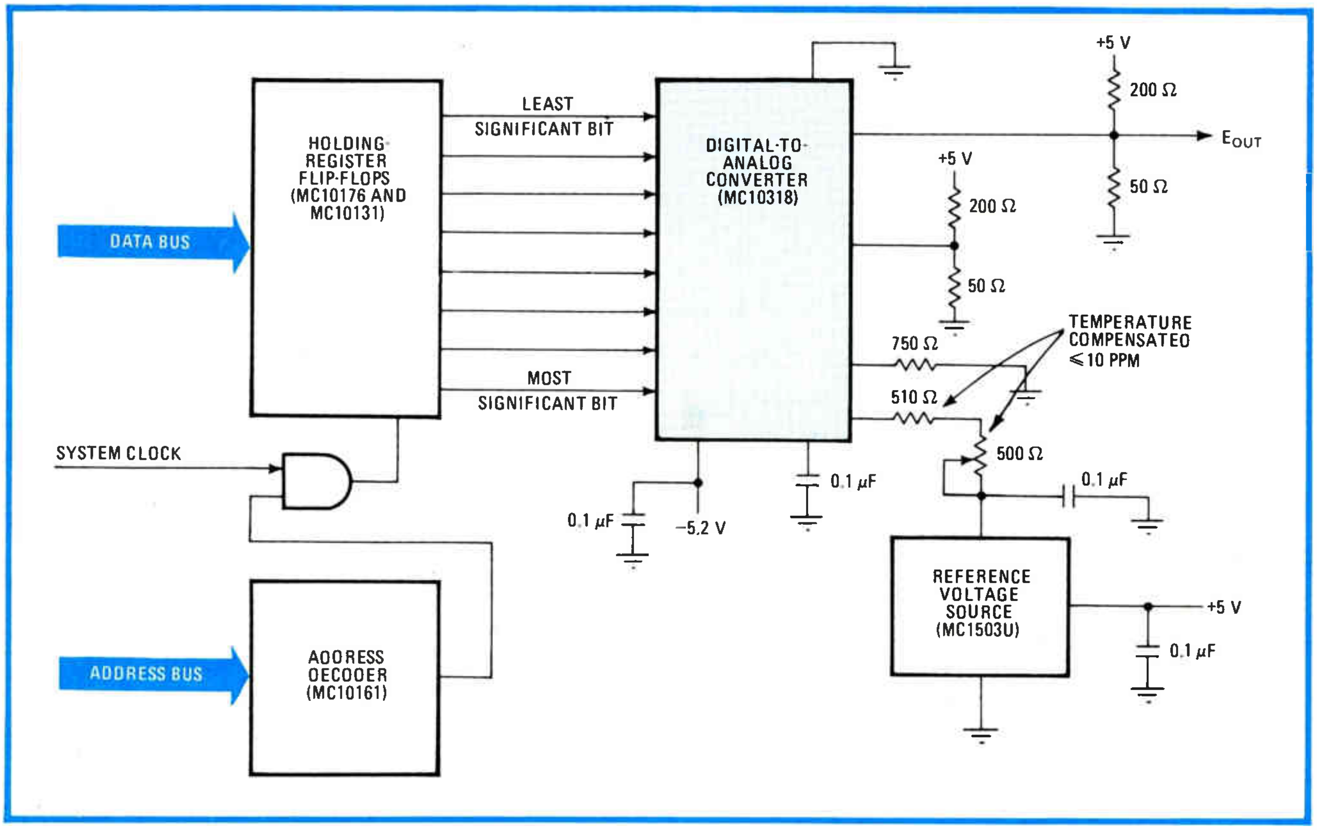
☐ Monolithic digital-to-analog converters have been able to match the relatively low speeds of MOS logic and microprocessors for some time. But high-speed bipolar logic, such as a TTL or emitter-coupled-logic bit-slice microprocessor with a 100-nanosecond cycle time, is vastly underutilized when used to drive a 300-ns d-a converter.

The MC10318 monolithic 8-bit d-a converter, however, gives ECL drive circuitry a chance to work to capacity. It has a combined conversion and settling time of 10 ns. Test and communications equipment involved in digital filtering or signal processing could benefit from the 10318's speed, as could other high-speed digital systems that must produce an analog output.

Compatible with Motorola's MECL 10,000 family, this converter does away with the complex interface normally required between high-speed processors and slower d-a converters. The 10318 accepts an ECL 8-bit binary input and generates analog current outputs that are accurate to within ±½ least significant bit. Driving this converter with a microprogrammed M10800-family ECL bit-slice processor to produce high-resolution waveforms of nearly any shape demonstrates what it is capable of doing. A circuit diagram of such an arrangement is shown in Fig. 1.

How it's done

The microprogrammed processor used to drive the d-a converter is shown in Fig. 2. Microprogram memory addressing is performed by the MC10801 micropro-



1. Microprocessor-driven. The MC10318 10-ns monolithic digital-to-analog converter can easily be driven by a bit-slice microprocessor to produce high-resolution waveforms. Minimal interfacing is required, since the converter is fast enough to keep up with the microprocessor.

gram-control integrated circuit, in a word/page format. Feedback signals from the microprogram memory instruct the 10801 on how to sequence through the program. Sequencing occurs in response to common instructions like increment, direct jump, conditional jump, jump to subroutine, and so on.

Next-address inputs are normally used to supply program-jump destinations from the microprogram memory. In this application, the 10801 microprogram controller allows next-address information to be transferred from look-up tables placed in the microprogram memory to the arithmetic and logic unit (ALU) and data outputs. This permits random waveforms to be generated extremely rapidly.

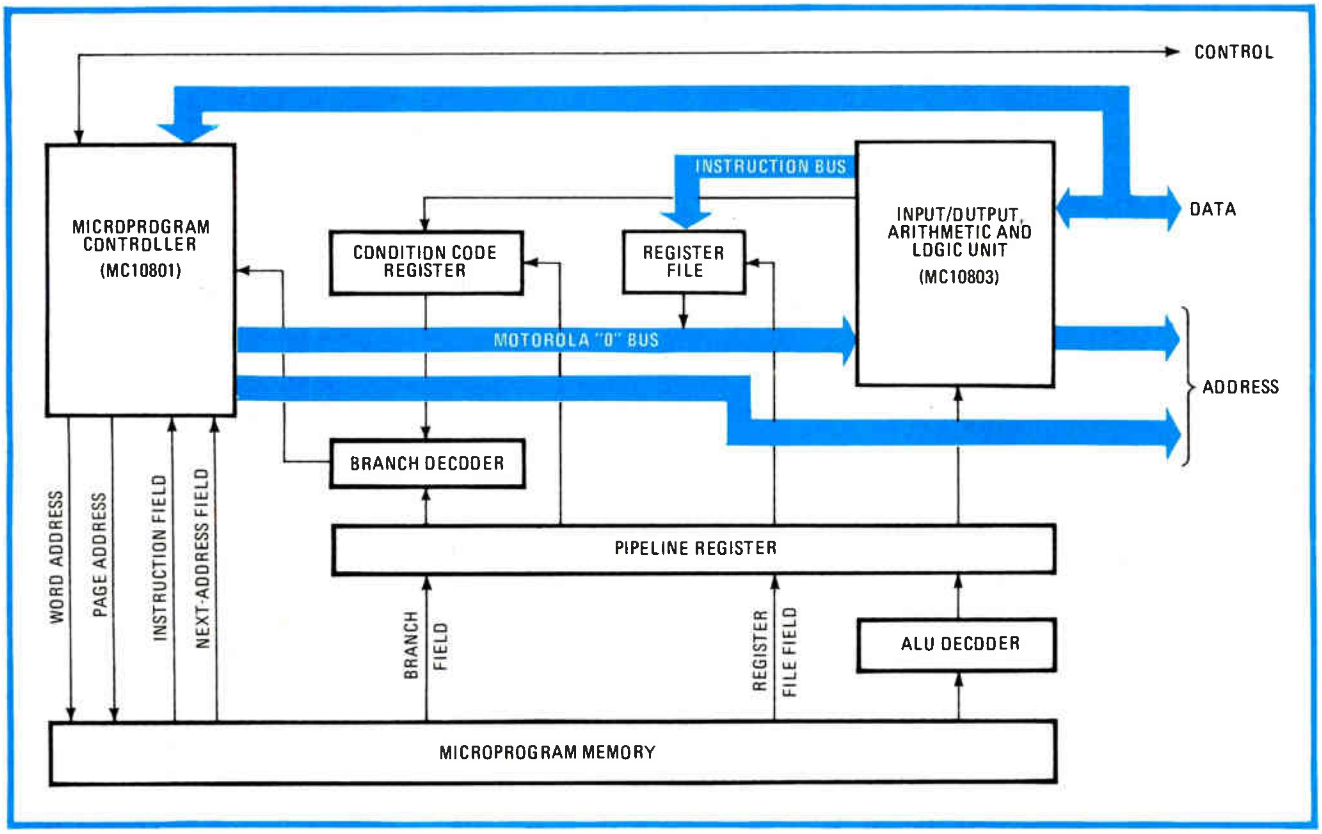
ALU and input/output operations are handled by an MC10803 memory-interface circuit. The 10803 is primarily an I/O device, but part of it is used as an ALU. It offers excellent interfacing at the expense of some arithmetic power, compared to the MC10800's ALU capability. Four internal 10803 accumulators and a 16-word register file store ALU operands, addresses, and data constants. A pipeline register (built using the MC10176 hexadecimal flip-flop) holds microprogram information, allowing the 10801 to generate a new microprogram address in parallel with the 10803 while the latter is executing a microinstruction. The overlap of addressing and execution permits a 100-ns worst-case microinstruction cycle time. This ability to update the 10318 in 100 ns, either from a lookup table or with simple ALU calculations, is 30 to 60 times faster than is possible with a MOS microprocessor doing the same job.

Address, data, and control lines from the processor interface easily with the d-a converter. An address-decode signal selects the converter as an output peripheral. A proper-address signal then enables the system clock to initiate the transfer of data-bus information to an 8-bit holding register. Binary outputs from this holding register are then fed to the d-a converter for conversion to an analog output current. The holding register's outputs remain constant as long as no address signal is received.

The d-a converter can produce a wide range of output voltage levels (between −1.3 and +2.5 volts) and output currents of up to 51 milliamperes. The use of 200-ohm resistors between the converter's output pins and the +5-volt line, as well as 50-Ω resistors from the outputs to ground, provides an analog output voltage range of +1 to −1 V at a full-scale output current of 50 mA. Output accuracy is maintained by the MC1503U, a temperature-compensated, well-regulated 2.5-V source connected to the d-a converter's reference input. The 500-Ω potentiometer is set for a calibrated full-scale output of 50 mA.

The use of 50-Ω resistors from output to ground allows the substitution of properly terminated 50-Ω coaxial cables. This permits the analog output to be transmitted a reasonable distance without special buffers or drivers.

The use of a look-up table in microprogram memory is the most direct way to use the bit-slice microprocessor. Any waveform mapped on the grid of Fig. 3 can be duplicated at the d-a converter's analog output. The converter's resolution of 8 bits provides it with 256



2. Bit-slice microprocessor. The MC10803 emitter-coupled-logic microprocessor specializes in input/output; it features microprogramming capability for a 100-nanosecond cycle time. This allows a high-speed digital-to-analog converter to be driven efficiently.

Building a high-speed d-a converter

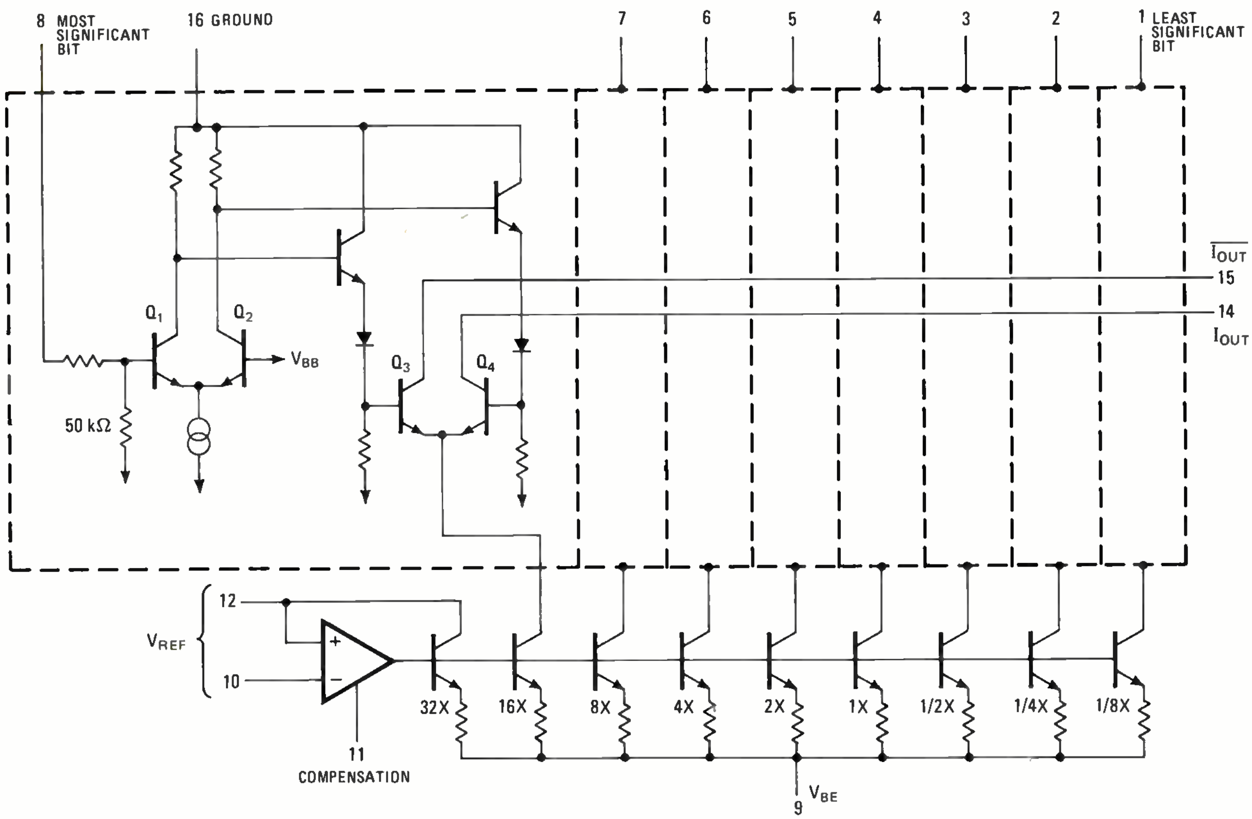
The MC10318's high speed results from the use of emitter-coupled-logic differential amplifiers, a high-speed current-summing conversion technique, and ECL integrated-circuit processing technology. The converter's current summing is shown below. Signals on the eight inputs, compatible with the MECL 10,000 family, have a logic 1 level of −0.9 volt referenced to ground, and a logic 0 level of −1.7 V. The input signals are measured against an internally generated bias-voltage source of about −1.3 V.

Collector outputs of the input differential amplifiers are buffered and translated downward to current-summing differential amplifiers. Precision constant-current sources in the respective current-summing amplifiers are weighted according to bit value with the most significant bit have 128 times more current than the least significant bit. Reference inputs to the constant-current sources are used for calibration and to establish full-scale current levels.

Full-scale current is approximately 15.9 times the reference input current (3.1 mA for a full-scale 50-mA output).

The presence of logic 1 levels on all data inputs causes transistor Q_1 to conduct, thereby cutting off transistor Q_2. This in turn causes transistor Q_4 to conduct and cut off transistor Q_3. Maximum output current is then pulled from the current output, I_{out}, while its complement, $\overline{I_{out}}$, is kept essentially floating.

The presence of logic 0 on all data inputs reverses the process, pulling maximum output current from $\overline{I_{out}}$. A combination of input logic levels 1 and 0 splits the current between both outputs in proportion to bit weight. The total of both outputs is always equal to the maximum output current. Constant-current sources in the input differential and current-summing amplifiers keep the converter's power level constant, independent of input and output signals, for minimum noise and maximum speed.

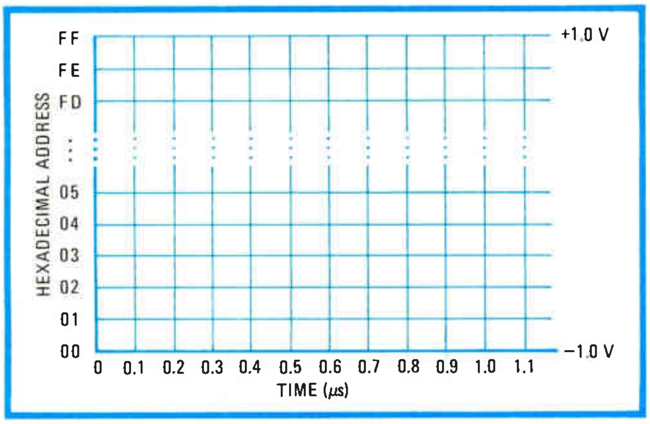


distinct voltage levels (hexadecimal address codes 00 to FF) over a range of −1.0 to +1.0 v. The horizontal axis in the grid of Fig. 3 is divided into 100-ns increments, the top cycle time for the microprocessor. Since the microprocessor is made up of static bipolar circuits, the system clock can be varied from 0 to 10 megahertz for additional output frequency control.

An example of the possible waveforms is shown in Fig. 4 (top), which has true (upper trace) and complementary (lower trace) analog outputs formed by a five-level stairstep program. It only takes six microprogram words to generate this waveform, each equal to a 100-ns microcommand. The program is as follows:

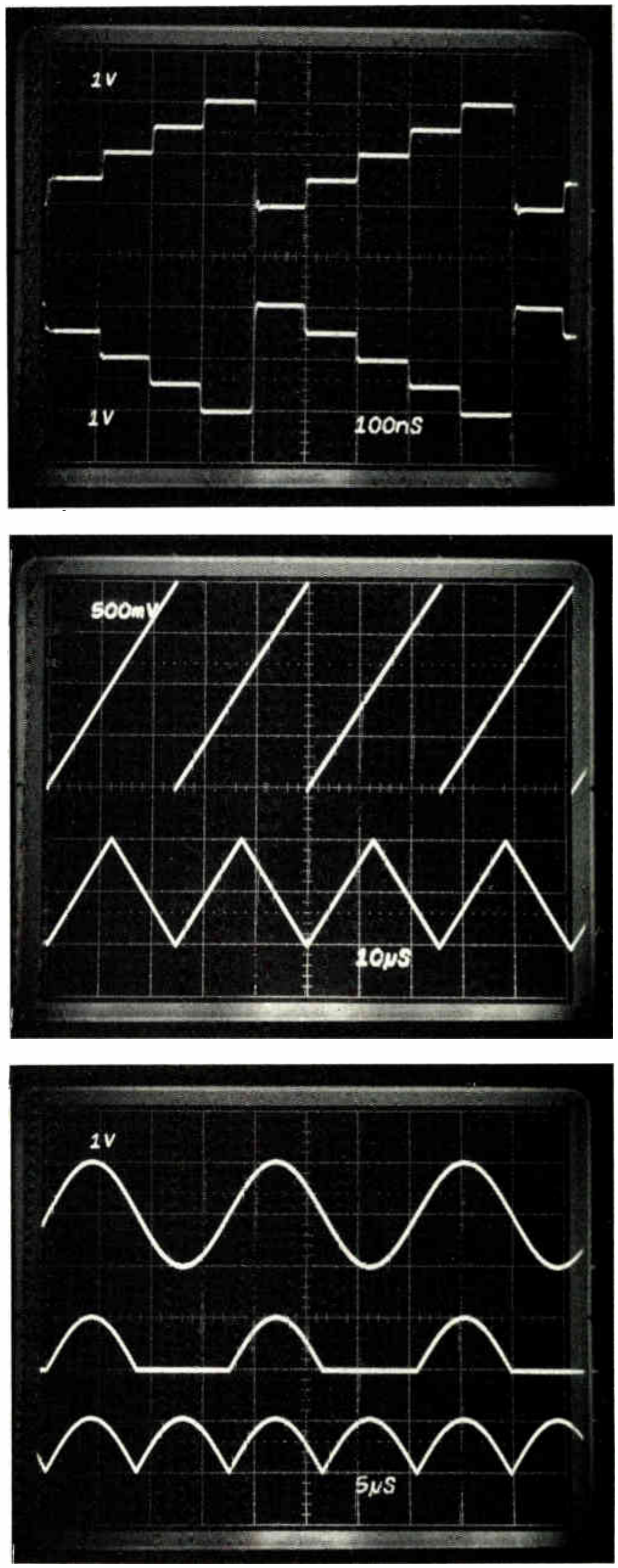
1. Increment and set the d-a converter's address.
2. Increment and set the data bus to hexadecimal address code 00 (in this case corresponding to an output of −1.000 v).
3. Increment and set the data bus to hexadecimal address code 40 (output of −0.498 v).
4. Increment and set the data bus to hexadecimal address code 80 (output of +0.004 v).
5. Increment and set the data bus to hexadecimal address code BF (output of +0.498 v).
6. Jump to instruction 2 and set the data bus to hexadecimal address FF (output of +1.000 v).

Figure 4 also illustrates the model 10318 d-a convert-



3. Waveform grid. Processor-generated analog output of d-a converter can follow every waveshape drawn on this 256-line-by-11-interval (100 nanoseconds each) grid.

4. Microprogrammed waveforms. Various processor-generated waveforms illustrate the flexibility of driving a d-a converter with a bit-slice processor. Depending on program size, different patterns are possible. Shown are waveforms generated by a microprogram of 6 words (top), 2 and 6 words (middle), and 11 words (bottom).



er's short conversion time and high edge speeds. As can be seen, changes in the analog output are only a small percentage of the 100-ns-per-division oscilloscope trace.

The microprocessor's ALU can calculate simple patterns to reduce program space that would otherwise be required for a look-up table. Figure 4 (middle) shows two ramp patterns based on incrementing or decrementing the data bus every microinstruction. The upper trace, a 256-step ramp requiring 25.6 microseconds per cycle, needs only a two-word microprogram:

1. Increment and set the d-a converter's address.
2. Jump to instruction 2 and increment the data bus.

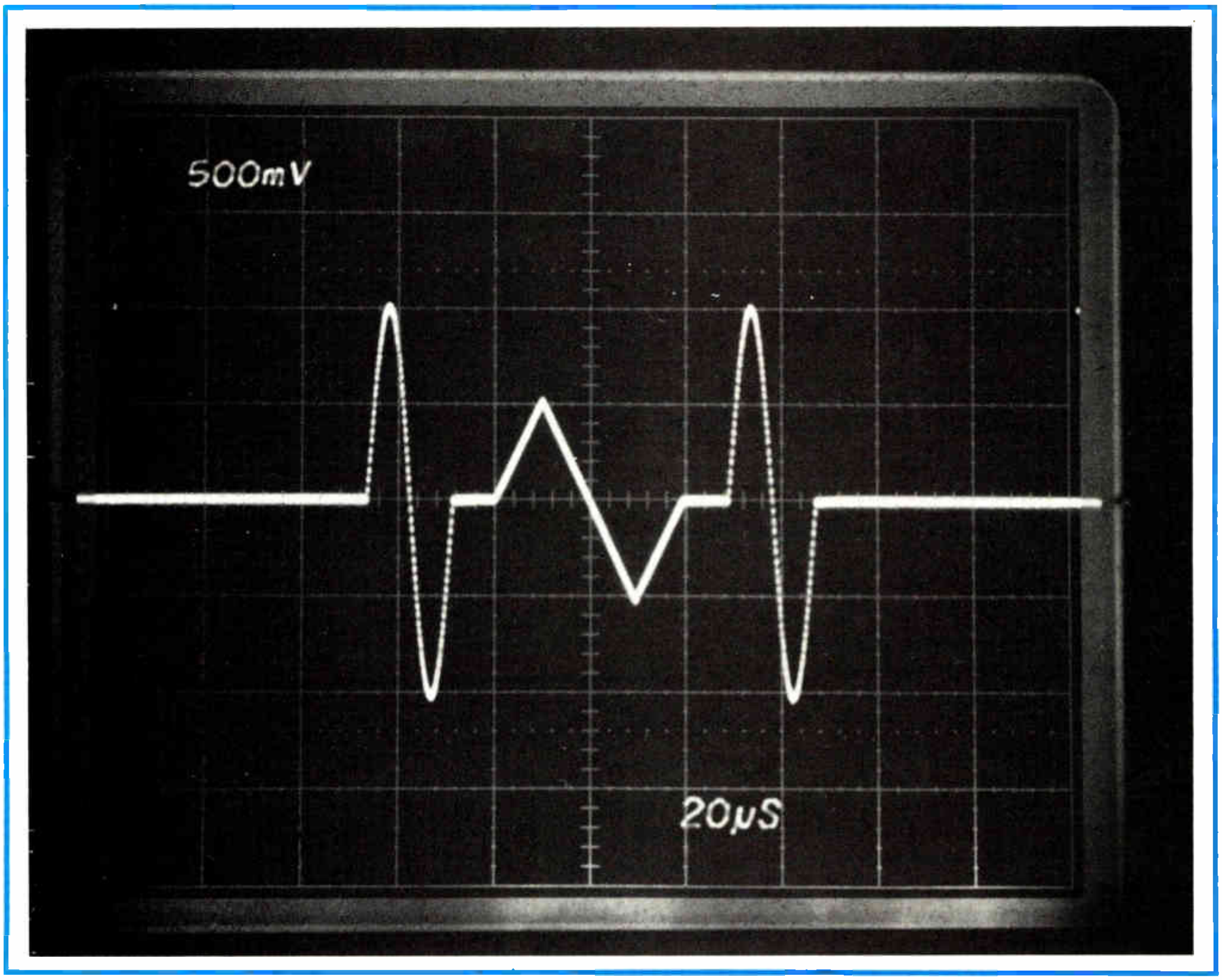
The lower trace of Fig. 4 (middle) makes use of more microprocessor features to control waveform end limits and the number of repetitive steps in a cycle. Its six-word program is as follows:

1. Increment and set the d-a converter's address.
2. Increment and set the data bus to hexadecimal address 40 (−0.498 v).
3. Increment and set the program cycle counter (in the 10801 microprogram controller) for 126 iterations.
4. Repeat and increment the data bus 126 times and move on to instruction 5.
5. Decrement and set the program cycle counter for 125 iterations.
6. Repeat and decrement the data bus 125 times and jump to instruction 2.

Note that words 5 and 6 are similar to words 3 and 4 in the program, except that the former are decrementing instructions. The repeat count in instructions 5 and 6 is one less than that in instructions 3 and 4 to compensate for the extra microinstruction at word 2.

The performance advantage of a microprogrammed bipolar LSI microprocessor over MOS microprocessors becomes more obvious when the program must keep track of program cycle counts as in the preceding example. The bipolar bit-slice microprocessor executes the 10801's repeat instructions in parallel with the 10803 ALU increment or decrement commands, maintaining a 100-ns converter update interval. An MOS microprocessor, on the other hand, handles cycle count in series with output results and would therefore be 60 to 120 times slower than the ECL microprocessor used here.

With a few more instructions and some subroutines,



5. Unique patterns. When different programs are combined, the MC10318 d-a converter can be driven by the MC10803 microprocessor to produce unique pulse patterns. The programming flexibility afforded allows the generation of an unlimited number of signal patterns.

sophisticated waveforms can be generated. The three waveforms in Fig. 4 (bottom) were generated with subroutines in the look-up table. One subroutine named Sinpos starts at the waveform's midpoint (0 V) and generates the first 180° of a sine wave in 3° increments. Another subroutine, Sinneg, provides the next sine wave half in a similar manner.

Table of subroutines

An 11-word program using the two subroutines just mentioned generates the respective sine-wave, rectified half-wave, and rectified full-wave output waveforms of Fig. 4 (bottom). With a little care, the program can be written to supply proper output data every microinstruction, even while jumping to and from subroutines. Such a program can look like this:

1. Increment and set the d-a converter's address.
2. Jump to subroutine Sinpos and set the data bus to hexadecimal address 80.
3. Jump to subroutine Sinneg and set the data bus to hexadecimal address 80.
4. Jump to instruction 2 and set the data bus to hexadecimal address 79.
5. Increment and set the d-a converter's address.
6. Jump to subroutine Sinpos and set the data bus to hexadecimal address 80.
7. Increment, set the program cycle counter for 58 iterations, and set the data bus to hexadecimal address 80.
8. Repeat, jump to instruction 6, and set the data bus to hexadecimal address 80.
9. Increment and set the d-a converter's address.
10. Jump to subroutine Sinpos plus one step and set the data bus to hexadecimal address 86.
11. Jump to instruction 10 and set the data bus to hexadecimal address 80.

Figure 5 further demonstrates programming flexibility by combining some of the programs of Fig. 4 into a unique output pulse pattern. More important, the examples given in Figs. 4 and 5 illustrate the capability of generating unlimited signal patterns. Although slower microprocessors and d-a converters perform similar functions, the quantum performance jump offered by the 10318 d-a converter and the M10800 ECL LSI processor family opens up new application areas for digitally generated analog signals. □

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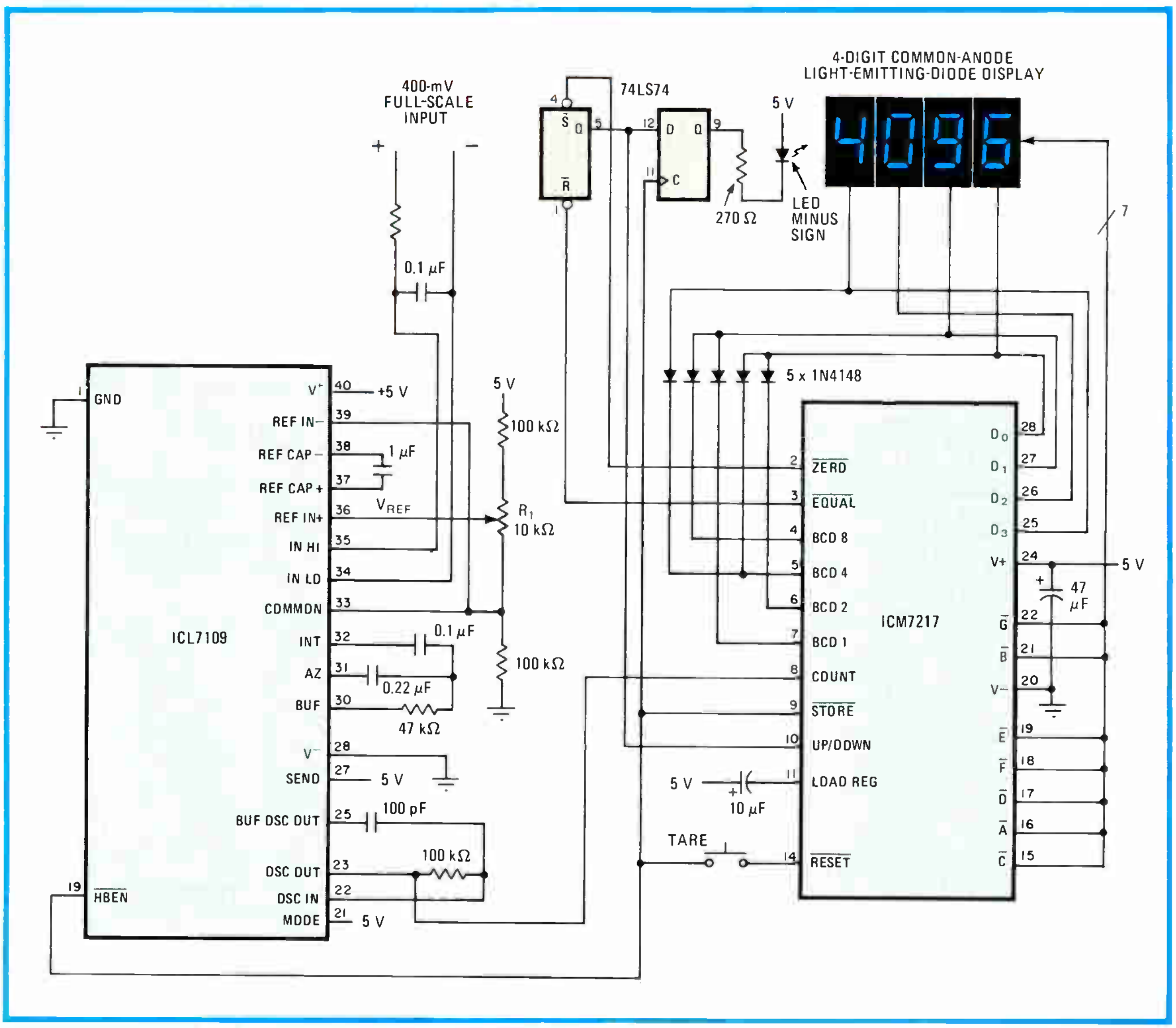
Programming systems for tomorrow...today.

Three-chip digital scale zeroes tare weight

by David Watson
Intersil Inc., Reading, Berks., England

A 12-bit analog-to-digital converter forms the nucleus of this digital scale, which compensates for the tare (the weight of the container holding the material to be measured) so that the net poundage can be determined. Combined with a decade counter that drives common-anode light-emitting-diode displays and a flip-flop for coordinating circuit activities, the unit makes for an accurate, compact, and direct-reading instrument that costs under $40.

An analog voltage corresponding to the object under measurement (obtained here from a 2-kilogram load cell transducer) is applied to the ICL7109 a-d converter, which uses the highly accurate dual-slope method of transforming analog potentials into their digital equivalent. In this technique, a two-step auto-zero and input-voltage integration phase is carried out in 4,096 clock periods, serving to eliminate offset voltages and deter-



Weight reduction. Digital scale in effect subtracts weight of container holding object to be measured so that true (net) poundage can be determined and displayed. Compact and accurate three-chip circuit can be built for less than $40, including display.

mine the magnitude and polarity of the sampled voltage. During this time period, the converter's oscillator delivers clock pulses to the ICM7217 counter/display. The deintegrating phase that follows steps the voltage to 0 in inverse fashion. When the voltage reaches 0, the $\overline{\text{HBEN}}$ signal is generated to freeze the counter/display, with the number of oscillator output pulses generated during this phase being proportional to the magnitude of the input voltage.

The counter's up and down line is controlled by the 74LS74 flip-flop, which is alternately set and reset by the zero (counter at zero) and equal (input equal to 4,096) lines of the ICM7217. Because the counter is preloaded to 4,096 on power up, it is thus free to cycle between 0 and 4,096 during each conversion. Therefore, a number between 0 and 4,096 will be displayed that is equal to the number of output pulses emanating from the converter during the deintegrating phase. With suitable scaling (selected with potentiometer R_1) and the appropriate choice of a presettable number in the counter, the displayed value can be made to correspond directly to the magnitude of the input voltage. As shown in the figure for the general case, the analog input that is required to generate a full-scale output of 4,096 counts occurs when $V_{in} = 2V_{ref}$.

When the tare weight is being measured, the $\overline{\text{HBEN}}$ pulse activates the store input of the counter every 8,192 clock periods, and a constant but initially random number is observed. When the tare button is momentarily engaged, the counter is reset by $\overline{\text{HBEN}}$ and the display will be zeroed. The display will remain cleared thereafter, because with an unchanged weight, $\overline{\text{HBEN}}$ enables the display at the same time in each measurement cycle. In this instance, the display is enabled when the counter reaches 0.

When a variable weight (the object weight) is added, corresponding to N counts of the a-d converter's internal clock, $\overline{\text{HBEN}}$ latches up N counts later than previously; therefore, a number greater than 0 is displayed. Conversely, if N bit values of weight are removed, −N will be displayed. Note that the minus-sign LED will be activated in this case, because F_1 will be low.

Because of input noise, the resolution of the a-d converter will be nominally limited to about 40 microvolts per count, and it will be much worse in industrial environments. Typically, the output of a load cell having 1-millivolt/volt sensitivity will be 2.5 microvolts/gram when operated at 5 volts. Under these circumstances, a stable preamplifier such as the ICL7601 commutating auto-zero (CAZ) device may be required. The input of the ICL7109 accommodates differential inputs, and thus the amplifier need not provide differential single-ended output ports.

If a resolution of greater than 4,096 counts is required, an a-d converter of greater accuracy can be readily substituted for the ICL7109. The ICM7217 can be cascaded with similar units to handle the increased number of bits. □

RAM diagnostic performs nondestructive check

by John Beaston and Mike Scott
Intel Corp., Brussels, Belgium

Although most routines for checking electrical faults in random-access memories are very effective, they usually destroy any data that may be stored in the RAM at the time the test is performed, thus precluding its testing during actual system operation. But a RAM may be examined without disturbing its contents if use is made of the technique illustrated in this program, which is written for the Intel MCS-48 microcomputer.

The routine uses a method long utilized in the testing of read-only memories—the checksum, wherein the actual contents of the device are compared to the known data that should be contained within it. The checksum technique is applicable here because the contents of RAM are fixed during the diagnostic test.

Initially, the program accumulates the checksum of the current contents of the RAM. The program then inverts the state of the first bit in the RAM and accumulates a new checksum. Because the state of the first bit is known, the expected value of the new checksum may be computed. If the computed checksum is equal to the actual accumulated checksum, the program returns the first bit to its original state.

This process is repeated for every bit in the RAM. By testing the RAM in this manner, any addresses or bits inadvertently linked will generate an incorrect checksum—that is, the accumulator will display a non-zero value. It should be noted, however, that due to the limitations imposed by the fact that the test is nondestructive, various bit errors can go undetected under certain conditions.

The software requires only 54 bytes, as shown. To conserve coding, the portion of the program commencing at the label CKSUM is used not only as a subroutine for the initial checksum but also for computing the checksum as the test proceeds. Because flag 0 is cleared before the initial call, the RETR (return with restore) instruction at location 0120 is executed. Upon return, flag 0 is set. When the program encounters CKSUM again, the JF0 (jump if flag 0 set) instruction branches around the return. Also note that RAM registers R_0–R_3 are used by the routine, and therefore are tested indirectly.

At the conclusion of the test, the routine returns to the calling program with the status of the check on the accumulator. The accumulator will contain the hexadecimal value 0FF if there is a fault in the RAM; 00 indicates the RAM is good. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

MCS-48, NONDESTRUCTIVE TEST FOR RANDOM-ACCESS MEMORIES					
Loc	**Obj**	**Source Statement**			**Comment**
0100			ORG	100H	;CAN START ANYWHERE
0100	BA01	RAMTST	MOV	R2 #01H	;INITIALIZE LOOP COUNTER/BIT MASK
0102	85		CLR	F0	;CLEAR SUBROUTINE FLAG
0103	3412		CALL	CKSUM	;COMPUTE CHECKSUM OF RAM AS IS
0105	AB		MOV	R3, A	;STORE CHECKSUM
0106	95		CPL	F0	;DISABLE CHECKSUM ROUTINE AS SUBROUTINE
0107	B83D		MOV	R0, #3DH	;SET CHECK POINTER
0109	18	BB	INC	R0	;BUMP CHECK POINTER'OVER R0-R3
010A	18		INC	R0	
010B	18		INC	R0	
010C	FA	AA	MOV	A, R2	;GET BIT MASK
010D	D0		XRL	A, @R0	;XOR BIT MASK WITH RAM DATA AT RAM POINTER
010E	A0		MOV	@R0, A	;PUT RESULT IN RAM AT RAM POINTER
010F	FA		MOV	A, R2	;GET BIT MASK AGAIN
0110	DB		XRL	A, R3	;XOR BIT MASK WITH CHECKSUM
0111	AB		MOV	R3, A	;PUT NEW CHECKSUM IN STORAGE
0112	893D	CKSUM	MOV	R1, #3DH	;CHECKSUM ROUTINE - INITIALIZE RAM POINTER
0114	27		CLR	A	;CLEAR ACC
0115	19	LOOP	INC	R1	;BUMP RAM POINTER TO NOT DO R0-R3
0116	19		INC	R1	
0117	19		INC	R1	
0118	D1		XRL	A, @R1	;XOR RAM DATA FOR CHECKSUM
0119	C9		DEC	R1	
011A	C9		DEC	R1	
011B	C9		DEC	R1	
011C	E915		DJNZ	R1, LOOP	;LOOP FOR ALL RAM EXCEPT R0-R3
011E	B621		JF0	$+3	;FLAG TEST - SUBROUTINE ONLY FIRST TIME
0120	93		RETR		;RETURN IF SUBROUTINE
0121	DB		XRL	A, R3	;COMPARE OLD/NEW CHECKSUMS
0122	C628		JZ	$+6	;IF GOOD, JUMP AROUND ERROR EXIT
0124	23FF		MOV	A, =OFFH	;COMPARE BAD - ERROR CODE TO ACC
0126	2437		JMP	FINISH	;EXIT WITH BAD ERROR CODE
0128	B5		CPL	F1	;TOGGLE FLAG TO DO EACH BIT TWICE
0129	760C		JF1	AA	;DO EACH BIT IN BOTH STATES
012B	FA		MOV	A, R2	;GET LOOP COUNT/BIT MASK
012C	E7		RL	A	;ROTATE FOR NEXT BIT POSITION
012D	AA		MOV	R2, A	;RESTORE BIT MASK
012E	07		DEC	A	;CHECK FOR CYCLE END
012F	960C		JNZ	AA	;LOOP WITH NEXT BIT MASK
0131	C8		DEC	R0	;DEC CHECK POINTER TO GET OVER R0-R3
0132	C8		DEC	R0	
0133	C8		DEC	R0	
0134	E809		DJNZ	R0, BB	;LOOP WITH NEXT DATA ADDRESS
0136	27		CLR	A	;CLEAR ACC FOR GOOD TEST
0137	83	FINISH	RET		;RETURN TO CALLING PROGRAM
					;USER PROGRAM STARTS HERE — ACC=00 GOOD TEST,
					;ACC=FF BAD TEST

Engineer's newsletter

Printed circuits enter the Iron Age

Looking for a really low-cost, low-current foil for printed-circuit boards to be used in consumer applications? A new electrodeposition process developed by Gould Laboratories has made it practical to form iron foil in thicknesses of only ⅓ to 3 mils. Iron foil is highly uniform and pore-free, glossy on one side and with a gray, textured matte finish on the other. The material bonds well, conducts electricity well, and has good magnetic shielding properties. **Most important of all, it is stronger and less expensive than most nonferrous foils used in pc fabrication.** A film pack with foil battery electrodes is another area where the low cost of iron foil could pay off. For further information, contact Timothy Wilson at Gould Laboratories–Materials Research, 540 East 105th St., Cleveland, Ohio 44108, or phone (216) 851-5500.

The op amp stars in its own video series

Despite great progress in digital circuitry, electronics is still an analog world and one of its most important elements is the operational amplifier. As **the op amp is a more complex and touchy circuit to work with than the relatively simple digital gates and latches,** Colorado State University's Engineering Renewal and Growth program is offering a three-part videotape course for engineers who want to acquire proficiency in using it.

Part 1 consists of eight 40-minute color videotapes on the frequency domain; its emphasis is on acquiring necessary tools and skills for circuit analysis. Part 2 discusses RC operational amplifiers and consists of a dozen 40-minute color tapes. Part 3 also consists of 12 40-minute color tapes and is intended to provide useful and practical knowledge of analog filter design using op amps. Each course is supplemented by a study guide and textbook. For more information, get in touch with W. L. Somervell, ERG director, Christman Field, Building 1000, Colorado State University, Fort Collins, Colo. 80523, or call (303) 491-8417.

Keeping solder from spoiling pluggable parts

If you want the option of unplugging dual in-line packages and certain other components from a printed-circuit board, you can press-fit hollow pins, called Holtite contacts, into the board's plated through-holes and plug the parts into the pins. But if components that cannot be inserted into these pins have then to be wave-soldered to the same board, you may find stray solder flowing into the backs of the pins, **making it impossible to remove the DIPs or whatever is plugged into them.**

The maker of the Holtite contacts, Augat Inc., has therefore come up with two types of soluble liquid masks that protect the pins from the solder: 322-HSM-WS is for use with rosin and organic acid fluxes; while 322-HSM-CS is for use with inorganic fluxes only. For further information, write Terry Hannan at Augat Inc., 33 Perry Ave., P. O. Box 779, Attleboro, Mass. 02703, or call him at (617) 222-2202.

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-Jerry Lyman

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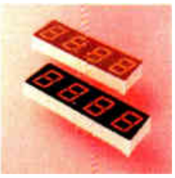

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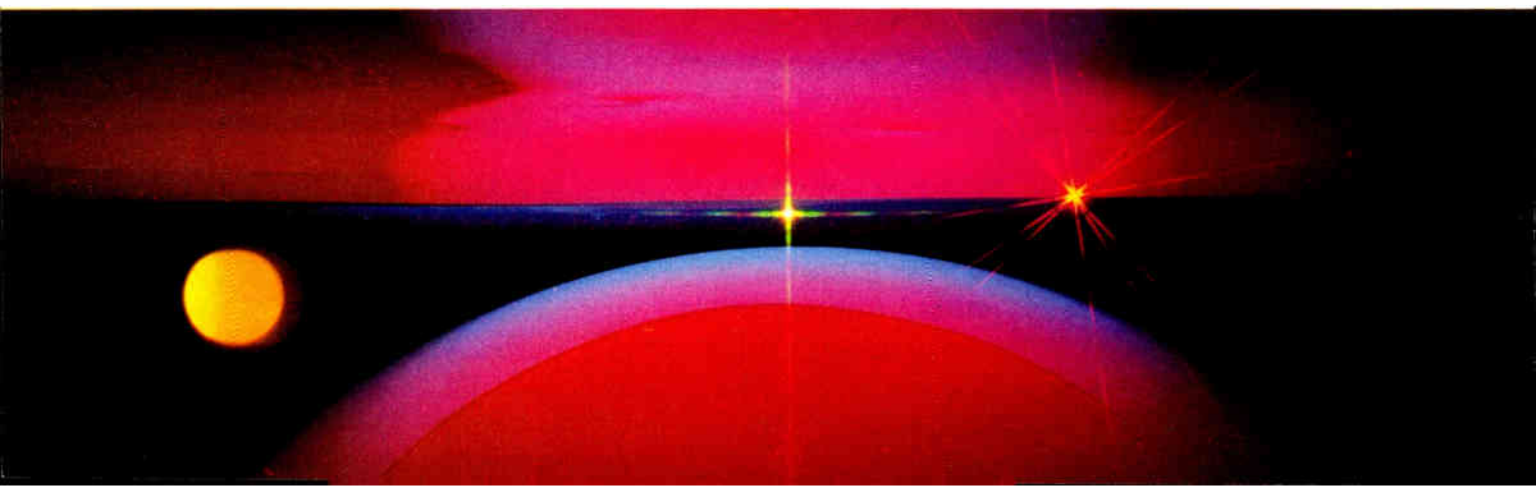


Single-board computer is fast, powerful

Z80A-based microcomputer with 16-kilobytes of RAM and a high speed math chip has 16 interrupt levels, uses CP/M2.0, and sells for $1,600

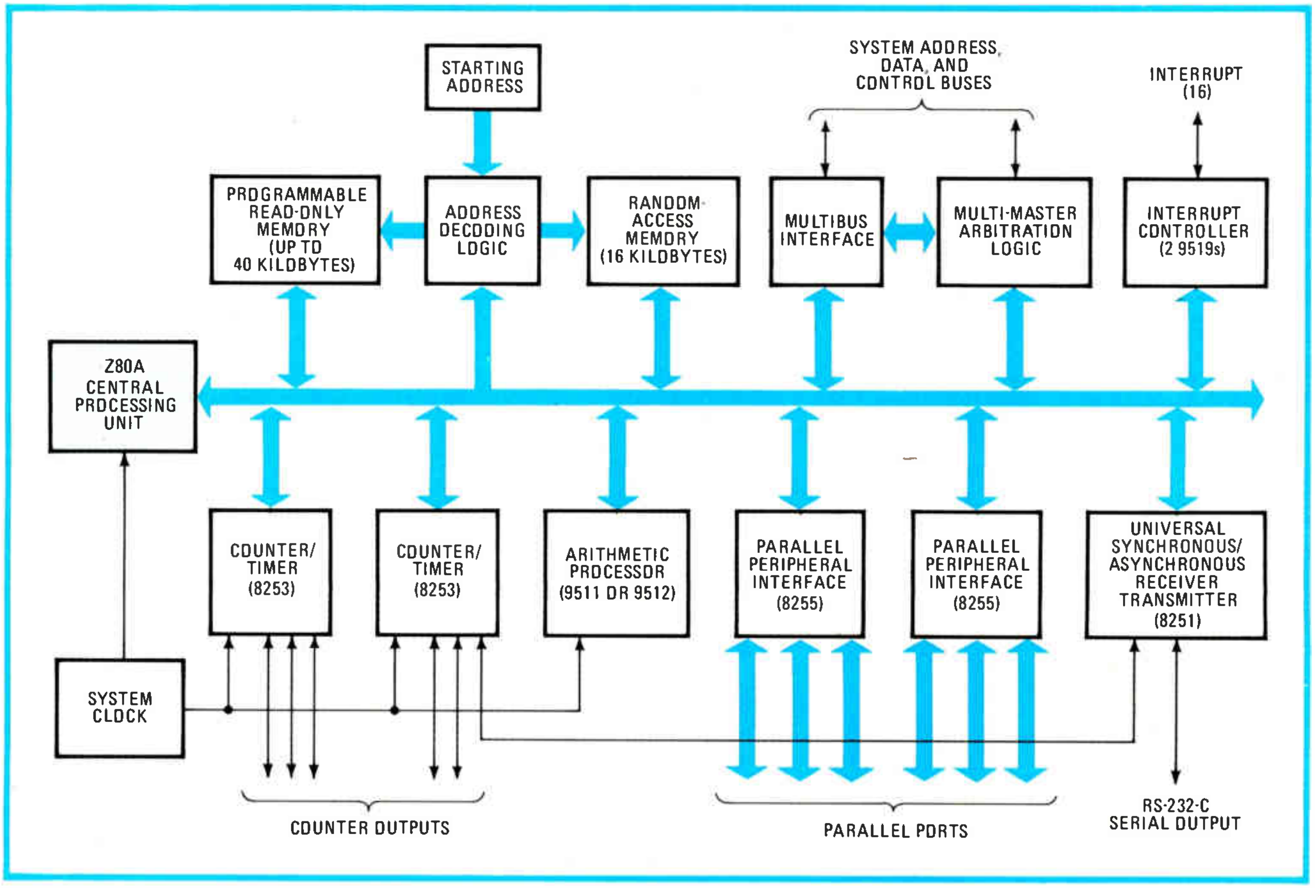
by Pamela Hamilton, Assistant New Products Editor

Video display systems are particularly demanding of their internal computers. Usually single-board units, these processors must have a lot of memory and high speed and yet add little to the cost of price-sensitive video systems. But designers at Matrox Electronic Systems Ltd., a company long in the business of making video boards, felt no single-board 8-bit computer on the market satisfied these requirements. So they set about developing the ZBC-80, a Z80A-based microcomputer board that operates at a clock rate of 4 MHz, is Multibus-compatible, has 16 levels of interrupt and lots of memory, and supports a wide variety of software packages.

Although the CPU board is a move away from video boards, marketing manager Barry Millet notes that the Montreal-headquartered company "needs vertical integration, and an 8-bit board is a logical extension of the video business." He adds that this introduction will place Matrox in a good position when the 16-kilobyte boards of the next generation become available.

The ZBC-80 provides 16 kilobytes of on-board random-access memory, with accommodation for up to 64 kilobytes when 64-kilobit chips become available. It also has sockets for up to 80 kilobytes of either read-only memory, or programmable ROM. "The on-board RAM runs without wait states," says Edward Dwyer, applications engineer. "That represents at least a 20% improvement in speed [over existing boards]," he adds.

The board uses the CP/M2.0 disk operating system from Digital Re-



search Inc. Assemblers, text editors, and debuggers as well as a number of high-level language utilities in such languages as Fortran, Cobol, Basic, and Pascal are supported by this operating system.

The ZBC-80 also offers bus arbitration logic to allow up to three masters to share the system bus in a serial priority fashion. Enhancing the Z80A's arithmetic capabilities is an optional high speed math chip, either the Am9511 or Am9512. The 9511 performs 16- or 32-bit fixed point and 32-bit floating point arithmetic. The 9512 performs 32-bit fixed point and 32- or 64-bit floating point arithmetic.

Other features of this board include: bootstrap-on-reset circuitry; six 8-bit programmable parallel I/O ports using two 8255 peripheral interface chips; six programmable timer/counters consisting of two 8253 chips; and a serial communications controller provided through an RS-232 interface and an 8251 universal synchronous/asynchronous receiver/transmitter (USART) chip. The board has an Am9519 eight-level universal interrupt controller chip as standard equipment. A second 9519 may be cascaded from the first to produce a 16-level interrupt controller that operates with fixed or rotating priorities.

Dwyer expects the company to begin shipping the CPU card in January. A fully equipped board—including an arithmetic chip, 16 levels of interrupt, two timer/counter chips, and 16 kilobytes of RAM—will sell for about $1,600 in single quantities, with the price dropping to around $1,200 in larger quantities. A stripped down version will sell for about $1,000, with larger quantities selling for $700 or less. Matrox will license the CP/M2.0 operating system for about $500.

The company also plans to offer the Mega-1, an add-on RAM card for the ZBC-80 in the first quarter of next year. The 128-kilobyte version will sell for about $2,000 and the 64-kilobyte version for about $1,000.

Matrox Electronic Systems Ltd., 5800 Andover Ave., Montreal, Quebec, H4T 1H4, Canada. Phone (514) 735-1182 [339]

Circle 155 on reader service card

Scientific computer costs $16,500

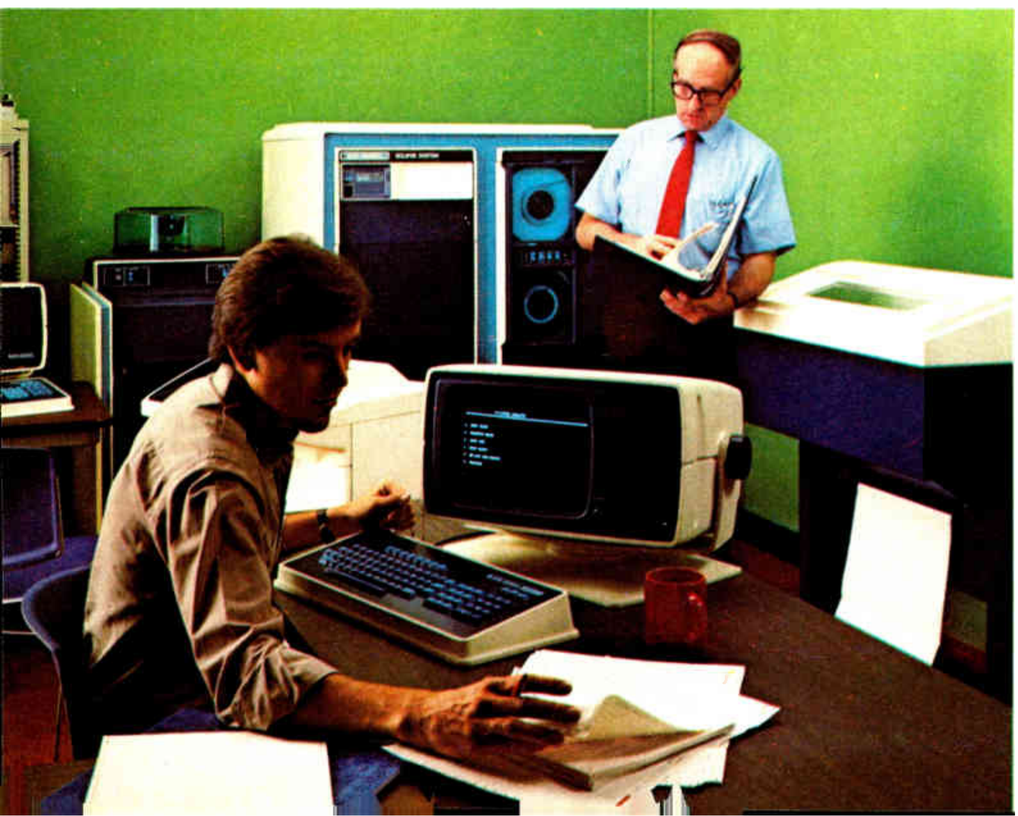
16-bit unit replaces cache memory with prefetch register, storing instructions from the four-way interleaved memory to speed cycle times

by James B. Brinton, Boston bureau manager

Price/performance ratios of scientific computers seem to improve with the introduction of every new computer. The Eclipse S/140 from Data General Corp. is the latest of such announcements [*Electronics*, Nov. 8, p. 33] with what the firm describes as an entry-level price. The S/140 is a 16-bit processor whose power falls between the company's S/130 and S/250 scientific Eclipses. But this computer's price is slightly lower than that of the 2½-year-old S/130 in similar configurations.

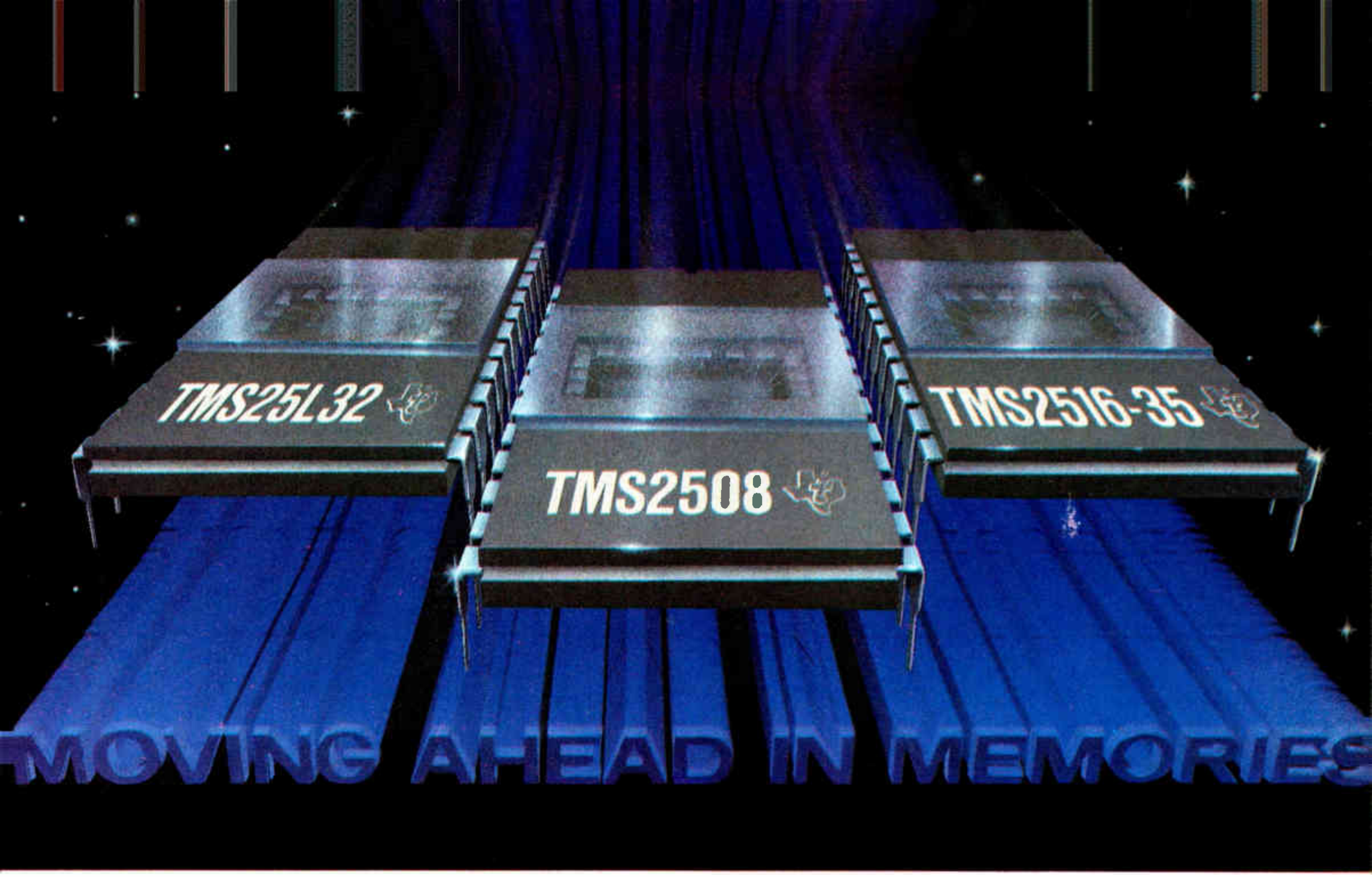
According to Richard A. Schreiber, product line manager for computational/scientific systems, "the S/140 is the nucleus of a fast, sophisticated Eclipse system that can expand economically with various system options to satisfy most high-performance 16-bit applications." The S/140 has characteristics in common with earlier Eclipse computers, but offers higher throughput than the more costly S/130, largely as a result of a combination of a microprogrammed, single-board central processing unit (CPU) with a moderately fast interleaved semiconductor main memory, in addition to what the company calls a prefetch processor (PFP) (instead of the usual Eclipse cache memory) to speed the flow of information between the CPU and memory.

Each of the S/140's memory boards uses four-way interleaving to yield an effective memory cycle time of 400 ns. The prefetch processor boosts apparent memory speed by a factor of 4 to 100 ns. The $16,500 computer comes with 128 kilobytes of MOS main memory, standard error checking and correction, real-time clock, and virtual console interface. A slower but otherwise equivalent S/130 sells for $20,500.



Data General sources are happy enough with the S/140's performance to go public with its Whetstone numbers—a standard set of Fortran tasks used as benchmarks of a computer's performance. For example, the S/140 is said to complete 450,000 Whetstone single-precision instructions per second and about 380,000 double-precision instructions per second. By contrast, the S/130 completes only about 240,000 single-precision and less than 125,000 double-precision instructions in the same time. The S/140's performance is therefore closer to the S/250's Whetstone benchmarks: more than 600,000 single-precision and more than 525,000 double-precision instructions per second.

One of the reasons for this speed is the S/140's prefetch processor. Earlier Eclipses had cache memories made of bipolar random-access memory, but according to Schreiber, the PFP offers a higher price/performance ratio than these earlier designs. The PFP is a first-in, first-out register capable of storing up to 13 instructions from the system's four-way interleaved memory and then cycling them out at a 100-ns clip, yielding an apparent fourfold memory speed increase. This is a less flexible way of "speed-buffering" memory than possible with RAM, he says, but it offers good performance and lower-cost implementation than would a RAM-based cache memory. As with other cache-like systems, one of the performance-optimizing tricks of the trade is writing the software to minimize the subroutine branching, which forces the cache



Fastest EPROM ever. Plus a low-power 32K...a faster 16K. All new from Texas Instruments.

At 250 ns max access, TI's new TMS2508 is the fastest EPROM on the market. It's made to order for state-of-the-art microprocessor systems. Reduces wait states, virtually eliminates the need for additional circuitry.

The TMS2508 is a true single 5-V supply, 8K device. Designed for speed, it provides all the outstanding characteristics of TI's 5-V EPROMs: 8-bit word configuration. Automatic chip select power down. Fully static operation. Simplified programming — singly or in blocks, sequentially or at random.

A very low power 32K also joins TI's growing EPROM family. The new 5-V TMS25L32 requires 40% less power than its standard counterpart. Active power dissipation is only 500 mW max — the lowest power per bit yet for EPROMs. Input noise immunity: 400 mV, high and low ends.

A high-performance 16K EPROM is now available from TI. The new 5-V TMS2516-35 features 350 ns max access time versus 450 ns for the standard 16K with no increase in power.

Compatible, available family: All TI EPROMs are pin compatible in rugged 24-pin dual-in-line ceramic packages. Upgrading is simple, since the family concept is designed into every new EPROM.

All offer state-of-the-art performance and all are in production.

To get the new, super fast 8K, or any other member of TI's EPROM family, call your nearest TI distributor. Or for more information, write Texas Instruments Incorporated, P. O. Box 1443, M/S 6955, Houston, Texas 77001.

TI's Growing EPROM Family

Device	Description	Power Supply	Max Power (0°C) Operating	Standby	Access Time	100-piece Price
TMS25L32	32K	5 V	500 mW	131 mW	450 ns	$102.00
TMS2532	32K	5 V	840 mW	131 mW	450 ns	53.80
TMS2516-35	16K	5 V	525 mW	131 mW	350 ns	55.40
TMS2516	16K	5 V	525 mW	131 mW	450 ns	36.92
TMS2508-25	8K	5 V	446 mW	131 mW	250 ns	36.90
TMS2508-30	8K	5 V	446 mW	131 mW	300 ns	30.80
TMS2716	16K	+12, ±5 V	720 mW	—	450 ns	24.60
TMS27L08	8K	+12, ±5 V	580 mW	—	450 ns	16.90
TMS2708	8K	+12, ±5 V	800 mW*	—	450 ns	12.30
TMS2708-35	8K	+12, ±5 V	800 mW*	—	350 ns	15.40

*T_A = 70°C

TEXAS INSTRUMENTS
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Circle 157 on reader service card

85121

memory, or PFP, to flush its contents, thus incurring a time penalty. This problem has been minimized since the S/140 is compatible with all existing Eclipse software, except for some commercial packages.

The S/140's memory expands in 128- and 256-kilobyte increments up to a total of a megabyte; Data General supports this with a memory allocation and protection (MAP) package as standard equipment. This MAP package supports privileged instructions, input/output device protection, and main memory write and validity protection in multiuser environments, which is important since the S/140 can handle up to 128 Dasher display consoles.

To speed throughput, there are two floating-point options, one designed for speed and implemented in hardware and the other for less demanding applications using a firmware implementation. The hardware unit performs a double-precision multiplication in 9.2 μs. For increased reliability, the S/140 includes automatic diagnostics to test CPU, memory, and I/O bus operation. There also is a standard automatic battery backup to provide power to a single 256-kilobyte memory module for up to 90 minutes.

Introduced at almost the same time as Data General's Xodiac, an X.25-compatible communications protocol, the S/140 is expected to play a large role in the firm's networking thrusts for the 1980s. The system's character instruction set option allows the S/140 to set itself up in business as a communications processor with bit, byte, and string instructions, including character compare, translate, move, and scan. There is an optional data-control unit that increases throughput in communications applications by acting as a front-end processor so as to offload interrupt processing, line protocols, and error control functions from the S/140's central processor.

Delivery of the S/140 takes 90 days.

Data General Corp., Route 9, Westboro, Mass. 01581. Phone (517) 366-8911 [338]

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Instruments

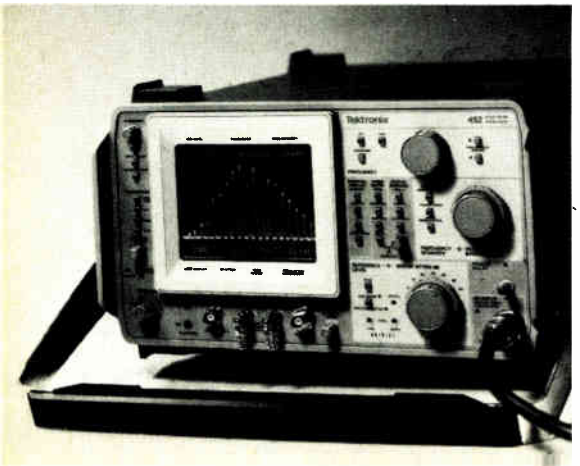
Analyzer covers 21 GHz, and more

Portable instrument offers digital storage, 100-Hz resolution

High-quality portable spectrum analyzers can range in price anywhere from $13,500 to $47,500, with the median around $20,000. Faced with that kind of expenditure, a prospetive purchaser wants to make certain that the instrument he buys is going to see a lot of service—that it earns its keep, so to speak. Tektronix' model 492 is therefore designed to spend more time on the job than resting on the shelf.

With just a set of coaxial cables, it can analyze waveforms with frequency components of 50 kHz to 21 GHz—an impressively wide bandwidth in itself. But because the range of frequencies of general interest is expanding, this instrument can work with a wide range of super and extremely high-frequency mixers, available from Hughes Aircraft Co. and TRG, among others. Using such external mixers, the 492 can display frequency components to 220 GHz.

Along with frequency components, the display contains a readout of seven key parameters—reference level, frequency, vertical display, frequency span, frequency range, resolution bandwidth, and rf attenuation—generated by the microprocessor from the control settings. The processor's presence makes it possible to add digital storage to the instrument, so it can compare a present spectrum with one previously stored, and to control operation via the general-purpose interface bus (GPIB). Both these capabilities are obtainable at the purchaser's option.



Complementing the overall bandwidth are selectable 6-dB resolution bandwidths ranging from 1 kHz to 1 MHz. But since the spectrum is getting more crowded, phase-locked stabilization and an even finer resolution of 100 Hz can be added optionally, to catch signals in densely packed bands.

Lest small signals be missed, the 492 has a dynamic range of 80 dB. Its sensitivity may be inferred from its average noise at 1-kHz resolution— −115 dBm from 50 kHz to 7.1 GHz, −100 dBm from 5.4 GHz to 18 GHz, and −95 dBm from 15 GHz to 21 GHz without optional preselection. That option increases average noise by about 5 dBm in each range, but at the same time it increases the dynamic range for harmonic measurements to 100 dB.

The model 492 weighs 44 lb—which is light for a spectrum analyzer. The single lifting handle makes it simple to carry in small spaces—it can even be passed through a submarine hatch. Further, the instrument meets the requirements of MIL-T-28800B, so it can take the rough handling instruments sometimes meet in the field.

But what are most likely to encourage field-service use are the unit's automatic features. At turn-on, it performs a self-test under microprocessor control and sets controls to a fixed set of positions each time. Autoresolution adjusts resolution to track span so that the best display is assured. An internal calibration generator eliminates the need for any additional equipment to perform a complete calibration.

In basic form, the 492 is priced at $17,850; adding the GPIB interface raises the price to $20,850. Digital storage adds $1,500 to both prices. Mixers covering the range from 18 to 60 GHz are available, and delivery time for the basic unit is 14 weeks.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077 [351]

$1,195 exerciser puts disk drives through paces

For use in both quality-assurance inspection and field-service repair, the Model FX-500 floppy disk exerciser tests floppy-disk drives by putting them through their paces and evaluating the typical problems they encounter. Drive characteristics are switch-controlled and include hard sectoring, separated or composite data and clock, single or dual heads or both, and 250-, 125-, or 500-kilobyte-per-second transfer rates for standard density.

It has a variety of modes, such as enable restore, incremental step, step to a selected track, and inhibit step. A variable step delay helps set up alignment adjustments. The FX-500 weighs 15 lb and has its own power supply. It is priced at $1,195 and delivery is 30 days.

Wilson Laboratories Inc., 2237 North Batavia St., Orange, Calif. 92665. Phone Dan Krongaard at (714) 998-1980 [357]

Simulation system generates test programs automatically

The Capable 4814 logic-simulation system is a minicomputer-based unit that analyzes software models of complex logic-circuit boards, determines a set of conditions under which the design is most likely to malfunction, and then generates programs to test for these specific faults or invalid machine states. The programs produced by the 4814 are designed to run on Computer Automation's Capable line of functional automatic test systems.

Unlike most previous systems, which used a single algorithm to select fault patterns from a table of undetected faults and then generated a stimulus sequence to drive the fault to a pin where it could be detected, the 4814 has a repertoire of four algorithms among which it switches for optimum fault detection. The system minimizes computer time by doing the easy faults first

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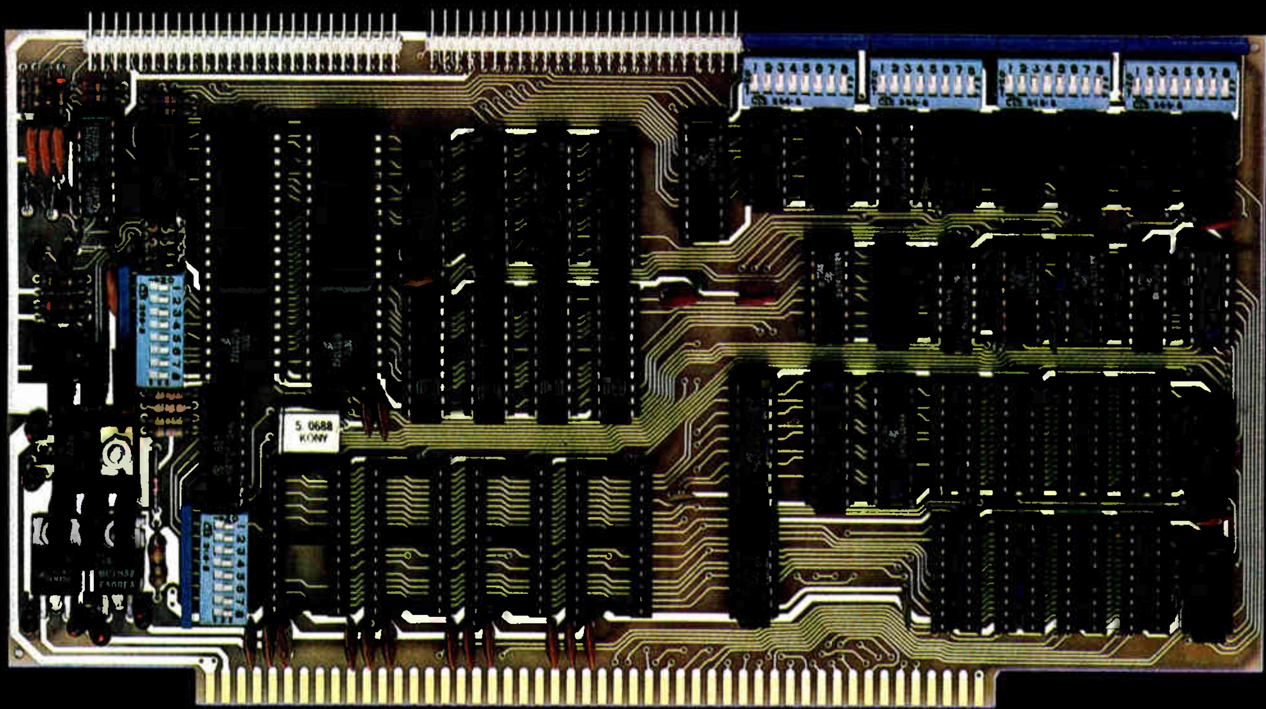
S-100 I/O INTERFACE ™



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And every port is switch-programmable for total flexibility in interfacing complex peripherals. . .such as 12-bit daisywheel printers.

Each parallel port can be switched for input or latched output. Both serial ports can be switched to any of 16 baud rates from 110 to 19,200. Each strobe and attention port flip-flop can be switched for pos or neg pulsing.

And yet, The SwitchBoard™ Interface won't hang you up on price or delivery. In kit form, it's just $199. $259 assembled. 2114 4K static RAM option (4 MHz Z-80 compatible), $70.

Ask your local computer shop to place your order immediately for priority shipping. Or, if unavailable locally, order direct from Thinker Toys™, 5221 Central Ave., Richmond, CA 94804.

Or call for The SwitchBoard™ at (415) 524-2101 weekdays, 10-5 Pacific Time.

*Sockets provided; chip set optional.

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New products

and then proceeding to the faults that are more difficult to detect.

Another factor distinguishing the new machine from most previous ones is its use of both forward and reverse propagation paths. In its optional library of data on standard circuits, the 4814 has entries that describe both types of paths; the system may thus always select the most efficient path—forward or backward—for any given fault.

A 4814 with a Naked Mini central processing unit using 320 kilobytes of memory, an alphanumeric cathode-ray-tube terminal, a 256-kilobyte floppy-disk drive, a 10-megabyte dual moving-head disk drive, the Montos operating system, the ATG-II software package, an emulation software package, and logic-simulation software and associated libraries sells for $110,000, including operator training and system installation. Delivery time is 90 days.

Computer Automation Inc., 2181 Dupont Dr., Irvine, Calif. 92713. Phone (714) 833-8830 [353]

3½-digit multimeter provides audible output

When an ohmmeter is used to test continuity, it should not be necessary to look at the instrument to get a reading. In the words of Harold Goldberg, president of Data Precision, "it is an indication and not a measurement" and can therefore be better accomplished with an audible alarm. Hence, his company's latest digital multimeter, the model 936, contains an audible alarm that goes off when the meter measures a low resistance. The alarm also sounds when the meter is subjected to an overvoltage.

Basically, the 936 is an upgraded 935. It has 29 ranges of ac and dc voltage, current, and resistance measurement; it operates from a 9-v transistor-radio battery. The 9.5-oz hand-held meter sells for $159; it is available from stock.

Data Precision Corp., Electronics Avenue, Danvers, Mass. 01923. Phone George Scott at (617) 246-1600 [358]

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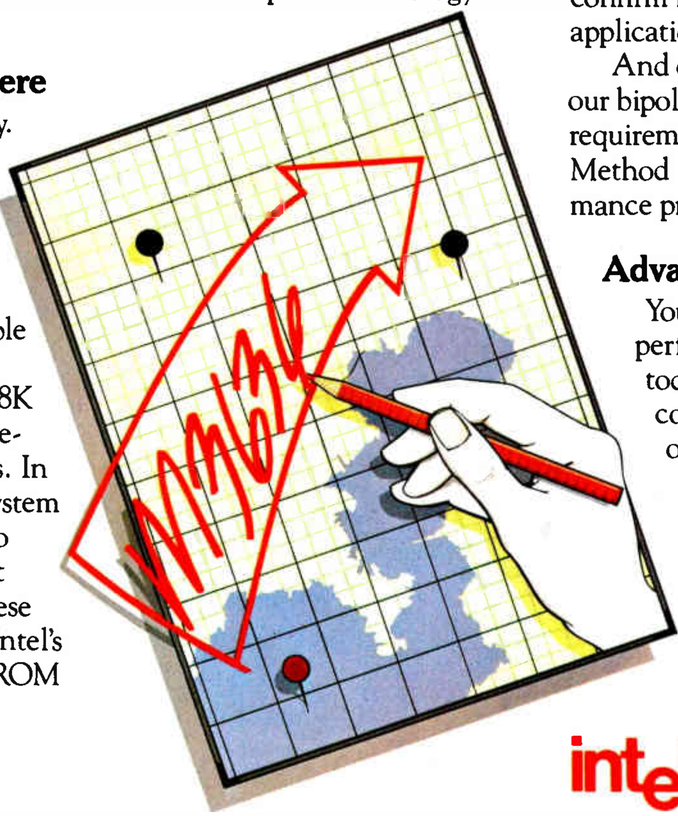
Our push for higher performance

M3636's performance advantages stem directly from a unique new bipolar process — the same we used to advance 4K designs with our M3625A bipolar PROMs. Today Intel's proven polysilicon technology combined with dual layer metalization gives you dramatically improved performance, higher density and increased programming yields.

Even more important, Intel's bipolar process means unparalleled reliability. We've already delivered thousands of memories made with this advanced bipolar technology.



Intel's Mil-Spec Bipolar PROMs

	M3636	M3624A	M3625A
Organization	2Kx8	512x8	1Kx4
Maximum Access	80ns	90ns	60ns
Package	24-pin DIP	24-pin DIP	18-pin DIP

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Millions of device hours of tests confirm its reliability for military applications.

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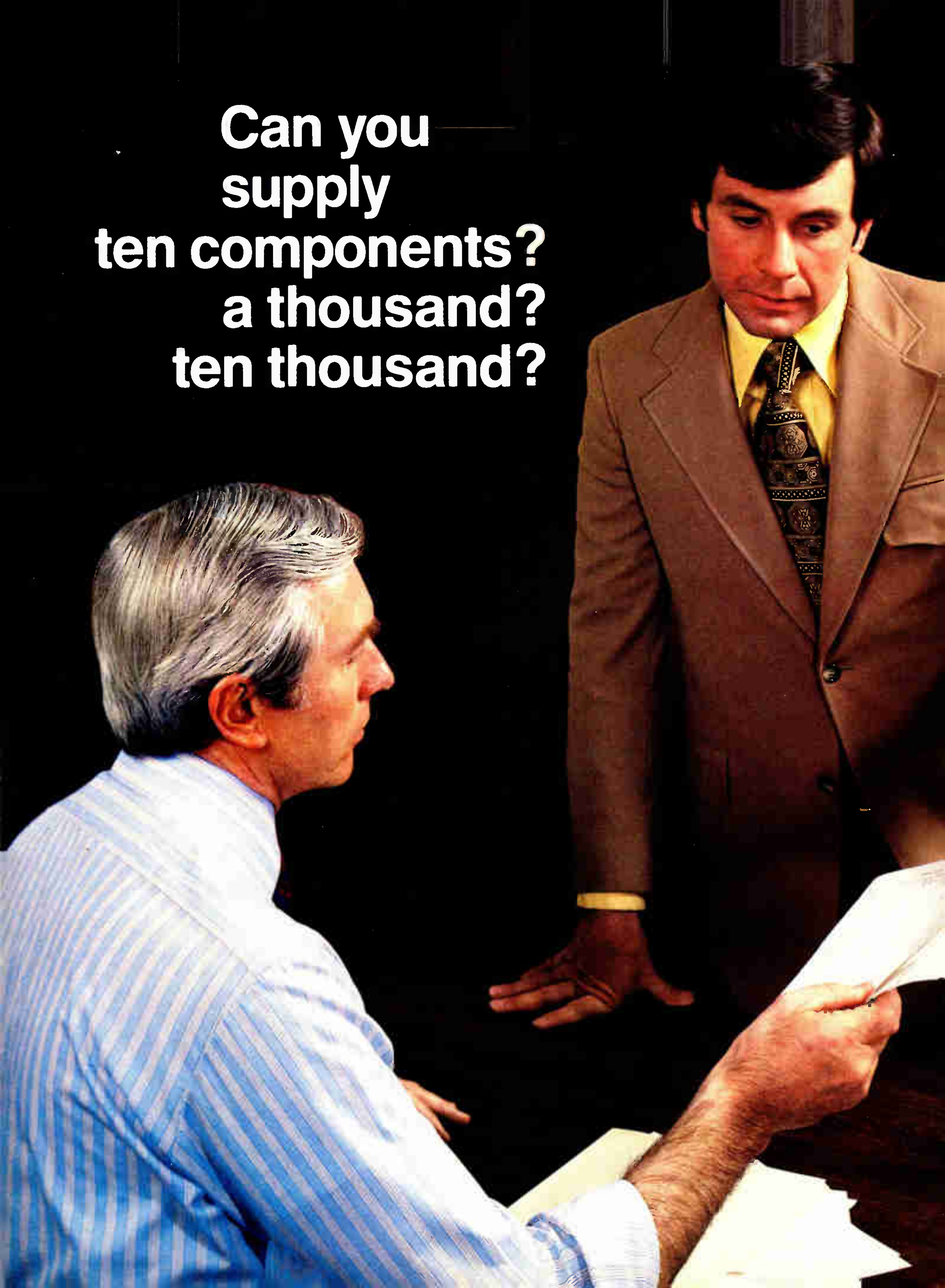
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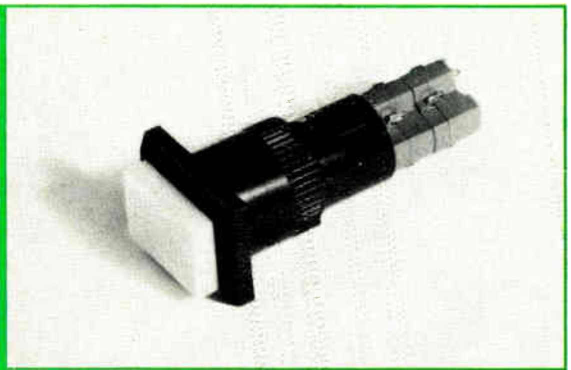

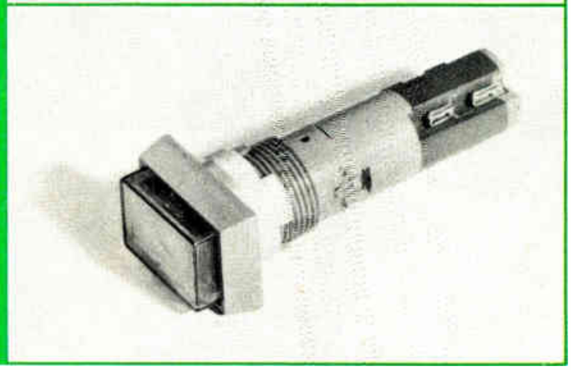

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We know that all switches are not created equal, so use your senses, beware of imitations, choose only the finest.

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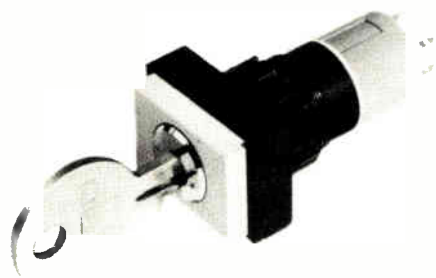

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32-K E-PROM starts as 64-K

Motorola's first-ever partial has 450-ns access time, 350-ns version due later

Considering the overall shortage of memory in today's marketplace, it's not surprising that Motorola Inc. has decided for the first time to offer a partial memory device for sale as a standard product.

Samples are available now of the MCM68732—an erasable programmable read-only memory that is made using a partially good MCM68764, Motorola's recently introduced 64-kilobit E-PROM [*Electronics*, Sept. 27, 1979, p. 176]. Introduction of the 68732 will enable Motorola to take advantage of 68764 fallout while still offering users 32 kilobits of guaranteed functional capacity.

Like its higher-density progenitor, the 68732 will be housed in a standard ROM-compatible 24-pin package, with the programming function and the chip-enable function multiplexed together on pin 20. The only difference, from a user's standpoint, between the 68764 and the 68732 relates to pin 21. On the fully good 64-K device, pin 21 is used for the extra address pin required at that density. On the partial device, pin 21 must be tied either to V_{SS} or to V_{CC}, depending upon which section of the device is functioning, explains Horst Leuschner, design engineer at Motorola's Austin, Texas, MOS operation. The 68732 devices are designated -1 or -0 accordingly.

The specs. Organized as 4-K by 8 bits, the 68732 is being offered with a 450-ns access time initially; a 350-ns version is scheduled to appear later. Typical power disipation in the active mode is 300 mW, and maximum active power disipation is specified as 880 mW. In the standby mode, these figures drop to 50 mW and 137.5 mW, respectively. Like the 68764, the 32-K partial operates on a single 5-V power supply.

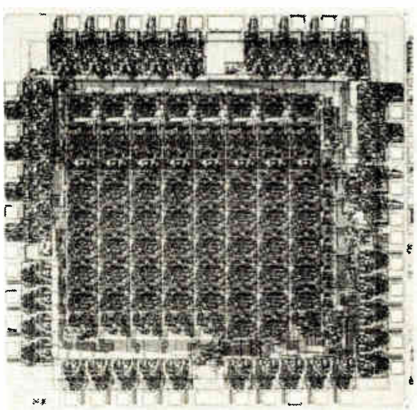
The 68732 sells for $82 in 100-unit quantities, which is exactly half of the 68764 price. Introduction of the 68732, however, will not crimp Motorola's plans to introduce a full-fledged 32-K E-PROM—the MCM2532—later this year or early next year, according to David Ford, MOS memory strategic marketing manager. At the same time, Ford says, Motorola's 64-K E-PROM yields will not be high enough, during the next 18 months at least, to preclude the sale of the 68732 partial devices. With 64-K densities, Ford feels partials are here to stay.

Motorola Semiconductor Products Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721 [411]

$70 device multiplies 8 bits by 8 bits in 45 ns

Performing a full 8-by-8-bit multiplication in 45 ns typically, the Am25S558 multiplier uses an array of full adders to form and add partial products in a single unclocked operation, resulting in a 16-bit parallel output product. The Am25S557, which will be introduced later this year, adds a 16-bit transparent latch, inserting it between the multiplier array and the three-state output buffers.

Both of these devices operate on unsigned, 2's complement, or mixed operands. Each can be expanded in either the signed or unsigned mode by offering both the most significant bit and its complement as outputs. A 16-by-16-bit configuration yields its 32-bit product typically in 110 ns.

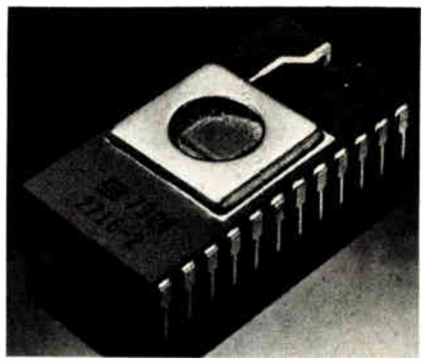


Each device is housed in a 40-pin dual in-line package, requires a single +5-V power supply, and consumes no more than 280 mA. Both military and commercial versions will be available. The price of each unit starts at $70 in 100-piece quantities.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. 94086. Phone (408) 732-2400 [413]

16-K E-PROM dissipates only 132 mW in standby mode

Operating from a single 5-V power supply and acting as a plug-in replacement for the industry-standard 16-kilobyte erasable-programmable read-only memory, the SY2716 ROM is erasable by ultraviolet light. Organized as 2,048 words by 8 bits, it is totally static and



requires no clocking. A chip-enable mode reduces power dissipation from 525 mW down to 132 mW in the standby mode.

The user programs the devices with 5-V pulses and may do so while they are actually on printed-circuit boards in a system. Each word can be written into the chip individually by means of a single-address feature. Total time for writing all 16,384 bits is less than two minutes.

Three versions of the chip, all rated from 0° to 70° C, are available. The SYC2716 has an access time of 450 ns and is priced at $38.50 each

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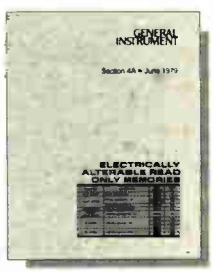
You are invited to learn more about the "just right" ER3400 and General Instrument's other EAROM products. Write or call General Instrument Microelectronics, 600 W. John St., Hicksville, NY 11802. For literature, 516-733-3107; For EAROM applications, 516-733-3192.



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in 100-unit lots. The SYC2/16-1, with an access time of 350 ns, sells for $55.00 in similar quantities. The SYC2716-2 has an access time of 390 ns, with a price tag of $42.80 (in lots of 100). Sample quantities of the units are available now, with larger quantities shipped 8 to 12 weeks after receipt of order.

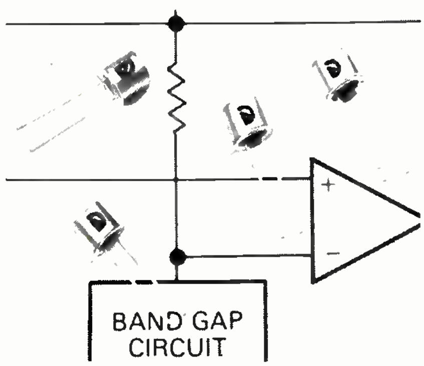
Synertek Inc., 3001 Stender Way, Santa Clara, Calif. 95051. Phone John Siemens at (408) 988-5623 [414]

Bandgap voltage reference sports 2.455-V output

Featuring a temperature coefficient as low as 30 ppm/°C, the VR-182 series of precision voltage references is made up of two-terminal monolithic bandgap devices with a 2.455-V output. An active regulator around the bandgap circuit of these devices results in a 0.1-Ω typical dynamic impedance with a 2-to-120-mA reference current range. This impedance is flat until about 4 kHz and then rises only to 1.2 Ω at 50 kHz. The devices also offer a ±1.43% voltage tolerance, 10-μV root-mean-square voltage noise, and 10 ppm/1,000 hr as a long-term stability specification.

The VR-182A has a 100 ppm/°C temperature coefficient; the VR-182B a 50 ppm/°C tempco; and the VR-182C is the 30-ppm/°C model specified earlier. The low reference voltage allows these devices to be used with 5-V logic supplies. Housed in a two-lead hermetically sealed TO-18 package, all three units will operate from 0° to 70° C.

In quantities of 1 to 24, the A



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model is priced at $2.65, the B at $3.95, and the C at $5.25, with delivery from stock to four weeks after receipt of order.

Datel/Intersil Inc., 11 Cabot Blvd., Mansfield, Mass. 02048. Phone Sumner Eagerman at (617) 339-9341, ext. 257 [417]

4- and 16-K RAMs have 55- and 120-ns access times

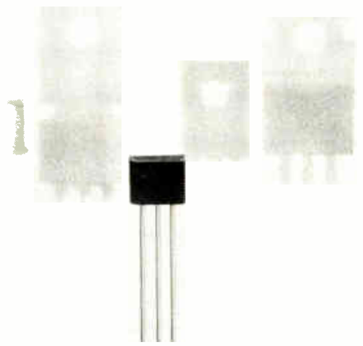
Expanding its line of high-speed, low-power complementary-MOS random-access memories, Hitachi Ltd. has developed the HM6148 series of 1-K-by-4-bit RAMs and the HM6116 series of 2-K-by-8-bit RAMs. The 6148 has an address access time of 55 ns and consumes only 150 mW during operation, or 5 μW during complete standby. The 6116 has an address access time of 120 ns and power dissipation during operation of 175 mW, or 20 μW during complete standby.

Both versions accept TTL-level inputs and produce TTL-level outputs. The 6148 has an 18-pin package compatible with the 2114 n-channel MOS static RAM. The 6116 is housed in a 24-pin package compatible with the 2716 erasable programmable read-only memory. The 6148 sells for $33 in quantities of 100 to 999, and the 6116 for $85. Deliveries begin in January.

Hitachi America Ltd., 707 West Algonquin Rd., Arlington Heights, Ill. 60005. Phone Jack Mattis at (312) 593-7660 [415]

Packed in TO-92 cases, transistors dissipate 1.5 W

The ZTX650 and ZTX750 series of power transistors dissipate 1.5 W at 25° C ambient temperature and are packaged in TO-92 cases. The 650 family of npn transistors spans the range from 45 V for the ZTX650 (the voltage represents the emitter-collector breakdown voltage) to 100 V for the ZTX653. The 651 has a breakdown rating of 60 V and the 652 one of 80 V. The ZTX750 series of pnp transistors features similar negative breakdown voltages for the 750, 751, 752, and 753. Both series of transistors will operate from −55° to +200°C and will accept a 2-A



continuous input current.

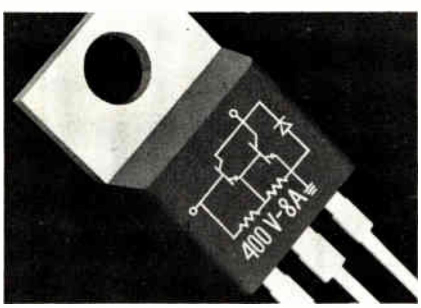
In 100-piece quantities, the 650 sells for 36¢, the 651 for 37¢, the 652 for 39¢, and the 653 for 41¢; in similar quantities, the 750 sells for 37¢, the 751 for 39¢, the 752 for 41¢, and the 753 for 44¢. Delivery is from stock to four weeks.

Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N. Y. 11725. Phone Tony Walker at (516) 543-0200 [416]

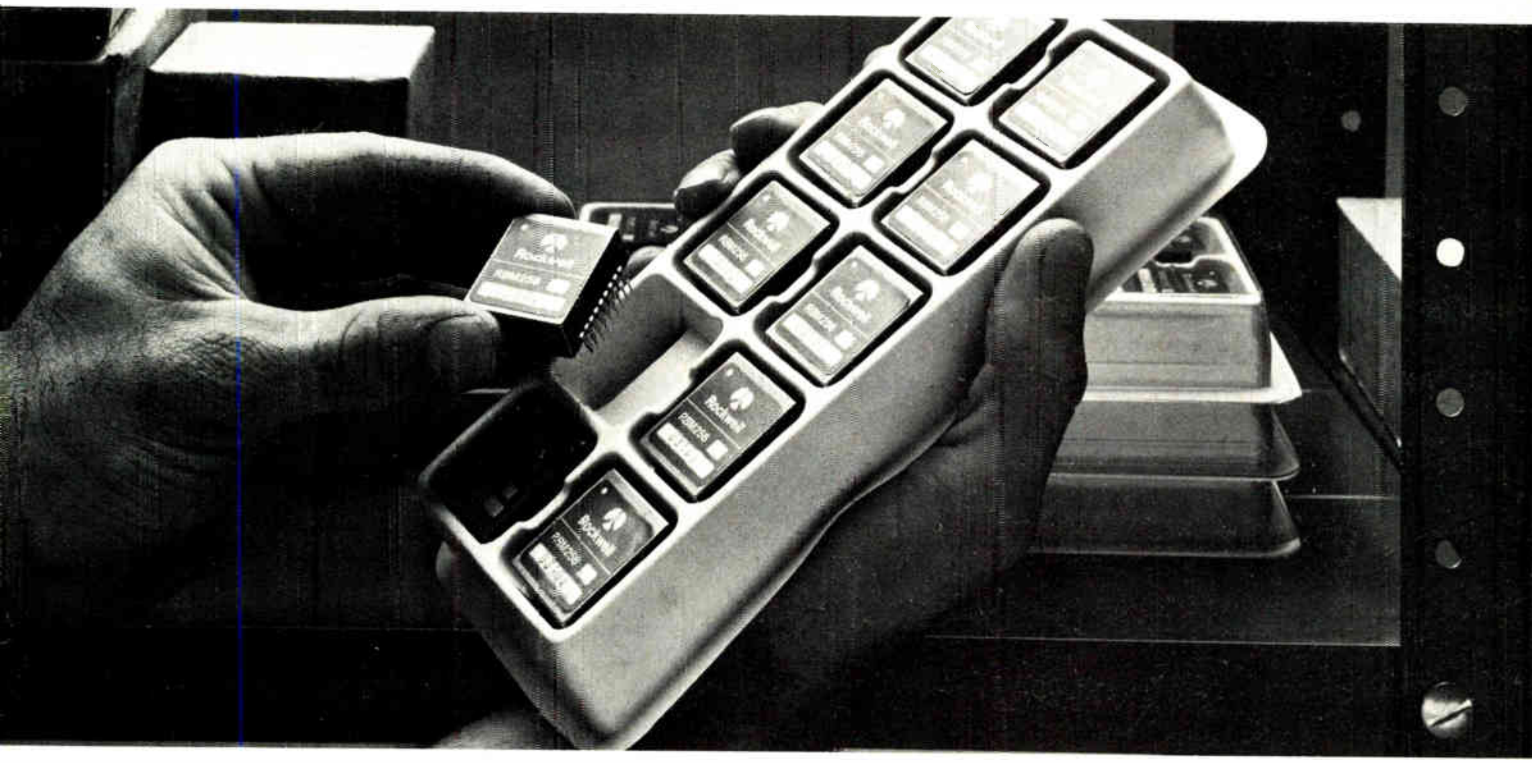
Darlington power transistors come housed in TO-220 cases

High-voltage Darlington power transistors are now available in TO-220 packages. The MJE5740, with a rating of 300 V, sells for $.99 in quantities of 100 to 999; the MJE5741 has a rating of 350 V and sells for $1.15; and the MJE5742, rated at 400 V, has a price of $1.35. Delivery on all three is from stock.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-6900 [419]



Announcing off-the-shelf Rockwell bubbles.



Rockwell 256K-bit volume-produced bubble memory devices are in distribution now.

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Rockwell International's volume production resources assure worldwide availability of its industry-standard 256K-bit devices. Second sources are already established.

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For special information write or call Bubble Memory Products Marketing, Electronic Devices Division, Rockwell International, P.O.Box 3669, D-F9 Anaheim, CA 92803, (714) 632-3321, Telex/TWX 910-591-1698.

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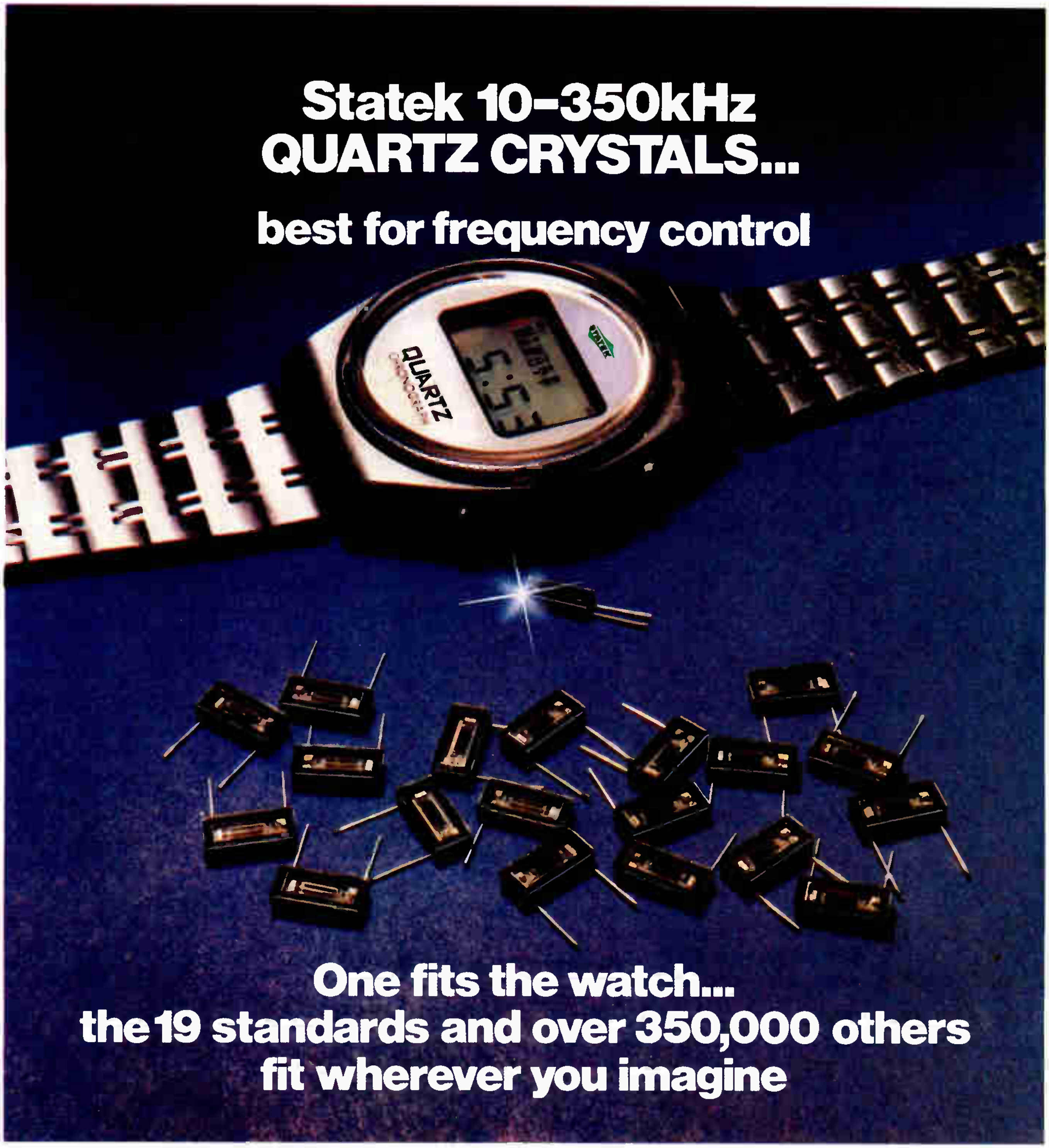

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Microcomputers & systems

LSI-11 memory has two ports

High-speed board can interface with other buses for enhanced flexibility

Unlike most add-in memories for the Digital Equipment Corp. LSI-11 microcomputer, the DSD-1 is a dual-ported board that allows both the LSI-11 bus and a second, user-specified bus (Intel's Multibus, for example) to have access to the same information. It fits into DEC's DDV11-B backplane, which is available to LSI-11 users who are building customized configurations. The unit's flexibility and a 250-ns access time make it attractive for applications such as high-speed signal processing and the refreshing of cathode-ray-tube displays.

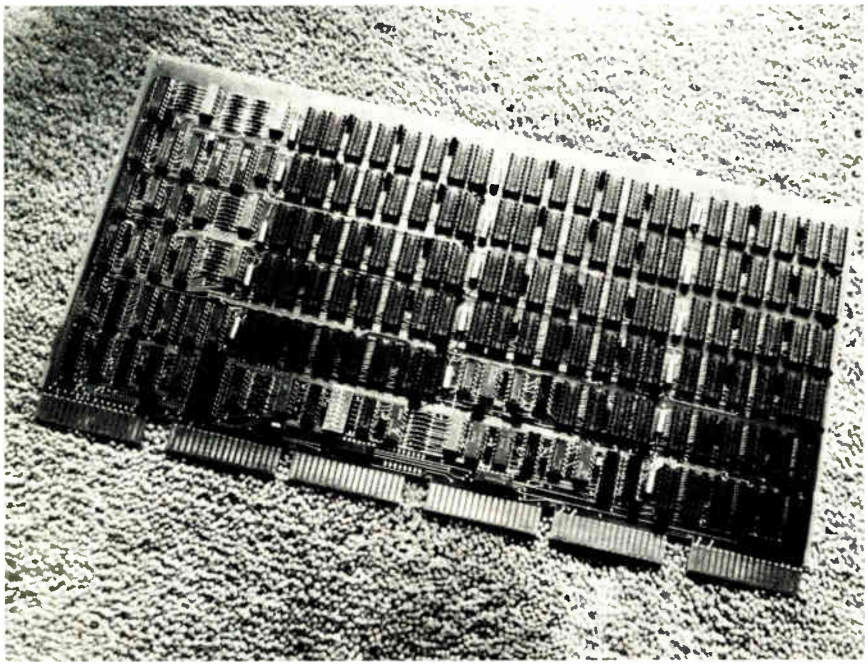
The DSD-1 has six connectors along one edge. Four are dedicated to the LSI-11 bus; the remaining two are free to be custom wired for interfacing with just about any other microcomputer bus.

The basic DSD-1 has a capacity of 4,096 16-bit words. It is expandable in 4,096-word increments to a maximum of 28-K words. Both the LSI-11 port and the "independent" port have full addressing and read/write capability. Any word on the board may be addressed identically from either port. When in the LSI-11 mode, the DSD-1 addresses both words and bytes and performs DEC-protocol bus cycles. It has the ability to support a standard DEC extended memory addressing scheme. When operating in the independent mode, it addresses words only; font memory performs word-read and word-write cycles.

Standard features of the memory board include switch-selectable page addressing, address offset, and automatic power-down.

Three DSD-1 models have typical maximum access times of 250, 350, and 500 ns. Cycle-time ranges of the three versions are 250 to 400, 350 to 500, and 500 to 650 ns. The units operate from a ±5-V supply, drawing from 16 to 27 W, depending upon memory speed. Operating temperatures range from 5° to 50°C. Prices start at $2,999 for lots of 1 to 100 units. Delivery time is 90 days after receipt of order.

DSD Laboratories Inc., 11 Dartmouth Dr., Framingham, Mass. 01701 Phone (617) 877-9076 [371]



Pascal runs on 8080, 8085 development systems

As the most recently announced high-level language to support 8080 and 8085 microprocessor software development, Pascal-80 joins its PL/M, Basic, Fortran, and iCIS-Cobol predecessors for use on Intellec microcomputer development systems. The Pascal-80 software package is available on both single- and double-sided flexible diskettes and runs under the Isis-II operating system on diskette-based Intellec series II and MDS-800 development systems.

A superset of the standard Pascal, Pascal-80 offers extensions to make the language more suitable for commercial and industrial applications. These extensions include three new data types: the string type, untyped files, and interactive files, as well as 28 predeclared procedures and functions; the programmer does not have to designate frequently used procedures and functions on an individual basis.

This software package includes a diskette containing a compiler, a pseudocode (p-code) interpreter, demonstration programs, a Pascal-80 user manual, and the second edition of the standard Pascal Text, "Pascal User Manual and Report," by Jensen and Wirth. Ordered under the product code MDS-381, the software package sells for $975 and is available now. The Pascal-80 software was developed under license to Queue Computer Corp., Berkeley, Calif.

Intel Corp., 3065 Bowers Ave., Santa Clara, Calif., 95051. Phone Dan Shafer at (415) 987-5020 [372]

Cross-compiler generates relocatable programs

PLM/S86, a superset of Intel's PL/M86, is a high-performance cross-compiler designed to meet the needs of users who are generating relocatable programs that take ad-

vantage of the megabyte address space provided by the new generation of 16-bit microprocessors. This cross-compiler will work with any large machine that supports PL/1 and has the ability to edit, compile, and debug syntactically a source program. PLM/S86 has extensive capabilities for error detection, as well as diagnostic work to aid the programmer in syntactic debugging. The cross-compiler has the added ability to download an object program for debugging to a development system for execution by an 8086 microprocessor.

A stand-alone license for the PLM/S86 will be about $30,000. The cross-compiler is scheduled for availability in January on the National CSS timesharing network.

SLR Compilers Inc., 1109 20th St., Suite 6, Santa Monica, Calif. 90403. Phone (213) 394-6800 [374]

Emulator terminal allows host computer to act as MDS

When connected to a host computer, the Microsystem Emulator series 2000 terminal allows the host to serve as a microprocessor development system. Microprocessors that may be emulated by the terminal include the 6800, the 6802, the 8048, the 8080, the 8085A, and the Z80A.

The 2000 may also be used as a terminal with dedicated microprocessor development systems from Intel, Motorola, and Zilog.

Operating at speeds up to 6 MHz, the terminal allows real-time emulation of the faster microprocessors. Real-time operation of the unit extends to an optional real-time trace capability, a debugging aid permitting the user to track the step-by-step performance of his design at full-rated speed. Real-time trace capabilities also offer a record of the 128 most recent operations to have been made so that program faults are uncovered quickly. Full software debugging capabilities offer 8 kilobytes of random-access memory. With this large amount of memory on board, the user is able to down-

load programs from the computer for execution in the emulator terminals.

The terminal also features direct-memory-access operation for use with the Z80A and 8085 microprocessors. Also offered is a high-speed serial data link. The emulator is priced at $4,500 with emulator cards for each of the microprocessors ranging from $1,000 to $1,500.

Millennium Systems Inc., 19020 Pruneridge Ave., Cupertino, Calif. 95014. Phone Martin Weisberg at (408) 996-9109 [373]

8086 macroassembler and editor require little RAM

The RA8086, a two-pass resident macroassembler, provides full assembly power for the 8086 microprocessor. Producing a listing, a sorted symbol table, and object code, all of which may be loaded with the Intel monitor for the 8086, the RA8086 uses standard Intel mnemonics and a full set of pseudo-operations. Requiring only 16 kilobytes of random-access memory and an automatic send-receive teletypewriter, the assembler features: fast execution through the use of a hash-code symbol table and a binary search of the mnemonic table; nested macros with up to 10 parameters; a conditional assembly with up to 10 nested levels; and I/O drivers that may be modified by the user.

A resident line-oriented context editor for the 8086, the Edit86 provides for the creation and editing of program and data files. It contains a wide set of editing and file manipulation commands and requires only 2.5 kilobytes of RAM for the code, and an ASR teletypewriter. A complete source listing is supplied to permit the user to customize the editor to available hardware.

Available as off-the-shelf items and including a user manual, source listings, and a paper-tape object code, the RA8086 sells for $249.95 and the Edit86 for $149.95.

Hemenway Associates Inc., 101 Tremont St., Suite 208, Boston, Mass. 02108. Phone (617) 426-1931 [377]

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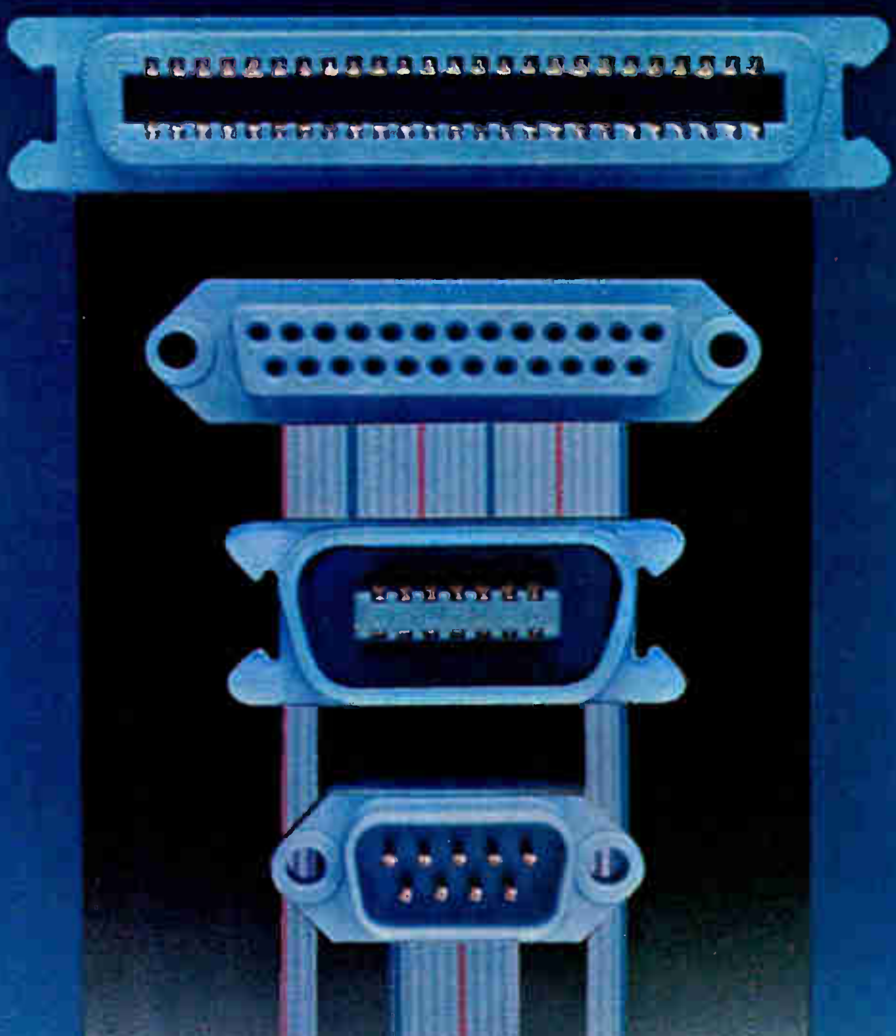

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Converter accepts BCD inputs

Monolithic digital-to-analog unit settles to within 1/2 LSB in 85 ns, sells for $2.95

Binary-coded decimal, a popular digital format in many instruments, presents a minor but persistent problem whenever the instruments' outputs must be converted into analog form, be it within the instruments or external to them. The problem is that the BCD signal must usually be converted to binary form because there are few inexpensive digital-to-analog converters on the market that will accept a BCD input. And of these few d-t-a converters that are available, none have been monolithic devices.

At least none were until very recently. The model DAC-20 from Precision Monolithics is a one-chip, two-digit, BCD-input device that sells for $2.95 each in quantities of 100 units or more. The converter has complementary current outputs, which settle to within half a least significant bit in 85 ns and allow the converter to be used with both positive-true and negative-true logic systems. Linearity error is no more than half a least significant bit for the standard version, but a premium unit, priced at $3.95, is rated at 1/4 LSB maximum nonlinearity. The unit can be expanded to handle up to 2½ digits, by use of external gates.

The converter may be operated from unipolar or bipolar supplies: the requirement is that the more-positive supply be more than 10 V and less than 36 V above the more negative one. The current-output converter has an output compliance voltage that can swing up to the more positive rail and down to within 8 V of the lower rail. When operated from ±5 V, the converter typically consumes 37 mW.

In a typical application, the DAC-20 forms the interface between an instrument's BCD output and an analog display element. Its actual analog output current is determined by both the BCD input and the magnitude of its input reference current.

The DAC-20 BCD-input d-a converter comes in a 16-pin plastic package. It is available now.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 246-9222 [381]

Computer-controlled a-d converter resolves 12 bits

The RAD1 analog-to-digital converter is a four-channel module designed for use in computer-controlled remote data acquisition and control. The module, which is fully supported with Fortran calls, features differential inputs, 14-bit resolution, and a maximum nonlinearity of half of a least significant bit. It may be installed at the signal source, up to 250 feet from the computer. The module has a conversion time of 20 μs, a transfer interval of 5 μs, a channel-change time of 10 μs, and an acquisition time of 6 μs. It can communicate with the computer at 4 MHz.

The fixed-gain model RAD1.A2 sells for $975. A variable-gain unit with a built-in 14-bit digital-to-analog converter, the model RAD1.A1, is priced at $1,450. Both are available from stock to eight weeks.

Precision Data Systems, 2030 North Forbes, Tucson, Ariz. 85705. Phone Donald Trumbo at (602) 882-8906 [385]

16-bit d-a converters sell for $72.50

The DAC-HP16BGC and the DAC-HP16DGC are high-resolution voltage-output digital-to-analog converters that sell for only $72.50. The maker suggests such applications as speech and waveform reconstruction, precision ramp generators, and com-

puter-controlled testing. The low cost is partly due to epoxy sealing. The converters offer a gain temperature coefficient of ±20 ppm/°C and a settling time of 15 μs to within 0.005% of the final value. The DAC-HP16B has 16-bit binary resolution linear to within ±0.003% of full scale, whereas the DAC-HP16D has 4-digit binary-coded decimal resolution with ±0.005% nonlinearity. Input coding is complementary binary and complementry offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10 V and ±5 V; the BCD version operates in unipolar mode only, with 0- to +10-V output.

The DAC-HP design uses thin-film hybrid technology. Selected Nichrome-on-silicon thin-film resistor networks are combined with matched quad current switches for 16-bit resolution. The thin-film resistors are functionally laser-trimmed and are available in an operating temperature range of 0° to 70°C. Delivery time is 10 to 12 weeks after the order is received.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone Sumner Eagerman at (617) 339-9341 [383]

Small synchro-to-digital modules track at 36,000°/s

Designed for printed-circuit-board mounting, a series of 10-bit synchro-to-digital converter modules can track input rates as high as 36,000°/s with no added error. Operating in the 50-to-400-Hz frequency range—with no external transformers needed—the modules measure 2.6 by 3.1 by 0.42 in. They will convert either synchro or resolver inputs of 11.8 V or 90 V at 400 Hz or 90 V at 50 Hz or 60 Hz into a 10-bit parallel binary output to represent an angle measurement, with an accuracy of ±30 minutes of arc.

The digital outputs are TTL- and complementary-MOS-compatible; bidirectional input data is accepted.

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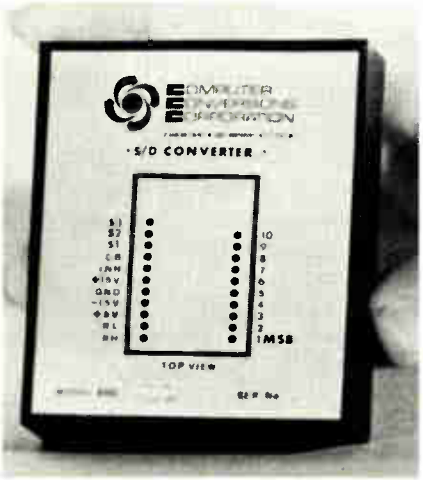
boschert SWITCHING POWER SUPPLIES

New products



The converters consume 500 mw of power and provide complete synchronization to a computer. The units operate over the temperature range of 0° to 70° C or −55° to +105° C. They are priced at $199 each, with delivery within four weeks.

Computer Conversions Corp., 6 Dunton Court, East Northport, N. Y. 11731. Phone (516) 261-3300 [386]

High-speed IC comparator fits 12-bit a-d converters

The 40-ns response time of the HA-4950 comparator makes it the only high-speed, high-precision, strobed integrated-circuit comparator that is compatible with 12-bit analog-to-digital conversion applications, says the manufacturer. The unit's maximum total input uncertainty is ±150 μV; its input offset voltage is 0.3 mV, and it has TTL-compatible strobed outputs. The ±150-μV uncertainty translates into an error of less than ⅛ least significant bit in 12-bit a-d conversion systems using a 10-V reference.

Besides being used in successive-approximation a-d converters, the comparator can be used for high-resolution comparisons in servo-positioning systems and other feedback control loops; in precision zero-crossing detectors for applications that require null-state detection; and in high-speed, high-accuracy measurement applications such as determining the settling times of fast amplifiers and high-speed d-a converters. The HA-4950 comes in a 14-pin ceramic dual in-line package in two temperature ranges: a high-reliability MIL-STD-883 wide-temperature-range version, the HA-4950-8, and the −55° to +70°C HA-4950-2. At $9.50 for a quantity of 100 or more, the latter are available for immediate delivery.

Harris Semiconductor Group, P. O. Box 883, Melbourne, Fla. 32901. Call Ron C. Pittenger at (305) 724-7407 [387]

8-bit analog-to-digital converters ride 8080 bus

The 20-pin dual-in-line-packaged ADC0801, 0802, 0803, and 0804 are complementary-MOS, 8-bit successive-approximation analog-to-digital converters requiring no external interface logic to operate with microprocessors. Using a modified potentiometric ladder similar to the standard 256R approach, these converters are configured to allow operation with the standard control bus of the 8080 microprocessors; they appear as memory locations or input/output ports to the microprocessor. Three-state output latches directly drive the data bus.

The units also feature: a differen-

New products

tial analog voltage input, an adjustable voltage reference; TTL-level inputs and outputs; an on-chip clock generator; and a 0-to-5-V power supply. The units have a conversion time of 100 µs, with a clock range of 100 kHz to 1.28 MHz. Available from stock, the units have prices starting at $2.95 (for the 0804), in hundreds.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Dave Whetstone at (408) 737-5856 [390]

Data-acquisition system has up to 1,000 channels

The Datalogger 2000 Basic System provides 40-channel internal capability—expandable to 1,000—with a 20-channel scan card and a signal-conditioning module. The 2000 offers microprocessing functions like signal processing, formatting, alarm assignment (up to 1,200 individually assignable alarms), and interfacing. It measures up to four mixed parameters selected from the temperature, dc voltage, dc auto-ranging, ac voltage, true rms, and transmitter output. It displays and records time and date, number, measured data and parameter symbols with the printout of English messages that identify alarm status without look-up tables.

The Datalogger 2000 offers skip channel capability and a ±25,000-count display of the data measured. The basic system is priced at $3,195, and delivery is from four to six weeks.

United Systems Corp., 918 Woodley Rd., Dayton, Ohio 45403. Contact Gary Day at (513) 254-6251 [388]

THE EXPERIENCE OF THE FEDERAL RESERVE WITH

DATA TRANSMISSION

Today, computers at the Federal Reserve transmit data, over a Bell System network, at 240,000 characters per minute.

Bell was chosen for this high-speed data transmission system because of the magnitude of the Fed's requirements—and because of Bell's technical capabilities. Bob Dunlap, Bell System National Account Manager, worked closely with the Fed to meet their special needs.

Mr. Dunlap explains: "This system eliminates flying computer tapes from one Federal Reserve bank to another. No more delays, no more getting fogged in. Banking transactions speed up.

"The Fed does a lot of payroll data transmission over the system," Mr. Dunlap explains. "This gets payrolls distributed on time, eliminates theft of checks from mail boxes, provides better service to banks and the larger commercial community. And," he concludes, "it helps arrest the staggering growth of checks."

If your agency is interested in data transmission, talk to your Bell System Account Executive. He/she can bring Bell expertise to your problem, and is the point of contact that opens the resources of the Bell System to your needs.

Bell System

Circle 193 on reader service card

Seven Reasons Why Perkin-Elmer Computer Users Prefer MDB Interface Products:

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PERIPHERAL DEVICE CONTROLLERS

MDB-46-206 Line Printer Controller; long line capability available
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MDB-46-234 Hollerith to ASC11 Converter

SYSTEMS MODULES

MDB-48-000 Universal Clock Module with line frequency clock
MDB-48-012 Line Frequency Clock Module
New! MDB-48-488 IEEE Instrumentation Bus Controller

COMMUNICATIONS/TERMINAL MODULES

New! MDB-47-102 Programmable Asynchronous Single Line Adapter (PASLA), single channel
MDB-47-102D Dual PASLA, two channels on a half-board, includes current loop; RS422 long line optional
MDB-48-024 Current Loop/RS232 Interface

GENERAL PURPOSE INTERFACE MODULES

MDB-48-002 General Purpose Interface Board, provides 197 user IC positions, accepts all sizes DIP packages; wire wrap pins and/or lo-profile sockets optional
New! MDB-48-002H General Purpose Interface Half-Board, provides for 91 user IC positions, wire wrap pins and/or lo-profile sockets optional
MDB-48-013 Universal Logic Module, basic 16-bit I/O board; options include second device controller, two output register options; wire wrap pins and/or lo-profile sockets for 92 positions of user IC logic
New! MDB-48-013H Universal Logic Half-Board; same, with 42 user IC logic positions

ACCESSORY HARDWARE

New! MDB-16-398 Half-Board Mounting Kit
MDB-ULLAB-01, 02 Universal RS232 Long Line Adapter Box, six or twelve RS422 differential long line receivers/drivers converted to RS232
MDB-ULLAB-03 Universal TTL Long Line Adapter Box, twelve RS422 differential long line receivers/drivers converted to drivers/receivers
GPIO Cable Subassemblies for 20, 26, 34, 40 and 50 conductor ribbon cable; connector with 10 foot unterminated cable

MDB interface products always equal or exceed the host computer manufacturer's specifications and performance for a similar product. MDB interfaces are completely hardware compatible and software transparent to the host computer. MDB products are competitively priced, delivery is 30 days ARO or sooner. MDB places an unconditional one-year warranty on its controllers and tested products.

MDB also supplies similar interface modules for DEC PDP*-11 and LSI*-11, Data General,** and IBM Series/1 computers. Product literature kits are complete with data sheets, pricing and discount schedules.

*TM Digital Equipment Corp. **Data General is a computer manufacturer unrelated to MDB

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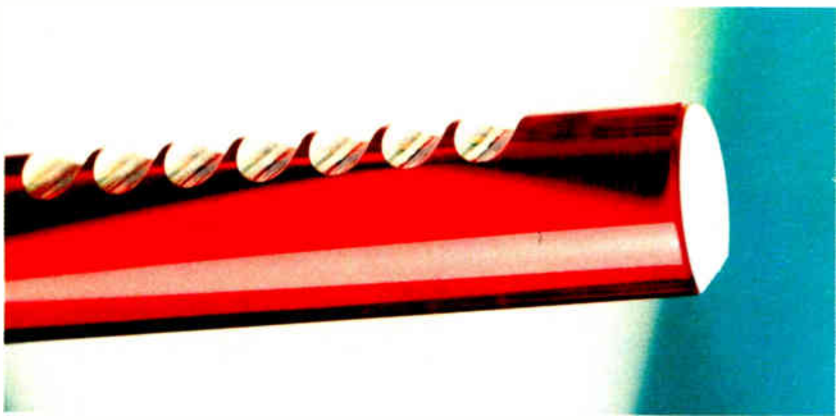
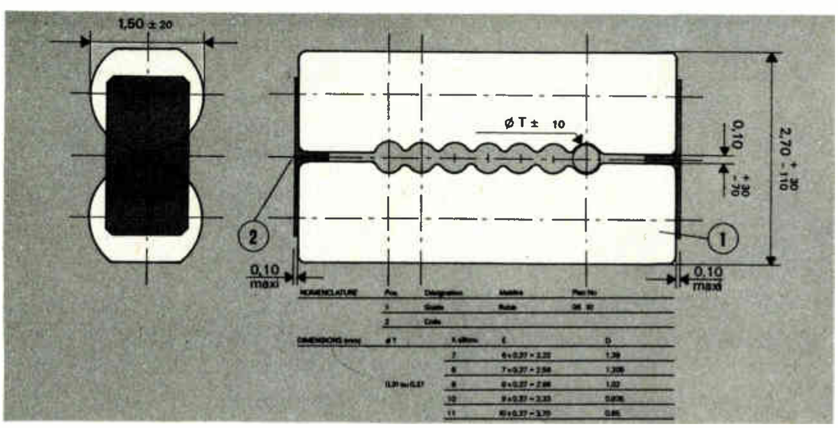
Circle 107 for P-E; 108 for PDP; 109 for LSI; 110 for DG; 194 for IBM.

New product, lower cost

Seitz

Seitz, c'est sûr !





Wire-guide bars for printing heads

All kinds of material have been tried out for the manufacture of wire-guide bars. The corundum in single crystal structure ($Al^2 O^3$) still remains the best one. Seitz knows it and uses it in an economic and intelligent way.
The form: a cylindrical bar, which means reduction of friction, improvement of the ribbon guiding, elimination of the wear of the head.
Application: in every type of head, thanks to the rigorously respected dimensions and tolerances.
Seitz is the pioneer of wire-guides and is furthermore the most important manufacturer of this product. Seitz has created and fixed its norms.
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Téléphone 032 / 22 65 11, Télex 34 566

Products newsletter

Printer company unveils innovative typewriter technology

In what appears to be a technology first, Centronics Data Computer Corp., Hudson, N. H., has introduced a new electronic typewriter technology—a low-cost, unlimited-font, hard-copy output technique aimed at the office environment. **The system uses a stylus controlled by miniature solenoids in the X, Y, and Z axes to press on, and through, a carbon typewriter ribbon.** Thus, while it writes silently like non-impact printers, unlike them, it can make multiple copies. The print rate varies with font size and complexity, but is said to be well within 15 to 20 characters per second. This approach also offers the ability to print in any programmed font—including cursive script simulating handwriting.

Nippon Electric expands with 8-bit microcomputer

Nippon Electric Co. is expanding its μPD line of processor chips and has designed an 8-bit microcomputer called the 7801. The chip will soon be available in the U. S. through NEC Microcomputers Inc., Wellesley, Mass. **Not only does the device have large amounts of internal memory, but it can also address external memories and 8080-compatible peripheral chips, which is made possible because of the device's 64-pin package.** The 7801 has its own instruction set, optimized for code efficiency.

Automatic prober will load, align 6-in. wafers

Look for Teledyne TAC, Woburn, Mass., to begin marketing an automatic wafer prober in the first half of next year. **The Mark 710 will have automatic wafer loading, alignment, and thickness compensation and will handle wafers up to 150 mm (6 in.) in diameter.** A CRT display will be available for feeding in instructions and diagnostic work. The microprocessor-based machine resembles a direct step-and-repeat lithography system using optical encoders. With its 10-in./s table speed, this system should greatly speed up throughput at wafer-probing positions.

AEG-Telefunken poised to penetrate U. S. power-device market

Ready to penetrate the lucrative market for high-power semiconductor devices, AEG-Telefunken's Power Engineering and Industrial Systems division, Route 22, Somerville, N. J., will shortly introduce several high-current, high-voltage diodes and thyristors. **Included will be a Hockey Puk diode capable of handling 3,500 A at 3,200 V, and an interdigitated gate-assisted turn-off thryistor with a 1,200-V rating and a rapid turn-off time of less than 10 μs.** Another device includes a silicon controlled rectifier with a 1,000-A rating at 85°C (2,500 A at room temperature), and a voltage rating of approximately 2 kV.

Siliconix drops price of V-groove MOS power devices

Perhaps signaling a trend, Siliconix Inc., Santa Clara, Calif., is immediately reducing the price on several of their V-groove MOS power field-effect transistor devices. **For example, the price of the VN64GA, an n-channel enhancement-mode V-MOS power FET designed for motor controllers and switching power supplies, is being slashed by 50%.** The device, which has a maximum continuous drain current of 12.5 A and a maximum drain-source on-resistance of 0.4 Ω, will now list for $6.88 in 1,000-piece quantities.

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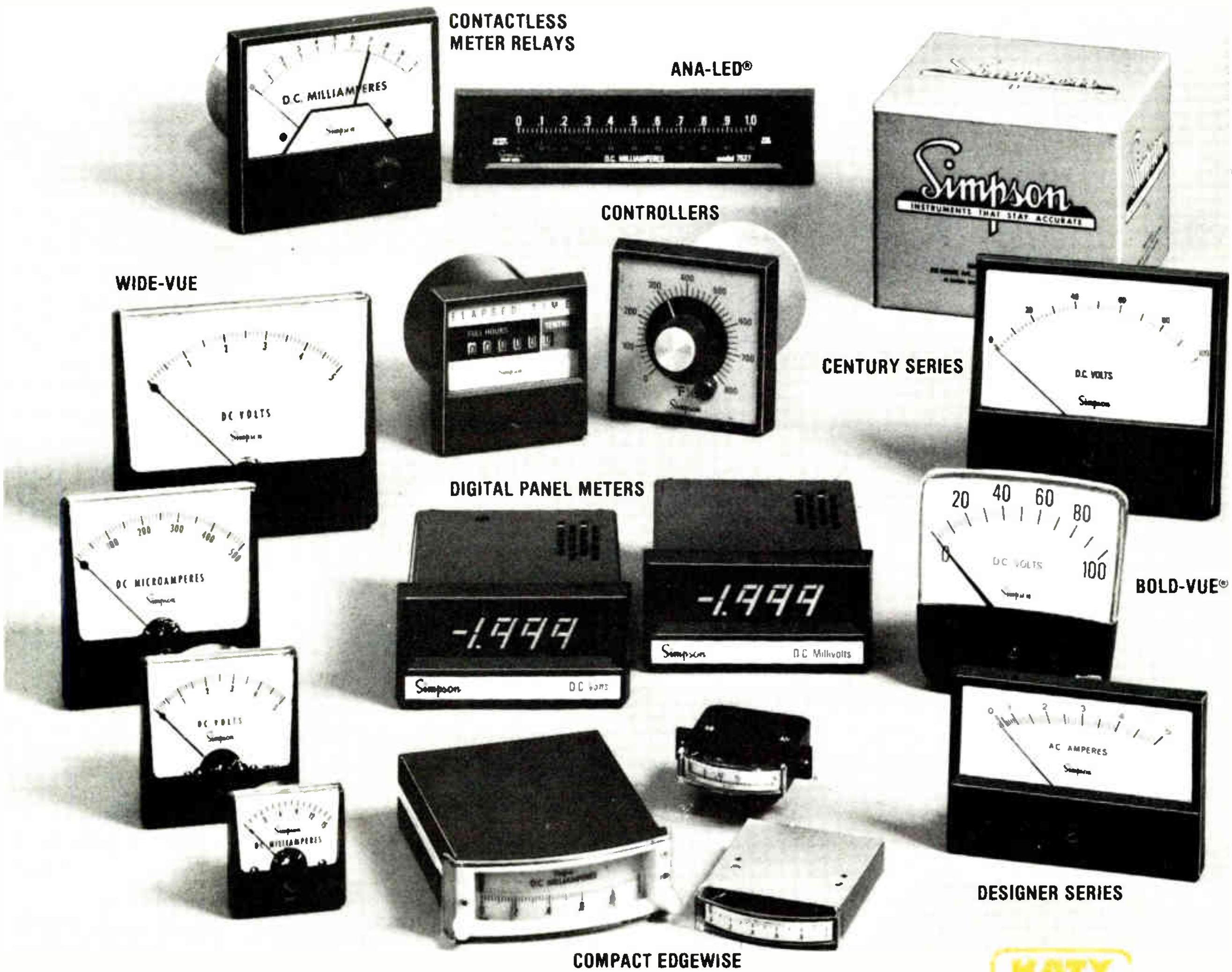

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Don't wait till there's trouble with your system before you give us a call about our ML422A and our complete line of communications test and measuring equipment. It can mean a savings in time that can make a difference in profit.

Frequency range	200Hz to 30MHz
Level measuring range	−120 to +30dBm
Level measuring accuracy	±0.1dB (10kHz to 13MHz, −80 to 0dBm)
Frequency stability	$\leqq 1\times10^{-5}$ (0 to 45°C)
Input impedance	75Ω, 135Ω, 150Ω, 600Ω (High)
Bandwidth	40Hz, 1.74kHz
Dimension/Weight	195(H)×426(W)×350(D)mm/ $\leqq$16kg

For comprehensive literature on the Selective Level Meter ML422A, contact—

Anritsu

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Circle 202 on reader service card

New products/materials

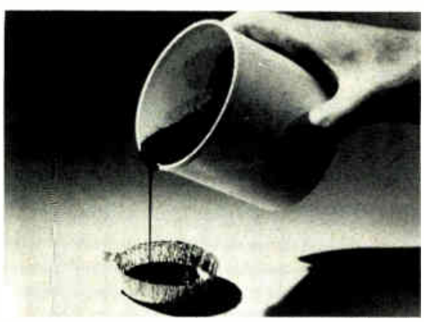
Thick-film resistor materials for high-voltage applications cover the resistivity range from 10 kilohms per square to 5 megohms per square. The 9500 series compositions can be fired in a 30- to 60-minute cycle with a nominal peak temperature of 850°C. According to the manufacturer, the sensitivity of the resistance value to the peak firing temperature

is less than 1%/°C, which compares favorably with the 5%/°C associated with most high-resistivity materials. Resistance change under a constant voltage load of 400 V/mm is negligible; for repeated surges of 3 kV/mm, it is less than 0.5%.

Du Pont Co., Public Affairs Department, Wilmington, Del. 19898. Attn: Barbara Wolf [476]

A low-viscosity casting resin, Stycast 3051 is a one-part material well suited for the filling and penetration of small spaces such as those encountered in high-density circuitry and coils. The potting and encapsulating compound has a viscosity of 3,000 centipoises at 25°C; this may be reduced by heating the material just prior to use. For example, if the solvent-free system is heated to 40°C (104°F), its viscosity drops to 1,600 cps.

Emerson & Cuming, Canton, Mass. 02021. Phone (617) 828-3300 [477]



There's a bright new face in 12" data monitors.

If you've got a need for a 12" CRT monitor, Sanyo has a model that will fill it.

For cost-sensitive applications, choose the 5000 series. You get your choice of AC or DC power, P4 or P31 phosphors, and separate or composite video and sync inputs. 15 MHz bandwidth and standard 15.75 kHz scan rate provide excellent resolution and easy application.

For extra-demanding jobs, pick the 6000 series. You get 1,000 line resolution and 22 MHz bandwidth for ultra-sharp graphics and crisp, high definition 80-character lines. TTL-compatible sync inputs make interfacing a snap.

With either series, you get a compact, rugged steel chassis with adjustable CRT tiltback to fit virtually any enclosure design. You also get adjustable scan size, plus remote brightness control capability. Single-PCB construction and one-connector hookup save time in assembly, testing, and maintenance. And Sanyo's many years of manufacturing field-proven CCTV monitors, and our unparalleled QC assure long, trouble-free service.

For all the facts on these exciting new open-chassis monitors, contact your local Sanyo sales representative listed below.

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Circle 204 on reader service card

New literature

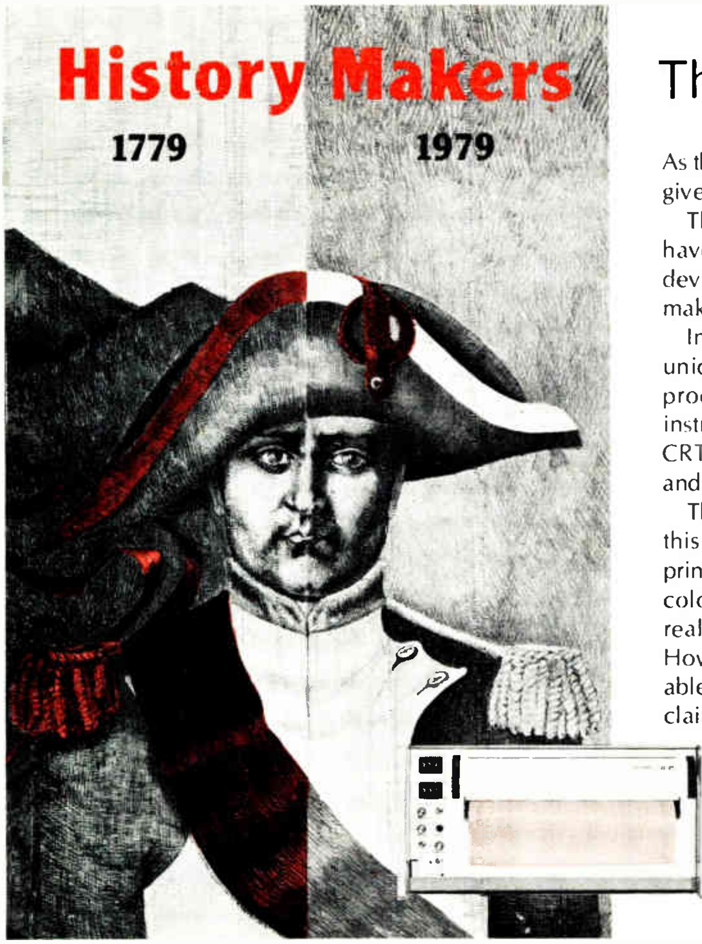
European market forecast. "The Mackintosh Yearbook of West European Electronics Data" has statistics and forecasts on 1980 electronics markets for each Western European country. From the same publisher come forecasts on the world watch and clock industry, as well as technical periodicals on microelectronics. Further details are available from Mackintosh Publications Ltd., Mackintosh House, Napier Road, Luton, LU1 1RG, England [421]

Temperature measurement. "The Temperature Handbook" contains more than 200 pages of information on temperature measurement and instrumentation. Besides reprinting some technical articles, notes, and applications, the handbook includes complete ANSI calibration labels and specifications and photos of existing as well as new products. For a copy, send $5.00 to NANMAC Corp., Dept. C, 9 Mayhew St., Framingham Centre, Mass. 01701

Liquid-crystal display. A 14-page, four-color catalog presents Hamlin Inc.'s complete line of liquid-crystal displays. The catalog highlights features and performance specifications

and photographs. A custom design sheet is included. The LCD catalog number B-93500 is available from Hamlin Inc., Lake and Grove Sts., Lake Mills, Wisc. 53551 [423]

Control switches. "EAO Lighted Pushbutton Controls" is a 20-page brochure that describes the compa-



The HR2000 Datagraph®

As there may be only a handful of true history-making men in a given period of time, so it is with technological breakthroughs.

The CEC Division of Bell & Howell sincerely believes they have now achieved that order of success in the design and development of their newest data recorder . . . the history-making HR2000 Datagraph.

In this, the world's first *all solid state* recorder, a series of unique digital electronic "gates" control the entire recording process. By removing the inherent error factors of earlier instruments — such as in electromechanical, light beam and CRT devices — the accuracy of trace linearity, step functions, and the presentation of square waves are of the highest order.

There are many other features and conveniences to enhance this remarkable recorder — for one, it will accept any direct print paper up to 12" in width — but you'll have to see our full color brochure to appreciate just how advanced the HR2000 really is. It will also contain the location of the CEC/Bell & Howell sales office nearest you. They are ready, anxious and able to demonstrate the instrument . . . and each of the above claims made for it.

CEC DIVISION
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Circle 116 on reader service card

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You'll be in good company in Georgia . . . in the midst of a growing electronics community. Complete with a full range of support services from manufacturers in allied areas.

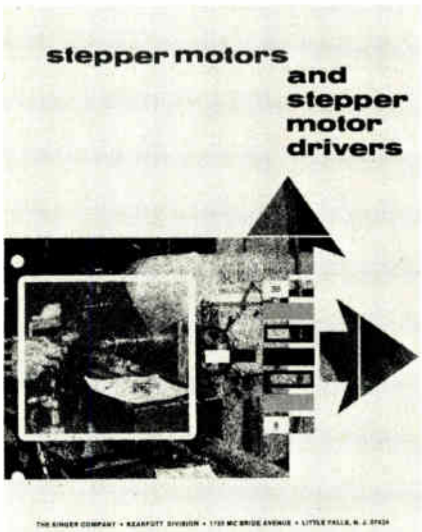
Your company will be able to take advantage of the engineering schools at Georgia Tech. For higher education. For research. For high quality engineering talent.

And Georgia's Quick Start training program will be working for you, too. With labor specifically trained for your operation. At our expense.

For more information, including confidential site selection assistance, call or write: W. Milton Folds, Commissioner, Georgia Department of Industry & Trade, 404/656-3556, P.O. Box 1776, Atlanta, Georgia 30301. Dept. EL-04.

ny's complete line of switches and accessories. It divides the products into two categories: instrument-grade and heavy-duty switches; it details each switch series' design features and functions with photographs, charts, and diagrams. An index for each category provides mounting dimensions, switch elements, and descriptions of parts and accessories. Catalog SF 20-1 can be obtained from EAO Switch Corp., 255 Cherry St., Milford, Conn. 06460 [424]

Stepper motors. A 16-page brochure on stepper motors and drivers describes and illustrates permanent-magnet and variable-reluctance stepper motors in frame sizes of 35 to 38. The brochure has a tabulation of characteristics, outline drawings, and wiring schematics for over 30 stepper motors, including details on a solid-state universal stepper-motor driver with input sequencing logic and universal output drive. The brochure is issued by the Singer Co.'s Kearfort Division, 1150 McBride Ave., Little Falls, N. J. 07424 [425]



Panel meters. A comprehensive panel meter catalog contains 40 pages of information, specifications, and prices on more than 12,000 panel meters, with options and accessory equipment. Included are new additions to the company's line: a minia-

Circle 117 on reader service card

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Dedicated solely to the design and manufacture of custom monolithic integrated circuits, Silicon Systems has developed a unique expertise that places it in the forefront of its technology. Consequently, no application which lends itself to a customized circuit falls outside of the range of SSi capability.

SSi designs both analog and digital functions–even both on the same chip–and we choose objectively between bipolar and MOS technologies. We produce circuit designs to the degree of complexity required by the customer's application–from small scale integration to very large scale integration.

For example, SSi was the first company to fully integrate a DTMF receiver on a monolithic chip, combining both analog and digital functions as well as fully integrating switched capacitor filters on the same CMOS chip. This technology is available to you for your custom application.

For a few more examples, see the circuits below: (a) a custom CMOS IC that replaced 60 standard IC circuits and 2 CMOS RAM's; (b) an I²L bipolar digital IC with 3300 random logic gates; (c) a bipolar linear capacitance threshold detector; (d) an MOS digital loop detector for vehicles; and (e) an MOS photo diode array.

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Silicon Systems incorporated, 14351 Myford Road, Tustin, California 92680. Phone: (714) 731-7110. TWX 910-595-2809.

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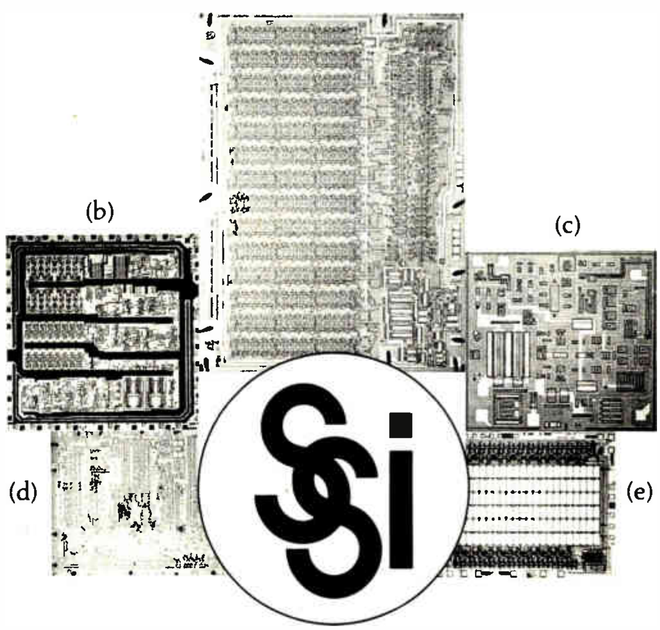

Silicon Systems
incorporated

New literature

ture 90° taut-band meter, designed for flush mounting and available in all dc ranges, and two 250° high-torque band meter movements. Pyrometers, control meters, and ac iron-vane meters are also covered in the catalog, which comes from Modutec Inc., 18 Marshall St., Norwalk, Conn. 06854 [426]

Reliability. The first reliability handbook for the semiconductor industry was prepared to meet the need for greater military standardization. The 832-page illustrated handbook features reliability considerations at each stage of manufacturing: die, assembly, and finished product. In addition, the book outlines reliability concerns for hybrid microcircuits. Appendices offer reference material on wafer fabrication, a list of government agencies, and a bibliography. The handbook (M/S 16250) can be bought for $20.00 from National Semiconductor Corp. distributors or directly from the company's Marketing Services, 2900 Semiconductor Dr., Santa Clara, Calif. 95051.

Telemetry. A "Telemetry Condensed Catalog" has 16 pages of information on analog and digital data-acquisition and reduction equipment. Sections describe products that range from signal conditioners to satellite baseband control systems. The catalog comes from Data Control Systems, Commerce Drive, Danbury, Conn. 06810 [428]

There are more reasons to come to Florida than just sunshine and Disney World - especially if you are an electronics engineer!

Electronics has been the major industrial component of the state's tremendous growth that began in the mid-60s and has continued strong through the 70s with projections very strong for the early 1980s. Currently over 275 electronic companies employ more than 56,000 persons in Florida.

This growth has put electronic engineers in an enviable employment position. Strong hiring competition among Florida companies insures an electronic engineer the opportunity to change jobs within the state rather than feel stranded if he is unhappy with his new employer.

Electronic firms, both large and small, are located throughout Florida but the metropolitan areas of Central Florida, Brevard County, the Gulf Coast (Hillsborough/Pinellas), and the Southeastern coastal strip contain the majority of companies.

Central Florida is the recent home of a General Dynamic's subsidiary, the Stromberg-Carlson Corporation, manufacturers of telecommunication equipment. Though 140 employees are located at their corporate headquarters in Tampa, Stromberg-Carlson employs 1,800 at several Central Florida locations. Their major concentration of electronic engineers is at two plants—the Digital Systems Center in Sanford and the Engineering Development Center in Longwood.

Harris Corporation is the largest industrial employer in Florida, with more than 7,000 employees working in the Melbourne area. Harris, which designs, produces and markets high-technology communication and information processing equipment and systems, projects growth by 1984 to 10,000 employees. The company's major divisions include: Controls, Composition Systems, Electronic Systems, Government Systems Group, Computer Systems, PRD Electronics, Satellite Communications and Semi-conductor.

Among the firms in the St. Petersburg-Clearwater area of the Gulf Coast are E-Systems/ECI Division and the Avionics Division of Honeywell. E-Systems employs approximately 1,500 in their St. Petersburg facility, specializing in sophisticated electronic communications equipment and systems for the United States government and its allies.

The Avionics Division of Honeywell-in-Florida, which employs more than 2,300 workers, is a leading subsystem supplier of diversified avionics products.

The fourth major area of electronics' development stretches southward along the east coast from Fort Pierce to Miami.

International Business Machines (IBM), located at Boca Raton since 1967 and employing approximately 3,000 workers, is the world's largest manufacturer of business machines and data processing equipment.

Siemens Corporation expanded, in December, 1978, its Telecommunications Engineering Division, also at Boca Raton. Located in the Arvida Park of Commerce, more than 250 employees began work for research and development of Siemens telecommunications products.

Following IBM and Siemens Corporation to Boca Raton, the corporate headquarters of Mitel Corporation has moved into the area. Opening their new facilities with more than 100 employees—and anticipating employing 500 within the next three years—Mitel designs, manufacturers and markets electronic telephone equipment and highly sophisticated components for telecommunications systems.

Further south at Ft. Lauderdale, the Communications Group of Motorola employs over 2,500 persons who are involved in the design, manufacture and marketing of high technology communications products and systems. Also to be noted is Motorola's recent announcement of a second major Florida "campus" at Boynton Beach.

A major concern for many electronic engineers considering relocation is the ability to continue their educations. As the number of electronic companies in Florida grows, the number of electronics-related courses at educational institutions expand. Many state supported schools in Florida offer the opportunity for higher education in engineering.

PhD programs are offered by the University of Florida in Gainesville and the University of South Florida in Tampa. Colleges offering degrees through MSEE include: the University of Central Florida in Orlando, the University of Miami, Florida Institute of Technology in Melbourne, and Florida Atlantic University in Boca Raton. The last three also offer an optional program in computer engineering.

Electronic technology programs are offered by Florida A & M at Tallahassee and Florida International University (Miami). Florida A & M has a Data Processing program, and the College of Boca Raton offers a new degree program leading to the Associate in Science Degree in Electronics Engineering Technology.

Though there is much to be said for living in a growing area, Florida also offers a comparatively lower cost of living than most of the country. (See the accompanying table for indexes of comparative living costs for an intermediate household budget of residents in representative metropolitan areas.)

According to the Internal Revenue Service, Florida ranked 46th of 50 in average state and local taxes paid. (Source: February, 1978, Money

Governor Graham

Magazine.) The state of Florida and local communities have no state or city personal income tax, gross receipts tax, ad valorem tax on household goods and personal effects, or gift tax. There is a four percent sales tax for tangible personal property purchases or rentals, with food and drugs exempt of any taxes.

In addition to career opportunities, lower cost of living and the availability of continued education, Florida also offers its renowned climate. Due to the year-round, warm and sunny weather, many outdoors recreational activities are available in every season. The ocean offers a wide variety of entertainment and leisure activities including fishing, surfing, sailing, swimming, scuba diving, and sun bathing. And because most electronic firms are near the coast, these activities are readily available to electronic engineers.

Numerous lakes throughout the state afford residents the opportunity for water skiing and fresh water fishing. Naturally, tennis and golf are chief among activities due to the favorable weather and availability of facilities in every area of the state.

The state's attitude toward the growth of manufacturing is very aggressive. State government has given strong support to industry by encouraging expansion. This continued positive attitude of the Governor's office will encourage further growth and thus enhance career opportunities in the electronics industry.

INDEXES OF COMPARATIVE LIVING COSTS FOR AN INTERMEDIATE BUDGET
AUTUMN, 1978

METROPOLITAN AREA	BUDGET	FOOD	TRANSPORTATION	HOUSING	PERSONAL INCOME TAXES
U.S. Urban Average	100	100	100	100	100
ORLANDO, FLORIDA	88	89	96	86	61
Northeast					
Boston, MA	111	106	117	138	144
New York, NY	116	112	93	127	145
Pittsburgh, PA	97	103	100	90	98
Northcentral					
Chicago, IL	101	102	103	103	95
Cleveland, OH	102	101	100	104	95
Detroit, MI	103	99	98	103	109
St. Louis, MO	96	103	105	90	89
Milwaukee, WI	108	96	101	108	139
Minneapolis-St. Paul	104	98	98	98	138
South					
Atlanta, GA	91	96	95	82	79
Baltimore, MD	100	96	96	95	118
Durham, NC	97	93	94	94	104
Washington, DC	108	102	103	111	130
West					
Los Angeles-Long Beach	95	97	103	90	79
San Francisco-Oakland	104	101	107	104	98
Seattle-Everett, WA	100	100	102	104	81

(Source: U.S. Department of Labor, Bureau of Labor Statistics. Autumn, 1978, "Urban Family Budgets and Comparative Indexes for Selected Urban Areas.")

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- Broad knowledge of Government Contracting and ASPRs.
- Broad experience in Service Sub-Contracting and High Dollar Procurements.
- Knowledge of broadline and specialty distributors/ procurement methods and processes.
- Ability to function in heavy workload, pressure situations.

TEST ENGINEERS

- Familiarity with test methods and systems. Heavy Fortran/ Assembly programming experience in real-time application.
- 2 years experience in system testing and trouble-shooting of digital control or communications systems. Test team leadership ability and technical discussions with customers.
- Disciplines in system trouble-shooting and RF test equipment design and checkout. Logic design experience useful.
- 5-10 years experience in digital test equipment design. Interface with system design team to determine test and test equipment requirements.
- Experience in microprocessor design and software. Intel SRC experience helpful.
- Program and operate computer controlled automatic test systems for test and evaluation of large scale integrated circuits, including microprocessors and peripheral devices. Have understanding of digital logic design and micro-processor fundamentals.

COMPONENT ENGINEERS

- Parts/Materials/Processes experience with expertise in the field of mechanical parts, epoxy and adhesive bonding, specification writing and vendor negotiation, and process control.
- Experience in: generation of Hi-Reliability parts program requirements; establishment of parts screening philosophy with emphasis on micro-electronic devices; vendor interface; and Component Engineering Sub-task Management.

MANUFACTURING/ PRODUCTION ENGINEERS

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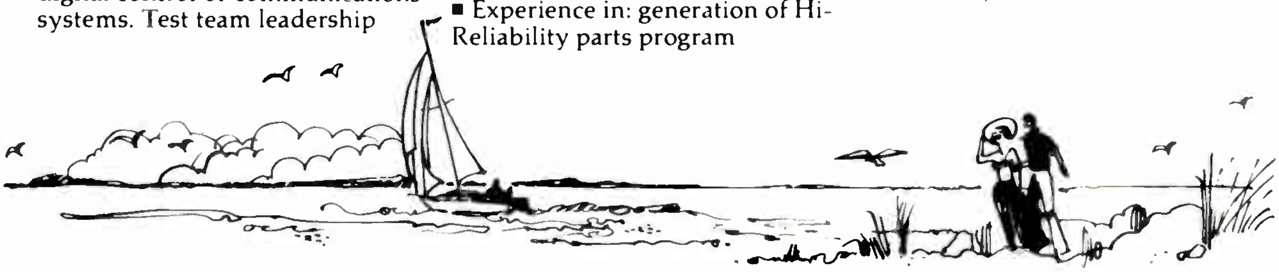
- Experience in airborne electronics hardware assembly.
- Experience in electrical design of digital and analog circuits.
- Hi-Reliability, Black Box Producibility Engineering experience.
- PCB's, Harness Fabrication, and/or electro-mechanical assembly.

Send resume with salary history to: Mr. R.B. Jones, Manager, Professional Staffing, Harris Government Systems Group, P.O. Box 37E, Melbourne, Fl 32901.



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- ☐ Test and debug experience of electronic digital circuits and hardware.
- ☐ Experience with electronic test equipment and techniques in using them.
- ☐ Practical experience in the areas of schematics, parts lists and logic diagrams.

For prompt consideration of your credentials, please forward your resume, including salary history to: Timothy Murray, Burroughs Corporation-Small Systems Group, 4000 N.W. Coral Ridge Drive, Coral Springs, FL 33065.

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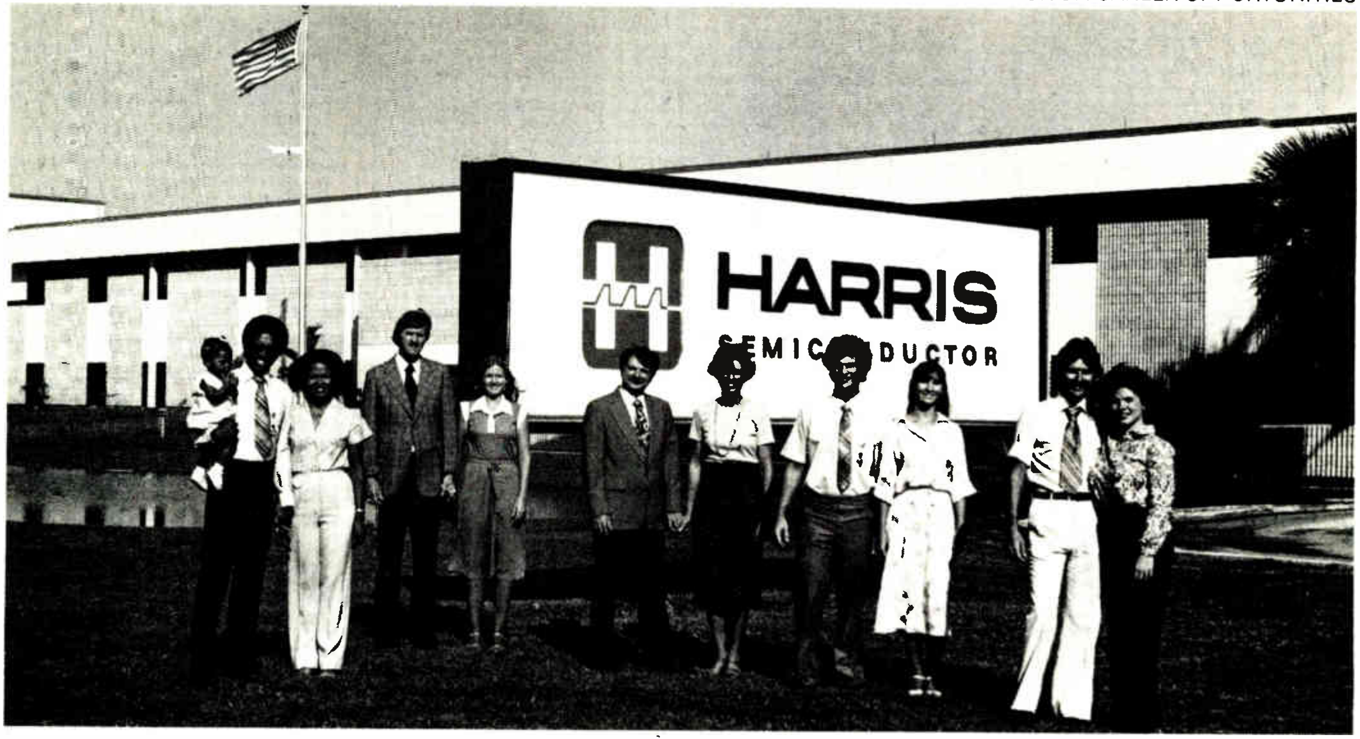

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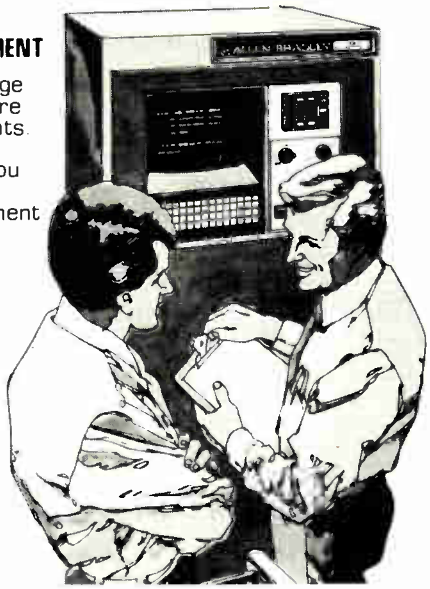

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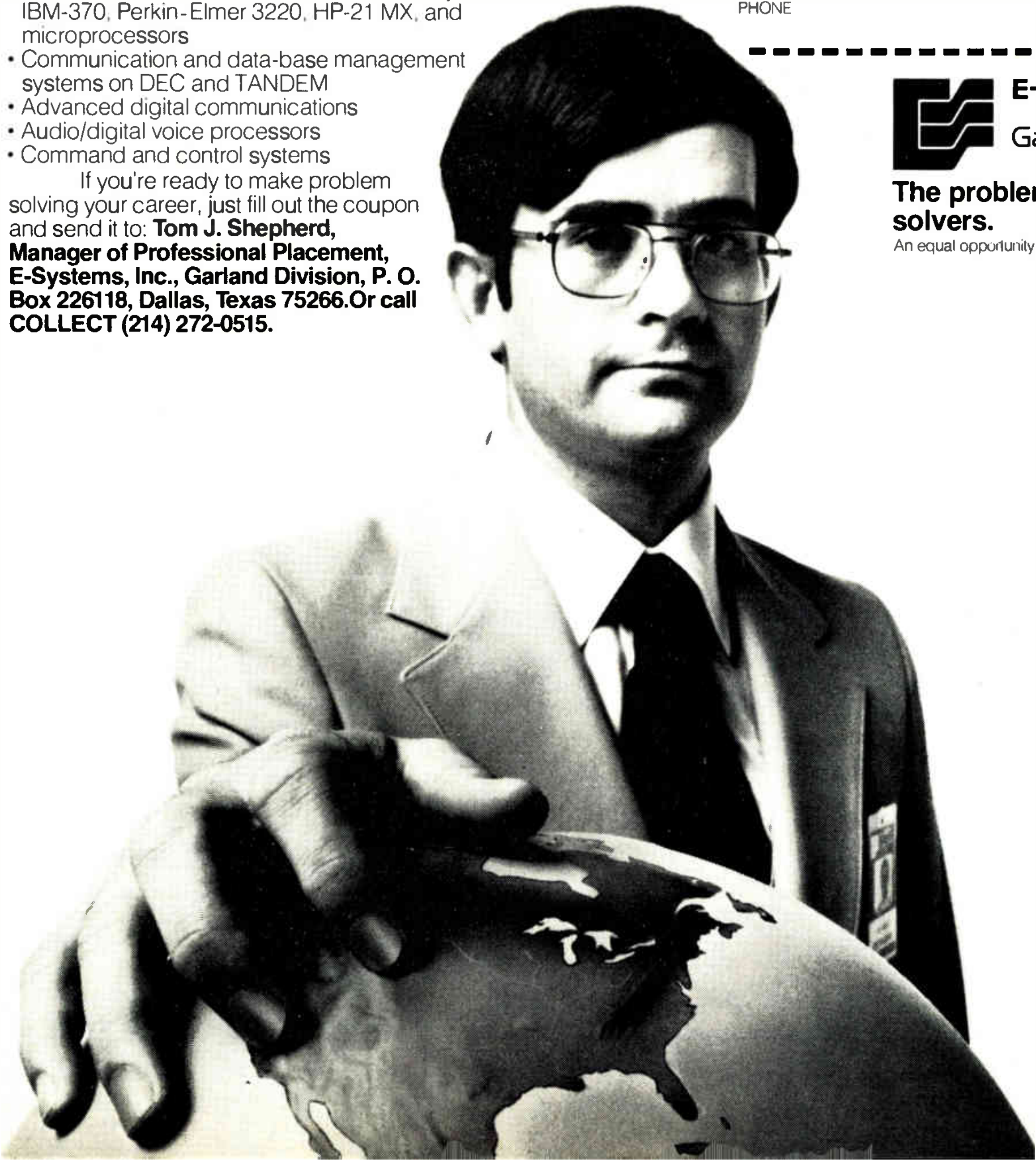

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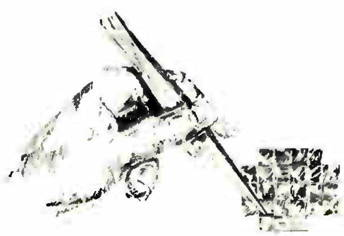

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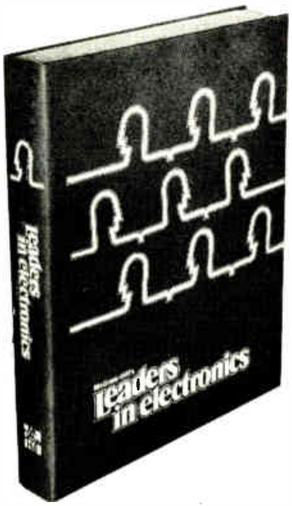

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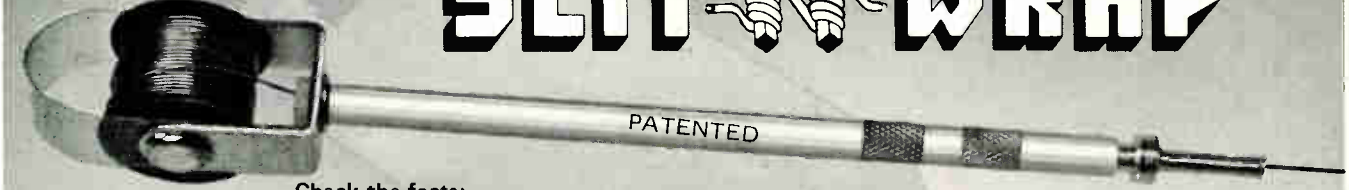


Check the facts:

✔ Vector tools slit insulation over **full wrapped length of post**—*competitive tool wedges wire against post corner, a less reliable way.*

✔ **Daisy-chain wiring** reduces number of wraps needed.

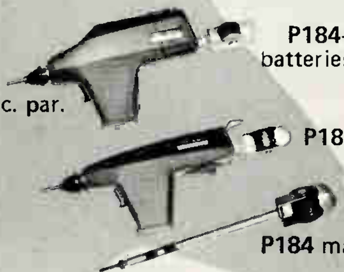
Cross section cut on diagonal at bottom unwrapped wire at top.

✔ Vector tool passes MIL-STD-1130A, wrap spec. par. 5.6. *No such claims made for competitor tool.*

✔ **Rugged** 28 AWG Tefzel silver plated wire or compact polyurethane wire.

✔ **Fast wrapping!** 3 X faster than conventional manual wrap tools. Wraps on .1" spaced pins.

✔ **MOTORIZED** and **MANUAL TOOLS** by Vector—*manual only by competitor.*



P184-4T with NiCad batteries, recharger, $105.

P184-4T1 110 volt AC model, $105.

P184 manual model, $30.

YOU CAN DEPEND ON VECTOR TOOLS—the result of thousands of hours of intensive development

Vector Electronic Company
INCORPORATED

690679 12460 Gladstone Av., Sylmar, CA 91342; phone 213-365-9661, twx 910-496-1539

Circle 236 on reader service card

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machinex 5

The Compact R & D Shop for Electronic Labs

$399.95 complete with 1/4-hp motor

MACHINEX 5 is a ruggedly built metal lathe complete with 1/4-hp motor that machines any material—steel, cast iron, brass, aluminum, plastic, or hardwood. With 5" swing capacity, the lathe can turn large work, yet is so compact it can be used anywhere. MACHINEX 5 is so easy to use that a beginner can precision machine metal parts his first try.

MACHINEX 5 is more than just an ordinary small lathe, for the lathe can be converted to a precision drill press/milling machine in less than a minute with the accessory vertical column.

In all, MACHINEX 5 is really a universal benchtop machine shop. It's an all-in-one lathe/drill/mill that performs all standard metal-machining operations—turning, drilling, milling, boring, and grinding—and preforms them all with split-thousandth precision.

Send 50¢ for brochure $2 brochure and operating manual.

AMERICAN EDELSTAAL INC., DEPT. MK-9
1 Atwood Ave., Tenafly, NJ 07670

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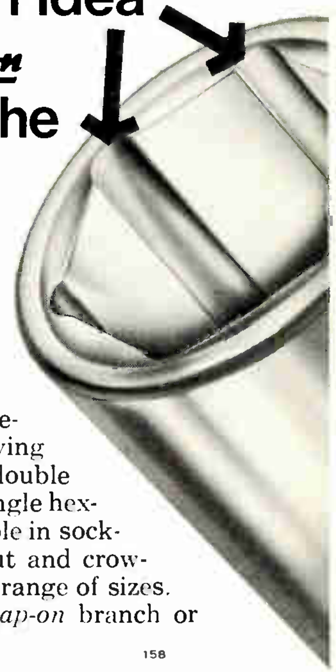
Flank Drive

Best wrench idea since *Snap-on* pioneered the detachable socket!



These new *Snap-on* sockets contact nuts, bolts and cap screws at the flanks instead of the corners. Result: a firm, corner-saving pressure on 12 point (double hexagon) and 6 point (single hexagon) fasteners. Available in sockets, Boxockets, flare nut and crowfoot wrenches in a wide range of sizes. Phone your nearest *Snap-on* branch or write us.

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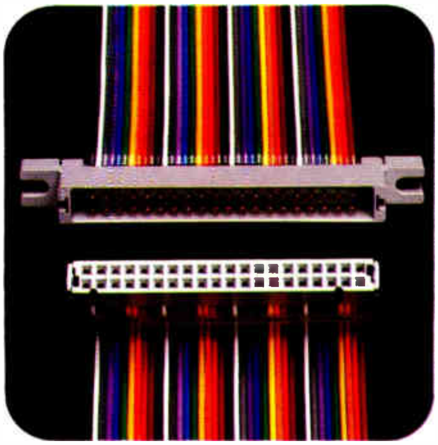
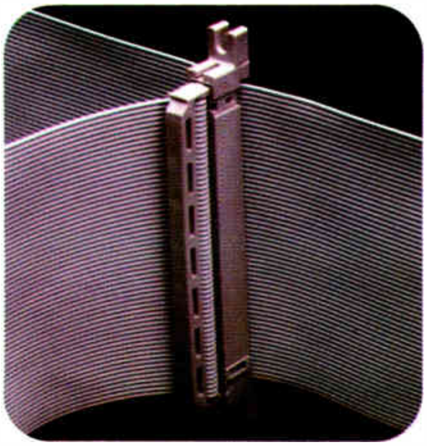
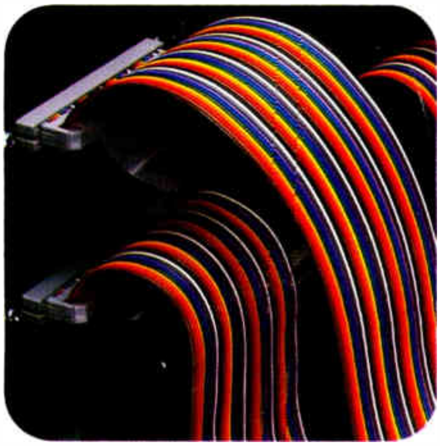
FOR ALL INDUSTRY
SNAP-ON TOOLS
8051-K 28th AVENUE KENOSHA, WISCONSIN 53140

Circle 238 on reader service card

We'll help you make Splices, T-taps and I/O interfaces quickly, and in one step.







Scotchflex® brand plug connectors bring the proved labor-saving of mass termination to T-taps, splices and I/O interfaces. Designed to give you pin configuration continuity in both mid-span and rack and panel applications, Scotchflex plugs are compatible with all socket connectors in the complete Scotchflex line.

Positive polarization.

The design of Scotchflex plug connectors includes two channels in the sidewall. When our polarizing keys are inserted, the plug may be mated one way, and only one way, with its corresponding Scotchflex socket. So you get positive polarization, without the loss of an electrical position. Excellent socket retention. And you eliminate the possibility of equipment damage due to misalignment.

Now up to 60 positions.

To meet your specific design needs, Scotchflex plug connectors are available in 10, 20, 26, 34, 40, 50 and 60-pin sizes, with mounting flanges for panel mounting or without for T-tap or splice applications. Strain relief clips are also available.

There's only one source.

The 3M Scotchflex line offers you the widest choice of mass terminating connectors, cable and system components. Plus proven reliability. Off-the-shelf availability through a nationwide network of distributors. And the unmatched experience of the people who pioneered the concept of electronic mass termination.

Scotchflex connectors are recognized under the component program of Underwriters Laboratories, Inc.

"Scotchflex" is a registered trademark of 3M.

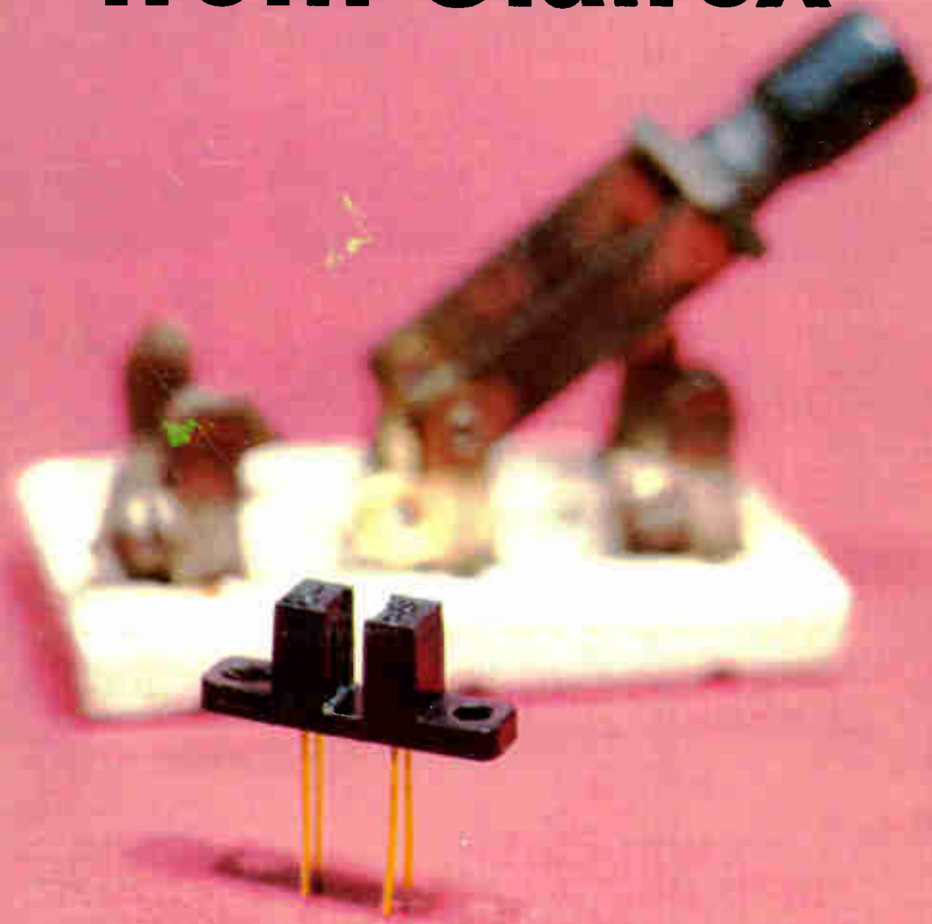
Scotchflex® systems from 3M. The source.

3M

Circle Number 901 on Reader Service Card

Switch from the old to the new!

Low-cost OPTICAL SWITCHES from Clairex



Switch from slow switching, moving parts and arcing problems to fast switching, solid-state, low-cost optical switches from Clairex.

Seventeen optical switches in the CLI 800 series lets you choose from: a wide range of sensor currents; phototransistor and photodarlington outputs; and two voltage ranges, 30 and 55 volts. Each series features a model with a ten-mil slit over the sensor for applications necessitating stringent target resolution.

Clairex also offers the CLI 200 and CLI 300 series that are designed for harsh environmental applications.

For details on the full line of Clairex Optical Switches, call (914) 664-6602 or write Clairex,® 560 South Third Avenue, Mount Vernon, New York 10550.

CLAIREX ELECTRONICS

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Circle 902 on reader service card