OCTOBER 11, 1979

EE SHORTAGE WORRIES IC MAKERS/98

Could a four-pin memory chip halve system costs?/144

New 16-bit microprocessor stresses simple software design/118

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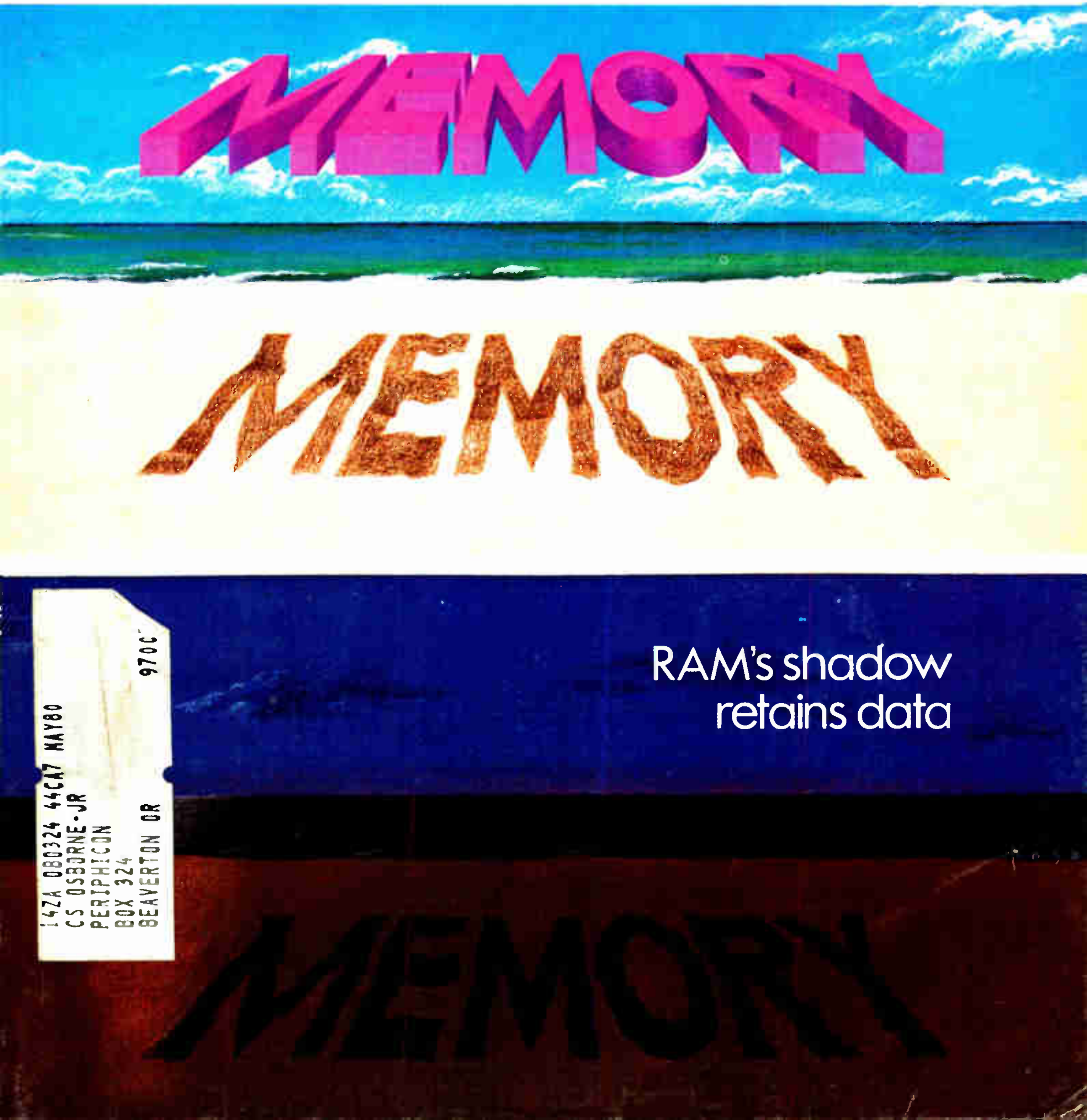

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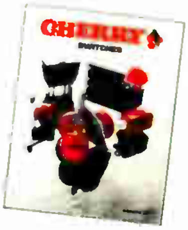

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Electronics

The International Magazine of Electronics Technology

Vol. 52, No. 21 • October 11, 1979

Highlights

Cover: The shadow remembers, 111
Floating polysilicon gates form a nonvolatile backup array for a 1-K static random-access memory, resulting in a nonvolatile device that can be erased and programmed with 5 volts.

Cover art is by Microsystems & Software Editor John Posa.

Lithography limits broken, 92
Optical lithography looks towards line widths well below 1 μm. And lines possible with X-ray lithography have shrunk from 1,000 to 200 angstroms, the Semicon/East audience learned in Boston late last month.

Keeping improved computers compatible, 131
Using the latest hardware to boost a minicomputer's performance need not be done at the expense of mechanical and software compatibility with existing family members. Microcode helps.

Transistors sense temperature accurately, 137
Recent improvements in geometry control allow matched transistors to serve interchangeably as cheap, accurate temperature sensors.

. . . and in the next issue
Electronics' annual technology update . . . the 1979 achievement award.

Publisher's letter

It is unusual for the person who edits a cover article also to execute the cover illustration. But that's what happened with this issue's cover story (see p. 111). Our Renaissance man is John Posa, microsystems and software editor, who handled the article on Xicor Inc.'s new nonvolatile memory and then left the typewriter for the easel to translate its meaning into visual form.

The transition was not a hard one. John has long enjoyed painting and is at present a part-time art student at Pratt Institute in Brooklyn, a school from which many of America's finest artists and designers have graduated.

It all began with the usual meeting between the editors involved and art director Fred Sklenar to invent a concept for the cover illustration. Various suggestions were tossed around by John, chief editor Sam Weber, and technical managing editor Ray Capece, and when Fred crystallized them into a single idea, John announced, "Hey, I'll do it."

Fred's reaction? "I knew John painted, so why not give it a try?"

Actually, John had illustrated articles for a fiction journal while attending engineering school at the University of Michigan and more recently has been working in oils, concentrating on tropical beach scenes. He did the cover picture, though, in Prismacolor over tempera, or, as he puts it, in colored pencils over poster paint.

"Having edited the article and knowing how the device works definitely helped in doing the illustration," John observes. "It made me

Talented. John Posa demonstrates his ability to pose for pictures as well as paint 'em.

sure the execution was correct."

The art director was pleased, too. "It's a totally professional job, and I look forward to another," says Fred.

It could happen—John has a special report coming up. In the meantime, he's enjoying the satisfaction of having done this one.

"My family and friends back in Michigan don't yet know I did a cover," says John, "I plan to surprise them with it. I send them issues from time to time, but I get the feeling that my articles go unread because they're too specialized. I wanted this cover to be something everybody could pick up and enjoy."

The issue started a joke around the office; that from now on, whoever edits the cover article has to draw the cover also.

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Readers' comments

Wanted: Committee participants

To the Editor: The reactivation of the Joint Electron Device Engineering Council (Jedec) JC-30 Committee mentioned in the Electronics Newsletter [August 16, p. 33] is based on current need within the hybrid manufacturing industry for practical standards in products and components and is vital to the continued welfare of hybrid technology.

The key issue confronting the industry and its interface with military and aerospace users centers on MIL-STD-883 and MIL-M-38510. Since its issue, MIL-STD-883 has undergone numerous changes to incorporate hybrid microelectronics within its scope. Addition of MIL-M-38510 to the requirement for hybrids has been less than completely successful because of the specification's generality. MIL-M-38510 is sorely in need of attention from industry representatives to make it a viable document for use by the end user—JC-30 will address that need as one of its initial tasks.

Since the practical implementation of hybrid manufacturing concepts encompasses nearly every microelectronic material and component science, from monolithic technology to ceramics, we encourage participation in the committee by all those who have professional interests in specifying, designing, or manufacturing such devices. Our intention is to work as a unified, mature industry toward more rational standards for hybrid assemblies—whether standard or custom designs—and to offer military and aerospace users the means for presenting their needs to the hybrid industry through professionals engaged specifically in that science.

As we proceed toward our goal of effective standards, we will encounter a number of peripheral items such as component standardization, package standardization, and process-inspection standards. We expect to deal with each of those items as appropriate to complete MIL-M-38510 (for hybrids) to the level of monolithic devices.

Committee activity to reach our goal requires technical participation by ISHM members, the industry at large, and qualified representatives from Government groups such as the Defense Electronic Supply Center (DESC) and Rome Air Development Center (RADC), as a minimum.

The first JC-30 Committee meeting will take place on October 16 at the San Francisco Airport Hilton. Those from industry or the military with an interest in hybrid technology should contact me at Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 01730, (617) 275-1570.

G. J. Estep, Chairman
JC-30 Committee on Hybrids
Bedford, Mass.

Worth it?

To the Editor: Perhaps Sandia should check its figures relative to the payback of the solar concentrator systems discussed in the July 19 issue ["A burst of energy in photovoltaics," p. 105]. At full power output 24 hours a day, 365 days a year, for 6 years with no maintenance, its energy producton would cost about 10 times the current national average.

R. S. Siebert
Newport Beach, Calif.

Please note

To the Editor: I very much enjoyed the article on peripheral chips in your Aug. 16 issue ["Peripheral chips shift microprocessor systems into high gear," p. 93]. I would, however, like to correct one oversight regarding the 1791 floppy-disk controller: Synertek will be second-sourcing Western Digital's 1791-01.

Stephen J. Faris
Synertek Inc.
Santa Clara, Calif.

Three authors, not one

To the editor: In our article, "Optically coupled triac driver chip interfaces logic to ac load" [August 30, p. 145], I was listed as the sole author, when in fact this work was a product of the efforts of three of us—myself, Paul G. Alonas, and David M. Gilbert, all of Motorola.

Vernon P. O'Neill
Phoenix, Ariz.

Three ways that pre-owned instruments are better than new.

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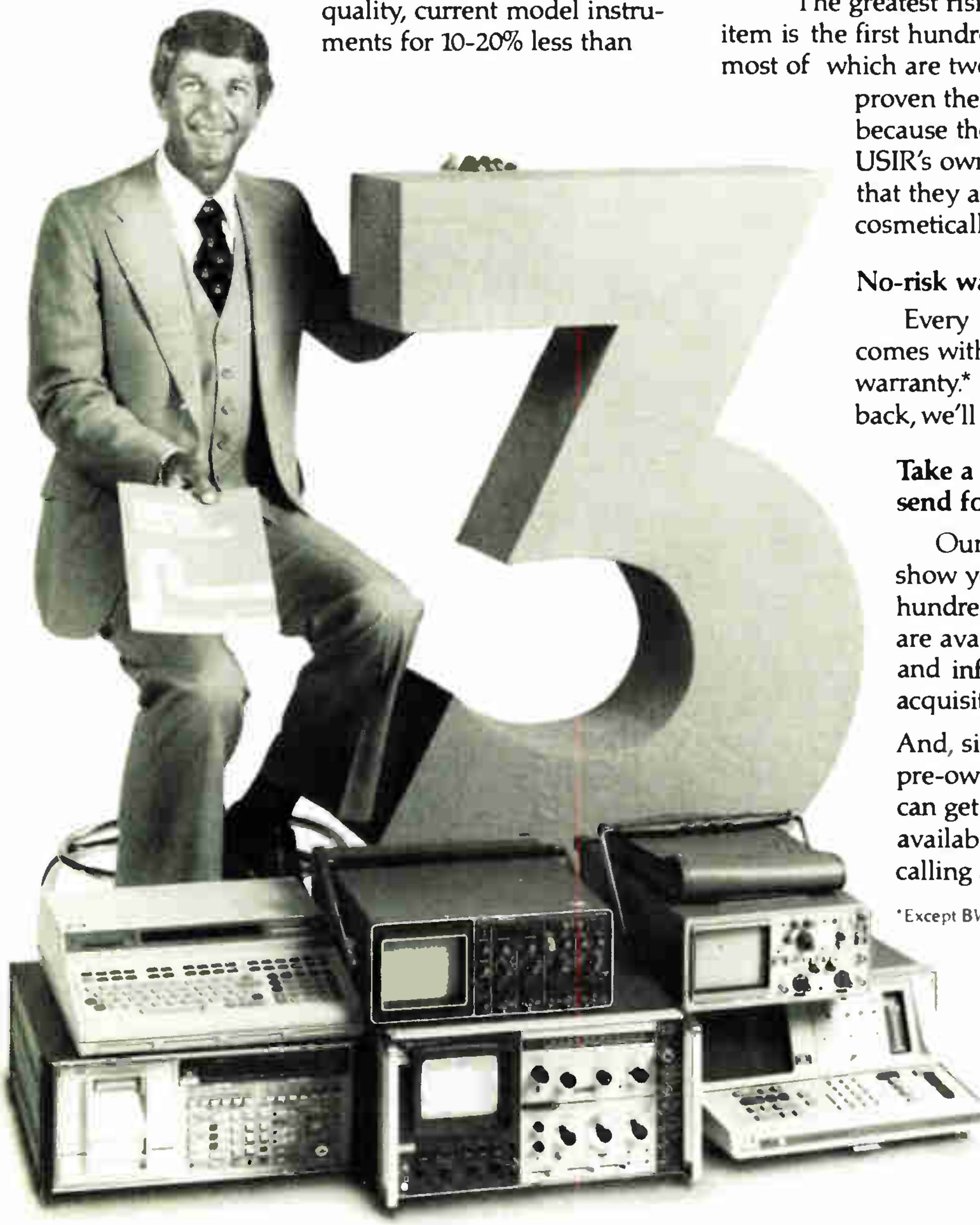

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News update

■ Comsat General TeleSystems Inc., the recently established manufacturing branch of Comsat Corp., is deeply involved in the echo-canceler business on the basis of the work of its parent, Comsat Laboratories, over the past 11 years. Like Bell Laboratories' chip [*Electronics*, Aug. 2, p. 41], Comsat's echo-canceling board is "basically a digital device," although it is designed to operate on analog circuits, points out Ivan T. Riley, manager of market planning at TeleSystems.

Furthermore, notes Riley, the device is fully operational and is currently being sold to RCA American Communications Inc., among others, for use by its satellites. As at present configured, the canceler requires one circuit board (about 10 by 18 inches) per channel end. And, while the system, which uses large-scale integrated circuits, consumes just over 20 watts per board, smaller designs with lower power are under development.

Riley says that, outside of the Bell System, the Comsat organization is the leading manufacturer of echo cancelers and "intends to remain a leader." Backing him up, Louis Pollack, Comsat's executive director for satellite communications research, says several hundred cancelers built by Comsat are now operational in the U. S. and Canada. For now, Riley will say only that TeleSystems is looking at the possibility of putting all or part of its echo cancelers on an LSI chip, but no target date for this development has been set.

Engineers involved with echo cancelers and satellite circuitry are at present waiting the Consultative Committee for International Telephony and Telegraphy to issue changed recommendations regarding acceptable transmission delays for telephone circuits. The current ones refer to echo suppressors, but new figures are being eagerly awaited now that the canceler has reached such a level of sophistication and popularity. As Comsat executive Pollack says, "echo cancelers provide the solution for echo-related problems." **-Harvey J. Hindin**

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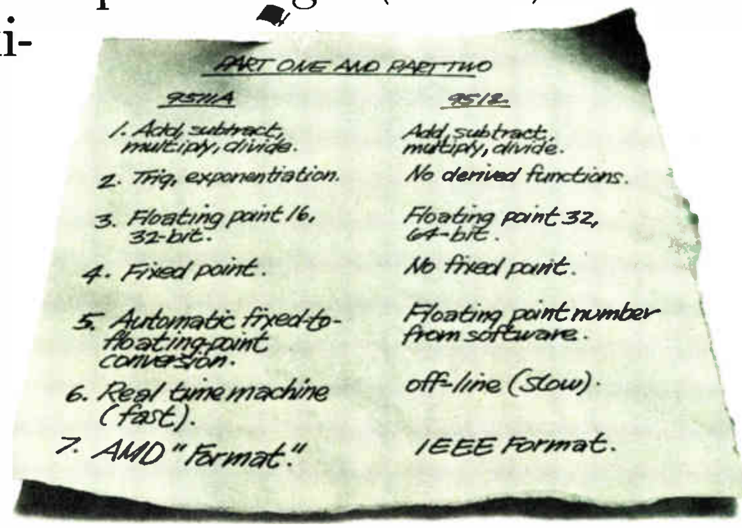

MATH CHIPS: PART TWO.

Young high-tech companies need nourishment

If there is a recession, it was nowhere in evidence to the more than 50,000 attendees who descended on San Francisco during the recent Wescon. The packed aisles, standing-room-only technical sessions, and general ebullience cannot be entirely interpreted as meaning that the electronics industries have reached that long-predicted state of grace known as being "recession-proof." But there was enough talk about full order books to show that the brash innovative spirit of our industries is keeping them well above the problems besetting much other business.

We hope the Congress was paying attention, because that brash, innovative spirit is not being cherished and nurtured by the U. S. government the way it should be, particularly in small, high-technology companies—the very kind that were originally responsible for the developments leading to our current boom.

Recently, the Small Business Administration and the Department of Commerce set up a task force of three citizen panels to study job creation and domestic innovation. Their reports were submitted to the House of Representatives' Committee on Small Business as a matter "of national urgency."

The panels found that a wide array of Federal policies have an adverse impact on small innovative businesses. For example:

- Federal tax, pension-fund and security policies have eliminated almost all forms of capital from small business ventures.
- The Government's tendency to treat large and small firms alike in fact discriminates against small firms.
- Federal research and development funding and procurement regulations virtually exclude small innovative firms from effective participation in Government programs.
- Federal patent policies diminish the value of patent protection for independent inventors and small businesses.

All this runs counter to the accumulated evidence that small, innovative businesses are the driving force behind major economic growth. For example, a study made at the Massachusetts Institute of Technology for the Department of Commerce shows that small concerns with 20 or fewer employees created 66% of all net new jobs in the private sector between 1969 and 1976, while 87% of all new jobs came from firms with 500 or less.

Another MIT study of 16 highly successful industry leaders compared growth in employment and tax revenues to that of sales in the 1969–1974 period. The results were startling. In that period, young technology companies like Data General, National Semiconductor, and Digital Equipment, with sales only 2% as large as those of mature firms like Du Pont, General Electric, and Bethlehem Steel, created 34% more jobs. Total employment in the mature firms increased only 3.2%, compared to 23.7% for the innovative companies. And the latter group provided nearly $2.3 billion of income tax revenues compared to $1.5 billion for the mature companies.

But the task force also found that today's environment for small business innovation is not healthy. Citing a tenfold decline in productivity over the past 15 years and a hundredfold decrease in capital flow to small innovative businesses, the report calls for detailed changes in Government policies if a "rebirth of vigorous innovation" is to occur.

Unfortunately, as Milton D. Stewart, chief counsel for advocacy of the SBA, said in urging quick consideration of these changes, "over the past 25 years numerous blue-ribbon panels, commissions, and task forces have [made similar] recommendations . . . What is tragic is that . . . Government has failed to respond by enacting their recommendations."

That's why we hope there were members of Congress among the throngs at Wescon. In the bustling stands, the payoff of the innovation that thrived over the past decade was there for all to see.

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People

Signetics seeks a new microprocessor presence

Although Signetics Corp. does a comfortable microprocessor business by making the 2650 and second-sourcing the 8048 and 8021, it has lacked the proprietary punch to offer the marketplace an identifiable mainstream product. But Roger Badertscher, the new vice president and general manager of the MOS Microprocessor division, plans to change that by offering proprietary products at both ends of the market as well as several peripherals, such as data-communications circuits and cathode-ray-tube controller chip sets.

Part of what is fueling his thinking is that on the single-chip microcomputer end, for example, there is a lot of room for innovation as the 8-bit models become more sophisticated. Coming into the marketplace are single-chippers incorporating 50,000 transistor-type circuits, but Badertscher foresees more complex parts coming out in two years, containing several times more transistors and integrating more memory, more input/output, and analog-to-digital conversion functions.

Moreover, as the technology progresses, "it's natural to expect single-chip microcomputers to evolve into the 16-bit area, although 8-bit design-ins will continue," the new general manager says.

"That's in contrast to multichip computer systems, where 8-bit CPUs will give way to 16-bit devices." Badertscher jokes, however, that for designers and users that might pose a problem of "how you use 200,000 transistors."

Still going up. On the high end, he thinks the last word has not been said, not even in 16-bit microprocessors. He has several alternative roads that Signetics can follow at the 16-bit level, he says, including second-sourcing, although he believes that "clearly, for a benchmark machine, you have to have something equivalent to a Z8000 or 68000."

Badertscher took his new job because he could manage a "more integrated effort—I can broaden myself more meaningfully here than at the Zilog job," where he was general manager of the Components division. Part of that integrated effort includes monitoring the annual $1 billion in research and development spent by parent NV Philips Gloeilampenfabrieken of the Netherlands. Meanwhile, he has two immediate objectives—to develop a good strategy and to pull together a substantial state-of-the-art wafer-fabrication capacity, putting it into production in 1980.

More coming. Signetics' Badertscher plans new proprietary microprocessor products.

There is capital available for the right companies

Fledgling electronics firms looking to leave the startup nest are finding there is money available to give them that necessary takeoff boost. But that does not mean every company with a good idea will find backing, says Jay Cooke, executive vice president for the Wall Street firm, Laidlaw Adams & Peck Inc.

Cooke is managing director of the corporate finance department, which is making something of a specialty of finding capital for emerging technology-based companies. A recent beneficiary was R. C. Sanders Technology Systems Inc. [*Electronics*, Aug. 30, p. 48].

For investment bankers, the most attractive technology companies are in areas where demand exceeds supply, "where the return on equity

People

Money provider. Jay Cooke says high technology still attracts investors.

capital is very high, say, 30% or better," Cooke says. He and his associates have identified four such areas in the electronics industries:

- Medical electronics.
- Data communications.
- Systems houses.
- Peripheral makers.

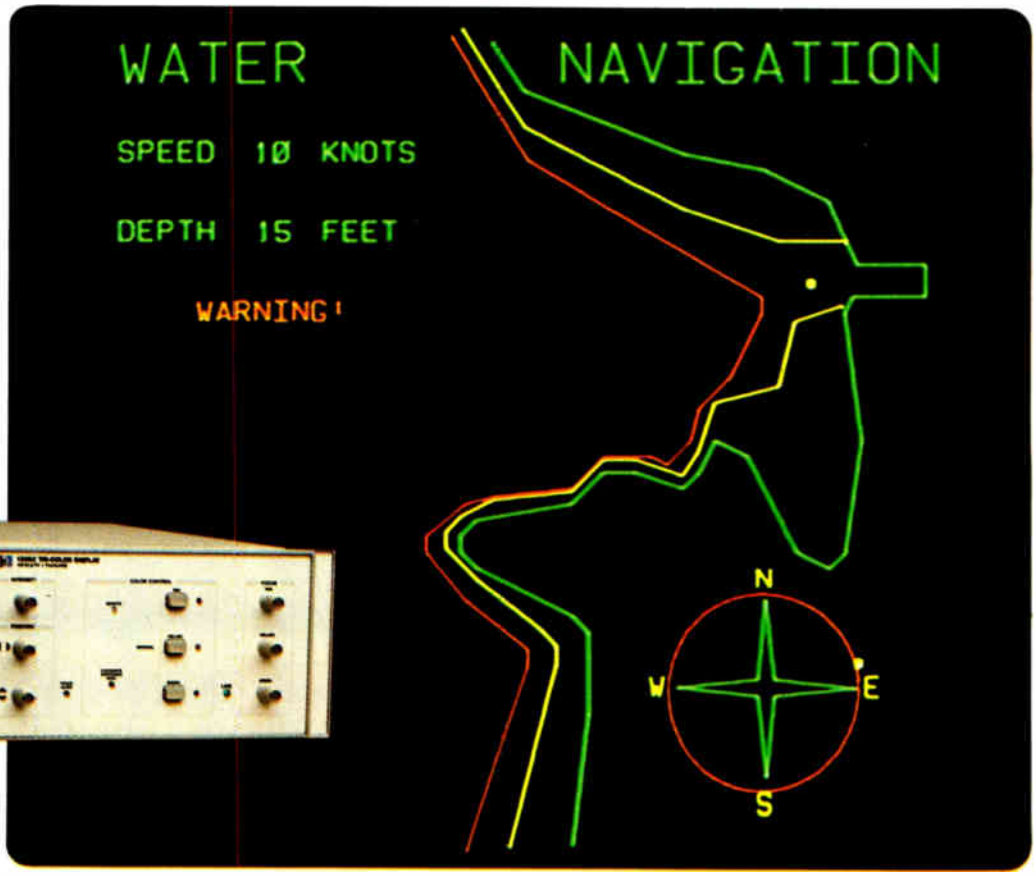
Other candidates might appear to be energy-related companies, but "that's no business for startups," Cooke says, because the investment required is beyond the resources of any but major corporations. For the same reasons "we would have very serious reservations about financing any hardware company" in such areas as mainframes, minicomputers, and microcomputers, he adds.

But for the right company, there is no question that capital is available, Cooke affirms. Initial backing is more likely to come from venture capitalists [*Electronics*, May 10, p. 88], who look for established credibility on the part of the principals in the new firm and for a sound, well-documented business plan, he notes. For second-stage financing and beyond, investment bankers can play a role. By raising money through such means as initial public offerings of stock, companies usually can garner more dollars for relinquishing a given share of ownership, he says.

Qualifications. What firms such as his seek in a company are market acceptability of the product or service, visibility in the marketplace, and the track record—at the company—of the principals. And a lot of companies out there meet these specifications, he avers.

hp MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

AUGUST 1979



HP's Tri-Color Display generates random-scan presentations in three color hues to clearly separate or highlight information for easier and faster interpretation in waveform analysis, computer-aided design (CAD), radar, flight simulation and more.

HP-IB

New tri-color display features high-resolution and high-speed vector presentations

As information density on graphics displays increases, analysis becomes difficult and errors multiply. An effective method for reducing such errors and speeding analysis is to differentiate the information by color. Using the latest advancements in beam penetration phosphor technology, Hewlett-Packard's new 1338A Tri-Color Display offers a cost-effective solution to the problem of high-density data differentiation.

This high-resolution, high-speed electrostatic CRT display generates red, green, and yellow color hues for separating or highlighting information for applications including waveform analysis, radar, computer-aided design and data acquisition. For example, in waveform analysis, color visually separates overlapping waveforms. In data acquisition systems, color can differentiate between data types and out-of-limit conditions. In avionics color differentiation can be put to excellent use in flight simulation, navigation and electronic countermeasure receiver systems.

Shadow mask designs cannot match the high resolution color displays made possible with the 1338A because discrete red, green, and yellow dots and vectors can be written randomly on the 1338A screen. Color hues are generated when changes in post-accelerator voltage excite different phosphors. A high-

(continued on third page)

IN THIS ISSUE

Compact lab power supply features triple outputs

This low-cost, compact, three-in-one power supply is a handy addition to the lab bench where single or multiple voltages are needed for designing and testing breadboards and prototypes. The HP 6235A Triple Output DC Power Supply delivers three adjustable DC output voltages: 0 to 6 V at 1 A, 0 to +18 V at 0.2 A, and 0 to −18 V at 0.2 A. A single 0 to 36 V output at 0.2 A can also be obtained by connecting across the −18 V and +18 V terminals. The +6 V and +18 V outputs can be adjusted independently. The −18 V output is adjusted with a tracking ratio control, after which it will proportionately follow the +18 V output as the +18 V control is adjusted. The +18 V and −18 V tracking outputs are especially useful for powering operational amplifiers and other circuits requiring symmetrical operating voltages.

The supply is a constant voltage/current limit type, with each voltage continuously adjustable over its range, while the maximum current available is automatically limited to prevent overloading. You can quickly select and monitor voltage or current for each output with the pushbutton meter switches.

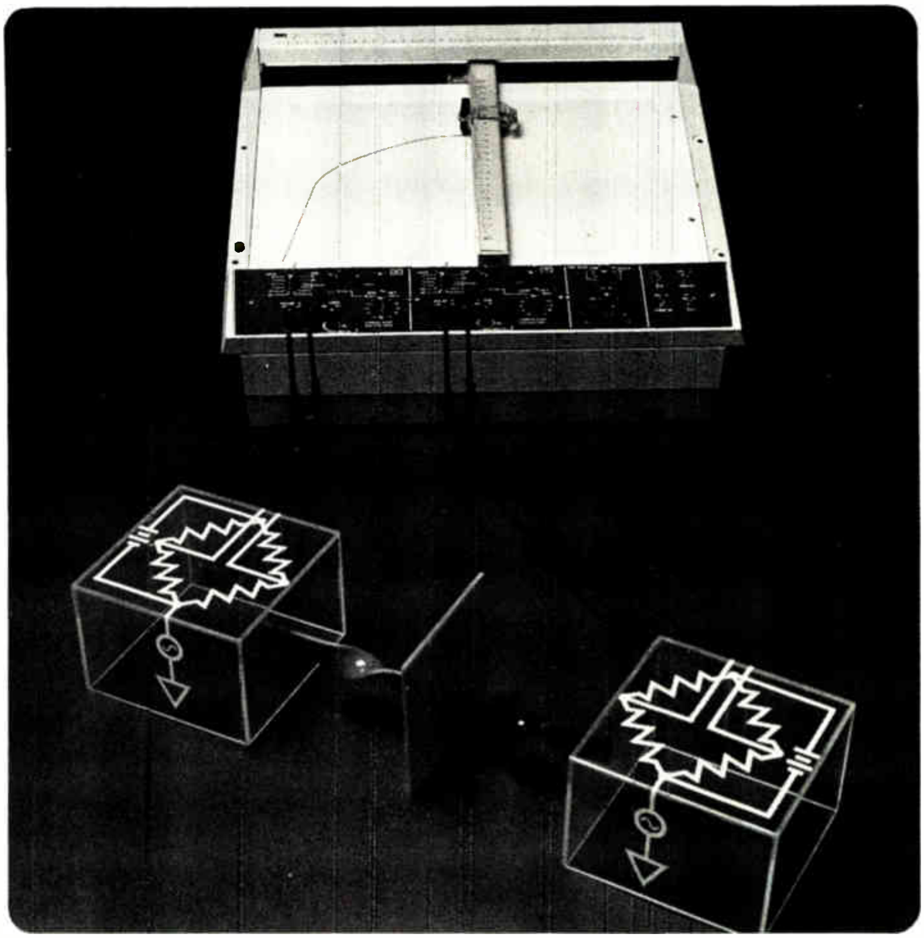
Weighing only 2.3 kilograms, (5 lbs.), the 6235A is small enough to pick up with one hand. It can be powered from 115 V or 230 V, 47-63 Hz AC input.

*Check **B** on the HP Reply Card for more information about this and other low-cost power supplies for your lab bench.*

Convenient power for circuit breadboards is yours with this new three-in-one lab bench power supply.

Automatic guard for recorder provides convenience and high-sensitivity

HP-IB



A major convenience feature, "automatic guard", is incorporated into HP's 7047A's High Sensitivity Recorder to provide you with complete freedom in connecting input terminals. Automatic guard removes the necessity for connecting the guard to maintain good common mode rejection.

Until the development of automatic guard, the input terminal connection configuration was an often overlooked but potentially serious noise source for high sensitivity recording. The type and severity of input noise is largely dependent on the input configuration used. Problems can result from two sources:

1. A common-mode signal can result in excessive noise, and
2. "Pump-out" current from the measuring instrument can interact with the signal's circuit to produce excessive noise.

Both of these sources are extremely troublesome on instruments such as recorders using null balance servo systems. However, the 7047A's input circuit removes the need for a guard connection and forces the "pump-out" current to approach zero. The result is usable high sensitivity, independent of guard connection and input connection configuration.

The 7047A was designed to combine high sensitivity with high performance. It has a maximum input sensitivity of 0.02 millivolts/cm on each axis.

It is an 11 × 17 inch, or A3, X-Y recorder combining high dynamic performance (8 g acceleration) with usable high sensitivity (20 microvolts/cm) and calibrated offset (10 scales). Other 7047A features include TTL level remote control, electrostatic paper hold-down, and both X and Y axes timesweeping.

*Two HP technical notes covering 1) the subject of input noise and its relationship to input connection configuration, and 2) the circuitry used in providing automatic guarding are available. If you would like to receive these technical notes, circle **C** on the HP Reply Card.*

Fiber optics sheds new light on HP-IB capability

HP-IB

Users have long appreciated the convenience and practicality of the Hewlett-Packard Interface Bus (HP-IB). Now, HP has combined this proven (IEEE 488) interface with the innovative technology of fiber optics for improved speed, reliability, and configuration flexibility.

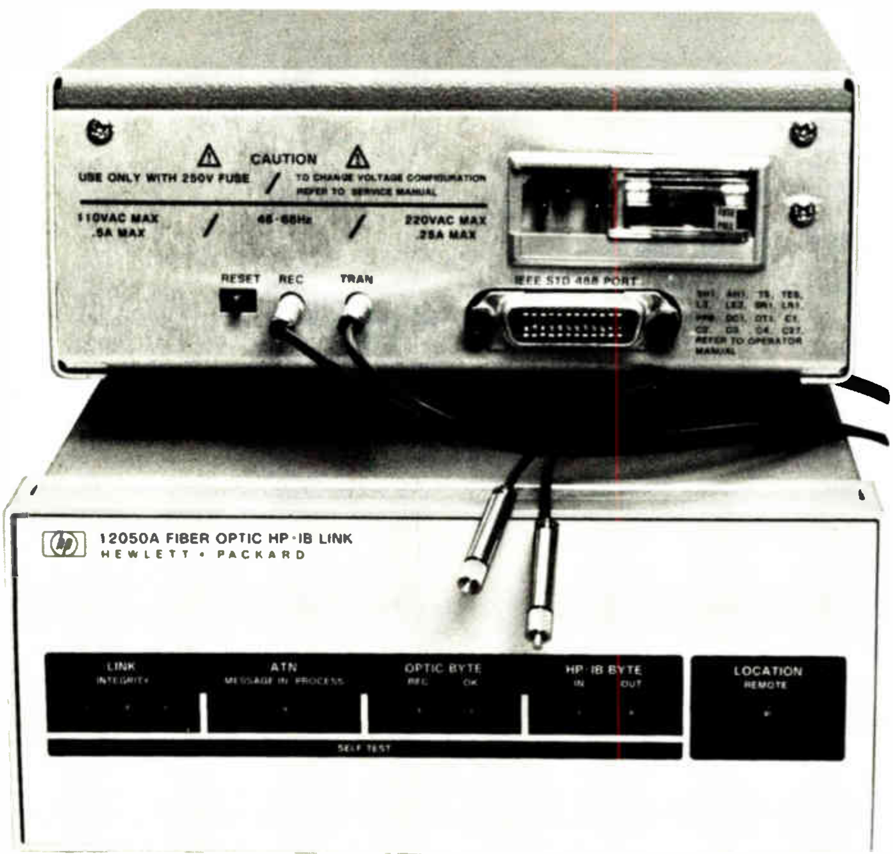
The new HP-IB Fiber Optic Link permits instrument clusters to be located up to 100 metres (328 feet) from any HP-IB controller. Two 12050A units are required, which function as transmitter/receiver at each end of the link, connected by a dual fiber optic cable. HP-IB bit parallel protocol and TTL signals are converted to a bit serial stream that is transmitted optically, then converted back to HP-IB format at the distant site. In other words, pulses of light traveling over hair-thin optical fibers in the cable replace traditional electrical transmission over copper wires.

This exciting new technology greatly increases HP-IB utilization in demanding industrial applications. Here are just some of the link's highlights:

- High-speed data transmission (20,000 bytes/second).
- Detection of service interrupt requests within 100 μs.
- Excellent electromagnetic noise immunity—the cable can be used near rotating machinery, transformers, switch gears, large power supplies, etc. without loss of data integrity.
- Complete electrical isolation between computer and remote instrumentation—no need to worry about unwanted ground loops or spurious spikes damaging computer equipment or distorting signals.
- Safe for explosive environments—since the cable carries no electrical energy, it is harmless even if cut.

The 12050A transmitter/receiver unit also has a built-in microprocessor that performs self-testing and checks for transmitted errors during system communication.

To learn more about this new high-performance remote instrumentation interface, check **D** *on the HP Reply Card.*



Satisfy a variety of stimulus needs with one instrument. New application note shows how.

Reporting on research, development and maintenance projects, HP's new Application Note #289 shows a variety of stimulus needs satisfied by just a single instrument—this instrument is the HP 8165A Programmable Signal Source, a pulse/function generator with synthesizer stability.

In this A.N., case histories from industry, space, transport and navigation describe the performance of HP's 8165A in a range of applications. Applications chart and feature summary are included in the A.N. to let you see quickly how the 8165A can contribute to your own measurement needs.

For your free copy of A.N. #289 and the 8165A data sheet, check **E** *on the HP Reply Card.*

Easy data interpretation with tri-color display

(continued from first page)

speed switch changes this voltage in as little as 100 μs.

Because the 1338A is an electrostatic deflection CRT, it requires less power than electromagnetic systems, thus reducing heat and improving reliability.

The reasonable cost for this exciting new display now makes it feasible to include in systems and instruments where increased visual cues and rapid decision making are extremely important. Interfacing the 1338A to a system or instrument requires only one TTL level color bus and three analog inputs through rear panel connectors. The 1350A Graphics Translator can be used to connect this display to systems with an HP-IB or RS-232C interface.

Check **B** *on the HP Reply Card for additional details.*

RF and microwave component designers can now measure noise figure more accurately

Noise figure is one of the most important specifications for amplifiers, signal conversion devices, and many system components. HP's new 346B Noise Source combined with a power meter measuring technique now offers substantial improvements in noise figure measurement. With solid state technology driving noise figure characteristics to new lows, measurement uncertainty is decreased.

Present measurements have uncertainties caused by noise source SWR mismatch, change of SWR from noise source ON to noise OFF condition, accuracy of the excess noise ratio (ENR), and finally the instrument accuracy. Uncertainties up to ±2 dB were not unusual for automatic instrumentation, a barely tolerable situation as component noise figures approach 4 or 3 dB.

The new HP 346B Noise Source (10 MHz to 18 GHz) has very low SWR; <1.3, 10 to 30 MHz, <1.15, 30 MHz to 5 GHz <1.25, 5-18 GHz and changes little from ON to OFF condition. Further, the nominal ENR of 15.2 dB is measured and charted individually at 20 cardinal frequencies on each noise source. Root sum of squares (RSS) uncertainties of those ENR calibration points varies from ±0.1 dB at 10 MHz to ±0.19 dB at 18 GHz.

The new high-accuracy measuring technique depends on the HP 436A Digital Power Meter operating under desktop computer control to measure Y-factor and compute noise figure. The system enhances accuracy by using the actual ENR furnished with each source. Y-factor uncertainties can be as low as ±0.04 dB and along with improved ENR accuracy and lower mismatch, overall uncertainties can be below ±1.0 dB. In addition, the computer can tune the down-converter local oscillator to provide the sweep frequency. Bias power for the noise source comes from a standard programmable power supply.

The 346B source improves measurements with traditional automatic noise figure meters too. The well-known HP 340B/342A furnishes bias power through an HP 11711A Noise Source Adapter. Most non-HP noise meters which supply 28 ±1V power are also compatible.

Obtain all the details by checking **G** *on the HP Reply Card.*

+8 dBm synthesized signals from 2 to 18 GHz

Hewlett-Packard's 8672A Microwave Synthesized Signal Generator is now available with Option 008, +8 dBm minimum specified output power from 2 to 18 GHz. This increase in leveled output makes the instrument more useful in applications such as local oscillator service or where power must be delivered at the end of a long cable.

For applications requiring even higher power, +10 dBm specified output can be achieved by combining Option 008 with Option 001 (deletion of the calibrated output attenuator in the 8672A).

For more information, check H *on the HP Reply Card.*

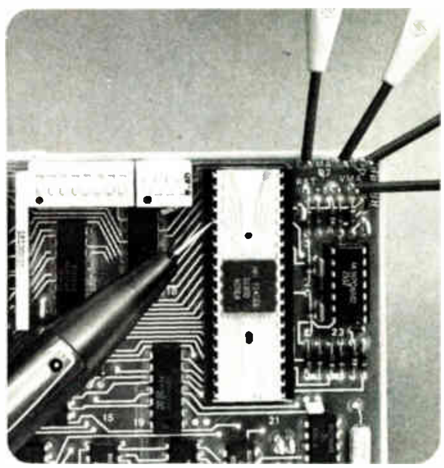
Can you retrofit your product for signature analysis?

If design is already frozen on your microprocessor-based product, and you thought it was too late to consider signature analysis testing, check out a new HP Application Note. There may be a possibility of retrofit.

Signature analysis, S.A., is a new technique for troubleshooting microprocessor-based products to the component level. It uses HP's 5004A Signature Analyzer to detect and display the unique digital signatures associated with the data nodes in a circuit under test. By comparing these actual signatures to the correct ones, a troubleshooter can backtrace to a faulty node. Some features are usually designed into a product to allow full testability and serviceability via signature analysis. However, by using the "free-run" technique, many manufacturers are discovering that they can retrofit their products for partial S.A. testability—say 50%-75%. This margin often makes a big difference in cutting the high cost of digital troubleshooting.

Free-running retrofit is the subject of one section of the new HP Application Note #222-2 *Application Articles on Signature Analysis*. Other sections detail case histories of successful S.A. designs selected from the 50 HP products that now use S.A.

Check **I** *on the HP Reply Card for your complimentary copy of Application Note #222-2. Check* **J** for a full S.A. information package, including three application notes and data sheet on the HP Model 5004A Signature Analyzer.



To check out a Signature Analysis retrofit for your microprocessor board, read HP Application Note #222-2.

HP-41C, a whole new standard in personal calculators

HP-41C is a synthesis of the latest state-of-the-art technology and HP human engineering. It's powerful, easy to use and flexible enough to solve a multitude of problems.

The new HP-41C, the most powerful handheld calculator HP has ever designed, can be converted into a personal calculating system by adding a series of companion peripheral devices. The HP-41C has alphanumeric capability, customized keyboard, continuous memory and enhanced programmability. Plus—when you need them: extra Memory Modules, an "extra smart" Card Reader, a Printer/Plotter, Application Modules and the Wand.

The Calculator

The HP-41C features over 130 functions. It offers you 400 lines of program memory or 63 data storage registers—expandable to over 2,000 lines or 319 registers. And, RPN logic for power, ease of use and efficiency.

It communicates. Alphanumeric capability lets you label programs, functions, variables and constants. The HP-41C utilizes a high resolution liquid crystal display (LCD) that is easy to read in the office or out in the bright sunlight.

Customized Keyboard. You can "customize" your HP-41C by reassigning any standard function, any programs you've written, or functions provided in plug-in options to any keyboard location you want. And change them any time you wish. Keyboard overlays are provided to notate these assignments.

Continuous Memory. Even when turned off, the HP-41C retains all your programs, data, and key assignments.

Enhanced Programmability. With your HP-41C, programming is simplified. With its alpha capability, programs can be labeled with easy-to-remember names.

This calculator delivers unprecedented capability for the money.

The System

Memory Modules store your programs and data. Each Memory Module plugs inside one of the calculator's four ports. Any one Module contains 63 data storage registers, or up to 400 lines of program memory.

The "extra smart" Card Reader plugs into one of the HP-41C ports and becomes an integral part of the calculator. It records your programs and data onto blank mag-cards. It lets you load programs in any order and accepts pre programmed HP-67/97 mag-cards. "Program Security" allows programs to be run but not reviewed or altered.

The Printer. The whisper-quiet thermal printer easily plugs into the calculator. Using batteries or ordinary house current, it prints upper and lower case alpha, double-wide characters, character plotting, and has adjustable contrast.

The Wand, a unique input device enters programs and data by reading "bar-codes" much like those found on many grocery items. The Wand and bar-coded programs will be available with HP-41C software in Spring 1980.

Application Modules is a growing library of preprogrammed solutions for a wide range of problems. Clinical Lab, Financial Decisions, Surveying and Stress Analysis to name a few.

Check **A** *on HP Reply Card for details.*

Highest performance frequency standard now lasts even longer

HP's 5061A Cesium Beam Frequency Standard with high performance option 004 provides the best, by two to ten times, in specifications that mean the most in critical applications.

Accuracy (incl. 0-50°C temp. and 2 gauss mag. field, ac/dc): $\pm 7\times10^{-12}$

Stability (fractional freq. fluctuation)

avg. time	stability
1s	5×10^{-12}
10s	2.7×10^{-12}
100s	8.5×10^{-13}

Settability (degree to which frequency can be set to match a reference:) $\pm1\times10^{-13}$ with degausser.

Despite this high accuracy, the 5061A is rugged too, having passed stringent U.S. military tests:

Shock: MIL-E-5400
MIL-T-21200, C.1
Vibration: MIL-STD 167-1
EMC: MIL STD 461

You get another benefit in HP Cesium Beam Standards, also: unmatched experience. We've been building them longer than anyone else, and they are the accepted standard in more places than any other primary, atomic, frequency standard. For example, it is the standard for timekeeping centers of more than 26 countries, for Loran C., for Omega and for other terrestrial navigation, satellite tracking, interplaetary navigation, radio astronomy and source communications.

For more details, check **K** *on the HP Reply Card.*

90,000,000 hours of Cesium Beam Frequency Standard reliability data— the longest in the industry—have now been accumulated by HP's units. And recent improvements have extended life of the optional high-performance beam tube.

High speed automatic data acquisition system for on-line computation, processing and control

Select from one of three desktop computers to obtain the language, display, memory and other features best suited for your application.

Hewlett-Packard's low-cost 3052A Data Acquisition System now offers a choice of three desktop computers which can provide a solution to data logging and data acquisition problems. Excellent in areas such as component tests, environmental monitoring, energy usage monitoring, production process monitoring, evaluation and quality assurance, the 3052A offers a measurement capability that includes both high-precision, low-speed measurement and high-speed moderate-precision measurements.

Computer controlled, the HP 3052A can measure physical/electrical parameters in the form of AC/DC and resistance at speeds up to 23 rds/sec. Higher speed measurements (up to 5000 rds/sec) can be made with 3½-digit resolution on a single channel. Four-terminal input, microvolt resolution and longterm stability enable precise temperature measurements.

A choice of computers which are friendly, interactive, fast, and powerful, allows you to select the best computer for your data acquisition application need. HP's 9825S computer has an alphanumeric display, uses HPL language (similar to BASIC and FORTRAN) and has 23K byte memory. The HP 9835A has a CRT display, uses BASIC language with 50K byte memory, expandable to 248K bytes. HP's 9845A with full graphic display, also uses BASIC with 82K byte memory.

The HP 3052A Data Acquisition System is fully integrated, tested, verified, and specified as a system with complete software and documentation supplied.

Call your HP instrument field engineer today to discuss your application, or check **L** *on the HP Reply Card for literature.*

New low-cost option extends counter frequency range to 1 GHz

Now, Hewlett-Packard's 5315A/B Universal Counters extend their 100 MHz frequency measurement range to 1 GHz with Option 003 for only $250 more. This expanded measurement range opens up uses for the 5315A/B in new areas of design, production and maintenance of equipment for communications, navigation, FM and TV broadcasting.

The 5315A/B also measures low frequency communications pilot tones to a high resolution as it measures input waveform period and inverts the measurement to display frequency directly. The 5315A/B achieves a resolution of at least seven digits (0.0001%) in a measurement time of only one second, from 1 Hz up to 1 GHz.

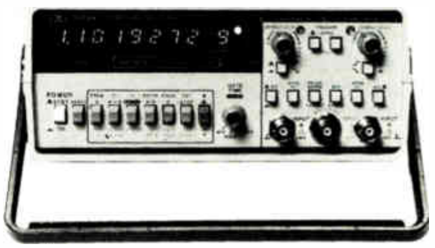
Communications Applications

Also enhancing its usefulness in communications applications are:

- Very low electrical noise (RFI/EMC) for testing sensitive receivers.
- Battery pack option with built-in charging circuits for portable field use.
- High stability time base option where requirements call for extended time between calibration and for greater freedom from effects of ambient temperature changes.

The 5315A/B without extra cost options has measurement functions of frequency, frequency ratio, period, period average, time interval, time interval delay, time interval average and it will totalize events. Model 5315B is the 5315A in a metal, rack-mountable package.

For more information, check **M** *on the HP Reply Card.*



The high resolution of HP's 5315A/B Universal Counters is now brought to the communications market with a new 1 GHz frequency option.

Certified 100% error-free data cartridge available from HP

Certified 100% error-free at time of shipment, the Hewlett-Packard 98200A Data Cartridge is a compact, magnetic-tape device offering reliable data storage for Series 9800 Desktop Computers and HP 264X Series Display Terminals.

To certify superior performance, HP automatically tests each cartridge over its entire tape length by recording and reading back tightly-packed data bits on both tracks.

Designed, manufactured and supported by HP, the 98200 offers quality features that bring out the best performance in HP desktop computers—

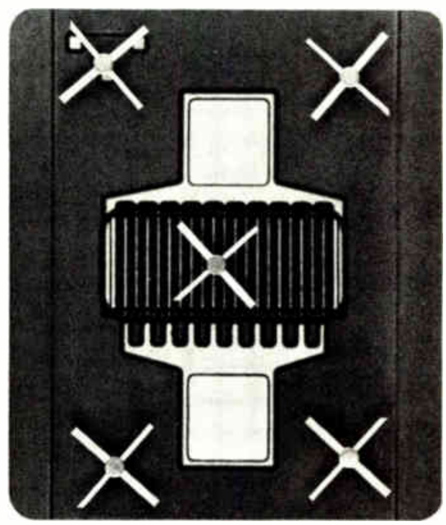
- As much as 5.4 megabits of unformatted data can be stored on the 98200's 42.7 m (140 ft) of 3.8 mm (0.150 in) wide tape, assuming a recording density of 1,600 bits per inch.
- Speeds of up to 90 inches per second make short access times and fast transfer rates possible.
- Acceleration rates of up to 2,000 inches/second² are possible, helping to keep start/stop distances to a minimum.

Model 98200A is one carton of five cartridges individually boxed. An unlabeled version, Model 98200U, and quantity discounts are available.

For further information, check **N** *on the HP Reply Card.*

HEWLETT-PACKARD COMPONENT NEWS

Two new microwave transistors with guaranteed gain and noise figure for 2 GHz designs



New, smaller packaged bipolar transistors offer guaranteed noise figure and gain for first and intermediate stages of amplifier designs at 2 GHz.

Two new small signal NPN bipolar transistors, both using a rugged 70-mil diameter alumina package, have been optimized for designs at 2 GHz. The HXTR-2102 is a general purpose transistor with minimum tuned gain (guaranteed) of 13 dB and typical linear output power of 100 mW (20 dBm).

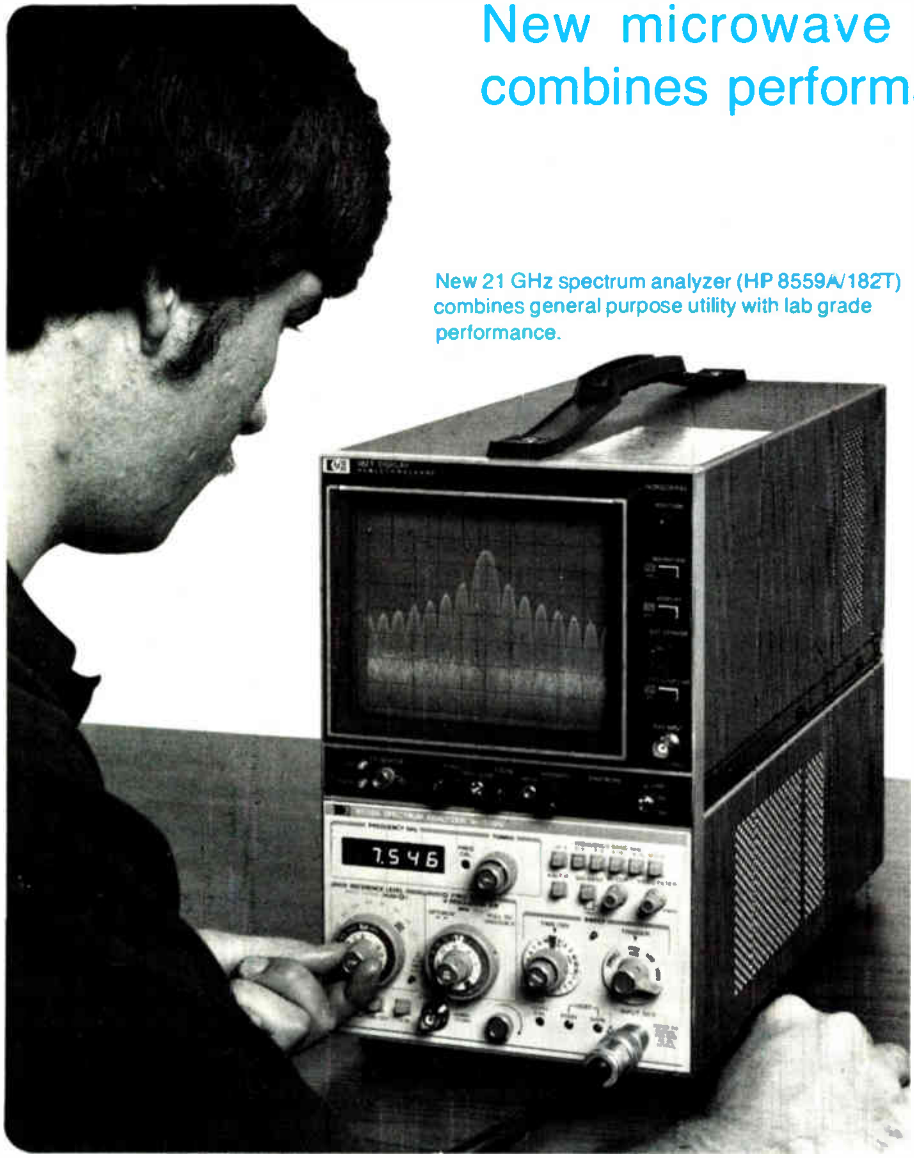
The economical HXTR-6106 is a low noise transistor that can be used in a wide variety of low noise communications, radar and ECM applications. Characterized from 500 MHz to 6 GHz, it has a guaranteed noise figure of 2.7 dB maximum at 2 GHz, with a typical associated gain of 11.5 dB.

Both of these transistors are offered in the small HPAC-70GT, a rugged, hermetically sealed metal/ceramic package. The size of the package ensures that the loss in gain due to package parasitics is minimal and that circuit designs make efficient use of available space.

The HXTR-2102 and HXTR-6106 complete the family of new HP transistors specified at 2 GHz. These two transistors are functional replacements for the similarly packaged HP 35800 series devices. However, the new devices are lower priced with superior performance characteristics.

Check **O** *on the HP Reply Card for a data sheet.*

New microwave spectrum analyzer combines performance and economy



New 21 GHz spectrum analyzer (HP 8559A/182T) combines general purpose utility with lab grade performance.

Attractive performance, attractive price, convenient size and weight, and pleasantly easy to operate—all of these statements describe the new HP 8559A Microwave Spectrum Analyzer. Covering 10 MHz to 21 GHz, the 8559A plugged into the HP 182T Display Section weighs just 18 kg (40 lbs). Amplitude measurement range is from −111 to +30 dBm, and the distortion-free dynamic range is >70 dB. Resolution bandwidths from 1 KHz to 3 MHz are provided. The 8559A has high frequency accuracy which is complemented by a 5-digit LED readout with 1 MHz resolution.

Most measurements made with the 8559A only involve the use of three controls: "Tuning,"to position the signal of interest; "Frequency Span," to zoom in on the signal for detailed analysis; and "Reference Level," to determine the signal's amplitude. Other functions such as Resolution, Video Filtering and Sweep Time are automatically adjusted to their proper settings for the selected frequency span.

The performance, size, convenience and price (it's HP's lowest priced microwave spectrum analyzer) of the 8559A/182T all contribute to its value in lab, production test and field test applications.

If you're interested in further details, please check **P** *on the HP Reply Card.*

East-4 Choke Cherry Road, Rockville, MD 20850, Ph (301) 258-2000
South-P.O. Box 10505, 450 Interstate North Pkwy., Atlanta, GA 30348, Ph. (404) 434-4000.
Midwest-5201 Tollview Dr., Rolling Meadows, IL 60008, Ph (312) 255-9800.
West-3939 Lankershim Blvd, North Hollywood, CA 91604, Ph. (213) 877-1282.
Europe-Central Mailing Depot., P O. Box 529, Amstelveen-1134, Netherlands, Ph. (020) 47 20 21.
Japan-Yokogawa-Hewlett-Packard Ltd., Ohashi 29-21 Takaido-Higashi 3-chome Suginami-ku, Tokyo 168, Ph. 03-331-6111.

HEWLETT hp PACKARD

MEASUREMENT COMPUTATION news
product advances from Hewlett-Packard

September/October 1979

New product information from

HEWLETT-PACKARD

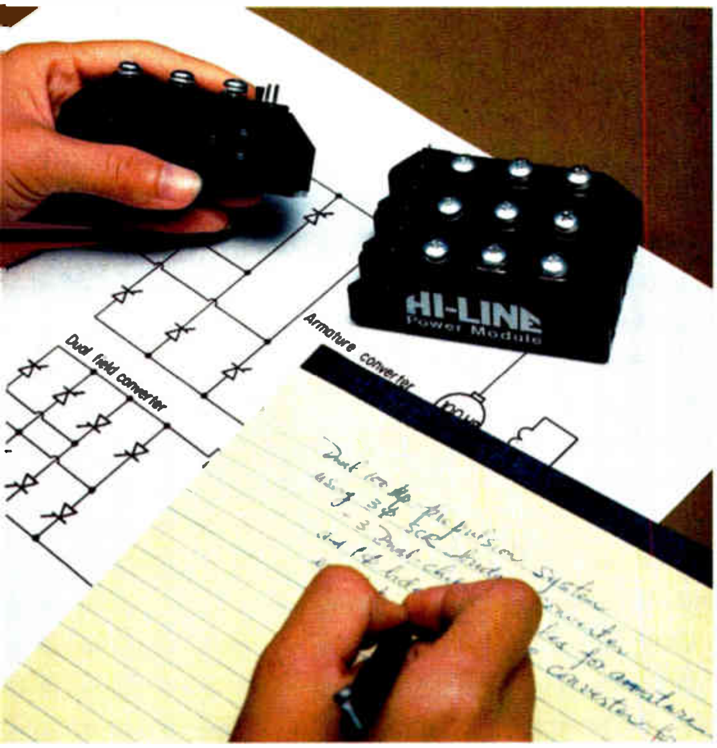
Editor:
Bojana Fazarinc

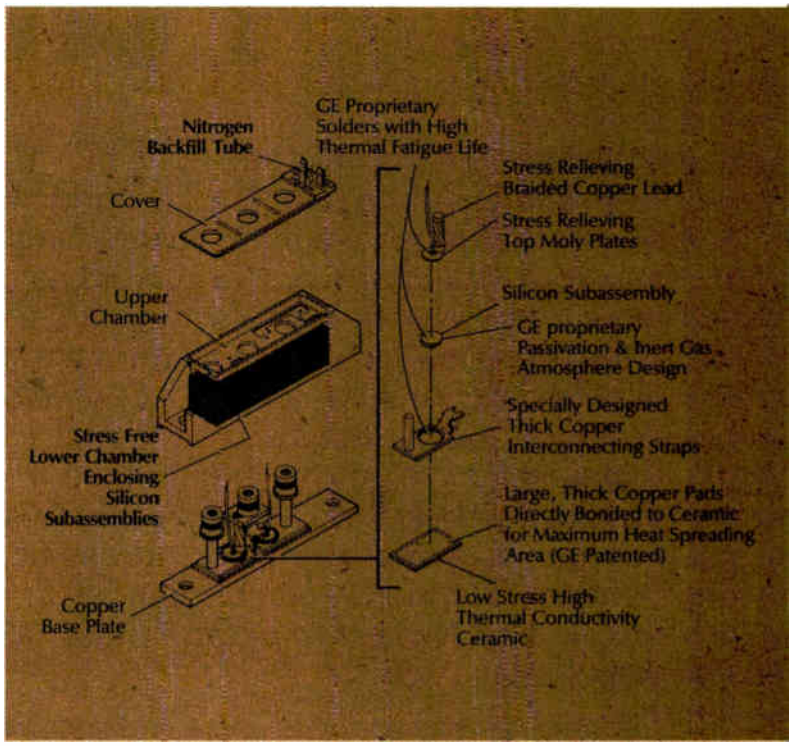
Editorial Offices:
1507 Page Mill Road
Palo Alto, California, 94304 U.S.A.

00985

What makes the HI-LINE™ power module different from all the rest?

General Electric packaging technology.





Most power modules look alike. To tell the difference you have to look inside. See how it's designed and put together. See the inside difference.

Only the HI-LINE™ power module has General Electric packaging technology. And only the HI-LINE™ power module can offer these three design features:

- **Low thermal resistance:** Obtained by placing the semiconductor elements closer to base plate and heat sink. Large, thick copper pads directly bonded to ceramic for maximum heat spreading. Cooler running increases device reliability.
- **Low mechanical stress:** Achieved by using a cavity-type package and unique dual chamber design. Epoxy-filled upper chamber seals housing. Controlled gas chamber encloses silicon subassemblies and is free from stress forming encapsulants and degrading gases. The advantage is better blocking life and thermal cycling capability.
- **Extended blocking life:** The device is vacuum baked and internal atmosphere is extracted through an evacuation tube. The cavity is then backfilled with dry nitrogen resulting in a tightly controlled inert atmosphere. The evacuation tube is then sealed. A GE proprietary passivant is applied to the element to extend blocking life for greater reliability.

HI-LINE™ model W4DC55 contains two isolated phase control SCR's in a center tap configuration for motor controls, power conversion and lighting controls.

HI-LINE Power Module—Model W4DC55 Specifications

Voltage—300-1200 Volts

I_T (Avg)—55 Amps } Baseplate temp. of 85°C

I_T (RMS)—90 Amps } Baseplate temp. of 85°C

I_{TSM}—1000 Amps (60 Hz half-sine at 125°C)

Fusing current—4,150 A^2S (8.3-ms surge, half cycle)

Isolation blocking voltage—2500 V RMS

Discover the inside difference for yourself. Contact your nearest GE electronic sales office, authorized distributor or write General Electric Co., West Genesee St., Box 14, Auburn, N.Y., 13021. For specific questions or consultation call (315) 253-7321, ext. 375 or 458.

In Europe, contact the International General Electric Company of New York, Dundalk, Ireland (042) 32371, telex 33816.

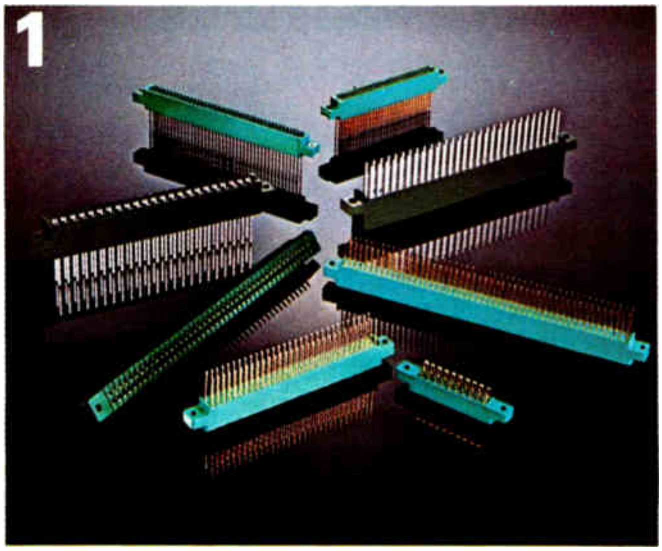
222-18

GENERAL ELECTRIC

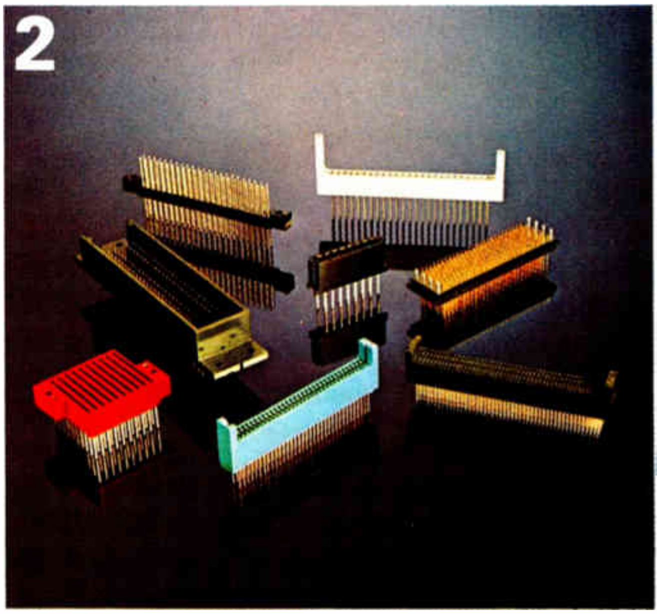
TM: Trademark of General Electric Company

Good
run in our

Our family members have one thing in common, a good solid background. It all started when we began producing custom PC connectors for major electronic equipment manufacturers. We now produce millions of custom and standard connector assemblies yearly. Many of them have become industry standards. We've also expanded our product family with a complete line of flat cable and connectors, press-fit connectors, and a total backpanel capability. Now, step up and meet the family.



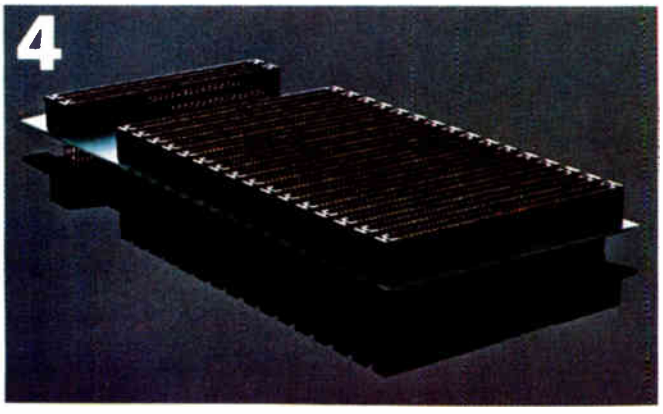
1 Our family has the edge in off-the-shelf PC connectors, with the broadest line of available products in the industry. We've got fast delivery, competitive prices, and total flexibility in connector design. Regardless of insulator type, contact design, or plating, Sylvania has the right connector for your application.



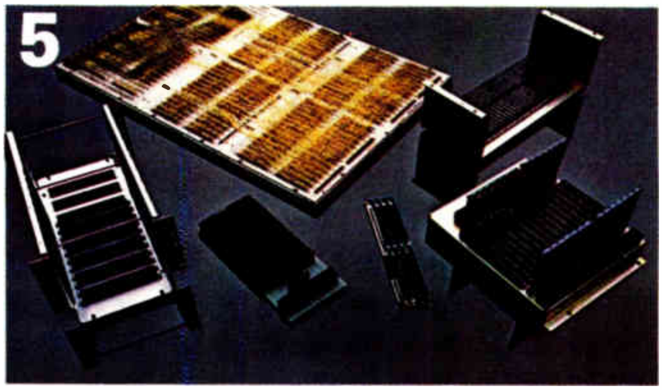
2 Special connectors are an old family custom. Our years of experience include solving the most challenging design problems involving numerous critical tolerance components. When you look inside the enclosure of a business machine, a mini or main-frame computer, a large telephone switching system, or an industrial controller, chances are that you'll see our connectors. Our systems consistently provide the reliability, useful life, and feasibility you need, at a price you can afford. If you have a connector application that is a problem, we're ready to apply our special skills and knowledge to its solution.

connections family.

3 A flat answer is exactly what you get for your mass termination needs from our family of flat-cable connector products. If lowest installed cost with maximum reliability is your requirement, a complete line of standard or stackable sockets, PCB connectors, and headers are available for quick delivery. Additional savings and ease of assembly are realized with our universal termination tool system. Whether you need a complete zero-defect assembly or only component parts, we can fill your application.



4 Our stored energy contact keeps us uptight in any printed wiring board solderless backpanel application. By using our special press-fit connector assemblies, we optimize the benefit that compliant connector technology can bring you. The result is maximum electrical continuity and mechanical retention. With our approach, all you do is plug the connectors into your PC board application.



5 To bring this all together, let the backbone of your system be our total backpanel assembly. Again, we offer the complete flexibility of supplying backpanels in either bits and pieces, or as a complete zero-defect package. From contact to wiring to total final testing, you'll have single-source responsibility, maximum quality and reliability, and time and money saved.

Now that you've met our entire family, why not turn it into a close relationship? Just call or write GTE Sylvania, CPO, Box 29, Titusville, Pennsylvania 16354. Phone 814-589-7071.

SYLVANIA GTE

Circle 29 on reader service card

Meetings

Semiconductor Test Conference, IEEE, Cherry Hill Hyatt House, Cherry Hill, N. J., Oct. 23–25.

Newport Conference on Fiber-Optic Markets, Kessler Marketing (22 Fairwell St., Newport, R. I. 02840), Sheraton Islander, Newport, Oct. 25–26.

New Directions in Command, Control, and Communications Systems and Technology, American Institute of Aeronautics and Astronautics (Box 91295, Los Angeles, Calif. 90009), Shoreham Americana, Washington D. C., Oct. 25–26, and Pacifica Hotel, Los Angeles, Nov. 15–16.

Optical Signal Processing for C³I (Command, Control, Communications, and Intelligence), Society of Photo-Optical Instrumentation Engineers (Box 10, Bellingham, Wash. 98255), Marriott Hotel, Boston, Oct. 29–30.

NCF–NEC/79—National Communications Forum/National Electronics Conference, National Engineering Consortium Inc. (Oak Brook, Ill.), Hyatt Regency O'Hare, Chicago, Oct. 29–31.

Autofact II—The Automated, Integrated Factory of Tomorrow Conference and Exposition, Society of Manufacturing Engineers (Detroit, Mich.), Cobo Hall, Detroit, Oct. 30–Nov. 1.

Interface West/79—Third Annual Data Communications, DDP and Office Automatic Systems Conference, Interface West (Framingham, Mass.) *et al.*, Anaheim Convention Center, Anaheim, Calif., Oct. 30–Nov. 1.

64th Convention, Audio Engineering Society Inc. (60 East 42nd St., New York, N. Y. 10017), Waldorf Astoria, New York, Nov. 2–5.

13th Annual Asilomar Conference on Circuits, Systems, and Computers, IEEE the Naval Postgraduate School, and U. of Santa Clara, Calif. Asilomar Hotel and Conference Grounds, Pacific Grove, Calif., Nov. 5–7.

Midcon/79 Show and Convention, IEEE and Electronic Conventions Inc. (El Segundo, Calif.), O'Hare Exposition Center and Hyatt Regency O'Hare Hotel, Chicago, Nov. 6–8.

Productronica/79—Third International Trade Fair for Manufacturers in Electronics, (Postfach 12-10-09, D-8000, Munich 12), Munich Fair Grounds, Nov. 6–10.

Ninth Annual Fall Conference on Consumer Electronics, IEEE, Ramada O'Hare Inn, Des Plaines, Ill., Nov. 12–13.

Concepts and Requirements for Battlefield Interdiction in Europe, Electronic Industries Association *et al.*, Institute for Defense Analysis auditorium, Arlington, Va., Nov. 13–14.

International Technical Symposium, International Society for Hybrid Microelectronics (P. O. Box 3255, Montgomery, Ala. 36109), Bonaventure Hotel, Los Angeles, Nov. 13–15.

International Micro and Mini Computer Conference, IEEE *et al.*, Astro Village, Houston, Nov. 14–16.

Non-Ionizing Radiation Symposium, American Conference of Governmental Industrial Hygienists (2205 South Rd., Cincinnati, Ohio 45238), Capitol Hilton Hotel, Washington, D. C., Nov. 26–28.

Short courses

Hall Effect Commemorative Symposium, Nov. 13, Johns Hopkins University. Write to JHU's Department of Physics/Department of Electrical Engineering, Baltimore, Md. 21218.

Microprocessor Control of Power Electronic Systems, Nov. 13-16, University of Missouri-Columbia. Write to Engineering Conferences, 1020 Engineering Building, Columbia, Mo. 65211

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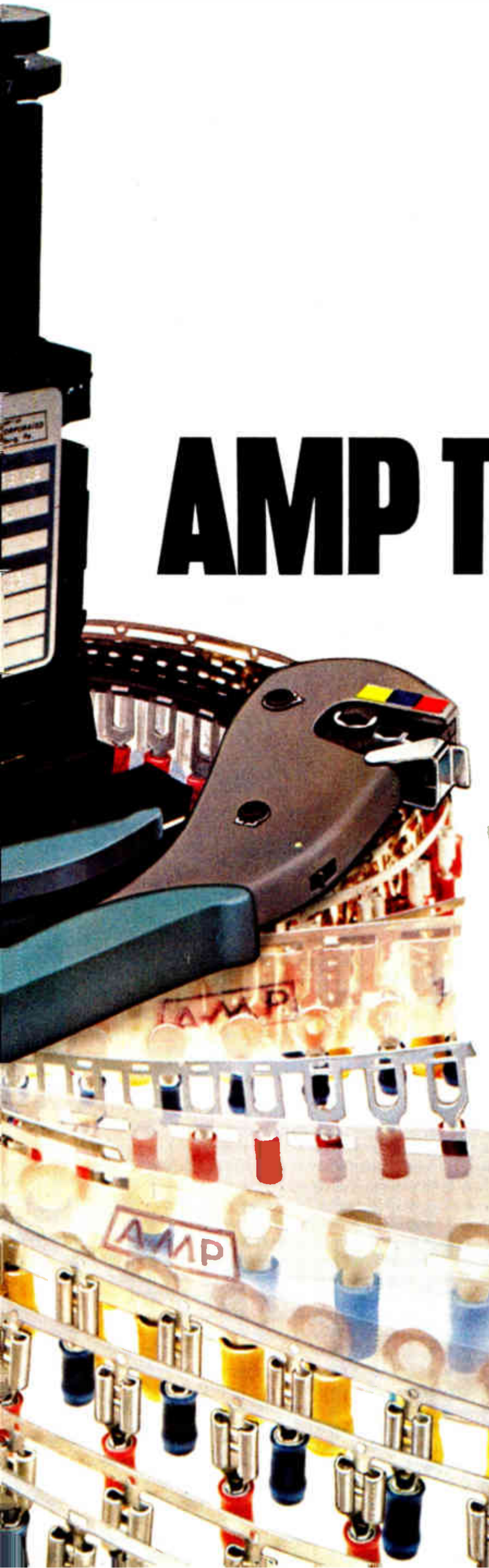

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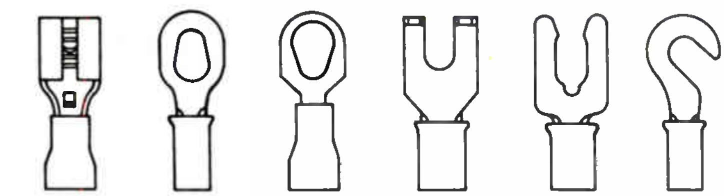

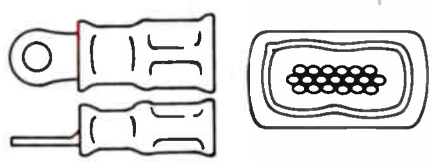

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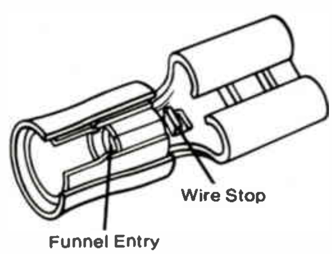

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Circle 33 on reader service card

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For technical data circle No. 34

Electronics newsletter

New line of mainframes due from Honeywell

Honeywell Information Systems Inc. in Waltham, Mass., will fulfill its promise to expand its mainframe line when it unveils four new 36-bit large-scale mainframe computers, and a new operating system. The biggest of what will be called the DPS-8 series, the DPS-8/70, is **almost twice as powerful as any computer currently made by the company** and is expected to be even more powerful than Honeywell's ill-fated attempt last year to expand its line with the Level 66 model 85 computer. And although the company last year said it had ironed out problems with its current-mode logic, it has chosen Schottky TTL for the new models. Prices range from about $400,000 to $5 million, and the new GCOS-8 operating system will be compatible with existing software.

Electronic Arrays to assemble 16-K RAMs from NEC

Nippon Electric Co. will start making 16-K dynamic random-access memories in February at its wholly owned subsidiary in Mountain View, Calif., Electronic Arrays Inc. Initially, only assembly and testing will be performed on 100,000 devices per month. **Front-end processing, including diffusion, will be added in the future.** Nippon Electric claims it will be the first Japanese company to fabricate 16-K dynamic RAMs in the U. S.

A 16,000-ft^2 assembly line will be installed to handle the RAMs and other products. Electronic Arrays has done its own front-end processing, with assembly in Southeast Asia; the new line will enable the company to assemble about half of its own devices, cutting lead time for customers in the U. S. The company now has about 400 employees and will add another 100 by February in preparation for the start of assembly operations.

CTS moving into communications component arena

CTS Corp. of Elkhart, Ind., is joining other component makers such as Methode and Molex in moving away from Japanese-dominated consumer electronics markets and into communications gear. Once a primary supplier of variable resistor networks to Midwestern television assemblers, CTS expects volume to drop $10 million this year. But "we do not have much more business to lose in that particular market segment," remarks Robert Hostetler, executive vice president of the company, which expects total sales of $180 million [*Electronics*, May 24, p. 102]. To compensate, **the company has a new design for an over-the-air encoder-decoder for the pay-television market** and a new contract to build another type of decoder. In addition, a new insert-molded variable resistor, produced in a continuous strip on automated equipment, is now in small volume production: CTS plans to double resistor sales to $50 million within two years. More assembled telecommunications products are coming, too, Hostetler says, while sales of sensors for automotive electronics applications should grow to $25 million by 1982, compared with more than $1 million now.

Borg-Warner going head on with Exxon in motor market

Going into direct competition with Exxon Corp., Borg-Warner Corp. of Chicago has developed a microcomputer-controlled inverter for ac motors. **Production of the inverter, the CF-1000, will begin immediately** at the company's Morse Chain division. Borg-Warner executives point out that, although Exxon's device promises twice the energy savings of theirs, it is not scheduled for production until 1982. Borg-Warner's, on the other hand, is not only in house and ready to roll off the lines, but is also backed by two and a half years of field service. Exxon is engaged in a controversial effort to take over Reliance Electric Corp. to give it a manufacturing base.

Electronics newsletter

IBM unveils more colorful and less costly terminals . . .

Expanding its widely used 3270 family of cathode-ray–tube data terminals, IBM Corp.'s Data Processing division in White Plains, N. Y., has introduced the high-end 3279 color display station, the 3287 color printer, and the budget-priced 3101 display and 3102 printer. **The new 3279, which can display up to seven colors on its 14-in. screen, will be available in the second quarter of 1980** at prices starting at $4,300. With purchase prices of $1,295 to $1,520—almost half those of the current IBM line—the new 3101 is the company's first teletypewriter-compatible unit that can be connected to computers without an intermediate controller.

. . . and typewriter with microprocessor

IBM's Office Products division is calling its new microprocessor-based IBM Electronic Typewriter 75 its **"most significant typewriter announcement since the Selectric."** Using 36-K random-access memory chips, the unit stores 7,500 characters, optionally expandable to 15,500 characters, for documents, phrases, margins, and tabulations. The Franklin Lakes, N. J., division will start deliveries of the $2,075 machine later this year.

HP develops new generations of SOS devices

While some chip makers eye complementary-MOS-on-sapphire technology with suspicion, Hewett-Packard Co. is already into its second generation of products, one that is 50% denser, with an even tighter third process in the works. HP's priorities for C-MOS on sapphire include high-density random-access memories, cache static RAMs with bipolar-equivalent speeds, and high-density read-only memories several times faster than anything else available. **Convinced that C-MOS-on-sapphire's speed-power product beats both n-MOS and bulk complementary-MOS,** HP has 60 parts in production, going into more than 60 company-wide products such as central processing units, controllers, and interface chips, with more in design. In production is a 16-bit microprocessor, with a 32-bit device a possibility.

Two Ward's stores to sell computers from two makers

While Sears, Roebuck & Co. and J. C. Penney Co. are mounting a broad-based home-computer marketing effort [*Electronics*, Sept. 27, p. 33], Montgomery Ward & Co., Chicago, is taking it slowly: this month the Mobil Oil Corp. subsidiary opens two computer stores **as a test of the mass-marketing appeal of hardware from Ohio Scientific Inc. in Aurora, Ohio, and Interact Electronics Inc.** of Ann Arbor, Mich. A Houston, Texas, store will feature several models of the $600-and-up Interact line, which was introduced last year and features a full keyboard and integral tape drive. A St. Paul, Minn., store has the low end of the Ohio Scientific line. Unlike Sears, though, Ward will put no computer ads in its catalog.

Addenda

When IBM Corp. made its first venture into the debt market last month, saying it planned to offer $1 billion in debt securities, industry observers said the borrowing confirmed the tremendous demand for the new 4300 computers. **They also saw the move as an indication that IBM is expanding production in preparation for the announcement of the top-of-the-line H series. . . . Texas Instruments Inc. plans to begin building in 1981 a 600,000-ft² plant on 113 acres in Colorado Springs, Colo.** It will be operated by the Equipment Group, which handles most of the Dallas company's big Government and military contracts.

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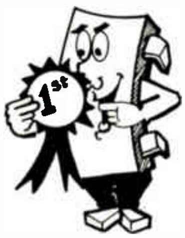

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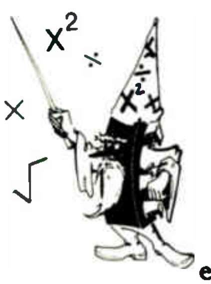

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Electronics review

Significant developments in technology and business

Signal processor for speech synthesis is programmable

by William F. Arnold, Palo Alto bureau manager

Chip set will work with variety of vocal tract models; system to which it belongs converts text to speech

No doubt about it: speech synthesis is rapidly becoming practical, thanks to the application of large-scale integration. The latest example is Telesensory Systems Inc.'s realization of a programmable digital signal processor in two LSI chips.

Because it is programmable, the PDSP will simulate a variety of mathematical models of the vocal tract, such as linear predictive coding and formant coding. It will be part of a text-to-speech system producing as many as 200 English words a minute, primarily for blind persons. It could also vocalize computer outputs and be used in telecommunications systems.

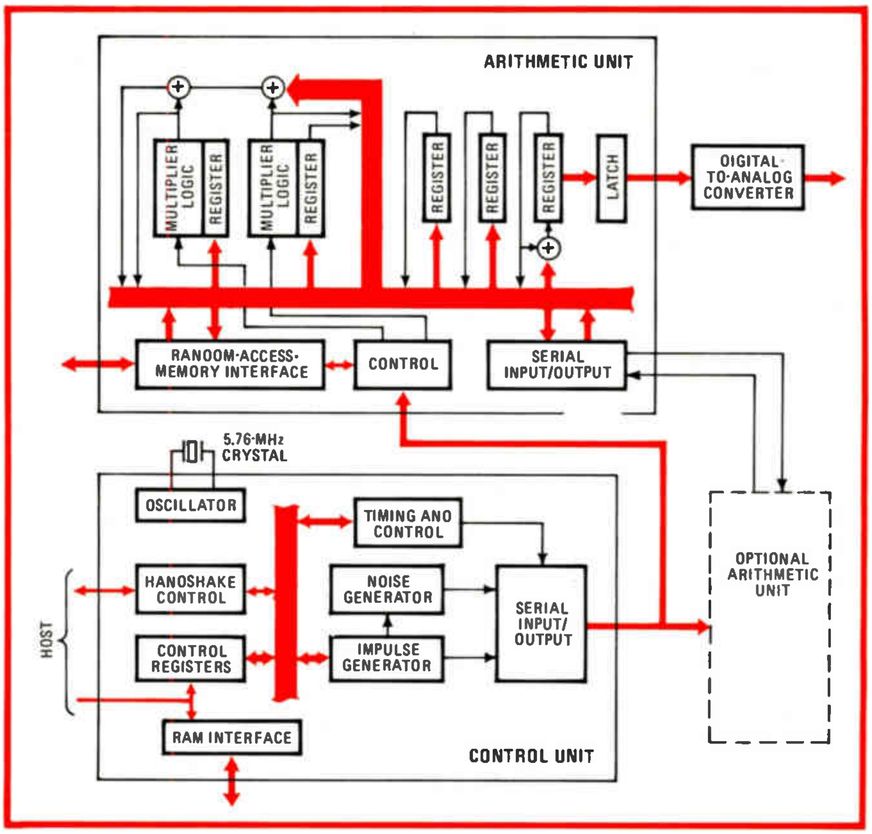
System. The Palo Alto, Calif., firm's system begins with an optical character reader that produces an ASCII-formulated text. A microprocessor-based module converts this character stream into phonemes, byte-encoded basic elements of speech, at a rate of several thousand bytes a minute. A second microprocessor (the "host" in the figure) translates the phoneme string into a sequence of control parameters for the vocal tract model in use.

In real time, the PDSP [*Electronics*, Aug. 31, 1978, p. 116] uses intricate algorithms to provide subtle speech characteristics, says James Caldwell, project leader for the maker of electronic products for the blind. Its output goes to a digital-to-analog converter and then to a loudspeaker. The first chip, the control unit in the figure, is a high-speed data-transfer and buffer unit that also synchronizes the data stream for the second chip, the arithmetic unit. Caldwell notes that "a vocal tract model is essentially a programmable filter capable of approximating the frequency response of the human vocal tract," so the arithmetic chip is in effect a specialized programmable digital filter.

"Every 100 microseconds it produces one 10-bit sample of the speech waveform," he says. This translates into 10,000 samples per second and yields a speech signal bandwidth of 5 kilohertz. It is possible to add a second arithmetic chip, enabling the PDSP to handle more complex vocal tract models.

Another. The chip set is not the first LSI voice synthesizer—Texas Instruments Inc., for one, has its three-chip set [*Electronics*, Aug. 31, 1978, p. 109]. But the TI synthesizer is not programmable, working only with linear predictive coding.

Telesensory Systems expects to



Synthesizing speech. Working with a host microprocessor, Telesensory Systems two-chip digital signal processor produces speech from phonemes encoded from a text.

see silicon in December from a supplier Caldwell will not identify. The chips will be in standard n-channel MOS for its speed and density, although details such as chip size and cost remain secret.

Caldwell does report that the PDSP chip set will replace about 900 small- and medium-sized integrated parts on the breadboard, or about 100 or more off-the-shelf parts, "which would be costly and use a lot of power." Once the chips are realized, he expects something over a year to elapse before the text reader is introduced. **-William F. Arnold**

Companies

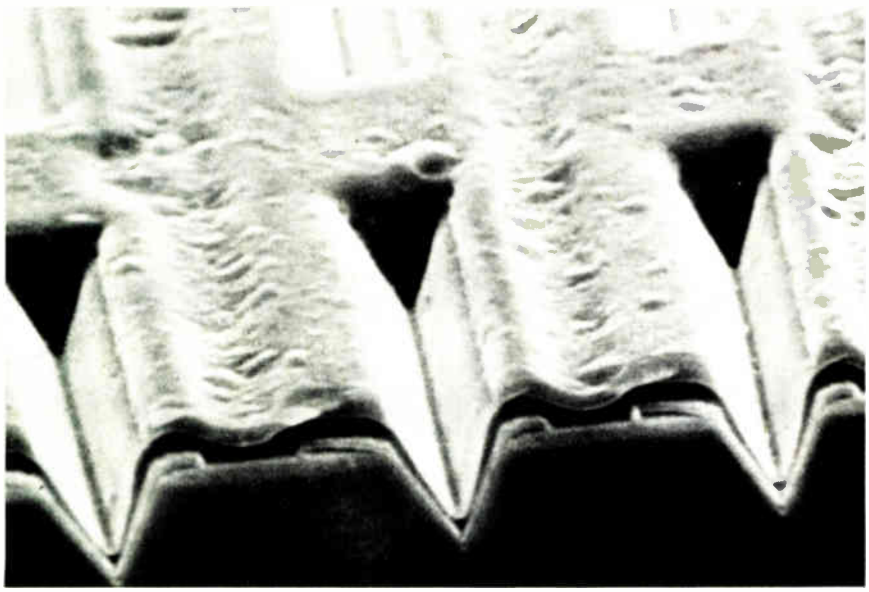
AMI backing off from V-MOS process, will push n-channel, C-MOS products

After several years of trying to build its dense but tricky vertical-groove MOS technology into a leading-edge process, American Microsystems Inc. has abruptly decided to turn to mainstream technology for growth. V-MOS will take a back seat to complementary-MOS and n-channel MOS processes and will be used only in AMI's lucrative custom work, its signal-processing peripheral device, and probably some microprocessor logic-support circuits.

"V-MOS had much more limited applications than we thought," says Carm Santoro, vice president for microprocessors and memories, which are most of the Santa Clara, Calif., company's standard parts business. Although V-MOS is a good logic technology, it has limitations in high-speed memories and cannot turn out erasable programmable read-only memories, he claims.

So long. The only V-MOS memory AMI is now making is a 64-K ROM for a Ford dashboard computer. Gone are a series of static random-access memories such as the 4-K 2147 and 2148 and a 16-K model in development.

Gone also is T. J. Rodgers, credited with being the guru of V-MOS [*Electronics*, Oct. 27, 1977, p. 94]. Rodgers maintains that his development work clearly demonstrated that V-MOS matches state-of-the-art n-channel MOS in speed and performance. "It's an excellent memory technique and perhaps a little bit better in random logic," he says.



Downgraded. The fate of V-groove MOS lies in limbo as American Microsystems retrenches. The relatively costly process proved unprofitable for commodity memory products.

However, others view V-MOS differently. "From the beginning, we didn't see it as a viable technology compared with H-MOS or other n-channel technologies," says Handel H. Jones, vice president of Gnostic Concepts Inc., a market research firm in Menlo Park, Calif. He approves AMI's move: "It should give them additional capacity and funding to get back on the right course. It's been a big cash drain."

But a semiconductor marketing manager from a competing firm surmises that AMI has not had the resources to develop both V-MOS and advanced n-MOS. "Unless they've kept up with scaled n-channel, they're going to have trouble bringing competing products into the marketplace," he says.

Insiders report that V-MOS moved too quickly from development to production, without enough testing and failure analysis. Also, it is about 25% more expensive a process than is, say, H-MOS, they claim.

In this year's first quarter, the process broke even on the production lines, but then it went through a yield bust that was "long, hard, and expensive to fix," recounts one insider. Totting up development and manufacturing costs estimated to be close to $12 million, management decided to throw in the sponge.

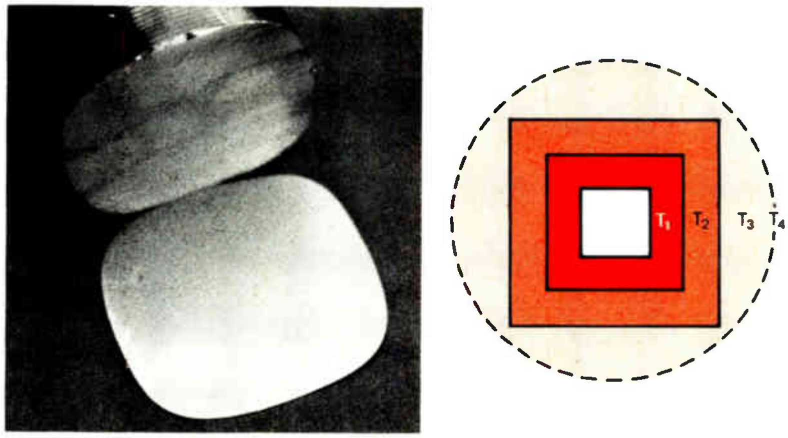
"Our standard products ran counter to what the company is good at," Santoro says. "We were trying to do what everyone else is doing, instead of what we do best."

Plans. Major strengths, he feels, are making logic parts in finely honed standard processes and responding quickly to market demands built up from the custom business that will be 75% of the firm's $100 million business this year. With the downgrading of V-MOS, microprocessors will take priority.

A block-structured family of n-MOS parts built around an 8-bit central processing unit should surface in 1981. Also planned is a family of C-MOS uncommitted logic or gate arrays for processing and telecommunications, as well as C-MOS microprocessors. **-William F. Arnold**

Photovoltaics

Motorola pulls square ingots



Going square. Motorola is getting close to square silicon ingots (left). To achieve perfect square growth, the thermal temperature zones in the melt must be square (right).

Since the bulk of the cost of a silicon solar cell is in the cost of the material, various techniques, such as the use of square ingots, are under study to get the most silicon for the money. Motorola Inc. is putting a new twist on Czochralski crystal-pulling to grow single-crystal ingots that are not quite square, but "we intend to get there," vows E. David Metz, director of the Phoenix research and development laboratories of the Semiconductor Products Group.

Square slices are sought for better solar collector packing. When round disks sliced from the usual cylindrical ingots are butted as close as possible on a solar panel, roughly 25% of the surface is bare of the energy-converting silicon material.

Of course the circles can be cut into squares for full coverage, but that means about 25% of the silicon is wasted. It cannot be thrown back in the melt because it is usually contaminated by that time.

Square die. Motorola uses a square die that acts as a thermal shaping device; the temperature zones on the melt surface are squarish. These zones, called isotherms, encourage the growing crystal to solidify into a square. Hence the ingot assumes a squarish cross section as it passes through the die as it is pulled from the melt.

Also, Motorola places the seed crystal with its (100) plane face down in the molten silicon. This orientation encourages growth of the cubic lattice structure that helps form a square ingot.

Motorola does not let the growing crystal touch the sides of the die, because the ingot must be rotated for even growth and distribution of any impurities present in the melt, says Metz. In contrast to the uniform rotation used to fashion cylindrical ingots, Motorola uses quick 90° turns.

The ingot remains stationary and aligned with the square die for about 15 seconds while it grows corners and sides. Then it undergoes a 2-s 90° rotation so as to be in line with the square die again for continued growth. This process continues until completion, and Metz says it takes about the same time to grow the square ingots as the round ones.

One challenge of the technique is the composition of the die material. Metz will say only that it is not metal but has the ability to react quickly to temperature changes in the melt. It still reacts too slowly to facilitate growth of a perfectly square ingot. "If at 1,400° we could control the [die] temperature to within a tenth of a degree, we'd have the problem licked," he adds.

Single crystal. One of the advantages of Motorola's scheme is that the resulting ingot is of single-crystal material, like any ingot pulled with the Czochralski method. Some companies dump molten silicon into a square mold to cast blocks of silicon [*Electronics*, July 10, p. 110, and Oct. 26, 1978, p. 68]. But this technique produces polycrystalline silicon with a lower solar-energy conversion efficiency.

Another approach is to pull thin silicon ribbons [*Electronics*, Oct. 27, 1977, p. 41]. But this demands complicated machinery, and the ribbons are not always single crystals. Therefore, Metz feels justified in predicting that the Motorola method "will be an efficient way to produce large-area solar cells."

Motorola's ingots are presently 2 inches on a side, and it intends to double that. Moreover, if the technique is perfected for photovoltaics, it may eventually be used for logic as well. **-John G. Posa**

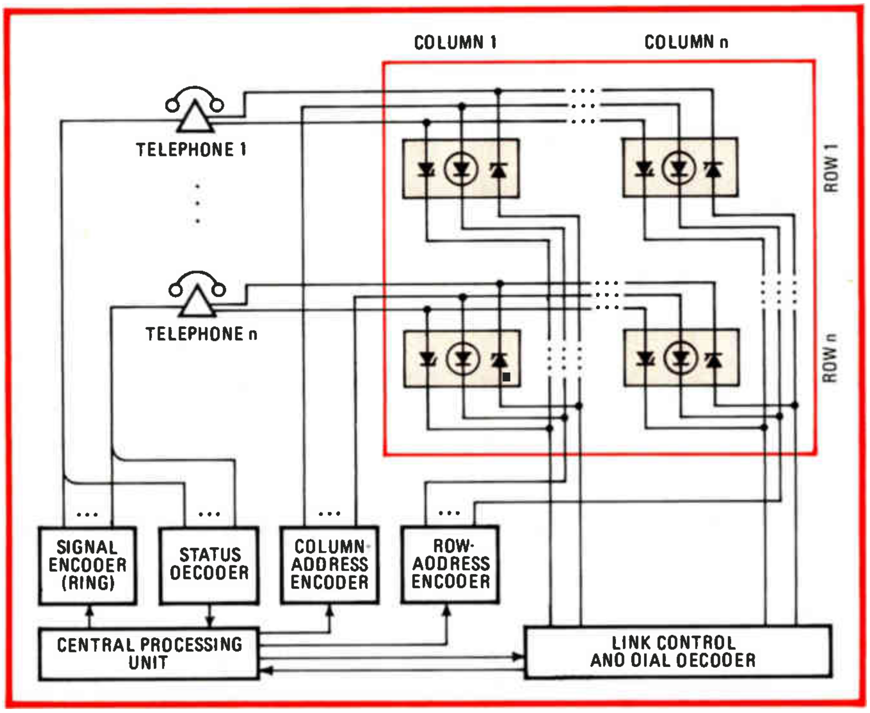
Communications

Solid-state crosspoint switches with light

With switching circuits going solid-state, makers of telephone equipment are looking for optoelectronic control of these matrixes. Just such a scheme is showing up in a system for offices with 5 to 75 handsets.

Optoelectronic control ensures that no noise is coupled between signal and control lines, because they are electrically isolated. Such arrangements are under study for the large switching matrixes found in phone company central offices [*Electronics*, March 1, p. 41].

In the new system, the interconnect portion uses a microprocessor-controlled solid-state switching matrix, says Thomas E. Feil, director of engineering for the manufacturer, Interconnect Planning Corp., New York. "The switching crosspoints each have silicon controlled rectifier chips, which are activated by a single



Light switch. Solid-state crosspoints (tinted) contain two SCRs and an LED controlled by a CPU. When the LED switches the SCRs to conduct, phone links are established.

light-emitting diode," he says.

To connect any phone in the system to another, the central processing unit in the figure pulses the anode high and the cathode low in the associated crosspoint's LED. This causes the two SCRs to latch, which in this setup means that both change from nonconducting to conducting.

Immediately, the CPU latches the crosspoint associated with the called phone onto the path. It clears the link by momentarily interrupting the current flow from the link control.

Easy match. Because the optoelectronic crosspoints operate at low impedance levels, they can be connected to the rest of the low-impedence telephone circuitry without the matching devices necessary with previous solid-state switches. Since there is no signal loss due to impedence mismatch, amplifiers are eliminated, and thus the sending and receiving capabilities of each phone are more uniform with those of all the others.

The crosspoint was designed by Feil, whose engineering background facilitated his work with Ed Rodriguez of Theta-J Corp., Woburn, Mass., to integrate the circuit onto a chip. The integrated circuit fits into a six-pin package insertable on a printed-circuit board. Theta-J builds similar optoelectronic devices for relay applications.

For now, the IC is built to switch the incoming pair of wires to one outgoing pair, but Feil says he is studying a one-by-four crosspoint chip, which would connect the incoming pair to a total of four systems. Development and production costs of the one-by-one crosspoint IC were such that it is put into the system for about $1 each, he says. **-Harvey J. Hindin**

Software

Chip would decode enciphered orders

A novel solution to the problem of software piracy is just emerging from the patent office: a microprocessor that executes enciphered programs. The proposed cryptomicroprocessor, as its inventor is calling it, has a circuit that deciphers each encoded instruction as it is being fetched for execution.

Software pirates would be unable to alter, disassemble, or copy the deciphered instructions because the processor would not yield them, says inventor Robert Best, a Seattle, Wash., programmer and systems analyst. No chip yet exists; in fact, he is looking for a manufacturer interested in developing one.

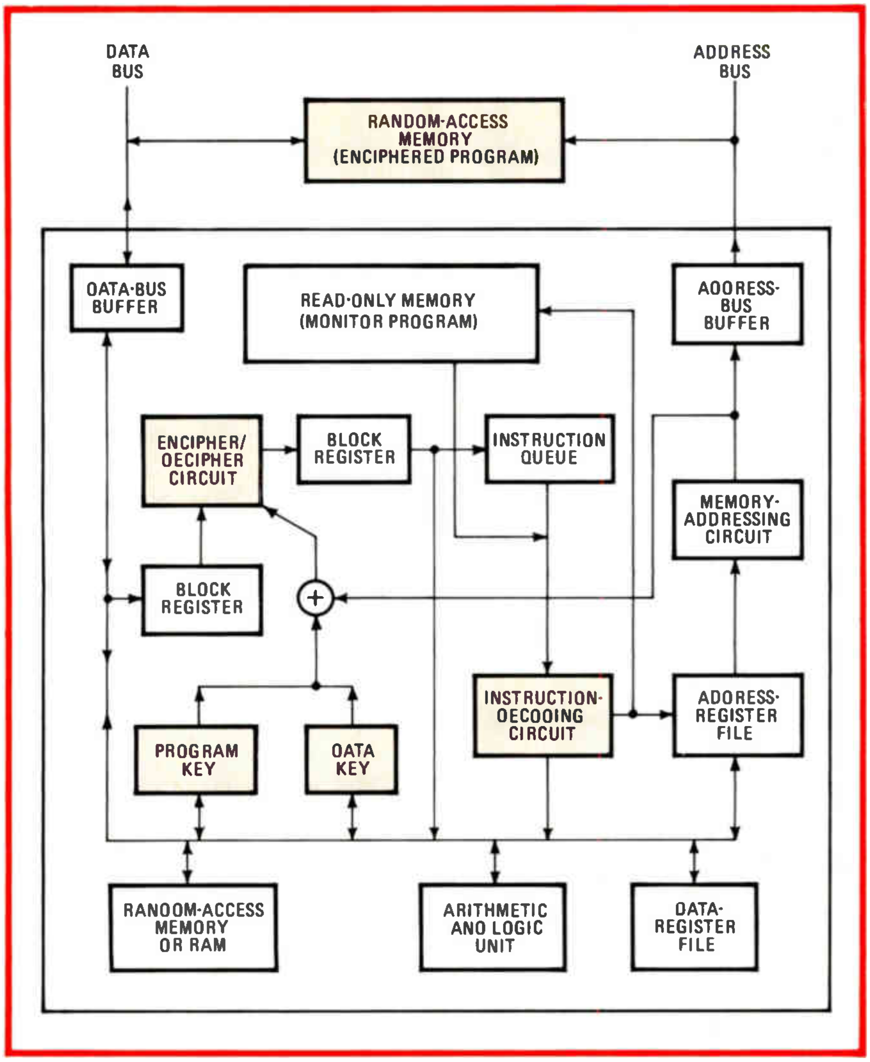
More software. By eliminating piracy risk with a relatively simple solution, the cryptomicroprocessor should encourage investment in proprietary software, Best predicts. A notable example would be programs for personal computers, an area where data-encryption devices are becoming available [*Electronics*, Sept. 13, p. 42].

An enciphered program is executed only by a cryptomicroprocessor with a matching decryption key. It cannot be executed by microprocessors lacking the key nor can it be disassembled for use in competing software products.

"One of the encryption methods possible, a polyalphabetic substitution cipher, is not intended for absolute secrecy, just to make decryption of the encoded program not worth the bother," Best says. The decryption uses "several small tables of randomly generated bits stored on the processor chip. Each deciphering cycle overlaps a bus addressing cycle, so additional clock cycles are not required. This may permit cryptomicroprocessors to be competitive in performance with conventional microprocessors."

DES encryption. For more protection, cryptomicroprocessors may execute programs enciphered in 8-byte blocks using the data encryption standard [*Electronics*, June 21, p. 107]. Although the DES requires a minimum of 16 clock cycles (using random logic) and is therefore rather slow compared with polyalphabetic methods, it has the advantage of established credibility.

In the figure, DES is used in the deciphering circuit and is controlled by a decryption key from the program- and data-key blocks. This key is different for each block because the bus is exclusive-ORed to



Mum. Instructions cannot be read out of the cryptomicroprocessor. Each enciphered instruction is deciphered as it is fetched into the instruction queue for execution.

the program and data keys.

"Cryptomicroprocessors should not be confused with data encryption chips [*Electronics*, June 21, p. 117], which are used for secure data communications," Best says. "Unlike enciphered messages, which are ultimately deciphered for disclosure, an enciphered program is deciphered by a cryptomicroprocessor solely for execution within that processor and is not disclosed to anyone." He will deliver a paper on the concept at Compcon '80. **-Harvey J. Hindin**

Test equipment

Fast units use emitter-coupled logic parts to handle LSI circuit testing

With large-scale integrated circuits proliferating, two members of the test community are ready to talk about general-purpose test systems that are fast enough to characterize these and next-generation ICs. Fairchild Camera and Instrument Corp. is unveiling a machine able to test with clock rates of 20 megahertz and higher, and Japan's Nippon Telegraph and Telephone Public Corp. has an even faster system for its own use.

At the Oct. 23–25 Semiconductor Test Conference in Cherry Hill, N. J., Fairchild's Test Systems group will put its new Sentry series 20 through its paces. The 20 can do limited testing at speeds of up to 40 MHz—"a conservative figure," according to Mike Gillette, marketing manager for LSI products at the San Jose, Calif., group. Selling for around $600,000 with two 60-pin test heads, it will start moving onto production lines in the beginning of next year.

Faster. Also at the conference, NTT researchers will describe a system made for them by Takeda Riken Industry Ltd. Like the System 20, it relies on high-speed emitter-coupled-logic parts for its performance.

The Japanese tester (see "Fast NTT tester has many pins," p. 46) tops Fairchild's in speed (100 MHz) and cost (about $2 million)—but it is not for sale. However, industry observers note that Tokyo-based Takeda Riken has discussed similar systems in the past and will likely come up with a product.

There is no doubt that such machines will be welcome, in spite of the high cost involved. "Some microprocessors (Digital Equipment Corp.'s LSI-II and Ferranti Ltd.'s F100L, among others) are clocking input/output in excess of 10 MHz, and some of the new RAMs (the 2147 and 2148, for example) are reaching speeds of 40 MHz and above," says Fairchild's Gillette. "Most general-purpose LSI test systems don't have the ability to produce test rates in excess of 10 MHz." Exceptions are dedicated memory systems, which typically test at about 25 MHz.

To gain the series 20's speed—20 MHz with a full 60 pins and 40 MHz or more with 30 pins—the Test Systems group uses 100,000-gate ECL parts supplied by the Semiconductor Products group. Such parts, which include registers, latches, and line receivers, slash gating times by an order of magnitude compared to the TTL parts that earlier Sentry VII

Fast NTT tester has many pins

The Musashino Electrical Communications Laboratory of the Nippon Telegraph and Telephone Public Corp. decided on separate input/output channels, rather than combined ones, for its 100-megahertz tester. This setup contributes to the unit's extremely high speed because it eliminates time-division I/O multiplexing.

The NTT system can be expanded to as many as 384 channels in groups of 64 (32 input and 32 output). Researchers point out that the division of channels by function does not severely limit the system's usefulness since a pin count of more than, say, 120 is not likely for some time to come.

Two types of extremely high-speed ICs developed by the lab provide high performance where it is needed most. In the sequential pattern processor, which has a depth of 32-K words of 192 bits each, 1-K emitter-coupled-logic random-access memories with an access time of 7.5 nanoseconds are used as a two-way, interleaved cache memory. Six other key circuits have as their basis a 200-gate master slice developed as an arithmetic and logic unit and shifter in electronic telephone exchanges. In addition, hybrid circuits designed around microwave transistors are used in the test stations. Further boosting throughput is the extensive use of pipelining.

The overall control of the system is in the hands of a 32-bit control processor, overseen by a supervisory processor. The control processor communicates with all other parts of the system by a 1-MHz bus; communication within these parts, which are functionally independent modules, is by 100-MHz buses. Different modules with different levels of performance have been developed so a user can tailor the system to his own needs, adding multiple test stations, for example. **-Charles Cohen**

and VIII systems used.

The series 20 also has a larger memory than those systems, thereby boosting throughput because the complex test programs can be run in larger blocks. Its testing manager, an FST-2 general-purpose computer, has a directly addressable semiconductor memory of 96-K 24-bit words, expandable to 196 K. For program store, it has a 4-K cache memory, expandable to 16 kilowords once 16-K random-access memories are available in sufficient quantities.

Unlike earlier Sentry systems (and most competitive systems), the series 20 has 16 timing generators rather than 8. Furthermore, these 16 different timing groups can be switched on the fly, that is, after each clock cycle. "This increases testing flexibility, needed for some of the new microprocessor chips with their very exotic timing schemes," Gillette explains.

This flexibility, combined with the basic 20-MHz testing rate, should help Fairchild Test Systems extend its lead, at least temporarily, in the LSI testing field. A spokesman for Tektronix Inc.'s Measurement Systems division in Beaverton, Ore., notes that its S-3270 automated test system "by comparison has limited flexibility at full 20-MHz testing," but "we are not standing pat," he adds. **-Bruce LeBoss**

Microprocessors

Chip emulates 8085, has Z80 instructions

It's hardly uncommon for semiconductor manufacturers to emulate popular parts, but National Semiconductor Corp. is going to emulate two of them in one microprocessor. In November, the Santa Clara, Calif., company will begin offering samples of a processor, using its new high-density complementary-MOS process, which is built around the architecture of Intel Corp.'s 8085 and executes the instruction set of Zilog Inc.'s Z80.

The NSC800 "combines the best of both worlds," claims Anne Wagner-Korne, marketing manager for low-power microprocessors. "The 8085 increases the level of functionality with its multiplexed address data bus, so we gain additional pins." Thus, National can add a clock generator, multiple interrupts, and other functions on chip. In contrast, "the Z80 has a standard bus structure, but we pick up the best mid-range instruction set (really a superset of the 8080)."

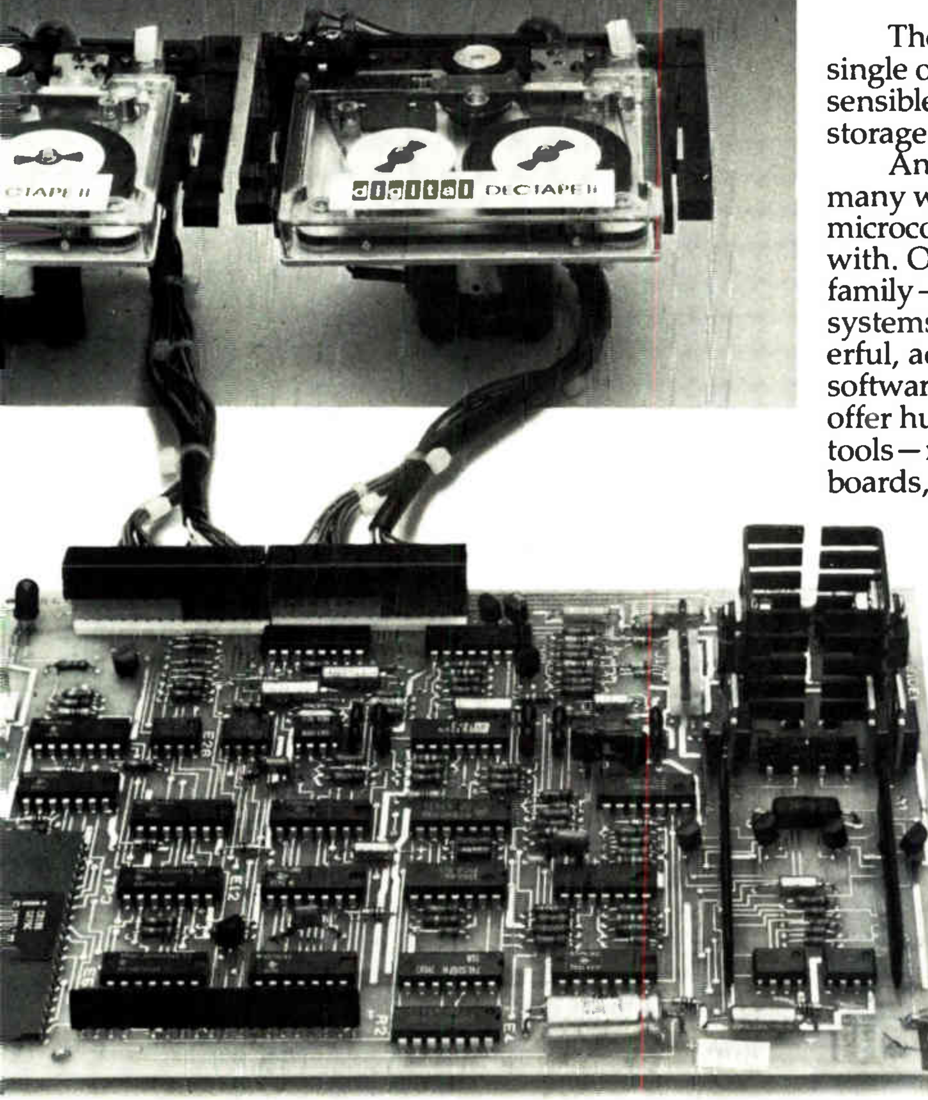
Shot. Consequently, National believes that the combination, coupled with its advanced P²-MOS techniques gives it a direct shot at "applications where you have to have a C-MOS microprocessor but need the performance of the 8085 or Z80," Wagner-Korne says. One of the company's targets is RCA Corp.'s 1802, the most widely used C-MOS microprocessor.

Looming on the horizon is Mitel Corp.'s C-MOS version of Motorola's 6802 microprocessor. Also coming is RCA's planned 8085 in silicon on sapphire, which Wagner-Korne considers closest in performance to the NSC800.

Stacked up against available 8-bit processors, the 800 offers the same power dissipation as the 1802—0.1 watt at 5 volts—whereas the Z80, 8085, and 6800 are in the 2.5-to-2.8-W range. Maximum cycle time is 400 nanoseconds; minimum is 250 ns, the same specifications as for the Z80. The 8085 and 1800 have slightly better cycle times, whereas the 6800 takes about twice as long.

Making possible this nearly n-MOS performance is the P²-MOS process, which borrows some advances of n-channel like scaling and planar approaches, according to George Simmons, C-MOS process development. The double polysilicon brings some density improvement although parts in the 4-micrometer geometry range are about 20% less dense than n-MOS parts, he says. However, Simmons allows that it is a more complex process than National's X-MOS variant of scaled n-MOS.

National is aiming the 800 at "the 25% of the mid-range designs that could benefit from the lower power," Wagner-Korne says. Also, "there's an outrageous variety of hand-held devices in such markets as acoustic



analysis and geological surveying." At the low end, the chip would fit well into process-control applications where the environment is noisy and hot and limited space precludes a fan, she adds.

The company is marshalling its P^2C-MOS attack complete with support circuits that parallel the 8085's support. Quickly following the 800 central processing unit will be the 830 read-only memory and input/output controller and the 810 that will combine I/O control, timer, and random-access memory. Wagner-Korne hints that in six months there could be an 820 communications chip, along with direct-memory-address, arithmetic, and other chips. Integrating the 800, 810, and 830 on one chip also is a possibility, she continues.

To aid acceptance of its P^2-MOS 800 family, National already is offering samples of the NMC6504 4-K-by-1-bit static RAM and the NMC6514 1-K-by-4-bit partner and is bringing out versions of eight standard C-MOS gates, inverters, and other interface chips that are three times faster.

The company has seen first silicon on the NSC800 and expects to be in production during the second quarter of 1980, according to Wagner Korne. **-William F. Arnold**

Memories

Laser-based optical storage system uses fixed media, revolving record/read setup

A new laser-based optical data-storage system appears ready to give video disks a run for their money. Developed at Battelle Memorial Institute's Northwest Research Laboratories, the scheme promises lower cost, higher density storage, and faster bit transfer rates than disks are delivering.

Using a variety of fixed storage media, both permanent and erasable, the system can store up to 625 megabits per square inch in the form of dots 1 micrometer in diameter and 1 μm apart. It records and reads out this data by a spinning wheel.

Depending on the storage medium, the price of storage runs from less than a tenth of a cent per megabyte to something under a penny. In contrast, one well-placed source figures disk-stored data would cost about 10 cents a megabyte [*Electronics*, Sept. 27, p. 97]. Densities for the laser-based disks are 160 to 180 megabits/in.^{2}

All the applications touted for video disks—from home digital video and audio to bulk data storage—can be served by the new technique, according to its developer, James T. Russell, staff scientist at the Richland, Wash., labs. The system can be built to write data as well as simply read it, a step that developers of disk systems also plan to take.

Despite the performance claims, Russell has worked to keep the hardware and software costs low. He figures the worst-case cost to produce a home video-playback system is $260. A more reasonable figure is about $120—and even that is on the high side, he claims.

Fixed. In contrast to disk systems, the storage medium does not move, a feature that cuts costs and simplifies operation, Russell explains. In a typical application, a circular record the diameter of a doughnut would be placed on a window in the top of a playback system's sealed enclosure and its contents scanned by a laser and photodetector system. Being immobile, the storage media may be more fragile than those used for video disks, which have to endure severe mechanical stresses as they rotate at high speed.

But something still moves in the new system—the spinning scanner wheel, which is directly responsible for its high bit transfer rate. Mounted on the wheel is an array of six lenses through which the laser beam scans the data. As a result, the

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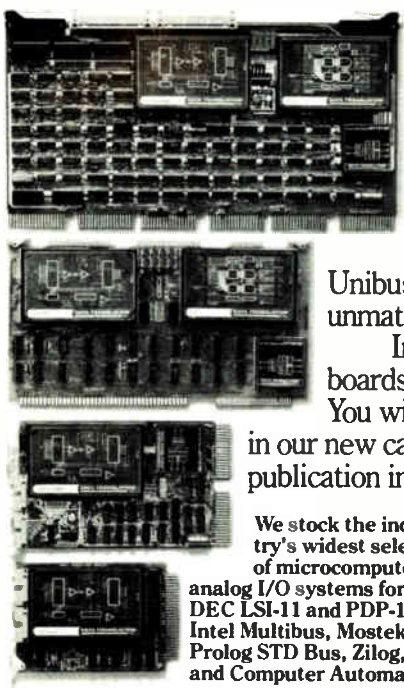

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data is scanned six times per revolution, compared with a video-disk system's once. What's more, the wheel can spin faster than any storage disk, since it can be made of far tougher material.

Five types of recording media are under study by Russell and system licensees. They range from photographic-like film for permanent storage to magnetic films and thermoplastics, erasable by demagnetization and heat, to photochromic materials that can self-erase.

Copies of some of these media could be reproduced using a variation on contact printing at about 0.01 cent a megabyte, according to Russell. That cost would be 10 to 1,000 times cheaper than disks.

Russell says that when potential licensees first hear about the system's resolution and packing density, they tend to dou
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Battelle is interested in resea
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According to DRC's president, Sarason D. Liebler, first applications will probably be in digital data storage. The first licencees are Fuji Photo Film Ltd., Tokyo and the Datatape division of the Bell & Howell Co., in Pasadena, Calif. **-James B. Brinton.**

News briefs

Wescon attendance zooms

Wescon celebrated its 30th anniversary late last month by breaking its attendance record. An unaudited total reports better 50,660 persons visited the 809 booths of some 450 exhibitors in the three-day show in San Francisco. The previous record was 47,770 at a four-day session in 1966 in Los Angeles, the alternate site, where attendance is traditionally higher. "If we're in any phase of a recession, you couldn't tell it," says a spokesman.

Semiconductor growth seen slowing

Next year's growth rate for U. S.-based semiconductor manufacturers should drop to 11.1% from this year's 30.6%, predicts the Semiconductor Industry Association, pointing to the U. S. recession as the cause. However, the SIA adds, predicted 1981 and 1982 growth rates of 19.2% and 17.7%, respectively, will push the industry near $10 billion in worldwide sales—in fact U. S.-based chip makers appear to be retaining their two-thirds share of world semiconductor production, largely because of their advantage in microprocessors and related products. As might be expected, the growth rate of discrete products is predicted to trail that for integrated circuits: a 2% rise to 1980 sales of $1.9 billion versus 15% to $5.1 billion.

Third-graders to write programs

Beginning this month, third-graders will do homework on personal computers at a private school in Dallas as part of a study of how children learn and how computers can help. For the experiment, Texas Instruments Inc. of Dallas is collaborating with the Massachusetts Institute of Technology's Logo project—a long-term program to develop computer-based aids to education. TI is adapting its new 99/4 home computer [*Electronics*, June 21, p. 23] to provide children at the Lamplighter School with portable learning stations on which they can program graphics for exercises in mathematics, geometry, and spatial relationships, as well as type and edit compositions. After modifications, the 99/4 will accommodate the simple Logo language, an associated text editor, and display graphics. It will also be able to store the students' programming activities. Furthermore, TI will add 16 kilowords to the computer's main memory—a capability that TI may market.

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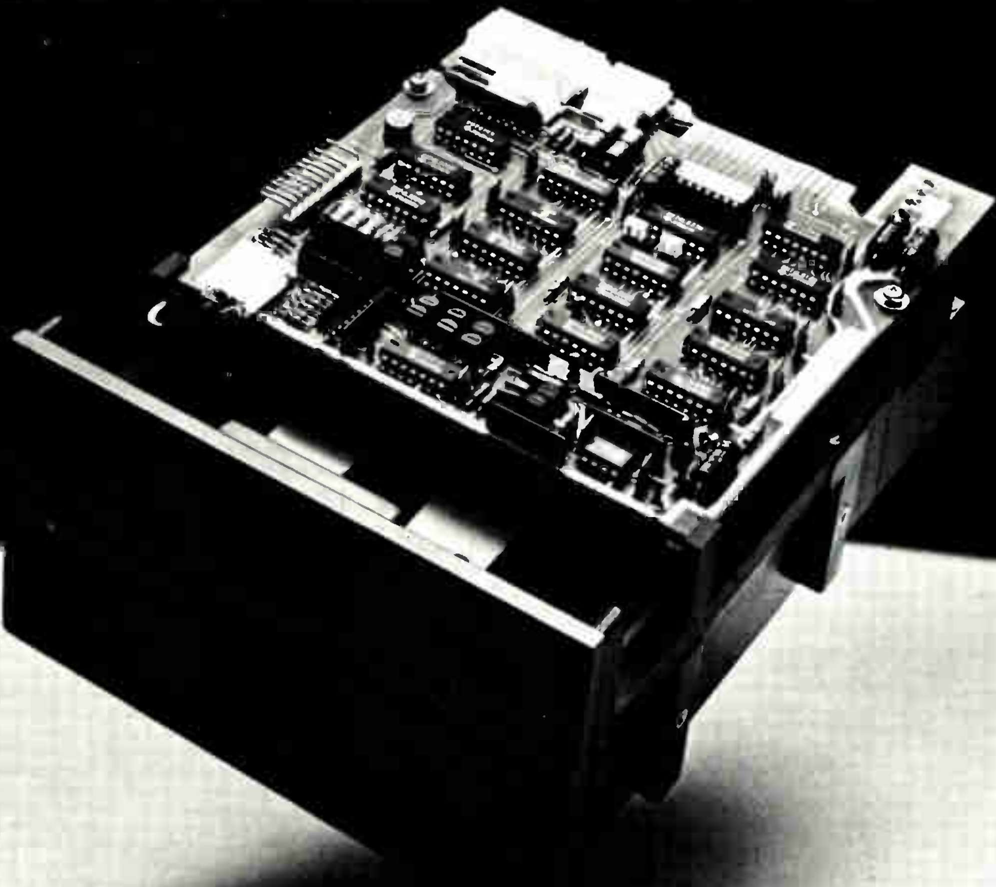
The FD-50A is designed to reduce the chances of data loss to a minimum. Write-protection circuitry allows you to protect valuable disks from accidental erasure. A door lock prevents inadvertent opening of the door while the disk is in use. And a precision stepper motor ensures accurate, reliable head positioning. FD-50A. The fast Mini Disk Drive from TEAC.



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Circle 62 on reader service card

Washington newsletter

State licensing of engineers opposed by EIA

The Electronic Industries Association is moving to oppose state licensing of engineers proposed under a model law written by the National Council of Engineering Examiners and being submitted to state legislatures. The NCEE, which is composed of members of state engineering licensing boards, wants licenses required for **all those in "responsible charge" of engineering activities, all those who are called engineers, and all those who teach engineering in any setting.**

EIA president Peter McCloskey says the association has formed an Ad Hoc Committee on State Licensing of Engineers to oppose the "discernible threat to the public." Industry engineers, he points out, provide their services not to the public but to employers who are responsible for their products and services. Employers "are further disciplined by competition and by numerous safety regulations imposed by all levels of government," McCloskey notes.

ITT-Northrop team gets FAA job for VOR, Vortac

The team of ITT Avionics and Northrop Wilcox proved to be the sole bidder on a $115 million Federal Aviation Administration program to replace its 927 vacuum-tube radio navigation aids with solid-state equipment in a five-year program. The new systems will replace the VOR and Vortac units, whose radio signals guide pilots from one ground station to the next. VOR—very high-frequency omnidirectional radio range—is used by civilian pilots, whereas Vortac packages share a frequency allocation with the Tacan military tactical air navigtion systems. **The FAA estimates it will save $27 million a year in operating the solid-state replacement systems** because of their longer lifetimes and lower power requirements. International Telephone and Telegraph Corp.'s Avionics division in Nutley, N. J., and Northrop Corp.'s Wilcox Electric Inc. in Kansas City, Mo., have received an initial $78.5 million to build and install the first 586 systems, with an option for 364 later.

U. S. investment abroad to rise again by 12% in 1980

Majority-owned foreign affiliates of U. S. electronics companies and other manufacturers in the Commerce Department's "electrical machinery" category plan to boost 1980 capital investment by 12% to $1.5 billion. The increase marks the **continued, steady rise in capital investment abroad, which will reach $1.3 billion this year,** or 23% above the 1978 level, according to the department's Bureau of Economic Analysis. Bureau officials note that the 1979 investment growth figures reflect a number of considerations, including the greater availability of capital abroad, as well as expansion of foreign business activity and the depreciation of the U. S. dollar in foreign exchange markets last year.

Addenda

The Treasury Department will **continue its investigation of Japanese dumping of countertop microwave ovens in the U. S. market** on the recommendation of the U. S. International Trade Commission. The ITC says imports from Japan rose to 800,000 units in 1978, a 34% market share, from the 1976 level of 500,000, a 30% market share, although Japan's market share has declined in the first half of this year. . . . **Exports of measurement and control instruments, like computers, continue to rise,** generating a $607 million positive trade balance in the first half to a total of $698 million, while imports increased only 14% to $91 million, the Commerce Department says.

Resolving the FCC's data-communications dilemma

Apart from its own inertia, the Federal Communications Commission's biggest obstacle on the road to deregulation of new data-communications equipment and services is the American Telephone & Telegraph Co.'s 1956 consent decree precluding its entry into any market other than regulated communications. The FCC clearly wants to get around the 23-year-old antitrust ruling and let AT&T compete along with everybody else in this rich new market, and it said so early in July in its Second Computer Inquiry's "tentative decision." But the FCC doesn't know quite how to go about deregulation without violating the consent decree and setting the world's largest corporation loose to grind down its competitors.

There was not a glimmer of guidance from the White House last month when Jimmy Carter made known his policy views on telecommunications to a Congress that is still struggling to amend the 1934 Communications Act. Carter's "new policy" merely rewrote and reheated old generalities in favor of greater deregulation and increased competition that the FCC has been hearing for nearly a decade.

Industry's proposals

The most specific recommendations to the FCC on how to cope with the problems of AT&T's entry into the data-communications market came early this month from the Computer and Business Equipment Manufacturers Association and the Computer and Communications Industry Association. Both come out strongly for complete deregulation of all data-communications services and customer equipment and agree that entry of AT&T or any other significant common carrier must be done through totally separated subsidiaries.

The FCC should note well the similarity of the two associations' basic recommendations, since their constituencies are significantly different. The CBEMA numbers 14 computer industry heavyweights among its 38 members, including Control Data, Digital Equipment, Honeywell, IBM, and Univac, while the CCIA speaks for smaller manufacturers of mainframes, plug-compatible peripherals, and terminals. The commission should also take note of the CBEMA's and the CCIA's differences.

Where the CBEMA calls for common carrier subsidiaries selling unregulated data-communications services and equipment to be completely separate, with "separate officers, personnel, facilities and books," as well as separate financing, research and development, manufacturing, marketing, procurement, and installation and maintenance activities, the CCIA goes a step further. It calls for all of these things and, in addition, a limitation of carrier ownership to two thirds of a subsidiary's stock.

Rewriting the law

More important is the division between the CBEMA and the CCIA on the issue of the consent decree. The FCC says technical advances since 1956 have inextricably merged some aspects of communications and data processing. Thus it wants to proceed to propound new policies "in the public interest," unconstrained by the consent decree. Otherwise, it suggests that each new service would be subject to the years-long regulatory process of investigation, hearings, and rehearings that lead to the establishment of "equitable" tariffs.

Both the CBEMA and the CCIA want to avoid this, of course. But where the CBEMA urges the commission to proceed with its policies, unconstrained by the consent decree—suggesting that the issue will probably wind up in the courts anyway—the CCIA urges the agency to first adopt rigorous competitive safeguards against AT&T's market dominance and "then seek modification of the decree before a court having proper jurisdiction." The CCIA contends that "it is quite probable that such rigorously defined separation would be acceptable not only to the Department of Justice [which must be persuaded to seek the modification], but also to potential third party intervenors," who might bring their own suits to keep the FCC from allowing AT&T into the competitive fray.

The CCIA may be the smaller and less influential of the two industry groups in this case, but it has taken its recommendations one step further to spell out to the FCC what it can do to achieve its goals in the shortest possible time. The CBEMA's position is somewhat less developed, but it is not far behind; in view of the differences of opinion among some of its larger members—Honeywell and IBM, for example—CBEMA's position is probably about as well developed as it could have been.

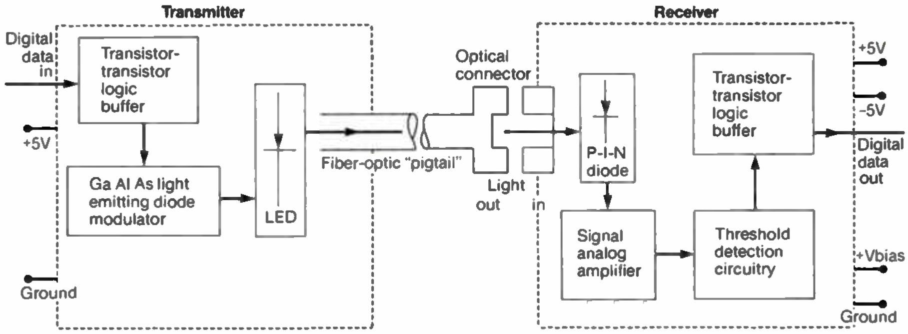
The FCC has now received the advice of the two organizations whose members would be most threatened by an AT&T entry into the data-communications marketplace. If the commission heeds that advice, its dilemma about how to resolve the issue of full competition in data communications could be resolved in less than a year. For the FCC, that is but the twinkling of an eye.

Ray Connolly

RCA

A report on electro optics: For optical communications.

RCA offers a systems approach for fiber-optics data transmission.



More and more companies are turning to fiber-optics for data transmission.

For many, it's a completely new technology and start-up problems can be immense.

RCA has a solution: Consider one of our prepackaged digital data link systems.

Complete compact modules.

RCA data links (below) are complete transmitting/receiving units, each measuring only 3.5 cubic inches. Everything you need is pre-assembled.

Applications include: secure data transmission, high voltage optically isolated systems, computer interface, or process control systems.

High-speed transmission.

A high-speed gallium aluminum arsenide IR emitter together with a TTL gate and a gallium aluminum arsenide LED modulator forms the heart of the transmission module.

The emitter chip is an edge emitting design with a small source size, for optimal coupling with fiber-optic materials.

On the receiving end, a fast response RCA P-I-N photodiode drives a signal analog amplifier to reproduce TTL compatible output signals.

Customized systems.

RCA offers a choice of four variations on the data link system (see chart below).

All four types can be modified to meet almost any specialized requirement, which enables the designer to pick the right sensitivity and bandwidth for his application.

Or we can go one step further and custom engineer your system from the ground up.

RCA's expertise in electro optics and our wide range of proven components (IR emitters, injection lasers, P-I-N and avalanche detectors) is your assurance we can get the job done.

Typical performance characteristics.

RCA system type	Transmitter power output,* microwatts	Receiver NRZ, megabits/sec.	Receiver sensitivity, microwatts**	Allowable loss, decibels**
C86003E	100	20	0.50	-23
C86004E	100	5	0.25	-25
C86005E	100	2	0.10	-27
C86012E	40	20	0.50	-20

*Minimum. **Bit error rate 10^{-9}.

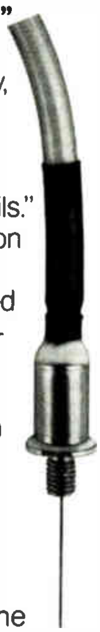
A full range of emitters and lasers designed for efficient coupling.

If you decide to design your own fiber-optics transmission system, picking the right package can be just as critical as emitter performance.

That's why it pays to design your module around RCA components.

RCA offers a full line of IR emitters and CW lasers optimized for optical communications. In a variety of packages designed for low light-loss coupling to fiber-optic cables.

With output "pigtails."



If you want to be sure of maximum coupling efficiency, let us do it.

RCA offers both IR emitters and injection lasers with integral fiber-optic "pigtails."

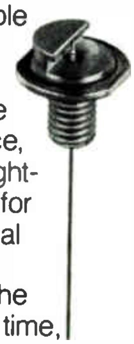
Our C86002E CW injection laser, with optical feedback, features an internally mounted P-I-N photodiode. The photodiode is positioned so that current is proportioned to the laser output. This feature with the use of an external feedback circuit controls laser output stability over a wide temperature range.

RCA gallium aluminum arsenide CW lasers include the C86010E which produces 1.0 mW (minimum) CW output power with Siecor 112 cable, and the C86007E rated at 2.0 mW output (minimum) using DuPont PIFAX cable. Both exhibit a typical radiant flux of 820 nm.

The C86008E and C86009E gallium aluminum arsenide IR emitters also have integral fiber-optic cables. They exhibit a typical rise time of 3 ns and a typical frequency response of 150 MHz.

With removable caps.

The RCA C86017E and C86018E high-speed gallium aluminum arsenide IR emitters are edge emitting devices with small source sizes and removable protective caps.



With the caps off, the fiber can be coupled close to the surface of the source, thus virtually eliminating light-loss. Output performance for the C86017E is 3 ns typical rise time, 50 MHz typical frequency response. For the C86018E 8 ns typical rise time, 100 MHz typical frequency response.

Also available with removable cap (on special request) is the C86000E low threshold gallium aluminum arsenide injection laser. The "stripe contact" emitting surface of this device limits output radiant flux to a narrow area for efficient collection into the fiber-optic cable.

And its geometric coaxial stud package is designed for simple mounting and good thermal dissipation.

Output wavelength of 820 nm is matched to the maximum response of P-I-N and avalanche photodetectors.

Silicon photodiodes with integral light pipes for easy coupling.

On the receiving end too, performance can make or break a system. That's why RCA offers fiber-optic detectors (C30920E, C30921E) packaged with an integral light pipe to complete the optical path from the fiber to the surface of the photodiode. The core of the light pipe is sufficiently large (0.010 inch diameter) and is accurately centered to facilitate alignment of single fibers to the package.

As a result, performance can be specified for the accessible end of the integral light pipe.

Extremely fast response.

RCA fiber-optic photodiodes are also designed for rapid response. Our C30921E avalanche photodetector has a response time of 0.5 ns, spectral response range of 400 to 1000 nm. and is optimized for 830 nm.

Our C30920E P-I-N photodetector has a similar spectral response range and a response time of 3 ns.

With built-in preamp.

For best possible performance, choose one of our photodiodes with a built-in preamplifier (below). These units (C30910E, C30917E) integrate RCA's widely acclaimed high performance avalanche detectors with low noise preamplifiers. This results in optimum sensitivity and bandwidth in a package that permits efficient coupling to optical fibers and bundles. Typical sensitivities as low as 4×10^{-14} watts/(Hertz)$^{1/2}$ can be achieved with system bandwidths of 50 MHz.

These detectors are available as complete systems including temperature compensating circuitry.

Or if you'd rather do your own circuit design, get them without preamplifiers (C30904E, C30905E, C30908E)

RCA technical support.

RCA has a lot more to offer than parts and specs.

Whether you need product information or design help, you can always give us a call.

For further information on RCA data link modules and emitters, contact RCA Electro Optics, Lancaster, PA 17604. Phone: (717) 397-7661.

For photodetectors, contact RCA Ltd., Ste. Anne-de-Bellevue, Quebec, Canada. Telephone (514) 457-9000.

Or contact RCA, Buenos Aires, Argentina. Brussels, Belgium. Sao Paulo, Brazil. Sunbury-on-Thames, Middlesex, England. Stuttgart, West Germany. Mexico 16 D.F., Mexico.

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We've just added two hard-hitting rookies to our winning lineup.

Now that the new F6802 microprocessor and F6846 combo chip have joined Fairchild's F6800 team, you've got a minimum, microprocessor-based-system solution to your design problems. One that's low cost and easy to work with too. Like the rest of our F6800 family, these two great new NMOS products are made using Fairchild's patented Isoplanar™ process.

The F6802 and F6846 are already becoming big hits in the microcomputer field. When you put them on your team, they're bound to score some winning runs for you.

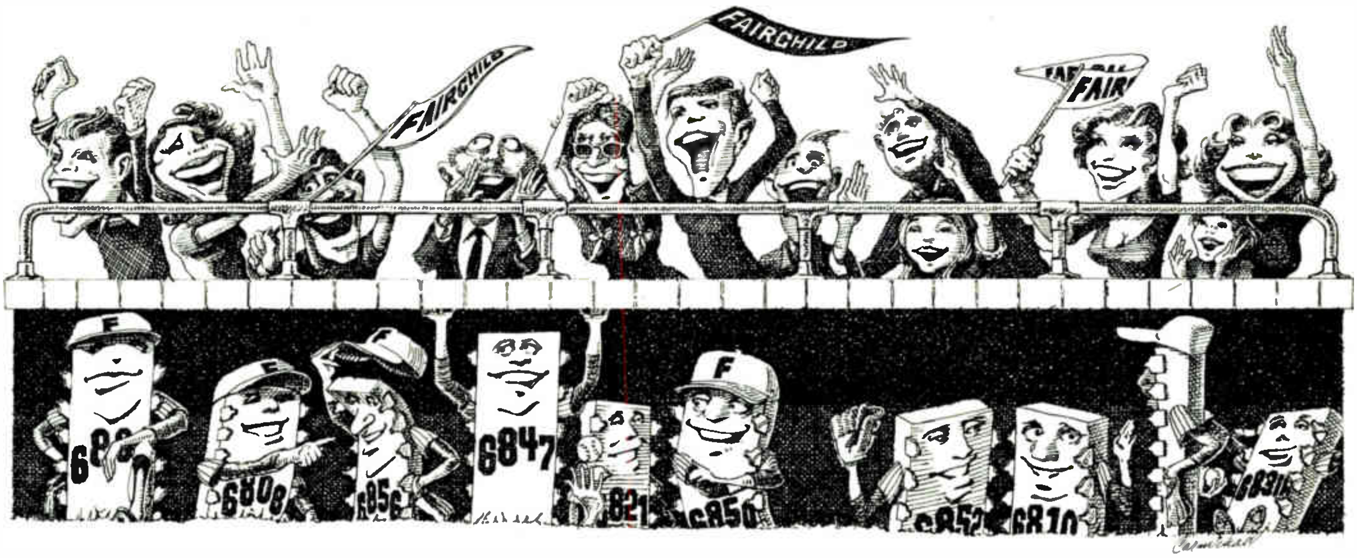
The F6802 microprocessor. It sends your design problems to the minors.

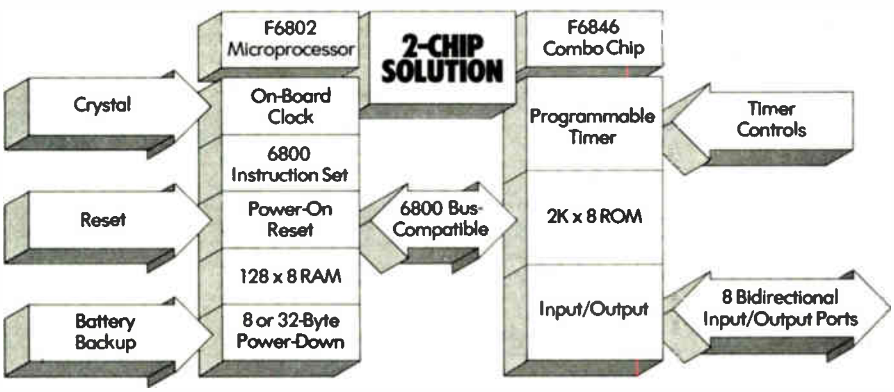
And that's where they'll stay, thanks to this enhanced version of the F6800 central processing unit. The F6802 offers an on-chip power-on reset function, on-board clock for easier use and on-board 128 x 8 RAM with options of 8-byte or 32-byte power-down. Now you no longer need an additional RAM with battery backup systems.

The F6802 features a memory-ready line for slow or fast memory. So you can use memories in synchronous or asynchronous mode. And the F6802 is bus-compatible for easy use with all of the other F6800 peripherals.

The F6846 combo chip. It's a memorable teammate.

The F6846 is a user-defined ROM-based peripheral element. It features 2K x 8 ROM, a powerful programmable binary timer, and eight bidirectional input/output ports on the same circuit. It's also F6800 series bus-compatible.





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We support your team.

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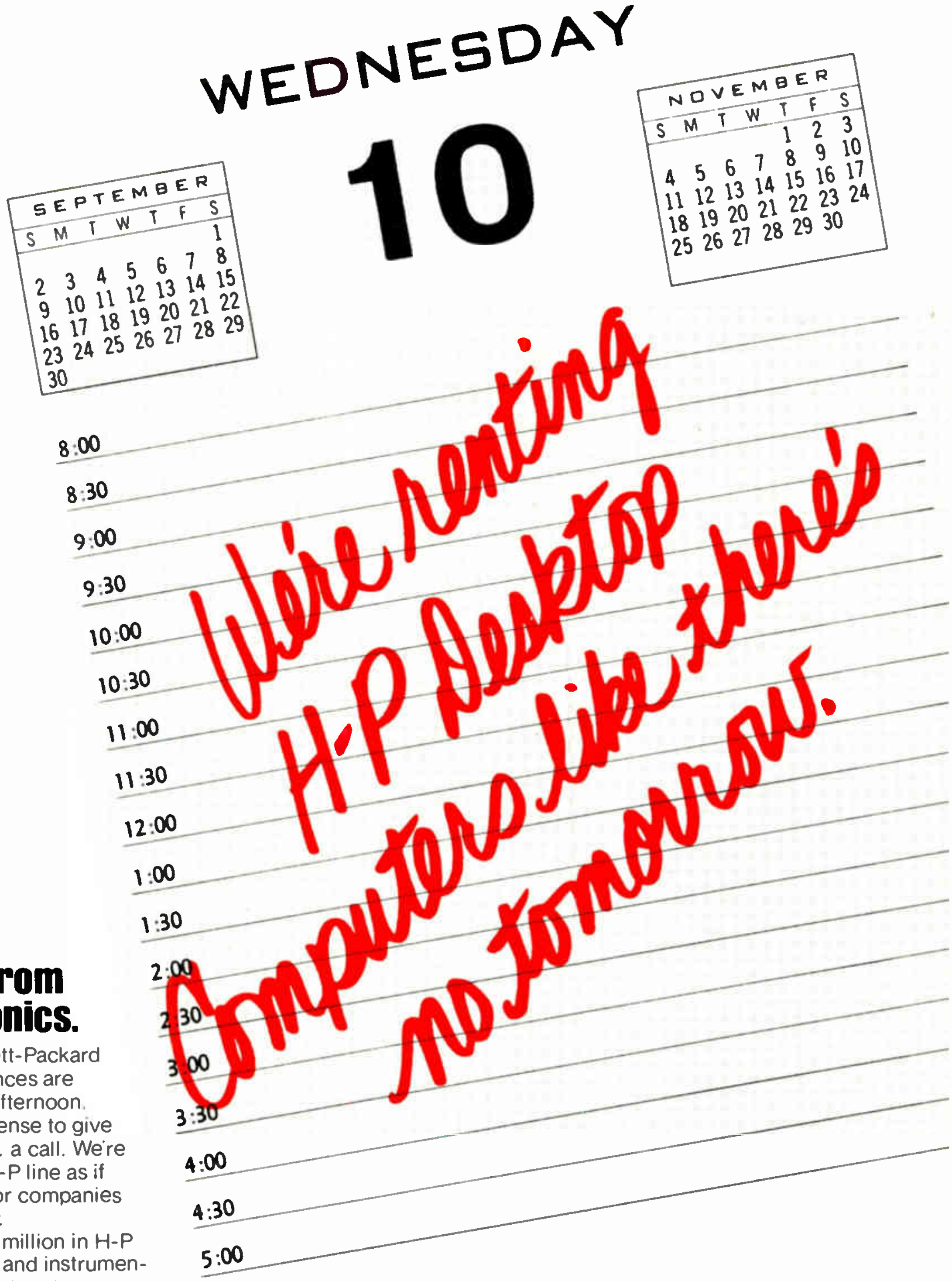

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Circle 71 on reader service card

Siemens targets 64-K RAM market

The Components division of Munich-based Siemens AG is wrapping up the development of two separate 64-K dynamic random-access memories. One, using 3-μm geometries, is **a standard n-MOS double-polysilicon device** with a single ±5-V supply and an access time of less than 150 ns. It should become available for the open market around the end of next year. The other, using 4-μm geometries, is **an aluminum-gate V-groove MOS device** with a +8- and a −2-V supply and an access time of between 200 and 300 ns. Production of the V-MOS RAM, which is slated for in-house consumption at least initially, is scheduled to start early next year. In going with V-MOS, Siemens is pushing ahead with a technology that others are rejecting for memory fabrication (see p. 42).

French make small LCD still smaller

The Laboratoire d'Electronique et de Technologie de l'Informatique (LETI) in Grenoble, France, has developed **a 2-cm² liquid-crystal display with a 256-by-256-element matrix.** The display, capable of 32 shades of gray, produces between 10 and 15 images per second. An improvement of an earlier LCD [*Electronics,* Dec. 22, 1977, p. 55 or 3E], it has a center-to-center distance between elements of 5 μm. It was developed at the behest of the Centre National d'Etudes des Télécommunications, the research arm of the State Secretariat for Posts and Telecommunications, and may be used in the interactive terminals that are to be distributed to all French telephone subscribers [*Electronics,* July 15, 1979, p. 85].

West Germans claim lowest attenuation for graded-index fiber

Researchers at the ITT subsidiary Standard Elektrik Lorenz AG (SEL) in Stuttgart, West Germany, have obtained what they claim is the lowest attenuation so far reported for a graded-index optical fiber. **At a wavelength of 1.20 μm, the attenuation checks in at 0.54 dB/km; it drops to 0.31 dB/km at 1.55 μm.** The low figures have been achieved, SEL says, by decreasing the impurity level in the glass fiber to less than 0.2 ppm and by a careful balance of the doping materials. With core and outer diameters of 50 and 125 μm, respectively, the fiber corresponds to proposed international standards. Its low attenuation, SEL predicts, should make possible wideband transmissions over more than 100 km (about 62 miles) without repeaters. In Japan, Nippon Telegraph and Telegraph Public Corp. earlier announced achieving an attenuation of 0.20 dB/km for a step-index fiber [*Electronics*, March 29, p. 48].

IBM Japan joins competitors with kanji display system

IBM Japan Ltd. has taken a big step in catching up with its domestic competitors in an area that will become increasingly important in the Japanese market by announcing the IBM 3270 kanji information display system. The unit can display a total of 7,190 characters, including 6,709 kanji characters, the Chinese characters that are used together with the native kana syllabary to write Japanese. The system is supported by all of IBM's mainframes and by the 8100 information system. Input is by a keyboard containing 216 keys for one hand and 12 for the other. The board gives direct access to 2,567 characters; other characters are entered by their 2-byte code. Also available is the IBM 3284-52 ink-jet printer, which prints 37 kanji or 74 kana or Roman characters per second. Both work with a special controller, the IBM 3274-52C. IBM has also developed a version of its laser printer, the IBM 3800-2 kanji printer subsystem, for high-speed printing.

ITT Semiconductors readies one-chip speech synthesizer . . .

Watch for the ITT Semiconductors Group to come out with a speech-generator circuit that synthesizes human speech digitally and is intended for use in consumer applications. By using several data-reduction methods, ITT engineers have managed to accommodate all necessary speech elements for a vocabulary of more than 20 different words, together with the required control circuitry, on a 30-mm² (46,500-mil²) very large-scale integrated metal-oxide-semiconductor chip. **The stored words are combined into sentences by means of control signals** decoded by the circuit. The group's headquarters company, Intermetall GmbH in Freiburg, West Germany, sees the chip applied in talking clocks, in telephone-answering devices, and in equipment that alerts an operator to a system's particular status or condition.

. . . and sets up UK plant for H-MOS memories

The ITT Semiconductors Group plans to put on stream an H-MOS (for high-performance MOS) production plant at its Footscray, UK, facilities. The investment, says the headquarters company, Intermetall GmbH in Freiburg, West Germany, "underlines the decision to concentrate our worldwide memory development and production activities in the UK." **Running the H-MOS plant as microlithographic engineering manager will be Karl Harris, formerly with National Semiconductor Corp.** in the U. S. and reportedly an expert in the latest electron-beam mask production and step-and-repeat processes.

Poland keeps color TV production on schedule

Fulfilling plans drawn up several years ago [*Electronics*, Aug. 4, 1977, p. 67], Poland's fledgling color TV industry seems to be pretty much on target with color tube and set production. By the end of this year, the Unitra Polkolar TV facilities will produce some 25,000 color display tubes, made under licenses from RCA Corp. and Corning Glass Works. Output of the precision in-line tubes will be stepped up to 200,000 next year, to 600,000 by 1982, and to 1 million by 1985. Color set production will probably get under way before the end of this year. **These efforts will gradually make Poland independent of color TV imports,** which are now mainly from the Soviet Union.

Hungary's computer ICs behind by a decade, French report says

Hungary trails the world's most developed countries by 8 to 10 years in computer development, according to a report prepared by three computer specialists within the Hungarian government. The report notes that although Hungarian industry is producing third-generation integrated circuits, **the level of integration is no higher than what was being achieved in the developed countries in 1970.** The authors explain that Hungarian authorities are attaching greater importance to the expansion of data-processing applications than to technological advances. They note that Western countries refuse to sell computers to Eastern Europe larger than, for example, an IBM System/370—a policy that maintains the 8-to-10-year gap. The report, financed by the French Ministry of Industry as part of a project entitled "Six Countries in the Face of Computerization," places the number of computers in Hungary as of 1977 at 850, with only 19 of those large mainframes.

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For example, SSi was the first company to fully integrate a DTMF receiver on a monolithic chip, combining both analog and digital functions as well as fully integrating switched capacitor filters on the same CMOS chip. This technology is available to you for your custom application.

For a few more examples, see the circuits below: (a) a custom CMOS IC that replaced 60 standard IC circuits and 2 CMOS RAM's; (b) an I²L bipolar digital IC with 3300 random logic gates; (c) a bipolar linear capacitance threshold detector; (d) an MOS digital loop detector for vehicles; and (e) an MOS photo diode array.

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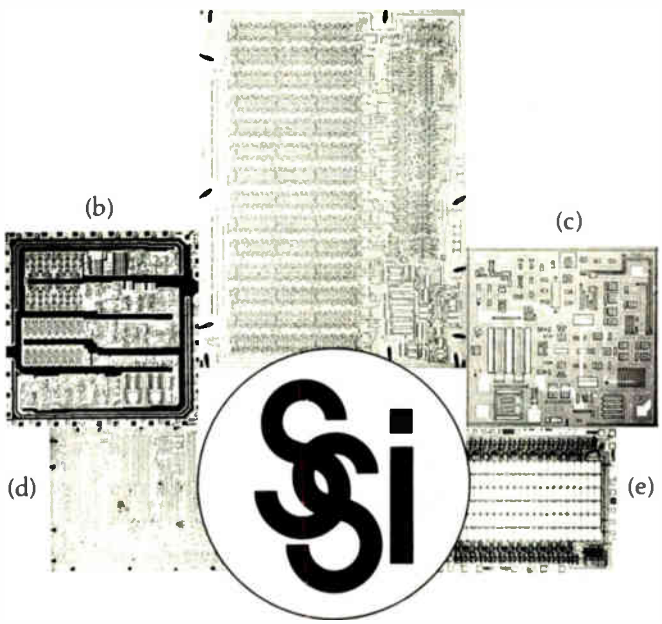
(a)



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SCIENCE/SCOPE

Fiber-optic cables allow sensitive information to be transmitted across unsecured areas without the need for encryption. A new communication link built by Hughes for the U.S. government connects command centers to computers in separate buildings with hair-thin glass fibers. Alarms are triggered anytime there is an unauthorized attempt to obtain access to the link. The new link, which may transmit at rates as high as 100 million bits per second, is less costly and allows considerably more system flexibility than protected wire systems using conventional security techniques.

Improved processing techniques have created silicon solar cells that produce 15 percent more power than their predecessors in converting sunlight into electric power for spacecraft operations. Advanced cells developed by Spectrolab, a Hughes subsidiary, generate 20 milliwatts of power per square centimeter. The increase in power is attributed to improving the thermal and optical properties of the cell and to a chemical etching method that sculpts microscopic tetrahedrons (pyramids) on the cell's surface. The result provides a dull-surfaced cell that abosorbs more sunlight than cells with polished surfaces.

Using special temperature-controlled chambers, NASA scientists will create clouds for study aboard Space Shuttle flights in the early 1980s. To properly form clouds in the weightlessness of space, the chambers, which are flat-plate heat pipes, must be extremely level over a large area (2'x3'x3/4") and uniform in temperature to within $.01^{\circ}$C. Neither requirement has ever before been met in a heat pipe of this size. Hughes, under contract to General Electric, is developing eight isothermal vapor chambers to form the inner walls of the Atmospheric Cloud Physics Laboratory. The project is managed by NASA's Marshall Space Flight Center at Huntsville, Alabama.

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A new traveling-wave tube for use in the ground terminal transmitter of commercial satellite communications systems has been developed by Hughes. The Ku-band device, designated Model 876H, provides 700 watts of CW power over the frequency range of 14.0 to 14.5 GHz. It incorporates a two-stage collector that enhances efficiencies to greater than 41 percent over the operating band. This design decreases total beam power when the drive level to the tube is reduced, making the tube desirable for operation in a pulsed mode, and minimizing the primary power drain when operating in the small signal region.

Computer processes multiple instruction sets, multiple data streams

by John Gosch, Frankfurt bureau manager

Prototype machine uses microcomputer modules to perform 32 million operations per second

Computer architectures based on arrays of microprocessors and memory are increasingly popular research topics because they promise the most cost-effective means of achieving high processing power. This segment of advanced technology is coming a step closer to reality in a new prototype system from West Germany's Siemens AG that features the unusual capability of simultaneously processing multiple sets of instructions on multiple streams of data.

Using a total of 128 microcomputer modules, engineers at the firm's research laboratories, located in Munich, have built what they call a "structured multimicroprocessor system" (SMS), in which the modules operate in parallel to tackle a problem jointly.

Parts. Each module solves a small element of the problem—a part of a partial differential equation, for example. Such partitioning of the overall problem simplifies programming, Siemens says, even though it must be done by the programmer. Any relationships or interactions between elementary problems are taken into account by exchanging the interim results between individual modules.

The SMS 201, now in its prototype stage, boasts a computational capability equivalent to that of a large mainframe, says Rudolf Kober, the SMS project engineer. For elementary operations, the instruction stream amounts to 32 million operations per second; for floating-point operations, it is 550,000 operations per second. With more powerful devices, the instruction stream can be increased tenfold to a hundredfold, Kober says.

The system has a memory capacity of 2.5 megabytes, evenly distributed over the 128 microcomputer modules. Since these modules are self-contained units (see the photograph above), they can be programmed in the conventional manner using any available programming language.

Each of the modules consists of a central processing unit with program and data memory, an input/output interface, and a communication memory. These components, all part of Siemens' SAB8080 microprocessor family, are linked via an interconnection network to a main processor. The latter, typically a small process computer of Siemens' 300 series, coordinates the system inputs and outputs, selects and starts the module programs, and controls the single data bus on which all the data exchange takes place.

SMS is the latest of several experimental multiprocessor machines. It joins, most prominently, International Computers Ltd.'s distributed-array processor and Massachusetts Institute of Technology's data-flow computer [*Electronics*, April 27, 1978, p. 69; April 26, 1979, p. 92] in reaching the prototype stage. (Delivery of the first ICL machine, originally scheduled for early this year, has been moved back to late 1980.)

Contrasts. The SMS 201 distinguishes itself from most other multiprocessors in several ways, Kober asserts. Unlike a machine with a fixed size, the modularly constructed system can be made either smaller or larger to handle less or more complex tasks at hand. In contrast, ICL's machine is less modular.

Also, its use of standard microcomputers, programming languages, and operating systems gives the SMS 201 a high price/performance ratio. What's more, each module can handle a program on its own, in contrast to the processing elements of comparable machines—for example, MIT's distributed-array processor—in which a single program in the main processor controls a number of processing elements in an instruction-by-instruction fashion.

Combining the advantages of array processors with those of decentralized multiprocessor systems, the SMS concept features central control of all its modules and provides a high degree of parallelism. As a result, says Kober, it is possible to translate a problem consisting of a number of coupled subproblems into subprograms for the microcomputer modules. Moreover, the amount of intermodule data exchange, which represents the interaction between the subproblems, is small compared with

Multiple. The SMS 201 array processor uses 128 of these microcomputer modules. At top right are RAM chips. Along upper left are four PROMs; directly below is the CPU, to its right the RAM control. Bottom section is bus coupler. I/O ports are at top.

the amount of calculations each module performs.

Of note is how the SMS concept uses the communication memories (CM). Each microcomputer module has access only to its own CM. All communication between individual modules, as well as between them and the main processor, is controlled and carried out by the main processor through these memories.

Benefits. To be sure, this organization requires more hardware than one based on a common CM, Kober points out, but it makes programming and applications easier. Also, it avoids conflicts over access, a problem encountered, for instance, in MIT's data-flow machine, whose microprocessors continuously access a common memory. The absence of such conflicts, he says, considerably enhances a system's high-speed computational capability.

As a typical application, Kober cites weather forecasting over areas as large as, say, one hemisphere of the earth. Siemens is also trying out various other applications. Among them are the prediction of the paths of space probes under the influence of the various planets, stability computations in power-generation and -distribution facilities, the calculation of the propagation of ultrasonic waves, and spin-model simulations in solid-state physics.

The firm says that samples of the system as currently configured will be available shortly.

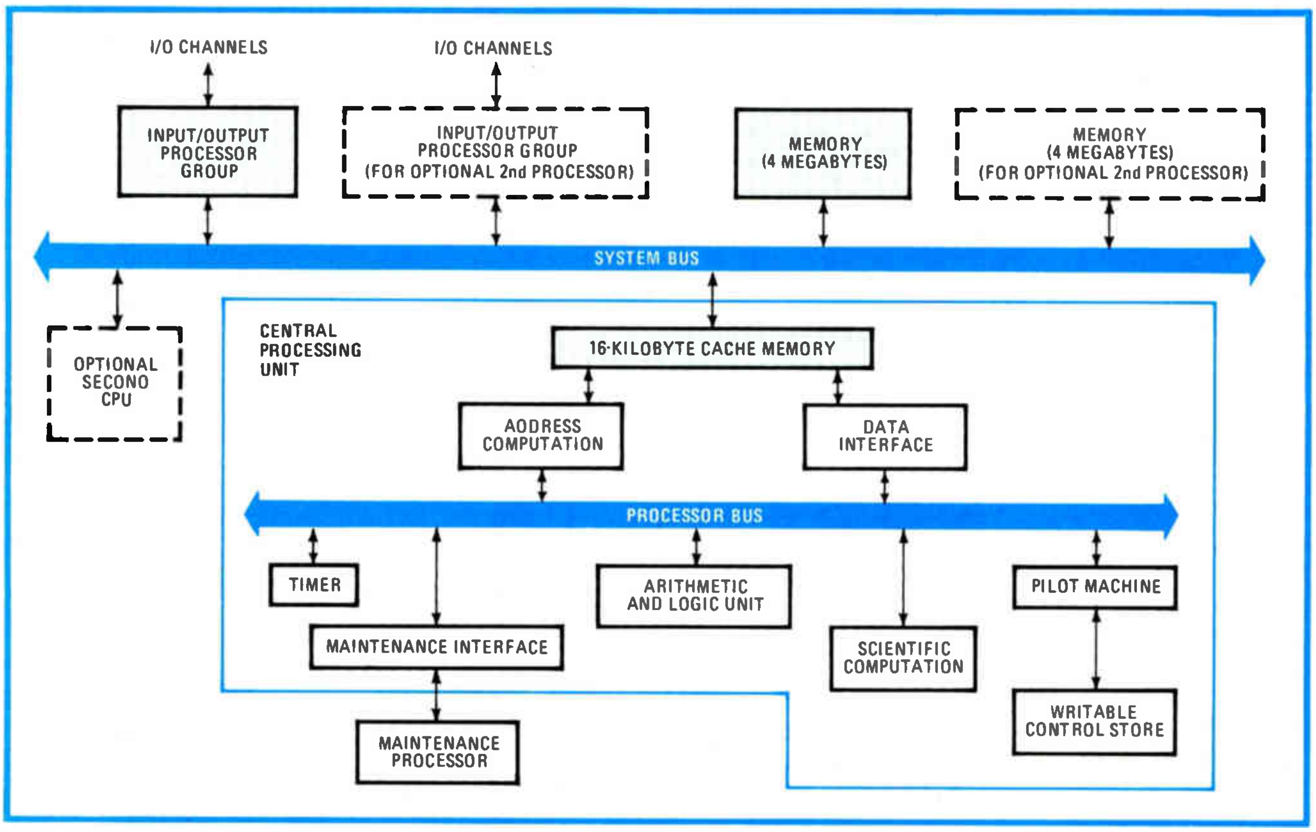
France

CII-HB launches merged product line with two bus-oriented mainframes

CII–Honeywell Bull unveiled last month the first elements in its new product line. The bus-oriented uniprocessor DPS 7/80 and its sister multiprocessor, the DPS 7/82 [*Electronics*, Sept. 27, p. 71], are the first pieces of major hardware from the Paris-based computer company's Unysis program.

Unysis is a three-year-old effort to bring about the convergence of the different lines of the two companies that merged in 1976 to form CII-HB—La Compagnie Honeywell Bull, the French subsidiary of Honeywell Information Systems Inc., and La Compagnie Internationale pour l'Informatique. The key to CII-HB's solution is extensive use of microprogramming in the DPS 7 systems' distributed internal architecture, made possible thanks to large-scale integration and lower costs for semiconductors.

Compatibility. The microcode that makes the system compatible with the company's three existing product lines is stored in a memory having a



Mass transit. CII–Honeywell Bull has opted for a bus-oriented architecture for its new line of computers, which is compatible with the three previous lines of its predecessor companies. The central bus can handle data-transfer rates of up to 36 megabytes/s.

capacity of 12,000 64-bit words. It is written in 56-bit words, with 8 bits added for error detection.

"The use of microcode gives us enormous flexibility," explains Jean-Julien Gahviler, a technical consultant on CII-HB's corporate marketing staff, "enabling us to drastically transform internal architecture without substantial modifications as far as end users are concerned."

The various modules in the DPS 7 mainframes are arranged around a 32-bit-wide bus that can handle data transfer rates of up to 36 megabytes per second (see figure). Linked directly to this central bus are the central processing unit (or units for the DPS 7/82); four input/output processors (up to 12 more can be added to the 7/80 and 28 more to the 7/82); and the main memory units, with up to 4 megabytes capacity for the uniprocessor and twice that for the multiprocessor.

The input/output processors can support I/O channel speeds of 2.5 megabytes per second and an aggregate I/O rate of 29 megabytes per second. Up to 21 peripheral devices can be supported by the 7/80, and up to 45 devices by the 7/82. For communications, up to 256 lines can be attached to the 7/80, whereas the 7/82 can support as many as 512 communications lines.

The CPU, with an internal cycle time of 110 nanoseconds, is likewise organized around a central bus. A 16-kilobyte cache memory is directly linked to the CPU module. "We put it there instead of with the main memory in order to keep the bus as unencumbered as possible," Gahviler says.

Logic. All of the processors use current-mode logic (CML) in a master-slice gate-array configuration, with the master-slice circuits being provided by RTC–La Radiotechnique Compélec, Honeywell, and Nippon Electric Co. Current levels within the CML integrated circuits are constantly monitored to provide a warning of possible overheating or other malfunction.

This technology is the same one that Honeywell Information Systems originally encountered problems with and then solved in its ill-fated 66/85 computer [*Electronics*, March 30, 1978, p. 46]. CII-HB says it opted for CML for both its high integration possibilities and its speed.

Using its automated packaging techniques, in which ICs fixed to a sprocketed tape are automatically mounted on a ceramic substrate, CII-HB says it can make up to 40 input or output connections per chip, with each chip containing an average of 35 logic gates. What's more, it notes that CML is five times faster than transistor-transistor logic and more than twice as fast as emitter-coupled logic. **-Kenneth Dreyfack**

Denmark

All-digital telephone instrument lowers system costs, adds features

With digital technology pushing hard into telephone systems, the major manufacturers are devoting much attention to electronic switching hardware, the systems' intelligent nerve centers. Still, they have not neglected the nerve endings.

A new generation of electronic instruments has begun to emerge, bringing to ordinary household subscribers the new services that phone systems can offer. Judging from the Sept. 20–26 Telecom '79 in Geneva, the quadrennial telecommunications fair sponsored by the United Nations' International Telecommunication Union, the front-running European instrument right now is the all-digital Digitel 2000, developed by Standard Elektrik Kirk A/S, a Danish subsidiary of International Telephone and Telegraph Corp. Challengers, though, should turn up fairly soon in France, West Germany, and elsewhere.

Standard Elektrik Kirk's instrument converts analog speech signals into digital pulse-code-modulated (PCM) signals that can be passed directly to a digital exchange. "The 2000 itself will cost more than a conventional instrument, but the overall cost for the phone system will be less," says Vagn Robert Wissing, the firm's technical director. With the Digitel, he explains, there is no need for expensive analog-digital interfaces at the exchange. Also, he points out, because the set has an electronic buzzer, the phone network does not need to supply a 90-volt ringing voltage.

Testing. The Jutland telephone company, which is installing an ITT system 12 digital exchange in its network, obviously sees merit in Wissing's arguments. It will start running field tests next year in the town of Juelsminde with between 100 and 200 instruments. "They want to check out the effects of PCM sets on their network," he says.

The Digitel transmits PCM signals at a rate of 80 kilobits per second. The format is a 10-bit pattern—8 bits for the speech sample, 1 for signaling, and 1 for synchronizing. Drawing 50 milliamperes from the 48-V supply on the phone line, the set can operate on loops up to 3 kilometers long.

Kirk based the design on an Intel 8048 microprocessor and programmed a batch of conveniences for users. The number of the caller, for example, shows on the set's 16-digit light-emitting-diode display until the receiver is picked up, information that presumably will be welcome to most subscribers at least part of the time.

Number, please. Up to four unanswered calls can be stored and their numbers called back on the display. The set will dial these numbers automatically if that is wanted.

It also has room in its memory for up to 50 numbers for abbreviated dialing (only 10 are implemented in the prototype sets). What's more, if a caller wants to know how much a conversation is costing, the instrument will meter tariff pulses and display the charges as they run up.

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Electronic dictionary has many talents

An electronic translator from Sharp Corp., to go on sale in Japan next month, features 48 kilobytes of read-only memory together with sophisticated logic and display-control circuits. The use of complementary-MOS and a liquid-crystal dot-matrix display enables it to run for about 1,000 hours on three silver-oxide cells.

Designed as a substitute for a Japanese-English, English-Japanese dictionary, the unit is intended primarily for Japanese people learning English. It displays English words in the standard Roman alphabet, either upper- or lower-case, but Japanese words are displayed only in the katakana syllabary—there are no phonetic equivalents in the Roman alphabet to aid an English speaker in the pronunciation of new words.

Each of the 16 characters of the display is a five-by-seven-dot matrix. Entries longer than 16 characters are scrolled. The dimensions of the case are 6.3 by 3.2 by 0.65 inches.

The translator, designated the IQ3000, is based primarily on words rather than phrases. It has a central-processing-unit and two display-control chips, and it has four 12-kilobyte ROMs encoded with a total of 2,500 English words, 300 English compounds, and 5,000 Japanese words.

Conjugations of English verbs are provided, and the dictionary form can be called up from another tense at the push of a button. For example, starting with "bought" will call up the dictionary form "buy," the conjugation "buy, bought, bought," or the Japanese translation: "verb transistive, *kau, konyu suru.*" Also available are the singular and plural noun forms and the adjectival form, together with its comparative and superlative.

As another example, starting with the noun "flower" yields the Japanese equivalent, *hana,* with the parenthetical remark *skokubutsu,* meaning plant. Pushing the button for the same sound or meaning turns up "nose," and depressing the button for the Japanese translation again yields *hana,* with the parenthetical remark "face," followed by *kyukaku,* which means olfactory organ.

The unit also has a key that will call up homonyms or synonyms. Furthermore, it has a test key for checking the spelling of an English word, with a reply of "good" or "wrong." It can also process incorrect or incomplete information. For example, if a user tries to translate "speake," the display will respond with "speak?" If the button for Japanese is then depressed, the translator will display "v [for verb] *hanasu.*"

Using the search key, a user can start with the fragment "ab" and search for words starting with those letters. Successive depressions of the key will bring forth "able?" "about?" and "above?"

Also included in the unit's capabilities are eight-digit, four-function arithmetic calculations, percentage calculations, and a memory that can provide the cumulative total of a series of calculations, store a number for later use, or store a constant for use in calculations. **-Charles Cohen**

calculator built in. "We had a few bytes left over and thought that would be a good way to use them," explains Erik Stridbaek, the project engineer for the Digitel 2000.

Along with 8048, the key circuits in the subset are a Mostek 5156 coder-decoder, an Intersil 6561 1-kilobyte random-access memory with battery backup, and six operational amplifiers for a Chebyshev filter. This lineup will change somewhat when Kirk starts mass-producing the instrument.

To cut power consumption, it will shift to a complementary-MOS microprocessor like the Intersil 80C48. The RAM could well be a nonvolatile type, eliminating the battery. The firm also plans to integrate the filter on a single chip. **-Arthur Erikson** intel delivers.

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Such a system is a virtual reality. For example, the Bell System's Advanced Communication System (ACS) is a digital data network, linking computers, intelligent terminals, facsimile devices and printers in real-time. Linking them, and also providing data processing functions that essentially make a time-sharing computer system.

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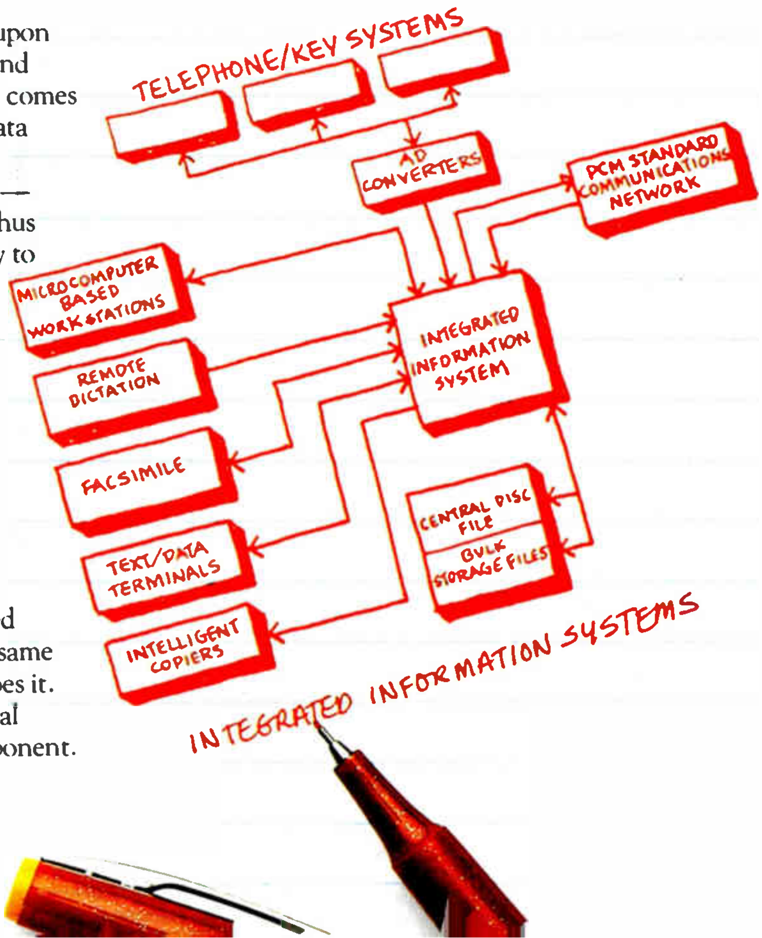
The microcomputer—invented by Intel in 1971—has been the key component that's made possible distributed processing networks, with central computers linked to remote "smart" terminals, printers and local processors.

Today, the biggest obstacle to the growth of such networks is the cumbersome analog-based



transmission system. One alternative—already in use—is to use satellites to bypass the traditional transmission system. To compete, the telecommunications industry will have to convert to the high speed, wide bandwidth of digital transmission. And, ultimately, "telecomputerization" will require the extension of digital standards to the subscriber station.

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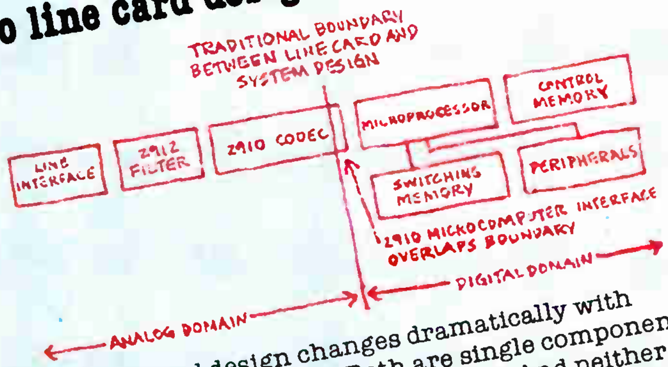

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Plug-compatible makers face doubts

Mergers, led by National-Itel deal, and other realignments are the rule as industry seeks to counter IBM's moves

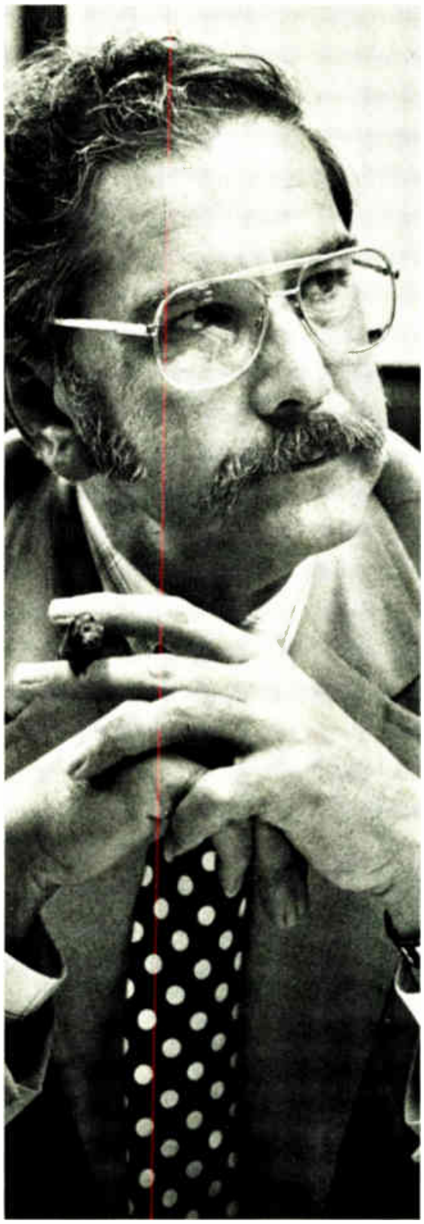
by Bruce LeBoss, West Coast Editor, Computers & Instruments

Suppliers of computers and peripheral devices that are plug-compatible with those of International Business Machines Corp. are apparently taking a new tack in the wake of the dramatic hardware and software offerings embedded in IBM's new 4300 computers.

They are joining forces through mergers, equity positions, or other associations with a view to shoring their positions, or becoming more formidable competitors. But whether the plug-compatible industry will be able to weather this and future storms created by the industry leader remains in doubt.

Perhaps the most striking evidence of this new trend is the agreement late last month between National Semiconductor Corp. of Santa Clara, Calif., and Itel Corp. of San Francisco. Itel's computer marketing and service operations in the U. S., Canada, Europe, and Singapore were transferred to National, effective on Oct. 1. Itel had been marketing and servicing IBM-compatible central processing units manufactured by National for the past 2½ years, but the firm recently posted a $60.2 million loss in its second fiscal quarter due to an even larger operating loss by its Data Products Group.

In a letter to directors and plant managers, National's president, Charles E. Sporck, notes that the arrangement with Itel worked very well from the first shipment in March 1977 through calendar year 1978. However, he adds, "the computer industry was surprised by IBM's announcement of a four-times price/performance improvement for its 4331 and 4341 machines" introduced in January 1979. "The resulting decrease in computer profitability for Itel is one of the factors which has contributed to their financial difficulties," and, he continues, "they found it difficult to get orders from prospective customers because they were not certain Itel would be able to continue to support their requirements."



Taking over. National president Charles E. Sporck is leading his firm into computer marketing and servicing business with its takeover of Itel Corp.'s operations.

Sporck calls the latest National-Itel accord "a logical step in our commitment to being a major factor in the growing computer marketplace." He says he believes that this combination "will result in significant efficiency improvements, a reduction in overall inventory levels, and thus a much more competitive force." He further states that Itel has developed very capable computer marketing and servicing teams "and having them join National will accelerate our program to become a full-service computer supplier."

Keeping company. National is by no means alone in this approach. In midsummer of this year, Amdahl Corp. in Sunnyvale, Calif., a manufacturer of IBM-compatible computers, began merger negotiations with Santa Clara–based Memorex Corp., a producer of plug-compatible peripherals. Neither firm entered the marriage talks from an overwhelmingly strong position. Amdahl suffered an 89% earnings decline in its second quarter on a much smaller drop in revenues. Amdahl president John C. Lewis commented that new-product announcements made by IBM constituted one of the main factors that "caused customers to delay decisions to acquire new computers."

Meanwhile, Memorex was having its difficulties. Although net income before extraordinary credit and revenues in the second quarter increased 3% and 14%, respectively, over the comparable period a year ago, earnings for the year are "unlikely to reach a 25% increase, which was previously indicated to be achievable," says Robert C. Wilson, president. The Memorex chief executive notes that the second quarter was "characterized by a continuation of IBM's aggressive actions" and that these actions concurrently reduced prices and caused customers to delay purchase decisions.

"IBM's actions have compounded the profit pressures of inflation, energy, and recession," according to Wilson. "The effects of all of these factors," he says, "have been reflected in our second quarter results and have affected others in our industry." Memorex has since forecast that its third quarter profit is expected to be significantly below year-earlier levels. Again, the firm says that is largely caused by competitive price actions and lower-than-anticipated order rates.

Still another alliance of sorts involves plug-compatible peripherals manufacturer Pertec Computer Corp., Los Angeles, and North American Philips Corp., the New York–based firm that intends to acquire approximately 45% of Pertec's outstanding common stock. Interestingly, North American Philips is an affiliate of NV Philips Gloeilampenfabrieken of the Netherlands, which, in turn, is linked to the United States Philips Corp. That firm owns semiconductor manufacturer Signetics Corp. and Two Pi Corp., the Santa Clara–based manufacturer of IBM-compatible computers. Thus, the transaction, if approved, may provide Two Pi with a friendly source of peripherals with which to face IBM in the systems marketplace.

Quién sabe? Whether these alliances, and others that are surfacing, will strengthen the plug-compatible industry is uncertain. But one thing that is certain, according to Grant S. Bushee, associate director and computer industry specialist at market researchers Dataquest Inc. of Cupertino, Calif., is that "IBM made a very big statement with the 4300 announcement. It was geared to get the PCMs [plug-compatible manufacturers] and was a strategy to minimize the erosion of IBM's market share by those firms." "It told the world," he adds, "that IBM can meet the PCMs on the battlefield and beat them."

National's Sporck thinks otherwise. In a letter welcoming Itel's Data Products Group employees to National, the official notes that "the computer industry has taken a dramatic turn in recent months." But, he says, "we feel that an aggressive semiconductor-based manufacturing and marketing company can evolve into a major supplier to the computer marketplace. Together we are a real computer company, with all the necessary pieces in place—technology, total systems experience, proven manufacturing capability, and a highly competent marketing and service force. Together, we offer our customer the alternative for state-of-the-art computing."

Some doubt. However, industry observers question the ability of National to succeed in the computer business in view of the firm's decision to shelve its system 200 and 400 computer programs and what they refer to as a not-too-successful Starplex development system. "I frankly don't see the synergism with their existing semiconductor business, other than that their computers will use their semiconductors," says Dataquest's Bushee.

Most microprocessor companies have taken a route of making a gradual transition into system-level products. National, in contrast, "is making a complete leapfrog into mainframe computers," Bushee says. "They are saying: 'We are not going to walk before we run, we're going to gallop.'" The semiconductor business is a commodities business, and, he continues, "to jump into a business that is service- and support-oriented and requires them to come up with end-user solutions is mind-boggling. If they can pull it off, it's a major coup."

Some of the other proposed alliances may, indeed, result in more efficient and formidable rivals to IBM. An observer of Amdahl and Memorex notes that the combination of these two firms would give them greater financial stability and improved financial resources. "Memorex brings to Amdahl memory technology, both in the peripherals and add-on fields. If they can put some of their resources into that area and offer some new capabilities to the marketplace, they will be able to enhance their overall CPU offering," he says. What's more, he adds, Amdahl has management talents, more so than Memorex, that it brings to this proposed marriage. "This combination would indeed make them a more potent competitor for IBM," he states.

Getting products out. Furthermore, Memorex already has a large sales and service organization worldwide and is especially strong in Europe, according to another computer industry analyst. "Its strength is in distribution, and they are able to move products out to the marketplace very rapidly. Having more products to sell, namely, those of Amdahl," he says, "would make it a more cost-effective operation.

James Geers, marketing vice-president at Two Pi, sees little or no benefits coming to his firm as a result of the North American Philips–Pertec deal. "There is nothing happening from a business standpoint, although I could use all the help I could get," he states. Pertec makes a tape drive that, Geers says, is "the only synergistic equipment." "However, I consider that to be the least important element," he adds.

What benefits, if any, will materialize as a result of the plug-compatible manufacturers joining forces against IBM cannot be seen at this early date. But whether any are needed is questionable inasmuch as most of the plug-compatible manufacturers, "from big to small, have not dropped out of the business," says Dataquest's Bushee. Furthermore, "all are telling a story that they're as strong as ever," he states.

According to Bushee, there really is no reason why plug-compatible manufacturers should not do well in the future. "Plug-compatibility of computers will be increasingly common, because the price of hardware is going down while that of software is spiraling." □

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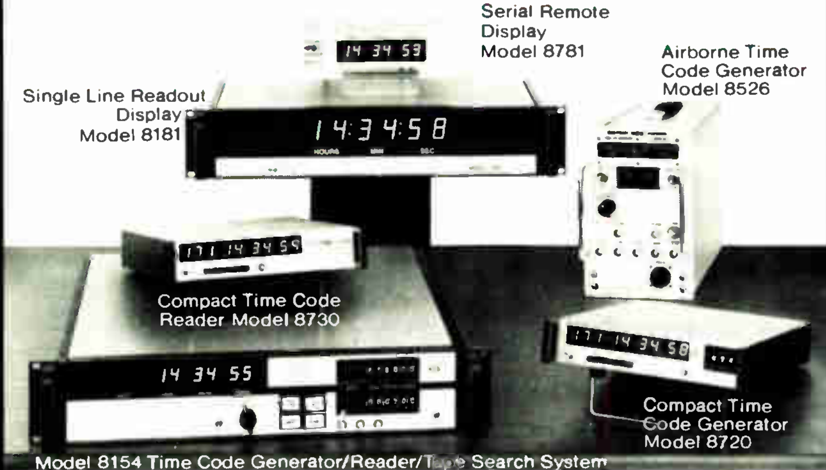

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Packaging & production

Fine-line lithography nears its day

Optical techniques can be pushed beyond 1-μm widths, while masking technique permits 200-angstrom lines

by Jerry Lyman, Packaging & Production Editor

Semiconductors are moving into what has been called the second integrated-circuit revolution, one whose end is submicrometer geometries. And those responsible for providing the means to that end, who develop the systems and the science with which such circuits will be manufactured, found two surprises waiting for them late last month at their Semicon/East meeting in Boston.

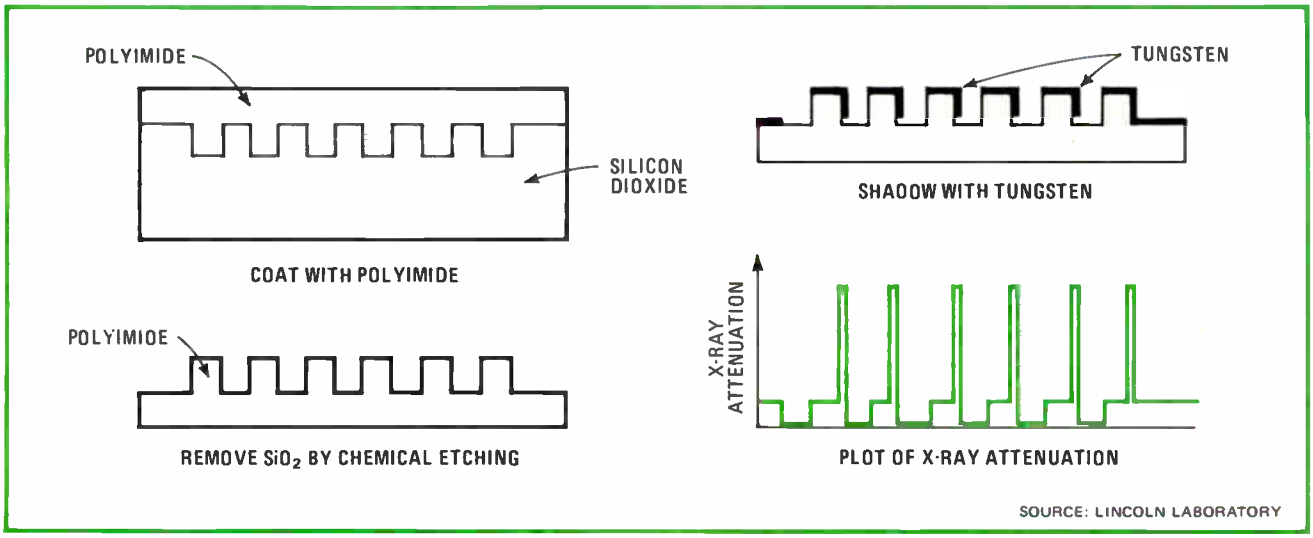
First, the possibility of submicrometer geometries punches a hole in the conventional wisdom, which maintains that 1-micrometer line widths are the limit of optical lithography. Second, X-ray lithography has progressed much further than most in the industry have supposed; in fact, a masking technique that makes possible 200-angstrom lines in silicon was described. Today's limit is 500 to 1,000 Å.

All that news emerged from the same Semicon session. There, David Markle of Perkin-Elmer Corp., Norwalk, Conn., told his audience that "optical lithography is going to be pushed much further than most people expect." In fact, he surmises that it could conceivably reach the 0.5-μm region before bottoming out.

Markle showed how the limits of optical lithography are related to the numerical aperture (the sine of the angle between the outermost ray entering the objective and the optical axis) of the lens system, the wavelength of the light source, the sensitivity of the photoresist, and mask-to-wafer alignment.

Photolithography will move toward the use of deep ultraviolet light sources (2,000 to 2,700 nanometers) and higher numerical apertures, Markle said. However, he noted, application of deep ultraviolet to 1:1 projection photolithography would require new resists, special silica mask substrates, a high-intensity light source, and accurate alignment. Of all these requirements only the mask substrates are readily available [*Electronics*, May 24, p. 29]. As Markle was speaking, Perkin-Elmer was demonstrating on the conference floor an automatic alignment system with a 0.125-μm alignment accuracy that could possibly be suitable for a deep-ultraviolet 1:1 projection system.

The machinery, shown in the photo opposite, uses a pattern-recognition system coupled with edge-detection techniques. A television camera views the sharp edges of the alignment targets, and information is then processed through edge-detector circuitry and memory buffers to a microcomputer. Alignment is completed whenever a small diamond on the mask pattern is symmetrically nested and centered within a large diamond on the wafer pattern. This system will be avail-

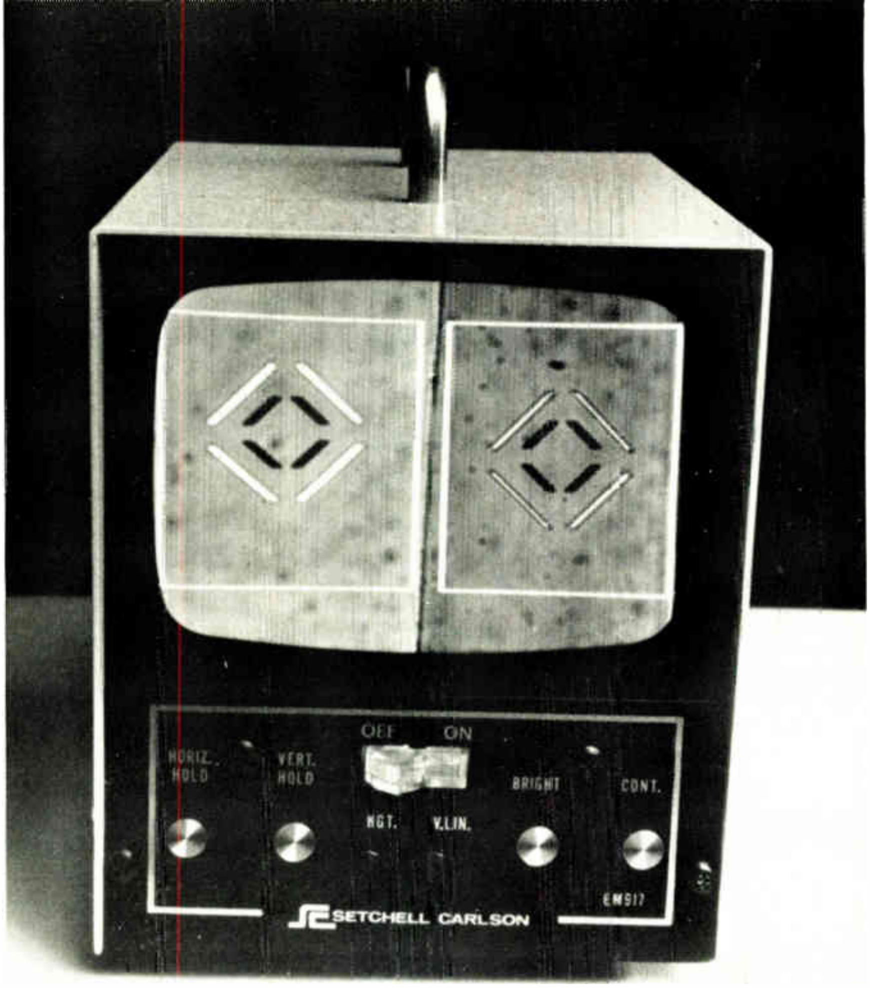


Shadowed. These are the steps in fabricating a shadowed polyimide X-ray mask with a square-wave profile. The SiO_2 square-wave structure is made by reactive ion etching. Masks of this type, combined with a carbon K X-ray source, have exposed 200-angstrom lines.

able in the second quarter of 1980.

Perhaps most pertinent in Markle's presentation was a comparison of today's optical systems with possible alternatives that have improved parameters. The latest Perkin-Elmer projection aligner has a numerical aperture of 0.164 and operates around the 3,900-nm wavelength, resulting in a minimum line of 1.78 μm. Typical step-and-repeat projection aligners have numerical apertures of 0.27 and operate at 4,360 nm, resulting in a minimum line width of 1.2 μm, but they have less throughput. But a 1:1 projection aligner with the same numerical aperture as the present Perkin-Elmer system and a 2,700-nm deep ultraviolet source and silica optics could possibly expose 1.1-μm lines.

Markle sees a possible breakthrough if a projection aligner (probably a step-and-repeat) with a 0.24 aperture and a 2,500-nm source could be developed. The result would be an optical machine capable of imaging 0.78-μm details. Of course, with an even higher numerical aperture, shorter wavelength, and a more sensitive photoresist, optical techniques could conceivably reach 0.5 μm. But this is pure conjecture.



Automatic alignment. Pattern recognition and edge detection permit Perkin-Elmer system to get 0.25 μm alignment accuracy on projection aligners also made by the company.

The X-ray picture. X-ray lithography has for some time been capable of putting 0.1-μm (1,000 Å) images on a resist-covered wafer. So why, two researchers from MIT's Lincoln Laboratory were asked, has progress been so slow? Disagreeing that it has been slow, Harry Smith and D. C. Flanders insisted that X-ray techniques have made great advances.

Smith pointed out at the Semicon technical session that while present electron-beam scanning systems have data rates of 1 to 2 megahertz, X-ray systems can handle equivalent data rates of 50 to 100 MHz. With synchrotron X-ray sources, equivalent data rates approach 1 gigahertz.

He also said that Lincoln Lab was building an X-ray lithography machine aiming for a mask-to-wafer alignment accuracy of 200 Å. A laser interferometric alignment using wafer and mask gratings is to be used, a principal already demonstrated. Such a method should give accuracies comparable to those of present scanning electron-beam systems, the most accurate known. Lincoln Lab investigators are also looking at X rays generated from hot plasma as a possible exposure source for their new machine.

But for Smith's listeners, the best was yet to come, when he brought news of a new method that allows X-ray lithography to expose 200-Å lines onto a substrate.

To create such a precisely controlled line, Lincoln Lab developed a new way to fabricate high-contrast X-ray masks. The technique is based on the deposition at an oblique angle—or shadowing—of X-ray absorber material onto relief structures having triangular or square cross sections. The relief structure consists of a polyimide membrane.

For the typical line, a square-wave surface relief structure is fabricated in silicon dioxide by reactive ion etching. This structure is then transferred to polyimide by molding. The silicon dioxide is then removed by etching, and the remaining polyimide surface is shadowed at an angle of 30° with 200 Å of tungsten. The mask is replicated by a carbon K X-ray source into 600-Å-thick polymethyl methacrylate, a resist, coated on an SiO_2 substrate.

The 200-Å linewidth is the narrowest such structure produced by any lithographic technique to date on a thick substrate. However, researchers at IBM Corp. already have made 80-Å lines with electron-beam techniques on thin self-supporting layers of graphite.

The new mask-making method is ideally suited to investigation of the ultimate resolution of X-ray lithography and to generation of simple device geometries. However, it is interesting to note that the method is based on a silicon dioxide (silica) rather than silicon substrate.

Noteworthy is Smith's agreement with at least one equipment maker, William Tobey, marketing director of GCA Corp., Bedford, Mass., on the future of step-and-repeat X-ray lithography systems based on reticles rather than masks [*Electronics*, Aug. 16, p. 109]. Such systems, they believe, will do the submicrometer work of the late 1980s. □

You and your career

EE shortage threatens growth

IC industry finds problems in hiring enough of the right people hasn't inhibited R&D yet, but leaders are worried

by William F. Arnold, manager, San Francisco region bureau

As semiconductor companies leave the '70s, hoping for equally smooth sailing in the '80s, they are increasingly concerned about a dark cloud on the horizon. "The bottom line of it all is that the limitation for our industry is the number of engineers, the number of good engineers," W. J. Sanders III, president of Advanced Micro Devices Inc. of Sunnyvale, Calif., warned an industry seminary recently.

To Sanders, "The debacle of the aerospace program in the 1960s dissuaded the students from the technical professions." The upshot for electronics companies is that "we don't have enough engineers—we're going to be burdened with that for the next decade."

Nor is Sanders on the West Coast the only one worrying about the availability of engineers. "The engineer shortage is real, and it's more severe in the IC field than in others," declares Robert S. Pepper, formerly vice president and general manager of the semiconductor division of Analog Devices Inc., Norwood, Mass., who recently became vice president of RCA Corp. and general manager of its Solid State division. He points out that the industry is growing at about 20% a year compounded and microprocessor production even more than that, while integrated-circuit complexity is growing, too. The result: not enough engineers to keep pace.

Ray Stata, Analog Devices' president, also agrees that "the most fundamental and enduring limitation to growth" of high-technology companies, and by implication to research and development, is the number of knowledgeable and skillful personnel available. A graphic observation about the shortage comes from a Southern California job consultant for many electronics companies: attrition from job-jumping is at a record high.

Broad impact. If the IC industry is being hit hardest, where are the shortages felt most? "Across the board," answers James Phillips, manager of personnel for American Microsystems Inc., Santa Clara, Calif. However, process engineers rate first with Roy Brant, vice president for human relations at National Semiconductor Corp. in Santa Clara. He observes that any engineering job that has no glamorous aspects is hard to fill. Swen Simonsen, vice president and technical director for Advanced Micro Devices, adds circuit and product engineers to his list. To fill slots in its integrated circuit operation in Austin, Texas, Motorola Corp. is having a tough time finding enough circuit designers, as well as product and process engineers, states Norman Skelton, who as corporate recruiting manager works at the Schaumburg, Ill., headquarters.

Analog Devices' Stata explains the problem this way: a sudden increase in demand for engineers creates a dynamic shortage that is exacerbated by the fact that it takes

Keeping 'em down on the farm

Recruiting engineers may be only half the battle, though, because keeping them may be just as hard as hiring them. Semiconductor Corp.'s Roy Brant, vice president for human relations, for example, says the arrival of newly hired engineers at higher salaries "obviously creates a compression problem" with engineers hired a year or more before. To quell disgruntlement and departures, National regularly reviews its employees to stabilize salaries among those hired within a three-to-five-year period. After that, "people seek their own level," he observes.

Intersil Inc., which claims a substantially lower turnover rate than its competitors, helps solve the problem with a clever cash profit-sharing plan. Every six months, 10% of the profits—which are running better than 8½% of salaries—are distributed to employees, according to Tim Hough, technical recruiter. But only 5% of the profits are distributed in the first six-month period. The rest, or 3½%, are divided and distributed during the next two six-month periods, Hough explains. In other words, it would take a new employee 18 months to receive his first full six-month cash profit-sharing sum. Naturally, the excess over 5% each period overlaps and builds during good times, the longer an employee stays with the company.

Motorola's Norman Skelton, corporate recruiting manager, describes another plan. Motorola has developed a "technical ladder" concept. Heretofore, technical people felt they had to go into management to get higher salaries. But the technical ladder approach provides a "parallel career path" aimed at reassuring the engineer who wants to stay on the technical side that he can do it and keep up financially with his management counterparts, Skelton says.

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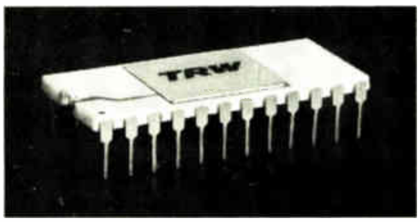

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five years on average to graduate an engineer and another five years of experience for him or her to reach professional maturity. He gloomily predicts that "unless we have another severe recession, we are in for a prolonged period where demand for professionals, especially technical professionals, will simply exceed the supply."

Consequently, some worry that research and development, the lifeblood of progress—and potentially larger market shares in market areas for companies—might suffer. Acknowledging that there has been some difficulty, AMD's Simonsen says that, so far, "no programs have suffered in any material way" but concedes "that doesn't say that in the next year it might not become a problem. Jerry Welch, employment manager at Mostek Corp., Carrollton, Texas, says that R&D is hurting no more than other areas.

Two-year deal. As RCA's Pepper explains, "As the chip grows, the amount of development engineering needed goes up just about in proportion. It now takes about two years to develop one or more complex chips—that's two years of development time, with maybe a little research added in." So, he cautions that "managers have got to be very careful how they allocate human resources today—can you imagine investing two years of company time in a dud product?"

At Motorola, however, R&D probably hurts less over the short pull than the product areas. The reason, the company explains, is that R&D is more of a long-range proposition when it comes to recruiting. Consequently, Motorola believes that recruiting for engineering and development programs can be planned more effectively.

Even so, if companies are chasing a limited pool of talent, how do they compete against each other and recruit the engineers they need? L. J. Sevin, board chairman and chief executive officer of Mostek, states that today's EEs are looking for three things. The first is money, and Sevin says that any EE job-hunter who isn't emphasizing that in

Machine aids

As much as slick recruiting and retention plans help, RCA Corp.'s Robert S. Pepper, general manager of the solid state division, points out another tack for managers: "There are artificial ways to ease the engineer shortage, like computer-aided design, circuit analysis, layout, and cell libraries. Still, it takes a pretty talented engineer to get the most out of available CAD." Consequently, "I think the next step will be CAD tailored for less brilliant engineers," he predicts.

today's market is a "damn fool." He thinks a close second is "the challenge of the job." A poor third on Sevin's list of engineers' desires is job security.

Not everyone totally agrees. Money is not the cause for engineers' changing jobs, counters AMI's Phillips. "Engineers themselves don't want to move," he says. Phillips sees the key as giving people a technological environment in which to work on challenging state-of-the-art projects. However, AMI has an employee-retention program that seeks to identify causes of turnover, reduce stress, and improve communications with managers. Phillips also says that AMI recently helped relieve its engineer shortage by hiring six EEs from England.

Bounty system. A common and fairly successful method used by companies to find engineers is to give bonuses to employees who refer candidates. For example, Intersil Inc., Cupertino, Calif., gives from $150 to $500 per engineer who is successfully hired, according to Tim Hough, technical recruiter. Of course, the most common method is newspaper and periodical advertising where an ad in a prominent publication will cost anywhere from $500 for one of modest size to $2,000 for a quarter page. When the costs are totted up, a company can spend anywhere from $3,000 to $5,000 to catch one prize semiconductor engineer. But some companies complain that their recruitment costs go up when they have to use outside employment agencies. ☐

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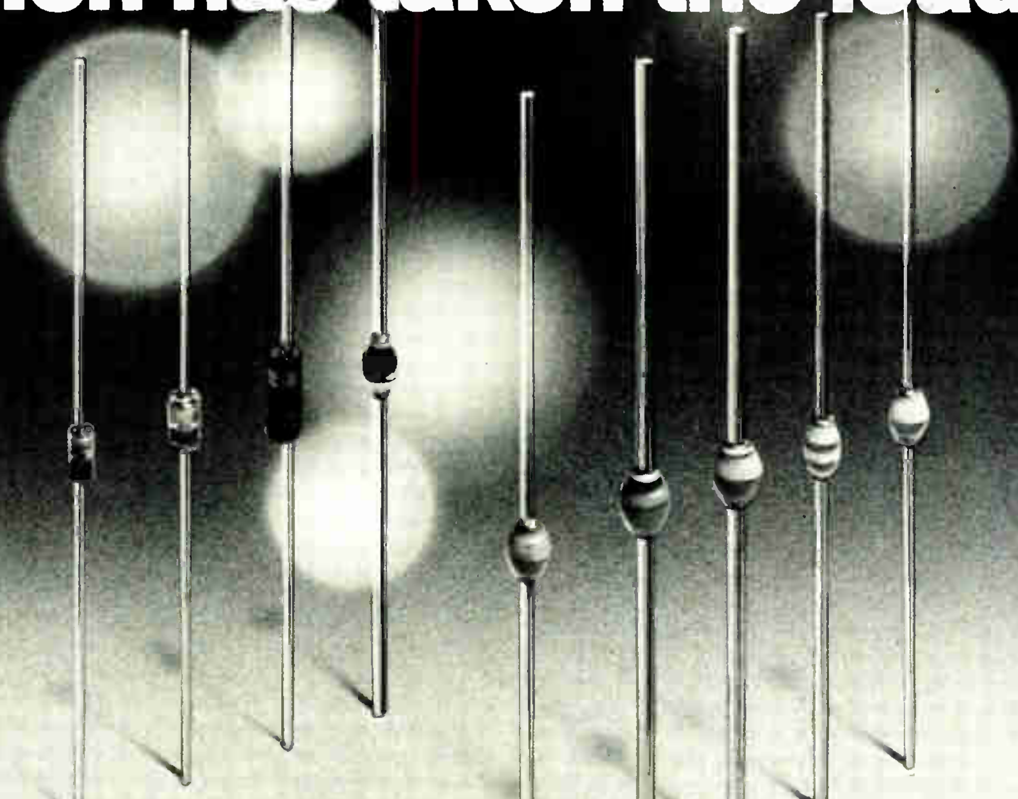

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BYW 52–BYW 56[1])[2])	200 V–1000 V	2 A	≙ 1N 5059–1N 5062
BYW 72–BYW 76	200 V– 600 V	3 A	
BYW 82–BYW 86[1])[2])	200 V–1000 V	3 A	≙ 1N 5624–1N 5627
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Military electronics

ASPJ: a $1.5 billion ECM market

Navy leads development of Airborne Self Protection Jammer as Air Force drags its feet and NATO watches and waits

by Ray Connolly, Washington bureau manager

As the market for airborne electronic countermeasures continues to expand and flourish, manufacturers are keeping a close eye on the military's newest and largest effort, the Airborne Self Protection Jammer (ASPJ), as it moves into engineering development.

Beyond its $1.5 billion potential, ASPJ bears other good news. For one thing the modular system proposed for use in four Navy and two Air Force planes is expected to advance the state of the microwave art in integrated circuits and high-power traveling-wave tubes while bringing down costs. For another, it will introduce a new approach to competitive production and perhaps generate new business within the North Atlantic Treaty Organization. Should NATO and other U. S. allies like Israel adopt the ASPJ, overall sales potential could jump from the 1,600 to 1,700 systems for American use to as many as 5,000 over the decade beginning in 1986.

The bad news for the ASPJ involves getting full Air Force collaboration in the Navy-directed program despite a Department of Defense mandate making it a joint effort. Navy–Air Force program conflicts are nothing new, of course: "It's like trying to mix oil and vinegar," opines one frustrated Pentagon official. But the Air Force in this case believes that it already has a "next generation" standard tactical jammer for its McDonnell Douglas F-15 Eagle in the ALQ-131 pod now being produced by Westinghouse Electric Co. and that it will get a better one by updating its newer ALQ-135 for the General Dynamics F-16 multimission fighter.

Competition. First deliveries of the ASPJ, designated the ALQ-165, are not scheduled until early in fiscal 1986, with production—following engineering development, prototype fabrication, and flight tests—to be divided between the two companies on the winning team. The two development teams consist of ITT's Avionics division and Westinghouse's Aerospace and Electronic Systems division, which got $15 million in late August; and Northrop Corp. and Sanders Associates, which received $12 million for the 15-month competition. Losing in the early competition were the teams of Cutler-Hammer's AIL division and Loral Electronics, and of the California-based electronic-warfare operations of Raytheon, Hughes Aircraft, and Tasker Systems.

To receive a package. Among the aircraft designated as possible recipients of the antijamming equipment is the F-14 Tomcat. Its gear would include a second wideband jammer.

Splitting a winning development team into competitors for production is a new approach that the Naval Air Systems Command believes could cut costs by 15% to 40%. Navair's Capt. Walter G. Carlson, an electronics engineer who has made a career in electronic warfare systems, says production shares would be split between the two winning companies "on a disproportionate basis, say 60–40, with the lower price getting the larger share."

As ASPJ's program manager, Carlson sees the goal as "getting a 20-times extension of an aircraft's life [through successful countermeasures] at a cost of 5% of its flyaway price." That compares with a 12% figure for the Navy A-4 Skyhawk attack jet's electronic countermeasures (ECM) package, he says, the capability of which "is one fifteenth that of the ASPJ."

Carlson's design-to-cost goal is $330,000 in constant dollars for each ASPJ package. Each consists of a computer-controlled receiver and a processor linked to the Navy's ALR-67 or the Air Force's ALR-62 and

Northrop's ECM money machine

Perhaps the biggest economic impact from the post-Vietnam surge in defensive electronic countermeasures (ECM) will come in Rolling Meadows, Ill., not far from Chicago and the home of Northrop Corp.'s Defense Systems division. Radar-jamming ECM is the Los Angeles based company's fastest growing product line. To accommodate that growth, Northrop disclosed at the end of September that it will invest $8 million to expand its Rolling Meadows operations by two thirds with the addition of another 200,000 square feet of plant space and next year will hire another 500 workers. That will bring the job level to 2,700, including the 550 persons added this year.

Although Northrop will not say precisely how much its ECM business contributed to its 1978 corporate sales of $1.8 billion, the company offers these clues for the arithmetically oriented: Northrop's 1978 ECM sales were 38% higher than the year before and more than double those of 1976. For 1979, the company estimates that those sales will jump another 58% from the 1978 high.

ALR-69 radar warning receiver, plus two wideband transmitters for jamming high and low frequencies. This 230-pound package can be either pod-mounted or installed internally (as a replacement for the aging ALQ-126) on board the Navy's attack and fighter versions of the F-18 Hornet, now under contract to Northrop and McDonnell Douglas.

A 350-lb ASPJ version augmented with a second wideband jammer operating at even higher frequencies is proposed for internal mounting on larger planes like the Navy's A-6E Intruder and its tactical jammer counterpart, the EA-6B Prowler, and the F-14 Tomcat fighter. Grumman Aerospace builds all three, as well as the Air Force EF-111's tactical jammer, another ASPJ candidate.

Trends. Navair's Carlson sees a variety of technological opportunities as his new program moves to counter a perceived increasing Soviet threat. Opportunities to advance the state of the art generally fall into four categories: large-scale integration, radio-frequency processing circuits, microprocessors, and traveling-wave tubes. But Carlson is also convinced that the ASPJ must successfully demonstrate the performance of its "critical items"—like higher power traveling-wave tubes spanning broader frequencies, hybrid microwave circuits, and high-speed memories—in the first two years of the program as well as get "a firm handle" on their costs.

One school of thought in the ECM business holds that the Navy-directed program will be better motivated to meet those goals so long as the Air Force continues to hang back and explore other operations, such as improvements of its ALQ-131 and the ALQ-135.

For example, the Westinghouse ALQ-131, now in its third production run, operates in five bands, employs replaceable modules that permit up to 16 configurations for a variety of missions, and incorporates a programmable digital computer in the control and interface module, which also contains a digital waveform generator that can produce up to 40 simultaneous waveforms for deception modulation. Navair's Carlson knows all that, of course, but notes that the ASPJ "is better and has even wider frequency coverage."

What rankles some ASPJ proponents is that NATO nations are still not ready to commit themselves to adopting the new system until the Air Force goes beyond its present obligation to use 75% of the ALQ-165's components in the comprehensive power management system for the ALQ-131. "NATO wants to see if the Air Force is willing to go all the way and use ASPJ in the F-16," says one contractor's man. "After all, the F-16 represents our first big common production program with NATO." Navair's Carlson concedes that responses to two ASPJ initiatives to NATO and a third to West Germany have not yet produced a commitment, although he notes that the West German air force is exploring a new ECM package of its own. □

Companies

How tough is Gould?

Executives of companies taken over by conglomerate say its reputation as a heartless master is undeserved

by Larry Marion, Chicago bureau

Now that they have been left waiting at the altar twice this year in attempts to take over semiconductor makers—the latest jilting coming when Mostek Corp. instead eagerly grasped the hand of United Technologies Corp.—executives of Gould Inc. must be wondering about the reputation their company has acquired as a corporate headchopper.

This must be especially true in view of opinions expressed by executives of several companies acquired in the last few years by the $1.8 billion conglomerate with headquarters in Rolling Meadows, Ill. The consensus appears to be that Gould does not interfere with the internal operations of a new division if it produces the expected revenues and profits—admittedly a big if. One such executive, John A. Blaeser, general manager of the Modicon Corp. subsidiary, says, "Gould is primarily concerned with sales and earnings growth for stockholders. If you produce, it's a good place to work. If you don't do what you said you were going to do, you get hit with a two-by-four." Blaeser is unbruised: his Andover, Mass., firm was an $11 million manufacturer of programmable controllers when it was acquired in 1976; today it is an $80 million performer.

Well run. Despite that pressure—not unlike the stresses at many other companies—some present and former executives maintain that the advantages of working with Gould outweigh the disadvantages. "It's the best-run company I've ever seen in my life," says David J. Blecki, now general manager of Biomation Inc. in Santa Clara, Calif., a maker of digital logic analyzers. He and others at Modicon and elsewhere say that Gould permits existing management to remain with a company unless it fails to perform.

Mostek finds its white knight

When Mostek Corp. of Carrollton, Texas, found out that Gould Inc. had agreed to buy the 21% of its stock owned by Sprague Electric Co.—1.2 million shares for $51.5 million, or $42 a share—the first thing it did was look for a way to exercise its 60-day option to match that deal. The second thing it did was hire Martin Lipton, a New York attorney who is something of a specialist in fighting unfriendly takeovers [*Electronics*, Sept. 27, p. 34]. Lipton had in fact represented Fairchild Camera and Instrument Corp. in its successful effort to escape a takeover by Gould and before that helped McGraw-Hill Inc., the New York publisher, in its maneuvering to avoid an unfriendly acquisition by American Express Co. earlier this year.

This led to step three, the announcement late last month that Mostek had found its white knight in the person of United Technologies Corp. of Hartford, Conn. The result was a handshake between Mostek chairman L. J. Sevin and United Technologies chairman Harry J. Gray over a deal that calls for Mostek to buy the 1.2 million Sprague shares at $42 and then resell them to United at the same price. For the rest of Mostek's roughly 6 million shares, United will offer $62 apiece, making a total outlay of some $385 million. That should make everyone happy except Gould.

But there are other concerns when Gould takes over. One of them is pressure to introduce new products. To encourage cross-fertilization of technologies among the diverse parts of a company that manufactures transformers, oscilloscopes, batteries, automatic test equipment, mechanical bearings, and propulsion systems, Gould operates several laboratories that do basic research. It also sponsors numerous internal technical symposiums to familiarize designers with the latest advances at other divisions and subsidiary companies.

In addition, it encourages informal information exchange. Says Donald J. Kramer, formerly group vice president for Gould's Instrument and Controls Group and now president of Henrix Electronics Inc. in Manchester, N. H., "They try to cross-fertilize through transfers of people, by putting people from different divisions in close proximity to one another. Cross-fertilization happens by osmosis."

Typical of Gould's approach to a new acquisition was its treatment of Modicon. Kramer says that chairman William T. Ylvisaker and other senior officials practice a "bottom-up" style of management: "They said, 'You know your business better than we do, so you tell us what you're going to do.' "

Gould's interest in motivating its key people makes the company a lucrative place to work. Ylvisaker is dedicated to motivating personnel, as current and former staff members will attest. "A good measurement of an electronics company is if it can keep the high technologists, the free thinkers. At Modicon, the manage-

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Determined. Gould chairman Ylvisaker has made acquisition of a circuit maker a must.

ment team has remained intact," notes Blaeser. In fact, Ylvisaker's motivational zeal extends also to health and physical fitness. An avid sports buff himself, he has had athletic facilities installed at Gould's Rolling Meadows headquarters.

In court. However, foes of Gould acquisitions point to the legal battles it has become entangled in with the Federal government, as well as with unwilling takeover targets. When it moved unsuccessfully to acquire Fairchild Camera and Instrument Corp. last spring, there were lawsuits by both companies alleging violations of antitrust and securities laws [*Electronics*, May 24, p. 58], plus notices of investigations by the Securities and Exchange Commission and the Federal Trade Commission. The SEC said it wanted to investigate a Fairchild charge that Gould had leaked its intention to buy Fairchild to encourage speculative stock purchases, and the FTC said it was seeking information about "interlocking personal relationships."

Moreover, when Gould acquired I-T-E Imperial Corp., an electrical products manufacturer, the largest deal of the 30 it has completed in the last 11 years, the result was a consent decree with the SEC. Foes also point out that Gould conducted a housecleaning of I-T-E management. That, concedes former group vice president Kramer, was an exception, but not unfair. He adds: "I never saw an action that I disagreed with." □

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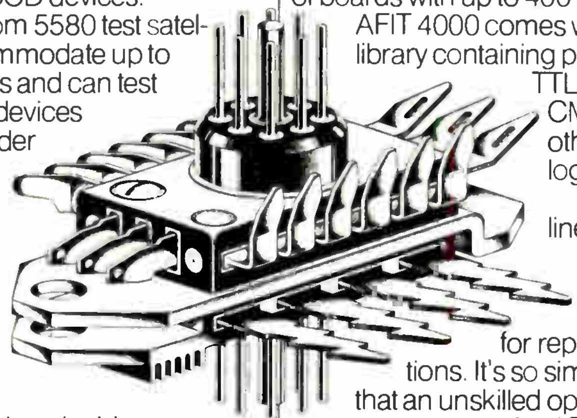

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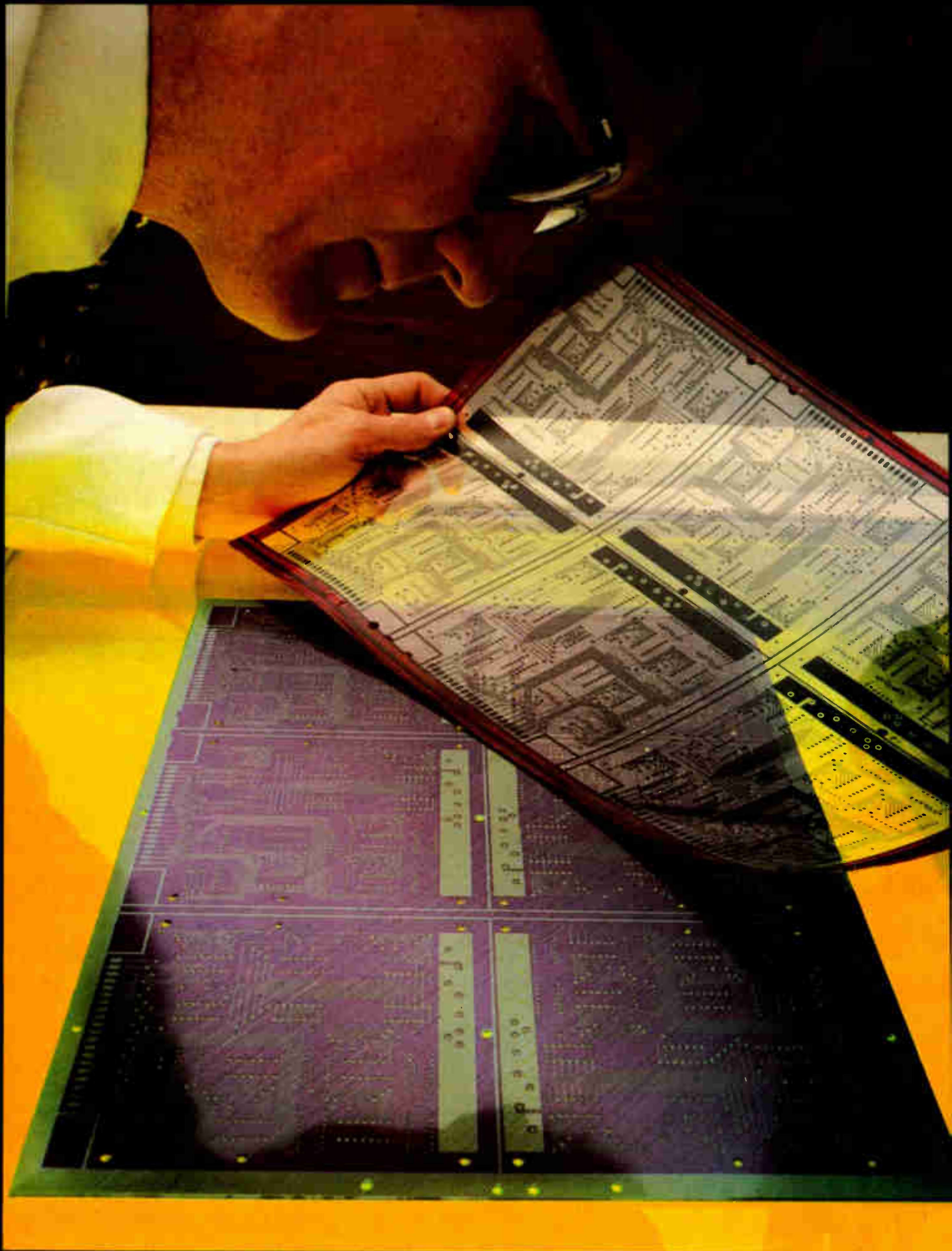

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5-volt-only, nonvolatile RAM owes it all to polysilicon

Electrons tunneling to and from floating gates back up static cells in 1-K n-MOS memory

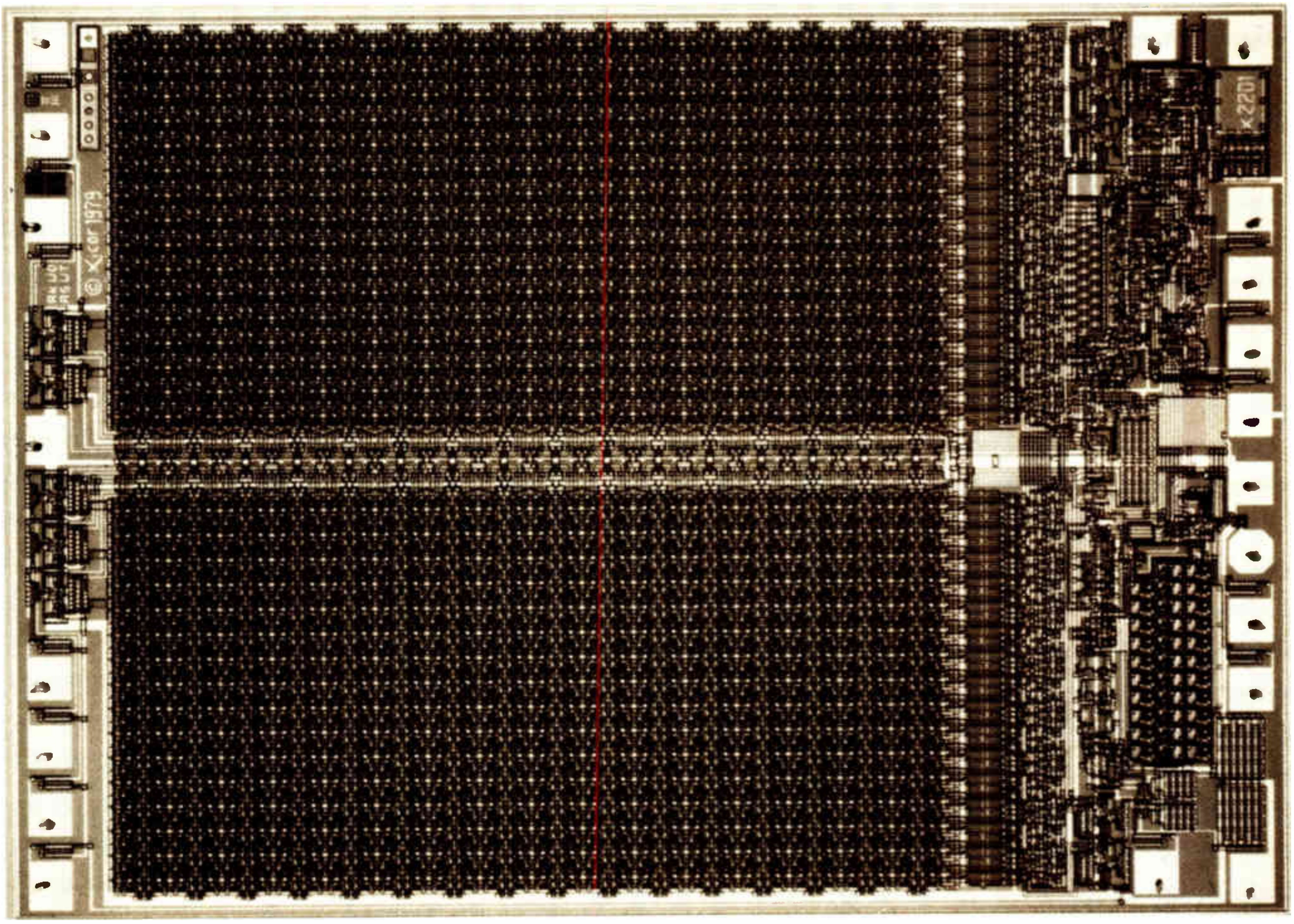
by Raphael Klein, William H. Owen, Richard T. Simko, and Wallace E. Tchon, *Xicor Inc., Sunnyvale, Calif.*

☐ The search for a nonvolatile semiconductor random-access memory has led in many weird and wonderful directions. Some devices can be programmed only infrequently or only with high voltages, while others need batteries as backup or expensive quartz lids for erasure by ultraviolet light.

Two new nonvolatile static RAMs dodge all these problems. They are as easy to use as a standard 2102-type memory, but they have the bonus of a nonvolatile backup—which is achieved by transforming what was formerly a limitation of standard n-MOS silicon-gate technology into a unique kind of storage mechanism.

The X2201 and X2202 devices therefore need no unusual materials or unusually thin layers. They deliberately tunnel current through their oxide layers to charge and discharge a floating-gate storage element [*Electronics*, Sept. 13, 1979, p. 39]. Also, they require only a 5-volt supply for any of their operations, and all their input, output, and control signals are TTL-compatible.

Both the devices contain a 1,024-by-1-bit static RAM with an access time of less than 250 nanoseconds. But both also contain a 1-K nonvolatile electrically erasable



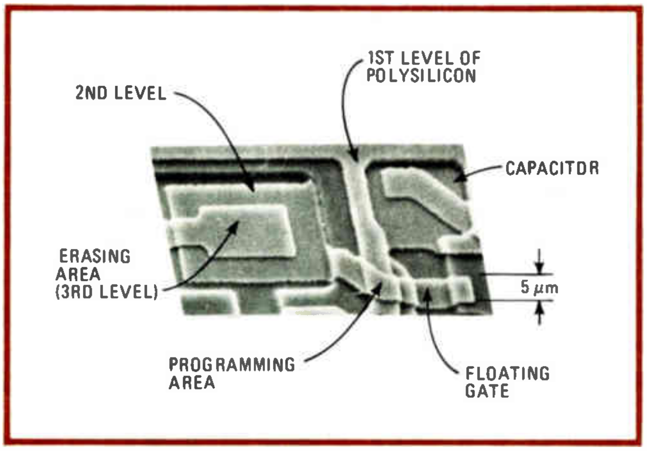
1. Two in one. In Xicor's memories, a nonvolatile matrix backs up a static RAM on a bit-by-bit basis. The photograph is of the X2201, wherein all nonvolatile data is restored to the RAM at once. In the X2202, also 118 by 164 mils in area, bits are brought back individually.

programmable read-only memory (EE-PROM) that "shadows" the RAM on a bit-by-bit basis. Data is written from the RAM into its nonvolatile counterpart by applying a TTL-level signal to a single pin. Thus, if power fails, the RAM's data can be saved by transferring it to the backup. On power up, however, the reverse happens automatically, and the same data will reappear in the RAM.

In the technology's present state, the number of floating-gate programming cycles may be limited to a range of about 10^3 to 10^6. However, unlike some other would-be nonvolatile RAM storage elements, floating-gate devices are excellent at retaining data and provide the unlimited number of read (recall) cycles that is the most important consideration in most of their applications.

The only functional difference between the 2201 and 2202 devices involves the recall to the RAM of the data from the nonvolatile array. With the 2201, a simple signal to the recall pin brings back the array's entire contents. (A photograph of the 118-by-164-mil die of the 2201 device is shown in Fig. 1.) With the 2202, bits are restored selectively—the address bus pinpoints a single bit for return to RAM.

The ability to electrically change nonvolatile data makes in-circuit programming of these devices feasible—writing, erasing, and reading without removing them from a circuit. The few previous devices to attempt this required impractically high voltages and complex voltage sequencing.



2. Closer look. A scanning electron microscope has captured most of a Xicor cell. It uses n-channel MOS technology and three polysilicon layers. The second forms a floating gate that collects and releases charge as the nonvolatile array is programmed and erased.

When a technology capable of high-volume production of nonvolatile electrically erasable RAMs has been sought for so long, it is ironical that n-channel silicon-gate technology, the current workhorse of the semiconductor industry, should prove fully capable of filling this role. In so doing, it uses three levels of polysilicon, one of which serves to provide the floating gates. These have a long record of reliability, as is evident from the popularity of E-PROM devices, which also use floating gates to store charge for indefinite periods of time but are erasable only by ultraviolet light.

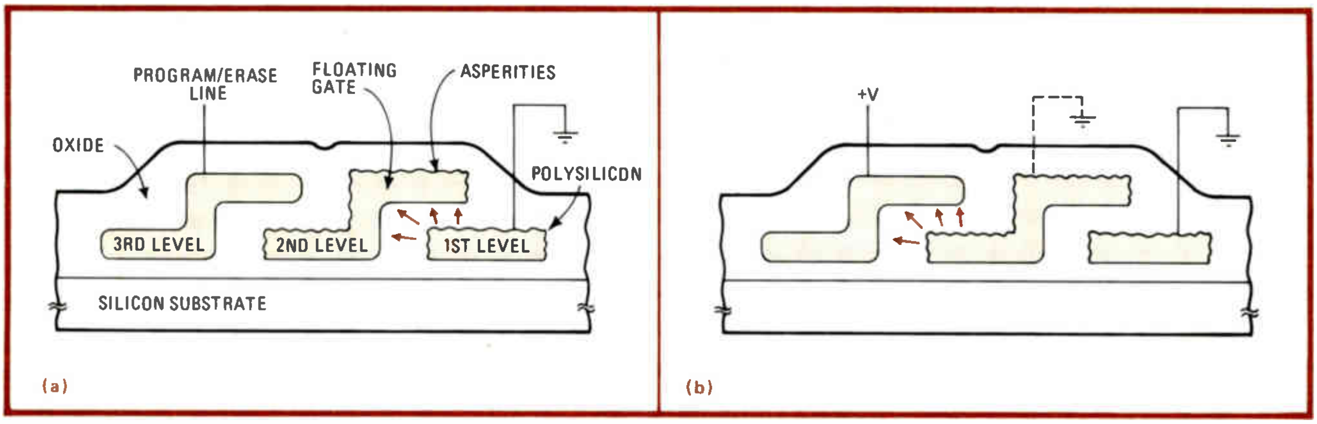
Birth of the idea

However, literature published by IBM Corp., Texas Instruments Inc., Siemens AG, and other corporations indicates that these gates could also form the basis of an electrically erasable memory. In brief, a floating gate is an island of conductive material surrounded by oxide and coupled capacitively to the silicon substrate to form a transistor. The presence or absence of charge on the gate determines whether the transistor is on or off. This charge, once on the gate and the charging voltage removed, will remain trapped indefinitely since the oxide normally acts as a barrier to the flow of current.

In the 2201 and 2202 devices, this oxide barrier is overcome by electrons that flow in response to a relatively low applied voltage between the floating gate itself and the two other polysilicon layers.

Originally, of course, multiple levels of polysilicon were used simply to increase the density of n-MOS silicon-gate circuits. The advent of low-pressure chemical vapor deposition of polysilicon made the process technically feasible on a large scale, and today large lots of wafers of this type are run routinely.

But it was observed for many years that a fairly low voltage would cause electrons to flow from one polysilicon layer to the next in unexpectedly large numbers.[1,2,3,4] This enhanced electron tunneling was found to be due to projections, called asperities, that exist uniformly across the surface of the polysilicon layer. The surface texture may be enhanced by growing oxide on the polysilicon within a particular temperature range. The triple polysil-



3. Hold and let go. The program/erase line is raised, coupling the floating gate to a positive potential. In (a), the gate is charged as electrons tunnel through oxide from the first-level asperities. The floating gate potential is lowered in (b), and electrons tunnel off for erasure.

In pursuit of the nonvolatile RAM

The use of nonvolatile storage to back up or shadow a random-access memory is not a new concept. Although the programming of an electrically erasable device remains a lengthy process, it need be carried out only when power falters. Thus by mixing a nonvolatile memory and a faster read/write memory on the same die, the user gains fast access to data that remains long after the power goes away.

In the U. S., General Instrument Corp. recently introduced a 1-K memory called the ER1711. Although it needs high voltages to program and erase its nonvolatile metal-nitride-oxide-semiconductor (MNOS) transistors, these can be easily derived from an external circuit that requires the same voltages that the chip uses for RAM operation: +5 and −12 volts. This same circuitry also allows simple pulses (from a microprocessor, for example) to control all data flow to and from RAM and EE-PROM.

The Toshiba and Hitachi designs (see table) are farther from practical application, but performance is being improved. For increased speed and for +5-V-only operation, both use n-channel MOS rather than the p-MOS technology usually associated with MNOS structures. While all the other approaches back up a static RAM, Hitachi shadows a dynamic RAM with what it calls dynamic injection MNOS, or DIMNOS. It currently uses three gates per cell but plans to go to two, at which time cell area will be reduced to only 0.62 mil² [*Electronics*, Sept. 27, p. 78]. And Toshiba hopes to build 4-K and larger nonvolatile static RAMs with 3-μm design rules.

The M 120 from SGS-ATES Componenti Elettronici SpA, Milan, Italy, bears the most resemblance to Xicor's chips though it is actually a quickly programmed EE-PROM rather than a RAM with backup [*Electronics*, May 10, p. 130]. In the 1-K memory, floating polysilicon gates retain data, and silicon nitride is not required. But unlike Xicor's parts, the M 120 requires an external +20-V supply for programming and uses complementary-MOS cells. SGS-ATES is also working on a 4-K memory and a 272-bit chip with automatic television tuning circuitry.

-John G. Posa

RANDOM-ACCESS MEMORIES WITH NONVOLATILE BACKUP

	General Instrument Corp. ER1711	Hitachi Ltd.	SGS-ATES M 120	Toshiba Corp.	Xicor Inc. X2201, X2202
Organization	256-by-4-bit static	experimental dynamic	256-by-4-bit EE-PROM	16-bit experimental static	1-k-by-1-bit static
RAM technology	p-channel aluminum gate	n-channel polysilicon gate	complementary-MOS polysilicon gate	n-channel aluminum gate	n-channel polysilicon gate
Nonvolatile element	MNOS transistor	dynamic injection MNOS	polysilicon floating gate	MNOS capacitor	polysilicon floating gate
Elements/cell	8 transistors, 2 MNOS transistors	3 transistors	6 transistors	6 transistors, 2 capacitors	8 transistors, 1 capacitor
RAM voltages	+5 V, −12 V	+5 V	+5 V	+5 V	+5 V
RAM access time	900 ns	100 ns	450 ns	100 ns	250 ns
RAM-to-backup voltage Recall voltage Erase voltage	−21 to −17 V* −15 to −10 V* +25 to +30 V*	+25 V n.a. n.a.	+20 V n.a. n.a.	+30 V n.a. −30 V	+5 V +5 V +5 V
RAM-to-backup transfer time	1 ms/3 days of retention	50 ns/cell +1 ms	2 to 100 ms	1 ms	2 to 4 ms
Recall time	100 to 300 μs	0	0	0	1 μs
Endurance	10^4 cycles	–	10^4	10^5 cycles	$10^3 - 10^5$ cycles
Package	22-pin	n.a.	18-pin	n.a.	18-pin
Comments	*supplied by external dc-dc converter that needs only +5 and −12 V	small cell size (< 0.62 mil²)	bit-alterable		X2201 has array recall X2202 has bit recall

SOURCE *ELECTRONICS*

icon process used for the Xicor devices exploits this tunneling effect. The scanning electron microscope photograph in Fig. 2 shows the relationship between the layers. The second of them forms the floating gate, a schematic of which is shown in Fig. 3.

The polysilicon electrodes in Fig. 3 are separated by oxide layers 1,000 angstroms or so thick. No appreciable tunnel current would be expected to flow through such a thickness without an applied voltage of 100 V or more. Yet the asperities help to create a reproducible flow of electrons in response to a much lower voltage.

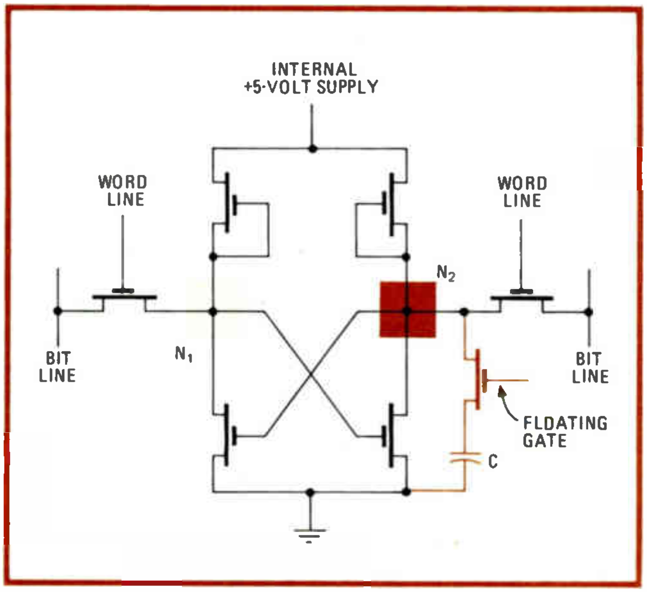
The method of programming (or adding electrons to) the floating gate may be understood from the first part of Fig. 3. As the program/erase line is brought to a positive voltage, it capacitively couples the floating gate to a positive potential. The programming electrode (the first level of polysilicon) is held at ground and, with a large enough electric field, emits electrons that are captured by the floating gate, making it negative.

For erasure (Fig. 3b), the floating gate is held close to ground potential while the program/erase line is brought high. To avoid the need for an extra polysilicon electrode, a switching transistor holds the gate to ground. With the established electric field between the program/erase electrode and the floating gate, the asperities on the gate emit electrons to the electrode so that the gate becomes positively charged.

The key mechanism

The floating gate is part of an n-channel transistor whose ability to turn on and off is the basis for the operation of the nonvolatile memory. When the memory is being programmed, the floating gate is charged with electrons, turning the transistor off; during erasure, electrons are removed from the gate, turning the transistor on. Hence a programmed floating gate is at a negative potential and an erased gate is positive.

Also worth noting is the fact that the enhanced electron tunneling mechanisms described are much more

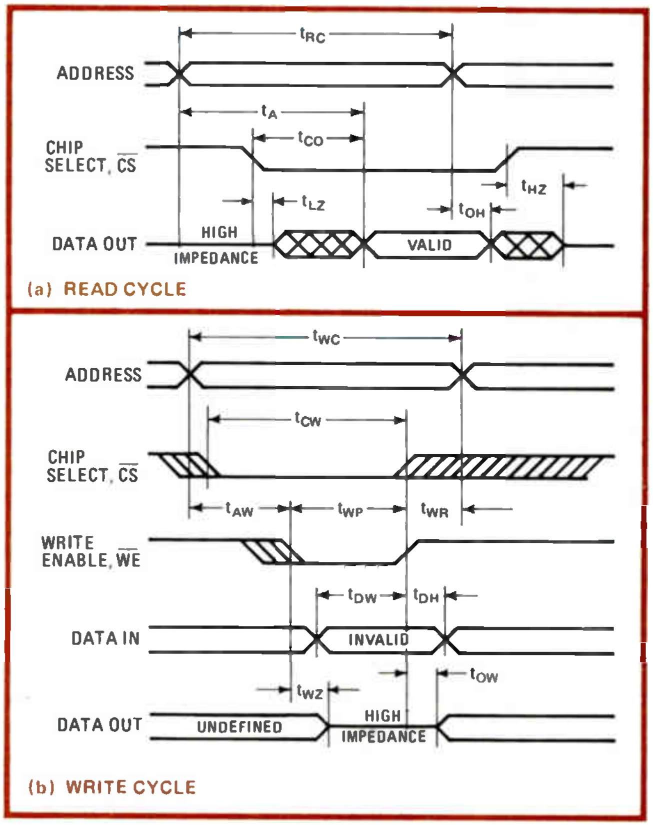


4. Flip-flop plus. The capacitor has no effect when the devices are used as RAMs. If the floating gate is charged, N_2's rise is slowed by the capacitor and the flip-flop latches with N_1 high. If the floating gate is off, the cell latches with the opposite polarity.

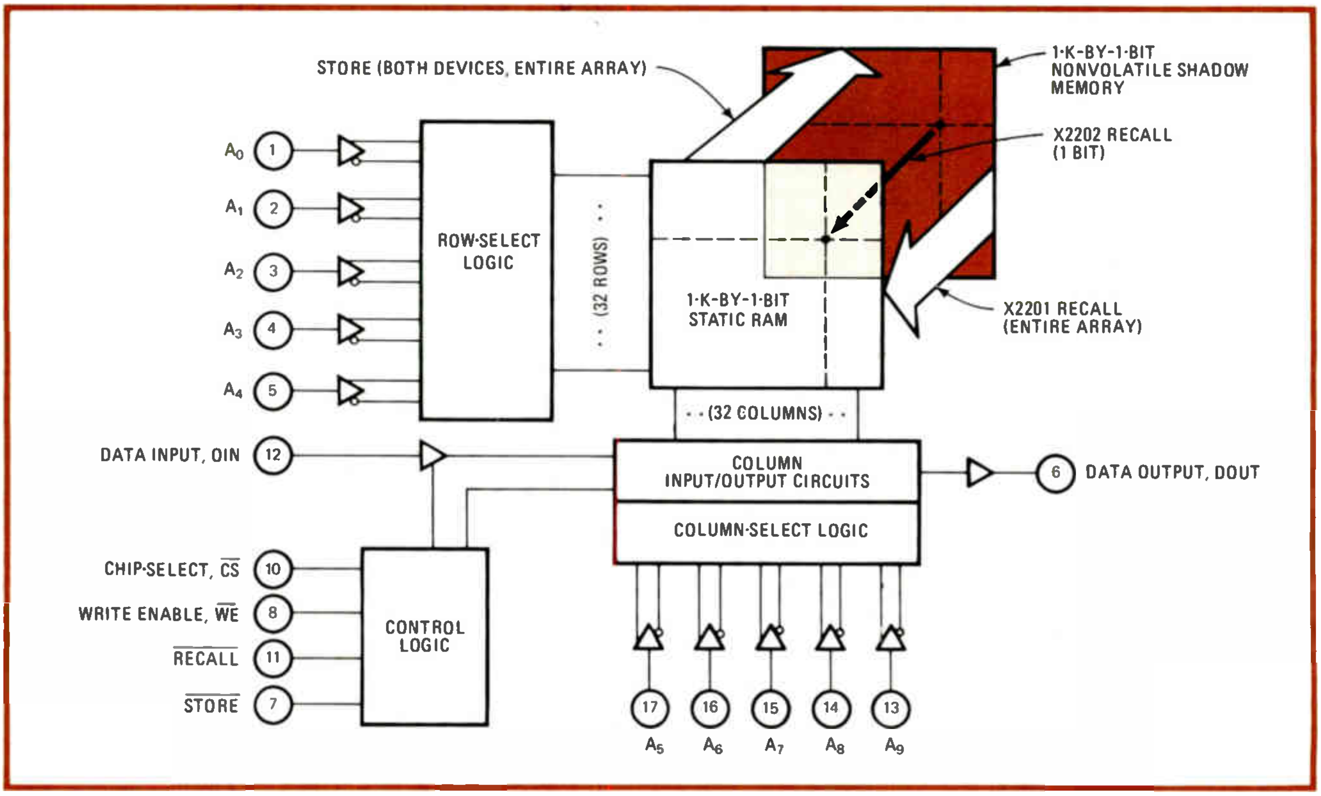
TABLE 1: RAM OPERATION (BOTH DEVICES)

Symbol	Parameter
Read cycle	
t_{RC}	read cycle time[1]
t_A	access time[1]
t_{CO}	chip select to output valid
t_{OH}	output hold from address change
t_{LZ}	chip select to output in low Z
t_{HZ}	chip deselect to output in high
Write cycle	
t_{WC}	write cycle time[1]
t_{CW}	chip select to end of write
t_{AW}	address to write setup time
t_{WP}	write pulse width[2]
t_{WR}	write recovery time
t_{DW}	data valid to end of write
t_{DH}	data hold time
t_{WZ}	write enable to output in high Z
t_{OW}	output active from end of write

1. 250 ns maximum   2. 150 ns maximum



5. Read/write RAM. These timing diagrams apply when the Xicor devices are operated as standard static RAMs. Part (a) is for reading and (b) is for writing. Timing is almost identical to that of 2102-type 1-K-by-1-bit memories, and access time is less than 250 ns.



6. The shadow knows. The store and recall functions are depicted by arrows to and from parallel planes. Both devices come in 18-pin packages, but the actions initiated by the recall pin are different for the two devices. Pin 9 is ground and pin 18 is for power.

efficient than techniques using avalanche breakdown, or hot-electron emission. With these, only a small fraction of the programming current ever reaches the floating gates. The large currents therefore drawn in such inefficient structures, combined with their high voltage requirements, are not consistent with the trends in large-scale integration. The program-erase voltage internal to the 2201 and 2202 devices can be generated on chip because the current requirements of the efficient tunneling structure are exceedingly small.

Nonvolatile elements that can be completely integrated on chip with no external supply other than the standard +5 V will enjoy widespread use as memories and in microcomputers and fault-tolerant systems.

A nonvolatile static-RAM cell

The 2201 and 2202 nonvolatile static RAMs mate a standard six-transistor depletion-load static RAM cell and a nonvolatile element at each memory location (Fig. 4). Interfacing the nonvolatile element to the static cell is the floating gate.

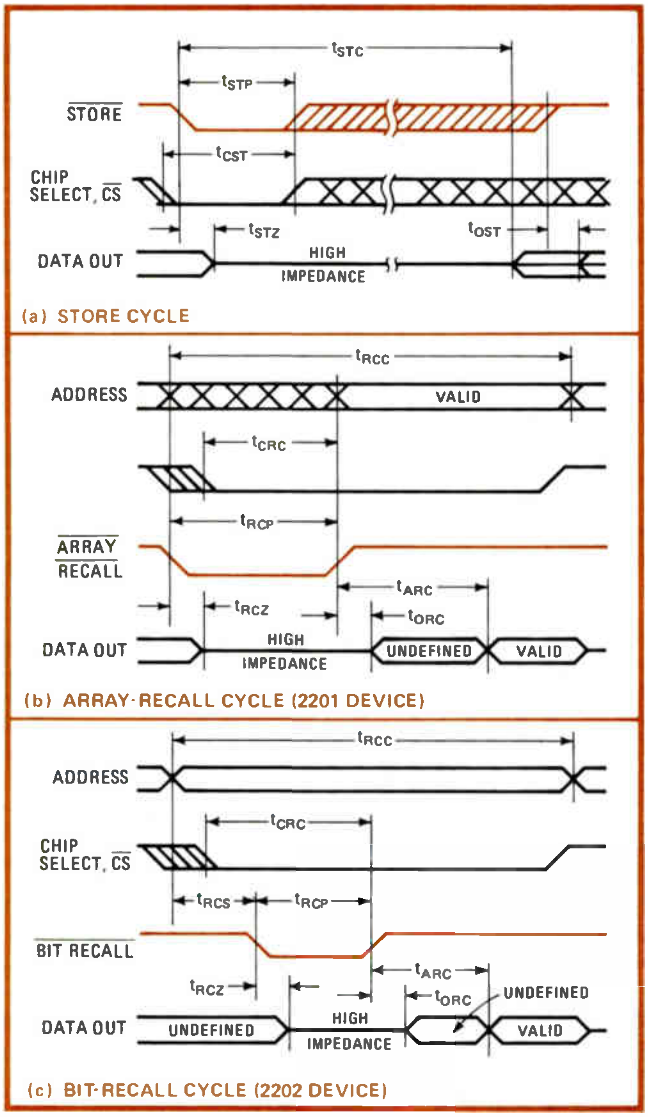
When either chip is operating as a standard static RAM, the high impedance load of capacitor C has no effect and the data can be read or written into the cells as in any static RAM. When data is required from the nonvolatile memory, however, it is detected by the floating gate. The floating element, programmed and erased as described above, always stores the nonvolatile data regardless of static RAM contents. Data stored on the floating gate is of course valid with or without power, and this data is recalled from the nonvolatile memory by switching the internal power supply line from ground to +5 V. During this switching, the cells are deselected; in terms of Fig. 4, the word-select lines isolating nodes N_1 and N_2 from the bit lines are turned off.

Now if the floating-gate transistor is on, N_2 will have a larger capacitance than N_1. This causes N_2 to rise more slowly than N_1, and the cell will latch with N_2 low and N_1 high. Similarly, if the floating-gate transistor is turned off, the capacitive load on N_1 will be larger than that on N_2. As the internal +5-V supply switches from ground to +5 V, node N_2 will rise more quickly than N_1 and N_2 will latch high with N_1 low.

Nonvolatile memory data remains separate from the contents of the RAM and depends only on the condition of the preprogrammed floating-gate electrode.

The cell structure described means that each array location actually comprises a normal static-RAM bit and an overlaid electrically erasable nonvolatile bit. More specifically, the Xicor 2201 and 2202 devices contain a total of 2,048 bits. (Timing diagrams for their purely static RAM operation are shown in Fig. 5.) Data is moved between the RAM and EE-PROM positions under the control of two TTL signals (Fig. 6). Any time a store signal is applied, a 1,024-bit snapshot of the RAM is copied into the EE-PROM, for later recall or modification in accordance with the timing diagrams that are shown in Fig. 7a. After being written into the EE-PROM, the RAM data remains available for routine RAM operation. But any time a TTL recall signal is applied, the EE-PROM data is copied back into the RAM.

The 2201's array-recall signal (Fig. 7b) brings all the EE-PROM data back into RAM in less than 1 microsecond. The 2202's bit-recall signal restores just a single bit at a



7. Shadow timing. Storage-function timing is shown in (a), the 2201's array-recall timing in (b), and the 2202's bit-recall timing in (c). To make RAM data nonvolatile, only one pin is signaled after the device is slated. The same is true of bringing data back into the RAM.

time. With this bit recall, it is possible to partition the 2202 chip into areas of ROM and RAM, for use as two different memory types. And through address selection, the ratio of ROM and RAM can be altered.

The nonvolatile store function is analogous to a standard RAM write cycle but typically requires a few milliseconds to complete. However, a store cycle requires no attention from the user once it is initiated, for it will automatically continue until completed. Similarly, the 2201's array recall and the 2202's bit recall operations resemble standard RAM read cycles, and these are completed in less than 1 microsecond.

Automatic recall

Another unique feature of the 2201 and 2202 devices is an automatic array recall when power is applied. This means that the RAMs of both devices power up with a copy of the nonvolatile EE-PROM data and it is ready for immediate use. No user signals are required during the

TABLE 2: STORE AND RECALL OPERATIONS

Symbol	Parameter
Store (both devices)	
t_{STC}	store cycle time[1]
t_{STP}	store pulse width[2]
t_{CST}	chip select to end of store
t_{STZ}	store to output in high Z
t_{OST}	output active from end of store
Array recall (X2201)	
t_{RCC}	array recall cycle time[3]
t_{CRC}	chip select to end of recall
t_{RCP}	recall pulse width[4]
t_{RCZ}	recall to output in high Z
t_{ORC}	output active from end of recall
t_{ARC}	recalled data access time from end of recall
Bit recall (X2202)	
t_{RCC}	bit recall cycle time[3]
t_{CRC}	chip select to end of recall
t_{RCS}	address to recall setup time
t_{RCP}	recall pulse width[4]
t_{RCZ}	recall to output in high Z
t_{ORC}	output active from end of recall
t_{ARC}	recalled data access time from end of recall[4]

1. 2 ms typical
2. 150 ns maximum
3. 1 μs maximum
4. 500 ns maximum

automatic array recall other than application of +5 V. In addition, there is no need to specifically shape or control the rising edge of the power supply.

The organization and ease of use of the 2201 and 2202 point to widespread usage—especially in microcomputer-based systems. The nonvolatile RAM can replace many existing products as it is both a static RAM and an EE-PROM. For the system designer, products are now available with nonvolatile memory that can be modified in the circuit via simple software commands. The devices, 18-pin dual in-line packages, have the modularity appropriate for small systems where maintaining minimum overhead is critical.

A nonvolatile bootstrap program can be kept in the EE-PROM shadow memory while an independent program is accessed from the RAM. At any time, data may be transferred back and forth between the RAM and the nonvolatile shadow through simple store and recall signals. This capability has many interesting possibilities, such as firmware changes that are directly loaded under software control. □

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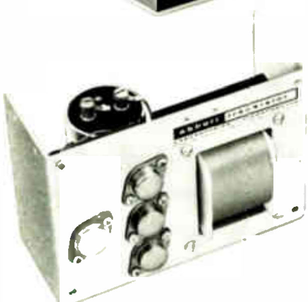

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16-bit 68000 microprocessor camps on 32-bit frontier

Symmetrical architecture, a large register set, and hard-working instructions relieve software bottleneck

by Brad Hartman, *Motorola Inc., Austin, Texas*

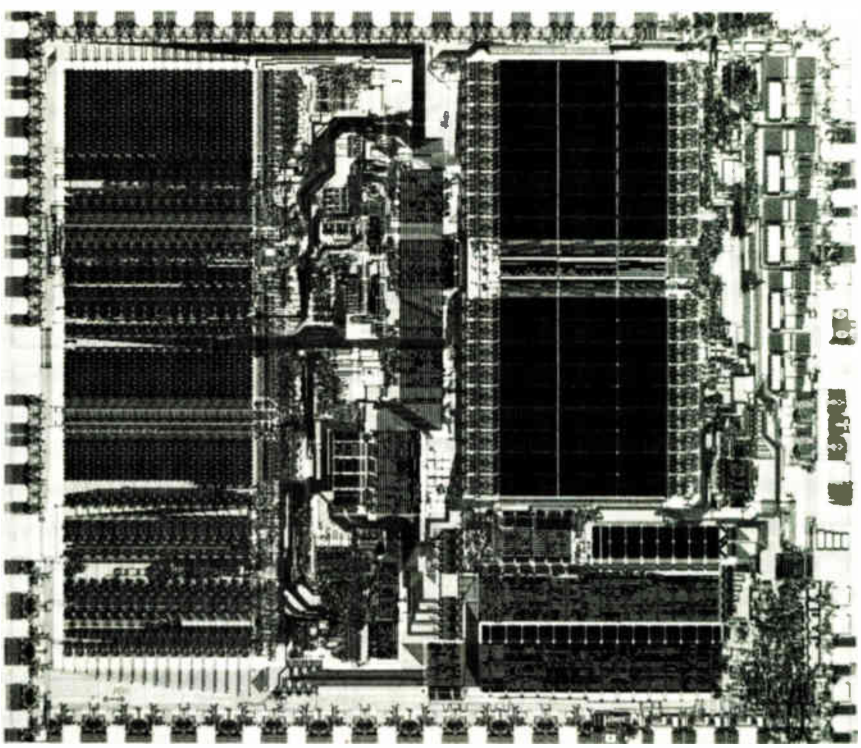
☐ With the MC68000, many architectural concepts proven in minicomputers have been cast in silicon for the first time. This thoroughly modern microprocessor packs in features left out of earlier designs in a compromise between being sooner and being better.

Really a 32-bit microprocessor disguised as a 16-bit machine because of current packaging limitations, the 68000 features a multilevel-microprogrammed controller, parallel-pipelined operations with prefetching, and nonmultiplexed asychronous buses. Its highly regular architecture and instruction set support high-level languages and rapid program repair. Its extensive ability to process exception conditions allows the programmer to deal with unusual hardware and software problems in a neat and consistent manner. This ability and a supervisor state provide a high degree of error protection.

Of all the considerations given to the design of the 68000, performance took top priority. The objective was to develop a microprocessor with performance better than that of the 8-bit 6800 by an order of magnitude. That goal was reached. When a choice had to be made between performance and some other factor, for the most part performance won out. For instance, multiplexing the address and data buses would have resulted in a smaller package, but that would also have reduced performance by as much as 30%, so the buses were not multiplexed.

The second most important consideration given to the 68000 was consistency, in respect to hardware and software alike. Consistency, or orthogonality, not only makes the machine more flexible and powerful, but easier to use as well. All data registers function identically, for example, as do all address registers, and all data and address registers may serve as index registers.

The 68000's instruction set consists of a relatively small number of general-purpose instruction types. Most instructions operate on bytes, 16-bit words, and 32-bit long words, the data size being specified in the mnemonic. Consequently, consistency in operations on different data sizes is maintained. Consistency in the



1. 68,000. On a 246-by-281-mil die, 68,000 transistors or 13,000 gates are fabricated using a minimum feature of 3.2 micrometers. Over half of the devices are used in read-only memory and programmable-logic-array structures. The chip typically dissipates 1.2 watts with an 8-megahertz clock.

setting of condition codes is also found in the 68000. Those instructions that are special cases of more general instructions set the condition codes in the same manner. For example, executing a TST instruction (which subtracts zero from an operand) affects the condition codes in exactly the same way as a SUB #0 instruction.

Emphasis was also placed on the support of high-level languages. Special attention was focused on frequently encountered operations that normally require several lines of code. Several such operations were implemented in the 68000 as single instructions, thereby increasing compiler efficiency and decreasing memory requirements at the same time.

The 68000 is intended to serve as a base for broad future growth and expansion. Future implementations of the device will take advantage of its unused microcode (approximately 20%) to add floating-point and string operations and to expand the trap structure. Extending the address space to cover over 4 billion bytes will be easily accomplished by taking full advantage of the 32-bit internal program counter, currently truncated to 24 bits. In addition, support products such as development systems are designed to accommodate a 32-bit microprocessor, a possible future version of the 68000 (see "The 68000: a future of support," p. 124).

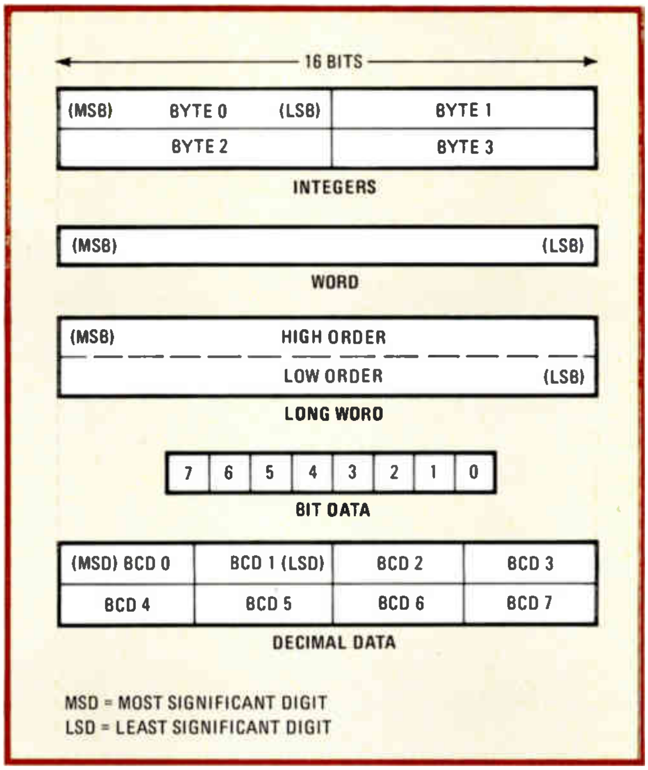
User and supervisor modes

The 68000 operates in two different modes of privilege: a user state for normal functions, and a supervisor state for the execution of privileged instructions. The instructions available in the user state are a subset of those available in the supervisory state. This concept allows operating-system control over critical functions such as memory management and software-initiated resetting, as well as in other situations where the user may cause blunders that might otherwise prove catastrophic. The supervisor state is entered during all trap, interrupt, and reset operations.

Data types associated with the 68000 include integers, bits, and binary-coded-decimal (BCD) digits (see Fig. 2). Integer data may be represented in byte, word, or long-word form. Byte data may be addressed on even- or odd-address boundaries, whereas word and long-word data is addressed only on even-address boundaries. Bit data is represented as a specific bit in a byte. To address a single bit, the byte location and bit number (0–7) are given. Special instructions are available to operate on BCD digits, which reside two to a byte.

A look into the register file of the 68000 (Fig. 3) reveals eight 32-bit data registers, nine 32-bit address/stack registers, a program counter, and a status register. The address registers may function as stack pointers using the predecrement and postincrement addressing modes, and all data and address registers may be used as index registers.

The stack pointers A7 and A7′ are used in the user and supervisory states, respectively. Interrupts, traps, subroutine calls, and so on use these stacks to save the machine's status (normally the contents of the program counter and status register). The 32-bit program counter supports 32-bit calculations, with its lower 24 bits used in conjunction with the address bus.



2. Data types. Data types associated with the 68000 include integers, words, 32-bit long words, individual bits, and decimal numbers. Integers may be represented as bytes, words, or long words; binary-coded-decimal data is packed two digits to a byte.

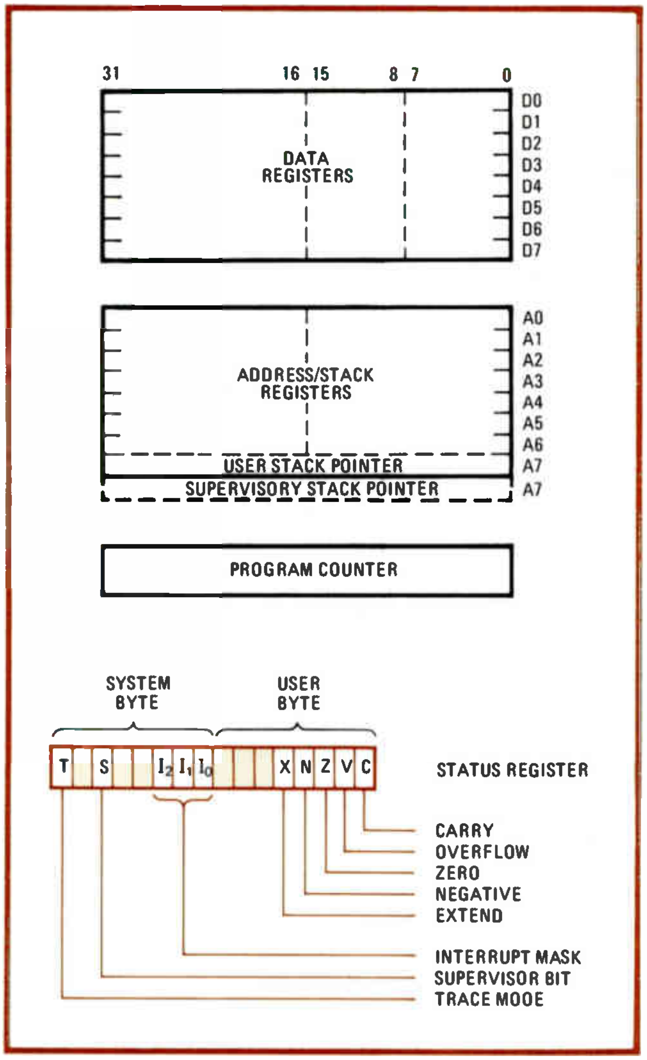
The status register consists of a user byte and a supervisor byte, as shown in Fig. 2. The entire status register may be read in both the user and supervisory states. Writing into the user byte is allowed in the user state, but writing into the entire register may occur only while in the supervisory state.

The user byte contains the condition codes C, V, Z, N, and X. Carry (C) is set if a carry or borrow is generated from an addition or subtraction. Overflow (V) is set in the event of an arithmetic overflow. Zero (Z) is set if a result equals zero and the negative bit (N) is set if the result is negative. Extend (X) is used in extended precision arithmetic and is set in the same manner as the carry bit.

The system byte contains an interrupt mask, the supervisor bit, and a trace bit. The interrupt mask, bits I_0, I_1, and I_2, holds the current interrupt-priority level. The supervisor bit (S) determines which state the processor is operating in. The trace bit (T), if set, invokes a trap to the 68000's trace routine after execution of each instruction. The machine returns to normal processing after the trace bit is cleared. The trace mode is a powerful tool that may be used to assist the programmer in a step-by-step debugging process.

Exception processing

Exception processing in the 68000 is much more complex than that in typical 8-bit microprocessors. Exceptions to be processed may be initiated externally or internally. External exceptions include interrupts and bus errors; internal exceptions result from illegal condi-



3. Register file. The 68000 has eight registers for data, seven for addresses, two stack pointers, a program counter, and a 2-byte status register. The device has user and supervisory states, with a stack pointer and status byte provided for each state of privilege.

tions and instruction-generated traps.

Exception processing begins with the 68000 entering the supervisor state. Next, the associated vector number is determined, through an external fetch in the case of a vectored interrupt and internally in all other cases. Then the current status of the processor is saved on the supervisor stack. Finally, the program counter value is fetched from the exception vector and processing of the exception routine proceeds.

The exception vectors begin at memory location 0 and extend to location 1,023, each vector being 4 bytes long (see Table 1). Of the 256 possible exception vectors, the upper 192 are reserved for vectored interrupts and the lower 64 are dedicated to traps and nonvectored interrupts. Vectored interrupts, however, may select one of the lower 64 vectors.

Interrupts are given a priority and may be vectored or nonvectored. Priorities range from level 0 (no interrupt) up to level 7 (highest priority, nonmaskable). An interrupt request is acknowledged if the incoming priority level is greater than the current level of processor priority. The only exception to this is level 7, which will acknowledge another level 7 interrupt request.

Vectored interrupt processing begins with completion of the current instruction. At this point the processor compares the incoming interrupt request priority level with the interrupt mask in the status register. If the incoming level is of sufficient priority, then the interrupt sequence is processed; otherwise the new request is postponed. Assuming that the existing sequence continues, the processor fetches a vector number (0–255) from the least significant byte of the data bus. This vector number selects the priority of the next exception routine.

Many existing peripheral devices are incapable of supplying a vector number during an interrupt sequence, so provisions have been made to allow for nonvectored interrupts. When the 68000's valid peripheral address (VPA) pin is asserted during an interrupt-acknowledge cycle, the 68000 does not fetch a vector number from the data bus. Rather, it looks at the priority level and fetches the appropriate auto vector. For instance, if the interrupt is of level 4, then the level 4 auto vector becomes the selected exception vector number. Exception processing then continues in the usual manner.

Traps are handled like interrupts except that all vector numbers are furnished internally. Special traps such as those generated by an address error and division by zero are initiated automatically, whereas software traps may occur only after execution of the appropriate instructions. In either case, the vector number is supplied by the processor and exception processing follows.

Two exception vectors (10 and 11) are dedicated to the emulation of future instructions. Any instruction with 1010 or 1111 in its 4 most significant bits will automatically trap the line 1010 or line 1111 emulation traps, respectively (see Table 1 again). Later versions of the 68000 will include instructions beginning with these bit patterns and will be executed in hardware rather than through trapping routines via these vectors.

Asynchronous buses

The nonmultiplexed data and address buses allow efficient operation without the need for external latches. These lines are capable of being put in the high-impedance state for external control. The 16-bit data bus allows transfers of bytes, words, and long words.

Although there are 23 address lines on the 68000, as mentioned previously, 24 bits are actually used by the program counter. The 23 address lines select a word address; the upper data strobe (UDS) and lower data strobe (LDS) select the upper and lower bytes of the word. Therefore, for byte operations, either UDS or LDS is asserted, whereas both are asserted for a word operation. These two lines are also normally included in the chip-select equations of memory and peripherals, as input and output in the 68000 is memory-mapped.

The asynchronous buses of the 68000 match the processor's speed to the speed of memory and peripheral devices. That is, the processor slows down for devices having long access times and speeds up for faster components. This is accomplished via asynchronous bus-control lines. This asynchronous handshaking begins with the processor lowering the address strobe, AS, which indicates that the address bus is stable. The external device being addressed must lower DTACK (data transfer acknowledge) when ready to transfer data. The time between AS and DTACK normally corresponds to the access time of the device being addressed.

Bus-arbitration lines allow an external device to control the 68000's buses. External control is initiated by the external device signaling the 68000's bus-request line, BR. The processor issues BG (bus grant) when its buses are available. The external device asserts BGACK (bus grant acknowledge) to indicate that it has possession of the bus, and then brings BR high. Finally, the processor negates BG and waits for BGACK to be negated. BGACK is negated when the external device has finished, and normal processor operation resumes.

Interrupt hierarchy

Interrupts are requested via the IPL0, IPL1, and IPL2 lines. These three interrupt lines are continually monitored for changes. For instance, if the processor is currently processing a level 6 interrupt and a level 2 interrupt request appears, the processor will ignore the request until the level 6 interrupt is completed. Afterward, if the level 2 interrupt is still present on IPL0–IPL2, then the processor will honor that request. However, if the processor was operating on a level 4 interrupt at the time the level 6 interrupt was honored, then the processor will ignore the level 2 request, complete the level 4 interrupt, and finally honor the level 2 request if it is still present on IPL0–IPL2.

When an interrupt request is honored, the processor enters its supervisory state, machine status is saved on the supervisory stack, the interrupt mask in the status register is changed to the new level, and the processor signals an interrupt acknowledgement via its function-code lines. At this time either vectored or nonvectored interrupt processing takes place. The interrupt sequence terminates with a RTR (return-and-restore) or RTE (return-from-exception) instruction.

System control is accomplished with the BERR, RESET, and HALT signal lines. BERR (bus error) is an input that, when zero, signals the processor that an error has occurred on the bus and a trap to the bus-error routine is in order. Typical applications include hang-ups on the asynchronous bus (such as a loss of handshaking), an illegal memory access used in conjunction with external memory management, or a device that does not respond during a vectored interrupt sequence.

RESET is a bidirectional signal used for both externally and internally initiated resets. External resets require a low-going signal on both the RESET and HALT lines. This signal resets all devices tied to RESET and begins an internal reset sequence. The processor goes into the supervisory state, the value of the supervisor stack pointer is loaded from vector 0, the program counter for the reset routine is loaded from vector 1, and processing of the reset routine begins. For an internally initiated reset, the 68000 executes the RESET instruction described above. This drives the RESET pin low for approximately 124 clock pulses, but does not reset the 68000 itself.

HALT is another bidirectional signal line. When brought low externally, the processor suspends execution

TABLE 1: EXCEPTION VECTORS

WORD ADDRESS		NUMBER
1023	192 USER INTERRUPT VECTORS	255 … 64
256	UNASSIGNED RESERVED	63 … 48
192	16 TRAP INSTRUCTION VECTORS	47 … 32
128	LEVEL 7 AUTOVECTOR INTERRUPT	31
124	6	30
	5	29
	4	28
	3	27
	2	26
100	LEVEL 1 AUTOVECTOR INTERRUPT	25
96	SPURIOUS INTERRUPT	24
94 … 48	UNASSIGNED, RESERVED	23 … 12
44	LINE 1111 EMULATOR	11
	LINE 1010 EMULATOR	10
	TRACE	9
	PRIVILEGE VIOLATION	8
	TRAPV INSTRUCTION	7
	CHECK INSTRUCTION	6
	ZERO DIVIDE	5
16	ILLEGAL INSTRUCTION	4
12	ADDRESS ERROR	3
8	BUS ERROR	2
0	RESET	0

after completion of the current bus cycle and will remain in this state until the line is returned high. There is no maximum time limit on the duration of a halt because refreshing inside the machine continues. The majority of the bus lines are in a high-impedance state during the halt operation. Manipulation of the HALT line can be used for stepping a program cycle by cycle for debugging purposes.

If the processor encounters a double bus fault (two bus errors within a certain time period) or a double address error, then the processor will halt. The processor signals this to the outside world by lowering the HALT line. Only an external reset can get the processor to leave this state.

Upward compatible

Compatibility with existing 8-bit M6800-family peripheral devices is accomplished with the VPA, VMA, and E lines. These are synchronous peripheral devices and the MC68000 must be synchronized with them. Asserting VPA (valid peripheral address) when access to a 6800-family peripheral is desired changes the operation of the 68000 from asynchronous to synchronous, with no DTACK required. It also generates the VMA signal required by the peripherals. The required enable signal, E, is a free-running signal with a period equal to 10

TABLE 2: FUNCTION CODE LINES

Function code output			Reference class
FC_2	FC_1	FC_0	
0	0	0	(unassigned)
0	0	1	user data
0	1	0	user program
0	1	1	(unassigned)
1	0	0	(unassigned)
1	0	1	supervisor data
1	1	0	supervisor program
1	1	1	interrupt acknowledge

68000 clock cycles. Its operation is never altered, even during a reset operation.

The function-code signal pins FC0, FC1, and FC2 can be considered an extension of the 68000's address bus (see Table 2). These tell the outside world whether user data, user program, supervisor data, or supervisor program is being addressed. Thus these lines may be externally decoded and employed to extend the address space of the 68000 to four 16-megabyte segments for a total of 64 megabytes. Three combinations of these lines are reserved for future use.

The function code lines may also be used by external devices to ensure that certain operations are done in the correct state. For instance, an external memory-management device may require that its control registers be addressed only when the 68000 is in its supervisory state. FC2 can be used to determine which state the processor is operating in, and the memory management device can generate a bus-error signal if necessary.

The system clock of the 68000 is a TTL-compatible signal that is internally buffered and requires a square wave with a 50% duty cycle. The remaining pins on the 68000 are +5 volts and ground. There are 2 pins for each, bringing the total pin count to 64.

Addressing modes

There are 14 addressing modes available to the 68000. As Table 3 shows, they fall into six basic groups: register direct, immediate, relative, absolute, implied, and register indirect.

The most flexible of the addressing modes in the 68000 is register indirect, wherein the contents of an address register points to the operand. Address register indirect with postincrement automatically adds 1, 2, or 4 to the address register after the register is used. Similarly, address register indirect with predecrement automatically subtracts 1, 2, or 4 from the address register before it is used.

The 1, 2, and 4 refer to the data size specified in the instruction. Thus, a byte operation using the postincrement or predecrement modes either adds or subtracts 1 from the address register, and a long-word operation would add or subtract 4 from the address register. These two addressing modes may be employed to maintain user stacks and queues.

Indexes and offsets can also be used with register indirect addressing. Address register indirect with displacement adds a 16-bit signed integer to the contents of an address register, then uses this value to point to the operand. Address register indirect with index and offset adds the contents of an index register, an address register, and an 8-bit signed integer and then uses the result to point to the operand.

Instructions set the pace

The rich instruction set of the 68000, coupled with the 14 powerful addressing modes, sets a new standard of software performance in the microprocessor industry. The 56 instruction types are general-purpose and powerful at the same time. The set may be broken down into eight groups for data movement, shift and rotate, bit manipulation, logic, BCD operations, binary arithmetic, program control, and high-level language support. Additional instructions, variations of these 56 types, appear in Table 4.

Register-to-register, register-to-memory, memory-to-register, and memory-to-memory data transfers by byte, word, and long word are all accomplished with one single instruction, MOVE. MOVEM (move multiple registers) moves any of the data and address registers to memory or vice versa with a single instruction. The DBcc instruction (test condition, decrement, and branch) allows repetitive loops with long backward and forward branches, again, with one instruction.

Data movement is normally accomplished with the MOVE instruction. However, the exchange of any two data or address registers is made possible with EXG (exchange registers), and swapping the lower half of a data register with the upper half is accomplished with the SWAP instruction.

Bit-manipulation instructions allow operations on a single bit of data, either in memory or in a data register. These instructions test the bit and effect the appropriate condition codes. In addition, bits may be changed, set, cleared, or left unaffected.

BCD instructions utilize the extend bit in the status register. Extended-precision addition, subtraction, and negation are made possible with these instructions, without additional decimal-adjustment instructions.

Program control instructions allow for conditional and unconditional transfer of control, as well as privileged operations. Branch instructions and branch-to-subroutine instructions offer 8- and 16-bit signed displacements to allow a wide addressing range for position-independent programs. The JMP (jump) and JSR (jump-to-subroutine) instructions transfer control to an effective address located anywhere in the memory map. Return instructions include RTS (return from subroutine), RTR (return and restore), and RTE (return from exception). These instructions restore the program counter, the program counter and condition code register, and the program counter and status register, respectively.

TRAP and TRAPV are software-initiated traps. TRAP allows exception processing to take place at one of 16 trap routines specified in the TRAP instruction. These

TABLE 3: ADDRESSING MODES

Mode	Generation
Register direct addressing	
data register direct	EA = Dn
address register direct	EA = An
Absolute data addressing	
absolute short	EA = (Next Word)
absolute long	EA = (Next Two Words)
Program-counter-relative addressing	
relative with offset	EA = (PC) + d_{16}
relative with index and offset	EA = (PC) + (Xn) + d_8
Register indirect addressing	
register indirect	EA = (An)
postincrement register indirect	EA = (An), An ← An + N
predecrement register indirect	An ← An − N, EA = (An)
register indirect with offset	EA = (An) + d_{16}
indexed register indirect with offset	EA = (An) + (Xn) + d_8
Immediate data addressing	
immediate	DATA = Next Word(s)
quick immediate	Inherent Data
Implied addressing	
implied register	EA = SR, USP, SP, PC

Notes: EA = effective address; An = address register; Dn = data register; Xn = address or data register used as index register; SR = status register; PC = program counter; d_8 = 8-bit offset (displacement); d_{16} = 16-bit offset (displacement); N = 1 for byte, 2 for words and 4 for long words; ( ) = contents of; ← = replaces

can be viewed as 16 unique software interrupts. TRAPV (trap on overflow) tests the overflow bit in the status register and traps to the TRAPV routine if the bit is set; otherwise, normal processing continues.

The STOP instruction halts the processing of instructions and resumes execution upon an interrupt request of sufficient priority or an external reset. Attempted execution of STOP or RESET, which are privileged instructions, results in a trap to the privilege violation trap if the processor is operating in the user state.

Shift-and-rotate instructions operate on bytes, words, and long words. The shift-and-rotate counts may be specified statically in the instruction (1 to 8 bits) or dynamically in a data register (up to 64 bits). The carry and extend bits in the condition-code register are treated differently during rotation operations to preserve the carry bit.

The logical instructions AND, EOR, NOR, and OR yield standard Boolean operations. Byte, word, and long-word operands are valid here as with most 68000 instructions.

Instructions for binary integer arithmetic include those for addition, subtraction, negation, multiplication, and division. Addition, subtraction, and negation may include the extend bit at the programmer's discretion to allow extended-precision arithmetic. Multiplication and division may be signed or unsigned.

CLR (clear operand) places zeros in the appropriate byte, word, or long word. EXT (sign extend) converts a byte to a word or a word to a long word. This is useful, since arithmetic and logic operations often require their operands to be of equal size. TST (test operand) subtracts

TABLE 4: INSTRUCTION SET VARIATIONS

Mnemonic	Variations	Description
ADD	ADD	Add
	ADDA	Add address
	ADDQ	Add quick
	ADDI	Add immediate
	ADDX	Add with extend
AND	AND	Logical AND
	ANDI	AND immediate
CMP	CMP	Compare
	CMPA	Compare address
	CMPM	Compare memory
	CMPI	Compare immediate
EOR	EOR	Exclusive OR
	EORI	Exclusive OR immediate
MOVE	MOVE	Move
	MOVEA	Move address
	MOVEQ	Move quick
	MOVE from SR	Move from status register
	MOVE to SR	Move to status register
	MOVE to CC	Move to condition codes
	MOVE to USP	Move to user stack pointer
NEG	NEG	Negate
	NEGX	Negate with extend
OR	OR	Logical OR
	ORI	OR immediate
SUB	SUB	Subtract
	SUBA	Subtract address
	SUBI	Subtract immediate
	SUBQ	Subtract quick
	SUBX	Subtract with extend

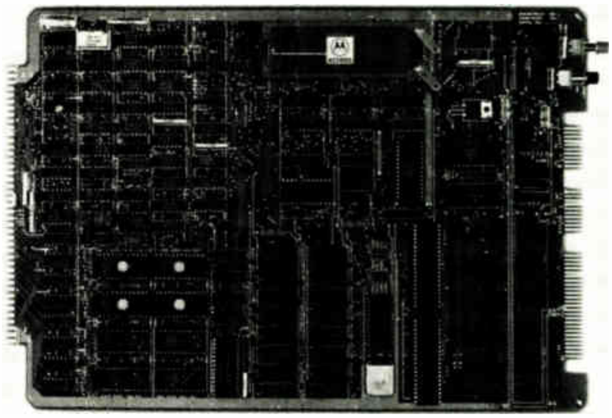
The 68000: a future of support

Motorola shipped its hundredth MC68000 sample in August and now sells small quantities for $249 apiece. It hopes to reach volume production in early 1980.

For second sources, Rockwell International Corp. has been lined up in the U. S., Hitachi Ltd. in Japan, and in Europe, the Société pour l'Etude de la Fabrication de Circuits Intégrés Spéciaux, a company jointly owned by Thompson-CSF and France's atomic energy agency.

Motorola plans four support devices for the 68000 family, including a peripheral controller, a memory-management unit, a bus-arbiter module, and a direct-memory-access controller. The last device, which Hitachi is building, may be out early next year. Rockwell has agreed to build the bus arbiter and bubble-memory support chips; in return Motorola will second-source Rockwell's 256-kilobit and upcoming 1-megabit bubble memories.

A design module, the MEX68KDM, is now available for evaluating the 68000, at a price of $1,795 (see photo). It has 32 kilobytes of random-access memory, four data ports, three timers, and an 8-kilobyte read-only memory containing debugging routines called MACSbug. The EXORmacs development system will be introduced next year with a new 260-line bus structure to support 32-bit data and an operating system for at least eight users; it will support high-level languages and will eventually be fitted with hard-disk storage. **-John G. Posa**



zero from an operand and affects the condition codes appropriately without altering the operand.

The high-level language support instructions were included in the 68000 instruction repertoire with the intent of reducing compiler overhead in frequently encountered commands. Parameter passing, boundary checking, repetitive looping, and efficient context switching are made easier with these specialized instructions.

High-level language support

LINK and UNLK allow for the allocation and deallocation, respectively, of local variable storage for procedure calls. LINK uses an address register as a frame pointer to mark the beginning of local variable storage on the stack (see Fig. 4). The stack space for local variables is automatically reserved through incrementing the stack pointer by the number of bytes used for local storage. Access to the local variables is accomplished by using the frame pointer as a base register. Upon completion of the procedure, UNLK decrements the stack pointer to remove the local storage and then restores the previous frame pointer, to allow nesting of procedures.

Boundary checking can be accomplished using the CHK instruction (check register against bounds). Execution of CHK compares the contents of the data register with zero and an upper limit. If the register contents is less than zero or greater than the limit, a trap to the CHK routine is invoked.

Bounds testing is useful for maintaining arrays. The upper limit used in the CHK instruction could be set equal to the dimension of the array. The data register contains the element number of the array and the address register contains the starting address of the array. Prior to array access, the CHK instruction is executed to ensure that the array bounds have not been violated. If valid, then access to the array would be accomplished by using indirect addressing with index, where the starting address added with the index would point to the memory location of the array element. If not valid, the CHK routine would generate an error message.

Often it is desirable to pass parameters from one procedure to another. This may be accomplished by simply pushing the parameter on the stack. Another technique involves pushing the address of the parameter on the stack. The 68000 allows effective address calculation with a PEA (push-effective-address) and LEA (load-effective-address) instruction. These instructions perform the address calculation automatically and place it either on the stack (PEA) or in an address register (LEA).

Another operation frequently encountered by compilers involves performing Boolean operations on integer values. For instance, let X, Y and Z be integers:

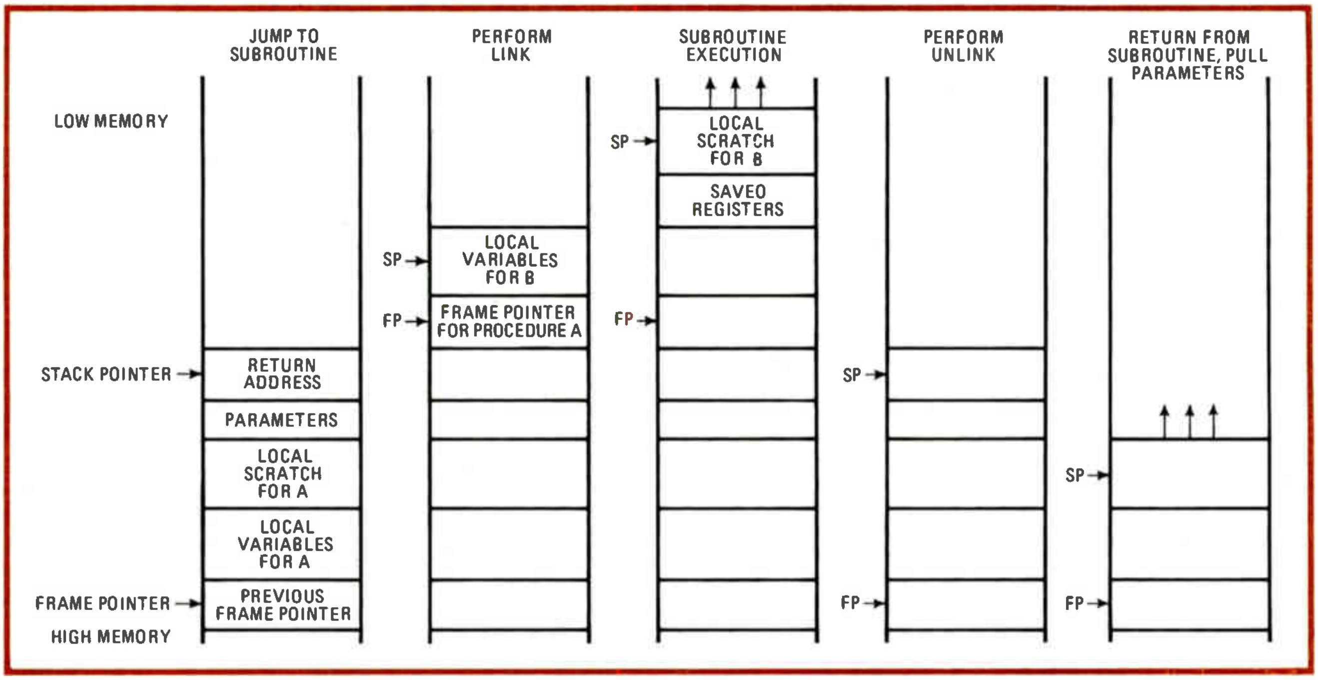
if $(X > Y)$ and $(Y \leq Z)$ then

This Pascal statement requires that each expression contained in parentheses be evaluated and converted to a Boolean variable. Then the Boolean AND function is applied to these variables. The compiled assembly code might look like this:

CMP X,Y	compare X and Y
SGT TEMP1	set memory location Temp1 to all ones if greater than; otherwise set to zero
CMP Y,Z	compare Y and Z
SLE TEMP2	set memory location Temp2 to all ones if less than or equal; otherwise set to zero
AND TEMP1, TEMP2	AND Temp1 and Temp2; Temp1 holds result

At this point the compiler knows the result of the IF statement and can proceed accordingly.

Multiprocessing often requires that two or more processors share a common memory. The TAS (test-and-set) instruction allows a processor to interrogate a



4. High-level assembly. Some assembly-language instructions for the 68000 do so much they could be termed higher-level instructions. The link-stack and unlink-stack commands, for example, allocate and deallocate, respectively, local storage for procedure calls.

test byte, set the condition codes accordingly, and then place a 1 in the most significant bit of the byte. If the memory is busy, the program can keep trying until it is free.

This is accomplished with the following routine:

LOOP	TAS TEST	test and set location TEST
	BNE LOOP	if not = 0, test again
		(body of loop)
	CLR TEST	clear TAS byte

It is important to note that TAS is an indivisible read-modify-write instruction that prohibits another processor from interfering with the TAS operation once it has been initiated.

Efficient looping

Repetitive looping is one of the most common techniques used in computer programming. The test condition, decrement, and branch instruction (DBcc) allows efficient looping with a variety of features.

The process begins by initializing a data register with the number of loop iterations. The body of the loop follows, with the DBcc instruction appearing at the end of the loop. Specified in the instruction is one of 16 conditions and the data register that holds the count. When DBcc is encountered, the processor tests to see if the condition is true, decrements the data register, and also checks to see if the specified data register equals −1. If neither of these criteria is met, the processor branches backward or forward up to 32 kilobytes. If one or both are true, however, looping is terminated and normal processing continues.

Consider the following code segment:

MOVE	D1, #50	initialize loop count
LOOP	(first statement)	beginning of loop
		(body of loop)
DBLE	D1, LOOP	end of loop

The loop count is equal to 50 and resides in data register D1. Upon completion of the loop, the condition-code register is checked for the less-than-or-equal-to condition. If true, the loop is terminated; if false, D1 is decremented. If D1 equals zero, the loop is terminated. If not, the processor branches back to the label LOOP and executes the loop's body again.

Since the 68000 has so many data and address registers, saving them all during exceptions or subroutine calls could prove to be time-consuming, so register saving is left up to the programmer. This is easily facilitated with the MOVEM instruction. Any or all of the registers may be moved to a contiguous memory block with MOVEM, and contiguous memory may similarly be moved to selected registers. For instance:

MOVEM.L D1, D5, D6, A3, A4, SAVE

moves the contents of registers D1, D5, D6, A3, and A4 to the memory beginning at location SAVE. Likewise:

MOVEM.L SAVE, D1, D5, D6, A3, A4

restores the same registers with the data starting at location SAVE. Thus, only the critical registers need be saved, thereby maximizing context switching.

More help on the way

The 68000 will be supported by a full complement of development systems, micromodules, operating systems, and high-level language compilers, allowing total flexibility for both hardware and software designers. A typical configuration would include a 68000-based EXORmacs development system, hard-disk storage, a printer, and satellite systems for other microprocessors. These satellite stations would have access to the system resources of the EXORmacs via bus arbitration. This sharing of resources reduces system costs. □

Tunable equalizers set amplitude and delay

by P. V. Ananda Mohan
Indian Telephone Industries Ltd., Bangalore, India

Equalizing networks providing constant amplitude and/or delay over a wide range of frequencies are easily realized by utilizing the feed-forward and feed-back techniques of these tunable circuits. More specifically, a parallel-T arrangement of resistors and capacitors as shown in (a) makes it possible to select the equalizing delay with a single potentiometer. Equalization and selection of amplitude can be attained by adding a single operational amplifier stage of variable gain (b) to the basic circuit. If the parallel-T is made tunable (c), the equalizer's center frequency can be adjusted with very little difficulty.

The circuit that is illustrated in (a) is so configured that its transfer function is that of an all-pass network having a roll-off dependent on circuit Q, or:

$$\frac{e_{out}}{e_{in}} = \frac{s^2 - s(\omega_o/Q) + \omega^2}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

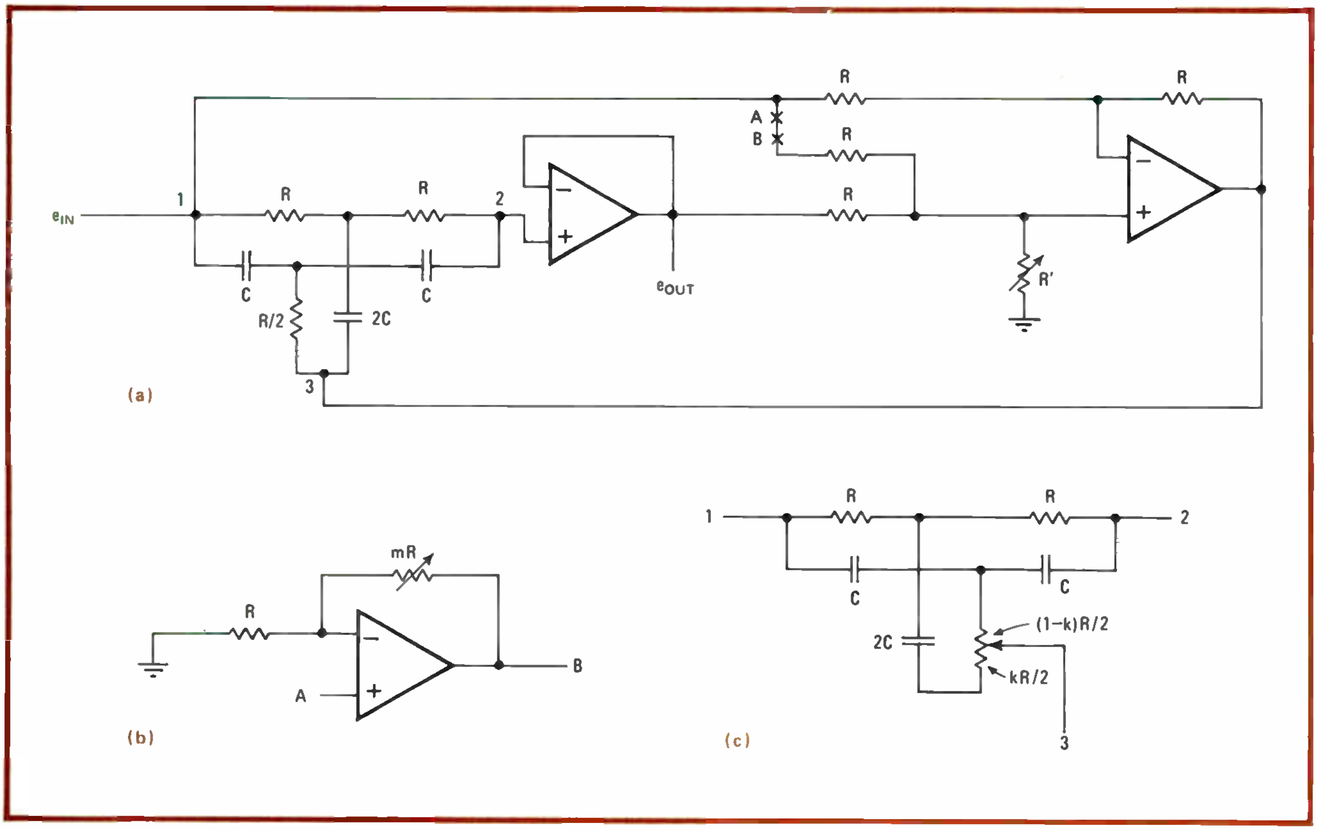
where $\omega_o = 1/RC$ and $Q = 1/4 + R'/2R$. The amount of delay is selected with potentiometer R′, as the amount of phase shift introduced by the RC network is:

$$\theta = t - 2\tan^{-1}[\omega\omega_o/Q(\omega_o^2 - \omega^2)]$$

where θ will vary little about ω_o, provided ω is sufficiently removed from ω_o.

If the op amp circuit (b) is placed between ports A and B in (a), the equalizer's gain at mid-frequency ω_o becomes $G = (2R'm)/R - 1$, and so the gain may be set by varying R′ and/or m. Note that the delay is still a function of R′ and that G will not vary significantly over a wide range of frequencies.

The center frequency of the equalizer may be adjusted if the parallel-T network shown in (c) replaces the network in (a) enclosed between points 1 and 3. In this case, $\omega_o = \omega/(1-K)^{1/2}$ and $Q = (1/4 + R/2R)/(1-K^2)^{1/2}$, where K is the fraction of the total resistance of P_2, as measured from its lower end. □



Selection. Parallel-T RC network simplifies design of tunable two-stage equalizer network. Delay is set with only a single control element, R′ (a). Amplitude equalization or adjustment in network's center frequency is attained by adding op amp (b) and tunable RC (c), respectively.

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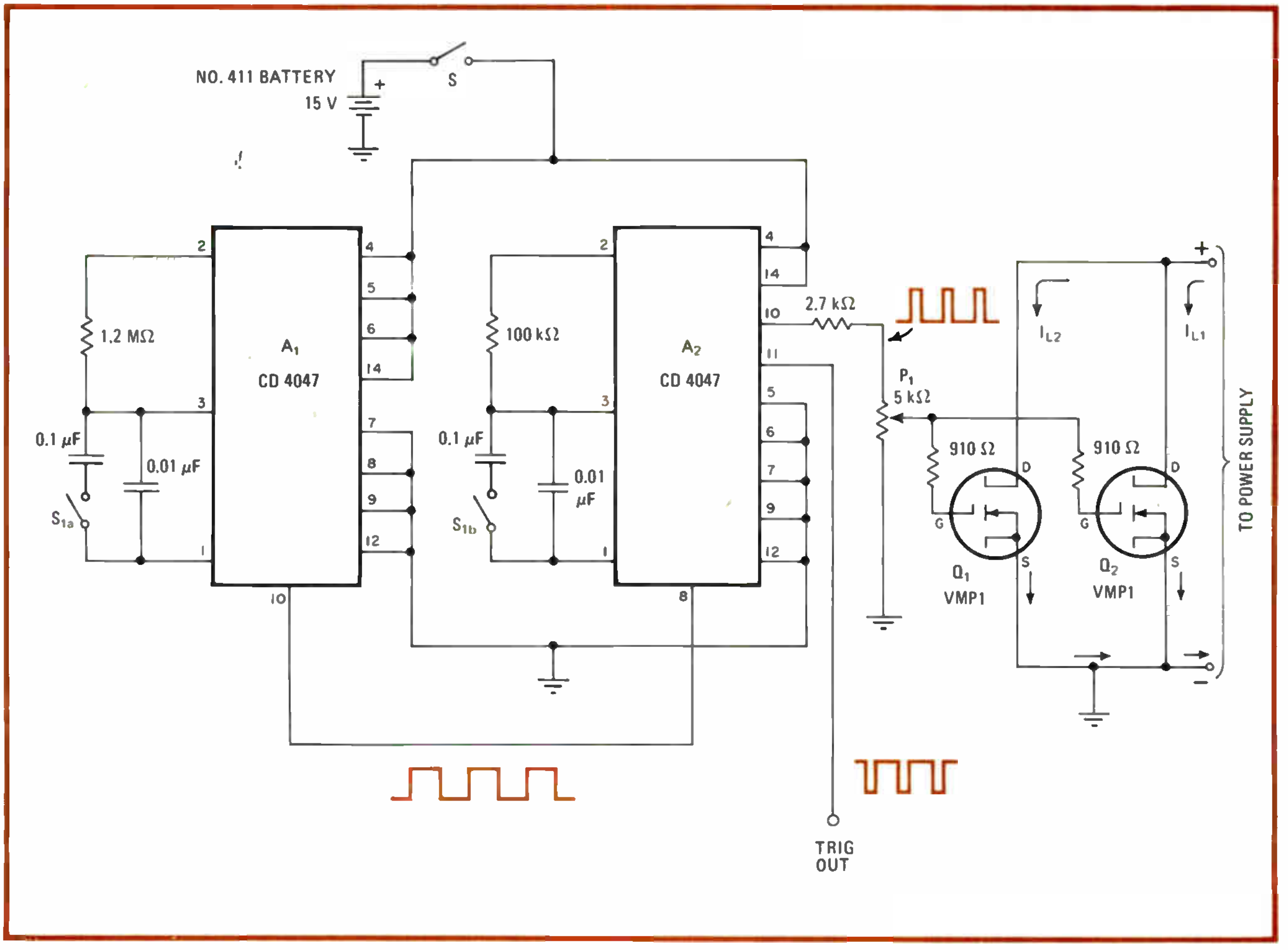
Switched load checks power supply response

by William M. Polivka
Department of Engineering, California Institute of Technology, Pasadena

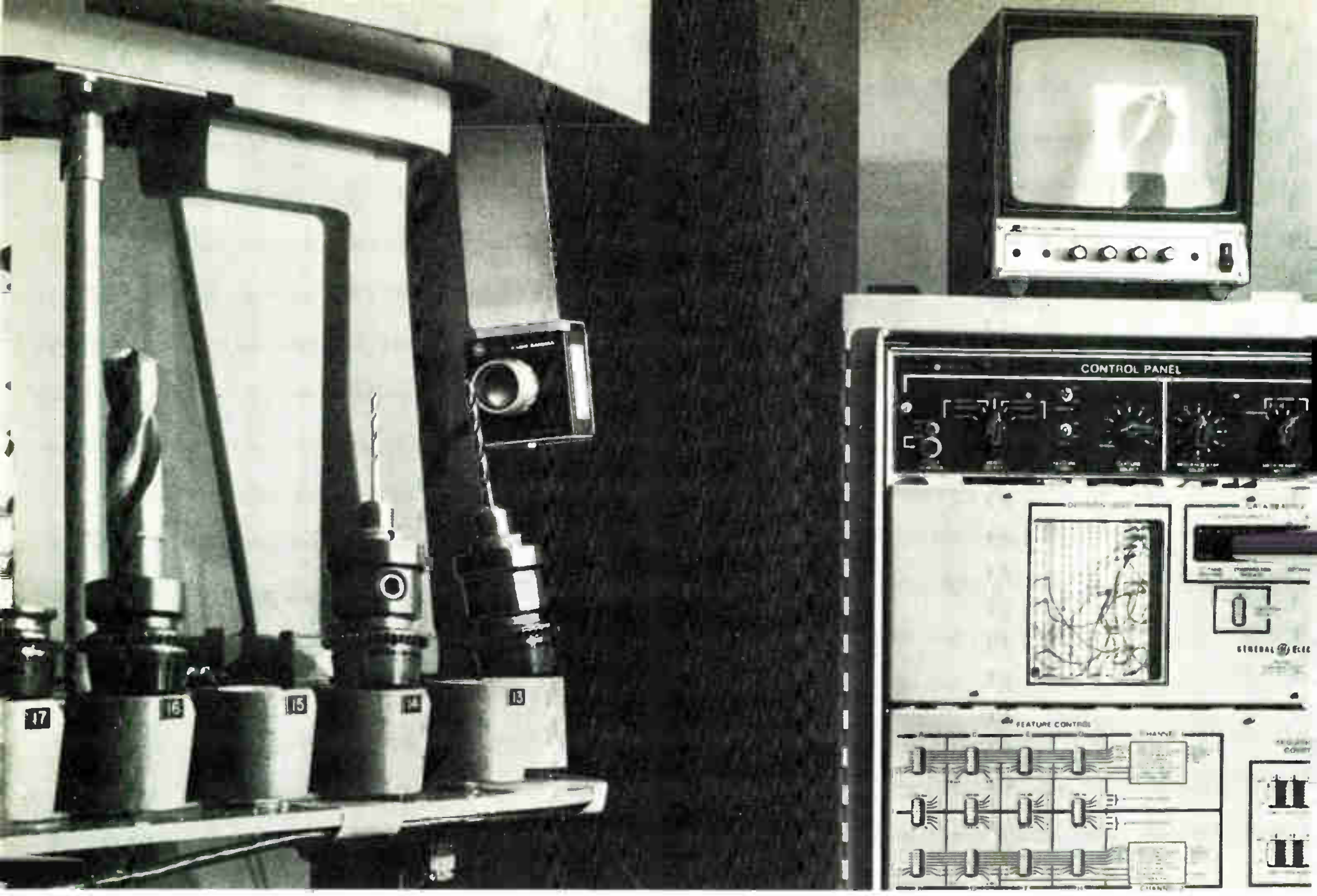
The transient response of a power supply is easily checked with the aid of this pulse loader, which periodically places a short circuit across the supply's output in order to simulate sudden load changes. Using complementary-MOS integrated circuits and V-groove MOS power transistors, the compact, self-contained unit runs on a battery, so that it presents no ground-loop problems to the supply under test.

As shown in the circuit for the pulsed load, astable multivibrator A_1 and one-shot A_2 set respectively the frequency and the width of the pulses that switch on load transistors Q_1 and Q_2. S_1 selects either of two combinations of frequency and width—in this case, 2 hertz at 25 milliseconds or 20 Hz at 2.5 ms. Note that a low duty cycle is required to reduce heat dissipation in Q_1 and Q_2. A trigger signal for driving an oscilloscope or other instrument to observe the supply's response appears at pin 11 of A_2.

Potentiometer P_1 sets the point at which Q_1 and Q_2 fire, so that the magnitude of the pulsed supply current passing through the load transistors can be selected from zero to the maximum capability of the V-MOS devices. Each field-effect transistor handles 2 amperes at 12 volts, values that derate to 400 milliamperes at 60 V. Moreover, an increase in supply loading may be attained simply by adding transistors in shunt at the output of the unit, as required. □



Load dynamics. Low-cost tester, with aid of scope, finds transient response of power supply by ordering periodic increase in supply current to simulate load changes. A_1 and A_2 set frequency and width of switching waveform. $Q_1 - Q_2$ sink current proportional to setting of P_1.



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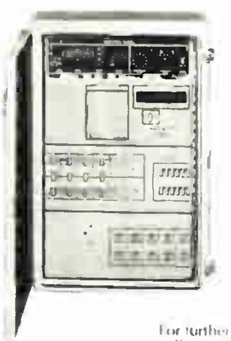

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Pseudorandom generator has programmable sequence length

by Ajit Pal
Indian Statistical Institute, Calcutta, India

Providing a pseudorandom binary sequence of order i in the range of 2 to 16, this generator will find many uses in fault-detection and speech-scrambling equipment. Any sequence having a maximum length of $2^{16}-1$ can be generated. If the sequence can be selected electronically, instead of mechanically by means of a manual-switching arrangement as shown, the unit will be extremely useful in automatic-test environments.

The pseudo-random sequence is produced with the aid of a 16-bit shift register and appropriate circuitry for providing a feedback signal to the register's first stage. A_1–A_4 are the 4-bit registers that comprise the 16-bit stage, wired to shift bits from left to right on every system clock. A_5–A_7, connected at the register's outputs, and A_8 are exclusive-OR gates used to generate the feedback signal, which is determined by switches S_i^F. The switch positions are set in accordance with the primitive polynomial of the binary sequence to be generated. Note that the settings of the switches in the figure correspond to a sequence of length $2^{15}-1$, or an equivalent primitive polynomial of $x^{15}+x+1$.

A_9–A_{13} detect the all-zero condition of A_1–A_4 and ensure that the register will not be locked in that state on power-up or during normal operation. The mode control input otherwise allows A_1–A_4 to be set at any point in the sequence as determined by the S_i^I switches. □

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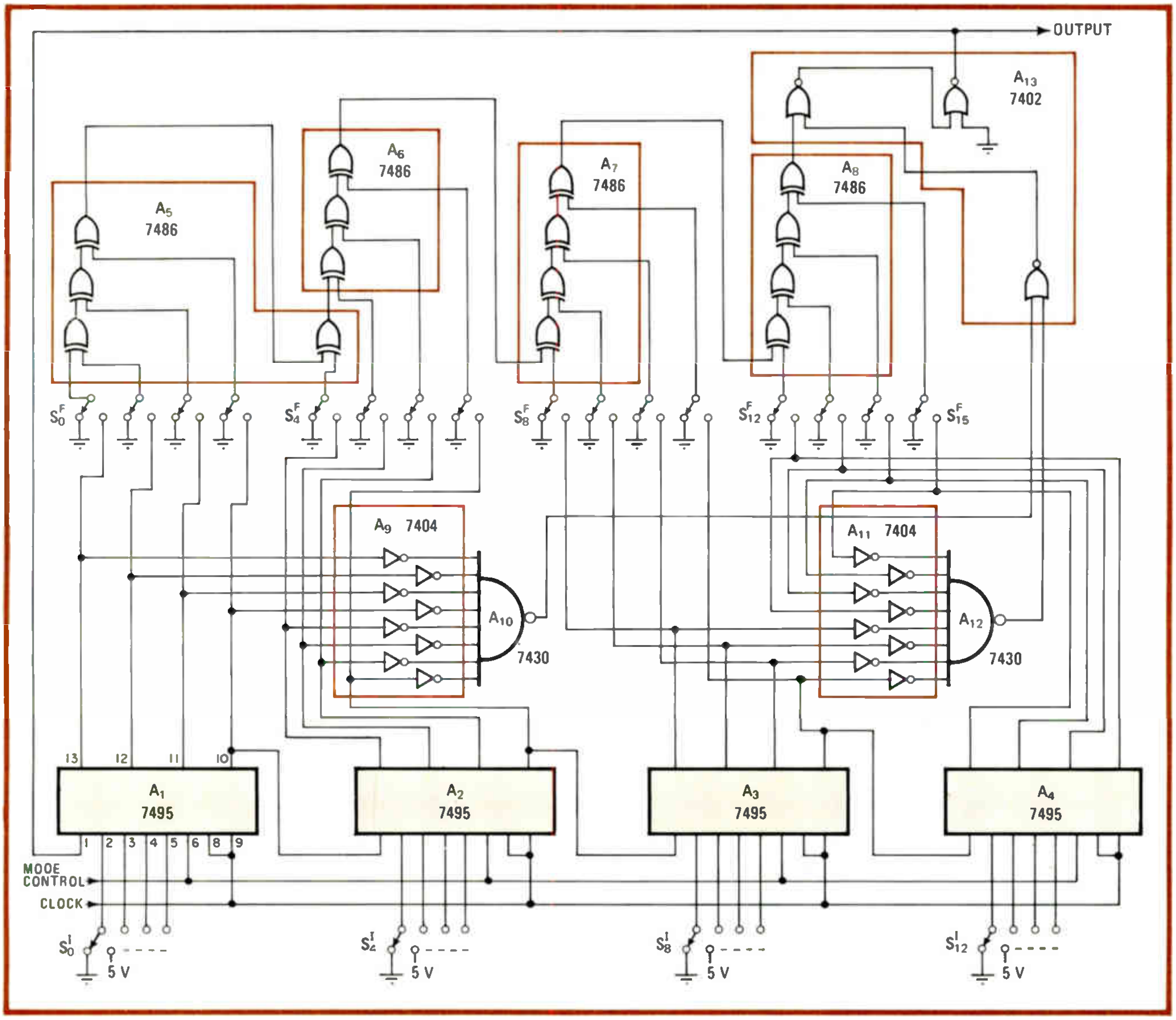

Selection. Switches S_i^F and A_5–A_8 derive suitable feedback signal so that shift register A_1–A_4 can generate a pseudorandom binary sequence of selectable length. A_9–A_{13} detect register's all-zero state and prevent register lock-up by generating logic 1 bit to A_1–A_4 input during power-initialization period. Switches S_i^I initialize registers at any point in a sequence that may extend to $2^{16}-1$ bits.

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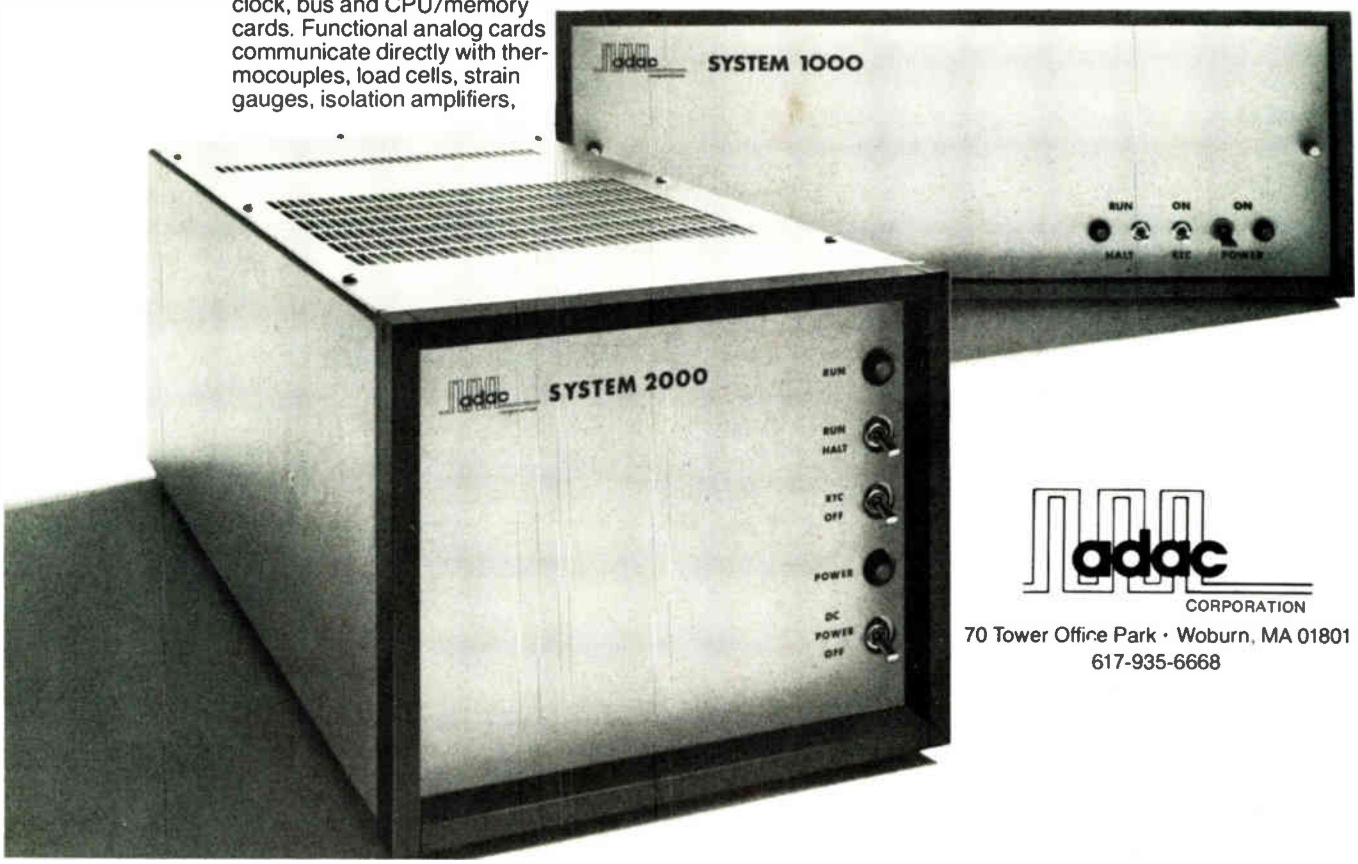

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Making it compatible and better: designing a new high-end computer

New bit-slice ALU, cache memories, and added instructions let the 990/12 triple the performance of the 990/10 while preserving the architecture of the 990 family

by Daren R. Appelt, *Texas Instruments Inc., Austin, Texas*

□ Given the extent of the investment in software on the one hand, and the advances in hardware and architecture on the other, computer engineers are facing a growing challenge: improve the speed and performance of a computer line without losing compatibility with existing family members. Texas Instruments' 990/12, a new top to its line of minicomputers [*Electronics*, May 24, 1979, p. 40], is a good illustration of new design procedures required to meet that challenge.

By using the latest bit-slice microprocessors and adding instruction pipelining to its hardware architecture, the designers tripled the computer's average performance with existing software over the previous top of the line, the 990/10. Further performance improvements come from the unique work-space cache that takes the place of—and outperforms—a conventional register file.

In addition to keeping the computer software-compatible, the designers also made it electrically and mechanically compatible with previous 990/5 and 990/10 units both to permit current memory and peripheral controller boards to be used in new systems and to allow the machine to be upgraded in the field (Fig. 1).

What's more, by doubling the instruction set and adding a writable control store, they have provided users with a means to increase speed and performance to levels competitive with those of high-end minicomputers like Digital Equipment Corp.'s PDP 11/60 and PDP 11/70 or Data General Corp.'s Eclipse line.

The third objective in designing the 990/12 was to improve its reliability and testability over that of previous processors. About 20% of the 990/12 processor's hardware is there only to enhance automatic hardware self-testing.

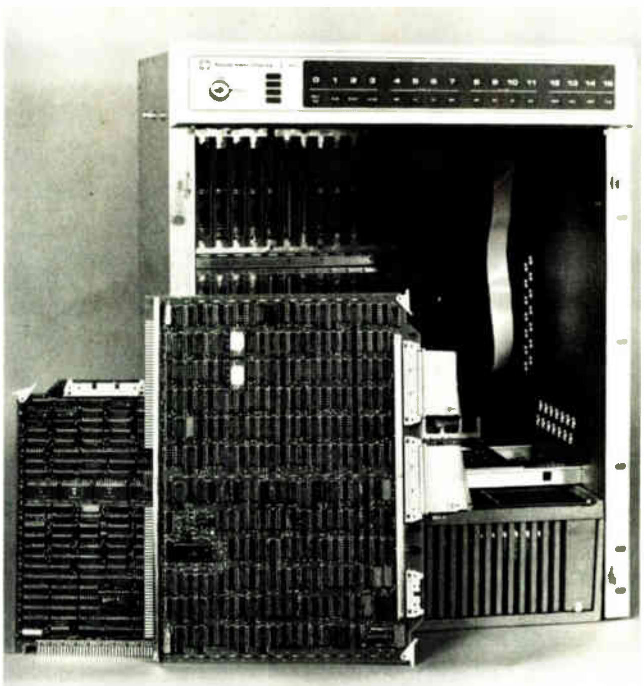
As part of the overall compatibility, the 990/12's central processing unit (CPU) is electrically interchangeable with the 990/10's. Both computers are built on two circuit boards and the identical signals are wired to identical pins at their connectors. These similarities enhance the compatibility of the machines. But there are some limits to their compatibility.

The 990/12 runs three times faster than the 990/10. It also draws nearly three times the power—about 22 amperes at +5 volts for the 990/12 versus 8 A for the 990/10. The greater power consumption means that the older, 13-slot chassis is substantially underpowered for the 990/12's CPU. Therefore a 990/10 cannot be upgraded to a 990/12 in the 13-slot chassis. The 990/10 and 990/12 can be operated interchangeably, though, in the new 17-slot chassis.

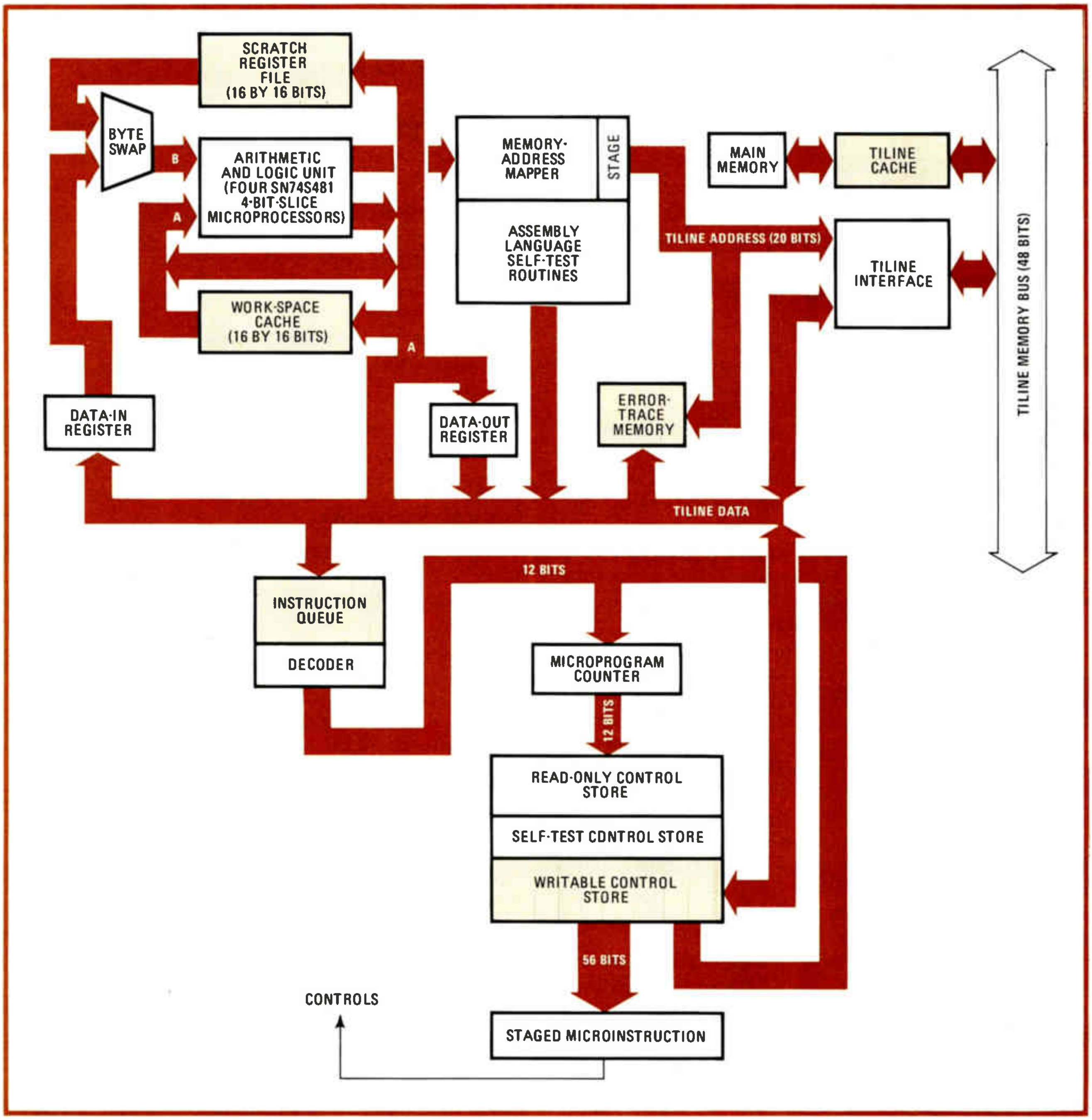
Hardware highlights

The hardware of the 990/12's CPU that resulted is different in several ways from that of existing 990 computers (Fig. 2). Instruction pipelining and the addition of two cache memories, aided by new semiconductor technology, speed up the 990's unique work-space architecture. A special error-trace memory is the center of special hardware added to promote reliability and self-diagnostics. The writable control store and new instructions further extend the 990 family's performance range (see "A question of performance," p. 136).

Instruction processing is now overlapped by staging, or



1. Growing power. The new 990/12 minicomputer, whose two-board central processing unit is shown here, not only runs existing software but is electrically and mechanically compatible with other computers. The 17-slot chassis has a bigger power supply, however.



2. Memory expansions. Adding more memory to the 990's architecture speeds the 990/12's performance. Among the new units are the work-space cache, TIline cache, scratch-register file, and writable control store. The error-trace memory aids diagnosis.

pipelining, the memory-address mapping cycles ahead of the actual memory-access cycles. It is accomplished by look-ahead instruction fetches into a two-register instruction queue and by staging micro-instructions and data to and from memory. One thing that has remained the same is the 48-bit-wide TIline bus that forms the computer's backplane, interconnects the elements of the computer, and is the basis of the 990/12's electrical and mechanical compatibility.

The arithmetic and logic unit (ALU) portion of the 990/12's CPU is implemented with TI's SN74S481s, 4-bit-slice Schottky TTL microprocessors, instead of with the slower standard TTL used on the 990/10. The SN74S481 contains a double-length (32-bit) accumulator, a program counter, and a memory-address register. In addition to logic and arithmetic operations, this microprocessor has a built-in sequence for multiplying, dividing (both signed and unsigned), and generating a cyclic redundancy code.

Two transparent latches at each input to the arithmetic and logic unit allow ALU input buses to be used twice. That is, after these latches have stored the input operands to the ALU, the buses are free to be used to transfer different data to other places in the system.

The scratch register file, also new to the 990 family, is used primarily to assist in implementing the extended instruction set, especially the floating-point routines, and uses written microcode. The 16 registers are visible only at the micro-instruction level, and only one register (the work-space pointer) is preempted by the system.

The memory-address mapper implements the same mapping functions as in the 990/10. Although most of the mapping functions are executed on the state prior to the memory reference, the penalty for not premapping is minimized by making the mapping time fast.

A new two-word instruction register queue, used in pipelining, especially benefits the shorter, single-word instructions. It also makes decoding for two-word instructions easier and faster—an important factor, as the new extended instruction set has many such instructions.

Support hardware for the self-testing features allows the CPU to be tested without depending on other system members and lets the fault be isolated to the printed-circuit-board level, while at the same time qualifying the CPU hardware to execute diagnostic software used at higher levels. The test-support hardware consists of 256 words of read-only control store, a portion of the writable control store used for rolling in additional tests from the local erasable programmable read-only memory (E-PROM), latches that create loop-back paths when there is no other way to directly confirm test results, and internal error-trace memory.

The self-test sequence is automatic on power-up or can be initiated by diagnostic software with an execute-microdiagnostics instruction. In either case, the sequence begins with execution of the 256 micro-instructions of the microdiagnostic initialization program that is written into the control store.

Error-trace memory

During normal operation of the 990/12 system, a circular buffer memory of 16 32-bit words is always functioning to record each memory reference. This circular buffer, unusual in a minicomputer, is called the error-trace memory and is used for recovery and diagnosis in case of errors caused by software or hardware. Each word in the error-trace memory records the details of what happened during one reference to memory, including the 16-bit address, whether a read or write was attempted, and the condition of various flags. The reference to memory will be recorded in the error-trace memory regardless of what type of memory is referenced—the work-space cache, TIline cache memory, or the main memory.

In the 990/12, interrupt level 2 is reserved as the system-error interrupt level. As soon as the level 2 interrupt trap occurs, the error-trace memory is stopped, maintaining the record of what happened for the last 16 memory references. Level 2 interrupt software examines the error-interrupt status register to determine why the interrupt was generated. Then, by examining the error history recorded in the error-trace memory, the software can reconstruct how and why an error occurred.

However, not all level 2 interrupts are really system faults. Other conditions are handled at this level if their disposition is similar to faults. For example, if a breakpoint has been set up in the breakpoint register and its conditions are met, the level 2 trap occurs. This preserves a record of the events leading up to the breakpoint—very useful information for software debugging.

The addition of a work-space cache to the 990's hardware results in a significant increase in the speed of the basic architecture.

Work-space cache

The 990's unique work-space architecture actually has its register file in main memory, instead of having dedicated registers in the CPU. This cost/performance tradeoff favors low-end applications of the architecture in those applications having many interrupts—the kinds of application in which a TMS 9900 microprocessor or microcomputer is typically used. Even though an average of 40% of the CPU's memory references are spent accessing the work-space, the 990's work-space architecture fares well in such busy applications because the efficiency of the context switch largely makes up for the extra memory cycles spent accessing the work-space registers. No special memory cycles are needed to save the contents of the registers, since the registers are already in memory. The next context supplies a brand-new set of work-space registers already loaded with values needed for the task, thus saving the additional cycles usually used to load the new register values.

However, in high-end minicomputer applications more code is usually executed between context switches. In fact, additional statistics on processor activity for a typical high-end minicomputer application (running Cobol while servicing several inquiry terminals) show that typically about 30 instructions are executed between context switches, each of which performs on the average about 1.7 work-space register references. In this environment, the extra memory cycles spent accessing work-space registers are not made up for by the efficient context switch.

Aids to efficiency

To increase the 990/12's operating efficiency in such applications, 16 hardware registers were added. They can be accessed by the processor independently of main memory, but instead of operating as a typical register file, they are managed as a cache for, or buffer to, the work-space registers. The cache not only improves the performance of the 990's work-space architecture, but also lets the 990/12 outperform an equivalent conventional, register-file machine.

Each of the 16 registers has a flag bit to indicate when it has been loaded (when it is "dirty"). This cache is then operated according to the following procedure. First, at the start of execution in a new context, all registers and "register dirty" flag bits are cleared. Then, as registers are loaded during execution of the program, each corresponding register-dirty flag is set.

If an instruction tries to read a register that is not yet dirty—that is, a cache miss—the memory read cycle referencing the real work-space register (that is, in memory) is performed. This loads the value obtained from memory into the equivalent work-space cache register (marking it now dirty) and lets the execution of the instruction continue. Finally, when a context switch is to occur, those registers that were flagged dirty are

HOW MEMORY ACTIVITY IS DISTRIBUTED		
Memory function	Number of memory cycles required per 100 potential cycles	
	Without work-space cache in processor	With work-space cache in processor
Instruction-stream references	40 (40 read ; 0 write)	40 (40 read ; 0 write)
Work-space references	40 (26.7 read ; 13.3 write)	6 (2 read ; 4 write)
General data references	20 (13.3 read ; 6.7 write)	20 (13.3 read ; 6.7 write)
Total memory cycles required for execution	100 (80 read ; 20 write)	66 (55.3 read ; 10.7 write)

returned to the work space in memory and the context switch is performed.

According to the statistics of this procedure, there are typically 7.5 memory cycles used during a typical context to service the work-space cache. Since the average instruction makes about 1.7 work-space register references, the cache management overhead and the cache misses are amortized in slightly more than four instructions. ($7.5 \div 1.7 \approx 4$). Thus more than 25 out of 30 instructions run without having to perform any memory references for work-space register data. This means that a 990 with a work-space cache will use fewer memory cycles for managing the register file than will a machine with a conventional general register file, since a minimum number of registers are saved and restored for each context. Secondly, saving and restoring the appropriate registers is automatically done by hardware, eliminating the memory cycles necessary to reference register management code used in a register-file machine.

In the 990/12 processor, the work-space cache is implemented with 16 bipolar 16-bit registers and 16 separate dirty flag bits. Each of these hardware registers always corresponds to the same logical work-space register. The work-space cache procedure is performed by microcode sequence, whereas hardwired logic tests the appropriate dirty flag.

Moreover, a buffer was added to the TIline to improve the access time to main memory. In order to estimate the potential benefit of various cache memory designs to the 990/12, the designers considered the effect of a work-space cache on the activity of the processor's interface with main memory.

As can be seen from the statistics in the table, the work-space cache in the 990/12 processor changes the functional distribution of memory activity on the TIline bus and reduces the total number of cycles required to execute a program. With the work-space cache, instruction stream references dominate the memory activity. This will, in general, increase the hit ratio—the number of times what is wanted is found over the number of times it is looked for—of the new TIline memory cache, the reason being that the cache is filled with adjacent blocks from memory and references to the instruction stream tend to be localized. The dramatic reduction of work-space-related memory activity will, in addition, allow more room in the cache for storing instructions and general data, further increasing the cache's hit ratio.

Since the number of memory write cycles required to execute a program is cut nearly in half by the work-space cache, it is less important for a TIline cache to be efficient on write cycles. One result is a cost savings in the cache design at very little detriment to system performance. Overall, adding the work-space cache to the processor not only reduces the number of references to the main memory, and hence its bandwidth requirements, but also improves the effectiveness of the new TIline cache memory.

Microcoded

As with the 990/10, the instruction set of the 990/12 was implemented with microcode. But the new computer also allows users to develop their own instructions using the writable control store (WCS) area.

The control store was designed to contain up to 4,096 64-bit words, much more than the 256 56-bit words used in the 990/10 (Fig. 3). Only the first 3,072 words are currently implemented. The first 2,048 words are currently implemented in read-only memory and contain the microcode for the 990/12 instruction set and a portion of the self-test microcode. The next 1,024 words are the writable control store and are implemented in random-access memory. Of these, 496 words and some of the extended-operatons (XOP) instruction levels are reserved for use in future software packages.

Entry to the WCS is via the XOP instruction. This instruction can operate in two ways: it can perform a context switch indirectly through a work-space pointer and program counter vector in memory, or it can transfer control directly to the microcode in the WCS.

The fact that the XOP instruction has two operating modes allows a developer to write applications that use special XOP functions and have those same functions be implemented in either microcode or assembly language. This flexibility provides software compatibility, since the application program does not have to take into account whether the function is implemented in microcode or assembly language subroutine. A user can run the application program on the low-performance model or on a

990/12 with the function implemented in microcode in the writable control store.

During the design of the 990/12's hardware, a parallel effort was started to produce a set of utilities for implementing the instruction, self-test, and diagnostic microcode. The plan was to supply these same utilities later on for customers to use when developing writable control store microcode. The result is an unusually complete set of utilities, including a microcode assembler (MICASM), a microcode debugger (MICDBG), and a microcode converter (OBJIO).

Microcode development utilities

The microcode assembler accepts directives, comment statements, and microcode statements from the user; performs validation on the statements; and produces object microcode. Microcode assembly directives determine such things as the format of the assembly listing, whether a cross-reference of microcode mnemonics and labels is to be produced, and what the next microcode address will be.

Although the assembler performs three types of validation on each microcode statement, a user could develop a microcode that would put the 900/12 in such a state that it would have to be reinitialized. Therefore the microcode debugger was developed. This utility allows a user to debug his microcode to such a degree that he can be 99% confident that his microcode will operate as designed when it is finally loaded into the writable control store.

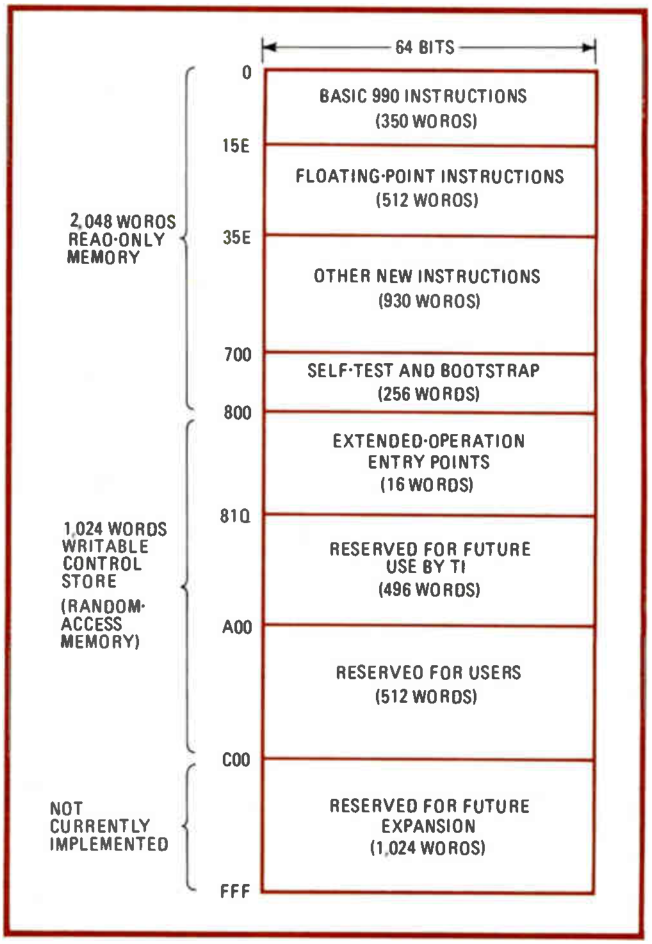
At the beginning of the 990/12's development, only the microcode assembler was thought necessary. There was great reluctance to commit valuable and limited manpower to the implementation of a microcode debugger. The feeling at the time was that 990/12's hardware would be operational when the instruction microcode was ready to be checked out and therefore could be used for that purpose.

The decision to implement the debugger anyway was a good one for several reasons. As it happened, the hardware was not ready as soon as expected, and without the debugger a big slip in the schedule for testing the microcode would have resulted. Also, microcode integration on the 900/12 check-out machine in fact went very quickly because the majority of programming bugs had already been found by the debugger. Finally, when problems were found, it was easier to determine whether the hardware or the microcode was to blame.

The converter's job

The microcode assembler and debugger both use a logical microcode layout when performing their operations to make implemention and documentation easy, but the layout must be rearranged before loading the microcode into the writable control store. Consequently, the microcode converter was designed to map the logical bit pattern to the physical bit pattern of the microcode word and to place the microcode into a file in the format required by the operating system.

The 990/12's instruction set consists of two parts: the basic 72 instructions implemented on the 990/10, and the 71 instructions that were added to enhance the new machine. Of the basic 990/10 instructions, 31 deal with program control and 41 operate on data.



3. Room for more. Of the 4,096 64-bit words of control store in the 990/12, only 3,072 are currently implemented. Of these, 1,024 words are available for the first time as a writable control store and other sections are reserved for future software enhancements.

Among the new instructions, the most important are those dealing with floating-point arithmetic, string manipulation, bit operations, and a new stack capability. The 22 floating-point commands provide full support of both single-precision (32-bit) and double-precision (64-bit) floating-point arithmetic in the standard IBM format (hexadecimal exponent). These operations are examples of how implementing instructions in firmware can eliminate software. For instance, the floating-point operation ADD REAL, which is in firmware in the 990/12, was a subroutine in the 990/10's software.

For the first time, a member of the 990 family can deal directly with strings of up to 65,536 bytes because of the 7 new byte-string commands. Another 10 of the new instructions operate on bit arrays and variable-length bit fields in memory. Previously, masking routines of greater complexity were needed to manipulate just single bits. The new instructions also provide data movement to and from stacks. Push, pop, and move-from-stack operations can be performed, and each instruction can move a variable amount of data.

Among the other new commands are 11 that enhance the basic instruction set by adding new address modes

A question of performance

Performance is the real benefit that a 990/12 offers to a user, but the obvious question is how much? Simple answers, however, are hard to come by and could in any case mislead customers.

First, consider the problem. The 990/12 has, for example, 25 possible operand derivations for the add instruction. The source may be register, register pointer, register pointer increment, indexed memory, or nonindexed memory. There are the same five possibilities for the destination, and since any source may be combined with any destination, the result is 25 possibilities.

The 990/12 also has a subset of possible memory locations for each operand data word. Memory data may be located in cache or main memory; register data may be located in work-space cache, cache memory, or main memory. The combination of different operand derivations plus different memory-access times yields 2,025 possibilities for that one instruction.

Furthermore, the 990/12 has instruction look-ahead. That means that the execution time of an instruction varies according to the identity of the preceding instruction and locations of the operands for that instruction. In actuality, the execution time for the add instruction varies only from 0.552 to 4.364 microseconds.

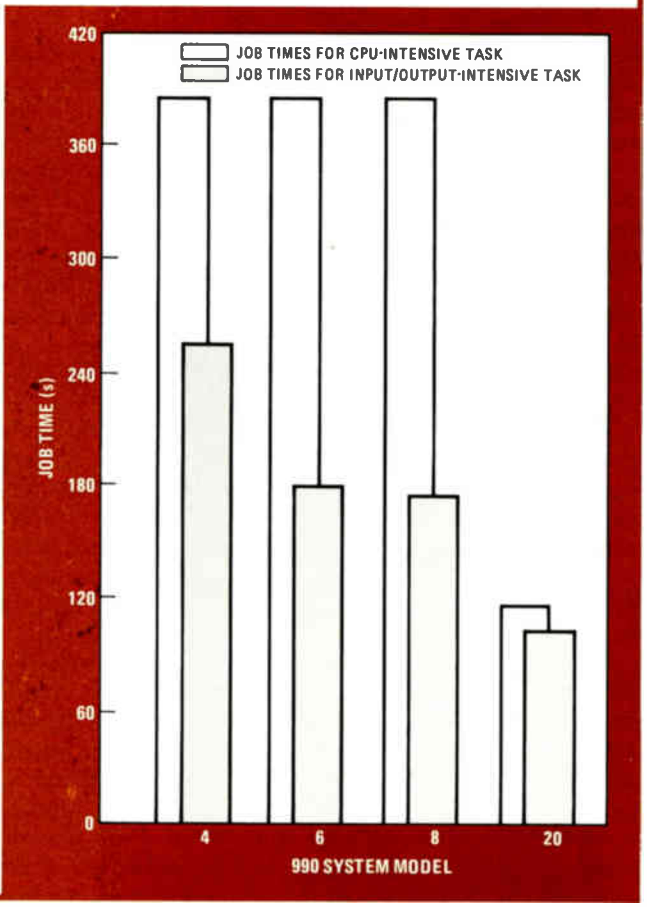
Obviously, it is impossible to look at a table of 990/12 execution times and draw meaningful, accurate conclusions about its speed, although some people would no doubt make the attempt.

Statistical methods provide a more accurate performance picture. The obvious solution is to run a great deal of code through a 990/12 and measure the average execution time. One problem with this approach, though, is that there are a number of factors that affect the average execution time, including the size of the files, the size of the records, and so forth.

TI is currently benchmarking the 990/12. The graph to the right is representative of the data to date. For these tests, four system configurations were tested: a model 4 consisting of a 990/10 CPU and a 10-megabyte disk; the model 6 with a 990/10 CPU and 25-megabyte disk; a model 8 made up of a 990/10 CPU and a 50-megabyte disk; and finally the model 20, the new 990/12 CPU with both caches and a 50-megabyte disk.

On test 1, a CPU-intensive task, note that models 4, 6, and 8 all execute in the same time, 380 seconds, because they all use the same CPU—the 990/10. The model 20 uses a 990/12 CPU with TIline cache and executes in 115 seconds—slightly more than three times the speed of the 990/10, as expected.

Test 2 is an input/output-intensive task. The model 4 uses a slower disk and therefore requires the longest time to execute. Models 6 and 8 use disks with identical transfer times but with a slightly faster average access time on the latter. Both are faster than the model 4, and the difference between them and the model 4 depends on disk performance only. The model 20 uses the same disk as the model 8, and the difference in this case is due to the higher performance of the 990/12's CPU. Thus it can be seen that I/O-intensive tasks depend mostly on the speed of the peripheral device.



and more efficient program control, 10 that operate on extended-precision binary values, 2 for decimal conversion, 1 for searching linked lists, and 3 for controlling the writable control store.

The new hardware self-test instruction, execute microdiagnostics (EMD), causes the entire state of the processor to be cleared, including all internal registers and the WCS, and activates hardware reset lines that clear and reset all peripheral controllers and interrupts. It then causes execution of the microdiagnostic portion of the initialization program, checks the entire control store, and tests the microcontrol RAM (the WCS) and the data paths in the basic ALU using microdiagnostics overlaid into the WCS. Successful testing will result in execution of the power-up trap (interrupt level 0). An unsuccessful test will light appropriate board-level fault indicators.

Needless to say, EMD is a privileged instruction and is used by software only as a last-gasp measure to ensure that the 990/12 processor is functional. It is automatically executed when power is turned on.

The 990 computer family was planned starting in 1973 to be cost-effective over a very wide performance spectrum. It now encompasses a full range of 16-bit processors, ranging from the TMS 9900 microprocessor, to the 9940 one-chip microcomputer, the TM 990 family of microcomputer boards, and on to several minicomputers, including the TM 990/4, the 990/5, the 990/10, and the new 990/12. □

Transistors—a hot tip for accurate temperature sensing

Matching transistors by their base-emitter voltage and dc gain ensures consistent operation from unit to unit

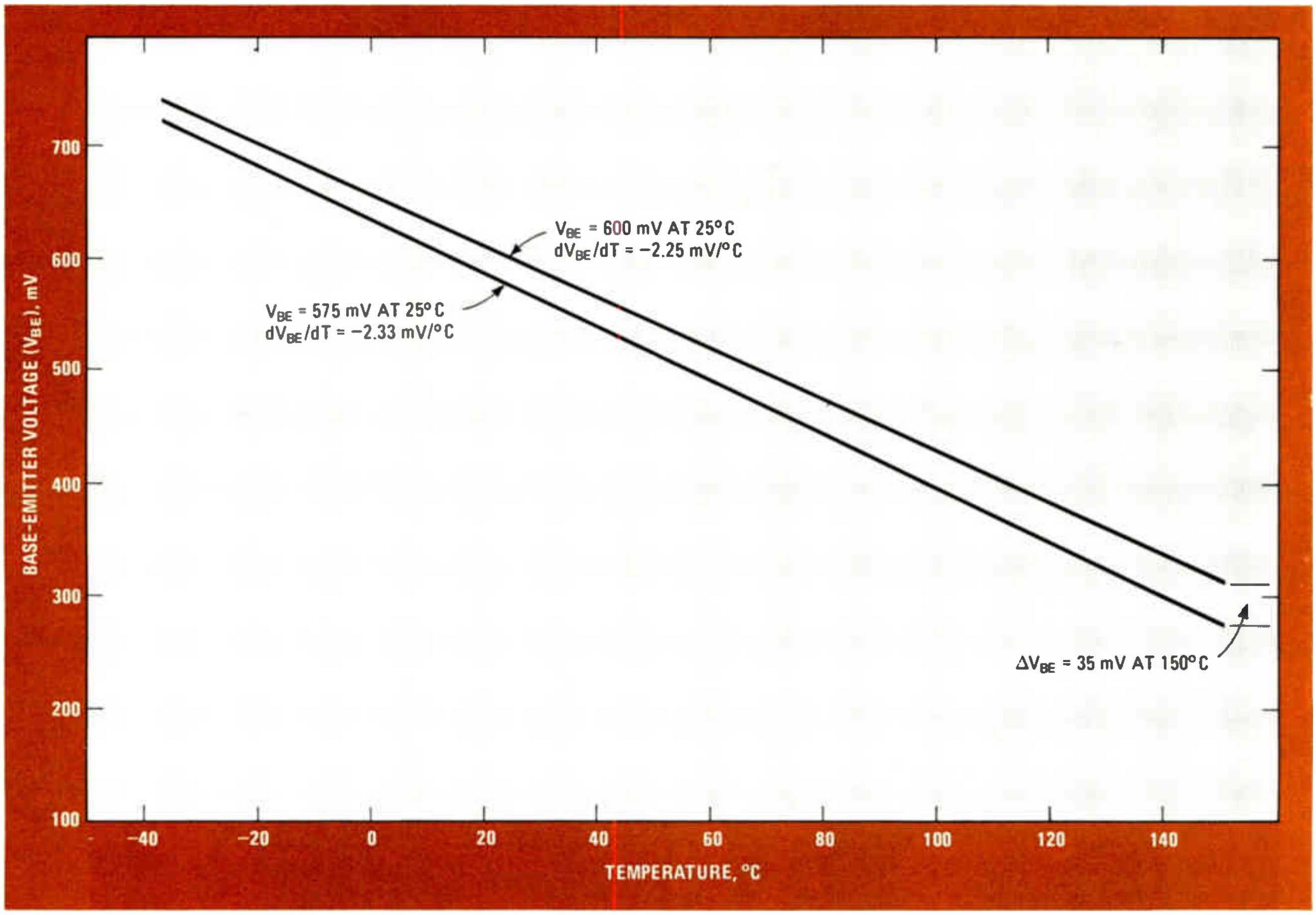
by Pat O'Neil and Carl Derrington, *Motorola Semiconductor Products Inc., Phoenix*

☐ Transistors would seem to be ideal temperature sensors. Their low cost, their ability to operate consistently over long periods, and their sensitivity and linearity recommend them for this use. For some time, in fact, temperature measurements have been made using the base-emitter voltage of forward-biased transistors.

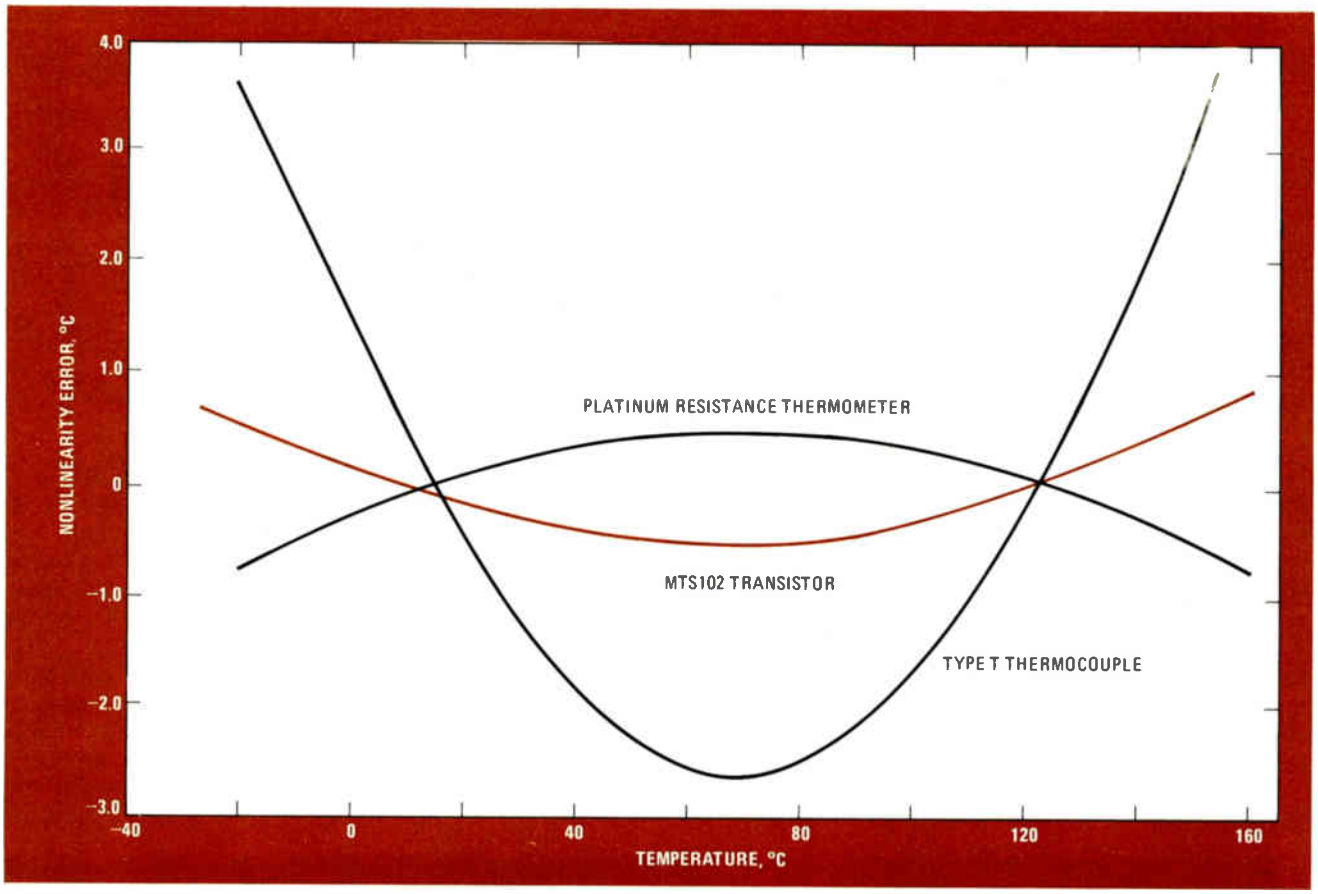
The big problem in using transistors in this application has been that of finding transistors with characteristics matched closely enough to allow them to be used interchangeably. If it were not for this difficulty, their use as temperature sensors would be widespread indeed.

The quest for interchangeable semiconductor sensors has led manufacturers to build monolithic integrated circuits whose output is the difference of two junctions with differing current densities or ones that employ laser trimming to equalize circuit parameters. Although these techniques do provide interchangeable devices, they do so at a cost that prohibits their use in throwaway applications—monitoring the curing temperature of concrete with imbedded sensors, for example.

But the improvements in production line capability that make large-scale integration possible also make it possible to produce discrete transistors with tightly controlled and matched geometries. Motorola's MTS family is a transistor series selected specifically for temperature sensing applications. It consists of three



1. Single-point prediction. When transistors have the same dc gain, their performance across a range of temperatures can be predicted by measuring their base-emitter voltage at a specific temperature. Variation in V_{BE} can result in large errors.



2. In context. Although they are inherently nonlinear, transistors perform quite admirably when compared to other devices. Between -40° and +150°C, the MTS102 rivals more expensive platinum resistance thermometers and easily outshines type T thermocouples.

transistor types: the 102, 103, and 105, which provide guaranteed accuracies to within ±2°, ±3°, and ±5°C, respectively, over the range from −40° to +150°C.

Transistors with these accuracies are obtained by screening transistors for matched direct-current gain and base-emitter voltage at room temperature, using a constant collector current of 100 microamperes. For any type within the family, the base-emitter voltage (V_{BE}) must be within a specified tolerance; nominal V_{BE} may be any value from 580 to 620 millivolts. For example, the V_{BE} of an MTS102 is matched to a tolerance of ±3 mV and the nominal figure, say 600 mV, is printed on its package. Any MTS102 can be used to replace another with the same V_{BE} with the stated ±2°C accuracy maintained. In matched lots of 10,000, the sensors are priced at 27 to 66 cents apiece, depending upon the temperature tolerance.

Electrical consistency

For any given series of transistor temperature sensors, it is necessary to specify only the relevant and measurable electrical characteristics—V_{BE} and the direct current gain at some temperature—to ensure consistent operation within a known tolerance from sensor to sensor. Furthermore, circuits can be built using such transistors that provide accuracies within ±0.01°C. The design of these circuits requires an understanding of the temperature dependence of the transistors' measured parameters. The best route is an examination of the equations that describe a transistor's operation.

The base-emitter junction of a transistor can be regarded as a simple pn junction diode. If a constant current, I_F, is forced through the junction in a forward direction, then its relation to the measurable junction voltage, V_J, is given by the Shockley equation:

$$I_F = I_{sat} e^{qV_J/kT - 1} \quad (1)$$

where k is Boltzmann's constant, q is the net charge in coulombs, T is the temperature in kelvins, and I_{sat} is the saturation current.

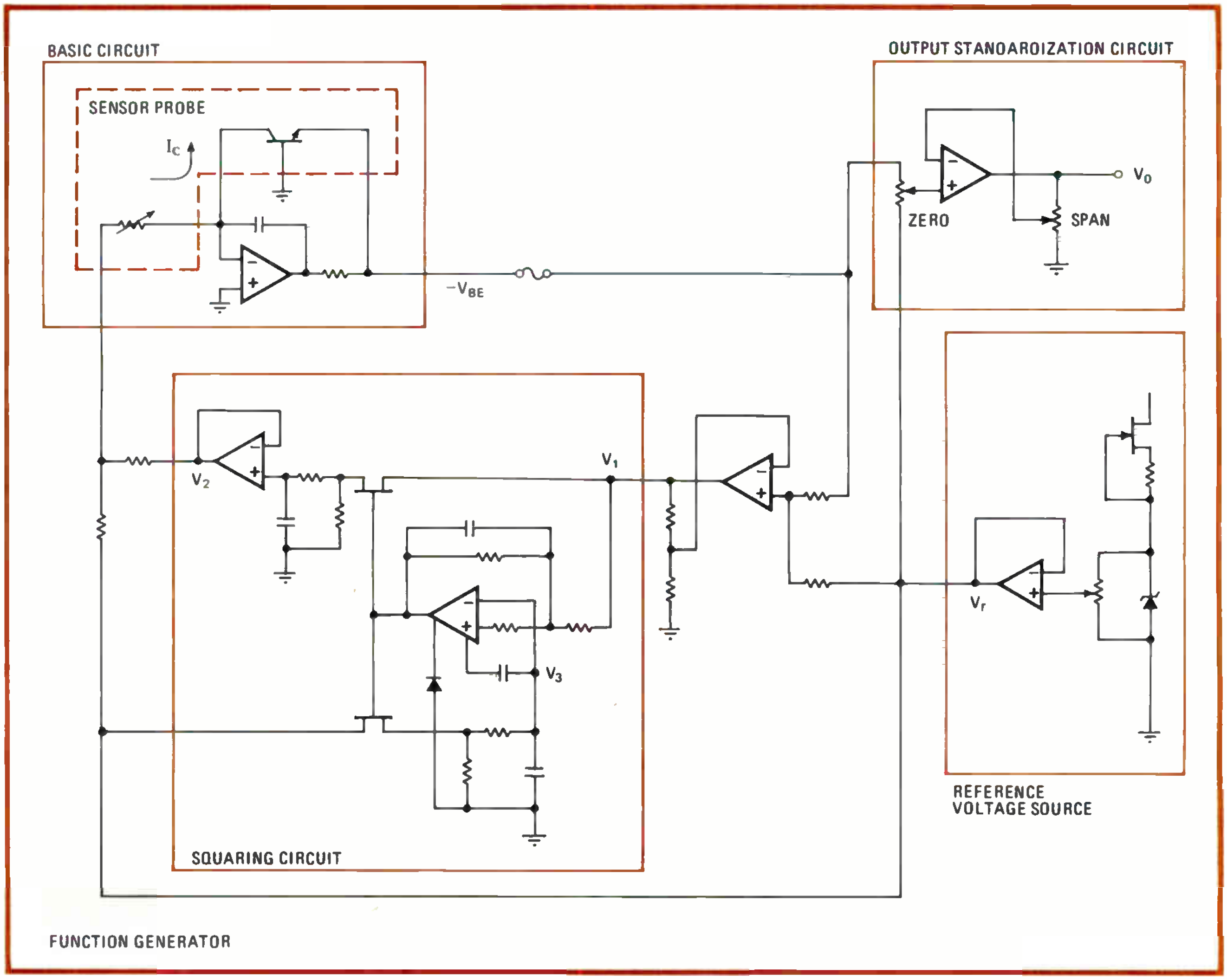
When the junction voltage is sufficiently large (that is, when the diode is sufficiently forward-biased), the −1 term in the exponent can be ignored and the equation can be expressed in terms of V_J:

$$V_J \cong (kT/q)\ln(I_O/I_{sat}) \quad (2)$$

With I_F held constant, if all other terms in the equation were independent of temperature, the junction voltage would be directly proportional to the thermal voltage expression kT/q and thus to temperature T. Unfortunately, the saturation current is composed of two temperature-dependent currents: that due to the hole diffusion, I_p, and that for the electrons, I_n. The hole-diffusion current is given by:

$$I_p = qA(D_p/L_p)p_{no}$$

where A is the area of the device, D_p is the diffusion constant for the holes, L_p is the diffusion length for holes



3. High accuracy. To obtain high performance, the collector current of temperature-sensing transistors can be varied in accordance with temperature (reflected by base-emitter voltage) raised to some power. The squaring circuit shown performs this function.

in the n region, and p_{no} is the equilibrium hole concentration in the n region.

The last term, p_{no}, is temperature-dependent and is defined by:

$$p_{no} = n_i^2/N_D$$

where N_D is the concentration of donor atoms imparted to the material by doping and n_i^2, the square of the intrinsic concentration, is given by:

$$n_i^2 = N_c N_v e^{-E_G/kT}$$

The terms N_c and N_v are the equivalent concentrations of conduction and valence states for the doped material; E_G is the potential of the energy gap between bands in electron volts.

Defining saturation

The equation for I_n is similar to that for I_p, with appropriate substitution of n terms for p terms: D_n is the diffusion constant for electrons, L_n is the diffusion length for electrons, and N_A is the concentration of acceptor atoms.

Adding the equation for I_p to the equivalent equation for I_n results in the following expression for the saturation current:

$$I_{sat} = I_p + I_n = qAN_cN_v e^{-E_G/kT} g \qquad (3)$$

where g represents $[D_p/(L_pN_D)] + [D_n/(L_nN_A)]$. Substituting this expression into Eq. 2 gives:

$$V_J \cong E_G/q + (kT/q)\ln[I_F/(qAN_cN_v g)]$$

Again, this seems to result in a directly linear relationship of voltage to temperature. But the terms D_p and D_n are both related to temperature-dependent terms: the thermal velocities of holes and electrons. Furthermore, this dependence need not be identical. So while the quantity represented by g above can be obtained by a measurement of V_J at a specific temperature, finding that two V_Js are equal at that temperature in no way guarantees that they will be equal at another.

Fortunately, there is the familiar dc gain term for the transistor, h_{FE}. This term represents the relationship:

$$h_{FE} = I_n/I_p = [D_n/(L_nN_A)]/[D_p/(L_pN_D)]$$

If the dc gains of two transistors are equal, it means that I_n and I_p vary in the same way with respect to one

Bounding the error

The curves in Fig. 1, which are used to set a tolerance for V_{BE} that limits the temperature measurement error, assume a linearity for transistors that does not exist, as experience proves. A demonstration that these linear curves form the boundaries of possible error is required for confidence in their use.

The assumption that the transistor's V_{BE} is linear leads to the following expression for the approximate value of V_{BE} ($\tilde{V}_{BE}$):

$$\tilde{V}_{BE} = \tilde{V}_{BE1} + (dV_{BE}/dT)(T - T_1)$$

Since the measured curve is not linear, the error in the above expression can be minimized by using the following linear regression coefficients to adjust measured values:

$$d\tilde{V}_{BE}/dT = \{(V_{BE} - \{V_{BE}\})(T - \{T\})\}/\{(T - \{T\})^2\}$$
$$\tilde{V}_{BE1} = \{V_{BE}\} - (dV_{BE}/dT)(\{T\} - T_1)$$

where the symbols $\{\ \}$ indicate the average value of the enclosed quantity within the operating range.

If T_1 is now chosen to be the average temperature in the range from $T_1 - \Delta T$ to $T_1 + \Delta T$, the above equation can be restated as:

$$d\tilde{V}_{BE}/dT = (r/3)(k/q) - (V_{go} - V_{BE1})/T_1 - (r/2)(k/q)(T_1/\Delta T)^2[1 - f_1(1 + \Delta T/T_1)(1 - 2\Delta T/T_1) + f_2(1 - \Delta T/T_1)(1 + 2\Delta T/T_1)]$$
$$\tilde{V}_{BE1} = V_{BE1} + (r/2)(k/q)T_1(1 - f_1 + f_2)$$

where

$$f_1 = (1 + \Delta T/T_1)/[2(\Delta T/T_1)\ln(1 + \Delta T/T_1)]$$
$$f_2 = (1 - \Delta T/T_1)/[2(\Delta T/T_1)\ln(1 - \Delta T/T_1)]$$

An examination of these expressions indicates that a simple bounded estimate of the error resulting from the assumption of linearity is obtained by joining the extreme points of the V_{BE}-versus-temperature curves, as has been done in Fig. 1. At temperature T_1, the resulting error is:

$$\Delta\tilde{V}_{BE} = (r/2)(k/q)[(1 + \Delta T/T_1)\ln(1 + \Delta T/T_1) + (1 - \Delta T/T_1)\ln(1 - \Delta T/T_1)]$$

another. So if two transistors have equivalent h_{FE} and V_J (which, for a transistor rather than a diode, is the base-emitter voltage V_{BE}), they will react in the same way with temperature variation. Thus they will be interchangeable for temperature-sensing applications.

Inherent nonlinearity

While defining the base-emitter voltage and dc gain does ensure similar operation, the inherent nonlinearity of the transistor must be considered if devices are to operate within a desired tolerance. Starting with the linear equations above, it is possible to move into the world of real, nonlinear operation to see how these parameters dictate actual performance.

For a transistor, I_F in Eq. 1 is actually the collector current I_C. If the summation term is expressed as a function of temperature, T, raised to some power r, substituting Eq. 3 for I_{sat} in Eq. 1 yields:

$$I_C = A'T^r e^{-qV_{go}/kT} e^{qV_{BE}/kT - 1} \quad (4)$$

A′ represents the pre-exponential constants qAN_cN_v, and the band-gap potential of silicon at 0 K (V_{go}) multiplied by charge q has been substituted for the more general term E_G.

When the collector current is constant and V_{BE} is sufficiently large that the −1 term in the exponent of Eq. 4 can be ignored, it is possible to express V_{BE} in terms of a specific base-emitter voltage, V_{BE1}, known at temperature T_1:

$$V_{BE} = V_{BE1}(T/T_1) + V_{go}(1 - T/T_1) - r(kT/q)\ln(T/T_1)$$

This represents the basic relationship governing the operation of the transistor as a temperature sensor. Taking this equation's derivative with respect to temperature naturally gives the rate of change of V_{BE} with respect to temperature, usually referred to as the temperature coefficient:

$$dV_{BE}/dT = -rk/q - (V_{go} - V_{BE})/T$$

For the MTS series of transistors, an empirical version of this equation has been determined using a V_{BE} of 600 millivolts at 25°C:

$$dV_{BE}/dT = -2.25 + 0.0033(V_{BE} - 600)\ \text{mV/°C}$$

Figure 1 plots this equation when the actual V_{BE} is 600 mV and when it is 575 mV. Comparison of the two curves shows that variation in V_{BE} can result in measurement errors of as much as 15°C. Fortunately, it can be shown (see "Bounding the error," above) that specifying the maximum change in V_{BE} at the extreme points of the curve limits the possible measurement error.

Measured nonlinearity for a typical MTS102 transistor is shown in Fig. 2, along with typical nonlinearity curves for a type T thermocouple and a platinum resistance thermometer. Calculating the regression coefficients for a least-squares fit to a straight line (R^2 = 1.00000 for a perfectly linear device) yields a value of 0.99866 for a type T thermocouple and 0.99999 for the MTS102 and the platinum resistance thermometer. This indicates that the transistor is far superior to the thermocouple and equal in capability to the more expensive platinum thermometer for this range.

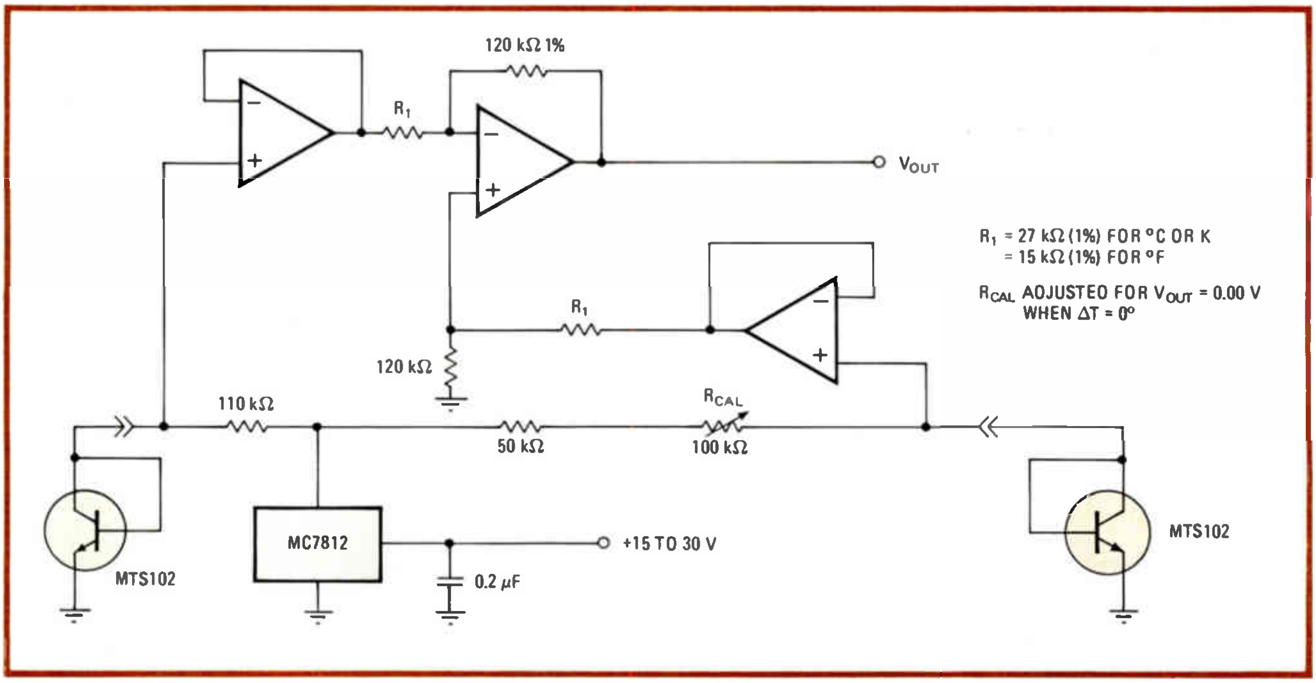
Circuits improve accuracy

There are, of course, many applications in which the error due to the nonlinearity shown would be unacceptable. For such cases, it has been found that the operation of transistor temperature sensors can be improved if the collector current I_C is forced to react in accordance with this equation:

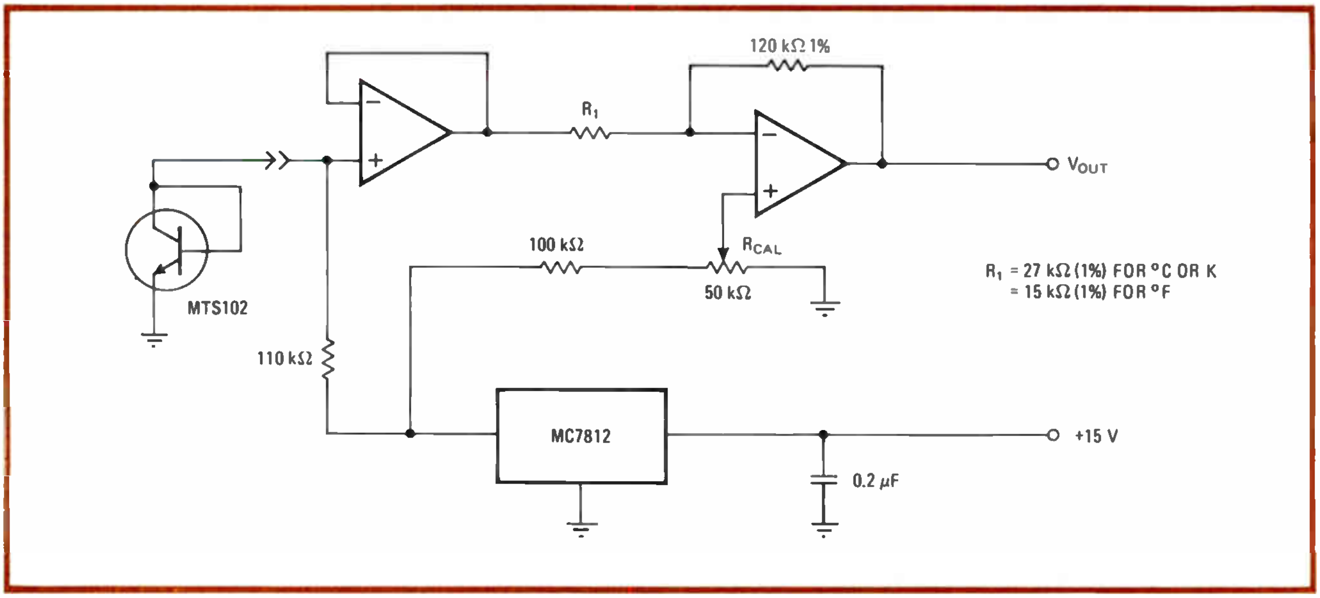
$$I_C = I_{C1}(T/T_1)^x$$

where I_{C1} is the collector current at T_1. The theoretical value of x at which nonlinearity ceases is r, the exponent of T in Eq. 4.

Using this concept, practical circuits have been built in which a standard transistor used as a sensor yielded accuracies within ±0.1°C (see Fig. 3).[1] Using a more



4. Simple difference. Differential temperature readings, frequently needed in process controlling, can be inexpensively obtained using the configuration shown. The same circuit could also be used to set an alarm when temperature stability is critical.



5. Even simpler. A single transistor version of the circuit shown in Fig. 4 requires even fewer components. Since the transistor itself is inexpensive, it and others like it can be left in place and the remaining circuitry built into a portable meter.

complex and precise squaring circuit and three-point calibration, ±0.01°C uncertainty can be achieved. It is also interesting to note that the worst-case error occurs when x is equal to zero (that is, when I_C is constant), as has been assumed throughout the preceding analysis.

Since it is possible to match transistors so that their responses track variations in temperature, there are many low-cost designs that are commercially viable. For example, Fig. 4 shows a design for a differential temperature sensing system that could easily be used for process monitoring. The output voltage of Fig. 5 can become the input to a digital multimeter that displays temperature in kelvins or degrees Centigrade or Fahrenheit.

Design engineers faced with the task of devising new systems for monitoring and controlling temperature would do well to bear in mind three important advantages of the transistor temperature sensor. First, it can be used interchangeably and is low enough in cost to be disposable. Second, the high sensitivity of this type of sensor provides a potential for increased accuracy, which can be realized by conditioning the collector current. Third, the transistors' relatively high output and span can often eliminate the need for amplifiers. □

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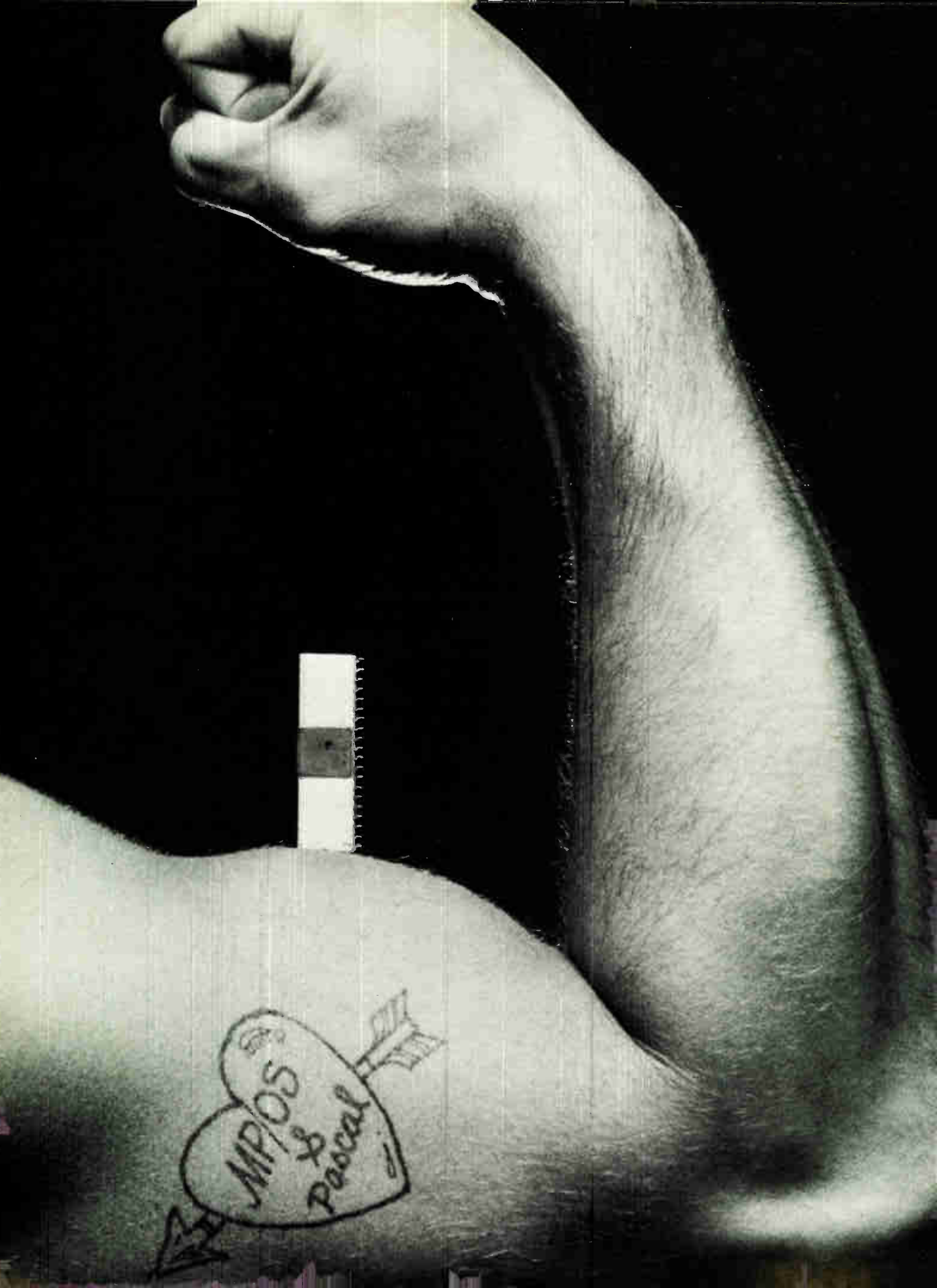
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A smart dynamic memory needs only four pins

With on-chip circuits to time-share its functions among its pins, block-oriented memory would fill the gap between disk and main memories

by Don Lauffer, *NCR Corp., San Diego, Calif.*

☐ Magnetic bubbles have been competing with charge-coupled-device memories to fill the gap in cost and performance between magnetic-disk and semiconductor random-access memories. Yet semiconductor memories, either CCDs or dynamic RAMs, could fill that gap if they adopted a new architecture at the device level: adding intelligence to the memory chip itself.

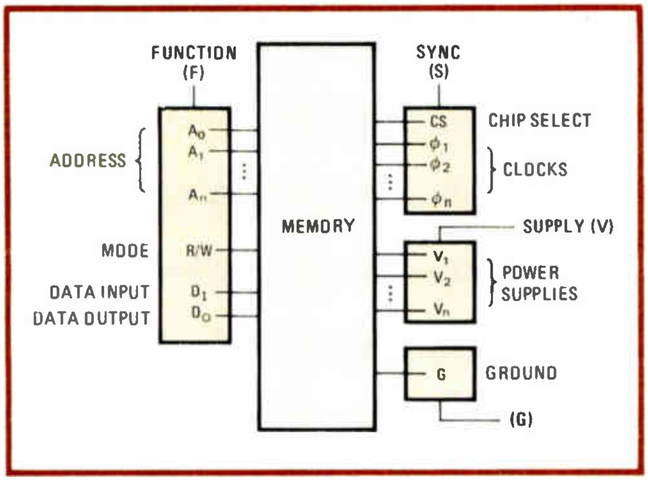
Such devices would greatly reduce the cost per bit of present-day RAMs at the system level, yet their performance would barely be compromised. Moreover, they would be easy to upgrade because they could skirt many of the pinout and bit-organization problems of current memory chips.

Time-shared functions

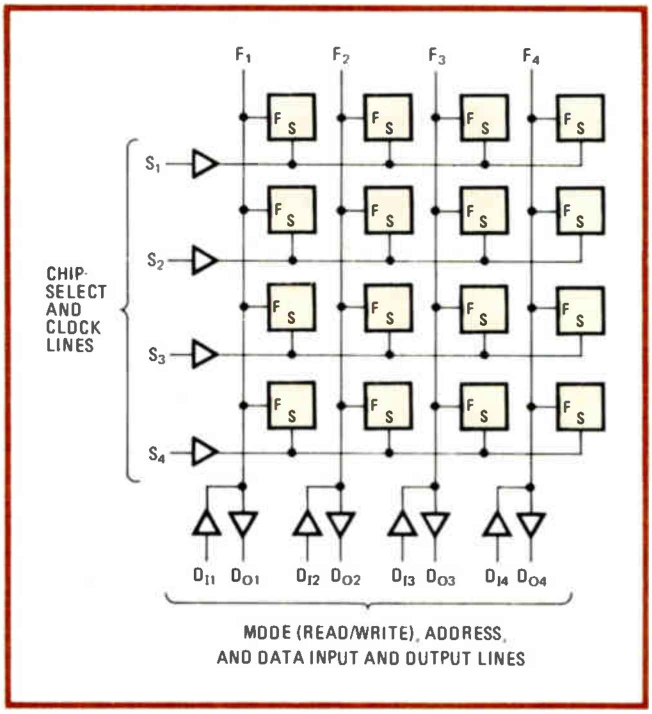
The intelligent memory would integrate on chip the electronics for time-sharing its functions among many fewer pins. The extra circuitry required is surprisingly simple and would add little to chip area since the dozen or so bonding pads and associated driver circuits of conventional memories would be eliminated. The approach is applied here to a hypothetical block-oriented memory that uses only four pins (see "Why a block-oriented random-access memory is useful").

A reduction in pin count has slashed memory costs before. The 4-K dynamic RAM realized nearly a 2-to-1 system-level density advantage in migrating from a 22-pin package to a 16-pin one. With that improvement in density, system-level bit cost was reduced correspondingly by the need for fewer printed-circuit boards, fewer peripheral circuits, and lower power requirements (see "The impact of packaging on cost per bit," p. 148). The same approach will reduce the system level cost even more dramatically if a 16-pin device can be put in a 4-pin package. In fact, as the system-level bit density improves eight times through the use of 4-pin packages, the cost savings over existing 16-pin memories approaches 50%.

The practical minimum number of pins for a block-oriented memory device is four: power supply (V), ground (G), clock or sync (S), and input/output function (F). (A possible but less practical solution would be two



1. Try four pins. A dynamic memory could be built with only four pins if intelligence were added to it. Besides supply (V) and ground (G) pins, a sync pin (S) would receive clock and chip-select information, and a function pin (F) would pass addresses and data serially.



2. Easy layout. A four-pin memory would make circuit-board layout a cinch. On a square grid F lines run vertically to stack bit-wide blocks into words, while S lines run horizontally to chip-select the words. For clarity, supply rails V and G are not shown.

pins, with the power and ground generated on the chip by rectification of the S and F signals.)

The functional pinout of a typical 16-pin memory device is shown in Fig. 1. The four boxes at the periphery of the memory serve to group the functions that must be time-shared so that the F, S, V, and G pins of a four-pin memory will be capable of handling all operations.

A typical application of the four-pin memory will best illustrate the types of circuits required. A matrix of 16 four-pin devices would be interconnected on a printed-circuit board as shown in Fig. 2. (For simplicity, the V and G connections are not shown). The example would represent a memory system comprising 256-K words of 4 bits each, if the 4-pin chips were 64-K-by-1-bit devices. The new architecture appears even more attractive if the 16 4-pin chips were each packaged in a miniature single in-line package (SIP), so that all told they would occupy the same board area as a pair of 16-pin dual in-line packages (DIPs).

All F pins in a Y axis are wired in common to permit input/output to 256-K words of 1 bit through the common input (DI) and output (DO) drivers. Likewise, the S pins in an X axis are connected to provide chip-select and clock signals to 4 of the 16 chips to form the 4-bit words. What's more, the concept lends itself to wafer-scale integration, since the four-bond dice could

Why a block-oriented random-access memory is useful

A random-access memory that, once addressed, sequentially read out (or allowed to be written into it) its complete or partial contents would be a block-oriented RAM. Such a device would be constructed by adding to a conventional dynamic RAM a presettable row counter that overflowed into a presettable column counter on the row- and column-address-decode inputs. The operation would first apply a read or write signal to the mode-control pin (R/W̄), next apply the row and column addresses and then the chip-select input, and finally apply the necessary clock signals.

The presettable counters initially accept the random address and allow reading the contents from or writing new contents into that address. Subsequent clock signals would increment the row counter with each clock pulse and allow reading from or writing into the contents of each corresponding cell until the last row. A carry bit would overflow from the row counter into the column counter, thus incrementing to the first row address in the next column. This operation could continue either until the complete memory contents were accessed or until the desired contents were accessed—at which time the chip would be deselected. With the row counter already incorporated in the device, there would be no need for addressing to refresh the cells, since it would happen automatically as the device was clocked in its unselected mode.

Such a device could be manufactured using the same process, design, and 16-pin packaging scheme as dynamic RAMs are today. However, use of the same technology and design would result in at least the same cost per bit as for a conventional dynamic RAM.

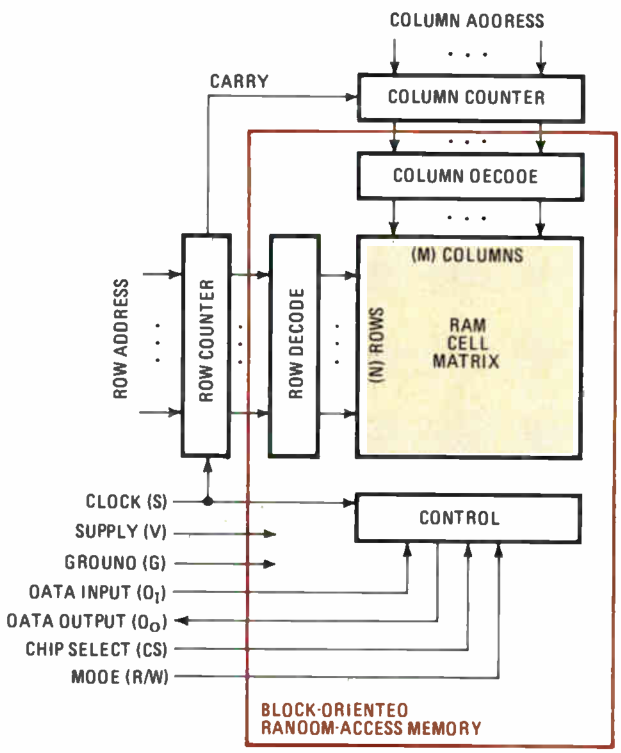
If the block-oriented RAM were to use the architecture of the four-pin concept, however, it could significantly reduce the system-level cost and power. True, the device would have a long access time, because of the serial nature of its instructions; once accessed, however, it could spew forth its contents at a high data rate.

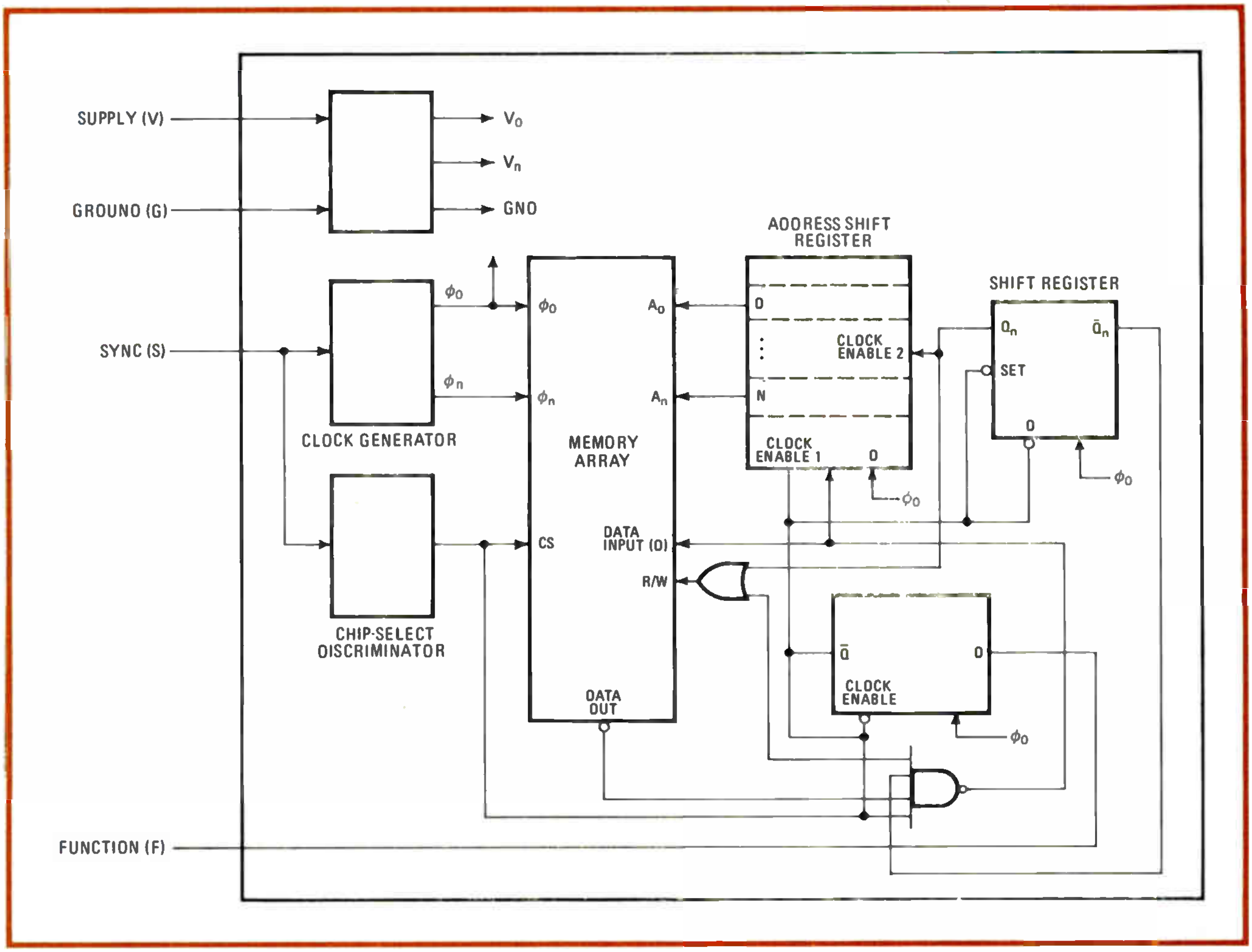
If, for example, the device contained 64-K bits, it would require access-instruction cycles corresponding to 16 serial address bits plus a chip-select and a read/write mode cycle—a total of 17 cycles to access the first bit. Thus, if the chip had a cycle time of 200 ns, it would require 3,400 ns or 3.4 microseconds to access the first bit. However, once that bit was accessed, the device could stream through its total of 65,536 bits at a rate of 5 MHz, if desired.

The access time could be improved if all blocks of data were allocated so that the first bit was always in the first row (or column). In this case, only a column (or row) address would need to be entered during access and the row (or column) address could be automatically reset to the first row (or column) on receipt of a chip-select signal. Consequently, a rectangular matrix rather than a square one might be advantageous, to optimize access time over block length.

For example, a 64-K device could use a cell-matrix of 128 columns and 512 rows. Entering only 7 bits (to select 1 of 128 columns) plus 1 bit for mode select would result in an access time of only 1.6 μs, assuming a 200-ns cycle time. However, if the block were not arranged to coincide with the first row, inordinate access delay would result. The device should end up similar to a short-loop CCD.

Using such a block-oriented RAM structure of 64-K bits housed in a four-pin package would provide a system access time of approximately 1.6 to 3.4 μs—10 times that of a conventional 64-K RAM. But the structure is suited to block storage, where it can move its entire contents at high speed—and at half the system cost of regular RAMs, it has great appeal.





3. Added intelligence. The additional interface circuits for the four-pin memory might appear excessive, but would actually occupy little additional chip area. The reason is that the dozen or so bonding pads and associated driver circuits of conventional chips are eliminated.

be laid out just as easily on a wafer. In fact, four 256-K devices could cluster to form a 1-megabit chip comprising 256-K 4-bit words, and still the package would have only seven pins—three additional ones to accommodate the wide word. It is obvious that each four-pin chip must provide its own means of extracting chip-select (CS) and clocking (ϕ) information from its S pin and of permitting entry of address, read/write control, and I/O of data on its F pin.

The S pin's tasks

Since the memory array is dynamic, comprising either one-transistor RAM or CCD cells, each cell requires refresh, or continuous clocking by means of which the stored data is amplified and restored to its full representative voltage level. Present-day CCD memories generally use two to four clock pulses each cycle to rotate the memory by 1 bit. Similarly, the circuitry in the front end of the chip's S pin could develop the various clocks required to rotate the memory by 1 bit when a synchronizing pulse is applied.

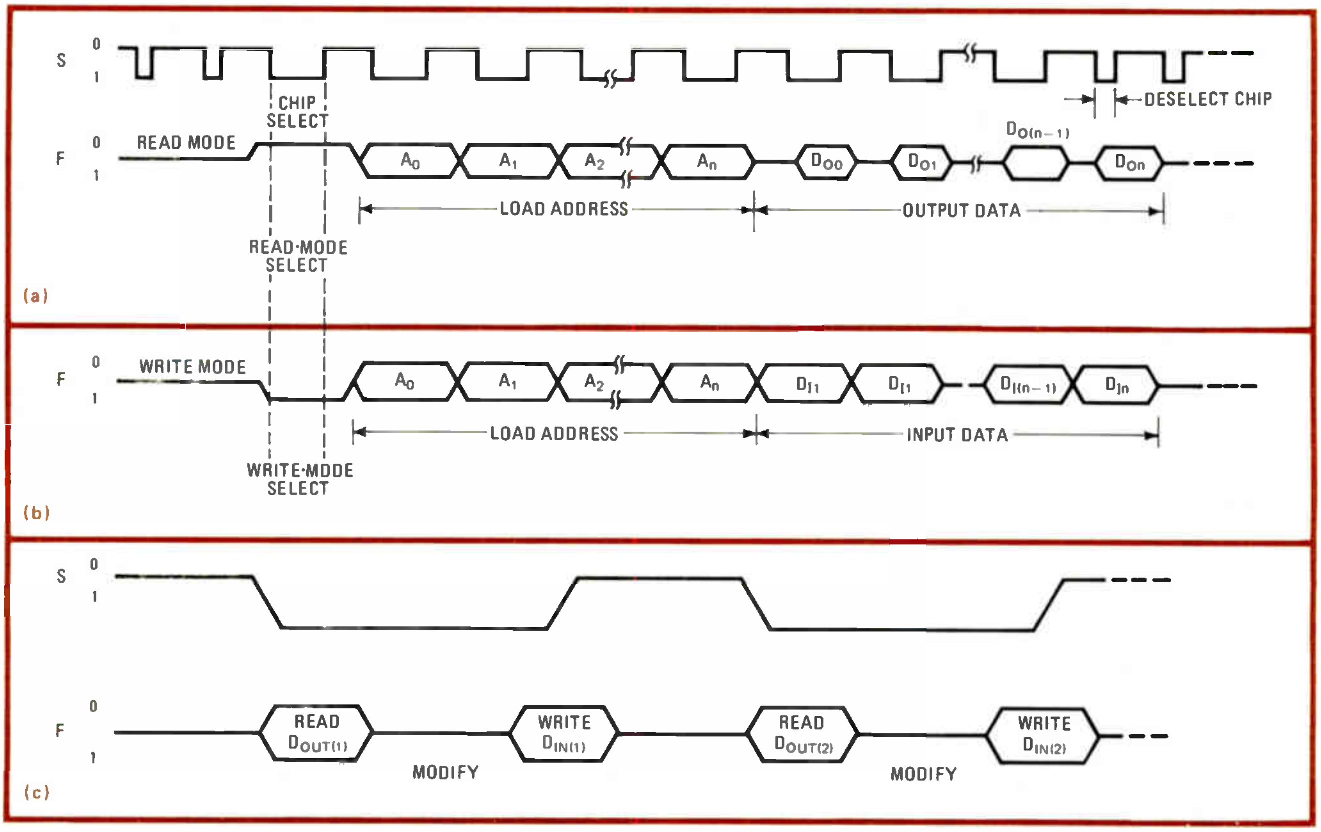
In addition, a means must be provided to select and deselect the chip with the same sync pulse. The most practical method of chip selection appears to be modulating the sync pulse width, although other methods, such as amplitude modulation, could be used for the same purpose.

A discriminator circuit would provide a chip-select (CS) signal only if the sync pulse width exceeded the delay through a string of inverters, for example; no CS signal would occur if a sync pulse width narrower than the delay were used. Consequently, when the device is only being refreshed and data is not being read in or out of the F pin, narrow sync pulses (approximately 60 nanoseconds in duration) can be applied. When the chip is selected, wide sync pulses (lasting approximately 160 ns) are applied.

Figure 3 is a block diagram of the memory device showing the added interface electronics that allows the chip to be packaged with only four pins. Interestingly, the memory array within the diagram could be made up just as readily with cells of any other type or density: CCDs, RAMs, ROMs, and so on.

The F pin's tasks

The F pin is arranged as for a three-state, bidirectional serial bus. The bus will be in a high-impedance state both when the memory is receiving data and when it is unselected. During data output, the bus will be under the control of the device. The input/output is controlled



4. Timing. Refresh applies a narrow pulse to S while F is in the high-impedance state. To read (a), a wide pulse is applied to S, and F is high. To write, F is driven low (b). In both cases, addresses and data flow serially through F. The scheme accommodates read-modify-write (c).

externally through the F pin by defining a standard format and by providing appropriate internal circuits for I/O control functions. Figure 4a shows a timing diagram of a proposed format. The chip requires three basic modes of operation: refresh, read, and write.

During the refresh mode, the sync pulse that is applied to the S pin is narrow and the chip is unselected. The device is thus being refreshed in synchronization with the pulse train. In this mode of operation, the F pin is in the high-impedance state. Just prior to the wide sync pulse, which selects the chip, the F pin is driven to high level to initiate a read operation. A series of address bits is then applied to the F pin in synchronization with each wide sync pulse and is clocked into a serial-to-parallel shift register; a second register counts the sync pulses while the address is loading.

Read and write

When the address register is full, the address is decoded and the chip initiates a readout of the data in the decoded address. Each wide sync pulse causes each successive data bit to be read out through the F pin. To terminate data readout and to deselect the chip, a narrow sync pulse is applied to the S pin. The lack of a wide chip-select pulse automatically deselects the chip and re-establishes the refresh mode. The write operation is similar except that a low level is presented to the F pin during chip-select and data is written to the memory through the F line (Fig. 4b).

Other formats and modes could be used to tailor a memory operation to particular functions. For example, a format that allows a read-modify-write operation is of special interest, since it would allow external error-correcting schemes to be applied to compensate for soft errors caused by alpha or cosmic radiation. In a system including that mode, the format could be so organized that, after address entry, each successive wide sync pulse would cause a bit to be read out to an external register through the F pin in synchronization with the falling edge of the pulse. The bit could be modified, if desired, during the low sync pulse state and the write mode initiated by the rising edge of the sync pulse.

The SF story

Figure 4c shows a timing diagram illustrating the relationships of the S and F signals for data input (D_{in}) and output (D_{out}) to execute a read-modify-write operation. Note that the device is under complete control of the user at all times. The user can set the sense strobe (just as in regular dynamic RAMs), then command the device to read out by applying a low-level signal on the sync line. The device will provide data output for a predetermined period of time described by the internal circuits, and the F bus is then relaxed to the high-impedance state so that the user may apply the data input. Assuming that normal refresh requirements are met, the user may hold the sync line low for a long enough period of time to correct errors in or modify data. The sync signal is driven high only after data has been entered on the F line.

Figure 5 is a block diagram of external circuitry—support chips for the four-pin memory—that can control

The impact of packaging on cost per bit

Proving that a reduction in the number of pins on a memory package has a significant impact on the system-level cost per bit, an interesting case study is available in the history of the 4-K dynamic RAM. The first parts (type 2107A) were housed in 22-pin packages, while a later design (the 2104A) took on a smaller 16-pin format. And, in fact, designing with the newer 16-pin package actually doubled system density over the earlier 22-pin type.

The first photograph shows a 32-kilobyte memory board comprising 80 2107A type 22-pin RAMs. The 11-by-14-inch board requires about 50 support chips in addition to the memories. The second photograph shows the same-sized board stuffed with 16-pin (type 2104A) RAMs. Since 160 of the smaller devices can now fit on the board, the memory storage doubles to 64-K bytes.

Interestingly, the doubled-density board also requires approximately 50 support circuits, even though it has twice as many RAMs as the 32-kilobyte board. A lesser production of support circuitry is required for two reasons: first, two sets of 6 address bits each are multiplexed through 6 RAM pins, rather than one set of 12 addresses through 12 pins; and second, the 16-pin RAM uses only TTL clock signals, whereas the 22-pin devices also require high-level (12-V) clocks—and the associated driver circuits as well.

The cost savings of using one board instead of two can be analyzed as follows:

$$C_1 = NC_R + M$$

where

M = total cost of one board, including all material, labor, and peripheral circuitry (which is assumed to remain constant per board), but less the cost of the RAM chips

C_R = unit cost of RAMs in the system

N = the number of RAM chips in the system.

The cost of a two-board system is:

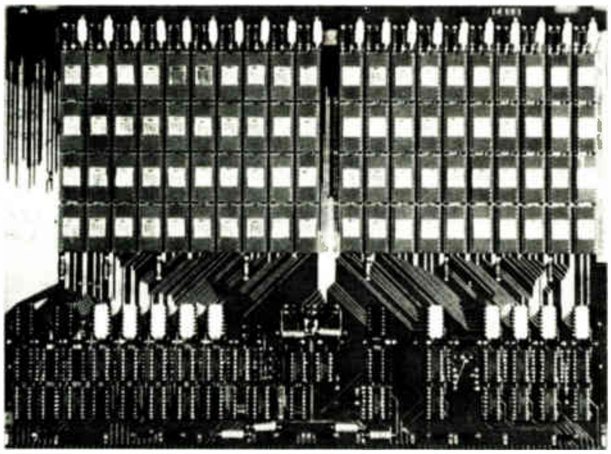
$$C_2 = NC_R + 2M$$

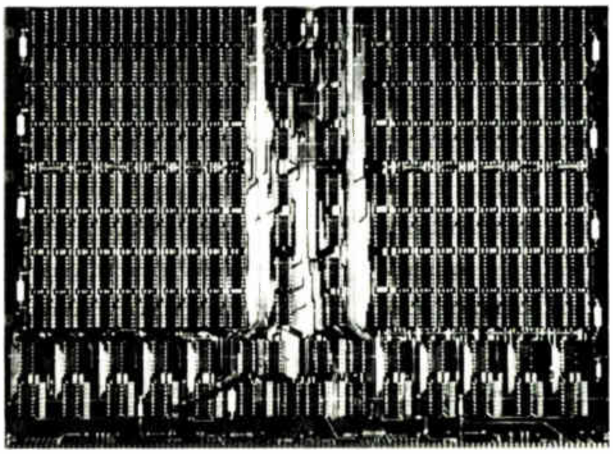
and the percentage savings P of a single-board system over a two-board system can be calculated as:

$$P = 100(C_2 - C_1)/C_2 = 100M/(NC_R + 2M)$$

which approaches 50% as the cost of RAMs drops.

A plot of that last equation for different RAM costs is shown in the first graph. A typical cost for the board (M) is \$300 to \$500, and 4-K dynamic RAMs (C_R) are about





the I/O function of the F bus. As shown, the circuit is relatively simple and inexpensive.

Once the decision is made to develop a four-pin memory that is serially interfaced, many organizational and functional opportunities become apparent since there is no longer any need to be concerned about pin limitations.

New opportunities

Historically, in order to migrate to a denser device and maintain the same pin count, it has been necessary to reassign the functions of some of the existing pins in order to expand the addressing capability. The four-pin device could be upgraded in bit density without any concern for the redesignation of pin functions. In fact, the same printed-circuit board memory array could be used from generation to generation for any device density as long as the timing and macrocontrol was provided from a separate board. Because of these advantages, intelligent memories could incorporate many added modes and features beyond conventional memories.

The serial interface to the four-pin device costs very little in reduced performance in block-oriented memory applications. For example, the efficiency loss due to the addition of a serial interface in using four pins for a 64-K CCD memory can be calculated with this equation:

$$\text{Efficiency loss} = 100(n + m)/N$$

where

n = the address bits required to select a loop

m = the instruction bits required to select the mode

N = is the number of data bits in a loop.

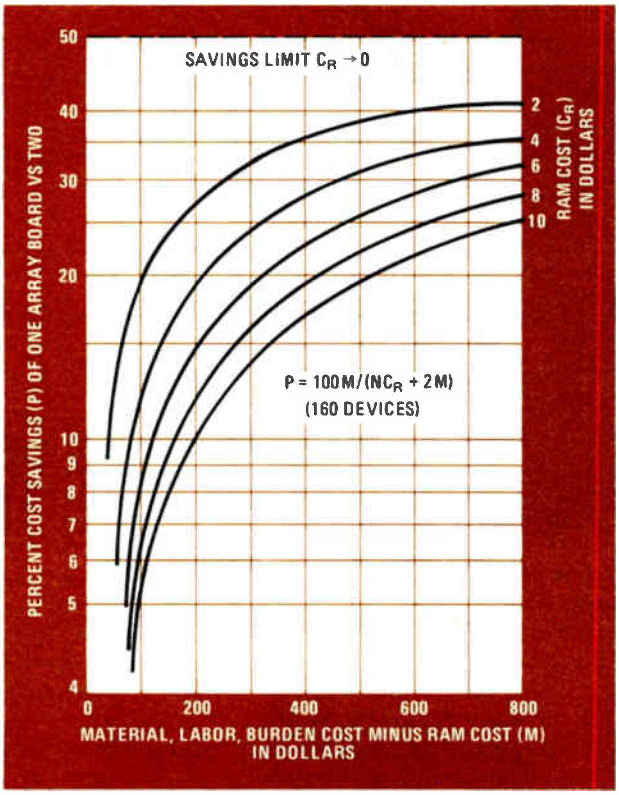
In a 64-K CCD, the organization of the device is 16 loops of 4,096 bits each. It requires n = 4 bits or clock cycles to select one of 16 loops and m = 1 bit or clock cycle for mode- or chip-select. The overhead performance loss is calculated as:

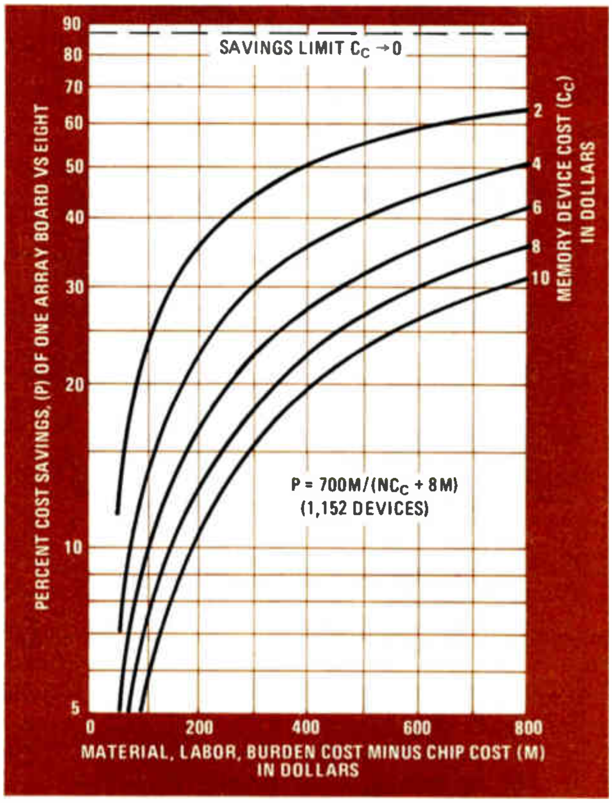
$$100(4 + 1)/4{,}096 = 0.122\%$$

Two additional modes of operation can be achieved for

$2 each. Using those figures, the savings in the single-board approach ranges from 33% to 38%. The saving is significant, and it does not even consider the additional economies in cabinet space, power supplies, and cooling.

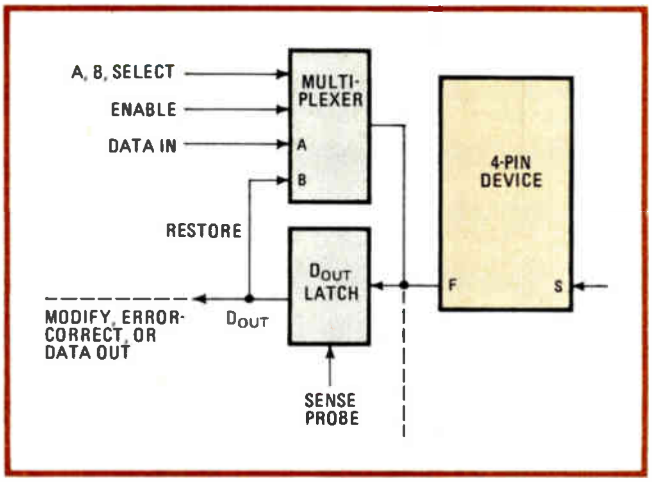
From the example, two assertions can be made: that for every pin on a memory package, there is something required to drive it, receive from it, power it, or cool it that costs money and/or space; and that the number of support circuits on a memory board is more directly related to the number of pins on the devices than to the number of devices. The same calculation can be carried out for an 8-megabyte system that uses 1,152 64-K memory devices. Whereas 16-pin, 64-K RAMS or CCDs would require eight boards, 4-pin versions would require only one board. The cost savings of one board over eight is depicted in the second graph. Note that for a per-board cost of $300 to $400 and a device cost of $2.00, the savings ranges from 45% to 55%—and again, that does not take into consideration the cost of cabinetry, power, and cooling reductions.



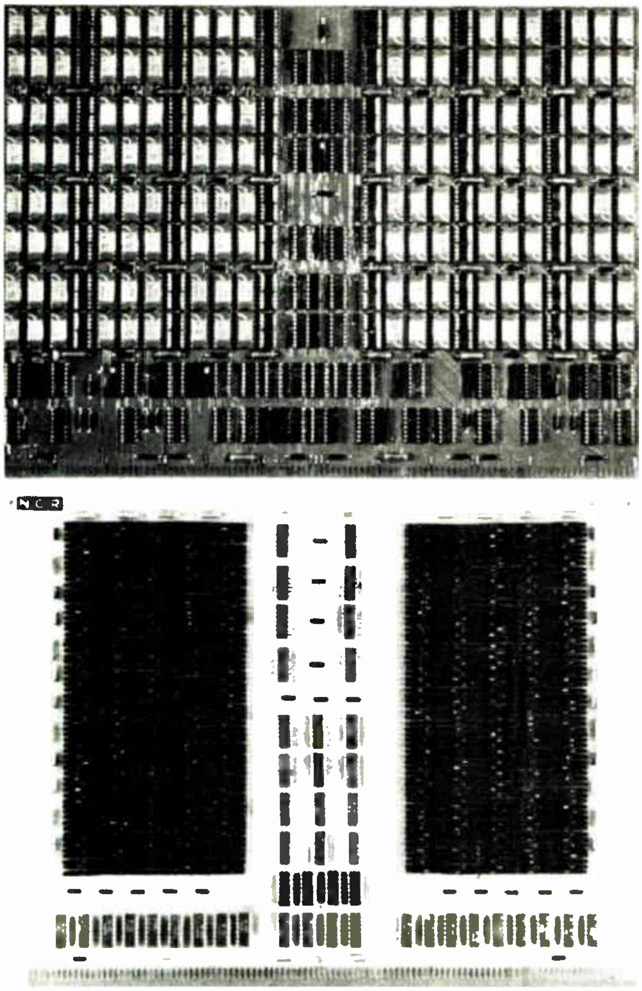


each bit added to the format at an efficiency loss of only 0.024% per added bit. Versatility can thus be added with minor losses in performance. For example, intelligence can be designed into the memory such that it operates in four modes with the following instruction coding: read, 00; write, 01; read-modify-write, 10; and page, 11. The 2-bit instruction coding could be sequenced either before or after the address bits. In this case, n = 4, m = 2, and the efficiency loss, including addressing, for a 64-K device is calculated as: $100(4+2)/4{,}096 = 0.146\%$. Semiconductor manufacturers could develop a variety of different four-pin devices, each with the same pinout, that could be used with the same printed-circuit board artwork. The circuit-board layout allows extremely high density yet is simple because it involves a basic X-Y matrix pattern of four conductors.

Studies were performed to compare the density, cost, and power of systems using currently available 16-pin 64-K CCDs with those using the proposed 4-pin 64-K CCDs. Figure 6 shows an array board that uses 144



5. External support. The support circuits to drive the F pins are relatively simple. A multiplexer allows either addresses or data to flow over an F-pin line, and a latch receives data flowing out of the line. Select signals would derive from a master control board.



6. Big improvement. The advantage of a 4-pin memory in a miniature single in-line package is immediately apparent from board densities. A 1-megabyte board (top) using 16-pin 64-K CCD chips is the same size as an 8-megabyte mockup of 4-pin 64-K CCDs (bottom).

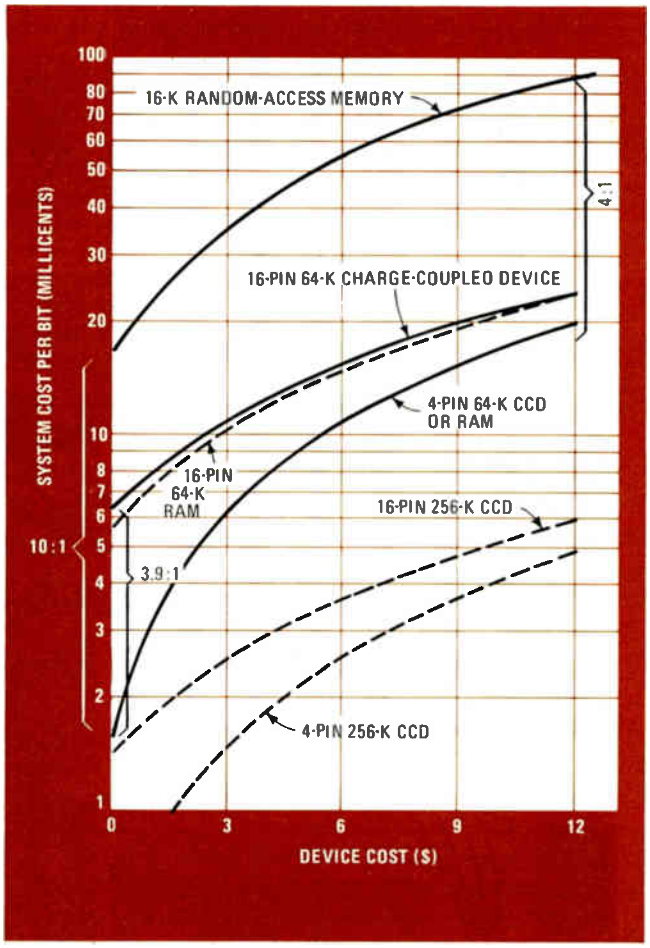
16-pin CCDs to develop a 1-megabyte memory subsystem. A mockup of a board of the same size using 4-pin CCD chips packs 1,152 SIPs to build an 8-megabyte memory subsystem, as shown in Fig. 6. The advantage of the 4-pin package is impressive and far-reaching, since building an equivalent 8-megabyte system with the 16-pin version would require considerable peripheral circuitry, packaging cabinetry and added power.

System-level size, cost, and power dissipation were compared, using two array boards of identical physical size as models. (Control electronics, cabinetry, and power supply costs were considered in the evaluation.) The results were found to be relatively insensitive to memory size, beyond one complete array board.

At the system level

Figure 7 shows the results of a comparison in system-level cost per bit for 16-pin and 4-pin CCDs and RAMs. Note that when a 4-pin, 256-K CCD reaches $3.00 per package, systems cost will be approximately 1.4 millicents per bit—or $140.00 per megabyte.

Another major savings of the 4-pin device is in power. Even though 100 milliwatts per CCD package is added for the 4-pin device in the calculation of system power (to cover the extra on-chip circuits), the system power dissipation is reduced by about 32%. The calculations indicate system-level power for the 16-pin device to be 29 watts per megabyte for a 64-K CCD and 20 W/megabyte for the 4-pin device. This significant power reduction is principally due to the elimination of the duplication of peripheral hardware and to the serializing of the address information.



7. Compare costs. The system-level cost per bit drops dramatically when a 4-pin memory package replaces standard 16-pin devices. The effect is especially important as the device cost falls—the figure could be as low as a few millicents per bit for a 4-pin 256-K device.

Space savings

The 4-pin device reduces the volume of the system by approximately 77%. With 64-K CCDs, the 4-pin device would require 31 cubic inches per megabyte, as against 133 in.^{3}/megabyte for the 16-pin device. The figures include interface electronics, 0.5 in.^{3}/W for power supplies, and 30% volume for cooling. Both volume and power per megabyte would shrink by approximately a factor of four if 256-K CCDs were used in place of the 64-K CCDs. Moreover, power consumption could be as low as 5 W/megabyte using a 4-pin 256-K CCD, and a system volume would be on the order of 8 in.^{3}/megabyte—including power supplies. Finally, significant further power savings would result when power supply voltages were reduced from 12 volts. □

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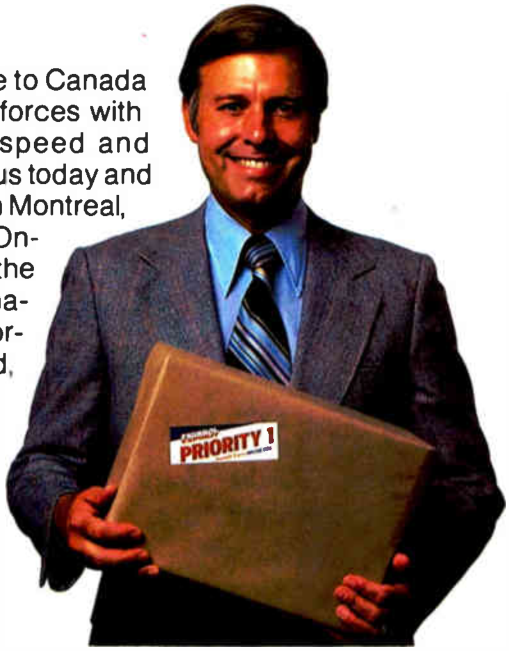

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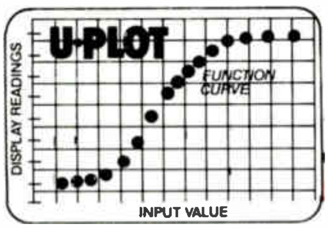

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Reducing the dropout voltage of programmable regulators

by Carlo Venditti
The Charles Stark Draper Laboratory Inc., Cambridge, Mass.

A programmable regulator's dropout voltage—the minimum allowable potential between its input (V_{in}) and output (V_{out})—can be improved by adding an external output stage and negative feedback. The resulting regulated output voltage (E_{out}) not only approaches V_{in} more closely, but the the current-drive capability is also better, thanks to the outboard power-transistor stage.

The design technique used to achieve this improved performance is described here for Fairchild's popular μA78MG regulator, which has a nominal dropout voltage of 3.0 volts. As shown in the figure, a change in V_{in} causes V_{out} to increase temporarily. The corresponding increase at E_{out} that is applied to the control input of the μA78 forces V_{out} lower, toward the value it had initially. If the resistor network R_1 to R_3 is optimized, E_{out} can be brought to within 1.5 V of V_{in}.

Consider the case where the output voltage E_{out} is to be kept at 12.5 V ±50 mV for a V_{in} ranging from 14 to 15.5 V. When V_{in} is at 14, V_{out} cannot be above 11, owing to the dropout voltage of the regulator. Thus with an output voltage of 12.5, the voltage at the base of Q_1 is 13.1 (0.6 V higher).

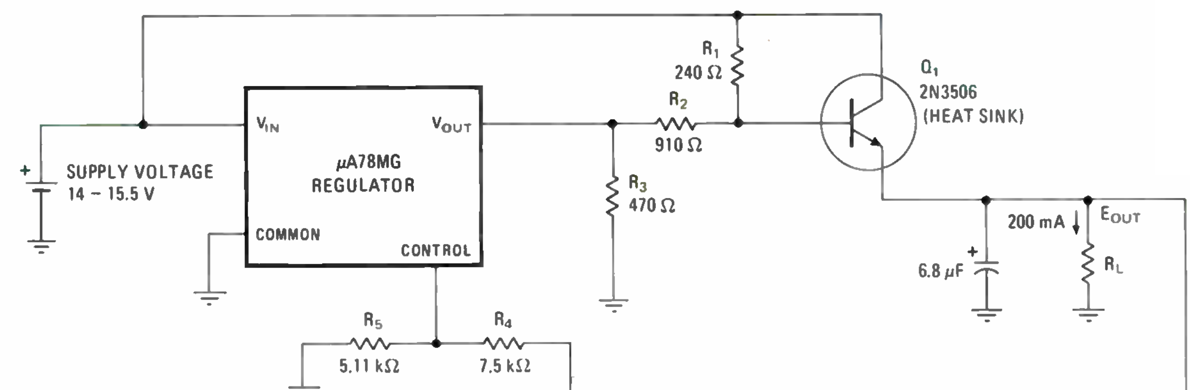
Now R_1 can be selected to pass a given value of transistor base current, I_b, of say, 1.2 milliamperes, and a current through R_2 of perhaps twice this value (2.4 mA), plus a small amount to account for variations in I_b. Thus $R_1 = (14-13.1)\text{V}/3.75\ \text{mA} = 240\ \Omega$, and $R_2 = (13.1-11)\text{V}/2.4\ \text{mA} = 910\ \Omega$.

The next condition to be addressed is the case where V_{in} assumes a value of 15.5 V, so that R_3 may be determined. Because V_{out} ultimately decreases with an increase in V_{in}, V_{out} should be made to move to its minimum value so that the maximum dynamic range of the circuit is realized. From the data sheet of the μA78, $V_{out(min)} = 5.0$ V. Note that changes in V_{out} are scaled by the R_2/R_1 ratio, and these resistors ensure that a change of $910/240 = 3.8$ V occurs for every 1-V increase in V_{in}.

Thus the current through R_2 at this time will be $(13.1-5.0)/910 = 8.8$ mA, and assuming the minimum (quiescent) current of the regulator is 2 mA, the current through R_3 is $(8.8+2.0) = 10.8$ mA. Therefore $R_3 = 5/10.8 = 470\ \Omega$. The table summarizes the actual dynamic performance of the regulator. Note the apparent dropout voltage of the regulator has been reduced to $14.0-12.482 \approx 1.5$ V when V_{in} is at its minimum.

The junction temperature of the on-chip power transistor is $T_j = \theta_{JA}P_T + T_A$, where θ_{JA} is the junction to ambient thermal resistance (80 Ω, see data sheets) and T_A is the ambient temperature. Thus, assuming $T_A = 25°C$, $T_j = 35°C$, well below the 125°C thermal shutdown temperature of the μA78.

A check on the chip's temperature will confirm that the regulator's thermal shutdown point has not been reached. The temperature reaches a maximum when $V_{in} = 14.0$. At this voltage, the regulator's output current is



V_{IN}	V_{OUT}	E_{OUT}
15.5	5.19	12.502
15.0	7.20	12.495
14.5	9.04	12.489
14.0	10.90	12.482

Closer. Outboard power transistor stage, and resistor pad R_1–R_3 set E_{out} to within a few volts of V_{in}, so that $(E_{out} - V_{in})$ is below μA78's dropout value. Q_1 also provides increased current capacity. Table summarizes dynamic range attained for example using technique discussed in text.

20.8 mA, and the output power is 20.8 (14 − 11) = 62.5 mW. The quiescent current is 4 mA (see data sheets), and the quiescent power drain becomes 4(14 V) = 56 mW. As a consequence of these figures, the total output becomes P_T = 118 mW. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

Doubling the character rate handled by CRT controllers

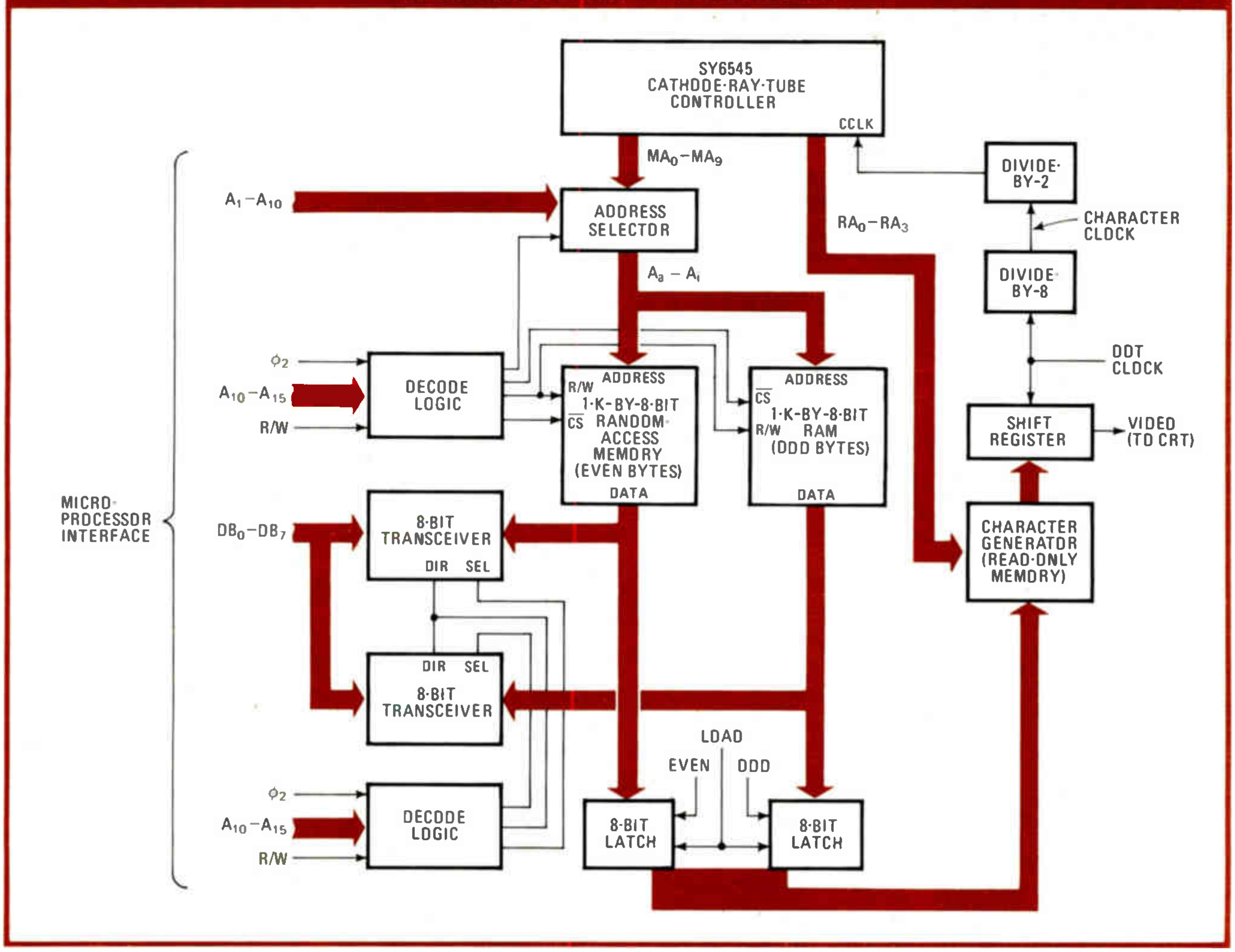
by Conrad J. Boisvert
Synertek Inc., Santa Clara, Calif.

Controllers that transfer display information from a microprocessor to a cathode-ray tube can be made to operate at effective character rates in excess of the normal maximum value. Specifically, by accessing 2 bytes of data per fetch and implementing logic to apply the characters to the display one at a time, the effective character rate can be doubled. The technique is applied here to the Synertek SY6545 chip, although the principle can be extended to most of the popular controllers.

The system architecture necessary for doubling the effective character rate is shown in the block diagram. The memory scheme gives the microprocessor overriding priority in selecting the video-display memory. Other configurations could be implemented, but this is the simplest and focuses attention on the more significant aspects of the method. Also note that the video-display memory is assumed to be 8 bits wide (ASCII coding requires only 7 bits) and that 8 horizontal bits define one character.

A key circuit point is that the SY6545 address lines, MA_0–MA_9, are routed through the address selector block to memory addresses A_a–A_i of both the odd and even memory blocks. In this way, as the SY6545 steps through its states, the two memories are accessed simultaneously. Memory addresses A_1–A_{10}, on the other hand, are routed through A_a–A_i, with the memory address line, A_0, selecting either the even or odd memory, but not

BLOCK DIAGRAM OF CRT CONTROLLER SYSTEM



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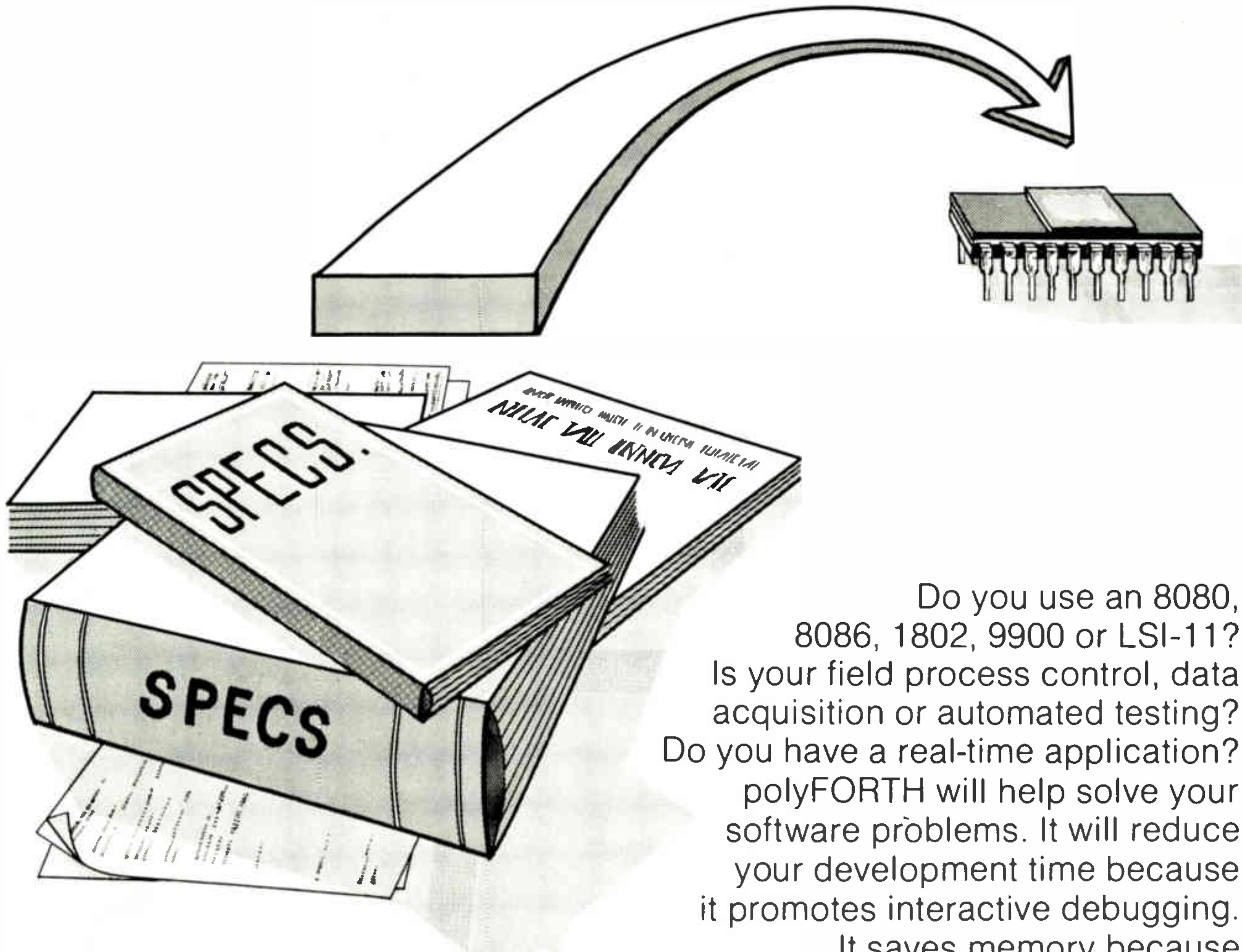

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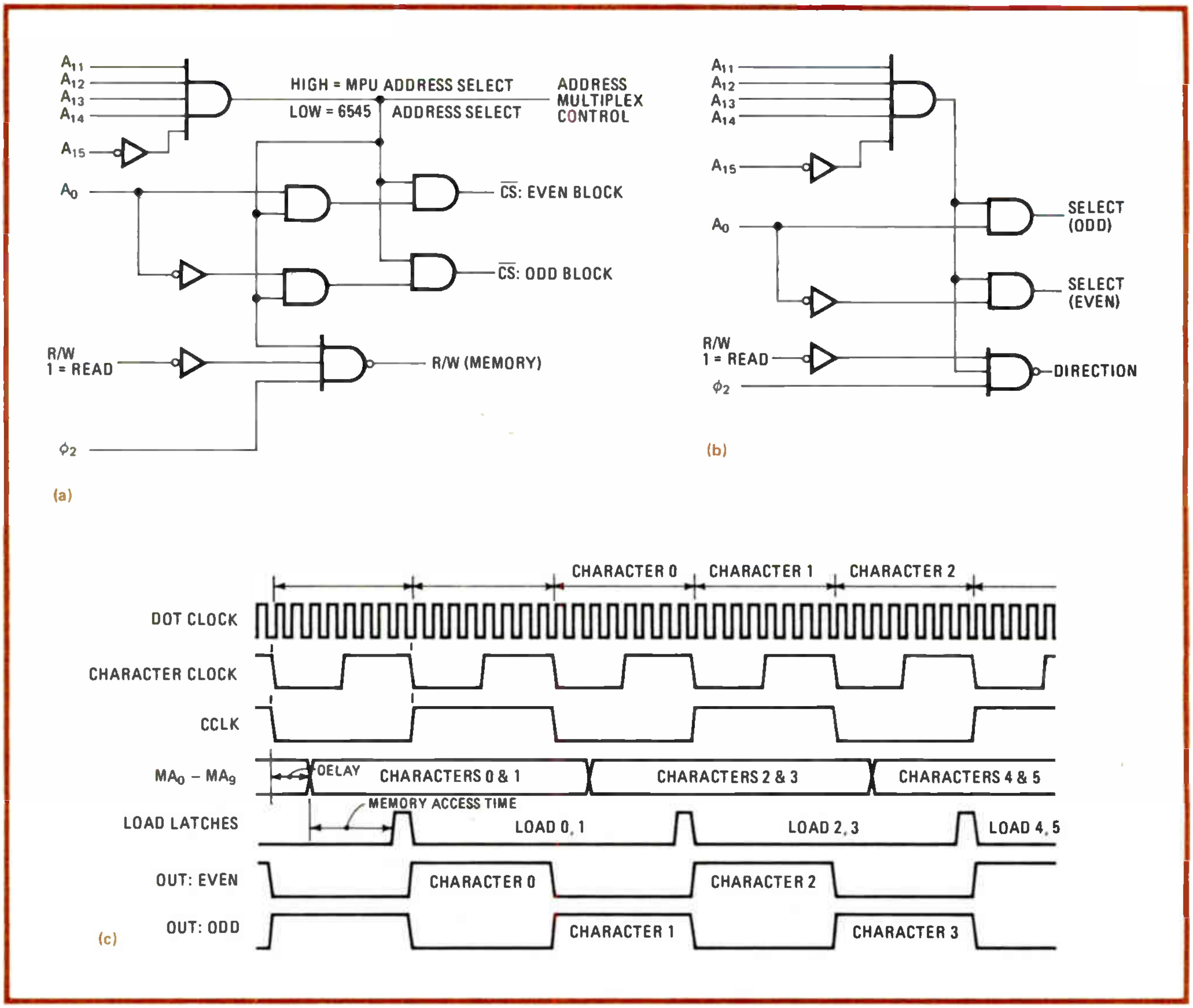

Hardware. Logic for increasing character rate handled by CRT controllers uses readily available gates. Circuitry for memory control (a) and data transceivers (b) adapts system for two-character fetch and display. Timing diagram (c) details system operation.

both. Thus, a dual-port memory is configured, accessing the data memory as a 1-K-by-16-bit block, and the microprocessor as a 2-K-by-8-bit block.

The logic required to control the memory is shown in Fig. 2a. The chip-select lines $\overline{CS}$ must always be low if the microprocessor is not addressing memory. A_{11}–A_{15} correspond to the decoded memory-map location of the addressed memory, with A_0 used to select either the odd or the even block. Under these conditions, the address selector (Fig. 1) is activated. The R/W signal may then be applied to the memories.

Similar logic for controlling the data-bus transceivers is shown in Fig. 2b. Here, the transceiver's odd or even select outputs are energized after inputs A_{11}–A_{15} have settled. The transceivers are deactivated and the microprocessor data bus isolated from the video display if A_{11}–A_{15} do not match the decode pattern.

The timing diagram clarifies the system operation (Fig. 2c). Note the character clock, which normally drives the SY6545's CCLK pin directly, is divided by 2 because two characters must be fetched per cycle.

The horizontal registers associated with the character total, the display, the sync position, and the sync width will be affected by the aforementioned modification, and steps must be taken to alter the way in which they are programmed. In any case, the value programmed must be half the value that is normally entered. For example, to achieve a display of 80 horizontal characters per line, the number 40 must be programmed into the horizontal display register.

Finally, external logic must be incorporated into the system to achieve a cursor output signal that will be active for each character handled. This function may be implemented with three NAND gates.

The SY6545's cursor output is first combined at one NAND gate with the even latch-select signal of Fig. 2b and the negated output of the PAO port signal of the SY6520 peripheral interface (not shown). PAO, the cursor signal, and the odd latch-select signal are combined at the other NAND gate. Both gate outputs are joined at the input of the third (two-input) NAND, whose output represents the modified cursor signal. □

Engineer's newsletter

NBS catalog lists calibration labs and capabilities

Engineers who must concern themselves with the calibration and accuracy of test instruments will welcome the new **Catalog of Federal Metrology and Calibration Capabilities published by the National Bureau of Standards.** The catalog outlines the particular capabilities of the measurement-standards laboratories of the Departments of Defense, Energy, and Transportation and the National Aeronautics and Space Administration. In addition to a cross-index by agency and geographical location, it provides the names and telephone numbers of information contacts.

Copies of NBS Special Publication 546 are available from the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. The cost is $2.50. Request stock number 003-003-02082-6.

LED tape monitor for KIM-1 checks data flow

Even though the popular KIM-1 microprocessor has a built-in tape-recorder interface, it lacks a tape-reading monitor; thus, the entire program must be read before it can be determined if it has been properly loaded. Fortunately, however, **a simple monitor can be built for immediate detection of the two most common types of data-transfer problems encountered with the KIM-1**—improper signal levels or a bad interconnecting cable between the interface and the microprocessor. Cass Lewart of System Development Corp., Eatontown, N. J., makes such a device by placing a light-emitting diode in series with a current-limiting 1-kΩ resistor and connecting the combination between the output of the tape reader's phase-locked-loop (pin E-X of the KIM-1 board) and ground. A lit LED indicates that data signals are being received at the KIM-1.

McGraw-Hill will offer courses in all phases of data communications

Data Communications magazine will offer courses in all phases of data communications beginning early in 1980, to fulfill the growing need for employee training and practice in this vital area. The first is a basic, 70-hour course that will begin on Jan. 7 at McGraw-Hill headquarters in New York City and will last two weeks. **It is geared to the needs of technicians, engineers, and managers,** as well as representatives of vendors of data-communications equipment. Among the topics covered will be: regulatory agencies; functional network subsystem relationships; central hardware considerations; and network diagnostics, monitoring, planning and design. All participants will receive a text prepared specifically for the institute by a leading data communications specialist. Tuition is $1,100. For further information, contact the Data Communications Institute, McGraw-Hill Publications Co., 1221 Avenue of the Americas, New York, N. Y. 10020; phone (212) 997-6050.

CIES extends deadlines for Fulbright applicants

The Council for International Exchange of Scholars has waived some deadlines for the American applications it is reviewing for the 1980–81 program year in order to make recommendations to the Board of Foreign Scholarships and to overseas Fulbright agencies. It will accept additional applications for a number of positions—most notably **teaching science and engineering in Africa, Asia, Eastern Europe, and Latin America.** Applicants must be U. S. citizens and have appropriate educational and professional qualifications. Further information is available from the Council for International Exchange of Scholars, Dept. N, 11 Dupont Circle, Washington, D. C. 20036.

-Vincent Biancomano

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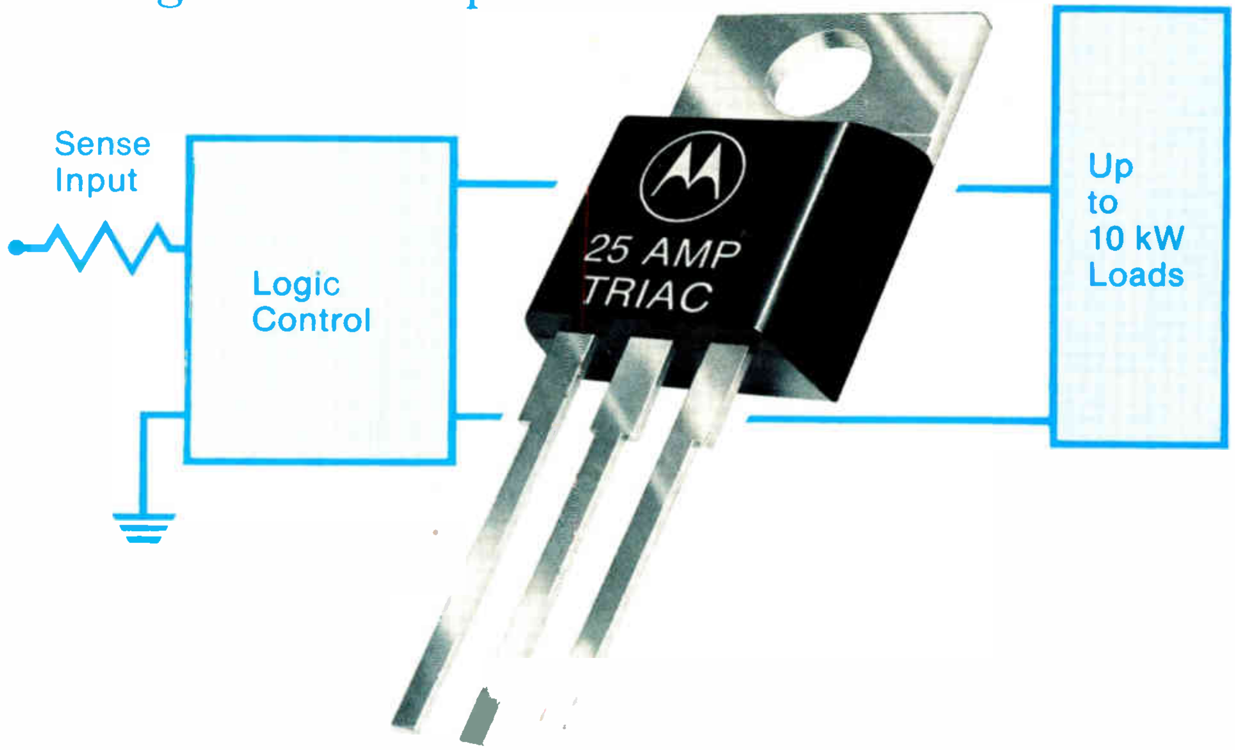

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Call our authorized distributor or contact Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for complete data on the MAC223/223A Triac.

Motorola SuperPower discretes like these will always be in control of the world's

Innovative systems
through silicon.

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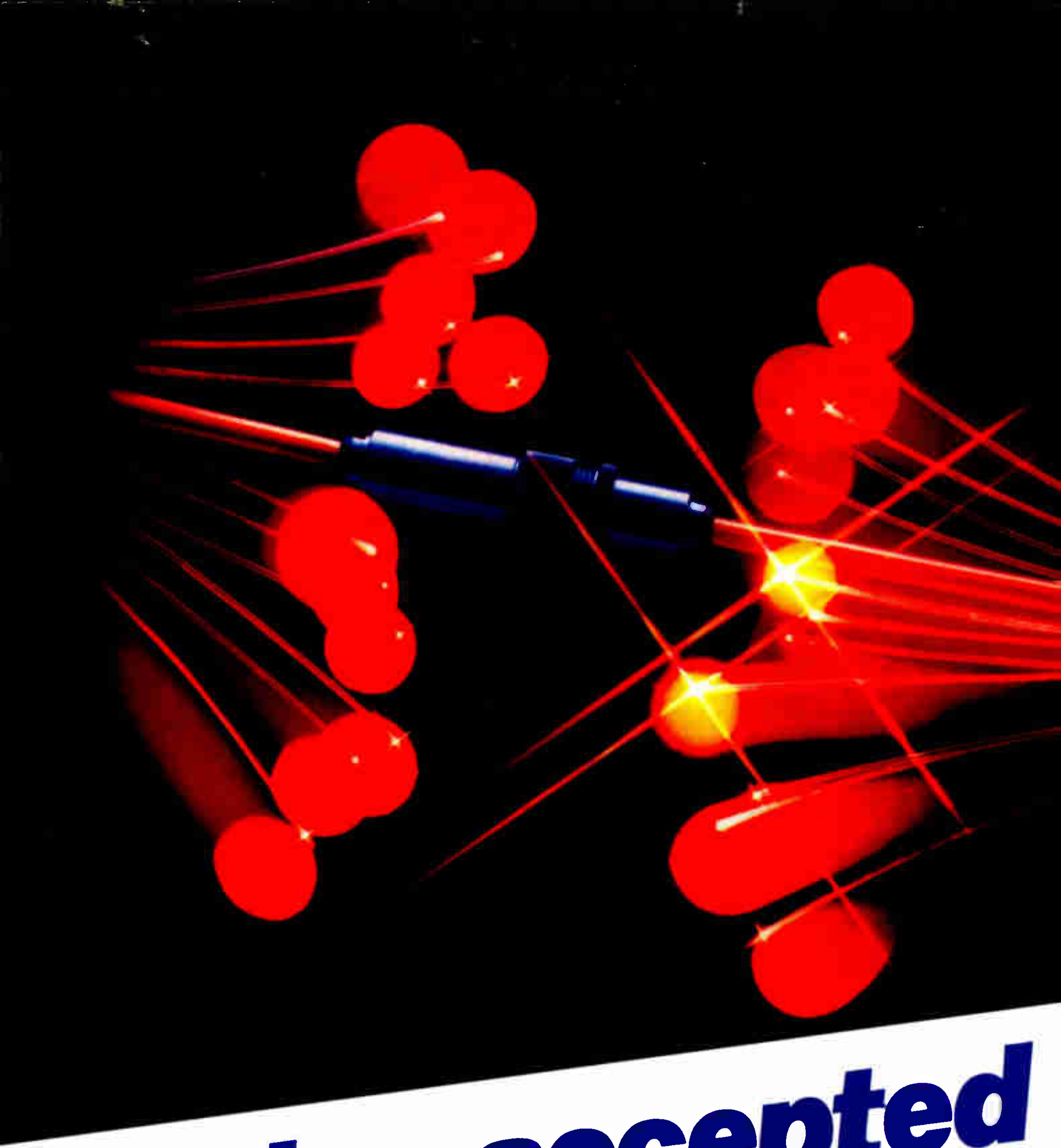


When it comes to connector innovation, TRW Cinch picks up the gauntlet! Take our newest single-fiber optic connector, OPTALIGN,* for example.

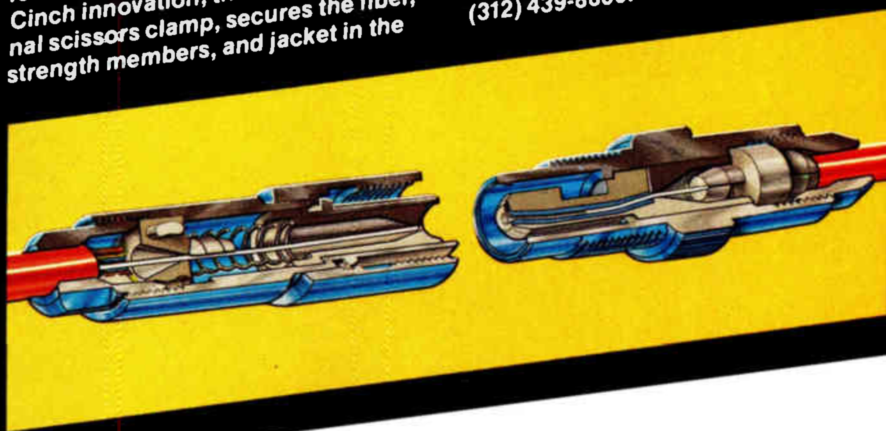
A patented fiber alignment system restricts light losses to less than 1 db. We've developed an alignment element that's compatible with most commercially available fibers. The element is based on a four-rod glass array that is clean, inert and stable, and mates fibers in a manner that yields excellent shock and vibration immunity.

This glass array does not require precision tolerances, yet assures ultra-precise fiber alignment to achieve low light losses. This means lower costs and fast, precise connections without using time-consuming epoxies. In fact, OPTALIGN can be field-assembled in less than four minutes. Another TRW Cinch innovation, the exclusive internal scissors clamp, secures the fiber, strength members, and jacket in the lightweight aluminum OPTALIGN housing.

Compact OPTALIGN plugs and receptacles are ideal for computers, CATV, telecommunications, medical, instrumentation and military applications. Dimensions are ⅝" diameter x 1½" in length.

If you require a miniature single-fiber optic coupling, we've got that too. It's our new Light Line* SMA Connector, another innovative, high-value offering from TRW Cinch.

These are just two new products from the new Cinch. We'll think "Innovation" when it comes to meeting your connector challenges, too! Call your TRW Electronic Components Sales Office... listed in EEM. TRW Cinch Connectors, A Division of TRW Inc., 1501 Morse Avenue, Elk Grove Village, IL 60007. (312) 439-8800.



the challenge innovation.

TRW CINCH CONNECTORS

See us at Midcon, Booth No. 1520 thru 1528

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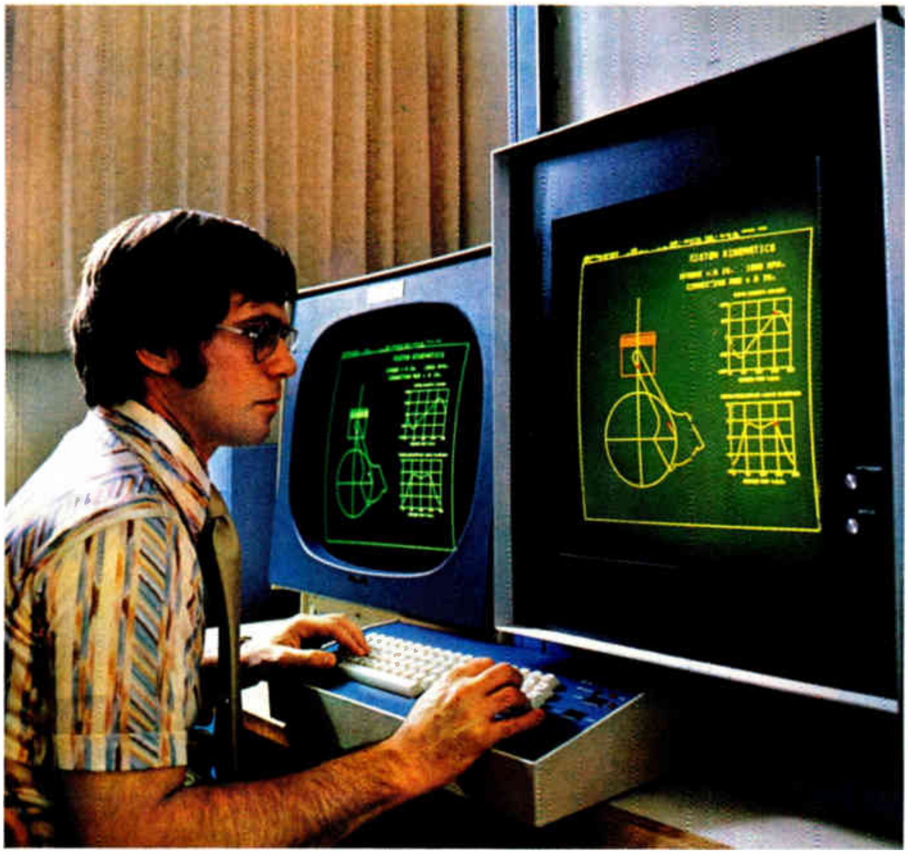
Control Data: Committed to

Control Data people, systems and services are helping manufacturers prepare for the '80's.



Exemplifying what state-of-the-art CAD technology can do for manufacturers, Chrysler Corporation Chief Engineer Robert Brauburger reports dramatic gains in the speed and efficiency of their design process. Above: a Chrysler engineer uses a color graphics terminal to analyze piston performance. Below: the control room at Chrysler's Technical Computing Center, where an operator monitors four interconnected Control Data® CYBER 170 systems.

American manufacturers are challenged by spiraling inflation and increasing competition. They must keep pace with productivity gains abroad to maintain market share and protect the jobs of their employees.

In the U.S., the annual growth in productivity over the last ten years has been half of what it was over the previous two decades. Many manufacturers are turning to computer-based technology to reverse this trend.

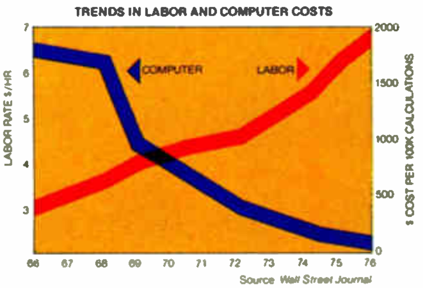
Over half the FORTUNE 500 are using our products and services.

Large scale Control Data computers are recognized for their outstanding ability to perform complex scientific and engineering computations rapidly and with great accuracy. Our systems are installed in major manufacturing companies around the world. And Control Data's recently announced CYBER 170 Series 700 continues in this tradition by offering increased performance at reduced cost.

Control Data also offers manufacturers a wide range of data services through some of the world's foremost data processing networks.

Through our CYBERNET® Services we provide the benefits derived from processing on Control Data computer systems, along with sophisticated application programs

the Manufacturing Industry



for structural, mechanical and electronic design and analysis.

Through our Service Bureau Company, we provide a whole range of services for business planning, analysis and control, plus a complete interactive system for material requirements planning, production control and management information.

In addition, many companies are training their personnel with our PLATO® computer-based educational service.

A new automated design and drafting system

One of the most important ways Control Data is helping manufacturers make better use of human resources is through computer-aided design (CAD).

Recently, we announced AD-2000,* an automated design and drafting system which speeds the design process by eliminating many of the tedious, time-consuming tasks previously performed by hand. AD-2000 offers practical and up-to-date design and drafting capabilities while providing a link to numerical control and other computer-aided manufacturing (CAM) functions.

Coming from Control Data—a fully integrated CAD/CAM system

The critical link between CAD and CAM is the effective control and flow of data among respective systems. Control Data has the products and expertise to allow the interface of design, analysis and manufacturing applications.

And when our new CAD/CAM technology is available, manufacturers will be able to go from a design on a CRT screen to a finished part—all with greater productivity and better use of resources than offered by the present technology.

Control Data is committed to helping industry bridge the gap between the old and new technologies. Through our Manufacturing Consulting Services organization we are helping manufacturers plan and implement their CAD/CAM strategies through training, consultation and technical assistance. And through Commercial Credit Company, an important part of Control Data, we provide manufacturers with a whole range of financial services, including capital equipment financing.

Boeing, a long time user of Control Data computers, recently installed two CYBER 175's in a CAD/CAM center to assist in the design of its new generation of passenger aircraft.

Systems. Services. Solutions. Measures of Control Data's commitment to the manufacturing industry.

For further information, write: Control Data Corporation, Manufacturing Industry Marketing, HQW09F, Box 0 Minneapolis, MN 55440.

CONTROL DATA CORPORATION

More than a computer company

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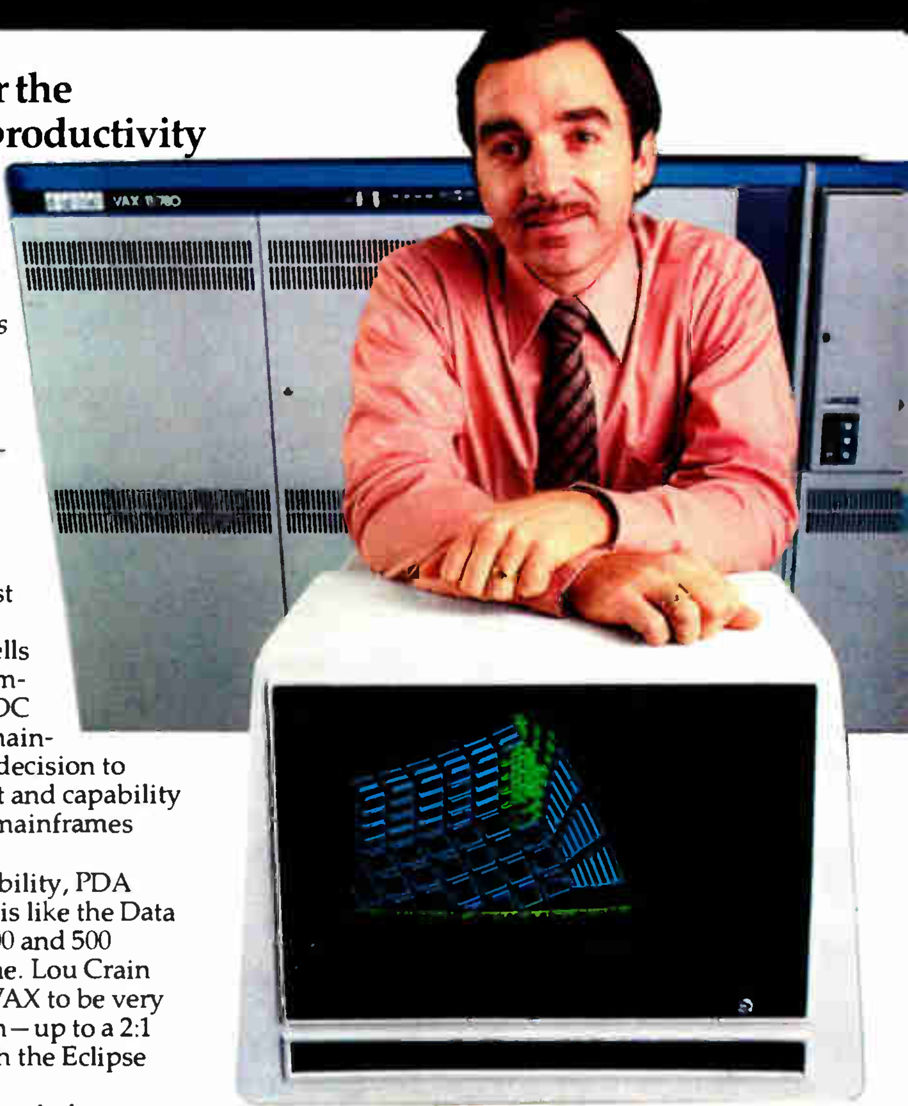
VAX Performance. Ask any user.



"VAX simply ran over the competition. In cost/productivity ratios, nothing even came close."

Lou Crain, Mgr. of Software Products
Prototype Development Associates
Santa Ana, California

PDA is an employee-owned engineering concern whose business ranges from fundamental research in structural analysis to the manufacture of critical aerospace components.

The VAX-11/780 is PDA's first in-house computer. Lou Crain, Manager of Software Products, tells us, "We've been doing all our computing through utilities using CDC 6600, Cyber 74 and Univac 1108 mainframes. The key elements in our decision to acquire the VAX-11/780 were cost and capability — compared to service bureaus, mainframes and competitive minis."

From the standpoint of capability, PDA considered traditional superminis like the Data General Eclipse and the Prime 400 and 500 series, plus a used 1108 mainframe. Lou Crain says, "Our benchmark showed VAX to be very powerful against the competition — up to a 2:1 performance advantage over both the Eclipse and the 1108."

"After installation," Crain concludes, "VAX has lived up to our expectations and has performed impressively. It's resulted in better products for our customers, as well as improved cost-effectiveness. Having our own interactive capability in-house has meant an increase in engineering productivity of up to 300%."

"VAX turns out to be twice the machine for the same amount of money."

Roger Vossler,
Section Manager and Systems Engineer
TRW Defense and Space Systems Group
Redondo Beach, California

Sensor data processing and distributed processing systems in support of real-time embedded applications are among the specialties of TRW's Defense and Space Systems Group.

To find the right computer, TRW continues to evaluate numerous machines—including Digital's VAX-11/780. They've also conducted numerous FORTRAN and PASCAL benchmarks.

In every test, VAX stands out as a clear winner.

Roger Vossler, Section Manager and Systems Engineer, says, "VAX is one of the best implementations we've seen of a successful integrated hardware and software system."

Since TRW's sensor data processing applications require enormous memories—over a million bytes to store a single image, for example—VAX's true 32-bit address space is vitally important. In addition, says Vossler, "VAX's I/O bandwidth capabilities are extremely important for effectively moving large quantities of real-time data at very high data rates."

Because TRW already had an investment in Digital technology, Vossler is particularly impressed with the relative ease of moving PDP-11 series programs onto VAX.

"But," says Vossler, "Even if I were starting all over again—without our Digital experience—I would still pick VAX, on the basis of its architecture, both hardware and software, and its impressive performance."

"Implementation was faster on VAX than on 25 other machines."

Brian Ford, Director
Numerical Algorithms Group
Oxford, England/
Downers Grove, Illinois

The Numerical Algorithms Group develops and maintains mathematical and statistical software libraries for customers in industry, science and academia.

Before VAX, NAG had implemented their complex Mark 6 Library on 25 major machines, including the Burroughs 6700, CDC 7600, Univac 1100, and the IBM 370. The average implementation time was 13 man-weeks.

VAX took five.

In Dr. Ford's words, "A successful implementation requires the correct functioning of the 345 library routines to a prescribed accuracy and efficiency in execution of NAG's suite of 620 test programs. Whilst the activity is a significant examination of a machine's conformity to the ANSI standard of the FORTRAN compiler, its main technical features are file creation, file comparison, file manipulation and file maintenance."

And implementation performance was just the start. Dr. Ford comments on VAX's impressive record of reliability after the program was up and running: "No problems were encountered in the VAX/VMS software even though approximately 3000 files were being handled. The operational availability time for the machine was close to 100%, an outstanding statistic for new hardware and a new operating system.

"VAX," Dr. Ford concludes, "is an implementor's dream."

Digital's VAX-11/780 has re-defined the level of performance you can expect from computers in its price range.

If your application requires large number crunching capability, high floating point accuracy, or lots of high-speed real-time calculations, there is simply no better system.

But don't take our word for it. Send for our new brochure. And listen to our customers.

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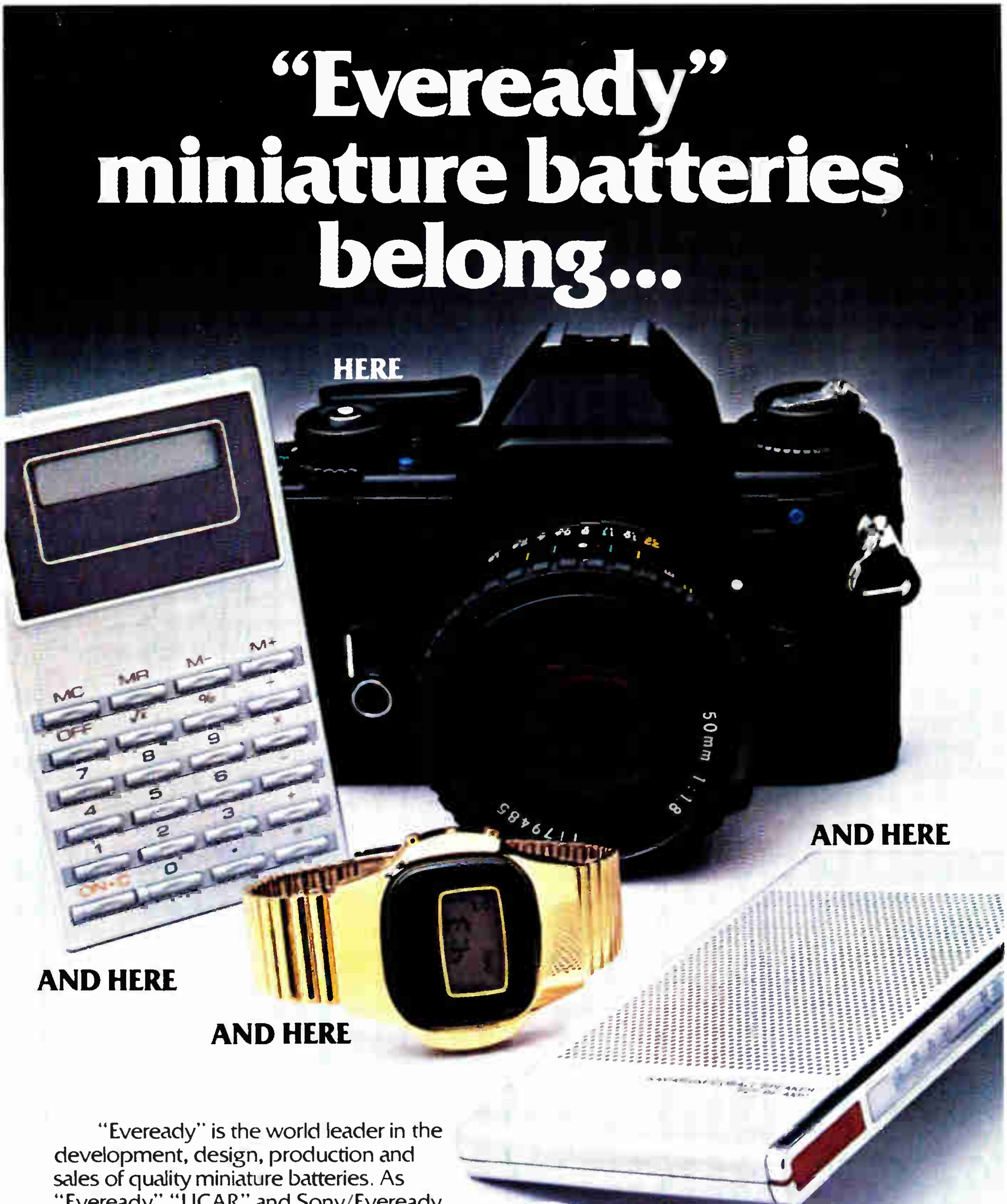

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Test generator costs less, does more

Second-generation automatic system for functional testers uses four algorithms and bidirectional fault propagation for high efficiency

by Bruce LeBoss, West Coast Editor, Computers & Instruments

Automatic test generation is probably the most advanced technique developed for checking the functional performance of complex circuitry. And although ATG was a big step forward, it has been more exciting in concept than in actual performance; currently available systems require considerable manual guidance and intervention from product designers or test engineers. What's more, user acceptance of functional testers has been slower than anticipated because of the high degree of programming involved and the machine's inability to generate comprehensive test programs automatically.

Computer Automation Inc. plans to change all that with the introduction of second-generation logic simulation system at the 10th Annual Cherry Hill (N. J.) Test Symposium later this month. Called the Capable 4814 ATG-II, this system not only offers truly automatic generation of test programs, but will be priced at about one-third the cost of first-generation commercial systems, according to Edward E. Erny, manager of product management at CA's Industrial Products division, Irvine, Calif.

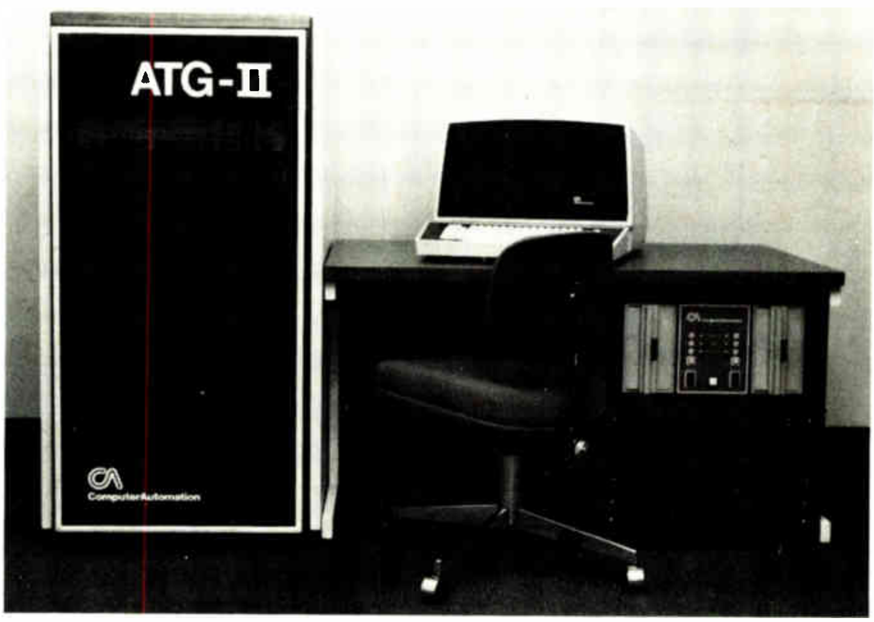
The 4814 was developed on the premise that the single-algorithm approach used throughout the industry today has been insufficient, states Erny. "By equipping a system with multiple algorithms, it would be possible to do a better job of finding faults with the system. Algorithms could be tuned individually to look for various types of faults." Also, he notes, engineering involvement in programming considerations would be reduced by an order of magnitude, and in most cases, the system operation would be truly automatic.

The advances contained in the 4814 ATG-II algorithms, Erny says, "overcome most, if not all, of the drawbacks associated with previous levels of ATG algorithms." The system can be assigned to search overnight for faults in a software model of a complex circuit board without designer or test-engineer inputs, he adds, and will continually analyze sections of the model in ever greater detail to uncover a higher percentage of faults than was possible before.

The output of the new system is generated specifically for CA's Capable family of functional automatic test systems, which run the ATG-II output programs and then search for faults on the actual circuit boards in production. The system will be available either as a stand-alone configuration with a base price of $110,000 or as an add-on to existing Capable systems for approximately $50,000, depending on which version of the Capable line a user has.

The 4814 incorporates two proprietary techniques in testing methodology, according to Erny. Previous programs for automatically generating test patterns used a single algorithm to select a fault pattern from a table of undetected faults. The algorithm then determined the propagation path, calculated the stimulus for that path, and generated the stimulus to drive the fault out.

By contrast, the ATG-II is based on four algorithms, with the system automatically switching among them for maximum fault detection: "90% or better," Erny claims. The system optimizes the computer's time by working on easy faults first and then proceeding to the more difficult ones. A comprehensive set of checks



and balances prevents the system from spending all its time on one or even a few difficult faults until all the easier ones are resolved.

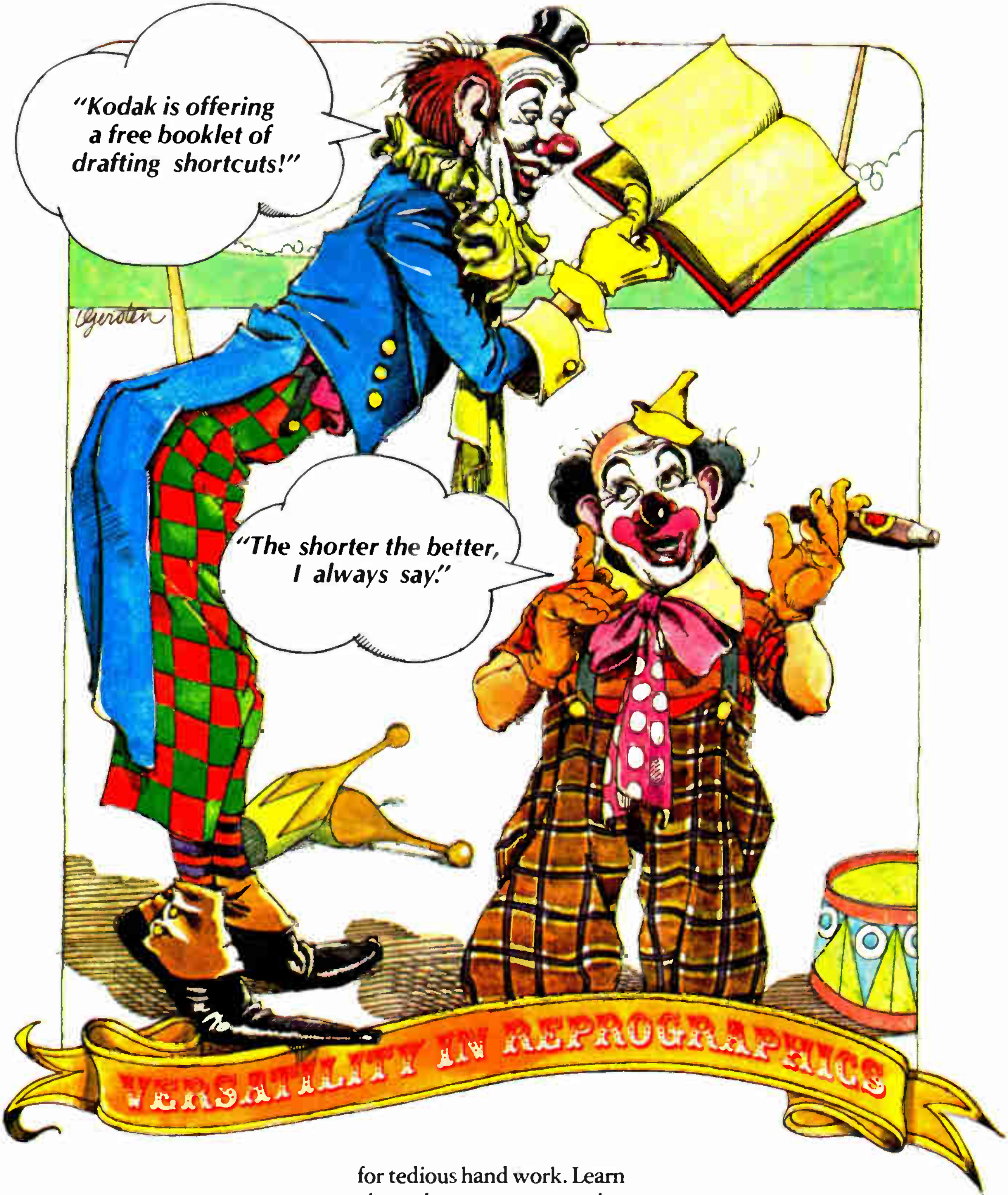
"It's a case of software getting smarter and smarter," Erny observes. "It takes a lot of memory to support software this analytical, but advanced technology enables us to equip the 4814 with 320 kilobytes of semiconductor memory and still produce a system for far less than semiautomatic test generating systems," he states.

The second proprietary advance, Erny continues, is contained in an optional ATG-II library. Whereas prior ATG logic propagated faults in a "forward" direction only—that is, the way electrical signals would actually flow through the circuit—the ATG-II library contains entries that describe reverse as well as forward fault propagation through electronic devices. "This enables ATG-II to quickly and intelligently select, or synthesize, the most efficient path along which the fault may be propagated out for detection, and then to actually drive the fault along this path and identify it," he states.

As with most standard libraries, the ATG-II library can be enhanced by the addition of user-generated tables. Use of up to two of these tables per device, Erny says, "enhances the speed of the system generating the program, as well as the effectiveness of detecting the possible faults that can occur on a board."

Available 90 days after receipt of the order, the 4814 ATG-II hardware configuration consists of a 16-bit minicomputer with 320 kilobytes of memory, an alphanumeric cathode-ray-tube terminal, a 256-kilobyte floppy-disk drive, and a 10-megabyte dual-moving-head disk drive. Also included is the Montos operating system, the ATG-II software package, a functional emulation software package, and a DES (design engineering simulator) logic simulation software package with associated libraries.

Computer Automation, 18651 Von Karman, Irvine, Calif. 92713. Phone (714) 833-8830 [338]



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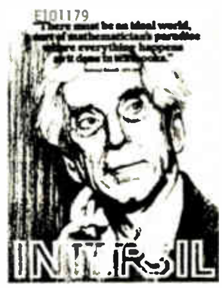

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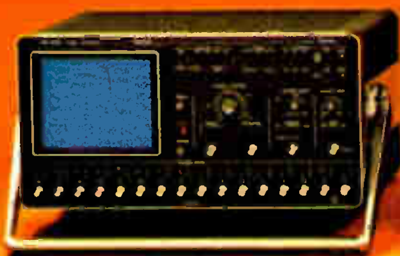

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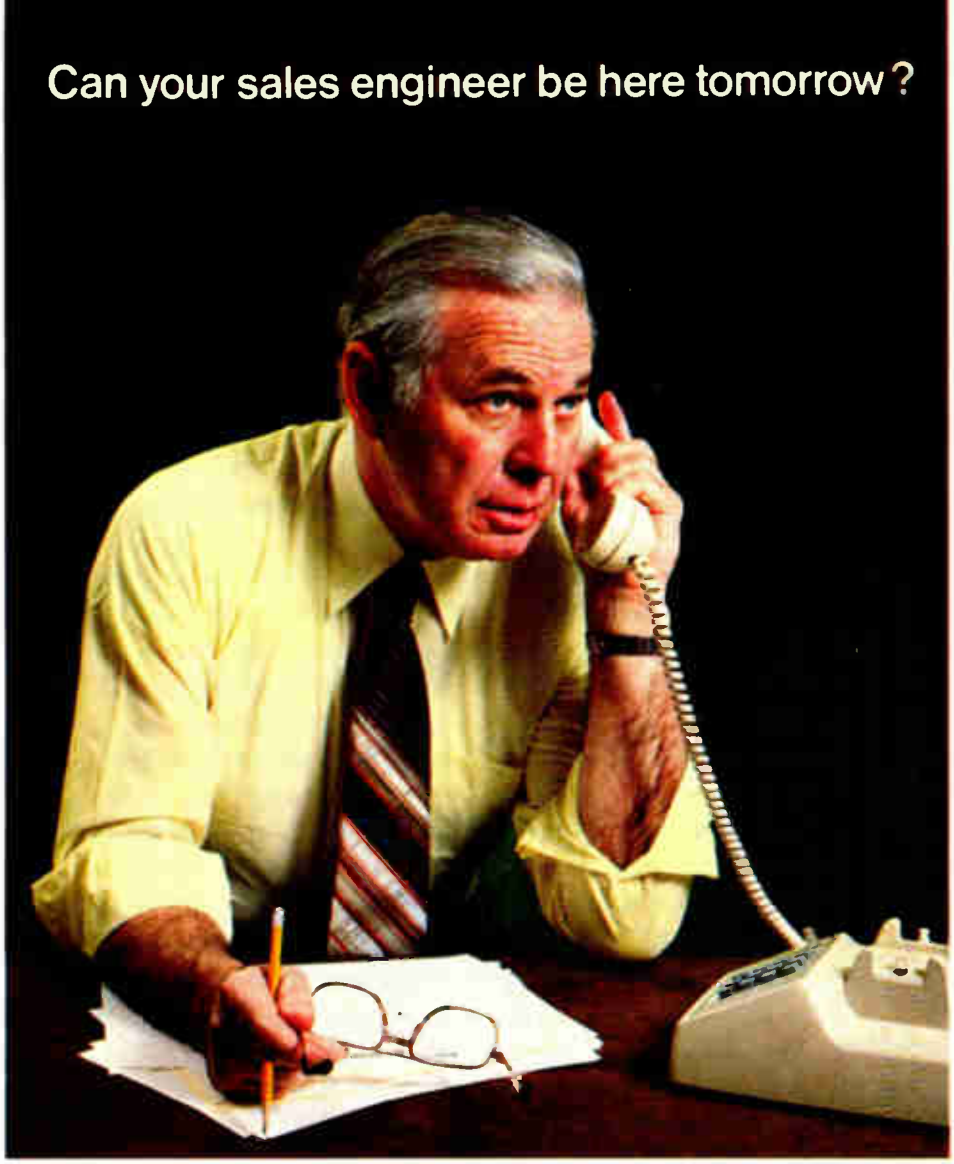

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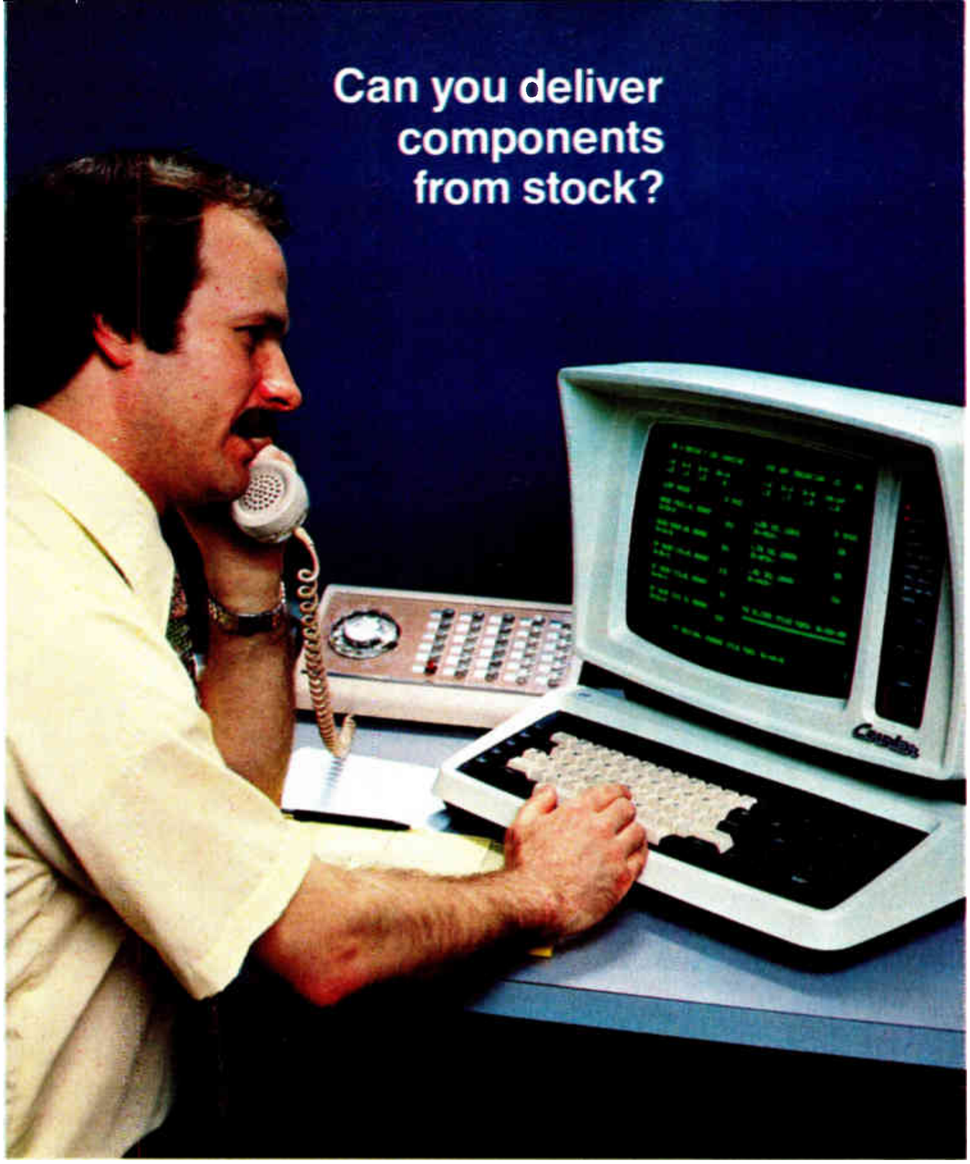

Product availability is maintained through a world-wide network of factory-trained distributors with large stocks on hand, plus in-depth back-up inventories at the TRW plants. With 300 product lines, not every item can be stocked, but TRW markets more components types through distributors than any other electronic component manufacturer.

Customer service is maintained through 250 people in more than 50 sales offices, with factory engineering and marketing staffs to help them. At TRW, service, before *and* after the sale is as important as consistent quality and competitive prices.

When you want yes for an answer, call your TRW distributor, TRW/ECG sales office or Renfrew Electronics in Canada.

You'll find them listed in EEM, Gold Book, Electronics Buyers' Guide, Who's Who in Electronics, the Electronic Industry Telephone Directory and the Electronic Buyers' Handbook.

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Computers & peripherals

Printer offers high resolution

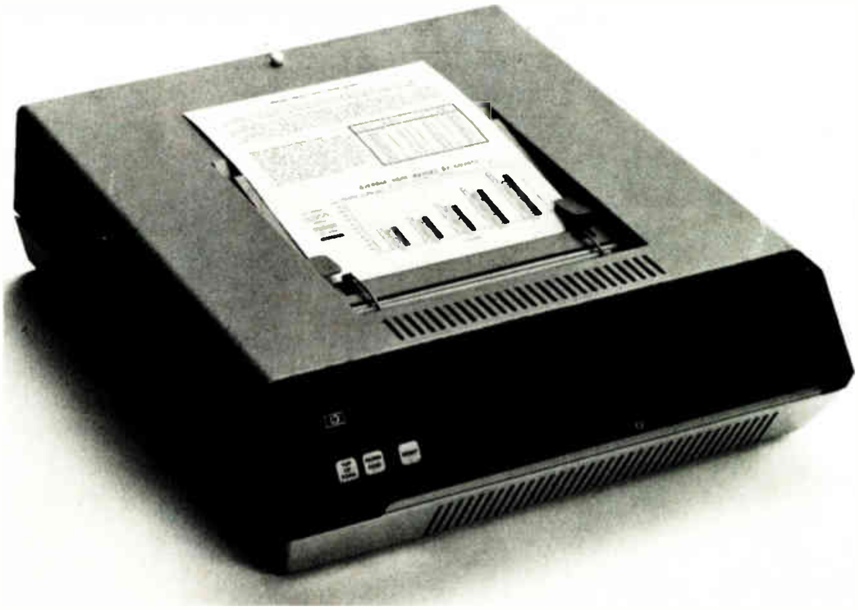
Thermal-writing raster unit for text and graphics prints 720 dots across 8.5 in.

In many instances, it is desirable to produce hard-copy records of display images or text information generated on a cathode-ray-tube display. However, to do so has often required either discrete text and graphics printers for each type of data, or a CRT copier with a video interface, which prints only the data appearing on the display screen at a given time. Now, there is a more comprehensive solution to this printing problem in the form of a high-resolution text and graphics printer from Hewlett-Packard Co.

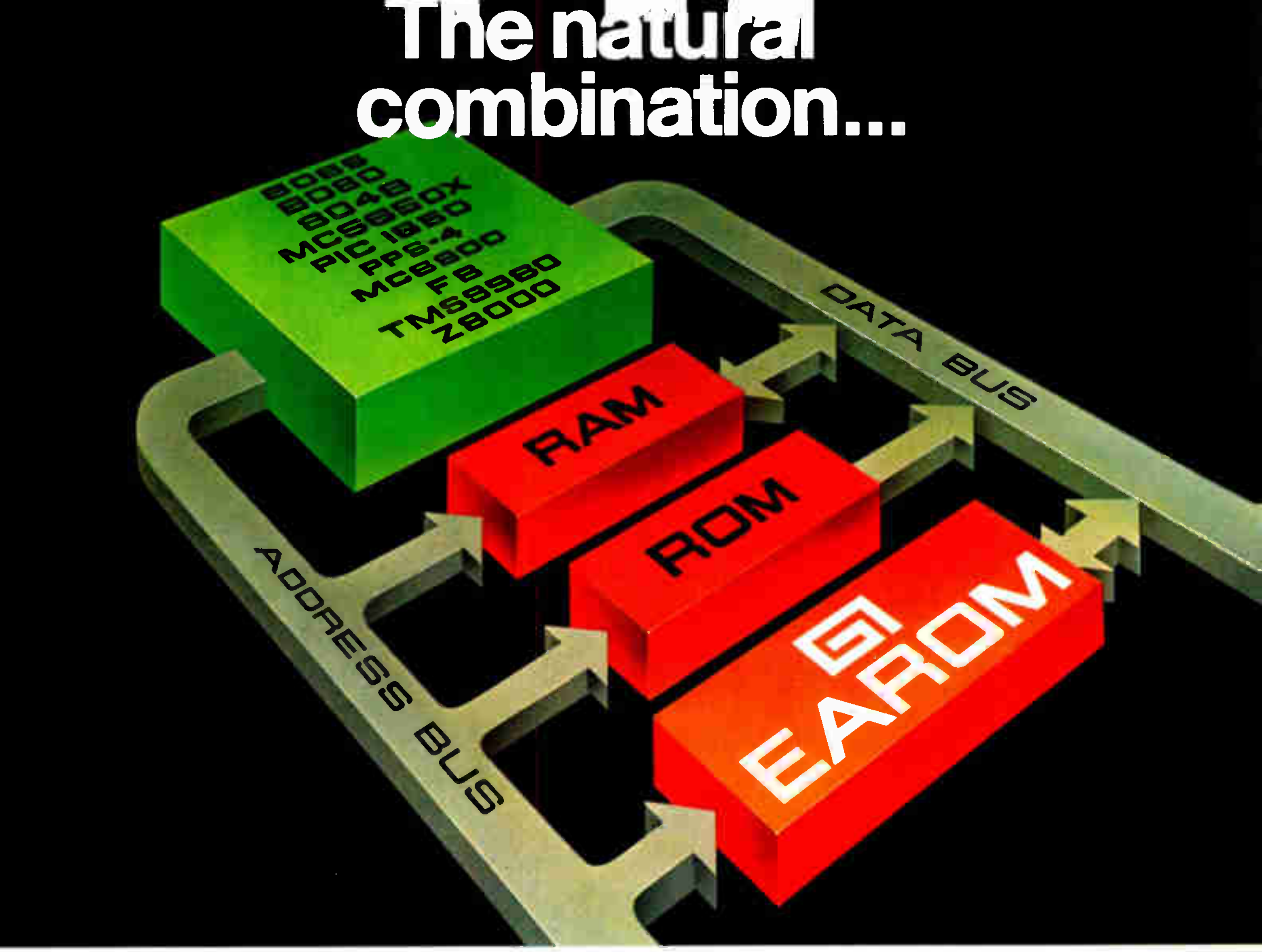
Dubbed the 7310A, this computer peripheral is the first in a family of thermal-writing raster-graphics and text printers produced by HP's San Diego division. Not only does it come with two operating modes, a character-oriented line printer, and a raster-oriented graphic display printer, but the 7310A is capable of combining both text and graphic images on the same page. In addition, because it gets its signal directly from the memory in the CRT terminal, rather than from the display screen or a storage tube, it can print all the information that has been generated, and not just that on the CRT screen, says product marketing engineer Tom Tremble.

The primary emphasis in developing the 7310A has been to produce fast, high-resolution graphics copy. Single- and multiple-page copies are made by moving roll-format thermal paper past a fixed linear array of thin-film resistors arranged in six individually replaceable assemblies. Each assembly contains 120 resistors on 0.01-in. centers, producing a total of 720 dots across the width of a standard 8.5-in. page. A provision for seven assemblies allows up to 780 dots for displays that require higher resolution.

Operating as a graphic CRT display printer, the 7310A prints out, dot for dot, graphic and alphanumeric data generated elsewhere in a two-dimensional binary array format. Data is transmitted to the unit a line at a time, with eight successive dots encoded into 8-bit bytes. Each raster line is preceded by an escape character sequence. Absolute picture size is determined by the number of dots in the source. Assuming no limi-



The natural combination...



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GI EAROMs will meet your needs for parallel or serial I/O, in 4, 8 or 16-bit word widths. A non-volatile electrically-alterable ROM, it allows you to erase and program individual words, while data can be stored reliably, and without power, for ten years.

Unlike EPROMs, EAROM-stored data can be easily updated—reprogrammed electrically in the system. As a non-volatile memory, EAROM can save data or pointers in the event of a power failure...like a RAM with a battery—without the battery!

GI EAROMs are available *now*. In quantity. Priced competitively. For metering pumps, appliance timers, controllers, calculators, data terminals, and countless other applications. If the system is microprocessor-based, GI's EAROM is bound to make it better!

Prove it yourself on your next project. Our Application Notes and engineers will assist you. Just write or call General Instrument Microelectronics, 600 West John Street, Hicksville, New York 11802. (516) 733-3192.

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GENERAL INSTRUMENT CORPORATION
MICROELECTRONICS

GI

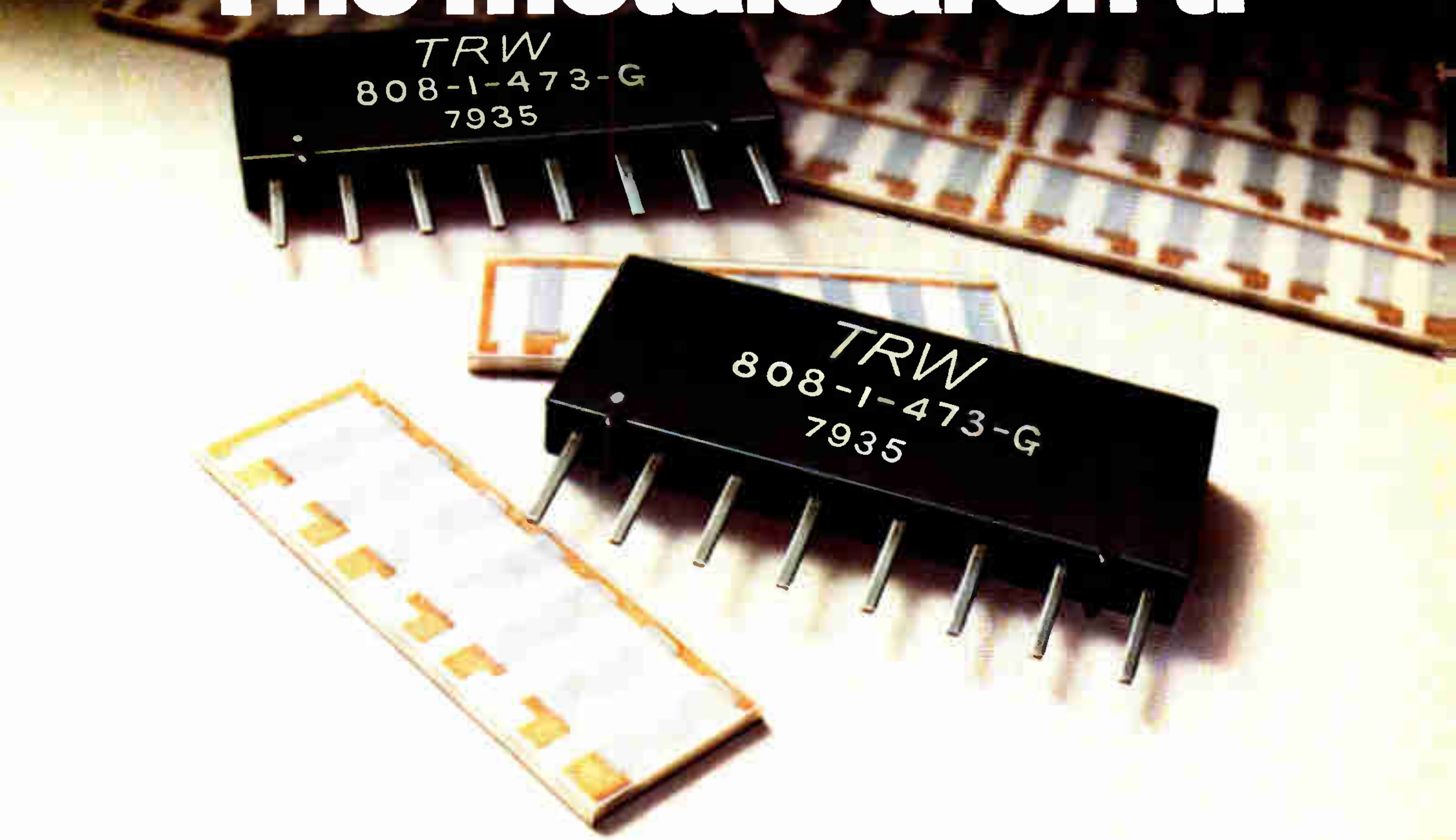
tations from data transfer rates, the graphic print speed in the raster mode varies from 125 dot rows per second for light density to 16 dot rows per second for maximum density. According to Tremble, "a full 8.5-by-11-inch page can be printed in as little as 10 seconds."

As a text printer, the 7310A will print 80-character lines of ASCII-coded text, one complete line at a time, using internally generated fonts based on a seven-by-nine-dot matrix within a 9-by-15-character cell. Character aspect ratio is programmable in the vertical direction over a range of 1:4 through 2:1. The default condition provides a 1:1 dot ratio, with 0.1-in.-high characters. Depending on line length and density, text is printed at 200 to 500 lines per minute.

The 7310A can have a total of six character sets at any time, although the basic unit is provided with a 128-character ASCII font, an HP Roman extension set, and a proportionally spaced set for enhanced display. An optional "language enhancements" capability adds terminal line drawing (forms) and math symbol sets, provision for up to 14 user-defined symbols, programming symbols for such languages as APL, and additional language sets, among them the Japanese Katakana script.

Controlled by two 8-bit microprocessors — a Z80 that does text and graphics formatting and an F8 that takes raster data, accumulates and prints it and advances the paper — the 7310A is programmable through 27 text operations commands. Among those things that can be programmed are character set selection, enhancement modes, page size, margins, and other printer functions such as tab control, character size, and line spacing. The specific character set and enhancements for underline, inverse printing, bold-face print, and variable ratio are programmable through escape character sequences and shift-in/shift-out protocol on a per-character basis. These programming techniques are identical to those used in the HP2640 series of graphic and alphanumeric terminals and HP9825 and

The performance is noble. The metals aren't.



New! TRW Series 800 Single-in-line Thick Film Networks.

TRW's cermet thick film networks perform like they were made with precious metals. Except that our system is totally non-noble, *eliminating* gold, silver and platinum group metals entirely.

Take our patented TanTin™ resistive material. It's a tin oxide system fired in inert N_2 at 1000°C. Our own thick film copper conductors are also fired at very high temperatures, producing an exceptionally rugged, stable resistor network. And an IR100 award winner.*

Our *new series 800* SIP's come in a transfer molded package in 6, 8, and 10 pin configurations, dimensionally clean and saving PCB real estate.

For example, 808-1 7 resistor SIP uses < 46 mm². That's less than one discrete ½W resistor laying flat on the board.

Now, you can get noble performance, without noble metals. Look:

Resistance Range = 33Ω–1 Meg, ± 2, 5% tolerance laser trimmed.

Schematics include N-1 common, N/2 isolated resistors.

Power Ratings are 1.5–2.7W/package, 0.3–0.5W/resistor.

TCR Tracking is ≤ .005%/°C. ± .02%/°C absolute TCR.

TCR Slope provides excellent hot to cold side differential.

See EEM '79-'80 Master Catalog pp 3644-45

Also ask for our low profile SIP and DIP configurations.

For more information contact your local TRW/ECG sales office or TRW/IRC Resistors, an Electronic Components Division of TRW Inc., Greenway Road, Boone, N.C. 28607. Dept. N, (704) 264-8861.

*(TM) TanTin (a TRW trademark), received *Industrial Research/Development Magazine* award as one of the top 100 industrial product developments of 1978.

TRW IRC RESISTORS
A DIVISION OF TRW INC.

Circle 179 on reader service card

9835 desktop computers.

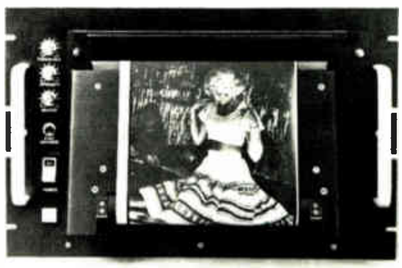
Priced at $4,750 and available within six weeks, the 7310A is housed in a 17.5-by-6-by-20.2-in. package. Its principal market, according to Tremble, is as a peripheral for HP graphic and future high-resolution terminals, where an HP-IB interface is used. An RS-232-C asynchronous serial interface connects the 7310A as a printer peripheral to HP alphanumeric terminals and can also be used as a remote connection to HP's series 1000 or 3000 computer systems. An I/O (8-bit-parallel) interface broadens applications to include non-HP computers and graphic display systems.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [361]

Rugged graphic recorder uses fiber optics and CRT

Increasing its efforts in the peripheral printer and plotter industry, EDO Western Corp. is intensifying production of fiber-optic-based graphic recorders. The recorders, with their fiber-optic faceplates, offer resolutions of up to 400 lines per inch, and will print up to 32 varying shades of gray. They will also reproduce graphics and alphanumerics on different types of paper and film, at different rates of speed.

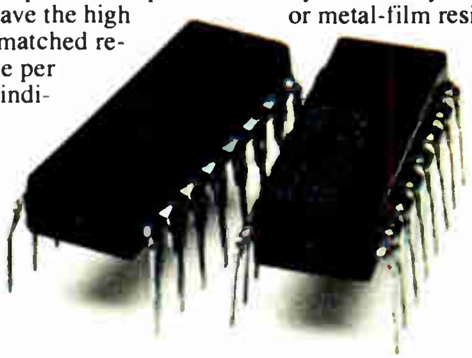
The printers use a flat-faced cathode-ray tube against which a bundle of fiber-optic wires is placed. The fiber-optic wires transfer the light images from the CRT directly onto photosensitive paper or contact film. "No lenses or other equipment are used," notes Howard Jones, engineering manager for the company. Analog or digital data is transmitted



Beckman breaks the cost barrier in thin-film networks.

Now you can get the precision performance of thin-film networks at the low cost of metal-films. Our large volume production and extensive experience in resistor networks makes this low cost possible.

Our 14- and 16-pin DIP's, models 699 and 698, with their close ratio matching and exceptional temperature tracking, have the high performance of matched resistor sets, yet the per resistor price of individual discretes.



Using Beckman thin-film resistor networks results in more savings than just their direct cost, however. You also reduce component count, assembly costs and inventory levels.

Finally, thin-film networks can ease your reliability worries with their long-term accuracy and temperature stability. Whether you're using wirewound or metal-film resistors, Beckman's thin-film networks offer you a superior alternative. In both performance and cost.

Call your local Beckman representative today, or write: Network Products Operations, Beckman Instruments, Inc., 2500 Harbor Blvd., Fullerton, CA 92634. In Europe write: Beckman Instruments (Belgium) S.A., 14, Avenue Hamoir, 1180 Bruxelles, Belgium. Telex: 23577

- Low cost...comparable to metal-film discrete resistors.
- 1% to 0.1% resistor tolerances available.
- 0.1% ratio accuracy.
- ±50 $P/10^6/°C$ tempco for improved environmental stability.
- ±5 $P/10^6/°C$ tracking.
- Saves cost in manufacturing, stocking and inspection.

Design Beckman thin-film in.
Design problems out.

BECKMAN

Circle 181 on reader service card

New products

through a video line to the CRT for display. Jones points out that parallel interfacing to a bus is needed to link the printer with a computer.

"It's more than a lab instrument," he says, adding that the printer is ruggedized and will probably be used mainly in the field. Applications include down-hole oil-well studies, as well as shipboard and aircraft data recording. Each unit will be made to order; prices start at about $13,000 and can go as high as $60,000 depending on the customer's needs. Delivery time is approximately four to six months.

EDO Western Corp., 2645 South 300 West, Salt Lake City, Utah 84115. Phone Randy Waters at (801) 486-7481 [363]

System turns video signals into hard copies in 20 s

Providing archival-quality hard copy from raster-scan-display terminals and video sources within 20 s, the 1641A video hard-copy system has a 132-column computer printout rate of 1,000 lines per minute and a computer graphics printout rate of six pages per minute, both with a resolution of 160 dots per linear inch. A single 1641A system can serve up to eight terminals.

The 1641A consists of two modules: an electrostatic printer and plotter, and a video interface, which may rest on a desktop or be rack-mounted. When equipped with long-line capability, the printer may be separated from the computer interface by a distance of up to 1,000 ft. The video interface unit allows the same signal sent to the video monitor to be sent to the printer, permitting

Your Marketing department wants a new black box design. They want it to handle 37 bytes of information. It has to be solar energized. It has to fly. It has to speak. It has to reproduce. Naturally, it'll need special cable configurations. Call Belden.

We've developed workable wire, cable and cord answers for a lot of extraordinary new products. In fact, a lot of designers have found that working with Belden in the early stages of a design project usually pays dividends in compatibility, workability and lower overall costs.

And once your product is rolling, we're ready to dig in to wire processing, assembly and installation problems to help insure that your idea makes it to market economically.

You see, Belden's capabilities in wire, cable and cord are comprehensive. Sure, we make thousands of standards, but we can also provide just about any custom that you can imagine. And our technical knowhow ranges from innovative packaging to in-depth value analysis.

Just imagine a wire, cable or cord—and we'll come through with it. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 317-966-6661. Out West, contact our Regional Sales Office in Irvine, CA at 714-833-7700.

8-7-9A

Your special designs need a special wire source

the printer to be at the end of a daisy chain of CRT monitors. The video interface produces an 8-bit digital signal to drive the printer.

The 1641A should find use in office environments with management information systems, as well as in other areas where hard copies of CRT images may be desired, such as those produced with computer-aided-design systems.

The 1641A—with both the electrostatic printer and plotter and the video interface—sells for $10,500 in the U. S., and $13,725 internationally. Delivery is within 90 days, after receipt of order.

Versatec, a Xerox company, 2805 Bowers Ave., Santa Clara, Calif. 95051. Phone Bruce Fihe at (408) 988-2800 [364]

Video digitizer displays, stores data from camera

Operating on data from a video camera, a fast-scan video digitizer has been designed to work with S-100-bus computers. The device converts the output from the camera—or any other source of composite video material—into 8-bit, gray-scale, digital information.

The data can be transferred through software to either a memory-mapped high-resolution video board, or to main memory for later retrieval. A complete driver program, implementing 16 gray shades, is included for board control, image dispay on a high-resolution video board, image storage on disk, and image printing on a matrix printer.

The maximum horizontal resolution is approximately 700 points per line, with vertical resolution at 480 lines per image.

The digitizer can be used in a variety of consumer environments, as well as for medical, security, and other special-purpose applications requiring image storage and analysis. Priced at $175, the digitizer, factory-assembled and tested, is available from stock.

Vector Graphic Inc., 31364 Via Colinas, Westlake Village, Calif. 91361. Phone (213) 991-2302 [366]

NEC Newscope

Fiber Optics System For CATV

In Japan, the world's longest fiber optics CATV system was recently put into service by Lake-City Cablevision Co. (LCCV) at Suwa City in the central part of the country.

LCCV is one of the largest CATV companies in Japan, serving more than 10,000 subscribers along its 31-kilometer trunk cable which includes the newly completed 10-kilometer fiber optics system made by NEC. The company rebroadcasts local television shows as well as programs televised by key TV stations in Tokyo about 180 kilometers east of Suwa.

The Suwa area is well-known for thunder storms and is often hit by lightning. The fiber optics system, however, can provide extremely high-quality video service completely free from the noise disturbance which is most apt to occur with conventional copper wire cable.

NEC engineer installing pole type repeater of a fiber optic CATV main trunk line.

Circle 186 on reader service card

Trinidad-Tobago Orders Eight ESSs

Trinidad and Tobago Telephone Company Limited, Republic of Trinidad and Tobago in the West Indies, has awarded NEC an order for electronic switching systems to be installed at 8 exchanges in the country.

NEC is responsible for the manufacture and installation of ND20 electronic switching systems for 8 exchanges to accommodate a total of 34,000 local lines and 5,000 trunk lines.

The ND20 will offer new custom calling features for the first time in the country, including abbreviated dialling, call forwarding, call waiting and three-way calling. Besides these custom calling features, the systems will be equipped with LAMA or CAMA (local/centralized automatic message accounting) feature.

Circle 187 on reader service card

Low Power Microwave Equipment For Peru, Madagascar

Peru is to have a new microwave link, partly powered by solar cells, running northeast at a distance of about 375 kilometers from Cerro de Pasco at an elevation of 4,350 meters in the Andes to Pucallpa in the upper reaches of the Amazon. When completed in mid-1980, it will provide 960 high-grade telephone channels and a television channel over a 4 GHz band.

Since the area to be covered by the new 12-station link includes many peaks of the Andes range, with a height of over 4,000 meters, and the deep forest region in the upper reaches of the Amazon, the link will be provided with a highly reliable low-power consumption microwave communications system to withstand the severe geographical and other natural conditions.

NEC's low-power consumption microwave system can run on the small power of 18 watts per transmitter/receiver, thus a radio repeater station which accommodates 2 routes including protection system can be operated on a total power of 83 watts.

Therefore, six of the 12 repeater stations are to be powered by solar cells.

Another energy-saving microwave communications system is to be installed in the Democratic Republic of Madagascar off the coast of East Africa.

The system will consist of 16 terminal stations, 3 repeater terminal stations and 14 repeater stations. It will cover a total distance of about 830 kilometers from Antananarivo, the capital in the central part, to Tulear on the southwestern coast providing 960 telephone circuits and a color television channel.

Ten of the 14 repeater stations will be provided with a unique power supply unit, a liquid fueled thermoelectric generator also developed by NEC, instead of a conventional diesel engine generator. The new power equipment, measuring 100cm(h) x 90cm(d) x 30cm(w) and weighing 72kg, needs only 0.4 litres of diesel fuel or kerosene to generate 100 watts at 7 volts per hour. This is enough to power three units of low-power consumption radio equipment.

Newly-developed NEC energy-saving liquid fueled thermoelectric generator for low-power consumption microwave systems has no rotating parts.

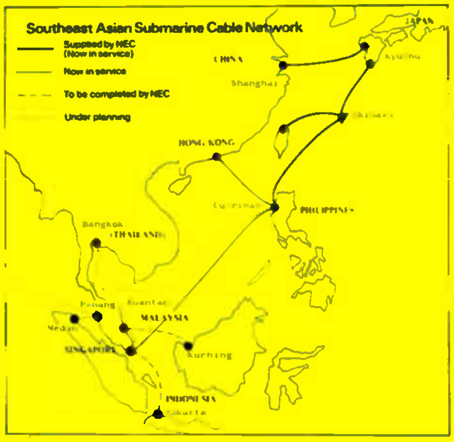
Circle 265 on reader service card

No.110

Malaysian Submarine Cable Contract To NEC

NEC succeeded in winning an order from the Government of Malaysia for the submarine cable system between Kuantan, Peninsular Malaysia, and Kuching, Sarawak. This submarine cable will link Peninsular Malaysia with Sarawak and Sabah which have rich natural resources and are to be developed rapidly in the near future.

The system is called the 12M system submarine coaxial cable which is 1.5" in diameter and has the capacity of transmitting 1,200 channel telephone circuits. This contract is on a turn-key basis and includes system engineering, manufacturing and supply of equipment, cable laying, maintenance and training of the personnel. The cable for this project will be laid between Kuantan and Kuching along a distance of about 860 kilometers and the most modern burying technique is to be adopted for approximately 98 per cent of the route. This method has already shown remarkable results in the prevention of damage from vessels and trawling nets because the cable is buried under the sea bed.



NEC, as a prime contractor, has already received orders for submarine cable systems from many countries, including Okinawa-Philippines, Okinawa-Taiwan, Tripoli-Benghazi (Libya) and Indonesia-Singapore.

Circle 266 on reader service card

New NEC Color Display CRTs

NEC has developed new high-resolution color display CRTs having many advantages over conventional color display picture tubes. The 12- and 14-inch products have already been placed on the market and 16-and 20-inch types are to be marketed in the near future.

The new color display CRTs use a self-convergence system which automatically converges the electron beams, eliminating the need for a dynamic convergence assembly and circuitry.

The neck is only 29mm and the deflecting power is reduced by as much as 25% compared to that needed for conventional 35.6mm-necked products. The neck diameter has been greatly diminished by the use of a newly-developed 'in-line' electron gun, yet the new CRTs feature the sharpest possible focusing capability.

The use of a pigmented phosphors and black matrix screen assures outstanding brightness and contrast. In addition, the new products feature high resolution capability because the shadow-mask aperture pitch is 1/2 that of conventional products, resulting in an increased number of 'picture elements'.

New NEC high-resolution color display CRT.

Other features include a quick-start cathode for instant viewing and internal magnetic shield which ensures the vividness of colors and adjustment-free convenience.

Circle 267 on reader service card

New Semiconductor Lasers Have Many Better Features

NEC has developed two types of semiconductor lasers: one achieves a high output power that has so far been possible only with gas lasers and the other is capable of producing very high-quality light.

The new high-output power semiconductor laser can achieve an output power of 1.8 watts in pulse operation, or 80 milli-watts in DC operation while conventional semiconductor lasers can only achieve about 10 milli-watts.

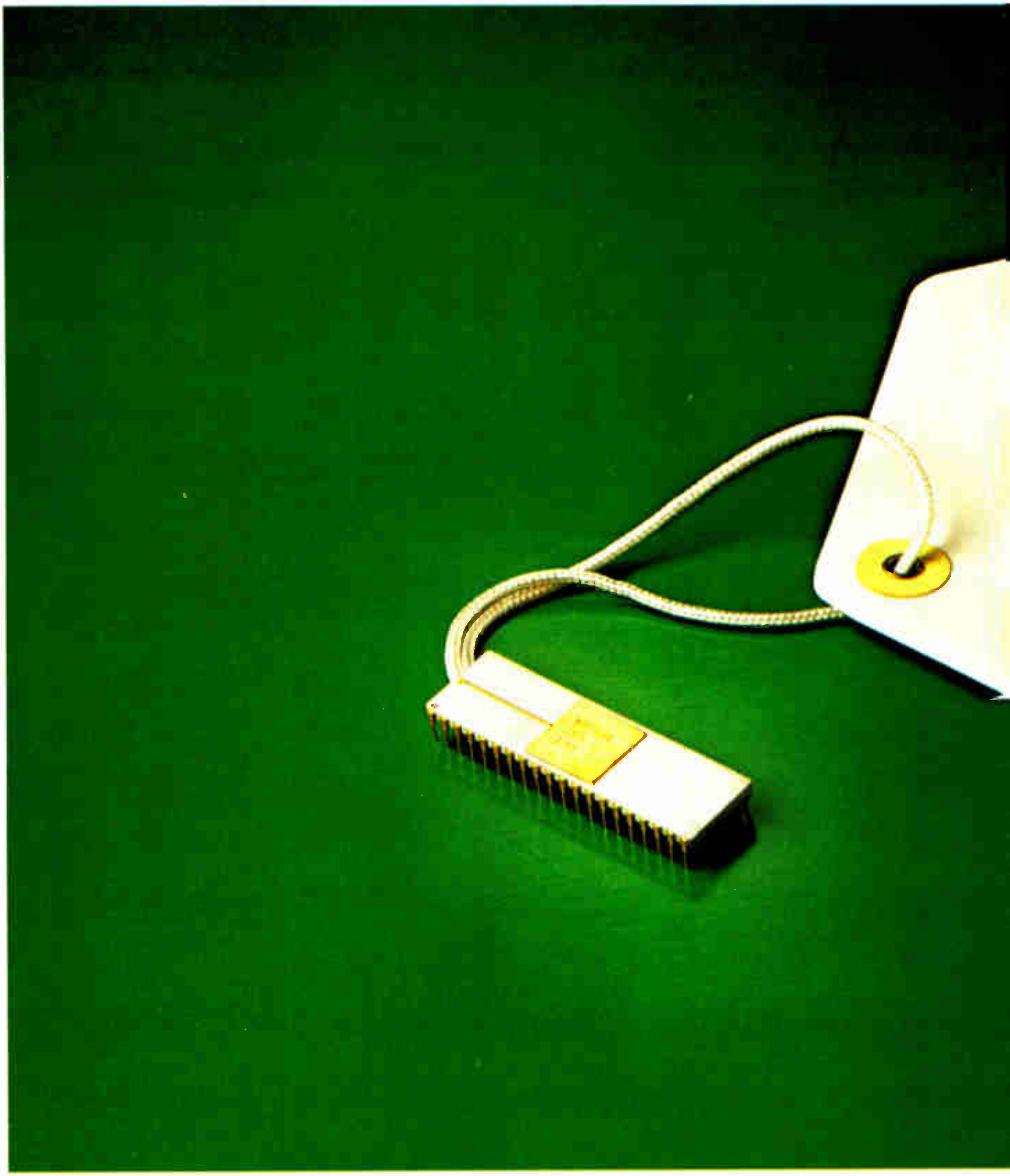
With its high output capabilities, the new semiconductor laser will be effective in long-distance optical fiber cable transmission systems or atmospheric optical communications systems. It can also be used for a laser printer, laser facsimile, laser machining, etc., by fully utilizing its exceptionally high light-energy density (about 10 megawatts/1 square centimeter).

High-output semiconductor laser.

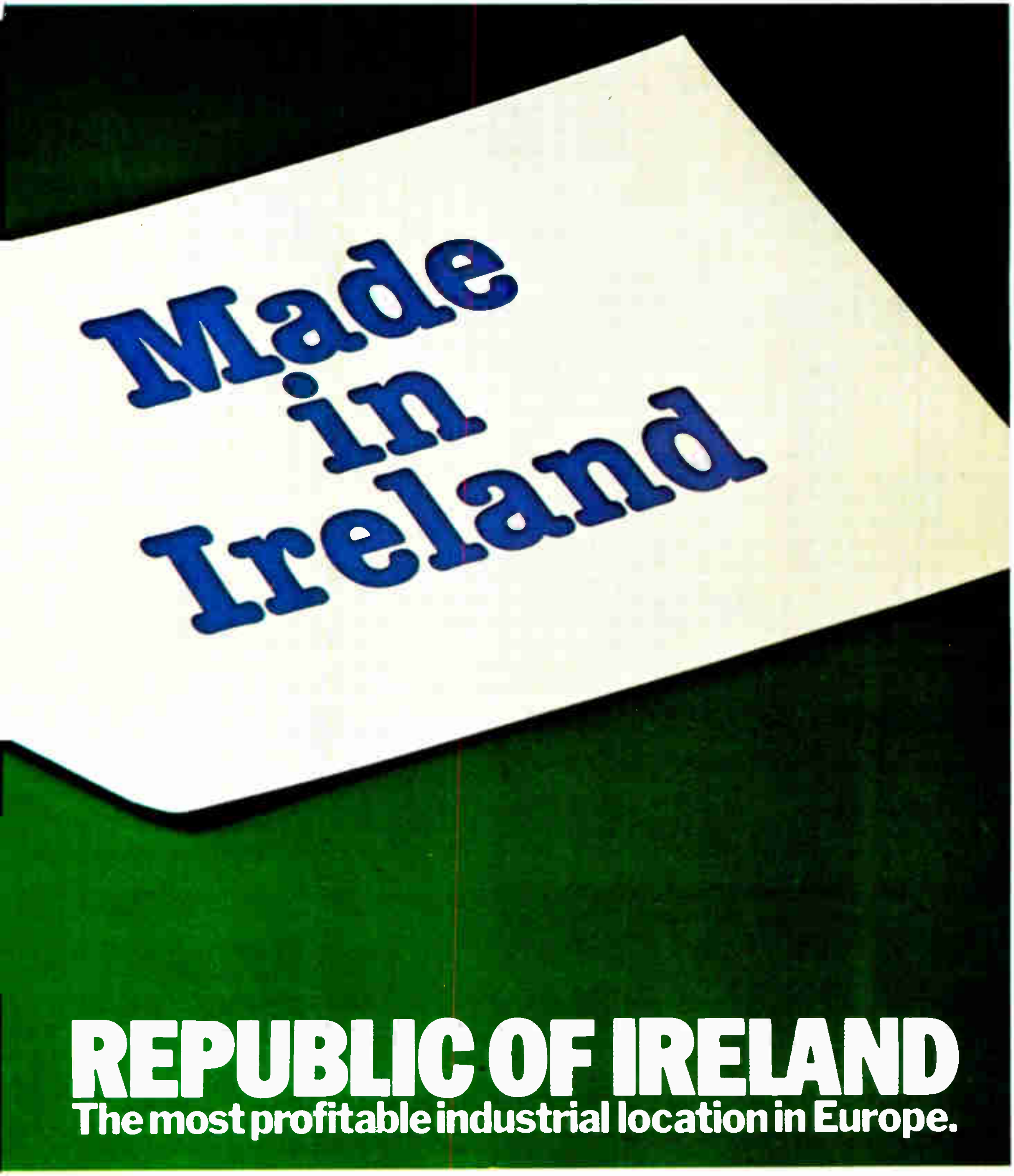
The other semiconductor laser, which is capable of producing outstandingly high-quality light, features excellent monochromaticity of oscillation spectrum, outstanding linearity of laser light vs. electric current, a small light-emitting spot and minimum light distortion.

Thanks to these outstanding features, it can produce high-quality laser light constantly and will enhance long-distance broadband fiber optical communications systems and high-precision optical equipment.

NEC
Nippon Electric Co.,Ltd.
P.O.Box 1,Takanawa,Tokyo,Japan.



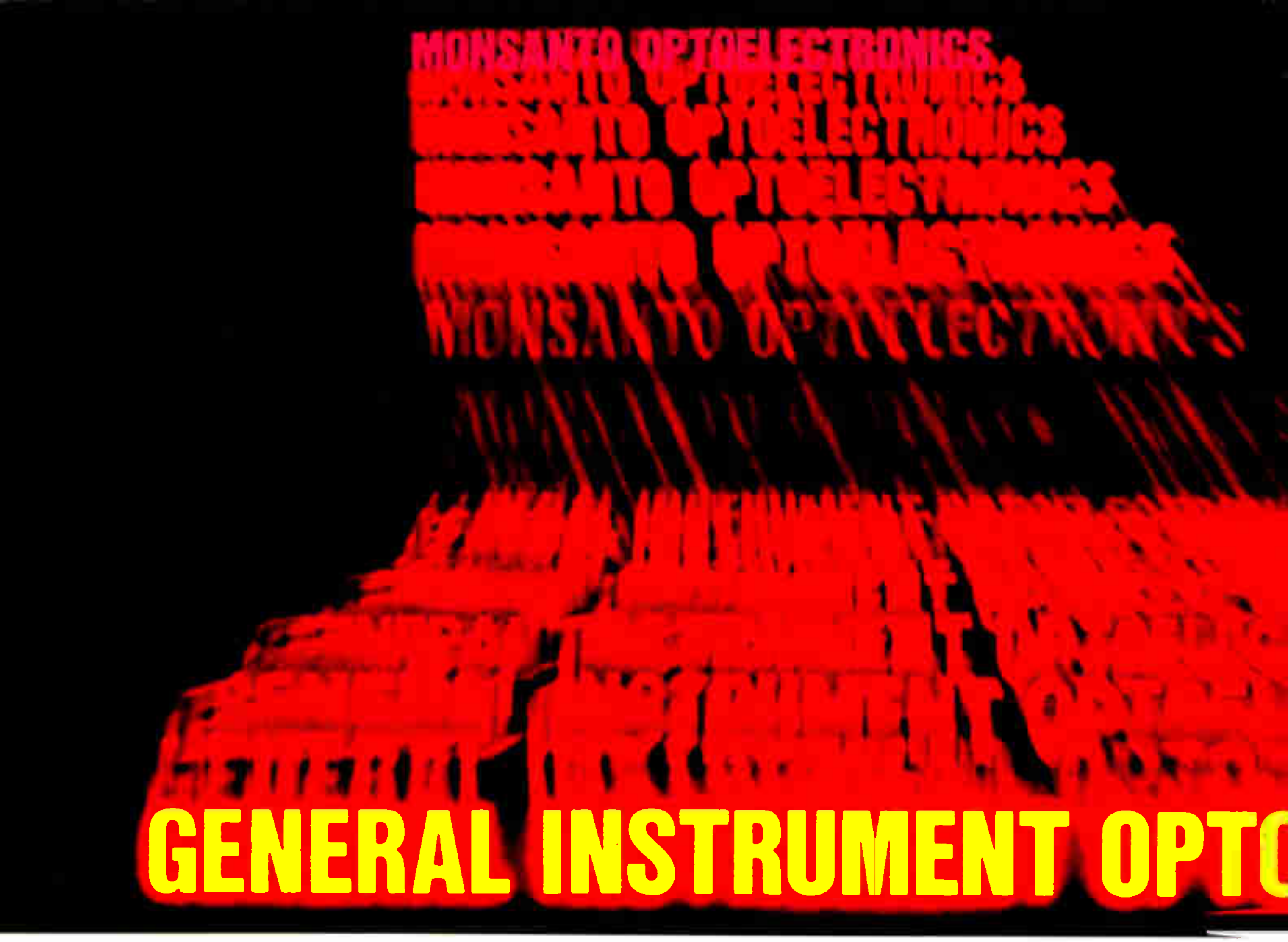
Designed and manufactured in Ireland by Analog Devices – one of 55 overseas electronic companies now operating here.
A quad scope integrating 13 bit analog to digital converter for use in converting analog voltage into digital language.



US Department of Commerce statistics for the period '74-77 show a 28% average annual return on investment for US manufacturers located in the Republic of Ireland-more than twice the European average.

IDA Ireland
INDUSTRIAL DEVELOPMENT AUTHORITY

The Irish government's industrial development agency has offices in New York, Tel (212) 972-1000; Chicago, Tel (312) 644-7474; Houston, Tel (713) 658-0055; Los Angeles, Tel (213) 624-1024. Overseas offices also in Toronto, Amsterdam, London, Paris, Cologne, Stuttgart, Copenhagen, Milan, Madrid, Tokyo and Sydney.



It's a name that is already well known in semiconductor products as well as in data systems, cable TV products, and industrial components. Now, we're taking it into another area of high technology.

In June, General Instrument acquired the total optoelectronics operations of Monsanto. Their broad product line. Their experienced people. Their modern production facilities. And most important . . . an outstanding expertise in optoelectronics.

TEN YEARS OF EXPERIENCE IS A GOOD PLACE TO START

Since 1969, the major thrust has been to apply high technological capability to product development. Result—a continuing series of "firsts" in LED lamps, displays and optoisolators. Today, you can select from over 150 high performance devices in our product line. And you are assured of high quality and top performance because of vertically integrated production . . . from LED crystal to finished LED product.

NO BREAK IN CONTINUITY OF CUSTOMER SERVICE

The same conscientious and dedicated people will continue to back up our product line. With the same prompt product and technical assistance, order processing and after-sale service. Even the product

We are the new name in optoelectronics . . .

designations remain the same. The only change you will notice is a more aggressive attitude. General Instrument is committed to providing total resources to become the leader in optoelectronics.

OUR FIELD ORGANIZATION IS THE SAME TOP TEAM

Over 50 of the most competent distributors throughout the world will continue to provide our customers with immediate availability of our wide variety of optoelectronic products. And our sales representatives are strategically located to give on-the-spot assistance in design and product selection.

THE FUTURE IS EVEN BRIGHTER

During the past year we "enlightened" the industry with better ways to use alphanumerics, new approaches to panel design and how to get bigger, brighter digits in less space. And that's just the beginning. You'll soon see the result of constant research and development as we announce a number of creative new products in the months to come. As the "oldtimer-newcomer" in optoelectronics, we'll continue to design, produce and improve the products that best fill your design needs. That's a promise.

General Instrument Optoelectronics Division, 3400 Hillview Avenue, Palo Alto, California 94304, Telephone (415) 493-0400

GENERAL INSTRUMENT

and we will continue to make a name for ourselves.

Circle 191 on reader service card

Packaging & production

In-line system inserts pc parts

Board component assembly line handles radial- and axial-leaded parts and pins

With the introduction of a flexible in-line automatic-insertion system by Universal Instruments Corp., it is possible to insert components into bare printed-circuit boards without any operator assistance at all. With the fully in-line Pass-Thru system, magazines of bare boards are loaded with axial- and radial-lead components and test pins by a bank of computer-controlled machines.

The first such system, which went for about $335,000 and is shown in the photo, has already been sold to Zenith Radio Corp. for pilot-line production of boards for a current TV set. It is expected to cut labor costs, reduce handling damage, and lower in-process inventory.

Modular. As currently configured, the Pass-Thru system is an array of modules comprising: a high-speed variable-center-distance (VCD) axial-lead inserter, a radial-lead sequencer/inserter, a wire-fed automatic termination-pin inserter, and magazine handler buffers. In the near future, an inserter for dual in-line packages will be added.

Although there have been previous in-line insertion systems, they have all been dedicated lines, devoted to a single board type. The Pass-Thru, on the other hand, can be rapidly changed over to a new board in 10 minutes or less using tooling plates designed for each new board. Another feature of the new system is its ability to accommodate machines running at different rates. For example, in the Pass-Thru, the VCD module can insert 12,500 devices per hour, the radial-lead module can insert 7,000 components per hour, and the pin inserter inserts 8,000 pins per hour. This wide difference in rates is buffered by a transfer-magazine handling system that receives processed boards in compartmentalized magazines that can hold a two-hour supply of partially processed boards.

Breakthrough. The big news in the system, in addition to its over-all capability, is the model 6341 radial-lead sequencer/inserter. This module raises the percentage of possible machine-inserted parts from 75% to 90%. It can handle several types of capacitors, including ceramic, electrolytic, film, and tantalum. It also does peaking coils and a variety of axial-lead components in the stand-up position, often used to maximize board packing density.

The sequencer/inserter can have 80 input stations in its waist-high horizontal sequencing and feeding system. Taped components are fed to the feed stations from reels or rolls. From there, they are delivered to an endless-chain conveyor in the precise order called for by the machine's computer-guided insertion program. An insertion spindle can position components at 0° or 90° rotation under program control.

All of the modules in the system are capable of operating in a stand-alone mode. A lead time of 36 weeks is currently being quoted for the new in-line system.

Universal Instruments Corp., Box 285, Binghamton, N. Y. 13902. Phone (607) 772-7522 [391]

Silicone-treated wire has built-in moisture barrier

Offering more corrosion protection than ordinary wire, a recently introduced stranded wire from TRW has a built-in barrier against water. The

New products

wire will also maintain a low resistance indefinitely.

The anticapillary wire uses a silicone blocking compound to displace practically all the air space normally found around individual wire strands. The material prevents moisture from traveling by capillary action from one end of the wire cable to the other.

The silicone compound is being offered with 18-gauge, 19-strand hookup wire initially, but the process is adaptable to other wire sizes, the company says. Applications currently range from electronic ignition systems to navigation buoys.

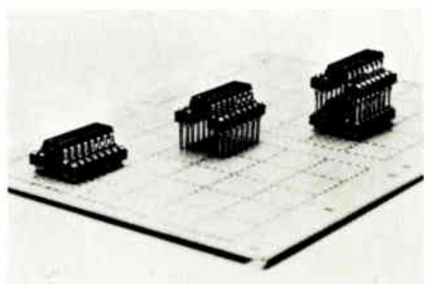
Available with tin coating or as uncoated copper wire strands, the anticapillary wire has insulation that meets ASTM standards for oil resistance. Prices, per foot, range from 1.5¢ to 3¢. Delivery takes approximately six weeks.

TRW Holyoke Wire & Cable, 775 New Ludlow Rd., South Hadley, Mass. 01075. Phone Tom Miles at (413) 533-3961 [393]

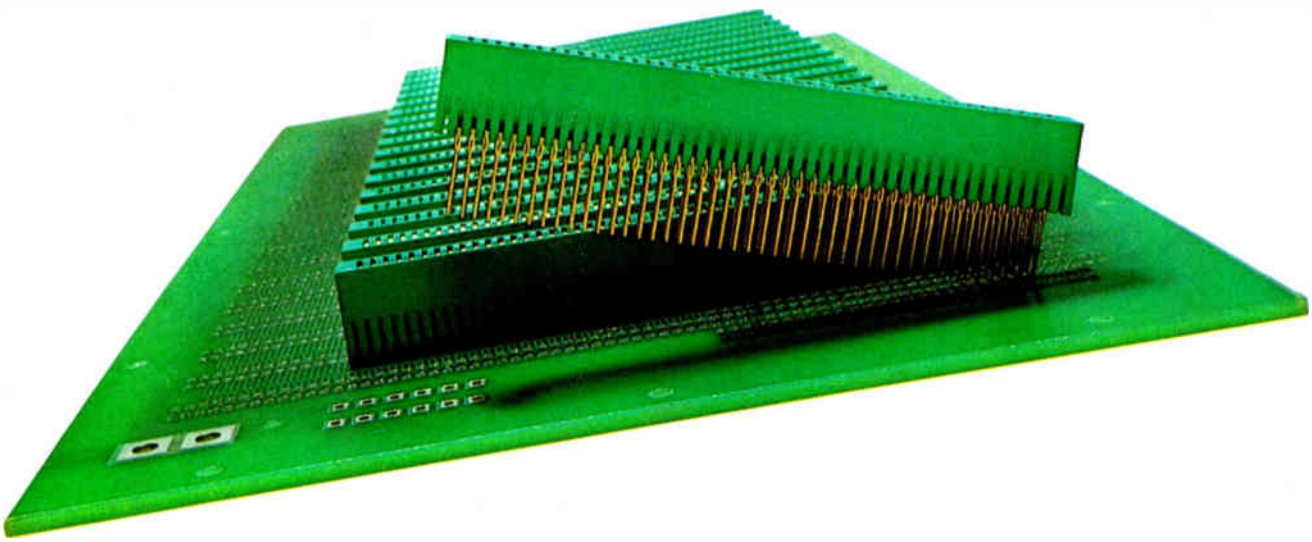
Socket strips stack onto other sockets or board-mount

With the terminals of one contact row connected to the terminals of the other row, stacking socket strips allow common termination for each double strip. The terminals come with either short pins for board mounting or long pins for stacking and clearance when plugged into another strip.

The double sockets provide a way of stacking devices vertically as well as busing. The outer contacts can be used as a connection point when breadboarding. All contacts are four-finger beryllium-copper in a

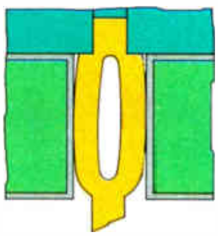


Building Backpanels? Elco's discrete press-fit card-edge connectors make it easier.



Lower costs

Elco's pre-assembled, press-fit card-edge connectors insert with simple tooling, and require low insertion forces due to a compliant press-fit section on their pins. They achieve both mechanical stability and a reliable, gas-tight electrical connection in one operation. No screws or other fastening devices. No soldering. Much lower installation costs.



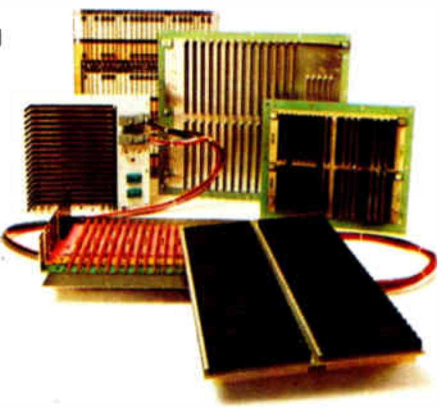
Since the circuitry is etched on a PC board backpanel, wire wrapping can be dramatically reduced or even eliminated. When wire wrapping is required, Elco's discrete card-edge connectors make it easier because the PC board places the connector tails in a known position.

The discrete advantage

Now the advantages of a press-fit connector are available with no need to cut insulators and reels of pins. Elco offers immediate delivery on one-piece connectors of any length up to 50 pairs, with a .100 x .200 grid pattern. Other grid patterns will soon be available. The standard finish is 20μ" gold over 50μ" nickel. However, other plating thicknesses, and selective plating are available.

Total Interconnect Package

Of course. Elco will be pleased to build your backpanels for you. Our capabilities extend into a broad range of press-fit, metal plate and card-edge connectors, as well as heavy copper backpanels, sophisticated multilayer and aluminum backpanels and backpanel systems — all assembled to your specifications. For more information, call or write:



Elco Corporation
Interconnect Systems Division
2250 Park Place, El Segundo, Ca 90245
(213) 675-3311/TWX 910-325-6602

Elco Corporation
a Gulf + Western manufacturing company

machined brass shell to provide a closed entry, no solder wicking, and high reliability. Connections may be made up to 1,000 times with no degradation.

Prices start at 10¢ each for double-position socket strips ordered in 100-piece quantities. Delivery is from stock.

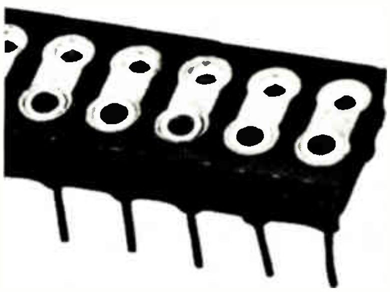
Samtec Inc., 810 Progress Blvd., New Albany, Ind. 47150. Phone Sam Shine at (812) 944-6733 [394]

Single in-line adapter accommodates several ICs

A single in-line adapter for use with dual in-line package sockets will accommodate several IC devices when it is plugged into any standard integrated-circuit socket or universal wrapped-wire panel. The adapters are available in standard lengths of two through 50 terminals with 0.100-in. center-to-center spacing with a pin offset of 0.100 in.

The IC devices the adapter can handle include: single in-line packages with 0.1-in. spacing, dual in-line packages with 0.3-in. spacing, 4-K random-access-memory devices with 0.4-in. spacing, universal asynchronous receiver/transmitter interface units with 0.5-in. spacing, and large-scale ICs with 0.6-in. spacing.

The adapter is made from G10 glass-epoxy with gold- or tin-plated brass terminal sleeves and gold-plated beryllium-copper socket clips. Prices range from 6¢ to 15¢ per terminal in moderate quantities, with delivery time ranging from



approximately two to four weeks.

Garry Manufacturing Co., 1010 Jersey Ave., New Brunswick, N. J. 08902. Phone Harry A. Koppel at (201) 545-2424 [395]

Water oxidation system replaces diffusion furnaces

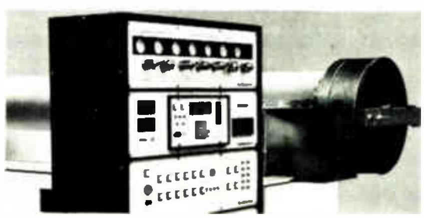
Replacing several ordinary diffusion furnaces, a recently introduced high-pressure, low-temperature water oxidation system can operate at pressures as high as 25 atmospheres. Unlike the earlier HiPOx hydrogen-oxygen oxidation system, the new one uses deionized water fed directly into the unit. With DI water, a wide operating temperature range for high-pressure oxidation is obtained. A lower operating temperature results in almost total absence of: crystalline defects, vertical and lateral diffusion, and tube devitrification.

The DI water oxidation HiPOx system is offered with direct digital control for programming, as well as a remote-control panel. The microprocessor-based digital control allows up to three separate, 30-step processes to be programmed; it sets the gas/water flow for start/stop; it permits temperature ramping; and it programs sequence timing. The remote-control option allows the HiPOx pressure vessel to be operated at a remote location while offering full monitoring capability.

Other options available for the system include a thermowell for profiling temperatures at pressure, plus a choice of perpendicular or in-line laminar flow hoods.

The system's price ranges from $101,000 to $145,000 depending on configuration selected. Delivery time is approximately 16 weeks.

Gasonics Inc., a division of Atomel, 453-C Ravendale Dr., Mountain View, Calif. 94043. Phone (415) 961-0624 [396]



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Why not try our modules XE-120, 121 and 122? They are so convenient you'll be glad to let them handle your problems.

Specifications

Items \ Model	XE-120	XE-121	XE-122
Input & Output	0 — +5V or 0 — ±5V		
Input Impedance	1M ohm		
Accuracy	±0.5%/FS	±0.1%/FS	±0.05%/FS
Power Supply	DC ±15V ±35mA		
Dimension	50W x 50D x 16H mm		

Usage

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- Automatic zero adjustment of electronic balances
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Circle 199 on reader service card

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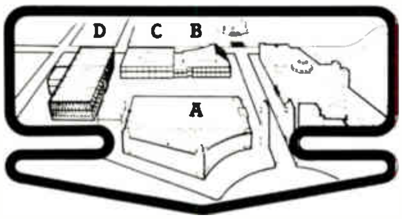
XVII INTERNATIONAL IMAGE, SOUND AND ELECTRONICS SHOW

TO SEE AND HEAR



4 large exhibitions dealing with:

(A) In Palace No. 1 (A) there will be manufacturers of radio and TV who will demonstrate their state-of-the-art know-how in the production of hi-fi systems, comprising amplifiers, modular sets, tuners, and other accessories. The exhibition will be highlighted by the most modern sound and image recording and playback equipment.

(B) The Palace of Congresses (B) will house the largest photography show in our country. Here the visitor will find equipment, from the simplest to the most sophisticated, including complex professional developing and processing units. Moreover, supplementing the Photographic Show, will be the whole wide, fascinating range of audiovisual equipment.

(C) The Fair Palace (C), specially set aside for sound, is where the professional and the amateur will find everything relating to hi-fi, public address, sound and vision recording and playback, musical instruments and show illumination.

(D) Electronic components will be exhibited in the Fiftieth Anniversary Palace (D), together with production systems and materials for electronic design, measuring and control instruments, communications (both at the highest technical and professional level and for radio hams) and security systems.

65,000 SQ. M. OF SHOW SPACE WITH 380 EXHIBITORS REPRESENTING 1200 FIRMS FROM 30 COUNTRIES.

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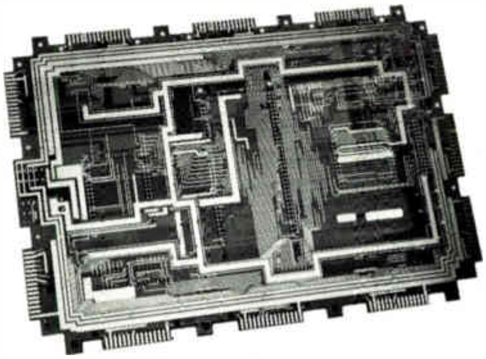
Circle 274 on reader service card

There's a big difference between PCB's and KCB's



KCB's are Kalmus precision printed circuit boards. You'll find they are an important step ahead of ordinary PCB's—in solderability, overall performance and quality.

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Circle 275 on reader service card

PHILIPS

BEAMWRITER

VECTOR SCAN LITHOGRAPHY SYSTEM

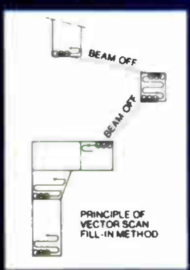
The Best Production EBL You Can Buy

Choosing an electron beam lithography system is a difficult task. Your selection will depend upon your specific requirements; however, throughput, uptime, precision, flexibility and minimum feature size are the most relevant factors in the majority of applications. That's why Philips designed the Beamwriter Lithography System to excel in each of these areas:

Throughput

In a production environment, the number of masks, reticles or chips produced per hour determines the cost effectiveness of the equipment. Throughput is critical. Philips' Beamwriter system gives you highest throughput for most applications by using vector scan technology and high dose rates.

Vector Scan



Philips' Beamwriter system is the only commercially available production oriented vector scan EBL. You achieve higher throughput with vector scan than raster scan because the beam wastes no time scanning unnecessary areas. This makes vector scan especially efficient in the production of reticles.

High Dose Rate

The efficient electron optical design of Philips' Beamwriter system gives you an exposure dosage twenty times greater than other commercially available EBL systems. This enhanced dosage enables a faster maximum writing speed and a wider choice of resists.

Uptime

Three main factors affect uptime — reliability, serviceability, and service response:

Reliability

The Beamwriter system's exceptional reliability results from Philips' 30 years experience in building dependable electron microscopes. Offstage drives are mounted in the main working chamber. By eliminating the need for bellows, the Beamwriter eliminates the possibility of downtime due to bellows failure. The stage utilizes ball bearings coated with a molecular layer of lubricant, which eliminates bearing wear. This specially chosen lubricant does not contribute to any column contamination.

Serviceability

Designed for serviceability, the Beamwriter incorporates a lifting jack within the column for quick separation of parts. This gives you access to the X-Y table in 10 minutes. Recalibration is rapid because of the unique assembly configuration of the X-Y table and the electron optics column.

Service Response

Philips has more than 3000 electron microscopes installed around the world with an experienced team of over 250 service engineers to maintain them. No other microscope or EBL manufacturer has a service organization that comes close to this in numbers, experience or dedication.

Precision

Electron Beam productivity requires alignment accuracy. The Philips' Beamwriter system eliminates drift due to thermal effects. All lenses and lens reference power supplies are water cooled. The rigidly-built working chamber utilizes special materials which have low coefficients of thermal expansion. The working chamber is also temperature stabilized. Consequently, the Beamwriter offers you overlay accuracy twice as good as other commercially available systems.

Flexibility

The Beamwriter system is built for direct writing as well as mask making. The unique substrate height sensor, standard in the Beamwriter, enables block by block refocusing of the beam to compensate for wafer distortion. Four backscatter detectors offer optimum alignment on topographical markers.

Minimum Feature Size

The Beamwriter system has a minimum beam diameter 10 times smaller than other commercially available production EBL equipment. Furthermore, vector scanning provides the potential for proximity correction, necessary to achieve narrow geometries. The Beamwriter's variable clock rates capitalize on this potential.

Philips combines 30 years of Electron Optics experience with an intimate knowledge of semiconductor manufacturing to give you the best production EBL available.

Philips delivers the systems today that others hope to build tomorrow.

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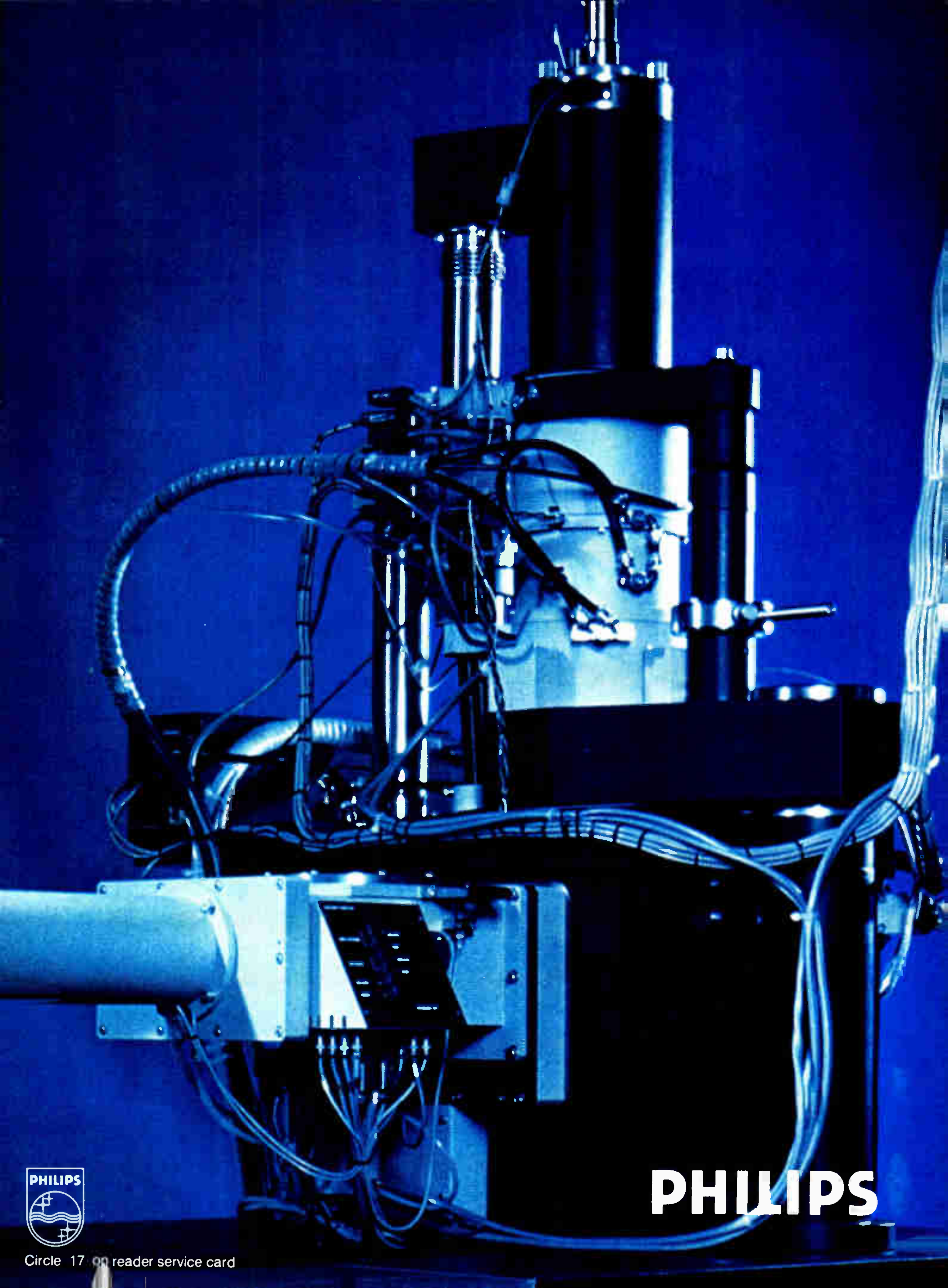
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Data acquisition

System acquires data at 35 kHz

12-bit lab unit based on LSI-11/2 processor has 14- and 16-bit options

Add Data Translation Inc. to the growing number of companies with microcomputer-based data-acquisition systems for the laboratory. The company's new system is based on a Digital Equipment Corp.'s LSI-11/2 processor, with Fortran IV and a custom set of Fortran-callable subroutines to manage all analog inputs and outputs, real-time clock, and digital input/output functions. In some models, direct memory access (DMA) is also available.

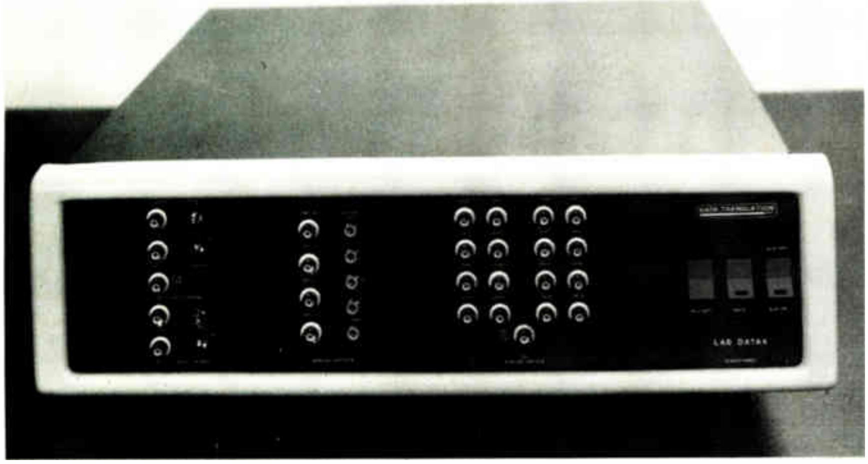
"Our basic Lab Datax is capable of throughputs in excess of 10,000 samples per second," says Data Translation's president, Fred Molinari. That is at 12 bits per sample, he points out, adding that 14- and 16-bit capabilities are optional at some cost to throughput. Speed drops to 10 kHz with 14-bit resolution and to 2.5 kHz at 16-bit resolution. The standard 12-bit version has a 35-kHz throughput rate. There is also a high-throughput option capable of achieving single-channel throughputs to memory of up to 125,000 12-bit samples per second.

Lab Datax will be available in four versions: a basic unit (DT4021), an expanded unit (DT4022), a high-throughput model (DT4023), and an expanded high-throughput version (DT4024). There will also be a user-configured Lab Datax (DT4025). Prices will run from $16,900 to $21,000, with the user-configured unit having a base price of $13,900. Adding 16-bit conversion capability will increase the price by $500 to $1000, depending on configuration.

Common ground. The different versions have much hardware and software in common. Each includes an LSI-11/2 computer with 64 kilobytes of random-access memory, a fixed- and floating-point instruction set, an asynchronous serial interface, a bootstrap loader, a line-frequency clock, and other LSI-11–supporting devices.

The mounting box for the system consists of a card cage, a power supply (+5 V at 25 A, +12 V at 3 A), cooling fans, and—unlike most other laboratory data-acquisition systems—a user-configurable front panel equipped with BNC connectors and separate analog and digital grounds. The rack-mountable case measures 5.25 by 19 by 21 in.

Software support includes a single-job monitor, foreground and background monitors, EDIT, Macro-11, Linker, and various utilities. There is also Fortran IV, version two, a superset of the ANSI standard, plus a laundry list of Fortran-calla-



ble subroutines christened DTLIB, to support Lab Datax at work.

All but the user-configurable systems come with a programmable real-time clock, a crystal-controlled unit with frequencies from 100 Hz to 1 MHz, plus 60-Hz and external inputs. The clock has four programmable modes and slope and reference-signal-level selection and can be directly connected to the Lab Datax's analog-input system for clock control of analog-to-digital conversions. Expanded systems include 32 digital inputs and outputs versus the standard version's 16 each. The digital interface is TTL-compatible and includes four control lines.

Differences. Things start getting different at the analog I/O level; for example, the DT4021 includes 16 single-ended or 8 differential inputs. The unit takes high-level signals directly or uses a programmable-gain amplifier for low-level signals and has a 35-kHz data-acquisition rate. Its analog outputs are driven by four 12-bit digital-to-analog converters with 0-to-10-V, ±10-V and ±5-V outputs and 20 mA of current drive. The analog inputs and outputs all come with BNC-equipped front-panel connections.

The DT4022 has 64 single-ended or 32 differential inputs and a 35-kHz data-acquisition rate. High-throughput units have either 16 or 32 single-ended or 8 or 16 differential inputs, DMA, and a 125-kHz data-acquisition rate. They also use a high-throughput analog-output point plotter with two or four 12-bit d-a converters and four digital outputs, as well as a DMA interface. Again, the BNC-studded front panel is standard.

Molinari is exuberant about his front-panel design. "It is going to make the lab environment much easier to work in because it makes ground loops far less likely and separates analog and digital grounds. Electrical noise should be far less of a problem." Also, unlike connections used on some other lab data-acquisition systems, all terminations are made outside the case; thus shield connections, which might be carrying interfering signals, are excluded, making for an environment nearly free of electromagnetic interference. Molinari expects users to value this aspect of the Lab Datax's design as much as its throughput. Delivery time is within eight weeks.

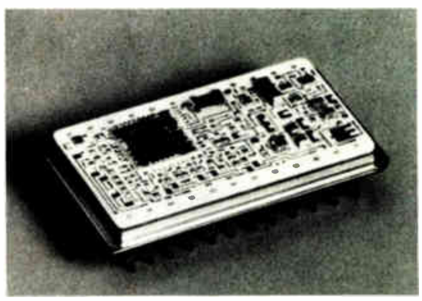
Data Translation Inc., 4 Strathmore Rd., Natick, Mass. 01760. Phone (617) 655-5300 [381]

12-bit d-a converter features fast settling time

Providing fast settling and low glitch, a 12-bit digital-to-analog converter comes complete with an internal reference, feedback resistors, and an output amplifier. Pin-programmable for either current or voltage output, the DAC-8528 has a settling time to within ±½ least significant bit for a full-scale input change of 60 ns maximum for current output and 1 μs maximum for voltage output. The glitch area is 3 mA-ns maximum for current output and 2.5 V-ns for voltage output.

The unit has a maximum linearity error of ±0.0125% over temperature; gain and offset errors are trimmable to zero. Voltage ranges are ±2.5, ±5, ±10, 0 to −5, and 0 to −10 V. Current ranges are ±2.5 and 0 to 4 mA. Processed to MIL-STD-883 with optional burn-in, the converter is available with two operating temperature ranges: −55° to +125°C, and 0° to 70°C.

Coding is binary or offset binary.



The hybrid device requires ±15-V power supplies. It is housed in a hermetically sealed metal case that measures 1.4 by 0.8 by 0.2 in. The price of the DAC-8528 starts at

$250 in quantities of one to nine.

ILC Data Device Corp., Airport International Plaza, Bohemia, N. Y. 11716. Phone (516) 567-5600 [383]

A-d unit converts 12 bits in 2 μs maximum

With a 2-μs maximum conversion time, the ZAD7100, a 12-bit successive-approximation analog-to-digital converter, is fast. The unit features a differential nonlinearity temperature coefficient of 3 parts per million/°C, a ±½ least-significant-bit quantizing error, and ±0.012% relative

accuracy (nonlinearity error).

Housed in a diallyl-phthalate package measuring 2.0 by 4.0 by 0.4 in., the hybrid uses low-temperature-coefficient thin-film resistors to ensure no missing codes over the 0° to 70°C operating temperature range.

Requiring 50 mA at ±15 V and 180 mA at +5 V, the unit is priced at $299 in quantities of one to nine. It is delivered within 30 days.

Zeltex Inc., 940 Detroit Ave., Concord, Calif. 94518. Phone (415) 686-6660 [385]

12-bit current-output d-a converter has $29 price

The DAC563 is a 12-bit current-output digital-to-analog converter priced at $29 in 100-piece quantities. Complete with internal reference, it is pin-compatible with other 563-type converters. Nonlinearity is typically ±¼ least significant bit (±½ LSB maximum). Gain drift is ±5 parts per million/°C maximum, bipolar offset drift is ±4 ppm/°C maximum, and differential linearity drift is ±3 ppm/°C, maximum.

The unit has a settling time to ±½ LSB (with current settling into a short circuit) of 3.5 μs maximum for a full-scale step. The output current for unipolar models is 0 to −2 mA, and −1 to +1 mA for bipolar operation. The DAC563 comes in two temperature versions: one specified at 0° to 70°C and the other at −25° to +85°C. Both versions are monotonic over the specified temperature range.

Incorporating a stable, weighted current-switch chip, a thin-film laser-trimmed resistor chip, and an internal reference chip, the converter is hermetically sealed in a 24-pin dual in-line package. The internal reference is stabilized for consistent accuracy over temperature, according to the company.

The DAC563 is available from stock.

Burr-Brown Research Corp., Box 11400, Tucson, Ariz. 85734. Phone Herman Loopeker at (602) 746-1111 [386]

$884 portable data loggers handle up to 50 sensors

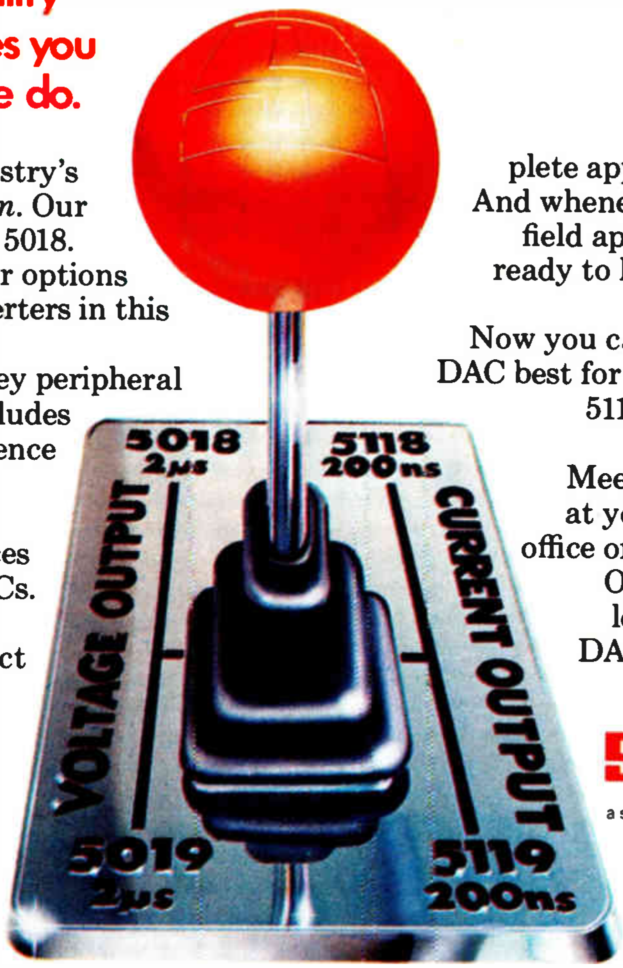
The model 1040 data collector series features compact, portable (9-lb) devices particularly well suited for the display and printout of short-term test data. At about one fifth the cost of more elaborate data loggers, the 1040 has a typical unit price of $884. Various models record such laboratory and industrial measurement parameters as temperature, flow, voltage, strain, and optical density. These versatile data loggers can be triggered either by an internal timer, a real-time clock accessory unit, or an external switch closure or computer.

An associated digital multiplexer allows the 1040 to read up to 10 remote digital panel meters. Alternatively, a maximum of five analog multiplexers can be stacked in one 1040 unit, permitting input from up to 50 analog sensors.

Precision Digital Corp., 368 Hillside Ave., Needham, Mass. 02194. Phone (617) 449-2265 [387]

Signetics is 1st, 2nd, 3rd and 4th in DAC systems.

For true μP-compatibility in DACs, nobody gives you more options than we do.



We brought you the industry's first monolithic DAC *system*. Our microprocessor-compatible 5018.

Now we've increased your options with three more 8-bit converters in this single-chip series.

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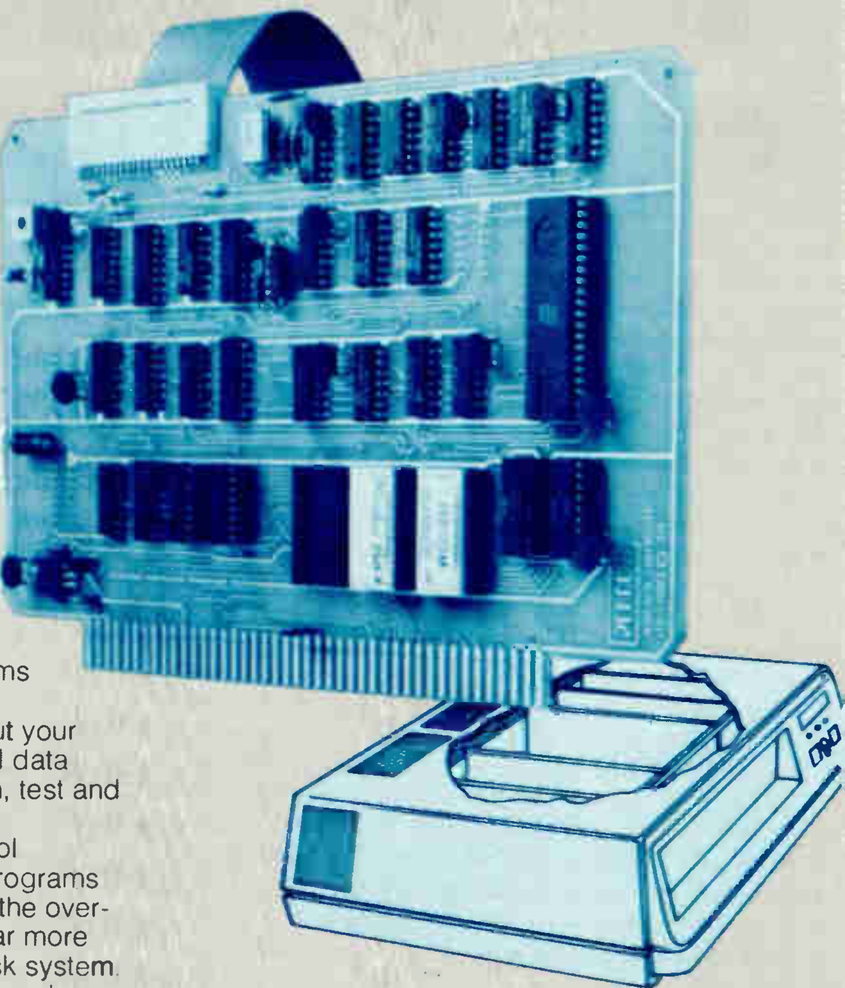

One-, two- and three-drive systems. Prices start at only $649.95, complete. Software support includes a ROM DOS on the controller — at no extra cost, advanced DOS and file management systems, a data base manager, assembly language program development aids and Percom Super BASIC.

Fast mini-disk data storage and retrieval make your EXORciser* or Micromodule* an efficient general purpose unit that's far more than a development system.

And now you can get affordable mini-disk systems and support software from Percom. Add 102K bytes of formatted, on-line disk capacity for only $649.95; add as much as 600K bytes for only $2245.95. Moreover, programs on disk start as low as $25.95.

With fast, random access storage you can put your development system to work in any of the myriad data capture or data retrieval applications of research, test and production environments.

Even if you use a mini-disk *only* to load control programs you'll save. Simply because loading programs from tape is awkward and time consuming. And the overhead of burning PROMs can quickly add up to far more than the price of an inexpensive Percom mini-disk system.

And consider this. At Percom's low hardware and software prices it becomes economical to not only develop your systems on an EXORciser* or Micromodule*, but to continue to use the same development system components as the final working system. The savings in training and documentation costs alone would be substantial.

An EXORciser* or Micromodule* with a low cost Percom disk system that's backed by Percom's low-cost software would also serve admirably as a rugged general purpose computer for individuals and small businesses. In other words, you'd have industrial quality at personal computing prices.

PRICES

Model	1-drive system	2-drive system	3-drive system
LFD-400EX™	$649.95	$1049.95	$1449.95
LFD-800EX™	$945.95	$1599.95	$2245.95

Single-quantity prices of mini-disk systems are set forth above. A system includes (1) the drives with integral power supplies — Percom's husky, open-frame PS-401 units — mounted in an enamel-finished enclosure, (2) the controller PC card for the EXORciser*/Micromodule* bus with an on-board ROM DOS, (3) an interconnecting cable and (4) a comprehensive users manual documenting operation, software and equipment. LFD-400EX™ drives have 40 tracks and store 102K bytes of formatted data. Both sides of a minidiskette may be used for storage with a -400EX model. LFD-800EX™ drives have 77 tracks and store 200K bytes.

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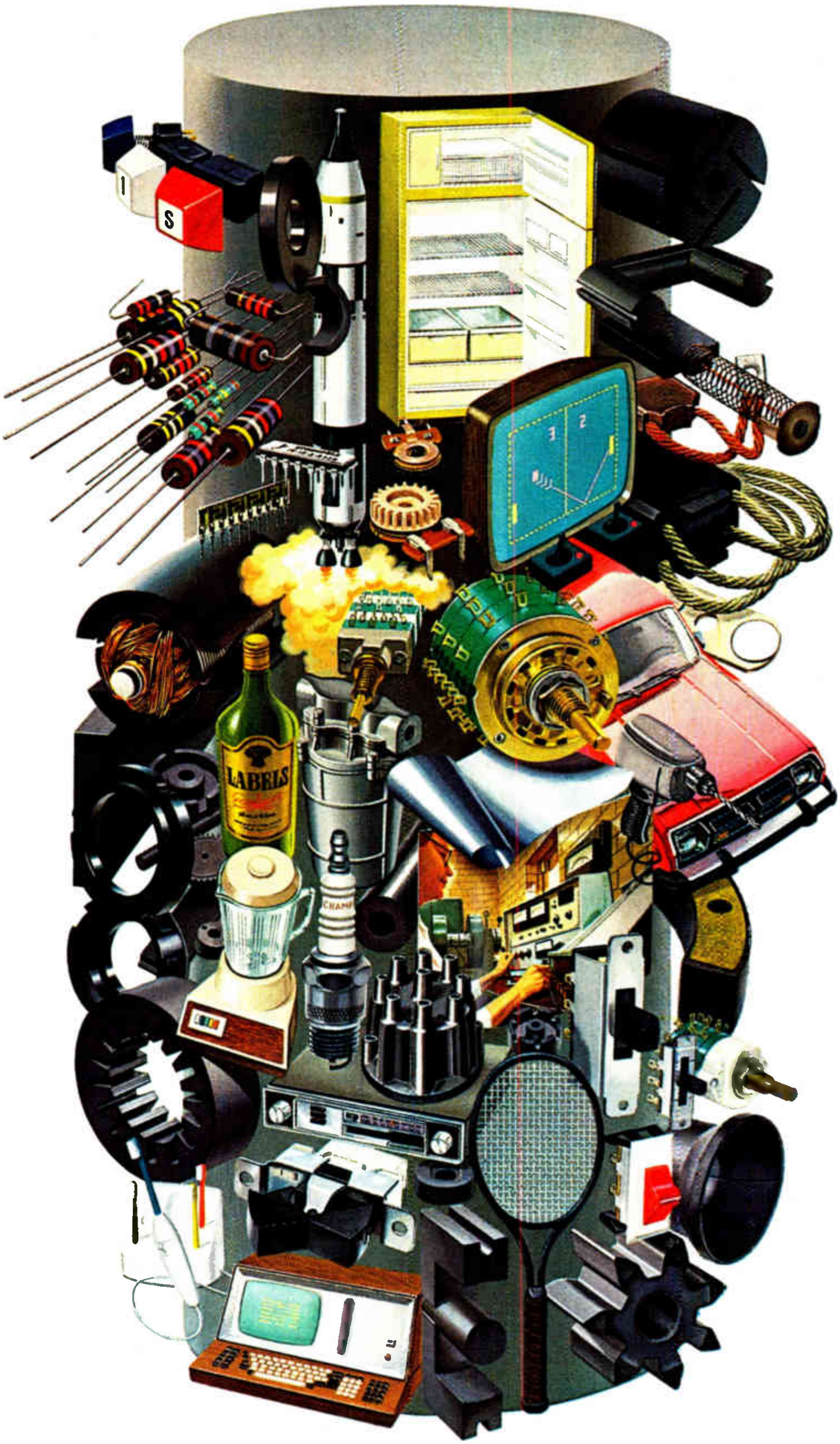
What is a Stackpole?



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"Most important is how well your component fits in with our overall design. Can you help?"

We can. Because at Stackpole we understand the concerns of electronic design engineers. And we can help by supplying a variety of standard as well as custom components that are flexible and adaptable, for more specialized jobs.

More than just an electronics company

A half-century of component manufacturing experience has made us the world's largest producer of slide switches for commercial applications. And we produce millions of rotary, rocker and key switches annually.

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Our carbon-comp, carbon-film, industrial and special-purpose resistors, as well as our resistor networks, are integral parts of the electrical and electronic products we all use every day.

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More than just another source.

As a result of our manufacturing expertise and electronics know-how, we're capable of meeting your specific design needs. Whether your concern is switching, resistance or ferromagnetics, Stackpole has both the products and a special willingness to help solve your component and materials problems.

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Micro power

The first modular 2400 bps modem. That's Rockwell Micropower.

Now you can easily and economically integrate a 2400 bps modem within the functional system of terminals or communications equipment.

The reason — the versatile design of Rockwell's R24, a synchronous MOS-LSI modem. The R24 divides its functions into three modules: one for the transmitter and two for the receiver.

Each module is encased in a plastic package that can be plugged into standard connectors or wave soldered onto system PC boards. Total module area required is only about 25 sq. inches.

R24 gives designers functional flexibility, too. It's Bell 201 B/C and CCITT V.26 and V.26 bis compatible. And with a minimum of interfacing circuitry, it can be configured for operation on leased lines or the general switched network.

Rockwell gets you started in performance analysis and system design with an R24 modem on an evaluation board. Everything you need for your prototype design.

A new generation of modems from the leading OEM manufacturer of high speed LSI modems. That's Rockwell Micropower working for you.

For more information, contact D-727-F8 Microelectronic Devices, Rockwell International; P.O. Box 3669, Anaheim, CA 92803, or phone (714) 632-3729.

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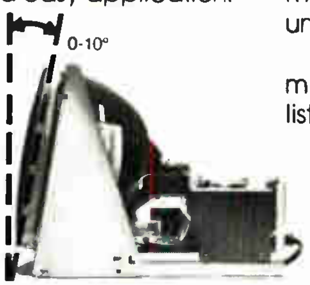
...where science gets down to business

There's a bright new face in 12" data monitors.

If you've got a need for a 12" CRT monitor, Sanyo has a model that will fill it.

For cost-sensitive applications, choose the 5000 series. You get your choice of AC or DC power, P4 or P31 phosphors, and separate or composite video and sync inputs. 15 MHz bandwidth and standard 15.75 kHz scan rate provide excellent resolution and easy application.

For extra-demanding jobs, pick the 6000 series. You get 1,000 line resolution and 22 MHz bandwidth for ultra-sharp graphics and crisp, high definition 80-character lines. TTL-compatible sync inputs make interfacing a snap.



With either series, you get a compact, rugged steel chassis with adjustable CRT tiltback to fit virtually any enclosure design. You also get adjustable scan size, plus remote brightness control capability. Single-PCB construction and one-connector hookup save time in assembly, testing, and maintenance. And Sanyo's many years of manufacturing field-proven CCTV monitors, and our unparalleled QC assure long, trouble-free service.

For all the facts on these exciting new open-chassis monitors, contact your local Sanyo sales representative listed below.

SANYO

Communications Products Division
1200 W. Artesia Blvd., Compton, CA 90220 (213) 537-5830

Contact your nearest Sanyo rep:
AKRON: Avcom, Inc. (216) 777-2060 **ATLANTA:** Len Elliott Company (404) 875-9701 **ATLANTIC CITY:** Austin Associates (609) 871-9290 **BALTIMORE:** David H. Brothers, Inc. (301) 764-7189 **BOSTON:** Piper Associates (617) 449-1144 **CHICAGO:** George Petit Company, Inc. (312) 261-0342 **DALLAS:** The Crockett Sales Co. (214) 748-8209 **DENVER:** Mile-High Marketing (303) 457-2058 **DETROIT:** Burcaw Co. & Associates (313) 533-7700 **INDIANAPOLIS:** Midwest Rep. & Assoc., Inc. (317) 844-4555 **KANSAS CITY:** Pacer Sales Corporation (816) 358-6638 **LOS ANGELES:** Marketing Specialists (213) 341-1471 **MIAMI:** L. Haas Company (305) 945-6544 **PORTLAND:** Earl & Brown Co., Inc. (503) 245-2283 **SAN FRANCISCO:** Tech-Rep Associates (415) 785-4531 **SEATTLE:** Earl & Brown Co., Inc. (206) 284-1121 **ST. PAUL:** Skor, Inc. (612) 645-6461 **WHITE PLAINS:** Irving Langbaum Assoc., Inc. (914) 634-1141

Circle 211 on reader service card

Semiconductors

Converter has 97% efficiency

C-MOS device multiplies input voltage by $-1 \pm 0.1\%$ and delivers up to 20 mA

Capitalizing on its considerable experience with complementary-MOS circuitry, Intersil has developed a dc-dc voltage converter that accepts input voltages from +1.5 to +9 V dc and delivers an output that is equal to the negative of the input to within 0.1%. What's more, the device, which can put out about 20 mA, has an efficiency of approximately 97% for load currents of 2 mA and greater [*Electronics*, Sept. 27, 1979, p. 33].

Because of its unique combination of attributes, Intersil believes the ICL7660 will find applications in low-power signal-processing systems, data-acquisition systems, inexpensive negative power supplies, simple voltage multipliers, and even conventional operational-amplifier circuitry, which often requires both positive and negative supplies.

Besides its premier efficiency rating, the 7660 has other features aimed at attracting a diversity of users. For one thing, according to engineering manager David Bingham, it is easy to use because it requires only two external capacitors. It is also protected against short circuits and static discharge.

Bingham says that in designing the unique device, he used a "lot of past experience," circuit tricks, and an "understanding of the four-layer action of the C-MOS process." The 7660 also had to be latch-up–proof, and C-MOS is tricky that way, he points out.

Body snatcher. Bingham put onto the chip a series dc power supply, an RC oscillator, level-changing transistors, a thermal shut-down circuit, four output power MOS switches, and what he calls a "body snatcher" logic section. This section, he explains, senses the most negative voltage at any point in the device and ensures that the bodies of the n-channel output switches are never forward-biased. The rest of the circuitry the company considers to be proprietary.

The 7660 is designed to supply up to 20 mA, but users who need more current can connect two or more in parallel, Bingham points out. Because the converter allows access to +V and −V, where V is the input voltage, it may be used as a voltage doubler in some situations. Further, although the C-MOS circuitry itself is limited to an absolute maximum of 18 V, several of the 7660s can be made into a ladderlike circuit, "so that you can multiply up to 50 V, if you want to," Bingham says.

The ICL7660, one of a new series of power-supply parts trademarked MaxCMOS, comes in three versions. The CPA, in an eight-lead miniature dual in-line package, covers the commercial temperature range; the CTY covers the same range, but in a TO-99 can; and the MTY, also in a TO-99 can covers the military range.

The price for the plastic miniDIP 7660CPA will be $1.25 each in hundreds. Availability is slated for distributor stock in November.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [411]

Power transistors work in 900-MHz band at up to 40 W

Eight newly announced power transistors for operation in the 900-MHz band span a 1-to-40-W output range. The MRF800 family has guaranteed performance at 870 MHz; its members are designed for 12.5-V, large-signal-amplifier applications in industrial and commercial fm equipment operating in the 806-to-947-MHz range.

Characterized for Class C amplifier service in mobile fm transmitters, these devices are tested for burn-out at a 15.5-V supply voltage, with 50% rf overdrive and a load with a 20:1 standing-wave ratio. The units have an all-gold–metallization construction with emitter ballasting and silicon nitride passivation.

The MRF838/A and the similar MRF870/A are 1-W and 3-W output parts, respectively, and have been designed for common-emitter applications. The 10-W, 20-W, 30-W, and 40-W output units—the MRF840, 842, 844, and 846—are connected for common-base operation in the internally matched-input (controlled-Q) CS-12 package.

Power gain varies from a low of 4.3 dB for the 40-W output model MRF846 (priced, in 100s, at $32) to a high of 6.5 dB for the 1.0-W output 838 (priced at $4.90). The units are available from stock.

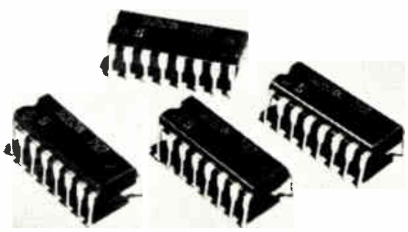
Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone Alan Wagstaffe at (602) 244-6900 [414]

ICs provide control for switched-mode supplies

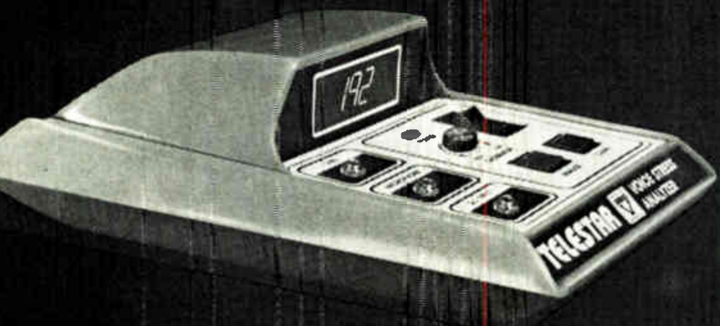
The members of a series of switched-mode power-supply circuits can be used to maximize efficiencies in forward, flyback, and push-pull converters. Packing all the control circuitry needed for a power-supply inverter or switching regulator onto single monolithic chips, the SG1524, 2524, and 3524 feature complete pulse-width-modulation control circuitry, single-ended or push-pull outputs, and line and load regulation of 0.2%. Total supply current is less than 10 mA with an operating frequency beyond 100 kHz.

The 1524 is specified for operation over the −55° to +125°C military range, while both the 2524 and 3524 operate over the commercial range of 0° to 70°C.

Included in the 16-pin, dual in-



NEW ELECTRONIC TRUTH DETECTOR MONITORS THE HUMAN VOICE!



THE TRUTH MACHINE T.M.

It gives you an honest answer even if someone else doesn't!

Now you can detect deception with the push of a button. . .anytime, anywhere. The Truth Machine is a new generation voice stress analyzer that is so compact, lightweight, and portable that it easily fits into your desk drawer or briefcase.

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TODAY YOU NEED A TRUTH MACHINE

You succeed by knowing the answers. By making the right decisions. To make the right decision you need the facts. . .you must know the whole truth. But unfortunately, almost everyone you deal with has a motive to practice at least some deception. Unless you're a mind reader you never know whether or not you're getting a straight answer when you ask:

* Is this your lowest price. . .your best offer?
* Have you mailed that check to me yet?
* Can you deliver my order on time?
* Have you told me everything I need to know?
* Can I depend on you?
* Are these figures correct?
* Are you confident about this investment?
* Will they settle out of court?

When you ask a direct question you deserve a straight answer. And that's the beauty of the Truth Machine; it will give you a straight answer. . .even if someone else doesn't. It's your best possible defense against doubt, risk, and deception.

YES, IT'S ETHICAL!

It's simply a fast, efficient way to verify the truth and protect yourself against dishonesty. And after all, which is immoral - for a person to be deceitful or to have their dishonesty uncovered? There is nothing unethical about uncovering deceit and deception. In fact, you can usually prevent dishonesty simply by letting everyone know that you own the Truth Machine. It's a powerful deterrent for anyone who is tempted to mislead you or tell you less than the truth!

IT'S AMAZINGLY SIMPLE!

Like many technological discoveries, voice stress analyzers grew out of military research during the Vietnam war. Army intelligence needed something better than the standard polygraph to interrogate prisoners. A simple method that could be used without the subject's knowledge. The voice stress analyzer was the result!

The principle is remarkably simple. Scientists already knew lying produced unconscious and uncontrollable stress that could be recorded by a polygraph. Researchers soon discovered that this stress also affected the muscles controlling the vocal cords, and caused an inaudible "microtremor" in the voice. All that was needed was a device sensitive enough to pick up and record these inaudible vibrations. And that was a relatively easy accomplishment considering the state of modern electronic technology.

BUSINESSMEN BECOME MIND READERS

In addition to police and intelligence agencies, many of the "Fortune 500"corporations have quietly been using voice stress analyzers for several years. Large industrial and retail companies use it to control employee theft and screen job applicants. And dozens of large insurance companies have been using voice stress analyzers to uncover false claims. They simply tape an interview with anyone filing a suspicious claim, then play back the recording and monitor it with a voice stress analyzer.

In the past only the largest, most profitable companies felt they could justify spending $1500 to $5000 to purchase a voice stress analyzer. However, like everything else in the electronics field, these high prices reflect the heritage of a prototype, and not the quality of a reliable voice stress analyzer.

The new cost-saving, solid state, micro-chip technology and mass production have made voice stress analyzers affordable. Today, for only $149.00 you can have a compact unit that is far more sensitive than the top-secret units originally used by the military! There is no better way to get at the truth. . .and remove the risk and uncertainty from those important decisions that face you every day!

AND IT'S ENTERTAINING!

Because it can pick up and analyze any audible statement, use of the Truth Machine is limited only to your imagination. Seeing the stress reading go wild when politicians and celebrities give their 'candid' views during television press conferences and talk shows can provide you with hours of amusement, and some very important insight. You can have the satisfaction of knowing the real truth about the energy crisis. . .what people in power really expect from the economy. . .how safe experts actually think you are from a nuclear power plant. . .and you'll find the real truth behind many intriguing and controversial people in the news. You may be surprised!

EASY TO OPERATE!

Unlike the polygraph, there are no sophisticated operating techniques to learn. With our easy, step-by-step instruction manual you can easily master the Truth Machine with only a few hours of practice. You simply turn it on and adjust the sensitivity calibrator knob for average stress in the speaker's voice. Then sit back and watch the LED display. When the numbers on the digital read-out reach the stress area, you know you're hearing less than the truth. And it's versatile. You can pick up the speaker's voice with the Truth Machine's ultra-sensitive microphone. Or use the special sensor that connects it to your telephone. You can even tape a conversation with any standard tape recorder and analyze it at your convenience by attaching the special output jack and playing back the tape!

DEPENDABLE QUALITY

The Truth Machine from Telestar is the ultimate voice stress analyzer. It features solid state electronics and is manufactured to the highest technological standards. Even its tough shatterproof case was designed to withstand the roughest handling. The Truth Machine is designed and built to guarantee you years of dependable use. It should never need servicing. But if anything ever does go wrong, we will repair it through our service-by-mail center and return it to you in a matter of days.

USE IT RISK FREE!

We would like you to use the Truth Machine without obligation for 30 days. Experience its advantages. Take it to the office and enjoy surprising people with your infallible new 'insight'. Use it at home for entertainment and add a whole new dimension to your television viewing pleasure. If you don't agree that being free of doubt makes it possible for you to really relax and enjoy life more. .simply return it within 30 days for a prompt, courteous refund.

* Consent of all parties must be obtained for use in Pennsylvania.

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200 S. Front St, Wormleysburg, PA 17043**

Circle 213 on reader service card

line package are voltage reference, oscillator, error amplifier, and current-limiting output circuits, plus a pulse-steering flip-flop. An internal series regulator generates a nominal 5-v output, which is used to generate a reference voltage and serves as the regulated source for all internal timing and circuit control.

Two identical npn transistors with uncommitted collectors and emitters act as output circuits. Each output transistor has antisaturation circuitry to provide fast response, as well as current limiting set to provide a maximum output current of approximately 100 mA. The error amplifier is of the differential-input, transconductance type.

All three models are available from stock. In quantities of 100 or more, price begins at $4.00 each for the plastic, commercial temperature range products.

Signetics, 811 East Arques Ave., P. O. Box 9052, Sunnyvale, Calif. 94086. Phone (408) 746-1836 [413]

SCR, diode bridge circuits have low thermal resistance

Rated to 25 A, the B series of Powertherm silicon controlled rectifier and diode bridge circuits has sufficient power to provide phase control for a 2-hp motor. The devices have low thermal resistances because their ceramic bases interface directly with heat-sink mounting surfaces. Junction temperatures have been measured at 10°C less than those of units with metal heat plates. And a patented process for the internal connections to the chips allows for a minimum number of bonds.

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To serve these 6 functions and guarantee your system reliability.

We offer 25 different solvent combinations for electronic cleaning, contact cleaning, tape head cleaning, flux removal, freezing and release agents for epoxy potting and for injection molding.

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2 Flux Removal	MS-190 Freon TMC Solvent — Flux Remover & Cleaner	MS-190HD Flux Remover & Cleaner — Heavy Duty
3 Contact Cleaning	MS-230 Contact Re-Nu® MS-238 Contact Re-Nu & Lube*®	
4 Tape Head Cleaning	MS-200 Magnetic Tape Head Cleaner	
5 Freezing	MS-240 Quik-Freeze®	
6 Release Agents	MS-122 Release Agent — Dry Lubricant For Cold Molds	MS-136 Release Agent For Injection Molding & Hot Molds

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LOS ANGELES • CHICAGO • DANBURY, CT • TORONTO wire leads that can terminate in a single molded socket—is offered as an option. A typical B series unit with two SCRs and three diodes sells for $8.00 in 1,000-piece quantities. The units are available from stock.

Gentron Corp., 6667 North Sidney Place, Milwaukee, Wis. 53209. Phone Lance Kaufman at (414) 351-1660 [415]

GaAs FET offers low noise, high gain from 2 to 12 GHz

Designed for such applications as land and satellite communications and radar, the recently introduced HFET-2202 is a low-noise, Schottky-gate gallium-arsenide field-effect transistor. Packaged in a 100-mil² hermetic metal and ceramic stripline package, the 0.5-by-250-μm-gate GaAs FET chip from Hewlett-Packard is a transistor with excellent noise and gain performance in the 2-to-12-GHz range. Typical noise figure values at frequencies of 4, 6, and 8 GHz are 1.1, 1.4, and 1.9 dB, respectively. Gains for the devices at these same frequencies are 13.6, 11.3, and 9.6 dB.

HP believes the FET will be especially useful in lower-frequency, narrow-band applications, such as the 3.7-to-4.2-GHz telecommunications band. In fact, at 4 GHz the company has set radio-frequency guarantees at 1.4 dB for the maximum noise figure and 12.0 dB for the minimum associated gain.

In quantities of one to nine, the HFET-2202 sells for $115, while in quantities of 10 to 49, the price drops to $98. The units are available from stock.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [416]

Passivation process cuts rectifier packaging costs

Because of a metal-oxide-passivated-silicon (MOPS) process, newly announced rectifiers from Codi Corp. boast performance levels comparable to those of rectifiers hermetically

ANRITSU'S MULTI-PACKAGE.

Our new Frequency Counters MF57A/MF63A pack a lot of functions in one cabinet.

Take a close look at our new MF57A/MF63A and you'll see some functions you won't see on an ordinary frequency counter. Functions like BURST, which permits measurement of intermittent signals like pulsed RF signals. And MULTI, for high resolution of 0.0001 Hz at audio frequencies from 50 Hz to 10 kHz. Then, of course, there's an AGC for effective measurement of noisy signals.

The bright, green LED display has two decimal point positions (one for MHz and one for kHz) and is easy to read in all lighting conditions. So consider all the features. Then add the time and money you'll save, and we think when it's time for counting frequency, you can count on Anritsu.

	MF57A	MF63A
Frequency Range	10 Hz to 600 MHz	10 Hz to 1,000 MHz
Maximum Sensitivity	10 mVrms	
Digit	9 digits	
Display	7-segment LED, zero-blanking, memory display	
Reference Crystal Oscillator:* Aging Rate	$\leqq 2 \times 10^{-8}$/day	
Power AC90-140V (180-280V), 50/60 Hz	≦28 VA (100/200 V) (≦33 VA warm-up)	
Dimensions/Weight	85(H)×205(W)×280(D)mm, ≦4 kg	

* Four types of crystal oscillators are optionally available.

For comprehensive literature on the Frequency Counter, contact—

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Circle 217 on reader service card

sealed in glass, even though they may be packaged only in inexpensive transfer-molded epoxy cases. These MOPS devices use a hard, glassy oxide-passivation technique that greatly improves the reliability of the rectifier and diode junctions.

The metal oxide is formed over the critical junction areas on the perimeter of the silicon chip at temperatures above 600°C. This oxide, which fully wets and covers the exposed junction, is far more stable and rugged than the organic material it replaces, particularly at high temperatures. The MOPS process seals the chip against increases in reverse leakage induced by humidity or temperature.

Currently the company is using the process on its line of 1- and 3-A axial-lead single-junction rectifiers, with peak inverse voltage ratings to 1,200 V. The company is also changing over its line of full-wave rectifier bridge assemblies to use MOPS chips. In 1,000-unit quantities, a 3-A, 600-V axial-lead rectifier sells for 31¢, and a 10-A, 400-V full-wave rectifier for $1.85, with delivery from stock to six weeks.

Codi Semiconductor Inc., Pollitt Drive, Fair Lawn, N. J. 07410. Phone Bill Adikes at (201) 797-3900 [417]

TI introduces 8-K E-PROM with 250-ns access time

Featuring a maximum access time of 250 ns, a new 8-K erasable programmable read-only memory (E-PROM) from Texas Instruments requires only a single 5-V power supply. The TMS2508 offers automatic chip-select and power-down, low power dissipation, and fully static operation. Data stored in the device is erasable by ultraviolet light. Programmable either singly or in blocks, sequentially or at random, the device is fully compatible with other members of TI's TMS2500 family. In 100-unit quantities, the TMS2508 sells for $36.90.

Texas Instruments Inc., MOS Memory Division, P. O. Box 1443, M/S 6955, Houston, Texas 77001 [418]

Communications

Meter measures PCM jitter

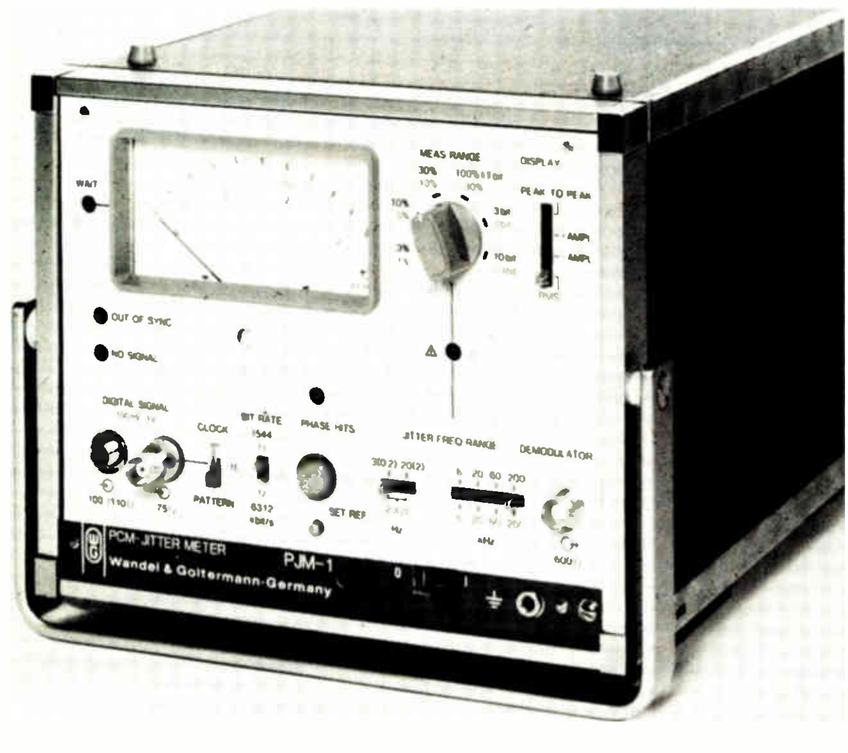
Direct-reading instrument combines broad bandwidth with wide dynamic range

Timing jitter—an important cause of errors in data-transmission systems—has always been a difficult parameter to get a handle on because measuring it has been a subjective process. The procedure involves displaying the bit stream on an oscilloscope and studying it; thus the measurement error includes the scope error, which is known, and the operator error, which is not.

Now a direct-reading analog jitter meter from W & G Instruments eliminates this problem by determining and displaying timing jitter on T1, T1C, and T2 pulse-code-modulation systems. The PJM-1 can handle any two of three standard bit rates: 1,544, 3,152, or 6,312 kilobits per second. It has six jitter amplitude scales, ranging from 3% of a bit full scale to 10 bits full scale, in a 1-3-10-30 progression. The upper frequency limit of the measured jitter is switch-selectable to be 6, 20, 60, or 200 kHz, and the lower limit may be set at either 0.2 or 2.0 Hz.

The PJM-1 does more than just measure peak-to-peak jitter. It also determines and displays the negative-peak, positive-peak, and root-mean-square values of the jitter it sees. By providing all of this information, the meter gives the operator valuable clues about the source of the jitter. To aid system diagnosis further, it makes the demodulated jitter signal available at a 600-Ω output for connection to another instrument, such as a spectrum analyzer.

Compatible with all standard PCM equipment, the German-made instrument has 100-Ω balanced and 75-Ω unbalanced inputs; a high-impedance bridging probe is offered as an option. Voltages between 100 mV and 3 V are required for proper operation of the meter; if no measurable signal is present, a front-panel indicator lamp advises the operator of the fact. Another lamp warns of a phase hit whenever the jitter exceeds a preset limit.



The PJM-1 measures 11 by 9 by 18 in. and weighs 20 lb. It operates from 45° to 104°F and consumes about 60 W. The unit runs on any standard voltage between 110 and 240 V ac. It is available now.

W & G Instruments Inc., 119 Naylon Ave., Livingston, N.J. 07039. Phone (201) 994-0854 [401]

X.25 simulator and tester eases U. S. users' networking

A multipurpose, microprocessor-based X.25 protocol simulator and tester has just been introduced in the U. S. for common carriers and network suppliers, as well as for manufacturers of X.25-compatible terminals and other equipment. The tester interfaces directly with terminals and front-end processors, or it can be operated remotely over full-duplex synchronous lines using modems. The console can also be used remotely from the unit via asynchronous lines.

Both data-terminal equipment (DTE) and data-circuit–terminating equipment (DCE) are simulated in four different modes: the frame manual test allows the user to enter frames through the terminal; the frame automatic test implements an automatic data generator to allow the user to send frames at any specified rate; the packet-level test sends packets typed on the terminal (in this mode the frame level is handled automatically); and the interactive terminal interface (ITI) test. The DTE and DCE parameters are simu-

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lated at any speed as long as the unit under test can be externally clocked. In the line-monitor mode, the device handles all common baud rates up to 19,200; the interface with the console can be operated asynchronously at up to 9,600 bits/s.

With an optional cathode-ray-tube console, the simulator-tester can monitor the information chain that the DTE computer would be exchanging with a network. For interfacing with a CRT, it has powerful operating commands for control of protocol parameters, frame and packet functions, and data and error-condition generation. Any errors caused by the specific piece of equipment under test are also signaled.

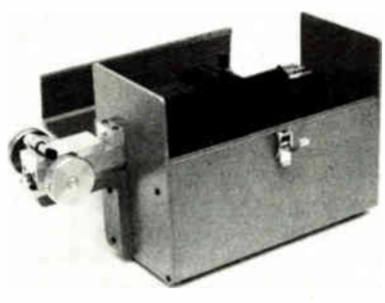
The simulator-tester is priced at $11,900 and is available within 60 days.

Applied Data Communications, 14272 Chambers Rd., Tustin, Calif. 92680. Phone (714) 731-9000 [404]

Unit determines attenuation in fiber-optic cable

Measuring the length of fiber-optic cable, the model 401 Optical Time Domain Reflectometer can precisely locate breaks, connectors, and splices in the cable. Using the Rayleigh back-scattering technique, overall cable attenuation and local attenuation at a defect can be measured from one end. Breaks less than 40 cm from the input end can also be detected.

Used in conjunction with a wide-band oscilloscope, the 401 is portable and may be operated on a 110-V, 60-Hz power supply or on an exter-



nal 12-V dc source. The dynamic range of the instrument is over 60 dB. Unterminated fibers of various sizes may be measured; if they are terminated, adapters for all major connectors may be ordered.

Applications include monitoring cable installations, as well as use in some manufacturing and laboratory environments. The unit sells for $5,800. Delivery is within 60 days.

Optixx, 7220 Owensmouth Ave., Suite 105, Canoga Park, Calif. 91303. Phone Jack Buhn at (213) 340-9532 [406]

Noise source improves SWR and ENR specifications

The recently introduced solid-state HP 346B noise source—operating from 10 MHz to 18 GHz—offers improvements in two specification

areas for accurate noise-figure measurements. The first lowers the standing-wave ratio (SWR) to less than 1.3 over the 10-to-30-MHz range, to less than 1.15 for 30 MHz to 5 GHz, and to less than 1.25 over the 5-to-18-GHz range. The second measures and charts excess noise ratio (ENR) at 20 individual cardinal frequencies for each source. The root-sum-of-squares uncertainty of each of these ENR calibration points varies from ±0.1 dB at 10 MHz to ±0.19 dB at 18 GHz. Nominal excess noise is 15.2 dB.

Higher measurement accuracy may be obtained by using a power meter technique to measure the Y factor and a desktop computer to operate the instrument automatically and to compute the noise figure. Using an HP 436A digital power meter and a table of excess noise corrections from the calibra-


Ten years ago, Advanced Micro Devices had no products, zero sales and eight of the best people in the business.
Today, Advanced Micro Devices has more than 600 products, $200 million in sales and 8,000 of the best people in the business.
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tion report furnished with each noise source, instrumentation error can be as low as ±0.04 dB. With improved ENR accuracy and lower mismatching, overall uncertainty can be below ±1.0 dB.

The 346B sells for $1,200. Delivery takes up to four weeks.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [407]

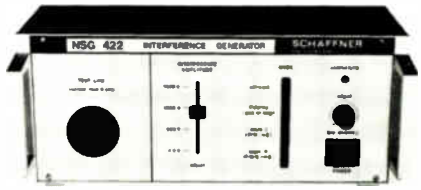
Line interference simulator's spikes aid designers

Producing interference spikes similar to those typically produced by switches, relays, and so on, the Schaffner NSG 422 line-interference simulator—generating pulses of up to 300 MHz—enables equipment designers to create equipment configurations with maximum interference immunity. The simulator also lets them trace interference-sensitive components and take necessary suppression measures before the product reaches the market. Typical instrumentation that could be affected by interference spikes includes microprocessors, controllers, data transmission units, and security systems.

The fast, low-energy interference spikes can be either positive or negative. A free-running oscillator enables the spike to be superimposed on the power-line input over an entire sinusoidal waveform, and a filter in the unit ensures that the interference generated is not reflected back into the power lines. Designed for a load of up to 6 A, the simulator directly powers the equipment or sub-units under test.

The NSG 422 line interference simulator sells for $2,300, with delivery from stock.

Rohde & Schwarz Sales Co., 14 Gloria Ln., Fairfield, N. J. 07006. Phone Carroll Barlow at (201) 575-0750 [408]



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The new AO STEREOSTAR® Zoom "T" microscope features the "T" zoom body with coaxial illumination and photo capabilities. It may be just what you need to boost output in your production, assembly or inspection department.

Like no other stereozoom microscope, the Zoom "T" gives you a constant 4" of working room. It has a 1x - 6x magnification range, and with auxiliary lenses and eyepieces it offers a total range of 5x - 300x. Magnification can be conveniently changed with controls on both sides of the body. No matter what magnification you're working with, you get crisp, sharp image definition.

Modular in construction, the Zoom "T" can be ordered with or without the coaxial illuminator. In fact, any accessory can be simply added at any time. However, if you're working with highly reflective opaque surfaces, coaxial illumination is invaluable because it gives contrast without hot spots, glare, reflections or shadows.

We invite you to compare the new AO STEREOSTAR Zoom "T" microscope, feature by feature, with any other competitive microscope.

We're confident you'll immediately see that it offers the outstanding value in its field. See your AO dealer or representative for a demonstration. Or write for a detailed brochure. American Optical, Scientific Instrument Division, Buffalo, NY 14215.

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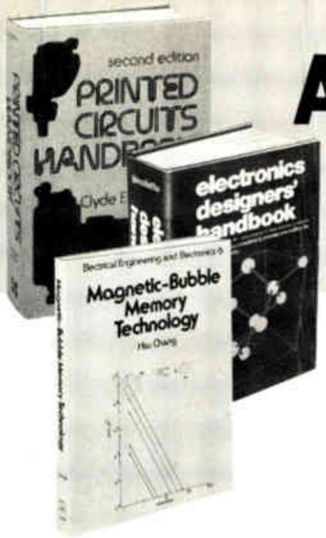

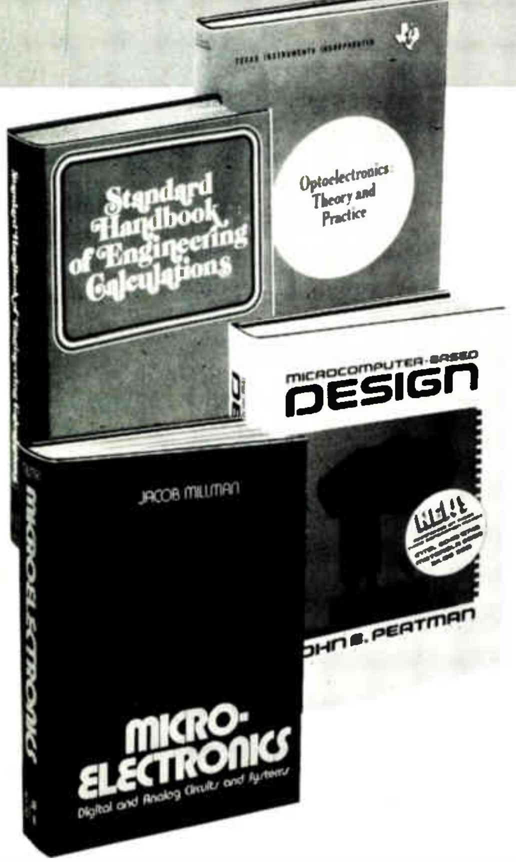

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ELECTRONIC DISPLAYS. By E. G. Bylander, Texas Instruments Incorporated, *172 pp., illus*. The book describes current electronic displays by family types, discussing all aspects of their operation, application, and circuit requirements. You cover photometry and contrast enhancement, together with the fundamentals of such critical components as mounts and drives, interface requirements, and other necessary engineering information.
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DIGITAL FILTERS. By A. Antoniou, *524 pp., illus*. This all-inclusive, up-to-date treatment guarantees your thorough understanding of today's digital filters and the theories, techniques, and procedures you'll be using in their analysis, design, and implementation. The book gives you many design examples, together with the numerous possible approaches and engineering tradeoffs relating to their hardware implementation.
021/171 Pub. Pr., $23.95 Club Pr., $18.50

BUCHSBAUM'S COMPLETE HANDBOOK OF PRACTICAL ELECTRONIC REFERENCE DATA. By W. H. Buchsbaum, *2nd Ed., 645 pp., 371 illus., 70 tables*. It gives you all the technical electronic information you need—from the factual foundations of electronics to the latest technical advances in optoelectronics, large scale integrated circuits, digital logic, microprocessors, and computers. Hundreds of formulas, graphs, charts, and tables.
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RADIO HANDBOOK. By W. I. Orr, *21st Ed., 1,135 pp., 1,364 illus*. Now completely updated, expanded, and more deserving than ever this profusely illustrated reference gives you everything you need to know to understand, design, use, and experiment with every circuit and piece of equipment. (All recent technological breakthroughs are covered).
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TRANSFORMER AND INDUCTOR DESIGN HANDBOOK. By W. T. McLyman, *428 pp., illus*. User-oriented throughout, it covers everything from transformer design and inductor design with dc, power inductor design, designing for regulation, inductor design without dc, constant voltage transformer, current and three-phase transformer, to application of magnetic components in power electronics.
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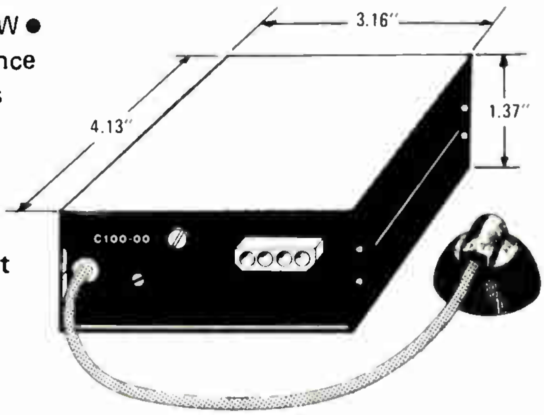

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Products newsletter

TO-220 thyristors and SCRs reach 2.5-kV isolation

Users of TO-220 silicon controlled rectifiers can now depend on stand-alone 2.5-kV dielectric isolation from the Thermotab family of thyristors introduced at Wescon by the semiconductor division of Teccor. Until now, the only way to get so substantial an isolation with the small TO-220 case was to mount it on a large external alumina substrate—effectively diluting much of its size advantage. **The Irving, Texas, firm achieved this isolation by mounting the alumina substrate internally.** The devices are rated from 1.6 to 20A and are available in four to six weeks. Devices with 4-kV isolation are also available, through screening, within six to eight weeks.

Ballantine to sell Iwatsu line in U. S.

An ageement between Ballantine Laboratories Inc., Boonton, N. J., and Iwatsu Electric Co. Ltd., Tokyo, **provides for the American firm to sell selected Iwatsu test and measuring instruments in this country.** The first product to be so marketed will be a 40-MHz dual-trace oscilloscope, which will be designated the Ballantine 1042A.

Test chamber measures 64 ft³

A 64-cubic-foot environment test chamber has been added to the line of chambers made by Associated Environmental Systems, a subsidiary of Walter Kidde & Co. The model BK-1164 **has a temperature range of −100°F to +425°F and features a control stability of ±0.5°F over its entire operating range.** The chamber, which works with either liquid carbon dioxide or liquid nitrogen, gets down to −100°F in 12 minutes. The Lawrence, Mass., company makes similar chambers with capacities of 2, 4, 8, and 27 ft³. Prices for the BK-1164 start at $6,400, and the chamber has a 30-day delivery time.

Interface boards drive both Japanese and U. S. printers

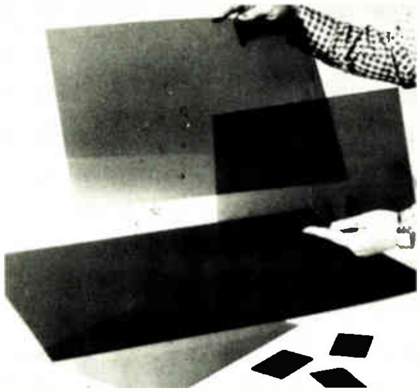
Microprocessor-based, single-board interfaces for use with the dot-matrix impact printers in Japan's C. Itoh Electronics' Epson series 200 have recently been introduced by Interface Electronics. **Based on Mostek's 3870, the HIF-200 interface boards allow full 96-character ASCII printing on the 27-column Itoh/Epson 210, 220, and 240 printers.** Using either serial- or parallel-selectable inputs to drive the printers via software control, the interfaces have head drivers and control logic—both easily programmable for use on domestic point-of-sale printers. With a programmed ability to set the head in an on or off position and to establish the buffer size automatically on power-up, the boards range in price from about $165 to $180, with large quantity discounts available. The Allston, Mass., division of Capital Circuits Corp. charges an engineering fee to adapt the boards to domestic printers.

Power-supply family serves many needs

Look for Boschert Inc. of Sunnyvale, Calif., to introduce a series of standard switching power supplies that can be **tailored to meet the wide-ranging requirements of domestic and international original-equipment manufacturers with no need to go to the expense of custom units.** The four-output supplies will be regulated to within ±3% for load-current variations over a 10:1 range and will accommodate input voltages from 90 to 265 V ac to satisfy user needs in the U. S., Japan, and British Commonwealth countries, among others.

New products/materials

Polycarbonate-base Chromafilter, available in sheet form, enhances the readability of electronic readout displays by improving their contrast and eliminating reflections and glare from external light sources. It also provides good resolution and protects the readout against marring and chemicals. The polycarbonate sheets offer excellent impact resistance, withstand temperatures up to 250°F, are highly resistant to ultraviolet radiation, and carry the UL 94 V-2 flammability rating.



Available on acrylic and rigid vinyl substrates, Chromafilter sheets come in sizes of 18 by 24 in. and 24 by 24 in. and thicknesses of 0.030 and 0.060 in. All materials and sizes are available for immediate delivery from the factory.

Panelgraphic Corp., 10 Henderson Dr., West Caldwell, N. J. 07006. Phone (201) 227-1500 [476]

A thixotropic ceramic adhesive for bonding resistance heaters is applied by means of production dispensing equipment. When dried and then cured at 200°F, Ceramabond 503-SHV has a temperature resistance up to 3,000°F. It has been used to bond nichrome resistance wires to mica and porcelain insulation for the heaters used in hair driers, toasters, radiant heaters, broilers, industrial hot air guns, and space heaters.

Ceramabond 503-SHV is available in small quantities from stock. Fifty-gallon lots, at $76 per gallon, have a delivery time of three weeks.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562. Phone (914) 762-0685 [477]

Perforated, conductive foam, CP105P Statfree, is an electrically conductive packaging material that protects devices against physical shock and static discharge. It is used for packaging integrated circuits, hybrid circuits, complementary-MOS microprocessor chips, and other devices sensitive to static electricity. The foam, which is unaffected by humidity, is perforated, enabling the user to separate integrated circuits into small packages. It is noncorrosive to IC leads to the extent laid down in MIL STD 883B, method 1004.2

Charleswater CP105P Statfree perforated conductive foam is available off the shelf in 12-by-24-in. and 24-by-24-in. pads with thicknesses of 0.25 and 0.50 in. It has a volume resistivity of less than 3×10^3 Ω-cm and a surface resistivity of less than 30×10^3 Ω/square. The foam sells for $10.50 per 12-by-24-in. pad (quantity discounts available). A nonperforated foam is also available.

Charleswater Products Inc., 87 Crescent Rd., Needham, Mass. 02194. Phone Katy Lehman at (617) 449-1811 [478]

Rush Dip Strip fused salts, for clean chemical wire stripping, can be used on all types of magnet wire, including copper-clad aluminum. The salts come ready to heat. They are poured into a solder pot for stripping. The wires may be pretwisted, coiled, or bundled together before stripping. For best results, the wires should be rinsed in warm water after stripping. Available in 2-lb bags, the salts sell for $6.60/lb. Two pounds is the minimum order.

The Eraser Co., P. O. Box 4961, Syracuse, N. Y. 13221. Phone (315) 454-3237 [479]

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Major fabricators and users of printed circuitry specify Norplex® laminates because of complete confidence in the uniform quality of our product.

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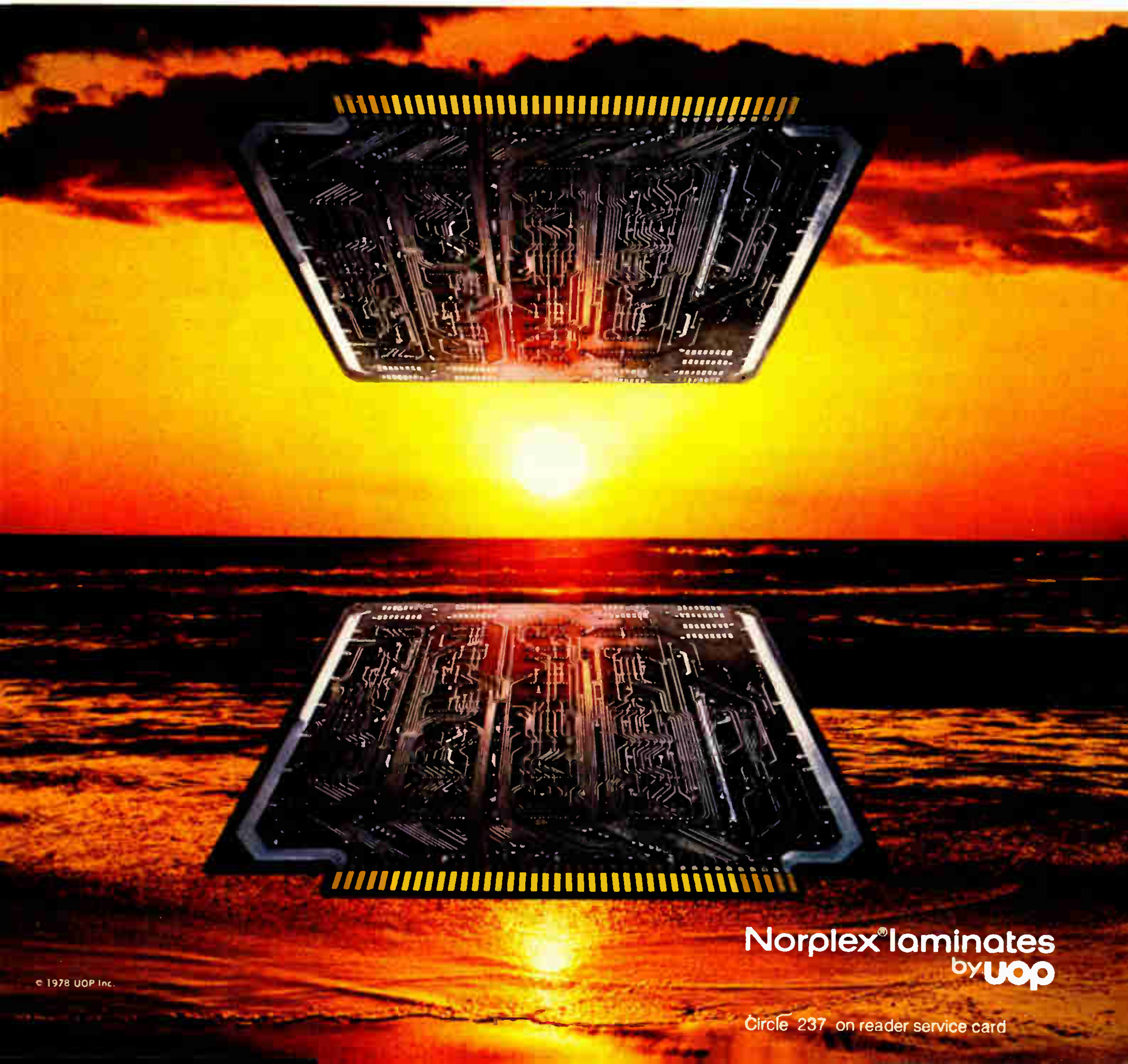
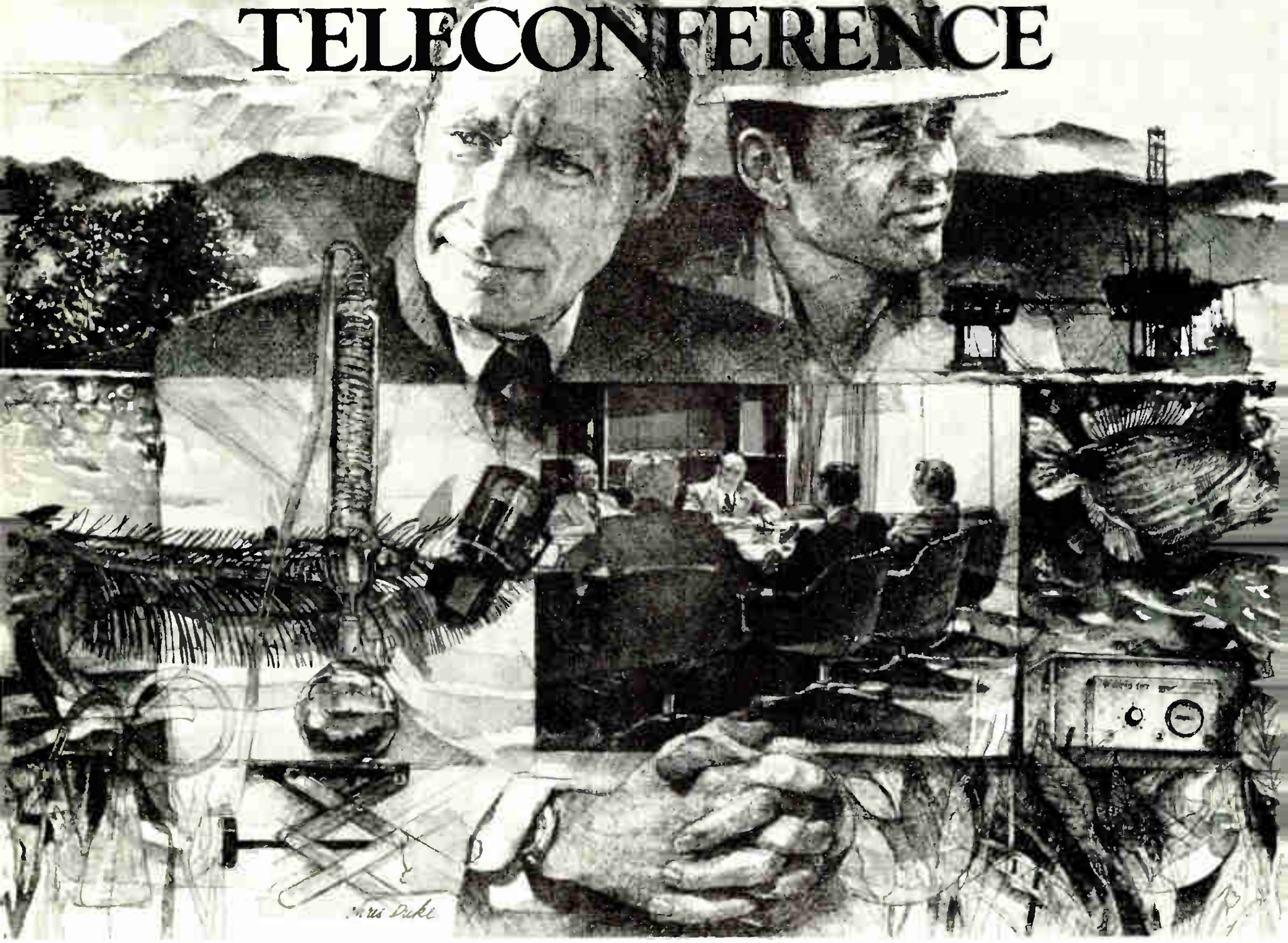


THE EXPERIENCE OF THE GEOLOGICAL SURVEY WITH THE

TELECONFERENCE



There's an unusual teleconference network in operation at the Geological Survey—the first of its kind. In its initial six months of operation, this network saved enough in travel to equal its cost.

Steve Frantz, Bell System Account Executive assigned to the Geological Survey's Conservation Division, explains: "Every Monday morning, the division managers in Reston, Virginia talk to field staffs at four regional offices.

"They conduct a meeting—a teleconference.

"These key people from Reston carry on a round table review of new policy, new regulations. In turn, the field people report in on their programs, problems, and needs.

"All this means that management has more effective control and can react faster than before.

"It means that travel is reduced—and with it, travel costs. Instead of being seated in an airplane, people remain seated at their desks.

"Another unusual thing about this network," Mr. Frantz points out, "is that you can dial a point outside the circuit. So it's easy to call a field location as remote as Alaska. And add it to the conference."

To get the same kind of help that the Geological Survey got, talk to your problem-solving Bell Account Executive. The Account Executive can bring Bell expertise to your problem and is the point of contact that opens the resources of the Bell System to your needs.

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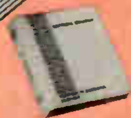

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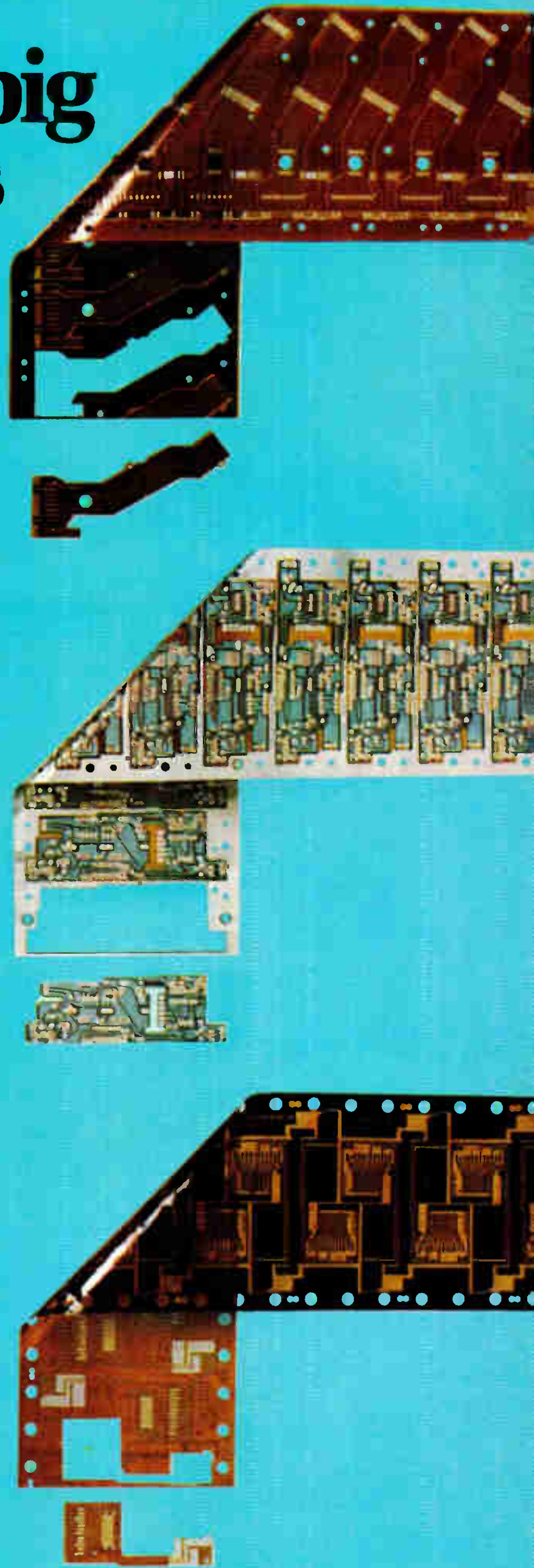
New literature

UL Safety standards. The July 1979 catalog of the Underwriters Laboratories Standards for Safety lists the first edition of "Safety Standard for Electrical Analog Instruments—Panel Board Types," and "Standard for Safety for Coin and Currency Changers and Actuators." The catalog also contains new editions such as the standards for electric coin-operated washers and dryers, fluorescent lighting fixtures, refrigeration unit coolers, and low-voltage video products. The proposed editions cover low-voltage fixtures for use in recreational vehicles and transient-voltage-surge suppressors. More than 400 previously published safety standards are also listed in the catalog. Some of the UL standards are available in French and may be obtained by writing to the Association Française de Normalization (Afnor), Tour Europe-Cedex 7, 92080 Paris La Défence, France. Underwriters Laboratories Inc., Publications Stock Department, 333 Pfingsten Rd., Northbrook, Ill. 60062. Circle reader service number 421.

Index to IRPS. Information on the reliability physics of electronic devices is provided in the "Search and Retrieval Index to IRPS Proceedings—1968 to 1978." The papers read at the International Reliability Physics Symposiums cover all aspects of electronic device technologies: testing, screening, environments, uses and applications. The papers also describe the work currently being done by the electronics industries to understand and overcome the physics of failure in electronic devices. The document provides a detailed index of 3,080 terms, an author index, a corporate index, and an alphabetical listing of the detailed index terms. The index is available for $20 a copy ($24 outside the U. S.) by ordering No. TRS-2 directly from Reliability Analysis Center, Griffiss AFB, N. Y. 13441.

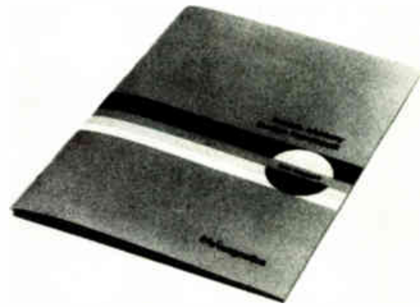
Optoelectronics. "Optoelectronics Designer's Catalog 1979" contains photographs, package dimensions, features, operating characteristics,



New literature

and performance graphs on optoelectronic components. The 384-page catalog has sections on fiber optics, light-emitting-diode displays, and other solid-state lamps, optocouplers, p-i-n photodiodes, and emitter/detectors; it also includes an alphanumeric index to part numbers and an introduction to each product's capabilities. For a copy of publication number 5953-0400 write to Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [423]

Bubble memory. Presented in the "Bubble Memory Design Handbook" are the features, descriptions, and functional characteristics of the 7110 1-megabit bubble memory and its family of support chips. The 64-page handbook contains specifications, diagrams, and tables for the 7110/7112 magnetic-bubble memory, the 7220 controller, 7230 current



pulse generator, 7242 dual formatter/sense amplifier, 7250 coil predriver, 7254 V-groove MOS drive transistors, and IMB-100 development board. Descriptions of the BPK-71 bubble memory prototype kit, design considerations for working with bubble memories, and a system interconnection diagram are also discussed. A free copy of the handbook may be obtained from Intel Corp.'s Literature Department, 3065 Bowers Ave., Santa Clara, Calif. 95051 [424]

Connectors. "Coaxial Connectors and Cable Assemblies" describes the SMA, SMB, and SMC line of miniature coaxial cable connectors designed for microwave applications in aerospace, electronic countermeas-

...for the superior reliability required by the computer industry.


Actual size of the Fotoceram® slider shown above.

In the highly competitive computer industry, one of the biggest goals is to reduce the storage and retrieval costs per bit of information to the end user. In recent years, the evolution of the Winchester disk drive technology has achieved just that—more information packed on the same size disk.

The narrower and higher density information tracks on the disk, made the precision of the read/write head an extremely critical factor. So the choice of slider material was critical as well. The solution was Fotoceram® glass-ceramic by Corning.

Fotoceram glass-ceramic had already been established as one of the most reliable slider materials available. It is known for superior wear characteristics during start and stop contact conditions. Surface smoothness of less than a micro-inch. Superior homogeneous structure. Compatibility with ferrites and sealing glasses. Precision tolerances to .001". And the bonus of low tooling costs. In addition, designers found that Fotoceram could be configured to smaller and more complex shapes required for this application.

What can Fotoceram glass-ceramic do for you? Use your imagination. With Fotoceram material, we can photo-etch holes, slots or channels in any shape or configuration you choose. Dimensions can be as small as .002", with tolerances as tight as .001". And you can pack up to 50,000 holes per square inch into sheets as thin as .010".

Fotoceram glass-ceramic is rigid, strong and dimensionally stable. It can easily handle heat to 750°C and stress to 3,000 psi. Electrical stability is excellent and moisture absorption is zero. And Fotoceram glass-ceramic is just one of three photo-etchable materials by Corning. The other two are Fotoform glass and Fotoform Opal glass-ceramic. Although all three are derived from the same photo-sensitive glass, each has its own distinct properties.

The uses for these materials are endless. They're being used for dot matrix printer wire guides, flat panel display cell sheets, fluidic devices, dielectric spacers and more. If you've got a possible application, we've got all the specs in our technical package "Materials for the Design Engineer." Just write. We're the Fotoform Products Group, part of the Materials Business, MS 123A, Corning Glass Works, Corning, New York 14830.

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CORNING

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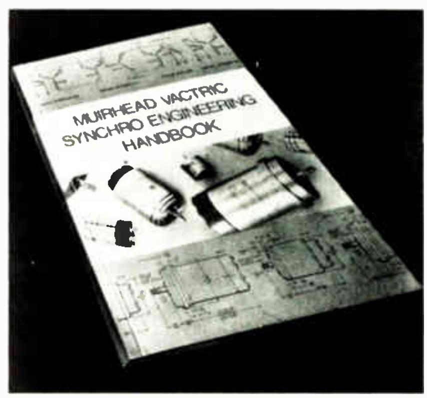
New literature

ures, communications, and instrumentation; they meet the requirements of MIL-C-39012. The catalog contains a cross-reference index to part numbers. Socapex, 6660 Variel Ave., Canoga Park, Calif. 91303 [425]

Polymers. A range of polymer formulations has been developed to meet specific requirements for a variety of parts. "Polymer Selection Guide" lists the physical properties, service temperature, ozone resistance, and fluid resistance of the various polymers. Neoprene, Hypalon, Viton, Fluorel, Kel-F, Cymax 70, Norsorex, and Fluoroelastomer are some of the polymers listed in the chart. Industrial Electronic Rubber Co., 8589 Darrow Rd., Twinsburg, Ohio 44087 [426]

Components. Testing methods, specifications, and applications on precision rotating components such as synchros, servomotors, and similar devices are discussed in "Muirhead Vactric Synchro Engineering Handbook." The 235-page handbook has chapters on rotating components, nomenclature and frame sizes, torque synchros, control synchros, servomotors and tachometer generators, basic servo systems, resolvers and other related instruments,



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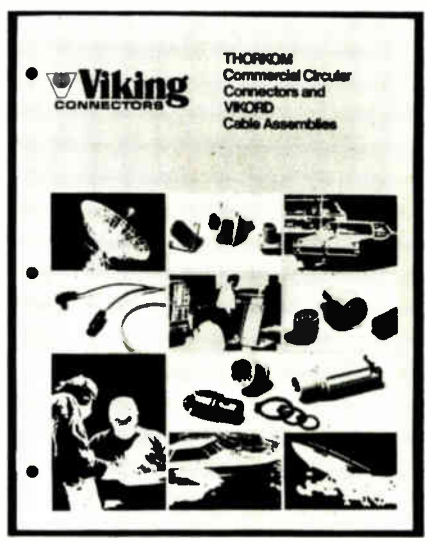
synchro and servomotor installation practices, specifications, testing, and production tests, type approval tests, servo design considerations, applications, reversals, and stepper motors. The handbook is available at $9.95 from Muirhead Vactric, 1101 Bristol Rd., Mountainside, N. J. 07092.

Capacitors. "LS Series miniature aluminum electrolytic capacitors" provide the voltage rating, part number, and standard or resin-seal dimensions of axial-leaded and radial-leaded capacitors. The eight-page bulletin contains specifications, which include operating temperature range, rated working voltage range, capacitance range and tolerance, complete capacitor dimensions, dc leakage, capacitance variation as a function of frequency and a variety of mechanical and environmental specifications. A list of cleaning solvents that are safe to use on the capacitors is also included in the bulletin. Panasonic Co., One Panasonic Way, Secaucus, N. J. 07094 [429]

Connectors. Thorkom circular quick connect/disconnect thermoplastic miniature connectors and Vikord molded cable assemblies are discussed in a 16-page catalog. Specifications, applications, and ordering information are also provided in the brochure. Viking Connectors Inc., 21001 Nordhoff St., Chatsworth, Calif. 91311 [427]



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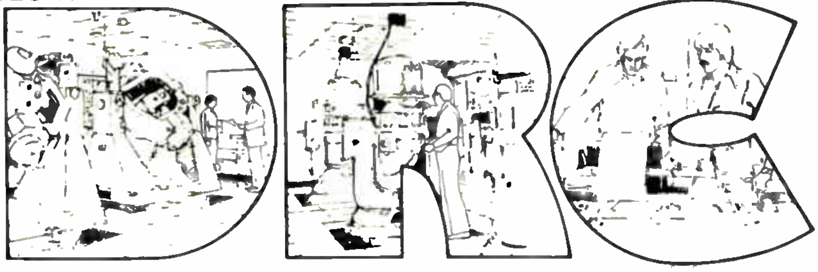

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- Design and direct test programs on inertial components.
- BSEE or ME with 5 years in the testing of inertial components.

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- Be principal instigator for study to recommend software standards and management guidelines for DOD projects. Also develop a status-monitoring management information system for DOD software, reporting to government agencies/contractors as required.
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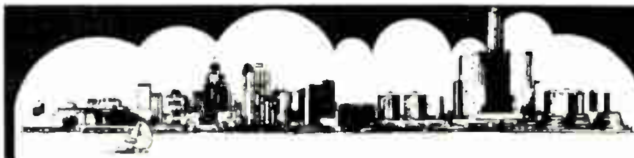

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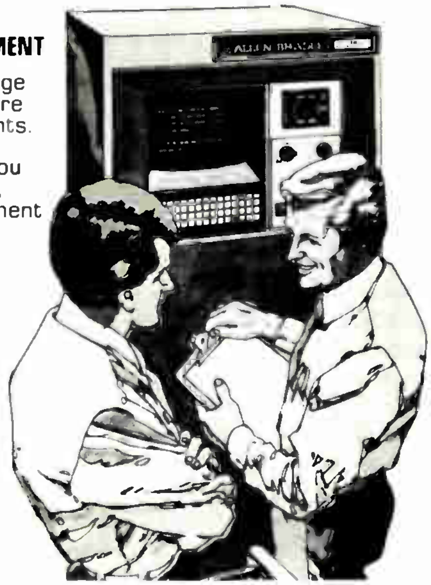

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