

SEPTEMBER 27, 1979

**CHERRY HILL CONFERENCE TO TACKLE VLSI TEST PROBLEMS/89**

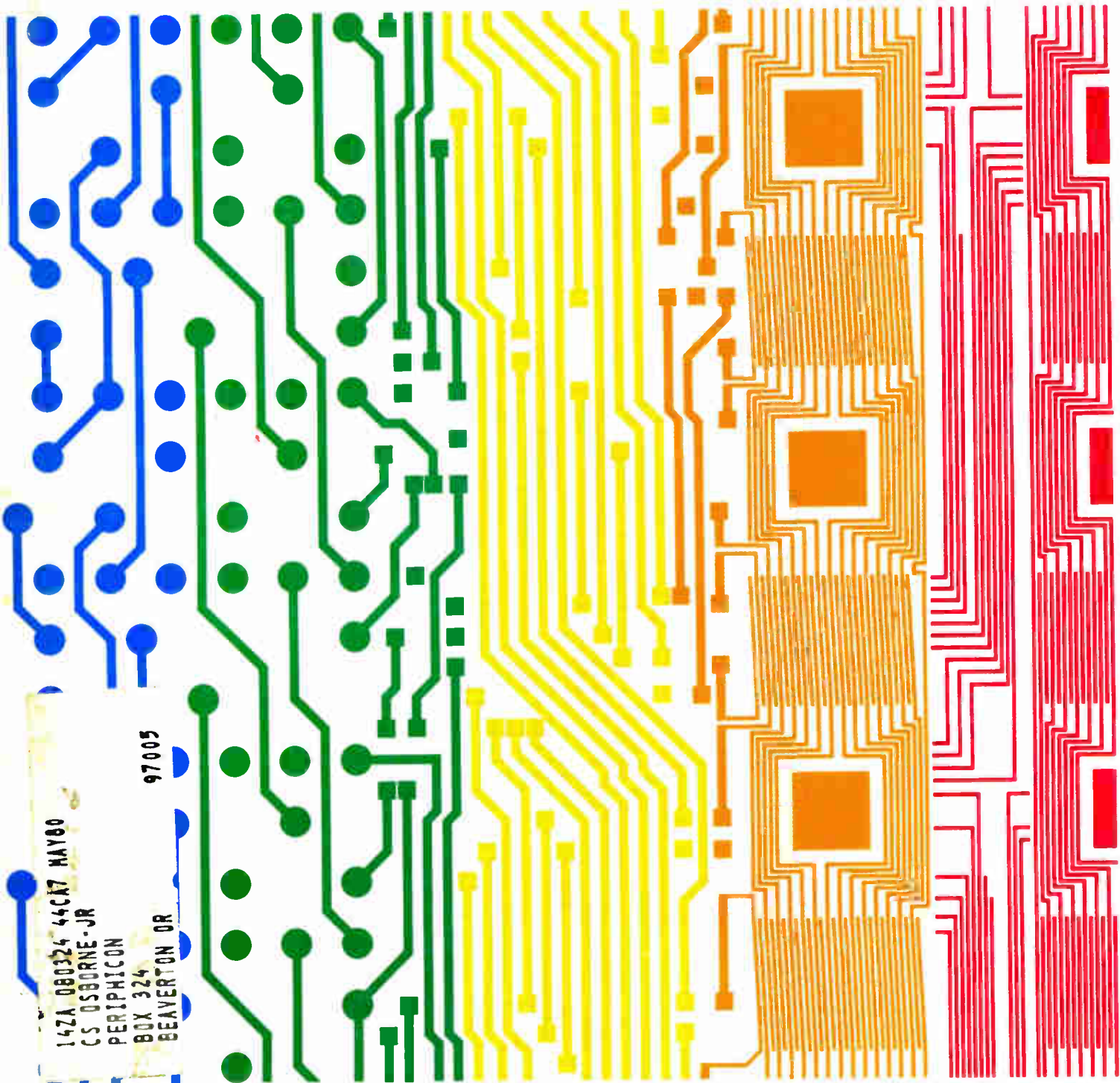
More LSI processes: static RAMs hit 8 K with polysilicon loads/ 131  
16-bit architecture eases software burden of 8-bit microprocessor/ 122



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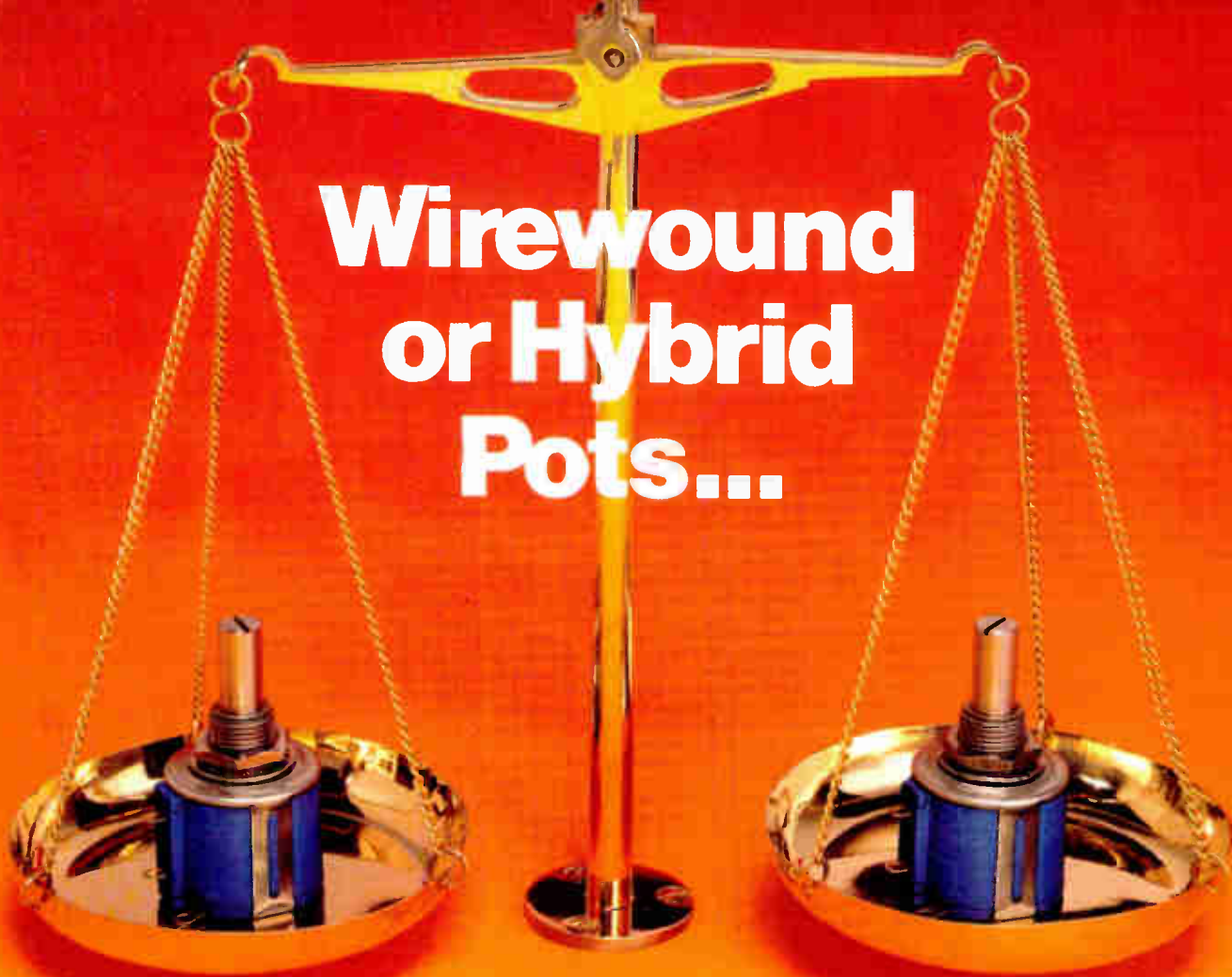
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## Highlights

### Cover: What's next in interconnects? 113

Denser integrated circuits are fast rendering the familiar printed-circuit board obsolete. The technology that dominates the next generation of boards will offer multilayer wiring on a 10-mil grid, surface-mounted components, and buried vias—all at reasonable cost.

Cover illustration is by Gabor Kiss.

### European research brightens dark corners, 93

Unusual subjects like self-testing integrated circuits and a stacked integrated-injection-logic process figure prominently in papers delivered at the Fifth European Solid State Circuits Conference held in England Sept. 18 through 21.

### 8-K static RAMs boast versatile pinout, 131

Their pinout scheme, similar to that of read-only memories, suits a pair of dense byte-wide random-access memory chips to fast mainframe cache and microprocessor applications alike.

### Stalking the elusive femtoampere, 145

Designing a supersensitive meter to complement today's low-power devices requires attention to obscure sources of current and leakage.

### ... and in the next issue

A look inside a nonvolatile static random-access memory . . . using transistors as temperature sensors . . . a 16-bit microprocessor designed for high-level languages.

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## Publisher's letter

**H**ow will components be mounted in the future? According to author Charles Lassen, manager of advanced products for ITT Exacta Circuits Ltd. in Selkirk, Scotland, the digital substrate of the 1980s will be the multistrata.

His article describing the multistrata concept appears on page 113. Although the technology needed to produce this unique substrate is already in existence, discussions of its practical applications have been largely theoretical. Now, however, Lassen believes that its time has come. He predicts that prototypes will be made next year and first applications by selected systems houses could be taking place in 1981-82. First production-volume runs could be in 1983.

"My involvement with systems and interconnection first started with Standard Telephones & Cables Ltd. in 1970," he recalls. "It intensified when I joined Exacta in 1974 and worked on product development of flexi-rigid multilayers. It became heavy when I started working with physical designers in ITT's System 12 development in the United States and has been ongoing throughout my time as Exacta's manager of advanced products."

What stimulated his interest in multistrata? "The myopic view of interconnection that exists among many printed-circuit and hybrid producers and the opportunities a package change opens up," he reports.

And Lassen is making his point. Besides writing the cover article in this issue, he is preparing a two-day seminar to bring together systems companies, components producers,

and materials firms to discuss "Interconnection in the '80's."

An accomplished offshore small-boat sailor, Lassen may need all his navigator's skill to get multistrata across to the attendees, whose ideas on printed-circuit board design do not always agree.

**N**ow it's Europe's turn to host a top-notch conference on solid-state technology. Like the recent meeting on solid-state devices in Tokyo [*Electronics*, Aug. 31, p. 85], the fifth European solid-state circuits conference, held in England, Sept. 18-21, underscored the internationalization of semiconductor technology.

As London bureau manager Kevin Smith points out in his summary of the conference (p. 93), Europeans have much to show for their effort, especially in nonstandard products and unusual processes.

Perhaps the best illustration of the internationalization, however, was the interest in uncommitted-logic-array technology. Kevin remarks that the subject was up for discussion simultaneously at this month's Wescon in San Francisco and at the Southampton, England, conference. These days it can no longer be assumed that significant advances in solid-state technology are made only in the U. S.



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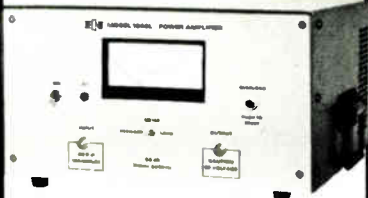
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## Readers' comments

### Simpler with priority encoders

To the Editor: With regard to "Scanner finds interrupt with highest and lowest priorities" [July 5, p. 135], I would like to mention that the same objective can be met more simply with two conventional priority encoders (74LS348s, for example)—one connected to the interrupt sources in the desired order of priority, the other in reverse order. The inverted 1's-complemented outputs of the latter will give the number of the lowest priority interrupt.

Herbert Wehlan  
Stuttgart, West Germany

### Really first

To the Editor: In "Chip makers ride CRT controller wave" in the July 19 issue [p. 85], Mitch Goozé of American Microsystems is quoted as saying that AMI's device will be "the first and only MOS mask-programmable CRT controller." In fact, the Standard Microsystems cathode-ray-tube controller, the CRT 5027, announced in the Feb. 17, 1977, New Products section of *Electronics*, was the first available standard large-scale integrated CRT controller. It is both mask-programmable and processor-programmable.

John F. Tweedy Jr.  
Standard Microsystems Corp.  
Hauppauge, N. Y.

### Hidden bug

To the Editor: In "Data-block transfer program is efficient and flexible" [June 21, p. 147], Chris Taylor presents a technique for implementing a 16-bit loop counter that he calls simple, efficient, and relatively unknown. But it is not unknown to any programmer of the 8008 microprocessor, the 8080's predecessor. That is because the 8008 did not have any double-precision operations like DAD or DCX, which are the well-known methods of controlling a loop beyond the 256-count limit of the DCR instruction.

There is a hidden bug, however, in the method given, which does not work properly when the loop count is 0000; in that case, 256 loop iterations will be performed, not 0. Perhaps not so obvious is that for

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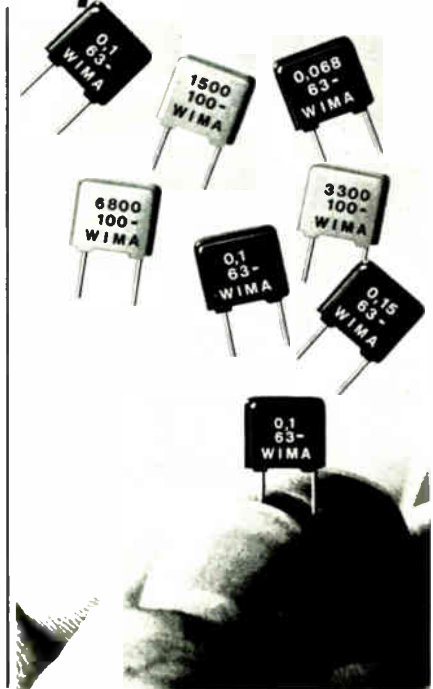
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8 Circle 8 on reader service card

## Readers' comments

any count that is a multiple of 256 the construct also breaks down and 256 extra iterations are performed. This bug is hard to detect, since it occurs only at discrete values, which might not be tested during program development.

Bruce Komusin  
Woodbury, N. Y.

## Flywheels not that big

**To the Editor:** The interesting special report on photovoltaics ["A burst of energy in photovoltaics," July 19, p.105] included several errors in the "Subsystems and Applications" section.

The flywheel being developed by the Massachusetts Institute of Technology's Lincoln Laboratory, shown on page 120, is not a 1:10 scale model, but one storing one tenth the energy of a residential-sized system. The actual linear scale is closer to 1:2.25. As a result, the "huge" flywheel for a single residence described on page 121 would have a diameter of about 3 feet, not 14. It would weigh between 1 and 2 tons (as would batteries) and, as described, would take dc power from the solar array and produce regulated 50-hertz ac.

The article should also have quoted me as stating that, on a life-cycle basis, a flywheel system is expected to cost less than today's battery system and perhaps less than an advanced battery system.

Alan R. Millner  
Lincoln Laboratory  
Lexington, Mass.

## PROM programmer option

**To the Editor:** The author of "Software-based controller simplifies PROM programmer" [July 19, p.147] shows a fine scheme for utilizing the Intel Universal PROM Programmer. But for those without access to this programmer and its particular personality modules, I would like to suggest a programmable read-only memory programming board for the S-100 bus that is manufactured by Szerlip Enterprises, Harbor City, Calif.

The Szerlip board comes standard for the 2708, 2716 (Texas Instru-



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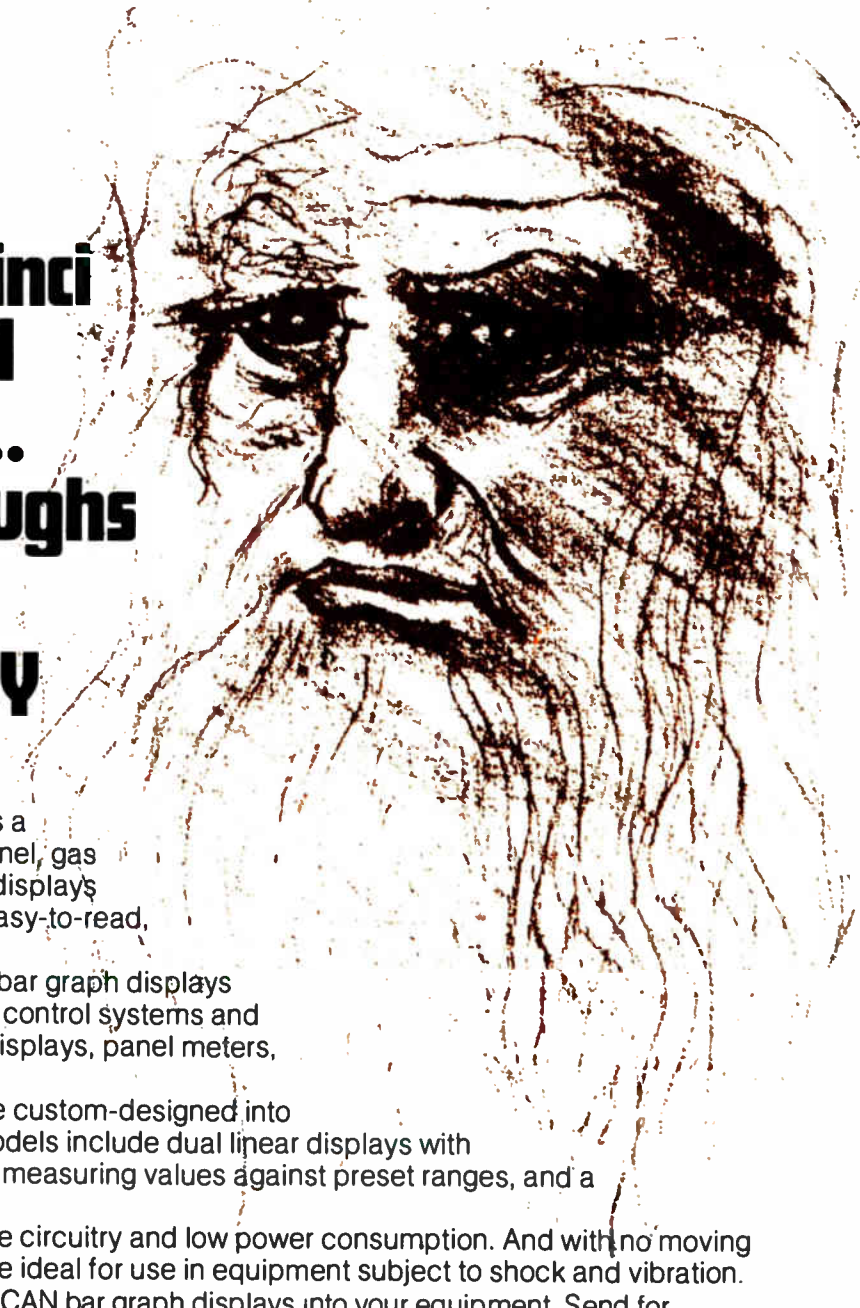
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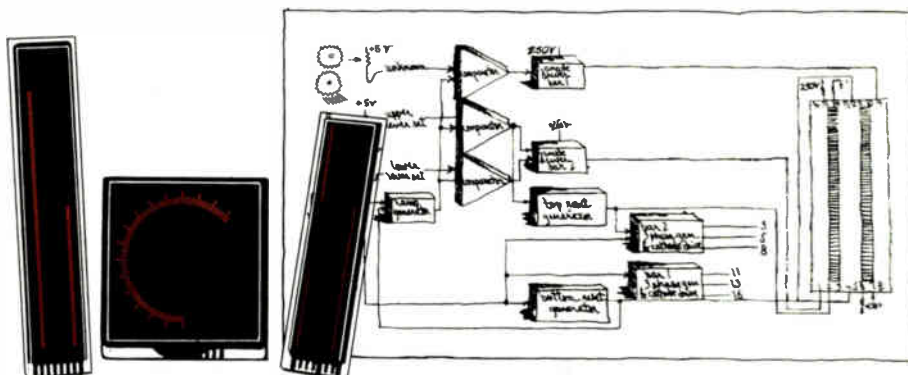
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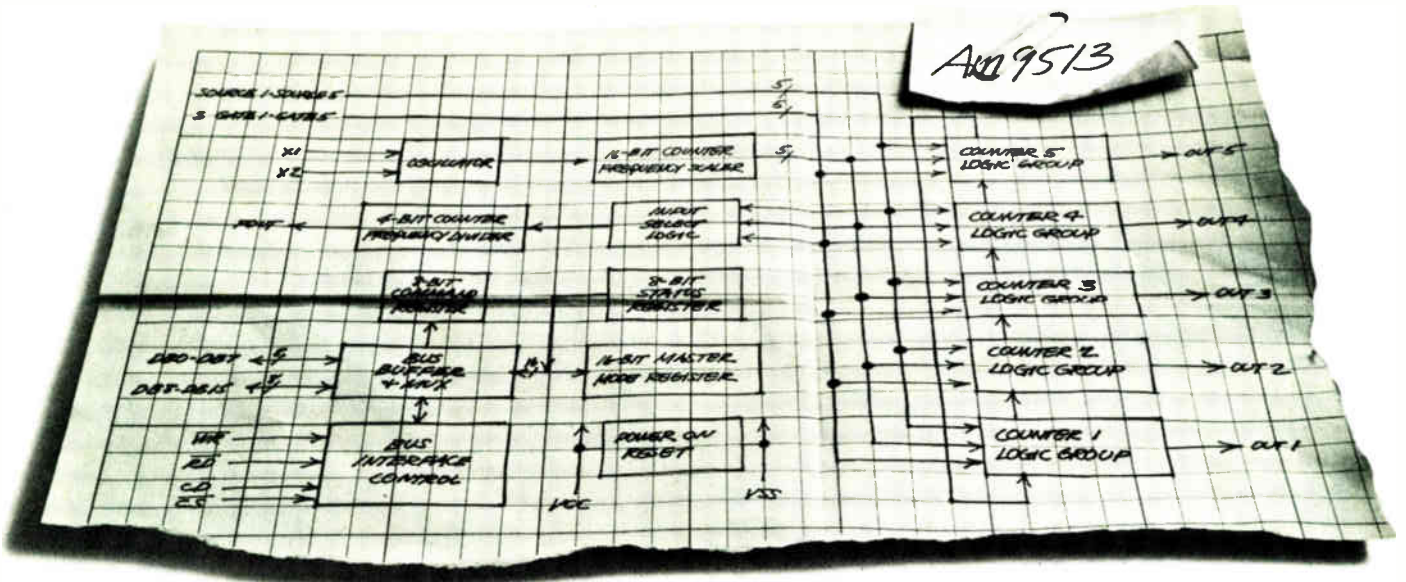
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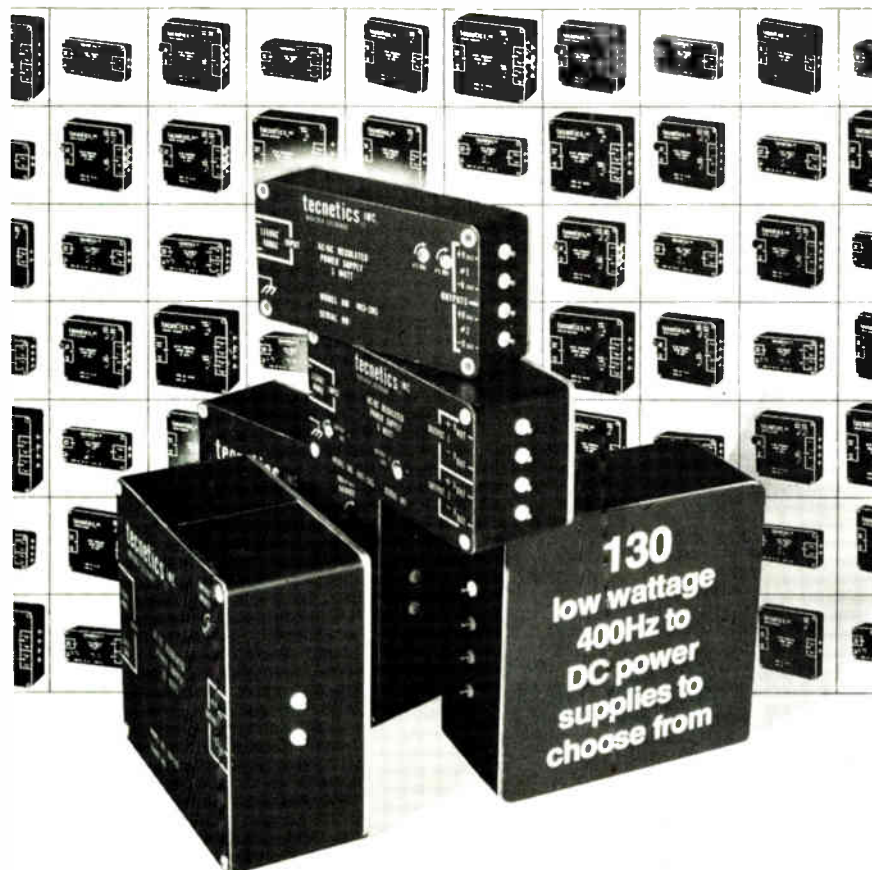
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## Readers' comments

ments' version), or 1702. Additionally, with its operating instructions, jumpers for just about any PROM or erasable PROM are easily made. All timing and voltages are software-programmable.

Donald M. Dodge  
Gardena, Calif.

### Take the red out of your eyes

**To the Editor:** Thanks for the editorial of Aug. 2 in support of the four-day work week ["A timely idea deserving consideration," p. 12]. I agree with you that this is an idea whose time has come. Actually, a change in our medieval five-day work week with two weeks off each year for good behavior (vacation) is long overdue.

I don't think you will get any support for this plan from the Institute of Electrical and Electronics Engineers, since it is politically impotent. In addition, the political naivete, or more frankly the political stupidity, of engineers is so appalling that I think most of us will timidly wait for the trade unions to fight this battle for us. As you know, our five-day work week and two-week vacation was won by their "hit the bricks" job action sacrifices.

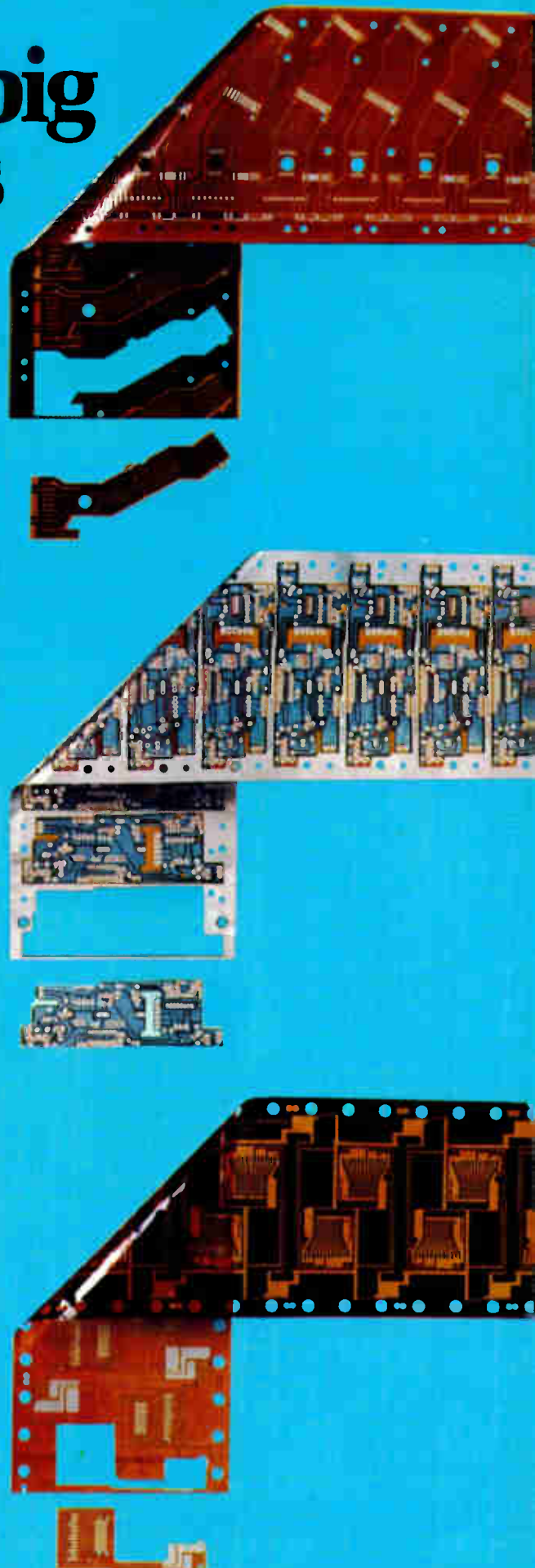
Isn't it ironic that President Carter and the Department of Defense are against our patriotic four-day energy-saving work week.

Just as coal miners succumb to black lung disease, I think electronics engineers will die economically from red-eye malaise. Red-eye malaise causes real-time blindness that renders engineers unable to see the real world of cost-of-living raises and pension adjustments to keep up with inflation, portable pensions, sabbaticals, and better tax schedules that would end job hopping as a loss of pension rights and an exercise in futility, etc. When it comes to the economic state of the art, engineers are still living in the Stone Age.

Don't you think it's time we invented the me-too flu, or do politically timid engineers really believe that the meek shall inherit the earth?

A. J. Andres  
Orange, Calif.

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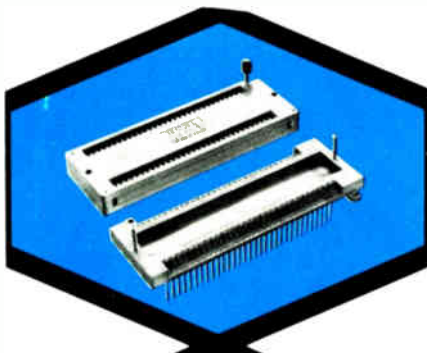
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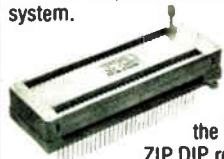
## EXPANDED ZIP DIP® II Socket/Receptacle Series

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## People

Two American entrepreneurs find their own niche  
in semiconductor business through Swiss connection

The entrepreneurial spirit of Silicon Valley is not dead yet—it just has to go to Europe to breathe. The founders of Xicor Inc. came to that conclusion after searching the valley for a manufacturer to build the semiconductor invention on which they base their company.

S. Allan Kline and Raphael Klein designed a nonvolatile random-access memory. "Our first thought was to have the chips we designed built by custom semiconductor houses here in the U. S.," explains Allan Kline, chairman of the Sunnyvale, Calif., company and a former director of Intersil Inc. "But we were discouraged. All the manufacturers are production-limited and wouldn't deliver for six months."

**Looked to friends.** So Allan Kline, 57, contacted some friends from the young days of semiconductors in California who now are at Ebauches Electroniques SA in Marin-Epagnier, Switzerland. Kurt Hubner is now general manager of the semiconductor manufacturing division of Ebauches, and Hans G. Dill is in charge of integrated-circuit manufacturing. Between the two, they convinced Allan Kline that

Ebauches, whose parent company is a privately owned watchmaker and one of the largest suppliers of watches and watch chips in the world, would be able to handle the requirements.

So Raphael Klein, Xicor's president, flew over to check out Ebauches' manufacturing facilities. "We needed to have an intimacy with the company that built the part," explains the 36-year-old Israeli-born physicist. He knew that making the new RAM, which relies on a relatively new operating phenomenon and uses three-level polysilicon processing [*Electronics*, Sept. 13, p. 39] would require a special relationship with their counterparts at Ebauches.

"I gave the facility the white-glove check, and it was cleaner than anything I've seen in Silicon Valley," says Raphael Klein. He is qualified to draw the comparison, having spent much time in the valley at Monolithic Memories Inc., at National Semiconductor Corp., at Fairchild Camera and Instrument Corp., and at Intel Corp. Most recently, he had been consulting and had been instrumental in setting up many

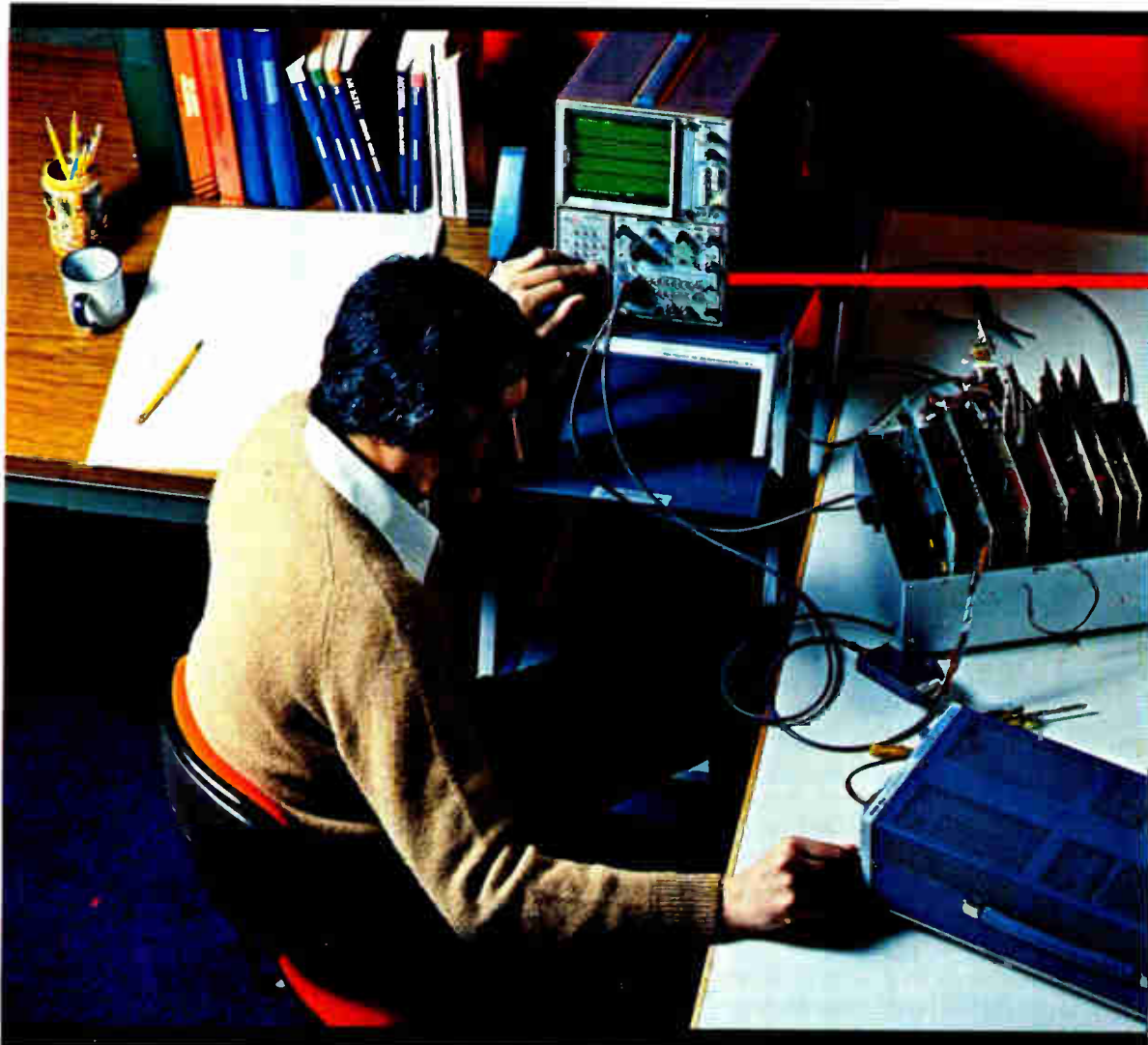


**Teamwork.** Xicor founders S. Allan Kline and Raphael Klein, second and third from left, designed the RAM that Kurt Hubner, left, and Hans G. Dill of Ebauches Electroniques make.



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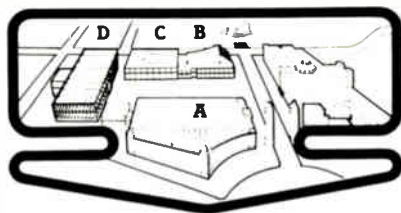
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## People

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Raphael Klein set to work helping Ebauches gear up for the Xicor memory—the Swiss company's first industry-standard component. In fact Ebauches had just changed from metal-gate complementary-MOS processing to polysilicon gate when Klein arrived.

**Due on shelf.** All that was just over a year ago, and now Xicor says production at the Swiss facility has moved into high volume. As soon as negotiations with two major distributing firms are settled, Xicor can begin to stock its distributors' shelves with the parts.

The two Xicor founders are not afraid of pressure from the semiconductor giants, they say, because the 1-K nonvolatile RAM complements the market. "It has its own niche and doesn't make anything obsolete," says Raphael Klein.

The two physicists—during World War II, Allan Kline worked on the Manhattan Project, which developed the atomic bomb—are pleased with the friendly agreement with Ebauches. "We're partners, and from the start we've had no problems. Each company can go its own way and Ebauches is free to market the part as it sees fit," says Allan Kline, whose entrepreneurial endeavors have carried him into other industries. For example, he is currently involved in the development of new technology in the food industry as well: a healthful "junk-food" snack made from yogurt and wheat based on a new process that puffs the proteinaceous part of the grain and not the starch.

Klein and Kline are excited by the challenge posed by their new high-technology company—a spirit they feel has long left the large, centralized semiconductor companies. Xicor, which is now just a handful of people, will eventually build a plant in the U. S. Says Allan Kline, "We believe that with top-quality technical and marketing people, you can grow a company in a very decentralized fashion and maintain the original spirit." □

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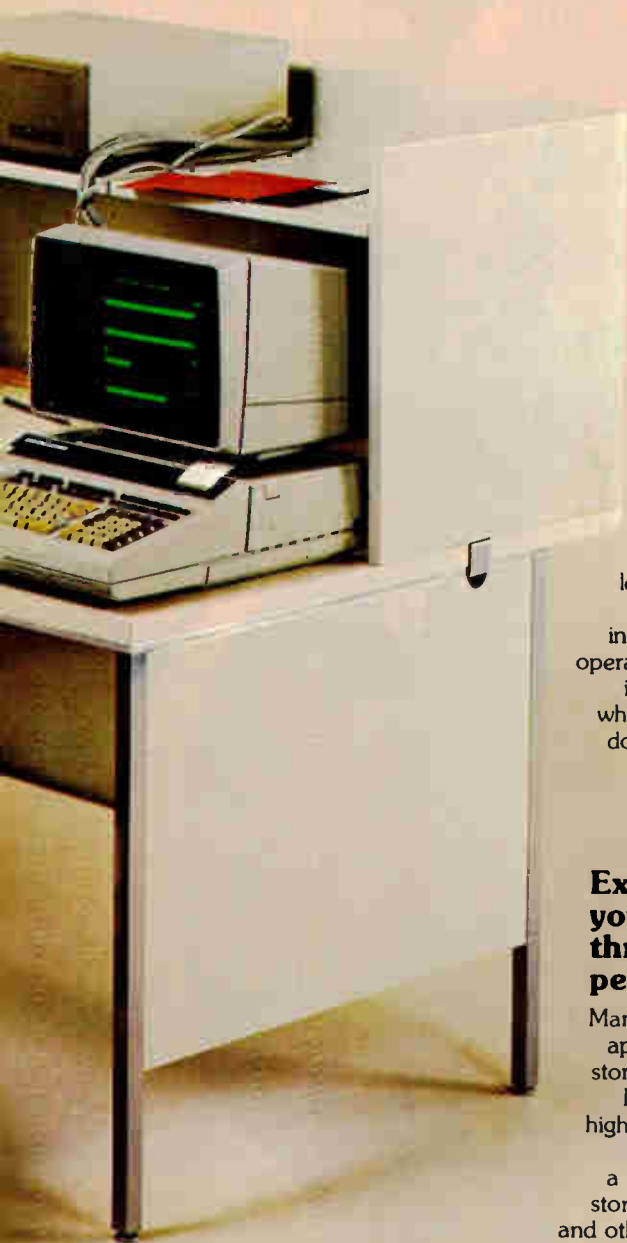
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# IMAGINE



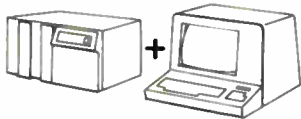
# IMAGINE

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## The base package, the Model 10.

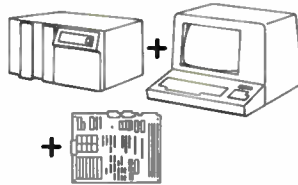
Your most economical entry to Z8000 product development. Everything you need to start your Z8000



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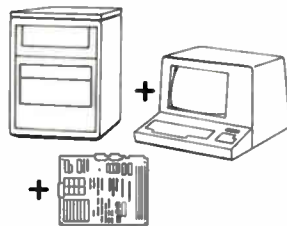
## Try it out with the Model 15.

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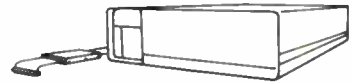
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The fireworks have just begun!



## Which way is up?

Just what is progress? What at one time were obvious answers have in many cases become questions. Or, in the words of William H. Davidow, vice president and general manager of Intel Corp., "As the world has become more complex and sophisticated, it has become increasingly difficult to determine what constitutes progress."

Focusing his views on electronic technology in general and computers in particular, Davidow says that everyone involved with computers would believe that the transistor was good, integrated circuits were better, and semiconductor memories represented a further advance, "and that VLSI [very large-scale integration] is essential to the continued progress we hope to make within the next few years."

Now take a look at microcomputers. As Davidow observes, "the first generation of microcomputers was good, the next generation was better, and future generations of these products will be even more significant." They will do more, be more complex, and lead more quickly to the development of new products. And when this comes to pass, the world will be a better place for all of us—engineers, business executives, and the five-year-old across the street who this month marched bravely off to his first day of kindergarten.

But hold, cries Davidow; that is not necessarily so. "I feel compelled to say that it is no longer evident to me that to maintain the existing rate of progress is optimum. And it is no longer evident that the majority of microprocessor users are going to be capable of exploiting the next explosion in microprocessor technology. . . . However, it may be true that rapid technological progress is going to slow the use of microprocessors to an increasingly narrow spectrum of applications." Davidow's point is that as

microcomputers become able to handle throughput faster, they will become suitable only for that higher order of jobs that requires such speed and power. Thus, their horizon will constrict to enclose fewer opportunities, reducing their commercial appeal.

Gordon E. Moore, president of Intel and Davidow's boss, has preached much the same gospel—that there is a point at which growth outstrips utility. So taking Davidow's corollary to Moore's law and applying it to electronic technologies of all sorts, one must wonder if all the complexity and progress possible are, indeed, usable or even useful. After all, what good is the sweat and toil in the laboratory if what emerges is admired and valuable only to a handful of fellow scientists or ultrasophisticated users?

Clearly, what has made electronic technology so pervasive in the past decade or so is its promise of the most good for the most people: "Great idea!" says the populace: "Why didn't someone think of it sooner?" But equally clearly, what brought the electronic technologies to this high level in the first place was the impetus that has been lent them by military considerations—the Government's concern over both conventional national defense and the space program. Indeed, the next big leap in semiconductors seems likely to come from the Department of Defense's Very High-Speed Integrated Circuit (VHSIC) program, and its results are intended to please the generals, not the populace.

Davidow's and Moore's remarks make sense in terms of a world at peace with itself. But with the Salt 2 Treaty having such difficulty passing the Senate, the arms race is alive and kicking, and complaints that technology is becoming needlessly complex are likely to go unheeded. At least for the foreseeable future, progress will continue to push performance, whatever its drawbacks.



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## Meetings

**International Electrical and Electronics Conference and Exposition**, IEEE, Exhibition Palace, Toronto, Oct. 2-4.

**ATFA/79—Advanced Techniques in Failure Analysis Symposium and Exposition**, International Society for Testing and Failure Analysis (Redondo Beach, Calif.), Airport Marriott Hotel, Los Angeles, Oct. 8-11.

**Annual Meeting of the Optical Society of America** (Washington, D. C.), Genesee Plaza Holiday Inn and Americana of Rochester, Rochester, N. Y., Oct. 8-12.

**International Symposium on Electromagnetic Compatibility**, IEEE, Town & Country Hotel, San Diego, Calif., Oct. 9-11.

**Symposium on Industrial Technology, Innovation and Industrial Development**, Massachusetts Institute of Technology, Cambridge, Mass., Oct. 16-17.

**Fifth Annual Fall Symposium**, International Word Processing Association (2360 Maryland Rd., Willow Grove, Pa. 19090), Shamrock Hilton, Houston, Oct. 16-18.

**12th Annual Connector Symposium**, Electronic Connector Study Group (Box 1428, Camden, N. J. 08101), Cherry Hill Hyatt House, Cherry Hill, N. J., Oct. 17-18.

**Computers in Aerospace Conference II**, American Institute of Aeronautics and Astronautics *et al.*, Hyatt House, Los Angeles, Oct. 22-24.

**Ninth Annual Conference**, Association of Computer Programmers and Analysts, Washington, D. C., Oct. 22-24.

**Defense Electronics in the 1980s Symposium**, Electronic Industries Association, Jack Tar Hotel, San Francisco, Oct. 23-25.

**24th IEEE Machine Tools Conference**, IEEE, Troy Hilton Inn, Troy, Mich., Oct. 23-24.

**Semiconductor Test Conference**, IEEE, Cherry Hill Hyatt House, Cherry Hill, N. J., Oct. 23-25.

**Newport Conference on Fiber-Optic Markets**, KMI Inc. (20 Fairwell St., Newport, R. I. 02840), Sheraton Islander, Newport, Oct. 25-26.

**Optical Signal Processing for C<sup>3</sup>I (Command, Control, Communications, and Intelligence)**, Society of Photo-Optical Instrumentation Engineers (Bellingham, Wash.), Marriott Hotel, Boston, Oct. 29-30.

**NCF-NEC/79—National Communications Forum/National Electronics Conference**, National Engineering Consortium Inc. (Oak Brook, Ill. 60521), Hyatt Regency O'Hare, Chicago, Oct. 29-31.

**Autofact II—the Automated, Integrated Factory of Tomorrow Conference and Exposition**, Society of Manufacturing Engineers (Detroit, Mich.), Cobo Hall, Detroit, Oct. 30-Nov. 1.

**Interface West/79—Third Annual Data Communications, DDP and Office Automatic Systems Conference**, Interface West (Framingham, Mass. 01701) *et al.*, Anaheim Convention Center, Anaheim, Calif., Oct. 30-Nov. 1.

**64th Convention**, Audio Engineering Society Inc. (60 East 42nd St., New York, N. Y. 10017), Waldorf Astoria, New York, Nov. 2-5.

### Short courses

**Introduction of Teleprocessing Software**, three-day session in various cities; the first Oct. 3-5 in New York. Write to Datapro Research Corp., 1805 Underwood Blvd., Delran, N. J. 08075, or call (800) 257-9406 or in N. J. (609) 764-0100.

**Software Reliability Technology**, an Oct. 11-12 seminar in Rosslyn, Va. Write Software Research Associates, P. O. Box 2432, San Francisco, Calif. 94126, or call (415) 957-1441.

# Introducing the Micalign<sup>®</sup> 200 Series. Higher throughput than step-and-repeat at a much lower price.

Perkin-Elmer designed the new Micalign Model 200 to be the most cost-effective projection mask aligner available. In performance, it achieves 2-micron geometries or better in production, distortion/magnification tolerance of 0.25 micron, and 4 percent uniformity of illumination. Options available include automatic wafer loading and automatic alignment. Soon to be available: deep UV optical coatings for still smaller geometries.

Compared to the leading step-and-repeat aligner, the Micalign Model 200 delivers outstanding performance for not much more than half the cost. It takes about a quarter of the floor space. It provides consistently higher throughput regardless of die size.

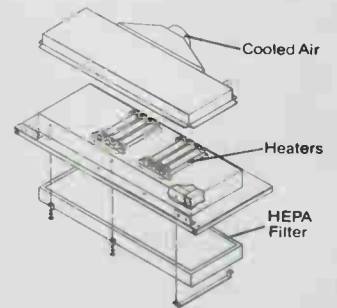
The Model 200's remarkable performance is the result of a number of major innovations.

## Improved optical design and fabrication

We improved the optical design to provide increased resolution and depth of focus. Optical manufacturing tolerances are five times tighter to ensure precise overlay from aligner to aligner.

## Near-zero vibration

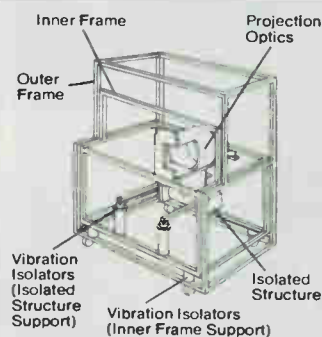
We minimized vibration. We constructed the Model 200 with two frames—one inside the other. The inner frame, which carries the projection optics and carriage drive, is completely isolated from the outer frame.



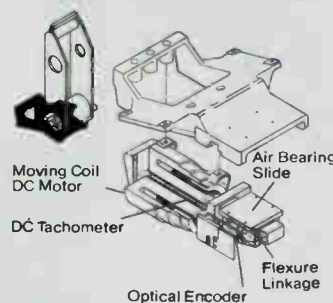
We included a separate thermal control for the mask, to compensate for mask run-out.

## No mask contamination

We designed a sealed mask carrier for the Model 200. You put the mask in the special carrier right in the mask department. Seal it. When you load the sealed carrier in the Model 200, the cover plates are automatically removed. After use, the cover plates are automatically replaced.



We incorporated a superb linear motor carriage drive with air bearing slide. This drive does more than eliminate vibration. With the air bearing feature there's no contact and no wear. And no limit to carriage drive durability.



## Built-in environmental control

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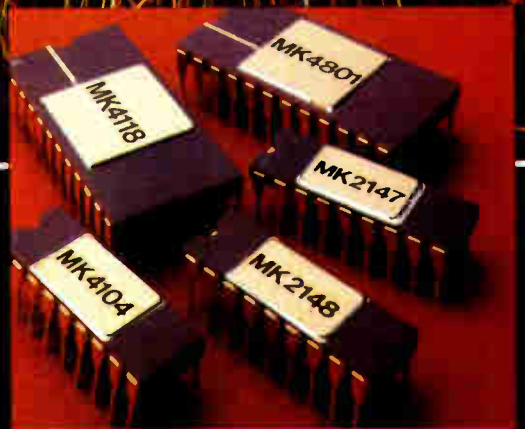
## Proven production capabilities

Perkin-Elmer, the leader in projection mask alignment systems, offers six years of proven production capability, with an excellent training and service record.

## Get all the facts

These are just a few of the features that make the Micalign Model 200 Series a completely new concept in projection mask aligners. Get more details on how these and other improvements in design can translate into improvements in your production. For literature, write Perkin-Elmer Corporation, Microlithography Division, 50 Danbury Road, Wilton, CT 06897. Or phone (203) 762-6057.

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Our MK4118 is designed with the user in mind, providing optimum density and performance in a pin-out that's compatible with ROMs and EPROMs. It's the first of many RAMs in Mostek's family of Byte-Wyde™ memories, developed for easy interface to all microprocessors.



Product	Org.	Speed
MK4104-3	4K X 1	200ns
MK4118-2	1K X 8	150ns
MK4801	1K X 8	<100ns
*MK2147	4K X 1	<100ns
*MK2148	1K X 4	<100ns

Our next introduction will be a 2K x 8-bit static RAM for even more flexibility of system design.

In addition to 16K RAMs, we will introduce a pair of 4K RAMs. The MK2147 and MK2148 will provide sub-100ns performance. And, like the high-speed 1K X 8-bit MK4801, these new products will use our advanced Scaled Poly 5™ process. So you can look forward to higher system density, lower power and reduced system cost.

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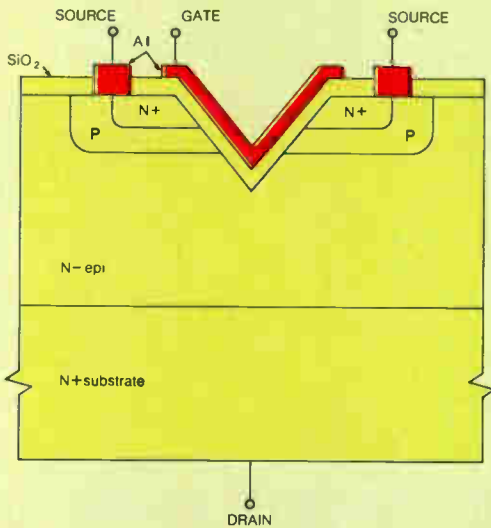
For years, you've been reading about the advantages of VMOS power FETs: Reducing the need for high current drivers. Improved thermal stability. High breakdown/high current combined with ultra high speed switching. And of course, lower component count. You said you'd use them in quantity. There was only one problem: They weren't available in quantity. Now, they are. Because Intersil is making VMOS work.



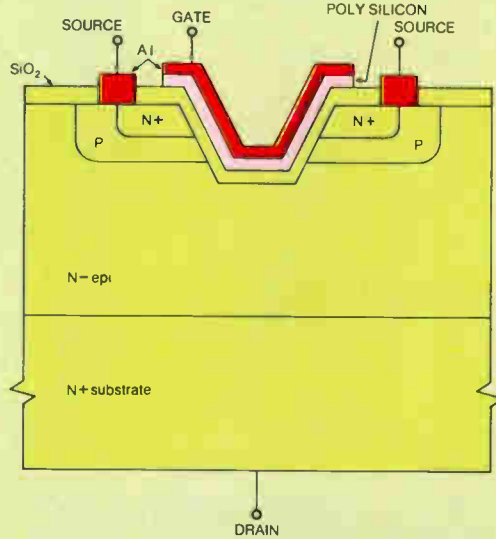
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# Electronics newsletter

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## **Sears to stock its stores with Atari computers**

Can home computers be mass-merchandised at nonspecialty stores? The big test, and possibly the answer, comes as Sears, Roebuck and Co. places Atari home computers, disk drives, and printers in up to 500 stores around the country and in its fall catalogue, available this week. Point-of-purchase displays of the unit will appear at larger Sears stores within a month, sources say, **and the merchandiser expects to sell at least 100,000 personal computers a year** [*Electronics*, Jan. 4, p. 34]. The models for sale will be the Atari 400, which includes a touch-pad keyboard, at a retail price of \$550 and the 800, which includes a standard keyboard but will be available at fewer stores at a list price of \$1,000. J. C. Penney also will stock the smaller Atari unit.

## **Fairchild to unveil series 20 system at Test Conference**

Fairchild Camera and Instrument Corp.'s Test Systems Group is preparing to defend its position as the industry leader at next month's Fifth Annual Test Conference in Cherry Hill, N. J. (see p. 89). The San Jose, Calif.-based group will come to the arena armed with a new general-purpose system that can test the latest microprocessors, peripheral chips, and other large-scale integrated circuits **at a basic 20-MHz test rate or at 40 MHz and above with a limited format**. Dubbed the series 20, the system relies on 100,000-gate emitter-coupled-logic devices from Fairchild's semiconductor operation to give it the high-speed capability. Its price is \$600,000.

## **Boards coming from NEC Micro; floppy controller first**

NEC Microcomputer Inc., already the largest importer of Japanese memory, peripheral, and microprocessor integrated circuits, is going into the board business. The Wellesley, Mass., firm's first of about a half dozen planned major introductions will be a smart floppy-disk controller. The model BP-2190 will be based on the firm's 765 peripheral chip and would operate with a mix of standard and double-density, single- and double-sided floppies, as well as with as many as four 8-in. and three 5<sup>3</sup>/<sub>4</sub>-in. drives simultaneously. The board should be priced well below \$2,195 in small lots and be available in November.

## **SLIC to join Motorola 3-chip phone set**

In the potentially lucrative market created by the telephone industry's coming conversion to digital circuitry, the subscriber loop interface circuit (SLIC) is critical to leadership, declares James R. Fiebiger, Motorola Inc. vice president and general manager of the company's MOS operation in Austin, Texas. And with Motorola's complementary-MOS codec and accompanying filter scheduled to move from the sample into the early production phase in Austin during October, Fiebiger likes what he sees looking westward to Phoenix, where Motorola's bipolar crew is **readying the MC3419 SLIC for delivery in sample quantities during the fourth quarter**.

## **Intersil C-MOS chip converts voltages at 99.9% accuracy**

Watch for Intersil Inc. to bring out a highly accurate complementary-MOS voltage converter for data-acquisition systems. Such systems, because they employ digital and analog signal processing, require both positive and negative power supplies. Called the ICL7660, the new device will, for example, convert a +5-v supply to a -5-v supply with 99.9% accuracy and can supply power to a load of 2 to 20 mA typical currents, at conversion efficiencies of about 97%, says the Cupertino, Calif., company.

### **Gould to move some scope work back to U. S.**

Concerned about its ability to satisfy an increasing demand for its products in the U. S., Gould Inc.'s Cleveland-based Instruments division is planning to establish an assembly operation in the U. S. for oscilloscopes at present manufactured at its British plant in Hainault. **Initial plans call for Gould to assemble low-frequency scopes** and then move into manufacturing higher-frequency and digital scopes sometime next year. The move parallels that of Philips Test and Measuring Instruments Inc., which will soon begin manufacturing low-frequency (25-to-35-MHz) scopes in a 15,000-ft<sup>2</sup> facility in Mahwah, N. J.

### **TI enters fast 2147 market with 2.5- $\mu$ m part . . .**

Texas Instruments Inc., eyeing Intel Corp.'s success with fast 4-K-by-1-bit 2147 static random-access memories, is going to second-source the popular devices. TI's single-5-v, fully static TMS 2147 features automatic chip-select/power-down and comes in three access times of 55, 70, or 90 ns. However, TI says the 2147 augurs other TI parts, such as a faster 2147 or a 1-K-by-4-bit fast 2148 static RAM, also now made by Intel. **To get the performance, TI uses a 2.5- $\mu$ m scaled-down MOS technology** employing a single-polysilicon depletion-load technique, though it had hinted it might use the 2147 as an entry device for the vertical-groove MOS (V-MOS) approach it has under license from American Microsystems Inc. But TI thinks that V-MOS is better because it is a good logic technology.

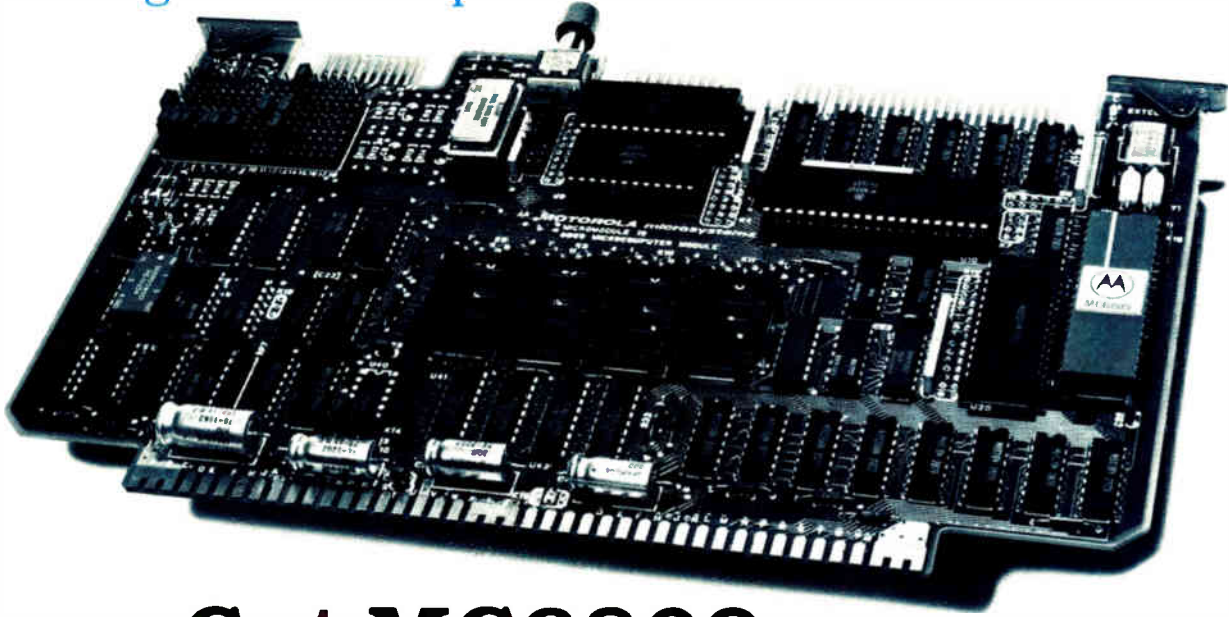
### **. . . while Hitachi offers C-MOS static versions of 2147, 2148**

Meanwhile, Japan's Hitachi Ltd. is building up a series of industry standard static random-access memories made with complementary-MOS technology for much lower power than the Intel 2147 and 2148 device. One part is an HM6147 that is compatible with the Intel 2147 4-K-by-1-bit, 900-mW part but dissipates a minimum of only 200 mW. Following that into production in early 1980 will be the HM6148 version of Intel's 1-K-by-4-bit 2148 with 55- and 70-ns access times and 150 mW typical operating power. Hitachi also plans to supply samples in March 1980 an **HM4847 version in n-channel MOS of Intel's high-speed 35- and 45-ns 2147**. In dynamic RAMs Hitachi plans to supply samples of an HM4816 16-K-by-1 device later this year that operates on a single 5-v supply with a 100-ns access time. A 64-K stablemate is due in early 1980 with 120- to 200-ns access times. The two 5-v parts have typical operating power figures of 225 and 175 mW, respectively.

### **Addenda**

In its efforts to fend off an unfriendly takeover attempt by Gould Inc., Mostek Corp. of Carrollton, Texas, **has hired Martin Lipton, a New York attorney with a good track record as an antitakeover specialist**. Most recently he successfully represented Fairchild Camera and Instrument Corp. against Gould, and McGraw-Hill Inc. against American Express Co. . . . Hitachi Ltd., which second-sources Motorola's 8-bit 6800 microprocessor, **will second-source the 16-bit 68000**. . . . Still uncertain about its role in the plug-compatible computer industry, National Semiconductor Corp., Santa Clara, Calif., has not yet decided whether to sever, continue, or extend its relationship with financially troubled Intel Corp.'s Data Products division. **However, National's proposed S/400 minicomputer program is being placed on hold** because National says it is sharpening the focus of its Computer Products group on the development, manufacture, and direct sale of medium- to large-scale computer products.

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## Get MC6809 power with Micromodule versatility.

Motorola's M68MM19 is a new MC6809 microprocessor-based monoboard microcomputer that epitomizes the power and versatility of its entire Micromodule™ family.

With its 16-bit instructions, 16-bit internal data paths, and 10 addressing modes, the MC6809 is the most powerful 8-bit MPU of its generation. All the speed, power and software design efficiency of the MC6809 is carried upward to the M68MM19 monoboard microcomputer.

The M68MM19 packs greater I/O flexibility and considerably more RAM, ROM and EPROM capacity than any previous 8-bit one-board microcomputer. The 2K bytes of static RAM are accessible from external DMA, and sockets are provided for up to 16K bytes of EPROM, ROM or pin-compatible RAM.

Twenty lines of parallel I/O are handled efficiently by the board's MC6821 Peripheral Interface Adapter, and there's an option for either of two types of serial I/O. The standard MC6850 Asynchronous Communications Interface Adapter is easily replaced by the MC6852 Synchronous Serial Data Adapter for synchronous applications.

Yet another M68MM19 flexibility option is strap selection between the RS-232C, RS-422 and RS-423 interface standards for the serial port. The board also includes a triple 16-bit

programmable counter/timer, dynamic RAM refresh control logic, DMA interface logic and full bus buffering for address, control and data lines.

### **Micromodules, a complete family.**

Motorola's complete Micromodule family now offers a choice among seven different monoboard microcomputers and a broad spectrum of board-level modular subassemblies. These include 21 digital and analog I/O modules, MC6800- and MC6809-based processor modules, the new M68MM14 high-speed arithmetic module and nine different ROM and RAM modules.

The family of nearly 50 boards and accessories provides a powerful, cost-effective design approach to a wide range of applications in process control, testing, intelligent instrumentation and general microcomputer system prototyping.

A comprehensive brochure covering the entire Micromodule family, firmware/software, auxiliary support modules, power supplies and packaging hardware is available on request. Write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036. For fast, direct response, call our Microsystems Product Marketing, 602-962-2223.

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## Bubble memory family extends to megabit size

by Raymond P. Capece, Solid State Editor

2- $\mu\text{m}$  bubble diameters and new planar technology appear in three-part line that ranges from 256 K up

Stepping up the pace in bubble memories, Texas Instruments Inc. launched at Wescon a family of 256-K, 512-K, and 1-megabit chips that share packaging and semiconductor support circuits. Based on 2-micrometer bubbles using a new all-planar process, the family follows Intel Corp. to the million-bit goal but does so with some distinct differences.

The Dallas-based firm is using a second-generation technology to scale its bubble diameters down to 2  $\mu\text{m}$ ; its own earlier 256-K bubble chip relies on 3- $\mu\text{m}$  bubbles, like that of Rockwell International Corp. and like Intel's 1-megabit part [*Electronics*, April 26, p. 105]. As a result, the million-bit TI chip is 340 by 440 mils—just under a square centimeter. Intel's die is four times that size.

**Storage.** Also, TI is using a different organization. Still a block-replicate architecture duplicating data in minor loops into a major loop without ever removing it, the million-bit part comprises two identical data-storage sections with 256 loops of 2,048 bits in each. (Actually each section has 300 loops; 18 are allotted for error-correction information and as many as 26 are allowed to be defective.) The resulting format of 512 loops of 2-K bits each has half the access time of Intel's 256 4-kilobit loops: 11.2 milliseconds at a 100-kilohertz field frequency.

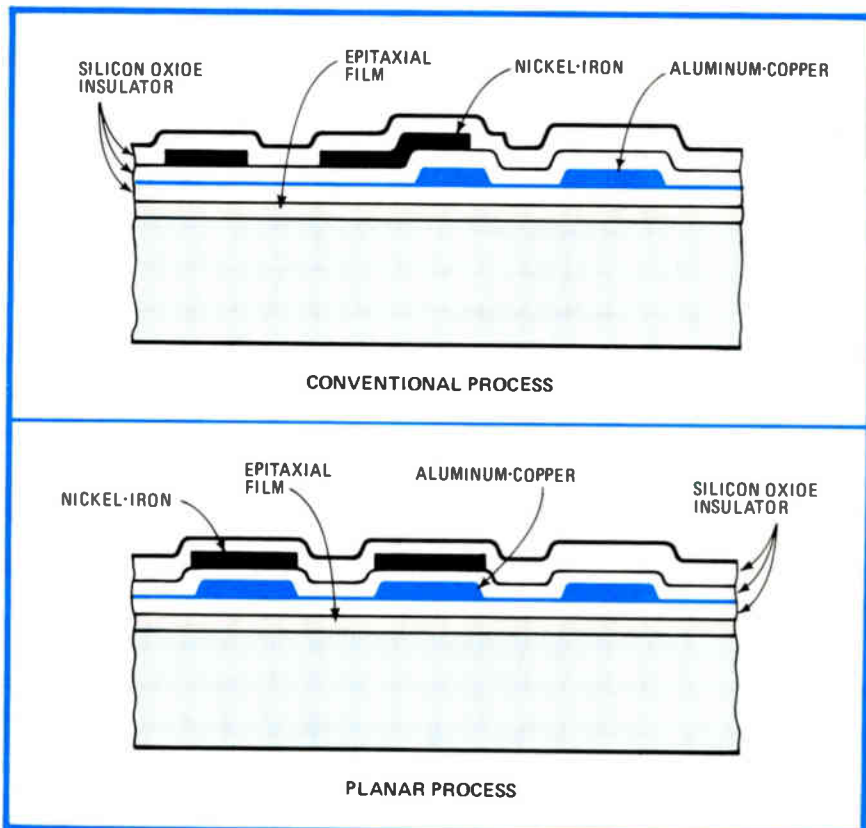
That the new organization lends

itself well to the family approach is no accident. The two-section megabit chip dices easily into 512-K parts, since each chip section is fully endowed with generator, detector, and replicators. The new 256-K chip is identical to a 512-K chip except that its loops are shorter—1,025 bits each. The 256-K bubble memory will supersede the company's earlier part, which used an unwieldy nonbinary organization.

The family approach plays into customers' needs, according to H. Dean Toombs, vice president, who

manages the magnetic-bubble operation. "Applications seem to fall into distinct memory-size requirements that cluster around the quarter-, half-, and megabit boundaries."

**Support.** For upgradability, all three parts had to use the same support circuits. The company therefore designed the controller, coil driver, function-timing generator, sense amplifier, and function driver ICs—all of which will be available in production quantities in 1980's second quarter—to work with all its bubble chips. (The support chips for



**Flatter.** Conventional 3- $\mu\text{m}$  magnetic-bubble processing requires step coverage of Permalloy over the Al-Cu conduction layer. TI's new 2- $\mu\text{m}$  process requires no step coverage.

TI's first bubble device, a 92-kilobit chip, were unable to work with the followup 256-kilobit device.)

**Process advance.** As recently as a year ago, the feasibility of a block- replicate chip that used 2- $\mu\text{m}$  bubbles was uncertain. It proved very hard to build the gates for such functions as swapping and replicating in what are called conduction-gate regions. The problem is how to cover the metalization steps with Permalloy, a process that is difficult to handle and often the yield-determining factor in production. TI's new fully planar process (see figure on p. 37) requires no steps to be covered and has made possible 2- $\mu\text{m}$  technology—a process that sometimes requires resolution down to 1  $\mu\text{m}$ .

Minimum features of 1  $\mu\text{m}$  do push the limits of current lithography equipment. The company is relying on direct-wafer-stepping

equipment with a 10 $\times$  reticle and has added its own laser-controlled alignment equipment.

What eases production of the process is its self-aligning nature, maintains Toombs. The aluminum-copper conductors are etched with dry plasma, to which the Permalloy of the second level is resistant. The alloy can therefore be used as a mask for certain portions of the gate-conduction area and thus relaxes lithographic registration and resolution requirements.

Toombs expects that the bubble family will beat down the cost of bubble memories, currently about 100 millicents per bit. No pricing has been given for the new chips, but next month two evaluation boards, which pack either a half or full megabit of memory plus support chips, will be available for \$2,100 and \$3,100, respectively.

provides vastly more I/O combinations of binary data.

"The chip logic remains binary: Tricode is only a way to transfer information in a compressed form," says its creator, Gregory W. Ledenbach, engineering manager for MOS/LSI design at the Santa Clara, Calif., company.

In the National technique, the standard TTL logic levels of 0 and 5 volts are used, along with the binary chip's high-impedance state to represent a logic 2. "It's like a two-pole switch, with a center off position, and you feed a center tap into the circuitry," Ledenbach explains.

**Implementation.** Tricode is in use in circuitry for remote-control garage-door openers marketed by Sears, Roebuck and Co. With nine inputs, it gives the door openers a reasonably safe 19,683 ( $3^9$ ) logic combinations versus the relatively insecure 512 ( $2^9$ ) binary combinations, hardly enough in heavily populated areas, Ledenbach says.

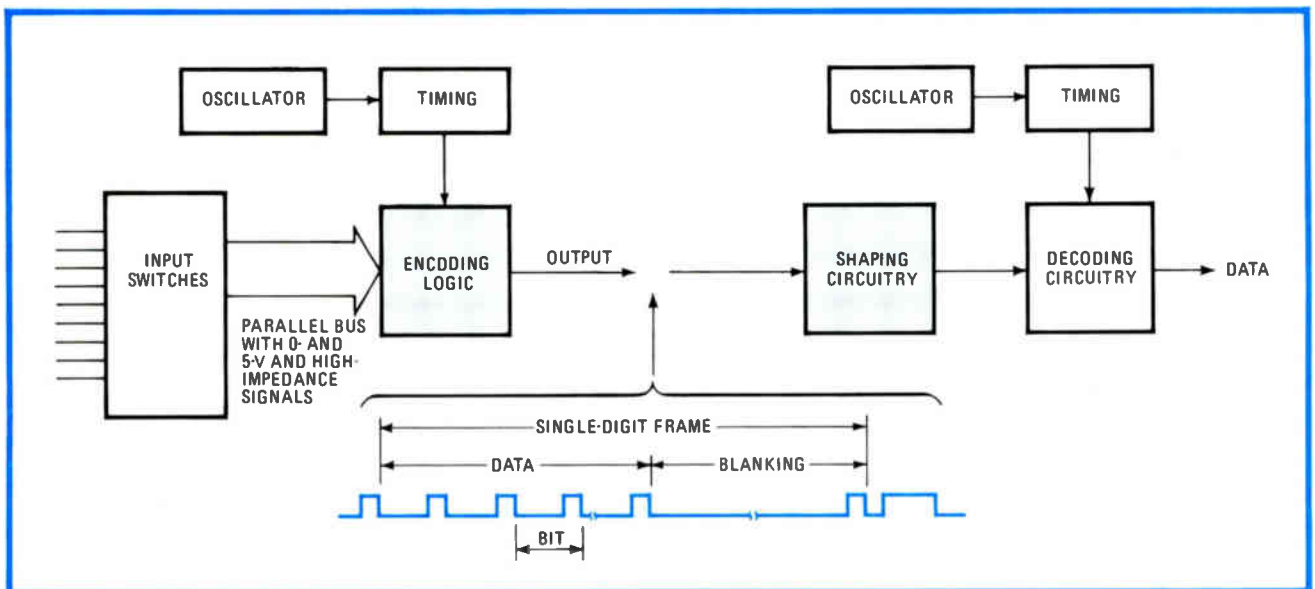
"As the number of inputs increases, the differential becomes even greater," he points out. For example, a 16-bit microprocessor with 16 I/O lines could directly address some 43 megabytes ( $3^{16}$ ) of memory as opposed to the present 64-K ( $2^{16}$ ) bytes. Another major advantage is greatly enhanced data

## Semiconductors

### Three-level addressing compresses bits to overcome package pin limitations

With large-scale integrated circuits threatening to generate more data than their input/output lines can hold, binary logic could hit a barrier

thrown up by pin counts. One way out, says National Semiconductor Corp., is Tricode, a company-devised three-level addressing technique that



**Three-level addressing.** With a logic chip like a microprocessor providing TTL logic levels plus its high-impedance state for a logic 2, National Semiconductor's Tricode circuitry converts the three-level signals into PWM waveforms, compressing the data for transfer.

security possible with the jump in logic combinations.

The encoding circuitry converts the three-level signals into pulse-width-modulated waveforms (see figure) that use the usual 0- and 5-v levels. A pulse with a 25% duty cycle represents a logic 0, a 50% cycle represents a 2, and a 75% cycle represents a 1.

The transmitted signal takes the form of repeated frames in which the variable-duty-cycle pulse is copied four times altogether and followed by a blanking period. The result is that each output line carries a pulse train with information for 0, 1, or 2, as in a true trinary scheme.

That the information for the transmitted bit is repeated in each frame enhances reliability. Circuitry in the decoder can detect any transmission error and flag it.

Few details. Until patents are granted, National will not provide details on the encoding and decoding circuitry. The company does say that a nine-digit system would employ nine input switches. The parallel buses throughout have as many lines as there are inputs.

Tricode is simple enough that the encoding could be performed by microcomputers, Ledenbach says. Decoding is relatively complex and so would best be performed by a dedicated IC to avoid eating up microcomputer overhead, he maintains.

-William F. Arnold

## Military

### Foreign companies eyeing VHSIC

A push by semiconductor companies in Japan, Europe, and Canada to share in the Very High Speed Integrated Circuit project looms as the latest threat to the U. S. Department of Defense's controversial effort. The VHSIC project, aimed at boosting semiconductor research and development efforts, is expected to carry considerable civilian fallout, and foreign participation is likely to raise American hackles.

## The money melodrama

Can the Pentagon persuade Congress to restore some \$25 million to begin Phase I of its Very High Speed Integrated Circuit program in fiscal 1980? Who stands to get the VHSIC Phase Zero definition awards (using existing funds) that have slipped a month to late October? Those questions persist as congressional conferees on the defense budget continue to ponder the issue. Program advocates in the Department of Defense and industry agreed they will have to stay tuned until next month for answers.

As the money melodrama unfolds, VHSIC insiders are betting that Congress will restore some funds, persuaded by what DOD calls "the excellence and depth" of the 15 Phase Zero proposals it has in hand [*Electronics*, Aug. 30, p. 57], as well as by DOD's promise to invoke tight management controls at the department level rather than letting the military services supervise the contracts and to establish broad rules guaranteeing that participation would provide no technological advantages to its semiconductor contractors at the expense of others. The requirement that VHSIC contractors agree to sell and license products resulting from the program, including everything from chips to production equipment, is designed to assuage the concerns of the program's vocal opponents. There will be anywhere from 3 to 12 awards. Technical evaluation of those proposals is now complete, says DOD, which is treating them as secret documents.

Even now the DOD is attempting to persuade the House and Senate Conference Committee on Appropriations and Armed Services to restore \$25 million for first-phase VHSIC contracts to the fiscal 1980 budget (see "The money melodrama"). Now program advocates inside the Pentagon are searching for a policy to combat foreign participation and its threat of technology transfer abroad.

**Internal split.** Compounding the problem of formulating that policy are divided views within the Department of State and DOD. For example, under secretary of defense William Perry, responsible for research and engineering, is known to favor the prospect of joint British and Canadian proposals from companies with an expertise in such areas as lithography. Reportedly he favors participation by companies in other member countries in the North Atlantic Treaty Organization, which has led to expressions of interest from German companies.

Moreover, the military mission in the U. S. embassy in Japan made a strong recommendation to VHSIC program chief Larry Sumney for a data-exchange agreement covering the U. S. program and Japan's VLSI project. Sumney got that proposal on a June visit to Japan, during which

several semiconductor makers indicated to him their interest in participating in the program's Phase III, to complement the principal efforts.

Sumney will not comment on reports that he was approached by companies like Hitachi and Sharp, but a copy of his memorandum obtained outside the Pentagon confirms details of the trip. Of the embassy recommendation, it says the "rationale was based on the assumption that the U. S. would gain information on Japanese efforts pertinent to VHSIC technology, such as lithography and dry-etch technology and equipment development. The obvious disadvantage would be to make data and information on development under VHSIC available to the Japanese."

**Public.** At present, Sumney will go no further than to call for careful study of the proposal. Now that the approach and the Japanese interest are becoming public, they are likely to provoke a storm of comment from U. S. semiconductor houses.

Undoubtedly, that response will be as varied as has been the reaction inside the Government. On a related issue, it should be noted that some U. S. manufacturers are looking askance at making VHSIC technology subject to the rigid export provisions of the International Traffic in Arms

Regulations of the U. S. government.

As one observer says, "Once something gets on the ITAR list, it is almost impossible to get it off," which could prevent U. S. exports of any commercial products that could evolve from VHSIC. The Electronic Industries Association and the Semiconductor Industry Association are due to make a mid-October recommendation on the subject to DOD. They are likely to favor keeping VHSIC off the list, although they undoubtedly will propose some alternate protection.

-Ray Connolly

## Memories

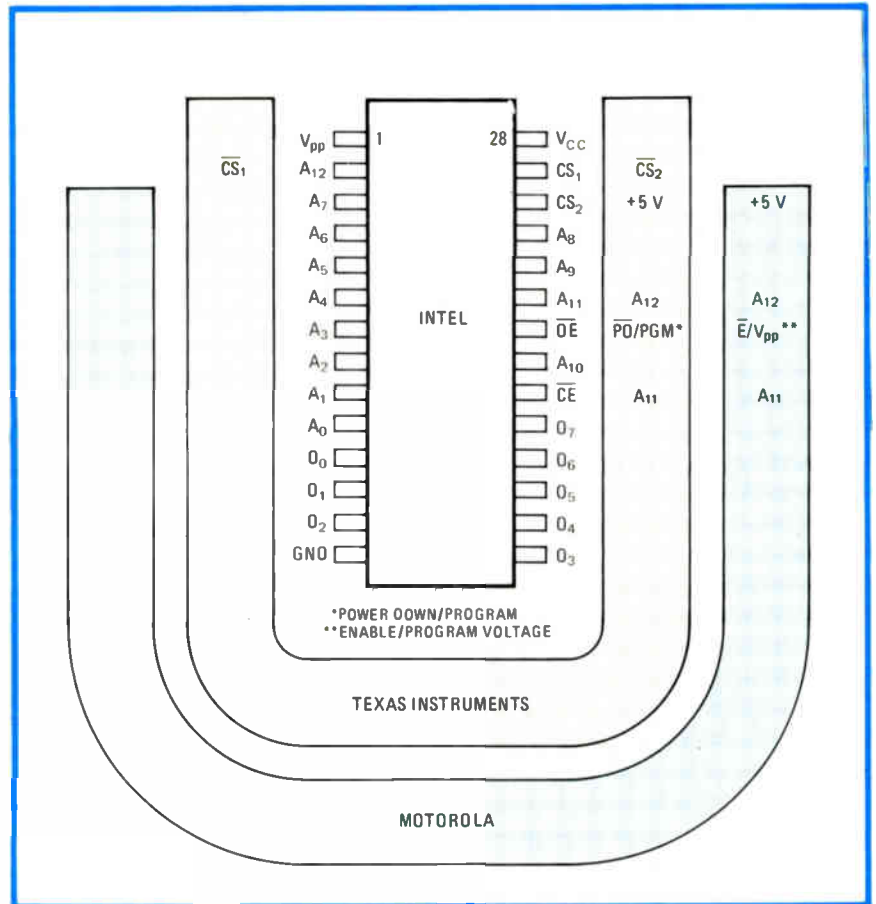
### E-PROM pinout battle looming

More than one semiconductor manufacturer these days is taking aim at the growing market for erasable programmable read-only-memory devices that run on a single supply. And as the state of the art reaches 64-K densities, a battle is looming over which E-PROM package and pinout configurations will become the standard. When the smoke clears, there may even be two "standards" left to shoot it out in the marketplace.

The first shots were fired by a couple of chip makers in announcements timed for Wescon last week. As expected [*Electronics*, Sept. 13, 1979, p. 215 and, in this issue, p. 176], officials at Motorola Inc.'s MOS division in Austin, Texas, unveiled the MCM68764, an 8-K-by-8-bit, 5-volt-only, E-PROM device.

**24 pins.** By multiplexing more than one function on a pin, Motorola was able to pack the 64-K device in a 24-pin package and avoid moving to a 28-pin package. Thus the new E-PROM should be easily interchangeable with industry standard 24-pin ROMs of equal or lower density, as well as with new 5-V 16-K and 32-K E-PROMs planned or announced as part of the new Motorola family.

Also announcing a 64-K E-PROM device was Texas Instruments Inc. The Dallas firm's 5-V-supply byte-



**Doubling up.** Like Intel, TI favors a 28-pin 64-K E-PROM, but with a power-down mode multiplexed on pin 22. Motorola multiplexed its chip-enable on pin 22 to make 24 pins do.

organized TMS2564 is housed in a 28-pin package, whereas its 32-K device, the TMS2532, is in a 24-pin package. The 2564 thus diverges not only from the Motorola approach, but also from the tack expected of Intel Corp.'s 64-K version.

Like TI, Intel is planning to move from a 24-pin 32-K E-PROM package to a 28-pin carrier for its 64-K unit. As with its 32-K device, the Santa Clara, Calif., company is expected to design its 64-K pinout for compatibility with its own ROM-E-PROM devices [*Electronics*, Feb. 16, 1978, p. 44]. Intel's 64-K pinout thus will differ from the TI approach, providing yet a third option.

It was at the 32-K level that TI caught up with E-PROM leader Intel, which had dominated the single-supply market with earlier-generation devices such as the 2716. TI announced its 2532 in March 1978, several months before Intel brought

out its 2732. The Texas company reportedly had difficulty at first in delivering the 32-K devices in quantity, however, and according to estimates by one market research firm, it is now running about even with Intel in terms of shipments of their respective 32-K E-PROMs. Quantities coming from each firm are currently pegged at about 15,000 to 20,000 units monthly.

**Choosing sides.** As noted by Larry Jordan, Intel's strategic marketing manager for its E-PROM family and other products, market preference and the ability of suppliers to deliver will ultimately determine which E-PROM approach wins out. The Intel official declines comment on when his company's 64-K device might be expected.

But in terms of its pinout approach, Intel has made its intentions clear to the Joint Electron Device Engineering Council's JC-42



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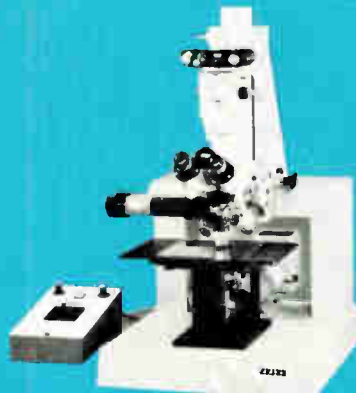
2. Epi-Microscope.

Circle 31



3. Universal.

Circle 33



4. ACM.

Circle 34



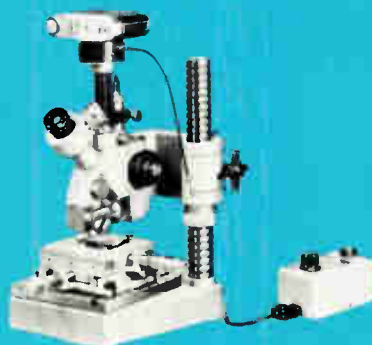
5. Ultraphot.

Circle 37



6. Stereo SR.

Circle 38



7. Light-Section Microscope. Circle 39



8. Axiomat.

Circle 40

subcommittee, which is charged with setting an industry standard for the parts. Actually, that group's recent actions suggest that both the Intel and the TI approaches may end up as standards for 28-pin E-PROM devices. In an initial ballot tabulated last month, the Intel approach barely missed the 90% vote required for industry standardization. So now a second ballot has been authorized by which members may endorse both approaches as standard.

**Precedent.** There is plenty of precedent for such a move, says Mostek Corp.'s Sam Young, who heads up the JC-42 group. In more than one case involving competing approaches in memory devices of the previous generation, the subcommittee has voted for a dual standard, leaving the final decision to the marketplace.

Young sees the current round of 28-pin package decisions as particularly critical. Standards set now, he says, affect "two or three generations" of not only E-PROMs, but other memory devices that will also require 28-pin package counts as densities go up.

There is some sentiment among industry officials that the current severe shortages of memory parts may leave room for more than one high-density E-PROM standard to develop. In the meantime, a number of manufacturers—including Mostek, National Semiconductor, and Syntertek—are known to be developing E-PROM strategies of their own. The pinout approach that these firms choose to adopt could prove to be important as the E-PROM battle unfolds. **-Wesley R. Iversen**

register set and arithmetic and logic unit and can easily become a true 32-bit processor when packaging and economics allow.

The parts join a competition that includes well-launched entries: Intel's 8086, Motorola's 68000, and Zilog's Z8000. But the Santa Clara, Calif., firm has yet to see silicon.

**Two languages.** The two smaller parts are "bilingual," says George Chao, director of microprocessor marketing. They will be able to execute an emulation of the popular 8080 instruction set as well as the instruction set common to their family, he explains.

National claims its native instruction set has 20 times the performance of existing 8080-based systems. The two devices can switch between the two instruction sets via a single software command, Chao adds. Moreover, the firm plans to support them with high-level languages.

One argument for the bilingual feature is retention of the company's existing 8-bit software base—it second-sources the popular 8080. "A user doesn't have to start from scratch," Chao says, yet can upgrade to a more powerful instruction set while—importantly—staying within the NS16000 family.

Engineers headed by Zvi Soha at National's Israel design center have packed considerable memory-addressing capability into the 48-pin CPUs. They will be made in x-MOS, the company's high-performance, fine-line MOS process.

With samples about a year away, performance specifications are far from complete, but many design features are set. They include a symmetrical architecture for the registers and memory addressing modes and powerful instructions and data types (see table). Unlike the recent three 16-bit entries, the National family will feature a uniform, unsegmented memory address.

The two smaller parts can directly address 16 kilobytes of memory, whereas the 32-bit processor handles 16 megabytes. Moreover, a memory-management peripheral chip, due for introduction at the same time, will enable all three to address 32 mega-

**Microprocessors**

**National aims at raising stakes in 16-bit game with three chips that range up in capabilities**

Coming from National Semiconductor Corp. are not one but three microprocessors, late entries in the 16-bit race. Still in the early development stage, the NS16000 family will feature not only upward compatibility, pointing towards a 32-bit processor, but also considerable

memory-addressing capability.

The three devices begin with the 16008, a 16-bit chip with an 8-bit multiplexed bus. Next is the 16016 with the same architecture and a 16-bit bus. Topping the line is the 16032 processor that has a 16-bit bus and a 32-bit general-purpose



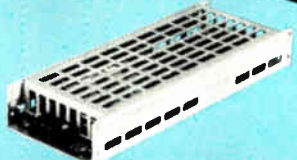
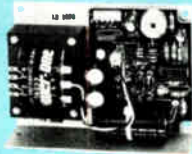



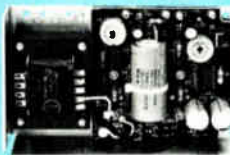
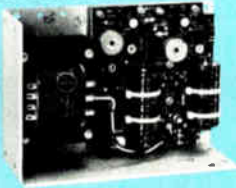
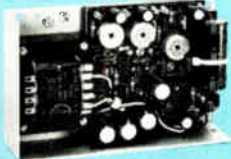

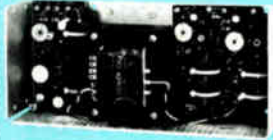
16-BIT MICROPROCESSOR DATA-HANDLING CAPABILITY						
Data types	TI 9900	Intel 8086	Zilog Z8000	Motorola 68000	National	
					16008/16016	16032
Integer: byte or word double word		X	X X	X X	X	X X
Logical: byte or word double word	X	X	X	X X	X	X X
Character strings: byte, word double word		X	X		X	X X
Binary coded decimal: byte word double word	X	X	X	X X	X X	X X X
Floating point					X	X

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## Electronics review

bytes. Chao says the theoretical limit of the 16032 is 4 billion bytes.

National plans production of the family, including a floating-point processor, in 1981 and concedes that it will be late in the 16-bit race. "A lot of designs today really need 16-bit devices, but there will be even more tomorrow," Chao notes. "People will be migrating up; performance requirements of systems will increase; and existing designs won't suit their needs. Then they're going to be looking for something else."

-William F. Arnold

## Automotive

### Detroit's processors incorporate self-tests

The specter of unsophisticated automobile mechanics trying to troubleshoot microprocessor-based engine-control systems has not deterred Detroit from embracing semiconductor technology. Still, General Motors Corp. and Ford Motor Co. are adding self-diagnosis to their electronic engine-control modules.

However, the companies diverge in the degree of microprocessor power they allot to self-testing. In its 1980 Cadillac Sevilles and Eldorad-

os equipped with electronic fuel injection, GM has programmed checks on 25 possible failures, available on a dashboard display. In two variations, Ford offers the mechanic a more limited range of computer-controlled checks that require readout instruments.

**Tradeoffs.** Each company has a basic engine-control module with some processing power available for other tasks. Ford opted for an 11-function dashboard display [*Electronics*, Aug. 2, p. 43], whereas GM settled on more under-the-hood diagnostics, discontinuing an optional trip computer in favor of gas-mileage checks only.

The 25 GM failure codes in the module's 8-K read-only memory indicate when there are breakdowns of sensors and of other parts of the engine-control system, explains Robert J. Templin, chief engineer at the Detroit-based Cadillac division. If, say, a pressure sensor fails to produce data to mix air and fuel precisely, the 6800-based microprocessor substitutes nominal values.

To isolate the fault, the serviceman orders the diagnostic mode, which appears on the light-emitting diode display of the climate-control system (see figure). A serial interface between the engine-control module and the climate-control sys-

tem provides the data path, explains Anthony Derhake, who is a staff project engineer.

"We have the capability for more codes," Templin adds, "and the control module forewarns about some potential problems, too." The system can be expanded to include failure codes for additional sensors and for other parts of the auto.

Though GM appears headed toward an instrument-free troubleshooting philosophy, Ford is relying on a multitiered instrument strategy. Its less sophisticated control module on its small cars displays eight failure modes, such as the temperature sensor, via a pulse code on a serviceman's voltmeter, explains Louis J. Graziano, who is service research and predelivery operations manager for the Parts and Services division in Dearborn.

**More checks.** Another control system introduced in the 1980 full-sized Fords provides 11 checks. They require special readout instruments that use a semaphore code rather than a digital readout.

Ford officials concede that their troubleshooting approach is too cumbersome. Therefore they are eager to incorporate more self-test capabilities. "We are exploring the use of computerized diagnostic service equipment to simplify the technician's job," notes Graziano. In a field test, the company has just shipped 200 such units that provide failure data in standard English on a video display.

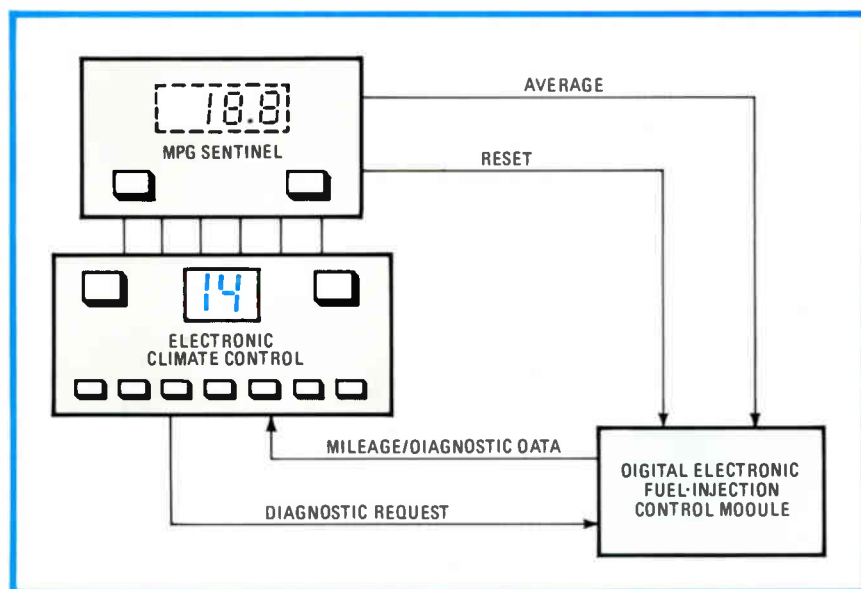
-Larry Marion

## Hybrids

### Standardization push coming on strong

The makers of hybrid circuits are enthusiastically heading for standardization. After five years of inactivity, the JC-30 Hybrid Standards Committee is resurrecting itself with considerable industry participation.

The move came at a mid-month meeting of another committee, which also is a subgroup of the Joint Electron Device Engineering Coun-



**Check it out.** 1980 Cadillacs offer an option that shows failure codes on the climate-control display when put into the diagnosis mode. A 14 indicates a failed coolant sensor.

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## Electronics review

cil of the Electronic Industries Association. At the JC-13 Government Liaison Committee, it was clear that "support for the standards move is just about unanimous," says Jedec executive secretary John F. Hessman (see "Hybrid bandwagon").

**Impetus.** Five years ago, most hybrid devices were custom, proprietary circuits, so interest in the standardization thrust faded away, Hessman says. The growth of second-sourced and pin-compatible products is rekindling the interest in standardization of testing, parts, processes, and packaging, as well as standardization of specifications.

Standard products grew as hybrid circuits became more than a transitional phase between discrete and monolithic devices, says JC-30 chairman G. James Estep, manager of advanced development at Hybrid Systems Inc., Bedford, Mass. "It turns out, that hybrids show promise of being a cutting-edge technology into the future."

Estep points to three advantages hybrids can claim over monolithics:

- Higher ratios of reliability to complexity.
- Easy mixing of technologies.
- Ever larger circuits of monumental complexity.

Underlining the thrust towards standardization is a proposed Air Force Space and Missile Systems Organization standard for ultrahigh-reliability spaceworthy hybrids. It probably will be the first military hybrid-circuit standard, and Jedec hopes to participate in its fine tuning, says Hessman.

**Rationalization.** Such a standard would rationalize a traditionally confused area of military procurement. Contractors often specify hybrids manufactured in accordance with MIL-M-38510—but since this standard applies almost entirely to monolithic devices, hybrid suppliers often can honor it only in spirit, Estep explains.

But for every silver lining, there's a cloud. "There's a tendency . . . not to think of hybrid technology as a semiconductor technology," says Estep. "Now, as the hybrid sector rationalizes its own situation,

## Hybrid bandwagon

With its first meeting scheduled for Oct. 16, the JC-30 hybrid standards committee already has a long list of members, with more to come.

Organizations already on board include AEL, AIL, Amperex, Analog Devices, Beckman Instruments, Circuit Technology, Datel-Intersil, Honeywell, Hybrid Systems, ILC Data Devices, Micro Networks, National Semiconductor, RCA, Rockwell International, Samsco, Sperry Rand, Teledyne-Philbrick, and Westinghouse. Bendix and Burr-Brown will become members soon, and JC-30 chairman Estep predicts that a dozen more firms will apply for membership shortly.

The goal of the committee is to produce a full complement of standards within the next 18 to 24 months.

it is going to have an impact on almost all other devices, because hybrids include almost all other part types." He notes that the necessary second-level standardization may be difficult for some makers of these other devices. —James B. Brinton

## Consumer

### Home earth station tunes into satellites

The joys of cable TV are lost on households beyond the cable links. Therein lies a market for relatively low-cost satellite receiving stations, says Fredric J. Hopengarten.

At 33, he is the founder, president, chief counsel, and almost the entire payroll of Channel One Inc., Newton, Mass., which will assemble, install, and service private receiving stations for those he calls the "entertainment-starved" because they cannot hook up to community-antenna television (CATV). All they need is something near \$20,000 for the ground station and a location with an unobstructed view of the satellites

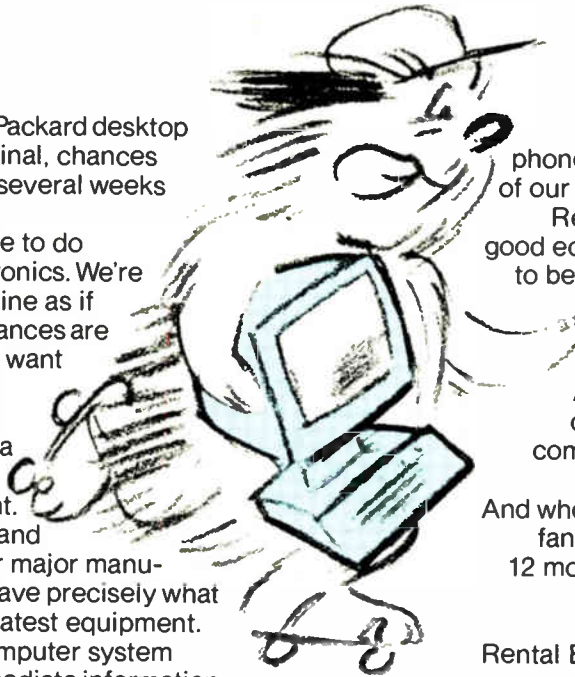
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## Electronics review

populating the southern sky. (For a related story, see p. 98.)

Though he agrees those requirements will limit demand, Hopengarten estimates at least 10,000 private earth-station installations are possible at present prices. That figure could go as high as 100,000 with decreases in hardware costs, he says.

**Price.** His Earth-link system will cost \$15,000 with a parabolic antenna 3 meters in diameter and \$18,500 with a 5-m dish. It can receive even more satellite transmissions than any one CATV operator offers.

Hopengarten will assemble the system by putting together various available components.

A possible roadblock between Channel One and its market is the Federal Communications Commission, which is considering regulation of private earth stations. Hopengarten expects a favorable outcome when the FCC announces its decision this

week. Private, passive reception of common-carrier transmissions has never been regulated and is not in the commission's jurisdiction, he asserts. Supporting his position is a brief filed before the FCC by the Justice Department.

Fifty opposing briefs were submitted by CATV companies, station owners and the National Association of Broadcasters. One major industry representative, Southern Satellite Systems, stated in its brief that satellite transmissions are "not intended for the public" except through CATV distribution.

The possibility that Earth-link presents a threat to CATV profits amuses Hopengarten. "I seriously doubt someone would pay \$15,000-plus for an earth station if he lived on a cable line and could have it all for \$15 a month. My customers will be people CATV couldn't serve in any case."

-Linda Lowe

## News briefs

### MX missile awards forthcoming

No doubt about it: the electronics share of the strategic weapons market is on the increase. Some \$500 million of \$903 million in the Air Force's first four major awards for the MX intercontinental missile will be electronics-oriented. Rockwell International Corp.'s Autonetics Strategic Systems division in Anaheim, Calif., gets the biggest electronics dollar share—\$259 million to design, develop, and integrate the guidance and control system, including the flight computer. Denver-based Martin Marietta Corp. will get more than \$321 million for weapons system assembly and test and system support. Much of its funding will go for system electronics, as well as for computers, instrumentation, and other electronics hardware supporting the company's activities. The other two five-year contracts are for development stages 2 and 4 of the propulsion system.

### Ampex to furnish 8-inch disks

A shadow over the fledgling 8-inch Winchester-technology disk drives has been whether disks can be supplied in adequate quantities in the two standard millimeter dimensions [*Electronics*, June 21, p. 83]. Ampex Corp. has now come to the rescue with its announcement that it will supply its thin-film plated Alar disk in both the 200- and the 210-mm sizes used by the disk-drive makers. Compatible with thin-film, standard ferrite, and Winchester head-technologies, the plated disks can store as many as 12,000 bits per inch, the Redwood City, Calif., company says.

### 32-bit mini line gets new top

Perkin-Elmer Corp.'s Computer Systems division is topping its 3200 series of 32-bit minicomputers with its new 3240. Said to offer about 1.6 times the performance of the 3220 introduced last spring [*Electronics*, March 1, p. 46], the unit can handle up to 16 megabytes of main memory. Prices for the basic computer start at \$76,500, with deliveries set to start next month. The Oceanport, N. J., firm says the shortage of 16-K memory chips means initial machines will be limited to 4-megabyte main memories.





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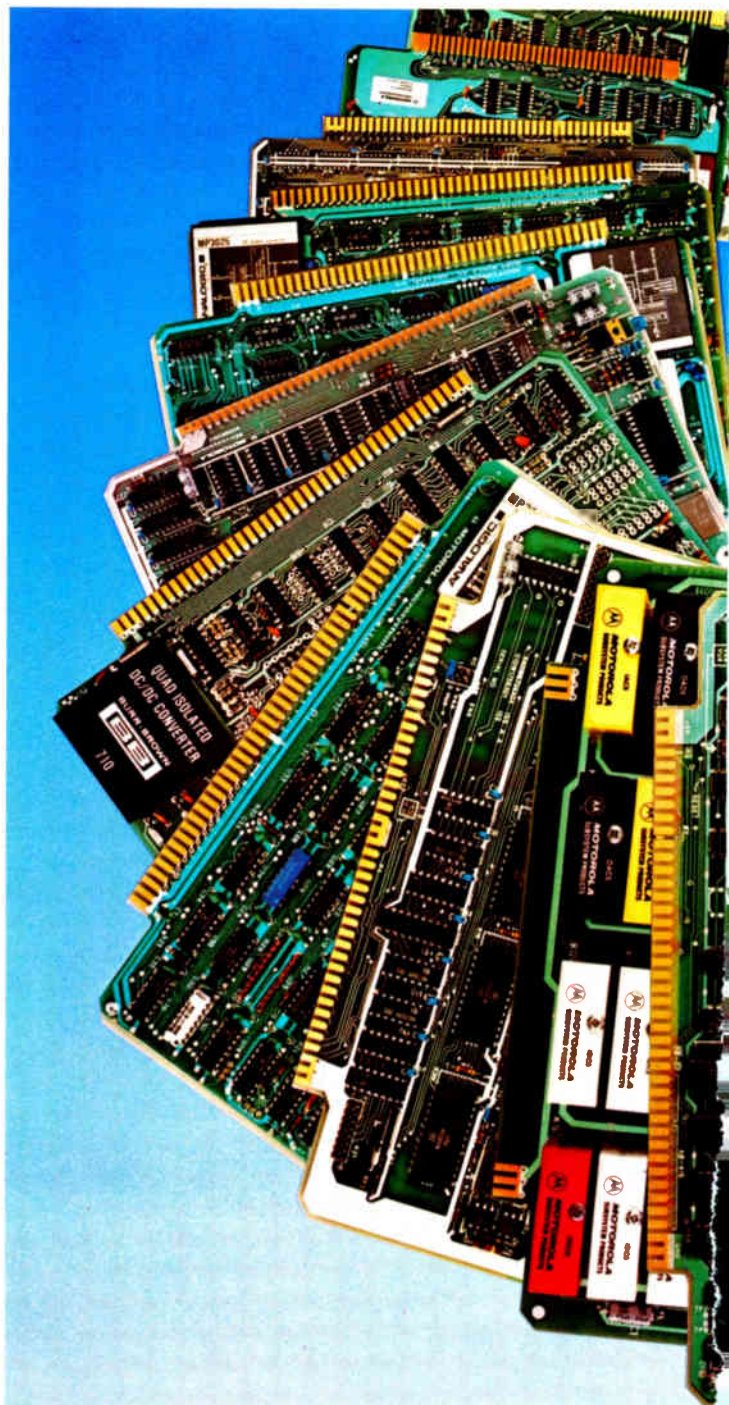
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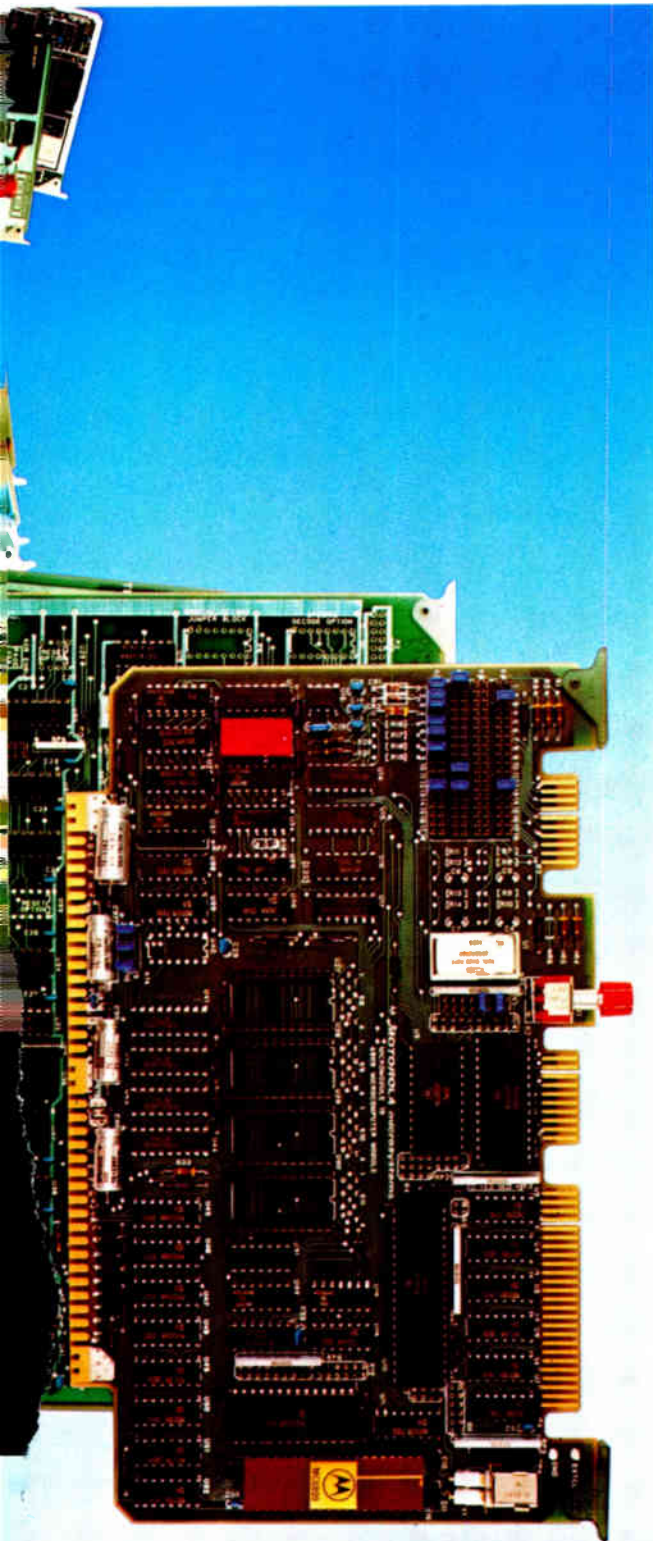
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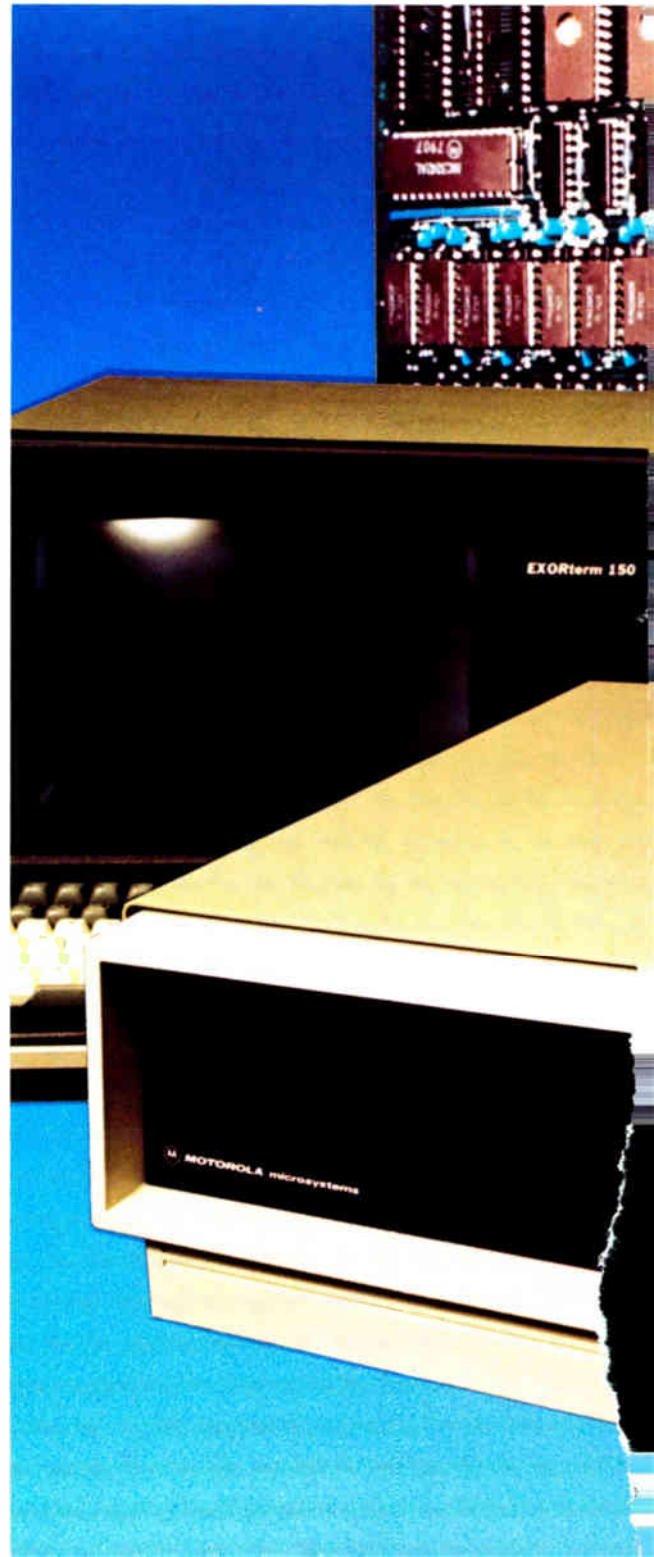
## Hardware, and the system peripherals.

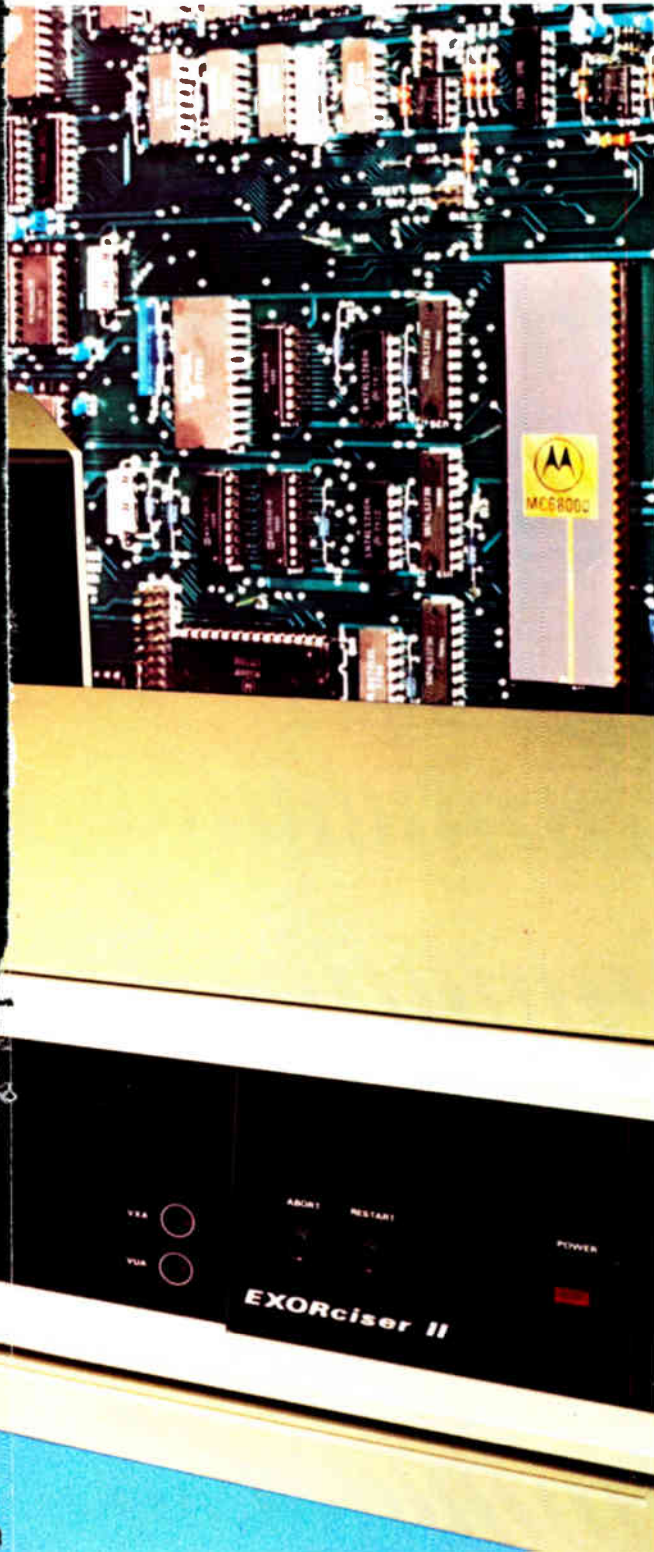
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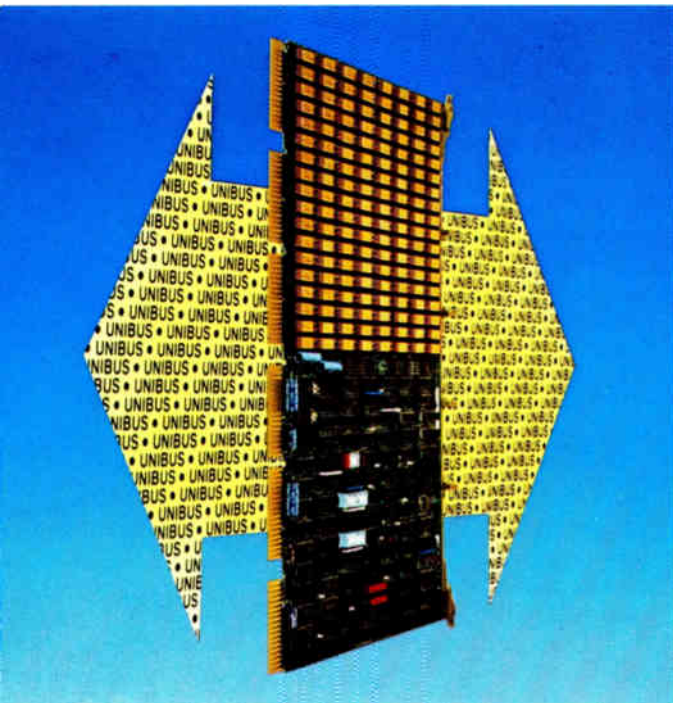
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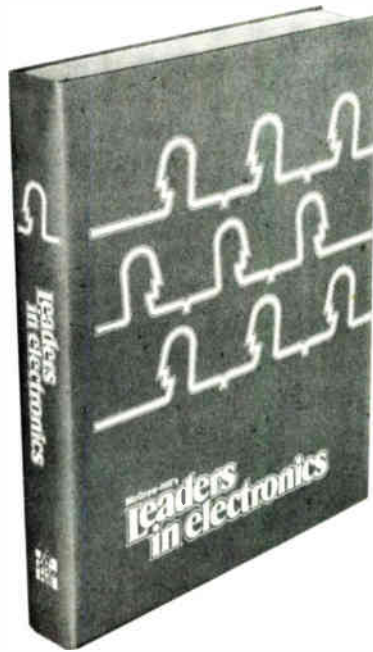
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Chmn & CEO, Microprocessor Div of Computers Inc, 1023 W Warner Ave, Dayton, OH 45479, Tel (513) 555-2000. **Born:** Mar 26, 1926, Philadelphia, PA. **Education:** MBA, Harvard Business School, 1950; BSEE, Univ of Ill., 1946; PhD (Hon), Yale Univ, 1977. **Professional Experience:** Natl Bur of Standards, 1956-74, Adm Eng; Litton Ind, 1954-56, Sr Eng; NCR Corp, 1950-54, Eng. **Directorships:** Computers Inc since 1975. **Organizations:** IEEE since 1946, Sec Head 1972-73; AAAS since 1971; Midwest Ind Mgt Assn since 1974. **Awards:** Fellow, IEEE, 1977; Public Service Award, City of Dayton, 1976. **Patents Held:** 8 in computer circuits, incl Special Circuit for Microcomputer Chip Design 1975. **Achievements:** founded Microprocessor Inc 1974; project manager of first application of microprocessors for standard interfaces 1975. **Books:** 4 incl *Small Circuits and Their Applications* (editor), McGraw-Hill, New York, 1975. **Personal:** married 1950 to Mary (Smith), children John Jr, Jane Anne, Kevin. **Residence:** 344 W 34th St, Dayton, OH 45403, Tel (513) 555-4343.

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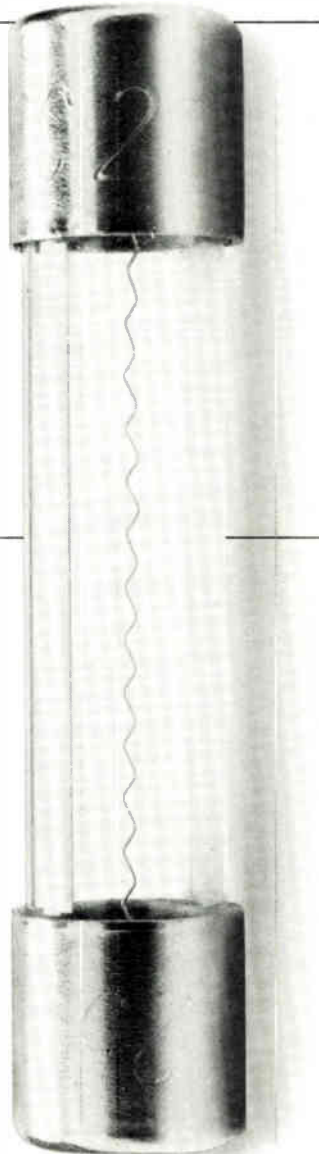
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# Washington newsletter

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## **Inquiry sought on offering by AT&T unit**

Another charge that American Telephone & Telegraph Co. is illegally offering data-processing services, this time in Pennsylvania, has been lodged with the Federal Communications Commission by the Computer and Business Equipment Manufacturers Association. CBEMA wants an investigation of Bell Telephone Co. of Pennsylvania's service using **Comm-Stor II, Sykes Datatronics Inc.'s magnetic-disk storage and retrieval system** that gives users "the data-processing services of a central processing unit in a customer-premises terminal." The trade group says that is in violation of FCC rules against common carriers offering data processing. CBEMA says it appears AT&T plans a nationwide marketing program for the Comm-Stor II, whose capability "goes well beyond" the Dataspeed 40/4 service already offered by the Bell System.

## **Pentagon wants Thermalloy barred as semicon supplier**

The debarment of Thermalloy Inc. and its president, David Kennington, as a manufacturer or supplier in the military market is being sought by the Defense Logistics Agency. This follows the conviction of the large Dallas-based supplier of semiconductor accessories for fraudulently certifying "**that transistor mounting pads and ceramic insulators [heat sinks] were made of material which met military specifications, knowing that they did not.**" The Government also expects to sue to recover damages from the substitution scheme. Thermalloy and Kennington pleaded guilty and were convicted last month in U. S. District Court in Dallas on nine counts of making false statements. Thermalloy was fined \$80,000 and Kennington \$10,000. The maximum period of debarment is three years.

## **Rescue system test using satellites set for 1982**

Test and evaluation of a worldwide search and rescue system using satellites and doppler shift techniques will begin in 1982 as a joint effort of the U. S., Canada, and France, with the possible entry of the Soviet Union later. The 15-month orbital trial of the Satellite-Aided Search and Rescue System (SASRS) is expected to dramatically reduce rescue response time to aircraft and ship accidents **by locating and fixing emergency sites within 13 miles.**

Under the three-party agreement, Canada will provide spacecraft transponders and France will provide receiver-processors to be placed on U. S. National Oceanic and Atmospheric Administration polar-orbiting environmental satellites. The National Aeronautics and Space Administration will modify and launch the satellites and develop experimental 121.5-MHz and 406-MHz emergency beacons for planes and ships to be used with the system. The SASRS will measure the varying doppler shift in the emergency transmitter signal as the satellite approaches, passes, and moves away from the site. It will then transmit the data to ground computers to pinpoint the location and alert rescue forces. Negotiations on a compatible system are under way with the Soviet Ministry of Merchant Marine.

## **U. S. finally sues for dumping duties on Japanese TVs**

The Justice Department is finally moving **to recover \$30 million in unpaid duties on Japanese television receivers dumped on the U. S. market 1970 and 1974** by filing seven civil suits in as many Federal District Courts against a total of 34 defendants. The Treasury Department found in 1971 that Japanese sets were being dumped on the U. S. market at prices less than those in Japan, but it has failed to collect duties in the past because of what outraged American producers label political considerations—notably,

to maintain favorable overall relations with Japan.

Defendants named as owing more than \$1 million each in duties are five U. S. subsidiaries of Japanese manufacturers, including: Matsushita Electric Corp. of America, which makes Panasonic, and a company it controls, JVC America Inc.; NEC America Inc.; Sanyo Electric Co.; and Sharp Electronics Corp. Other defendants include bonding and insurance companies that guaranteed duty payments. The U. S. Customs Service says it is weighing assessment of additional millions of dollars in dumping duties for the years since 1974.

## **October shutdown set for CTS, first 12-14-GHz satcom**

After 3½ years and more than 160 American experiments, Canada's Communications Technology Satellite (CTS) will be shut down at the end of October because of degraded signals. The world's first 12-to-14-GHz satellite, called the forerunner of commercial broadcast satellites, was designed and built by Canada's Department of Communication with the U. S. National Aeronautics and Space Administration. It provides a solar-powered traveling transmitter with 10 to 20 times the broadcast power of current communications satellites. The CTS, which almost doubled its two-year design lifetime, "taught us that new frequency bands can be tapped successfully" and "demonstrated that low-cost earth terminals may be substituted for conventional big-dish antennas," says NASA's Daniel Shramo, director of space system and technology at the Lewis Research Center.

## **Redesign urged for mass transit uncoupling systems**

A call for redesign of semiautomatic car-coupling circuitry for rapid transit systems has been issued by the National Transportation Safety Board (NTSB) to improve evacuation of passengers from disabled or burning trains in tunnels. The recommendation to the Urban Mass Transportation Administration follows an investigation of a short-circuit fire on a San Francisco Bay Area Rapid Transit train in the transbay tube in January. In the BART accident, a short in the train's control circuit prevented the on-board system from uncoupling the damaged cars and removing passengers on undamaged cars. An NTSB survey of six other transit systems in New York City, Long Island, New Jersey, Chicago, and Philadelphia also showed that a similar short could prevent uncoupling of cars from inside the train.

## **Addenda**

The Air Force says its Rome Air Development Center in New York State is exploring development of **alternative architectures for the 1990s requirements of the Air Force's Intelligence Information Processing System**. Responses are expected by Oct. 1. . . . **Development of a standard interface for data modems and telephone lines** will begin Nov. 13 with the first meeting of the Electronic Industries Association's new subcommittee on telecommunication network interfaces (TR-30.3). The chairman will be GTE's John Skaug. The EIA is recruiting participants—Skaug's telephone: (203) 357-3201. The first two projects will be to develop interfaces between data terminals, on the one hand, and the four-wire private-line data channel and the public switched telephone network.

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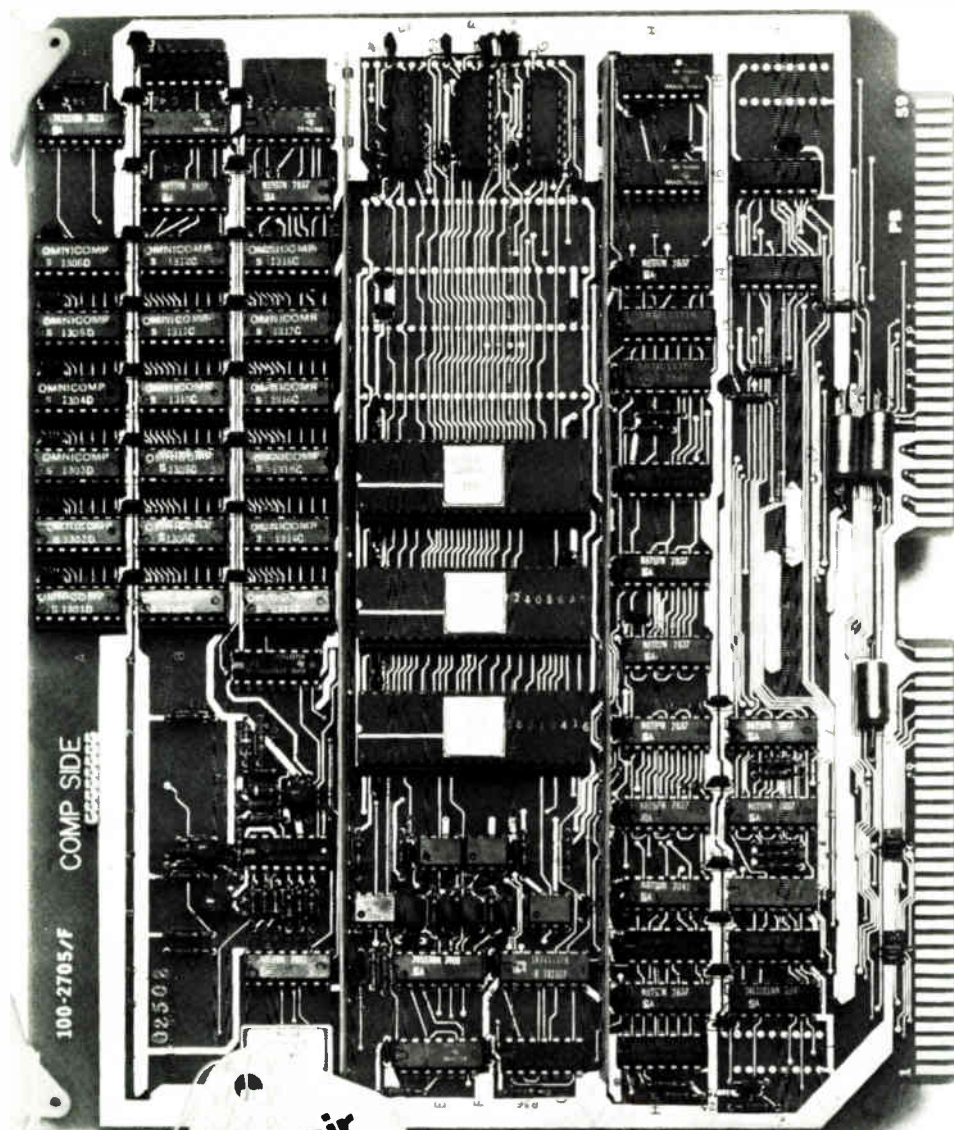
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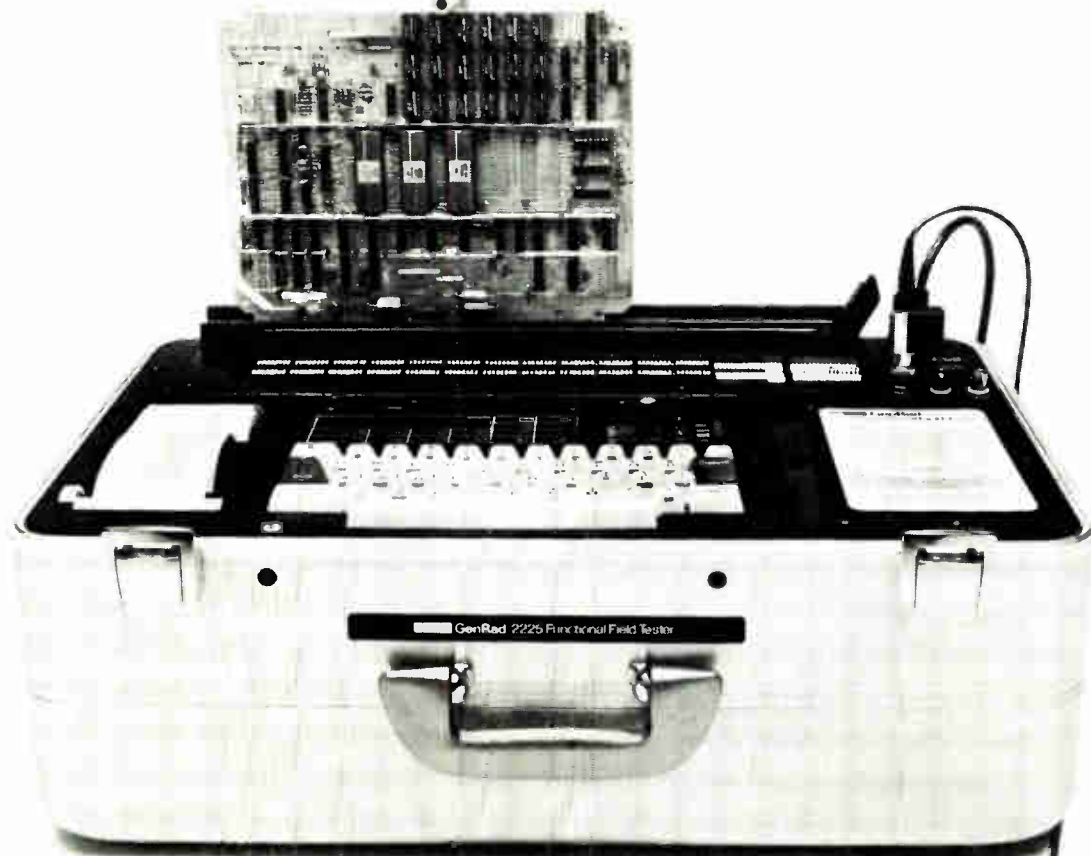
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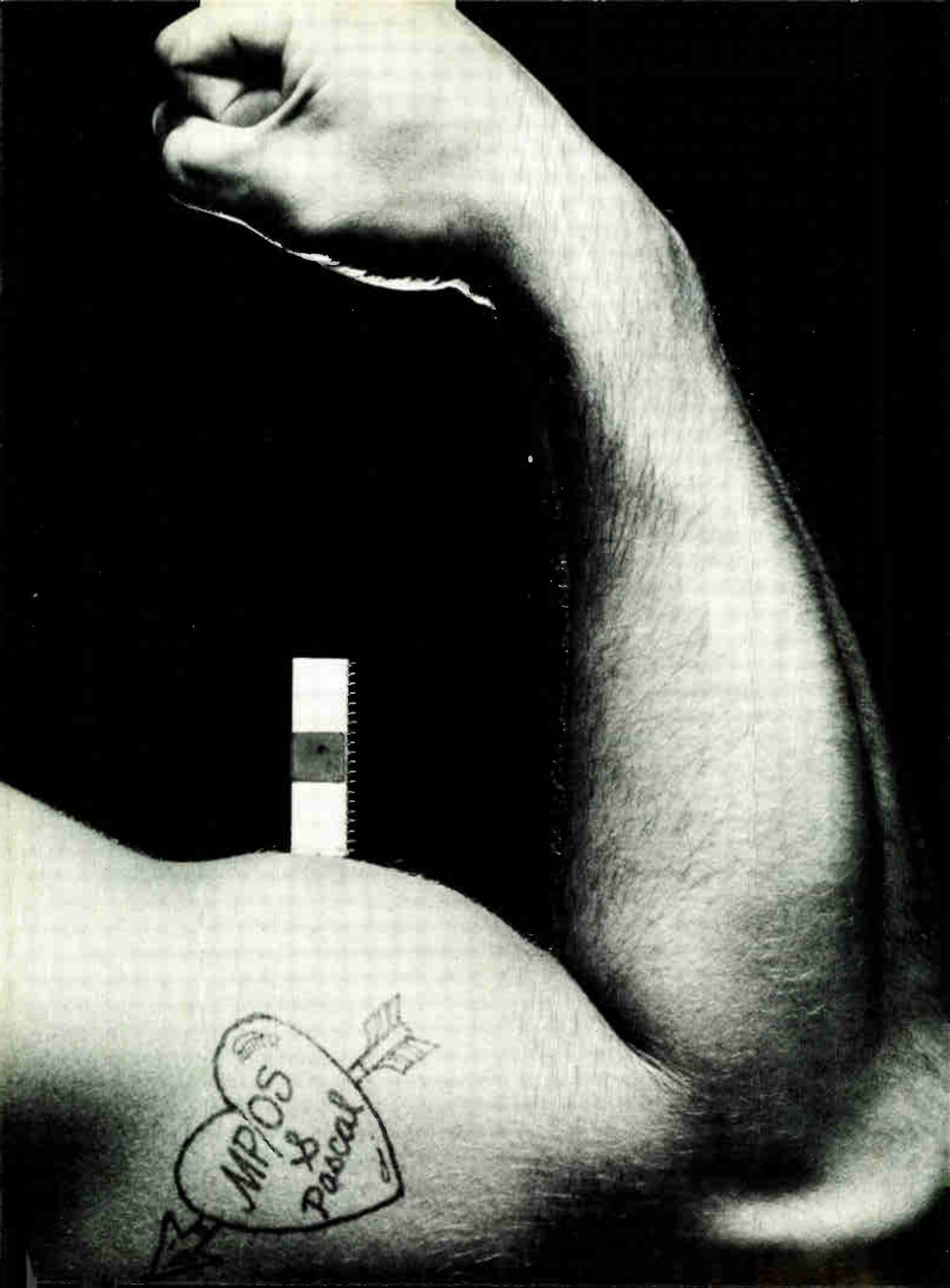


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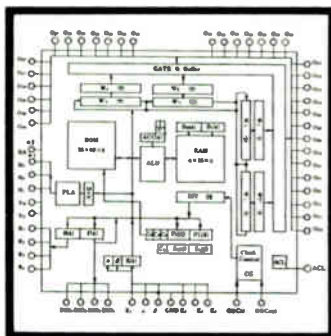


## 4-bit 1-chip C-MOS microcomputers for direct interface with LCDs

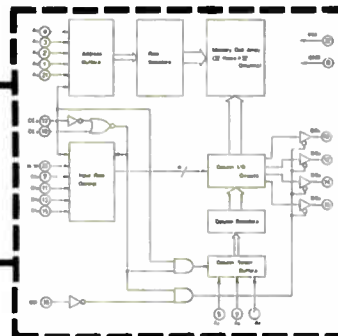
Sharp gives your products a boost in reliability and performance with these two low power consuming microcomputers. They provide direct interfacing with LCDs (accurate time control with crystal oscillator). They can be practically incorporated for the controller of telephone dialers, for programmable digital timers, cash registers,

vending machines, calculators and countless other products. They come with high ROM/RAM capacity, static shift register, 15-stage divider with reset, and other peripheral circuits on 1 chip. And, best of all, Sharp mass produces these tiny chips with a system that provides a substantial reduction in cost. So look over the specs below, take your pick and order today. Then watch your products do more and do it better.

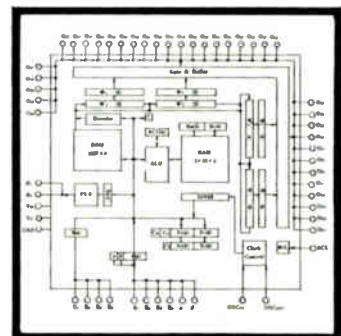
SM-4



1K RAM



SM-5

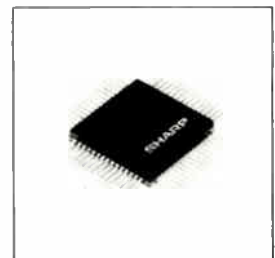


### C-MOS SM Series (4-Bit 1-Chip Microcomputers)

	Cycle time (Typ)	Vcc	Pd (Typ)	Instructions	ROM (bit)	RAM (bit)	Package
SM-4	62.5 $\mu$ sec.	-3V	0.06mW	54	2268 $\times$ 8	96 $\times$ 4	60 Flat
SM-5	62.5 $\mu$ sec.	-3V	0.06mW	51	1827 $\times$ 8	65 $\times$ 4	60 Flat

### C-MOS Static Random Access Memories

Model No.	Constitution (bit)	Access time (Max.)	Cycle time (Min.)	Supply volt.	Package	Remark
LH-5101S	256 $\times$ 4	3000 nsec	3000 nsec	3V	22 Dip	Expansion RAM for SM-4
LH-5101W	256 $\times$ 4	800 nsec	800 nsec	5V	22 Dip	
LH-5102	512 $\times$ 4	1200 nsec	1200 nsec	5V	22 Dip	



### SM-4 applications

Auto telephone dialers, AM/FM digital display units, home health equipment, clock-calculators, programmable remote controls, programmable digital timers, etc.

### SM-5 applications

Pocket bells, thermometers and pulse counters, cash registers, POS terminals, vending machines, controllers for home appliances and audio equipment, etc.

# SHARP

For further information, write to:  
Mr. Nobukazu Yagi, Sales Representative  
**SHARP ELECTRONICS CORPORATION**  
10 Keystone Place  
Paramus, New Jersey 07652



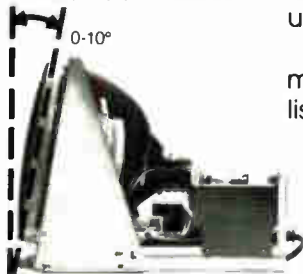
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### **Japanese transmit 800-Mb/s optical signal over 30-km fiber**

An 800-megabit-per-second signal has been transmitted through 30 km of continuous single-mode fiber-optic cable with an error rate of less than  $10^{-12}$  by researchers at the Yokosuka Electrical Communication Laboratory of the Nippon Telegraph and Telephone Public Corp. The input injected into the fused-quartz cable was  $-4$  dBm. The signal source for the experiments is a  $1.3\text{-}\mu\text{m}$ -wavelength indium-gallium-arsenide-phosphide laser operating at room temperature. The attenuation at this wavelength is much lower than at the  $0.85\text{-}\mu\text{m}$  wavelength commonly used for laser transmission. Overall loss of the optic cable at this frequency is only  $0.73$  dB/km, including the losses in the splices that are required at 2-km intervals. Furthermore, total dispersion at this wavelength can be reduced to virtually zero, making possible an extremely wide bandwidth.

### **CII-HB Introduces two mainframes with fast bus**

CII-Honeywell Bull introduced last week a pair of mainframes featuring three levels of distributed architecture and a bus that can handle 6 megabytes per second. The DPS 7/80, which falls between IBM's 3031 and 3032 models, according to the Paris-based firm, contains a single processor with a 16-kilobyte cache memory. The DPS 7/82, with two processors and two 16-kilobyte cache memories, falls between IBM's 3032 and 3033. **Both use current-mode logic.** Deliveries will start late next year.

### **Toshiba to show prototype optical-disk file system**

Toshiba Corp. may get a jump on potential competitors by readying a laser-based optical-disk file system for facsimile use. This technology is the subject of much attention for audio-visual use and of continuing research for data storage (see p. 96). In addition to laser writing and reading on the disk in a manner similar to a system being developed by Hitachi Ltd. [*Electronics*, July 19, p. 68], Toshiba's unit will include a laser scanner to encode information from documents for input and a laser printer that provides output copies similar to those obtained from an office copier. Each disk will store 10,000 average-sized pages with a resolution of 8.5 lines per millimeter. Sales are scheduled to start in late 1980 or early 1981. **The company says it will be the first to demonstrate a complete prototype system** when it does so at the end of November. The probable price of the system is between \$35,000 and \$45,000; disks will cost \$22 to \$45 initially. Hitachi, says its planned date for a commercial system is similar, but competition from Toshiba might speed development.

### **Phone voice-input unit doesn't care who talks to it**

A telephone voice-input system that recognizes the speech of most callers and converts each word of a limited vocabulary into a unique digital code for computer entry has been developed by Hitachi Ltd. The company says that the standard word patterns stored in the system have been derived from the pronunciation of 100 persons, male and female, young and old, and **disregard the individual differences among speakers.** This approach is unlike that of most available systems, in which the speech pattern of each user is registered before use. The basic HR-150 speech-recognition system is designed to be connected to a single telephone circuit. For most applications, it would be combined with a display or a speech-response system, both of which are readily available from Hitachi and others. The price varies from some \$22,000 for a unit with patterns for 16 words to about \$67,000 for one with patterns for 128 words. It is built around a fast 8-bit microcomputer using the Am2901 4-bit-slice microprocessor.

## International newsletter

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### **British government splits BPO, ends phone receiver monopoly**

The British government will split the British Post Office into autonomous public corporations for posts and telecommunications and end the BPO's monopoly on the supply of telephone receivers [*Electronics*, July 19, p. 88]. The move will allow customers a greater choice while increasing the competition for the post office's traditional suppliers, GEC Telecommunications Ltd., Plessey Telecommunications Ltd., and Standard Telephones & Cables Ltd. However, there won't be an immediate free-for-all. **Talks now starting between the Department of Industry and the three firms are aimed at granting a grace period during which British manufacturers can ready more attractive and competitive offerings.**

### **Japan to get own version of the 8086**

Japan will have its own source of the 8086 microprocessor when Nippon Electric Co. starts shipping its version in the second quarter of 1980. NEC says it is developing the device on its own. **It will thus be the second domestically produced one-chip 16-bit microprocessor, after the  $\mu$ COM-1600, also produced by NEC.** The latter was described at the 1978 International Solid State Circuits Conference and first used in the company's NEAC 100 and NEAC 150 small-business computers that went on sale last October [*Electronics*, March 2, 1978, p. 63, and Dec. 7, 1978, p. 71], but it lacks some of the 8086's general-purpose attributes.

### **Matra to build first French telecom birds**

The Aerospace division of Matra SA in Vélizy, a Paris suburb, will build France's first telecommunications satellites. Matra's \$83 million contract awarded last week, is for three satellites, two of which are to be launched in late 1982 and early 1983, respectively, with the third a standby. Télécamm 1 will handle digital data communications within metropolitan France and telephone and television transmissions between France and overseas French departments in the West Indies and French Guiana. For data communications within France, the satellite will use six repeaters, each capable of transmitting 25 megabits per second, with up links in the 14-to-14.25-GHz band and down links in the 12.5-to-12.7-GHz band. The overall cost of the project is put at \$355 million.

### **Addenda**

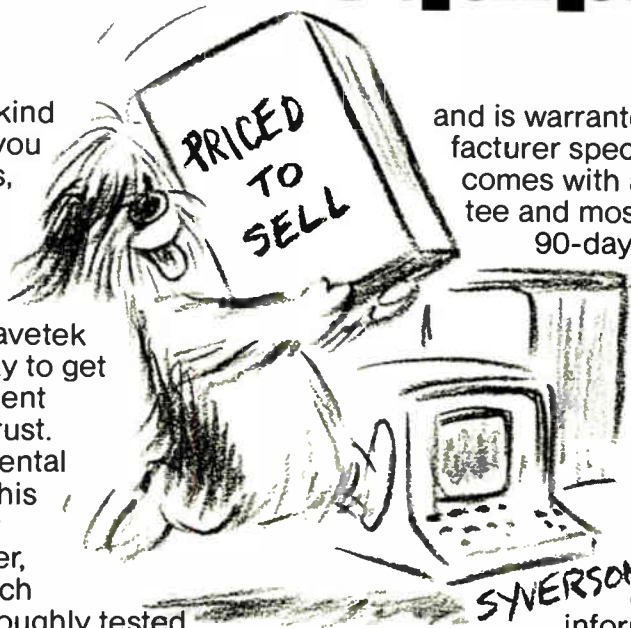
**Siemens AG, its Austrian subsidiary, and Thomson-CSF will furnish \$1.8 billion worth of telephone equipment to Egypt over the next four years.** The West German, Austrian, and French companies will supply public and private digital time-division switching exchanges, telex equipment, cables, and transmission facilities. . . . **Mitsubishi Electric Corp. has joined the 2-k-by-8-bit static memory parade with its M58725S (ceramic) and M58725P (plastic) n-channel MOS devices.** The random-access memories feature a maximum access speed of 200 ns, power dissipation of 200 mW typically and 400 mW maximum, and standby dissipation of less than 50 mW maximum . . . After intensive investigations of different consumer video-disk systems, West Germany's Grundig AG has opted for the Video-Long-Play (VLP) technique from NV Philips Gloeilampenfabrieken in the Netherlands and plans to eventually produce the equipment itself. Grundig-labeled systems, built to PAL color TV standards, will go to market "whenever there is an ample supply of VLP disks with German-language programs and movies," the Nuremberg-based company says. In a related development, **Philips recently concluded a licensing deal with Sharp Corp.** that lets the Japanese firm produce and market VLP units.



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**GenRad 1933-9714 Sound and Vibration Analyzer System.** 5 Hz to 100 kHz, 10 octave bands, microphone input, sound levels 10 db to 130 db re 20  $\mu$ N/m<sup>2</sup> with 1-in. microphone. \$2350.

**Hewlett-Packard 8660B Synthesized Signal Generator.** 10 kHz to 1300 MHz, synthesizer stability  $\pm 3 \times 10^{-8}$  24 hrs., 1 Hz resolution, calibrated output over 150 db range. AM FM or pulse modulation, TTL programmable. Requires plug-ins. \$6300.

**Hewlett-Packard 3460B Digital Voltmeter.** 1 V f.s. to 1 kV, acc.  $\pm 0.004\%$ , range 1 VDC f.s. to 1 kVDC, acc. = 0.004%, 5-digit display. \$1850.

**Tektronix 7D01 Logic Analyzer.** Acquires up to 16 channels of data into 4096-bit memory at asynchronous sample intervals from 10 ns to 5 ms, or synchronously with a clock of up to 50 MHz. \$3050.

**Data I/O Model IX PROM Programmer.** Direct readout of all commercially available PROMs; 2k x 8 RAM buffer; auto error detection; keyboard data entry. \$1795. Personality card sets and socket adaptors also available (price upon request).

**Honeywell 1858-T79 Fiber Optic Recorder.** DC to 5 kHz, 18 chan., sens.  $\pm 100 \mu$ V to  $\pm 300$  V depending on input module. Price without input modules. \$4875.

**Dranetz 606-3/101/103 Power-Line Disturbance Analyzer.** Storage capability for Multiple Faults; three input channels 1  $\phi$  or 3 $\phi$  — 115, 230, 460 volts; measures — slow average RMS changes — SAGS, SURGES, and IMPULSES that have occurred; alarms and prints when adjustable thresholds exceeded. \$2975. (\$3495 with 101, 103 options)

**Tektronix 465 Portable Oscilloscope.** BW 100 MHz; display 8 x 10, 5 mV/div to 5 V/div sens.; sweep rate 50 ns/div to 0.5 s/div; x10 magnifier; dual trace; delayed sweep; x-y operation. \$2095.

**Hewlett-Packard 141T Spectrum Analyzer Display Section.** Normal persistence approx. 0.1 sec., variable persistence 0.2 sec. to 1 min., storage time 2 hours, use in Spectrum Analyzer with 8550 series RF & IF plug-ins. \$2125 (IF and RF sections also available.)

**Tektronix 7904 Oscilloscope.** 500 MHz; display 8 x 10; accepts 4 7000 series PIU; CRT readout. \$4850.

**Philco-Sierra 340B Envelope Delay Test Set.** 300 Hz to 110 kHz, sweep 0.5 sweeps/min, 2 sweeps/min, or 4 sweeps/min, delay meas.  $\pm 20 \mu$ sec. to 18.5 msec. \$3650.

**Honeywell 5600 Magnetic Tape Recorder.** 7 data channels with  $\frac{1}{2}$  inch heads or 14 channels with 1-inch heads, to 300 kHz direct. to 40 kHz FM, elect select speeds 15/16 ips to 60 ips. \$8350. Full complement of electronics available (price upon request).

**Brush 260 Strip Chart Recorder.** 1 mV to 500 V, chart speed 125 mm/sec. to 1 mm/min., incl. four event markers, pressurized ink, response DC to 100 Hz. \$5400.

**Beehive Mini Bee II Terminal.** 25 lines x 80 characters, 6.3" high x 8.4" wide, 64 characters ASCII, serial RS232C communication interface. Transmission rate up to 9600 baud, 10 or 11 bit word. \$1350.

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## Dc electroluminescent panels get green light for auto displays

by Kevin Smith, London bureau manager

Emerging from lab, technology will appear in instrument combination from Smiths; full dashboards set for future

New kinds of displays are moving from the research labs to pilot production at Smiths Industries Ltd.'s Vehicle Instrumentation division. After several years of work, the company's dc electroluminescent technology, which produces a pleasing bright yellow display on a glass substrate [*Electronics*, March 3, 1977, p. 55 or 3E], will make its debut next year in a combined tachometer, battery-condition indicator, and digital clock for after-market sales.

For small displays, Smiths is evaluating other technologies—a Motorola 68000-based trip computer introduced at the Sept. 13-23 International Automobile Exhibition in Frankfurt, for example, will use a vacuum-fluorescent display. Both the new electroluminescent panels and the trip computer will be manufactured at a facility equipped with a clean room that is being built to handle the new technology. The Acton, North London, plant, which is financed in part with government funds, will also be used to make hybrid circuits for display drivers.

For the long term, explains Brian Shepherd, technical director of the Vehicle Instrumentation division in North London, Smiths plans to custom-fabricate entire car dashboards on a single glass substrate for auto makers, using its dc electroluminescent technology. It has already



**To market.** Smiths Industries is readying the first use of its dc electroluminescent display technology, a three-instrument combination for automotive after-sales.

delivered prototype systems to several European manufacturers for evaluation, but while waiting for manufacturers to commit to the new technology, it aims to establish a production capability and prove the technology in the marketplace by attacking after-market sales in car accessories.

The attraction of the technology, says Shepherd, lies in its excellent display qualities, its potential for mass production, and the ease with which entire displays can be customized for different manufacturers. Construction is carried out by a process of photolithography, evaporation, and screen printing, promising low-cost panels.

**Licensed.** The basic dc electroluminescent technology licensed from Phosphor Products Ltd. [*Electronics*, July 1, 1977, p. 36.] uses zinc-

sulphide powder phosphors doped with polycrystalline copper and manganese that can be screen-printed onto a glass substrate. The three-instrument combination to be launched next year, for example, has a display on a glass substrate measuring 6 by 3 inches. These panels, says Shepherd, can be manufactured six at a time. (The largest display the group has produced measures 16 by 4½ in.)

Because dc electroluminescent displays have a long afterglow, they lend themselves to multiplexed operation. But one disadvantage is the 120-volt driver voltage needed for operation. Smiths gets around this problem by splitting the driver requirement between integrated front- and back-plate driver circuits operating in a push-pull mode so that each has to deliver only 60 v,

## Multiplexing the display

The multiplexing scheme worked out by Smiths Industries with Plessey Co. for its dc electroluminescent auto displays simplifies interconnection and cuts down on the number of driver circuits needed for a fully integrated panel. With their arrangement, a back-plate driver circuit is required for each instrument integrated into a single display, but only one front-plate driver circuit is needed for all the instruments.

Controlling both front- and back-plate drivers is a low-voltage integrated circuit, called a "logic multiplex" IC, that divides the multiplexing frame into 80 sections, or time slots. The IC driving the front panel scans all segments sequentially. It converts a 4-bit binary-coded-decimal timing signal from the multiplexer-controller into a series of 10 sequential 200-milliampere outputs. In an 80-segment analog bar-graph speedometer, for example, segments 1, 11, 21, and so on, are linked to the first 200-mA output. The back-plate driver switches segments 1 to 10, 11 to 20, 21 to 30, and so on. It is similar to the front-plate driver but has only to convert a 3-bit binary signal into a series of eight sequential outputs.

The logic multiplexing IC also generates an inhibit signal to switch the back-plate electrode off at the correct scan time. In the speedometer function, for example, an internal ramp voltage, reset at the beginning of every frame, is compared with the speedometer's frequency-to-voltage converter output. When they are equal, the back plate is switched off. —K. S.

which is within the capabilities of several bipolar processes.

**Help.** In fact, Smiths worked with Plessey Co.'s Allen Clark Research Centre to develop the needed integrated circuits. However, the work took longer than anticipated, putting the program back a year, according to Shepherd. Now, he says, the company has a set of seven ICs that can be used as building blocks.

One of the biggest and most complex provides a regulated inverted supply of 120 v ac at 10 watts from the car battery. It also incorporates the electronics for speedometer and tachometer drives. The stabi-

lized power supply is designed to work with an external switching transistor and a small ferrite core to produce various voltages. It can thus be used with several display technologies. Two channels of frequency-to-voltage conversion on the chip provide dc voltages proportional to engine and road speed that are fed to the logic multiplexing chip.

A serializer, an odometer register, and a digital clock circuit are among the other chips. With this building-block kit, Shepherd estimates that dashboards would be competitive with electromechanical versions right now.

## Japan

## 2-K-by-8-bit static RAM dissipates little power with C-MOS periphery

Hitachi Ltd. is readying a fast 2-K-by-8-bit static random-access memory using its proven Hi-CMOS process. The approach—which surrounds an n-channel static-cell array with a complementary-MOS periphery that includes a bipolar pull-up transistor—features extremely low standby power dissipation that will make the part outshine the two other 2-K-by-8-bit static RAMs, from Tex-

as Instruments and American Microsystems [*Electronics*, July 20, 1978, p. 39; May 24, 1979, p. 137].

**To come.** The process shows even greater promise because of its speed—Hitachi's 4-K-by-1-bit 6147 sports a maximum access time of 55 nanoseconds [*Electronics*, April 26, 1979, p. 126]. Thus it is likely the firm will follow soon with a 16-K-by-1-bit RAM that would be a good

candidate for mainframe cache and buffer memories.

As with the 4-K part, the 16-K RAM—the subject of a paper at the recent International Conference on Solid State Devices in Tokyo [*Electronics*, Aug. 30, p. 85]—uses four n-channel MOS transistors and two polysilicon load resistors with values in the tens of gigohms for each memory cell, with the cells fabricated in a p well.

Hitachi engineers are able to eliminate the usual aluminum power-supply line by leaving an n-type island in the p well in each cell and feeding the power-supply voltage through the n-type substrate (see figure). The p-type silicon in the p well surrounding each island, though, behaves like the gate of a buried junction field-effect transistor and pinches off the current if the island is smaller than about 8 by 8 micrometers.

The area of the n island is the only control available—other than doping levels—since the voltage of the p well that forms the gate cannot be varied. The design is not critical, however, because the only requirement is that the resistance of the J-FET should be one tenth or less that of the load resistor—which is on the order of 60  $\Omega$ .

**Shrunk.** The individual cell area is less than in the 6147. Because the cell is connected to the power supply through a buried J-FET designed not to exhibit FET-like characteristics, Hitachi engineers were able to shrink it to 28 by 32  $\mu\text{m}$  (1.1 by 1.26 mils), for a reasonable chip size of 4.66 by 5.5 millimeters (187.4 by 216.5 mils). In contrast, the size of the cell in the 6147 is 1,100  $\mu\text{m}^2$ .

The RAM will come in a 24-pin package compatible with popular programmable read-only memories and operate from a single 5-volt power supply with TTL-compatible input/output levels. Prototype devices have a 55-ns access time and a 55-ns read cycle time, but commercial devices, samples of which will be available toward the end of the year will be offered with guaranteed access times of 100 or 150 ns.

The typical operating current will

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 CLIMATIC CATEGORY : - 55°C/+ 175°C/56 days

**CONFORM TO MIL-R-55182/9**

**RCK 02/RCK 02 A**

Dimensions  
 8 x 7.5 x 2.5 mm  
 0.33 W at 125°C  
 2.5  $\Omega$  to 150 k $\Omega$

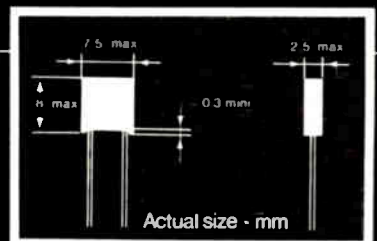
**RCK 04**

Dimensions  
 10.5 x 15 x 3.5 mm  
 0.6 W at 125°C  
 5  $\Omega$  to 300 k $\Omega$

**RCK 05**

Dimensions  
 10.5 x 22.6 x 3.5 mm  
 0.9 W at 125°C  
 7.5  $\Omega$  to 450 k $\Omega$

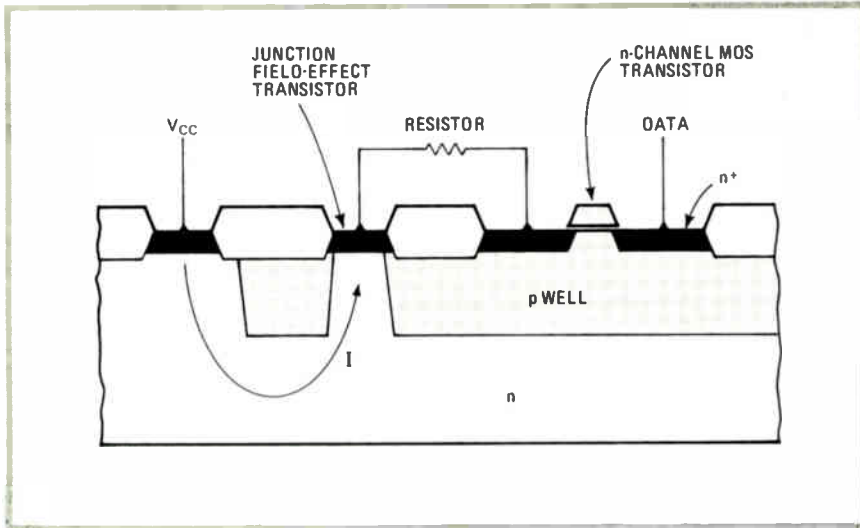
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**Smaller.** For its low-power 16-K static RAM, Hitachi has cut the size of the n-MOS cell by adding a J-FET that supplies power without the need for interconnections.

be 40 milliamperes; and the maximum, 80 mA. The standby power dissipation will be 100 microwatts typically and 4 milliwatts maximum.

Data retention will be guaranteed down to 2 V, at which the typical current is 4  $\mu$ A and the maximum is 100  $\mu$ A.   
 -Charles Cohen

## New approach to MNOS cell looks good for dense nonvolatile RAMs

Dynamic-injection metal-nitride-oxide-semiconductor memory cells have been devised that offer another approach to that elusive ideal: the nonvolatile semiconductor RAM. Though the resulting devices would not be true nonvolatile random-access memories—they are actually RAMs backed up by electrically erasable programmable read-only memories—they should be able to provide the performance desired. Thus these new devices, being developed by Hitachi Ltd.'s Central Research Laboratory, will probably take their place in the hierarchy of nonvolatile memories whose contents can be changed with decreasing ease: EE-PROMs, fuse-link PROMs, and mask-programmable ROMs.

The devices were discussed at the recent International Conference on Solid State Devices in Tokyo [*Electronics*, Aug. 30, p. 85]. They will join other MNOS-backup types from Toshiba Corp. that use a more orthodox approach to achieve similar performance [*Electronics*, Aug. 16,

1979, p. 68; Sept. 16, 1976, p. 40].

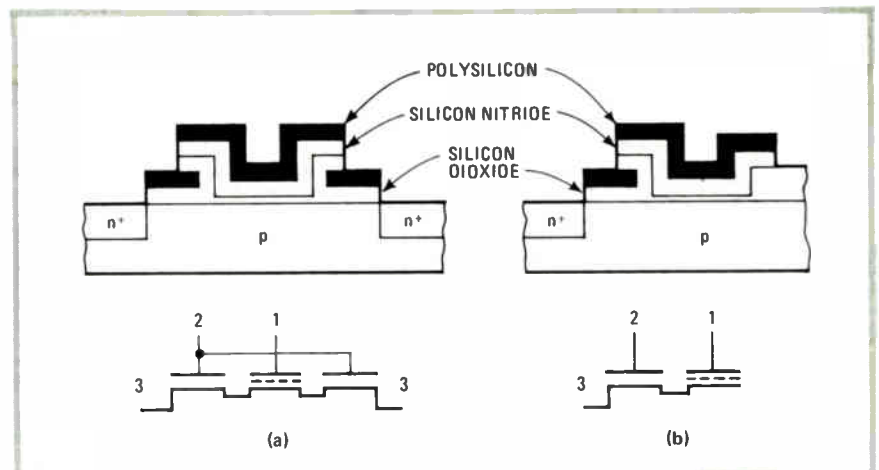
**Different.** The devices operate as ordinary read/write RAMs from a single 5-volt supply but require a 25-V supply for MNOS writing. They use an n-channel MOS silicon-gate configuration rather than the p-channel MOS aluminum-gate configuration commonly used for MNOS.

But a more important difference is that electrons are injected into the nitride layer from a portion of the channel that can be inhibited. In previous devices, majority carriers have always been available in the channel from an adjacent highly doped drain.

Dynamic injection is achieved by connecting one of two n-MOS transistors in series with the memory transistor and using their gates for control. A three-gate MNOS tetrode for static memories and a dual-gate MNOS device for dynamic memories are fabricated as merged structures only slightly larger than a single transistor (see figure).

**Promise.** Because the operation of the three-gate device is better understood, it is being used for development. But the dual-gate MNOS configuration offers greater promise because it would make possible a dynamic RAM with a cell area of only 400 square micrometers (0.62 square mil).

The dynamic injection scheme permits the words of the memory to be written in parallel for a total writing time that is almost the same as that for one word—about 1 millisecond. The gates of the series transistors that turn on the channel of the MNOS transistor must be on only for about 50 nanoseconds to initiate the writing. Even after these gates are turned off, electrons cannot escape and writing continues as long as the writing voltage is applied to the gate



**Twosome.** Hitachi is using three-gate MNOS tetrode (a) to develop nonvolatile RAMs, but dual-gate MNOS transistor (b) is more promising. The two form merged structure.



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\*suggested retail price

of the memory transistors.

The writing cycle is started by lowering all terminals to 0 v. Then the gates of all the MNOS transistors are raised to 25 v and held at that level until after the writing cycle is completed. The gates of the series transistors of all the cells of one word to be written in are raised to 5 v for about 50 ns and then returned to 0 v. To write the entire memory in parallel, the process is repeated by raising the gates of the series transistors of the next word to 5 v for 50 ns, then lowering them to 0 v, and then repeating the procedure for the other words in turn. After the last word is written, the writing voltage is kept on for 1 ms and then reduced to 0 v.

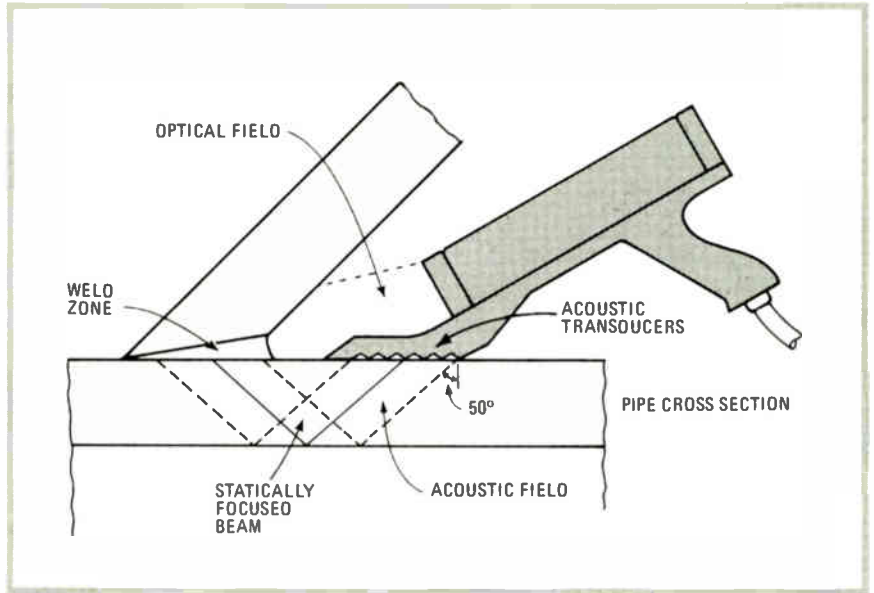
The dynamic MNOS cell operates as a standard dynamic memory when the MNOS transistor is erased. During writing, the contents of each word must be stored in peripheral circuits, but the sense amplifiers can be used for that purpose. -C. C.

France

3-d ultrasonics spots underwater flaws

A French research and development company specializing in underwater oil pipeline and drilling platform work in the North Sea is adding a new dimension to the art of flaw detection by developing an underwater imaging system that uses coherent ultrasonic waves to create three-dimensional sonic images. Faults in pipelines or platform welds show up as light spots on light-emitting-diode and cathode-ray-tube displays.

The system was developed jointly by InterSub Développement SA, a subsidiary of Marseilles-based Inter-Sub SA, and HoloSonics Inc. of San Jose, Calif. "Right now, we only have a prototype, but we are likely to put the equipment into field operation some time next year," explains Yves Durand, general manager of InterSub Développement in the Paris suburb of Rungis.



**Spotter.** Ultrasonic imaging system operates like phased-array sonar to detect weld flaws underwater. Reflection of waves at 50° angle allows inspection of inaccessible joints.

The system, whose prime function is to inspect welds on drilling platforms, amounts to a kind of phased-array sonar. A physically flexible matrix of 160 acoustic transducers at the end of a hand-held gun is fixed to a section of the platform adjacent to the weld. Arranged in five rows of 32 elements, the piezoceramic transducers emit coherent bursts of 2-megahertz waves.

Upon entry into metal, these waves are transformed into shear waves, in which vibrations occur perpendicular to the propagation direction. These do not propagate in liquids and are strongly reflected by interfaces between a liquid and a solid. Therefore they reflect off the other side of the metal section (see diagram). Thus waves emitted at a 50° angle allow inspection of physically inaccessible welds.

**Three ways.** Three different methods provide the three dimensions of the image. One is the acoustical equivalent of phased arrays used in radars. By programming the phasing of the coherent wave bursts, the device can operate in 32 different focal planes.

Another depends on the duration of each burst. The longer the waves are transmitted, the deeper they reach into the material. Finally, the transducers, which operate in groups

of 12, themselves are focused, much as light is focused through a lens, to create a third focal plane.

With 32 elements in each of the five rows of transducers, each focal plane consists of 160 image points. Since phase programming permits 32 different planes, the total number of image points comes to 5,120. "It is very much like a side-scanning sonar, but more precise," says Inter-Sub Développement's technical director, Alain G. Stankoff.

When the system is receiving, the data from each group of 12 transducers is preamplified and demodulated through comparison with 12 reference signals. It is then stored as 4-bit words in 5 kilobytes of semiconductor random-access memory. Next, it is displayed both on a matrix of LEDs and on a CRT and recorded on magnetic tape.

The LED matrix, located directly on the gun, enables the diver to monitor the results of his inspection immediately. The CRT display and magnetic recording apparatus are located inside the submarine to which the diver is linked.

For the prototype, the program is stored in programmable read-only memory, but Stankoff says microprocessors will be used once the firm begins producing the devices for its submarines. -Kenneth Dreyfack





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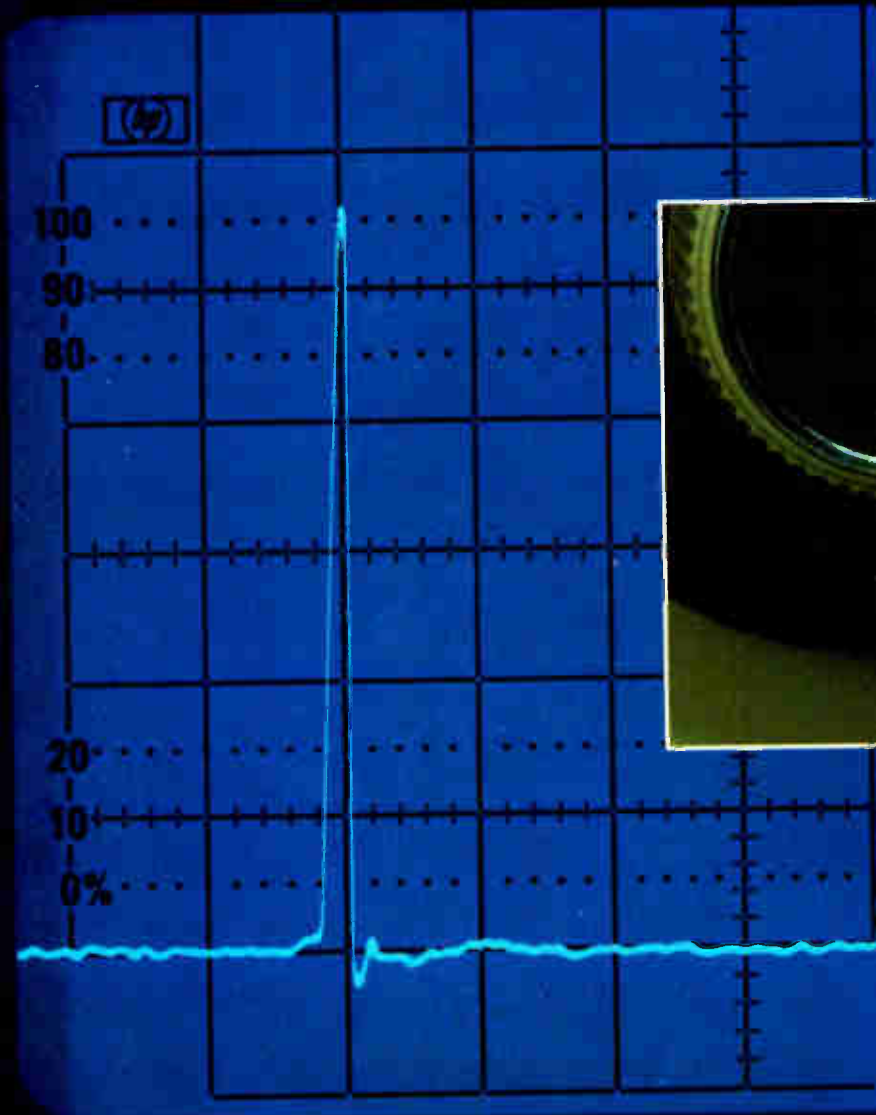
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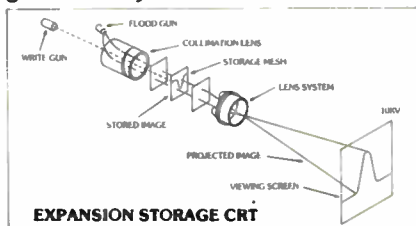
Storage trace as seen using a viewing hood

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**Catch that glitch.** Expansion Storage technology combines a small storage mesh (about the size of a postage stamp)

and an expansion lens system. This exclusive arrangement permits a writing speed of 1800 cm/ $\mu$ s and a fine spot size, which lets the 1744A write faster and further than any other 100 MHz storage scope. That gives you full-scan glitch capture capability over a broad range of sweep speeds and repetition rates.

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Rounding out the 1744A's capabilities are these convenient measurement features: **Easy-IC Probes** to improve closely spaced probe connections and eliminate shorting hazards; a selectable input impedance (1 megohm/50 ohm) for general purpose probing or 50 ohm matching; and measurement sensitivity as low as 1 mv/div to 30 MHz on both channels without cascading. Priced at \$5250\*, the 1744A furnishes the state-of-the-art technology and performance needed today in digital design and troubleshooting applications.

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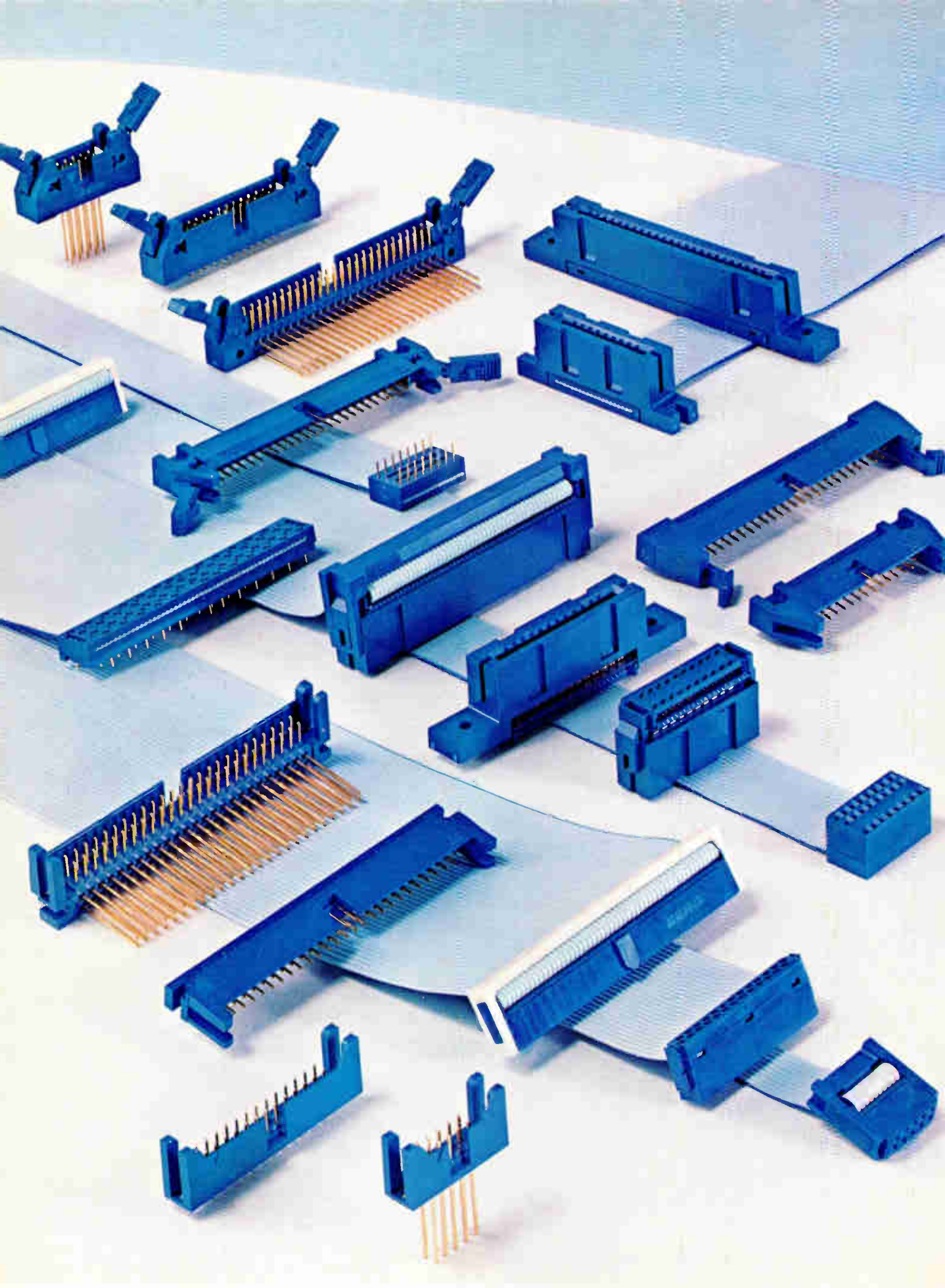
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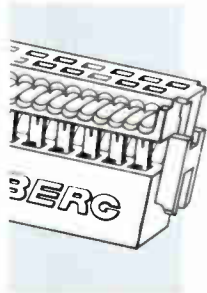
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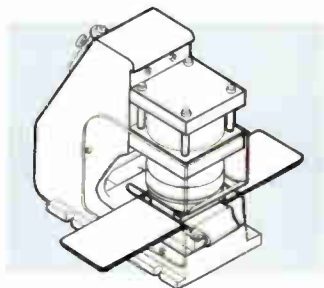
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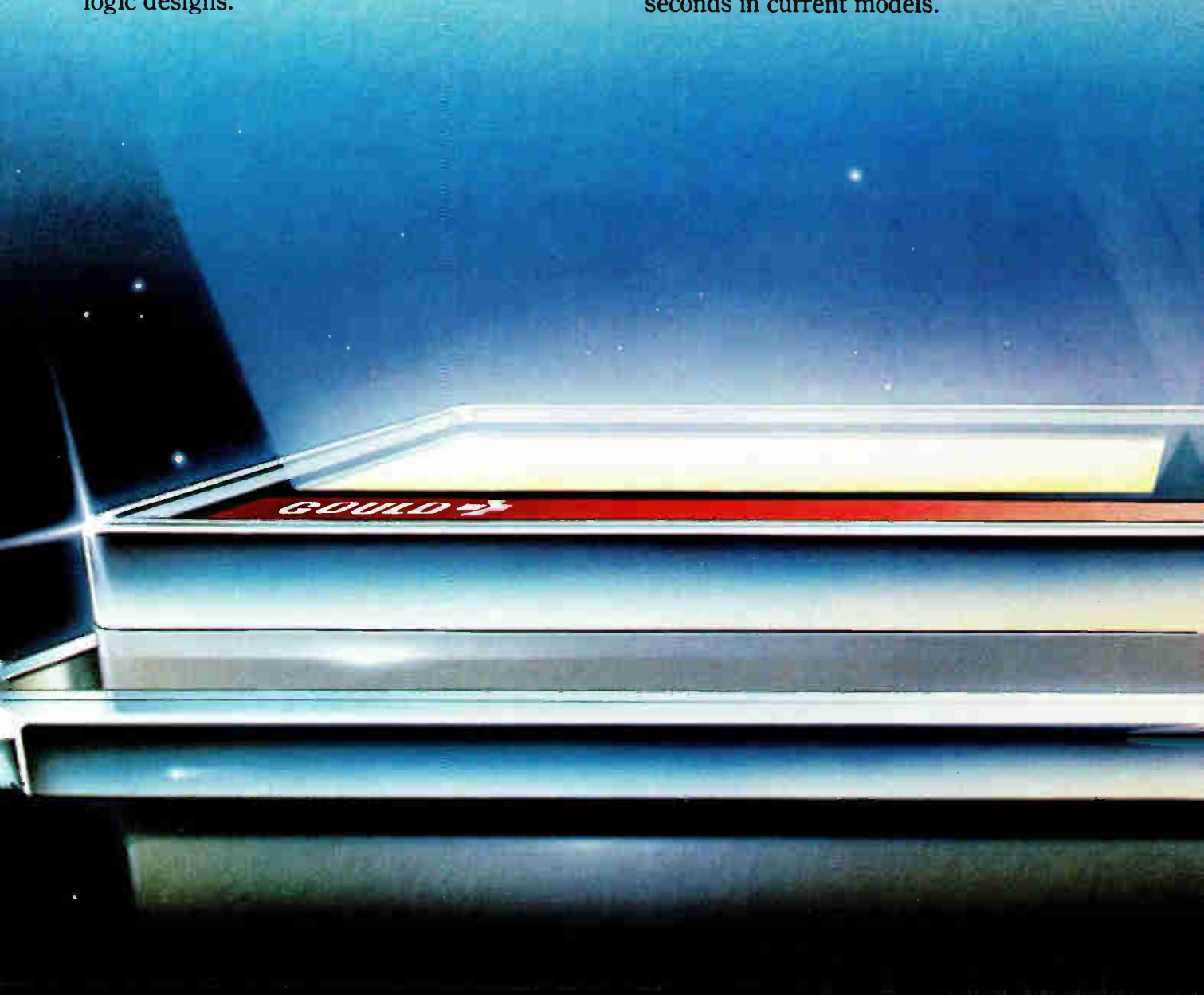
The new demands of digital logic are what Bill Moore, Biotation's first chief engineer, had in mind when he developed the logic analyzer, back in '73. He called it a "glitch fixer," designed to track and unravel the mysterious electronic glitches that plague digital logic designs.

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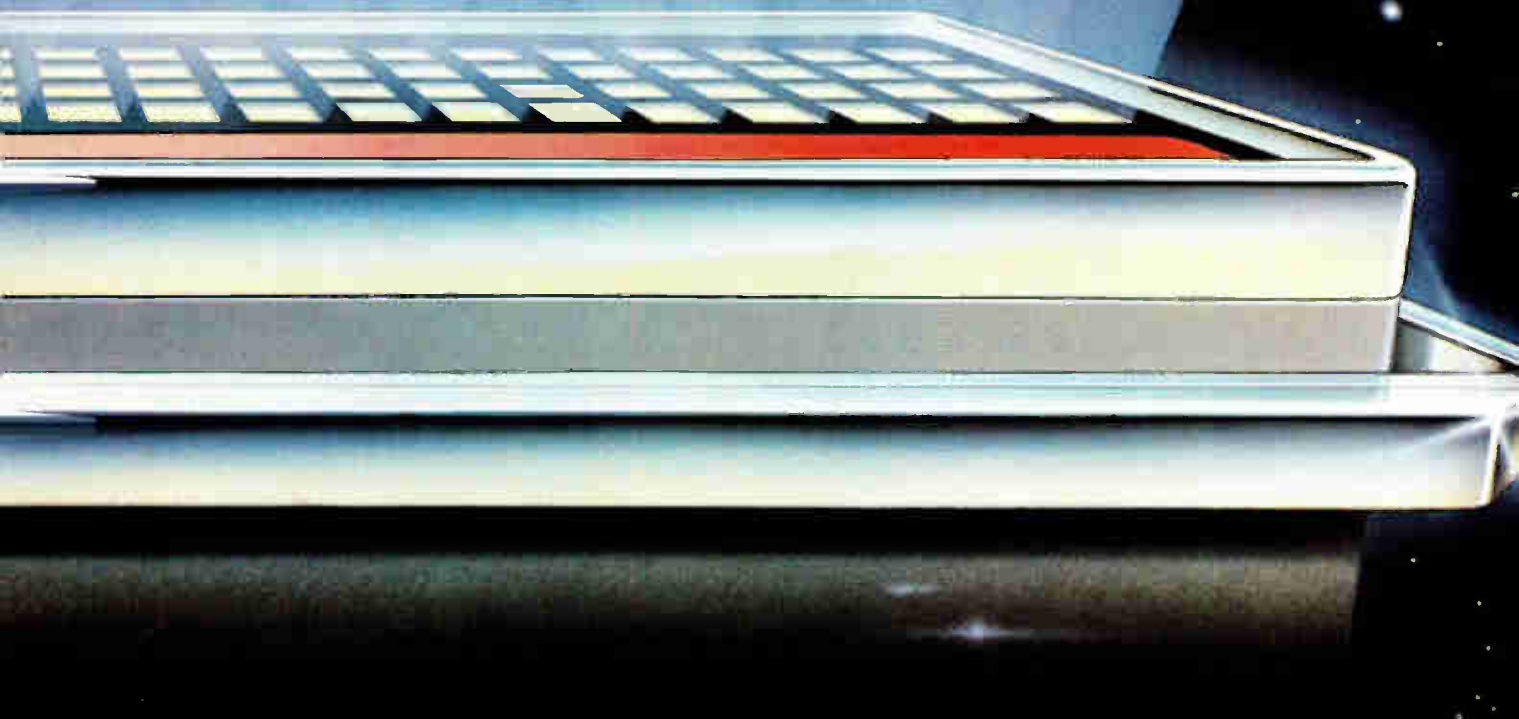
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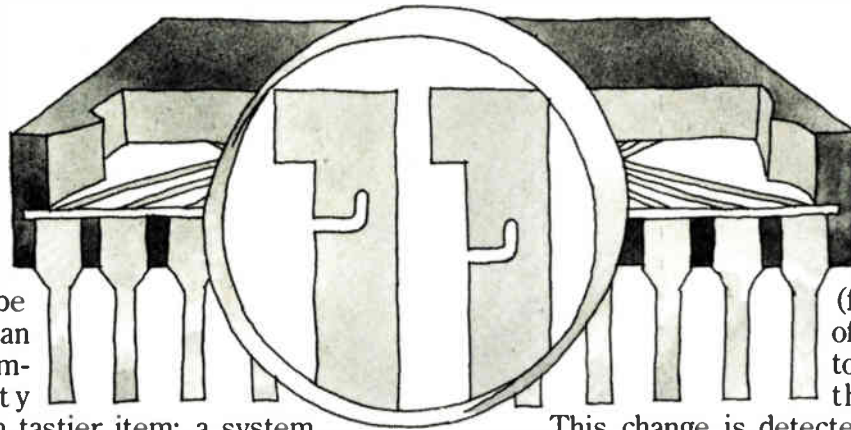
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Circle #87 for information



# Laser trimming of monolithic circuits

Silicon valleys



No sooner have we swallowed the fact that 86,000 thick-film resistors can be laser-trimmed in an hour than the trimming fraternity serves up an even tastier item: a system capable of trimming monolithic circuits with a laser beam only 6 micrometers in diameter.

Now, to put a spot size of 6 micrometers into focus (so to speak), the new trim system can very easily write your name inside the period at the end of this sentence, with room left over for a troupe of dancing angels.

Producing a spot this small is basically an optical feat, accomplished by lensmanship of the highest order. To be useful in monolithic trimming, however, beam reduction must be accompanied by equally remarkable positioning accuracy, there being no known application for a wandering 6-micrometer laser kerf.

Teradyne's closed-loop galvanometer beam positioner, used for some time on the W411 Laser Trim System, had already wiped out hysteresis and greatly reduced nonlinearity. That left geometry errors in the step-and-repeat table and registration errors from die to die as the principal error sources to be dealt with.

The solution to these problems is a new technique for nondestructive edge sensing, called "Laser Eye." Before the laser beam starts trimming, it is attenuated and brought to the leading edge of the circuit. When it encounters the circuit edge, there is

an abrupt change in the amount of laser energy reflected (from high reflection off the light substrate to low reflection off the dark circuit).

This change is detected by a photodiode, and the exact position is passed along to the computer, which adjusts the stored trim coordinates and the focus of the laser beam accordingly. The edge-sensing is typically repeated on every die to ensure positioning accuracy, with focus adjusted every inch or so to compensate for any wafer warp.

As further insurance against positioning errors, the entire mechanism is shock-mounted against the effects of vibration. The trim system is, after all, designed not as a laboratory instrument but as a machine to grind out parts on a factory floor.

The combination of closed-loop galvanometer positioning, Laser Eye, and solid systems engineering yields a bottom-line, no-strings positioning accuracy of 2.5 micrometers. That means that, on any given circuit, the laser beam will be within 2.5 micrometers of where it's supposed to be, period.

Monolithic trimming is currently of principal interest to makers of monolithic 12-bit D to A converters. But now that lasers have broken the IC, who knows what uses may be found for 6-micrometer holes, coming thousands per second, right on the money every time?

*The first 12 essays in this series are now available in booklet form. For your copy, write to Teradyne, Department E, 183 Essex Street, Boston, MA 02111.*

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## Smaller boards mean bigger problems

Annual Cherry Hill test conference next month will continue yearly debate over built-in testability as VLSI casts its shadow

by Richard W. Comerford, Test, Measurement & Control Editor

The gains in board-testing ease that have been won since the last Annual Test Conference at Cherry Hill, N. J., are being threatened by advances in integration technology. In fact, many industry observers are worried that unless solutions to testing problems can be discussed and agreed upon now, the upcoming very large-scale integrated circuits will be untestable.

Perhaps one measure of the test community's concern is the increase in preregistrants for the three-day conference that begins on Tuesday, Oct. 23. Not only are those figures 20% more than last year's, but the number of exhibitors—who come not only to display their wares but also to learn firsthand the problems of users and to see what their competitors are up to—has risen from last year's 21 to 32. According to a spokesman for the show's sponsors, the Institute of Electrical and

Electronics Engineers' Philadelphia Section and its Computer Society Test Technology Committee, 1979 is "the first year we have had to turn away exhibitors for lack of space."

Among the people they will listen to, Tom Williams, manager of LSI design rules control for International Business Machines Corp., has already encountered the problems that increasing integration can cause. "The people who are using the components are literally suffering, having difficulty at the card level," he says. As chairman of the IEEE subcommittee on design for testability that has for the last two years held workshops in Boulder, Colo., Williams will also lead the first technical session, which is devoted to just that topic. He, like others, feels that independent IC manufacturers must build testability into their parts.

In places like IBM, Bell Laboratories, and Nippon Electric Co., cap-

itive IC facilities are already generating logic that conforms to their testability criteria. Thus, when they get to the board and subsequent levels of packaging, they are able to preserve testability. "The problem for the small original-equipment maker and the horizontally integrated company is that he must buy his parts from some IC house," Williams points out, and those houses have not been economically motivated, as they must be, to put in some testability attributes."

Michael Chalkley, vice president and general manager of Fairchild Camera and Instrument Co.'s Xicom Systems division in Chatsworth, Calif., agrees on motivation. "The IC houses," he says, "are only going to build in testability when there is an economic threat large enough to force them to do that. Large main-frame companies are slowly but surely pushing their heretofore cap-

CHERRY HILL AT A GLANCE

	Tuesday, Oct. 23	Wednesday, Oct. 24	Thursday, Oct. 25
MORNING	<b>SESSION</b> <b>1</b> 9:30-11:30 Keynote address and invited papers  The ATE industry: a historical perspective — A. d'Arbelloff, Teradyne Inc.	<b>SESSION</b> <b>6</b> 8:30-11:30 Self-test at board and system <b>7</b> 8:30-11:30 Computer-aided analog test design <b>8</b> 8:30-11:30 Memory testing	<b>SESSION</b> <b>13</b> 8:30-11:30 Component microprocessor testing <b>14</b> 8:30-11:30 Design for testability at component level <b>15</b> 8:30-11:30 Production board testing
	<b>2</b> 1:30-5:15 Design for testability <b>3</b> 1:30-5:15 Bubble memory testing <b>4</b> 2:30-5:15 Test equipment correlation workshop	<b>9</b> 1:30-5:30 Computer-aided test pattern generation <b>10</b> 1:30-5:15 Complex analog LSI testing <b>11</b> 2:30-5:15 Test economics	<b>16</b> 1:30-5:30 Board microprocessor testing <b>17</b> 1:30-5:15 High-speed testing
	<b>5</b> 8:00- Digital test problem	<b>12</b> 8:00- Analog test problems	
AFTERNOON			
EVENING			

## Probing the news

tive assembly outside, so I think you are going to find intense competition to meet these companies' requirements, if for no other reason than that they provide a good measure of economic stability." Such stability may prove to be the driving economic factor in the 1980s.

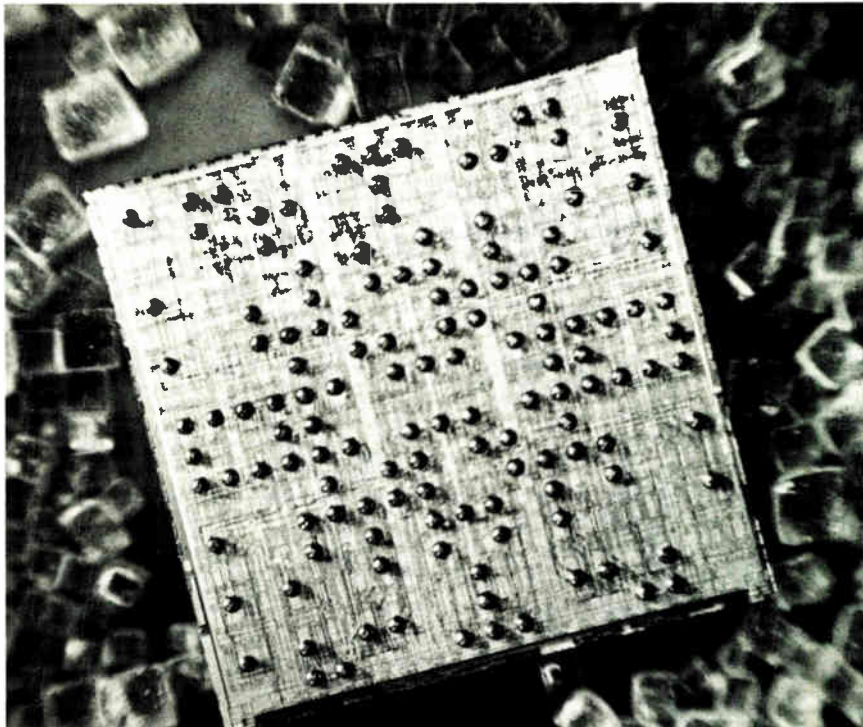
While chip makers are scrambling for real estate, the techniques that can provide testability at the chip level—level-sensitive scan, scan-set, and scan-path design, among others—can take up from 4% to over 40% of the available chip space. All these techniques reduce sequential problems to combinational ones by putting shift registers onto the chip to permit access to otherwise unreachable nodes.

**From IBM.** Level-sensitive scan design [*Electronics*, March 15, p. 108] was developed by IBM and is used in its self-testing System/38. The dual-clock technique requires from 4% to 20% of a chip's space and requires that the system clock be stopped so that readings can be taken. Similar to the LSSD technique is the scan-path technique developed by Nippon Electric. Though functionally equivalent, it allows designers to employ a larger, "richer" set of hazard-free, polarity-hold latches, such as D triggers and set-reset latches.

The scan-set design developed by Sperry Univac differs from both the other approaches in that the shift registers are outside the data-flow path. With this design, it is possible to sample data while the chip is functioning, without stopping operation. But designers must give up sizeable real estate—40% or more.

While much attention will be given to the coming technologies at Cherry Hill, the conference will not ignore the problems that users and designers are experiencing now. The evening sessions on Tuesday and Wednesday, for instance, will be given over solely to present digital and analog test problems, respectively, and other daytime sessions will focus on current problems.

**Scarce parts.** Another session that will tackle an important current problem, that of testing semiconduc-



**Way to go.** IBM uses these logic chips, with built-in testability, in its new System/38. They are 4.6 millimeters square and house a maximum of 704 TTL circuits.

tor memories, will be held on Wednesday morning. The shortage of parts in this area has been cause for concern among many manufacturers. Engineers from one company, NCR Corp., will present a paper on an approach to parallel testing for the 16-K random-access memory. Co-author of the paper, Larry Calhoun, manager of test equipment engineering for NCR's West Columbia, S. C., facility, says "We're looking at the problem as a buyer of parts rather than as a manufacturer, so we have a different framework."

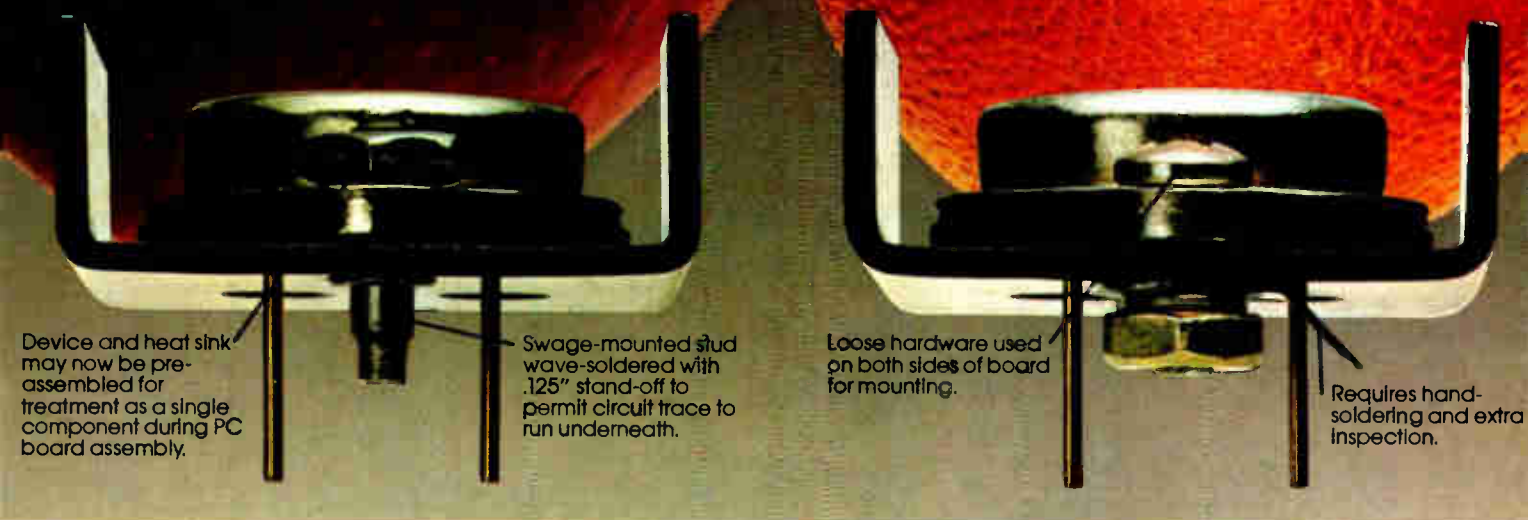
That framework consists of adopting the philosophy that incoming parts have been well characterized for dc parameters by their manufacturers. "What we do is very extensive pattern testing. For example, they cannot do a Galpat [galloping pattern] test on an outgoing basis but on an incoming basis, testing to our specific needs, we can. A vendor would have to get much more information to bin out such parts, whereas we just need a go/no-go answer." A fully implemented system developed by the company can presently test up to 256 16-K RAMs (two system loads) per hour, but the testing does not ensure the accuracy of dc parameters. This information can

be obtained, however, by sample tests on a lot.

One of the lessons already learned from semiconductor memory testing has resulted in scheduling a session on bubble memory tests, according to Steve Bisset, president of Megatest Corp. in Santa Clara, Calif. "When RAMs first started to appear," he says, "people weren't aware of the importance of the various failure modes that could occur." So that this does not create problems for future designs using magnetic-bubble storage devices, the Monday afternoon session will disclose typical performance parameters for the parts, which are just starting to move into full production."

Even the last session will undoubtedly draw much attention. Here, representatives of Nippon Telegraph and Telephone Public Corp. and Takeda Rikon will continue their tradition of unveiling trend-setting systems [*Electronics*, Nov. 23, 1978, p. 48]. But their 100-megahertz general-purpose digital test system, with 384 test pins, will not be alone in astounding those present, and the entire conference promises to live up to its reputation for animated and controversial discourse, not to mention some argument.

# It's an unfair comparison. But let's do it anyway.



Device and heat sink may now be pre-assembled for treatment as a single component during PC board assembly.

Swage-mounted stud wave-soldered with .125" stand-off to permit circuit trace to run underneath.

Loose hardware used on both sides of board for mounting.

Requires hand-soldering and extra inspection.

## Thermalloy's new solderable heat sinks cut assembly steps in half.

When you compare conventional heat sinks with the new Thermalloy Timesaver Solderable models, you'll see just how unfair that comparison is. With the Timesavers, you can now pre-assemble the transistor and heat sink, drop in the plated-through hole and treat it as a single component for production. All work is done on one side of the PC board. Then, it's wave-

soldered with the rest of the board. Makes three steps take the place of six.

Available "off the shelf" in Model 6108 for TO-3 cases and in Models 6109 and 6110 for plastic power cases. This patented technology is being adapted to other case styles and heat sink shapes.



### New Timesaver Method

1. Board components, including heat sink/transistor, are pre-assembled.
2. Wave soldered, cleaned and trimmed.
3. Inspected once.



### Conventional Method

1. Board components to be wave soldered are pre-assembled.
2. Wave soldered, cleaned and trimmed.
3. Inspected first time.
4. Heat sink mounted with loose hardware.
5. Hand soldered, cleaned and trimmed.
6. Inspected again.



**Thermalloy, Inc.**

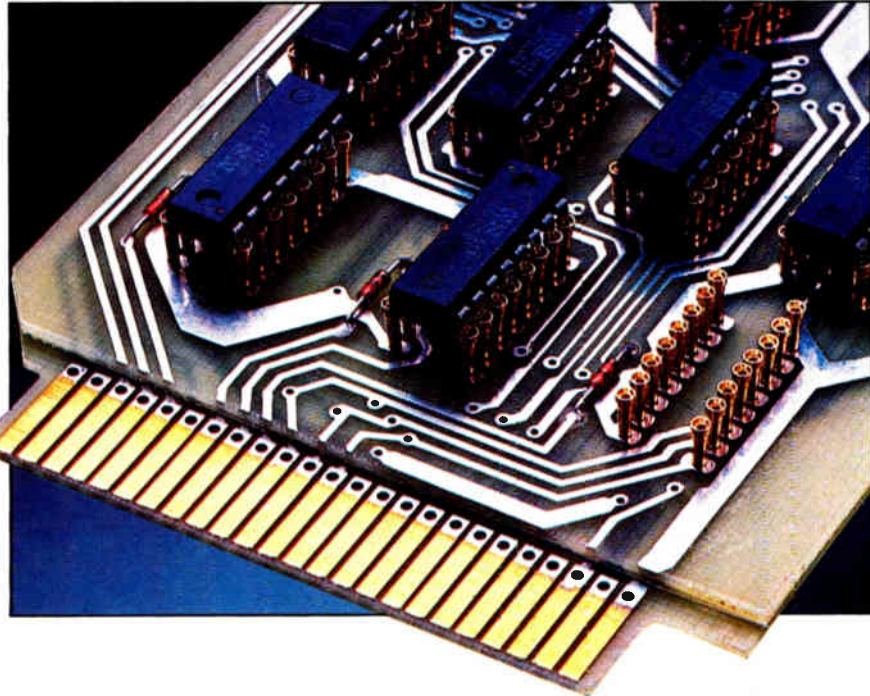
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Circle 91 on reader service card

# Expanding the parameters of press-fit technology



## New press-fit I.C. socket offers lower cost, higher density and cooler operation.

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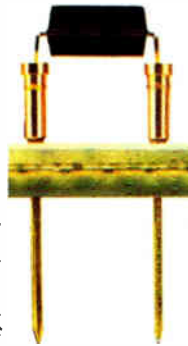
Using a conventional precision screw machine contact, press-fit into the circuit board, this new socket is a major improvement over time-proven packaging methods. This innovative conversion to press-fit techniques greatly increases cost effectiveness by reducing need for external wiring and the elimination of soldering.

Characteristics of the new socket allow us to selectively plate a portion of the tails with significant savings in gold plating.

### High Density—Greater Design Freedom

The new socket stands rather high on the board (.190")—but with good reason.

The .062 pad now allows a trace to be run between contact holes for greater circuit density. This should allow a drop from a 3-wrap tail to a 2-wrap—or no tail at all. The 2-wrap offers about the same spacing as a conventional low profile socket with 3-wrap tail. Used in an Elfab Multi-Pac® system, you can get up to six planes of circuitry on a modular daughter board or backpanel. You eliminate the need for



complex and expensive multilayered boards.

### Cooler Operation

Since the socket stands up off the board, air flow aids in heat dissipation giving you much cooler operating temperatures. This is especially significant with higher pin count IC's.

### Oriented Contact — both clip and contact tail.

Clip is so oriented that the four contact tines are in perfect alignment with the IC lead. Each tail is oriented square and parallel with the others to accept a mating connector when desired.

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Solid State

## Europeans strut their stuff

Solid State Circuits Conference in England shows off impressive array of new developments and products

by Kevin Smith, London bureau manager

Though overshadowed by the United States in integrated circuits, European aspirations still burn bright in new research fields and nonstandard sectors. That's evident from papers presented at the Fifth European Solid State Circuits Conference that convened at Southampton University, England, Sept. 18-21.

New products described in more than 50 papers presented by European research organizations were:

- A bipolar operational amplifier that uses a 1.1-volt power supply and dissipates 300 microwatts in its standby mode.
- A high-gain MOS amplifier circuit for use in sampled-data systems.
- A bus-oriented self-checking IC that offers a solution to testing very-large-scale integrated circuits.
- An analog process timer on a single mask-programmable chip.
- A micro-associative processor built with integrated injection logic (I<sup>2</sup>L).
- A single-chip communications microprocessor using complementary-MOS on sapphire.

**Shiny stuff.** New developments described included:

- A double ion-implanted n-channel MOS process with a high (100-v) breakdown voltage.
- A new stacked I<sup>2</sup>L process for high circuit densities.
- A speedy sample-and-hold circuit fabricated in high-mobility gallium arsenide.

U.S. and Japanese companies, though not represented in strength, managed to make their presence felt with several papers, giving Europeans at the meeting benchmarks to aid their perspective. Particularly impressive was a high-density, high-



performance process from Nichiden Toshiba Information Systems, Tokyo, used to fabricate an emitter-coupled-logic 8-by-8-bit multiplier with 700 gates on a single chip. It is intended for mainframe applications. Nine of these chips whiz through a 64-by-64-bit multiplication in 100 nanoseconds. The process uses three-layer metalization, polycrystalline resistor structures, and self-aligning base and collector regions that are also fabricated in polycrystalline silicon.

Apart from these innovations, the major trend to emerge from the conference was the growing interest in uncommitted-logic-array technology as an inexpensive method of exploiting the advantage of VLSI in semicustom designs. At this month's Wescon conference in San Francisco, an entire session was devoted to the subject; at Southampton, several papers pointed up the growing power and flexibility of the technology (see "ULA stands for versatility," p. 94).

**Self-testing.** Two papers, one from France and another from West Germany, addressed the problem of self-testing ICs. With increasingly complex circuits, the authors believe, self-checking will be needed both to simplify testing during manufacture and later in the field if high-reliability fault-tolerant computer and other control systems are to be developed (for the view from the U.S., see "Smaller boards mean bigger problems," p. 89).

One elegant solution, proposed by B. Könemann, J. Mucha, and Z. Zwiehoff of the Technical University of Aachen, West Germany, exploits the modular and highly bus-oriented structure of many VLSI systems.

## Probing the news

These buses are interfaced by on-chip latches that, with only a slight increase in circuit overhead, can be used to test the circuit. One latch, for example, can be used as a pseudorandom sequence generator by configuring it as a shift register with gated feedback. The circuit response to test patterns generated by this circuit can be checked by a signature-analysis technique using existing latches modified to produce a linear-feedback shift register.

The resulting signature is evaluated either by an exclusive OR comparison with a nominal signature stored on the chip or by scanning it at a primary output pin. The technique permits simultaneous testing of several chips on a wafer at internal speeds and testing in the field.

Interest in n-MOS technology for analog processing is growing in Europe, too. A paper from P. U. Calzolari and S. Graffi of the Istituto di Elettronica of the University of Bologna describes a novel single-channel MOS amplifier that overcomes the inherently low gains of conventional MOS amplifiers to achieve high voltage gain, low power consumption, and small chip area. The device is intended for sampled-data applications and uses the inher-

ent sampling action to switch an interstage capacitor.

Also from Aachen's Technical University was a paper on a low-voltage operational-amplifier circuit that can operate from 1.1 v and has a standby power dissipation of 300 microwatts. The circuit, which has a unity-gain frequency of 1.5 megahertz and a low-frequency gain of 67 decibels, can be fabricated with any bipolar process.

**One more.** Work at West Germany's Siemens AG has resulted in a 5-v n-channel logic circuit with a high-voltage output capability. By the addition of only one extra process stage in the double ion-implanted process, the output breakdown voltage is extended to 100 v.

Looking to the future, England's Plessey Research (Caswell) Ltd. described work toward a high-performance 250-MHz integrated sample-and-hold circuit using high-mobility GaAs base material instead of silicon. With a slew rate of 750 v per microsecond and an on-to-off ratio of 40 dB, Plessey sees the device as having video-processing applications. The current design incorporates the switch, part of the drive circuitry, and a matched pair of field-effect transistors for the front end of the following amplifier.

From the Société pour l'Etude de la Fabrication de Circuits Intégrés

Spéciaux (Efcis), Grenoble, France, was a special-purpose single-chip C-MOS-on-sapphire microcomputer, the MOM 400, which has been optimized for man-machine communications and is specified for applications in instrumentation, remote sensing, and telecommunications. With 1 kilobyte of programmable read-only memory and 256 bits of random-access memory, it can drive up to 16 seven-segment displays, a 256-by-4-bit external RAM, and/or a 64-key keyboard, with pull-up resistors provided on the chip.

One paper from the European facility of a U.S. company, Analog Devices BV of Limerick, Ireland, described a digitally programmed monolithic audio attenuator developed for use in hi-fi systems. It provides up to 88.5 dB of attenuation in 1.5-dB steps plus full muting. A 6-bit binary code determines the degree of attenuation. Incorporated on the 74-by-100-mil C-MOS chip is a digital-to-analog converter with a logic curve and decoding logic.

**For timing.** A multifunction package for use in process timing and other applications was a third entry from the Technical University of Aachen. It incorporates, on a single chip, a mask-programmable logic-array timer, a regulated power supply, and a zero-voltage switch trigger. □

## ULA stands for versatility

All the uncommitted-logic-array approaches described at Southampton use prediffused wafers containing arrays of standard cells on each chip that can be interconnected to a customer's requirement by a one- or two-layer metalization pattern. The approach, say its advocates, combines the economics of large-scale production with the advantages of a custom design.

Two systems houses that have turned to ULA technology to gain a technological leverage in key areas of product development and to speed design turnaround are two British firms: Rascal Microelectronic Systems Ltd. and International Computers Ltd.

Rascal buys prediffused 224- or 448-cell wafers of its own design from Mitel Semiconductors Inc. and completes the final aluminum interconnect patterns. The Mitel Iso-C-MOS process combines very low power with high cell density. With two complementary transistor pairs per cell, chip densities of up to 800 equivalent gates are possible [*Electronics*, May 24, p. 70].

To achieve connection efficiency, Rascal uses a hexagonal cell design, with the cells connected by horizontal and diagonal interconnecting tracks. Power-supply con-

nections are made through the substrate leaving space between cells for the tracks. Six cross-unders are provided.

ICL has developed its own ULA technology to shorten circuit design time and simplify the design of large-scale integrated circuits for computers. Its approach is optimized for high-speed computers and is compatible with 10-K emitter-coupled-logic parts and fast random-access memories. Typical worst-case propagation time through a two-level AND-OR gate is 1.3 nanoseconds.

Even faster ULAs with subnanosecond performance are promised from Plessey Research (Caswell) Ltd. S. Hollock described a 144-cell ULA offering logic densities of up to 400 equivalent gates that has propagation delays of 500 picoseconds per gate and dissipates a total of 3 watts. A second, low-power version, compatible with the first, offers a gate delay of 1.3 ns for a power dissipation of 500 milliwatts. Both chips measure 137 by 160 mils and have 64-pin connections.

Furthermore, an even faster version having a propagation delay of only 200 ps is on the way in which the process is scaled down to 3-micrometer geometries.

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Industrial electronics

## Video disk gets blue-collar role

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Industrial applications will be the first step  
for the technology as IBM's entry provides giant push

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by Anthony Durniak, Computers & Peripherals Editor

"When IBM announced it was getting into the video disk business, the industry was born."

Although others have been pursuing the so-called video disk technology for some time, many in the industry agree with the statement made by Jerome Drexler, a disk maker.

IBM endorsed the concept when it teamed up with MCA Inc., Universal City, Calif., earlier this month to form a joint venture called DiscoVision Associates [*Electronics*, Sept. 13, p. 33]. As those in the video disk and related fields react to the news, it is becoming increasingly clear that the laser-based optical playback technique and its industrial applications will predominate for a while.

Under development for several years, video disk technology is a means of storing video and audio information on a plastic disk resembling a long-playing record. Planned as a means of supplying consumers with special entertainment, like feature movies, the device is perfect for audio-visual training and could be adapted to store such digital information as computer data.

To date the only commercially available video disks are those manufactured by MCA, under the DiscoVision name, which the new associates will distribute. And Magnavox Consumer Electronics Co., the Fort Wayne, Ind., subsidiary of North American Philips Corp., is marketing its \$775 Magnavision player in a limited number of cities only [*Electronics*, Dec. 21, 1978, p. 33].

But DiscoVision Associates is now marketing the PR7820, an industrial version of the disk player manufactured since earlier this year by Universal Pioneer Corp., the Japan-



**Headed for workplace.** This video disk player, made by Universal Pioneer Corp., will be sold for industrial applications by DiscoVision Associates, the IBM-MCA joint venture.

based joint venture of Pioneer Electronics Corp. of Tokyo and MCA Inc. Pioneer says IBM could acquire 25% of the new company.

Based on the same laser and optics technology developed in conjunction with Philips, this player differs from the consumer model primarily because it is controlled by a Fairchild F8 microprocessor with 1,024 bytes of random-access memory. This microprocessor allows random access, according to frame index number, to any of the 54,000 frames stored on an average video disk; the consumer

version can only freeze a frame chosen haphazardly from the program when a button is pushed. The player has a remote hand-held numeric keypad with which the user can run the unit, enter the frame index number, or program the microprocessor. There also is a port that lets the player be hooked to a computer.

**Teaching tool.** The microprocessor-based player is especially useful in educational applications because it can step a user through audio-visual information according to the program in memory. Multiple-choice



questions can be asked, and depending on the answer put on the keypad, the microprocessor can advance the audio-visual information on a correct answer or can branch on a wrong answer either to a specified frame to review the same material or to a different portion for a more intensive tutorial.

A vanguard user of the DiscoVision player is General Motors Corp., which will have some 8,500 of them installed at its Canadian and American dealers by the end of October. GM is using the player both for sales films of its cars, and, more significantly, to train its sales staffs in the features of the new models. In the next phase, GM is contemplating offering training for mechanics. A DiscoVision spokesman notes that by combining the audio with television quality video, it is possible not only to show how to diagnose and repair a part of the engine, for example, but also to demonstrate what whines or other sounds indicate an engine problem.

**Together.** Jerome Drexler is president of Drexler Technology Corp., a Palo Alto, Calif., maker of photolithography supplies that is now sampling its Drexon line of optical disks for 1980 delivery. He calls this ability to selectively combine digital and audio-visual material a major advantage of video disks.

"Home computers, for example, won't enter the mass market until sophisticated software and large data bases are available. Video disk puts a large data bank into the home," he says.

And since the video disks can be mass-produced with techniques similar to those currently used for records, they are a perfect medium for widespread distribution, he says.

But so far, these are the only two units on the market. Apparently not wishing to seem pushed to react to the IBM-MCA announcement, RCA Corp., the only other announced competitor, declined to have its technical people talk with the press. Rather, it restricted itself to the bland statement that it "is proceeding at the fastest pace possible to achieve market introduction" of its Selectavision VideoDisk [*Electronics*, Feb. 2, 1978, p. 44]. Marketing plans for the system, which uses a

contact capacitive pickup instead of the laser-based optical method, are still to be announced in the fourth quarter of the year, as RCA president Edgar H. Griffiths had stated previously. Direction of the video disk program has since last January been in the hands of Jay J. Brandinger in the Consumer Electronics division in Indianapolis. Richard W. Sonnenfeldt, who led the technology to the completion of a prototype model has, since June, been executive vice president of operations and technical services for National Broadcasting Co. in New York.

As for RCA's effort to develop a video disk version for industrial applications, "we have nothing new to report at this time," says a spokesman for RCA Advanced Technology Laboratories in Camden, N. J.

Also under development are stylus units at the Victor Co. of Japan (JVC) [*Electronics*, Oct. 26, 1978, p. 67], Matsushita Electric Industrial Corp., and AEG-Telefunken, while France's Thompson-CSF and Japan's Hitachi Ltd. are reported working on laser-based optical video disk sets.

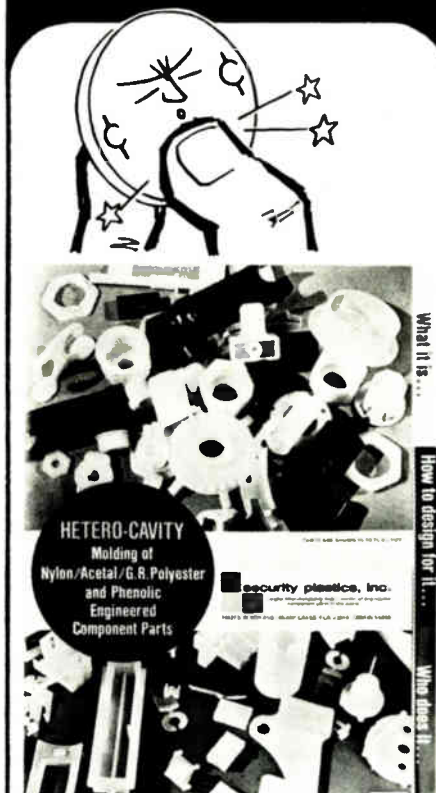
**For storage.** Also of interest, although apparently further down the road, is the storage of digital data on optical disks. Magnavox's Government and Industrial Electronics Co. has developed a prototype that can store  $2 \times 10^{10}$  bits on a dual-sided 12-inch disk.

Engineers at RCA's Advanced Technology Laboratories are also exploring the laser-based optical techniques for digital storage. Though RCA will not discuss details at this time, it predicts disks could make magnetic storage media seem uneconomic by the 1980s. In addition, Hitachi's Central Research Laboratory has recently said it could store as much as 500 megabytes on a 12-inch optical disk [*Electronics*, July 19, p. 68].

Such optical storage will be perfect for archival storage, Drexler says, because the optical media will not fade as does magnetic tape, the currently popular archival medium. He predicts it will cost less, too. "Our Drexon media will cost 10¢ a megabyte where today's high-quality magnetic tape costs about 40¢ a megabyte." □

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Communications

# Germans, French plan TV satellite

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Bird would be in orbit by 1983 to beam television  
and radio shows directly to subscribers' homes

---

by John Gosch, Frankfurt bureau chief

If all goes according to plan, West Germany and France could be the first countries to have operational direct-broadcast television satellites in orbit. To be launched by early 1983, these spacecraft will beam TV and radio signals directly to the home, covering areas too remote to receive program signals from existing links and making more channels available elsewhere.

As things stand now, Volker Hauff, West German minister for research and technology, and André Giraud, French industry minister, will meet in the West German capital of Bonn early next month to discuss a joint TV-SAT project. "We are hopeful our two countries will reach an agreement," says a ministry spokesperson in Bonn. But he cautions that it may take months to work out all the details.

French sources indicate that a basic understanding has already been reached and that Hauff and Girard will simply bless the deal. Officials have been hassling for months over which country will furnish which satellite components. "But we have come to a tentative agreement," says an official of the Centre National d'Etudes Spatiales, the French space agency. Part of the deal is for the satellite to be launched by Ariane I, which is being built by France and several other European countries.

A bilateral accord would be contrary to what looked like a strong possibility only 15 months ago: a multilateral experimental TV satellite project under the wings of the European Space Agency [*Electronics*, May 25, 1978, p. 99]. But meanwhile, the chances for the so-called high-energy satellite (H-SAT) project have dimmed considerably, partly because of the West Germans' objections to putting up an experimental satellite. They favor an operational version right away.

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**Feed from France.** This antenna feed for a direct-broadcast television satellite was designed and built by Thomson-CSF. Franco-German TV-SAT is to be in orbit by 1983.

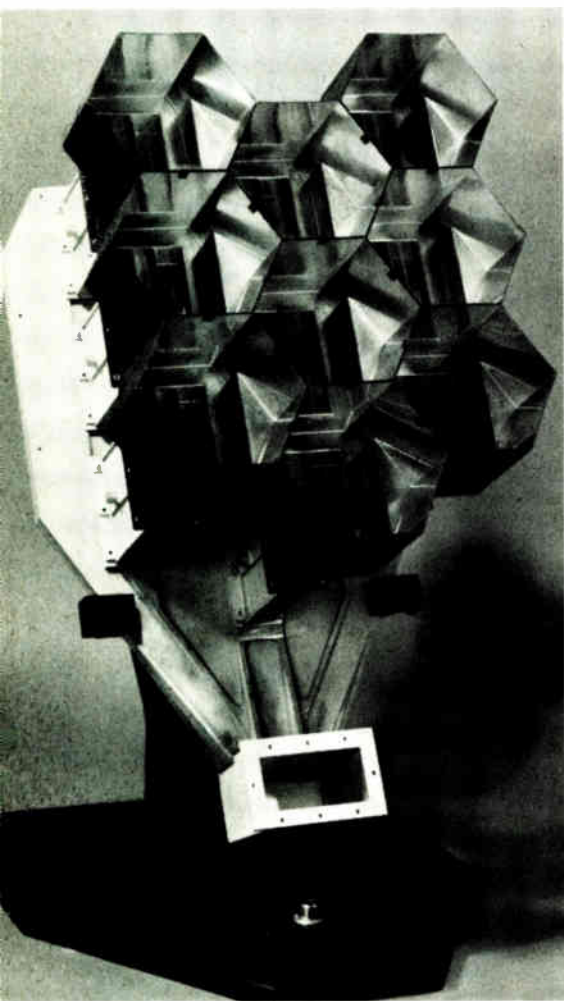
Direct television broadcasting will spawn new communications business in Europe worth hundreds of millions of dollars in the decade ahead. The cost of developing and building the first flight version of a TV satellite can run as high as \$120 million, though its successors cost less, and launch costs vary between \$20 million and \$50 million depending on which launch vehicle is used.

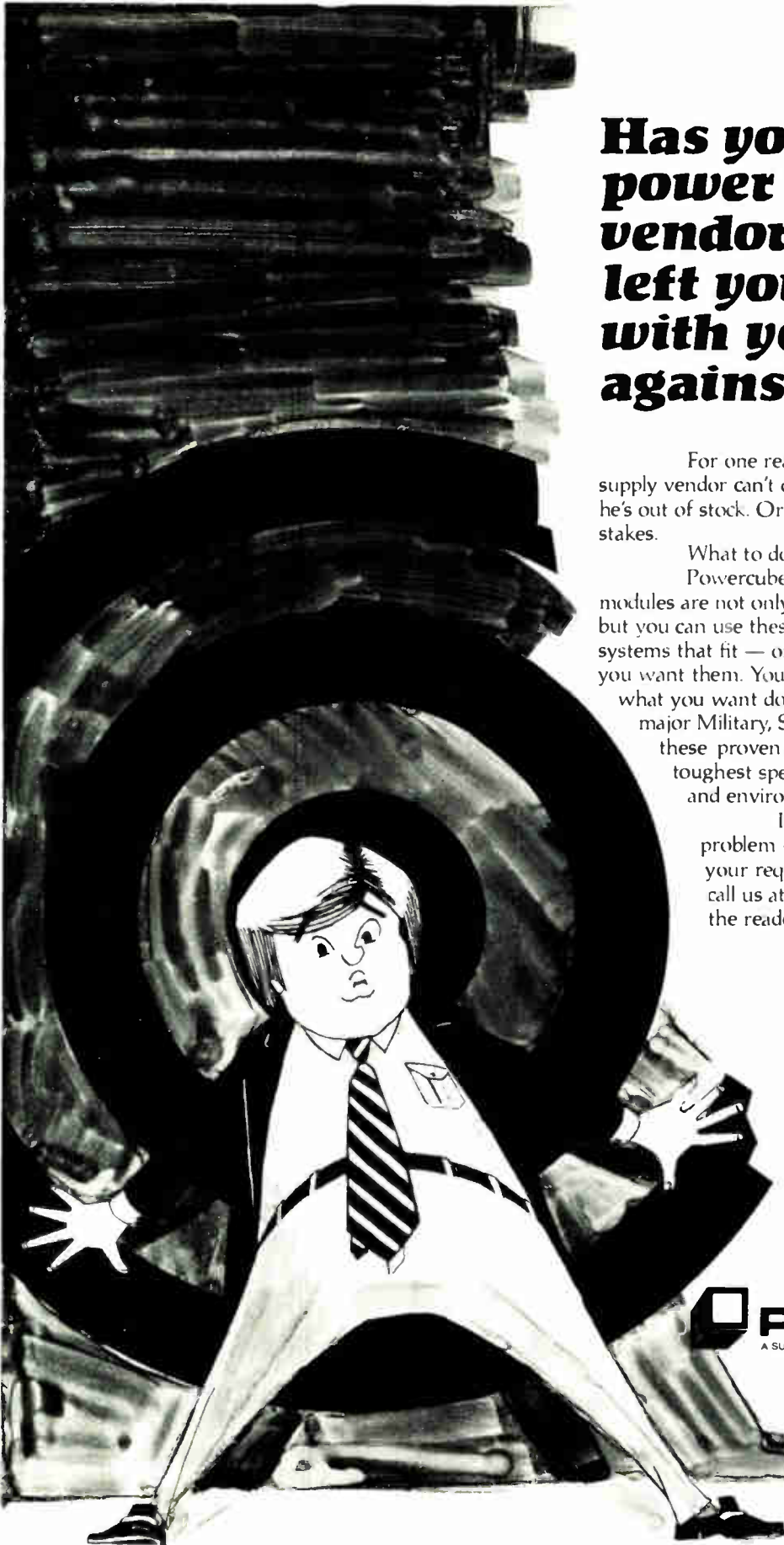
**On the ground.** Electronic gear involves not only on-board systems but also ground-based devices. These are mainly the rooftop-mounted parabolic dish antennas, from 70 to 90 centimeters in diameter. The antenna, plus the converter needed to change the 12-gigahertz satellite frequencies into signals the home TV set can handle, could run between \$250 and \$750, depending on the quantities produced.

Beyond all that are the prospects for the sale of TV satellites and their technology to other countries. For example, West Germany's aerospace firm Messerschmitt-Bölkow-Blohm GmbH has already signed an agreement with the Chinese Academy for Space Engineering that provides for the joint development and construction of a number of TV satellites to cover China [*Electronics*, March 15, p. 72]. MBB is negotiating similar deals with other countries.

If a TV-SAT accord is reached between the German and French, the latter will probably go for the basic satellite concept that Munich-based MBB has worked out. However, to meet individual requirements, the two countries' vehicles will have different maximum transmitting power and other parameters.

**Study tells tale.** The basic TV-SAT





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## Probing the news

concept is described in a \$3 million study prepared for West Germany's Ministry for Research and Technology by an MBB-led consortium consisting of electronic firms AEG-Telefunken and Standard Elektrik Lorenz AG, an ITT subsidiary, and aerospace companies Dornier System GmbH and ERNO Raumfahrt-

technik GmbH. After the go-ahead is given, all four will participate in building the German satellite versions, which are configured for launching either by the French Ariane I rocket or the U.S. space shuttle.

According to Dietrich Koelle, manager of advanced programs at MBB, the German plans call for a two-year preoperational phase, to provide experience in direct TV

broadcasting, culminating by early 1983 in a satellite launch. Parked in a geostationary orbit about 36,000 kilometers above the Equator at 19° west, this first satellite will provide all of West Germany with three channels, one each for the country's two TV networks and the third for broadcasting up to 16 stereo radio programs. An estimated 10,000 receiving stations—either individual rooftop or community antennas—will pick up the programs.

The truly operational phase will be ushered in by a second satellite launched in 1984 in the same orbital position. It will provide five channels, at least one of them intended also for several stereo radio programs. Who will administer these channels has not yet been decided. During this phase, program coverage will be on a broad scale with any number of receiving stations involved and with the preoperational satellite serving as a standby.

**WARC's word.** The channel allocations in the 12-gigahertz band for the West German satellites are those determined at the 1977 World Administrative Radio Conference (WARC) in Geneva [*Electronics*, March 3, 1977, p. 69]. The WARC plan assigns each European country 5 of the 40 channels into which the 11.7-to-12.5-GHz spectrum, is split.

MBB sees its satellites shaping up as a box-type structure divided into three functional modules: the communications module incorporating the repeater and the antenna system, the service module containing spacecraft subsystems, and the propulsion module with electrical-ion thrusters for orbit control that use little fuel. "The modular construction makes for high flexibility, especially in the communication payload," Koelle says. That, in turn, means the same vehicle can be used for different national payloads.

Designed for a lifetime of 10 years in orbit, including a five-year standby period, the operational satellites will have two- and even three-fold redundancy of some critical components like the traveling-wave tubes (TWT), the attitude-control devices, and telemetry circuits. The satellite's antenna system comprises elliptical transmit and receive reflectors measuring 260 by 160 centimeters. □

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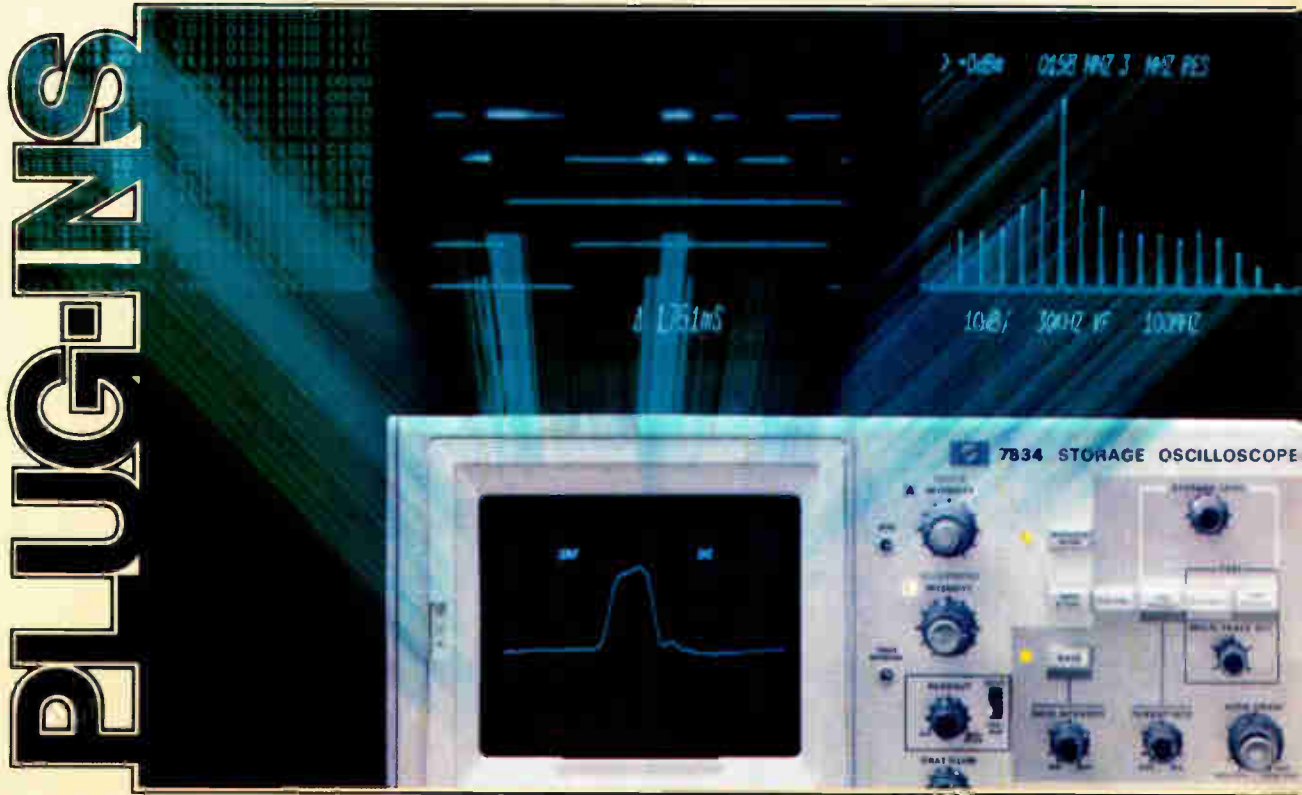
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†HP's implementation of IEEE Standard 488 and the identical ANSI Standard MC1.1.

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Government

## AEA buffeted in Congress

Legislation to ease export licensing watered down in House as electronics executives meet in capital

by Ray Connolly, Washington bureau manager

As American Electronics Association members caucused in mid-September with government officials at the foot of Capitol Hill to exchange ideas on accelerating and simplifying Federal export controls, AEA-supported legislation to resolve some of those concerns was being gutted by amendments on the floor of the House.

"You could say we were smote hip and thigh," said AEA's Kenneth C. O. Hagerty, vice president of government operations, referring to

the floor votes on H. R. 4034. The bill would have revised the Export Administration Act to limit the government's decision time on export applications to between 90 and 150 days, depending on the extent of any agency challenges, and would have required annual reviews to remove unnecessary controls and cut paper work.

But floor amendments by Rep. Richard Ichord (D., Mo.), chairman of the House Armed Services research and development subcom-

mittee, put modification of export controls in limbo for another 12 months until the Pentagon has completed work on identifying critical military technologies to be put on the list of commodities subject to export control. The House action makes moot an earlier 74-to-3 Senate vote in favor of a companion bill, S. 737, sponsored by Adlai Stevenson (D., Ill.) and John Heinz (R., Pa.).

As the House debated the export control legislation, AEA's audience at

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**Top Democrat.** House Majority Leader Jim Wright of Texas addressed the AEA dinner at the group's capital caucus this month.

nology that is now under way should ease the Pentagon's problem in having to evaluate export proposals case by case. Of the 80,000 annual export applications to the Department of Commerce, an estimated 4,000 are referred for evaluation to the DOD, which has only five case officers on the program, Kapper said.

Kapper told the AEA audience that he expects to "work myself out of a job in 18 months," so optimistic is he about successfully developing a DOD policy on technology exportation and a control program based on critical technology lists. The technology exports specialist said the Pentagon has nearly completed evaluation of three of the eight book-length reports prepared by as many industry-staffed Critical Technology Expert Groups. Five more reports have yet to be delivered.

Kapper identified the three areas as very large-scale integrated circuits, microwave components, and structures, materials, and process technologies. He speculated that the final number of critical technologies



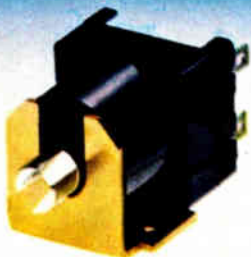
**Tax expert.** Al Ullman, chairman of the House Ways & Means Committee, has proposed a value-added tax.

the nearby Hyatt Regency Hotel heard the Pentagon's director of technology exports, Frank Kapper, sympathize with industry criticisms of extremely long lead times in the Government's processing of applications for export licenses. Kapper said the Defense Department's development of lists of critical military tech-

will probably total 19 after the Pentagon's 13 areas are merged with the list of 12 developed by the Department of Energy. Later, some of Kapper's audience expressed reservations about his optimism, noting that the Defense Department has been struggling for four years to come up with a policy that would

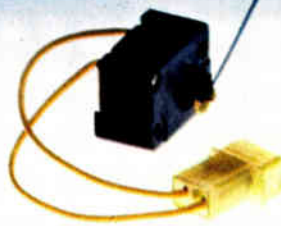
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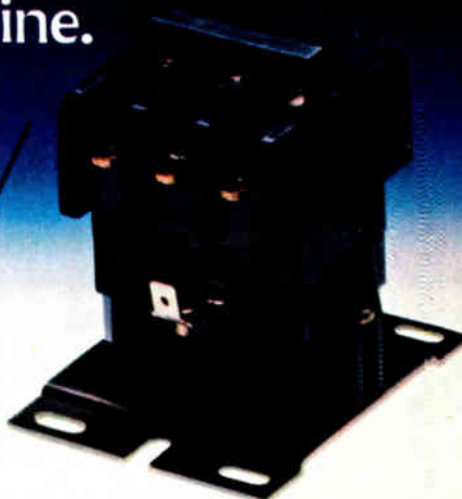
**NEW S85 Solenoid.** General purpose solenoid has an enclosed coil for extra protection. Pull on operate coils available in AC and DC voltages for intermittent or continuous duty. UL Recognized materials, including Class A (105° C) insulation, are used. Use in machine-tool controls, vending and business machines.

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Circle 271



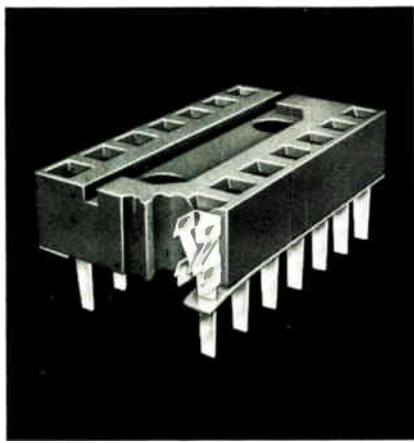
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**NEW SDAS-01 AC Current Sensor.** Zero insertion loss. Field adjustable for overcurrent and undercurrent levels from 1.5 to 15 amps. Solid State sensing circuit is inductively coupled to a high potential power line. Controls internal SPDT, or DPDT relay. Can switch contactors or annunciators. Built-in time delay allows normal start up and line current variations. Control voltage is 24V AC.

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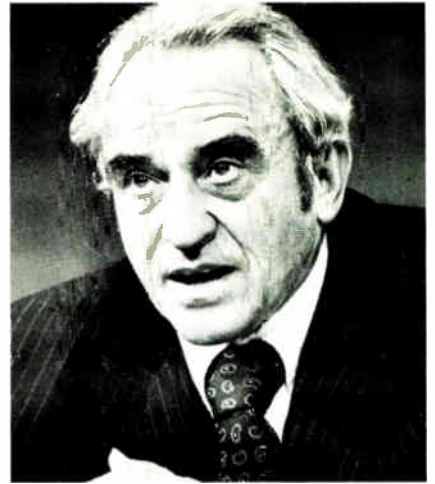
## Probing the news

permit export expansion of technology products while protecting transfer of U. S. production know-how.

**Politicking.** The two-day AEA session was devoted almost completely to political issues. There were lobbying efforts on Capitol Hill by the more than 150 executives in attendance, as well as presentations to the AEA by three congressional leaders and assorted committee staffers seeking industry support for their legislative goals. Key speakers included Sen. Ernest F. Hollings (D., S. C.), chairman of the Senate communications subcommittee and sponsor of the S. 611 rewrite of the 1934 Communications Act; Rep. Al Ullman (D., Ore.), chairman of the House Ways and Means Committee, who has just proposed a major revision of U. S. tax law by enactment of a 10% value-added tax (VAT) to generate between \$120 billion and \$150 billion a year and permit a rollback of Social Security taxes and income tax rates; and House majority leader Jim Wright (D., Texas).

Ullman, with Senate support from chairman Russell B. Long (D., La.) of the Finance Committee, says he will begin hearings next month on the VAT proposal. The tax, widely used in Europe, is much like a sales tax that is levied at each step of manufacturing on the value added to a product. It is generally favored by industry and conservative economists as a spur to exports—it can, unlike an income tax, be rebated to exporters—as well as to industrial investment. However, the VAT concept is strongly opposed by organized labor and the consumers to whom it is passed on. Nevertheless, Ullman and Long believe some form of VAT, possibly with food products exempted, will be enacted by 1981. AEA vice president Hagerty says the association is working to adopt a joint position on VAT legislation with the Electronic Industries Association.

Senate communications subcommittee chairman Hollings gave further support to the industry view that congressional amendment of the 1934 Communications Act to enhance telecommunication competition and cut back Federal Communi-



**C'mon down.** Sen. Ernest Hollings, sponsor of the Communications Act rewrite, invited firms to move to his native South Carolina.

cations Commission regulations is unlikely to pass this session. But some members of AEA, whose rolls contain no telecommunications industry heavyweights, complained privately that Hollings' breakfast presentation took on a "tacky Chamber-of-Commerce quality" as he injected pitches for high-technology companies to establish plants in his native South Carolina.

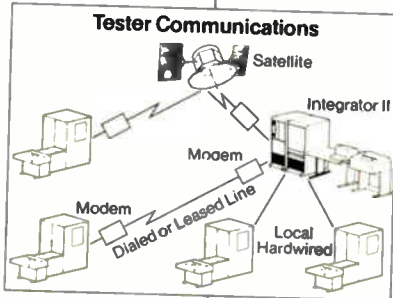
**AEA's other move.** The failure of government policies to control inflation produced some internal political action by the AEA during its Washington meeting. Adopting a new position on inflation control, AEA chairman Noel Fenton, president of California's Acurex Inc., rejected the association's earlier nominal support of President Carter's voluntary price and wage guidelines in favor of a constitutional amendment to control Federal spending.

The amendment, drafted by conservative economists Milton Friedman and Paul McCracken, has been proposed by Sen. John Heinz (R., Pa.) and Richard Stone (D., Fla.) as Senate Joint Resolution 56. Although congressional observers give the Heinz-Stone amendment no chance of serious congressional consideration in this session and only a slight chance of passage any time in the future, AEA executives say they will continue to push it, recalling their earlier success in promoting passage of a capital gains tax rollback that was written off prematurely as politically unacceptable. □



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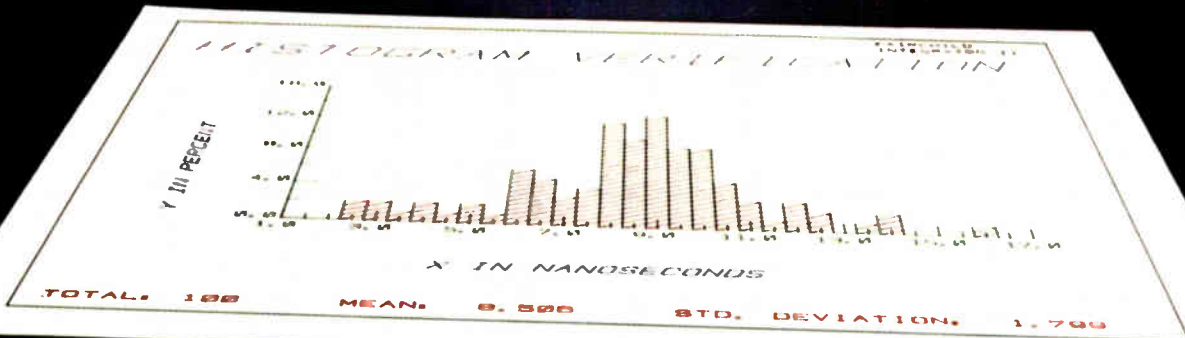
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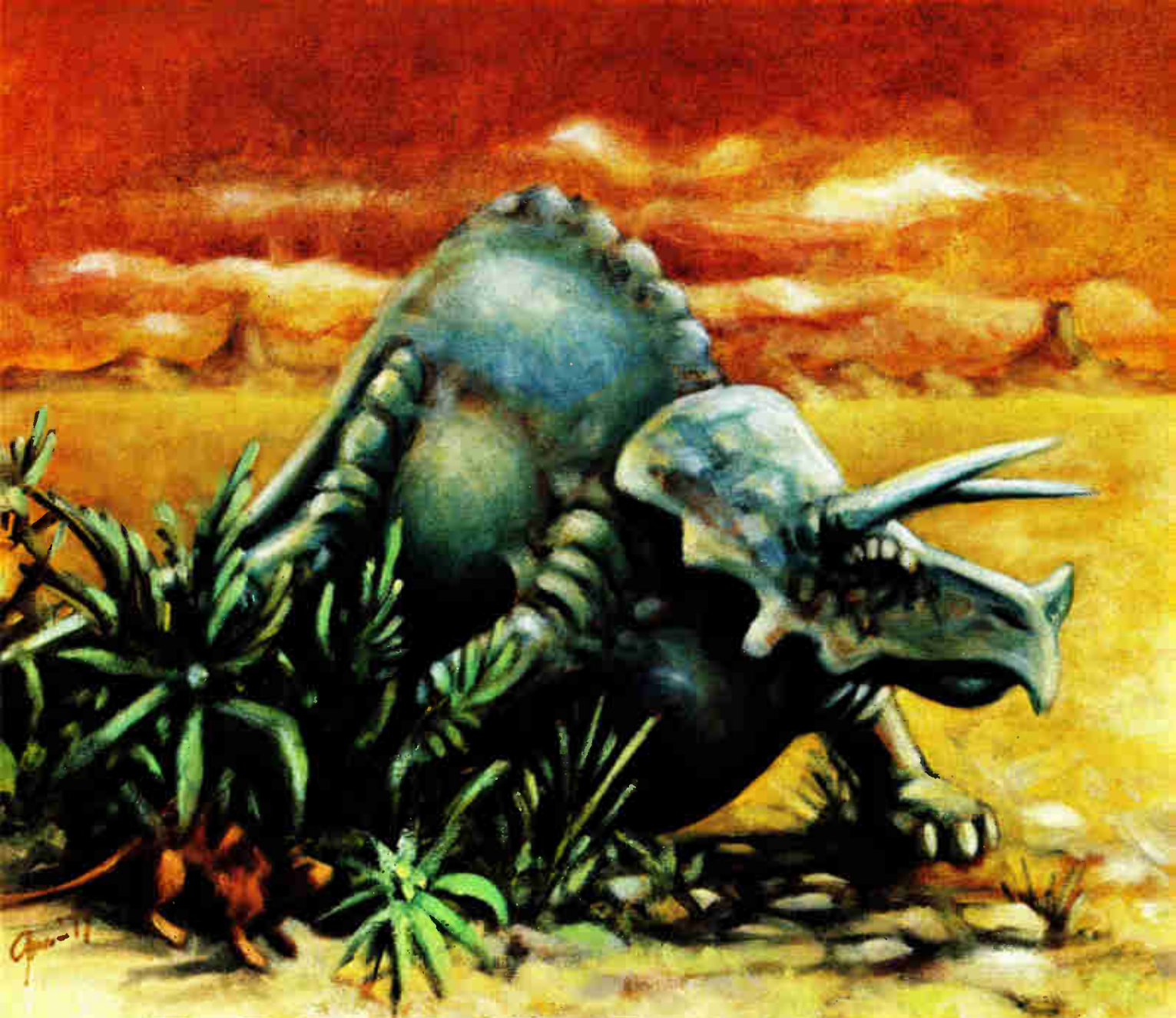
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## Clad vs. plated.

A good basis for understanding "clad" is to compare it with gold plating. Essentially, the difference between the two is the molecular structure of the gold on the contact surfaces, and how the gold is applied.

The gold in a TI clad connector is *wrought* gold which is pressure bonded to a base "spring" metal. The bonding process



Partially bonded strips of metal.

starts when long strips of hard 18kt gold foil are actually rolled into the base metal. After annealing to complete the bond, this inlayered composite is then rolled under tremendous pressure until it's reduced to the desired contact thickness.

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Besides being smooth, the gold is also thick. TI clad connectors have a minimum of 50 microinches of gold at the point of contact, the only place it's needed.

On the other hand, most gold platings are no more than 20 to 30 microinches thick — much too thin for durability. And since plating is an electro-chemical deposition process, many gold plated surfaces tend to be porous and rough, making the connector vulnerable to the kinds of corrosion and abrasion that cause intermittencies.

Clearly, gold plated connectors just don't measure up to clad.

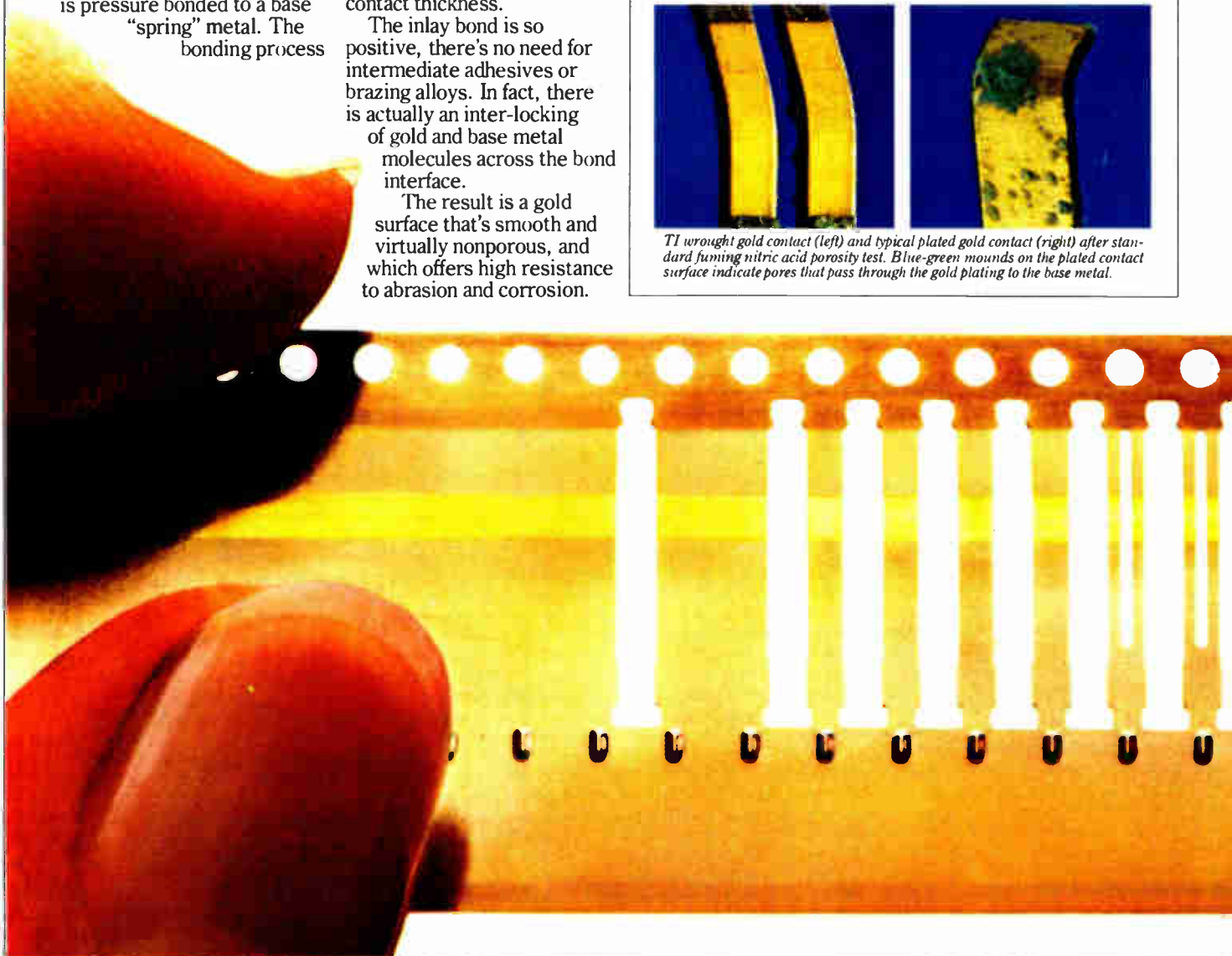
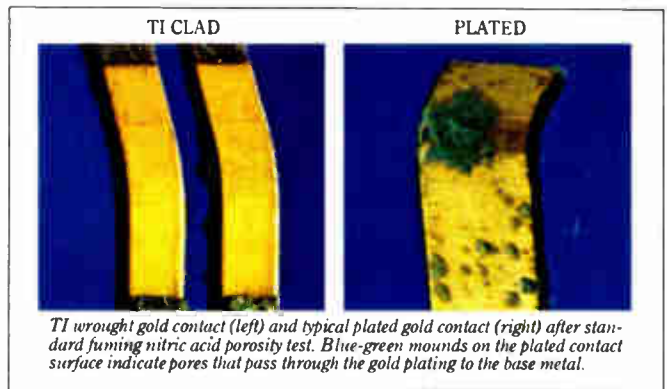
But how about price? If our clad connectors are so

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only where it's needed – at the point of contact – you can count on the price being *less* than what you'd pay for an ordinary connector.

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Though a wrought gold inlay is the outstanding feature of a clad connector, there are, of course, other features. They're not as easy to see as the gold, but nevertheless, they're there. They include the following:

Preloaded cantilever contacts that provide excellent insertion/withdrawal force ratios.

Highly conductive, corrosion resistant CA 725 alloy base metal.

Bifurcated contact beams for double protection against system failure.

Individually replaceable contacts which can be changed without removing an entire connector from its mounting.



*Cross section of H4 Series Edgeboard Connector.*

And UL approved polyester insulating material.

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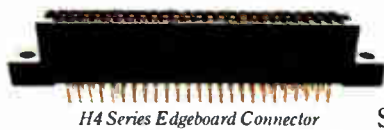
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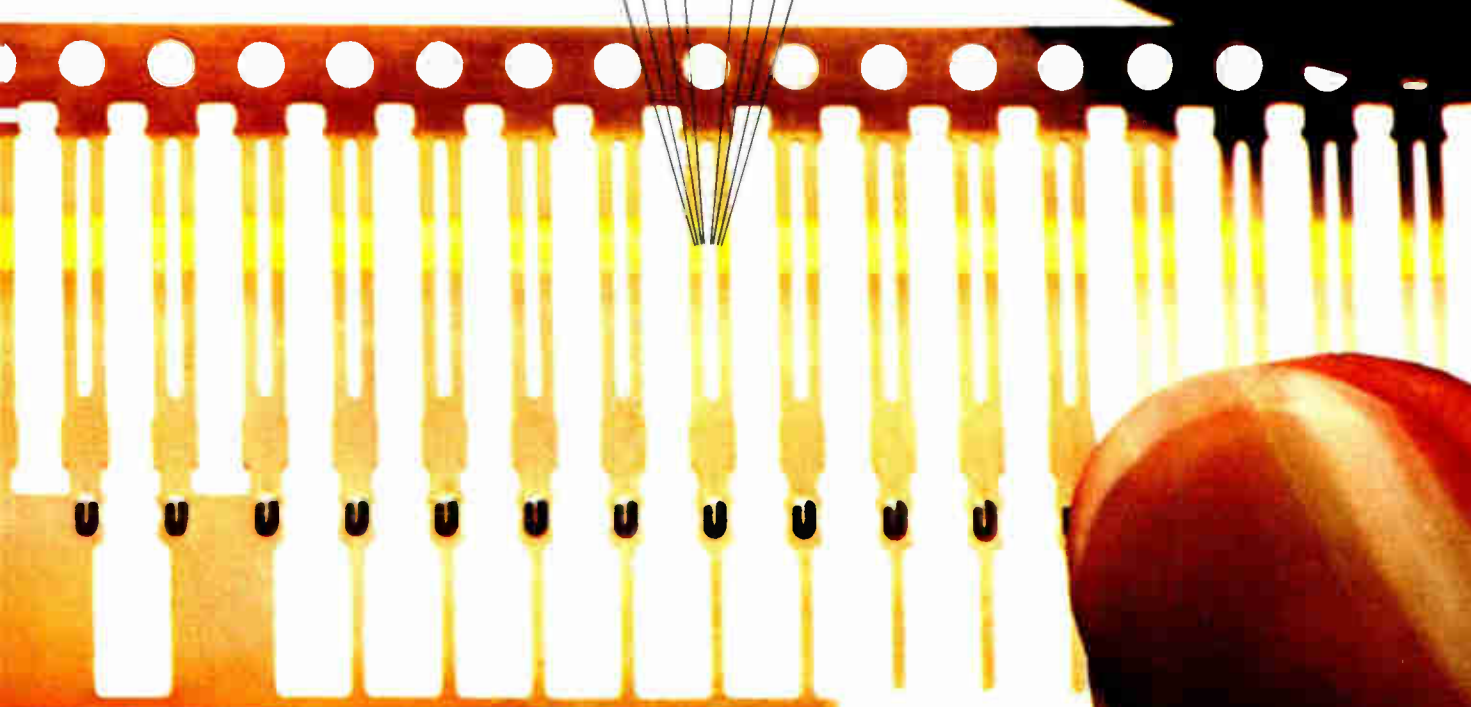


*H4 Series Edgeboard Connector*

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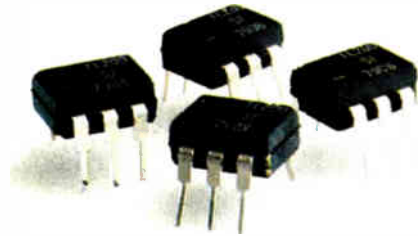
*Clad metal is:*

- More conductive*
- More durable*
- Non-porous*
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*Clad metal strips are stamped into contacts by high speed presses.*

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IL-203	225 to 450%	50% min.	5000 volts	\$1.20

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ILD-1	2	20% min.	2500	30	50	\$1.36
ILQ-1	4	20% min.	2500	30	50	\$2.90

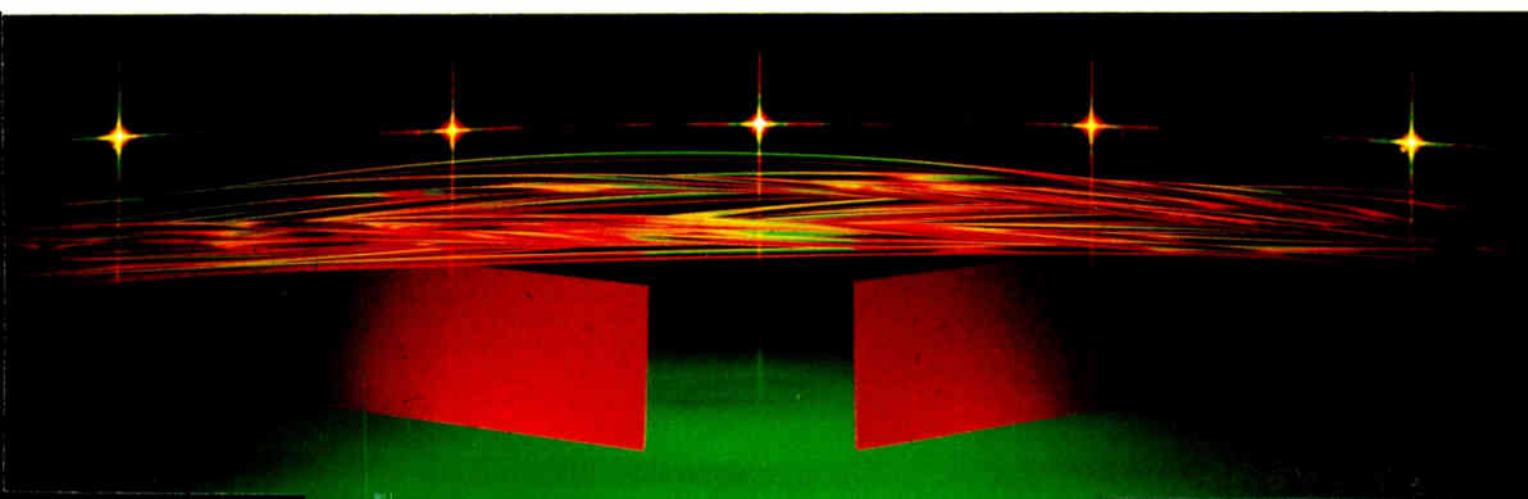
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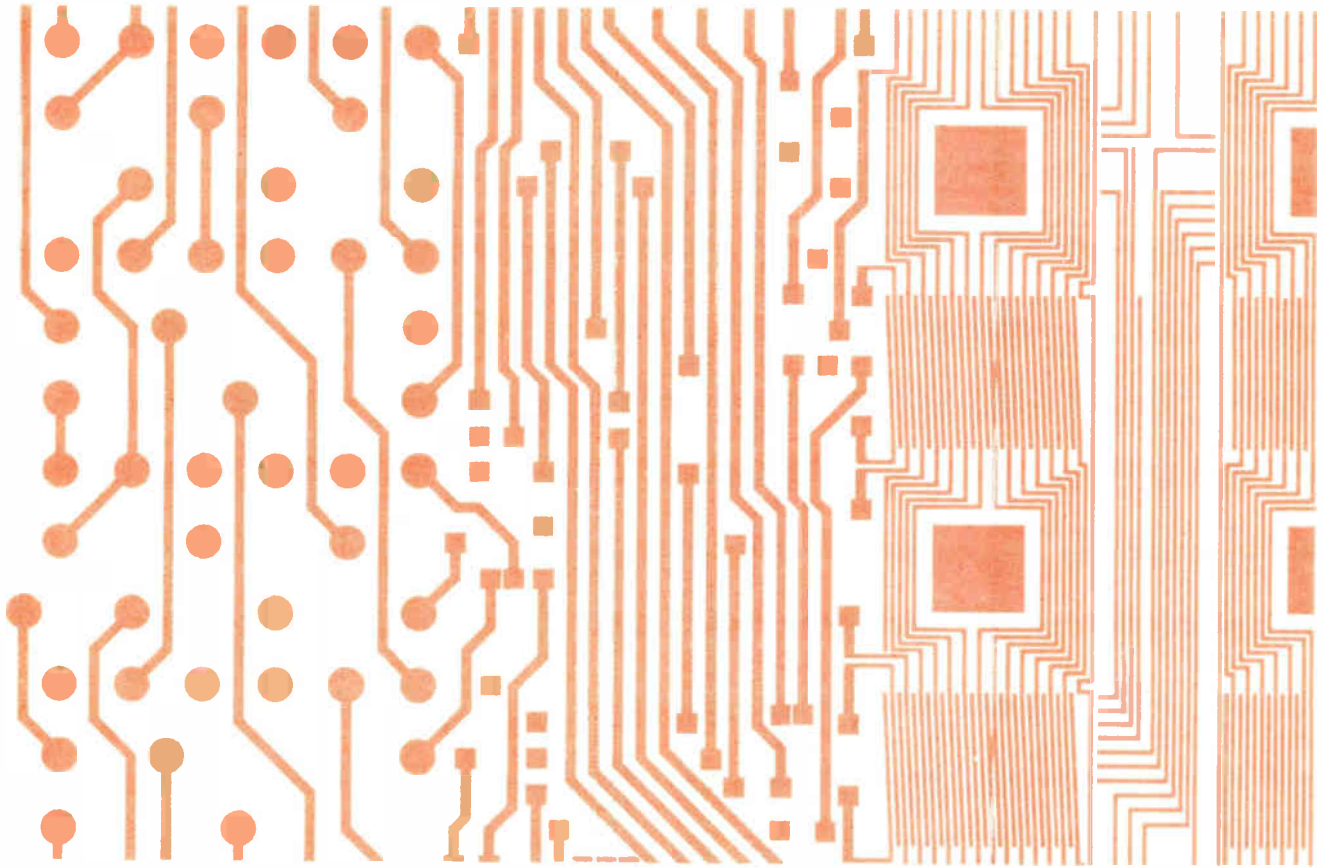
Circle 112 on reader service card

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## THE LIGHTS FANTASTIC







# Wanted: a new interconnection technology

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Neither thick-film hybrid nor printed-circuit board, the substrate of the future will achieve high density with surface-mounted components

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by Charles L. Lassen, *Exacta Circuits Ltd., Selkirk, Scotland*

□ Succumbing to the strong temptation to play soothsayer for the semiconductor business, many feel that all signs point to the emergence of a new breed of interconnecting substrate. Increasing chip density has required more pins per package, which in turn has meant an increase in interconnection density. The following is an attempt to predict the future development of this as-yet-unborn ideal substrate, which will be neither printed-circuit board nor thick-film hybrid and will be referred to here as multistrata.

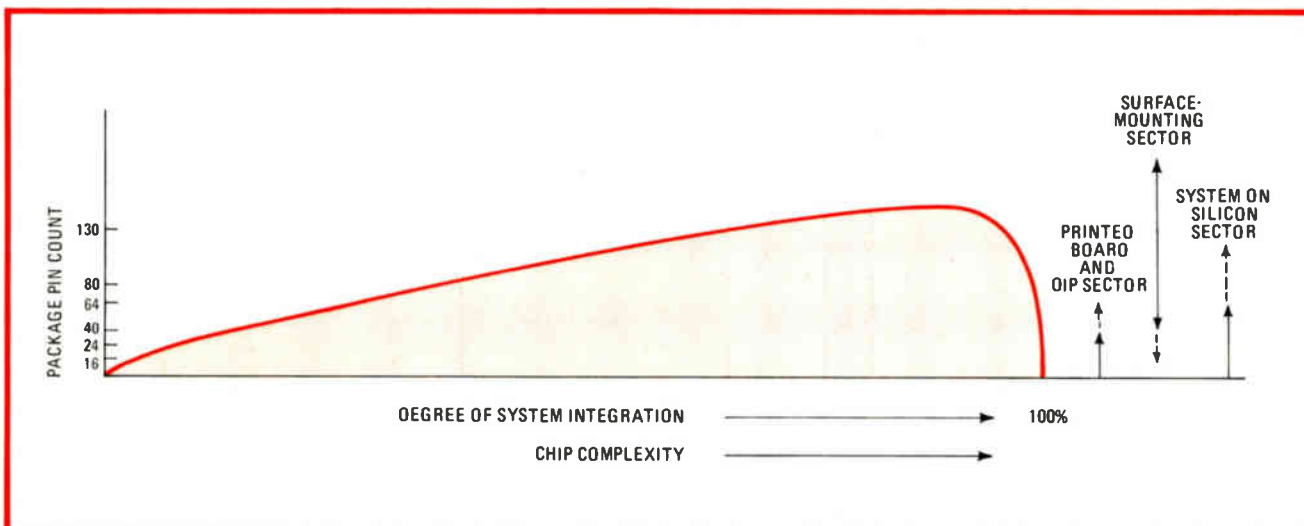
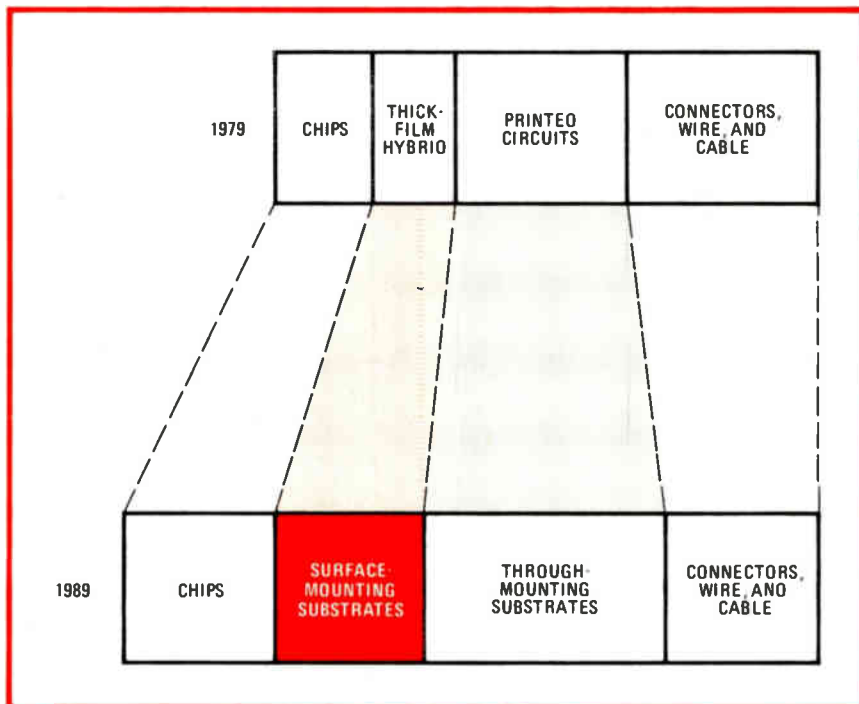
To understand the detailed requirements of the possible "substrate of the future," it is necessary to consider how the components that it is designed to interconnect will evolve. In the near future, two things will happen.

First, a larger proportion of components housed on substrates of any type will be active devices and, secondly, there will be many more of them. Now, for instance, two out of four component terminals connected by printed wiring are integrated-circuit terminals. By 1985 that proportion will have risen to three out of four, and the total number of terminals to be connected will have more than doubled.

### Climate of change

In today's electronic packaging area, the dual in-line package (DIP) and the pc board with plated through-holes have now established such a dominant position that it is difficult to conceive of a new combination of pack-

**1. Today and tomorrow.** This is a projection of packaging trends from the present to 1989. According to this scenario, a new surface-mounted substrate will emerge in the late 1980s under the pressure of cost reduction and densely packed VLSI.



**2. Integration versus pin count.** This is a diagrammatic representation of integration versus pin count for three different packaging media. As the degree of chip complexity goes up, surface-mounted boards become the most effective packaging medium.

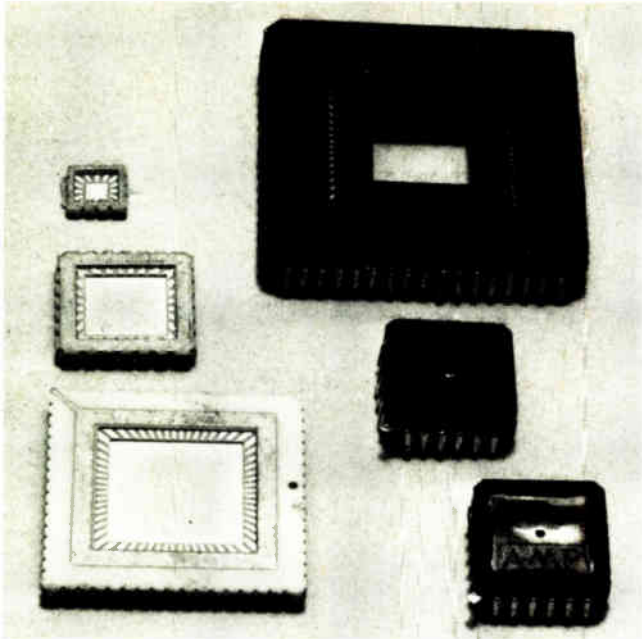
aging technologies that could evolve in the future for general applications.

However, the new smaller IC packages, increased interconnection density, the need to shorten the cycle from design to prototype, faster circuits, the trend toward single-board equipment, higher heat densities, the challenge of surface-mounted components, and the increasing cost of interconnection are sure to demand new methods. This climate of change promises to create the need for large-area substrates for surface-mounted components. A possible scenario for electronic packaging in 1989 is depicted in Fig. 1.

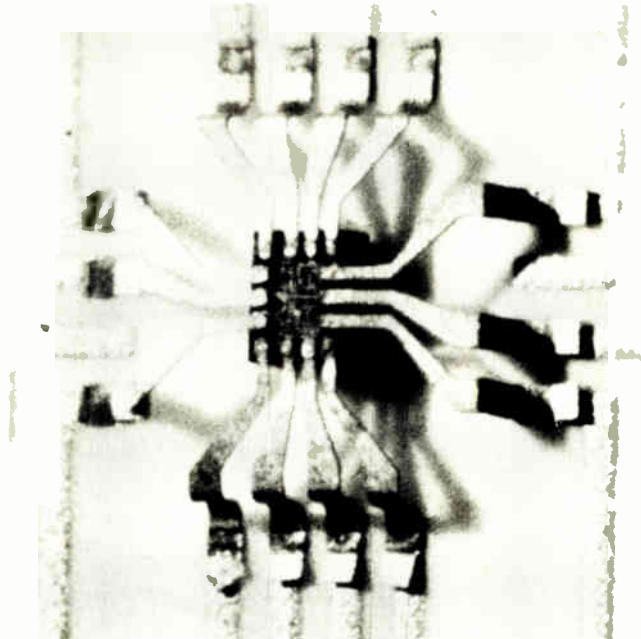
Of all the factors affecting interconnection, it will probably be a package change that will be the pivot and cost reduction that will be the driving force. The enormous economies possible with greater chip integration

have unfailingly produced an annual increase in chip complexity of one and a half times, and this trend is predicted to continue.

The ongoing integration effort will push up the pin count per package until complete systems on silicon are reached, when the pin count will start to decline again (Fig. 2). Custom chips are currently being made with 60, 80, and more than 100 pins, and uncommitted logic arrays, which need 50 pins or more, are available. The 1980s will see neither the widespread adoption of complete systems on silicon nor a continuation of today's configuration of one or two large-pin-count devices surrounded by small- and medium-scale integration. The need to interconnect a number of high-pin-count devices could well arise as very large-scale integration embraces a larger proportion of IC production.



**3. Chip-carriers or TAB.** The multistrata achieves its high component density with surface-mounted active and passive components. Illustrated to the left are small leadless ceramic and plastic chip-carriers. To the right is a chip on a film carrier.



These high-pin-count devices are unlikely to be housed in dual in-line packages, which are less cost-effective above 40 pins. The DIP with a high pin count occupies a lot of real estate, has long electrical paths, is awkward to attach and remove from the board, and is expensive to manufacture. The quad in-line type (a rectangular package with two pairs of rows of staggered pins on 100-mil centers) is a temporary improvement, but the chip-carrier (a small, square, ceramic or plastic, leadless package) is most likely to be preferred for the growing family of devices with a high pin count.

Tape automated bonding (TAB), which mass-bonds ICs to copper micro-interconnections on insulated film, is also receiving a good share of development dollars. The availability of machines to handle, sequence, and place random TAB components automatically from slide carriers will give this technology the impetus it deserves. Standardization of tape patterns and the incorporation of circuitry for testing during burn-in will be required before these components can offer a major advantage over bare chips.

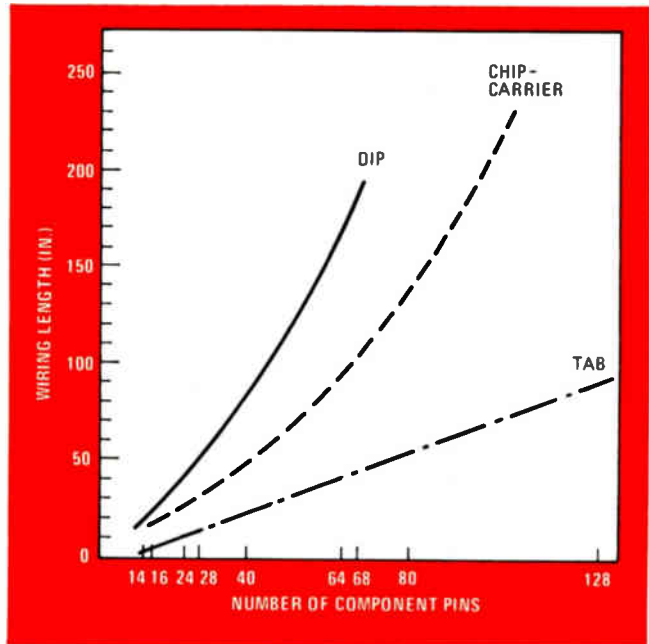
Both chip-carriers and TAB have as packages very significant implications for the interconnection substrate. They are surface-mounted (Fig. 3) and, as fully tested devices, they enable 100 or more components to be assembled, with acceptable production yield, onto a single substrate.

#### Interconnection density

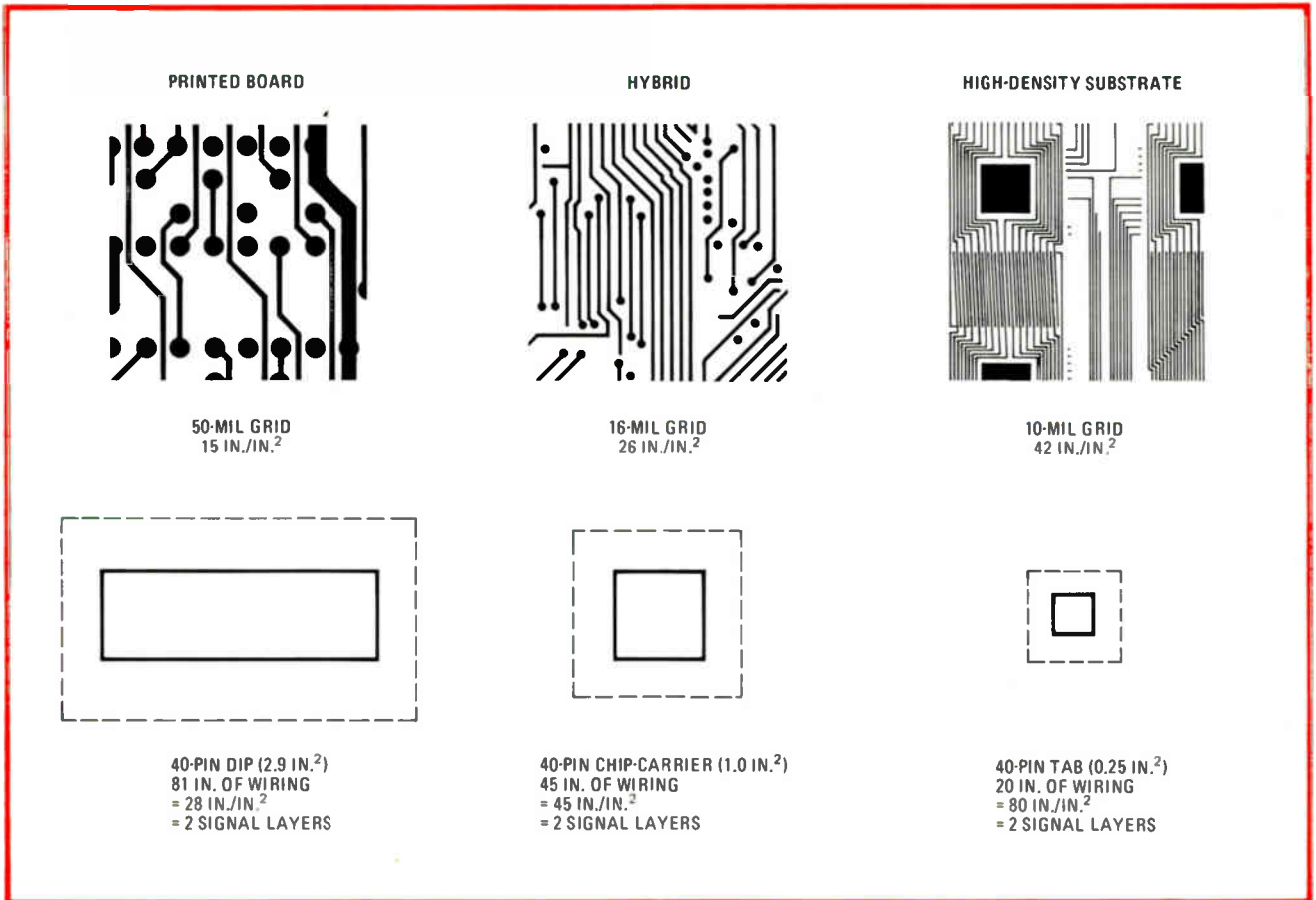
One of the first results of high pin counts on 40- or 50-mil centers (chip-carriers) or 20-mil centers (TAB) is an increase in the interconnection density on the substrate. Figure 4, based on the observations of IBM's Donald Seraphim and others, plots the typical substrate interconnection length against pin count for devices packaged in DIPs, chip-carriers, and TAB. Figure 5 shows the normal wiring density achievable today in production

with different substrate technologies. This is expressed in terms of inches of wiring length per square inch of signal layer.

In the specific example of 40-pin devices, a DIP requires 81 in. for interconnection; a chip-carrier 45 in., and a 40-lead TAB component 20 in. Assuming that these lengths must be accommodated in an area equivalent to that occupied by the package and its immediate surroundings, it can be seen how appropriate current double-sided plated-through-hole pc geometry is to the



**4. Wiring lengths.** This plot of wiring length in relation to the number of component pins for DIP, chip-carrier, and TAB packages reveals that the TAB package is by far the preferred option. At present, though, the DIP and chip-carriers are more readily available.



**5. Wiring density.** A comparison of wiring densities achieved with 40-pin DIPs and film chip-carriers shows that film carriers on a 10-mil grid have a wiring density of 80 inches per square inch of surface as compared to 28 in./in.<sup>2</sup> for DIPs on a multilayer pc board.

DIP components and how substrates with 16- and 10-mil grids respectively are required for chip-carriers and TAB if two signal layers are to interconnect.

Interconnection density can be eased if more than two layers are used. Additional planes may well be required for power distribution, reduction of cross-talk, and to provide a controlled impedance. A buried-via connection between signal layers that does not pass through all layers improves interconnection density and makes design layout much easier, particularly if a computer is being used.

So if one were to write an ideal multistrata product specification in the area of interconnection density, it might read:

- Channeling: 10-mil grid.
- Line width: in the range 1 to 5 mils as appropriate to meet electrical and production yield tradeoffs.
- Vias: buried and integral with line.
- Number of layers: two or more.

Thick-film multilayers can achieve the required density quite economically. The simple crossover via of a thick-film hybrid does not suffer the channeling interruption of the printed-board hole and pad, while the hybrid's ceramic base has the added advantage of providing printed resistors that are low-cost and stable, though this advantage will be less important in the future. But available areas are small and the material is fragile, which makes the substrate a component or, at

best, a daughterboard. Other drawbacks are the very tight control of screen printing required for large-area multilayers and the problems of location, flatness, and registration for automatic chip assembly. Poor track conductivity is only likely to be a problem with power distribution.

### Design layout and tooling

The true cost of design layout and tooling of multi-layer pc boards is seldom recognized. Figures furnished by Exacta, one of the large European manufacturers of multilayer and plated-through-hole boards, show an average lot size per order of 206 units. Assuming a typical board price of \$30 and design and tooling costs of \$2,000, amortization of these costs increases the unit board price for this lot size by a third. This type of amortization calculation is seldom done by a purchaser who is concerned with the unit price of the board and is divorced from the in-house cost of the design layout.

It is therefore not surprising that circuit-writing techniques such as Multiwire, which automatically lays down insulated wires on an adhesive-coated epoxy-glass board, have as yet achieved relatively little market penetration. But true cost awareness is emerging, and some in-house board makers are thinking of using the digital tape drive for the photoplotter to generate prototype track patterns directly, thus cutting out the hassle of plotting, spotting, contacting, and punching artworks.

The semiconductor industry's use of electron-beam printing and the thick-film industry's flirtation with fast writing equipment—both eliminate the need for masks or screens—serve as examples. Circuit writing is essential for any new interconnection technology, both for prototyping and during development. Production yield may also improve. The specification for the ideal multistrata might therefore continue:

- Conductor generation: by fast digitally driven circuit-writing techniques.

Solder-Wrap, an automatic wiring method in which wires are wrapped, cut, and soldered onto special low-profile terminals on a regularly patterned pc board, is fast. Multiwire, although slower, offers a substrate with controlled electrical characteristics recognizable as a printed board rather than a breadboard. These and other discrete sequential wiring systems are ideal for circuit modifications and development. However, they all suffer from the problem of high unit cost as soon as the volume crossover point with conventional technology has been passed.

### Electrical characteristics

The speed of integrated-circuit operation is steadily increasing, and even faster circuits are coming. Some projections of gate delay times and memory access times are shown for VLSI circuits in Table 1.

Fast rise times increase the problems associated with line reflection and crosstalk, and these problems will become more widespread in the future. Line reflection generally becomes a problem if the conductor length exceeds one hundredth of a wavelength. With a rise time of 1 nanosecond, this means that control of impedance is desirable for conductor lengths on epoxy glass in excess of 3½ in. Crosstalk on double-sided boards becomes a problem when line spacings go below 30 mils.

Only a small percentage of engineers actively engaged in circuit layout understand transmission-line theory and the physical design needed for fast switching circuits. The computer programs for circuit layout increasingly used to aid these engineers are very difficult to program to take account of electrical rules as well as routing.

It is unlikely that the proportion of engineers with transmission-line understanding will increase enough to meet the accelerating need for circuit designs using fast devices. Therefore any new interconnection technology must as far as possible be electrically forgiving. The advice KISS—keep it short, stupid—is very appropriate to the reduced line lengths possible when chip-carrier packages and particularly TAB are used.

For longer lengths, precise control of dielectric and track width will be required. Thin dielectric separation will be required in the multistrata because of the desirable buried-via construction and the need to keep a reasonable aspect ratio in the hole to ease manufacture. A dielectric material with a constant of 3.5 or less must be used to reduce capacitance and propagation delay and achieve an adequate characteristic impedance with manufacturable line widths. For example, a 50-ohm line in stripline construction might have a line width of 3 mils and a dielectric separation between track and ground plane of 5 mils.

ACCESS AND DELAY TIME PROJECTIONS				
Average values for advanced circuits				
Nanoseconds		1975	1980	1985
Memory	MOS	150	40	10
	bipolar	15	4	2
Logic	MOS	15 – 50	5 – 15	2 – 5
	bipolar	4 – 40	3 – 10	2 – 4

SOURCE: GNOSTIC CONCEPTS INC

The ideal multistrata product specification for electrical characteristics might read:

- Line length or controlled impedance: under 3.5 in. where possible or 50, 75, or 100 ohms  $\pm 10\%$  using minimum track width suitable for economic production, with a minimum dielectric thickness and a dielectric constant under 3.5.

The high packaging density will require high-conductivity power planes, so copper is the preferred conductor.

Conventional pc-board geometry is well suited to controlled-impedance circuits. With track widths in the range of 5 to 20 mils and a dielectric constant of 5.02, a wide range of impedances can be obtained. Unfortunately, the required interconnection density is achieved only at the expense of additional layers. To provide printed-circuit electrical characteristics with reduced physical dimensions, the multistrata must trade off manufacturing technique in the areas of deep buried vias and production yield with narrow conductors.

Another consequence of greater integration is a tendency toward single-substrate systems, which emphasizes the growing importance of integral input/output access to the substrate. Figure 6 illustrates some combined flexible-circuit and multilayer developments at Exacta that were based on a belief in the importance of a single interconnection package to mount components and access them. This feature should be available to the multistrata, and where there is a need for multiple modules, as in racked equipment, a low-cost connector with 20-mil pitch fingers for reflow surface mounting is required.

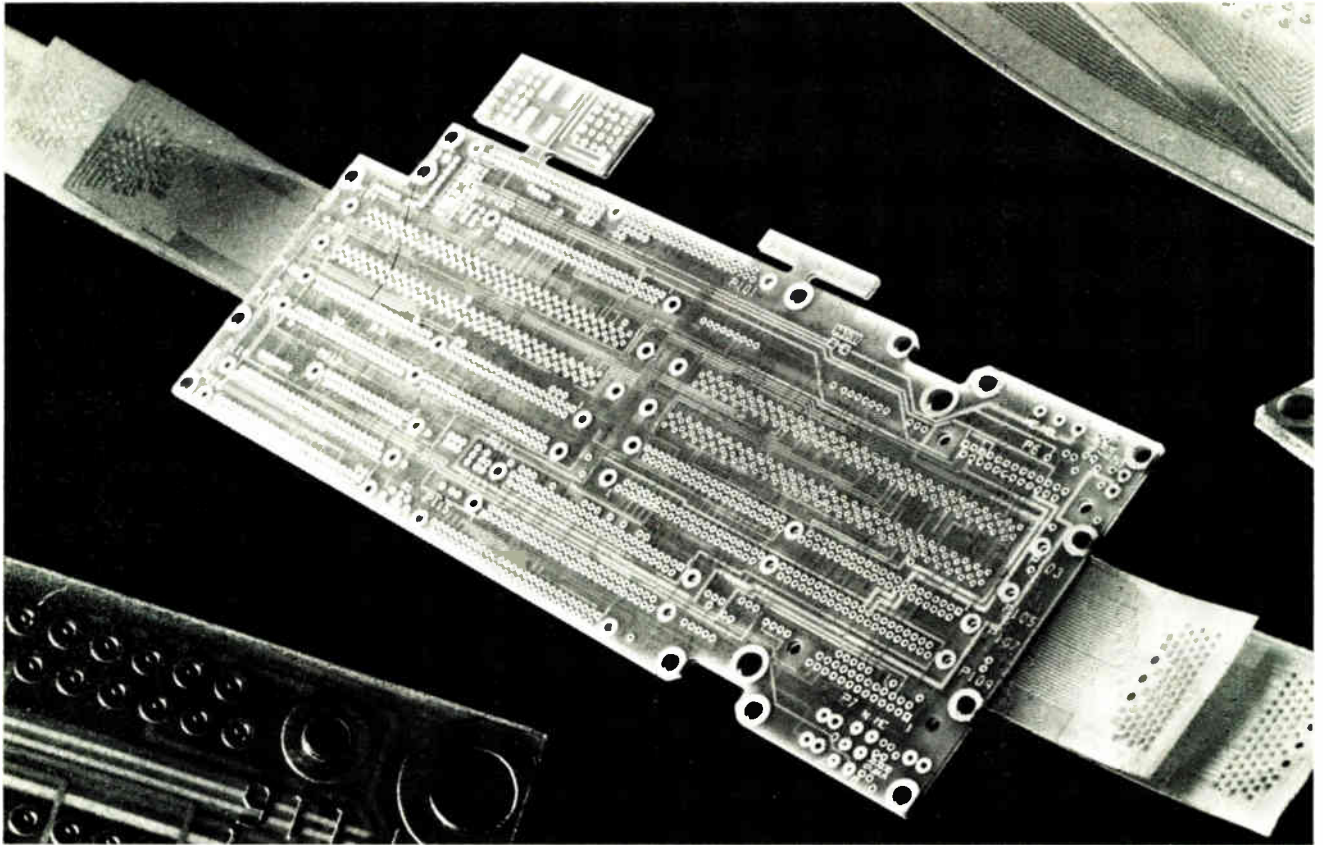
### Greater accommodation

Substrates may have to accommodate 60 or more active devices before production yield, testability, and service considerations become critical. This number is generally much higher than for conventional ceramic hybrids but it still remains within the cost realm of a throwaway item. For chip-carriers this indicates a substrate area of 45 to 50 in.<sup>2</sup>, and for TAB an area of 10 to 15 in.<sup>2</sup>. Figure 7 indicates some of the possible configurations.

The ideal multistrata product specification in this area therefore reads:

- Input/output address: by integral flexible circuit or 0.020-in.-pitch surface connector.
- Substrate size: up to 50 in.<sup>2</sup>.

A technology that most nearly approximates this spec-



**6. Flexi-rigid.** The concept of putting complete systems on one board has led to combination flexible and rigid multilayer boards. The rigid section contains components and interconnections; the flexible sections give added input/output and eliminate cabling and connectors.

ification and that meets as well many of the other requirements is the Lampac circuit that has been described by Verne Brown of Bell Laboratories in Denver. Using a 5-mil film circuit bonded to an insulated steel backing, this technique achieves high density at medium cost over a large area, with reasonable heat dissipation and the option of flexible access tails. The steel plane reduces crosstalk but does not provide the controlled characteristics achievable with a multilayer board. Material movement of the thin circuit during processing is likely to lead to assembly problems with small features over a large area.

### Thermal considerations

While the power consumed per integrated-circuit function is decreasing, the number of functions per chip is increasing. This has led to increased power consumption per device, but opinion is divided on what power the VLSI of the 1980s will dissipate. A norm of around 1 watt per device is predicted.

The greatest impact on a substrate's thermal management will be due to the package change, which will enable chips to be placed much closer together. Power densities of 0.75 w/in.<sup>2</sup> and 3 w/in.<sup>2</sup> may have to be handled for chip-carriers and TAB respectively.

If junction temperatures are to be held to a reasonable level (about 100°C) by using convection cooling or forced air in the worst case, it may be necessary to add a heat stud to the chip-carrier and certainly necessary to have a good thermal path from the chip to a finned heat

sink if TAB circuits are to be used.

The multistrata thermal specification therefore reads:

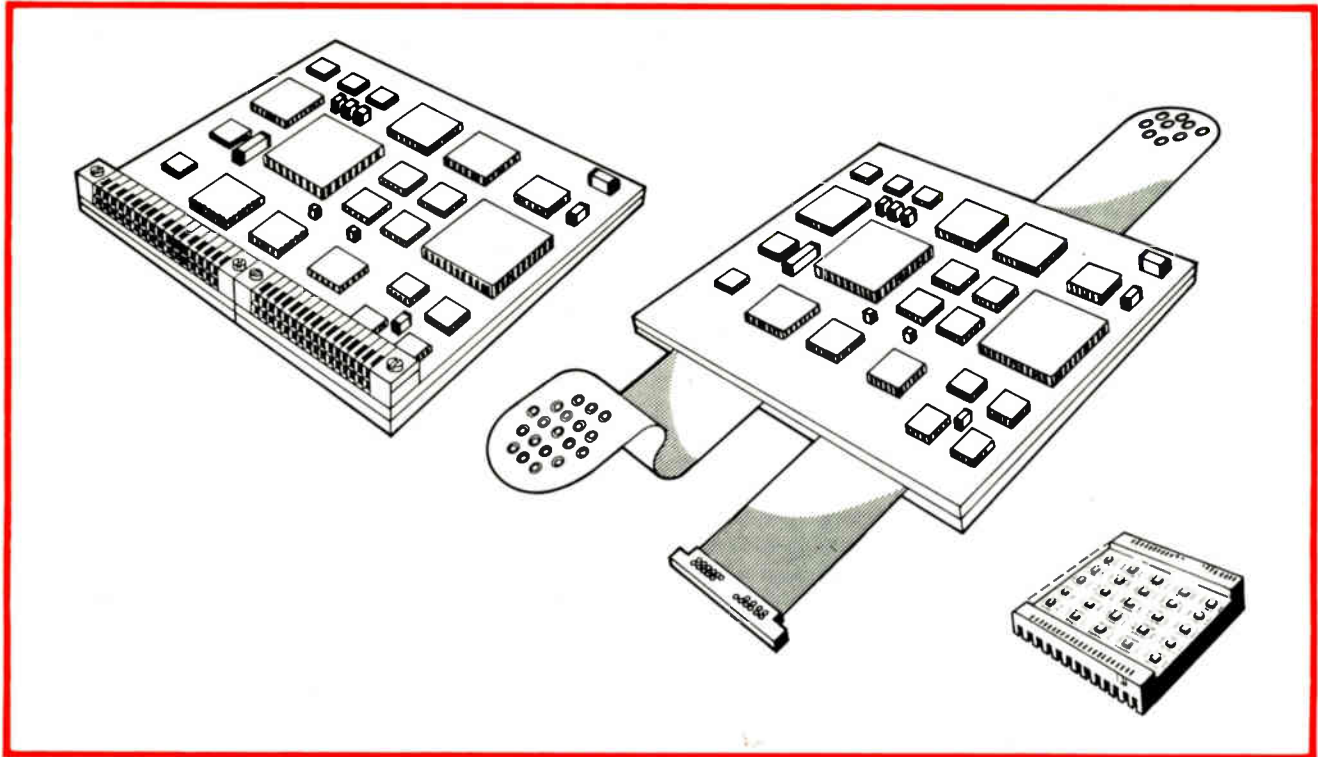
- Construction: thermal path from chip to built-in heat sink such that, with a density of 3 w/in.<sup>2</sup>, chip junction temperatures of 100°C are not exceeded using blown air at 600 ft<sup>3</sup>/minute and 25°C.

Most metal-cored board constructions provide good heat spreading but not particularly good dissipation. A substrate offered by the Pactel Corp. (Fig. 8) solves this problem with a stud plated with solid copper directly under the chips leading straight to an aluminum heat sink. This board also has the advantage of high interconnection density, large area availability, and precise feature definition and registration. The real cost of volume manufacture of this type of unit is not yet known, but it could be high unless yield can be improved and the number of process operations reduced.

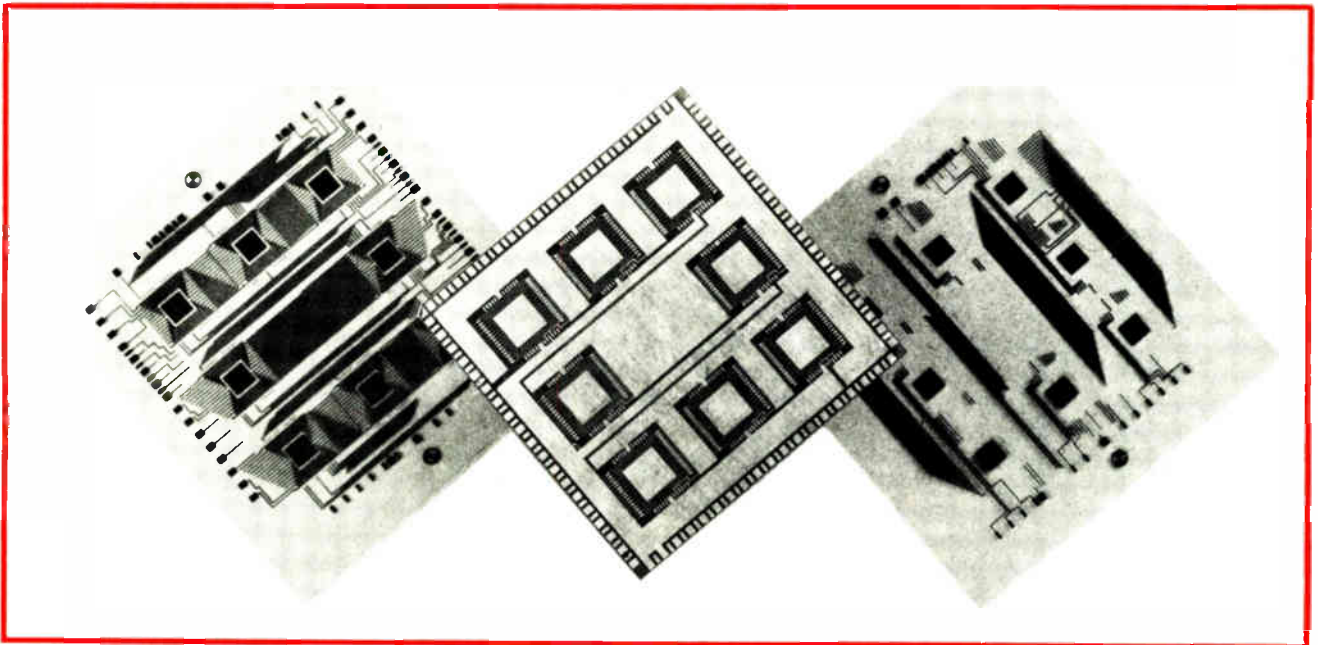
### Component attachment

A number of passive components exist for surface mounting and fully tested active components will also become available, boosting the substrate demand. Chip capacitors and resistors for reflow soldering are compatible with ceramic chip-carriers, and some work has been done to provide capacitors in TAB form for military applications. Like resistor nets available in DIP form, passive components will become available to suit chip-carrier or TAB assembly.

The real choice in surface-mounted devices is between compliant or noncompliant leads. Plastic chip-carriers



**7. Multistrates.** To the left is a multistrate that is based on chip-carriers and resistive and capacitive chips. In the center, a chipstrate is combined with flexible circuitry to give greater access. To the right is a small densely packed multistrate covered with TAB components.

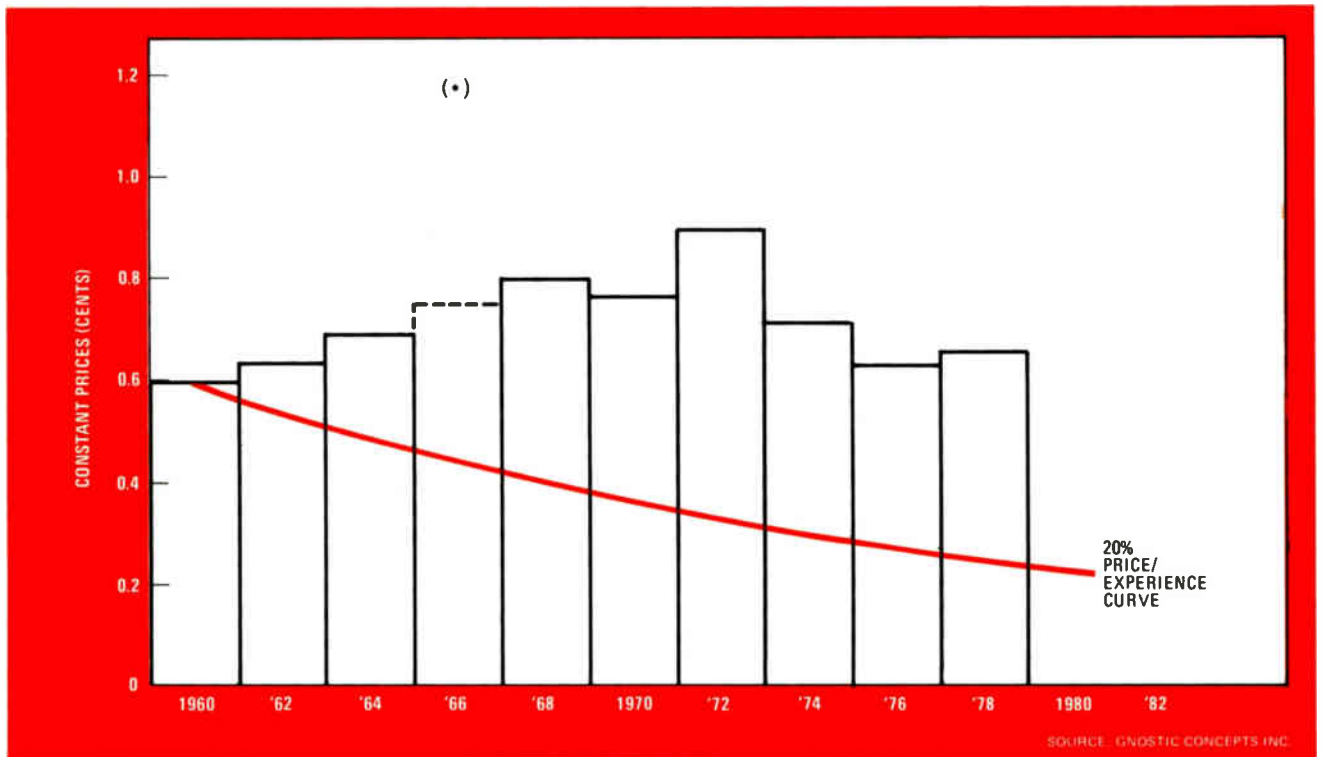


**8. TAB on aluminum.** At center is a Pactel multilayer substrate containing eight 64-pin TAB custom chips. On either side is artwork for two inner layers. Layers of polyimide film with additively plated conductors laminated to an aluminum plate compose the board.

and TAB have compliant leads, as does the old flat pack. Engineers with experience of flat-pack assembly may not warm to the resurrection of this type of surface mounting, but conditions are different today, what with the sheer quantity of components requiring automatic assembly and the large volume of successful consumer experience with surface mounting. Japanese firms have used plastic multileaded flat packs for some time.

If noncompliant leads are to be used, the substrate needs to have a coefficient of expansion closely matching that of the component packages, which will probably be ceramic. Dielectric reinforcing materials with a negative coefficient of expansion have been successfully incorporated and the circuit supported by materials such as nickel-iron alloys.

The other critical aspect of the automatic assembly is



**9. Rising costs.** Pc board costs have gone contrary to the normal price-experience curve. Instead of decreasing with time, they have either increased or remained constant. Complexity of new board designs caused by changing LSI designs has prevented board cost savings.

pad registration. Although optical search and alignment equipment can be incorporated, it slows down assembly. Solder collapse can take up registration tolerances only over a small area.

The multirate product specification in the area of component assembly therefore reads:

- Substrate thermal coefficient of expansion (TCE): 2 to 10 ppm/°C.
- Component pad registration to datum line:  $\pm 2$  mils.
- Substrate temperature withstanding: 265°C for 5 seconds.

Porcelainized steel is also an attractive substrate. This technology combines the interconnection density of thick film with the large area of a printed board, as well as the option to mount a limited number of high-power components, plus reasonably stable printed resistors.

### Steel factors

However, from an assembly viewpoint, porcelain and screen print control must be very good to achieve registration over a large area, and the low-cost attraction of this high-volume technology may be diminished for high-density short runs. Thermal characteristics are reasonable and the TCE may just be good enough for leadless ceramic components.

The various technical factors outlined above are, by themselves, insufficient reasons to make a general and dramatic change in interconnection technology. But it has been said that there are 10 good reasons for doing anything and the first 8 of them are cost. The pc board cost content of electronic equipment now rivals IC cost content in dollar value. But it so happens that, though IC cost content per function continues to decrease, pc board

cost content per interconnection is largely static.

Figure 9 shows the cost per printed board interconnection at constant dollar prices. A 20% price experience curve is superimposed, and the cost per interconnection would be expected to follow this curve. Perhaps one reason why the cost per interconnection has not been substantially reduced is that component packing densities, unlike those of semiconductors, have shown only slow decreases over the years, being limited by the universal 100-mil spacing of the DIP leads.

This indicates that a package change could yield a breakthrough in cost per interconnection. Line widths and spaces on the new substrate technology may not be substantially different from those achieved by today's best printed board production (5 mils) but the density of lines per in.<sup>2</sup> will be much greater.

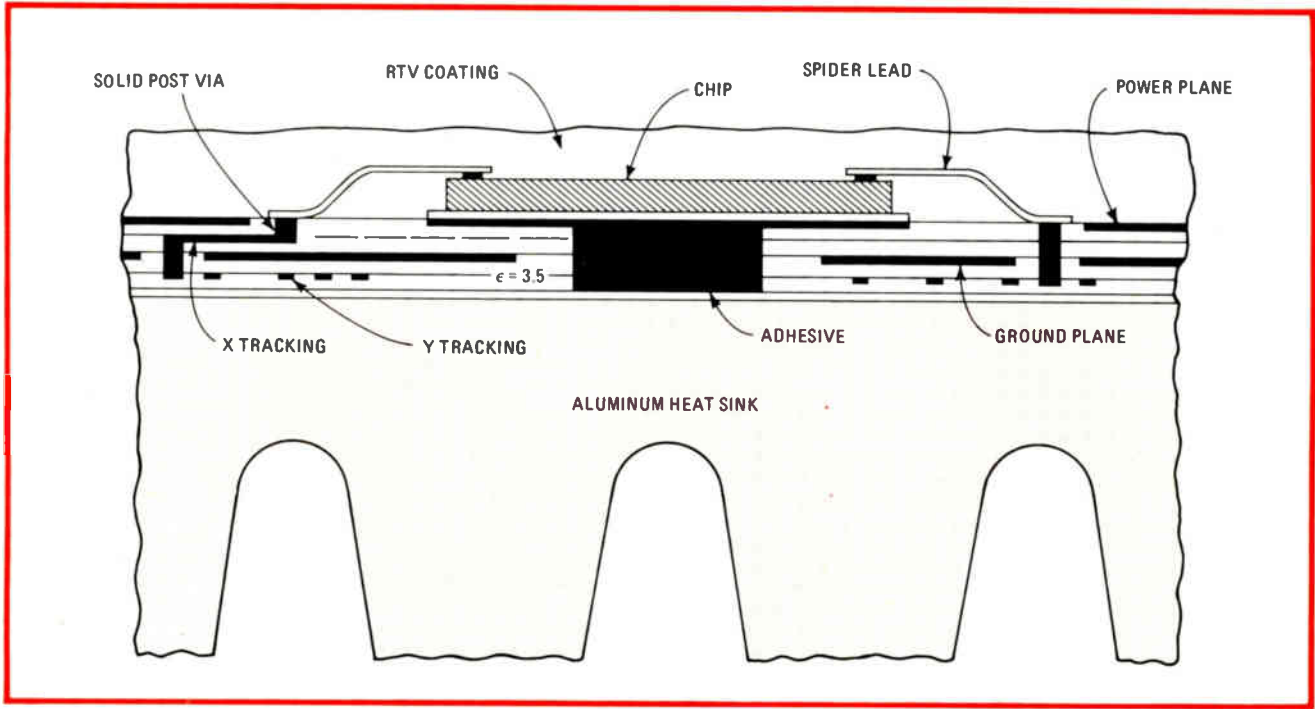
Currently the real estate occupied per integrated circuit costs typically \$0.28 in Europe. To reach the threshold of acceptance, a new technology must aim to cut this cost per device area by 25%.

### Manufacturing options

A manufacturer has the option of processing a lot of small substrates very quickly or larger substrates more slowly and then cutting them up. The latter approach is preferred here because of its use of photo printing for precise registration and to retain the flexibility of size options. Assuming four TAB components per square inch, it is a far from impossible task to produce a substrate with two signal layers and 10-mil channeling for a finished cost of \$90 per square foot and with a 75% yield.

The multirate product cost specification should therefore read:





**10. The future?** This is a side section of a conceptual multistrata designed for chips on film-carriers (TAB). Basically the unit is a high-density sequential multilayer with an organic dielectric mounted on a metal plate having an area between those of a hybrid and a pc board.

■ Selling price per conductor layer: \$60 per square foot for lot sizes of 200 and over (TAB).

One low-cost technology for surface mounting that gives high density is the cofired ceramic multilayer, a structure where all layers are fired simultaneously. Many layers at low cost rather than a few higher-density layers at higher cost achieve high density. Unfortunately, available area is limited, prototypes and short runs require fairly heavy tooling charges, and—because conductor features must be printed prior to firing—it is difficult to achieve the precise location of pads in relation to an assembly datum.

### Manufacture

This attempt to formulate an idealized product specification shows the desirability of high-density, sequential multilayer with an organic dielectric of specific thickness mounted on a low-expansivity metal plate, sized somewhere between a hybrid and a printed board, which can be produced at low cost and high yield using digital “wiring” techniques.

The physical characteristics of the substrate will be different for chip-carriers and for TAB. For example, a support plane of nickel-iron alloy would be appropriate for leadless ceramic chip-carriers, whereas an extruded aluminum heat sink might be required for TAB components, but in both cases the technique of building up sequential layers from a metal plate is identical.

An indication of what a section through a multistrata for TAB components might look like is shown in Fig. 10. The dielectric is a 5-mil-thick polymer, applied from a roll to produce a conformal coating with a flat surface for subsequent processing. Blind via holes are formed by laser drilling, using the reflective properties of copper. Via conductivity is achieved by plating, but the possibili-

ty of a mass injection of controlled amounts of conductive polymer is being investigated.

Having achieved a planar surface with what are effectively a series of conductive spots, the conductor writing can be carried out. Photo exposure of the sensitized surface by a digitally driven reflected light source and subsequent additive plating is potentially a rapid and accurate approach that can be used with multiple heads for volume production. However, the planar surface opens the way for other techniques, such as conductive polymer writing with a stylus or stitch wiring between pads. Production costs using both these techniques can be low, provided each layer is unidirectional and multiple heads are used. The next layer of dielectric is then applied and via formation continues as before. Some of the processes are suitable for building up on an etched, flexible access circuit bonded to the heat sink.

### Development

These and other approaches are currently being explored at Exacta, but until promising combinations have been proven in small-scale manufacture, it would be unwise to select one approach.

The specification outlined in this article will not cover every application, but systems house designers are currently facing interconnection and associated packaging problems the multistrata is designed to solve. The availability of a large-area surface-mounting substrate of the type described opens up new opportunities to designers. What is now required is a consensus on a specification and development by a printed-board or hybrid-unit fabricator in conjunction with forward-looking systems engineers. If this idea attracts interest, the 1980s may well be the time for a new interconnection technology. □

# How a 16-bit microprocessor makes it in an 8-bit world

External 8-bit bus feeds 16-bit architecture that boosts throughput and supports use of high-level languages

by Mitch GOOZÉ, *American Microsystems Inc., Santa Clara, Calif.*

□ Although 16-bit microprocessors are beginning to emerge, most peripheral devices have input/output requirements that are oriented toward 8-bit-wide data, and more chips of this kind continue to proliferate. A new microprocessor in the 6800 series resolves the conflict and, to top things off, succeeds in keeping software costs down, too.

The 6809's 8-bit external bus interfaces it with a wealth of peripheral chips. Its internal 16-bit bus soups up its processing powers. Its efficient execution of programs written in high-level languages and its relocatable firmware packages almost literally minimize the amount of microprocessor code that has to be generated—a huge asset when it is recalled that it takes a programmer a day to write 10 to 15 working, documented lines at a cost of \$10 per line.

The new device is totally compatible with 6800 microprocessor hardware and upwardly compatible with regard to software—that is, it executes 6800 source

code. Two versions are available: one has an internal oscillator that requires only a crystal to be connected between two pins, while the other (the 6809E) has an external clock driven by an external TTL-compatible clock source. For each version, 1 megahertz is the standard speed while the optional A series operates at 1.5 MHz and the B series at 2 MHz.

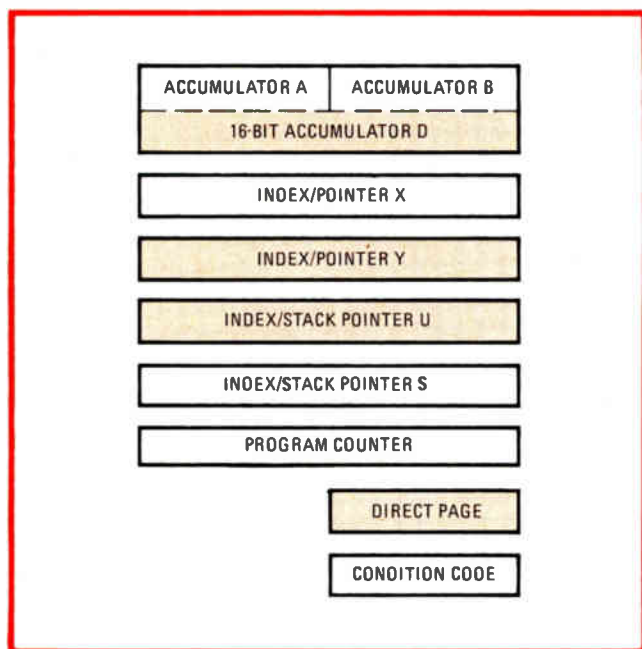
## A lower package count

Besides its software advantages over the 6800, the 6809 boasts several hardware improvements that reduce the amount of external logic needed to interface it with peripheral devices. Along with the 6800's signal lines for interrupt request (IRQ) and nonmaskable interrupt (NMI), the new microprocessor also incorporates a fast interrupt request line called FIRQ. This pin can be activated when it is known that the interrupting routine will be using the registers' existing contents, the goal being to waste no time on storing them unnecessarily elsewhere in memory. On receiving a FIRQ, the processor finishes executing its current instruction but then, rather than store all working registers, stores only the program counter and condition-code register on the stack. Control is then passed to the FIRQ interrupt-service routine, via a vector address.

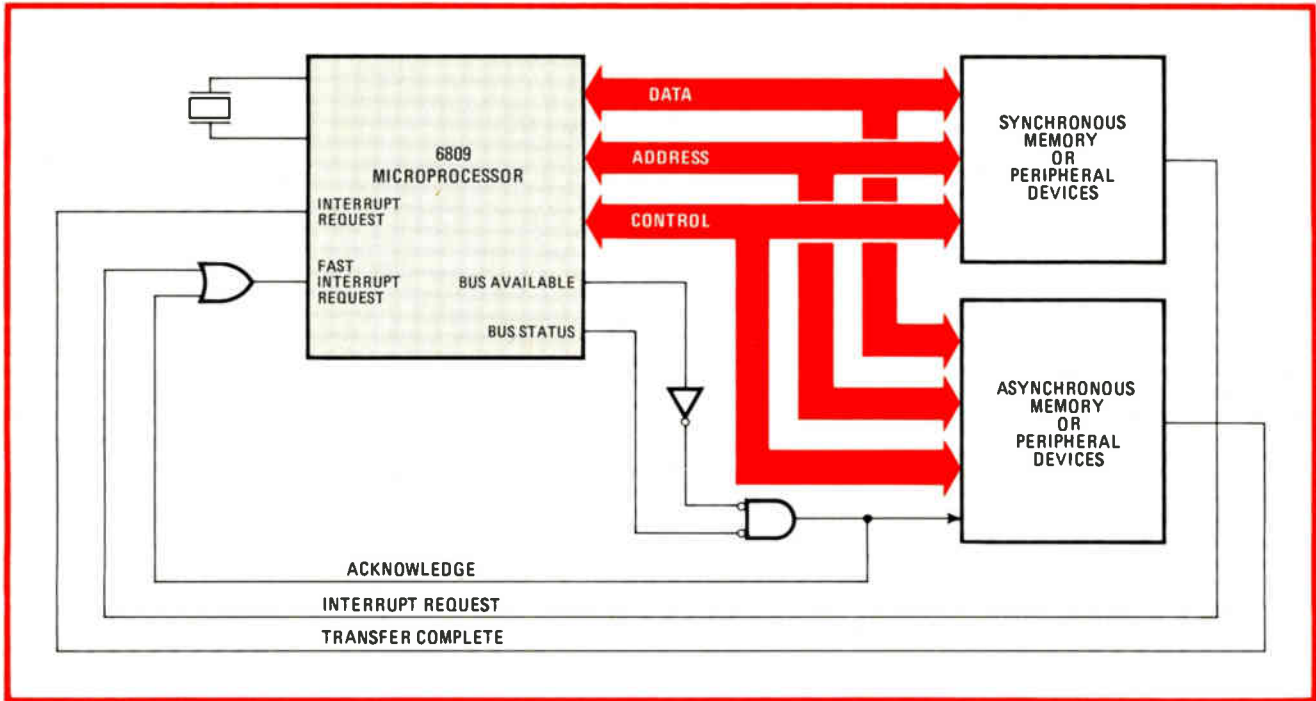
Another hardware enhancement is a memory-ready (MR) pin that stretches the duration of phase 2 of the clock up to 10 microseconds, to ease interfacing with slow memory devices. In addition, a processor-busy signal (BUSY) indicates when a read-modify-write cycle is in process—a useful feature in multiprocessor situations. Finally, a last-instruction-cycle (LIC) signal indicates that the 6809 is executing the last cycle of an instruction, alerting external devices that a new instruction will begin on the next clock cycle.

The 6809 also has more registers, more flexibly arranged, than the 6800, as Fig. 1 indicates. This enhancement not only speeds program execution because there is less data movement needed between registers and memory, but it also aids software development, since registers can easily be instructed to perform different functions at different times.

For instance, the 6809 has two 8-bit accumulators, A and B, like the 6800, but in addition can concatenate them to create a single 16-bit D accumulator for 16-bit logical and mathematical operations. Similarly, where



1. **Coding model.** The tinted registers are those common to the 6800 and the 6809. But the 6809 not only adds more registers—it also makes many of them multipurpose. The X and S registers, for example, can also function as pointers in the 6809.



**2. Interrupt sync.** The 6809 has features that allow it to easily synchronize interrupts with external components. When a sync instruction is executed, the device stops and waits for a request, which is fed back to it from synchronous or asynchronous peripheral chips.

the 6800 has a 16-bit index register (X), the 6809 has two such registers, X and Y, that will also function as pointers. Also, the 6800's 16-bit stack pointer has been replaced by two stack pointers, registers U and S, that can also be used for indexing purposes. Finally, the 6809 adds an 8-bit direct-page register for use with its direct addressing modes.

It should also be noted that the 6800 uses only 6 of the 8 bits in its condition-code register. In the 6809, one of the remaining bits is used as a FIRQ mask and the other as an internal flag to distinguish whether an IRQ or FIRQ was executed. This distinction is required to insure that the correct registers are restored at the end of an interrupt service routine.

It is this register setup in conjunction with a large number of addressing modes that makes it possible for compilers for the 6809 to generate efficient object code. So efficient is this code that it occupies hardly any more memory space than it would if the program had originally been written in assembly or machine language. In contrast, the Fortran, Cobol, and Pascal compilers available for many other microprocessors generate machine code that requires 50% to 100% more memory than code generated by hand—a penalty that often exceeds what the system designer can bear.

### Almost a score

The 6809, besides direct addressing, offers extended addressing, two modes of immediate addressing, and five modes of indexed addressing. It also has indirect versions of these extended, immediate, and indexed modes. That gives it a total of 19 addressing modes, in contrast to the 6800 microprocessor's 6.

With direct addressing, only the lower 8 address bits are incorporated into an instruction statement. The

upper 8 are generated by the direct-page register (DPR). After a reset, the direct-page register is cleared to zero and, if unmodified, the 6809's direct addressing will take effect and perform just like the 6800's—that is, it will reference page zero. However, as will be noted later, modification of the DPR is easily accomplished. Thus, memory accesses from anywhere in the memory map are achieved through 2-byte instructions.

If address locations outside of page zero must be referenced, the extended addressing mode can be used, in which case the instruction employs a 2-byte absolute address. Available for all of the memory-access instructions, this mode blankets the 6809's entire 64-kilobyte memory space.

### Immediate addressing

The 6809 has 8- and 16-bit immediate-addressing modes. Immediate addressing includes fixed data within an instruction statement—for example, the 8-bit value 01101110 (6E) to be loaded into a memory location or the A accumulator. Further, with the 6809, 16-bit values can be loaded into the D accumulator, any of the index registers, or two successive memory locations simply by referring to the first location.

The two modes of program-counter-relative direct addressing are offered by the 6809; byte-relative and 16-bit relative. Both modes can be used with any memory-access instruction. In PC-relative addressing, an offset is specified within the program statement. The offset carries a mathematical sign and is interpreted as relative to the value of the program counter at the time of execution. This eliminates the need for absolute addresses and allows true position-independent programs to be written without significant software overhead.

As noted, the 6809 has four index registers: X, Y, U,

## The 6809's instruction set

The 6809 microprocessor's instruction set is upwardly source-compatible with the 6800 set (and also the 6801 and 6802 sets).

Data-movement instructions are available in it to:

- Load and store any accumulator (A, B, or D) or any index register (X, Y, U, S).
- Transfer and exchange data between any two 8-bit registers (A, B, DP, or CC) or between any two 16-bit registers (D, X, Y, U, or S).
- Push or pull data onto S or U from any one register or more (X, Y, U, S, A, B, DP, CC, or PC).
- Load an effective address into X, Y, U, or S.

Logical instructions allow the user to:

- AND, OR, or EXCLUSIVE-OR the contents of any memory location with those of A or B.
- Shift and rotate the contents of any memory location with those of A or B.
- Complement, negate, and clear any memory location with those of A or B.
- AND and OR immediate data into the condition-code register.

With the arithmetic instructions, the user can:

- Add or subtract the contents of any memory location to or from A, B, or D.
- Add or subtract the contents of any memory location with carry to or from A or B.
- Add 8-bit immediate data to the contents of A, B, X, U, or S.
- Increment or decrement the contents of any memory location, any accumulator (A, B, D), or any index register (X, Y, U, S).
- Multiply A times B and put the result in D, at a 5- $\mu$ s execution time with a 2-MHz 6809.

Instructions for testing:

- Arithmetically compare the contents of any memory location with the contents of any accumulator (A, B, D) or any index register (X, Y, U, S).
- Logically compare the contents of any memory location with those of A or B.
- Perform 14 different branches (byte and 16-bit) on test conditions.

Finally, miscellaneous instructions allow direct jumps and jumps to subroutines, direct branches, branches to and from subroutines, and three software interrupts.

and S. Any of these registers can be used in any of the five indexed-addressing modes and on any memory-access instruction. In the standard indexed mode, the effective address is the contents of the selected index register; for example, EA equals IR, where IR denotes any index register (X, Y, U, or S). In the indexed-with-immediate-offset mode, the contents of the selected index register are modified by the addition of a 5-bit, 8-bit or 16-bit immediate value. The modified value is then used to address memory.

Similarly, in the indexed-with-register-offset mode, the contents of the selected index register are modified, but by the addition of one of the three accumulators (A, B, or D). This modified value is the selected address.

The indexed mode and the two post-increment-and-indexed and the two predecrement-and-indexed modes allow more than one instruction to effect the block transfer of data. The alternative—a dedicated block-move instruction—is limited to a single operation.

In the post-increment addressing modes, the effective address is the contents of the selected index register. After use, that register is automatically incremented by one or two. Similarly, in the predecrement addressing modes, the effective address is automatically decremented by one or two.

The 6809's indirect indexed addressing modes are virtually identical to its indexed addressing modes. In them, the contents of the selected index register points to a pair of addresses whose contents become the effective address. These indirect indexed addressing modes do not offer a 5-bit immediate offset option, however.

The other indirect addressing modes include PC-relative (byte and 16-bit) and extended indirect. With PC-relative indirect, the effective address is the contents of the address pair pointed to by the program counter plus an 8-bit or 16-bit immediate offset value specified in the instruction statement. The extended indirect mode

simply utilizes a 16-bit immediate offset specified in the instruction as an indirect pointer to an address pair whose contents become the effective address.

Additional operations to be performed with the X, Y, U, and S registers include the ability to push and pull data onto and off the U and S registers themselves. Any number of registers may be pushed or pulled with one instruction and, using the previously described indexed offset addressing mode, the programmer can obtain simplified access to data stacked several levels deep.

Mechanisms are provided in the 6809 to synchronize interrupts. For example, when an instruction to wait for interrupt is executed, all registers are stored on the S stack. Then, upon receiving a request to interrupt, the processor immediately jumps to the interrupt service routine, based on a vector value.

Execution of a synchronization instruction causes the processor to stop executing code and wait for the next interrupt request. If the interrupt is masked, the processor will start executing code again. If the interrupt is not masked, then it will be acted upon as a normal interrupt. This allows an external asynchronous device to be synchronized with the processor. A typical system implementation is shown in Fig. 2.

### Instructions galore

Add to this multiplicity of registers and addressing modes a large instruction set (see "The 6809's instruction set"), and the 6809's software advantages can now be understood more completely. The 6809 promotes the use of modern software techniques, such as position-independent, modular, and re-entrant programs, as well as programs written in high-level languages that have not been economically attractive for microprocessor coding because they added too much to the software overhead on some machines.

Position-independent programs execute properly, re-

TABLE 1: 6809 SOFTWARE BENCHMARKS WITH NORMALIZED DATA

Operation	6809	Z80	6800	8080/8085
Insertion sort	1.00 / 1.00 / - / - *	—	1.61 / 1.54 / - / -	—
Floating-point package	1.00 / 1.00 / - / -	—	1.35 / 1.20 / - / -	—
Substring search	1.00 / 1.00 / 1.00 / 2.00	1.75 / 1.59 / 1.74 / 2.78	2.00 / 2.08 / 2.00 / 4.00	2.22 / 2.13 / 3.10 / 4.66
Move block	1.00 / 1.00 / 1.00 / 2.00	1.00 / 1.11 / .97 / 1.56	2.78 / 1.89 / 3.56 / 7.10	2.27 / 1.59 / 2.35 / 3.54
3-byte multiply	1.00 / 1.00 / 1.00 / 2.00	2.50 / 1.61 / 5.69 / 9.10	1.69 / 2.27 / 6.25 / 12.50	3.23 / 2.13 / 12.09 / 18.18
Interrupt data transfer	1.00 / 1.00 / 1.00 / 2.00	1.00 / .64 / .75 / 1.20	.86 / .78 / 1.00 / 2.00	1.48 / 1.36 / 1.94 / 2.92
High-level language primitives (data manipulation)	- / 1.00 / 1.00 / 2.00	- / 7.56 / 1.92 / 3.08	- / 1.61 / 1.67 / 3.34	—
High-level language program	- / 1.00 / 1.00 / 2.00	- / 1.33 / 2.31 / 3.70	- / 1.25 / 1.56 / 3.12	—
Performance score	1.00 / 1.00 / 1.00 / 2.00	1.56 / 1.31 / 2.23 / 3.57	1.72 / 1.58 / 2.67 / 5.34	2.30 / 1.80 / 4.87 / 7.32

\* Format: number of instructions / number of bytes / execution time with a fast clock / execution time with a slower clock

ardless of location in the processor address space. They do not use absolute addresses; for example, hexadecimal addresses such as 4000<sub>16</sub> or 03FC<sub>16</sub> are not assigned to particular software steps. This eliminates the need for a relocating loader and allows identical programs to be used in many different systems. Also, since absolute addresses are not assigned, specific read-only-memory-address decoding need not be a problem. The 6809 allows efficient implementation of position-independent programs through its 8- and 16-bit PC-relative branch and memory-access instructions and through flexible stack storage hardware techniques.

**Modular programming**

Another modern technique allows programs to be easily divided into small manageable modules. The ability to write modular programs, as they are called, lets the microprocessor software designer use a top-down approach to programming. Thus, programmers with a thorough knowledge of the system's requirements can divide the project up and design these modules independently as well as test each module thoroughly on a stand-alone basis. The ability to effectively exploit a modular approach requires flexible access to parameters on a stack or on multiple stacks, which the 6809 has the ability to manipulate.

The ease of software development that the 6809 provides helps to hold down software risk. Although the costs associated with the software design task are amortized over the number of systems actually built, the cost of software errors that occur in the field is not. Since software is inherently less testable than hardware, additional effort must be expended to insure its reliability. The ability of the 6809 microprocessor to make use of modular programming allows more thorough testing of these independent software modules prior to their incorporation in the final system.

Re-entrant programs contain software routines that can be called by interrupt and noninterrupt programs without destroying data. By using the same software routines for independent processes and for different priorities of the same process, such programs use program memory and less programming time. This technique

TABLE 2: SUMMARIZED BENCHMARK PERFORMANCE OF THE 6809

Performance criteria	6809	Z80	6800	8080/8085
Number of instructions	1.00	1.56	1.72	2.30
Number of bytes	1.00	1.31	1.58	1.80
Execution time with a fast clock (μs)	1.00 (2 MHz)	2.3 (4 MHz)	2.67 (2 MHz)	4.87 (3 MHz)
Execution time with a slower clock (μs)	2.00 (1 MHz)	3.57 (2.5 MHz)	5.34 (1 MHz)	7.32 (2 MHz)

requires stack indexing and convenient stack manipulation, and the 6809 microprocessor excels in both.

Tables 1 and 2 summarize software benchmarks for the 6809. These benchmarks were produced with an eye toward evaluating the design and not as a promotional tool. Table 1 includes the results of several individual types of instructions, including those for sorting and searching, block moves and interrupt data transfer, floating-point math and 3-byte multiplication, and high-level language support.

**Comparative merits**

Three criteria were measured. The first was the number of instructions required to perform the function, which in turn are a measure of the programmer's effort. The second was the number of bytes, which measures the memory needed, and the last the throughput at two clock rates. All the data is normalized to 1.00 for a 2-MHz 6809. Any numbers that are greater than 1.00 indicate poorer performance.

Table 2 summarizes the results. Compared to the 6800, the 6809 affords a 72% decrease in number of instructions required, a 58% decrease in program memory, and a 167% increase in throughput. Thus, the 6809 allows the system designer not only greater flexibility and increased reliability of design, but also greater programming ease and increased system throughput. □

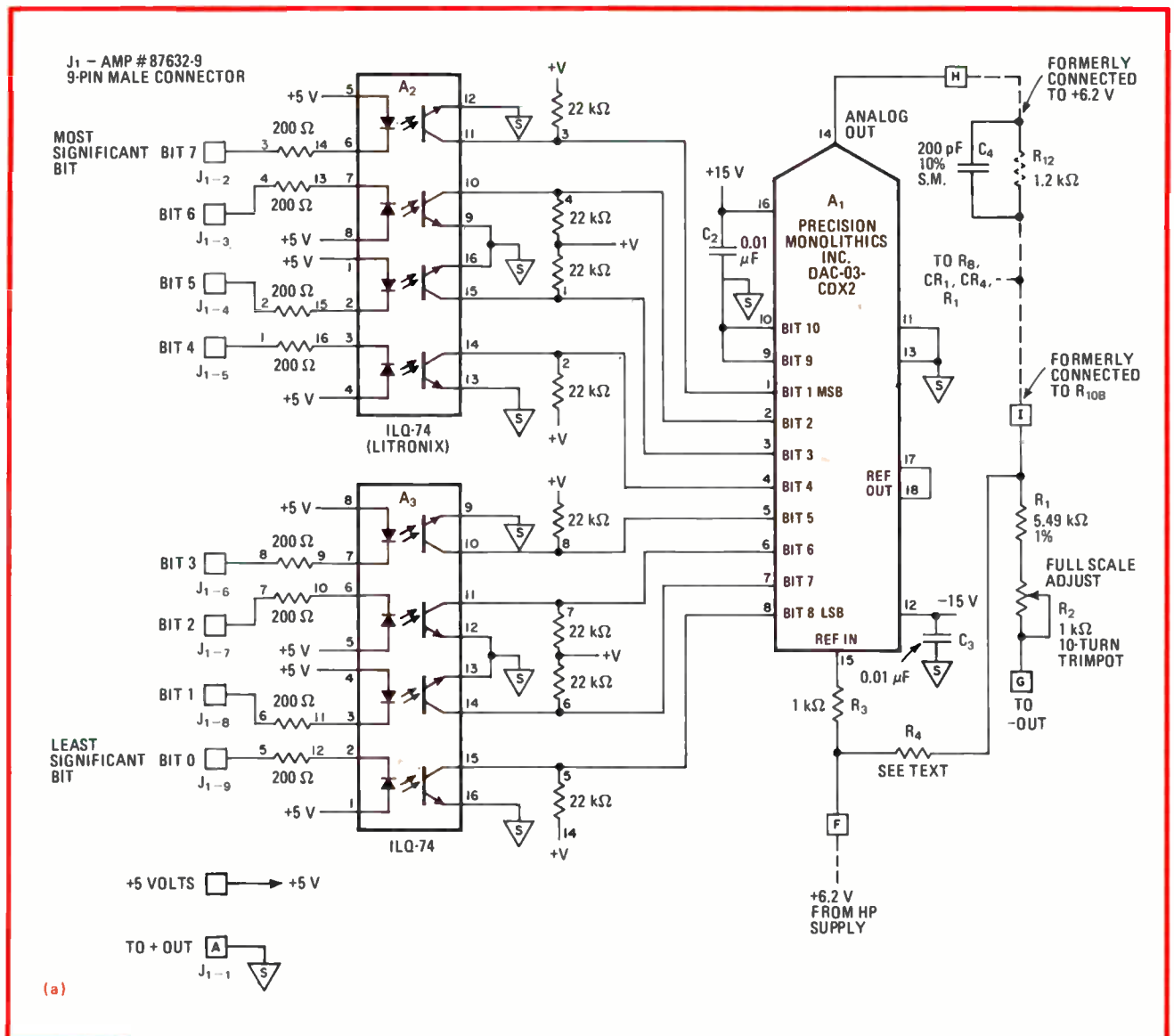
## Modifying a power supply to add programmability

by Eric Kushnick  
Bose Corp., Framington, Mass.

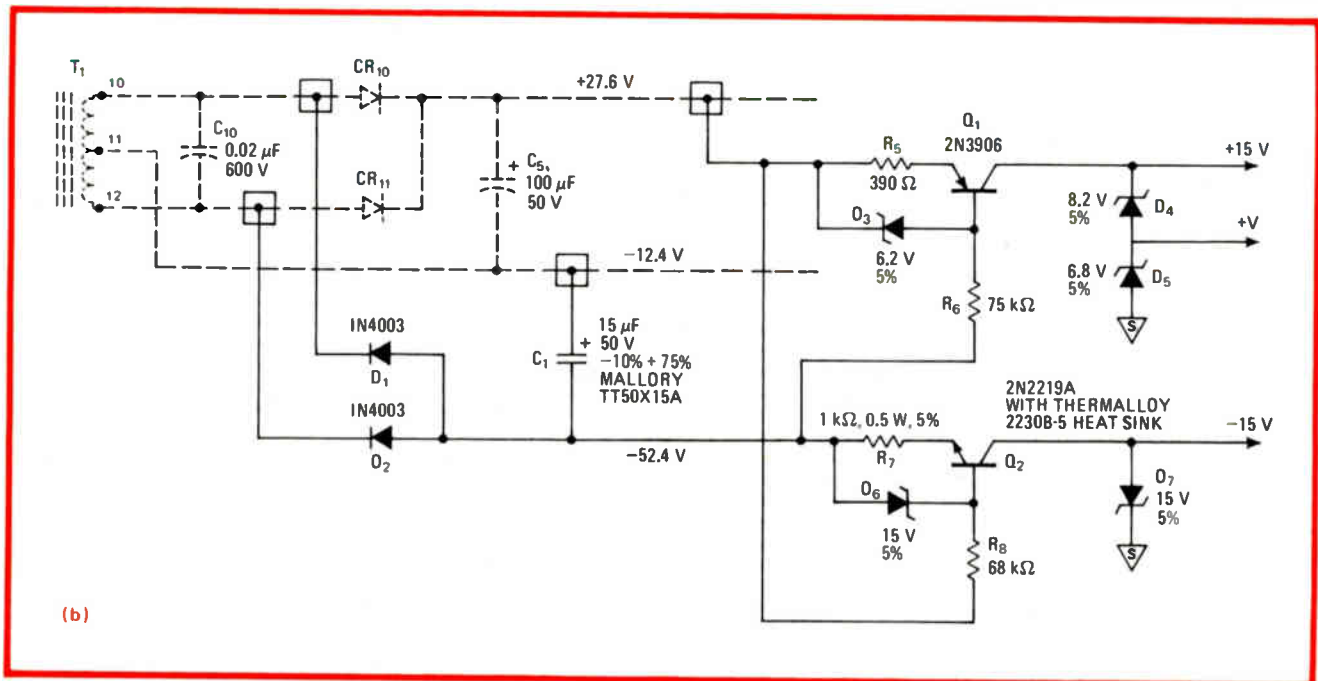
Modifying the commercial bench-type supply is a simple but effective and low-cost solution to the problem of obtaining a programmable power source if the supply's response time is not a primary consideration. Here, members of the popular Hewlett-Packard series

(6212A-6218A) are converted by adding opto-isolators and a digital-to-analog converter to their basic circuits so that 8-bit programming capability is achieved. The modification may be completed for less than \$50.

The initial changes required are shown in (a), and they are fairly straightforward. The 6.2-volt reference from the supply is disconnected from one end of  $R_{12}$  and reconnected to the analog input of  $A_1$ , the Precision Monolithics DAC-03-CDX2 d-a converter.  $C_4$  is then mounted directly across  $R_{12}$ . The analog output of the converter is reconnected in place of the 6.2-v reference and the supply's front-panel potentiometer,  $R_{10}$ , previously used for coarse-voltage adjustment, is replaced by the  $R_1$ - $R_2$ - $R_4$  combination. The digital



**Bits of voltage.** Adding digital-to-analog converter and optocouplers (a) to bench supply gives the source 8-bit programming capability. Separate power tap (b) for energizing converter is required to eliminate interaction with supply's regulator (not shown).



programming inputs to the converter are isolated from the power supply by  $A_2$  and  $A_3$ , the Litronix ILQ-74 optocouplers.

Additions to the section in the reference regulator (not shown) that derives the supply's internal voltages must be made next, as shown in (b), so that the converter can be powered. Note that the components within the dotted line show the standard configuration of the HP supply (this part of the circuit is not modified).

Here, the converter is powered through the circuitry surrounding  $Q_1$  and  $Q_2$ . Note that none of the regulator's current can flow into the s terminals, so that regulator operation, which depends on a complex balance of currents to maintain a given output voltage, is not disturbed.  $C_1$  must be in the range of 10 to 30 microfarads to prevent turn-on and turn-off transients from

reaching the output of the supply.

The added circuitry can be placed on a printed-circuit board and mounted inside the supply with a small metal bracket bolted to the transformer's mounting screws. As for circuit details, all resistors are 1/4-watt carbon-film devices and all capacitors are ceramic-disk types, rated at 25 v, unless otherwise specified. All 200-ohm resistors are contained within a resistor network (Sprague 916C201X5SR). Similarly, the 22-kilohm resistors are contained within the Sprague 914C223X5PE network.

The calibration of the supply is simple. First  $R_4$  is adjusted for a minimum offset voltage at 0 v, and then  $R_2$  is set for a full-scale output voltage of 29.88 v. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.

## Low-cost m<sup>2</sup>fm decoder reduces floppy bit-shift

by Vikram Karmarkar  
Hindustan Computers Ltd., New Delhi, India

Like mfm, dual-density m<sup>2</sup>fm information from a floppy disk may not fall at its nominal position in data cells because variations in disk speed cause the bits to shift, thus reducing the cells' data margin and causing errors in the system's decoding circuitry. Using a hardware

implementation of an algorithm that predicts whether the data will fall early, at the center, or late in any particular cell, this circuit adjusts the data-to-clock ratio to 1:1 or 3:2 (50 milliseconds to 50 ms, or 60 ms to 40 ms) as required, so that the data can be recovered.

The difference between single-density (fm, or frequency-modulated) and double-density (mfm, or modified fm) recording methods was summarized in two recent articles<sup>1,2</sup>. M<sup>2</sup>fm resembles mfm in that it, too, provides a way to encode double-density data. But being encoded at a lower bit rate, it has inherently better tolerance to bit shift. A high-resolution recording head is not required, as in mfm. Further, fm systems can be upgraded to m<sup>2</sup>fm encoders without the need to change disk drives.

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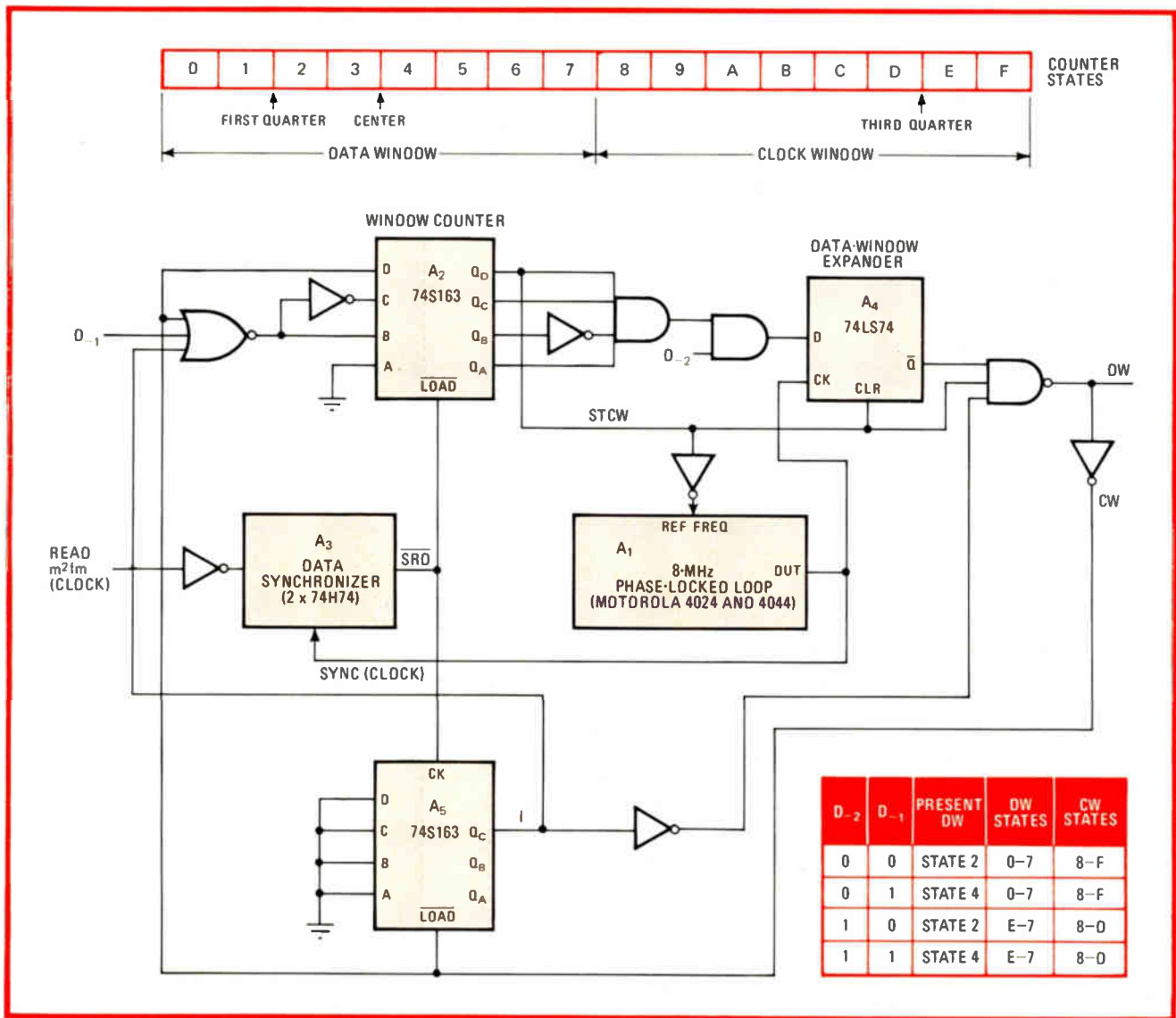
\*U.S. Prices only

# Signal generator users just got lucky.



For demonstration circle 128  
For literature circle 129





**Guess when.** Decoder for double-density floppy determines where to place receiving window for recovering  $m^2fm$  data, based on flux transitions of two previous data bits that can cause resultant shifts in position. Circuit adjusts data-to-clock ratio at 1:1 or 3:2 for each cell as required to recover data, compensates for bits removed  $\pm 250$  ms from their ideal position.

The typical  $m^2fm$  cell has 16 states (see figure, top), 8 of which comprise the data window and the remaining 8 the clock window. The algorithm for decoding the data:

- Applies each system clock pulse to the center of the clock window.
- Initializes the data window at the first-quarter point in the cycle at the arrival of a data pulse if the previous data bit,  $D_{-1}$ , equals 0. The data window is centered if  $D_{-1} = 1$ .
- Initializes the data window at the third-quarter point in the clock window for the current data bit if the second previous data bit,  $D_{-2}$ , equals 0.

An acid test for this algorithm is the handling of the mark bytes found in the data stream, since these bytes do not fit into the  $m^2fm$  clock pattern. The hardware used to decode the data will process the data, the ID address, and selected data markers with no problem, while maintaining the system margin.

The circuit used to achieve the decoding is shown in

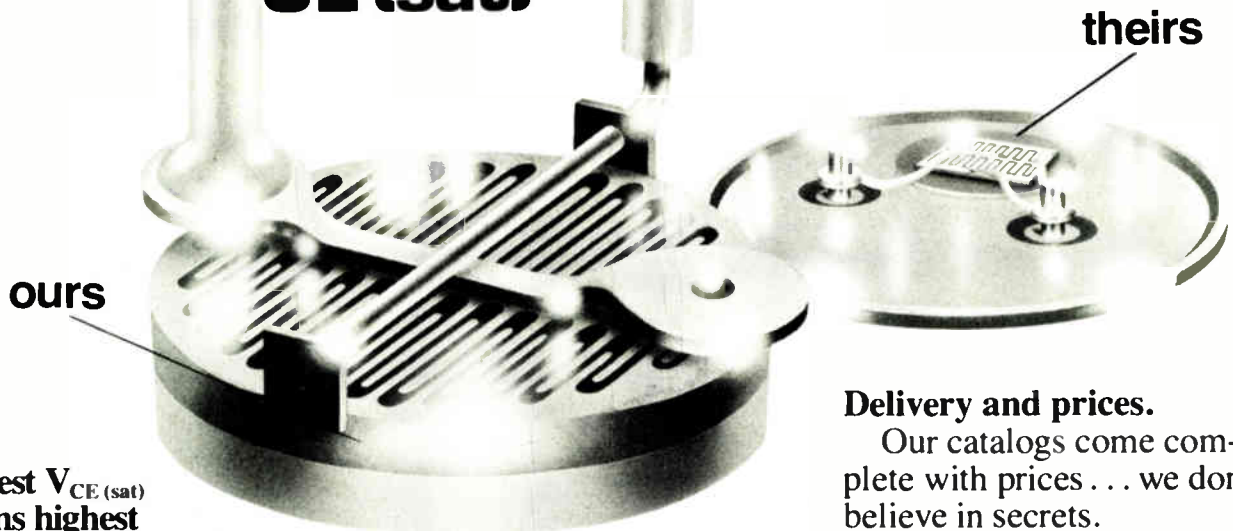
the main part of the figure.  $A_1$  generates a center frequency of 8 megahertz for the modulo-16 window counter,  $A_2$ , thereby providing cells of 125 ms in width. States 0 through 7 constitute the nominal (50-to-50-ms) data window, and states 8 to F the clock window. Note the PPL can be replaced by a fixed-frequency (crystal) oscillator with no degradation in circuit performance if little additional drive current is required.

Any clock pulse appearing at the read  $m^2fm$  input presets  $A_2$  to state 2 or 4, respectively, as governed by the truth table.  $A_4$  converts the data-to-clock ratio to 60:40 when necessary. Thus it is seen that the circuit can handle a bit tolerance of  $\pm 250$  ms in position. Inversion counter  $A_5$  places the clock and data pulses into their corresponding windows. □

**References**

1. Curt Terwilliger, "Pattern generator simulates double-density floppy," *Electronics*, Sept. 13, 1979, p. 131.
2. John G. Posa, "Peripheral chips shift microprocessor systems into high gear," *Electronics*, Aug. 16, 1979, p. 93.

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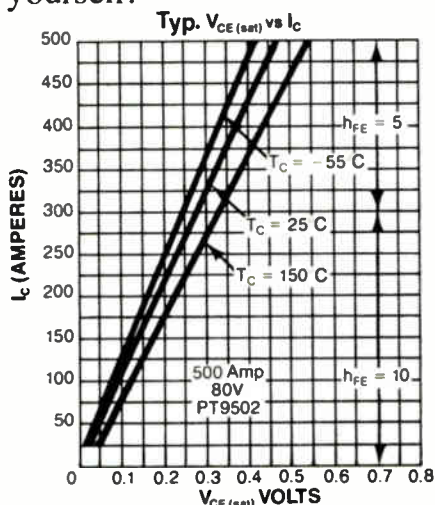
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# Polysilicon-load RAMs plug into mainframes or microprocessors

The Poly R process builds a dense 8-K MOS static random-access memory; Scaled Poly 5 boosts its speed to a bipolar level

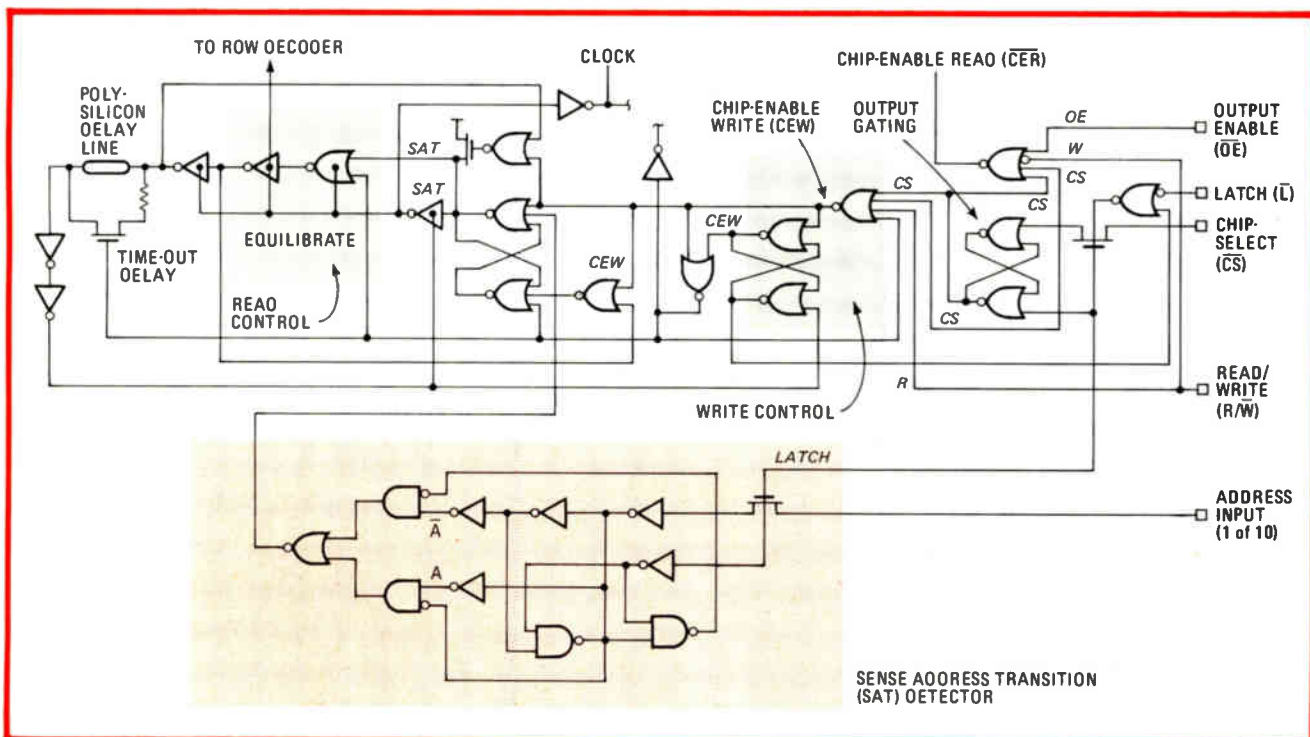
by David Huffman, *Mostek Corp., Carrollton, Texas*

□ The past decade has witnessed a truly phenomenal growth in the number of MOS random-access memory types, with corresponding improvements in speeds and densities. But most of the emphasis has been on designs for mainframe computer memory. The chips in that type of memory are best organized in a bit-wide fashion (as in a 4-K-by-1-bit device) and must be inexpensive on a per-bit basis. But microprocessors have different requirements, and there the 8-bit-, or byte-wide, chip organization has proved the most efficient. Today's generation of MOS microprocessors are high-performance, multifunctional, easy to use, and low-

cost—and the memory designed for them has to have the same features.

At the same time, MOS performance has improved to a point where an MOS RAM can fill many of the high-speed applications for which bipolar memories alone were once suitable: buffer and cache memories and writable control stores are examples. The question now is, can one memory suit both the microprocessor and the fast mainframe applications?

Enter the MK4118 and MK4801, a pair of 1,024-by-8-bit static RAMs that run that gamut of applications from microprocessor to mainframe. The devices have the



**1. Transition sensor.** Key to Mostek's MK4118 and MK4801 1-K-by-8-bit static RAMs is Address-Activated operation. A sense address transition circuit on each address line detects rising and falling edges to initiate the sequence of internal clocked peripheral circuits.

same functions and 24-pin packaging, but differ in processing and speed (see "Concepts for a dense new RAM"). The 4118 is built with Mostek's Poly R process and meets microprocessor speed requirements with its 120-to-250-nanosecond access times; the 4801, on the other hand, uses the new Scaled Poly 5 process to achieve 55-to-90-ns accesses offering a lower-power, higher-density alternative to the current generation of bipolar RAMs, such as the 4-K-by-1-bit 93471 from Fairchild Camera and Instrument Corp.

The design of a flexible RAM had to take the needs of control, power-down, and timing into account. A technique first used by Mostek in its 1-K-by-4-bit MK4104

static RAM was a clocked, or dynamic, control periphery, similar to that used in dynamic RAMs. Although the technique reduced power consumption, the RAM required an external chip-enable pulse to initiate the internal timing sequences. A different approach is used by Intel Corp. in designing the fully static 1-K-by-4-bit 2148, which instead relies on its chip-select input to turn off some of the internal circuits, thereby power-gating the device.

### Power-down approaches

Both approaches, however, place certain restrictions on signal timing, such as minimum precharge or active time for the chip-enable or chip-select inputs. Indeed, the 4104 will not read or write at all unless its chip-enable input ( $\overline{CE}$ ) sees a signal with a falling edge. But the 4104 was unique in that it contained circuits to detect such an edge—called edge activation—and start the internal sequence of events. The advantage was clear:

## Concepts for a dense new RAM

In 1976, Mostek introduced its Poly R process with the MK4104, a 4-K-by-1-bit static RAM. The part diverged from the usual static RAM designs in that it replaced the depletion-mode MOS transistor loads in its cell with ion-implanted polysilicon resistors (figure a below). The design not only saved chip area but also greatly lowered power dissipation. Since the polysilicon resistors are actually laid over the four transistors, the cell of the 4104 shrank to 2.75 mil<sup>2</sup>—roughly half the size of conventional cells.

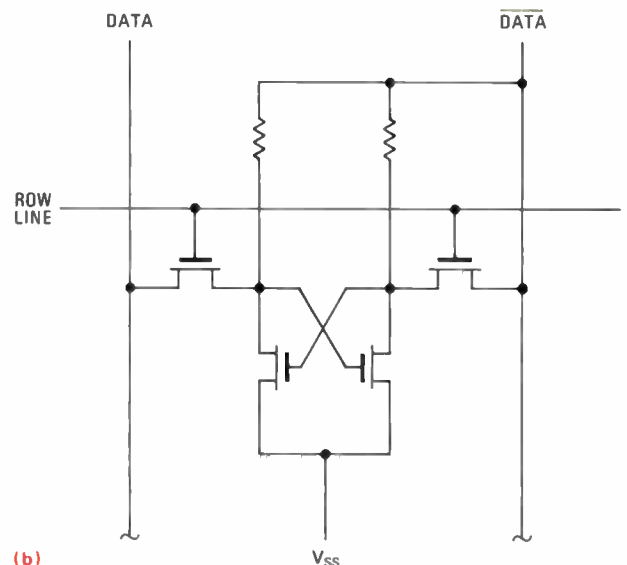
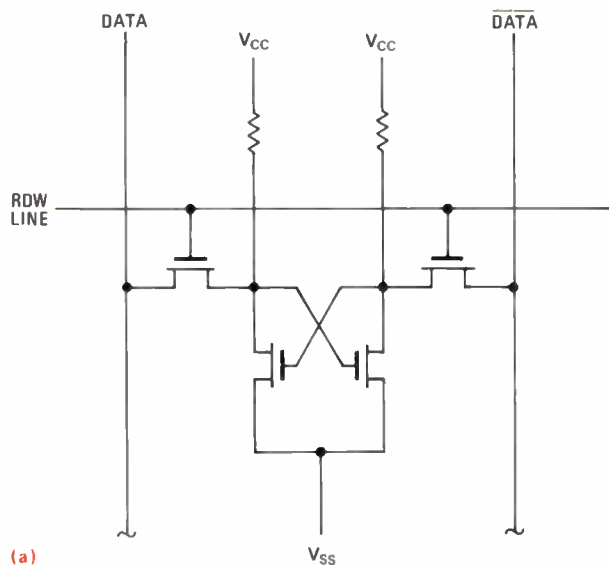
The power is reduced because the high resistivity of the polysilicon loads—typically, 5,000 megohms, accurately controlled by ion implantation—squeezes the current flow down to less than 1 nanoampere per bit. Another feature of the Poly R loads is their negative temperature coefficient, which automatically compensates for increased leakages that normally occur at elevated temperatures. Moreover, the polysilicon loads allow data retention in the cells even at greatly reduced supply voltages.

Both the 4118 and 4801 utilize the polysilicon-load

concept, with one basic difference. Rather than connecting the load resistors to the positive supply ( $V_{cc}$ ), as in the 4104, the 8-K statics tie both resistors to one of the two data lines, depending on which side of the chip the cell lies, as shown in figure b. Thus, power is fed to the cells via the column lines through the polysilicon load resistors. The key advantage of this arrangement is the elimination of the  $V_{cc}$  contact in the cell and the metal interconnection it required. Using that technique, the 2.75-mil<sup>2</sup> cell of the 4104 drops to 2.0 mil<sup>2</sup> in the 4118. Not only is the cell size reduced by tying the loads to the data line, but furthermore the low power and self-compensation advantages of the 4104 are carried through to the 4118, which packs 8-K bits onto a 27,000-mil<sup>2</sup> chip.

**Now scaling.** The 4801 is the first part to use Mostek's Scaled Poly 5 process, which further reduces the 2.0-mil<sup>2</sup> cell of the 4118 to 1.3 mil<sup>2</sup>. The process is Mostek's answer to what will be required for the next generation of products.

Scaling down refers to reducing all physical dimensions



reduced power in both the active and standby modes, just as in a dynamic RAM.

The 4118 and 4801 take the edge-activated concept a step further by eliminating the need for an external clock. That is accomplished by a circuit that can sense a transition, whether high- or low-going. With such a circuit on each of the chips' 10 address lines, the 4118 and 4801 can each generate its own clock pulse to start the internal timing, based on a change on any of those address lines.

The sensing circuit in the address buffers that generates the pulse is called a sense-address-transition (or SAT) detector (Fig. 1). The address buffer is, in effect, connected to the control periphery; the negative edge of the SAT pulse, which occurs at any address transition, starts the internal cycle.

The 4118 and 4801 thus have the advantage of clocked periphery—low power—without the restrictions of an external clock requirement. This feature is called

Address-Activated operation, and it is totally transparent to the user.

In addition to the SAT detector circuit, the 4118 and 4801 have other circuits designed to cut power dissipation. Tree decoders and clocked sense amplifiers are other examples. The decoders draw only leakage current in any stable state of chip operation; power is drawn only during transitions.

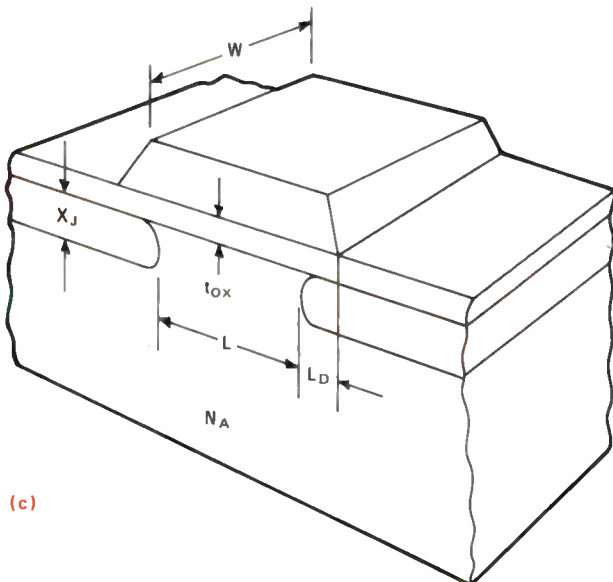
### Automatic power-down

Another example of low-power design is the chips' automatic power-down feature. Unlike the 2148, which powers down only when its chip-select input ( $\overline{CS}$ ) is brought high, the 4118 and 4801 automatically reduce power to a standby mode once data is latched, as an internal clock shuts off power to the decoders and to the clocked sense amplifiers. The reduction in power dissipation is about 30%; although other power-down RAMs may offer a greater reduction, the 4118 and 4801 devices

both horizontally and vertically, as well as reducing the operating voltage. It is not to be confused with shrinking, which simply reduces the critical spacings and the number of elements, say, in a cell; the result is a squeezing together of the circuitry. Scaling down reduces actual design dimensions, plus certain operating characteristics, including voltage power, signal level, and so on.

Below are shown a cross section of a typical MOS transistor and some of the critical dimensions that determine the operating parameters. Thanks to new lithography techniques, the old 5-micrometer dimensions are no longer necessary. Also, since the new 5-volt-only parts reduce the operating voltage (from the 12-V level), oxide thicknesses can also be reduced.

In theory, all parameters can be reduced by a constant—5/12 is a good starting point, since the operating voltage is scaled from 12 to 5 V. This brute-force technique, however, is not necessarily the most efficient and must be modified somewhat. Table 1 shows both the brute-force and modified approaches.



(c)

The differences between the two approaches are there to enhance not only performance but manufacturability and reliability as well. Look, for example, at substrate resistivity. The brute-force technique would reduce it from 10 to 6 ohm-centimeters. The result of that, however, would be high junction capacitance and higher effective threshold voltage due to the body effect. Moreover, manufacturing tolerances also come into play.

Scaled Poly aims also at improving overall device reliability. Table 2 shows the changes in reliability when scaling down by a factor of K. The important one to note is power dissipation. It is a well-proven fact that the lower the power dissipation, the better the inherent device reliability. Current density increases, but there is no net effect on overall reliability because the previous design and process rules were overly conservative.

A final factor in scaling is the type of equipment required to manufacture a device. Scaled Poly 5 can be manufactured with existing equipment and technology—no new equipment is required for current products.

TABLE 1: COMPARING METHODS OF DEVICE SCALING

Device parameter	Standard n-MOS	Brute force	Scaled Poly 5
Channel length, L ( $\mu\text{m}$ )	5	2.1	2.5
Oxide thickness, $t_{OX}$ ( $\text{\AA}$ )	850	354	500
Substrate resistivity ( $\Omega\text{-cm}$ )	10	6	30
Power supply voltage (V)	12	5	5
Junction depth, $X_J$ ( $\mu\text{m}$ )	1.2	0.45	0.4
Lateral diffusion, $L_D$ ( $\mu\text{m}$ )	1.0	0.41	0.3

TABLE 2: MOS DEVICE PARAMETER CHANGES DUE TO SCALING

Parameter	Variation
Field strength	1 $\leftrightarrow$
Power per unit area	1 $\leftrightarrow$
Current density	1/K $\uparrow$
Device power	$K^2 \downarrow$
Device voltage	$K \downarrow$
Power-delay product	$K^3 \downarrow$

pay no timing penalties for their use of this feature.

The 1-K-by-8-bit RAMs also feature a latch function. An active-low input, the latch ( $\bar{L}$ ) causes the address information to enter the device, eliminating the usual external latch chips needed in schemes with a common address and data bus. Taking  $\bar{L}$  low initiates two basic operations: it first isolates the address line from the SAT detector, then delivers the addresses to the on-chip latches, which are part of the SAT circuit. These same events occur when the chips are put in the write mode (the write-enable input,  $\bar{WE}$ , is driven low): referring to Fig. 1, the state of the chip-enable-write (CEW) flip-flop changes, in turn changing the  $\phi_1$  flip-flop, which again isolates the SAT detector from the address lines.

Address data must be stabilized at the time either the latch or the write-enable lines are driven low. When writing data, the cycle will not be terminated until the clock signal has propagated through the polysilicon delay line; once through, the clock signal changes the state of the CEW flip-flop and thus reconnects the address line to the SAT detector. In a latched-read cycle, however, the address will not reconnect to the SAT detector until the latch input  $\bar{L}$  returns high.

### Special pump

Both the 4118 and 4801 rely on a substrate-bias generator (or charge pump) to supply the substrate with a negative voltage, which reduces junction capacitance and lowers the body effect in the MOS devices. The charge pump supplies  $-9$  volts with more than enough drive to compensate for leakage currents in the chips. A unique feature of the bias generator in the 4118 and

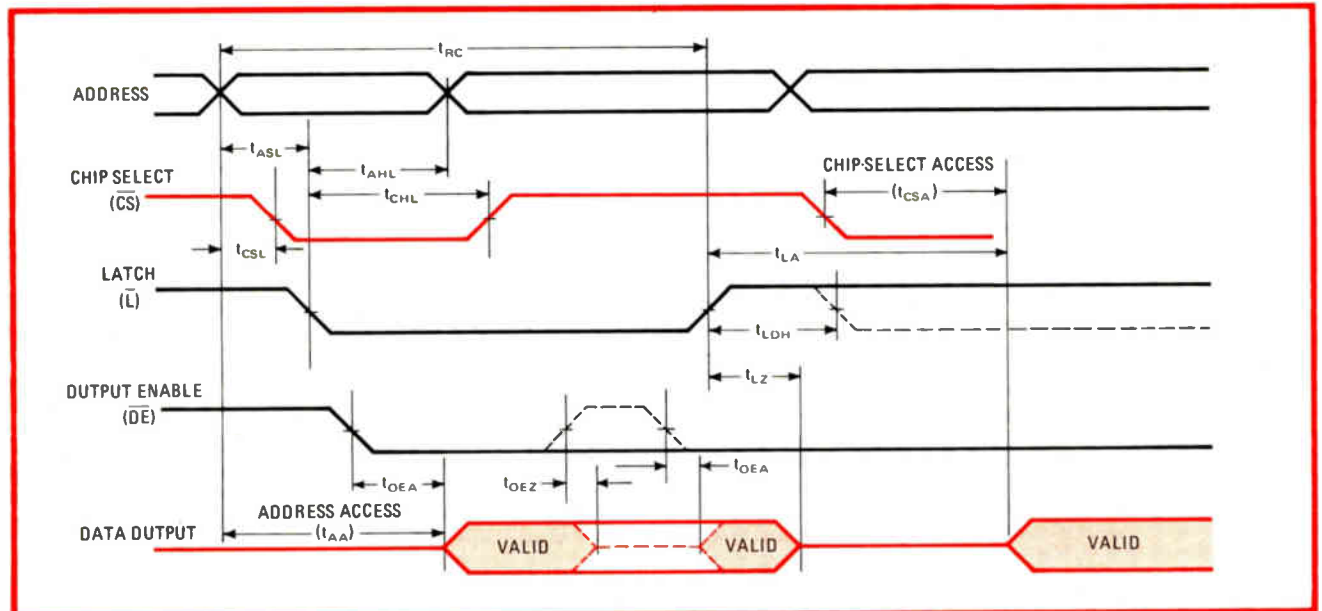
4801, however, is that it pumps at all times, either more negative or more positive. Most other substrate-bias generators pump only a negative bias; they rely on substrate current to pull the bias more positive, and that means a slower response to any fluctuations that may occur in substrate voltage.

### Using the RAMs

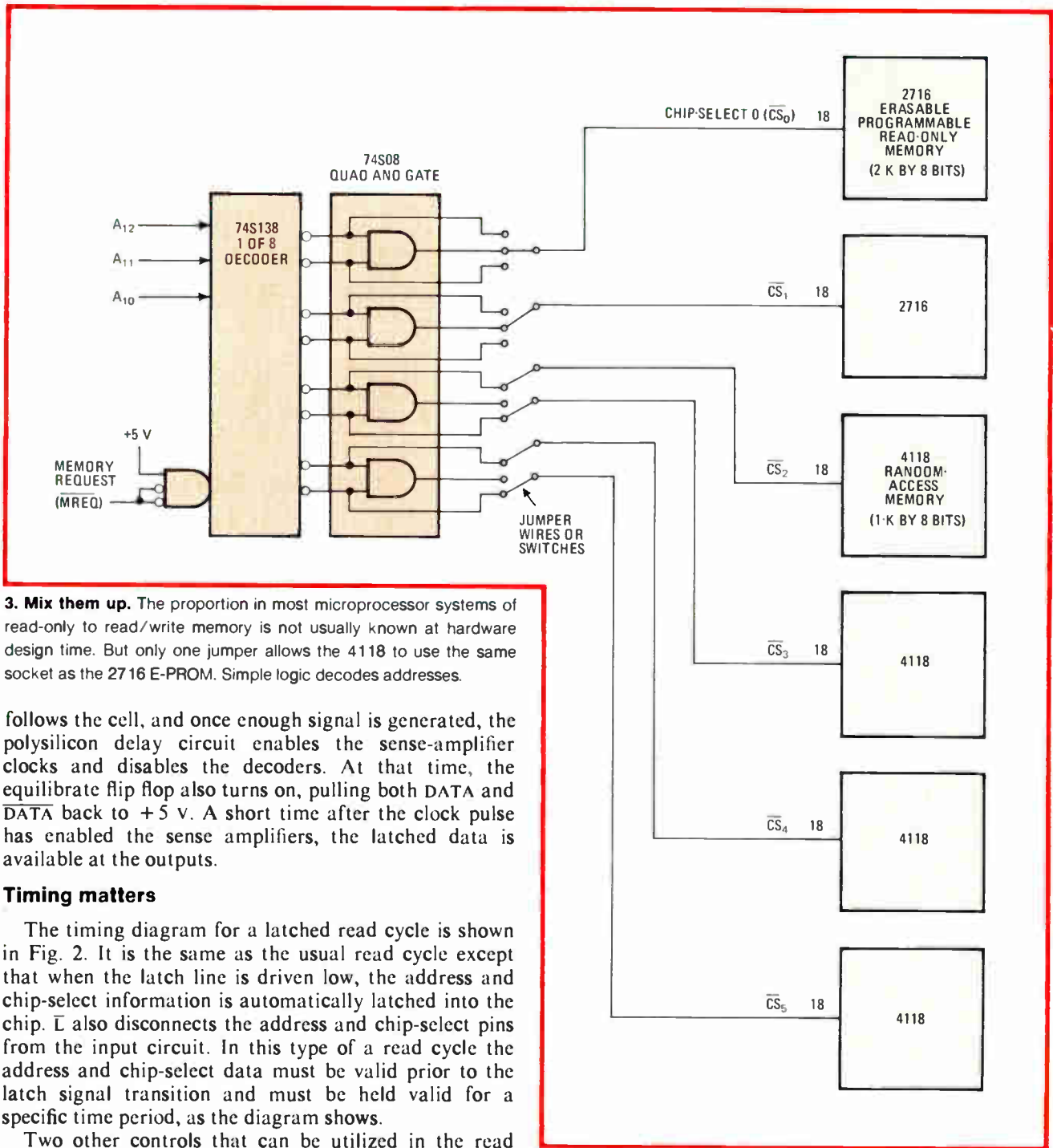
As in nonclocked (fully static) RAMs, any change on the address lines will cause new data to be accessed in the 4118 and 4801 RAMs. In an unlatched read cycle ( $\bar{WE}$  is high), where the chip-select ( $\bar{CS}$ ) and output-enable ( $\bar{OE}$ ) lines are low, the last address transition to occur generates the SAT pulse, which starts the internal timing sequence; any cycles previously started by an early address transition are aborted by the last transition. Again referring to Fig. 1, the SAT pulse disables the equilibrate function and enables the fetch function, thus powering up the row decoders and initiating the time-out polysilicon-delay circuit.

Before a bit cell is read, the equilibrate signal's function is to hold the complementary DATA and  $\bar{DATA}$  lines of the cell to  $+5$  v. When this signal is disabled, the complementary lines float at  $+5$  v. It is only when a particular cell is accessed that one of the two data lines is pulled to ground.

If a low signal is stored on the side of the cell not supplying power to the load resistors, the data line supplying power remains near 5 v. But though it would appear detrimental that the line supplying power to the cell should be pulled to ground, the timing of the 4118 and 4801 is such that an adequate differential signal is generated between the DATA and  $\bar{DATA}$  lines long before the low-going line can be pulled low enough to cause the voltage on that line to drop below the value required to maintain data in the column of cells to which it connects. That 200-to-300-millivolt difference between DATA and  $\bar{DATA}$  is amplified by the differential amplifier that



2. Latched read. The 4118 and 4801 have built in latches that are handy in multiplexed-bus systems. A latched-read cycle (write-enable,  $\bar{WE}$ , high) is performed by taking latch input ( $\bar{L}$ ) low, which latches address and chip-select inputs and supplies data to the output drivers.



**3. Mix them up.** The proportion in most microprocessor systems of read-only to read/write memory is not usually known at hardware design time. But only one jumper allows the 4118 to use the same socket as the 2716 E-PROM. Simple logic decodes addresses.

follows the cell, and once enough signal is generated, the polysilicon delay circuit enables the sense-amplifier clocks and disables the decoders. At that time, the equilibrate flip flop also turns on, pulling both DATA and  $\overline{\text{DATA}}$  back to +5 V. A short time after the clock pulse has enabled the sense amplifiers, the latched data is available at the outputs.

**Timing matters**

The timing diagram for a latched read cycle is shown in Fig. 2. It is the same as the usual read cycle except that when the latch line is driven low, the address and chip-select information is automatically latched into the chip.  $\overline{\text{L}}$  also disconnects the address and chip-select pins from the input circuit. In this type of a read cycle the address and chip-select data must be valid prior to the latch signal transition and must be held valid for a specific time period, as the diagram shows.

Two other controls that can be utilized in the read cycle are the chip-select and output-enable inputs. If those inputs are not taken valid during the cycle, the output buffers will not be enabled. The chip, however, will go ahead and access data from its cells for presenting to the output buffers. Because of that, both the 4118 and 4801 have a fast access time as measured from output enable or chip select—50% that of the normal address access time.

The write cycle is slightly more complicated than the read cycle. The write-enable line going low has the same effect on addresses as  $\overline{\text{L}}$  going low: both addresses and the chip-select are latched. Both of these therefore have a set-up and hold time with respect to the leading edge of

the  $\overline{\text{WE}}$  signal.

In the 4118 and 4801, the actual write operation does not occur until the rising edge of the  $\overline{\text{WE}}$  signal. When that edge occurs, internal circuits pull either the DATA or  $\overline{\text{DATA}}$  line in a cell to ground. But writing differs from reading in that the line must be pulled all the way to ground to set the flip-flop in the cell. Just as in the worst case of the read cycle—when the data line supplying power to the cell is pulled to ground—writing again pulls the data line low on a whole column of cells, which would seem disastrous.

However, the design is such that the RC time constant

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of the load resistors and the corresponding parasitic and cell capacitances is high enough for the voltage on the unselected cells do not drop significantly in the short period of time that the data line is held at ground. The only disadvantage of this type of approach is that neither the 4118 nor 4801 allows a fully static write operation; each write cycle must be initiated and terminated by a falling or a rising edge of the  $\overline{WE}$  signal, respectively. Also, since the actual write operation does not occur until the rising edge of the  $\overline{WE}$  signal, the input data will have a setup and hold time with respect to  $\overline{WE}$ .

### Compatibility

Static RAMs have always suffered a lack of compatibility and an uncertain growth path. Of the standard devices, for example, the 1-K RAM is in a 16-pin package and the 4-K in an 18-pin package. The 24-pin, 600-mil-wide package is the next standard size, however, and it can fit up to 16-K bits: not only is it suitable for the 4118 and 4801 devices, but will house the next-generation MK4802, a 2-K-by-8-bit static RAM. After that, higher-density devices will have to accommodate themselves to 28-pin packages.

The pinout of the 4801 allows easy upgrade to the 4802, since it substitutes the extra address bit ( $A_{11}$ ) for the latch input. (Consequently, a system that is designed to eventually be upgraded should allow for that fact if it is using the latch input.)

As for densities higher than 16 K, the 32-K and 64-K static RAMs must be put in 28-pin packages, unless some data and address-multiplexing scheme is used. But the 28-pin package is the same width as the 24-pin one, and the pins on the 4118 and 4801 have been arranged such that it is possible to design a memory system to handle 1-K and 2-K-by-8-bit RAMs in the lower 24 locations of a 28-pin socket and still accommodate 32-K and 64-K devices when those become available. In fact, a memory system comprising RAM, ROM, or E-PROM can be designed today using 28-pin sockets that will guarantee upgrade compatibility through three memory generations, or for the next four to six years.

### Mixing with RAM

The compatibility question comes into play especially when considering microprocessor systems that mix read-only memory with RAM. The exact mixture of RAM and ROM is rarely known at hardware-design time, and it frequently changes even during the course of the product life. The memory designer must allow for expansion with spare sockets in the memory matrix, and if RAM is not pin-compatible with ROM, two matrixes are needed. The result is an excess of unused circuit-board area, which could be avoided by designing around a RAM that is compatible with a ROM—and thus around a single memory matrix that can mix RAM and ROM at will.

Figure 3 shows a typical microprocessor system that

mixes RAM and ROM. Six sockets provide 8 kilobytes of memory in any mixture of erasable programmable ROM (E-PROM) and RAM. Address differences between the 16-K 2716 E-PROM and the 4118 are taken care of by a jumper wire on pin 19 of the 4118.

Figure 4 shows the upgrade compatibility of the system, which packs 33 kilobytes—8 K of ROM, 16 K of E-PROM, and 9 K of RAM—into eight sockets. The MK37000 is a 28-pin version of the MK36000 8-K-by-8-bit ROM, and the MK2764 is an 8-K-by-8-bit E-PROM. Both the devices are scheduled for introduction in the beginning of next year. Allowing 28-pin packages for the whole matrix increases the capacity of those eight sockets to 64 kilobytes.

The fuse-link PROMs provide a flexible scheme for decoding the socket address space, and switches in dual in-line packages fill the role of address jumpers. Further selection of the memory blocks can be handled by the extra addresses on the PROMs.

The pin compatibility carries further, since high-speed applications can be served by the 4801. It is pin- and performance-compatible with the 82S2708 bipolar PROM—both have 70-ns access times—and the two can be paired well in a computer's control store, for example, where the PROM serves as read-only storage and the RAM as writable control store.

Last but not least is the question of compatibility with the 1-K-by-8-bit RAMs of other manufacturers. Currently, at least five manufacturers have announced intentions of producing devices compatible with the 4118 and 4801. Most of those products will be pin-for-pin-compatible except on pin 19; competitors will leave no connection on that pin, but it must be tied high if it is not used on the 4118 and the 4801.

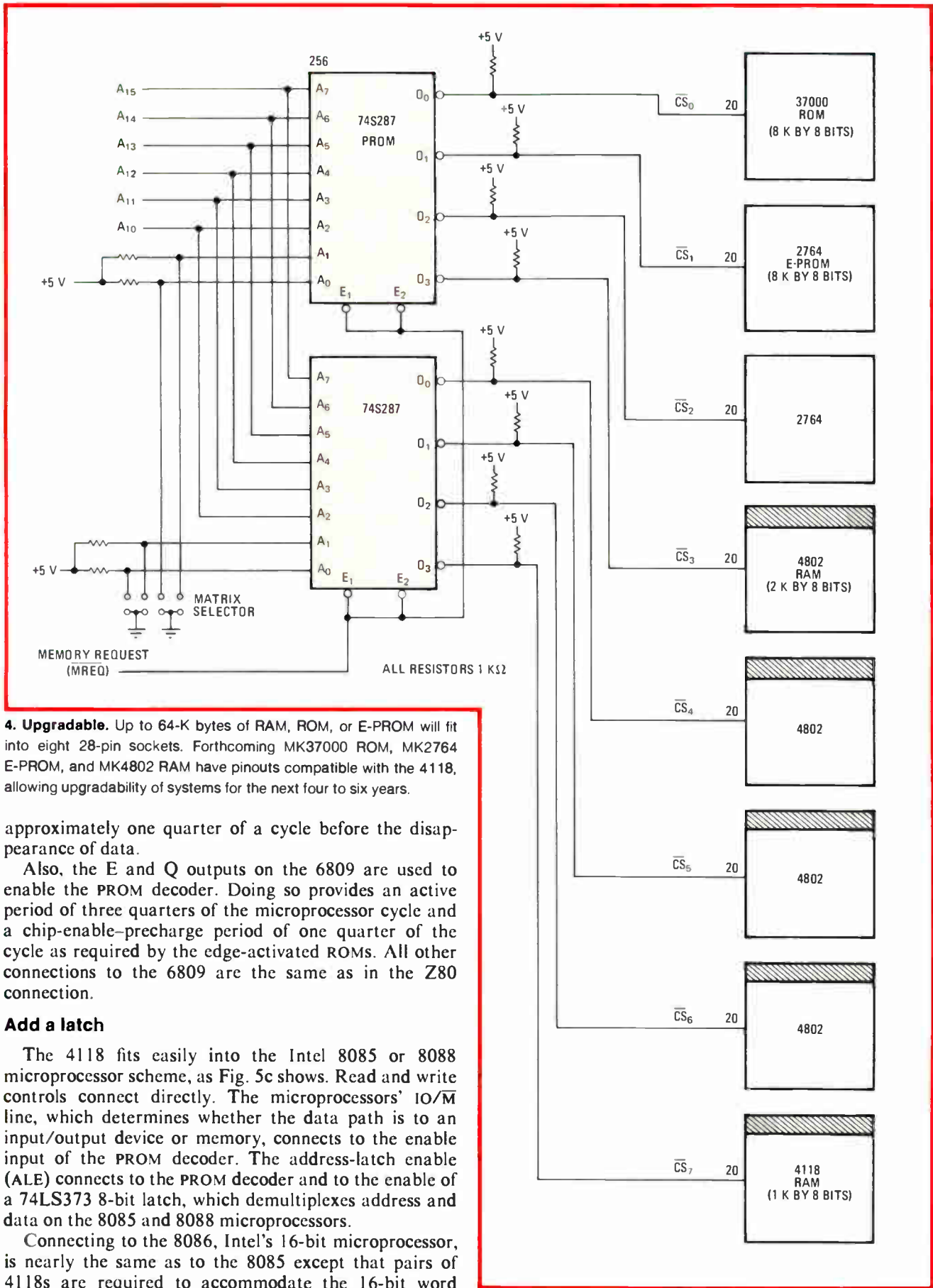
### Applications spectrum

The 4118 fits into those applications requiring good performance at low cost. As Fig. 5 illustrates, the part can easily interface with any microprocessor.

The 4118 is shown in a memory system for the Zilog Z80 microprocessor (Mostek's MK3880) in Fig. 5a. The configuration uses 28-pin sockets and can mix RAM, ROM, and E-PROM. The high-order microprocessor address bits are fed to a 74S287 256-by-4-bit bipolar PROM for address-space decoding. The PROM allows the space to be redefined at any time. All that is needed is an additional PROM address-decoder to expand the system to eight sockets, which would boost the memory capacity to 64 kilobytes.

A system connecting the 4118 to Motorola's 6809 microprocessor is shown in Fig. 5b. The control signals in this case require some additional logic for two reasons. The first is that the 6809 puts the read/write control ( $R/\overline{W}$ ) on a single pin, and logic is needed to separate the output-enable and write-enable signals. The second reason is a combination of several items of timing. To begin with, the 4118 requires that data inputs be held valid after the trailing edge of the  $\overline{WE}$  signal; in the 6809, however, data goes away at the same time as the  $R/\overline{W}$  signal. The extra logic combines clock output E on the 6809 with quadrature clock output Q to take the RAM's  $\overline{WE}$  high before  $R/\overline{W}$ . This ensures that  $\overline{WE}$  goes high





**4. Upgradable.** Up to 64-K bytes of RAM, ROM, or E-PROM will fit into eight 28-pin sockets. Forthcoming MK37000 ROM, MK2764 E-PROM, and MK4802 RAM have pinouts compatible with the 4118, allowing upgradability of systems for the next four to six years.

approximately one quarter of a cycle before the disappearance of data.

Also, the E and Q outputs on the 6809 are used to enable the PROM decoder. Doing so provides an active period of three quarters of the microprocessor cycle and a chip-enable-precharge period of one quarter of the cycle as required by the edge-activated ROMs. All other connections to the 6809 are the same as in the Z80 connection.

**Add a latch**

The 4118 fits easily into the Intel 8085 or 8088 microprocessor scheme, as Fig. 5c shows. Read and write controls connect directly. The microprocessors' IO/M line, which determines whether the data path is to an input/output device or memory, connects to the enable input of the PROM decoder. The address-latch enable (ALE) connects to the PROM decoder and to the enable of a 74LS373 8-bit latch, which demultiplexes address and data on the 8085 and 8088 microprocessors.

Connecting to the 8086, Intel's 16-bit microprocessor, is nearly the same as to the 8085 except that pairs of 4118s are required to accommodate the 16-bit word

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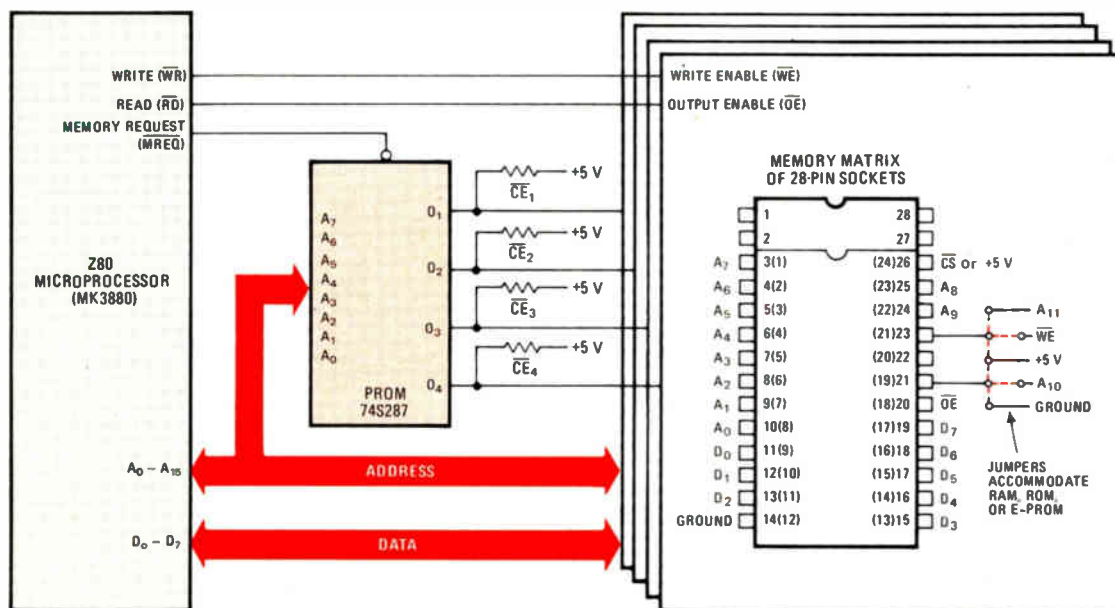
PROCESSES

**5. Easy interfacing.** The 4118 RAM hooks easily to most microprocessors. Connecting to the Z80 requires only a PROM for decoding (a). The 6809 requires additional logic (b), whereas the 8085 and 8088 need a latch (c) for demultiplexing. The 16-bit 8086 needs memory pairs (d), as well as a pair of PROMs for byte addressability.

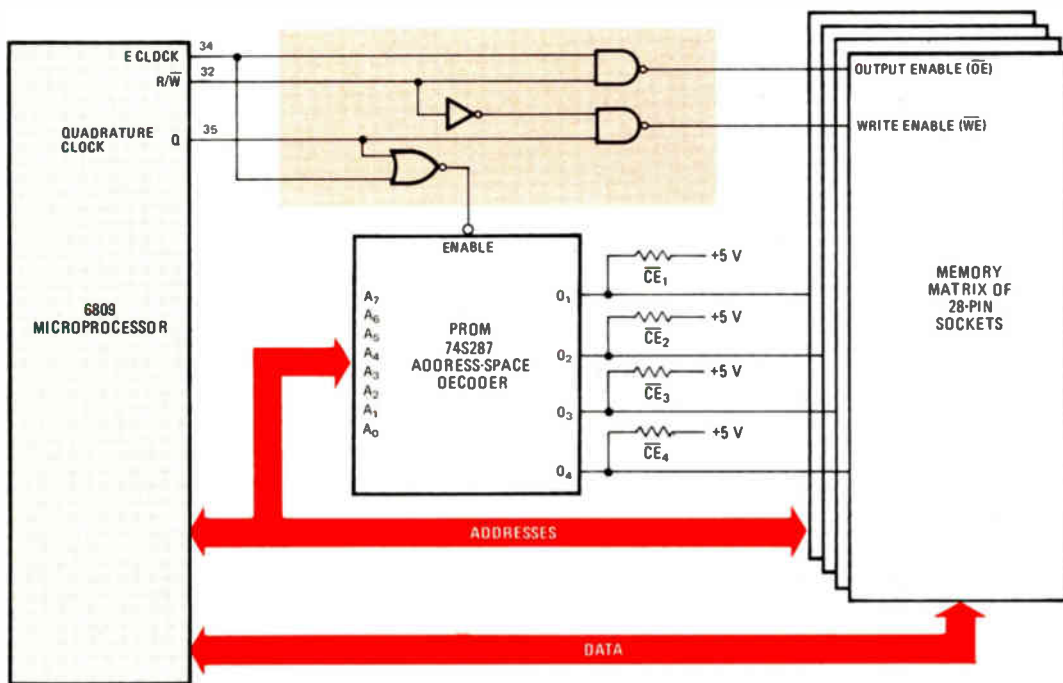
(Fig. 5d). Two PROM decoders are required to generate the chip-enable signals to meet the byte addressability requirement—the 8086 can pick either 8- or 16-bit data at a time—otherwise a single decoder would suffice.

### High-speed applications

The 4801 serves the high-speed applications market, which currently relies on bipolar RAMs. The largest bipolar RAM is Fairchild's 93470, organized as 4-K by 1 bit. The 4801 has twice the density, yet can dissipate as little as one fourth the power when used in a 4-K-by-8-bit



(a)



(b)

array. (A similar array using 93415 1-K RAMs would dissipate six times as much power as a 4801 implementation.) In addition, the 4801's byte-wide organization fits well into a good number of bipolar applications.

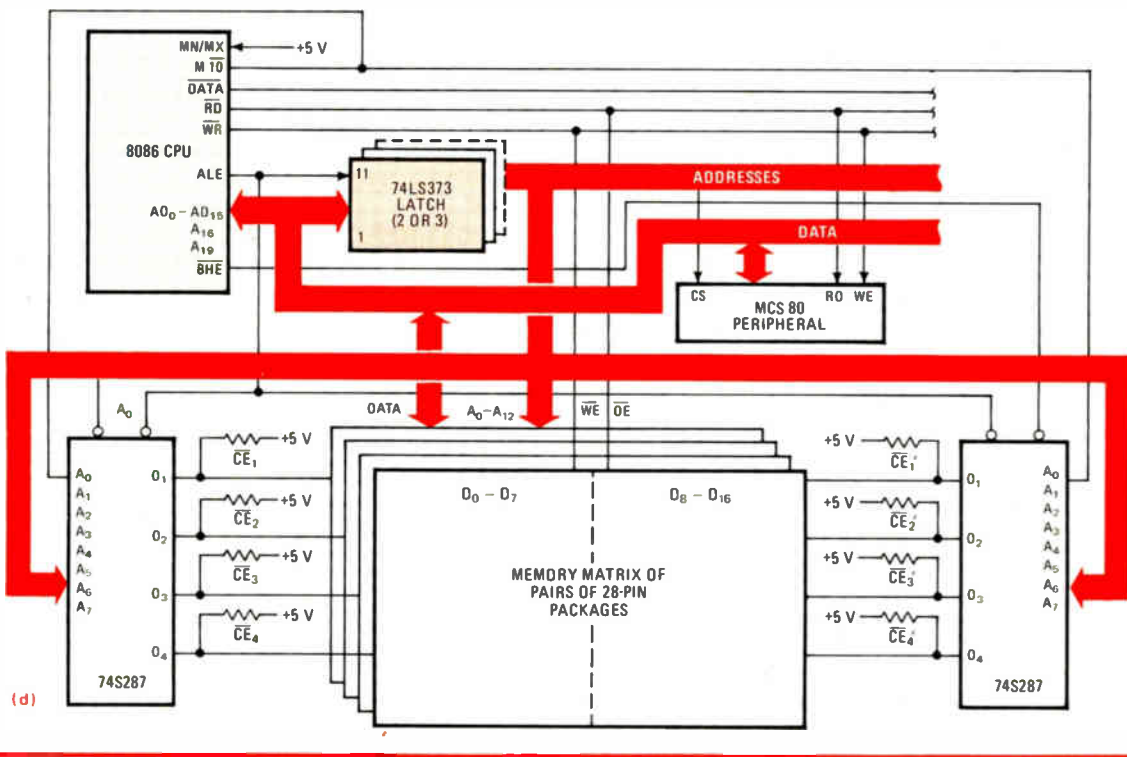
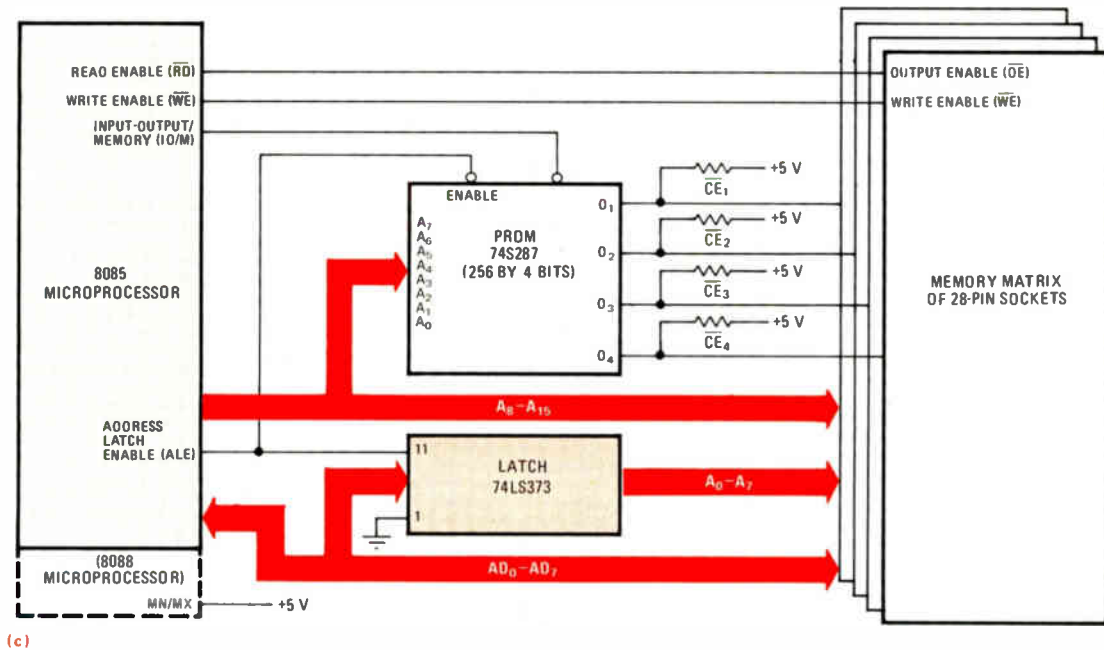
### Bettering bipolar

One application that has always used bipolar memories exclusively is caches and writable control stores in a computer. The 4801 can serve as a cache between a bit-slice processor and main memory, which would use dynamic RAMs, and at the same time can fill the various

requirements of the processor's writable control store.

Another application that requires the 4801's high speed is multiported memory. Many distributed systems have several slow microprocessors that share a global memory.

If the memory is fast enough, which the 4801 is, the system can be configured such that all memory is shared without any significant slowing of either the overall system speed or the speed of any individual processor. In this application, the 4801 can greatly cut system costs by eliminating memory redundancy. □



# Microcomputer-based control smoothes universal motor performance

N-channel MOS chip makes feedback loop cost-effective in consumer applications

by Tom Slade, *General Instrument Corp., Microelectronics Division, Hicksville, N. Y.*

□ Universal motors, so-called because they can run on either an alternating or a direct current, are widely used in vacuum cleaners, blenders, power tools, sewing machines, and other consumer appliances that need to operate at varying speeds. These motors supply high horsepower relative to their weight and size, easy speed control, high starting torque, and economical operation. But they also demand high starting current, generate a lot of noise, overheat at low speed, and suffer from inherently poor speed regulation as well as poor efficiency when the load is variable.

A microprocessor-based closed-loop motor controller (Fig. 1) reduces or eliminates these disadvantages. Being less costly and more reliable than a closed loop built with discrete devices, it is practical for a great many more consumer applications. It is also a cost-effective means of adding several desirable operating features.

For instance, the input speed of a power tool may now be set through a digital keypad or potentiometer. (In the latter case, the microcomputer converts the analog input into digital form before setting tool speed.) Moreover, microprocessor-controlled automatic current limiting enhances the reliability and life of the universal motor, replacing the passive components that generally keep its starting and overload currents to levels that are safe for its brushes, on-off switch, and owner's housewiring. In addition, such current limiting protects the motor from overheating.

## Open versus closed loop

With a constant voltage input, the load that a universal motor must move determines its speed. But as Fig. 2 shows, the speed-torque curve that describes this open-loop relationship (solid black line) is highly nonlinear, and it remains just as nonlinear throughout any change in driving current used to shift it (dashed black line) and thus alter motor speed. Moreover, full torque is not available at lower speeds in any case.

The operating curve for a motor with closed-loop speed control is entirely different. Now the speed remains almost constant under a variable load (nearly horizontal solid colored line) so long as the peak load does not exceed the available torque.

It is worth noting at this point that a universal motor with a closed-loop control and a variable load draws less current as a function of torque (colored dotted and

dashed line) than does one without such a control (black dotted and dashed line). This not only saves power but also reduces the amount of audible noise because, when a motor uses less current, it is slower and therefore less noisy—and what is more, interferes less with its user's television reception.

A microprocessor-based implementation of such a closed loop requires only a few external components, including a speed pickup, a triac, and a power supply (see Fig. 1 again). It assumes ac, not dc, operation of the universal motor.

A typical speed pickup might consist of a 20-pole magnetic disk and a Hall-effect sensor. Such an arrangement would feed back 10 pulses per motor revolution to the microprocessor, since a high-resolution input is necessary if the loop is to have refined control over its output to the triac.

## Triac triggering

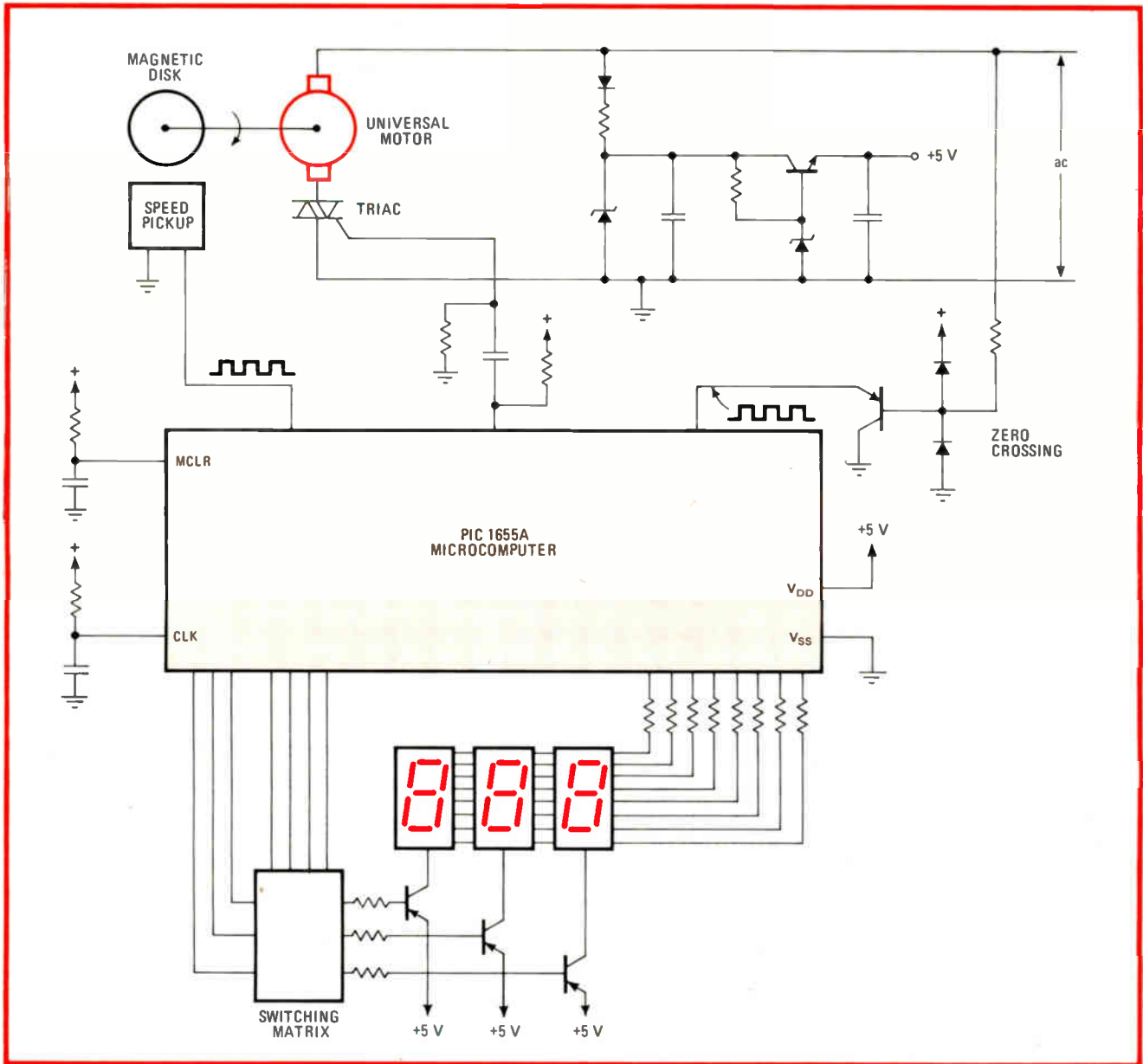
The loop triggers the triac at varying times after the ac reference signal's zero crossing. This variable firing angle in turn varies the power delivered to the motor by setting the average current fed to the series windings. Typically the triac is rated at 6 to 15 amperes and drives a motor of 0.5 to 2 horsepower.

The user's input to the loop may be made through a keypad and display, incorporated in it with the addition of a few extra components as shown in the figure. This keypad can be scanned and the display multiplexed at up to a 250-kilohertz rate by the microcomputer—a more-than-adequate rate for consumer applications.

In operation, the microprocessor continually compares the speed set by the user with the speed measured by the Hall-effect pickup and then adjusts the power delivered to the motor to minimize any error in performance.

For instance, in a blender application, the desired motor speed and run time would be entered by the cook, and the microcomputer would then send the triac the pulses appropriate for applying a steadily rising current to the motor until it reached the speed the cook wanted. In larger appliances, of course, this "soft" start would limit the typically very large initial surge currents of the universal motor, thus safeguarding switches and wiring.

Moreover, current limiting of the universal motor is readily achieved by limiting the firing angle of the drive triac as a function of the maximum speed desired. In



1. **Close the loop.** Older feedback loops for motor control had many parts and offered few features at a high cost. But the microprocessor approach allows the use of just a few inexpensive additional components and gives the user more precise control over the motor.

essence, the maximum allowable number of pulses from the speed pickup in a given period of time is made to determine the maximum firing angle.

The operating characteristic of the motor is then modified to follow the solid vertical colored line of Fig. 2 in an overload condition. (It is to be noted that \* on the colored dotted and dashed current curve corresponds to this limit.)

This principle can be extended to protect the motor from overheating when it is being forced by heavy loading to run at low speed. A simple timer incorporated into the control loop just rolls back the current to a safe limit after a predetermined time (indicated by the colored dotted line in Fig. 2).

In sum, then, the operation of the universal motor is limited to the horizontal solid colored line of Fig. 2 for various loads until the overload condition is reached.

Then its speed drops while a constant current is maintained along the vertical line. In this condition, the motor is overheating, and after a period of time predetermined by the microprocessor, the current rollback feature moves the load line back to the dotted line in the figure. When the load is reduced, the operating point will move up the dotted line to the horizontal one and into the normal region.

### Firing angle control

Universal motor torque is a nonlinear function of firing angle and speed (Fig. 3a). In order to linearize it, so that a speed variation produces a corresponding change in torque, the deviation of the actual from the set speed—the speed error—must be mapped into the phase angle, which can then be used to adjust matters.

Done empirically, this mapping (Fig. 3b) yields a

## Why universal motors?

Series-wound motors, in which the same current passes through both rotor and stator, are perhaps the most popular of fractional and subfractional motor types. They deliver high motor speed, high starting torque, wide speed capability and reasonable efficiency. By way of an example, the figure analyzes the motor described in the article.

Essentially the same as shunt-wound motors in appearance, a series motor has its armature and field connected in series with the power supply, rather than being shunted with respect to it. This allows some series machines to be designed for operation on either ac or dc power—hence the name universal. (Other series motors are not universal, being optimized for a particular power supply, and might fail if operated on a different supply.)

No universal motor has the same performance on ac as on dc. Usually, for example, the motor will run slower on ac, because of the higher impedance it creates in its windings, than on dc. The higher the load, the more obvious this difference becomes.

In addition to their power supply versatility, series-wound motors have the highest horsepower per pound and per dollar of any motor that can operate on standard single-phase ac power. This at least in part accounts for their utility as motors in household appliances and power tools. To obtain greater efficiency and brush life, they are usually unidirectional devices, but bidirectional series motors can also be produced. One reversible series motor is the three-wire design, which can be reversed with a simple single-pole, double-throw switch.

The speed of a series motor can be adjusted over a broad range by means of a rheostat, an adjustable transformer, or an electronic control. Both the no-load and the operating speed motors are usually quite high. In fact, no-load speeds in excess of 15,000 revolutions per minute are common.

Although high speed is a significant advantage, it does not come without a price. It shortens bearing and brush life badly enough to limit series motors to intermittent-duty application, such as occurs in vacuum cleaners and power tools. In these appliances, brush life generally ranges from 200 to 1,200 hours.

Universal motor speed can be changed simply by varying the voltage across the motor. For this purpose a variable resistor, a variable voltage transformer, or an electronic control may be used.

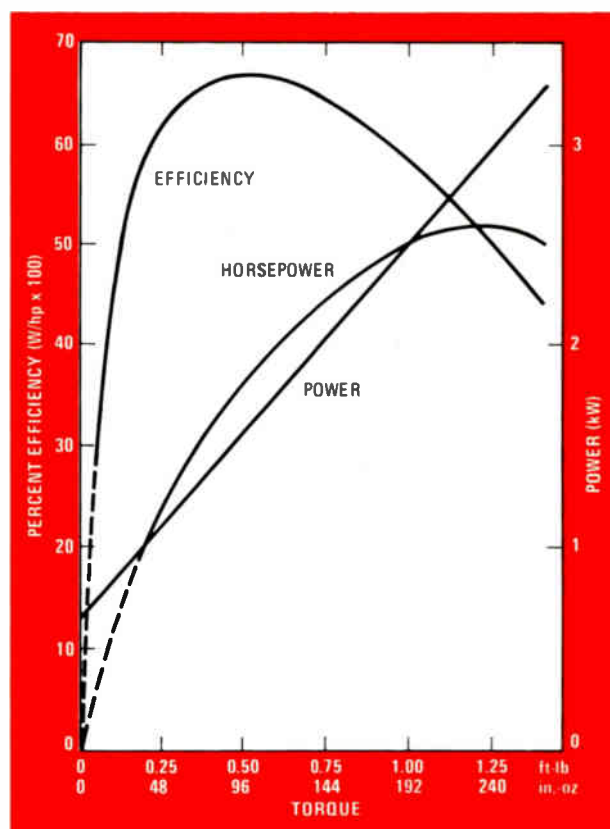
A variable resistor or rheostat in series with the motor will decrease the speed of the motor at any load as the resistance is increased. In theory, the motor speed could be adjusted to zero. In practice, the minimum speed is usually limited to some finite value due to friction.

A variable transformer typically varies the speed of a series motor over a range of 4:1 to 7:1. If a full-wave bridge is used to convert the output of the transformer into dc, the speed range will be increased because of the improved regulation and starting torque.

A typical older method of electronic control for a series motor is a half-wave device with feedback. Since these controls are half-wave, the maximum voltage to the motor is much less than 115 volts, so that the top speed of the motor is also low. However, if there is a feedback that corrects for the drop in speed due to load, it usually allows an extension of the speed range on the low end, due to improved starting torque and speed regulation.

Triac control—essentially two silicon controlled rectifiers in parallel with reversed polarity—is also possible. It is the most modern and cost-effective of all approaches when used with a microprocessor-based feedback control.

**-Harvey J. Hindin**



curve of speed error versus torque that is almost linear. This curve's independence of a specific speed is assured by correlating speed error with firing angle for each of various speeds.

### Speed measurement

The speed control algorithm built into the microprocessor uses the percentage error between the actual and set speed. For relatively small changes in speed, the percentage change in the period of revolution is approximately the same as the percentage change in speed.

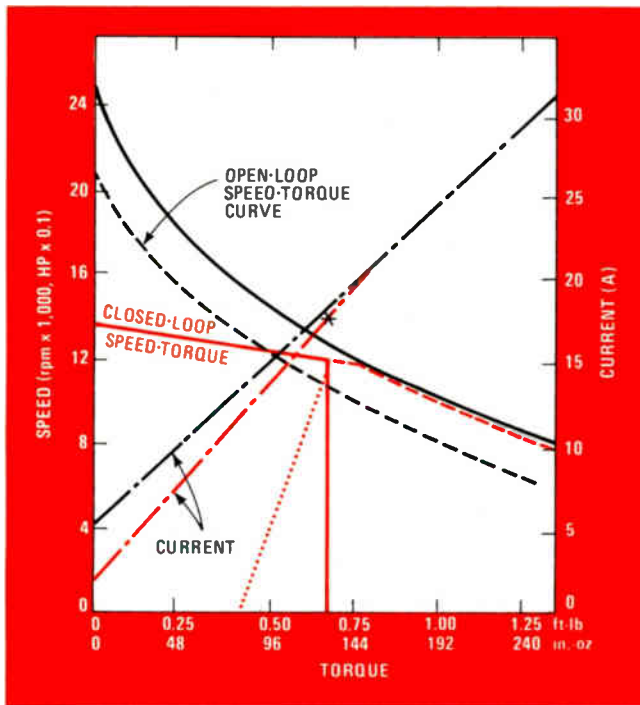
If measurements for all possible set speeds in the same

length of time are made with sufficient resolution, by picking up many pulses per motor revolution, the percentage error difference between the set period and actual period is approximately the negative percentage speed error.

This is easily shown mathematically. The fractional error in speed,  $E_s$ , is of course the difference between the set speed,  $S_s$ , and the actual speed,  $S_A$ , expressed as a fraction of  $S_s$ , or:

$$E_s = (S_s - S_A) / S_s \quad (1)$$

The speed in revolutions per minute is 60 times the



**2. Change the curve.** The speed-torque curve of a universal motor determines the motor's operating point for a constant voltage input and applied load. Only a closed-loop controller will allow the speed to be kept relatively constant in the face of a variable load.

product of the reciprocals of  $N$ , the number of pulses per revolution, and  $P$ , the period in seconds of those pulses. So by substitution in Eq. 1:

$$\begin{aligned}
 E_S &= [(60/NP_S) - (60/NP_A)] / (60/NP_S) \\
 &= (1/P_S - 1/P_A) / (1/P_S) \\
 &= 1 - [P_S / (P_S - P_E)] \\
 &= -P_E / (P_S - P_E)
 \end{aligned}$$

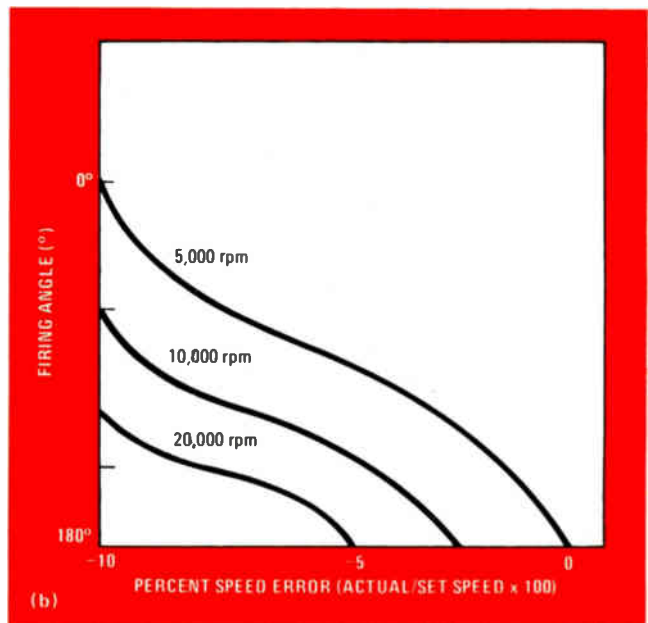
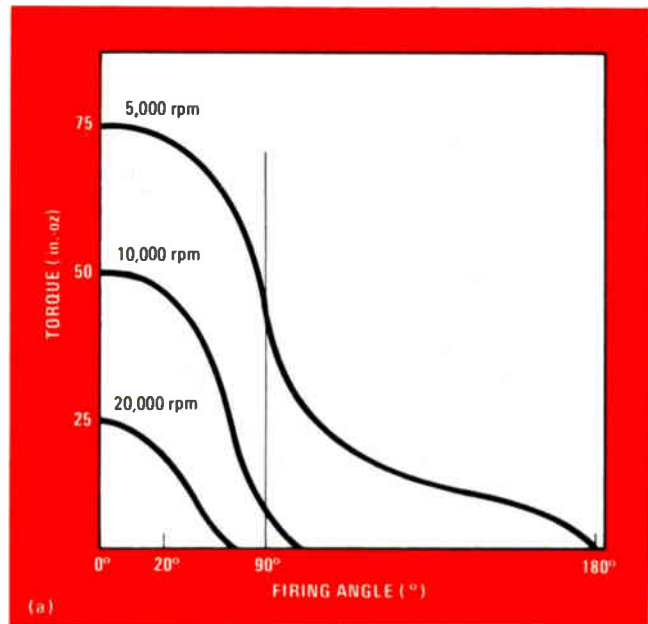
where  $P_A$ ,  $P_S$ , and  $P_E$  are respectively the actual, set, and error periods in seconds. But if the error period is very much smaller than the set period (the usual case),  $E_S = -P_E/P_S$ , as was stated.

For these constant or near constant measurement period approximations, the error in period is proportional to the percentage speed error and can replace it in the firing angle mapping to achieve proper control (Fig. 4). For fixed speeds, the values of  $N$  and  $P$  can be stored in a look-up table, and for variable speed control they can be calculated by means of a divide routine. Both of these are stored in the microprocessor.

### Ripple control

To refer back to Fig. 3b, it is important to note the sharp change in torque for a given change in firing angle around  $90^\circ$ . The resolution of the firing angle at this point determines how much ripple there is in motor speed. At low speed, inadequate resolution can cause sputtering where the torque change is such that it produces very noticeable jerks in speed.

For instance, when the motor starts from zero speed, the first load line corresponding to a small firing angle (Fig. 5) is followed up to the first speed point. There a second and larger firing angle is switched in. This



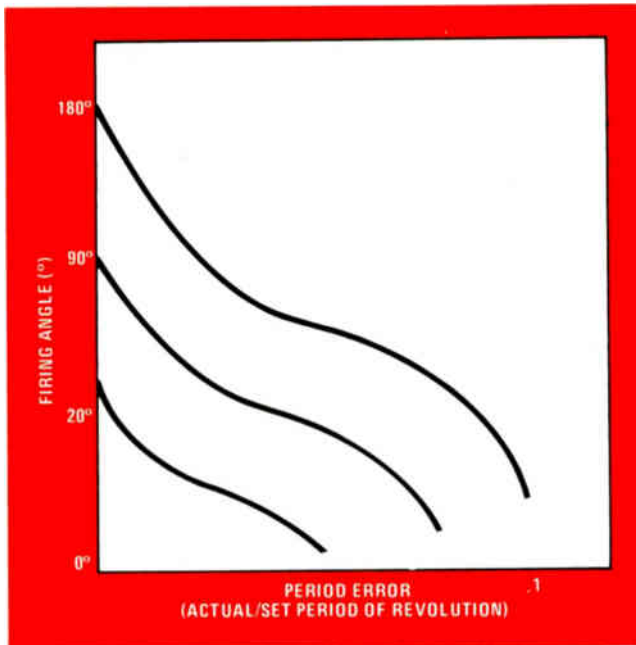
**3. Mappings.** Torque is a nonlinear function of both triac firing angle and motor speed (a). For linear motor speed regulation, the speed error must be mapped into firing angle (b). If done properly, a linear speed-error versus torque curve is achieved.

discrete control is continued until the motor runs out of torque. From this diagram it is clear that any ripple will be determined by the step size in measurement made by the speed pickup and the resolution of the firing angle as set by the microprocessor.

### Microcomputer requirements

A microcomputer used in universal motor speed control must have an 8-bit data word and an instruction execution rate of at least 250 kHz to perform the functions discussed. And of course it should and does consume relatively little power.

The first two requirements are important because of the relatively complex calculations that must be



**4. Period.** For small changes in speed, the change in the period of motor revolution is the same as its change in speed. Consequently, the error in the motor period is proportional to its speed error and can therefore replace that variable in the firing-angle mapping.

performed quickly and the high resolution required for the triac firing angle at low motor speeds.

The General Instrument n-MOS PIC 1655A was specifically designed to meet these constraints. A one-chip microcomputer that uses only 35 milliamperes from a 4.5-to-7-volt supply, it has a pipelined architecture, 12-bit instructions, and an 8-bit data path.

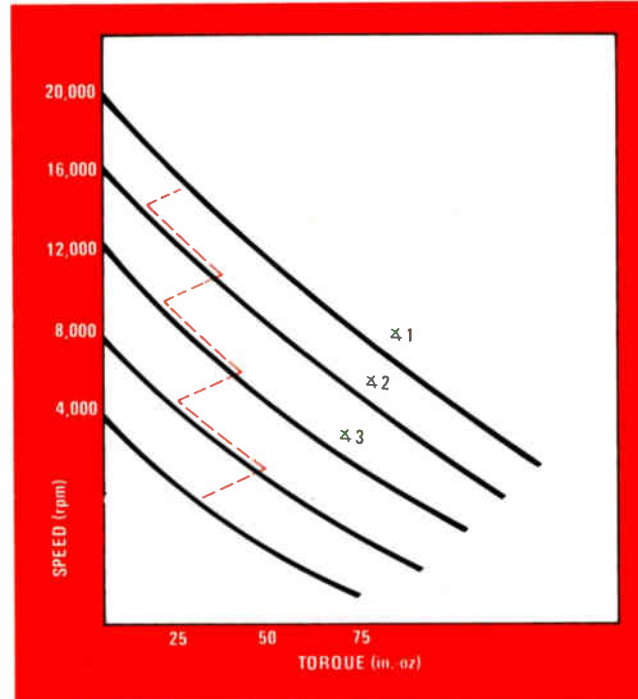
Pipelining, or fetching the next instruction while executing the current one, shortens its instruction execution time to 4 microseconds. Also, the internal functions—the arithmetic and logic unit, memory, and input/output—need have data settling times of only 2 to 3  $\mu$ s to permit a conservative design and extended temperature ranges.

The 12-bit instruction word is long enough to eliminate the need for multiple fetches of instructions. The instruction set includes, in addition to common operations such as add, subtract, AND, OR, and exclusive-OR, other powerful bit operations like bit set, bit clear, and bit test. For example, the BSFSC 7, 2 instruction will skip the next instruction when bit 2 of I/O register 7 is low.

The 8-bit data path is adequate for most control applications. However, the PIC can handle the double precision necessary when 16-bit resolution is required. Its double-precision signed-integer math routines, including addition, subtraction, multiplication and division, are contained in 90 instructions.

#### More suction

What can a microcomputer do for a home vacuum cleaner? On the one hand, the vacuum motor can have a soft start. That is, current is limited during startup. With this feature, larger motors can be installed to allow higher vacuums and greater air flow without dimming the lights, blowing fuses, or exceeding Underwriters



**5. Jumpy.** Starting from no motor movement at all, the first load line of the motor—which corresponds to a small firing angle—is followed up to the first speed switch point, where the next firing angle takes over. This process continues until the motor runs out of torque.

Laboratories specifications on turn-on.

In addition, the vacuum motor can be run at maximum efficiency. Depending on motor design, this might correspond to a constant speed of about 15,000 revolutions per minute for about 70% to 80% efficiency. Now the centrifugal blower can also be optimized for constant speed operation, further enhancing efficiency and lowering peak noise.

Note that the term “constant speed” means speed regulation within a certain limit, which will depend on the application. A speed decrease of about 10% from no load to full load is actually desirable since an increase of about 30% in vacuum pressure in fact accompanies decreased flow.

#### Another trick

An alternative to constant pressure control is constant torque operation—allowing the speed to vary to maintain constant air flow. Furthermore, it permits the use of a motor designed for very high speeds, but one that normally draws too much current at lower speeds. Higher available vacuum pressure than would otherwise be possible is the result.

An improvement desirable in a vacuum cleaner is a reliable “bag full” indication. The indication of a full bag is low air flow over a period of time. Since the flow is most often proportional to torque in constant speed operation, the microcomputer can digitally filter the torque input signal and turn a lamp on. If the vacuum is run with constant torque, the bag will be full when the average speed goes over a certain limit. And finally, it is easy to hook up several push buttons to preset carpet beater speed and vacuum level. □





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# Supersensitive measurement demands critical input design

The more esoteric sources of current and leakage must be taken into account when counting electrons

by Robert Miles, *Keithley Instruments Inc., Cleveland, Ohio*

□ The success of the ongoing quest for electronic devices that do their jobs with less current at lower voltages brings with it an attendant problem: that of convenient measurement of these extremely low currents, voltages, and charges.

Recent improvements in MOS field-effect transistors and the development of complementary-MOS logic, bipolar FETs, and MOS FET operational amplifiers have reduced input and operational current requirements by decades. The widespread use of these and related devices with input currents in the picoampere range has increased the demand for ultralow-current and ultra-high-impedance measurements.

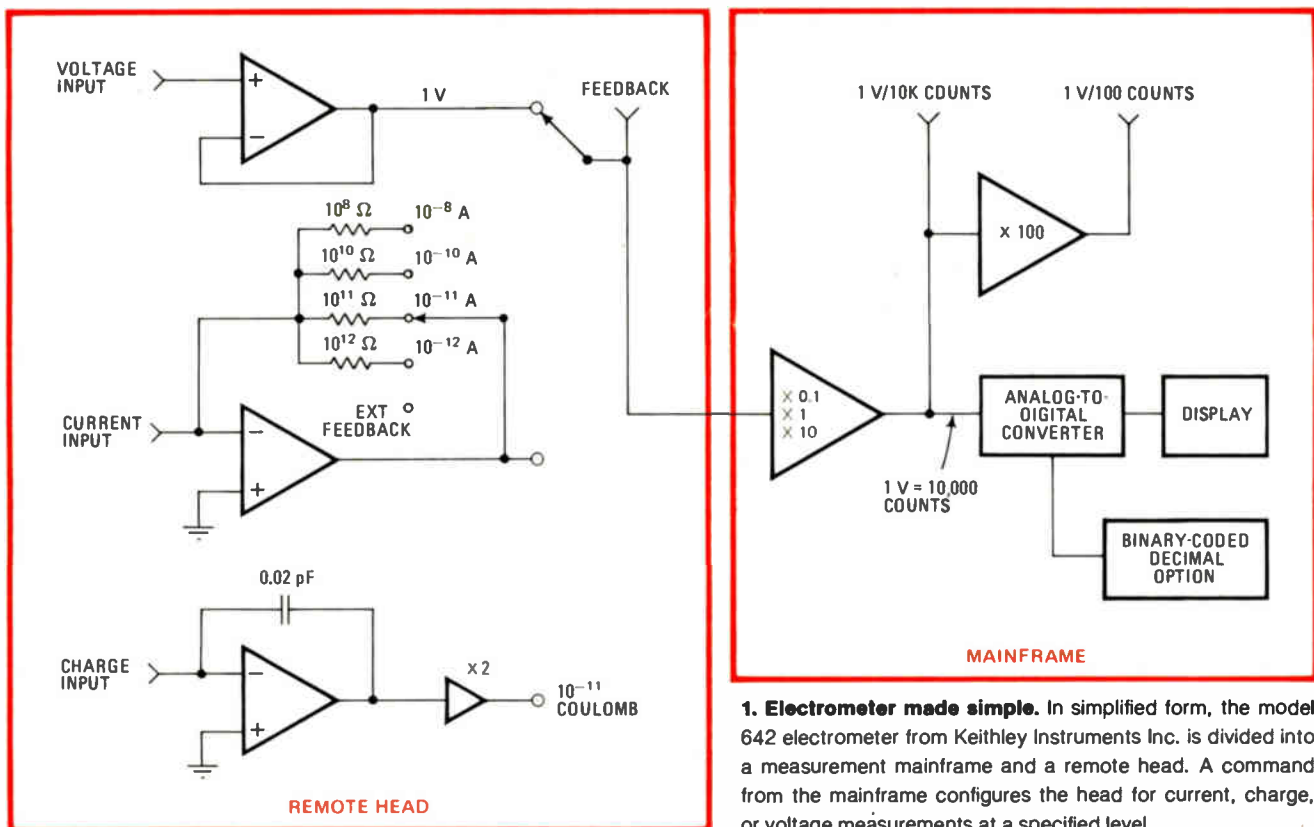
Many other situations exist that require convenient, low-current measurements, such as the examination of semiconductor current-voltage relationships, low-level photodetector response, and other phenomena in special-

ized applications of physics and chemistry. The design of a portable, solid-state instrument such as the Keithley model 642 electrometer [*Electronics*, Dec. 7, 1978, p.159] shown in Fig. 1 embodies the concepts and techniques necessary to make measurements at these levels and so bears close examination.

## Extremes

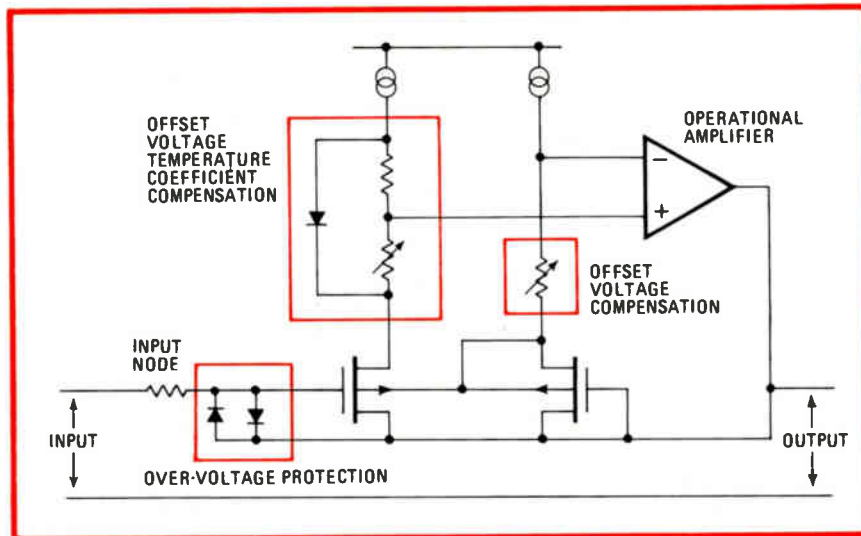
Basically, an electrometer is a refined direct-current multimeter. It can be used for virtually any task normally performed by a conventional multimeter. But its input characteristics permit it to perform voltage, current, resistance, and charge measurements far beyond the realm of the conventional multimeter.

An electrometer's input resistance is very high, typically above  $10^{14}$  ohms and sometimes as high as  $10^{16}$   $\Omega$ . Offset current at the input is typically  $5 \times 10^{-14}$  ampere



**1. Electrometer made simple.** In simplified form, the model 642 electrometer from Keithley Instruments Inc. is divided into a measurement mainframe and a remote head. A command from the mainframe configures the head for current, charge, or voltage measurements at a specified level.

**2. More for less.** In addition to providing less expensive circuitry, the use of MOS field-effect transistors in the electrometer's input circuit allows compensation for offset voltage and its temperature coefficient. Both compensation networks can be independently located in either source lead.



or lower. These characteristics allow voltage measurement that causes only an extremely small amount of circuit loading. Electrometers are capable of monitoring current levels down to the theoretical limits imposed by the level of the input offset current: the Keithley 642's most sensitive current scale reads 200 femtoamperes full-scale. Full-scale charge readings on the instrument's 4½-digit display go from  $10^{-10}$  to  $10^{-12}$  coulomb; currents below  $10^{-15}$  A are generally best measured using the charge function and a strip-chart recorder to monitor the analog output. In this way, resolutions of  $10^{-17}$  A can be achieved. Its high input resistance and low current offset also enable the electrometer to measure resistances from ordinary levels up to extremely high values.

At these levels of measurement, the user must always be sure that the interconnecting structure that carries the signal from the current or voltage source being measured to the input connector of the electrometer does not contribute to or otherwise degrade that signal.

### Detection

Central to any electrometer design is the active input device that detects the voltage imbalance at the input junction (or input node). A number of useful criteria exist for the selection and evaluation of such devices: the input gate current and resistance, the offset voltage stability with time and temperature, the voltage and current noise, and the complexity of any associated circuitry needed.

The electrometer input devices most widely used today are MOS FETs, but it is difficult to obtain them with input gate currents below  $10^{-14}$  A. For the model 642, a minimum input current requirement of  $5 \times 10^{-17}$  A was established (about 300 electrons per second).

Other instruments capable of measuring inputs at this level employ a vibrating capacitor, or reed, as the input device. These capacitors and their associated circuitry are relatively costly, and the circuitry presents additional performance problems. The forward gain block in a vibrating reed configuration consists of an alternating-current amplifier with multiple poles in its response when mapped in the complex frequency plane. The amplifier's stability is easily compromised if there is an

additional pole in any feedback network.

A solid-state input device, on the other hand, with an output response down to dc, permits the use of an integrated circuit operational amplifier with only a single, dominant pole in its response. Its performance stability with feedback is therefore much better than that of the vibrating reed circuitry. Its overall cost is lower, as well.

### Plugging the leaks

The MOS FET input gate current is lowered by dealing with two of its major leakage mechanisms: that of the header and the leads. Special die processing and packaging eliminates all unguarded leakage paths save that of the silicon dioxide gate insulation. The MOS FET die is mounted on an alumina substrate which in turn is affixed to a TO-8-package metal header. The use of the alumina substrate avoids committing the header to the MOS FET substrate, so each lead in this package passes through a glass feed-through insulator and is both shielded and guarded from all other leads by the header. Guarding is a construction technique wherein all potential leakage paths from the conductor being guarded are interrupted by another conductor that is driven (by a low-impedance source) to the potential of the guarded conductor.

Another advantage in using MOS FETs is that they allow compensation for offset voltage and its temperature coefficient. In the 642 electrometer, the input MOS FET is operated as a source follower, with another MOS FET providing a gate-to-source voltage reference; each MOS FET's source is driven by a constant current supply, as shown in Fig. 2. The operational amplifier gain block is then driven from the dual MOS FET source. The offset-voltage temperature coefficient is cancelled by a portion of the forward voltage of a silicon diode mounted in close proximity to the input MOS FET. A fixed-source resistance is used to cancel any residual MOS FET offset or diode forward voltage. With this configuration, a voltage-offset temperature coefficient of 30 microvolts/°C is obtained; vibrating-reed input devices typically have a temperature coefficient of about  $100 \mu\text{V}/^\circ\text{C}$ .

In the light of the sensitive input characteristics of any

## Three measurement demons

**Heat.** In a resistor, the kinetic energy of molecules produces motion of electrical charges. These charge movements result in noise called Johnson, thermal, or heat noise. In theory, the power available from this motion is constant and given by:

$$P = 4kT\Delta f$$

where  $k$  = Boltzmann's constant,  $T$  = temperature in kelvins, and  $\Delta f$  = the noise bandwidth in hertz over which the measurement is being made. Metallic conductors approach this theoretical noise level; other materials produce more noise than theory predicts. From the equation, Johnson voltage noise ( $E$ , in volts root mean square) developed in a resistor,  $R$ , can be found:

$$E = (4kT\Delta fR)^{1/2}$$

and Johnson current noise ( $I$ , in amperes rms) becomes:

$$I = (4kT\Delta f/R)^{1/2}$$

**Pressure.** Piezoelectric currents are generated when mechanical stress is applied to certain insulating materials, notably ceramics and other crystalline material. Teflon

and some other plastics used for insulated terminals and interconnecting hardware exhibit what is known as a space charge effect, wherein an applied force creates a change in capacitance and thus a charge redistribution. The behavior is the same as for piezoelectric materials: a physical force creates a current.

**Friction.** Triboelectrically generated currents result from the creation of charges at the interface between a conductor and an insulator due to frictional forces at the interface, as in the case of a cable that is moved. The mechanism involved is one of rubbing off electrons, creating a charge imbalance and thus a current flow. Low noise cables are available that have a conductive coating (usually graphite) at the metal-insulator boundary, reducing this effect significantly. Currents down to 1 picoampere can be measured using cables treated in this manner. Rigidly securing the cable from any movement will permit its use down to a few femptoamperes. Rigid airline coaxial cable such as GenRad GR874 series is suitable down to 0.1 fA. Below this current level, special connection schemes and the use of high quality insulators such as sapphire are required.

electrometer, input over-voltage protection is essential. Silicon diodes can be used to limit the input-to-guard potential during input overload, but an additional leakage source at the input is the price paid. Available devices reduce this leakage to  $10^{-14}$  or  $10^{-15}$  A.

To obtain better leakage characteristics, the junction characteristics of diodes made from other materials were examined. Experimentation showed that gallium phosphide (GaP) diodes had better leakage characteristics at low voltages, with both forward and reverse bias.

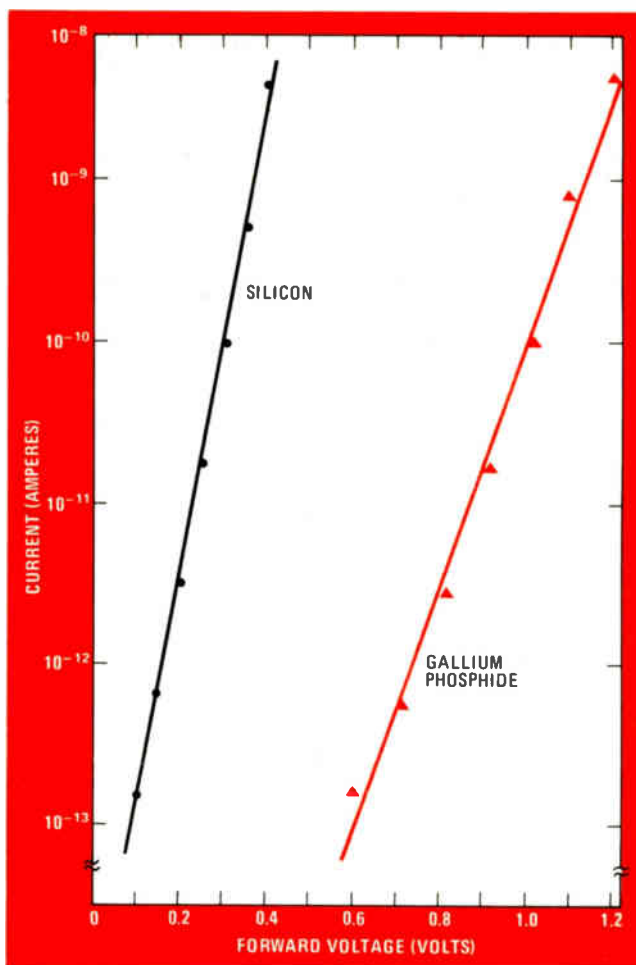
### Johnson noise

A more important concern is the impact of the input protection device on the instrument's input current noise. To minimize Johnson current noise (see "Three measurement demons") that could degrade input resolution, particularly in the charge function, the resistance across the amplifier input must be maximized. A number of sources contribute to input resistance, including structural insulators, the input MOS FET, and the input protection device. Of these, the resistance of the input protection device is the most significant.

Evaluation of available silicon and gallium phosphide diodes yielded the characteristic current-voltage plots shown in Fig. 3. By extrapolating these plots, an estimate of the junction resistance at zero forward bias for silicon ( $7.5 \times 10^{12} \Omega$ ) and gallium phosphide ( $3.9 \times 10^{16} \Omega$ ) was obtained.

Although these figures have not been rigorously verified for very small forward bias voltages, they serve to indicate the superiority of GaP, which is borne out in the actual performance of the 642. The GaP diodes are connected back-to-back in the instrument and mounted in a guarded package similar to that used for the input MOS FET. The resistance in series with the input (see Fig. 2) limits the input overload current.

The selection of an insulating material to mechanical-



**3. Si vs GaP.** The choice of gallium phosphide rather than silicon diodes for overvoltage protection is dictated by GaP's higher junction resistance. Estimates of both diode types' resistances near zero forward voltage are obtained from the slope of the plots shown.

TABLE 1: PROPERTIES OF INSULATING MATERIALS

Material	Volume resistivity (ohm-centimeters)	Resistance to water absorption	Minimal piezoelectric effects	Minimal triboelectric effects
Sapphire	$10^{16} - 10^{18}$	■	■	□
Teflon	$10^{17} - 10^{18}$	■	■	■
Polyethylene	$10^{14} - 10^{18}$	□	■	□
Polystyrene	$10^{12} - 10^{18}$	□	□	■
Kel-F	$10^{17} - 10^{18}$	■	□	■
Ceramic	$10^{12} - 10^{14}$	■	□	■
Nylon	$10^{12} - 10^{14}$	■	□	■
Glass epoxy	$10^{10} - 10^{17}$	■	□	■
Polyvinyl chloride	$10^{10} - 10^{15}$	■	□	□
Phenolic	$10^5 - 10^{12}$	■	■	■

Key

- Very good in regard to the property
- Moderately good in regard to the property
- Weak in regard to the property

TABLE 2: COMMON THERMOELECTRIC POTENTIALS

Materials	Potential (microvolts/°C)
Cu - Cu	0.2
Cu - Ag	0.3
Cu - Au	0.3
Cu - Cd/Sn	0.3
Cu - Pb/Sn	1 - 3
Cu - CuO	1,000

ly support and electrically isolate the input node is a key element in the performance of any electrometer or low-current instrument. Material properties that must be considered are volume resistivity, water absorption, and susceptibility to piezoelectric and triboelectric effects (see "Three measurement demons"). Table 1 compares these properties for many commonly available insulating materials. Not only is sapphire an excellent choice for its insulating properties, but it provides a rigid mounting surface for the input node. Its performance in the 642 was further enhanced through the use of guarding.

As important as the input device, input protection, and insulation are to the operation of the electrometer is their structural configuration. In the 642's remote head, the input node (Fig. 4) is a rod-like conductor that runs downward from the input connector to the MOS FET input device and its protecting GaP diodes. A guard tube

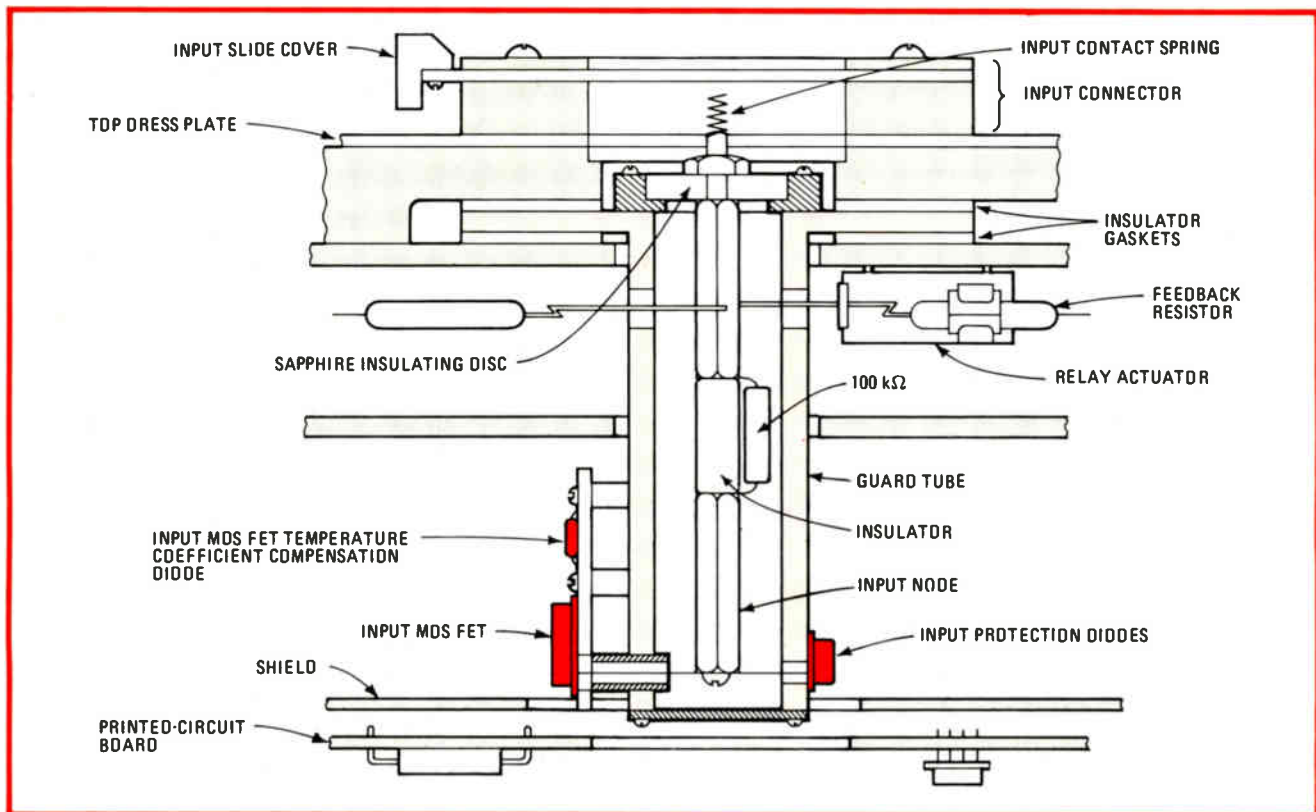
surrounds the conductor coaxially and a sapphire insulating disk supports the conductor at the connector end. The input devices at the opposite end are mounted on the guard tube. Minimizing the volume surrounding the input node reduces the ion-chamber effect caused by background radiation.

Feedback connections are made through holes along the length of the guard tube. Feedback elements are used to convert the input current or charge to a voltage that can in turn be transformed by an analog-to-digital converter into a numerical value for display. The high-value resistors used for current-to-voltage conversion are mechanically supported by their glass enclosure; a special relay mechanically manipulates a lead from the resistors so that it contacts the input node through a hole in the guard tube. Charge-to-voltage conversion is accomplished by connecting a specially constructed sapphire-insulated, air-dielectric capacitor to the node in much the same way as are the high-value resistors. The feedback elements and the relay actuators are mounted radially on two levels along the length of the guard tube and normal to it.

**Avoiding ionization**

The rest of the remote-head electronics are on a printed-circuit board at the bottom of the enclosure; this circuitry is shielded by a metal plate to prevent it from ionizing air in the region around the input node.

Within the realm of low-current measurement, ionizing radiation can be a significant source of error currents. As noted, the susceptible portion of the struc-



**4. Heading off trouble.** Careful design and solid construction of the 642's remote head prevent problems from a number of sources: piezoelectric and triboelectric potentials, electromagnetic coupling, alpha radiation, and vibration, among others.

ture is the air volume between the input node and the guard tube, which in effect forms an ion chamber.

The air ionization along the path of an alpha particle greatly exceeds that caused by any other constituent of background radiation. Since alpha particles will not pass through metals of any appreciable thickness, the only possible alpha sources that can affect measurements are the metals used to construct the node and guard—a fact that has been experimentally verified. Similar sources of low-level radiation have recently been credited with causing soft errors in charge-coupled devices and dynamic MOS memories.

The alpha-particle emissions of various materials have been measured; this data was consulted in designing the 642. Domestic lead produces many alpha particles, but there is no detectable activity above background for cadmium, so cadmium-plated, low-lead brass was used throughout the remote head. Cadmium solder was used in place of tin-lead solder for structural and electrical connections in the vicinity of the input node to further minimize alpha radiation. Other low-alpha materials are gold and silver.

Although thermoelectric potentials do not normally present problems in high-impedance circuits, they can be a factor when operating at high voltage sensitivities. They develop at the junctions of dissimilar metals, a fact that is made use of in thermocouples. The potentials are a function of the metals' properties, their impurities, and the temperature gradient across the junction. Table 2 lists some typical thermoelectric potentials.

With careful mechanical design, these error sources

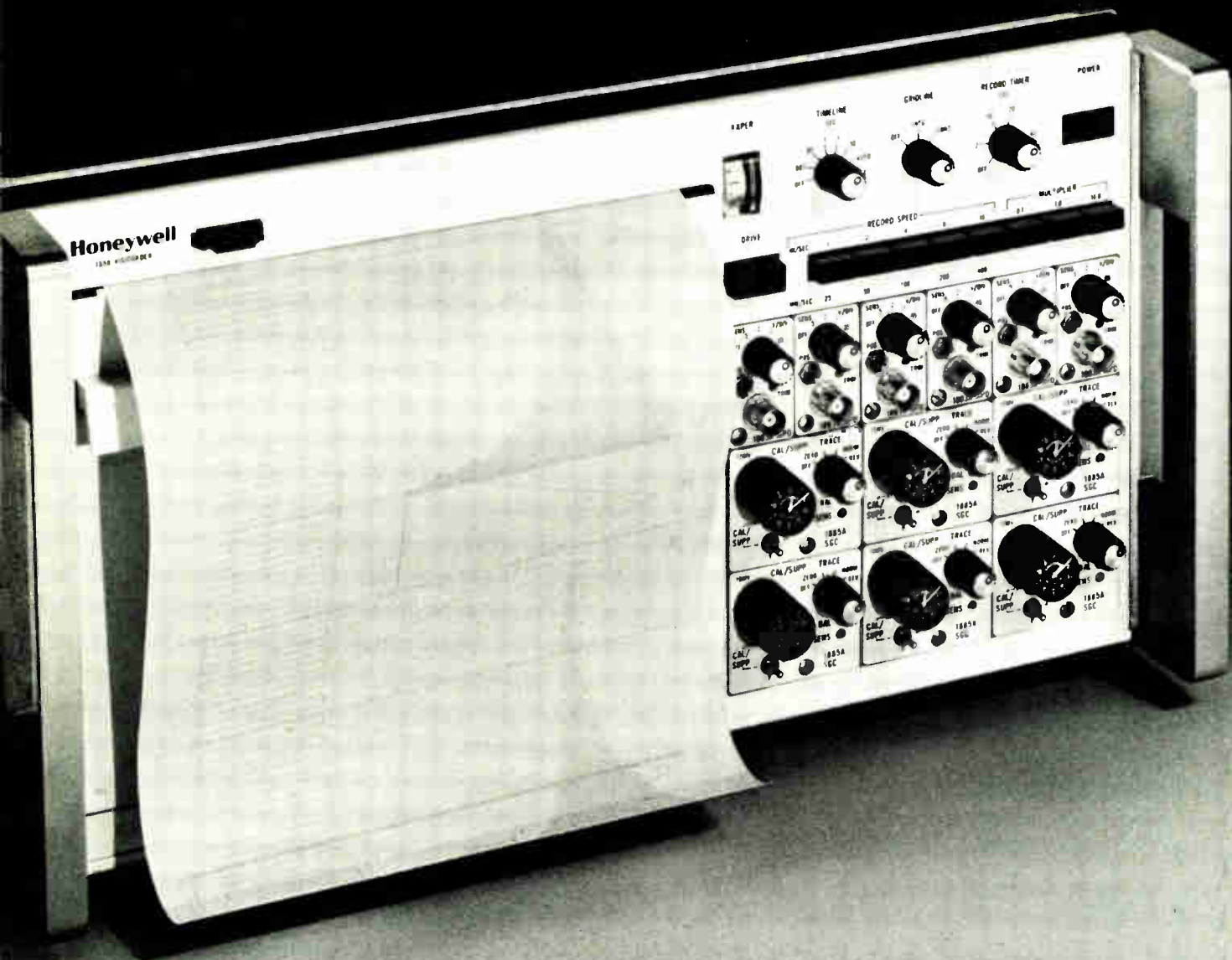
can be reduced or eliminated. When dissimilar-metal junctions cannot be avoided, heat sinks can be arranged so as to reduce the temperature gradient across them.

By dividing an electrometer into a mainframe with the controls and display and a separate remote input head, the sensitive input circuitry can be located directly at the signal source, and the path over which low-level signals must travel can be minimized. This separation also removes the instrument's operator from the measurement environment, where he might inadvertently affect the sensitive circuitry.

### Physical integrity

Rigid construction of all parts of the remote head serves to reduce or eliminate spurious input signals due to vibration or distortion. A sealed environment and an internal, replaceable or rechargeable desiccant help to maintain the integrity of the remote head's internal insulators and high-impedance circuitry. (The external insulators that support the input node must be kept clean since contamination or high humidity may degrade the insulator's surface resistivity or, in the case of contamination by ionic chemicals, weak "batteries" between two conductors may form. The guarded insulator minimizes the effect of shunt resistance in the former case, but has no effect in the latter.)

A contaminant not normally considered is light. At ultralow current levels, photoemission—predominantly from solid-state components—can become significant. For the 642, this problem is addressed by using opaque glass feed-through insulators for such devices' leads. □



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For detailed information on how the Model 1858 might meet your recording needs, call Lloyd Moyer at (303) 771-4700. Or write for technical data sheets on the Model 1858 and our illustrated brochure that describes all of Honeywell's oscillographic recorders, magnetic tape systems and signal conditioning modules. Honeywell Test Instruments Division, Box 5227, Denver, CO 80217.

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# Honeywell



## Telephone tester detects line distortion

by Hector Urbina  
Western Union International, Los Angeles, Calif.

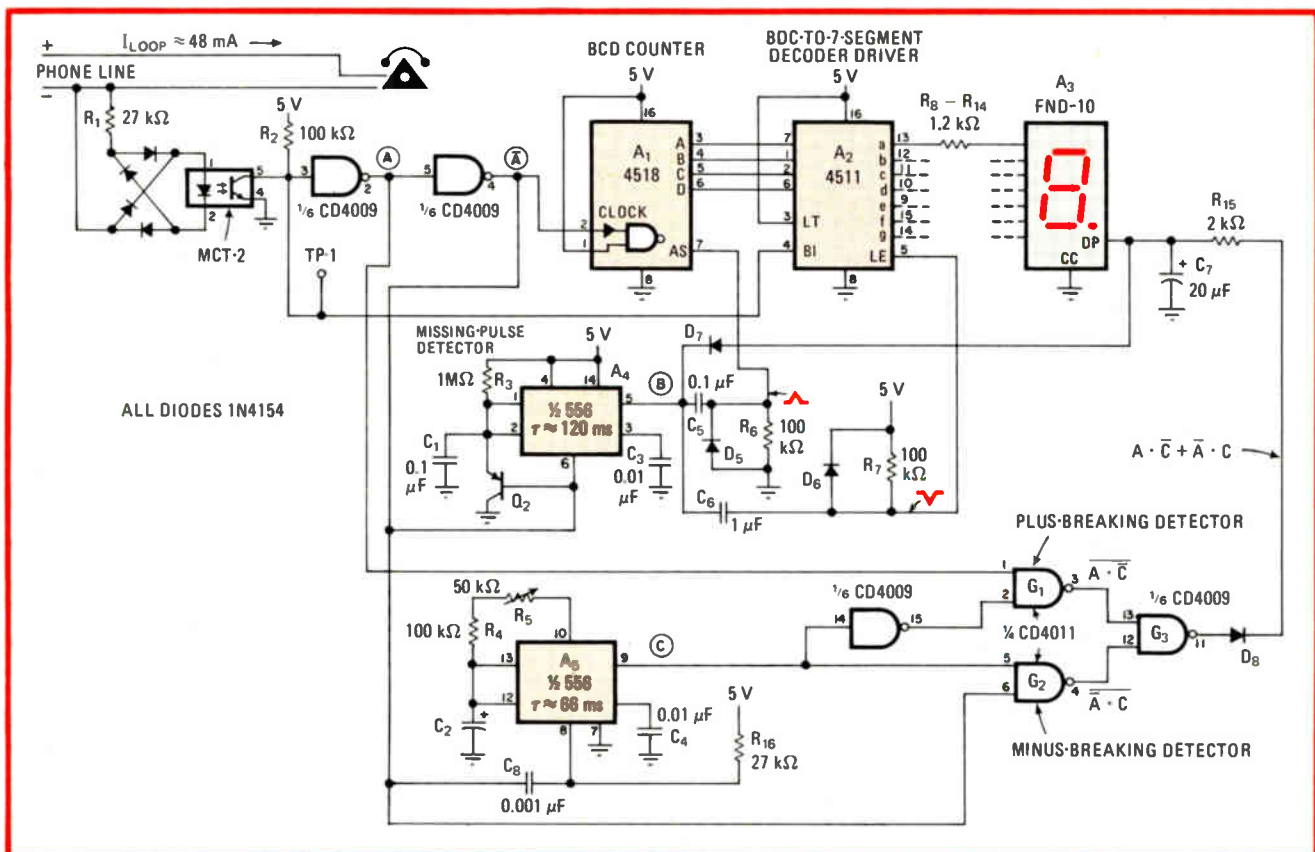
This telephone tester monitors each dial pulse sent along a two-wire telephone line in order to detect the existence of pulse distortion—the ratio of a pulse's break interval to the sum of the make and break times. It is invaluable for checking the signaling parameters of the various rotary-dial systems found in the U. S., since in many cases it can serve as a stand-in for the more sophisticated test sets.

An optically isolated input circuit presents the outgoing pulses to counter  $A_1$  and decoder-driver  $A_2$  so that the number represented by each group of pulses dialed can be displayed by  $A_3$ .  $A_4$  detects the start and end of the pulse train for any particular digit, and differentiators  $R_6C_5$  and  $R_7C_6$  derive positive- and negative-going pulses, respectively, for resetting  $A_1$  and latching  $A_2$ . The numbers displayed can thus be checked against the known numbers dialed to determine if the telephone set,

the line, or points in between are generating faults.

Meanwhile, one-shot  $A_5$  is triggered through  $R_{16}C_8$  for every pulse received.  $A_5$ 's output is used as a reference signal to be compared with the actual break time of the pulses on the line. Note that  $A_5$ 's time constant can be selected over the range of 51 to 77 milliseconds with potentiometer  $R_5$ , so that the unit can be made test-compatible with the system under measurement. Thus, in modern Bell System links (pulse rate of  $10 \pm 0.5$ /second),  $A_5$  is set for an on-time of 58 to 64 ms. For dated Bell links, E & M (receive and transmit) loops, and old switchboards,  $A_5$  assumes the range 59.5 to 67.5 ms. The break times become 57 to 64 ms for E & M senders, and 62 to 66 ms for new switchboard systems.

If the break pulse is wider than the reference signal,  $G_1$  generates a signal whose width is proportional to the distortion; similarly,  $G_2$  generates a corresponding signal if the break is less than the reference. Thus,  $A_2$ 's decimal point will be driven by a current via  $G_3$  if either condition exists. Neither condition necessarily indicates that the distortion is excessive, since the break width can never be expected to be exactly equal to the reference width. Thus, the detector's integrator ( $R_{15}C_7$ ) is designed to pass an average current sufficient to activate the decimal point when the break distortion exceeds about 10%. Note that the distortion measurement is not



**Break boundaries.** Test unit displays numbers generated by rotary-dial telephone and detects dial-up distortion created in systems that generate variations in the nominal make-to-break ratio of dial pulses. Unit monitors signaling parameters of all U. S. standard systems.

affected by the time interval between dialed digits—the interdigital interval.

Several other display or decimal-point conditions may occur during operation, and it is advantageous to know them in order to prevent misinterpretation of the test results. For instance, when the telephone set is on the hook, the display will be off and the decimal point will be

active. A flashing display and decimal point indicate a ring signal on the line. Also, the display may flash if the distortion on the line greatly exceeds 10%.

A square wave having a period of 100 ms and a duty cycle of 50 ms can be injected at test point TP-1 to verify the monitor's performance. The opto-isolator input must be disconnected from the phone line at this time. □

## Calculator notes

# TI-59 performs fast Fourier analysis

by J. G. Willis  
San Diego, Calif.

Employing an algorithm for the fast Fourier transform (FFT) used by Stearns,<sup>1</sup> this TI-59 program determines the spectral-density distribution of many driving functions in a relatively short time. It takes the iterative program no more than 5 minutes to provide an 8- or 16-point representation of the function. In contrast, an analysis using a 16-point Fourier transform would take 15 minutes to complete with the TI-59, and an hour or so to perform by hand.

The program stores the input data as a complex number in bit-reversed order in memories 10 to 25 and 30 through 45, then performs 240 multiplications and additions to find the FFT. Given the number of points and the sampling interval, the program will pause to display the column and value of each node through the algorithm before halting at node 10. Pressing the R/S key successively yields the real and imaginary components at all points.

Consider the elementary example of an input ramp

that increases from 0 to 2 volts in increments of 0.5 v every 0.02 s, then levels off thereafter, as shown in the figure. Input data to the program is introduced in the locations following the LBL C entry. Thus, 0.5 STO 11, 1 STO 12, 1.5 STO 13, 2 STO 14, STO 15, GO \*E, are keyed in.

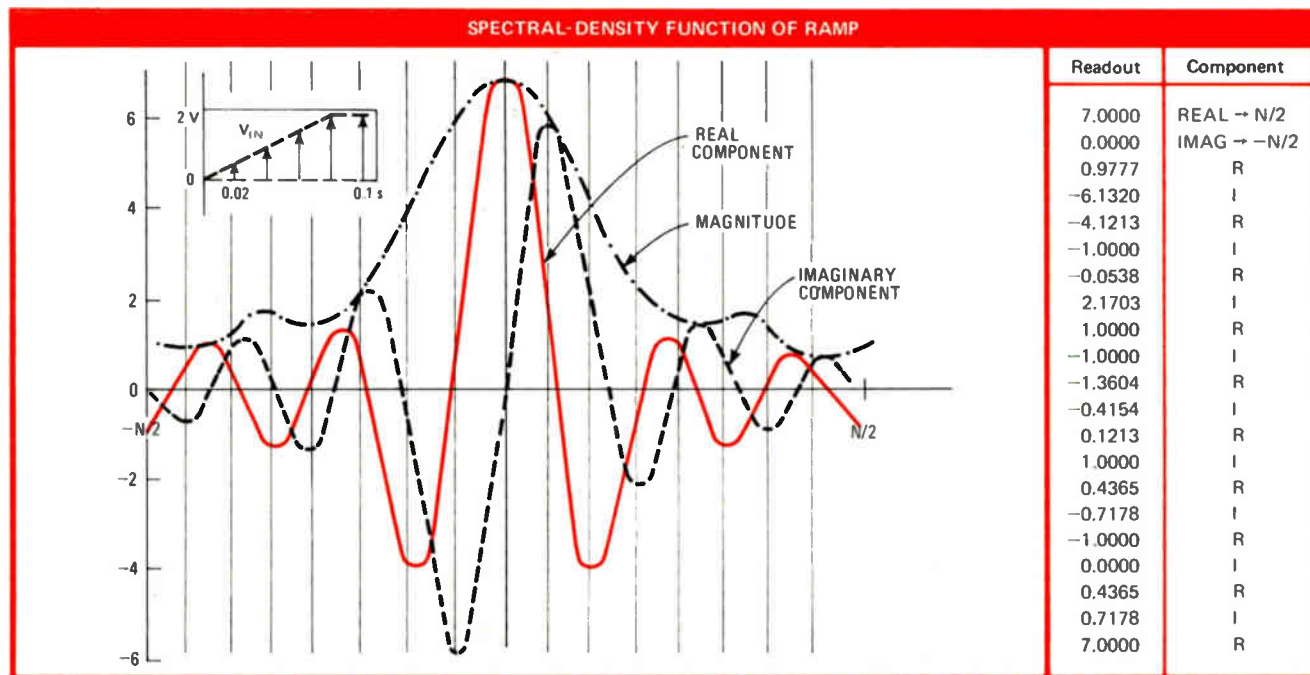
Entering the number of desired points, N; the sampling interval,  $\tau$ ; the measurement interval, N/2; and the column index,  $\gamma$  (in this case, 16, 0.0013, 8, and 4, respectively) in registers A, B, D, and \*D, respectively, as instructed will yield the curve shown, obtained from the program's tabulated results. Note that the real components are tabulated from the origin toward the N/2 point, whereas the imaginary components proceed from the origin along points towards  $-N/2$ ; in any case, however, the curve is symmetrical, so that the points not tabulated can be readily plotted. Note also that the real components of the transform are found in locations 10 through 25 for each successive point, with the imaginary parts found at locations 30 to 45.

In addition, the program has sufficient space available to specify a continuous waveform directly. For example, consider the waveform  $e^{-t} \sin t$ , which is programmed under LBL C as shown in the coding. □

### References

1. Sam D. Stearns, "Digital Signal Analysis," Hayden Publishing Co., 1975.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.



PRINTER LISTING: TI-59 PROGRAM FOR FAST FOURIER TRANSFORMS

000	LBL	061	X	122	(	183	(	244	X = T	305	17	366	RCL
001	A	062	$\pi$	123	RC*	184	RCL	245	RCL	306	RCL	367	15
002	STO	063	$\div$	124	58	185	27	246	02	307	21	368	R/S
003	05	064	RCL	125	X	186	-	247	GE	308	EXC	369	RCL
004	R/S	065	07	126	RCL	187	RCL	248	COS	309	23	370	35
005	LBL	066	)	127	54	188	29	249	(	310	STO	371	R/S
006	B	067	STO	128	+	189	)	250	RCL	311	21	372	RCL
007	STO	068	52	129	RC*	190	ST*	251	07	312	RCL	373	16
008	03	069	LBL	130	59	191	59	252	$\div$	313	10	374	R/S
009	RAD	070	E	131	X	192	1	253	2	314	GTO	375	RCL
010	FIX	071	RCL	132	RCL	193	SUM	254	Yx	315	B'	376	36
011	04	072	02	133	55	194	56	255	(	316	LBL	377	R/S
012	R/S	073	PAU	134	)	195	SUM	256	RCL	317	A'	378	RCL
013	LBL	074	(	135	STO	196	04	257	01	318	RCL	379	17
014	D	075	RCL	136	28	197	RCL	258	-	319	11	380	R/S
015	STO	076	56	137	(	198	09	259	RCL	320	EXC	381	RCL
016	07	077	PAU	138	RC*	199	X = T	260	02	321	14	382	37
017	1	078	+	139	59	200	RCL	261	)	322	STO	383	R/S
018	STO	079	2	140	X	201	04	262	)	323	11	384	RCL
019	09	080	0	141	RCL	202	GE	263	STO	324	RCL	385	18
020	STO	081	)	142	54	203	SIN	264	09	325	13	386	R/S
021	02	082	STO	143	-	204	GTO	265	RCL	326	EXC	387	RCL
022	1	083	57	144	RC*	205	00	266	02	327	16	388	38
023	0	084	(	145	58	206	71	267	1	328	STO	389	R/S
024	STO	085	(	146	X	207	LBL	268	0	329	13	390	RCL
025	56	086	RCL	147	RCL	208	SIN	269	STO	330	RCL	391	19
026	R/S	087	56	148	55	209	0	270	56	331	10	392	R/S
027	LBL	088	+	149	)	210	STO	271	GTO	332	GTO	393	RCL
028	D'	089	RCL	150	STO	211	04	272	00	333	B'	394	39
029	STO	090	09	151	29	212	(	273	34	334	LBL	395	R/S
030	01	091	)	152	(	213	RCL	274	LBL	335	COS	396	GTO
031	R/S	092	STO	153	RC*	214	05	275	E'	336	RCL	397	COS
032	LBL	093	58	154	56	215	+	276	RCL	337	10	398	LBL
033	B'	094	+	155	STO	216	9	277	11	338	R/S	399	C
034	(	095	2	156	51	217	-	278	EXC	339	RCL	400	
035	(	096	0	157	+	218	RCL	279	18	340	30	401	
036	2	097	)	158	RCL	219	09	280	STO	341	R/S	402	
037	Yx	098	STO	159	28	220	)	281	11	342	RCL		
038	(	099	59	160	)	221	X = T	282	RCL	343	11		
039	RCL	100	(	161	ST*	222	RCL	283	12	344	R/S		
040	01	101	(	162	56	223	56	284	EXC	345	RCL		
041	-	102	RCL	163	(	224	GE	285	14	346	31		
042	RCL	103	56	164	RCL	225	TAN	286	STO	347	R/S		
043	02	104	-	165	51	226	RCL	287	12	348	RCL	462	GTO
044	)	105	1	166	-	227	09	288	RCL	349	12	463	C
045	+	106	0	167	RCL	228	SUM	289	13	350	R/S	464	LBL
046	RCL	107	)	168	28	229	56	290	EXC	351	RCL	465	EE
047	05	108	X	169	)	230	GTO	291	22	352	32	466	0
048	)	109	RCL	170	ST*	231	00	292	STO	353	R/S	467	STO
049	EE	110	52	171	58	232	71	293	13	354	RCL	468	00
050	INV	111	)	172	(	233	LBL	294	RCL	355	13	469	STO
051	EE	112	STO	173	RC*	234	TAN	295	15	356	R/S	470	10
052	INV	113	53	174	57	235	1	296	EXC	357	RCL	471	1
053	INT	114	COS	175	STO	236	SUM	297	20	358	33	472	6
054	X	115	STO	176	27	237	02	298	STO	359	R/S	473	X = T
055	RCL	116	54	177	+	238	(	299	15	360	RCL	474	RCL
056	05	117	RCL	178	RCL	239	RCL	300	RCL	361	14	475	05
057	)	118	53	179	29	240	01	301	17	362	R/S	476	GE
058	(	119	SIN	180	)	241	+	302	EXC	363	RCL	477	E'
059	STO	120	STO	181	ST*	242	1	303	24	364	34	478	GTO
060	06	121	55	182	57	243	)	304	STO	365	R/S	479	A'

↑ Input data  
↓

Input data coding for $f(t) = e^{-t} \sin t$			
400	(	416	SIN
401	(	417	)
402	RCL	418	STO
403	00	419	52
404	X	420	(
405	RCL	421	RCL
406	03	422	00
407	)	423	+
408	STO	424	1
409	51	425	0
410	+/-	426	)
411	INV	427	STO
412	LNx	428	10
413	X	429	RCL
414	RCL	430	52
415	51	431	ST*
432	10		
433	1		
434	SUM		
435	00		
436	(		
437	RCL		
438	05		
439	-		
440	1		
441	)		
442	X = T		
443	RCL		
444	00		
445	GE		
446	EE		

- | Instructions   |
|--|
| • Key in program   |
| • Enter function to be analyzed (input data is entered following LBL C)  |
| • Specify number of transform points, sample interval, measurement interval, and accuracy factor:<br>$(N), A, (\tau), B, (N/2), D, (\gamma), *D$ |
| • Press C to run   |

## Using flat-cable terminals as connectors for conductive inks

The circuits for one of the most popular low-cost keyboards are so simply put together that you'd think it would be easy to connect to them. But it's not so. Inexpensive conductive inks are screened onto a Mylar substrate or film to lay down the circuit pattern. The film is then folded over so the two halves of each switch face each other but are separated by a spacer with holes. When the user presses a switch, the two sides of the folded film touch through the hole, thus closing the circuit. The problem in connecting external wires to the switch array is that the **conductive inks are so thin that soldering may cause breakage.**

AMP engineers have solved that problem by adapting one of their standard flat-cable machines to make economical connections to conductive-ink switches. They drive a proven flat-cable insulation-displacement terminal through the plastic film to crimp it onto the conductive-ink path and create a rugged switch-to-board interface. For more information about this method, write to AMP Inc., Harrisburg, Pa. 17105.

## Custom LSI—learn when to make it or buy it

If you are interested in designing and manufacturing a set of custom large-scale integrated circuits for one of your company's products, but you are not sure just how to go about it, there's a 155-page report that can help you weigh the alternatives. The report by Anderson and Bogert, "Vertical Dis-Integration," **explores and compares three approaches to gaining LSI capability:** by developing it internally, by acquiring a company that already has the capability, or by having a specialty firm custom-make the LSI. Included in the report are excellent marketing profiles of all current custom and semi-custom LSI firms.

You can get your copy of the \$475 report from Electronics Trend Publications, 10050 North Wolfe Rd. SW 3, Suite 3200, Cupertino, Calif. 95014, or call (408) 996-7401.

## Primer gives principles of parallel-mode high-density recording

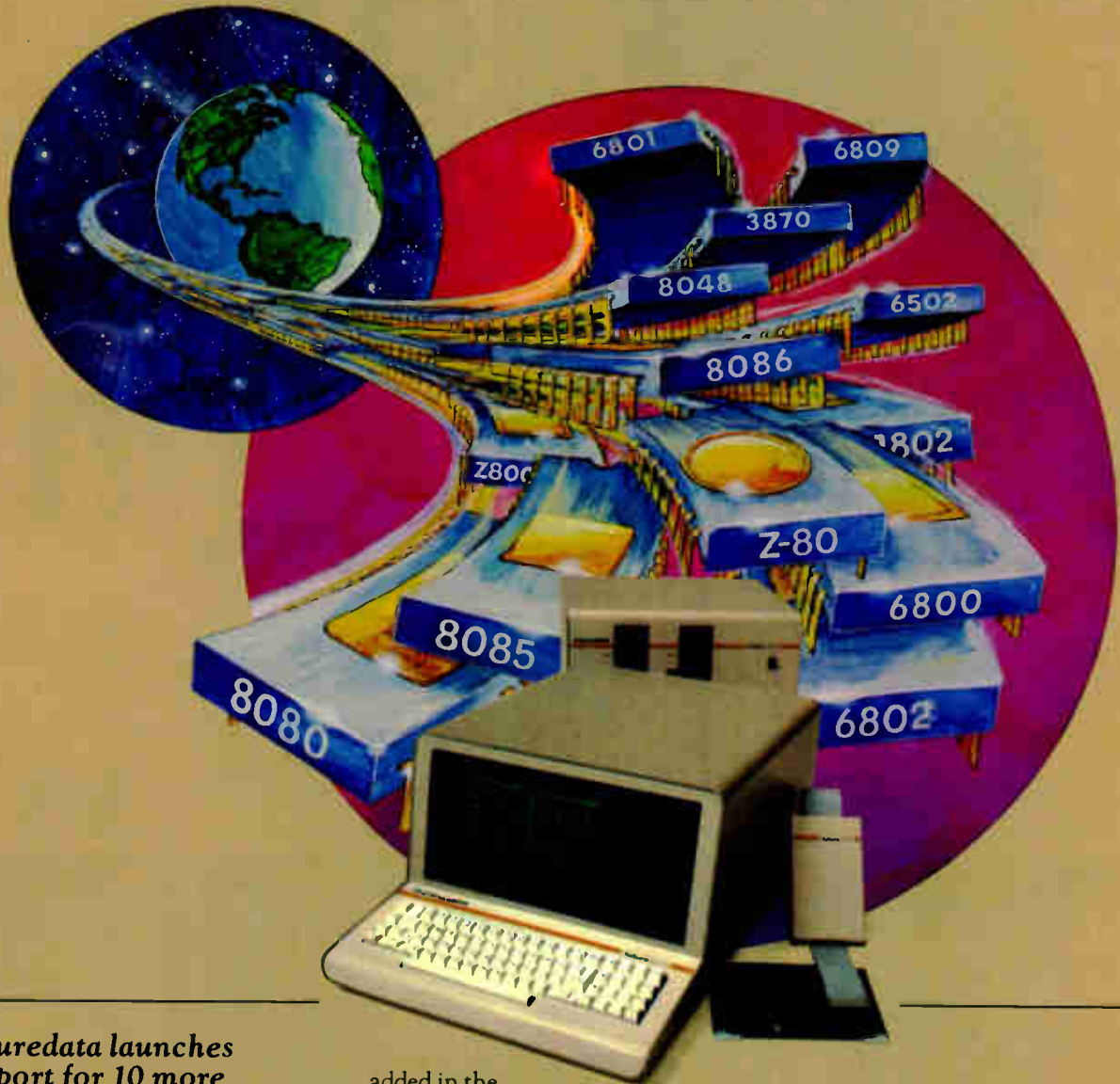
With parallel-mode high-density digital recording, it is possible to record huge quantities of binary digital information on magnetic tape at throughput rates that can climb as high as 100, 300, or even 600 megabits/s. Until recently, engineers unsuccessfully tried to scale those heights by updating an old technique: they have been working at optimizing the digital performance of existing analog recorders, and they have had rather less than satisfactory results.

The impasse was broken by the development of **data-encoding schemes that overcame the analog tape recorder's inherent shortcomings**, permitting, among other things, automatic bit-error detection and correction techniques to be implemented economically, thus ensuring maximum data integrity. Three such encoding schemes have recently come into commercial use, including one known as Enhanced-NRZ.

A primer on similar encoding techniques has been published by Bell & Howell Datatape division. Entitled "Parallel-Mode High-Density Recording—Technical Fundamentals," the 88-page book is intended for the engineer who is somewhat familiar with the principles of magnetic-tape recording, but who has no prior experience with high-density digital recording techniques. The book is available from the company in Pasadena, Calif., for \$15.

-Jerry Lyman

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Circle 155 on reader service card

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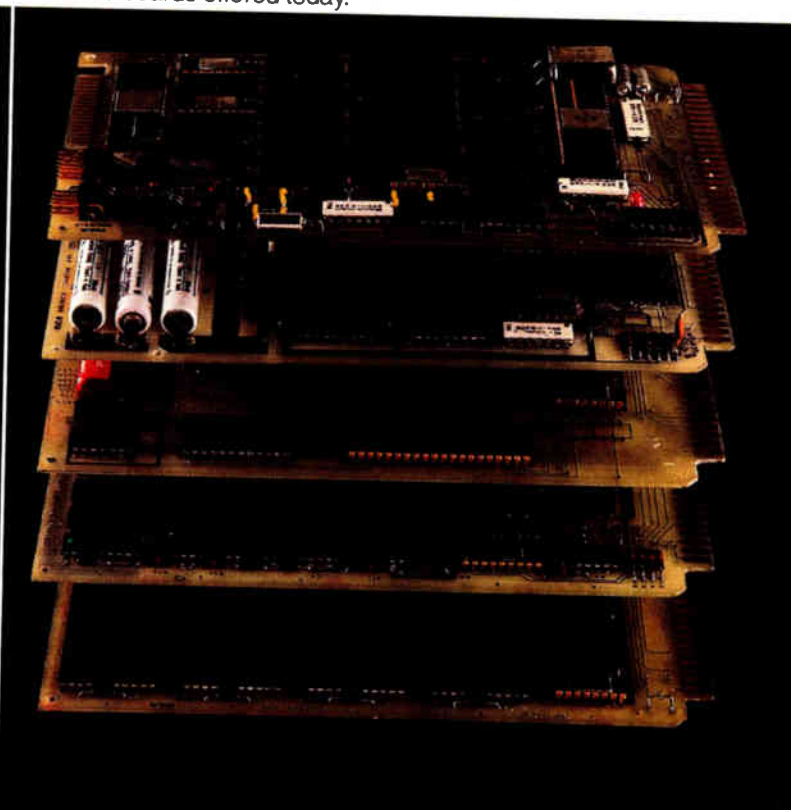
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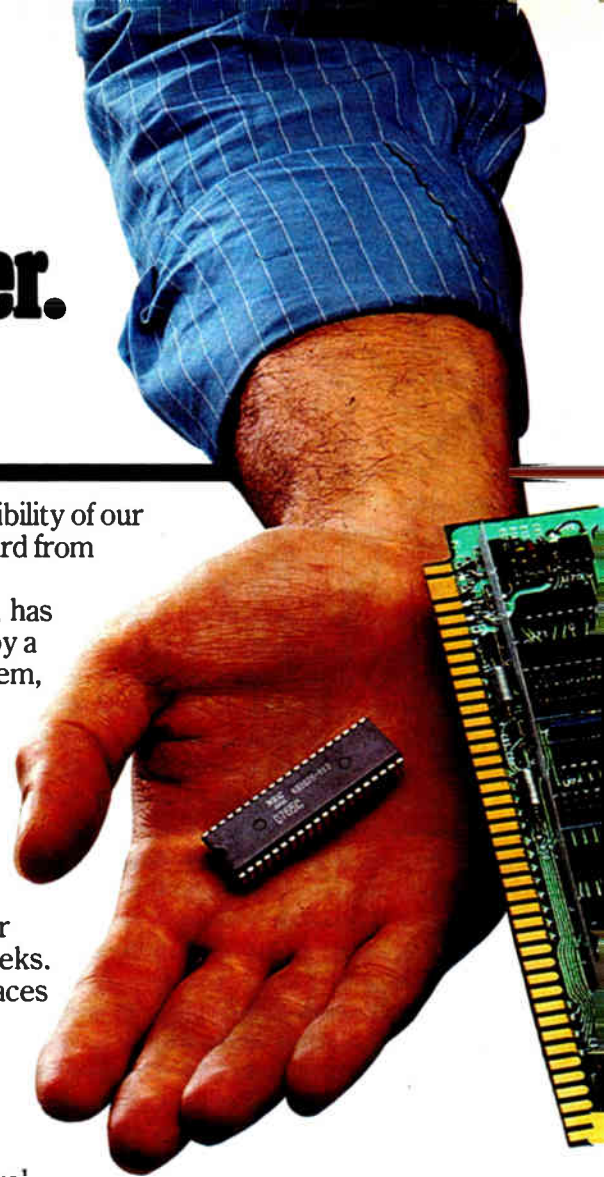
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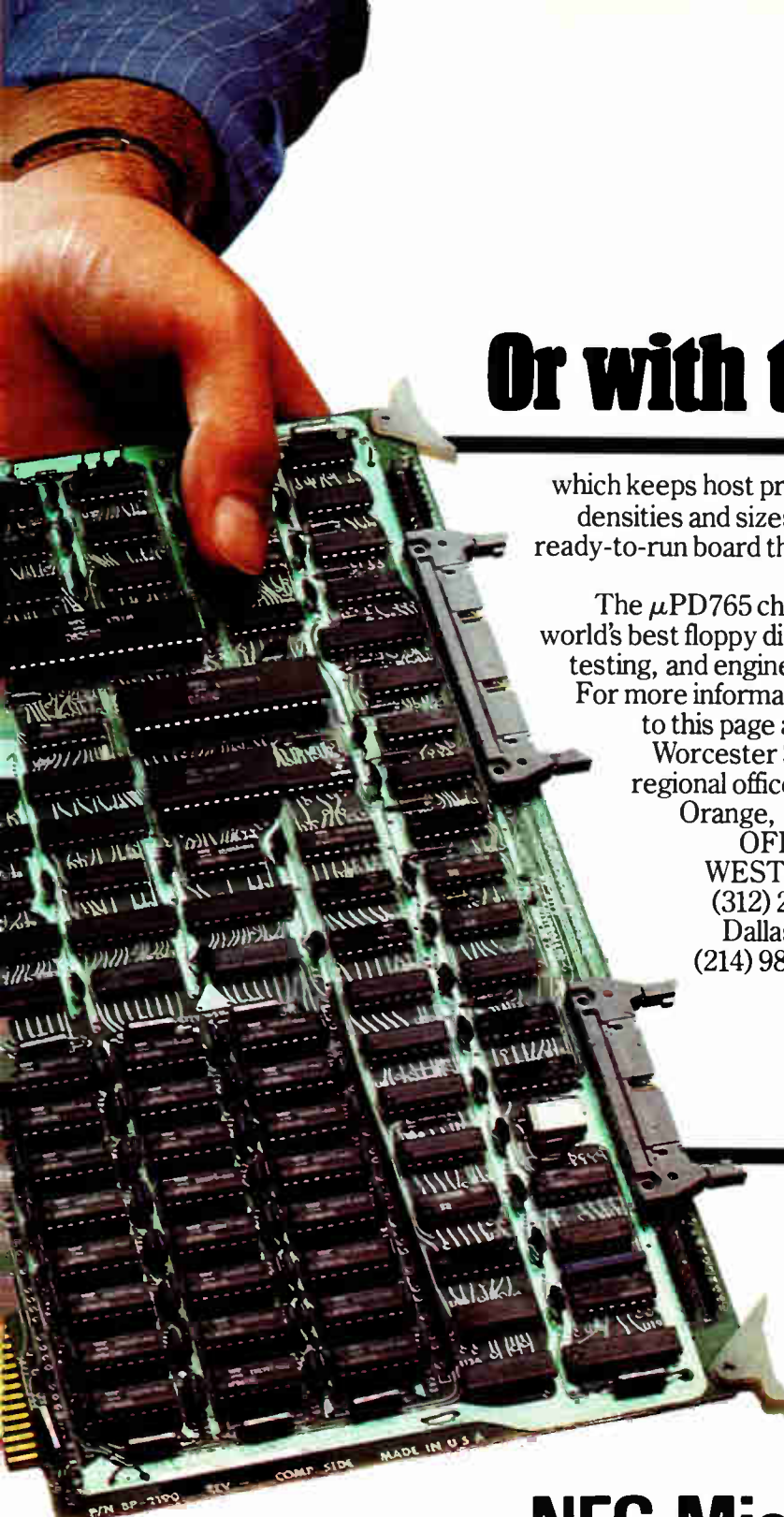


**Controller Chip** REPS: Action Unlimited, Arlington, TX, Spring, TX; Cerco, San Diego, CA; Contact Sales, Inc., Burlington, MA; D/Z Associates, Inc., Denver, CO; Electronic Innovators, Inc., Minneapolis, MN; Eltron, Phoenix, AZ; HLM Assoc., Torrington, CT, Northport, NY, Parsippany, NJ; Imtech, Inc., Cleveland, OH, Dayton, OH; K-Mar Engineering & Sales, Inc., Grandview, MO; Kaytronics Limited, Ville St. Pierre, QUEBEC, Concord, ONTARIO, Surrey, BRITISH COLUMBIA; L & M Associates, Pikesville, MD, Montpelier, VA; Harry Nash Associates, Willow Grove, PA; R.C. Nordstrom & Company, Lathrup Village, MI; Perrott Associates, Inc., Fort Lauderdale, FL, Clearwater, FL, Orlando, FL; Santana Sales, Costa Mesa, CA; Stone Component Sales, Waltham, MA; Technology Sales, Inc., Palatine, IL; Trident Associates, Inc., Sunnyvale, CA; Tri-Tronix, Albuquerque, NM; Tri-Tronix, NW., Mercer Island, WA; 20th Century Marketing, Inc., Huntsville, AL, Knoxville, TN; Wolff's Sales Service Company, Raleigh, NC.

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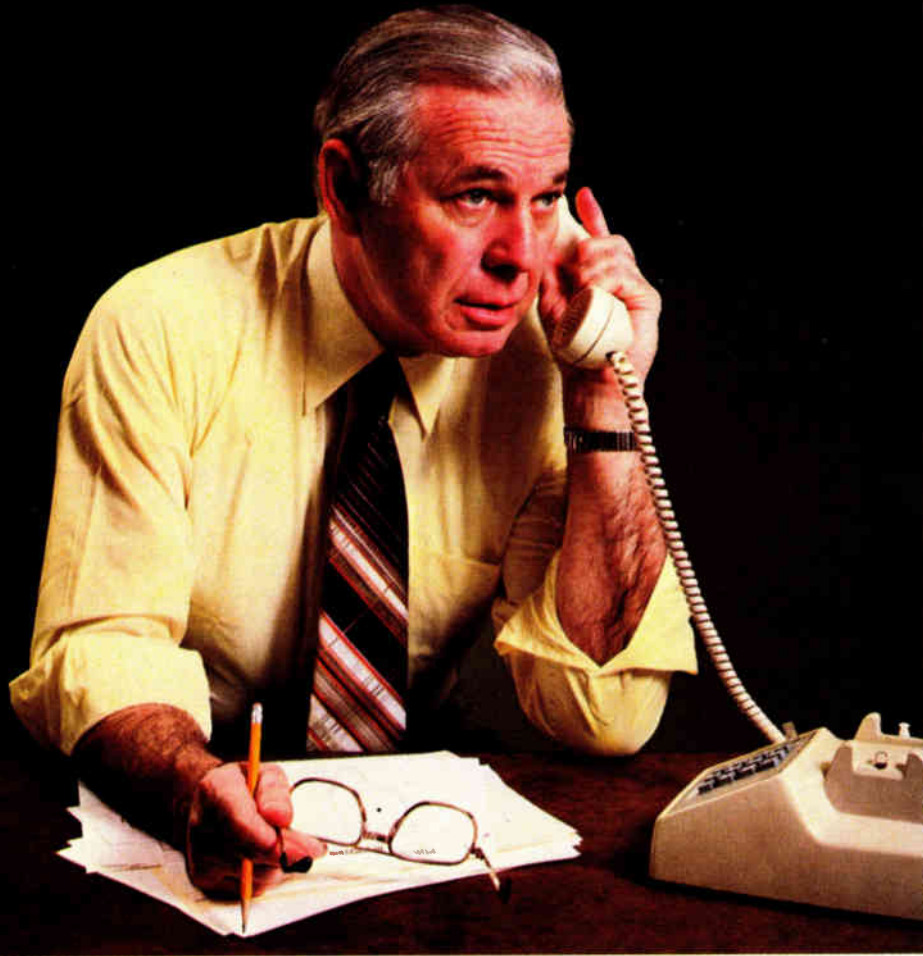
# NEC

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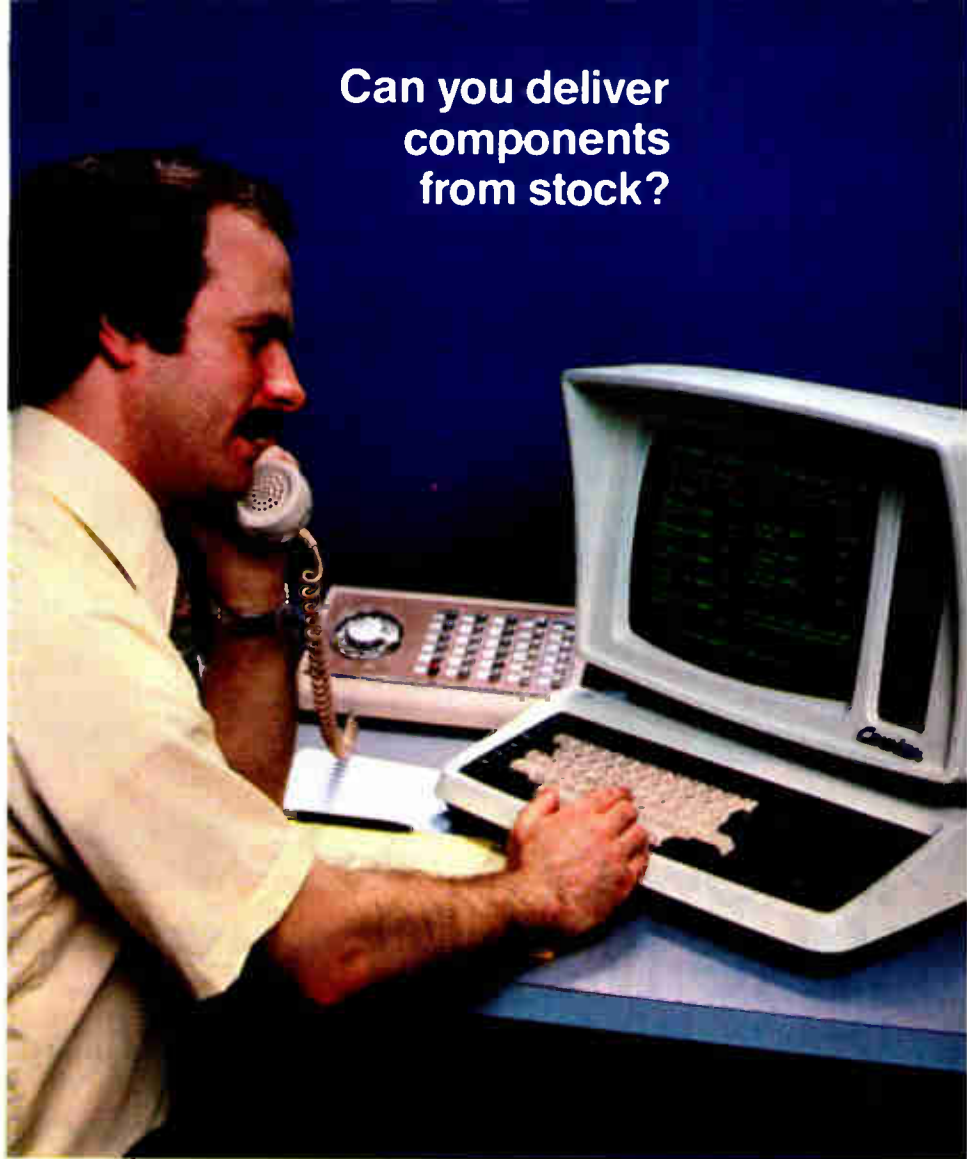
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Earlier, Mariner space probes took long-distance shots that revealed a terrain with towering volcanoes, some perhaps still active. At least one three times as high as Mount Everest.

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# ELECTRONICS

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*and we will continue to make a name for ourselves.*

Circle 167 on reader service card

# 12-bit d-a converter sells for \$9.95

Glass-filled-epoxy package is about 20 times cheaper than conventional hybrid-circuit housings, and it is tough

by James B. Brinton, Boston bureau manager

The most costly part of a hybrid circuit is often the package, according to Hybrid Systems Corp., which set out to change this state of affairs about a year ago. The first fruit of that effort is its DAC9356, a complete 12-bit digital-to-analog converter with a combination of tight specifications, high reliability, and a low price tag of \$9.95 in 1,000-unit lots.

If the price-performance ratio is attractive, the package is responsible. Built of glass-filled epoxy, the new package is being patented by Hybrid Systems, and it appears to be tough, as well as inexpensive. According to G. James Estep, manager of advanced development, the packaged converters easily pass tests like:

- Thermal cycling and shock, 0° to 85°C.
- Military leak testing at a gage pressure of 60 psi.
- 1,000-hour burn-in.
- Installation, removal, reinstallation, etc., on printed-circuit boards.

tion, etc., on printed-circuit boards.

- The dishwasher and Calgon test.
- Pressure-bomb, dye-penetrant tests.

In addition to standard industry and military tests, the units have also been subjected to some more inventive ones. Hybrid Systems executives towed several 9356s behind a sailboat during a Cape Cod vacation without a failure.

If this seems extreme, Estep points out that some commercial environments are tougher in their own way than many military ones. Under a car hood, for instance, devices will encounter wetness, hydrocarbons, battery acid, and wide temperature swings, yet reliability must be high.

A product also must come cheaply if it is to get into such applications in the first place. That is why the low cost of the package is so important, says Estep. "A typical package for commercial hybrid circuits can cost several dollars to start with, and by

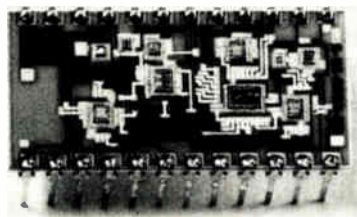
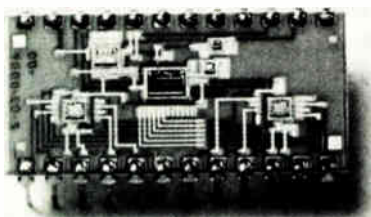
the time you've rejected some at incoming inspection, taken the unavoidable yield losses, and added labor and other factors, you wind up with an overall package cost of \$15 to \$20. At the same point in the production cycle, our new package costs less than 75¢. . . . Factoring this into our production, we can save about \$20 or \$25 per device just through the move to the new package," he says.

The price difference between Hybrid's almost identical DAC356—offered in high-reliability and military-specification versions—and the new DAC9356 illustrates this savings. In lots of 1 to 24, the 356 is priced at \$57 to \$126 while the DAC9356, in identical lots, runs from \$16.50 to \$19.95. And Estep adds that the price is no come-on for it is a true stock part.

The new package buys even more, according to Estep. "For a given package size we can pack in more substrate area than is possible with other packages. The new package also helps make our production process more uniform and that raises yield. Finally, if a part fails inspection or test, our investment in parts is low enough that we can afford to throw it away rather than rework it to save the costly package. That also helps drive the price down."

Despite its low price, the 9356 is not a "cheap" product. It is a complete unit with an internal, temperature-compensated voltage reference; a laser-trimmed thin-film resistor ladder; an output amplifier; and switches. No external components are necessary.

The device's 12-bit resolution is backed by an initial accuracy of





# ENLIGHTENMENT

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## Now, a power to logic optical interface that monitors AC line status

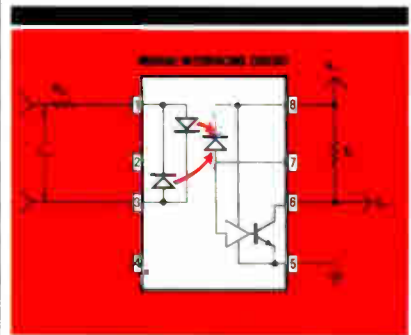
**General Instrument's MID400.** It's the first optically isolated interface to have direct operation from an AC line current and direct compatibility to TTL and microprocessor systems. Not only do you get a device with direct interface from line voltages ranging from 24V to 240V, but one with externally adjustable time delay and AC voltage sensing. Add to that . . . logic level compatibility and high isolation between input and output.

**A system sentry with motor to logic capability.** The MID400 is the perfect answer to monitoring AC "line down" conditions. When the power goes, the MID400 can activate auxiliary power control. In industrial control applications, the MID400 is an ideal "closed loop" interface between electro-mechanical elements such as solenoids, relay contacts, small motors and microprocessors. This closed loop capability may also

be utilized in emergency shut down or fail safe applications. And if your system needs an AC current status monitor, a 2 or 3-phase power line status monitor, telephone ring detector or a low speed, high gain optocoupler interface, there's no better device than the MID400.

**Low power . . . low current.** AC line voltage is monitored by two back-to-back GaAs LED diodes in series with an external resistor. A very high gain detector circuit senses the photodiode current and drives an open collector transistor to a logic low condition.

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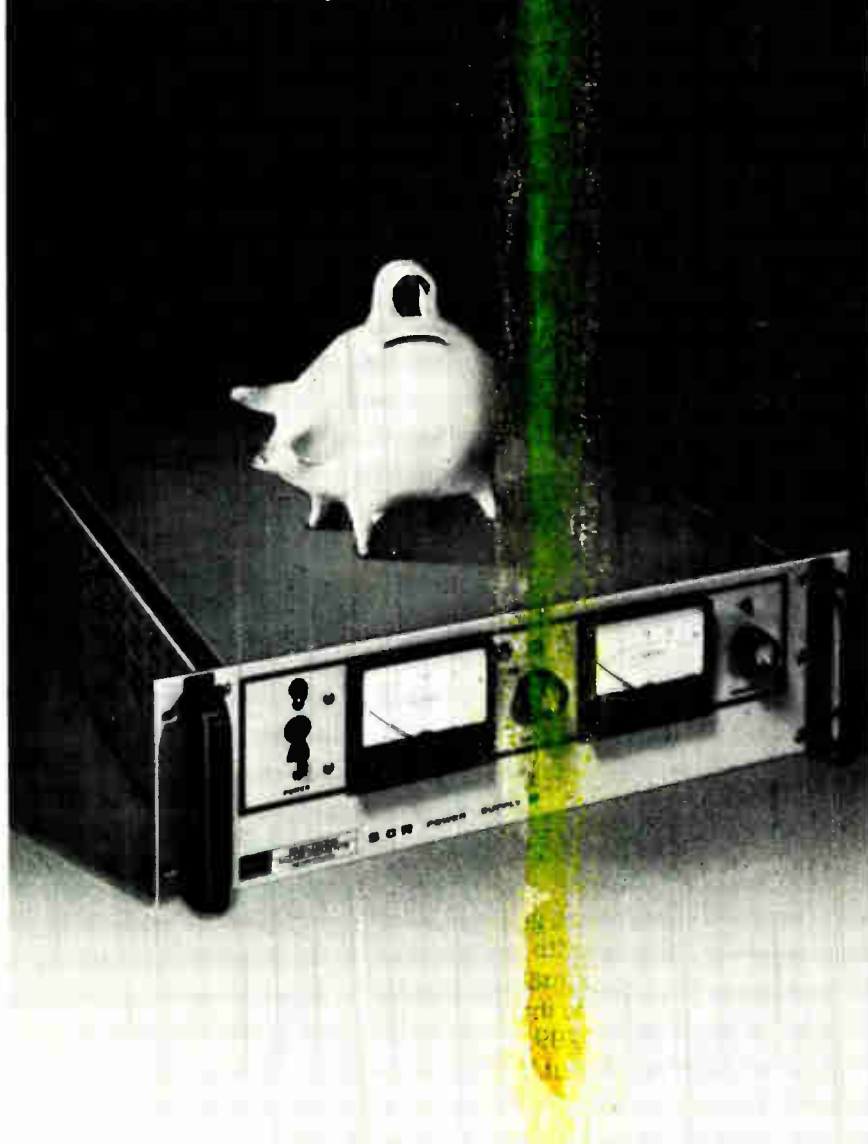
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Delivery of the DAC9356 is from stock to four weeks.

Hybrid Systems Corp., Crosby Drive, Bedford, Mass. 07103 Phone (617) 275-1570 [339]

### More to come . . .

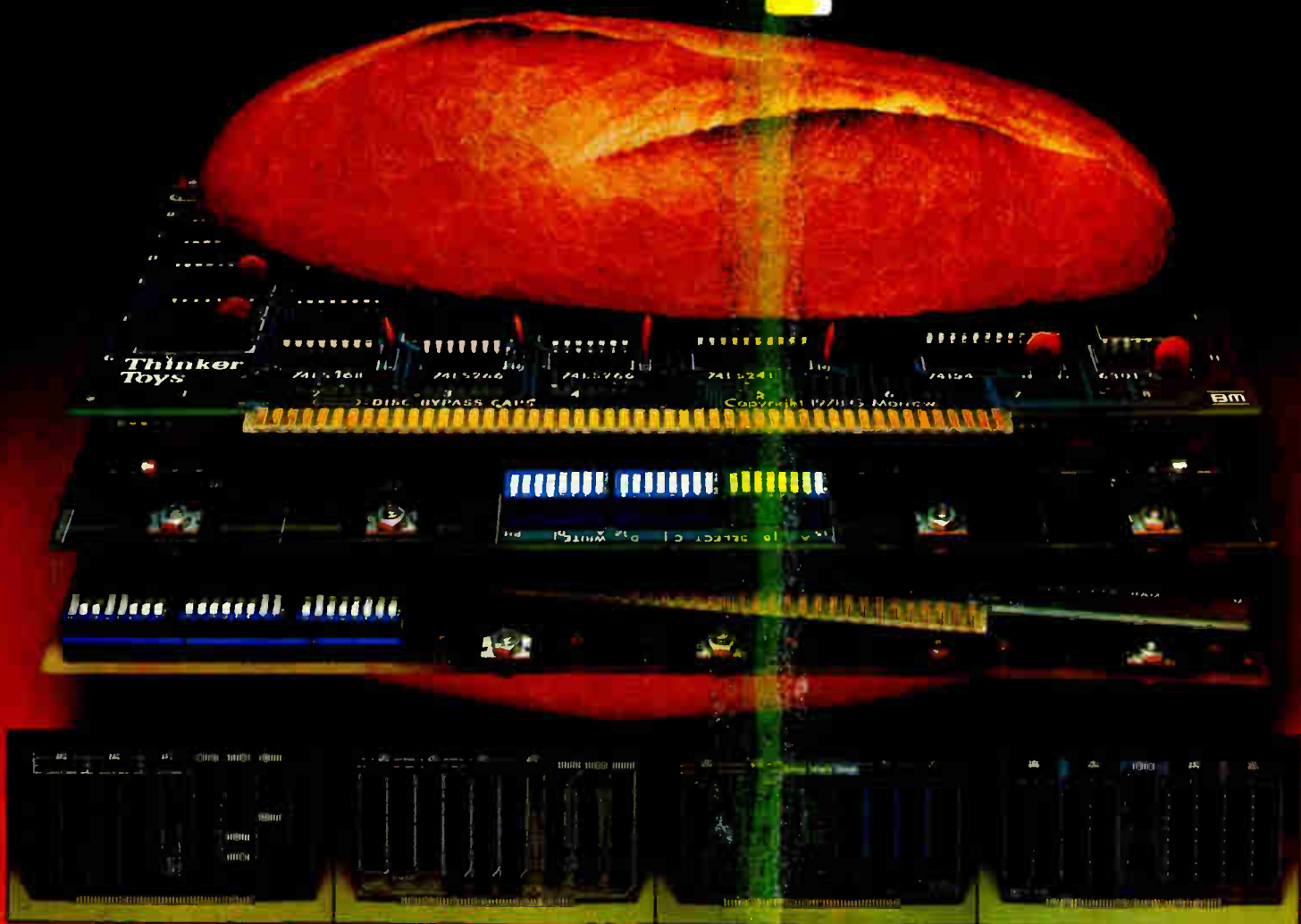
The DAC9356 is only the first in a wave of low-cost products that Hybrid Systems will introduce in the near future. Due almost immediately is the DAC9349, a 12-bit converter with multiple output ranges, tighter drift specifications than those of the 9356, and a higher power-supply rejection ratio. It is offered with either a binary-output or a three-decade binary-coded decimal output and should be available in October.

Coming next is the 9331-14, a multiplying converter with "real 14-bit accuracy and linearity," according to Hybrid's Estep, who claims that the competition has less linearity than resolution. Hybrid should begin sampling the 9331 in October.

These will be more costly products than the 9356; though price has not been firmly set as yet, Estep estimates that for lots of 1,000, \$25 is a good ballpark figure.

Estep cheerfully gives the impression that almost all of Hybrid's high-reliability line will eventually be encapsulated in the new low-cost package. If that's the case, the move should bring a number of very high-performance products with extreme reliability within the reach of the consumer electronics manufacturer.

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MM16K/\$349 = 2.1¢

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For the Gemini series, in 1965-66, Motorola developed and produced the spacecraft's digital command system.

Neil Armstrong's historic "one small step for man" was



# PICTURES OF THE GIANT.

relayed from Moon to Earth in 1969 by a Motorola S-band transceiver.

In 1971 the Lunar Rover, first car on the Moon, had a Motorola FM receiver.

The first color photographs from the surface of Mars, in 1976, came to Earth from the Viking orbiter via Motorola equipment.

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## MOTOROLA

**Making electronics history since 1928.**

# Motorola introduces 64-K E-PROM

Device uses single 5-V supply, is housed in 24-pin package, dissipates only 500 mW when activated, and sells for \$164 in 100s

by Wesley R. Iversen, Dallas bureau manager

Though single-supply 64-K read-only memories have been available from a number of manufacturers for more than a year, debugging for systems using those parts has required a bit of ingenuity due to a lack of erasable programmable ROM parts with comparable 65,536-bit densities. Typically, four 16-K E-PROMs have been used in conjunction with an adaptor socket or other mechanism for 64-K ROM program debugging.

Now comes the MCM68764/68A764, a 64-K E-PROM from Motorola Inc. that will simplify the debugging process. As the first

single 5-v supply 64-K E-PROM to be formally introduced, the 68764 will be housed in a 24-pin package with a pinout matching the industry standard for 16-K, 32-K, and 64-K ROMs [*Electronics*, Sept. 13, p. 215]. Thus, the 68764 can be debugged simply by being plugged into the 64-K ROM socket on a production board. Upgrading systems designed for 16-K and 32-K parts will also be easier.

Indeed, Motorola is counting on this E-PROM and ROM interchangeability with the 64-K level to help the 68764 compete against 64-K E-PROMs expected later from Intel

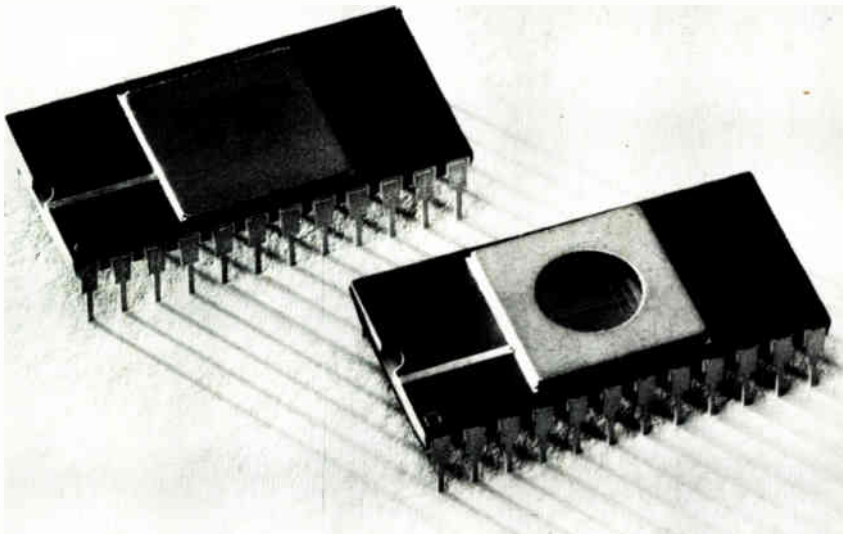
and Texas Instruments. With an eye toward the next generation, both of those firms are planning to house their 64-K E-PROMs in 28-pin packages, though each will use a different pinout.

Motorola squeezed the 68764 into a 24-pin package by giving pin 20 two functions. During programming, the required 25-v pulses are applied through pin 20. While in normal operation, pin 20 serves the chip-enable function with automatic standby power-down when the chip is deactivated. According to Peter Bagnall, marketing manager for MOS memories in Motorola's integrated-circuit operation in Austin, Texas, the 68764 will dissipate about 500 mW in its active mode, with standby power dissipation dropping to about 100 mW. With a die size of about 60,000 mil<sup>2</sup>, the Motorola part is organized as 8 K by 8 bits, Bagnall says.

The 68764 is specified for a 450-ns access time. Samples will be available during the fourth quarter of this year, priced at \$164 in 100-unit quantities, according to Motorola officials. The 68A764, which has a 350-ns access time, is expected in smaller quantities than the slower part, but will also be available during the fourth quarter, priced at \$196 in units of 100.

In addition to the 64-K device, Motorola also plans to supply samples of fully specified 5-v-only 16-K E-PROMs during the fourth quarter as well. A compatible 32-K E-PROM is to be available in the first quarter of next year.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6000 [340]





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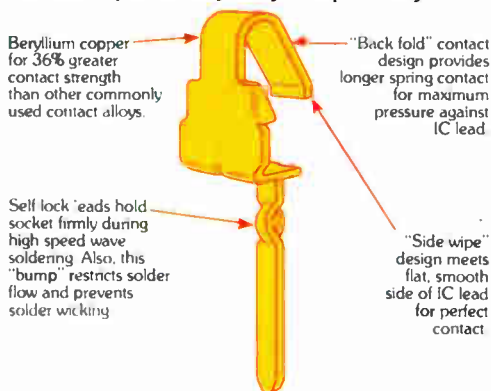
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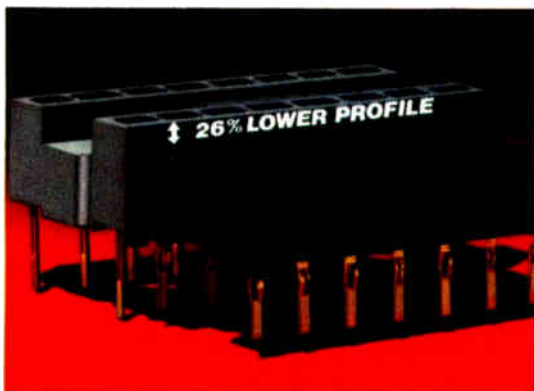


# DEBUNKS

## low profile DIP socket MYTH

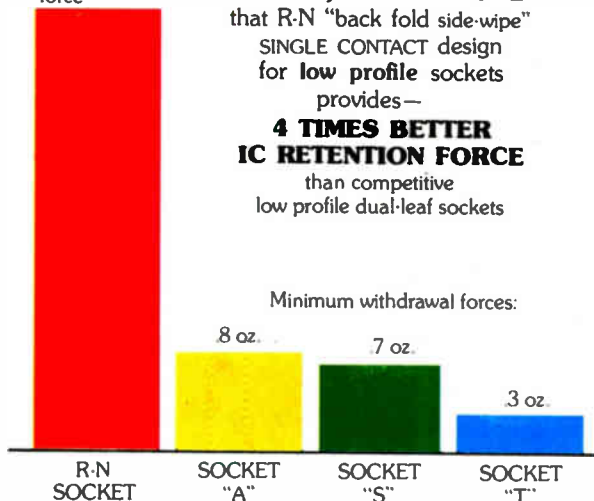
**“...TWO contacts are not more reliable than ONE!”**

Surprisingly, a low profile (.150" high) DIP socket is a different breed of cat when it comes to engineering in contact reliability. Most standard DIP sockets have dual contacts. (R-N's dual "side-wipe" contacts are among the most reliable in the industry.) But, when you shorten the contact length to achieve the "low profile" you lose a great deal of contact force and IC retention strength. So, to achieve effective low profile socket reliability you must redesign the contacts and make them out of the strongest contact material available.



Low .150" profile of ICL socket reduces board density by 26%.

AVERAGE  
3.5 oz.  
minimum  
withdrawal  
force



Fat-Skinny **TESTS PROVE\*** that R-N "back fold side-wipe" SINGLE CONTACT design for low profile sockets provides—  
**4 TIMES BETTER IC RETENTION FORCE** than competitive low profile dual-leaf sockets

\* In "Fat-Skinny test," withdrawal forces are measured using the smallest size (.008") lead after insertion of largest size (.012") lead.

### Representative NORMAL FORCE Test Scores for 10 R-N ICL low profile sockets

TEST SOCKET	NORMAL FORCE *
1	410 grams
2	465 grams
3	480 grams
4	465 grams
5	395 grams
6	425 grams
7	465 grams
8	395 grams
9	410 grams
10	425 grams

AVERAGE — 430 grams

This force is 4 to 5 times greater than average dual contact socket NORMAL FORCE

\* NORMAL FORCE means force perpendicular or at right angles to IC lead. The single ICL contact exerts this kind of force against the IC lead when inserted into the socket.

WRITE TODAY for latest R-N "Short Form" Catalog of R-N production DIP sockets. Contains full specs, dimensions and material data. Get yours now.



# RN ROBINSON NUGENT, INC.

800 East Eighth Street, New Albany, Indiana 47150 • Phone: (812) 945-0211 — TWX: 810-540-4082

Circle 179 on reader service card

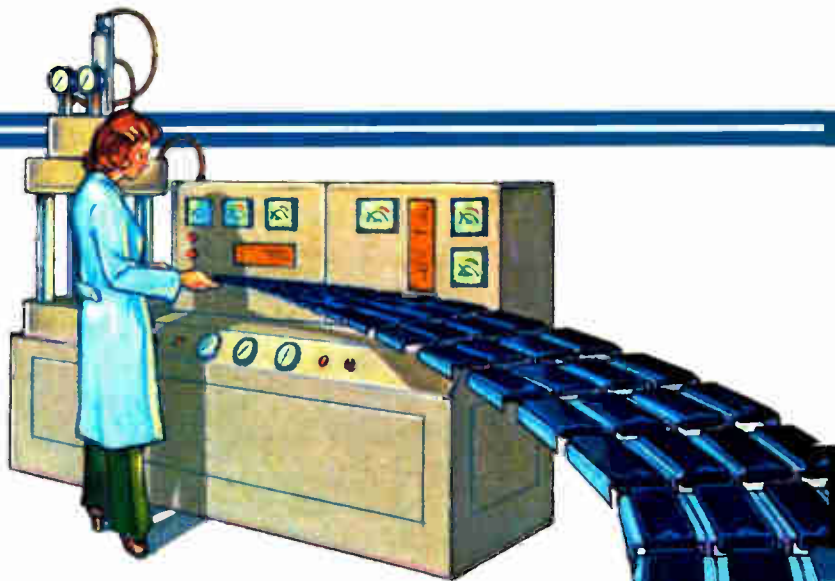
# Productivity. Hysol Epoxies mean more of it. And you can prove it.

You can prove, on your own existing equipment, that you can mold more units per shift than with competing products.

That's increased productivity *without* increased capital investment.

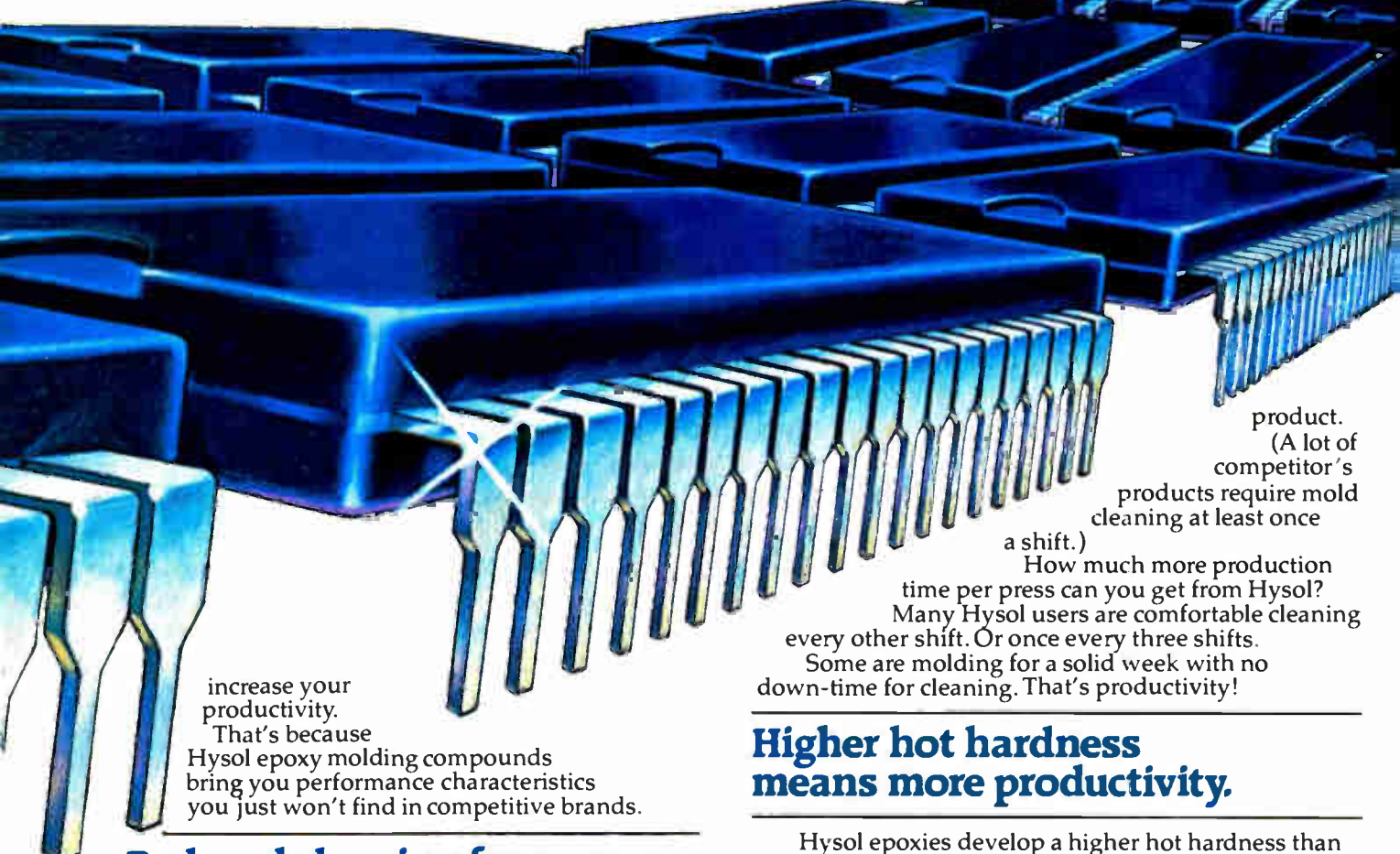
You won't be sacrificing quality or reliability.

You'll be adding to them—significantly. As you



You cut your down-time spent cleaning molds.

You also can make longer molding runs before residues have any effect on the appearance of the



increase your productivity.

That's because Hysol epoxy molding compounds bring you performance characteristics you just won't find in competitive brands.

## Reduced cleaning frequency means more productivity.

Hysol epoxies leave molds cleaner than competitive products.

And Hysol leaves those molds cleaner much longer. More than twice as long!

product.  
(A lot of competitor's products require mold cleaning at least once a shift.)

How much more production time per press can you get from Hysol?

Many Hysol users are comfortable cleaning every other shift. Or once every three shifts.

Some are molding for a solid week with no down-time for cleaning. That's productivity!

## Higher hot hardness means more productivity.

Hysol epoxies develop a higher hot hardness than competitive products.

And they develop it in less time.

The average close-to-close time for molding is about three minutes.

Hysol customers achieve a close-to-close time as low as two minutes.

Your molding press operators can make more 'shots' per shift.

And the more shots per shift, the better your productivity.

## Far less flash means more productivity.

Hysol epoxies are *lowest* in flash by an enormous amount.

In fact, for some products, you don't need a de-flashing step at all.

With Hysol you either completely eliminate the cost of deflashing, or you reduce it significantly.

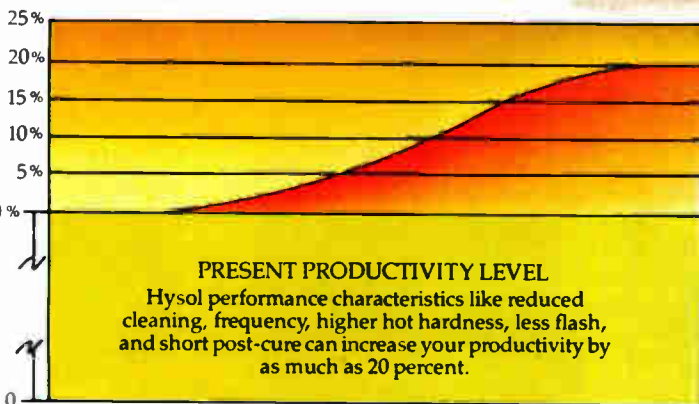
## Short post-cure means more productivity.

The typical post-cure for semiconductor grade epoxies is specified as six hours.

Many Hysol users safely cut that time to two hours.

Post-cure time this short means faster throughput—more productivity—for you. Plus significant energy savings.

Other epoxies take a lot longer to cure. And no matter how long they take, they wind up with a lower



glass transition temperature ( $T_g$ ).

Hysol's higher  $T_g$  means that their epoxy has a lower temperature coefficient of expansion over a wider temperature. This reduces thermal intermittents. And increases reliability.

To these three performance characteristics which contribute to productivity, add Hysol's better thermal stability and moisture resistance—which contribute to higher reliability.

Just more reasons why Hysol is the epoxy to be preferred in the semiconductor industry!

## Prove it first-hand

Why not see how Hysol can mean more productivity on your own production floor, using your own mold, and press?

We'll arrange it for you. And we'll supply, at no cost to you, the epoxy and a qualified field sales engineer to assist in the trial and discuss potential productivity improvements in terms of your existing equipment and procedures.

You keep all the samples so your own engineering and R & QA people can evaluate them.

OR...

Send your own engineer to our testing lab and we'll run our samples side-by-side with yours—or *any others you specify*.

To get things rolling—either at your place or ours—just call Ron Benham, our Product Marketing Manager, Semiconductor Molding Compounds at (213) 968-6511.



THANKS!

I'm not quite ready (yet) for an in-plant demonstration of Hysol Productivity.

But I would like to see your new brochure on molding productivity, quality and reliability with Hysol.

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 TITLE \_\_\_\_\_  
 COMPANY \_\_\_\_\_  
 ADDRESS \_\_\_\_\_  
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Mail to: Hysol Division, The Dexter Corporation, 15051 East Don Julian Road, Industry, California 91749.



# HYSOL EPOXIES

THE DEXTER CORPORATION

Circle 181 on reader service card

# Introducing the 5610 Automated Network Analyzer System...

**Fast, Automatic and  
Accurate from  
10 MHz to 18 GHz.**



# It's a Wiltron.

Now you can automatically make the most important microwave measurements...return loss (SWR), transmission loss or gain and absolute power...quickly and accurately over the 10 MHz to 18 GHz range with hard copy output. Straightforward program-guided inputs are easy to follow.

Wiltron's new 5610 desktop computerized system gives you a new level of accuracy, convenience and cost savings. You simply plug in the preprogrammed cartridge that comes with each system, enter a few simple inputs through the controller, then get hard copy test data over a 66 dB (+16 dBm to -50 dBm) dynamic range from 10 MHz to 18 GHz. No other scalar system is remotely comparable.

## Turnkey system includes programming.

Wiltron's 5610 system is delivered complete and ready to work. The system includes a 560 Scalar Network Analyzer, 610D Sweep Generator, 560-97A50 (GPL-7) SWR Autotester, 560-7A50 Detector, HP 9825A Desktop Computer and HP 7225A Plotter. We also include the preprogrammed measurement software cartridge, as well as all cables and accessories. Option 3 provides a WSMA test port connector. Option 4 is Type N. Special versions are available for operation up to 40 GHz.

## A new era in microwave measurement.

0.01 dB resolution. • SWR measurements with better than 40 dB directivity. • 66 dB dynamic range. • One sweep generator covers the 10 MHz to 18.5 GHz range. • A new WSMA (SMA compatible) connector with improved return loss measurement accuracy and life expectancy. • Digital memory techniques which substantially improve measurement accuracy. • Calibration techniques which correct for variations caused by frequency response variations and test port mismatch errors. • Refreshed display of memory-corrected measurement results.

## Wide Application.

The 5610 is well suited to both laboratory and production line applications. Almost every kind of RF component or system can be tested. For instance:

Test amplifiers to measure gain, power, isolation and return loss over 66 dB dynamic range.

Test filters to plot insertion loss and return loss individually or together on a single page with 0.01 dB resolution.

Test antennas to make precise return loss measurements with 40 dB directivity accuracy and memory-corrected test data.

## In the lab, on the line, payback is fast.

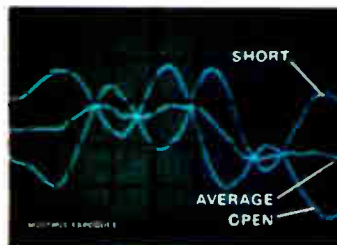
Even if you're only testing a single device, substantial savings are yours with the new Wiltron 5610 system. And, on the production line, you'll get your initial investment back even faster.

For an early demo or full data, phone Walt Baxter, (415) 969-6500, or address Wiltron, 825 East Middlefield Road, Mountain View, CA 94043.

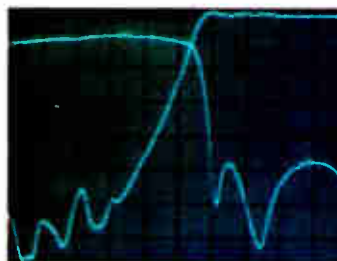
## Easy 4-step operation

```
DATE?:          AUGUST 1, 1979
DEVICE UNDER TEST?: HIGH PASS FILTER
DUT SERIAL NUMBER?: 4782
START FREQUENCY IN GHz?: .01
END FREQUENCY IN GHz?: 10
FREQUENCY STEP SIZE IN MHz?: 100 MHz
WHAT TYPE OF MEASUREMENT - TRANSMISSION (T),
REFLECTION (R), OR BOTH SIMULTANEOUSLY (S)? S
```

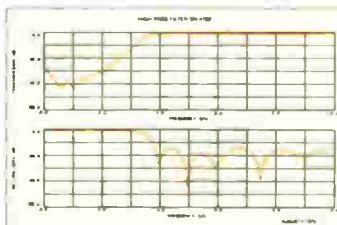
Enter test parameters on controller



Store system residuals in memory for later correction of test data




Use CRT display to confirm proper operation of system and to adjust device under test



Initiate automatic measurements and hard copy printout

**WILTRON**

Circle 183 on reader service card

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for component solutions . . .

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The secret to widening your choice of pushbutton switches is the unusual flexibility of Centralab's modular pushbutton switch systems. You'll find lighted and non-lighted switches for pc board or front panel mounting; single station or ganged assemblies with 10 to 25mm spacings; 2-4-6 or 8 pole designs for push-push, push-pull, momentary or interlocking operation with lockout options; silver or gold contacts; epoxy sealed terminals; and a variety of switch housing materials. An outstanding choice of other options include buttons, colors, lenses, filters and legends.

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## New products

Packaging & production

# Connector has ground bus

Selectively grounded unit for  
planar twisted pairs doubles  
number of I/O connections

As digital logic continues to speed up, packaging engineers increasingly use planar twisted-pair cables to serve as the cabling interface between various building blocks of large mainframes. This technique calls for a ground-signal-ground type of wiring that requires a ground wire for every signal wire. Because of this, most twisted-pair cables in digital applications have been terminated until now with two cable headers at each end (one for each of the resulting two layers of cable).

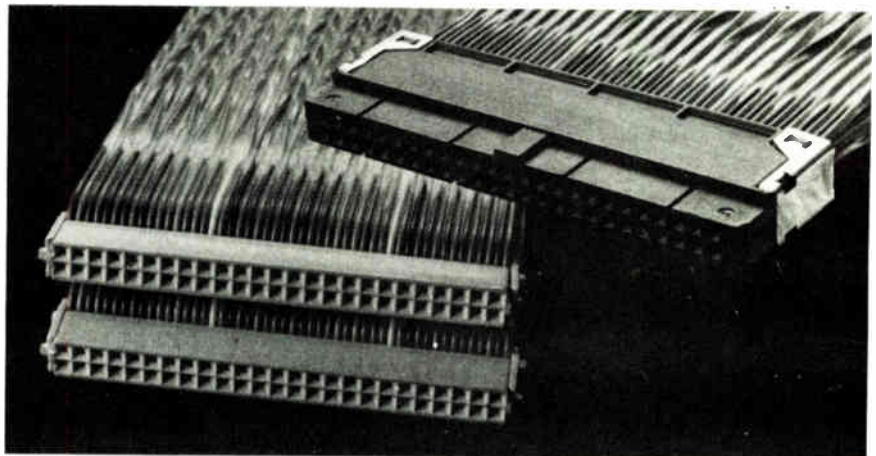
A new selectively grounded (SG) connector system jointly developed by Augat Inc., Attleboro, Mass., and Pintek Inc., Newton Upper Falls, Mass., uses only a single selectively grounded connector with insulation-piercing contacts to accommodate the two layers of cable resulting from the planar twisted pairs. This interconnection efficiency is gained by connecting the ground wires in common to a special internal bus, allowing the majority of the connector's contacts to be devoted to signal wires and only one of them to an external ground.

The new system doubles the number of I/O signal connections with the same printed-circuit-board real estate as a conventional connector pair. Its clever design allows any combinations of signal-ground assignments. (The ground bus may be segmented to allow for multiple separate grounds.) Use of the SG connector can eliminate the requirement for paddle boards, lower the cost of circuit boards, and reduce space requirements of both cable runs and mating headers.

To prevent incorrect plugging of the connector, a total of 16 positions can be attained without loss of contact position by means of keying clips mounted on the SG connector and on the header. In addition, an aluminized Mylar shield protected by a 60-mil-thick polyvinyl chloride jacket allows the cable assembly to be used over extended distances.

This concept is a patented development of David Hatch, president of Pintek. Hatch formerly was a sales representative for Spectra Strip Inc. and first noticed the need for a new termination method for flat twisted-pair cables in the course of his sales activities with large computer firms. At present, Augat has a 30% interest in Hatch's company and has taken a license on the patent in order to produce the product.

The SG system consists of four major components: a cable connector, a mating header, a keying system, and a cable shield and jacket. The new connectors, which accept two layers of standard twisted-pair flat cables with conduc-



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\*\*Data General is a computer manufacturer unrelated to MDB.

Circle 121 for DG; 122 for PDP; 123 for LSI; 124 for IBM; 125 for Interdata

## New products

tors on 50-mil centers, are currently available in 40- and 50-pin configurations with the pins located on a 100-by-100-mil grid.

The SG connector itself comprises two body halves, a divider, signal contacts, bus bars, and retaining clips. The two body halves are identical except for a polarizing key. Each half contains a row of signal contacts and a row of bus contacts.

The signal contacts feature dual cantilever-beam contact arms with domed contact points. An industry-standard insulation-displacement-connector (IDC) configuration provides a wedging action during the initial thrust into the cable, which aligns the cable with the contacts before piercing.

The bus bar consists of two rows of IDC contacts on one strip. One row interconnects every ground wire; the other row intercepts all the signal wires. The ground output contact is determined by trimming away all but one selected intercepting contact. Separate grounds can be achieved by dividing the bus into two or more sections.

Both headers and connectors are molded from Underwriters Laboratory-listed 94 V0 thermoplastic polyester and are available as assemblies from either Augat or Pintek in standard cable lengths, such as 12, 24, 37, 72, and 120 inches, as well as in nonstandard sizes.

Augat Inc., 33 Perry Ave., P. O. Box 779, Attleboro, Mass. 02703 [391]

Pintek Inc., P. O. Box 98, 90 Oak St., Newton Upper Falls, Mass. 02164 [392]

## Flat-cable shield provides continuous protection

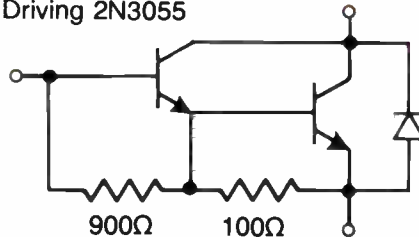
Ensuring 360° shielding of flat multiconductor cables, a shield assembly consisting of a laminated composite of conductive metal foil and insulating plastic film may be used as a floating system or grounded to a common system.

The major advantage of the shield is its continuous envelope of metal, according to the manufacturer. Conventional shields have seams at the

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Replacing 2N3054  
Driving 2N3055



## COMPARE THESE SPECIFICATIONS!

Parameters	SDM 5002	PMD 10K-60	Solitron's Superior Performance
$h_{FE} @ I_C = 6.0A$	1500 Min.	1000 min	50% Higher Min. Gain
$h_{FE} @ I_C = 15.0A$	750 Min.	None	No Comparison At All
$V_{CE(sat)} @ I_C = 6.0A$	1.0V Max.	2.0V Max.	50% less Sat. Voltage
$I_{S/b}$	2.5A @ 60V	5.0A @ 30V	100% Higher Voltage at SOA

With just one of our new Single Diffused NPN Power Darlington Transistors, you can replace up to five components\* in linear power circuit applications. Plus, these devices have superior performance over other existing Darlington transistors, including an expanded SOA range at higher voltages.

Solitron's Single Diffused Power Darlington transistors have proven their extreme ruggedness by undergoing thousands of hours of rigid testing by a major automobile manufacturer. Some typical applications include motor controllers, audio amplifiers, series pass regulators and power supplies. Contact us today for data sheets on the 150 Watts SDM5001-5017 and 117 Watts SDM4001-4017 Series! They're competitively priced, waiting for you right now!

Dial toll-free 800-327-8462 for complete information.

\*Output diode, driver transistor, input resistor, output resistor, and output transistor.

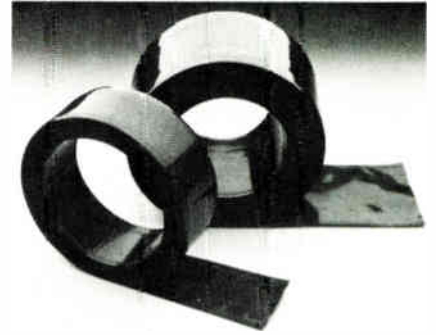
**Solitron** DEVICES, INC.

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## New products



edges, whereas the new cable shield has overlapped metal at both edges to provide metal-to-metal contact along its entire length. Other advantages include: a wide selection of conductors and insulating films, ease of making ground connections, and good tear strength. The shield is offered in standard sizes for 25- and 50-conductor cable, in continuous rolls or precut lengths.

The standard shield consists of aluminum as the conductive element, with Mylar film as the internal low-friction insulation, and Tedlar as the external dielectric layer for electrical insulation and scuff resistance. Other materials available include a copper conductive component and polyvinyl chloride or Teflon insulating layers.

The company expects the assembly to sell for less than \$1 per foot in reasonable quantities. Delivery is within a week to 10 days.

TME Corp., 16 Flagstone Dr., Hudson, N. H. 03051. Phone Bob Deeley at (603) 880-4807 [393]

Power transistor socket  
fits directly onto pc boards

A transistor socket designed for direct mounting to printed-circuit boards has recently been introduced for high-power applications. Fully insulated, the power-transistor socket is to be used with diamond-style TO-3 cases. Its polyester body reinforced 30% by glass is recognized by Underwriters Laboratories as 94V-0. The socket also has phosphor-bronze contacts and gold plating over silver.

The mounting plate is tapped for

## PUT YOUR PENNIES IN A NICKEL BASE BY MASDEN

A nickel-plated base from Masden Industries costs pennies but your chips, hybrid circuits, microprocessors are assured of sound, dependable housing. That's because the whole package is manufactured under the same technological and management roof. From design to destination, Masden people supervise the production of each header. Pins, glass insulators, nickel-plated platforms are all made and then assembled at Masden-owned companies. Each is ruled by the same high standards of excellence — quality control, performance, dependability, delivery. Bank on Masden for a firm foundation.



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Circle 188 on reader service card

## Fantastic! 1mcd at 1.6mA

Xciton's XC-5569-R red GaP LEDs, in a standard T-1 $\frac{3}{4}$  package, provide a typical 1 mcd of light output at 1.6 mA of drive current. This superior brightness at very low current drive levels creates a new design flexibility in power sensitive applications.

### Advantages

#### For Your Customer's Power Sensitive Designs:

- Power conservation in isolated power supplies such as medical electronics, and in PC board status indicators
- Longer battery life due to reduced power drain

#### For The Design Engineer:

- Capable of one gate load drive from TTL
- Directly driven from CMOS and MOS circuits
- Used to advantage in smoke detectors, intrusion alarms, and portable instruments
- 697nm wavelength makes XC-5569-R a highly efficient driver for CdS and Si Photodetectors

#### For The Purchasing Agent:

- Integrated quality assurance and engineering support program
- Timely delivery of product
- Prompt quotations, competitive pricing, and unmatched product service with a 1 year warranty
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188 Circle 58 on reader service card



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“Take the Intel® 8086, their 16-bit micro-computer, for example. It’s enabled us to technologically leapfrog the competition. The raster graphics state-of-the-art is limited by monitor technology to a million elements. Coincidentally—or not—the 8086 with its million byte addressability means each dot on the

screen can be addressed individually—and very rapidly. That’s opened up all sorts of feature and capability possibilities.

“With Intel’s Intellec® development system and ICE-86™ in-circuit emulation, we’ve been able to take advantage of the 8086 by quickly developing sophisticated proprietary software.

“And the Intellec system helps us be responsive to the needs of our large OEM customers by customizing software. In a matter of days, we can develop unique capabilities for a customer, store the program in PROM and deliver it to the field.

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## Momentary pushbutton switches are a snap



C&K's got them. All kinds of snap-acting momentary pushbutton miniature switches. All you need. In SPDT, DPDT, 3PDT, and 4PDT Models with a variety of actuator and termination options.

Models 8121 through 8421 have a 1 amp rating. UL listing available. Models 8125 through 8425 are rated at 0.4 Volt-Amps for dry circuit applications.

The Primary Source Worldwide  
C & K Components, Inc.  
15 Riverdale Avenue, Newton, MA 02158  
Tel: (617) 964-6400, TELEX: 92-2546, TWX: 710-335-1163



Circle 61 on reader service card

## The right angle is the right idea.



C&K's right angle miniature toggle switch mounts directly on P.C. boards with a low profile that makes a good design look even better. An integral switch support bracket reduces stress on the terminals. Right on.

C&K makes it with a wide range of actuator, and bushing options in 1, 2, 3 and 4-pole versions, with contact ratings of 0.4 VA max. UL listing available.

The Primary Source Worldwide  
C & K Components, Inc.  
15 Riverdale Avenue, Newton, MA 02158  
Tel: (617) 964-6400, TELEX: 92-2546, TWX: 710-335-1163



### New products



6-32 screws. Integrally mounted bosses on the mounting holes eliminate the need for separate washers.

In production quantities, the company says that the sockets will sell for 20¢ each, with delivery from stock.

Projects Unlimited Inc., 3680 Wyse Rd., Dayton, Ohio 45414. Phone Greg Kimpton at (513) 890-1918 [394]

### Hand-held test duo checks on RS-232 interfaces for \$85

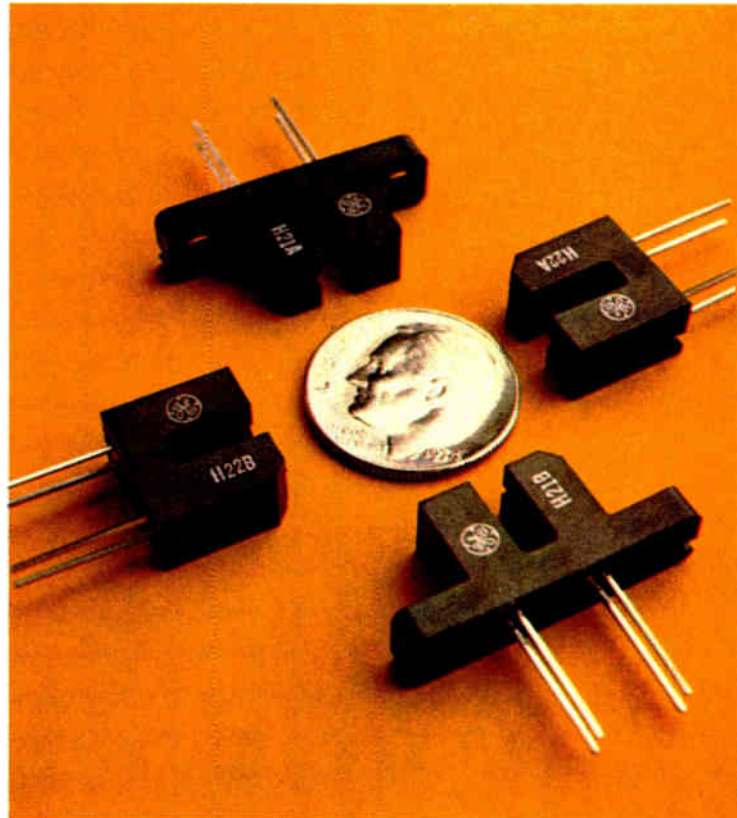
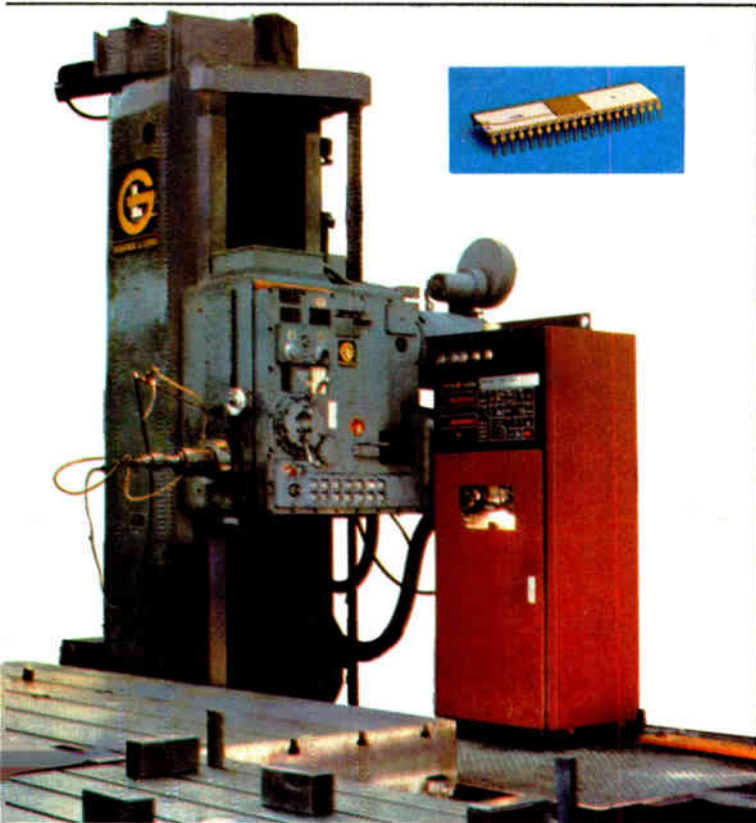
A hand-held data-communications device and a pencil-sized logic probe are teaming up to provide a low-cost test set for checking all 25 RS-232 leads. BOB (for break-out box) and PAP (for pencil activity probe) are both battery-free.

BOB offers permanent and temporary reconfiguration of an RS-232 interface, making all of the interface's 25 leads available for solder or patch connections and for monitoring. Two connectors—one male and one female—are connected to the pc board by means of 50 solder positions and 56 patch positions. Two side-mounted grommets holes are also provided for any extra cable



# What brings $\mu$ processor precision performance to your workhorse?

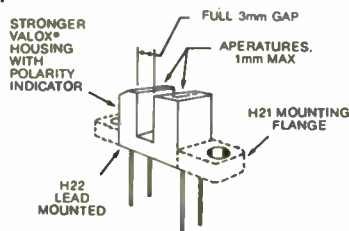
# GE's new supersensitive interrupter module.



Equipment from computer peripherals to machine tools can now take advantage of precision  $\mu$  processor performance with General Electric's H21 series interrupter modules. Compatible with popular logic systems from CMOS to relays, these new high current, high voltage modules have been optimized to improve resolution and accuracy, and provide up to 25MA minimum specified output and 55V blocking capability.

The H21 and H22 modules provide a consistent light beam with maximum dimensions of 1 mm x 1.5 mm.

There are 24 types of interrupter modules available, 12 transistor detectors and 12 darlington detectors. Transistors feature low saturation



voltage ( $\leq 0.4V$  at 1.8 MA) and darlington's high output current, ( $\geq 50$  MA at 1.5V). All with the high performance you need in measurement systems and mechanical/electronic interfaces.

Supersensitivity. Improved resolution and accuracy. All part of General Electric's new optimized interrupter modules. For a design specification sheet and free sample, write to General Electric Company, West Genesee Street, Auburn, NY 13021. Or call Bob Brewster (315) 253-7321 X420, or contact your authorized distributor.

222-12

**Attend GE State-of-the-Art Application seminars on optoelectronics, transient voltage protection and power transistors to be held in eight Eastern cities during November. Write or call (315) 253-7321 Ext. 225.**

®Registered Trademark of General Electric Company

**GENERAL ELECTRIC**

Circle 191 on reader service card

## New products

connections needed.

PAP is designed for checking any RS-232 lead for low state, high state, toggling, ground, and broken connections. PAP has voltage protection to  $\pm 75$  v dc.

BOB sells for \$56, and PAP for \$29. Delivery is from stock.

Expandor Inc., 400 Sainte Claire Plaza,

Upper St. Clair, Pa., 15241. Phone Gene Yost at (412) 746-2910 [395]

Minigrabber has in-line banana jack for under \$2.50

ITT Pomona Electronics has just

introduced a minigrabber with an in-line banana jack. The minigrabber on the model 4649 features a gold-plated beryllium-copper contact with 20-gauge wire and a body made of polyvinyl chloride.

The jack accepts all standard banana plugs. The brass used is nickel-plated with glass-filled nylon insulation.

Available with wire lengths from 12 to 60 in., the minigrabber with banana jack sells for \$2.25 to \$2.45, with delivery in two weeks.

ITT Pomona Electronics, 1500 E. Ninth St., Pomona, Calif. 91766. Phone Carl Musarra at (714) 623-3463 [396]

# GOODBYE ALIAS, HELLO GAIN

The new Precision 416 combines filter and amplifier in 16 programmable channels. You save 35% by buying one instrument instead of two for conditioning analog data for digital conversion. Time delay filters superior to Bessel. Elliptics with 80 dB/octave attenuation. DC differential input stage with

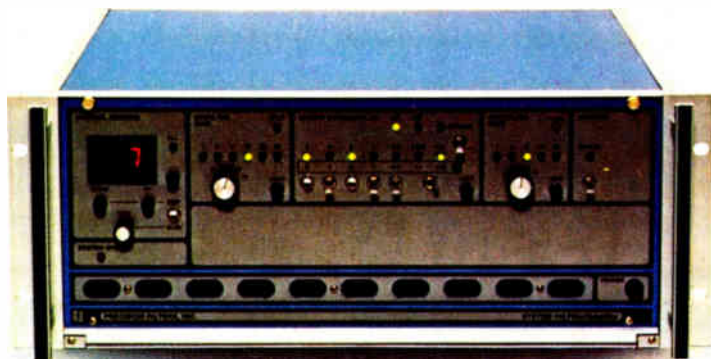


100 db CMRR. Both pre-filter and post-filter gain are programmable for optimum signal quality. Both include overload indicators. Interfaces with mini, micro or GPIB. Phase match is less than  $2^\circ$ . Call Don Chandler, 607-277-3550, or write for demonstration and complete specs.



**PRECISION FILTERS, INC.**

303 W. Lincoln, Ithaca, N.Y. 14850



Unit inserts jumper wires of various lengths

A system for inserting jumpers into printed-circuit boards includes a continuous coil of round or square jumper wire and an applicator machine. A major feature of the Autojumper system is that jumper spacing is adjustable to 1.125 in. The system also eliminates the need to stock various lengths of jumpers because it uses a continuous coil.

The user positions the pc boards on a table and starts up the machine. The machine feeds in a length of jumper material and then cuts, forms, and inserts it into the board — in a single operation. It can insert 1,500 to 2,000 jumpers per hour at a cost ranging from \$2.00 to \$3.00 per thousand jumpers.

The machine may be adjusted to various thicknesses of pc boards. The standard jumper material is 0.025 in. in diameter, with brass-tin plating, but other alloys and platings are offered. A typical supply reel holds enough material to make about 30,000 jumpers.

Three types of applicator machines are available: single-insertion, pantograph, and CNC (computer numerically controlled). Prices range from \$1,575 for a single-insertion system to \$17,000 for a computer-controlled unit.

Autosplice Inc., 220 East 23rd St., New York, N. Y. 10010. Phone (212) 674-4369 [397]



# YOU DON'T HAVE TO SEE THE LIGHT TO KNOW THE WAY.

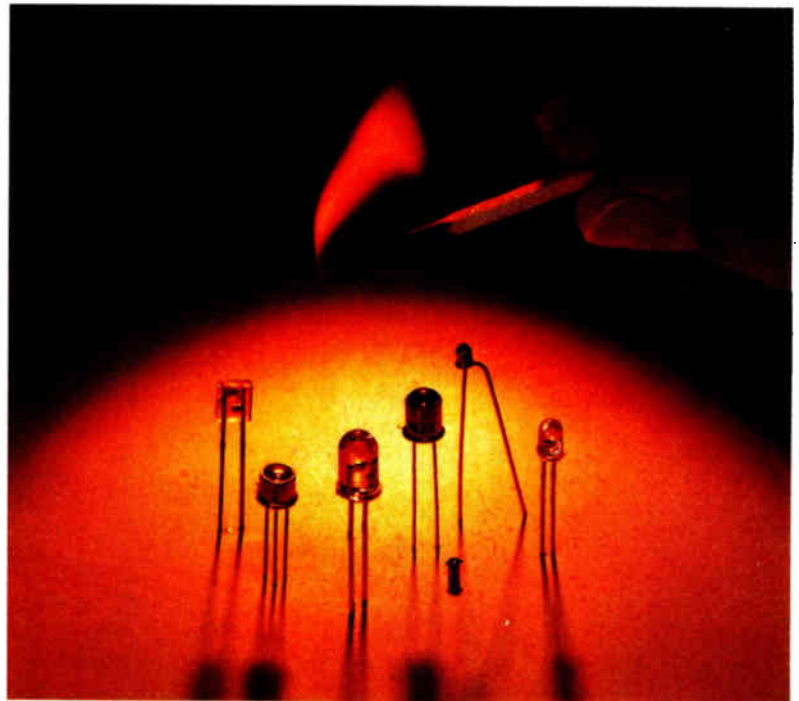
Maybe you can't see the light from our infra-red LED components, but we'll show the way to successful opto design.

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Already, they've been highly successful in applications like automobile cruise controls, business machine paper detectors, vending machine and telephone coin detectors, smoke detectors, industrial controls, even fiber optics.

Or if you'd rather buy pre-assembled products, we offer industry standards in slotted interrupter



modules, optically coupled isolators and fiber optic modules. You can even get assemblies custom designed for your application.

So if you've got an idea for an optoelectronic design, let us know. We'll show you how to make it shine.

Give us a call at 214/234-4271. Or write us at 830 East Arapaho Road, Richardson, Texas 75081.

***Spectronics***  
A Division of Honeywell

# VAX Performance. Ask any user.

**"VAX simply ran over the competition. In cost/productivity ratios, nothing even came close."**

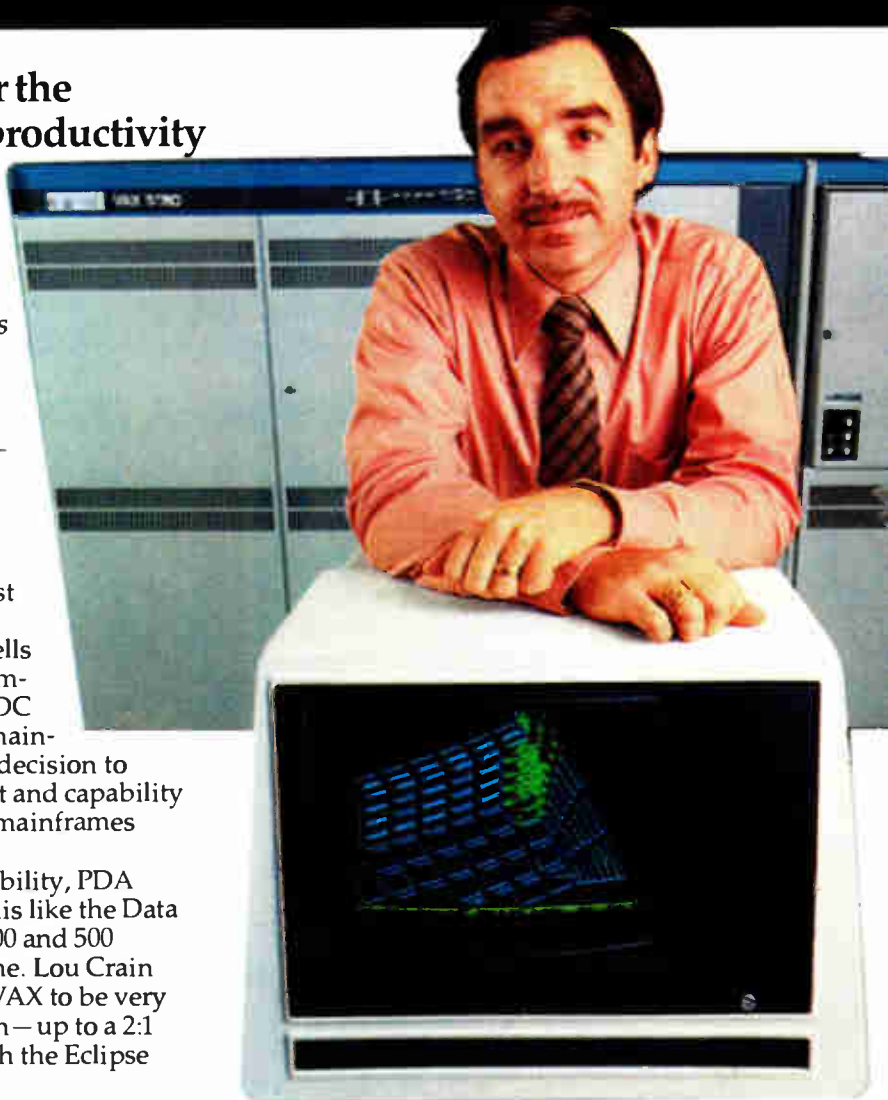
*Lou Crain, Mgr. of Software Products  
Prototype Development Associates  
Santa Ana, California*

PDA is an employee-owned engineering concern whose business ranges from fundamental research in structural analysis to the manufacture of critical aerospace components.

The VAX-11/780 is PDA's first in-house computer. Lou Crain, Manager of Software Products, tells us, "We've been doing all our computing through utilities using CDC 6600, Cyber 74 and Univac 1108 mainframes. The key elements in our decision to acquire the VAX-11/780 were cost and capability — compared to service bureaus, mainframes and competitive minis."

From the standpoint of capability, PDA considered traditional superminis like the Data General Eclipse and the Prime 400 and 500 series, plus a used 1108 mainframe. Lou Crain says, "Our benchmark showed VAX to be very powerful against the competition — up to a 2:1 performance advantage over both the Eclipse and the 1108."

"After installation," Crain concludes, "VAX has lived up to our expectations and has performed impressively. It's resulted in better



products for our customers, as well as improved cost-effectiveness. Having our own interactive capability in-house has meant an increase in engineering productivity of up to 300%."

**"VAX turns out to be twice the machine for the same amount of money."**

*Roger Vossler,  
Section Manager and Systems Engineer  
TRW Defense and Space Systems Group  
Redondo Beach, California*

Sensor data processing and distributed processing systems in support of real-time embedded applications are among the specialties of TRW's Defense and Space Systems Group.

To find the right computer, TRW continues to evaluate numerous machines — including Digital's VAX-11/780. They've also conducted numerous FORTRAN and PASCAL benchmarks.

In every test, VAX stands out as a clear winner.

Roger Vossler, Section Manager and Systems Engineer, says, "VAX is one of the best implementations we've seen of a successful integrated hardware and software system."

Since TRW's sensor data processing applications require enormous memories — over a million bytes to store a single image, for example — VAX's true 32-bit address space is vitally important. In addition, says Vossler, "VAX's I/O bandwidth capabilities are extremely important for effectively moving large quantities of real-time data at very high data rates."

Because TRW already had an investment in Digital technology, Vossler is particularly impressed with the relative ease of moving PDP-11 series programs onto VAX.

"But," says Vossler, "Even if I were starting all over again — without our Digital experience — I would still pick VAX, on the basis of its architecture, both hardware and software, and its impressive performance."

## "Implementation was faster on VAX than on 25 other machines."

*Brian Ford, Director  
Numerical Algorithms Group  
Oxford, England/  
Downers Grove, Illinois*

The Numerical Algorithms Group develops and maintains mathematical and statistical software libraries for customers in industry, science and academia.



Before VAX, NAG had implemented their complex Mark 6 Library on 25 major machines, including the Burroughs 6700, CDC 7600, Univac 1100, and the IBM 370. The average implementation time was 13 man-weeks.

VAX took five.

In Dr. Ford's words, "A successful implementation requires the correct functioning of the 345 library routines to a prescribed accuracy and efficiency in execution of NAG's suite of 620 test programs. Whilst the activity is a significant examination of a machine's conformity to the ANSI standard of the FORTRAN compiler, its main technical features are file creation, file comparison, file manipulation and file maintenance."

And implementation performance was just the start. Dr. Ford comments on VAX's impressive record of reliability after the program was up and running: "No problems were encountered in the VAX/VMS software even though approximately 3000 files were being handled. The operational availability time for the machine was close to 100%, an outstanding statistic for new hardware and a new operating system.

"VAX," Dr. Ford concludes, "is an implementor's dream."

Digital's VAX-11/780 has re-defined the level of performance you can expect from computers in its price range.

If your application requires large number crunching capability, high floating point accuracy, or lots of high-speed real-time calculations, there is simply no better system.

But don't take our word for it. Send for our new brochure. And listen to our customers.

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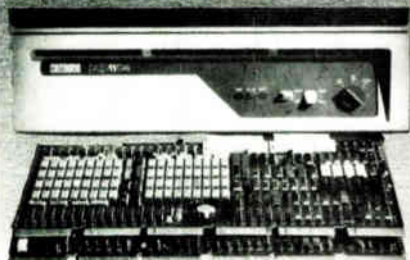
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- micro processor control
- 1 Hex board-plugs into PDP 11

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### The low cost array processor

- extensive array library
- 1024 Real FFT in 7ms
- on-board 4k memory
- 2 Hex boards-plugs into PDP 11

## Display — MDP-3

### The programmable image processor

- 64k x 18 Bits Refresh Memory
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- Full color capability
- 2 Hex boards-plugs into PDP 11



**Computer Design &  
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(617) 964-4320

## New products

Semiconductors

## Unit multiplies in 70 ns at most

8-by-8-bit device has  
typical multiplication  
time of only 45 ns

To use an 8-by-8-bit multiplier chip, a design engineer has to choose between one from Monolithic Memories Inc. and another from TRW, and it's really a choice, because the two parts are neither performance- nor pin-compatible. But Advanced Micro Devices Inc., plans to change that with a new 8-by-8-bit multiplier that is pin-compatible with MMI's part but twice as fast.

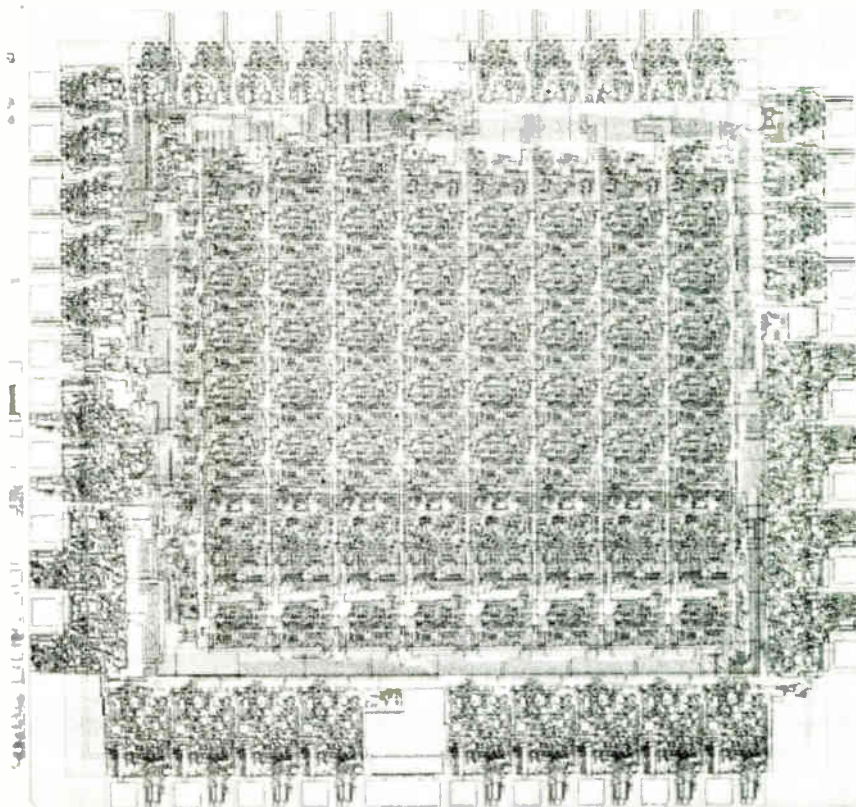
AMD's new Am25S558 will typically perform a full 8-by-8-bit multiply in 45 ns with a target worst-case specification of 70 ns, says Lyle Pittroff, marketing manager for new products, bipolar logic, and interface

operations. Moreover, like MMI's 67558, AMD's Am25S558 can be cascaded, so that in a 16-by-16-bit configuration (32-bit output), the typical multiplication time is 110 ns.

Thus, Pittroff says, AMD eyes applications in high-speed signal processing, such as radar, sonar, and fast Fourier transform systems; in real-time instrumentation; in array processing; and in communications, such as digital filters and modems. The device is compatible with 8080 8-bit and Z8000 16-bit systems and fits in well with AMD's own 2900 series bit-slice logic family, he says.

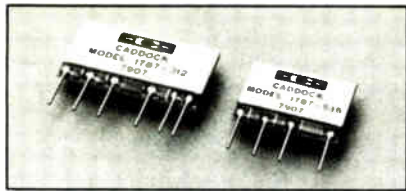
Actually, it looks as though the 558 pinout may be on its way to becoming the industry standard for 8-by-8-bit multipliers. Besides AMD, Raytheon is second-sourcing MMI's parts and expects to have parts later this year, and Fairchild Camera and Instrument Corp., has leaked the fact that it is planning a similar part that will employ its Fairchild Advanced Schottky Technology (FAST) approach.

Right now, however, AMD is the new kid on the block who is already



**Current sensing resistors for multi-range instruments.**

**NEW**



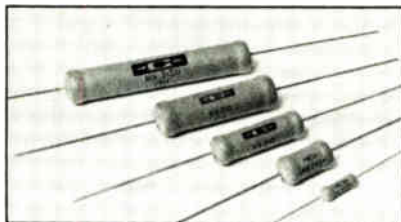
**Caddock's Type 1787 Current Shunt Resistor Networks.**

Absolute resistance tolerances of 0.25%, 0.1%, 0.05% and 0.02% make these 2-, 3- and 4-decade current shunt resistor networks the ideal replacement for expensive, bulky discrete resistors.

16 standard models are now available. The basic network design provides a series total resistance of 1000 $\Omega$ , 100 $\Omega$ , 10 $\Omega$  and 1 $\Omega$ . Other standard models provide commonly used variations of this basic design.

For Type 1787 data, circle Number 201.

**Non-inductive precision resistors for power switching circuits.**



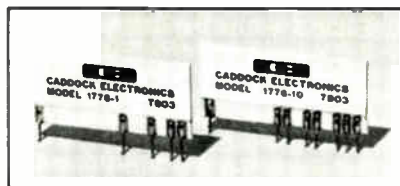
**Caddock's Type MS Power Film Resistors.**

Caddock's patented Non-Inductive Design in power ratings from 2 watts to 15 watts assures minimum voltage transients in all types of power switching circuits.

High stability Micronox\* resistance films operate to +275°C and years-long load-life tests demonstrate extended-life stability better than 0.05% per 1000 hours.

For Type MS data, circle Number 203.

**Off-the-shelf precision decade voltage dividers.**



**Caddock's Type 1776 Precision Decade Resistor Voltage Dividers.**

When used as a 10 Megohm input voltage divider, the Type 1776 family can provide high accuracy voltage division in ratios of 10:1, 100:1 and 10,000:1.

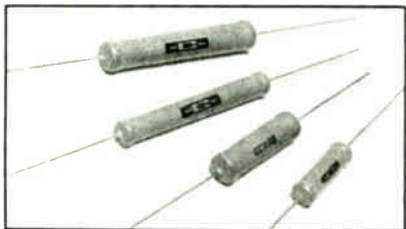
Type 1776 Precision Decade Resistor Voltage Dividers are now available in 25 standard models with ratio TCs from 50 ppm/°C to 5 ppm/°C. Caddock's laser production techniques keep OEM quantity prices low, too.

For Type 1776 data, circle Number 205.

**CADDOCK Resistor Technology solving problems across the board!**

**NEW**

**High stability resistors for very-high voltage control and measurement circuits.**



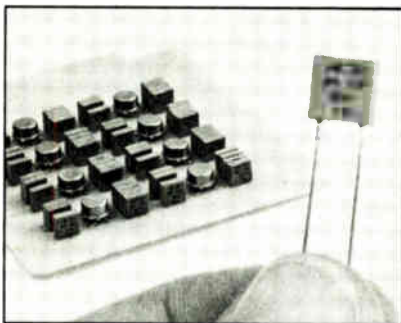
**Caddock's Type MG High Voltage Resistors.**

High voltage probes and control circuits make wide use of Type MG resistors for precision high voltage regulation and high voltage measurements.

Long-term stability — plus proven reliability — have also made these precision resistors first choice in communications satellite voltage control circuits.

For Type MG data, circle Number 202.

**100 Megohms in a miniature package.**



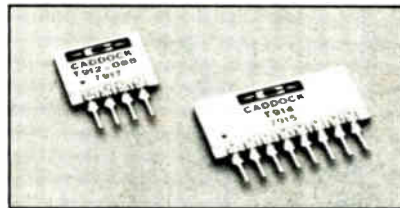
**Caddock's Type MK Precision Film Resistors.**

Precision values to 100 Megohms in a miniature CK 06 case make the Type MK ideal for low current designs.

These non-inductive resistors find wide application in high-impedance analog circuitry.

For Type MK data, circle Number 204.

**Resistor pairs and quads with very low ratio TC.**



**Caddock's Type T912 and T914 Precision Resistor Networks.**

Ratio tolerances to +0.01%, ratio TCs of 2, 5 or 10 ppm/°C and ratio stability within  $\pm 0.01\%$  at full load for 2000 hours provide exceptional stability in precision analog circuits.

Both pairs and quads have isolated resistors of equal value. Standard resistance values are 5 k $\Omega$  to 1 Megohm and custom variations with unequal values are available.

For Type T912 and T914 data, circle Number 206.

Caddock's latest General Catalog provides complete performance data and specifications on over 100 models of these outstanding 'problem-solving' resistors.

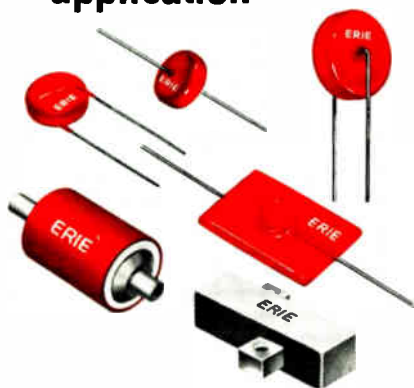
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## New products

peddling his wares. The high speed should help sales. Pittroff attributes it to a new high-performance, low-power Schottky process, "the same process we use to run most of the 2900 products now." He says that the ECL-like circuit design benefits internally from tighter design rules and smaller geometries, which reduce capacitance and increase speed.

The combinational circuit (no clock required) also comes in a 57 version, which has a transparent 16-bit latch between the multiplier array and the three-state output buffers. Both parts feature three-state outputs. Other features include unsigned 2's complement or mixed operands and the implementation of common rounding algorithms with additional logic. The circuit comes in a 40-pin Cerdip and dissipates about 1.1 W over the full military temperature range.

Price will be \$70 in 100 lots. Samples available now.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94086 [411]

drive a vacuum-fluorescent display directly, eliminating the need for an IC display driver. This control chip also has its own memory for 10 pre-selected stations, with last-station recall on both a-m and fm. It can be directly interfaced with General Instrument's electrically alterable read-only memory for nonvolatile memory applications.

The chip has all necessary logic for performing control functions as well as the phase-locked-loop circuitry; only a prescaler is required to make a complete tuner controller.

Features that can be programmed onto the chip include: stereo-only scan, scan up and down, scan favorite station, scan local stations only, and direct frequency entry.

In 1,000-piece quantities, the device sells for \$9.60. Production quantities are available now.

General Instrument Corp., 600 West John St., Hicksville, N. Y. 11802. Phone M. Burden at (516) 733-3120 [414]

## IC eases station selection on a-m/fm stereo radios

An electronically tuned universal tuner controller is now available in integrated-circuit form for use in home and automotive a-m/fm stereo radios. The dedicated AY-3-8118 control chip incorporates phase-locked-loop tuning techniques, thereby achieving high accuracy and eliminating the need for some system components. It is also mask-programmable, which allows the radio designer the convenience of



changing features without spending much time on redesigning the control IC.

The AY-3-8118 is designed to

## Monolithic device senses pressure for under \$10

Similar to other piezoresistive integrated-circuit transducers, the LX0503A absolute-pressure sensing device produces an output voltage proportional to the applied pressure. It sells for less than \$20 in 100-piece quantities—and less than \$10 in large quantities. The monolithic device, packaged in a TO-5 can, does not contain signal conditioning, scaling, or buffering circuitry.

A single inlet tube axially aligned with the package allows the working medium to make contact with the circuit side of the IC's diaphragm, which is covered by a thin, pliable layer of parylene. Although the parylene layer protects the circuit in humid environments, the device is really only suited for immersion in nonionic fluids.

The X0503A is temperature-compensated with respect to voltage sensitivity and features a low offset temperature coefficient—typically 0.015 psi/°C. Rated for use over the temperature range from 40° to

# System 5500 converts any fiber optic link into a high precision analog data link.

Many measurement and control systems deal with slowly changing parameters...a difficult function for conventional fiber optic systems, since their accuracy...while adequate at higher frequencies...usually falls way off at about 30Hz.

System 5500 is a simple two-module set which utilizes proprietary voltage-frequency-voltage conversion tech-

niques to provide 0.1% accuracy...even at pure DC... and 500KHz bandwidth.

Send for APPLICATION TECHNIQUES bulletin AT-802. It provides information and guidance on utilizing fiber optic links in analog systems, and contains complete

System 5500 design specifications.



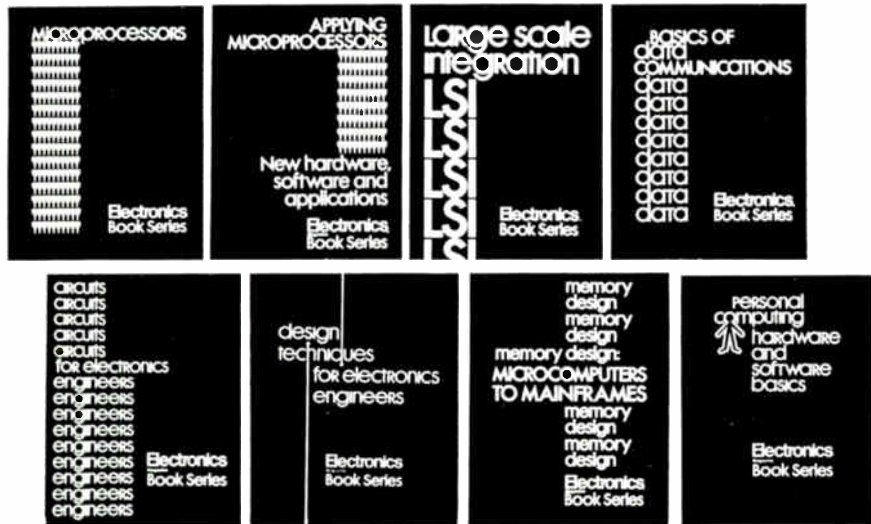
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## New products

105°C, the device has a sensitivity of 2 to 8 mv/psi over the 0-to-30-psi pressure range.

The pressure sensor is suited for use in barometers, hot-bulb thermometers, medical diagnostic equipment, engineering diagnostics, microphones, and low-pressure and vacuum devices. Delivery is from stock to four weeks.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif, 95051. Phone (408) 737-5000 [413]

## Beam-lead p-i-n diodes have low losses

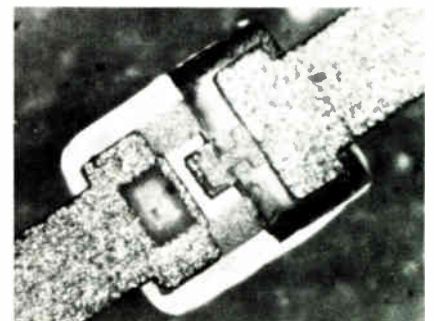
Two ruggedly constructed beam-lead p-i-n diodes have been designed specifically to exhibit low capacitance and low series resistance. The HPND-4001 and HPND-4050 utilize a mesa process, which allows fabrication of diodes with a very low resistance-capacitance product.

The 4001 has a typical series resistance of 1.8 Ω and a typical capacitance of 0.07 pF. The associated typical breakdown voltage is 80 v, and typical reverse recovery time is 3 ns. The 4050's comparable specifications are: a series resistance of 1.3 Ω, a capacitance of 0.12 pF, a breakdown voltage of 40 v, and a reverse recovery time of 2 ns.

For use in stripline or microstrip circuits, the diodes have applications in switching, attenuating, phase shifting, and modulating at microwave frequencies.

In quantities of 10 to 99, the 4001 is priced at \$14.40, and the 4050 at \$11.25, with delivery from stock.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [417]





# PROMs

## ECL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
32 x 8	MCM10139A	25	ECL output	16
256 x 4	MCM10149A	30	ECL output	16

## TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
64 x 8	MCM5003/5303A	125	Open collector	24
64 x 8	MCM5004/5304A	125	2K pull-up	24
512 x 4	MCM7620A	70	Open collector	16
512 x 4	MCM7621A	70	3-state	16
512 x 8	MCM7640A	70	Open collector	24
512 x 8	MCM7641A	70	3-state	24
1024 x 4	MCM7642A	70	Open collector	18
1024 x 4	MCM7643A	70	3-state	18
1024 x 8	MCM7680A	70	Open collector	24
1024 x 8	MCM7681A	70	3-state	24
2048 x 4	MCM7684* <sup>A</sup>	70	Open collector	18
2048 x 4	MCM7685* <sup>A</sup>	70	3-state	18
2048 x 4	MCM7686* <sup>A</sup>	70	Open collector with latches	20
2048 x 4	MCM7687* <sup>A</sup>	70	3-state with latches	20
2048 x 4	MCM7688*	----	Open collector with registers	20
2048 x 4	MCM7689*	----	3-state with registers	20
1K x 8	MCM76LS81*	175	3-state	24
1K x 8	MCM82708* <sup>A</sup>	70	3-state	24

# EPROMs

## MOS EPROMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
1024 x 8	MCM2708C <sup>A</sup>	450	3	24
1024 x 8	MCM27A08C <sup>A</sup>	300	3	24
1024 x 8	MCM68708C <sup>A</sup>	450	3	24
1024 x 8	MCM68A708C	300	3	24
2048 x 8	TMS2716C <sup>A</sup>	450	3	24
2048 x 8	TMS27A16C <sup>A</sup>	300	3	24
2048 x 8	MCM2716C* <sup>A</sup>	450	1	24
2048 x 8	MCM27A16C* <sup>A</sup>	350	1	24
4096 x 8	MCM2532C* <sup>A</sup>	450	1	24
8192 x 8	MCM68764C*	450	1	24

# MOTOROLA MEMORIES

Motorola has developed a very broad range of MOS and bipolar memories for virtually any digital data processing system application. And for those whose requirements go beyond individual components, Motorola also supplies Memory Systems and Micromodules.

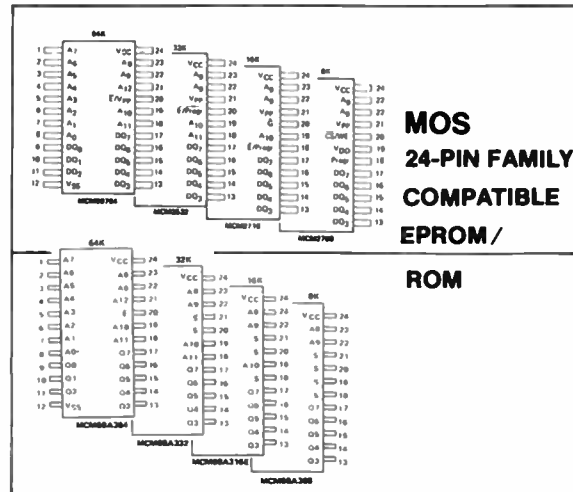
New Motorola memories are being introduced continually. This selector guide lists all those available as of September, 1979. For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Data sheets may be obtained from your in-plant VSMF Data Center, distributors, Motorola sales offices or by writing to:

Literature Distribution Center  
 Motorola Semiconductor Products Inc.  
 P.O. Box 20912  
 Phoenix, AZ 85036.



**MOTOROLA INC.**



# MOTOROLA MEMORIES Selector Guide

# RAMs ROMs PROMs EPROMs

September 1979



**MOTOROLA INC.**



# RAMs

## MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies <sup>1</sup>	No. of Pins
4096 x 1	MCM4027AC-2 <sup>▲</sup>	150	3	16
4096 x 1	MCM4027AC-3 <sup>▲</sup>	200	3	16
4096 x 1	MCM4027AC-4 <sup>▲</sup>	250	3	16
4096 x 1	MCM6604AC	350	3	16
4096 x 1	MCM6604AC-2	250	3	16
4096 x 1	MCM6604AC-4	300	3	16
16,384 x 1	MCM4116BC-15 <sup>▲</sup>	150	3	16
16,384 x 1	MCM4116BC-20 <sup>▲</sup>	200	3	16
16,384 x 1	MCM4116BC-25 <sup>▲</sup>	250	3	16
16,384 x 1	MCM4116BC-30 <sup>▲</sup>	300	3	16
16,384 x 1	MCM4516L-15 <sup>▲▲</sup>	150	1	16
65,536 x 1	MCM6664L-20 <sup>▲▲</sup>	200	1	16

## TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 x 4	MCM93412 <sup>▲</sup>	45	Open collector	22
256 x 4	MCM93422 <sup>▲</sup>	45	3-state	22
1024 x 1	MCM93415 <sup>▲</sup>	45	Open collector	16
1024 x 1	MCM93425 <sup>▲</sup>	45	3-state	16

\*To be introduced.  
 ▲Second source.  
 Heavy black type denotes industry standard part numbers.  
 Operating temperature ranges:  
 MOS 0°C to 70°C  
 CMOS -40°C to +85°C and -55°C to +125°C  
 ECL Consult individual data sheets.  
 TTL Military -55°C to +125°C, Commercial °C to 70°C

<sup>1</sup>MOS power supplies:  
 3 +12, ±5 V  
 1 +5 V  
 All MOS outputs are 3-state except the 2115A which is open-collector.

<sup>2</sup>Character generators include shifted and unshifted characters, ASCII, alphanumeric control, math, Japanese, British, German, European and French symbols.

## MOS STATIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
128 x 8	MCM6810	450	1	24
128 x 8	MCM68A10	360	1	24
128 x 8	MCM68B10	250	1	24
1024 x 1	MCM2115AL-70 <sup>▲▲</sup>	70	1	16
1024 x 1	MCM2115AL-45 <sup>▲▲</sup>	45	1	16
1024 x 1	MCM2125AL-70 <sup>▲▲</sup>	70	1	16
1024 x 1	MCM2125AL-45 <sup>▲▲</sup>	45	1	16
1024 x 4	MCM2114P-20 <sup>▲</sup>	200	1	18
1024 x 4	MCM2114P-25 <sup>▲</sup>	250	1	18
1024 x 4	MCM2114P-30 <sup>▲</sup>	300	1	18
1024 x 4	MCM2114P-45 <sup>▲</sup>	450	1	18
1024 x 4	MCM21L14P-20 <sup>▲</sup>	200	1	18
1024 x 4	MCM21L14P-25 <sup>▲</sup>	250	1	18
1024 x 4	MCM21L14P-30 <sup>▲</sup>	300	1	18
1024 x 4	MCM21L14P-45 <sup>▲</sup>	450	1	18
4096 x 1	MCM6641P-20 <sup>▲</sup>	200	1	18
4096 x 1	MCM6641P-25 <sup>▲</sup>	250	1	18
4096 x 1	MCM6641P-30 <sup>▲</sup>	300	1	18
4096 x 1	MCM6641P-45 <sup>▲</sup>	450	1	18
4096 x 1	MCM66L41P-20 <sup>▲</sup>	200	1	18
4096 x 1	MCM66L41P-25 <sup>▲</sup>	250	1	18
4096 x 1	MCM66L41P-30 <sup>▲</sup>	300	1	18
4096 x 1	MCM66L41P-45 <sup>▲</sup>	450	1	18
4096 x 1	MCM2147C-55 <sup>▲▲</sup>	55	1	18
4096 x 1	MCM2147C-70 <sup>▲▲</sup>	70	1	18
4096 x 1	MCM2147C-85 <sup>▲▲</sup>	85	1	18

## CMOS STATIC RAMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
256 x 4	MCM5101-1 <sup>▲</sup>	450	1	22
256 x 4	MCM5101-3 <sup>▲</sup>	650	1	22
256 x 4	MCM5111-8 <sup>▲</sup>	800	1	22
4096 x 1	MCM6504-45 <sup>▲▲</sup>	450	1	18
1024 x 1	MCM6508-46 <sup>▲▲</sup>	460	1	16
1024 x 1	MCM6508-30 <sup>▲▲</sup>	300	1	16
1024 x 1	MCM6518-46 <sup>▲▲</sup>	460	1	18
1024 x 1	MCM6518-30 <sup>▲▲</sup>	300	1	18

## ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
8 x 2	MCM10143	15	ECL output	24
256 x 1	MCM10144 <sup>▲</sup>	26	ECL output	16
16 x 4	MCM10145 <sup>▲</sup>	15	ECL output	16
1024 x 1	MCM10146 <sup>▲</sup>	29	ECL output	16
128 x 1	MCM10147 <sup>▲</sup>	15	ECL output	16
256 x 1	MCM10152 <sup>▲</sup>	15	ECL output	16
256 x 4	MCM10422 <sup>▲▲</sup>	10	ECL output	24

# ROMs

## MOS STATIC ROMs Character Generators<sup>2</sup>

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
128 x (7 x 5)	MCM6670P	350	1	18
128 x (7 x 5)	MCM6674P	350	1	18
128 x (9 x 7)	MCM66700P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66710P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66714P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66720P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66730P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66734P	350	1	24
128 x (9 x 7)	MCM66740P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66750P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66760P <sup>▲</sup>	350	1	24
128 x (9 x 7)	MCM66770P	350	1	24
128 x (9 x 7)	MCM66780P	350	1	24
128 x (9 x 7)	MCM66790P	350	1	24

## Binary ROMs

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
1024 x 8	MCM68A30P8	350	1	24
1024 x 8	MCM68A308P7	350	1	24
2048 x 8	MCM68A316P91	350	1	24
1024 x 8	MCM68B30AP <sup>▲</sup>	250	1	24
1024 x 8	MCM68A30AP <sup>▲</sup>	350	1	24
1024 x 8	MCM68B308P <sup>▲</sup>	250	1	24
1024 x 8	MCM68A308P <sup>▲</sup>	350	1	24
2048 x 8	MCM68A316EP <sup>▲</sup>	350	1	24
2048 x 8	MCM68A316AP <sup>▲</sup>	350	1	24
4096 x 8	MCM68A332P <sup>▲</sup>	350	1	24
4096 x 8	MCM68A332P2	350	1	24
8192 x 8	MCM68A364P <sup>▲▲</sup>	350	1	24
8192 x 8	MCM68A364P3 <sup>▲</sup>	350	1	24
8192 x 8	MCM68B364P <sup>▲▲</sup>	250	1	24

## CMOS ROM

Organization	Part Number	Access Time (ns max)	No. of Power Supplies	No. of Pins
256 x 4	MCM14524	1200	1	16

# Advances in your field you should be aware of. (And can be —very easily.\*)



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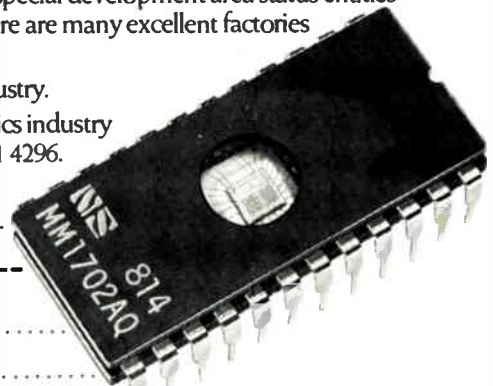
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The silicon chip illustrated (type MM 1702 AQ) is manufactured in the Strathclyde Region by National Semiconductor (UK) Ltd.

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## New products

Computers & peripherals

# Modem runs at 2 megabauds

Low-cost board unit with 30-dB dynamic range uses fm for good noise immunity

It is well established that DMA (direct memory access) block transfers are the fastest and most efficient means for moving large amounts of data into and out of computer memory. For distributed-processing systems in which the various processors are co-located, this presents no problem. However, when the processors are widely separated, telephone lines are typically used to interconnect them, and ordinary telephone lines cannot accommodate DMA speeds.

For computers separated by no more than 25,000 feet, the solution is a combination of a dedicated coaxial cable and a model 30-0078 modem. The 30-0078 operates at any data rate from dc to 2.0 megabauds without adjustment. It employs both frequency modulation and extensive high-pass filtering to reject interference, such as is frequently encountered in industrial and commercial environments. Capable of half-duplex operation over a single cable or of full-duplex operation over two

cables, the 30-0078 is connected to the cable (or cables) by a simple Tee. No directional couplers are required, and multi-drop party lines are easy to set up.

The modem's operation is simplicity itself: the only control signal is a gate signal that is turned on for the duration of the transmission. Messages need no preambles because the receiver detects the very first bit in the message after the carrier is turned on.

The modem has a 30-dB dynamic range, making it possible to connect devices at any point along a cable with no concern for the distance between modems and with no need to make any gain adjustments. Ac coupling to the cable permits safe grounding of each modem at every point along the cable, even in the presence of ground noise circulating in the outer shield.

The modem, whose receiver has a typical bit error rate of less than one bit in  $10^{12}$  for a 20-dB signal-to-noise ratio, is offered in three versions that differ only in their fm carrier frequencies and their maximum data rates. The 0.5-megabaud unit uses a 1-MHz carrier and can transmit up to 50,000 feet over JT3750J cable. Using the same cable, the 1-megabaud modem, with its 3-MHz carrier, has a maximum transmission distance of 32,000 feet. Finally, the 2-megabaud unit (5-MHz carrier) is good for 25,000 feet. Of course, lesser cables may be used when long distances are not involved; using



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**CALIFORNIA:** Glendale, R.V. Weatherford, 6921 San Fernando Rd., Glendale, CA 91201. (213) 849-3451; Palo Alto, Kieruff Electronics, 3969 East Bayshore Rd., Palo Alto, CA 94303. (415) 968-6292; Sunnyvale, TI Supply, 776 Palomar Ave., Sunnyvale, CA 94086. (408) 732-5555; United Components, 480 Oakmead Pkwy., Sunnyvale, CA 94086. (408) 737-7474.

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**IOWA:** Cedar Rapids, Deeco, 2500 16th Ave. SW, Cedar Rapids, IA 52406. (319) 365-7551.

**MARYLAND:** Baltimore, Arrow Electronics, 4801 Benson Ave., Baltimore, MD 21227. (202) 737-1700. (301) 247-5200; Gaithersburg, Cramer/Washington, 16021 Industrial Dr., Gaithersburg, MD 20760. (301) 948-0110.

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**MICHIGAN:** Ann Arbor, Arrow Electronics, 3921 Varsity Dr., Ann Arbor, MI 48104. (313) 971-8220.

**NEW JERSEY:** Camden, General Radio Supply, 600 Penn St., Camden, NJ 08102. (609) 964-8560; Clark, TI Supply, 301 Central Ave., Clark, NJ 07066. (201) 382-6400; Clifton, Wilshire Electronics, 1111 Paulison Ave., Clifton, NJ 07015. (201) 340-1900; Moorestown, Arrow Electronics, Pleasant Valley Ave., Moorestown, NJ 08057. (609) 235-1900; Saddlebrook, Arrow Electronics, 285 Midland Ave., Saddlebrook, NJ 07662. (201) 797-5800.

**NEW YORK:** Farmingdale, Arrow Electronics, 900 Broad Hollow Rd., Farmingdale, NY 11735. (516) 694-6800; Hauppauge, Cramer/Long Island, 129 Oster Ave., Hauppauge, NY 11787. (516) 231-5600; Liverpool, Cramer/Syracuse, 7705 Mallage Dr., Liverpool, NY 13088. (315) 652-1000.

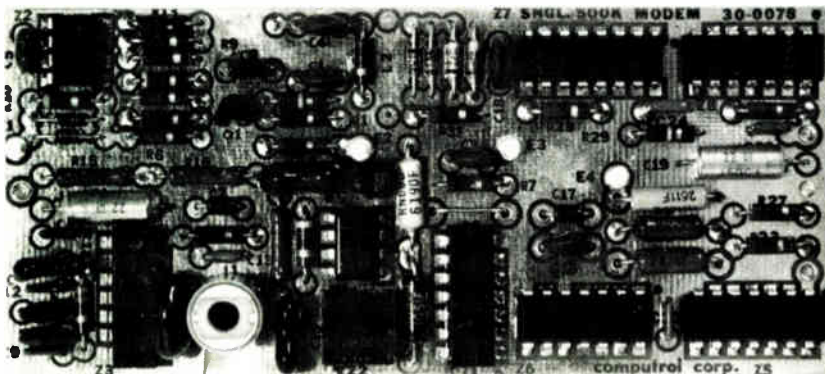
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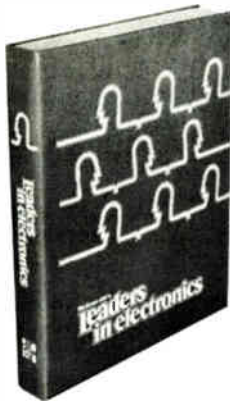
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## New products

RG-59, the distances just cited become 6,000, 5,000 and 4,200 feet,\* respectively.

The 30-0078 asynchronous modem is contained on a printed-circuit card with dimensions of 2 by 4.5 in. Its 0.375-in. height permits mounting in systems with half-inch centers.

In lots of 100 to 249, the 30-0078 sells for \$240. A synchronous version, the 30-0080, is priced at \$400 in the same quantities. Both units will be available in November.

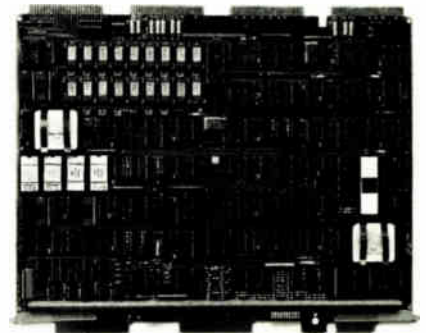
Computrol Corp., 15 Ethan Allen Highway, Ridgefield, Conn. 06877. Phone (203) 544-9371 [361]

## Communications processor lightens CPU chores

An intelligent communications processor that can take control of data-communications tasks releases the central processing unit for other jobs, thereby improving the performance of the total system. The Intelligent Network Processor is, therefore, a significant addition to the HP 3000 series of minicomputers.

Based on the proprietary silicon-on-sapphire microcomputer chip (MCC) and 32 kilobytes of on-board random-access memory, the single-board processor can control up to four synchronous data-communications lines operating at data-transmission speeds as high as 56 kilobits/s. Until now the HP 3000 could only operate the slower asynchronous communications lines or, through a controller, a single synchronous line at 9,600 bits/s.

Robert T. Bond, HP's General Systems division marketing man-





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## New products

ager, notes that "20% of a CPU's resources [that is, time and memory] can be taken up by four synchronous communications lines. But with the Intelligent Network Processor, that's reduced to only 2%."

Because of its processing power, the INP can handle the RJE 3000 software that simulates IBM's 2780 and 3780 remote job-entry terminals. And the company says the new unit is especially useful on computers equipped for HP's Distributed Systems Network Architecture.

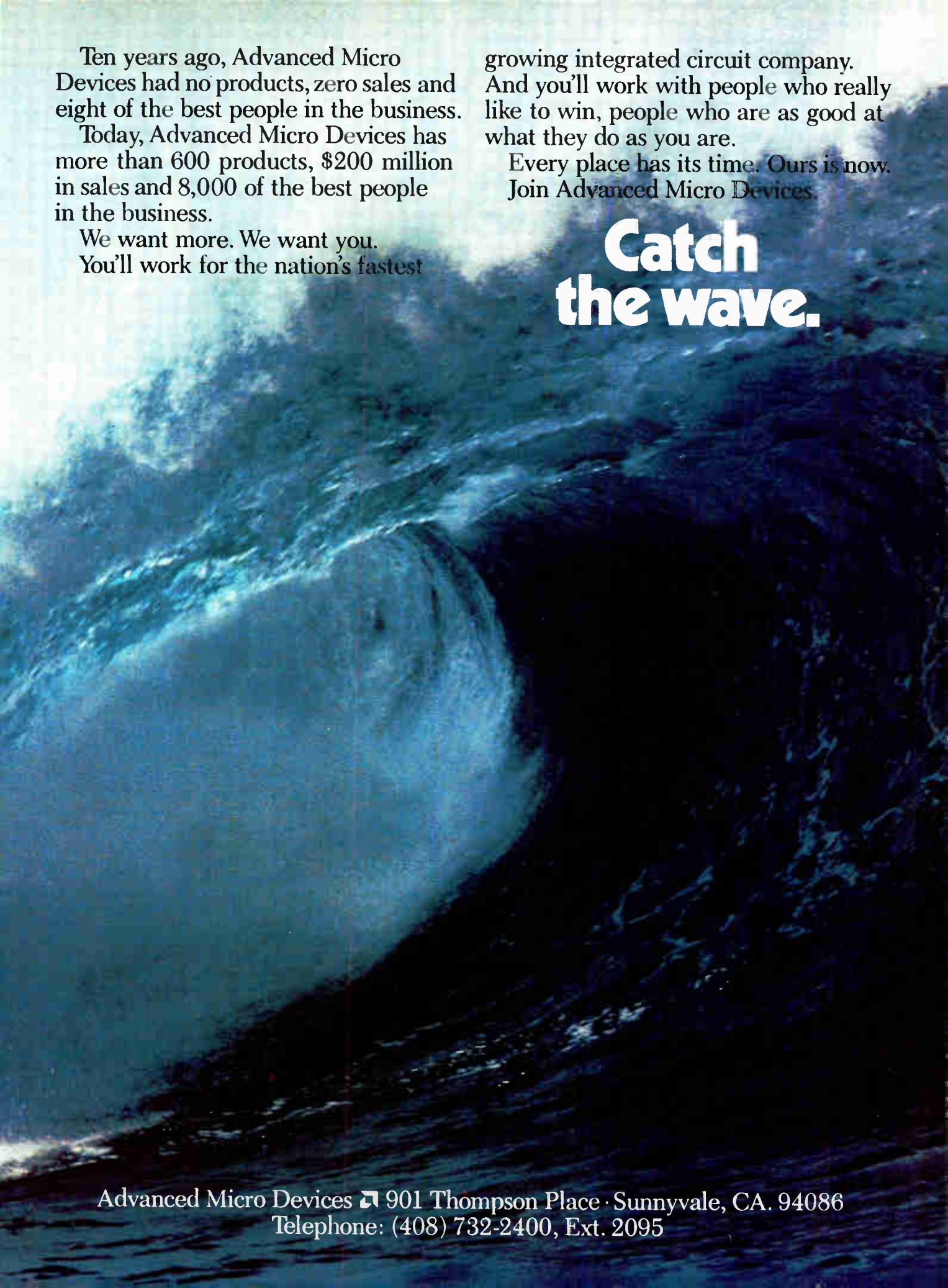
A more compact member of the HP 3000 series is also available now. Called the HP 3000 series 30, it uses the same central processor as the 10-month-old series 33 [*Electronics*, Oct. 2, 1978, p. 39], but comes in smaller configurations ranging from 256 kilobytes of main memory to a maximum of 1 megabyte—half of the series 33's maximum memory.

With a 1-megabyte floppy disk, four asynchronous terminal ports, a systems console, a 20-megabyte hard disk, and eight input/output expansion slots, the basic series 30 sells for \$49,750. With 1 megabyte of memory, the same system is priced at \$64,750. Delivery times are between 12 and 16 weeks. The Intelligent Network Processor is priced at \$4,500, and delivery time is estimated at eight weeks.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [363]

## Word-processing system stands alone, shares logic

There has been little middle ground in word-processing equipment: users have had to choose between stand-alone, single-processor systems and multi-user, centralized systems with many terminals. While the larger systems offer far more storage capacity and shared-data abilities, the smaller ones provide better reliability and operator productivity. But a "shared-resource system" recently introduced by CPT Corp. [*Electronics*, Sept. 13, p. 33] combines these attributes to give the user stand-alone functionality and



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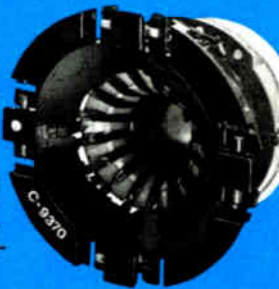
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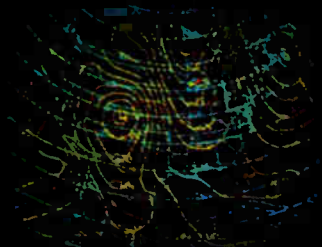
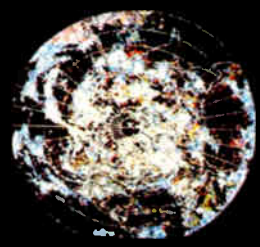
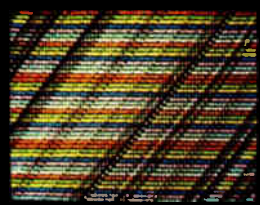
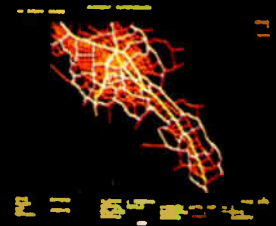
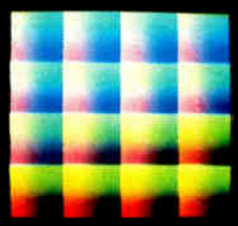
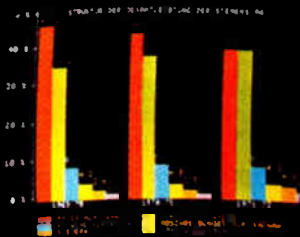


shared-logic capability.

A CPT 8000 word processor provides the basis for these new systems. Each 8000 has its own 8080 microprocessor and features dual diskette storage, while supporting two printers as well as an optical character-recognition input, a photo-composition output, or a telecommunications link via an asynchronous line protocol. To build up a multi-user, Wordpak system, the user may add one of two 14-in., 25-million-character, Winchester-type fixed-disk drives (from Shugart), in addition to new interfaces. The CPT 8040 disk drive is the basic unit for Wordpak I systems, while Wordpak II systems use the CPT 8050 disk drive, which has its own microprocessor controller, memory, and input/output logic. The CPT 8042 is a 25-million-character expansion module providing additional storage on the Wordpak II system, for a total of 50 million characters.

A Wordpak I configuration can combine up to four individual CPT 8000 workstation clusters, all of which may have access to the 25-million-character CPT 8040 disk drive. The Wordpak II system, field-upgradable from the Wordpak I, will support up to eight CPT 8000 workstations, and allow these stations access to up to 50 million characters. At this time, a single stand-alone CPT 8000 can support telecommunications links, as well as do simple number calculations (number processing) and word processing. The company hopes to add data-processing capabilities to the system later this fall.

Deliveries of Wordpak I systems



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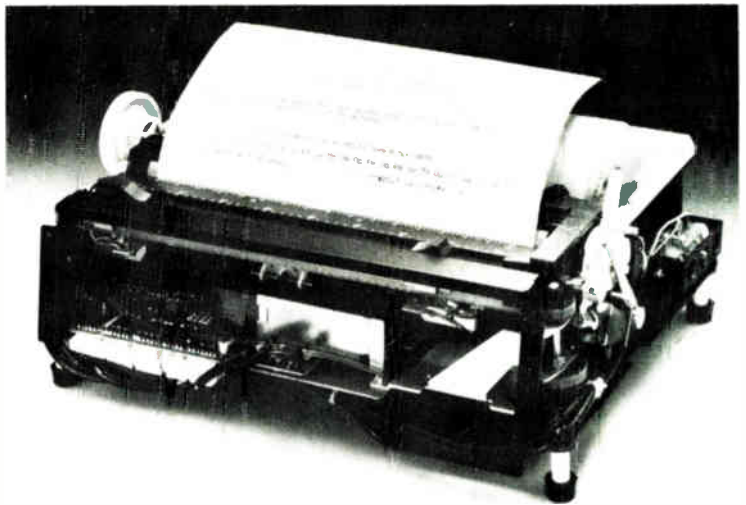
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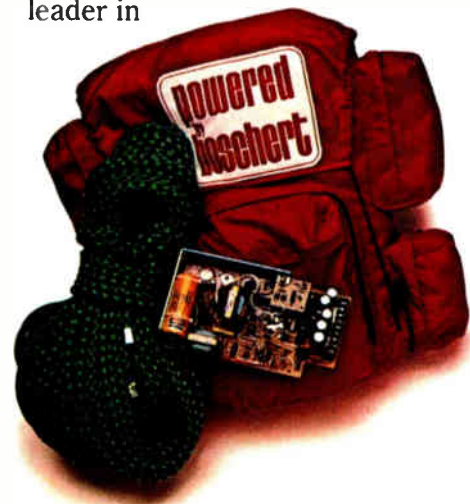
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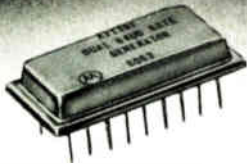
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Communications

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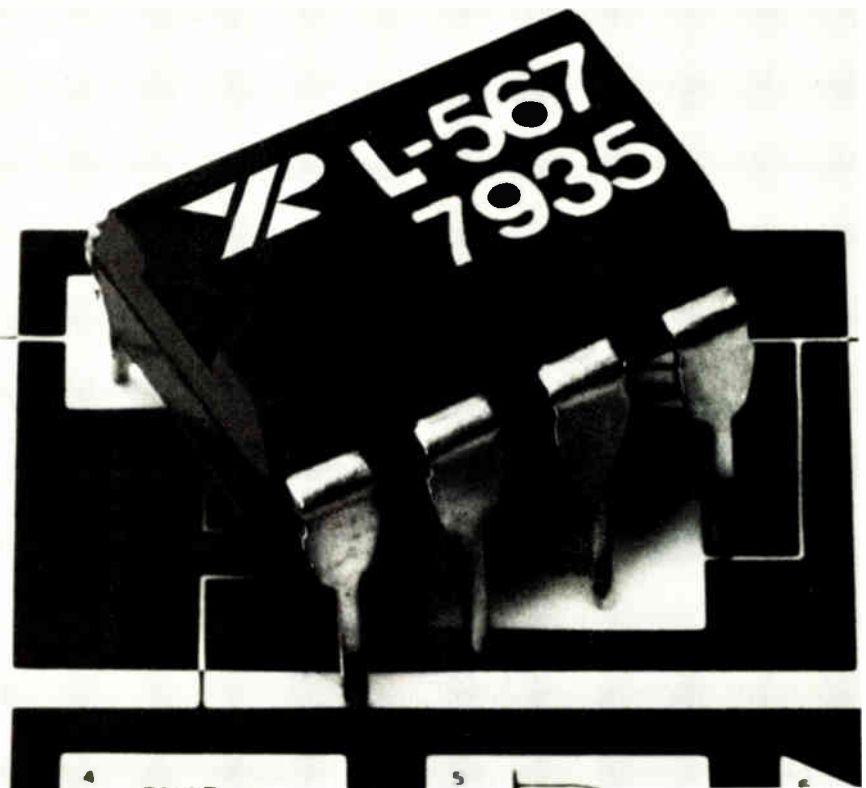
About 10 years ago, Signetics introduced the 567 monolithic tone decoder, which became so popular that even today Signetics and other suppliers such as Exar Integrated Systems Inc. and National Semiconductor Corp. together sell several million units a year. Now Exar is bringing out an enhanced version that dissipates about a tenth the power of the popular standard part.

"It's intended for battery-powered equipment," declares Alan B. Grebene, Exar vice president, ticking off such applications as remote control of satellite and instrumentation telemetry gear, sequential tone decoding, and communications paging.

The 5-v XR-L567 micropower tone decoder has a typical quiescent power requirement of 4 mW, he says. Moreover, it achieves that low figure without sacrificing the conventional 567's features of oscillator stability, frequency selectivity, and detection threshold. Grebene estimates that 30% to 40% of 567 users will pay the price premium to cut down on power consumption.

Pin-compatible with the phase-locked-loop 567, the XR-L567 contains a phase detector, a low-pass filter, and a current-controlled oscillator, which make up the basic phase-locked loop. In addition, there's a second low-pass filter and a quadrature detector that let the circuit recognize the presence or absence of an input signal at the center frequency.

Grebene says that ion implantation makes the new unit's low power dissipation possible. "Low-power circuits require high resistor values," he says, "but there's no way you can make a high-value resistor without taking up area, because the value is proportional to length." With ion implantation, Exar has been able to





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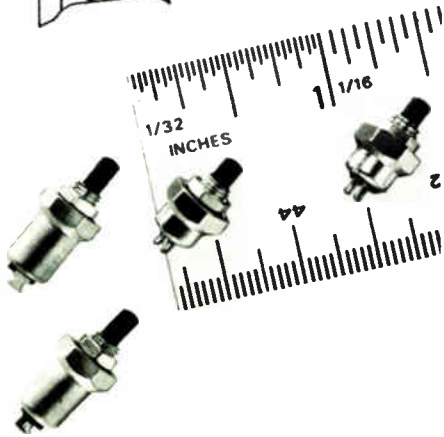
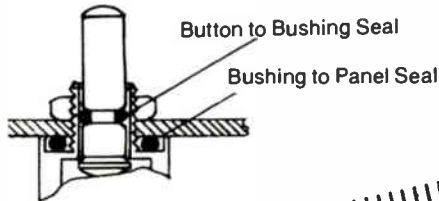


One of The Signal Companies

Circle 221 on reader service card



# New Ultraminiature Grayhill Pushbutton Switch Provides a Watertight Seal to the Front Panel.



Designed to be the smallest shaft and panel sealed pushbutton switches available anywhere, these new SPST switches have a host of applications in medical electronics, outdoor equipment, electronic scales, etc.

They're available in both Normally Open and Normally Closed versions, with red or black integral buttons. Red, white, or black accessory caps are available at additional cost.

The switches feature momentary action, butt contacts, and are rated to make and break 1/2 amp, (SPST-N.O.), 1/4 amp (SPST-N.C.), 115 VAC, resistive load for 250,000 operations. Total travel is 0.035" ± 0.015" for the N.O. switch (Part No. 39-351), 0.042" ± 0.010" for the N.C. (Part No. 39-352).

For complete specifications, let us send you Bulletin #296.



561 Hillgrove Avenue • LaGrange, Illinois 60525  
(312) 354-1040

## New products

increase the values by 15 times at no increases in area, he says.

The XR-L567 has a center frequency adjustable from 0.01 Hz to 50 kHz and can sink up to 10 mA of load current, compared with 0.01 Hz to 500 kHz and 100 mA for the conventional 567. Operating temperature range is 0° to 75°C and maximum power dissipation for the 8-pin device is 385 mW (ceramic package) and 300 mW (plastic). Bandwidth, center frequency, and output delay are independently determined by the selection of four external components. The price is \$1.23 in lots of 100, about 50% higher than the 567. Exar Integrated Systems Inc., 750 Palomar Ave., Sunnyvale, Calif. 94088 [401]

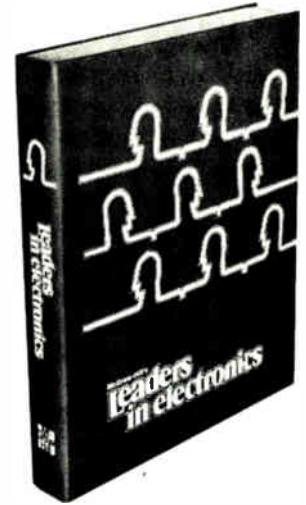
Detector spans 10 MHz to 34 GHz, sells for \$250

Covering the 10-MHz-to-34-GHz range, a recently introduced detector is suited for applications requiring output-voltage tracking over a wide dynamic range. Using a newly developed version of the SMA connector that is compatible with all other SMA connectors, the 70S50 detector is available in two models: the 70S50A, with a frequency range from 10 MHz to 18.5 GHz; and the 70S50B, with a range from 10 MHz to 34 GHz. The input return loss on the A model is 22 dB from 10 MHz to 8 GHz and 18 dB from 8 GHz to 18.5 GHz. Frequency response over the entire range is ±0.6 dB.

For the B model, the input return loss is the same as for the A version through 18.5 GHz; from 18.5 to 26.5 GHz, it is 15 dB, and from 26.5 GHz through 34 GHz, it is 10 dB. Frequency response is the same as



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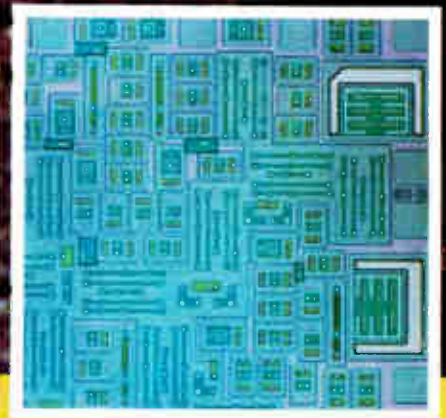
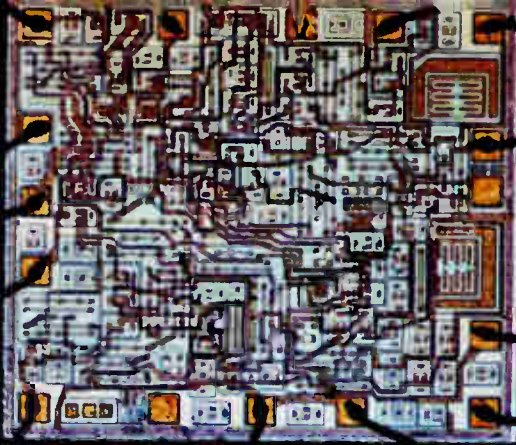
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## This integrated circuit was manufactured to a custom design and delivered in a matter of weeks.

Section of an Exar Master Chip before customizing. Note the individual circuit components already on-chip, but still unconnected. After the customer has designed circuit connections according to his system needs, Exar prepares a final mask and fabricates the custom chip, as shown in large photograph above.

**YOU CAN CUT DEVELOPMENT TIME UP TO NINE MONTHS ON BIPOLAR AND I<sup>2</sup>L CUSTOM CHIPS... WHILE YOU SLICE COSTS TO THE BONE... THROUGH THE UNIQUE "SEMI-CUSTOM DESIGN PROGRAM" FROM EXAR INTEGRATED SYSTEMS.** Compared to traditional development times for custom ICs, which frequently exceed one year, and tooling costs which can be five to ten times greater, this new concept allows custom chips to be justified economically at far smaller quantities than previously thought practical.

### How the semi-custom idea works.

Exar's standardized circuits contain undedicated active and passive components such as transistors, resistors, logic gates, etc., fabricated onto the chip, but left unconnected. You choose how to interconnect these components to create your own custom circuit. The actual interconnection process is simple, requiring only one to three layers of tooling. As a result, development time compresses drastically, becomes far less expensive and virtually risk free.

### Choose from eight different chips.

Five of the standard semicustom chips are bipolar, and are best suited for linear designs. Some (XR-A100, XR-C100, XR-F100) feature high current NPN output transistors, making them suitable for drive circuits. The others (XR-B100, XR-D100), more appropriate for signal amplification or control circuits, contain only small signal, low current transistors. All, however, present the designer a wide variety of NPN and PNP transistors, Schottky diodes, various resistors and ample bonding pads.

Exar's three I<sup>2</sup>L digital chips (XR-300, XR-400, XR-500) contain high density I<sup>2</sup>L logic arrays and bipolar interface circuitry. Outwardly they look and per-

form like a bipolar LSI chip, readily interfacing with TTL or MOS level signals. This feature, incidentally, makes it very convenient to retrofit I<sup>2</sup>L LSI designs into existing MOS or TTL logic systems.

And Exar has in development additional semi-custom chips offering even greater applications flexibility.

### If you decide to modify your design.

Even after evaluation of initial design prototypes, if you see a need to modify the custom chip, a new design iteration usually takes less time than the original development cycle. And typical costs of additional design cycles are proportionately less than the original prototype development cost.

### What about second sources?

This is one of our most asked questions. In response, Exar has made alternate-source agreements with other IC manufacturers, so you can specify and order custom circuits with confidence.

### Testing, testing.

After prototype acceptance of semi-custom devices, Exar will develop software and fixtures for fully testing all production ICs. Production devices receive 100% electrical testing, and are

screened to agreed-upon Acceptable Quality Level (AQL) standards. Charges for this test engineering are nominal, and vary depending on the complexity of the tests.

### Semi-custom to full custom. For when the numbers get big.

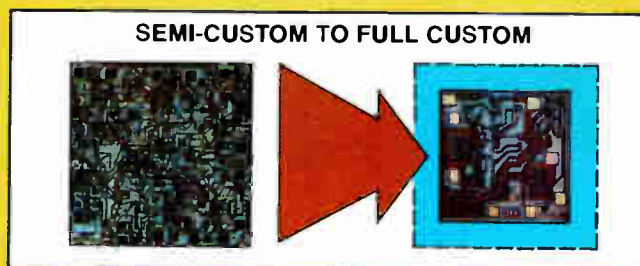
Because Exar manufactures its own wafers, it can grow with your needs. As your product matures we can convert your semi-custom chip into a customized IC. Consider the advantages: You get the quick, inexpensive turnaround of semi-custom chips, providing prototypes and initial production units; then when your design has proven itself and your market has developed, the subsequent full custom product provides further cost savings at high volume production... often with a significant improvement in product performance!

### Design kits make it simple.

Exar provides linear and digital design kits, including circuit components for breadboarding, comprehensive design manuals and layout worksheets corresponding to Exar's master chips. These, as well as technical assistance when you need it, will speed and simplify your preliminary steps toward custom IC design.

### Learn the economics and advantages of semi-custom.

Exar's entire semi-custom story is detailed in a 40-page data book, "Semi-Custom IC Design Programs." For your copy, write on company letterhead to your nearest Exar representative or to Exar, 750 Palomar Ave., Sunnyvale, CA 94086.



Exar can convert your semi-custom chip to a custom IC, reducing chip size, saving money, and often providing added performance benefits.



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### Germanium and silicon transistors

low (up to 300 mW) for medium (up to 1.5 W) and high (above 1.5 W) power ratings, and for low (up to 3 MHz), medium (up to 30 MHz) and high (above 30 MHz) frequencies.

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## New products

for the A through 18.5 GHz also, but from 18.5 to 26.5 GHz it is  $\pm 1.2$  dB, and from 26.5 to 34 GHz, it is  $\pm 1.2$  dB with a 2.5-dB slope.

The zero-bias Schottky diode modules used in the detectors are field-replaceable—for the A version, the price is \$85, and for the B, it is \$100.

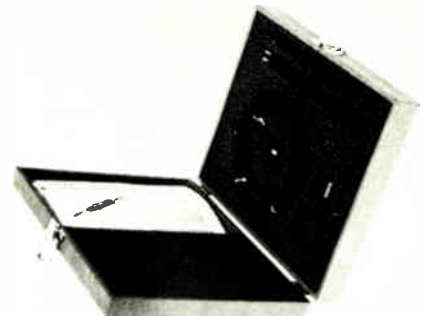
The 70S50A sells for \$195, and the 70S50B for \$250. Delivery time for the units is 60 days.

Wiltron Co., 825 East Middlefield Rd., Mountain View, Calif. 94043. Phone Walt Baxter at (415) 969-6500 [403]

Kit allows users to practice with fiber-optic technology

Intended for use by design engineers and laboratory technicians in the computer, electronics, optical, and communications fields, the Fiber Optic Engineering Kit will allow these users to gain experience in applying the new fiber-optic technology. The kit includes an assortment of plastic-fiber cable and connector components, together with the tooling necessary to assemble bidirectional links.

The kit uses single plastic fibers.



Optoelectronic devices supplied with the kit have terminated permanent fiber pigtailed which require only one type of fiber-to-fiber connector. Also included with the kit is a booklet explaining the fundamentals of both wave propagation and coupling techniques.

Price per kit is approximately \$300, with delivery from stock to six weeks; price and delivery depend on

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DA50-1H



DAX200-1H



DAX500-2H

### SPECIFICATION

Model	DA50-1H	DA200-1H	DAX200-1H	DAX300-1H	DAX300-2H	DAX500-2H
Output Power	50VA	200VA	200VA	300VA	300VA	500VA
Input Voltage	DC11 ~ 16V	DC11 ~ 16V	DC11 ~ 16V	DC11 ~ 16V	DC22 ~ 32V	DC22 ~ 32V
Output Voltage	AC115(230)V	AC115(230)V	AC115(230)V	AC115(230)V	AC115(230)V	AC115(230)V
Output Regulation	Less than +5%	Less than +5%	Less than +5%	Less than +5%	Less than +3%	Less than +3%
Output Distorsion	Less than 10%	Less than 10%	Less than 5%	Less than 5%	Less than 5%	Less than 5%
Dimension (mm)	178 × 110 × 233	178 × 153 × 213	180 × 183 × 261	180 × 183 × 391	180 × 183 × 391	220 × 350 × 300
Weight (kg)	6.0	6.3	7.0	12.0	12.0	15.0

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## New products

which components the user selects. T&B/Ansley Corp., Subsidiary of Thomas & Betts Corp., 3208 Humboldt St., Los Angeles, Calif. 90031. Phone Roland Kolu at (213) 223-2331 [404]

### Edge-emitting diode extends emissions to 1,300 nm

Using an indium-gallium-arsenide-phosphide (InGaAsP) pellet, a newly announced infrared edge-emitting diode has an output that extends out to 1,300 nm. The RCA C86013E produces a high radiance emission pattern by utilizing an oxide-isolated stripe contact. The device is constructed with a length of fiber-optic cable terminated with a Siacor T11 connector; the cable is internally coupled to the emitting region of the chip.

The device has a typical continuous power output of 10 mw when driven by a forward current of 200 mA. Typical rise time is less than 10 ns.

The device is particularly useful in applications where fiber optic materials with low attenuation losses in the spectral region beyond the OH-absorption band may be utilized. In quantities of one to nine, the device sells for \$1,129 with a delivery time of 30 days.

RCA Electro-Optics and Devices, Lancaster, Pa. 17604. Phone (717) 397-7661, Ext. 2377 [405]

### Fiber attenuation test set measures many parameters

Capable of measuring fiber attenuation under many different launch conditions, the AT-1 fiber attenuation test set has a monochromator with a special grating to cover 600 to 1,600 nm at high efficiency. The electronic equipment in the system is based on a microprocessor-controlled ratiometric lock-in amplifier, and provides time-sensitivity products to within a factor of four of the theoretical limits. An RS-232-C interface is used for remote control and data

Electronics/September 27, 1979

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polyester, polycarbonate and polypropylene capacitors in foil/foil versions and metalized, aluminum-electrolyte capacitors, tantalum capacitors with liquid electrolyte, tantalum capacitors with solid semiconductor electrolyte, ceramic capacitors.

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## AND FURTHER

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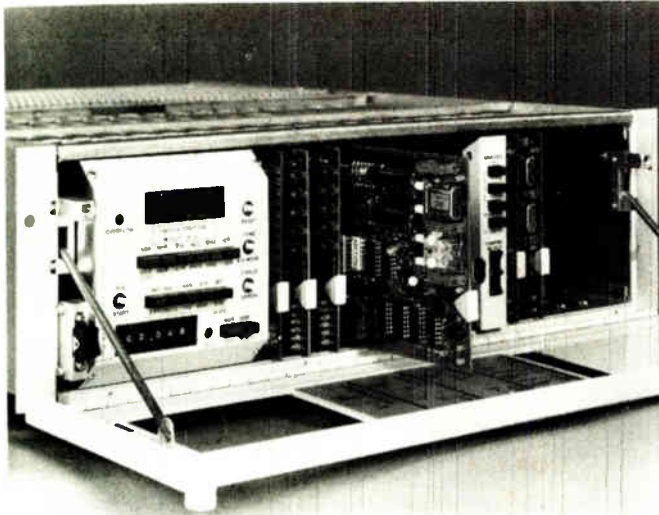
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**Ampex calls it the *M<sup>2</sup> Digital Encode/Decode Unit*. You'll call it the most cost-effective modem you've ever seen for high density digital multi-channel transmission applications.**

Used in conjunction with an analog instrumentation recorder, the Ampex *M<sup>2</sup> Encode/Decode Unit* gives you a digital capability of 5 megabits/second at 120 ips, working in Biphase-L, Miller or *M<sup>2</sup>* codes. And you can get as many as 10 channels of record/playback in a package only 5½ inches high by 19 inches wide.

The built-in test option functions as an error counter with a digital readout to diagnose input rates, and it also serves as both a tape and a total system certification system, displaying number of errors in either  $10^6$  or  $10^8$  bits. It can also be used as a frequency counter.

Use this unique unit as a digital recording front end, as a self-standing modem on wideband telephone and a signal circuits, or as a multichannel diagnostic adjunct. Power supply is 115/220V, 47 to 400 Hz, and price ranges from about \$6,000 to \$12,000 depending upon channel count and installed options.

Rene Chikhani can provide complete technical and performance specifications, and he'll work with you on custom system applications. Call Rene at 415-367-2758, or write to him at Ampex Data Systems, 401 Broadway, Redwood City, California 94063.

## AMPEX

### New products

processing by an external device.

Selector wheels provide controls for the spot size (from 15  $\mu\text{m}$  to 300  $\mu\text{m}$ ), launch and exit numerical apertures (from 0.3 to 0.05), order-sorting filters for filtering harmonics from the monochromator output, and the selection of different sources and different detectors.

Prices for the test set start at \$25,000. Delivery time is within 120 days.

Fiberguide Instruments, 1101B State Rd., Princeton, N. J. 08540. Phone John Henness at (609) 921-9127 [406]

### Digital data link transfers data without modems

Providing multiple channel data transfers without the use of modems, a 32-channel digital data link significantly lowers the cost of interfacing computers with each other and with peripheral devices. The data link consists of two interface electronics units interconnected by a ruggedized fiber-optic cable to allow totally electromagnetic-interference-free multiple channel interconnections over long distances—up to 6,500 ft.

Time-division multiplexing combined with the fiber optics also provides other benefits, such as the elimination of large, unwieldy wire cables, ground loops, and grounding problems. In asynchronous applications, 32 channels may operate completely independently at a rate of up to 50 kilobits/s. Sixteen channels can operate at up to 100 kilobits/s, and 8 channels at up to 200 kilobits/s.

In synchronous byte-parallel applications, externally clocked rates are: 500 kilobits/s for 32-bit; 1 megabit/s for 16-bit; and 2 megabits/s for 8-bit.

Computer or peripheral I/O interfaces can be supplied as MIL-STD-188C, RS-232-C, or others.

The price of a 32-channel digital data link is \$12,000 for full-duplex operation; cabling is extra.

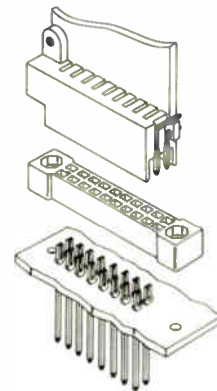
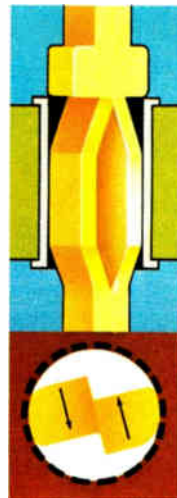
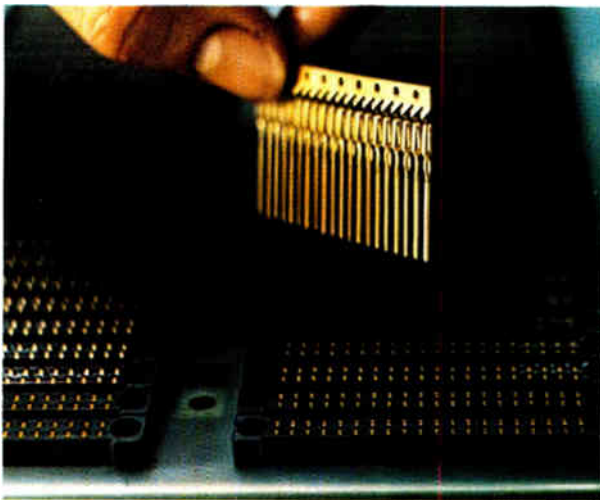
Harris Corp., Fiber Optic Systems, P. O. Box 37, Melbourne, Fla. 32901. Phone Dick Stackhouse at (305) 724-3518 [407]





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ACTION PIN contact's two spring members compress in opposite directions to exert force against hole.

ECONOMATE V connectors present some truly worthwhile opportunities for designers. They utilize the AMP ACTION PIN—a compliant design contact which gives you positive retention on a standard pc board. No solder. No aluminum plates. So with ECONOMATE V connectors you can reduce wiring. You can shorten leads. You can design higher speed systems—all at lower cost and less weight.

The tuning fork contact design incorporates all the features that assure military reliability. Performance has been excellent, with several billion hours of successful service.

These components are designed specifically for panels using two-sided or multi-layer pc boards. And AMP is fully equipped to supply ECONOMATE V panels and products which will meet the anticipated requirements of the new military specification for SEM and ISEM assemblies.

Fully tested ECONOMATE V panels can be supplied in sizes up to 22 x 28 inches (558.8 x 771.2 mm) using two-sided or multi-layer boards from .093 inches (2.36 mm) to .160 (4.06 mm) thick.

The AMP Technical Staff is ready to help you establish those design parameters and solve equipment problems to maximize the quality and efficiency in your packaging. Just call the AMP ECONOMATE Information Desk at (717) 564-0100, Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

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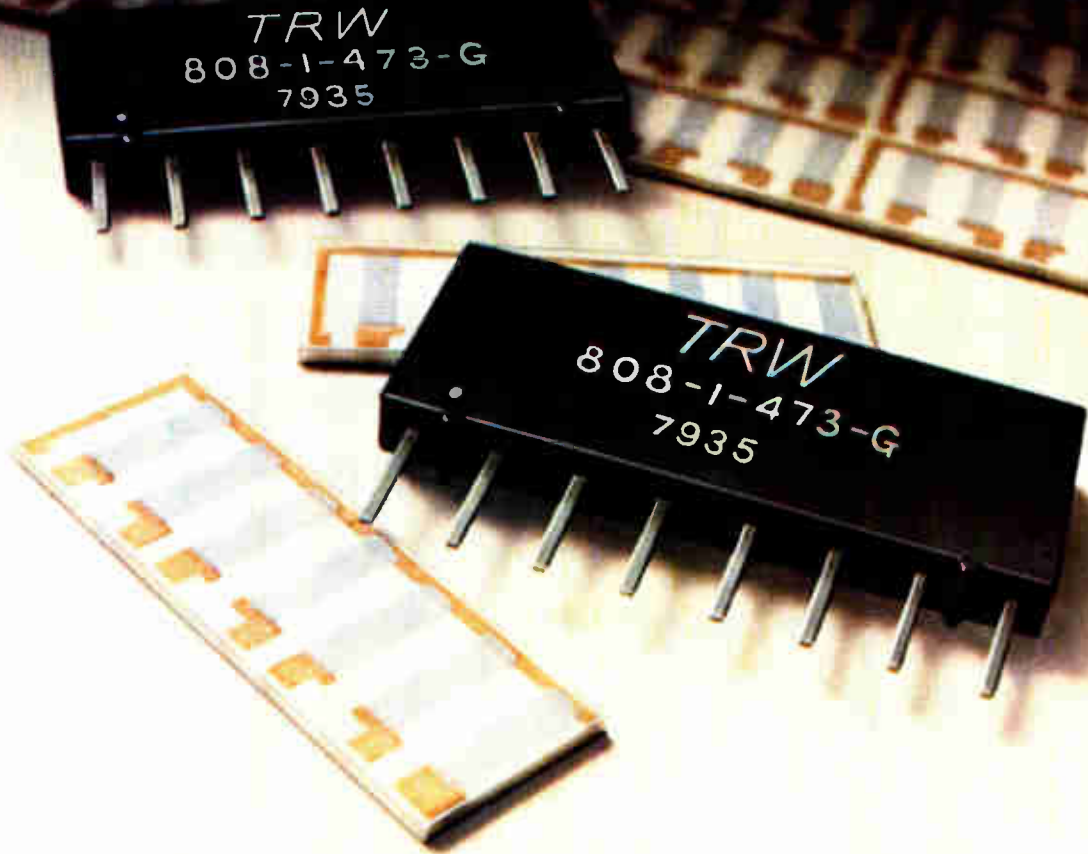
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## New! TRW Series 800 Single-in-line Thick Film Networks.

TRW's cermet thick film networks perform like they were made with precious metals. Except that our system is totally non-noble, *eliminating* gold, silver and platinum group metals entirely.

Take our patented TanTin™ resistive material. It's a tin oxide system fired in inert N<sub>2</sub> at 1000°C. Our own thick film copper conductors are also fired at very high temperatures, producing an exceptionally rugged, stable resistor network. And an IR100 award winner.\*

Our new series 800 SIP's come in a transfer molded package in 6, 8, and 10 pin configurations, dimensionally clean and saving PCB real estate.

For example, 808-1 7 resistor SIP uses < 46 mm<sup>2</sup>. That's less than one discrete ½W resistor laying flat on the board.

Now, you can get noble performance, without noble metals. Look:

*Resistance Range* = 33Ω-1 Meg, ± 2, 5% tolerance laser trimmed.

*Schematics* include N-1 common, N/2 isolated resistors.

*Power Ratings* are 1.5-2.7W / package, 0.3-0.5W / resistor.

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See EEM '79-'80 Master Catalog pp 3644-45

Also ask for our low profile SIP and DIP configurations.

For more information contact your local TRW/ECG sales office or TRW/IRC Resistors, an Electronic Components Division of TRW Inc., Greenway Road, Boone, N.C. 28607. Dept. N, (704) 264-8861.

\* (TM) TanTin (a TRW trademark), received *Industrial Research / Development Magazine* award as one of the top 100 industrial product developments of 1978.

**TRW** IRC RESISTORS  
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# Suddenly your last year's Electronics Buyers' Guide is as outdated as last year's phone book

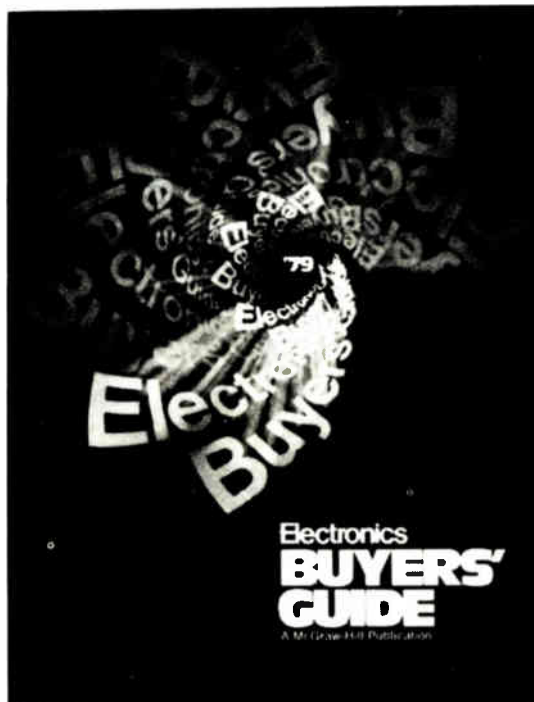
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Allan Haynie, Wordstream's Vice President of Operations



The Wordstream Corporations are subsidiaries of MAI Inc. They manufacture and market the Wordstream™ word processor, a shared logic system capable of handling 12 video display terminals, 10 diskette drives and three printers at once.

At the heart of the Wordstream system, you'll find Augat wirewrap\* panels. Allan Haynie, Wordstream's Vice President of Operations, gives the details. "We use a large Augat board with about 250 integrated circuit chips in each printer station, diskette station, visual display and CPU. These boards are fabricated for us at Augat manufacturing facilities in Attleboro and Mashpee, Massachusetts and El Campo, Texas. Wire-wrapping is performed at their Datatex subsidiary in Houston."

At one time, Wordstream assembled their own IC panels. When asked why they switched to Augat wire-wrap, Allan Haynie replied, "basically, there were two reasons - the economy of Augat wirewrap panels and the service of Augat engineers. For

example, Augat people worked closely with ours to develop a prototype board using their Data-logic™ computer-aided design service. They also designed the most economic way to wrap the boards. As a result, we've saved time and money during our prototype and design stages."

In the past, some users felt that wire-wrapping was not cost effective in large volume programs. Wordstream's experience shows that the opposite is true. Says Haynie; "because Augat supplies completely wired boards, our in-process inventory costs are significantly reduced. In addition, Augat panels give us the flexibility to implement design

changes on the production line and in the field quickly and easily. We don't have to replace boards, just rewire them. And that means we can assure our customers that



their Wordstream system will always remain at the state of the art.

Even our final quality control is simplified with IC's replaced right at the test stations quickly and easily with no need for routing through production."

If you'd like to save time and money from prototype through production, listen to the words of Allan Haynie at Wordstream. Call your nearest Augat representative. Or contact us directly, Augat Incorporated, 33 Perry Avenue, P.O. Box 779, Attleboro, MA 02703. Tel. 617-222-2202.

European Headquarters - Augat SA - France: 9 allée de la Vanne, (Z.I. Sofilic) B.P. 440 Cedex/94263 Fresnes, France. Tel: 668.30.90. Telex: 201.227. AUGSAF.

\*Registered trademark of Gardner Denver

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## New products

### Components

## Film capacitors are smallest yet

Metalized-polyester-film devices have 2.5-mm lead spacing and 63-V dc rating

A family of metalized-polyester-film capacitors is claimed to be the smallest of their kind. They have a lead spacing of only 2.5 mm, making them well suited for use on tightly packed printed-circuit boards. Capacitance values of the self-healing MKS 02 series are between 0.01 and 0.1  $\mu\text{F}$  with a tolerance of  $\pm 20\%$ .

The devices, which are the successors to a line of subminiature capacitors introduced in 1974, owe their smaller size to the use of an extremely thin film, typically 1.5  $\mu\text{m}$  thick. Despite this very thin dielectric, the devices are rated to handle 63 v dc. Their range of operating temperatures extends from  $-55^\circ$  to  $+100^\circ\text{C}$ , and their insulation resistance, at  $20^\circ\text{C}$ , is more than 10,000  $\text{M}\Omega$ .

Compared to multilayer and tantalum capacitors, polyester-film types are much less sensitive to voltage peaks (these can handle about 200 v), have higher insulation resist-

ance, and have a loss factor that is an order of magnitude lower. Moreover, the capacitance of the polyester-film units is less sensitive to temperature.

Pricing on the new capacitors is not yet firm, but the manufacturer says that the price will be "lower than that of multilayer ceramic capacitors of the same size."

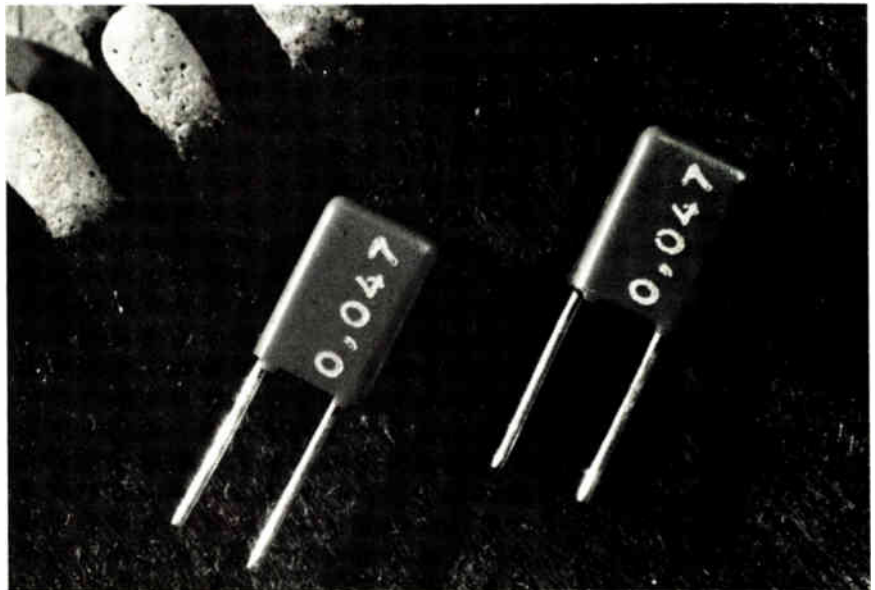
The Intertechnical Group Inc., P. O. Box 23, Irvington, N.Y. 10533. Phone (914) 591-8822 [341]

Outside the U. S.: Wilhelm Westermann (WIMA), 6800 Mannheim 1, P. O. Box 2345, West Germany [342]

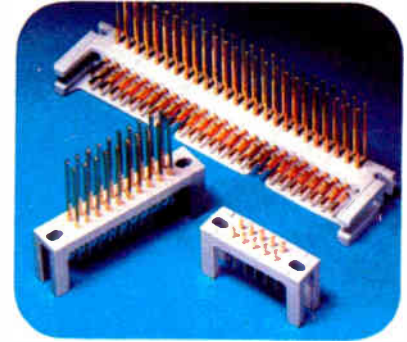
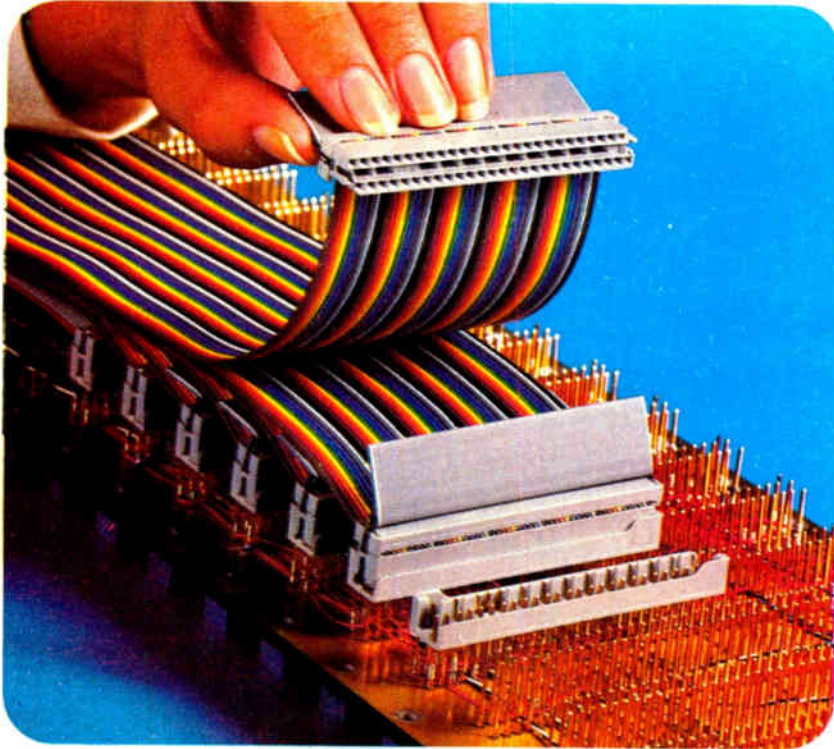
### Mercury-film relay operates in any position

Unlike conventional mercury-wetted relays, the W1728 operates in any mounting position. It features bounce-free performance and self-healing contacts. At loads ranging from 2 A to as low as 1 pA, reliability exceeding two billion mean cycles between failures may be expected at a 90% confidence level. Contact resistance varies by no more than 0.02  $\Omega$  over the life of the relay.

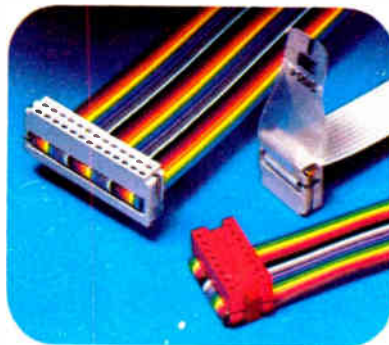
The LC2 switching capsule at the heart of the W1728 is hermetically sealed and uses a film of mercury rather than a mercury reservoir to wet its welded-metal contacts. In



# Want simpler backplane connections? Come to the source.



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For more information on Scotchflex products call 612-733-3350.

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## New products



contrast with fragile reed switches, the mercury-film device withstands shocks of 30 g. The switch capsule and the coil both are encapsulated in hard epoxy for added strength.

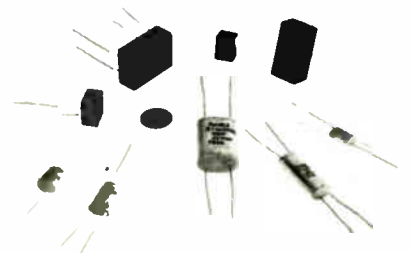
The relay, which is aimed at applications in telephony, data acquisition, medical electronics, and automatic testing, sells for under \$1.80 in large production quantities.

Fifth Dimension Inc., 707 Alexander Rd., Princeton, N. J. 08540. Telephone (609) 452-1200 [343]

## Capacitors with four leads have few failures

Series K high-reliability, metalized-polycarbonate capacitors, each having four axial leads (series K 14) or four radial leads (series K 54) are designed for applications where low-probability or momentary failure is intolerable.

Generally, in metalized-dielectric capacitors, connections are made between leads and windings by means of a metal spray deposited at the ends of the winding. The thickness of deposited metal at this junction is about  $10^{-2}$   $\mu\text{m}$ , which makes the junction the capacitor's most vulnerable point and increases the probability of failure due to high



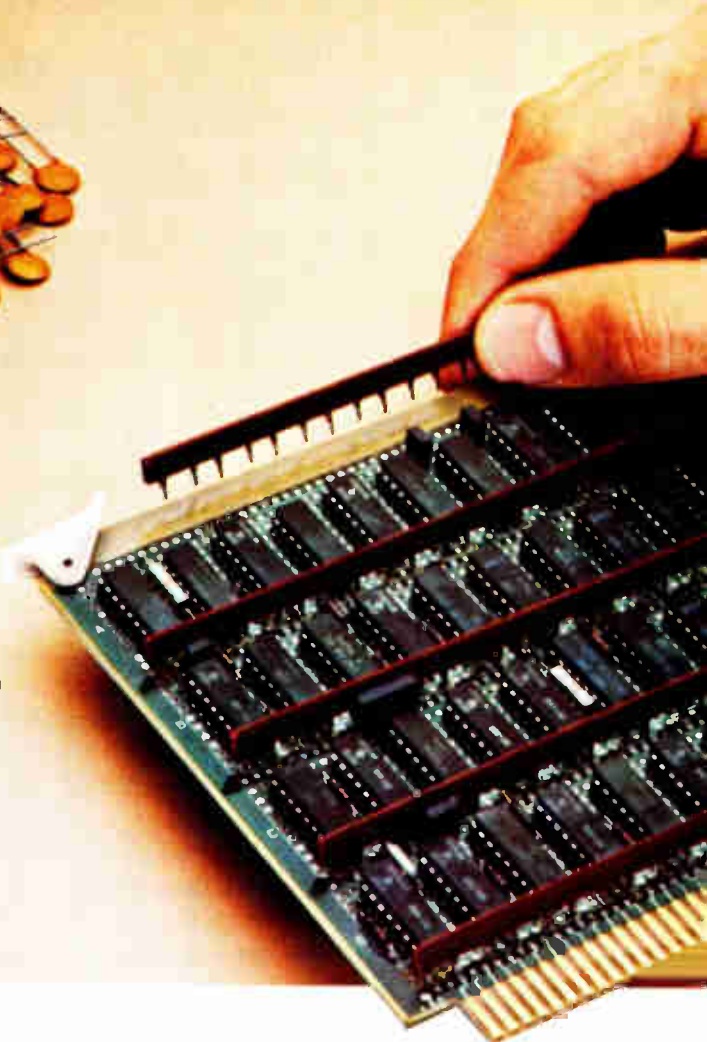


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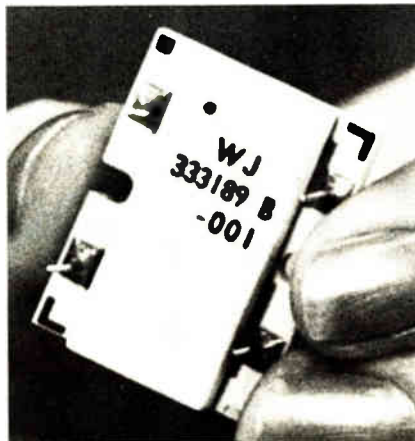
Currently available in a single-pole, single-throw, momentary-action version with a choice of solder-blade, quick-connect, or printed-circuit terminals, the switch is priced at \$2.64 each in quantities of 1,000. Delivery is from stock.

Dialight, A North American Philips Co., 203 Harrison Pl., Brooklyn, N.Y. 11237. Telephone (212) 497-7600 [345]

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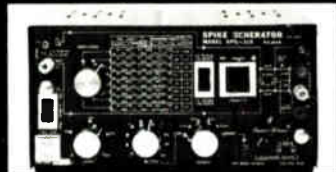
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## New products

to +100°C and can withstand non-operating temperatures as low as -65°C and as high as +125°C. Other specifications include operation to 70,000 feet of altitude, the ability to withstand 20 g of shock, and the ability to withstand 50 g of vibration at 2,000 Hz. Every module is screened to MIL-STD-883 requirements, including precapping, stabilization baking, temperature cycling, and acceleration.

Prices range from \$100 to \$77 each, depending upon the quantity ordered. Delivery is from stock to 30 days. Units that operate from 28 v dc and units housed in TO-8 packages are also available.

Watkins-Johnson Co., 440 Mt. Hermon Rd., Scotts Valley, Calif. 95066. Telephone (408) 438-2100 [346]

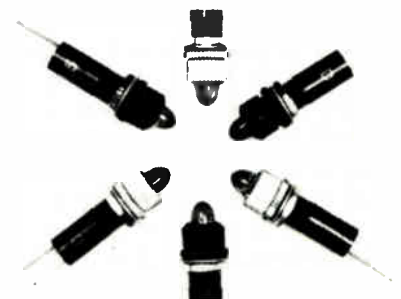
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Data Display Products, 303 N. Oak St., Inglewood, Calif. 90302. Telephone (213) 677-6166 [347]



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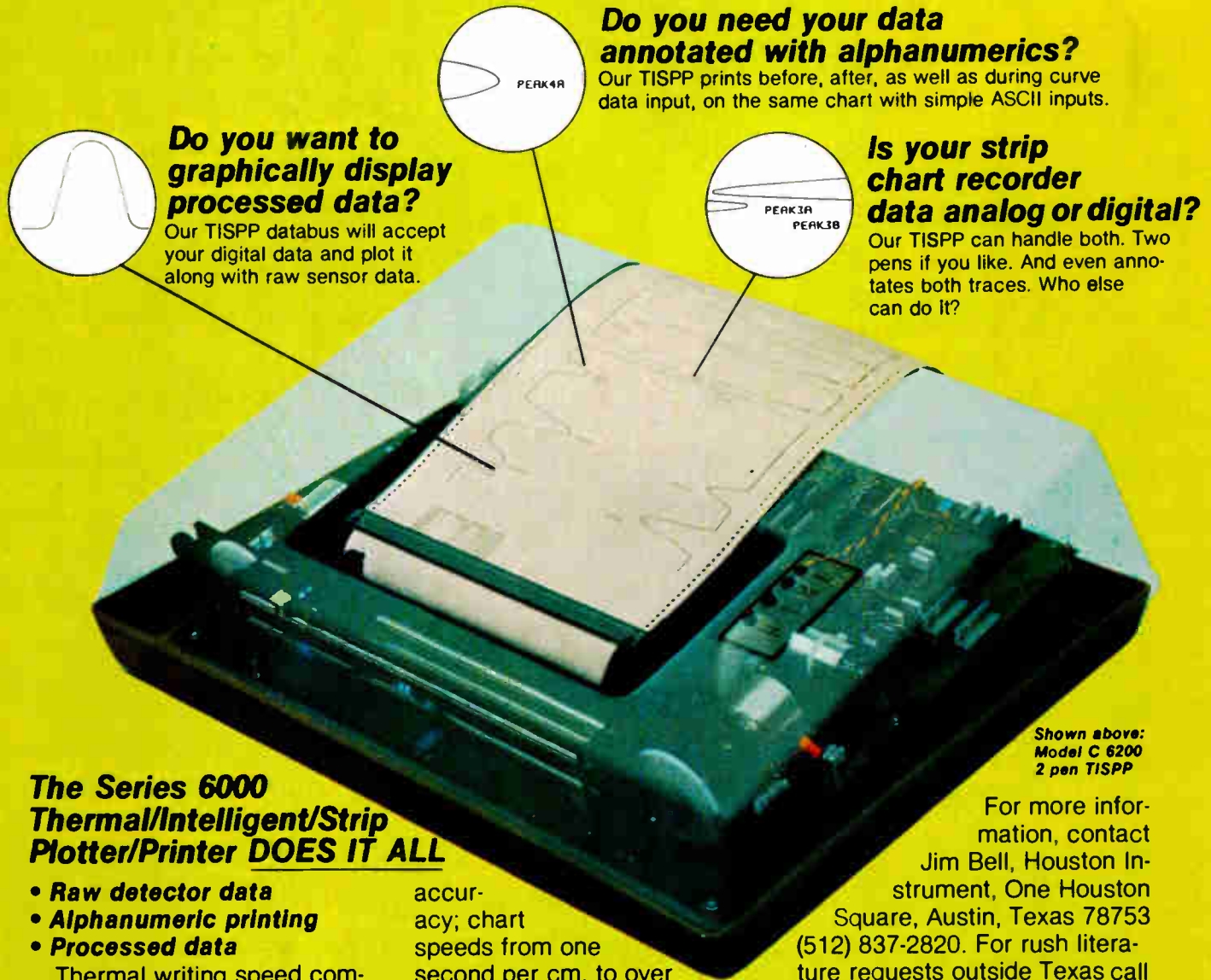
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For more information, contact Jim Bell, Houston Instrument, One Houston Square, Austin, Texas 78753 (512) 837-2820. For rush literature requests outside Texas call toll free 1-800-531-5205. In Europe contact Houston Instrument, Rochesterlaan 6, 8240 Gistel Belgium. Phone 059/277445 Telex Bausch 81399.

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### **Printers use CRT images to mix text and graphics**

Look for Hewlett-Packard Co.'s San Diego division to introduce soon the first in a family of thermal-writing raster graphics and text printers. The printers will incorporate stationary thin-film writing elements to produce permanent hard-copy records of images and text generated on a cathode-ray-tube display. **Raster-encoded data, printed at up to 12,500 dots per second, permits combined text and graphics on the same page.** A full 8.5-by-11-in. page of typical graphic images can be printed in as little as 10.5 s.

### **Cambridge Memories makes PDP-11 mass memory faster**

A mass-storage subsystem using 16-K dynamic n-MOS RAMs has just been introduced by Cambridge Memories Inc. as a direct replacement for Digital Equipment Corp.'s RK-05 disk on PDP-11 systems. **The CMI-05/1 offers a 500-ns access time and a 2.2-megabyte/s transfer rate,** compared with the 70-ms access time and 180-kilobyte transfer rate achieved by the fastest RK-05 disk. The subsystem's 1-megabyte basic memory is expandable in 256-kilobyte increments to 4.35 megabytes; the memory and its associated controller mount in a 19-in. rack. The single-quantity price for the Waltham, Mass., firm's subsystem is \$19,500 with delivery in 90 days.

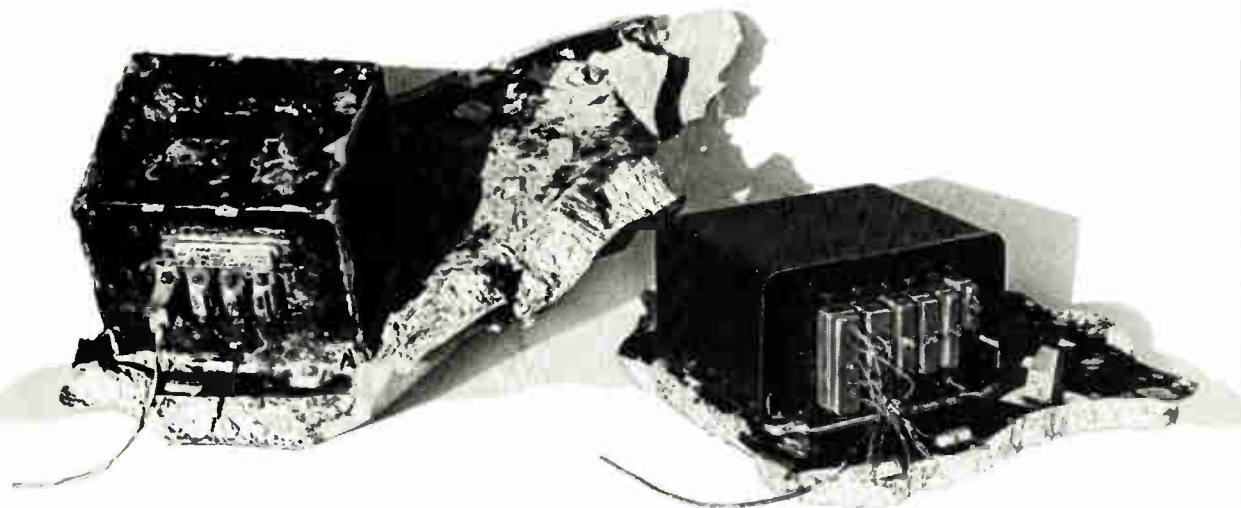
### **Users of 8089 now have assembler support software**

Intel Corp. has just unveiled an assembler support package that will make it easier for users to design in the Santa Clara, Calif. firm's new 8089 I/O processor. **An ASM-89 assembler will permit users to write programs on an Intellec microcomputer development system in the 8089's symbolic assembly language and then to translate the program quickly into machine operation codes.** LOC-86 software next appends absolute memory addresses to 8089 object modules, which are combined with the object code of 8086 and 8088 multiprocessor systems using Link-86 software. Software utility OH-86 converts the machine operation codes of the three devices into a hexadecimal format, and UPM-86 software provides additional aid for PROM programming. The entire assembler package is available on a flexible diskette for loading onto an Intellec MDS.

### **Siemens packages its 16-K RAM in plastic, and lowers the price**

A less expensive version of Siemens AG's ceramic-packaged, 16-K dynamic MOS random-access memory is now available. **Now housed in plastic, the HYB4116 has a typical access time of 200 ns—the same as for the ceramic device.** And the West German company is hinting that it has HYB4116 RAMs in the works with an access time of only 150 ns. The ceramic and plastic versions now available come in 16-pin dual in-line packages, and have a 16,384-by-1-bit memory organization. The older ceramic version sells for \$10 in 1,000-unit quantities, with delivery from stock. The newer plastic version has a price tag of \$9 in similar quantities, with a lead time of three months. Both units are available from the company's U. S. outlet in Iselin, N. J.

# THE ONE THAT GOT AWAY...



## ...ALMOST

At 23.51 on September 13th, 1977 the range safety officer at Cape Canaveral destroyed the OTS-1 launch vehicle in response to alarm signals from one of its engines.

The separated satellite continued to return normal telemetry until it slid beneath the waves off the Atlantic coast.

Over a month later, the corroded remains of the satellite were recovered, and returned to their manufacturers. The above photograph shows the Instrumentation Electronics and Squib Driver units as received back at BTM, where they were connected, unopened, to their checkout equipment and subjected to full electrical acceptance tests. They passed. 100 %.

If you think our underwater technology's good,  
you should see our flight hardware.

*Bell Telephone Manufacturing Company*

Société Anonyme

**Space Systems Department**

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Tel.: 031/37.17.17 Telex: 31226 Bella-B

Acc. IT 103-178253 E

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# LOGIC DESIGN

## Z80 • 6800 • 8080

Our **Programming for Logic Design** books describe the implementation of sequential and combinatorial logic using assembly language with an 8080, 6800 or Z80 microcomputer system. Traditional assembly language programming concepts are neither useful nor relevant to microprocessors used in digital logic applications; the use of assembly language instructions to simulate digital packages is equally wrong. These books clarify these concepts by first simulating digital logic sequences, then demonstrate more efficient solutions to illustrate proper microcomputer usage. Each book contains a complete instruction set for the microprocessor discussed. By Adam Osborne and co-authors.



### Tables of Contents:

Introduction  
 Assembly Language and Digital Logic  
 A Simple Program  
 A Programmer's Perspective  
 The Instruction Set  
 Some Commonly Used Subroutines  
 Standard Character Codes

## Order Form

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## New products/materials

A silica-based ceramic coating, Ceramacoat 512, replaces asbestos insulation as a coating for radio-frequency coils. A premixed paste, it can be brushed or sprayed onto the copper rf coil to form a hard, dense ceramic



coating resistant to oils and acids.

Ceramacoat 512 is available from stock at \$40 per quart. A thinner, 512-T, is offered at \$20 per quart for diluting the 512 paste for spray or dip coating.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562. Phone (914) 762-0685 [476]

A light-weight epoxide casting resin for embedding electronic parts, Stycast 1090, may be used over the temperature range of  $-100^{\circ}$  to  $+400^{\circ}$ F. It has low shrinkage when cured at room or elevated temperatures; a low coefficient of thermal expansion, allowing large metallic inserts to be embedded; and a low dielectric constant, which has a minimum effect on circuit operation.

The resin is also available as Stycast 1090 SI and Stycast 1090 FR. Stycast 1090 SI has better flow properties than Stycast 1090 and is reduced in specific gravity. Useful for module potting, it can produce void-free units with high component density. Stycast 1090 FR is the flame-retardant version of Stycast 1090. It follows the Underwriters Laboratories' test 94 for flame-retardant materials and may be classified as UL94 V-0. It has a yellow card listing for UL94 V-0 for 0.249 in. when cured with Catalyst 11 and 0.377 in. when cured with Catalyst 9. The FR version retains all the

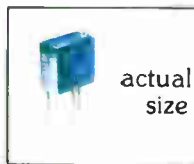


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Critical control assures you of consistent quality in every detail ... whether you buy 10 or 10,000. The 860 is just one of a plentiful crop of precision trimming



potentiometers designed for your every need. Military (RJ26) and Established Reliability (RJR26) models also available. For evaluation samples, specifications and complete pricing, write or call today.

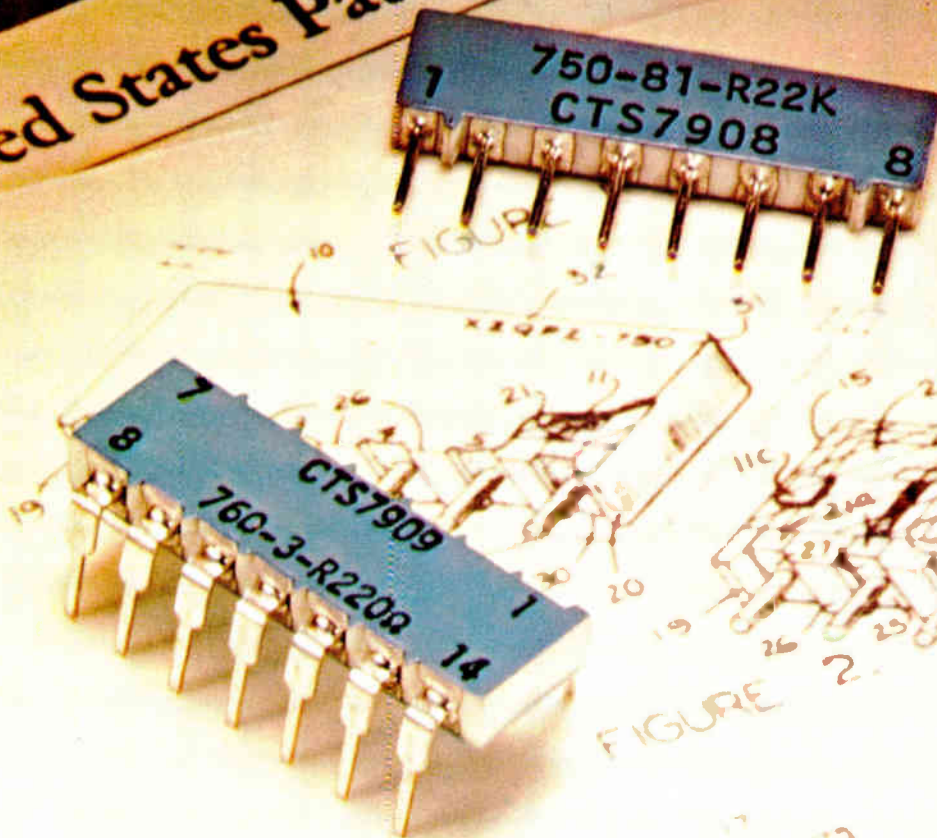
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**Schlumberger**

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TWX 510-656-2902  
Telex 83-1873

Circle 253 on reader service card

United States Patent Office



## Patent Number 3,280,378.

Termination strength is the key to network reliability —  
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are the key to strength.

The secret? Our patented process forcefully drives the leads into tapered holes in the substrate, cold forming the lead to the substrate and wedging it tightly in place prior to soldering. Try pulling out a CTS lead; you'll see how much assurance our 5 lb. pull strength gives you. Then try it with a competitive product! You'll see what we mean.

Why risk a loose termination that can alter the resistance value of your network? CTS, and only CTS, can deliver the superior mechanical and electrical reliability qualities of Anchor Lock™ terminations. The same exclusive insertion process applies to both CTS Series 750 SIP and Series 760 DIP style cermet resistor networks.

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more than one billion element hours of extended load life testing, CTS resistors have exhibited a failure rate of only 0.00041%/1,000 hours @ a 95% confidence level. Each SIP and DIP network is 100% value and tolerance tested before shipment.

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**CTS CORPORATION**  
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## New products/materials

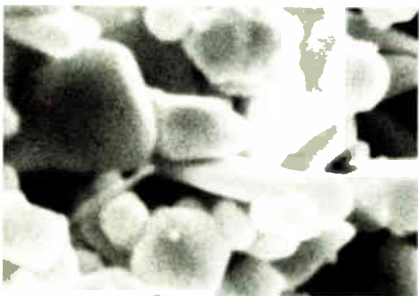
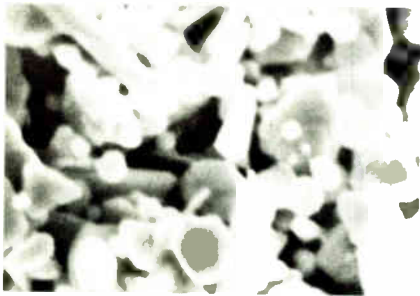


properties of the SI.

Emerson & Cuming, Dielectric Materials, Dewey and Almy Chemical Division/W. R. Grace & Co., Canton, Mass. 02021. Phone (617) 828-3300 [477]

**E-19A gold powder**, for use in conductive inks for thick-film multi-layer circuits on high-purity alumina and other substrates, has high electrical conductivity, excellent paste-making qualities, good wettability, ease of dispersion, and the ability to carry a high metal content. Seventy-five percent of the brownish powder consists of spherical particles 1  $\mu\text{m}$  in diameter; the remainder consists of flakes from 2 to 5  $\mu\text{m}$  long. The material's ignition weight loss at 110°C is 0.05% maximum, and its soluble chloride residue does not exceed 0.005%. The normal surface-area yield is from 0.4 to 0.7  $\text{m}^2/\text{g}$ , but can be held at a range of 0.5 to 0.6  $\text{m}^2/\text{g}$ .

General Telephone & Electronics, Wesgo Division, 477 Harbor Blvd., Belmont, Calif. 94002 [478]



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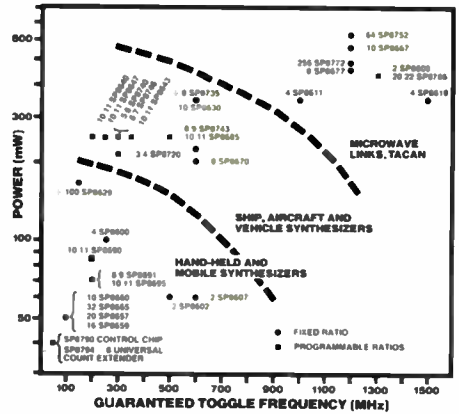
Our prescalers feature VHF and UHF input ports, TTL/MOS-compatibility, and are all guaranteed to operate from dc to at least the frequencies shown.

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and hassle, so contact us for details and a demonstration today.

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**ITT North**  
Microsystems Division



## New literature

**Amplifiers.** "LogiMetrics" describes traveling-wave-tube amplifiers and systems as well as signal generators and systems. Included in the traveling-wave-tube amplifier section are specifications and drawings on each low-power, high-power, dually redundant, and pulsed-microwave TWT amplifier. The signal generator sec-



tion specifies a variety of models such as Two-Tone rf, fm-a-m, rf, a-m, Signallock rf and CB Test Set. Also included in the 48-page catalog is a section on LogiMetrics systems and subsystems capabilities. LogiMetrics Inc., 121-03 Dupont St., Plainview, N. Y. 11803. Circle reader service number 421.

**Fluxes.** "An Alpha Flux For Every Soldering Application" describes rosin and water-soluble fluxes. Rosin fluxes are subdivided into nonactivated (type R), mildly activated (type RMA), fully activated (type RA), and superactivated (type RSA). Water-soluble fluxes are subdivided into organic-acid (type OA) and inorganic-acid (type IA). The four-page brochure features a flux-selection guide that tabulates each flux and indicates specifically the applications for which the flux was formulated. A copy of the handbook may be obtained from Alpha Metals, Inc., 600 Route 440, Jersey City, N. J. 07304 [423]

**Photodetectors.** "Centronic Silicon Photodetectors" reviews the physical and electrical properties of silicon

# Radio Active

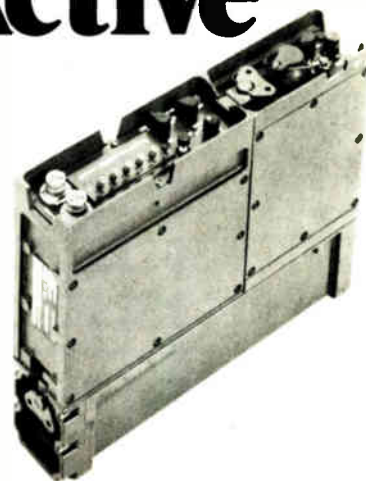
In radio-communications, Plessey offers the most comprehensive line of IC's available.

IC's that will cut the costs, reduce the size and increase the reliability of your designs for everything from commercial CB sets to manpack radios like the Hughes PRC-104 shown.

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Our SL 6640 (with audio output) and SL6650 (without audio) are similar, but go a bit further, adding dc volume control to the on-chip preamp, amp, detector and carrier squelch.

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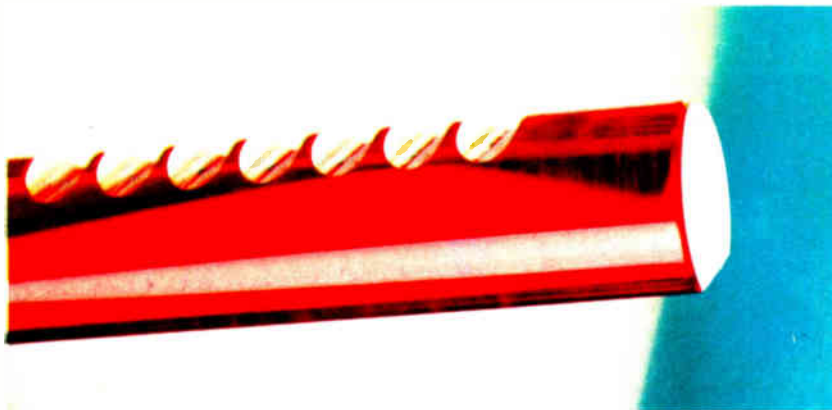
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Wire-guide bars for printing heads

All kinds of material have been tried out for the manufacture of wire-guide bars. The corundum in single crystal structure ( $Al^2 O^3$ ) still remains the best one. Seitz knows it and uses it in an economic and intelligent way.

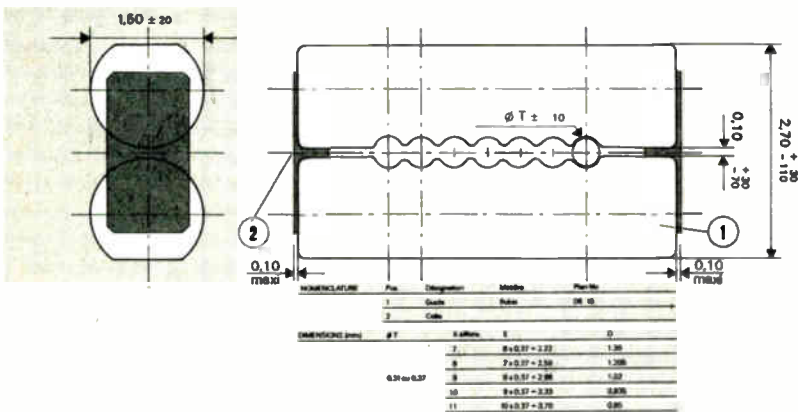
The form: a cylindrical bar, which means reduction of friction, improvement of the ribbon guiding, elimination of the wear of the head. Application: in every type of head, thanks to the rigorously respected dimensions and tolerances.

Seitz is the pioneer of wire-guides and is furthermore the most important manufacturer of this product. Seitz has created and fixed its norms.

Seitz wire-guide bars: A technical and economic solution.

Seitz wire-guide bars:

A technical and economic solution.



## New literature

photodetectors, providing basic information on their structure, response, sensitivity limits, temperature effects, and equivalent operating circuits. Graphs, charts, tables, and circuit diagrams are also provided in the 20-page catalog, along with dimensional packaging drawings on optoelectronic detectors that include standard and special single elements; multielement quadrants, arrays, and matrixes; small- and large-area photovoltaics; hybrids; temperature-monitoring devices; and fiberoptic transmitters and receiver modules. Centronic, 1101 Bristol Rd., Mountainside, N. J. 07092 [422]

**Instruments.** "1979 CSC" features signal generators, electronic test instruments, logic probes, frequency counters, solderless breadboards, digital troubleshooting instruments, and integrated-circuit test clips. The 32-page catalog describes a group of products such as the Probe Case, the Handheld Case, the Portable Case and the Benchtop Case, not to



mention the Experimenter System, which provides pre-etched, predrilled printed-circuit boards, and pre-printed worksheet pads as complements to CSC's popular Experimenter solderless breadboards. Copies of the catalog may be obtained from Continental Specialties Corp., 70 Fulton Terrace, New Haven, Conn. 06509 [424]

**Switches.** Featured in the 1979 edition of the "Alcoswitch Catalog"

# Power Play

A.C. power control is almost child's play with any one of a series of zero-voltage switches from Plessey.

They all provide better, more economical control for your hair-dryers and heaters, freezers and furnaces, pools and percolators, or whatever else you may be working on.

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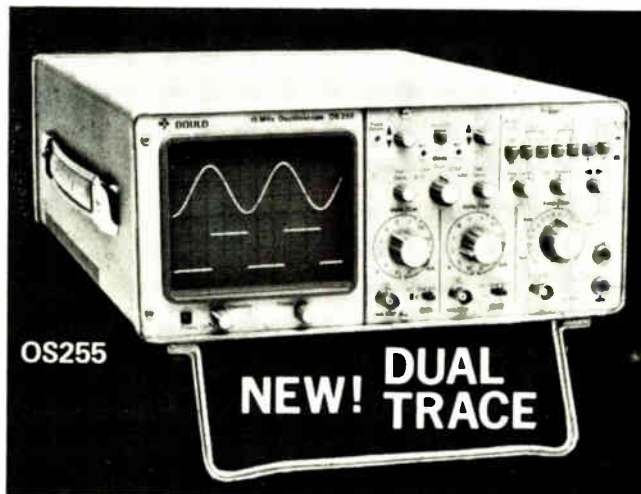


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100 pcs. of each size complete with cabinet  
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With thread sizes of 4-40, 6-32 and 8-32.  
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**1/4" HEX Male/Female Standoffs Brass Nickel Plated**  
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- High-speed APU
- 11,4MB Winchester hard disk drive (max. 45.6MB)
- 350KB minifloppy disk drive (back-up)
- Extended BASIC

\*\* Our low-cost, easy-to-operate

● **SORD Word Processor** available as an option

#### Software Options

- BASIC Compiler (APU Version)
- FORTRAN IV
- COBOL
- Multi-user BASIC (available soon)

#### Bench mark test

B. No.	M200 mark II		M200 mark II + APU		M200 mark VI	
	Interpreter	Compiler	Interpreter	Compiler	Interpreter	Compiler
1	2.8 SEC	2.3 SEC	1.2 SEC	0.9 SEC	0.86 SEC	0.71 SEC
2	11.4	2.1	7.7	0.9	5.45	0.72
3	25.5	8.6	16.6	1.9	11.6	1.45
4	25.0	8.9	16.4	1.9	11.6	1.54
5	26.7	9.0	17.2	2.0	12.2	1.55
6	42.4	20.1	27.4	7.0	19.3	5.2
7	65.0	23.0	49.4	11.0	34.5	7.9

users area 29KB      users area 32KB



Model M223 mark VI

Interested distributors and OEM's please contact our office.

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Telex: 220104 (LDRESOL F)

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Telex: 30245 (MELMM AA)

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Telex: 58799 (CPTX CH)

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## New literature

are devices that can be mounted on printed-circuit boards, including miniature and subminiature toggle and slide types, push buttons, and rotary switches. The 159-page catalog discusses the TT series, which provides a choice of custom switches, such as lighted versions in subminiature form, employing the standard 0.1-in. mounting centers throughout. Also listed is a variety of lamps, light-emitting diodes, panel indicators, and three families of control knobs. Alco Electronic Products Inc., 1551 Osgood St., North Andover, Mass. 01845 [425]

**Camera tubes.** The six-page application note, "SIT and SEC Camera Tubes," discusses the characteristics and differences of Silicon Intensified Target and Secondary Electron Conduction camera tubes and helps the designer select the correct camera type for a particular application. The basic structures of the two camera tubes are diagrammed and their properties are explained and compared. Technical note 10 is available from Qantex Corp., 252 N. Wolfe Rd., Sunnyvale, Calif. 94086 [426]

**Microcomputer analysis.** "Microcomputer Analysis" is the subject of a report indicating that the major growth in microprocessor sales in the next few years will probably be in the area of 16-bit microprocessors. The beginning of the report discusses the advantages of wider words in memory and processor registers and the fact that wider words are easier to manipulate. Sometimes, however, fewer wider words will fit in data storage. The report provides a diagram of the empirical ranking of 16-bit microprocessors and illustrates the relationships of the various processors to one another. The report concludes by examining and comparing six of the major 16-bit devices—Motorola's MC68000, Zilog's Z8000, Intel's 18086, Western Digital's WD9000, Texas Instruments' 9900, and National's INS8900. Mackintosh Publications Ltd., Mackintosh House, Napier Road, Luton LU1 1RG, England [427]

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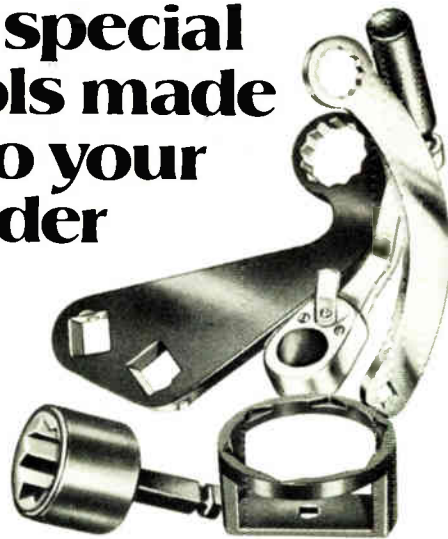
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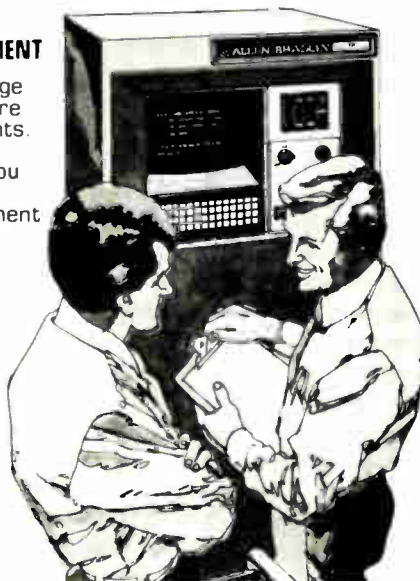
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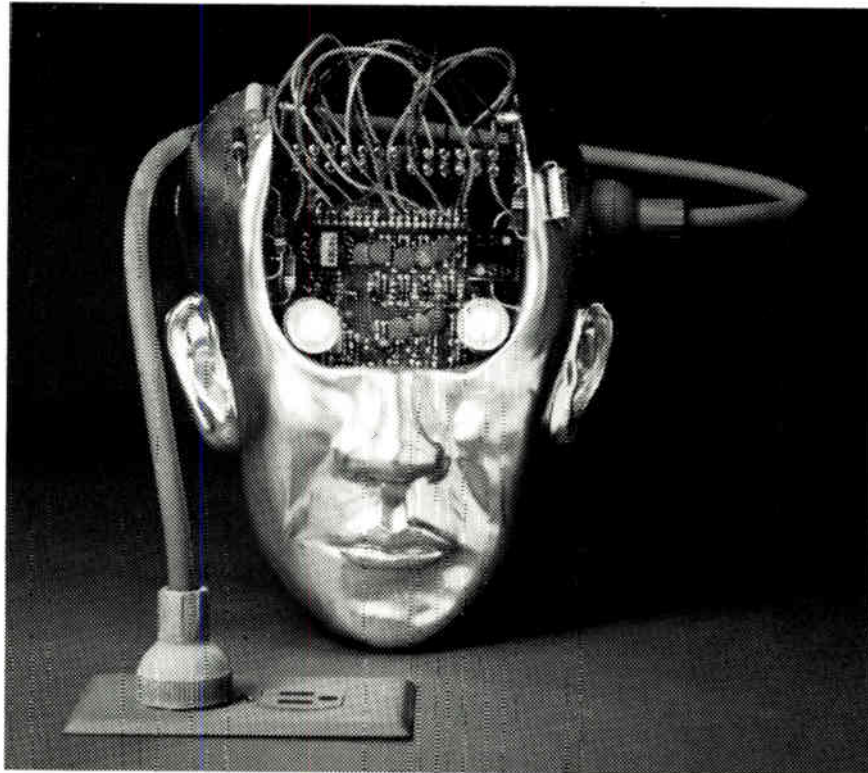
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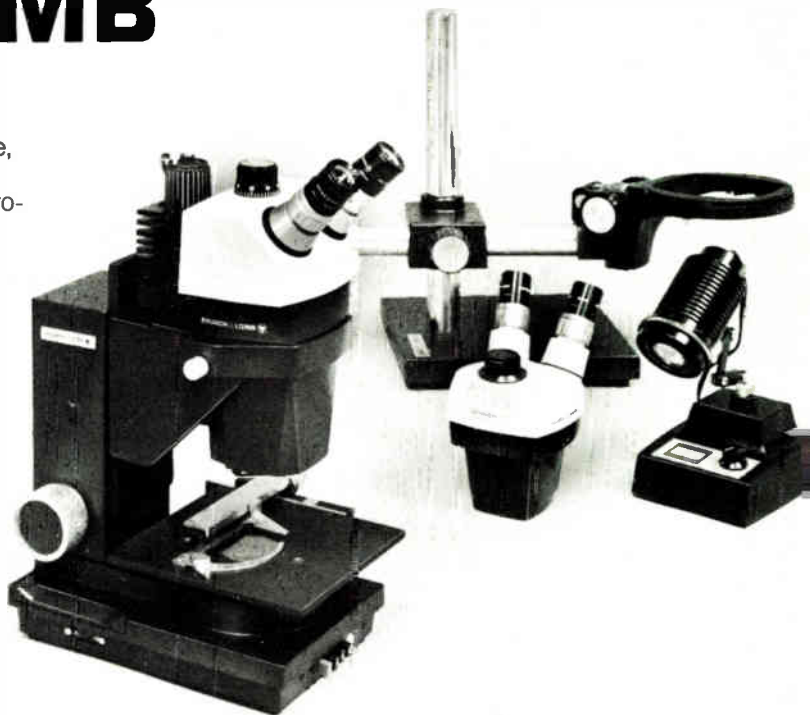
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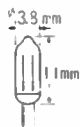
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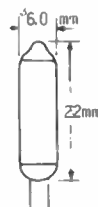
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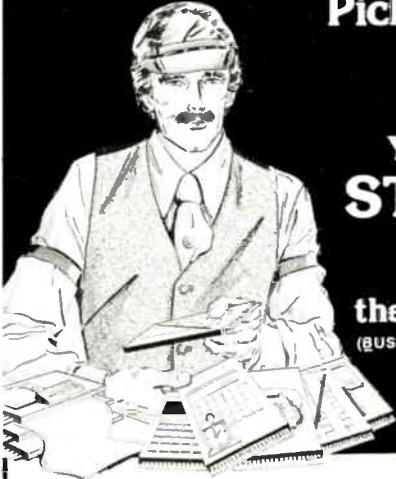
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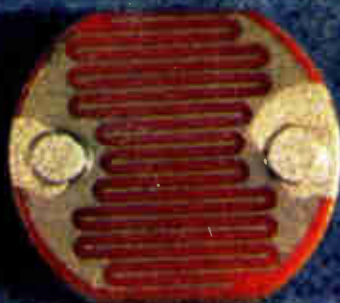


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