

SEPTEMBER 13, 1979

WORLD POWERS SLICE UP THE ELECTROMAGNETIC SPECTRUM/87

Sampled-data technique cuts size of a-d converter chip/134

Logic analyzer or development system: which is right for the job?/141



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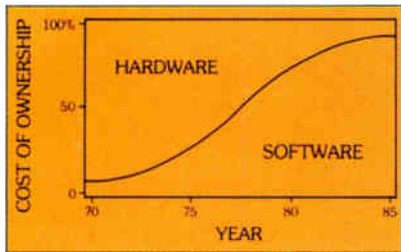
LOOKING OVER THE NEW LSI PROCESSES



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SOFTWARE: THE HIDDEN CONSIDERATION IN SELECTING AN AUTOMATIC BOARD TEST SYSTEM.

The hardware of an automatic PC board test system is tangible. It can be seen, touched, and specified. However, software is much more difficult to evaluate. Yet, as the diagram below shows, software costs can be a large percentage of the total cost of ownership. For this reason, software is one of the most important considerations in selecting a board test system.



Three important criteria.

The three factors that have the greatest impact on software costs are: ease of programming, ease of debugging, and expansion capability.

Program generation is a large part of your software investment. But high-level languages and automatic program generation packages can save time and minimize the need for skilled programming personnel.

Program debugging and changes necessitated by engineering change-orders can also require large software revisions. But advanced debugging techniques can minimize that investment.

Finally, system expansion could require significant software revisions unless there is provision to add programmable instruments without major software changes.

Programming and debugging by nonprogrammers.

Hewlett-Packard's approach to software in the HP 3060A Board Test System (\$78,000* for standard operating system) enables non-programmers to quickly generate and edit test programs.

For example, with in-circuit testing, you simply assign node numbers to all nodes on the schematic. Using the schematic, plus a parts list with values and tolerances, the board topology can then be entered into the 3060A by a nontechnical person.

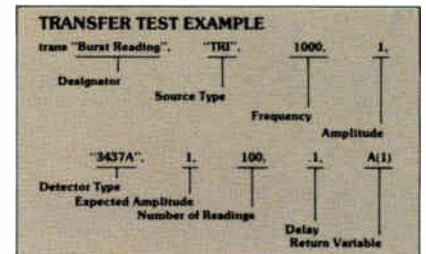
From that point, the 3060A's automatic In-circuit Program Generator (IPG) takes over. It selects appropriate guarding and measuring techniques; analyzes measurement errors and adjusts tolerance specs if necessary, and generates a complete program in HP's Board Test Language (BTL) as shown below. It also calculates an estimated run time and even produces a map to aid in fixturing.

Functional testing is also simplified. HP's BTL provides high-level language

```

01: "LEAVE FIRST THREE LINES"
11: Jmp 2
21: sto "START"
31: "SBUS" :scan.0201
41: "IBUS" :scan.0302
51: "ABUS" :scan.0405
61: "GBUS" :scan.0503
71: "BBUS" :scan.0606
81: "LBUS" :scan.0704
91: "START" :dsp "Install board; press continue"
101: pass :if on
111: ncon4.0302;5.0403
121: scone "B" 1 nodes 4 5
131: ncon3.0202;6.0503;2.0004
141: scone "nen" 1 nodes 3 6 2;250;120
151: ncon1.0002;5.0403
161: wurd2.0105;2.0007;1.0304;5.0006
171: ncone "C" 1 nodes 1 5;4.3e-4;20;20;
181: ncon1.0002;2.0103
191: wurd5.0205
201: ncone "C" 2 nodes 1 2;1e-4;20;20;"esen"
211: ncon5.0402;2.0103
221: ncone "R" 1 nodes 5 2;2.7e1;5;5;"ss"
231: ncon9.0002;1.0003
241: ncone "L" 1 nodes 9 1;2.2e-4;5;5;"edss"
251: ncon1.0002;6.0503
261: scone "Z" 1 nodes 1 6;8.93;0.00
271: faoff 1;f r;120;pass
281: sto "START"
+14002
    
```

statements (as shown below) that are used to set up stimulus and response instruments for analog, digital, or combined testing. A technician or test engineer familiar with the board and its test requirements can easily master BTL and develop the functional test program.



Program debugging and editing to optimize testing is speeded by the 3060A controller's typewriter-style keyboard and dedicated editing keys. It's a simple matter to call up a specific program line, revise appropriate portions, and store the corrected line.

When you expand.

Expansion of your board test system is almost certain, and addition of programmable instruments shouldn't require another major software investment.

With the 3060A, expansion capability is built in through the HP-IB.** That means you can add measurement capability yourself—without factory modification or special software.

For additional information.

There are other benefits to PC board testing with the HP 3060A. To get complete details, send for our HP 3060A data sheet or contact your local HP field engineer.

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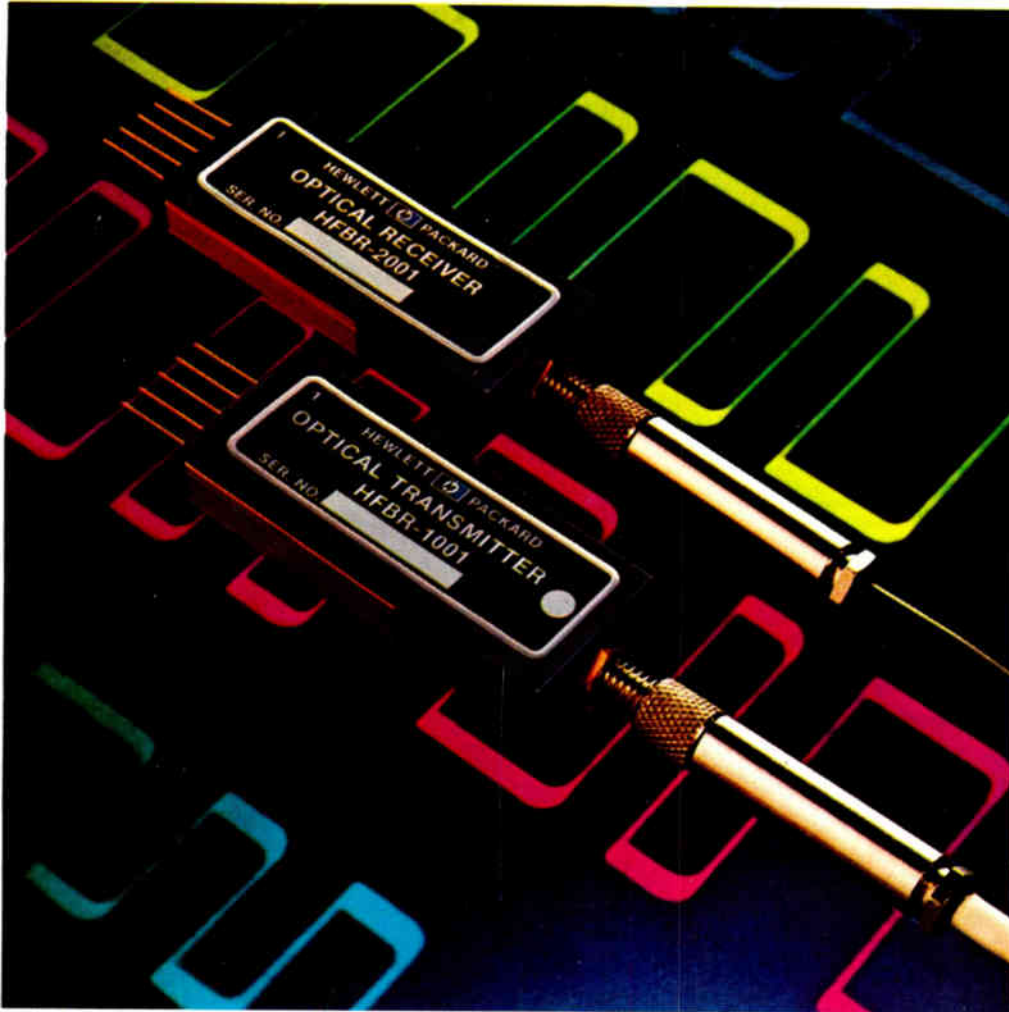
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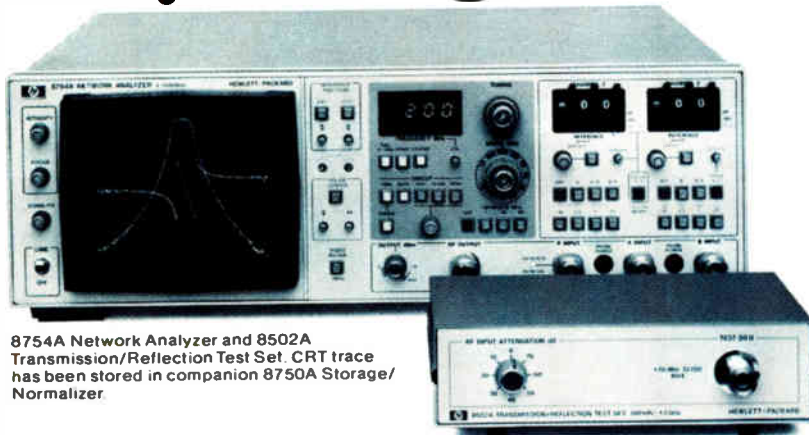
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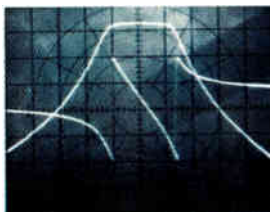
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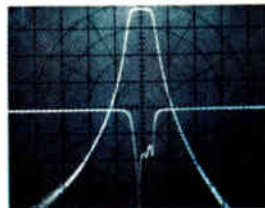
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Highlights

Cover: Blink and the LSI scene changes, 109

Random-access memory fabricated in new MOS processes rivals bipolar speed; bipolar counters by boosting density and cutting power consumption. Meanwhile, other new processes promise glittering performance.

Cover photograph is by Don Carroll. Background circuitry is courtesy of Bell Laboratories.

Wind turbines interfere with TV signals, 96

The growing interest in wind-generated power may be blunted somewhat by the turbine blades' effect on television reception. Researchers are studying methods for minimizing signal-scattering problems.

Sampled-data a-d converter is smaller, 134

An 8-bit monolithic analog-to-digital converter using a charge-balancing converter achieves low-cost microprocessor-compatible performance on a reasonably sized chip.

Development systems confront analyzers, 141

Confusion has arisen over the application areas of logic analyzers and microprocessor development systems, now that the latter can also do some real-time analysis. But a careful look at the different stages of system development reveals which should be used when.

. . . and in the next issue

A new LSI memory process . . . the problems of convenient low-level measurement . . . new techniques for making interconnections.

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In the fast-changing world of electronics technology, few things change as rapidly as semiconductor processes. That's why we run frequent assessments of progress—like Solid State Editor Ray Capece's look at the new LSI processes (p. 109). Incidentally, that's Ray looking them over, on the cover.

What we are seeing, says Ray, are advances in the familiar MOS and bipolar processes that will mean another new generation of devices to appear early next year. "There's a lot of work in progress that will really improve performance for all the conventional processes," he predicts.

Such progress warrants a closer look, and the two articles following Ray's special report provide just that kind of detailed examination. Moreover, there will be similar articles in forthcoming issues.

The progress in the processes means that the parts produced are getting closer and closer together in terms of lower costs, higher densities, increased speed, and reduced power, Ray argues. "But there are going to have to be some basic changes as all processes get to the same level of performance."

A notable example, he says, is the relationship between logic levels and switching speeds. All the conventional processes, MOS and bipolar, have gotten along well using the 0- and 5-volt logic levels established in the early days of small-scale TTL packages. "But when all the processes get to the 20-nanosecond memory speed, we're going to have to go to a lower logic level. The swing between 0 and 5 V is too great to send around the circuit in that brief switching time."

"It's entirely possible that we'll see the TTL levels chopped to 0 and 2 V," he continues. Another possibility is a move to the logic levels found in the one technology that's already below 20-ns switching speeds: emitter-coupled logic.

Unfortunately, there is no single set of ECL levels as with TTL-compatible logic. So before ECL-compatible voltages flourish, there will have to be an agreed-upon logic swing: in a word, standardization, maintains Ray.

On the masthead to the left there is an important change. Sam Weber, executive editor and long-time head technical maven, has become editor in chief, replacing Kemp Anderson, who has been promoted. Sam's career with *Electronics* goes back a good number of years, and he has had a major hand in shaping the magazine.

Kemp, whose association here has also been long and distinguished, has been tapped by parent McGraw-Hill Publications Co., the magazine operation of McGraw-Hill Inc. He is filling a new position, that of vice president for business-systems development. A major responsibility will be increasing the company's capability in data processing and telecommunications. Of course, a number of the technologies involved come right from his former bailiwick.



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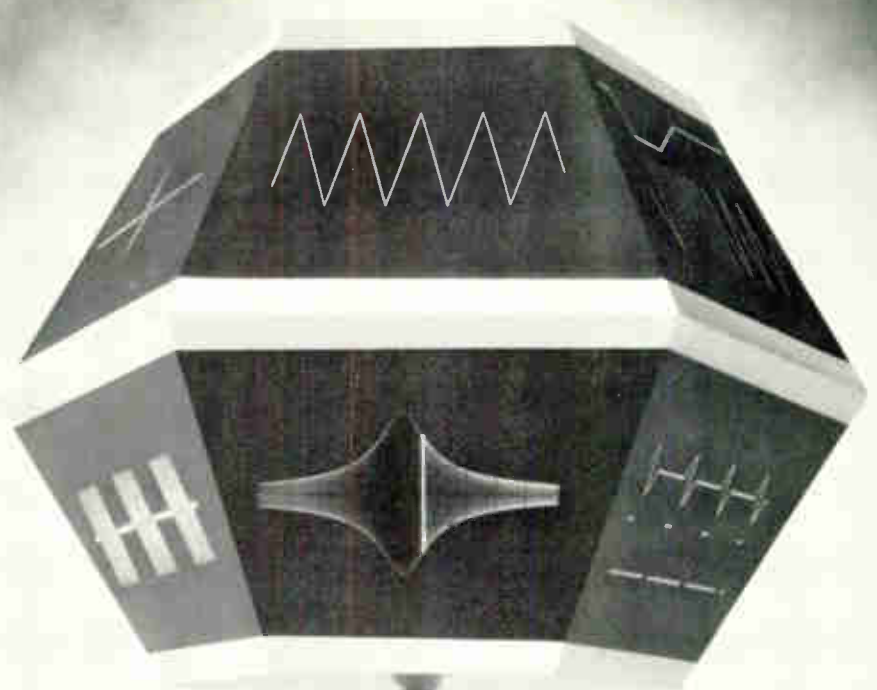
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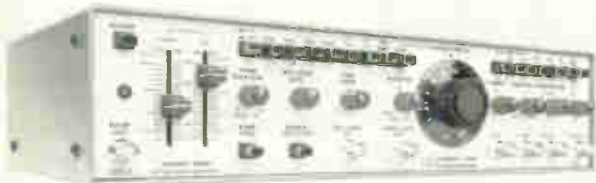
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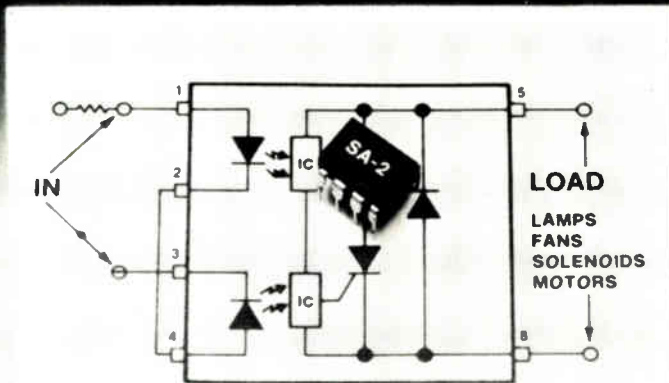
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Readers' comments

Assigning first place

To the Editor: In "In the beginning" in the May 24 issue [p. 112], part of your special report on computer architecture, it was stated that the first electronic digital computer was built in 1946 in the United States. That is incorrect, though a popularly held notion.

"The COLOSSUS" by Brian Randell, published by the University of Newcastle upon Tyne, England, in 1976 (Technical Report Series, no. 90), shows the date to be 1943, for the purpose of code breaking. This I know also through personal research done at King's College, Cambridge University, England, on the papers of Alan Turing, to whom, after all, we owe so much.

Paul Pangaro
New York, N. Y.

Not with silicon

To the Editor: In your interesting article "A burst of energy in photovoltaics" [July 19, p. 105], you report that "electrochemical cells with single-crystal-silicon electrodes immersed in an electrolyte have already demonstrated conversion efficiencies of 8% to 10%". Neither 8%-to-10%-efficient silicon-based electrochemical cells nor stable silicon photoelectrodes have been reported. Bell Labs has, however, reported 9%- and 12%-efficient electrochemical solar cells with single-crystal gallium arsenide.

Adam Heller
Electronic Materials Applications
Research Department
Bell Laboratories
Murray Hill, N. J.

It can be done

To the Editor: It was a pleasure to see, according to Tektronix' John Addis on page 131 of your June 21 issue, that the "conventional" oscilloscope has caught up with the sampling oscilloscope, after only about 18 years. But before he claimed you cannot have a single-transient sampling oscilloscope, he should have read my old Tektronix paper, presented on April 16, 1963 at Cecon, "Storage to Picosecond—A Survey of the Art." This paper



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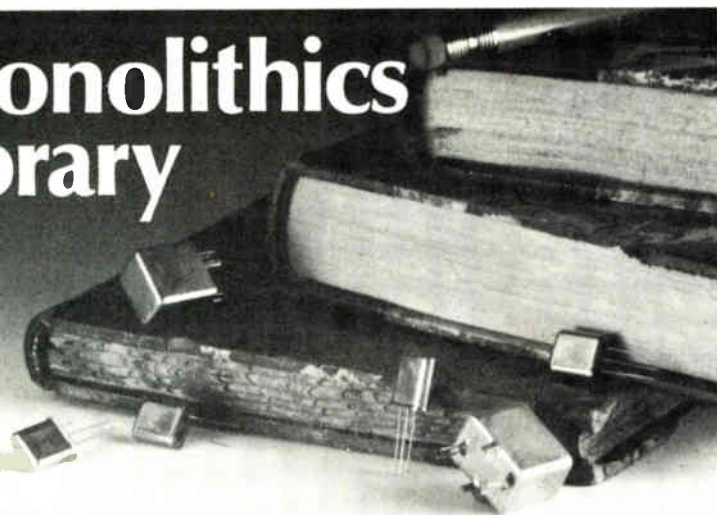


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Readers' comments

points out that in a sampling oscilloscope, you sample a signal in “time space.” This means you can sample a signal at one point in space many times (by repeating a signal, either with successive signals produced by a recirculating delay line or by literally generating new signals in succession) or one time at many points in space (for example, taps on a delay line).

I guess Tek is so big now the conventional scope designers don't get to talk to the sampling boys, as in the old days, when I did the N unit and Cliff Moulton did the 519, a mere 20 years ago!

C. N. Winningstad
Portland, Ore.

Multiplexing has been around

To the Editor: In “Transparent memory ends conflicts over CRT control” [July 5, p. 136], Messrs. Trotter and Matic are to be commended for their good overview. Direct random-access cathode-ray-tube display is growing in popularity due to its inherent advantages in many applications.

The “clever multiplexing technique”—to avoid central-processing-unit contention problems such as streaking—alluded to the article, however, has been in common use in Viuram display drivers manufactured by Computer Technology for nearly three years. The new generation of large-scale integrated CRT controller chips, notably the Motorola MC8645, have also employed variations of this scheme with a high degree of success, resulting in high-quality displays which operate at full mainframe speeds.

Thomas H. Birchell
Oakland, Calif.

Correction

In “Current source for I^2L saves energy” (Aug. 16, p. 115), pin 13 of A_1 should connect to pins 5, 6, and 12 only and not to the other pins as shown. Also, the expression for I_{out} in the text should agree with the correct equation shown in the schematic.

Electronics/September 13, 1979

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People

There's room for all,
says RCA Labs' Kressel

For Henry Kressel, variety is more than the spice of life; it is the leaven in the expansion of the semiconductor industries. There will always be a diversity of processes and a diversity of devices, predicts the recently appointed staff vice president for solid-state technology at RCA Laboratories.

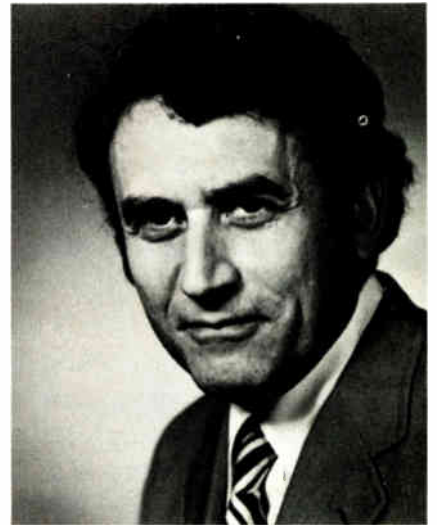
"It would be a foolish misstatement to say that you have one technology that is good for everything," he argues. "One way to look at it is: you choose your technology for your applications."

Kressel was talking about the place of the RCA-developed silicon-on-sapphire technology, a complementary-MOS large-scale integration process in what is increasingly an n-channel MOS world. Other technologies like SOS can flourish in market segments that need their advantages, he maintains.

These advantages of low power dissipation, density, and radiation hardness will often offset the premium price necessitated by the higher price of the substrate. Moreover, RCA is hard at work increasing yields by "doing all the things you do with LSI," such as improving the quality of the epitaxial layer.

Another tack is to reduce the substrate cost through the lab-developed ribbon-growth process for the substrate, which avoids the waste inherent in sawing ingots into wafers. The molten sapphire is pulled from the melt through a die, and the resulting ribbon is the right thickness and need only be snipped into wafers.

Both processes and devices occupy the attention of Kressel's 95 researchers at the Princeton, N. J., labs. As well as SOS, solar cell and laser work, they are developing new charge-coupled-device structures, looking at radiation hardness, and modeling new devices. Their work overlaps that of the 210 researchers at Kressel's other major responsibility: the solid state technology center at Somerville, N. J. It develops



Speaking up for SOS. Henry Kressel is new vice president for solid state at RCA Labs.

custom circuitry and does pilot production for the Solid State division, the Government Systems division, and other RCA operations.

The new vice president was born in Vienna 45 years ago and was educated in the U. S., receiving both a master's degree in business administration and a Ph. D. in metallurgy and materials science from the University of Pennsylvania. He has been with RCA since 1959, most recently as director of the materials and processing research lab.

GM's Jaumot wants better semiconductor reliability

If, despite Bob Dylan's assurance of a decade ago, you still doubt that the times they are a-changin', look at General Motors Corp.'s Delco Electronics division for further proof that they are indeed. For not only has GM combined the division's automotive, aviation, and military engineering groups, but it also has recognized the ascendancy of auto electronics over what used to be the glamour groups by promoting a longtime automotive hand to director of advanced engineering for the combined operation.

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| MKB4027-83 | 4K X 1 | -55° to 85°C | 200ns | 467mW | 40mW |
| MKB4027-84 | 4K X 1 | -55° to 85°C | 250ns | 467mW | 40mW |
| STATIC RAMS* | | | | | |
| MKB4104-85 | 4K X 1 | -55° to 125°C | 300ns | 150mW | 53mW |
| MKB4104-86 | 4K X 1 | -55° to 125°C | 350ns | 150mW | 53mW |
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| MKB34000-84 | 2K X 8 | -55° to 125°C | 450ns | 550mW | NA |
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| MKB2716-77 | 2K X 8 | -40° to 85°C | 390ns | 633mW | 165mW |
| MKB2716-78 | 2K X 8 | -40° to 85°C | 450ns | 633mW | 165mW |
| MKB2716-82 | 2K X 8 | -40° to 85°C | 650ns | 633mW | 165mW |
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| MKB3881-20 | PIO | -55° to 125°C | 2.5 MHz | 788mW | NA |
| MKB3882-20 | CTC | -55° to 125°C | 2.5 MHz | 1050mW | NA |

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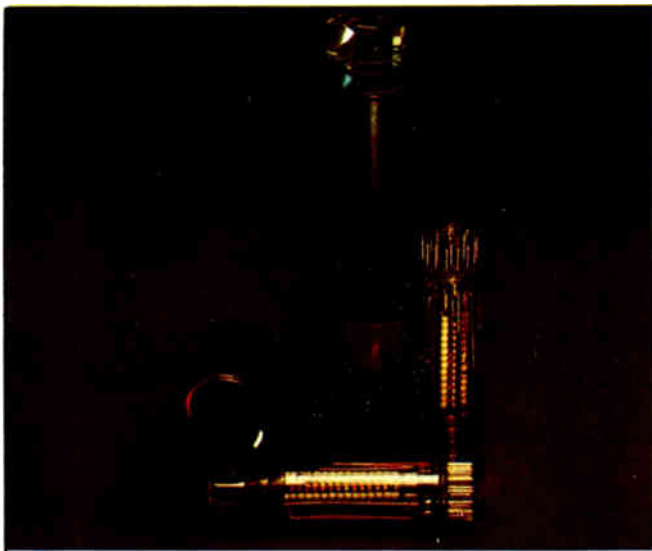
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People



New organization. GM has placed electronics operations under Frank E. Jaumot Jr.

has a staff of about 1,425 persons designing electronic components, military and commercial navigation systems, and advanced automotive concepts such as an electric vehicle.

Combining the three operations and placing Jaumot in charge of engineering makes sense. With Jaumot's engine-control engineering staff becoming a manufacturing operation—it will turn out 25,000 engine-control computers daily for 1981 cars—the crunch of fitting the Motorola 6800 microprocessor-based systems to each GM car and engine required the expertise of aviation staffers in Santa Monica, Calif., and of military designers in Milwaukee. "Their contributions were critical," says Jaumot.

The reorganization is aimed at meeting future needs, Jaumot explains, as the technical requirements for automotive electronic systems move closer to the level of those used in commercial aviation and military equipment. "We needed to better integrate the advanced technology area," he says.

Tackling complex control problems is only part of Jaumot's job, because the Delco division also will be manufacturing 20 million to 30 million integrated circuits annually. Jaumot says that improving the reliability of semiconductors is high on his list of priorities. For example, work is under way to reduce contamination and improve bond strength and oxide integrity. "We're asking for a lot," he concedes.



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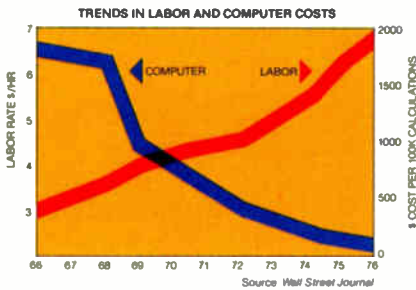
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The outcome was actually two models. The HP 2621A, which sells for \$1450. And the HP 2621P, which has a built-in printer, costs \$2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

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Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and

able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.



Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard. And the 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

- I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
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- I'd like to know more about HP's complete family of terminals.

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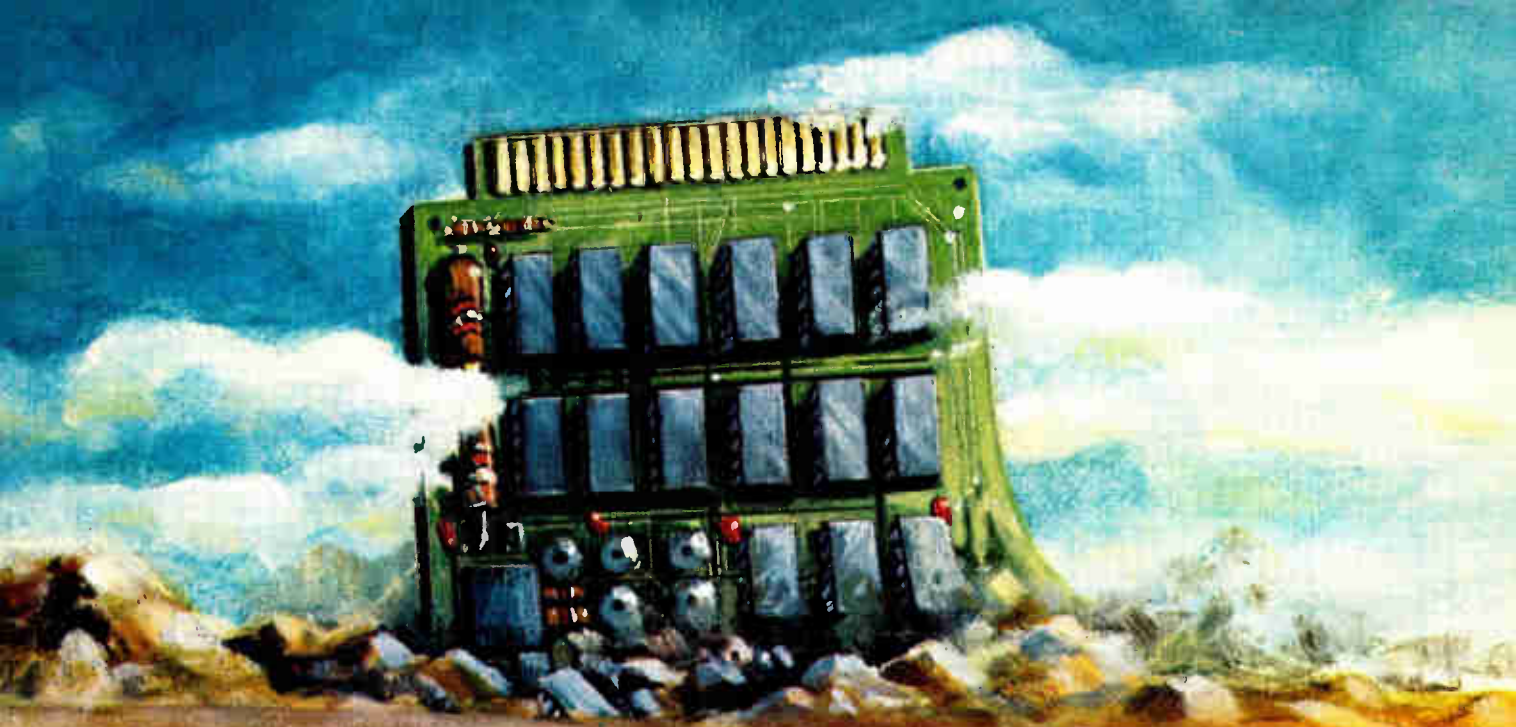
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Circle 21 on reader service card



**If you
can't bring
the board
to the test...**



... bring the test to the board in the field with the Testline AFIT 1000. And exercise your digital printed circuit board more completely and more economically than with any other portable tester.

You can test ten ICs per minute, confirming commands and test results through visual and audible indicators. And you can test all TTL families, DTL, CMOS, CTL and other saturated logic with TTL compatible I/O. Data storage in the AFIT 1000 is handled by a mini-cassette tape cartridge with a keyboard for data and command entry and with a powerful microprocessor in control.

You can use this same test capability when you bring your boards to the test in repair depots and in PCB production. Our AFIT 1500, 3000A and 4000 test systems provide complete compatibility of test software and test results.

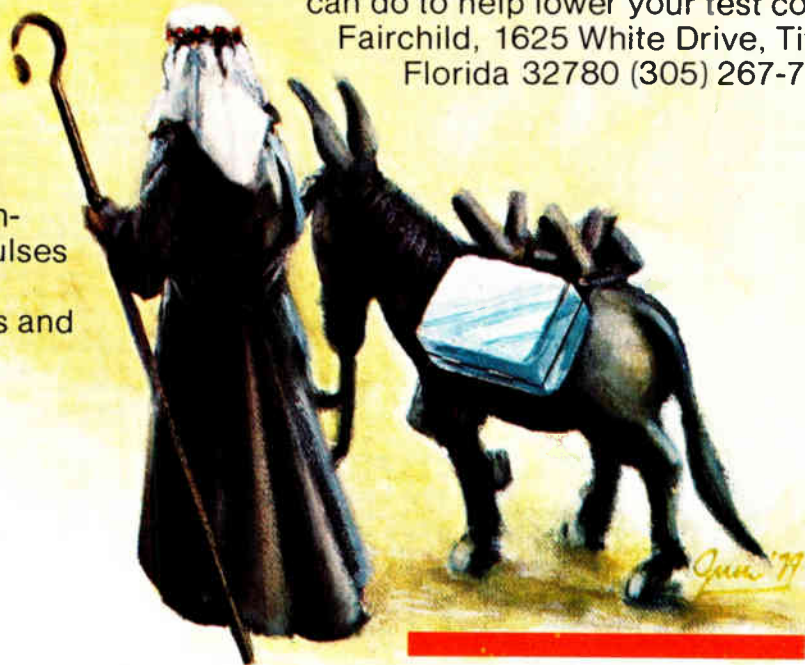
All AFIT systems use identical pin driver electronics to functionally exercise logic. And the 1500, 3000A and 4000 systems extend testing to ECL devices. Full truth table function stimulus is applied to the individual IC. Low impedance drivers exercise the IC with high-power, short-duration pulses that quickly distinguish between assembly faults and device failures.

A custom-designed 24-pin universal clip provides the test access for the AFIT 1000 and a similar 40-pin clip is used with the 1500 and 3000A. Our fast 4000 production test system uses Fairchild's Thinline® Vacuum Fixture System ... the nearest thing yet to universal fixturing.

Working within our Testline family gives you maximum software economy because you program a dedicated disk for the PCB to be tested, using a furnished data base library of standard out-of-circuit truth tables for common IC logic families. That's important because software is the critical cost factor in testing.

Whether you bring your boards to the test or the test to your boards, Testline systems give you the technology and the flexibility to develop the best systems for production testing, repair diagnostics and field testing. And the system is backed by Fairchild service and technical support world wide.

Call or write and we'll show you what we can do to help lower your test costs.
Fairchild, 1625 White Drive, Titusville,
Florida 32780 (305) 267-7212



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Test Systems Group

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Circle 23 on reader service card

Parking problems for WARC

Experts have long been warning that the number of orbital parking slots for satellites is limited and rapidly filling as communications satellite usage soars. As an example of this, citing the usual "high demand," RCA American Communications Inc. has asked the Federal Communications Commission for permission to launch Satcom IV in June 1981.

Basically the same as its three predecessors in the series, the satellite has some more advanced battery technology and is earmarked for a spot at 83° west longitude. It will carry commercial private leased channels, Government services, broadcast television, and radio traffic.

But there is one rub. Unlike the previous satellites, Satcom IV cannot put a beam on Hawaii: the 83° position is just too far east,

while the other available slot, at 140°, is too far west to properly serve the major markets on the U. S. East Coast. The Hawaiians will get by, but it is clear that the predicted compromises are starting to be made. While this one was not too difficult to work out, future decisions may defy such easy execution.

All of which calls attention to one of the issues to be addressed by the World Administrative Radio Conference, meeting this month in Geneva: satellite orbit slots and ownership thereof. Certainly, U. S. delegates must stick to technical arguments as advocated by delegation chairman Glenn Robinson. Economic and political polemics should be avoided. At the same time, if they are not going to speak for us — who will?

Solutions only the U. S. can make

The frustration of American manufacturers, particularly in electronics, runs deep. Declining productivity, tightness of capital, Government rules that seem designed to harass rather than protect, and, perhaps most important, increasing shrinkage of overseas markets and inroads by foreign competitors are sources of dismay.

In a recent speech, William S. Anderson, chairman of the NCR Corp. and a British citizen, discusses these problems and some solutions "requiring a fundamental reorientation of our international economic policies." The redirection, says Anderson, should start with "the establishment of a comprehensive national export policy, to be headed by a Department of International Trade with Cabinet status." DIT, as such an entity would inevitably be called in Washington, would help American companies compete in foreign markets, keep the Government from using trade to influence other nations' political or social affairs, revise export controls, reduce antitrust actions as regards overseas trading ventures and "encourage joint ventures by U. S. companies

to bid on foreign projects," modify restrictions such as those in the National Environmental Policy Act where they apply to exports, and offer tax and financial incentives to overseas trade.

Not satisfied with that ambitious program, Anderson also has five points of attack for Congress to "improve the climate for capital formation and investment." They are:

- Changing current depreciation laws to recognize the impact of inflation.
- Liberalizing investment tax credits.
- Providing incentives for personal savings.
- Offering tax credits for accelerated industrial research and development.
- Reviewing regulatory policies to determine how much they are costing the economy and to measure their benefits against their costs.

There is much food for thought in Anderson's plan. But whether one agrees with all of it or not, it is difficult to find fault with his thesis that "it's easy to blame other countries. . . . But it is the U. S. itself which has created most of its problems, and it is only the U. S. which can solve those problems."

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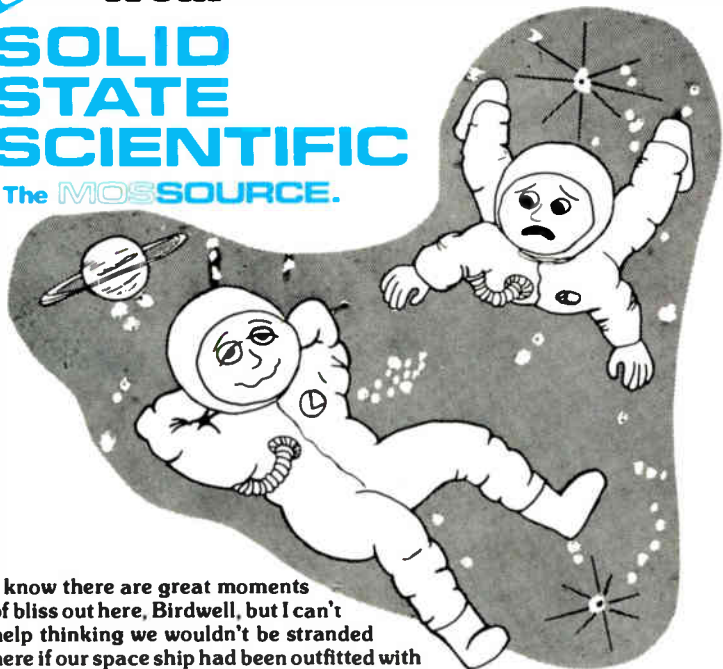


Circle 25 on reader service card



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Meetings

Telecom '79—Third World Telecommunications Exhibition, ITU, Palais des Expositions, Geneva, Sept. 20-26.

IPC Fall Meeting, The Institute for Interconnecting and Packaging Electronic Circuits (Evanston, Ill.), Sheraton Palace Hotel, San Francisco, Sept. 23-27.

Electrical Overstress/Electrostatic Discharge Symposium, ITT Research Institute (c/o RADC/RBRAC, Griffiss Air Force Base, N. Y. 13441), Stouffer's Denver Inn, Denver, Colo., Sept. 25-27.

Military Electronics and Defense Exposition, Industrial and Scientific Conference Management Inc. (Chicago), Rhein-Main Halle, Wiesbaden, West Germany, Sept. 25-27.

Mini/Micro Computer Conference and Exposition, sponsored by the organization of the same name (Anaheim, Calif.), Convention Center, Anaheim, Sept. 25-27.

Second International Conference on Electrical Variable Speed Drives, Institution of Electrical Engineers, at the IEE headquarters, London, Sept. 25-27.

Ultrasonics Symposium, IEEE, Monteleone Hotel, New Orleans, Sept. 26-27.

Gallium Arsenide Integrated Circuit Symposium, IEEE, Sahara Tahoe Hotel, Lake Tahoe, Nev., Sept. 28-29.

Northeast Personal and Business Computer Show, Northeast Expositions (Brookline Village, Mass.), Hynes Auditorium, Boston, Sept. 28-30.

Annual Meeting of the Industry Applications Society, IEEE, Bond Court, Cleveland, Sept. 30-Oct. 4.

International Electrical and Electronics Conference and Exposition, IEEE, Exhibition Palace, Toronto, Oct. 2-4.

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Now you can bring that microcomputer idea to the surface with Mostek's 3870. Already, hundreds of companies have chosen it for its flexibility, reliability and low cost:

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Ed Shortridge, Chief Engineer.

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"Mostek's 3870 cost-effectively replaced a three-chip microprocessor set.

As the controller in the Saxon 301, 302, and soon—the 301R—bond copying machines, the 3870 has improved the Saxon-line reliability with field up-time at all time highs." *Mike Bonavia, Electronic Engineer.*

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Engineering said these new counters were the best values in the industry.

We said "prove it."

They did.

You'd expect our design engineers to be biased in favor of these new counters. But when we challenged them, they convinced us by going back to basics:

"Face it, in a counter, basically two elements determine whether or not you can get accurate repeatable readings: the input amplifier and the crystal oscillator.

In these new counters we've used new thick film hybrid circuits to control input amplifier circuit characteristics and reduce instrument costs.

With these new hybrids we get excellent sensitivity, a flat response and, at the same time, we have reduced the effect of parasitics.

As a side benefit, with hybrids the parts counts are less. This means there are fewer components to fail.

The new ovenized oscillator options were designed especially

for these new counters. That means you get better temperature spec's, aging rates, and better short term stability than with either free air crystals or TCXO's.



As a result, measurement accuracy is improved and calibration cycles can be

extended.

And because these low-power ovens can operate from batteries, there's no time wasted in the cal lab waiting for the oscillator to warm-up. More importantly, cal lab accuracy is preserved when you take the instrument back to the bench."

The engineers went on and on. For example, to reduce false triggering



due to noise, they incorporated stainless steel RFI shields. They're standard on all models.

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Fluke solved the problem of putting low-cost products on the IEEE-488 bus with the Model 1120A IEEE Translator.

With it, you can use any of these new counters with a number of other Fluke instruments in compact, portable IEEE-488 mini-test systems.

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For design engineering and R&D, the Models 7260A and 7261A are full-feature universal counter-timers. Both are 125 MHz models with options to 1300 MHz.**





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|----------------------------------|---------|-------------|------------|------------|
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| Frequency Options | | | 520 MHz | 520 MHz |
| | | | 1300 MHz** | 1300 MHz** |
| Sensitivity (RMS) | 50 MHz | 10 mV | 10 mV | 10 mV |
| | 100 MHz | 15mV(80MHz) | 15 mV | 15 mV |
| | 125 MHz | — | 35 mV | 35 mV |
| Period | | × | × | × |
| Period Average | | × | × | × |
| Time Interval | | 100 ns | 100 ns | 10 ns |
| Time Interval Average | | | × | × |
| Phase Modulated Time Base Option | | | | × |
| Ratio, Totalize, CPM | | × | × | × |
| Autoranging | | × | × | × |
| RFI Shield | | × | × | × |
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Take our 9800 Series Desktop computers. For single-station interactive computing, they're in a class by themselves. With up to 449K bytes of memory, enhanced BASIC, graphics capabilities, and a built-in keyboard and display, you get the power of a minicomputer in one complete, integrated package. And there's easy interfacing with HP instruments and peripherals for jobs like control and testing, statistical analysis, and even engineering design.

For more complex multi-processing tasks, the HP 1000 computer has the power and flexibility to meet your needs. You can choose from a broad range of computation power to process your data, from the low-cost M-Series to the high-speed floating point F-Series. All of the configurations use upward-compatible RTE operating systems, so you don't have to rewrite your programs when you change

jobs or move up to another model. And if you need additional storage, you can expand the systems to two megabytes of main memory starting at only \$18K/per megabyte.

The HP 1000 system also comes with a number of applications tools to minimize your programming costs. HP's new DATACAP/1000 software, for example, lets you design a real-time factory data collection system according to your shop floor needs. And to help you manage vast quantities of technical data, we developed our powerful IMAGE/1000 data base management system. Just a few simple keystrokes give you up-to-the-minute information on inventory levels or instrument check-out status. If you'd like a really clear picture of your information, HP's GRAPHICS/1000 will plot your data in a way you can understand: as a bar graph, pie chart, logarithmic graph, and more.



nd from a computer, ould look at HP

Communication made simple.

General purpose interface cards let you adapt the HP 1000 to a variety of tasks, including A/D conversion and multi-point communications. What's more, with the plug-in HP-IB (interface bus), you can process and control data from over 200 sophisticated measurement and testing instruments.

Talking to the computers is easy, too. The HP 1000 uses BASIC and FORTRAN as well as assembly and micro-code languages. And our powerful communications software, DS/1000, lets you hook HP 1000 computers together in any network configuration you want—across your plant or around the world.

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HP's family of computer products is constantly growing to meet your scientific, engineering, and manufacturing needs. Whether it's instrumentation front ends, CRT terminals, plotters or digitizers, HP's compatible products let you add to your system at any time without writing new software. And of course, you get HP's full support, service, training and documentation.

Go ahead and ask your own computer some tough questions. Then ask ours and see the difference. For a hands-on demonstration of the HP 1000, just call your nearest HP sales office listed in the White Pages. Or for more information write Hewlett-Packard, Attn: Roger Ueltzen, Dept. 659, 11000 Wolfe Road, Cupertino, CA 95014.

Here are just a few of HP's range of products for manufacturers and engineers:

1. HP 9845 Desktop Computer.
2. HP 9825 Desktop Computer.
3. HP 1000 Model 45 Real-time System with HP 7906 Disc Drive and HP 2648A Graphics Terminal.
- 4-6. HP 1000 F-, E-, and M-Series Computers.
7. HP 2108 Board Computer.
8. HP 7925 Mass Storage Unit.
9. HP 2240 Measurement & Control Processor.
10. HP ATS Automatic Test System.
11. HP 12050 Fiber Optics.
12. HP-IB Link IEEE-488 Standard Interface.
13. HP 2621 CRT Terminal.
14. HP 3075 Data Capture Terminal.
15. HP 3077 Time Reporting Terminal.
16. HP 3455 Voltmeter.
17. HP 3495 Scanner.
18. HP 5328A Universal Counter.
19. HP 5342 Microwave Frequency Counter.
20. HP 436A Power Meter.
21. HP 4262 LCR Meter.
22. HP 8566A Spectrum Analyzer.
23. HP 8754A Network Analyser.
24. HP 3325A Synthesizer/Function Generator.
- 25-6. HP 8660A & HP 8672A Synthesizer/Signal Generators.
- 27-8. HP 9876A & HP 2608 Printers.
29. HP 2631G Graphics Printer.
30. HP 7245A Thermal Plotter/Printer.
31. HP 7221A Plotter.
32. HP 7225A Graphics Plotter.
33. HP 9872A Programmable Graphics Plotter.
34. HP 9874A Digitizer.
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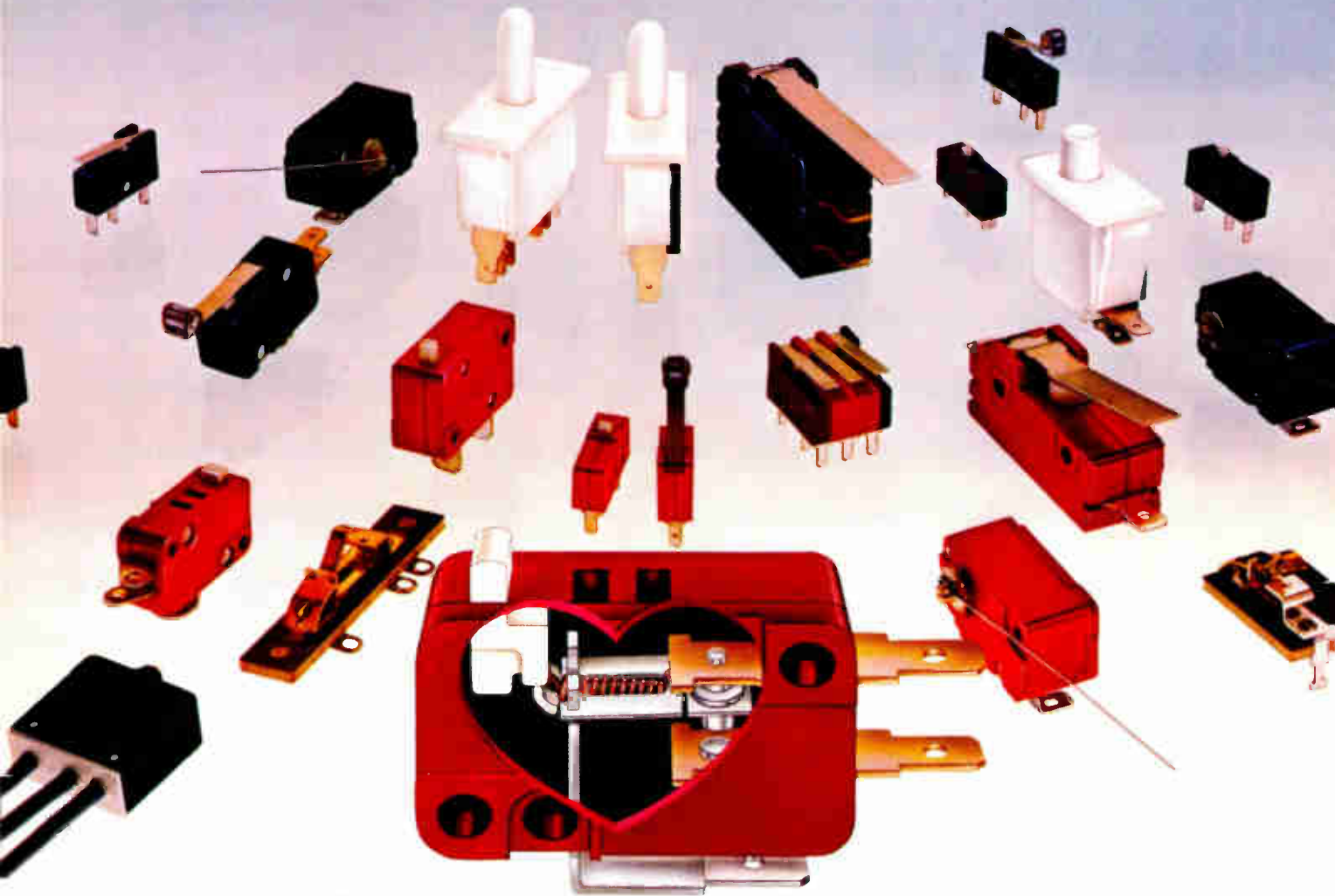
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Word processor combines best of stand-alone, sharing

Word processing has advanced another step in ease of use and reliability with the introduction of two systems from CPT Corp. Combining the dependability and productivity of stand-alone systems with the information storage and retrieval abilities of shared logic systems, **Wordpak I and II use Winchester-type disk drives interfaced with up to eight individual work stations to provide multi-user, multitasking systems.** The Hopkins, Minn., firm is basing what it calls these shared-resource systems on the CPT 8000 word processor to give users access to up to 50 million characters of information. Both systems will support peripherals, printers, and telecommunications links via an asynchronous line protocol from each CPT 8000 work station. The Wordpak I, supporting up to four stations priced at \$10,990 each, uses a CPT 8040 disk drive unit costing \$8,500. The Wordpak II, with up to eight stations, is based on a CPT 8050 disk drive with its own microprocessor controller, memory, and input/output logic; the 8050 sells for \$12,000.

Intel to become second source for AMD math chips

It looks as if Intel Corp. will be selling arithmetic peripheral chips sooner than expected. Watch for the Santa Clara, Calif., company to second-source the industry-leading AM 9511 arithmetic processor and AM 9512 floating-point processor devices introduced by Advanced Micro Devices Inc. **The move will be part of the deal by which AMD second-sources Intel's 8085 8-bit microprocessor.** Samples of Intel's H-MOS parts, the 8231 and 8232, respectively, are due out soon, but prices are undetermined. However, AMD sells the two chips at \$175 each in small volume. The 8231 and 8232 will work with 8-bit bus systems, such as the 8080, 8085, and 8088, but Intel is known to be readying a blockbuster 8087 arithmetic processing chip that will work hand in glove with the 8086 16-bit microcomputer.

Gould takes first step in Mostek takeover

Attempting once again to buy its way into the semiconductor business after last spring's unsuccessful bid for Fairchild Camera and Instrument Corp. [*Electronics*, May 24, p. 58], Gould Inc. has purchased 21% of Mostek Corp.'s common stock from Sprague Electric Co. and says it may seek to acquire control, possibly with the \$175 million war chest it assembled for the Fairchild battle. The price paid by the Rolling Meadows, Ill., battery and controls maker for Sprague's stock was \$51.5 million, or \$42 a share. In Carrollton, Texas, Chuck Barker, Mostek's vice president for finance, says the company will say nothing until it spends some days evaluating the offer, though it does have the right to repurchase the Sprague stock within 60 days. **Industry insiders say that Mostek officials were caught by surprise,** although there have been reports for months about suitors for the company, which is believed to be willing to be acquired—though not by Gould. One source close to Mostek says that it will now look for a so-called white knight to outbid Gould.

IBM endorses video disk concept with MCA deal

International Business Machines Corp., apparently believing video disks will provide a good storage medium for information-processing systems, has formed a joint venture with MCA Inc. of Universal City, Calif., to develop, manufacture, and market video disks and their players. Already the holder of two patents on the basic optical recording and playback techniques used, IBM will pool its technology with that already developed

Electronics newsletter

by MCA in conjunction with Philips of the Netherlands; **the new joint venture will license these patents on a nondiscriminatory basis**, the companies say. Interestingly, IBM has placed responsibility for liaison with the new joint venture in the hands of its White Plains, N. Y., General Business Group, whose five divisions include the General Systems division, which makes small business machines, and the Office Products division, which makes typewriters and word processors.

Makers of heavy road, farm vehicles hit by IC shortages

Detroit auto makers, whose voracity for integrated circuits is mentioned as one reason for the current supply crunch, are also skewing the plans of other vehicle makers anxious to switch to electronics from electro-mechanical devices. Manufacturers of heavy-duty construction and farm vehicles, wanting to boost the productivity and reliability of their trucks, road graders, and tractors [*Electronics*, Jan. 4, p. 46], are anxious to install electronic controls and dashboard monitors, **but find components unavailable**. The drive to upgrade their vehicles by installing autolike systems has inspired a Silicon Valley-type recruiting raid—International Harvester Co. of Chicago has just hired John F. Ullrich, formerly the chief electronics engineer at Ford Motor Co.

Internally based connector saves space and cost

An innovative selective-ground connector that does without paddle boards and reduces printed-circuit-board costs while using less space will be introduced at Wescon (Sept. 18–20) by Augat Inc. of Attleboro, Mass. The connector is aimed at applications requiring mass-terminated planar twisted cables with a ground-signal-ground configuration.

In the new cabling system, which uses insulation-displacement contacts, an integral bus system interconnects and internally groups common wires from a single-ground input point. **This permits a single connector to accommodate two layers of cable**, a job that now requires two conventional connectors.

Shugart readying 58-megabyte fixed-disk drive

Xerox Corp.'s Shugart Associates subsidiary in Sunnyvale, Calif., has embarked on a development program that would culminate in the second half of the next year in a 58-megabyte, 14-in. fixed-disk drive. Presently, **Shugart makes and markets the SA4008 series, a 29-megabyte, 14-in. unit** that represents the top of the line in its family of fixed-disk drives utilizing Winchester head and media technology.

Addenda

GTE International Systems Corp. of Waltham, Mass., has won two contracts to update earth stations in Sweden and Morocco to compatibility with Intelsat 5, the 1980s' communications satellite system. **The stations will use a scheme that utilizes the same frequency or band twice.** . . . Making good on earlier-stated intentions [*Electronics*, May 10, p. 34], Texas inventor and freelance writer Forrest M. Mims III has filed a \$30 million lawsuit against Bell Laboratories charging unauthorized use of an idea Mims claims is his. . . . A new line of high-efficiency rectifiers is coming from the Unitrode Corp., Watertown, Mass. It will range from 1 to 50 A in packages ranging from the glass axial-lead type to TO 220. **The parts will have 100-ns recovery times and 15% to 20% improvement in forward voltage drop over available devices.**

TRY THE 4K RAM YOU DON'T HAVE TO RETURN.

Reliability spells the difference between "just another commodity RAM" and the EA 2114 1K x 4 static NMOS RAM. Reliability built-in with extra heavy lead frames that shunt more calories of heat away from your chip. Or IC circuitry painstakingly designed to provide $\pm 10\%$ power supply tolerances. It's this kind of reliability that gives you more usable parts at incoming inspection, and measurably fewer field problems in your finished products.

There's more. The EA 2114 comes in a variety of access speeds, including one of the fastest on the market: 150 ns. Look 'em over.

Then pick exactly the RAM you need, and buy it with confidence from Electronic Arrays. 550 East Middlefield Rd., Mountain View, CA 94043, (415) 964-4321; Philadelphia, (215) 643-1447; Chicago, (312) 858-8508.

| Part Number | Access Time |
|-------------|-------------|
| EA 2114L | 450 nsec |
| EA 2114L-30 | 300 nsec |
| EA 2114L-25 | 250 nsec |
| EA 2114L-20 | 200 nsec |
| EA 2114L-15 | 150 nsec |

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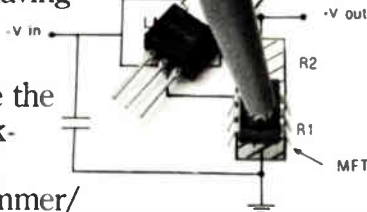
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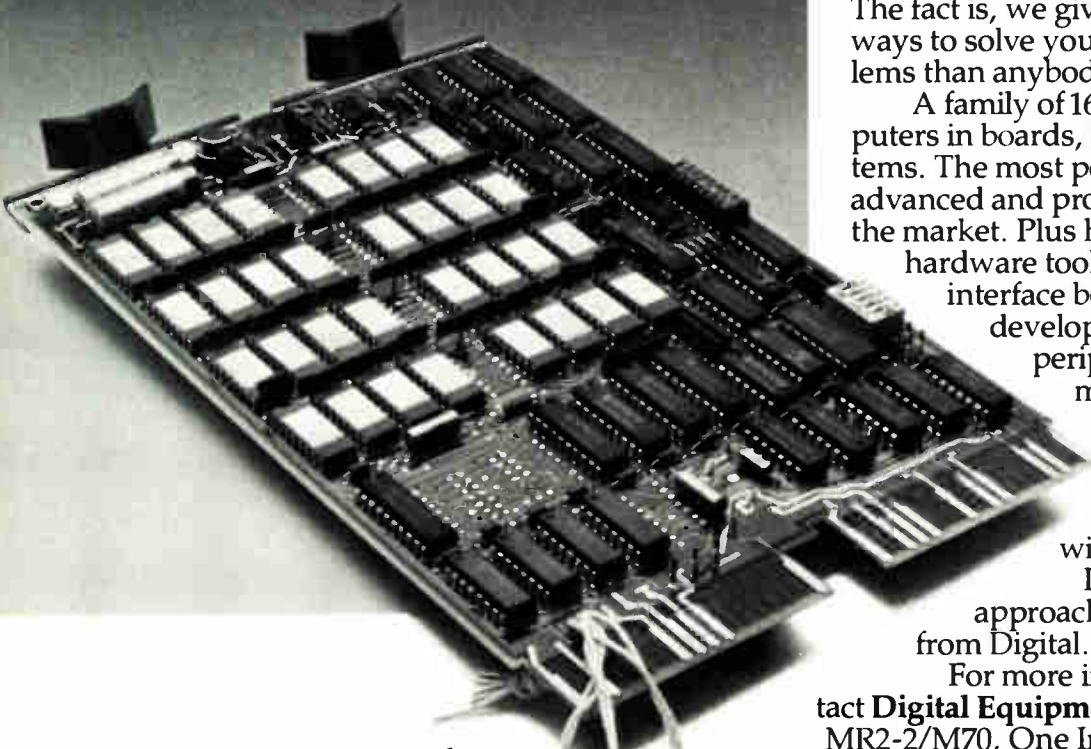
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Static RAM tunnels for nonvolatility

by Raymond P. Capece, Solid State Editor,
and John G. Posa, Microsystems & Software Editor

Backup memory locations
store data in floating gates;
intentional leakage
writes and erases the bits

Millions of research dollars have been spent on the electron tunneling that causes undesirable leakage currents in memory chips. Now that unwanted tunneling is the technological foundation for a company that will build nonvolatile random-access memories.

Newly formed is Xicor Inc., whose founders plan to take on the semiconductor giants with their nonvolatile 1-K static memories. The parts that the Sunnyvale, Calif., company is introducing have the basic operating characteristics of a standard 2102 static RAM but offer a nonvolatile "shadow" memory.

Shadow. Backing up each conventional memory location is a floating-gate transistor. It can store data independently or can save the data from the static cells. In either case, the static circuitry is the go-between.

Supporting a static RAM cell with nonvolatile storage is not new. Hughes Corp. and several Japanese companies have reported devising nonvolatile read/write cells of the metal-nitride-oxide semiconductor and floating-gate-avalanche metal-oxide-semiconductor types. But Xicor uses circuit and device twists to enable operation with a 5-volt supply and to ensure reliability.

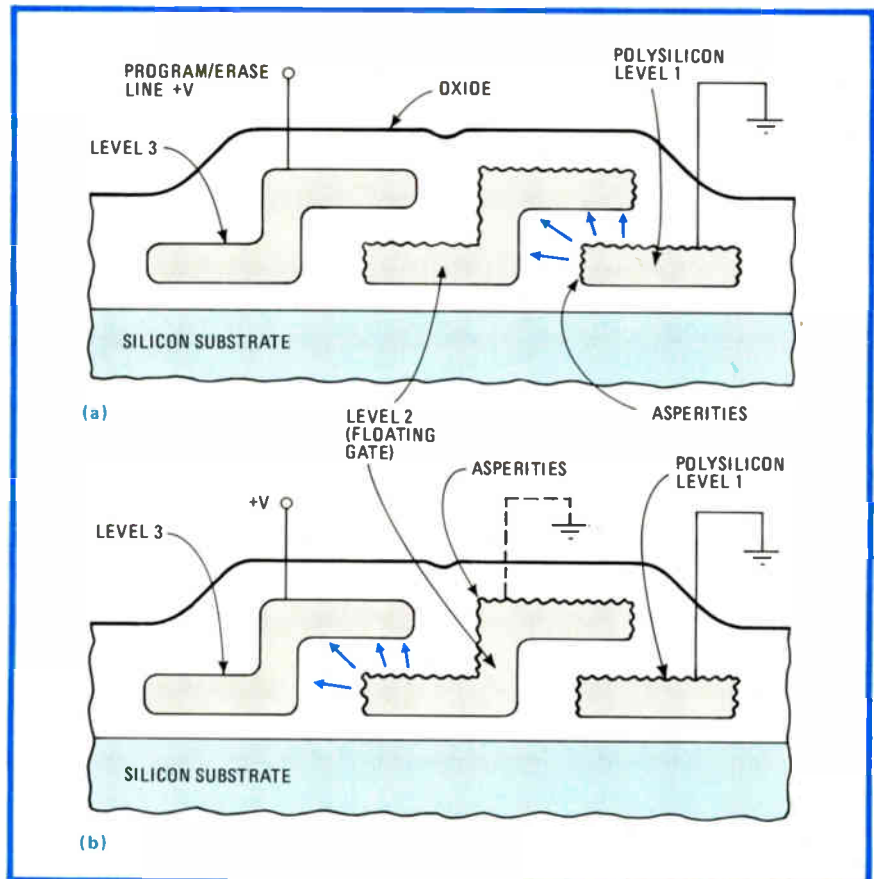
The nonvolatile locations store data on their floating gates, much as erasable programmable read-only memories and electrically erasable

PROMs do. It is in erasing the bits that the Xicor parts promise to star.

The erasure procedure for EPROMs is cumbersome and lengthy, involving as it does exposure to an ultraviolet light that causes the charge to leak off. (The parts also require a high writing voltage.) Forcing electrical leakage by applying a 26-to-40-V current as do EEPROMs is not reliable. (And there is a limit to the number of erasures possible.)

Xicor's parts rely on leakage induced by tunneling (see "The phenomenon of tunneling," p. 40). The method involved seems to hold promise for a solid basis for other nonvolatile memory types.

Three-level polysilicon. To build the parts, the firm uses a three-level polysilicon process (see figure). Data is written when a voltage is applied to the electrode formed in the third level, making electrons from the first-level electrode tunnel to and



Nonvolatile RAM. Charge tunnels to higher potential of the floating gate to store a bit (a). When gate potential approaches ground, charge tunnels to the third level (b), erasing the bit.

The phenomenon of tunneling

As early as 1973, Toshiba Ltd. discovered that conduction through insulating silicon dioxide grown thermally over polycrystalline silicon is markedly higher than that measured when the oxide is grown atop single-crystal silicon. IBM Corp. studied the phenomenon as an undesirable side-effect and concluded that electron tunneling was encouraged by sharp needle-like protrusions that were on the surface of the polysilicon (see figure on p. 39). The asperities, as they are called, concentrate charge at their tips and support enhanced, localized conduction, as much as an order of magnitude greater than on a flat polysilicon surface.

The asperities occur because oxidation progresses faster along some crystal directions than others. Since crystal orientation is by definition jumbled in polysilicon, there are points on its surface where oxide growth is reinforced, causing peaks, and other points where it is inhibited, causing valleys. Xicor intentionally grows the asperities on its first two levels of polysilicon to charge and discharge the floating gate.

Actually the polysilicon surface is rough to begin with, but the temperature of the oxide-growing process apparently determines the height and sharpness of the peaks. At 1,150°C, for example, the surface morphology is rather flat, but at 1,000°C asperities abound. Of course the temperature of the oxide growth controls more than the size and shape of the asperities: it also determines the size of the electric field necessary to induce leakage currents from them.

-J. G. P.

charge up the floating gate to which it is capacitively coupled.

Erase occurs when the floating gate is pulled to ground. This causes its electrons to leak off by tunneling to the third-level electrode.

Credibility. Several factors lend credibility to the company's exploitation of the tunneling phenomenon. First is that Xicor has persuaded Ebauches Electroniques SA, the Swiss watch and semiconductor maker, to produce the RAMs in return for European marketing rights. Second is that, according to Xicor, production volumes are already high enough to fill orders.

"We don't want people to think we've just got a discovery here," explains S. Allan Kline, chairman of the new company. "We've got parts on distributors' shelves." Kline, a former director of Intersil, and president Raphael Klein, a former program manager at Intel, have manufacturing facilities in planning.

The X2201 and X2202 devices they are introducing add two pins to the 2102 design. Both chips store by transferring all bits to the nonvolatile backups. To transfer the bits back to the static locations, the 2201 has an array-recall pin and the 2202 has a bit-recall pin.

Data communications

Bell providing TV data service in quiet testing of waters

With scarcely a splash, the Bell System is quietly testing the waters of the videotext business. American Telephone & Telegraph Co. and the New York Telephone Co. are testing what they call the Electronic Information Service: a randomly selected group of Bell customers in the Albany, N. Y., area will have video access

to Bell computers for directory information and weather, time, and sports updates.

Venture. The test signals Ma Bell's strongest involvement to date in the interactive data-access-and-retrieval business. This field has been dominated by European and Canadian interests, with General

Telephone & Electronics Corp. planning U. S. tests of Prestel, the British viewdata system.

Perhaps more important, the service or expanded versions thereof could become part of AT&T's proposed Advanced Communications Service [*Electronics*, Dec. 7, 1978, p. 83]. The computer is not limited to one type of data base and could provide many kinds of information. This is the route being taken by viewdata services, which link TV sets in the home or office to computer data banks via phone lines. Programs could include such highly interactive services as income-tax preparation or airline reservations.

A competing British-originated system, teletext, provides what might be called a broadcast magazine—pages of information distributed to TV receivers by transmitting special signals during the vertical blanking interval of TV signals. In the U. S., CBS Television is trying out Antiope, a French version of teletext [*Electronics*, Jan. 18, p. 33].

Hooking up. According to Edward Hancharik, AT&T's director of directory services in Parsippany, N. J., each user will have a cathode-ray-tube terminal and a keyboard for access to the system. The computer will display a menu on the viewing screen. The user need only type in the identifying alphanumeric of the desired menu item to get the requested information.

"The system is transparent to the terminal and the television set," says Hancharik. It appears then that many different kinds of users with a variety of terminals should be able to be hooked up rather simply. Just such a characteristic is what AT&T has been claiming will be the case for its ACS system when it comes along to provide business communications for the much heralded office of the future.

For now, no Yellow Page advertisements will be supplied, just easily updated listings from the computer, which is otherwise generally accessed by information operators. However, there is a "real possibility" of providing these ads in the future, Hancharik says. -Harvey J. Hindin

Development systems head to hard disks as application, systems programs tax capacities

Hewlett-Packard Co.'s long-rumored introduction of microprocessor development systems becomes a reality this week when its Colorado Springs (Colo.) division takes the wraps off its model 64000 universal development system. The multistation rig relies on the large amount of data storage and fast response time of a hard disk to give it a high-performance operating system.

Company. Nor is HP alone in moving to hard disks. Intel Corp.'s recently announced Intellec 240 also incorporates the large-capacity units (see following story). The impetus for the hard-disk add-on is simple enough: microprocessor programs are exploding in size.

Not only are application programs swelling, but programmers are becoming used to operating systems and high-level languages. Thus, storage-hogging systems programs and application programs under development must be housed in a readily available medium, such as large-capacity disks.

A typical 8-inch double-sided double-density floppy disk has a 1-megabyte capacity. Intel is offering 7.3 megabytes on its hard-disk drive, and HP apparently will offer from 20 megabytes up.

The multistation architecture of HP's 64000 can support as many as six development stations operating simultaneously and sharing a disk drive and printer. The basic system will cost about \$25,000, each additional station will cost perhaps \$8,000, and the largest configuration will go for about \$127,000.

Multisupport. When first deliveries begin in November, the system will support four of the popular 8-bit processors: Intel's 8080 and higher-performance 8085, Motorola's 6800, and Zilog's Z80. By mid-1980, similar relocating macroassemblers and real-time emulators should be available for such chips as Intel's 8048

microcomputer and 16-bit 8086.

While reports of the 64000 have been appearing [*Electronics*, July 19, p. 33], HP is keeping some details to itself, pending the official introduction. It appears that the hard disk is the company's standard 7096 cartridge disk drive which has fixed and removable disks of 9.8 megabytes each in its basic configuration. Total hard-disk capacity is expandable to 120 megabytes.

Each development station has a host processor, believed to be of 16-bit architecture, with a 64-kilobyte random-access memory. In addition to emulators for the four microprocessors, options initially available include as much as 128 kilobytes of emulation memory, a cartridge tape drive for file backup and software entry, an integral programmer for programmable read-only memories,

and an RS-232-C interface. There is no high-level language support at present, but HP says it intends to introduce a Pascal compiler.

That the 64000 is a universal system comes as no surprise to most industry observers. "This gives the stamp of approval to what we have been saying all along, and shows the dedicated system is dead," says Martin Weisberg, director of marketing at Millennium Systems Inc. The Cupertino, Calif., firm designed and manufactures the 8001 and 8002 universal systems marketed by Tektronix Inc.

Support. Agreeing that there will be more development-system hard disks is Galen W. Wampler, vice president of Dataquest Inc., the Cupertino market researchers. "A floppy disk is too slow, especially where it is going to be used by multiple users, and a removable disk pack is too bulky and expensive."

Availability is a key, says James M. McCoy, manager of product management at Shugart Associates, the Sunnyvale, Calif., manufacturer of floppy and hard disks. "Large-



Universal. Hewlett-Packard's first microprocessor development system will support numerous processors and as many as six development stations. It has hard-disk storage.

capacity memories have not been available for development systems," McCoy points out, but now inexpensive rigid disk-drive memory systems are available. **-Bruce LeBoss**

Second system goes to hard-disk memory

With microprocessor-based systems addressing megabytes of memory, support hardware must add capability to keep up. So it is that Intel's latest development system, the \$21,990 Intellec Series II Model 240, sports a 7.3-megabyte cartridge disk drive in addition to a 256-kilobyte floppy-disk drive, 65 kilobytes of random-access memory, and other hardware and extensive software facilities.

Intel Corp. chose to split up its mass-memory subsystem, with 3.65 megabytes each on a fixed 14-in. platter and a removable IBM 5440-type cartridge disk. "A removable medium is absolutely required," maintains Barry Yarkoni, who is product manager for development systems at Intel.

Suitabilities. Fixed storage is fine for system software and is particularly well suited for utility-routine libraries, he says. Removable storage, however, will hold application programs, he predicts, with each programmer working from his or her own cartridge disk.

The model 240 is intended to fill a gap that the Santa Clara, Calif., firm sees growing, as the notion of division of labor takes hold for multiple-station development systems. Intel expects the development stations to be dedicated to text preparation or in-circuit emulation.

"The missing link is a system geared for program compilation, linking, and location," says Yarkoni. So the 240 features a special version of the company's ISIS II operating system. It offers significantly higher performance in compilation and assembly over floppy-disk-based development systems.

Hard-disk latency is 50 milliseconds typical compared with 340 ms

for floppies; the transfer rate is 2.5 megabits per second compared with the Intellec systems' floppy-disk's 160 kilobits/s.

Choices. The system uses 14-in. disks rather than the 8-in. Winchester drives that seal disks and heads into a hermetic unit, "because they are available and because they are second-sourced," Yarkoni says. The makers of 14-in. disks "ship hundreds a day, and they work. And Winchesters are not plug-compatible. It's painful in a high-technology company to realize, in this instance, that state-of-the-art components cannot be used." Coming is an upgrade package that "will allow

any Intellec to use the system."

Still, floppy disks will not soon be supplanted by hard disks, Yarkoni believes—as does James M. McCoy, manager of product management at disk maker Shugart Associates. They will continue to be the standard distribution medium for software, as well as the most economical way to store source and object code from old projects, they say.

Also, in development laboratories that divide up labor, hard disks are overkill for text origination and debugging, so floppies will continue to suffice on those stations. Finally, they are an excellent means of carrying software. **-John G. Posa**

Computers

\$300 encryptor uses unique algorithm, keeps data secure in small systems

That's not garbage on the screen of the TRS-80 small computing system in the photograph on p. 44—that's a message coded in a unique algorithm by Cryptext, a surprisingly low-cost device that can plug directly into the back of the computer or into the expansion interface.

For \$300, users get the operational software and cigarette-pack-sized encryptor-decryptor; for less than \$50, they may buy additional software to store the coded data on disks or tape. The TRS-80 version is the first of a line of such devices for small computers, with a model for the Apple systems to be available by October.

At Radio Shack headquarters in Fort Worth, Texas, computer-division vice president Jon Shirley says the company has no plans to make a similar device. Though there is interest in ways to protect software developed for the TRS-80, there has been little call for an encryption device from the small businesses that are typical users, he asserts.

Unlike the typical computer encryptor, Cryptext uses a proprietary algorithm rather than the Federally sponsored data encryption standard [*Electronics*, June 21, p. 107]. Its

designers, Carl R. Nicolai, William M. Raike, and Carl R. Quale, principals in the Cryptext Corp., Seattle, Wash., claim their algorithm is better than DES because it offers more keys and is less susceptible to code breaking.

Lots of bits. To encode data, the user supplies the device with a key consisting of 10 characters from which Cryptext derives the scrambling pattern. In the 8-bit ASCII system used by the TRS-80, the key amounts to 80 bits, allowing 2^{80} different keys. The DES algorithm provides only 56 key bits.

In addition, what Raike calls a code-branch feature in the software allows the device to modify its sequence during coding so that over 2^{350} keys are available. Such a number is possible because the part's nonlinear pseudorandom-code generator has a period greater than 2^{350} .

This gigantic number of keys, of course, is not the whole encryption story, since it is useless if the algorithm can be broken. "That is not practically possible," says Raike, who drew on his background in mathematics and cryptography to develop the algorithm.

The code is less breakable than

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Secret stuff. By plugging in the Cryptext encryptor-decryptor, users of TRS-80 small computers can turn data into scrambled patterns. Units for similar computers are next.

the DES, he says, and he intends to offer a reward to encourage attempts to crack it. That is the ultimate test of a cryptographic system, as no known theoretical analysis will prove that a system is secure.

"The algorithm is highly nonlinear," is all Raiké will say of his creation. He and Nicolai expect major interest in keeping safe such information as tax data, financial information, medical and personal data, mailing lists, and, in fact, any list that must be protected from unauthorized access.

Safe delay. To enhance Cryptext's security, a delay is built into the software's initialization sequence. It prevents brute-force code breaking, which works by rapid and exhaustive key cycling.

To make matters worse for a would-be code breaker, the device is epoxy-potted and protected against both physical intrusion and radiation. Moreover, there is no storage of the key after initialization, nor is there any remnant of the plain text after encryption.

Encryption time is 20 microseconds per character and input/output time is about 2 μ s per character, so that relatively large data rates—up to 15,000 characters per second—can be handled by the 1-pound, 1.1-by-3.0-by-5.3-inch device. Thus, Cryptext can serve many small-system applications.

The unit typically requires 6

milliamperes at 18 volts but can run with anything from 7 to 25 v at 11 mA maximum in an 8-bit parallel asynchronous mode. A version designed to operate with the Electronic Industries Association's RS-232-C serial interface will be ready by the end of the year.

Cryptext was introduced at the Small Computer Show in New York at the end of August. There, computer buffs were shown documentation for each unit that permits development of software for access to the device from Radio Shack Level II Basic or assembly language.

-Harvey J. Hindin

Packaging & production

Deep UV option promotes fine lines

Semiconductor manufacturers contemplating production of very large-scale integrated circuits shudder at the cost of the lithography equipment necessary to achieve IC line widths of under 2 micrometers. Realizing this, Optical Associates Inc. is readying a relatively inexpensive optics package it says will allow contact and proximity printers to achieve line widths as fine as 0.7 μ m.

To resolve submicrometer dimensions, the OAI system uses a precisely controlled light source with spectral

emission optimized in the deep ultraviolet region (see figure on p. 46), says George A. Lee, president of the six-year-old Santa Clara, Calif., firm. To be available around the first of the year, the package is a retrofit for contact and proximity printers made by various companies, with a stand-alone UV source coming later.

Resists. The lamp and reflective optics are tuned to 220 nanometers, the optimal wavelength for the polymethyl methacrylate material used as deep UV positive resist. They also can be supplied for operation at 253.6 nm, the optimal wavelength for a newer resist, polymethyl isopropenyl ketone.

The system does nothing to lengthen the short mask life caused by the inevitable damage due to contact with both contact and proximity printers—and the fine-line masks for VLSI will of course be more expensive. Similarly, the alignment of successive masks becomes even more critical when the features being defined are under 2 μ m wide.

However, Lee expects the cost-effectiveness of OAI's solution to attract users. For \$15,000 to \$25,000 per unit, the semiconductor maker can extend the life of his present lithography systems, which rarely cost more than \$75,000—roughly a third that of projection printers.

OAI designed the system and is having the lamp built by an outside supplier. "We had to confront a number of complex factors, such as gas mixture and gas pressure in the lamp envelope, as well as the spectral absorption characteristics of the envelope itself," Lee says of the design process.

Part of the solution depended upon developing a special coating of multilayer dielectrics for the reflecting optics. These coatings are tuned to be reflective at the wavelength of interest, the optics becoming a "mirror that transmits infrared and reflects UV," he says.

The IR light is transmitted through the optics to a heat sink and carried away by a forced-air cooling system. "Thus we can regulate the temperature of the lamp and need not worry about having heat trans-

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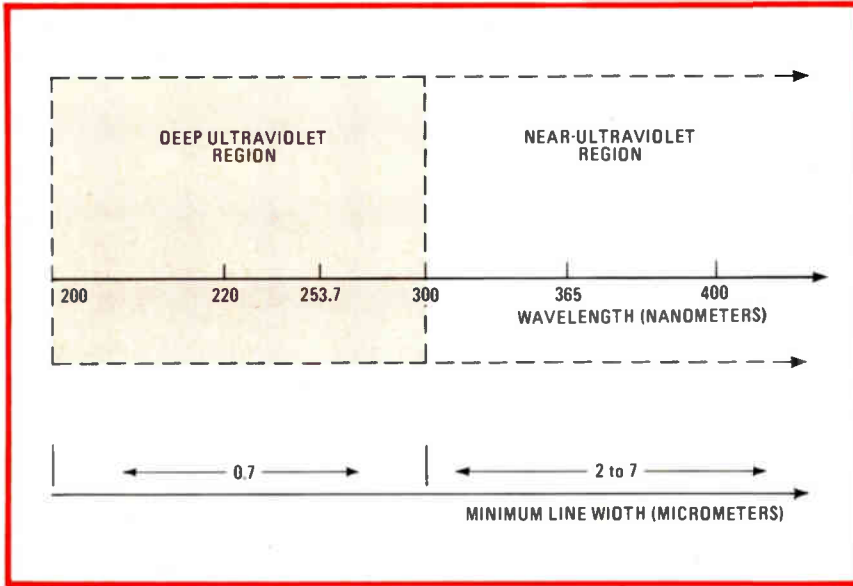


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Mighty fine. For optically based lithography units to define submicrometer features, a deep ultraviolet light source is needed. A new optics package can provide that source.

mitted to the wafer plane and warping the wafer," he says.

Is OAI moving into equipment that will disappear with the dawning of the VLSI age? Some makers of contact and proximity printers apparently think not, for they also have plans to extend their products into the deep UV band. For example, Japan's Cannon Inc. has a deep UV contact and proximity printer that sells for \$160,000.

Computervision Corp.'s Cobilt division in Santa Clara is reportedly

developing a 1- μ m deep UV retrofit for its CA-850 contact aligner, as well as a 2- μ m proximity option. It is understood that these developments are the preliminaries to a deep UV projection aligner.

Such upgrades may be seen as "an attempt to compete with projection aligners," which is all that a Cobilt spokesman will say. What's more, "there are a number of developments whose goal is to improve the yields for both contact and proximity systems."
-Bruce LeBoss

Trade

New law toughens dumping provisions; threat of future injury may be grounds

Charges that foreign companies are dumping their products in the U.S.—that is, selling them for less than they get at home—are difficult to prove. What's more, the procedure takes so long that even if guilt is established, the complaining American company might already be mortally wounded.

But the situation should be alleviated somewhat by the Trade Agreement Act of 1979 signed into law in July. Not only does the new law considerably shorten the en-

forcement timetable, but it also provides that evidence of the threat of future injury is enough ground to initiate antidumping action.

That latter provision is important: a company or industry may file dumping charges when it begins losing market share in a particular product to foreign competitors, instead of waiting until it is on the point of having to close factories.

Establishing the concept of threat is "clearly the intention of the Senate and House and [White

House trade specialists]," declares Peter Archy. He is with the Washington law firm of Peabody, Rivlin, Lambert, and Meyers, which represents the Semiconductor Industry Association (SIA). "They're agreed that the concept of threat now has received the attention it hasn't received before, particularly in a high-technology industry."

Worried about Japanese inroads—for example, 35% of the voluminous U.S. market in 16-K dynamic random-access memories—the SIA lobbied for the threat concept because "we saw no hope under the way the laws were written," explains Thomas Hinkelman, executive director. "There's no action based on market share we could take under the old law."

Pattern awaited. Still, the question of whether dumping charges will be easier to prove "will depend on how the law is interpreted and enforced," observes one White House trade expert. It will be months, possibly more than a year, before the patterns are clear, he thinks.

"Until now the damage had to have already been done," admits another White House trade specialist, "but that is changing." However, whether an injury threat is large enough to warrant Government antidumping action is going to be a matter of interpretation. What some manufacturers see as a threat may not seem so to the enforcing agency. Consequently, he says, "that is where the interpretation comes in, and it can become tricky when you are trying to forecast a trend instead of dealing with past practice."

Also clouding the issue is President Carter's proposal to reorganize the machinery for trade policy making [*Electronics*, Aug. 2, p. 57]. That plan is already under Senate attack as being a poorly conceived reshuffling of personnel. It would, for example, take enforcement of antidumping and countervailing duties away from the Treasury Department's Customs Service and put it in a new Department of Trade and Commerce. Some Government trade specialists fear that consolidating responsibility for dumping cases in

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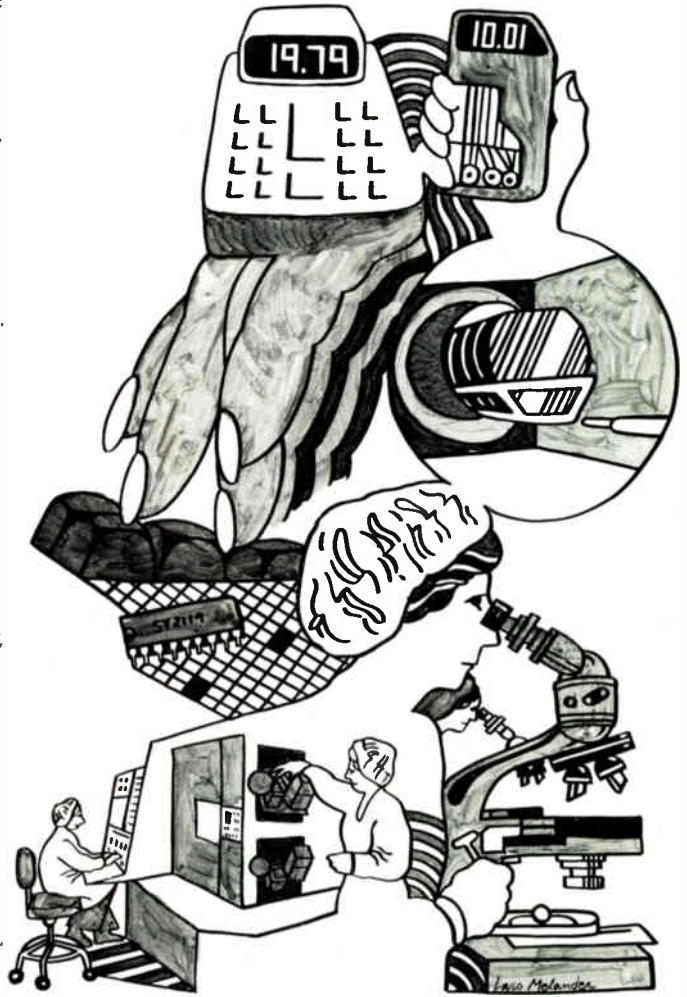
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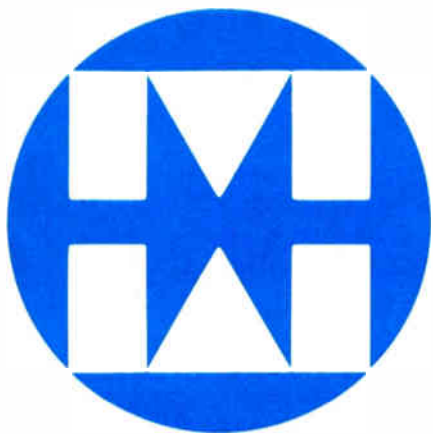
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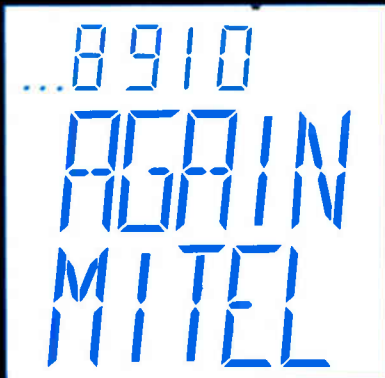
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Electronics review

the pro-industry Commerce Department could accelerate protectionism and handicap trade.

Now that the new trade law has made it easier for electronics companies to file complaints about dumping by foreign competitors, they should start taking advantage of it early and often, right? "Wrong,"

says a White House trade specialist. Companies should not let the new regulations go to their heads, because a sudden flood of complaints "buries the bureaucracy under piles of paper," which could "slow down the whole enforcement procedure and negate any advantages."

-William F. Arnold, Ray Connolly

News briefs

Intel, Amdahl score in user survey

Despite their present marketing problems, Intel and Amdahl beat IBM in a user rating survey just completed by McGraw-Hill's Datapro subsidiary. The Delran, N. J.-based firm sent questionnaires to its 10,000 subscribers asking about such items of user satisfaction as ease of operation, reliability, maintenance response, and technical support. (Datapro cautions, however, that unequivocal conclusions cannot be drawn from the survey because of the small sample.) Compiling the 894 responses on a scale of 1 to 4 showed that the users rated Intel 3.5, Digital Equipment Corp. 3.4, and Amdahl 3.3, with IBM, Honeywell and Control Data tying for fourth place with 3.1. Burroughs and Sperry Univac got 3.0 ratings, while NCR got a 2.9.

Sharp to make amorphous silicon parts

A search of almost two years for a commercial producer of amorphous silicon devices has ended for Stanford Ovshinsky. His Energy Conversion Devices Inc. [*Electronics*, June 8, 1978, p. 35] has signed Japan's Sharp Co. to a nonexclusive worldwide license to develop, manufacture, and market an electrically erasable programmable read-only memory. The Troy, Mich., firm had a design deal with Burroughs Corp., but the latter decided not to go into semiconductor supply.

Array processors, minis team

To provide end users with high-speed arithmetic processing for specialized scientific activities, Floating Point Systems Inc. is teaming up with systems house First Computer Corp. First Computer will take the new FPS-100, made by the Beaverton, Ore.-based maker of array processors [*Electronics*, April 12, p. 209], and integrate it with DEC PDP 11/23 minicomputers to create systems priced in the \$60,000 range. Jerome Martin, president of First Computers in Westmont, Ill., says these packages will offer "a new level of price/performance to scientists, engineers and researchers," reflecting the recent trend towards linking specialized peripheral processors with minicomputers to provide economical high-precision and high-speed processing found previously only in mainframe computers [*Electronics*, Aug. 30, p. 81].

Support is here for analog microprocessor

Users waiting to put Intel Corp.'s 2920 analog microcomputer to work now have the go-ahead. The Santa Clara, Calif., firm has brought out a follow-up support package for the real-time signal processing device, which sells for \$250 in 100-piece quantities [*Electronics*, March 1, p. 105]. The \$3,400 SP20 package consists of hardware and software, the latter supplied on diskette to work with Intellec microcomputer development systems. An assembler converts 2920 assembly language into the device's internal microcode format. The assembler also generates data for a software simulator.

Imlac enhances phototypesetting system

Companies with in-house publication departments are the target of a new phototypesetting system said to significantly ease the production of books and lengthy technical reports. The \$13,000 Bookmaker software package can be added to the \$59,000 Composer 1550 composition hardware. Both are made by Imlac Corp., the Needham, Mass., subsidiary of Hazeltine Corp.

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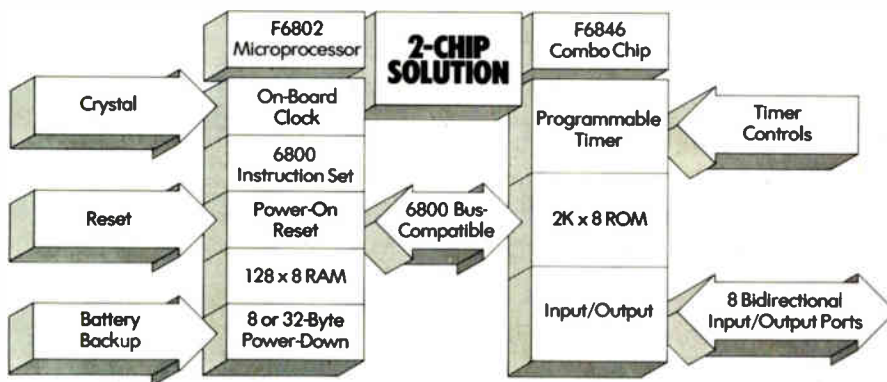
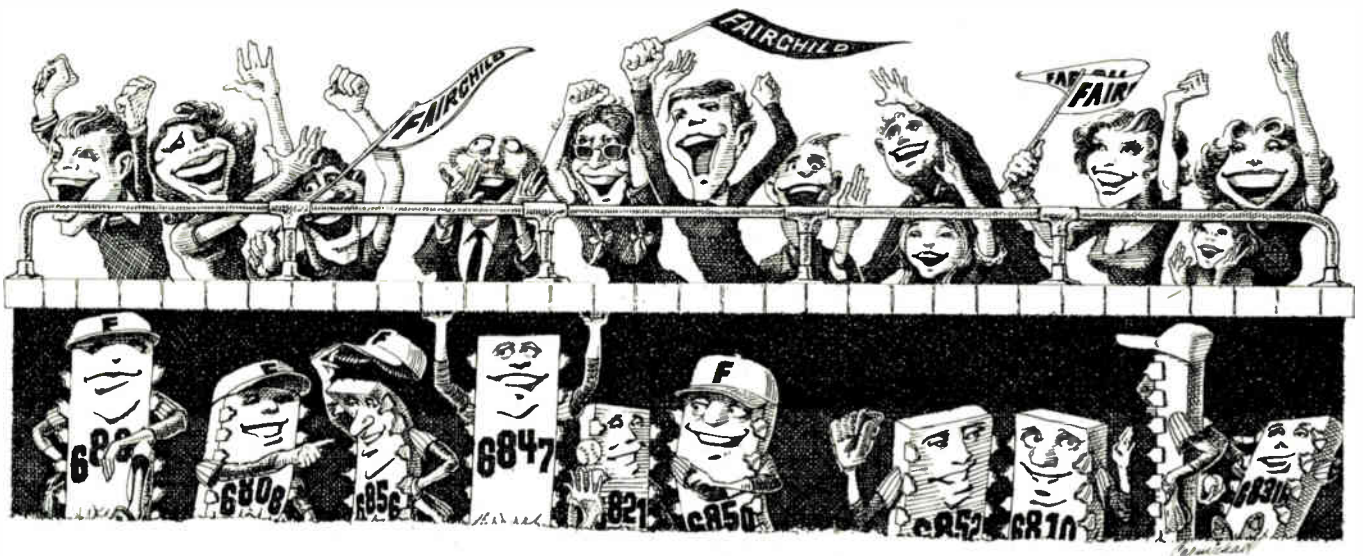
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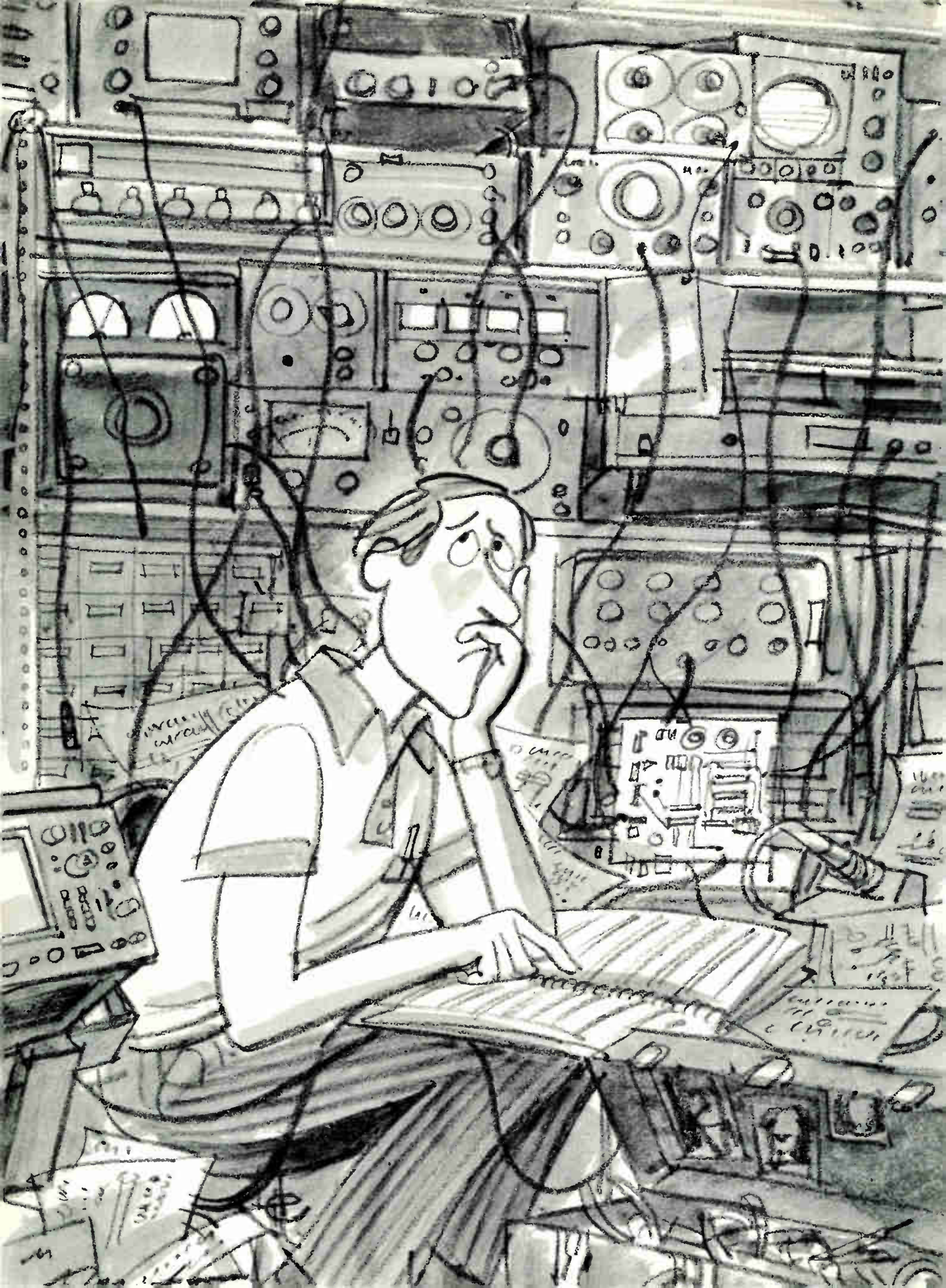
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Circle 62 on reader service card

Carter to reject Industry pleads for tax relief

President Carter's plan to spur industrial innovation may be unveiled by early October. The outlines of the strategy have been shaped and the final decisions concern just what and how much a tight budget will permit the White House to propose. Presidential advisers say that the package will deal with **research funding, regulatory policies, patent reform stimulation of small business, and easier access to Government information** on U. S. and foreign technologies.

Nevertheless, the indications are that most of the tax incentives advocated by industry advisory groups may go by the board. Some 30 agencies have also helped formulate the plan and one—the Treasury Department—has strongly opposed measures that would reduce its revenues. Since the Office of Management and Budget also opposes any large new spending programs, any new efforts probably will have to be financed from existing agency budgets. Even with these limitations, White House planners insist things can still be done to stimulate private innovation (see p. 24).

U. S. races to clear Japanese color TV dumping backlog . . .

The U. S. Customs Service has set up a special task force to liquidate on a crash basis the huge, seven-year-old backlog of unassessed dumping duties on imported Japanese color television sets. The task force is racing to complete the job before a tougher new antidumping law becomes effective on Jan. 1, 1980.

The Customs Service is expected to make a final assessment by the end of September of an estimated \$46 million worth of dumping duties that became due between April 1972 and June 1973. That should clear the way for assessing duties on color TV sets imported from Japan since then. The service estimated early last year that those duties totaled more than \$400 million. **The Committee to Preserve American Color Television (Compact), an industry-labor group, estimated that those duties now total \$600 million.** Duties would be assessed against U. S. importers of Japanese sets, including subsidiaries of Japanese television manufacturers.

Japanese color TV makers' concern over the threat of massive antidumping duties has been a major factor in the substantial investment by the big five Japanese consumer electronics companies in color TV production capacity in the U. S. This has led to a decline in imports of Japanese sets from 1,842,196 units, for the year July 1977 to July 1978, to 1,238,689 units in the following year.

. . . as controversy bolls over size of final bill

The Customs decision is bound to be fiercely controversial no matter which way it goes. Compact charges that the Treasury Department, under political pressure from the Japanese government and the State Department, is seeking to scale down the duties drastically on technical grounds. **Compact is suing the Treasury to force it to collect \$600 million from the importers.** The organization has strong support in Congress, notably from Rep. Charles A. Vanik (D., Ohio), chairman of the trade subcommittee of the House Ways and Means Committee. If the Customs Service does present a radically reduced dumping bill to TV importers, that could raise a political storm on Capital Hill where the Treasury and its Customs Service have come under heavy criticism for their delays in assessing duties on Japanese TVs. But if the service assesses duties on the order of magnitude of its original \$600 million estimate, it would seriously strain U. S. relations with Japan.

FCC appears likely to clear way for Xten network

The Federal Communications Commission has hinted that it will approve Xerox Corp.'s request to have frequencies in the 10-GHz band allocated for use in digital microwave systems for business communications, which would clear the way for the company's proposed Xten network. In its official notice of proposed rulemaking and inquiry, the FCC asked for industry comments on rules that would pave the way for competitive entry into the new services **"without the need for further proceedings."** It asked for industry comment on a number of technical, structural, and procedural questions by Nov. 14 and reply comments one month later. That could mean a final decision early next year.

Continental Phone to buy half of American Satellite

Continental Telephone Co. is breaking the mold of independent (non-Bell) telephone carriers with its decision to buy a half interest in Fairchild Industries Inc.'s American Satellite Corp., which specializes in AT&T's long-distance network. The move puts the independent, which controls exchanges serving 3 million telephones in 38 states, **in a position to compete with Satellite Business Systems, Xerox, and others** supplying specialized communications services.

In addition to extending Continental's service area for business customers from coast to coast, American Satellite facilities will also give Continental the option of connecting some of its digital exchange switches with digital satellite circuits for long-distance service. "We'll have an alternative if we need it," says Continental chairman Charles Wohlstetter, who hopes to "carve out some special services that others can't offer."

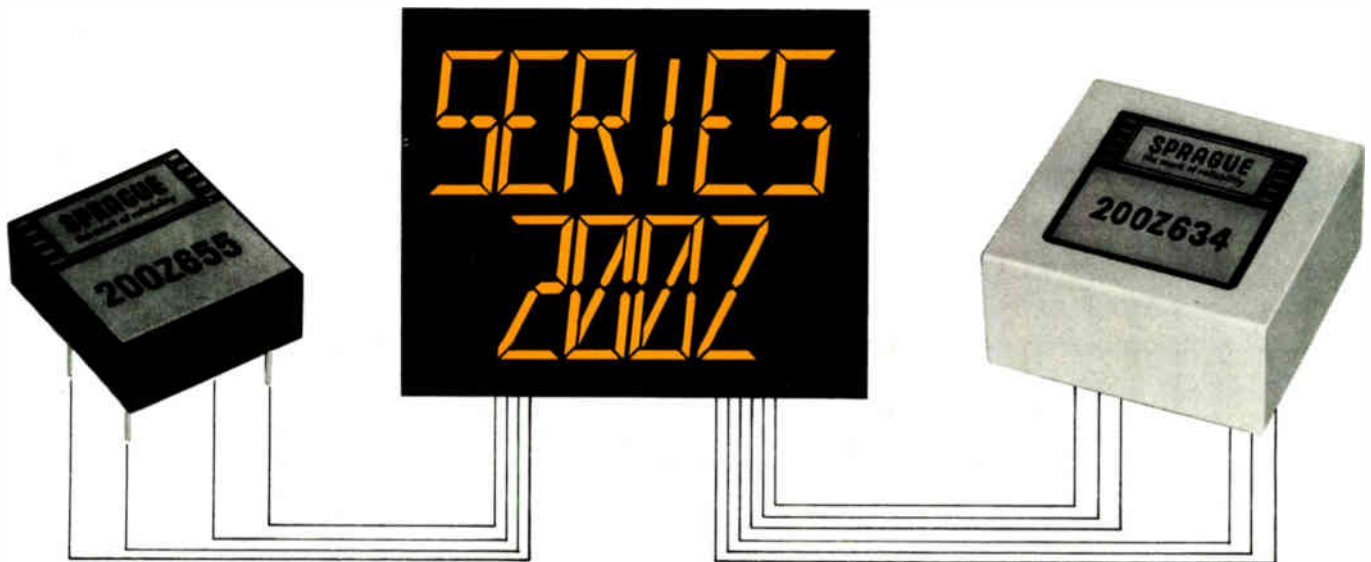
U. S. calls for change in formula dividing phone charges

Though many political observers believe that the chances for significant revision of the Communications Act died when Rep. Lionel Van Deerlin (D., Calif.) withdrew his rewrite [*Electronics*, Aug. 2, p. 88], hope seems to spring eternal at the Commerce Department's National Telecommunications and Information Agency. The agency is calling for legislation to create a board to oversee a **14-year program for changing the way revenues are shared between long-distance telecommunications carriers and local telephone companies.** The complex plan, which calls for a first phase of two years just to establish the boundaries of local phone companies, would provide more Federal jurisdiction over the telephone industry's settlements pool, which divides about \$4 billion per year in long distance revenues between Bell and the independents.

Addenda

Despite the reluctance of both President Carter and the Congress, a major tax bill will probably emerge early next year. And if a diverse coalition of industries gets what it wants—a radical change in laws governing business depreciation of plant and equipment—**benefits for the electronics industries would be less than for other sectors.** The reason: high-technology industries already have short depreciation schedules. . . . Using Federal as well as private funds, research continues to chip away at the cost of photovoltaic solar cells. Now SRI International Inc. of Menlo Park, Calif., says it has developed a simple process **that could produce pure silicon at \$5 to \$7 a kilogram,** compared to today's \$65 to \$70. The Energy Department's goal is electricity at 50 cents or less per peak watt, down from the current \$10.

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VECTOR SCAN LITHOGRAPHY SYSTEM

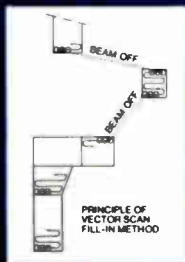
The Best Production EBL You Can Buy

Choosing an electron beam lithography system is a difficult task. Your selection will depend upon your specific requirements; however, throughput, uptime, precision, flexibility and minimum feature size are the most relevant factors in the majority of applications. That's why Philips designed the Beamwriter Lithography System to excel in each of these areas:

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In a production environment, the number of masks, reticles or chips produced per hour determines the cost effectiveness of the equipment. Throughput is critical. Philips' Beamwriter system gives you highest throughput for most applications by using vector scan technology and high dose rates.

Vector Scan



Philips' Beamwriter system is the only commercially available production oriented vector scan EBL. You achieve higher throughput with vector scan than raster scan because the beam wastes no time scanning unnecessary areas. This makes vector scan especially efficient in the production of reticles.

High Dose Rate

The efficient electron optical design of Philips' Beamwriter system gives you an exposure dosage twenty times greater than other commercially available EBL systems. This enhanced dosage enables a faster maximum writing speed and a wider choice of resists.

Uptime

Three main factors affect uptime — reliability, serviceability, and service response:

Reliability

The Beamwriter system's exceptional reliability results from Philips' 30 years experience in building dependable electron microscopes. Offstage drives are mounted in the main working chamber. By eliminating the need for bellows, the Beamwriter eliminates the possibility of downtime due to bellows failure. The stage utilizes ball bearings coated with a molecular layer of lubricant, which eliminates bearing wear. This specially chosen lubricant does not contribute to any column contamination.

Serviceability

Designed for serviceability, the Beamwriter incorporates a lifting jack within the column for quick separation of parts. This gives you access to the X-Y table in 10 minutes. Recalibration is rapid because of the unique assembly configuration of the X-Y table and the electron optics column.

Service Response

Philips has more than 3000 electron microscopes installed around the world with an experienced team of over 250 service engineers to maintain them. No other microscope or EBL manufacturer has a service organization that comes close to this in numbers, experience or dedication.

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Electron Beam productivity requires alignment accuracy. The Philips' Beamwriter system eliminates drift due to thermal effects. All lenses and lens reference power supplies are water cooled. The rigidly-built working chamber utilizes special materials which have low coefficients of thermal expansion. The working chamber is also temperature stabilized. Consequently, the Beamwriter offers you overlay accuracy twice as good as other commercially available systems.

Flexibility

The Beamwriter system is built for direct writing as well as mask making. The unique substrate height sensor, standard in the Beamwriter, enables block by block refocusing of the beam to compensate for wafer distortion. Four backscatter detectors offer optimum alignment on topographical markers.

Minimum Feature Size

The Beamwriter system has a minimum beam diameter 10 times smaller than other commercially available production EBL equipment. Furthermore, vector scanning provides the potential for proximity correction, necessary to achieve narrow geometries. The Beamwriter's variable clock rates capitalize on this potential.

Philips combines 30 years of Electron Optics experience with an intimate knowledge of semiconductor manufacturing to give you the best production EBL available.

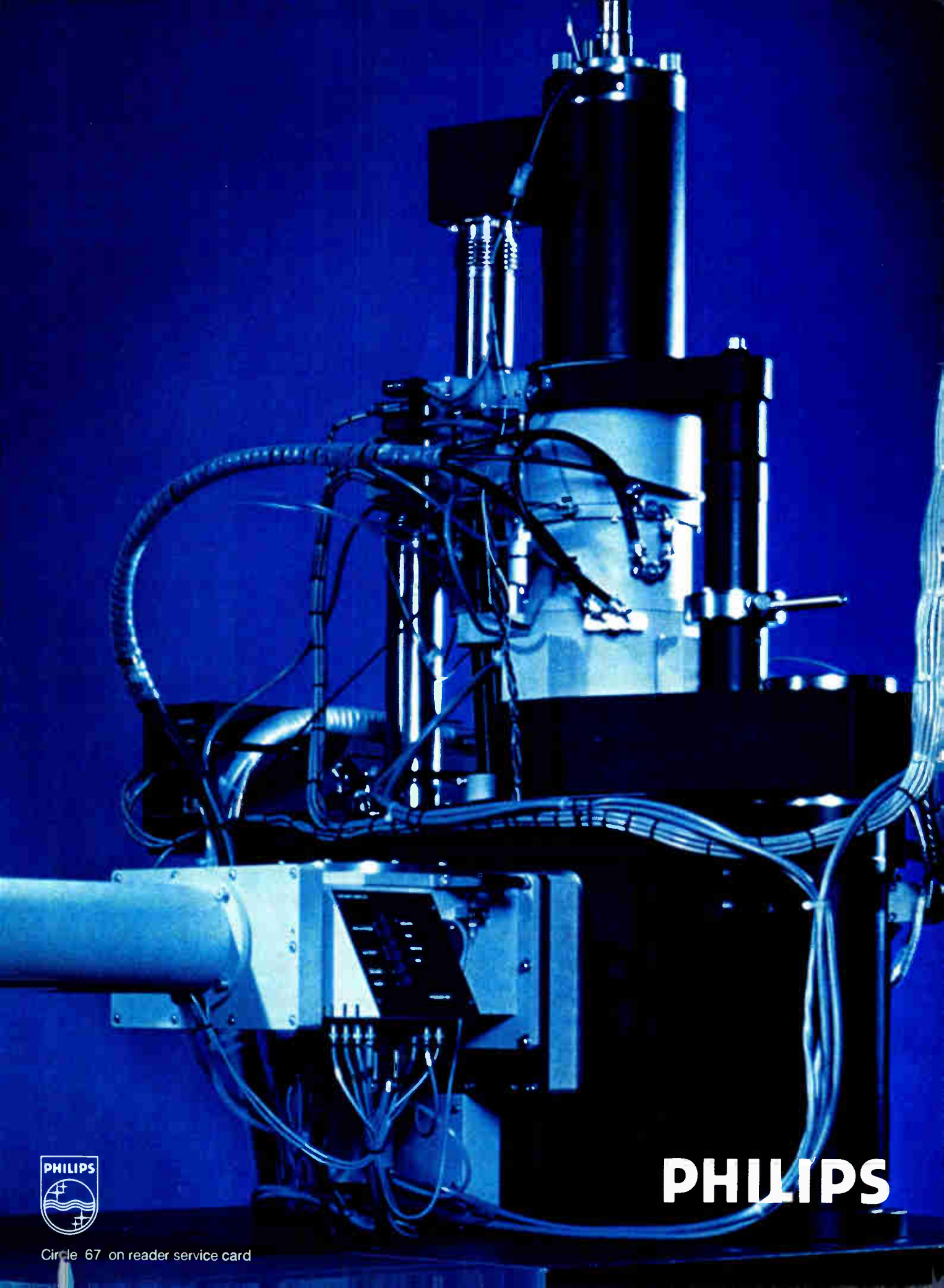
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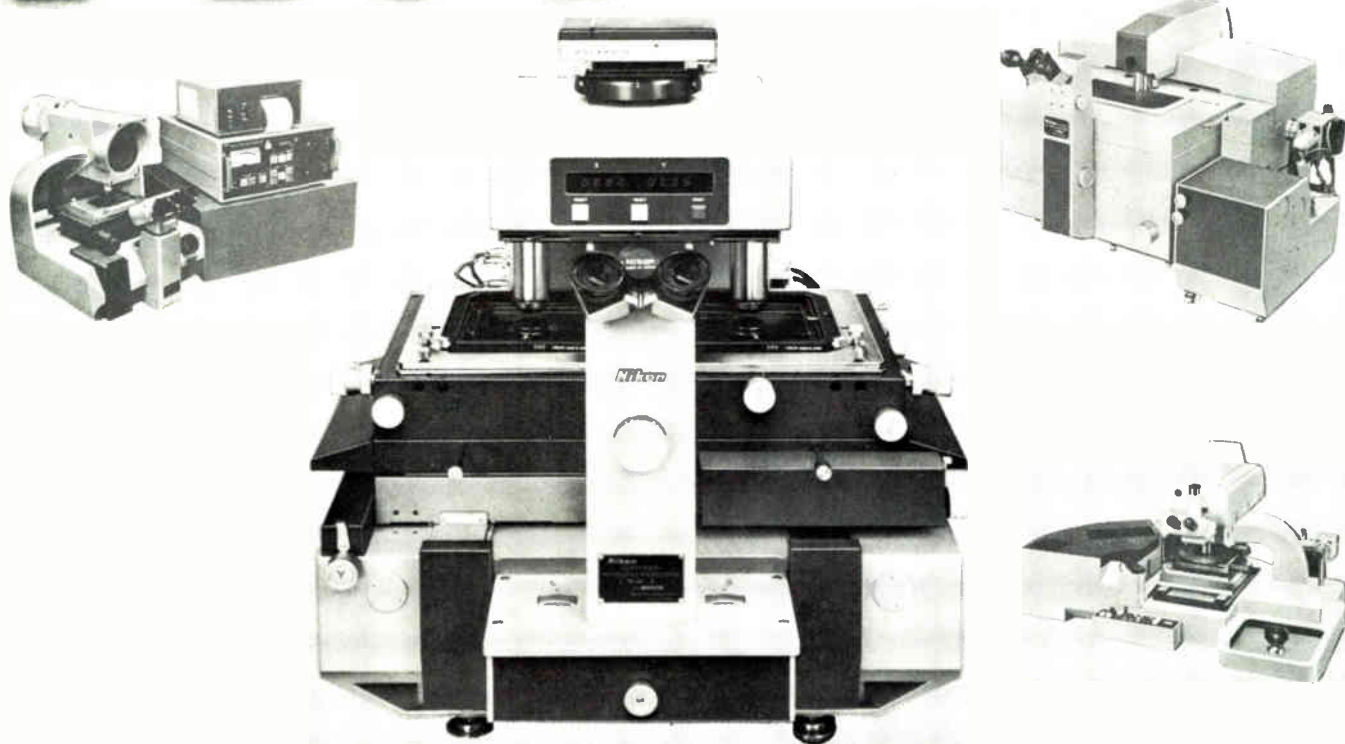
Outside U.S.A.: Mr. G. Janssen, NV Philips Gloeilampenfabrieken, TQ III-2, Eindhoven, The Netherlands, Phone: 040 788 232 ext 83626.



PHILIPS

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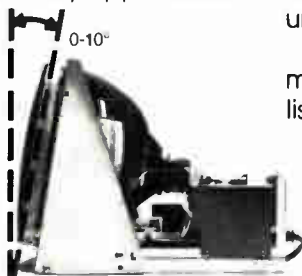
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International newsletter

Sony-Tektronix Introduces versatile 8-lb logic analyzer

A portable logic analyzer from the joint-venture company Sony-Tektronix Corp. will soon be aiding harried microprocessor service engineers around the world. The model 308 features four operating modes: 8-bit parallel timing analysis with sampling rates up to 20 MHz, 8-bit parallel state analysis, serial state analysis for RS-232 communications lines, and signature analysis. **An optional probe permits the instrument to operate with 24-channel triggering.** The small size of 4.6 in. high by 9.3 in. wide by 13.8 in. deep (11.7 by 23.7 by 35.1 cm) and light weight of 8.1 lb (3.7 kg) make this instrument truly portable. But the 4-in. cathode-ray tube limits the amount of data that can be conveniently viewed. Sales of the analyzer, which will cost some \$3,700, will start in Japan at the end of October. U. S. and European sales will start somewhat later.

Siemens develops seven-color ink-jet printer

Engineers of the Teletype and Data-Transmission group at Siemens AG in Munich have developed a prototype color ink-jet printer that can produce characters of seven different colors at the rate of 200 per second in both directions across normal paper. The unit consists of the company's older PT80 printer whose single-color ink-jet mechanism has been replaced by a **multinozzle unit for red, green, and yellow ink. Proper mixing of these inks yields the colors blue, magenta, cyan, and black.** Color and mixture data are stored in a floppy-disk memory whose program is derived from the output of a separate color scanner. One of the biggest problems involved, the Siemens engineers say, was developing nonsmearing inks that would stay liquid in the nozzles yet become dry right after they hit the paper. If customer reaction is favorable, the color printer will go into production. It will make possible multicolored graphic representations.

Ferranti IC to fit in future UK telephones

Ferranti Semiconductors Ltd. has delivered working samples of a high-performance integrated-circuit amplifier to the British Post Office for use with electret transducer microphones. The BPO is considering the latter as a **high-performance drop-in replacement for the carbon-granule microphone in almost universal use in telephones today.** Though cheap, the present microphone introduces nonlinear distortion, becomes increasingly noisy with age, and gives a greater output on short lines. The approach favored by the post office's Martlesham Research Centre uses an electret polymer-film membrane that, in a manner analogous to a permanent magnet, retains a charge received during manufacture. Movement of the electret diaphragm changes its capacitance to earth and generates an electromotive force in sympathy with sound waves. But unlike the carbon-granule microphone, the new device needs a microphone amplifier. Ferranti will use its collector diffused-isolation (CDI) process to make the device.

Sharp colors the picture within the TV picture

Sharp Corp. will show a 26-inch color TV with a color picture within a picture at the Japan Electronics Show starting Oct. 5 in Osaka. The firm will do market research during the show to decide which size TV it should add this feature to for production purposes. For storage of the inset picture, Sharp uses **the same 3,712-element bucket-brigade devices from Intermetall GmbH in West Germany that it uses in its black-and-white picture-within-a-picture TVs now on the market.** The major difference is that the color set requires a total of six devices, one for each color during both the even and the odd fields.

Telefunken building solar generator that puts out 4 kW

For the U. S.'s National Aeronautics and Space Administration Space-Telescope satellite, AEG-Telefunken will supply a solar generator whose 4-kw output "makes it the **highest-powered ever developed for a satellite,**" the Frankfurt-based firm says. The generator consists of four flexible panels that are rolled up during launching and unroll after the satellite has reached its orbital position. The panels have a total area of 58 square meters, about 640 square feet, and contain more than 50,000 silicon solar cells. Their high output is needed to meet the big power demand by the data-recording and -transmission equipment, as well as by the attitude-control system on the 10-ton, 43-foot-long space telescope. Scheduled for a 1983 launching, it will observe various celestial bodies.

Car radio tunes itself to one program as transmitters change

NV Philips Gloeilampenfabrieken of the Netherlands and its West German subsidiary, Philips GmbH in Hamburg, have developed a microcomputer-controlled car radio that automatically picks out the optimum frequency for the fm program selected by the driver. Called the MCC—for microcomputer control—auto radio, the set thus overcomes a problem that is particularly annoying to long-distance drivers: the need to retune the radio whenever the car gets outside the range of one fm transmitter and comes within that of another broadcasting the same program. The microcomputer has an electrically alterable read-only memory that stores up to 60 fm frequencies, 10 each per fm program. When a button on the radio is pushed, **the microcomputer looks for the frequency with the strongest signal, switches the set to the new frequency** (unnoticed by the driver), and shows it on a liquid-crystal display. To go to market next spring, the MCC radio will cost about \$500.

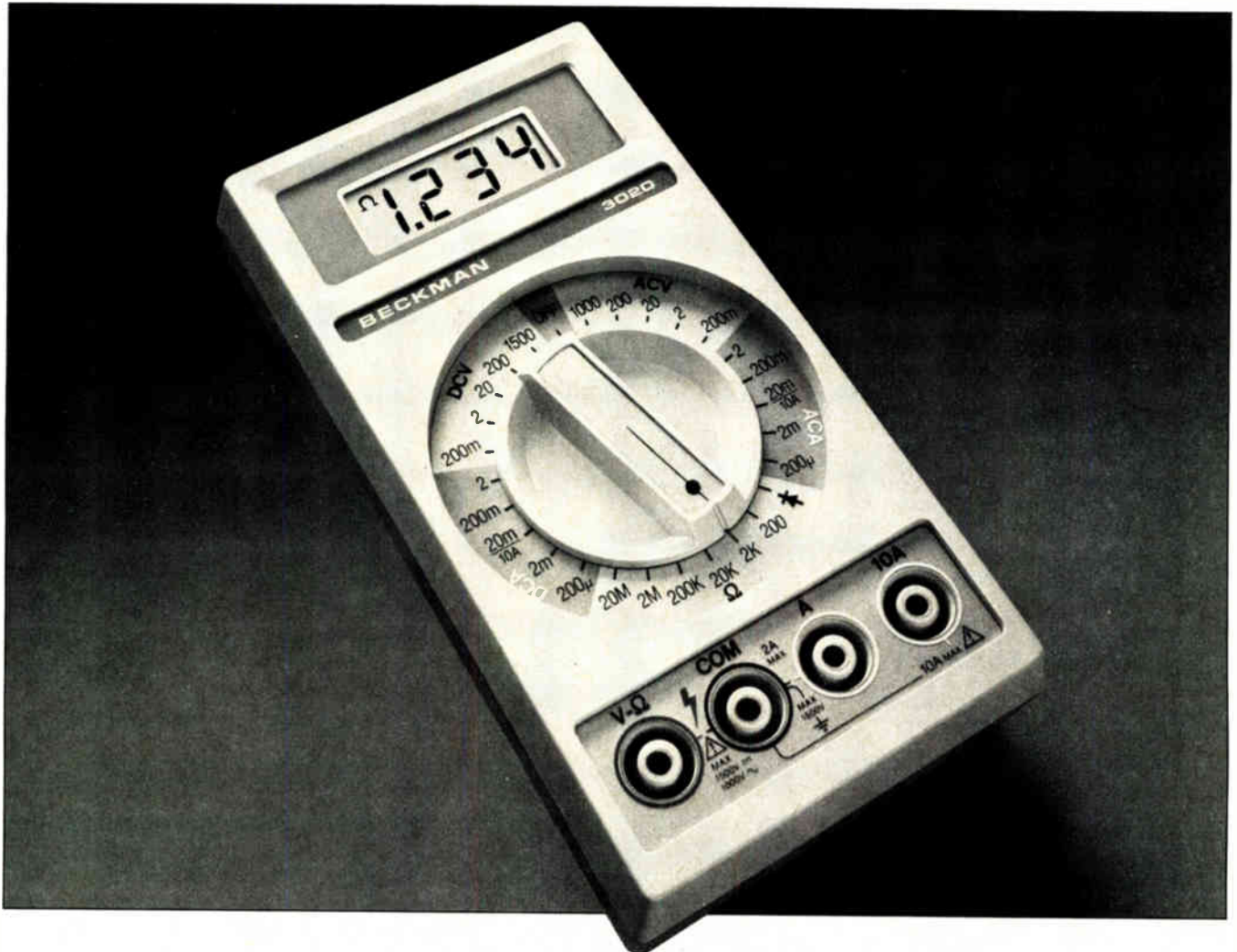
UK's Sinclair splits up, reverts partly to private ownership

Following losses in its last financial year of \$3.67 million, Sinclair Radionics Ltd. in St. Ives, Huntingdon, is to be dismembered by its principal shareholder, Britain's National Enterprise Board. The Instruments group has been sold to the NEB, while rights to Sinclair's present generation of pocket televisions—the \$200 2-inch Microvision—have been sold to Binatone International Ltd. in Wembley. Meanwhile, the NEB, the National Research and Development Corp. (NRDC), which helped fund the development of Sinclair's thin-screen TV [*Electronics*, July 19, p. 67], and Sinclair are currently negotiating with a UK company—possibly Philips subsidiary Mullard Ltd.—with the experience necessary to make such units. **Founder-director Clive Sinclair will continue development of the thin-screen TV and other products through his new, wholly owned company, Sinclair Research Ltd.**

French firm plans to profit from microfilm's likely new legal status

The French parliament's expected passage of a bill before year's end giving legal status to microfilm documents should give a much-needed boost to France's minuscule microfilm industry, say the organizers of the eleventh annual International Micrographic Congress, to be held Sept. 24–27 in Paris. Among those hoping to get into the new market is Benson SA, a firm based in the Paris suburb of Creteil. It will be showing its new color computer-output microfilm (COM) device, which it says is only the second such color unit on the world market. The device uses a high-brilliance cathode-ray tube and **a series of three color filters to display, process, and microfilm images with up to 1,024 tints.**

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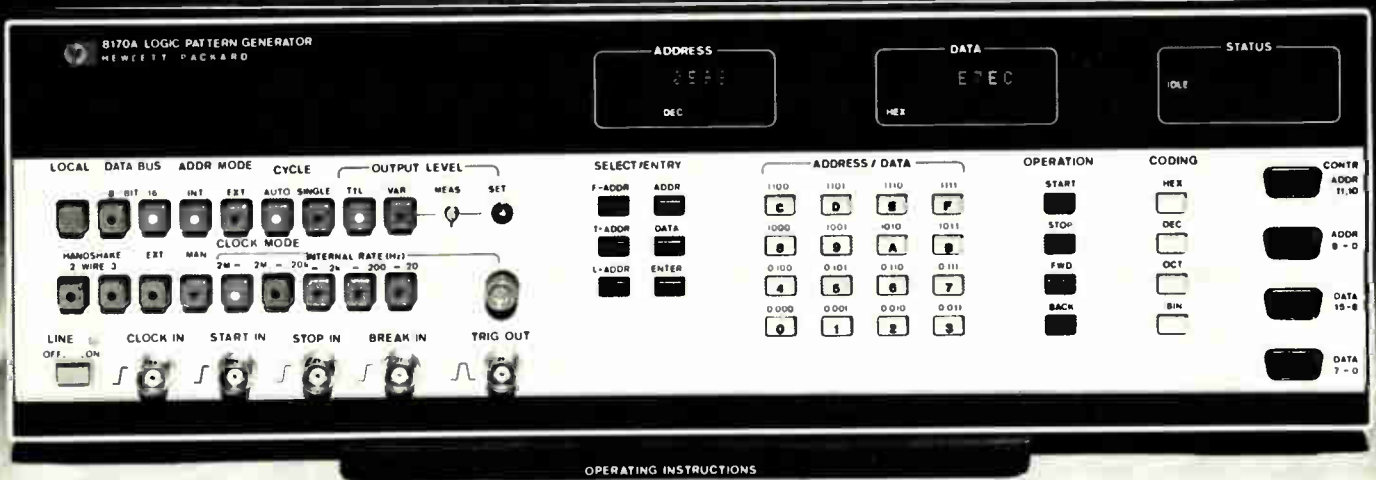
Then the Model RMS 3030 features true RMS ac current and voltage measurement capability, and 0.1% Vdc accuracy, for only \$190.

Whichever model you choose, you get long-term accuracy and reliability, assured through the use of band-gap reference elements, thin-film resistor networks, custom-designed CMOS LSI chips and more.

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Simulation of digitally controlled hardware. By simulating keyboards, tapes, printers or bus-compatible instruments, the 8170A simplifies at-speed functional testing of multi-channel hardware. The 8170A has a large 8K memory (32K optional) and gives you pushbutton selection of either 8 or 16 bit parallel outputs. Internal, manual, or external clocking allows dynamic testing at variable bit rates up to 2 MHz. With simple key strokes, you can start and stop data generation at any desired address, using whichever code you select. And you can step forward or back in single steps to any memory location for rapid debugging.

Bus Stimulation. Custom-built boxes with mechanical switches are no longer adequate for setting bus lines true or false for data simulation. The 8170A can simulate bus-compatible peripherals or instruments at speed for more complete system testing. Three-state outputs let you load the bus or effectively isolate the 8170A from bus activity. And the 8170A will generate data and data-valid signals in accordance with 2 or 3-wire handshake protocol.

Circle 74 on reader service card

ROM Simulation. Because of its external address capability, you can use the 8170A to simulate a ROM. Memory changes are easy to make, either through the front panel or under computer control via the HP-IB.** This means fast and flexible ROM simulation for low development costs.

Big memory, easy access, remote programmability and real-speed sequencing all help simplify functional testing of your digital systems. The price of the 8170A is \$5430* and includes HP-IB and RS 232C interfaces. The optional memory to 32K is \$545.* Ask your local HP field engineer for all the details.

* Domestic U.S.A. price only
** HP's implementation of IEEE Standard 488-1975

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Two bubble boards plug directly into memory systems

by Kevin Smith, London bureau manager

Plessey plans range of units:
first is a 64-kilobyte board;
second is a 2-megabit
two-board unit

With the bubble-memory market ripe for exploitation, Plessey Microsystems Ltd.'s long flirtation with the technology is turning serious. The firm is introducing a 64-kilobyte board using its 64-K chips and will follow up with a 2-megabit board using Rockwell's 256-K chips [*Electronics*, Aug. 30, p. 63].

The Towcester, Northants., company plans a range of such plug-in replacements for semiconductor boards and disk systems because it sees the bubble technology as alien to most system designers. Thus it is capitalizing on its research experience to provide these designers with system-level, ready-to-go products.

Entries. Both the 64-kilobyte PBM 80S and the forthcoming 2-megabit PBM 80M plug directly into the standard Intel Multibus. The 80S is a single-board unit, however, and the 80M puts the bubble chips on one board and the controller circuitry on another. Both designs use TTL small-scale integrated circuits in the control function, but coming along are large-scale ICs for sensing and driving.

The 80S offers a 100-kilobyte-per-second data-transfer rate and comes complete with the input/output circuitry and initializing software to make an operational system. It uses the company's 64-K single-loop bubble-memory chips.

Dwarfed as they are by the forth-

coming 1-megabit bubble chips from Intel and others, the Plessey chips have one big advantage: availability. "Furthermore, we are competitive on a cost-per-bit basis with Intel's board prices despite the smaller chip sizes," says Ken Baker, Plessey's marketing manager for memories. "Because our board takes one slot in an Intel chassis instead of two, we achieve the same packing density."

Prices. The Plessey half-megabit board will cost \$3,010 dollars, and is available within 12 weeks. The Intel 1-megabit chip is available in two kits—one a \$3,900 completely assembled evaluation board with an 8085A controller, the other a \$2,280 prototyping assemblage that includes support chips and is available in 100-piece quantities.

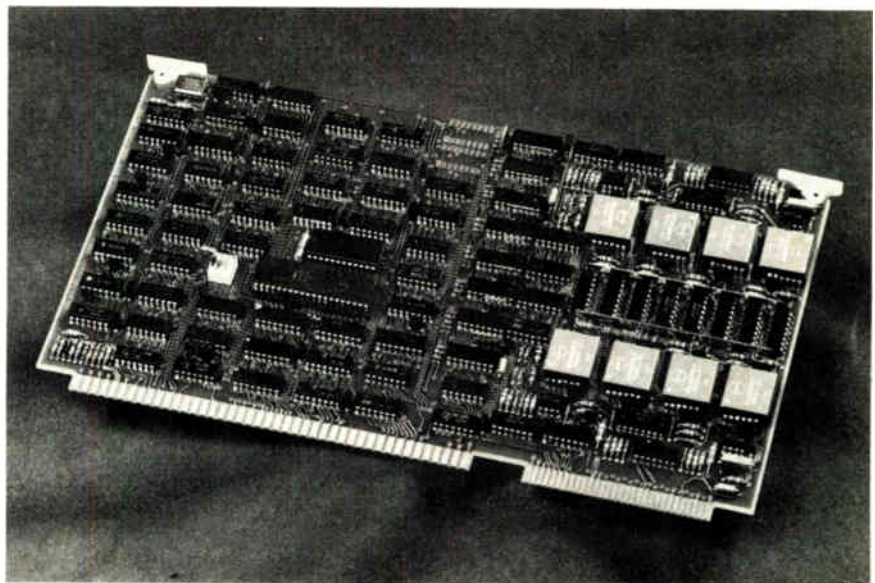
In the first quarter of 1980 will come the 2-megabit board. It will

have the same data-transfer rate and a 7-millisecond access time.

Plessey splits the 80M's memory and controller functions into separate boards for the same reason Rockwell did: more economical large systems. One controller board can govern up to eight memory boards.

As does the smaller board, the 80M will offer a cost-effective, high-reliability system for terminals, portable data-capture systems, and telecommunications computers, says Baker. It will cost \$6,690.

The 2-megabit board is also a harbinger of things to come, for Plessey has decided to follow the Rockwell block-replicate architecture [*Electronics*, March 29, p. 99] rather than its own single-loop design. "We think they have made the best set of design decisions in the number of bits per loop, number of



Single card. The PBM 80S is a 64-kilobyte bubble memory board using Plessey's 64-kilobit single-loop bubbles. The first of a family, it is Multibus-compatible.

bits per device, and degree of redundancy—and in identifying good loops” by storing the information in a PROM, says Peter Newman, head of bubble-memory-device development for the British firm. Within 12 months, he hopes to have a 256-K part using the same 4-micrometer bubble size as in the 64-K chips.

At the board level, too, “there is room for cleverness,” says Newman. Plessey plans to replace TTL control packages on its first two boards with two custom bipolar LSI circuits.

The company already has samples of a quad-sense amplifier with 0.1-millivolt sensitivity, capable of handling what Newman characterizes as “very nasty” wave shapes on the memory-sense lines. The other chip will be a quad write-drive incorporating protection circuitry for the bubble-generating conductive track that is so narrow that it can be very readily burnt out. Plessey’s Caswell Research Center is developing both ICs in the company’s high-performance Process III.

Custom bubble work also under way

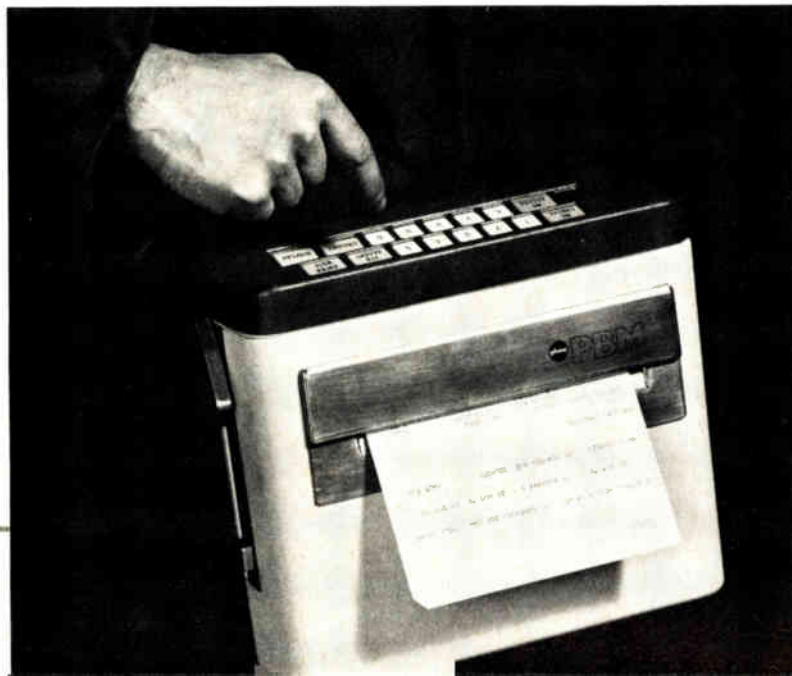
Plessey has more plans up its bubble-board sleeve than just standard products, for it also intends to seek out custom work. A case in point is the PBM 500 portable billing machine. The machine’s custom bubble-memory module is more compact and uses less power than do semiconductor memories and cassette tape transports. Another advantage over semiconductor solutions is that it needs no refresh circuitry.

Incorporating a Z80 microprocessor and a specially developed thermal printer, the PBM 500 allows a meter reader to issue an electricity bill on the spot, cutting postal costs and delays. Before a day’s calls, data such as the last meter readings at the households to be visited are loaded into the 64-kilobyte bubble memory. They can be called up on the machine’s display.

Plessey developed the unit and its support equipment in collaboration with the nation’s power authorities, who plan to buy substantial quantities. Other applications could be all the public services on the railways, or in stock control, or in any application calling for nonvolatile high-density data storage and very low power consumption, says Plessey’s Ken Baker.

Also under development is a replacement for disk memories used in military and severe-environment applications. The PBM 90M will use the 256-K Rockwell chips in a rugged 8-megabit package. As many as eight of these megabyte modules may be stacked and easily interfaced to most computer buses via the microcomputer-based controller cards and a simple personality card. The 90M is destined for the British Army’s Project Wavel, a battlefield communication and surveillance system, with production to start in the third quarter of 1981.

-K. S.



West Germany

VCR unit records, plays longitudinally

Despite the plethora of video cassette recorders of different formats, BASF AG is launching another one with some novel technical twists. The company is confident that these advances will help the LVR (longitudinal video recording) system grab a good chunk of the VCR market.

Already the Ludwigshafen-based company can point to the interest other firms have in the technology. It says the LVR color recorder’s advantages include simple mechanical design, high sound quality, and easy track access.

One head. The use of a single non-rotating audio-video magnetic head makes for a simple mechanical design and facilitates maintenance—the head can be replaced very easily. The system’s sound quality compares favorably to that of other VCRs, because the tape moves past the head at the high speed of 4 meters per second.

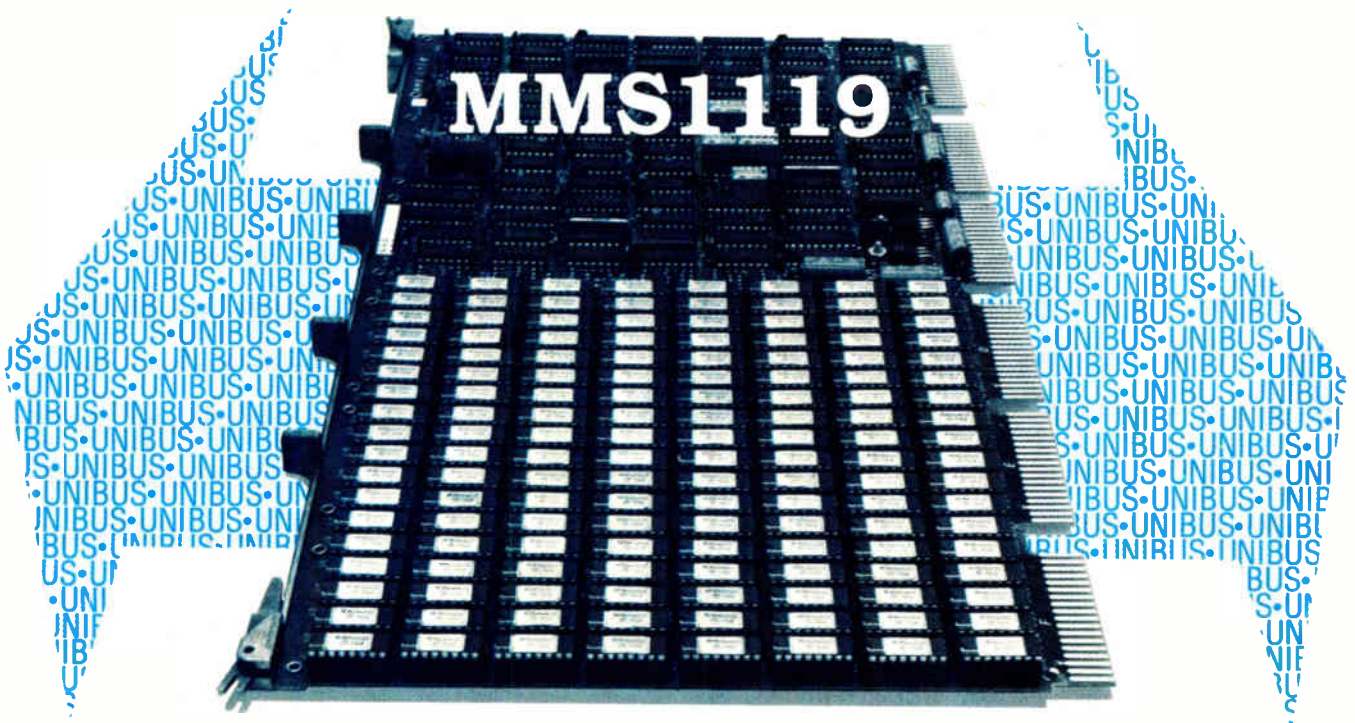
As its name implies, the LVR system records along longitudinal tracks running parallel with the tape edge. This concept radically departs from that of other video recorders, which use helical scan techniques requiring two rotating heads and are mechanically more complicated.

With its fixed head, the BASF system resembles Toshiba Corp.’s VCR equipment now in development [*Electronics*, March 15, 1979, p. 72]. But there the similarity ends.

Instead of using a continuous tape as does the one-hour Toshiba design, the LVR system employs a tape of finite length. Containing 72 tracks, each 100 micrometers wide, the 600-m tape runs through the system in 2½ minutes.

When the tape gets to one end, it reverses direction and the head switches to the next track. The switching process takes only 100 milliseconds—so fast that the eye or the ear cannot detect the reversal. The thin, tightly wound tape pro-

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It's organized as 512K words by 18 bits, with 22 address lines. On-board parity is standard, with no degrading effect on speed, and may be omitted.

The MMS1119 is also available in 64K, 96K and 128K word configurations, which are function-for-function and pin-for-pin compatible with the DEC* MS11-L series of PC boards. These smaller capacity boards use Motorola's MCM4116 16K RAM and are Modified UNIBUS compatible.

Typical access time of the MMS1119 is 300 ns, and cycle time is 420 ns. Stored data is automatically refreshed every 2 ms, with a single refresh cycle initiated every 16 μ s.

The one-megabyte MMS1119 uses less power than the comparable 128K-word board using three-supply 16K RAMs. Motorola's fully-populated MMS1119 is only a single UNIBUS load.

The MMS1119 is built with a standard HEX slot PC card, compatible with PDP-11 backplane connectors and card cages. All boards are given extended burn-in at 70°C, and a one-year limited warranty is standard.

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Evaluation units of the MMS1119 are now available. Production quantities are available in 30 days ARO (16K RAM versions). The 1119 is priced to save you money, and there are no delivery problems.

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MOTOROLA INC.

Cassette size shrinks

The new BASF video recorder uses a chromium-dioxide tape, 8 millimeters wide and 8.5 micrometers thick, housed in a cassette claimed to be the world's smallest for video recording. It measures 114 by 106 by 17 mm.

The cassette opens automatically after it is loaded. The capstan then pulls the tape leader through a channel onto the take-up reel, which winds the tape so tightly that any slippage during winding or unwinding is avoided. The tight winding, thin tape, and absence of a take-up reel in the cassette account for its small size.

-J. G.



vides three hours of playing time.

The simplicity of system design permits quick selection of specific tracks and thus ready access to any part of the recording, BASF says. For access to a certain track, the user simply pushes the appropriate number keys (such as track 12 or 37). Within seconds, the head positions itself over the desired track. With this access scheme, it is not necessary to play the tape back and forth until the desired scene is found.

Camera. The portable recorder can be used with a \$1,350 color TV camera. Weighing only 5 kilograms, the recorder is either line- or battery-powered. For the recorder-camera combination the battery provides enough power for up to 30 minutes' worth of program.

The LVR system has a 3-megahertz bandwidth and a video signal-to-noise ratio of better than 42 decibels. Sporting two stereo sound channels, the system boasts of a 40-hertz-to-12.5-kilohertz audio fre-

quency range, with a signal-to-noise ratio of 56 dB, providing relatively good sound quality. Wow and flutter is only 0.01%.

Room. Despite the well-established competing units, there is still plenty of room for the LVR, the company says. "The market is only at its beginning," a BASF spokesman says, pointing out that of Western Europe's 100 million-odd households only half a million had a VCR as of the end of last year. "So it's not too late to join the action."

Developed at the firm's American subsidiary, BASF Video Corp. in Newport Beach, Calif., the LVR system will go to market in Europe and the U. S. in mid-1980, selling for roughly \$1,100 in Western Europe. Production will start at BASF's U. S. facilities early next year. Chicago-based Bell & Howell Corp. has an option on the system, and the Austrian audio equipment firm, Eumig, is said to be interested in it.

-John Gosch

Japan

Transistor ballast cuts power loss

The conventional ballast for a fluorescent light is a combination of transformer, inductor, and capacitor—as low-cost and low-loss a circuit as might seem possible. Yet Toshiba Electric Equipment Corp. in Japan expects to be able soon to make an electronic device that will sell for less, have lower power loss, and perform even better.

Already the Tokyo subsidiary of Toshiba Corp. has ballasts for single and dual 40- and 110-watt fixtures that cost only 20% more than conventional ballasts. Their increased efficiency should pay back that premium in perhaps three years, given rising prices of materials and electrical power worldwide.

Inverter. Key to the new design is an inverter circuit with low power loss, which permits use of inexpensive transistors. The lack of suitable inexpensive power transistors capable of operating at 100-to-200-volt line voltages is a problem that has prevented ballasts based on transistor inverters from spreading beyond battery-operated uses in vehicles and emergency lights.

In fact, say Toshiba engineers, their design with an unfiltered power supply and a push-pull inverter circuit solves other problems. Standard power supplies with capacitance filters have a low power factor of 50% to 60%, and filter capacitor life usually is shorter than required for a ballast.

Also, the ferrite-core choke (L in the figure) has a high impedance at the oscillation frequency of 30 kilohertz. Thus it helps eliminate the radio-frequency noise coupled to power lines, interference that can be costly to reduce in something other than a conventional ballast.

The choke also prevents the current to the transistor inverter from changing at the 30-kHz inverter frequency. Therefore an almost constant current is switched between

SCIENCE/SCOPE

Major developments toward an optical filter that can be tuned electronically to specific wavelengths of light have been reported by Hughes scientists. The device is tuned by a microprocessor that varies the electric field distribution onto an electro-optic crystal. One filter with a lithium-tantalate crystal has been operated across the visible light spectrum from deep blue to deep red. Another has been tuned into the infrared portion of the spectrum. The device promises to find important uses in pollution monitoring, multispectral imaging, and monitoring color consistency in a wide range of commercial products.

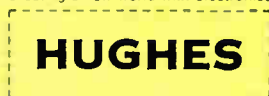
Using digital techniques to perform image processing tasks like scan conversion and information storage, a new microprocessor-controlled display system is finding a wealth of applications from medical diagnoses to non-destructive testing. The system, called the Hughes Anaram 80™ digital signal processor, is designed to create images with the natural look of analog displays while providing the data-handling benefits of digital techniques. The system can display 60 images per second, freeze one picture for an hour, enhance obscured detail, and display four pictures simultaneously for comparative analysis. Uses include medical ultrasonography, X-rays, radar, graphics terminals, and image transmission.

The way in which the brain processes visual information has been used to develop a set of rules to portray how combat pilots locate ground targets. The concept, which draws on years of research involving realistic simulations, was created by Hughes to improve equipment, procedures, and training. It divides the pilot's search into three stages -- an orientation, a preliminary look, and an examination of likely targets. Each step, the pilot makes decisions based on what he sees or expects to see. Because the concept follows the pilot's thinking, engineers can determine which stage of the target acquisition process is most difficult, and how it might be simplified by the design of more efficient systems.

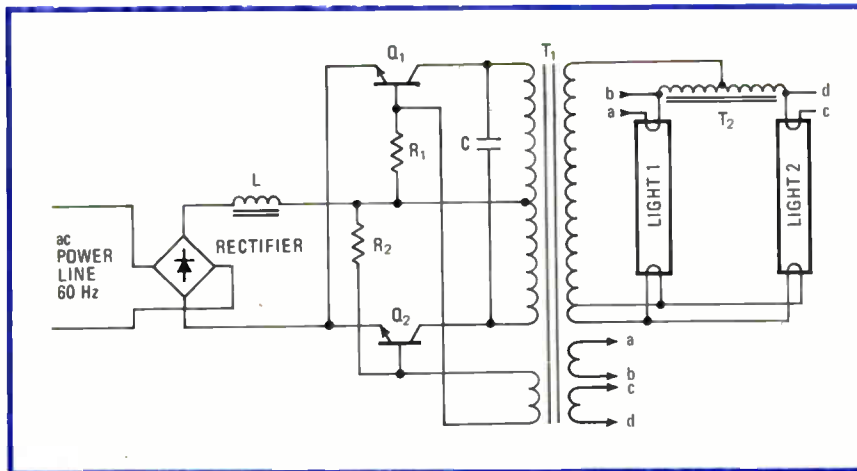
Hughes is seeking engineers to develop advanced systems and components for the following satellites: GOES D, E, and F for NASA; Anik C for Canada; GMS II for Japan; LEASAT for the U.S. Navy; and SBS, the next-generation domestic system. Fields with immediate openings include advanced communications, scientific and engineering programming, systems test & evaluation, microwave & RF design, structural design, spacecraft stress analysis, power systems design, data processing systems, control electronics computers, operating systems, and network systems. Please send your resume to T.W. Royston, Dept. SE109, Hughes Space & Communications Group, P.O. Box 92919, Los Angeles, CA 90009.

Two weapon-locating radars have achieved significant cost savings by equipping them with a computer using current microprocessor and memory technologies. The AN/TPQ-36 mortar-locating radar and the AN/TPQ-37 artillery-locating radar, in production at Hughes, are designed to track enemy shells in flight and determine their origins in an instant. Though the original computer easily met most requirements, Hughes developed a new one that would be more effective and cost less to build and maintain, while still being compatible with existing hardware. Estimated savings over the life of the program are \$28.7 million to the Army.

Creating a new world with electronics



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Efficient. Ballast for fluorescent lights is based on an inverter circuit that can use inexpensive high-voltage transistors. Low inverter power loss increases efficiency in light fixtures.

the two transistors, and the current through them is trapezoidal, rather than having a high peak. Elimination of high peak currents keeps transistor collector-to-emitter saturation voltage low.

Furthermore, collector current in the conducting transistor is commutated when collector-to-emitter voltage is lowest, keeping transient switching losses low. Thus the Toshiba design minimizes the two major sources of transistor dissipation and also minimizes current requirements, making it possible to use inexpensive high-voltage transistors.

Saving. Total ballast power loss is 8 w, compared with 12 w in the typical conventional ballast. Also, the output waveform of the new ballasts enables the lamps to operate more efficiently, so that each provides the same light output at 2 w less input. So there is at least an 8-w saving, and the power factor of better than 95% is superior to that of conventional ballasts.

Toshiba supplies fixtures using high-efficiency lamps, which need only a 35-w input from the new ballasts for the same light output. Thus power input is only 78 w, a savings of 8 to 14 w over conventional fixtures.

The high operating frequency yields two performance advantages. It eliminates the flicker often seen as the ends of lamps with conventional ballasts interchange anode and cathode functions at the power-line

frequency. It also eliminates the hum often heard from a ballast with loose laminations or coils.

Steady. Moreover, fixtures with the new ballasts deliver more light during both undervoltage and overvoltage, yet power drawn from the line is lower during the latter. The new ballasts also are insensitive to power-line frequency—advantageous when operating with poor frequency regulation, as with emergency power supplies.

In Japan, this feature means that the same ballast can be used with either the 50- or the 60-hertz line frequency used. The design of the balancing coil permits operation with only one lamp when the other is burned out or when a savings in energy is desired.

The new ballast also weighs only 0.5 kilogram, as against 1.4 kg for a conventional unit—an indication of its materials savings. In fact, Toshiba expects that the premium cost of its fixture will be wiped out in a few years as the cost of the electronic components and of assembly fall while the iron and copper in the conventional ballast continue to rise rapidly.

The company also points to side benefits of the lighter weight, such as reduced transportation and construction costs. Also, the lower power should mean that, in large buildings, wires of smaller diameters and smaller transformers can be used.

-Charles Cohen.

West Germany

Cordless phone uses infrared beams

Infrared beams, rather than the traditional radio-frequency link, transmit voice signals in a cordless telephone from Siemens AG. The West German firm is showing a prototype at the Third World Telecommunication Exhibition in Geneva Sept. 20-26.

Wireless communication is between the portable handset and a wall-mounted device from which the signals go into the telephone network. Two IR channels are used, one on which the handset transmits and one on which it receives. The IR transmitting diodes and receiving photodiodes are off-the-shelf Siemens components, with the voice signals pulse-phase modulated onto a 9-kilohertz carrier that in turn modulates the IR beams.

There need be no line-of-sight IR link between the handset and wall device for good communications, because the beams' reflections off the walls serve very well. The receiving diodes' sensitivity is such that the phone is fully effective in rooms as large as 1,100 square feet.

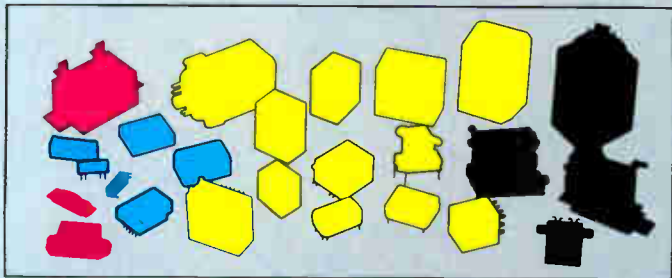
A 9-volt battery drives the handset, delivering enough power to permit a phone call lasting several hours. The battery recharges when the handset is returned to its cradle.

Controls. Pushbuttons on the set allow conversations with a secretary in an outer room and remote activation of a loudspeaker built into the wall device. In future versions, the cordless handset may well have pushbuttons for dialing numbers, says Siegfried Schön, head of the team at Siemens' Munich-based communications division, which is developing the set.

While the IR phone does not have the range of an rf unit, it is more compact and uses less power. Furthermore, use of IR beams needs no official approval. At least initially, it will be more expensive than a wired phone.

-John Gosch

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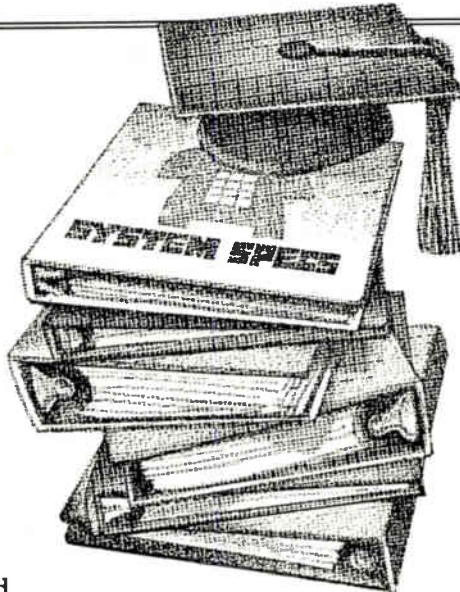
Per-channel PCM codecs and their associated filters are among the first analog LSI devices to be produced in volume.

From a testing standpoint, they differ from most other "new" LSI devices in that the standards for quality and compatibility of codecs and filters are already well established.

The specifications are spelled out in detail in the D3 and Digital Channel Bank Compatibility Specifications and those recommended by the International Telegraph and Telephone Consultative Committee (CCITT). These present a range of ac tests ensuring that the devices will function properly in a telecommunications system.

Not that having established specifications makes the testing job any easier. The standards are rigid, calling for a sizable number of complex tests on devices that operate at their theoretical limits.

The testing situation is further complicated by the need for high throughput in a production environment, the increasing need for detailed device characterization, and the existence of both μ -255 and A-Law devices.



Moreover, packaging combinations for the encoders, decoders, and filters are becoming increasingly varied, with all three elements destined to appear on a single chip in the near future.

For those reasons, Teradyne has developed its Telecommunications Test Package for use on the new A300 family of analog LSI test systems.

Now a device manufacturer or user can perform fast, thorough testing to the industry standards on μ -255 and A-Law encoders, decoders, and filters. Individually or in any combination, even when they are all packaged on one chip.

The Package performs both ac and dc tests, so it satisfies the industry needs for such ac testing as gain tracking, frequency response, and signal to total distortion, as well as providing

valuable characterization information for analyzing device design.

The Package can generate programmable PCM digital code for decoders and convert the code to the analog domain for encoders. It also provides programmable digital control logic to eliminate the need for customized logic for each device type. And its bit rate range well exceeds the requirements of today's devices.

Such thoroughness in testing was once assumed to require too much time — 30 to 60 seconds. But the Teradyne Telecommunications Test Package cuts test time to just a few seconds, meaning that high throughput *and* complete testing are now both possible.

The Teradyne Telecommunications Test Package is designed for use on the new A300 Analog LSI Test Systems, and is adaptable to the hundreds of J273 Linear Test Systems already in the field.

For more information, write Teradyne, 183 Essex Street, Boston, MA 02111.

TERADYNE

Nations gird for spectrum fight

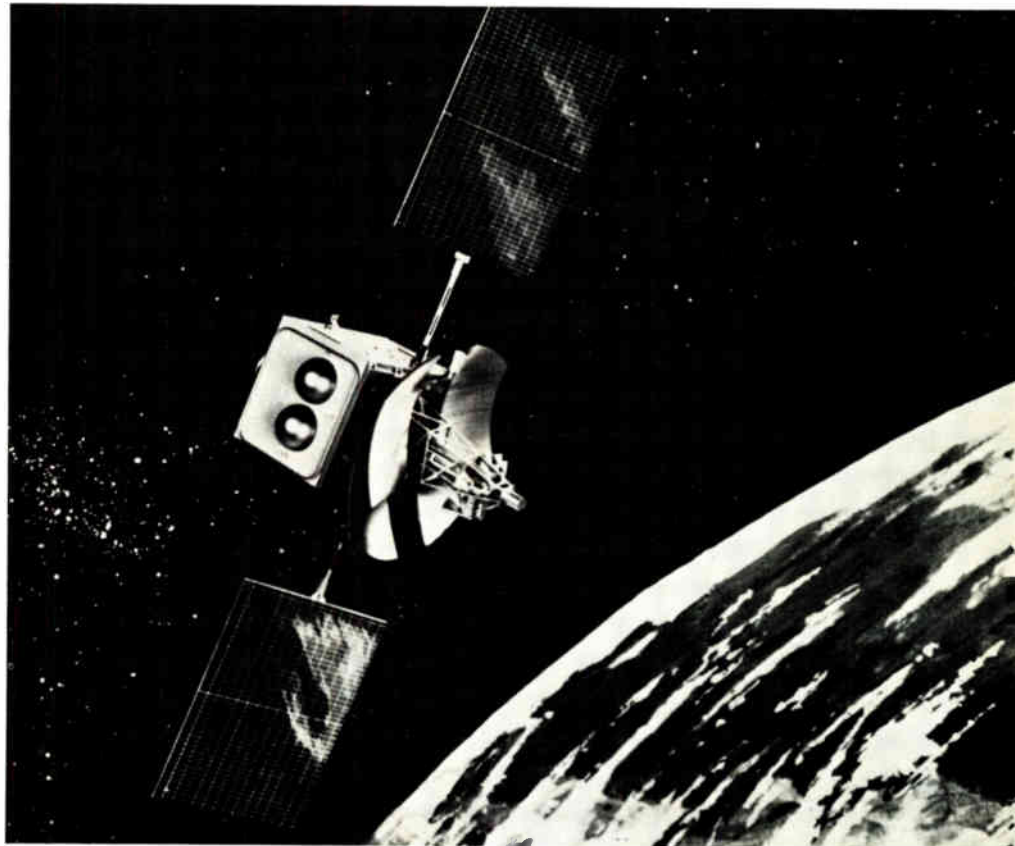
Less developed countries serve notice that they want larger slice of the frequency pie, as well as more voice in allocation decisions

by Kenneth Dreyfack, Paris bureau

On Sept. 24, delegates to the first full-scale World Administrative Radio Conference (WARC) in 20 years will gather in Geneva for 10 weeks of debate that could shake the communications world. They will plow through 4,000 pages of proposals as they set international communications allocations through the year 2000, and the less developed nations have served notice that they want a larger share of the frequency spectrum as well as a bigger role in the decision-making process.

At first glance, the preconference posturing by the world's less developed countries seems to be little more than rhetoric. After all, what difference does it make whether Togo has down-link frequencies allotted for a geostationary orbital communications satellite or if radio astronomers in Laos interfere with local amateur radio in the 6-meter (50-megahertz) band? But while some of the talk in the Third World of a "new information order" undoubtedly contains a fair share of empty words, those nations do have some very real problems to lay before WARC.

Oddly enough, the massing of forces is happening not along East-West battle lines, but North-South ones. On one side are the industrialized nations, socialist and capitalist—members of the "gentlemen's club" that has been deciding policy since the beginning of the century for the International Telegraph Union, now a United Nations body. On the other side are the less developed nations, striving for a greater role in ITU decision making and frequency allocations. Since those countries hold a clear majority in the



Bird problems. Communications satellites and the question of up links and down links will be the subject of debate at WARC. Shown is artist's concept of RCA's proposed Satcom IV.

154-member body under the one-nation, one-vote system, they have some weight to throw around. Of course, should they refuse to listen to what the larger nations define as reason, the "gentlemen" can pick up all their marbles and play among themselves somewhere else. However, both sides are hoping to avoid such a confrontation.

To illustrate the obstacles that must be hurdled in trying to reconcile the needs of the technology haves and have-nots, consider alloca-

tion in the 3-to-30-MHz band. The band is now used mostly for fixed point-to-point communications, with sectors also set aside for amateur radio, international shortwave broadcasting, and air and marine mobile communications. In accordance with existing allocations (decided, incidentally, without much input from the Third World), the less developed nations make much use of point-to-point high-frequency bands for phone communications and radio broadcasting. The technol-

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Probing the news

ogy involved is relatively cheap and straightforward. But now the developed countries want, in the eyes of the opposition, to change the rules in the middle of the game.

Called waste. Given the long-distance capabilities of high-frequency communications, the developed countries argue, it is a waste to allocate it for point-to-point communications especially in the light of satellite and microwave technology. They propose cutting back on the antiquated point-to-point allocations to make more room for mobile communications. Significantly, while some of the mobile high-frequency applications envisioned are civilian, many are military, making the problem much more sensitive than it might otherwise be.

At the same time, the developed countries are pushing for more international shortwave broadcasting channels in the high-frequency band and suggest that one way to cram them into the allotted frequencies would be to narrow bandwidth through use of single-sideband (SSB) modulation. Says Klaus Olms, a member of the West German post office WARC delegation, "If SSB is to come by the year 2000, we must start pushing for it now."

Some less developed nations oppose the whole idea of expanded international broadcasting, in some cases because governments want to restrict the free flow of information, in others because they see foreign broadcasts, especially from the U. S. and the USSR, as a form of imperialism. Then there is the problem of converting to SSB. Constantly forced to adapt and/or replace their equipment, they feel that they will never narrow the technological gap that makes them dependent on the industrialized world for all of their communications needs.

The Algerian solution. Recognizing the divergence between the two camps, Algeria proposes dividing the 3-to-30-MHz band 70:30. The Algerians, who are likely to play a leadership role within the bloc of less developed countries at the WARC, suggest that developed countries allocate 30% of the band and that

What the U. S. wants at WARC

These are the proposals that the U. S. delegation at WARC will put forward:

- Increase the spectrum allocations for maritime communications.
- Open a new band between 1,615 and 1,860 kilohertz.
- Assign more frequencies to international broadcasting.
- Convert short-wave to single-sideband transmission.
- Permit other services—for example, citizens' band, mobile telephone, and microwave relay—to use the ultrahigh-frequency band. It is now used only for broadcasting.
- Double the spectrum space in the 12-gigahertz band for use in telephone and data distribution.
- Improve the aim of satellite transmitters to cut the number of unwanted transmissions countries at present receive.
- Allow low-cost earth stations for two-way satellite communication.
- Protect frequencies used to monitor weather conditions.

the less developed nations allocate the rest.

In the ultrahigh-frequency band, from 300 MHz to 3 gigahertz, a U. S. proposal to experiment with radiating microwave power down to earth is running into opposition from countries in both camps. The idea is to collect solar energy and change it into electricity in space, then use a microwave beam to get the energy down into the power grid. Some nations are worried about possible environmental dangers, others are concerned that the system could be used as a weapon.

The U. S. and Canada are arguing over the 3-to-30-GHz band, since both use its frequencies for communications satellites in adjacent geostationary orbits. On the issue of up links for broadcasting satellites in the ITU Region 2, North and South America, Canada, and Japan suggest a 14-GHz band, although the Japanese would rather delay any allocation for three or four years, according to Nobukazu Morishima, director of the frequency division of the radio regulatory bureau within the Japanese ministry of posts and telecommunications. Canada proposes a second up link in the 17-GHz band.

Satellite position allocation is another domain where Third World aspirations are running head on into the technological needs of the developed world. Some equatorial nations are claiming the right to air space clear to outer space and propose that satellite users pay for their parking spots. Of course, enforcement would be difficult—satellites are harder to

seize than tuna boats. A proposal from the nonaligned nations suggests dividing the airspace above the equator suitable for geostationary orbital satellites into 154 equal parts, with one part for each ITU member.

Being first. Orbital parking places and frequencies have been allocated until now by the same principle that has governed most ITU decisions—first come, first served—with assignments more or less permanent. The French, who along with several other Western European countries feel it is important to demonstrate good faith to the developing world, suggest a compromise.

The proposal, as explained by René Bletterie, a radiocommunications expert for the French ministry of posts and telecommunications and a member of the French WARC delegation, is to assign frequencies for a maximum of 10 years, the longest lifespan that can be expected for a communications satellite. In this way, at least in theory, developing countries would be assured of allocations when needed.

The question of satellite frequency allocations for less developed nations is just academic, Bletterie insists. Wealthy developing countries, such as those on the Persian Gulf, could buy satellites for their own use and also for poorer friends.

He also sounds a warning. Given their technological superiority, he says, "developed countries could try to dominate the conference through brute force." But while such a strategy might work in the short term, he adds, "it would come back to haunt us in the middle and long term." □

Memories

When half good is good enough

That's when the supply of dynamic RAMs fails to meet the demand from computer makers, who are turning to partial devices

by Wesley R. Iversen, Dallas bureau manager

Even though International Business Machines Corp. has been using partially good semiconductor memory components since the early 1970s, neither their use nor the use of multichip packages has caught on to any extent among other mainframe manufacturers and minicomputer makers. But there may be some changes on the way.

For many computer houses and other large customers for memory these days, the continuing scarcity of available dynamic random-access-memory bits is prompting serious consideration of some previously untried approaches—including the first-ever use of two-chip or multi-

chip packaging schemes as well as the use of partially good dynamic RAM devices.

Such techniques still have their problems, computer makers say. But they are being explored—in some cases with encouragement from the chipmakers—as a possible means of lowering cost per bit, increasing memory density, and making maximum use of the bits produced per wafer before next-generation 64-K RAMs reach volume production.

As with the previous generation of memory components, 64-K RAM production programs will at first produce many devices with one or more defective chip quadrants. This means the chip cannot be sold as a fully functional 64-K RAM. But such parts can be sold or used as partial devices containing, say, 32 kilobits or 48 kilobits of guaranteed functional memory capacity.

The idea is not a strange one to semiconductor manufacturers. Some of them for years now have made intensive use of previous-generation memory partials for outside sales and for in-house systems applications as a means of improving overall wafer yield. A notable example is Intel Corp. of Santa Clara, Calif. But with the rapid increases in memory density over the years, coupled with rapidly falling memory cost per bit, most computer makers have found no need to purchase and use such partial devices when fully-functional prime devices were available in adequate supply.

Evidence of a changing picture, however, can be seen in the following:

■ At least one minicomputer maker—Data General Corp. of West-

boro, Mass.—has recently begun shipping its first memory systems ever to be populated with partial devices—16-K chips that contain 8 kilobits of functional memory capacity. According to Allen Burgess, director of processor development, the company has designed memory boards capable of accommodating everything from the 8-K partial devices to fully-functional 16-K devices to 64-K parts when they become available.

■ Officials at a number of semiconductor firms say they have noticed a change lately in the attitude of many of their mainframe and minicomputer customers—particularly at the

64-K level. As noted by Gene Miles, memory components marketing director at National Semiconductor Corp., Santa Clara, Calif., every mainframe house in the country began to show interest in partials after IBM announced its 64-K dynamic RAM last fall [*Electronics*, Nov. 9, 1978, p. 39]. As with earlier devices, IBM is planning extensive use of partials during the early stages of its 64-K RAM program when yields on fully functional parts are low, says Art Strube, laboratory director at IBM's General Technology division in Burlington, Vt.

Officials at several computer companies confirm an interest in 64-K partials, but they note that pricing on the devices is currently being pegged by the chipmakers at about the same cost per bit as for fully-functional devices, which some computer officials feel is too high.

Error mapping. As an alternate approach, however, several mainframe and minicomputer makers have launched internal programs aimed at determining the feasibility of using error-mapping techniques to go around the bad bits in the defective quadrants of the partially good devices. Using such an approach, a computer maker might hope to lower effective cost per bit; a device that was purchased at a price based on guaranteed 32-K density, for example, might turn out to contain 50 or 60 good useable kilobits. Overhead costs associated with testing for the bad bits as well as for additional system circuitry to do the necessary memory mapping by means of such an approach, however, are currently seen as possibly prohibitive.

As an alternate strategy for increasing memory density until the 64-K devices arrive, computer officials say they also are looking at the possibility of housing two 16-K chips in a single package, thus providing a 32-K module that can be plugged into sockets designed to use 64-K chips later. Mostek Corp., Carrollton, Texas, is pushing such an approach with its MK4332, which houses two 4116-type devices in a single chip-carrier. Though the 4332 package is an 18-pin device, sockets can easily be designed to accommodate the 16-pin packages in which 64-K chips will later be available,

says Sam Young, dynamic RAM strategic marketing manager.

In addition to the 4332, which uses traditional 16-K devices requiring three power supplies for operation, Young explains that Mostek also plans to offer a similar product known as the MK4532. It will house two parts having single 5-volt supplies and thus be compatible with 64-K RAM supply requirements. Mostek's single-supply 16-K device, the MK4516, is scheduled for sampling during the first quarter next year, at about the same time that the company's 64-K RAM is expected to appear. Because it is smaller and consequently easier to make Young expects the 4516 to move down the learning curve much faster than will the MK4564, which is Mostek's 64-K dynamic RAM. When the 4564 does become mature, however, Young says that it will be offered in a 4332-type carrier, producing an 18-pin package containing a total 128-K density.

Besides the possibilities for varying strategies involving use of partials and/or two-chip hybrid packages, a third factor that the industry is watching while it waits for the 64-K devices involves the cost-effectiveness of the single-5-volt-supply, 16-K parts planned by several manufacturers.

Officials at Texas Instruments Inc., however, are not planning to offer immediately a 5-v 16-K part. According to Don Brooks, assistant vice president and manager of TI's MOS Memory division in Houston, the Dallas-based company does not now perceive a cost-effective window for such devices. Because they will be offsprings of the chip makers' new 64-K dynamic RAM technologies, they will start at the top of a brand new learning curve, Brooks figures, and will consequently not become cost effective before 64-K RAMs themselves move into volume production.

Brooks also downgrades the feasibility of placing two 16-K chips in a package as an effective interim means for increasing system capacity because of the added overhead costs of a two-chip carrier. He estimates those costs at 15% to 25% more than when two 16-K chips are used separately. □

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Computers

Retailers welcome a newcomer

Heath joins the market with a line to be sold through three chains as other makers report business is good

Is it possible to sell minicomputers and microcomputers through retail stores? To the handful of companies that believe the answer is yes, add the name of the Heath Co., the Benton Harbor, Mich., firm best known as a kit maker. But for its computer-retailing enterprise, Heath, which was purchased recently by Zenith Radio Corp. from Schlumberger Ltd. for \$64.5 million, is eschewing the kit route and will sell only assembled systems through at least three retail chains.

Heath says the keys to success as a computer retailer are hardware, software, and support. For the first two, the company feels it has the right mix in its new machines (see "Heath casts its line," p. 94). As for support, the answer is simple: its 55 kit stores will also become service centers for computers.

Beating Heath to the minicomputer market are Digital Equipment Corp. of Maynard, Mass.—the world's largest minicomputer maker—and the Computer Store Inc. The latter led the way into the retail minicomputer business in 1976 when it opened its first outlet in Burlington, Mass. It now has three stores in Massachusetts, two in Florida, one each in Connecticut and New York, and another coming soon in Rhode Island. DEC's five are in Manchester, N. H., Philadelphia, New York, Dallas, and Costa Mesa, Calif.

How is business for these and other retailers, and who are the customers? There are still few hard statistics on retail sales at the 600 or more stores in the U.S. that sell machines of all sizes, partly because the chain stores refuse to reveal them and partly because the hardware makers do not separate retail sales from total sales. However, Heath has projected some numbers that provide a guide to growth. By 1982, the sales of small systems for small businesses—that is, those retailing for \$2,500 to \$15,000 and excluding sales to hobbyists—should reach \$2 billion, all through stores.

Corner store. One of Digital Equipment Corp.'s five retail stores. They sell only the company's PDP-8 line of minicomputers plus peripheral equipment.

And it quotes industry estimates for total retail sales of small and personal computers as reaching \$3.2 billion by 1983.

Busmen. One independent retailer, Eri Golembo, vice president of the Computer Mart in Iselin, N. J., says he would be surprised if there were more than 20 or 30 stores in the country grossing as much as \$1 million a year. His outlet, he says, does more than \$1 million annually, has 24 employees, and each month sells 10 to 20 systems in the \$3,000 class and four or five full \$10,000 rigs. And "90% of the users are busmen on their holiday," Golembo adds—engineers, technicians, programmers, and the like.

But what is probably the giant of the personal computer business, when all sizes of computers are considered, is the Radio Shack chain. Its 50 computers-only stores—one per state—also act as service centers for all its full-line outlets, which also sell computers. Industry sources estimate that Radio Shack, a subsidiary of the Tandy Corp., Dallas, has half the market for small systems; the company says it has sold 100,000 TRS-80 systems since the system was introduced two years ago. Also, Radio Shack sources say that the firm's New York City store on West 45th Street is its top grosser: \$25,000 a month.

At Consumer Computer Marketing Inc. in Sudbury, Mass., a wholesale minicomputer distributor, business has been "absolutely fantastic," says Jeffrey P. Turner, regional account manager. Claiming his firm is the largest national computer distributor, the company's vice president and general manager, Robert



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Probing the news

L. Washburn, says, "Sales through retailing are excellent."

At the store level, Richard Brown, president of the Computer Store chain, says sales are up 25% from last year. He also expects his stores to meet or exceed that total in 1980. According to Data General Corp., sales of its MicroNova systems through the Computer Store have more than doubled over the past year, led by the expanding market in small-business computers.

What they sell. The Computer Store's inventory ranges from hardware like the Data General MP 100 Model 9062—with 64 kilobytes of main memory, 10-megabyte disk drive, display, and 30-character-per-second printer for \$16,190—to Cromemco Inc.'s scientific and engineering models for \$5,000, and Apple Inc.'s personal business com-

puters with 16-K random-access memory for \$1,195. Business-oriented software and accompanying instructions are also available.

DEC's stores, on the other hand, sell the PDP-8 product line. With a matrix or letter printer the price is \$11,400; software sells for \$400. Store personnel are all part of DEC's sales force, and each store has a classroom for customer instruction.

For the future, retailers exhale optimism with each breath. DEC says it expects retail sales to make a significant contribution to overall company sales. But as for manufacturers, W. E. Johnson, Heath's marketing vice president, says that after a shakeout in the 1980s "there will be three or four companies who will enjoy a major share of the market. We intend to be one of the ones who remain in the business." □

This story was reported and written by Kim Conley in Boston, and Howard Wolff, John G. Posa, and Anthony Durniak in New York

Heath casts its line

Heath Co.'s Data Systems division in St. Joseph, Mich., is introducing an 8-bit microcomputer, a 16-bit minicomputer, a video terminal, and a printer. The 24-line-by-80-character WH-19 terminal is controlled by a Zilog Z80 microprocessor. Its case also has space for a 5 $\frac{1}{4}$ -inch floppy-disk drive and a processor card (that also boards a Z80), and when these and software are added, the terminal is transformed into the 8-bit WH-89 all-in-one-computer, as Heath dubs it. Heath's 16-bit mini, the WH-11A, comes as two boxes: one containing Digital Equipment Corp.'s LSI-11/2 processor and another with dual 8-in. floppy-disk drives. An obvious choice of peripherals is the Heath terminal and WH-14 printer.

Hardware is only part of the story, however. W. E. Johnson, marketing vice president, points to a multipronged marketing push that includes aggressive pricing, software, distribution, technical support, and upward compatibility. Heath plans to price its systems well below the competition; for example, the WH-11A costs 26% less than a comparable Digital Equipment Co. PDP-11/03, says Heath, and the WH-89 will go for a third less than Radio Shack's TRS-80 model II [*Electronics*, June 7, p. 87]. Also, Heath is offering hefty discounts in original-equipment-manufacturer: for example, 35% for quantities of 100 in all six products; 39% for 1,000.

Software for the 8-bit machine accommodates word processing and Basic and Fortran programming. The mini has Heath's standard HT-11 operating system, but it can be fitted with a Dibex operating system from Information Access Systems Inc., with which Heath has signed a royalty agreement. Business packages are also available for both computers.

Heath has signed on with three retail distributors—Microage, Byte Industries, and Computerland—and is talking with others. And Heath's prices include substantial discounts for these retailers as well as for original-equipment manufacturers as it plans to exploit both outlets. Service will be provided by Heath's 55 kit centers located throughout the U.S. But that's the only part the centers will play since Heath wants the image of its new units divorced from the hobby world—after all, they will not be available in kit form. Finally, Heath plans some bold upgrade packages for future versions of its new product line, including more software, more mass storage, and possibly even more capable processor configurations. —John G. Posa

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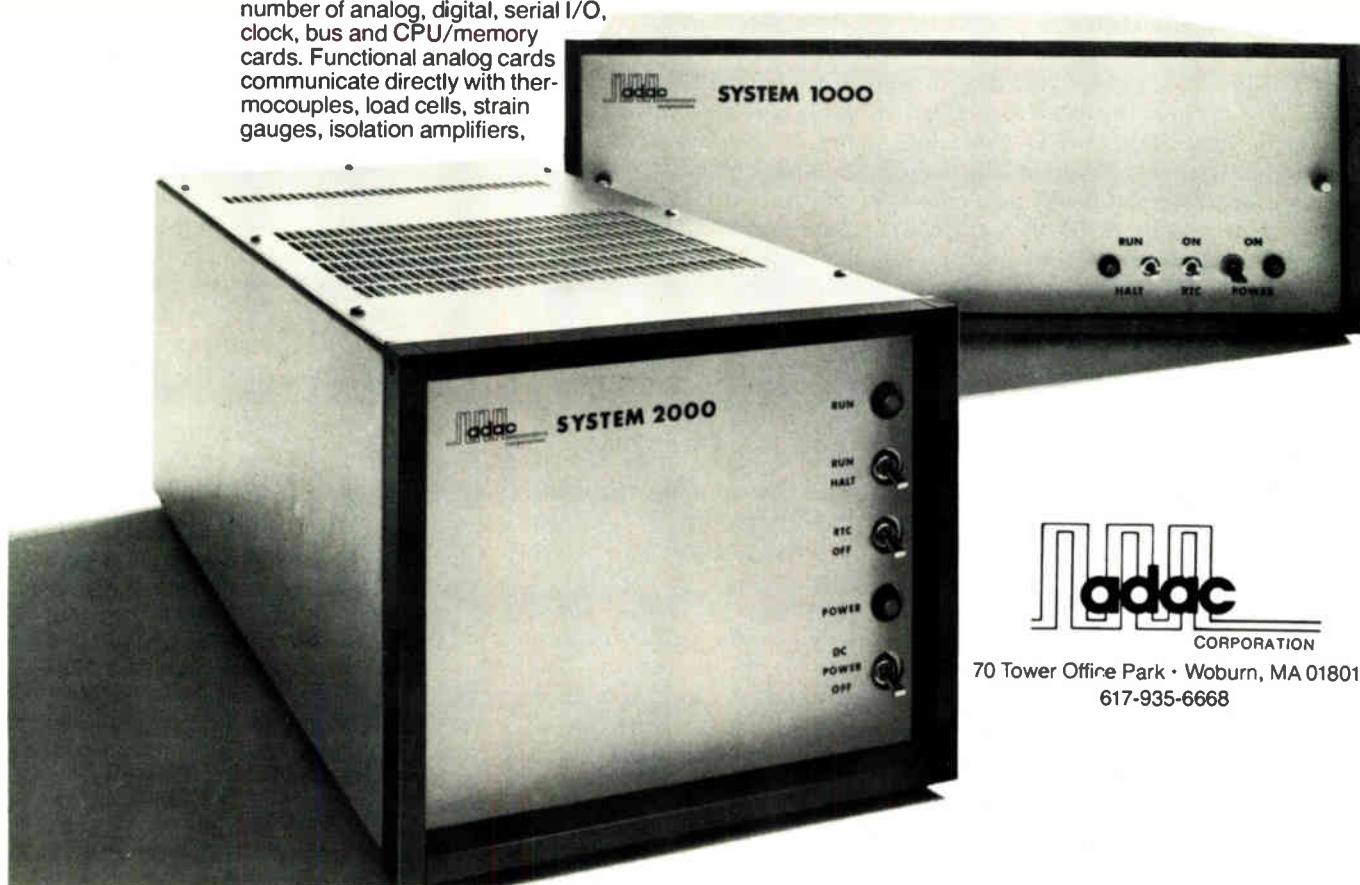
The compact System 2000 is built to hold 13 half quad cards. If you need greater capacity, slave units can be utilized or you can go to the larger System 1000 which accommodates any combination of 11 quad size cards or 22 half quad size cards. Both systems can be bench top or rack mounted and have a universal power supply that can support up to 256 kilobytes of memory.

The real heart of both System 1000 and System 2000 is their incredible number of analog, digital, serial I/O, clock, bus and CPU/memory cards. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers,

transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and other devices. All cards can be purchased as separate items.

A single System 1000 can be supplied with up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. A typical System 2000 contains a CPU, 64 kilobytes of memory, floppy disc controller, 16 channel A/D, 4 channel D/A, 32 TTL I/O lines, two serial I/O ports plus room for another six cards of your choice.

Another nice thing about both systems is their prices. They start at \$995 for the System 2000 and \$1550 for the System 1000. So you can choose the combination of price and capability that's just right for your application. Contact ADAC for full details.

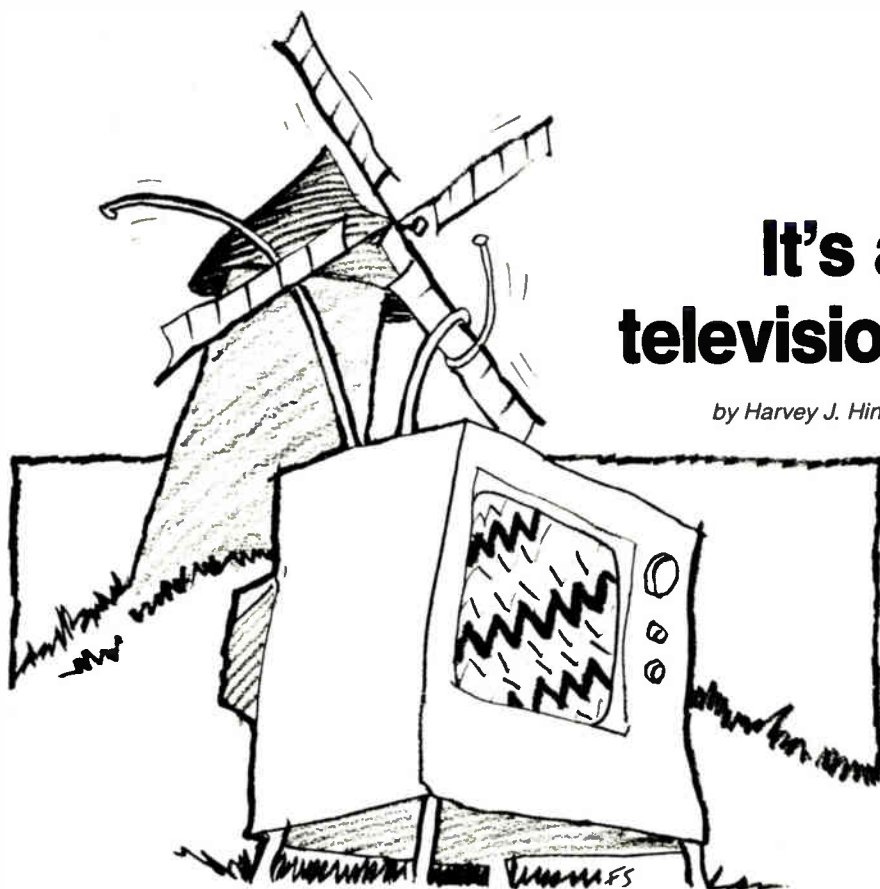


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Communications

It's an ill wind for television, study finds

by Harvey J. Hindin, Communications & Microwave Editor



It's annoying when an airplane flying over the house makes the television picture dance nervously for a few seconds just as the fullback rips into the end zone. However, it seems that people living near one of those big windmills that will go up to help solve the electrical power generation problem in this country ain't seen nothin' yet; those blades may give their pictures a permanent shake for as long as the windmill is turning.

"The rotating blades of a windmill can produce pulse amplitude modulation of the total television signal that a viewer receives," says Thomas B. A. Senior of the University of Michigan in Ann Arbor. "So, if you are located near one and your antenna is pointed so that you can pick up the forward scattering off the blades, the extraneous modulation can distort the video portion of the signal."

This distortion, Senior and his research colleague, Dipak L. Sengupta, point out, is likely to be more of a nuisance in the ultrahigh-frequency (uhf) rather than very high-frequency (vhf) bands since the apparent modulation becomes worse

as frequency increases. The audio portion is unaffected.

Why worry? The television interference problem is more than just an annoyance, says Senior. In fact, he notes it may be severe enough to affect acceptance of windmills, or wind turbines, as they are more properly called. They may possibly affect the operation of instrument landing systems at airports, a development that is under investigation, says Sengupta. Although the country is not dotted with Dutch scenes yet, large-scale construction programs could blow up a storm of major radio-frequency interference problems. There is apparently no problem with frequency-modulated radio or Loran navigation systems, he adds.

Lest anyone scoff at the thought of large-scale windmill programs, some large aerospace firms are currently working on them (see "Blowing in the wind," p. 97) with sponsorship from both the government and private sectors. A \$4-million windmill with 200-foot blades being developed by General

Electric Co. is typical.

"These problems would only apply to large installations," says Sengupta. "The small backyard windmill would generate few problems with home television unless the antennas and the blades were facing each other at the right heights."

TVI experiments. To get a handle on what might happen in a real situation, Senior and Sengupta have carried out both a theoretical and an experimental analysis using a 100-kilowatt windmill with 37.5-m blades that the National Aeronautics and Space Administration has constructed near Sandusky, Ohio. The two-blade rotor of this installation is metal-covered and is typical of turbines that may be built in the future.

The theoretical analysis showed that television interference that the windmill may cause is most likely to be video distortion attributable to amplitude modulation of the signal. Just how much distortion can be expected depends on the size of the rotors, the rotation speed, the height of the rotor and receiving antenna above the ground, the frequency of the signal, the distance between the windmill and the receiver, and other variables. This plethora of variables makes it difficult to predict the exact quantity of interference. In order to obtain experimental data, a number of on-site measurements were made in Sandusky. Several channels and several different kinds of television receivers were tested.

Lots of data. While the results varied widely in response to different test conditions, there were several cases where the distortion was so bad that it led to "a form of video distur-

Blowing in the wind

Today, although the homeowner or farmer can buy a wind turbine, it is uneconomical in most places. However, this situation is changing rapidly. Starting with today's 5,000 or so wind turbines, one study holds there will be 30,000 small ones and 1 million large ones operating in the U. S. by the turn of the century. Upwards of 5% of the country's electricity may eventually be generated in this way.

This year, at any rate, the Department of Energy will spend \$60 million on wind turbine research. Southern California Edison Co. is putting up a 3-megawatt machine and expects to have 18 of them working by the mid 1980s. Design and development work is being done by Grumman Aerospace Corp., General Electric Co., Alcoa Inc., Boeing Co., and United Technologies Corp., among others.

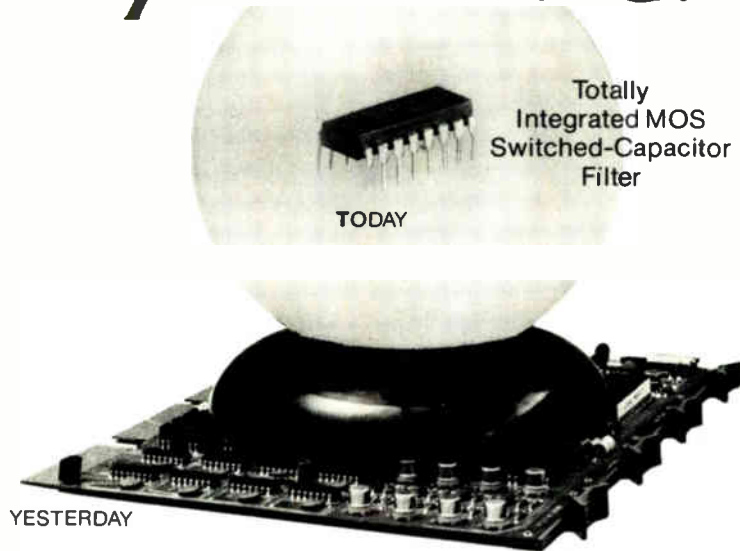
tion that can be quite painful to the eye," according to the researchers.

Since there was insufficient flexibility in actual site tests to cover a very broad range of conditions, simulations were also conducted under laboratory conditions to examine more combinations of variables. The most important part of the study was developing a graphical way to determine the interference region in any given situation. This calculation shows that the NASA windmill could cause unacceptable interference on channel 52 as far away as several kilometers under some conditions.

The researchers are at present performing tests with television signals they generate themselves. They are also scaling all the variables in their experiments so they can examine a complete range of possible operating conditions in a convenient, cost-effective way. The expected result is rules for siting windmills so as to minimize objectionable interference in most practical cases.

Senior and Sengupta are the only researchers looking into these problems at the present time. As the number of installations grows, however, it is likely that there will be a lot more interest in their work. □

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Packaging & production

New system challenges Wire-Wrap

Also developed at Bell Labs, Quick Connect offers advantages of one wire per connection and lower board profile

by Jerry Lyman, Packaging & Production Editor

Typical circuit boards and backplanes today are so densely packed that they can have up to 100,000 interconnections. Only automatic machinery can wire such boards, and a technique developed by Bell Laboratories in 1948 is still the dominant one: Wire-Wrap, a system for wrapping insulated wire around a square post.

But since 1975, a potentially serious competing technology has been waiting in the wings. It is Quick Connect, a technique also developed at Bell Labs. Invented by Charles von Roesgen, supervisor of the circuit development group at Bell

Labs' Holmdel, N. J., facility, it is also a point-to-point wiring system but one that uses insulation-displacement contacts rather than insulation-displacement wire wrapping. Like Wire-Wrap, it makes a gas-tight connection to a terminal, but unlike Wire-Wrap, it is not yet fully automatic.

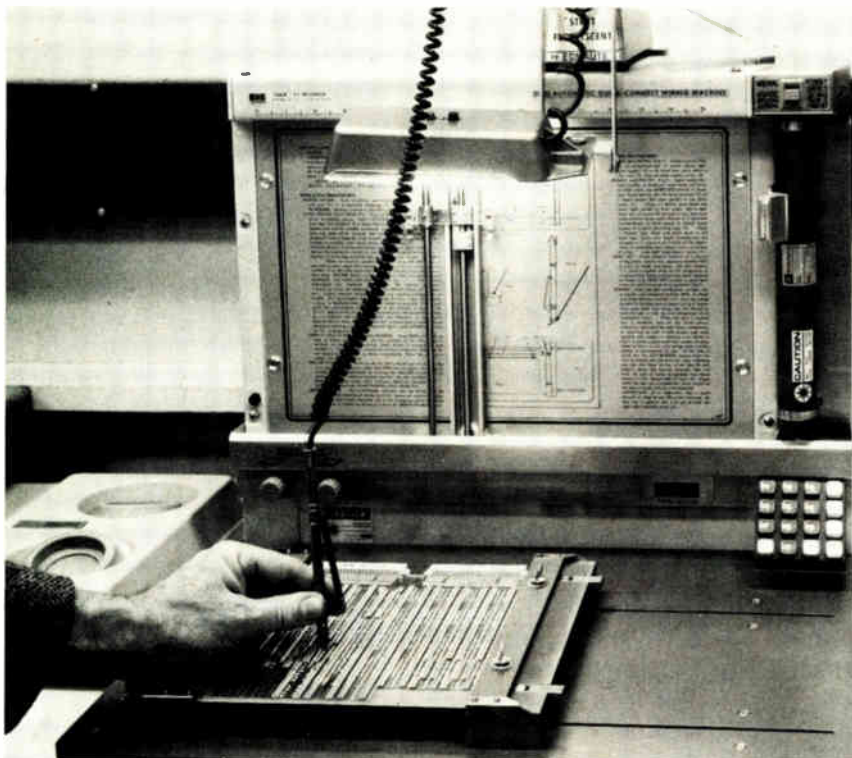
The impetus for Quick Connect's emergence into the world of commercial electronics will be provided by Robinson Nugent Inc. of New Albany, Ind. The manufacturer of connectors has developed a line of hardware, boards, and a manual wiring tool for the user.

Like Wire-Wrap, Quick Connect has three basic components: a wiring terminal, a board, and a wiring tool. The terminals, whose long development time is what really held back this system, are one-piece stampings made from beryllium copper. One end of the socket/terminal is barrel-shaped to accept integrated-circuit leads; the other end has a two-level insulation-piercing contact. The Robinson Nugent socket/terminal, (see figure on p. 100) has a wire stop to prevent wires from bottoming in the slot and to prevent IC leads from disturbing the wiring.

Arrays of these socket/terminals on 100-mil centers are press-fitted or soldered into plated-through holes on glass epoxy boards with plated-on ground and power planes. Then No. 30 AWG insulated copper wire is forced into the insulation-piercing contacts with a manual wiring tool or a semi-automatic wiring head.

Quick Connect has several advantages over Wire-Wrap and other competitive wiring systems. For one thing, no insulation stripping is required: wiring is point-to-point with each connection having both in and out potential (Wire-Wrap requires two wires per connection, Quick Connect only one).

Another important advantage is a lower board profile. Quick Connect has a 0.250-inch profile, compared to the 0.575 in. of the thinnest possible level (two-level) wire-wrapped board. This factor aids in high-speed logic operation as well as allowing more boards to be packed in a given volume. In addition, Quick Connect is easy to repair and modify, and the board is reusable. According to von Roesgen, Bell Labs is now using the



Quick system. One of eight semiautomatic wiring machines designed at Bell Labs is shown working on a Quick Connect board. No commercial versions are available.

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Probing the news

system for prototyping digital circuit boards at its Merrimac Valley, Mass.; Holmdel, N. J.; and Columbus, Ohio, facilities. Boards ranging in size from 13 by 7 in. to 2.5 by 6 in. are being wired for TTL, TTL-Schottky TTL, and Motorola's emitter-coupled-logic devices.

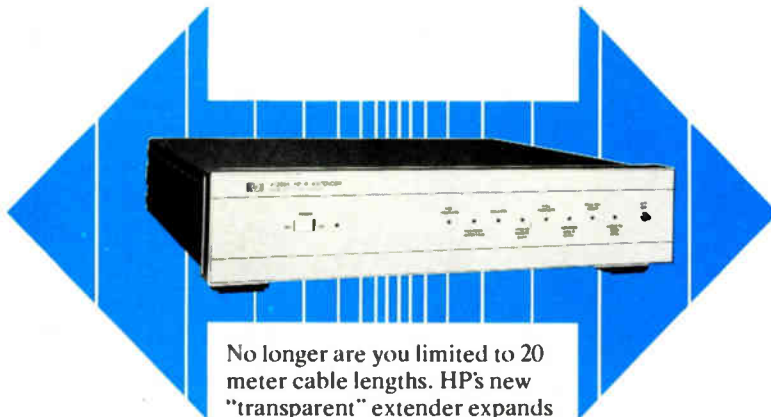
Bell's von Roesgen tried unsuccessfully for three years to get some-

one to build socket/terminals to Bell specifications. Then in 1977, Jim Jones, a senior vice president at Robinson Nugent, read about Quick Connect in *Electronics* and called von Roesgen about the possibility of his company furnishing the hardware.

The Indiana company paid for its own tooling and successfully developed a Quick Connect socket. It has since delivered thousands to Bell Labs. Stanford Applied Engineering Co. of Santa Clara, Calif., is pres-

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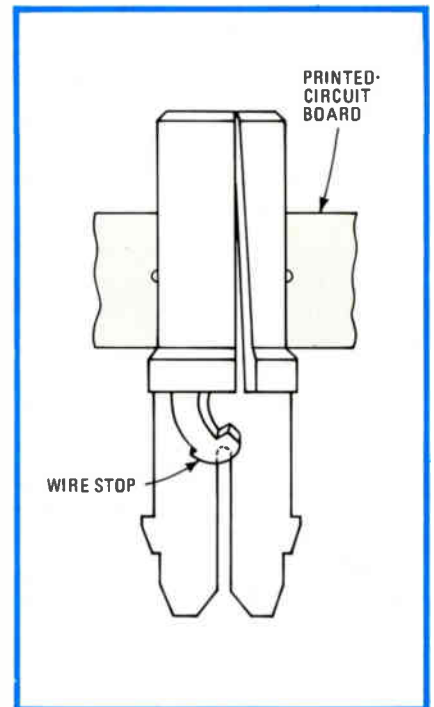
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Making connections. The Quick Connect socket/terminal permits IC insertion from the top, and two levels of wiring on the insulation-piercing contact side.

ently trying to qualify the same type of hardware.

Under its agreement with Bell, Robinson Nugent is allowed to market its hardware to other companies. In prototype quantities, Robinson Nugent can furnish strips of socket/terminal, customized or standard pc boards with the sockets already on them, a manual wiring pencil, and tooling to insert groups of socket/terminals.

Bell Labs has designed a semi-automatic wiring machine that can put down Quick Connect wiring at double the rate of a comparable semi-automatic Wire-Wrap system. Eight of the machines have been built to Bell specs—six by Bell and two by Gardner-Denver, Grand Haven, Mich. Gardner-Denver has no plans now to market them.

Robinson Nugent is now working with other companies such as Universal Instruments Inc. of Binghamton, N. Y., to design a reasonably priced semi-automatic machine. While Jones feels that only Robinson Nugent presently has the potential for full production of Quick Connect hardware, he says that for production use a semi- or fully automatic machine is a must. □

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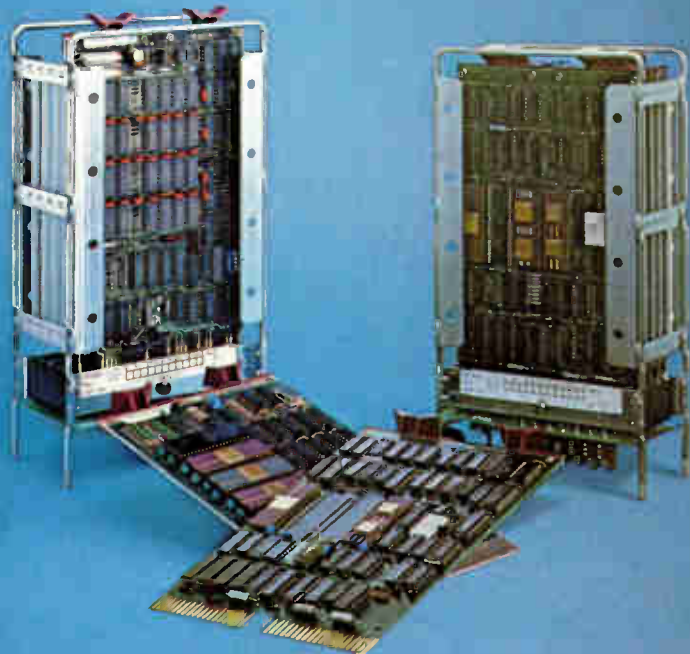
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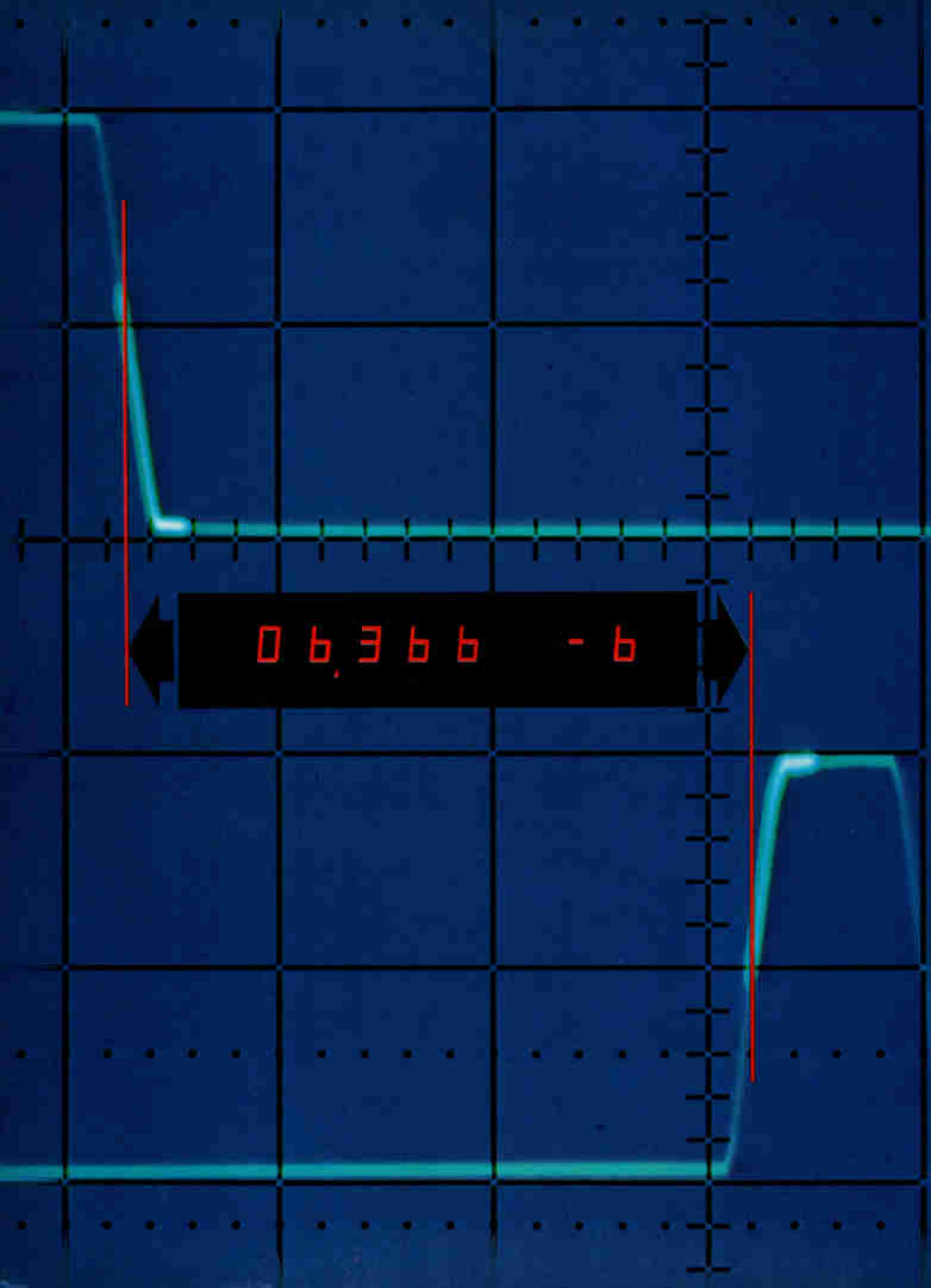
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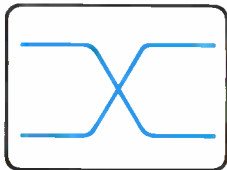


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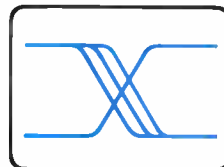
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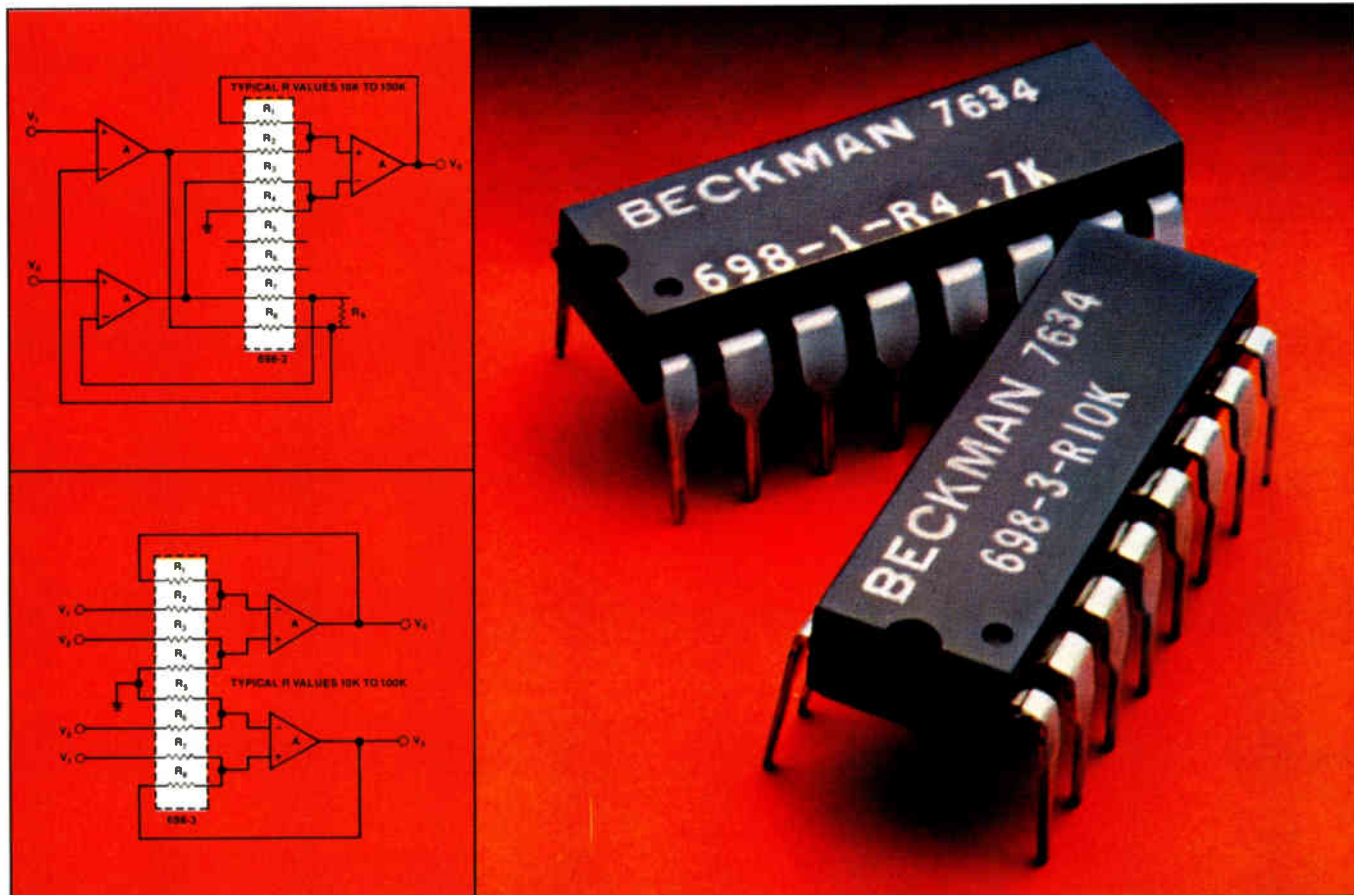
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Special report: new LSI processes

Older processes revamped as new arrivals extend performance limits

Improved MOS processes aim at speed rivaling bipolar;
fast new bipolar approaches cut power needs, boost density

by Raymond P. Capece, *Solid State Editor*

□ The stereotypical qualities associated with various semiconductor process technologies are sorely in need of reassessment. Anyone who thinks that complementary-MOS is only for watch chips, or that n-channel MOS is slow, or that bipolar circuits dissipate a lot of power, is way off base. The competition among processes in many application areas has heightened sharply as a result of improvements effected in every technology in the last few years. Designers depending on the old truisms are going to find their planning outdated. The two articles following this one and others in upcoming issues will spotlight the development work now in progress.

Recent improvements in both MOS and bipolar technologies will show up in parts later this year. And development work being done now promises dramatic new specifications in next year's memories, microprocessors, and logic circuits.

The new MOS

The versatile MOS processes are undergoing the most active development, both in memory elements and logic circuits, and the key word is speed. Whether for random-access or read-only memories or for logic devices like microprocessors, manufacturers of n-channel and complementary-MOS circuits are hard at work making their chips work faster. True, graduating density is an important consideration in the design of large memories and microprocessors, but attaining a higher level of performance comes first.

At the proving ground for speed—the static RAM for mainframe cache and control-store applications—

n-channel MOS has continually eroded the established base of bipolar memories. Intel Corp. of Santa Clara, Calif., was the first to attack the high-speed bipolar RAMs with its high-performance HMOS process. The technique involved scaling down transistor size (so that gate delays were minimized to about 1 nanosecond), but also required the development of faster peripheral circuits, such as the chip-select buffers and address decoders. In addition, driving MOS circuits to high speed made chip designers suddenly aware of the importance of minimizing RC delays and optimizing layout for the shortest possible runs of polysilicon interconnect.

In fact, these latter aspects, and not scaling, are often the most difficult. Though most MOS manufacturers are competent in 3.5-micrometer lithography and 700-angstrom oxide production technology, few of them can produce adequate yields on the 55-ns version of Intel's industry-standard 4-K-by-1-bit RAM, the 2147.

Now Intel has scaled its process further to what it calls HMOS II (see p. 124). The new name is tagged primarily to a reduction in active channel lengths to 2 μm and gate oxide thicknesses to 400 Å. The scaling of HMOS II aims at speed, reducing gate delays to 400 picoseconds; yet Intel claims it can be produced in volume on any HMOS line, because the improvements were made to be compatible with the earlier process and only the active areas of fast transistors are redefined to 2 μm . But again, the 2147H, the 4-K RAM built with HMOS II that currently carries a premium access time of 35 ns, is made possible not only by shrinking but by improved chip-select buffers and other peripheral

circuits surrounding the mercury array.

A variant of n-channel MOS, American Microsystems Inc.'s V-groove MOS technology is well along in fulfilling its promise for density, at least. Not that the n-channel technology is slow—the Santa Clara, Calif., firm is currently shipping samples of its V-MOS version of the 2147 with a 55-ns specification—but density is its strong suit. All the company's memories are coming out smaller than anyone else's. A look at the evolution of AMI's 1-K-by-4-bit 2114 gives a sketch of the strategy.

V-MOS is tops in density

The cell size of the 2114 laid out with $4\frac{1}{2}\text{-}\mu\text{m}$ design rules was 1.95 mil^2 , resulting in a die size of about $14,000\text{ mil}^2$ —itself small by industry standards. A new layout brought those numbers to the current production figures of 1.34-mil^2 cells in a $10,400\text{-mil}^2$ die.

Most dramatic, however, is size of the next-generation part. (It should be noted that AMI duplicates its cells throughout all its RAM products; thus, the fast 2147 parts will have exactly the same die size as the 2114.) The 2114 currently in layout with prototypes expected shortly will use shrunken $3\frac{1}{2}\text{-}\mu\text{m}$ design rules and will scale the active regions of its V-MOS transistors from $4\frac{1}{2}$ down to $4\text{ }\mu\text{m}$ and those of its n-channel devices from $2\frac{1}{2}$ down to $2\text{ }\mu\text{m}$. The resulting part will have a six-element (four transistors and two polysilicon load resistors) cell size smaller than anything in the history of static RAMs: 0.86 mil^2 . (The 4-K die size is also a record-breaker:

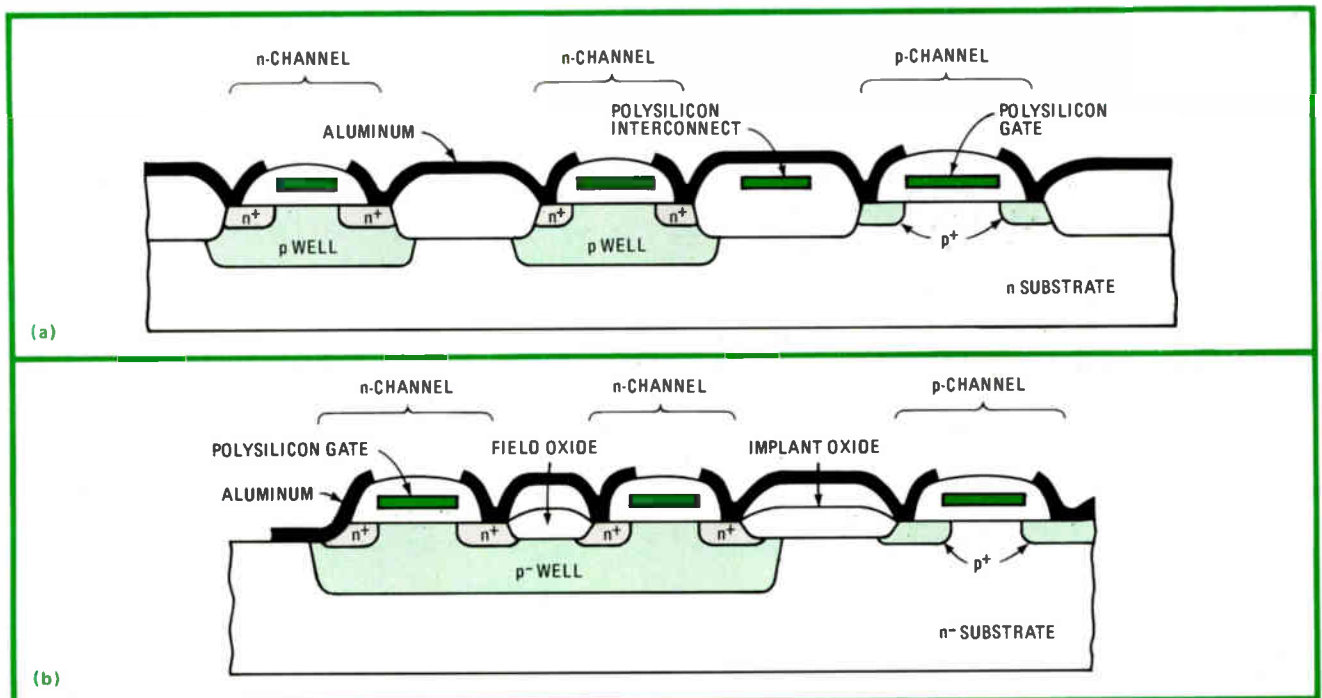
$7,225\text{ mil}^2$.) As a consequence, V-MOS not only has a better shot at achieving the density needed for the 64-K static RAMs of the next generation, but it will likely result in devices that are faster than their n-MOS counterparts in the same price range.

The density advantage of V-MOS is also apparent in AMI's read-only memories and dynamic RAMs. The company's forthcoming 64-K dynamic RAM, for example, is sure to be the industry's smallest, coming in well under $30,000\text{ mil}^2$ on the first pass, compared with the $33,000$ to $40,000\text{ mil}^2$ of other current designs.

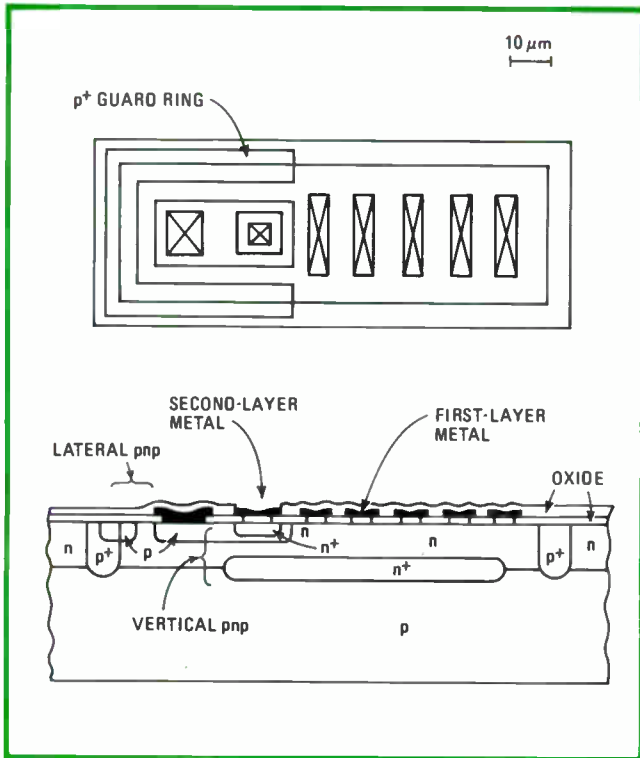
All MOS circuits will pay in power dissipation for increased speed as the circuit capacitances begin to take their toll. In a 4-K-by-1-bit n-channel RAM, for example, as much as half the maximum power is dissipated in driving the capacitively loaded output line. Complementary-MOS circuits, which are gaining in speed, will sacrifice their low power consumption for the cause. But the beauty of C-MOS is that, regardless of how much power it may draw at high speed, it still powers down to a microwatt standby mode when idle—automatically. For that reason alone, C-MOS will find its way into larger, fast memory systems, whereas now all the n-MOS and bipolar parts not being accessed draw power.

Developing C-MOS performance

Among those manufacturers developing high-performance C-MOS circuits are: Harris Corp., Melbourne, Fla.; Mitel Corp., Ottawa, Ontario, Canada; American Microsystems Inc.; and Toshiba Corp. and Nippon Electric Corp. in Japan. All are aiming at reducing capacitance, so that as the circuit is pumped up in speed, its power consumption does not rise inordinately in accordance with the law stating that power is dependent on capacitance, voltage, and frequency: $P = \frac{1}{2}CV^2f$.



1. Today's C-MOS. The process used by Mitel Corp. (a) isolates p wells, lending itself to logic fabrication; the ubiquitous p-well process (b) by American Microsystems Inc. aims at memories. Both challenge n-MOS performance when scaled to $3\frac{1}{2}$ -micrometer dimensions.



2. New bipolar. Integrated Schottky logic gate (shown in top view and cross-section without the current source) outperforms integrated injection logic, though it pays a slight penalty in area. Developed by Philips, ISL is being used by Signetics for fast, dense gate arrays.

The approaches are varied slightly, as Fig. 1 shows. Some, like Mitel, isolate all devices with oxide (not unlike some bipolar approaches, such as Fairchild's Isoplanar process) to boost speed. Harris and AMI believe that for memories, good performance at high density can be had using junction isolation between similar device types. While no revolutionary developments are in sight, subtle process improvements are eating away at the capacitance that slows C-MOS down. Moreover, simply scaling the current C-MOS technology, which uses 5- to 7- μm design rules, down to 3 or 4 μm will boost the performance proportionately, in much the same way it did for n-MOS. Table 1 compares today's 5- μm C-MOS processes with tomorrow's 3- μm super-C-MOS (see p. 116) and other technologies.

AMI's next C-MOS generation will be scaled to 3½- μm line widths and spacings. The layout will use only n+ polysilicon and is a ubiquitous p-well process, so called because adjacent n-channel transistors sit in a shared single region of p-type semiconductor. AMI is using this approach rather than the oxide-isolated (or isolated p-well) approach because it is suited to circuits that use more n-channel devices than p-channel ones, such as static memories whose cores are all n-channel devices.

According to Donald L. Wollesen, C-MOS research and development manager at AMI, the process will allow fabrication of high-speed static RAMs with C-MOS peripheral circuits surrounding a core of six-element n-channel cells. This approach has been taken by Hitachi Corp., which is enjoying much success with its 6147 4-K static RAM and is now producing prototypes of a

TABLE 1: COMPARISON OF MOS TECHNOLOGIES AT 5 AND 3 MICROMETER GEOMETRIES

| | Complementary-MOS | n-MOS | V-MOS | C-MOS on sapphire |
|---|-------------------|-------|-------|-------------------|
| ¹ Devices per mil ² | 5 μm | 0.67* | 1.0 | 0.7* |
| | 3 μm | 2.5 | 2.8 | 2.6 |
| ² Power-delay product (picojoules) | 5 μm | 6 | 12 | 2 |
| | 3 μm | 1.3 | 2.7 | 0.8 |
| ² Gate delay (nanoseconds) | 5 μm | 1.8 | 4.5 | 1.8 |
| | 3 μm | 0.5 | 1 | 0.7 |

¹ All figures assume devices are used in a static random-access memory whose cells have polysilicon load resistors except those marked *, which have depletion loads

² Energy and propagation figures are based on performance of a single inverting gate in a ring oscillator

SOURCE: American Microsystems Inc.

similar 16-K device. The 6147 is a pin-compatible substitute for the industry-standard 2147, yet it has a standby power in the microwatt range and dissipates only 220 milliwatts when running at 55-ns access speeds. AMI has similar plans for fast C-MOS memories. "But we expect to beat the 6147 in speed," says Wollesen.

What will undoubtedly contribute to the cause of C-MOS as a high-speed memory technology—in addition to its minute standby power dissipation—is its resistance to soft errors caused by alpha-particle bombardment [*Electronics*, March 15, 1979, p. 85]. Because the fully C-MOS static cell has active pullup transistors, any alpha-generated currents are drawn off. But even in the n-channel-core approach pursued by Hitachi and AMI, which uses high-resistivity (gigohm) polysilicon load resistors, the fact that the core is immersed in a p-type well allows alpha-generated carriers to either recombine quickly or join the majority-carrier flow. The result is a RAM with higher resistance to soft errors than any n-channel device using polysilicon loads.

Isolated approach

Mitel's process, which it calls Iso-C-MOS, has proven its high speed in the custom C-MOS gate arrays that the company designs. The gate delays are well below 10 ns, and Mitel reports that single gates have been clocked at 55 megahertz. What that means for the 3.5- μm process in the near future is a C-MOS version of Motorola Inc.'s 6802 8-bit microprocessor that uses a 5-MHz clock, plus a 2114-type 1-K-by-4-bit static RAM with an access-time target of well below 100 ns. Tying that process down could mean that oxide-isolated C-MOS, too, will find its way into mainframe memories.

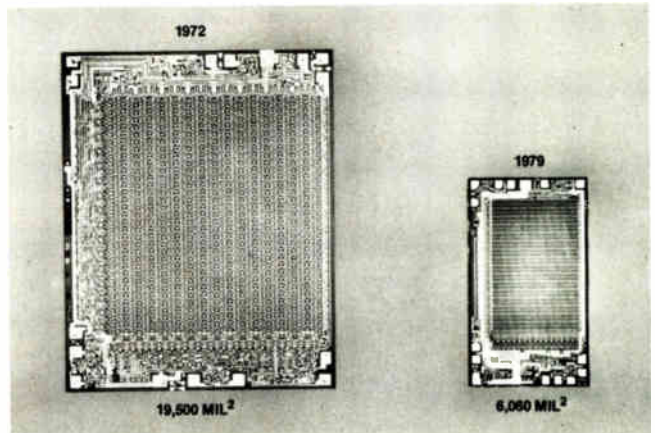
Mitel's Iso-C-MOS parts have a power-delay product that varies with operating speed. To be sure, it is good at all operating speeds, but rises dramatically as gate delays dip below 10 ns. Above 10 ns, the power-delay product is an exceptional 0.05 picojoule for the 5- μm process that Mitel uses today; that process pushed to

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1-ns gate delays would be in the 2-to-3-pJ range. Interestingly, Mitel has extrapolated data for its next-generation scaled devices that will push down the power-delay product even as speeds rise. For example, a 4- μm process operating at a 3-ns gate delay will have a power-delay product of less than 0.2 pJ; and when Mitel further scales to a 2- μm process, the 1-ns gates will have a power-delay product of about 0.1 pJ. That kind of performance cannot be matched by any other process, with the possible exception of C-MOS-on-sapphire.

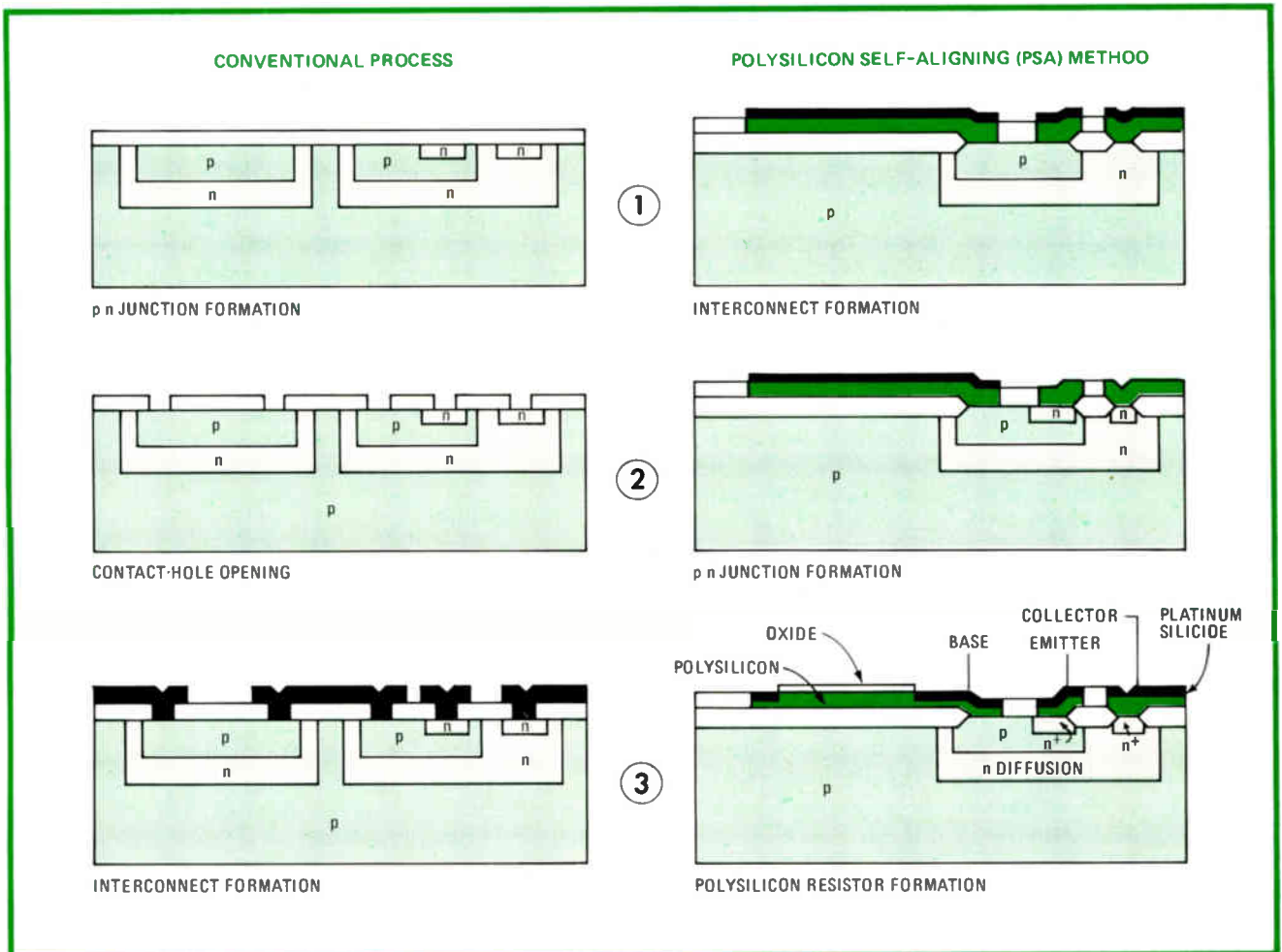
The C-MOS-on-sapphire quest

While at this point C-MOS on sapphire cannot be regarded as a mainstream production technology, it still holds promise for premium-speed applications of the future. It offers a slight density advantage over standard junction-isolated C-MOS, as evidenced by the 24,000-mil² die size of RCA Corp.'s C-MOS-on-sapphire 4-K static RAM compared with standard C-MOS 4-K parts made by

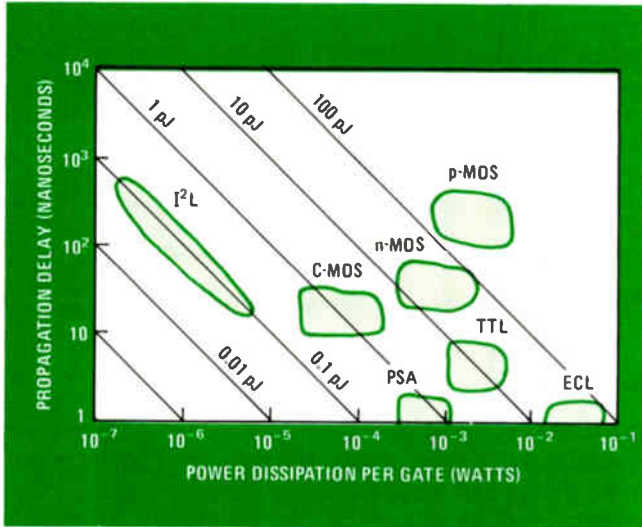


3. Shrinking. A boon to the speed of bipolar devices is the shrink. Here, Fairchild's new Isoplanar S process reduces the die size of the 93415 1-K static random-access memory from 14,000 mil² to 6,500 mil² while slashing the access time from 30 to 20 nanoseconds.

Harris Corp., Intersil Inc., and others, which come in at 30,000 mil² or more. It also has yet-unrealized potential for far lower power dissipation. The density advantage, however, hardly outweighs the cost premium of the sapphire substrate. Even the speed and power-dissipation



4. Add polysilicon. Nippon Electric Corp.'s polysilicon self-aligned bipolar process builds faster and denser memories since the polysilicon makes high-value resistors with low parasitic capacitance. PSA also differs from conventional processing in forming interconnects.



5. Stands alone. PSA combines emitter-coupled-logic speed with the moderate power dissipation of n-channel MOS. The process requires one more mask than conventional processing, but that is well compensated for by the ease of the self-aligning process.

advantages of C-MOS on sapphire are being eroded by bulk-silicon C-MOS, especially at finer geometries.

Rockwell Corp. is at work exploiting the speed of C-MOS on sapphire in custom analog-to-digital converters and counter chips toggling in the 500-MHz region, but the remarkable results are due to fine line work and the parts are still extremely expensive. Toshiba Corp. sees sapphire substrates as a route to higher-performance n-MOS as well as C-MOS, but maintains that until a sapphire wafer with silicon epitaxy drops in cost to \$50, C-MOS on sapphire will not be cost-effective. C-MOS-on-sapphire static RAMs operating with typical access times of 40 ns are currently in Toshiba's research and development labs.

What tarnishes the image of C-MOS on sapphire is the strides made by manufacturers of bulk-silicon C-MOS. AMI says it has no plans for sapphire; nor does Nippon Electric Corp., a major manufacturer of C-MOS circuits. The Japanese firm plans to announce a 55-ns 4-K static RAM—compatible with the industry-standard 2147—built entirely out of junction-isolated C-MOS early next year. That NEC's process does not suffer in density is evidenced by a 16-K C-MOS RAM that is currently in prototype. The part is built with $3\frac{1}{2}$ - μm geometries.

The new bipolar

Bipolar technology is relatively immature in certain ways, since little of the ambition with which MOS designers have forged ahead to higher speed and density has focused itself on bipolar LSI. The technology may have held fast to its niche of high speed and military customers, but thanks to pressure from MOS, makers of bipolar LSI have been obliged to improve it in several areas. Integrated injection logic has established high-density bipolar LSI, and improving its speed as well. Also, logic and memories fabricated in TTL are being revitalized with finer lithography.

A version of integrated injection logic called integrated Schottky logic (ISL) developed by NV Philips

Gloeilampenfabrieken in the Netherlands [*Electronics*, June 3, 1978, p. 41], is coming to fruition at Philips' U. S. subsidiary, Signetics Corp. The Sunnyvale, Calif. company is now building gate arrays with ISL, using the 5- μm -collector gates shown in Fig. 2

ISL has the potential to be a high-speed, low-power technology with good drive capability. "ISL can be as fast as MOS in those applications where you need speed and a strong TTL drive," says Stephen Lau, product line marketing manager for custom LSI products at Signetics. "When there are no loads, n-MOS switches fast," he explains, "but in the real world, loading slows it down considerably."

Lau adds that the density figures originally reported by Phillips—a penalty of 40% to 50% over standard I^2L —were misleading. "We're seeing about the same density as I^2L . The gate array we've built is 15% to 20% larger than the I^2L version, but that's only because we've added three more collector outputs per gate."

The speed-specification targets for ISL are worst-case delays of 4 ns per gate, with a typical figure of 2 ns. Signetics has also improved on Philips' original power specifications. The injection current is 150 microamperes and the power dissipation of the 1,000-gate array is a scant 225 microwatts.

Signetics has plans for standard products built with the new technology along the lines of high-speed controller circuits, though it will give no details right now. While ISL does not lend itself as well to analog circuits as I^2L , Signetics has mixed ECL, low-power Schottky TTL and ISL on a single chip for proprietary custom circuits.

Faster TTL

Fairchild Camera and Instrument Corp. has initiated the first installment in what it calls its Isoplanar S program for scaling down bipolar circuits [*Electronics*, Aug. 30, 1979, p. 39]. The process has been applied to the Mountain View, Calif., company's 1-K-by-1-bit RAM, the 93415, which has been shrunk from 10,000 mil^2 to 6,000 mil^2 in the new 93F415 (Fig. 3)—a part that is also 33% faster, with a 20-ns maximum access time. There are three areas of concentration in the Isoplanar S program. The first is lithography. The 93F415, for example, uses minimum line widths of 4 to 5 μm , which is 2 to 3 μm less than earlier Isoplanar work. According to Devereux Rice, strategic marketing manager for bipolar LSI at Fairchild, the line widths will drop to 2 or even $1\frac{1}{2}$ μm over the next two years as direct-wafer-stepping equipment is brought on line. (DSW equipment has just been installed and will be used to make Fairchild's first 16-K RAMs, to use 4- μm lines. They are due out the first quarter of next year.)

The second area of focus in Fairchild's program is the metal systems—the alloys used for interconnections. In addition to looking at different alloys in hopes of finding better ones for fine-line lithography to replace the silicon-aluminum-copper alloys used in the past, metal deposition techniques are being researched. Fairchild is investigating sputtering and vacuum vapor-oxidation techniques aimed at reducing the defect levels, which must be scaled down with the geometries if good yields are to be maintained. Fine-line metalization does have

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its associated problems with etching and electron migration, concedes Rice, "but they are directly analogous to the problems MOS manufacturers have with polysilicon."

The third leg of the Isoplanar S program attacks power dissipation. The goal here is to reduce the power levels without sacrificing speed, and the job requires changing basic device structures. Walled resistors with higher values are used in place of the usual diffused resistors, and new pnp structures are being developed to cut power. Also, Rice expects the improved alignment technique to reduce capacitances and thus further reduce power dissipation.

According to Lou Williams, bipolar RAM marketing manager at Fairchild, powering down bipolar RAMs—in much the same way that MOS RAMs cut power by as much as 80% when deselected—is entirely possible, although perhaps not to the same degree. "We're doing preliminary analysis to see what it would take," he says. "But the only market we see for power-down RAMs is the military. The commercial markets are happy so long as we keep the parts at about a half watt." Williams adds that his primary drive is still for speed.

Is there a limit to this quest for speed? The answer is yes. Says Williams: "Our goal is to bring all parts—1-K, 4-K, and 16-K RAMs—down to a worst-case access-time specification of 20 ns. There's no sense in going beyond that with a TTL-compatible RAM, because then the memory is faster than the logic." But Fairchild is also in the emitter-coupled logic business, where speeds below 10 ns are not unusual, and it will continue its program

there. (All of Fairchild's TTL RAMs, in fact, are first made in ECL, then redesigned for production in TTL.)

Once the speed problems are licked, the main goal is higher density. Fairchild is expecting its first 16-K RAMs at about year end. The parts, built with 4- μ m metal lines, will first be run on DSW equipment. The organization will likely be first 16 K by 1 bit, then 4 K by 4 bits to suit the needs of mainframe cache memories, writeable control stores, and bit-slice processors.

The limit

If bipolar manufacturers see a speed limit on TTL-compatible RAMs and logic parts and look to ECL as the next frontier for high-density designs, where will MOS manufacturers wind up? Probably in the same arena. According to Richard Pashley, manager of static RAM circuit design and technology development at Intel, TTL-compatible MOS RAMs will bottom out at the TTL limit of 20 ns—even though the MOS process promises even faster parts. "But when TTL runs out of speed," Pashley says, "people will have to standardize on one brand of ECL, and ECL will really begin to grow as the parts become readily available off the shelf at a decent price." As to whether Intel will move into ECL-compatible MOS RAMs, Pashley says, "It's definitely a possibility. The smaller voltage swings of the ECL levels would certainly help along faster MOS devices."

With all the emphasis on high-speed circuits, ECL is getting more attention from bipolar device manufacturers. Some, like National Semiconductor, choose not to work on TTL RAMs, for fear of MOS pressure, and have shifted bipolar design to ECL memories. The level of ECL circuit complexity has risen to the borders of LSI, as shown in the 1,000-plus-gate ECL gate arrays and the new bit-slice parts. Fairchild has recently introduced an 8-bit ECL slice [*Electronics*, Aug. 2, 1979, p. 120] and

TABLE 2: SUMMARY OF PROCESS PROPERTIES

| Property | CURRENT TECHNOLOGY, 1979 - 1980 | | | | | | | | FUTURE, 1985 - 1990 | |
|--|---------------------------------|---------------------|------------------|------------------|-----------------|--------------|---------------|--------------|---------------------|--------------------|
| | T ² L | LS T ² L | ECL | I ² L | p-MOS | n-MOS | C-MOS | | Silicon on sapphire | GaAs |
| | | | | | | | bulk | on sapphire | | |
| Relative process maturity (1-10 scale) | 10 (8)* | 9 (4 to 5)* | 8 to 9 (3 to 5)* | 4 | 10 | 9 | 8 | 4 | 2 (1980) | 1 (1980) |
| Process complexity (processing steps) | 18 to 22† | 18 to 23† | 19 to 23† | 13 to 17 | 8 to 14 | 9 to 15 | 14 to 17 | 14 to 20 | 14 to 20 | 16 |
| Logic complexity (components per 2-input gate) | 12 | 12 | 8 | 3 to 4 | 3 | 3 | 4 | 4 | 3 to 4 | 2 |
| Packing density (gates/millimeter ²) | 10 to 20 | 20 to 40 | 15 to 20 | 75 to 150 | 75 to 150 | 100 to 200 | 40 to 90 | 100 to 200 | 200 to 500 | 300 to 1,000 |
| Typical propagation delay (nanoseconds) | 6 to 30 (10) | 2 to 10 (5) | 0.7 to 2 (2) | 7 to 50 (20) | 30 to 200 (100) | 4 to 25 (15) | 10 to 35 (20) | 4 to 20 (10) | 0.2 to 0.4 (0.3) | 0.05 to 0.1 (0.07) |
| Power-delay product (picojoules) | 30 to 150 | 10 to 60 | 15 to 80 | 0.2 to 2.0 | 50 to 500 | 5 to 50 | 2 to 40 | 0.5 to 30 | 0.1 to 0.2 | 0.01 to 0.1 |
| Typical supply voltages (volts) | +5.0 | +5.0 | -5.2 | +0.8 to +1.0 | -15 to 20 | +5.0 | +10.0 | +10.0 | +2.0 | +1.2 |
| Signal swing (volts) | 0.2 to 3.4 | 0.2 to 3.4 | -0.8 to -1.7 | 0.2 to 0.8 | 0.0 to -15.0 | 0.2 to 3.4 | 0.0 to 10.0 | 0.0 to 10.0 | 0.0 to 2.0 | 0.0 to 0.8 |
| Guaranteed noise margin (volts) | 0.3 to 0.4 | 0.3 to 0.4 | 0.125 | <0.1 | 1 to 2 | 0.5 to 2.0 | 3.5 to 4.5 | 3.5 to 4.5 | 0.2 to 0.8 | 0.2 to 0.3 |

* () Estimated for oxide-isolated processes. † Oxide isolation steps are extra.

SOURCE: Lockheed Microelectronics Center

Advanced Micro Devices Inc., Sunnyvale, Calif., has designed a 16-bit microprocessor with ECL [*Electronics*, Aug. 16, p. 42]. Both devices are up against the power-dissipation limits of ECL, and for that reason, bipolar manufacturers are at work to decrease power dissipation.

PSA bipolar needs less power

In Japan, NEC is working on the problem of high power consumption in fast bipolar circuits through the use of polysilicon. Called PSA, for polysilicon self-aligning, the process changes the usual bipolar processing entirely, even forming the interconnects at the same time as the junction. The process sequence is compared to the conventional bipolar process in Fig. 4.

According to NEC, the PSA process, which has first been used to build 4-K ECL RAMs of the 10470 variety, has everything going for it. Not only do its small parasitic capacitance and its high-value polysilicon resistors give it low power dissipation, but the self-aligning process builds gates of relatively small area— $2,000 \mu\text{m}^2$, or 3 mil²—which makes for high packing density. As for speed, no sacrifice is made; propagation delay per gate is a scant 1.58 ns. The RAM's access time is 20 ns, though it dissipates less than 500 milliwatts.

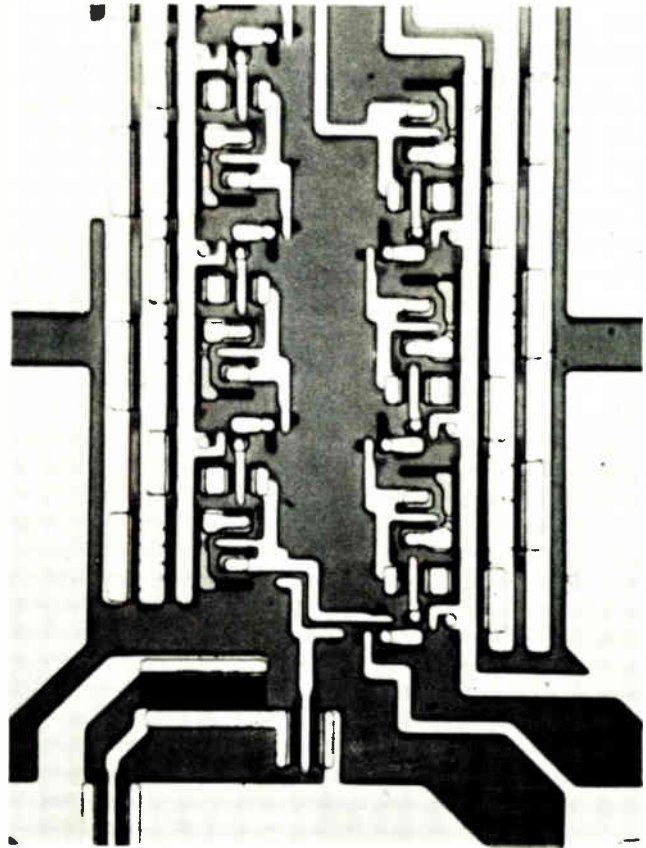
As the graph plotting propagation delay against power per gate in Fig. 5 shows, PSA stands alone. It is as fast as ECL with the power dissipation of fast n-MOS. The polysilicon does add to the process's total of 10 mask steps, compared to ECL's 8 or 9, but denser chips that can amortize the increased cost will be made using PSA.

Kenji Okada, a supervisor at NEC's first integrated-circuit design engineering department in the IC division, maintains that PSA will allow fabrication of 1-gigahertz transistors smaller and lower in power consumption than ECL. "The technology is also suitable to linear LSI," he adds. An example of such a circuit is NEC's μPB553 prescaler chip for frequency-modulation radios that works at 150 MHz. "TV is the goal for next year," Okada says. "We plan to prescale the ultra high-frequency section for digital tuning using the 1-GHz PSA process."

Few U. S. bipolar manufacturers are experimenting with polysilicon; it seems a different discipline that only MOS manufacturers have skill in. "NEC was the first to use polysilicon extensively in bipolar processing," Okada maintains. "But we don't see many others working on it." The high resistance values possible with polysilicon can cut power requirements dramatically, and it is just a matter of time before similar high-speed, low-power circuits emerge from other manufacturers.

GaAs status

The future of gallium arsenide as a standard process technology is just now beginning to become clear. (Table 2 shows the future of GaAs as it appears with respect to the current technology.) One particular form standard GaAs logic may take was recently demonstrated at Rockwell International Corp.'s science center in Thousand Oaks, Calif. It is a strong contender, as it uses relatively simple planar processing of Schottky diodes and depletion-mode (normally on) metal-semiconductor field-effect transistors to achieve high density and record-low switching energies and delay times.



6. GaAs on deck. Rockwell has recently demonstrated record low power-delay products for depletion-mode gallium-arsenide metal-semiconductor field-effect transistors. This ring oscillator built with $3\text{-}\mu\text{m}$ gates exhibits dynamic switching energies of 16 femtojoules.

The process, called Schottky-diode-FET logic (SDFL), uses extremely small (1 to $2 \mu\text{m}^2$) Schottky diodes to perform all the logic functions except inversion and gain. While much work is being done by other manufacturers on enhancement-mode MES FET devices, Rockwell has demonstrated with the ring oscillator in Fig. 6 that SDFL is not only faster—propagation delays of 136 picoseconds compared to 300 ps—but lower in switching energy—16 femtojoules versus 30 fJ, the best reported for enhancement-mode GaAs ICs.

Although SDFL was demonstrated by Rockwell almost two years ago, the company has only recently proven the logic's feasibility in medium-scale integrated circuits. Ripple counters comprising a string of D-type flip-flops have been built that operate with clock rates as high as 1.875 GHz, equivalent to a 110-ns propagation delay. In addition, divide-by-8 ripple counters comprising 25 NOR gates have been built that operate at 1.1 GHz and dissipate only 45 mW.

Logic-gate propagation delays of 100 ps are a realistic expectation for SDFL, comparable to reported delays for other depletion-mode GaAs FET IC approaches. But at 100 ps, SDFL will dissipate one hundredth the power of the other approaches. In fact, SDFL is entirely capable of extending the complexity of GaAs circuits into the large-scale integration range without sacrificing switching speed or noise margin, as do the very low-power enhancement-mode logic approaches. □

C-MOS LSI: comparing second-generation approaches

Using either isolated or ubiquitous p wells, new C-MOS processes get set for high-performance memories and analog circuits

by Donald L. Wollesen, *American Microsystems Inc., Santa Clara, Calif.*

□ As complementary-MOS circuits grew in density and silicon-gate technology emerged in the early 1970s, the first generation of large-scale integrated C-MOS was born. C-MOS LSI was initially used for watch and calculator chips, and to this day the battle in those applications between the simpler metal-gate process and the denser though more expensive silicon-gate technology yields no clear winner.

But today's memories and microprocessors demand far greater speed than watches and calculators, and for these uses silicon-gate C-MOS is clearly the victor. Products at the density level of 4-K static random-access memories, which also demand high speed, mandate an entirely new approach in process technology and device structures. Moreover, the burgeoning analog-digital LSI that mixes linear circuits with logic makes new demands in terms of performance and density.

Those demands have been answered by a second generation of C-MOS LSI. The C-MOS circuits of fast converters, microprocessors, and memories are catching up with n-channel MOS in speed while retaining the advantage of low power dissipation. Three somewhat similar approaches to this new generation have evolved, each with its own advantages.

Several reasons make it important to understand the operation of each type. One reason is that a potential second-sourcing manufacturer may be unable to build a particular process if his tooling is not compatible. Another is that anyone who contemplates a custom circuit should be fully aware of the differences, because his layout may be suitable to one technology and not to the other two. The good news, though, is that a single layout can be done to accommodate all three.

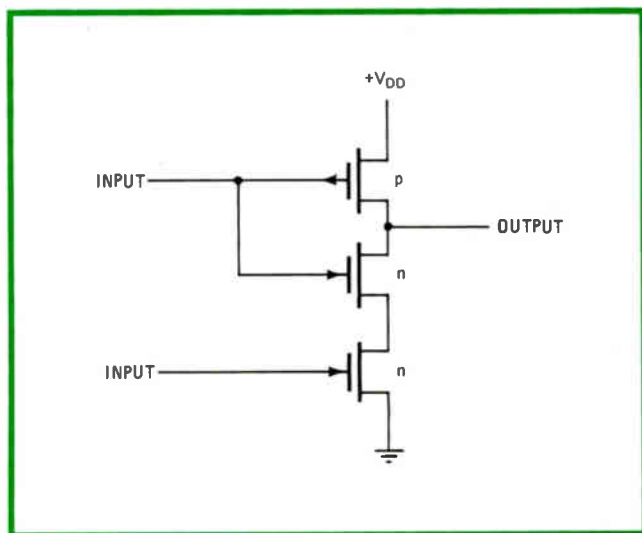
The second generation

Looking at a portion of a C-MOS gate (Fig. 1) will be helpful in comparing the three C-MOS approaches. Simple plan-view and section drawings illustrate the differences; for all examples, the line width and spacing rules are consistent, so that a comparison in gate layout area may be made.

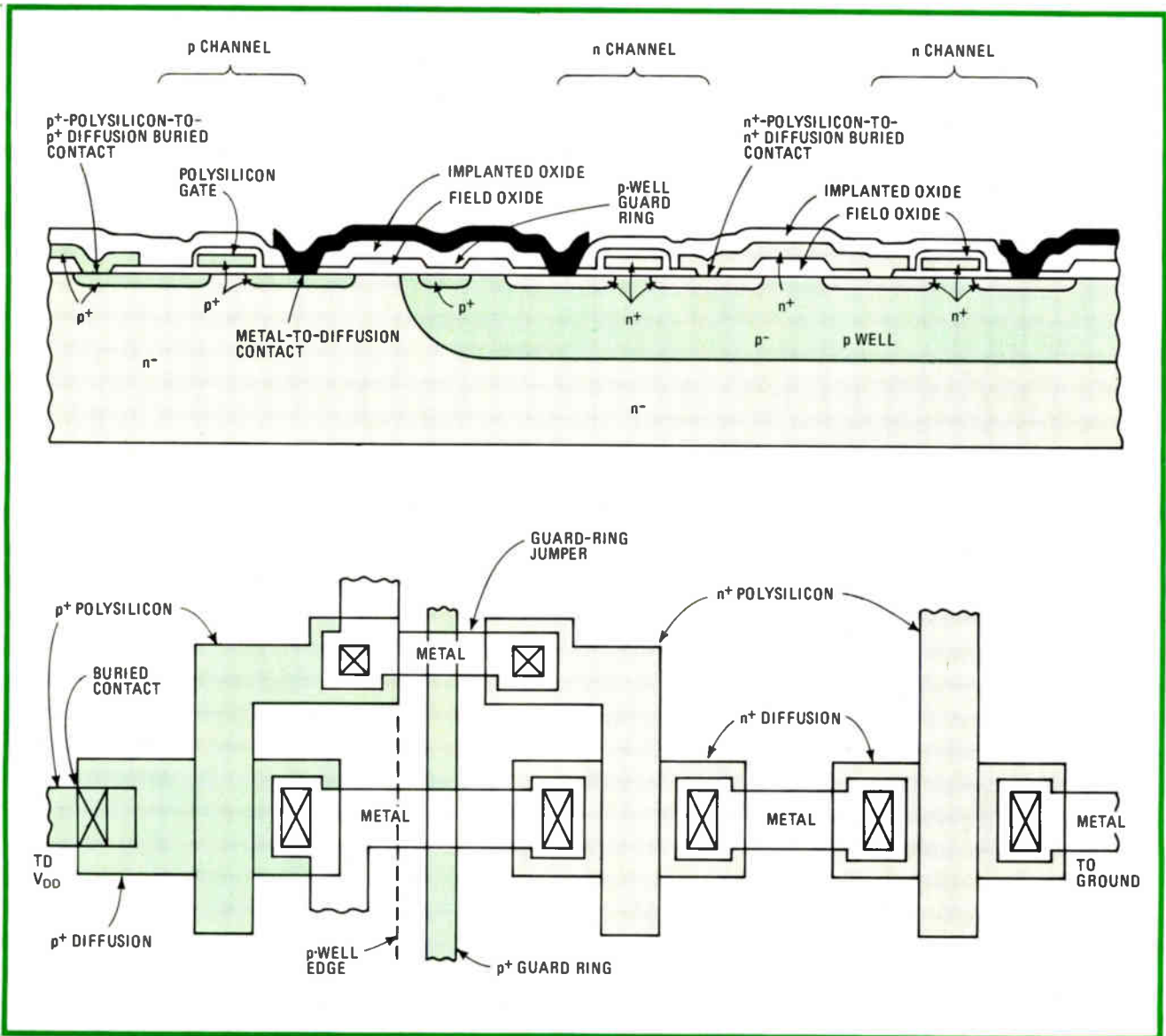
The first implementation of the gate portion is a process that uses both n⁺ and p⁺ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added. (At American Microsystems Inc., the selective field-oxidation process is used only to shrink existing designs down to 5-micrometer rules; it is not applied to new designs.)

Figure 2 shows the plan and section views of the three-device gate portion. Because the p well in the top view spans both n-channel devices, it is referred to as ubiquitous, and the process is called ubiquitous p well.

In this planar process, p⁺ guard rings are used to reduce surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of n⁺ polysilicon in the p-channel areas. The plan view shows the construction of the bridges linking p⁺ to



1. Gate portion. This simple portion of a gate will serve to compare C-MOS layouts. Two series n-channel transistors mark a key difference between the approaches, which either put all n-channel devices in a single p well or give each device its own well.



2. Two-polysilicon approach. The first high-performance complementary-MOS process upgraded earlier designs for 5- μm geometry. Its drawbacks: two types of polysilicon are used, and the unavailability of field implant doping ties field threshold to device thresholds.

metal to n^+ . (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect n-channel and p-channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n^+ polysilicon to n^+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available C-MOS vendors.

The planar process of n^+p^+ ubiquitous p well is a disadvantage in that it precludes field-implant doping. The result is that the field threshold voltages are

unavoidably linked to device thresholds. For example, if the gate-oxide thickness is 1,200 angstroms for a device with a 1-volt threshold, then a 12,000- \AA field oxide fixes the field threshold at approximately 10 v. That dependency constrains the process designer, since low device thresholds will force low field thresholds—field oxide cannot be made much thicker than 15,000 \AA without ensuing step-coverage problems.

Nor does the process lend itself to small-geometry devices. The gate oxide cannot be made too thin lest a phenomenon called boron penetration occur. Thin oxides allow boron from the p^+ doped polysilicon in the p-channel device to diffuse through the gate oxide to the channel region, causing thresholds to be changed so radically that sometimes the enhancement-mode transistor actually turns into a depletion-mode device—highly undesirable for complementary-MOS.

The second-generation C-MOS approach that offers the most advantages uses a selective field-oxidation process

and requires only n^+ polysilicon. The selective field-oxidation process (referred to as Isoplanar or Planox by certain manufacturers) is preferable, since it not only eases metalization step coverage, but also allows for field implantation, so that field thresholds are not tied to device thresholds.

The n^+ -only approach

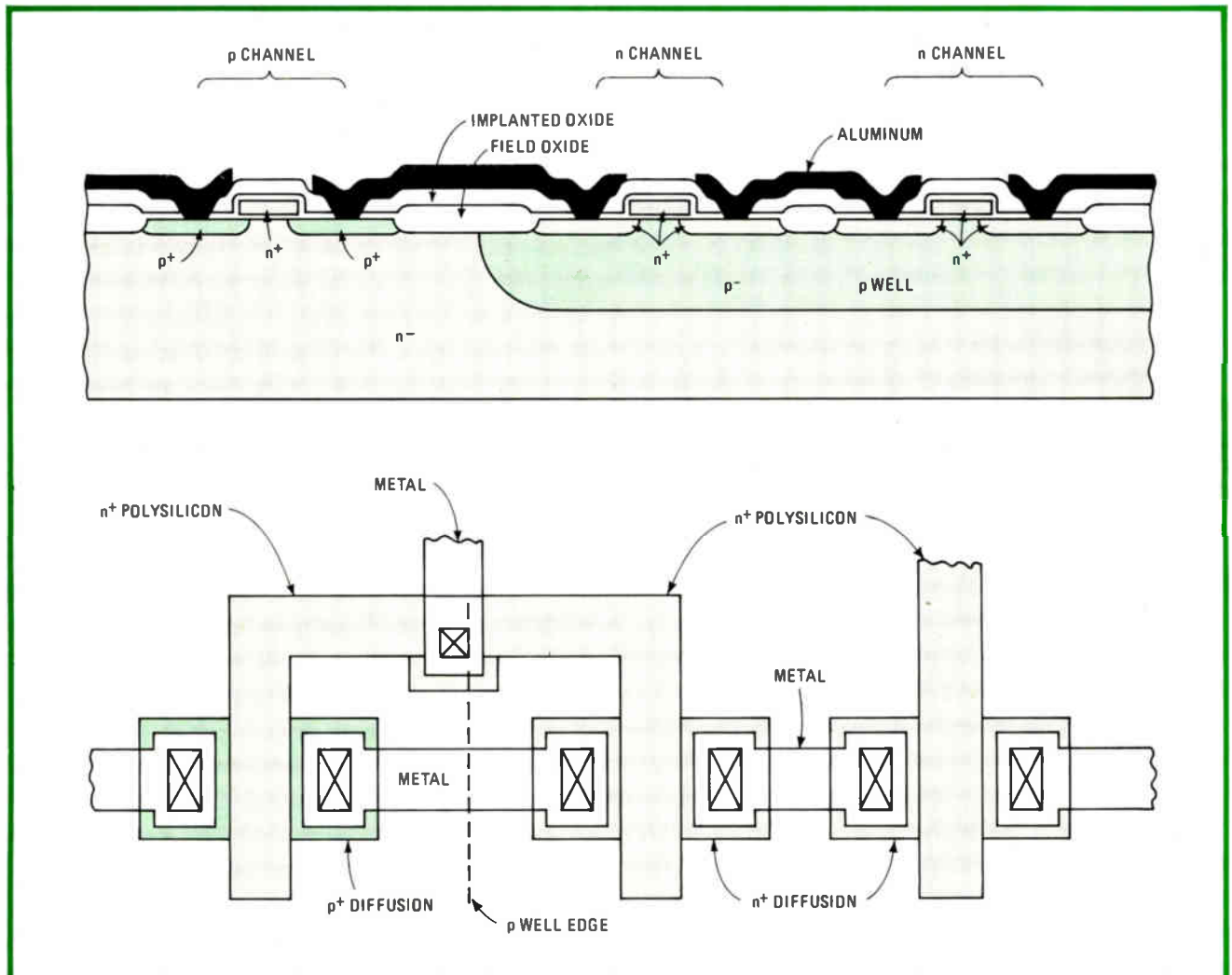
Both of the second-generation C-MOS processes that follow are variants of the n^+ -only, selective-field-oxide approach. One closely resembles the p^+n^+ ubiquitous-p-well process, since it, too, has a ubiquitous p well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated p well, has separate wells for each n-channel device that are implanted after field oxidation.

Figure 3 shows the section and plan views of the

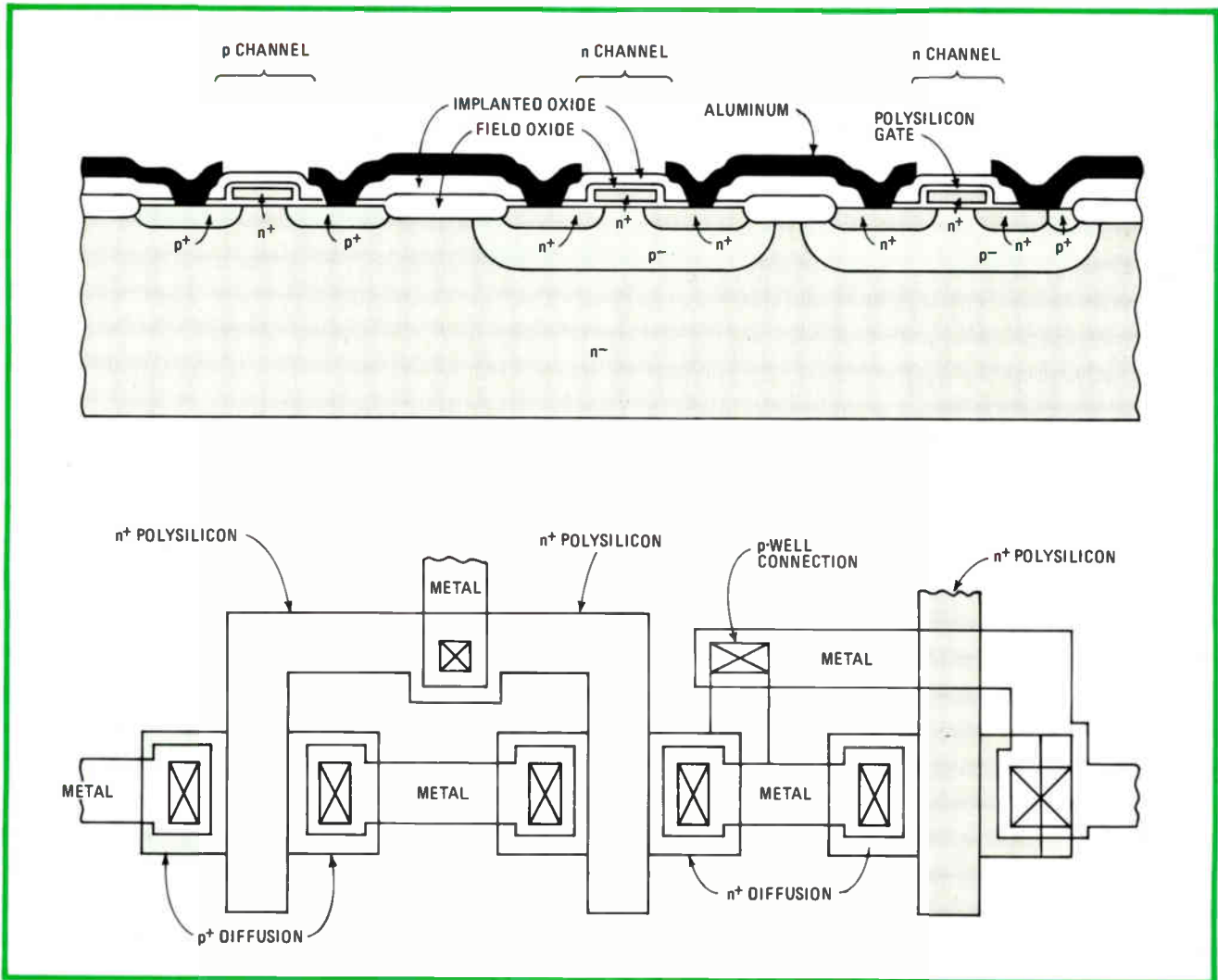
n^+ -only ubiquitous-p-well approach used to build the partial gate of Fig. 1. This is the $5\text{-}\mu\text{m}$ process recommended by AMI and others for new, high-performance C-MOS designs. The layout is simpler than with the two-polysilicon ubiquitous-well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required. Polysilicon can thus cross directly from p- to n-channel device areas without the need for bridges or polysilicon-dioxide contacts.

Note that all polysilicon is n^+ , even in p-channel devices. Because of that, however, a buried contact between n^+ polysilicon and p^+ diffused areas is impossible. Moreover, even though a buried contact between n^+ polysilicon and n^+ diffused silicon is possible, the benefit rarely outweighs the cost of the extra mask step, and therefore the contact is usually unavailable in this type of process.

The problem of boron penetration is eliminated because all polysilicon is doped with phosphorus. Consequently, the process makes possible thinner gate oxides than the two-polysilicon approach, and that means tran-



3. One-polysilicon approach. All new high-performance C-MOS circuits will use one type of polysilicon. This version has a ubiquitous p well; that is, series n-channel devices sit in a common p well, which, implanted before field oxidation, runs under the field oxide.



4. Isolated wells. The third C-MOS approach isolates all n-channel devices in separate p wells. Since the isolated wells must be doped much more heavily than those of the ubiquitous-well approach, n⁺-to-p-well capacitance is greater and switching speeds lower.

sistors can have higher gain and lower threshold voltages with no adverse effect on field thresholds. On the other hand, thanks to field implants, field threshold voltages can be made higher with no direct effect on transistor thresholds. Since the field oxide is selectively grown, fairly thick field-oxide regions can be obtained without paying the penalty of the precipitous oxide steps found in planar approaches.

A variant of the all-n⁺ polysilicon process just discussed uses basically the selective field-oxide approach except that the p wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the p wells are naturally isolated from one another, the process is called n⁺ isolated p well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p⁺ diffusions or with top-side metalization that covers a p⁺-to-p-well contact diffusion.

In the isolated-well process, the p wells must be doped much more heavily than in the ubiquitous-well process. One result is a higher junction capacitance between the n⁺ areas and the wells that both slows switching speeds

and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

Although currently available from AMI and other manufacturers, the isolated-well process is in fact not recommended for new designs by AMI. Its layout takes up more area than does one using the ubiquitous-well approach, even though its p-well-to-p⁺-area spacing is slightly less.

Compatibility is key

A layout with the isolated-well approach appears to almost guarantee process compatibility with the ubiquitous-well approach. However, there are two hitches: first, the ubiquitous-well approach needs about 5 μm more space between n-channel and p-channel transistors; second, p wells in the isolated-well approach will often be purposely separated using only the field mask, thereby linking the wells to one another if the mask set is used with the ubiquitous p-well process.

Though the former presents no serious layout-compatibility problems, the latter could in practice prove trou-

biesome. Consider, for example, a circuit requiring that the isolated wells not both be tied to ground but instead be operated at different potentials. That could be accomplished only if both the p-well and field-oxide masks are used. Figure 5 shows such a situation and how it can be handled. The rule is that if the p-well mask is merged (that is, the wells are not separated) in the isolated-well process and isolation accomplished only with the field mask, the process will not be compatible with the ubiquitous-well process.

Table 1 summarizes the major layout concerns for process compatibility. The most versatile layout would:

- Eliminate buried contacts.
- Include polysilicon-diode contacts.
- Use layout rules of the ubiquitous-well process.
- Assume the isolated-well process.
- Make contact to all isolated p wells.

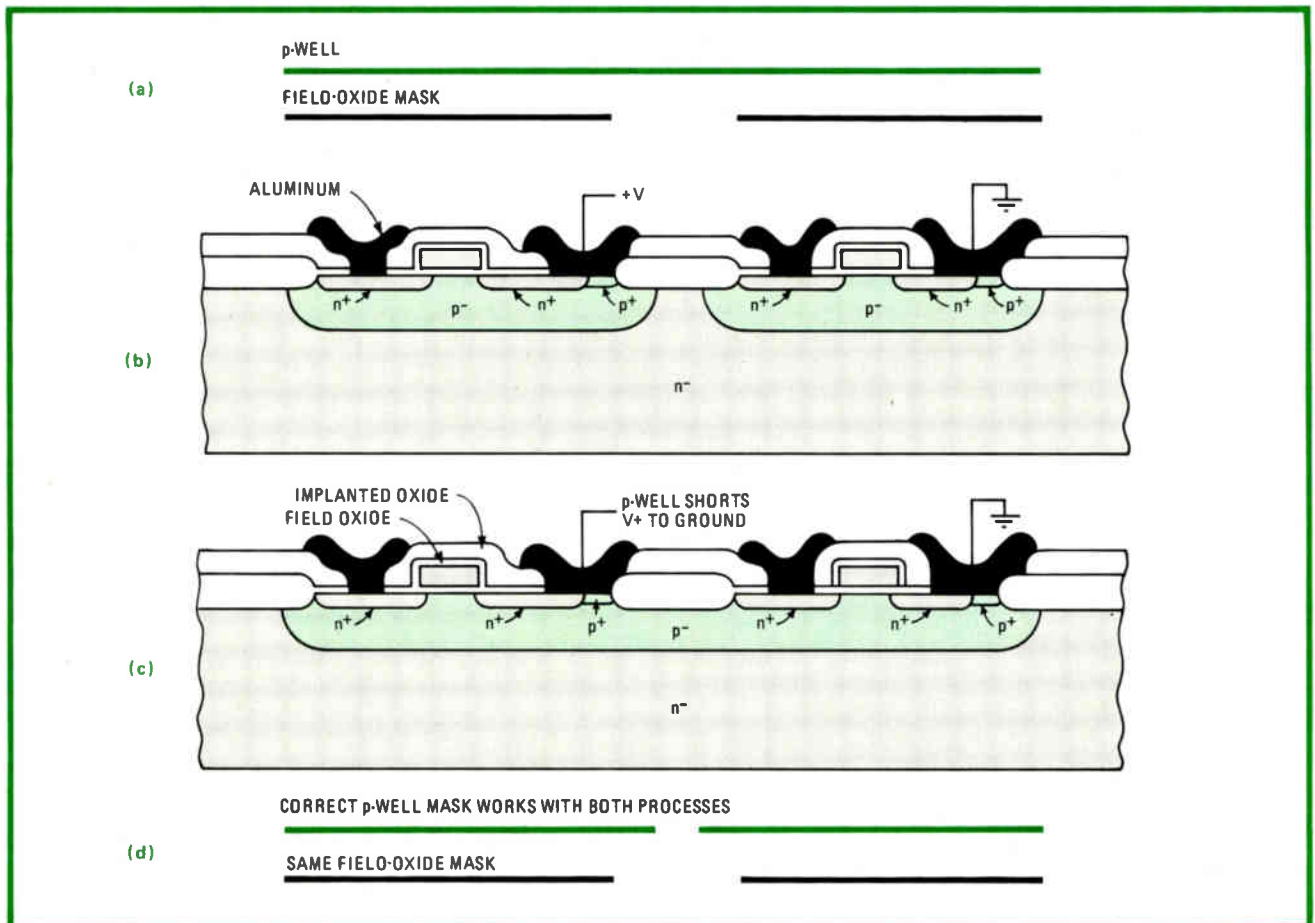
The circuit takes up more area using the versatile layout approach, but it may be a small price to pay for compatibility.

Comparing the density of different processes is more a

sport than a science; a manufacturer who wants to prove his process is better can present his design rules in the best light but is unlikely to do the same for his competitors' approaches. Here, though, the simple cells shown all have the same 5- μm line widths and spacings, as was noted earlier.

In all fairness, it must be pointed out that the gate portion of Fig. 1, from which the data in Table 2 was derived, was chosen to illustrate a compatibility risk between processes. In practice, a designer would not use series n-channel devices in the isolated-well process because such an arrangement occupies more area than other circuits and because in this process the body effect, which slows circuit speed, is particularly pronounced in n-channel devices. Also, the n⁺ regions between the two n-channel devices would be merged, instead of using a metal or polysilicon jumper. In general, therefore, it is fair to regard the densities of both n⁺-only processes as roughly equal.

It should also be pointed out that certain types of circuits tend to favor different layout schemes. For example, in the classic six-transistor static random-access memory cell, the buried contact that is available in the two-polysilicon process actually reduces cell area by about 5%. Fabrication costs, however, are higher because of the extra mask step required by buried contacts, and that offsets the area advantage.



5. Compatibility. If p wells are isolated only with the field-oxide mask (a), the isolated-well (b) and ubiquitous-well (c) processes are compatible—but the power supply could short to ground if the wells are at different potentials. Solution: use the p-well mask, too (d).

TABLE 1: LAYOUT COMPATIBILITY CONCERNS FOR C-MOS PROCESSES

| Layout feature | n ⁺ /p ⁺ polysilicon ubiquitous p well | n ⁺ -only polysilicon ubiquitous p well | n ⁺ -only polysilicon isolated p well |
|---|--|--|--|
| Buried contact | X | no | no |
| Polysilicon diode contact | yes | X | X |
| p well isolation with diffusion mask | no | no | yes |
| Tight p-well-to-p ⁺ spacing | no | no | yes |
| Layout care required for p-well electrical contacts | no | no | yes |

X = does not matter

TABLE 2: COMPARING AREAS FOR C-MOS PROCESSES

| Process | Area (mil ²) | Area (percentage) | Number of masks |
|---|--------------------------|-------------------|-----------------|
| n ⁺ /p ⁺ polysilicon ubiquitous p well (Fig. 2) | 4.1 | 114 | 9-11 |
| n ⁺ -only polysilicon ubiquitous p well (Fig. 4) | 3.6 | 100 | 8-9 |
| n ⁺ -only polysilicon isolated p well (Fig. 5) | 4.0 | 111 | 8-10 |

Note: All processes done with 5- μ m lines and spaces

TABLE 3: COMPARING PERFORMANCE OF SINGLE C-MOS INVERTERS

| Process | Rise time (ns) | Gate power-supply current (μ A) | Speed-power product (pJ) |
|--|----------------|--------------------------------------|--------------------------|
| n ⁺ /p ⁺ polysilicon ubiquitous p well | 2.4 | 900 | 10.8 |
| n ⁺ -only polysilicon ubiquitous p well | 1.4 | 900 | 6.3 |
| n ⁺ -only polysilicon isolated p well | 1.4 | 1,300 | 9.1 |

Notes: All processes use 5- μ m lines and spaces. Data is based 13-stage ring counters.

The n⁺-only ubiquitous-well process uses the fewest number of masks, is the simplest to lay out, and takes up the least area in most cases. It is therefore the most cost-effective C-MOS process available today.

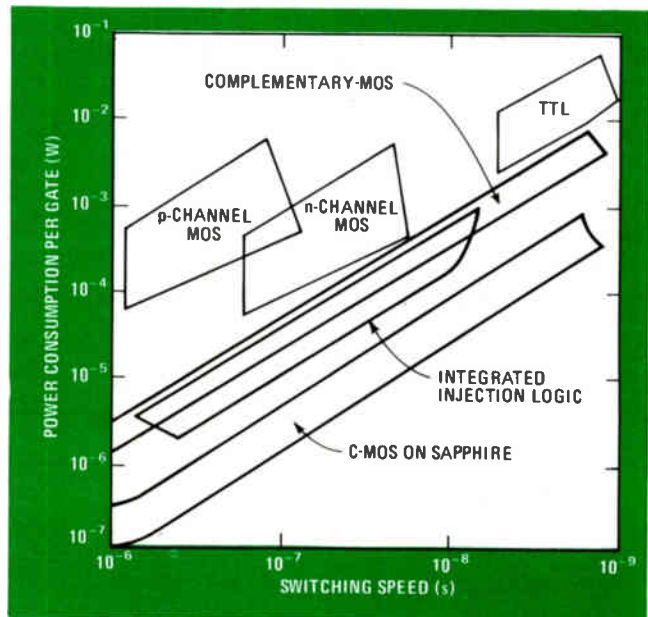
Whereas the first generation of C-MOS LSI was applied to products that demanded low power consumption—watches, calculators, and military gear—the second generation is beginning to change that situation. The new C-MOS LSI will certainly make inroads into places where C-MOS has not been used before, such as large memories of all types. Moreover, it will build microprocessors of the same complexity and capability as existing n-channel parts and—besides being much lower in power consumption—will be faster. Performance figures of 5- μ m C-MOS approaches are shown in Table 3.

Critics of C-MOS technology argue that although it can be fast and draws very little standby power, at top speed it draws considerable power. Actually, that dependence can be used to advantage: higher speed does incur power costs, but since C-MOS automatically reduces its power as the switching speed goes down—it is the only technology to do so—the choice is left to the user.

Comparative judgments

Figure 6 compares several technologies in switching speed versus power consumption. It is, however, based on the performance of a single-input inverting gate; every gate in the system would have to be toggling at maximum rate for an extrapolation of gate-level performance to system-level performance. But it at least gives an idea of relative performance. C-MOS does tend to slow down as a function of the number of gate inputs—for a single-gate switching speed of 2.5 nanoseconds, a four-input gate would switch in about 10 ns—but with only a slight penalty in power dissipation.

The data is based on 5- μ m technologies operated at 5 V. It is worth noting that, from the standpoint of speed, 5- μ m bulk silicon matches 5- μ m C-MOS on sapphire. The reason is that although bulk C-MOS exhibits far greater junction capacitance, C-MOS on sapphire is limited in its majority-carrier mobility, which holds it to a lower gain constant for a given device. Still, C-MOS on sapphire



6. Energies. This comparison of switching energies (based on performance of a single 5- μ m gate) shows bulk C-MOS equal in speed to C-MOS on sapphire. The former's junction capacitance is offset by the latter's losses in majority-carrier mobility.

retains a substantial advantage in gate power. However, it may not yield any advantage at a system level because its standby leakage current is much higher. Also, it is a very expensive technology. Still, C-MOS and C-MOS on sapphire are the only technologies that dissipate power only on logic transitions.

Integrated injection logic is a constant loss-load technology, unlike C-MOS—high speed is traded off against low power by the designer. I²L has a broad speed-power band, but it follows the entire speed-power curve only if its bias current is changed from standby to active, something that is not usually done in small systems.

The inherent standby attribute of static C-MOS technology is one of its greatest strengths from a system standpoint. Consider an 8-bit microprocessor with 16-K bytes of RAM. Because the microprocessor can perform

THE NEW PROCESSES

only one address operation at a time, 16,383 bytes of memory do nothing but remember while 1 byte is being accessed. Moreover, in most cases any peripheral interfacing circuits will also be having to wait while memory is being accessed.

Current comparison

Table 4 compares the currents required for C-MOS, n-channel (2114 type), and n-channel power-down memories, based on the assumption that the 16-K bytes of memory are made up of 32 4-K-by-1-bit static RAMs. At any given time, 8 chips are active and 24 are inactive. The memory system's total current, which is the sum of the standby and active currents, is 30 times greater with n-channel than with C-MOS RAMs. Even power-down n-channel RAMs, which are not often used in microprocessor systems because the cost or the increased system complexity is rarely worth the trouble, draw almost nine times as much current as C-MOS.

C-MOS is the only logic form that operates in an automatic power-down mode. Even if I^2L static RAMs were available commercially, they would at best compete with edge-triggered n-channel RAMs and would probably have similar operating currents; only the standby currents would be less than with n-MOS.

Although the world of linear integrated circuits is currently dominated by bipolar technology, C-MOS has

invaded such LSI devices as digital-to-analog and analog-to-digital converters, coder-decoders (codecs), and most dramatically, fixed filters using switched-capacitor designs.

There are two main reasons why MOS technology in general has been unable to compete with bipolar circuits in the field of linear ICs: offset voltage and noise. For a matched dual-input transistor pair, bipolar transistors have about 0.5 millivolt of offset voltage, whereas MOS devices often match so poorly that their offset is 10 mV or more. Similarly, $1/f$ noise at 100 hertz is about 20 nV/Hz^{1/2} as against 500 nV/Hz^{1/2} for the MOS device pair.

However, certain circuit techniques have made possible the development of competitive linear circuits, despite those noise and offset handicaps. As an example, the 5- μ m n⁺-only ubiquitous-p-well process has been used to build an operational amplifier competitive in performance with the general-purpose bipolar types. Table 5 compares the internally compensated C-MOS op amp with its bipolar counterpart, the popular 741. Figure 7 is a photograph of an oscilloscope showing the C-MOS op amp's large-signal unity-gain output response. Note that, unlike the case with a 741, the positive and negative slew ramps are nearly equal and are well behaved.

Converting

Other circuit design tricks have allowed C-MOS to work around the shortcomings of its linear-circuit performance. The best example is in a-d conversion. There, analog signals are quantized, and as long as the exact value of the signal is known at the end of the quantizing period—the most accurate quantization

The complexity of C-MOS

Historically, complementary-MOS has been the most complex MOS technology; since p-channel and n-channel MOS technologies each use only one device type, they would naturally build lower-cost circuits. Over time, the drive for increased performance has de-emphasized p-MOS. But the combined demand for higher density and a lower power-delay product has jacked up the process complexity of n-MOS.

The techniques used by circuit designers to reduce the power-delay product have, in fact, raised the complexity of n-MOS processes to the level of C-MOS technology (see the table). One way is by boosting speed with circuits that combine devices of several different thresholds—a few enhancement types, a few depletion types, and even devices with 0-volt thresholds—which require extra mask and implant steps.

Another, the use of clocked, or dynamic, circuit design, is aimed at reducing power consumption. Clocked logic definitely reduces power dissipation, but it also increases circuit complexity. What's more, because the attendant clock lines must run throughout the chip, clocked logic sacrifices density. Clocked n-channel logic is not as fast as and dissipates more power than C-MOS of equivalent line width. Thus, compared with past circuits, the area and cost penalties for going to C-MOS in today's high-performance world are continually growing smaller.

Another advantage of C-MOS coming to light is that for gate lengths of 5 micrometers or less, device modeling is more accurate than in n-MOS and therefore circuit simulations fit actual circuit performance better. The result is not only lower cost for circuit development, but greater ease in predicting development time and adhering to a schedule—simply because the C-MOS circuit is more likely to work the day it is supposed to without redesign or process adjustments.

Of course, more closely controlled development time is especially important to custom-circuit scheduling. Indeed, computer-aided simulation techniques will become increasingly important as circuits graduate in density to the very large-scale integration level.

COMPARING THE COMPLEXITY OF C-MOS PROCESSES

| | Line width (μ m) | Number of masks | | |
|------|-----------------------|----------------------------|----------------------------|--------------------------------|
| | | Silicon-gate p-channel MOS | Silicon-gate n-channel MOS | Silicon-gate complementary MOS |
| 1973 | 7.5 | 5-7 | 5-7 | 8-9 |
| 1975 | 6 | 6-8 | 6-8 | 8-9 |
| 1977 | 5 | — | 7-9 | 8-10 |
| 1979 | 3-4 | — | 8-10 | 8-10 |

TABLE 4: CURRENT REQUIREMENTS OF 16-K BYTES OF RANDOM-ACCESS MEMORY (mA)

| Technology | Standby | | Active | | Total |
|-----------------------------|-----------|----------|-----------|---------|-------|
| | Each chip | 24 chips | Each chip | 8 chips | |
| C-MOS | 0.005 | 0.12 | 5 | 40 | 40 |
| N-channel | 35 | 840 | 45 | 360 | 1,200 |
| N-channel (with power-down) | 3 | 72 | 35 | 280 | 350 |

Note: All memory elements are 4-K-by-1-bit static RAMs.

TABLE 5: COMPARING C-MOS AND BIPOLAR OPERATIONAL AMPLIFIERS

| Parameter | C-MOS op amp | Bipolar (741 type) |
|----------------------------------|--------------|--------------------|
| Offset voltage (typical, mV) | 6.3 | 1.0 |
| Offset current (typical, nA) | <1 | 20 |
| Bias current (typical, nA) | <1 | 80 |
| Power-supply voltage (V) | ±5 | ±15 |
| Power-supply current (mA) | 0.5 | 1.4 |
| Output voltage swing (V) | ±4.5 | ±13 |
| Open-loop gain (dB) | 96 | 106 |
| Common-mode rejection ratio (dB) | 66 | 70 |
| Slew rate (V/μs) | 10 | 0.5 |
| Cell area (mil ²) | 172 | 1,100 |

occurs at the exact end of the sample period—what goes on between the beginning and the end of the period is immaterial. C-MOS can make good use of that time between samples.

An example of what can be performed during the sample period is reset stabilization of an op amp. By measuring the offset voltage of the op amp, storing that voltage value on a capacitor, and then algebraically subtracting the potential on the capacitor from the offset error of the op amp during the quantizing period, an op amp with extremely low offset voltage, regardless of temperature, can be built.

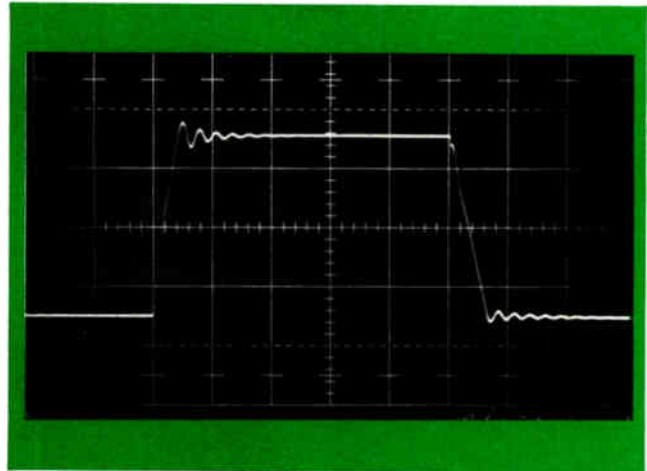
The technique is a viable one that has already been used in codecs. There, a 3.3-kilohertz voice bandwidth is used, and the sampling frequency is 8 kHz. Thus the analog signal is quantized every 125 microseconds, and there is enough time between quantizing periods to perform the reset stabilization.

That technique is extremely important in telephony, because it allows the offset voltage to be lowered to less than 1 microvolt over the entire temperature range, and it reduces 1/f noise at 100 Hz. Since the principal contribution to 100-Hz 1/f noise is in the region where the 1/f corner frequency falls for MOS devices—around 8 kHz—sampling at that rate neatly sidesteps the inherent noise problem of MOS transistors.

C-MOS or n-MOS

As for whether n-channel alone or C-MOS builds better linear circuits, there is a good historical comparison in the history of bipolar linear devices. The 709 op amp was built using only npn transistors. Compared with the 741 and the 101A, which use both npn and pnp transistors, the 709 is vastly inferior.

Likewise, an n-MOS op amp will simply not perform as well as an op amp that uses both n-channel and p-channel devices. One good reason is that p-channel



7. C-MOS linear. C-MOS is proving itself in linear circuits as well as digital. Here, the large-signal unity-gain output response of a C-MOS operational amplifier shows equal, well-behaved positive and negative slewing ramps—unlike those in the bipolar 741.

transistors are required for building current mirrors referred to the positive voltage supply. The lack of a good current mirror is a serious handicap for the n-MOS circuit designer.

Switched-capacitor and charge-coupled-device filter techniques are available in both n-MOS and C-MOS for building high-pass, low-pass, and bandpass filters from audio to video frequencies, a feat that bipolar technology will have difficulty matching. Interestingly, the area penalty that C-MOS pays versus n-MOS in digital designs is actually reversed in these applications. Despite smaller actual transistors in n-MOS, because fewer circuit elements are available and so many more devices are required, n-channel linear circuits take up more real estate than C-MOS.

Other pluses

Other elements, too, are available in the C-MOS process—for one, zener diodes, which can regulate power-supply voltages on chip. That is a boon for digital applications in which power-supply regulation is poor, as in automotive circuits. Zeners can also protect a chip from voltage surges, and they serve in linear circuits as voltage references. The zener reference diodes in AMI's C-MOS processes have been designed with an avalanche of just under 6 V.

Also inherent in the C-MOS process is a bipolar device. The p well serves as a base region, an n⁺ diffusion as an emitter, and the substrate as the collector. Because the collector is tied to the substrate, the transistor is limited to an emitter-follower configuration, but it is a handy device nonetheless. The npn transistor has a breakdown voltage of over 50 V and, depending on the geometry used, a gain (h_{fe}) of 50 to 300.

One use for the built-in npn device is an output-stage pull-up transistor. Since it supplies more current for a given topological area than a p-MOS transistor, it takes up less die area for a given drive capability. A pair of transistors can even be used as a bandgap voltage reference, offering the designer the choice of zener or bandgap techniques in the same process. □

HMOS II static RAMs overtake bipolar competition

Shrinking process comes up with improved access times, new production remains compatible with HMOS fabrication

by R. M. Jecmen, C. H. Hui, A. V. Ebel, V. Kynett, and R. J. Smith, *Intel Corp., Santa Clara, Calif.*

□ MOS devices have pushed aggressively towards higher performance and density during the past decade. This work has taken MOS from a relatively slow, low-density technology to a leadership position in random-access memory performance. For the first time, with the introduction of static RAMs fabricated in HMOS II, n-channel MOS achieved a superiority in access time over bipolar, while maintaining its advantages of low power dissipation and the ability to power down.

A number of different technological improvements have contributed to the MOS cause over the years (see "The evolution of MOS," p. 127). But the main differences between this second generation of the Intel HMOS process (the H is for high performance) and its immediate ancestors have to do with device scaling. To understand its key features requires an understanding of basic scaling theory.

Scaling

Figure 1 illustrates several of the device dimensions critical to scaling theory. Generally, to maintain the characteristics while shrinking an MOS device, all of the physical dimensions—channel length (L), gate-oxide thickness (T_{ox}), junction depth (X_j), and lateral diffusion of the source and drains under the gate (L_D)—must be reduced by the scaling factor $1/K$. At the same time, threshold and punchthrough voltage levels are maintained by increasing the substrate doping concentration by a factor of K and reducing the power-supply voltage by a factor of $1/K$.

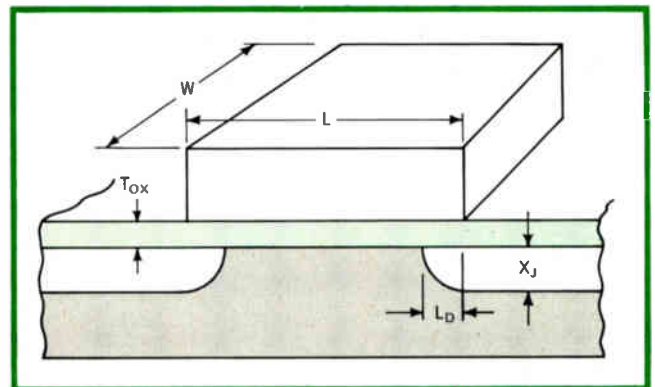
HMOS II does not follow scaling theory exactly, however. Since industry compatibility demands that the supply voltage not be scaled down from the standard 5 volts, deviations from first-order scaling theory were necessary. To be sure, the impact of maintaining a 5-v supply is significant. All of HMOS II's deviations from scaling theory (Table 1) originate from three effects intrinsic to maintaining the 5-v supply voltage.

First, reduced dimensions result in more intense electric fields, so channel doping concentrations must be

increased by a factor of αK (where α is greater than 1) to prevent device punchthrough. Secondly, the scaled MOS structure has higher gain, which produces higher currents per unit width. HMOS II takes advantage of this increased current drive by scaling channel width (W) by αK rather than simply by K . Finally, the constant supply voltage has a major impact on the power dissipation and power-delay product of a technology. Whereas scaling theory predicts that the power-delay product and power dissipation would drop by $1/K^3$ and $1/K^2$ respectively, a constant 5-v supply allows a less dramatic reduction of $1/\alpha K$ for the power-delay product—and no change in power dissipation.

New lows

By scaling the active transistors down to gate lengths of 2 micrometers and oxide thicknesses of 400 angstroms, HMOS II achieves a minimum gate delay of 400 picoseconds and a power-delay product of 0.5 picojoule. As shown in Fig. 2, the figures represent a scaling factor of 3 compared to 1976 industry-standard MOS



1. MOS scaling. The basic operating characteristics of MOS devices can be maintained if all dimensions—channel length (L) and width (W), oxide thickness (T_{ox}), junction depth (X_j), and lateral underdiffusion (L_D)—are reduced in the same proportions, while the substrate doping concentration is increased by that proportion.

technologies. The performance improvement, however, is nearly tenfold.

Much of the HMOS II development centered on optimizing the scaling parameters. The emphasis was on boosting speed instead of density, but rapid development of a commercial product was deemed equally important. Therefore, HMOS II was designed to use most of the same process steps as HMOS; only those process blocks critical to switching speed were modified. Limiting engineering development to the scaled MOS transistor resulted in a very short turnaround time for the new process, with minimum impact on manufacturing.

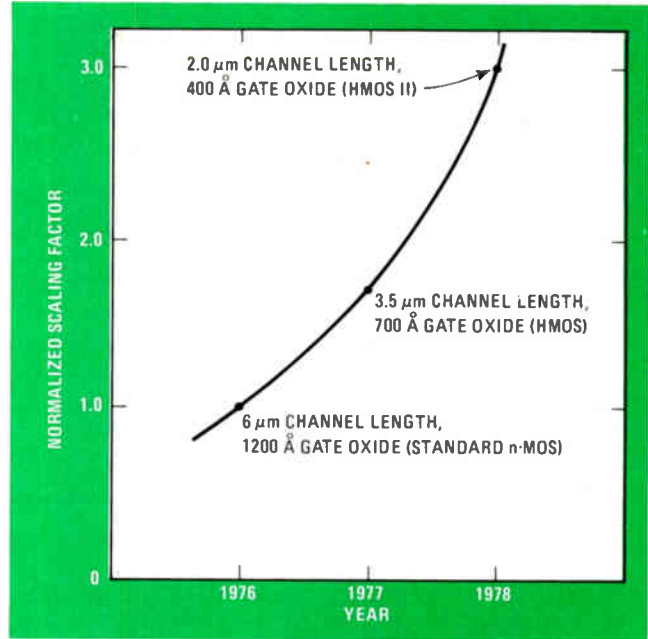
The performance improvement did not add significantly to process complexity or expense. Since HMOS techniques are used for all major process blocks of HMOS II except the active transistor definition (Table 2), the compatibility of HMOS II with existing HMOS manufacturing lines is excellent. Even the finer transistor definition does not require any major modification to the existing production process or equipment. The 2- μm gate lengths are generated with standard optical photolithography and etching techniques. Moreover, the first HMOS II parts use the same single-level polysilicon depletion-mode transistors for loads as the HMOS parts. These keep process defect levels low and avoid the manufacturability and potential reliability problems of polysilicon-load approaches.

Soft errors pose a potential reliability problem for static RAMs that use polysilicon loads, which have been shown to be sensitive to alpha radiation. Alpha-induced errors are inversely proportional to cell capacitance and load current, and polysilicon resistors significantly reduce both compared to depletion-load approaches. Great care must therefore be taken in cell design and processing of polysilicon-load technologies. HMOS II static RAMs have depletion loads, and accelerated testing using high-dose sources of alpha radiation have shown a zero failure rate per 1,000 hours.

Short channels revisited

The short lengths and high electric fields associated with HMOS II do have an impact on MOS device characteristics that goes beyond the first-order scaling theory. Besides the increased gain of the scaled MOS device, a number of short-channel effects occur that must be characterized in detail to optimize any design for HMOS II. Two of the effects are also apparent in HMOS.

Both threshold voltage and source-to-drain punch-



2. Progress. Recent improvements in processing have enabled the scaling to 2- μm channel lengths and 400-angstrom oxide thicknesses in HMOS II. The scaling factor of 3 relative to 1976 standards represents an eightfold drop in power-delay product.

through voltage are inversely proportional to channel length for devices with the shortest channels. As with HMOS, those effects are a result of the drain voltage affecting the turn-on characteristics of the channel. Falling threshold voltage with rising drain voltage or decreasing channel length is a result of the electric field region around the drain depleting part of the channel charge. Thus a lower gate voltage is necessary to form the channel inversion region. Punchthrough voltage characteristics for HMOS II show the same second-gate effect seen with HMOS [*Electronics*, Aug. 18, 1977, p. 94]. In this case, the drain field inverts the channel from the terminated field lines at the oxide-silicon interface. HMOS II prevents each of these short channel effects from becoming catastrophic by scaling down the gate-oxide thickness (thereby reducing the impact of the second gate) and by increasing the channel doping concentration to a greater extent than the scaling factor.

Add velocity saturation

Another short-channel effect that only begins to show at those fields and channel lengths used in HMOS II is one

TABLE 1: DEVICE SCALING APPROACHES

| Device parameter | Scaling factor | |
|----------------------------------|----------------|--|
| | Theoretical | HMOS II approach |
| Device dimension T_{OX} , L, W | 1/K | 1/K ($K_W = \alpha K$), $\alpha > 1$ |
| Doping concentration | K | αK |
| Voltage | 1/K | 1 |
| Current | 1/K | ~ 1 |
| Capacitance | 1/K | 1/ αK |
| Propagation delay | 1/K | 1/ αK |
| Power dissipation | 1/ K^2 | 1 |
| Power-delay product | 1/ K^3 | 1/ αK |

TABLE 2: COMPARISON OF HMOS AND HMOS II TECHNOLOGIES

| Characteristic | HMOS | HMOS II |
|----------------------|-------------------|-------------------|
| Gate thickness | 700 Å | 400 Å |
| Gate length | 3.5 μm | 2.0 μm |
| Isolation definition | | unchanged |
| Contact definition | | unchanged |
| Metal definition | | unchanged |
| Layout density | | 120% of HMOS |
| Gate delay | 1 ns | 0.4 ns |
| Power-delay product | 1 pJ | 0.5 pJ |

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that reduces the drain-to-source current. Called velocity saturation, it occurs when the electric fields become high enough to excite electrons moving from the source toward the drain to higher energies than the equilibrium thermal energy of the silicon lattice. At these high energies, electrons interact with the optical phonons instead of with the acoustic phonons as is normal; because of this, the electrons lose energy more rapidly. The net result is a saturating of average electron drift velocity at high electric fields, with the consequence that

increasing channel fields actually reduces mobility.

When the MOS transistor operates in the saturation region, its channel is pinched off and the potential drop becomes a function of $V_{GS} - V_T$, where V_{GS} is the gate-to-source voltage and V_T is the threshold voltage. Velocity saturation will limit the rise in drain current with increasing gate voltage to a linear function instead of the normal square function. This result is illustrated in Fig. 3, which shows the current-voltage characteristics of a normal MOS device and one in velocity saturation. The compression of the current-voltage curves at high gate voltages is direct evidence of the reduction in mobility occurring as a result of electron-phonon interaction.

The impact of velocity saturation is the reduction in current gain of an HMOS II transistor. This works against the original intent of device scaling, since larger devices

The evolution of MOS

No fewer than four major changes in MOS technology have occurred over the past 10 years that have fostered its rapid improvement in performance without changing the basic nature of its operation.

In 1969, the standard MOS technology was an aluminum-gate p-channel process that exhibited low density and speed relative to today's standards. The first major advance in MOS performance came when silicon-gate processing replaced the original metal-gate approach. The silicon gate offered the great advantage of self-alignment: the usual overlap design required to accommodate misregistration of the gate with respect to source and drain regions was no longer necessary. With parasitic overlap capacitance greatly diminished, the pathway to greater speeds was cleared.

In 1972, the arrival of n-channel MOS meant an immediate boost in device speed, since the mobility of electrons is superior to that of the holes in p-channel MOS. At the time, Intel introduced the 2102 1-K static random-access memory, which was built only with enhancement-mode transistors using 6-micrometer channel lengths. Its typical address-access time was 500 nanoseconds.

Two years later, faster circuit speeds were made possible by the introduction of producible depletion-mode devices used as active loads. Using them, the 2102A dropped its typical access time down to 150 ns.

Since then, advances in MOS circuit speed have been attributable to device scaling. First, the 2115 1-K static RAM used 4.5- μm channels and 1,000-angstrom oxides for its typical access time of 55 ns.

In 1977, a comprehensive approach to scaling was

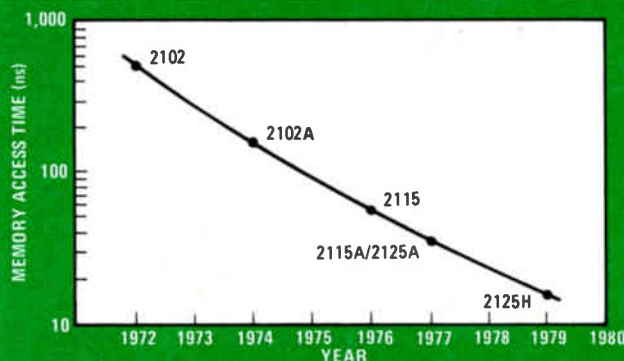
applied in Intel's HMOS process. The result was the 2115A, built with 3.5- μm gate lengths and 700- \AA oxides, to reach down to a typical access time of 35 ns. Through selective scaling of many critical physical and electrical parameters of the MOS devices, the trend toward higher speeds was maintained. At the same time, power requirements were reduced, thus significantly improving the power-delay product of MOS technology.

HMOS II goes a step farther. A direct descendant of HMOS, it employs device-scaling principles to improve performance beyond any MOS technology currently in production. The 15-ns typical address-access time (at room temperature) of the 2125H, made with HMOS II, is twice the speed of the 2115A, and an incredible 33-fold improvement over the 2102, which was introduced only seven years ago.

HMOS II is not the end of the road by any means. With the introduction of improved lithographic equipment such as direct-wafer-stepping exposure systems, resolution well below 1 μm will soon be possible. Yet even though the technology to produce the submicrometer devices of the 1980s might be well within reach, the introduction of such devices in a commercial process could be delayed by another factor—the adherence of industry to today's standard 5-volt power supply. Although HMOS II and possibly the next generation of scaled devices are achievable without reducing the supply voltage, there is no question that industry acceptance of a new voltage standard—say, a 2- or 3-V level—is inevitable. But that hurdle could turn out to be more difficult to get over than the technology development itself.

EVOLUTION OF MOS TECHNOLOGY

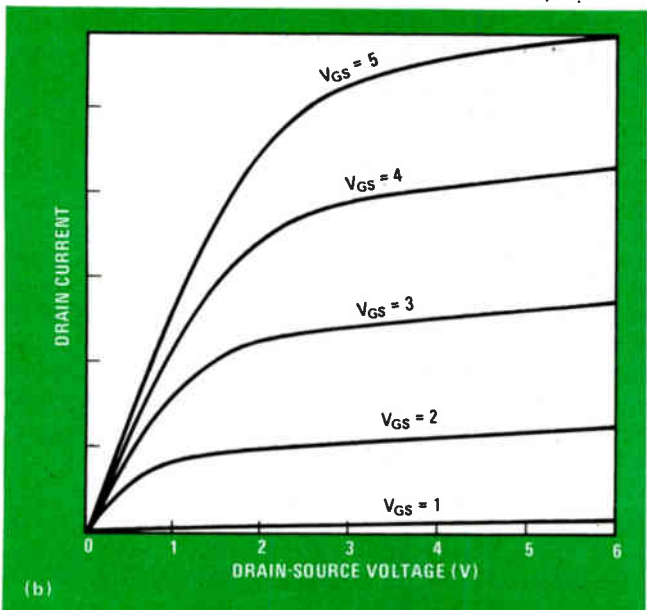
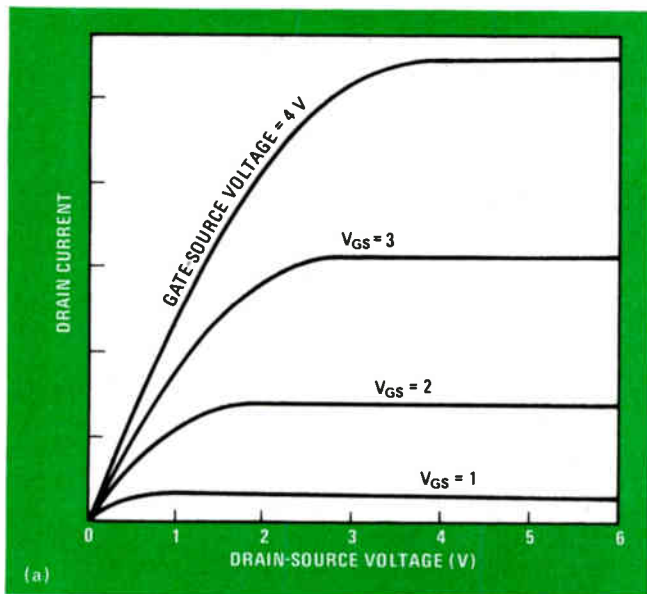
| Device/circuit parameter | Al-gate p-MOS 1969 | Si-gate p-MOS 1970 | Si-gate n-MOS 1972 | Depletion mode n-MOS 1974 | HMOS 1977 | HMOS II 1979 |
|---|--------------------|--------------------|--------------------|---------------------------|-----------|--------------|
| Gate length L (micrometers) | 20 | 10-12 | 6 | 6 | 3.5 | 2 |
| Lateral diffusion L_D (μm) | 5 | 2 | 1.4 | 1.4 | 0.6 | <0.6 |
| Junction depth X_J (μm) | 2.5 | 2.5 | 2.0 | 2.0 | 0.8 | <0.8 |
| Gate oxide thickness T_{Ox} (angstroms) | 1500 | 1200 | 1200 | 1200 | 700 | 400 |
| Power supply voltage V_{CC} (volts) | 12 | 12 | 12 | 5 | 5 | 5 |
| Minimum gate delay T (nanoseconds) | 80-100 | 40-50 | 12-15 | 4 | 1 | 0.4 |
| Power delay product (picojoules) | 60-80 | 30-40 | 18 | 4 | 1 | 0.5 |



will be necessary to provide the same current drive as a device not in velocity saturation. Again, the unscaled power-supply voltage takes a performance toll.

Reliability key

One critical question that arose during the course of HMOS II development was the long-term reliability of short-channel, thin-oxide technology. With the supply fixed at 5 v, substantially higher electric fields occur both laterally and vertically within the scaled-down MOS structure. One possible effect of these high fields that impacts long-term reliability is the generation of hot electrons. Electrons become hot when accelerated to such a high energy that their temperature is greater than the equilibrium temperature of the lattice.



3. Saturation. Scaling can produce velocity saturation, which occurs when increased electric fields cause electrons to interact with lattice phonons. The effect on the current-voltage characteristics of a normal (unscaled) MOS device (a) is compression of the I-V curves at high gate voltage (b) due to a reduction in current gain.

The danger is that hot electrons can overcome the potential barrier at the oxide-silicon interface; once injected into the oxide they may become trapped. Electrons trapped in the oxide cause a positive shift in a device's threshold voltage that increases with the concentration of trapped charge. Thus, cumulative hot-electron trapping can cause a time-dependent threshold-voltage shift with a corresponding degradation in circuit performance over time.

Fortunately, charge-trapping effects have been successfully modeled. Theory predicts that the trapping rate increases with lateral and vertical electric fields (thus the concern for HMOS II) as well as with reduced temperatures. These relationships work to the advantage of reliability testing by allowing accelerated evaluation of threshold-voltage and circuit-performance implications. Stressing at high voltages (8 v) and low temperatures (-70°C) for 1,000 hours can simulate the hot-electron trapping effects of 50 years of standard operation. This accelerated stress-testing procedure was performed on both 4-K memories and discrete transistors fabricated with the HMOS II process. The results: address-access time of the 4-K memory increased less than 1 nanosecond, and the discrete transistors displayed no observable threshold shift. HMOS II simply does not have a hot-electron trapping problem.

IBM concurs

That conclusion is supported by a recent study by IBM Corp. Researchers at IBM who fabricated devices with even smaller geometries than those used in HMOS II showed that the current injected into the oxide of devices at normal voltages can only be observed at extremely low temperatures—for instance, -196°C . The temperature and channel-length dependence of the injected current indicates that HMOS II is still in an operating range where hot-electron effects will be unmeasurable.

A second reliability issue intrinsic to HMOS II is the integrity of the 400-Å gate oxide. Improved oxidation techniques have made HMOS II oxide integrity equivalent to the 700-Å oxide of HMOS despite the higher fields associated with the new technology. The breakdown voltage for the 400-Å oxide is typically well above 20 v with acceptably low defect densities. Moreover, the final testing procedure stresses the thin oxides at 10.5 v to guarantee product reliability. Since oxide breakdown is a time-dependent effect that increases exponentially with electric field, the short stress test eliminates all of the infant failure population.

A detailed product-reliability program has been completed for two static RAMs built with HMOS II: the 1-K 2125H and the 4-K 2147H. The reliability qualification includes 125°C dynamic burn-in with test intervals of 48 to 1,000 hours. The program also includes low-temperature testing, static-temperature cycling and a 250°C bake for 500 hours. Failure rates on HMOS II indicate long-term reliability should be at least as good as for HMOS. After 3.6 million device-hours of testing at 125°C , the HMOS II failure rate was 0.016% per 1,000 hours at 70°C and 0.010% per 1,000 hours at 55°C .

The 2125H, a 1,024-by-1-bit static RAM, became the yield and development vehicle for HMOS II. A previous

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HMOS product, the 2125A, provided the basic layout. Some of its internal circuits were modified to optimize their design for the new technology; but since the basic layout remained intact, the 2125H has the same die size and organization as its HMOS counterpart.

Although the improved circuit density of HMOS II was not capitalized upon in the 2125H, the part provides information about the technology's potential circuit performance. A twofold improvement in performance or density is generally necessary to justify a major technology development; HMOS II is no exception. Typically the 2125H exhibits an address-access time of 15 ns with a power dissipation of 370 milliwatts. The 15-ns access time (at room temperature) is better than twice as fast as the typical 35-ns time of the 2125A.

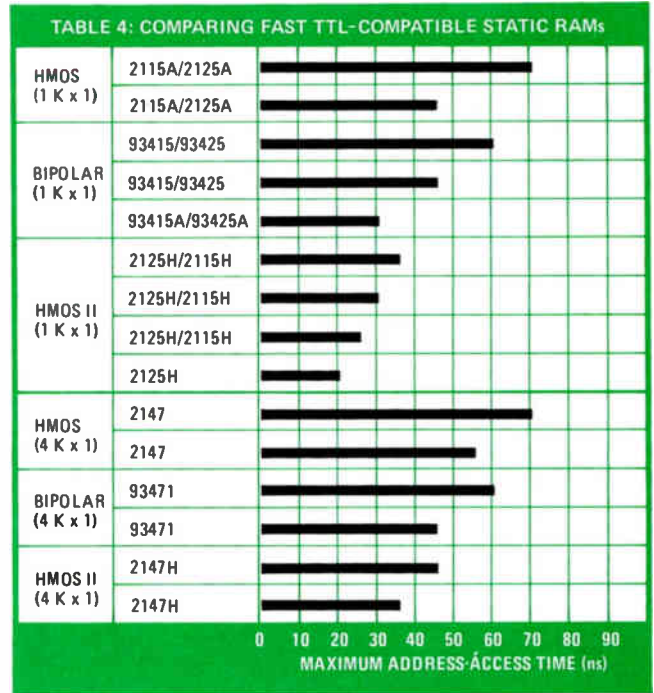
Fully optimized

The first complete design to be fully optimized for HMOS II is the 2147H 4-K-by-1-bit static RAM. Since it is an entirely new design, the chip layout takes advantage of the 20% density improvement over HMOS offered by HMOS II. The die size of the 2147H is 120 by 177 mils, or 21,240-mil², compared to the 25,000-mil² 2147.

The 2147H is organized similarly to the 2147, with two memory planes separated by a common row decoder. This type of a layout conserves space for the decoder while minimizing the slowdown of access time due to word line resistance-capacitance delays that bits far from the row decoder suffer.

The peripheral circuitry is located mainly at one end of the chip. The 2147H has its substrate-bias generator, column decoders, output buffer, and all of the control circuitry at one side; only half the address buffers are found at the other side of the chip.

The main feature of the 2147H is not its die size or



layout, however, but its performance specifications. The speed offered by the shrunken HMOS II technology together with some design improvements in the row decoders, chip-select buffer, and output allow the 2147H to achieve a typical access time of 22 ns (35 ns guaranteed) with no increase in power dissipation over its 55-ns 2147 HMOS predecessor. The specifications of both the 2125H and the 2147H are summarized in Table 3. The typical access times noted above for both products have allowed the announcement of a 20-ns 2125H and 35-ns 2147H over the full commercial temperature range. These parts have the fastest address-access time of any TTL-compatible RAMs available today, as the comparison with bipolar devices shows (Table 4).

Production compatibility

The fact that HMOS II is based so heavily on HMOS pays important dividends. Not only was development time held to a minimum, but the always-delicate transfer from engineering to production control of the process proceeded smoothly. As a result, HMOS II is in production today, and the availability of the 2125H and 2147H static RAMs is excellent. Not only is a large family of static RAMs planned for the future, but HMOS II exhibits the same flexibility for a broad design base enjoyed by HMOS—it will be applied to high-performance microprocessors and a variety of peripheral chips. Because MOS is more suited to device scaling than bipolar technology, recent advances in photolithography and scaled wafer processing indicate a bright future for MOS performance.

The fast rate of its improvement in the 1970s should continue in the 1980s with the incorporation of direct wafer-stepping equipment and advanced dry-etching techniques. The performance improvement record for MOS over the past decade will be difficult to match; however, the tools and techniques are available today to make it happen. □

TABLE 3: TYPICAL CHARACTERISTICS OF HMOS II RANDOM-ACCESS MEMORIES

| Parameter | 2125H | 2147H |
|--|-------------------------|-------------------------|
| Physical characteristics | | |
| Die size | 10,816 mil ² | 21,240 mil ² |
| Organization | 1,024 x 1 | 4,096 x 1 |
| Dc characteristics (typical) | | |
| Supply voltage | 5 V | 5 V |
| Active power dissipation | 330 mW | 500 mW |
| Standby power dissipation | — | 45 mW |
| Input/output levels | TTL | TTL |
| Output sink current (V ₀ = 0.45 V) | 26 mA | 31 mA |
| Output source current (V ₀ = 2.4 V) | 31 mA | 33 mA |
| Ac characteristics (typical) | | |
| Address-access time | 15 ns | 22 ns |
| Chip-select access time | 6 ns | 22 ns |
| Power-down time | — | 10 ns |
| Read-cycle time | 15 ns | 22 ns |
| Write-cycle time | 15 ns | 22 ns |

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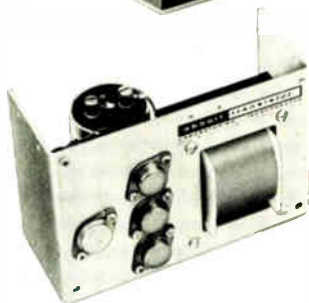
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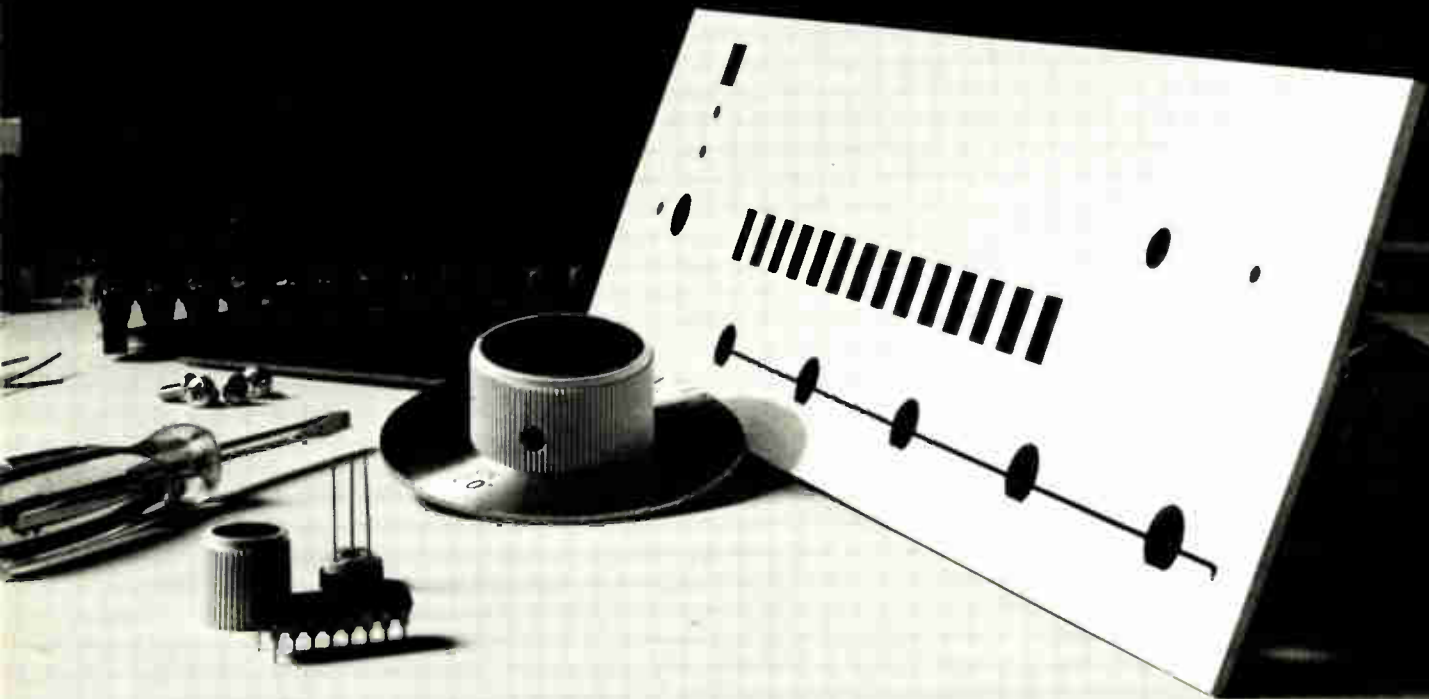
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MOS sampled-data technique shrinks a-d converter chip

Charge-balancing comparator with space-saving ladder design produces 8-bit monolithic device that interfaces with microprocessors

by Thomas P. Redfern, J. John Connolly, Sing W. Chin, and Thomas M. Frederickson

National Semiconductor Corp., Santa Clara, Calif.

□ Armed with know-how accumulated in MOS technology, semiconductor manufacturers are increasingly turning their attention to the problems of analog-to-digital conversion. Eager to put their expertise to work in a new area, they are focusing their sights sharply on the potentially huge and lucrative market for low-cost a-d converters that can interface easily with microprocessors. To achieve economy, some form of monolithic integrated circuit is the obvious choice. But, because they either are too slow or take up too much chip area, monolithic ICs have traditionally been unsuited to most a-d conversion techniques.

Now, however, building on a few earlier monolithic approaches to converter design and adding some unique circuit wrinkles, new 8-bit a-d converters are appearing [*Electronics*, May 10, 1979, p. 105] that substantially meet the goals of low cost with simplicity of application and offer performance advantages over monolithic designs of the past. One is trademarked the Naked-8 a-d converter by engineers at National Semiconductor Corp., Santa Clara, Calif., and its more explicit family ties are to the ADC 0801/02/03/04 series. It incorporates a unique charge-balancing comparator, uses a sampled-data technique, and also achieves microprocessor-compatible performance on a reasonably sized chip. Designs already in the works will extend the techniques to devices with 10- and 13-bit capacity.

Evolution

Monolithic integrating analog-to-digital converter products have been available for many years. These bipolar designs primarily use a dual-slope or multislope technique that performs excellently in all areas except speed. Their conversion time, T_c , is generally in the 100-millisecond range. With successive-approximation designs, the T_c is reduced to 10 to 100 microseconds, making approaches that use these designs very popular.

In the course of bipolar circuit development, the monolithic d-a converters typically appeared first. Later, they were incorporated into the hybrid a-d converter. These monolithic d-a devices used emitter-area-scaled transistors with bases biased in common. Each emitter had a binary-weighted precision resistor tied to a common negative power supply voltage, thus limiting the maximum groupings of transistors to four because of the large—16:1—resistor ratio that was needed; more inter-

quad divider resistors were necessary to create hybrid d-a converters of up to 16 bits. Most of today's hybrid d-a 12- and 16-bit devices take this approach, using a monolithic quad current source IC with added resistors.

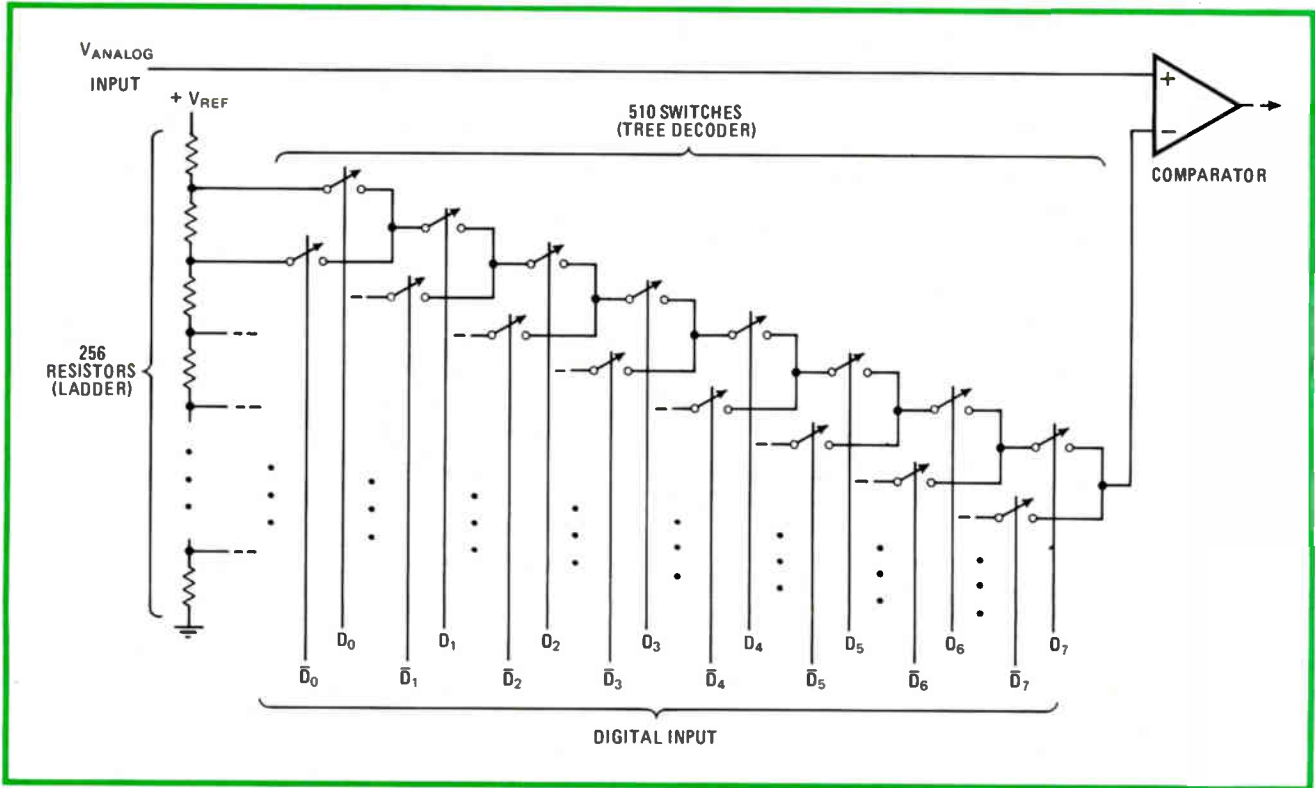
MOS technology was first applied to hybrid a-d products using the now-familiar R-2R ladder in the normal or voltage-switching mode. C-MOS switches are used to drive the high-impedance ladder network. IC products have also been built using C-MOS switches in the current mode, or inverted R-2R ladder configuration. This created the four-quadrant multiplying d-a converters, where the current through the ladder is converted to a voltage via an external op amp. These very successful devices are used today to build a-d converters.

Something new with MOS

A few years ago, the p-MOS 8-bit a-d converter (ADCO800) was introduced. Incorporating a technique economical only with a monolithic approach, it was the first monolithic successive-approximation a-d converter. It used a sampled-data comparator and a multi-tap, diffused-resistor string (ladder) between a reference voltage (V_{ref}) and ground. A tap was provided for each of the 2^N possible analog voltage levels. This was therefore dubbed the $2^N R$ potentiometric technique, and it has been used in several monolithic 8-bit a-d converters, such as the 8-bit C-MOS National Semiconductor ADCO816 and the converter in the Intel 8022 microprocessor. These devices have much faster conversion times, 10 μs to 100 μs , in contrast to the milliseconds of the earlier monolithic integrating devices.

At first it appeared that MOS potentiometric a-d devices would be limited to 8-bit designs because, even at 8 bits, 256 resistors and 510 ($2^{N+1} - 2$) analog decoding switches are needed, as shown in Fig. 1. This large number of switches is used in a so-called tree-decoder to reduce the number of drive lines needed. Though this eases the layout problem, it places eight switches in series between each tap on the ladder and the comparator input, greatly increasing their total on-state resistance. What's more, even for 8-bit designs, the resistor ladder and tree-decoder switches typically occupy up to 50% of the total die area of the a-d device.

Improved techniques are therefore needed to reduce the large chip size that would result from straightforward application of the $2^N R$ potentiometric technique to



1. Ladders and trees. In a typical potentiometric analog-to-digital converter, the number of resistors and analog switches that is required imposes a severe limitation on the total number of bits that can be handled. In this 8-bit $2^N R$ potentiometric design, 256 resistors are required for implementation, as well as 510 switches in a tree-decoder layout. These elements can take up half the chip area.

10- and 12-bit converters. Much effort has been made to reduce the number of required resistors and switches.

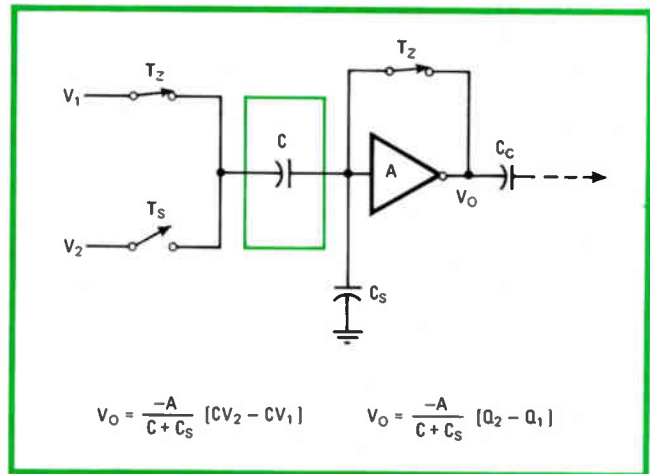
The comparator is the key element in the design of an a-d converter. Oscillation problems occur when standard IC comparators are operated in their linear, or active, mode. Because they must operate at a precise trip point, hysteresis cannot be used to prevent oscillations. This problem becomes more severe for higher-resolution converters and is very challenging at the 12-bit level.

Using the comparator

In a typical successive-approximation design, the comparator output is sampled only near the end of the comparison interval, so there is less susceptibility to noise. Based on the state of the comparator output at this time, the most recently examined bit from the register is either kept or reset. This decision remains final for the ongoing conversion. Thus the noise or oscillation of the comparator is indicated by generating more than one code for a given analog input voltage. This problem is greatest at or around changes in code and creates ambiguity at these points. Unfortunately, though the use of hysteresis in the design of the comparator solves this problem, it introduces a new one—the active code changes depend on whether the analog input voltages are increasing or decreasing.

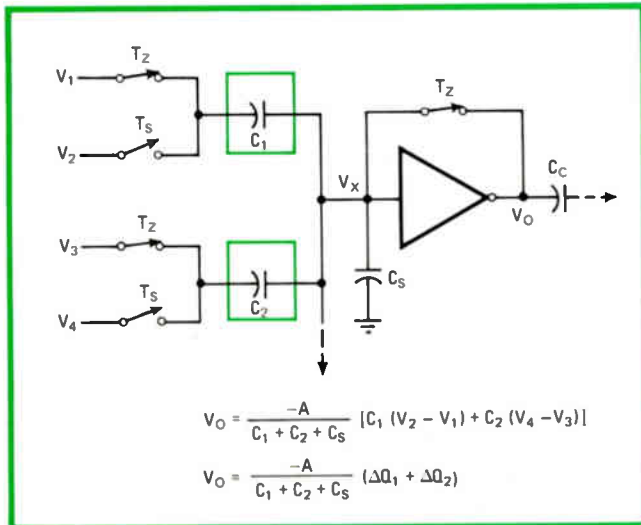
Finally, comparator response time depends on the amount of overdrive provided. Higher-resolution converters operate with smaller overdrives (less than 1 mV), and this can create response-time problems.

MOS technologies now offer many new basic circuit



2. Sampled and autozeroed. Lending itself to MOS implementation is this autozeroed sampled-data comparator, shown in basic form. The circuit works by sampling input signals V_1 and V_2 successively and charging input capacitor C to the difference. The output logic level depends on whether the difference is positive or negative.

conversion approaches. One example is the autozeroed MOS sampled-data comparator of Fig. 2. It consists of a cascade of capacitor-coupled gain stages, where each stage is a slightly modified logic inverter, as shown. This circuit zeroes on one input signal, V_1 , and samples a second, V_2 . For example, during an initializing time interval, T_z , the switch to the V_1 input is closed and the switches shunting each inverter are also closed. This zeroing interval charges the input capacitor C to the V_1



3. Charge-balanced. The basic comparator of Fig. 2 can be modified to include many more differential input pairs. The level of V_x determines the output logic level in this circuit. Values of the input C_s can be chosen to scale individual voltages from each input pair.

input voltage minus the stage bias voltage. The T_z switches are then opened and the T_s (sampling time) switch is closed. If the input voltage V_2 is the same as V_1 , the input voltage of the comparator is in exact balance and the output of the inverter stage will remain at the bias-voltage level. For $V_2 > V_1$, the input of the inverter increases and this voltage change will be amplified by the total open-loop gain of the cascade of inverter stages

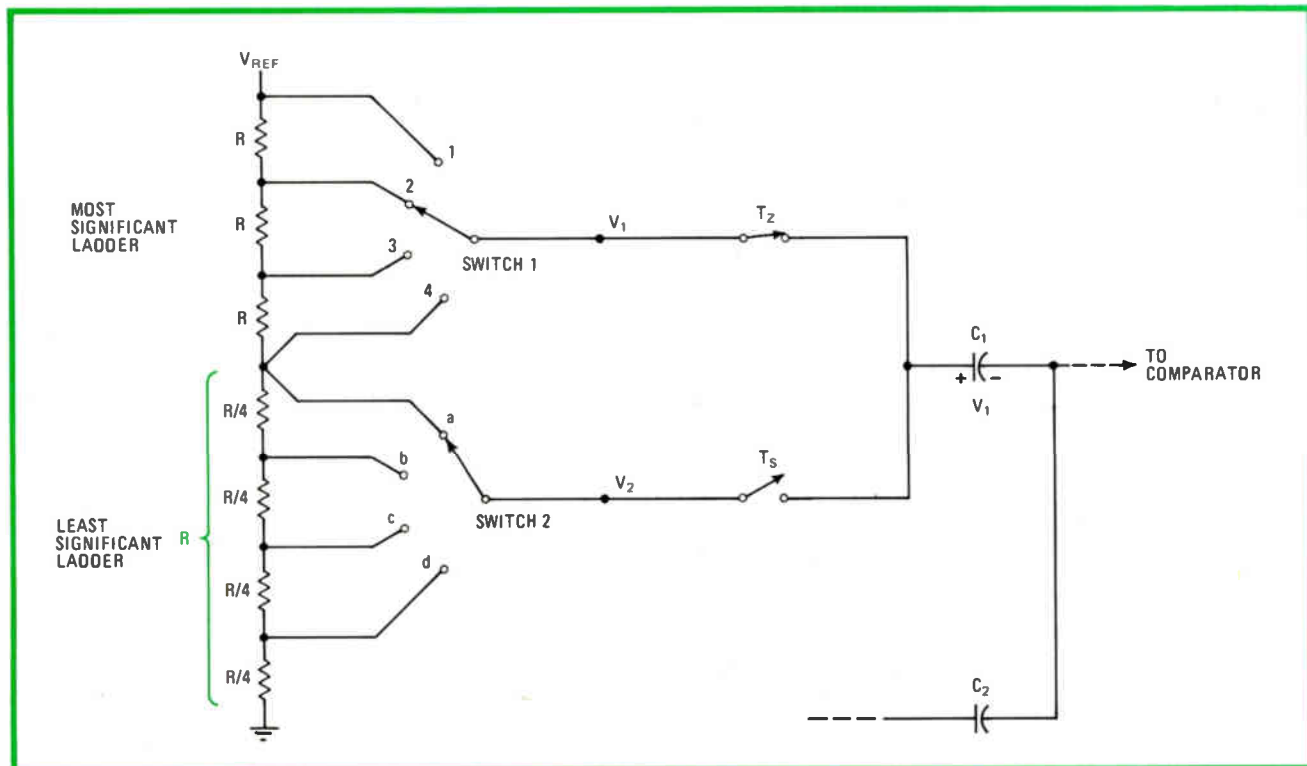
to give a definite logic state at the output. For $V_2 < V_1$, the input change is negative and, when amplified, provides the opposite logical output state.

The offset voltage of these autozeroed comparators is caused by parasitic charge coupling caused by imperfect switches. Compensating devices and care in mask design can keep this residual voltage to a minimum. But the important factor is that it is constant and essentially independent of temperature change and time. Comparator noise is reduced by sampling at frequencies well above the $1/f$ noise corner.

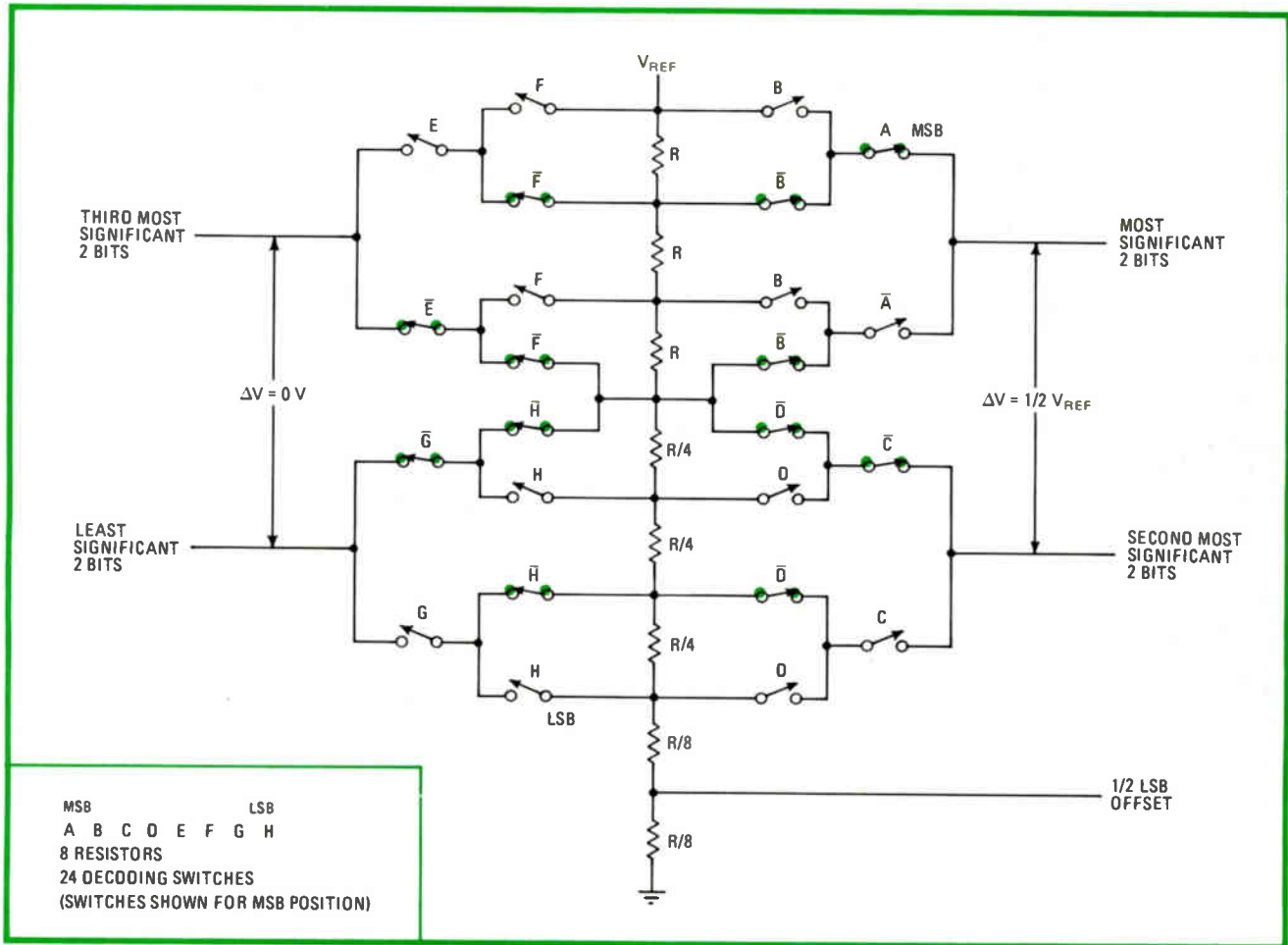
Extending the comparator's usefulness

Still more improvements in a-d converter designs are possible by modifying the basic MOS comparator of Fig. 2 to include a multiplicity of differential input-voltage pairs as shown in Fig. 3. Here the voltage from the change in charge at the comparator input is amplified. There are now many inputs available for both the unknown analog signal to be converted and the d-a output. For example, V_1 and V_2 can provide differential analog inputs, and V_3 and V_4 (and even more differential pairs) can be used for the d-a inputs. If the charge transfer from the d-a converter is equal and opposite to the charge transferred by the analog differential input, then comparator equilibrium—or charge balance—is obtained ($V_x = 0$). This circuit permits the values of the individual input capacitors to weight or scale each input voltage pair, which makes possible a new ladder extension to be discussed later.

Unique to this technique is that capacitors convert



4. Extension. It is possible to conserve chip real estate by coupling the multiple differential-input comparator with an appropriate ladder design. Here a single ladder has actually been formed from two—a coarse or most significant ladder and a fine or least significant ladder. In the particular 4-bit example illustrated here, only 7 resistors are required instead of the 16 that would be needed by a $2^N R$ approach.



5. Further extension. Here the principle of ladder extension has been applied to an 8-bit decoder, in which two 2-bit ladders are utilized twice to provide appropriate differential inputs for the charge-balancing comparator. In the switch positions that are shown in the illustration, the converter is generating differential voltages of $V_{ref}/2$ and $0V$ in the first interval of a successive-approximation register search.

voltage into charge, which is then algebraically summed. Notice that input voltages are directly subtracted and compared with the sum of the effects at other differential inputs. This circuit function has never before been achieved in comparators.

Economizing on die area

When the comparator has been modified to accept multiple, differential inputs, a savings in die area can be achieved in the ladder design. The basic idea is to use at least two ladders, a coarse or most significant (MS) ladder and a fine or least significant (LS) ladder. For the 4-bit example in Fig. 4, the MS ladder provides the 2 most significant bits (MSBs) and the LS ladder the 2 least significant bits (LSBs). The comparator allows the higher resolution of the LS ladder to be fitted or extended into any of the additional three segments of the MS ladder and thereby provides the equivalent of a 4-bit potentiometric d-a converter—even though only 7 resistors are used (not 16 as required for the $2^N R$ approach) and correspondingly fewer analog switches are needed.

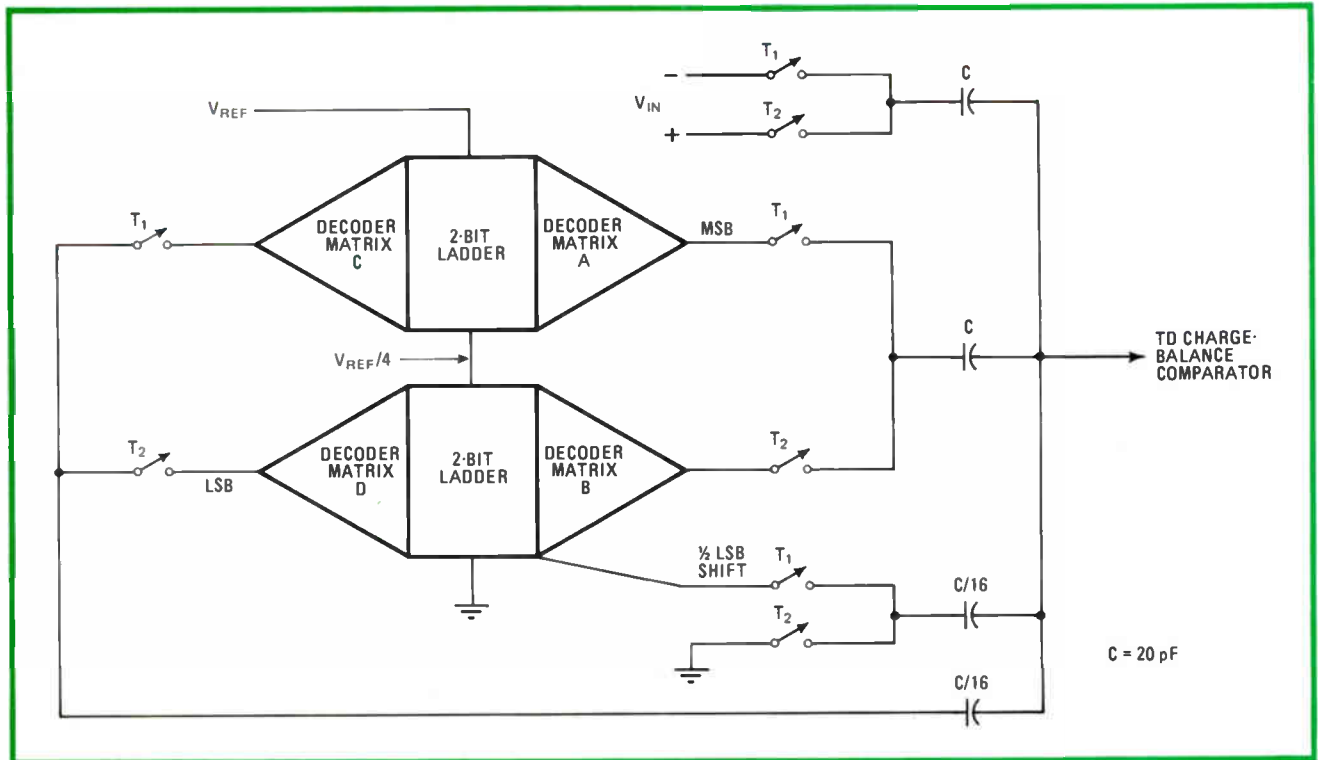
An additional savings in die area results if this ladder is reused, simply by adding extra analog switches to expand the resolution of the a-d device further.

This new charge-balancing comparator has been

designed into a novel 8-bit monolithic a-d IC. A single resistive ladder (Fig. 5) is used that has taps of $1/4 V_{ref}$ in the upper portion and taps of $1/16 V_{ref}$ in the lower portion. The two MSBs, A and B, increment in $1/4 V_{ref}$ steps and the second 2 bits (C and D) increment in $1/16 V_{ref}$ steps. By using the additional voltage scaling provided by setting the ratio of the input capacitor values, this same ladder is used for the 4 LSBs and the comparator properly combines all 8 bits over the whole dynamic range. For example, during the first interval of a successive-approximation register search ($\bar{A} \bar{B} \bar{C} \bar{D} \bar{E} \bar{F} \bar{G} \bar{H}$), the d-a converter is generating voltage differences of $1/2 V_{ref}$ and $0V$, as shown in Fig. 5.

Figure 6 shows how the concepts of Figs. 3, 4, and 5 have been combined to make the 8-bit a-d converter. Decoding matrixes A and B supply the 4 MSBs through input capacitor C, and decode matrixes C and D supply the 4 LSBs through the scaled capacitor $C/16$. As can be seen, there is a total of four sets of differential inputs to the comparator. A special input is used to supply a $1/2$ -LSB-shift input to the comparator. This is used in all a-d devices to center the quantization error about the proper analog input voltage.

The required matching of the various capacitors is relaxed with this approach. For example, if the capacitor



6. Combination. Decoding matrices A, B, C, and D and the 2-bit ladders are shown arranged to provide the four differential inputs to the comparator. An additional $\frac{1}{2}$ -LSB shift input has been provided for centering the quantization error.

that couples the analog differential inputs should be imprecise in relative value, only a scale error would be introduced. The capacitor from the LS d-a device, $C/16$, needs to match the capacitor of the MS d-a converter to only 6 bits (1 part in 64) to keep an acceptable overall error ($\frac{1}{4}$ LSB) between the d-a sections. Finally, the $\frac{1}{2}$ -LSB shift has an even larger tolerance and essentially no influence on the overall performance of the a-d converter.

The complete 8-bit a-d converter uses only eight resistors, four capacitors, and 32 switches. The eight resistors are implemented from identical units in the interest of good matching; a total of 16 such resistors are required. It is fabricated with a compatible C-MOS/Si-Cr process on a chip 120 by 127 mils and exhibits linearity errors of less than $\frac{1}{16}$ LSB (typically below $\frac{1}{2}$ LSB). The performance characteristics are listed in the table.

To evaluate the comparator's performance, a 16-bit d-a converter was used to supply the analog input voltage to the a-d unit in 153-microvolt steps and the error was plotted for both increasing and decreasing analog-input voltage sweeps.

Better linear performance

The linearity plot (Fig. 7) shows total error as a function of the analog input voltage. Any error in excess of $\pm\frac{1}{2}$ -LSB quantization is due to an imperfect a-d device. Note that this plot shows errors of only $\frac{1}{8}$ LSB in excess of the quantization error and therefore represents better performance than that of the additional $\pm\frac{1}{2}$ LSB typically specified for an a-d converter.

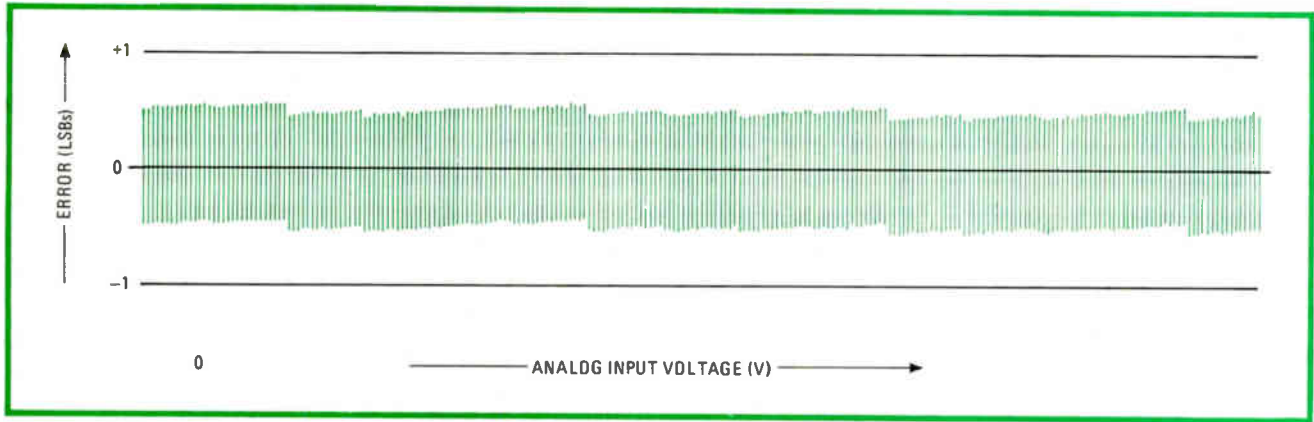
In designing an a-d converter into a real system, problems often arise. The manufacturer usually assumes

a zero output code for an input voltage of zero and a full-scale output code (all 1s) for a full-scale input voltage. In a real system, the input voltage may not go as low as 0 V, or approach a full scale of 5 V. Perhaps the system operates with ratiometric transducers whose output may only range from 15% to 85% of the voltage supply. This complicates the analog design and does not make full use of the available resolution. Further, the a-d device may have been specified for a 5.000 V_{dc} voltage reference and a single 5-V power supply is insufficient to bias a 5-V reference.

Solving applications problems

Two design features of the ADC0801 series solve these application problems. The first provides a differential analog input and the second operates the internal ladder for the d-a converter at only 2.5 V dc. As shown in Fig. 8, this a-d converter can operate with a 5-v dc supply as either a ratiometric or an absolute reference.

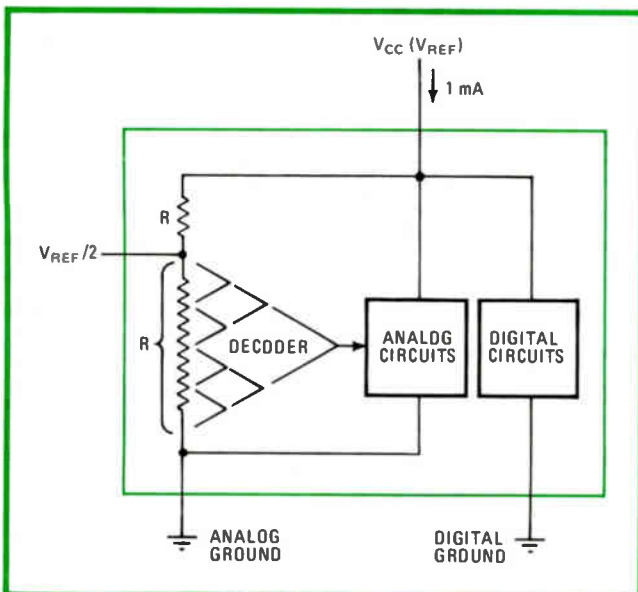
| 8-BIT a-d CHARACTERISTICS (ADC0801) | |
|--|---------------------|
| Linearity | $\frac{1}{4}$ LSB |
| Conversion time ($f_{clk} = 640$ kHz) | 100 μ s |
| Analog input range | 0- V_{cc} |
| f_{clk} range (external RC) | 100 - 800 kHz |
| Supply voltage range | 4.5 - 6.3 V dc |
| Current drain | 1.8 mA dc |
| $V_{REF/2}$ range | 0 - 5 V dc |
| Logic input levels | Std TTL |
| Logic output | 1 TTL load |
| Package | 20-pin dual in-line |



7. Error plot. The recording of total error as a function of the analog input shows that it is only $1/16$ LSB more than the quantization error of $\pm 1/2$ LSB—a figure well within the additional $\pm 1/2$ LSB that is usually specified for an analog-to-digital converter.

The 2.5-v tap point is brought to a package pin so this point can be supplied with an external 2.5-v reference (which can be powered from the 5-v dc supply). The $V_{ref}/2$ tap can also serve as a full-scale adjust pin when the a-d device is operated ratiometrically from the V_{cc} supply. This permits adjustment for a wide variety of low-cost transducers. Also this $V_{ref}/2$ tap can be forced even lower to increase the resolution of the a-d device. For applications with a limited analog-input dynamic range, the resolution can easily be increased to equal that obtainable in a 9- or 10-bit converter. Finally, this $V_{ref}/2$ pin can be grounded to give a high-gain, microprocessor-interfaced comparator to output all 1s for $v+ > v-$. If an input analog multiplexer is used, some channels can be a-d and others can be comparators.

These features can also be used both to offset the zero level and to accommodate a reduced analog span. This easily solves the problem that occurs when working with a basic ratiometric transducer, which ranges neither to zero nor to the power supply limit.



8. Half-reference. A feature of the ADC0801 is a 2.5-v tap on the 5-v reference that is brought to a pin for a variety of uses. For example, the tap can serve as a full-scale adjustment for various transducers or as a ratiometric reference.

Further, the dc common-mode gain is less than $1/16$ LSB over the complete range of 0 v dc to 5 v dc and a dynamic common-mode voltage of 1.9 V_P at 60 Hz before $1/4$ LSB of error is introduced. This can be used to eliminate the need for an instrumentation amplifier in many applications. This dynamic common-mode response is achieved by maintaining four and a half clock intervals between voltage samples at the differential inputs (assuming a 640-kHz clock). At power-line frequencies, the maximum allowed input voltage range would most likely be exceeded before the dynamic common-mode response could become a problem.

Providing a real interface

For many chips, the claim is made that they provide a microprocessor interface. Often this simply means that a three-state output has been provided. To provide a “real” microprocessor interface simply means that no external logic packages are required, that the dc logic levels are compatible, and the protocol and timing requirements are met—with special attention to the time from the read strobes to valid data on the bus.

It is most desirable to have the converter work directly with the control and data buses of the microprocessor system. This has been accomplished in the ADC0801 series by using the standard chip-select, \overline{CS} (which is decoded from the address bus), and write strobe, \overline{WR} , to cause the converter to start. When the conversion is complete, an output pin of the a-d converter asserts an interrupt, \overline{INTR} (active low). This replaces the conventional end of conversion (EOC) signal. If the converter is restarted or if the data is read, the \overline{INTR} output is automatically reset. This removes the interrupting signal. Finally, to obtain the digital output from the converter, the microprocessor will generate the address of the a-d device (which provides the \overline{CS} input) and a read strobe, \overline{RD} . This activates the converter’s three-state output buffers and places the digital data on the bus. By simply redefining the traditional controls of the a-d converter, no external hardware is needed in a microprocessor application. All logic is designed to meet exactly the TTL input and output voltage levels, and the data is valid on the data bus 135 ns after the falling edge of the \overline{RD} strobe (with 100-pF loading on the bus). This permits an interface to popular microprocessor systems. □

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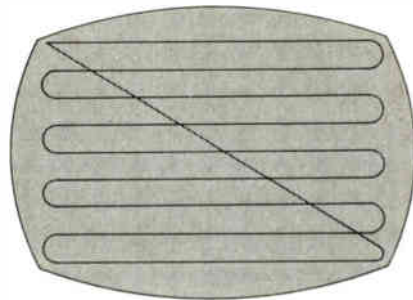
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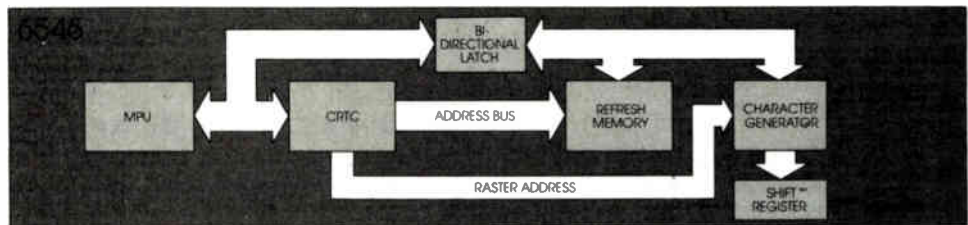
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When logic analyzers meet development systems

Choosing the right one for the job is harder now that development systems have added some analytic capabilities

by Bruce Farly, Hewlett-Packard Co., Colorado Springs Division, Colo.

□ As the contribution of logic analyzers to digital design and troubleshooting receives more recognition, some of the more sophisticated microprocessor development systems are adding logic analysis in the form of optional real-time trace modules. Why then should a design team need an analyzer as well as a development system?

The fact is that the two instruments' areas of application overlap only at certain stages in the realization of a microprocessor-based system (Fig. 1), and even at those points, their seeming similarity needs careful scrutiny to determine which is better fitted for the task in hand.

The work flow

Figure 2 recapitulates the sequence of tasks typical of a microprocessor design project. The assigned team of hardware and software designers first describes the functions of the target system and its subsystems in engineering terms. Next, the hardware designers generate and test the necessary circuitry. Meanwhile, the software designers devise an algorithm to manipulate data appropriately, then encode it in a source program (usually in assembly language for a microprocessor application), and finally assemble it in machine language, using an assembler program to produce the object program. When possible, they may choose to simulate program operation to eliminate any bugs.

At this point, the new hardware is ready to be tried out with the new object code and much time is spent not just on correcting errors but on solving thorny compatibility problems.

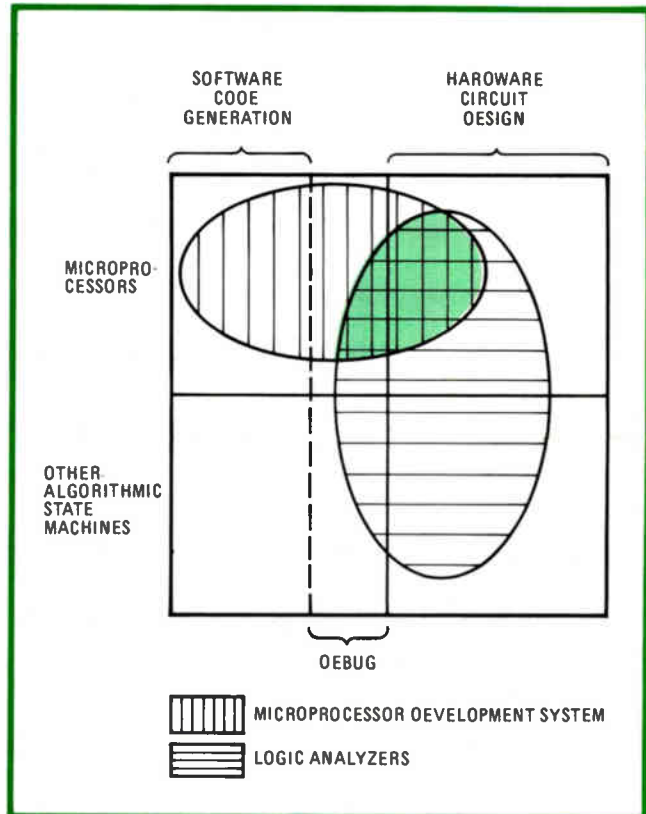
Conventionally the hardware engineer uses a logic timing analyzer during the design phase for his troubleshooting tasks while the software designer uses a development system for debugging as well as preparing and installing programs. During the integration phase, both find logic-state analysis becomes the critical measurement to pinpoint erroneous system behavior.

Now, while the sweeping change to microprocessor-based designs has freed the hardware engineer from many trivial tasks and lets him view design from a system level, it also forces him to work with system architectures that are increasingly bus-oriented and have specialized input/output functions. Faced with these changes, his first wish might be for a multichanneled oscilloscope with which he could simultaneously hunt for glitches and check signal timing. But in any case, a scope

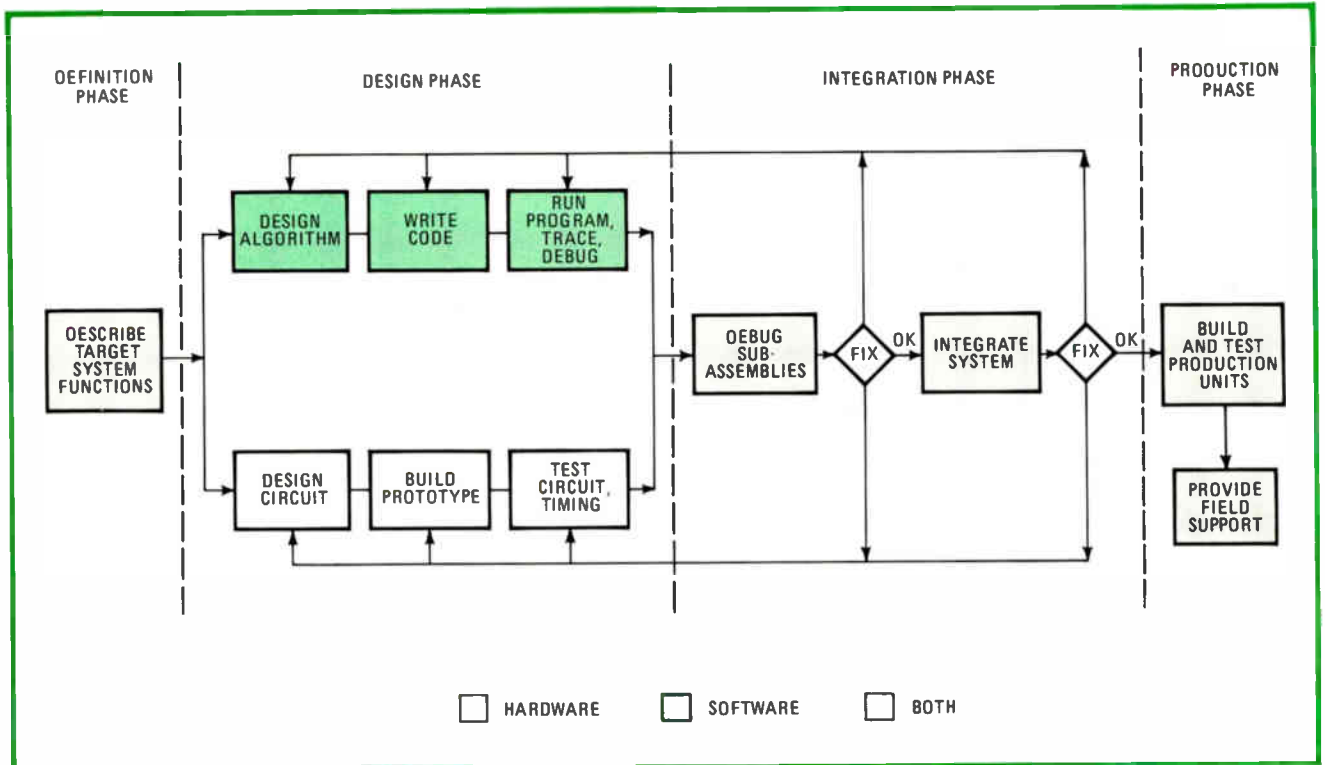
would be unable either to display signals with the extremely low recurrence rates common in digital design or to offer a backward look in time.

Logic timing analyzers lack these limitations. They can sample eight or more input channels simultaneously, displaying a voltage that falls within logic high or low as a discrete level on the vertical axis (Fig. 3). Time, displayed on the horizontal axis, is set by the analyzer's internal oscillator and varies in accordance with the sampling rate chosen.

Some analyzers enhance the sampling process by registering multiple transitions that occur between sampling times, thereby capturing and displaying pulses



1. **Area of confusion.** The present overlap of microprocessor development system and logic analyzer applications confuses designers of microprocessor-based equipment, who need to know which is the more appropriate for a given task.



2. Metamorphosis. Microprocessor development systems, originally built to aid the software design phase, are now moving into the integration phase with the addition of logic analysis capabilities, thus creating confusion about the role of dedicated logic analyzers.

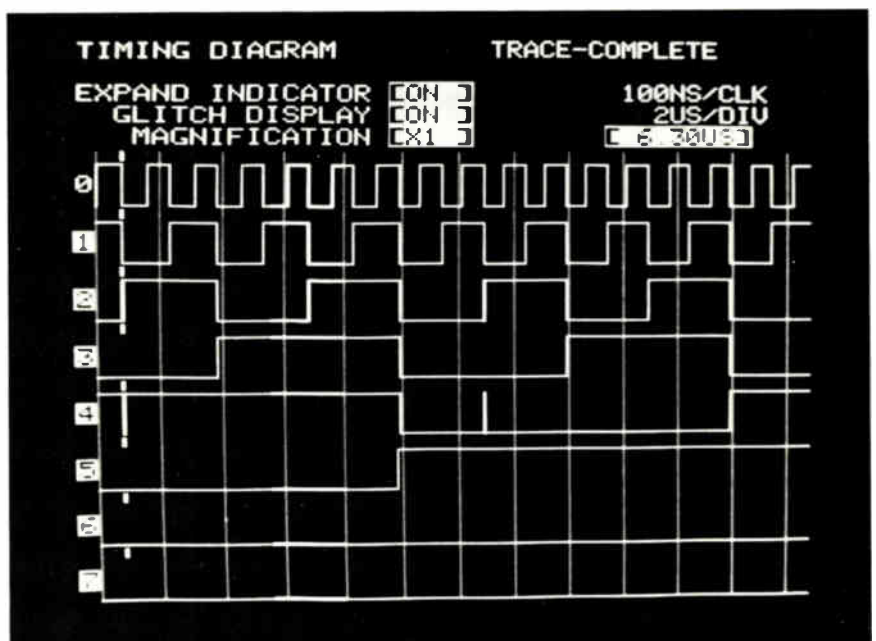
that are too short for them to sample directly. The analyzers also come with digital storage for each channel, so that they can display the events that precede as well as follow a certain occurrence.

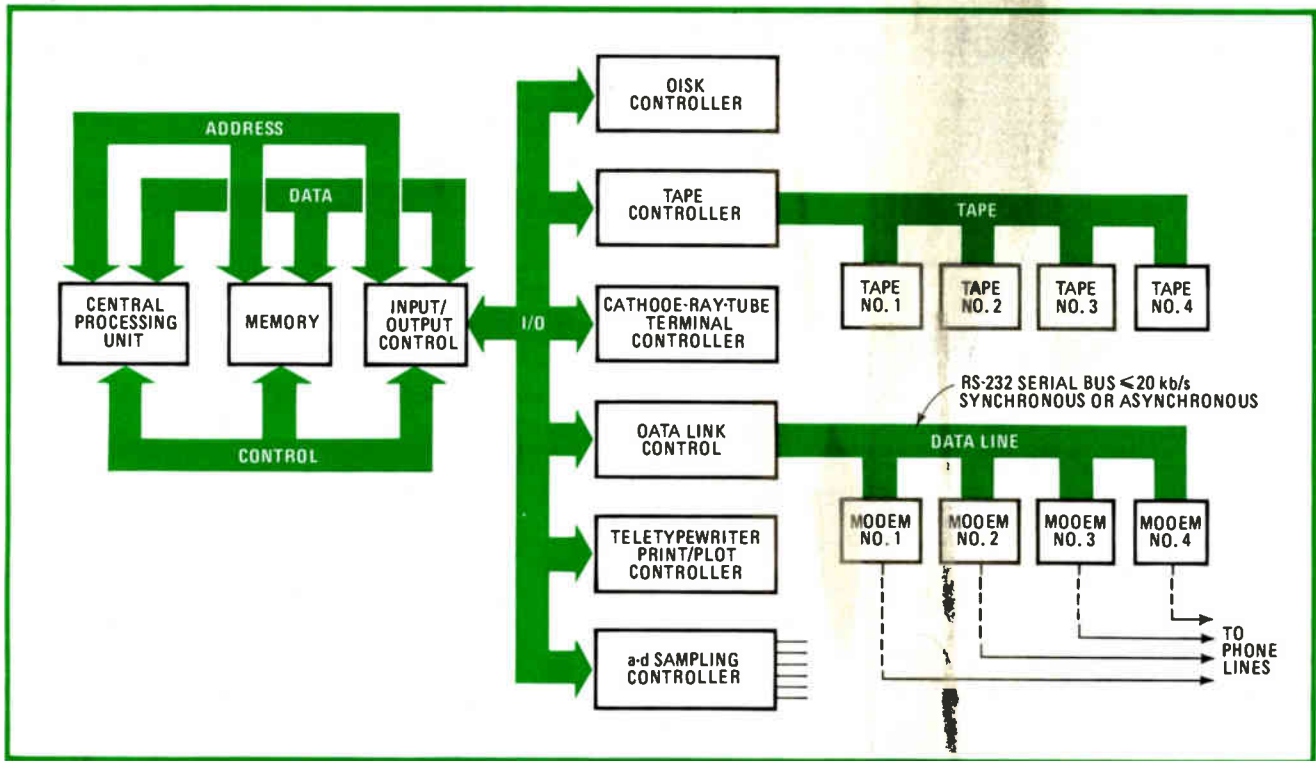
With good triggering, therefore, and the ability to look backward in time, logic analyzers are well suited to tracking down control-line problems and checking for asynchronous events that cause errors. And when a closer look is needed at the erroneous signal found, the analyzer often can trigger an oscilloscope.

To appreciate the usefulness of the logic timing analyzer in the hardware design, consider how it might be employed to troubleshoot part of the system that is shown in Fig. 4.

Associated with the system's processor are address, data, and control buses. By correlating data and address bus activity, the execution of the program within the processor can be monitored. Since these two buses are synchronous, they can best be examined using logic state techniques. Before examining the flow of data on these

3. Private world. The ability to display asynchronous changes in logic timing states is the sole province of the logic analyzers at present. This information is invaluable to the hardware designer, who must be certain that control and clock signals are properly distributed before program operation can be verified.





4. In between. The hardware designer must now deal with system architectures that are highly bus-dependent, such as that shown here. Asynchronous buses mandate timing analysis. Synchronous bus operation and data translations most often require state analysis.

buses, however, the hardware engineer must be sure that the signals controlling the processor's interaction and timing are in proper order.

The control bus is composed of lines that most frequently operate asynchronously, so that it is necessary to view the states of multiple lines for a continuous period of time—a function to which the logic timing analyzer is suited by design. Analyzing the asynchronous operation of control lines also requires the ability to trigger on truly unique events, to carefully discriminate between line states. Control line signals may be transitional states only a few nanoseconds long, and intermittent, narrow spikes caused by crosstalk or noise may appear. To capture these phenomena, the hardware engineer needs a logic timing analyzer that not only recognizes these states but triggers reliably when they appear.

Once the control bus is operating properly, the hardware engineer can further test the hardware and its response to the processor's modes of addressing and data fetching and its execution of instructions. To do so, he can generate some simple code and put it in a programmable read-only memory that he plugs into the system. But at this point, he is as interested in the actual timing of signals as in the flow of data in the system—the transfer of information versus strobe signals such as memory enables or read/write pulses. He has entered the logic state domain, where it is better to read data in machine code.

When the board appears to be operating properly, the hardware engineer will welcome some code from the software designer, and the integration phase can begin.

The software designer's role has undergone vast changes with the integrated-circuit revolution. Now

there are complete microprocessor development systems available that simplify software design by providing editor and assembler software for program generation as well as mass storage for easy file management.

Once a program has been written and assembled on a development system, it is possible to make it operate in the target system while still resident in the development system, thanks to the in-circuit emulator. After debugging, a program can be downloaded into PROM and, to the extent permitted by the memory mapping capabilities of the in-circuit emulator, further checking can be done on combinations of target system ROMs and emulated ROMs resident in the development system. The in-circuit emulator provides the "hooks" and "handles" needed to access the processor and internal registers, as well as the emulated memory for modification during the debug phase.

A new development

The recent offering of optional logic state analysis capabilities in development systems seems to place them in competition for the role now filled by dedicated logic analyzers. The way out of this dilemma is to concentrate on the unique contribution of each instrument and how best to make use of it at each stage of the design.

There is little cause for confusion during initial software writing and circuit design, when bugs appear in quantity but are relatively simple to find and correct (Fig. 5). Similarly, when hardware and software are integrated, the obvious bugs will be quickly found and corrected using any reasonable analysis approach.

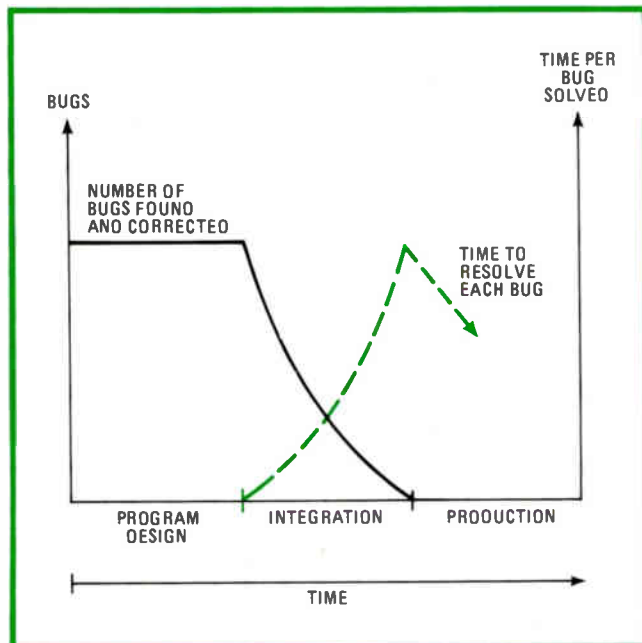
After this point, however, the more subtle and elusive bugs will become evident. Though fewer in number, they

ERROR SOURCES IN BUS-ORIENTED SYSTEMS

| Bus | Characteristics | Independent problems | Joint problems |
|--------------|--|--|--|
| Address | synchronous, less than 10-MHz transfer rate, 12 to over 20 lines | algorithm errors, lost programs, program stuck in loop, execution time efficiency | With data bus: algorithm errors, data-dependent errors With control: program-related glitches, effects of handshaking and of timing variations on program |
| Data | synchronous, less than 10-MHz transfer rate, 8 to 16 lines | | With address: as above With I/O: data transfer |
| Control | asynchronous, pulse duration under 50 ns to greater than 100 μ s 3 to AA lines | glitches, noise, crosstalk, timing sequence errors | With address: as above |
| Input/output | synchronous or asynchronous, often multiplexed, 8 to 16 lines | protocol violations, multiplexing errors, glitches, noise, crosstalk, handshaking errors | With data: as above With tape: data transfer With data link: serial-parallel conversion With a-d, d-a converters: conversion a-d, d-a |
| Tape | asynchronous, less than 5 MHz, often multiplexed, 8 to over 20 lines | | With I/O: as above |
| Data link | synchronous or asynchronous, 20 kb/s or less | protocol violations, handshake, data transfer to remote node | With I/O: as above |

take much longer to eradicate. The degree of subtlety and the remoteness of the problem symptoms from the CPU itself will usually lead the designer to conclude that a dedicated logic analyzer is the most efficient analysis tool. As the production deadline approaches, programs

are already in ROM and the fine tuning of the hardware becomes paramount. The software team is therefore partially free to move on to a new project, for which it will of course need the microprocessor development system. But if the hardware team is relying on the same system for hardware debugging, there will be harsh words at best and missed deadlines at worst. Thus, since software has become firmware and the target system can run independently, a logic analyzer can prevent conflict by addressing both the hardware and firmware problems while the microprocessor development system is being set up for the next project.



5. Hardy species. The many bugs that appear during initial software development are readily squashed. But while their number declines as hardware and software integration continues, the time spent finding each one increases as obvious faults give way to subtler ones.

Testing, testing

There is another and even stronger reason for preferring the logic analyzer to the development system in this phase: it eases the transfer of the system to production and the field. When the system moves into production and thence into field service, it will have to be accompanied by some practical test procedures and maintenance documentation. In view of the cost, it would be preferable to use a logic analyzer to find faulty modules quickly in production testing, which can even be automated when the analyzer is equipped with an IEEE-488 interface. Further troubleshooting to the component level is best implemented through signature analysis [*Electronics*, March 3, 1977, p. 89], a technique that can be enhanced by the gating signals provided by a logic analyzer's tracepoint outputs.

Until now, the development system with state analysis capabilities and the logic state analyzer have been treated as if they were virtually interchangeable. But in

| ADDRESS | | DATA | | EXTERNAL | |
|----------------|-------------|----------|------|----------|--|
| TRIGGER | | 0B85 | | | |
| TRACE TRIGGERS | ----- | LINE | 0 | | |
| ADRS | OPCODE/DATA | EXTERNAL | | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |
| 0B85 | 80 INPUT | 0000 | 0000 | | |
| 0B85 | 81 OPCODE | 0000 | 0000 | | |

| ----- | | TRACE LIST | | | ----- | | EXCHANGE-COMPLETE |
|-------|------|------------|-----|-----|-------|--|-------------------|
| LABEL | A | C | D | E | | | |
| BASE | HEX | BIN | OCT | DEC | | | |
| START | 2850 | 000 | 344 | 1 | | | |
| +01 | 2851 | 000 | 010 | 1 | | | |
| +02 | 2852 | 000 | 010 | 1 | | | |
| +03 | 2852 | 000 | 010 | 1 | | | |
| +04 | 2853 | 000 | 112 | 1 | | | |
| +05 | 2853 | 000 | 112 | 1 | | | |
| +06 | 2854 | 000 | 052 | 1 | | | |
| +07 | 2854 | 000 | 052 | 1 | | | |
| +08 | 2855 | 000 | 372 | 1 | | | |
| +09 | 2851 | 000 | 010 | 1 | | | |
| +10 | 2852 | 000 | 010 | 1 | | | |
| +11 | 2852 | 000 | 010 | 1 | | | |
| +12 | 2853 | 000 | 112 | 1 | | | |
| +13 | 2853 | 000 | 112 | 1 | | | |
| +14 | 2854 | 000 | 052 | 1 | | | |
| +15 | 2854 | 000 | 052 | 1 | | | |
| +16 | 2855 | 000 | 372 | 1 | | | |
| +17 | 2851 | 000 | 010 | 1 | | | |
| +18 | 2852 | 000 | 010 | 1 | | | |
| +19 | 2852 | 000 | 010 | 1 | | | |

6. Selective. Logic analyzers offer great flexibility in selecting the information to be captured from buses. In (a), the HP1611A displays a trace triggered only by the appearance of address 0B85. In (b), an HP1610A trace is restricted to a 285x address.

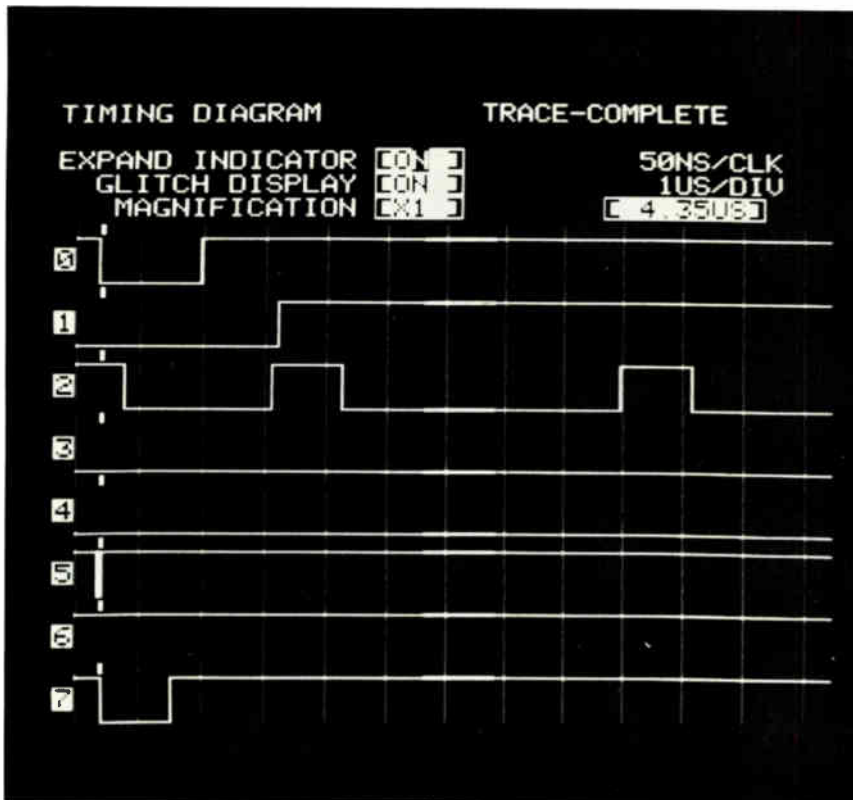
reality, the two tools are quite different in nature.

Logic analyzers are transparent to the system under test; they can grab data with their high-impedance probes as it occurs, while the system runs as it normally would. In contrast, most development systems function only by imposing breakpoints in hardware or software; typically the test system runs until it reaches such a point, stops, and returns control to the development system console to report test results. Therefore, many development systems cannot run continuous, transparent tests in real time, and they can run tests only on systems that can be started and stopped at will.

The in-circuit emulator used by the development system is real-time only to a first approximation because

often it relies on the host system memory. System bus contention or differences in access times between the host and target system memories frequently create wait states during test that will not exist in the final product. Consequently, execution times measured thus during development will be different from the final product's.

The time it takes to set the instrument up for a test is also important both to the user, because it makes his life easier, and to his company, because the waste of his time costs money. Clearly, the logic analyzer has the advantage here. As their primary function is analysis, logic analyzers are built to do it easily, having such inherent advantages as key-per-function or menu-driven operation. A measurement executed with only one or two



7. Glitch-catching. At the dashed cursor, the display shows the glitch (channel 5) that causes a monostable circuit to trigger and thus generate a false interrupt signal. The ability to specify the glitch as part of the trigger condition is the only way to reliably distinguish the error condition from legitimate interrupt signals.

| TRACE SPECIFICATION | | TRACE-COMPLETE | | |
|---------------------|----------|----------------|----------|--------------|
| LABEL BASE | A OCT | D OCT | F BIN | OCCUR DEC |
| FIND IN SEQUENCE | 00035 | XXXX | | 00001 |
| THEN | 05700 | XXXX | | 00001 |
| [START] TRACE | 05726 | XXXX | | 00002 |
| SEQ RESTART [ON] | 02132 | XXXX | | |
| TRACE | | | | |
| [ONLY STATE] | 050X | XXXY | | 00001 |
| COUNT [STATE] | 05000 | XXXX | | |

| TRACE LIST | | | | TRACE-COMPLETE |
|---------------|----------|----------|----------|-----------------------|
| LABEL BASE | A OCT | D OCT | F BIN | STATE COUNT DEC |
| SEQUENCE | 00035 | 115320 | 0 | [OFF] |
| SEQUENCE | 05700 | 011472 | 0 | 13 |
| START | 05726 | 103135 | 0 | 5 |
| +01 | 05031 | 037233 | 0 | 23 |
| +02 | 05032 | 027042 | 0 | 3 |
| +03 | 05042 | 067232 | 0 | 1 |
| +04 | 05043 | 006103 | 0 | 2 |
| +05 | 05044 | 027061 | 0 | 1 |
| +06 | 05061 | 065717 | 0 | 1 |
| +07 | 05062 | 006002 | 0 | 1 |
| +08 | 05064 | 027111 | 0 | 1 |
| +09 | 05031 | 037233 | 0 | 394 |
| +10 | 05032 | 027042 | 0 | 3 |
| +11 | 05042 | 067232 | 0 | 1 |
| +12 | 05043 | 006103 | 0 | 2 |
| +13 | 05044 | 027061 | 0 | 1 |
| +14 | 05061 | 065717 | 0 | 1 |
| +15 | 05062 | 006002 | 0 | 1 |
| +16 | 05064 | 027111 | 0 | 1 |
| +17 | 05031 | 037233 | 0 | 338 |

8. Inside the program. By defining a series of trigger events as shown in (a), logic analyzer users can take a look at selected activity in, say, the middle of nested subroutines (b). This is a capability that is unavailable in present microprocessor development systems.

keystrokes on a modern logic analyzer could require a considerable amount of typing on the general ASCII keyboard of the typical development system.

A good overview of the analytical capability of the instruments can be obtained by seeing how they would handle typical measurements. The table on page 144 shows what kinds of problems are likely to occur where.

To analyze data-dependent errors, it is necessary to monitor not only the program flow but the data read from or written to the point of interest. So the trigger event will be the occurrence of a particular data word at a particular address, precluding the use of those development systems that trigger only on address information. It may be necessary to examine the effect the error has on downstream data, and this precludes the use of systems that trace only pretrigger events. Such selective traces are easily made in real time by logic analyzers (Fig. 6). On the other hand, microprocessor development systems that can also perform selective traces must often surrender real-time capability in order to operate in the debug mode. If the data-dependent error requires the processor's internal registers to be monitored, then the development system's in-circuit emulator and debug capabilities shine. While this type of error can be examined by a logic analyzer also, the analyzer must interrupt the processor and turn control over to a system's monitor program. This monitor may be an artifact the user is unwilling to add during product development.

Data transfer problems can be a real challenge, for data may either arrive at one rate and leave at another rate or be transformed, say, from serial into parallel form. Observations on transmissions of different rates cannot be made by development systems, which operate on a single clock, or by any logic analyzer that operates with a single clock. This situation requires a logic analyzer than can handle two or more clock rates.

Locating timing anomalies, glitches, and other similar gremlins on control lines is a measurement that belongs exclusively to logic timing analyzers. Development

systems cannot observe asynchronous events like those shown in Fig. 7. This figure is an example of a glitch causing a monostable to pulse, an event that results in a false interrupt. To solve the problem, the glitch was specified as part of the trigger conditions for separating the false interrupt from legitimate interrupts.

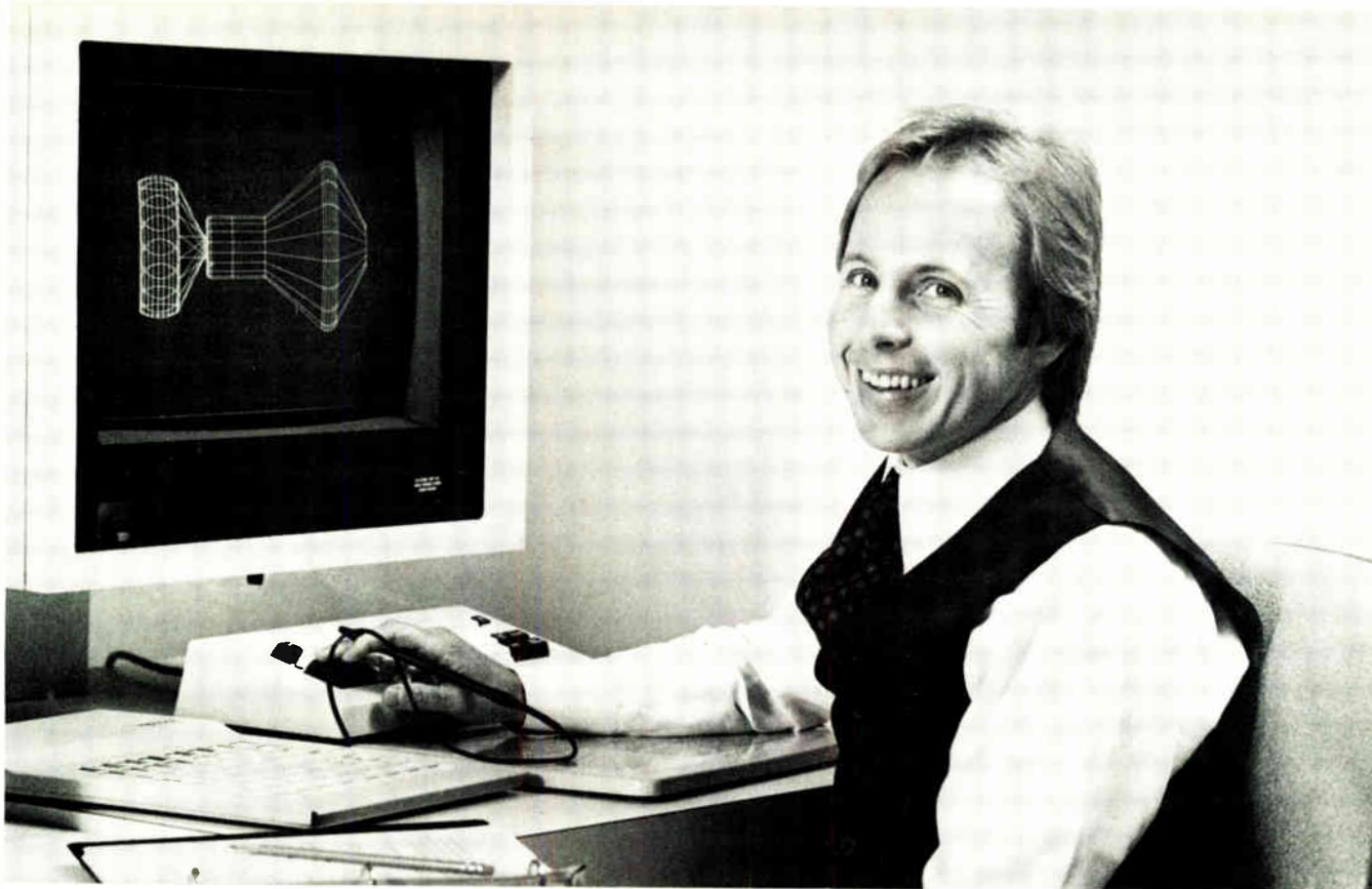
Many levels

Systems with more complex software further complicate things. For instance, software with many levels of nested subroutines or with recursive or re-entrant subroutines requires very sophisticated tracing capabilities. The only way to pinpoint a particular area of code may be to use trace specifications with several levels of sequential triggering. Tracing real-time capability of this degree is available in at least one logic analyzer on the market, but not yet in development systems.

Figure 8 illustrates a complex trace specification involving several levels of sequential triggering. Notice the restart term, which restarts the search for a given sequence when the entire sequence has not been found before the restart word appears.

In sum, then, the analytical capabilities of logic analyzers go well beyond those offered by typical microprocessor development systems. The logic analyzer, with its transparent real-time tracing features, becomes more valuable as problems become more subtle and more remote from the CPU. Yet the microprocessor development system is an efficient tool for software development and will also serve in the early stages of debugging an integrated system.

In a rapidly changing market, this article of necessity generalizes about what is currently available. Some of the analytic limitations attributable to the "typical" development system are absent in others—for instance, the 64000 recently announced by Hewlett-Packard has overcome many of these shortcomings. Nevertheless, a logic analyzer remains an integral part of the total systems analysis. □



David Lunn, Applications Engineer at Applicon, Inc.

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Cascaded regulators prevent pass transistor's burnout

by Christopher Tocci
Krohn-Hite Corp., Avon, Mass.

Cost-conscious designers are often tempted to squeeze every bit of available energy from a linear, voltage-regulated source that must deliver high output power, and the overheating and/or secondary breakdown that may result can cause component failures. In these cases, it will be less expensive to cascade several regulators so that no one element of any device, most notably the series-pass transistor, undergoes excessive electrical or thermodynamic strain. The design technique for achieving the n-cascade arrangement is described here.

The cascade connection of n regulators is shown in block form in (a). In general, if the following conditions are met, namely

$$V_{in} - V_1^o = V_2^o - V_1^o = \dots = V_{n-1} - V_o \quad (1)$$

$$V_i^s = V_i^f \quad (2)$$

$$V_i^f = \frac{1}{2}V_i^o \quad (3)$$

where

V_i^s = the resistor string voltage at the ith regulator

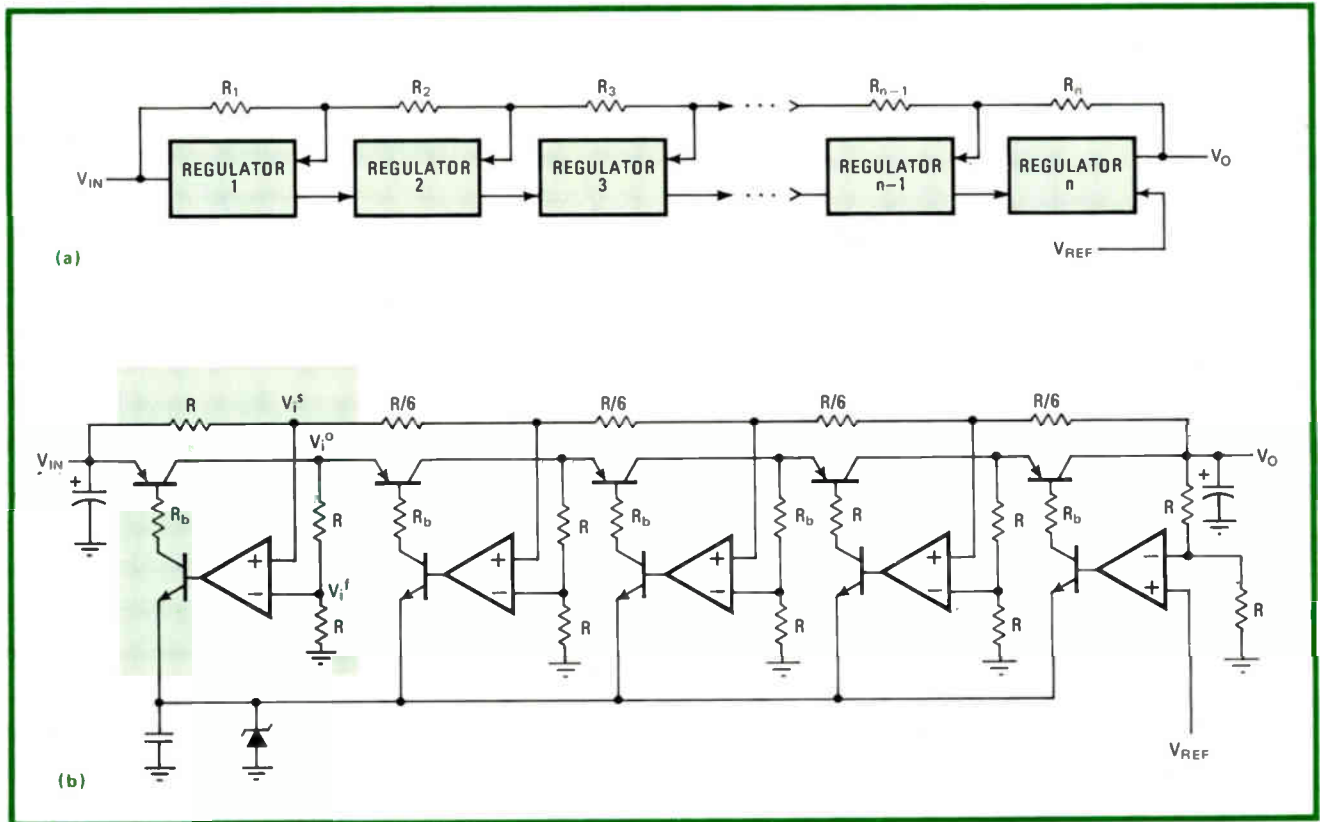
V_i^o = the local output voltage from the ith regulator

V_i^f = the local feedback voltage to the ith regulator

then $R_i = R/(n+1)$ for $i = 2, 3 \dots n$, if $R_1 = R$. More importantly, it can be shown that the voltage across the series-pass transistor of each regulator becomes $V_i^o - V_{i+1}^o = (V_o + V_{in})/n$.

Equations 1 through 3 can be realized by connecting each regulator together as shown for a discrete five-stage unit in (b), where R is selected arbitrarily, within the limits of the technology (transistors, op-amps, etc) of the active elements used in the regulators. Under this arrangement, $V_o = 2 V_{ref}$. The output voltage can be made variable over a greater range than 2:1 by appropriate selection of local feedback resistances. It is necessary that the op amps be of the type that can be operated from a single supply so that the feedback resistances R may be adjusted in order to attain the desired dynamic range.

Two problems are inherent in this design—the ripple generated at the nodes of the resistor string and the occurrence of oscillations due to unwanted feedback. The first problem is not a critical one because most of



Cooler. N-stage regulators (a) combine to equalize voltage drop across their respective series-pass transistors so that no device is destroyed by heat or breakdown, as may happen when high power is drawn through a single device. Design technique discussed in text is employed in discrete five-stage regulator (b). Supply ripple is eliminated at last stage. Oscillations are avoided with bypass capacitor in R/6 string.

the ripple will be eliminated by the last regulator, which derives its reference voltage from a stiff supply.

The second problem may be overcome by placing a large capacitor between the center of the resistor string and ground. Note that using too large a value of capaci-

tance, however, will cause a turn-on lag that is excessive and that may create a low-frequency oscillation. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

Calculator notes

HP-67/97 program plots antenna's polar pattern

by D. C. Mitchell
Milan, Mich.

Computing the radiation pattern of driven antenna arrays in polar form is easy with this HP-67/97 program. Given the relative spacing, phasing, and orientation of a multielement array having parallel or colinear half-wave elements in the horizontal plane, the routine tabulates the power gain of the array as a function of the incremental compass angle specified by the user.

The program solves the equation derived by Weeks¹:

$$P(\theta) = \left| 1 + \sum_{N=1}^n R_n B_n \cos(\theta_n - \theta_i) - A_n \right|$$

where:

$P(\theta)$ = the phasor sum magnitude of the interference pattern produced by n elements

R_n = the ratio of the power applied to the n th element

to the power supplied to the user-defined reference element, r

B_n = the relative spacing in electrical degrees between the n th element and r

θ_n = the orientation of the n th element with respect to r (0° if elements are in parallel, 90° if colinear)

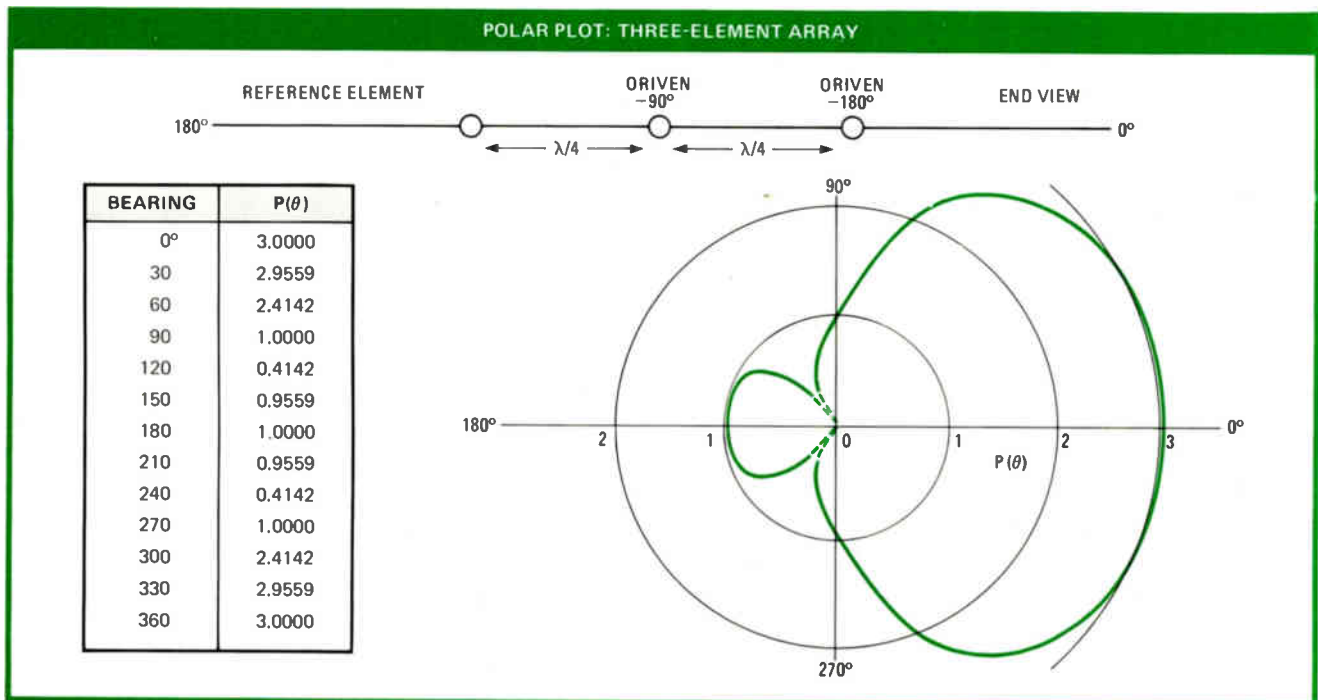
θ_i = the bearing, in degrees, at which field strength is measured

A_n = the relative phase in electrical degrees between element n and r .

Note that the directive (E-plane) pattern as tabulated is not affected by the antenna height above ground, although the user will need a set of ground-reflection factor charts² to find the relative gain at a specific take-off angle for a given antenna height and bearing.

An example illustrates the usefulness of the program. A three-element array is arranged as shown in the figure, with each member driven 90° out of phase (lagging) with its preceding element as measured with respect to the reference. $P(\theta)$ is required in increments of 30° , starting from 0° .

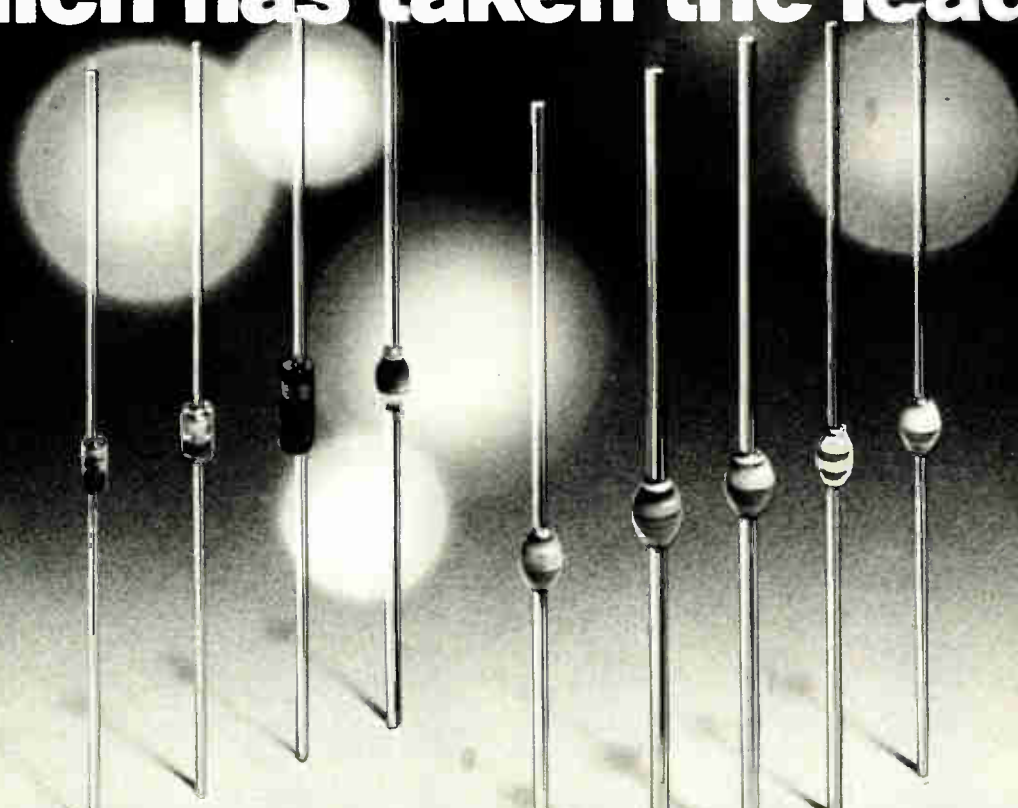
Thus $\theta_{incr} = 30^\circ$, $n = 3$, and for the second element, $A = -90^\circ$, $R = 1$, $\theta = 0^\circ$, and $B = 90^\circ$. Keying in these parameters, followed by $A = -180^\circ$, $R = 1$, $\theta = 0^\circ$ and



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|-----------------------------|-----------------|-----------------|-------------------|
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| BYW 32–BYW 36 | 200 V– 600 V | 2 A | |
| BYW 52–BYW 56 ¹⁾ | 200 V–1000 V | 2 A | – 1N 5059–1N 5062 |
| BYW 72–BYW 76 | 200 V– 600 V | 3 A | |
| BYW 82–BYW 86 ¹⁾ | 200 V–1000 V | 3 A | – 1N 5624–1N 5627 |
| BYX 82–BYX 86 ¹⁾ | 200 V–1000 V | 1,5 A | |

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$B = 180^\circ$ for the third element, yields the tabulated results as shown, from which the polar plot is constructed.

Note that the analysis of parasitic arrays is possible

with this program if the effective power ratios, R_n , and the relative phase factors, A_n , are known.

References

1. W. L. Weeks, "Antenna Engineering," McGraw-Hill, 1968.
2. J. Kraus, "Antennas," McGraw-Hill, 1950.

HP-67/97 PRINTER LISTING: E-PLANE RADIATION PATTERN FOR DRIVEN ANTENNA ARRAYS

| | | | | | | | |
|-----|--------|-----|--------|-----|--------|-----|--------|
| 001 | *LBLA | 032 | CHS | 063 | FRC | 094 | RCLB |
| 002 | CF1 | 033 | X | 064 | X < 0? | 095 | DSP0 |
| 003 | STOD | 034 | ST + i | 065 | CHS | 096 | PSE |
| 004 | ISZI | 035 | P ≠ S | 066 | → R | 097 | PSE |
| 005 | RTN | 036 | ISZI | 067 | ST + 0 | 098 | RCLE |
| 006 | *LBLB | 037 | RCLi | 068 | X ≠ Y | 099 | DSP4 |
| 007 | STOA | 038 | RCLA | 069 | P ≠ S | 100 | PRTX |
| 008 | RTN | 039 | X = Y? | 070 | ST + 0 | 101 | RCLB |
| 009 | *LBL1 | 040 | GTO0 | 071 | P ≠ S | 102 | 3 |
| 110 | RTN | 041 | GTO1 | 072 | RCLi | 103 | 6 |
| 011 | *LBLC | 042 | *LBL0 | 073 | 1 | 104 | 0 |
| 012 | STOi | 043 | RCLB | 074 | X ≠ Y | 105 | X ≤ Y? |
| 013 | X < 0? | 044 | P ≠ S | 075 | X ≤ Y? | 106 | GTO2 |
| 014 | SF1 | 045 | DSZI | 076 | GTO3 | 107 | 0 |
| 015 | RTN | 046 | RCLi | 077 | GTO0 | 108 | STO0 |
| 016 | *LBLc | 047 | INT | 078 | *LBL3 | 109 | P ≠ S |
| 017 | EEX | 048 | - | 079 | RCL0 | 110 | STO0 |
| 018 | 6 | 049 | COS | 080 | P ≠ S | 111 | P ≠ S |
| 019 | CHS | 050 | RCLi | 081 | RCL0 | 112 | RCLB |
| 020 | F1? | 051 | FRC | 082 | X ≠ Y | 113 | RCLD |
| 021 | CHS | 052 | 1 | 083 | P ≠ S | 114 | + |
| 022 | ST + i | 053 | EEX | 084 | → P | 115 | STOB |
| 023 | RTN | 054 | 6 | 085 | 1 | 116 | RCLA |
| 024 | *LBLD | 055 | X | 086 | EEX | 117 | STO1 |
| 025 | P ≠ S | 056 | X | 087 | 6 | 118 | GTO0 |
| 026 | STOi | 057 | P ≠ S | 088 | X | 119 | *LBL2 |
| 027 | RTN | 058 | RCLi | 089 | → R | 120 | CLRG |
| 028 | *LBLd | 059 | INT | 090 | 1 | 121 | P ≠ S |
| 029 | 1 | 060 | CHS | 091 | + | 122 | CLRG |
| 030 | EEX | 061 | - | 092 | → P | 123 | CF1 |
| 031 | 6 | 062 | RCLi | 093 | STOE | 124 | R/S |

| Registers | | | | | | | | |
|----------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|---|---|
| R ₀ | R ₁ | R ₂ | R _n | S ₁ | S ₂ | S _n | A | C |
| Temporary | A ₁ R ₁ | A ₂ R ₂ | A _n R _n | θ ₁ B ₁ | θ ₂ B ₂ | θ _n B _n | N | θ |

| Instructions |
|--|
| <ul style="list-style-type: none"> • Key in program • Enter angle increment for which tabulated results for $P(\theta)$ are desired and number of elements in array (θ_{incr}, A, (N), B). • Specify phase lag between reference and second driven element, ratio of power applied to second element versus the reference power, and relative position and spacing of elements (A), C, (R), f, c, (θ_n), D, (B), f, d. • Repeat previous step as required for third to nth elements. Program is executed automatically upon receipt of all information, displaying angle, then printing the relative power output for that angle. |

An Innovative way to stay current with computer Innovations

Keeping up with the breakneck pace of technological innovation in computer systems requires some innovation in continuing education for engineers. A unique experiment along those lines is being sponsored by the Profession Development Committee of the Institute of Electrical and Electronics Engineers' Computer Society.

The 15 one-day courses are being organized in three groups over the week of Dec. 10-14 and will be held at the Hotel del Coronado in San Diego, concurrently with the DEC User Society meeting at the Town and Country Hotel in that city. Software engineering and development will be handled in Track 1 of tutorials, while **distributed processing and communications will be covered in Track 2**. A variety of microprocessor and applications topics will be included in Track 3. Registration fees are \$85 per tutorial or \$400 for the whole week for IEEE members (\$100 or \$475 for others). For additional information and registration details, write to Tutorial Week '79, P. O. Box 639, Silver Springs, Md. 20901.

Interactive software speeds up circuit design

With computer-aided design becoming an almost standard tool for engineers of electronic devices, design software is becoming more important. One such new software package, called F/Logic, is now available from Canada's Bell-Northern Research Ltd. Running on an IBM System/370 or 303X computer with the VM/CMS operating system, the F/Logic package can simulate circuits with up to 32,000 gates.

Its interactive software helps **accelerate the design process by making it easier to evaluate design alternatives and to explore component and timing tolerances**. It can test worst-case timing conditions, simulate over 100 faults in parallel, and check out circuits with its own random pattern generator or else with user-created custom test patterns. Graphic displays of output waveforms can be produced on a terminal, a line printer, or a plotter under the control of the program and are supplemented by a printed summary. Licenses to use the F/Logic software and documentation can be purchased through Roger Fetterman at Bell-Northern's U. S. subsidiary, BNR Inc., Stanford Industrial Park, 3174 Porter Drive, Palo Alto, Calif. 94304.

New calculator solves equations and Integrates

Finding real roots of equations or the definite integral of a function can be a laborious—if not impossible—task with most hand-held calculators. But Hewlett-Packard's Corvallis division has added algorithms to perform those functions to its new HP-34C calculator. The programmable unit, selling for \$150, also has 70 lines of program storage, 20 data registers, and a continuous memory that enables the calculator to continue storing programs even while it is turned off. When needed, the 20 data registers can be converted to store up to seven lines of programming each, **allowing a total of 210 program lines to be stored**.

The company has also introduced continuous-memory versions of its HP-33E and 38E calculators. Called the HP-33C and HP-38C, the new versions have been priced at \$120 and \$150 respectively. Additional information on any of the new units can be had by writing to the Inquiries Manager, Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304.

-Anthony Durniak

Our SIP Capacitor Network gives you thousands of choices.



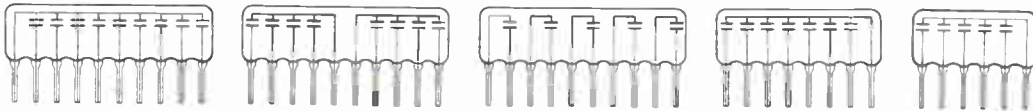
And saves you money.

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One of our 11 standard patterns will probably meet your circuit require-

ments. If not, choose a 12th — your own. Send us your requirements and we'll put our designers to work for you. (Or send today for your free copy of our handy Designer's Guide — and design your own package.)

The point: We'll make your SIP Capacitor Network the way you want it — and give you the high reliability our expertise in capacitor manufacturing guarantees.

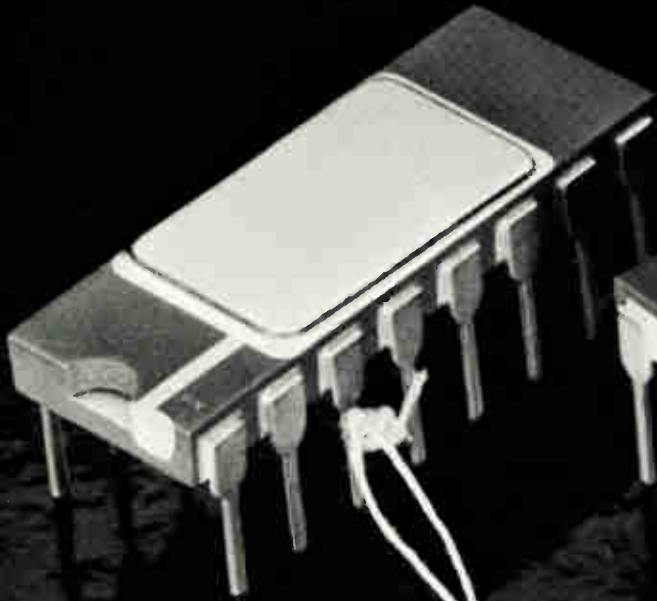


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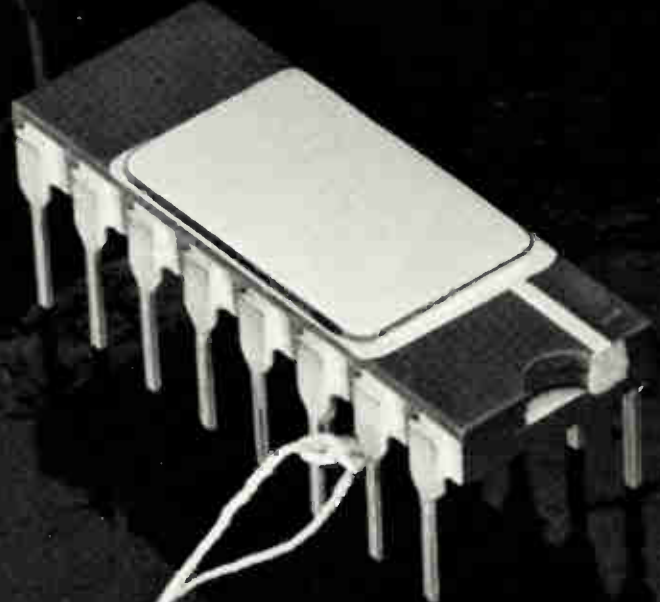
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\$18



\$15

There may be no difference.

But, because of cautious test system guard bands, too many high performance memories are downgraded, their potential lost to manufacturers as a revenue source and to users as a factor in new designs.

Now, however, the new J387A Memory Test System from Teradyne lets you set the tightest guard bands ever. Its half-nanosecond accuracy in edge placement gives you higher yields of premium devices. And you can bin with added confidence throughout the performance distribution of a memory design.

The J387A delivers its half-nanosecond accuracy with plenty of speed, too. You get 20 MHz for dynamics, and 40 MHz for statics.

Plus the flexibility of 16 independent timing sets for testing complex devices like the 5-volt, address-multiplexed, page-mode memories.

Couple the accuracy, speed, and flexibility of the J387A with its powerful software and uncommon system reliability. Factor in Teradyne's Automatic Edge Control II, which eliminates manual calibration. And add, for engineering applications, the optional Real-Time Bit Mapping for chip evaluation and characterization down to the bit level.

The result is a superb production, incoming inspection, and engineering memory test system, whose performance and correlation are unrivaled in the industry.

The Teradyne J387A Memory Test System. It gives you A Definite Edge. And that can make all the difference.

For more information, write: Memory Product Group, Teradyne, Inc., 21255 Califa Street, Woodland Hills, California 91367.

WHAT'S THE DIFFERENCE BETWEEN AN \$18 MEMORY AND A \$15 MEMORY?

American Optical gives you a big stage...for a really big show.

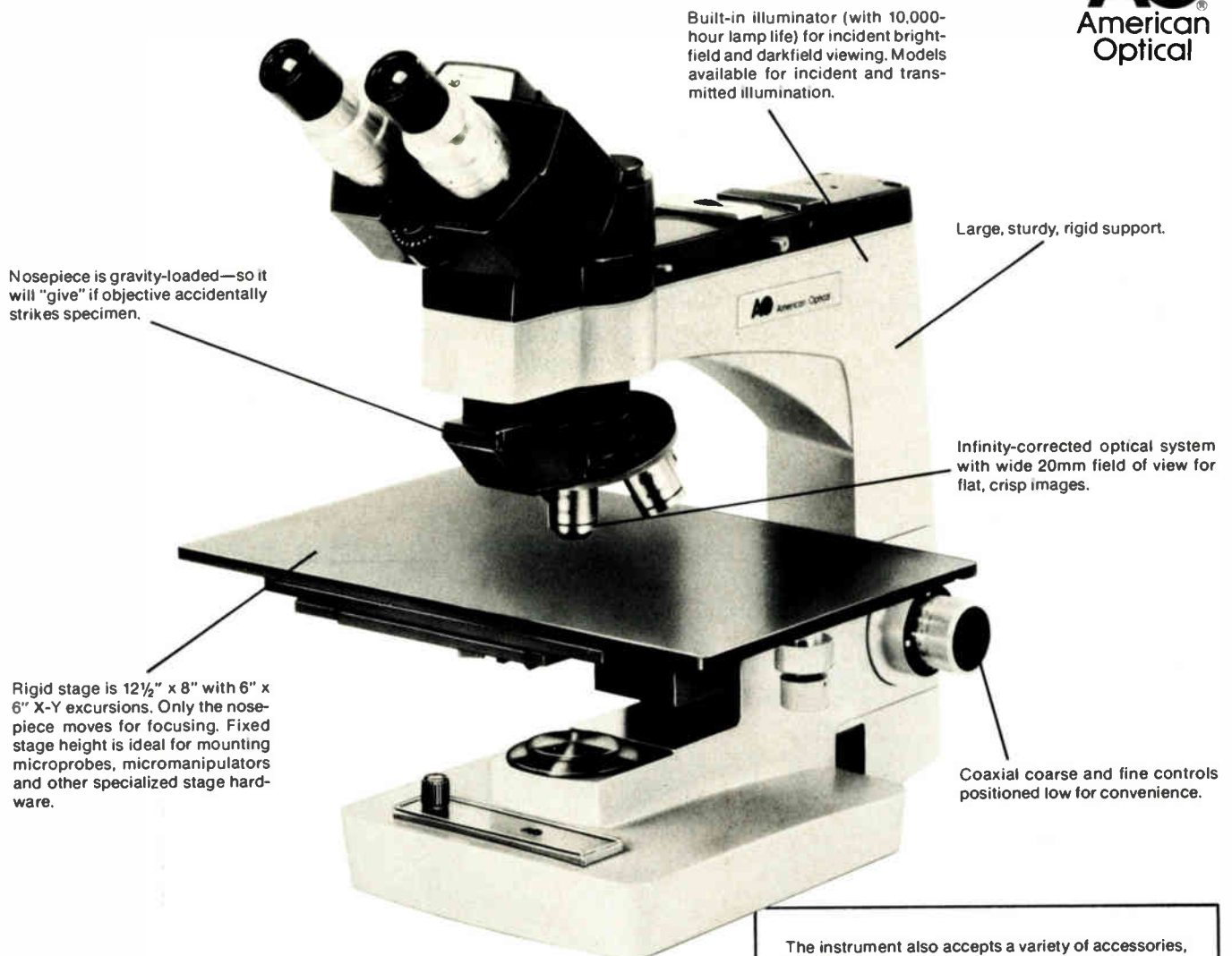
The AO® Series 1860 Industrial Microscope offers a 12½" x 8" stage with a full 6" x 6" X-Y stage travel, for quality control, failure analysis, fabrication or general inspection of masks, wafers and other microelectronic components.

With exclusive AO nosepiece focusing, the stage height remains fixed for excellent stability and easier use of ancillary equipment.

And the stage will accept carousels or any other commercially available stage hardware.

If you'd like to see how an AO Series 1860 Industrial Microscope can fit into your production number, contact your American Optical dealer for a demonstration. Or call or write: American Optical, Scientific Instrument Division, Buffalo, NY 14215; (716) 895-4000.

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Built-in illuminator (with 10,000-hour lamp life) for incident bright-field and darkfield viewing. Models available for incident and transmitted illumination.

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Nosepiece is gravity-loaded—so it will "give" if objective accidentally strikes specimen.

Infinity-corrected optical system with wide 20mm field of view for flat, crisp images.

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Coaxial coarse and fine controls positioned low for convenience.

The instrument also accepts a variety of accessories, including those for dual viewing and multi-viewing, photomicrography and differential interference contrast. Ask your dealer for details.

Modular counter can be customized

Microprocessor-controlled mainframe accommodates four input-signal-conditioning units for time and frequency measurements

by Bruce LeBoss, West Coast Editor, Computers & Instruments

Users in the market for universal counter/timers have often had to buy more capability than they really needed. But thanks to a new concept in frequency and time measurement from Systron-Donner Corp., users now can specify the actual measurement capability of these instruments by selecting from a spectrum of functional modules.

Unlike earlier universal counter designs that were either discrete instruments with a fixed range of frequencies and measurements or mainframes into which only a single frequency module could be plugged at any one time, the new UC 1100 from Systron-Donner's Concord Instruments division is a microprocessor-controlled mainframe that has space for four functional modules. "For the first time, an instrument can be configured, using an array of input-signal-conditioning modules, to perform measurements in the time domain, for low frequency, or rf in the same instrument," claims product manager Neil Harrer.

To be introduced at next week's Wescon exhibition in San Francisco, the UC 1100 is based on a Motorola 6802 8-bit microprocessor that gives the user total control over the specified signal-conditioning modules. What's more, the microprocessor provides system management functions and interfacing to the IEEE-488 bus.

The UC 1100 mainframe features two identical channels—dual eight-digit light-emitting-diode displays, and associated controls—that make possible simultaneous measurements of different parameters, such as frequency, period, period average, time interval, time-interval average,

ratio, and ratio average, as well as totalizing and complex mixed simultaneous measurements.

The initial signal-conditioning modules to be introduced will include: a 100-MHz input amplifier; 512-MHz and 1.25-GHz prescalers; and a 3½-digit voltmeter. These input modules will allow direct measurement of frequency up to 100 MHz, period and time interval to a resolution of 10 ns, ratio to 105, and totalize, Harrer points out. The DVM, he explains, is available to monitor universal input module trigger levels or to display external dc voltages on its own LED display.

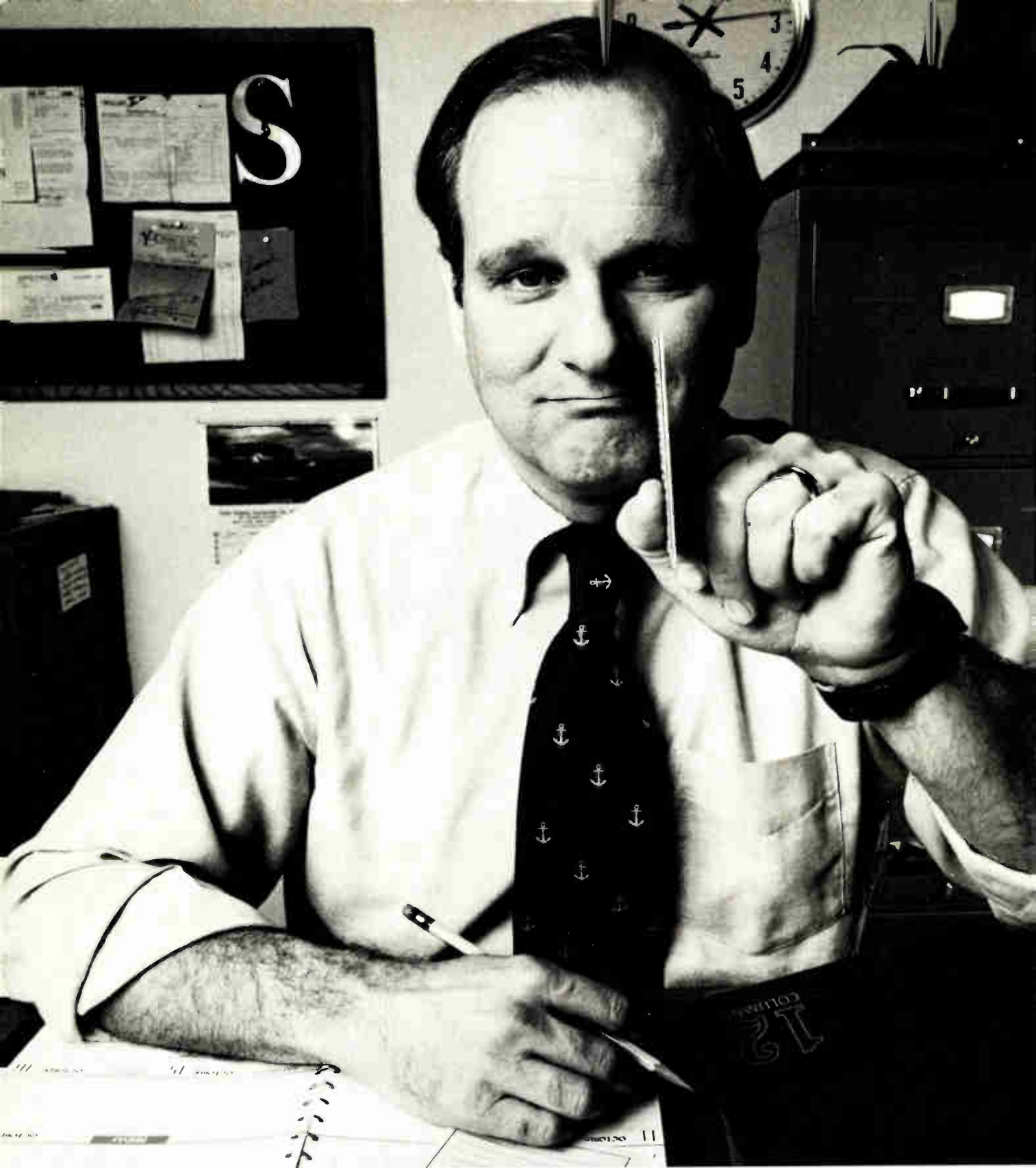
According to Harrer, future modules will extend the measurement capability of the UC 1100 through the microwave range, while allowing measurement of the input level and providing frequency offsets. Among those modules planned next for the mainframe are 6.5-, 18- and optional

24- or 26-GHz prescaler inputs, as well as a pulsed-rf module that will measure carrier frequency, pulse width, and pulse repetition rate, for example. Subsequent modules will include: a 520-MHz direct-counting input; an offset module that allows the user to do addition, subtraction, multiplication, and division, all linked to the display; and various computer/calculator controls.

Measuring 3.5 by 17 by 17 inches, the UC 1100 is a full-rack instrument that is targeted for systems applications such as those in the military and the automatic test equipment marketplaces. However, the UC 1100 can also be used on a bench, Harrer says. Available around the end of this year, the basic UC 1100, with the initial four plug-in modules will cost about \$2,000.

Systron-Donner Corp., 10 Systron Dr., Concord, Calif. 94518. Phone Neil Harrer at (415) 676-5000 [339]





**THIS IS GENERAL ELECTRIC
SUPPLY'S COMPETITIVE EDGE
FROM BELL.**

PROBLEM:

General Electric Supply Company (GESCO), a division of the General Electric Company, sells in a highly competitive market. Many of the 80,000 products it offers are matched in performance by those of other distributors, which puts extra emphasis on cost and customer service.



Buyers have been buried in catalogs.

Buyer and seller alike felt the growing administrative expense. Getting and giving price quotes, checking availabilities, taking and confirming orders were highly labor-intensive chores.

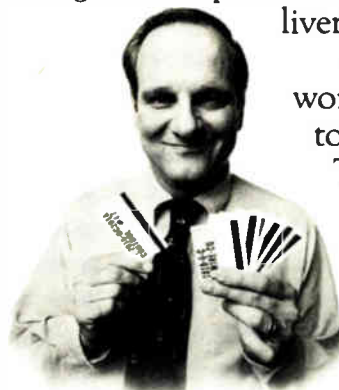
And with every order came a flurry of paperwork, often repetitive, always time-consuming and error-prone, too often snarled in mail hang-ups.

What GESCO needed was a way to streamline the whole process, build orders, and reduce paperwork for itself and its customers.

What GESCO needed was a way to streamline the whole process, build orders, and reduce paperwork for itself and its customers.

SOLUTION:

GESCO, working with a Bell System team of data experts, developed a new order entry and processing system, which GESCO calls SENTRY. It reduces the repetitive pricing calls by offering customers supplies on a contract basis, with agreed-on prices and responsive delivery times. And to eliminate paperwork, the system is totally automated.



The customer slides his identification card through...

...and enters the order in seconds. At GESCO, picking tickets and purchase orders are automatically generated, and a copy goes back to the customer.



...a Transaction telephone for quick push-button ordering.

The time and expense the customer saves are a clear value added to GESCO's services—a decisive competitive edge.

If you haven't talked systems with your problem-solving Bell Account Executive lately, your company is missing something.

The system is the solution.



\$28,000 unit tests memory and logic

Digital IC tester performs functional tests on 48-pin, VLSI devices with two microprocessors and a microprogrammed sequencer

by James B. Brinton, Boston bureau manager

A digital integrated-circuit tester should cover the gamut of today's memory and logic chips to be effective. GenRad's latest digital IC tester, the 1732, promises to do just that: test anything from small- and medium-scale devices to very large-scale integrated circuits. The 1732, a companion tester to the 1731 analog IC test system introduced five months ago [*Electronics*, March 29, p. 136], performs dc and functional tests on most of the digital ICs that are now available.

According to John T. Chase, 1732 product marketing manager, the console-sized system will test the largest available memory chips and all microprocessors except for a few 16-bit devices in 64-pin packages. The system already boasts a test library covering more than 150 devices using complementary, p-

channel, and n-channel MOS, and TTL, emitter-coupled, high-threshold, and integrated injection logic.

"We are aiming at the peak of the benchtop market," says Chase. "We have decided to offer as many of the capabilities of large testers as possible, at as low a price as possible." They seem to have succeeded: base price for the smallest 1732, capable of testing ICs in 16-lead packages, is \$28,000. The tester expands in \$4,000, 8-pin increments, to reach a 48-pin capability at \$44,000.

Flexibility. The designers have crammed this much capability into the 1732 by using two microprocessors and a sequencer: a Z80 to control test, calculation, and display, a 6502 for data-cartridge mass-storage control, and a high-speed 2910 microprogrammed sequencer to apply test patterns to devices under

test. There is yet more capability with the use of combined drive and sense pins—each equipped with 4 K by 4 bits of memory—and several sophisticated programming tricks.

The 1732's high-speed, microprogrammed test-pattern processor runs tests and implements subroutines and looping instructions. These instructions allow specific test patterns to be extended to tens of thousands of steps, enough to exercise the most complex microprocessor, according to GenRad. Simultaneously, microinstructions simplify test-pattern generation.

The test-pattern processor is connected to the device under test using the memory-backed drive or sense pins. These circuits can switch from driver to sensor at 2 MHz for checking bidirectional data pins or to test float in three-state devices. Input voltages are program-controlled, as are sensor thresholds. Device outputs are loaded by a pair of programmable current sources to guarantee worst-case operating conditions.

Self-test is automatic, as is calibration; all 1732 internal voltages are compared with a precision voltage reference, and system offset and gain variations are recorded automatically before the start of a test. These readings are used by the 1732's software to allow for system deviations and to correct system outputs.

The memory at each pin allows significant test parameter flexibility. There is a choice of: two drive voltages and two sense-voltage windows, two sets of programmable sensor currents for loading device outputs, two driver latch times, and two sensor strobe times. Each drive or



Johanson

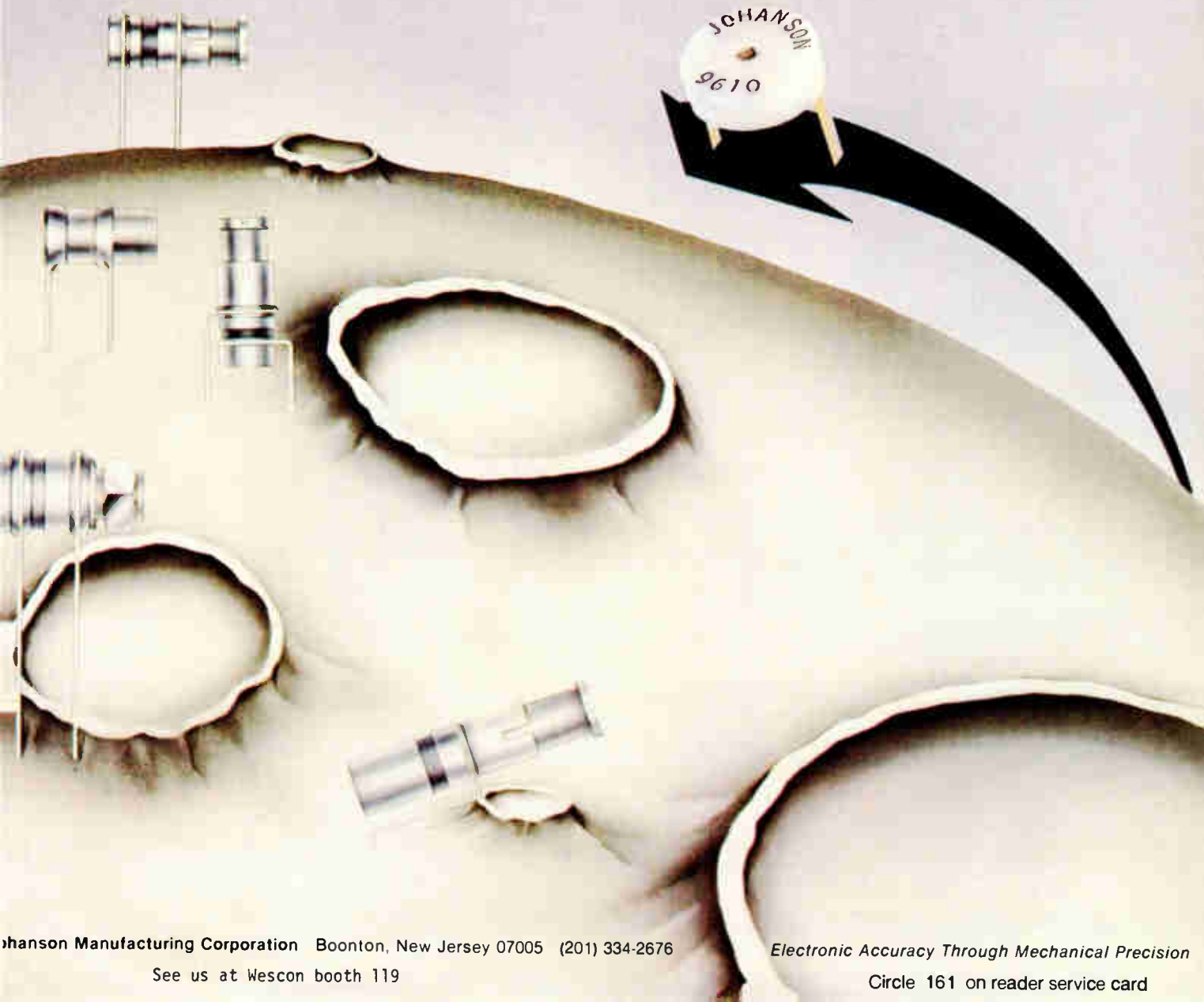
WELCOMES A NEW PRODUCT
TO THE FAMILY.

Seal Trim™ Ceramic Capacitors

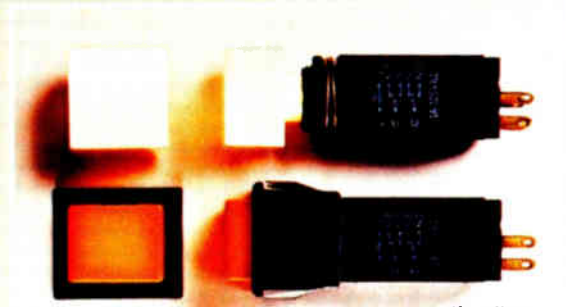
- WITHSTANDS WAVE SOLDERING. ■ CONFORMS TO SPECIFICATION MIL-C-81.
- HIGH Q FACTOR AND FREQUENCY RESPONSE. ■ LOW TEMPERATURE COEFFICIENT AND DRIFT RATES. ■ IMPERVIOUS TO ALL STANDARD P.C. BOARD CLEANING SOLVENTS. ■ TAMPER PROOF, NON-SLIP ADJUSTMENT WITH UNIQUE SQUARE DRIVE TUNING.

SEAL TRIM™ capacitors are a new, innovative outgrowth of the popular Johanson "Thin Trim" capacitor family. These sealed miniaturized variable ceramic capacitors are intended for microwave, RF, video and digital applications, where small size and contamination-free operation are required (.250 dia.).

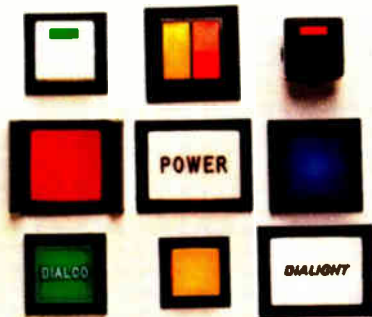
The sealed capacitor body is designed to prevent the intrusion of solder flux, cleaning agent and atmospheric contamination.



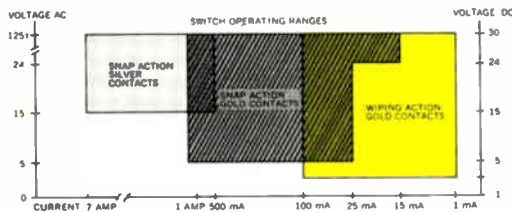
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554 SERIES Snap-action illuminated switches with gold or silver contacts . . . Wiping-action switches with gold contacts. Rated life: up to 750,000 operations. Bezel or panel mounting available. Choice of over 300 cap shapes, sizes and colors . . . choice of legends. Listed by Underwriters Laboratories and CSA approved.



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This chart is intended to be used as a general guide only.
†125 VAC applies to snap action switches only

554 SERIES You'll find a Dialight illuminated switch within your desired operating range. The above chart will make your selection easier.

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Circle 162 on reader service card

New products

sense pin may be programmed independently during testing.

Test programming uses a fill-in-the-blanks process, with four programming displays called up on the unit's small cathode-ray tube. Each display describes the data to be filled in, and the operator need only use the calculator-like keypad to enter it; all parameters are entered in simple decimal units of current or voltage.

Because the drive/sense pins are universal, the operator can determine the function of each pin during any phase of testing; the programming display shows only the pins needed for a given test and the programmer fills in a function under each pin number. This information is carried forward to truth-table displays containing the input and response data required to perform a functional test. Truth-table entries are made just as pin assignments are, and since the role of each pin is defined, the system rejects illegal or inappropriate entries. Special micro-instructions in the pattern-processor system allow portions of the truth table to be written as subroutines or inside loops. This reduces greatly the number of entries needed to build up complex test patterns.

The process is further sped by the unit's learn mode; an operator enters an L in a truth table for any unknown output state. A known good device is then tested and its output states are used to fill in designated data automatically.

After testing, data can be fed out of the 1732 via an IEEE-488 interface or a 20-mA current loop, or to an optional printer. It can also be stored in an on-board data cartridge.

The 1732 interfaces with wafer probers and with manual and automatic handlers of packaged devices. Its socket adapter system can easily be combined with a remote handler, since all test electronics are located within it and only control signals and test results must travel to and from the small main console.

First deliveries are scheduled to begin in February 1980.

GenRad Inc., 300 Baker Ave., Concord, Mass. 01742. Phone John Chase at (617) 369-4400 [338]



Fastest EPROM ever. Plus a low-power 32K...a faster 16K. All new from Texas Instruments.

At 250 ns max access, TI's new TMS2508 is the fastest EPROM on the market. It's made to order for state-of-the-art microprocessor systems. Reduces wait states, virtually eliminates the need for additional circuitry.

The TMS2508 is a true single 5-V supply, 8K device. Designed for speed, it provides all the outstanding characteristics of TI's 5-V EPROMs: 8-bit word

configuration. Automatic chip select power down. Fully static operation. Simplified programming — singly or in blocks, sequentially or at random.

A very low power 32K also joins TI's growing EPROM family. The new 5-V TMS25L32 requires 40% less power than its standard counterpart. Active power dissipation is only 500 mW max — the lowest power per bit yet for

EPROMs. Input noise immunity: 400 mV, high and low ends.

A high-performance 16K EPROM is now available from TI. The new 5-V TMS2516-35 features 350 ns max access time versus 450 ns for the standard 16K with no increase in power.

Compatible, available family: All TI EPROMs are pin compatible in rugged 24-pin dual-in-line ceramic packages. Upgrading is simple, since the family concept is designed into every new EPROM.

All offer state-of-the-art performance and all are in production.

To get the new, super fast 8K, or any other member of TI's EPROM family, call your nearest TI distributor. Or for more information, write Texas Instruments Incorporated, P. O. Box 1443, M/S 6955, Houston, Texas 77001.



| TI's Growing EPROM Family | | | | | | |
|---------------------------|-------------|--------------|------------------------------|---------|-------------|-----------------|
| Device | Description | Power Supply | Max Power (0°C) Operating | Standby | Access Time | 100-piece Price |
| TMS25L32 | 32K | 5 V | 500 mW | 131 mW | 450 ns | \$102.00 |
| TMS2532 | 32K | 5 V | 840 mW | 131 mW | 450 ns | 53.80 |
| TMS2516-35 | 16K | 5 V | 525 mW | 131 mW | 350 ns | 55.40 |
| TMS2516 | 16K | 5 V | 525 mW | 131 mW | 450 ns | 36.92 |
| TMS2508-25 | 8K | 5 V | 446 mW | 131 mW | 250 ns | 36.90 |
| TMS2508-30 | 8K | 5 V | 446 mW | 131 mW | 300 ns | 30.80 |
| TMS2716 | 16K | +12, +5 V | 720 mW | — | 450 ns | 24.60 |
| TMS27L08 | 8K | +12, +5 V | 580 mW | — | 450 ns | 16.90 |
| TMS2708 | 8K | +12, +5 V | 800 mW* | — | 450 ns | 12.30 |
| TMS2708-35 | 8K | +12, +5 V | 800 mW* | — | 350 ns | 15.40 |

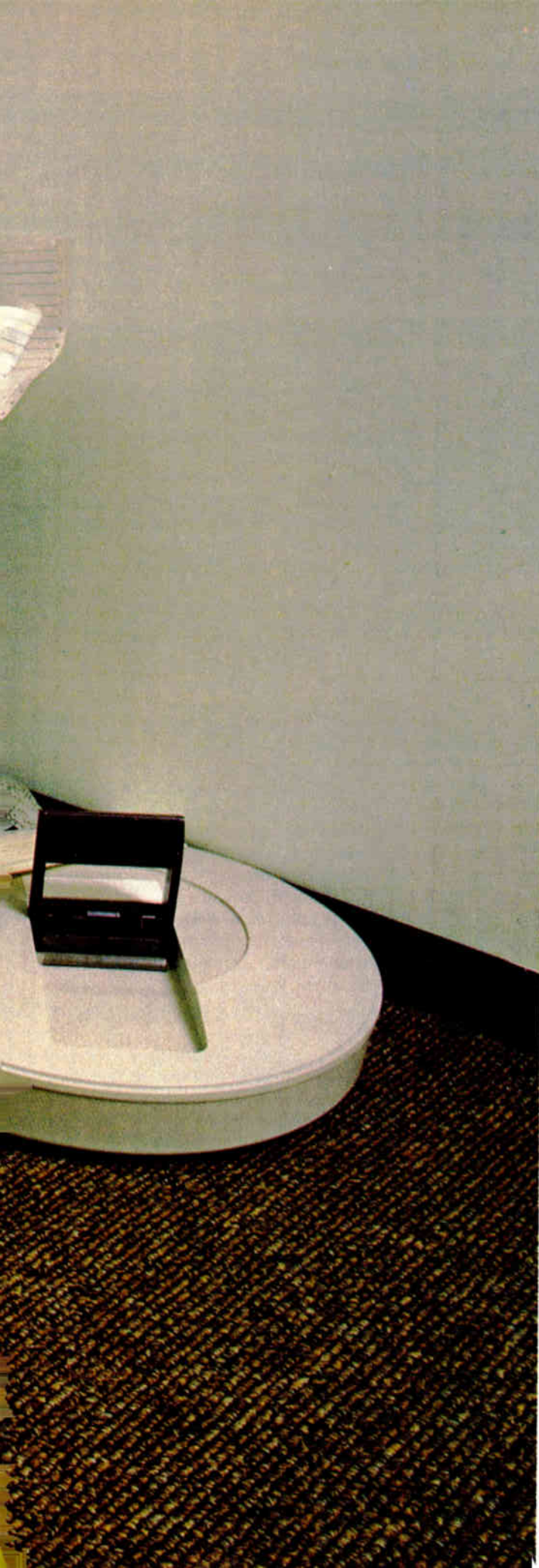
*T_A = 70°C

TEXAS INSTRUMENTS
INCORPORATED

Circle 163 on reader service card



**This year's OEM hardware shouldn't cost you
last year's OEM software.**



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At Digital, our approach has always been to give OEMs more than just great products. Just as important are the extra quality features, the extra testing that can make your design and marketing job easier. The worldwide service capability that can be tailored exactly to the way you run your business. It's an approach designed to help you meet a wide range of computer strategies.

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**We build a lot more than performance
into an OEM computer.**

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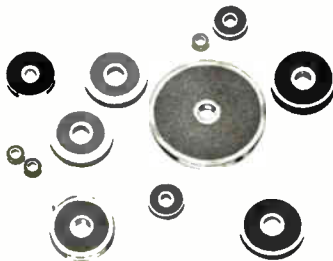
ERIE MONOBLOC® Ceramic Capacitors...

Now available in
**TUBULAR and
DISCOIDAL
FORM**



MONOBLOC TUBULAR Ceramic Capacitors

ERIE offers a multitude of sizes and capacitance values in tubular monolithic ceramic construction. The tube can be solid dielectric or buried electrode type in both Pi and feed-thru "C" configurations. For additional data write for Bulletin MT-100.



MONOBLOC DISCOIDAL Ceramic Capacitors

ERIE offers a wide range of discoidal capacitors... many as standard stock items. These reliable discoidals have a capacitance range from 10 pF to 5 μ F with a typical voltage range of 28 Vdc to 250 Vac. For additional data write for Bulletin MD-500.

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New products

Instruments

Ac meter reads 2 μ W at 1 GHz

Rf comparator provides
NBS-traceable measurements
with only 1% uncertainty

A null measurement technique that permits highly sensitive measurements of voltages from 100 kHz to beyond 1 GHz is achievement enough for a new 50- Ω voltmeter system. The new Ballantine series, based on a National Bureau of Standards design for radio-frequency comparators, also comes with an attractive price.

Company president Fred L. Katzmann calls the system, being introduced at this week's Wescon show in San Francisco, "a way of getting to NBS traceability that just hasn't been done before." Working with a differential alternating-current voltmeter, it comprises a \$985 1610A control unit and either the \$850 low-voltage 16101A comparator head or the \$695 16102A high-voltage head, or both.

Ballantine says the new system can be calibrated with respect to the NBS prime voltage standard for a

measurement uncertainty of less than 0.1%. Over the full frequency range, uncertainty is typically less than 1%. The system anticipates user interest for calibration and NBS certification of communications and navigation systems, rf signal generators, millivoltmeters, amplifiers, and attenuators.

Especially important, says the firm, is its use in rf power-meter verification. It can make NBS-traceable power-meter checks up to 1 GHz and down to 10 mV at 50 Ω (2 μ W). The lowest traceable levels in earlier precision voltmeters were about 1 mW, or 224 mV at 50 Ω , Ballantine maintains.

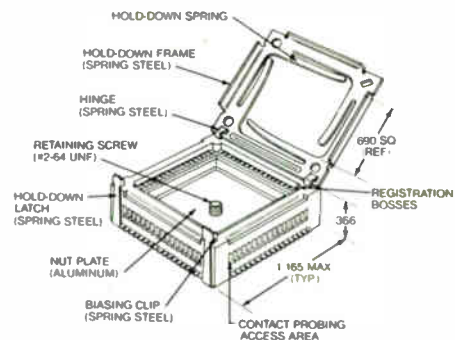
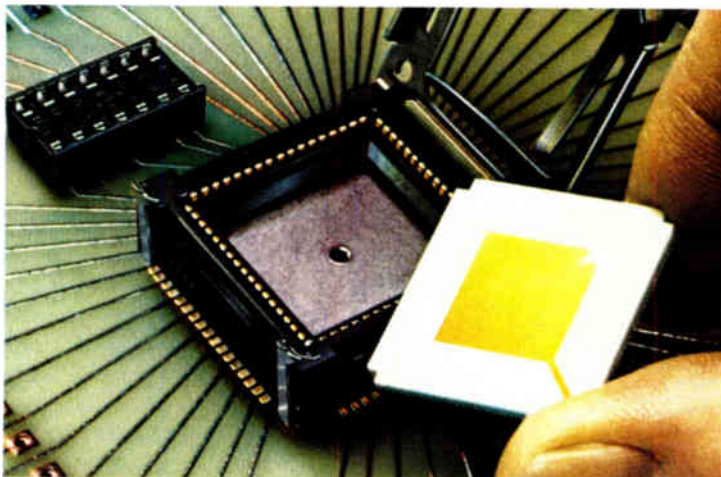
Measurement begins by comparing the unknown signal with an accurately known reference voltage generated by an ac voltage calibrator in the 1-to-100-kHz range. These voltages, of widely divergent frequencies, feed a pair of matched Schottky diodes, one positive and one negative, and then are algebraically summed in the comparator. The summing network's output is proportional to the difference between the two voltages, and the user reduces it to zero by varying the ac reference voltage until the 1610A control unit indicates a null. Then he need only read the output of the reference ac voltage calibrator, which is the same as that of the unknown voltage.





“Those new four-sided substrates can help make some really incredible advances in packaging. But how do you connect them to the board?”

Easy. New AMP ADS Connectors.



With the new AMP Active Device Substrate Connector you can design those compact, new four-sided substrates right into your boards and start saving real estate.

This unique 68-position connector accepts a leadless ceramic LSI chip carrier (Type A JEDEC LST Package Standard). And that's just the beginning.

The whole AMP substrate-connector package delivers far greater design elegance to your boards. You can use shorter traces. You can equalize trace lengths. You can enhance both the accuracy and speed functions. And, just as important, you can go into production with these benefits working for you right now.

Mounting the connector is simple. One screw holds it down. Alignment guides are built in,

assuring proper registration of the high pressure contact to board pads. A solder-to-board version is available too.

A hinged window-frame device on the connector permits a finned heat sink while exerting more than 50 grams normal force per contact on the pads of the ceramic package. You're assured of a truly reliable interface.

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Let NEL's years of frequency control experience work for you. Our clock oscillators are available over the frequency range 600~ to 60 MHz. We supply either TTL or CMOS compatible units in our all-metal, resistance weld sealed Dip package. Write or call for Data Sheets 7810A (TTL), 7810B (CMOS), or 7902A (Overtone).

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168 Circle 115 on reader service card

New products

Other precision voltmeters use thermal sensing technologies, in which the signals feed through some sort of temperature-sensitive resistive devices. However, the problems associated with resistors then need to be overcome, often at considerable cost. These include: sensitivity to ambient temperatures, insensitivities at very low power levels, and power dissipation at points other than the resistive element.

The new comparators also have about 2,500 times greater dynamic range than do thermal voltage converters. The 16101A measures from 10 mV root-mean-square to 3 V rms at frequencies from 100 kHz to 1 GHz; the 16102A measures from 3 to 20 V rms from 100 kHz to 10 MHz. Delivery time is about 45 days. Ballantine Laboratories Inc., P. O. Box 97, Boonton, N. J. 07005 [351]

Modular test system is easy to program

The 8600 GPIB Signal Director interfaces the IEEE-488 bus via its own internal communications bus with a group of plug-in modules to create systems capable of testing everything from chips to circuit boards.

Essentially a mainframe equipped with a power supply, the 8600 needs only one GPIB address and one simple programming convention to be in business. It is priced at \$1,295.

The 8601 System Timing Module (\$645) can be programmed to produce pulses from given inputs after delays of 2 μ s on up to 23 hours. Its internal clock reads out the time of day when an event occurs and can produce pulses at preselected times.

The 8603 Trigger Module (\$445) triggers one of its internal trigger lines when a preset signal occurs at its analog input channel. Three TTL inputs permit external information, such as limit switch changes, to be accessed and incorporated into a test routine.

The 8604 Programmable Voltage Source (\$745) is self-calibrating. Its two channels each have a ± 10 -V

Electronics / September 13, 1979

WE CALL IT BECKMAN'S INTELLIGENT DISPLAY SYSTEM

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That's visibly bright and microcomputer smart!

In fact, it's more than two times brighter than comparable gas discharge display systems. Beckman's SM-810-001 alphanumeric display system is the apex of the five-year development of the Screened Image technology. That's what makes it so bright. And, makes it flexible enough that you can do your own customizing. The microcomputer gives it the control and versatility that only a microcomputer can.

The SM-810-001 will give you 40 — count 'em 40 — high brightness characters in a 5 by 7 matrix of large, uniformly illuminated dots. Each of the quarter-inch characters provides a minimum of 100 footlamberts of brightness. Think what 40 of them will do for the overall illumination. In addition, the unit offers a remarkable viewing angle (for a subsystem) of 130°, plus a flicker-free 94 Hertz refresh rate. And, it's all in one compact,

microcomputer-controlled assembly . . . smaller than a carton of cigarettes.

The SM-810-001 is currently being evaluated by several major users. Obvious applications include: medical/scientific instrumentation, process control and point-of-sale. More importantly, the almost limitless flexibility of the Screened Image concept makes it possible to adapt this display system to your system . . . without the usual, high engineering design and development charges.

Significant Features of the SM-810-001

- High Viewability.
 - High Brightness & Wide Viewing Angle.
- Versatile, Microcomputer Control.
 - Direct User Access.
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 - Expanded ASCII — 98 Character Set.
- Compact, self-contained assembly.
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 - Single, 5 Volt Supply.
 - 8 Bit Parallel Bidirectional Bus.

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SM-810-001 JOINS THE SA-252.



If you prefer a larger character, 14-segment display, you may also wish to investigate Beckman's SA-252 Alphanumeric Display System. Its 16 characters are each 0.55" high, and provide excellent viewability, even at long distances. The SA-252 is also microcomputer controlled, with direct user access. And, it's ideal for biomedical, process control and general electronics applications.

BECKMAN

When Quality Counts!



Anritsu's Standard Signal Generator MG439A

The standard signal generator is one of the most basic test instruments on any radio technician's workbench and one of the most important. The new Anritsu MG439A reflects the latest thinking about how a reliable test instrument should work. It is designed for the manufacturer or maintenance facility that deals with AM and SSB receivers on a day in day out basis. This is the signal generator to consider when only the best will do. Special consideration has been given to easy operation, high stability, high output and superb signal purity. What kind of specifications are we talking about? Consider the following:

- Frequency range 50kHz to 50MHz in 9 bands, 7 digits
- Stability $\leq 30\text{Hz}/30\text{ min. at } 50\text{MHz}$
- SSB AM noise $\leq -130\text{dBc}/\text{Hz}, 1\text{kHz offset}$
- Output level -24 to $132\text{dB}\mu$, and -137 to $+19\text{dBm}$ at 50Ω
 -24 to $132\text{dB}\mu$ at 75Ω
- Source impedance 50Ω and 75Ω , BNC connector
- Modulation Up to 100% AM at $130\text{dB}\mu$ output
- Internal modulation frequency 0.3, 0.4, 1, 2, 3kHz,
accuracy: $\pm 2\%$

For comprehensive literature on the
Standard Signal Generator MG439A, contact—

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• Malaysia O'Connor's (Malaysia) SDN. BHD. Tel: 51563/5 • Brazil Anritsu Eletrônica Comércio Ltda. Tel: Rio 221 6086

New products

analog output and a TTL output, and these outputs can be stepped automatically.

The 8605 Digital I/O Module (\$695) handles TTL-compatible signals over 32 digital I/O lines and has a 16-bit comparison mode. The six-channel 8606 Switch Matrix (\$775) can be preprogrammed with a variety of switching sequences.

Delivery takes 60 days.

Jaycor, P. O. Box 370, Del Mar, Calif. 92014.
Phone Tom Kurtz at (714) 453-6580 [354]

Scanner analyzes optical spectra fast

When linked to an oscilloscope or other display device, a new optical spectrum analyzer probe gives a picture of the entire spectrum from 375 to 725 nm instantaneously. Analysis and recognition of almost any sample is therefore much faster than with monochromators or filter sets.

The CE395 Spectroscan Fast Spectral Scanner measures constant, continuous light and also changing or even pulsed light in both the reflection and transmission modes. In operation, it focuses the light at its entrance slit onto a diffraction grating. The resulting spectrum is optically coupled to an array of 256 photodiodes, which are scanned electronically to yield a signal. This is then amplified, has its background noise suppressed, and is fed through a BNC connector to a scope. To optimize the display, the scanning rate is set at line frequency at the factory. A timing signal for triggering the scope is fed through a second BNC connector on the spectrum analyzer probe.

As an all-solid-state, low-cost, laboratory-grade instrument that is also simple to operate, the CE395 also has its appeal for industrial and educational uses. It is a simpler version of the CE390, which is intended for system and computerized control applications.

CE395 kits sell for \$895 to \$1,600, said to compare well with the price of a package containing a



Low-cost hard disk computers are here

11 megabytes of hard disk and 64 kilobytes of fast RAM in a Z80A computer for under \$10K. Two floppy drives, too. Naturally, it's from Cromemco.

It's a reality. In Cromemco's new Model Z-2H you get all of the above and even more. With Cromemco you get it all.

In this new Model Z-2H you get not only a large-storage Winchester hard disk drive but also two floppy disk drives. In the hard disk drive you get unprecedented storage capacity at this price—11 megabytes unformatted.

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You get expandability, too. The high-speed RAM can be expanded to 512 kilobytes if you wish.

And the computer has a full 12-slot card cage you can use for additional RAM and interface cards.

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With the Z-2H you also get the broadest software support in the

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- Z80 Macro Assembler
- Word Processing System
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With all its features the new Z-2H, including its hard disk drive, is still housed in just one small cabinet.



Hard disk drive at lower left can be interchanged just by sliding out and disconnecting plug. Seven free card slots are available. Z-2H includes printer interface card.

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With its high performance and low price you KNOW this new Z-2H is going to be a smash. Look into it right now. Contact your Cromemco computer store and get our sales literature. Find out when you can see it. Many dealers will be showing the Z-2H soon—and you'll want to be there when they do.

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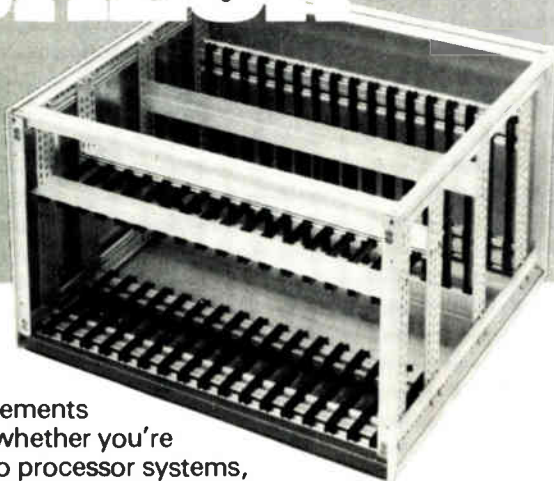
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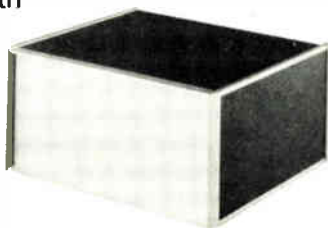
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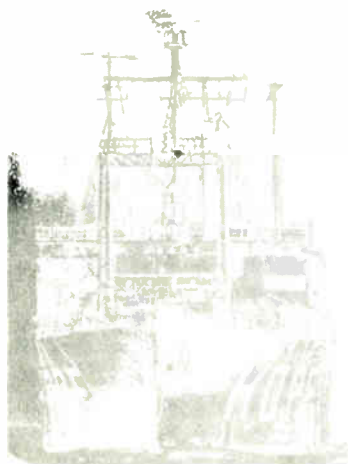
For more information on Horizon, the cabinet that lets you create the electronic package to fit your design requirements, send for our 4-page brochure. Write: Bud Industries, Inc., 4605 East 355th Street, Willoughby, Ohio 44094, or Bud West, Inc., 3838 North 36th Avenue, Phoenix, Arizona 85019.



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New products

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Spectron Instruments Corp., Dept. S, 1342 West Cedar Ave., Denver, Colo. 80223. Phone (303) 744-7088 [355]

Meter tracks trends, responds digitally

The Helmeter is as sensitive to a changing input as a d'Arsonval meter yet reads it out on a light-emitting-diode display with the accuracy and reliability of a digital meter. It can be retrofitted in place of any standard 3½-in. analog panel meter.

"You get more information from one glance at the Helmeter than from any other meter now available," says Donald F. Wilhelm, president of Helm Instrument Co. The instrument shows the rate and magnitude of input changes with a 1% maximum reading error. Its LED display has a range of 0% to 150% and automatic bipolarity with full-scale reading. The analog input configuration is bipolar true zero, with an impedance of 500 kΩ. The voltage range is 50 mv to 10 v dc, with special ranges available upon request.

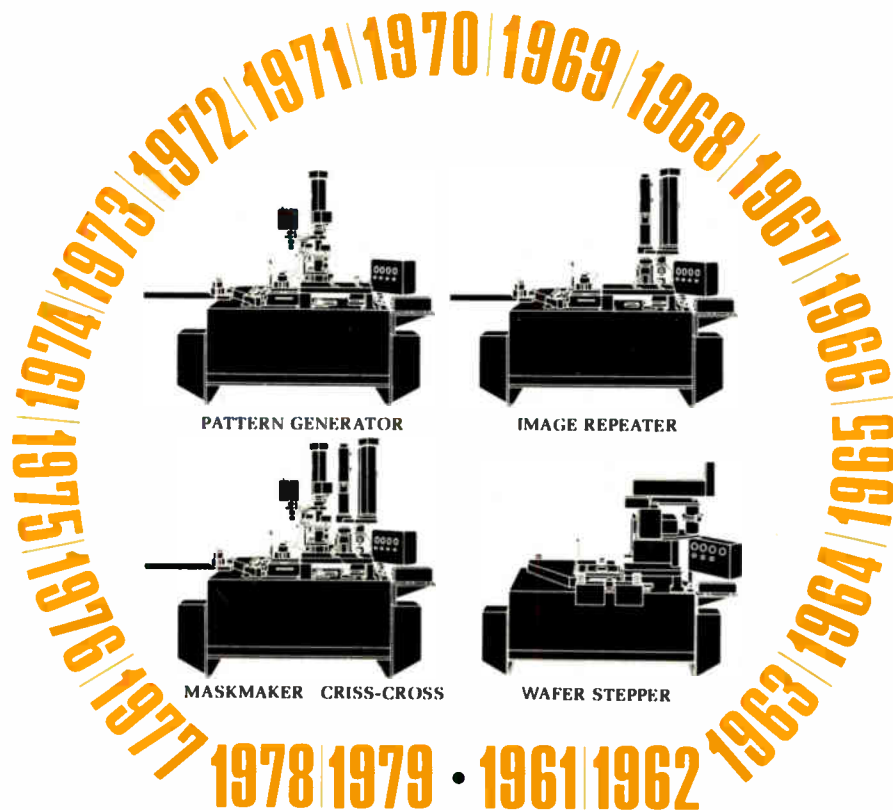
Helm originally developed the meter to improve the readings of the highly sensitive electronic load monitors it manufactures for metalworking presses. But the device should also be useful in instrumentation, communications, automotive, aircraft, and marine applications, industrial controls, and military and consumer products. The company is applying for a patent on the new instrument.

The meter has a vibration-tested steel and aluminum case and weighs 8 oz. Its operating temperature range is 0° to 60°C, and neither atmospheric pressure nor magnetic fields affect it.

A single Helmeter sells for \$150; delivery takes one to two weeks.

Helm Instrument Co.; 4511 South Ave., Toledo, Ohio 43615. Phone (419) 531-0146 [356]

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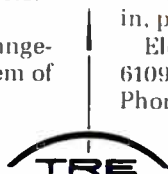
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During the past year we "enlightened" the industry with better ways to use alphanumeric, new approaches to panel design and how to get bigger, brighter digits in less space. And that's just the beginning. You'll soon see the result of constant research and development as we announce a number of creative new products in the months to come. As the "oldtimer-newcomer" in optoelectronics, we'll continue to design, produce and improve the products that best fill your design needs. That's a promise.

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Since 1962 Bavaria's GNP growth rate has been above the federal average. Productivity in industry increased by approx. 50 per cent between 1970 and 1978. Bavaria is a leading location for West Germany's electronics and electrical engineering industry and the principal center of the country's aerospace industry.

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176 Circle 176 on reader service card

New products

Semiconductors

**DTMF chip set
uses little power**

Dual bandpass filter and
tone decoder draw
only 2.2 mA at 5 V

Receivers for dual-tone multifrequency (DTMF, or Touch-Tone) signaling have gone from hybrid to monolithic form, but even those that use the latest switched-capacitor filtering techniques can draw considerable power. Now a two-chip set from Mitel Semiconductor Inc. is available that dissipates so little power that it can be operated right off the phone line.

Both chips from the Mitel Corp. subsidiary—the MT8860 tone decoder and the MT8865 bandsplit filter—are built with complementary-MOS logic. The 8865 separates the low and high bands of the multifrequency tones, while the 8860 discriminates between tones in each of the bands and decodes the tones into 4-bit binary outputs.

The 8860 is actually an improved version of an earlier Mitel decoder chip, the MT8820A, which was housed in a 24-pin package and did not offer the on-chip reset, delayed data strobe, and microprocessor-bus-compatible outputs of the 18-pin 8860. The 8860 also uses Mitel's Iso-C-MOS, a polysilicon-gate C-MOS process that is more reliable than the metal-gate C-MOS in the 8820.

The 8865, which works with either of Mitel's back-end decoder parts, is the first device to use the company's new Iso²-C-MOS, a double-polysilicon C-MOS process. The 8865 is a dual bandpass filter (not just a band splitter) so that it not only separates high and low bands, but performs dial-tone and 60-Hz rejection at the same time. Before the device was available, an analog front-end bandsplit network was needed; now the 8865 uses switched-capacitor analog techniques to do the job.

The Iso-C-MOS and Iso²-C-MOS processes also allow low-voltage operation—both parts are rated at 5–12 v. But Mitel has achieved its low power—typically 2.2 mA at 5 v, or 11 mW—by using a minimum of the switched capacitor filters. “The filters are good, but even though they are built with C-MOS, each filter uses an operational amplifier that requires dc bias current when in operation,” explains Christopher J. Bailey, director of marketing and applications engineering. “Our tone decoding is done digitally by period averaging,” he adds. The only single-chip DTMF receiver on the market, the SSI201 from Silicon Systems Inc., Irvine, Calif. [*Electronics*, Feb. 15, 1979, p. 105], uses all switched-capacitor filters and typically draws 29 mA from a 20-v supply. Worst-case, it pulls 1 w.

While not all DTMF receiving applications require low power, Bailey says there are new in-phone applications, such as remote signaling by Touch-Tone keyboards, that will have a place in industrial control. Thousand-piece prices for the 8860 and 8865 are \$11.80 and \$17.12 each. Both are available now. Mitel Semiconductor Inc., P. O. Box 13089 Kanata, Ottawa, Ontario, Canada K2K 1X3 [411]

**Display generator chip has
384 available characters**

The 2670 Display Character and Graphics Generator (DCGG), a mask-programmable 11,648-bit device, provides a 10-by-9-element matrix in a 16-by-10-element field for 128 characters. To expand the number of distinct patterns available, the circuit's 8-bit character code can also be translated into 256 additional possible graphic patterns for a total of 384 characters.

Other features include character and line-address latches, 15 optional special characters for forms applications, an internal shifting capability that lowers the matrix to provide descenders for such characters as j, y and g, and selective blanking of data

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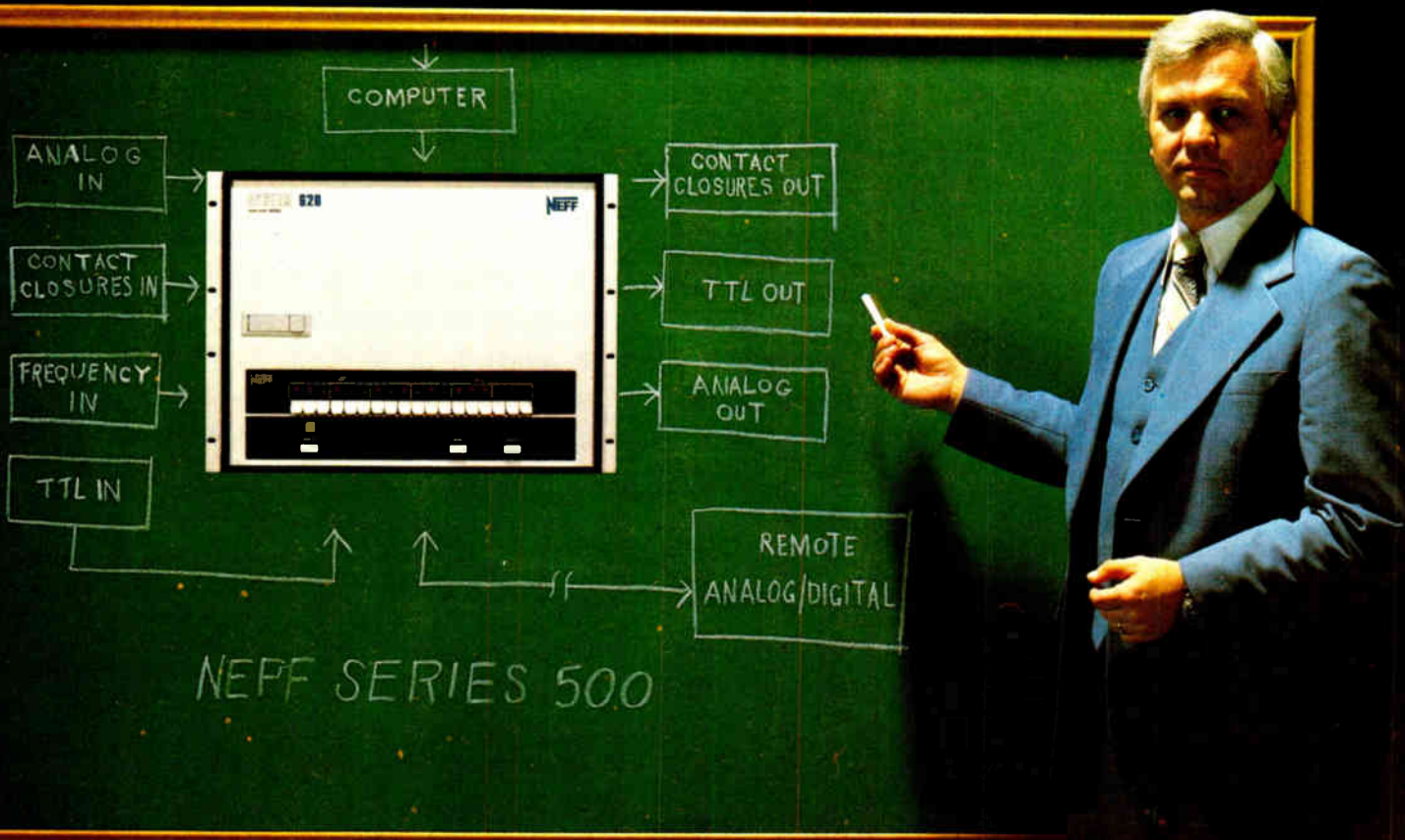
Expandability All systems are expandable at both local and remote sites.

Analog Input The Series 500 supports operation of the Neff high-performance analog input subsystems - the most powerful and versatile in the world.

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Telex: 06-961437

178 Circle 116 on reader service card

New products

output for ASCII control characters. For special applications, one or more of the character output bits can be used as control signals to initiate logic for half-dot shifting and color selection.

Specifications include a 300-ns maximum character access time, +5-v operation, TTL-compatible input and output, and static operation. Users can specify their custom version of the 2670 by supplying the manufacturer with standard 80-column tab cards describing data to be stored.

The 2670 is the first in a series of devices aimed at simplifying the hardware design of microcomputer-based cathode-ray-tube terminals. To be introduced later this year are a programmable keyboard and communications controller, a programmable video controller, and a video and attributes controller.

The standard version of the 2670 DCGG is priced at \$6.90 in quantities of 100.

Signetics Corp., 811 East Arques Ave., P. O. Box 9052, Sunnyvale, Calif. 94086. Phone (408) 746-1680 [413]

8-by-80-bit static shift register is 8 bits wide

A low-power 8-by-80-bit static shift register has been designed for use in cathode-ray-tube terminals, especially computer display peripherals. When used with a DP8350 CRT controller, the MM5034 can be applied to CRTs that require heavy use of memory to update screen information. It can replace two quad shift registers to lower component count on boards.

Fabricated using n-channel low-threshold enhancement-mode and ion-implanted depletion-mode MOS structures, the MM5034 requires only a single 5-v power supply. The shift register is available in a 22-pin dual in-line package. All inputs and outputs are TTL-compatible, and the chip has recirculation logic, internal clocks, and three-state output buffers on board. A 20-pin version—the MM5035—is also available for use with simple data-in/data-out opera-



Now Gould offers a range of digital storage oscilloscopes that offer a world of advantages over conventional tube storage technology, beginning with being able to capture transient of "one-time" events and store them indefinitely for display or hardcopy printout. This makes them ideal for electronic, electromechanical, educational, and biophysical applications.

Both the OS4000 and the new OS4100 combine the capabilities of semi-conductor memory with a bright, stable, flicker-free display. This technique allows analysis of signal build-up and decay characteristics through pre- and post-trigger viewing. Expansion of the display after storage permits detailed study of specific areas of the trace.

The new model — OS4100 — also offers

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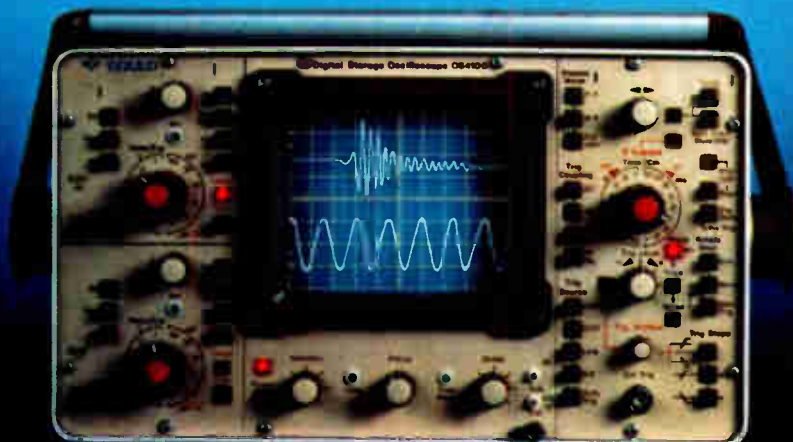
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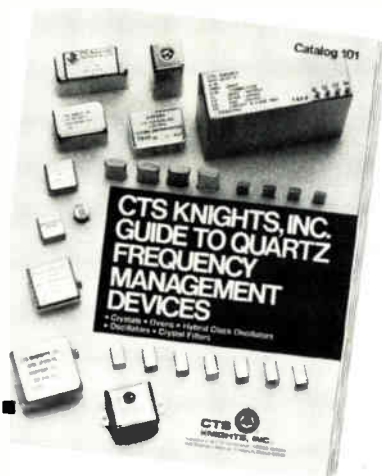
Other outstanding features include automatic operation, display of stored and real time traces simultaneously and hard copy memory output in digital or analog form. And IEEE488 is available for compatible interfacing.

And, remember that Gould scopes are backed by a two-year warranty of parts and labor, exclusive of fuses, minor maintenance and calibration. For further information, contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114. Or Call (216) 361-3315, Ext. 395, for a demonstration.

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New products

tions. The devices are identical, except that the three-state output control lines are omitted from the 20-pin model. Both versions offer high speed and feature static operation.

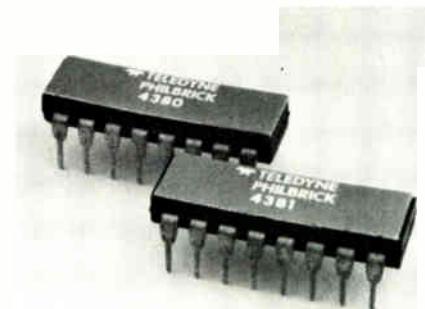
The MM5035 is priced at \$8.16 each and the MM5034 at \$8.40 each in lots of 100 to 999.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Fred Wickersham at (408) 737-5402 [414]

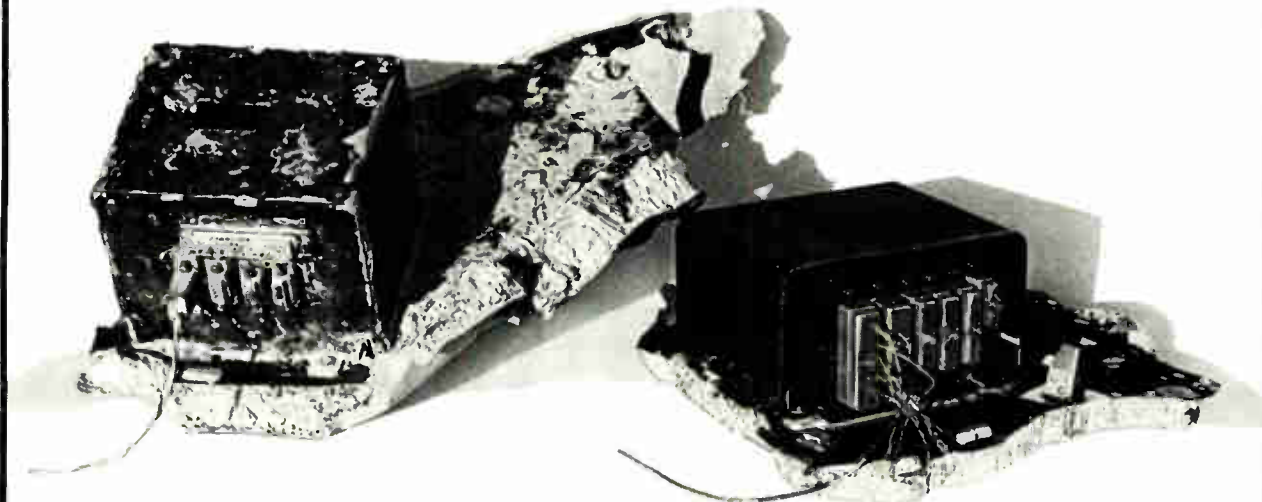
Log amplifier handles six decades of current

The 4380 is a monolithic logarithmic amplifier capable of handling six decades of current input or three decades of voltage input. Its antilog counterpart, the 4381, generates one decade of output voltage for each one-volt change at the input. The log unit is temperature-compensated from 0° to 70°C and is nominally designed to provide 1 V of output for each decade change of input. Over the top two decades of its operation, the unit has a small-signal bandwidth of 50 kHz, but this drops sharply as the current decreases and is only 100 Hz at the bottom of the range (1 nA).

Guaranteed specifications include the dynamic ranges specified above, an error of no more than 30 mV for the 4380 and 10 mV for the 4381, an untrimmed voltage offset of 25 mV for either unit, and an output voltage swing of ± 10 V for both units. For increased flexibility, the scale factor and reference current as well as the offset voltage are externally adjust-



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Over a month later, the corroded remains of the satellite were recovered, and returned to their manufacturers. The above photograph shows the Instrumentation Electronics and Squib Driver units as received back at BTM, where they were connected, unopened, to their checkout equipment and subjected to full electrical acceptance tests. They passed. 100 %.

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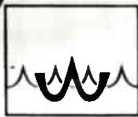
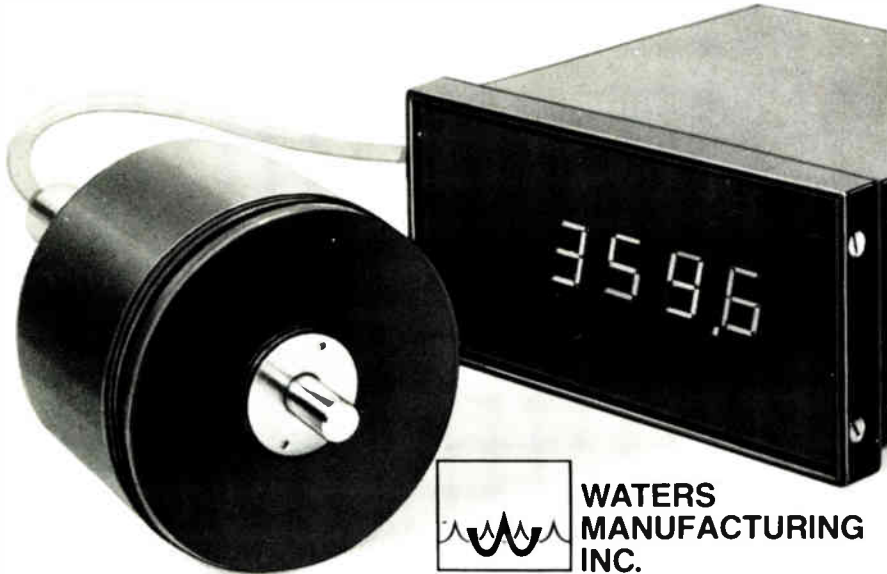
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Circle 182 on reader service card

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able. The 4380 and 4381 are housed in 16-pin plastic dual in-line packages. Both units are available from stock at \$37.50 each in quantities of one to nine.

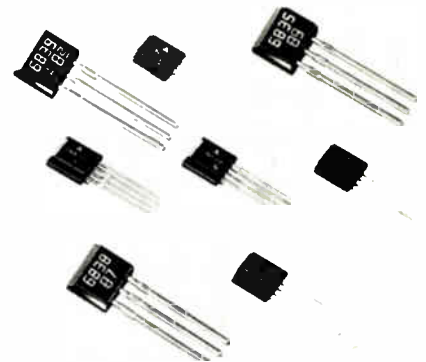
Teledyne Philbrick, Division of Teledyne Inc., Allied Dr. at Rt. 128, Dedham, Mass. 02026. Phone Wah Fea Ng at (617) 329-1600 [415]

Hall-effect devices provide 10 mA to drive TTL and MOS

For use in switching and detection applications, a family of three- and four-lead linear and switching Hall-effect devices has single or differential outputs. Three three-lead units each have a single output, while five four-lead devices have two complementary outputs. Both types include switching and linear models. In addition to the basic Hall device, both types have full capability to drive diode-transistor logic, TTL, and MOS circuitry directly, and the linear model provides outputs of up to 10 mA. The switching units operate on a supply voltage between 4.5 and 16 v dc, while the linear integrated circuits operate on 5 v dc.

The devices have various magnetic ranges. For example, a three-lead switching device with a single output (model 6839) has a magnetic flux density of 750 gauss maximum from output high to low and 100 gauss minimum from low to high. Another, a four-lead linear device with differential output (model 835), has a magnetic flux density offset of -350 gauss minimum, or +350 gauss maximum.

The switching units will be useful in keyboard switches, microswitches,



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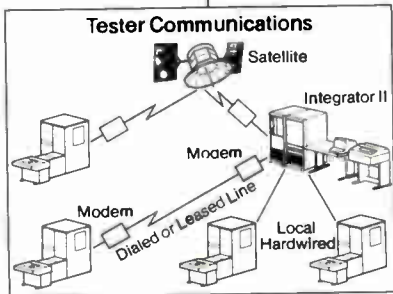
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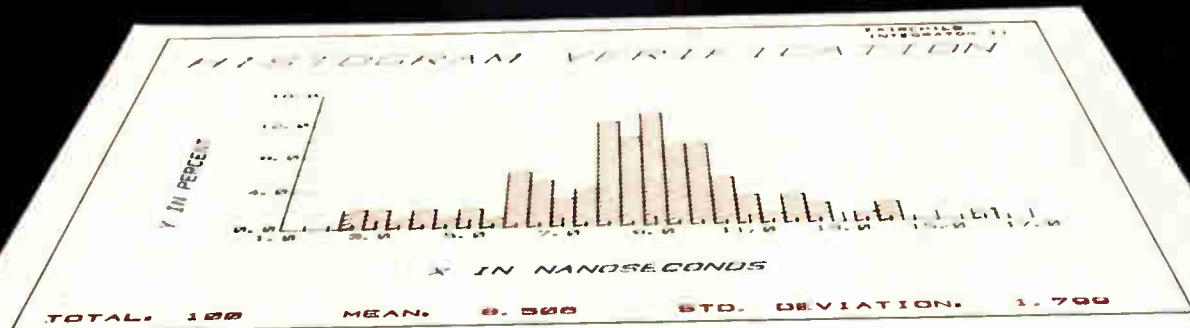
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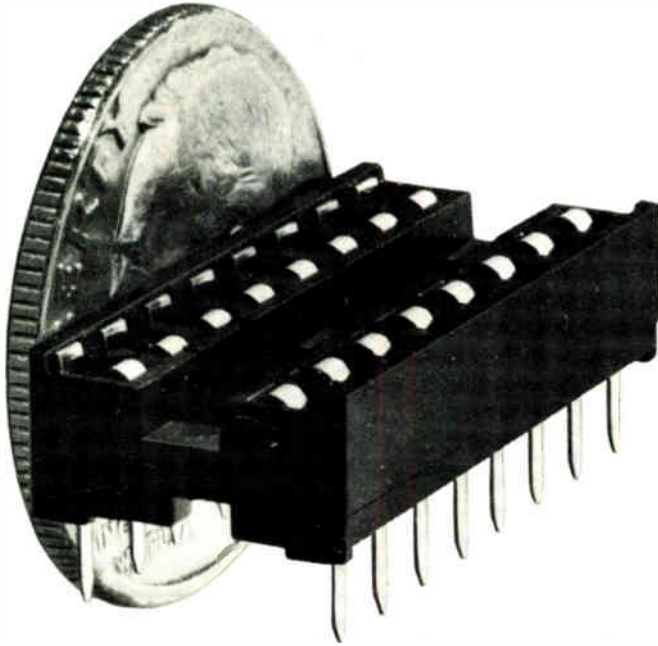
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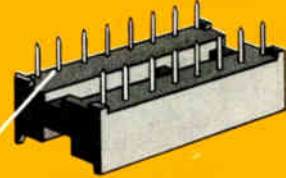
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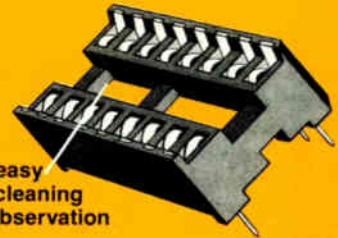
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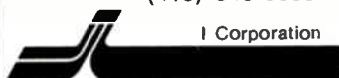
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The instrument consists of an electronics package with displays and controls plus a remote optical probe. Probes are available in three standard wafer sizes—3, 3.25, and 4 in.—and each contains nine sensors, one in the center and eight near the periphery.

When the model 310 is being

used, its probe is positioned so that the nine sensors lie in the plane of the wafer surface. The ultraviolet source is then adjusted so that its intensity (in mW/cm^2) at the center of the probe is at the desired level. This intensity serves as the reference level for deviation measurements.

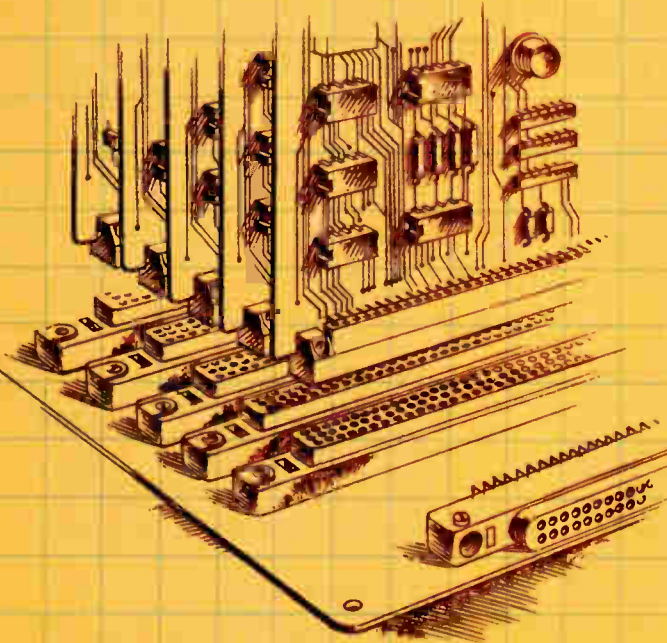
The profiler measures the UV intensity at each of the eight peripheral sensors and compares them with the intensity at the center sensor. To ease the job of adjusting the light distribution, the percentage deviations, including sign, are presented simultaneously on eight two-digit light-emitting-diode displays that read from -99% to $+99\%$.

A channel-selector switch allows the user to determine the absolute intensity at any of the nine sensor points on the optical probe. This intensity is shown on a three-digit display and may range from 0.1 to $99.9 \text{ mW}/\text{cm}^2$. As shown in the photograph, the channel number is displayed alongside the reading.

According to Optical Associates president George Lee, users of the new instrument will be able to check the uniformity of light intensity across a wafer in less than a third of the time required by previous methods. Furthermore, he claims, they will be able to do so with greater accuracy. The model 310 has an



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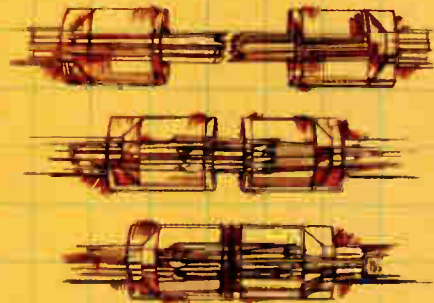
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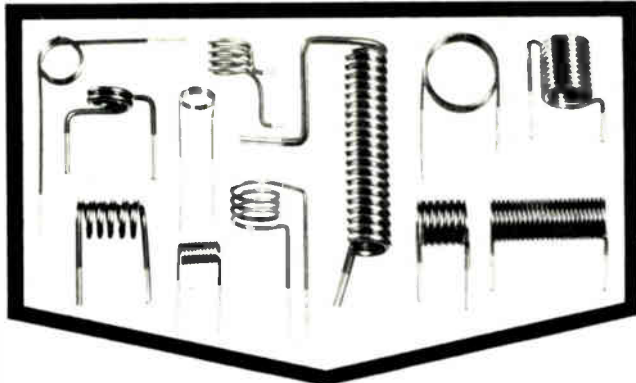


For full information, call (607) 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

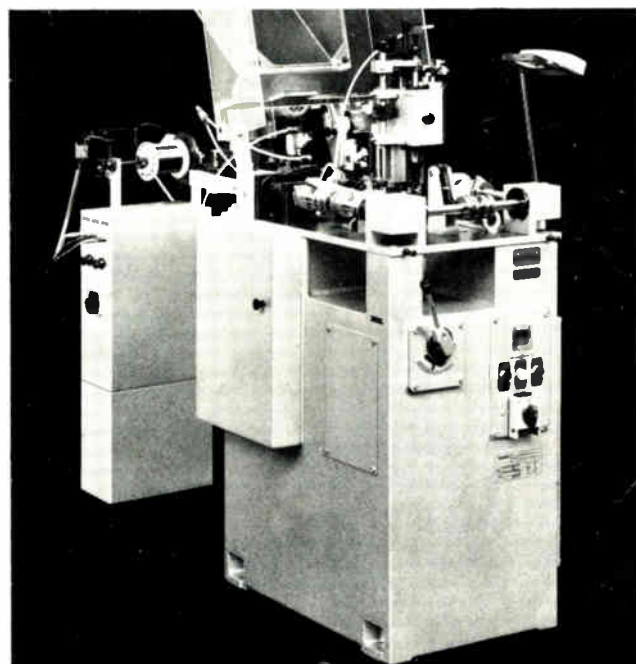


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Optical Associates Inc., 3300 Edward Ave., Santa Clara, Calif. 95050. Phone George Lee at (408) 988-6900 [391]

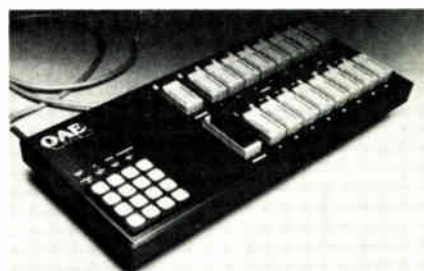
Unit tests and duplicates

16 E-PROMs simultaneously

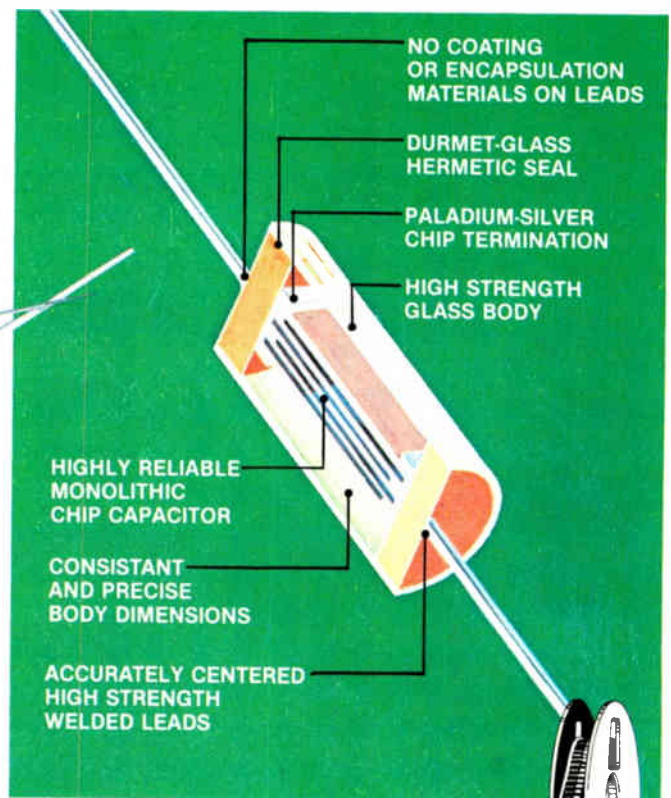
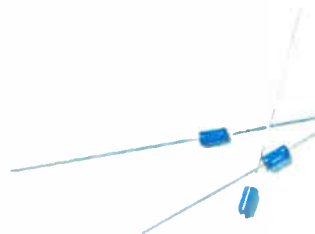
A tester and duplicator that evaluates erasable programmable read-only memories both before and after programming will be exhibited at this month's Wescon show. The UPP-2700 also detects incorrectly inserted or static-damaged E-PROMs as they are being loaded into the programmer.

When the user presses a single key, the internal 6-MHz 8048 microprocessor tests, blank-checks, programs, verifies, and retests 16 individual 2708 E-PROMs in less than 130 s. A satellite tester/duplicator allows up to 32 devices to be tested and duplicated simultaneously. If there are any incorrectly inserted devices or test failures, a solid-state audio beeper alerts the user.

A 40-pin personality module contains the programming and test algorithms for a complete generic E-PROM family. Currently there are six personality modules available to be used with the following devices: 2704, 2708, 27L08, TMS2716, I2758, I2716, TMS2516, TMS2532,



It's no coincidence that Murata-Georgia's new glass-encapsu- lated monolithic ceramic capacitors can't be beat for automatic insertion



Automatic insertion equipment puts stringent demands on component dimensional consistency, stability and reliability. To meet these demands, Murata-Georgia now offers highly reliable monolithic chip capacitors encapsulated in a leaded, hermetically sealed glass envelope with mechanical performances second to none in the industry. What's more, these new capacitors offer overall electrical performance that simply can't be beat.

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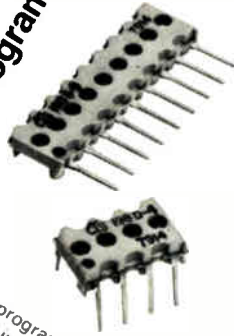
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New products

I2732, and the soon-to-be-announced MCM68764.

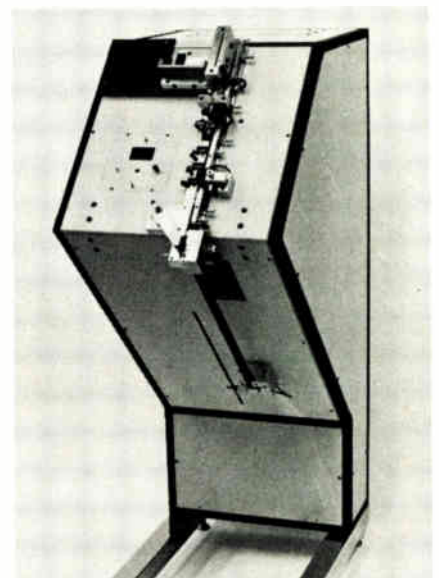
A complete system, with one personality module, sells for less than \$2,500. The optional satellite tester/duplicator has a price of under \$2,000.

Oliver Advanced Engineering Inc., 676 West Wilson Ave., Glendale, Calif. 91203. Phone (213) 240-0080 [394]

Machine separates, tests, and loads ceramic substrates

Designed to separate, test, and load ceramic substrates, the STL (for Singulator/Tester/Loader) automatically processes thin- or thick-film laser-scribed ceramic plates.

When operating, the intake hopper of the machine accepts several ceramic substrate plates—each measuring up to 4 by 4 in.—that have been screened, scribed, and solder-pasted, if required. The machine then snaps the plates into individual substrates as small as 0.125 by 0.250 in. It tests them electrically for continuity and/or tests them optically for rejection marks or missing chips. After rejecting defective parts, the STL loads tested and oriented parts into magazines. Depending on testing requirements and percentage yield, the machine can cycle up to 4,000 units per hour. The machine



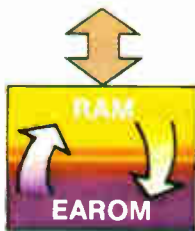
The RAM with the non-volatile memory.



GI offers the advantages of RAM and EAROM in a single chip.

Now there's a RAM that retains its data in a power-down situation without the need for a backup battery. The mating of a RAM with an EAROM in a single low-cost chip — the ER1711 — has created a whole new world of design possibilities.

In normal operation, the ER1711 is a 256 x 4-bit static RAM with a fast 900ns read or write time. At power on/power off/power fail occurrences, single pulse programming controls the data flow to and from the RAM and EAROM cells.

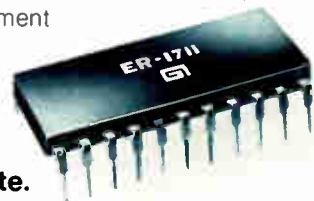


Data can be stored and recalled in the EAROM cells up to 10⁴ times.

With fast read and write times coupled with a non-volatile memory, the ER1711 opens new application options. Examples: business machines and instruments where constantly changing data must be retained in a power off status; and any microprocessor based system where a portion of the memory must be retained to insure its operating functions.

If you have specific application questions, or would like complete specifications on the ER1711 RAM/EAROM write or call General Instrument

Microelectronics,
600 West John Street,
Hicksville, N.Y. 11802,
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New products

also provides a built-in diagnostic system for sequence interrupts.

Shelf-type magazine-loading systems are available for thin-film devices and hybrids, whereas tube-type systems are offered for thick-film units. The price of the STL will vary according to the test mode options selected and the magazine-loading system required. Base price for the machine is \$24,000, with delivery time in 12 to 14 weeks.

MTI Corp., 55 Industrial Ave., Ivyland, Pa. 18974. Phone Jacques Werth at (215) 355-3110 [395]

Linear scale has two 10× optics for close-up work

Eliminating the parallax error in a wide range of linear scaling and precision measurements, the Opto-Scale, a precision glass measuring instrument, combines many useful features. The unit has two removable, full-focusing 10× optics, each offering a two-group achromatic, 35-mm lens system to provide a sharp, 1-in. (25.4-mm) field of view.

Other features the Opto-Scale sports include: a dual-precision-aligned, 0.005-in. and 0.1-mm inch/metric-scale pattern, with chrome etching on the bottom of the scale to eliminate errors due to parallax; full 24-in./610-mm measuring capability with overall accuracy of ±0.0005 in., or 0.013 mm; a sturdy, aluminum frame with easily gripped handles; and a thick, stable-based glass plate that is practically impervious to normal fluctuations



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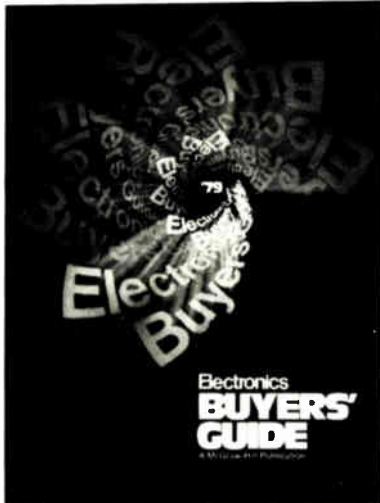
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A complete Opto-Scale package, with a protective lens cap for each optic and a lens cleaning cloth, sells for \$395.

Bishop Graphics Inc., 5388 Sterling Center Dr., P. O. Box 5007, Westlake Village, Calif. 91359. Phone Allen Ferrin at (213) 991-2600 [396]

Stacking connector uses thin wires to join pc boards

Providing electrical connections between printed-circuit boards mounted in mother-daughter fashion, the Conmet stacking connector is now available. The connector element consists of very fine wires—0.003 in. in diameter—that are vertically suspended and equally spaced in a single row in solid silicone rubber; the contacting wire tips are left exposed. This connector is secured in a plastic holder slot to assure correct alignment of pc board contacts.

Good electrical contact and environmental sealing are achieved by mounting the connector between two pc boards. The high wire density in the Conmet component allows interconnection of any contact arrangement on a board which has a least 0.025-in.-wide pads and 0.010-in. spaces—0.035 in. center to center, or 28 contacts per inch.

The plastic holder for the connector is designed to be used with 0.062-in.-thick pc boards; it is available in 0.025-in.- and 0.325-in.-high models, and measures 0.438 in. wide by 2.5 in. long.

The connector is available from stock and is priced at 16¢ each in quantities of 10,000.

Technical Wire Products Inc., 129 Dermody St., Cranford, N. J. 07016. Phone (201) 272-5500 [397]

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Elec-Trol now offers its Blue Boy Reed Relays in both an instrument and a commercial grade. The instrument grade provides low and stable contact resistance over a large number of operations, for use in such applications as ATE systems, data acquisition and telecommunications.

The new commercial-grade units have a higher contact resistance and a lower life expectancy but are well suited for applications where contact resistance is not critical, such as switching into high impedance loads, for use in such end-products as microwave ovens, water heaters, and TV's.

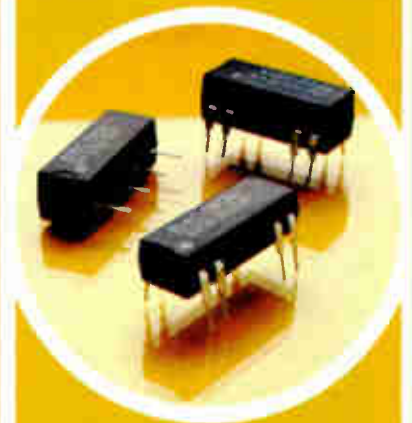
Both grades are totally encapsulated in rock-hard epoxy, and the reed switch contacts and coil are secured to a rigid internal lead frame which incorporates the PCB terminals. These little inch-long units incorporate a 1 Form A hermetically-sealed reed switch, and can switch low-levels up to 10W with 5-48 VDC coils. For prices or samples, contact your local Elec-Trol distributor.

Elec-Trol, Inc., 26477 N. Golden Valley Road, Saugus, CA 91350, (213) 788-7292 (805) 252-8330. TWX 910-336-1556.

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A Place to See

Oregon. A place of constantly changing scenes; natural paintings that seem to shift their colors and patterns so that no two days are ever quite the same. That's part of the magic of our state. Some of us came here from the technology and business communities...tired of pushing out the edges of the state-of-the-art at work, and then pushing through the traffic jams to get home. We built our own electronics community in Beaverton, Oregon: 18,000 people contributing to the research, development, and manufacture of advanced electronic instrumentation, graphic display systems, and computer peripherals. The name is Tektronix. The place is Oregon. The reason is people. Think about it. If you have any of the skills a Fortune 500 electronics manufacturer and marketer needs to maintain steady growth, contact us. Professional Staffing, TEKTRONIX, INC., P.O. Box 500, 8-E, Beaverton, Oregon 97077.

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New products

Microcomputers & systems

Zilog seeks business market

Z80 computers get Cobol, communications, and text-formatting packages

For this year's Wescon, Zilog Inc. is introducing three products designed to extend the range of applications for its Z80-based microcomputer systems in business and other database markets. The biggest package adapts the MCZ microprocessor system so that interactive Cobol programs interact with up to five terminals, explains Paul Reilly, software product marketing manager.

This multiterminal Cobol capability extends MCZ power in such areas as business, reservations, inventory control, data entry, real estate, and other uses. And it clearly is a response to the need for software programs to work in multiterminal or distributed processing environments, Reilly says.

With the multiterminal Cobol package, two hardware products are offered: the MCZ-1/50, a version of the desktop MCZ-1/20 microcomputer system, but packaged with dual floppy disks; and the MCZ-1/70, a rack-mounted model. Both units contain a Z80 microcomputer board and a memory disk controller. Field-upgradable options are a serial input/output board with four additional ports to handle the multiterminal Cobol, a hard-disk controller set, and an additional dual floppy-disk unit.

The second new product is Asynch, an asynchronous communications package that will let users of either MCZ or microcomputer development systems use telephone lines to transfer data to a centralized computer. Designed for small-business users, it aids in fast turnaround times because programs can be created at work stations, and when complete, can be forwarded to a

centrally located computer, Reilly points out.

The Asynch package, which runs on Zilog's RIO Standard MCZ operating system, also comes in two parts: a RIO hardware driver and an asynchronous protocol terminal emulator. The driver allows users to write programs that communicate with other computers and operates either in an MCZ system over an asynchronous serial port provided by a serial interface board or in a development system by means of an auxiliary serial and parallel I/O board. The emulator, using the driver as an interface, permits the user to transfer source-code files in high-level language between a disk and an external system or to transfer data from an outside system to a printer.

The third new product is a text-formatting package that enables users to compose letter-quality documents in business, office, or engineering applications. The package contains software for text formatting, including pagination and tabulation, indentation and page headings, as well as footings, text centering, and justification.

Preliminary prices for the microcomputer systems, including a CRT, are: \$10,200 for the MCZ-1/50 and \$7,700 for the rack-mounted MCZ-1/70. The optional serial I/O board for the multiterminal Cobol package is \$595. The Cobol software is priced at \$1,450. The price for the Asynch package is \$500, while for the text-formatting package, including letter-quality printer and printer interface, it is \$6,175.

Zilog Inc., 10341 Bubb Rd., Cupertino, Calif. 95014. Phone (408) 446-4666 [371]

CP/M developed for the STD bus

The STD BUS microcomputer card system, a modular backplane interconnect scheme for microcomputers recently developed by Pro-Log and Mostek, will probably become even more popular now that the CP/M disk operating system has become available for it.

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In addition to an 8-in. diskette containing the CP/M system, the Micro/sys package contains two STD bus cards compatible with both the 8085 and Z80 microprocessors. They are the SB8500 floppy-disk controller, which controls up to four floppy-disk drives from a single STD bus slot, and the SB8420 dual serial interface, which provides communication with a console device.

CP/M provides a set of tools for system development. In addition to disk-file management, it incorporates a text editor, an 8080 assembler, a dynamic debugger, and various utilities. The Micro/sys CP/M package is priced at \$695.00. Delivery time is one to four weeks.

Micro/sys Inc., 1353 Foothill Blvd., La Canada, Calif. 91011. Phone Ken Finster at (213) 790-7957 [373]

Full C Compiler contains over 75 functions

Producing faster code than Pascal with more extensive facilities, Whitesmiths' full C compiler has over 75 functions for performing input/output, string manipulation, and storage allocation. The compiler conforms to the UNIX version seven implementation of C, as described by Kernighan and Ritchie in the appendix of their book, "The C Programming Language."

The compiler's output is in what Whitesmiths calls A-Natural. Using an A-Natural software package that comes with Whitesmiths' C, A-Natural is easily translated into Microsoft Macro-80 assembler source code. The package also contains a narrative assembler, a librarian, an extensive 8080 subrou-

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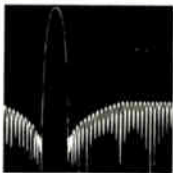
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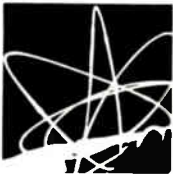
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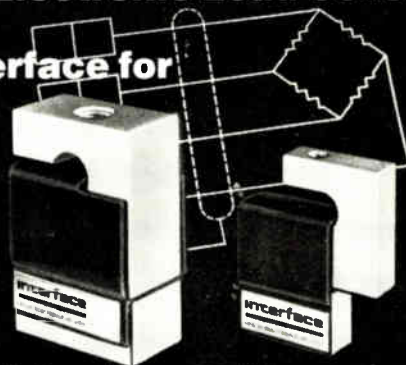


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tine library in A-Natural format, and a translator from relocatable A-Natural to Microsoft source.

Whitesmiths' C runs under CP/M + and sells for \$630 (\$30 for the manual alone). The A-Natural package is also sold separately for \$330 (\$15 for its manual).

Lifeboat Associates, 2248 Broadway, New York, N. Y. 10024. Phone (212) 580-0082 [374]

The IMB-100 utilizes one 7110 bubble-memory module

A 128-k byte bubble-memory development board utilizes one 7110 bubble memory module, an 8085A-based controller, and standard components. The IMB-100, designed to interface with Multibus systems, plugs into Intellec Series II micro-computer development systems and can be used with the ISIS-II operating system.

The IMB-100 transfers data at a rate of 68-k bits/s and operates at temperatures from 0° to 50°C. Address, data, and control signals are TTL- and Multibus-compatible. The system central processing unit communicates with the 8085A through registers on the board via input/output commands. Data is passed via a first-in, first-out register on the board, also through I/O commands. Included on a double-density diskette is a set of six programs that provide transfers of data between a RAM buffer and a standard ISIS-II device or the bubble memory.

The IMB-100 bubble-memory development board sells for \$3,900 in single quantities. Delivery time is four weeks.

Intel Magnetics, 3000 Oakmead Village Dr., Santa Clara, Calif. 95051 [376]

CP/M 2.0 and MP/M available for 8080 and Z80

Digital Research, originator of CP/M, has added to its line two new operating systems—CP/M 2.0 and

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New products

MP/M. Both are adaptable to any 8080 or Z80 computer system having back-up disk storage.

CP/M 2.0, an enhanced version of CP/M, maintains upward compatibility and operates with disk capacities ranging from simple minifloppies up through large-capacity hard-disk drives through its expanded file system. Configuration is accomplished through a definition table.

MP/M is a CP/M-compatible multiterminal operating system. It supports real-time multiprogramming, along with background and foreground modes, and serves as a program development environment or as the center for terminals or processors that are accessing a common data base. The construction of particular MP/M configurations is simplified by an interactive system generation procedure. Currently, the MP/M operates with 8080 or Z80 microprocessors, but will soon be available for the more powerful 8086.

The single-copy prices are \$150 for CP/M 2.0 and \$300 for MP/M, which includes both documentation and diskette.

Digital Research, P. O. Box 579, Pacific Grove, Calif. 93950. Phone (408) 649-3896 [375]

E-PROM programmer aims for AIM-65 computer's use

The model 6516, a simple-to-use programmer for 2716 erasable programmable read-only memories, has been developed for use with Rockwell's AIM-65 computer. The small card provides the hardware to program the 5-v 2716s, including a zero-insertion-force socket; 44-conductor female and male edge connectors interface it to the AIM-65.

The routines for programming are contained in an interactive monitor ROM. Monitor commands include program, compare, erased, fill, move, and load.

The model 6516 sells for \$149.00, fully assembled and tested.

Cubit, 897 Independence Ave., Building 4A, Mountain View, Calif. 94043. Phone Mark Nicewonger at (415) 962-8237 [377]

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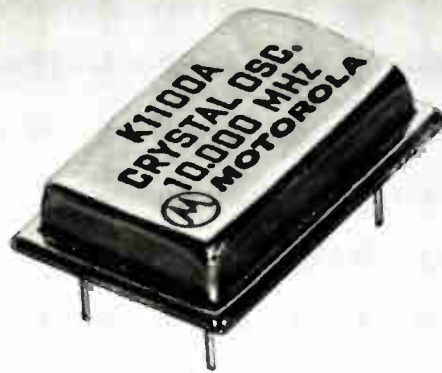
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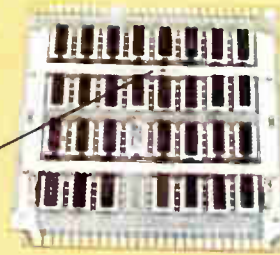
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How the smart companies

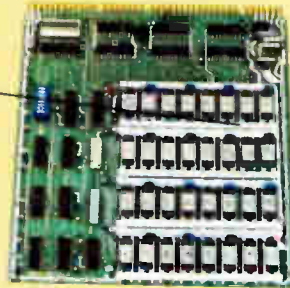
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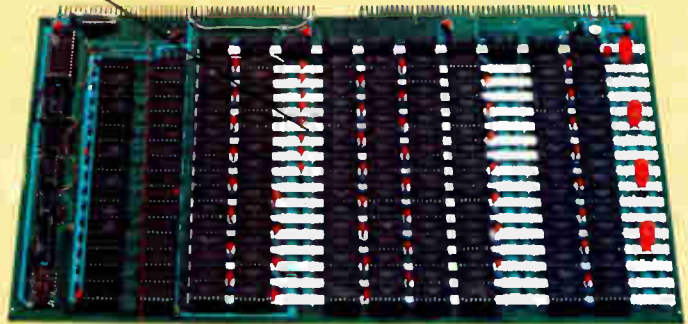
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New products

Power supplies

Quad switcher delivers 300 w

Aimed at microcomputer systems, supply is offered in four standard versions

Users of complete microcomputer systems that need four different voltage outputs have typically had to use two power supplies. However, a single 300-w switcher to be introduced by ACDC Electronics at Wescon has four outputs that can run virtually any microcomputer system, including floppy-disk systems. High reliability in the RQ Sub-modular Switcher series is achieved by incorporating LSI control circuits mounted on printed-circuit boards to form three standard modular assemblies that perform input, output, and converter functions within the supply. Instead of discrete wires, an interconnection strip joins these sub-assemblies.

The RQ switchers can also be used with minicomputers and pe-

ripherals. They are designed to meet the interference specifications of West German VDE standard 0875, as well as safety specifications established by UL 478. The 5-by-8-by-10-in. unit offers the following output voltage configurations:

| | |
|-------------|-------------|
| 5 v at 30 A | 5 v at 30 A |
| 12 v at 5 A | 12 v at 4 A |
| 12 v at 5 A | 15 v at 4 A |
| 5 v at 5 A | 5 v at 5 A |

| | |
|-------------|-------------|
| 5 v at 30 A | 5 v at 30 A |
| 12 v at 5 A | 15 v at 4 A |
| 12 v at 5 A | 15v at 4 A |
| 24 v at 4 A | 24 v at 4 A |

Input voltage is user-selectable to be 115 or 230 v ac at 47 to 63 Hz. Operating range is 90 to 132 v ac for the lower voltage, or 180 to 264 v ac for the higher. No-load to full-load regulation is 0.1% plus 5 mv at constant line voltage. Line regulation for a $\pm 10\%$ input-voltage change is 0.2% plus 5 mv. The unit has a ripple of 5 mv rms maximum, and 50 mv peak to peak maximum. Holdover storage is 30 ms minimum, but the output specifications will usually be met for 40 ms after a power-line dropout. Operating temperature is the usual 0° to 71°C, with 100% of rated output at 40°C, derating to 50% at 71°C. The RQ series



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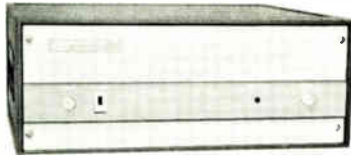
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New products

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In quantities of one to nine, the units sell for \$625.00 apiece, with delivery in eight weeks.

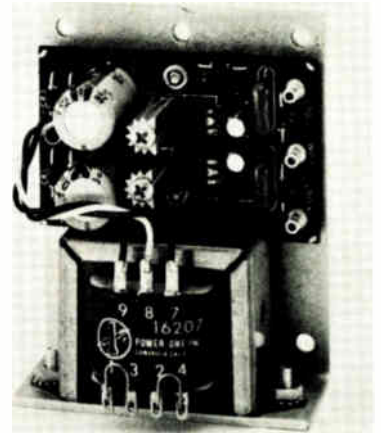
ACDC Electronics, Division of Emerson Electric Co., 401 Jones Rd., Oceanside, Calif. 92054. Call Chris Edman at (714) 757-1880 [381]

Dual-output power supplies come in potted-unit sizes

Because they are built in the same sizes as encapsulated supplies of equal power, the HAD series of dual-output open-frame supplies can be used in low-power applications where potted units are normally used. However, the operating-temperature specifications for the dc power supplies are 0° to 50°C, so they must be fan-cooled or derated to 70% at 60°C and to 40% at 71°C when they are mounted in a confined area.

The HAD12 and HAD15 measure 3.75 by 3 by 1.4 in., weigh 1 lb, and have outputs of ± 12 v at 0.25 A and ± 15 v at 0.25 A, respectively. The manufacturer says the series will power combinations of most semiconductor devices, including p-, n-, and complementary-MOS and linear devices.

The units have 115/230 v ac $\pm 10\%$ ac input capabilities, between 47 and 440 Hz. Regulation is $\pm 0.1\%$ for 10% line and 50% load changes. Maximum output ripple is 10 mv peak to peak. Efficiency with 115 v ac input and full load on output is 45% for each unit. Standard features include short-circuit and thermal overload protection. In addition, the supplies meet the shock and vibration requirements of MIL-STD-810B, and each of them also comes



with a two-year warranty.

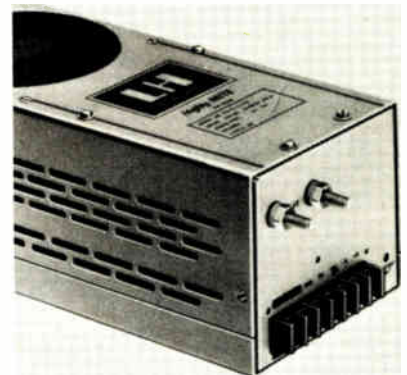
Price is \$32.95, and delivery is from stock.

Power-One Inc., Power-One Dr., Camarillo, Calif. 93010. Phone Larry Steen at (805) 484-2806 [385]

MM-11 switchers offer 375 W in a compact package

The Mighty-Mite M-11 series of 375-w single-output switching regulated power supplies weigh only 8 lb and measure approximately 4 by 5 by 12 in. The compact units are available with a choice of standard output voltages: 2 v at 75 A, 5 v at 75 A, 12 v at 31 A, 15 v at 25 A, 18 v at 21 A, 24 v at 15 A, or 28 v at 13 A.

Like other series MM units, the MM-11 is up to 80% efficient and features 1% or 50 mv peak to peak ripple and noise on its outputs. Line regulation is 0.4% over the entire input range, and load regulation is



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Circle 209 on reader service card

New products

0.4% from no load to full load. Response time after a 25% load change is 200 ms. Operating temperature is 0° to 70°C, with full rating maintained to 40°C, derating to 60% at 70°C. An integral fan is provided for cooling.

Other features include remote sense, remote on/off, power fail detection, internal thermal switch, limited inrush current, and automatic internal sensing.

The MM-11 is UL-recognized, CSA-certified, and comes with a two-year warranty. Price for one to 24 units is \$470 each, with a delivery time of four to six weeks.

LH Research Inc., 1821 Langley Ave., Irvine, Calif. 92714. Telephone (714) 546-5279 [387]

Dual-output switchers have extra-wide voltage input

SD300 dual-output 300-w switching power supplies have an extra-wide 117/234 v ac (-23% to +11%) input range. The six open- and closed-frame models come with one overvoltage-protected standard output of 5 v at 60 A, and give the user a choice of 5 v to 28 v with current ratings of up to 20 A for the second output.

Features include 20-ms loss-of-line holdup, input surge-current limiting, and suppression of differential and common-mode electromagnetic interference. All models meet UL 478. Combined line and load regulation for the main output is 0.1% for full line and load change. Ripple and noise are 50 mv peak to peak for outputs below 15 v and 100 mv p-p for outputs of 15 v or greater. All outputs are fully rated up to 50°C. Nominal efficiency is 70%. Overvoltage protection is optional for the second output.

Price is \$469 plus extra costs for overvoltage protection on the second output and for a screen cover. Deliveries are currently scheduled for approximately 11 to 12 weeks.

Deltron Inc., Wissahickon Ave., North Wales, Pa. 19454. Phone Jack Phillips at (215) 699-9261 [386]

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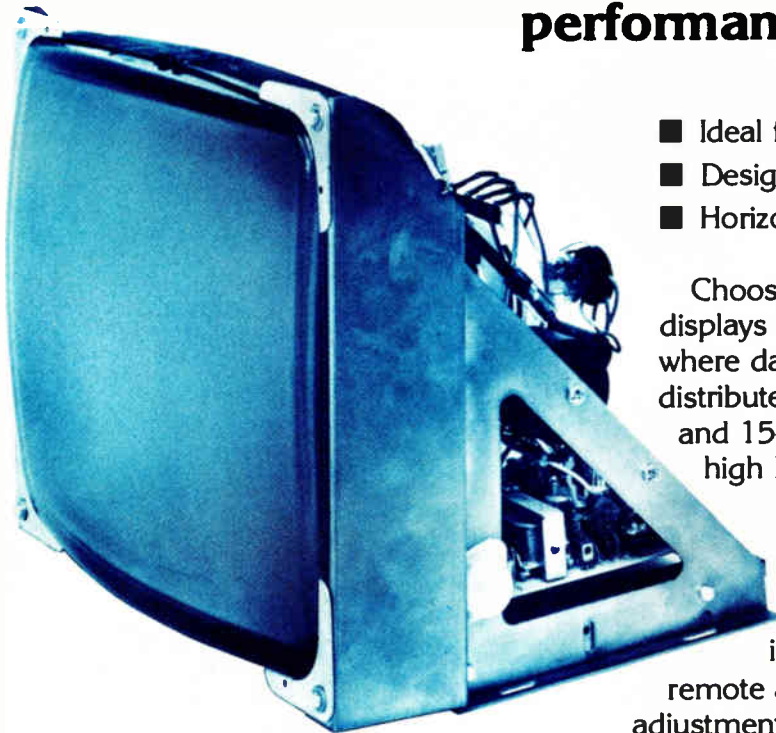
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Fluke reads 5½-digit top-end multimeter

About to burst onto the scene from John Fluke Manufacturing Co. is a microprocessor-controlled 5½-digit multimeter with a most unusual new feature—a **burst mode of operation that allows users to make and store up to 400 readings at speeds ranging from one an hour to 500 per second.** The readings stored in the model 8520A may be selectively recalled in raw form, or they may first be processed by one or more preprogrammed computational functions. The burst of readings can also be sent to a controller via the IEEE-488 bus. The full-blown 8520A will sell for less than \$3,500, while a slightly stripped-down version with fewer computational functions and capacity for storing only 50 readings will list for under \$3,000.

Datel adds data-acquisition boards

Datel Systems Inc., Manchester, Mass., is expanding its Sine-Trac series of data-acquisition boards for Intel SBC microcomputers with the addition of two models aimed at industrial applications. The ST-711RLY boards, which are offered with 8 or 16 differential input channels, **use a flying-capacitor multiplexer relay to achieve high common-mode noise rejection (126 dB) and high isolation (250 v rms).** A passive RC filter attenuates normal-mode noise. These attributes, along with full-scale ranges as low as 10 mv, make the boards well suited for acquiring typical low-level transducer signals in electrically noisy industrial environments. Prices for the 8- and 16-channel ST-711RLY models are \$650 and \$995.

Motorola heads race for single-supply 64-kilobit E-PROMs

Motorola will apparently be first out of the gate in the race to produce single-supply erasable programmable read-only memory devices at the 65,536-bit density level. **Officials at the company's Austin, Texas, integrated-circuit operation are planning a Wescon unveiling for the MCM68764, which the company says will be available in sample form in the fourth quarter, priced at \$164 in 100-piece quantities.** Housed in a 24-pin package, the 8-k-by-8-bit organized 68764 will have a specified access time of 450 ns. The device will also feature an automatic power-down standby mode that will reduce power dissipation to about 100 mW, compared with 500 mW when it is in the active mode.

TI expands memory for FS990 MDS to 64 kilobytes

The introduction of two optional expansion boards for the FS990 AMPL development system from Texas Instruments Inc. this month will allow users to do real-time emulation with as many as 64 kilobytes of memory. **Real-time emulation with these systems has previously been limited to 8 kilobytes, but the new 2263420-0001 and 0002 boards can be used to add 56 kilobytes and 8 kilobytes, respectively.** The 0001, priced at \$3,000, allows real-time emulation with the full 64 kilobytes addressable by the Dallas company's 16-bit TMS9900 microprocessor. The 0002 module, priced at \$1,000, is targeted toward prototyping the TMS9980, an 8-bit data-bus version of the 9900 limited to 16 kilobytes in total addressing capability. To use the new boards, customers with older FS990 systems (purchased before 1979) will also need a modified emulator board, costing an additional \$1,800 to \$2,400.

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The B&K-PRECISION DP-50 is the digital probe that offers more than logic. In addition to indicating logic status, this compact instrument actually displays pulse



presence to 50 MHz. The intensity of its PULSE LED reveals the duty cycle of the signal observed, up to a 10:1 ratio.

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The DP-50 is a multi-family device, compatible with popular logic types, so it simplifies analysis of any digital circuit.

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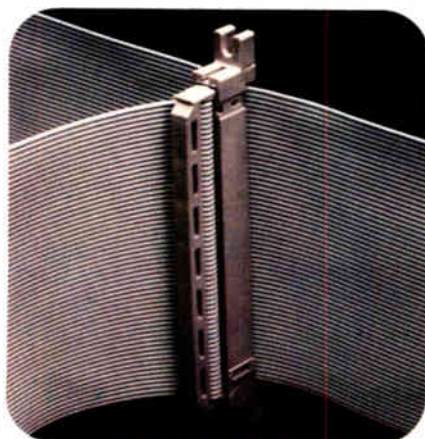
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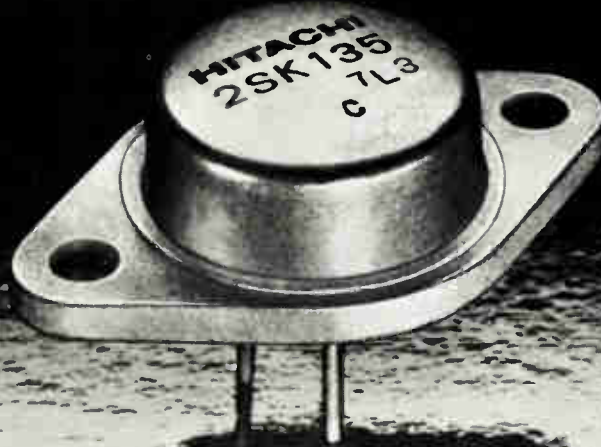
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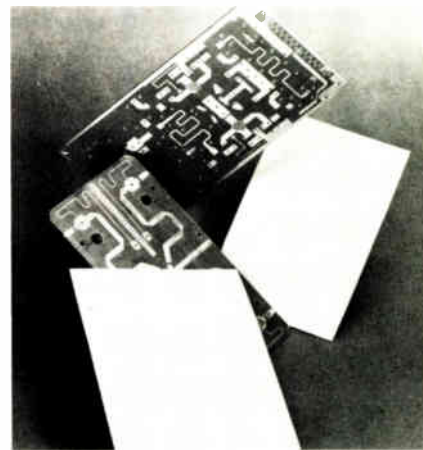
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Epoxy Technology Inc., Marketing Department, 14 Fortune Dr., P. O. Box 567, Billerica, Mass. 01821 [478]

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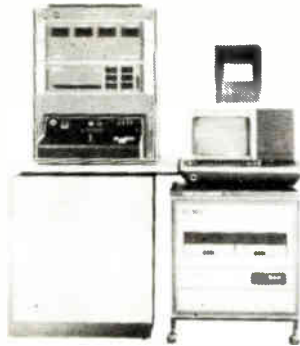
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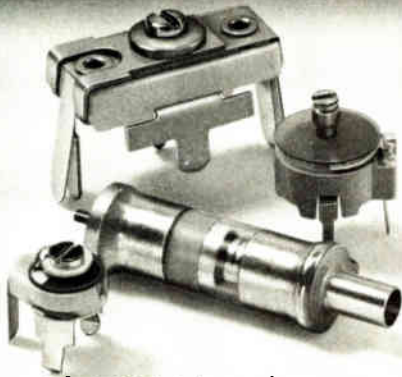
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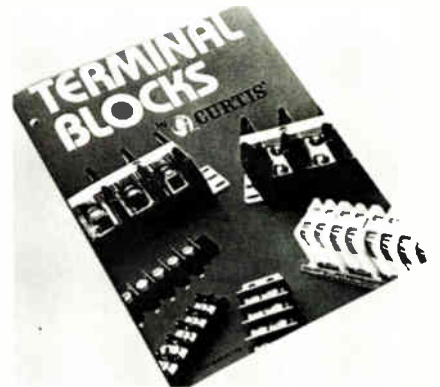
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New literature

Glass-to-metal seals. Designs and application information for glass-to-metal and ceramic-to-metal seals used in electronic and solid-state devices, such as relay headers, dual in-line and TO packages, and sight glasses, are provided in a six-page technical report, "Glass-To-Metal Seals—What You Need to Know." Airpax, Woods Road, Cambridge, Md. 21612. Circle reader service number 421.

Terminals. "Terminal Blocks" describes the design features of each series of Curtis terminal blocks—including insulated feedthrough, special-purpose, snap-in track-type, miniature, modular, and multilevel blocks, and circuit breakers. Also listed for each series are terminal variations, engineering specifica-

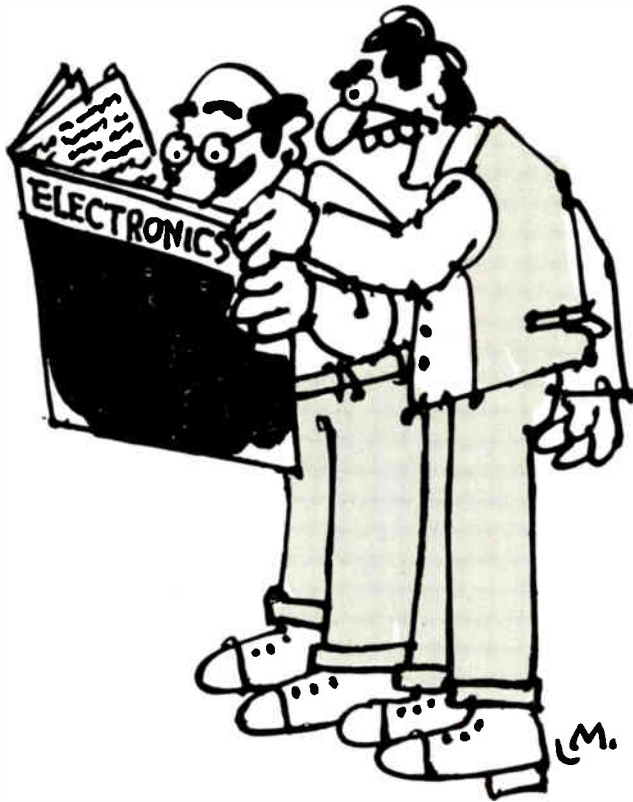


tions, temperature-rise charts, dimensional drawings, mounting tables, accessories, and ordering instructions. An index and preselection chart lists the basic specifications and engineering data for each Curtis series. For a copy of catalog No. 1178, write to Curtis Industries Inc., 8000 W. Tower Ave., Milwaukee, Wis. 53223 [422]

Data-acquisition components. Specifications of digital-to-analog converters, sample-and-hold amplifiers, analog multiplexers, analog switches, voltage references, and comparators are provided in "Harris Data Acquisition Products Guide." A preview of future data-acquisition components offering state-of-the-art performance is also discussed in the eight-page guide. Harris Semicon-

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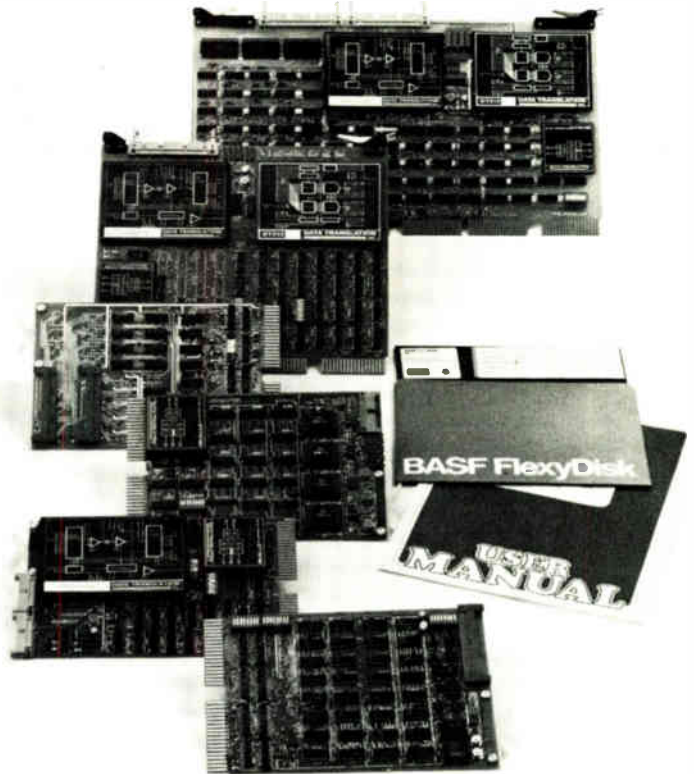
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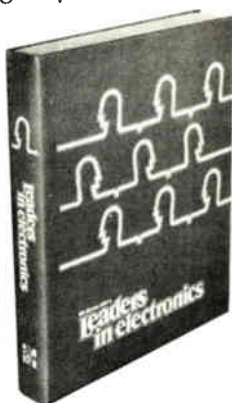
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New literature

ductor, Dept. 53-035, P. O. Box 883, Melbourne, Fla. 32901 [424]

Instruments. Oscilloscopes, frequency counters, and audio and video devices are among the products featured in "Leader Test Instruments." The 60-page catalog gives complete specifications and applications for more than 50 instruments, including probes and other accessories. Leader Instruments Corp., 151 Dupont St., Plainview, N. Y. 11803 [423]

Free newsletter. "Grayhill Engineer" provides insights into recent developments or established technologies in the field of electronics. Each quarterly issue contains a lead article that discusses an interesting development in the electronics industry, yet takes less than five minutes to read. For a free subscription to this newsletter, contact Tom Menzenberger at Grayhill Inc., 561 Hillgrove Ave., LaGrange, Ill. 60525 [425]

Mixers. "Lorch Electronics Mixers and Mixer Preamps" describes 87 different types of mixers, ranging in frequency from 10 kilohertz to 11 gigahertz. The 20-page catalog describes a series of mixer-preamplifiers contained in a 0.81-by-0.81-by-0.15-inch flatpack housing and provides a mixer selection chart that helps choose the proper mixer for a specific application. Copies of Catalog No. FC-794 may be obtained from Lorch Electronics Corp., 105 Cedar Lane, Englewood, N. J. 07631 [426]

Relays. The capabilities and specifications of the Airpax series 37 relay are discussed in a four-page publication. The 5-ampere relay may be used on products built on printed-circuit boards, whether alarm systems, motor generator set control, copy machines, or television circuitry. Also provided in the publication are diagrams of side and bottom views of the Series 37 Relay as well as pc-board-mounting dimensions. Airpax/North American Philips Controls Corp., Husky Park, Frederick, Md. 21701 [430]

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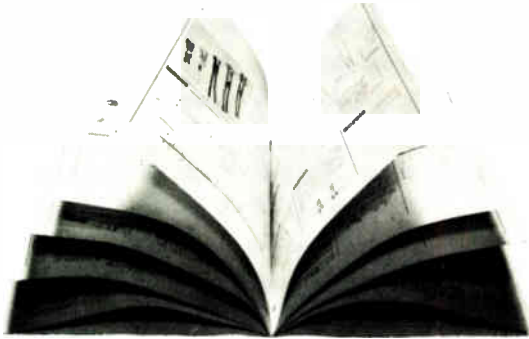
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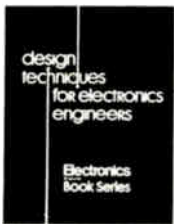
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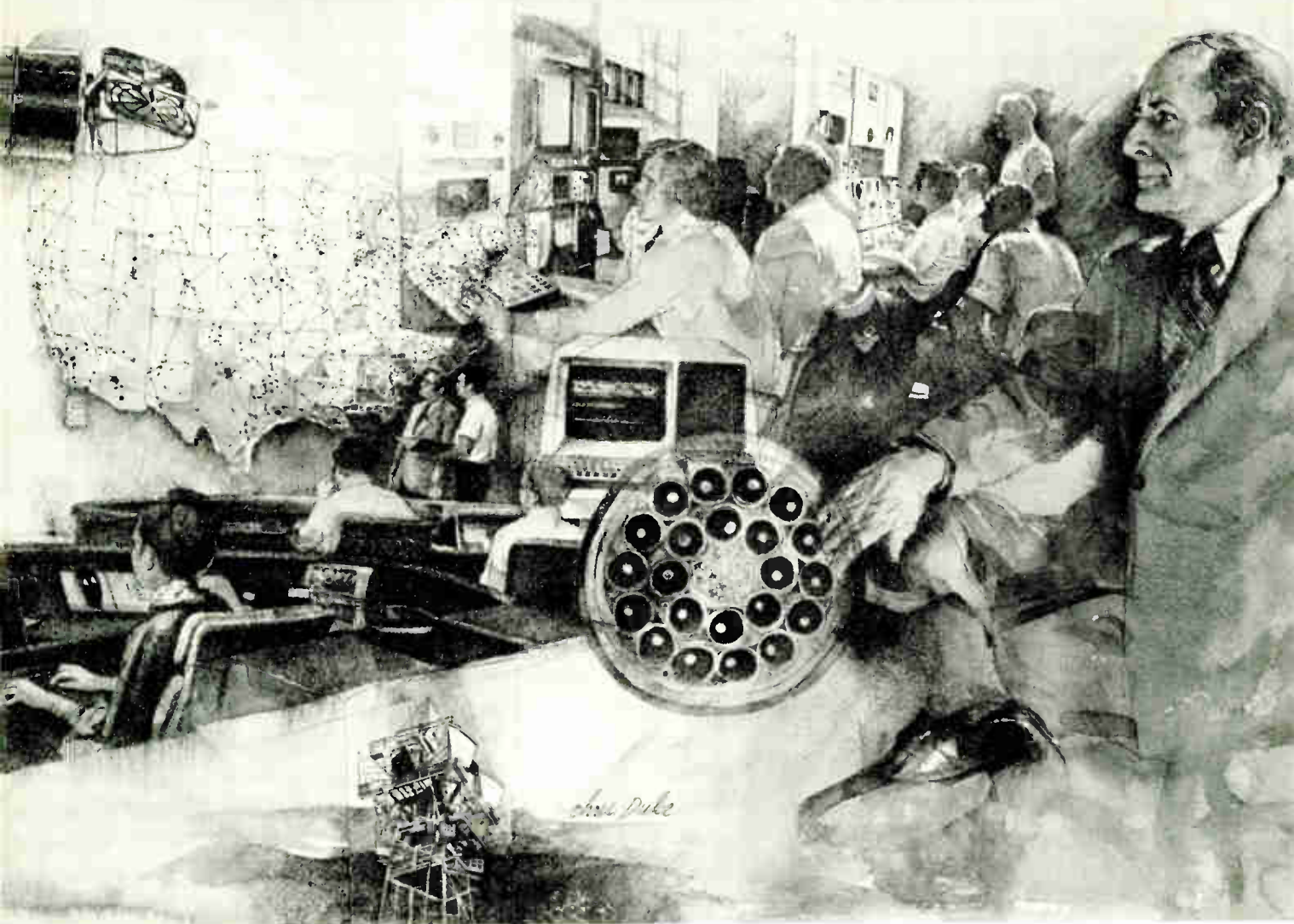
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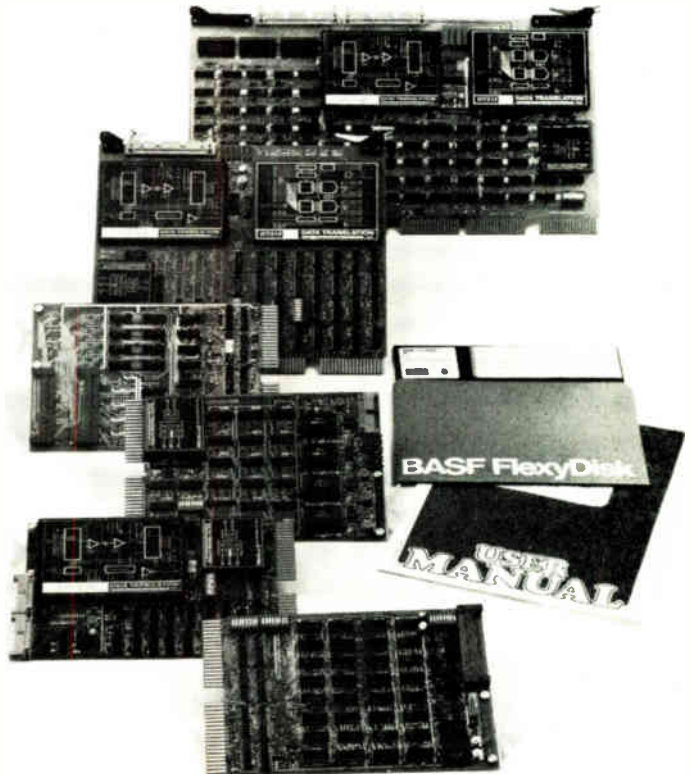
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These openings require senior level engineers with practical experience in system design involving digital multiplexers, switching and transmission equipment. Experience with front-end processing and concentrators, as well as traffic and throughput analysis is desirable. Familiarity with military and international telecommunication standards is required.

● COMMUNICATIONS TERMINAL ENGINEERS

New designs in subscriber terminals with internal processing capability have created openings for system engineers experienced in the definition and application of hard copy and interactive terminals for communication networks to analyze intelligent terminals and their interaction with common link protocols such as X25 and BISYNC. You will have the opportunity of full design, follow-through, implementation and sell-off.

● COMMUNICATIONS CONTROL ENGINEERS

The application of microprocessors in system control has created openings in the development of advanced methods of communications management. Experience required in the analysis of operational requirements of telecommunication systems, their traffic patterns and volumes. You will develop computerized control techniques and integrate with signalling schemes for switching and network control.

● DATA TRANSMISSION ENGINEERS

Develop fiber optic data busses, digital 16K bit/sec modems and programmable voice band terminals using advanced techniques for error detection and correction, digital demodulation of FSK, nonrecursive digital filtering, and digital phase locked loops. Hybrid and custom LSI technologies are used when required.

● MESSAGE SWITCHING ENGINEERS

Apply multiprocessing architecture using microprocessors and custom LSI. Develop diphas modems, high speed forward error correcting encoders/decoders, and cryptographic controllers. This hardware will support multiprocessing software that has specific line protocols, message routing policies and system control concepts.

● CIRCUIT SWITCHING ENGINEERS

Develop a family of low power, high performance circuit switches. PCM and CVSD voice digitization techniques are used with the latest LSI technology to produce a modularly expandable switch. These switches will go into systems ranging from 64 subscriber tactical intercoms to 2000 line all-digital centrals.

RADAR TECHNOLOGY

● RADAR SYSTEMS ENGINEERS

These positions will enable you to lead proposal efforts, studies and system design related to tactical systems using radar and electro-optical technologies. Your background must include previous systems engineering.

SOFTWARE APPLICATIONS

● SOFTWARE SYSTEMS ENGINEERS

Assignments exist for senior level systems engineers with experience in hardware and/or software associated with large scale realtime systems to formulate command and control system requirements and provide specifications for implementation.

POWER SUPPLY

● SR. POWER SUPPLY ENGINEERS

Will develop switching mode power conversion hardware and power distribution networks for large military communications, computer and display systems.

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● LOGIC/FIRMWARE DESIGNERS

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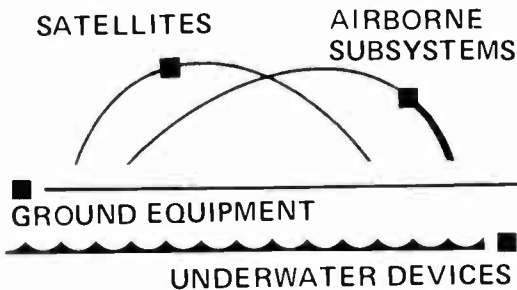
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POSITION: We are seeking a senior development engineer to provide leadership for advanced development of robot hardware and software systems.

REQUIREMENTS: The successful candidate must have a record of accomplishments, innovation and demonstrated ability to lead independent applied research and development of computer interface hardware/software system and electro-mechanical machinery. Must have a strong interest in robotics development. Strong support groups are available in mechanical design, control systems engineering, computer science, and machinery development.

Educational/Experience requirements: An MS or Ph.D. in Mechanical Electrical Engineering, Computer Sciences, Engineering Mechanics or equivalent plus experience in development of computer controlled equipment.

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- **TEST PLANNING**
- **CONTROL SYSTEM ANALYSIS**
- **ELECTRONIC SYSTEM ANALYSIS**
- **SYSTEM SAFETY**
- **POWER DISTRIBUTION ANALYSIS**
- **FACILITIES ENGINEERS - ELECTRICAL/MECHANICAL**
- **MANUFACTURING RESEARCH & DEVELOPMENT ENGINEERS**
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We're seeking engineers to design hardware and software to meet our customer specifications. For hardware design, you'll need a BSEE and 5 years of experience in digital and/or analog in a hardware design environment; microprocessor experience is a plus. Software designers will work with IBM, Honeywell and Burroughs protocols. You'll need a computer science degree and 3-5 years of minicomputer, real-time systems, and programming experience.

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Radio Network Director of Engineering—Six-station interconnected FM radio network in Minnesota seeks engineer with AM, FM, audio, microwave and satellite experience, plus administrative skills, to be responsible for engineering activity as Director of Engineering. Send resume, salary requirements, letter of interest and references to Tom Kigin, Minnesota Public Radio, Box A, 400 Sibley St., St. Paul MN 55101 AA/EQE.

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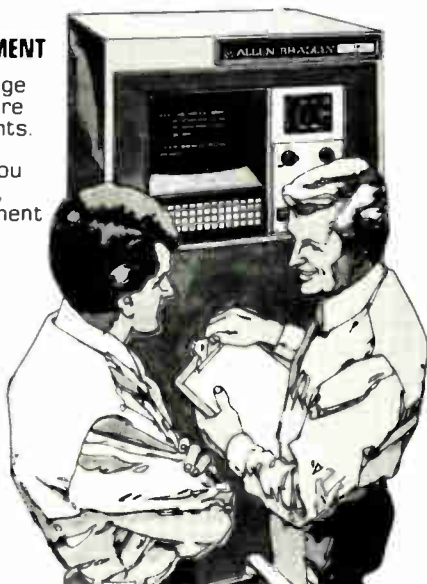
You can apply your 3-5 years of assembler and higher level software expertise to integrate mini-computer and peripheral equipment with programmable controllers, developing new concepts in control functions. Develop sophisticated software by combining your Electrical/Computer Engineering degree with experience in data structuring and systems programming.

COMPUTER AIDED MANUFACTURING SOFTWARE DEVELOPMENT

Develop software systems that can control an entire manufacturing process by interlinking programmable controllers and numerical controls. Initiate programming strategies, translator systems, interfaces and establish host computer/peripheral networks. Your Electrical/Computer Engineering degree and 3-5 years related experience have prepared you for the responsibilities of this position.

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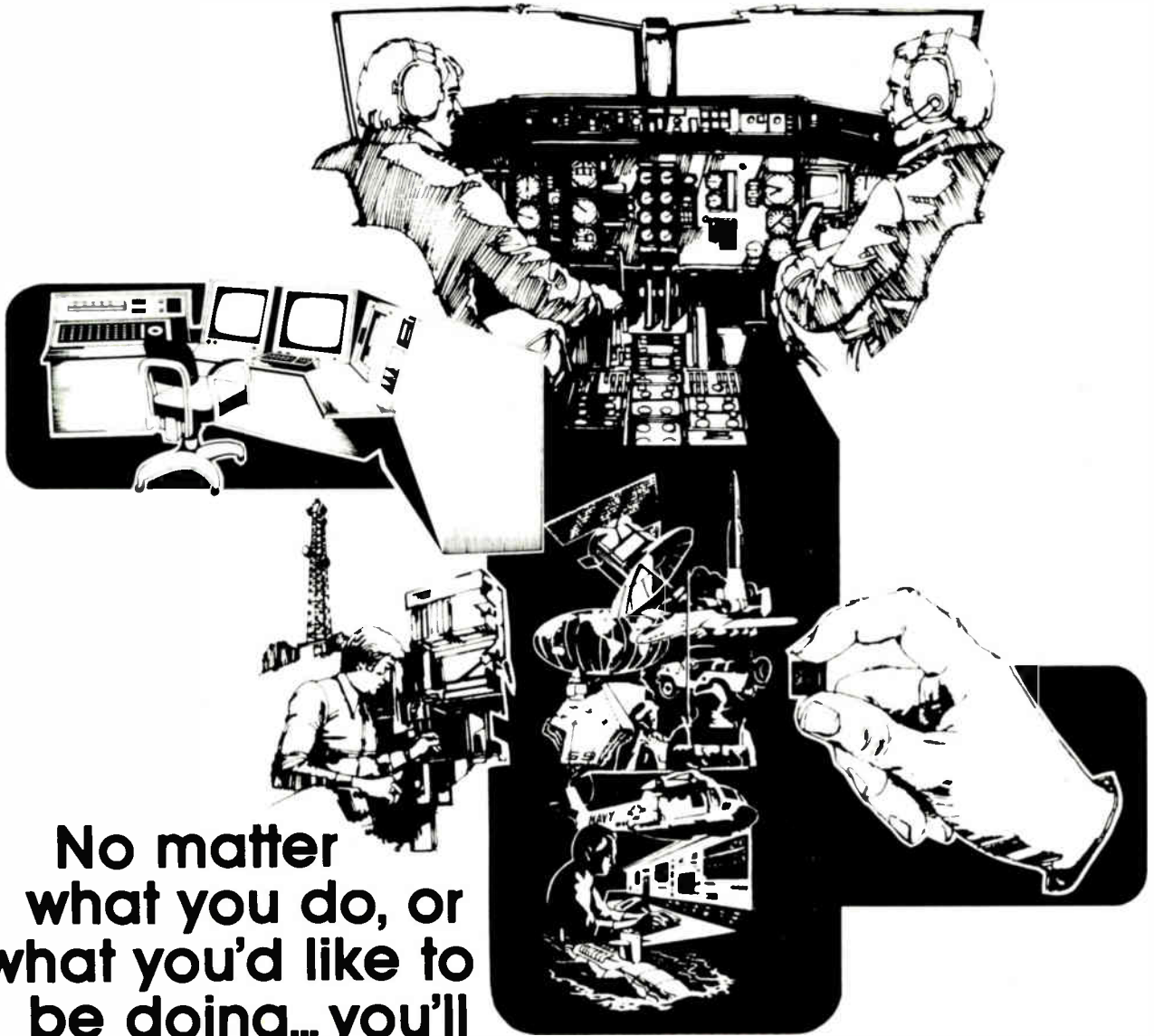
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Located in scenic Cedar Rapids, Iowa, a city that proudly boasts of being comparatively free of pollution, noise, and crime. Cedar Rapids has all the advantages of city life, but in a pastoral setting. In this combination of urban and rural life, our Avionics divisions—the Collins Air Transport Division, the Collins General Aviation Division and the Collins Government Avionics Division—continue the Rockwell tradition of designing and producing quality products through the proper application of state-of-the-art, cost-effective technologies and engineering principles.

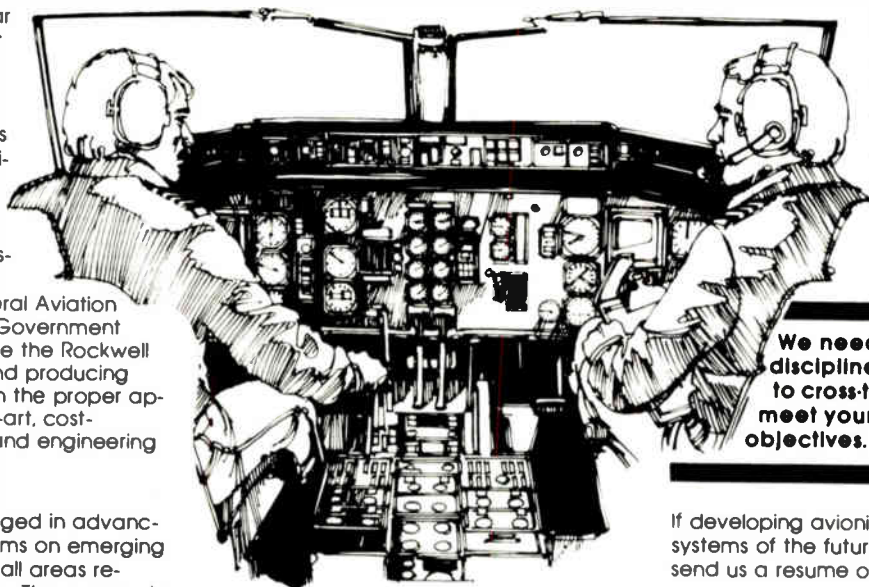
Our engineers are engaged in advanced experimental programs on emerging technologies related to all areas required to product design. These areas include: avionics systems, analog/digital circuits, digital computers, software, microwave circuits, sensors and display. As well as developing new products and technologies, Rockwell is the established industry leader in quality and reliability for aviation products.

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Not to be outdone, the Collins General Aviation Division is also a leading supplier of avionics systems, products, and services to a broad range of customers in business and private aviation. Our



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Our Collins Government Avionics Division is a dedicated group of people that specialize in supplying high-technology avionics and automated test equipment to the U.S. military and other governments throughout the free world. Our engineers not only supply the world with the most up-to-date equipment for military aircraft, but are also hard at work developing the next generation of navigation systems. Recently, they were awarded a contract to help develop the Navstar

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MISSILE X (MX)

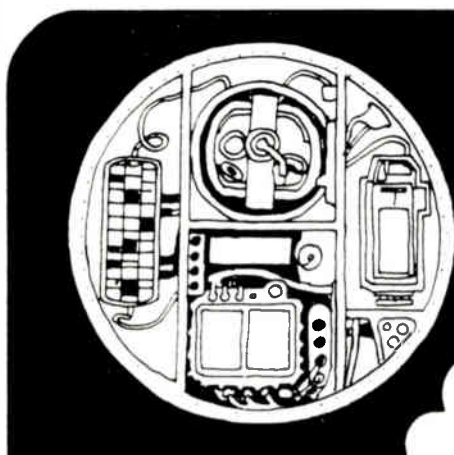
The Autonetics Strategic Systems Division in Anaheim, California is involved in the development of guidance and control systems, and advanced electronics for missiles, space vehicles and aircraft.

ASSD has been selected to play a major role in the full scale development of the nation's newest generation of land-based ICBM's-MISSILE X. The division will have responsibility for the MX guidance and control system, and for the critical operational support equipment. In addition, they are involved in ongoing programs for the Minuteman and a new, light-weight, highly accurate strapdown navigator which employs electro-statically supported gyro technology.

MISSILE X will introduce state-of-the-art technology that calls for the nation's highest levels of scientific and engineering skills. For instance: Accuracy-3 times better than Minuteman III; Hardness-10 times Minuteman III requirements; Device Technology-Bipolar MSI circuits based upon Trident parts...plated-wire memory...potential alternate memory using hardened MNOS/SOS technology.

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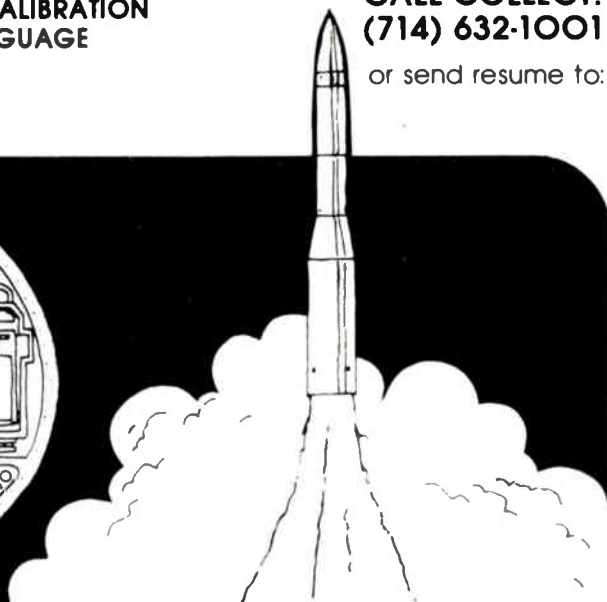
A majority of the available positions are for engineers with less than six years experience, including many opportunities for recent college graduates.

The MISSILE X (MX) high priority contract calls for team effort by the nation's finest scientists and

engineers, and staffing for the program is underway.. If you would be interested in participating in this effort, ACT NOW. We will be selecting qualified candidates as rapidly as possible, and we invite you to explore opportunities on Rockwell International's MISSILE X Team.

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MARINE SYSTEMS

Autonetics Marine Systems Division (AMSD) in Anaheim, California is a leader in research and development involving ships inertial navigation systems, ships signal processing, sonar processing equipment, shipboard data multiplex systems, shipboard command and control systems, and a state-of-the-art electrostatically supported gyro monitor.

The Navy has recently awarded AMSD a contract to design, develop, manufacture and test an Advanced Mobile Acoustic Torpedo Target (ADMATT), to simulate evasive actions taken by an enemy submarine.

The Division's submarine systems experience encompasses detailed analytical studies...hardware design and production...operational and interface software design...system integration...computerized systems simulation and evaluation...and design and production of training equipment.

AMSD's efforts in acoustic signal processing, beamforming and automatic tracking have been supported by Navy contracts as well as substantial independent and development funds.

A significant breakthrough in ship design and construction methodology, developed by AMSD, involves the use of multiplexing for shipboard data transfer, which replaces the traditional massive amounts of cabling, junction boxes, switchboards, etc.

Autonetics Marine Systems Division has a dedicated, secure hardware/software integration capability for developing and testing a full range of software for the effective integration of increasingly complex electronics systems such as communications, navigation, radar, sonar, and fire control systems.

Graduate engineers with experience, and new college graduates, will be interested in a variety of positions available in Anaheim, California; Arlington, Virginia; and Groton, Connecticut. If your experience and/or

- SHIPBOARD INERTIAL NAVIGATION SYSTEMS ENGINEERING

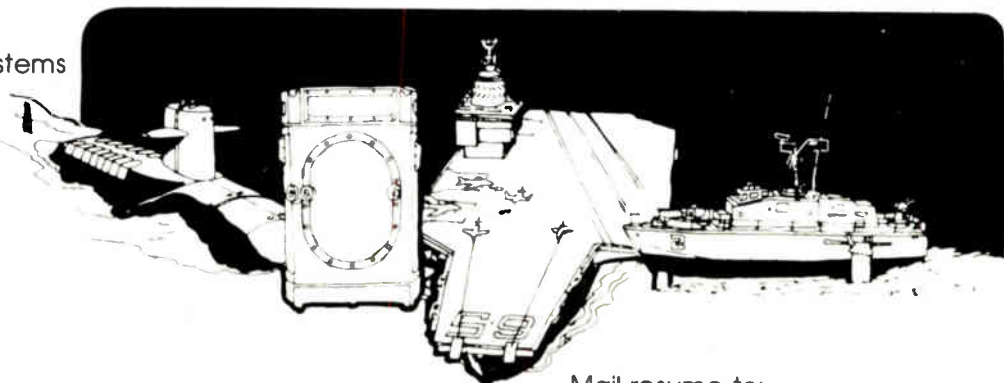
- ACOUSTICAL ENGINEERING

- TRAINING REQUIREMENTS

- SYSTEMS MAINTAINABILITY

- FIELD ENGINEERING

- TECHNICAL WRITING



Mail resume to:

**Autonetics Marine
Systems Division
Rockwell International
3370 Miraloma Avenue
Anaheim, CA. 92803**

Attn: Dept. E830-AA39

We are an equal opportunity employer. Minorities, women and handicapped are encouraged to apply.

interests lie in any of the following areas, we would like to hear from you!

- NAVAL TACTICAL DATA SYSTEMS ENGINEERING

- SONAR SYSTEMS ENGINEERING

- SUBMARINE COMBAT SYSTEMS ENGINEERING

- SHIPBOARD COMBAT SYSTEMS ENGINEERING



**Rockwell
International**

...where science gets down to business

TELECOMMU-

SPACE & SECURE TELECOMMUNICATIONS SYSTEMS

Rockwell's Space and Secure Telecommunications Systems Division is one of the world's leading suppliers of satellite communication terminals and tactical and strategic data communications equipment.

Products range from microminiature components to large scale systems, and cover the entire frequency spectrum from very low frequency to light.

The Division is a leading supplier of satellite communication systems and products to military and government agencies around the world in the UHF, SHF and EHF ranges, and of space-qualified electronic products for use in satellites.

We are also a leader in secure communication systems, provide strategic and tactical communication and surveillance systems and cryptographic devices for submarine, shipboard, airborne, and shorebased applications.

Our engineers and scientists provide the base for the Division's continued technological leadership in the fields of satellite communications, real-time signal processing, software systems and electro-optical imaging. Some of the positions currently available include:

SIGNAL PROCESSING ENGINEERS: Enter the challenging world of real-time signal processing using bit-slice microprocessors imbedded in state-of-the-art modems for VLF, HF and UHF communications systems.

ANALOG CIRCUIT DESIGNERS: Immediate openings for engineers in all facets of analog design, with particular emphasis on special techniques for controlling EMI and TEMPEST hazards.

DIGITAL CIRCUIT DESIGNERS: Perform conceptual design and implement state-of-the-art military communications hardware.

Successful candidate will perform system and equipment design, breadboard and prototype testing and hardware-software integration.

SOFTWARE SYSTEMS PROGRAMMERS: Perform systems design through all of the development stages, including design, code, test, and system integration. Hardware background with

microprocessor development desirable. You should have strong assembly language programming skills related to microprocessor development systems.

SENIOR SATCOM SYSTEM ENGINEER: Immediate opportunity for senior engineer with an MS or PhD and 10 years analytical and design experience.

COMPONENT/RELIABILITY ENGINEERS: Opportunities exist for engineers with a thorough knowledge of passive and/or active devices including connectors, materials and processes.

If our careers sound interesting to you, send a resume or call us COLLECT:

Jeff Dwhylie
Mgr. Personnel Resources
Space & Secure
Telecommunications
Systems Division
Rockwell International
P.O. Box "C"
Newport Beach, Calif. 92660
(714) 833-4442

TELECOMMUNICATIONS PRODUCTS

The Collins Telecommunications Products Division of Rockwell International is located in Cedar Rapids, Iowa and produces a wide and diverse range of advanced communications equipment for airborne, shipboard, vehicular, manpack, and fixed-station applications.

As one of the world's largest communications equipment suppliers, we manufacture many of the traditional Collins products that have established industry standards for excellence in quality and reliability. Our capabilities extend throughout the communications spectrum with products that are sold worldwide to government, industrial, and individual customers.

Major new programs in advanced tactical communications represent an unusual opportunity for degreed engineers who can bring fresh thinking and innovative approaches to these growing business areas.

HF COMMUNICATIONS: Experience in HF technologies such as skywave propagation, channel characterization, and communication equipment design.

MICROPROCESSOR SOFTWARE/FIRMWARE: Beginning and intermediate

positions in our Advanced Technology department. Experience with soft/firmware desirable.

AUTOMATIC TEST EQUIPMENT: Software support and hardware design. Analysis, design, development and integration of special test instrumentation and adaptor utilizing microprocessors, calculators and HP MS21 minicomputers. Knowledge of Fortran-IV, Basic and HP RTE III/IV Operating systems required.

RF ENGINEERS: Application of fiber optics for control and communication in EM environment. EMI/EMC engineering and use of large computer/analysis tool. Knowledge of EM coupling or propagation and antennas required.

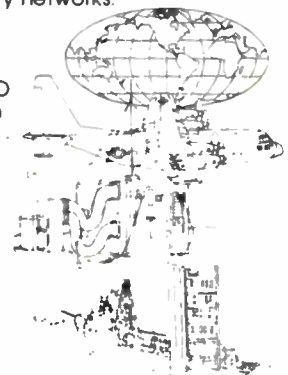
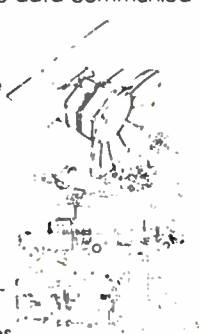
Send Resume or call COLLECT:
Nelson Brown, Professional Staffing
Collins Telecommunications
Products Division
Rockwell International
855 35th Street, N.E. M/S 137-157
Cedar Rapids, Iowa 52406
(319) 395-2381

TELECOMMUNICATIONS SYSTEMS

The Collins Telecommunications Systems Division of Rockwell International's Electronic Systems Group-Dallas is a major supplier of telecommunications systems for tactical, strategic, and national networks. Spanning the entire communications frequency spectrum and all modes of operation, these systems have been supplied to military and government agencies in more than 40 countries and are the backbone of many U.S. military networks.

One of the division's major programs is the Navy's TACAMO Communication System. This airborne system provides the only around-the-clock communication link that allows the President to relay messages to deployed strategic submarines. For the Air Force, the division supplies numerous types of systems including communication shelters, such as the TSC-60 which can be transported by air or truck to new sites as needed. The division also provides various communications systems to international government and military customers.

To maintain our leadership position in



COMMUNICATIONS

these markets, we are continually investing in the development of new technologies and systems capabilities. Because of the commitment to improvement, we are looking for:

MECHANICAL ENGINEERS who can develop and implement communications systems, thermal and stress analysis, mechanical design, and electronic packaging.

ELECTRICAL ENGINEERS who will participate in the design of communication systems, and should be familiar with military communications.

SOFTWARE ENGINEERS with experience in the design, use, testing, and documentation of real-time software-systems.

Interested and qualified candidates are invited to submit resume or call collect:

Alan Leverett,
Mgr. Salaried Resources
Collins Telecommunications
Systems Division
Rockwell International
P.O. Box 10462, Dallas, Texas 75207
(214) 996-7021

SWITCHING SYSTEMS

Voice and Data Switching Systems, Fingerprint Identification Systems, and Energy Management Systems...that's what the Collins Communication Switching Systems Division is all about. We solve communications problems for a wide diversity of industries. Banks use our switching systems to handle their transactions. Most major airlines have turned to our voice switching systems to handle reservations. Electric Utilities are depending upon our Energy Management Systems to permit them to continue to provide power at a profit to an increasing number of customers despite inflation and fuel shortages. And our Fingerprint Identification Systems should soon provide the solution to numerous security problems by replacing the commonly used "lock & key" with the touch of a finger.

The Division has an immediate need for the following individuals.

SOFTWARE SYSTEMS PROGRAMMERS: PL-1 or Pascal with DEC POP-11 experience

DATA BASE MANAGEMENT SYSTEM DEVELOPERS: CODASYL level DBMS experience as applied to digital switching product lines

COMPILER DEVELOPERS: Compiler organization experience coupled with knowledge of Fortran and global optimizers code/generators

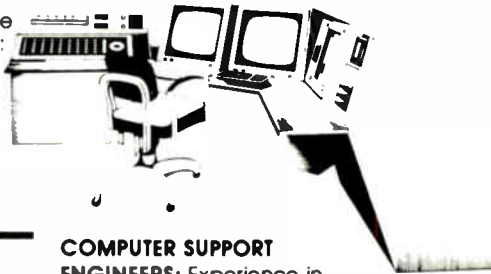
OPERATING SYSTEM SPECIALISTS:

Knowledge of DEC POP-11 RSX-11 operating system

PROTOCOL SPECIALISTS: Experienced in Bisynch protocol

SOFTWARE SUPPORT ENGINEERS: Experience in real-time environment, large scale operating system. Knowledge of Fortran, assembly, design, coding, documentation and integration on a Xerox Sigma mainframe

SYSTEMS ENGINEERS: Knowledge of system design engineering, network planning, transmission performance specification, T-Carrier technology



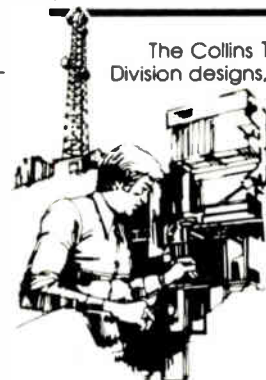
COMPUTER SUPPORT

ENGINEERS: Experience in support and maintenance of mini-computers

Qualified candidates are invited to submit a resume or call collect:

Mr. William McKinney
Collins Communication
Switching Systems Division
Rockwell International
3330 Miraloma Avenue
Anaheim, California 92803
Div. 090, SA-O1
(714) 632-1841

TRANSMISSION SYSTEMS



The Collins Transmission Systems Division designs, develops,

and manufactures microwave systems (primarily used by telephone companies and railroads), satellite communications (design and install earth station systems), and commercial broadcast products (everything needed to put an

AM/FM station on the air).

Microwave transmission provides multi-channel voice, data and video as primary communication for long haul,

inter-city and intra-city interconnections. The bulk of these communications is between central office switching centers where communications are concentrated, processed and distributed.

Satellite transmission provides point-to-multipoint communications for television, radio and news services, as well as point-to-point telecommunications for voice, data and facsimile.

Broadcast provides electronic equipment for commercial and educational AM and FM radio stations.

Opportunities exist for recent graduates and experienced candidates at the BS, MS and PhD levels in the following areas:

SATELLITE SYSTEMS ENGINEERS: Perform analysis, design and test of satellite communication systems for domestic and international applications.

MECHANICAL ENGINEERS: To design and document electronic packaging for microwave and multiplex subsystems and modules.

FIELD SUPPORT ENGINEERS: To assume responsibilities for installation, test and alignment of microwave systems or satellite ground stations throughout the world.

ANALOG/DIGITAL/LOGIC DESIGN

ENGINEERS: Circuit design and product development engineering for communications systems.

MULTIPLEX DESIGN ENGINEERS: To assume hardware design and development responsibilities for multiplex and sub-system units.

UHF/MICROWAVE DESIGN ENGINEERS:

To assume hardware design and development responsibilities for microwave radio-relay communications equipment.

INDUSTRIAL ENGINEERS: To develop basic manufacturing, fabrication, and inspection methods, processes, labor cost, standards, performance and assembly line write-ups.

Interested and qualified candidates are invited to submit resume or call collect:
Don Elder, Employment Manager
Collins Transmission Systems Division
Rockwell International
1200 North Alma Road
Richardson, Texas 75080
(214) 996-7189

We are an equal opportunity employer. Minorities, women and handicapped are encouraged to apply.



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MICROELECTRONICS

The best electronic brains are still human

In the ever advancing world of microelectronics, leadership belongs to companies which prize the value of human resources. This is the source of Rockwell's power in microelectronics.

Rockwell's Electronic Devices Division supplies components and devices to the company's billion-dollar-plus electronic control, guidance and communications operations. We're also a major microelectronic supplier to key firms worldwide.

Rockwell's commitment to leadership in microelectronic research, design and production is also a commitment to providing professionally satisfying careers for our engineers and scientists. Rockwell's current activities document this:

- Rockwell is the first company to demonstrate a megabit bubble domain memory device, and the first to put a 256K-bit device into production. Volume production of megabit devices begins in 1980 while Rockwell scientists work on 4 megabit and larger devices.
- Rockwell, a leader in high speed LSI modems, is the first company to design and market a modular 2400 bps modem capable of low-cost integration into systems of

communications and computer related equipment.

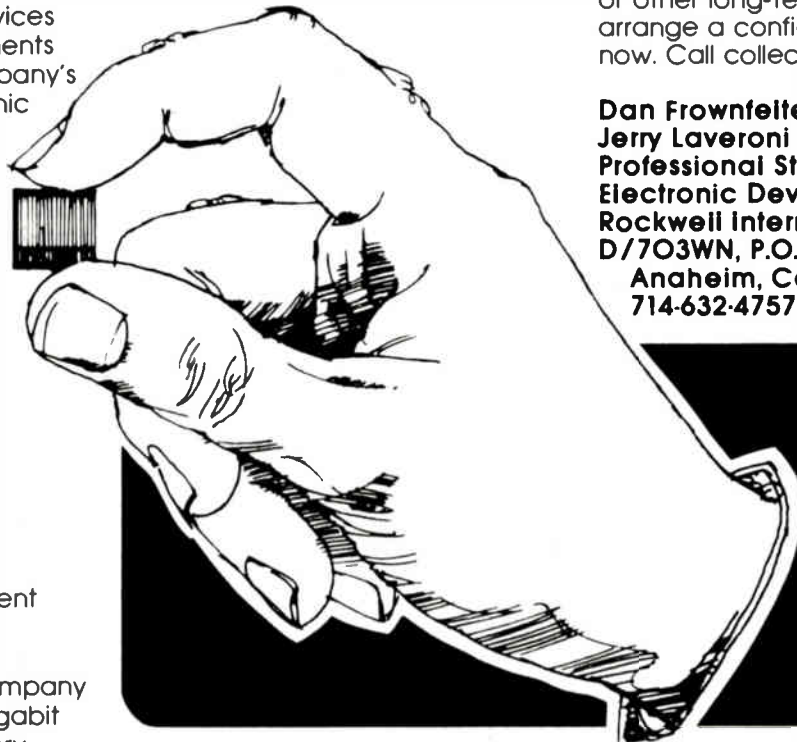
- Rockwell is volume producing NMOS, third generation R6500 microprocessor devices, and is phasing into VLSI production. In our laboratories, we've fabricated NMOS transistors with

developing gallium arsenide (GaAs) technology.

Career opportunities at Electronic Devices Division

If you're interested in enlarging your career in the fields of bubble memories, data modems, VLSI and VRSIC, SOS-LSI, GaAs, or other long-term technologies, arrange a confidential interview now. Call collect or write:

**Dan Frownfelter or
Jerry Laveroni
Professional Staffing
Electronic Devices Division
Rockwell International
D/703WN, P.O. Box 3669
Anaheim, California 92803
714-632-4757**



1/4-micron gate lengths in a ring oscillator that's achieved switching speeds of 80 picoseconds.

- We're leaders in developing CMOS-SOS-LSI technology. We've demonstrated an 8,000-FET device with two micron gate lengths operating at 70 megahertz. We're transferring CMOS-SOS-LSI technology into production. Rockwell also leads in

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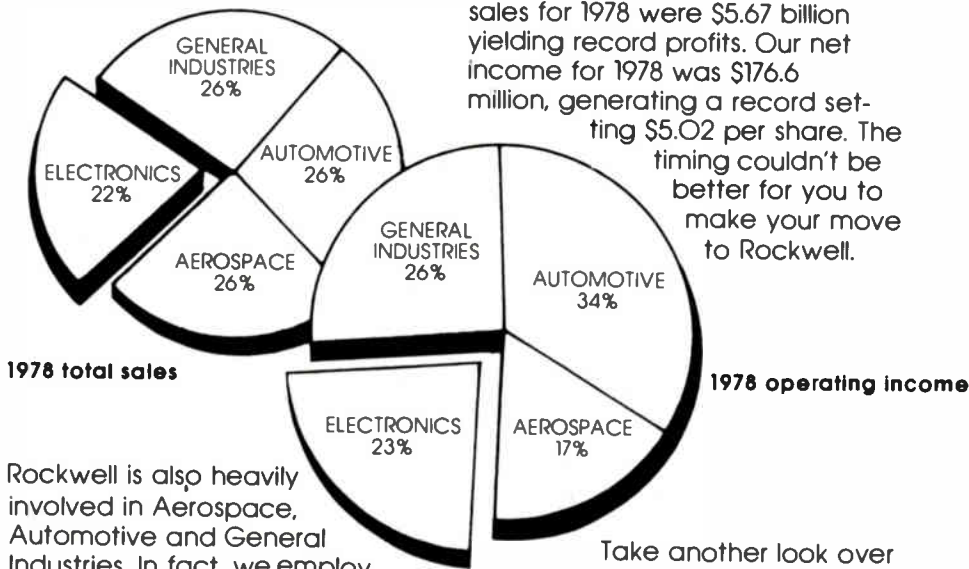
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ROCKWELL INTERNATIONAL OFFERS MORE...MUCH, MUCH MORE!

You have just seen a sampling of the outstanding opportunities available with Rockwell International's Electronics Operations.

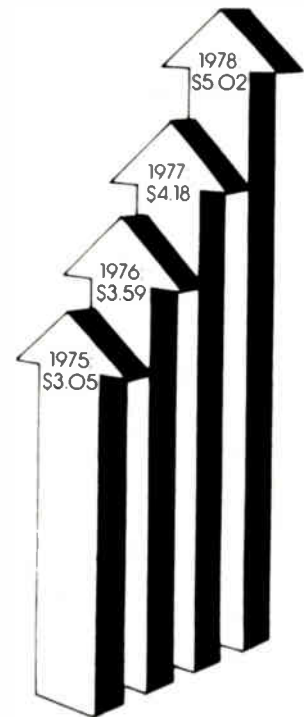
Rockwell International's total sales for 1978 were \$5.67 billion yielding record profits. Our net income for 1978 was \$176.6 million, generating a record setting \$5.02 per share. The timing couldn't be better for you to make your move to Rockwell.



Rockwell is also heavily involved in Aerospace, Automotive and General Industries. In fact, we employ over 14,300 scientists and engineers...or approximately one percent of America's total scientific-engineering community. If the ideal position for you doesn't exist within our organization, chances are that it just doesn't exist.

Take another look over this section. Call or write the representative immediately following the position of most interest to you. Feel free to contact as many of our people as you desire. Everyone from recent college graduates to seasoned professionals are welcome.

Earnings per share



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SOFTWARE ENGINEERS



TRW VIDAR
on the
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continues to broaden
its scope of activities
in the telephony industry
with controlled but
outstanding growth
in the development
of its digital
switching systems.

You have exciting and rewarding opportunities awaiting you with TRW Vidar, as one of the leading companies in the industry. Our current needs in our Switching Product Assurance group require individuals interested in continuing their professional development in such a challenging, dynamic environment.

Working as a Switching System Test & Evaluation Engineer, you will have responsibility for planning, designing, documenting, introducing & supporting programs for Product Assurance testing of our digital switching systems. In addition to a degree in CS or EE, your background should include experience in microprocessor programming with real time operating systems. Familiarity with current hardware technology and prior telephone switching systems experience are a plus.

Professional opportunities at TRW Vidar are excellent. Our outstanding benefits program and attractive work environment make our company the right one to explore.

Call 415/961-1000 for Dick Duncan in our Professional Placement department to discuss your background, or send him a resume outlining your experience. (You'll receive prompt consideration.) TRW Vidar, 77 Ortega Ave., Mt. View, CA 94040. An equal opportunity employer M/F.

TRW VIDAR

Electronics Design Engineer

We are a major producer of instruments and chemicals for the life science market with a requirement for an Electronics Engineer to be responsible for the design of analog and digital circuitry for operations of analytical instrumentation. Work includes power supplies, control circuitry and transducer signal processing. Familiarity with digital logic and microprocessor fundamentals desirable. BS or MS in electronic engineering and 3-5 years' experience required.

We are located in the San Francisco Bay Area and offer an environment for personal achievement and career growth. For confidential consideration send resume to Personnel Director, Bio-Rad Laboratories, 2200 Wright Avenue, Richmond, CA 94804. An equal opportunity employer.

BIO-RAD Laboratories

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ELECTRONICS ENGINEERS, \$15K-\$40K. Immediate west coast & national positions entry level thru mgmt in commercial, aerospace & communications industries. We will put you in contact with large, medium or small prestigious cos desiring backgrounds in analog, digital, microprocessor, instrumentation, microwave technology & related areas. For immediate confidential response, call or send resume w/salary history to Glenn English, President, GLENN ENGLISH AGENCY, 7840 Mission Center Ct., San Diego, CA 92108 (714/291-9220).

ELECTRONICS ENGINEERS, \$18,000-\$50,000. Choice entry level to management positions immediately available in Pennsylvania & national locations. Reply in strict confidence to J. G. Weir, President, WEIR PERSONNEL SERVICES, 535 Court St., Reading, PA 19603 (215/376-8486).

DESIGN ENGINEERS to \$38K. Central Penna. Design connectors/terminals, micro-processors. Outstanding relocation packages. Prompt confidential reply. MECK ASSOC. PERSONNEL, 1517 Cedar Cliff, Camp Hill, PA 17011 (717/761-4777).

all positions fee-paid



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At National we are making an investment to change computer design through semiconductor technology. This is part of our commitment to making computers accessible to a broader market at more effective price and performance, than is available today.

Areas of experience should include major mainframe manufacturer's mini-computer manufacturer's and microprocessor manufacturer's. 3 to 5 years working experience with CPU's, peripherals, operating systems, traditional languages, and systems configuration or integration knowledge, plus a technical education is required.

INVEST IN YOUR FUTURE BY JOINING NATIONAL'S COMPUTER PRODUCTS GROUP

Computer systems professionals with areas of specialties that include: Mini, Micro, Mainframe, and Memories...the following positions are currently open:

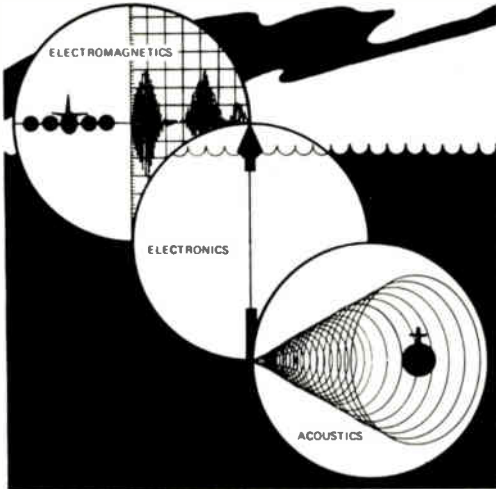
- Software Development
- Mechanical Packaging
- Software Support
- Manufacturing Engineering
- Analog Design
- Digital Designers
- Design Drafting
- Field Service
- Product Management
- Micro Code Specialists
- Test Engineers
- Software/Hardware Training Specialists
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For information, call Jim Rook COLLECT (408) 737-5000, or send your resume to him at: National Semiconductor, 2900 Semiconductor Drive, Santa Clara, California, 95051. An equal opportunity employer m/f/h.

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 **National Semiconductor**
Computer Products Group

SPARTON ELECTRONICS



Sparton Electronics -- Our approach has always been a little different. It's our nature to experiment and innovate -- you see it in everything we do. But it's not just the innovation, it's the testing and research behind it. That's why we place such importance on you -- the engineer -- and that's why we have so much to offer. If you are an experienced EE or ME looking for more challenge and responsibility or maybe you just enjoy a small town atmosphere with easy access to almost any kind of recreation, check out Sparton Electronics.

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Electronic Design Engineers - Responsible for the design of VHF-UHF receivers and transmitters, sonar receivers and transmitters, and various analog and digital circuits. Experience applicable to one or more of these areas required.

Mechanical Design Engineers - Responsible for the mechanical design of low-cost, high-quantity electromechanical and electronic equipment. Experience should include the design of injection moldings and die castings. Responsibilities consist of conceptual design, prototype build and qualification, and production support.

Call or send resume and salary requirements to:
Gary Whitworth, Employee Relations Manager



sparton electronics

2400 E. Ganson St
Jackson, Michigan 49202
Phone (517) 787-8600

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IC ENGINEERS

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Our 160,000 square foot facility will include a full wafer fab line, test capability and an R&D department. Immediate openings are available for:

- 10 Process Engineers (NMOS, CMOS)
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- 10 Design Engineers (MPU's, Memories)

These truly exceptional opportunities require a BS/MS/PhD degree and one to five years of experience, preferably in MOS. Fluent French is NOT mandatory, as complete language training will be provided in France.

Depending upon experience, a short time will be spent at one of National's facilities prior to relocation. For a unique combination of challenge and lifestyle, send your resume to **Bob Hasselbrink at National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051**. An equal opportunity employer, m/f/h.

An expansion program at our client, a major non-military division of a leading international technology company, has created the following career opportunities.

MANAGER ELECTRONIC TECHNOLOGY \$40,000-45,000

Working manager of a growing group, responsible for new concepts and systems in international Research & Development of advanced technology programs for consumer and industrial products.

Should have R&D management experience in automatic controls, microprocessor and PC board technology, circuit design, servomechanisms and electro/mechanical power transducers, in addition to electronics or physics degree. This position leads to definite further management growth.

GROUP LEADER LSI DESIGN \$30,000-35,000

Working leader of small group involved in developing digital MOS chips. Some knowledge of analog and hybrid design helpful for future work.

Electronic packaging expertise would also be useful. Must be able to use simulation techniques to verify design. EE or equivalent degree plus 5 years applicable experience necessary

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SALES ENGINEERS

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Minneapolis, Minn.
Portland, Ore.

Responsible for the sale of engineered materials and components for the electronics, transportation, and electrical original equipment manufacturing markets. Seeks new product opportunities and applications with new and existing customers. Works with R&D, Marketing, Engineering, and Production. BSEE, BSME, or equivalent plus 3-5 years related sales experience working with electrical/electronic design engineers required. Send resume, salary requirements and geographic preference to: J.A. Richie, Corporate Employment Administrator, Rogers Corporation, Rogers, Conn. 06263.

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- Power Systems Engrs.
- Sr. Military Systems Engrs.
- Field Engrs.(Electronic Equip.)
- Digital Systems Engrs.
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- Technicians

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Submit Resume, Call or Visit:
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Boston, Massachusetts 02110
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Motorola's Government Electronics Division - Scottsdale and Tempe, Arizona - is seeking design and development engineers for our communications, radar, and tactical electronics operations. GED is over 4000 people strong, setting records in sales and bookings, and has opportunities in a wide range of disciplines.

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- ★ Frequency Synthesizers - Circuit design experience at 1 GHz and below including VCO's, filters, mixers, and phase locked loops.
- ★ Space Data Systems - RF experience including OP amps, stable oscillators, and low noise detection of signals.
- ★ Wideband Receiver Systems
- ★ Microwave Synthesizers - experience with UHF band, wide tuning ranges, low phase noise.
- ★ FM Telemetry/Pulse Amplifiers - knowledge of fast pulse and spread spectrum techniques.
- ★ Microwave Circuit Design - 5 to 10 years experience in solid state circuits built in a variety of transmission lines operating at frequencies from 1-20 GHz.
- ★ S/X Band Transponders - design and test

DIGITAL SYSTEMS AND HARDWARE

- ★ Satellite Communications Systems - A/D converters, microprocessors, control circuitry.
- ★ Digital Circuits - radar applications, micro-processor design, some tempest design.
- ★ Design and test of MOS LSI and TTL devices.

ANTENNA DEVELOPMENT

- ★ Project engineers experienced in tracking antennas, active phased antennas with knowledge of stripline and millimeter wave techniques.
- ★ Analog/Servo Mechanisms - antennas, servo amps, and analysis.

LOGIC DESIGN

- ★ Broadband high speed (1-1000 MHz) logic design and hardware implementation.
- ★ Senior Logic Designer/Task Leader - TTL, CMOS, and ECL, MPU hardware and software.
- ★ Wideband Sampled Data Systems - high data rates (100 Mbps).

EW SYSTEMS

- ★ Subsystem development to include antenna, acquisition, set-on receivers, processors, and repeater loops. ECM configuration.

FUZE SYSTEMS

- ★ Radar Fuze Design - High G environment.
- ★ Microwave Experience - microstrip RF head design in high G environment.
- ★ PCM and FM telemetry

MECHANICAL ENGINEERS

- ★ High density packaging - RF and microwave
- ★ Airborne and Ground TTL packaging
- ★ Space-borne equipment

HP 21 MX

- ★ Design and programming of distributed systems - Assembly Language and Fortran

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- ★ Industrial Engineers - tool engineering, mechanization, floor layouts, work flows.
- ★ Project Managers - project planning and control, budget, and scheduling.

Accept our challenge. It is your opportunity to join a very successful electronics team in an environment conducive to your professional growth. If you are interested in joining our team, please apply in person or forward resume to:

Rich Moran, Dept. 476

MOTOROLA
Government Electronics Division

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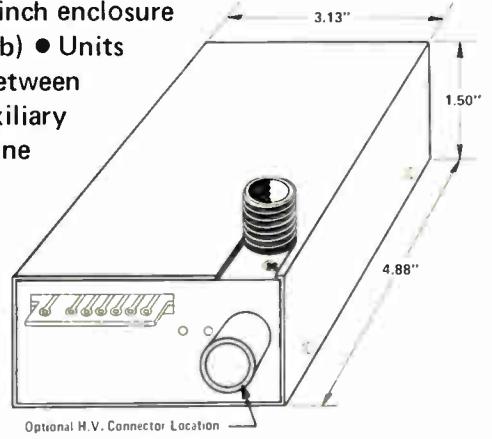
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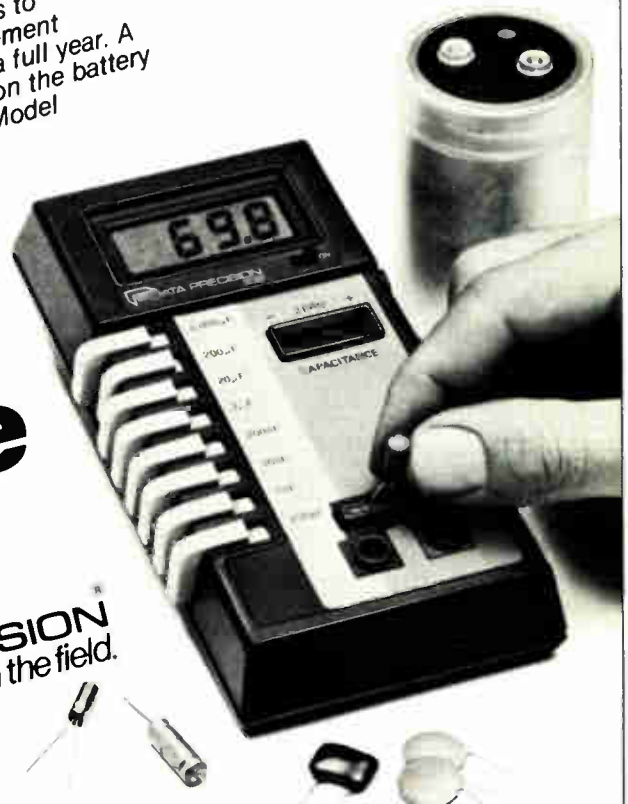
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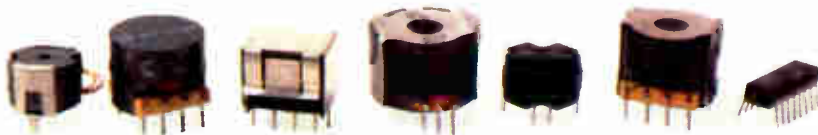
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