OCTOBER 12, 1978

PULLOUT GUIDE TO THE WORLD'S COMMUNICATIONS SATELLITES/120

Pascal looms large as software language/81

How to compress long test patterns for large-scale integration/136

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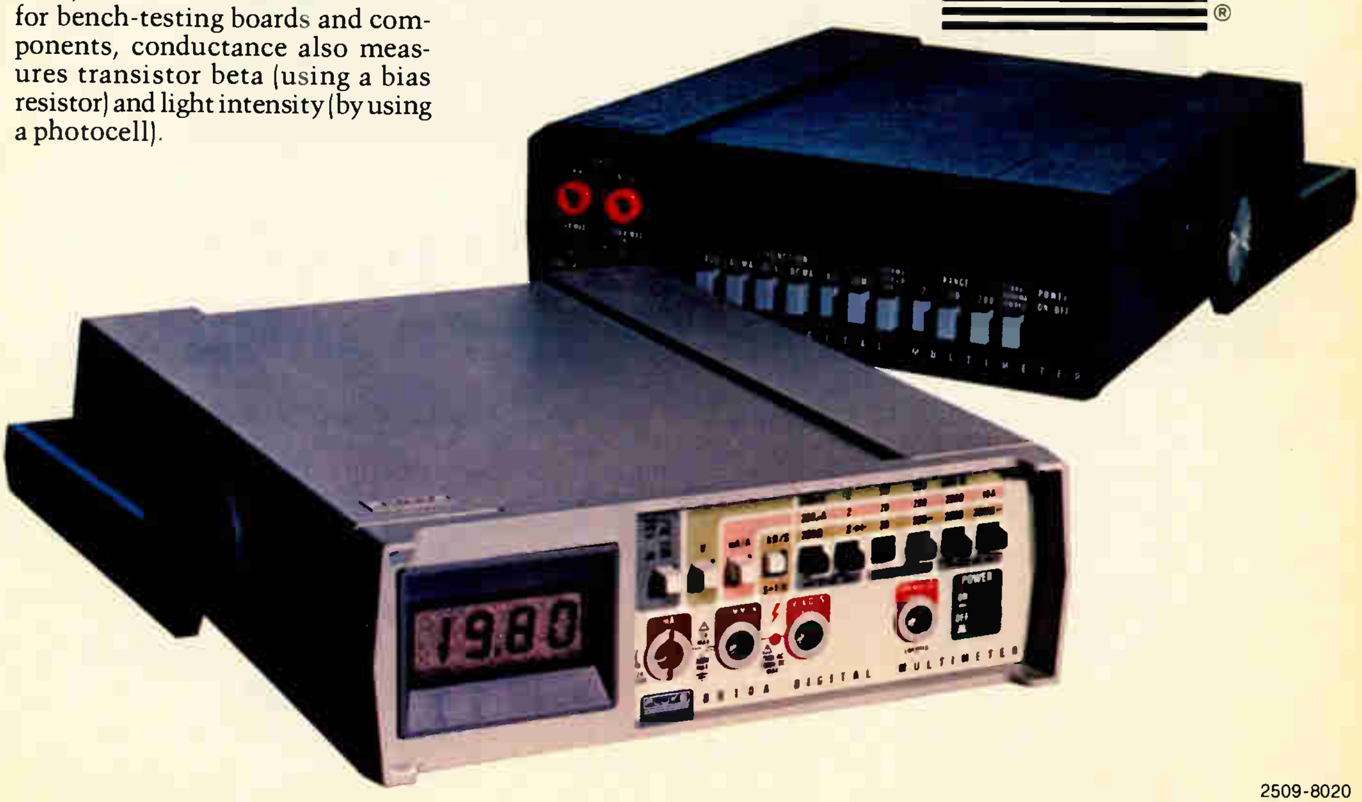

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Electronics

The International Magazine of Electronics Technology

Vol. 51, No. 21 • October 12, 1978

Highlights

Cover: 16-bit board works with 8-bit units, 105
The iSBC 86/12 16-bit single-board computer can execute the 8-bit instructions of its predecessor, as well as its own 16-bit set. Furthermore, it can address a megabyte of memory while working over the same system bus as the 8-bit boards.

Cover is by Gabor Kiss.

Everybody's talking Pascal, 81
The 10-year-old programming language, Pascal, has caught on of late and is proving itself a versatile tool for the microcomputer. An underlying factor is its portability.

Hook can be conquered, 111
Hidden printed-circuit-board capacitance, known as "hook," has been convicted of causing unexplained discrepancies in circuitry output. Now it is possible to trace, measure, and design out this effect.

Bird watchers' guide, 120
More than 55 active communications satellites are in geostationary orbit, and more soon will be launched. This handy pullout table summarizes the principal characteristics of the world's satellite programs.

And in the next issue . . .
Electronics' annual technology update . . . the 1978 achievement award.

Electronics

Publisher's letter

Blaise Pascal was a 17th century Frenchman for all seasons—a gifted mathematician, physicist, and cleric. His name is attached to a high-level programming language whose popularity is snowballing among designers and programmers of computers and microcomputers. Niklas Wirth, the Swiss who devised the language in 1968, dubbed it Pascal because he admired the Frenchman's versatility. Another admirer of both the man and the language is John Posa, our Microsystems and Software editor, who wrote the story on the spread of Pascal that begins on page 87.

As a design engineer who worked on intelligent-terminal development, John appreciates the virtues of Pascal. "It takes the best features and avoids the worst of languages like Algol, Fortran, and PL/1," he says. "Engineers need to learn high-level languages like Pascal because software costs are rapidly approaching 90% of total system costs. Efficient high-level languages will be absolutely essential for cost-effective and fast design.

"An ideal language would be totally comprehensible to anyone, and at the same time be as efficient as assembly code. I doubt if any one language will meet that ultimate definition, but Pascal has already proved its versatility."

Incidentally, this issue marks the debut of a newly established technical department under John's wing. As Microsystems and Software editor, he'll be watching applications of microcomputers from chips to boards, keeping an eye on development systems and other tools to aid engineers in designing microcomputers, and informing you of the latest developments in software.

A BSEE from the University of Michigan, John put in engineering stints with RCA Corp. and Ann Arbor Terminals. Despite what he has learned about high-level languages, he enjoys working with assembly code. "It's intellectually challenging," he says, "and I got reasonably efficient at it."

In this issue you'll find a comprehensive fold-out guide to existing and soon-to-be-launched communications satellites (p. 120). It's unique in that all the major operating parameters of interest to both system designers and potential users are collected in one place.

The guide was assembled by Wilbur L. Pritchard, president of Satellite Systems Engineering Inc. He founded the firm to provide consulting and systems engineering services to governmental agencies and private companies worldwide. He has been associated with communications and satellites for more than 30 years.

After 15 years at Raytheon Co., he became group director of communications satellite systems at Aerospace Corp. Then in 1967, he became vice president and first director of Comsat Labs at Communications Satellite Corp. He served as president of Fairchild Space and Electronics Co. from 1973 to 1974.

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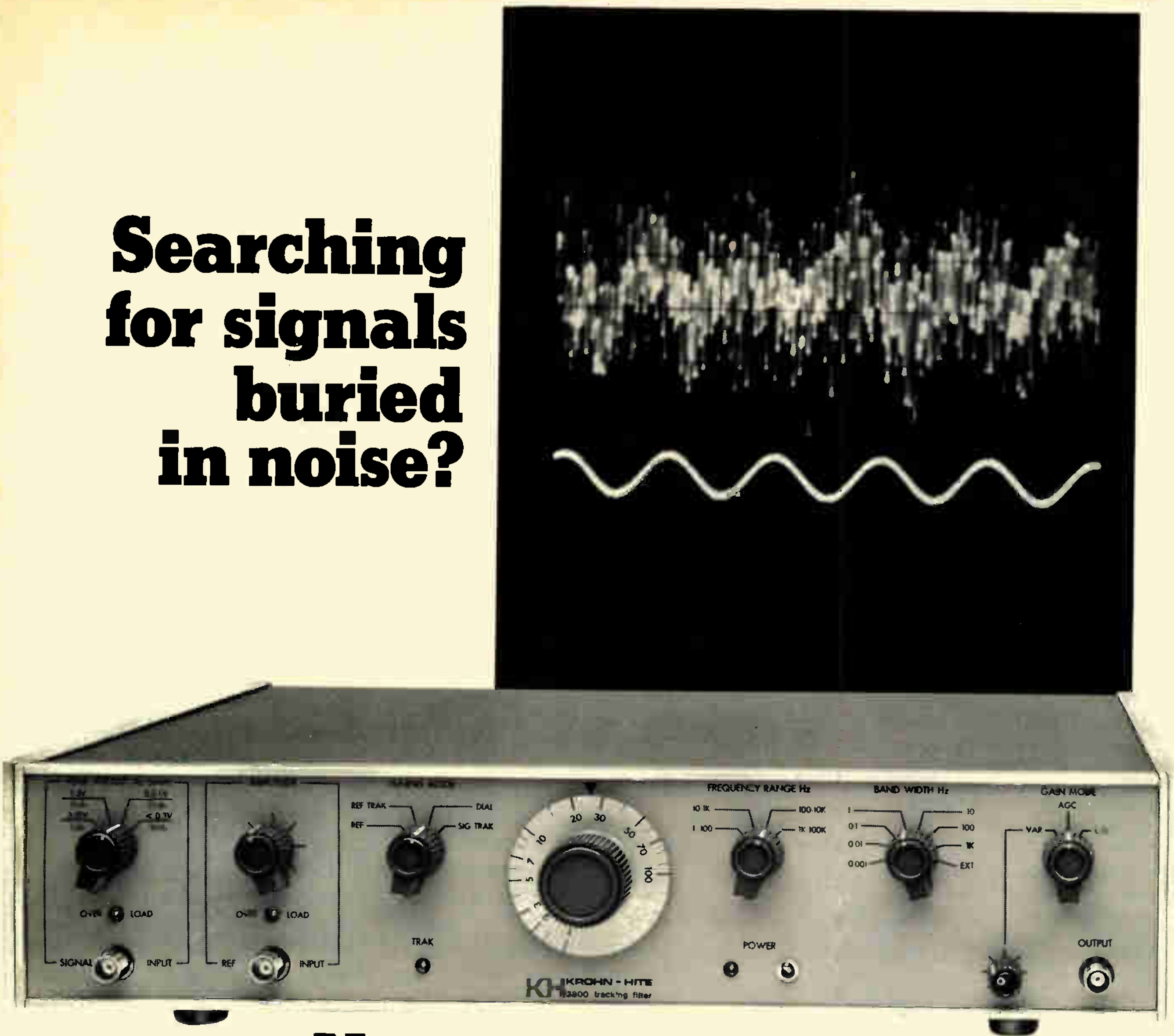

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Readers' comments

Beaten out

To the Editor: The Aug. 3 issue [Electronics Newsletter, p. 36] mentions the microprogrammability of Digital Equipment Corp.'s LSI-11 as "marking the first time a microprogramming option has been offered in a microcomputer." The Texas Instruments TMS 1000 has had that option since its introduction in 1974. It also has a programmable logic array with a mask-programmable output and is available in both p-channel and complementary MOS versions.

Betsy Donner
Texas Instruments Inc.
Houston, Texas

Not fast enough?

To the Editor: Part 2 of "How bit-slice families compare" [Aug. 17, p. 96] states that Advanced Micro Devices' Am2910 microsequencer "makes the 2909 and 2911 obsolete." This statement is misleading in view of the poor speeds of the 2910.

According to AMD's specs dated May 18, the next-to-longest data path is 100 ns (clock to Y_{out}) on instructions 8, 9, and 15. The longest data path has not yet been released; it occurs when prior instructions are 4, 12, or when RLD is low. The instruction selection time, I_0–I_3 to Y_{out}, is 70 ns. Compare these figures with the high-speed circuits you can design using the fast, flexible 2909/2911, whose longest data path (clock to Y_{out}) is 45 ns, with a select time (S_0–S_1 to Y_{out}) of 30 ns.

As for the appearance of second sources for National Semiconductor's 2901A-1 [Part 1, Aug. 3, p. 91], NEC Microcomputers Inc. announced samples of its 2901A-1 several months ago.

Max Baron
National Semiconductor Corp.
Santa Clara, Calif.

Look at the figures

To the Editor: On page 96 of your Aug. 31 issue ["They're off and running at the IEEE"], you quote Irwin Feerst as saying that the Institute of Electrical and Electronics Engineers "denudes itself in [certain] areas, such as pensions, anti–wage busting, and the problems of age bias and alien engineers." The budget of the institute's U. S. Activities Board for 1977 and 1978 indicates otherwise.

Increasingly more resources are being allocated by the USAB to achieve positive results in these areas, as well as in others affecting our members. For example, in 1978 we boosted the budget for pension activity to $66,000 from $30,000 in 1977. Similarly, the budget to combat wage busting was increased to $30,000 from $25,000, and the one to fight age discrimination to $50,000 from $15,000. Since 1973, no funds have been provided for looking into the question of alien engineers. At the moment, no real basis exists for implying that this is a problem for the IEEE membership.

Bruno O. Weinschel
U. S. Activities Board
Institute of Electrical and Electronics Engineers
New York, N. Y.

Poor audio quality is no excuse

To the Editor: I differ with the statement by Mr. Davis in the Aug. 31 issue [p. 6] in which he blames the poor programming of domestic a-m radio on its less than desirable audio quality. For refutation, one only has to listen to international shortwave broadcast stations, which, in spite of an octave-narrower bandwidth and more severe fading and interference problems, have higher-quality music programming than do domestic a-m stations.

James Long
Pasadena, Calif.

Clarification

The output-power comparison in the Aug. 17 International Newsletter (p. 63) for single-mode laser diodes from Standard Telecommunications Laboratories Ltd. and Mitsubishi Electric Corp. is misleading. Performance figures from STL are for a laboratory device; those from Mitsubishi are for production devices. The Japanese firm says its laboratory devices have achieved three times the output power of its production diodes.

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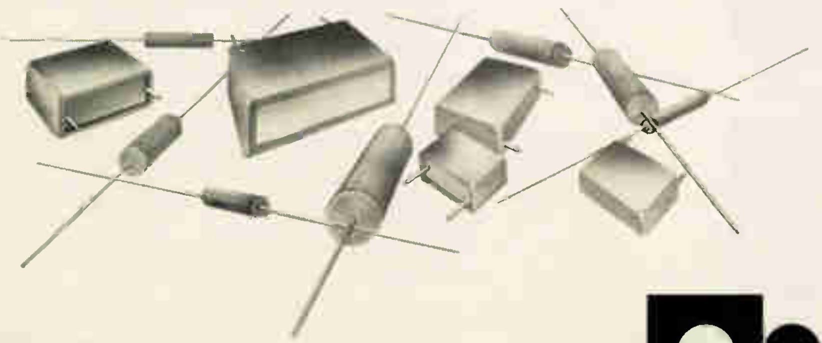

News update

■ The military services hope this month to establish a beachhead in their latest efforts to obtain a new battlefield telephone exchange system. The reason: Conrac Corp. of Stamford, Conn., is making initial delivery of a Visual Display Unit for the tri-service Unit Level Circuit Switch program [*Electronics*, Nov. 25, 1976, p. 35].

The Visual Display Unit that Conrac is designing and developing consists of a 14-inch raster-scan cathode-ray-tube display, as well as an alphanumeric generator and an interface to the system's computer. It displays 2,000 alphanumeric characters as 25 lines of 80 characters each. The unit is to be used both in the communications operation and as a device for troubleshooting and maintaining the all-digital tactical telephone switching system.

Conrac's Systems-West division in Duarte, Calif., is managing the Visual Display Unit program under a $250,000-plus contract from International Telephone and Telegraph Corp.'s Defense Communications division in Nutley, N. J., which is prime contractor for the AN/TTC-42 system. According to a Conrac spokesman, options to the firm's contract are valued at $1.2 million.

■ The military's interest in fiber-optic technology is reaching new heights. For example, the Air Force, which has concentrated its fiber-optic systems developments on data buses for signal transmission in aircraft [*Electronics*, Aug. 5, 1976, p. 83], now plans to test optical waveguides in outer space.

The Air Force Weapons Laboratory at Kirtland Air Force Base in New Mexico recently advised Corning Glass Works that a long length of waveguide fiber from the Corning, N. Y., firm, will be exposed to space environment. Scheduled for a space shuttle launch in March 1980, the experiment will last 6 to 12 months and determine how optical waveguides and other electro-optical items are affected by the radiation in the Van Allen belts and space's temperature extremes. **Bruce Le Boss**

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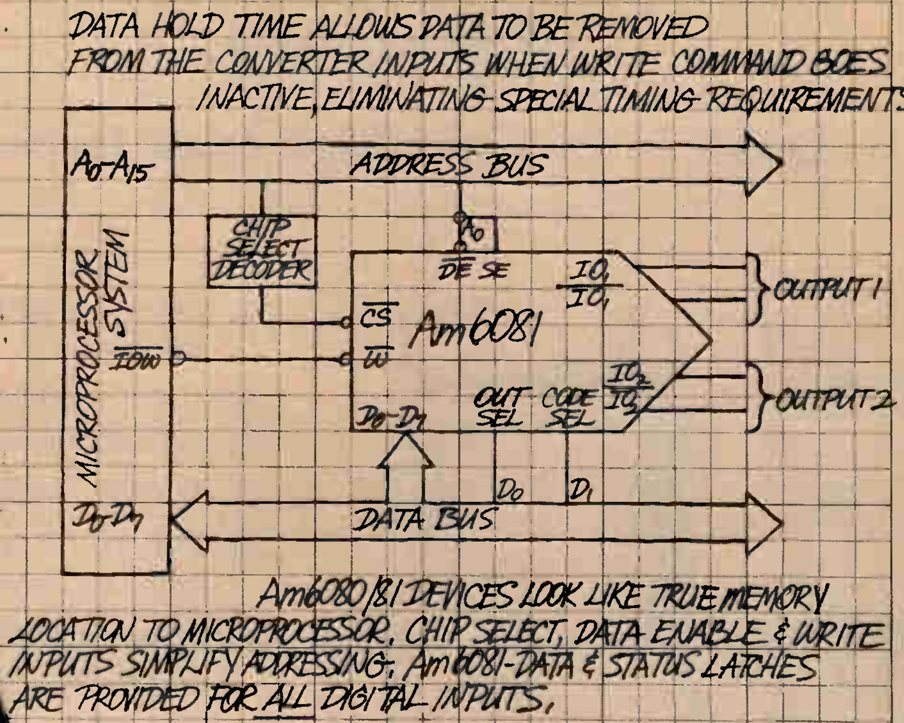

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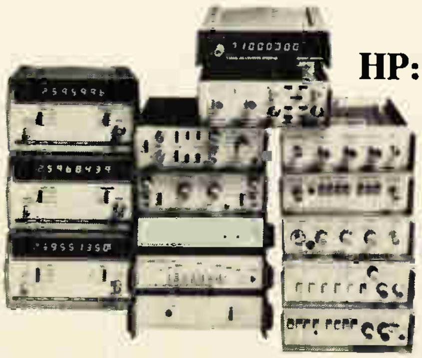

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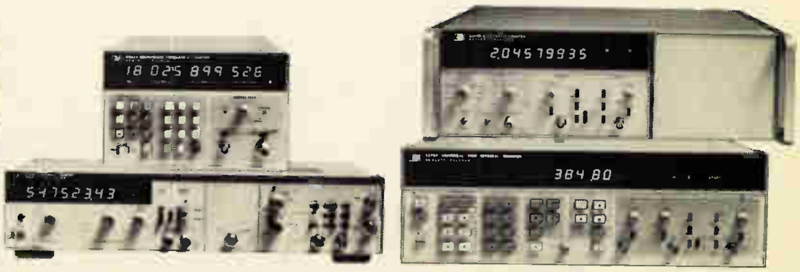

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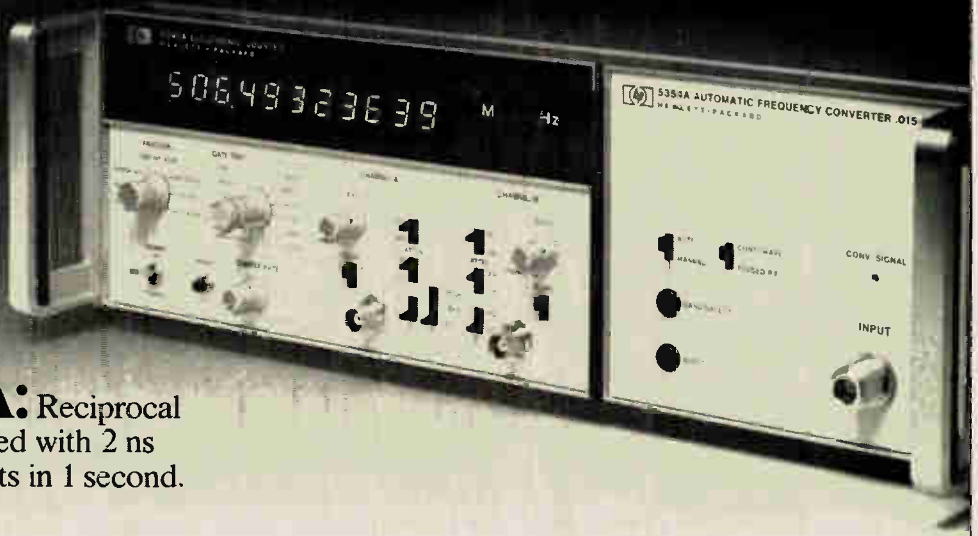

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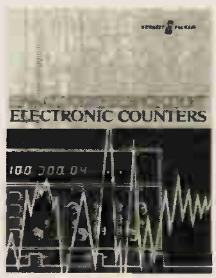

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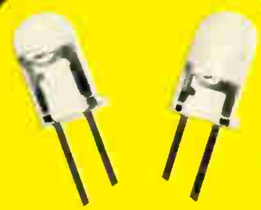

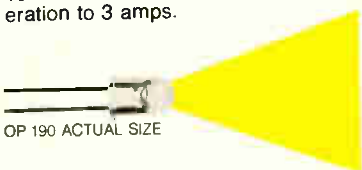

People

Litton's Bridge sees LSI as key to technology transfer

Builder. Charles Bridge is guaranteeing technology flows among Litton's divisions.

Ensuring a technology fallout from divisions doing state-of-the-art work into more settled commercial product areas is tough for big diversified companies, which are often geographically scattered. Solutions vary from institutionalized departments to informal charts. Now Litton Industries is opting for a middle course. It has named 53-year-old Charles S. Bridge its new chief scientist and charged him with spurring what president Fred W. O'Green calls "communication of ideas and technology transfer."

How does the veteran manager of inertial navigation development programs see his task? Not surprisingly, he answers: "It's digital LSI that's the key to the whole effort." Bridge is convinced of the value of keeping close tabs on what the semiconductor industry has to offer, partly because of his training as a physicist and partly as a result of his experience since joining Litton in 1959 in putting ever improving semiconductors to work in navigation systems. And he commands a lot of attention from semiconductor makers, being in such a visible position at a big device user (more than $2 billion of Litton's nearly $4 billion in sales come from electronic systems and equipment).

Indeed, Bridge says his role in counseling divisions puts a premium on looking at devices as a user. "We're systems people, not circuit designers," he says, "so we have to look at the bigger picture of how things work." In regard to the relationship, "the industry is very responsive to our needs, but they can't do everything." So Litton spends a lot on its own device research and development, "to keep pace with the latest developments and to see what's coming."

As Litton policy dictates, Bridge is not building a corporate staff. Instead he uses outside consultants freely, picks bright scientific staffers from divisions for specific help on projects, and pitches in himself. A pitfall so far is that "some division people want me to be a policeman, beating on so-and-so to deliver those RAMS."

Most recently a vice president of business development for Litton's Defense group, Bridge pronounces himself enthusiastic about the new job, where he "has free rein." In fact, president O'Green (who himself is an engineer) follows technological matters so closely that "he says I have the best job in the company, but so far he hasn't offered to trade with me."

Boschert's Jordan calls power supplies the last frontier

After heading the Honeywell team that helped engineer the first practical dynamic random-access memory for memory systems and then, as founding manager of Intel Corp.'s Memory Systems division, producing a mass market for them, what brings William F. Jordan to Boschert Inc., a maker of switching power supplies? "I like the idea of a new venture," declares the firm's new vice president of engineering.

"Designing switching regulated power supplies still is a complex process," for which "we'll have to use all the skills we've acquired," he says. In his new post, he will direct Boschert's technological attack on the entrenched linear power supplies by trying to beat them on cost, efficiency, and size [*Electronics*, March 16, p. 14]. Tracing the increasing integration of logic and memory

AMI's 6800 GOES TO EXTREMES.

From −55° C to 125° C. Our military temperature range 6800 microprocessors work in the most hostile environments. And at −40° C to 85° C, our industrial versions hold their own too. We even have 1.5 and 2 MHz high-speed 6800s. Today, manufacturers in just about every industry from cars to computers are specifying the 6800. And AMI, a pioneer in MOS/LSI circuits, is making them. With plants in California, Idaho and Korea, we're geared to handle any size order. And we'll go to extremes to get it to you quickly.

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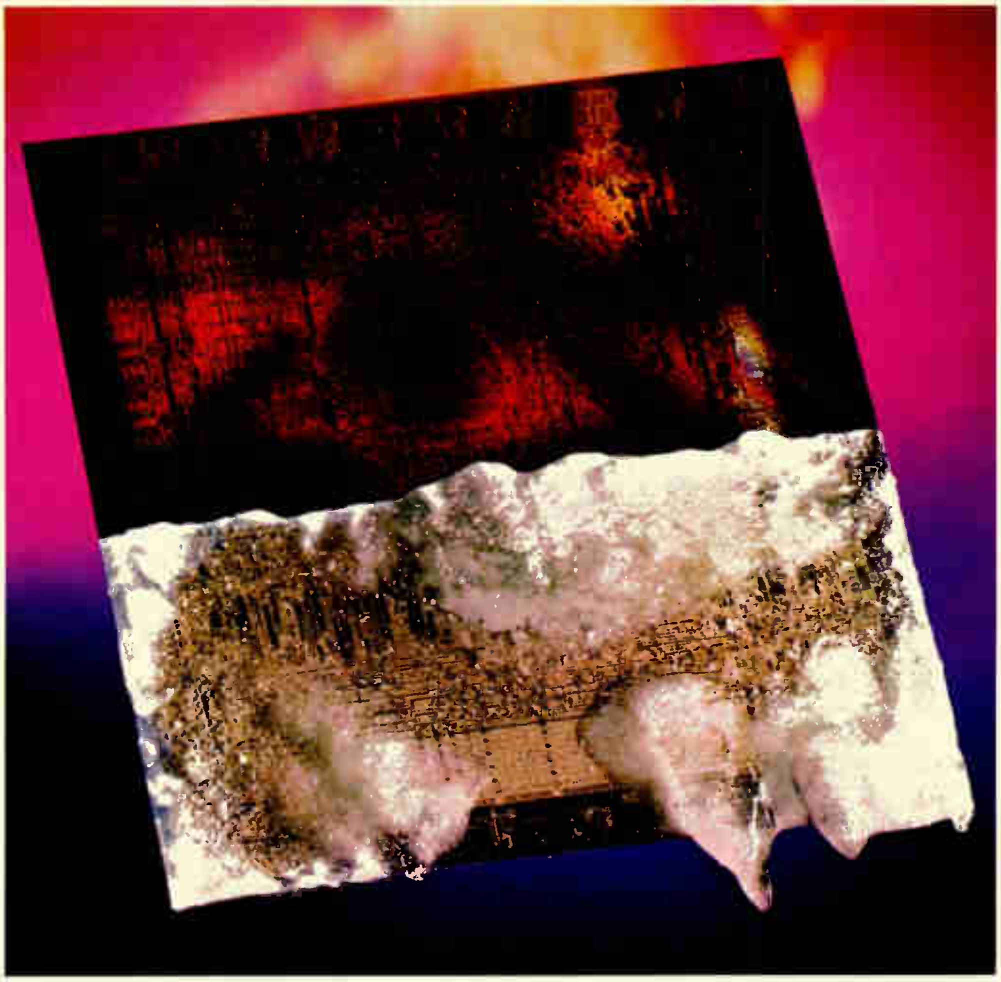
The AMI S6800 MPU comes with a whole family of memories and peripheral circuits. They include the S6810 128 x 8 static RAM, the S6820 and S6821 PIAs, the S6831 16K static ROM, the S6834 512 x 8 EPROM, the S6850 ACIA, the S1883 UART and the S2350 USRT. And we offer a range of memories, from high-speed VMOS RAMs to low power CMOS.

The 6800 is designed like a minicomputer, so it's simpler to program than the 8080. Especially with our Microcomputer Development Center, which can cut programming time from hours to minutes. It includes a very smart CRT with full debug software, a flexible text editor, a macro-assembler and a built-in PROM burner. A powerful 40-channel Logic Analyzer lets you choose your own layout and format, and modify programs instantaneously.

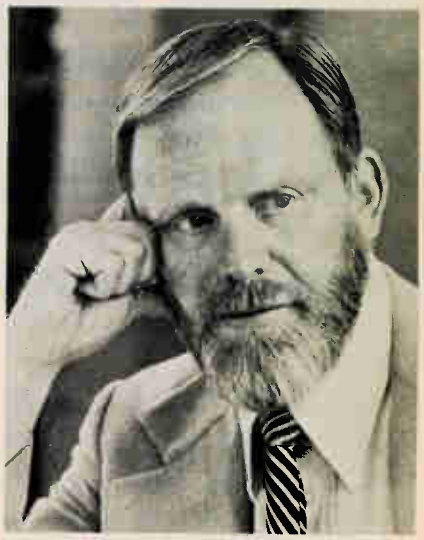
Want to learn more about our 6800 family? Contact your nearest AMI distributor or write to AMI Marketing, 3800 Homestead Road, Santa Clara CA 95051. Or call (408) 246-0330.



AMI

AMERICAN MICROSYSTEMS, INC.

Circle 15 on reader service card



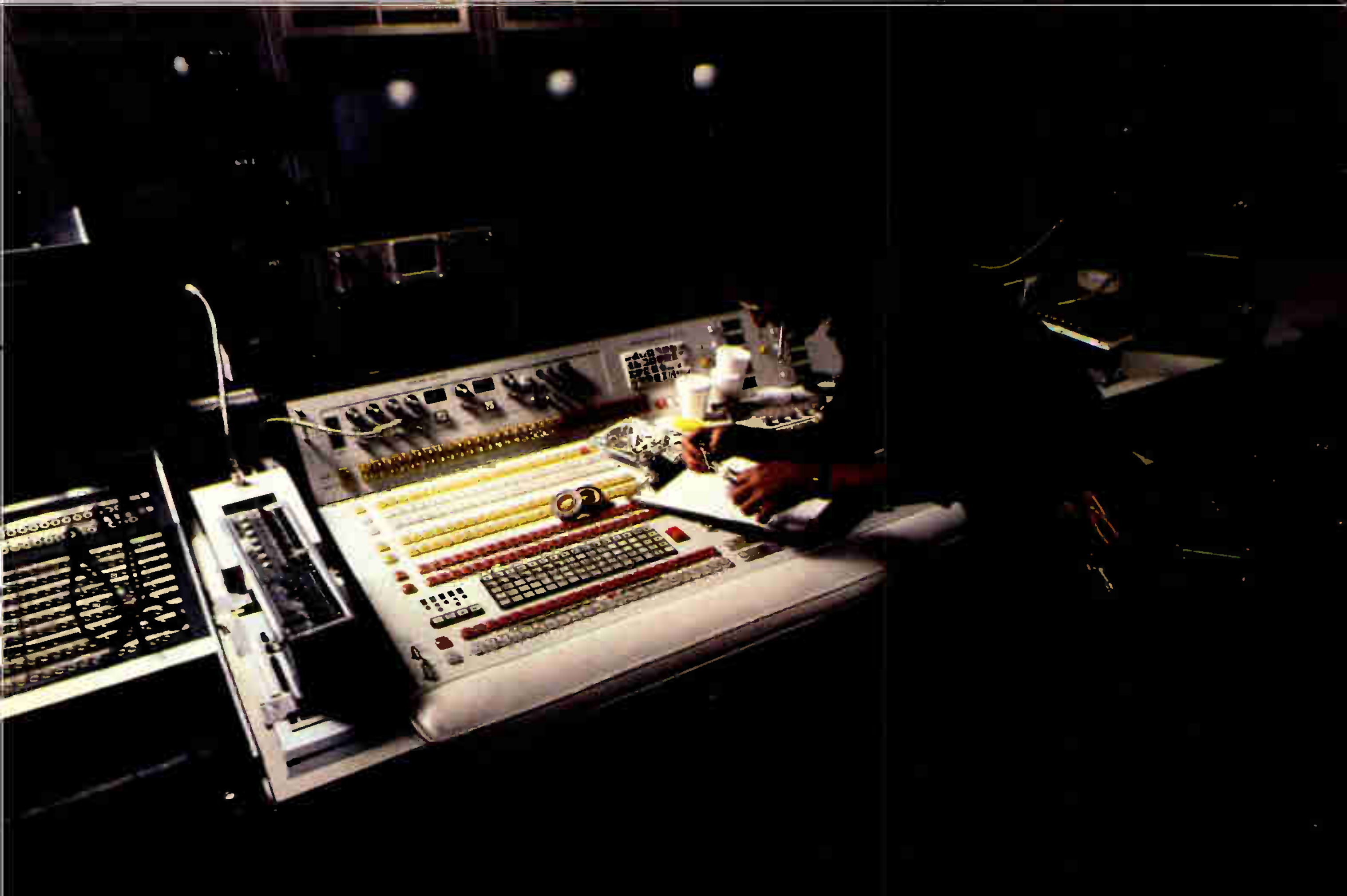
Explorer. William Jordan likes the challenge of power supplies and company management at his new employer, Boschert Inc.

components, he thinks that "now power supplies are the last frontier of circuit development."

"The real challenge is to design circuits with the fewest parts," says Jordan. Though it makes no sense to integrate higher power levels, he believes that lower-power circuitry could be integrated, such as portions of the logic signal circuitry. Jordan names two particularly challenging areas in switching power supplies: the feedback amplifiers that must zero out error signals; and the magnetic component modeling to get low-cost transmission and inductors.

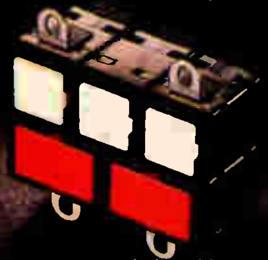
Acknowledging that power supplies are not a glamorous part of the industry, Jordan answers, "That's one of the things that make it a neat business." He says, "My contribution at this stage of my career is on the management end of things" by guiding good circuit designs and rejecting bad ones.

Jordan is well prepared to head out toward his last frontier. After getting his BSEE degree in 1956 from Worcester Polytechnic Institute, Jordan worked for CBS Electronics and Avco's R&D division before joining Honeywell's Computer Control division, where he spearheaded development of the 1103 RAM. In 1971, he became founding manager of Intel's Memory Systems division and corporate vice president. □



You may not know how expensive a pushbutton really is until months after it's paid for.

The true measure of a pushbutton's cost isn't so much what you pay. It's how many times you pay it.



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No matter how many words you use to describe the broad AML lineup, it all comes down to just two: cost effectiveness. For a panel that's pleasing to the eye as well as the budget.

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Circle 17 for Data

From CPU to software, It's the beginning of a new

Intel's new 16-bit microcomputer is here. It's the 8086, designed to deliver ten times the processing power of our 8080.

More important, right now you can get CPU, memory, peripherals, software, development tools and design assistance. We've made MCS-86™ the most comprehensive microcomputer system ever introduced.

Our challenge was to build the most advanced 16-bit microcomputer. And to give 8080 and 8085 users a direct upgrade path. We accomplished it. The 8086 is the world's most advanced microprocessor. Yet it's a direct evolution of our 8-bit 8080 and 8085. It's software-compatible with both, supporting all their instructions in addition to its own advanced instructions. And the 8086 utilizes readily available Intel microcomputer peripheral chips and low cost, standard MOS memory.

8086 is an architectural triumph, etched in HMOS. The standard 8086 delivers 5 MHz speed. And it delivers direct addressability to a full megabyte of memory, with both 8-bit and 16-bit signed or unsigned multiply and divide in hardware. It gives you efficient byte-string operations and improved bit manipulation. Plus it provides capabilities never before supported by a microprocessor, such as dynamic relocation, reentrant code, position-independent programs and instruction look-ahead.

All in all, 8086 sets a new standard for microcomputer processing capabilities.

We designed MCS-86 for design flexibility. It can operate on a full set of 16-bit registers, or on an 8-bit subset which corresponds to the 8080 register set. That makes MCS-86 adaptable to traditional 8-bit applications as well as larger, more complex applications.

A minimum MCS-86 configuration includes only the CPU, the 8284 Clock Generator, two 8282 Octal Latches, 2K bytes of 2142 RAM and 4K bytes of 2716 EPROM.

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For easy expansion, add our 8288 Bus Controller, which generates Multibus™ timing signals. And, using our 8286/8287 Octal Transceivers, MCS-86 interfaces with larger, buffered systems.

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Circle No. 19 for more information

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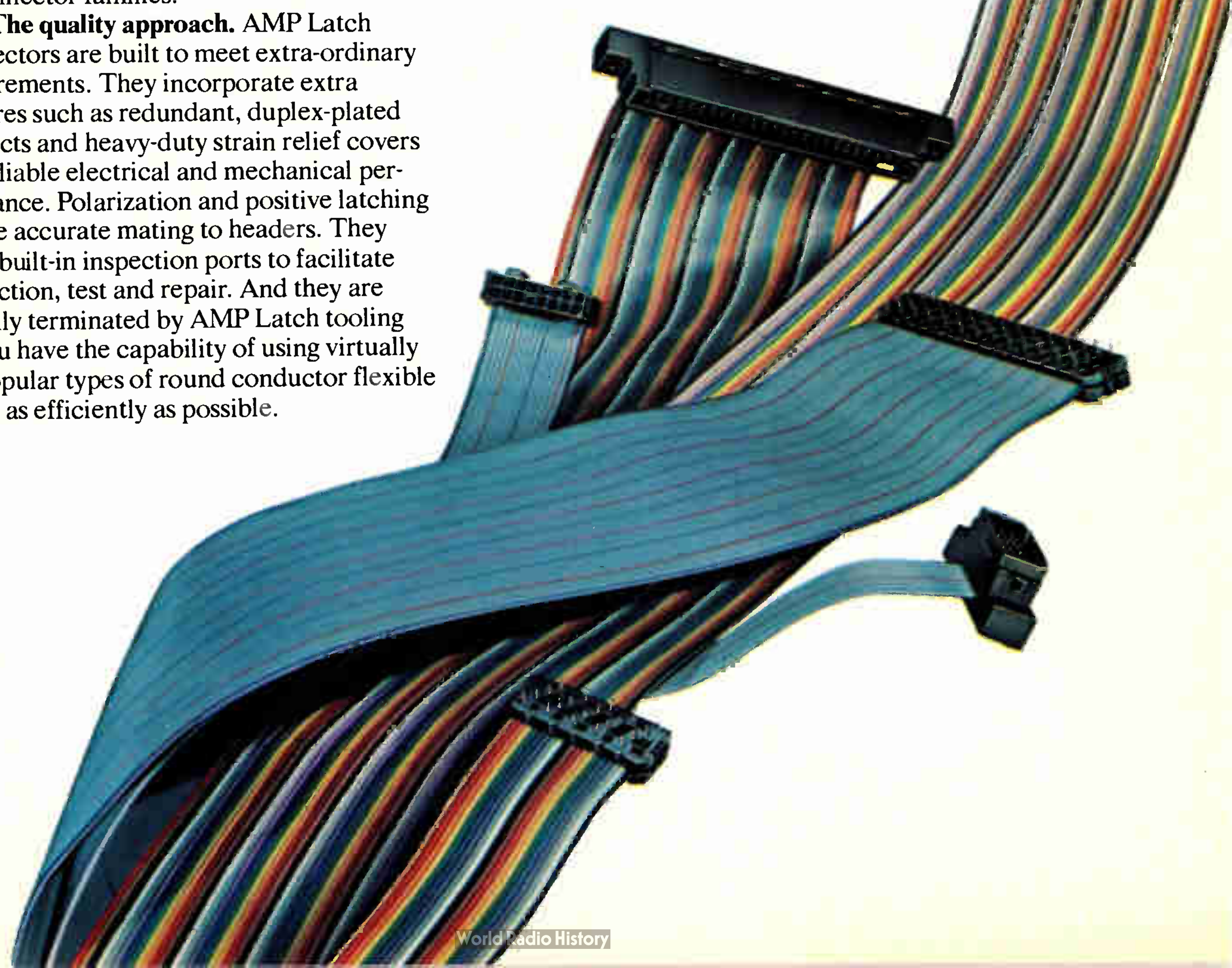
Too many times you may select a connector that does the job—but that's all it does. You can't expand with it. With AMP Latch connectors we make sure that won't happen.

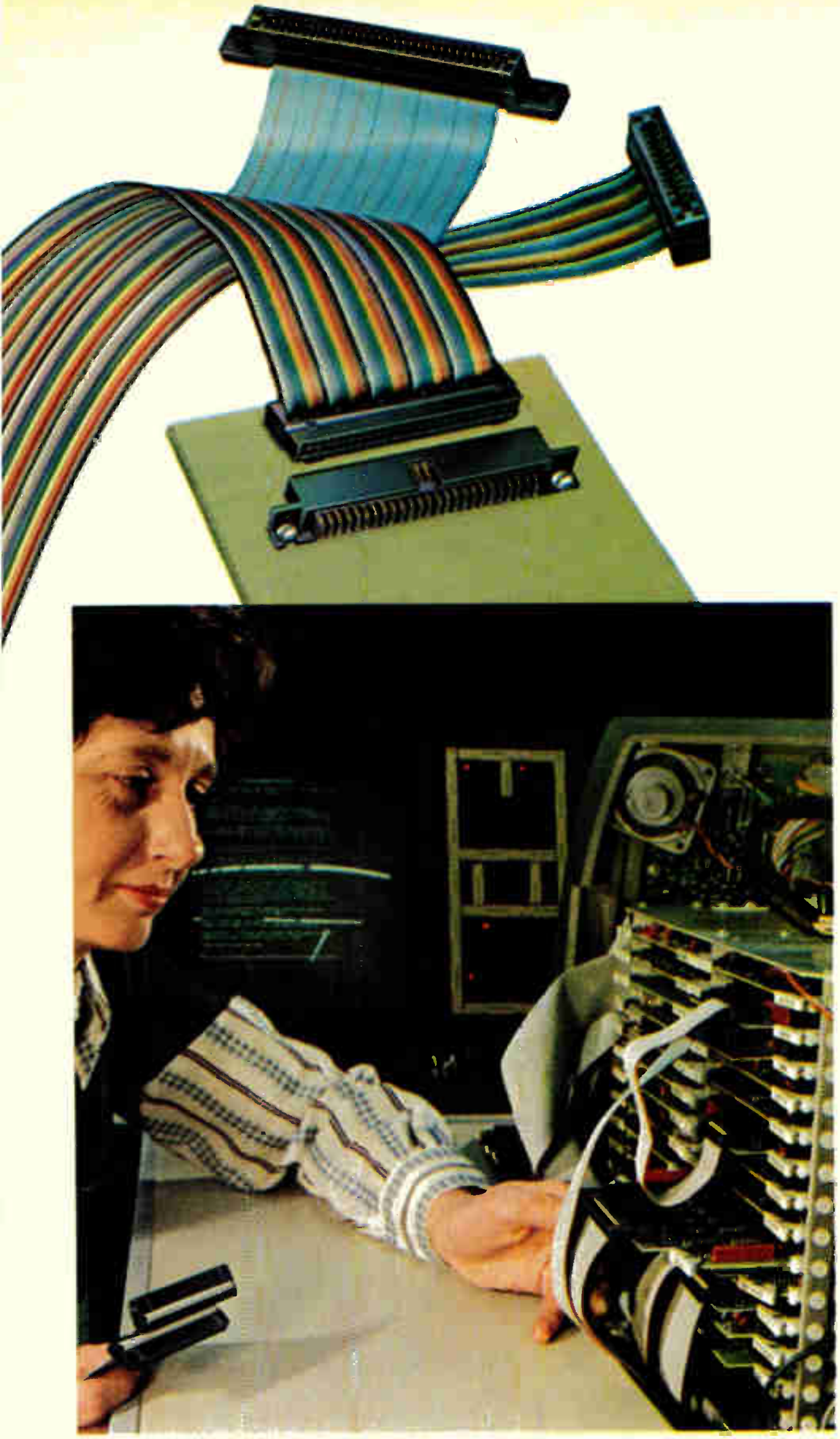
The complete approach. Every AMP Latch connector is designed as part of a larger approach to packaging. For example, AMP Latch is available in cable-to-cable, edge card, DIP and receptacle connectors. And it works with twisted pair cable, round conductor ribbon cable and round conductor bonded cable. In addition, it mates with the full range of AMPMODU headers including standard right angle and feed-thru types, as well as header barriers for mixing a variety of connector families.

The quality approach. AMP Latch connectors are built to meet extra-ordinary requirements. They incorporate extra features such as redundant, duplex-plated contacts and heavy-duty strain relief covers for reliable electrical and mechanical performance. Polarization and positive latching assure accurate mating to headers. They have built-in inspection ports to facilitate inspection, test and repair. And they are quickly terminated by AMP Latch tooling so you have the capability of using virtually all popular types of round conductor flexible cable as efficiently as possible.

The AMP approach. Of course, AMP Latch connectors, and all AMP products, are backed by AMP technical service. Not just ordinary service, but the kind that says we'll help you with system design. Application tooling. Training your people. And more.

We invite you to find out more about AMP Latch and the AMP approach. Just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.





AMP has a better way... Mass Termination.

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We have mass termination connectors for discrete wire and virtually any type of cable: ribbon coaxial, flat etched, twisted pair, round conductor, flat flexible. All have preassembled contacts, eliminate costly wire preparation and offer productivity savings and benefits never before possible.

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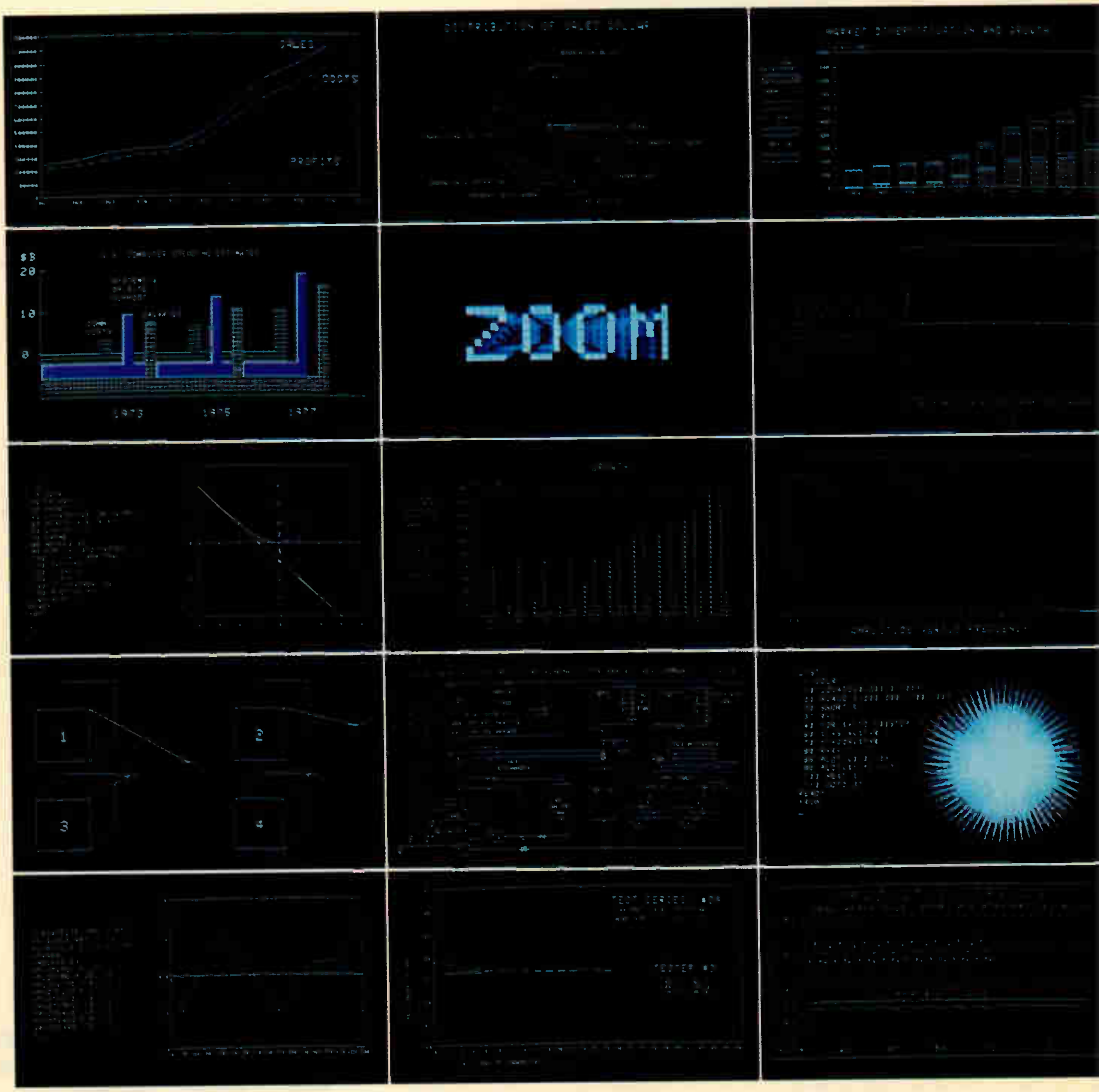
Circle 21 on reader service card

Graphics. Without



graphics software.

You just lost your last excuse for sticking with phanumerics. Because with HP's new 2647A Intelligent raphics Terminal, you get graphics without digging to your CPU's software.

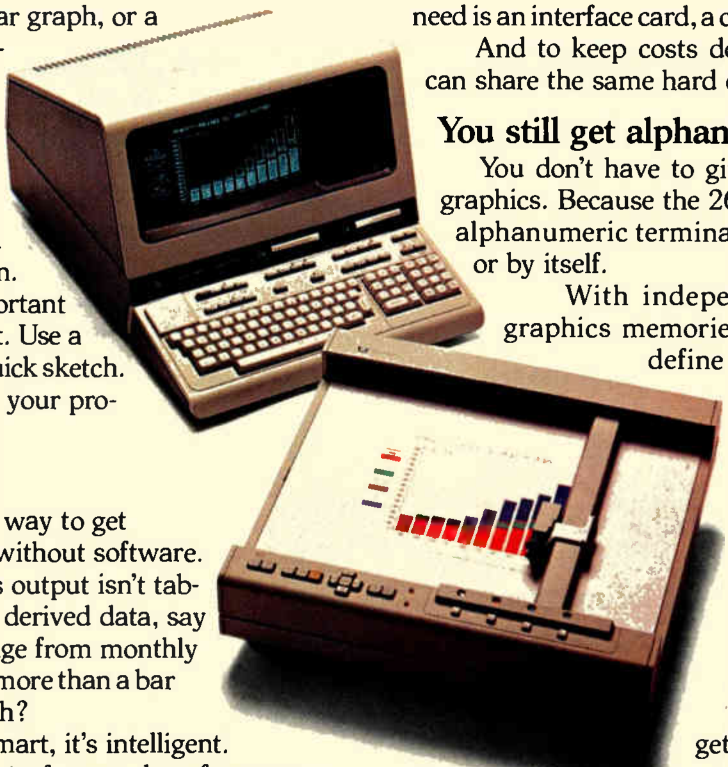
picture's worth a thousand numbers.

On an alphanumeric terminal, your data's just a reen full of numbers. But with the 2647A you ın plot tabular data as a bar graph, or a e chart, or a linear or loga- :hmic line graph. Quickly, ith just a few keystrokes.

Now you can really see ›ur data, not just look at it.

What's more, with the 547A you can zoom in and ıt. Pan right, left, up, down. ·lectively erase. Shade important eas to make them stand out. Use a ıbber-band line to make a quick sketch.

Without any help from your pro- ·amming department.



's more than smart.

The 2647A's the smart way to get aphics from tabular data without software.

But what if your CPU's output isn't tab- ar? Or if you'd like to plot derived data, say three-month moving average from monthly les figures? Or if you need more than a bar aph, pie chart or line graph?

The 2647A's not just smart, it's intelligent.

You can program it to reformat data from your PU, or to compute more data, in easy-to-write BASIC. nd you can program it in AGL, our high-level graphics nguage extension of BASIC. Its powerful commands, ıch as FRAME, AXES, LABEL, LOCATE and PLOT, ıt sophisticated graphics at your fingertips.

Either way, your program runs on the 2647A without any help from your CPU.

Hard copy's easy.

How do you get graphics into your briefcase?

The 2647A makes graphics as portable as alpha- numerics. It interfaces easily with our 9872A Four-Color Plotter (which can even make overhead transparencies), and with our 7245A Thermal Plotter-Printer. All you need is an interface card, a cable and the peripheral itself.

And to keep costs down, more than one 2647A can share the same hard copy peripheral.

You still get alphanumerics.

You don't have to give up alphanumerics to get graphics. Because the 2647A's also a programmable alphanumeric terminal for interactive use on-line or by itself.

With independent alphanumeric and graphics memories. Eight soft keys you can define to do several steps with a single keystroke. A bright, easy-to-use, high resolu- tion display. And built-in dual cartridge tape drives for 220K bytes of mass storage.

Best of all, the 2647A with full memory and data communications interface costs only $8300.*

Which makes it easy to get the picture.

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Circle 23 on reader service card

Watching the spectrum slip away

If someone in the United States fails to get excited about it soon, this country is liable to have a great deal of spectrum space pulled out from under it. That is what could happen next year at WARC—the World Administrative Radio Conference—to be held in Geneva under the auspices of the International Telecommunications Union. WARCs are held every 20 years, so that the agreements drawn up in 1979 will literally tie down the spectrum until 1999.

The key question in Geneva will be: who gets what frequencies and for what purpose? Everyone manages to dip an oar into the sea on that one: from radio astronomers, who resent the interference of satellite transmissions, to manufacturers of mobile communications equipment, who need frequency space to keep up with the demand for their services, and satellite users, whose need for spectrum seems inexhaustible. The political, social, technical, and, perhaps most important, economic issues involved are complex. And that is where the U. S. and the rest of the developed nations are threatened.

WARC's one-nation, one-vote governing concept gives the smaller, less developed nations the same input and impact as the larger, more technologically advanced ones. The arrangement could hurt the heavy spectrum users that need the space and are not anxious to share it. For their part, the developing nations claim that they are ready for their share of the spectrum pie and also need it for their own development.

But that's not all. It has been proposed that rent be paid for the use of geosynchronous orbit positions, with unused frequencies assigned to the less developed nations for rent to those who need them. Such a fund-raising procedure brings up the basic question of whether orbit position and frequencies can be owned by any one nation.

Against this background, there is concern that the U. S. position will be weak because of inadequate funding, insufficient time spent on preparation, and less than complete understanding of all the aspects of all the issues involved. The Senate's Commerce, Science, and Transportation communications subcommittee, for one, is "deeply disturbed." Prof. Glen Robinson of the University of Virginia, who is to head the U. S. delegation to Geneva, will not be able to work full time on WARC until mid-1979—just before the meeting. Getting to the core of the problem, Sen. Harrison Schmidt (R., N. M.), a former astronaut, has proposed that the one-nation, one-vote concept be replaced by a user-based organization geared to use and need rather than "nationalistic and political considerations."

Certainly the WARC delegation will not be able to reach fair and sensible agreements unless the central position of telecommunications in our society is realized. There must be a great deal of preparation to safeguard legitimate national interests. It seems clear that there should be broad Government, industry, professional society, and public debate, and it should start now. Next year will be too late.

Meetings

Engineering in Medicine and Biology, IEEE, Marriott Hotel, Atlanta, Oct. 21–25.

Fourth International Conference on Digital Satellite Communications, IEEE Canadian Region, Queen Elizabeth Hotel, Montreal, Oct. 23–24.

Conference on Fiber-Optic Markets, Kessler Marketing Intelligence (Newport, R. I.), Sheraton Islander, Newport, Oct. 23–24.

Eleventh Annual Connector Symposium, Electronic Connector Study Group Inc. (P. O. Box 1428, Camden, N. J. 08101), Cherry Hill, N. J., Oct. 25–26.

Military Microwaves 78 Conference and Exhibition, Microwave Exhibitions & Publishers Ltd. (Sevenoaks, Kent, England), The Wembley Conference Centre, London, Oct. 25–27.

Intelec—International Telephone Energy Conference, IEEE, Sheraton Park Hotel, Washington, D. C., Oct. 25–27.

Annual Test Conference, IEEE, Cherry Hill Hyatt House, Cherry Hill, N.J., Oct. 31–Nov. 2.

CEC '78—Fourth International Symposium on Computers, Electronics, and Control, IEEE, Toronto Hilton, Toronto, Nov. 1–3.

Workshop on Electromagnetic Interference, National Bureau of Standards, Gaithersburg, Md., Nov. 2–3.

1978 Chicago Fall Conference on Consumer Electronics, IEEE, Ramada O'Hare Inn, Rosemont, Ill., Nov. 6–8.

12th Annual Asilomar Conference on Circuits, Systems, and Computers, IEEE, Asilomar Hotel, Pacific Grove, Calif., Nov. 6–8.

Fifth Annual Computer Security Conference and Exhibition, Computer Security Institute (Hudson, Mass.), Statler Hilton Hotel, New York, Nov. 6–8.

Introducing Mostek's 3876 and a new ISE age.

Mostek's 3876 is the newest member of Mostek's 3870 single-chip microcomputer family. To the designer, this family opens a new dimension in system design. The reason: Mostek's In-Socket Expandability (ISE-1™) concept.

ISE-1 means that any 3870 device may be replaced with any other 3870 family member *in the same socket* without hardware redesign. Start with a 3870. Need more RAM? Switch to a 3876. Need more ROM and RAM? Plug in a 3872. Expansion only requires exchanging one 3870 device for another.

The result is complete system flexibility with minimum investment in new designs. And there are more 3870 family members coming. The 3873 serial I/O version will interface to devices such as terminals, shift registers, and CCD memories.

Mostek also offers complete development support ranging from single cards to a complete floppy-disk system with an Application Interface Module (AIM™-72) for real time in-circuit emulation.

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Mostek's 3870 Family

	ROM	RAM	I/O	POWER
MK3870	2048x8	64x8	32	+5V
MK3872	4032x8	128x8	32/30*	+5V
MK3876	2048x8	128x8	32/30*	+5V

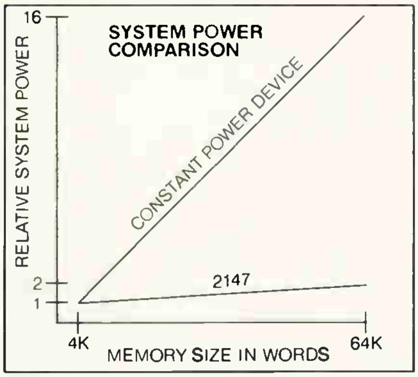
*WITH STANDBY POWER MODE OPTION

MOSTEK

Intel's 2147 is with volume availability


Intel's 4K static RAM, the 2147, is the industry standard for high speed, low power memory design, delivering access times to 55ns with traditional MOS economy. Now there are new military and even lower power versions, too. And all 2147 components are available now to support volume production.

From the start, designers have been attracted to the 2147's low active power dissipation and automatic power down on deselection. In stand-by mode, the 2147 can dramatically reduce overall power consumption compared to systems where all components dissipate constant power. It allows you to substantially simplify design of cache, fast buffer, control store and even large main memories. And since we've widened supply tolerance from ±5% to ±10%, design is easier and even more economical.



Now our new 2147L low power version takes you a step further, with maximum standby current of just 10 mA—about 1/10th that of bipolar 4K static RAMs.

There is a new military version, too, manufactured in total compliance with MIL-STD-883B, Level 5004 and 5005 specifications. It gives you 2147 performance over the full mil temp range and is offered in three levels of product assurance: Level B, Level C and Extended Temperature Range.

here in force, and two new versions.

HMOS is the key to the 2147's high producibility, high speed, high reliability and low power. It's the high performance technology we pioneered with our 2115A/2125A 1K static RAMs. And it has led to such dramatic advances as our 8086 16-bit micro-computer. We've delivered millions of HMOS devices, a proven track record of volume availability.

	2147	2147L	2147-3	M2147
Max. Access Time (ns)	70	70	55	85
Max. Active Current (mA)	160	140	180	180
Max. Standby Current (mA)	20	10	30	30
Operating Temperature Range (°C)	0-70	0-70	0-70	−55 to +125

HMOS means reliability, too. We've already matched the dependability of our long-time standard 1K static RAM, the 2102A. Get the details in our comprehensive Reliability Report #18.

The 2147 uses the widely accepted 18-pin, 4K x 1 standard pinout. It's fully static and can be used in both clocked and unclocked systems. All versions are directly TTL compatible in all respects: inputs, outputs and operation from a single +5V supply.

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Circle 29 on reader service card

Model	No. of Digits.	DC Volts	AC Volts	True rms AC	OHMS	Programmable Parallel	GPIB	Auto-Range	MP Based	AC/AC Ratio	Basic DC Accuracy	Base Price (U.S. List)
2000	3½	★	★		★						0.5%	$ 199.50
2100	3½	★	★		★						0.25%-1yr.	$ 249.00
4200	4½	★	★		★						.05%-1yr.	$ 399.00
4324†	4½	★	★		★						.01%-6mo.	$3,295.00
4600	4½	★	★		★			★			.01%-6mo.	$ 549.00
4800	4½	★	opt.	★	opt.	★		★			.01%	$2,995.00
5000	5½	★	opt.	★	opt.	★	★	★			.005%	$ 995.00
5100	5½	★	opt.	★	★			★			.0025%	$ 995.00
5900	5½	★	opt.	★	opt.	★	★	★			.001%	$2,195.00
5940	5½	★	opt.	★	opt.	★	★	★		★	.001%	$3,695.00
6000	6½	★	opt.	★	opt.	★	★	★	★	★	.001%	$2,995.00
6900	6½	★	opt.	★	opt.	★	★	★			3PPM	$3,495.00

† MIL-Spec

Tomorrow has arrived.

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	250 ohms to 10 megs		Modified Log CW (A) or CCW (B)			
Cermet	100 ohms to 5 megs	±10%	Linear (U)	2.0 Watts at 70°C	1.0 Watt at 70°C	2.0 Watts at 70°C
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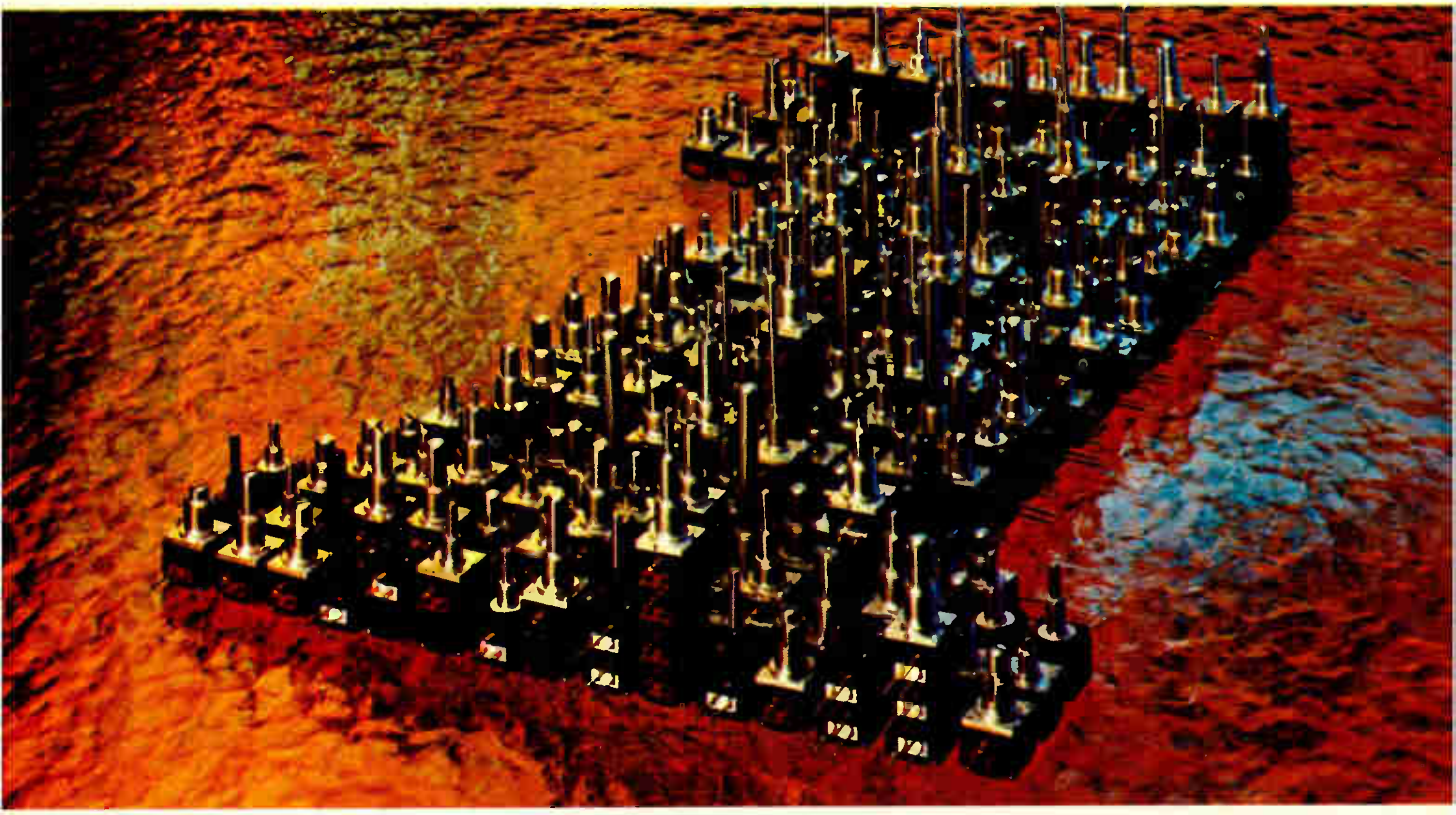

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 Circle 32 on reader service card

Sub-50-ns RAM tester already on line

Without advance fanfare, a second-generation memory tester billed as capable of matching the sub-100-ns speed of current random-access memories is already in place at a manufacturer. Macrodata Corp. of Woodland Hills, Calif., confirms it has shipped the first M-1 tester, reportedly to Intel Corp. Intended to fill a void in the tester lineup, where the state of the art is 10 to 12 MHz, the Macrodata machine can fully exercise such devices as a 4-K static RAM, **making accurate measurements to 40 ns at a 25-MHz cycle time, according to the company.** In an obvious challenge to the market leader, the complete unit is priced at $110,000, some 25% below the model J-387 10-MHz tester built by Teradyne Inc.'s Semiconductor Test division.

TI lowers price of 7-bit converter to 50 cents

In selling its new 7-bit analog-to-digital converter for 50¢ in large quantities, Texas Instruments Inc. may have found the price floor for such devices. The TI 507 converter, which will be in volume production in November **and will cost 65¢ in lots of 100, is intended for the nonprecision industrial and consumer markets.** Ramesh Gidwani, linear marketing manager for TI's integrated-circuit operation in Dallas, says the new IC will replace a handful of discrete components selling for $2.50 to $3.

Univac looks to C-MOS on sapphire as a VLSI route

"The low-capacitance and low-power characteristics of complementary-MOS-on-sapphire technology suggest it may be the choice for very-large-scale integration in the long run." That is the view, not from RCA Corp.'s Solid State division, a bulwark of sapphire-substrate technology, but from the director of research and technical planning at Sperry Rand Corp.'s Sperry Univac division in Blue Bell, Pa. Barry R. Bergerson says Sperry Univac's research center in Sudbury, Mass., **is completing the transfer of 7-μm-channel-length sapphire technology** to a semiconductor facility in Eagan, Minn., that is producing limited quantities of C-MOS-on-sapphire devices. They will be in new products from Sperry Univac's Defense Systems division and Sperry Rand's Flight Systems division. Meanwhile, the research center is starting work on 4-μm processing.

Itel, Four-Phase, German firm create development system

Itel Corp. of San Francisco has joined hands with two other firms to create Maestro, **a minicomputer-based, distributed software-development system** that comprises a printer, up to four disk units, a tape drive, up to 10 video terminals, and a central controller that connects to a wide range of mainframes. Software for Maestro is licensed from Softlab GmbH of Munich, West Germany. Under an OEM agreement, all hardware is supplied by Four-Phase Systems Inc., Cupertino, Calif.

IBM builds own 64-K RAMs for new computer

While semiconductor manufacturers are struggling to finish their 64-K dynamic random-access memories, IBM Corp. is announcing a computer that will use its own such chips. Built at IBM's General Technology Division in Burlington, Vt., **the n-channel metal-gate devices will be used in the company's 8100 distributed-processing system,** which will be available in 1979's third quarter. In its smallest configuration, the 8100 uses 48 of the RAMs and with disk drive, three printers, and six terminals will sell for $91,815.

Electronics newsletter

Signetics builds fast chip to control disks

Because MOS technologies are too slow, Signetics Corp. is about to spring a bipolar floppy-disk-controller chip that is two times faster than double-density data rates, or a speed of 8 μs per byte. The Sunnyvale, Calif., company claims the 8X330 is **the first third-generation controller because it has data separation and precompensation in chip.** Moreover, all program elements are under program control, so that the 8X330 can handle all the mainframe formats and their variations. The 63,000-square-mil chip, which combines analog with Schottky-transistor-transistor- and integrated-injection-logic circuitry, is designed to work with Signetics blindingly fast 8X300 bipolar microprocessor. Soon to go to customers for evaluation, the nine-chip 8X330-based controller system is due early in 1979. Western Digital Corp. and Nippon Electric Co. have previously announced double-density floppy-disk-controller chips.

Radio, TV ICs due from National

Two speedy ICs aimed at the consumer market are coming from National Semiconductor Corp. in Santa Clara, Calif. **The firm uses both integrated injection logic and emitter-coupled logic** in its DS8907 digital-frequency synthesizer IC. Aimed at stereo and auto-radio markets, the chip handles a-m signals to 15 MHz and fm signals up to 120 MHz. National is also offering samples of a linear bipolar IC: the LM1886 video-matrix digital-to-analog converter, which boasts generation of 512 shades of color, eight levels of gray, low-power-Schottky-TTL inputs, and compatibility with both U. S. and European video specifications.

AMC aims at Intel with five new boards

By announcing the AMC 95/4000 as the industry's most powerful single-board microprocessor-based system (p. 174), Advanced Micro Computers Inc., the joint venture between Advanced Micro Devices Inc. and West Germany's Siemens AG, is drawing a bead on industry-leading Intel Corp. with five more boards for the single-board-computer marketplace.

In November, the Sunnyvale, Calif., company will add a 32-K random-access-memory board, the 95/1032. In January will come two more: the 95/2000, a 32-K erasable read-only-memory board, and the 95/6011, which can be added to Intel's 8080-based SBC boards to give them floating-point arithmetic capability. **Later in 1979, AMC plans to launch a floppy-disk controller board and a 16-bit microprocessor board** based on the Z8000 that AMD is second-sourcing from Zilog Inc.

Addenda

Looking to expand a telecommunications business that accounts for about $100 million of its revenues, General Instrument Corp. of New York is expected to join the manufacturers of communications products and systems **that are vertically integrating into the fiber-optics field.** GI's chairman and chief executive, Frank G. Hickey, confirms that his company is in the early stages of negotiations to acquire a producer of fiber-optic transmission equipment. . . Data General Corp. of Westboro, Mass., has unveiled the smallest member to date in its Eclipse family. The C/150 is an **entry-level computer designed for a variety of dedicated commercial applications** as well as distributed-processing environments. . . RCA Corp. will join the growing list of semiconductor makers in the codec business with a four-channel device due to appear in 1980 or 1981. **The single-chip part will be made with complementary-MOS-on-sapphire technology** and will be an A-law device for the European market.

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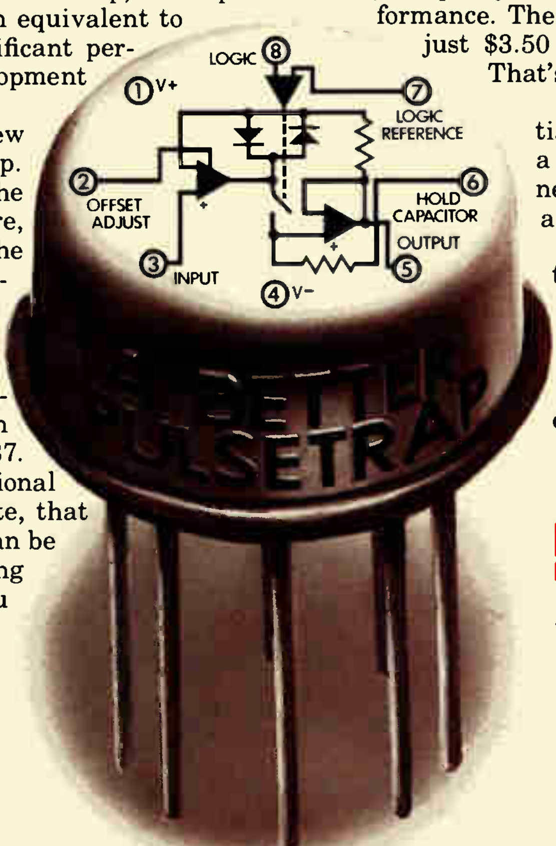

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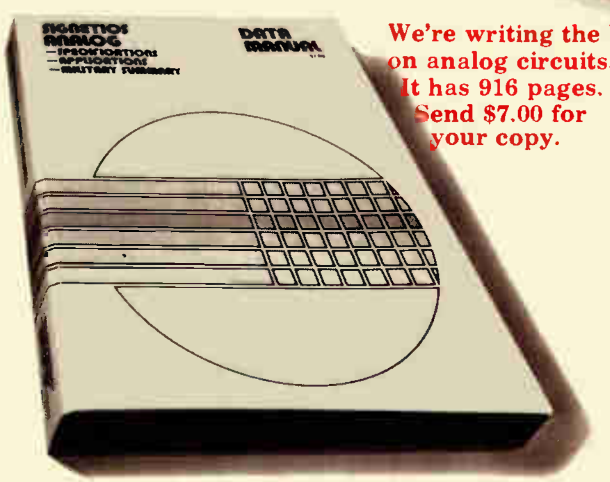

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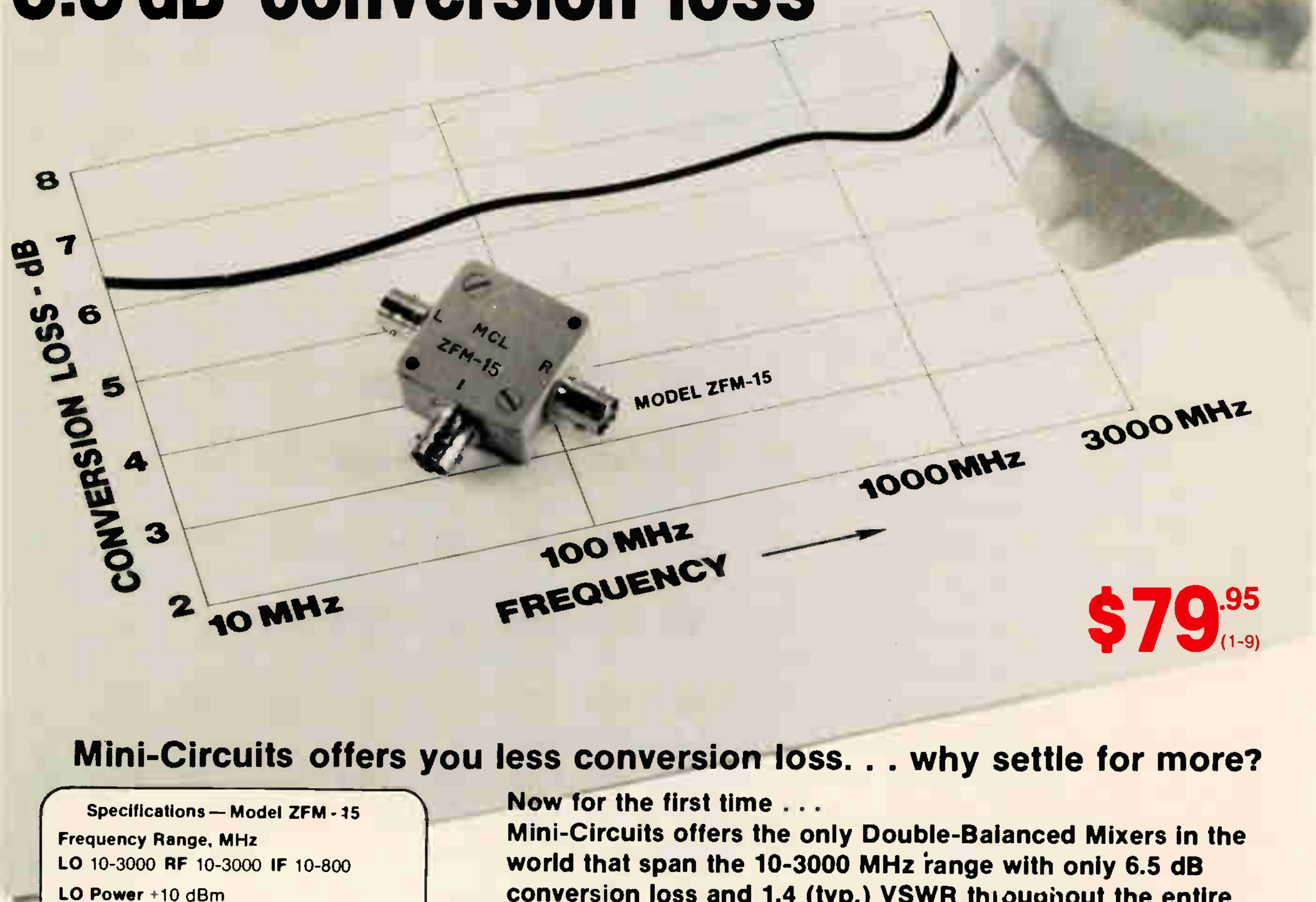

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Circle 38 on reader service card

R30/Rev/A

SOS technology gets big boost from HP computers

LSI central processor reduces nine-board model to three chips measuring 200 mils each on a side

If silicon-on-sapphire technology needed more credibility to become a full-fledged contender for use in large-scale integrated circuits, then Hewlett-Packard Co.'s new three-chip SOS LSI central processing unit should provide some.

The new CPU in effect shrinks over 90% of the logic of HP's 3000 series II minicomputer's nine-board CPU—some 700 square inches—to slightly less than 1 square inch. What's more, its microprogrammable architecture permitted HP to use it in two new computer systems, the model 300 and the 3000 series 33.

"The three chips comprise all the arithmetic and microprocessor registers, the arithmetic/logic unit, and the processor itself," says Jacob R. Jacobs, engineering section manager at HP's General Systems division in Santa Clara, Calif. Those chips enabled HP's system designers to fashion a two-board CPU with the capability of the 3000 series I's CPU that is even faster, Jacobs says.

The firm was first attracted to SOS technology by the prospects of high speed, low power, and design flexibility inherent in the static complementary-metal-oxide-semiconductor logic placed on a sapphire substrate; the design team had to reckon with problems like high leakage currents, poor metal coverage of oxide steps, and low breakdown voltages. Hewlett-Packard continued to nurse its infant technology along until its research and development efforts paid off with a new process called local-oxidation SOS, or Losos.

Rather than etching the field regions down to the sapphire surface, only half the silicon-nitride film layer is etched away and oxides are allowed to fill in these island channels, thus forming a planar surface. This eliminates metal-coverage and breakdown-voltage problems. Leakage has been markedly reduced by making the process cleaner and controlling epitaxial film growth rates and thicknesses more precisely.

Last year, HP introduced the 16-bit CPU, a device with 125-nanosecond clock speeds that dissipates only 350 milliwatts. The newest members of HP's growing SOS family, however, operate at 90-ns clock rates.

The evolution of the RASS (regis-

With SOS. The HP 3000 Series 33 computer in foreground, introduced last week, incorporates three-chip silicon-on-sapphire central processor, requiring just two boards.

ter, address, skip, and special), RALU (register, arithmetic/logic unit), and PCU (processor control unit) chips followed the 16-bit CPU chip [*Electronics*, May 26, 1977, p. 103] quite smoothly, according to Jacobs.

"These chips [each less than 200 mils on a side] average 8,000 devices each," says E. David Crockett, program director of advanced computer systems. While that is less than spectacular contrasted with n-MOS device densities in the tens of thousands, Crockett points out, "We're using 6-micrometer design rules and are really just breaking ground with this technology."

Crockett believes the resources of SOS have barely been tapped and this new CPU board set, the integrated computer family Processor 25, is likely to be just one of a group of such designs that will be incorporated in future HP products.

Secret revealed. Two of those products were unveiled last week in New York City. The smaller of the two, code-named Amigo, surfaced as the small-business system HP 300. Beneath a deceptively simple exterior, which resembles a cathode-ray-tube terminal on a pedestal, is the 16-bit CPU and 256 kilobytes of main memory consisting of 16-K n-MOS random-access memories. Inside the pedestal is HP's new 12-megabyte Winchester-type fixed disk drive, which it makes in house. And HP's first floppy disk drive to be manufactured in house—a 1-megabyte version—is mounted next to the CRT.

The 300 is designed to answer a fundamental user dilemma, according to Vijay Kapoor, that product's manager. "Now, he has basically two choices: either a general-purpose computer system or a dedicated minicomputer system," he says. Unfortunately, neither is the optimal choice, he says, because the first is too expensive and has an architecture attuned to multi-user tasks, whereas the second lacks sufficient program storage or growth capability. "Amigo has the optimal combination of both," Kapoor believes.

The second new system, the HP 3000 Series 33 was known as Project Toothpick. With prices ranging from $70,000 to $160,000, the new Series 33 is expected to replace the older 3000 Series I which started at $75,000, and some Series II units, which started at $110,000.

The 256-kilobyte n-MOS random-access main memory can be expanded to a megabyte and the rigid-disk drive storage capacity can grow to 960 megabytes. Up to 32 remote terminals can be hooked to the Series 33 and its menu of programming languages includes Basic, RPG II, Cobol, Fortran, and SPL. "The 3000 Series III can only handle one other—APL," Edwards points out.

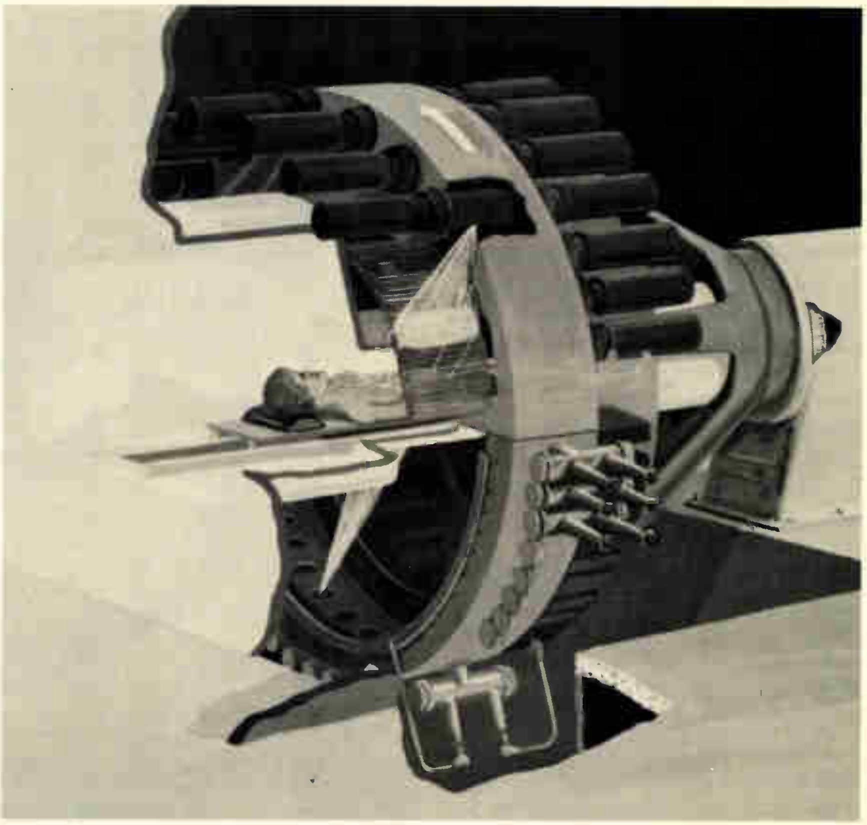
The reason it is possible to build very different systems around the same CPU architecture is the built-in microprogrammability. "The only differences between the two CPUs are their read-only-memory microprograms and a resistor jumper," says Edwards. The company is scheduling deliveries of the first of its new systems in about 14 weeks. □

Medical

X-ray machine will allow doctors to reconstruct images of moving organs

Doctors will be watching moving pictures soon, but what they will be seeing is a little different from a Hollywood film. With the help of a novel X-ray machine being built by Raytheon Co. for the Mayo Clinic, physicians are going to be able to view a heart pumping, lungs breathing, or blood circulating in near real time.

The machine, known as the dynamic spatial reconstructor, will take X-ray scans in rapid succession, which will then be computer-



Dynamic. Artist's rendering of Raytheon X-ray machine shows X-ray tubes mounted on lower semicircle and their radiation picked up on fluorescent screen just above the patient.

processed for display. Using this diagnostic aid, Mayo researchers hope to be able to detect organic disorders at a very early stage.

The DSR is similar to computerized-axial tomography scanners in that it moves around the patient at about 15 revolutions per minute while taking X-ray pictures. But there the resemblance stops.

The CAT scanner has one X-ray tube; the DSR has 28 X-ray tubes and modulators aligned in a semicircle opposite 28 imaging systems, which pick up the images and send them to a fluorescent screen. Everything is gantry-mounted and computer-controlled to maintain an optimum timing sequence for the tube firings, as well as to open and to close the gates on the imaging system.

Scanning. "The DSR allows synchronous, volumetric scanning instead of cross-sectional views," says Dr. Earl H. Wood, professor of physiology and medicine and senior consultant at the Mayo Medical School in Rochester, Minn. By using a fan-shaped beam from the 28 different sources, a volume of about 25 by 30 centimeters in diameter is scanned, instead of the 1-millimeter-thick slice that is obtained by a CAT scanner.

Each of the 28 X-ray tubes can be fired every 1/60 of a second, in any programmed order. The X rays pass through the patient's body and are projected on a single semicircular fluorescent screen, which forms the base of a U-shaped chamber housing the 28 imaging systems. Each imaging system contains an image intensifier to amplify the light and hold the X-ray pattern, plus a television camera to record the picture.

"The TV camera does a normal scan-pickup. It can do it as fast as it can be done electronically," says Herman J. Yost, manager of special programs at Raytheon's Equipment Development Laboratory in Wayland, Mass. The data is then stored on video disks.

The stored data feeds into a computer, where anatomically based algorithms help excise any unwanted information, such as bone-tissue data, from the video data. The computer then combines the various two-dimensional pictures to create a picture moving in three dimensions. Four seconds' worth of scanning, which will be about normal for most diagnostic work, will generate enough data to strain the resources of the clinic's computer and software programs.

However, the clinic will soon have a Classic computer from Modcomp Corp., Fort Lauderdale, Fla. With software programs now being developed in house and by outside consultants, the computer should eventually enable doctors to see the moving X-ray pictures in close to real time.

Parts. The gantry, weighing 10 tons and measuring 24 by 13 feet in diameter, is loaded with X-ray tubes and imaging chains being supplied by Raytheon. The X-ray sources and modulators, as well as the anode motor control housed off the gantry, are being manufactured by a subsidiary, Machlett Laboratories Inc., Stamford, Conn.

Raytheon is also supplying an encoder for positional data on the tubes, a Z80 microprocessor to control timing intervals and tube-firing sequences, as well as a 120-kilovolt power supply. Mayo is supplying the fluorescent screen and imaging systems through other contractors. "These combinations are new, but the technology is well known. You have to be pretty sure of yourself when you're grounding 60 kilovolts," observes Yost.

Raytheon has received $1.7 million for its work from the Mayo Clinic grant of $5.3 million from the National Institutes of Health for the DSR hardware and software development. A model of the device was shipped early last month and, starting in January, 1979, full-scale assembly will begin at Raytheon's Wayland facility, with delivery slated for late spring. Researchers at the clinic hope to have most of the system in operation within the next two years. □

Ultrasound scans small body organs, giving high-resolution video pictures

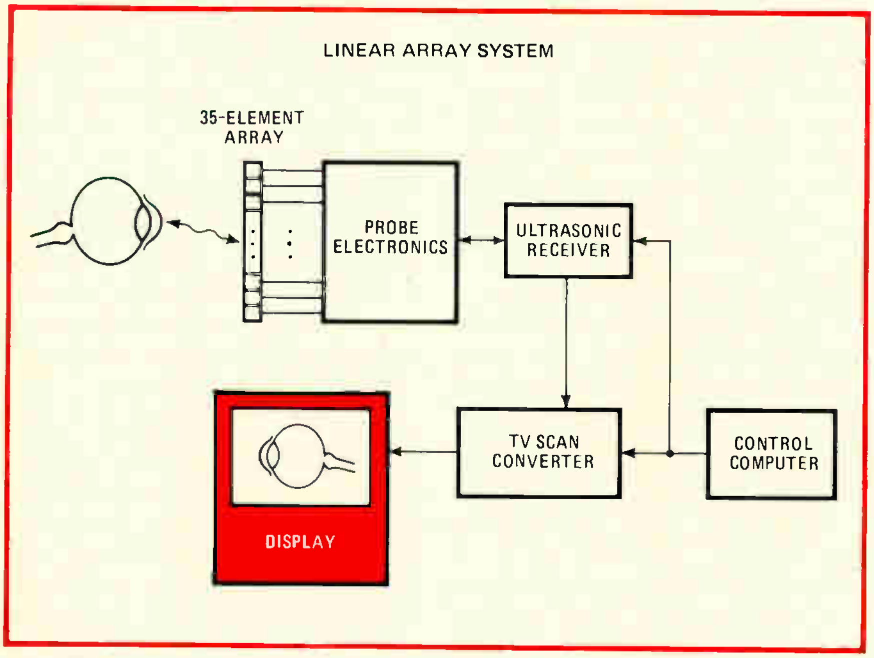
Although ultrasonic scanners are generally a safe way to probe body organs, even mechanical versions do not offer enough resolution to let clinicians view small moving organs. Now, Stanford University engineers have turned to an electronically switched array of ultrasonic transducers to build a scanner that yields high-resolution video pictures of moving body organs, such as an eye or a neck artery.

"It allows us to do dynamic real-time imaging of small organs," says Dr. Alan L. Susal, clinical assistant professor of ophthalmology at the school of medicine who also holds a BSEE degree. The scanner performs well, having an axial resolution of 0.3 millimeter and a lateral resolution of 2 mm.

Like the Raytheon X-ray machine in the preceding story, the scanner is one of the projects funded by a grant from the National Institutes of Health, this one to Stanford's Center for Integrated Electronics in Medicine, which combines the expertise of Stanford's Electronics Laboratory and its School of Medicine. In spite of their vastly differing setups, both machines have a common use: exploration of the living body.

Generally speaking, there are two types of ultrasonic scanners. The A-scan produces a display similar to a sonar display, while the slower B-scan provides an oscilloscope display similar to a cross-sectional X-ray picture. Even with motorized switching, B-scan arrays still produce flickering images. Stanford's approach uses a solid-state technique to convert the low-rate ultrasonic video signals into television rates. The system is controlled by a Zilog Z80 8-bit microprocessor.

So that doctors can easily use the scanner, it comes in two parts: a hand-held probe connected by a 6-foot cable to the control unit, which contains the 9-in. television



Sounding. Transducer array designed by Stanford engineers is the front end of an ultrasonic imaging system that will permit real-time images of small organs as they move.

monitor, push-button controls arranged in functional groups, and the logic circuitry. The probe has 35 in-line 1-by-4-mm transducers that are electronically scanned by custom high-voltage double-diffused metal-oxide-semiconductor multipliers made in the university's integrated-circuit laboratory. The transducers are scanned in groups of four, shifting down line one element at a time. The array can scan 3.2 centimeters; four elements together have a near-field range of 6 cm at the 7.2-megahertz operating frequency.

The ultrasonic video signal coming into the control unit is digitized into 6-bit words, explains Terry Walker, research assistant. It takes 560 words just to produce one 80-microsecond transmit-receive ultrasonic cycle; these are temporarily stored in a high-speed shift-register memory.

After two adjacent ultrasonic lines are stored, they are read out at twice the speed to get the time conversion necessary to fit the 40-μs timeframe for horizontal television lines. Simultaneously, a third memory line is available to collect new inputs. In addition, the intermediate digital storage permits an interpolator to smooth the vertical display.

Stanford's scanner displays the B-scan information; the calibrated A-scan wave, from which a doctor can derive additional information about the organ under examination; and information on reticule scales, alphanumeric data, and distance measurement cursors. The Z80, with 4,096 bytes of random-access memory and 8,192 bytes of read-only memory, also permits such features as remote frame freezing and video-tape recording.

Although the scanner originally was designed for eye examination, where it can detect detached retinas hidden behind bleeding, Dr. Susal says it can also be used safely, for example, to examine neck arteries for constrictions that could lead to strokes. □

Computers

Burroughs unveils networking scheme

In the past few years, computer manufacturers have filled a horn of plenty with proprietary versions of the distributed processing concept. Beginning with IBM and its Systems Network Architecture, one mainframe maker after another has introduced a network architecture. Most recently, Burroughs Corp., Detroit, Mich., added its two cents with its Burroughs Network Architecture.

Last but not least. Although Burroughs was in the distributed processing market early with its Terminal Computers or TC line of equipment, it was the last of the large mainframe computer companies to unveil its networking architecture. The network supports any of Burroughs' mainframes in the B1000 through B7000 series. Other makers' computers can be included in the network as well.

In this respect, BNA is more versatile than IBM's SNA. Moreover, SNA limits the number of host computers in a network, centralizes control in one host, and limits the amount of processing power any other element in the network can have. Control of the network in the Burroughs approach is not centralized [*Electronics*, Aug. 31, p. 34]. Instead, a software package is installed in each of the network's computers.

The two-part package consists of Network Services, which handles the communications protocols, and Host Services, which manages the distributed data-processing functions. Network Services supports Burroughs' Data Link Control Protocol, as well as the standard High-Level Data Link Control (HDLC), Burroughs' Global Memory Interface, and X.25 packet-switching interface. It also handles the routing of messages through the network and manages the network topology.

Host Services, which resides in the operating system, has protocols for transactions under Burroughs Data Management System, file and task handling, work flow language, status inquiry, and station handling. These protocols allow any processor in the network to access data and share resources resident in other network processors.

Although this is the first formalization of its networking philosophy, Burroughs points out that most of the functions performed by the Host Services portion are already imple-

SCIENCE/SCOPE

"The greatest contribution to communications since the synchronous satellite" was the promise made by a Hughes official for the tri-service Joint Tactical Information System (JTIDS). It is being developed to deliver critical command-control-communications securely, with resistance to countermeasures. In a totally inter-operational manner for the Joint Chiefs of Staff, the system could feature three basic terminal types: Class I for large platforms like the USAF/Boeing E-3A Airborne Warning and Control System and the Navy's Naval Tactical Display System carriers; Class II for air superiority aircraft such as the F-14, F-15, A-10 and F-4; Class III for Manpack radios and remote piloted vehicles.

Orbiter's 300 million mile journey to Venus ends, and its scientific mission begins on December 4. Then this first of two Pioneer Venus spacecraft, with its dozen scientific instruments, goes into orbit around the planet. While circling, Orbiter will determine the detailed structure of the upper atmosphere and ionosphere. It will look for variations in the gravitational field, and use remote sensing to survey Venus' atmosphere and surface. A cloud polarimeter will provide visible- and ultraviolet-light pictures resembling those taken of the earth by weather satellites. A Hughes-developed radar mapper will pierce the dense cloud cover to make pictures of Venus' surface.

The spacecraft will orbit for at least one Venusian day (243 earth days). Data obtained should help scientists understand Venus' weather patterns, and provide new insights into causes of the earth's complex weather cycles. Orbiter and its sister ship, Multiprobe, were built by Hughes for NASA's Ames Research Center.

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Television broadcasting direct from satellites to schools, hospitals, hotel and motel chains, and other institutional users may be one result of a new NASA program. Hughes will develop for NASA's Goddard Space Flight Center a low-cost, mass-producible 12-GHz receiver for TV reception from broadcast satellites. Objective: a smaller, less expensive receiver to sell for under $1000. Current ground terminals are in the 4-GHz frequency range, and cost between $20,000 and $30,000. The higher frequency range has already been approved by the FCC for domestic TV satellite systems.

Creating a new world with electronics

HUGHES

HUGHES AIRCRAFT COMPANY

ry System, which allows up to four B6800 processors to access a common portion of main memory. BNA currently supports only host-to-host communications on the network. Communications between the host and any network of terminals will continue to be handled by Burroughs' network definition language and message control system. □

Solid state

Giant radio telescope uses 19,500 chips for complex signal processing at 100 MHz

Everything about what will be the world's largest radio telescope is gargantuan. It stretches across an area 26 miles in diameter and consists of 27 separate, movable antennas, each weighing 210 tons, with 82-foot dishes. Such a telescope, using phased-array antennas to get the effect of one large unit, poses king-sized circuitry demands in keeping with the physical dimensions of the project.

So the National Radio Astronomy Observatory is turning to large-scale integration for circuitry to help pick out weak deep-space signals. The telescope, near Socorro, N. M., will use 6,500 emitter-coupled-logic correlator chips and 13,500 transistor-transistor-logic integrator chips designed for the project by Silicon Systems Inc., Irvine, Calif.

The gathered signals, emanating from events thousands of light years away, usually are weaker than the background noise in the front-end antenna receivers. The only way to pick signals out of the noise is to combine the output of the 27 receivers and put them through digital filtering in real time.

Complicated. "It's no easy task, that's for sure," says Ray Escoffier, design engineer for NRAO. Filtering out the common signal component in real time requires comparing each antenna output to every other one, for 351 antenna pairings, plus multiplying each against 16 points to be measured in the observation process. "This amounts to 11,654 digital multiplications at a 100-megahertz data rate," says Escoffier.

Designers had to look to LSI technologies, he says, because discrete circuitry was too bulky, too slow, and too hot. "It was soon clear that ECL was the only way to go," he recalls, particularly for the correlator. Because such parts do not exist commercially and because large semiconductor houses will not take on such a low-volume application, NRAO turned to Silicon Systems, which is an independent semiconductor manufacturer specializing in all types of custom integrated circuits.

The chip sets can function at a clock rate of up to 300 MHz with static inputs or 200 MHz with dynamic inputs—far above the NRAO requirement. As key links in the signal-processing chain, the chip sets take the 100-MHz, three-level digital code from analog-to-digital converters and produce signal data in 4-MHz serial form for the central computer to analyze further.

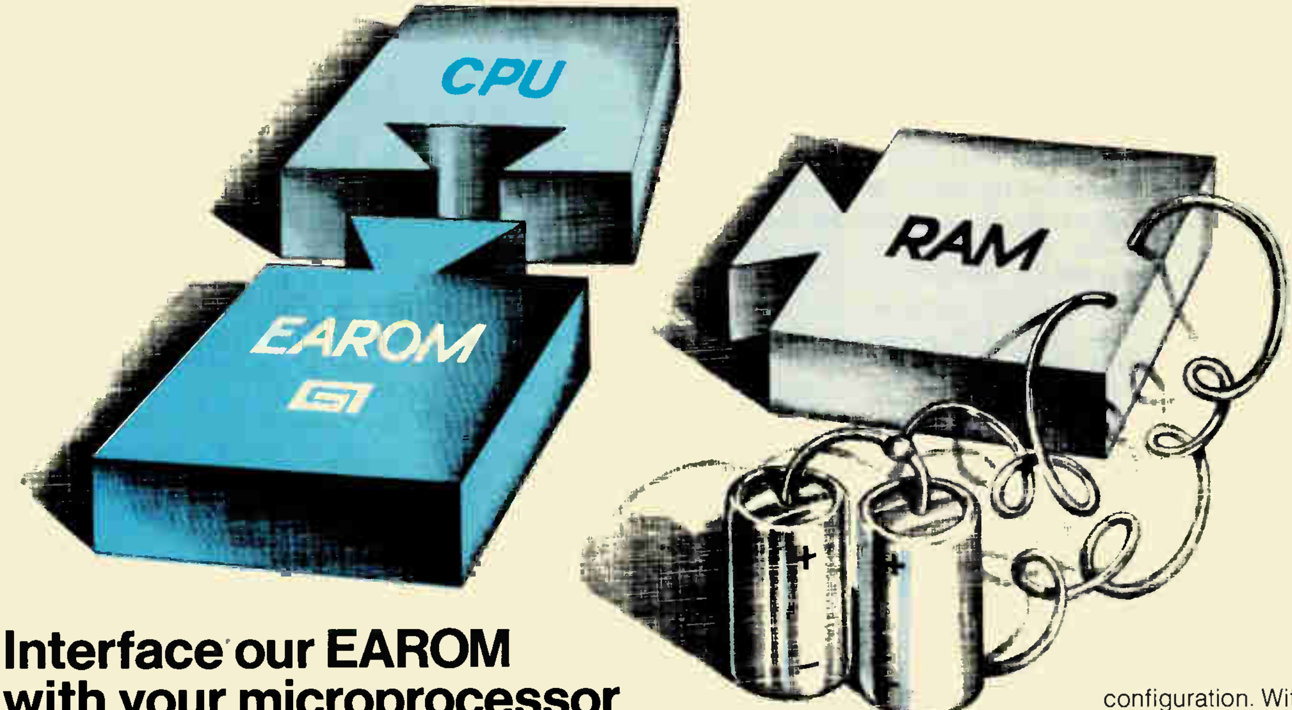
For the 100-MHz data-rate correlator, Silicon Systems fabricated a 90-by-93-mil ECL chip. It has three tiers of logic gating implemented by stacking current switches in three layers, a configuration that cuts propagation delay time. Essentially, the 6,500 ECL chips are digital multipliers, which filter out the common signal component from the 27 antennas. The design has four flip-flops, eight input buffers, and two ECL-to-TTL converters.

For the somewhat slower integrator, low-power Schottky TTL was adequate for a 423-transistor device (78 by 93 mils) that essentially serves as a counter and shift register. The 13,000 integrator chips combine the correlator outputs for 4-MHz transmission to the mainframe computer.

Escoffier believes the ECL devices represent a significant improvement over discrete technology. "Power dissipation is cut from 25 watts to 7.8 W, and the space required for the 6,500 correlator and 13,000 integrator chips takes up half what a

Listening. Twenty-seven of these 82-foot-diameter dishes will form the gargantuan antenna of the National Radio Astronomy Observatory's radio telescope, being built near Socorro, N. M., which uses custom-designed ECL and TTL parts.

GI EAROM, the reliable non-volatile memory.



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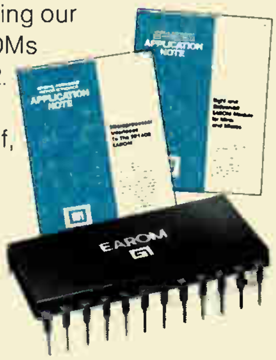

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discrete system would." Two racks house the printed-circuit boards that hold the chips.

Another benefit, he thinks, is increased reliability from cutting interconnections and bonds from 900,000 to 175,000. Furthermore, the Silicon Systems LSI cost $100,000 less than discretes would have. "The ECL chips can be useful in any high-speed signal processing," he says and refers to at least three other observatories to use the Silicon System ICs.

Startup. With 15 antennas completed, the telescope will start working late this month, and the other 12 antennas will be phased in, as they are finished, at the rate of one each six weeks. The antennas will permit astronomers to use what is called spectral-line processing, which yields more information about space phenomena than the continuum technique used since the mid-1970s in a 12-antenna array. Spectral-line processing, however, needs better resolution (50 megahertz at gigahertz frequencies) and therefore requires extra antennas and faster processing for real-time work. □

Layered GaAs ups semiconductor speed

In pursuit of speed, semiconductor manufacturers have scaled down transistor dimensions, reduced charge-storage delays with Schottky diodes, and revamped circuit designs. But at Bell Laboratories, researchers are juggling with a much more fundamental semiconductor dimension—the crystal structure—to enable electrons to travel several times faster than their conventional solid-state speeds.

The technique, developed at the Murray Hill, N. J., labs, alternates layers of two different materials, gallium arsenide and aluminum gallium arsenide, to isolate the electrons from the positively charged donor ions that slow their flow. The result is that electron mobility, which translates indirectly into device switching speeds, doubles at room temperature and increases nearly 20 times at temperatures approaching absolute zero.

CCD benefit. The approach appears most immediately suitable for charge-coupled devices, since those are the simplest of semiconductor devices, requiring no extra impurities or junctions to be formed. An insulating layer would be deposited directly onto the high-mobility GaAs layer, and a metalization pattern would move underlying charge packets in accordance with a clocking scheme. The multilayered semiconductor would allow much faster clocking rates than current CCDs. Furthermore, its three-dimensional characteristic could be used to improve density: another insulator could be deposited, followed by another two-layer structure, and so forth.

In the basic process, the alternating GaAs and AlGaAs layers are each made about 50 molecules (100 angstroms) thick. The AlGaAs layer is doped very near its center with silicon, which donates the electrons. The free electrons then migrate to the lower energy level of the GaAs layer and are thus isolated from the influence of the embedded positive silicon ions.

Contributor. The advancement is made possible by Bell's molecular-beam epitaxy process for growing crystals, which literally constructs materials a layer of molecules at a time. The process is very slow—a layer is grown in about 3 seconds, and 100,000 or more layers are often built up for a workable sample. In Bell Labs' solid-state department, technical staff members Raymond Dingle and Horst Stormer, who designed the layered structure—also called a super lattice—admit that much more work remains before its properties can be optimally applied to a useful device.

"The material does lend itself well to field-effect devices," says Stormer, "but we think the devices that will really use the layered structure to the fullest haven't been invented yet."

Dingle adds that other semiconductor materials can also be used, as long as the energy band gaps are sufficiently different "and the atoms stack well." What's more, says Dingle, since the effects are far more dramatic at very low temperatures, the process seems applicable to devices acting as interfaces to Josephson-junction logic circuits at supercooled temperatures. □

Packaging & production

Making tape drive is like child's play

Anyone who has put together a plastic model airplane is familiar with the snap-it-together assembly method long popular with toy makers. The method is now being applied in an industrial product—the transport and housing for a palm-sized digital tape recorder.

The Qantex division of North Atlantic Industries Inc. of Plainview, N. Y., builds these elements for the model 200 Minidrive by removing 16 premolded plastic parts from a common stem and snapping them together. The 4-by-2-by-4-inch recorder accepts a 3M DC100a miniature tape cassette.

Joel Kramer, president of Qantex, says, "We were looking for an assembly technique that would give us high-output productivity with a minimum labor content, so we decided to go to a tape transport that required an almost hardwareless assembly procedure for its plastic parts, electromechanical parts, and printed-circuit boards." The model 200 is now in full production, and Kramer estimates that the method has saved approximately one hour per drive in assembly time and has also cut hardware costs.

Key to using the method for this tape transport was the choice of plastic. To be satisfactory, the material had to have both a low coefficient of friction for the drive's moving parts and tape guides and a high dimensional stability for precisely dimensioned parts like the magnetic head's housing.

Qantex's choice was Du Pont's

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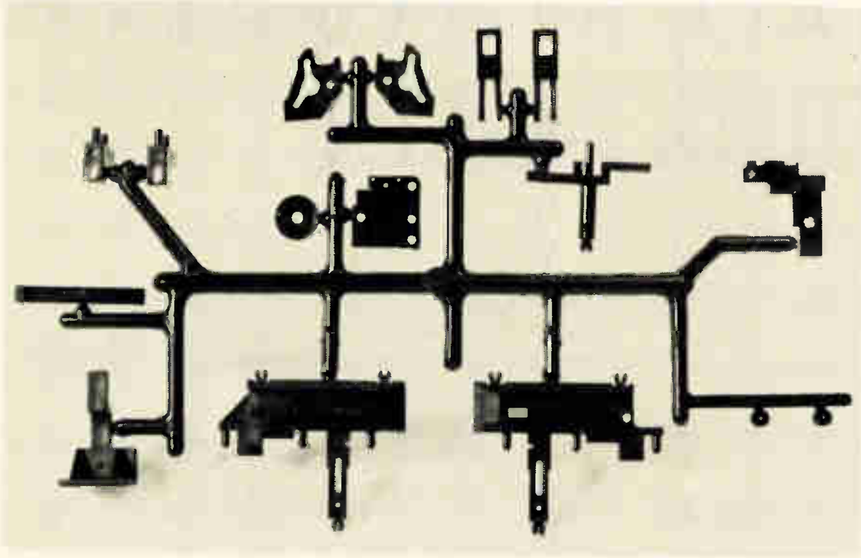

Snap together. Shown above are the 16 molded Delrin parts of the Qantex model 200 Minidrive tape transport after removal from a mold. These precision parts are separated from the single molded piece and assembled with a minimum of hardware onto an aluminum base.

Delrin, a metal-like material that has the required dimensional stability as well as excellent surface lubricity. This smooth, hard material has been used to manufacture gears and the pinch rollers of commercial audio tape recorders.

Piece work. To start, the 16 pieces that make up the housing and transport are injection-molded as a single unit. Next, the 16 pieces are separated and then assembled on a stamped aluminum plate by a novel method that uses a minimum of hardware and fasteners.

Each of the 16 molded pieces has cylindrical rods that are inserted into mating holes on the plate. After a washer has been dropped over a protruding rod, heat is applied, flattening the plastic rod against the washer and filling the hole. To hold critical parts that might need alignment, such as the tape guides and magnetic head holder, nuts are threaded into the Delrin posts. As a final touch, the pc boards that carry the system electronics are held in plastic-molded forks instead of in the conventional screw/nut type of mount.

The plastic structure has passed environmental and life tests, which leads Kramer to the assumption that the method can be applied to parts of other data peripherals. He says Qantex's next "big" product will use the same kind of snap-together construction that is being proven in the Minidrive. □

is wire-(bond-)less

How about a substrate as thin as 0.17 millimeter (32 mils) to package integrated circuits? That will be possible with a Matsushita-developed packaging method called film on frame. As a bonus, FOF eliminates a production step, substituting thermal bonding for wire bonding of the chips to their substrate.

The new technique will contribute to making hybrid systems considerably smaller, according to Masaharu Noyori, Hirokai Fujimoto, and Isamu Kitahiro of the Matsushita Electrical Industrial Co.'s semiconductor research laboratory in Osaka, Japan. It could be particularly useful in consumer products, they say.

Advantages. Besides giving high component density and ultrathin packaging, an FOF substrate can be bent as needed and eliminates specially bumped chips, the researchers claim. Moreover, the technique offers inherent high reliability since there is only one contact per interconnection, compared to the two that are required in wire-bonded packages.

When the researchers put together a calculator/clock package, the height of the substrate plus chips was only 0.8 mm. This compares with 1.55 mm for the typical printed-circuit-board substrate plus chips, such as epoxy glass. The technique is still experimental.

As described by the researchers at the 1978 International Microelectronics Symposium in Minneapolis last week, the fabrication consists of five basic steps (see p. 51). The substrate itself is formed at 300° C by rolling a film consisting of a polyimide insulating layer and a fluorinated ethylene-propylene bonding layer onto a specially etched metal frame divided into a mainframe support and subframes that serve as external and internal leads. The polyimide is about 12.5 micrometers thick, the ethylene-propylene from 1.0 to 1.5 μm. The frame, usually made of nickel, typically is 150 μm thick, depending upon the substrate's size.

In the next step (b), photolithography and chemical etching provide contact holes. The ethylene-propylene bonding layer is not affected by the etching.

Then the bare chips are heated to about 300°C, and their input/output pads are aligned with the contacts on the polyimide layer. As (c) shows, they are aligned on the ethylene-propylene side of the substrate, but the composite film's thinness and transparency make this easy. After alignment, a special jig presses the heated parts into the bonding layer, providing permanent bonding, and the ethylene-propylene at the bottom of the contacts is etched away with a plasma gas.

Conducting. In the fourth step (d), a 0.2-μm-thick layer of chromium and a 5-μm-thick layer of copper are evaporated onto the polyimide and the contact holes. After this, a silicone or epoxy resin coats the bottom of the ICs. In the last step (e), photolithography and etching forms the conductor patterns on the metal-covered polyimide surface. Typi-

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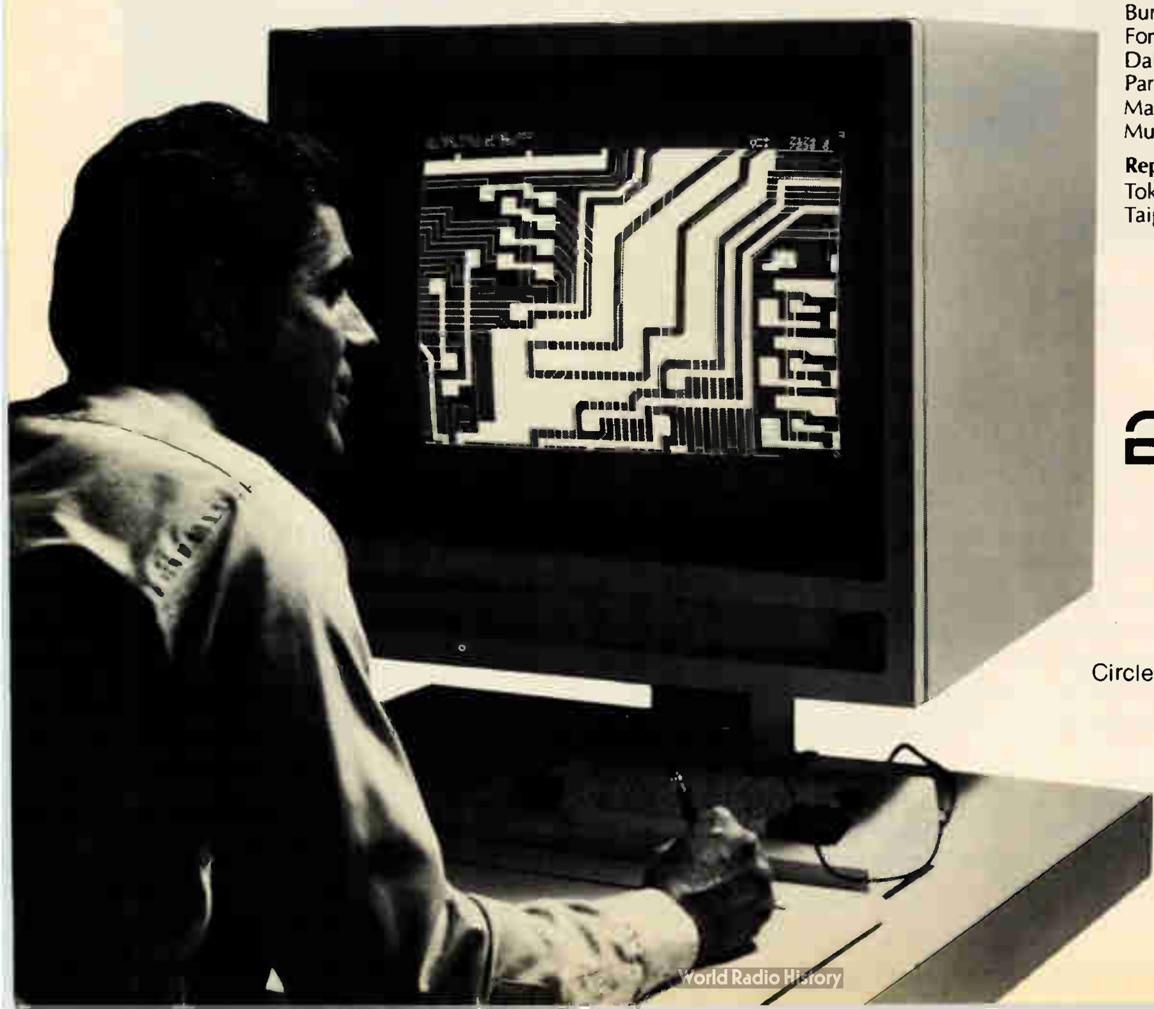

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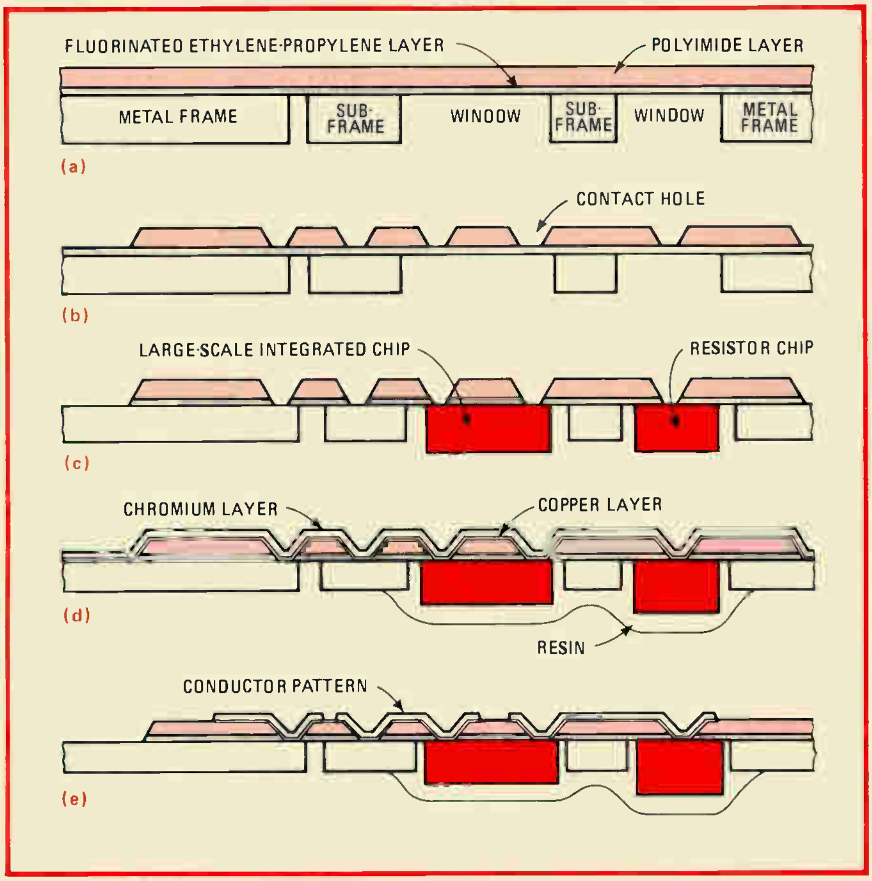


Low profile. With this five-step process, Matsushita researchers have produced a calculator-clock circuit only 0.8 mm thick, about half that of conventional packaging techniques.

cally, the lines and the intervening spaces are from 50 to 75 μm wide.

As a test vehicle, the authors packaged a calculator/clock that has operated for over 5,000 hours without a failure. The FOF substrate contained 16 electronic devices: 2 large-scale ICs, 10 resistor chips, and 4 capacitor chips. All fit within a 20-by-20-mm film area. □

Memories

Error correction enhances RAM board for 16-bit single-board microcomputer

Error checking and correction in main memory—a feature common in minicomputer and mainframe memories—is working its way down to the microcomputer level. A family of 16-bit random-access memory boards, which are compatible with Intel Corp.'s recently announced one-board computer (see p. 105), comes from Mupro Inc. in Sunnyvale, Calif. It could set the tone for larger microcomputer memory arrays, especially for the next generation of 16-bit systems that are coming along.

Mupro offered the first on-board error-detection-and-correction capability for Intel's Multibus interface specification and its iSBC 80 8-bit board family [*Electronics*, May 11, p. 166]. Now it is extending that capability to the just-introduced 16-bit iSBC 86/12.

The company is convinced that microcomputer memory arrays will continue to expand as RAM prices

News briefs

Digital watch patent issued to Commodore unit

A patent for a "solid-state watch with single time and date selector button," the operating approach used by virtually all digital electronic watch suppliers, has been granted to Frontier Inc., a unit of Commodore Business Machines Inc.'s Semiconductor division in Palo Alto, Calif. According to division president Bud Frye, the single-button technique is so fundamental to all electronic digital watches that "I know of absolutely no manufacturer of popular-priced digital watches who doesn't already use this approach."

ITT, Qume set merger accord

International Telephone and Telegraph Corp. of New York and computer peripherals manufacturer Qume Corp. have agreed in principle for Qume to become part of ITT through an exchange of stock valued at about $145 million. Principally a maker of impact printers, the Hayward, Calif., firm would continue operations under the Qume name with its existing management.

National will market PDP-11/34–compatible mini

National Semiconductor Corp. plans to begin marketing, possibly as early as November, a System 200 minicomputer that will be totally compatible in software and input with Digital Equipment Corp.'s popular PDP-11/34. The Santa Clara, Calif., company also announced that it has filed action in the U. S. District Court for Northern California, asking that various DEC patents on computer architecture be declared invalid and unenforceable.

Inmos wins first round in court

The first courtroom skirmish has been won by Inmos Ltd. in the opening stages of a trade secrets suit filed against the firm by Mostek Corp., Carrollton, Texas [*Electronics*, Aug. 31, p. 42]. Dallas Federal District Court Judge Robert Porter refused late last month to issue a preliminary injunction requested by Mostek against the newly formed British-backed firm. The judge said Mostek failed to prove that Inmos has already used or disclosed any proprietary Mostek trade information or that it intends to do so.

drop, and that means soft errors—errors that occur randomly and can be corrected when detected—are inevitable. Whether they are caused by power-supply fluctuations or alpha particles besieging the dynamic-RAM cells, only error-correcting schemes can fight the odds.

"With 64 kilobytes of memory, a soft error will occur once every eight months," says James Moon, Mupro's engineering vice president. "For certain users, like utility companies and some process-control industries, down time is money—they can't afford those errors."

Big board. Mupro's largest-capacity board, the MBC-128, is made up of 128 kilobytes—the largest array yet to be aimed at a microcomputer bus, and also the level at which most minicomputer makers say correction to safeguard against soft errors is an absolute necessity. The error-correction scheme Mupro uses is a modified Hamming code that adds 5 bits to each byte for its 8-bit memory systems and appends 6 bits to each 16-bit word for the new iSBC 86 family.

That means error correction is still a luxury, since the 128-kilobyte board needs a total of 88 16,384-bit RAM chips instead of just 64. "But boards are increasing in capacity for the same reasons the 8086 microprocessor can address a megabyte," says Moon. "When you're using a high-level language and an accompanying operating system, memory gets eaten up in a hurry."

Other manufacturers can be expected to offer the option for their systems either at the 64-kilobyte or 128-kilobyte level. Mupro is eyeing the 65,536-bit RAMs, which will be available in quantity sometime next year. Says Mupro's president Joel Korelitz: "If we put 64-K chips where those 16-K parts are, then error correction and detection will be inevitable." □

SIEMENS

Innovation in inductors too: Miniature coils with magnetic shielding

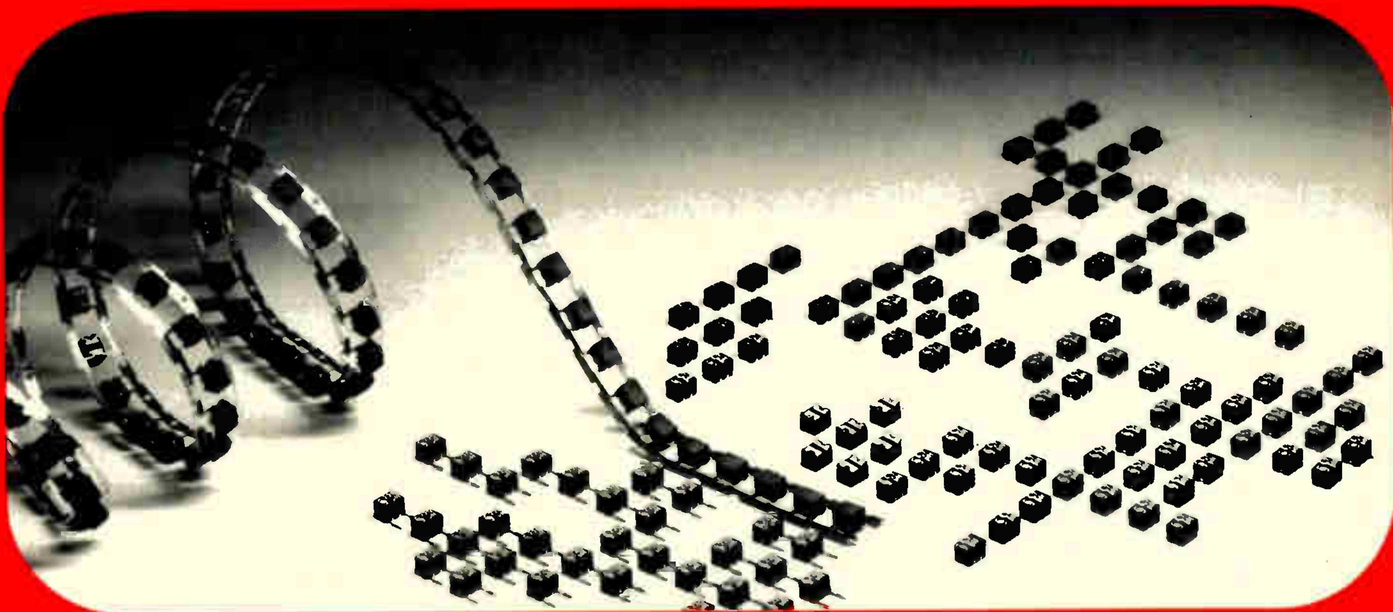
Integration, miniaturization and extremely high packing density put exacting demands on ferrite coil technology: Small size alone is not enough – of equal importance are perfect magnetic shielding against leakage flux and undesired coupling, and naturally also a favorable price.

All these requirements are satisfied by the new component family MIFI – miniature ferrite inductors from Siemens. The first MIFI line is already available: coils for PCBs and in chip form for film circuits, inductance range 0.10 to 470 µH, tolerances 5% and 10%. MIFI transformers and adjustable inductors are in development.

The constant high quality and favorable price of all MIFI components are the outcome of fully automatic fabrication, such as can only be implemented through close cooperation between ferrite and fabrication technologists, with one single, continuous production run from the blank to the wound, checked and marked inductor.

For detailed information write to Siemens Corporation, Components Division/Ferrites, 186 Wood Avenue South, Iselin, New Jersey 08830, quoting "Miniature inductors".

During production a fire-tinned tape is used for assembling and contacting the coil, only leaving therefrom small terminal pins or soldering surfaces at the finished coils.



MIFI: miniature ferrite inductors from Siemens

B 7814.101 a

Circle 53 on reader service card

Door To Verbal Control Of Machines Opened With NEC's Voice Terminal

NEC has successfully commercialized a voice data input terminal for machines.

The innovational DP-100 Connected Speech Recognition System recognizes 120 words, and accuracy is as high as 99% or more. Moreover, words can be spoken continuously at normal speed. All that is necessary is to register the operator's voice in advance so that the equipment can memorize the operator's voice pattern.

Since it has a built-in general purpose microcomputer, it can have a variety of programs required by specific users.

Making the DP-100 even more useful is the fact that the status of recognition is displayed, which enables the operator to confirm instantly the information he has just put in. In addition, it can be used in noisy places — even under environmental noise conditions of 85 dBA (85 phons).

The DP-100 Connected Speech Recognition System will be very effective when used for stock controlling, data feeding at points of sales, preparation of NC system control tapes, high-speed merchandise sorting in transportation, warehouse and many other operations.

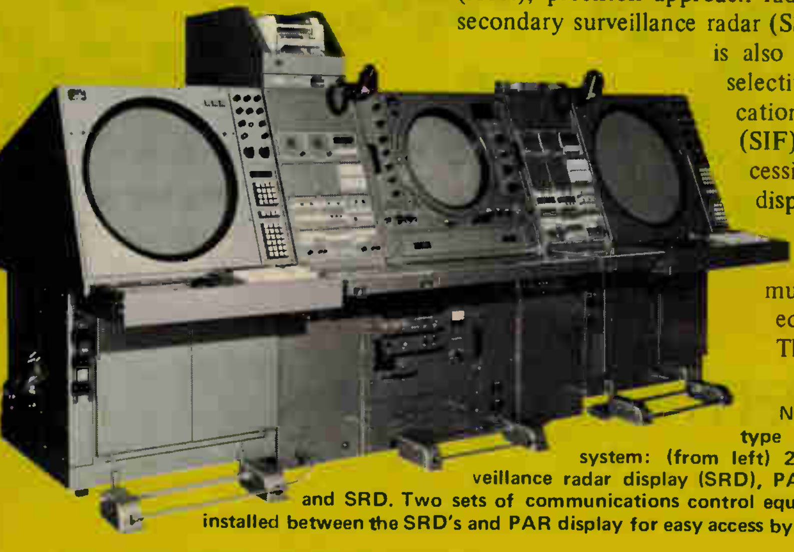
The standard DP-100 is provided with two channels and can be used by two operators at the same time.

The DP-100 Connected Speech Recognition System is a breakthrough in simplifying computer operations.

New GCA System Improves Air Traffic Control

To ensure air traffic safety in the face of ever-increasing amounts of air traffic, it is vital to modernize air terminal control facilities so as to improve efficiency in air traffic control as well as to reduce the workload of controllers.

NEC's new fixed type ground-controlled approach (GCA) radar system consists of airport surveillance radar (ASR), precision approach radar (PAR), secondary surveillance radar (SSR) which is also called the selective identification feature (SIF), data processing and display equipment, and communications equipment. The system features many state-of-the-art techniques for improved operation and maintainability such as outstanding clutter reduction by ASR digital MTI (moving target indicator) and LOG/CFAR (constant false alarm rate) system, digital PAR angle data generation and integration of map generator and display.



NEC's fixed type GCA radar system: (from left) 23-inch surveillance radar display (SRD), PAR display and SRD. Two sets of communications control equipment are installed between the SRD's and PAR display for easy access by controllers.

The system automatically detects and tracks beacon transponder equipped aircraft within its coverage. It then automatically correlates the aircraft with previously registered flight plans for a controller directing the airplane.

In this system, target symbols with a data block depicting call-sign, altitude and velocity data are displayed on a large 23-inch flat face CRT in a time-shared mode with raw radar video signals. A digitally generated map, departure and arrival list and system data are also displayed.

The NEC fixed type GCA radar system can cover an air space of 60 nautical miles and an altitude of 30,000 feet for a small jetfighter.

Brunei Telecoms Contract To Boost National And International Lines

NEC recently won a contract for a total of six electronic switching systems — five for central office use and one for international connections — from the Jabatan Talikom of Brunei.

The turn-key base contract, calls for NEC to manufacture, supply and install five ND-20 central office systems and one NXE-20 international switch in addition to managing the project. NEC will also train local engineers.

The five ND-20 systems will accommodate a total of 25,000 lines, and the NXE-20 ESS will provide high-grade 216 international circuits for rapidly growing Brunei.

The ND-20 is one of NEC's ND-series ESS's, and can accommodate up to 32,000 lines. It offers abundant software packages for both telephone switching and the corresponding support systems. By combining the required software packages, various customer calling services and basic telephone switching services can be made available.

The NXE-20 is also one of NEC's NXE-series stored program controlled international switching systems. It gives a line capacity up to 4,000 international circuits, and can be used as a toll or a combined toll and international switch.

System Information Display Board of the NXE-20 ESS.

NBC Orders Switchers For '80 Olympics

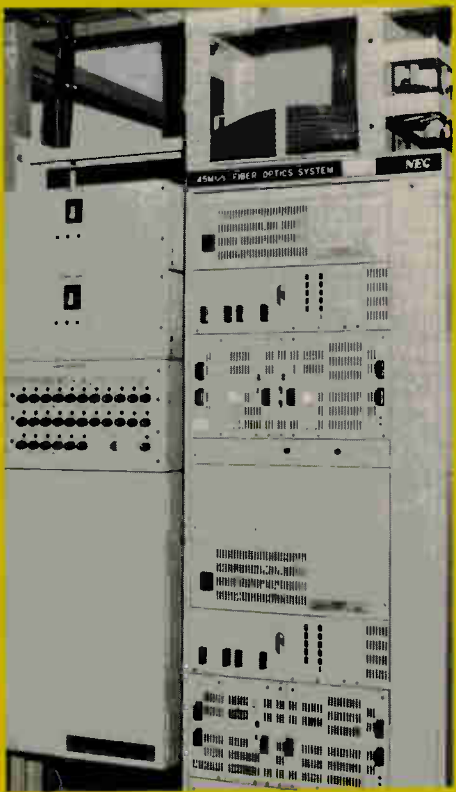
The National Broadcasting Company (NBC) of the U. S. has placed orders with NEC for audio/video routing switchers for broadcasting.

The switchers, NEC's Model TKA-105, will be installed first in Burbank near Los Angeles by June next year and thereafter in Chicago and New York. A portion of the equipment to be installed in Burbank will be transferred to the U.S.S.R. after the acceptance test to televise the Moscow Olympics.

The Model TKA-105 television switcher can handle 150 input signals and 270 output signals, the largest capacity model of its kind now available on the market. It incorporates many of the latest advances in electronic technology, including LSI switching devices to ensure low power consumption and high reliability.

NEC Optical Communications System Adds New Wonder At Walt Disney World

An NEC optical communications system was put into public service at Walt Disney World, Florida in July of this year.



The Vista-Florida Telephone System, a telephone operating company in Walt Disney World, installed an NEC optical communications system to link two telephone offices over a distance of about 9 kilometers in the famous resort complex.

The system is capable of transmitting information at a bit rate of 45 Mb/s or 672 telephone channels.

NEC systems use SELFOC glass fiber cables as thin as a strand of hair to transmit voice, data and video signals by means of laser light.

SELFOC is a light focusing glass fiber developed jointly by NEC and Nippon Sheet Glass Co. in 1968.

45 Mb/s fiber optics system carries operational traffic between two central offices.

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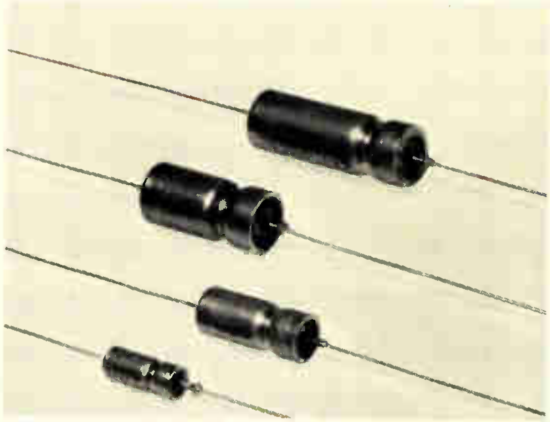
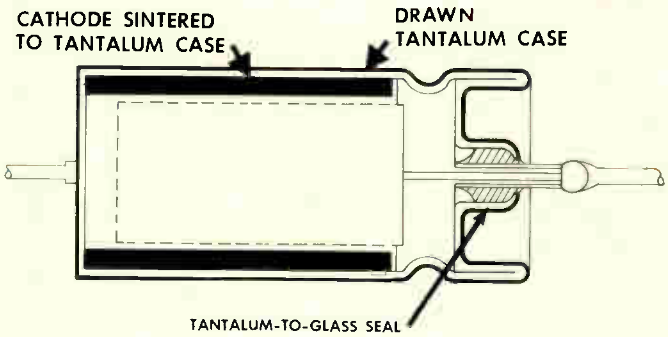


(Exceeds Standard MIL 20*g* Sinusoidal Requirements)



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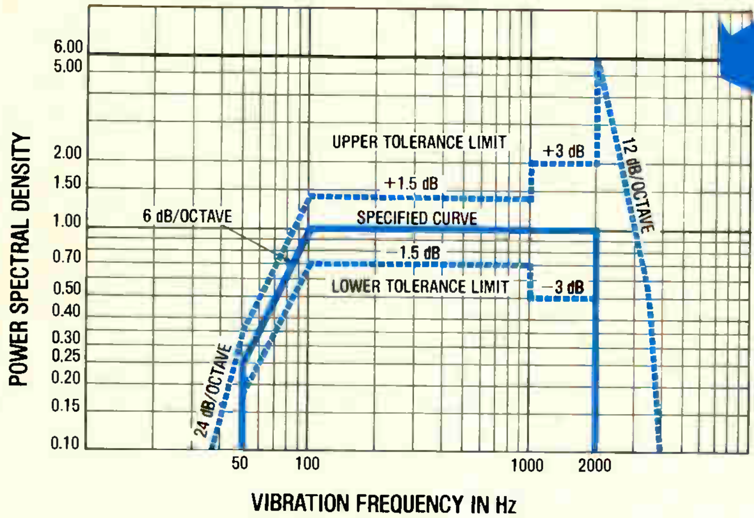

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Washington newsletter

Military buy-out of Motorola MECL-2 line proposed

The military intends to thwart Motorola's plan to terminate its long-established MECL-2 family of digital integrated circuits at the end of October. Its buy-out proposal would guarantee the company an estimated $2 million to $3 million in annual sales over an estimated two to three years until the services can fill their circuit requirements. Even though technology has leapfrogged MECL-2, which has been on the market for about a decade, **the circuits are "inexpensive and highly reliable,"** explains an Air Force Systems Command official.

The command coordinator of the proposal figures the price will be "five to six times" less than redesigning the systems that use MECL-2, since there are more than 40 basic chips in the series with some 400 military parts numbers involved. The Defense Electronics Supply Center in Dayton, Ohio, will act as buyer for all three military services under the plan. A prime MECL-2 user is the Air Force E-3A Advanced Warning and Control System. The Awacs surveillance command and control communications aircraft, with its large Westinghouse rotating radar dome, has an estimated 2,500 MECL-2 parts. Other military systems using the circuits include simulators, tactical air navigation packages, and fuzes.

Mainland Chinese show satcom interest in U. S. visits

The People's Republic of China is expressing strong interest in developing its own satellite communications network, possibly using American technology. That is the impression being left by a six-member delegation headed by Shau Wen-hau now visiting 12 plant sites of seven U. S. electronics companies on both coasts. Shau directs the Communications Engineering Institute's microwave department in Peking; the Electronic Industries Association is sponsoring the three-week visit. The EIA's John Sodolski, Communications division vice president, says **the delegation expressed particular interest in satellite earth stations and test and measuring equipment.** When the tour is completed on Oct. 30, the Chinese will have visited California Microwave, Digital Equipment Corp., GTE Sylvania, Hewlett-Packard, ITT, RCA, and Scientific-Atlanta.

U. S. eyes extension of import controls to most color TVs

The White House wants to extend color TV import controls to Taiwan, Korea, Mexico, and Singapore. The decision was triggered by strong complaints from Japan and a coalition of U. S. labor and industry that **increased imports from those four countries are more than offsetting restraints on Japan** under the Orderly Marketing Agreement that took effect last year. Taiwan and Korea, with the largest color TV shipments to the U. S. after Japan, will be asked by White House trade specialists to curb shipments to the U. S. Both Japanese and American TV makers have manufacturing operations in the two Asian countries.

Compact—the Committee to Preserve American Color TV, a heavily labor-oriented organization with three company members led by cathode-ray-tube-envelope maker Corning Glass Works—estimates imports of completed sets will rise nearly 10% this year to 2.7 million sets, despite a decline of 18% in Japan's shipments from last year to 1.6 million. Compact estimates that 1978 imports from Taiwan will total 581,000 sets, nearly double last year, and will increase another 66% in 1979 to 975,000 if not controlled. Korean totals will hit 265,000 this year, nearly triple the 1977 total, and reach 460,000 in 1979, Compact says. Overall 1979 imports could rise 22% to 3.3 million for completed sets.

Washington commentary

Can VHSI succeed where other standards have failed?

The nation's three military services are close to selecting the six systems they will use for brassboard demonstrations of the large, very high-speed integrated circuits that are to be competitively developed over the next six years under the Pentagon's $200 million VHSI program [*Electronics*, Sept. 14, p. 81]. Each service will select and fund demonstrations of VHSI in two systems, according to the plan now being refined by the Department of Defense.

The Navy's selections, for example, reportedly include a 10-hertz digital spectrum analyzer for processing electronic intelligence aboard aircraft and spacecraft, plus a jam-resistant, low-power spread-spectrum communications system for use on airplanes and spacecraft as well as on small missiles and remotely piloted vehicles. The Air Force contemplates using VHSI to achieve three-dimensional terminal guidance on its Cruise missile, for airborne synthetic-aperture radars, and electronic warfare radar-pulse processors capable of handling 1 to 10 million pulses per second, as well as wideband satellite links with data rates of 1 gigabit per second. The Army's options include data correlation for over-the-horizon targeting and fire control and mobile tactical signal intelligence systems.

There are other potential applications, of course. An important one is antisubmarine warfare where a greater number of signals from satellites and aircraft can be correlated to detect and locate hostile boats better.

A question of volume

The military's long list of possible VHSI applications is already raising questions in industry both about the number and type of circuits it will be asked to produce and about the length of circuit production runs for a customer—the Pentagon—that regularly replaces one system with another before the first is fully deployed. For VHSI to succeed without busting the military budget, program advocates within DOD and industry agree that circuits will have to be turned out in large volumes on highly automated production lines.

J. Fred Bucy, president of Texas Instruments Inc. of Dallas, is one such advocate. He is convinced that DOD must change its approach to military electronics procurement and deployment if VHSI is to attract industry's best talent. He laid what he calls his "systems roadmap" before the Institute of Electrical and Electronics Engineers's Electronics and Aerospace Systems Conference late last month in Washington.

First, the military must substitute evolution for revolution in weapons development if it wants to achieve the volume production that is a prerequisite for design-to-cost disciplines, Bucy contends. Second, he believes the three services must subordinate special system performance goals and promote instead VHSI "function standardization" that will permit development of a family of digital subsystem modules or building blocks that "could roll over several times within the lifespan of a weapons system."

Will perspective change?

The military services—and a number of their contractors—may find it harder to set aside their biases in favor of custom-tailored hardware than the semiconductor industry expects to find it to advance the state of the art. Many military leaders remain convinced that commonality means compromise, which they insist equates with second-best. Some contractors, too, see commonality as a threat to their ability to lock the customer into a commitment to their particular products and services.

TI's Bucy admits that his "systems roadmap" for planned evolutionary improvement for weapons, rather than replacement, will require "a change of perspective" on the part of the services. But he notes that evolution can be successful, citing such varied systems as the Sidewinder air-to-air missile and the TOW anti-tank weapon, as well as the Paveway laser-guided bomb.

Bucy believes that systems evolution will be required if VHSI and design-to-cost concepts are to succeed. "Design-to-cost works in consumer electronics, in commercial electronics, and it will work in military electronics," he insists.

If VHSI can be made to work, it will be because the technologists have been able to come up with volume-production circuits of such complexity that military users will not have to sacrifice performance for price and will be able to introduce improved modules into weapons without going through a complete redesign.

The greater part of the VHSI burden, then, rests on the design engineer. "In implementing a functional module approach across all DOD weapons systems, perhaps one of the greatest problems is not one of procedures and funding, but a culture problem," Bucy concludes. "Until it becomes second nature for equipment designers to think 'modular digital functions,' we cannot maximize the impact of microprocessors and standard architectural approaches."

Ray Connolly

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Circle 59 on reader service card

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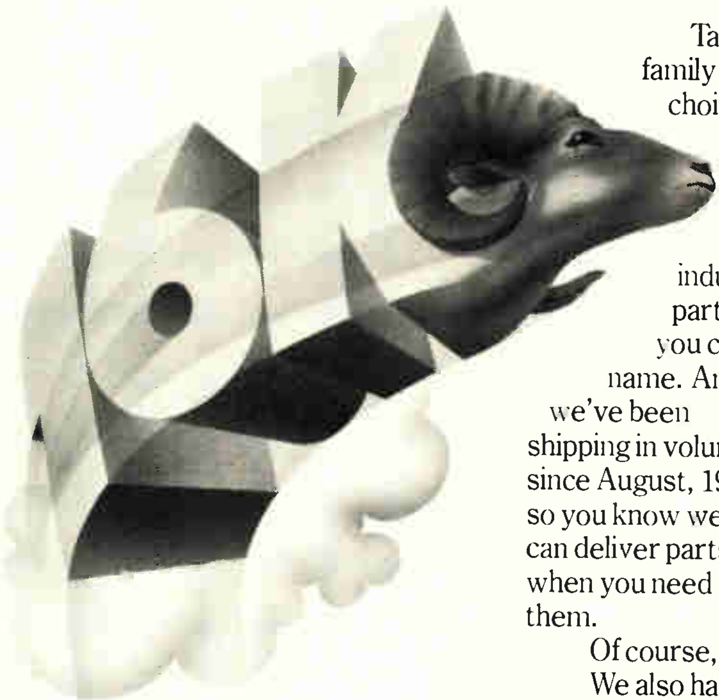

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P/N	t_{RAC}	t_{RC}	I_{DD1}	I_{DD2}
μPD416-5	120 ns	320 ns	35 mA	1.5 mA
μPD416-3	150 ns	375 ns	35 mA	1.5 mA
μPD416-2	200 ns	375 ns	35 mA	1.5 mA
μPD416-1	250 ns	430 ns	35 mA	1.5 mA
μPD416	300 ns	510 ns	35 mA	1.5 mA
t_a = 0°C to +70°C				

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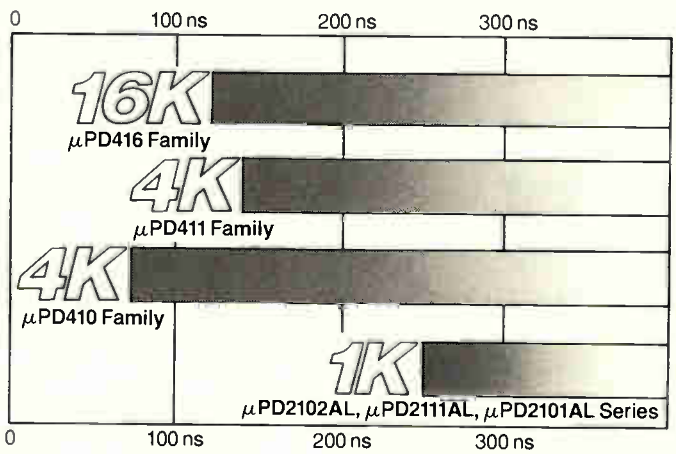

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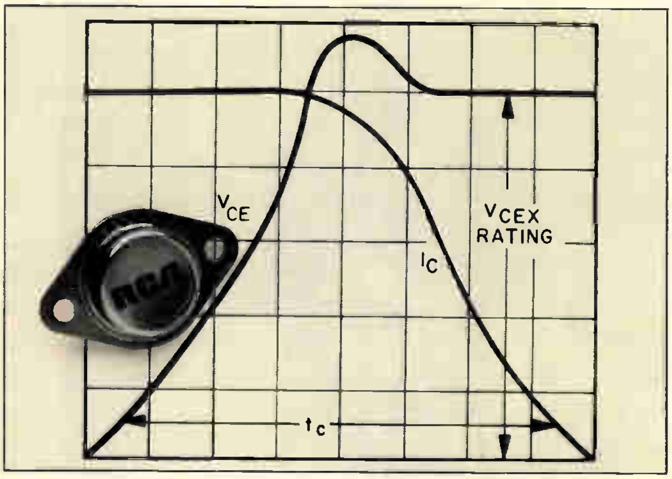
SwitchMax. A new series of RCA transistors designed and built for high performance in off-line power supplies, converters, and pulse-width-modulated regulators. SwitchMax transistors are hot-temperature tested. To give you new predictability under operating conditions. New efficiency in heat sink design.



Performance that starts with design. These RCA n-p-n transistors have a multiple-epitaxial, double-diffused structure, fine emitter geometry, and a trimetal system. Which make SwitchMax transistors rugged. And give them excellent high-current and fast switching characteristics, with improved second breakdown.

Types	V_{CEV} Rating	I_C (sat)	t_c (max) at I_C (sat) µs
2N6671 2N6672 2N6673	450 V 550 V 650 V	5 A	0.4 (25C) 0.8 (125C)
2N6674 2N6675	450 V 650 V	10 A	0.5 (25C) 0.8 (100C)
2N6676 2N6677 2N6678	450 V 550 V 650 V	15 A	0.5 (25C) 0.8 (100C)

Verified by worst-case testing. Every SwitchMax transistor is tested at 100° C or 125° C against precise limits for all switching parameters. Including inductive turn-off time and saturation voltage. To give you switching characterization that lives up to RCA's reputation in second breakdown, safe operating area, and thermal cycling ratings.

As the table shows, SwitchMax transistors cover a wide voltage and current range. Send for our brochure detailing how to use them in your designs. Contact your local RCA Solid State distributor. Or RCA Solid State headquarters in Somerville, NJ; 1130 Brussels, Belgium; Sunbury-on-Thames, Middlesex, England; Quickborn 2085, W. Germany; Ste.-Anne-de-Bellevue, Quebec, Canada; Sao Paulo, Brazil; Tokyo, Japan.

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Circle 62 on reader service card

International newsletter

Projection aligners for E-beam masks set for production

Dropping the other shoe, Japanese VLSI researchers are showing how they intend to project the semiconductor masks fabricated by the electron-beam process they are developing. They are unveiling two fine-pattern step-and-repeat projection aligners that will give highly precise optical exposure. **The machines will be made by Canon Inc. and Nippon Kogaku KK (Nikon), which developed them for the Cooperative Laboratory** of the very large-scale integration project [*Electronics*, June 9, 1977, p. 101]. The Canon aligner has same-size projection optics with a 2-by-2-in. mask that exposes a 30-by-30-mm area with a minimum line width of 2 μm. The Nikon aligner has 10:1 reduction optics with a 4-by-4-in. reticle of a full-chip pattern that exposes a 10-by-10-mm area with a minimum line width of 1 μm. Step-and-repeat aligners will be required for VLSI because a full-wafer unit cannot obtain the necessary fine-line patterns.

British digital recording method heads for TV studios

Digital video recording in TV studios may be coming soon: West Germany's Bosch and Japan's Sony are planning to buy licenses to a British technique that overcomes the problem of excessive tape consumption. Developed by the Independent Broadcast Authority, **the technique records color TV pictures on 1-in. magnetic tape at speeds below 10 in./s** at a rate of 80 million bits per second, with no bit-rate reduction of the picture information. Digital recording eliminates the loss in picture quality that occurs when successive analog recordings are made during editing, because even severe tape noise will not affect detection of digital pulses.

Electronica to see Siemens 32-K ROM . . .

Look for Siemens AG to unwrap a 32-K read-only memory at the Nov. 9–15 Electronica show in Munich. Designated the SAB8332, the static MOS memory uses n-channel depletion technology, **has an access time of 450 ns, and dissipates a maximum of 330 mW.** The mask-programmed memory, with 4,096-by-8-bit organization, comes in a 24-pin dual in-line plastic package and operates off +5 V.

. . . and IC kit for digital tuning on TV sets

Also using Electronica as a stage for launching new products is Intermetall GmbH. Among the firm's novelties is an integrated-circuit kit that can be assembled into a frequency-synthesizer, phase-locked-loop digital tuning system for TV receivers. **The five-circuit kit also can implement program storage, automatic station search, and on-screen display of the channel number.** Combined with Intermetall's infrared remote-control system, the kit provides the building blocks for a setup that affords wireless control of TV games and similar upscale features.

$4,000 computer for small firms packs in features

Jumping into the market for small-business computer systems is Toulouse-based Société Occitane d'Electronique, with a unit that offers as much or more for its low price than comparable systems from even the big U. S. firms. The $4,000 X1 is available with special-purpose software for the medical and other professions and **includes 8 kilobytes of memory, two minifloppy disks, a keyboard with function keys, and a 12-in. display** showing 24 rows of 80 characters. A specialist in TV games, the French company uses Motorola 6800s in its new venture. Next in the cards: a bare-bones $1,000 system for personal computing and the like.

International newsletter

Grooveless disk planned for video and digital audio

Under development at the Victor Company of Japan (JVC) is a simple-to-fabricate, low-wear grooveless disk for stylus playback of video and digital audio recordings. JVC claims its scheme is an improvement over earlier stylus schemes and is a better solution than complex optical pickup by laser beams [*Electronics*, Nov. 24, 1977, p. 78]. **Elimination of the grooves permits a stylus with a large tip area for negligible wear of disk and stylus.** It also gives the stylus easy, rapid access to a desired track. Signal pickup is by capacitance variation between a narrow conducting strip on the stylus's trailing edge and the surface of the disk. Narrow auxiliary tracks provide a servo signal that keeps the stylus tracking properly. JVC uses conductive plastic for its disks, so a single pressing operation with no plating or other secondary operations is all that is necessary, just as in conventional audio records.

UK car makers going electronic for fuel, ignition control

Tough U.S. anti-pollution regulations are at last spurring UK automobile manufacturers to make the move to more efficient electronic fuel- and ignition-control systems. However, they are not yet combining the two systems, as are American car makers. At least three models slated for a mid-1979 launch will use **the Lucas digital fuel-injection system, which incorporates two custom chips from Ferranti Semiconductors Ltd.** [*Electronics*, July 8, 1976, p. 153 or 4E]. Meanwhile, Hughes Microelectronics Ltd. is working with Zenith Carburetter Ltd. on a low-cost electronically regulated carburetor system that monitors exhaust gases with a zirconium-dioxide transducer. It will be used by British Leyland on some export models. Also, Hughes is developing an electronic advance-retard mechanism that typically adjusts the ignition firing angle over 12° to 60° and works with rotor, reed-relay, or double-ended-coil ignition systems.

VCR makers in Europe plan production hikes

European production of video cassette recorders is shifting into high gear now that West Germany's Grundig AG has opened a VCR plant in Nuremberg and N. V. Philips Gloeilampenfabrieken of the Netherlands plans to concentrate its VCR production in a single facility in Austria. At Grundig's 30,000-m^2 plant, built for a daily output of some 1,000 VCRs, production already is at a level of roughly 400 units a day, and **"we are selling them as fast as they come off the assembly lines," a company official says.** For its part, Philips has earmarked about $135 million for a new facility in Vienna that will employ about 3,000 workers by 1980. Daily production, most of it slated for export, likely will exceed Grundig's by a good margin. As for West Germany's VCR market, Grundig pegs total sales this year at 85,000 units and next year at 150,000.

Amdahl chalks up two more UK orders

Europe is proving a rich hunting ground for Amdahl Corp. of Sunnyvale, Calif. The eight-year-old maker of IBM-compatible computers has snared a $14 million order from British Airways, a major IBM customer for 15 years. **The contract for four Amdahl 470 computers follows quickly on an order for a 470 V/5 from Ford of Britain.** Amdahl now has 16 big computer installations in Europe. To meet further European commitments, it has opened a manufacturing plant in Dublin.

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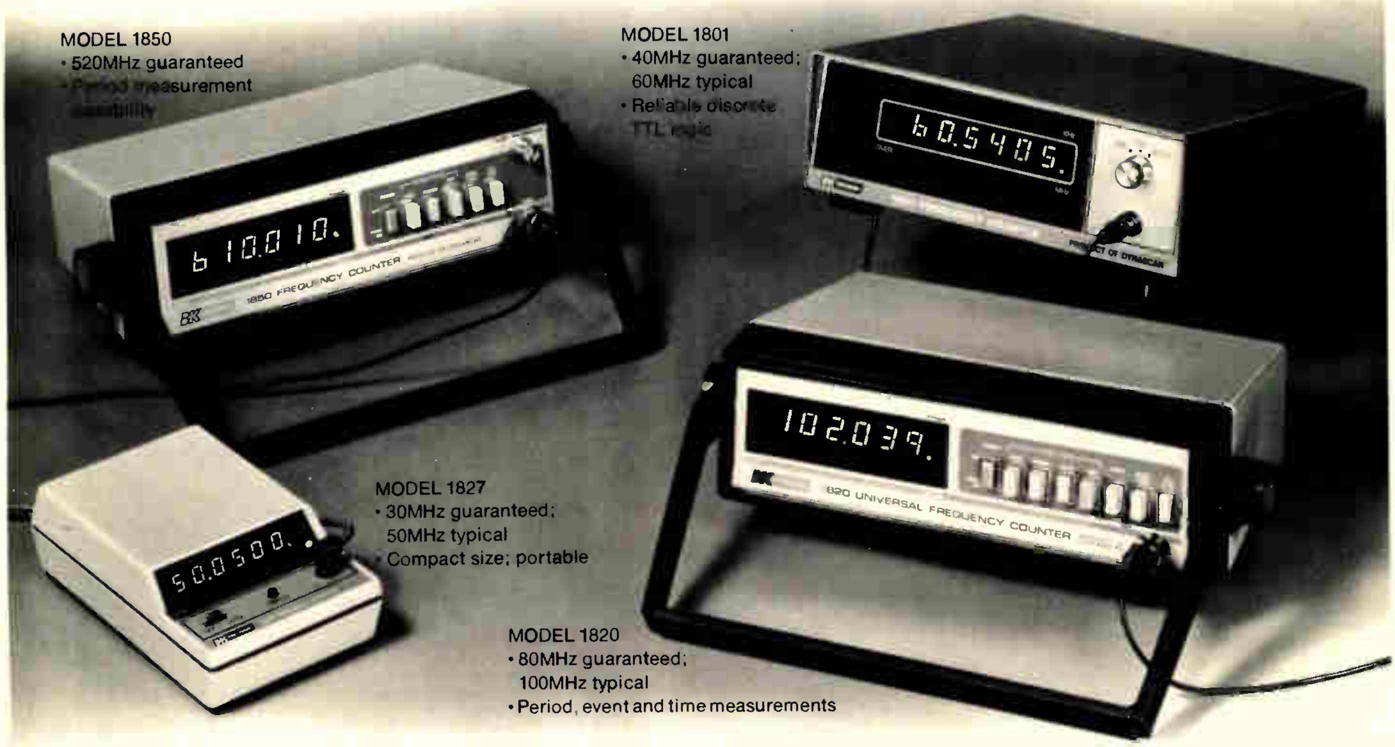

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Circle 66 on reader service card

LSI chip provides 600-gate array in semi-custom setup

Metal-oxide-semiconductor IC can replace whole boards of transistor-transistor logic and operate as fast or faster

Gate arrays may have been overshadowed by the rush to microprocessors for logic tasks, but the LSI wizards at Mitsubishi Electric Corp. are transforming these subsystems of small- and medium-scale integrated circuits into a large-scale integrated array. What's more, the company is offering semi-custom metal-oxide-semiconductor chips that can replace whole boards of transistor-transistor-logic SSI or MSI arrays, while operating as fast or even faster.

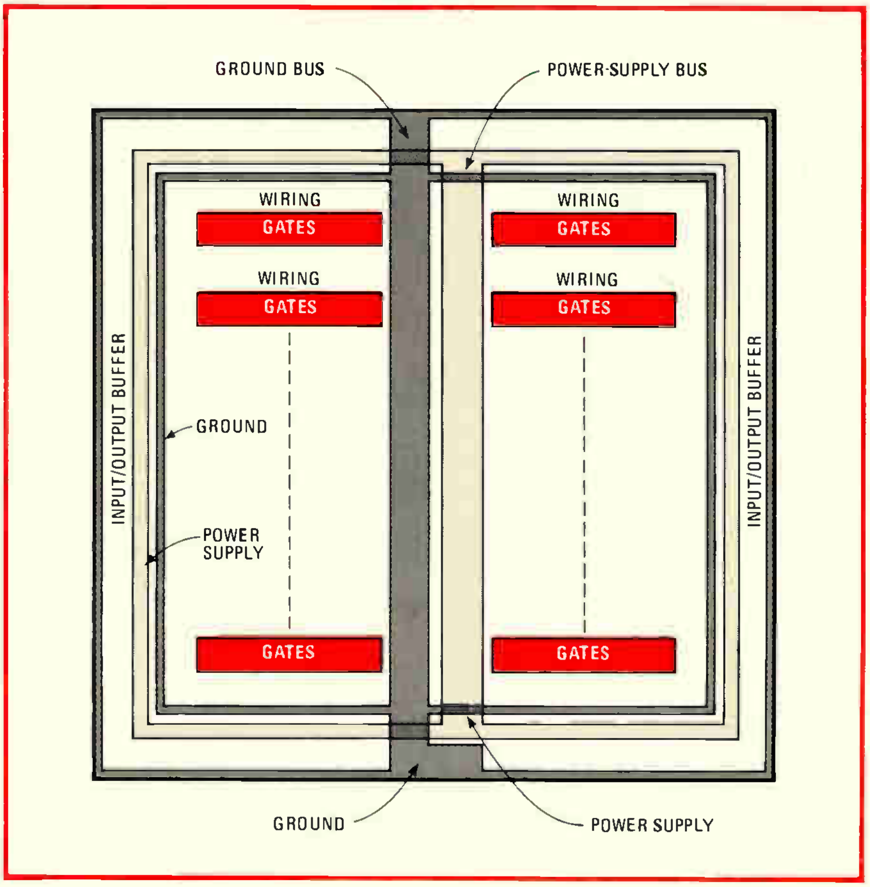
The company's Kitaitami plant near Osaka uses computer-aided design for the double-level aluminum layers that are added to partially processed wafers. Operating from a single 5-volt supply, each chip has 624 three-input NOR gates and 80 buffer gates (20 for input only, the rest for input or output).

Replacement. In practice, an array can replace one or two printed-circuit boards with numerous ICs providing up to 600 gates. In many applications requiring even more gates, one chip plus a few judiciously chosen additional standard TTL circuits will replace 10 or 20 of the MSI devices. Either way, there will be great savings in circuit-board area and power consumption, as well as in assembly costs.

The semi-custom IC array is economical in quantities of 1,000 to 100,000 pieces. For larger quantities, custom design would cost less, although delivery would take many times longer. For the one-time work, the firm charges about $18,000, with a 1,000-lot price of about $42 per 68-pin package. Also available are 40- and 84-pin packages.

Mitsubishi handles all development, including simulation and working up a test program, by computer-aided design after the customer gives logic specifications. Fast delivery of samples—four to six weeks after the receipt of specifications—is possible because CAD speeds up design and testing, and the wafers require only the addition of two levels of aluminum interconnections and packaging.

The diffusion self-aligned process Mitsubishi uses was first announced in Japan 10 years ago [*Electronics*, Oct. 13, 1969, p. 207], but this is its first application to high-speed general-purpose logic. In this process, it is



From one, many. Mitsubishi uses this master chip to provide semi-custom large-scale integrated gate arrays to customer specifications. Two levels of aluminum interconnections and bonding pads are added to the integrated circuit, which has 624 three-input NOR gates.

possible to reduce effective channel length to about a tenth that of standard MOS circuitry for higher speed at lower power. Mitsubishi engineers say that effective channel length in their new LSI devices is only 0.5 micrometer.

High-speed and low-power versions are available, both of which are compatible with TTL input and output levels. The output can be totem-pole, open-collector, or three-state, and the user may specify an inverting or noninverting output.

The specs. The high-speed type has an average propagation time of 2.6 nanoseconds and a power consumption of 5 milliwatts per gate. Specs for the low-power type are 4.9 ns and 2 mw. These speed-power characteristics must be balanced with the choice of package; dissipation ratings are 1, 1.5, and 3 watts for the 40-, 68-, and 84-pin packages respectively.

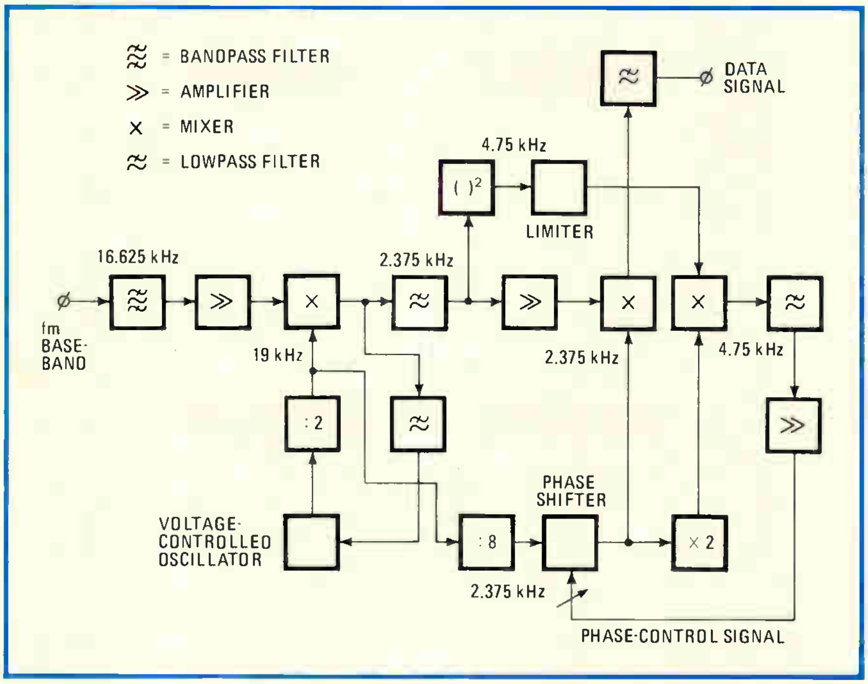
Both chips are a large 6.28 by 6.60 millimeters, but active circuits cover only about 30% of the area because of the generous space left for interconnections. This compares to the typical MOS chip's 70% active circuitry. With loss during processing almost proportional to active area, yield for the new chips is equal to that of conventional ICs less than half their size. □

The Netherlands

Digital signal accompanies fm broadcast to give station information to the listener

An fm receiver showing the listener to what station he is listening, its transmitter's location, and the type of music being broadcast may be in the cards for European radio owners. The Philips Research Laboratories, working with the Dutch broadcasting corporation NOS, has come up with a scheme to do just that.

The information on the cathode-ray-tube display of the SPI system (for station program identification) comes from a code transmitted with the regular fm signal. In the still experimental system, display and code-demodulating circuitry are in their own module, but circuit miniaturization will fit that module right into the receiver.



Showoff. Dutch-developed circuit for fm receivers demodulates a 16.625-kHz signal, transmitted with the regular broadcast signal, to provide a readout of tuning information.

The Philips/NOS system is designed to make fm tuning as easy as is European a-m tuning, where the station names or call letters are given on the dial. There are too many fm stations to show these, so the dial gives only frequencies or channel numbers.

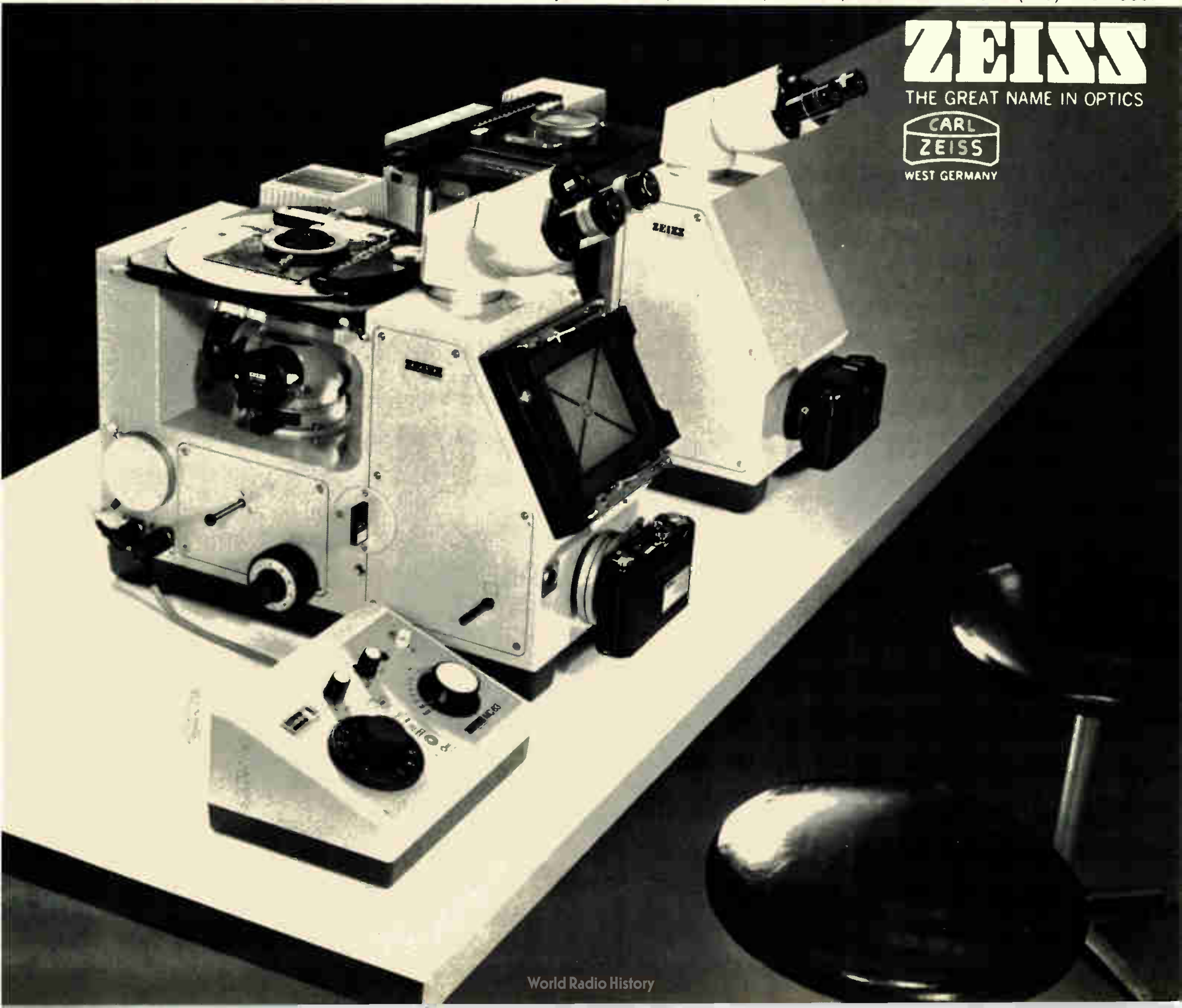
The SPI display would supplement this; in fact it would give the fm listener more information than the a-m listener now gets. It was described at the International Broadcasting Convention in London late last month by its principal developer, Johannes B. H. Peek of the Philips labs in Eindhoven, the Netherlands.

Interest. Although the SPI system is not just around the corner, it is no pipe dream. About a dozen experimental receivers are undergoing trials in Holland, France, the UK, and West Germany, Peek says. "In a survey it has conducted, the European Broadcasting Union has found that a definite demand exists for some kind of fm station-identification scheme," he says.

The code or bit pattern that produces the display information is transmitted at a rate of 640 bits per second. In station tuning, the radio user can spot a maximum of five displayed messages a second. With such a rate and with each message consisting of 16 7-bit characters plus one 16-bit start code, the transmission rate works out to 640 b/s.

The Philips/NOS designers chose a subcarrier of 16,625 kilohertz to transmit the code, because this frequency causes virtually no interference in the receiver. For as few errors as possible for a given signal-to-noise ratio, they decided on a phase-shift-keyed circuit to demodulate the code from the subcarrier. After appropriate demodulation (see figure), the data is recovered from the subcarrier and applied to the display circuitry.

Signals. As co-developer Johan M. Schmidt of the Philips labs explains



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it, the fm-baseband signal consists of the mono, stereo, 16.625-kHz subcarrier, and 19-kHz pilot signal, the last being typical for fm stereo broadcast. The subcarrier and the pilot signal are filtered out for a better signal-to-noise ratio and to avoid possible interference with audio signals in the neighborhood of 50 kHz (about the third harmonic of the 16.625-kHz signal).

Then the 19-kHz pilot signal is recovered in a phase-locked loop and mixed with the subcarrier signal to yield the SPI signal of 2.375 kHz. Two 4.75-kHz signals are produced, one derived from the 2.375-kHz signal by squaring and the other from the 19-kHz signal by frequency division and multiplication.

The 4.75-kHz signals are compared, and their respective phase shifts are automatically adjusted to zero. This phase control causes the 2.375-kHz frequency to have the same phase as the suppressed carrier, so that this signal can now be demodulated. The data signal so obtained is then filtered and processed for driving the display. □

Great Britain

Military manpack single-channel repeater exploits new fm signal-nulling technique

With more and more messages taking to the airwaves, more and more antennas are being clustered into smaller and smaller spaces—so considerations such as frequency-nulling techniques assume a new importance. A new nulling technique from Plessey Avionics and Communications Ltd. is the basis for a single-channel repeater aimed at military vhf communications systems. The unit replaces enough equipment to fill a Land Rover.

The firm's new Groundsat repeater permits operation of receiver and transmitter repeater units at the same frequency at the same site. The problem with one-channel repeaters has been that the transmitter output can swamp the incoming signal, creating a giant oscillator. This effect has been a big headache in mobile radios especially.

Answers. One solution, found in commercial mobile radios, is to position highly directional antennas so as to avoid the interference. Military users of mobile radios cannot bank on such careful antenna siting, so, at a great loss of operational flexibility, their repeaters use differing transmitting and receiving frequencies.

Single-channel. Plessey's new Groundsat repeater unit, shown in simulated army maneuvers, permits a vhf mobile system to operate easily over distances on a single frequency.

Plessey engineers are unwilling to disclose details of their breakthrough, apart from saying that the technique only works with angle-modulated systems. Rebroadcast ratios of greater than 100 decibels are possible using omnidirectional whip antennas separated by 20 meters.

But the technique has more in hand, and its inventor Chris Richardson says it could be developed to a point where both transmitting and receiving antennas could be mounted on a vehicle. Such a mobile repeater station could have military and civil applications.

A demonstration of the system convinced the UK Ministry of Defence of its great operational potential. It plans to buy equipment for field trials.

Operation. The 30-to-76-megahertz Groundsat repeater is usually operated in the single-channel simplex mode. Control of the repeater can be seized by a call-tone facility attached to each radio. After a set message interval, the repeater reverts to standby. Since the base station and any mobile unit can gain access to the repeater, it is well suited to unmanned operation.

Single-frequency duplex operation is also possible when two Groundsat repeaters are deployed. A unit can be used like a conventional manpack radio while a soldier is lugging it to an operating site.

Transmitter output power is 1 watt, while receiver sensitivity is typically 1 microvolt. The 24-volt rechargeable battery pack allows unattended operation in excess of 15 hours. □

EMI takes aim at the competition

With sales of its computerized X-ray scanners sagging badly, EMI Ltd., the company that invented the technology in 1972, is on the attack with five new scanners designed for a more cost-conscious market. Moreover, it is combining this attack with

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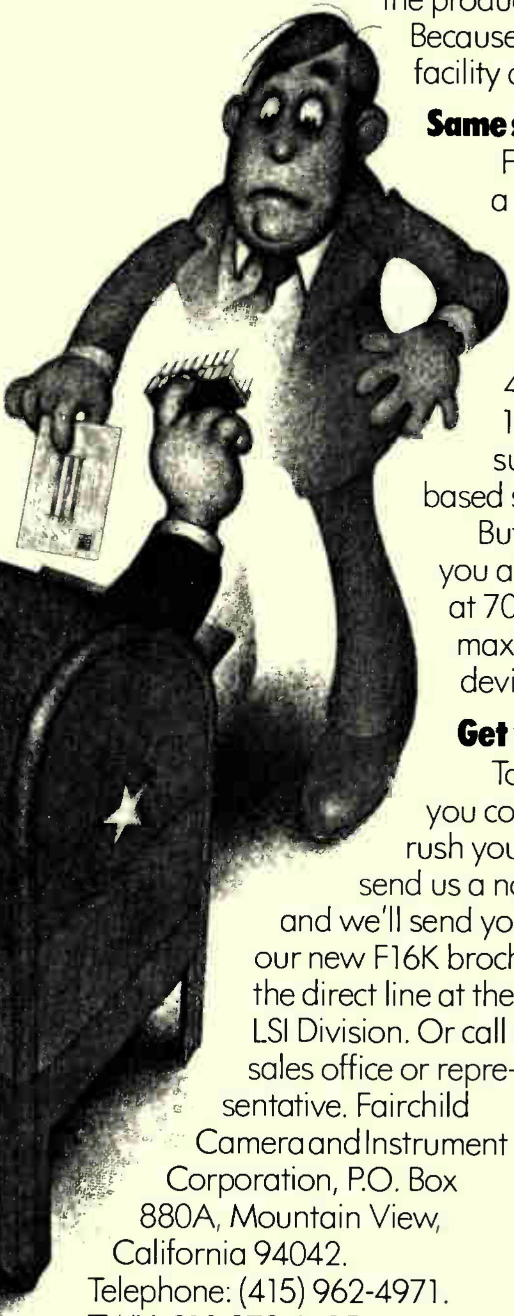

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aggressive pursuit of a patent-infringement campaign.

The root cause of the company's problems lies in the cost restraints on medical technology in the U. S. that have affected the entire market in computerized axial tomography. At the launch of the new family, EMI chairman Sir John Reed said that the U. S. market is looking "a little more hopeful" since Congress' rejection of Government control of health-care costs in favor of a voluntary scheme put forward by the medical profession and hospitals.

Choices. Even so, with more and more companies entering the market, EMI no longer has things all its own way. To meet the competition, its new series eschews the general-purpose approach to offer a spectrum of choices tailored to specific applications. The 7000 series ranges in price from $247,000 to $1.04 million, compared with the previous basic price of $370,000.

The five distinct users EMI addresses in the new range are:

- A research and teaching hospital with a need for high throughput.
- A cancer-treatment center concerned with the precise location of tumors and the planning and monitoring of a course of therapy.
- The accident unit of a general hospital, with a low, sporadic caseload mostly of head injuries.
- The general hospital with a heavy caseload that includes a wide range of conditions in the body and head.
- A neurological clinic with a substantial workload of head and neck diagnoses.

Top of the line is the 7070 general-purpose scanner for advanced research and teaching hospitals. It offers a 3-second scan time, compared with 18 s for earlier models, without sacrificing image quality. The reduced scan times are achieved by the use of a rotate-nutate mechanical scanning system (shift the detectors) instead of the more conventional rotate-translate system (shift the patient).

However, the increased speed is bought at the expense of a 1,000-detector array scanning the patient's body, instead of the 30 detectors in earlier models. This increase pushes the price to above the million dollar mark, so the potential increase in patient throughput can be exploited only in big teaching hospitals where economies of scale are possible.

Also a new development is the integrated therapy system, which can locate a tumor precisely and plan and monitor a course of X-ray therapy. Working directly off the scan image and using a light pen in conjunction with a color display on a special adaptation of the basic console, the operator can plot beam paths and dosage levels in seconds.

Moves. The company has already booked 30 orders for systems in their new range. Moreover, it recently took over the CAT body-scanner line from G. D. Searle & Co. of Skokie, Ill. This wider-beam but lower-resolution rotate-rotate system offers a 5-s body scan and fits into the range between the 18-s and 3-s scanners.

With some 500 patents worldwide, the British company is also taking another tack in its struggle to stay on top of the CAT-scanner market. It is well embarked on a court campaign against U. S. manufacturers it claims are infringing its patents. In 1976, it filed suit against Pfizer Inc., followed with another against Ohio Nuclear Inc., and last month took the General Electric Co. to court.

If its infringement cases are successful, royalties and any sales boost from the new range could help reverse the medical division's setbacks. The present order book, for example, stands at less than 100 machines, compared with peak sales of 470 systems at $400,000 a unit back in 1975–76. A loss of around $10 million is likely this year. □

Clearing the air with electronics

Electronic monitoring systems that trigger an alarm when specific limits of certain air pollutants are exceeded are simple-minded devices: they serve as sentinels and nothing else. Now there's a move afoot to provide systems that report pollutant levels in the parts-per-million range and control the operation of ventilation fans and the like, as well as setting off alarms.

A Swedish company, Ingenjoersfirma Harry Rudberg AB, has redesigned the amplifier end of its electronic monitor to add the functions. Owner Harry Rudberg says that so far only more expensive monitoring systems using infrared absorption technology have offered these functions.

In Rudberg's 7000 UF and 8000 UF, electronic sensors provide a logarithmic output signal, which passes through a three-stage operational-amplifier unit to produce a linear signal. It may be produced as a 0-to-10-millivolt output for a dial or a paper or chart recorder and as a 0-to-1-milliampere signal for process control: starting or stopping fans, valves, or ventilating units, and so on. A separate op amp triggers the alarm.

In the initial versions, each electronic unit can serve three sensors, which may be as far as 1,000 meters away. Rudberg says this is a great advantage over the IR systems, which operate by drawing air or gas to the central analyzer and so are limited to a range of 50 m or so. He claims that the purchase price is about half that of IR units. A system consisting of one amplifier unit and one sensor costs about $1,000 in Sweden.

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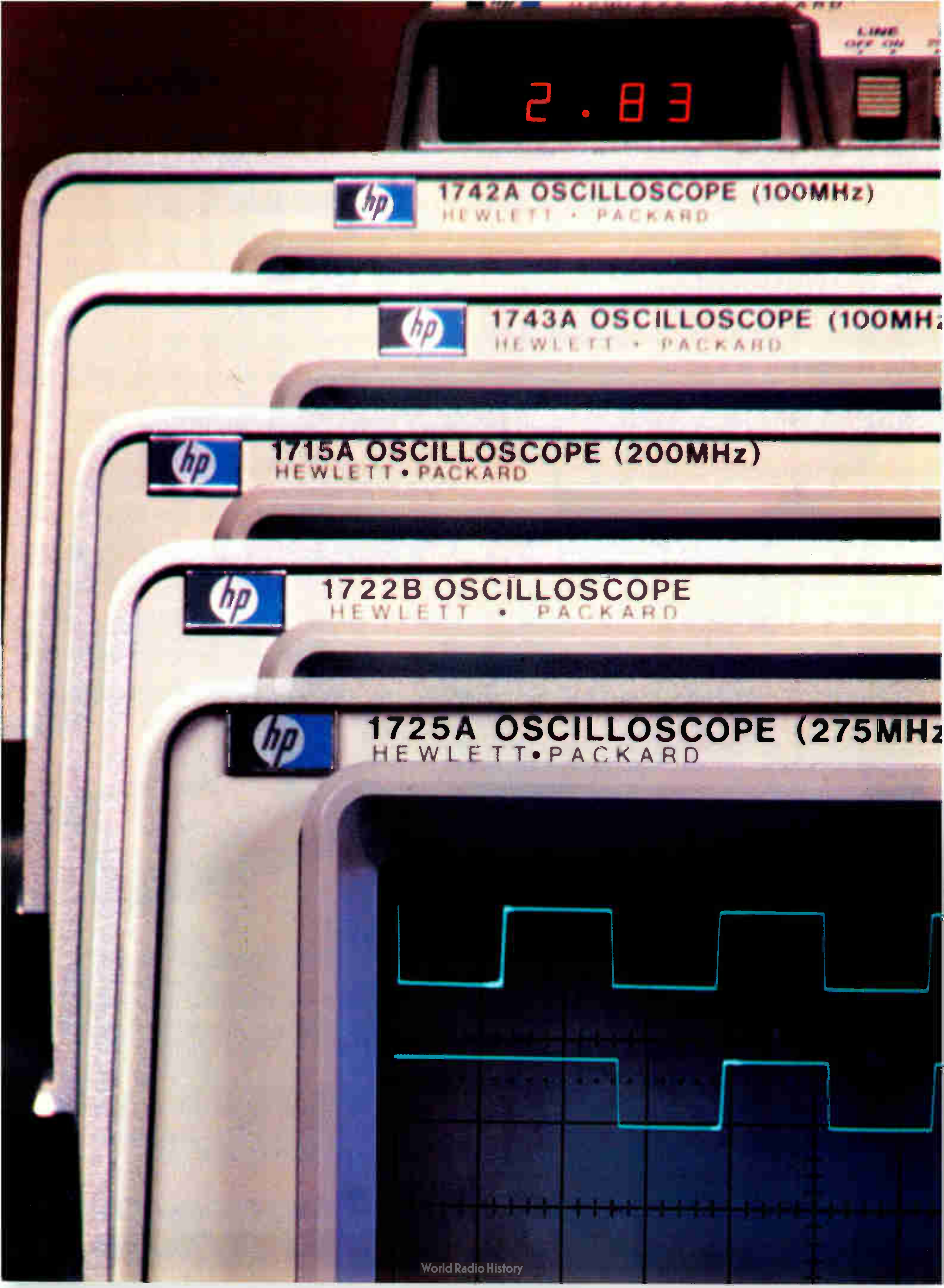
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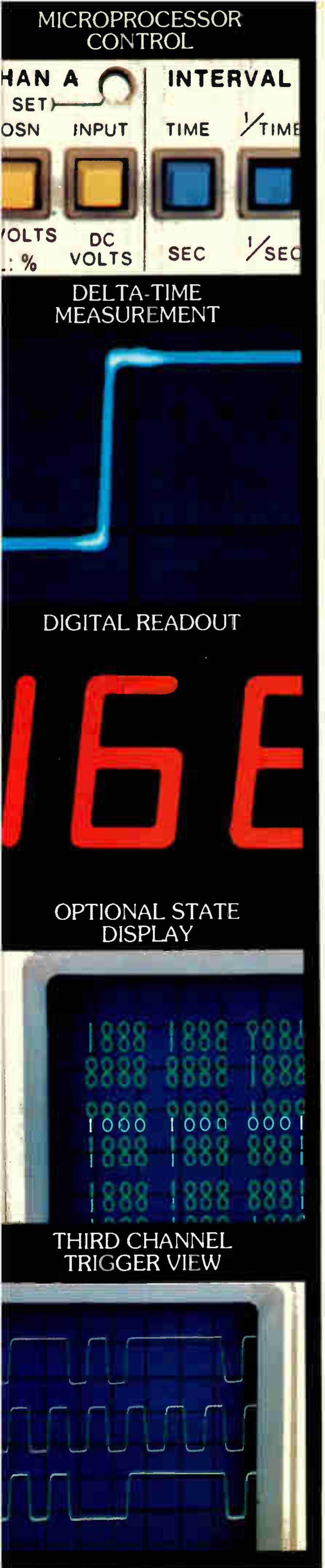

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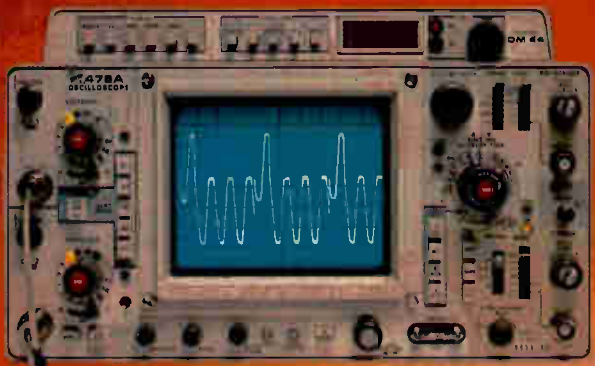

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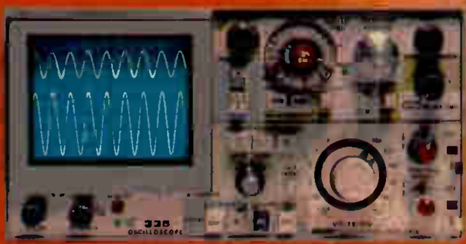

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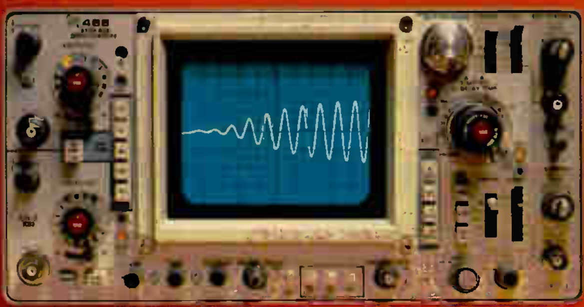

466

465M

	Product	Bw	Dual Trace	Delayed Sweep	Fastest Sweep Rate	Other Special Features	Price*
Storage Models	466	100 MHz @ 5 mV/div	yes	yes	5 ns/div	2000 div/μs stored writing speed	[illegible]
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	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	[illegible]
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)	[illegible]
	214	500 kHz @ 10mV/div	yes		1 μs/div	Only 3.5 lbs (1.6 kg)	[illegible]
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	[illegible]
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	[illegible]
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250-MHz portable	[illegible]
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	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	[illegible]
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	AN USM 425 (v) 1 Tri-service standard scope	[illegible]
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw	[illegible]
	335	35 MHz @ 10 mV/div	yes	yes	20 ns/div	Only 10.5 lbs (4.8 kg)	[illegible]
	326	10 MHz @ 10 mV/div	yes		100 ns/div	Internal battery	[illegible]
	323	4 MHz @ 10 mV/div			500 ns/div	Only 7 lbs (3.2 kg)	[illegible]
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	213	1 MHz @ 20 mV/div			400 ns/div	DMM Oscilloscope @ 3.7 lbs (1.7 kg)	[illegible]
	212	500 kHz @ 10 mV/div	yes		1 μs/div	Low cost for dual trace & battery	[illegible]
	T935A (New)	35 MHz @ 2 mV/div	yes	yes	10 ns/div	Variable trigger holdoff and differential	[illegible]
	T932A (New)	35 MHz @ 2 mV/div	yes		10 ns/div	Delayed sweep and differential	[illegible]
	T922	15 MHz @ 2 mV/div	yes		20 ns/div	Low-cost dual trace scope	[illegible]
	T922R	15 MHz @ 2 mV/div	yes		20 ns/div	Rackmount version of T922	[illegible]
	T921	15 MHz @ 2 mV/div			20 ns/div	Lowest-cost TEKTRONIX Portable	[illegible]
Time Interval Readout	DM44	Optional, factory-installed, direct-numerical readout of time intervals and DMM functions for the 464, 465, 466, 475, and 475A					[illegible]

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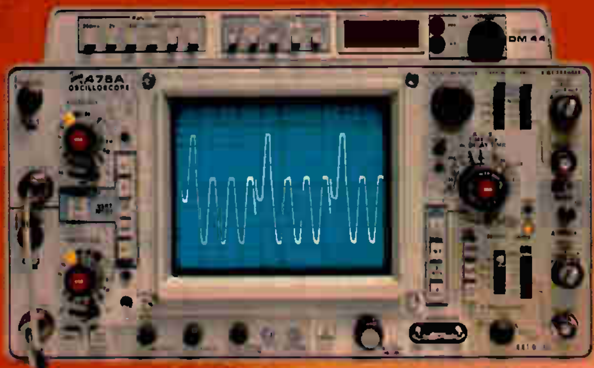
Labels identify statements so they can be referenced. Constants equate numbers with names for use throughout a program, like pi = 3.14. Data types are numerous; furthermore, structured types can be defined to include arrays, records, sets, and files. Each named variable must be followed by its type. Procedures can be put within procedures, and the statements for each must be preceded with the keyword "begin" and terminated with the word "end." Operators are defined for multiply, divide, add, subtract, logical, and relational, and numerous control statements are allowed.



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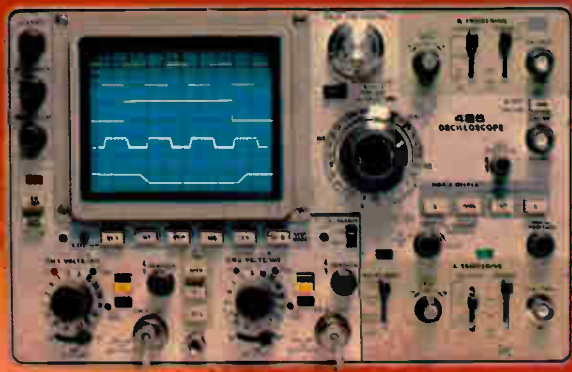

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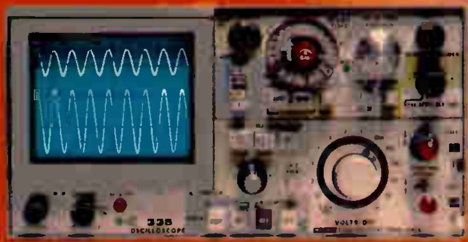

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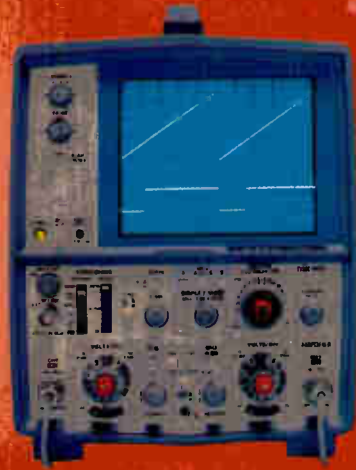

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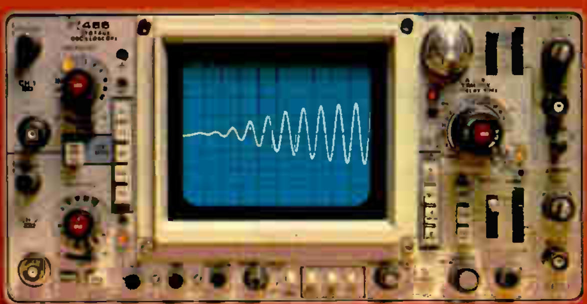

466

465M

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	434	25 MHz @ 10 mV/div	yes		20 ns/div	Split-screen storage	[illegible]
	314	10 MHz @ 1 mV/div	yes		100 ns/div	Only 10.5 lbs (4.8 kg)	[illegible]
	214	500 kHz @ 10 mV/div	yes		1 µs/div	Only 3.5 lbs (1.6 kg)	1520
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage	[illegible]
Nonstorage Models	485	350 MHz @ 5 mV/div	yes	yes	1 ns/div	Widest bw in a portable	[illegible]
	475A	250 MHz @ 5 mV/div	yes	yes	1 ns/div	High-performance 250 MHz portable	[illegible]
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	465	100 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 100-MHz bw	[illegible]
	465M	100 MHz @ 5 mV/div	yes	yes	5 ns/div	AN/USM 425 (V) 1 Tri-service standard scope	[illegible]
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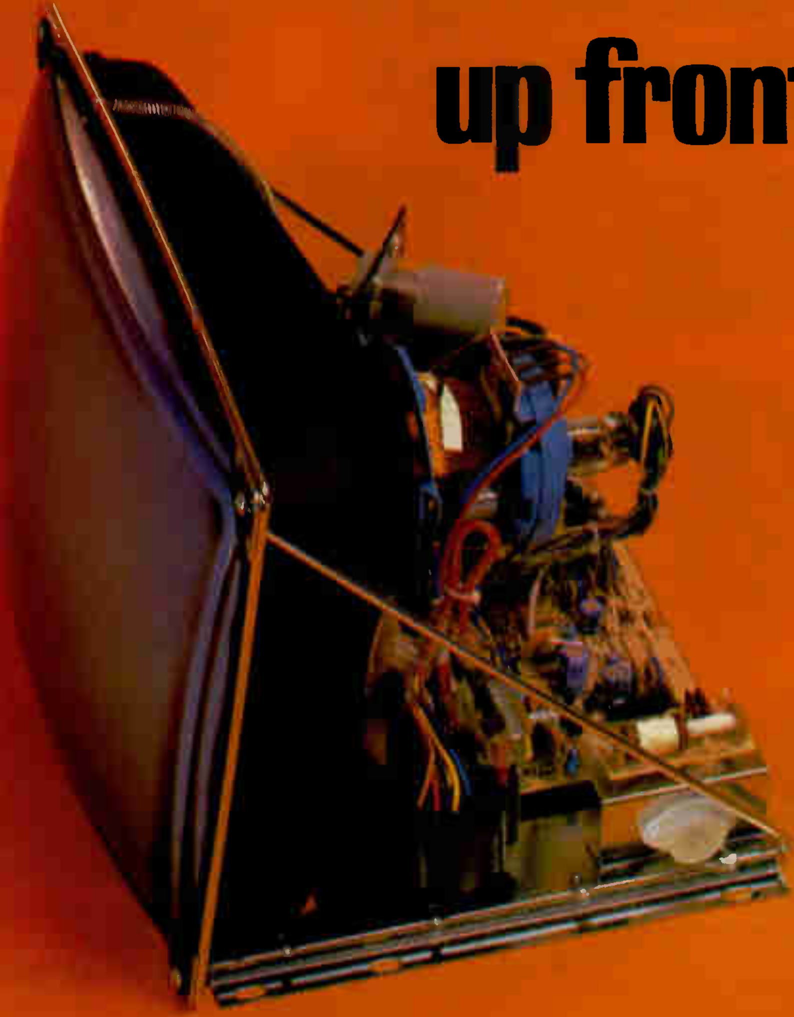

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Pascal becomes software superstar

Programming language has captured fancy of industry in past two years for use in wide range of computers

by John G. Posa, Microsystems and Software Editor

From the mountain fastness of Switzerland there came 10 years ago a programming language called Pascal. For the first few years of its life it created little stir, but then it began to gain popularity in academia and eventually industry. Today, Pascal is finding its way into machines of all shapes and sizes around the world.

Pascal has exercised the hardware of more than 60 families of computing machines, and new ones are being added to the list at this moment. It has been dubbed "PL/1 done right" and "Basic of the future," and it has been made to run on the ubiquitous 8080 microprocessor, Cray Research's giant, superfast Cray-1, and a host of machines in between.

Kenneth Bowles, director of the Institute for Information Systems at the University of California at San Diego, and his colleagues are now a major force pushing for Pascal in the U. S. They have put together a single-user operating system that an increasing number of people are using and even redistributing as part of their own systems.

Looking back, Bowles feels it was just lucky that Pascal was chosen. While using Algol during a seven-year stint as director of UCSD's Computer Center, he became convinced that the benefits of structured programming practices could not be overemphasized. He also realized that microcomputers would not disappear and that they represented a very cost-effective teaching aid.

Now for a language. About four years ago, Bowles looked to Pascal. Algol just was not general enough and Pascal, which was designed to teach programming in the first place, was starting to be used as an academic tool. "We saw industry producing a number of different machines and we didn't want to be locked into any one in particular," he remembers. "We needed software that would last a long time and could also be traded between various institutions." So portability became an underlying factor in their work.

Pascal, drafted in 1968 in Zurich by Niklaus Wirth (see "Obeisance to Pascal," p. 84, was chosen as the starting point, but its memory requirements were excessive. With eyes on the LSI-11 as a target machine, Bowles used frequency-based encoding to squeeze the compiler's requirements down to less than 20 kilobytes. (Simply stated, frequency-based encoding rearranges operators so that the most frequently used are the easiest to access.) He got this working on the PDP-11 and knew it would also go on the LSI-11, so in June of last year he reset his sights on the 8080.

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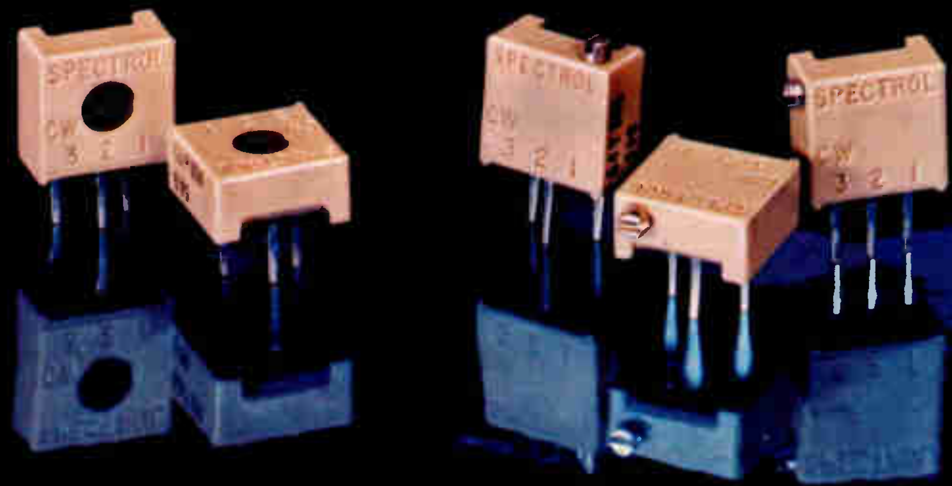
Six great features these two popular trimmers have in common:



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with 30% to 40% of the new programs being written in it. Included are those for initial software development, tools like compilers and libraries, and systems programming. In April, TI began offering Pascal for its DS990 disk-based minicomputer systems. The 990 compiler and several 990 system software modules are themselves coded in Pascal. Even Fortran routines can be embedded into TI's Pascal source code.

Another user is Electro Scientific Industries Inc. of Portland, Ore., a manufacturer of instruments and minicomputer-based laser trimmers. "We were coding in assembly language, but realized that we wouldn't be flexible enough to track the needs of our users," says Don Cutler, manager of systems engineering. So, like TI, the company went shopping for a high-level language. Basic and Fortran did not provide the real-time performance sought; PL/1 was too thorny and not benchmarked enough on small machines.

Choice. But Pascal seemed easy enough to understand and implement, so the firm obtained a compiler from the University of Illinois, changed about 99% of it to add things like real-number-processing capabilities, and ESI's software needs were satisfied. "The code generated typically uses only twice the memory and execution time of an assembly version," says Cutler.

But Electro Scientific did not go the P-code route. "When we started about five years ago, there wasn't much being done with P-code," says Cutler. Instead, its compiler generates macrocode and a macro assembler generates assembly code. The macrocode gives ESI certain advantages. For efficient execution, complex operations like fast Fourier transforms can be written in macrocode and embedded directly. Also, macro debuggers for the PDP-11 can be utilized. But Cutler does not scoff at P-code. "Given a random processor, P-code is the only way to go because it's so portable. Microprocessor implementations center around it, and it's the way of the future," he says.

The firm's compiler has spawned a separate company called Oregon Minicomputer Software. It has exclusive rights to market the compiler, which sells for $1,500, and has written versions to run on the PDP-11 with the RT-11, RSX-11/M, and RSTS operating systems. Oregon Minicomputer also has developed symbolic and variable editing packages in collaboration with its parent firm, and is about a year away from an optimized compiler that will be even more efficient, although it may not be appropriate for small machines.

Question. But even as the enthusiasm builds, one may reasonably ask, "If Pascal is so wonderful, why is it that every new user has to practically rewrite it?" The answer stems from the fact that all languages have their shortcomings, and Pascal has some too. First, Wirth's definition does not allow for separate compilation, which can be cumbersome. It means that a Pascal program must be compiled in its entirety: if a new routine must be added, it has to be entered into the original source code and recompiled.

Another complaint voiced by some users is that the size of an array must be fixed at the time of compilation. Pascal is very big on type-checking, which means that if a variable is of a certain type (integer, for example) in one part of a program, it must remain that type. This is actually a desirable programming practice, except that if the size of an array changes, it is considered a new type and genuine Pascal will flag it as an error.

In terms of system programming, it can be awkward to introduce modules of the type necessary for concurrent processes. Large arrays must be set up with global variables for the procedures to use, and if one of the variables is altered inadvertently, problems arise.

But complex operating systems can be written in Pascal, as Per Brinch-Hansen proved a few years ago with his Concurrent Pascal. And Wirth himself is now concerned with a new language called Modula that is based on Pascal and aimed at the concurrent-computation problem.

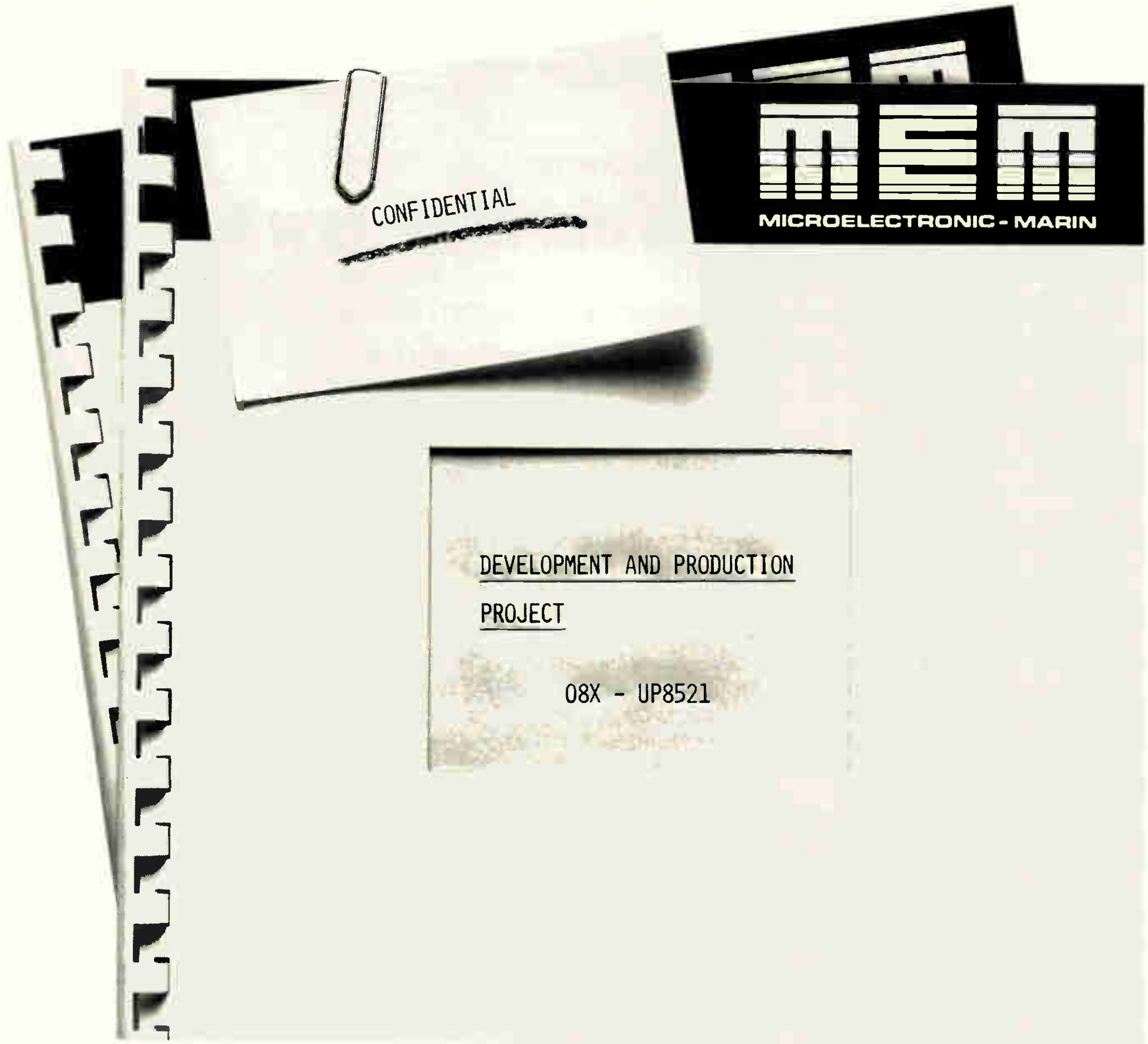
The newer Pascal compilers have all but eliminated some of these headaches. For example, Electro Scientific and others simply insert a dummy header with the variables they will use and add the actual procedure later. And TI has an expression to vary the size of an array without getting reprimanded. The only remaining problem seems to be exactly what extensions should become standard and how they should be implemented. Standards are important not to force their use but to enable those not adhering to them to state in precise terms how they are being different.

Workshop. This summer, UCSD held a workshop to discuss such standard extensions, and over 30 different firms were represented. Many ideas were discussed, including interrupts and the ability to pass procedure and function names as parameters; the report from that meeting will soon be available.

The military, too, began with Pascal to develop its standard language, now in the so-called Steelman phase [*Electronics*, Aug. 3, p. 59]. For a while, it was believed that the result would be Pascal with standard extensions. However, recent documents reveal a widening gap between the Defense Department's language and Pascal, to the extent that Pascal may not even be a proper subset. Compatibility may be possible, however,through filter programs that would translate one language into the other. □

Obeisance to Pascal

Why Pascal? The programming language apparently was named by its author, Niklaus Wirth, for the French philosopher and mathematician Blaise Pascal (1623–1662) for no reason other than the high esteem in which Prof. Wirth holds his teachings. The language is a relatively young one: a preliminary version was drafted at the Technische Hochschule in Zurich, Switzerland, by Wirth in 1968. Two years later, Urs Ammann, also at Zurich and aided by Wirth and colleagues, developed an accompanying compiler for Control Data Corp.'s CDC 6000 computer, and Pascal was off and running.



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Government

Small-business aid finds few takers

Electronics firms hit hard by foreign competitors are not participating in Federal loan program

by Wesley R. Iversen, Dallas bureau manager

For Cibco International Corp., the deadly blow came in mid-1977. At the time, the small Oklahoma City manufacturer of citizens' band antennas was riding a rising sales wave, with 60% of its volume coming from a new design. When a Japanese competitor entered the market with a similar, Taiwan-made design at about half the price, it signaled the beginning of the onslaught that would send Cibco's sales tumbling to 500 units per month, compared to an earlier 4,200.

Cibco president Marvin Joyner has managed to keep the firm afloat. But he has done so only by laying off 90% of his workforce and moving from the company's former 12,000-square-foot facility to a 3,000-square-foot plant, where remaining employees now assemble components around cheaper, imported antenna parts.

For Cibco and countless other small electronics-related companies that have been similarly hurt, there may be Federal "trade adjustment assistance" available. Under provisions of the Trade Act of 1974 administered by the Commerce Department's Economic Development Administration, companies that can document adverse import impact can receive Federally funded technical assistance, as well as help in the form of direct and Government-guaranteed loans.

Program goals. With current limits of $1 million per company for direct loans and $3 million for a Government-guaranteed package, the Trade Adjustment Assistance Program is geared primarily to smaller firms. For a variety of reasons, however, including apparently widespread ignorance of the program and reluctance to tackle time-consuming paperwork necessary to qualify, few electronics companies have used the plan.

Since inception of the current program in April 1975 through August this year, some 147 U. S. companies had been granted financial and technical assistance totaling $73 million, says Charles L. Smith, assistant chief of the EDA's Trade Act Certification division. The bulk of that aid has gone to companies in the footwear, apparel, and handbag industries. But there are many more millions available. As Smith puts it: "We haven't had many requests for certification from firms in the electronics field and we're actually a little surprised."

To obtain aid under the program, a company must first be certified eligible by Smith's division in Washington, D. C. A petition and supporting documents must be filed demonstrating that the firm's total production or sales have declined, that employment has declined, and that increased imports are a cause.

The EDA is required by law to make a decision on a certification request within 60 days after accepting a petition. While officials at some companies complain of hassles and red tape in becoming certified, others say the certification process is not a burden.

Certification approval, however, is no guarantee that assistance will automatically be provided. In order to obtain a direct or guaranteed loan, the certified firm must then prepare what is called an economic adjustment proposal, which spells out the company's recovery plans.

By EDA's own admission, though, the time between certification and approval of a loan or loan guarantee can be three to six months.

Speeding things up. But now, spurred in part by an emphasis on the program by the Carter Administration that led to a large influx of additional funding this year, the Commerce Department moved late last month to speed up benefits delivery to affected firms by establishing "trade adjustment assistance centers" in 10 U. S. cities. □

Aid for the many

Of some 300 companies overall that had received certification under the Trade Adjustment Assistance Program through August this year, only 11 were electronics-related firms. Of those, just one had successfully pursued a loan application with its requisite red tape all the way to actual approval. "My accountant and I worked nights and weekends on it . . . we spent many, many, many hours. It just took incredible amounts of time," recounts Jack Perlmutter of the paperwork required to obtain a $335,000 direct loan for his firm under the program. Perlmutter, who is president of Temple Sound Equipment Co. in New York City, filed his original petition for certification in March 1977. And while certification was granted within 45 days, it was more than a year before his loan was eventually approved last April and the money was forthcoming.

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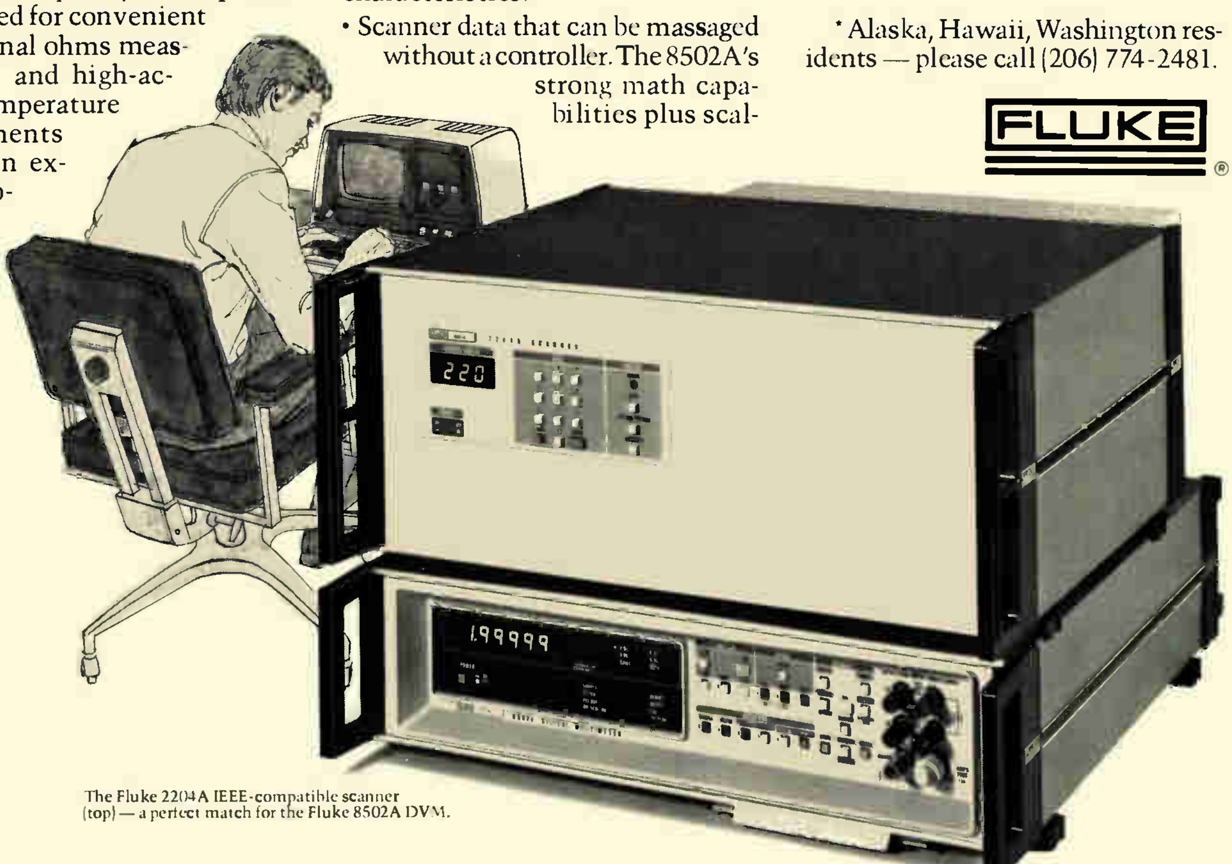

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Probing the news

Semiconductors

SIA forecasts 9% growth rate in 1979

Semiconductor Industry Association says market for U. S. firms will total $4.705 billion in 1978, $5.123 billion next year

by William F. Arnold, San Francisco bureau manager

The growth in worldwide shipments by U. S. semiconductor companies will slow to only half the rate of a banner 1978, but will pick up in 1980 and 1981 to show a bullish 15% compound growth rate for the four-year period. That's the latest estimate by the Semiconductor Industry Association, which forecasts no recession in 1979 and a modest rise in U. S. gross national product of 3% in real terms after a first-quarter dip.

In dollar terms, this means that the total worldwide market for U. S. chip makers will rise 22% this year to $4.705 billion, 9% in 1979 to $5.123 billion, and end the four-year forecasting period at $6.74 billion. The forecast assumes that about two thirds of the business will be domestic sales, according to John Welty, senior vice president of Motorola Semiconductor in charge of semiconductor operations and chairman of the SIA board of directors. It is based on individual members' predictions of their shipments, figures that may have been adjusted for inflation.

Consequently, because GNP is a leveraging factor in semiconductor growth, the SIA foresees a growth decline in all five market areas. It expects the consumer business, which should grow around 20% this year, to limp along with 4% growth in 1979. Similar growth declines are expected in computers, from 26% to 10%, industrial from 23% to 10%, and even surging communications from 27% to 16%. The military marketplace will show only a modest decline from 8% to 7% growth, Welty says.

Within that market mix, "digital MOS is the largest and fastest growing category," he says, including "the explosively growing n-MOS, tempered by moderate C-MOS growth and declining p-MOS." In fact, the association's estimates show digital metal oxide semiconductors accounting for almost half of the $3.556 billion integrated-circuit market with memories overtaking logic circuits in 1979.

In the digital bipolar area, Schottky transistor-transistor logic is growing fast and should overtake the faltering standard TTL as the largest segment in 1980. Emitter-coupled logic also will grow respectably.

Linear circuitry, although growing slower than MOS, should equal digital bipolar sales by 1983 or so. In 1979, the linear-device market is expected to increase 12.2% to $782 million with hefty increases in data conversion and interface circuits counterbalancing the modest 2.6% increase in special consumer circuits.

Last and least. Rounding out the forecast, the discrete-circuits sector, which will grow only 0.6% to $1.567 billion in 1979, actually shows dropping growth rates in diodes and small signal transistors, effectively no growth in rectifiers and thyristors, and only modest growth in power transistors and optoelectronics. Optoelectronics is the most volatile segment, showing a 9.1% growth even though the display and lamp portions register zero growth in 1979.

That's the SIA forecast in a nutshell. But how good are its

WORLD SHIPMENTS BY U.S.-BASED COMPANIES
(In millions of dollars and percent annual increase)

	1977	1978	1979	1980	1981
Total solid state	3,857	4,705 (22%)	5,123 (9)	5,846 (14)	6,740 (15)
Discretes	1,394	1,558 (11.8)	1,567 (0.6)	1,655 (5.6)	1,753 (6)
Integrated circuits	2,463	3,147 (27.8)	3,556 (13)	4,191 (18)	4,987 (19)
Digital bipolar	766	966 (26.1)	1,023 (5.9)	1,145 (11.9)	1,263 (10.3)
Digital MOS	1,136	1,484 (30.6)	1,751 (18)	2,119 (21)	2,626 (23.9)
MOS logic	633	740 (11)	843 (13.9)	984 (16.7)	1,185 (20.4)
MOS memory	503	744 (48)	908 (22)	1,135 (25)	1,441 (27)
Linear	561	697 (24.2)	782 (12.2)	927 (18.5)	1,098 (18.4)

SOURCE: SIA

Equipment makers are optimistic

Coinciding with release of the SIA forecast, members of the Semiconductor Equipment and Materials Institute from the Northeast met in Boston to give their outlook on their own industry and to hear the views of semiconductor-industry analyst Benjamin J. Rosen, vice president of Morgan Stanley & Co. Inc. of New York City. SEMI members supply capital equipment to semiconductor makers; they are mostly bullish about the next two years, with a few notes of caution.

For his part, Rosen says Morgan Stanley revised its forecast some time ago from a 15% increase in the dollar value of semiconductor shipments this year to 22%. Where he had been predicting a slowing to a 5% growth rate in 1979, that number has been boosted to 10%. "So we look for a deceleration from strong growth to slow growth, but the business troughs are moving farther into the future." Rosen expects such a trough, possibly in 1980, but only a "mild correction," nothing like the disaster that struck in 1974–75.

Typical of the SEMI member comments were these:

Milton Greenberg, president, GCA Corp., Bedford, Mass.: "The semiconductor industry is much more stable now than it was in 1973. We don't expect the boom and bust cycles; that's not in our planning." The industry has not overbuilt capacity, Greenberg explains.

Sheldon Weinig, president, Materials Research Corp., Orangeburg. N. Y.: "For the first time, my sales manager isn't complaining that if we could paint the new model green instead of red, or deliver on time, he could sell more. He's saying 'Give me enough salesmen and I can sell more.' "

Frederick Kulicke, president, Kulicke & Soffa Industries Inc., Horsham, Pa.: "We don't see a downturn in the next 24 to 36 months."

Lawrence Curran

numbers? Welty, in presenting the forecast at the association's annual dinner meeting late in September in Palo Alto, Calif., conceded that the SIA missed the boat last year when it forecast an 11% growth for this year. He attributes this to several things: drastically underestimating the growth in Japan by 10 times; undershooting the growth in GNP in all countries; and not anticipating the effects of the dollar's devaluation. In fact, he says that the impact of the dollar's dip knocks three to four percentage points off this year's growth rate to 18% or 19%.

Doubts. As for the new estimates, other analysts raise some questions. The rise in discrete-device business seems low at 0.3% and should equal the forecast's 3% rise in product shipments, observes Stephen Cottrell, vice president for solid-state devices at Creative Strategies International, a San Jose, Calif., market-research firm.

Furthermore, considering the unexpected 40% growth rate this year in the Japanese market, he questions the forecast's 10% growth figure for 1979. "I see no reason why it won't increase beyond 10% if only because of dollar devaluation. I look for 14% to 18%," he says, pointing out that U. S. companies are further along the learning curve.

"As an overall bottom-line projection, I think that a 9% figure is reasonable," observes Daniel Klesken, vice president of Dataquest Inc., a Menlo Park, Calif., market-research firm. He sees capital spending in instruments and test equipment doing well.

The computer segment should be strong primarily because "a computer is an effective inflation fighter," he says. However, he guesses that discretes will rise 1% to 2%, instead of the 0.6% the SIA estimates.

The SIA forecast assumes that the dollar devaluation will help U. S. sales abroad and that there will be no further devaluation in 1979 and beyond. Moreover, it predicts that Japan, which is about 5% of the market for the U. S. firms, could have a growth in real GNP of as much as 6% over the next few years. Europe, about 25% of the market, could grow 4% by 1980.

The forecast represents consensus estimates of net product shipments of U. S.-based chip makers including foreign subsidiaries and intradivisional and intracompany sales. □

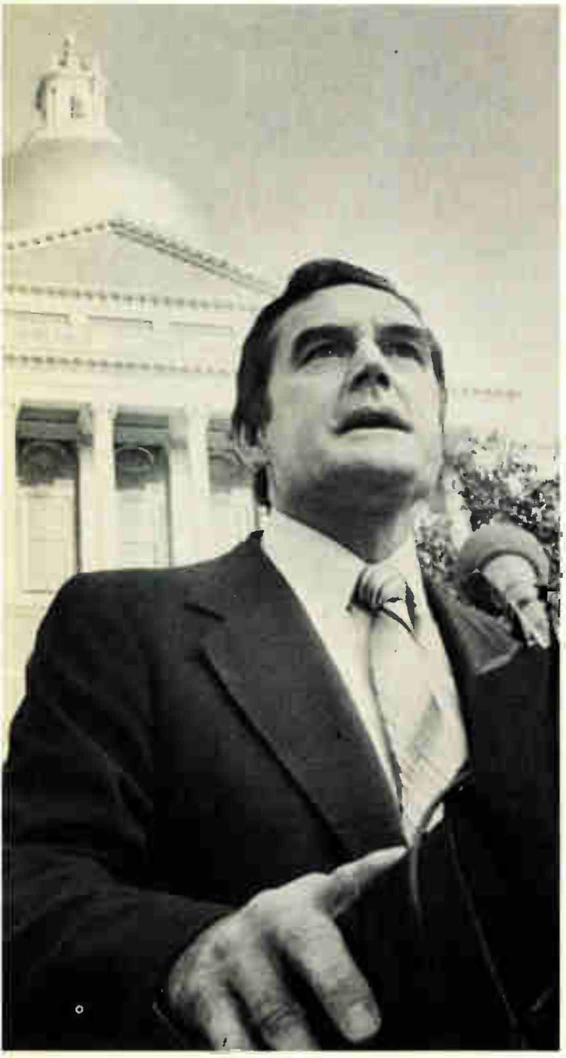
Commentary

Vote encourages Massachusetts firms

Defeat of Dukakis in gubernatorial primary fits pattern of emerging American revolution against taxes

by Lawrence Curran, Boston bureau manager

The conservative mood sweeping the United States, manifest in voter reactions to their tax burden, could affect efforts across the nation to gain tax relief for high-technology firms. Just last month, Massachusetts voters surprised pollsters and an incumbent by selecting conservative Democrat Edward J. King to be that party's candidate for governor in the November general election.



King made Michael Dukakis a one-term governor when he beat Dukakis and a third candidate in the Sept. 19 Democratic primary, and Ray Stata thinks the vote bodes well for the Massachusetts High Technology Council. Stata is president of the council, formed late last year to change what member companies' top executives say is an antibusiness climate in the commonwealth [*Electronics*, Jan. 5, p. 112]. He thinks the council could be the prototype for what electronics companies in other states with high taxes may have to do, and California is certainly in that category.

Stata is also president and chairman of Analog Devices Inc. Like many of the other MHTC companies, Analog Devices is finding recruitment from outside Massachusetts difficult because of the big personal tax bite prospective technicians, engineers, and engineering managers would face in the Bay State.

Moving. A large percentage of the 81 MHTC member companies are in the electronics industries, and many of them are creating jobs outside the state faster than they are within. Their top executives argue persuasively that they are moving because other states, like New Hampshire, North Carolina, and Texas, give them and their employees a better tax break. That is particularly true of members Digital Equipment Corp. and Data General Corp., the two minicomputer manufacturers, which are expanding rapidly outside the state.

Tax cutter. Edward J. King, Democratic candidate for Massachusetts governor, says he wants to cut taxes and state spending.

Stata has considerable respect for Dukakis, but the governor's response to a recent council proposal to curtail taxes was less enthusiastic and specific than that of King, who faces Republican Francis W. Hatch Jr. in November's election. The council has also sought Hatch's reaction to its initiative; he has not responded yet, but his September message to voters hit hard at the need to cut taxes and state spending.

Too little. Against the backdrop of Proposition 13, Dukakis' more liberal stance, even though the governor hammered away at how many more in-state jobs were created in his administration, did not go down well with the voters. Stata says the most significant recent development favorable to the council's initiative is that the voters "are disappointed with the status quo, let alone any move to the left" in the form of more social programs.

MHTC's tax-cut proposal to the Dukakis administration—and to candidates King and Hatch—will be brought home to candidates for the legislature in a series of one-on-one meetings between the candidates and top executives from council-member companies who live in their districts. Alexander d'Arbeloff, president of Boston-based Teradyne Inc., the automatic test equipment maker, heads the council's legislative caucus. He is coordinating the effort to get the council's views across to key members of the legislature.

The legislature is the arena in which the council's major thrust will be made in the coming year, Stata says. And indeed it should be, for even Dukakis had his problems with the heavily Democratic legislature. But the council is working hard, and the legislature should also be able to read the mood of an electorate fed up with ever higher state budgets and taxes. Ideally, the council wants its tax-cut proposal embraced and turned into legislation by influential legislators.

"We'd like to get them to carry our banner," Stata says, which is what d'Arbeloff's legislative caucus is all about. Once the legislation is filed—Stata hopes this fall—council members intend to lobby for it with both the legislature and the executive branch. The legislation they want will contain three main points:

- That the financial burden, as measured by total state and local government revenues collected from citizens and businesses, be reduced to the average level prevailing in 17 competing states by the end of the next governor's administration.
- That the principal source of revenue reductions be taxes, rather than fees, licenses, and tuition.
- That cuts center on those taxes that are out of line with those of competing states. Specifically, the council wants elimination of the surtax on personal income, reduction of taxes on unearned income, and reduction of property taxes.

Promises. King's response to Stata was, in part, that "the situation is properly termed a grave one when Massachusetts is the second highest in taxes" among the 17 industrial states with which the council competes for technical talent. "I support and am determined to accomplish your goal to reduce the tax burden to at least the average of the 17 states."

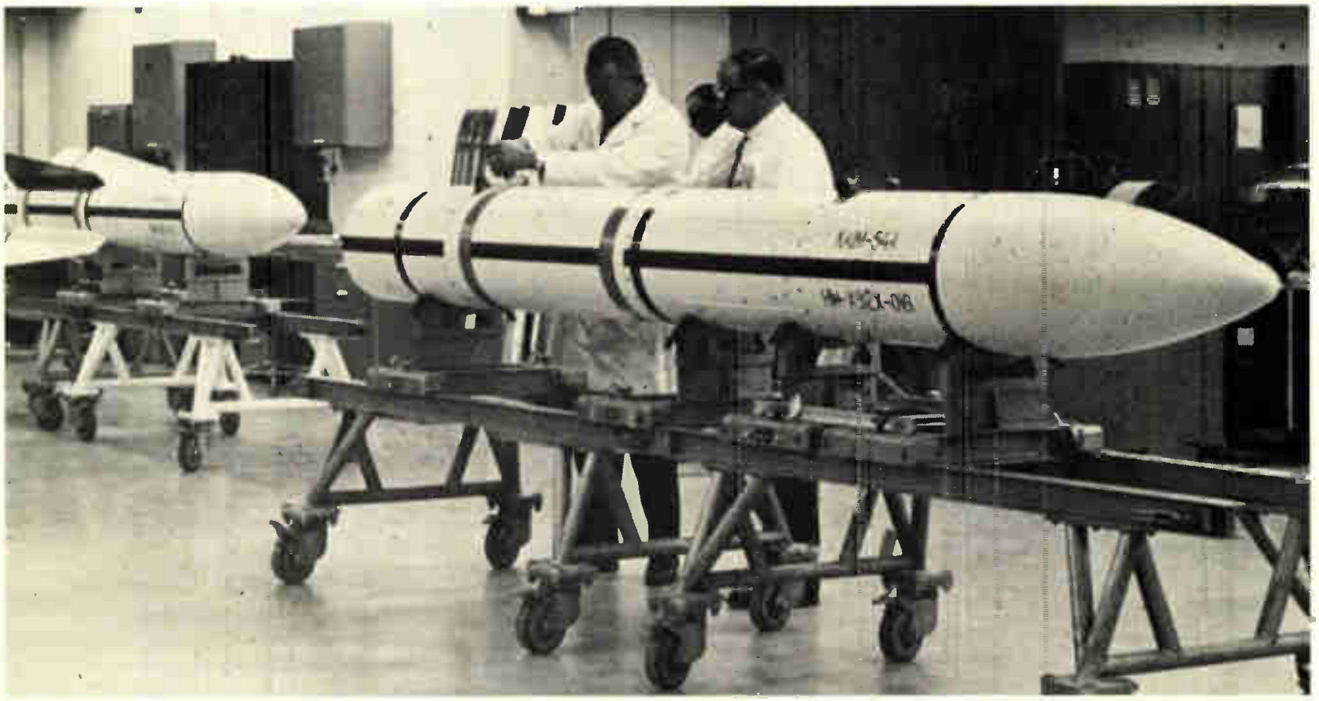
There's reason, then, for Stata and his council colleagues to be satisfied with their progress in less than a year, but there could be a big difference between the stances of a candidate King or Hatch and a governor King or Hatch. Council members realize that, hence the emerging move to lobby in the legislature. Stata says the high-technology companies have no historical enemies in Massachusetts, as did the textile industry, which has largely fled the state. But changing an environment that lacks enemies into one where friends can be counted isn't easy. □

Military

Missile makers eagerly await LSI

Use in computers for tactical weapons is still years away, say Hughes scientists, but will have dramatic effect

by Larry Waller, Los Angeles bureau manager



Without LSI. Phoenix missiles move along their production line at Hughes, where 44 are turned out each month.

With large-scale integrated circuits now commonplace, news of another application usually evokes a ho-hum reaction. But in the very demanding arena of on-board computers for tactical missiles, things are different: giant problems of small size, high speed, and low cost have kept these years behind other computers in using digital LSI.

"We are just now nibbling at LSI," admits a scientist who has been in the middle of missile development since the 1940s. But Hans A. Maurer, technical director of Hughes Aircraft Co.'s Missile Systems Group, is so turned on by the potential of new devices that he sees them having "a dramatic effect on tactical-missile computer architecture," even though it will take "two or three years before true LSI finds a modest role." Maurer, who directs advanced design of Hughes missiles, and Knut S. Kongelbeck, senior staff engineer, gave a paper on the subject earlier this month at the military electronic defense exposition in Wiesbaden, West Germany.

Hughes' missile group provides a prime vantage point for viewing trends, since it probably has built more tactical missiles of different types than any organization anywhere. Its current roster includes the high-performance air-to-air Phoenix, the air-to-ground Maverick, and the Tow, a wire-guided surface-to-surface weapon.

Production volumes range from the Phoenix's 44 per month, through Maverick's 300, to Tow's 3,000 per month. To date, Hughes has turned out 214,000 Tows, against a contract for 275,000 through 1980. Group headquarters are in Canoga Park, Calif., with production in El Segundo, Calif., and in Tucson, Ariz.

Slow spread. Digital computers have been tardy working their way into tactical missiles, the Hughes scientists explain, because of the application's unique requirements. "On one hand, limitations of size and power dissipation have to trade off against performance, or computer speed measured in throughput by thousands of operations per second. But dominating the design choice is the cost consideration, because each

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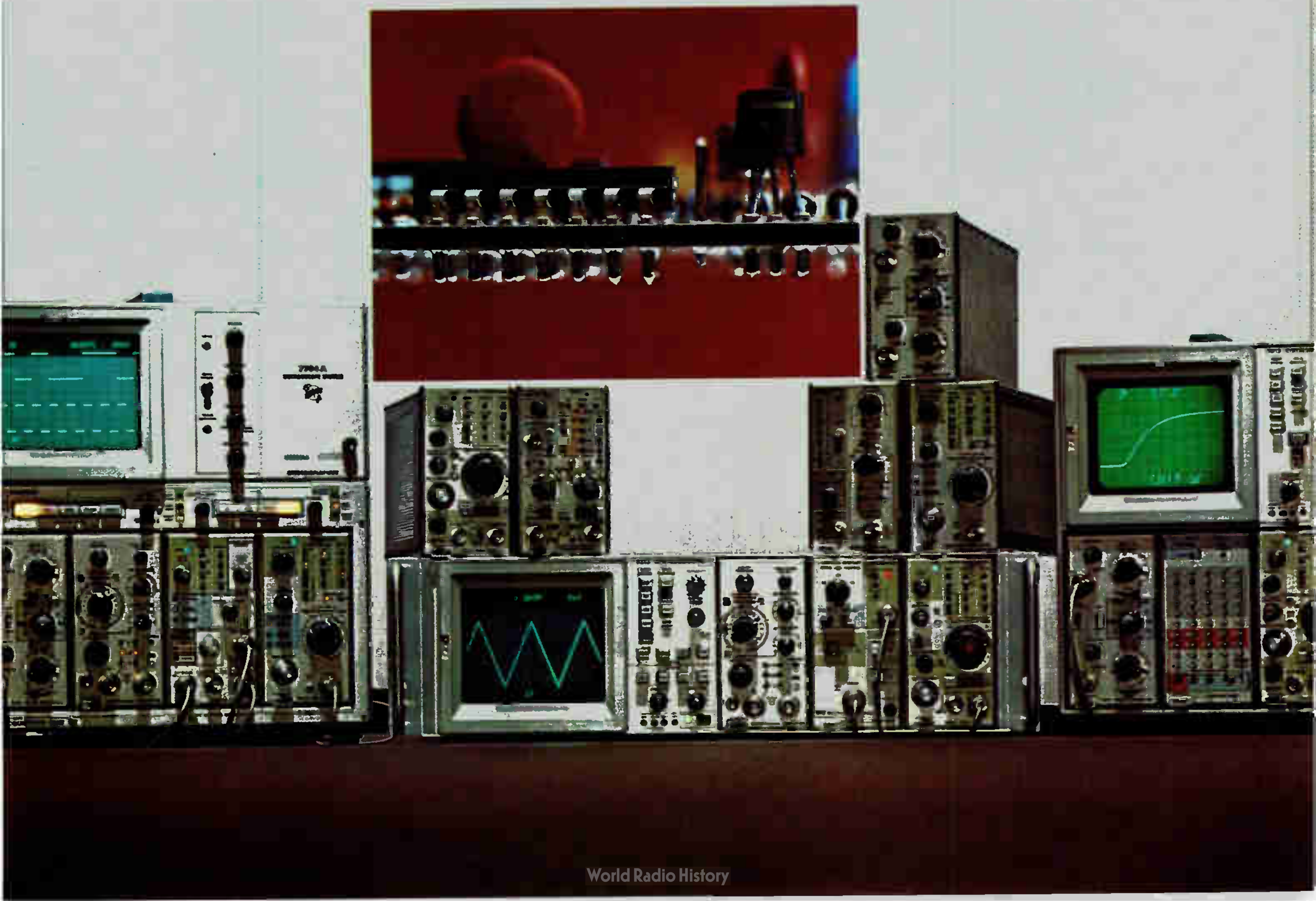

computer is used only once."

In the past, a designer resolving such tradeoffs had no choice but to opt for analog circuits in processors to keep costs within reason. The result is that U. S. tactical missiles now operational employ circuitry that, for the most part, was discarded 10 years ago by commercial users and even by the military for other projects such as avionics, ground-based data systems, and strategic missiles.

New mission, new needs. But the changing nature of these weapons' missions is fostering new designs that cry for digital processing. "One of the driving forces for increased guidance complexity, for example, is the desire for multimode missiles, which might contain both infrared and radar [millimeter-wave] guidance capability," they continue. Such added complexities make "our functions speed-hungry," says Maurer.

Also, the fact that missiles operate in a real-time environment requires a computer throughput greater than that of some bigger avionics computers, points out Kongelbeck. These rates are 400,000 operations/s for the Maverick and 2.1 million for the Phoenix, higher than present microprocessors can attain.

Besides the textbook advantages of digital processors over analog (modularity, no need for calibration, and repeatability), Maurer homes in on another: microprogrammability—important because it can prolong the life of today's missiles. "With the microprogrammability of digital LSI, we can not only change the program, which you can't do with hard-wired analog, but we can also add the little extras of speed, memory, and logic that boost performance," he says. This feature permits rapid change of missile control programs to beat electronic countermeasures.

Evaluations. Hughes has not yet put digital LSI into any of its missiles as the central processor, although some dedicated chips are in place for input/output or interfacing. Now in prototype form for evaluation for the Phoenix missile is a minicomputer, at the medium-scale integration level, committed to Schottky transistor-transistor logic and a bipolar chip set being evaluated for Maverick.

Two ways. With the potential of digital LSI coinciding with a planned jump in missile performance, the Hughes researchers are hard at work trying to bring the two together. "In the laboratory, we're forging ahead in those areas where there's a need," says Maurer. As he and Kongelbeck see it, "future device technology offers two alternatives for meeting requirements of the new missiles." In fact, the architecture of the missile computers will depend on which type is chosen, they say.

One alternative is very-high-speed logic: gallium-arsenide field-effect transistors, transverse electron devices, Josephson-junction logic, or dielectrically isolated emitter-coupled logic. These hold the promise of speeds almost 10 times faster than today's components; however, there has not been much improvement in densities and power dissipations.

MISSILE COMPUTER CLASSES				
Processor type	Throughput (thousands of 16-bit operations/s)	Central processing unit		Board area (cm^2)
		Power dissipation (W)	Cost/unit ($)	
8-bit MOS processor	25	2	75	160
16-bit MOS processor	170	2	200	160
Bipolar LSI chip set	500	20	1,000	400
MSI custom minicomputer	2,100	60	2,000	600

SOURCE: HUGHES AIRCRAFT CO.

And since makers of the fastest mainframe computers provide the impetus for these types, their commercial availability at low cost is questionable. Maurer notes, though, that the Pentagon's new very-high-speed integration, or VHSI, program could help [*Electronics*, Sept. 28, p. 89]. Another hurdle: these processes are still in research labs, at least five years away from missile designers.

Giving promise of earlier access are very dense LSI logic parts—probably available within two to three years. Included here are integrated injection logic, silicon on sapphire, and high-performance (short-channel) metal oxide semiconductors. Depending on the achievement of lithographic resolution of first 1 to 2 micrometers, and later less than 1 μm, their allure is lower cost at reduced power and volume.

Moreover, the high-density approach lends itself to distributed processing (as opposed to a single central computer), which can perform the processing tasks of missile subsystems and at the same time integrate the functions. This is possible now only with more expensive bipolar chip sets. "With the increased throughput of a new generation of 16-bit microprocessors approaching 400,000 to 500,000 operations per second, the distributed processor will gain acceptance for medium and high-performance applications," the Hughes engineers maintain.

One overriding requirement of missile planning is "reliability, which makes us inflexible in adopting new techniques," says Maurer. "Maturity of a technology" is an oft-mentioned phrase, but hard to come by in fast-moving semiconductors. Also, their observation that "the missile world is a hard life for LSI" refers not only to difficult environments and absolute reliability, but also to the gestation period of a tactical missile, which has been estimated at eight years from first funding to full operation. □

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The HP 1000 Model 45 comes with a fast (25 msec seek time) 20M byte disc drive and an HP 2648A Graphics Terminal, as well as our new Graphics/1000 support software to help you write graphics programs. You can also team it up with other HP products like the HP 9872A four-color plotter and the HP 7245A printer/plotter.

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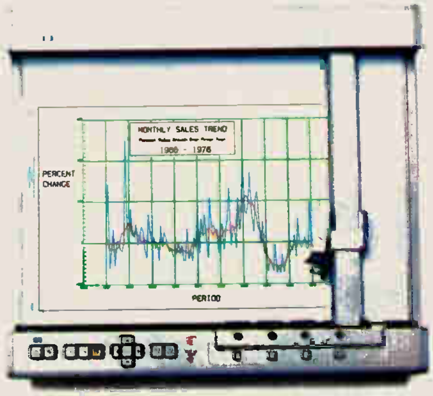

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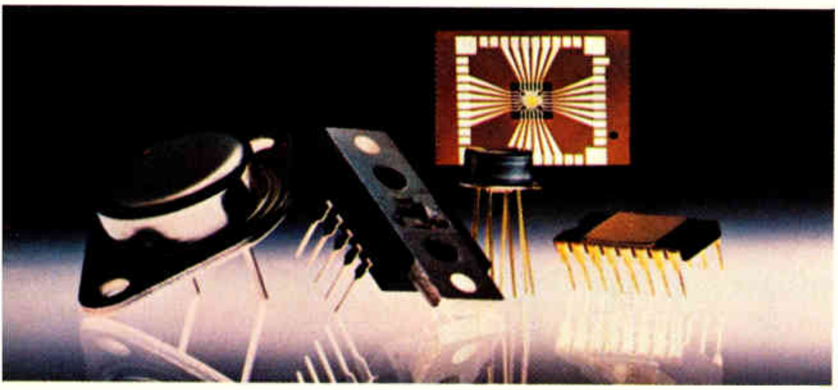

Components – The newest memories and other logic devices, consumer and industrial linear parts, and discrete components can be tested and evaluated on Teradyne systems.

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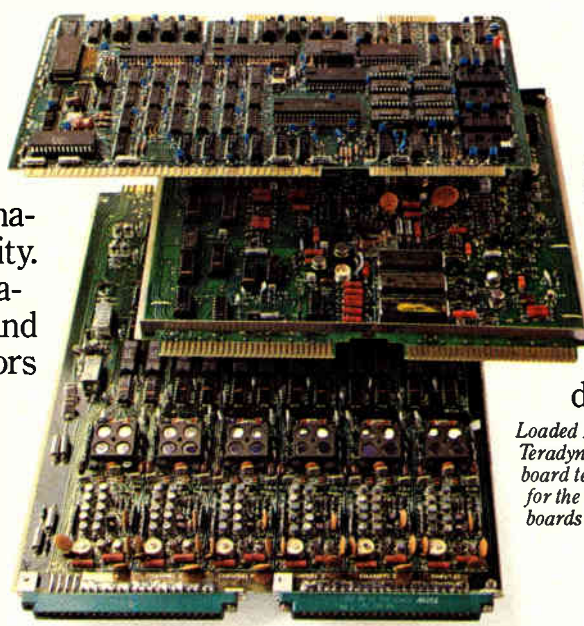

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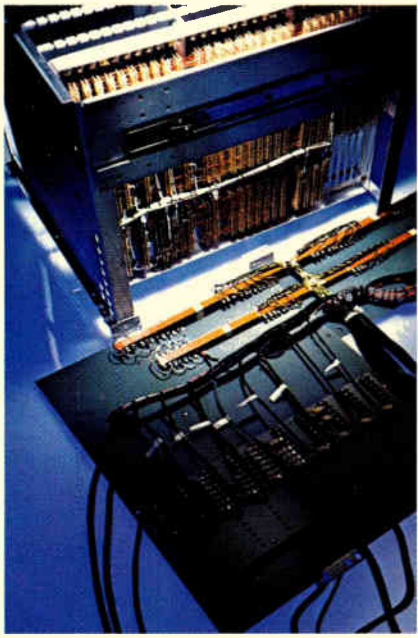

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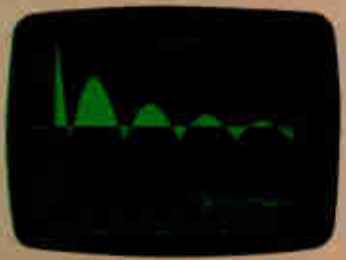

Waveform Analysis

Regression Analysis

Bar Chart

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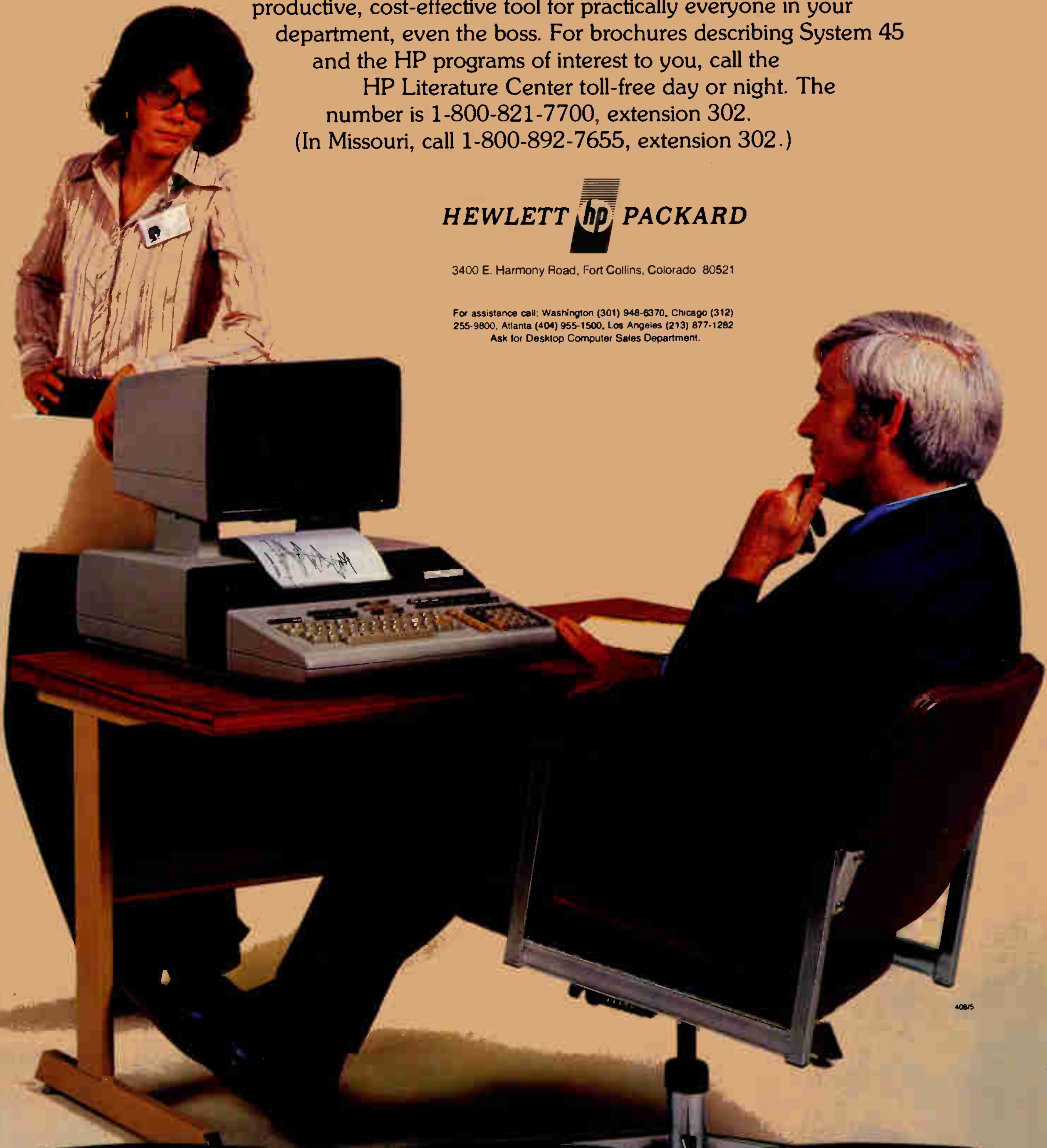

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16-bit single-board computer maintains 8-bit family ties

Three-bus 8086-based board addresses a megabyte, communicates over expanded system bus

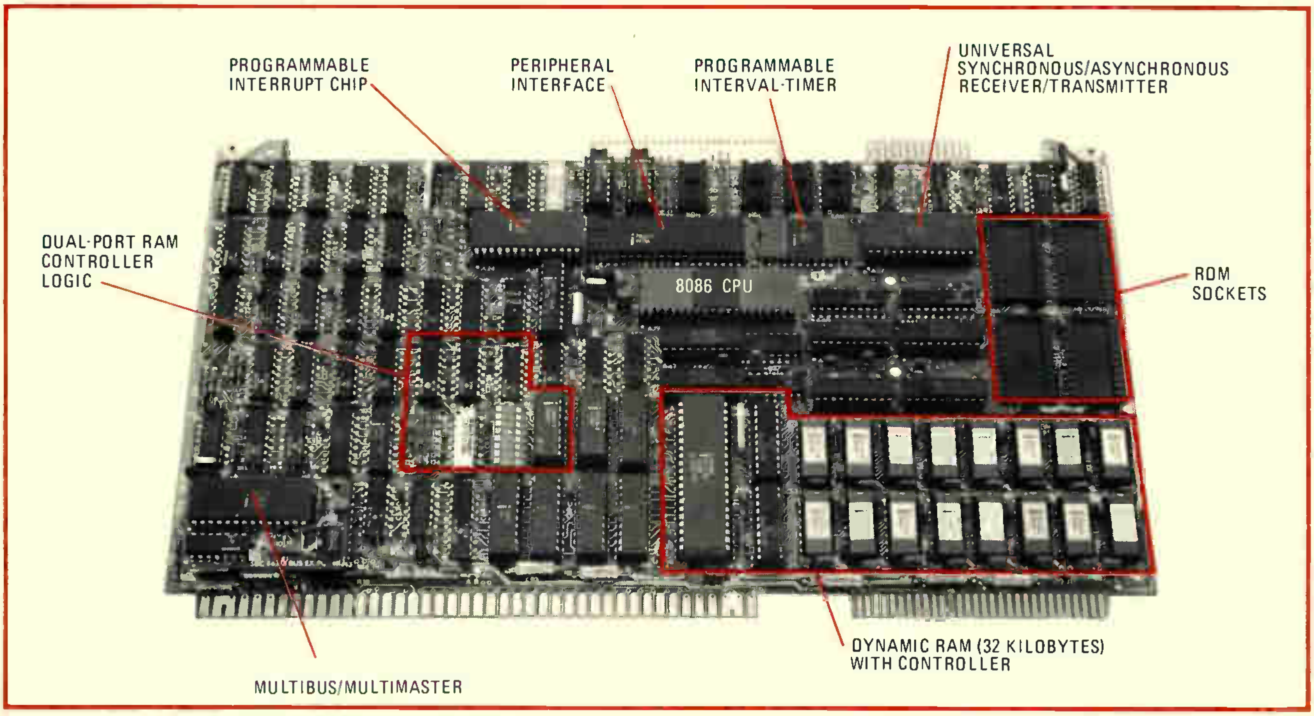
by Robert Garrow, Jim Johnson, and Les Soltesz, *Intel Corp., Santa Clara, Calif.*

☐ For the first time ever, 8- and 16-bit single-board computers can brainstorm over the same system bus. The iSBC 86/12 16-bit SBC has been designed to work intimately with its predecessors, the iSBC 80 family of 8-bit boards. What's in it for the user? Design flexibility—8-bit designs can be enhanced to 16 bits, developed software can be transported and, beyond that, 8- and 16-bit devices can be mixed in multiprocessing configurations. Several features make these options possible: a 16-bit CPU and instruction set designed for 8-bit compatibility; greatly expanded memory resources; and an extension of the Multibus specifications.

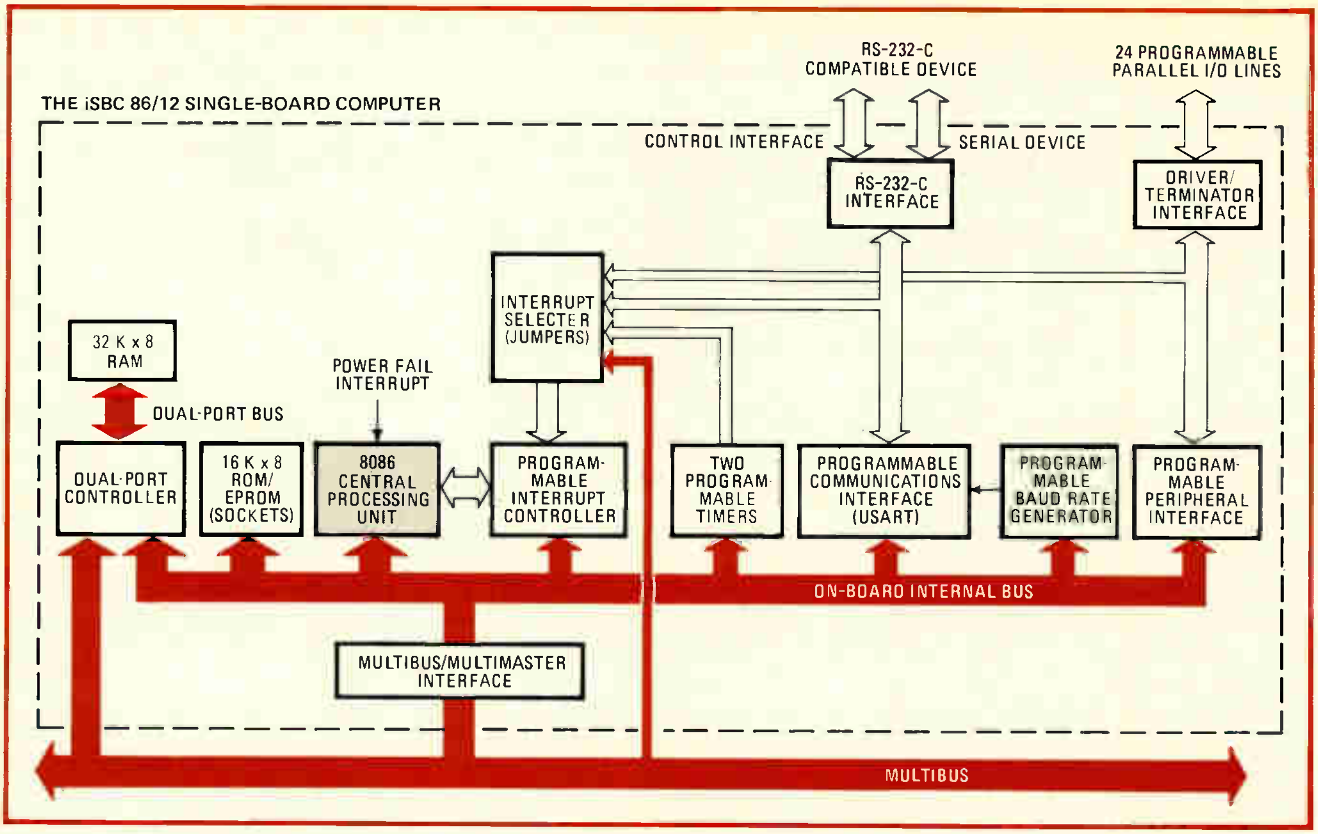
At the heart of the iSBC 86/12 is a 16-bit, high-performance metal-oxide-semiconductor 8086 central processing unit that operates at 5 megahertz. Because the 8086 instruction set is a superset to that of both the 8080A and 8085A 8-bit processors, the CPU can execute the full set of 8080A/8085A-type 8-bit instructions plus a new set of 16-bit instructions. Thus, programs generated for 8-bit-CPU systems can easily be upgraded to run on the iSBC 86/12 using the software tools available with the Intellec microcomputer development system. Programs written in Intel's high-level programming language, PL/M, can be executed on both iSBC 80 and iSBC 86 products, preserving the software investment in 8-bit systems as a user moves into 16-bit applications.

Other features of the 8086 CPU are signed 8- and 16-bit arithmetic (including multiply and divide), efficient interruptible byte-string operations, and improved bit manipulation. Furthermore, the 8086 provides mechanisms for reentrant code, position-independent code, and dynamically relocatable programs.

This enhanced processing power is supported by the largest memory ever offered on a CPU board (Fig. 1). Memory address space has been extended over the iSBC 80 series to one million bytes. Up to 16 kilobytes of



1. What a board. The iSBC 86/12 has 32 kilobytes of RAM and room for 16 kilobytes of ROM. The 5-MHz 8086 CPU executes 8080A/8085A-type as well as 16-bit instructions, including multiply and divide. Address space has been increased to a megabyte.



2. LSI + SBC = 86/12. A number of programmable LSI devices take credit for the power and flexibility of the iSBC 86/12. Note their interconnection to the three-bus hierarchy. When the 8086 requests a resource, the system bus is used only as a last resort.

read-only memory can be installed on the iSBC 86/12 itself. Furthermore, an additional 32 kilobytes of dynamic random-access memory with on-board refresh may be accessed independently by the CPU or by the system bus (Multibus).

Like the iSBC 80/30, the 86/12's RAM has dual ports to extend its use off board for access by other Multibus masters, including single-board computers, direct-memory-access devices, and peripheral controllers [*Electronics*, Aug. 17, p. 109]. All memory operations on the board occur independently of the Multibus, freeing it for external parallel operations. For applications that require data integrity at all times, a separate bus supplies power to the RAM and support logic via the edge connector. An auxiliary power source energizes the RAM in the event of power failure.

Multibus—the new look

To exploit the greater performance of the 8086 CPU and simultaneously make the iSBC 86/12 fully compatible with the iSBC 80 family of SBCs and expansion products, the Multibus specification has been extended to support 20 bits of address and 16 bits of data. The control lines, too, have been expanded to direct 8- and 16-bit data transfer over the system bus. These improvements enable the iSBC 86/12 to address directly a full one megabyte of system memory, access data in 8- or 16-bit word lengths, and recognize and acknowledge a variety of interrupts.

Address space has been enlarged to 1 megabyte by adding four address lines, A_{10}–A_{13}. Next, 8- and 16-bit data operations have been defined to permit both types in the same system. This is done by reorganizing the memory modules, adding one new signal and redefining another. The memory is divided into two 8-bit data banks, which form a single 16-bit word. The banks are organized such that all even-byte-addressed data is in one bank (D_0–D_7) and all odd-byte-addressed data is in the other bank (D_8–D_F). A new bus-address signal has been defined to control the odd-byte bank called byte high enable (BHEN) during 16-bit operations. When active, BHEN enables the high byte of the data word from the addressed boards on the D_8–D_F Multibus data lines. A_0 controls the even byte bank and, when inactive, enables the low byte of the data word on the D_0–D_7 Multibus data lines. All word operations must occur on an even-byte-address boundary with BHEN active for maximum efficiency. (A_0 is inactive for all even addresses—see the table.) Word operations on odd-byte boundaries will be converted to 2-byte operations by the 8086, one for low-byte, one for high-byte. Byte operations can occur in one of two ways. The even bank is accessed when BHEN and A_0 are both low. This puts the data on D_0–D_7. To access the odd bank (normally placed on D_8–D_F during a word operation), a new data path has been defined. The active state of A_0 and the inactive state of BHEN are used to enable a swap-byte buffer, which places the odd data bank on D_0–D_7. This permits an 8-bit master access to both bytes of the data word while controlling only A_0. A_0 therefore specifies a unique byte and is not part of the word address, since all word operations are on even-byte boundaries.

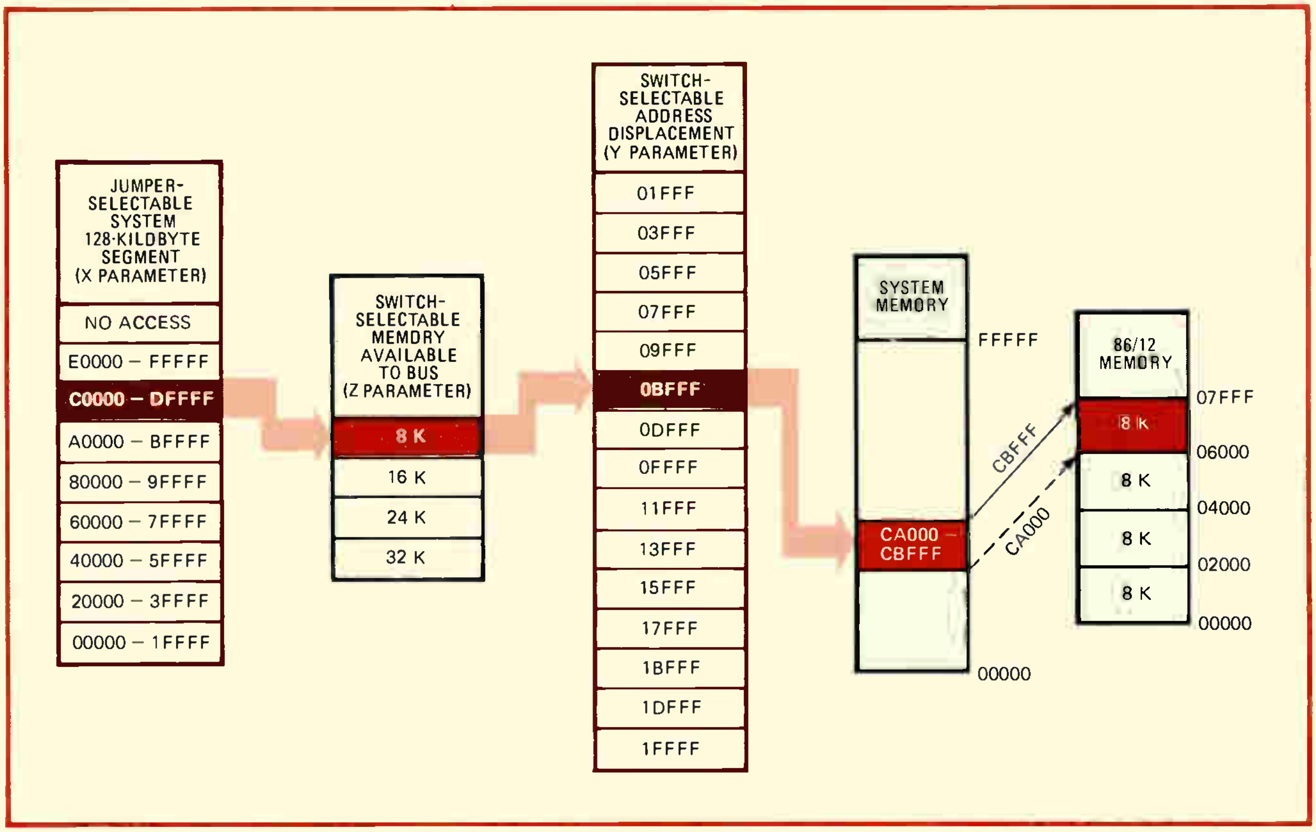
Flexibility: LSI chips are the key

The iSBC 86/12 owes much of its flexibility to programmable large-scale integrated devices. An 8255A peripheral interface chip provides 24 programmable I/O lines that may be tailored to the customer's needs by simply programming the device for input, output, or bidirectional modes with or without handshaking abilities. In conjunction with the 8255A's configuration the user may then select appropriate line drivers and terminators for the I/O lines that can be inserted into sockets on the iSBC 86/12 board.

An 8251A universal synchronous/asynchronous receiver/transmitter is included to provide an RS-232-C interface for serial communication with other computers, RS-232-C-type peripherals (cassette tape, modems, etc.) or cathode-ray-tube terminals. The 8251A enables the user to customize the communication link. Synchronous/asynchronous mode, data format, control character format, parity and baud rates from 75 to 38.4 kilobauds are all under program control.

For system timing functions an 8253 programmable interval timer provides two programmable timers, each of which may be used as a square-wave generator, retriggerable one-shot multivibrator or as an event counter.

The interrupt structure of the iSBC 86/12 encompasses nine levels with vectored priority. Eight of these levels are handled by an 8259A programmable interrupt controller chip, which may be configured for different priority processing modes in accordance with the application. One nonmaskable interrupt is available to immediately alert the CPU to catastrophes like a power failure, in which case the CPU can branch to an appropriate routine in memory to effect an orderly system shut-down.



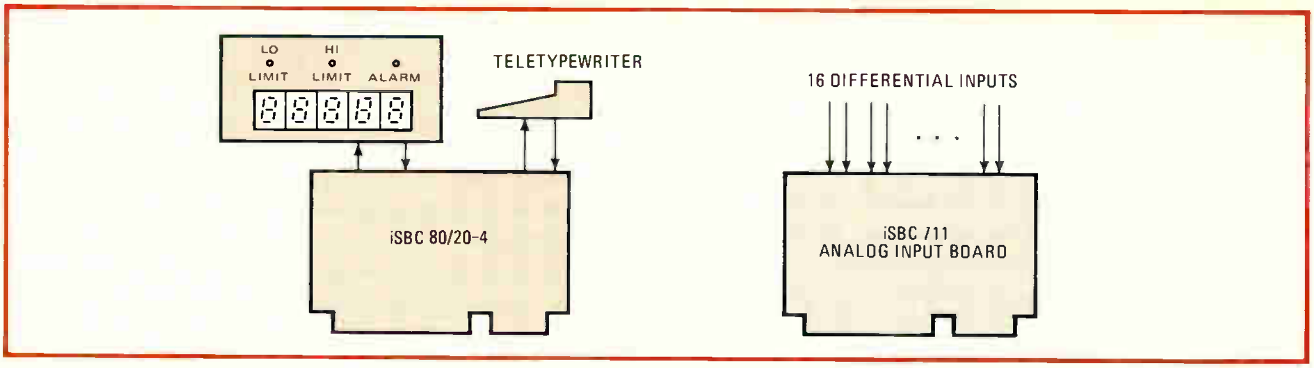
3. RAM, please. The 8086's view of on-board memory is fixed from zero to 07FFFH. When an outside master accesses this space, the DP controller performs the translation. Here, locations 06000H to 07FFFH are available to another master by addressing CA000H to CBFFFH.

Since all 8-bit accesses via Multibus are done on the lower byte of the data word, the iSBC 86/12 can access 8-bit memory or I/O devices from the system bus. This makes the iSBC 86/12 compatible with all iSBC 80 Multibus modules.

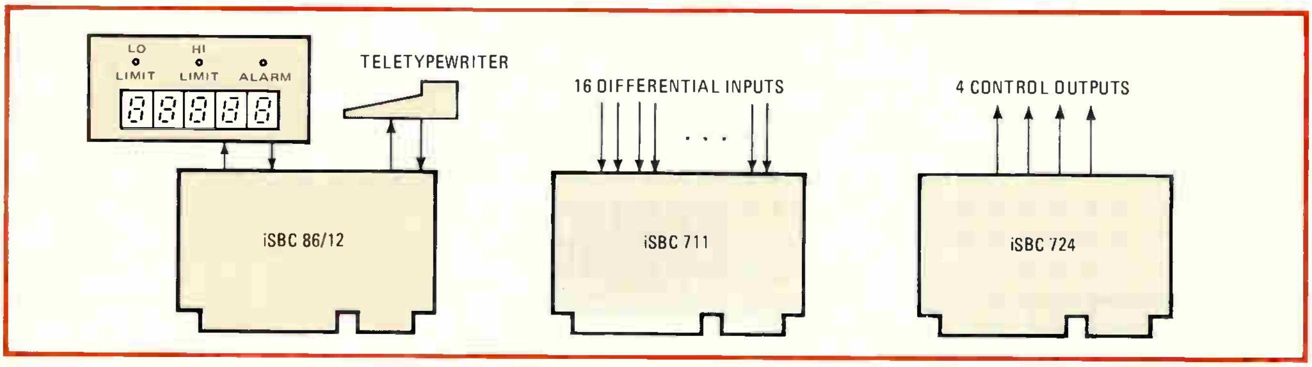
More interrupts, too

The iSBC 86/12 expands the previous Multibus definition of interrupts by creating two distinct types: non-bus-vectored (NBVI) and bus-vectored (BVI) interrupts. Each Multibus interrupt line can be individually defined through software to be a BVI or NVBI. Using BVIs, the interrupt capability of a Multibus system can be increased to 64 bus-vectored-priority interrupts.

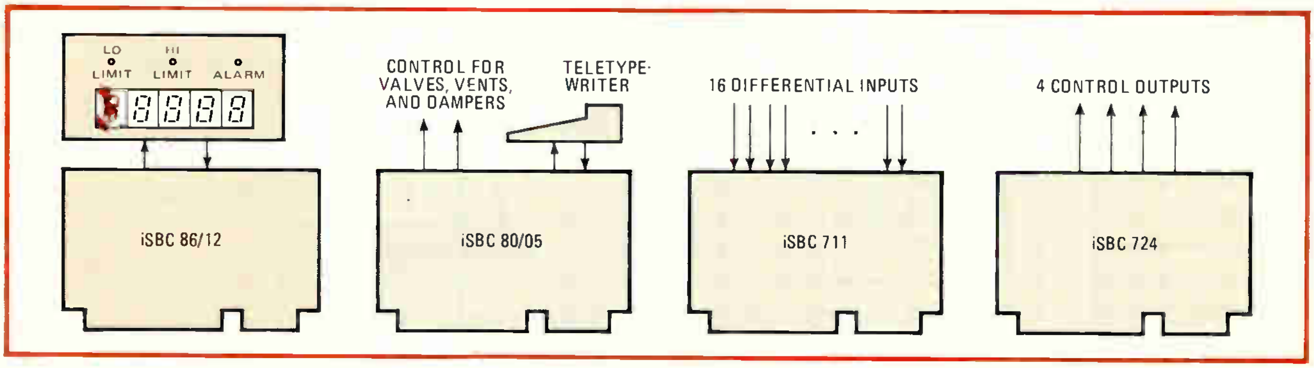
Using NBVIs, a slave module activates an interrupt line and the interrupted bus master generates its own restart address to service that interrupt. The Multibus address or data lines are not used. A BVI uses the Multibus address and data lines to communicate with the interrupting slave. When the slave module generates an interrupt, the bus master requires that module to generate the restart address. One additional command signal is



4. Open loop. Shown above is a simple alarm and monitoring system. The iSBC 711 analog-input board samples 16 differential inputs and the 8-bit iSBC 80/20 compares the inputs to the high and low limits. An alarm condition illuminates an LED and gets logged on a teletypewriter.



5. Closed loop. Suppose the system in Fig. 4 needs to be upgraded to handle a closed-loop system. For this application an iSBC 86/12 replaces the 80/20-04 to cope with the higher processing. The output control variables are handled by an iSBC 724 analog-output board.



6. Multi/master. To enhance the control system in Fig. 5, add a dedicated CPU to control valves, vents, and dampers that, in turn, affect pressure and flow parameters in the system. This has been done by adding an iSBC 80/05 in a Multibus/multimaster arrangement.

defined—interrupt acknowledge (INTA)—to request the restart address from the slave module.

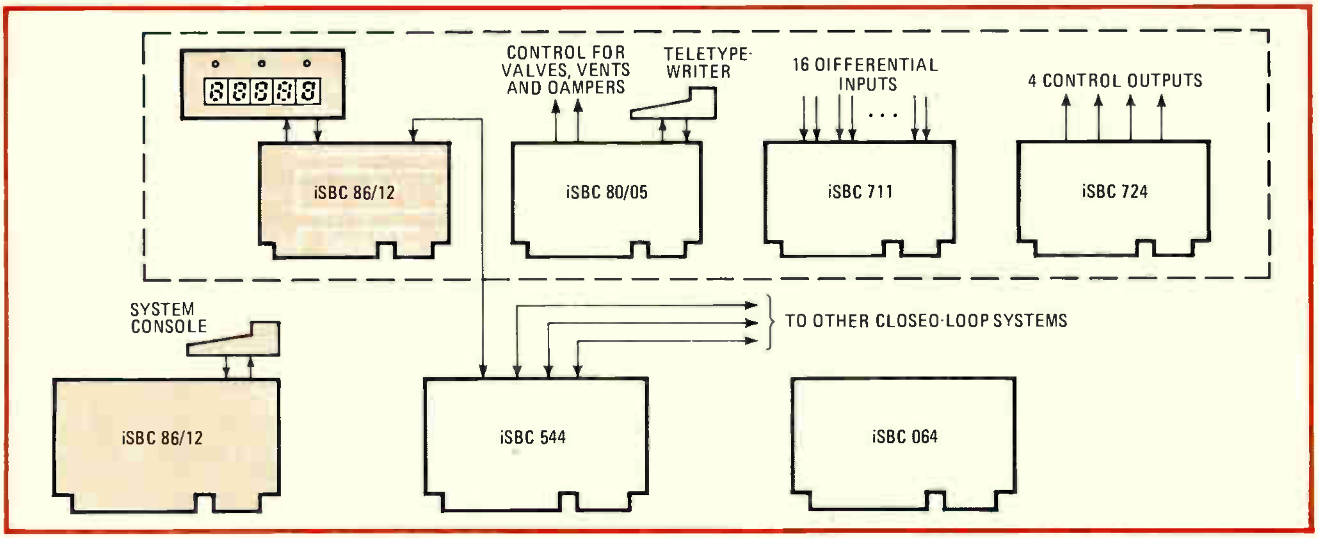
The iSBC 86/12 board architecture, like that of the 8-bit iSBC 80/30, is organized around a three-bus hierarchy: an on-board bus, a dual-port bus and a system bus (Multibus). All three buses have been expanded over their 80/30 counterparts to incorporate 20 address lines and 16 data lines.

The iSBC 86/12 architecture

The on-board bus links the 8086, all the I/O peripherals, and the read-only memory. Next in the hierarchy is the dual-port bus, which connects to the DP controller, 32 kilobytes of dynamic RAM, and the dynamic RAM controller. Finally, the system bus permits expansion of system resources through Multibus modules (Fig. 2).

The bus protocol of the iSBC 86/12 dictates that each of the three buses communicate with an adjacent bus or operate independently. When the CPU makes a request for a resource, the on-board and dual-port buses simultaneously determine if their hardware can fulfill the request. If the on-board bus is able to acknowledge the request, it does so and the DP bus is not disturbed. (The DP bus is not interrupted to determine whether it can acknowledge the request.) The 8086 always controls the on-board bus, and requested operations can be completed without delay. If the DP bus is needed, it is requested and the dual-port controller grants the use of the bus to the processor. Thereafter, the dynamic-RAM controller completes the operation and generates an acknowledge.

If neither the on-board nor the DP bus can satisfy the request, the CPU asks for the system bus. The 8086 must use the on-board and dual-port buses to communicate



7. Four loops. An iSBC 86/12 can be used in conjunction with an iSBC 544 intelligent communications controller to perform a supervisory function for four closed-loop systems. The iSBC 544 controls the line protocol and the iSBC 86/12 processes the 544's data.

with the system bus. The 8086 takes control of the DP bus when the system bus is granted. This prevents lockout problems with the DP bus—that is, when the processor requests the system bus while another bus master has control of it and is accessing the dual-port RAM.

Naturally, the fewer the buses it has to access, the faster the iSBC 86/12 completes a transaction. The on-board bus always operates at maximum board speed. But the DP bus operates at maximum board speed only if it was not busy or taken up with a memory refresh cycle. When the system bus is brought into play, the processor speed depends on the overhead in acquiring it and the type of Multibus module being accessed.

With this three-bus architecture the iSBC 86/12 can be operating over its on-board bus at the same time as another Multibus master is using the system bus. It does so by accessing data from the DP RAM at no reduction in board speed. The on-board bus permits access only from the 8086. Thus all I/O and ROM are private to the 8086.

The dual-port controller has two independent address decoders—one for the 8086 and one for the Multibus. The 8086 decoder fixes the 8086's RAM addresses from hexidecimal 00000 to 07FFF using a fusible-link programmable ROM. The Multibus decoder allows the user to select any address range for the on-board RAM by specifying two parameters—a top-of-memory pointer and the size of the accessible memory. The TOM pointer (as seen by another Multibus master) can be set to any 8-kilobyte boundary in the 1-megabyte memory space. The amount of memory on the iSBC 86/12 accessible by another master can be set to 8, 16, 24, or 32 kilobytes (or no access) with an on-board jumper. For example, fixing the accessible memory size to 24 kilobytes provides the 8086 with 8 kilobytes of RAM that only it can access. This private area can be used for the processor's stack, interrupt jump table and other special system parameters that are generally protected from other Multibus masters. The only addressing restriction is that the memory block accessible to the Multibus cannot cross a 128-kilobyte boundary.

Suppose a Multibus master wants to load a program into the iSBC 86/12's dual-port RAM for execution. Since the 8086's view of the DP-RAM address space is fixed, the Multibus address must be translated into the on-board 8086 memory space. The DP controller performs this translation by mapping the TOM pointer (as seen by other Multibus masters) to 8086-address 07FFFH, the top of the 8086's on-board RAM. Pointer − 1 is mapped to the top of 8086 on-board RAM − 1, and so on.

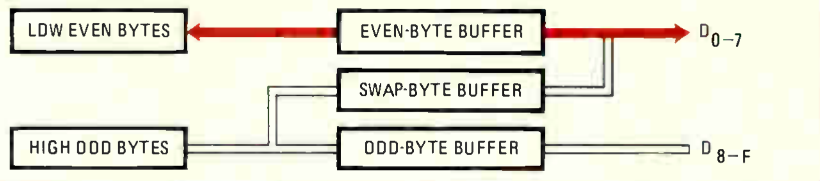
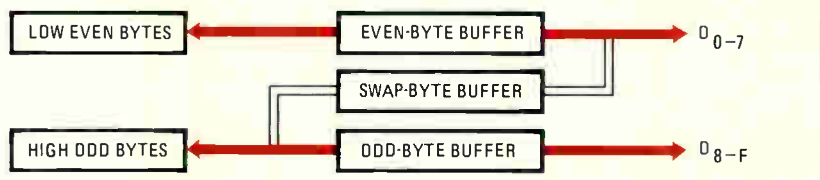
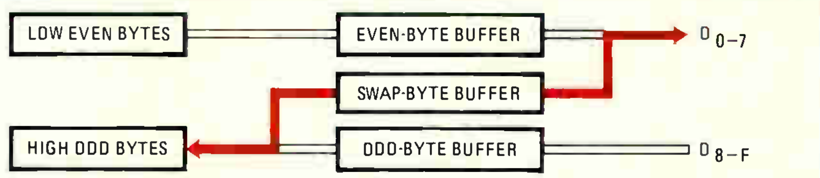
In the example shown in Fig. 3, the Multibus address selection is divided into three parts—two selecting the TOM pointer (X and Y) and one selecting the size of the accessible memory (Z). The TOM pointer is equal to a 128-kilobyte segment (X) plus address displacement (Y) from that segment. In this example, X is set to C0000H and Y is set to 0BFFFH, so the TOM pointer equals CBFFFH. Next, the size of the accessible memory (Z) is set, in this case to 8 kilobytes. This address translation makes the top 8 kilobytes of the 8086's RAM locations 06000H to 07FFFH available to another Multibus master when it addresses locations CA000H to CBFFFH. The 8086 still has 24 kilobytes (00000H to 05FFFH) of private memory.

Multiprocessing schemes

In multiprocessing systems, a master must be able to access the system without another master obtaining the bus. The iSBC 86/12 incorporates bus-arbitration logic to effect these transactions. Since the system bus is only requested when a system resource is needed, the iSBC 86/12 can perform true parallel processing with other iSBC 80 or 86 masters.

A typical example is the use of a common memory location that contains the status byte (busy/not busy) of a floppy-disk controller. When the floppy disk is needed, the master must first read the location and, if not busy, write the status word without another master obtaining the bus (to use the floppy disk). A bus-lock function on the iSBC 86, once enabled, allows the iSBC 86 to maintain control of the system bus until the lock is disabled by program control. This bus-lock function may

NEW MULTIBUS MEMORY ORGANIZATION

Data	Master	BHEN	ADRO	Data paths
8-bit even address	8-bit 16-bit mixed	0	0	
16-bit	16-bit	1	0	
8-bit odd address	8-bit 16-bit mixed	0	1	

be activated in one of two ways—by an output bit from the resident 8255A peripheral-interface chip or by a software prefix on any 8086 instruction. The iSBC 86 can perform the test and set function by exchanging the accumulator with the memory location, preceding the instruction by a lock prefix. For example, the status word is read into the accumulator and, without another intervening bus cycle, a busy status is written. The accumulator is then tested: if busy—try again (writing a busy does not destroy status as it was already busy); if not busy, the floppy disk is now under the master's control and the status location is set to busy.

The iSBC 86/12: a design tool

For system debugging and full-speed execution, the iSBC 86/12 can be linked to the Intellec microcomputer development system. Programs generated on the Intellec system can be downloaded into the iSBC 86/12 RAM via cables. Through a virtual-terminal capability, the Intellec console can directly access an iSBC-resident monitor, which provides commands for software debug. Once the debugging cycle is completed, the user has the option of uploading the software back to the Intellec for storage on diskettes.

The Multibus and form-factor compatibility of the 8-bit iSBC 80 and 16-bit iSBC 86 single-board computers provide a degree of design flexibility previously unobtainable. Initial design problems can be solved with low-cost 8-bit hardware. As product requirements evolve, 16-bit performance can be added. Eventually, 8- and 16-bit multiprocessor solutions can be conveniently implemented.

Consider the application shown in Fig. 4, an alarm and monitoring system in a typical process plant. Sixteen differential inputs from pressure and flow transducers are sampled once every second, then compared to high and low limits previously entered through thumbwheel switches. The iSBC 711 analog-input board takes care of sampling the inputs and the 8-bit iSBC 80/20-4 compares the data to the high and low limits. Whenever these limits are exceeded, an alarm LED lights up and the alarm condition is logged on the system teletypewriter along with input identification, high limit, low limit and sampled value.

Closed loops

Instead of an open-loop system, suppose the design must be enhanced to control four output variables—thereby making it a closed-loop system. The sampling rate must be increased to once every third of a second and more processing will be required to run through the control algorithm and output the control-loop data. For this application, and iSBC 86/12 replaces the 80/20-4 to handle the higher processing requirements. An iSBC 724 analog-output board is also added to provide the four output-control variables (see Fig. 5). Carrying this example one step further, one may want to dedicate another processor to controlling valves, vents, and dampers that in turn affect pressure and flow parameters in the system. This can be done by adding an iSBC 80/05 in a multimaster arrangement as shown in Fig. 6.

Finally, an iSBC 86/12 can be used with an iSBC 544 intelligent communication-controller to supervise four closed-loop systems of the type shown in Fig. 6. The 86/12 of each system interfaces with the supervisory system via its serial interfaces, which are connected to the iSBC 544's serial ports (see Fig. 7). The iSBC 544 performs the control functions associated with the line protocol. The supervisory iSBC 86/12 can access the iSBC 544's dual-port memory and can perform further processing of the data received from the four closed-loop systems. In this configuration large amounts of memory may be required; since the iSBC 86/12 can address up to 1 megabyte, this presents no problem. □

Getting rid of hook: the hidden pc-board capacitance

Those previously unexplained discrepancies in circuitry output can be traced and measured and then designed out

by Wallace Doeling and William Mark, *Tektronix Inc., Beaverton, Ore.*
and Thomas Tadewald and Paul Reichenbacher, *UOP Inc., Norplex Division, LaCrosse, Wis.*

☐ Lurking beneath the apparently stable surface of many printed-circuit boards is a mysterious and relatively unknown phenomenon: hook. What this seemingly capricious and thoroughly confusing effect can do to an electronic circuit is a design tragedy: apparently well-designed high-impedance circuitry performs below the specifications that both theory and experience firmly establish as reasonable claims. Even perfectly designed and assembled test instruments read incorrectly.

Hook may be defined as the effect on a signal's voltage caused by a change in pc-board capacitance with frequency. Board capacitance is created between pc-board conductors separated by dielectric material. It can change the response time of a square wave and can bring about erroneous responses at certain frequencies of sine waves.

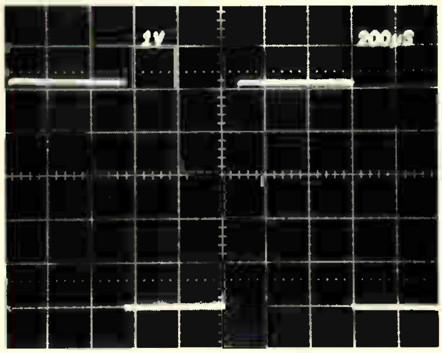
In an effort to lay bare the mysteries of hook, Tektronix and Norplex undertook investigations of the phenomenon [*Electronics*, July 6, p. 41]. The results tell a great deal about the causes and the effects of this hidden menace. They also make it imperative that designers no longer ignore the electrical parameters of the laminates onto which their brainchildrens' components and printed wiring go.

To that end, this article will discuss the nature of hook and will look at its causes and methods of measurement. It will show how precise measurements are clearing the way to understanding the variables that bring about hook, and it will suggest what both the users and the makers of the laminates can do.

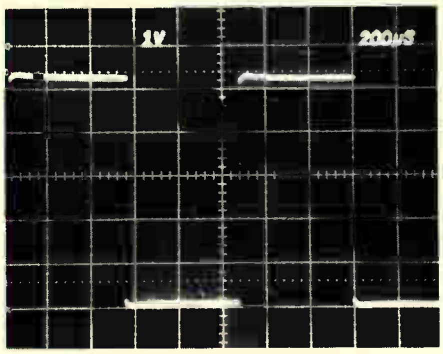
Variance with frequency

The investigations have discovered that the board capacitance that brings about hook varies inversely with frequency, up to about 10 kilohertz. From 10 to 100 kHz, it appears to be relatively flat.

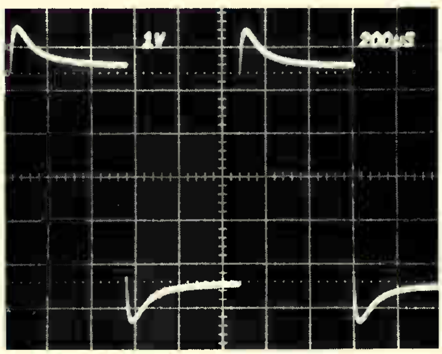
Apparently, above certain frequencies the molecular orientation and dipole-to-dipole alignment of the polymers used for pc boards do not change rapidly enough to cause variations in board capacitance. Below these



(a) LOW HOOK

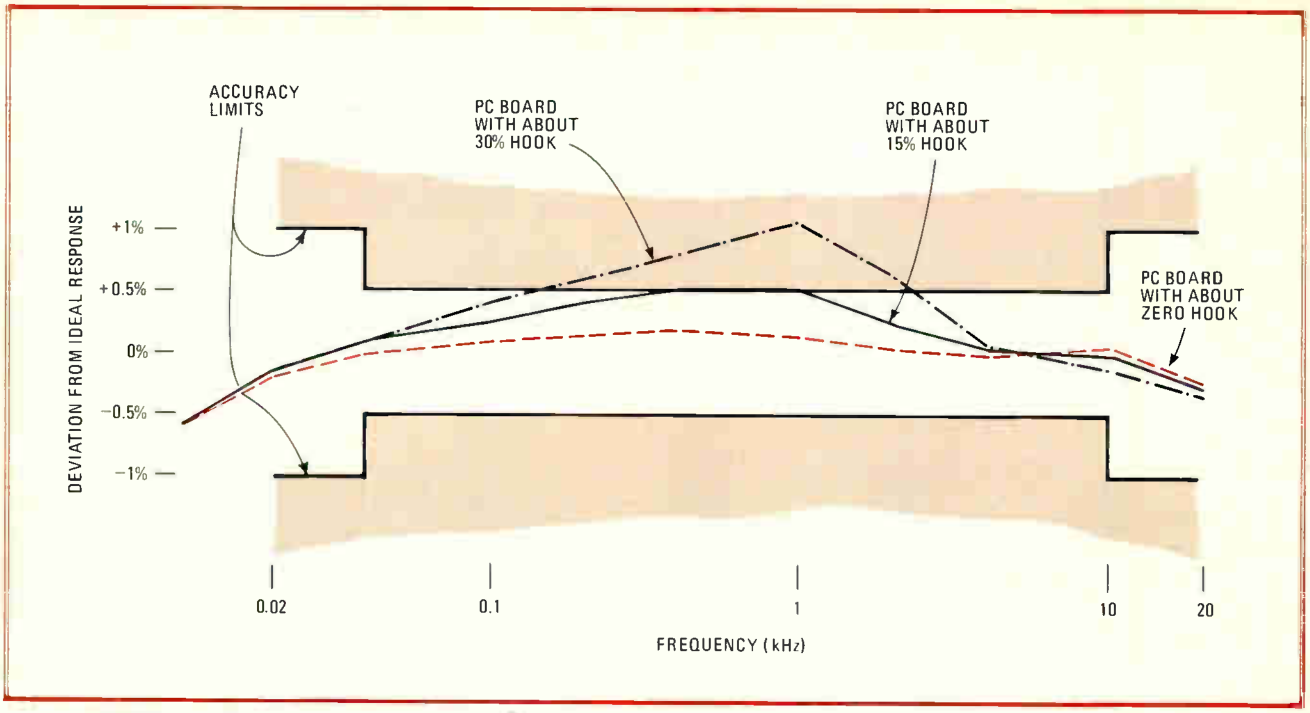


(b) MODERATE HOOK



(c) LARGE AMOUNT OF HOOK

1. Hook. These waveforms are at the outputs of three identical high-impedance networks, each mounted on its own pc board. One board (a) has low hook, a second (b) has moderate hook, and the third (c) has a large amount of hook.



2. Digital deviation. Digital multimeters are particularly vulnerable to large and medium values of hook, which can result in out-of-tolerance deviation measurements. This plot was taken for an ac voltmeter, using 100:1 high-impedance attenuators.

frequencies, the various molecular components orient themselves at differing time constants. Hence, capacitance varies with frequency.

The variable capacitance compounds the circuit designer's difficulties, for example, in the construction of high-impedance attenuators for oscilloscopes and digital multimeters. These attenuators are networks of resistors and capacitors connected to provide a diminished output proportional to the input signal's amplitude for all frequencies within the bandwidth of the instrument. The most frequently used method of interconnecting the components is with a pc board. Hook prevents the attenuator from giving outputs proportional to the inputs for the frequencies of interest.

Hook in scopes and DMMs

Tektronix assigns "hook" to describe a particular type of distortion seen on a waveform displayed on an oscilloscope. Figure 1a shows the proper response of a scope's attenuator to an input square wave. The leading edge should be square, with no overshoot and no undershoot.

The waveforms of Figs. 1b and 1c come from attenuators on printed-circuit boards with a moderate and a large amount of hook, respectively, and leading edges are no longer square. The deviation from a square wave is measured as a percentage of the latter's full amplitude, with an acceptable level of distortion being less than 0.5% to 1.5%, depending on the oscilloscope's performance requirements.

In digital multimeters, hook raises its ugly head in the ac voltmeter section. Attenuators in these meters generally use higher-value resistors than those of an oscilloscope, making the circuits even more susceptible to the high impedance of the board capacitance. The ac voltmeter function of a DMM is most accurate when measuring undistorted sine waves. Its measurement accuracy is usually specified as ±X% of the reading within a given bandwidth. Hook distortion for this function is best viewed by plotting a graph of the deviation of the displayed reading from the true input-signal amplitude.

Effects on accuracy

The effects of various amounts of hook on three DMMS of the same type are shown in Fig. 2. An ideal response curve plotted in this graph would be a straight line following the 0% deviation axis. With two of the DMMS, accuracy limits were exceeded between 700 hertz and 1 kHz. Hook in the pc boards renders these two instruments unsalable.

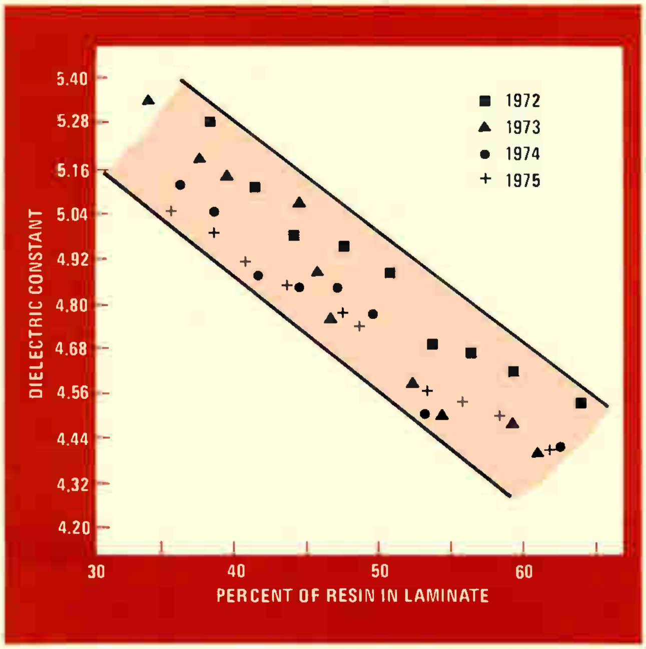
Hook can affect other circuits as well. In general, it will affect those in which all of the following occur:

- Resistors have high values (between 500 kilohms and 1 megohm).
- Board capacitance is an appreciable portion of the total circuit capacitance.
- Frequencies of interest are below 10 kHz.
- Required accuracy is better than 2% to 5%.

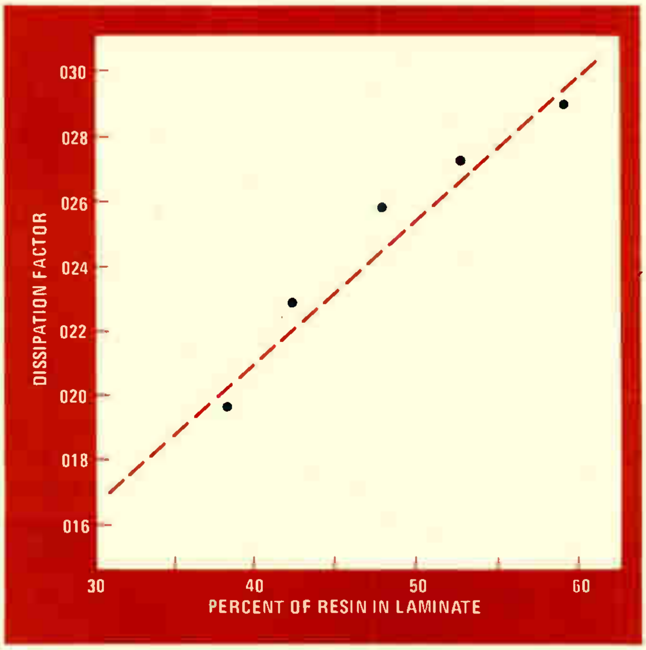
For such circuits, a quick way to gauge the effect of hook is to see if the board capacitance conducts an appreciable part of the signal current at frequencies below the 1-to-10-kHz range. If so, look for improper circuit operation with frequency variation.

Hook is not restricted to pc-board materials. It has been observed in dielectric materials used in some types of switches and capacitors, as well as in the junction capacitance and reverse-biased diodes and in metal-oxide-semiconductor capacitors. The investigations leading to this article, however, have been limited to pc-board capacitance.

Anything that affects board capacitance will affect



3. Dielectric constant. The dielectric constant decreases as the percentage of resin in the laminate increases. This data is from more than 600 samples of Norplex FR-4 laminates produced from 1972 to 1975, with resin contents varying from 30% to 75%.



4. Inverse relationship. The dissipation factor of boards made of FR-4 goes up with resin content, unlike the dielectric constant. The variation of both the dielectric constant and the dissipation factor are related to the amount of resin in a laminate.

hook. Thus the board's dielectric constant and its dissipation factor were early objects of the investigation into hook. Inquiry centered on the effects of such factors as resin content upon these two parameters.

Previous work showed that the dielectric constant (ϵ) and the dissipation factor (ϵ') of FR-4 (flame-resistant epoxy-glass) laminates to be proportional to resin content; ϵ decreases while ϵ' increases with increasing resin content. With F_r = fraction of retained resin in a given laminate, then:

$$\epsilon = 6.2 - 3 F_r$$
$$\epsilon' = 0.0037 + 0.0435 F_r$$

The constants in these equations apply to Norplex FR-4 laminates produced during 1972–75 and having resin contents varying from about 30% to 65%. For humidity conditioning, each laminate (over 600 samples) was submerged in distilled water for 24 hours at 23°C per MIL SPEC 13949E (D-23/23) before testing at 1 megahertz. The regular variations shown in Figs. 3 and 4 are generally consistent with the equations above.

Measuring hook

Because hook is a change in capacitance with a change in frequency, it is necessary to measure board capacitance at various frequencies. An important aspect of the Tektronix/Norplex investigations was to devise an accurate measurement method. Several techniques were studied, with varying results.

The simplest method of measurement is with a capacitance bridge. It can measure low capacitance values, 1 to 50 picofarads, at frequencies ranging as high as between 100 kHz and 1 MHz and as low as 10 Hz. However, the stray capacitance of the bridge can affect the measurement of low-capacitance samples. Another problem: most capacitance bridges are single-frequency devices.

A second measurement method is with a high-impedance attenuator. Such an attenuator (Fig. 5) can be constructed with two capacitances: C_1 being the board capacitance to be tested and C_2 being adjusted to produce an output waveform complying as closely as possible with the input square wave. The deviation, in percentage, of the output waveform from the input square wave indicates the relative amount of hook.

Wide frequency range

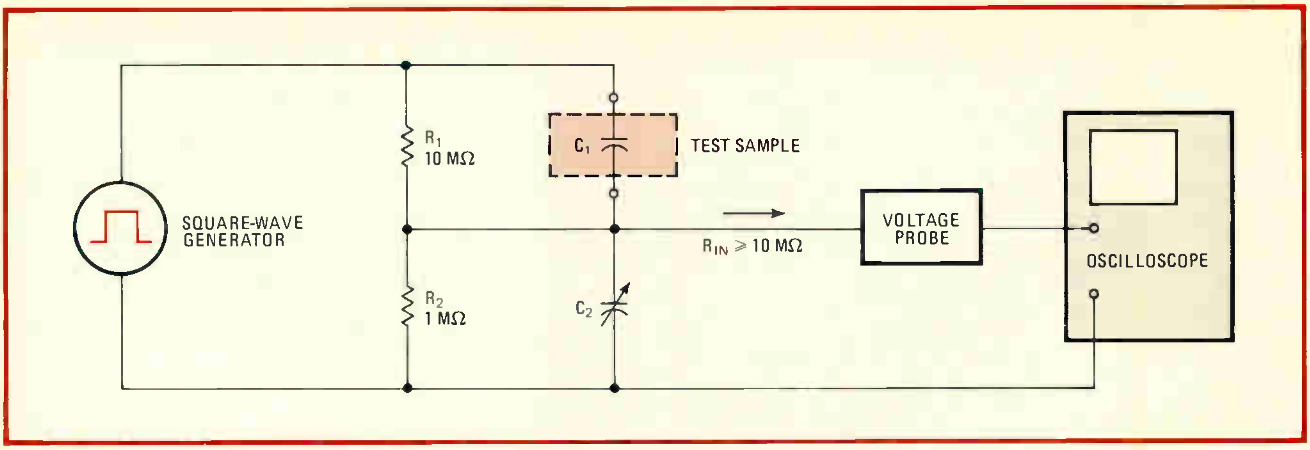
Since the square wave is composed of many frequencies, this measurement approach covers a wide range of frequencies at one time. Moreover, this technique is simple and economical, since it requires only an oscilloscope and a square-wave generator.

However, the attenuator method provides no direct reading of the quantity of hook (the change in capacitance), and stray capacitance in parallel may swamp out hook for low values of C_1 (less than 5 to 25 pF). At low frequencies (just where one most wants to measure hook), the 1-megohm resistors become the dominant elements of the circuit: thus the capacitance effect drops out of the picture.

The most exact way to measure hook is with the charge-amplifier circuit (Fig. 6). This is an operational amplifier with extremely low input bias currents—less than 0.1 picoampere is desirable, and 1 pA is maximum. This precision circuit uses capacitors as both the series-input and feedback impedances for setting the amplifier's closed-loop gain.

The output signal of the charge amplifier is a function of three parameters: the input signal; the fixed capacitance, C_f; and the sample's capacitance, C_i.

The relationship between these components is:



5. Playing hooky. One of the earlier methods of measuring hook uses a high-impedance attenuator with circuit-board capacitance as an element. However, a drawback is that the circuit is incapable of giving a direct reading of circuit-board capacitance.

TABLE 1: LAMINATE HOOK AT 10 Hz

Type	Resin	Reinforcement	% hook	
			Before humidity conditioning	After humidity conditioning
FR-3	FR – epoxy	paper	14	large
CEM-1	FR – epoxy	paper/glass	5	10
FR-4*	FR – epoxy	glass	4	9
G-11	high-temperature epoxy	glass	3	9
Polyimide	polyimide	glass	4	6
N-3	phenolic	nylon	9	14

*Average of 12 FR-4 laminate variations

$$V_{out} = \frac{C_i}{C_r}(V_{in})$$

If C_r is a known-accurate, high-quality capacitor exhibiting no hook, and if the characteristics and accuracy of V_{in} are known, then the characteristics of V_{out} can only be influenced by C_i.

The signal generator used can be either a sine-wave or a square-wave generator. A sine-wave generator allows capacitance measurement at any given frequency within the bandwidth of the system. A square-wave source allows a dynamic capacitance measurement at all frequencies within the spectrum of the square wave at one time; that is, it shows how the hook capacitance changes with time.

Actual measurements

With an acceptable measurement technique established, the evaluation of materials can start. For testing of laminates, two-sided boards with plated-through holes allow hook to be measured along three orthogonal axes. While X, Y, and Z values of hook often show differences for a given laminate, only the effect of laminate type on the average hook value will be presented here.

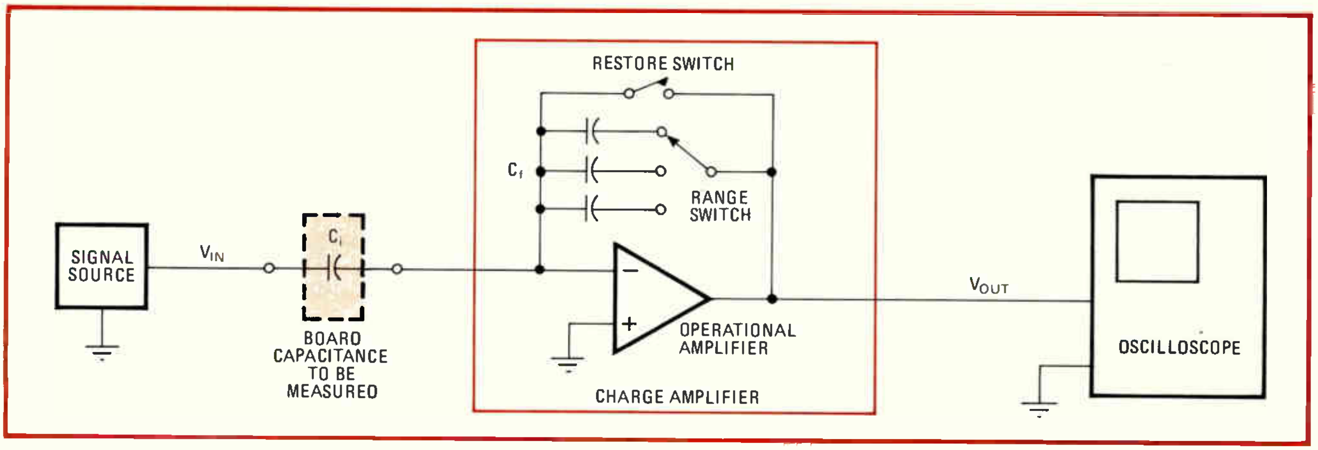
When measuring a good capacitor (one with no hook), the output signal can be expected to look exactly like the input from the signal generator. NPO ceramic and polypropylene capacitors (units with dielectrics having extremely low dissipation factors) can be inserted as standard C_is in the circuit of Fig. 6 to develop a reference waveform. Any distortion caused by the signal generator, oscilloscope, or charge amp will be seen in the output waveform associated with the standard C_i, allowing for compensation in any future measurements.

Figure 7 shows capacitance vs time measurements taken on a charge-amp circuit at Tektronix on FR-4 circuit-board materials that have low hook, moderate hook, and a large mount of hook. Hook is measured as a percentage given by the distance the waveform's leading edge has dropped divided by its peak-to-peak amplitude. Circuit-board materials measured are the same materials used in the attenuators that have their responses shown in Fig. 1. However in this case, capacitance is directly displayed.

The waveforms display capacitance vertically. The capacitance in Fig. 7a changes very little after the initial step, compared to the larger changes in Fig. 7b and 7c. In fact, the latter capacitances would continue to increase with a waveform of longer period.

Increase in capacitance

A measurement of board capacitance with a variable sinusoidal generator as the signal source of a charge-amplifier measurement circuit is plotted in Fig. 8.



6. Charge amplifier. An operational amplifier with capacitors as feedback elements can measure board capacitance directly. The wave shape of the signal can be either a sine or a square wave. A square-wave drive results in a display of hook capacitance vs time.

Board capacitance was measured at various frequencies from 1 Hz to 100 kHz. The graph shows that, for frequencies below 1 kHz, the change in capacitance rapidly increases.

Capacitance at still lower frequencies was not measured because of equipment limitations. Presumably it would continue to increase for frequencies somewhat below 1 Hz before reaching a limit.

At Norplex, measurements were made on 12 different types of FR-4 laminate, plus five other printed-circuit laminates. Hook was measured with a 10-Hz square wave before and after humidity conditioning. Results are given in Table 1, along with the composition of the various laminates.

Moisture absorption results in greater hook, and, for a given resin system, paper reinforcement is worse than glass fiber (see FR-3 and FR-4 in the table). These observations may be related: paper-based laminates absorb more moisture than those with glass-fiber bases.

Table 1 also shows that other resin systems, such as G-11 and polyimide, can be used to produce low-hook laminates. The N-3 nylon-phenolic laminate was an early attempt to study some less traditional systems.

Other factors

The Tektronix/Norplex investigations established that laminate construction and processing may affect hook as much as the materials used, as Table 2 shows. It offers data on the 12 different FR-4 laminate samples, each made somewhat differently. While hook varies substantially from sample to sample, it is possible to produce an FR-4 laminate with low hook, even after moisture

Advice for pc-board users

Current research into hook is beginning to lead to a good economical guarantee of relatively hook-free, FR-4 laminates for printed-circuit boards. But insufficient understanding of the cause of hook still precludes an accurate and reliable formula for the composition of hook-free material.

For instance, hook seems to be a batch- or lot-oriented problem. Years may pass, and several lots of material may be used with hook being low enough not to be objectionable. Then all at once a bad lot of material will be received and cause havoc. All vendors of G-10 or FR-4 laminate material used at Tektronix have supplied both good and bad lots of laminate.

There are, however, several methods that can reduce the effect of hook on circuits.

First, design the circuit and the layout of the printed-circuit board to minimize stray capacitance caused by pc interconnections. It may be necessary to mount all critical components on Teflon standoffs and to do point-to-point wiring to these posts rather than to points directly on the pc board. This keeps the circuit-board capacitance to a minimium, but, of course, drives manufacturing costs up.

Another problem: insufficiently cured laminate material can be noticeably hooky. Baking FR-4 material can be a remedy in some cases.

Another approach is to ask the laminate vendor to agree to a maximum hook specification. A few are now willing to address this requirement. Alternatively, this specification can be in the form of a limit on the change of dielectric constant of the material as measured at 100 kilohertz and at 10 hertz.

The Tektronix approach for FR-4 laminate is a combination of sampling of the incoming material by batch and measuring finished circuit boards for hook before component assembly. A hook test pattern, etched on samples of each batch of material received, checks all three axes. Use of the material in critical applications depends on the results of that test.

For these applications, a 100% check of the finished pc boards before component assembly provides further insurance against scrapping expensive finished boards because they do not meet performance specifications. The cost of a bad board found in an assembled instrument at the calibration stage can be tremendous.

Finally, one important step a laminate user can take is to explain his needs to the vendor. The vendor should realize that today's pc-board requirements go far beyond just supporting and interconnecting components. Today the dielectric properties of a circuit board are decidedly the most important.

absorption (see variation 12, for example).

Again, while high resin content throughout and on the surface of FR-4 laminates generally gave low hook results, the table indicates that other factors also affect laminate hook. It appears that resin-glass interactions are critical.

Hook measurements on laminates also have been made at 1 kHz and 100 kHz. Because of the tentative relation found between resin content and hook, correlations between surface resistance and hook were begun with new test patterns.

Not all variables have been explored in detail. The data was derived from measurements of hook at 10 Hz and at 1 kHz and surface (insulation) resistance at 500 V dc using a special board pattern in four different modes. Tests included four FR-4 types and two other laminates, each measured before and after moisture conditioning.

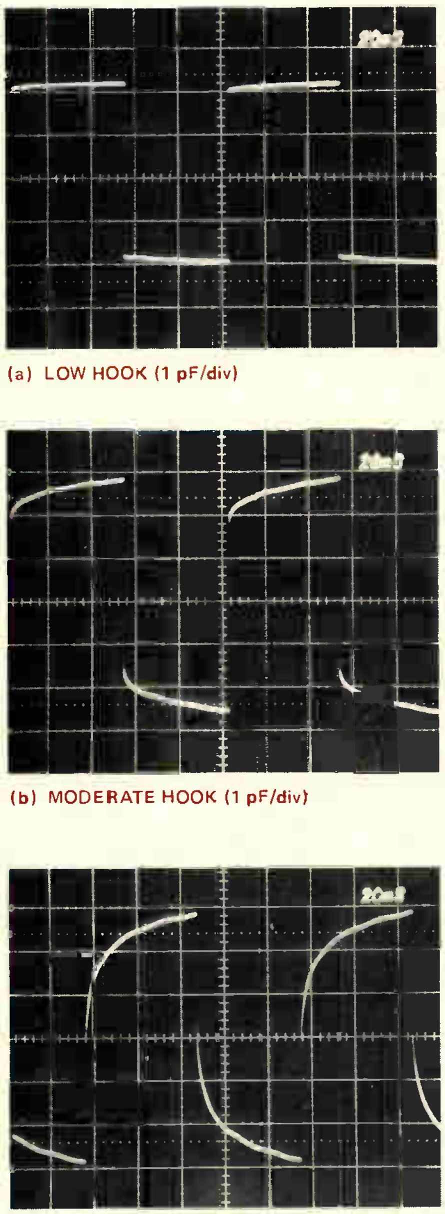
A note of caution: understanding data from experimental sets where many parameters affect the observed results often requires statistical interpretations to separate important from trivial parameters and to identify interactive parameters. The data bank is not complete enough to permit such rigorous interpretation; however, some trends do seem to be fairly apparent by now.

The data indicates that an increasing moisture content in laminates generally increases hook. The CEM (composite epoxy material) and polyolefin samples tested are not generally recognized laminate materials. The former is a variation of a CEM-3 construction (woven plus nonwoven glass fiber with FR-4 resin), and the polyolefin is Norplex's NZ-932 developmental laminate designed for certain specialized applications.

The results for the various FR-4 types reinforce a conclusion stated earlier. While moisture and material type influence hook, variations within a given laminate show that the process of fabrication also strongly influences hook.

While increased moisture content usually raises the hook of a given laminate, it also increases the material's dielectric constant and decreases resistance, even if no more than traces of ionic materials are present. Therefore, hook would be expected to decrease with increasing laminate resistance.

Test results generally confirm this expectation at each of the frequencies used for these surface hook measure-

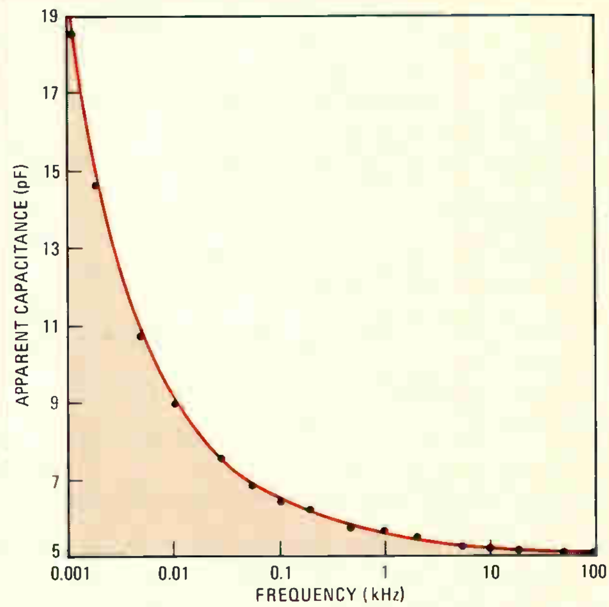


(a) LOW HOOK (1 pF/div)

(b) MODERATE HOOK (1 pF/div)

(c) LARGE AMOUNT OF HOOK (2 pF/div)

7. Capacitance vs time. Typical capacitance vs time measurements were taken on FR-4 laminates with a charge amplifier. The hook capacitance associated with moderate and large amounts of hook would continue to increase if a longer period were used.



8. Sinusoidal drive. Driving the charge-amp capacitance-measuring circuit with a sine-wave generator produces a curve of this type for a board with considerable hook. Change in board capacitance is particularly rapid in the dc-to-10-kHz range.

TABLE 2: HOOK IN FR-4 VARIATIONS (10 Hz)

FR-4 variations	Resin content	Resin at surface	% hook	
			Before humidity conditioning	After humidity conditioning
1	low	low	5	12
2	high	low	5	6
3	low	low	5	12
4	low	low	4	11
5	low	high	4	11
6	high	high	4	11
7	high	high	4	8
8	high	high	4	7
9	low	high	3	11
10	high	high	3	7
11	high	high	3	7
12	high	low	2	4

What the laminate vendor can do

The present state of the art permits tests of hook in laminate material, which do in fact relate to end-use performance. However, evaluation of the role of laminate manufacturing techniques in the production of hook should be continued and expanded. This work would develop the necessary theory for the consistent production of laminates that exhibit minimal signal aberration over a wide range of operating conditions.

To assure uniform resin composition, incoming materials should be analyzed in a number of ways with an integral role assigned to chromatography, which separates and analyzes mixtures of chemical substances by differential absorption. This technique determines resin molecular distribution, which must be reproducible in order to maintain a variety of constant laminate electrical properties, including low hook.

Additionally, researchers at laminate manufacturers are using chromatographic processes to separate various fractions from the polymers. This activity will allow a better understanding of the hypothesis that molecular polarizability has a dominant effect on laminate dielectric properties such as hook.

The makers of printed-circuit boards primarily use epoxy-glass-supported laminates for most sophisticated applications, such as wide-band, high-speed, low-drift analog circuitry. Earlier, phenolic products chiefly were used, but the increasing need for electrical stability in the electronics industries is beyond the capabilities of the phenolics. There is some concern that as electronics design becomes more refined, the epoxy-glass system will also become inadequate. This is the main reason for continuing to look at other materials in the polymer world.

ments; however, the picture is not entirely clear. Some discrepancies in the results may be partly due to measuring surface resistance at 500 v dc while measuring hook using a 30-v square wave. It is not expected that surface resistance will depend on frequency or amplitude, but this deserves consideration in future inquiries.

More importantly, the laminate test results reinforce the notion that materials and the methods used for laminate construction are important in determining hook. The surface hook for the two experimental laminates, CEM and polyolefin, is especially sensitive to surface resistance changes.

In other words, moisture conditioning of these laminates caused only small changes in surface resistance (relative to most of the FR-4 laminates), while significant changes in surface hook were measured. It is clear that no simple mathematical relationship between laminate hook and resistance has yet been identified. While investigations into hook are well launched, there is a long voyage ahead until all the factors that produce hook are pinned down and a mathematical relationship relating these factors is derived. □

Closing the loop

The authors will answer questions on this article. For telephone inquiries until Friday, Oct. 20, the Tektronix authors may be reached from 9 a.m. to 5 p.m. Pacific Standard Time at (503) 644-0160, and the Norplex authors may be reached from 9 a.m. to 5 p.m. Central Standard Time at (608) 784-6070. Direct written inquiries to: Tektronix, P. O. 500, Beaverton, Ore. 97077, or Norplex Division, UOP, 1300 Norplex Drive, LaCrosse, Wis. 54601

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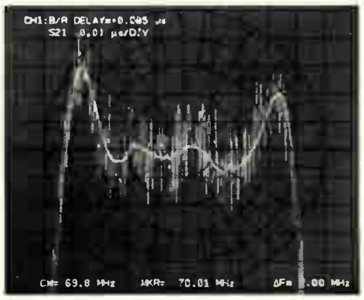
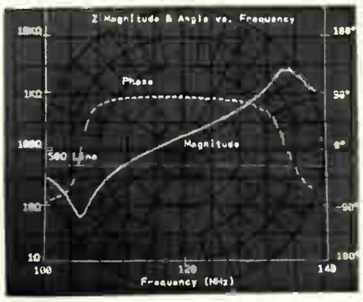


Group Delay of 70 MHz bandpass filter with and without averaging. (Vert. scale: 5nsec/div)

When the HP-IB programmable 8501A is combined with the automatic 8505A/computing controller combination, the system offers versatile display capabilities for text and graphics plus high-speed digitizing for fast, yet precise and comprehensive measurements.



Reflection Coefficient data reformatted to impedance magnitude and angle.

Circle 119 on reader service card

Communications in orbit

Table summarizes important operating characteristics of present and soon-to-be-launched satellites

by Wilbur L. Pritchard, *Satellite Systems Engineering Inc., Washington, D. C.*

☐ *So rapidly is the satellite business expanding that even engineers responsible for the planning and usage of communications networks find it hard to keep up. Over 55 active satellites are in geostationary orbit today and more are under construction in a total of some 25 programs. The accompanying table summarizes the principal characteristics of current programs.*

The service each program offers is indicated by means of International Telecommunications Union designations and the traditional band letters for frequency. These frequencies are approximate figures only, since the actual frequency assignment details are complicated and vary from region to region throughout the world. Anyone requiring this more specific information should consult the system operator or the Federal Communications Commission's Radio Regulations.

All but one

With the exception of one system, all the satellites are in a circular orbit in the plane of the earth's equator and about 19,323 nautical miles above it. Their rotation period is 23 hours, 56 minutes, and 4.09 seconds, or one sidereal day, so that, with minor adjustments for perturbations, they maintain a fixed, geostationary position relative to any point on the earth.

The Molniya System deployed by the Soviet Union several years ago is the exception. It has a highly elliptical orbit with a period of about 12 hours, an apogee of 40,000 kilometers, and, most important of all, a 62½° inclination to the equator. In this alignment, the major axis of the ellipse does not rotate, but stays constant relative to the earth. Consequently, the apogee remains over the Northern Hemisphere, so that most of the time the individual satellites remain within view of the far northern reaches of the Soviet Union. Payloads can also be greater in this orbit than if they had to make the sharp turn into equatorial orbit that would be needed from a northern launch site. Tracking earth stations are required, however, as is periodic hand-over from one satellite to another.

The stabilization system for satellites is usually described as either spin or three-axis. But since spinning satellites with despun platforms are also stabilized along three axes so far as the antenna beams are concerned, it would be more accurate to describe the two types as drum-stabilized and wheel-stabilized. The mass in every case is the initial weight on final orbit, including station-keeping propellant.

The primary power figure shows the total number of watts available from the on-board solar array during equinox at the beginning of life. Typically, power requirements depend not only on the total radiated power but also on the receiver system, degree of redundancy, and the amount of service to be provided during eclipses of the sun. Variations in these elements from one program to another account for the differences in primary power in relation to the radiated radio-frequency power.

As for the kinds of transponders and antenna beams that are available, only an approximate picture can be given, because the system block diagrams for most of these satellites show a great variety in redundancy, switching possibilities, and bandwidths. The number of transponders is equal to the number of rf channels with the bandwidths as shown in the row below.

The satellite receiver figure of merit may have more than one value. These apply to different beams or transponders or bandwidths and this is evident from the rest of the chart. Similar considerations hold for certain other specifications.

Still more variety

A wide variety of modulation and multiple-access systems is available and their implementation is usually standard. For example, multiple voice channels start out by being multiplexed by terrestrial communications systems using single-sideband modulation. In this approach, voice channels are stacked up in groups of 12 each on a subcarrier. An alternative approach is to code the voice signals with either pulse-code or delta modulation and time-division–multiplex a collection of channels. These voice channels are synthesized into composite signals at high bit rates—typically 1.544 megabits per second.

It is important not to confuse the radio-frequency carrier modulation system with the multiple-access scheme for many earth stations using the same transponder. Note also that the single-channel-per-carrier technique is a special type of frequency-division multiple access. ☐

Electronics

A USER'S GUIDE TO COMMUNICATIONS SATELLITES

	Intelsat IV	Intelsat IV-A	Intelsat V		Molniya	Statsionar	Anik A	Anik B	Anik C	RCA Satcom	WU Westar
Service[1]	fixed tel., TVD	fixed tel., TVD	fixed tel., TVD		fixed tel., TVD	fixed	fixed tel.	fixed tel.	fixed	fixed tel., TVD	fixed tel., TV,TTY
Frequencies[2]	C	C	C	Ku	L, C	C	C	C/Ku	Ku	C	C
Launch vehicle	Centaur	Centaur	Centaur (shuttle or Ariane)		A–2 Soyuz	A–2 Soyuz	Thor Delta 2914	Thor Delta 3914	Thor Delta 3910/STS	Thor Delta 3914	Thor Delta 2914
Prime contractor	Hughes	Hughes	Ford				Hughes	RCA	Hughes	RCA	Hughes
Stabilization	spin	spin	3-axis		3-axis	3-axis	spin	3-axis	spin	3-axis	spin
Mass (kg)	731	790	1,012		1,000	1,250	272	440	522	461	297
Primary power (W)	569	708	1,220		500		300	840	925	770	300
Coverage[3]	global spot	global hemisphere spot	global hemisphere zonal	spot	global USSR	global spot	Canada	Canada	Canada	Conus Alaska, Hawaii	Conus
Number of transponders	12	20	21	6	1 32	6	12	12/6	16	24	12
Transponder bandwidth (MHz)	36	36	36 72	72 240	40 10	40	36	36 72	54	34	36
Number of antenna beams	6/4	7/3	5/5	2: East and West	1	2–4	1	1 4/1	4/1	2	2
Polarization	circular	circular	circular	linear	circular	circular	linear	linear	linear	linear	linear
G/T (dB/K) (figure of merit)	−18.6	−11.8	−18.6 −11.6 − 8.6	0.0 E 3.3 W	−10	−15.8	−7	−6/−1	+1	−5 −10	−6
EIRP (dBW) (effective isotropic radiated power)	22.5 34.5	22 26 29	23.5, 26.5 26, 29 29	41.4 E 44.4 W	35 26	30.8	33	36 47.5	48	32 26	33
Modulation[4]	FDM/fm fm QPSK SCPC	FDM/fm fm QPSK SCPC	FDM/fm fm QPSK	FDM/fm fm QPSK	FDM/fm	FDM/fm	FDM/fm QPSK, SCPC	FDM/fm QPSK, SCPC	FDM/fm QPSK, SCPC	FDM/fm QPSK SCPC	fm QPSK
Multiple access[5]	FDMA TDMA	FDMA TDMA reuse	FDMA TDMA reuse	FDMA reuse	FDMA	FDMA	FDMA TDMA	FDMA TDMA	FDMA TDMA reuse	FDMA	FDMA TDMA

	TDRS Advanced Westar		Comstar	Indonesia Palapa	SBS	Comsat Marisat	(ESA) Marots 1	Insat		Symphonie
Service[1]	fixed		fixed tel.	fixed tel., TV	fixed tel., TV	mobile tel., TTY	mobile tel., TTY	fixed TV and radiometry		fixed experimental
Frequencies[2]	C	Ku	C	C	Ku	L ship C shore	L ship C shore	S	C	C
Launch vehicle	STS		Atlas Centaur	Thor Delta 2914	Delta 3910 or STS	Thor Delta 2914	Thor Delta 3914	3910		Thor Delta 2914
Prime contractor	TRW		Hughes	Hughes	Hughes	Hughes	HSD	Ford		CIFAS
Stabilization	3-axis		spin	spin	spin	spin	3-axis	3-axis		3-axis
Mass (kg)	2,132		810	300	460	326	466	1,054 (into transfer)		230
Primary power (W)	>1,204		760	300	1,000	330	500	1,250		300
Coverage[3]	Conus, Alaska, Hawaii	Conus	Conus, Puerto Rico, Alaska, Hawaii	Indonesia	Conus	global	global	India		Europe, North America
Number of transponders	12	4	24	12	10	2	3	2	12	2
Transponder bandwidth (MHz)	36	225	36	36	43	4	2.5 3.0 0.5	36	36	90
Number of antenna beams	2	7	4	1	1	1	1	1		2/1
Polarization	linear	linear and circular	linear	linear	linear	circular	circular	linear		linear
G/T (dB/K) (figure of merit)	−7 −12.5 −12.5		−8.8	−7	2 to −2	−17 −25	−11.2 ?	—		−15.0
EIRP (dBW) (effective isotropic radiated power)	33 28 26	42 − 50.3	33	32	43.7 to 40	20–29.5 18.8	35.5 ?	34	42	29
Modulation[4]	fm QPSK	250 Mb/s TDMA	FDM/fm	fm fm/SCPC	QPSK	fm BPSK	CPSK fm SCPC	fm QPSK		fm QPSK
Multiple access[5]	FDMA TDMA	beam switching	FDMA reuse	FDMA	TDMA	TDMA FDMA	TDMA	FDMA		FDMA

	NASA ATS-6	CTS	Japan BS	Japan CS	Sirio	OTS/ECS	DSCS II	DSCS III	(UK) Skynet 2B	NATO III	Fleetsatcom
Service[1]	broadcast experimental	fixed experimental	broadcast experimental	fixed experimental	fixed experimental	fixed	fixed military	fixed military	fixed military	fixed military	mobile military
Frequencies[2]	S,C, uhf	Ku	Ku	K/C	Ku, Kc	Ku	X	X	X	X	uhf, X
Launch vehicle	Titan IIIC	Thor Delta 2914	Thor Delta 2914	Thor Delta 2914	Thor Delta 2910	Thor Delta 3914	Titan IIIC	Titan IIIC shuttle	Thor Delta 2313	Thor Delta 2914	Atlas Centaur
Prime contractor	Fairchild	CRC Canada	Toshiba/ GE	Mitsubishi/ Ford	Compagnia Nazionale Aerospaziale	Hawker Siddeley Dynamics	TRW	GE	Ford	Ford	TRW
Stabilization	3-axis	3-axis	3-axis	spin	spin	3-axis	spin	3-axis	spin	spin	3-axis
Mass (kg)	1,356	350	352	340	218	324	536	748	232	340	862
Primary power (W)	600	1,260	1,000	521	118	600	520	800	258	538	1,435
Coverage[3]	various	1,850-km spot	Japan	Japan	North Atlantic, Europe spot	spot Europe A Europe B	global spot	global spot	global	Atlantic Europe	global
Number of transponders	6	2	2	6/2	1	6	4	6	2	2	13
Transponder bandwidth (MHz)	12 30 40	85	50 80	200	32	120 40 5	410 total	395 total	20 2	17 85 50	0.025
Number of antenna beams	10	2	1	1	3	3	3	multiple array	1	2	1
Polarization	linear and circular	linear	linear	circular	circular	linear, linear, circular	circular	circular	circular	circular	circular
G/T (dB/K) (figure of merit)	13.5 to −20	7.8	−8.2	noise figure = 13 dB/9 dB	−22.2, −17.2	4.2 −4.8 −2.2	8.5 20.2	−1.0, −16.0	−17	−14.1	−16.7 (uhf)
EIRP (dBW) (effective isotropic radiated power)	54.5–17	60	55	37 29.5	24	48.5 39.5 42.0	28 40	23–40	17.2 23.2	35 29	26–28 (uhf) 27
Modulation[4]	various	fm video	fm and digital	100-Mb/s digital	PCM–PSK and fm video	fm PSK	fm QPSK	fm QPSK	fm QPSK	fm QPSK	fm QPSK
Multiple access[5]	various	FDMA	SCPC	TDMA	SCPC	TDMA	FDMA TDMA CDMA	FDMA TDMA CDMA	CDMA FDMA	CDMA FDMA	FDMA

[1] Fixed — satellite service to specified fixed points
Mobile — satellite service to ships, airplanes, and mobile ground terminals
Broadcast — satellite service intended for reception by the general public
TTY — teletypewriter
Tel. — telephone
TVD — television distribution

[2] P band or uhf — 200 to 400 MHz
L band — 1,530 to 2,700 MHz
S band — 2,500 to 2,700 MHz
C band — 3,700 to 4,200 MHz
5,925 to 6,425 MHz
6,625 to 6,875 MHz

X band — 7,250 to 7,750 MHz
7,900 to 8,400 MHz
K band — 10.95 to 11.2 GHz
11.45 to 12.2 GHz
12.5 to 12.75 GHz
14.0 to 14.5 GHz
17.7 to 20.2 GHz

[3] Conus — continental United States without Alaska and Hawaii

[4] SCPC — single channel per carrier
FDM — frequency-division multiplexing
fm — frequency modulation
PCM — pulse-code modulation
PSK — phase-shift keying
BPSK — binary phase-shift keying
QPSK — quadri phase-shift keying (four-phase-shift keying)
CPSK — coherent phase-shift keying

[5] CDMA — code-division multiple access
FDMA — frequency-division multiple access
TDMA — time-division multiple access
Frequency reuse — same carrier frequencies assigned to different users through use of separate beams or polarizations

This chart was compiled by Satellite Systems Engineering Inc., Washington, D.C. 20014

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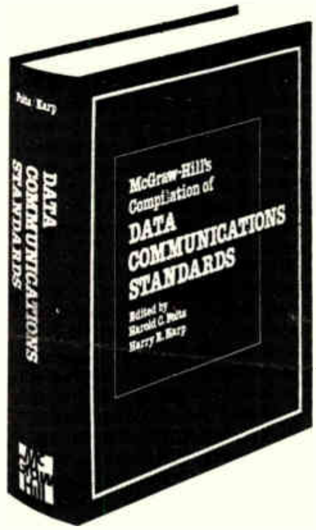

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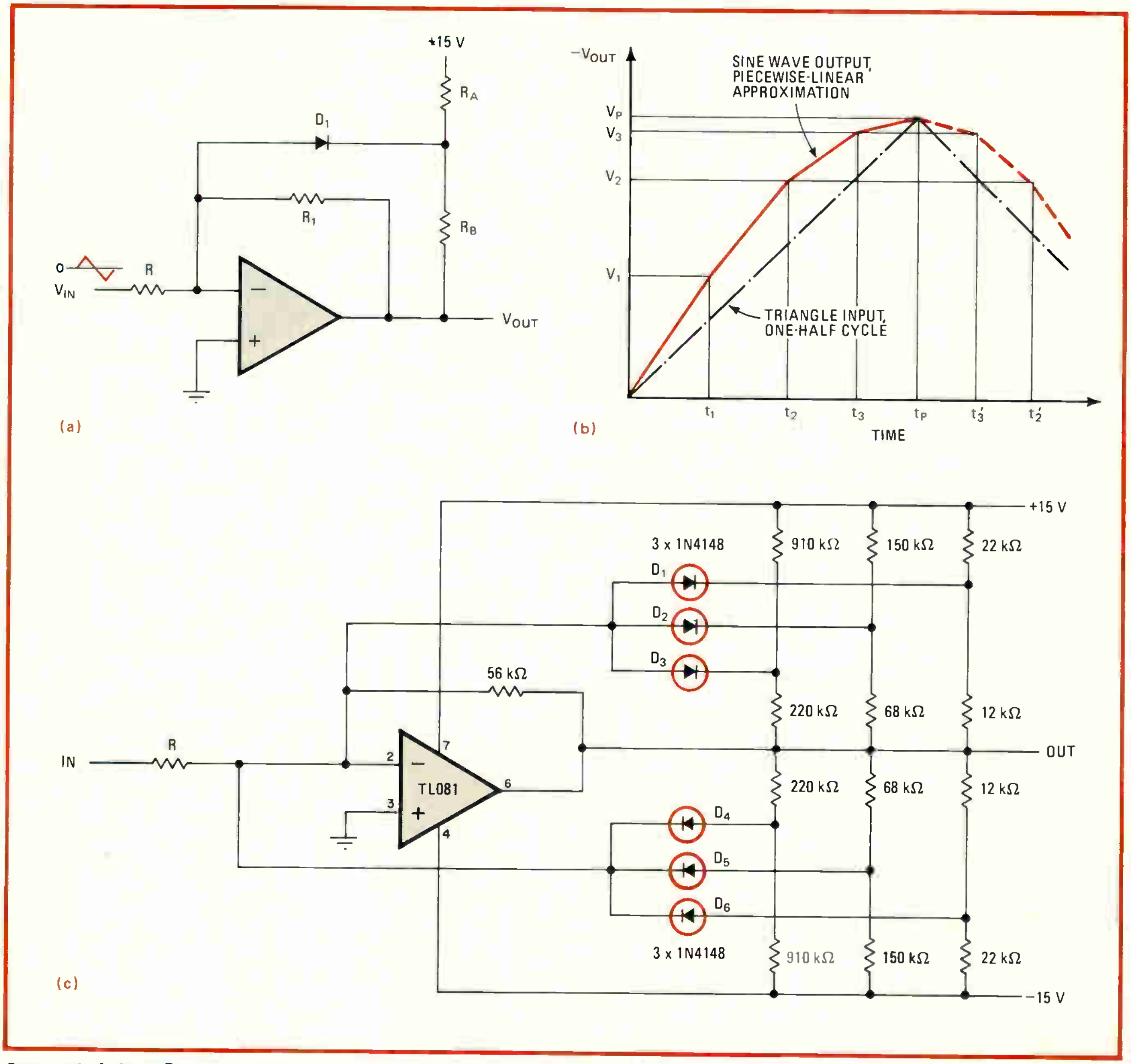
EL 1

Diode-shunted op amp converts triangular input into sine wave

by Giovanni Righini and Franca Marsiglia
Florence, Italy

Finding applications in low-frequency function generators, linear voltage-controlled oscillators, and, in general, wherever it is necessary to have an output with a constant amplitude that is independent of frequency, this converter transforms a bipolar triangular wave into a sinusoidal output having a total harmonic distortion of less than 1%. The circuit uses a single operational amplifier and several diodes placed across its input and output ports to synthesize a transfer function that decreases the amplifier gain as output voltage increases. Thus it generates a piecewise-linear approximation of a sine wave for corresponding changes in triangular-signal amplitude.

The principle upon which the converter operates is simple, as shown in (a). If the input voltage to the op



Segmented sines. Diode and resistors (a) reduce op amp gain when output signal falls, placing point C at 0.6 volt. Circuit can be expanded to generate piecewise-linear approximation of half a sine wave (b) from triangle wave when other diode-resistor networks are added (c) to reduce gain further with increasing input voltage. Adding D_4–D_6 networks permits generation of other half cycle of sine wave.

amp is such that the output voltage is positive, diode D_1 does not conduct and the amplifier gain will be R_1/R. But when a positive input voltage from the triangular input is applied to the inverting port, the output will go negative and D_1 will conduct when point C reaches a threshold value of -0.6 volt.

In effect, if the internal impedance of the diode is neglected so long as it is conducting, resistor R_b is in parallel with R_1, and the amplifier gain is reduced to $R_1R_b/(R_1+R_b)R$. The change in gain occurs at point V_1 on the transfer function (b).

By placing additional resistor-diode networks that include D_2 and D_3 at the output of the op amp (c) and by selecting resistor values appropriately, the voltage at which conduction occurs for each diode can be set. So, for each progressive rise of the triangular voltage the transfer function can be extended to points V_2 and V_3. A good approximation to a half sinusoid can be obtained by using four segments for every quarter of a (sine wave) period, as shown.

To process the negative-polarity portion of the triangular wave (which is required to generate the other half of the sine wave), resistor-diode networks including D_4, D_5, and D_6 are placed in the circuit. Note that the diodes will conduct in sequence as the op amp's output voltage exceeds the predetermined positive values.

The component values have been selected to produce three segments corresponding to end-point values of $|V_1|=4.35$, $|V_2|=7.7$, $|V_3|=9.15$. V_P is limited by the maximum voltage of the input signal. Only resistors having a tolerance of 5% or below should be used in this circuit, to keep distortion to a minimum.

The gain of the op amp is most conveniently controlled by varying R and can be selected to handle a wide range of input voltages—from a few tens of millivolts to tens of volts. R should be about 1.8 kilohms for input voltages of 1v peak to peak and should be trimmed to minimize sine-wave distortion at the output.

The frequency response of the circuit will exceed 30 kilohertz when the TL081 op amp is used. □

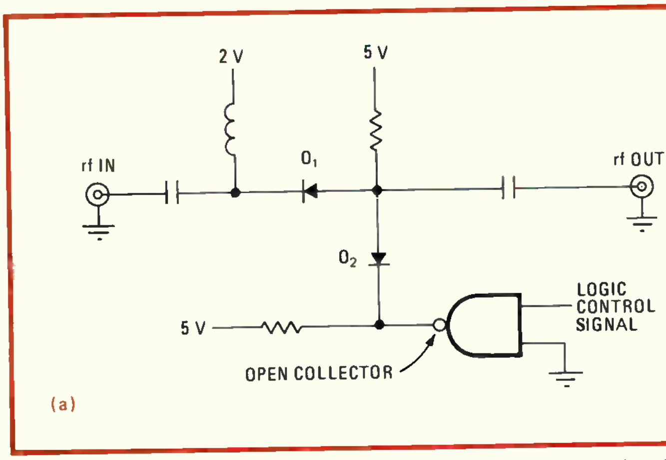
Open-collector logic switches rf signals

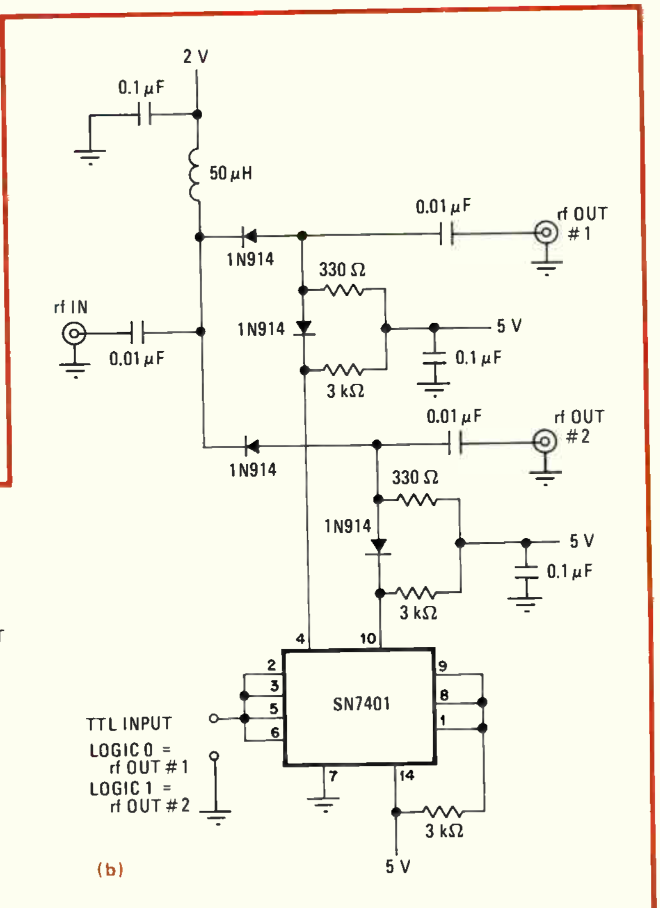
by W. B. Warren
TRW Subsea Petroleum Systems Inc., Houston, Texas

The open-collector outputs of transistor-transistor logic can provide a simple way of switching low-level radio-frequency signals and thus digitally selecting signal sources in test equipment or filters in a communications receiver. With a 50-ohm source and load, the rf attenuation through the switch at 10 megahertz is only 1.3 decibels when the switch is active and greater than 40 dB when it is open.

Shown in (a) is the basic rf switching element. When the logic control signal is low, the open collector output of the NAND gate is high. Thus diode D_1 is back-biased, D_2 conducts, and the switch is turned on. The capacitance of the open-collector output of the logic element will not affect circuit operation, since the reverse-biased D_1 prevents the element from shunting the rf path.

When the control signal is high, the open-collector output is low and D_1 conducts, forcing the dc voltage at





Digital rf switch. Logic signal is capable of switching low-level radio-frequency signals without significant attenuation, if open-collector transitor-transistor-logic element is used (a). Basic idea can easily be extended to single-pole, double-throw rf switch (b).

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the junction of the diodes to a low value. The voltage across D_1 is therefore not sufficient to keep it conducting (that is, it is reverse-biased), and the rf signal cannot appear at the output.

The application of the basic element to a single-pole double-throw rf switch is shown in (b). Logic control for the SPDT switch is provided by two 7401 open-collector NAND gates. □

Converters simplify design of frequency multiplier

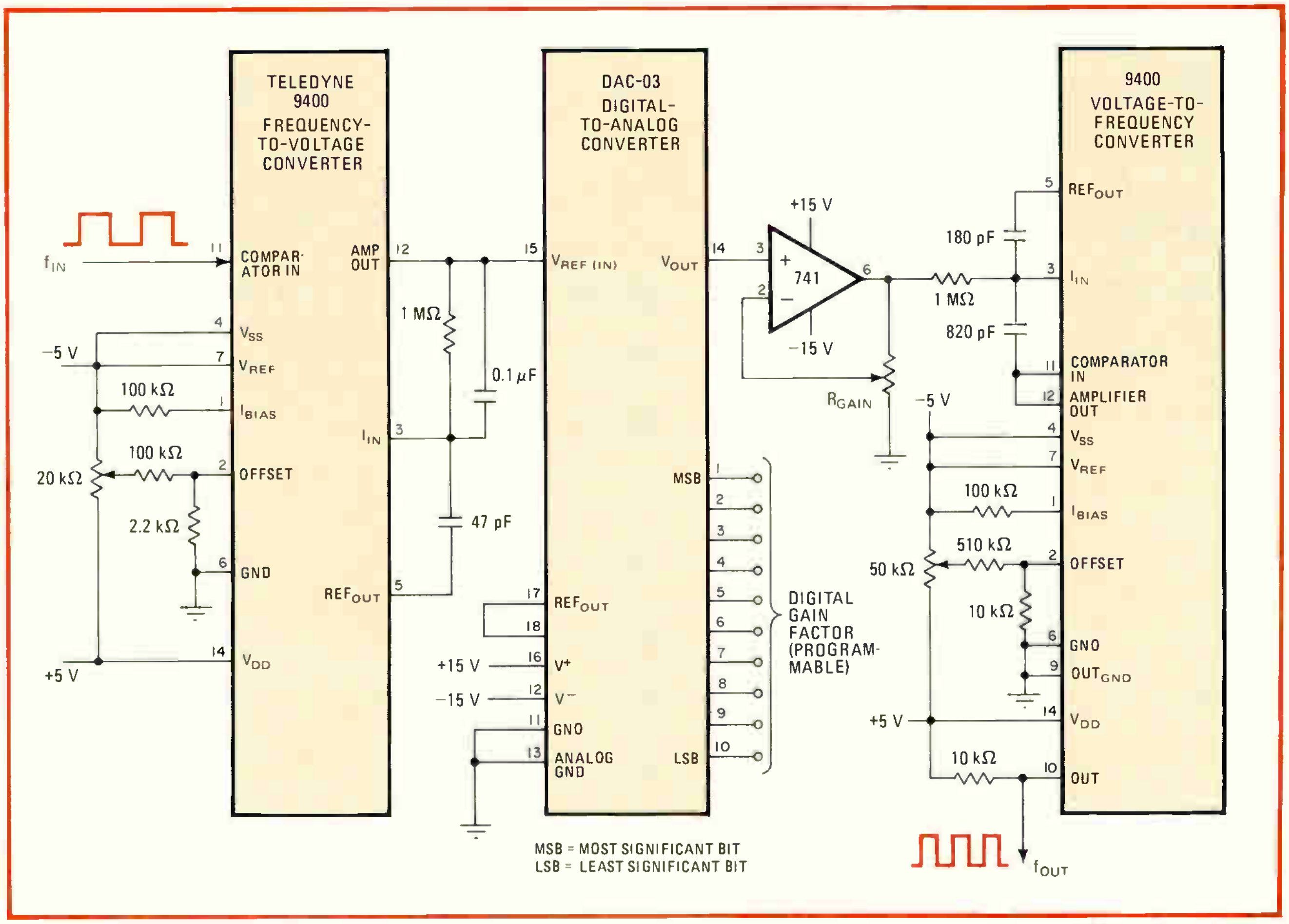
by Michael K. McBeath
Burroughs Corp., Goleta, Calif.

By using a programmable digital-to-analog converter in combination with frequency-to-voltage and voltage-to-frequency converters, this circuit can multiply an input frequency by any number. Because it needs neither combinational logic nor a high-speed counter, it is more flexible than competing designs, uses fewer parts, and is simpler to build.

As shown in the figure, the V-f converter, a Teledyne 9400, transforms the input frequency into a corresponding voltage. An inexpensive device, the converter requires only a few external components for setting its upper operating frequency as high as 100 kilohertz.

Next the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to noninteger values. The V-f device then converts the input voltage into a proportionally higher or lower frequency. □



All numbers. Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

I²L gives codec superior ac performance

Device exceeds Bell System requirements to take into account future revisions

by Ronald Ruebusch and Enjeti Murthi, *Signetics Corp., Sunnyvale, Calif.*

☐ The new integrated-circuit encoder-decoders, like other products, must compete on the basis of performance as well as price. Requirements for these devices are given by the Bell System's D3 specifications for a pulse-code-modulated channel. But the designers of the ST100 codec have provided it with much higher performance and reliability.

To this end, the ST100 employs Signetics' integrated-injection-logic process. Because this process produces a thicker epitaxial layer than Schottky I²L, it can be used to fabricate high-performance I²L transistors as well as transistors with collector-to-emitter on-voltages greater than 12 volts, to accommodate the analog circuits.

Like all bipolar devices, I²L parts are inherently quieter than metal-oxide-semiconductor ones because they are less susceptible to 1/f noise. The ST100 is no exception. Over 0° to 70°C, the idle-channel noise is 13 dBrnC0 worst case (that is, with continuous dual-channel signaling). Without signaling, the maximum idle-channel noise over the same temperature range is 10 dBrnC0, as compared with the almost 15 dBrnC0 of similar MOS devices.

As the part is intended to be incorporated into the Bell Telephone system, ac performance is crucial. Moreover, the Bell System ac specifications will almost certainly be tightened in future revisions. For that reason, too, the ST100 was designed to exceed the current D3 specs.

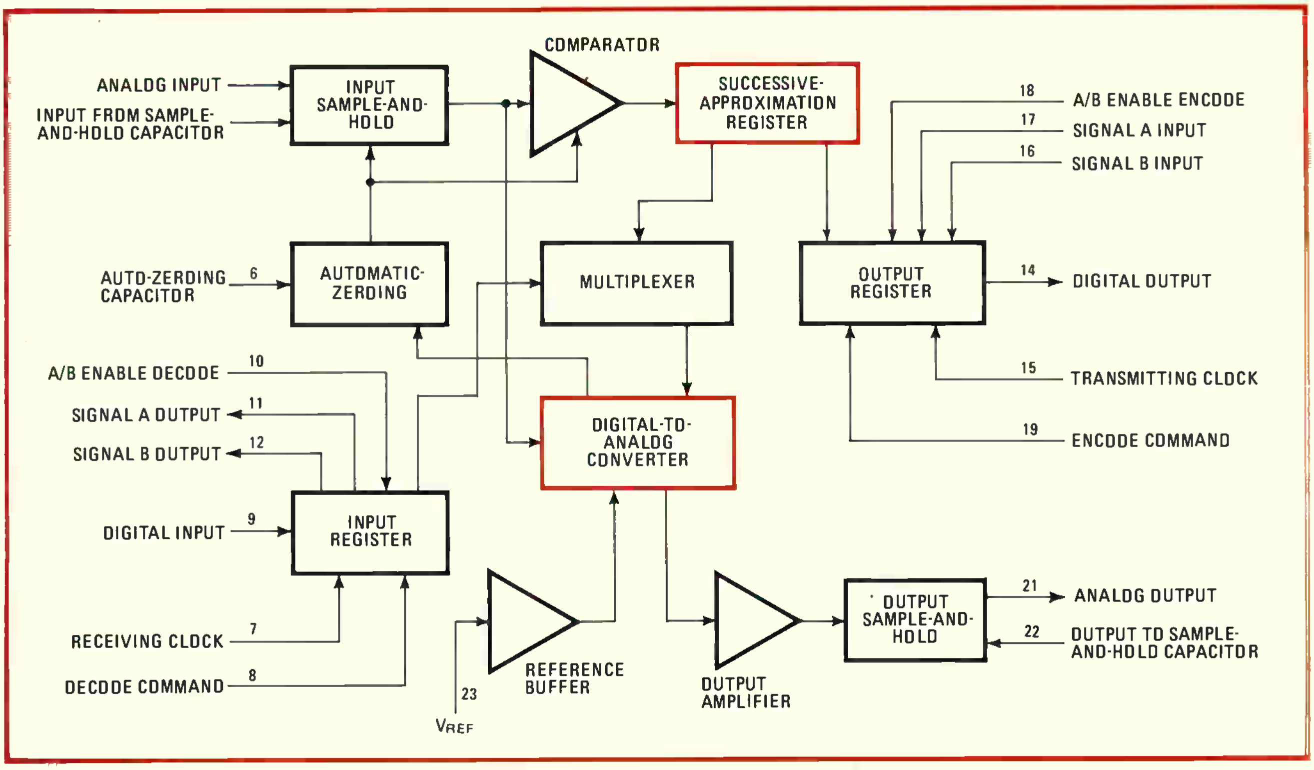
The worst-case signal-to-quantizing-noise distortion ratio over temperature during signaling is at least 5 decibels better than the D3 requirement at all signal levels. When the I²L codec is looped back or connected end to end, the worst-case frequency response during signaling, over temperature, has less than ±0.1-dB ripple over the 300-to-3,400-hertz voice band.

This margin over the D3 specifications lowers manufacturing costs because it covers any variation in tolerances that can occur with high-volume production.

System design

Besides superior electrical performance, the ST100 offers the system designer a number of other advantages. For one, I²L can drive high currents. Therefore, the analog-output port on the receiving side of the device has a low output impedance of about 10 ohms and is capable of driving a full-scale signal across a 5-kilohm load. This capability greatly reduces the problem of interfacing with the receiving filter and eliminates the need for a buffer circuit to perform impedance conversion.

In addition, the codec's bipolar nature allows all the digital interfaces on the chip to be transistor-transistor-



1. Sharing. In the ST100 codec chip, the digital-to-analog converter is time-shared between both transmission directions, with the d-a conversion taking precedence over the a-d. The chip uses a separate voltage reference to guarantee proper channel operation in the PCM mode over time and temperature, thus minimizing drift with fluctuating temperatures and also exceeding current D3 specifications.

logic-compatible. A further advantage is that I²L allows many functions to be packed on the chip. Power dissipation is typically 375 milliwatts in the active and 50 mw maximum in the standby mode.

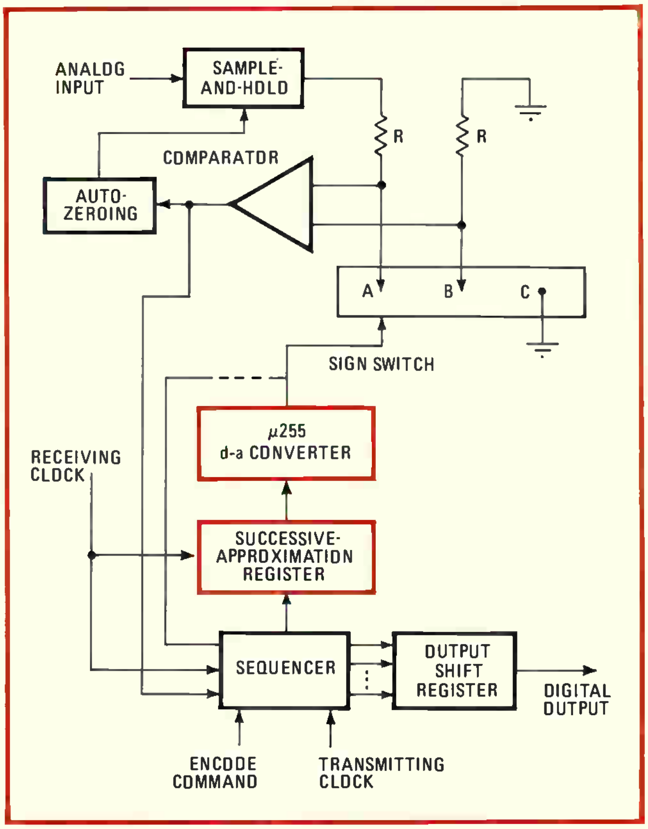
The only portion of the codec requiring the 1.544-megahertz receiving clock is the input and output shift registers. This speed is compatible with the needs of I²L circuits, since the maximum clock rates these circuits can handle are on the order of 2.1 MHz. By properly adjusting the source resistors, only those portions of the circuits operating at 1.544 MHz need to have high injection current; the remainder of the circuits may operate at significantly lower current levels.

All the chip's digital inputs and outputs have TTL-compatible buffers, which in turn drive the I²L circuitry. Buffers are also used within the I²L circuits to provide the drive necessary for high fan-out points, such as clock lines, thereby preventing delay problems from occurring when several I²L stages are cascaded.

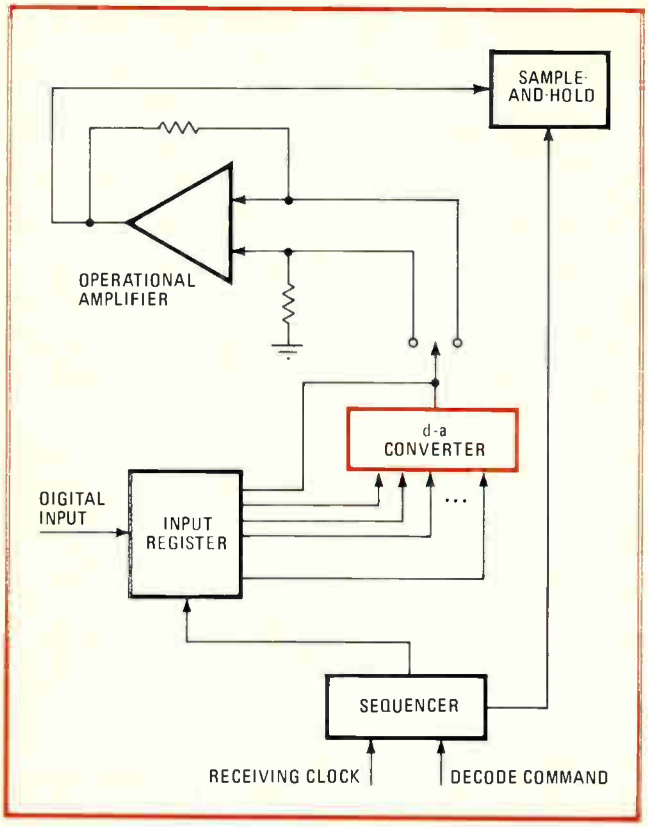
The right architecture to cut system cost

Besides performance, the codec user must be acutely aware of system cost. The architecture of the ST100 is arranged so that, at the system level, per-channel costs can be minimized without sacrificing reliability. The analog input is capable of withstanding dc offsets from a ground of ±20 millivolts without affecting signal transmission when employing the auto-zero function. This means that the analog input may be dc-coupled to the transmitting filter, thus saving the cost of a large decoupling capacitor.

The ST100 operates off ±12 V for the analog signals



2. Required presence. The internal 512-kHz master clock is derived from the 1.544-MHz receiving clock, which must always be present for sequencing to occur. The a-d conversion is done by a successive-approximation register plus a μ-law d-a converter.



3. 8+8. The decode command on the ST100 codec generates a request for digital-to-analog conversion. An interval of 8 microseconds allows the data to be shifted in and the converter to settle. Another interval of 8 microseconds is used for the conversion.

and +5 v for the logic circuitry. A power-down feature is included for those applications, like private automatic branch exchanges and central-office switches, where continuous operation is unnecessary.

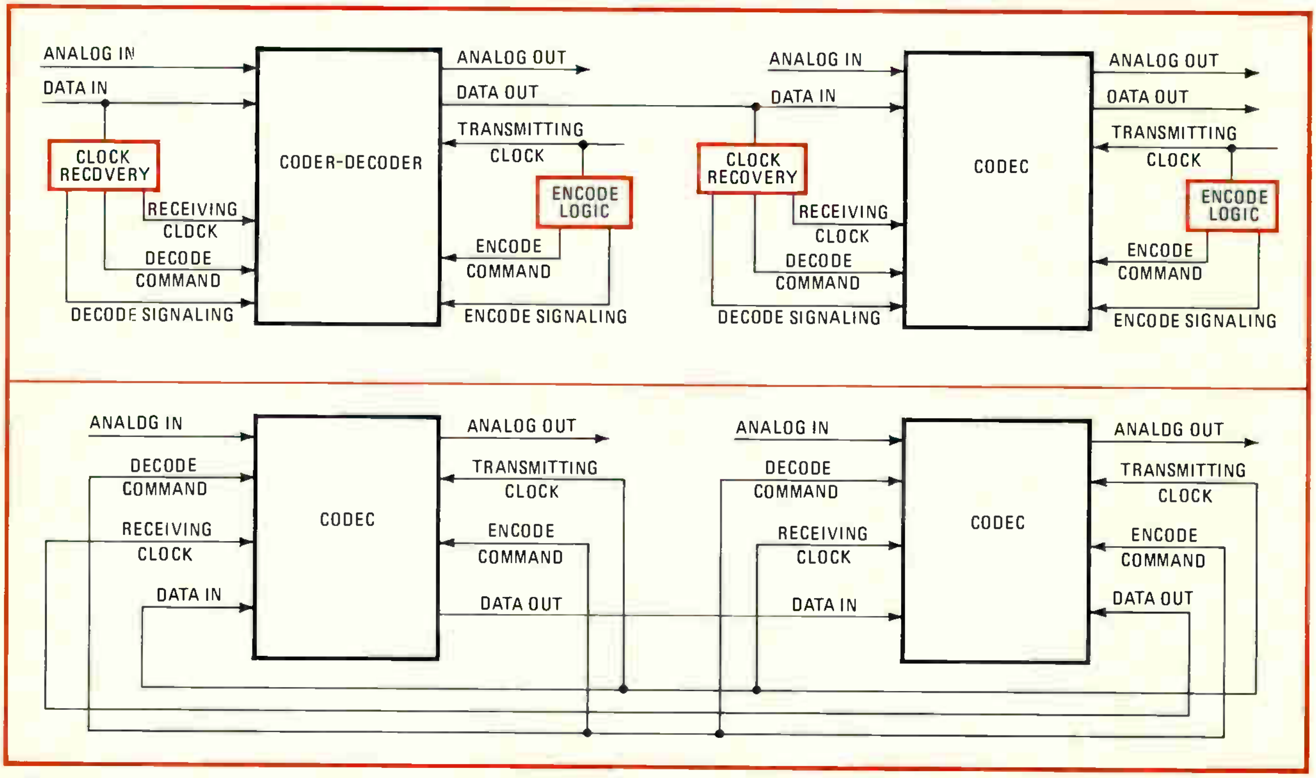
Time-slot assignment is carried out by a single TTL-compatible pulse to either the encoding or the decoding command port, thus eliminating the control circuitry needed to generate 8-bit time-slot assignment commands. The ST100 operates with data rates from 256 kilobits to 2.048 megabits per second and with sampling rates from 8 to 16 kilohertz. This flexibility gives the system designer the freedom to optimize his design when the D3 standard clocking and sampling rates do not apply.

No need for reference

Furthermore, the ST100 includes dual-channel signaling, as well as zero-code suppression for channel bank applications. Voltage reference for the digital-to-analog converter, however, is not included, and for a very good reason. The reference is keyed to the conversion process and, in the overall operation of the codec, it is imperative both that it not drift with age or temperature and that its initial value be very close to its nominal value. Otherwise, transmission quality deteriorates.

An external reference can be guaranteed to meet these requirements independently of the codec. That being the case, the question becomes one of system cost, and a savings results from improved yields for the codec when the reference is not included.

Signetics will introduce a high-performance, very low-cost reference called the ST135 along with the ST100.



4. By the clock. For asynchronous operation, external clock-recovery circuits have to be implemented to extrapolate the clocks from the data stream when decoding. In synchronous operation, the receiving and transmitting clocks are wired together. The encode and decode commands are also tied together and are controlled through the internal timing configuration.

HOW THE ST100 PERFORMS		
Parameter	Value	Test conditions
Signal-to-distortion ratio (input signal at 1 kHz)	37 dB 30 dB 27 dB	at +3 to −30 dBmO at −40 dBmO at −45 dBmO
Tracking deviation from gain for 1-kHz input signal at 0 dBmO)	±0.1 dB ±0.2 dB	from +3 to −37 dBmO from −37 to −50 dBmO
Frequency response (deviation from ideal [sin x] /x curve with respect to 1 kHz)	±0.1 dB	180 − 3,400 Hz
Idle-channel noise	13 dBrnCO	
Quiet code	2 dBrnCO	
Single-frequency distortion (for 0-dBmO input-signal level)	44 dB 32 dB	at 1 kHz from 0 to 12 kHz
Note: A and B signaling during all measurements; temperature range = 0° to 70° C; full-scale signal = ±3 V pp.		

Use of the two together will guarantee that the PCM channel will be fully operational over time and temperature. It will also afford a lower system cost, since yields can be optimized on each of the parts independently.

Figure 1 is a block diagram of the 24-pin device. It consists of analog-input and -output sample-and-hold sections, a comparator, a d-a converter, shift registers, control circuitry, and buffers. The converter is time-shared between both transmission directions, with the digital-to-analog conversion taking precedence over the analog-to-digital conversion. Thus, if an encoding sequence is in process when a decode command is received, the encoding is halted, the decoding is performed, and then the encoding is resumed.

System operations

Circuitry is included on the chip that allows A and B signaling to be inserted into the data stream. To transmit these signals, the signal A input, signal B input, and A/B enable-encode ports (pins 17, 16, and 18, respectively) must be accessed. Recovery of the signals is accomplished through the signal A output, signal B output, and A/B enable-decode terminals.

Two frames after the positive edge of the A/B enable-encode command, the value at the signal A input replaces the least significant bit in the transmitted data stream. The same thing occurs for signal B two frames after the negative edge of the command. On the receiving side, the signal A value is latched at the signal A output terminal on the first decode command after the positive edge of the A/B enable-decode command, and signal B is latched in after the negative edge. The period of the A/B enable command may be as small as 6 frames, although in transmission applications 12 frames is standard.

Figure 2 shows the part of the system employed in the encoding process. The encode command and the transmitting and receiving clocks are the only digital commands necessary for an encoding operation.

The presence of the receiving clock is always required for chip sequencing, since the codec's master clock is derived from it. The encode command begins the encoding process by causing the sequencer to issue commands for the a-d conversion. The analog input signal is sampled at a rate from 8 to 16 kHz, and each sample is converted into a folded (positive-data-train) binary non-return-to-zero 8-bit code. The first bit in the code is the sign bit and the remaining 7 bits determine the sample value companded according to the μ law.

The a-d conversion is achieved by using a successive-approximation register in conjunction with a μ-law d-a converter. The register operates at 256 kHz. This clock is divided down from the 512-kHz master clock, which in turn is derived from the 1.544-MHz receiving clock. The 256-kHz rate allows sufficient time for the comparator to settle after the input analog signal is compared with the output of the converter.

The sign of the sample data is discerned by comparing the input signal directly with ground potential, C. The full signal A is then compared with the output of the converter, which is controlled by the successive-approximation register. Ten pulses from the register are used for the successive approximation, after which the encoded data is loaded into the output shift register.

The total time for a conversion is 40 microseconds unless the process is interrupted by a decode command, in which case 56 μs is needed. The transmitting clock, together with the next encode command, generates the output shift clock, which has the job of serially shifting the data encoded during the previous frame out of the digital-output terminal.

In the decoding portion of the system (Fig. 3), only a decode command and the receiving clock are required. The receiving clock, in the presence of a decode command, generates an eight-pulse shift clock that accepts the input data. This shift clock is 90° out of phase with the receiving clock, allowing the data to be shifted in at the center of a data bit.

The decode command also generates a request to the converter that begins d-a conversion. An internal timer allows 8 μs after the request for the data to be shifted in and for the converter to settle, and another 8 μs is used for the conversion. The digital data from the input shift register is applied in parallel form to the converter. The operational amplifier changes the current outputs to voltage outputs.

The ST100 may be operated synchronously or asynchronously. Figure 4 shows examples of both modes, and the table gives the typical performance data. □

This article is the fourth in a series on the new integrated-circuit codecs. The first two articles appeared in the Sept. 14 issue, pp. 105–114; the third, in the Sept. 28 issue, pp. 141–144. A reprint of the entire series is available for $4.00. Write to Electronics Reprint Dept., P. O. Box 669, Hightstown, N. J. 08520. Copyright 1978, Electronics, a McGraw-Hill publication.

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THE MICROSYSTEM ANALYZER

Compressing test patterns to fit into LSI testers

By identifying repeated elements and manipulating them intelligently, technique shortens lengthy patterns needed to test complex devices

by Trent Cave, *Tektronix Inc., Beaverton, Ore.*

☐ As integrated circuits have evolved from small-scale into large-scale devices, the problems in testing them have increased exponentially. Not the least of these is the length of the test pattern required to check out a device thoroughly. Often it is too long to fit into the LSI tester's local memory, and then some means of compressing it becomes essential.

Most small-scale ICs have fewer than 100 functions and thus can be thoroughly tested with patterns of fewer than 100 vectors (see "Test pattern genesis"). However, testing the basic instruction set of an 8-bit microprocessor requires approximately 50,000 vectors—and this does not include testing for instruction sequence sensitivities. But the local memory of most large-scale-integration testers is typically limited to 4,096 bits per pin, and device pinouts are growing steadily.

The obvious solution to the problem is to simply expand the fast (emitter-coupled-logic) local memory, but this means expanding it for every one of the up to 64 pins at present available in testers. A quick calculation shows that such a solution is far too costly in terms not only of dollars but also of heat dissipation.

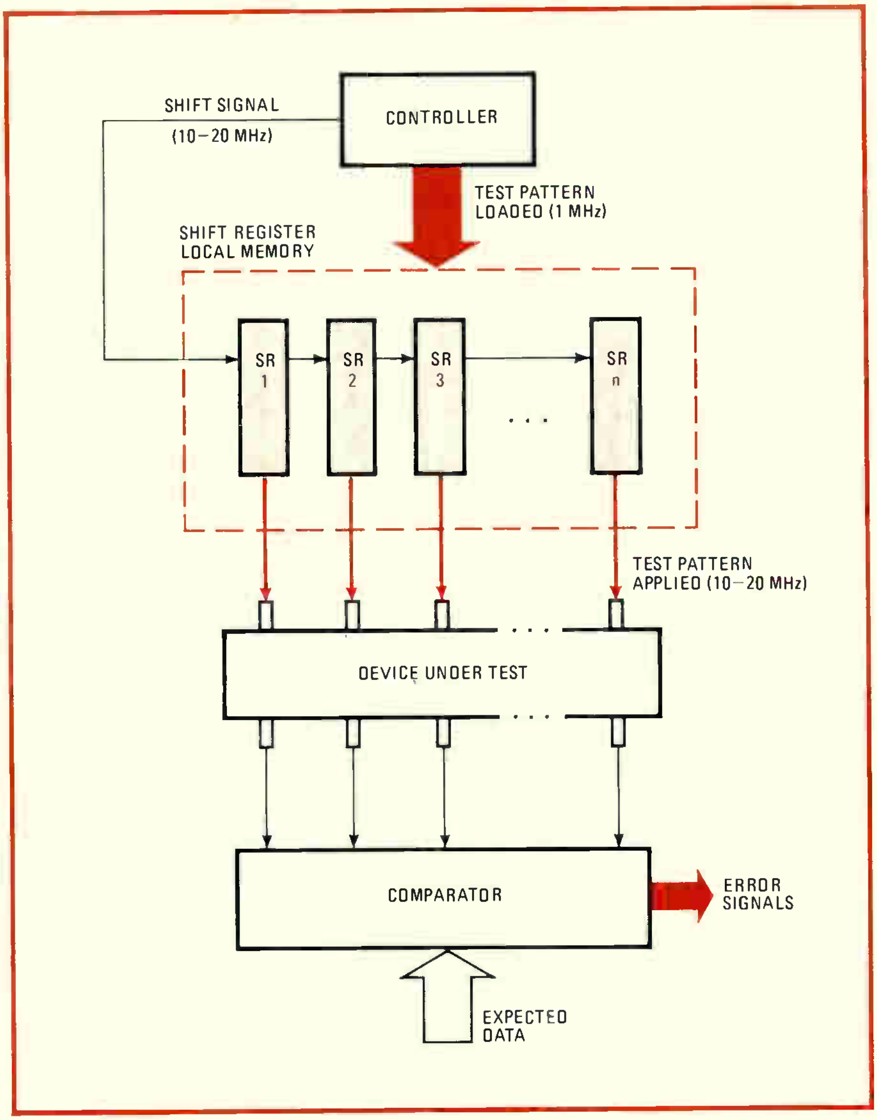
The alternative is test pattern compression, the technique for which involves both hardware and software. Hardware pattern compression is done by coupling an intelligent controller to the local memory. For example the Tektronix S-3200 series tester's PRAM (programmable random-access memory) contains registers that have been programmed by microinstructions to control looping, subroutines, and error branching. This enables the tester to handle intermixed random and algorithmic sequences of pattern at the test rate of the device. Software pattern compression works together with these hardware features by identifying subroutines and loops.

Types of test patterns

Test patterns for LSI devices typically mix random sequences of vectors, sometimes with other sequences that can be algorithmically described. It is possible to distinguish four distinct types of vector sequences: a completely random or unique vector applied to the device only once in the test pattern; a single repeated vector, in which one vector is applied to the device a certain number of times before another one is applied; a sequence of vectors in the form of a looping pattern that is applied to the device repeatedly before the next test-pattern vector takes over; a randomly repeated sequence of vectors, applied to the device more than once during execution of the test pattern.

Usually considered separately from these four types of vector are memory algorithm patterns (walking 1s, walking 0s, galloping patterns, and so forth) since these are oriented around two-dimensional geometry algorithms. Tester manufacturers use special hardware generators to simplify this type of test pattern construction with user-definable memory algorithm instructions.

The LSI tester's local memory control can apply test patterns to a device in one of three ways—by means of shift registers or random-access memories or a dual memory configuration of both shift registers and RAMs. In the first method, the controller loads the pattern into the shift register at a relatively slow rate, then shifts the



1. Shift-register storage. The test pattern is loaded into the shift register by the controller and remains stored there until a shift signal is sent, again by the controller. Each signal applies a test vector to the device under test at the device's rate, which is much faster than the loading rate.

test pattern vectors out to the device under test much faster, at the device's test rate (Fig. 1). This method has two advantages. It allows rates of up to 20 MHz since only a shift pulse is required to apply a new test pattern vector to the device. Also, error data can be logged in real time by being routed into the other end of the shift register. The primary disadvantage is the lack of subroutine capability, which limits pattern size to the size of the shift register.

In the RAM method (Fig. 2), the RAM is loaded by the computer and applies test vectors to the device by selecting the appropriate address sequence. The RAM's address sequence is controlled at the test rate by a pattern controller that is usually microprogrammed. The capabilities of a test system's pattern controller vary from system to system. The use of subroutines and looping on an address are both possible with the RAM approach. But existing pattern controllers are slower than shift registers and are not capable of accessing argument data (variables) when executing a subroutine.

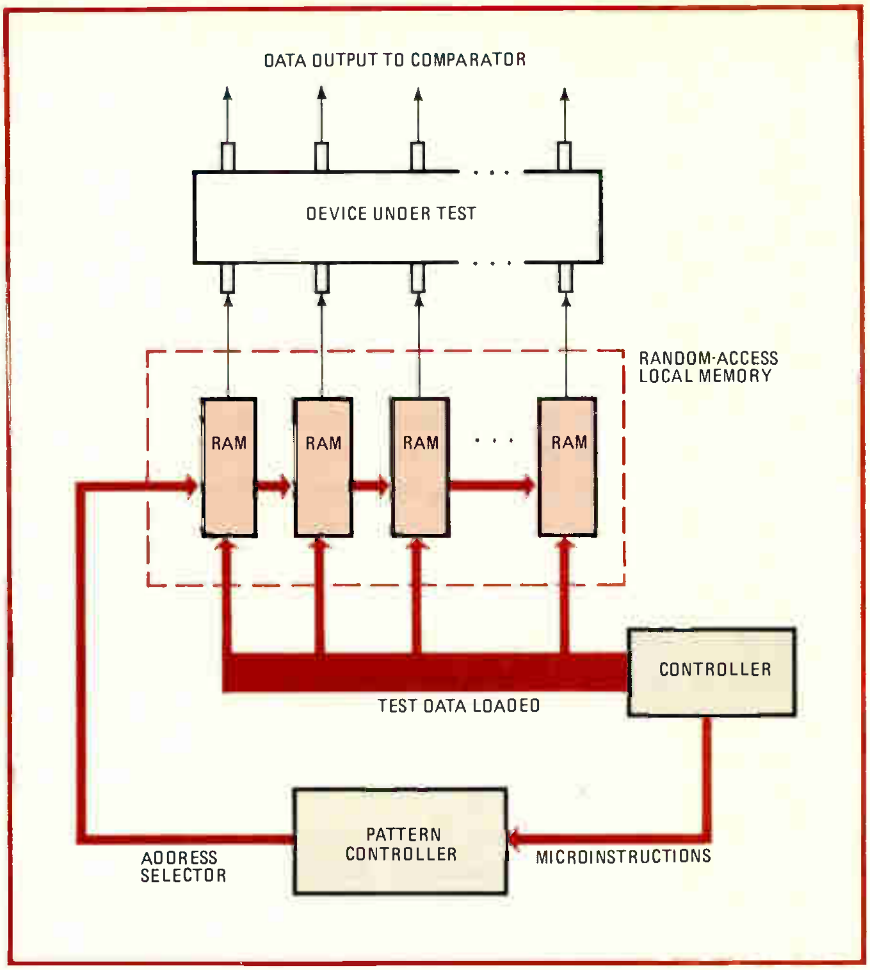
The dual-memory method (Fig. 3) involves loading both a shift-register memory and a random-access memory from the computer memory. A pattern controller is again used with the RAM to address pattern vectors. However, it is now possible both to execute a subroutine with the RAM and to have argument data applied to the device in a first-in, first-out manner by means of the shift register.

Test pattern compression

There are five steps to follow in fitting large sequential test patterns into a local memory under the control of a pattern controller:

- Run the test pattern through a data-reduction program.
- Identify all unique vectors.
- Identify all groupings of three or fewer unique vectors (not necessary in all cases).
- Identify subroutines.
- Identify subroutines that use argument data (useful only with the dual-memory approach).

The first step is software analysis of the test pattern. This is done by putting the pattern into the computer for processing through a data-reduction program that will recognize test pattern subroutines, loops, and algorithms. At this stage, repeated single vectors should be identi-



2. RAM setup. After the controller has loaded the test pattern into the RAM, a pattern controller (usually microprogrammable) selects the RAM's address sequence, thus applying the test pattern to the device. This method is more flexible but somewhat slower than the shift-register approach.

fied, for the size of the pattern storage required can be reduced by using hardware capable of single-vector looping. Such hardware is available with all three types of local memory. (A good example of a device with many single-vector loops is a universal asynchronous receiver/transmitter.) Pattern compression is achieved by loading a counter and applying pattern vectors to the single-vector looping hardware until the counter is decremented to 0.

The second step is to identify all unique vectors—the combinations of 1s and 0s that are never repeated in the test pattern. The number of these vectors will indicate how many memory locations will have to be reserved for them. If there are too many unique vectors to fit into the local memory, then subroutines or reloads will be required. If the pattern controller has subroutine overhead—that is, it needs to reserve locations in local memory to enter and exit the subroutine—then step three is necessary. Some pattern controllers can execute subroutines without overhead, however, so that local memory storage requirements are reduced and the third step can be skipped.

Otherwise, the third step is to identify all groupings of three or fewer unique vectors. Since two memory locations are required to store a subroutine and another one to call it, no savings result from converting these groups of three into subroutines. Again, if the number of memory locations for these groups is greater than local memory size, the test pattern will not directly fit into the local memory. Reloads will therefore be required, but it is possible to reduce their number through further compression steps.

The fourth step is to begin identifying subroutines. The larger the subroutine and the more identical subroutines there are, the greater the probability that the test pattern will prove compressible into the local storage. All the subroutine location sizes and the calls to the subroutines should be added to the grouping and unique vector storage requirements, and if the sum is greater than local memory size, then the test pattern will not directly fit into it and reloads are still indicated.

How dual memory helps

These steps represent the limits of most RAM-only LSI test systems. However, if the LSI tester has dual-memory architecture, a fifth step of compression is possible for those devices which perform repeatable functions but with different sets of data. An example is a microprocessor's fetch subroutine, which of necessity must be executed for all instructions but also fetches different data most of the time.

In such cases, subroutines can be developed to run from RAM storage using arguments supplied from shift-register memory. This hardware pattern-compression method can greatly reduce the size of pattern storage required. Software can be used to identify the pattern

Test pattern genesis

A test pattern may be defined as the series of machine-language statements, arranged sequentially in rows, that is needed to exercise all desired functions of a device under test. A test vector (see Fig. 4) is either a row of this test pattern or an algorithmically generated pattern and exercises a particular function of the device under test.

The large test patterns needed today are increasingly being generated by computers. In fact, some manufacturers of large-scale integrated circuits use large computers to model them and (they hope) to generate worst-case, or race, patterns for them. These patterns usually give the device user a good first-try approximation at a test pattern, with failures generating the feedback he needs to improve it.

Manufacturers of device testers, on the other hand, may not have the internal layout of the device to work from, so they offer software from which the user can build test patterns by simulating the device functions. For example, tester manufacturers have had software for generating test patterns for the 8080 microprocessor available for several years. The user merely types the 8080 mnemonics in the sequence desired for testing the part, and the test pattern is then automatically generated and stored on a disk file [*Electronics*, Feb. 17, 1977, p. 109].

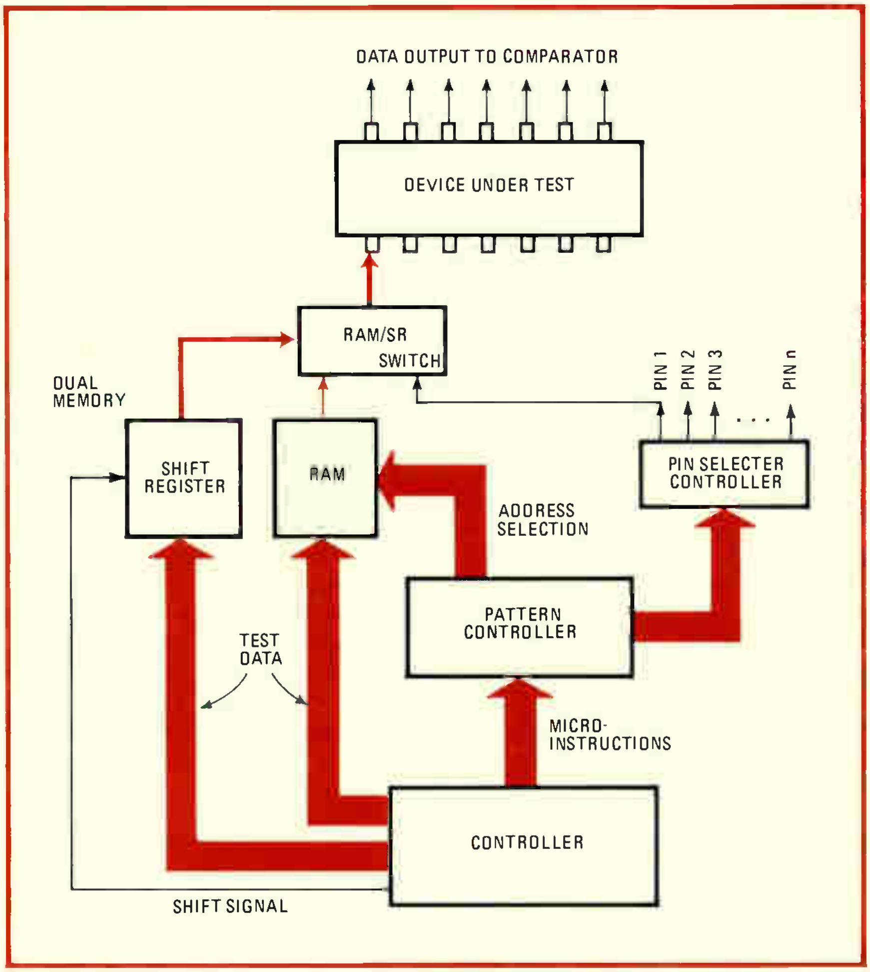
The advantage of this approach is that it provides a test pattern that will be equally valid for all devices of a given numbered type, such as the 8080, regardless of the vendor. The combination of device functions can be used to build a test pattern capable of exercising any of these devices adequately.

There are two commonly used methods of applying pattern vectors to the device under test. In the first, a computer applies the pattern vectors as fast as it can to the device. But most semiconductor devices now require faster test cycle rates than the 1 megahertz typical of a computer-rate tester, although many home-brew testers being built still use this technique.

The other approach is faster and is preferred by most tester manufacturers. In it the test patterns are loaded into local memory in the LSI tester and the vectors are applied to the device at the test rate desired—around 10 to 20 MHz. Test patterns can be run sequentially on most testers. But reloading is required when the test pattern exceeds the size of local memory.

The drawbacks to this technique revolve about this reloading of local memory. For instance, if it takes longer than the device refresh time, testing of dynamic devices becomes a problem.

Also, reloading decreases throughput since disk or core access time will slow down test times. Finally, the testing of a device at its rated speed cannot continue during a local memory reload.



3. Dual memory. When the pattern controller can load both RAM and shift register with test data, it becomes possible to test subroutines using variable data. The necessary argument data from the shift register is called up along with the RAM's addressing sequence.

EXAMPLE OF PATTERN COMPRESSION

Uncompressed test patterns

15 locations	1 0 1 1 0 0	
	1 0 1 1 0 0	Single vector loop
	1 0 1 1 0 0	
	0 1 1 1 0 0	Unique vector
	0 0 0 0 0 1	
	0 0 0 0 1 0	Subroutine A
	0 0 0 1 0 0	
	1 1 1 1 0 0	Unique vector
	0 0 0 0 0 1	
	0 0 0 0 1 0	Subroutine A
	0 0 0 1 0 0	
	1 0 1 1 0 0	Unique vector
	0 0 1 0 0 0	Subroutine similar to A (use of dual memory allows it to be handled together with A)
	0 0 0 0 1 0	
	0 0 0 1 0 0	

(a)

Compressed test pattern (dual memory method)

	RAM	Pattern controller	Second memory (shift register)	
7 locations	1 0 1 1 0 0	Test, Loop 3		
	0 1 1 1 0 0	Test, Call Sub		
	1 1 1 1 0 0	Test, Call Sub		
	1 0 1 1 0 0	Test, Call Sub		
		Halt		
	0 0 X 0 0 X	Sub: Use secondary memory	Z Z 1 Z Z 0	3rd time
	0 0 0 0 1 0	Test	Z Z 0 Z Z 1	2nd time
	0 0 0 1 0 0	Test, Return	Z Z 0 Z Z 1	1st time
	Contents of X locations supplied from secondary memory		Contents of Z locations supplied from RAM	

(b)

4. Compression. Test pattern is shown before compression (a) and after (b). Step-by-step analysis eliminates repeated patterns, reducing memory location requirements from 15 to 7. Color indicates similar vectors and arguments that are manipulable in dual memory.

vector section (arguments) that must be supplied by the alternate memory source. Knowledge of the device can also be very helpful.

The best way to understand test pattern compression is to do it for the test pattern shown in Fig. 4.

Step 1. The repeated single vector is 101100, and the number of repeats is 3. This reduced to one local memory location with a loop instruction.

Step 2. There are altogether eight different vectors in the uncompressed test pattern on Fig. 4 requiring RAM storage. If local memory size were 7, then a RAM hardware method of pattern compression would not work, even with a pattern controller that did not have any subroutine overhead. The number of distinctly different vectors represents the theoretical limit in a purely RAM-type system.

Step 3. This can be skipped because the pattern controller hardware has no subroutine overhead. If it did have overhead, no pattern compression would be possible for the example given because all the subroutines occupy three locations anyway.

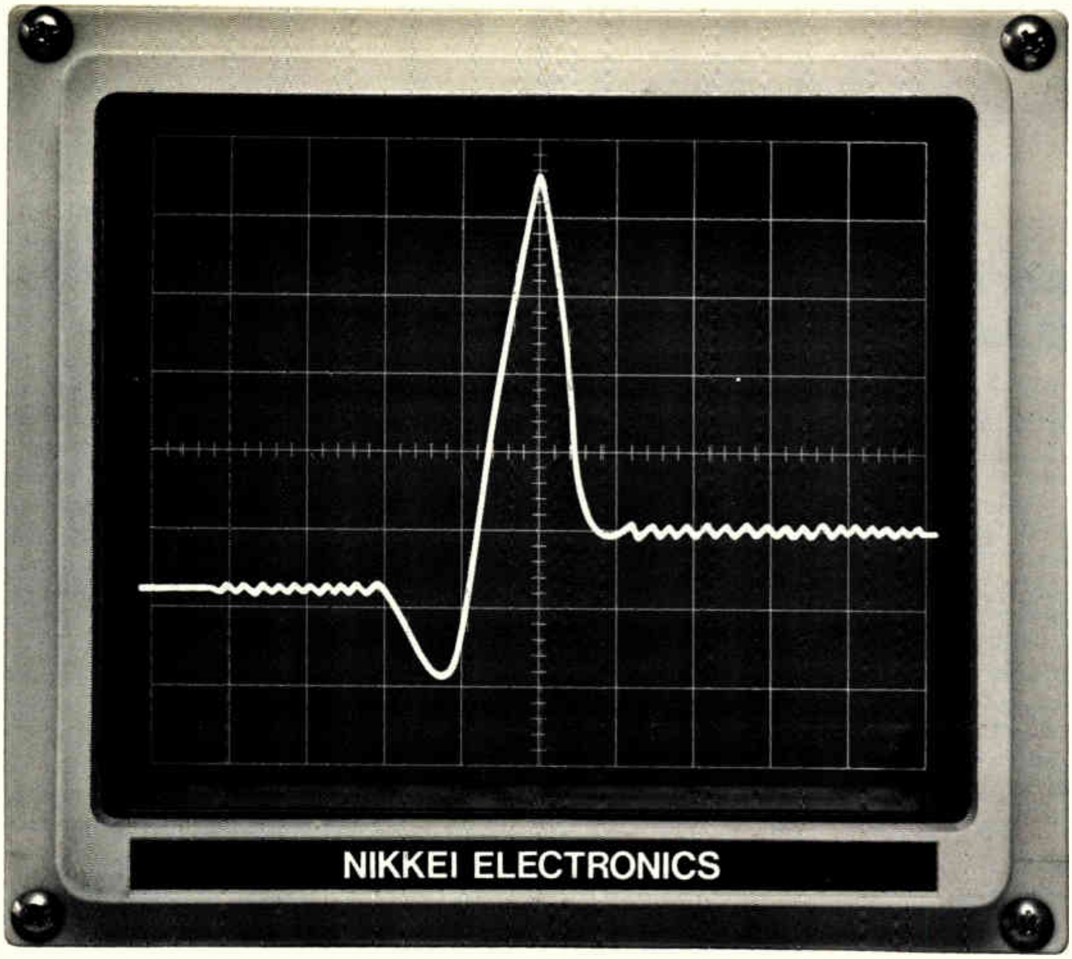
Step 4. There are two identical subroutines and a third, similar one that can be handled as straight-line code without dual memory. A subroutine call, to the location Sub + 1, can be used to cut down on storage in a RAM-only system. This permits the use of only eight locations, the theoretical compression limit determined in the second step, and is programmed as:

1) Test, loop 3
2) Test, Call Sub
3) Test, Call Sub
4) Test, Call Sub + 1 Halt
5) Sub: Test
6) Test
7) Sub + 1
8) Test, Return

Step 5. A dual-memory configuration makes it useful to identify all subroutines, even those only with similarities, and to identify the pins (columns of the test pattern) that must be modified. In this case the third column and the last column must change, as indicated by the X in the RAM layout of Fig. 4. In the simplified example given, there is only a savings of one local memory location over the RAM-only method covered in step 4. In reality, however, such an operation might be repeated very often, so that the overall reduction in memory requirements could be quite large. Large test patterns typically show a 5-to-1 reduction in pattern storage requirements when a dual-memory architecture is used instead of a RAM-only architecture. □

Closing the loop

The author of this article is willing to answer any questions readers may have. He can be reached between 8 a.m. and 4:30 p.m. Pacific Standard Time from Oct. 16 to 20 at (503) 645-6464, ext. 1203.



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Processor's PROM decoder extends addressing capabilities

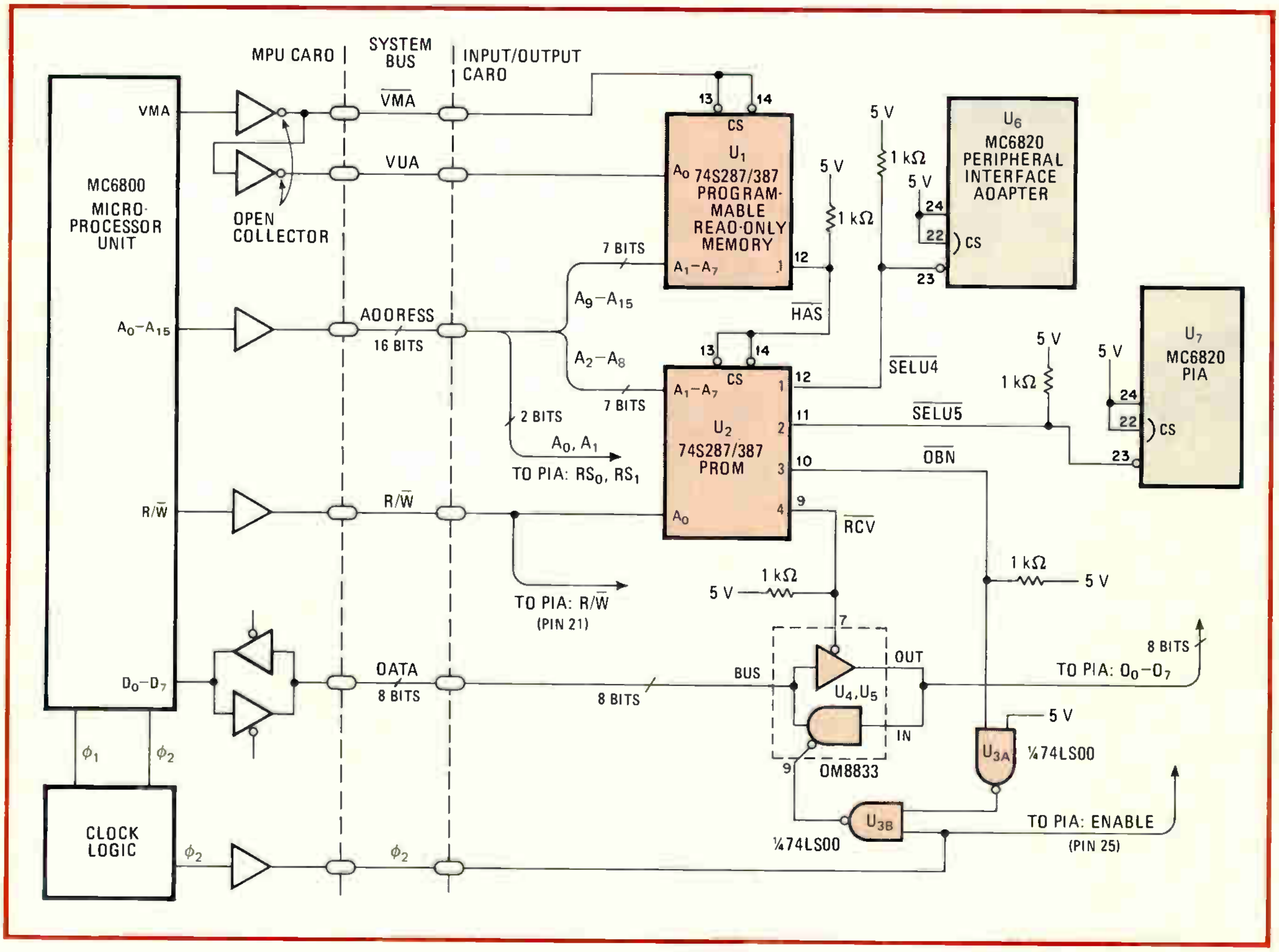
by Robert S. Rodgers
Lehigh University, Chemistry Department, Bethlehem, Pa.

The idea of using a programmable read-only memory to replace logic that activates circuits in a microprocessor-based system ["PROM decoder replaces chip-enabling logic," Sept. 2, 1976, p. 100] can by extension be applied to controlling bus interfacing as well. In addition, system addressing capabilities can be increased by using the PROM to coordinate the operation of two peripheral interface adapters employed in a typical M6800 system.

Figure 1 shows how two 256-by-4-bit PROMs of the fusible-link variety (U_1 and U_2, the 74S287 or 74S387) can be used to meet both objectives. These devices, combined with one half of a 74LS00 quad NAND gate, U_3, and two DM8833 quad three-state transceivers, U_4, and U_5, make up the complete address-decoding and bus-interface logic. (Only one transceiver is shown.)

The signals on the system bus are a buffered (transistor-transistor-logic) version of the signals emanating from the MC6800's address, data, and control lines. However, one wiring change in the standard bus is made to facilitate direct-memory-access devices and to enhance the flexibility with which the PIAs may be addressed: the valid memory access line (VMA) is active low on the system bus. The signal VUA is also developed from $\overline{\text{VMA}}$ and is a delayed version of the original VMA signal. This modification means that a DMA signal, such as a control pulse emanating from the microprocessor's front panel, need only drag the VMA line low to show that it is placing a valid address on the bus, while VUA makes possible shadowing of memory locations.

For example, front-panel control can be used to bring VUA low after the system is reset, thereby disabling any



Flexible. Using PROM decoder for accessing peripheral interface adapters provides for a myriad of addressing schemes. All control lines of 6800 are buffered on a system bus. U_1 decodes address lines VUA, $\overline{\text{VMA}}$, and seven highest address bits, A_9–A_{15}; U_2 decodes R/$\overline{\text{W}}$ and A_2–A_8. U_2 selects the PIAs and controls the data-bus transceivers, U_4 and U_5, as well.

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Address										
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–	0	0	X	X	X	X	X	X	X	1
$68 y z	0	1	0	1	1	0	1	0	0	0
All others	0	1	†	†	†	†	†	†	†	1

Signal	$\overline{HAS}$	$R/\overline{W}$	A_8	A_7	A_6	A_5	A_4	A_3	A_2	$\overline{SELU4}$	$\overline{SELU5}$	$\overline{DBN}$	RCV
U_2 pin	13, 14	1	2	3	4	5	6	7	15	12	11	10	9
Address													
–	1	X	X	X	X	X	X	X	X	1*	1*	1*	1*
$6810	0	1	0	0	0	0	1	0	0	0	1	0	1
$6810	0	0	0	0	0	0	1	0	0	0	1	1	0
$6820	0	1	0	0	0	1	0	0	0	1	0	0	1
$6820	0	0	0	0	0	1	0	0	0	1	0	1	0
$6830	0	0	0	0	0	1	1	0	0	0	0	1	0
All others	0	X	†	†	†	†	†	†	†	1	1	1	1

$ = indicates hexadecimal number
X = "don't care" state

*PROM is not enabled, but outputs are pulled up
† bits as required to access specific address

memory location enabled by VUA. The front-panel switches may then be used in place of the system's reset vector. In addition, any random-access-memory subsystem enabled by VUA may be write-protected by logic that drags that line low during a write cycle referencing that particular RAM. Individual memory locations or entire blocks of data may be guarded in this way.

The address decoding scheme used here allows the designer the option of enabling the PIAS with either $\overline{VMA}$ or VUA, depending on how the PROMS are programmed. $\overline{VMA}$ is used to enable U_1, with VUA and A_9–A_{15} selecting the location within the PROM. One output of U_1 is used to generate a high-address select ($\overline{HAS}$) command that is active low. The 74S287 was chosen for the PROM because unprogrammed locations will be at logic 1, equivalent to having placed $\overline{VMA}$ at logic 1 to deselect the chip. Only one link of the PROM need be fused to decode VMA, VUA, and A_9–A_{15}.

The $\overline{HAS}$ signal is used to enable a second PROM, U_2, which decodes A_2–A_8 and $R/\overline{W}$ (the system read/write line). All four of this PROM's outputs are used. Two outputs enable the PIAS (U_6, U_7) directly through the use of an active-low chip-select on each adapter. A third output directly controls the receiver-enables of the DM8833's, used as the data-bus transceivers. The remaining output is gated with phase 2 of the buffered clock to enable the 8833's transmitter during a read cycle. Because the chip-enable lines of the PROMS are used in decoding pull-up resistors are needed.

A fringe benefit of this address decoding scheme is highly flexible addressing. The PIA board containing U_6 and U_7 may be assigned several addresses simply by fusing more links in the appropriate PROM; that is, each address may be used to refer to a different enabling scheme. For example, the board may be given two addresses, say, $10yz (where use of the $ sign represents a hexadecimal number), in which case it will respond only when VMA = 0 and VUA = 1 and $20yz, in which case it will respond when VMA = 0 (the two links corresponding to VUA = 0 and VUA = 1 are both fused). Consequently, the board is protected against overwriting (shadowed) at address $10yz, but not at address $20yz.

One feature of the MC6820 peripheral interface adapter is that the CA_2 or CB_2 handshake lines (not shown) may be programmed to emit a low pulse for one cycle upon the receipt of a read or write command from the appropriate data register. In some applications, it may be desirable to program simultaneous pulses on two or more CA_2 or CB_2 lines, and this PROM addressing scheme does that without external hardware.

By properly fusing U_2's links, both PIAS may be enabled by a reference to a particular address, say, $6830, keeping in mind that this can only be done during a write cycle. The link at each select output of the PIAS corresponding to that address and R/W status must be fused. Each adapter may be given a second address to which it, and it alone, responds—say, $6810 for one and $6820 for the other. A write into address $6810 will produce a CA_2 pulse on PIA 1, a write into $6820 will produce a CA_2 pulse on PIA 2, and a write into $6830 will make a pulse emanate from both adapters simultaneously. The table details the PROM programming. Also,

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a similar scheme may be used to read from several PIAS simultaneously, although care must be taken not to enable the 8833's transmitters during a multiple read instruction to prevent conflicts on the data bus. Otherwise, the system may read meaningless data during the read operation and the internal interrupt flag bits (CR_6 and CR_7, not shown) of the adapters may be cleared simultaneously with a single load instruction (LDAA). □

Linear light polarizers sense angular position

by Yishay Netzer
Haifa, Israel

Two sets of light polarizers can be used to build an angular-position sensor that will find many uses in servo-setting applications and flexure measurements. The circuit suffers from none of the major drawbacks inherent in conventional sensors, notably the friction, bulkiness, and cost of electromechanical transducers.

The design of the circuit shown in the figure is based upon the principle that the amount of light passing through two linear light polarizers is a function of the angle separating their polarizing axes and can be detected by a photodiode. The index of transmission is equal to $(K_1 + K_2 \cos^2 \theta)$, where θ is the angle between a stationary polarizer and one affixed to the rotating shaft whose position is to be determined; K_1 is the transmission coefficient of light through the stationary polaroid when $\theta = 90°$; and K_2 is the transmission coefficient through the stationary polarizer when $\theta = 0°$.

To eliminate the shortcomings of a circuit operating with one photodiode and a single pair of rotating-stationary polarizers (no reference zero position and poor stability), a second sensor and set of polarizers are used, as shown, along with differential and summing amplifiers. All components of the angular-position sensor act to normalize the output voltage for a given shaft angle and to generate bipolar output voltages, which do not vary with most operating parameters.

The second photodiode is covered with a polarizer whose axis is at right angles to that placed over the first sensor. These and a standard visible-light source mounted symmetrically above them comprise the static portion of the circuit. The defined zero shaft position is the polarizing axis of the rotating polaroid, which should be placed 45° to that of the stationary polarizers.

If the photocurrent at the sensors is I_1 and I_2, respectively, their difference, which is applied to A_1, is:

$$I_1 - I_2 \propto K_1 + K_2\cos^2(45° + \theta) = K_2 \sin 2\theta \qquad (1)$$

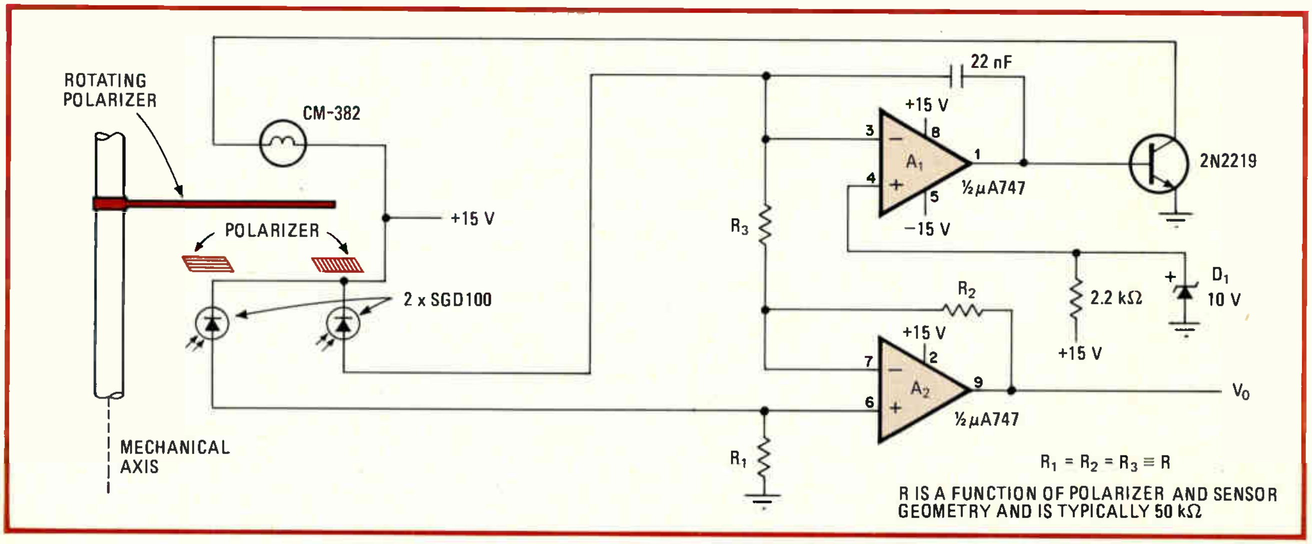
This current is then converted into a corresponding output voltage by A_1. The signal is symmetrical about zero and linear to within ±1% in the ±15° range, and to ±5% in the ±30° range. The linear range can be extended to ±45° by a nonlinear sine-wave converter or power-series linearizing circuit.

In any case, the output would still be sensitive to temperature-induced variations, were it not for the compensation provided in this circuit. To reduce these variations and to make the circuit immune to power instability, the two signals I_1 and I_2 are summed by A_2, and this sum is held constant by an internal feedback loop that includes transistor Q_1, the light source, and a 10-V reference provided by D_1. The sum current is then given by:

$$I_1 + I_2 \propto K_1 + K_2\cos^2(45° + \theta) + K_1 + K_2 + \cos^2(45° - \theta) = 2(K_1 + K_2) \qquad (2)$$

and thus it is independent of angular position.

The circuit is slightly sensitive to stray light. This problem can be avoided by substituting an infrared-light-emitting diode suitably modulated for the normal



On the beam. Amount of light reaching photodiode is a function of angle between polarizing axis of stationary and rotating polarizers. Shaft, affixed to rotating member, thereby modulates light beam, transmits its angular position to detector.

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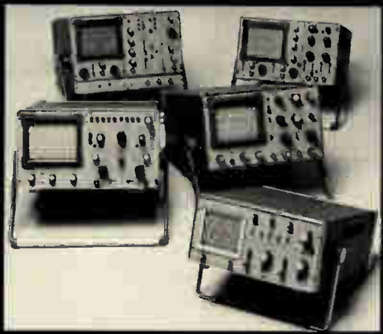

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light source. The difference current $I_1 - I_2$ can then be detected by synchronous means. At these wavelengths, though, a standard polarizer will not be effective, and a type HR polarizer should be used.

Note that with visible light, K_1 in Eq.1 is almost zero and K_2 is about 0.4. If the light source is an incandescent lamp, a large portion of the energy detected will also be in the infrared region where the optical material is ineffective. Therefore, if standard polarizers are to be used, an appropriate filter would be employed to pass just the visible spectrum. The filter would serve to eliminate the K_1 term from Eq. 2, while holding factor K_2 almost constant. ☐

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

11-byte program generates 2 billion pseudorandom bits

by Tomasz R. Tański
Warsaw, Poland

Making efficient use of the 8080A microprocessor for digital testing and simulation applications, this 11-byte program generates pseudorandom binary numbers anything from 31 to 2,147,483,687 bits long. Unlike many programs, this one does not use instructions to access the locations and contents of external random-access memories for each number to be generated, so that the fetch/store overhead is eliminated and execution time is consequently minimized.

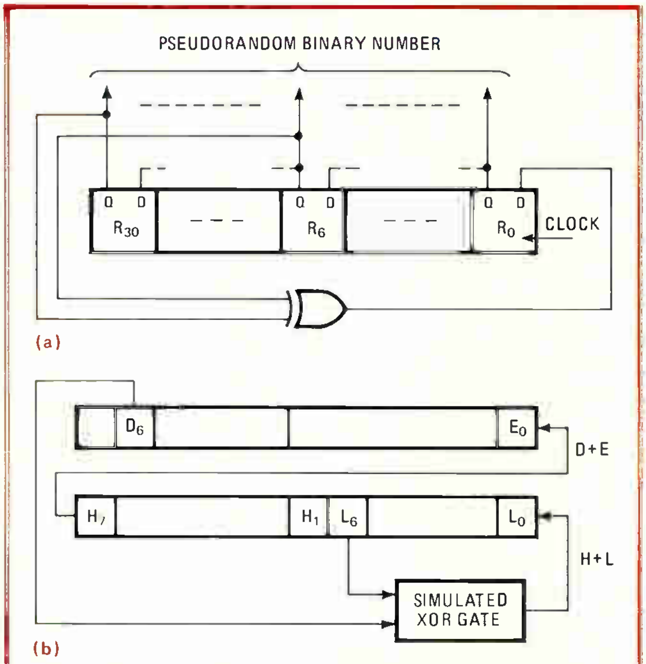
The hardware circuit simulated by the routine is a 31-stage shift register and an exclusive-OR gate, with the register's serial input derived from stages 6 and 30 (a). These two stages were found to provide the most efficient operation, in terms of saving program steps.

In software (b), the shift register is simulated by four of the 8080A's 8-bit registers: D, E, H, and L. One other register, A, is used for temporary storage.

In program operation (c), all registers are shifted before the value of a particular feedback bit is calculated. First, the contents of register L, the least significant bits in the hardware register, are shifted left and added to the contents of H. The higher bytes in E and D are then rotated one by one, with the aid of the accumulator and carry flag.

Now the feedback value can be computed by the simulated XOR gate, and the L_0 bit, which had been cleared earlier by the DAD H instruction, can be updated accordingly. Note the bits to be combined by the XOR gate are the most significant bits in registers A and L, so that no rotation to align the bits is needed.

On the return of the program to its starting point, a new 31-bit binary number is available for the calling program in registers D, E, H, and L. In most cases, the initializer, or calling program, will have to make provision somewhere in memory for saving the last number generated, because it must be reloaded into the registers each time a new call is made, to ensure that a completely random number sequence is generated. Storing the last number generated also ensures that D, E, H, and L will not be loaded by all zeros each time the system is initialized during a power up, but by the number previously stored. ☐



8080A PSEUDORANDOM-NUMBERS PROGRAM

```
PRBN:  DAD H    ;SHIFT LOWER PART, CLEAR L0
       MOV A,E  ;SHIFT HIGHER BYTES SEQUENTIALLY
       RAL      ;     8080A:  USE AC, CY
       MOV E,A  ;     Z80  :  RL E, RL D
       MOV A,D
       RAL
       MOV D,A
       ZRA L    ;CALCULATE FEEDBACK
       RP
       INX H    ;UPDATE L0 IF NEEDED
       RET
```

(c)

Processed digits. Hardware realization of pseudorandom-binary-number generator (a) may be simulated with four of 8080A's 8-bit registers (b) and only 11 software bytes—10 if the Z80 processor is used (c). Program does not call upon external memories for number generation, thus eliminating fetch/store overhead and minimizing execution times.

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Engineer's newsletter

Inverted chip-carrier keeps programmable chip programmable

Suppose you could program a custom digital chip 7,000 different ways simply by changing its external wiring, but that you also had to mount it on a thick-film hybrid with other chips. What would be the most cost-effective way of programming it? Engineers at Circuit Technology Corp. in Farmingdale, N. Y., faced this problem in a thick-film hybrid design for a secure communications link and came up with a novel use of a standard 3M leadless ceramic chip-carrier.

They simply placed the chip in the cavity of the carrier, die- and wire-bonded it in place, and then attached the carrier **with its gold input/output pads facing up, rather than down against the substrate,** as would be normal. That made it possible to run different wire-bonded connections from the substrate's conductors to the carrier's pads for each of the IC's program variations. Thus only one substrate pattern is needed, instead of a different one for each program variation.

Watch those clock specs on microprocessors

Douglas Schmidt of Computer Automation Inc., Irvine, Calif., has noted some specsmanship in microprocessor manufacturers' claims of superlative performance due to enhanced clock speeds.

He points out that the Z80, for example, boasts of a 250-ns clock cycle. But close examination reveals that **the Z80 memory cycle actually lasts 750 ns at that clock rate.** Also, fetching the op code actually takes 1 ms, since it must include a "hidden" refresh cycle.

The Intel 4-MHz 8085 is billed as the "world's fastest 8-bit microcomputer." This translates into a memory cycle time of 600 ns. He notes, however, that the Rockwell 6502A and the Motorola 6800 microprocessors execute memory cycles in 500 ns with a 2-MHz clock.

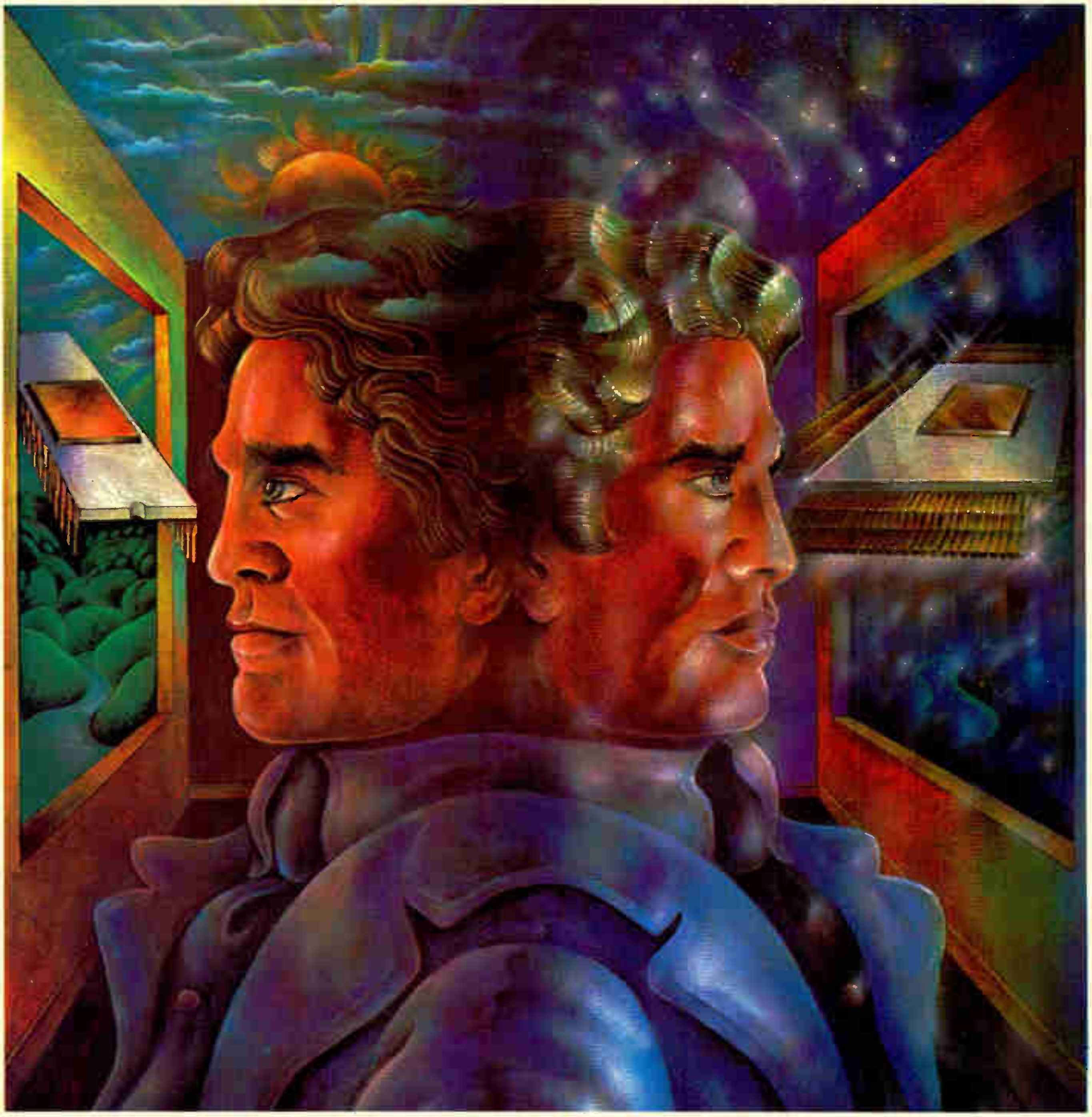
Silicone cushions flat cable against breaks

Silicone rubber is normally thought of as either a conformal coating or encapsulant. But a flexible cushion of clear silicone rubber has stopped extremely fine wires from fracturing in computer transmission cables woven by Woven Electronics, a division of Southern Weaving Co., Mauldin, S. C. The flat cable is surrounded first by silicone, then by epoxy within the connector. **With the silicone buffer (Dow Corning 3140 RTV), the cable can be flexed at least 270° in each direction** at the point where it enters the shell of its connector assembly. Without the buffer, the sharp edge of the connector assembly's rigid epoxy encapsulant cuts through the magnetic wires, some of which are only 5 mils in diameter.

Where to go to learn about solar cells fast

Do you need an intensive short course in solar cells? Then consider attending "Solar Cells—From Basics to Advanced Systems," to be presented on Nov. 17 in San Francisco under the joint sponsorship of Continuing Education in Engineering and the College of Engineering, University of California, Berkeley. The course will cover the fundamentals of solar cells, the state of the art, and upcoming developments, **including new approaches to increasing efficiency and lowering cost.**

Sessions will be held in the Hilton Inn at the San Francisco International Airport. The registration fee is $150. For further details, write to Continuing Education in Engineering, University of California Extension, 2223 Fulton St., Berkeley, Calif. 94720. **Jerry Lyman**



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Multiple pass testing? Chances are, you're occasionally forced to do some multiple pass testing of complex multi-pin devices. Well, the Sentry VIII can eliminate that extra pass. It has the ability to change any pin or timing assignment (input, output or format) on the fly. That can represent a tremendous improvement in throughput and can save as much as 50% of your testing time.

Still testing devices one at a time? By multiplexing the 120 fully programmable I/O pins on the Sentry VIII you can test two, even three, LSI devices simultaneously. Another 50% to 60% savings in test time.

And you can save even more. To provide lower operating costs, the Sentry VIII features multi-task (foreground/background) software for simultaneous compiling, editing and testing; a CPU that provides 50 to 200% faster throughput; a sequence processor to handle high complexity devices; and a pattern processor to tackle the largest memories.

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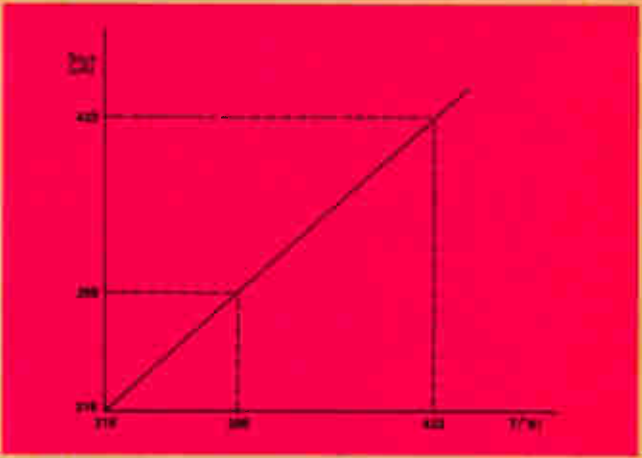

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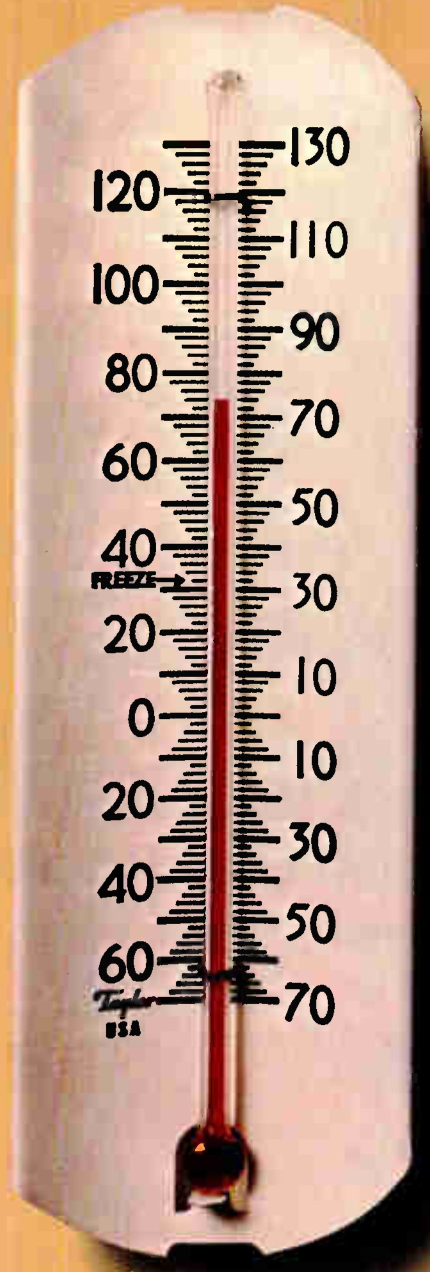

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Microcomputer made for Pascal

Stack-oriented 16-bit computer interprets P-code in hardware; four-chip set addresses 64 kilowords, will also be available in packaged form

by John G. Posa, Microsystems and Software Editor

In an unprecedented and welcome step, Western Digital Corp. has designed a microcomputer around a language, instead of the other way around. The language is Pascal.

One way to compile this high-level programming language is to do it in two steps. First, Pascal source code is compiled into its intermediate code, P-code. Then the P-code is executed interpretively on the host machine. This interpreter is actually an idealized stack machine and can be implemented in software. That is, with the proper routines, a processor can be turned into a pseudomachine whose native language is the P-code.

Western's four-chip set is a hardware realization of the pseudo P-machine, with the advantages of faster execution of Pascal and reduced memory requirements. The system is specifically suited to use the P-code generated by the version of Pascal developed by the University of California at San Diego.

Each of the four integrated circuits is contained in a 40-pin package. The first is an arithmetic chip, which contains a microinstruction decoder, an arithmetic and logic unit, and an internal register file. The second chip is a microsequencer. It contains a macroinstruction decoder, portions of the control circuitry, the microinstruction counter, and input/output control logic. The set's other ICs, two 512-by-22-bit read-only memories, hold the microinstructions and microdiagnostics.

Together, the chips form a stack-oriented 16-bit computer. Some of the features include the ability to address 128 kilobytes (or 64 kilowords) of memory, four interrupt levels, and facilities for controlling direct memory access. Moreover, hardware floating-point arithmetic capabilities are included as part of the instruction set.

The system uses three supplies, of +5, +12, and −5 V, and runs off a 3-MHz clock signal that is subdivided into four nonoverlapping phases; users may generate these four signals as they wish or buy an IC that provides them from Western Digital. All I/O signals are three-state and compatible with transistor-transistor logic. Also, an expansion capability allows two more similar ROMs to be added for future enhancements, such as custom implementations for original-equipment manufacturers.

"The system can cover a majority of application areas from real-time controllers to dedicated processors, small-business systems, or virtually any of the application areas for which you'd use a minicomputer or any other product that requires software development based on a high-level language," says Joe DeVita, manager of systems engineering at Western Digital.

The manufacturer is also putting together a packaged system. The chip set is on an 8-by-16-in. board contained in a low-profile (5.25-in.) enclosure. Besides the four processor components, the board contains 32 kilobytes of random-access memory, two RS-232 asynchronous serial ports with switch-selectable baud rates from 110 to 19,200 bits/second, two 8-bit parallel ports, and a floppy-disk controller that is switch-selectable for single- or double-density minifloppy or 8-in. floppy disks. The floppy controller will also handle direct memory accesses and up to four drives of the same type.

The UCSD Pascal operating system is also supplied on floppy disk with the packaged unit. It contains a Pascal compiler, a Basic compiler, a file manager, a cathode-ray-tube-screen–oriented editor, as well as a debugging program and an interactive graphics package.

Need more? The system will also be sold with peripherals manufactured by a distributor of Western Digital products called Computer Interface Technology of Santa Ana, Calif. CIT will support the system with a variety of floppy-disk subsystems, printers, and terminals. "We are in the process of training their sales people, and they will make their announcement soon," says Larry Lotito, vice president of Western's Computer Products division.

Western Digital is not new to microcomputer technology. "We wouldn't have been able to do it so quickly without having the experience of both the LSI-11 and Alpha Microsystems' AMS100," admits Lotito. But the chip set does represent an entirely new product line for the company and it plans to introduce a series of related products during the next year.

The four-chip set sells for $195 in single quantities. For 1,000 plastic-packaged parts, the cost is $117 a set; and for 5,000, $83.90. For ceramic, add $8 for each set.

The chip set and packaged version will be available in the first quarter of 1979. Western Digital is aiming to have both product configurations ready by no later than January of that year.

Western Digital Corp., 3128 Red Hill Ave., Box 2180, Newport Beach, Calif. 92663. Phone (714) 557-3550 [338]

NEC introduces The College Board.

Our educational TK-80A–the first complete 8080A based single board computer.

Here's the perfect system for all levels of computer education—from basic computing to advanced programming techniques.

It's a complete 8080A based computer on a single board. With a 25-key pad, 8-digit display, 1-8K byte EEPROM monitor, 1-4K byte RAM, and three 8-bit programmable I/O ports.

And it's fully expandable. Memory can be increased off-board to a total of 64K bytes. And a standard Kansas City interface lets you hook up a cassette for additional storage. If you need a terminal, a TTY or RS 232 interface can be easily attached.

What's more, 2 or 3 TK-80A boards can be connected for instruction in sophisticated programming techniques—such as distributed processing, parallel processing, and peripheral control.

And once students have mastered the TK-80A, they can easily apply what they've learned to process control, energy control systems, and environmental control and monitoring.

The TK-80A is not only supported by our thorough documentation, it's backed by our 90-day warranty on the entire board and one year warranty on the components.

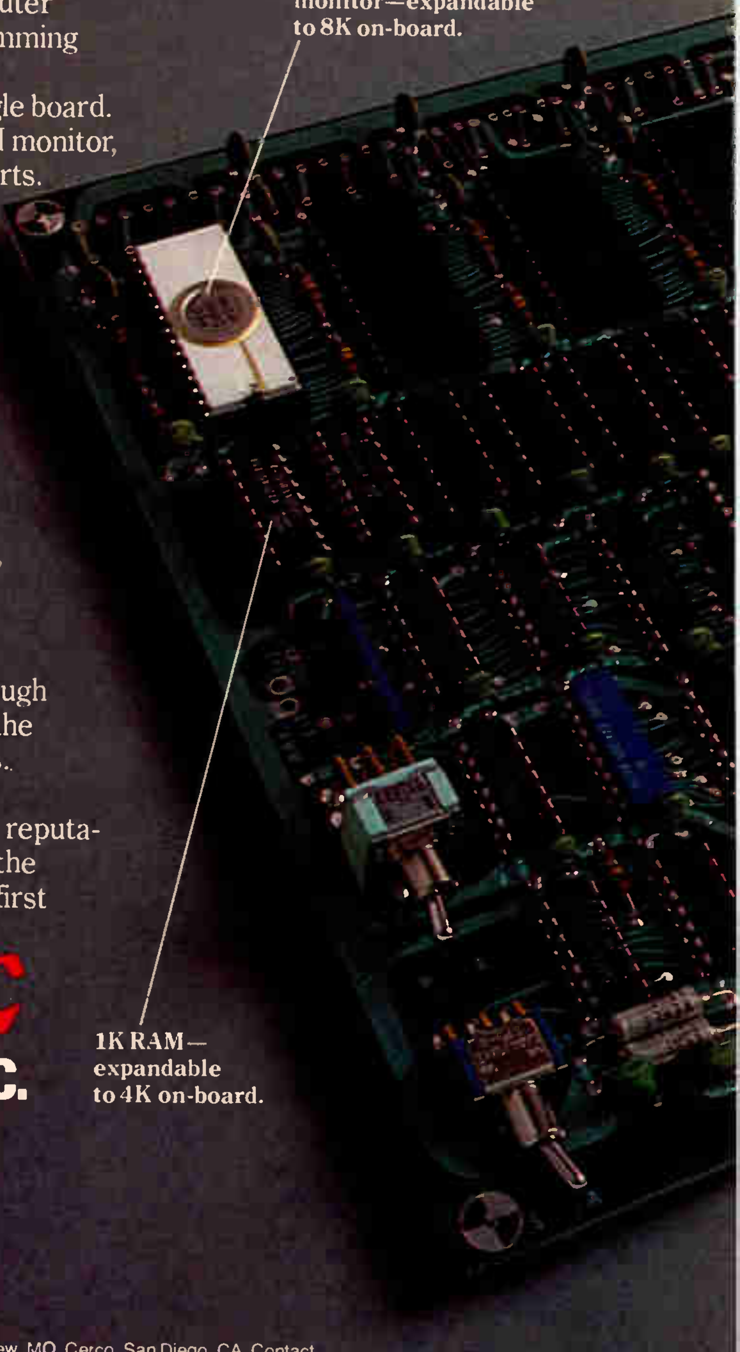
And the price is only $299.

At NEC Microcomputers, we've already built a reputation as one of the most reliable component suppliers in the industry. Now we're putting our reputation behind the first complete 8080A based computer on a board.

For more information on NEC's new college board, send in the coupon.

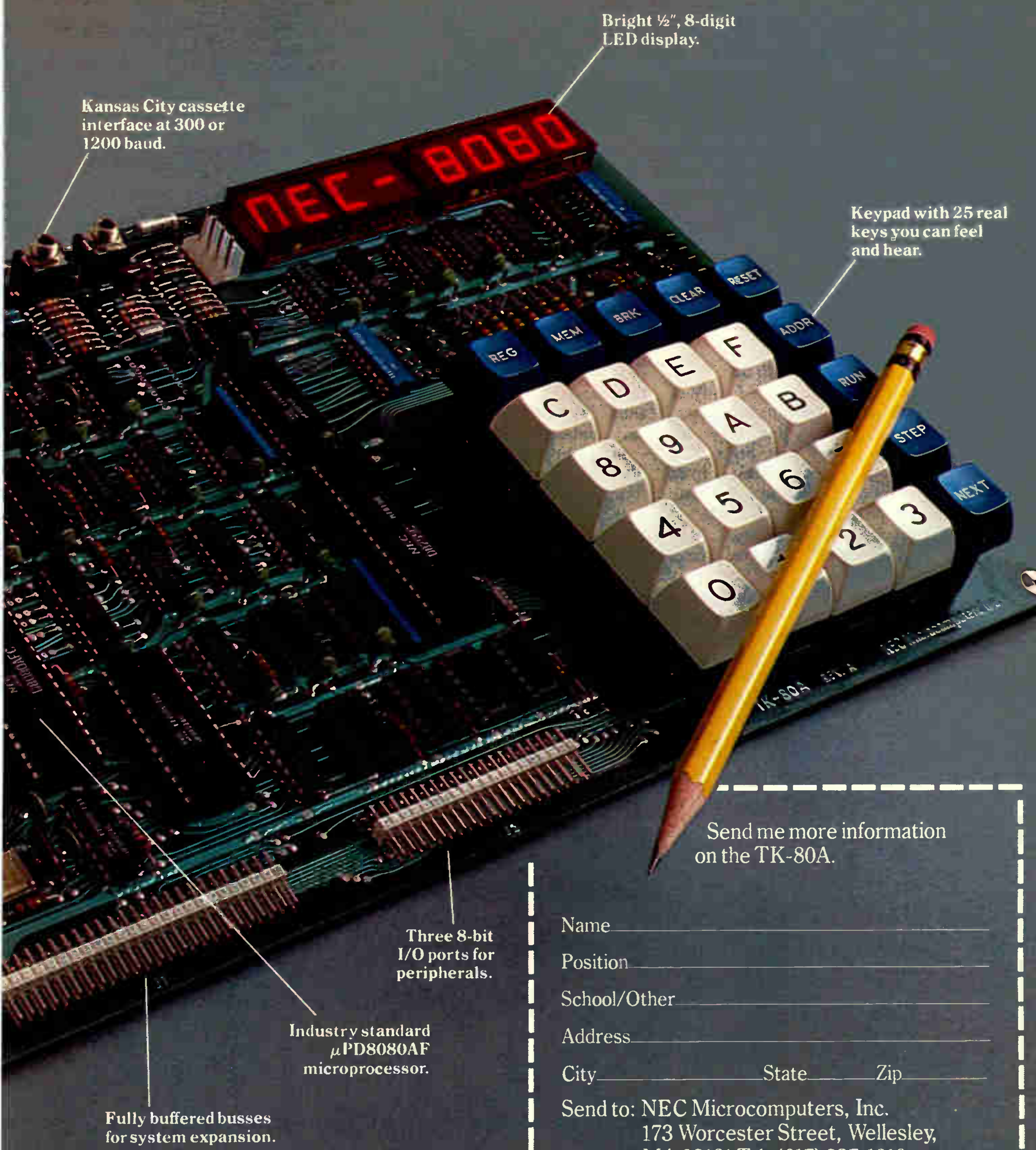
NEC

NEC Microcomputers, Inc.



REPS: Action Unlimited, Arlington, TX; Spring, TX. Burton-Medley Associates. Grandview, MO. Cerco, San Diego, CA. Contact Sales, Inc., Burlington, MA. D/Z Associates, Inc., Denver, CO. Electronic Innovators, Inc., Minneapolis, MN. Eltron, Phoenix, AZ HLM Assoc., Northport, NY; Parsippany, NJ. Imtech, Inc., Cleveland, OH; Dayton, OH. Kaytronics Limited, Ville St. Pierre, Quebec; Downsview, Ontario; Surrey, British Columbia. L & M Associates, Pikesville, MD; Montpelier, VA. Harry Nash Associates, Willow Grove, PA. R.C. Nordstrom & Company, Lathrup Village, MI. Perrott Associates, Inc., Fort Lauderdale, FL; Clearwater, FL; Orlando, FL. Santana Sales, Costa Mesa, CA. Stone Component Sales, Waltham, MA. Technology Sales, Inc., Palatine, IL. Trident Associates, Inc., Sunnyvale, CA. Tri-Tronix, Albuquerque, NM. Tri-Tronix NW, Mercer Island, WA. 20th Century Marketing, Inc., Huntsville, AL; Greenville, TN. Wolff's Sales Service Company, Raleigh, NC.

DISTRIBUTORS: Almo Electronics Corp., Philadelphia, PA. Baltimore, MD. Bell Industries, Bellevue, WA. Century Electronics, Albuquerque, NM; Wheatridge, CO; Salt Lake City, UT. Norman Davis Electronics, South Euclid, OH. Diplomat/Westland, Inc., Sunnyvale, CA. Diplomat/Southland, Inc., Clearwater, FL. Diplomat/Lakeland, Inc., Elk Grove Village, IL. Diplomat/IPC of Mass., Chicopee Falls, MA. Diplomat, Holliston, MA. Diplomat/Northland, Inc., Farmington, MI. Diplomat/Electro-Com Corp., Min-


Bright ½", 8-digit LED display.
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Three 8-bit I/O ports for peripherals.
Industry standard μPD8080AF microprocessor.
Fully buffered busses for system expansion.
NEC-8080
REG
MEM
BRK
CLEAR
RESET
ADDR
RUN
STEP
NEXT
TK-80A

Semiconductors

Triacs shed heat well

25-A units use beryllia to keep thermal resistance down to 1.2°C/W maximum

When used as switches in appliances and industrial controls, a family of triacs does better than electromechanical relays—and they approach the relays' low price. The CSB20, 40, and 60 series from Unitrode Corp. have peak off-state voltages of 200, 400, and 600 V, respectively, and are housed in a package designed for good heat dissipation.

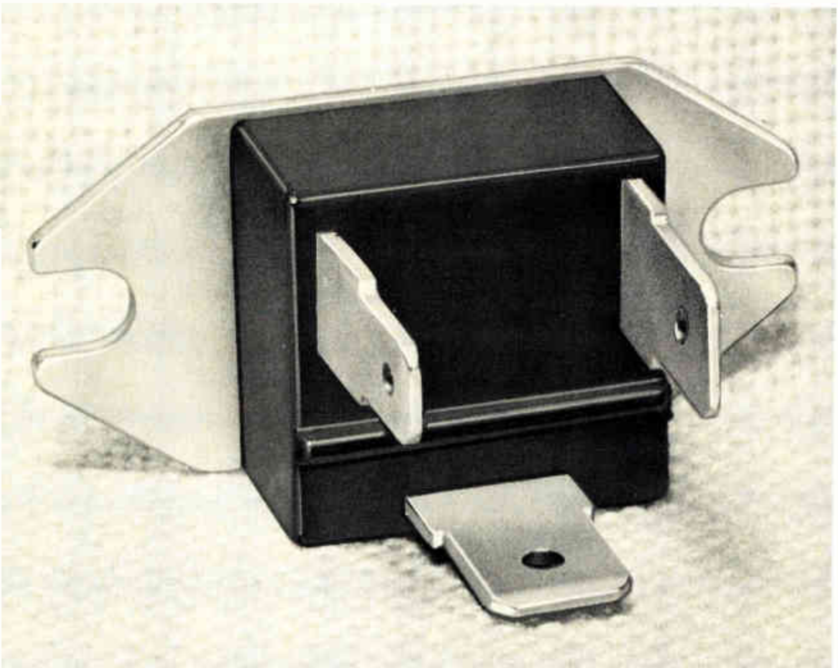
Joseph Pappalardo, product marketing manager for thyristors, says the triacs are being evaluated by a number of potential users for application in motor controls for washers and dryers and in power and motor controls for microwave ovens, machine tools, and energy control and conservation systems.

The CSB family is designed in accordance with Underwriters Laboratories requirements, and Unitrode has applied for UL approval. On-state current is 25 A rms at 65°C, with voltage isolation of 2,500 V rms between any of the triac's three quick-disconnect terminals and its TO-3–type flange.

Peter Jenner, Unitrode's manager of product marketing, says the triac's lack of mechanical movement, combined with the package's thermal design, will mean longer life. This should appeal to appliance manufacturers because it will reduce their warranty costs. "And," Jenner adds, "we think reliability is an idea that can be sold to consumers."

In each of the packages, the chip is soldered to a one-piece copper lead frame that, in turn, is soldered to a beryllia substrate. The substrate isolates the triac electrically from the flange, but continues the low-thermal-resistance path to the nickel-plated copper flange. That path contributes to the low overall thermal resistance of these devices—a maximum steady-state level of 1.2°C/W. The series uses the same basic design and manufacturing techniques as the company's popular ChipStrate line of power devices.

These are not the first 25-A triacs aimed at the white-goods and industrial market. Unitrode officials know



Sol.® The small computer that won't fence you in.

A lot of semantic nonsense is being tossed around by some of the makers of so-called "personal" computers. To hear them tell it, an investment of a few hundred dollars will give you a computer to run your small business, do financial planning, analyze data in the engineering or scientific lab — and when day is done play games by the hour.

Well, the game part is true. The rest of the claims should be taken with a grain of salt. Only a few personal computers have the capacity to grow and handle meaningful work in a very real sense. And they don't come for peanuts.

Remember, there's no free lunch.

So before you buy any personal computer, consider Sol.® It costs more at the start but less in the end. It can grow with your ability to use it. Sol is not cheap. But it's not a delusion either.

Sol small computers are at the very top of the microcomputer spectrum. They stand up to the capabilities of mini systems costing four times as much.

No wonder we call it the serious solution to the small computer question.

Sol is the small computer system to do the general ledger and the payroll. Solve engineering and scientific problems. Use it for word processing. Program it for computer aided instruction. Use it anywhere you want versatile computer power!

Build computer power with our software.

At Processor Technology we've tailored a group of high-level languages, an assembler and other packages to suit the wide capabilities of our hardware.

Our exclusive Extended BASIC is a fine example. This BASIC features complete matrix functions. It comes on cassette or in a disk version which has random as well as sequential files.

Processor Technology FORTRAN is similar to FORTRAN IV and has a full set of extensions designed for the "stand alone" computer environment.

Our PILOT is an excellent text oriented language for teachers.

Sold and serviced only by the best dealers.

Sol Systems are sold and serviced by an outstanding group of conveniently located computer stores throughout the U.S. and Canada.

For more information contact your nearest dealer in the adjacent list. Or write Department B, Processor Technology, 7100 Johnson Industrial Drive, Pleasanton, CA 94566. Phone (415) 829-2600.

In sum, all small computers are not created equal and Sol users know it to their everlasting satisfaction.

Processor Technology

Circle 159 on reader service card

of one competitive unit already introduced, but contend that the CSB series' lower price and beryllia substrate will make it more attractive. The competitive unit has an alumina substrate, and beryllia has better thermal conductance.

Sample quantities are available now, with production volumes to come in January. Prices in quantities of 1,000 to 9,999 for the CSB20, 40, and 60 are $2.60, $2.85, and $3.35 each, respectively, dropping to $1.98, $2.15, and $2.54 each, respectively, in lots of 10,000.

Unitrode Corp., 580 Pleasant St., Watertown, Mass. 02172. Phone Joseph Pappalardo at (617) 926-0404 [411]

Analog detectors discriminate up to 100 discrete levels

The TL490 and 491 convert input signal levels to outputs consisting of 1 to 10 discrete signals. Similar to the five-output TL489 analog-level detector introduced earlier this year [*Electronics*, March 16, p. 39], these devices contain 10 comparators and an internal voltage reference network. But unlike the earlier version, the new devices have a threshold increment field-adjustable from 200 mv down to 50 mv, so that by placing at most 10 units in parallel it is possible to detect up to 100 analog levels.

The two new units differ in their output capabilities. The TL490 can sink up to 40 mA and withstand 32 V, so it drives light-emitting diodes, filament lamps, or transistor-transistor-logic or metal-oxide-semiconductor devices. The TL491, with its emitter pull-up outputs, offers 55 V and can source 25 mA for driving vacuum fluorescent displays.

Available now in 16-pin dual in-line plastic packages, both units operate in the 0°-to-70°C range. The TL490 and TL491 are priced at $1.08 and $1.22, respectively, in quantities of 100 or more. Ceramic-package units are also available in sample quantities.

Texas Instruments Inc., Inquiry Answering Service, P. O. Box 225012, M/S 308 (Attn: TL490/491), Dallas, Texas 75265. Phone Dale Pippenger at (214) 238-5908 [416]

24-bit multiplier heads high-performance family

Because new applications for fast Fourier transforms and digital filtering are pushing the limits of device

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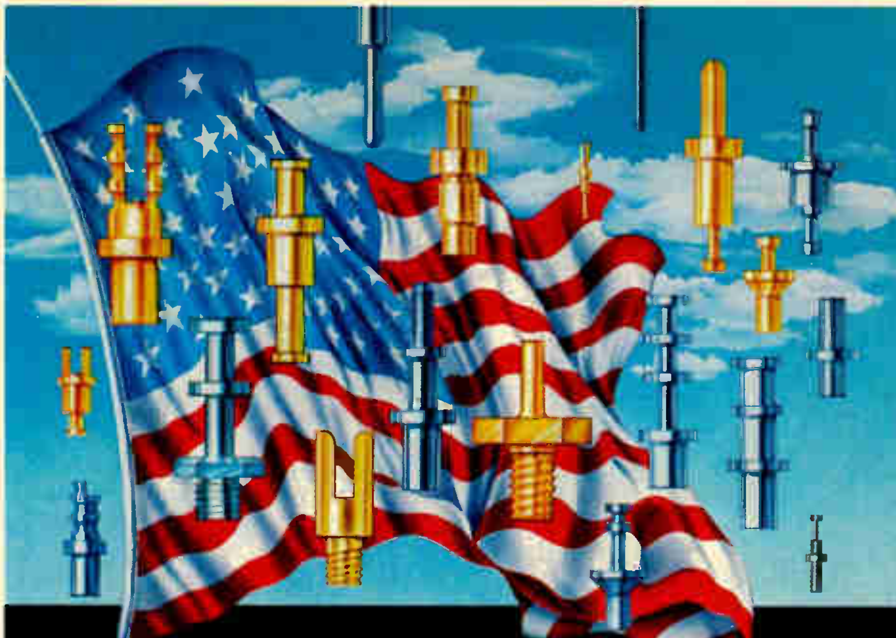
Mail Catalog #243



Our solder terminals never die, never fade away.

They are made of the finest materials, by people who care about quality and durability. CAMBION offers 96 basic styles, more than 400 types—the widest selection of off-the-shelf solder terminals you can get anywhere. Terminals come in swage, press and thread mount types. Single, double or triple turrets, pin types without turrets, feed-thru, double-ended, hollow, flared and forked types. Close tolerances, precision threads, durable finishes, the best quality base materials—all are standard from CAMBION. Try us. You *will* return. For a free catalog, write or call CAMBION. Cambridge Thermionic Corporation, 445 Concord Avenue, Cambridge, MA 02138. Phone: (617) 491-5400. In California, 2733 Pacific Coast Highway, Torrance, CA 90505. Phone: (213) 326-7822.

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We make the widest range of inkless, thermal-writing OEM strip chart recorder modules in the industry. Twenty models in all. Everything from our new lightweight, miniature, single-channel, DC model to eight-channel modules that write on plastic or chemically coated paper.

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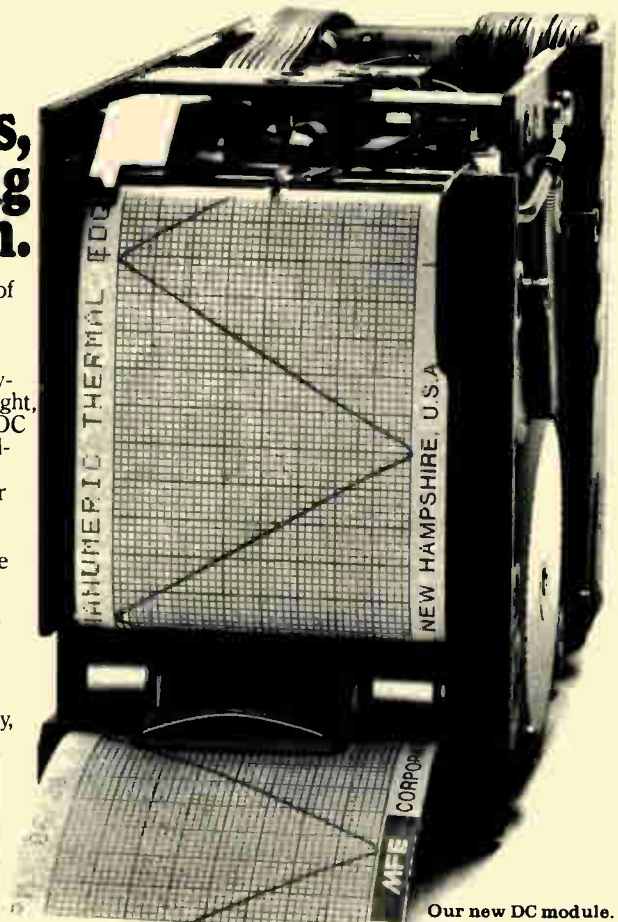
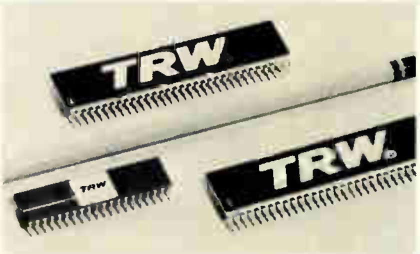
#1 in OEM Recorders. **MFE**



Our new DC module. (Seen here actual size.)

Circle 244 on reader service card

New products



number crunching and processing speeds, TRW has created a family of high-performance monolithic multipliers. Heading this group is the MPY-24HJ, a device that can produce a 48-bit product from two 24-bit numbers in just 200 ns.

Cramming over 30,000 electronic components on a 324-by-348-mil chip, the arithmetic unit can provide the product of 2's complement or absolute numbers, or a mixture of both. With its simplified clocking, no data hold time is necessary, and, for asynchronous output, the output can be made transparent.

Also included in the MPY/HJ line are 16- and 12-bit multipliers that take a respective 100 and 80 ns to produce a product while consuming only 3 and 2 W, respectively. These units have the features of the 24-bit unit already mentioned and are plug-compatible with earlier, slower AJ versions. Also available are 8-bit versions intended for digital video applications.

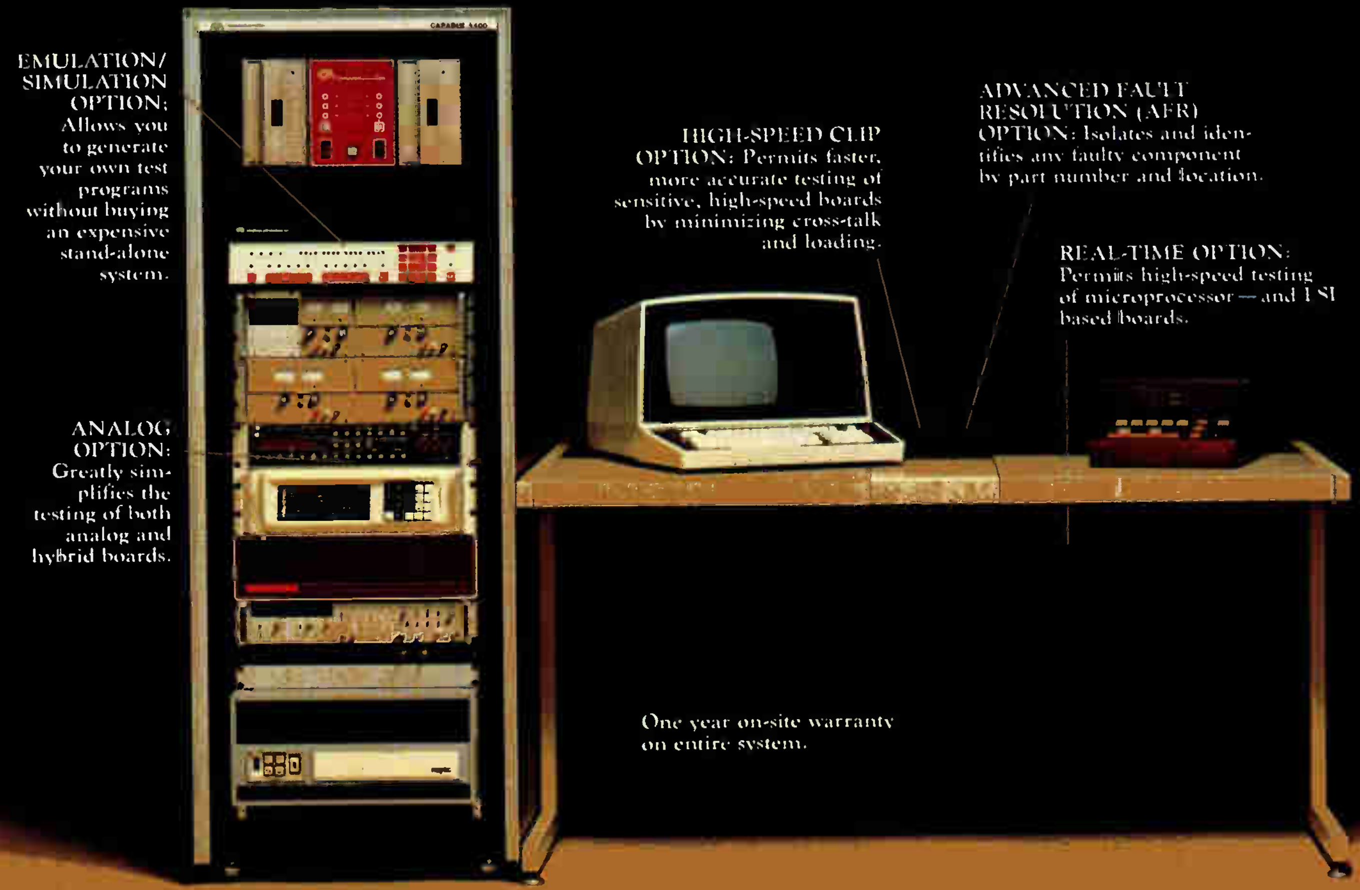
The MPY-24HJ is priced at $310 in hundreds. In the same quantities, 16- and 12-bit units are priced at $157 and $103, respectively. A 65-ns 8-bit multiplier is priced at $59; a faster, 45-ns 8-bit device costs $71. All units will be available from distributors by next month.

TRW LSI Products, P. O. Box 1125, Redondo Beach, Calif. 92078. Phone Bill Koral at (213) 535-1831 [414]

Voltage regulator boasts thermal regulation spec

Not content to specify only line and load regulation for their latest integrated-circuit voltage regulator, designers of the LM150 have added a new specification: thermal regula-

INTRODUCING THE AUTOMATIC CARD TESTER YOU CAN'T OUTGROW.



You're looking at a CAPABLE™ Tester from ComputerAutomation.

But what's more important, you're looking at an automatic card tester that's truly modular in design.

And that makes it totally different from any other brand of tester on the market today.

Designed-in modularity means no matter how complex your boards become, they can't outgrow a CAPABLE Tester.

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An Ample Example.

Take our CAPABLE Tester Model 4100. It's perfect for fast production-line testing and fault isolation. While keeping overall costs down.

What's more, you get all the basics. A powerful ComputerAutomation LSI-2 computer. 32K words of memory. A rugged floppy disk drive. A full-function CRT. Plus a comprehensive software package that includes computer Guided Fault Isolation (GFI), Fault Detection Verification (FDV) and Automatic Fault Isolation (AFI).

Where you grow from there, though, is entirely up to you.

You can keep things small, relatively specialized. Or, you can build your CAPABLE up into a model like the 4400 (as shown) to test complex boards containing LSI, VLSI and microprocessor components.

No more growing pains. Ever.

The CAPABLE's designed-in modularity makes it remarkably easy to add-on whatever you need. More programmable pin modules. Real-time testing. Advanced Fault Resolution (AFR). Or an analog test option.

You can even expand your CAPABLE into a full-blown Logic Simulation System and develop your own test programs.

Best of all, no matter how far you grow, ComputerAutomation provides you with all the operating software you need—absolutely free—including enhancements, updates and new features.

So, before you buy an automatic card tester that will literally stunt your growth, look into the CAPABLE Family from ComputerAutomation.

We have a way of growing on you.

ComputerAutomation
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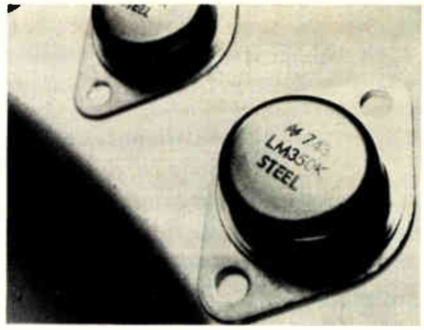
We're making history in ATS.

2181 Dupont Drive, Irvine, California 92713, (714) 833-8830. Or, call one of the following regional offices in: **Bloomfield, NJ,** (201) 338-8870; **Des Plaines, IL** (312) 297-1606; **Santa Clara, CA** (408) 985-6800. District offices located in **Dallas, TX; Waltham, MA; Falls Church, VA; Santa Ana, CA; Kettering, OH;** and **Toronto, Canada. In Europe:** CAI Ltd., 44-27324140; CAI G m b.H., 49-61033627.

Circle 163 on reader service card



tion. With this parameter, users will be able to calculate worst-case output change under any condition of line and load change.

The monolithic device, which is capable of providing over 3 A for any user-selected voltage in the range from 1.2 to 32 V, offers a typical line regulation to within 0.005% of output voltage and load regulation to within 0.1%—specifications that are highly respectable by themselves. But in addition, thermal regulation—defined as the change in output voltage for a change in power dissipation over a 20-ms period—is guaranteed to be within 0.01%/W, which compares with 0.1%/W for earlier regulators.

The reason for so specifying the device is that changes in line and load result in a change in IC power dissipation. When this occurs, the temperature gradient across the chip affects the voltage output in about 5 to 50 ms. Since most regulation tests are done in approximately 100 μs, ordinary specifications do not reflect the results of these changes.

Different versions of the device are available specified for operation in different temperature ranges. In quantities of 100 and up, prices begin at $8.65.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Dave Whetstone at (408) 737-5856 [415]

Signal transistor raises voltage rating to 450 V

Designed for applications where voltage swings of over 400 V are encountered, the DTN9000 is an


The quarter billion keyboard. Our unique "Golden Touch" capacitive keyboard is rated at 250,000,000 MCBF per keyswitch. That's at least double anybody else's rating. New patented features make the "Golden Touch" exceptionally resistant to moisture, dust and electrical noise. We guarantee a 1% AQL and give a two-year warranty. Every "Golden Touch" we produce is designed precisely to *your* specifications... because we sell only to volume OEM manufacturers. So *you* name whatever options, circuitry, configuration and legends you want. All this at competition-beating prices.
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Circle 165 on reader service card
World Radio History

npn transistor that has a V_{CEO} rating of 450 V—a considerable increase over the 300 to 350 V ratings of similar signal transistors. Its high rating should make it particularly attractive for application in electrostatic printers and ignition systems, as well as in cathode-ray-tube discharge, and electroluminescent displays.

A planar transistor, the DTN9000 has protected junctions that reduce collector-to-base leakage current to only 50 nA. Maximum collector current is 500 mA.

Versions of the transistor designated with a T suffix have a heat sink tab and thermal resistances of 150°C/W in free air and 35°C/W with an infinite heat sink. Those without the tab have a thermal resistance of 200°C/W.

The transistors can replace 2N5830, 2N6218, 2N6515, and similar units. In quantities of 100 or more, the DTN9000 is priced at 64 cents, the DTN9000T at 73 cents.

Dionics Inc., 65 Rushmore St., Westbury, N. Y. 11590. Phone Manny Sussman at (516) 997-7474 [413]

General-purpose rectifier rates up to 2,200 A at 3,000 V

Offered in forward-current ratings of 1,300, 1,800, and 2,200 A and accommodating voltages of 100 to 3,000 V, the R9G0 is a general-purpose rectifier that handles as much as 20% more current than the R920, which it replaces, and similar size rectifiers. The device can be used in battery charger power supplies and controls for dc resistance welders and motors.

Disk packaging allows the device to be cooled from one or two sides. The R9G0 is available in factory air- or water-cooled heat exchangers; matched units are available for series or parallel operation. A 2,200-A, 1,200-V rectifier is priced at $167 in quantities of 100 to 999; four to six weeks is required for delivery.

Semiconductor Division, Westinghouse Electric Corp., Youngwood, Pa. 15697. Phone (412) 924-7272 [419]

Microcomputers & systems

Analyzers talk to each other

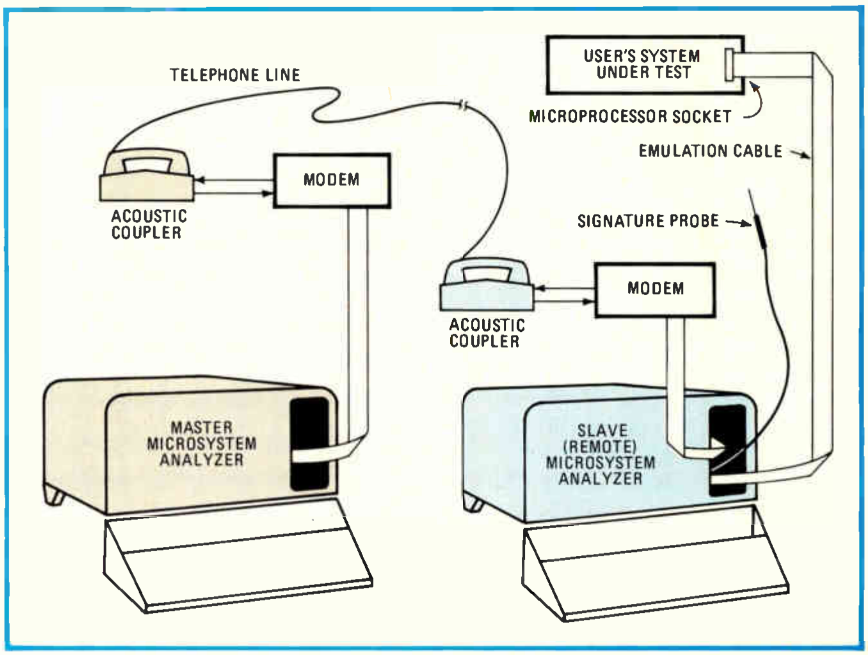
Communications board lets a home-office μSA control a similar unit in the field

A communications option for the MicroSystem Analyzer fault-isolation and diagnosis tool allows two μSAs to collaborate through a serial link to solve problems together. The communications board fits into the field serviceman's portable μSA unit. If, while using the μSA's in-circuit-emulation and signature-analysis capabilities to troubleshoot a microprocessor-based system, a serviceman finds himself in trouble, he can easily get help. With the new feature, along with a modem and an acoustic coupler, a service specialist miles away from the trouble site can acquire full diagnostic control of the system under analysis over standard telephone lines.

The serial interface expedites fault diagnosis because a home office specialist may have greater familiarity with the particular system under test than the technician at the site. Moreover, a home-office data base may include many more test programs than the field technician has on hand at the service location. This option thereby reduces the inventory of test programmable read-only memories that the field service personnel must keep with them. Updating a test program in a central data location effectively updates it for everyone who must use it and eliminates uncertainty in the field regarding which revision level of the test is most recent.

The communications feature also enables the downloading of test routines into the μSA. An additional 8 kilobytes of random-access memory included with the option enables the transfer of diagnostic programs from a central data source, such as a disk-oriented controller or computer, to one or more μSAs. Conversely, the μSAs can return statistical information to the host controller or computer.

The serial interface permits two μSAs to be connected either directly or through a standard 103 modem. Available transmission rates are 110, 300, 600, 1,200, 2,400, 4,800, and 9,600 bits/second. When telephone lines form the communications link, an acoustic coupler is used—this provides transmission rates up to



Test track for fast LSI

The race is to the swift in LSI testing. And on this test track, you can really perform—at speeds of up to 20 MHz. Tektronix announces the high performance test tracks on the new S-3270 and S-3250 Automated Test Systems.

This team of test systems doesn't have a speed limit that keeps you in obsolescence. As microprocessors move faster—and we've already tested several that operate at 12 MHz and more—you'll be able to test them. That's a proven claim that not everyone in this business can make.

While the S-3270 handles device characterization, the S-3250 takes care of production testing or incoming inspection. Both give you uninterrupted error logging at 20 MHz. Both feature dual memory architecture, 8K of memory behind each pin, and high-performance drivers for set-up and hold measurements in one pass, and fast I/O bus testing.

The systems work together to solve the test problems of the faster, more complex devices. The S-3270 starts the race in characterization, delivering data in concise, readable form. Both systems use TEKTEST III, a device-oriented, English-like language. The S-3250 interfaces with popular handlers and probers, for optimum throughput. Together, the S-3270 and S-3250 take you from the start of the race through the checkered flag.

Don't get stuck on a track that will soon be obsolete. Call us at Tektronix to find out more about winning the LSI testing race with the S-3270 and S-3250.

See the S-3250 and S-3270 at work at the IEEE Cherry Hill Symposium, Oct. 31-Nov. 2, Cherry Hill, N.J.

For a fast response to your information needs, call our toll free Automatic Answering Service—1-800-547-1512 (Oregon residents, call collect, 644-9051)—or call your nearest Tektronix field office.

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For Technical Data circle #169 on Reader Service Card
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300 b/s. Alternatively, if a dedicated serial link is used, the system will run at any of the available transmission rates.

Although the keyboard of the slave μSA is normally locked out, identical diagnostic information is displayed on both the local and remote system analyzers.

The basic μSA, including one emulator, sells for $2,750. The communications option adds $1,250 to that price. Delivery time for a μSA, complete with interface board, is 30 days.

Millennium Systems Inc., 19020 Pruneridge Ave., Cupertino, Calif. 95014. Phone Dave West at (408) 996-9109 [371]

Graphic display system offers higher resolution

With 1,280 by 1,024 picture elements, the System 3400 graphic display offers 25% greater pixel resolution than other available systems. Both color and black-and-white graphics can be generated using the system's 12-bit, 80-ns-cycle-time microprocessor and 1,280-by-1,024-bit memory. Multiple planes of graphics may be shown separately or in combination.

Full-resolution displays have a 30-Hz interlaced refresh rate; for a 60-Hz refresh rate, a scrollable, zoomable window of 604-by-512 pixels may be displayed from the full buffer. Full memory can be refreshed, even if the displayed picture is only a subset of full memory.

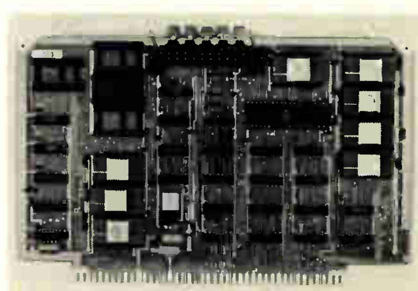
Single units sell for $10,130.

Lexidata Corp., 215 Middlesex Turnpike, Burlington, Mass. 01803. Phone (617) 273-2700 [376]

Simulator set readies users for 16-bit microprocessor

Designers who have been anxiously awaiting the introduction of Motorola's 16-bit microprocessor, the MC6809 [*Electronics*, Feb. 2, p. 95], can usefully expend some of their anticipatory energy by experimenting with a simulator module and macroinstruction assembler. The MEX6809SIM set is used in conjunction with Motorola's Exorciser, Exorciser IA, or Exorterm 200. (Also required are Exordisk II, an editor, 24-K memory and terminal.)

The simulator module has on-



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board programmable read-only memories containing an expanded version of EXbug 1.2 and a program simulating the coming microprocessor's instruction set, as well as MC6810 random-access memory for simulated variable storage and a user interrupt handler. The macro assembler comes on a diskette, along with a program demonstrating various module switch functions.

The module plugs directly into the development system's motherboard and source code is entered through the terminal console using the editor. This diskette-stored program is then assembled with the MEX6809SIM set, and the process repeats until a correctly assembled program is obtained. The object code is then loaded into development system memory for debugging.

Single sets are priced at $2,500 and are available from stock.

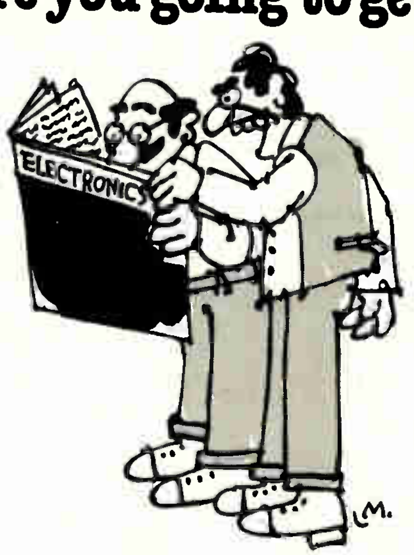
Motorola Semiconductor Products Inc., Motorola Microsystems, P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 962-2223 [374]

Z80 systems can speak powerful algorithmic language

Though generally regarded as the most powerful algorithmic/procedural language available today, APL has primarily been used for conversational terminals only in large time-sharing systems. Now, however, an APL interpreter is available that can be run on Z80 systems with a video console, 35 kilobytes of workspace, and dual 8-in. floppy disks.

Dubbed APL/Z80, it contains nearly all primitive functions and operators of APL; those not present are easily implemented as defined APL functions. The Z80 version was designed to provide a highly interactive system that responds quickly during program-development tasks. To all but intensely computationally bound tasks, response time is at most a few seconds.

APL/Z80 consists of two modules: a supervisor and an interpreter. The supervisor performs all input/output-device handling and buf-



fering, character-set translation, and overstrike recognition and generation. It transmits completed code strings to the interpreter and receives formatted values from it for display. The supervisor also handles disk input/output, allocates workspaces, and copies objects to and from active workspaces.

The interpreter module also consists of two parts. The first part interfaces with the supervisor, accepts code strings, transforms them into tokenized form, and prepares an appropriate workspace entry. In the second part, the entry is either evaluated or, in the definition mode, linked together with other lines of a defined function. Syntax analysis is done by decision-table techniques that provide high-speed and modular construction.

Licenses are available to original-equipment manufacturers for object and source code.

Vanguard Systems Corp., 6812 San Pedro, San Antonio, Texas 78216. Phone (512) 828-0553 [373]

AMD-Siemens announces single-board computer

Nine months after the technological wedding of Advanced Micro Devices and Siemens [*Electronics*, Jan. 5, p. 62], the union—Advanced Micro Computers—has produced the AMC 95/4000 single-board computer. The fast-paced device offers computational speeds as much as twice that of similar units.

The AMC 95/4000 is configured with 48 programmable input/output lines, 4 kilobytes of static random-access memory, sockets for as much as 12 kilobytes of programmable read-only memory or erasable PROM, four independent direct-memory-access channels, and eight fully programmable vector-interrupt channels. Controlling all these features is either an Am9080A or an Am9080A-4 microprocessor, depending on whether the purchaser needs a clock rate of 2 or 4 MHz, respectively.

Also on board is AMD's propri-

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TRW metal films with muscle are available from 1/8W to 5W, 200 V to 15 KV, with 1, 2 and 5% tolerance. For standards in all types of resistors, contact your local TRW distributor. Or TRW/IRC Resistors, 401 N. Broad St., Philadelphia, Pa. 19108. (215) 922-8900, Dept. G.

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™ Metal Glaze is the TRW trademark for its thick metal film resistors.

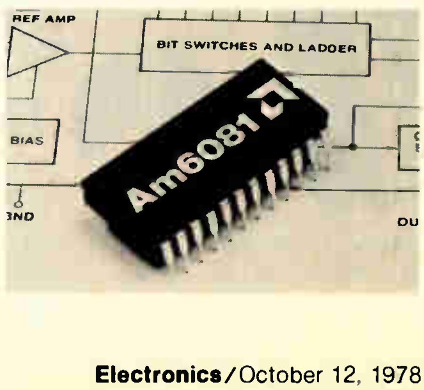
has its own independent recording amplifier and can be set for the required signal level with a built-in calibrator. Channels not used initially may be used for recording data at a later time.

The units conform to International Standards Organization and International Recording and Instrument Group standards or proposed standards. They are available in both ac models, which operate from 120- or 240-V, 50- to 60-Hz sources, and in battery-powered dc models for 12- or 24-V operation. The PR-260 dc model weighs 57 lb without batteries, and the ac model weighs 61 lb. They sell for $12,000 each. The 77-lb dc and the 88-lb ac PR-280 are priced at $17,000 each. Both models are currently available.

AMPEX Corp., 401 Broadway, Redwood City, Calif. 94063 [383]

D-a converters interface directly with microprocessors

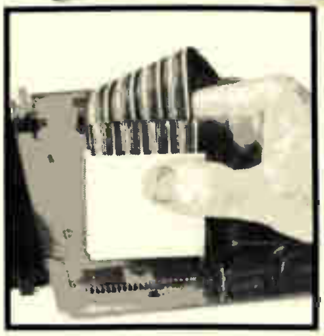
Designed to interface with virtually any 8-bit microprocessor, regardless of whether it employs bipolar or metal-oxide-semiconductor technol-



AQ Microprocessor Analyzers won't give your chip the bends.

Our clip-on probe connection is fast and safe. Your microprocessor chip remains in its own socket, or can be soldered in. There is no possibility of static damage or bent pins, and no risk of degrading socket reliability by insertion of damaged test plugs.

AQ Microprocessor Analyzers are the cost effective alternative to in-circuit emulators and CRT analyzers. Their powerful features include the ability to examine or modify the contents of all memory, I/O ports, and internal registers, including the program counter and stack register.



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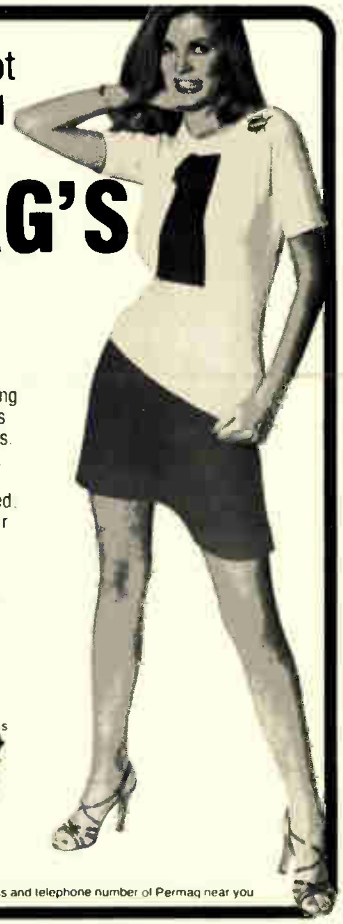

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ogy, Am6080 and Am6081 are 8-bit digital-to-analog converters containing data bus input latches as well as address and encoding circuitry.

Both devices have a minimum data-hold time of 10 ns, operate from supply voltages in the range from ±5 to ±15 v, and come in models with maximum nonlinearities of either 0.1% or 0.19% of full scale. The Am6080 delivers a differential analog output and has four control lines: most-significant-bit select, data enable, write, and chip select. In addition to these features, the Am6081 offers a second pair of differential outputs as well as status-enable and output-select control lines.

In 100-piece quantities, the 20-pin Am6080 and 24-pin Am6081 are priced at $5; they are available now from distributors.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. 94086. Phone (408) 732-2400 [385]

12-bit d-a converter settles quickly and accurately

Using a precision ladder network driven by fast, equal-value current sources, the 12-bit DAC-681 digital-to-analog converter achieves a maximum differential nonlinearity of ±½ least significant bit and a maximum output settling time of 400 ns for a full-scale change. Typical values for these same parameters are ±¼ LSB and 200 ns, respectively.

Included in the converter is a matched thin-film feedback resistor for use with an external operational amplifier and a matched resistor for bipolar offsetting. With these resistors, the maximum gain temperature instability is 5 ppm/°C.

The converter requires 9 mA from a 5- to 15-v supply and 28 mA from a −15-v supply. The military and commercial versions are priced at $145 and $39.50 each, respectively, in quantities from 1 to 25. Delivery time is four weeks.

Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021. Phone (617) 828-8000 [386]

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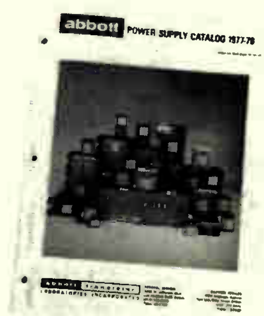
See Power Supply Section 4000, and Transformer Section 5600, Vol. 2, of your EEM catalog; or Power Supply Section 4500, and Transformer Section 0400, Vol. 2, of your GOLD BOOK for complete information on Abbott products.



abbott transistor

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Packaging & production

Fiber links need little room

Low-profile plastic-packaged assemblies fit on boards mounted on 0.5-in. centers

They're not exactly cheap now, but Texas Instruments' latest plastic-packaged fiber-optic source and detector assemblies, introduced at the Laser 78 Show in Boston, point the way toward TI's ultimate objective—a complete data link for $10. Basically, the new assemblies differ from earlier metal-can units in two important ways: the fiber pigtail exits its low-profile package parallel to the printed-circuit board on which the package is mounted instead of perpendicular to it, and the detector assembly uses a new low-voltage, high-speed silicon p-i-n photodiode. Furthermore, the entire plastic assembly has been designed for easy, inexpensive, large-scale production.

The devices are not designed for long-distance telecommunications. Rather, they are expected to be used for short runs in systems that require the particular advantages—such as noise immunity—of optical cable. As their prices drop, however, they may become competitive with flat cable and edge connectors for board-to-board wiring. But that is not likely to happen very soon.

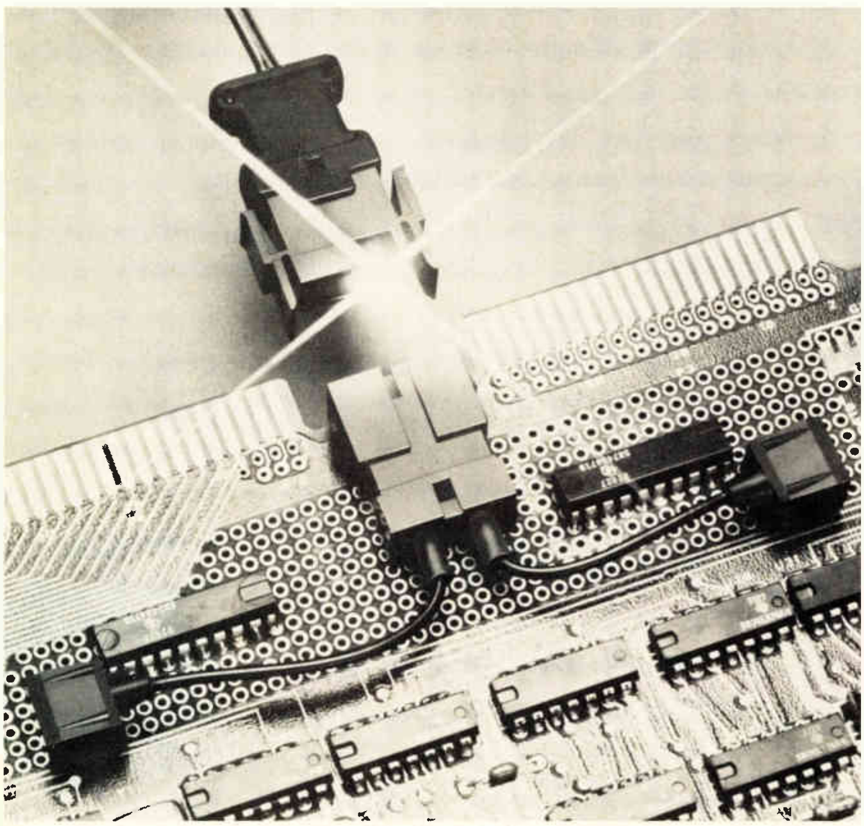
The new assemblies are housed in six-pin plastic dual in-line packages that measure 0.35 by 0.42 by 0.60 in. Because the fibers run parallel to the boards, the units can be used in systems with boards mounted on half-inch centers.

The TXES478 through TXES481 source assemblies consist of an infrared light-emitting diode mounted in a six-pin DIP, a length of fiber-optic cable, and a connector. The cable, which is made of Du Pont PFXPIR140 plastic fiber, is available in lengths from 5 to 100 cm. Two connector options are provided: the Amp Optimate single-position unit, or a ferrule for use with the Amp Optimate multiple-position connector.

The TXED455 and 456 detector assemblies are mechanically similar to the source units. However, instead of an LED, they contain a newly developed high-resistivity p-i-n photodiode that operates in the reverse-bias mode. Unlike many devices currently on the market, which require as much as 100 v for full depletion, the new diode uses an extremely thin silicon structure that allows it to be fully depleted at 5 v. With its rise time of 8 ns at 5 v, the detector, like the LED source, is compatible with transistor-transistor logic. If greater speed is required, it can be obtained by increasing the supply voltage. For example, at 25 v, the rise time drops to 3 ns.

In quantities of 100 or more units, the source assemblies sell for $39.29, the detector assemblies for $33.99. In both cases, the prices are for units with 25-cm fibers.

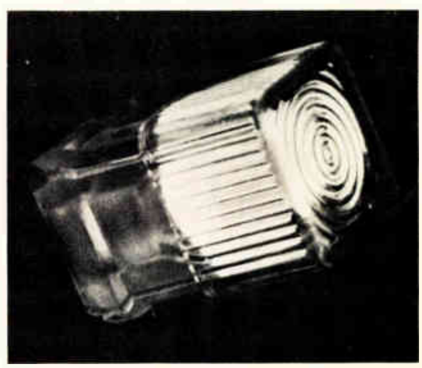
Texas Instruments Inc., Electro-Optical Components Group, P. O. Box 225012, M/S 12, Dallas, Texas 75265 [391]



LED mounting cube lights way to bar-graph takeover

A simple ⅜-in. plastic cube has joined ranks with those devices aimed at making VU meters obsolete. Dubbed Cubelite, the device can house a standard, round T 1¾ light-emitting diode and mount it on a front panel; several units in a row can form a bar-graph display.

Recognizing that if such displays are to replace standard VU meters,



There's one fully programmable LSI test system priced under $200,000

The MX-17, at $37,750

The MX-17 is an automatic, fully programmable LSI test system. At $37,750, base price, it is by far the most affordable software-programmable system on the market.

MX-17 performance is equally impressive. The MX-17, in fact, is the *only* small system that can deliver every one of these large-system capabilities:

A powerful production/engineering tool

A true general purpose system, the MX-17 permits completely valid electrical and logical testing of microprocessors, support chips, RAMs, ROMs, and custom LSI devices. It can be used for manual test or with automatic handling or probing equipment.

As an engineering tool, the MX-17 provides error diagnostics, full reporting capabilities, data logging of all test variables, and "joystick" slewing of parameters.

Software programmable

Unlike other low-cost testers, the MX-17 is fully programmable. Logic sequences, strobe placement, phase widths and relationships, and data and address formats are all under program control. Test variables can be changed as required, allowing the device under test to be stressed and margined for worst-case conditions.

Faster test times

No laggard, the MX-17. All pins are tested simultaneously for continuity. Rigorous tri-state testing is done at speed during functional testing. And DC parametric tests can be made on a pin-by-pin basis, or in parallel.

The result? Higher throughput than any other LSI test system, regardless of price.

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The MX-17 is completely field-expandable by simple card plug-in. The expanded system can include 69 timing edges, 21 voltage levels, 56 drive/sense channels, a 32K controller memory, and storage for truth tables up to 65K.

Available now

The MX-17 is fully operational — the only high-performance "low-cost" LSI test system available today. It is backed by a complete package of training, programming and field support services.

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Circle 185 on reader service card

they will have to benefit instrument designers as well as users, Cubelite's manufacturers have provided a product that eases LED mounting and yields a bright, attractive display. Gangs of lights can be mounted on a 1/16-to-1/8-in.-thick panel by simply pushing the Cubelite into a 1/4-in.-high slot from the front and slipping the LEDs into the mounts from the rear. Striated lines on the unit's sides and fresnel rings on its viewing front increase its brightness when viewed from angles of up to 90° from normal.

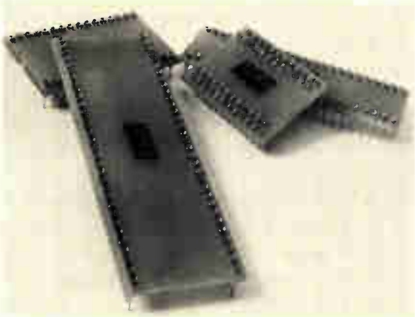
The LED mount is made from Butyrate plastic and comes in a clear version as well as in four transparent colors: red, amber, green, and yellow. Cubelites costs 15¢ apiece when ordered in 1,000-piece quantities, and deliveries are from stock to two weeks.

Visual Communications Co., P. O. Box 986, El Segundo, Calif. 90245. Phone (213) 822-4727 [393]

Low-profile LSI sockets carry 64-pin DIP and QUIP devices

Designed for the newer large-scale integrated circuits, the LSI socket series accepts dual in-line and quad in-line packages with up to 64 pins on 0.900-in. centers. The low-profile sockets have a two-piece, tapered socket terminal with a four-leaved, machined inner sleeve that permits them to double as carriers for the large-scale devices.

Closed-end construction of the socket's contacts prevents problems with solder or flux wicking. The 1,000-piece prices for the series begin at $2.94 for 32-pin units and range to $5.38 for 64-pin sockets.



Interconnection Products Division, Augat Inc., 33 Perry Ave., Attleboro, Mass. 02703. Phone (617) 222-2202 [394]

Plastic pc board spacers install quickly with no tools

Models 6044 and 6045 printed-circuit-board supports are plastic spacers that can be quickly installed without tools. One end of the support is pushed into a 0.187-in.-diameter hole in a chassis while the other is inserted in a 0.156-in.-diameter hole in the pc board.

The model 6045 (shown) is a self-locking style that retains the board with a 25-lb force, while the model 6044 is a tension-retaining device that can be used in applications that require frequent board changes. Both types are available in 12 lengths providing board clearances of 0.187 to 1.375 in.

Purchasers may choose between supports made of standard or fire-retardant nylon. Depending on style and length, prices range from $14.50 to $62.00 per 1,000 in 25,000-piece lots. Free samples are available upon request.

Grayhill Inc., 561 Hillgrove Ave., La Grange, Ill. 60525. Phone Jim Heil at (312) 354-1040 [397]

Connector terminates cables in 15 s without stripping

For use with either flat cables or flexible circuitry, the Clincher connector simultaneously mates with all conductors in the cable and is ready for use within 15 seconds. Mating is performed with a pneumatic applicator that presses the "teeth" of the

This plain brown box keeps things under control.

It may not look like much, but our new VDP-410, a general purpose minicomputer, is one intelligent building block for system development.

It gives OEMs the flexibility to configure a wide variety of systems.

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The VDP-410 is a low-cost, 16-bit CPU with enough speed and ports to support a variety of peripherals. From communications controllers without external storage capabilities, to sophisticated time-sharing systems with a string of terminals, printers and disks — the VDP-410 feels right at home in any and all of them.

The 410's DMA channel provides easy expansion. You can get a cable and an expansion chassis with five slots for 15" cards and a hefty power supply.

HERE'S WHAT'S INSIDE THE BOX.

The basic system consists of a CPU with 600 nanosecond cycle time, and 16-bit, 32K word memory, and I/O capabilities for communication with three external devices. The CPU also includes an expansion port with serial/parallel I/O capabilities.

The VDP-410's instruction set, memory organization, and I/O architecture are compatible with hardware made by Data General and other manufacturers. Operating systems, file management systems, and programming utilities are available from leading software houses as standard packages, so it doesn't take any custom configuring to please the VDP-410.

THE VDP-410. SIMPLE, INTELLIGENT, AND POWERFUL.

The 410's instruction set is Nova* compatible, and provides memory access, arithmetic, logical, and I/O functions. And it's augmented with load/store-byte, inclusive/exclusive OR, exchange accumulators, multiply/divide, and block move. So OEMs get an incredibly powerful instruction set for tasking and data management.

If you're looking for a way to keep your system under control, call or write to us. We'll be happy to tell you all about our new VDP-410.

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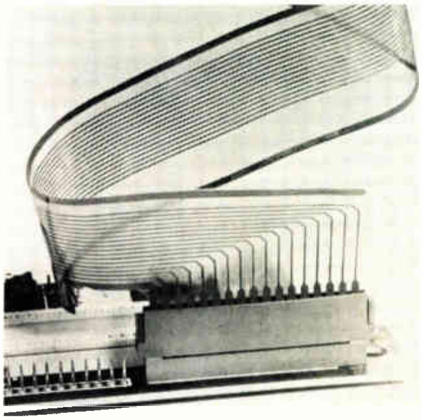
*Nova is a registered trademark of Data General Corporation.

Circle 187 on reader service card



connector through the insulation so that no cable stripping is required. Gas-tight connections are made and the connector snapped shut in a single applicator cycle.

The female connectors are stackable on 0.100-in. centers in double-row configurations and are compatible with 0.025-in. pins, as well as BergStik and other standard Berg headers. Single-row connectors that accept from 8 to 20 pins are presently in stock and other models will soon be available.

Berg Electronics Division, Du Pont Co., Route 83, New Cumberland, Pa. 17070. Phone (717) 938-6711 [398]

Machine "stitches" wires at 125-per-hour rate

Intended for low-profile wiring of printed-circuit boards, backplanes, and packaging panels, a stitch-wire machine from Interconnection Technology wires at a rate of 125 wires per hour on manually positioned boards. Activated by hand or foot-pedal, the machine can accomplish point-to-point, routed, or twisted-pair wiring on planar or pin-loaded boards.

The wirer has an overvoltage protection circuit, in addition to an internal bond monitor that meets the requirements of Navy stitch-wire specification WS-14783. The machine is priced at $995 in its basic configuration.

Interconnection Technology Inc., 1310 Logan Ave., Costa Mesa, Calif. 92626. Phone (714) 540-2424 [400]

L29

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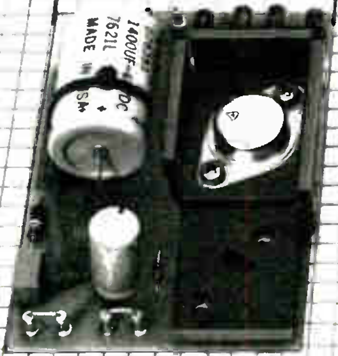

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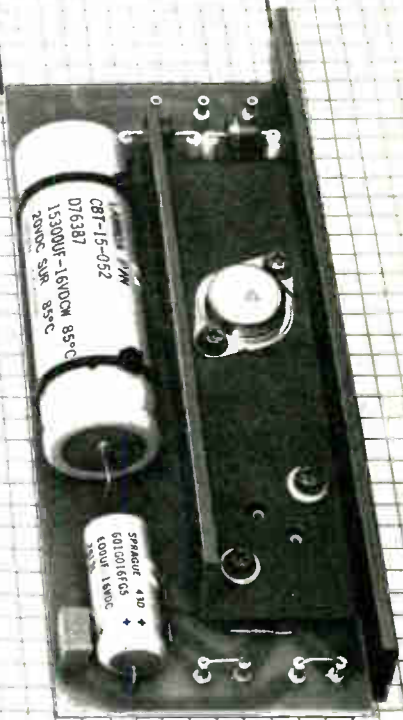
+12 VOLTS 3.0 AMPS



+5 VOLTS 5.0 AMPS

Typical triple output custom supply using Lambda's new sub-modules— total cost of three modules, only $65.00*

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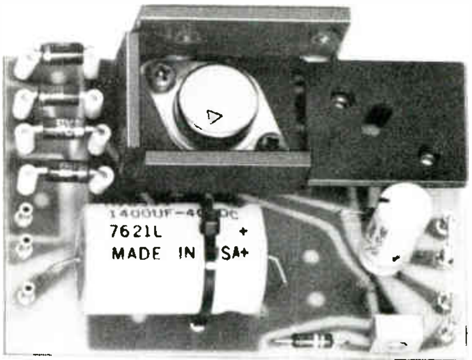

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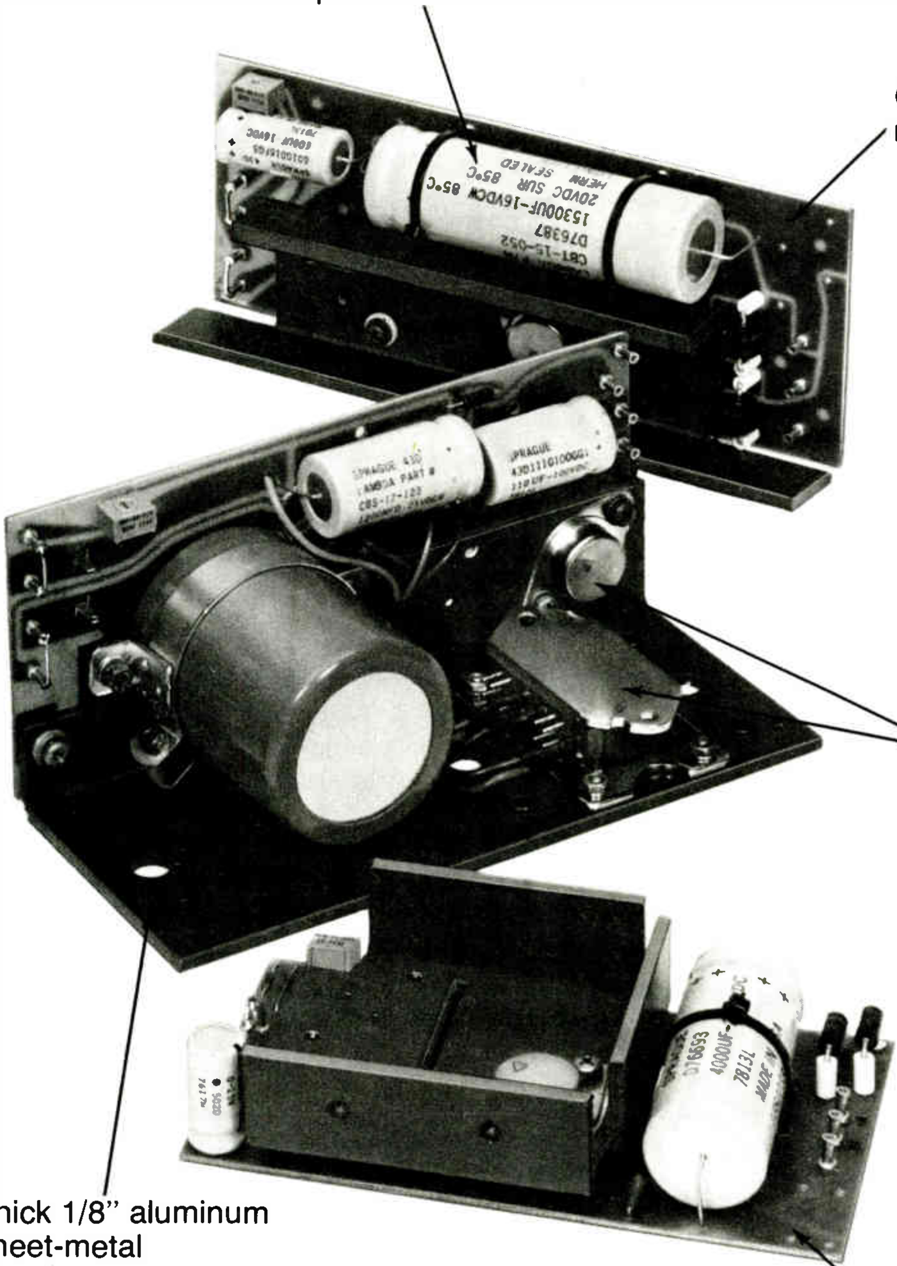
- ☐ Design change reaction time reduced
- ☐ No charge for thermal design data


Sprague electrolytic capacitors.
Only 8 to 12 parts for maximum reliability and minimum repair.
Advanced design Lambda monolithic and hybrid semiconductors provide superior performance and simplify design.
Thick 1/8" aluminum sheet-metal chassis
CC4®printed circuit board with plated thru-holes, fungus inert, flame retardant

RATINGS AND PRICES

V_o-VOLTS	MODEL	MAX I_o AMPS	COMPLETE ELEC & MECH SPEC. PG.	UNIT PRICES* 100 Pc. MIX	500 Pc. MIX	1000 Pc. MIX
5 VOLTS						
5±2% FIXED	LSS-50-5	1.5	5-6	$21	$19	$13
5±5% ADJ	LSS-80-5	10.0	11-12	$53	$48	$45
5-6 VOLTS						
5-6 ADJ	LSS-50-01	1.5	5-6	$23	$21	$18
	LSS-60-01	3.0	7-8	$26	$23	$20
	LSS-70-01	5.0	9-10	$40	$36	$32
6 VOLTS						
6±5% ADJ	LSS-80-6	10.0	11-12	$53	$48	$45
9-15 VOLTS						
9-15 ADJ	LSS-50-02	1.5	5-6	$23	$21	$18
	LSS-60-02	3.0	7-8	$26	$23	$20
	LSS-70-02	5.0	9-10	$40	$36	$32
12 VOLTS						
12±2% FIXED	LSS-50-12	1.5	5-6	$21	$19	$13
12±5% ADJ	LSS-80-12	8.5	11-12	$53	$48	$45
15 VOLTS						
15±2% FIXED	LSS-50-15	1.5	5-6	$21	$19	$13
15±5% ADJ	LSS-80-15	8.0	11-12	$53	$48	$45
20-28 VOLTS						
20-28 ADJ	LSS-50-03	1.5	5-6	$23	$21	$18
	LSS-60-03	3.0	7-8	$26	$23	$20
	LSS-70-03	5.0	9-10	$40	$36	$32
24 VOLTS						
24±5% ADJ	LSS-80-24	7.5	11-12	$53	$48	$45
28 VOLTS						
28±5% ADJ	LSS-80-28	7.0	11-12	$53	$48	$45

*PRICES ARE FOR MIX QUANTITIES. A MIX CAN CONSIST OF 100 OF THE SAME UNIT AS WELL AS 100 DIFFERENT MODELS.

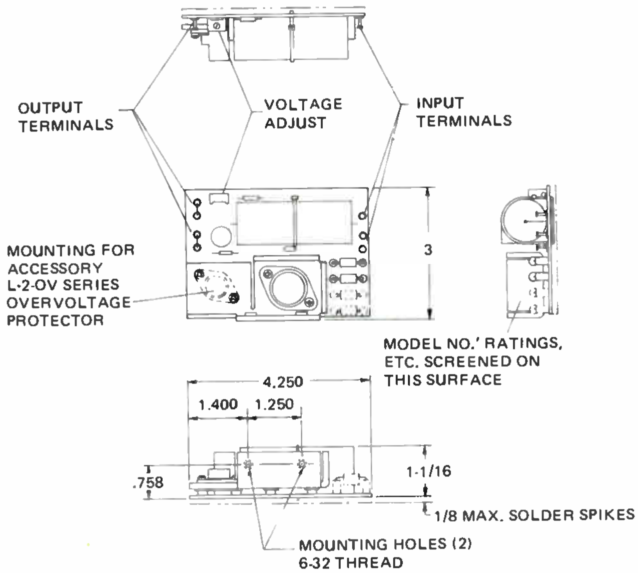
PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX
INPUT VOLTAGE	$V_{IN}DC$	$I_o = 1.5A$	$V_o + 3.4V$	SEE TABLE I
	$V_{IN}PKAC$	$I_o = 1.5A$	$\frac{V_o + 3.9V^{(1)}}{.85}$	SEE TABLE I
OUTPUT VOLTAGE	V_o		5V	28V
OUTPUT CURRENT	I_o			1.5A
CURRENT LIMIT KNEE	I_K	$V_{IN} = V_o + 5V$		2.8A
SHORT CIRCUIT CURRENT	I_{SC}	$V_{IN} = 20V$		1.8A
STANDBY CURRENT	I_Q	$V_{IN} = V_o + 5V$		10mA
STORAGE TEMPERATURE	T_S		-40°C	+85°C
AMBIENT OPERATING TEMPERATURE	T_A		0°C	65°C
LOAD REGULATION		$V_{IN} = V_o + 5VDC$, $\Delta I_o = 1.5A$		0.6% V_o
LINE REGULATION		$I_o = 1.5A$, $\Delta V_{IN} = 5$ VDC		1.0% V_o
PROGRAMMING RESISTANCE	R_P			200Ω/V
PROGRAMMING VOLTAGE	V_P			IV/V
TEMPERATURE COEFFICIENT	T.C.	$V_{IN} = V_o + 5$ V, $I_o = 100mA$		0.03% V_o/°C
RIPPLE AND NOISE				SEE FIGURE 3

(1) ASSUMES 60Hz INPUT LINE FREQUENCY AND A RECTIFICATION EFFICIENCY (V_{CF} AVG/V_{SEC}PK) = 85%

TABLE I

MODELS	$V_{IN}DC$ MAX	$V_{IN}PKAC$ MAX (NO LD.)	INPUT CAP (μf)
LSS-50-01	16.5V	18.5V	3.9K
LSS-50-5	16.5V	18.5V	3.9K
LSS-50-02	25.5V	29V	2.5K
LSS-50-12, 15	25.5V	29V	2.5K
LSS-50-03	40V	40V	1.5K



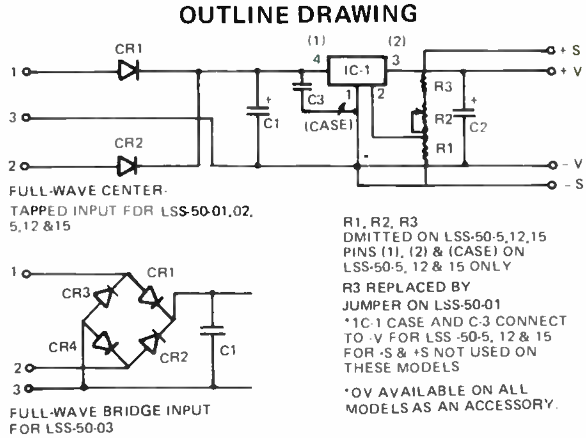
OUTLINE DRAWING

DESIGN EXAMPLE

Requirements: $V_o = 12V$ @ 0.5A
$T_A = 60°C$
Input Line Voltage = $117V_{RMS}$ ±10%, 60 Hz

1. For 12 volts at 0.5 AMP choose LSS-50-12. (or LSS-50-02)
2. From specification table, V_{IN} peak minimum =
$$\frac{Vo + 3.9}{.85} = \frac{12 + 3.9}{.85} = 18.7V$$
[Note that this assumes a rectification efficiency $\left(\frac{V_{AVG}}{V_{PEAK}}\right)$ of 85%]
3. From the transformer design, calculate V_{IN} peak maximum at high line. For this example, assume that V_{IN} peak maximum is 25.0 volts. Therefore $V_{AVG}MAX$ = 25 x .85 = 21.25V.
4. Compute the voltage differential (V_D) across the module as follows: $V_D = V_{AVG}MAX - V_o$
$V_D = 21.25 - 12 = 9.25V$
5. From Design Curve (Fig. 1) at $V_D = 9.25V$, $I_o = 0.5A$ and T_A=60°C, power dissipation (P_D) = $V_D \times I_o$ = 4.625W and the thermal impedance of the required heat sink (θ_{RAD}) is 10.75° C/W. This corresponds to an absolute heat sink temperature of 107.5°C.

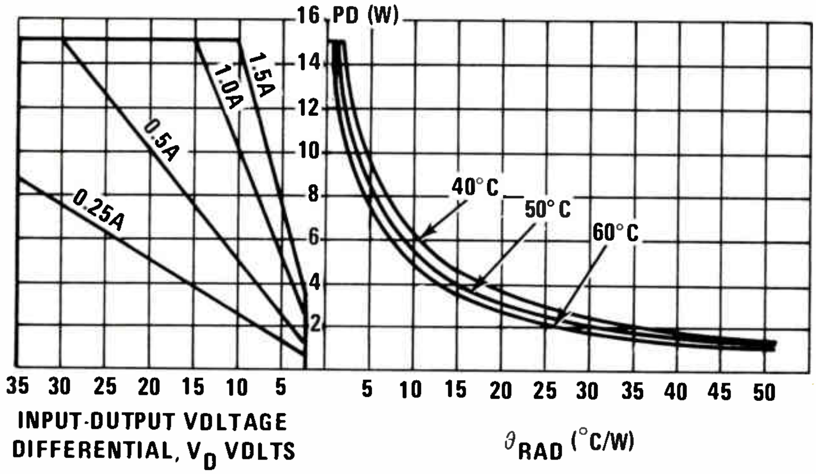
Note: For DC input in the above example, V_{IN} minimum would be V_o + 3.4V (from specification table) and $V_{AVG}MAX$ would be $V_{IN}MAX$-1.



SCHEMATIC DIAGRAM

OPERATIONAL DATA

FIG. 1 POWER DISSIPATION VS INPUT-OUTPUT DIFFERENTIAL
POWER DISSIPATION VS RADIATOR THERMAL
IMPEDANCE FOR VARIOUS OUTPUT CURRENTS



ABSOLUTE RATINGS

1. $2.4V \leq V_D \leq 40V$
2. V_{IN} MAX = 40V
3. $5V \leq V_0 \leq 28V$
4. I_0 MAX = 1.5A

FIG. 2 POWER DERATING AS A FUNCTION OF RADIATOR TEMPERATURE

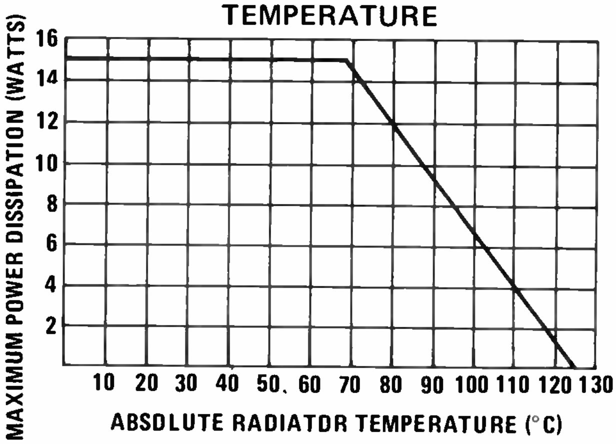


FIG. 3 OUTPUT RIPPLE AS A FUNCTION OF OUTPUT VOLTAGE WITH 3V PK-PK INPUT RIPPLE @ 120 Hz

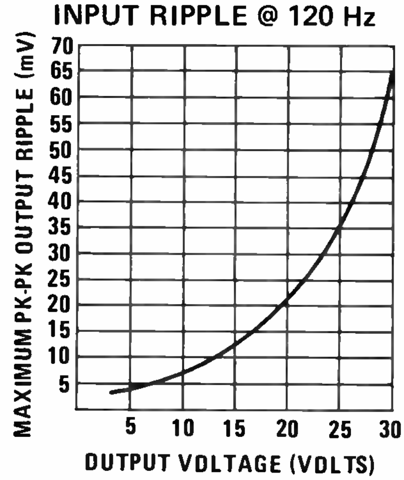


FIG. 4 D.C. SAFE OPERATING AREA AS A FUNCTION OF RADIATOR THERMAL RESISTANCE AT 40°C AMBIENT TEMPERATURE

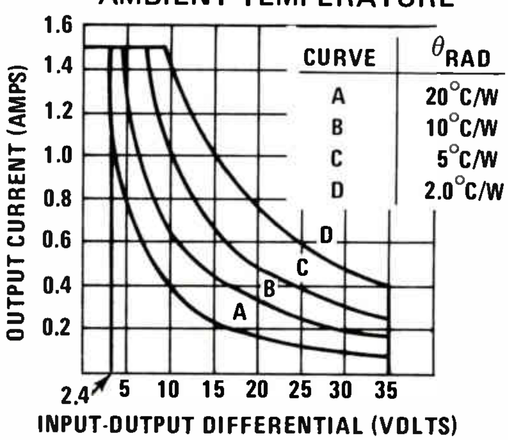
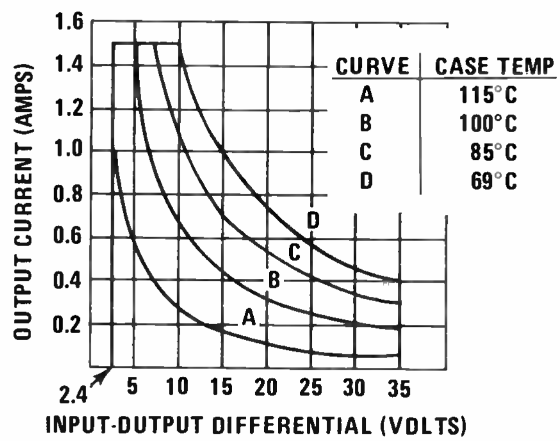


FIG. 5 D.C. SAFE OPERATING AREA AS A FUNCTION OF HEATSINK TEMPERATURE



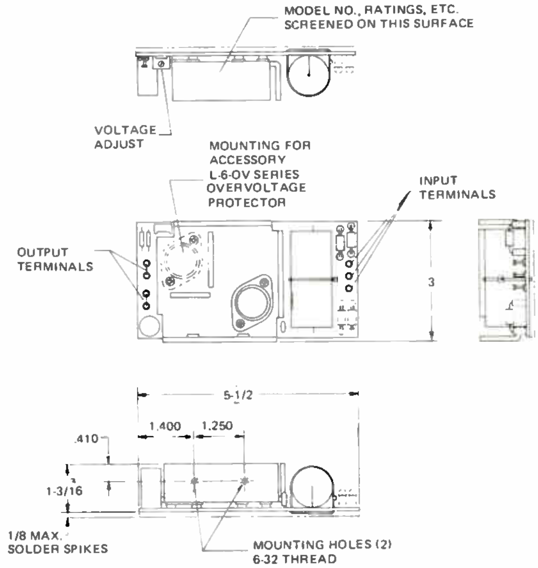
PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX
INPUT VOLTAGE	$V_{IN}DC$	$I_O = 3.0A$	$V_O + 3.3V$	SEE TABLE I
	$V_{IN}PKAC$	$I_O = 3.0A$	$\frac{V_O + 3.8V^{(1)}}{.85}$	SEE TABLE I
OUTPUT VOLTAGE	V_O		5V	28V
OUTPUT CURRENT	I_O			3.0A
CURRENT LIMIT KNEE	I_K	$V_{IN} = V_O + 5V$		4.5A
SHORT CIRCUIT CURRENT	I_{SC}	$V_{IN} = 25V$		2.0A
STANDBY CURRENT	I_Q	$V_{IN} = V_O + 5V$		25mA
STORAGE TEMPERATURE	T_S		-40°C	+85°C
AMBIENT OPERATING TEMPERATURE	T_A		0°C	65°C
LOAD REGULATION		$V_{IN} = V_O + 5VDC$, $\Delta I_O = 3.0A$		0.6% V_O
LINE REGULATION		$I_O = 2A$, $\Delta V_{IN} = 3.5$ VDC		1.0% V_O
PROGRAMMING RESISTANCE	R_P			200Ω/V
PROGRAMMING VOLTAGE	V_P			IV/V
TEMPERATURE COEFFICIENT	T.C.	$V_{IN} = V_O + 5V$, $I_O = 5mA$		0.03% V_O/°C
RIPPLE AND NOISE				SEE FIGURE 3

(1) ASSUMES 60Hz INPUT LINE FREQUENCY AND A RECTIFICATION EFFICIENCY (V_{CF} AVG/V_{SEC}PK) = 85%

TABLE I

MODELS	$V_{IN}DC$ MAX	$V_{IN}PKAC$ MAX (NO LD.)	INPUT CAP. (μf)
LSS-60-01	16.5V	18.5V	6.6K
LSS-60-02	25.5V	29V	4.4K
LSS-60-03	40V	40V	2.8K



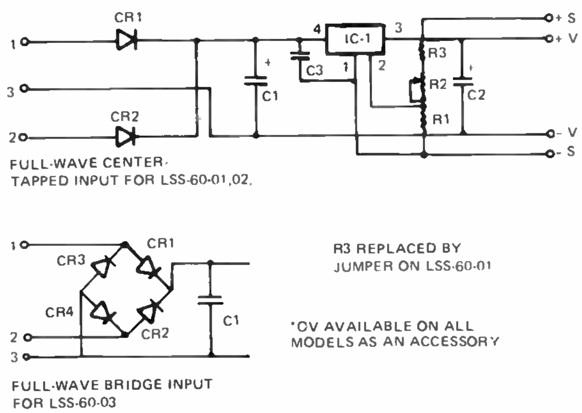
OUTLINE DRAWING

DESIGN EXAMPLE

Requirements: $V_O = 15V$ @ 1.0A
$T_A = 40°C$
Input Line Voltage = 117V_{RMS} ±10%, 60 Hz

1. For 15 volts at 1 AMP choose LSS-60-02.
2. From specification table, V_{IN} peak minimum =
$$\frac{V_O + 3.8}{.85} = \frac{15 + 3.8}{.85} = 22.1V$$
[Note that this assumes a rectification efficiency $\left(\frac{V_{AVG}}{V_{PEAK}}\right)$ of 85%]
3. From the transformer design, calculate V_{IN} peak maximum at high line. For this example, assume that V_{IN} peak maximum is 29.0 volts. Therefore $V_{AVG}MAX$ = 29.0 x .85 = 24.7V.
4. Compute the voltage differential (V_D) across the module as follows: $V_D = V_{AVG}MAX - V_O$
$V_D = 24.7 - 15 = 9.7V$
5. From design curve (Fig. 1) at $V_D = 9.7V$, $I_O = 1.0A$ and T_A=40°C, power dissipation (P_D) = $V_D \times I_O$ = 9.7W and the thermal impedance of the required heat sink (θ RAD) is 6.5°C/W. This corresponds to an absolute heat sink temperature of 105°C.

Note: For DC input in the above example, V_{IN} minimum would be V_O + 3.3V (from specification table) and $V_{AVG}MAX$ would be $V_{IN}MAX$-1.



SCHEMATIC DIAGRAM

OPERATIONAL DATA

FIG. 1 POWER DISSIPATION VS. INPUT-OUTPUT DIFFERENTIAL
POWER DISSIPATION VS. RADIATOR THERMAL
IMPEDANCE FOR VARIOUS OUTPUT CURRENTS

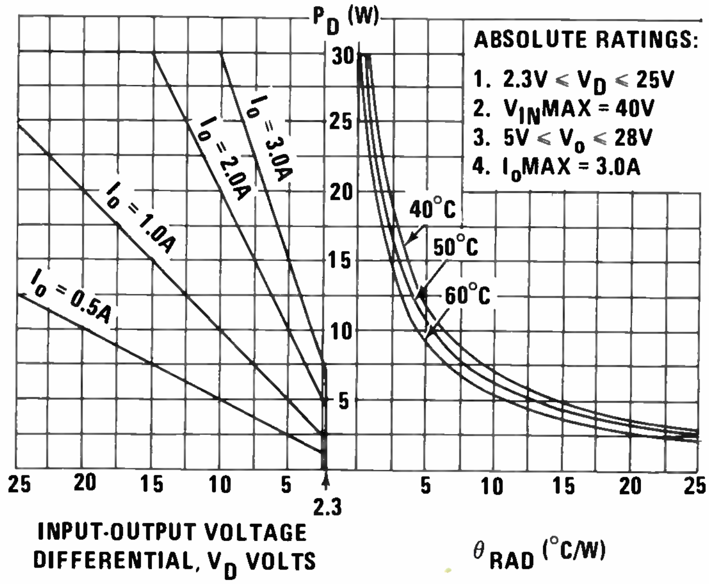


FIG. 2 POWER DERATING CURVE AS A FUNCTION OF HEAT SINK TEMPERATURE

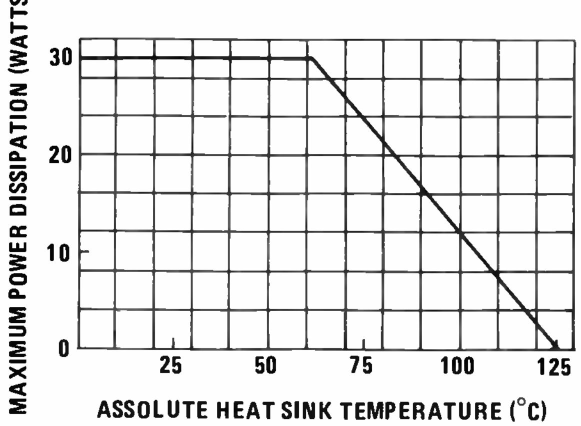


FIG. 3 OUTPUT RIPPLE AS A FUNCTION OF OUTPUT VOLTAGE WITH 3V PK-PK INPUT RIPPLE @ 120 HZ

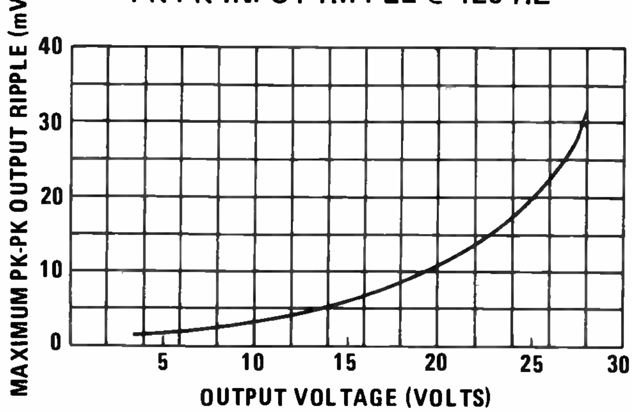


FIG. 4 DC SAFE OPERATING AREA AS A FUNCTION OF HEAT SINK THERMAL IMPEDANCE TO AIR AT 40°C AMBIENT TEMPERATURE

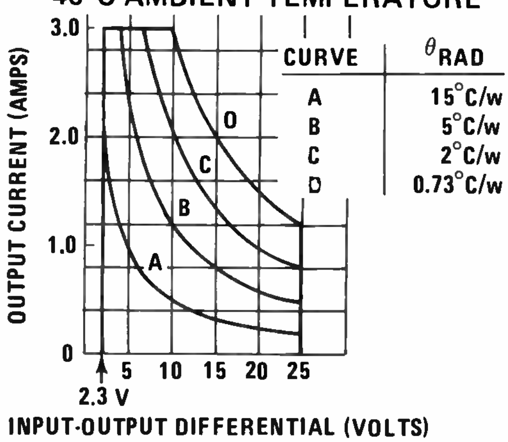
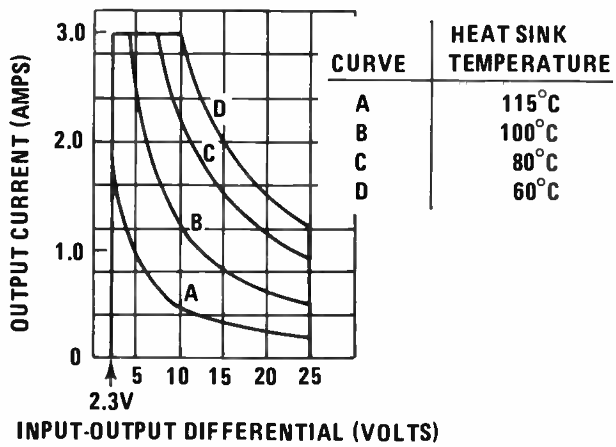


FIG. 5 DC SAFE OPERATING AREA AS A FUNCTION OF HEAT SINK TEMPERATURE



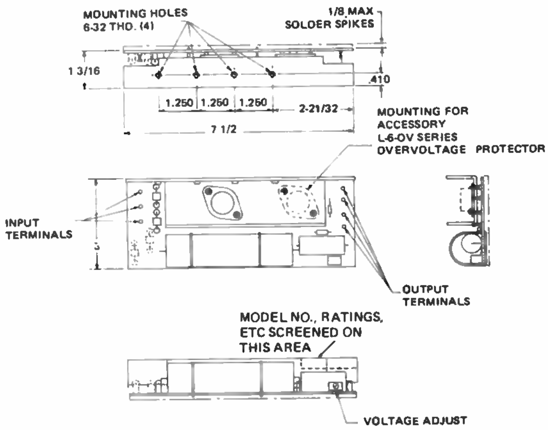
PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX
INPUT VOLTAGE	$V_{IN}DC$	$I_o = 5.0A$	$V_O + 3.6V$	SEE TABLE I
	$V_{IN}PKAC$	$I_o = 5.0A$	$\frac{V_o + 4.1V^{(1)}}{.85}$	SEE TABLE I
OUTPUT VOLTAGE	V_o		5V	28V
OUTPUT CURRENT	I_o			5.0A
CURRENT LIMIT KNEE	I_K	$V_{IN} = V_o + 5V$		6.5A
SHORT CIRCUIT CURRENT	I_{SC}	$V_{IN} = 25V$		2.0A
STANDBY CURRENT	I_Q	$V_{IN} = V_o + 3V$		25mA
STORAGE TEMPERATURE	T_S		-40°C	+85°C
AMBIENT OPERATING TEMPERATURE	T_A		0°C	65°C
LOAD REGULATION		$V_{IN} = V_o + 5VDC$, $\Delta I_o = 4.95A$		0.6% V_o
LINE REGULATION		$I_o = 5.0A$, $\Delta V_{IN} = 4.5VDC$		0.5% V_o
PROGRAMMING RESISTANCE	R_P			200Ω/V
PROGRAMMING VOLTAGE	V_P			1V/V
TEMPERATURE COEFFICIENT	T.C.	$V_{IN} = V_o + 3V$, $I_o = 100mA$		0.02% V_o/°C
RIPPLE AND NOISE				SEE FIGURE 3

(1) ASSUMES 60Hz INPUT LINE FREQUENCY AND A RECTIFICATION EFFICIENCY (V_{CF} AVG/V_{SEC}PK) = 85%

TABLE I

MODELS	V_{IN}DC MAX	V_{IN}PKAC MAX (NO LD.)	INPUT CAP (µf)
LSS-70-01	16.5V	18.5V	15K
LSS-70-02	25.5V	29V	10K
LSS-70-03	35V	35V	5.2K



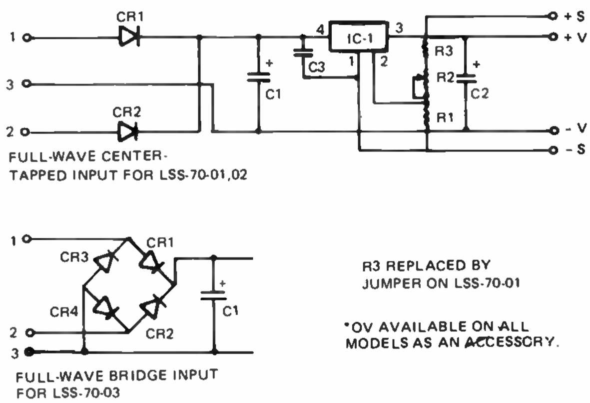
OUTLINE DRAWING

DESIGN EXAMPLE

Requirements: V_o = 9V @ 2.0A
T_A = 60°C
Input Line Voltage = 117V_{RMS} ±10%, 60 Hz

1. For 9 volts at 2.0 AMPS, choose LSS-70-02.
2. From specification table, V_{IN} peak minimum =
   $$\frac{V_o + 4.1}{.85} = \frac{9 + 4.1}{.85} = 15.5V$$
   [Note that this assumes a rectification efficiency $\left(\frac{V_{AVG}}{V_{PEAK}}\right)$ of 85%]
3. From the transformer design, calculate V_{IN} peak maximum at high line. For this example, assume that V_{IN} peak maximum is 21.0 volts. Therefore $V_{AVG}MAX$ = 21.0 x .85 = 17.85V.
4. Compute the voltage differential (V_D) across the module as follows: $V_D = V_{AVG}MAX - V_o$
   V_D = 17.85 - 9 = 8.85V
5. From design curve (Fig. 1) at V_D = 8.85V, I_o = 2.0A and T_A = 60°C, power dissipation (P_D) = V_D x I_o = 17.7W and the thermal impedance of the required heat sink (θ_{RAD}) is 2.35° C/W. This corresponds to an absolute heat sink temperature of 100.5°C.

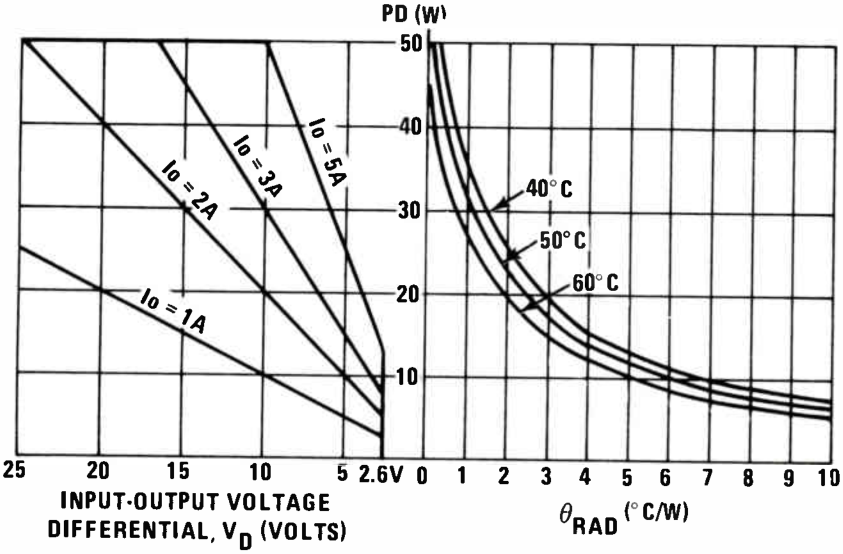
Note: For DC input in the above example, V_{IN} minimum would be V_o + 3.6V (from specification table) and $V_{AVG}MAX$ would be $V_{IN}MAX-1$.



SCHEMATIC DIAGRAM

OPERATIONAL DATA

FIG. 1 POWER DISSIPATION VS INPUT-OUTPUT DIFFERENTIAL
POWER DISSIPATION VS RADIATOR THERMAL
IMPEDANCE FOR VARIOUS OUTPUT CURRENTS



ABSDLUTE RATINGS:

1. 2.6V ≤ V_D ≤ 25V
2. V_{IN} MAX = 35V
3. 5V ≤ Vo ≤ 28V
4. I_o MAX = 5.0A

FIG. 2 POWER DERATING
CURVE AS A FUNCTION OF
HEAT SINK TEMPERATURE

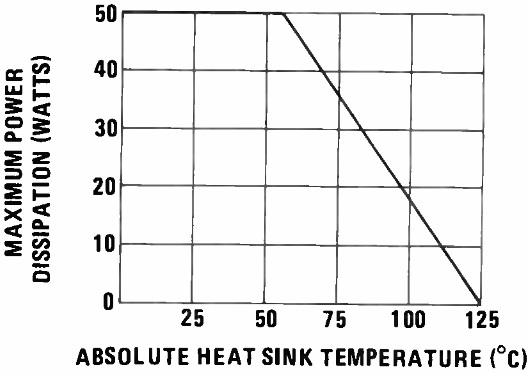


FIG. 3 OUTPUT RIPPLE AS A FUNCTION
OF OUTPUT VOLTAGE WITH 3V
PK-PK INPUT RIPPLE @ 120 Hz

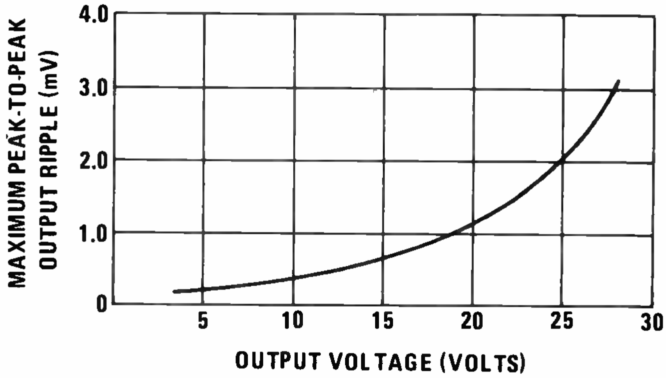


FIG. 4 DC SAFE OPERATING AREA AS A
FUNCTION OF HEAT SINK THERMAL IMPEDANCE
TO AIR AT 40°C AMBIENT TEMPERATURE

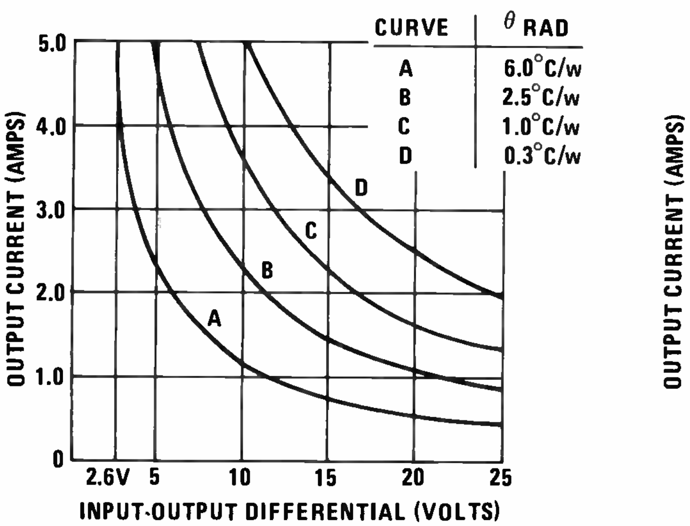
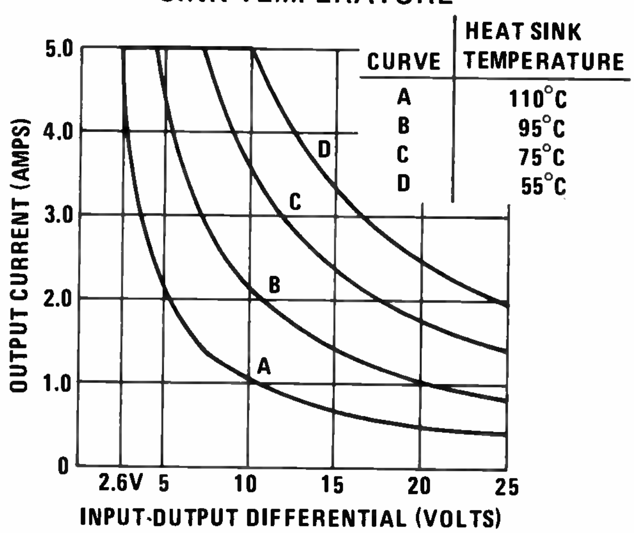


FIG. 5 DC SAFE OPERATING AREA
AS A FUNCTION OF HEAT
SINK TEMPERATURE



PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX
INPUT VOLTAGE	$V_{IN}DC$ $V_{IN}PKAC$		$V_O + 6.2V$ $\frac{V_O + 4.0V^{(1)}}{.85}$ (3)	SEE TABLE I SEE TABLE I
OUTPUT VOLTAGE	V_O		4.75V	29.4V
OUTPUT CURRENT	I_O			10.0A
CURRENT LIMIT KNEE (4)	I_K		9.8A	13.5A
SHORT CIRCUIT CURRENT (4)	I_{SC}		2.1A	3.0A
STANDBY CURRENT	I_Q			31mA
STORAGE TEMPERATURE	T_S		-40°C	+85°C
AMBIENT OPERATING TEMPERATURE	T_A		0°C	65°C
LOAD REGULATION		V_{IN} = CONSTANT $\Delta I_O = 10A$		0.2%
LINE REGULATION		$I_O = 10A$ $\Delta V_{IN} = V_{IN}MAX - V_{IN}MIN$		0.01% $V_O/\Delta V_{IN}$
PROGRAMMING RESISTANCE	R_P			200Ω/V
PROGRAMMING VOLTAGE	V_P			1V/V
TEMPERATURE COEFFICIENT	T.C.			0.015% V_O/°C
RIPPLE AND NOISE			60dB (2)	

(2) 54dB MINIMUM FOR 24V AND 28V MODELS (3) $V_{IN}PKACMIN = \frac{V_O + 6.7V}{.85}$ FOR LSS-80-24 AND LSS-80-28

(1) ASSUMES 60Hz INPUT LINE FREQUENCY AND A RECTIFICATION EFFICIENCY ($V_CFAVG/V_{SEC}PK$) =85%

TABLE I

MODELS	$V_{IN}DC$ MAX	$V_{IN}PKAC$ MAX (NO LD.)	INPUT CAP (μf)
LSS-80-5	16.5V	18.5V	20K
LSS-80-6	16.5V	18.5V	20K
LSS-80-12	25.5V	29V	14K
LSS-80-15	25.5V	29V	14K
LSS-80-24	40V	40V	10K
LSS-80-28	40V	40V	10K

(4) MAX VALUE APPLIES TO LSS-80-5; MIN VALUE APPLIES TO LSS-80-28

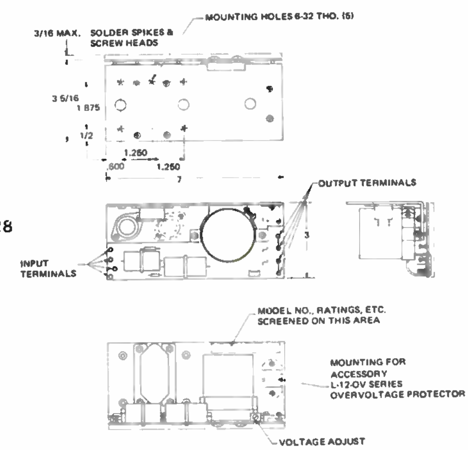
DESIGN EXAMPLE

Requirements: V_O = 24V @ 4.0A
T_A = 40°C
Input Line Voltage = 117V_{RMS} ±10%*, 60 Hz

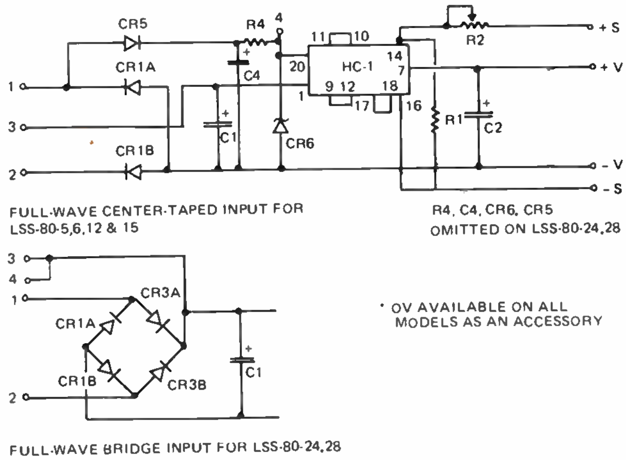
1. For 24 volts at 4 AMPS, choose LSS-80-24.
2. From specification table, V_{IN} peak minimum = $\frac{V_O + 6.7}{.85} = \frac{24 + 6.7}{.85} = 36.1V$
   [Note that this assumes a rectification efficiency $\left(\frac{V_{AVG}}{V_{PEAK}}\right)$ of 85%]
3. From the transformer design, calculate V_{IN} peak maximum at high line. For this example, assume that V_{IN} peak maximum is 40.0* volts. Therefore $V_{AVG}MAX$ = 40 x .85 = 34V.
   [Note that the maximum input voltage is 40V]
4. Compute the voltage differential (V_D) across the module as follows: $V_D = V_{AVG}MAX - V_O$
   $V_D = 34 - 24 = 10V$
5. From design curve (Fig. 1) at V_D = 10V, I_O = 4A and T_A = 40°C, power dissipation (P_D) = $V_D \times I_O$ = 40W and the thermal impedance of the required heat sink (θ_{RAD}) is 1.8°C/W. This corresponds to an absolute heat sink temperature of 150°C.

Note: For DC input in the above example, V_{IN} minimum would be V_O +6.2V (from specification table) and $V_{AVG}MAX$ would be $V_{IN}MAX$-1.

*Note that this value of peak input voltage requires restricted line swing



OUTLINE DRAWING



SCHEMATIC DIAGRAM

OPERATIONAL DATA

FIG. 1 POWER DISSIPATION VS INPUT-OUTPUT DIFFERENTIAL
POWER DISSIPATION VS RADIATOR THERMAL IMPEDANCE
FOR VARIOUS OUTPUT CURRENTS

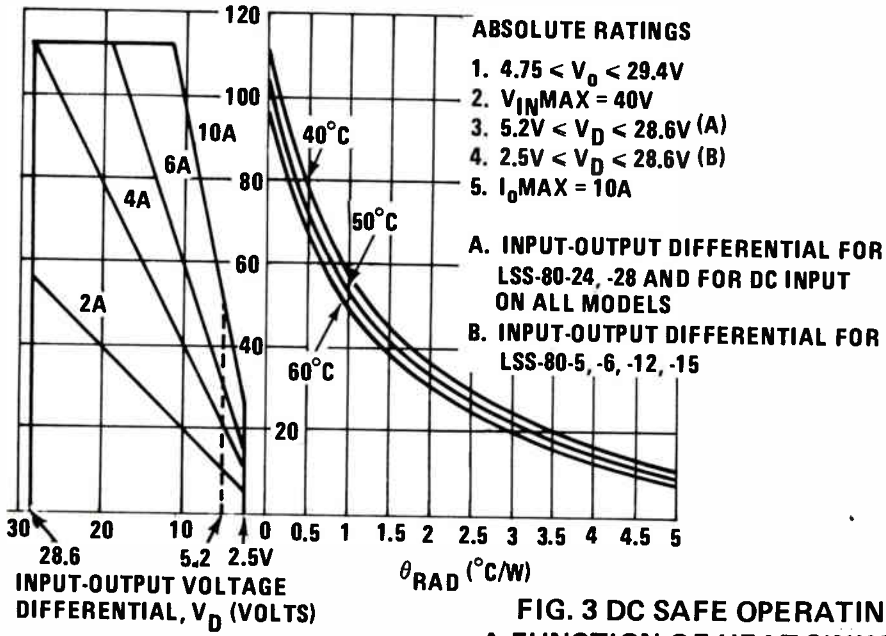


FIG. 2 POWER DERATING CURVE AS A FUNCTION OF HEAT SINK TEMPERATURE

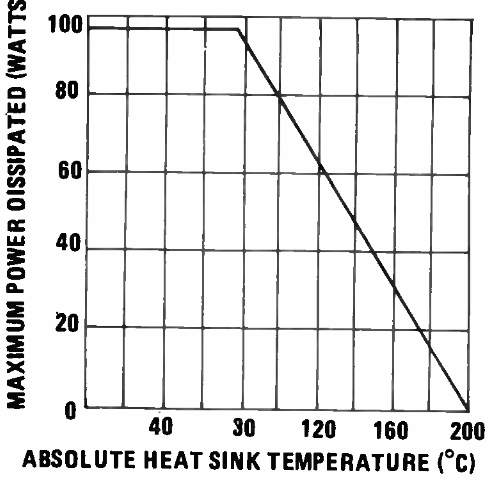


FIG. 3 DC SAFE OPERATING AREA AS A FUNCTION OF HEAT SINK TEMPERATURE

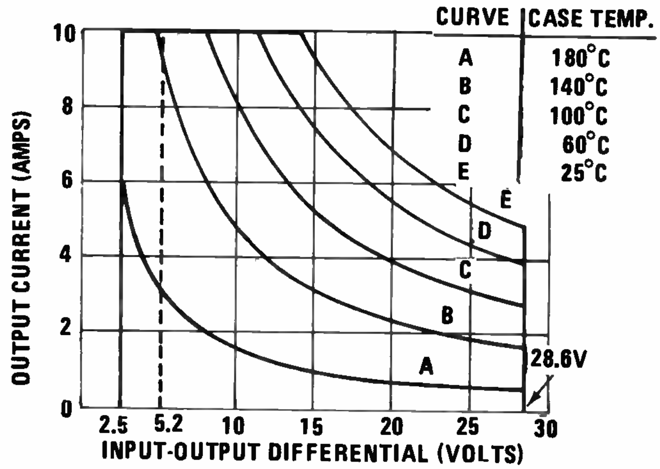
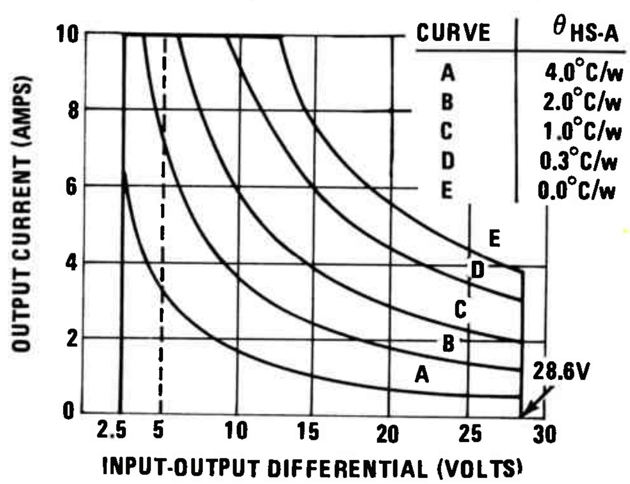


FIG. 4 DC SAFE OPERATING AREA AS A FUNCTION OF HEAT SINK THERMAL RESISTANCE TO AIR AT 40°C AMBIENT TEMPERATURE



New products

Instruments

100-MHz analyzer dedicates keys to ease operation

Logic-state analyzers, while not the most expensive of instruments, are far from cheap. So it behooves would-be purchasers to shop for one that will not become obsolete as microprocessor clock rates double over the next few years. Perhaps that is why so many window shoppers at last month's Wescon could be found eyeing the K100-D. Not only does the instrument offer both time- and data-domain analysis techniques in a single package, but it accepts 16 inputs at rates up to 100 MHz.

Besides providing for the future with fast clock rates and data analysis capabilities of up to 32 bits, the designers of the MC6800-based K100-D have kept the measurement realities of the present in mind and paid particular attention to the configuration of the unit's front panel. While it is always tempting with a microprocessor-based instrument to let the chip handle everything, leaving the operator with a few front-panel pushbuttons and months of operating-manual study, this route was avoided. Instead, the unit has many keys that each handle a few functions at most. These functions are displayed on a simple menu after the unit has been powered up and has performed self-diagnostics.

Entering the appropriate data on the menu allows the operator to record selectively the various strings of data he wishes to examine in the analyzer's 16-by-1,024-bit memory. Through proper selection of arm mode, enable and trigger words and qualifiers, and trigger delay (which may be specified in terms of events or clock cycles), users can enter nested sequences at the point of interest. The information recorded may then be displayed in, say, the time domain and thoroughly examined with cursors and scale expanders controlled by keys. Once captured, the information can be shifted to a second 16-by-1,024-bit memory, tests repeated, and the two sets of data compared manually or automatically.

In the data domain, information can be displayed in hexadecimal, octal, binary, or even ASCII format. The K100-D also can identify the number of times the same address occurs within a loop, indicating the first and last occurrence and the number of events stored in memory.

The unit's probe has also been carefully designed, since reflection, ringing, changing input capacitance, and crosstalk can become major problems at 100 MHz. The unit comes with individual active probes, allowing users freedom in placing them while preserving signal information integrity in the same manner as active probe pods.

The entire K100-D, including two 10-probe sets and an operating and maintenance manual, is priced at $8,800.

Biomation Corp., 4600 Old Ironsides Dr., Santa Clara, Calif. 95050. Phone Dave Blecki at (408) 988-6800 [353]

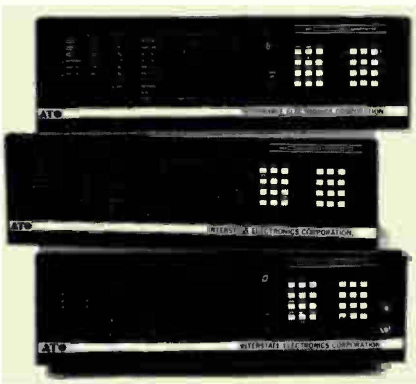
Pulse-function generators are microprocessor-based

In addition to creating totally new markets in the electronics industry, microprocessors are rejuvenating product areas that have been considered fully matured. Eyeing one such area, Interstate Electronics Corp. hopes to leapfrog competitors with its microprocessor-based programmable pulse and function generators.

Unveiled at last month's Wescon, the first three members of the family offer extended performance features and lower prices than comparable competing models, according to test equipment products marketing manager Donald O. Leach. All three models operate on the IEEE-488 bus at state-of-the-art rates, he notes, citing an average handshaking time of 1.25 μs. The instruments can also work directly in ASCII format.

At the line's low end is the $2,295, 14-MHz model 820, a programmable generator offering sine-wave, square-wave, ramp, triangle, and dc functions, as well as trigger and offset capabilities. For $700 more, the model 845 additionally provides true pulse and crystal-referenced clock frequencies together with programmability of pulse delay, width, offset, amplitude, and mode.

Topping the line is the 0.01-Hz-



to-20-MHz model 860, which sells for $3,995. Noting that it has all the features of the other models and higher frequency, Leach characterizes the unit as "particularly valuable to high-speed testing of digital hybrid circuits." Microprocessor control provides store, recall, and learn modes for up to 20 sets of programmed parameters. The store and recall capability of the model 860 makes it convenient for such repetitive operations as incoming inspection testing. Furthermore, its battery-supported complementary-metal-oxide-semiconductor memory retains stored information for more than a month when power is off.

All units are available from stock.

Interstate Electronics Corp., 707 E. Vermont Ave., P. O. Box 3117, Anaheim, Calif. 92803. Phone (714) 772-2811 [354]

3½-digit phasemeter tends to its own needs

The ultimate solution to simplifying the design of front-panel controls is offered by the model 6200A phase-

meter. The 3½-digit instrument is fully automatic, needing no adjustment by the operator. Measuring differences in phase angle for both sine and square waveforms in the frequency range of 10 Hz to 1 MHz, the unit is accurate to within 0.5° and can resolve 0.1°.

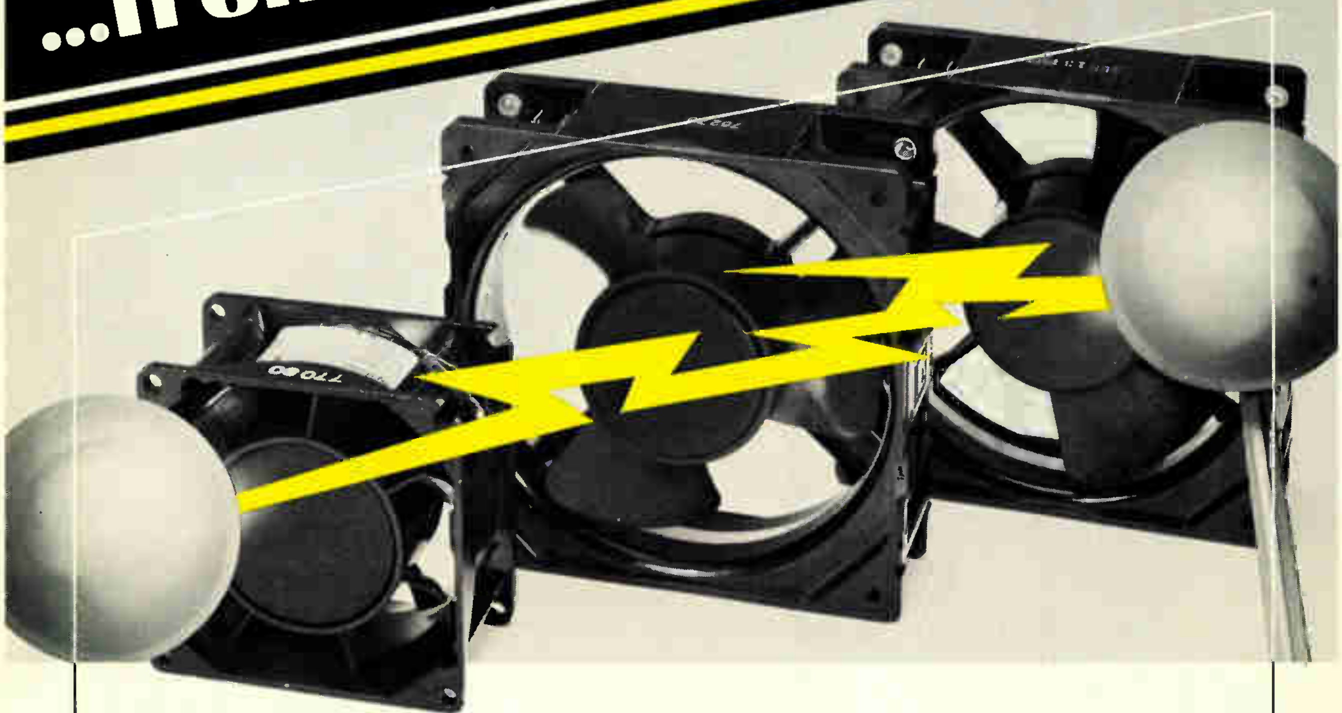
The unit will accept reference and measurement inputs having voltages between 0.1 and 120 V rms. In addition to its display, the unit has an analog output and, optionally, a binary-coded-decimal output. The self-sufficient 6200A is priced at only $795.

Krohn-Hite Corp., Avon Industrial Park, Bodwell St., Avon, Mass. 02322. Phone (617) 580-1660 [355]

Logic generator tests multichannel devices

Designed for functional testing of multichannel hardware, the model 8170A programmable data generator works with 512-by-16-bit and 1,024-by-8-bit systems and is optionally expandable for systems twice as large. The instrument can be programmed to produce output data in binary, octal, or hexadecimal format; data, memory address, and operating modes may be entered using one or more of these formats at

Revolting developments ...from Rotron



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4572

Products newsletter

A-d converter mates with microprocessors

Interfacing microprocessors with the analog world keeps getting easier. The latest evidence of this fact is the AD574 analog-to-digital converter from Analog Devices Inc., Norwood, Mass. The 12-bit device, which is contained in a 28-pin ceramic DIP, **offers three-state output buffer circuitry for direct coupling to 8-, 12-, or 16-bit buses.** The converter comprises two chips—the AD565 d-a converter, which includes a voltage reference, and a control chip that includes an integrated-injection-logic successive-approximation register, the system clock, a latching comparator, and the bus interface. The d-a chip also includes high-speed current switches, a thin-film resistor network, a buried zener reference, and input-scaling and bipolar offset resistors. It settles to within ½ least significant bit in 200 ns.

Low-noise generator stores 10 setups

Hewlett-Packard Co., Palo Alto, Calif., is readying a 1.28-GHz synthesized signal generator that allows the operator to preprogram 10 complete front-panel setups and recall them as needed. The low-noise, microprocessor-based model 8662A can perform precision digital sweeps and **has a maximum amplitude error of ±1 dB.**

Bright LEDs may show up in many places

Plessey Ltd.'s Optoelectronics and Microwave Group, Towcester, England, plans to try to find major new applications for its special avionics light-emitting diodes. The gallium-phosphide devices are visible in the 100,000-lux light levels typically encountered by airplane pilots flying in direct sunlight above the clouds. The company is committing $2.4 million to a production and marketing program **that includes an automated line for the assembly of standard and custom displays.** To its family of standard displays, the company is adding its first alphanumeric unit—a five-by-seven-dot matrix with a 6.5-mm bright-yellow character housed in a stackable ceramic package. The high-reliability unit will sell in the U. K. for $33.64 each in quantities of 100 and more. Plessey says custom designs are undergoing tests in automobiles, heavy vehicles, and factories.

NEC makes Intel's one-chippers

NEC Microcomputers Inc. is offering immediate delivery of its fully compatible versions of Intel 8035 and 8048 single-chip 8-bit microcomputers. **The μPD8048 has 1,024 bytes of read-only memory** and 64 bytes of random-access memory, 27 input/output lines, an 8-bit counter-timer, and oscillator and clock circuitry. The μPD8035 is the same except that it has no on-board ROM. The Wellesley, Mass., subsidiary of Nippon Electric Corp. plans to offer its μPD8748 equivalent of Intel's 8748 erasable programmable ROM before the year's end.

V-f converter spans 100 dB

Raytheon's Semiconductor division in Mountain View, Calif., is introducing a voltage-to-frequency converter chip, which includes an ion-implanted, buried zener diode reference and a high-gain operational amplifier. Called the RC 4153, the converter has a **dynamic range in excess of 100 dB, a top frequency of 250 kHz, and a 100-piece price of $3.25.**

Sorry, wrong number

In our write-up of the meta assembler offered by Step Engineering Inc., Sunnyvale, Calif., on p. 238 of our Aug. 31 issue, the telephone number appeared incorrectly. **The correct number is (408) 733-7837.**

New products/materials

A protective coating, for application to printed-circuit boards after soldering, will prevent atmospheric oxidation and contamination from affecting the circuit and soldered joints. Multicore PC 52 will also isolate and protect the metallic surfaces from humidity changes that can cause current leakage. The material meets the climatic require-

ments of MIL-S-6872A and has low oxygen absorption and high humidity resistance. It can be sprayed or brushed on and, when applied properly, will not discolor or crack. Storage life at room temperature is indefinite. Multicore PC 52 sells for $7 for 1 qt or for a 16-oz spray.

Multicore Solders, South Service Road, Westbury, N. Y. [476]

An aluminum finish can be applied to electrical and electronic components such as connectors, switches, and lamp sockets. It has good corrosion resistance and will not insulate the devices as anodizing does. Besides these properties, Decoral has good lubricity and heat resistance. Products can be immersed in the aluminum paint at room temperature with no need for electroplating. It comes in a wide range of colors, making it

useful as a coding material.

The Lea Manufacturing Co., Chemical Finishes Division, 55 Commercial St., Medford, Mass. 02155 [477]

Ceramic-coated steel substrates, ranging in size from 1 by 2 in. to 4 by 4 in., are packaged in evaluation kits of 100 samples. The kits will introduce engineering and production personnel to Alphamet's use in the design and manufacture of both printed-circuit boards and hybrid circuits. The material can be drilled, punched, coined, and put through any other metalworking process before ceramic coating. Alphamet has the wave-soldering capability of conventional resin-glass laminates, yet can be economically printed with thick-film components. With the use of insulating glass and crossover circuits, the substrate can also provide the equivalent circuit density of multilayer constructions. The kit includes data sheets, applications bulletins, and a sample of the firm's resistor test pattern.

Alpha Metals Inc., 57 Freeman St., Newark, N. J. 07105 [478]

Air-shrinkable hypalon sleeving can withstand a temperature range from −35° to +150°C, making it useful for a variety of applications. The tubing is first dilated by use of a chemical agent, Hypasol, and is then packaged. Once removed, Hyp-150 tubing shrinks due to evaporation of the solvent to no more than 101% and no less than 90% of its specified length. While the material is recovering, it can be stretched to 3 times its recovered size for 15 minutes; at 20 to 30 minutes, flexibility varies. The material has a minimum tensile strength of 2,000 lb/in.^{2} and a minimum elongation of 400%. It exhibits good electrical properties as well, with a dielectric strength of 500 v/mil and a volume resistivity of 10^{14} ohm-cm. The recovered sleeve retains most of its original properties, even after long-term exposure to various types of chemicals including acids, alkalis, hydraulic fluid, and gasoline.

Insulation Systems Inc., 1233 Reamwood Ave., Sunnyvale, Calif. 94086 [479]

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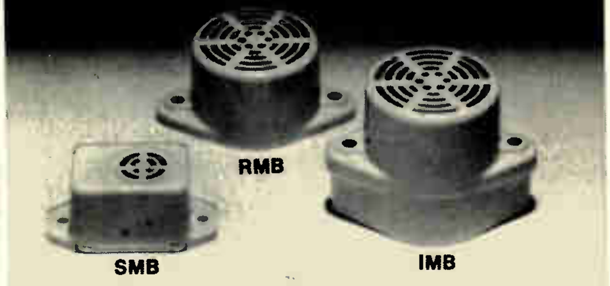
(Write for new catalog.)



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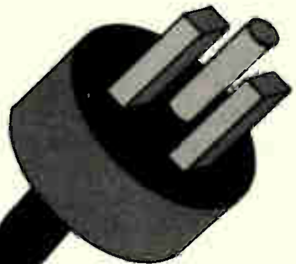

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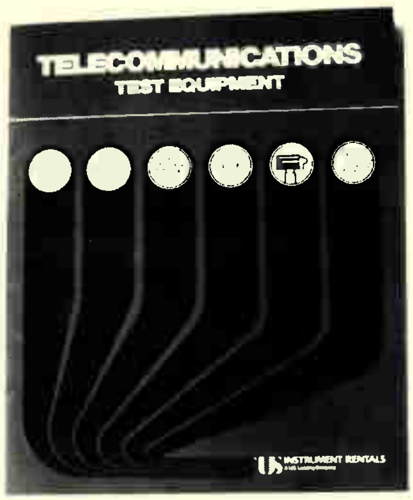
New literature

Communications. Descriptions and specifications are provided for a line of broadband signal-processing components that cover the frequency range from 10 kilohertz to 2,000 megahertz. Among devices dealt with by the 70-page catalog are power dividers, mixers, and phase shifters. Werlatone Inc., P. O. Box 258, Brewster, N. Y. 10509. Circle reader service number 421.

Rentals. "Telecommunications Test Equipment" will interest those who need equipment for microwave transmission, mobile radio, carrier, computer protocol, data communications, and cable fault applications. The catalog points out the advantages of renting telecommunications equipment and describes numerous rental and leasing plans. United States Instrumental Rentals Inc., 951 Industrial Rd., San Carlos, Calif. 94070 [423]



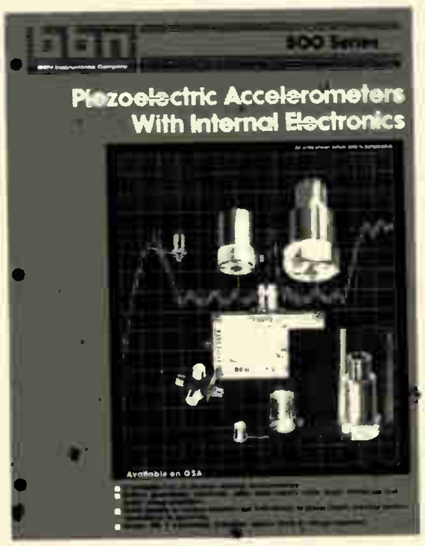
Filtration and separation. "Basics of Filtration and Separation" explains fluid-flow principles to those whose knowledge of them is limited. The 70-page handbook discusses centrifugal separation and filtration and various types of filter media and filter aids. It compares depth filters with microfiltration membranes. How to perform membrane separation through dialysis, electrodialysis, reverse osmosis, and ultrafiltration is also covered. The throughput and flow-rate factors in microfiltration

New literature

are discussed in detail. A glossary of terms is included. Copies of the handbook are available from Nuclepore Corp., 7035 Commerce Circle, Pleasanton, Calif. 94566 [422].

Flashtubes and coils. Designed for use by original-equipment manufacturers, this 12-page catalog offers specifications and detailed information on several types of tubes and coils. The major factors affecting the performance and life of a flashtube are discussed, including light intensity, light spectrum, pulse duration, operating voltage, and operation in total darkness. Flashtube and trigger-coil drawings and data for each device are also given. Mura Corp., 177 Cantiague Rock Rd., Westbury, N. Y. 11590 [424]

Accelerometers. "Piezoelectric Accelerometers With Internal Electronics," an eight-page catalog, contains information and specifications on seven types of accelerometers,



with particular emphasis on the ones with built-in preamplifiers. Four types of power supplies that provide a general-purpose interface between the accelerometers and other devices are discussed as well. BBN Instruments Co., 50 Moulton St., Cambridge, Mass. 02138 [425]

Optical-fiber evaluation. "Keeping Pace With Changing Needs In Optical Fiber Evaluation" explains

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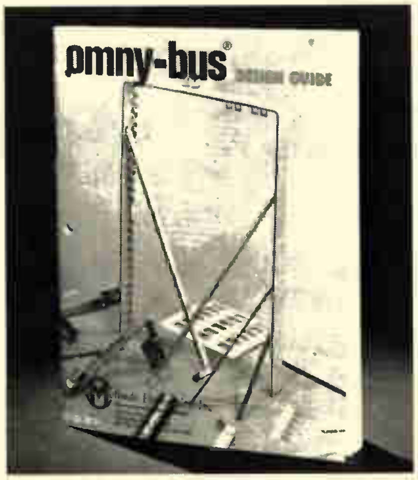
New literature

how to obtain performance parameters with the Digital Processing Oscilloscope system, which consists of a digitizing oscilloscope, a controller, and Basic software. The concept note describes how to measure numerical aperture and spectral attenuation and how to obtain data for determining pulse spreading, frequency response, and impulse response. Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077 [426]

Bus bars. More than 60 different bus-bar designs for ground and power- and signal-distribution systems are presented in a 48-page design guide. Specifications are



listed for printed-circuit, solderless-wrap, telecommunications, power-distribution, jumper, and flexible bus bars. Dimensional tolerance guidelines are also included. Methode Electronics Inc., Interconnect Products Division, 1700 Hicks Rd., Rolling Meadows, Ill. 60008 [427]

Wire and cable. "Product & Technical Handbook," a 235-page book, contains information about the high-temperature wire and cable industry. Various products are listed, wire- and cable-engineering data and other technical information given, and charts and tables provided, as well as specification references. The book costs $3 plus shipping charges. Order from Department T of Tensolite Co., Division of Carlisle Corp., Old Post Road-Route 9A, Buchanan, N. Y. 10511

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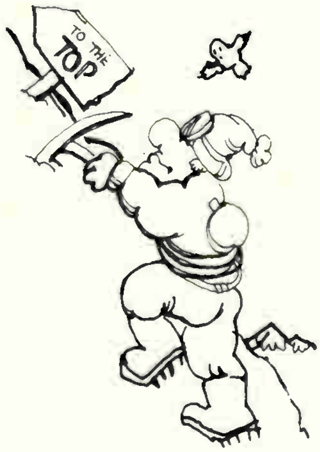

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Develop mathematical models for microwave, millimeter wave, laser, and IR hardware components and seeker configurations. Define test programs to validate models and assess guidance system performance.

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- Microprocessors
- Software development
- Signal processing
- Digital systems
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- Radar Systems
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NOTE: Candidates with less than 3 years experience in the areas of signal processing, pattern recognition, digital electronics, systems analysis optics and solid state electronic components are invited to apply and will be considered for the grade level for which qualified.

This is a career Civil Service position with all the normal fringe benefits. Travel and transportation expenses, including shipping of household goods, will be paid for the selected applicant.

Interested applicant should submit Standard Form 171, Personal Qualifications Statement, or detailed resume to:

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Grumman Aerospace Corporation has an immediate opening for an Electronic Engineer with a B.S./M.S. in Electrical Engineering, Physics or Electro-physics. Two to five years experience in the design, development, test and integration of various types of antenna and related microwave components into aircraft and space vehicles is also required.

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If you have a BS or MS in Electrical Engineering and at least four years of experience as described above, please forward your resume to Ed Connelley, Polaroid Corp., 565 Technology Square, Dept. 24, Cambridge, MA 02139.

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(ELECTRONICS)

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- Advanced signal processing techniques
- Classical or modern control theory
- Target signature analysis
- Optical design/analysis
- Pattern recognition
- Real time software design
- Waveform analysis
- Kalman filter and estimation theory

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Experienced in microwave circuit design. Duties will involve Circuit Analysis/Design for automatic test station and writing programs for automatic test units and circuit subassemblies. A background on equipment operating at frequencies up to 16 GHz is desirable.

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- Experience in digital/logic and analog circuit design. To perform digital and analog circuit analysis/design for an automatic test circuit cards. Power supply design/analysis experience desired for some positions.
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With recent relevant experience in the design and development of RF/IF, digital, or analog circuits for missle guidance systems. MSEE, software/hardware integration experience also desirable. Must be familiar with applicable state-of-the-art components—phase and frequency lock loops, wide and narrow receivers, use of microprocessors.

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These positions require system engineering for missile systems using radar and electro-optical technologies. This includes defining design characteristics, interfaces, test requirements, and performing trade studies. Weapons experience not required, but previous systems engineering, servo analysis, or circuit or logic design experience in the above technologies is desirable.

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To perform design and anlaysis for state-of-the art electro-optical missile seekers. Job assignments require ability to develop mathematical models for missile guidance systems performance evaluation. Proficiency in advanced one and two-dimensional signal processing techniques desired.

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To participate in digital systems analysis and designer trade offs on RF components, subsystems and systems. Write design requirements, specifications and test requirements. Do RF modeling, hybrid missile flight simulation. Knowledge of Machine Languages, Basic and Fortran. Familiarity with microprocessor use in analytical and control systems. Interface equipment to systems.

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SOFTWARE DEVELOPMENT ENGINEER

Candidate should possess a Bachelor's Degree. Will be responsible for organization and technical direction of microprocessor program development activities. Minimum of three (3) years of microcomputer program development and M-6500 or equivalent experience required.

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Engineers with a BS degree for field applications of advanced microcomputer systems. Primary activities include configuring the system hardware and software to meet customer requirements and train user personnel in the field. Minimum of four (4) years electronic experience required.

FIELD TECHNICIAN

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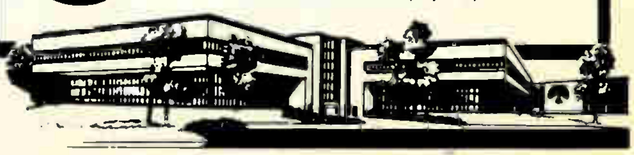

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